THE UNIVERSITY OF SHEFFIELD

Applications of GaN HFETs in UV detection and Power electronics

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Table of Contents

Abstract

Gallium nitride (GaN) has some unique material properties including direct band gap, ability to form a heterostructure resulting in two dimensional electron gas (2DEG) formation and a wide band gap (3.4eV) to offer high breakdown voltage. Such material properties make GaN extremely attractive for optoelectronics and power electronics applications. In this thesis, GaN HFETs applications as an Ultraviolet light detector and for power electronics sector are explored.

In comparison to other GaN based UV detectors, the AlGaN/GaN HFET is found to be ultra sensitive to UV illumination. A very high dc responsivity (~4.3×10^{7}A/W) value is reported and gain mechanisms in the devices are shown to be due to a photo voltage effect in both the AlGaN barrier layer and the GaN buffer region. Understanding of the gain mechanisms from this work will help optimise the design of the future UV photo detectors.

For power electronics applications, GaN HFETs grown on a Si substrate are characterized. To reduce buffer leakage both Iron (Fe) and Carbon (C)-doped structures are considered. The vertical leakage mechanism is identified as a Poole Frenkel emission process for both the Fe and C-doped structures. A novel method to reduce the gate leakage current in GaN HFETs is established by using surface chemical treatments. Sulfuric acid works by oxidizing the surface which has a strong passivating effect on the gate leakage current. The surface leakage mechanism is explained by a combination of Mott hopping and Poole Frenkel models.

The fluorine ion implant technique is used in GaN HFETs for the development of enhancement mode transistors required in power switching applications. The requirement for a +3V threshold voltage in the power electronics sector is met by combining the fluorine implant with a deposited dielectric layer under the gate. More efficient fluorine incorporation is observed in AlInN/GaN HFETs compared to conventional AlGaN/GaN HFETs. The recipe for fluorine implant in AlInN/GaN HFETs is also optimized to maintain high channel conductivity and transconductance.

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List of Publications

[1] Zaffar H. Zaidi and Peter A. Houston, "Highly Sensitive UV Detection Mechanism in AlGaN/GaN HEMTs," IEEE Transaction on Electron Devices, vol. 60, no.9, pp. 2776-2781, September, 2013.

[2] Z.H. Zaidi, K.B. Lee, I. Guiney, H. Qian, S. Jiang, D.J. Wallis, C.J. Humphreys and P.A. Houston, "Sulfuric Acid and Hydrogen Peroxide Surface Passivation Effects on AlGaN/GaN HEMTs," Journal of Applied Physics, 116, 244501, 2014.

[3] Z.H. Zaidi, K.B. Lee, I. Guiney, H. Qian, S. Jiang, D.J. Wallis, C.J. Humphreys and P.A. Houston, "Enhancement Mode operation in AlInN/GaN MISHEMTs on Si Substrates using Fluorine Implant," [In preparation].

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[1] Z.H. Zaidi, K.B. Lee, I. Guiney, H. Qian, S. Jiang, D.J. Wallis, C.J. Humphreys and P.A. Houston, "Enhancement Mode AlInN/GaN MISHEMTs using Fluorine Implant," 8th International Workshop on Nitride Semiconductors, Poland, Wroclaw, 24-29 August, 2014.

[2] Z.H. Zaidi, K.B. Lee, I. Guiney, H. Qian, S. Jiang, D.J. Wallis, C.J. Humphreys and P.A. Houston, "Effect of SiN Passivation and Chemical Treatments (H_2SO_4 and H_2O_2) on AlGaN/GaN HEMT on Silicon Substrates" 38th Workshop on Compound Semiconductor Devices and Integrated Circuits, Delphi, Greece, 18-20 June, 2014.

[3] Z.H. Zaidi, K.B. Lee, I. Guiney, H. Qian, S. Jiang, D.J. Wallis, C.J. Humphreys and P.A. Houston, "Normally-Off AlInN/GaN HEMTs on Si Substrate using Fluorine Implant," Uk Semiconductor Conference, Sheffield, United Kingdom, 8th and 9th July, 2014.

[4] Z.H. Zaidi, K.B. Lee, I. Guiney, H. Qian, S. Jiang, D.J. Wallis, C.J. Humphreys and P.A. Houston, "Enhancement Mode AlGaN/GaN MISHFETs using Fluorine implant and SiN_x," Uk Semiconductor Conference, Sheffield, United Kingdom, 3rd and 4th July, 2013.

[5] Z.H. Zaidi and P.A. Houston, "Highly Sensitive UV Detection in AlGaN/GaN High Electron Mobility Transistors," 6th Space Agency, MOD Workshop on Wideband gap Semiconductors and Components, Noordwijk, Netherlands, 8th and 9th October, 2013.

List of Figures

List of Tables

Chapter No 1: Introduction

1.1 Overview and Motivation

In the history of technology, microelectronics or semiconductor based industries are clearly dominated by silicon based devices. Silicon has displaced most materials in a wide range of applications and only been kept out of the race in optoelectronics where it cannot compete due to unsuitable material properties. The silicon dominance of the semiconductor industry can be attributed to its excellent material properties, mature processing techniques, lower cost, availability, presence of natural oxide and stable mechanical and thermal properties. The continuous scaling of Si CMOS (Complementary Metal Oxide Semiconductor) transistors has met the ever increasing requirements for speed and bandwidth with the 11nm node expected to launch in 2018. [1] However, further scaling of these devices would be difficult and there is a need for the higher frequency, higher temperature, and higher power operations with capabilities to work in the harsh environments which demand materials with superior properties.

The wide band gap semiconductors such as Gallium Nitride (GaN), Silicon Carbide (SiC) and Diamond are potential candidates for attaining superior and robust performances. The larger band gap implies an ability to handle higher electric fields before breakdown, thus enabling devices with higher operating voltages. The operation at elevated temperatures requires better thermal conductivity, so that more heat can be effectively radiated out of the device keeping lower device temperature and consequently reducing the cost and size of the cooling systems. Higher frequency and power performance are required in radar, microwave circuits, satellite communication and RF applications. These can be characterized by Johnson figure of merit [2], which is proportional to the electron saturation velocity and breakdown electric field. Therefore, materials with higher saturation velocity and breakdown electric field strength are required. The comparison of different material properties is shown in the table 1.1 [3-5] below.

Diamond appears to be the most attractive candidate for the modern semiconductor devices in the high frequency and power regime with its highest breakdown field, thermal conductivity and saturation velocity. However, there are many synthesis and fabrication problems associated with it, including finding appropriate n-type dopant, optimization of the growth technique, high contact resistance and surface state densities [6-7]. Recently GaN on diamond

devices have been reported to achieve a better thermal conductivity suitable for harsh environments [8-9] and may be further developed in the future.

Property	*Si*	*4H-SiC*	*GaN*	*GaAs*	*Diamond*
Bandgap energy E_g (eV)	1.12	3.26	3.45	1.43	5.45
Electric breakdown Field E_c(kV/cm)	300	2200	3300	400	10000
Electron mobility $\mu_n(cm^2/V.s)$	1500	1250	1250 (Bulk) 2000 (2DEG)	8500	2200
Thermal Conductivity λ (W/cm.K)	1.5	4.9	1.3	0.46	22
Saturated Electron drift velocity, v_{sat}(×10^7 cm/s)	1	2	2.2	1	2.7

Table 1.1 Comparison of material properties for different materials [3-5].

GaAs has overall good electron transport properties and offers excellent performance for high speed operation but these devices are not particularly suitable for power electronics applications due to lower breakdown strength, higher substrate cost and poor thermal conductivity compared to some other materials. SiC offers a mature technology with reasonable material properties. It has been extensively used in power electronics sector for more than a decade and with excellent thermal conductivity is all set to replace Si in power electronics. The major drawback of using SiC is its very high material cost and growth on smaller size substrates.

In the recent years, GaN has attracted major attention for both optoelectronics and electronics applications due to its superior material properties such as direct band gap, higher electric breakdown field strength, both higher electron mobility and saturation velocity, high melting point and the ability to form a heterostructure. The major advantage of using GaN and GaAs materials is the formation of the heterostructure which results in the creation of a two dimensional electron gas (2DEG), where energy states for electrons are quantized and electrons can only move laterally. Very high electron mobility [10] can be achieved in these devices, since carriers are screened from their respective donors, mitigating ionized impurity scattering. The ability to form a heterostructure and the fact that GaN can be grown on foreign, cheaper substrates such as Si gives it an upper hand in comparison with SiC.

The spontaneous polarization in GaN due to its wurtzite crystal structure, lack of inversion symmetry and piezoelectric polarization due to strain, are ten times higher than conventional III-V and Arsenide based materials [11-12]. The presence of these polarization effects in GaN makes it possible to fabricate devices without intentional doping of the upper wide band gap materials unlike AlGaAs/GaAs HFETs. This means further reduction in ionized impurity scattering and "on" state resistance with much improved carrier mobility. Due to these polarization effects the 2DEG sheet charge density in AlGaN/GaN heterostructure is about five times higher ($>1 \times 10^{13}$ cm^{-2}) than in doped AlGaAs/GaAs HFETs [13].

The figures of merit are most commonly quoted for applications in high power and high frequency operations to compare the relative strengths of different materials taking into account various material properties. The four most commonly quoted and regarded figures of merit in power electronic sectors are summarized in table 1.2 below and a detailed description can be found in Baliga's work [14-15].

Figure of Merit	*Si*	*4H-SiC*	*GaN*	*GaAs*	*Diamond*
JFoM $(E_c v_{sat} / 2\pi)$	1	180	760	7.1	2540
KFoM $\kappa(v_{sat} / \varepsilon)^{1/2}$	1	4.61	1.6	0.45	32.1
BFoM $(\varepsilon \mu E_c^3)$	1	130	650	15.6	4110
BHFoM (μE_c^2)	1	22.9	77.8	10.8	470

E_c = Breakdown electric field strength ε = Dielectric constant κ = Thermal conductivity
v_{sat} = Saturation velocity μ = Electron Mobility

Table 1.2 Comparison of Figure of Merits of different materials [14-15].

JFoM is Johnson's figure of merit [2] based on breakdown electric field and saturation velocity for handling high frequency operations. KFoM is Keyes's figure of merit [16] taking into account the thermal conductivity for capability to work at high temperature. Baliga derived two figures of merit [14-15] one for high frequency operation (BHFoM) and one for low frequency operation (BFoM) to measure the high power handling capabilities and considered mobility, dielectric constant and breakdown electric field as shown in table 1.2. Even though diamond appears to dominate GaN in all figures of merit but there are still many development and research challenges ahead for diamond to compete with the state-of-the-art GaN devices.

1.2 Applications of GaN HFETs

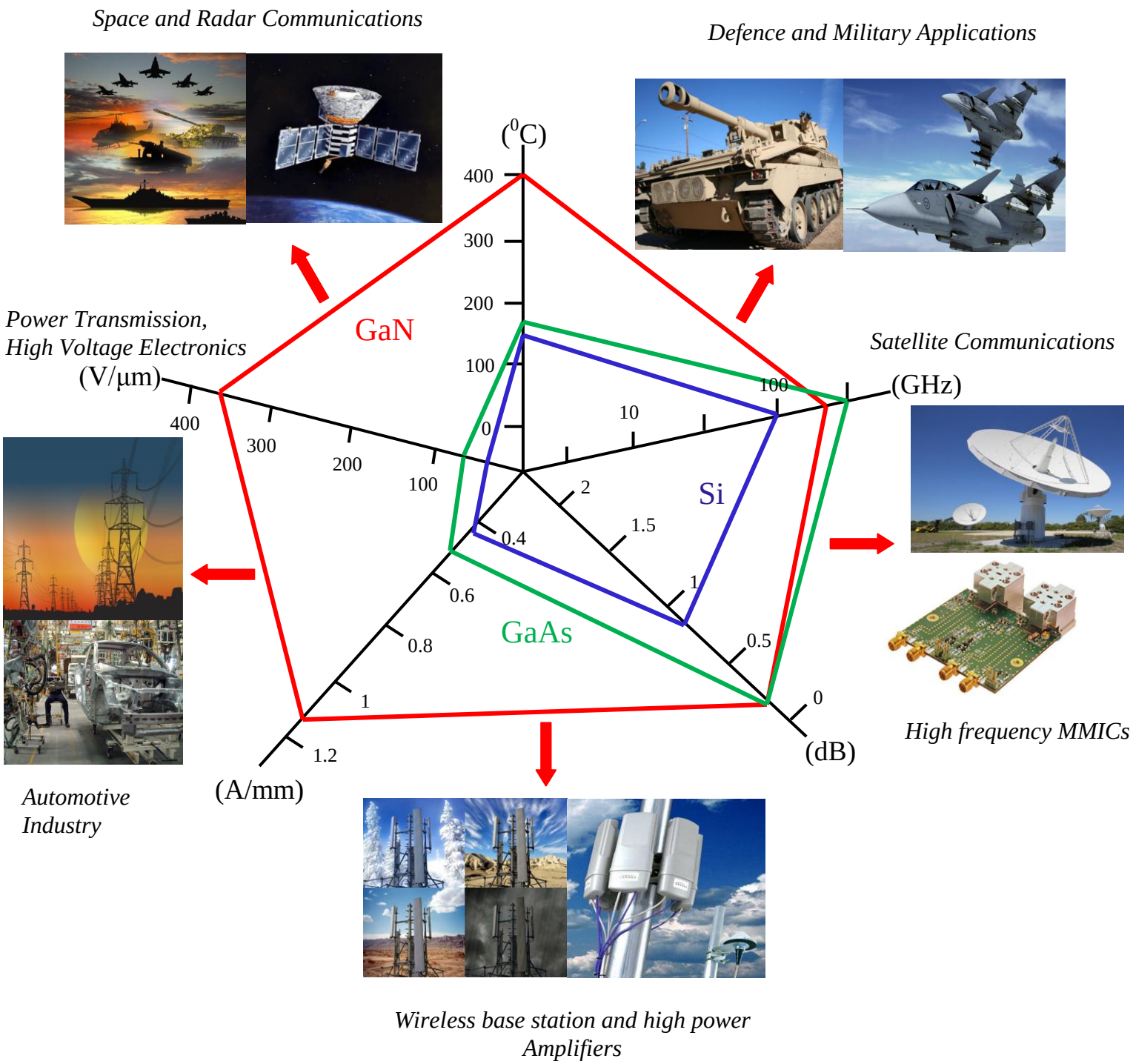

Figure 1.1 GaN operation capacity and applications in various sectors [17]

Due to some excellent material properties of GaN as discussed earlier it offers a much wider operation window compared to the conventional Si and GaAs based devices as shown in the figure 1.1.

For applications in space based microwave transmission and power systems, GaN based semiconductor devices hold a particular promise. When realized in the space sector, GaN based devices would result in the reduction of size, cost and mass of the cooling systems, due to its superior ability to operate at much higher voltage and temperature regimes than conventional semiconductors. Additionally, the radiation hardness of GaN [18] makes it more able to survive the environment of deep space while delivering superior and robust output performance. In the RF devices used for both commercial and military applications [19], GaN can offer better efficiency, higher output power density and enhanced thermal transfer characteristics compared to conventional Si devices.

As the more established Si based devices reach maturity, GaN present a major challenge to the conventional Si-MOSFETs and IGBTs used in the power sector [20]. In our everyday life, power electronics is very important to improve the battery life of our mobile phones, tablets, and laptops. The use of semiconductor based power electronics extend to hybrid vehicles, railways, efficient high voltage transmission lines and energy efficient lighting systems. In a bid to reduce the CO_2 footprint and for controlling the renewable energy sources of the future, adoption of energy efficient electronics is vital. GaN advancements in the high voltage transistor 600-1200V class are very attractive for the employment in the traction inverter of the hybrid vehicles [21]. To visualize tomorrow's smart electricity grid station – the *Internet of electricity* – mass production of highly efficient power electronics devices is required. Very low static and dynamic losses are required for power conversion to avoid wasting precious energy. At the same time, this technology should operate at high frequency, high voltage and high temperature with a minimal loss, have a long lifetime and should be ultra reliable. The technology for energy efficient control of electrical machines in the factories is predicted to save 9% of total energy consumption in the UK. For the future of the low carbon economy where renewable are predicted to produce 30% of UK electricity by 2020, adopting GaN semiconductors in control electronics can deliver a 50% improvement in the energy efficiency compared to Si [22-24].

Despite all these claims, there are several technical and commercial challenges faced by GaN in power electronics. GaN semiconductor material production is still more expensive than Si to produce and therefore efficient manufacturing processes are required. Other challenges which are under active research investigation include fabrication of high positive threshold voltage enhancement mode transistors, optimum gate dielectrics to improve device reliability issues, optimal surface passivation technique for current collapse, design of highly insulating

buffers to withstand high blocking voltage and optimized growth on Si substrate for die size scalability [25-26].

1.3 Choice of Substrates

GaN structures are normally grown heteroepitaxially on foreign substrates, most commonly on sapphire (Al_2O_3), SiC and Si. This is due to the lack of free standing GaN substrates, since it is very difficult to synthesise them and they are only available in small sizes with very high price. However, recently the hydride vapour phase epitaxial (HVPE) technique is used to grow 2-inch GaN substrates [27] but still they are very expensive. When growing on foreign substrates lower dislocation density and excellent crystallographic quality are desirable to achieve minimum defects in the crystal structure. Thus a minimum lattice mismatch between the substrate and GaN layer is required. Another important factor to consider for HFET substrate is the thermal conductivity, which relates to the ability of substrate to effectively radiate heat out of the device. The GaN HFETs are required to operate at high current and high voltage regimes which can generate plenty of heat. Self-heating in the device can severely degrade the current transport mechanism as the crystal lattice temperature is increased it leads to both negative output conductance and suppression in maximum achievable current due to phonon scattering. Therefore, good thermal conductivity of the substrate is extremely important to dissipate as much heat as possible. Table 1.3 summaries the common substrate properties with respect to GaN.

Property	*Al_2O_3*	*6H-SiC*	*Si(111)*	*GaN*
Symmetry	*Hexagonal*	*Wurzite*	*Cubic*	*Wurzite*
Lattice Mismatch (%)	14-23	3.5	17	-
Thermal Expansion Coefficient ($10^{-6}K^{-1}$)	7.3	4.5	2.6	5.6
Thermal Mismatch (%)	34	24	56	-
Thermal Conductivity (W $cm^{-1}K^{-1}$)	0.5	4.5	1.5	1.3
Wafer Size	2-8 inch	2-6 inch	2-12 inch	2 inch
Cost	Moderate	Very high	Low	Extremely high

Table 1.3 Different substrates properties with respect to GaN.

The lattice mismatch between the GaN and sapphire is about 14-23% depending upon the relative orientation. When GaN is grown on sapphire it results in 1×10^8 to 1×10^{10} cm^{-2} dislocation densities due to large lattice (14-23%) and thermal expansion coefficient mismatch (34%) between the two materials. The sapphire substrates are cheaper but devices suffer from self-heating because of its poor thermal conductivity, typically 0.5 $Wcm^{-1}K^{-1}$. Despite all that, sapphire substrates are the most commonly used substrates for GaN based devices due to its good economical viability.

SiC substrates can offer a much better alternative with reduced lattice (4%) and thermal expansion coefficient mismatch (24%). Another attractive feature of using SiC is its high thermal conductivity, typically 4.5 $Wcm^{-1}K^{-1}$, which is very suitable for high power electronics applications. However, the SiC alternative is not so cost effective which led many researchers to focus on sapphire and Si substrates as the cheaper options. The Si substrates are available readily with much larger wafer size scalability (12-inch) and offers mature processing techniques together with acceptable thermal conductivity (1.5 $Wcm^{-1}K^{-1}$). The major challenge of using Si substrates is large lattice (17%) and thermal expansion coefficient mismatch (56%) between the two materials. The lattice constant of Si is larger than GaN, therefore GaN grows under tensile stress which leads to crystal defects. However, the major advantage of using Si as a substrate is the option to integrate the Si CMOS and GaN HFET devices together on a single chip [28].

Recently GaN devices on synthetic diamond substrates prepared by chemical vapour deposition (CVD) have been reported [29]. GaN microwave power amplifiers operating in X-band are limited by self-heating therefore a heat spreading mechanism is required to effectively manage the device temperature [30]. Diamond appears to be the ideal candidate for GaN as a substrate with highest thermal conductivity of any substance ranging from 1200 – 1500 W/mK, at least three times higher than SiC. Its electrical resistivity ranges from 10^{13} to 10^{16} Ω.cm which is comparable to sapphire (10^{17} Ω.cm) and much better than SiC (10^6 Ω.cm) [29]. However, GaN growth on diamond wafers faces many manufacturing challenges ahead including strain management introduced by different thermal expansion of two materials which makes it difficult in reducing the wafer bow and maintaining the device ready GaN surface morphology on the composite wafer [29].

1.4 Polarization Effects in Wurtzite GaN Semiconductors

GaN semiconductors can grow with Zinc blende and Wurtzite crystal formation [31-32]. However, AlGaN/GaN HFETs are primarily grown with Wurtzite crystal structure. The Wurtzite crystal structure is formed with hexagonal unit cell which further consists of two intercepting hexagonal closed packed (HCP) sub-lattices (one formed with Ga-atom and other formed with N-atom) which are shifted with respect to each other by $u_0 = 3/8c_0$, and c_0 is the height of the hexagonal whereas a_0 is the lattice constant [33] as shown in figure 1.2.

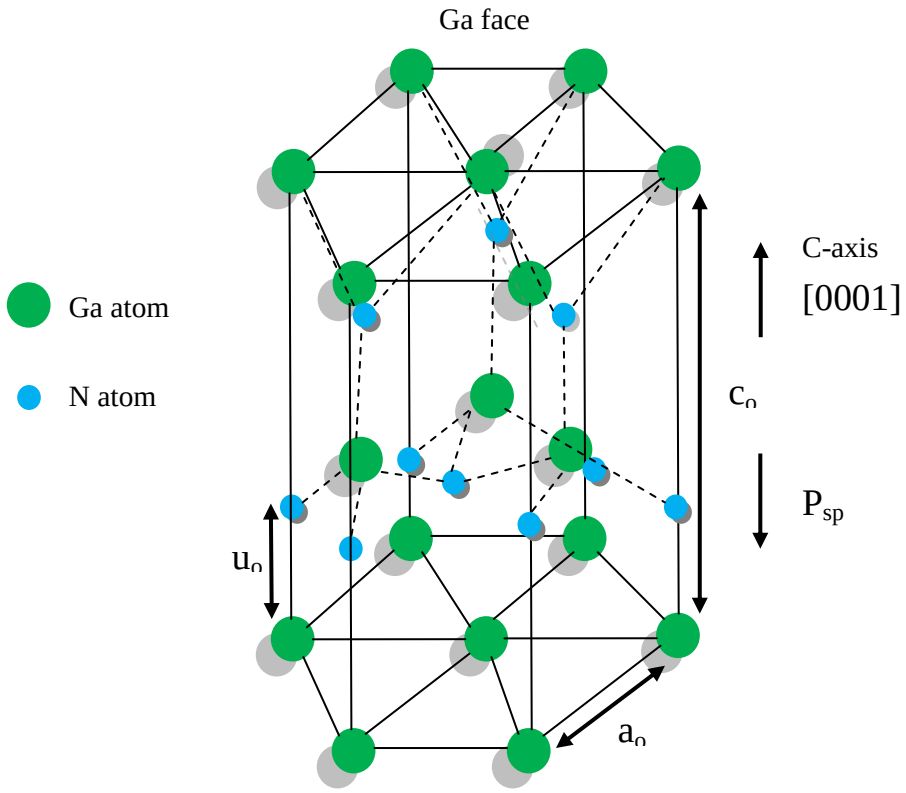

Figure 1.2 Hexagonal Wurtzite Ga-face terminated GaN lattice structure

The chemical bond between the two atoms in Wurtzite structure is partly ionic since there is a large difference in electronegativities of N and Ga atoms. Due to the presence of nitrogen which has the highest electronegativity in group V, III-nitrides compounds have some distinctive properties. The GaN Wurtzite structure lacks inversion symmetry along the c-axis or [0001] direction, resulting in polar axis.

There are two types of Polarization effects in Wurtzite GaN semiconductors, namely spontaneous polarization and piezoelectric polarization.

1.4.1 Spontaneous Polarization

The Spontaneous polarization (P_{sp}) occurs in Wurtzite GaN crystal structures without the application of any external strain in the crystal and is present in the unstrained crystal structure. The Spontaneous polarization is due to the natural Wurtzite structure of GaN [32], which lacks the inversion symmetry along the c-axis [0001] resulting in naturally distorted crystal structure with strong macroscopic polarization. The origin of spontaneous polarization is a microscopic polarization due to bonding between atoms, where the centre of negative charge (electrons) shifts away from the centre of positive charge (nuclei). Such a polarized atom constitutes a dipole with a dipole moment. In the absence of applied electric field, most materials have no dipole or the orientation of dipoles is random which results in zero total polarization. However in a low symmetry crystal, this may not be true and asymmetry of bonding may form dipoles which consequently become the source of spontaneous polarization (P_{sp}), even without any mechanical and electrical perturbation. The direction of polarization field is dependent on the polarity of the crystal structure. Two possible growth cases are Ga-face or N-face in [0001] bilayer which means that either the Ga-atom takes the top position (Ga-face) or the N-atom terminates the surface (N-face). In the Ga-face structure, spontaneous polarization always points towards the substrate for both AlGaN and GaN whereas in N-face structure the direction of polarization is inverted [12].

The Spontaneous polarization coefficients of GaN, AlN and InN along with lattice parameters are shown in table 1.4.

Parameters	GaN	AlN	InN
P_{sp} (C/m^2)	-0.029	-0.081	-0.032
a (A^0)	3.189	3.112	3.548
c (A^0)	5.185	4.982	5.760

Table 1.4 Spontaneous polarization coefficients and lattice constants of GaN, AlN and InN[12].

The Spontaneous polarization for ternary nitride, AlGaN and AlInN as a function of Al (x) composition can be expressed as [34],

$$P_{sp}\ (Al_xGa_{1-x}N) = -0.09x - 0.034(1-x) + 0.021x\ (1-x)\ C/m^2 \qquad [1.2]$$

$$P_{sp}\ (Al_xIn_{1-x}N) = -0.09x - 0.042(1-x) + 0.070x\ (1-x)\ C/m^2 \qquad [1.3]$$

1.4.2 Piezoelectric Polarization

The Piezoelectric polarization (P_{pz}) in AlGaN is due to the distortion of crystal lattice caused by strain, since the lattice constant of AlGaN is much smaller than GaN. Therefore when an AlGaN layer is grown on top of a GaN buffer, the lattice mismatch is accommodated by some tensile strain in the barrier layer as shown in figure 1.3. In contrast to spontaneous polarization, the piezoelectric polarization is due to externally exerted strain by growth in the crystal structure. This strain causes distortion in the crystal and results in a high strain induced piezoelectric field [12].

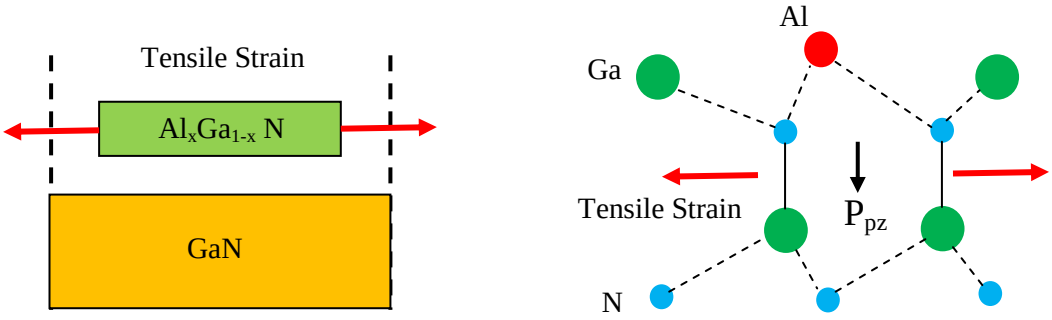

Figure 1.3 Growth of AlGaN Wurtzite Ga-face, resulting in tensile strain and piezoelectric polarization.

The strength of piezoelectric polarization is simply defined by the piezoelectric coefficients e_{33} and e_{13} as [12],

$$P_{pz} = e_{33}\varepsilon_z + e_{13}(\varepsilon_x + \varepsilon_y) \qquad [1.4]$$

$\varepsilon_z = (c - c_o)/c_o$ is the strain along the c-axis and in plane strain $\varepsilon_x = \varepsilon_y = (a - a_o)/a_o$ is assumed to be isotropic. a_o and c_o denotes the equilibrium values of lattice constants. By using the expressions for elastic constants c_{13} and c_{33}, the expression for piezoelectric polarization in AlGaN along the c-axis can be expressed as [35],

$$P_{pz(AlGaN)} = 2 \times \frac{a_{GaN} - a_{AlGaN}}{a_{AlGaN}} \left(e_{31} - e_{33}\frac{c_{13}}{c_{33}}\right) \qquad [1.5]$$

The expressions for lattice constant of GaN (a_{GaN}) and AlGaN (a_{AlGaN}) as a function of Al (x) composition along with piezoelectric coefficients and elastic constants are mentioned below [35],

$$a_{GaN} = 3.189 \times 10^{-10} \text{ (m)}$$

$$a_{Al_x Ga_{1-x}N} = \text{x. } a_{AlN} + (1\text{-x})\, a_{GaN} = (-0.077\text{x} + 3.189) \times 10^{-10} \text{ (m)}$$

$$c_{33} = (-32\text{x} + 405) \times 10^{9} \text{ (Pa)}$$

$$c_{13} = (5\text{x} + 103) \times 10^{9} \text{ (Pa)}$$

$$e_{33} = 0.73\text{x} + 0.73 \text{ (C/m}^2\text{)}$$

$$e_{31} = -0.11\text{x} - 0.49 \text{ (C/m}^2\text{)}$$

The piezoelectric polarization in the AlGaN barrier layer is a strong function of Al (x), composition. As the lattice constant of the AlGaN decreases with an increase in Al (x) composition the polarization increases. For any given, Al (x) concentration as the AlGaN barrier layer exceeds a maximum critical thickness, strain relaxation tends to occur in the crystal structure resulting in reduction of piezoelectric polarization. Therefore, piezoelectric polarization in expression [1.5] can be modified as [35],

$$P_{pz(AlGaN)} = 2\,[1 - r(x)] \times \frac{a_{GaN} - a_{AlGaN}}{a_{AlGaN}} \left(e_{31} - e_{33}\frac{c_{13}}{c_{33}}\right) \qquad [1.6]$$

where,

$$r(x) = \frac{a_{AlGaN,strained} - a_{GaN}}{a_{AlGaN,relaxed} - a_{GaN}}$$

$a_{AlGaN,Strained}$ and $a_{AlGaN,Relaxed}$ are the lattice constant of AlGaN barrier under stress and relaxed conditions respectively. The value of $[(e_{31} - e_{33}\frac{c_{13}}{c_{33}})] < 0$ is always negative for the full range of Al (x) composition, therefore under tensile strain ($a_{GaN} > a_{AlGaN}$) the magnitude of piezoelectric polarization is always negative and for compressive strain ($a_{GaN} < a_{AlGaN}$) it is positive. Since the spontaneous polarization is always negative and points towards the substrate (in Ga-face) for GaN, AlN and InN as shown previously in the table 1.3, the alignment of spontaneous and piezoelectric polarization is parallel for tensile stain and anti-parallel for compressive strain [12]. Another important feature in III-nitrides is that if the polarity of growth is flipped from Ga-face to N-face or vice versa then

both spontaneous and piezoelectric polarizations changes directions [12]. The combined effect and constructive combination of spontaneous and piezoelectric polarization in AlGaN/GaN heterostructure with Ga-face growth is described in figure 1.4.

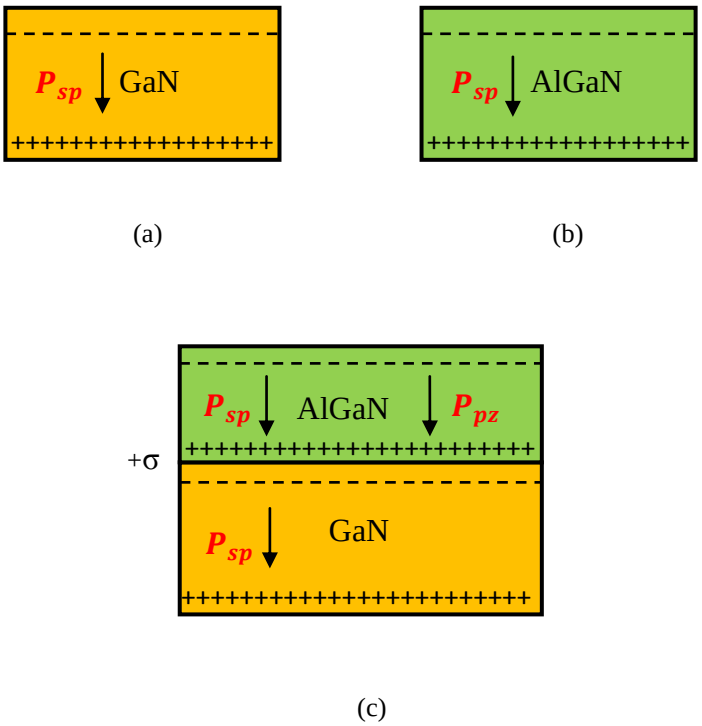

Figure 1.4 (a) Spontaneous polarization in Ga-face GaN and (b) AlGaN (c) Combined spontaneous and piezoelectric polarization in AlGaN/GaN heterostructure.

The difference in spontaneous and piezoelectric polarizations of two materials causes a high polarization sheet charge density to accumulate near the bottom of AlGaN/GaN interface which is defined as,

$$\rho_{Pol} = P_{AlGaN} - P_{GaN} = P_{AlGaN\ (Spontaneous)} + P_{AlGaN\ (Piezoelectric)} - P_{GaN\ (Spontaneous)} \qquad [1.7]$$

It is noteworthy that GaN buffer layer is fully relaxed and there is no piezoelectric polarization.

1.5 Theory of Heterostructure and 2DEG Formation

When a junction is formed between two different semiconductor materials with distinct band gap energies it is called a heterojunction or heterostructure and the interface between the two semiconductors is termed as the heterointerface [30]. Heterostructures are widely used in semiconductor lasers, photodiodes and microwave devices including HFETs. The inherit advantage of creating a heterostructure in HFETs is the formation of two dimensional electron gas commonly referred as 2DEG, which is formed due to the confinement of electrons in a well defined triangular quantum well. The electrons have quantized energy levels in one spatial direction and are only free to move laterally, along the heterostructure interface. This 2DEG has a unique characteristic of extremely high electron mobility (~2000 $cm^2V^{-1}s^{-1}$) leading to much reduced on-state resistance (R_{on}) and improved high frequency performance. Unlike AlGaAs/GaAs HFETs, the presence of very high polarization effects in GaN makes it possible to fabricate devices without the intentional doping of the upper wide band gap material. This significantly reduces ionized impurity scattering and Coulomb scattering as the 2D electrons are separated from the supply atoms. Due to these polarization effects the 2DEG sheet charge density in AlGaN/GaN heterostructures is about five times higher ($>1\times10^{13}cm^{-2}$) than in doped AlGaAs/GaAs HFETs [36].

Consider two different materials namely GaN and AlGaN as shown in figure 1.5. The AlGaN is a wide band gap material with band gap energy E_{g1} and GaN band gap energy is E_{g2}.

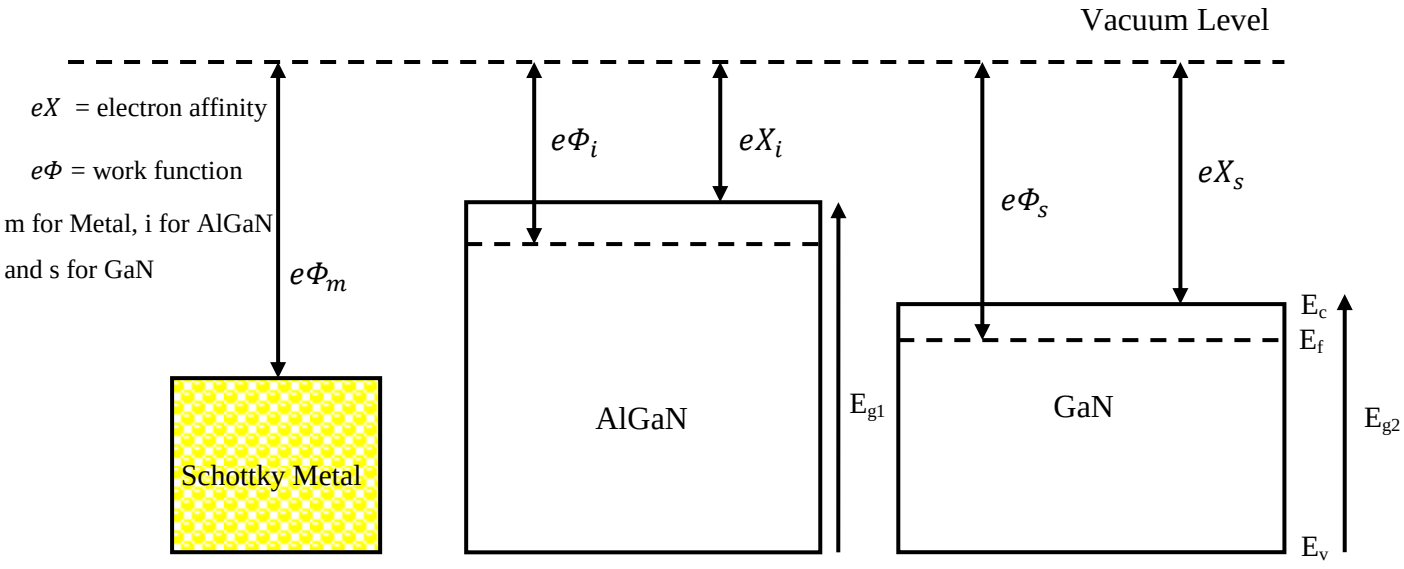

Figure 1.5 Energy band diagram for AlGaN and GaN before heterostructure formation.

Now if a heterostructure is formed between these two semiconductors then, because of the difference in band gap energies, the conduction (E_c) and valance band (E_v) cannot be continuous across the interface as shown in figure 1.6. When the semiconductors are brought together the Fermi level (E_f) aligns and band bending accommodates the discontinuity [30].

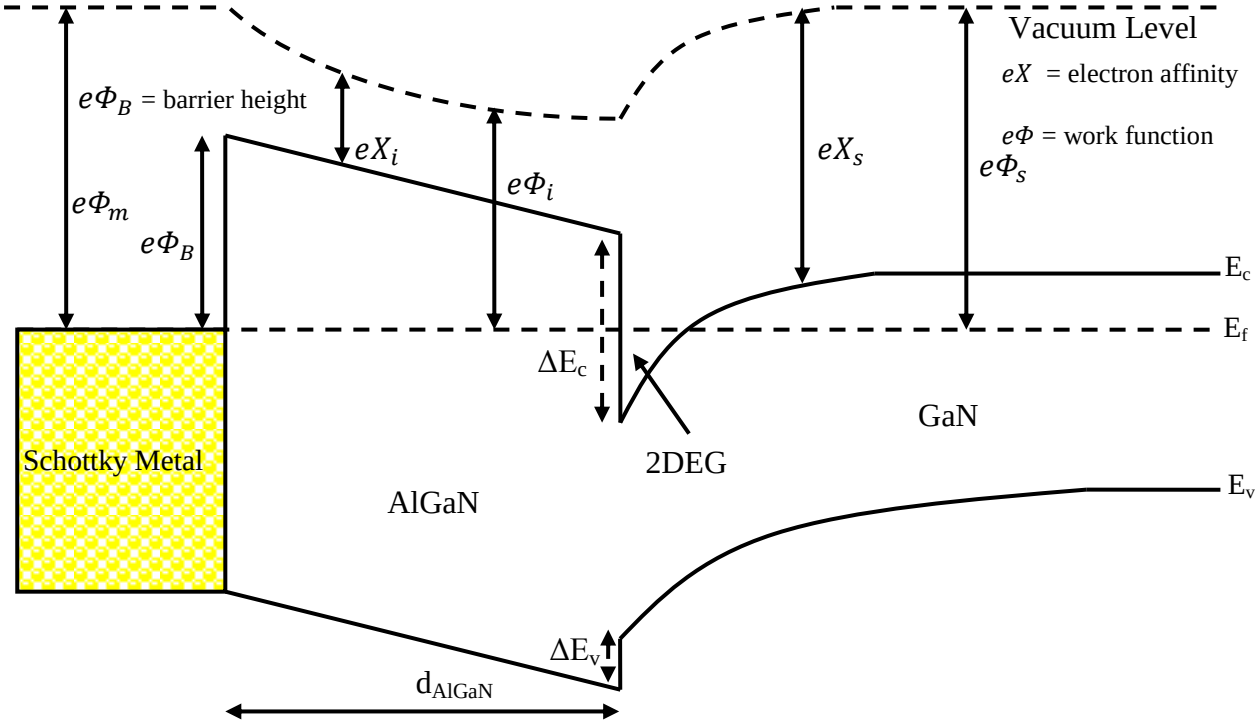

Figure 1.6 Energy band diagram for AlGaN and GaN after heterostructure formation.

The complete heterostructure for the HFET device also includes a Schottky gate contact which is used to modulate the 2DEG charge. A schottky barrier is formed between the gate and the AlGaN barrier layer and Fermi level (E_f) aligns for both semiconductors and metal. The formation of the heterostructure leads to the band gap discontinuities at both conduction band (ΔE_c) and valence band (ΔE_v). A triangular well containing the 2DEG emerges where electrons come from the donor like surface states or bulk GaN material. The origin of these electrons is further discussed in the next section 1.5. The maximum electron sheet charge concentration formed at the AlGaN/GaN interface is expressed as [12],

$$n_s(x) = \frac{\rho_{Pol}}{q} - \left(\frac{\varepsilon_o \varepsilon_r(x)}{d_{AlGaN}\, q^2}\right) \left[q\Phi_B(x) + E_F(x) - \Delta E_c(x) \right] \qquad [1.8]$$

where, ε_o is the vacuum permittivity constant, $\varepsilon_r(x)$ is the relative dielectric constant of AlGaN, q is the electron charge, ρ_{Pol} is the total polarization charge at AlGaN/GaN interface, d_{AlGaN} is the AlGaN barrier thickness, $\Phi_B(x)$ is the Schottky barrier height, $E_F(x)$ is the Fermi level with respect to GaN conduction band edge and $\Delta E_c(x)$ is the conduction band offset between the AlGaN and GaN interface.

The 2DEG sheet charge concentration as mentioned in equation 1.8 increases with the Al content in the barrier layer, because the Al(x) concentration increases both piezoelectric polarization and AlGaN band gap energy resulting in greater conduction band offset $\Delta E_c(x)$. However, some of the difficulties in making a wider band gap barrier layer are formation of good quality ohmic contacts and growth strain issues. Nevertheless, devices with 40-50% Al(x) concentration have been reported for RF and microwave applications [37]. The 2DEG sheet charge concentration also increases with the AlGaN barrier thickness but only up to a maximum critical thickness, typically 40nm, and then flattens out with further increase in the thickness due to strain relaxation.

Recently, more modified barrier designs have been reported to further improve the AlGaN/GaN HFETs performance such as AlGaN/AlN/GaN structures [38]. The major restrictions in achieving very high electron mobility in the 2DEG are interface scattering, dislocation scattering and alloy disorder scattering. With the insertion of a very thin (~1nm) and wide band gap (6.2eV) AlN material layer sandwiched between the AlGaN and GaN layers as shown in figure 1.7, the conduction band offset, ΔE_c, is further increased and electron alloy disorder scatterings are reduced. The binary AlN spacer layer reduces the penetration of electrons from the GaN channel into the ternary AlGaN barrier layer, thereby significantly improving the electron mobility. In this work, we have achieved nearly 30% improvement in the electron mobility with AlN mobility enhancement spacer layer.

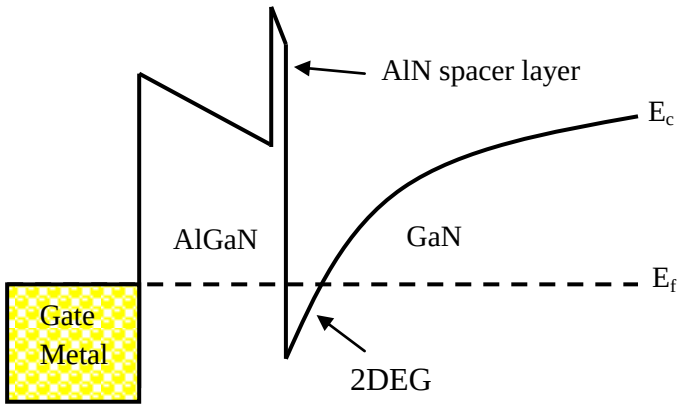

Figure 1.7 Conduction band diagram for AlGaN/AlN/GaN structure.

1.6 Origin of 2DEG and Surface States

Because the 2DEG charge concentration is achieved in AlGaN/GaN without the intentional doping in the AlGaN barrier layer, there is some uncertainty in the literature about the origin of 2DEG sheet charge. J. P. Ibbetson [39] proposed the most widely accepted theory for 2DEG formation, which explains the electron transfer from the surface states as main source of 2DEG sheet charge.

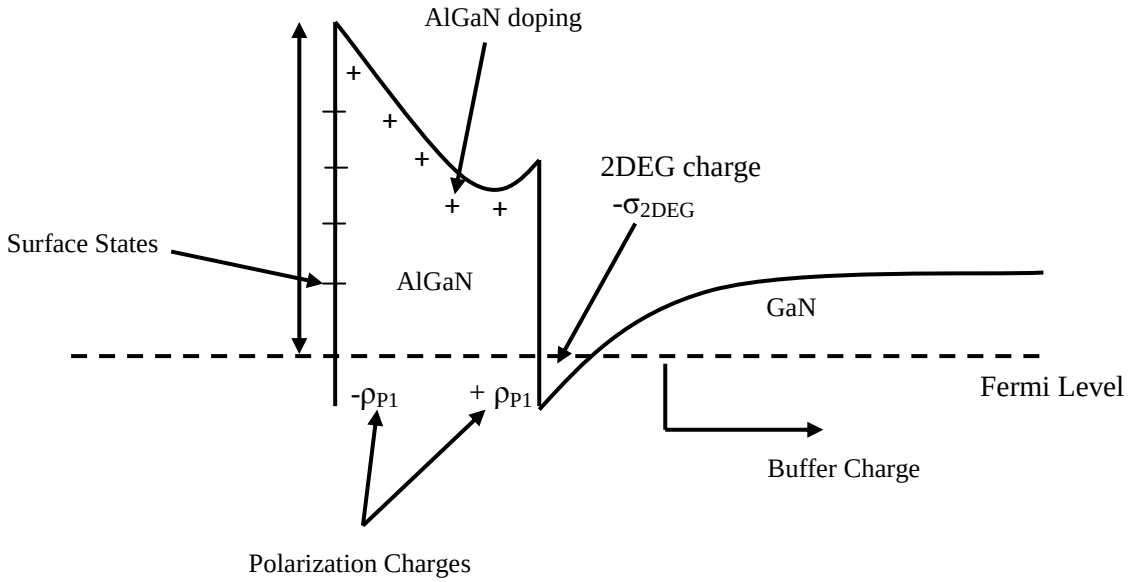

Figure 1.8 Conduction band diagram for HFET showing various charge components.

Figure 1.8 shows the conduction band of HFET with all the possible charge components including (i) polarization induced charges at AlGaN/GaN interface (ρ_{P1}) (both spontaneous and piezoelectric) (ii) negative 2DEG sheet charge (qn_s) (iii) ionized charge in AlGaN due to ionized donors (σ_{AlGaN}) (iv) buffer charge and finally (v) charge due to the ionized surface states ($\sigma_{Surface}$).

The sum of all these charge components must be zero in the absence of any electric field, as the overall system should be charge neutral. Now the polarization charges are present within the crystal structure and constitute a dipole with net positive and net negative charge. Therefore, the overall contribution of polarization charges would remain zero as $\pm\rho_{P1}$ balance each other. The buffer charge due to any background doping is generally very small in magnitude so it can be neglected for the sake of clarity [39].

This leaves the remaining charges in the charge balance equation as,

$$\sigma_{Surface} + \sigma_{AlGaN} - q n_s = 0 \qquad [1.9]$$

It is worth mentioning that ionized donors in AlGaN barrier layer are due to impurities or modulation doping (where charge particles move to the lower band gap GaN leaving behind the ionized donor states). Since no modulation doping is adopted in the AlGaN/GaN heterostructures used in this study, hence this component is taken as zero. This leaves the 2DEG charge concentration to be balanced by the ionized surface states in order to achieve charge neutrality. It is noteworthy that these donors like surface states would only ionize if the AlGaN barrier exceeds a minimum critical thickness (t_{cr}) level [40]. For a thin AlGaN barrier layer ($t < t_{cr}$), the surface states lies below the Fermi level and there is no 2DEG formation at the AlGaN/GaN interface as shown in the figure 1.9(a).

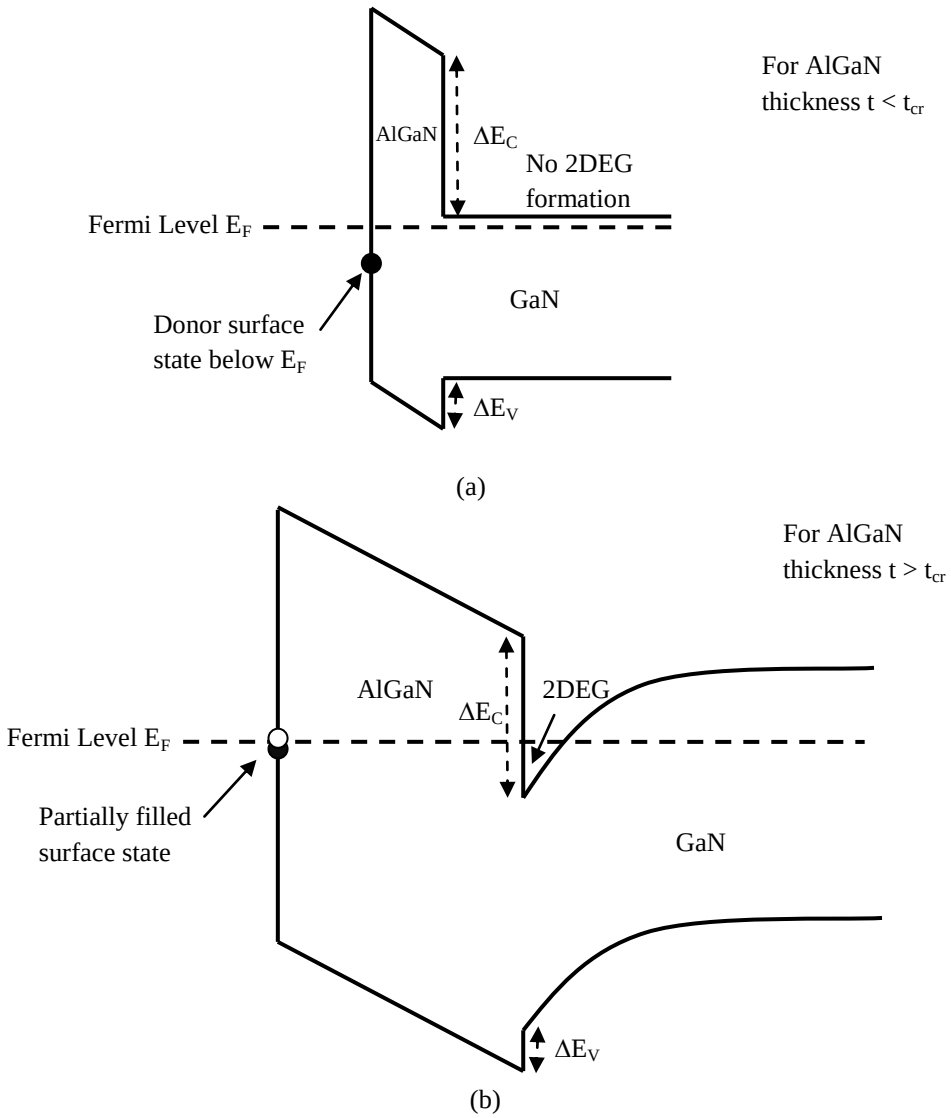

Figure 1.9 Energy band diagram for HFET with (a) AlGaN thickness less than t_{cr} and (b) AlGaN thickness greater than t_{cr} [40].

Now as the AlGaN barrier thickness increases, the Fermi level approaches the level of the surface states. When the barrier thickness surpasses a minimum critical (t_{cr} ~3.5nm) thickness value, the Fermi level reaches the surface states as shown in figure 1.9(b) and the 2DEG charge begins to emerge as electrons are transferred from the surface states to the AlGaN/GaN conduction band interface, leaving behind the positively charged surface states [39]. The nature of these surface states is donor like since they are neutral when occupied and positive when empty. Increasing the AlGaN barrier thickness beyond the minimum critical thickness ($t > t_{cr}$) results in transfer of more and more electrons into the 2DEG channel fast approaching the polarization induced charge. The charged 2DEG concentration in the AlGaN/GaN interface is therefore balanced by the (opposite) exact same concentration of the positively charged surface states [41]. The expression of minimum critical thickness is given as [39],

$$t_{cr} = (E_s - \Delta E_c) \frac{\varepsilon_r}{q\rho_{pol}} \qquad [1.10]$$

where, ε_r is the dielectric constant of AlGaN barrier layer, E_s is the energy level of surface state, q is the electron charge and ρ_{pol} is the polarization induced charge. The 2DEG charge only exists with the presence of positive surface states. The magnitude of 2DEG charge density ($t > t_{cr}$) as the function of AlGaN barrier thickness is expressed as [39],

$$qn_s = \rho_{pol} \left(1 - \frac{t_{cr}}{t} \right) \qquad [1.11]$$

1.7 Device Structure and Basic Operation

The basic device structure of the AlGaN/GaN heterostructure field effect transistor is shown in the figure 1.10 below.

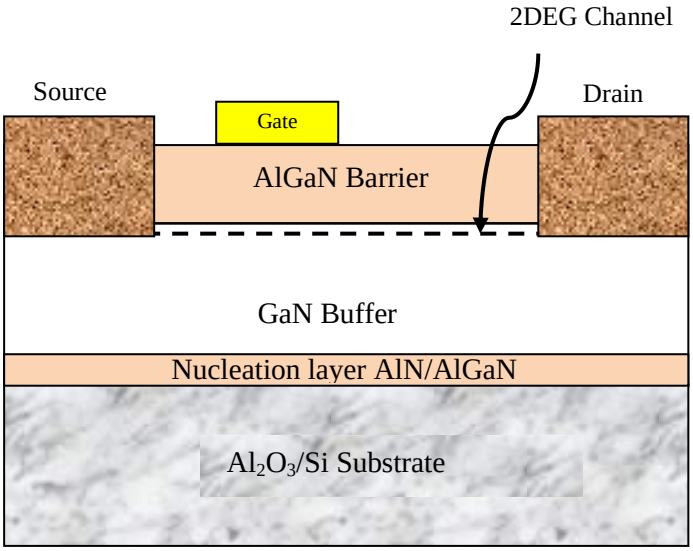

Figure 1.10 Basic device structure of a HFET.

The structures used in this study were grown by Cambridge University or Sheffield Univeristy by using Metal Organic Chemical Vapour Deposition (MOCVD) on a sapphire or Si substrate. A heterostructure is formed between the GaN (typically 2-4 μm) and the wide band gap AlGaN barrier (20-40nm) layer. As mentioned before, a two dimensional electron gas (2DEG) is created at the lower interface of AlGaN/GaN heterostructure to form a thin channel in the top GaN buffer region. It is important to grow a semi-insulating or a highly resistive GaN buffer layer to prevent any buffer conduction which can lead to both poor device pinch-off characteristics and unwanted leakage current paths. In order to accommodate the growth of a semi-insulating GaN buffer layer on unmatched substrates a nucleation layer consisting of a few nanometers of AlN or AlGaN layers is typically grown before the GaN layer to reduce the stress and lattice mismatch in the crystal structure. In some cases, a cap layer of undoped GaN with 1-2 nm thickness is also grown on top of the AlGaN barrier layer. This cap layer can prevent the surface oxidation of the AlGaN barrier and can improve the overall surface morphology.

The basic HFET device has two ohmic contacts, namely drain and source, and one Schottky gate contact formed between them. The ohmic contacts are formed using (Ti/Al/Ni or Ti/Au) metals stack layers. The Ti metal reacts with the AlGaN barrier to form a TiN (lower work

function) which helps in reducing the Schottky barrier height, thereby helping in achieving a good ohmic contact. It also creates N-vacancies by reacting with the AlGaN layer making it highly n-type making it easy for the electrons to tunnel into the semiconductor. The second Al metal layer prevents the oxidation of the underlying Ti layer. The third layer of either Ni or Ti is used to prevent the out diffusion of Al and intermixing of Al and Au metals. This layer also helps in achieving good surface edge acuity with ohmic contacts when annealed at high temperatures (800-850^{0}C). Finally, Au metal is deposited to prevent the oxidation of underlying layers and to enhance the conductivity. Annealing at more than 800^{0}C temperature for a few seconds helps metals to diffuse into the semiconductor and make contact with the 2DEG. The source is typically grounded while the drain is positively biased with respect to the source. The current flows laterally via the 2DEG channel along the heterostructure interface from the drain to source under a (V_{DS}) voltage bias.

The gate contact can be isolated from the channel by an insulator (MOSFET) [42], forming a pn junction (JFET) [43], or by Schottky barrier (MESFET) [44]. A similar Schottky barrier concept used in metal semiconductor field effect transistors is adapted in the HFETs. A negative gate to source voltage (V_{GS}) is applied to modulate or control the flow of current through the 2DEG channel. The negative gate to source voltage repels the electrons and creates a depletion region. The effect of this is a reduction in the current flow between the drain and a source terminal as the negative gate bias is increased. The 2DEG channel is therefore depleted by the gate electrode until the pinch-off point is reached, defined by the gate threshold voltage (V_{TH}) where the device turns-off. It is noteworthy that the gate contact is normally placed asymmetrically between the source and drain, slightly closer to the source contact in order to reduce the high electric field between the positive drain and negative gate contacts which can lead to device breakdown. To form the Schottky gate contact, Ni/Au metals are generally used. In order to suppress the device gate leakage in the off-state, thin insulating layers such as SiN_x and SiO_2 or other high-k dielectric layers such as Al_2O_3 and HfO_2 are inserted between the gate and AlGaN layer to form a Metal insulater semiconductor HFET (MISHFET) structure [45-49].

Traditional HFETs are normally-on or depletion mode devices and have negative threshold voltage. However, HFETs with positive threshold voltage are also available which are called normally-off or enhancement mode devices. The enhancement mode HFETs are discussed later in chapter 5 of this thesis.

1.7.1 Peformance Parameters

a) Transconductance

Transconductance (g_m) is defined as the ability of the gate to control the flow of current between the drain and source. It is a measure of responsivity of the device. Mathematically, it can be stated as the ratio of change in drain current (I_{DS}) to the change in gate to source voltage (V_{GS}). A large transconductance value is desirable for high gain of the device.

$$g_m = \frac{\Delta I_{DS}}{\Delta V_{GS}} \qquad [1.11]$$

In a real HFET there is some finite resistance between the source and gate, thus the actual transconductance is modified or reduced by the factor R_s, the source resistance between the gate and source according to,

$$g_{m(ext)} = \frac{g_m}{1 + R_S g_m} \qquad [1.12]$$

Thus, to maximize extrinsic transconductance ($g_{m(ext)}$), R_S needs to be reduced. This is the main reason why the gate is placed closer to the source.

b) Drain Current

Electric current is the movement of charge per unit time and it can be expressed by the product of charge density and velocity of electrons. [2] The electron velocity relates to the transport properties of the material, thus materials with higher electron velocity values are desirable to achieve more drain current per unit gate width (A/mm) given by,

$$I_{DS} = \mathrm{q}\, n_s v_{eff} \qquad [1.13]$$

where n_s is the sheet charge density, q is the electronic charge and v_{eff} is the effective velocity of electrons in the channel region. In AlGaN/GaN HFETs the sheet charge density can be maximized by increasing both spontaneous and piezoelectric polarizations together with an optimum AlGaN barrier thickness to achieve the desired tensile strain [12]. When the HFET is operated at low drain source bias ($V_{DS} < V_{GS} - V_{TH}$), the drain current rises linearly with the applied voltage this region is called the linear region as shown in figure 1.11. However, as the drain source bias is further increased ($V_{DS} > V_{GS} - V_{TH}$), the drain current tends to saturate and becomes independent of voltage bias. This region is defined as

saturation region. The saturation of drain current in this region is a consequence of channel pinch-off. The device turn-on resistance (R_{ON}) is defined in the linear region by drawing a straight line from the origin and taking the ratio of voltage and current near the current roll-off point as shown in the figure 1.11. Both drain current and transconductance of the HFETs are generally reported as normalized with respect to the gate width (W) of the device.

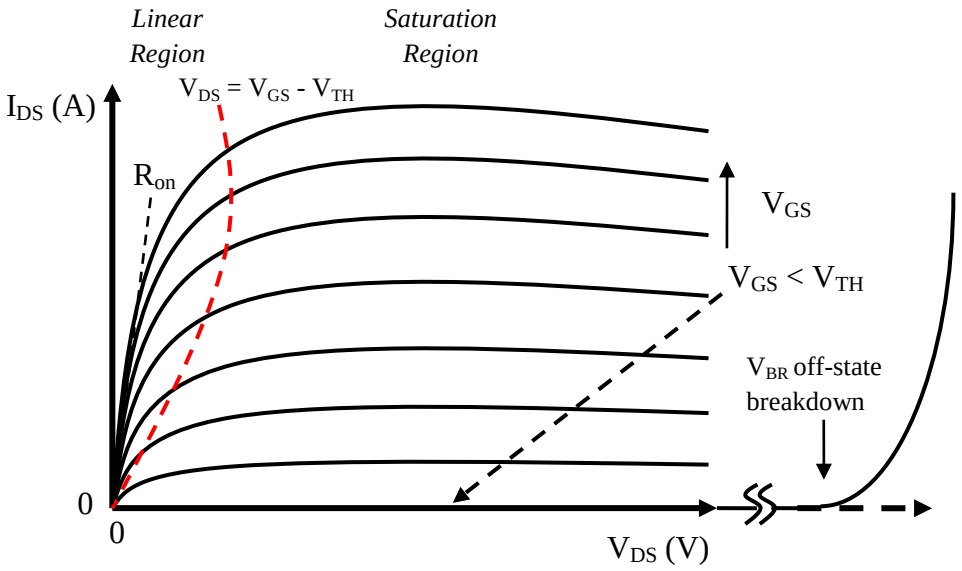

Figure 1.11 IV characteristics of a typical transistor.

The expression for the drain current in the saturation region is given as,

$$I_{DS} = \frac{\varepsilon_{AlGaN} W v_{sat}}{d_{AlGaN}} (V_{GS} - V_{TH}) \qquad [1.14]$$

where ε_{AlGaN} and d_{AlGaN} are the permittivity and thickness of the AlGaN barrier layer, W is gate width and V_{sat} is electron saturation velocity.

c) Sheet Resistance

Another reason to achieve higher sheet charge density, n_s, is to reduce the on-resistance of the device. The sheet resistance, R_{sh}, is inversely proportional to the product of n_s and electron mobility μ_n.

$$R_{sh} = \frac{1}{q n_s \mu_n} \qquad [1.15]$$

In AlGaN/GaN heterostructures, an increase in Al mole fraction of the AlGaN barrier tends to enhance n_s but degrade mobility because of higher alloy and interfacial scattering as the

centroid of the 2DEG moves closer to the AlGaN/GaN interface. Therefore, the optimum barrier thickness for maximum piezoelectric polarization is necessary to achieve higher sheet charge density [12]. R_{sh} is expressed in ohms per square and generally varies from 350 to 550 Ω /sq in HFETs.

d) Switching Speed

For the power electronics switching applications, an important figure of merit for any device is the product of on state resistance (R_{on}) and gate-drain charge or simply gate charge (Q_g).

$$FOM = R_{on} \times Q_g \qquad [1.16]$$

The conduction losses are determined by R_{on}, and the switching losses are proportional to gate charge. As a power switch, the transistor is switched on and off quickly from the pinch-off state into the linear region. The switching time is the time required to charge and discharge gate capacitance due to Miller effect. Since the total losses are the sum of both conduction and switching losses it is very important to minimize both on-resistance and gate charge.

e) Cut-off Frequency

The cut-off frequency (f_t) of any field effect transistor is defined as the frequency at which the current gain of the device falls to unity. Mathematically,

$$f_t = \frac{v_{sat}}{2\pi L_{eff}} = \frac{g_m}{2\pi C_g} \qquad [1.17]$$

v_{sat} is saturation velocity, L_{eff} is the effective gate length and C_g is the gate capacitance (per unit gate width). The cut off frequency is a very important figure of merit for applications in X-band or above in radar and satellite communication. Thus, to maximize f_t, materials with higher v_{sat} (GaN ~ 2.2×10^7 cm/s) and devices with shorter gate lengths are designed so that the transit time of electrons underneath the gate region is reduced.

f) Breakdown Voltage

The breakdown voltage (V_{br}) between the gate and drain terminal of the HFET in the off-state is a very important parameter to enhance the power handling capacity of the device. The output power of the device for a sinusoidal signal is given as,

$$P_o = \frac{I_{D(max)}}{8} \times (V_{br} - V_{knee}) \quad [1.18]$$

The knee voltage, V_{knee}, is the voltage at which drain current saturates and $I_{D(max)}$ is the maximum drain current of the device. Higher breakdown voltage is also desirable in power switching applications to sustain a large voltage in the off-state.

Increasing the drain – gate spacing and employing multiple field plates to reduce or modulate the electric field peaks at the drain side edge of the gate contact are methods reported in the literature to enhance the breakdown voltage of the device [50]. In addition to the breakdown mechanism taking place between the gate and drain contacts, device breakdown in the off-state can also result from the leakage current flow in the GaN buffer region, buffer substrate interface or the substrate itself, particularly for devices fabricated on conducting Si substrates [51-52]. To prevent such breakdown, highly insulating and thick buffer regions are required to sustain the large blocking voltages required in high power electronic applications [53].

1.8 Current Collapse and Surface States

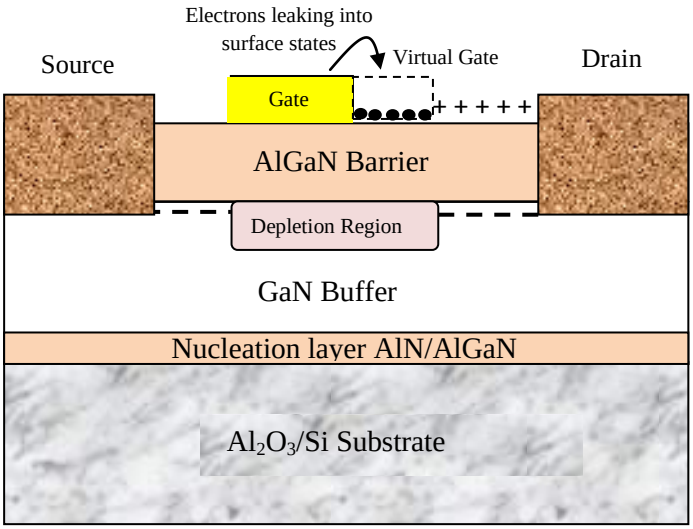

Figure 1.12 AlGaN/GaN HFET device structure showing formation of a virtual gate and electron trapping in surface states.

As discussed before, polarization effects in AlGaN/GaN heterostructures forms a dipole with opposite charges at top and bottom surface of AlGaN layer and 2DEG electrons arises from the surface states, leaving equal positive sheet charge on the surface [39-41]. During the off-state condition of AlGaN/GaN HFET large electric field is present between the drain and

negatively biased gate electrode. Under the influence of this large electric field, electrons are injected from the gate metal into the positive surface states, as shown in figure 1.12. The presence of electrons in the surface states near the gate edge region (drain side) extends the gated region, forming a negative virtual gate [54]. The consequence of this negative virtual gate is an extension in the depletion region beyond the gated channel region, as for every electron trapped in the surface state an electron from the 2DEG underneath is directly compensated.

The electron trapping effect in the surface states results in a DC to RF current discrepancy commonly defined as current collapse or current slump [54-56]. When the transistor is switched on and off or pulsed under RF operations, then in the off-state surface states are quickly populated with negatively charged electrons. But when the transistor is turned back on again, these trapped electrons must emit from the surface states to allow the channel current (via 2DEG) to flow. However, the associated emission time of these trapped electrons from the surface states are generally very slow, which degrades the device switching capability. This result in a slow 2DEG channel current recovery and a dramatic increase in the device turn-on resistance (R_{ON}) often stated as dynamic R_{ON}. The maximum achievable current in fast switching operation is therefore reduced due to this current collapse phenomenon which effectively increases the knee voltage (V_{knee}). If the traps in the surface states are sufficiently deep then device switching speed is severely degraded. However, shallow traps can emit electrons more quickly maintaining a good switching capability [54-56].

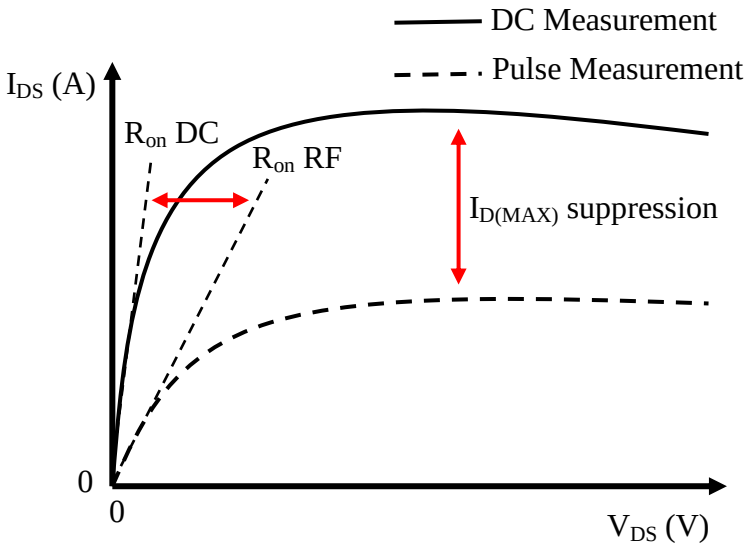

Figure 1.13 Dynamic IV characteristics of an AlGaN/GaN HFET.

Current collapse can severely restrict the adoption of AlGaN/GaN HFETs in power switching applications, but recently many researchers have significantly overcome the electron surface charge trapping effects in HFETs by using Plasma Enhanced Chemical Vapour Deposition (PECVD) silicon nitride (SiN_x) passivation layers [45]. It is reported that SiN_x layer reduces surface states and prevents the formation of a negative virtual gate [54]. After the 50-100nm thick SiN_x layer deposition on the surface, current collapse is significantly reduced in addition an almost 10% increase is observed in the DC output drain current together with a reduction in on-state (R_{ON}) resistance. Inserting overlapping and multiple gate field plates combined with silicon nitride passivation is also very effective in reducing electric field peaks near the gate edge [50], therefore reducing the tendency of electrons to leak into the surface states. Despite improvements in the surface charge trapping effects, AlGaN/GaN HFETs can still suffer from current collapse due to charge trapping effects in the deep levels of the GaN buffer region [57].

1.9 Organization and Thesis structure

In this thesis, AlGaN/GaN HFET applications in UV light detection and power electronics sector are discussed. Mainly, the research work is focussed on device fabrication and development of technology to enable enhancement mode operation in AlGaN/GaN HFETs. Material characterization on Si substrate is also presented with some methods to improve device performance.

Chapter 1: In this chapter, as discussed above an overview of GaN HFETs is presented with emphasis on material properties, device construction and applications.

Chapter 2: This chapter includes details of fabrication work carried out during this thesis. Fabrication methods for both depletion mode and enhancement mode devices are discussed. Characterization techniques which were performed to characterize the device performance are also presented. A brief description of GaN on Si growth is also presented.

Chapter 3: In this chapter, AlGaN/GaN HFETs application in UV light detection is explored. Extremely high UV light responsivity is obtained making AlGaN/GaN HFETs very attractive for UV detection purpose. The mechanism for high gain is discussed in both AlGaN barrier layer and GaN buffer region.

Chapter 4: The characterization of GaN HFETs on Si substrate with both Fe and C doping in the buffer is presented in this chapter. The methods to reduce gate surface leakage with novel chemical treatments and effect of SiN_x passivation layer are discussed. Models for surface leakage currents are identified.

Chapter 5: The highlight of this chapter is the fluorine implant technique to achieve enhancement mode operation in AlGaN/GaN HFETs. The requirement for a +3V threshold voltage in power electronics sector is met by combining the fluorine implant with a dielectric layer. The recipe for fluorine implant in AlInN/GaN HFETs is also optimized to achieve high drain current and transconductance.

Chapter 6: This chapter is about the conclusion and future work. For UV light detection, design of optimized device geometry is discussed. Some of the challenges to achieve reliable and robust enhancement mode operation with high positive threshold voltage in GaN HFETs are presented. Improved device construction methods and fabrication techniques are proposed to overcome some of the challenges.

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Chapter No 2: Fabrication and Characterization Techniques

2.1 Introduction

This chapter describes the fabrication procedures and characterization techniques used in (HFETs) Heterostructure Field Effect Transistors. A brief description of GaN on Si wafers growth conditions is also presented in this chapter.

2.2 Growth Conditions

All the wafers used in this work were grown using the metal organic chemical vapour deposition (MOCVD) technique either in Sheffield University, EPSRC National Centre for III-V Technologies or Cambridge University as a part of EPSRC grant on Silicon Compatible GaN Power Electronics. The material was grown on 2-inch sapphire substrates and 6-inch Si substrates. In MOCVD, group III elements are introduced in the form of metal organics [trimethylgallium (TMG), trimethylaluminium (TMA) and trimethylindium (TMI)]. Ammonia gas (NH_3) which serves as the source of group V elements (Nitrogen). Source gases flow over the heated substrate.

To facilitate the growth of GaN on Si substrates, a 250nm AlN nucleation layer is first grown at 1120^0C. It is used to act as a tensile stress suppressant for the top GaN buffer layer and also serves as an effective etch stop layer for TMGa. This is because TMGa reacts with Si at temperatures above 920^0C. The AlN nucleation layer is followed by a step graded or continuously graded (~0.8-1µm) AlGaN buffer layer grown at 1060^0C on top of which a GaN buffer region (~1.3-1.5µm) is grown at 1045^0C. Finally a standard $Al_{0.26}Ga_{0.74}N$ barrier layer (~27-30nm) is grown on the GaN buffer.

In the wafers used in this work, Iron (Fe) is incorporated by the use of an MO bubbler, Cp_2Fe (Ferrocene). Based on its molecular weight and vapour pressure constants, it is possible to calculate the molar flow and thus control the concentration accurately. Carbon (C) doping can also be done using a dedicated source like CBr_4 (Tetrabromomethane) or CCl_4 (Carbon Tetrachloride). But in our case, lower growth temperature (~960^0C) is used to encourage release C atoms from the metal organics to incorporate into the growing layer. Specifically, at lower temperatures, for a given NH_3 molar flux, the cracking efficiency of NH_3 will be lower than at higher temperatures. This results in less of the NH_3 reacting with TMGa or TMAl

which leads to more CH_4 groups becoming pyrolysed and therefore more C is incorporated into the GaN or AlGaN growing layers.

For the Fe doped wafers used in this work, Fe doping is always performed in the graded AlGaN buffer layer rather than GaN buffer region to avoid its influence through diffusion on the 2DEG channel transport properties. Since it is difficult to abruptly turn-off Fe due to the presence of residual gases in the MOCVD chamber because once the MO bubbler is turned off, the Fe rides on the surface of the subsequent "undoped" GaN layers until it eventually falls off completely [1]. In contrast, C offers much better control [2] and can afford to be placed closer to the 2DEG channel since it is incorporated by altering the growth temperature in the GaN buffer region. A 250nm undoped GaN channel region is grown after the C doped GaN buffer layer (~1.3-1.5µm).

2.3 Fabrication Sequence

All the results presented in this thesis were fabricated in Sheffield University, class 10,000 departmental clean room facility of EPSRC National Centre for III-V Technologies.

2.3.1 Sample Cleaving and Cleaning

Cleaving gallium nitride is slightly more difficult compared to Si or GaAs since it is a very hard material. Secondly, it is mostly grown on foreign substrates [3] e.g sapphire, SiC and Si using pseudomorphical epitaxial layer. Thus atomic misalignment due to this growth procedure further makes it difficult to cleave the samples accurately. A diamond tip scriber is used to cleave the samples and, in order to prevent any damage on epitaxial layers, cleaving is performed at the back side of the substrate. Clean glass slides are used to clamp the samples and then the scribe line is drawn at the back (rough side) of the sample in such a way that the cleaved line runs along the edge of the glass slides. As considerable force is required to cleave the samples, all glass slides were wrapped with filter papers to prevent any scratch marks on the epitaxial layer side. Once a sufficiently deep cleaved line is achieved, another glass slide is used to apply downward force on the sample while firmly holding it between the glass slides along the scribed line. In this way, fairly square samples were produced of various sizes and dimensions typically 1-3cm^2.

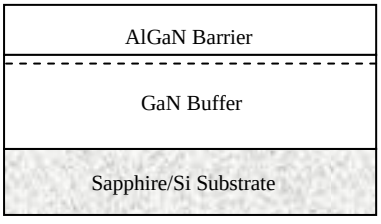
Cleaning the samples thoroughly is absolutely vital in fabrication of HFETs since its surface is very sensitive to any dust particle or dirt [4]. Sample cleaning also removes any native

oxides formed on the surface of semiconductor due to exposure to ambient atmosphere. Thus a cleaning step is performed after each fabrication sequence to ensure the sample has no dirt or dust particles on the device sensitive surface. The basic cleaning sequence for HFET involves a 3- step procedure.

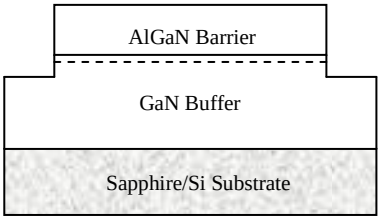
- After cleaving, sample is boiled in n-butyl acetate solution for about 1 minute.
- Then the sample is taken out and wiped with cotton bud dipped in hot n-butyl solution, to ensure no dirt particle is present on the surface.
- After that the sample is dipped in warm acetone solution for about 30 seconds.
- Then the sample is rinsed in hot Isopropyl alcohol (IPA) solution and a nitrogen gun is used to blow dry and prevent any drying stains forming on the surface.

The cleaning procedure is repeated several times until a sufficiently clean surface is achieved - typically less than 1 dirt particle in the field of view of a 100 magnification microscope lens. Cotton bud cleaning is effective in the initial process stages with no pattern formed on the sample. But after mesa isolation or ohmic contact deposition, it is not useful to use a cotton bud since any attempt to clean the sample with cotton bud would leave the contamination at the mesa edge or could even result in metal lift off. Therefore, normal 3-step cleaning is performed subsequently to clean the sample.

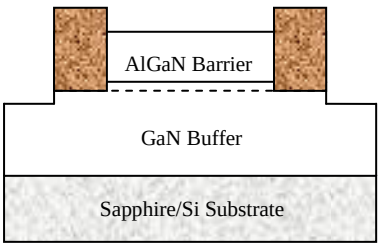
Fabrication sequence summary of HFET and MISHFET is shown in figure 2.1,



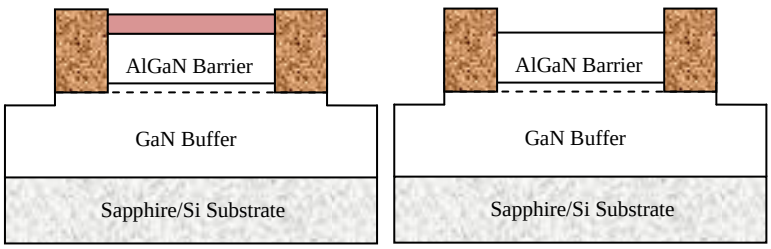
(i) Wafer cleaved 2-3 cm square samples



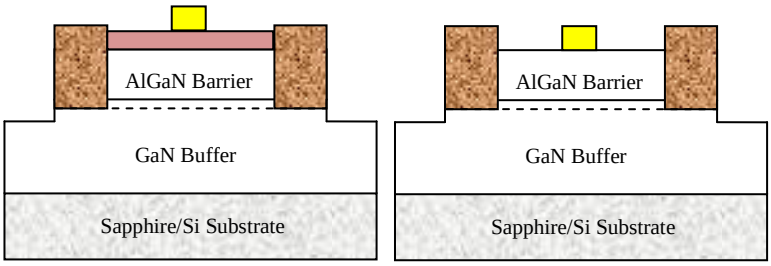
(ii) Device isolation achieved by ICP etching



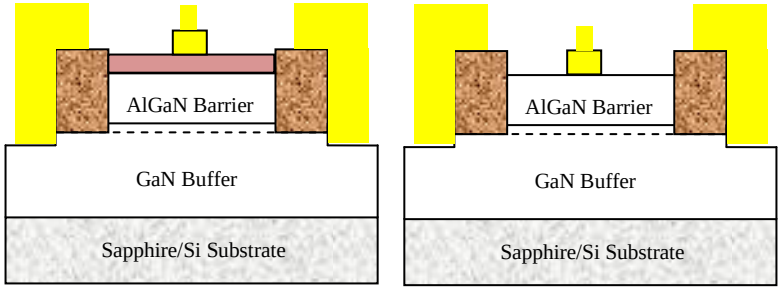
(iii) Ohmic contacts deposited and annealed



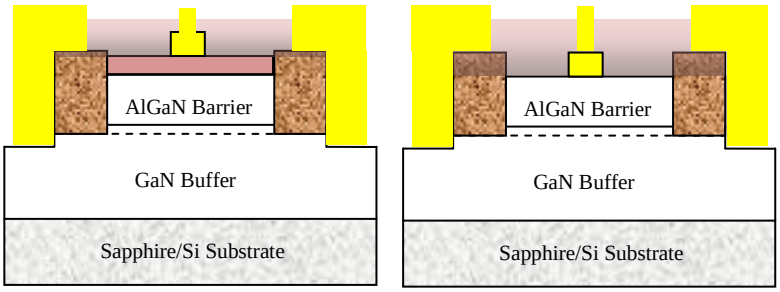
(iv) Dielectric (SiN/Al_2O_3) deposited for MISHFET)



(v) Schottky Gate contact defined



(vi) Bond Pad deposition for probing



(vii) Dielectric passivation (SiN) (optional)

Figure 2.1 Summary of Fabrication Sequence of HFET and MISHFET

2.3.2 Defining Mesa Isolation

A photolithography technique is used to define the mesa pattern and achieve device/mesa isolation in the first step before any metal deposition. Once the sample is sufficiently clean it is stuck to the glass slide using molten wax on the rough/substrate side. This improves sample

handling which is important for the lithography step. The glass slide is then baked to 100^0 C for 1 minute on the hot plate to ensure the wax spreads out uniformly and the sample is completely dry. Then the sample is placed on the photo resist spinner. Initial spinning of the sample helps monitor spin speed and a nitrogen gun blast is used to blow away any dust particle that could appear after cleaning the sample. It is then coated with BPRS 100/200 positive photo resist and spun for 30 seconds at 4000 rpm. The sample is then post baked for 30 seconds at 100^0C on the hot plate. The average thickness of the photo resist is around ~800nm measured by a dektak 3030 ST profiler.

A chromium mask plate with the desired pattern along with Karl Suss mask aligner (UV 300 or UV 400) is used to define the pattern on the semiconductor. The UV 300 mask aligner can define features down to 1µm compared to UV 400 features size of around 1.2µm. To ensure no dirt particle can be patterned on to the semiconductor, the mask plate is properly cleaned and rinsed with acetone and IPA solution. After every 10 exposures using the mask plate, it is cleaned with either decon solution or sulphuric acid which is very effective in removing hard photo resist. Cotton bud or soft toothbrush scrubbing is also done to properly clean the mask plate. Proper alignment and exposure time are key parameters in patterning the semiconductor. After exposure, the sample is developed by immersion in photo resist developer PLSI and DI solution (1:3) for 1 minute, rinsed in DI water for 30 seconds and blown dry with a nitrogen gun. The developer removes regions on the sample that were exposed to UV light, therefore selectively leaving behind the mesa pattern. Once the sample pattern is developed, a microscope is used to check for proper alignment and exposure time. It is crucial to ensure that the sample exposure time is appropriate to obtain sharp anisotropic profiles otherwise it may lead to inadequate sidewalls for the mesa which can become a problem in ohmic contact alignment. Figure 2.2 shows the figures with (a) correct, (b) overexposed and (c) underexposed features.

a) b) c)

Figure 2.2 Exposure time effect on features a) Correct exposure, b) Over exposed and c) Under exposed feature.

If the correct exposure is not achieved then the sample resist is removed by acetone solution followed by IPA cleaning and blown dry with a nitrogen gun. Then entire photolithography process is repeated with modified exposure time and alignments.

2.3.3 Inductively Coupled Plasma (ICP) Mesa Etching

After photolithography step, active device area is protected by the photo resist. The next step is to achieve device or mesa isolation through the inductively coupled plasma etching (ICP) process. ICP is a dry etching process which results in a very sharp anisotropic side walls formation. It relies on reactive plasma technology whereby a uniform plasma is produced in the chamber by inductive coils. Plasma is transferred to the wafer by electric field in the form of ions and a chemical interaction of ions with exposed sample surface results in etching of the semiconductor.

The recipe used for HFET involves three gases $SiCl_4$, Ar and Cl_2 with respective flow rates of 1.5, 4, 15 standard cubic centimetre per minute (sccm). The ICP power in the process is 450W with high RF power of 40W in the first step for 10 seconds and then low RF power of 10W in the second step to reduce plasma induced damage is used for 15-20 minutes. Etch rates are monitored by a laser reflectometer. Typical etch rates achieved in this process are 4-6nm of etching in one minute. It is necessary to etch down to the highly resistive buffer layer which in our case is 27-40nm down for AlGaN/GaN HFET to ensure proper active region isolation. Typical etch depths achieved in our case were 70-120 nm. 70nm etching is pretty good for device isolation, however higher etching depths can help in achieving sharp patterns which are useful for subsequent photolithography stages. After ICP etching dektak software is used to measure the etch depth by removing resist on the edge of the sample using a cotton bud dipped in acetone solution.

During the process of etching, the photo resist becomes hard due to bombardment of the ions and it cannot be easily removed through the standard 3-step cleaning procedure. Therefore, the sample is heated in Posis-strip EKC 830 resist remover at around 100^0 C followed by an ultrasonic bath for 5 minutes and then the 3-step cleaning is performed to ensure no residual resist is left over.

2.3.4 Ohmic Contacts Formation

After mesa isolation, ohmic contact patterning is achieved by a 2^{nd} stage photolithography step. Alignment marks formed in 1^{st} step are used to accurately pattern the features inside the

mesa boundaries. The entire method is similar to the above mentioned photolithography procedure for mesa isolation.

After photolithography, the sample is placed in an asher and then plasma ashing is performed for 1-2 minutes in oxygen plasma. The purpose of ashing is to kill any residual resist present on the pattern areas before forming ohmic contacts. The formation of native oxide on the surface of the semiconductor can be a problem for ohmic contacts, therefore the sample is immersed in HCL: DI (1:1) solution for 1 minute after ashing.

After that, sample is placed straight away into the thermal metal evaporator to avoid reformation of the oxide layer. The Edwards coating system E306A evaporator is loaded with metal coils and the sample. The metals used for ohmic contact Ti (20nm), Al (100nm), Ti (45nm) and Au (55nm) are boiled in n-butyl solution to degrease and then fitted in to suitable tungsten coil W. Coils are placed between two electrodes in the evaporator with 6cm and 12cm source to sample spacing. Higher temperature melting metals, such as titanium and nickel are placed at 12cm distance from the sample whereas lower melting metals including gold and aluminium are at 6cm distance. Once the evaporator is loaded with coils and the sample, it is pumped down to typically $2\sim4 \times 10^{-6}$ Torr. To monitor the deposition rates of the metals, an Intellemetrics IL200 thin film monitoring unit is used. All the metals are then evaporated in the above mentioned sequence with precise control of deposition rate and thickness. After metal deposition, the sample is immersed in acetone solution and left for 1-2 hours while the acetone attacks the photo resist which is coated with excess metal. A squeezy bottle of acetone can further facilitate the metal lift off by directing a jet of acetone on to the sample. An ultrasonic bath can also be used if any unwanted metal is left on the sample but care needs to be taken since too much ultrasonic bath can also remove the pattern metal. Once the excess ohmic metal is removed the sample is cleaned by the 3-step cleaning process.

2.3.5 Annealing Ohmic Contacts

Annealing of the source and drain metal contacts (Ti/Al/Ti/Au) is necessary to achieve ohmic behaviour. Rapid thermal annealing (RTA) enables the metal to diffuse into the semiconductor, thereby reducing the barrier for the carriers to tunnel across the semiconductor. The RTA system can achieve temperatures around 1000^0 C in few seconds. In HFETs generally two or three temperature stage annealing steps are performed. The sample is first annealed to 800^0C for 1 minute and then transmission line measurement

(TLM) is used to observe the ohmic behaviour, contact resistance and sheet resistance of the thin 2DEG channel. If the behaviour is not exactly ohmic then another annealing step can be performed at 850^0C for 30 seconds to attain ohmic characteristics.

It is important to perform TLM on different locations of the sample, especially for big samples to detect any variations of contact or sheet resistance across the entire sample. For samples processed in this work, contact resistance values vary from 0.4~1 ohm.mm with sheet resistance generally around 400~550 ohm per square inch.

2.3.6 Formation of Schottky Gate

In the HFET, a Schottky gate contact is formed between source and drain generally using nickel and gold metals, to modulate the 2DEG channel underneath it. A negative bias on the gate depletes the electrons from the 2DEG channel and hence stems the flow of current between the drain and source contacts. In order to form a gate contact of ~ 1 micron length, a photolithography step involving UV 300nm source mask aligner is used. The lithography step is exactly the same as explained for ohmic contacts but with 1 micron features it is very important to remove the edge bead around the edges of the sample to ensure proper pattern exposure. The edge bead is removed by covering the sample with a silicon wafer and then exposing the sample edges one after the other to UV light source. After lithography, if the pattern is not appropriate then resist is removed by immersing the samples in acetone solution followed by IPA, and then the same step is repeated until a desirable pattern is achieved. The sample is then placed in thermal metal evaporator where nickel and gold metals are evaporated to form the gate pattern. A similar metal lift off procedure is adapted as with the ohmic contacts.

2.3.7 Bond Pad Deposition

After defining the gate contact, the next step is to deposit metal bond pads which are used to electrically probe the devices and facilitate bonding the device to the header. An optical lithography step is used similar to the ohmic and gate contacts and then metal deposition is carried out in a thermal evaporator. It is essential to ash the sample after the lithography step for 2~3 minutes to remove residual resist on the surface and to ensure a good adhesive metal-semiconductor contact which can be critical while bonding the samples. Titanium and gold metals (20nm/200nm) are used for the bond pads. Typically ~220nm thick bond pad runs

down from the active device area to the highly resistive GaN surface. Metal lift off is performed similar to ohmic and gate contacts by immersing the sample in acetone solution.

2.3.8 Dielectric Deposition

The last step in fabrication of the HFET is the silicon nitride passivation deposited by Plasma-therma 790 series plasma enhanced chemical vapour deposition (PECVD). HFET passivation is normally performed to suppress the traps on the surface which result in current collapse [5]. As mentioned before, electrons from the gate are trapped at the surface resulting in the formation of a virtual gate [6] which depletes the 2DEG channel directly underneath it, resulting in current suppression. Passivating with SiN_x helps to improve this effect by burying the traps thereby improving RF characteristics of the device [5-6]. 50nm to 100nm of SiN_x is deposited whilst keeping the base plate temperature at 60^0 C and the chamber wall temperature at 300^0 C. The deposition rate of SiN_x as recorded by a Philips Ellipsometer is around 10nm/min.

In Metal Insulator Field Effect Transistors (MISHFET) fabrication, all the fabrication steps are similar to the HFET until the ohmic contact annealing. Then a thin (10~20nm) insulator is formed before the gate contact development. Again the PECVD technique can be used for dielectric deposition. SiN_x or atomic layer deposited Al_2O_3 carried out in Liverpool University as a part of EPSRC grant is used as insulators in the MISHFETs fabrication. The remaining fabrication steps are common for both HFET and MISHFET.

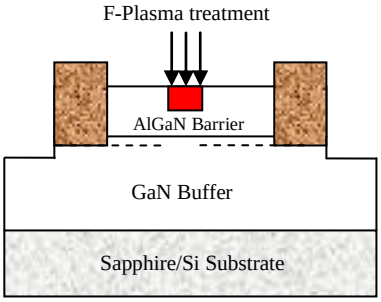
2.4 Fabrication Sequence of Enhancement Mode HFET and MISHFET

For the fabrication of normally-off or enhancement mode HFET and MISHFET, a fluorine plasma treatment is used. The fluorine ions have strong electronegativity and forms fixed negative charges in AlGaN barrier layer, effectively depleting the 2DEG charge to achieve positive threshold voltage [7]. The detailed theory of fluorine behaviour in gallium nitride HFETs is presented in the Chapter 5. The fabrication procedure is same as the HFET until the ohmic contact deposition. After ohmic contact formation, the gate photolithography is performed in a similar manner then, using the gate foot alignment, fluorine ions are incorporated underneath the gate region.

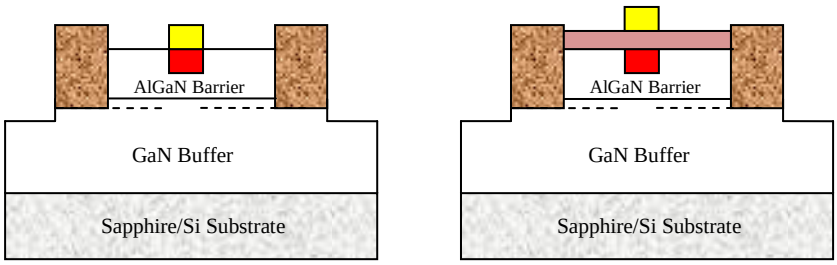
2.4.1 Fluorine Plasma treatment by ICP or RIE

After defining the 1st gate lithography, the sample is placed in an ICP or RIE chamber. Fluorine treatment is generally carried out by using CHF_3 (Trifluoromethane) gas [8], RF power is kept at 150W and gas flow of 40 sccm. In order to achieve proper normally off operation, the plasma exposure time varies from wafer to wafer depending on 2DEG concentration and barrier thickness.

For normally off HFETs the gate metal can be deposited straight after the fluorine treatment, but for MIS structures the dielectric (10~30nm) is deposited using either PECVD for SiN_x or Atomic layer Deposition for Al_2O_3 following similar procedures as mentioned above. It is imperative to clean the sample thoroughly before dielectric formation to remove all the photo resist. Posis-strip EKC 830 resist remover is used followed by three step cleaning to ensure no residual resist is left over. Later, the 2nd gate mask lithography is defined and the metal is deposited in a thermal evaporator and similar procedures are followed as for the HFET thereafter. The fabrication sequence of fluorine treatment is shown in figure 2.3,



(i) Fluorine Plasma treatment carried out in ICP or RIE



(ii) Schottky Gate contact defined for e- mode HFET and MISFET after dielectric deposition

Figure 2.3 Summary of Fluorine implant procedure in HFET and MISHFET structures.

2.5 Fabrication of Clover Leaf Hall Samples

In order to determine material characteristics including 2DEG concentration and electron mobility, Van der pauw clover leaf hall samples as shown in figure 2.4 were prepared. The detailed theory of Hall experiment is explained in Appendix B and brief fabrication procedure is described below,

- Samples were cleaved in square sizes, roughly 1 cm × 1 cm.
- The three step cleaning procedure is followed as in the normal HFET to ensure no dirt particles are present on the sample before fabrication.
- Mesa photolithography is carried out using a clover leaf mask shown in figure 2.5, and then ICP etching is performed to the highly resistive GaN buffer region (80~120nm mesa depth), similar to the HFET. The sample is then cleaned with EKC 830 resist remover at 100^0 C (ultrasonic bath ~5 min) followed by three step cleaning.
- The ohmic contact photolithography pattern is defined on the active region using alignment crosses in the mask plate. Once the desired pattern is formed, the sample is ashed for 1~2 min, then dipped in HCL: DI (1:1) solution to remove native oxide similar to the HFET.
- Finally, the sample is placed in a thermal evaporator and the ohmic contact metals (Ti 20nm/Al 100nm/Ti 45nm/Au 55nm) are evaporated to the desired thickness. After metal lift off ohmic contact annealing at 800~850^0 C for 1min or 30 seconds similar to HFET is performed.

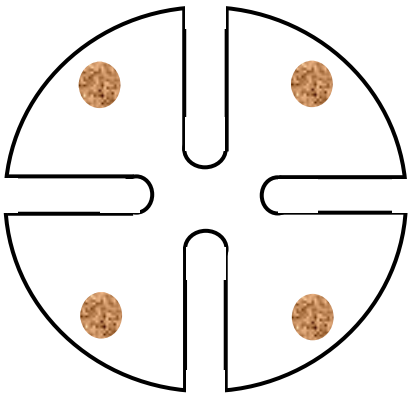


Figure 2.4 Top view of Van Der Pauw Clover leaf hall sample.

2.6 Electrical Characterization Techniques

2.6.1 Dc Current – Voltage Measurement

Since HFETs are three terminal devices, their output behaviour requires two Keithley Source Measure Units (SMUs). One SMU is used to configure the drain source bias whereas the other SMU is used to hold the gate source bias at a fixed voltage. A Keithley 2361 trigger controller is used to coordinate the two independent SMUs. The drain-source bias is normally swept from 0 V to 20 V with a step size of around 500mV at a fixed gate source bias. After every sweep of drain-source voltage, the gate bias is increased with a step size of ~ 1 V from pinch off voltage of the device. In this way, several sets of measurements are obtained for both drain and gate biasing with respect to source configuration. A typical setup for the device measurement is shown in figure 2.5.

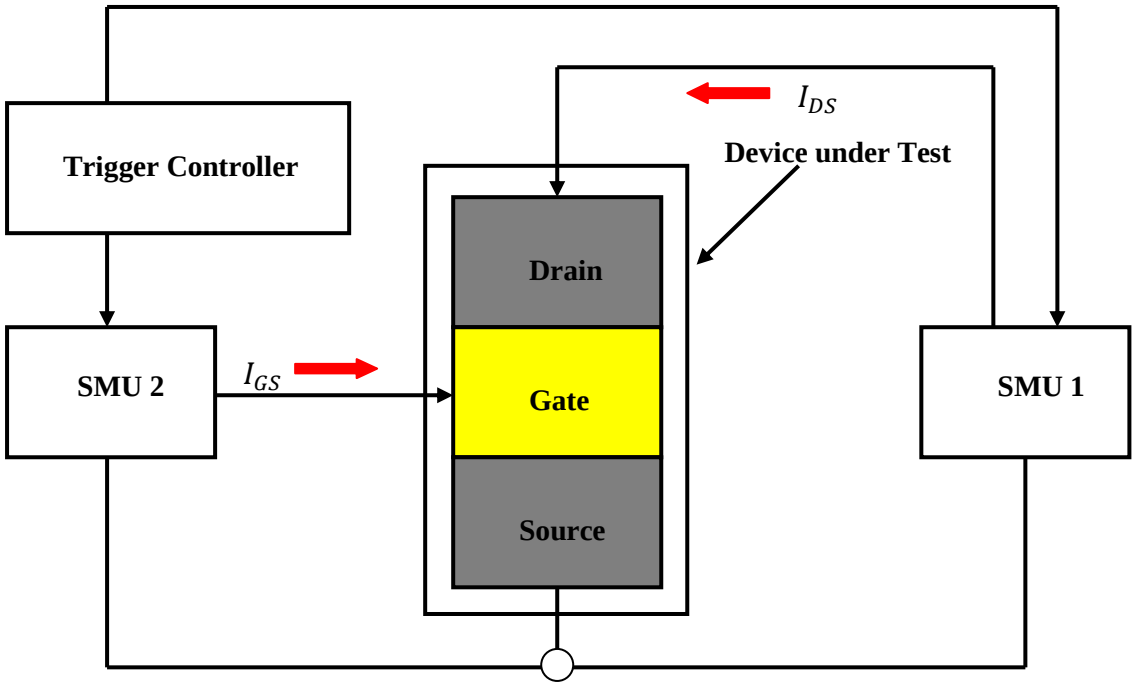


Figure 2.5 Block diagram for Current-Voltage Measurement.

2.6.2 Pulse Current – Voltage Measurement

AlGaN/GaN HFETs normally suffer from current slump or electron trapping, especially in the surface states [6]. In order to characterize the behaviour of these traps, short pulses of few nanoseconds are required. An Avtech Pulse Generator is used to produce pulses varying from

tens of nanoseconds to a few milli seconds. Either gate or drain can be configured for pulsing. Gate pulsing gives information regarding the surface traps and drain pulsing is normally used to evaluate the thermal heating effect in these devices. The circuit diagrams are in figure 2.6 and 2.7.

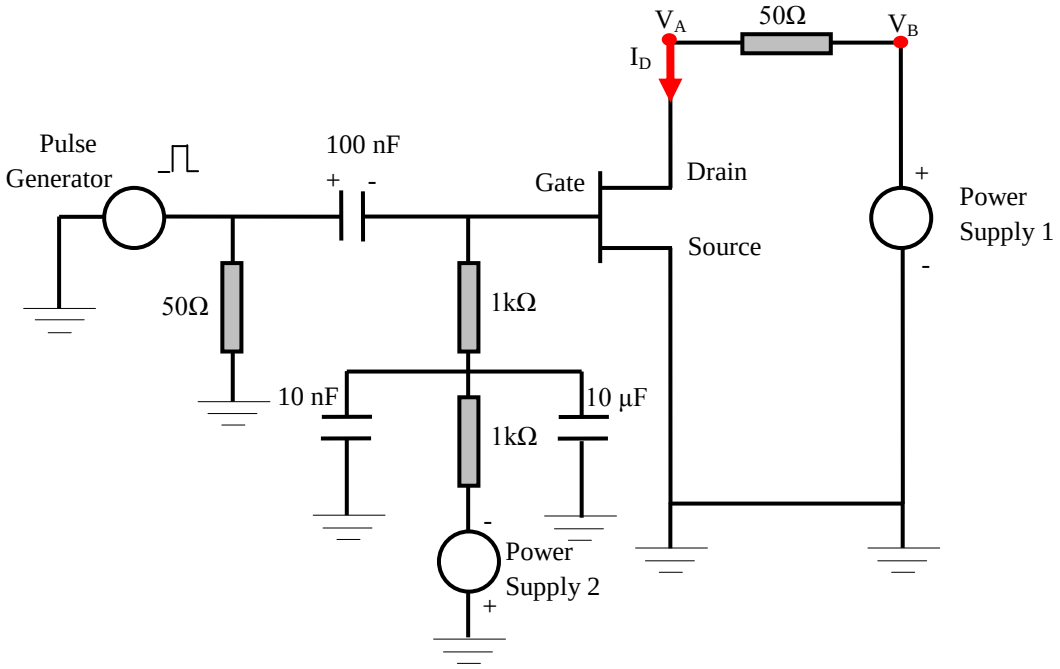


Figure 2.6 Gate pulse configuration for current-voltage measurement.

The Pulse generator is impedance matched with 50 ohm resistor. Power supply 1 is used to supply a fixed drain bias whereas the drain current is measured by using the 50 ohm resistor. The gate is pulsed from the pinch off voltage (typically -4~-8V) to 0 Volts by the pulse generator. Power supply 2 is used to hold gate bias at pinch-off when not pulsed.

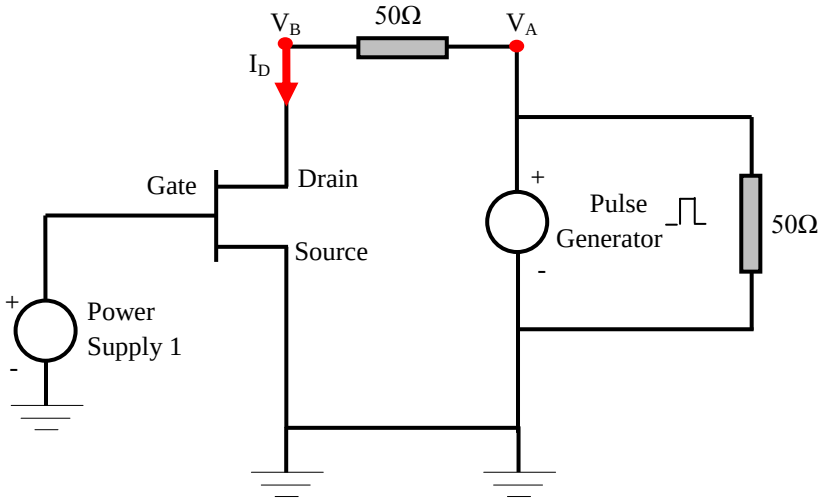


Figure 2.7 Drain pulse configuration for current-voltage measurement.

In the drain pulse configuration shown in figure 2.8, the pulse generator is used at the drain side and power supply 1 is used to bias the gate at fixed voltage (typically 0V or -1V). Again the drain current is calculated using the 50 ohm resistor. The pulsed drain bias is used to reduce self heating effects in the device.

2.6.3 UV Response Measurement

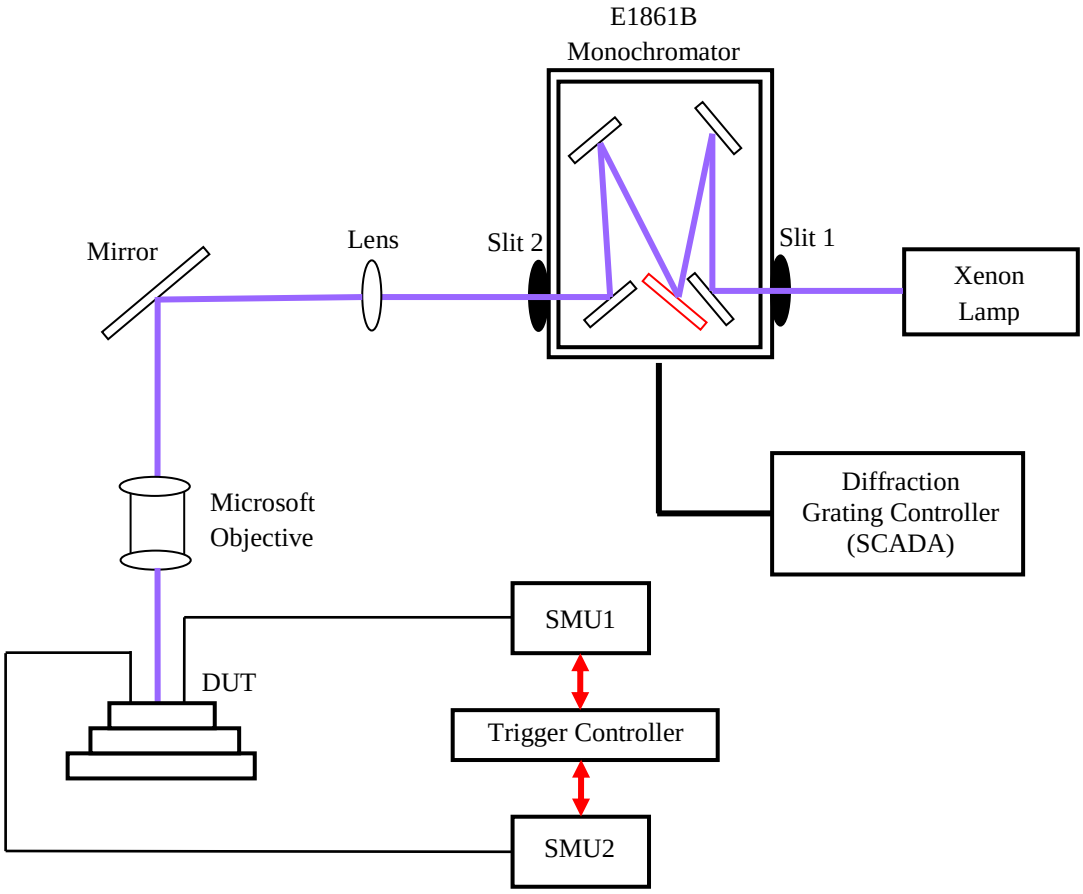


Figure 2.8 UV Response Measurement Setup.

The setup for the UV response measurement of HFETs is shown in the figure 2.8. Ultraviolet light detection mechanism in the HFETs is presented in Chapter 3. A Xenon lamp is used as a light source together with a Monochromator (E1861B from Horiba) to achieve a monochromatic beam of light. This beam was focused on the active region of the device using several lenses and mirrors. The optical power intensity of the beam was measured using a calibrated Si photo diode power meter from Thorlabs. The output wavelength is tuned by varying the position of the diffraction grating (1200 grooves/mm) controlled by a Supervisory Control and Data Acquisition (SCADA) System. The wavelengths were tuned from 250nm to 400nm to fully characterize the response in the UV region.

2.6.4 Hall Effect Measurement

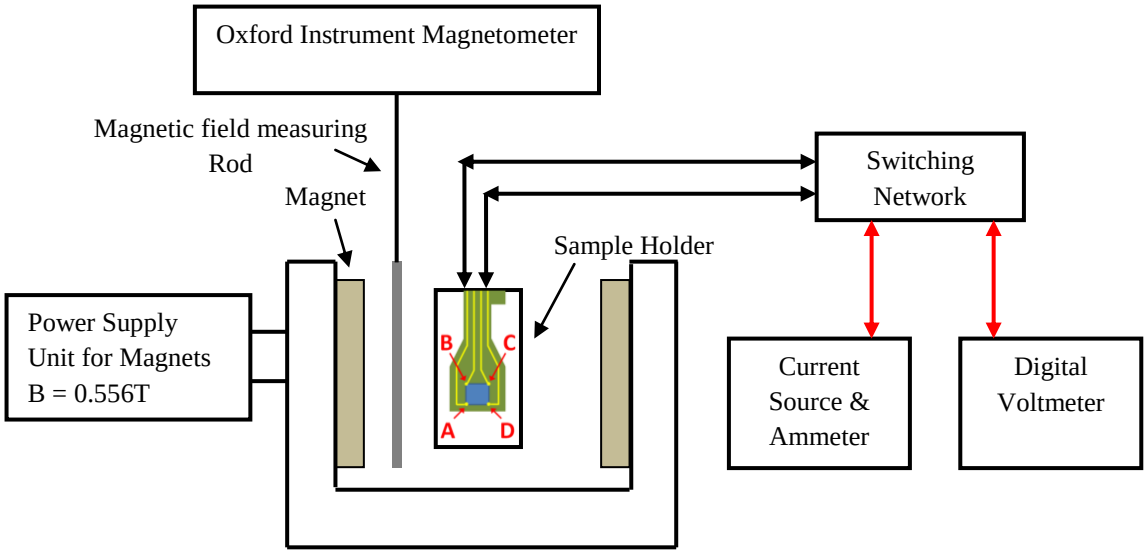


Figure 2.9 Hall Effect Measurement Setup.

The Hall measurement setup is illustrated in figure 2.9 and the theoretical explanation of the Hall experiment is explained in Appendix B. To reduce the errors in resisitivity and Hall mobility, clover leaf shaped samples are used. The sample is placed in a thermal flask positioned between a pair of magnet poles, such that the applied magnetic field is perpendicular to the sample surface. The sample is mounted on a printed circuit board with clipping pins for electrically connecting the four contacts on the clover leaf sample. The output probes from the printed circuit board are connected to the switching network where the desired current sourcing and voltage sensing configuration can be altered for each measurement step. In order to minimize the errors generated during measurement each resistance is calculated from two configurations by altering the flow of current in the forward and reverse direction using a switching network (see Appendix B). The measurement is conducted in the dark to ensure accurate reading. The magnitude of the magnetic field is 0.556 Tesla.

2.6.5 Capacitance Voltage Measurement

Capacitance voltage (C-V) measurements are frequently used in semiconductor studies to determine parameters such as doping profile, depletion width, barrier height, threshold voltage [9] e.t.c. In this work C-V measurements are preformed mainly to evaluate the 2DEG

charge concentration, barrier thickness and dielectric thickness for the MIS structures. A Hewlett Packard HP4275A inductor, capacitor and resistor (LCR) meter is used to generate low and high frequency signals (10 KHz to 1MHz) with a DC bias voltage. The C-V software gathers all the data including impedance, phase angle and capacitance. The capacitance is then plotted against DC bias voltage. In order to achieve valid C-V profile it is necessary to have a phase angle close to 90 degrees which reflects negligible leakage current through the device.

2.6.6 Transmission Line Measurement

Transmission Line Measurement (TLM) is an important tool to evaluate the contact resistance and sheet resistance of the devices [9-10]. TLM can help optimize the annealing time required to achieve a good ohmic contact between semiconductor and the metal. A higher contact resistance is detrimental to device performance as it would lower the output drain current and increase turn-on resistance of the device. As a result, knee voltage is increased and this reduces output power available and degrades high frequency performance. A brief theory of TLM technique is given in Appendix A. In TLM contact resistances of equal size pads (~125μm) are plotted against the varying gap spacing between the contacts. This graph gives a straight line which is extrapolated to zero gap, this gives the sum of contact resistances of two probed pads and sheet resistance is the slope of this line. Typical contact resistance value ranges from 0.4~1 ohm-mm and sheet resistance is 400~550 ohm/sq. All the TLM performed in this work were on rectangular geometries with one dimensional current flow only and device isolation was achieved by ICP etching. Circular TLM option is also available which eliminates the need for mesa isolation by using annular geometry but the area required is much larger compared to rectangular geometry.

2.6 References

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Chapter No: 3 UV Detection Mechanism in AlGaN/GaN HFETs

3.1 Introduction

In this Chapter, Ultraviolet light detection mechanisms in the AlGaN/GaN HFET are discussed. In the first section, absorption in the AlGaN barrier layer is discussed and in the second section absorption mechanism in GaN buffer layer is presented. A very high dc responsivity (~4.3×10^7 A/W) value is reported and gain mechanisms in the devices are shown to be due to a photo voltage effect in both the AlGaN barrier layer and the GaN buffer layer. All the work presented in this chapter is published in IEEE Transaction on Electron Devices.

In recent years, considerable progress has been made in the GaN based UV light detectors [1-3]. GaN is particularly suitable for UV light detection due to its direct wide band gap and robust nature. GaN pin diodes [4], Schottky diodes [5] and metal semiconductor metal (MSM) based photo detectors [6] have been demonstrated by various researchers. In contrast to silicon based UV photo detectors, GaN offers improved performance at elevated temperatures and it can be used in space applications because of its higher resilience to radiation. In comparison with other UV detectors based on photo conductors, AlGaN/GaN heterostructure based detectors [7] can offer high internal gain which is favoured by a very highly conductive 2DEG channel at the heterostructure interface and the associated short transit time under the gate. These detectors have wide applications in military and commercial areas such as flame monitoring, missile plume detection, UV environmental monitoring, space ozone monitoring, imaging arrays and others. By changing the mole fraction of AlGaN layer, the cut-off wavelength can be tuned from 200 – 365 nm to suit a particular requirement. The inherent advantage of using AlGaN/GaN HFET as a UV detector is a high response, ultra high sensitivity, integration with the mature HFET technology and flexibility to operate at low voltage regimes, particularly less than tens of volts.

AlGaN/GaN based HFETs have been explored in various sensor applications in modern years such as biochemical sensing including, pH monitoring, glucose sensing and gas sensing applications [8-10]. Almost all these sensor applications take advantage of the HFET ability to detect small variations in charge status of surface states density. As discussed before, due to a very strong piezoelectric polarization in AlGaN, a 2D electron gas is accumulated near the AlGaN/GaN interface and net positive charge surface states are formed in order to

maintain charge neutrality as shown in figure 3.1. Any change in the charge status of surface states would imply a change in the 2DEG charge concentration in order to achieve the charge neutrality balance [11]. Therefore AlGaN/GaN based devices would be extremely sensitive to variations in surface charge which forms the basis of various sensor applications.

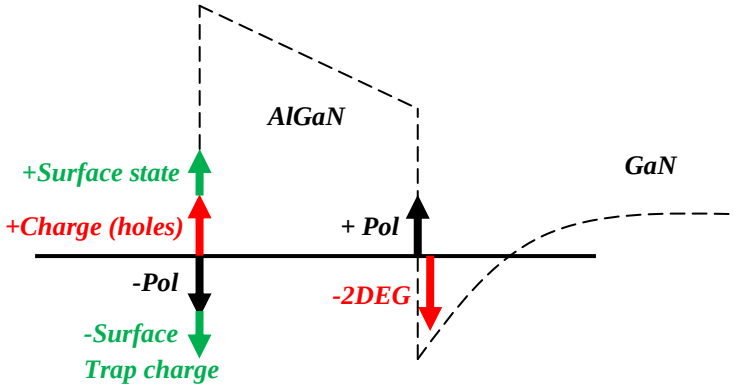


Figure 3.1 Conduction band diagram of AlGaN/GaN heterostructure, showing charge balance.

An AlGaN/GaN HFET based UV detector was first demonstrated by Khan [12] with a maximum responsivity of around 3000 A/W. In recent years, responsivity values of ~ 10^6 A/W have been demonstrated [13-14]. However there is a lack of understanding for such high gain mechanism. Various research groups have reported enhanced conductivity of the 2DEG channel due to some surface electron trapping mechanism [15-17] but a detailed understanding and analytical model of gain mechanism is not fully demonstrated. It was reported that upon the UV illumination, electrons trapped in the surface states are released which enhances the 2DEG concentration [16] since for every electron trapped in the surface state is compensated by the electron from the 2DEG channel. Some reports [15-19] have considered absorption in the GaN buffer layer but the mechanisms of the photo generated hole transport in this region is not explained. UV illumination of the devices is also studied to understand the trapping transient and mechanism in AlGaN/GaN HFETs [20]. In this study, we present detailed measurements and compare these with analyses on UV absorption in HFETs.

3.2 UV illumination of AlGaN/GaN HFET

The typical output characteristic of AlGaN/GaN HFET under Ultraviolet light illumination with 275nm LED is shown in the figure 3.2.

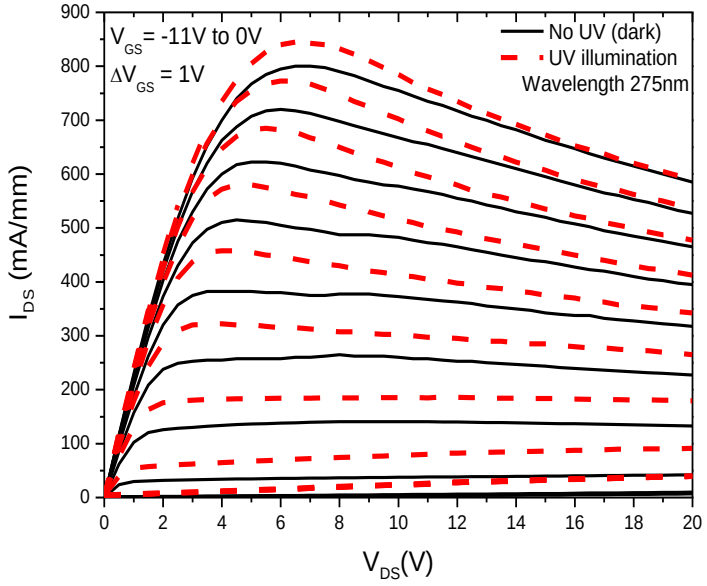


Figure 3.2 AlGaN/GaN HFET output characteristics in dark and under UV illumination.

With UV illumination, an increase in the drain source current is observed which is due to the contribution of photo generated electron hole pairs in both the AlGaN barrier layer and the GaN buffer region depending on the wavelength of illumination. The maximum increase in drain current is near the knee voltage region which is just before the onset of the conventional saturation region. At higher drain source bias, photo response and drain current both reduce subsequently which is attributed to self heating effect in AlGaN/GaN HFETs since these devices were fabricated on the sapphire substrate which has a poor thermal conductivity. The reduction in photo response with increase in temperature is due to the decrease in induced open circuit photo voltage which is well known in solar cells [21] and discussed later in section 3.4.3.

The proposed ultraviolet light absorption mechanism is further illustrated in figure 3.3(a) with electron hole pair generation in both the barrier (AlGaN) and the buffer (GaN) layers with 275nm wavelength. However, photon generation depends on the wavelength of

absorption and band gap energy. For the barrier layer, band gap energy depends on aluminium mole fractions Al(x) and can be extracted by using the following expression [22],

$$E_g\ (Al_xGa_{1-x}N) = 3.42eV + x2.86eV - x\ (1-x)\ 1.0eV \qquad [3.1]$$

where x = Al fraction

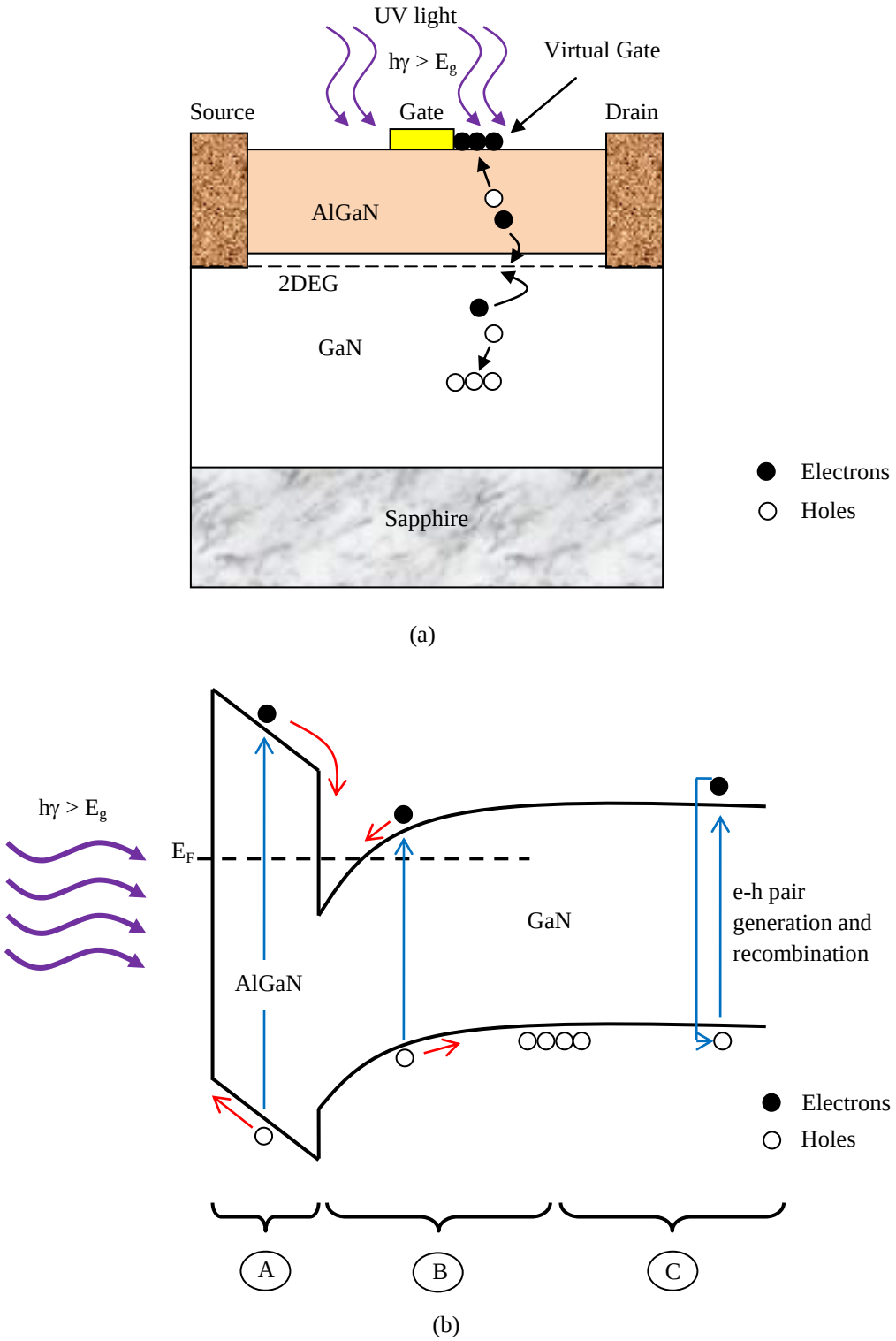


Figure 3.3 (a) AlGaN/GaN HFET under UV illumination showing the electron-hole pair generation and movement. (b) Equivalent mechanisms within the device band structure.

Figure 3.3(b) shows the electron hole pair generation in the heterostructure band diagram upon UV excitation. There can be three regions of photon absorption as shown in the figure 3.3(b),

A. Region A covers the AlGaN barrier layer, typically 20~40nm, only photons with energy greater than AlGaN band gap would be able to generate electron hole pairs in this region.
B. Region B is the buffer GaN region, typically 2-3µm covering from the 2DEG channel to the buffer layer.
C. Region C is deep inside the GaN buffer, covering up to GaN buffer substrate interface. Any electron hole pairs generated in this region would recombine immediately and would not contribute to any photo response.

Therefore, there can be two regions which contribute to photo response of the device namely AlGaN barrier region A and GaN buffer region B. We will now analyze the two regions separately in the following sections.

3.3 Absorption in AlGaN barrier layer

When electron hole pairs are created in the AlGaN barrier layer (region A), electrons move in to the 2DEG channel due to built in polarization field and the holes are swept to the surface, as shown in figure 3.4.

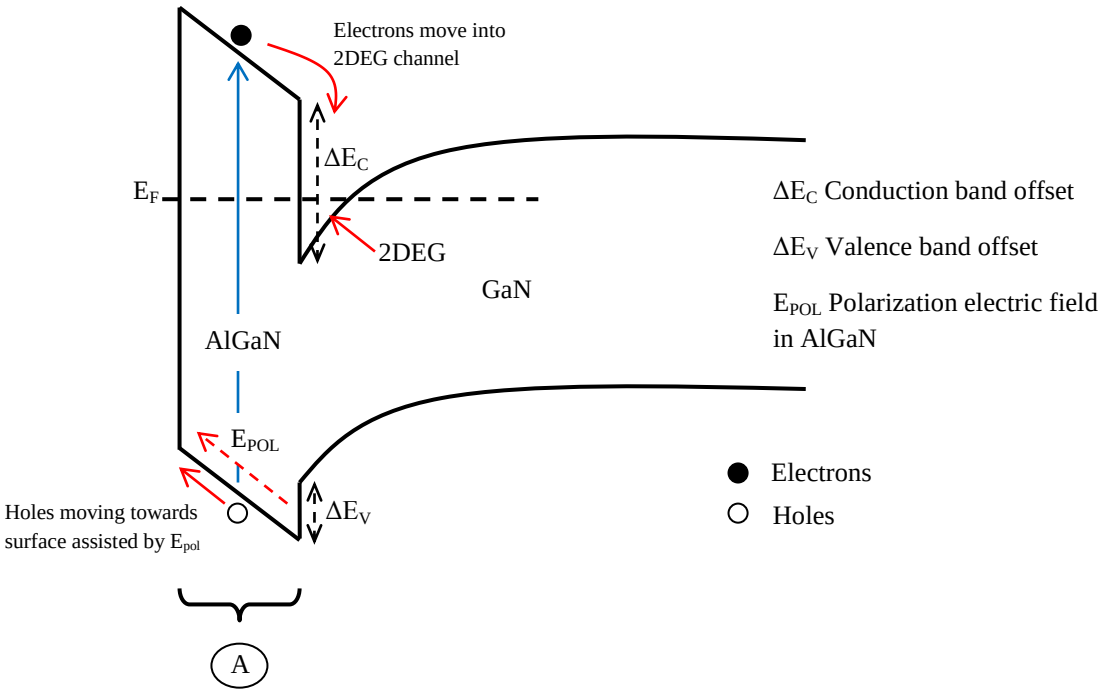


Figure 3.4 Band structure showing e-h pair generation in AlGaN barrier layer.

The magnitude of electric field in the AlGaN barrier can be estimated using the following expression [23], which is equal to band bending of the AlGaN divided by its thickness

$$E_{AlGaN} = \frac{\emptyset_b + \Delta - \Delta E_c}{d} \qquad [3.2]$$

$\emptyset_b$ is the AlGaN surface potential, ΔE_c is conduction band offset, d is the AlGaN thickness and Δ is calculated as [23],

$$\Delta = \frac{n_s \pi \hbar^2}{q^2 m^*} \qquad [3.2.1]$$

n_s is the 2DEG charge density, $\hbar$ is the Planck's constant, q is the electron charge and m^* is the effective electron mass ($m^*=0.22m_e$).

The calculated magnitude of the vertical polarization electric field in the AlGaN between the surface and the channel is more than 10 times higher than any applied lateral electric field between the source and drain contacts (estimated at 0.21 MV/cm and 0.014 MV/cm respectively). Therefore, under such a high vertical polarization electric field, and because of the shorter distance to the surface compared to the source over most of the active absorbing region, nearly all of the holes generated in the AlGaN region would move towards the surface (gate) [24] rather than source. And any applied negative bias at the gate would reinforce the polarization electric field, encouraging more holes to move towards the gate.

The accumulation of holes on the surface would neutralize the trapped electrons forming virtual gate, and as a consequence drain current would increase [24]. Any change in the charge status of surface states would be directly reflected in the 2DEG electron sheet concentration to maintained charge neutrality. This change in 2DEG electron sheet concentration can be directly measured by the change in channel conductivity σ_s, as given in equation 3.3 which, under UV illumination, would increase due to the combined effect of electrons contributing to the 2DEG well and holes moving towards the surface to neutralize trapped electrons.

$$\Delta\sigma_s = q\mu_n \Delta N_{2DEG} \qquad [3.3]$$

ΔN_{2DEG} is the variation in 2DEG electron concentration, μ_n is the electron mobility and q is the electron charge.

3.3.1 Role of Schottky Gate Contact

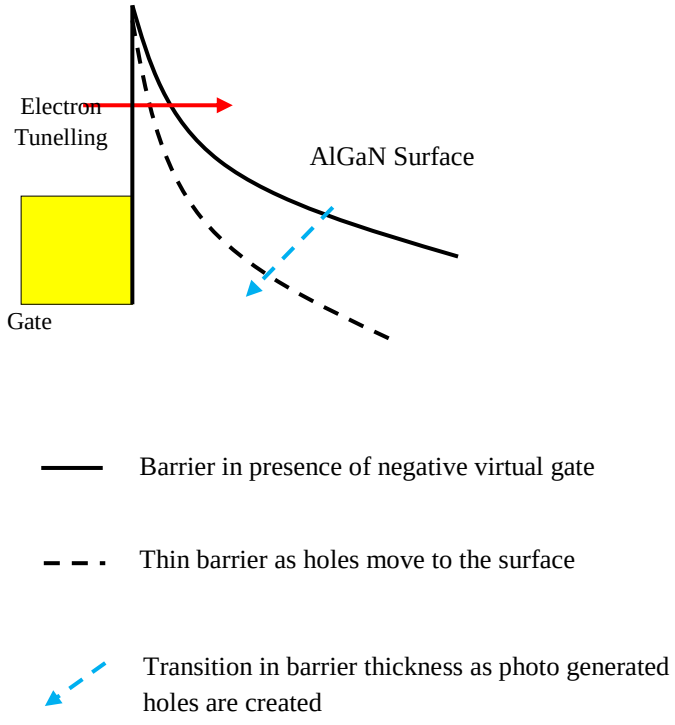
The optical gain in the HFET (assuming that all the light is absorbed) can be expressed as the ratio of effective lifetime of the photo generated holes to the transit time of electrons in the 2DEG channel.

$$G = \frac{\tau_h}{t_e} \qquad [3.4]$$

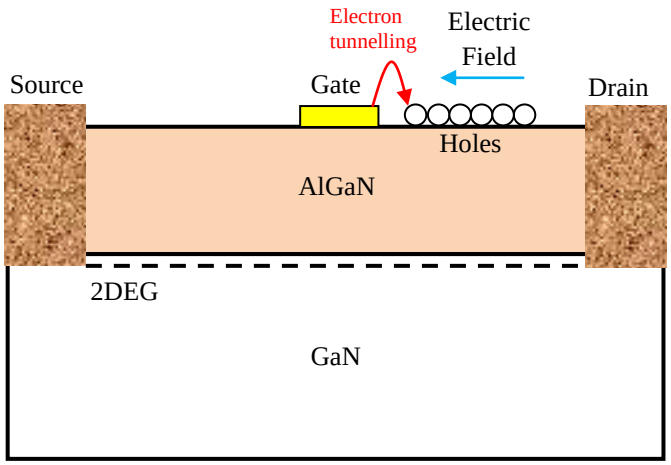
τ_h is the effective lifetime of hole whereas t_e is the transit time of electron underneath the gate. If the lifetime of holes is much greater than the transit time of electron then it would give rise to optical gain as many electrons would be able to traverse the electric circuit before recombining with holes. In an open circuit configuration where the holes cannot escape other than by recombination, the lifetime of the holes is enhanced by the barrier height which separates the photo generated electron hole pairs. Now in the presence of a Schottky gate contact, photo generated holes on the surface can leak away, affecting the life time of holes.

From the absorption coefficients of the AlGaN barrier layer [25] we estimated that about 30-40% of the 275nm light will be absorbed in the 40 nm thick barrier layer. In the case of a gated structure with trapped surface electrons outside the gate, photo generated holes produce an effective positive virtual gate bias. However, this net increase in positive surface charge encourages the gate metal to supply negative electrons through a tunnelling mechanism as explained in figure 3.5. The optically generated positive charge, together with the applied negative gate bias (with respect to the drain), narrows the barrier (broken line in figure. 3.5(a)) and enhances the electron tunnelling.

The holes accumulated along the surface near the gate metal edge are basically annihilated by the electrons or swept into the gate metal under the influence of large electric field present between the drain and gate region. However, the rate at which the gate can supply electrons to neutralize holes is limited by the electron injection rate and surface mobility of electrons. The electron transport along the surface is by a hopping conduction mechanism [26]. The lifetime of holes would thus be dominated by the slowest of the two processes namely electron injection and electron surface hopping conduction.



(a)

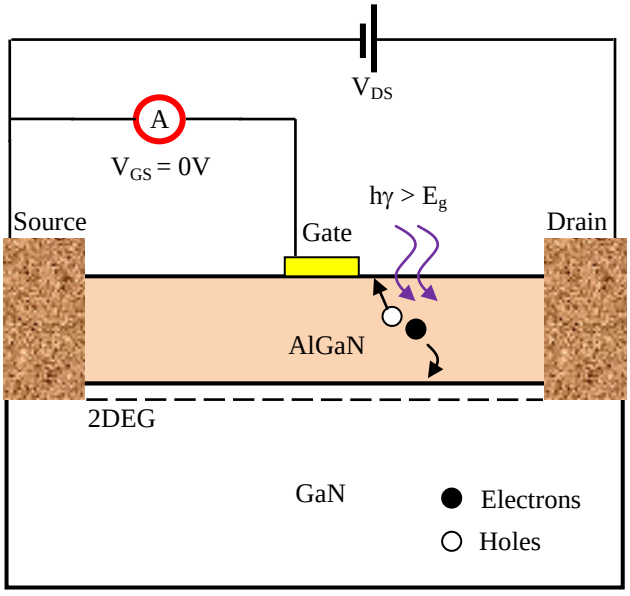


(b)

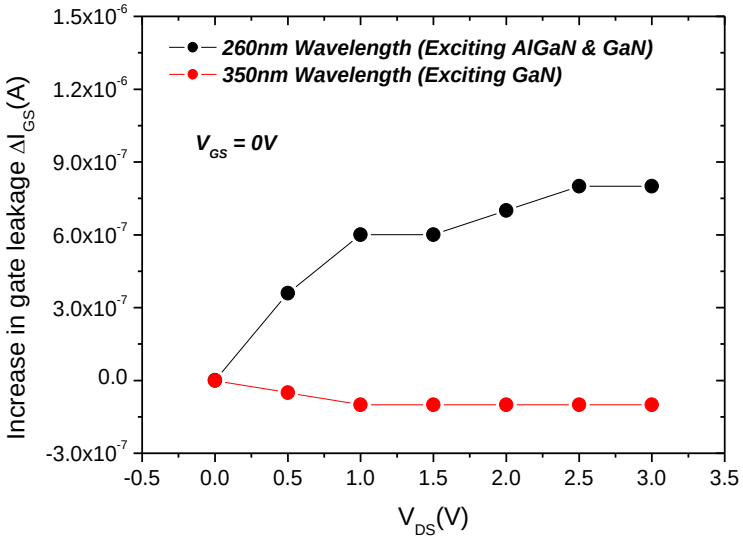
Figure 3.5 (a) Electrons tunnel through gate edge as holes accumulate along the surface and reduce effective barrier thickness (b) AlGaN/GaN HFET showing electron tunnelling under the influence of electric field.

3.3.2 Gate Leakage Measurement

In order to observe the change in gate current due to photo generated electron hole pairs in the AlGaN barrier layer, the device arrangement as shown in figure 3.6(a) was used.



(a)



(b)

Figure 3.6 (a) Device circuit configuration to monitor gate leakage (b) Increase in gate leakage under UV monochromatic wavelengths of 260nm and 350nm.

In this device circuit configuration, the drain source voltage is applied by the source measurement unit (SMU) whereas the gate to source bias is held at 0 volts in order to avoid any gate leakage effects. However, an electric field is present between the drain and gate terminal to induce electron tunnelling which can be observed by the Ammeter. The AlGaN/GaN HFET in the above circuit configuration was excited by UV monochromatic wavelengths of 260nm and 350nm and results are shown in figure 3.6(b). With shorter wavelength of 260nm which excites both the AlGaN barrier layer and the GaN buffer region, the change in gate current was of the orders 10^{-7} A whereas with longer wavelength of 350nm which only excite the buffer GaN region and photon energy is insufficient to create any electron hole pairs in the AlGaN barrier layer almost no change in gate leakage was observed. Even though the change in gate leakage was very small due to limited powers of UV monochromator source, it highlights the fact that increase in gate leakage is due to holes reaching the surface and only when the AlGaN barrier layer is excited [24]. Since the UV monochromator intensities were too small to observe any significant change in gate leakage at zero gate source bias, a higher power laser of wavelength 244nm with varying intensities adjusted by neutral density filters was used to measure the gate current.

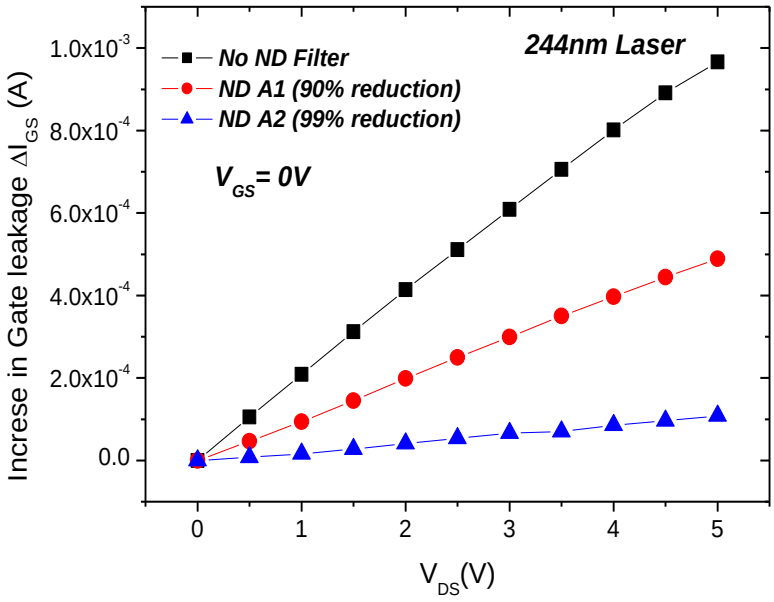


Figure 3.7 Increase in gate current under 244 nm laser light against drain bias with different neutral density filters.

The results are shown in figure 3.7. An increase in gate leakage can be observed with an increase in both drain source bias and UV intensities. This effect is due to the photo current generated in the AlGaN barrier region only. A highly nonlinear dependence of gate leakage is observed with changing UV intensities and it is quite difficult to explain due to the complex combination of drain gate electric field and photo generated holes on the surface near gate edge. The gate leakage is expected to increase under the influence of drain bias since a higher electric field would encourage more electrons to tunnel across the barrier to neutralize photo generated holes. However, at low drain gate bias insufficient gate injected electrons are available to neutralize the photo generated holes and a voltage between the surface and channel is formed due to movement of holes towards the surface. As these holes build up along the surface, the piezoelectric field in the barrier layer would collapse which causes increased recombination of photo generated carriers in the barrier layer. Under such conditions a reduction in photo response would be apparent since the barrier which separates the photo generated electron hole pairs diminishes and recombination dominates.

3.3.3 Gate Lag Measurement

To further investigate the role of surface hopping conduction, gate lag measurements were used. Gate lag measurements are normally used to study charge trapping effects in AlGaN/GaN HFETs [27]. Charge trapping in the device is reflected in gate lag, which is a delayed response of channel current modulated by the gate voltage. In these measurements, the gate is pulse biased with the pulse width of the orders of few nanoseconds. The channel is switched from an off-state where the gate is held at -10V (pinch-off voltage, V_p~-8V) to an "on" state with 0V gate bias and the drain source bias is held at 10V. The transient response or lag in the drain current as the channel is switched on is shown in the figure 3.8.

In the off-state ,where the gate is negatively biased, surface traps are filled with electrons injected from the gate but as the device is turned on with 0V gate bias there is a delay in built up of the drain current as electrons trapped in the surface states are emptied to reduce virtual gate effect. Gate lag measurements were performed in the dark at 20^{o}C, at 140^{o}C and under 275nm LED illumination (20^{o}C) as shown in figure 3.10. In the dark, a distinctive time lag in the drain current is quite apparent as the charge state of the surface states need time to respond to the change in gate voltage.

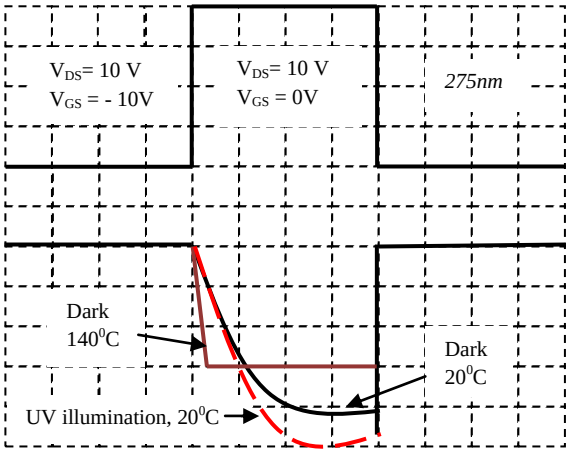


Figure 3.8 Gate lag measurement, gate was switched from 'pinch-off' to 'on' state. The increase in drain current was observed under UV illumination. Grid square corresponds to 1µs.

It can be seen that the gate lag or delay in response reduces in the dark when the temperature is increased from 20^{o}C to 140^{o}C. This is due to the thermally activated surface hopping conduction mechanism which increases with increase in temperature, thereby effecting the life time of trapped electrons in surface states. There is also a reduction in drain current magnitude from 20^{o}C to 140^{o}C which is due to increased phonon scattering mechanism at high temperature causing a reduction in 2DEG electron mobility. Under UV illumination of 275nm at 20^{o}C, the magnitude of drain current increases over the dark but the recovery time in response to gate bias is almost the same. This signifies that only temperature has an influence on the carrier's lifetimes on the surface.

3.3.4 Analysis for absorption in AlGaN layer

Now consider the analysis of UV light absorption mechanism in the AlGaN barrier layer. The barrier layer thickness is about 40nm extracted from the C-V measurement. From absorption coefficients of AlGaN it is estimated that about 30-40% of 275nm UV light would be absorbed in this region. The optical gain mechanism in this region (AlGaN barrier) is due to the ultra high sensitivity of the HFET to respond to any change in charge status of the surface states which are modified by UV illumination. As mentioned before, a change in the charge on the surface states is counter balanced by an equal and opposite change in the 2DEG channel concentration.

The surface charge per unit area on the AlGaN barrier layer is the product of the primary photocurrent density, J_{ph1}, and the effective hole lifetime on the surface, τ_h, i.e. $Q_s = J_{ph1} \times \tau_h$, and the photo voltage generated in this region can be defined as,

$$V_{ph1} = \frac{Q_s}{C_g} = \frac{J_{ph1} \times \tau_h}{C_g} \quad [3.5]$$

where C_g is the capacitance per unit area between the 2DEG channel and surface. From the definition of transconductance, g_{m1}, [28] for the HFET, the induced change in drain current due to the photo voltage can be expressed as,

$$\Delta I_{D1} = g_{m1} \times V_{ph1} \quad [3.6]$$

Substituting for the photo voltage,

$$\Delta I_{D1} = g_{m1} \times \frac{J_{ph1} \times \tau_h}{C_g} \quad [3.7]$$

Extending the definition of g_{m1}, [13]

$$g_{m1} = \frac{C_{gs}}{t_e} A \quad [3.8]$$

where t_e is the transit time of the channel electrons under the virtual gate and A is the active surface area of the device. Therefore, using this expression and converting from photo current density to photo current,

$$\Delta I_{D1} = I_{ph1} \times \frac{\tau_h}{t_e} \quad [3.9]$$

From equations 3.6 and 3.9 the link between the transistor amplification action, characterized by g_{m1}, and the traditional photoconductor gain given by the ratio of the hole lifetime and electron transit time [29-30] can be established. The gate lag measurement reveals that the electron surface transport, and hence $\tau_{h,}$ *is* thermally activated.

3.4 Absorption in GaN buffer region

The GaN buffer region is about 2-3µm thick and unintentionally doped. In the past several reports have considered UV absorption in the GaN buffer region of AlGaN/GaN HFET [15-19]. When electron hole pairs are created in the GaN buffer region, electrons drift into the 2DEG channel due to the built in band bending of the heterostructure as shown in the figure 3.3. However, the transport mechanisms of photo generated holes as proposed in the literature is not clear. It was first proposed by Vetury et al [16] that when holes are created in the GaN buffer, they are pulled towards the surface under the influence of electric field in AlGaN barrier. Later on Yun Chang [18] proposed that excessive holes are swept to the surface by absorbing thermal energy from UV illumination and neutralize charged surface states. However in our view [24], holes created in the GaN buffer region cannot be swept towards the surface because,

A. In order to move towards the surface, holes must overcome a significant barrier height presented by the heterostructure valence band discontinuity, ΔE_V, calculated to be ~0.12eV which is roughly five times greater than room temperature thermal voltage of 26mV.
B. Secondly, in order to drift towards the surface, holes first need to move in close proximity of the AlGaN/GaN interface overcoming the repelling built in electric field present in the GaN buffer due to band bending, as shown in the figure 3.9. Instead this built in field would always pull the holes towards the GaN buffer/substrate interface in opposite direction to surface.

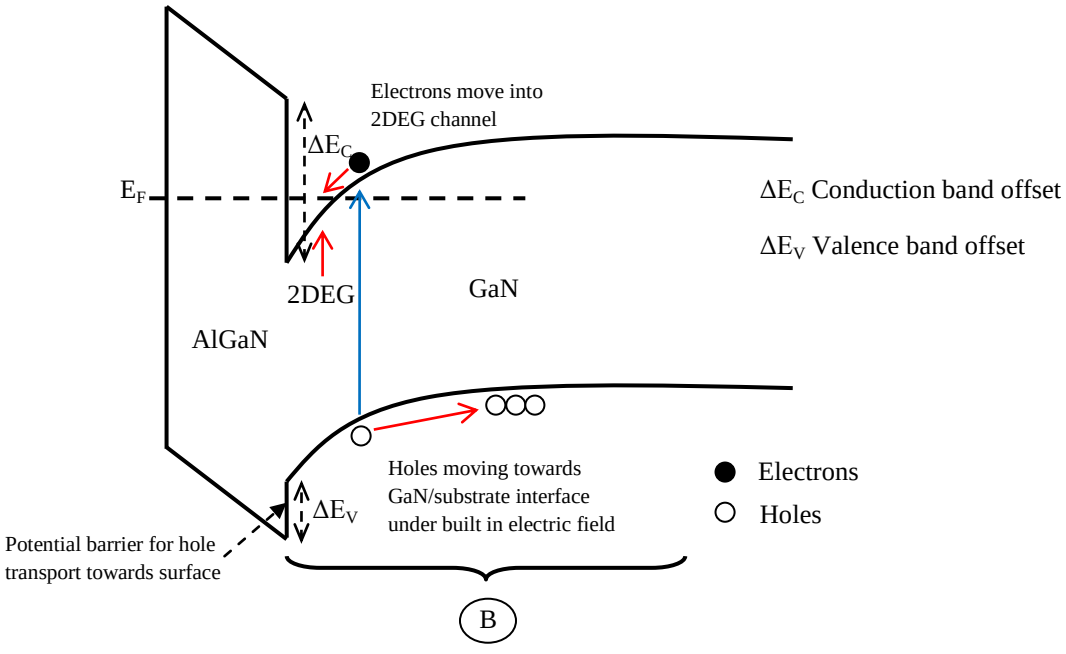


Figure 3.9 Band structure showing e-h pair generation and transport in GaN buffer region.

3.4.1 Photo voltage Effect in GaN buffer

The holes would therefore move towards the GaN/substrate interface under the influence of the electric field which is present due to band bending in the heterostructure. In contrast to the AlGaN barrier layer, region A, the excess holes generated in region B will not be able to escape due to the presence of the insulating substrate and will accumulate near the GaN/substrate interface. A photo voltage is thus generated in this region due to the separation of electron and hole pairs. The effective life time of holes would depend on the barrier height which separates the photo generated carriers. The barrier heights are different for holes produced in the AlGaN barrier, region A, and the GaN buffer layer, region B. The effective lifetime of holes then becomes,

$$\tau_h^* = \tau_h \exp\left(\frac{qV_b}{kT}\right) \qquad [3.10]$$

where V_b is the effective barrier height, q is the electronic charge, k is the Boltzmann constant and T is the temperature in Kelvin.

Under illumination a forward biased photo voltage will be produced due to the separation of the electron and hole pairs, effectively reducing the barrier height. Therefore, the expression for the gain can be modified as,

$$G = \frac{\tau_h}{t_e} \exp\left(\frac{(qV_b - V_{ph2})}{kT}\right) \qquad [3.11]$$

where, V_{ph2} is the photo voltage generated due to UV illumination.

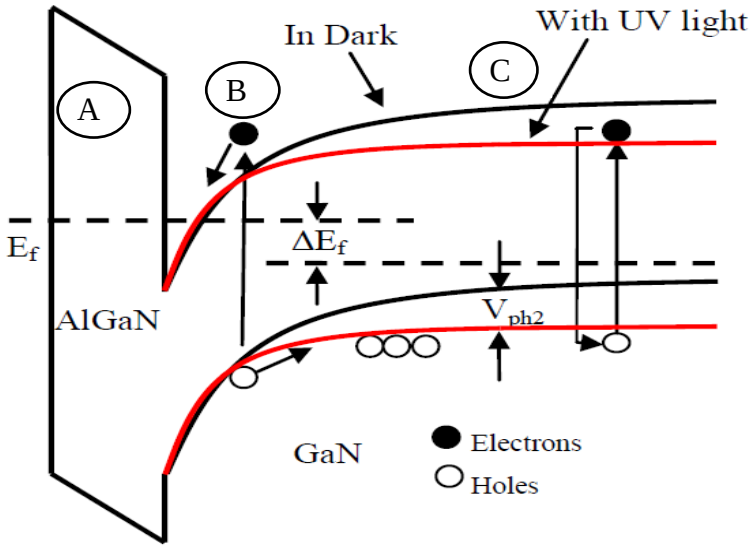


Figure 3.10 Band bending observed in GaN due to movement and accumulation of holes near the substrate.

This photo voltage forward bias the junction and tends to induce a band bending in the heterostucture as shown in the figure 3.10. This induced photo voltage causes a shift in the quasi Fermi level which is a direct consequence of the increase in carrier concentration under UV illumination. As the photo voltage builds up due to movement of holes towards the buffer/substrate interface, band bending increases and eventually encourages holes to recombine with the 2DEG electrons [24]. In other words, electrons would eventually spill out of the 2DEG channel under the influence of the band bending caused by the photo voltage effect to recombine with the photo generated holes. Therefore, current continuity is established under steady state illumination with the recombination current exactly balancing the primary photo generated current in region B, I_{ph2} as shown in figure 3.11. The photo voltage generated is that required to support I_{ph2} through the diode equation applied to the heterojunction.

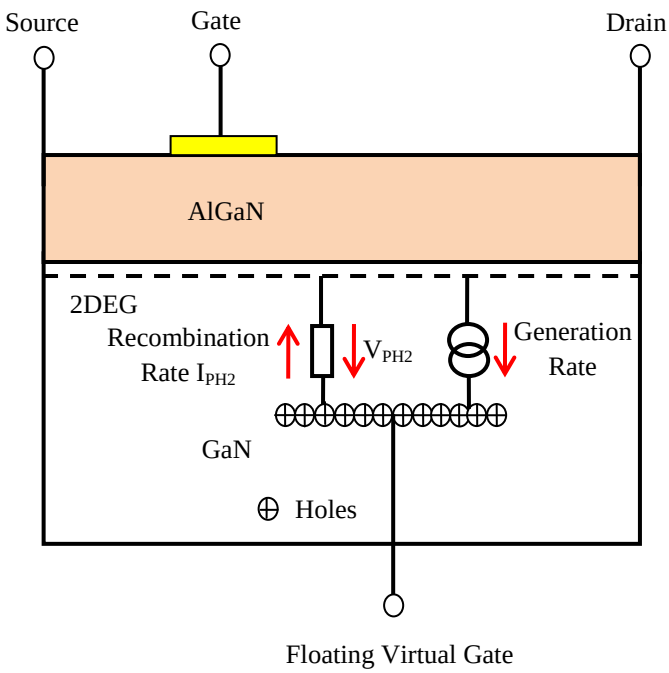


Figure 3.11 Equivalent circuit for UV absorption in the GaN buffer layer, illustrating the role of holes in producing a positive back gate bias.

The accumulated holes in GaN buffer region behaves as a positive back gate bias sustained by the photocurrent. Consequently, the 2DEG concentration increases as governed by the charge neutrality equation by moving more negatively charged electrons from the source contact. The holes basically behaves as floating virtual gate or positive back optical gate and

controls the concentration of electrons in the 2DEG channel. It is noteworthy that unlike the AlGaN, region A, these holes cannot escape other than by recombination.

3.4.2 Analysis for absorption in GaN buffer region

From standard open-circuit solar cell theory the photo voltage can be expressed as,

$$V_{ph2} = \frac{nkT}{q} \ln\left[\frac{I_{ph2}}{I_s} + 1\right] \qquad [3.12]$$

where, I_s is the reverse saturation current and n is the ideality factor (n~1 to 2) for the heterostructure junction, k is the Boltzmann constant, T the temperature in Kelvin and q is the electronic charge. The change in drain current, ΔI_{D2}, due to the photo voltage bias comes about through transistor action where,

$$\Delta I_{D2} = g_{m2} \times V_{ph2} \qquad [3.13]$$

where, g_{m2} is the appropriate transconductance for the back gate bias.

This photo voltage is superimposed on the gate bias and appears to change the effective gate bias to influence the carrier concentration. As expected from equation 3.13, it can be seen from figure 3.12 that the photo current follows a similar bell shaped curve to the transconductance as a function of gate bias and is shifted to positive direction compared to the g_m curve. This shift in photo current is due to the influence of the positive photo voltage which reduces the effective gate bias V_{gs}^* as,

$$V_{gs}^* = V_{gs} - V_{ph2} \qquad [3.14]$$

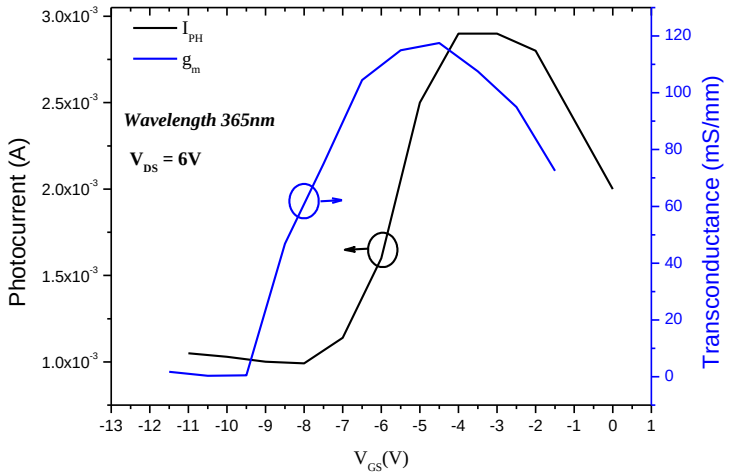


Figure 3.12 Photocurrent and transconductance as a function of gate bias.

Substituting for V_{ph2} from equation 3.13 gives,

$$\Delta I_{D2} = \frac{g_{m2} nkT}{q} \ln\left[\frac{I_{ph2}}{I_s} + 1\right] \qquad [3.15]$$

Assuming $\frac{I_{ph2}}{I_s} >> 1$, equation 3.15 predicts a logarithmic dependence of the photocurrent on input optical power, noting that the latter is proportional to I_{ph2}. This is different from the equivalent expression for absorption in the AlGaN barrier layer given by equation 3.9 which predicts a near linear dependence of photocurrent on UV intensity.

Figure 3.13, illustrates the experimental drain source photocurrent versus input power for 365 nm radiation (excites only the GaN buffer region) together with the fitted straight line expected from equation 3.15. An excellent straight line fit is obtained at intensities above 1 W/m^2, which illustrates the validity of the above arguments. For lower powers, the data points deviate from the straight line and this is thought to be due to the reduced and varying transconductance g_{m2}, (reflected in the slope) from the greater separation of the induced hole charge (back gate) at the GaN/substrate interface. At higher power, the depletion region will be narrow and fairly constant leading to a constant and larger effective transconductance. A similar response at 275nm radiation (excites both the AlGaN and GaN region) is also observed as shown in the inset in figure 3.13.

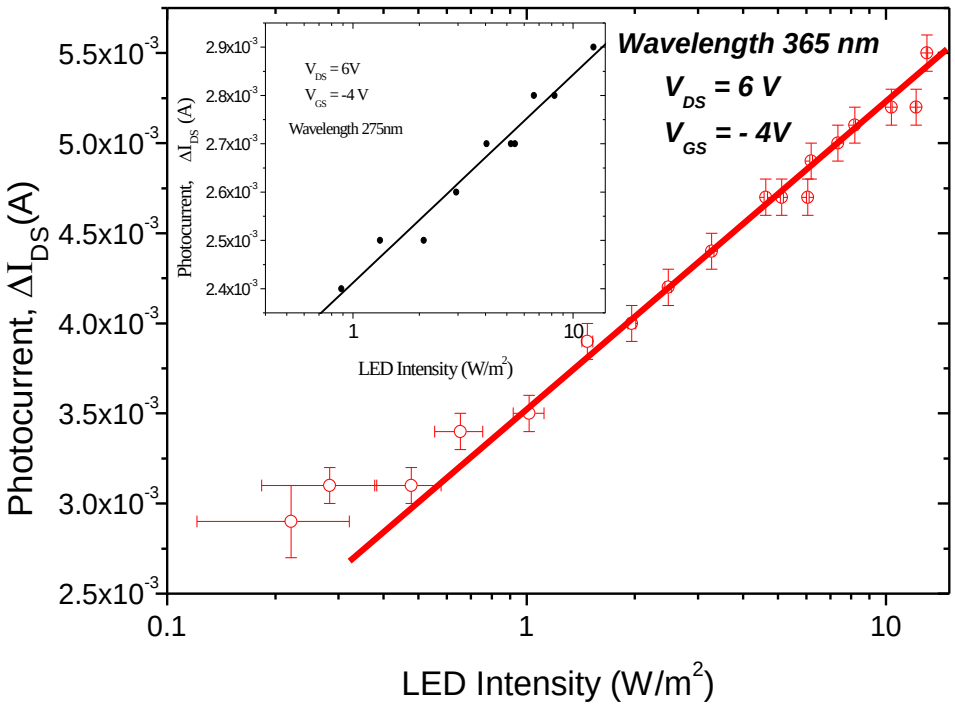


Figure 3.13 Measured photocurrent between drain and source versus 365nm UV light intensity. The solid line is a fit using equation 3.15. Inset shows response of 275nm LED.

By comparing the response of both LEDs at 8.2 W/m^2 intensity, around 82% higher photocurrent is obtained with 365nm radiation. However, considering the fact that around 32% less photons would be produced at shorter wavelength (275nm) suggests that nearly 50% more response is observed when only the GaN region is excited. A very useful figure of merit for a photo detector is responsivity, which relates electric current to incident optical power and is measured in terms of the photocurrent in the terminals of the device per unit incident optical power. Remembering that $\frac{I_{ph2}}{I_s}$>>1 in equation 3.15 and dividing both sides by I_{ph2} to get the responsivity,

$$\frac{\Delta I_{d2}}{B I_{ph2}} = \frac{g_{m2} nkT}{qB I_{ph2}} \ln [I_{ph2}] \qquad [3.16]$$

where, B is a constant which converts the primary photocurrent, I_{ph2}, into absorbed optical power. Figure 3.14 shows measured responsivity versus estimated power falling on the active area of the device on a ln-ln scale together with a line expected from equation 3.16. As expected, the data fits well with the theory. Physically, at low UV power the built-in field will extend throughout the highly resistive GaN buffer layer allowing efficient separation of the generated electron hole pairs. In this low power regime a large change in the photo voltage occurs for a small change in photo current as expected from the low current region of the diode I/V characteristic. As the power increases the photo current tends to saturate with an increase in recombination governed by the photo voltage effect, responsivity drops.

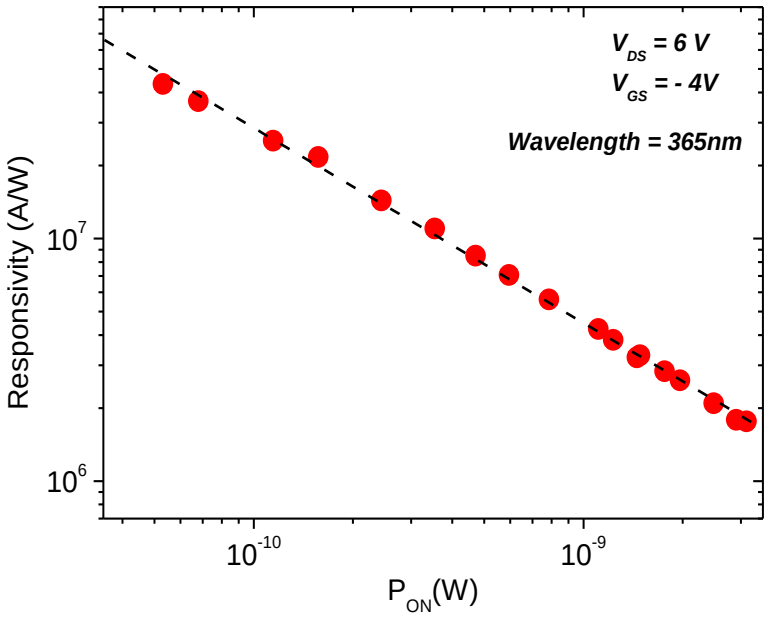


Figure 3.14 Measured responsivity calculated from drain source photocurrent as a function of the estimated optical power falling on the active area of the device. The broken line is from equation 3.16.

It should be noted that to get the measured responsivity of the HFET (maximum ~4.3×10^7A/W), the power falling on the device was estimated by comparing the device active area with the larger total UV beam area. The total beam power was measured using a calibrated Si photo diode. Although the limit of the LED power available was reached, two further data points were obtained using a higher power laser at 244nm, which indicated that the responsivity followed a similar trend at higher power levels (10^{-6} W) as shown in figure 3.15.

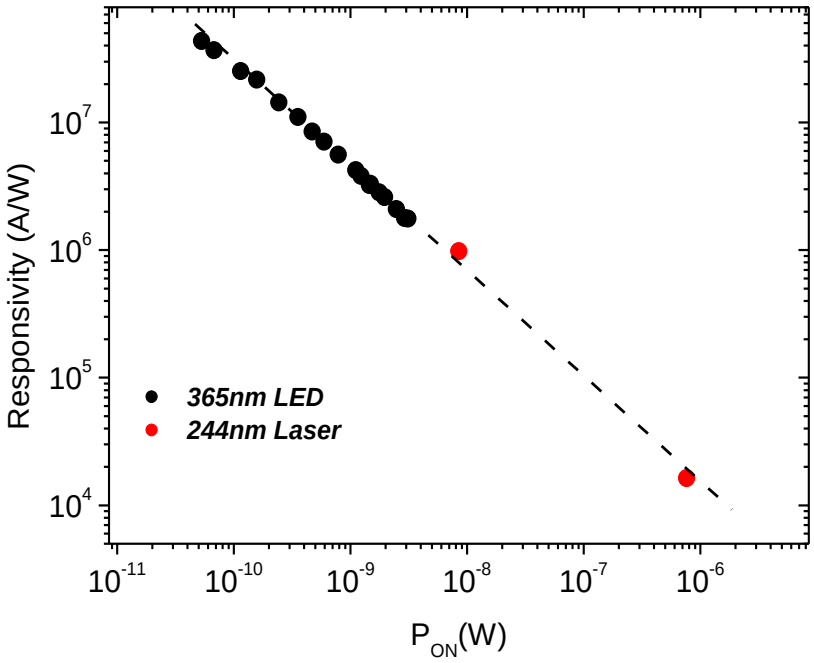


Figure 3.15 Measured responsivity of the device with additional data points from high power laser.

The data presented in figures 3.13 and 3.14 shows a highly non-linear photo response and responsivity to input optical power which is a characteristic of the photo voltage effect described above. Similar results were obtained when using 275 nm LED light which excites photo carriers in both barrier and buffer regions of the device. The dependence on photocurrent observed with the latter is highly nonlinear even though we expect significant powers to be absorbed in both regions. The weaker dependence on power expected from equation 3.7 and increased gate leakage indicates that the gain observed in AlGaN barrier is very weak compared to the absorption in the GaN buffer layer.

In order to compare the mechanisms in the two absorption regions more carefully, a UV monochromator with a Xenon lamp source was used to scan the device at wavelengths from 200nm to 400nm which covers the band gap energies for both the AlGaN and GaN regions. The power for each wavelength was kept the same in order to avoid the strong gain dependence on input optical power. Figure 3.16, shows the resultant photo current response as a function of excitation wavelength. A sharp transition is observed near the GaN cutoff wavelength, 365nm, but interestingly no distinct change was observed at the AlGaN cutoff wavelength (~ 320 nm). The response when only the GaN region is excited is expected to dominate as indicated by the previous data shown in figure 3.13, but no significant difference in photocurrent was observed over the range of wavelengths. It is unclear why no transition was observed near the AlGaN cutoff wavelength (~ 320nm) but a possible explanation for this can be the fact that the UV monochromator radiation intensity at these wavelenghts is very low and the response with longer wavelengths is only around 2mA which is below the lower non-linear region (see figure 3.13) compared to the magnitude of response abtained with the 365nm LED data in figure 3.13. It may be possible that some additional mechanism is happening at low intensity which is masking the expected overall photoresponse.

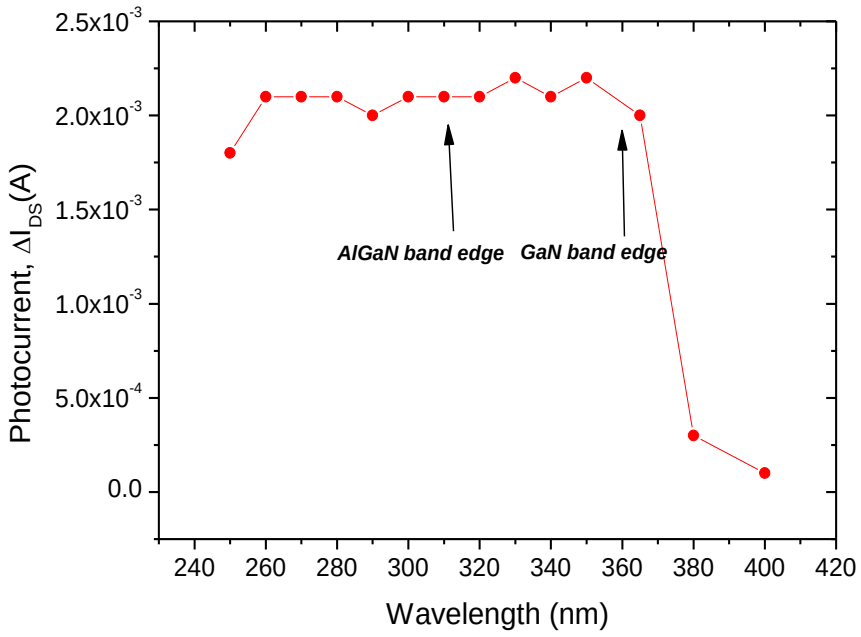


Figure 3.16 Photocurrent between drain and source of a device against the wavelength.

Another important figure of merit for photodiodes is detectivity, which evaluates the sensitivity of a photodiode. For the HFET, calculated value of detectivity is 1.58×10^{14} cm.$\frac{\sqrt{Hz}}{W}$ at the highest responsivity (~10^7 A/W).

3.4.3 Effect of Temperature on Photo voltage

Consider the expression for the photo voltage effect in equation 3.12 which is given as,

$$V_{ph2} = \frac{nkT}{q} ln \left[\frac{I_{ph2}}{I_s}\right] = \frac{nkT}{q} \left[ln\left(I_{ph2} - I_s\right)\right] \quad [3.17]$$

Using the saturation current (I_s) expression for a pn junction,

$$V_{ph2} = \frac{nkT}{q}[ln\,(I_{ph2}) - ln(BT^3\, exp(-\frac{Ego}{kT})] \quad [3.18]$$

Where, B is a temperature independent constant and E_{go} is the bandgap at absolute zero temperature [21].

Assuming I_{ph2} and B are independent of temperature and taking the derivative of equation 3.18 with respect to temperature,

$$\frac{dV_{ph2}}{dT} = \frac{V_{ph2}}{T} - \frac{3nk}{q} - \frac{nEgo}{qT} = \frac{-\left(\frac{nEgo}{q} - V_{ph2} + \frac{3nkT}{q}\right)}{T} \quad [3.19]$$

The term nE_{go}/q represents a voltage equivalent to the bandgap energy. nE_{go}/q is always bigger than V_{ph2} since the latter cannot exceed the band bending with no light as shown in figure 3.12.

Equation 3.19 predicts a negative dependence of photo voltage on temperature, [21] this causes a corresponding drop in photo current with an increase in temperature. In addition considering equation 3.13 which relates the photo current with the transconductance of the device, g_{m2} is also temperature dependent and reduces as the temperature increases, therefore adding to the overall effect.

In order to observe the temperature effect on HFETs, the photo response was measured both at room temperature and at 140^0 C. The results are shown in figure 3.17. A considerable reduction in photo current is observed at high temperature due to the reduction in induced photo voltage.

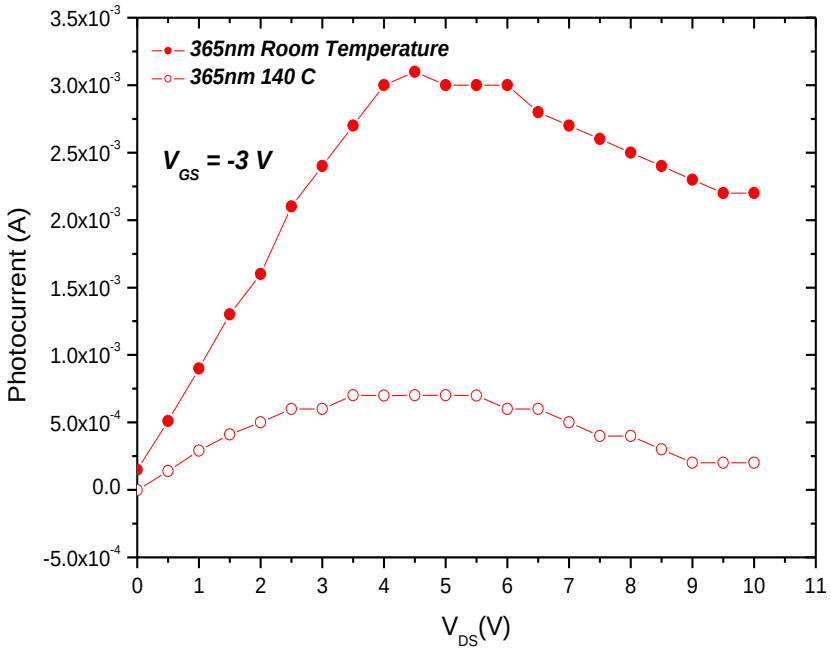


Figure 3.17 Photocurrent between drain and source of a device measured at room temperature and 140^0 C.

3.4.4 Effect of Silicon Nitride Passivation

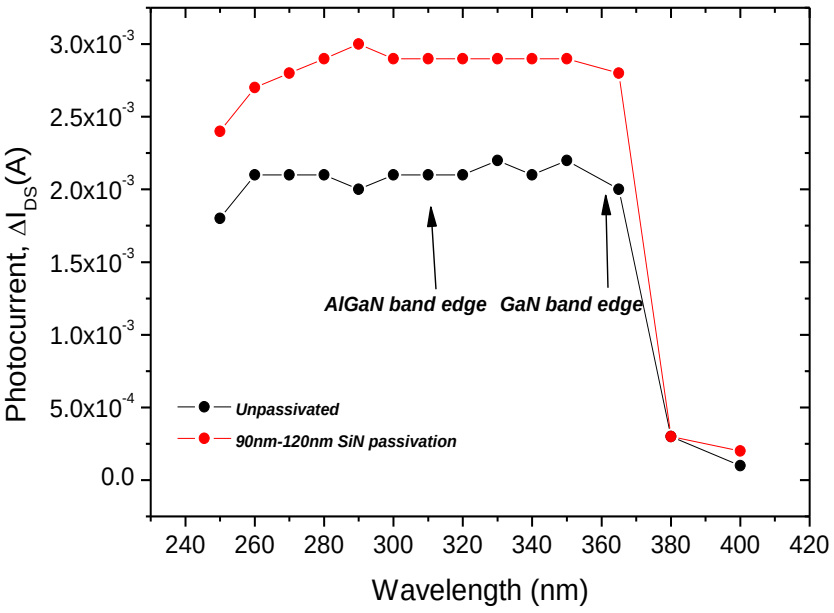


Figure 3.18 Photocurrent between drain and source of a passivated and unpassivated device against the wavelength.

In AlGaN/GaN HFETs SiN_x passivation is normally carried out to bury any surface states and hence to reduce current collapse [31]. However, SiN_x is widely used in photodiodes and solar cells as an efficient anti-reflective coating [32]. The advantage of using anti reflective coating is well documented in photo diodes [33]. It suppresses surface reflection of light thereby increasing absorption and improving overall efficiency. After ~90-120nm (this range is due to the variation in deposition rate of our PECVD tool) of SiN_x passivation, a slight increase in photocurrent was observed as shown in figure 3.18, this is thought to be due to an anti-reflection effect from the SiN_x . The calculated antireflective coating thickness multiple at 270nm wavelength is ~ 100nm and for 350nm is 129nm which is close to the deposited SiN_x thickness.

3.5 Conclusion

The UV absorption mechanism in AlGaN/GaN HFET is explained in both the barrier (AlGaN) and the buffer (GaN) layers. The optical gain in these devices is due to the generation of photo voltages between the surface and the channel and the buffer/substrate interface and the channel, depending on light absorption regions. Through transistor action of the device, 2DEG channel concentration changes as positive virtual gates are formed. Gate leakage along the surface influence the hole lifetime when carriers are generated in the barrier layer. However, in the GaN buffer region holes cannot escape other than by recombination. Consequently the gain of the GaN buffer region dominates the barrier layer, owing to both it being a thicker region and enhanced hole lifetimes. In comparison to other GaN based UV detectors, the AlGaN/GaN HFET is ultra sensitive to UV illumination. A very high responsivity (~10^7A/W) at very low power levels (~10^{-10} W) is demonstrated. HFET based UV detectors can be easily integrated with transistors on the same wafer. Although the dark current with the HFET geometry is quite high due to the presence of a highly conductive 2DEG channel, understanding the gain mechanisms can help optimise the design of future UV photo detectors.

3.6 References

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Chapter No: 4 GaN HFETs on Si Substrate

4.1 Introduction

In this Chapter, AlGaN/GaN HFETs grown on Si substrates are characterised. To reduce buffer leakage both iron (Fe) and carbon (C)-doped structures are considered. The GaN to substrate vertical leakage transport mechanism is identified based on Poole Frenkel emission process in both Fe and C-doped structures. A novel method to reduce gate leakage current in GaN HFETs is established by using chemical treatments. Combining the sulphuric acid treatment with SiN_x passivation can offer both reduce leakage current and current collapse.

In recent times, AlGaN/GaN HFETs grown on Si substrates have attracted significant attention due to numerous reasons including high growth quality, matured Si substrate processing techniques, better thermal stability, lower manufacturing cost and much larger wafer size scalability of Si substrates reaching up to 200mm (diameter size) [1-2]. In addition to keeping the raw material cost down for devices, Si substrates offer industries the opportunity to employ the same manufacturing tools currently used for back end processing of Si based electronics, therefore essentially making it a Si compatible manufacturing process. However, the growth of GaN on Si substrate is fraught with difficulties arising from the large lattice (17%) and thermal expansion (56%) constant mismatch between the two materials. As a consequence of these mismatches, the growth of GaN on Si results in a high dislocation density (typically > 10^{10} cm^{-2}), wafer bowing and crack formation arising from biaxial tensile stress in GaN/Si interface [3]. Therefore, without adopting growth optimization techniques, device performance would be severely degraded in GaN on Si substrates.

In order to overcome these difficulties various research groups have demonstrated Metal Organic Chemical Vapour Deposition (MOCVD) of GaN on Si using different buffer and intermediate layers for stress control. H. Marchand et-al [4] demonstrated the growth of GaN on Si (111) using a thick AlN nucleation layer and AlN-to-GaN graded buffer layers to achieve well defined device pinch-off characteristics. Later on, Arulkumaran et-al [5] demonstrated enhancement in the breakdown voltage by employing different thickness of AlN (8, 200, 300, and 500 nm) buffer layers and by eliminating the active defects at GaN/AlN/Si interface. In their structure, growth of AlN nucleation layer on the Si substrate was followed by a thick GaN/AlN super lattice structure (SLS). The use of step graded or

continuously graded AlGaN buffer layers is also reported to be effective in reducing stress [6]. It is believed that AlGaN layers with small lattice constant results in creation of compressive stress which counteracts the tensile stress created upon cooling the top GaN layer [7]. In this work, GaN on Si (111) structures were grown by combination of multiple AlN nucleation layer and graded AlGaN buffer layers. The wafers used in this study were grown at University of Cambridge.

4.2 Characterization of AlGaN/GaN HFETs

The Transmission Line Measurement (TLM) and IV characteristics of AlGaN/GaN HFET fabricated on Si substrate are shown in figure 4.1(a) and (b) respectively. The contact resistance extracted from TLM is around 0.8 ohm.mm and sheet resistance is ~450 ohm/sq.

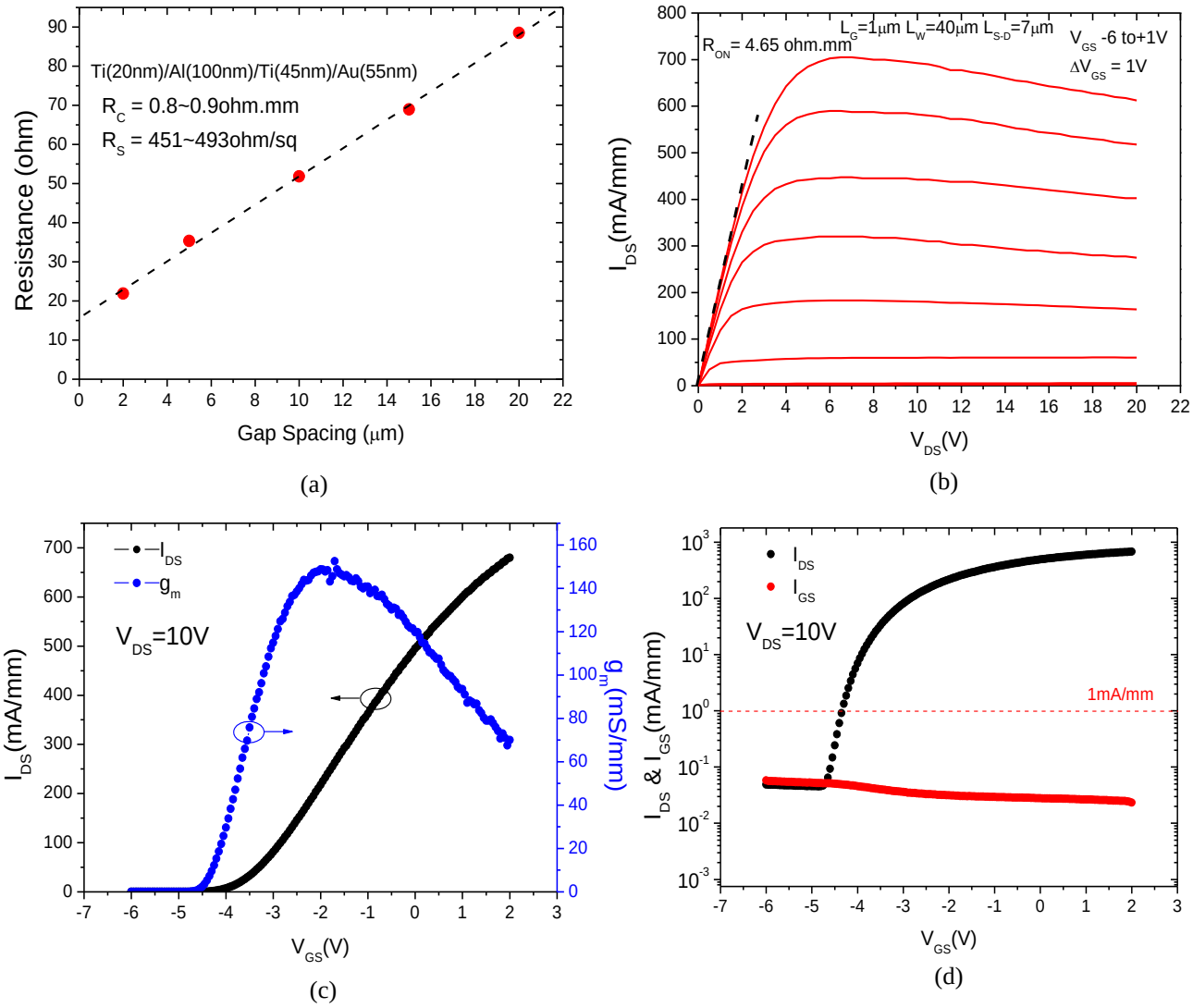


Figure 4.1 (a) TLM characteristics (b) IV characteristics (c) Gate transfer characteristics and (d) Pinch-off leakage currents of AlGaN/GaN HFET on Si Substrate.(The growth layer structure is similar to figure 4.7 except no Fe doping is performed in graded AlGaN region).

The gate transfer and pinch-off characteristics are also shown in figure 4.1(c) and (d) respectively. The peak drain current is around 700mA/mm at +2 V_{GS}, pinch-off voltage is ~ -4V, on resistance is 4.65m.ohms.mm and peak transconductance is ~150mS/mm. The pinch-off gate leakage current is 1.5 orders below 1mA/mm. The latter is considered a standard level for the device breakdown (generally leakage current three orders less than the "on" current level is considered acceptable). To extract the 2DEG carrier concentration and AlGaN barrier layer thickness, capacitance voltage (CV) measurements were performed and the results are shown in figure 4.2. The barrier layer is 30nm thick and the 2DEG concentration is 7.5×10^{12} cm^{-2} measured at 10 kHz.

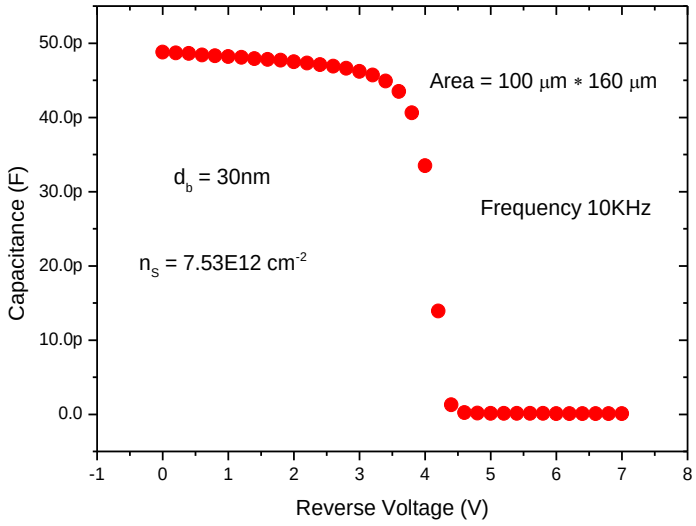


Figure 4.2 CV measurement performed on FATFET to extract 2DEG concentration and barrier thickness.

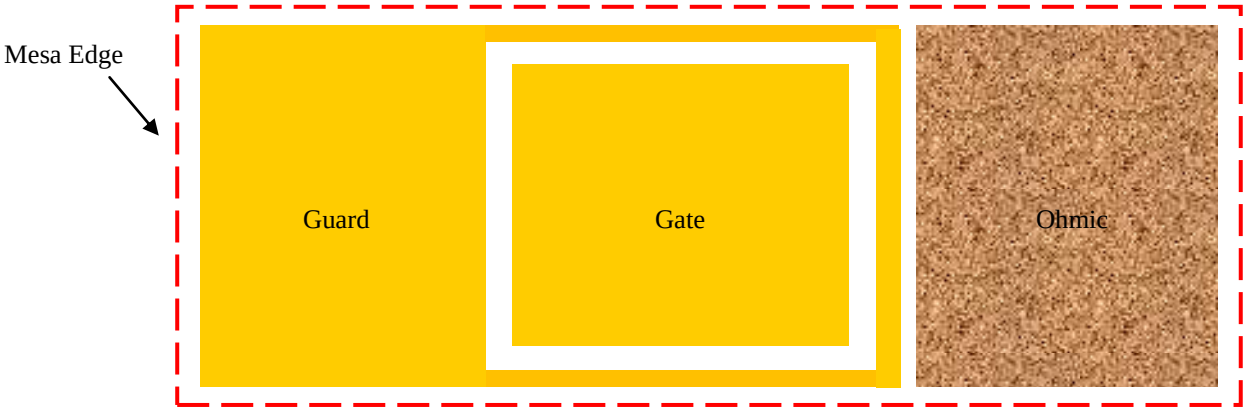
From clover leaf Hall measurements, carrier concentration and mobility were also extracted and a table summarizing the electrical properties of AlGaN/GaN HFET on Si substrate is shown in table 4.1

WAFER ID	CONTACT RESISTANCE R_C(Ohm.mm)	SHEET RESISTANCE R_S(Ohm/sq)	$V_{pinchoff}$ (V)	Peak I_{DS} @0V_{GS} (mA/mm)	CV n_s (10Khz) (cm^{-2})	CV d_b (nm) K=10.2	Hall R_{Sh} (ohm)	Hall n_S (cm^{-2})	Hall Mobility ($cm^2V^{-1}s^{-1}$)
CS073	0.8~0.9	450~493	-3.3~-4.5	420-600	7.53E+12	30±0.5nm	521	6.75E+12	1773

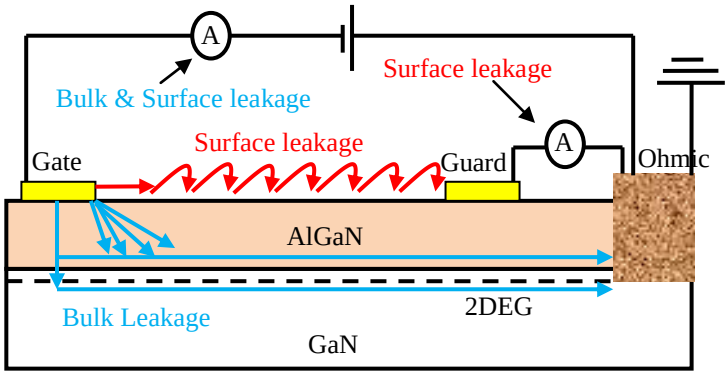
Table 4.1: Electrical properties of wafers CS073 (AlGaN/GaN on Si).

4.3 Surface Leakage Structure

A useful device geometry to study gate surface leakage in AlGaN/GaN HFETs is the surface leakage test structure shown in figure 4.3(a) which was first demonstrated by Tan et al [8]. The surface leakage structure consists of two Schottky contacts and one ohmic contact, which makes the connection with the 2DEG channel. One Schottky contact is the gate terminal which is reverse biased with respect to the ohmic contact and the other Schottky contact is the guard terminal which encloses the gate contact and is held at zero bias with respect to the ohmic contact as shown in the circuit configuration in figure 4.3(b).



(a)



(b)

Figure 4.3 (a) Surface leakage structure top view (b) Surface leakage structure circuit configuration, showing surface and bulk components.

The surface leakage structure separates the gate current into two components, namely surface and bulk leakages. Under the appropriate bias arrangements, any current flowing between the

ohmic and the gate terminal is denoted as the bulk component since it flows via the 2DEG channel or the AlGaN barrier region [8] and any current flow along the surface between the gate and ohmic contacts would be intercepted by the guard terminal and is termed as the surface leakage current. The typical output characteristic of the surface leakage test structure is shown in figure 4.4. The bulk leakage component is generally a few orders higher than the surface leakage and tends to saturate after the device pinch-off voltage (-4V) whereas the surface leakage current generally has a strong bias dependence and increases with the applied electric field.

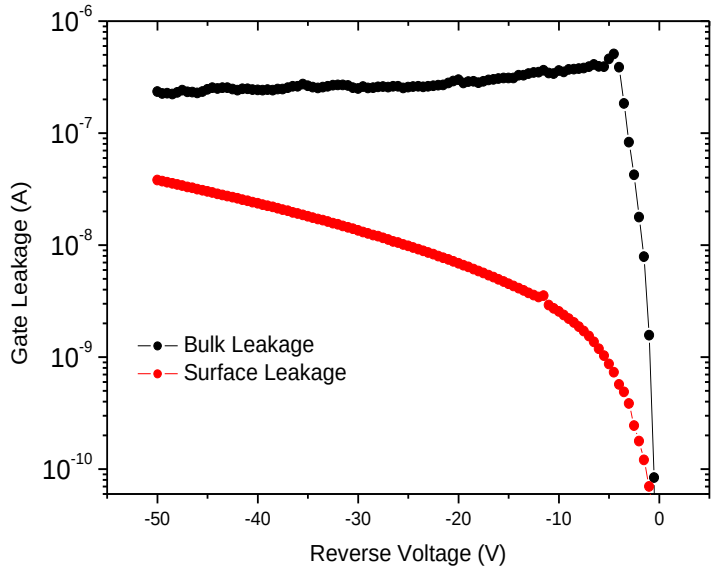


Figure 4.4 Typical output characteristics of surface leakage test structure.

4.4 Fe and C doped buffer in AlGaN/GaN HFETs

As mentioned before, in AlGaN/GaN HFETs used for high voltage operations the peak electric field near the gate edge (towards drain side) needs to be controlled by using combination of multiple field plates and optimized surface passivation techniques [9]. However, for the device to further sustain a large electric field, the creation of a highly insulating GaN buffer region is very important for both high voltage power electronics applications (sustaining high blocking voltage capability) and RF applications (to eliminate the short channel effects such as “punch through” in the buffer or “drain induced barrier lowering”) [10-11]. Therefore, in order to convert unintentionally n-doped GaN buffer to highly resistive or insulating, deep acceptor states are often introduced by doping with impurities such as iron (Fe) [12] or carbon (C) [13-14]. These dopants create different types

of acceptor centres (Fe 0.7eV below the conduction band and C 0.9eV above the valence band) [15]. C doping has proved to be more advantageous for achieving higher breakdown voltage and better trade-off between the breakdown and current collapse phenomena associated with buffer charge trapping. Additionally, unlike Fe, doping with C can be abruptly turned-off at a controllable distance from the AlGaN/GaN (2DEG channel) interface [16].

4.4.1 Buffer leakage and vertical leakage structures

In this work, both Fe and C doped wafers were characterized and, in order to measure the buffer conductivity, a buffer test structure is used and the circuit configuration is shown in figure 4.5. The buffer leakage test structure gives the buffer leakage between two isolated ohmic contacts (isolation is achieved by low RF power dry ICP etching) and a guard ring is also used to subtract any surface conduction component from the total leakage.

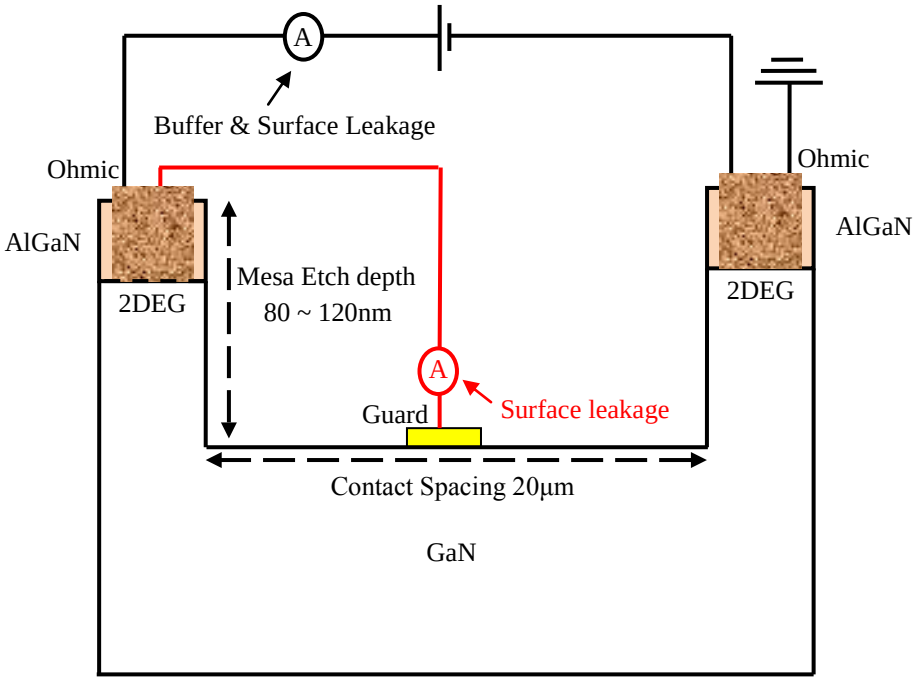


Figure 4.5 Test structure and circuit configuration for measuring buffer leakage in AlGaN/GaN HFET.

In contrast to AlGaN/GaN HFETs grown on insulating sapphire, conducting p-type Si (111) substrates allow electrical back contact probing. In this work, 100nm Al metal (un-annealed) is evaporated on the Si substrate to make a back contact. A vertical test structure is used to

measure the breakdown voltage of the GaN buffer and the subsequent layers grown on Si (111) substrate as shown in figure 4.6.

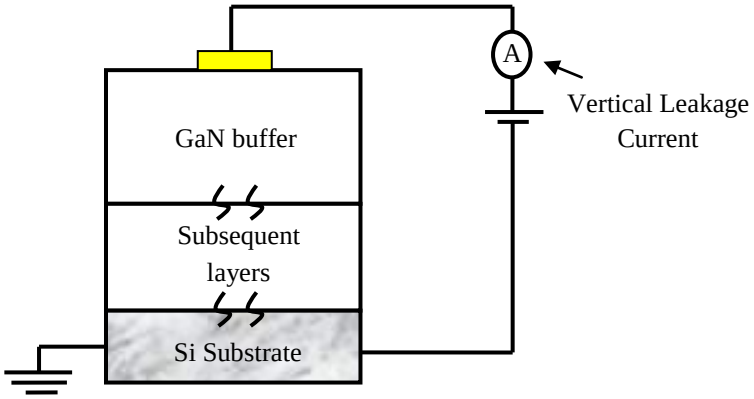


Figure 4.6 Test structure and circuit configuration for measuring vertical leakage in AlGaN/GaN HFET.

4.4.2 Fe doped AlGaN/GaN HFETs

The growth structure of the AlGaN/GaN HFET on Si substrate with Fe doped graded AlGaN buffer region is shown in figure 4.7. The doping level of Fe in AlGaN extracted from the Secondary Ions Mass Spectroscopy (SIMs) performed at Loughborough is 8×10^{18} cm^{-3} and Fe doping is turned off at the end of AlGaN layer to avoid its influence on the 2DEG channel transport properties. Despite that, some residual Fe could still be present in the 1.3µm GaN buffer region.

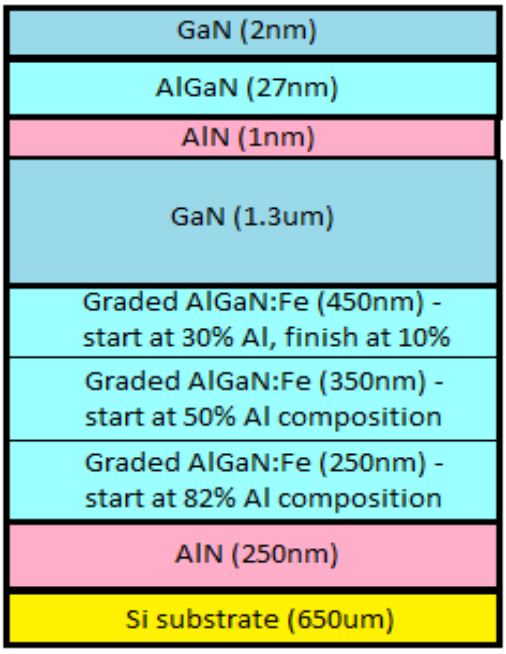
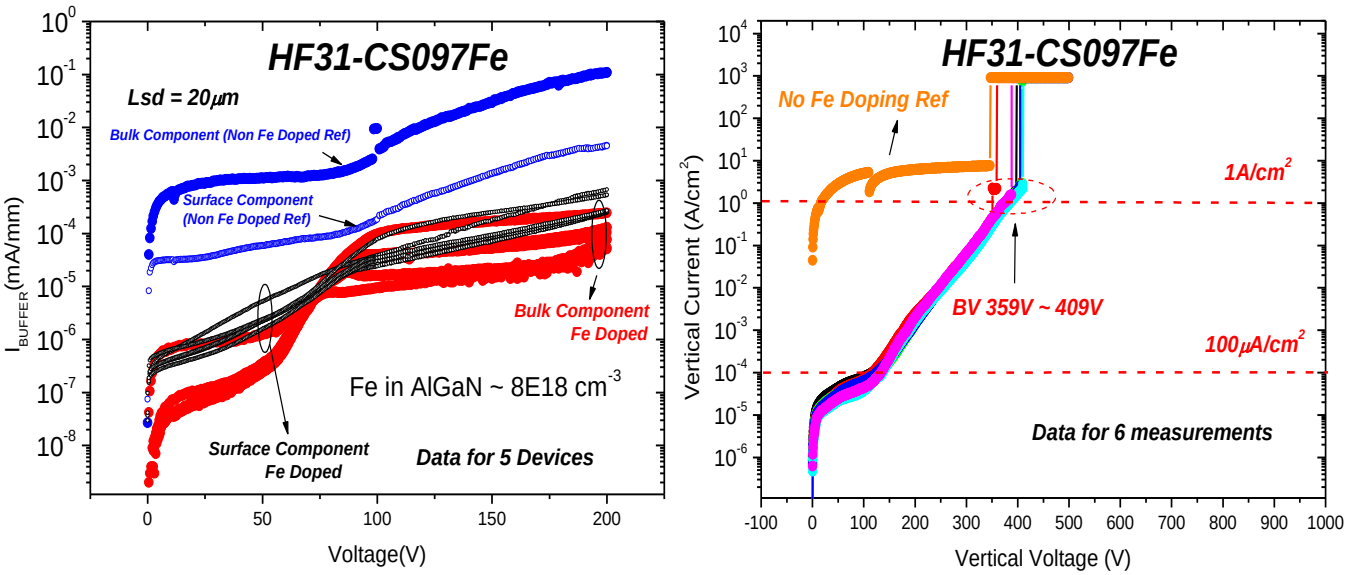


Figure 4.7 Growth structure of Fe-doped AlGaN/GaN HFET on Si substrate.

The comparison of lateral buffer conduction of the Fe doped wafer with an unintentionally n-doped wafer is shown in figure 4.8(a). It can be seen that Fe doping results in nearly three orders of magnitude suppression (measured at 200V) in buffer leakage.



(a) (b)

Figure 4.8 (a) Buffer leakage (b) Vertical leakage and breakdown voltage in Fe doped AlGaN/GaN HFET on Si substrate.

The vertical breakdown voltage (GaN to substrate) is also increased compared to un-doped structure from 10s of volts to nearly 400 volts (defined at 1A/cm^2 threshold level, standard criteria for breakdown in literature) as shown in figure 4.8(b). The breakdown electric field of the Fe doped structure is ~ 1.58 MV/cm.

4.4.3 C doped AlGaN/GaN HFETs

The growth structure for the C doped AlGaN/GaN HFET is shown in figure 4.9. In contrast to Fe doped wafers, the C doped buffer region can afford to be much closer to the 2DEG channel due to its better doping controllability. The vertical breakdown voltage of the C doped wafer is around 580V as shown in figure 4.10. The breakdown electric field is ~2 MV/cm which is greater than the Fe doped wafer (1.58 MV/cm). The buffer leakage current with different levels of carbon doping is shown in figure 4.11. Again the overall buffer leakage level is much lower than Fe doped wafers and a very weak or almost no dependence with change in the C concentrations is observed. These results suggest that compared to Fe, C doped HFET is much more effective in achieving highly insulating buffers.

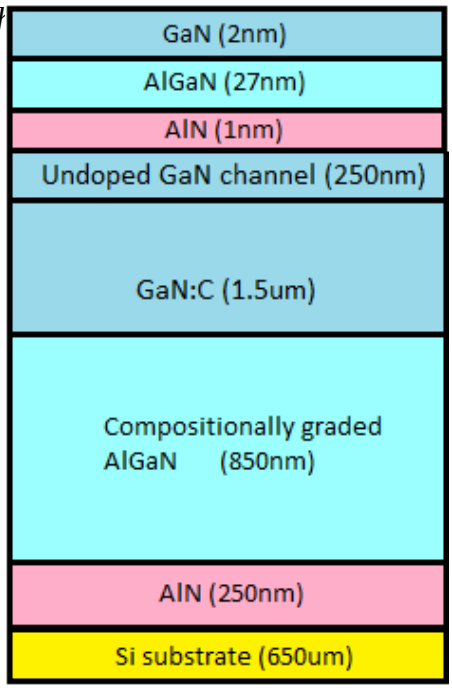


Figure 4.9 Growth structure of C-doped AlGaN/GaN HFET on Si substrate.

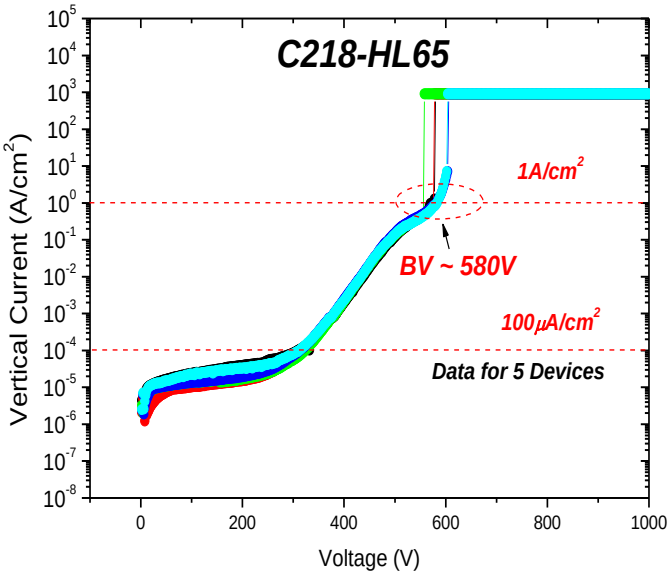
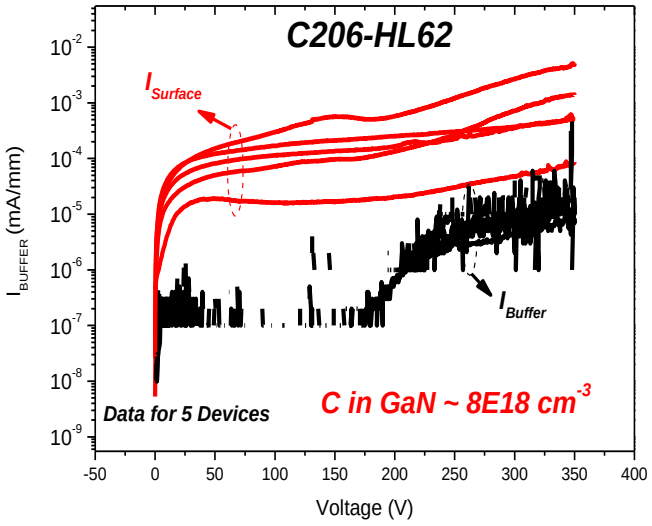
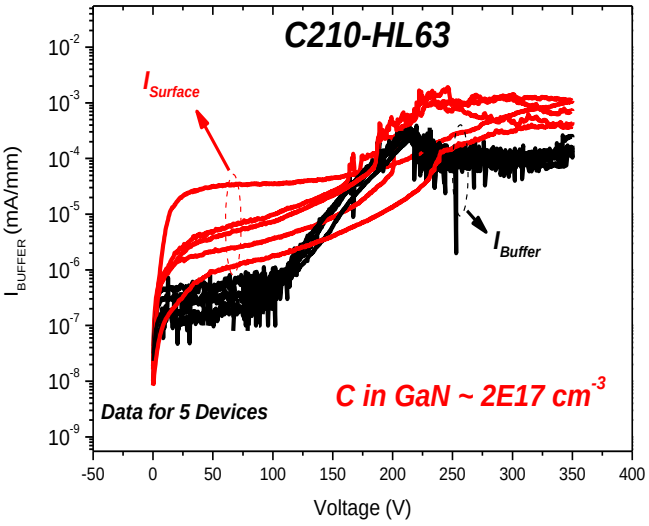


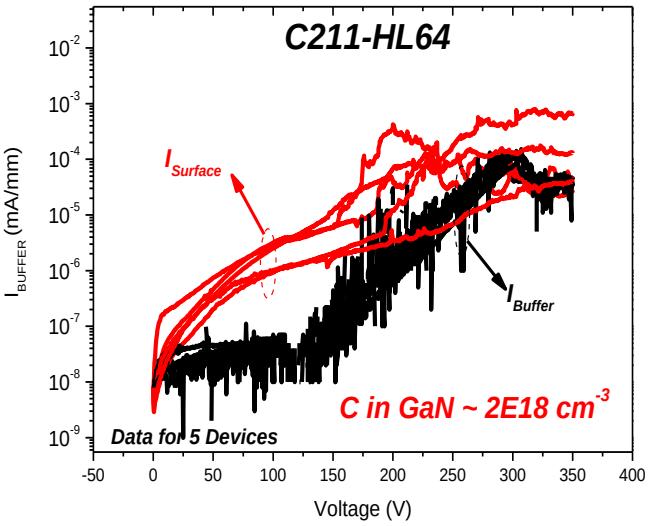
Figure 4.10 Vertical leakage and breakdown voltage in C-doped AlGaN/GaN HFET on Si substrate.



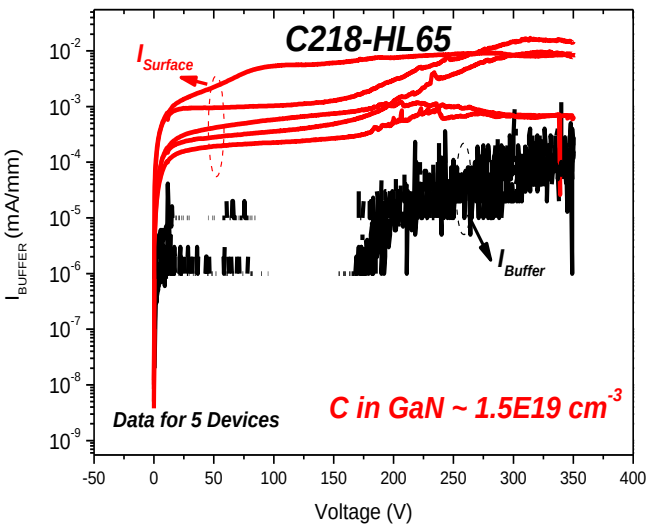
(a)



(b)



(c)



(d)

Figure 4.11 Buffer leakages in C doped AlGaN/GaN HFET with different C concentrations (a) 8 × 18 cm^{-3} (b) 2 × 17 cm^{-3} (c) 2 × 18 cm^{-3} and (d) 1.5 × 19 cm^{-3}

A summary of some wafer characteristics and electrical properties is shown in table 4.2.

WAFER ID	CONTACT RESISTANCE R_C(Ohm.mm)	SHEET RESISTANCE R_S(Ohm/sq)	$V_{pinchoff}$ (V)	Peak I_{DS} @0V_{GS} (mA/mm)	CV n_s (10Khz) (cm^{-2})	CV d_b (nm) K=10.2	Hall R_{Sh} (ohm)	Hall n_S (cm^{-2})	Hall Mobility ($cm^2V^{-1}s^{-1}$)	Vertical Breakdown Voltage (V) @1A/cm^2	Buffer Leakage (mA/mm)
Fe097	0.8±0.1	484±50	-3.8~4.7	480-640	7.68E12	30±1	608	6.97E+12	1472	380-400	10^{-4} @200V
Fe105	0.8±0.1	501±50	-4~4.5	420-560	6.82E12	31±1	502	6.05E+12	1554	400-450	10^{-5}-10^{-4} @200V
Fe109	0.9±0.1	535±50	-3.8~4.1	380-550	6.80E12	32±1	544	6.28E+12	1624	450-480	10^{-4}-10^{-3} @200V
C206	0.9±0.1	427±50	-4-4.7	478-594	7.46E12	31±1	533	6.58E+12	1775	400-430	10^{-5} @350V
C210	0.7±0.1	424±50	-3.9-4.4	500-567	6.81E12	31±1	543	6.50E+12	1765	570	10^{-4} @350V
C211	0.7±0.1	446±50	-3.7-4.2	516-570	6.76E12	31±1	490	6.85E+12	1855	550-570	10^{-5}-10^{-4} @350V
C218	0.8±0.1	413±50	-3.9-4.8	437-567	7.67E12	32±1	512	6.89E+12	1767	580	10^{-5}-10^{-4} @350V
C418	0.8±0.1	418±60	-3.8-4.2	550-580	9.7E+12	28±1	362	9.3E+12	1848	590	10^{-5} to 10^{-4} @350V

n.b Fe and C in the wafer ID are the reference for iron and carbon doping respectively. The growth layer structures are similar to figure 4.7 and 4.9 for Fe and C doping respectively.

Table 4.2: Electrical properties of Fe and C doped wafers (AlGaN/GaN on Si).

Experimentally, it is found that the three terminal off-state breakdown voltage of both C and Fe doped HFETs with a 3µm gate-drain spacing and no field plates is always dominated by the gate breakdown rather than buffer/substrate breakdown and breakdown voltage ranges from 120-200V.

4.4 Vertical Leakage Transport Mechanism in C and Fe-doped AlGaN/GaN HFETs on Si

In AlGaN/GaN HFETs fabricated on conductive p-type Si (111) substrate, the ultimate breakdown voltage is often limited by the vertical breakdown (top to bottom) between the drain contact and the Si substrate (conductive p-type Si (111), the substrate is normally grounded in device operation due to system requirements) [17]. In order to understand the physical mechanism responsible for the vertical leakage current transport in C and Fe-doped AlGaN/GaN HFETs we did temperature dependent I-V measurements on vertical leakage test structure and Arrhenius plots with different voltages for the C-doped buffer is shown in figure 4.12.

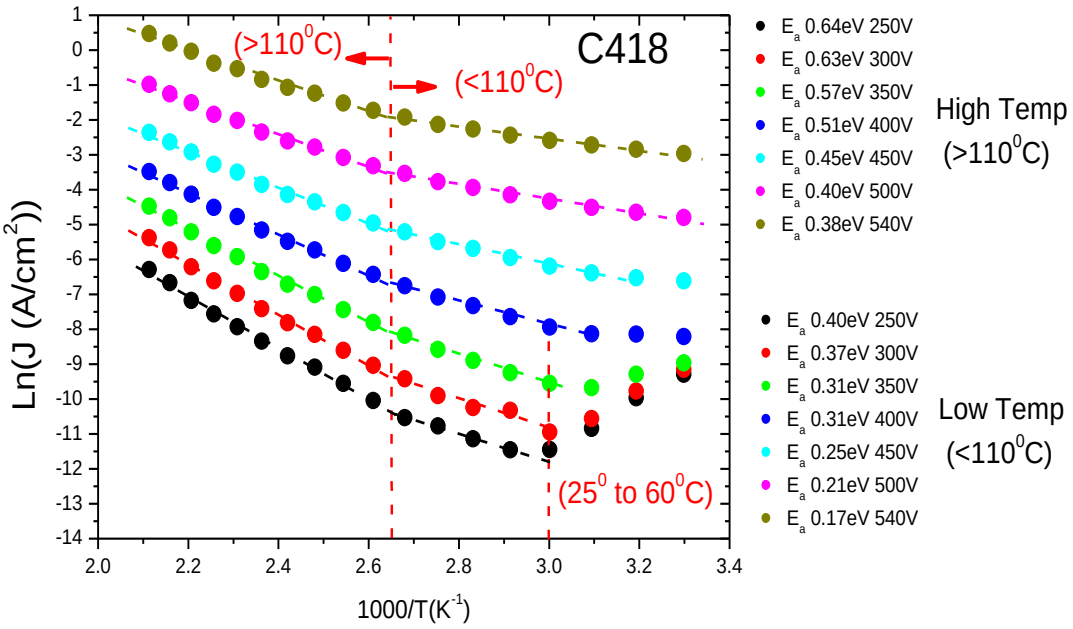


Figure 4.12 Arrhenius plot of vertical leakage in C-doped AlGaN/GaN HFET fabricated on Si Substrate

Due to the difference in slopes, the temperature axis is divided into two main regions namely high temperature (>110^{0}C) and low temperature region (<110^{0}C). An excellent straight line fit can be extended into both temperature regions indicating a thermally activated process and activation energies at different voltage bias are shown on the right hand side of figure 4.12. However, at low temperatures (<70^{0}C) and particularly low voltage bias (<400V) a negative temperature dependence of leakage current is observed. This mechanism can be explained by the fact that during the initial low voltage and temperature sweeps electrons are quickly captured by the traps spreading over the range of energy levels in GaN buffer and graded

AlGaN layers. Now, as the temperature is increased, more and more electrons are captured into the traps and become stuck resulting in a reduction of further electron flow as negative space charge builds up which counters the applied electric field. As the voltage and temperature increase further, trapped electrons gain sufficient energy to emit from the traps and leakage mechanism with positive temperature dependence is observed.

To understand the detailed leakage mechanism, a Poole Frenkel based emission model is considered. The Poole Frenkel model involves thermal excitation of electrons from the traps into the conduction band and under the influence of an electric field, Coulomb potential energy of the electrons is effectively reduced which increases the probability of electrons to emit from the trap state [18-19]. The Poole Frenkel emission for electrons and holes from the traps into the conduction and valence band respectively is shown in figure 4.13.

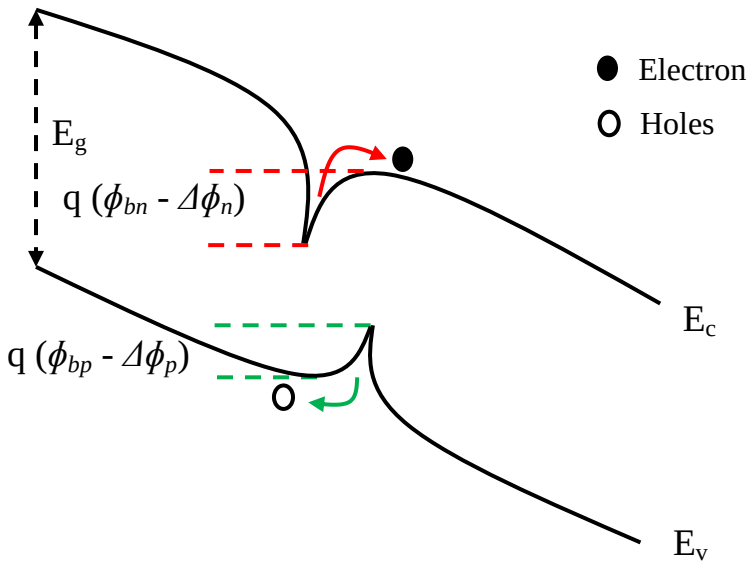


Figure 4.13 Sketch of Poole Frenkel emission from traps for electrons and holes into the conduction and valence band respectively.

where ϕ_{bn} and ϕ_{bp} are the trap depth of electrons and holes respectively. Application of an electric field will lower the barrier heights by $\Delta\phi_n$ for electrons and $\Delta\phi_p$ for holes.

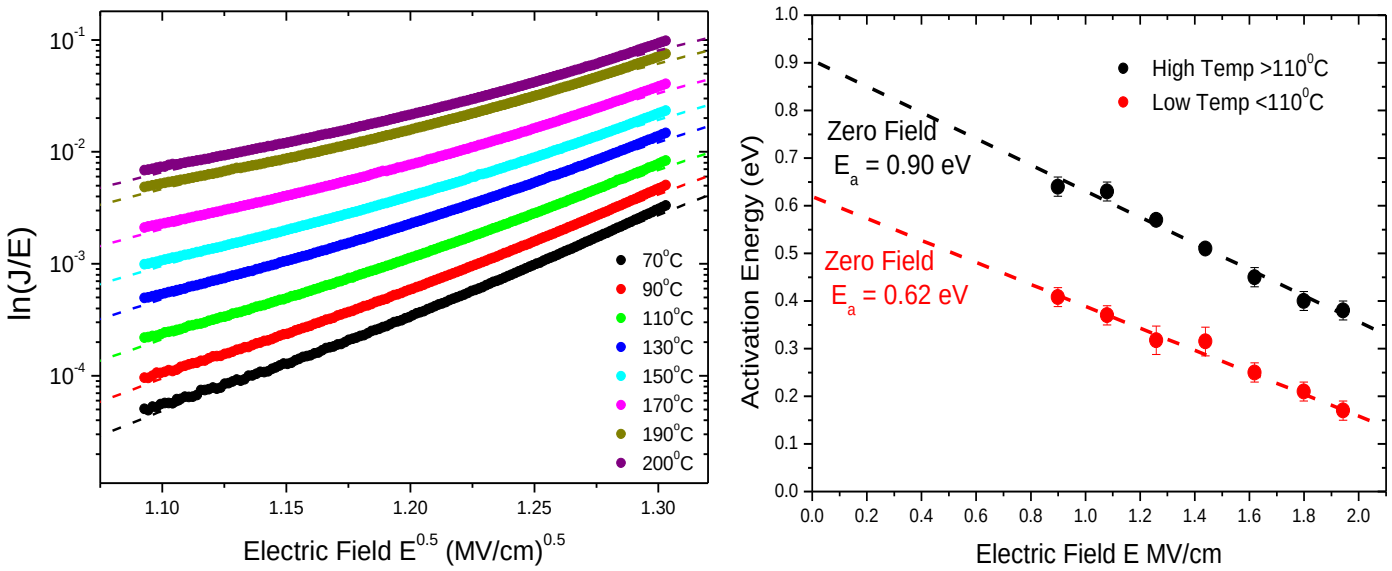
The functional reliance of the emission rate on the applied field and the temperature allows unambiguous recognition of the Poole Frenkel emission process and, as shown in figure 4.12, the activation energy in both the high and low temperature regions is systematically reduced

with the applied voltage. The mathematical expression for the Poole Frenkel mechanism is given by [20],

$$\frac{J}{E} = exp\left[\frac{-q\left(\phi_{b} - \sqrt{\frac{qE}{\pi\varepsilon}}\right)}{K_B T}\right] \qquad [4.1]$$

where J is the current density, E is the electric field, ϕ_b is the barrier height for emission from the trap state, q is the electron charge, ε is the permittivity of the semiconductor, k_B is the Boltzmann constant and T is the absolute temperature.

From this equation a plot of ln(J/E) versus square root of electric field should be a straight line if the leakage mechanism is due to Poole Frenkel emission. To verify this, ln(J/E) is plotted against the square root of applied electric field in figure 4.14(a) and a straight line fit is obtained. A uniform electric field distribution is assumed across all the buffer layers. In order to find the trap depth in the absence of any applied electric field, the activation energy is plotted against the electric field and the straight line fit is extrapolated to zero electric field as shown in figure 4.14(b).

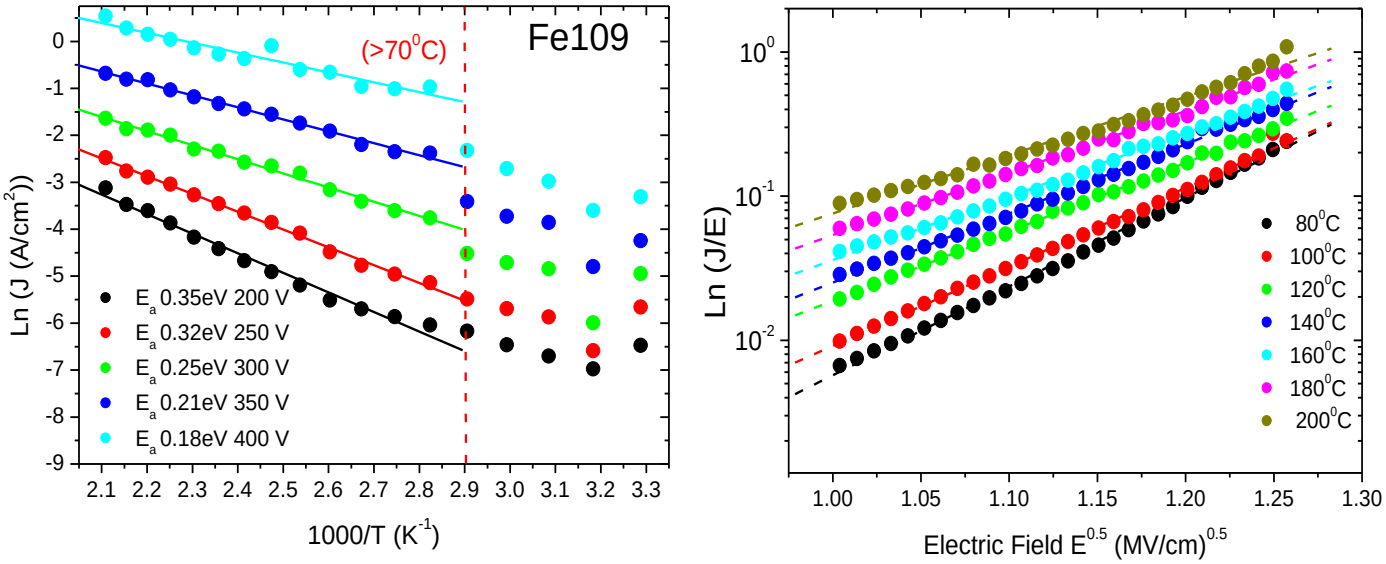


(a) (b)

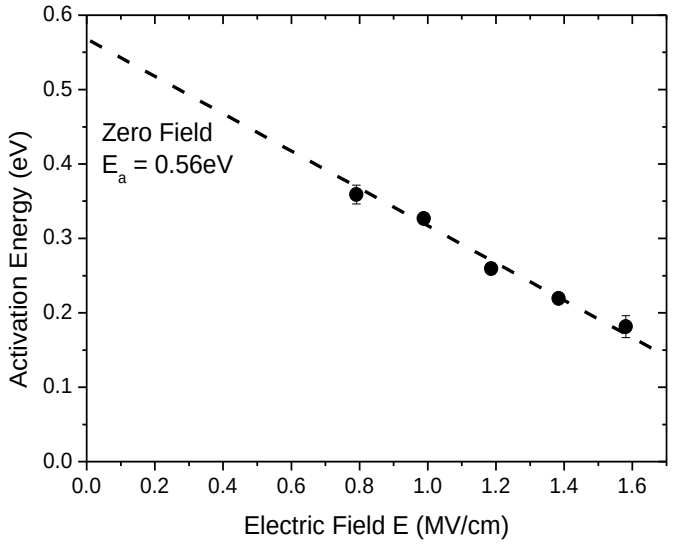
Figure 4.14 (a) Plot of Log (J/E) versus square root of electric field (b) Plot of activation energy against electric field to extract zero field activation energy.

In the high temperature region, an activation energy of 0.9eV is obtained which is consistent with the C acceptor level above the valence band and, in the low temperature region, a slightly lower trap depth of 0.62eV is obtained. The trap depth of 0.9eV (corresponding to C level) obtained in our experimental results could possibly be due to hole conduction in the valence band since a similar level of 0.86eV was reported previously by M.Uren et-al on C doped buffers by using a time dependent conductivity measurement [21]. The 0.62eV trap depth may be due to other defects such as threading edge dislocations in the GaN and graded AlGaN buffer layers.

A similar experiment was performed on the Fe-doped wafer for comparison and the results are shown in figures 4.15(a), (b) and (c).



(a) (b)



(c)

Figure 4.15 (a) Arrhenius plot of vertical leakage in Fe-doped AlGaN/GaN HFET fabricated on Si Substrate (b) Plot of Log (J/E) versus square root of electric field (c) Plot of activation energy against electric field to extract zero field activation energy.

A similar temperature assisted leakage process is obtained in the Fe-doped wafer and Poole Frenkel mechanism fits data well as shown in the figures 4.15(a), (b) and (c). However, in contrast to the C-doped wafer, a negative temperature dependence is observed to a much lesser extent in the lower temperature regime. The extracted activation energy is also lower and only a single activation energy of 0.56eV is obtained above 70^0C. The 0.56eV is close enough to the Fe acceptor level of 0.7eV below the conduction band and could be due to conduction of electrons in the conduction band. In conclusion, these results indicate a Poole Frenkel emission process is responsible for vertical current leakage mechanism in both Fe and C-doped wafers with different trap energies.

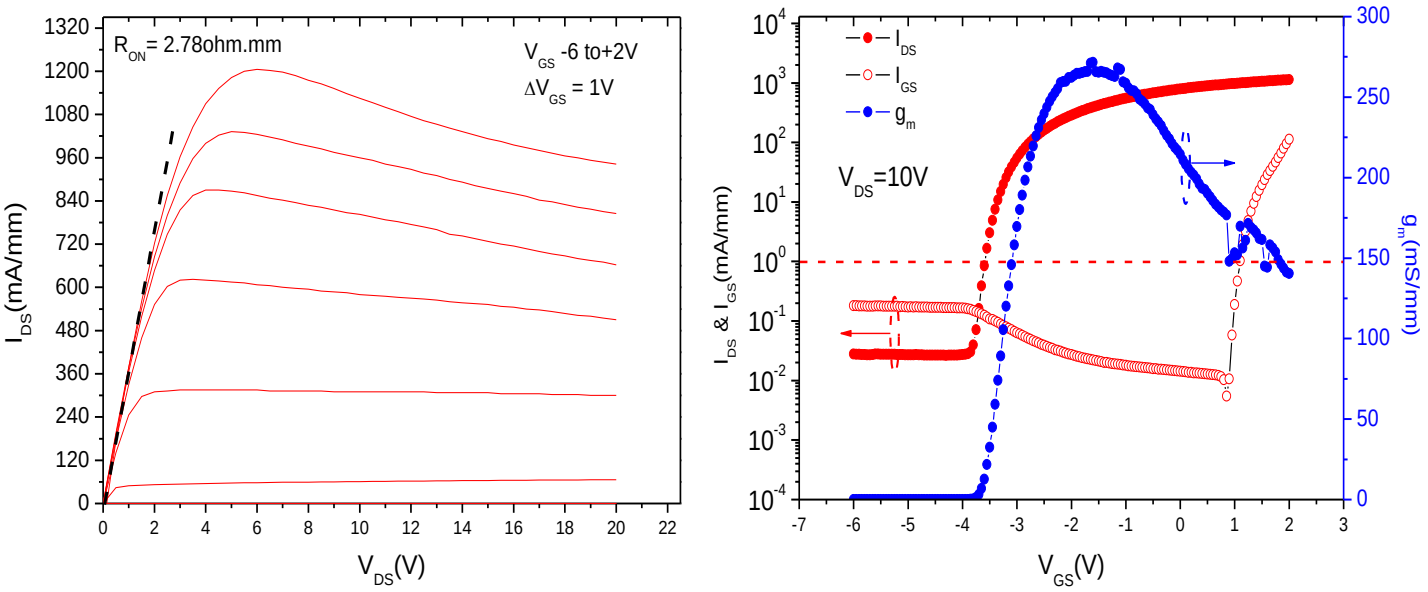
4.5 Characterization of AlInN/GaN HFETs

Lattice matched AlInN/GaN HFETs are competing with conventional AlGaN/GaN HFETs for RF, microwave frequency and high power amplifier applications [22-23]. One of the advantages of AlInN based HFETs is the growth of stress free lattice matched structures which can improve device reliability by reducing mechanical strain and dislocations in the structure. Additionally, high spontaneous polarization charge present in AlInN HFETs favors high 2DEG density and the thin AlInN barrier (11-13nm) offers high transconductance [24]. A brief summary of the electrical characteristics of the AlInN/GaN HFET is shown in table 4.3.

WAFER ID	CONTACT RESISTANCE R_C(Ohm.mm)	SHEET RESISTANCE R_S(Ohm/sq)	$V_{pinchoff}$ (V)	Peak I_{DS} @+2V_{GS} (mA/mm)	CV n_s (10Khz) (cm^{-2})	CV d_b (nm) K=10.2	Hall R_{Sh} (ohm)	Hall n_s (cm^{-2})	Hall Mobility ($cm^2V^{-1}s^{-1}$)
C316	0.4±0.1	240±20	-3--4	1000-1200	No pinch off (poor phase angle)	13±1	276	1.3E+13	1717

Table 4.3: Electrical properties of AlInN/GaN HFET grown on Si substrate.

The IV and gate transfer characteristics of the AlInN/GaN HFET are shown in figure 4.16(a) and (b) respectively. As expected from the high 2DEG density, the peak drain current is high (1200mA/mm) and R_{ON} is low (2.78ohm.mm). The presence of thin AlInN barrier (13nm) also results in much higher peak transconductance value of 275mS/mm compared to standard AlGaN/GaN devices.



(a) (b)

Figure 4.16 (a) The IV characteristics of AlInN/GaN HFET on Si Substrate (b) Gate transfer characteristics showing I_{DS} and I_{GS} on left hand side and g_m on right hand side.

4.6 Effect of Surface Chemical treatment (Sulphuric Acid and Hydrogen Peroxide) on AlGaN/GaN HFET

As discussed in chapter 1, due to the presence of a large number of surface states, AlGaN/GaN HFETs devices generally suffer from DC to RF dispersion, otherwise known as current collapse [25-27]. This effect can severely limit the HFET switching performance in power electronics applications. Additionally, for practical power applications at high operating voltages it is very important to reduce the gate leakage current in the blocking state. Device breakdown is often reported due to the large gate surface leakage current via surface states, supported by the presence of high electric field between the (positive bias) drain and gate contacts.

There have been several successful demonstrations of the suppression of surface related current collapse by depositing different dielectric layers such as SiN_x, SiO_2, AlN, HfO_2 and Al_2O_3 [28-32]. SiN_x deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) is generally effective and widely used as a passivation technique and also serves to support field plates for high voltage operation modulating peak electric field profile [33] but the surface leakage can be dependent on the prior chemical state of the surface and the details of the deposition conditions. It is observed that SiN_x is not always effective in reducing the surface

leakage current and inconsistency is observed in this work across wafers grown by different vendors and under different deposition conditions. In the past, hydrogen peroxide (H_2O_2) treatment on the AlGaN surface was shown [34] to reduce the gate leakage current by forming a thin oxide layer but no detailed studies on surface leakage mechanisms were conducted.

In this work, we have compared SiN_x passivation, hydrogen peroxide (H_2O_2) and sulphuric acid (H_2SO_4) treatment on GaN/AlGaN/GaN surfaces both after full device fabrication (post-gate metal deposition) and underneath the gate region (pre-gate metal deposition). The chemical treatments of post-processed devices were carried out by exposure to H_2O_2 (30% concentrated) or H_2SO_4 (98% concentrated) solutions for ~48 hours at room temperature. We initially performed H_2SO_4 treatment for ~6 hours and observed no significant change in gate leakage which suggests that it is a very slow process. We then did H_2SO_4 treatment for ~48 hours and observed significant reduction in gate leakage. Although we did not do a systematic study of the effect of treatment time and temperature, but large treatment time was thought to be due to the relative stability of the oxides of the GaN cap used in this work. The H_2SO_4 treatment was also performed pre-gate metal deposition. PECVD was used to deposit the 100nm SiN_x passivation layers. For consistency, the same devices were measured before and after the treatment.

The gate transfer characteristics of AlGaN/GaN HFET devices before and after 100nm PECVD SiN_x post-gate metal passivation, H_2O_2 and H_2SO_4 post-gate metal treatment and H_2SO_4 pre-gate metal treatment are shown in figure 4.17. Compared with SiN_x passivation, both chemical treatments resulted in much greater suppression of gate leakage current (<1μA/mm), an improved Sub-threshold Slope (S.S.) and higher on/off current ratios (~10^7). Although the untreated devices showed a range of gate leakage currents, over the devices studied in this work, H_2SO_4 treatment was found to be the most effective in suppressing the gate leakage current and improving the S.S.. Compared to other treatments, a noticeable reduction in peak drain current (from 647.5 to 427.5 mA/mm at V_{GS} = +2V) is observed in the H_2SO_4 treated device together with a larger positive shift in threshold voltage. These results suggest that H_2SO_4 treatment oxidizes the surface and, in the process, consumes some of the barrier layer (AlGaN) which in turn reduces the 2DEG charge. The formation of an oxide layer on the surface has a strong passivating effect and reduces the overall gate leakage current. The H_2SO_4 is a strong oxidizing agent but it is unclear whether H_2SO_4 is simply functioning by oxidizing the surface to reduce gate leakage since Sulfur has also been

reported to be used as a passivation method in III-V nitrides [35]. In order to extract the interface trap charge density (D_{it}) from the S.S. we performed H_2SO_4 pre-gate metal treatment as shown in figure 4.17(d) and an almost identical suppression in gate leakage is observed compared to treatment after the gate deposition. It is not possible to compare the same device in this case since H_2SO_4 treatment is performed pre-gate metal and variations in the electrical characteristics from device to device made it difficult to directly compare with and without treatment. However, the S.S. is reduced for a typical untreated device from 215 mV/decade to 90 mV/decade after the H_2SO_4 treatment.

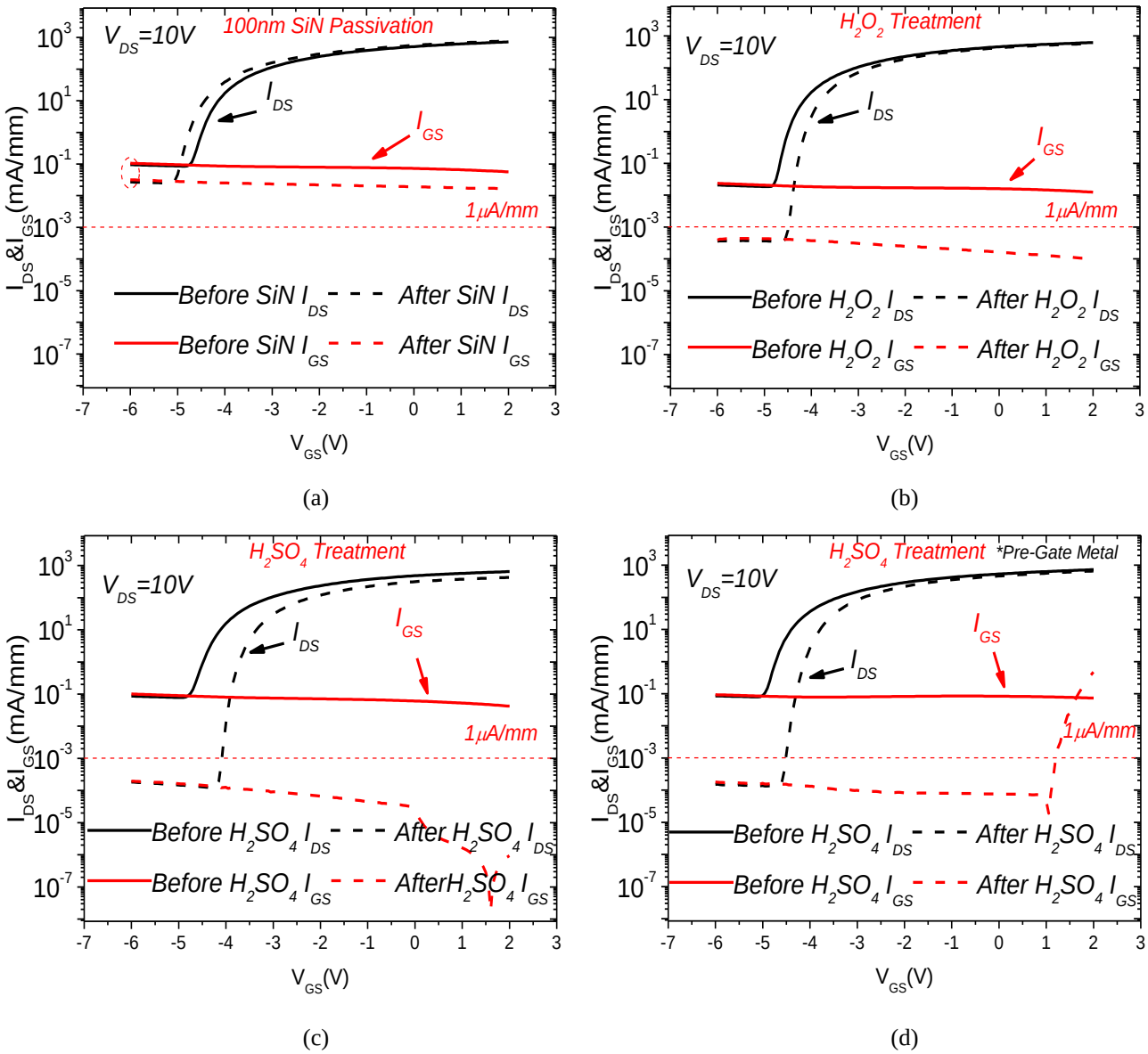


Figure 4.17 Gate transfer characteristics of AlGaN/GaN HFETs before and after (a) 100nm SiN post-gate metal passivation (b) H_2O_2 post-gate metal treatment (c) H_2SO_4 post-gate metal treatment and (d) H_2SO_4 pre-gate metal treatment.

The reduction in S.S. comes from the reduced gate leakage current which previously dominated the pinch-off leakages. In the past, a strong linear dependence of S.S. on reduced gate leakage current has been reported [36]. The low S.S. characteristics (60mV/decade ideal) are very important for reduced pinch-off leakages, increased gate modulation efficiency, reduced power dissipation and higher power added efficiency and reliability in power amplifiers [37].

The S.S. is also related to the interface trap charge density (D_{it}) existing between the metal and semiconductor by the expression given as [38],

$$D_{it} = \left(\frac{S.S.}{\ln(10)} \times \frac{q}{kT} - 1\right)\frac{C}{q^2} \qquad [4.2]$$

where q is the electron charge, k is the Boltzmann constant, T is the temperature in Kelvin and C is the gate capacitance per unit area. The measured equivalent reduction in D_{it} due to the reduction in S.S. after H_2SO_4 treatment is from 4.9 to 0.9 × 10^{12} $cm^{-2}eV^{-1}$.

In order to measure the gate surface and bulk leakage (through the channel) components independently, the surface leakage test structure incorporating a guard ring is used [8] as shown previously in figure 4.3(a) and the results before and after the chemical treatments are shown in figure 4.18.

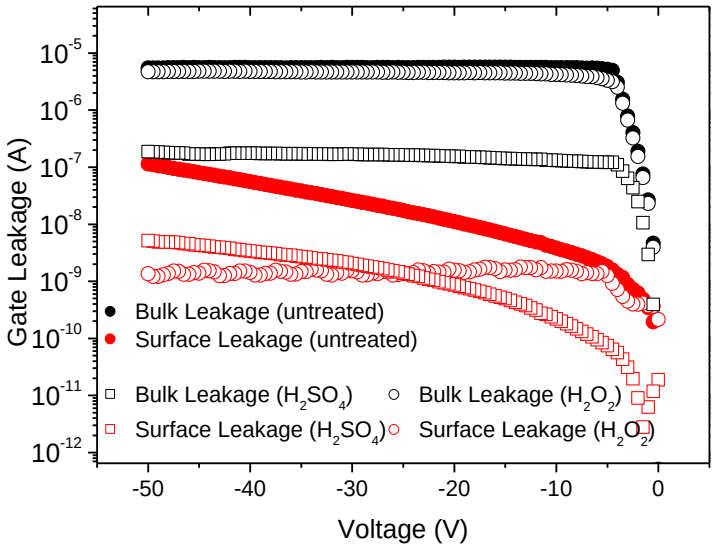
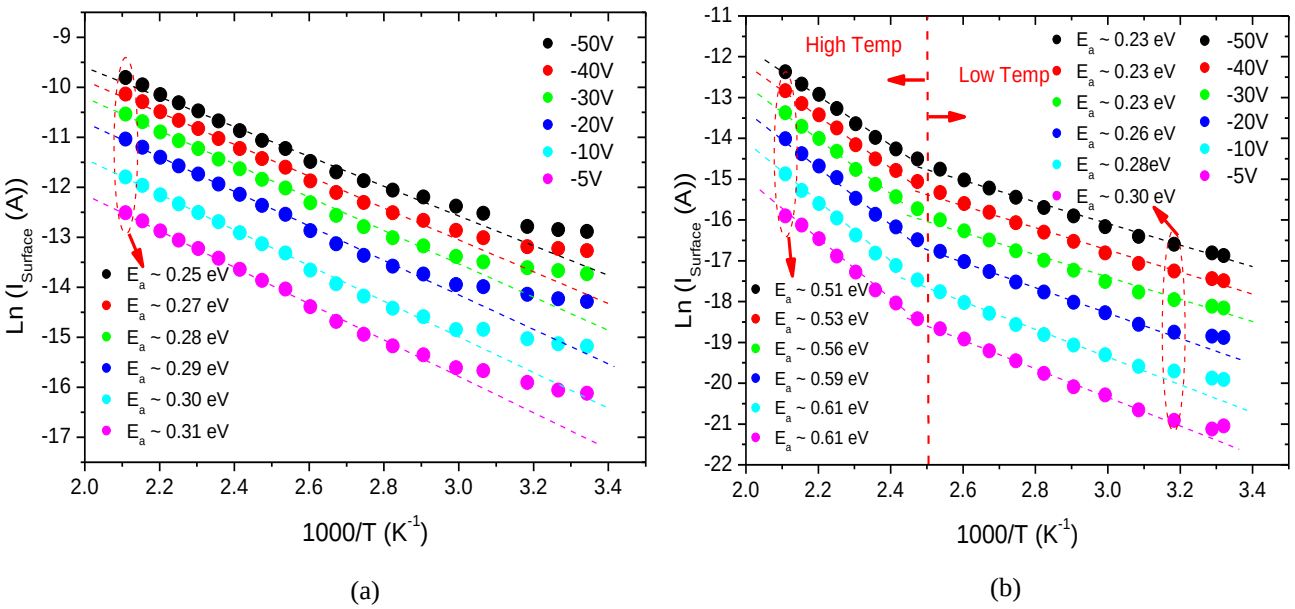


Figure 4.18 Leakage currents measured from surface leakage test structure after both H_2O_2 and H_2SO_4 chemical treatments.

It can be seen that compared to untreated devices, both H_2SO_4 and H_2O_2 treatments are effective in suppressing the gate surface leakage component as expected (variations of around 0.5~1 orders was observed in untreated, H_2O_2 treated and H_2SO_4 treated surface leakage current measured across different devices and samples studied in this work). However, H_2SO_4 treatment also suppressed the gate bulk leakage component by a few orders of magnitude as shown in figure 4.18. The suppression in gate bulk leakage is consistently observed with H_2SO_4 treatment across various devices and samples. These results suggest that surface oxidization by H_2SO_4 treatment influences the overall gate bulk leakage through modification of the gate edge electron injection where the electric field is highest. The reduction in 2DEG charge will also reduce the peak electric field near the gate edge.

4.6.1 Mechanism of Surface Leakage

We selected the H_2SO_4 treated devices for further detailed study of the gate surface leakage mechanism and compared it with the untreated device. The Arrhenius plots are shown in figure 4.19(a) and (b) with activation energies extracted from the gate surface leakage at different voltage bias for untreated and H_2SO_4 treated devices respectively. For identification purposes, we have split the inverse temperature axis into two regions in the H_2SO_4 treated device (low <130^{0}C and high >130^{0}C temperature).



(a) (b)

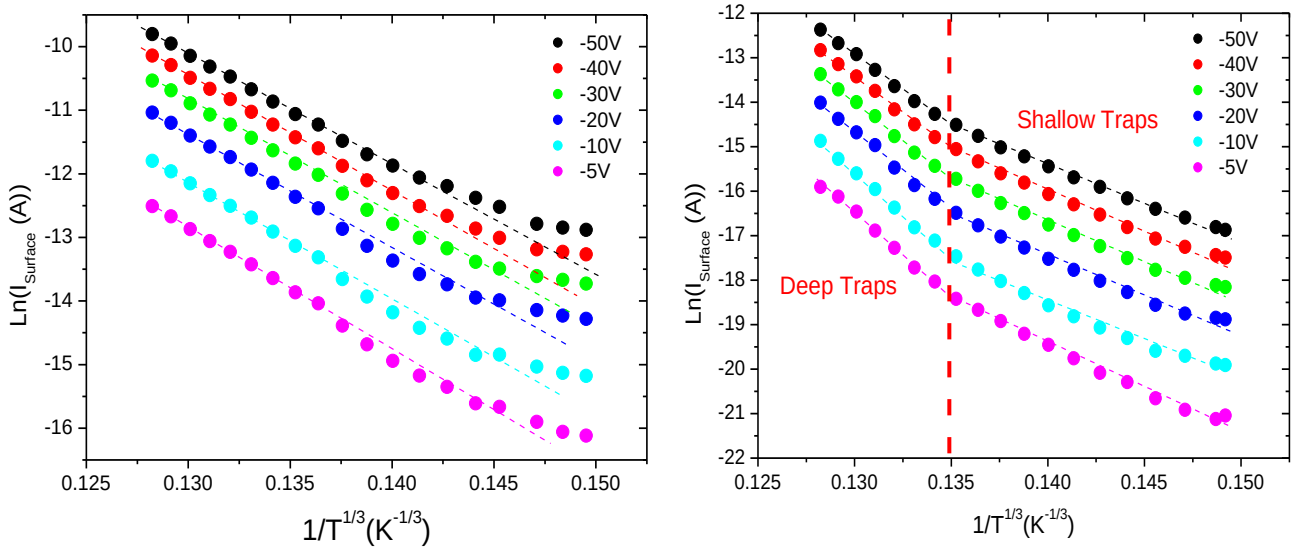
Figure 4.19 Arrhenius plot with activation energies extracted from gate surface leakage component (a) for untreated device (b) for H_2SO_4 treated device.

For the untreated device, a straight line fit can be extended over most of the temperature regime and activation energies are measured in the range ~0.26-0.31eV which agrees well with that reported in the literature [8, 39-40]. Note that there is a departure from the straight line at low temperatures. The reason for this is unclear but it may indicate the onset of the domination of states with much smaller activation energies. (It is also possible to draw two straight lines with overlapping regions to cover low temperature points but we stick with one line since it covered most experimental points). However, for the H_2SO_4 treated device two distinct slope regions can be seen. In the lower temperature region (<130^{0}C) the activation energy is similar to the untreated device, but at higher temperature (>130^{0}C) it has increased significantly to around ~0.5-0.6eV. For both cases the activation energy reduces with an increase in applied voltage. The clear dependence of surface leakage current on temperature rules out a tunneling mechanism. A two-dimensional variable range Mott hopping (2D-VRH) conduction model was used to analyze the data. The temperature dependent conductivity, σ, is given by the Mott expression in equation 4.3. [41-42]

$$\sigma\,(T)\;\alpha\;\exp\,[\,-\,(1/T)^{1/(d+1)}]\quad \text{where d is the dimension}$$

$$\sigma\,(T)\;\alpha\;\exp\,[\,-\,(1/T)^{1/3}]\quad \text{for our case (d=2)} \qquad [4.3]$$

where T is the temperature in Kelvin.



(a) (b)

Figure 4.20 Mott's hopping conduction model plot of surface leakage with $1/T^{1/3}$ temperature dependence (a) for untreated device (b) for H_2SO_4 treated device.

Plots of surface leakage current versus $1/T^{1/3}$ are shown for both the untreated and H_2SO_4 treated device in figure 4.20(a) and (b) respectively. A good fit of the surface leakage current with the 2D-VRH model is obtained. In contrast to the untreated device, two distinct fits in the H_2SO_4 treated device suggests that at the lower temperature range (<130^{0}C) electron hopping along the surface states is via shallow states and in the higher temperature (>130^{0}C) range electrons trapped in the deeper states are also introduced. These results indicate that even though H_2SO_4 treatment has reduced the interface trap charge density (D_{it}), in turn reducing gate leakage current, it has introduced some deeper level electron traps on the surface.

To understand the dependence of activation energy on applied voltage, Poole Frenkel behavior [18] is considered, as mentioned before in equation 4.1. The observed exponential dependence of surface leakage current with the square root of applied voltage (V_b), a characteristic of Poole Frenkel emission, is plotted with different temperatures for both the untreated and H_2SO_4 treated devices as shown in figure 4.21(a) and (b) respectively. In these plots, applied voltage is considered instead of electric field since it is very complex to calculate the electric field for surface leakage structure. Nonetheless, applied voltage must be proportional to the electric field. These excellent straight line fits suggest that a hopping conduction model combined with Poole Frenkel emission is responsible for the surface leakage mechanism.

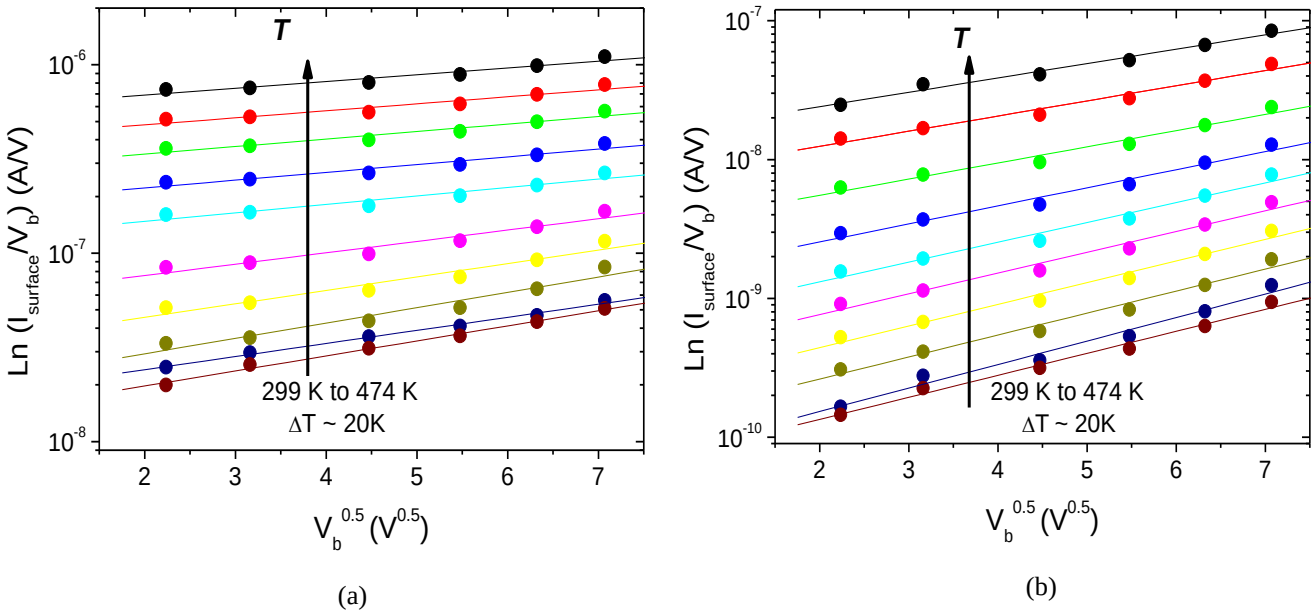
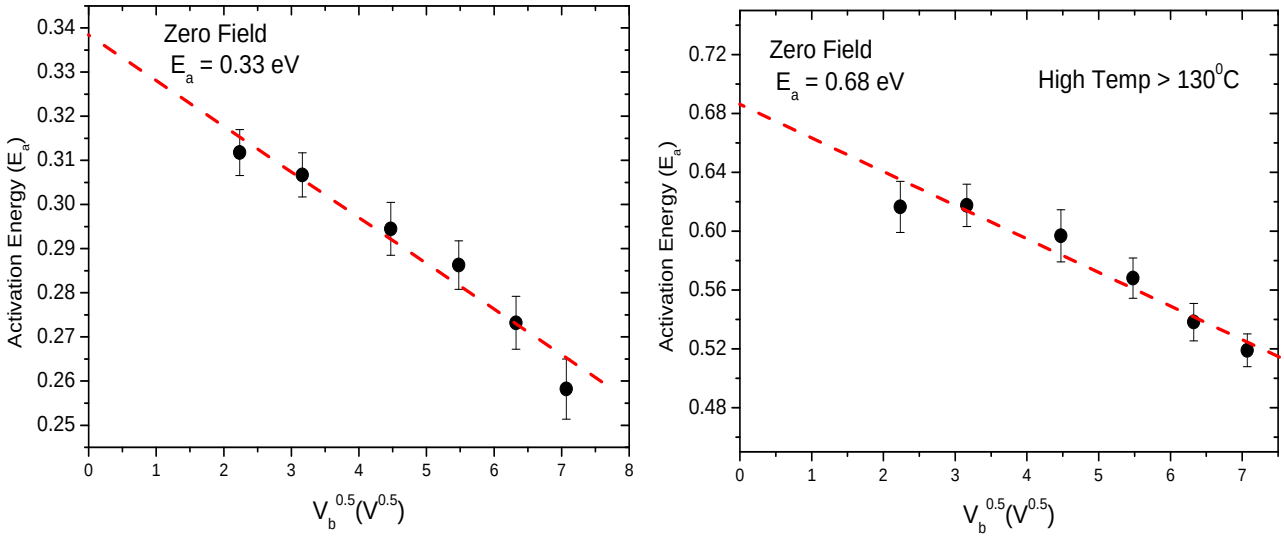


Figure 4.21 Plot of log ($I_{surface}/V_b$) versus square root of applied voltage (V_b) at different temperatures (a) for an untreated device and (b) for an H_2SO_4 treated device.

The extrapolated values of activation energy to zero bias from the plots of figure 4.19 are shown in figure 4.22. The zero bias activation energy values are a measure of the trap depth in the absence of any applied electric field. For the untreated device the activation energy is 0.33eV which is in good agreement with the low-bias Arrhenius plots of figure 4.19(a) and the trap depths reported previously [8, 39-40]. However, for the H_2SO_4 treated device the activation energy is very similar at low temperatures (0.3eV) but increases significantly to 0.68eV at high temperatures. This again highlights the fact that the H_2SO_4 treatment has introduced some deep level traps in the surface states.



(a) (b)

Figure 4.22 Extrapolated values of activation energy to zero bias plotted against the square root of voltage for (a) untreated device (b) H_2SO_4 treated device at high temperatures (>130^{0}C).

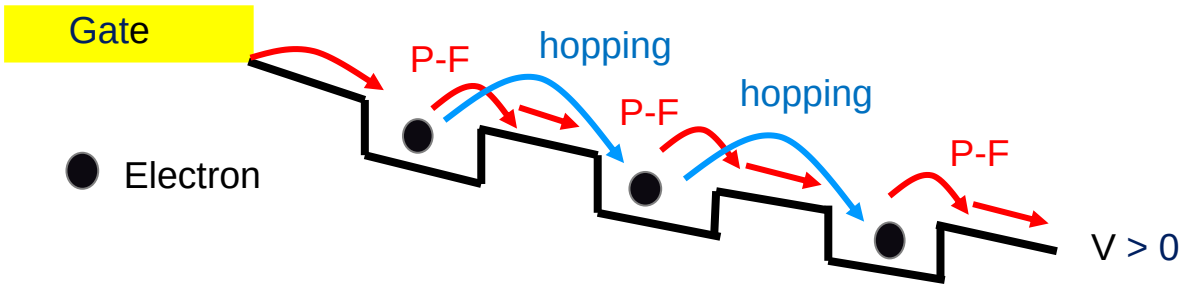


Figure 4.23 Gate surface leakage mechanism along the surface states explained by combined effect of hopping conduction (blue) and Poole-Frenkel (red) behavior.

The proposed model for the surface leakage conduction is shown in figure 4.23. From the experimental results, it appears that electron hopping conduction (jumping from one state to another) and Poole Frenkel behaviour (emission into conduction band from traps) co-exist for electron transport mechanism along the surface states. It is important to note that the hopping conduction would depend on the number of available surface traps and also on the distance between them which is likely to be a variable along the surface. Therefore, it is likely that electron hopping conduction dominates when the traps are very close together and Poole Frenkel emission occurs for traps which are widely separated.

4.6.2 Effect of SiN_x passivation on Surface Leakage

As mentioned before, SiN_x passivation is generally required in AlGaN/GaN HFETs to reduce current collapse and to support field plates [33]. However, the SiN_x passivation often results in increased gate leakage current which generally comes from the bulk leakage component. The physical mechanism leading to high gate leakage after passivation is not clearly understood. Some reports have identified silicidation of Ni metal in the gate edge after SiN_x passivation [43], reducing the work function and thus increasing the gate leakage current. There is also some inconsistency reported in the literature on the effect of SiN_x passivation on the gate surface leakage component [44]. The influence on surface leakage current would depend on various factors including initial conditions of the epitaxial surface, refractive index of the dielectric film and deposition conditions (including RF plasma power and chamber cleanliness). In this work, we have observed a variable behaviour of SiN_x passivation on the gate leakage current across different wafers processed at different time and different deposition conditions. The surface leakage test structure results after SiN_x passivation is shown in figure 4.24, indicating an order of magnitude increase in bulk leakage and a slight increase in surface leakage component.

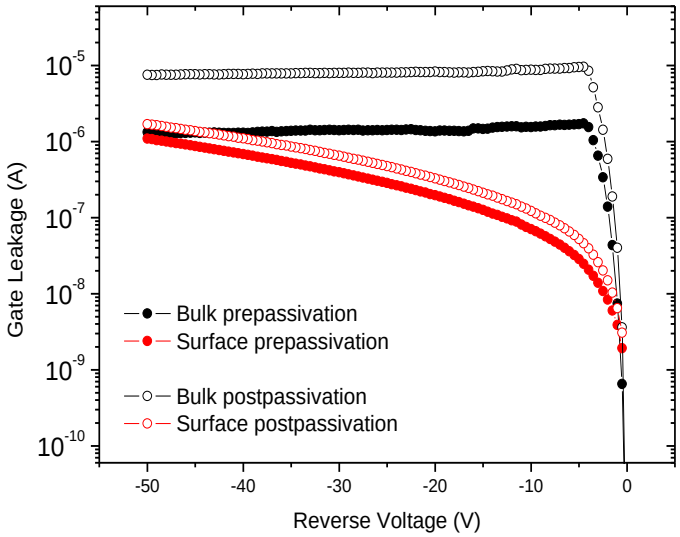


Figure 4.24 Gate surface leakage test structure after SiN_x passivation.

Despite the fact that SiN_x passivation causes an increase in gate leakage current, it is very effective in reducing the current collapse caused by surface related charge trapping effects. In order to characterise the trapping behaviour, we did some single pulse, gate lag measurements using the circuit configuration shown in chapter 2, figure 2.7. In the pulse measurements, the device is biased by a dc voltage source in the off-state below the gate pinch-off voltage (-6V) and then the gate is turned on by a short duration pulse (~400ns) during which the drain current flows and its magnitude is measured. The gate lag is the ratio of pulse to dc drain current at fixed drain-source bias (V_{DS}=10V) and the results are shown in the figure 4.25.

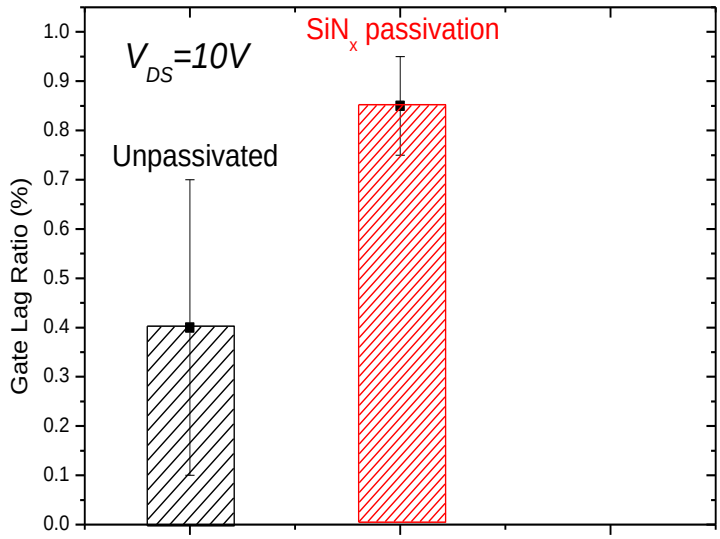
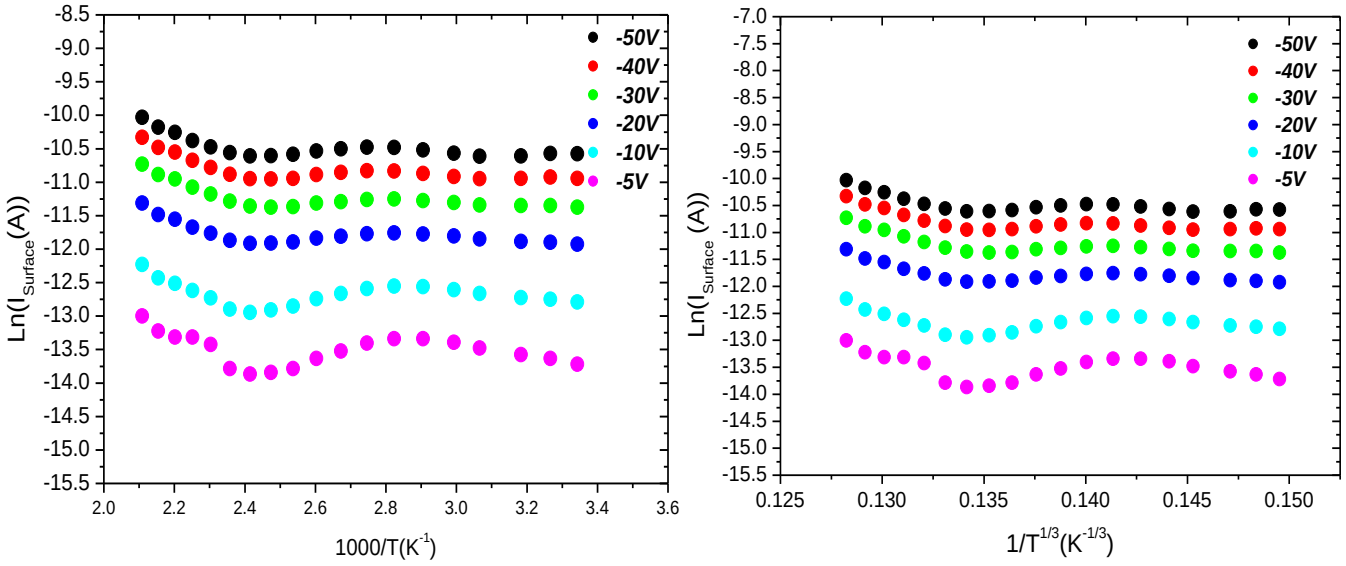


Figure 4.25 Gate lag ratio (%) before and after SiN_x passivation measured at $10V_{DS}$.

After the SiN_x passivation, the gate lag ratio is drastically improved to 0.85±0.1 compared to 0.4±0.3 for the unpassivated devices. These results indicate the effectiveness of SiN_x passivation in mitigating the surface related current collapse behaviour.

In order to further understand the surface leakage transport mechanism after SiN_x passivation Arrhenius plot of surface leakage current at different voltage bias is shown in figure 4.26(a). In contrast to the unpassivated and H_2SO_4 treated devices, very small and almost negligible activation energy values (<50meV) are observed after SiN_x passivation which suggest that passivation layer has effectively buried the surface states responsible for charge trapping

effect. However, an increase in surface leakage goes hand in hand with reduced activation energy.



(a) (b)

Figure 4.26 (a) Arrhenius plot of surface leakage current after SiN_x passivation (b) Hopping conduction model fit for surface leakage after SiN_x passivation.

The mechanism of surface leakage after SiN_x passivation also does not fit the two-dimensional variable range (2D-VRH) Mott hopping conduction model as shown in figure 4.26(b). These results indicate that SiN_x layer has replaced the temperature dependent leakage mechanism and introduced some additional leakage phenomenon (possibly tunnelling via the SiN_x layer).

4.6.3 Optimum combination of H_2SO_4 and SiNx passivation

As discussed before, H_2SO_4 treatment effectively reduces the gate leakage current but introduces some deep level traps. The presence of deep levels surface states can be catastrophic as electrons get trapped in the surface states under normal switching conditions causing a reduction in the total available drain current (current collapse) due to their sluggish response to changing bias. Therefore, to reduce the charge trapping effects and gate leakage and to improve the S.S., H_2SO_4 pre-gate metal treatment is combined with 100nm PECVD SiN_x surface passivation and the gate transfer results are shown in the figure 4.27. This optimum configuration sustains a low gate leakage (<1μA/mm) with reduced sub-threshold

slope (100±10mV/dec). These results indicate the effectiveness of chemical treatment before SiN_x passivation to sustain a low gate leakage and S.S.

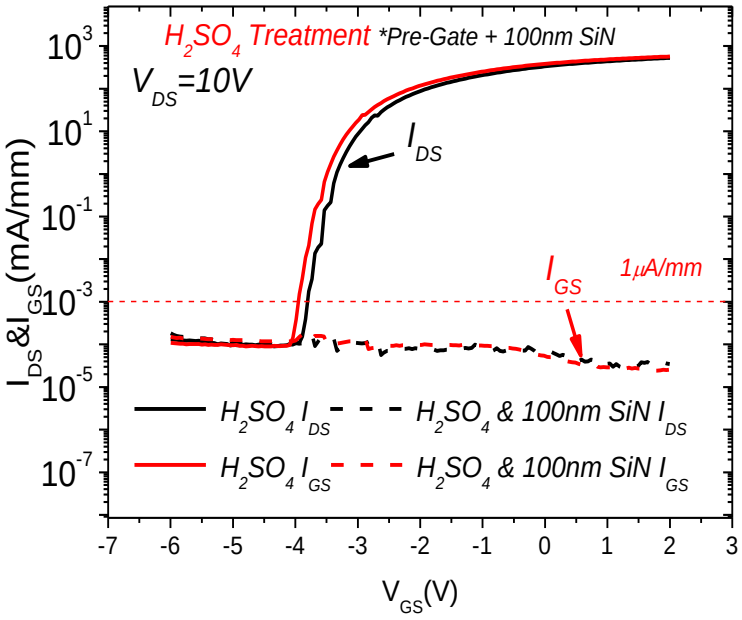


Figure: 4.27 Gate transfer characteristics of AlGaN/GaN HFETs with H_2SO_4 treatment (pre-gate metal) combined with 100nm SiN passivation.

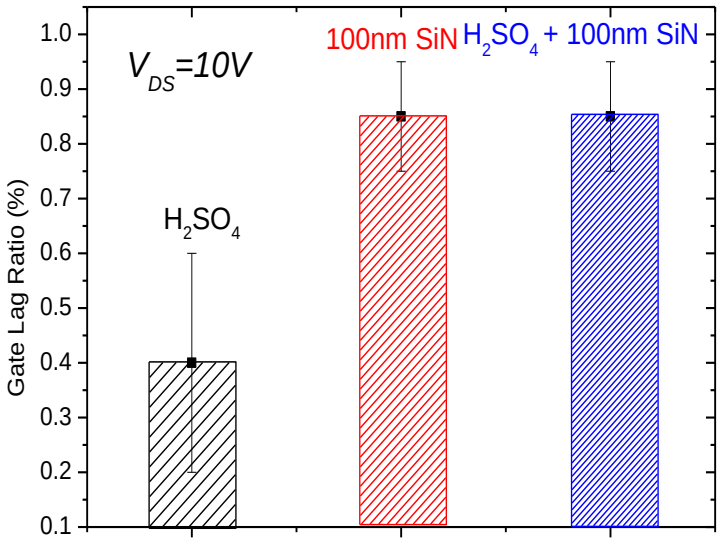


Figure: 4.28 Gate lag ratio (%) of AlGaN/GaN HFETs with H_2SO_4 treatment, 100nm SiN passivation and combined H_2SO_4 treatment with SiN passivation.

In order to characterize the charge trapping behaviour, the gate lag measurements is performed again and results are shown in figure 4.28. A low gate lag ratio of 0.4±0.2 is

measured in the H_2SO_4 treated devices, showing that the treatment is not effective in mitigating the current collapse. This may be due to the presence of 0.3eV and 0.68eV states which act as electron traps and hence lead to formation of virtual gate. However, with the addition of the 100nm SiN_x passivation gate lag ratio is improved from 0.4±0.2 to 0.85±0.1 which is similar to SiN_x passivation alone.

4.6 Effect of Sulphuric Acid surface treatment on AlInN/GaN HFET

As mentioned before, lattice matched AlInN based HFETs offers high 2DEG density but generally suffers from high level of gate leakage current due to the presence of a thin barrier layer (11nm) (Large electric field in barrier layer due to high (spontaneous) polarization charge together with a thin barrier layer can result in large gate tunnelling current). Therefore, it would be very advantageous to reduce the high gate leakage current in AlInN/GaN HFETs. In this work, we performed H_2SO_4 treatment on AlInN/GaN HFETs and the results of surface leakage test structure are shown in figure 4.29.

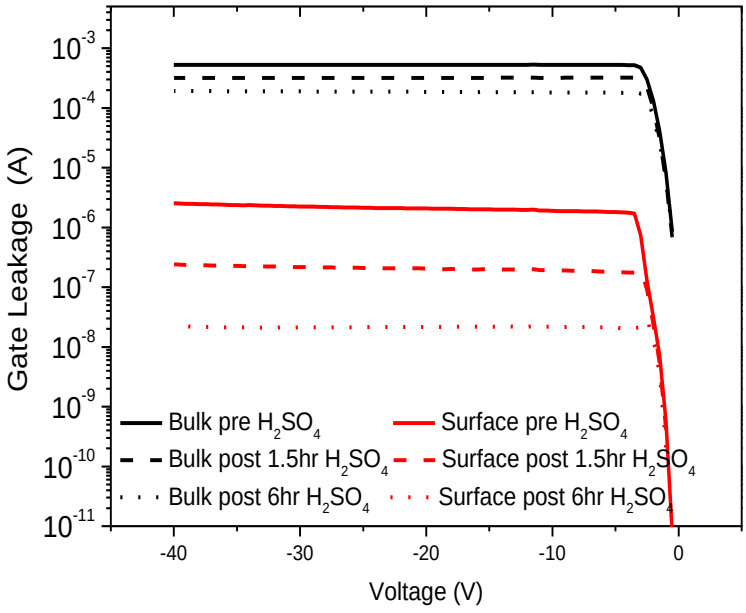


Figure: 4.29 Leakage currents measured from surface leakage test structure after H_2SO_4 chemical treatments on AlInN/GaN HFET.

It is important to note that the AlInN layer has a higher concentration of Al (~83%) and it would potentially oxidize a lot more quickly (forming Al_2O_3 oxide) compared to the AlGaN layer (with ~26% Al concentration) and also if a thin AlInN layer is oxidized or consumed it would drastically reduce the 2DEG concentration and so the drain current. Thus, H_2SO_4

treatment is performed first for 1.5 hours and then 6 hours at room temperature (which is in contrast to H_2SO_4 treatment for AlGaN HFETs where effective suppression is only observed after nearly ~48 hours) and the results are shown in figure 4.29. A systematic suppression of the surface leakage current is observed of more than two orders of magnitude after 6 hours of H_2SO_4 treatment, however only a slight change is seen in the bulk gate leakage which suggests that leakage through the thin barrier is difficult to suppress by H_2SO_4 treatment. Nevertheless, overall gate leakage current is reduced nearly 2 orders of magnitude close to 1µA/mm as shown in gate transfer characteristics of AlInN/GaN HFET after 6 hours of H_2SO_4 treatment in figure 4.30.

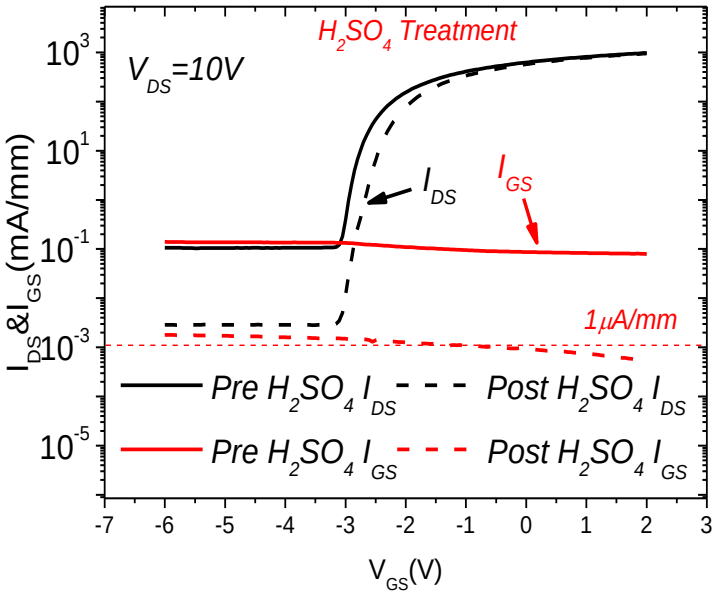


Figure 4.30 Gate transfer characteristics of AlInN/GaN HFETs before and after 6 hours H_2SO_4 post-gate metal treatment.

4.7 Conclusion

In this chapter, AlGaN/GaN and AlInN/GaN HFETs characterization results on Si substrate are presented. To reduce the buffer leakage and vertical substrate leakage for high breakdown voltage operation required in power electronic applications, Fe or C doping is necessary. In contrast to Fe doped HFETs, C doped HFETs are more effective in achieving low buffer leakage and increasing the vertical breakdown electric field (~2MV/cm). The vertical leakage transport mechanism in C and Fe doped wafer is studied and explained by Poole Frenkel emission model. Additionally, we have studied gate surface leakage mechanisms in GaN HFETs and demonstrated a novel method of reducing gate leakage current using chemical

treatments (H_2SO_4 and H_2O_2). The H_2SO_4 treatment is most effective in reducing the gate leakage current. The surface oxidization by the H_2SO_4 treatment has a strong passivating effect and reduces the overall gate leakage current. The chemical treatment can form a very effective and easy method to reduce high gate leakage currents in AlGaN/GaN HFETs. After the treatment the device sub-threshold slope is significantly reduced due to reduction in the interface trap charge density. The gate surface leakage mechanism is explained in detail by a combined Mott hopping conduction and Poole Frenkel models. After the H_2SO_4 treatment some deep level traps are introduced along the surface states resulting in current collapse. Therefore, an optimized H_2SO_4 treatment plus a SiN_x passivation is required to reduce the trap charge density and current collapse whilst maintaining low gate leakage with improved sub-threshold slope.

4.8 References

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Chapter No: 5 Enhancement Mode GaN HFETs

5.1 Introduction

In this chapter, enhancement mode operation in AlGaN/GaN HFETs is discussed by using the fluorine ion implant technique. The requirement for a +3V threshold voltage in the power electronics sector is met by combining the fluorine implant with a dielectric layer. The recipe for fluorine implant in AlInN/GaN HFETs is also optimized to maintain high channel conductivity and transconductance. After the fluorine implant, the sub-surface traps in AlInN barrier are reduced, reflected in improved threshold voltage stability at high temperature.

Due to the presence of an epitaxial AlGaN barrier layer (Al(x) ~ 20-25% and thickness ~ 25-30nm), HFETs are naturally depletion mode devices since the channel charge (2DEG) is present in the quantum well without the requirement to accumulate or induce charge to facilitate current flow. Typically, threshold voltages of the depletion mode AlGaN/GaN HFETs varies from -8 to -4 volts depending on various parameters such as barrier layer (AlGaN) thickness, doping density and Al(x) composition in the barrier layer which can directly influence the 2DEG concentration. However, in power electronics applications, normally-off or enhancement mode AlGaN/GaN HFETs are greatly desired due to the fail safe operation, which prevents device conduction when the gate is grounded, and the need for elimination of negative power supply for the gate drive circuits, enabling single polarity operation with simpler circuit configurations.

In the past, various techniques have been demonstrated in AlGaN/GaN HFETs to achieve normally-off operation, such as gate recessing [1-3], p-type cap layers [4-5], thermal oxidation of AlGaN barrier [6], use of thin barrier layer [7], low damage digital etch techniques to reduce the thickness of barrier [8] and fluorine implant [9]. Each technology has its own merits and drawbacks and there is no clear winner for the development of ultimate enhancement mode transistors. The simplest technique for achieving enhancement mode operation is perhaps gate recessing, where the AlGaN barrier is reduced underneath the gate region to deplete the channel charge. However, due to the lack of well established wet etching techniques for the AlGaN/GaN, low plasma power recipes are mostly used. Such etch techniques are difficult to control precisely and plasma induced damage is almost unavoidable which leads to lower gate or device breakdown voltages. For most p-type GaN or AlGaN cap layer techniques, normally-off devices are restricted by the positive gate turn-

on voltage, limiting the gate swing and hence drain current. Secondly, the desirable p-type doping level with magnesium doping in the GaN cap layer for a high positive threshold voltage (+3V) is difficult to achieve. The thermal oxidation of AlGaN generally involves a high temperature annealing (700-800^{0}C) process which can degrade ohmic contacts and, since photo resist (for gate foot definition) cannot withstand such high temperatures, it is difficult to realize the required self-aligned gate metal structures. The fluorine plasma exposure is a fairly robust technique, where fluorine ions are incorporated underneath the gate region in an ICP or RIE chamber and self-aligned gate metal structures can be easily achieved. However, there is no standard process followed for fluorine implant recipes and various research groups have reported different process parameters. Secondly, the reliability of devices incorporating fluorine ions has been questioned, although recent research reports have suggested excellent thermal stability of fluorine ions in GaN [10-11]. Additionally, to achieve high positive threshold voltage, fluorine implant can be combined with a dielectric layer which can offer higher positive threshold voltage (~+3V) for improved immunity against electromagnetic interference and current spikes. In this work, the fluorine implant technique is used to achieve normally-off operation and optimum conditions for the fluorine implant plus dielectric deposition are identified.

5.2 Fluorine Plasma treatment of AlGaN/GaN HFET

To establish the fluorine based enhancement mode HFETs at the University of Sheffield, fluorine plasma treatment was performed underneath the gate region of AlGaN/GaN HFETs and initial fluorine trial results are shown in figure 5.1 (a), (b), (c) and (d). The fluorine implant was carried out in a RIE chamber using CHF_3 gas with 20 sccm gas pressure, RF plasma power was 150W and exposure time was 200 seconds. In order to recover from any defects introduced during the fluorine implant process, the sample was annealed at 400^{0}C for 10 minutes in a RTA chamber after the formation of Schottky gate contact.

After the fluorine implant, the maximum drain current was reduced to 600mA/mm (at +4V_{GS}) compared to 970mA/mm (at +2V_{GS}) in the depletion mode device. The "on" resistance (R_{ON}) in the fluorine treated device (~6.92ohms.mm) is increased compared with the depletion mode device (~4.22ohms.mm) as shown in figure 5.1(a) and (b). This is due to plasma induced defects introduced during the fluorine implant process. The maximum possible output drain current in fluorine treated devices is restricted by the forward Schottky gate turn-

on causing excessive gate current flow at ~+4V, as shown in figure 5.1(b). At this bias, most of the current flows into the gate rather than between source and drain contacts.

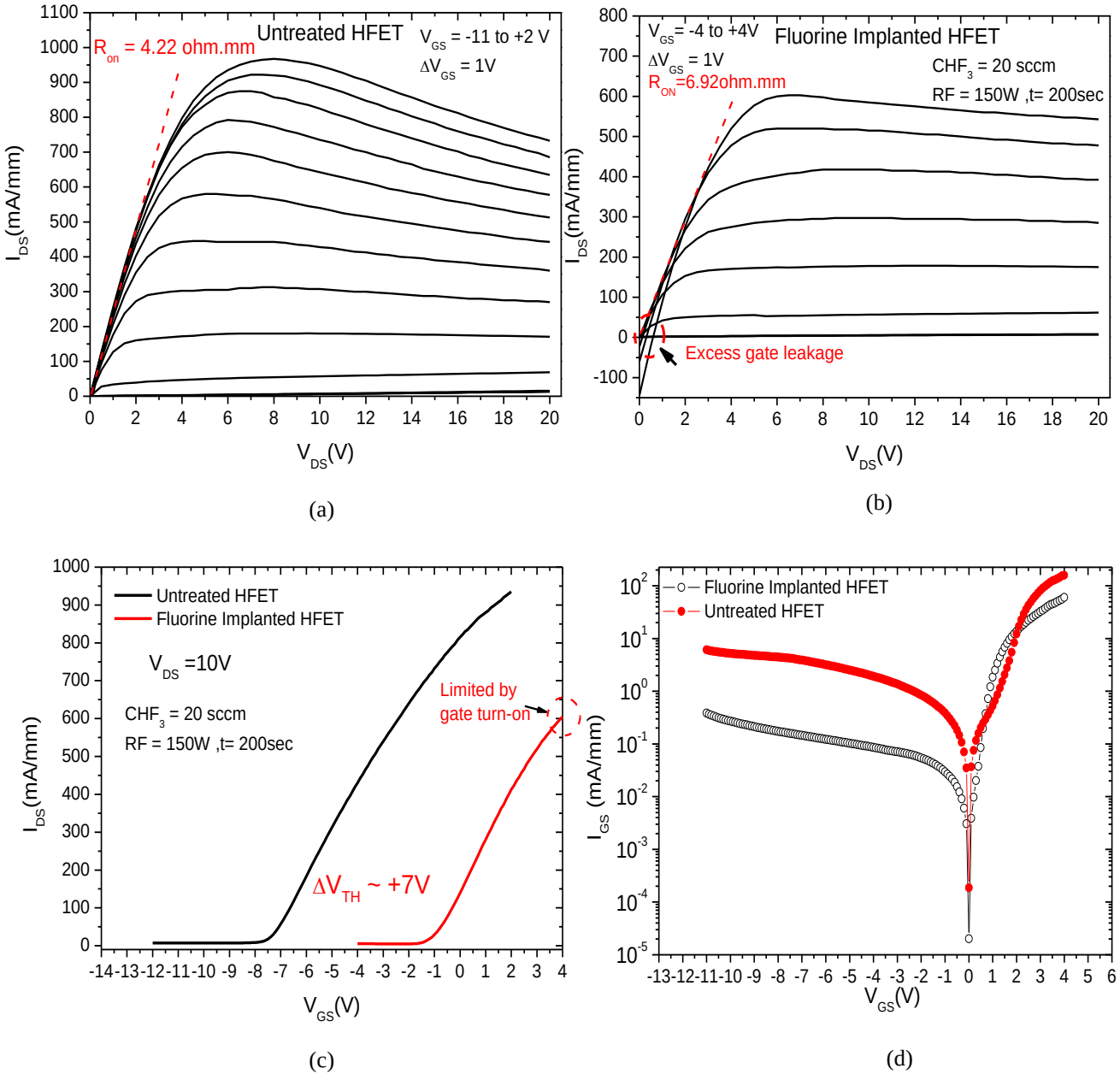


Figure 5.1 (a) IV Output Characteristics of untreated AlGaN/GaN HFET (b) fluorine treated AlGaN/GaN HFET (c) Gate transfer Characteristics of untreated and fluorine treated devices (d) Schottky gate leakage comparison of untreated and fluorine treated devices. (The wafer characteristics are, $n_s = 1.3 \times 10^{13}$ cm^{-2}, d = 40nm, electron mobility, μ_n = 1140 $cm^{-2}V^{-1}s^{-1}$ and Rs = 420 Ω/sq).

A significant positive shift in the threshold voltage (~ +7V) is observed after the fluorine implant as shown in figure 5.1(c). The fluorine ions possess strong electronegativity and behave as immobile, negatively charged, acceptor-like deep level states in AlGaN/GaN [9]. The fluorine ions in the AlGaN barrier effectively deplete the 2DEG channel directly underneath it by raising the conduction band of the heterostructure. Due to the negative charge accumulation in the AlGaN region, an upward band bending in the conduction band is observed [9], which increases the effective Schottky barrier height ($\phi_b + \phi_{fb}$) as shown in figure 5.2. The increased barrier height results in suppression of the Schottky gate leakage by nearly ~1.5 orders of magnitude compared to untreated depletion mode device as shown in figure 5.1(d).

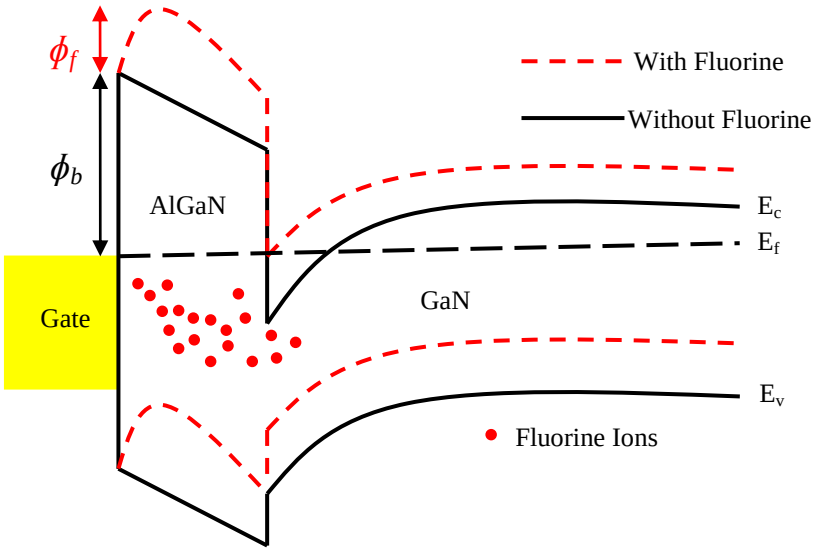
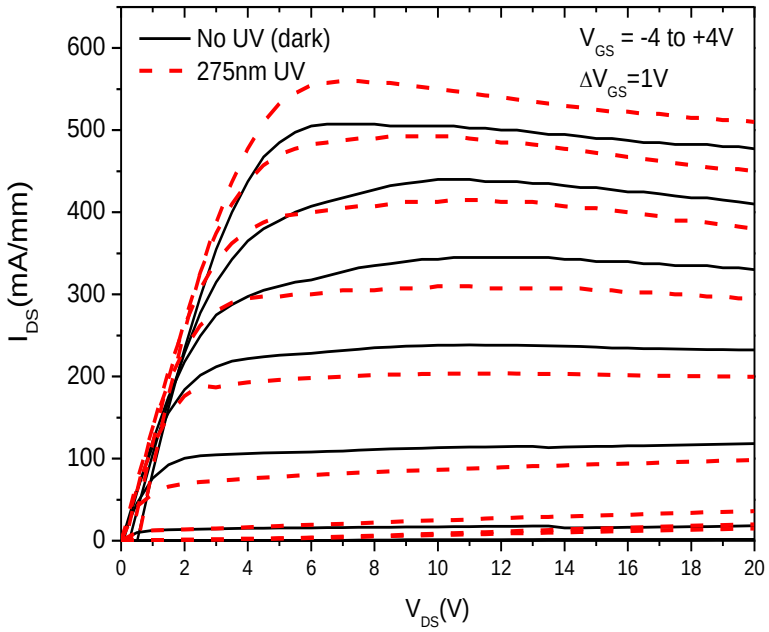


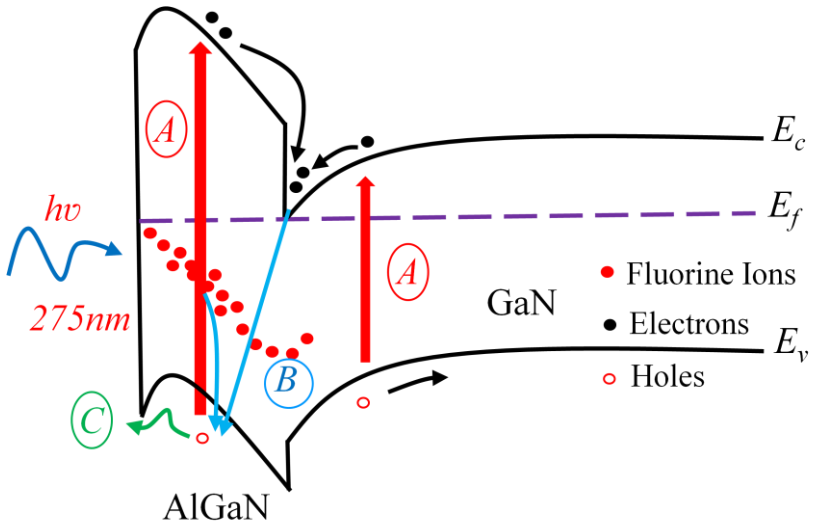
Figure 5.2 AlGaN/GaN heterostructure band bending without and with (broken red line) fluorine implant.

5.3 UV Excitation of Fluorine Treated HFET

In order to further understand the role of fluorine ions in the AlGaN/GaN HFETs, UV light excitation of fluorine treated HFET was performed similar to the depletion mode HFETs mentioned in Chapter 3. The output IV characteristics of the HFET under 275nm UV wavelength (sufficient energy to cause band to band transition in AlGaN barrier and GaN buffer region) and heterostructure band diagram are shown in figure 5.3 (a) and (b) respectively.



(a)

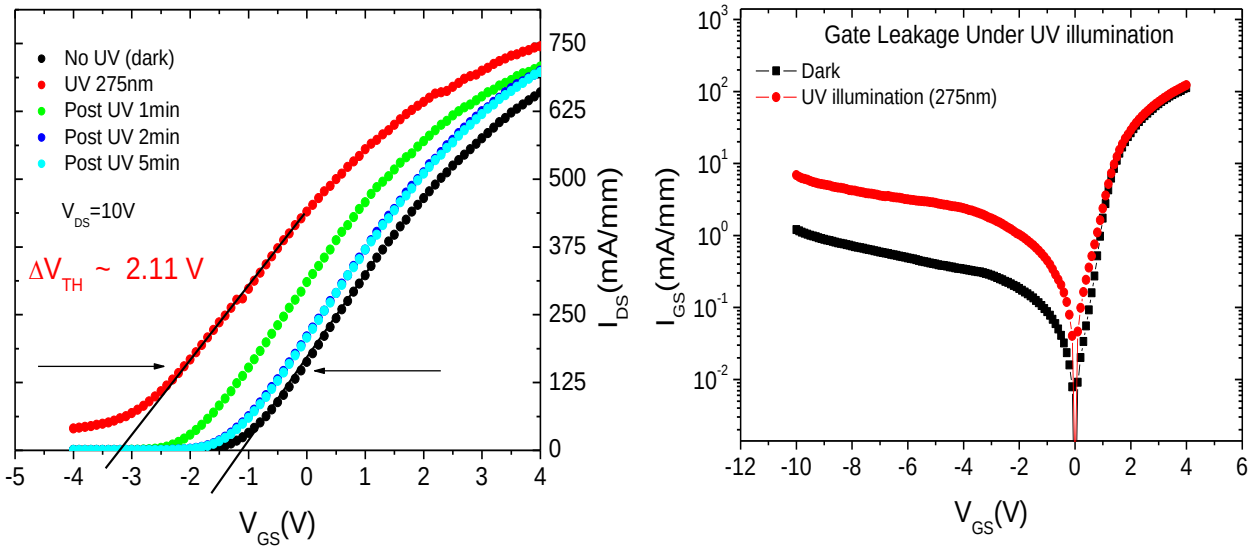


(b)

Figure 5.3 (a) Output Characteristics of fluorine treated AlGaN/GaN HFET under UV illumination (b) Equivalent mechanisms within the device band structure.

With UV light illumination, an increase in drain current was observed and the magnitude of increase is much higher than the untreated or depletion mode devices reported in chapter 3 under the same illumination conditions. The mechanism of photo current generation is explained by the band structure of the device in figure 5.3 (b) and described below in several steps.

A. With UV illumination, electron-hole pairs are generated in the AlGaN barrier layer and the GaN buffer region. Electrons in both cases contribute to the 2DEG, enhancing channel conductivity similar to depletion mode devices.
B. The holes created in the GaN region will create a similar photo voltage effect as in the depletion mode devices. However, for the hole transport, in the AlGaN barrier, there is a maximum in the valence band due to the fluorine ions which can enhance the hole trap lifetimes and allows them to slowly recombine either directly with the 2DEG electrons or via un-annealed defects in the fluorine treated region.
C. Both mechanism A and B should weaken the depletion in the 2DEG channel, which is reflected by the large negative shift of threshold voltage (~2V) in these devices shown in figure 5.4 (a). The accumulation of holes will counter the fluorine charge and barrier maximum caused by fluorine ions which is reflected in enhanced Schottky gate leakage under UV illumination as shown in figure 5.4 (b). The holes which do not recombine in the barrier will eventually flow into the gate electrode.



(a) (b)

Figure 5.4(a) Gate Transfer Characteristics of fluorine treated AlGaN/GaN HFET under UV illumination (b) Schottky Gate Leakage under dark and UV illumination.

A persistent photoconductivity effect is observed in fluorine treated devices as shown by post illumination gate transfer curves in figure 5.4 (a). This suggests a very slow recombination or decaying process of the photo generated holes.

5.4 Optimum Recipe for Fluorine Implant

The first enhancement mode device by implanting fluorine ions using CF_4 plasma treatment in HFETs was demonstrated by Chen et al [9]. However, it was recently proposed by C. H. Chen et al [12] that CHF_3 can offer a much improved performance compared to CF_4 because hydrogen atoms in CHF_3 compensate for Ga induced defects and traps which are introduced during plasma exposure. In the clean room facility at the University of Sheffield, CF_4 gas is not available, therefore, we compared CHF_3 and SF_6 based recipes for fluorine exposure.

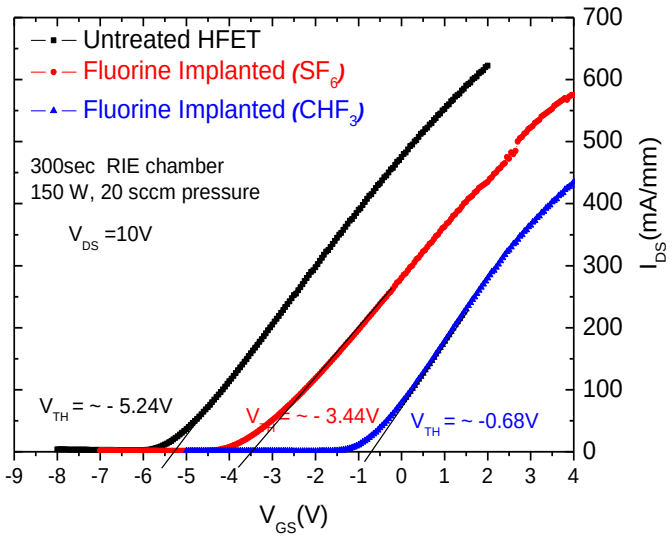
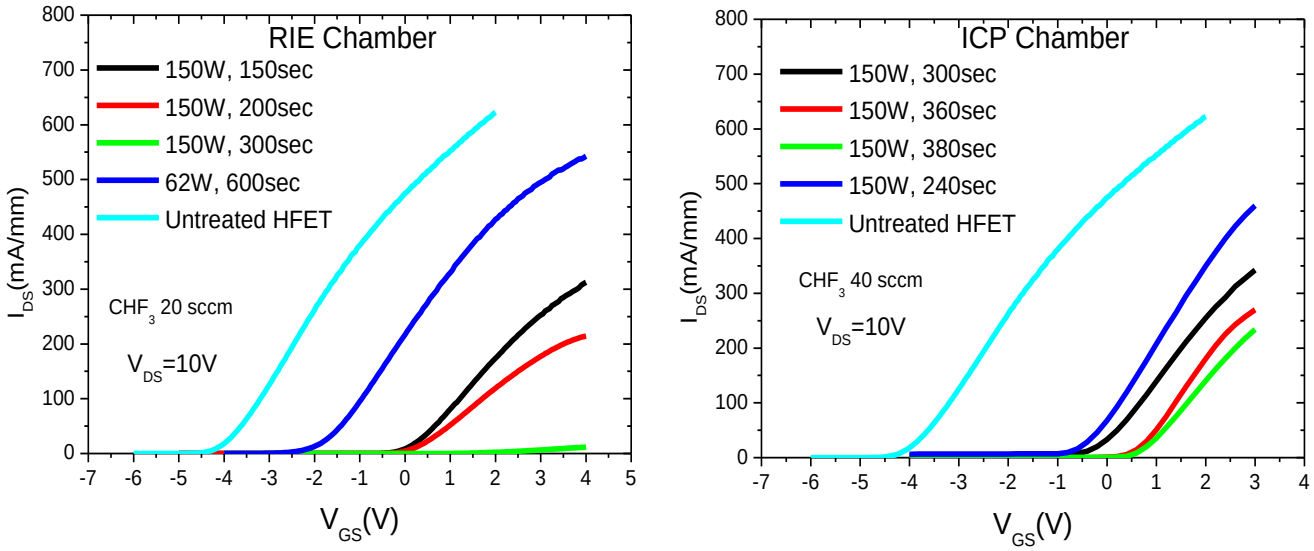


Figure 5.5 Gate Transfer Characteristics of untreated HFET and fluorine treated HFET with CHF_3 and SF_6 recipe. (The wafer characteristics are $n_s = 1 \times 10^{13} cm^{-2}$, $d = 28nm$, $\mu_n = 991\ cm^{-2}V^{-1}s^{-1}$ and $R_s = 400\ \Omega/sq$).

The gate transfer characteristics of the untreated, CHF_3 and SF_6 gas based, fluorine treated HFETs are shown in the figure 5.5. Under the same plasma exposure time (300 seconds), RIE RF power (150 W) and gas flow pressure (20 sccm), a much larger positive shift in the threshold voltage is obtained with the CHF_3 recipe. The Schottky gate leakage is also slightly more reduced with CHF_3 plasma compared to SF_6. Based on these observations, CHF_3 gas is used in all future devices for the fluorine ions implant process.

5.5 Optimum Plasma Exposure for Fluorine Implant

In order to achieve proper enhancement mode operation with threshold voltage greater than zero volts, fluorine plasma treatment optimization was carried out in both a Reactive Ion Etching (RIE) chamber and Inductively Coupled Plasma etch chamber (ICP). The results are shown in figure 5.6.



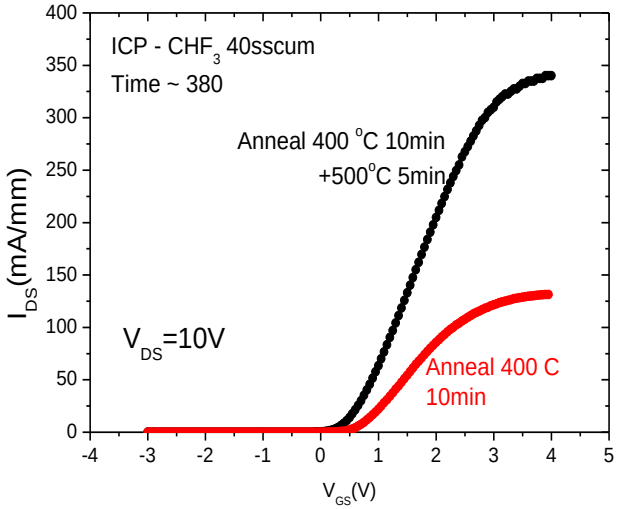
(a) (b)

Figure 5.6 (a) Gate transfer characteristics after fluorine plasma treatment in RIE chamber (b) Gate transfer characteristics after fluorine plasma treatment in ICP chamber.(The wafer characteristics are $n_s = 7.2 \times 10^{12} cm^{-2}$, d = 27nm, $\mu_n = 1476\ cm^{-2}V^{-1}s^{-1}$ and $R_s = 545\ \Omega/sq$).

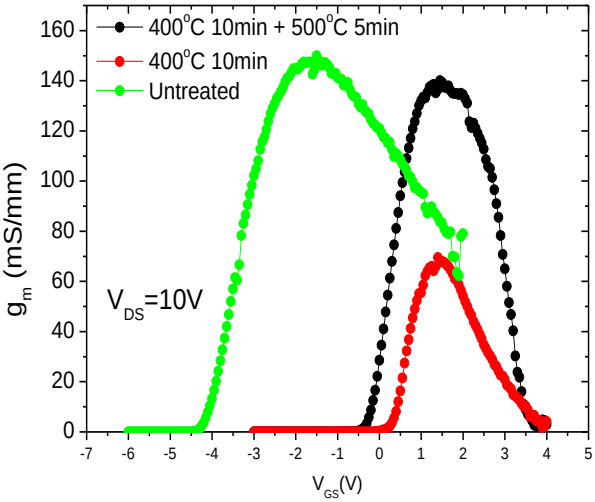
As shown in figure 5.6, the threshold voltage of the HFET shifts in a positive direction with increasing fluorine plasma exposure time (consistent with increasing fluorine concentration in the AlGaN barrier) in both RIE and ICP chambers. In both cases, CHF_3 gas is used as a fluorine ion source and RF power of 150 W with different exposure times (RIE 150sec and 200sec and for ICP 360sec and 380sec) in two chambers resulted in threshold voltage greater than zero volts. It can be seen that maximum output drain current is also suppressed with increasing fluorine plasma exposure time (overexposure) due to plasma induced defects. Therefore, more than optimized fluorine plasma exposure can significantly degrade device performance by reducing the drain current and transconductance of the device.

After fluorine exposure, rapid thermal annealing (RTA) is preformed to recover from any plasma induced damage which restricts the maximum drain current [9]. The annealing results are shown in figure 5.7. After 500^0 C annealing for 5 minutes considerable recovery in the

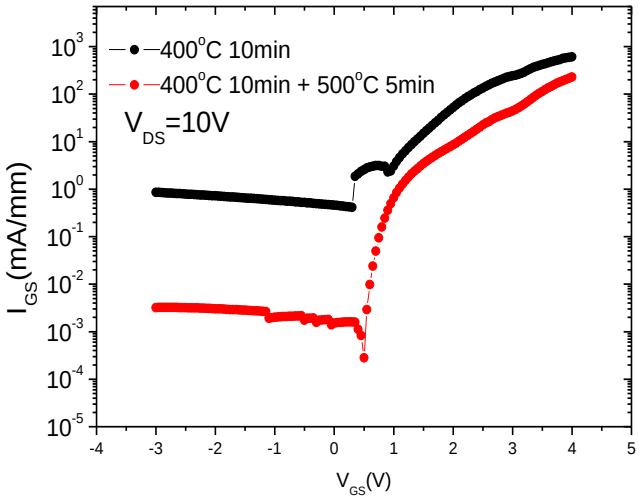
drain current is achieved compared to annealing at 400^0 C for 10 minutes. The peak transconductance is almost fully recovered (~140mS/mm) to depletion mode level (for the D-mode device 150mS/mm) after 500^0C annealing. However, there is a slight but noticeable negative shift in the threshold voltage from +0.7V after 400^0C to +0.4V after 500^0C annealing [9]. Annealing at even higher temperatures results in even more negative shift and eventually the threshold voltage becomes negative. The Schottky gate leakage is also suppressed after 500^0C due to reduced plasma induced defects but the forward gate current is still dominated by the Schottky diode turn-on voltage.



(a)



(b)



(c)

Figure 5.7 (a) Gate transfer characteristics comparison after fluorine plasma treatment with annealing at different temperatures (b) Transconductance comparison after fluorine plasma treatment annealed at different temperatures (c) Gate leakage comparison after fluorine plasma treatment with annealing at different temperatures. (The wafer characteristics are $n_s = 6.7 \times 10^{12}cm^{-2}$, d = 30nm, $\mu_n = 1773\ cm^{-2}V^{-1}s^{-1}$ and $R_s = 450\ \Omega$/sq).

5.6 Threshold Voltage derivation of AlGaN/GaN HFETs and MISHFETs

In this section, a threshold voltage equation is derived to aid the understanding of the various influencing factors. For enhancement mode AlGaN/GaN HFETs with and without oxide/dielectric layer, Gauss's Law [13] is considered as expressed in equation 5.1 which can be applied to each interface of the AlGaN/GaN HFET as follows.

$$\varepsilon_1 E_1 - \varepsilon_2 E_2 = \text{interfacial charge} \qquad [5.1]$$

where, E_1 and E_2 are the normal components of the electric field at the interface. The conduction band diagram is shown in figure 5.8

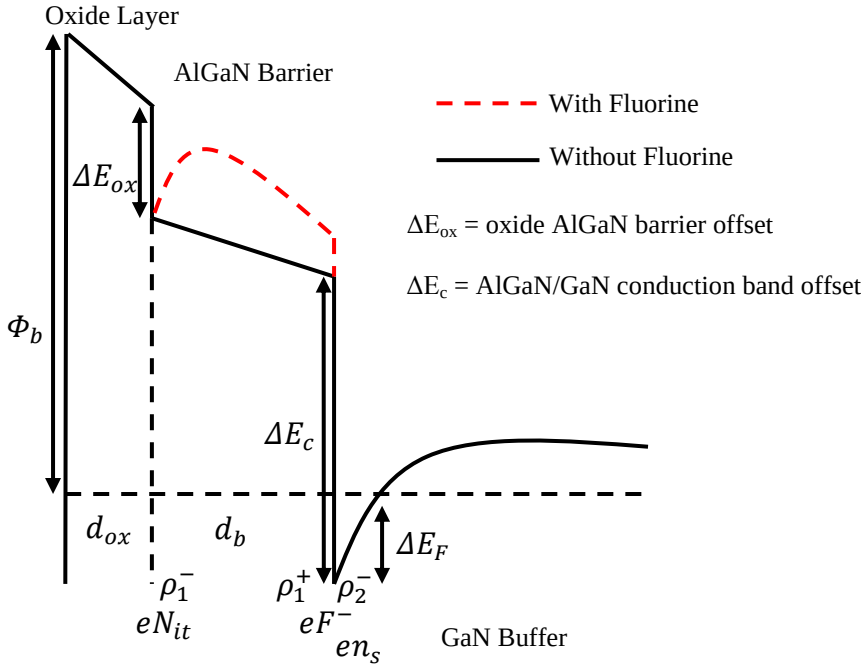


Figure 5.8 Conduction Band diagram of AlGaN/GaN HFET with oxide/dielectric layer showing band offsets and charge distribution.

Applying Gauss's Law to each interface of AlGaN/GaN HFET,

$$\varepsilon_{ox} E_{ox} - \varepsilon_b E_b = eN_{it} - \rho_1^- \qquad [5.2]$$

$$\varepsilon_b E_b - \varepsilon_{bu} E_{bu} = \rho_T - eF^- - en_s \qquad [5.3]$$

where, ε_{ox}, ε_b and ε_{bu} are the permittivity of oxide/dielectric layer, AlGaN barrier and GaN buffer region respectively and E_{ox}, E_b and E_{bu} are the electric fields perpendicular to the interface in the oxide/dielectric layer, AlGaN barrier and GaN buffer region respectively.

Converting the electric fields used in expression 5.2 and 5.3 to the respective voltage drops across each region, assuming zero space charge away from the interfaces

$$\varepsilon_{ox}\ \frac{V_{ox}}{d_{ox}}\ -\ \varepsilon_b\ \frac{V_b}{d_b} = eN_{it} - \rho_1^- \qquad [5.4]$$

$$\varepsilon_b\ \frac{V_b}{d_b} - \varepsilon_{bu}\ \frac{V_{bu}}{d_{bu}} = \rho_T - eF^- - en_s \qquad [5.5]$$

where, d_{ox}, d_b and d_{bu} are the thickness of oxide/dielectric layer, the AlGaN barrier and the GaN buffer region respectively. V_{bu} is zero which simplifies equation 5.5 and substituting it into expression 5.4 gives ($\rho_2^- = \rho_T - \rho_1^+$) the voltage developed across the oxide/dielectric and AlGaN barrier layer,

$$V_{ox} = \frac{d_{ox}}{\varepsilon_{ox}}\ (eN_{it} - eF^- - en_s - \rho_2^-) \qquad [5.6]$$

$$V_b = \frac{d_b}{\varepsilon_b}\ (\rho_T - eF^- - en_s) \qquad [5.7]$$

From inspection of figure 5.8,

$$(\Phi_b - eV_{ox} - \Delta E_{ox} - eV_b - \Delta E_c\ +\ \Delta E_F)\ =\ 0 \qquad [5.8]$$

Using the expression of V_{ox} and V_b in equation 5.8 and solving for n_s,

$$en_s = \frac{C_b}{C_{ox}+C_b}(eN_{it} - eF^- - \rho_2^-) + \frac{C_{ox}}{C_{ox}+C_b}(\rho_T - eF^-) - \frac{C_{ox}\,C_b}{C_{ox}+C_b}\left(\frac{1}{e}\right)(\Phi_b - \Delta E_{ox} - \Delta E_c\ +\ \Delta E_F) \qquad [5.9]$$

where, $C_b = \frac{\varepsilon_b}{d_b}$ and $C_{ox} = \frac{\varepsilon_{ox}}{d_{ox}}$ are the barrier and oxide capacitance respectively.

For no oxide layer, $d_{ox} = 0$, $C_{ox} = \infty$ and $\Delta E_{ox} = 0$. Therefore, equation 5.9 is simplified,

$$n_s = \frac{\rho_T}{e} - F^- - \frac{\varepsilon_b}{e^2 d_b}(\Phi_b - \Delta E_c\ +\ \Delta E_F) \qquad [5.10]$$

Adding a gate bias (V_G) to equation 5.8, $\Phi_b = \Phi_b - eV_G$ (Φ_b enhanced with negative V_G) and setting, the gate voltage (V_G) equal to the threshold voltage (V_{TH}) when the 2DEG charge is zero (n_s = 0), gives the expression of threshold voltage for AlGaN/GaN MISHFET,

$$V_{TH} = \frac{1}{e}(\Phi_b - \Delta E_{ox} - \Delta E_c + \Delta E_F) - \frac{d_{ox}}{\varepsilon_{ox}}(eN_{it} - eF^- - \rho_2^-) - \frac{d_b}{\varepsilon_b}(\rho_T - eF^-) \quad [5.11]$$

In the absence of any oxide/dielectric layer equation 5.11 is simplified to

$$V_{TH} = \frac{1}{e}(\Phi_b - \Delta E_c + \Delta E_F) - \frac{d_b}{\varepsilon_b}(\rho_T - eF^-) \quad [5.12]$$

It can be seen from equation 5.11, that in the absence of fluorine ions (F^-= 0), dielectric layer deposition will push the threshold voltage more negative due to the term $-\frac{d_{ox}}{\varepsilon_{ox}}(eN_{it})$ which is consistent with experimental results and what is observed in the literature for depletion mode MISHFETs [14]. The presence of fluorine ions obviously increases the threshold voltage towards the positive direction as indicated by equation 5.12 but the enhancement mode operation in MISHFETs is only possible once the fluorine ions concentration is sufficient to balance the interfacial charge, eN_{it}, minus the polarization charge at the upper GaN layer, ρ_2^-. In a scenario where fluorine is insufficient to balance this charge, deposition of the dielectric layer would result in a negative threshold voltage shift.

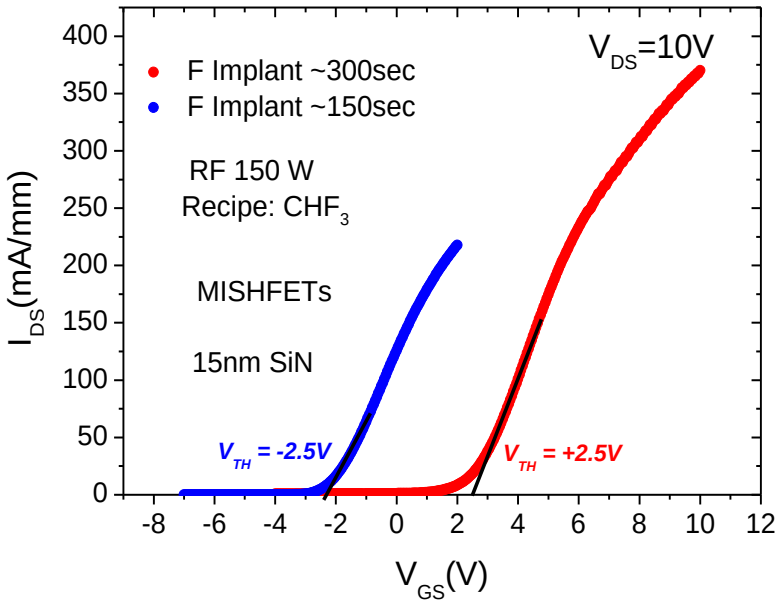


Figure 5.9 Gate transfer characteristics of AlGaN/GaN MISHFETs (15nm SiN) with different fluorine implant exposure time. (The wafer characteristics are $n_s = 1 \times 10^{13}cm^{-2}$, d = 28nm, μ_n = 991 $cm^{-2}V^{-1}s^{-1}$ and R_s = 400 Ω/sq).

Figure 5.9 shows the gate transfer characteristics of the AlGaN/GaN MISHFETs with the same dielectric layer thickness (15nm SiN_x) but different fluorine exposure times (150 and 300sec). The 150sec fluorine exposure is insufficient to counter balance the interface charge minus the polarization charge at the upper GaN layer, a direct consequence of which is a negative threshold voltage (-2.5V) after dielectric layer deposition. On the other hand, with 300sec exposure, the fluorine concentration is sufficient to balance this charge and thus a positive threshold voltage (+2.5) is achieved in AlGaN/GaN MISHFETs. In practical terms, the threshold voltage before any dielectric layer deposition needs to be slightly greater than zero volts (>0V) for it to shift in a positive direction or else the dielectric layer will always push the threshold voltage in a negative direction. These results highlight the fact that threshold voltage must be controlled precisely before any dielectric layer deposition for a positive shift and material inconsistency, including barrier layer thickness non-uniformity, must be taken into account for variation in threshold voltage.

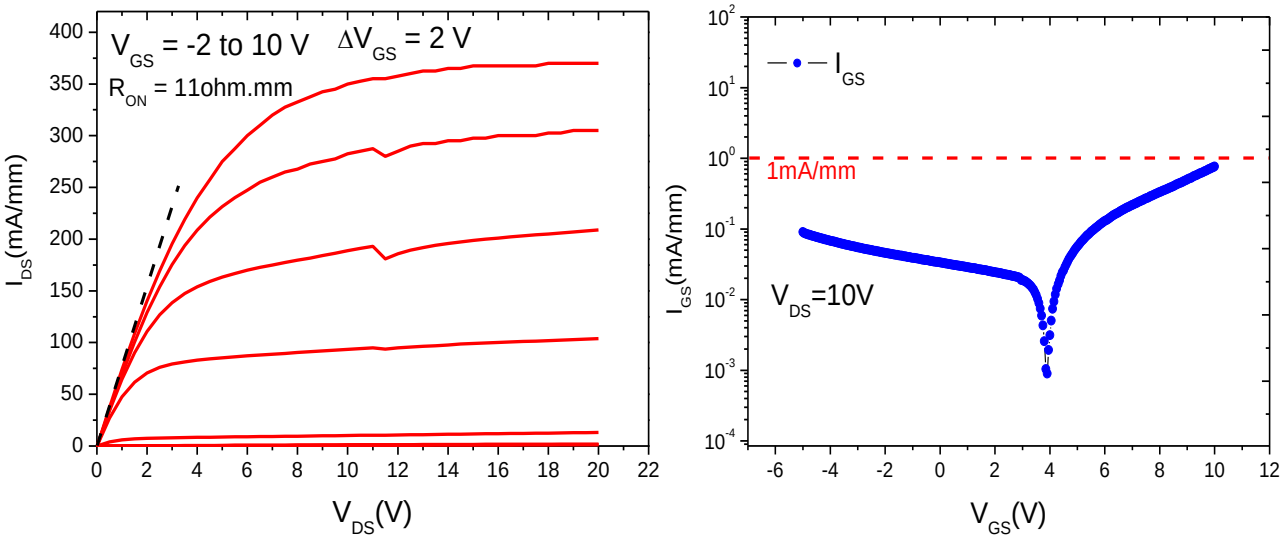


Figure 5.10 (a) IV characteristics of enhancement mode AlGaN/GaN MISHFETs (15nm SiN) (b) Gate transfer characteristics showing gate leakage. (The wafer characteristics are $n_s = 1 \times 10^{13} cm^{-2}$, d = 28nm, $\mu_n = 991\ cm^{-2}V^{-1}s^{-1}$ and $R_s = 400\ \Omega/sq$).

The IV characteristic of the enhancement mode transistor and the gate leakage current is shown in figure 5.10(a) and (b) respectively. The maximum drain current is 350mA/mm and the on-resistance (R_{ON}) is 11ohm.mm. It can be seen that the gate forward bias current is less than 1mA/mm (standard breakdown criteria in literature at that time) at 10V gate source bias

in figure 5.10(b) which suggests that the forward gate bias can be increased to 10V to facilitate more 2DEG drain current.

Equation 5.11 predicts that an increase in the dielectric layer thickness will increase the threshold voltage towards positive direction (if fluorine concentration is sufficient to induce a positive shift in first place) for the enhancement mode devices. The gate transfer characteristics of the fluorine treated enhancement mode MISHFETs with 10nm and 20nm PECVD SiN_x layer is shown in figures 5.11(a) and (b) respectively. As expected, the threshold voltage is increased with 20nm SiN_x to +3.1V compared to +2V with 10nm SiN_x layer. The peak transconductance value with 10nm SiN_x is 75mS/mm and reduces to 65mS/mm with 20nm SiN_x due to a reduction in the overall 2DEG channel to gate capacitance (barrier layer and dielectric/oxide capacitance). These results suggest that after optimum fluorine implant the threshold voltage can be further tuned to suit a particular requirement (e.g. +3V in power electronics applications) by choosing appropriate dielectric material (threshold voltage also dependent on dielectric constant) and thickness of the dielectric layer.

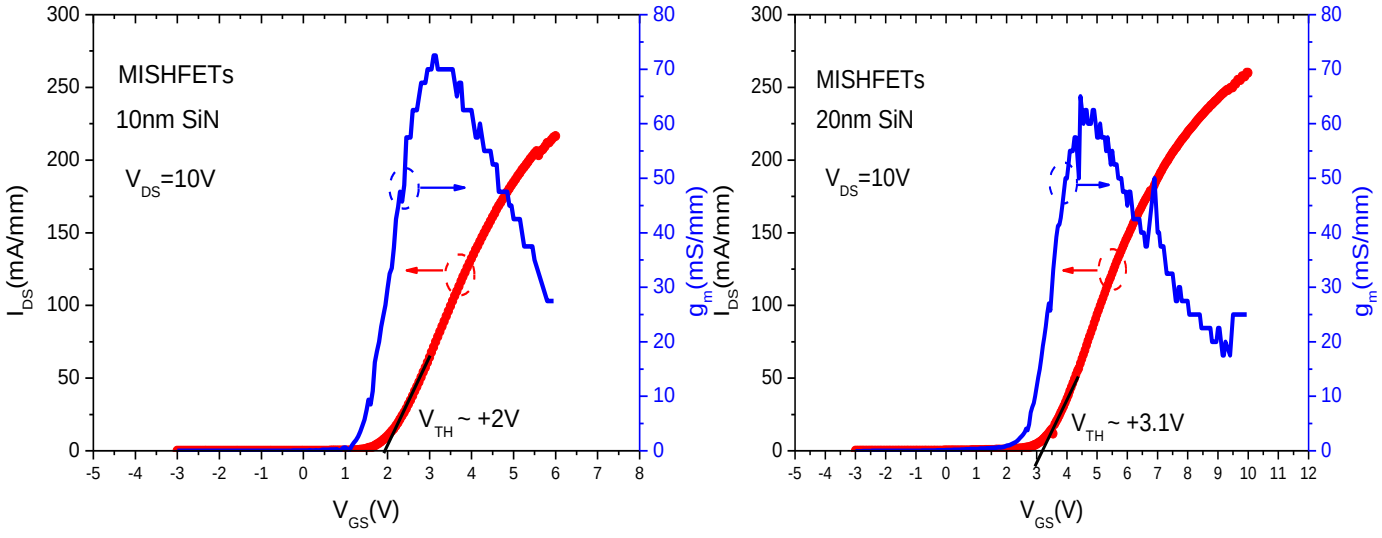


Figure 5.11 Gate transfer characteristics of enhancement mode AlGaN/GaN MISHFETs (a) with 15nm SiN) (b) with 20nm SiN layer. (The wafer characteristics are $n_s = 6.7 \times 10^{12} cm^{-2}$, d = 30nm, $\mu_n = 1773\ cm^{-2}V^{-1}s^{-1}$ and $R_s = 450\ \Omega/sq$).

5.7 Fluorine Implant in AlInN/GaN HFETs

In addition to interest in enhancement mode operation for power electronics switching applications, there is interest in developing normally-off GaN based HFETs for RF, logic and gate drive circuit applications because of simpler circuit configurations and reduced circuit size as well as enabling fail safe operation [15]. Since AlInN/GaN HFETs offers much higher 2DEG density owing to high spontaneous polarization, which translates to high drain current compared to conventional AlGaN/GaN HFETs, they are more favoured in RF applications due to lower R_{ON}. Additionally, stress free growth of the lattice matched AlInN barrier can potentially improve device reliability and a thin barrier offers high transconductance. Enhancement mode AlInN/GaN HFETs have also been realized using thin barriers [16] and recently, using a GaN/InAlN/GaN structure where the GaN cap reduces the 2DEG density [17]. However, devices with extremely thin barrier layer combinations may be difficult to reproduce uniformly across a wafer and from wafer to wafer. In this work, we have used fluorine plasma based implant to achieve normally-off operation in AlInN/GaN HFETs with high transconductance and drain current and compared it with conventional AlGaN/GaN HFETs.

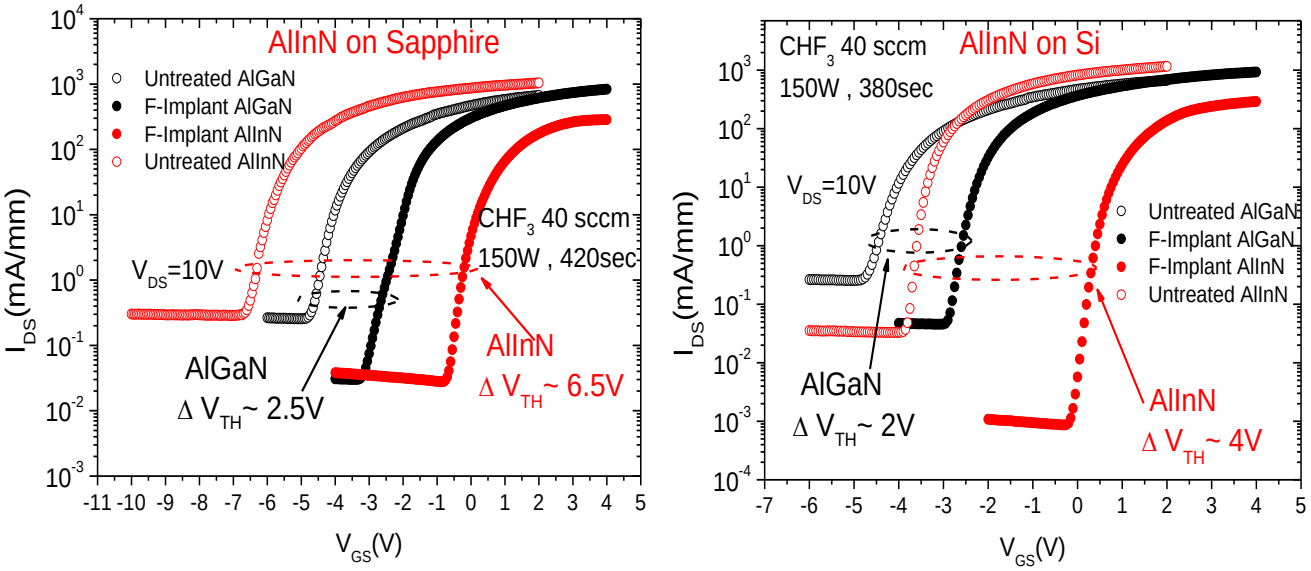


Figure 5.12 Gate transfer characteristics of fluorine Implant AlGaN/GaN and AlInN/GaN HFETs (a) AlInN/GaN on Sapphire substrate (b) on Silicon substrate. (The wafer characteristics for AlInN/GaN on Si are $n_s = 1.3 \times 10^{13}cm^{-2}$, d = 13nm, $\mu_n = 1717\ cm^{-2}V^{-1}s^{-1}$ and $R_s = 240\ \Omega/sq$ and for AlInN/GaN on sapphire are $n_s = 1.02 \times 10^{13}cm^{-2}$, d = 13nm, $\mu_n = 1907\ cm^{-2}V^{-1}s^{-1}$ and $R_s = 270\ \Omega/sq$).

The gate transfer characteristics of the fluorine implanted AlGaN/GaN and AlInN/GaN HFETs on sapphire and Si substrate are shown in figure 5.12(a) and (b) respectively. In both the cases, the samples were processed with similar fluorine exposure conditions, including RF plasma power and exposure time in the same chamber (ICP). Despite having a higher 2DEG concentration, a much larger positive threshold voltage shift (~+6.5V on sapphire and ~+4V on Si) is observed in the AlInN/GaN structure compared to the more conventional AlGaN/GaN HFETs (~+2.5V on sapphire and ~+2V on Si). The larger shift in AlInN/GaN HFETs is consistent across various other wafers processed in this work. The positive shift in AlInN/GaN HFETs confirms the fact that fluorine possesses similar chemistry (acceptor like deep level) as in AlGaN. However, it is unclear why consistently a large positive shift is observed in AlInN/GaN HFETs, since electrostatically any fluorine charge penetrating deeper in the GaN buffer region should make no difference to charge neutrality (given the same dose of fluorine charge in both HFETs). A possible explanation can be due to unrecoverable plasma induced defects in the thin barrier (13nm) AlInN HFETs which somehow results in more efficient incorporation of fluorine ions.

After the fluorine implant underneath the gated region in the AlInN/GaN device, the sub-threshold slope (S.S.) is reduced in both sapphire and Si substrates (from 424 to 293 mV/decade on sapphire and 175 to 121 mV/decade on Si substrate) which results from a reduction in the interface trap charge density, D_{it}. Using the same equation 4.2 as in chapter 4 [18].

$$D_{it} = \left(\frac{S.S.}{\ln(10)} \times \frac{q}{kT} - 1\right)\frac{C}{q^2} \qquad [5.13]$$

where q is the electron charge, T is the absolute temperature in Kelvin, k is the Boltzmann constant and C is the gate capacitance per unit area. D_{it} was reduced from 2.87 to 1.84 × 10^{13} cm^2eV^{-1} on sapphire and 8.76 to 4.68 × 10^{12} cm^2eV^{-1} on Si substrate after the fluorine treatment. Comparable observations for the AlGaN/GaN HFET on Si result in a reduction from 13.8 to 6.44 × 10^{12} cm^2eV^{-1}.

The gate transfer characteristics and transconductance of both AlGaN/GaN HFETs and AlInN/GaN HFETs after exposure to the fluorine plasma at RF powers of 150 W with different exposure times are shown in figure 5.13. A systematic shift in the gate threshold voltage is observed with an increase in exposure time to fluorine plasma, consistent with

increased fluorine dosage. After the plasma exposure, samples are annealed at 500 ^{o}C for 5 minutes to recover from any plasma induced defects.

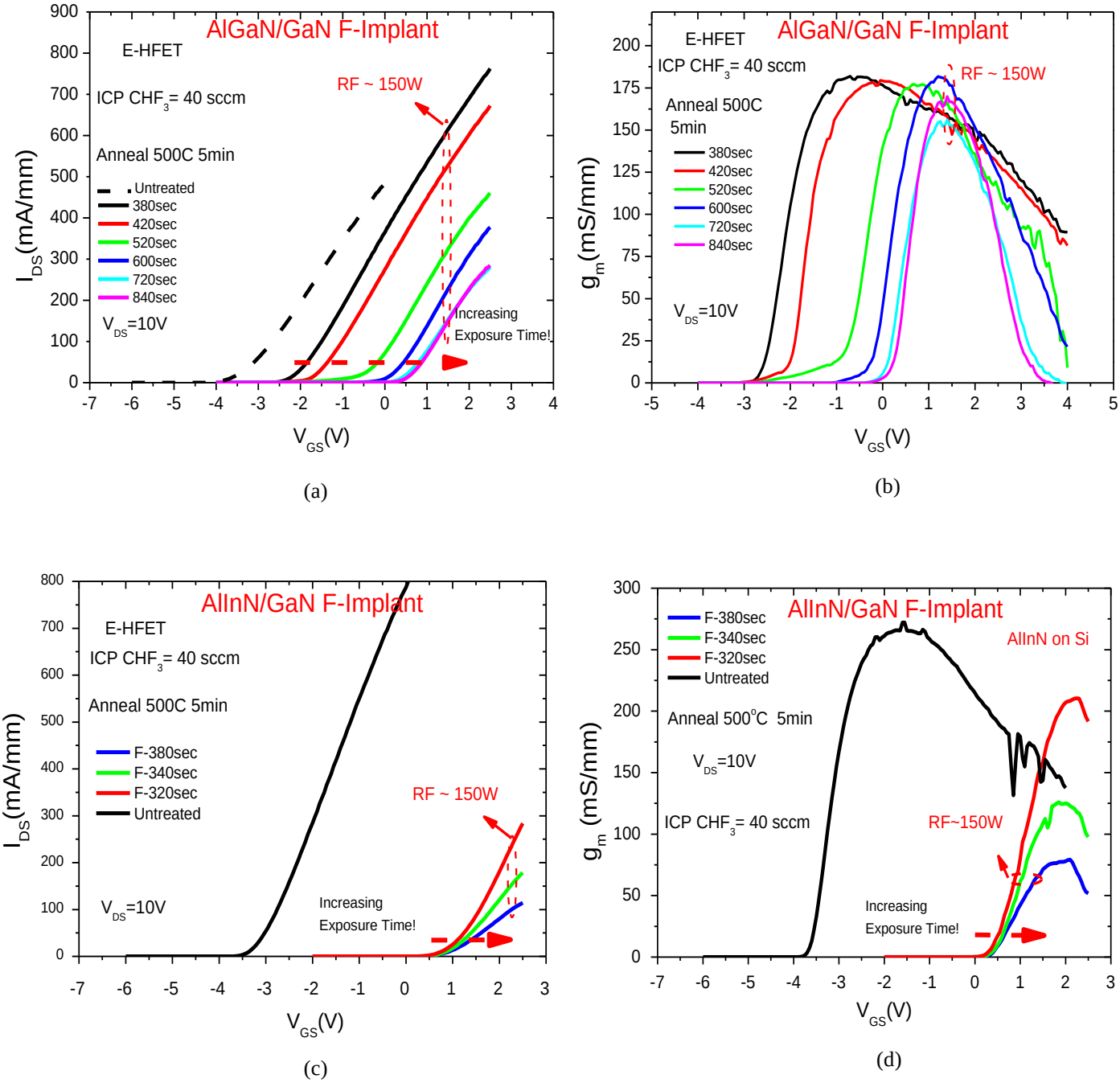


Figure 5.13 Gate transfer characteristics of fluorine Implant AlGaN/GaN HFETs (RF power 150W) with different exposure times (b) corresponding AlGaN/GaN HFETs transconductance (c) Gate transfer characteristics of fluorine Implant AlInN/GaN HFETs (RF power 150W) with different exposure times (d) corresponding AlInN/GaN HFETs transconductance. (The wafer characteristics for AlInN/GaN are $n_s = 1.3 \times 10^{13}cm^{-2}$, d = 13nm, $\mu_n = 1717\ cm^{-2}V^{-1}s^{-1}$ and $R_s = 240\ \Omega$/sq and for AlGaN/GaN are $n_s = 6.7 \times 10^{12}cm^{-2}$, d = 30nm, $\mu_n = 1773\ cm^{-2}V^{-1}s^{-1}$ and $R_s = 450\ \Omega$/sq).

As mentioned before, annealing at 500^0C for 5 minutes is much more effective in recovering the transconductance (degraded due to plasma defects) than 400^0C for 10 minutes. It can be seen from figure 5.13(b) that in AlGaN/GaN HFETs, the peak transconductance is almost fully recovered (150mS~160mS/mm) to the depletion mode device level after annealing. However, in contrast, for AlInN/GaN HFETs the transconductance is not fully recoverable even after annealing to 500^0C for 5 minutes. The degradation in transconductance indicates that fluorine ions have penetrated significantly beyond the 2DEG (see figure 5.14) in thin barrier AlInN/GaN HFETs, adversely affecting the channel mobility. In this case the mobility is not recoverable by annealing.

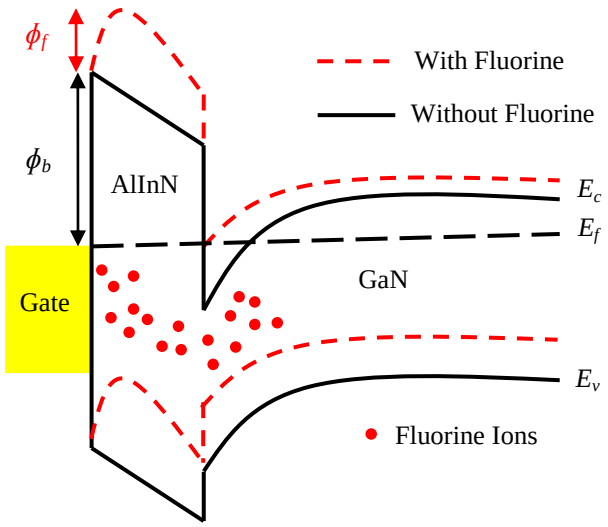


Figure 5.14 AlInN/GaN heterostructure band diagram showing deeper penetration of fluorine ions into GaN buffer region at RF power of 150W.

After the fluorine implant, one additional advantage is the increase in the effective Schottky barrier height ($\phi_b + \phi_{fb}$) which results in reduced gate leakage current as with AlGaN/GaN HFETs. The AlInN HFETs often suffer from high gate leakage currents due to the thin barrier layer and strong polarization electric fields, therefore fluorine implant can be helpful to reduce gate leakage. The observed reduction in gate leakage was more significant for devices with high gate leakage. A systematic reduction in gate leakage current with increase in fluorine plasma exposure at RF power of 150W was observed for devices suffering from a high gate leakage current as shown in figure 5.15.

In order to control the fluorine ion penetration in AlInN/GaN HFETs, the RF plasma power was reduced to 75W and exposure time was increased for optimized enhancement mode

operation. The gate transfer and transconductance characteristics are shown in figure 5.16 (a) and (b) respectively.

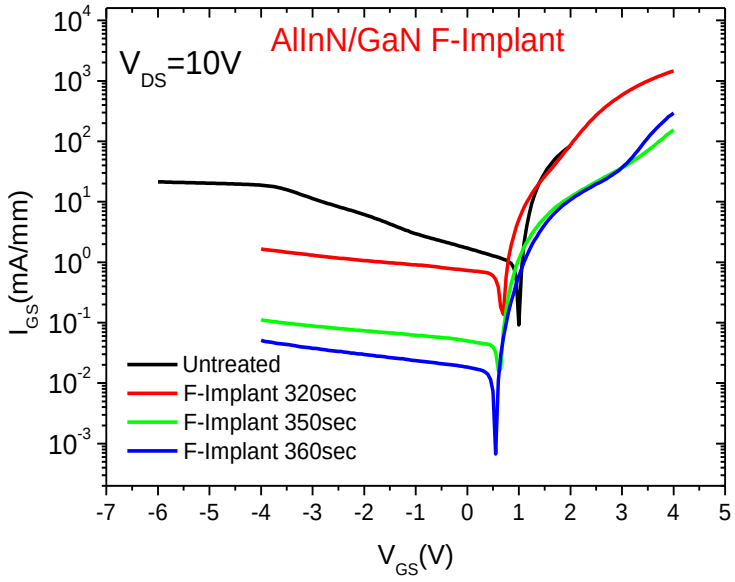
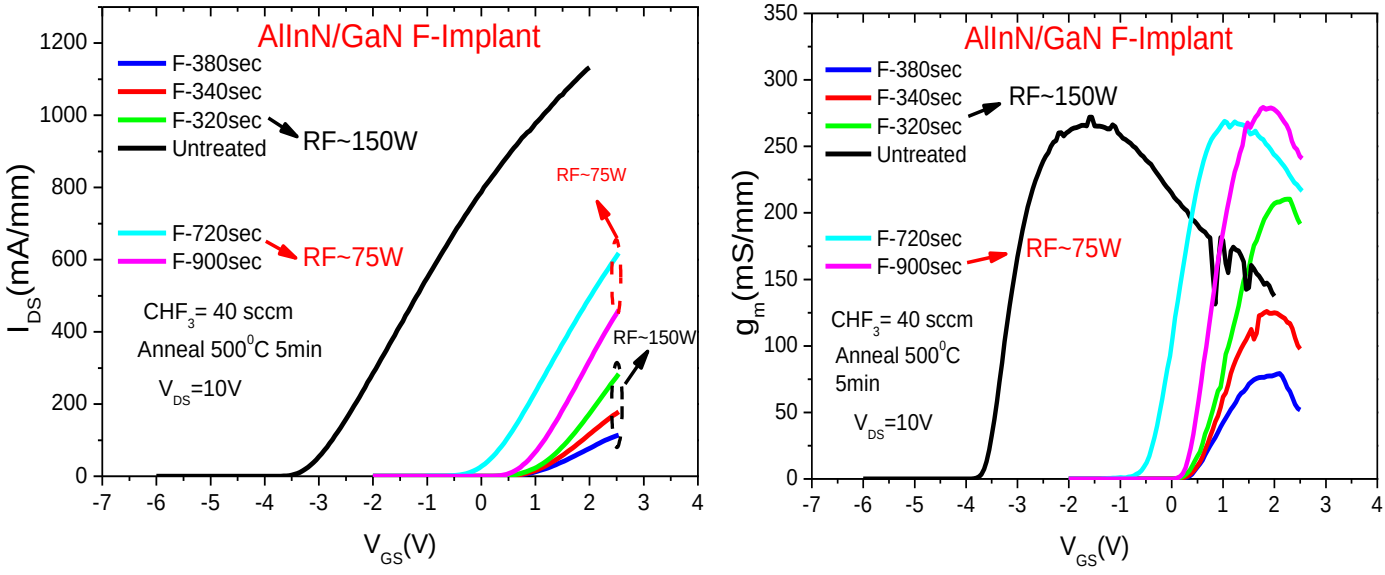


Figure: 5.15 AlInN/GaN HFET gate leakage current reductions after fluorine implant with different exposure times at RF power of 150W. (The wafer characteristics for AlInN/GaN are $n_s = 8.8 \times 10^{12}cm^{-2}$, d = 12nm, $\mu_n = 1413\ cm^{-2}V^{-1}s^{-1}$ and $R_s = 330\ \Omega/sq$).



(a) (b)

Figure 5.16 Gate transfer characteristics of fluorine Implant AlInN/GaN HFETs at high RF (150W) and low RF (75W) power with different exposure times (b) corresponding AlInN/GaN HFETs transconductance. (The wafer characteristics for AlInN/GaN are $n_s = 1.3 \times 10^{13}cm^{-2}$, d = 13nm, $\mu_n = 1717\ cm^{-2}V^{-1}s^{-1}$ and $R_s = 240\ \Omega/sq$).

It can be seen that with low RF power (75W) the drain current is drastically improved and transconductance can be fully recovered to depletion mode device level (~275mS/mm) after annealing at 500^0C for 5 minutes.

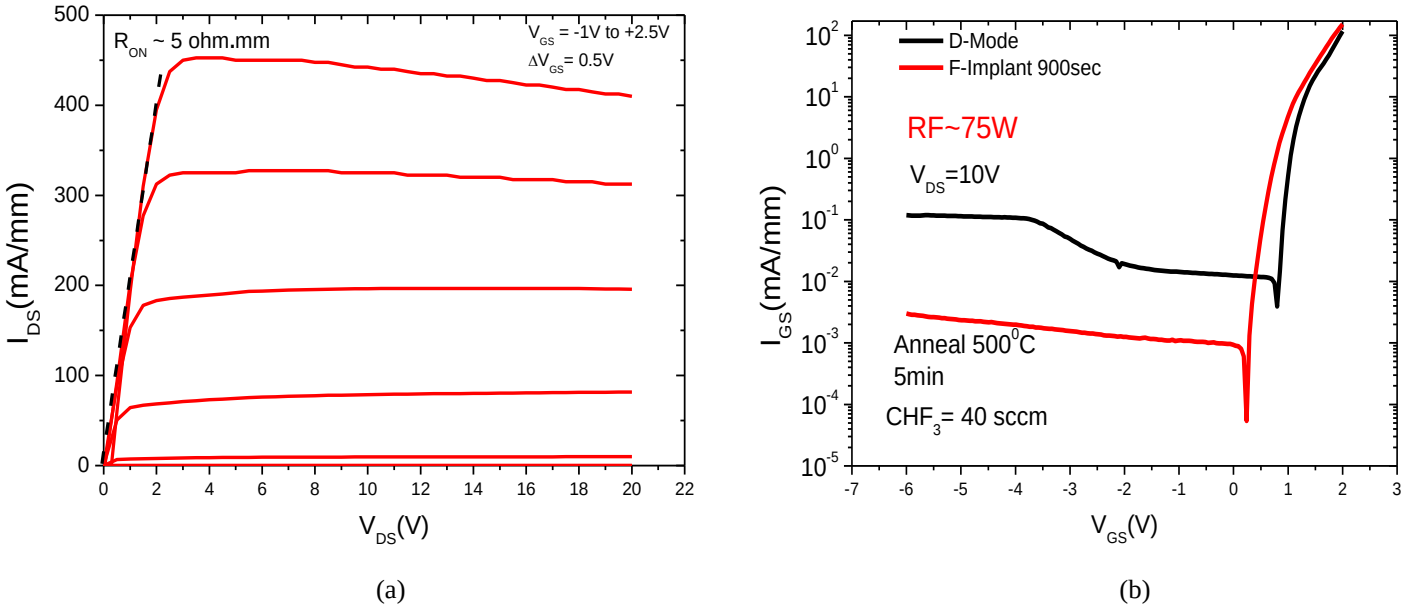


Figure 5.17 (a) IV characteristics of fluorine Implant AlInN/GaN HFETs at low RF (75W) power (b) gate leakage current after fluorine implant in AlInN/GaN HFETs.

Overall, excellent IV characteristics are obtained after the fluorine implant at low RF (75W). R_{ON} is 5ohms.mm (figure 5.17(a)) and gate leakage current is reduced by more than one order of magnitude as shown in figure 5.17(b).

After the fluorine implant, it is possible to achieve a higher threshold voltage (~+3V), again consistent with AlGaN/GaN HFETs by using a MISHFET structure. The gate transfer characteristics and transconductance after deposition of 25nm of SiN_x under the gate is shown in figure 5.18(a). A high positive threshold voltage of +3V is achieved. The peak transconductance is reduced to 65mS/mm, due to increase in the overall gate to channel distance. However, the MIS structure combined with the high barrier due to the fluorine space charge, allows an increase in forward gate voltage swing to +15V (shown in figure 5.18(b)), producing a maximum drain current of 540 mA/mm.

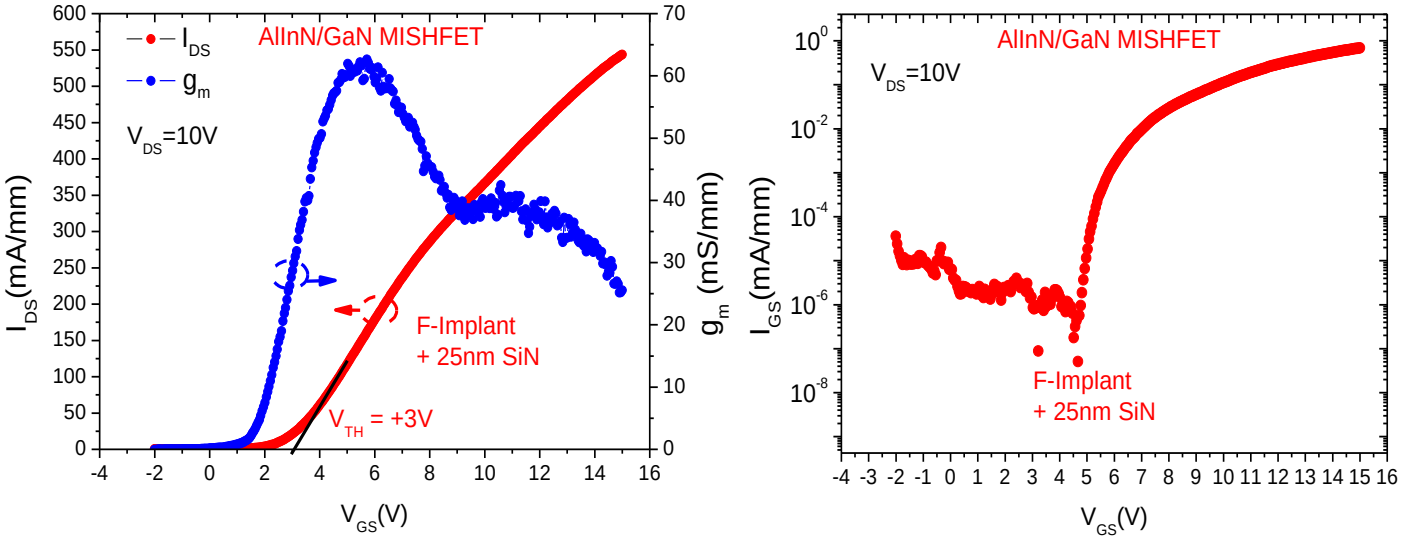


Figure 5.18 (a) AlInN/GaN (MISHFET) gate transfer and transconductance plot with fluorine implant and 25nm SiN dielectric layer between metal and AlInN barrier (b) MISHFET gate leakage current.

5.7.1 Temperature dependent IV measurements in AlInN/GaN HFETs

In order to analyze the thermal stability of threshold voltage and gate leakage in AlInN/GaN HFETs after 75W fluorine plasma exposure, gate transfer characteristics were performed at higher temperatures (up to 200^0C) and threshold voltage (defined by 1mA/mm) variation along with gate leakage current is plotted against temperature for both depletion mode and enhancement mode devices in figure 5.19.

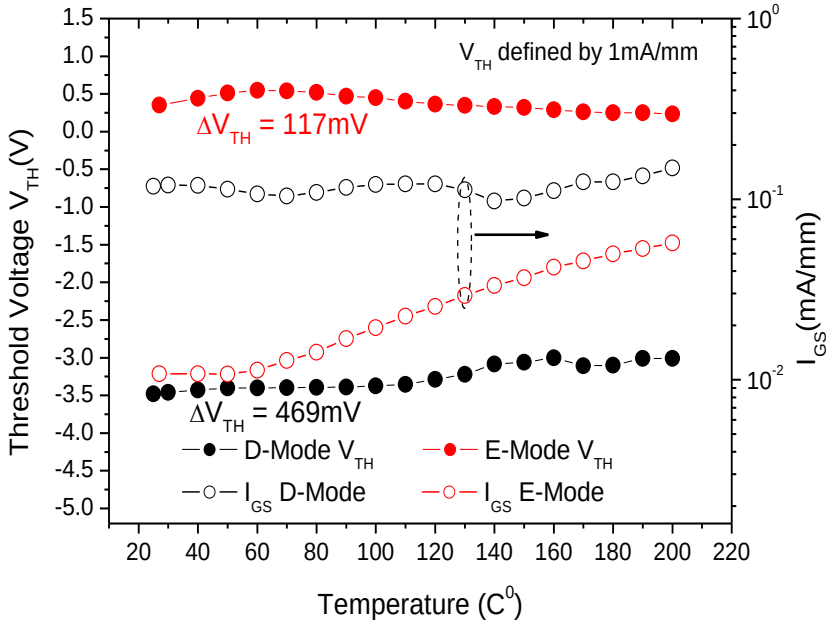


Figure 5.19 Threshold voltage and gate current variation with temperature for both depletion mode and enhancement mode (after fluorine implant at 75W) AlInN/GaN HFET.

It can be seen that in the fluorine treated device a negligible deviation of 117mV in the threshold voltage is observed at 200^0C from room temperature. This deviation in threshold voltage is much less than the depletion mode device (469mV) fabricated on the same wafer. The gate leakage current is slightly increased in the fluorine treated device with an increase in temperature whereas in the depletion mode device it is almost constant. Interestingly, in the depletion mode device the shift in the threshold voltage (+469mV) with temperature is positive which is in contrast to the fluorine treated device where a negative shift (-117mV) is seen. These results indicate that different mechanisms are involved for the threshold voltage drift in both depletion mode and the fluorine treated device. In order to understand the mechanism further, we did temperature dependent Schottky diode leakage measurements and the Arrhenious plot is shown in figure 5.20.

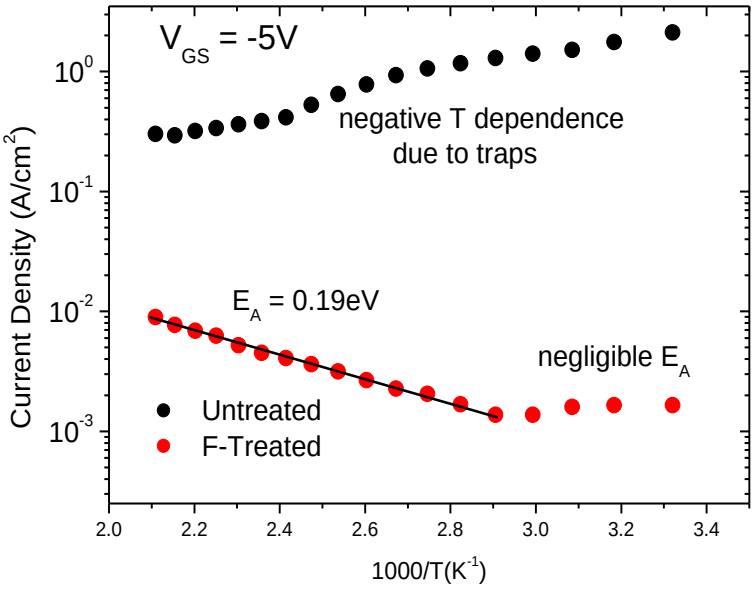


Figure 5.20 Arhenious plot of Schottky diode leakage current in untreated and fluorine treated AlInN/GaN HFET.

In the untreated diode, a negative temperature dependence is observed which is contrary to the fluorine treated diode which has a positive temperature dependence with a small activation energy (E_a ~0.2eV) in most of the temperature region. To ensure the activation energy in the fluorine treated diode is not a contribution from gate surface leakage component which was previously measured with a similar activation energy, measurements were

performed on a surface leakage test structure (figure 4.4(b) in Chapter 4) in order to subtract any surface leakage component, and almost identical behaviour was observed as shown in figure 5.21.

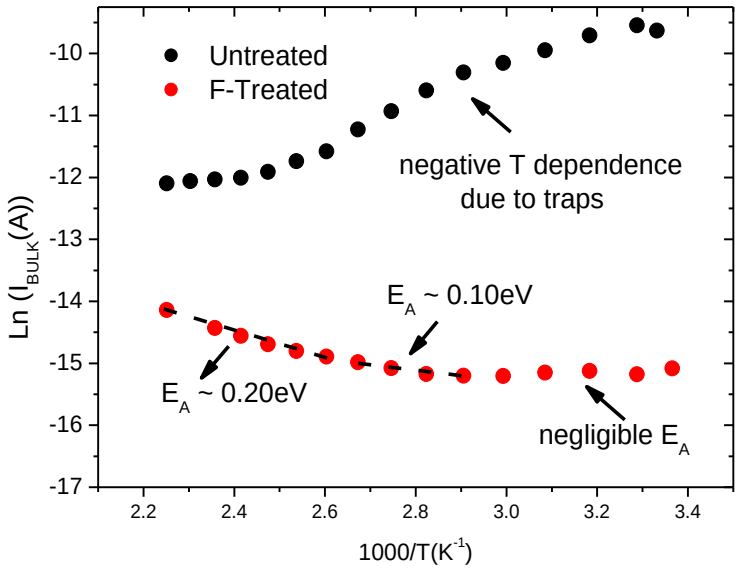


Figure 5.21 Arhenious plot of gate bulk leakage current extracted from surface leakage test structure in untreated and fluorine treated AlInN/GaN HFET.

In the literature, a negative temperature dependence of gate leakage current with positive shift in the threshold voltage is often explained by the impact ionization model in AlGaN/GaN HFETs [19]. However, in our study the Schottky diode had long gate widths, and applied voltages were restricted which makes impact ionization very unlikely. Therefore, in order to explain the negative temperature dependence in the untreated AlInN/GaN Schottky diodes, a donor like subsurface trap model is considered which was first demonstrated by R. Green et al [20] to explain a similar effect in AlGaN/GaN HFETs.

Considering that traps are located at a range of energy levels near the AlInN subsurface, the conduction band diagram of AlInN/GaN HFET in the presence of traps is shown in figure 5.22. In the reverse bias state, these traps will be able to capture electrons which will reduce or moderate the electric field in the AlInN barrier. The electron leakage mechanism is via trap assisted tunneling. More electrons will be able to access these traps with an increase in temperature and gate leakage current can be reduced due to a reduced electric field in the AlInN barrier. The presence of negative charge in the AlInN barrier also causes a reduction in

2DEG density which is reflected in a positive shift of threshold voltage with increased temperature.

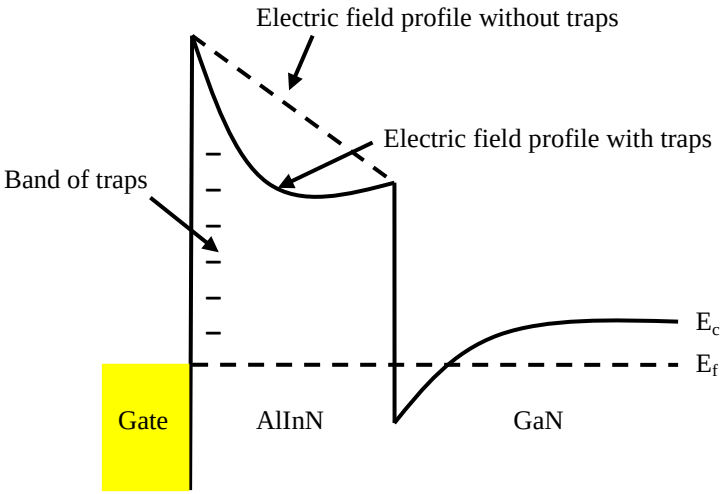


Figure 5.22 Modified conduction band diagram of AlInN/GaN HFET in presense of donor like subsurface AlInN traps.

After the fluorine implant in AlInN barrier, these subsurface traps are significantly reduced, which is consistent with a reduction in the measured interface trap charge density (D_{it}) and reflected by a positive temperature dependence of leakage current. These results suggest that fluorine improves the threshold voltage stability of AlInN/GaN HFETs by neutralizing traps in the barrier region.

5.8 Charge Trapping Effects in E-MISHFETs

Although inserting a dielectric/oxide layer between the barrier (AlGaN) and the gate metal can significantly suppress the Schottky gate leakage and thereby increase the gate voltage swing capability of the device to favour high currents, it also introduces charge states at the interface between the dielectric and the barrier layer [21]. Unlike the depletion mode devices, in the (fluorine treated) enhancement mode devices the gate is driven to high positive voltages (typically ~ +6 to +10V) to increase the 2DEG charge accumulation and drain current. Therefore, under high forward gate bias conditions electrons are likely to spill over from the 2DEG channel into the interface trap states (real space charge transfer), resulting in charge trapping effects as illustrated in figure 5.23. This phenomenon can adversely affect the threshold voltage (V_{TH}) stability in AlGaN/GaN MISHFETs and recent literature [21-22]

suggests that even state-of-the-art GaN devices suffer from V_{TH} instability at high forward gate bias conditions.

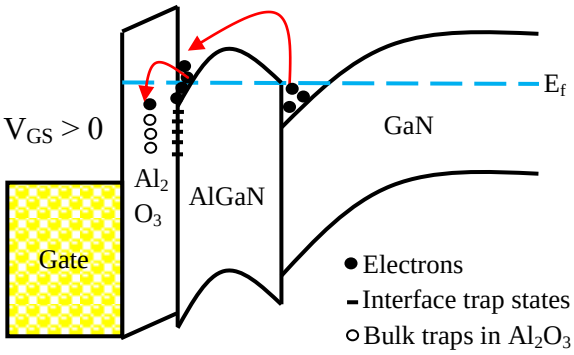


Figure 5.23 E-mode AlGaN/GaN MISHFET heterostructure under high forward bias condition showing real space charge transfer.

Figure 5.24(a) shows the gate transfer characteristics of the fluorine treated (E-mode AlGaN/GaN MISHFET) device with 20nm of Al_2O_3, deposited using an atomic layer deposition technique (at the University of Liverpool). The drain-source bias is held at +10V and the gate-source voltage is swept first from -6V to +10V (upward sweep) and then straight afterwards from +10V to -6V (downward sweep). A significant hysteresis (~3V) is observed in the double sweep and is believed to be caused by the electrons getting trapped in the interface (between Al_2O_3 and the AlGaN barrier) and bulk traps in the Al_2O_3 dielectric layer as shown previously in figure 5.23.

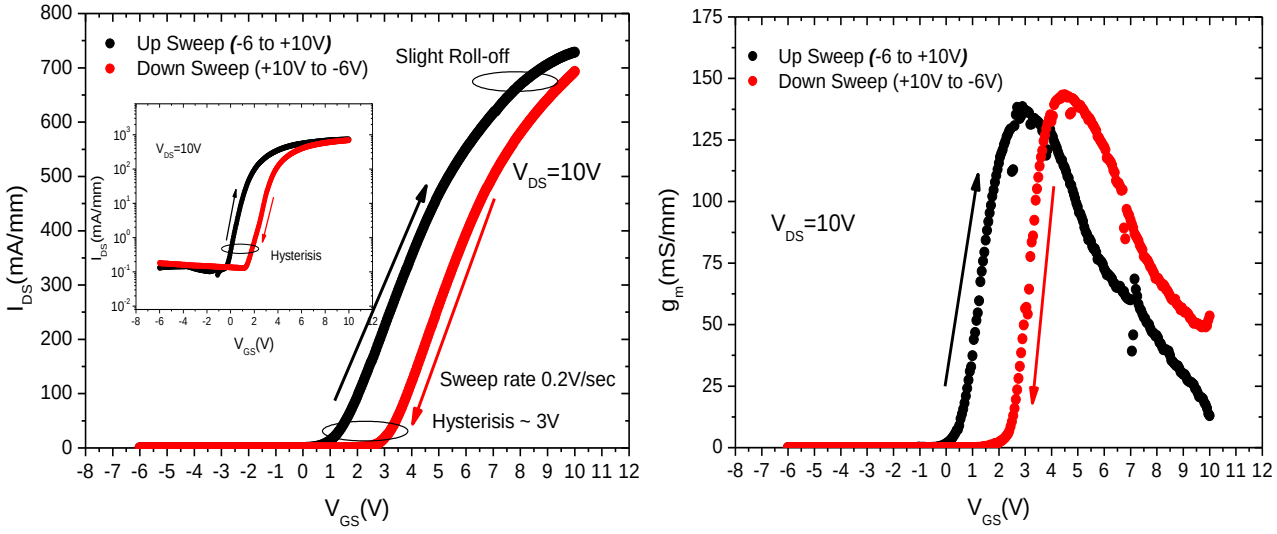


Figure 5.24 (a) Gate transfer characteristics of E-mode AlGaN/GaN MISHFETs with double sweep (inset shows the same figure in semi-log scale) (b) Transconductance of AlGaN/GaN MISHFETs in double sweep. (The wafer characteristics are $n_s = 6.7 \times 10^{12}cm^{-2}$, d = 30nm, $\mu_n = 1773\ cm^{-2}V^{-1}s^{-1}$ and $R_s = 450\ \Omega/sq$)

In the negative to positive gate sweep scenario (where the gate is swept from -6V to +10V) as the gate bias becomes more and more positive, electrons from the 2DEG channel jump over the bump caused by fluorine ions in the AlGaN conduction band into the interface states between Al_2O_3 and the AlGaN barrier layer (figure 5.23). This transfer of (electron) charge over the barrier reduces the ability of the gate at high forward gate bias to control the channel charge in the 2DEG. The loss of gate control is reflected in both roll-off of drain current in figure 5.24(a) and the drastic (more than usual) collapse of transconductance in figure 5.24(b) (black curve, at the high forward gate bias voltages).

When the gate is swept from positive to negative bias (+10V to -6V), electrons trapped in the interface states starts to de-trap. However, not all the trapped electrons can be de-trapped during the bias cycle (particularly those with slow de-trapping time constants) and negatively charged trapped electrons above the 2DEG channel result in enhanced channel depletion indicated by the higher positive threshold voltage (figure 5.24(a)). Also if there are traps inside the Al_2O_3 layer then electrons could eventually move into them once the interface states traps are full, and these bulk traps could be associated with the much slower de-trapping time constants.

It is observed that a negligible hysteresis is observed when the gate is swept several times from the negative to positive voltage (-6V to +10V) as shown in figure 5.25. However, when the gate bias starts from a positive voltage (+10V) and is swept towards a negative voltage, a significant drift is seen in the threshold voltage (figure 5.25 run7 to run 12). After six positive to negative sweeps (+10V to -6V) when the gate is swept again from the negative to positive voltage (-6V to +10V) (run 13 in figure 5.25) the threshold voltage somewhat recovers towards the initial value. These results suggests that the initial application of a large positive gate bias (+10V) is more critical for threshold voltage instability and negative gate bias (-6V) at the starting point of sweeps (-6V to +10V) is more efficient in de-trapping charge to suppress hysteresis. In other words, a large vertical electric field supported by the negative gate bias helps to recover or de-trap charge. Another observation is the build up of positive threshold voltage with the increase in the magnitude of positive gate bias, suggesting that larger positive gate bias encourages more electrons to get trapped and consequently results in higher positive threshold voltage due to enhanced channel depletion.

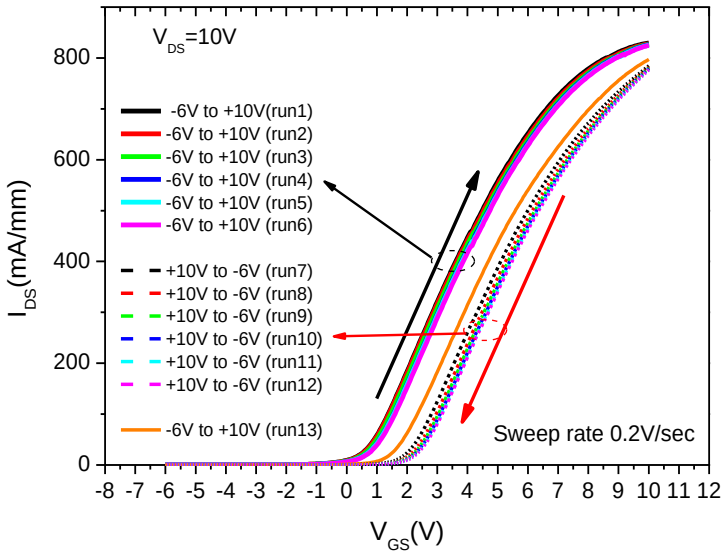


Figure 5.25 Gate transfer characteristics of E-MISHFET (ALD Al_2O_3~20nm) with several negative to positive and positive to negative gate sweep.

Forming gas anneal (FGA) is reported to be effective in reducing the oxide/dielectric and semiconductor interface traps to address threshold voltage stability in MOSFETs [22], but in our case no significant improvement is seen after the FGA treatment (10% H, 90%N) at 430^0C for 30 minutes (performed at University of Liverpool).

Recently, it has been reported that hysteresis in AlGaN/GaN MISHFETs is a strong function of dielectric layer material, thickness and the dielectric layer constant [23]. In this work, a significant hysteresis is observed with ALD (atomic layer deposition) Al_2O_3 MISHFETs (+2~3V) compared to PECVD SiN_x MISHFETs (~0.5-0.7V). In some fabricated MISHFETs with a PECVD SiN_x layer, almost no hysteresis in threshold voltage is observed, even with several positive to negative gate sweeps as shown in figure 5.26. However, the drain current curves tend to depart from each other at high gate bias. These results suggest that, compared to Al_2O_3 MISHFETs, much reduced traps, or traps with much faster time constants, are associated with SiN_x MISHFETs. Although this sample showed better results for PECVD SiN_x layer, this result was not consistent, indicating that tight control over the AlGaN barrier surface and the deposition conditions are required for reproducible results.

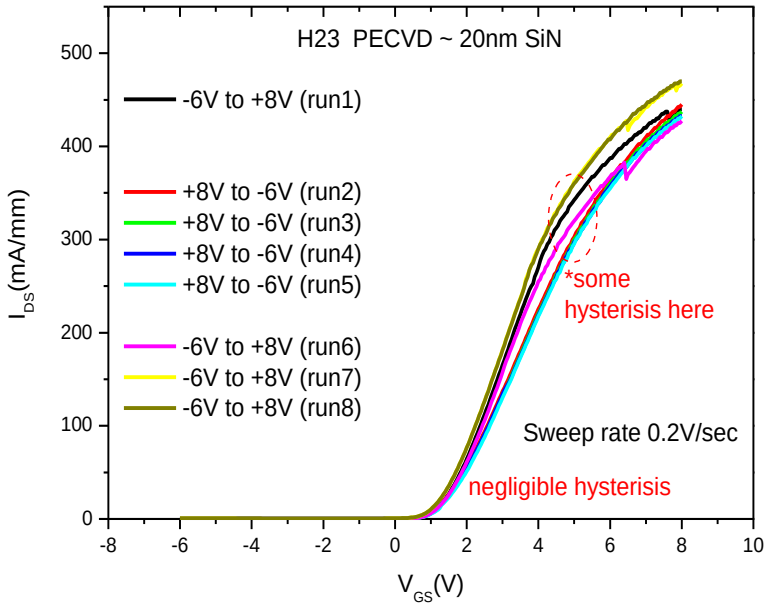


Figure 5.26 Gate transfer characteristics of E-MISHFET (PECVD SiN~20nm) with several negative to positive and positive to negative gate sweep.

5.9 Conclusion

In this chapter, the fluorine implant technique is used to achieve enhancement mode operation in GaN HFETs. The fluorine recipe is optimized for enhancement mode operation with maximum output drain current. The dielectric layer deposition after optimum fluorine implant is helpful to achieve a higher positive threshold voltage which can offer better immunity against electromagnetic interference. The expression for threshold voltage is derived using Guass's Law which explains the threshold voltage shift conditions after the dielectric layer deposition. In this work, we compared for the first time fluorine implant in AlInN and AlGaN barrier HFETs. In the thin barrier, AlInN/GaN HFETs, a much larger shift in threshold voltage is achieved with the same recipe of fluorine implant compared to AlGaN/GaN HFETs. A lower fluorine RF plasma power recipe is required for AlInN/GaN HFETs to maintain high transconductance and drain current suitable for RF applications. We have achieved a record high positive threshold voltage (+3V) in AlInN/GaN HFET combining fluorine implant and SiN_x dielectric layer. After the fluorine implant, the subsurface traps in AlInN barrier are reduced, reflected in better threshold voltage stability. The enhancement mode MISHFETs fabricated using Al_2O_3 showed large threshold voltage hysteresis in dual sweeps caused by interface traps. Therefore, for stable enhancement mode operation tight control over the semiconductor surface and dielectric deposition conditions is required.

5.9 References

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Chapter No: 6 Conclusions and Future Work

6.1 Summary and Conclusions

In this work, we have studied GaN HFETs for applications in UV detection and the power electronics sector. In chapter 3, UV light detection mechanism in AlGaN/GaN HFETs is decribed. The AlGaN/GaN HFETs can offer very high sensitivity to UV light and are able to detect very low UV power levels (10^{-10} W) with very high response (~10^{7} A/W). Such high response to UV light makes the AlGaN/GaN HFET a very attractive candidate for detecting tiny UV light radiation intensities. Optimized GaN HFET detectors can find wide applications in military and commercial areas, such as flame monitoring, missile plume detection, UV environmental monitoring, space ozone monitoring, imaging arrays and others. The UV absorption mechanism in AlGaN/GaN HFET fabricated on sapphire substrate is explained in both the barrier (AlGaN) and the buffer (GaN) layers independently. The optical gain in the device is due to the formation of a photo voltage effect between the surface and the channel (AlGaN barrier) and the buffer/substrate and the channel (GaN buffer) regions, depending on where light absorption takes place. The intrinsic transistor action of the device is responsible for the change in 2DEG channel charge concentration as positive virtual gate biases are formed on either side of the 2DEG channel. The gain of the GaN buffer region dominates the barrier layer, owing to both enhanced holes lifetimes and it being a thicker region. Despite offering a high gain, HFETs suffer from a large dark current due to the presence of conductive 2DEG channel and slow speed of response.

For power electronics applications, GaN HFETs fabricated on Si substrate are characterized. The iron (Fe) and carbon (C) doped buffer HFETs are compared using buffer leakage and vertical leakage test structures. Compared to Fe, C doped HFET has proved to be more effective in depleting the GaN buffer and offers higher buffer (lateral) and vertical breakdown voltages. The vertical breakdown leakage mechanism in both the Fe and C doped HFETs was found to follow a Poole Frenkel emission process. Two activation energy levels were found by extrapolating the applied voltage to zero volts in C doped wafer, 0.9eV and 0.62eV. The 0.9eV level is consistent with C acceptor depth above the valence band and 0.62eV is possibly due to traps associated with dislocations. In the Fe doped wafer, one activation energy of 0.56eV is found which is close to the Fe acceptor level below the conduction band.

A novel method of using chemical treatments (H_2O_2 and H_2SO_4) was also developed to suppress the gate surface leakage current in GaN HFETs. In comparison with SiN_x passivation, both chemicals are more effective in suppressing the overall gate leakage current, reducing the sub-threshold slope and improving the on/off current ratios of the device. In a range of samples and devices studied in this work, sulphuric acid (H_2SO_4) has proved to be more effective in suppressing gate leakage current. The reduction in gate leakage is due to the strong surface oxidation process. Experimental results suggest an effective gate edge passivation effect, where the electric field is highest under normal device operation. The interface trap charge density (D_{it}) is significantly reduced when calculated from the change in the device sub-threshold slope. However, when temperature dependent IV measurements were performed on the surface leakage current, it was found that deep trap levels (0.68eV) are introduced after H_2SO_2 treatment. These traps reduce the overall effectiveness of H_2SO_2 treatment since they introduce charge trapping effects (current collapse). Therefore, for an optimized passivation, a combination of H_2SO_2 treatment and SiN_x passivation offers both low current collapse and reduced gate leakage current. The gate surface leakage mechanism was also described and explained by a combination of Mott hopping and Poole Frenkel emission based models.

Enhancement mode AlGaN/GaN HFETs fabricated using a fluorine implant based process are presented in chapter 5. The devices were optimized for fluorine plasma exposure and thermal annealing afterwards to recover from plasma induced defects and to offer enhancement mode operation with high transconductance. A threshold voltage expression based on Gauss's Law was developed to explain the shift in enhancement mode HFETs. The influence of a dielectric/oxide layer on the threshold voltage is also described to attain higher positive (~+3V) threshold voltage. Devices with +3V threshold voltage are demonstrated for power electronics applications. Fluorine implant in AlInN/GaN HFETs was also carried out and compared with conventional AlGaN/GaN HFETs. The thin barrier AlInN HFETs were found to be more sensitive to fluorine ions and gave a larger positive shift in threshold voltage. A low fluorine plasma power (75W) based recipe was optimized for AlInN/GaN HFETs to offer high transconductance and drain current. Enhancement mode AlInN/GaN HFETs can be employed in RF applications without compromising the high transconductance. Finally, charge trapping effects due to real space charge transfer in enhancement mode MISHFETs which results in threshold voltage hysteresis and instability is explained.

6.2 Recommendations for Future Work

1. AlGaN/GaN HFETs have demonstrated very high responsivity (~10^7A/W) to UV light. However, due to the presence of an intrinsic AlGaN barrier layer, 2DEG channel charge is present which results in a very high dark current level. In other words, the photo current to dark current ratio is very small which makes absolute intensity detection difficult. However, it is possible to operate the transistor in the pinch-off state to reduce the dark current level to few nano Amperes but gain (photo response) is limited due to the collapse of the transconductance. Therefore, to realize transistors with low dark current levels, enhancement mode transistors need to be employed. The fluorine implant based transistor gives even higher gain to UV light but they are not suitable because of the persistent photoconductivity effect and time delay associated with traping effects. The enhancement mode transistor fabricated with dry recess etch techniques may also not be desirable due to plasma induced defects which can again limit the speed of response. The growth of a thin barrier layer (~4-8nm) can be a suitable alternative to reduce dark current level since the device would be inherently normally-off. Similarly, p-type GaN cap layer normally-off devices can be attractive to consider for UV detection.

2. To enhance the gain of the UV detector device it is important to increase the active absorption region of the device. The trade-off in making a very thick device is the delay time associated with the carrier transit time, but since these devices would be used for UV detection and not in optical communication systems, high sensitivity is still more desirable than fast speed of response. In AlGaN/GaN HFETs where surface states can be a serious issue, the gate leakage along the surface of large area devices needs to be increased to neutralize holes (generated when barrier region is excited) for optimized gain to delay ratio. Therefore, large area devices are prone to giving longer delay times and are not recommended. Instead, HFET devices or diodes can be designed such that the lateral distance between gate and surface region (towards drain and source) is constant (small) and the device width can be enhanced to give a larger absorption region. Additionally, small devices can also be combined in an array to offer high gain with respectable delay time.

3. Even though AlGaN/GaN HFETs are three terminal devices and may not be suitable for ultimate UV photo detector applications due to additional requirements of power supply, UV detection based on HFETs gives a useful insight into the gain mechanism involved and 2DEG based two terminal photodiodes (Schottky diodes) can be constructed for a better device performance. Optimized AlGaN/GaN photo detectors can be fabricated on the same wafer (with similar growth layers structure) as HFETs, allowing integration with a more mature technology.

4. In power switching applications, the breakdown voltage in large gate-drain spaced devices (20µm) fabricated on carbon doped wafers (in this project) is restricted to below 400V for 1µA/mm threshold for breakdown. The dominant leakage current is the drain to substrate leakage and only in thick wafers (7.2µm) were we able to achieve 600V breakdown voltage (1µA/mm). Therefore, it is necessary to grow highly insulating and thick buffer structures to support a high blocking voltage. Carbon has proved to be much more effective in suppressing the buffer leakage (both lateral and vertical) current. However, devices with deep acceptor levels are often susceptible to current collapse (buffer related) or high dynamic on resistance (R_{ON}). Therefore, an optimized buffer design needs to be constructed for better trade-off between breakdown and current collapse.

5. The chemical treatments presented in this thesis can form a very effective method of reducing gate surface leakage current. In this work, both H_2O_2 and H_2SO_4 treatments were performed at room temperature. In AlGaN/GaN HFETs, effective suppression in gate leakage current was observed after 48 hours. If the chemical treatment is performed at higher temperature it can be more effective and will save time. Therefore, it is important to optimize the gate leakage suppression with chemical treatment time (exposure time) at higher temperatures.

6. In AlInN/GaN HFETs chemical treatment was performed for shorter duration of time (~6 hours) and reduction in gate leakage current (~1µA/mm) was observed consistent with AlGaN/GaN HFETs. However, surface leakage mechanism in AlInN HFETs was not studied. It will be useful to study the surface conduction process in AlInN HFETs and then adopt chemical treatments for optimized leakage current and current collapse suppression. If deep level traps are also introduced in AlInN HFETs then

SiN_x passivation can be combined with chemical treatment similar to AlGaN/GaN HFETs for both low leakage and current collapse.

7. The enhancement mode devices studied in this work were based on fluorine ion implant. Fluorine treatment has proved to be quite effective and negligible hysteresis is observed in HFETs in double sweep gate transfer measurements. However, when the dielectric/oxide layer is inserted to form a MIS structure, a significant hysteresis (~0.5V) is observed. In the recent literature, almost all state-of-the-art enhancement mode GaN devices are suffering from some sort of hysteresis under high gate forward bias stress conditions (~+10V). The main culprit seems to be the interface traps between the dielectric and semiconductor layer where electrons get trapped. To improve the interface states before putting down the dielectric layer, we did try some chemical treatments (hydrochloric acid, nitric acid, potassium hydroxide and ammonia) but no significant benefit was observed. In future, it would be advantageous to do some surface nitridation (NH_3) with low plasma power to get rid of any oxygen bonds present on the surface. Additionally, the dielectric /oxide layer needs to be improved, since there may be a lot of bulk traps associated with a particular layer. The hysteresis observed with SiN_x dielectric layers is generally less than (ALD) Al_2O_3 layers. In future, different SiN_x layers reflected in different refractive index and plasma power can be tried to improve the threshold voltage variation with bias. In most enhancement mode devices, the dielectric/oxide layer is generally required to allow high gate forward bias and to increase the threshold voltage. However, the dielectric layers introduce interface traps. Recently, Panasonic [1] has demonstrated excellent stability with p-type GaN cap layer enhancement mode devices. Therefore, alternatively p-type grown cap structures can be developed for stable enhancement mode operation.

6.3 References

[1] Daisuke Ueda, et al, “GaN Power Electronics,” International Workshop on Nitride Semiconductors, Wroclaw, Poland, August, 2014.

Appendix A

Transmission Line Measurement Method

The transmission line method (TLM) was developed by H.H Berger in 1972 [1] and since then is very frequently used to measure the sheet resistance of the semiconductor film and the contact resistance of a particular metallization scheme. In the TLM test structure used in this work, a linear array of 5 ohmic contact pads with equal pad width but systematically increased spacing in between is fabricated as shown in figure A.1.

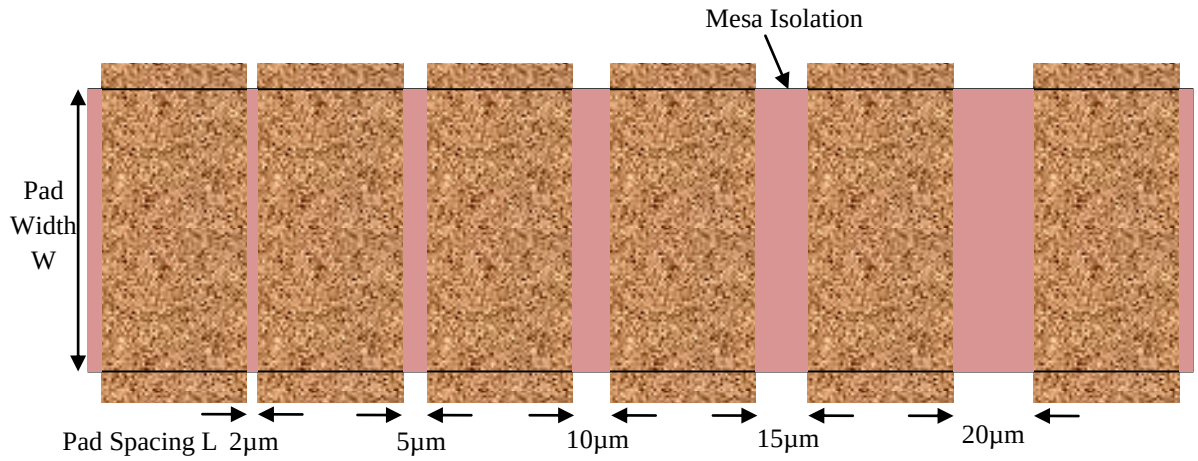

Figure A.1 The Test structure for a Linear Transmission line measurement.

In order to avoid the current spreading around the edges of contacts, a Mesa Isolation is done to etch through the 2DEG channel. The measurement is performed by forcing the current, I_P through the two adjacent pads and then the voltage, V_P across the same pad pair is measured. The measurement is repeated for all the 5 different pairs of pads with varying spacing L. It is assumed that the sheet resistance is uniform underneath and in between the pads, the total resistance R_T is given in equation A.1[2],

$$R_T = \frac{V_p}{I_P} = 2R_c + \frac{R_{sh}}{W} L \qquad [A.1]$$

whereas, R_c and R_{sh} are the metal contact and semiconductor sheet resistance respectively, W is the pad width and L is the pad or gap spacing. In this work, the pad width is constant ~ 125µm and the pad spacing is varied as 2µm, 5µm, 10µm, 15µm and 20µm.

The measured total resistance R_T for each pad pair can be plotted against the pad spacing L, which gives a linear straight line fit as shown in figure A.2

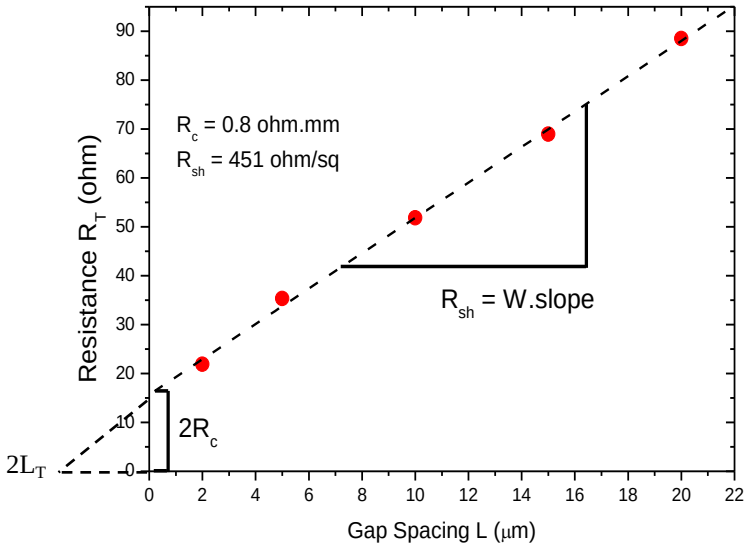

Figure A.2 Total resistance R_T plotted against the gap spacing L for all pads.

The contact resistance (R_c), sheet resistance (R_{sh}), specific contact resistivity (ρ_c) and transfer length (L_T) can be calculated as follows,

R_c = ½ y-axis intercept

R_{sh} = slope. W

$\rho_c = R^2_c \,.\, W^2/R_{sh}$

L_T = ½ x-axis intercept

The sheet resistance (R_{sh}) (units in ohm/sq) represent the resistance of the semiconductor (2DEG) between and underneath the pads. The contact resistance (R_c) is the resistance of the metal stacks and it is generally useful to measure it as Rc.W since it scales with the contact width (units in ohm.mm) which means contact resistance per mm of the pad width. The specific contact resistivity (ρ_c) is use to define the contact resistance in a unit area (units in $\Omega.cm^2$). Another important parameter is the transfer length (L_T) which denotes the amount of length current needs to travel in and out underneath the ohmic contact.

References

[1] H. H. Berger, "Models for contacts to planar devices", Solid-*State Electronics*, vol. 15, pp.145 -158, 1972.

[2] Dieter K. Schroder, "Semiconductor material and device characterization", third edition by John Wiley & Sons, 2006.

Appendix B

Hall Measurement Theory

Due to its simplicity and rapid turnover, the Hall Measurement is most frequently used in semiconductor research to extract the carrier concentration, material resistivity and carrier mobility. If a current (I_X) is flowing across a conductor placed in a magnetic field (B_Z) perpendicular to it, the resulting Lorentz force will create a build up of carrier's perpendicular to both magnetic field and current flow. This will give rise to a potential difference (V_H) and its equivalent electric field (E_H), which is more widely known as the Hall voltage and the Hall field.

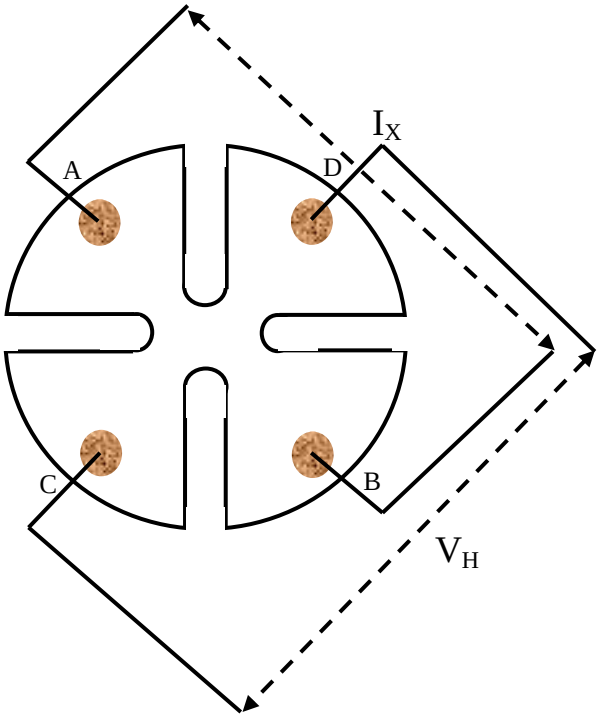

Figure B.1 The Hall measurement setup with current and voltage directions on clover leaf shaped sample.

The measurement setup of Hall measurement for clover leaf shaped sample is shown in figure B.1. The measured resistance $R_{AB,\,CD}$ is expressed as the ratio of voltage developed across terminals C and D, and current entering from terminals A and leaving from B.

$$R_{AB,\,CD} = V_{CD} / I_{AB} \qquad [B.1]$$

In a similar way resistance, $R_{BC, DA}$ is defined and the resistivity (ρ) of the material under no magnetic field is expressed as equation B.2 [1],

$$\rho = \frac{\pi d\ (R_{AB,CD}+R_{BC,DA})\ f}{2ln2} \qquad [B.2]$$

where, d is the thickness of the semiconductor layer (generally ~ 1 for 2DEG channel), f is the correction factor incorporated to take into account the sample inhomogeneity. In order to minimize the errors generated during measurement each resistance ($R_{AB, CD}$ and $R_{BC, DA}$) is calculated with two configurations by altering the flow of current in forward and reverse direction. The asymmetric factor, Q of the resistance can be defined as,

$$Q = R_{AB, CD} / R_{BC, DA} \qquad [B.3]$$

The correction factor, f is dependent on asymmetric Q and for Q<2, f is estimated as[1],

$$f = 1 - \frac{1}{2}\left[\left(\frac{ln2}{1!}\right)\left(\frac{Q-1}{Q+1}\right)^2\right] - \frac{1}{2}\left[\frac{(ln2)^2}{2!} - \frac{(ln2)^2}{3!}\left(\frac{Q-1}{Q+1}\right)^4\right] \qquad [B.4]$$

If either (holes or electrons) carriers dominates in a semiconductor material then the current density J_X is expressed as,

$$J_X = qNv_X \qquad [B.5]$$

where q is the electron charge, v_X is the drift velocity of majority carriers in the semiconductor and N is the carrier concentration.

The Lorentz force, $F_Y = qv_XB_Z$, which causes the carriers to build up in the positive y direction (perpendicular to both current and magnetic field), will be opposed and exactly balanced by the resulting electric field, E_Y under steady state conditions. Therefore,

$$q\ E_Y = qB_Zv_X \qquad [B.6]$$

The Hall co-efficient (R_H) is defined as,

$$R_H = \pm (r_H \frac{1}{qN}) \quad [B.7]$$

where r_H is the hall factor with a magnitude of around unity. The polarity of the Hall co-efficient (R_H) is very important and determines the nature of majority carriers in the semiconductor. A positive polarity indicates a p-type material (holes majority carriers) and negative polarity indicates n-type material (electrons majority carriers). By substituting from equations B.5 and B.6, R_H is given as,

$$R_H = \frac{1}{qN} = \frac{V_X}{J_X} = \frac{E_Y}{J_X B_Z} \quad [B.8]$$

The expression B.8, clearly suggests that R_H is a function of both electric field and voltage. Once the Hall co-efficient (R_H) and resistivity (ρ) is known, the carrier mobility can be extracted as,

$$\mu_H = |R_H| / \rho \quad [B.9]$$

References

[1] Dieter K. Schroder, "Semiconductor material and device characterization," Published by John Wiley & Sons, Inc., Hoboken, New Jersey, Third Edition, 2006.