The University Of Sheffield.

Organic Semiconductor Devices: Fabrication, Characterisation and Sensing Applications

by

Antonis Dragoneas

A thesis submitted for the degree of
Doctor of Philosophy
in Physics

Department of Physics and Astronomy
The University of Sheffield

November 2013

To my mother,

for propagating her pure love and passion for physical sciences

Abstract

Organic semiconductors have increased in popularity over the last two decades. The versatility of organic chemistry enables the development of organic semiconductor devices which can substitute for their abundant inorganic counterparts in various applications. A series of recent innovations in both synthetic chemistry and device fabrication have resulted in remarkable improvements in both the performance and the environmental stability of organic semiconductor devices, which had initially hindered their industrial growth.

Moreover, the processability of organic materials facilitates the development of large-scale electronics on flexible plastic substrates. In addition, the interesting peculiarities of organic semiconductors can be harnessed for the development of gas sensors. The field of organic field-effect transistors (OFETs) is promising for the development of gas sensors capable of detecting more specific interactions between the substance under investigation (analyte) and the sensitive materials of the sensor; the advantage of OFET sensors derives from their complex structure and the plethora of parameters which govern their operation.

This thesis focuses on the field of organic semiconductor devices intended for gas sensing applications. The research work presented here includes the optimisation of the device fabrication methodology with an emphasis on the field of OFETs, the development of bespoke readout electronics for the effective characterisation of these devices and the demonstration of their sensing capabilities by performing quantitative measurements with the aid of the developed readout electronics. Additionally, a study of the environmental stability of the fabricated devices was conducted; this study included an extensive investigation of the sensitivity of these devices to visible light illumination and a demonstration of how minor fabrication optimisations can result in significant light stability enhancement.

Table of Contents

List of figures

List of tables

List of technical drawings and photographs

Chapter 1. Fundamental concepts

1.1. Introduction

This thesis describes the author's contribution to FlexSMELL Marie Curie Initial Training Network (ITN) of the 7th Framework Programme of the European Commission. The main scope of this research network has been the development of an integrated olfaction system based on hybrid (organic and inorganic) electronics and built on a flexible substrate [1]. This system is mainly intended for food freshness monitoring by the incorporation of the appropriate sensors and readout electronics into food packaging.

The following chapters describe the research work conducted towards three major objectives:

i. The optimisation of the fabrication process of organic semiconductor devices, with a special focus on the field of organic-field effect transistors (OFETs). This includes the use of new dielectric materials and the fabrication of devices on flexible plastic substrates.
ii. The development of novel methods for the electrical characterisation of organic semiconductor devices, including the development of bespoke electronic circuits and supporting software, as well as the exploitation of these methods for the study of the performance and stability of OFETs.
iii. The use of the fabricated semiconductor devices in conjunction with the developed characterisation electronics for the delivery of quantitative vapour sensing measurements.

The sequence of the chapters follows a course from basic theoretical concepts to the fabrication, characterisation and use of organic semiconductor devices as actual gas sensors. A brief description of each chapter follows:

Chapter 1 provides an introduction to the terminology and the basic theory behind electronic gas sensors and the use of organic semiconductor devices for gas sensing applications. Moreover, an overview of the important concepts of both inorganic and organic semiconductor physics is given.

Chapter 2 discusses organic semiconductor devices with an emphasis on the concept of organic field-effect transistors (OFETs); this includes a description of their operation, their fabrication methodology and the materials used.

Chapter 3 discusses the methods employed for the morphological and electrical characterisation of the fabricated semiconductor devices.

Chapter 4 describes in detail the novel electrical characterisation system developed and extensively used for the needs of this project.

Chapter 5 discusses the results from the characterisation of OFETs made of different material combinations.

Chapter 6 discusses the results of a supplementary comprehensive study on the light sensitivity of organic semiconductor devices

Chapter 7 is dedicated to vapour sensing using organic semiconductor devices. The experimental methodology and the results from a series of gas exposure measurements are discussed in detail.

1.2. Gas sensors

1.2.1. Terminology

The *electronic gas sensors*, also known as *gas detectors*, are devices capable of detecting the presence of a particular substance within a gas sample; these devices can perform either qualitative or quantitative sensing and are designed to transduce the presence or the quantity, respectively, of this substance into a change in their electrical properties.

The airborne substance under investigation is commonly referred to as the *analyte* or *target analyte*; hereafter, the term *analyte* is used to describe it. An *interferant* is a substance other than the analyte that can induce an unwanted change in the electrical properties of the sensor; such change can be misinterpreted as a response of the sensor to the presence of the analyte. The *selectivity* of a sensor is a measure of its capability of detecting the actual analyte in the presence of interferants.

The limit of detection (LoD) of a sensor is the lowest analyte concentration that the sensor can detect. At a high analyte concentration a sensor may saturate; i.e. its output reaches a maximum (or minimum) and does not further change with increasing analyte concentration. The importance of LoD is very critical for particular applications. For instance, flammable gases have a *lower explosive limit* (*LEL*), i.e. a concentration level above which they can explode; a practical gas sensor for the detection of such a substance must have a lower LoD than the LEL of the gas. Similarly, in food spoilage detection applications, the LoD of a sensor must be lower than the minimum analyte concentration that can render the food inedible.

The analyte concentration range between the LoD and the saturation limit is called the *dynamic range* of the sensor. The *sensitivity* of a sensor is a measure of how much the output of the sensor changes for a change in the analyte concentration; for instance, for a linear-output sensor, its sensitivity is defined as the factor of proportionality between its output and the analyte concentration.

An electronic gas sensor typically consists of two functional parts, the sensitiser and the transducer. The sensitiser is the part that physically or chemically interacts with the analyte; this interaction is usually referred to as the *binding* of the analyte to the sensitiser. The transducer is the part of the sensor that converts this binding into a change of measurable physical quantities; the transducer is usually accompanied by *readout electronics*, which are designed to convert those physical quantities of the sensor into a meaningful electrical output. The majority of the reported and commercially available electronic gas sensors employ either resistive or capacitive transducers. However, more complex semiconductor devices, such as the field-effect transistors (FETs) discussed here, have grown in popularity, mainly thanks to their multiple changeable electrical properties which can be used as individual sensing parameters in some applications.

The reverse phenomena are equally important for the development of practical gas sensors. The time and the conditions which are required for the *unbinding* of an analyte and the return of the sensor to its initial state play a significant role in the concept of *sensor recovery*; i.e. the ability of its output to return to its pre-exposure value. Some exposure effects may be irreversible, impeding the use of the sensor for multiple exposures.

1.2.2. Field-effect transistor sensors

Inorganic FETs have long been used as gas sensing transducers; prominent examples are the ion-sensitive FETs (ISFETs) [2, 3], the suspended-gate FETs (SGFETs) [4], and the hybrid suspended-gate FETs (HSGFETs) [5, 6]. In the majority of these examples, the sensing interactions take place at the gate stack of the FET; changes, such as a drift in the work function of the gate electrode, can modulate the channel of the FET and consequently, detect the presence of an analyte in terms of a change in the electrical characteristics of the FET.

In the field of organic electronics, the relatively low mobility of organic semiconductors has hindered their growth and integration in demanding transistor applications, such as high-frequency integrated circuits (ICs). Nevertheless, the peculiarities in the chemistry of carbon and the nanoscale structure of organic semiconductors nominate them as good candidates for specialised applications, such as optoelectronics and gas sensing. There are several reports of organic field-effect transistors (OFETs) operating as gas sensors [7, 8]. Similarly to their inorganic counterparts, OFET-based transduction is a versatile platform which provides more information than resistive and capacitive transducers; additional electrical parameters, such as threshold voltage and field-effect mobility can be employed as sensing parameters [9]. Moreover, another advantage of OFET-based sensors is the fact that they are able to operate at room temperature, in contrast to metal-oxide semiconductor sensors which require elevated operating temperatures [10, 11]; this attribute enables OFETs to be used as a viable solution for low-power portable sensing systems.

A remarkable difference between inorganic and organic FET transducers lies in the fact that in OFETs, the semiconductor itself can be sensitive to a target analyte, acting as both the sensitiser and the active material of the transducer. For this reason, the OFET channel is deliberately exposed to the medium which contains the analyte; considering that a top gate stack practically acts as an encapsulation which inhibits any interaction between airborne species and the underlying semiconductor, the development of bottom-gate OFETs is more favourable for sensing applications [7, 8].

Moreover, the versatility of organic chemistry can be exploited for the enhancement of sensitivity and selectivity of OFET sensors; appropriate material engineering, such as additions of specific functional groups, in the form of side chains, to an organic semiconductor backbone, can effectively modify the sensing capabilities of an OFET sensor based on this material [12]. Although the exact phenomena that occur during the exposure of an organic semiconductor device to an analyte remain under investigation, it is commonly observed and accepted that analyte molecules bind to the semiconductor surface and trigger several mechanisms in the nanoscale. This binding is mainly attributed to electrostatic interactions between the analyte and the sensor active material molecules, be they of weak van der Waals, dipole-dipole or hydrogen bonding nature [7]. Macroscopically, the observed and quantified effect of an analyte binding is the alteration of the carrier injection and transport in an organic semiconductor device. Duarte *et al.* have given a report on the physics which govern the sensing of chemical vapours with OFET sensors [13].

Firstly, analyte molecules diffusing through the semiconductor and approaching the interface between the source and drain contacts and the organic semiconductor can affect the carrier injection [14]. Secondly, the migration of analyte molecules into the organic semiconductor

grain boundaries can deteriorate the carrier transport along the conduction channel of an OTFT, due to either the introduction of localised charge traps or the screening of the applied field by the accumulation of the analyte molecules [7]. These interactions may have an impact on the conductance of the channel and the mobility of the carriers. Additionally, the analyte molecules that diffuse deeper into the semiconductor film and migrate at the semiconductor-dielectric interface of an OFET can also affect the threshold voltage of the device.

Moreover, the introduction of analyte molecules into the semiconductor film can practically increase the dimensions, hence the volume, of the film; this effect is commonly referred to as *swelling* and sensors based on this mechanism have been demonstrated [15].

Furthermore, the presence of an analyte in the channel of an OTFT can sometimes enhance its conductivity, thanks to the introduction of more charge carriers into the channel; this mechanism is usually referred to as '*doping*' [16]. Doping may manifest itself as an increase in the off-state current flowing through the device, which can also be harnessed as a useful sensing parameter [17].

Alternatively, the sensitivity and selectivity of an OFET sensor can be enhanced by the addition of selective *receptor molecules* acting as sensitisers. For instance, *calixarenes* have been used as a coating of the active material for selective molecular uptake [18], whereas biosensors incorporate agents, such as antibodies, that are complementary to the analyte, leading to a very strong and selective binding, known as 'lock and key'. These kinds of interactions are not studied in this work.

Furthermore, the development of arrays of sensors made of different active materials or bearing differently sensitised surfaces allows for more specific analyte detection based on known patterns or identities for each target analyte; these configurations are known as *electronic noses* [19].

1.3. Inorganic semiconductors

In spite of the essential differences in their physics, a reference to the abundant inorganic semiconductors cannot be excluded from any organic semiconductor study, especially when its main focus is on transistor devices. From the first days of integrated circuits (ICs) to the recently announced (as of 2013) state-of-the-art microprocessors based on 14 nm CMOS technology [20], silicon has been the flagship of the semiconductor technology evolution.

This section provides a brief presentation of the fundamental concepts of inorganic semiconductor technology with a special focus on the properties of silicon. In the following sections, these properties will be compared and contrasted to those of organic semiconductors.

1.3.1. Conductors, insulators and semiconductors

A rather simplified yet widely adopted classification of solid-state materials employs their conductivity (σ) as the main categorisation criterion. Materials with conductivity magnitudes of less than 10^{-8} S/cm are classified as *insulators* and at the other extreme, the ones with σ greater than 10^{3} S/cm are called *conductors*. Materials falling within the intermediate range of conductivities are defined as *semiconductors*.

Inorganic semiconductors can be classified into two major categories with respect to their constituting elements. First, the *element semiconductors* consist of only one kind of atoms, which populate Group IV on the periodic table of elements; prominent examples of this category are *silicon (Si)* and *germanium (Ge)*. Second, the *compound semiconductors* are formed by two or more species of atoms. Despite their relatively higher fabrication costs, compounds of elements from Group III and Group V, such as GaAs, have been espoused by the industry, as thanks to their interesting properties, they may outperform silicon in specialised applications.

1.3.2. Crystals, charge carriers and energy bands

Silicon, as well as many other inorganic semiconductors, forms *crystals*; silicon atoms are periodically arranged at fixed relative positions in a three-dimensional space. The atoms remain bound to their initial position and can only vibrate around it due to thermal activation. The smallest primary building block of a crystal is called *unit cell*. A single crystal is formed by repetitive unit cells which constitute the so-called *lattice* of the crystal.

The atoms of a lattice are bound together by *covalent bonding*; each of them shares the electrons of its outer orbital with its neighbouring atoms. A silicon atom in particular, shares its four outer electrons with its four neighbouring atoms forming four pairs of electrons, also known as *covalent bonds*.

The electrons of an isolated atom have discrete *energy levels*. These energy quantities are commonly expressed in *eV*, a unit which is defined as the energy gained by an electron when its potential is increased by one volt. In the vicinity of other atoms, as in the case of crystals, the outer electron orbitals overlap and the interactions of the neighbouring atoms induce an increase in the number of the allowed energy levels; effectively, the existing energy levels are split into more closely spaced ones. The number of allowed energy states in a given energy

range, i.e. the allowed energy levels including the possible electron spin orientations, per unit volume is called *density of states*.

In the case of a silicon crystal, the interatomic spacing only affects energy levels of the four outer (valence) electrons. The orbital radii of the inner 10 electron energy levels are much smaller, leaving them intact. The third (outer) shell of the silicon atom is a doubly degenerate energy level which consists of 3s and 3p subshells. In an isolated atom, 3s subshell bears two allowed quantum states, whereas 3p has six. At absolute zero (T = 0 K), two of the four valence electrons are found in 3s and the remaining two in 3p. When the atom is found in a crystal lattice, its 3s and 3p subshells are altered and when the crystal is at an equilibrium state, they comprise four quantum states each. At absolute zero again, the four valence electrons occupy the respective quantum states of the 3s subshell leaving 3p unoccupied. This extreme condition, of a fully occupied 3s and an empty 3p subshell does not allow any charge conduction through the crystal.

The highest occupied band, which is 3s in this case, is called *valence band*, while the lowest unoccupied is named *conduction band*. The lowest energy level of the conduction band is denoted by E_C and the highest energy level of the valence band by E_V. There are no allowed energy states between E_C and E_V and the energy difference E_C-E_V is called *bandgap energy* (E_g). The E_g is an important figure of merit for semiconductors as it defines the required energy which can excite an electron from the valence to the conduction band leaving an unoccupied state in the former. These excited electrons are called *free electrons* and contribute to the electrical conduction of the crystal; meanwhile, the resulting electron deficiencies in the valence band are referred to as *holes*. Holes possess positive charges and also contribute to the total conduction of the crystal; electrons and holes are referred to as *charge carriers*. It is worth emphasising that the electrical conduction in a semiconductor requires the presence of charge carriers, which is possible only when its energy bands are partially filled with electrons.

This excitation described above is known as *electron-hole pair generation* and constitutes the mechanism which the conduction in semiconductors in based upon. Electron-hole pair generation can be induced by the absorption of photons of adequate energy. Also, E_g decreases with increasing temperature, while elevated temperatures can excite carriers across the bandgap, effectively increasing its conductivity.

The band structure illustrates the energy-momentum relation in a crystalline solid. It is a common practice to plot the energy bands, including E_C and E_V, as energy versus *momentum (k)*. The structure of E_C and E_V constitutes an important classification criterion for semiconductors; i.e. the dependence of E_C and E_V on k defines the type of the semiconductor. In a *direct bandgap semiconductor*, such as GaAs, the minimum of E_C occurs for the same k as the maximum of E_V, whereas in an *indirect bandgap semiconductor*, such as silicon, the respective minimum and maximum levels appear at different k. Direct bandgap semiconductors are of great importance for optoelectronic applications, as their band structure facilitates the absorption and emission of photons; this results in higher *quantum yields* compared to silicon, which is key for the development of very efficient devices, such as light-emitting diodes (LEDs).

Recalling the crystal lattice structure, when charge carriers move over distances extending beyond the size of the unit cell, their movement differs from that expected in vacuum. This difference can be simplified with the introduction of the concept of *effective mass* of electrons (m_e^*) and holes (m_h^*). The effective mass depends on the energy-momentum relation according to:

$$m_e{}^* = \frac{\hbar k^2}{2(\mathrm{E(k)} - E_0)} \tag{1.1}$$

where E(k) is the energy of the electron in band, E_0 is the edge energy of that band, ħ is the *reduced Planck constant* (~6.582 x 10^{-16} eV·s) and k is the momentum.

As a result, the effective mass can be extracted from the energy-momentum graphs by applying appropriate parabolic fits to them. However, the complexity of the band structures of most semiconductors does not provide for a single definition of effective mass. In practice, for common calculations, effective masses of particular materials are usually taken as constants.

1.3.3. Fermi energy, intrinsic and extrinsic semiconductors

In the absence of any other external excitations, the thermal activation at a given non-zero temperature is the only mechanism which can induce the electron-hole pair generation. When the concentration of impurities in a semiconductor crystal is small in comparison with the amount of thermally-generated carrier pairs, the semiconductor is called *intrinsic*.

The total number of electrons per unit volume in a semiconductor, also known as *electron density*, can be calculated as an integral of the product of the density of states *N(E)* and the probability of an electron occupying each state *F(E)* for a range which extends from the top of the conduction band to the bottom of the valence band. The probability function F(E) is known as *Fermi distribution function*. The energy for which F(E) = ½ is called *Fermi energy*. In the case of intrinsic semiconductors, the Fermi energy at room temperature lies in the middle of the bandgap E_g. The electron density at the bottom of the conduction band alone is denoted by *n*, whereas the *hole density* at the top of valence band by *p*. For an intrinsic semiconductor, n =p = n_i , where n_i is called *intrinsic carrier density*.

The addition of doping impurities, i.e. commonly other elements from Groups III to V, to the crystal introduces new energy levels and the semiconductor is then referred to as *extrinsic*. In general, additives which are more electronegative than the main crystal element donate electrons to the crystal, hence they are called *donors*. The extra electrons are loosely bound to their original nuclei and can more easily be excited to become free electrons, as described above. The required energy for this excitation is called *ionisation energy*. In a similar manner, electropositive dopants introduce holes to the crystal and they are referred to as *acceptors*. In some cases, dopants from the same Group can be deliberately added to the crystal; these techniques do not necessarily introduce charge carriers but aim to alter other properties of the carriers by changing the crystal structure. An example of this approach is strained-silicon technology based on Si-Ge heterostructures [21].

In lightly-doped semiconductors, commonly referred to as *non-degenerate semiconductors*, the electron or hole density is very small as compared to the effective density of states in the conduction or valence band, respectively. In the case of electron donation, it is assumed that

the thermal energy at room temperature can activate all donor atoms, which density is denoted by N_D, and consequently provide an equal number of electrons to the conduction band; a phenomenon which is known as *complete ionisation* [22]. The Fermi energy is affected by doping and moves towards the bottom of the conduction band and its value can be calculated by the following equation:

$$E_C - E_F = kT \ln\left(\frac{N_C}{N_D}\right) \quad (1.2)$$

where k is Boltzmann's constant, T is the absolute temperature and N_C is the effective density of states in the conduction band.

Likewise, when acceptors of N_A density are present in the crystal, the Fermi energy moves closer to the top of the valence band. Its magnitude can be calculated by:

$$E_F - E_V = kT \ln\left(\frac{N_V}{N_A}\right) \quad (1.3)$$

where N_V is the effective density of states in the valence band.

The *intrinsic Fermi level* is denoted by E_i. It is a common practice to express charge carrier densities with respect to the intrinsic quantities n_i and E_i:

$$n = n_i \, exp\left(\frac{E_F - E_i}{kT}\right) \quad (1.4)$$

and

$$p = n_i \, exp\left(\frac{E_i - E_F}{kT}\right) \quad (1.5)$$

As in the case of intrinsic semiconductors, the product of n and p constantly equals n_i^2 at thermal equilibrium. This relation is known as the *mass action law*:

$$n\,p = n_i^2 \quad (1.6)$$

Even in the presence of both donors and acceptors in the same crystal, the one of the highest concentration prevails and determines the conduction type of the semiconductor. The carriers with the highest concentration are called *majority carriers*, whereas the fewer ones are named *minority carriers*. When electrons are the majority carriers in an extrinsic semiconductor, the latter is characterised as *n-type semiconductor*. Similarly when holes prevail, it is a *p-type semiconductor*.

1.3.4. Charge carrier transport

The understanding of the charge carrier transport phenomena taking place in a semiconductor is of vital importance for the development of semiconductor devices. There are several contributing factors to the electrical conduction of inorganic semiconductors, the most important of which are *carrier drift* and *carrier diffusion*. However, in particular applications, other phenomena such as *electron-hole pair generation and recombination*, *quantum tunnelling*, *avalanche multiplication* and *thermionic emission* can have a major, even prevalent contribution to the current conduction of the semiconductor. Due to their significance and mainly due to the key differences in the carrier transport between inorganic and organic semiconductors, a brief description of first four mechanisms is given below.

1.3.4.1. *Carrier drift, mobility and conductivity*

As discussed above, in the absence of any external excitations, the electrons of a uniformly doped semiconductor are thermally activated at any non-zero temperature; the lattice vibrations provide kinetic energy to the electrons and consequently, the holes of the lattice. In non-ideal crystals and at non-zero temperatures, the motion of the electrons along a crystal lattice is subject to collisions; electrons may scatter due to the presence of crystal defects, the presence of impurities (atoms of different elements present in the crystal) and/or the thermal vibrations of the lattice. The thermal vibrations are described by a concept of quasiparticles, known as *phonons*.

Two important quantities related to these collisions are the distance an electron travels between collisions, commonly referred to as the *mean free path*, and the time between collisions, called the *mean free time* t_c. When a bias is applied to the semiconductor, an electrostatic force is exerted on the electrons of the partially occupied bands, i.e. free electrons; consequently, these carriers drift along the applied field lines. The velocity component induced by the presence of the electric field is named *drift velocity*, which can be calculated according to:

$$-q\mathcal{E}t_c = m_n^* v_n \tag{1.7}$$

or

$$v_n = -\frac{qt_c}{m_n^*}\mathcal{E} \tag{1.8}$$

where q is the elementary charge, Ɛ is the electric field and v_n is the drift velocity of electrons.

The factor qt_c/m_n^* is called *electron mobility* μ_n. Similarly, μ_p denotes *hole mobility*. Charge carrier mobility constitutes one of the most important quantities for both inorganic and organic semiconductors and it is commonly used as a benchmark of their electrical performance.

$$\mu = \frac{qt_c}{m^*} \tag{1.9}$$

where m^* is the effective mass of the charge carriers. The dependence of the effective mass on the energy-momentum relation, as described by eq. (1.1), also reflects on the dependence of mobility on this relation.

Mobility is vulnerable to various carrier scattering mechanisms which effectively act as mobility degradation factors. The two major mechanisms are *impurity scattering* and *lattice scattering*. The former occurs when the charge of ionised impurities deflects the drifting electrons and holes from their trajectory due to Coulomb force interactions; for this reason, it is usually referred to as *Coulomb scattering*. The latter is due to the interactions between the drifting carriers and the thermal lattice vibrations (phonons); likewise, this mechanism is also known as *phonon scattering*.

The effect of each of these mechanisms on the mobility is temperature dependent. At low temperatures, Coulomb scattering is the prevalent mobility degradation cause, especially in the case of heavily doped semiconductors, which comprise a large number of impurities. However, as temperature increases the higher kinetic energy of the carriers mitigates the Coulomb force effects. Conversely, at higher temperatures, phonons become the dominant

mobility degradation factor; the amplitude of vibrations increases, effectively increasing the probability of collisions and consequently, reducing the mean free time (t_c).

In principle, all carriers in a semiconducting crystal lattice suffer from mobility degradation at elevated temperatures. This constitutes a major difference between single crystal and amorphous or polycrystalline materials, in which temperature changes can induce opposite results as more carrier transport mechanisms are involved. A further discussion on the charge transport of amorphous organic materials is given in section 1.5.2.

The total current in a semiconductor induced by an applied electric field is called *drift current* I_{drift} and equals the sum of electron and hole drift currents. The *conductivity* σ of the semiconductor equals:

$$\sigma = q(n\mu_n + p\mu_p) \tag{1.10}$$

where n is the electron density, p is the hole density, μ_n is the electron mobility and μ_p is the hole mobility.

The *drift current density* J_{drift} is the drift current per unit area which flows through a semiconductor of a cross-sectional area A under the effect of an applied field Ɛ and it can be expressed by *Ohm's law*:

$$J_{\text{drift}} = \frac{I_{\text{drift}}}{A} = \sigma\mathcal{E} \tag{1.11}$$

1.3.4.2. *Carrier diffusion and total current density*

In the idealised assumption of a uniformly doped semiconductor, drift current is the only major carrier transport mechanism. When impurities are not uniformly distributed in the bulk of the semiconductor, their concentration gradients trigger the transport of carrier from high to low concentration regions. This mechanism is known as *carrier diffusion*. The diffusion process governs the operation of all semiconductor devices which employ *p-n junctions*, such as silicon diodes and bipolar transistors.

In this case, the induced current is called *diffusion current* I_{diff} and has two components; the *electron diffusion current* and the *hole diffusion current*. Its density J_{diff} in a semiconductor of cross-sectional area A is defined as:

$$J_{\text{diff}} = \frac{I_{\text{diff}}}{A} = q\left(D_n\frac{dn}{dx} - D_p\frac{dp}{dx}\right) \tag{1.12}$$

where D_n and D_p are the *diffusion coefficients, constants* or *diffusivities* of electrons and holes, respectively, and dn/dx and dp/dx are the spatial derivatives of electron density and hole density, respectively.

The total current density J_{total} is the sum of drift and diffusion current densities for both electrons and holes; from (1.10), (1.11) and (1.12), it is derived that:

$$J_{\text{total}} = J_{\text{drift}} + J_{\text{diff}} = q\left(\mu_n n\mathcal{E} + D_n\frac{dn}{dx} + \mu_p p\mathcal{E} - D_p\frac{dp}{dx}\right) \tag{1.13}$$

Interestingly, carrier drift and diffusion are associated through *Einstein relation*, which describes the dependence of the diffusion coefficient on mobility:

$$\mathrm{D} = \frac{\mu \mathrm{kT}}{\mathrm{q}} \tag{1.14}$$

where k is the Boltzmann constant (~1.3806 × 10^{-23} m^2 kg s^{-2} K^{-1}), q is the elementary charge and T is the temperature.

1.3.4.3. *Electron-hole pair generation and recombination*

The mass action law expressed by eq. (1.6) is valid at thermal equilibrium and in the absence of any external excitations. When more carriers are introduced to the semiconductor by an external stimulation, such as light illumination, this relation is no longer valid as:

$$n\,p > n_i^2 \tag{1.15}$$

In this occasion, competing mechanisms for the restoration of the thermal equilibrium conditions take place; the injected electrons may recombine with holes or vice versa. The process is called *electron-hole pair recombination* and results in the release of *photons* or *heat* which is transferred to the crystal lattice. The former case is known as *radiative recombination* and the latter as *non-radiative* recombination.

The nature of the recombination mechanism varies between direct- and indirect-bandgap semiconductors. In the former case, the process is called *direct recombination* and does not require any momentum change contributions from the lattice vibrations. At thermal equilibrium, electron-hole pair generation and recombination present themselves at equal rates so that the mass action law remains valid. However, the probability of the occurrence of the direct recombination mechanism in an indirect-bandgap semiconductor is very low. Most likely, a momentum change is required for a carrier pair to recombine; hence interactions with the lattice vibrations must be involved. In this case, the process is called *indirect recombination*.

1.3.4.4. *Quantum tunnelling*

When two different semiconductors or a semiconductor and a metal are separated by thin dielectric, i.e. a material with large bandgap energy, an energy barrier hinders carriers from crossing the interface between the two materials. Nevertheless, it is possible for charge carriers to *tunnel* from one another through the high intermediate energy barrier, even if their energy is lower than the barrier energy itself. This phenomenon is referred to as *quantum tunnelling*.

Although the effect of this phenomenon on large dimension semiconductor devices is usually negligible, quantum tunnelling constitutes a major impediment to the scaling of the very large scale integration (VLSI) technology down to the few-nm-node regime [23] and the continuation of the widely accepted *Moore's law* on VLSI evolution [24]. This is mainly due to tunnelling-induced high gate leakage currents which are encountered in *complementary metal-oxide-semiconductor (CMOS)* technology transistors of such small dimensions. However, special-purpose semiconductor devices, such as *tunnel diodes*, deliberately exploit quantum tunnelling in their operation.

1.4. Organic chemistry

Organic semiconductors (OSCs), which are commonly categorised according to their degree of polymerisation; they can be classified as either *low-molecular-weight semiconductors*, also referred to as *semiconducting oligomers*, or *semiconducting polymers*.

Inorganic semiconductor physics is based upon covalent crystal models; the major charge carrier transport mechanisms in inorganic semiconductors are best explained by band transport theory, which derives from the interactions of atoms in a crystal lattice. In OSCs, the crystal model and the band transport theory cannot adequately describe the occurring charge transport phenomena.

The difference in the charge transport of OSCs is mainly due to their molecular nature; the charge carriers are strongly bound to their original molecule, a concept known as charge *localisation*. The charge carriers cannot easily move between neighbouring molecules, even in the case of organic crystals. Recalling the carrier drift terms from section 1.3.4.1, it can be thought that, in the case of OSCs, the mean free path of charge carriers does not easily extend beyond the size of a molecule.

The transition from inorganic to organic semiconductor theory requires an understanding of the chemistry which dictates the bond formation in the case of carbon (C) atoms. An important peculiarity of carbon lies in the concepts of *promotion* and *hybridisation*, which are described in the following section.

1.4.1. Hybridisation and carbon bonds

In the ground state, the six electrons of a carbon atom are found in the locations shown in Table 1-I:

Table 1-I – Electron distribution in the orbitals of a carbon atom in ground state

Orbital →	1s	2s	$2p_x$	$2p_y$	$2p_z$
Number of electrons →	**2**	**2**	**1**	**1**	**0**

Promotion is carried out when one 2s electron moves to the previously empty p_z orbital; this promotion of the 2s electron results in the formation of three possible combinations of the remaining 2s electron with one to three 2p orbitals; these combinations are referred to as *hybrid orbitals* and are denoted by *sp*, *sp2* and *sp3* when they involve one, two or three 2p orbitals, respectively.

From a stereochemical point of view, each hybrid leads to different bonding arrangements in a three-dimensional space, as shown in Figure 1-1. First, sp3 hybrid orbitals form equispaced bonds. The angle between the bonds is roughly 109.5° as the four bonds coincide with the segments joining the centre and the vertices of a tetrahedron. An sp3 hybrid can form four bonds with the outer orbitals of its neighbouring atoms. Two sp3 hybrids are tied together by a strong *σ bond* (C-C).

Next, sp2 hybrid orbitals have three of these segments equispaced on one plane, forming 120° angles between them; the remaining p orbital is perpendicular to this plane. For a molecule to be formed, the presence of another sp2 hybrid is necessary. The two hybrids are linked by a

strong σ bond as in the case of sp3 hybrids plus a weaker bond due to the overlap of their perpendicular p orbitals. The latter bond is called *π bond* and the respective shared electron is referred to as *π electron*. The two bonds together constitute a bond commonly known as *double bond* (C=C), which is encountered in chemical compounds such as alkenes. It is worth noting that π bonds are weaker due to the fact that their respective orbitals are more distant from their parent nuclei, making π electrons loosely bound to them. This attribute is known as *delocalisation* and is of great importance for the charge carrier transport in organic semiconductors.

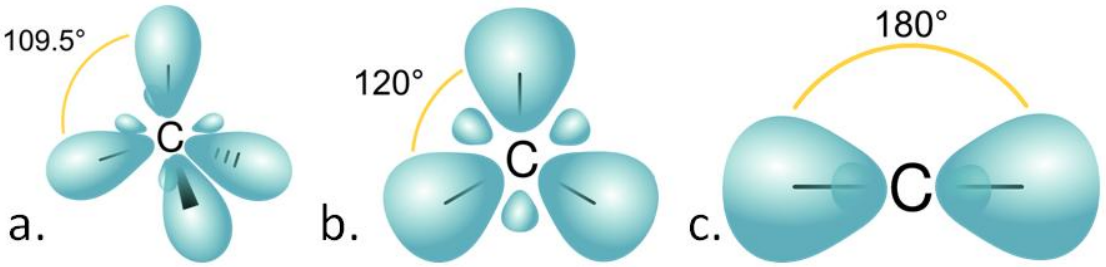

Figure 1-1 – Graphical representations of: a. four sp3 hybrid orbitals, b. three sp2 hybrid orbitals and c. two sp hybrid orbitals [25]

Last, sp hybrid orbitals have two of their segments on one axis, say x, and each of their remaining p orbitals on each of the two perpendicular axes, say y and z. A molecule can be formed by the combination of two sp hybrids. In this combination, three bonds are made; a σ bond between the orbitals of the respective x axes plus two π bonds between the perpendicular p orbitals. This combination of bonds is known as triple bond (C≡C), which is found in chemical compounds such as alkynes.

1.4.2. Conjugation, molecular orbitals and bandgap

The main building block of many functional organic semiconducting molecules is the benzene ring. Benzene is formed by six sp2 hybrids. The planar arrangement of the sp2 hybrid orbitals, with the 120° angles between their bonds, creates a planar regular hexagon with each carbon nucleus residing on each of its vertices. There is a σ bond between each atom of the ring, whereas each carbon hybrid makes a π bond with either of the neighbouring atoms. This results in two possible configurations as shown in Figure 1-2. Much of the material engineering for organic semiconductors focuses on the enhancement of conjugation, i.e. the delocalisation of π electrons over a larger extent of the system. These chemical modifications can result in desirable changes in properties such as the mobility of charge carriers, as discussed in section 1.5.

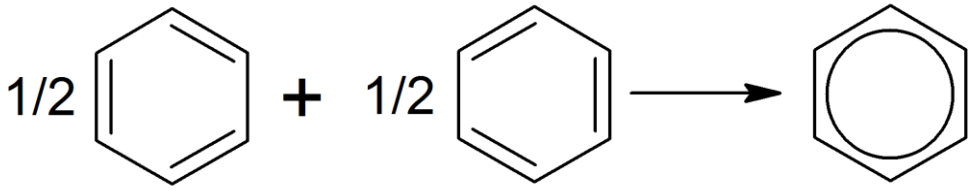

Figure 1-2 – Graphical representations of the possible benzene ring configurations

These configurations of alternating single and double (or triple) bonds between carbon atoms are a typical example of *conjugation* in organic systems; every organic molecule having this series of bonds is considered a *conjugated system*. In practice, the π electrons are not strictly associated with an atom or the bond between two adjacent atoms; conversely, they are *delocalised* and shared among a larger number of atoms of the same molecule.

The *molecular orbital (MO) theory* provides a better understanding of the behaviour of π electrons within an organic molecule. According to this model, a molecule constitutes an entity with its own orbitals rather than a superposition of individual atomic orbitals of its constituent atoms. In the case of semiconductors, the MO approach introduces concepts for organic molecules which bear some resemblance to their inorganic counterparts; the molecular electronic orbitals also have discrete energy levels, which are occupied by electrons. According to the MO theory, the most energetic orbital occupied by electron(s) is called *highest occupied molecular orbital (HOMO).* Similarly, the term *lowest unoccupied molecular orbital (LUMO)* refers to next higher orbital. It should be mentioned that the concept of HOMO is homologous with the valence band (E_V), whereas that of LUMO is homologous with the conduction band (E_C), in inorganic semiconductor theory, as discussed in section 1.3.2. HOMO and LUMO are called the *frontier orbitals* of a molecule.

An inherited inorganic term is the meaning of bandgap. In organic molecules, the energetic difference of HOMO and LUMO levels constitutes the bandgap of the molecule. The size of this gap depends on the delocalisation of π electrons, which, in turn, depends on the conjugation of the molecule. As the conjugation of a molecule increases, the π electrons become more delocalised; the decrease of the energetic difference between subsequent discrete energy states can be explained and visualised by an analogue of the *particle in a box* model of quantum physics by considering that this energetic difference scales with the extent of delocalisation according to:

$$E \propto \frac{1}{L^2} \tag{1.16}$$

where E is the energetic difference or the HOMO-LUMO gap (bandgap) and L is the size of the box in the typical model or can be thought as the length of delocalisation in an one-dimensional π system.

In molecules with extended delocalisation, the bandgap can drop in the range of a few eV, similar to the energy of visible light photons; this facilitates the excitations of electrons from HOMO to LUMO. For this reason, *conjugated molecules* can be classified as *organic semiconductors*. In practice, these two terms are usually interchangeable.

The elimination of bandgap in an one-dimensional π system and thus, the development of organic conductors, is inhibited by an instability explained by *Peierls transition*; this theorem implies that a bandgap always arises in an one-dimensional system regardless of the extent of delocalisation.

1.4.3. Polarons, ionisation potential and electron affinity

A fully occupied HOMO brings a molecule in its ground state. For the initiation of charge transport in a molecule, its ground state must be disturbed by the removal of an electron from its HOMO or the addition of an extra electron which will occupy its LUMO. These changes transform the molecule into a *radical ion*. In the former case, the ion bears a positive charge, thus it will be a *radical cation*. In the latter case, the total charge is negative and the ion is a *radical anion*.

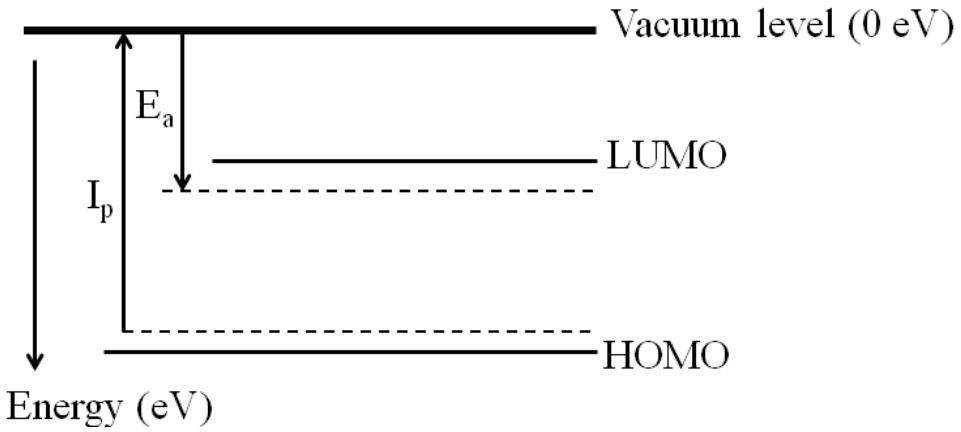

Figure 1-3 – A diagram illustrating the frontier orbitals of an organic molecule along with their electron affinity (E_a) and ionisation potential (I_p) levels.

Radical cations and anions are usually referred to as *hole and electron polarons*. The addition or subtraction of charge carriers not only affects the total charge of the resulting ion, but also results in alterations of its stereochemical configuration as compared to that of the molecule in the ground state. These alterations are usually referred to as *relaxation*. In other words, the molecule polarises itself under the influence of the added/withdrawn charge; hence, the concept of polaron covers both the charge and the induced polarisation of the ion.

The coupling of electrons with the stereochemical configuration of the molecule, known as *electron-phonon coupling*, complicates the energetic relations related to the development of polarons. As a result, the amount of energy needed to inject an electron into the LUMO or withdraw an electron from the HOMO does not equal the bandgap of the molecule. To account for this coupling, two additional energy levels are defined; the *ionisation potential (Ip)* is the energy needed for the withdrawal of electron from the HOMO and *electron affinity (Ea)* is the energy gained by an electron when added to the LUMO. I_p is of lower energy compared to HOMO, whereas E_a is of higher energy compared to LUMO. These energy levels are illustrated in Figure 1-3.

1.5. Charge injection and transport in organic semiconductors

The operation of all semiconductor devices hinges on the injection of charge carriers into a semiconducting medium and the transport of charge over the functional extent of the medium. In most device configurations, carrier injection is achieved by the use of metal electrodes brought in direct contact with the semiconductor; thus, the physics of the metal-semiconductor interface dictate the injection process. Section 1.5.1 refers to these mechanisms.

Charge transport in organic semiconductor devices has been mainly attributed to the properties of small polarons from the early years of the relevant research [26]. However, much of the transport mechanisms in both low-molecular weight and polymer semiconductors still remain under investigation. The involvement of extrinsic factors, such as the presence of impurities in the semiconductor, impedes the development of consistent models for the understanding and simulation of a pragmatic organic semiconductor device. Section 1.5.2 discusses the major charge carrier transport mechanisms which are widely accepted in modern organic semiconductor theory.

1.5.1. Metal work function, contact resistance and charge injection

The *work function (W_F)* is a surface property of a metal which expresses the energy required for the removal of an electron from its surface to a point in vacuum. W_F is commonly expressed in *eV*.

The selection of metals of appropriate work functions is of utmost importance for the operation of organic semiconductor devices. A good match of the W_F with either the electron affinity (E_a) of the semiconductor for electron injection, or its ionisation potential (I_p) for hole injection (electron withdrawal) is imperative. In a rather simplified notion, for the unhampered injection of charges from a metal to a semiconductor, the W_F must be higher than the I_p for hole injection or lower than the E_a for electron injection. In this case, the metal-semiconductor contact is considered as *ohmic*. However, in many cases, the W_F of the metal electrodes does not meet this requirement and this consequently introduces a potential difference which must be surmounted for carrier injection to take place. This potential difference is known as *injection barrier*.

Assuming that Schottky-Mott rule holds true, the injection barrier ($q\phi_b$) for electron injection from a metal to semiconductor simply writes:

$$q\varphi_b = E_a - W_F \tag{1.17}$$

and similarly for hole injection:

$$q\varphi_b = W_F - I_p \tag{1.18}$$

From an application perspective, this barrier can be interpreted as an additional requirement for the operating voltage of the semiconductor device; i.e. a portion of the applied voltage, which equals ϕ_b, will be used to compensate for the injection barrier.

However, several actual metal-semiconductor interfaces do not comply with the Schottky-Mott rule. Instead, complex physical and chemical interactions between the metal and the semiconductor induce the development of dipoles at their interface. The presence of dipoles

results in a misalignment of the vacuum levels for the metal and the semiconductor, which effectively results in an increase or lowering of the injection barrier. In other words, the dipole can either impede or enhance the injection of charge carriers depending on its polarity. Indisputably, the involvement of dipoles impedes the understanding of charge injection in real devices. In many cases, advanced characterisation techniques, such as *ultraviolet photoemission spectroscopy (UPS)* and *inverse photoemission spectroscopy (IPES)*, are required for precise quantification of the actual injection barrier in a device.

In inorganic semiconductors, injection barriers can be modified by deliberate *doping* of the semiconductor in the areas which come in direct contact with the metal. However, the doping of organic semiconductors for charge injection enhancement remains a challenging endeavour, especially in the case of electron injection [27]. Interestingly, it has been shown that in some instances, slightly contaminated metal-organic semiconductor interfaces can practically enhance injection [28]. In this example, contamination acts as a passivation layer which eliminates the interactions between the metal and the semiconductor and thus, the development of dipoles.

There is a variety of mechanisms underpinning charge injection from a metal to a semiconductor. While the energetic barriers discussed above could be overcome by thermionic emission, experimental studies have confirmed that field-emission, also known as *Fowler-Nordheim quantum tunnelling*, has a contribution to charge injection [29, 30]. Furthermore, it is suggested that defects of the semiconductor at its interface with the metal contact introduce intermediate energy states which could practically act as stepping stones for the injection of charges, in a process referred to as *defect-assisted injection* [31].

In most types of semiconductor devices, such as *organic field-effect transistors (OFETs)* and *chemiresistors*, described in sections 2.1.2 and 2.1.3, respectively, carriers are injected by a metal contact into a semiconducting film and after traversing a conduction channel, they get collected by a second metal contact. The two potential barriers, for the injection and collection of charge, manifest themselves as a measureable quantity, commonly known as *contact resistance (R_c)*. In practice, a metal-semiconductor contact is defined as ohmic when contact resistance is substantially smaller than the resistance of the semiconducting channel (R_{ch}), i.e.:

$$R_c \ll R_{ch} \tag{1.19}$$

However, when this condition does not hold true, the charge injection from a metal contact constitutes a bottleneck for the operation of a device. In this occasion, the charge carrier transport through the semiconductor device is considered as *injection-* or *contact-limited*.

Conversely, when channel resistance is comparable or even higher than contact resistance and charge carrier transport is considered as *bulk-limited*. The theory which describes the charge transport in the bulk of organic semiconductors is discussed in the following section.

1.5.2. Charge carrier transport in conjugated systems

As previously discussed, unlike inorganic semiconductors, the charge carrier transport in organic molecules cannot adequately be explained by the band transport theory. This section discusses the widely accepted theories which explain the charge carrier transport in organic semiconductors.

1.5.2.1. *The polaron model*

The occurrence of real band transport in organic semiconductors was first reported by Karl *et al.* to have been observed in pure crystals of oligoacenes [32]; the authors mainly base their conclusion upon the mobility (μ) dependence on temperature (T):

$$\mu(T) \propto \mathrm{T}^{-\mathrm{n}} \tag{1.20}$$

where n is typically a positive constant, thus μ is expected to decrease with increasing temperature. However, the validity of these claims remains challenged and controversial [33].

A better received theory is based upon the concept of polarons, discussed in section 1.4.3. Recalling the inorganic notion of drift velocity (v) under the application of an electric field (Ɛ):

$$v = \mu\mathcal{E} \tag{1.21}$$

According to the polaron model, the total mobility of carriers (μ) is defined as the sum of mobilities induced by a coherent (band-like) transport mechanism (μ_{coherent}) and an incoherent transport mechanism (μ_{hopping}), known as *hopping*:

$$\mu = \mu_{\text{coherent}} + \mu_{\text{hopping}} \tag{1.22}$$

It should be mentioned that the coherent mechanism is referred to as *tunnelling* by some authors [34]; to avoid confusion, this term is not adopted here as, in fact, the incoherent mechanism (hopping) also describes the thermally-assisted tunnelling of carriers between adjacent molecules.

The prevalence of either of these two contributing factors depends on the strength of electron-phonon interactions of a molecular system; for strong electron-phonon coupling, the hopping contribution becomes dominant. As previously mentioned in section 1.4.3, organic materials typically exhibit stronger coupling than inorganic materials and as a result, hopping is expected to be the major driving force for charge carrier mobility at room temperature. Hopping is a thermally-assisted phenomenon; the mobility of organic semiconductors typically increases with increasing temperature.

Contrarily, band-like transport can only be possible in the very low temperature regime, where the electron-phonon interactions are minimised, so is the hopping contribution to total mobility of charge carriers [35].

1.5.2.2. *The effect of disorder*

The structural *disorder* of OSCs, which is more pronounced in the case of amorphous and polycrystalline films, introduces additional impediments in charge carrier transport. Disorder can be classified into *diagonal* and *off-diagonal*. The former term refers to the distribution of the energetic (HOMO/LUMO) levels in the individual molecules of an organic system; the latter addresses the fluctuations in the strength of interactions between adjacent molecules. In the particular case of semiconducting polymers, diagonal disorder can stem from the distribution

of the *effective conjugation length* and other effects of electrostatic nature [34]. Conversely, off-diagonal disorder is closely related to the molecular packing and the morphology of a semiconducting thin-film; this fact underscores the importance of device fabrication conditions in the electrical performance of the device.

Bässler *et al.* have pioneered the study of the role of disorder in the charge carrier transport in organic materials by conducting Monte Carlo (MC) simulations [36]. In that study, equations for the numerical approximation of mobility based on the degree of both diagonal and off-diagonal disorder were introduced. The suggested equations predict a straight line in a plot of $\ln(\mu)$ versus $1/T^2$, which slope depends on the both the diagonal and off-diagonal disorder parameters. This dependence can be exploited for the quantification of disorder changes from electrical measurements taken at different temperatures [37].

This model was further expanded by Pasveer *et al.* to account for dependence of mobility on the charge carrier density [38].

1.5.2.3. *The effect of space charge*

The conductance of a real semiconductor device cannot be accurately described by Ohm's Law, described by eq. (1.11), as the strength of the electric field varies along the semiconducting film employed in the device. Assuming an initially intrinsic (undoped) semiconductor, the injection of charge carriers from a metal electrode into the bulk of the semiconductor introduces *space charges* along the conduction path; the presence of these charges effectively masks the externally applied field and, consequently, results in a reduction of the resulting current; this current is commonly referred to as *space-charge-limited current* (*SCLC*) and the respective current density is described by:

$$j_{SCLC} = \frac{9}{8}\epsilon_r\epsilon_0\mu\frac{V^2}{L^3} \tag{1.23}$$

where ε_r is the static permittivity of the semiconductor, ε_0 is the vacuum permittivity (~8.854 x 10^{-12} F/m), μ is the mobility of charge carriers, V is the externally applied voltage and L is the length of the conduction path.

Although the SCLC model is better suited for real organic semiconductor devices, the assumption of the absence of dopants, i.e. charge carrier donating agents, and charge carrier traps, discussed in the following section, remains an unrealistic scenario.

1.5.2.4. *The effect of charge carrier traps*

In real organic semiconductor devices the presence of charge carrier traps is unavoidable. Traps can be characterised as either *electron traps*, when their energy state is somewhat higher than the electron affinity (E_a) of the semiconductor, or hole traps, when their energy state is somewhat lower than its ionisation potential (I_p). Charge carriers are effectively trapped by these energy sites due to the aforementioned energy differences.

Traps are also classified into *shallow* and *deep* traps with respect to the thermal energy (k_BT); when thermal energy can easily release the trapped charge carriers then the trap is considered to be shallow, otherwise it is thought as a deep trap. Charge carriers need external excitations in order to be released from deep traps; this can be achieved by an increase in temperature, the application of an external electric field or illumination.

Moreover, the presence of deep traps is believed to define the type of an organic semiconductor; i.e. *hole-transporting (p-type)* or *electron-transporting (n-type)*. In inorganic terms, the type of a semiconductor is controlled by the deliberate introduction of dopants into the bulk of an intrinsic semiconductor such as silicon; the introduction of electron-donating atoms, such as arsenic (As), results in electron-transporting (n-type) properties, whereas the introduction of electron acceptors, such as boron (B), induces hole-transporting (p-type) properties. Instead, organic semiconductors have long been observed to intrinsically be either hole-transporting or electron-transporting materials, with the former constituting the vast majority of OSCs. However, studies on organic semiconductor devices employing materials with low trap densities have revealed that the transport of both types of carriers is possible for some semiconductors [39]; this type of semiconductors is commonly referred to as *ambipolar*.

The presence of traps introduces more parameters to be taken into account for the understanding of the operation of semiconductor devices; the experimental observations on actual devices usually deviate significantly from behaviours described by SCLC theory. In complex semiconductor devices, such as the organic field-effect transistors (OFETs), which constitute the main focus of this study, the presence of traps in the bulk of the semiconductor and at the semiconductor-dielectric interface, has an impact on important parameters, such as their threshold voltage and mobility. More information on the operation of OFETs is given in section 2.1.2.

Chapter 2. Organic semiconductor devices

2.1. Thin-film semiconductor devices

Thin-film semiconductor devices consist of a combination of either patterned or non-patterned thin films of materials in such fashion that can give the device particular functional properties. The concept of inorganic thin-film devices such as thin-film transistors (TFTs) was first introduced by Weimer in 1962 [40]. This concept has been adopted by the industry for the development of various electronic applications employing amorphous or polycrystalline silicon deposited onto insulating, and in some instances, transparent substrates; some of their most popular applications are the *active matrix*, *TFT liquid-crystal displays* (*LCDs*), in which TFTs are used to drive individual pixels of the display.

The thin-film architecture is the most successful approach in the development of organic semiconductor devices; the majority of the demonstrated devices, be they organic light-emitting diodes (OLEDs), organic photovoltaic cells (OPVs), organic chemiresistors or organic field-effect transistors (OFETs), are thin-film devices. This concept enables the fabrication of electronic devices on plastic, flexible and transparent substrates broadening the spectrum of potential applications.

This section describes the organic thin film deposition methods and equipment used for the purposes of this study; moreover, the structure and operation of OFETs and chemiresistors are discussed.

2.1.1. Organic thin film deposition methods

The ease of fabrication has been suggested as one of the major advantages of organic electronics. The most popular organic thin film deposition methods can be classified into two major categories; i.e. vacuum techniques and wet techniques. The former category comprises physical vapour deposition (PVD) methods, such as thermal evaporation and sputtering; the wet techniques include methods such as spin coating and, more recently, inkjet printing. Wet techniques are more favourable for the organic semiconductor industry as they can be used for the large-scale deployment of organic electronics; successful large-scale roll-to-roll (R2R) processes employ wet techniques for the deposition of various materials [41].

This section describes the two common deposition techniques, i.e. thermal evaporation and spin casting, that were used for the development of the devices presented in the following chapters.

2.1.1.1. *Thermal evaporation*

Thermal evaporation is one of the most used techniques for the deposition of thin films of metals and low-molecular weight organic semiconductors. The process is carried out in high vacuum. The source material, found in either solid or liquid phase, is placed in an appropriate holder and gets heated by electric means (filament). The material evaporates and its vapour travels a short distance in vacuum before it reaches a target surface, where it re-condenses forming a thin-film. The morphology and quality of the deposited film depends on several factors; the type and roughness of the target surface, the quality of the vacuum, the

deposition rate and the total thickness of the film have an impact on the final results. Furthermore, the temperature of the substrate has been found to play a key role in the morphology of the deposited organic semiconductors [42]. Higher temperatures do not necessarily improve the device performance; Dimitrakopoulos and Mascaro showed that the charge carrier mobility of pentacene films deposited on substrates heated at 57 °C were six orders-of-magnitude lower than that of substrates at slightly above room temperature (27 °C) [43]; considering X-ray diffraction measurements, the authors attribute the drop in mobility observed at this elevated temperature to a possibly high defect concentration due to the co-existence of two different 'phases' of pentacene: a well-ordered thin-film phase and a single-crystal phase. However, Song *et al.* have suggested that the ideal substrate temperature for the deposition of pentacene is 80 °C [44].

In the work presented here, thermal evaporation was used for the deposition of metal electrodes, employing aluminium, chromium, gold and silver, and three low-molecular weight semiconductors; i.e. tetracene, pentacene and PDI8-CN_2. Moreover, despite the general belief that polymers cannot successfully be evaporated and re-organise on a target surface, the recently introduced technique of thermal evaporation and deposition of low-density polyethylene (LDPE) as the gate insulator of OFETs was successfully tested and optimised.

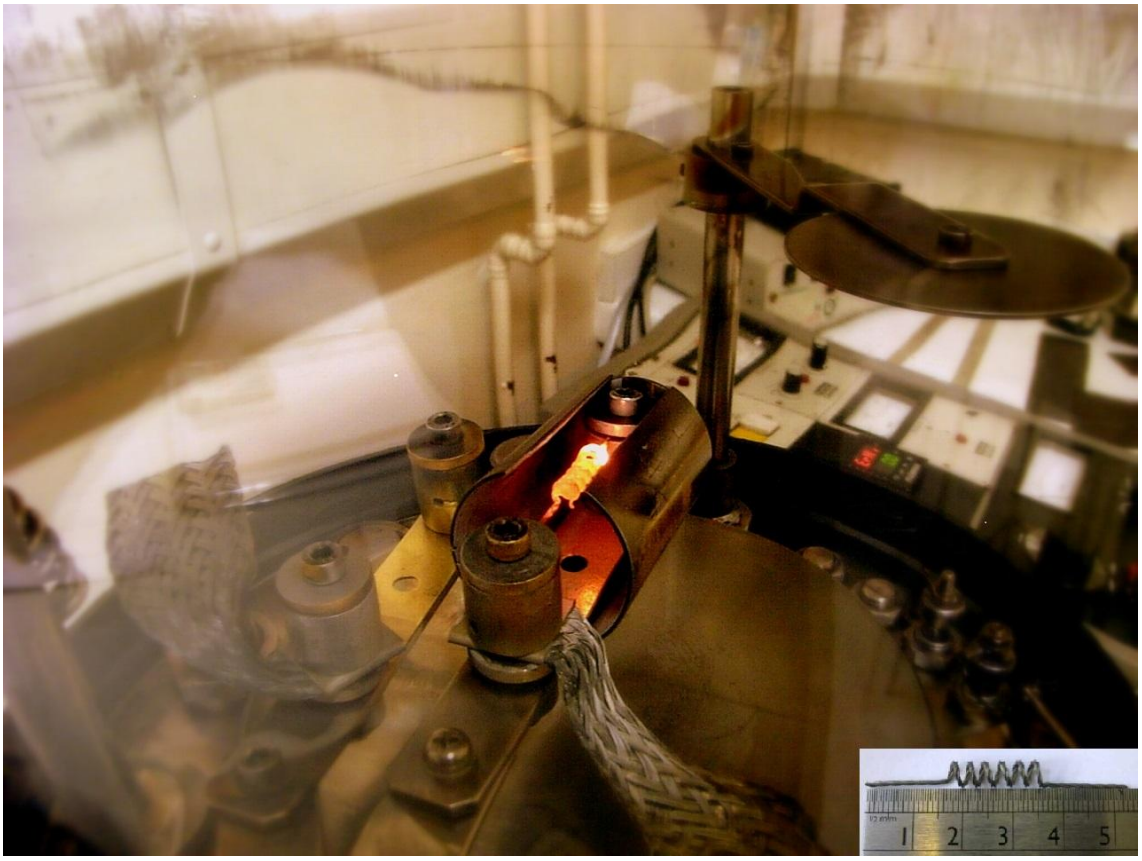

Figure 2-1 – A photograph of the thermal evaporator during aluminium deposition. The incandescent tungsten coil encompassing the aluminium source appears in the middle.

An *Edwards 306* (manual model) thermal evaporator was used for the deposition of the aforementioned materials. A removable glass bell jar, sealed by a rubber gasket, lies on the top side of the apparatus; this glass dome is kept in place by the difference between the pumped down internal pressure and the ambient pressure. All electrical feedthroughs, gauges and

vacuum and cooling piping are located at the metal bottom of the dome. A photograph of the evaporator during aluminium evaporation is shown in Figure 2-1.

The substrates are placed upside-down on specially designed steel frames based on a circular stage; the height of the stage can be adjusted so that the distance between the source and the target surface can be optimised. When patterned material deposition is required, magnetic sheets are placed on the rear side of the substrates. Then, thin ferromagnetic shadow masks are placed on the substrate surface and are kept in place by the magnetic attraction induced by the magnetic sheets on the opposite side of the substrates. An example of patterned aluminium electrodes using shadow masks is shown in Figure 2-7.

A rotary pump serves for rough pumping. Fine pumping is carried out by a mains-water- and liquid-nitrogen-cooled diffusion pump. The pumping sequence is manually controlled. The dome is initially roughly pumped down to a pressure in the range of 10^{-2} Torr. Then, the diffusion pump takes over and quickly reduces the pressure to 10^{-5} Torr. Prolonged pumping, assisted by continuous liquid-nitrogen cooling can yield pressure levels as low at 10^{-7} Torr.

The particular apparatus supports two material sources enabling the deposition of layers of two different materials (*bilayers*) without the need for venting the dome to the atmosphere. This asset can eliminate any possible contamination which could compromise the performance of the developed thin-film device. The source materials are either placed inside special tungsten 'boats' (a common practice for several metals), put in quartz crucibles surrounded by tungsten wire baskets (common for many organic materials which come in powder form) or wedged inside tungsten coils (as in the case of pure aluminium wire). The tungsten heating elements are powered by a manually-controlled variable DC voltage source, which is capable of supplying a maximum of 10 V. Typical current values for the evaporation of the materials used in this work range from 0.3 A to 2.0 A.

A quartz crystal microbalance (QCM) is placed inside the chamber, at roughly the same height as the target surfaces; its readout electronics reside outside the chamber and a thickness monitor provides information on the thickness of the deposited films. The deposition rate is calculated manually by the use of stopwatch. The calibration of the thickness monitor is necessary; apart from defining the density of the deposited material, the user must also calculate an additional calibration factor with the aid of profilometer measurements, discussed in section 3.1.3.

A shutter disc is interposed between the source material and the target surface; it is used in the beginning of the evaporation process to protect the target surface from residual volatile contaminants in the source material and undesired fluctuations in the deposition rate. When the desired deposition rate is achieved, the shutter is removed by the use of a lever and the thickness monitor is simultaneously reset to zero.

The deposition procedure varies among the materials used. The required dome pressure, source material quantity, supply current, deposition rate and final deposited thickness depend on the evaporated material and the intended thin-film device. These parameters are discussed in the respective sections below.

2.1.1.2. *Spin coating and drop casting*

Spin coating has been used for decades in the microelectronics industry; its main use has been the deposition of photoresist for the needs of photolithography. In organic electronics, it is the most common method for the deposition of polymers onto substrates.

The organic material must first be dissolved in an appropriate solvent. The concentration of the solution is usually quoted in milligrams of dissolved substance per millilitre of solvent (mg/mL). The dissolution can be assisted by heat and agitation using a magnetic stirrer. The selection of the solvent is crucial for the properties of the deposited film and, consequently, the performance of the fabricated devices [45]. One of the most important properties of a solvent is its volatility; when a solvent evaporates slowly, it allows more time to the deposited OSC molecules to organise into crystalline domains. The resulting increase in *crystallinity*, is usually desirable as it typically enhances the charge carrier mobility.

The substrates are placed onto a small turntable, known as the *chuck*. In the centre of the chuck, there is a pipe connected to a rotary vacuum pump; the substrates are kept in place by the force exerted by the vacuum. The chuck is usually placed in the middle of a cavity made of *polytetrafluoroethylene* (*PTFE*), also known as *Teflon*. A transparent lid covers the cavity and prevents splashing; the lid typically has a small opening on top of the chuck. The cavity is usually purged with dry nitrogen during the spin coating in order to eliminate the effects of ambient oxygen and moisture on the deposited thin films.

A small quantity of the solution is cast onto the substrates through the opening of the lid with the aid of a pipette. The casting can be done prior to the onset of spinning (static deposition) or during the spinning (dynamic deposition).

An electronic controller allows for adjustments of the rotational speed of the chuck, the spin time and, sometimes, the acceleration. Multiple phases of spin coating can usually be defined; two-phase processes are common, with an initial slow spin being succeeded by a faster one. The rotational speed is usually expressed in revolutions per minute (rpm).

The thickness (t) of the deposited film is a function of the rotational speed of the substrate (ω), the concentration (c) and the viscosity (η(c)) of the solution:

$$t \propto \frac{c\eta(c)}{\sqrt{\omega}} \tag{2.1}$$

The proportionality constant depends on the solvent, the temperature, the type of the substrate and other factors. Usually, profilometer measurements, discussed in section 3.1.3, are conducted for the quantification of the thickness of the deposited film and the optimisation of the concentration, speed and time parameters.

In this work, spin coating was used for the deposition of thin films of P3HT and PBTTT, discussed in sections 2.5.4 and 2.5.5. The solvents used, the solution concentrations and the exact spin coating conditions are discussed in the device preparation sections of the respective chapters. The typical values of concentration were 5 to 10 mg/mL and those of rotational speed were 1000 to 4000 rpm.

2.1.2. Organic field-effect transistors (OFET)

Organic field-effect transistors (OFETs), also known as organic thin-film transistors (OTFTs) share the same structural and operational principles with the inorganic thin film transistor (TFTs). As discussed in section 1.2, OFETs can be used as versatile gas sensing transducers. Their structure and operation are discussed in this section. Details on the fabrication and characterisation of OFETs are given throughout Chapter 5 and examples of their exploitation in gas sensing experiments are discussed in sections 7.3 and 7.4.

In the common, *bottom-gate/top-contact* architecture, illustrated in Figure 2-2 and adopted for all fabricated devices discussed in the following chapters, a thin film of a semiconductor is deposited on top of the *gate stack*. The gate stack consists of a conductor, i.e. usually a metal, doped silicon or a conducting oxide, and an insulating layer which separates the conductor from the semiconducting film; the metal electrode is usually simply referred to as the *gate* (*G*), while the insulator is known as the *gate dielectric*.

On top of the semiconductor, two patterned metal (or other conducting material) electrodes are deposited; the electrodes are known as the *source* (*S*) and the *drain* (*D*) of the transistor. In the devices presented in the following chapters, the source and drain electrodes have the same geometry and can, in principle, be swapped. As discussed in section 2.6.1, the manual alignment of the evaporation shadow masks can lead to unintentional asymmetries, which can effectively differentiate the two electrodes.

The area between the source and drain electrodes is referred to as the channel of the transistor, its *length* (*L*) is the distance between the electrodes and its *width* (*W*) is the width of the electrodes. Figure 2-3 shows an SEM image of the cross-section and the surface of the channel region of a pentacene OTFT with top gold contacts.

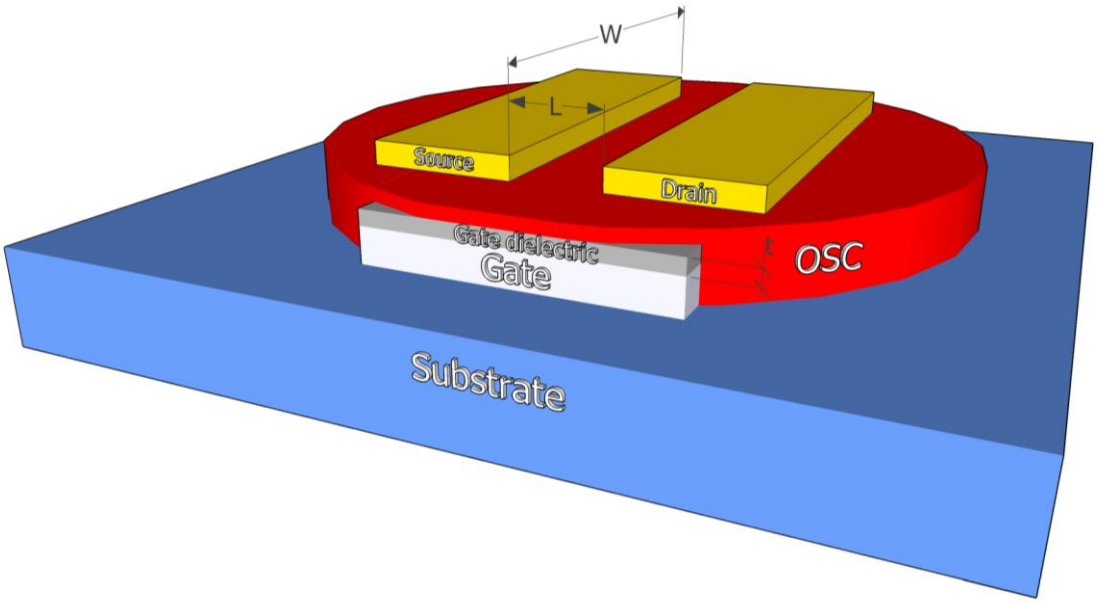

Figure 2-2 – Graphical representation of a bottom-gate/top-contact OFET. Typical values for the fabricated devices discussed here: L: 5 µm to 10 µm, W: 1 mm to 2 mm and t: ~6.5 nm (for aluminium oxide) / 100 nm to 300 nm (for silicon dioxide) 25 nm to 400 nm (for low-density polyethylene).

2.1.2.1. *MISFETs, TFTs and threshold voltage*

In a typical TFT configuration, the source is grounded and the gate and drain voltages are expressed with respect to the source voltage; i.e. $V_{GS}=V_G-V_S$ and $V_{DS}=V_D-V_S$, respectively. TFTs are voltage-controlled devices which typically operate in accumulation mode; this comes in contrast to the inorganic metal-insulator-semiconductor field-effect transistors (MISFETs) that usually operate in inversion mode. The accumulation and inversion terms refer to the charge carriers which populate the channel area and create a conduction path between the source and the drain of the device.

For instance, in an n-type silicon MISFET, the source and drain regions are made of n-doped silicon, whereas the silicon bulk is p-doped; when no gate bias is applied, the source and the drain are electrically isolated due to the presence of two p-n junctions placed back-to-back. The application of a positive gate voltage repels the majority charge carriers (holes) and attracts the minority carriers (electrons) at the semiconductor-dielectric interface; this action creates an inversion layer, in which the minority carriers populate the channel and form a conduction path (n-channel) between the source and the drain, effectively switching the device on.

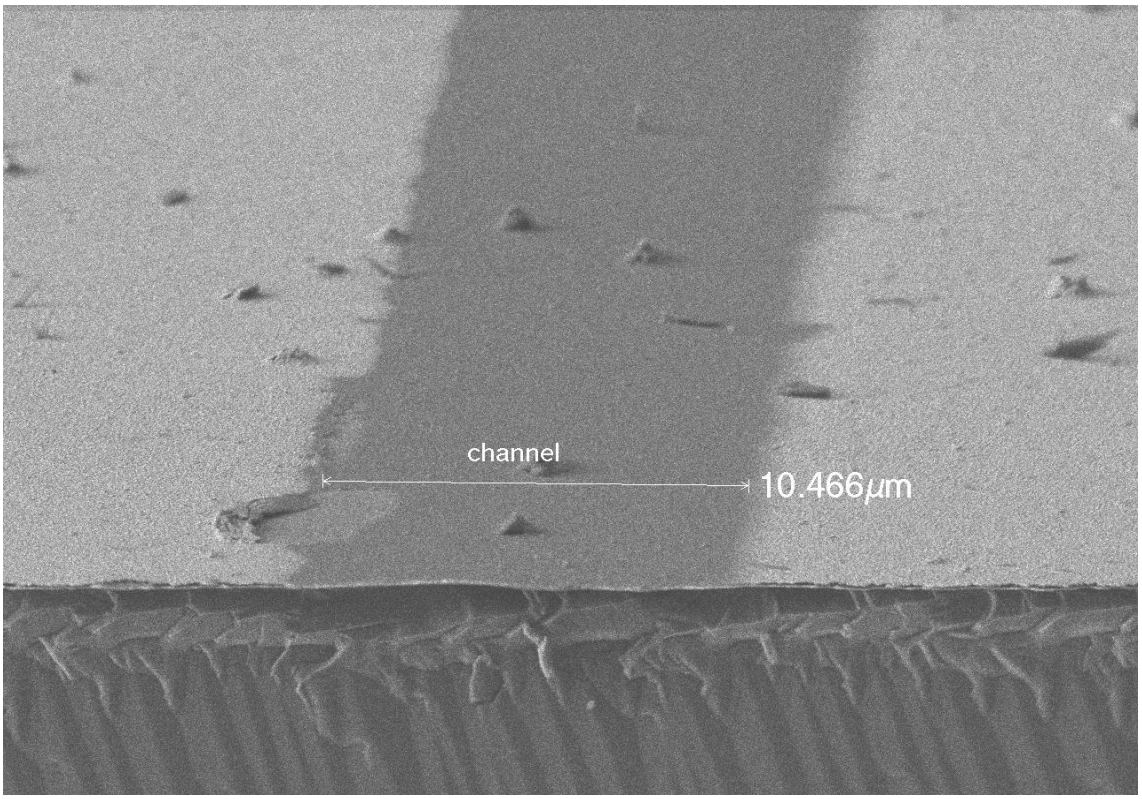

Figure 2-3 – Field-emission scanning electron microscope (FE-SEM) image of the top surface and the cross-section of the channel area of a top-gold-contact pentacene OFET based on AlO_x-LDPE dielectric. The sample was cut across the channel (longitudinal section). The two light-coloured lateral regions are the top source/drain gold electrodes and the darker region in the middle is the exposed pentacene channel having a length of roughly 10 μm. At the bottom of this image, the cross-section of the multi-layered OFET structure is shown; the silicon wafer is the thick lowest layer exhibiting sharp edges, while the overlying deposited layers cannot be clearly seen and visually separated as they tend to crumble during the sample cutting process.

Contrarily, in the case of OTFTs, the semiconductor can be intrinsic (undoped); charge carriers are injected from the source electrode into the bulk of the semiconductor and the application of a gate voltage of the appropriate polarity accumulates the injected carriers at the

semiconductor-dielectric interface. Gate voltage can modulate the current which flows through the channel, known as the *drain current* (I_D), by effectively controlling the amount of charge carriers present in the channel. OTFTs employing semiconductors which are capable of transporting electrons (*n-type*) are called *n-channel* transistors and respectively, those employing hole-transporting (*p-type*) semiconductors are known as *p-channel* transistors.

In MISFETs, the minimum gate voltage which can induce strong inversion at the semiconductor-dielectric is known as the *threshold voltage* (V_{th}) of the transistor [46]; above this voltage the device is capable of conducting 'substantial' drain current. Regarding OTFTs, the physical meaning of V_{th} was debated in the early days of organic electronics [47]; nevertheless, V_{th} is now widely accepted as an important concept that rationalises the operation of OTFTs, as explained below.

2.1.2.2. *Linear and saturation regions*

When gate voltage exceeds the V_{th} value, the conduction path (channel) has been formed. Both the gate (V_{GS}) and drain (V_{DS}) voltages control the drain current; their values determine the mode (region) of operation. Considering an n-type OTFT, when $V_{GS} > V_{th}$, there are two regions of operation :

a. when $V_{DS} < V_{GS} - V_{th}$ the transistor operates in the *linear region* and I_D is described by:

$$I_D = \mu C_i \frac{W}{L}\left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right) \quad (2.2)$$

where μ is the charge carrier mobility, C_i is the capacitance per unit area of the gate dielectric, W and L are the width and length of the channel, respectively.

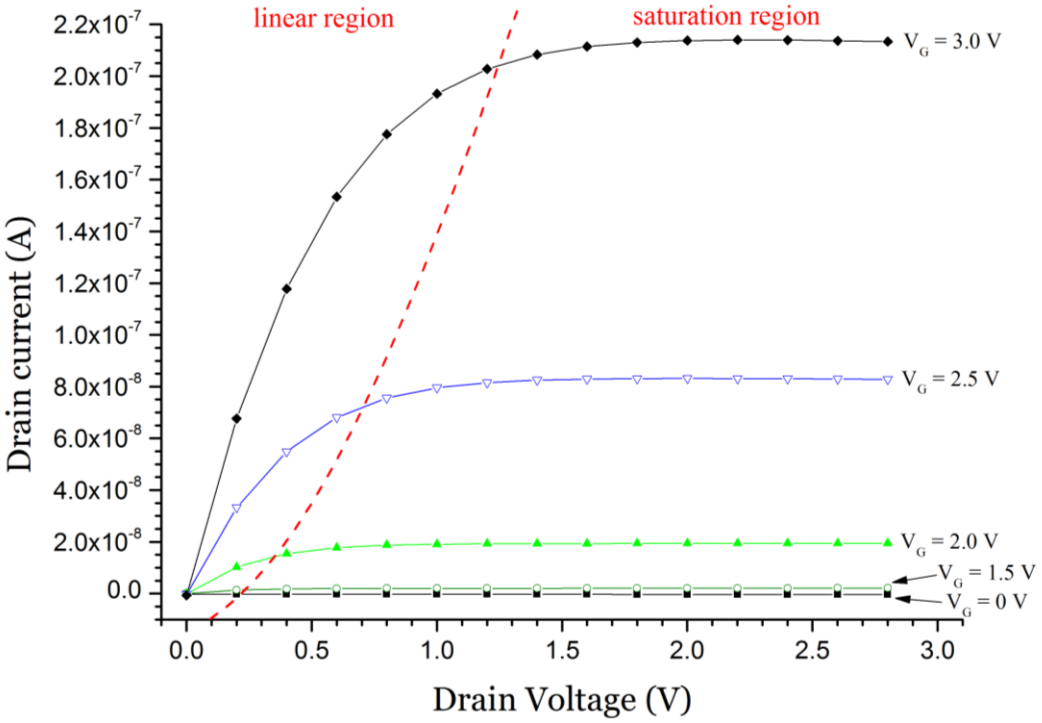

Figure 2-4 – An example of output characteristics of a typical enhancement-mode (normally-off) n-type OFET for different gate bias. The dashed red line illustrates the transition from the linear to the saturation regions.

b. at a given V_{GS} and as V_{DS} increases, the voltage difference between the gate and the drain electrodes is minimised; the field effect at the drain end of channel weakens and this effectively reduces the amount of charge carriers and shrinks the channel at this side. When $V_{DS} > V_{GS} - V_{th}$, the amount of charge carriers reaches a minimum at the drain end; this phenomenon is known as *pinch-off*. At pinch-off, the maximum drain current is limited (saturates) and can only be controlled by the gate voltage; in this case, the transistor operates in the *saturation region* and I_D is described by:

$$I_D = \mu C_i \frac{W}{2L}(V_{GS} - V_{th})^2 \tag{2.3}$$

The electrical characteristics of OTFTs are conventionally illustrated as either output or transfer characteristics. The output characteristics are plotted as drain current versus drain voltage at a constant gate voltage; usually the same drain voltage sweep is applied for different fixed gate voltage values, as shown in Figure 2-4. Conversely, the transfer characteristics are plotted as drain current versus gate voltage at a constant drain voltage; the saturated transfer characteristics, measured at a relatively high drain voltage are of great interest for the extraction of other parameters. An example is given in Figure 2-5. More details on the characterisation methodology are given in section 3.3.

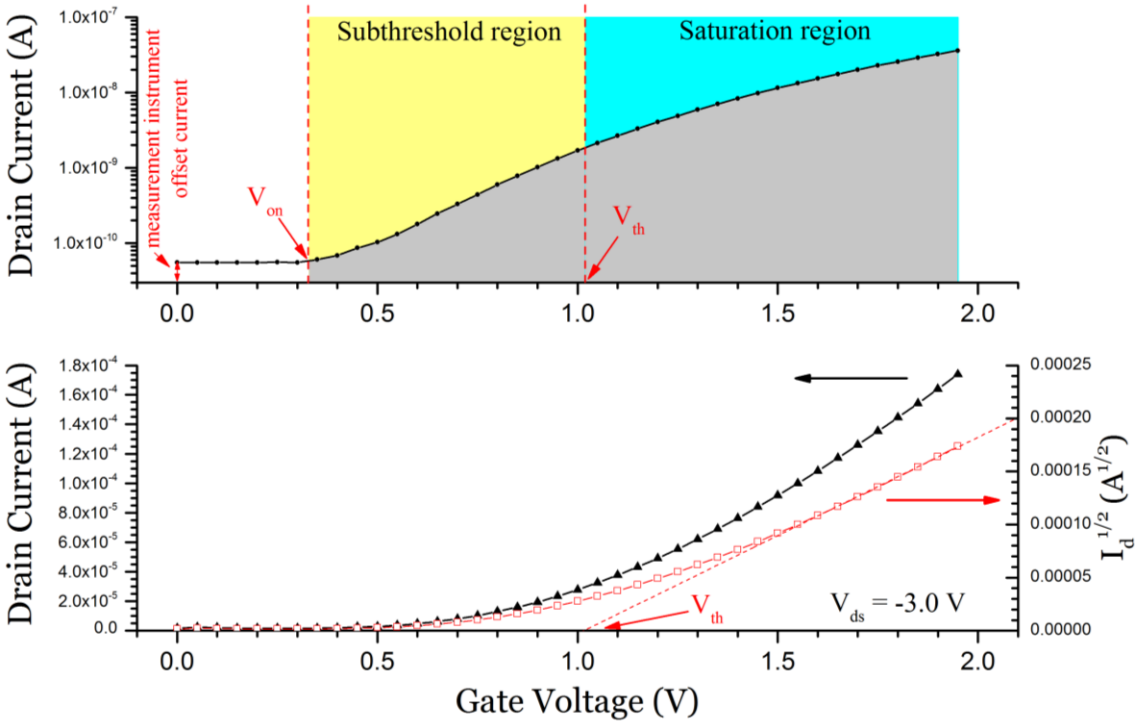

Figure 2-5 – An example of transfer characteristics of a typical enhancement-mode (normally-off) n-type OFET. Top: semi-log plot of drain current versus gate voltage, indicating the offset current (artefact) of the measurement instrument, the onset voltage (V_{on}), the threshold voltage (V_{th}) and the subthreshold and saturation regions; the linear region is not shown in this graph as the saturation condition, $V_{DS}>V_{GS}-V_{th}$ is always met over the entire gate voltage range. Bottom: The same data plotted in linear scale (black triangles) and as square root of drain current (red squares) versus gate voltage; the dashed red line indicates the simple linear regression fit used for V_{th} extraction. More details on parameter extraction are given in section 3.3.2.

2.1.2.3. *Subthreshold region*

Both eq. (2.2) and eq. (2.3) imply that I_D equals zero for $V_{GS} = V_{th}$; in reality, none of these equations can describe the operation of an OTFT when $V_{GS} \leq V_{th}$. When this condition holds true, the OTFT operates in the subthreshold region and I_D is described by [48]:

$$I_D = \mathrm{K}\mu C_i \frac{W}{L}\left(1 - \mathrm{e}^{-\mathrm{qV_{DS}/kT}}\right)\mathrm{e}^{\mathrm{qV_{GS}/nkT}} \tag{2.4}$$

where K is a constant that depends on the employed materials and the device structure, k is the Boltzmann constant (~1.3806 × 10^{-23} m^2 kg s^{-2} K^{-1}), q is the elementary charge, T is the temperature and $\mathrm{n} \geq 1$ is the ideality factor.

The subthreshold characteristics are usually plotted as the logarithm of drain current versus gate at a constant and relatively large drain voltage. A useful quantity is the inverse subthreshold slope, also known as subthreshold swing (S):

$$\mathrm{S} = \frac{\partial \mathrm{V_{DS}}}{\partial \log \mathrm{I_D}} \tag{2.5}$$

The subthreshold swing is proportional to the ideality factor according to:

$$\mathrm{S} = \mathrm{n}\frac{\mathrm{kT}}{\mathrm{q}}\ln 10 \tag{2.6}$$

This quantity typically expressed in units of *mV/decade*; this expression describes the gate voltage change required for an order-of-magnitude change in drain current.

At room temperature (293 K) eq. (2.6) writes:

$$\mathrm{S} = \mathrm{n}\ 57\ \mathrm{mV/decade} \tag{2.7}$$

For an ideal transistor and in the absence of traps, n=1; however, typical swing values for OTFTs are in the range of 0.5 to 5 V/decade [48]. Subthreshold voltage is of great importance for the study of trap densities at the semiconductor-dielectric interface; variants of eq. (2.6) account for the capacitance of the gate dielectric and the trap density. These equations are used for the comparison between different gate stacks; more details are given in section 5.2.2.3.

2.1.3. Organic chemiresistors

Two-contact organic semiconductor devices can be used as resistive gas sensing transducers, known as *organic chemiresistors*; there are numerous demonstrated examples of sensing with chemiresistors in the literature [15]. In this work, organic chemiresistors were used for the delivery of the humidity sensing tests described in section 7.2. Their structure and operation are discussed in this section.

Chemiresistors are devices of much simpler design as compared to OTFTs. In the case of a top-contact chemiresistor, a thin film of an organic semiconductor is deposited onto an insulating substrate and two patterned electrodes, made of metal or other conducting material, are deposited on top of the semiconductor. Conversely, in a bottom-contact chemiresistor, illustrated in Figure 2-6, the metal electrodes are first deposited onto the substrate and then, the semiconductor on top of them; this design can also be employed as the foundation for the development of water-gated OTFTs, as discussed in section 2.4.6.

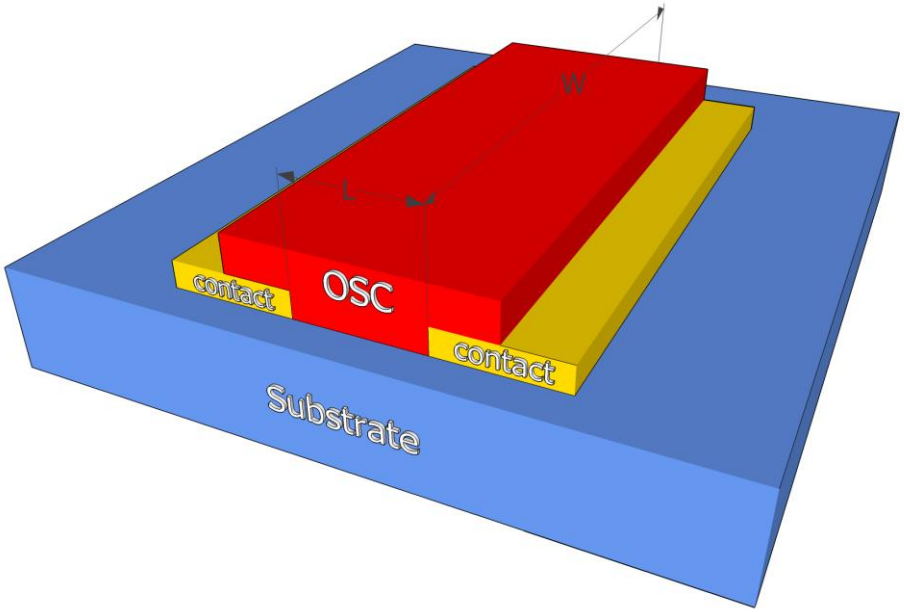

Figure 2-6 – Graphical representation of a bottom-contact chemiresistor. Typical values for the fabricated devices discussed here: L: 5 μm to 10 μm, W: 1 mm to 2 mm.

In the absence of a gate electrode, the conduction of a chemiresistor exclusively hinges on the conductivity of the semiconductor film and the efficient injection of charge carriers from and to the metal electrodes. A detailed discussion on charge carrier injection from metal electrodes is given in section 1.5.1.

The total resistance (R) of a chemiresistor writes:

$$\mathrm{R} = R_c + R_{ch} \tag{2.8}$$

where R_{ch} is the resistance of the channel between the two electrodes and R_c is the sum of the two contact resistance terms.

In spite of their structural simplicity, organic chemiresistors can be employed in various applications; in particular, there are numerous published examples that demonstrate chemiresistors as effective vapour sensing transducers [15, 49].

2.2. Substrates

The device substrate, apart from providing mechanical support to the device, can determine the properties of the overlying deposited layers and play a functional role in the operation of the fabricated device. This section briefly discusses the types of substrates used in this study and the substrate preparation methodology.

2.2.1. Silicon

Silicon substrates are a common solution for the development of organic semiconductor devices; their low surface roughness is suitable for the deposition of thin film of other materials. Moreover, the combination of a doped silicon wafer with a layer of thermal silicon dioxide (SiO_2), as discussed in sections 2.3.1 and 2.4.1, can serve as the gate stack of bottom-gate OFETs.

2.2.2. Quartz and fused quartz

Quartz and fused quartz substrates were mainly used in support of the spectroscopy measurements, thanks to their wide transparency range, which extends beyond the visible range limits [50]; thin films of organic semiconductors were deposited on these substrates and transmission measurements were conducted with the use of a spectrometer. More details on spectroscopy can be found in section 6.1.2.

2.2.3. Flexibles substrates

The development of flexible devices was one of the main objectives of this work. Two different types of plastic substrates were used: a foil of *polyethylene terephthalate* (*PET*) and A4-sized sheets of commercial overhead projector transparencies designed for laser printers (*Xerox Premium Transparencies*, part number: *003R98199*). The results on PET were poor, possibly due to its evident surface roughness. Nevertheless, the devices built of the laser printer transparencies exhibited comparable performance to their rigid counterparts. More details on device characterisation are given in Chapter 5 and a demonstration of vapour sensors built on flexible substrates is given in section 7.4.

2.2.4. Substrate preparation

The cleanliness of the substrates plays a very important role in the yield of the device fabrication and the quality of the fabricated devices. It was found that inadequate cleaning resulted in delamination of the deposited aluminium films; delamination of these films has been reported to occur during anodisation [51]. In this section, the substrate preparation techniques are described. All of the following procedures were performed in clean room facilities.

2.2.4.1. *Substrate cutting*

Most of the devices presented in this work were built on silicon substrates; these samples were cut from 3-inch arsenic-doped <100> wafers with a resistivity of 1-10 Ω/cm, a total thickness of 500 μm and an 100-nm-thick layer of thermally-grown oxide; the wafers were diced manually. A diamond-tipped glass cutter was used to scribe the rear (unpolished) side of the wafer with respect to its crystallographic orientation. Following that, the wafer was broken

into smaller parts by the application of manual force on both sides of the scribed line. This procedure was repeated until the silicon samples had the desired size. In most cases, the final dimensions were approximately 11 mm x 22 mm. Finally, the samples were blown with dry nitrogen for the removal of any remaining debris.

In some of the fabricated SiO_2-gated OFETs, substrates from a wafer with a 300-nm-thick thermally-grown oxide layer were used. A thicker oxide mitigates the gate-leakage-related problems which are common for thin insulators [52, 53]. This wafer was automatically cut by a dicing saw. These samples were also blasted with dry nitrogen prior to the wet cleaning procedures described below.

In the case of plastic substrates, two different materials were used; a foil of polyethylene terephthalate (PET) and common laser printer transparencies, as discussed in section 2.2.3. The latter have a special adhesion promoting coating on their glossy (top) side, thus this side was chosen for the deposition of the other layers. These soft materials were cut to the desired dimensions using either common scissors or a sharp blade. The standard size was the same as the one of the silicon substrates. For the deformation studies presented in section 7.4, substrates of a larger area of 40 mm x 40 mm were cut to match the dimensions of the syringe pumps used. More details on these measurements are given in that section.

2.2.4.2. *Alkaline solution cleaning*

All substrates were cleaned in an alkaline solution. A Petri dish containing a roughly 1:100 (v/v) solution of Hellmanex detergent in high-purity deionised (D.I.) water was placed on a thermostatically-controlled hot plate at 70 °C to 75° C. The substrates were immersed into the solution and preheated for 5-10 minutes. Then, the Petri dish was placed into an ultrasonic bath (model: *Digital Ultrasonic Cleaner UD100SH-3L*, power: 100W). The bath was filled with deionised water kept at roughly the same temperature. Due to the low power of the heater of the bath, the water was warmed in a separate kettle and then poured into the bath.

The samples were sonicated for 5 minutes. After sonication, each sample was rinsed with DI water at room temperature. Residual droplets were absorbed by touching the edge of the samples on a piece of lab wipe. The samples were finally placed in a clean Petri dish on the hot plate and left to dry completely.

2.2.4.3. *Isopropyl alcohol cleaning*

All silicon and glass substrates were further cleaned using isopropyl alcohol (IPA). The procedure is similar to the one described above. A Petri dish was filled with IPA and placed on the hot plate to get preheated at 70 °C. The previously dried samples were dipped into the warm solvent for 5 minutes. The Petri dish containing the substrates was placed in the ultrasonic bath and was sonicated for 5 minutes. It is important to keep the bath temperature well below 75°C to prevent IPA from boiling.

Similarly, the samples were rinsed with clean IPA, dried with the aid of a lab wipe and placed in a clean Petri dish on the hot plate until they had completely dried out.

2.2.4.4. *Ultraviolet light ozone cleaning*

A final ozone cleaning process was applied to all silicon and glass substrates. The samples were placed in a Petri dish and then the dish was put into an ultraviolet light ozone chamber (*Bioforce Nanosciences Inc.,* model: *UV.TC.220*).

This process took place at room temperature. The apparatus converts ambient oxygen into ozone using a mercury-vapour lamp. For the majority of the substrates, the application time was 260-280 seconds.

2.3. Gate electrode materials

In the case of electrolyte- and water-gated OTFTs, the selection of the gate electrode material has an impact on important device parameters, such as threshold voltage, charge carrier mobility and I_{on}/I_{off} ratio [54, 55]; however, in the case of conventional, i.e. dry, OFETs, the material selection is mainly made according to processability rather than functional considerations.

All OFET examples given in this work follow a bottom-gate architecture. Three different materials were used for this purpose: doped silicon, aluminium and silver. The properties of these materials are briefly discussed in this section.

2.3.1. Doped silicon

For the SiO_2-gated devices presented in the following chapters, the doped bulk of the silicon wafers was used as the gate electrode material; the wafers were arsenic-doped with a <100> crystal orientation and a resistivity of 1-10 Ω/cm.

For the delivery of electrical measurements, part of the insulating thermal oxide layer was scraped off of the silicon using a scriber; the doped silicon was typically contacted with tungsten needles.

2.3.2. Aluminium

Aluminium was used as the gate contact material for all low-voltage OFETs employing an aluminium oxide gate. It was also used as the bottom electrode material for aluminium oxide capacitors. It was thermally evaporated on silicon and plastic flexible substrates.

The evaporation source material comes in wire form. A tungsten coil was used as the heating element. Pieces of aluminium wire were wedged into the coil. The length of the aluminium wire used for each evaporation was roughly 15 cm. This quantity is adequate for the deposition of a maximum of 150 nm of aluminium film onto the target surface. The coil is connected to the power leads through insulated feedthroughs at the bottom of the thermal evaporator described in section 2.1.1.1.

As seen in Figure 2-7, the substrates were placed upside-down on a custom-made steel frame and magnetic sheets were placed on their bottom (rear) side. A thin ferromagnetic metal shadow mask was placed on the top side of each substrate and was held in place by the attraction of the magnetic sheets. These masks serve for the patterning of four 10-µm-channel OFETs per substrate.

The entire assembly, including the frame, the magnetic sheets and the substrates with the masks, was placed on a stage inside the evaporator, at a height of 100 to 150 mm above the aluminium source.

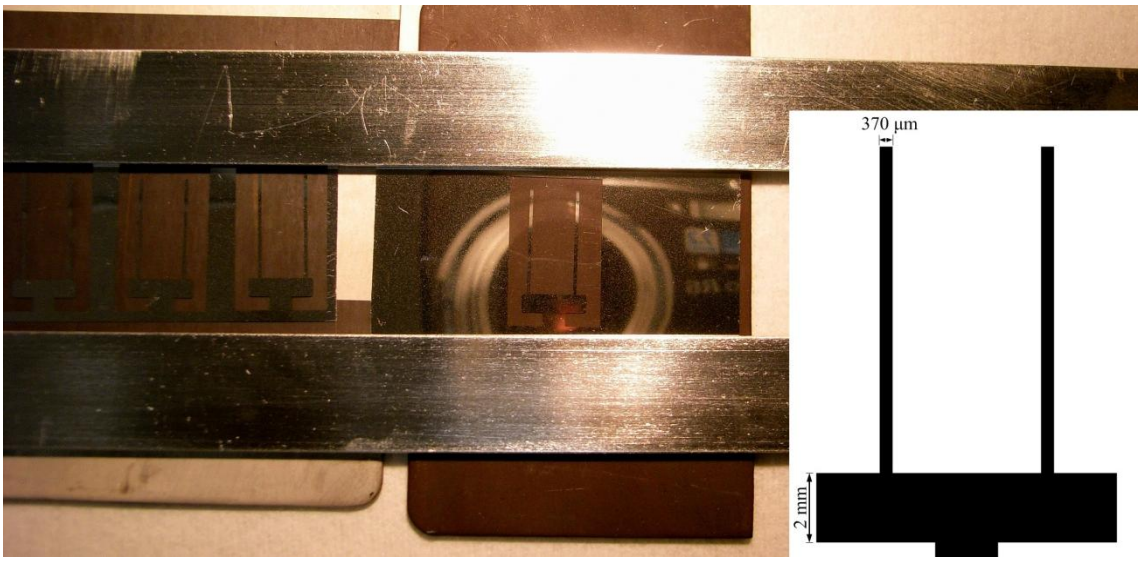

Figure 2-7 – A photograph of patterned aluminium features deposited on plastic transparent substrates. Inset: a graphical representation of the layout of the aluminium evaporation shadow mask.

The evaporator dome was pumped down to a high vacuum of < 5 x 10^{-7} Torr before each thermal evaporation process began. The typical thickness of the deposited aluminium layers was 100 nm. More details are given in the device preparation sections of Chapter 5.

2.3.3. Silver

Silver was used as a gate material for the OFETs which employed solely low-density polyethylene (LDPE) as their gate dielectric; it was also used as the bottom and top electrode material for LDPE-based capacitors.

Silver was thermally evaporated and successfully deposited on both rigid and flexible plastic substrates showing good adhesion. The raw material comes in the form of beads. A tungsten boat bearing a dimple in the middle was used as a heating element.

The deposition procedure was very similar to the aluminium evaporation process described in the previous section; shadow masks were used for the deposition of patterned features onto the substrates. The typical thickness of the silver thin films varied from 50 to 100 nm.

2.4. Dielectrics

In OFET devices, the gate dielectric physically and electrically separates the gate contact material from the semiconductor. In the most common case of enhancement-mode OFETs, the application of a bias of the appropriate polarity induces the accumulation of carriers charge at the semiconductor-dielectric interface, as discussed in section 2.1.2.1.

The properties and quality of the selected dielectric are of utmost importance for the performance and stability of the transistor. There are several factors that determine the selection of the appropriate dielectric for a device. Roughly speaking and according to the drain current equations, given in section 2.1.2, dielectrics with high permittivity can result in good OFET performance by yielding high drain currents.

Nevertheless, the dielectric layer plays a more complex role in the operation of an OFET; for instance, in bottom-gated devices, the underlying dielectric can have an impact on the morphology of the deposited semiconductor film and significantly alter its charge transport properties. Moreover, the presence and the amount of charge traps in a dielectric and at the semiconductor/dielectric interface determine important OFET parameters, such as the threshold voltage. The most common trends in the selection of dielectrics for OFETs are discussed below.

Silicon dioxide (SiO_2) has been the prevalent dielectric in inorganic semiconductor industry for decades and as such, it was inherited by the emerging organic semiconductor technology as the dielectric of choice for most of the demonstrated bottom-gate OFETs while it serves as a benchmark for all alternative dielectrics.

A newer approach is the employment of materials with relatively (as compared to SiO_2) high permittivity, known as *high-k dielectrics*. Most of these materials are inorganic oxides, such as *aluminium oxide* (Al_2O_3), also referred to as *alumina*, *tantalum oxide* (Ta_2O_5) , *titanium dioxide* (TiO_2) and *hafnium dioxide* (HfO_2); additionally, a selection of polymeric high-k dielectrics have exhibited remarkable results; these include materials such as *poly(vinyl alcohol)* (*PVA*) and *cyanoethylpullulan* (CYEPL) [56]. Despite their superiority in terms of permittivity, inorganic high-k dielectrics have been associated with high trap densities, which result in pronounced hysteresis in the I-V characteristics of FETs [57]. More information on hysteresis is given in sections 3.3.2.3 and 4.2.5.

An alternative approach is the use of polymeric dielectrics with relatively low permittivity, respectively known as *low-k dielectrics*; it has been shown that despite their low permittivity, these dielectrics, such as particular fluoropolymers, can effectively result in high OFET drain current values thanks to their low-polarity, which is closely related to lower charge trap densities [58]; this attribute can provide low threshold voltage values and low hysteresis, in conjunction with high FET mobility values, similar to those achieved in the bulk of the semiconductor.

Another widely used method is the application of self-assembled monolayers (SAMs) as a treatment for the surface of oxides. Hydrophobic silanes, such hexamethyldisilazane (HMDS) and octadecyltrichlorosilane (OTS) applied onto SiO_2 oxides result in alterations in the semiconductor grain formation and enhanced charge carrier mobility values [59]. Furthermore,

OFETs with aluminium oxide dielectric treated with phosphonic acid SAMs have also exhibited very good performance [60].

A different trend is the use of electrolytes as gate media for the development of electrolyte-gated thin-film transistors. The operating principle of these devices lies in the formation of an electric double layer (EDL) at the electrolyte/semiconductor interface; this layer effectively induces a very high capacitance, which is necessary for the accumulation of charge carriers and the channel formation. Both solid and liquid electrolytes have been demonstrated as candidate materials for the development of both p-type and n-type transistors. More recently, OFETs gated exclusively by water droplets have been demonstrated [54, 61, 62].

In this section, the dielectrics employed in this study are presented; their properties are discussed and their deposition methodology is described.

2.4.1. Silicon dioxide (SiO_2)

Silicon dioxide (SiO_2) is the best studied dielectric used as gate medium in both inorganic and organic FETs. SiO_2 is usually grown by thermal oxidation of silicon wafers. The dielectric constant of SiO_2 is 3.9 and its leakage current is very low for a thickness larger than 2 nm; for a lower thickness, quantum tunnelling becomes dominant resulting in significantly larger leakage current values [63].

In this study, silicon wafers with 100- and 300-nm-thick thermal oxide layers were used for the development of OFETs; the respective capacitance per unit area (C_i) values for these thicknesses are roughly 27 nF/cm^2 and 9 nF/cm^2. The surfaces of these dielectrics were prepared with appropriate cleaning techniques, described in section 2.2.4. In most cases, the oxide surfaces were treated with either octadecyltrichlorosilane SAMs or evaporated low-density polyethylene (LDPE); these approaches are described in sections 2.4.3 and 2.4.5, respectively.

2.4.2. Aluminium oxide by anodisation (AlO_x)

Aluminium oxide (Al_2O_3), also known as alumina, is a high-k dielectric which has been suggested as a good alternative of SiO_2. Aluminium oxide films intended for use in OFETs were first made with radiofrequency magnetron sputtering and were reported in 2002 [64]; a short time later, Majewski *et al.* demonstrated an OFET gated by an aluminium oxide layer made by anodisation of the underlying aluminium film [51]; their dielectric had low leakage current and a measured C_i of 60.7 nF/cm^2 for an anodisation voltage of 100 V. Later improvements from the same group include the growth of anodised aluminium oxide layers on plastic (Mylar) substrates; these layers had a C_i value larger than 600 nF/cm^2 using a anodisation voltage of 5 V [65]. It should be mentioned that aluminium oxide films made by anodisation are not as stoichiometric as that made by such techniques as sputtering [66]; hence, hereafter, aluminium oxide is abbreviated as AlO_x, rather than Al_2O_3.

The last approach was adopted for the development of AlO_x films on thin layers of aluminium deposited by thermal evaporation. A bespoke anodisation bath for the electrochemical oxidation of thin aluminium films, which was previously developed and demonstrated by Majewski *et al.*, was used for this purpose. The bath consists of a glass container with two thin platinum sheets covering two of its internal sides. The container is filled with a dilute aqueous

solution of citric acid (~1 mM). Up to two substrates can be anodised simultaneously; each of them is clipped with a pair of stainless steel tweezers, which is held by a crocodile clip suspended over the bath. The substrates are partly immersed into the solution so that their patterned aluminium features get wetted while the tweezers are not in contact with the solution. The surface of the substrate bearing the deposited aluminium is aligned so that it faces one of the platinum sheets while the distance between them is kept to a minimum (roughly 1-2 mm).

A constant DC current source with selectable voltage compliance powers the system. The positive terminal is connected to the dangling crocodile clip that is in contact with the thin deposited aluminium film on the substrate. The negative terminal is connected to the platinum sheets inside the bath.

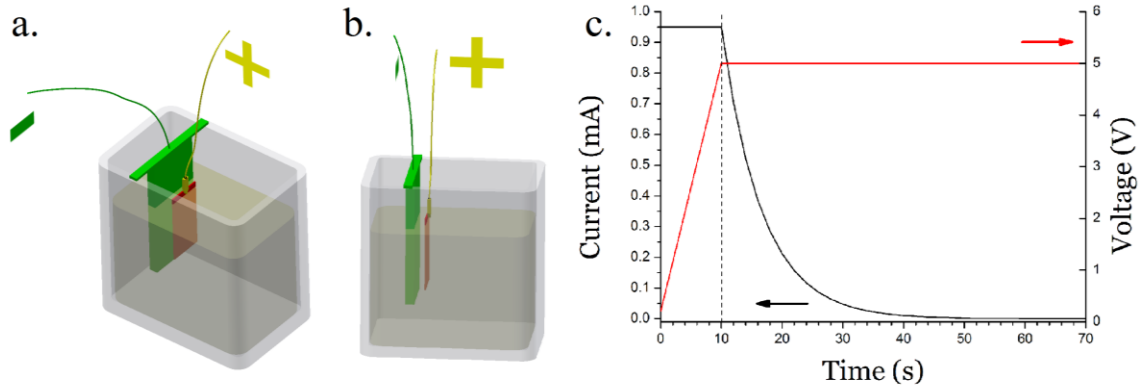

Figure 2-8 – a. and b.: a graphical representation of the anodisation bath from two different viewing angles; red features: silicon substrate, golden features: crocodile clip and cable to positive terminal, green features: platinum plate and cable to negative terminal, light yellow: citric acid solution. c. typical current and voltage curves during anodisation; the values shown are indicative.

The supply current is selected with respect to the intended current density J_{anod} and the area A of the immersed aluminium film:

$$I_{supply} = J_{anod} \times A \tag{2.9}$$

For all anodisation processes described in this work, the selected current density was roughly 9 mA/cm^2 and the maximum voltage limit was set at 5 V. The typical current application time was 75 seconds. According to the aforementioned studies, the thickness of the AlO_x can be estimated by:

$$t_{\mathrm{AlOx}} = c_{Al} V_{anod} \tag{2.10}$$

where c_{Al} is the anodisation constant of aluminium and V_{anod} is the maximum anodisation voltage. For the reported values of c_{Al} of 1.3 to 1.37 nm/V [67] and a V_{anod} of 5 V, the thickness of the grown oxide is calculated at 6.5-7.0 nm.

The impedance measurement results on capacitors based on these anodic AlO_x dielectrics treated with either OTS SAMs or evaporated LDPE layers, discussed in section 5.1, come in good agreement with the previously reported values by Majewski *et al.* for Al anodisation at 5 V, regardless of the largely different values of applied current density.

2.4.3. OTS treatment

As discussed in section 2.4, the application of self-assembled monolayers (SAMs) can enhance the morphology of the deposited semiconductor films and result in better electrical performance of the fabricated devices. Octadecyltrichlorosilane (OTS) is a common SAM treatment for OFET oxides, which provides multiple device enhancements. First, OTS passivates the –OH groups on the surface of the gate oxide, which act as charge carrier traps; this action can affect the threshold voltage of the OFET and increase the mobility of charge carriers. Second, it has been demonstrated that the semiconductor grain formation is enhanced by growing in repeatable patterns when the target surface is pre-treated with OTS [68]. Figure 2-9 a. illustrates the binding of a single monolayer of OTS to an oxide surface.

OTS treatment was first reported by Sagiv et al. in 1980 [69]. The presence of water molecules adsorbed on the surface of the oxide is essential for the binding of OTS molecules; however, excessive water content can result in polymerisation of the OTS molecules to the formation of cross-linked networks of molecules that are only partly anchored to the oxide surface [70], as shown in Figure 2-9 b. Hence, the control of the moisture present on the substrates during OTS self-assembly is very important. Moreover, apart from using OTS as a surface treatment of oxides, there are reports of metal-oxide-semiconductor (MIS) devices gated solely by a single monolayer of OTS grafted on the very thin native oxide of silicon [71].

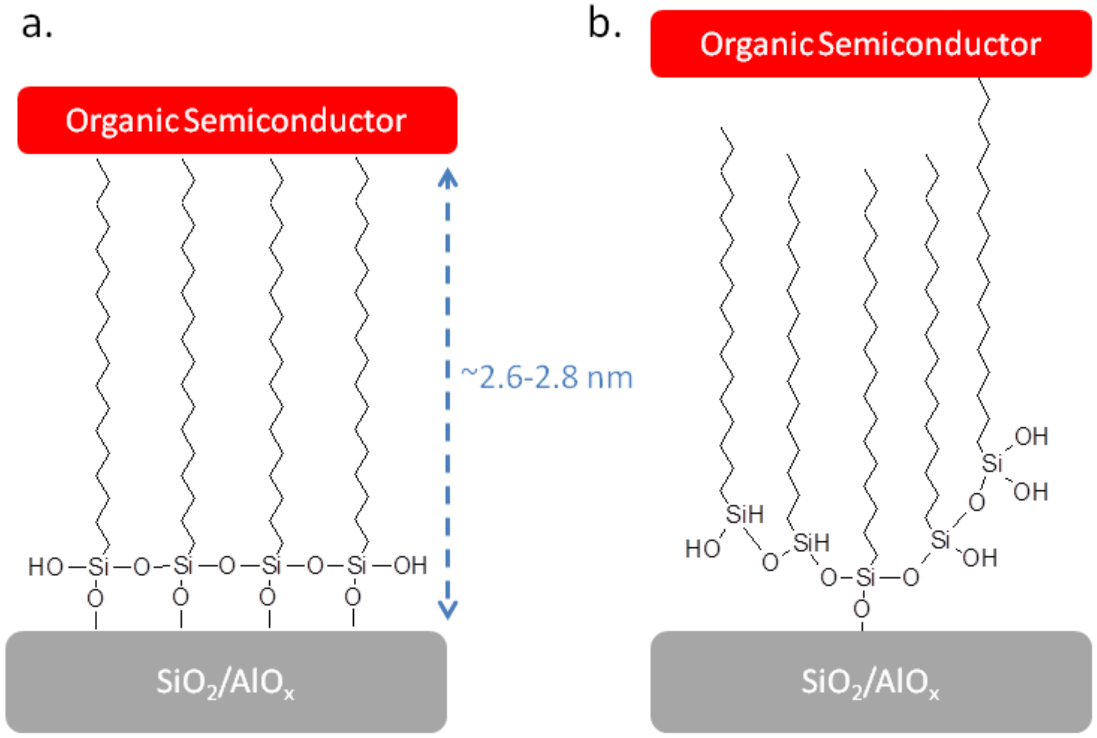

Figure 2-9 – Graphical representation of a. a single monolayer of OTS bound to an oxide surface and b. a polymerised network of OTS molecules with only one molecule bound to the oxide surface.

In the work presented here, OTS was used as a surface treatment for both SiO_2 and AlO_x dielectrics. OTS was purchased from Sigma-Aldrich (product code: *104817*) and was dissolved in cyclohexane (10 mg/mL). The substrates bearing the SiO_2 or AlO_x layers were immersed into the solution; the process was carried out in a nitrogen glove box to prevent the uncontrolled polymerisation of OTS, as mentioned above. The typical application times were 60 minutes for

SiO_2 and 10 minutes for AlO_x. After the OTS application, the substrates were rinsed with clean cyclohexane and dried on a hot plate before the deposition of the semiconductor.

2.4.4. Evaporated low-density polyethylene (LDPE)

There are very early reports of successful evaporation and deposition of polyethylene (PE); in 1965, White reported the vacuum deposition of PE by thermal evaporation at 290 °C. The use of polyethylene in the gate stack of OFETs was first reported by Chua *et al.* as a SiO_2 surface treatment that can yield electron transport in semiconducting polymers [39]. Very recently, the use of evaporated low-density polyethylene (LDPE) films as gate media for OFETs was first demonstrated by Kanbur *et al.* [72]; a C_{60} OFET gated exclusively by an LDPE layer, along with other p-type, n-type and ambipolar OFETs gated by bilayers of AlO_x and LDPE were successfully fabricated and presented in this paper. In the work presented here, pentacene and PDI8-CN_2 were successfully fabricated on both rigid and flexible substrates, employing either LDPE alone or a combination of oxide insulators and LDPE.

The LDPE was purchased from Sigma-Aldrich and was obtained in pellet form. The pellets were placed inside a quartz crucible and were sublimed in vacuum for several hours to degas. After the degassing process, the crucible was placed in an appropriate tungsten coil, inside the evaporator described in section 2.1.1.1. All LDPE evaporations were carried out in high vacuum with a pressure below 10^{-6} Torr.

The control of the evaporation temperature is crucial for the deposition of LDPE; according to the study of Kanbur *et al.* [72], as well as early studies on the evaporation of LDPE [73], the temperature must be kept below 350 °C during evaporation. In the absence of an appropriate high-temperature thermocouple, rough estimations of the coil temperature were made based on the voltage and current readings of the evaporator gauges; in this case, the coil itself was effectively used as a thermometer.

Assuming a negligible resistance on the current copper leads, due to their very large cross-section, and also assuming a uniform temperature along the tungsten coil, applying Ohm's law yields the resistance of the coil. At room temperature, its resistance (R_{ref}) was measured with a multimeter at 0.2 Ω. Then, according to:

$$R_{coil} = R_{ref} \times \left(1 + \alpha(T - T_{ref})\right) \quad (2.11)$$

where R_{ref} = 0.2 Ω is the filament resistance at reference (room) temperature, $a_{tungsten}$ is a constant which describes the sensitivity of tungsten to temperature (0.044 / °C) and T_{ref} is the reference (room) temperature (293 K). The calculated values of R_{coil} at 300 °C is 2.66 Ω, and at 350 °C is 3.1 Ω; accordingly, the resistance of the coil was kept below 2.7 Ω throughout the evaporation process.

All LDPE deposition processes were carried out in high vacuum with a pressure kept below 10^{-6} Torr. The deposition rate typically was in the 10^{-2} nm/s range. The typical thickness for OFETs gated exclusively with LDPE was 400 nm. Specific details on the deposition conditions are given in the preparation section of each investigated device in Chapter 5.

2.4.5. Evaporated LDPE as oxide treatment

The use of a combination of aluminium oxide with a thin layer of evaporated LDPE was first demonstrated by Kanbur *et al.* [72]; the combination of a high-k inorganic oxide with a polymeric surface treatment was shown to give good results for all p-type, n-type and ambipolar semiconductors, which confirms the low trap density at the semiconductor-dielectric interface.

In this work, evaporated LDPE was used as a surface treatment for both SiO_2 and AlO_x dielectrics for the fabrication of pentacene and PDI8-CN_2 OFETs. The deposition methodology was identical to the one described in the previous section; in this case, the typical thickness of the LDPE layer was 20 nm.

2.4.6. Water-gating

Kergoat *et al.* recently introduced concept of gating OTFTs with water [54]; this architecture is promising for the development of new applications, such as the sensing of waterborne species (analytes) with OTFT transducers. Indeed, the same research group has more recently demonstrated a water-gated OTFT used for DNA detection [74]; although the responses of this type of sensor were weak, this demonstration creates new prospects for water-gated OTFTs.

The operation of a water gate remains under investigation; according to Kergoat *et al.*, the operation of water as a gating medium is mainly a field-effect interfacial phenomenon, similar to that of conventional OFETs, rather than explained by electrochemical interactions in the bulk of the semiconductor [54]. In electrolyte-gated devices, a metal electrode is in contact with the electrolyte; when a bias is applied to the electrode, the mobile ions, which charge is of the opposite polarity to the applied bias, are attracted by the metal; this action induces the formation of an electric double layer (EDL) in close proximity to the electrode.

The EDL in water is believed to act as a high capacitance insulator, yielding C_i values in the range of a few $\mu F/cm^2$, which is even higher than the typical values of high-k dielectric gates; this attribute results in very low threshold voltage and substantially high drain current that allows water-gated TFTs to efficiently operate below the electrochemical window of water, i.e. 1.23 V approximately [75]. In the same study by Kergoat *et al.*, it was also shown that the selection of the gate electrode metal has an impact on the threshold voltage of the OTFT [54].

On the contrary, a drawback of electrolyte- and water-based gates is their susceptibility to high operating frequencies; mobile ions are known to move slowly, hence the time needed for the formation of an EDL is determined by their slow motion. For an efficient operation, the frequency of operation is limited to a few Hz [54].

An extensive study of water-gated devices has been conducted by our research group in the University of Sheffield; very recently, Al Naim *et al.* demonstrated the successful development of water-gated OTFTs using nanowires of organic semiconductors [62]. The electrical characterisation of these devices was performed with the I-V converter system, described in Chapter 4. Considering the peculiarities of water-gated devices, appropriate adjustments of the applied characterisation voltage and frequency were made; more details on the characterisation of these devices are given in section 4.1.2.

2.5. Organic Semiconductors

As mentioned above, organic semiconductors (OSCs) can be classified into two major categories with respect to their degree of polymerisation; i.e. *low-molecular-weight* materials, also known as *oligomers*, and *polymers*. The former are usually processed and deposited in vacuum, whereas the latter are usually prepared in solutions and deposited with methods such as spin coating or inkjet printing.

In this work, devices fabricated with three oligomers (tetracene, pentacene and PDI8-CN_2) and two polymers (P3HT and PBTTT) are presented. These materials are briefly discussed in the following sections.

2.5.1. Tetracene

Tetracene is a low-molecular-weight semiconductor that belongs to the family of oligoacenes; its molecular representation is given in Figure 2-10. Tetracene can be processed in vacuum and form polycrystalline films when deposited onto a target surface; however, much of the interest in tetracene processing lies in the development of single-crystals which have been shown to yield hole mobility values as high as 1.3 $cm^2V^{-1}s^{-1}$ [76]. Moreover, tetracene single-crystals have successfully been employed in the development of ambipolar organic light-emitting transistors (OLETs) [77]. The performance of tetracene is highly susceptible to ambient conditions, including light, oxygen and humidity; this fact impedes the development of environmentally-stable tetracene-based semiconductor devices, as discussed in section 5.4.

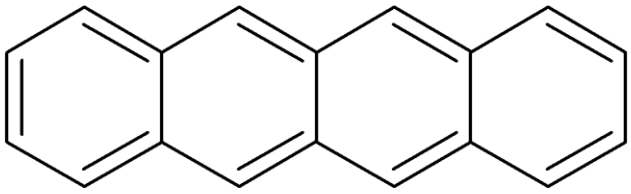

Figure 2-10 – A schematic representation of tetracene

In this study, tetracene was purchased from Aldrich ("*Benz(b)anthracene 98%*", product code: *B2403-100MG*, lot: *16596LMV*) and comes in powder form. The HOMO/LUMO levels, as given in the datasheet, are 5.4 eV / 2.7 eV [78]. The material deposition was performed with thermal evaporation in high vacuum; the powder was placed in a quartz crucible which was heated by a tungsten coil. More details on the deposition conditions for tetracene are given in section 5.4.1.1.

2.5.2. Pentacene

Pentacene is a popular low-molecular-weight semiconductor that is also a member of the family of oligoacenes; its molecular representation is given in Figure 2-11. Pentacene is usually processed and deposited in vacuum; the deposited films are polycrystalline and their morphology is favourable for the achievement of very high charge carrier mobilities; there are recently reported hole mobility values as high as 8.85 $cm^2V^{-1}s^{-1}$ [79].

Similarly to tetracene, one of the major drawbacks of pentacene is its environmental stability; significant mobility degradation is observed when pentacene OFETs operate in ambient conditions [80]. The low ionisation potential of pentacene facilitates its oxidation which results

in localisation of the conjugated π-system and, consequently, in reduced mobility. Factors such as ambient oxygen, humidity and ozone have all been associated with the mobility degradation of pentacene [81-83].

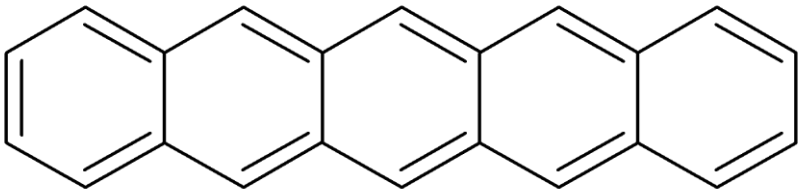

Figure 2-11 – A schematic representation of pentacene

In this work, pentacene was purchased from Sigma-Aldrich ("Pentacene triple-sublimed 99.995%", product code: *698423-500MG*, lot: *MKBC3171*) and comes in powder form. The HOMO/LUMO levels, as given in the datasheet, are 5.0 eV / 3.0 eV [84]. The material deposition was performed with thermal evaporation in high vacuum; the pentacene powder was placed in a quartz crucible which was heated by a tungsten coil. Typically, an amount of 5 to 7 mg is adequate for the deposition 100-nm-thick films; however, the majority of the grown films studied here had a thickness of 50 nm. More details on pentacene deposition are given in section 5.2.

2.5.3. PDI8-CN_2

N,N'-bis(n-octyl)-x:y, dicyanoperylene-3,4:9,10-bis(dicarboximide), known as *PDI8-CN_2*, is an low molecular weight semiconductor; its molecular representation is given in Figure 2-12. This semiconductor was first synthesised and demonstrated by Jones *et al.* along with a series of other modified *perylene tetracarboxylic diimide* (*PTCDI*) molecules with various substituent functional groups [85]; the material used in this study comes in powder form and is commercially available by *Polyera* in their *ActivInk™* series (product code: *N1200*) of organic semiconductors. PDI8-CN_2, as well as other perylene-based molecules, is known for its electron-transporting properties and it has been shown to have excellent environmental stability [85]. The HOMO/LUMO levels of this semiconductor are 6.4 eV / 4.3 eV [86].

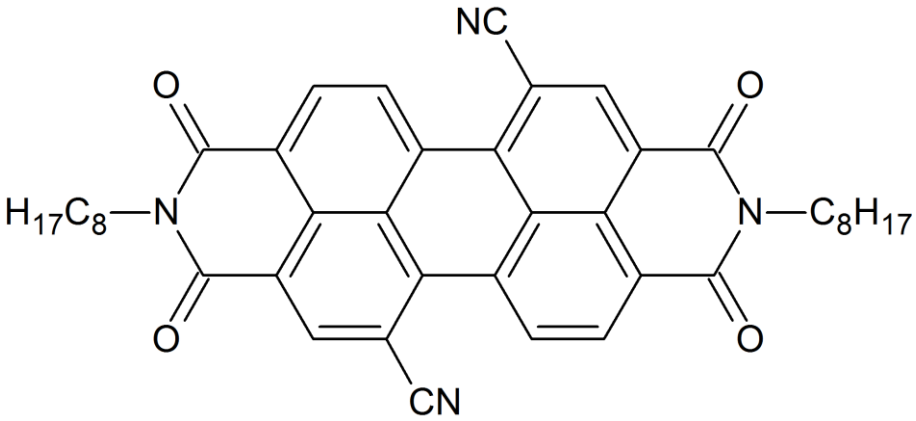

Figure 2-12 – The schematic representation of PDI8-CN_2

PDI8-CN_2 was thermally evaporated for the deposition of thin films on various dielectrics. Typically, an amount of 5 to 10 mg of substance were placed in a quartz crucible, a tungsten coil with a basket shape was used the heating element of the crucible. The typical thickness of

the deposited films was 50 nm. The exact details of the deposition conditions are given in section 5.3. Additionally, thin films of PDI8-CN_2 were deposited onto fused quartz substrates for the spectral analysis of their absorption; more details are given in section 6.1.2.

2.5.4. P3HT films and nanowires

Poly(3-hexylthiophene), known as *P3HT*, is an alkyl-substituted polythiophene; its molecular representation is given in Figure 2-13. The various polythiophene derivatives have been pioneering materials for organic electronics, being among the first polymers used for the development of functional semiconductor devices. Many of them, such as *poly(triaryl amine)* (*PTAA*), form disordered films with low charge carrier mobilities, in the range of 10^{-3} $cm^2V^{-1}s^{-1}$ [87]; however, appropriate material engineering and purification can result in ordered structures with good performance. A notable example is regioregular P3HT (rr-P3HT), initially synthesised by McCullough *et al.* in 1993 [88] and illustrated in Figure 2-14, which was the first semiconducting polymer to exhibit a hole mobility in the range of 0.1 $cm^2V^{-1}s^{-1}$ [89]. P3HT has been widely used as an OSC in thin film transistors [65, 90].

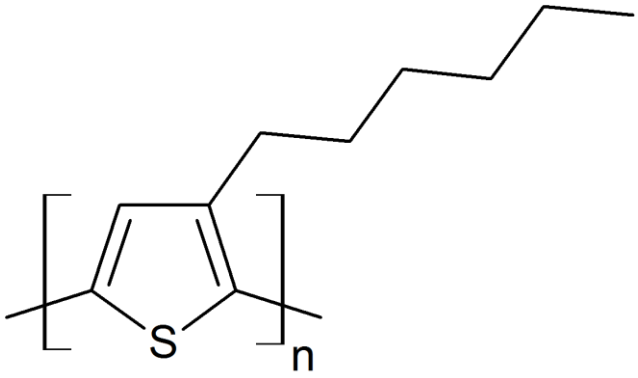

Figure 2-13 – A schematic representation of P3HT

In the past decade, a new concept has been introduced to the organic semiconductor processing and device fabrication; several research groups have demonstrated that various OSCs can be prepared in the form of organic nanowires (NWs), as reviewed by Briseno *et al.* [91]. NWs are long, needle-shaped crystals that may grow when some OSCs get subjected to suitable physicochemical treatment while in solution; for instance, this can be the a application of thermal cycles or addition of a non-solvent [91].

An interesting characteristic of organic NWs is that adjacent aromatic molecules, such as polythiophenes, stack face-to-face along the long axis of the NW, while the alkyl chains of the molecules extend across the width of the NW [92]. This molecular arrangement (π-stacking) facilitates the charge transport between adjacent molecules, resulting in high charge carrier mobilities [92]. In other words, the conductivity of nanowires is anisotropic with their long axis being more favourable for current conduction.

After preparation, NWs form stable suspensions in their growth medium and can be deposited by such techniques as spin coating or drop casting. However, the morphology of deposited films significantly differs from the smooth, uniform films obtained when casting OSCs from proper solutions. Depending on spin conditions, and NW density in the growth medium, films

may contain isolated single wires, lightly overlapping wires, or a dense multilayer NW network (mesh) [91].

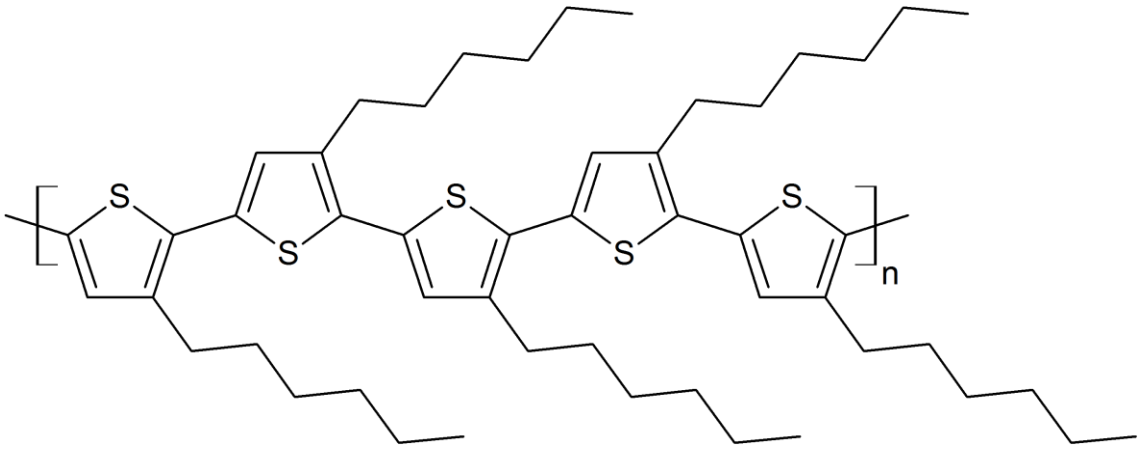

Figure 2-14 – A schematic representation of regioregular head-to-tail P3HT (rr-P3HT). Regioregularity describes polymers in which each repeat unit is derived from the same isomer.

In this work, solutions of P3HT and suspensions of P3HT nanowires were prepared and provided by our collaborating partners in the University of Cardiff; these materials were used for the development of the semiconductor devices employed in the humidity sensing tests, discussed in section 7.2. P3HT was originally purchased from Sigma-Aldrich and comes in powder form. The HOMO/LUMO levels of P3HT are 3.0 eV / 5.0 eV [93]. The conventional P3HT solution was prepared by dissolving P3HT in chlorobenzene. The P3HT NW dispersion was prepared following the whisker method by initially dissolving P3HT in anisole [94]. More details on the solution preparation and deposition conditions are given in section 7.2.2.

2.5.5. PBTTT

A variety of poly(2,5-bis(3-alkylthiophene-2-yl)thieno[3,2-b]thiophenes), known as *PBTTT*, semiconducting polymers with side chains of different lengths were introduced by McCulloch *et al.* in 2006 [95]; a schematic representation of PBTTT is given in Figure 2-15. The members of this family of polythiophenes were appropriately engineered to provide a twofold improvement. First, the incorporated fused aromatic unit effectively increases the ionisation potential; this fact results in a high environmental stability by inhibiting the oxidation of the molecule. Second, according to the authors, the rotational invariance of the fused rings promoted the formation of highly-ordered crystalline domains that practically enhance the mobility of charge carriers.

The material used in this study was poly(2,5-bis(3-hexadecylthiophen-2-yl)thieno(3,2-b)thiophene) (PBTTT-C16) and comes in powder form; it was purchased from *Ossila* (product code: *M141 PBTTT*) and was produced by *Merck* under the *Lisicon®* brand. According to the datasheet, its ionisation potential is 5.1 eV [96].

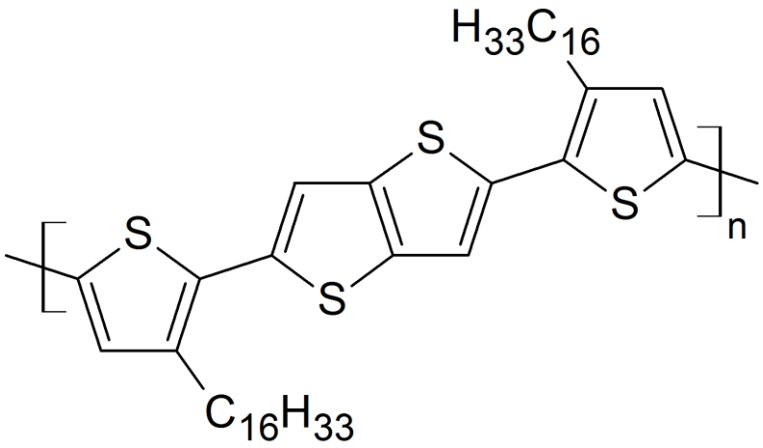

Figure 2-15 – A schematic representation of PBTTT

PBTTT-C16 was dissolved in 1,2-dichlorobenzene and was heated and stirred prior to spin coating. More details on the solution preparation and deposition conditions are given in sections 5.5.1.1 and 7.3.2.

2.6. Source-drain contact materials

The importance of the work function of the metal electrodes in the operation of organic semiconductor devices is discussed in section 1.5.1. Gold and silver were used as the source and drain contact materials; these metals are briefly discussed in this section.

2.6.1. Gold

Gold is the material of choice for the majority of the demonstrated p-type semiconductor devices. Its work function, with reported values ranging from 5.0 to 5.3 eV [87, 97], is a good match for the ionisation potential of most hole-transporting materials and thus, it serves for efficient injection of charge carriers with no or low potential barrier.

The gold used in this work comes in wire form and was thermally evaporated; a tungsten boat was used as its heating element. Shadow masks of appropriate dimensions were used for the patterning of the deposited electrodes. For the deposition of top gold electrodes on OFETs gated with aluminium oxide (AlO_x), the positioning of these shadow masks is crucial as it requires the manual alignment of a 10-μm-wide feature (channel area) with the 370-μm-wide underlying aluminium/AlO_x stripe. Misalignment results in an asymmetry in the overlap of the source and drain electrodes with the underlying oxide; in this case, considering that the parasitic capacitance is a function of the area of this overlap, the electrical properties of the source and drain electrodes will differ. More details on gold deposition are given in the respective device preparation section of Chapter 5.

One of the disadvantages in the use of gold is its low adhesion properties which might result in delamination of the deposited gold thin films. This problem can be circumvented by the deposition of few-nm-thick adhesion promoting layers made of other metals, such as titanium or chromium, prior to gold deposition. For some of the SiO_2-gated OFETs presented in this work, bilayers of aluminium and chromium were deposited on the SiO_2 surface prior to the semiconductor and gold deposition; these layers were patterned with shadow masks, having the same dimensions as the overlying gold electrodes. The preparation of these devices is discussed in section 5.5.1.1.

2.6.2. Silver

Silver was used as the top-contact material for the fabrication of polymer-gated PDI8-CN_2 OFETs; its work function (4.26 eV [77]) is very close to the electron affinity of this electron-transporting semiconductor making the injection of electrons very efficient. As discussed in section 2.3.3, silver was also the material of choice for the fabrication of parallel-plate capacitors.

The source material used was in the form of beads and was thermally evaporated using a tungsten boat. Shadow masks were used to pattern the deposited features. More details on silver deposition for the fabrication of n-type OFETs are given in section 5.3.3.1.

Moreover, it is worth mentioning that silver was successfully used in lieu of gold for the fabrication of top-contact polymer-gated pentacene OFETs; it was found that silver did not exhibit the gate-leakage problems derived from gold penetration into the insulator. However, further optimisation of the gold deposition rate overcame these problems and yielded functional devices with low gate leakage, as discussed in section 5.2.3.

Chapter 3. Morphological and electrical characterisation methodology

3.1. Morphological characterisation methods

This section gives a brief description of all the morphological characterisation methods used in support of this organic semiconductor device study. Some essential information on atomic force microscope, scanning electron microscopy, profilometry and optical microscopy follows.

3.1.1. Atomic force microscopy (AFM)

Atomic force microscopy (AFM) is a scanning probe microscopy (SPM) technique which has found very good reception in the field of thin film characterisation. Considering the importance of the surface morphology in the electrical performance of thin film devices, a good knowledge of the surface properties of a thin film allows for important correlations between the material morphology and the electrical properties of a device based on this material. The information taken from methods such as AFM can be used for the optimisation of material deposition and modification techniques, such as the thin-film deposition of thin films with thermal evaporation and the application of self-assembled monolayers (SAMs), which are both used and discussed in this study.

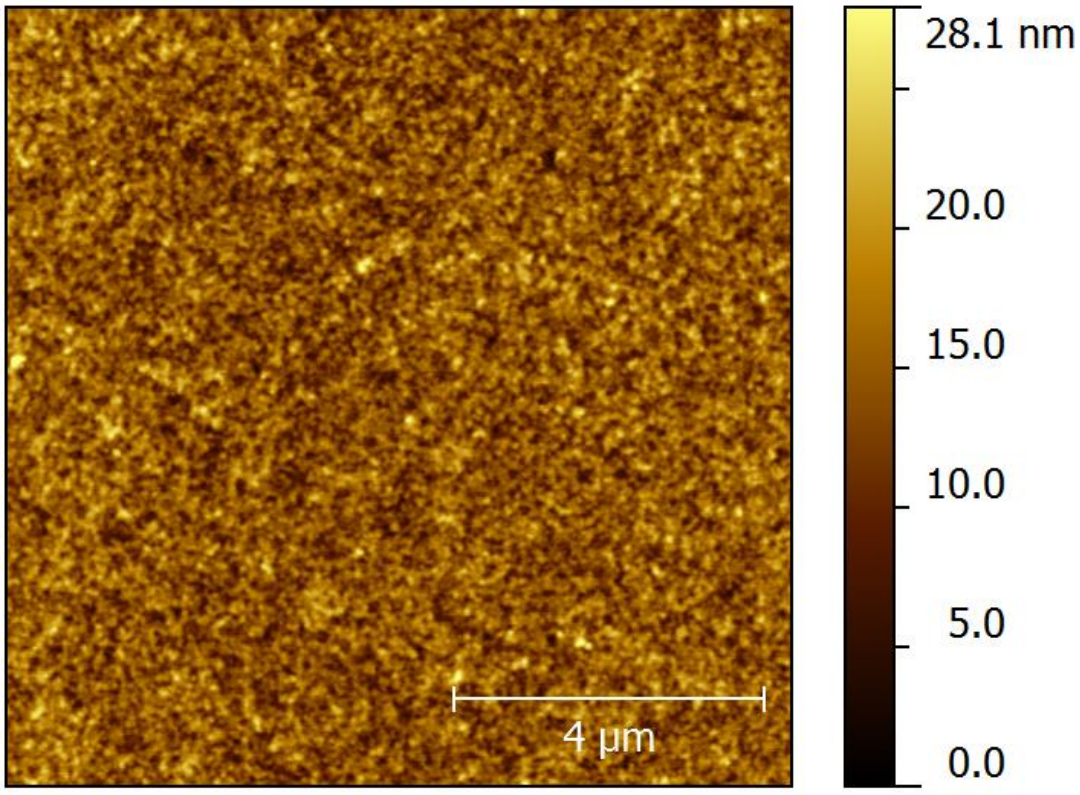

Figure 3-1 – An AFM image of a PBTTT film spin cast onto a SiO_2 surface.

In an atomic force microscope, a sharp tip is attached to the bottom side of the free end of a cantilever; this tip interacts with the surface under investigation. There are two common

modes of operation: the *contact mode*, in which the tip is continuously in contact with the surface, and the mode known as *tapping mode*, in which the cantilever oscillates at (or near) its resonance frequency [98]. Tapping mode is typically used for study of organic materials; all AFM images shown in this study were taken using this mode. A laser beam is used to read out the motion of the cantilever; the laser beam is deflected by the cantilever and sampled by a photodiode detector. AFM systems usually comprise a computer system with special control and data-processing software, which is capable of controlling and calibrating the instrument while extracting meaningful information from the measurement data.

A *Digital Instruments Dimension 3100* atomic force microscope was used for the imaging of various surfaces of the materials used in this study. An example is given in Figure 3-1. The contribution of other colleagues in AFM imaging is mentioned in the Acknowledgments.

3.1.2. Scanning Electron Microscopy (SEM)

Scanning electron microscopy (SEM) is a widely used kind of electron microscopy; a focused electron beam scans the surface of the sample under test. In the most common mode of operation, the process takes place in high-vacuum and secondary electrons, which get excited by the incident beam, are sampled by a detector. The image of the surface can be reconstructed by the readout electronics and, in modern SEM machines, by special digital signal processing (DSP) software.

A major drawback of this method is the need for conductive samples under test; non-conductive materials tend to accumulate electrostatic charge which leads to the appearance of undesired artefacts. Although this problem can be mitigated with the use of special techniques, such as the deposition of thin films of conductive materials, SEM images are rarely seen in organic electronic studies. Moreover, the soft nature of the employed material inhibits the sample preparation as these thin films are usually brittle.

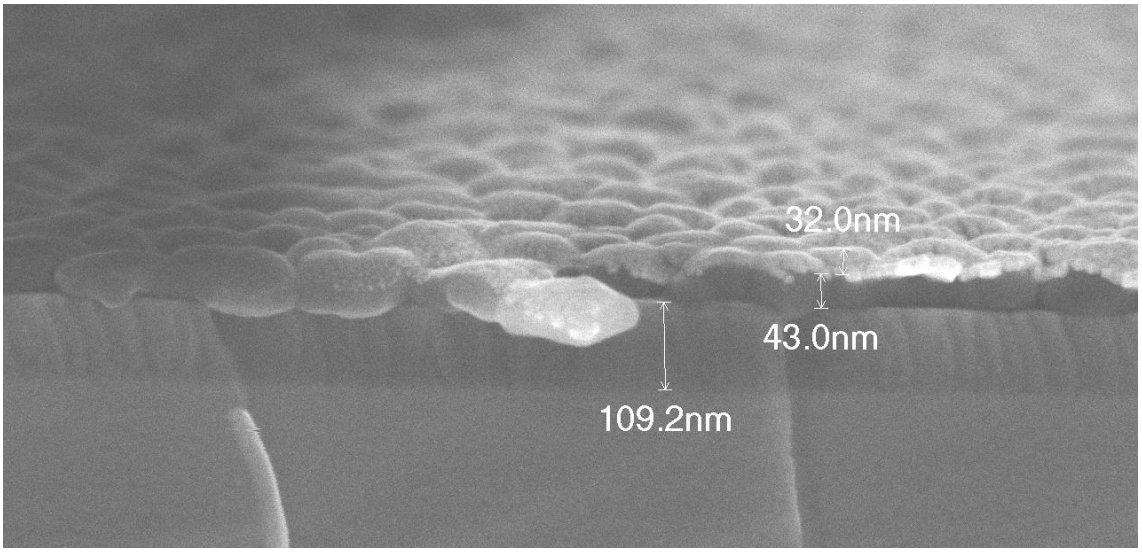

Figure 3-2 – An SEM image of the cross-section of a top-contact pentacene OFET under a top-gold-contact area.

Here, a *JEOL JSM-7401f* field-emission scanning electron microscope (FESEM) was used to image the cross-sections of a selection of devices for the precise quantification of the thickness of stacked layers of different deposited materials; this process is beyond the capabilities of a

contact profilometer, discussed in the following section. An example is given in Figure 3-2. The contribution of other colleagues in SEM imaging is mentioned in the Acknowledgments.

3.1.3. Profilometry

A contact profilometer (*Veeco Dektak³ ST Surface Profiler*) was used as an auxiliary tool for the quantification of the thickness of deposited films. The operation of this kind of instruments depends on the use of a stylus that comes in contact with and scans the surface under investigation; the motion of the stylus is converted into an electrical signal which is sampled and processed by a computer.

This profilometer was also used for the calibration of the quartz crystal microbalance (QCM) thickness monitor of the thermal evaporator. Thin films of materials were deposited onto control samples and their thickness was quantified by the profilometer; the results were used to calculate the appropriate calibration factor of the thickness monitor for a particular deposition process.

3.1.4. Optical microscopy

A standard optical microscope with a maximum magnification of 100x was used for performing quick inspections of the deposited films and fabricated devices. Its most frequent use was for the evaluation of shadow mask alignment and the detection of device fabrication problems such as shorts between the source and drain electrodes.

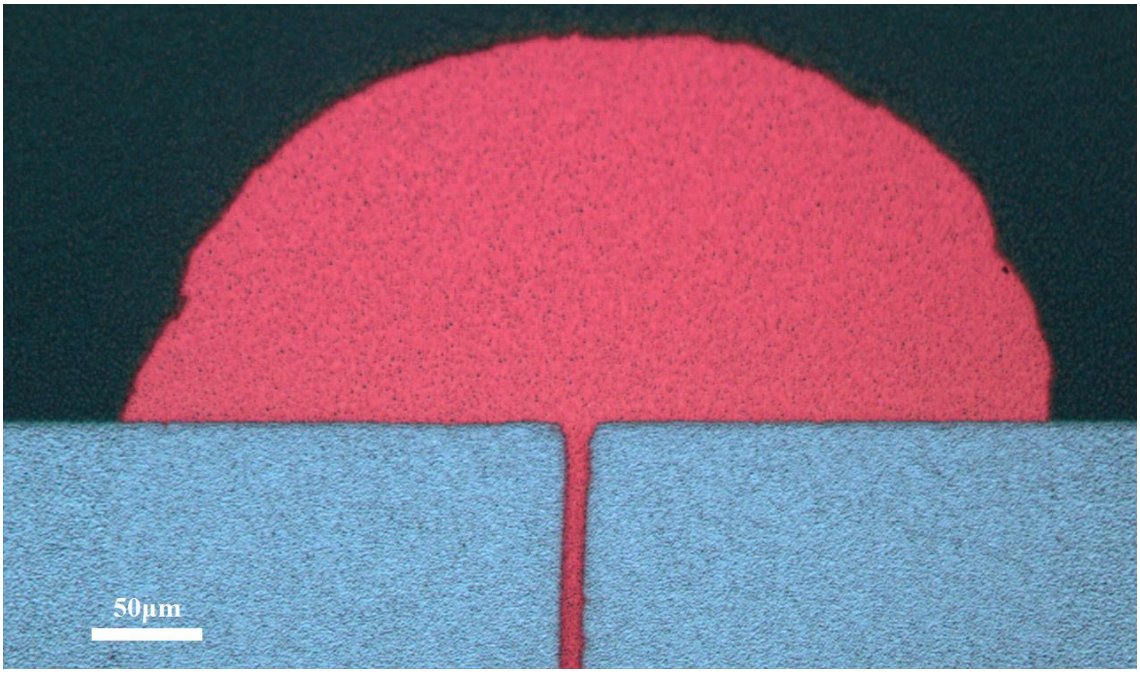

Figure 3-3 – A top-down optical microscope image of the channel area of a PDI8-CN_2 OFET with top silver contacts.

Figure 3-3 shows an example of an optical microscope image; a good alignment of the top silver electrodes with the underlying (red) AlO_x stripe is confirmed.

3.2. Impedance measurements

Impedance measurements were conducted on the three sets of capacitors, as described in section 5.1 using a *Solartron SI 1260 impedance / gain-phase analyser*. The instrument was remote-controlled by a computer running its control software (*SMaRT* v. 3.0.1).

A bespoke test rig was built for conducting the measurements. A stainless steel box served as a Faraday cage which enclosed the capacitor under test. Two *Cascade-Microtech PH100* probe positioners were also placed inside the box and contacted the capacitors with tungsten needles. Coaxial feedthroughs were placed on the chassis of the box and served for the connection of the probe positioners with the impedance analyser with the use of 50-Ohm coaxial cables. The operating frequency specifications of all employed components were orders-of-magnitude higher (in the GHz range) than the frequencies used for measurements presented here.

For all measurements, the same signal generator conditions were applied. The generated signal had an amplitude of 1 V with a zero DC offset and the applied frequency range was from 1 Hz to 10 KHz. The software calculates capacitance and resistance data which can be converted into capacitance per unit area (C_i) and leakage current density values. More information on parameter calculation, as well as the measurement results can be found in section 5.1.

3.3. OFET current-voltage measurements

The most common method of electrical characterisation of OFETs is the extraction of their *output* and *transfer characteristics*. In the former case, drain current is plotted versus source-drain voltage, whereas in the latter, drain current is plotted versus gate-source voltage. The output characteristics mainly serve for the qualitative analysis of an OFET, whereas for the quantification of other OFET parameters, the transfer characteristics are usually exploited. A new alternative method for the real-time characterisation of OFETs is described in detail in Chapter 4.

For the extraction of the output characteristics of an OFET, drain current is measured and plotted versus a drain voltage range at a fixed gate voltage. Usually, the output characteristics at various gate voltages are measured and all curves are plotted on the same graph. Figure 3-4 gives an example of the output characteristics a p-type and an n-type low-voltage OFETs.

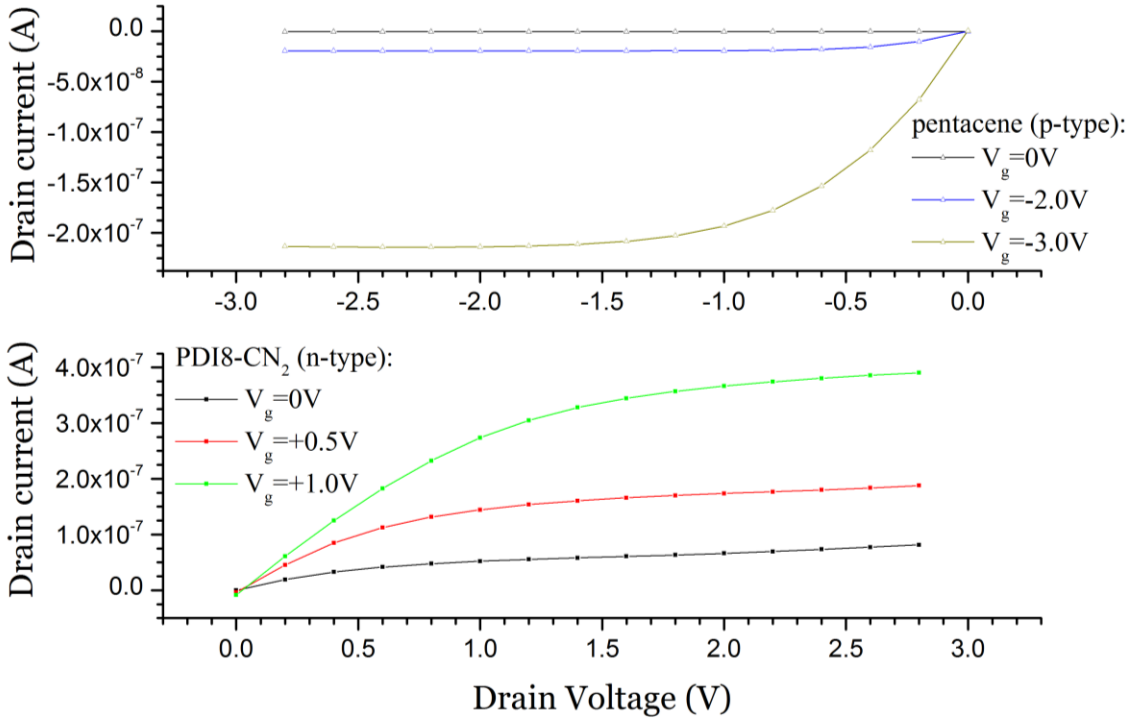

Figure 3-4 – Examples of output characteristics of OFETs based on hole-transporting (p-type) and electron-transporting (n-type) semiconductors. Top: a p-type (pentacene) low-voltage OFET. Bottom: an n-type (PDI8-CN2) OFET of the same device architecture.

The output characteristics can reveal interesting characteristics of an OFET. For instance, in the example given in Figure 3-4, from their output curves at V_G = 0V, it can be seen that the p-type OFET is a normally-off (enhancement-mode) device, whereas the n-type is a normally-on (depletion-mode) device. Moreover, in the same example, the drain current of the p-type OFET saturates as its output curves level-off as the modulus of drain voltage increases; conversely, the drain current of the n-type OFET shows poor saturation, which can be interpreted as an indication of doping. Furthermore, significant gate leakage can be indicated by the output characteristics; this can be observed at non-zero gate voltages, if the output curves and the x-axis do not intersect at x=0. Both devices in Figure 3-4 exhibit low gate leakage.

For the extraction of the transfer characteristics of an OFET, drain current is measured and plotted versus a gate voltage range at a fixed drain bias. Typically, the characteristics at a low (linear region) and a high (saturation region) drain voltage are measured.

The transfer characteristics are of great importance for the quantification of other important OFET parameters; threshold voltage, mobility and on/off ratio are typically calculated from the output characteristics of a device; detailed information on parameter extraction is given in section 3.3.2. Moreover, when plotted in $\log(I_D)$ versus gate voltage graph, the transfer characteristics can be used for the calculation of the subthreshold swing and for estimations of the trap density at the semiconductor-dielectric interface; more details on the subthreshold region are given in section 2.1.2.3 and examples of calculations on real devices are given in section 5.2.2.3

3.3.1. Equipment and methodology

There are specialised instruments for the conduct of electrical measurements on semiconductor devices available in the market; they are commonly referred to as *semiconductor parameter analysers*. These instruments are usually capable of automatically calculating several important device parameters based on user-defined OFET specifications. An *Agilent 4155C semiconductor parameter analyser* was used on PBTTT OFETs for the extraction of the results discussed in section 7.3.6.

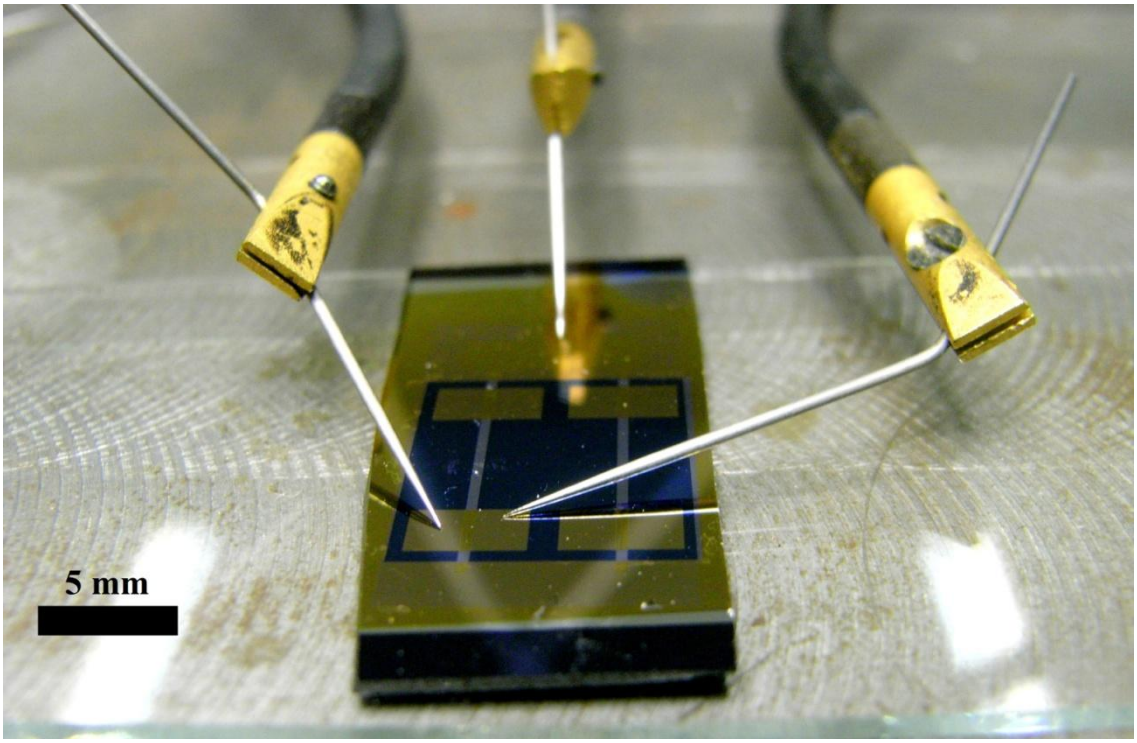

Figure 3-5 – A photograph of a substrate with four OFETs. The bottom-left device is contacted by the source-drain (lateral) tungsten needles. The common gate electrode is contacted by the tungsten needle seen in the back.

An alternative implementation is the combined use of a pair of general-purpose current-voltage source-meters. For most measurements presented in this work, a pair of *Keithley 2400 SourceMeter* instruments, connected to a computer over a GPIB bus and controlled by a custom Windows application was used. The ground terminals of both units were tied together and connected to the source of the OFET under test. One of the units controlled the gate

voltage and the other the source voltage, while measuring the gate leakage current and the drain current, respectively. This configuration was used for extracting all the output and transfer characteristics discussed in Chapter 5.

A custom-made steel stage served as a test bench for the characterisation of OFETs. Three *Cascade-Microtech PH100* probe positioners with tungsten needles were used to contact the OFETs under test. Coaxial cables were used for all interconnections; a bespoke switch box was also developed for quickly swapping between this characterisation system and the I-V converter system discussed in Chapter 4, without the need for changing any cable connections; this allowed for direct comparisons between the results extracted by these two systems.

In the accompanying software, there are separate modes for the delivery of output and transfer measurements. The test parameters are defined by the user; these include the number of sweeps per test (typically one or two), the voltage sweep range, the voltage step size, the delay between two consecutive steps and the current compliance. The data are plotted by the software and can be exported as tab-delimited text files. Only voltage and current values are exported; other parameters, such as threshold voltage and mobility can be calculated using other data analysis software; more details on OFET parameter calculation are given in the following section.

3.3.2. OFET parameter calculation

This section describes the commonly used conventions and methods for OFET parameter calculation that were applied in this study.

3.3.2.1. *Saturated Drain Current and on/off ratio*

For a normally-off (enhancement-mode) OFET, the saturated drain current ($I_{D,sat}$) is usually measured at $V_{DS} = V_{GS}$ for $V_{GS} > V_{th}$. It is a common practice to use the measured value at the maximum V_{DS} and V_{GS} of either an output or transfer characteristic curve.

The on/off ratio is a useful parameter which is defined as the ratio of the drain current in the saturation region over that in the off-state; this ratio is a measure of how effective the gating effect is. There is no standardised definition of on/off ratio; however, for a normally-off OFET, this quantity is usually expressed as the ratio of the drain current at the maximum V_{DS} and V_{GS} over the drain current at the maximum V_{DS} and V_{GS}=0, i.e.:

$$I_{on}/I_{off} = \frac{I_{D,\, V_{DS}=max,\, V_{GS}=max}}{I_{D,\, V_{DS}=max,\, V_{GS}=0}} \tag{3.1}$$

The I-V converter method, which was used in several OFET characterisation tests presented in this work, uses a different definition of on/off ratio; more information is given in section 4.2.2.

3.3.2.2. *Threshold voltage and mobility*

Threshold voltage (V_{th}) and charge carrier mobility (μ) are two parameters that are not directly measured but can be extracted from the I-V characteristics of an OFET. There are several suggested parameter extraction methods in the literature [99, 100]; these studies have shown that the use of different methods can lead to largely different calculated values. Section 4.2.4 gives examples of the use of different extraction methods based on the measurement data taken from the I-V converter system.

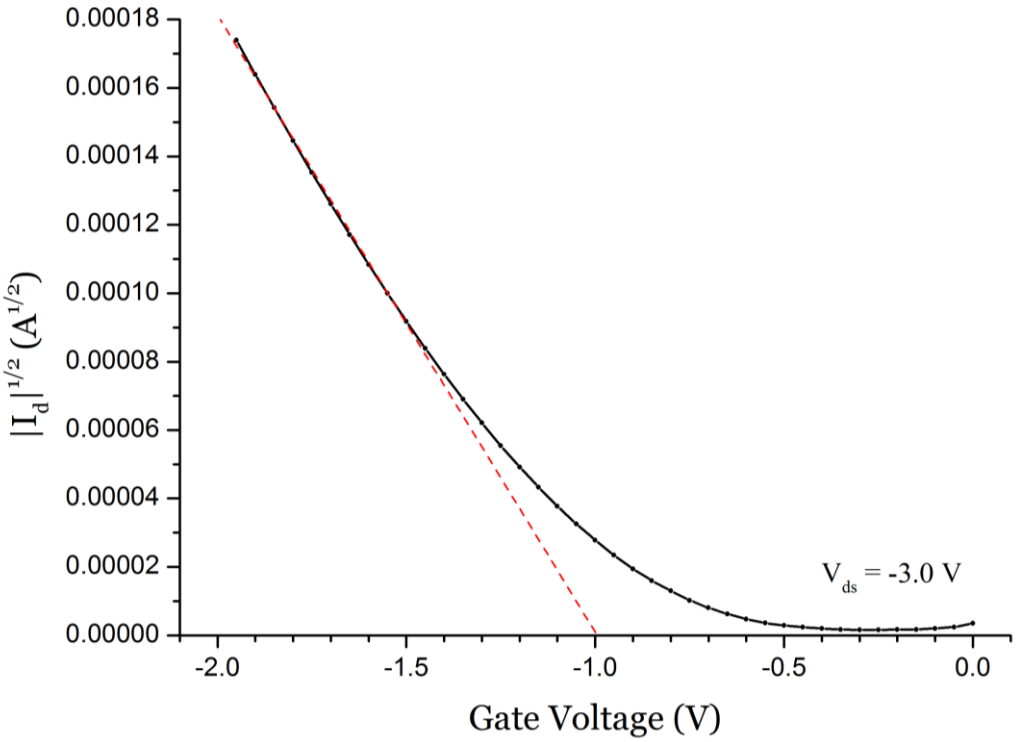

Figure 3-6 – An example of the application of ESR method. The calculated V_{th} value is roughly -1.0 V. Using this method, the selection of the measurement data range, taken into account for the application of a simple linear regression fit, has a significant impact on the calculated values. It is a common practice to arbitrarily choose this range, but this can result in significant deviations. A discussion on the data range selection and a comparative example are given in section 4.2.4.1.

A widely used parameter extraction method using conventional I-V characteristics is the extrapolation in the saturated region (ESR); this method was adopted for all V_{th} and μ calculations discussed in the following chapters. According to the ESR method, the saturated (at high V_{DS}) transfer characteristics are plotted as the square root of the modulus of drain current ($|I_d|^{1/2}$) versus gate voltage; a simple linear regression fit is applied to a data range of the curve (usually in the highest gate voltage range) and this straight line is extrapolated to the x-axis. The intercept of the straight line with the x-axis (for y=0) is the threshold voltage of the OFET; an example is given in Figure 3-6. The slope of the fit is used for the calculation of mobility; from the saturated drain current notions, described by eq. (2.3), it is derived that the slope of the fit depends on the charge carrier mobility, the capacitance per unit area (C_i) of the gate dielectric and the device dimensions (W and L) according to:

$$Slope = \sqrt{\mu C_i \frac{W}{2L}} \tag{3.2}$$

which also writes:

$$\mu = \frac{2L}{C_i W} Slope^2 \tag{3.3}$$

As eq. (3.3) signifies, a good knowledge of C_i is imperative for the calculation of mobility. The impedance measurements, discussed in section 5.1, come in support of these calculations.

More details on parameter calculation using this method, as well as the significance of the selected data range and the correction of doping effects, are given in section 4.2.4. An

example of the application of the ESR method to the saturated transfer characteristics of a low voltage p-type OFET is given in Figure 3-6.

3.3.2.3. *Hysteresis*

Hysteresis is a phenomenon which manifests itself as a short-term shift in the output and/or transfer characteristics of an OFET; the direction of the shift depends on the direction of the voltage sweep and other characterisation-related factors, such as voltage application time and the time between successive measurement points [101].

Hysteresis can usually be seen when two consecutive voltage sweeps are applied, i.e. one of increasing and one of decreasing voltage, or vice versa; the combination of the two curves appears as a loop. An example of mild hysteresis is given in Figure 3-7; in this graph, I_d values are slightly larger when drain voltage is swept from the maximum voltage down to zero (red dashed curve). In the literature, hysteresis is usually characterised as either clockwise or anticlockwise depending on the direction of the loop; nevertheless, as the direction of the loop also depends on the direction and the sequence of the applied voltage sweeps and since there are no standardised conventions that dictate how these measurements must be performed and interpreted, these terms are not used in this text.

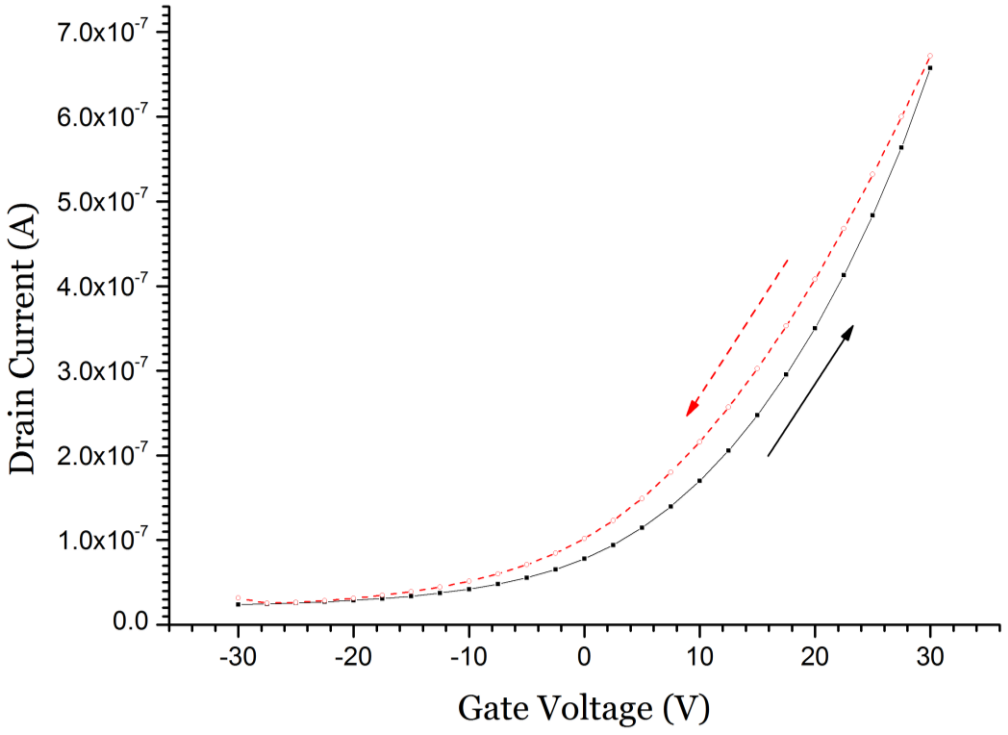

Figure 3-7 – Transfer characteristics of a PDI8-CN_2 OFET with evident hysteresis.

Hysteresis is related to the presence of traps at the semiconductor/dielectric interface, but mainly with those within the bulk of the semiconductor [102]. The IEEE standard 1620™ on OFET characterisation suggests the application of both rising (from off to on) and falling (from on to off) voltage sweeps in order the detect the presence of hysteresis [103]; however, this standard does not provide explicit suggestions on what data the OFET parameters must be calculated from.

In this study, pre-conditioning cycles including both rising and falling voltage sweeps were applied to all devices under test; however, hysteresis is not studied in the following chapters. As a convention, all parameter calculations were performed using only the measurement data taken from the rising voltage sweeps.

Moreover, section 4.2.5 introduces a new hysteresis quantification method, based on the measurement data of the I-V converter system.

Chapter 4. I-V converter method

This chapter describes the novel OFET characterisation system that was developed in support of the experiments discussed in this work. This portable system serves for the needs of real-time quantification of multiple OFET parameters; this capability is of great value for the detection of rapid parameter changes in applications such as gas sensing with OFET transducers, which constitutes one of the main objectives of this work.

In 2011, the principle of operation of this system was first demonstrated [37]. Many further technical modifications and the development of accompanying software followed this initial demonstration. As of 2013, a number of units have been built and the system has found application in other collaborating laboratories.

The operation, parameter calculation and the automated characterisation software are discussed in this chapter. The relevant circuit schematics and PCB information can be found in Appendix II.1.

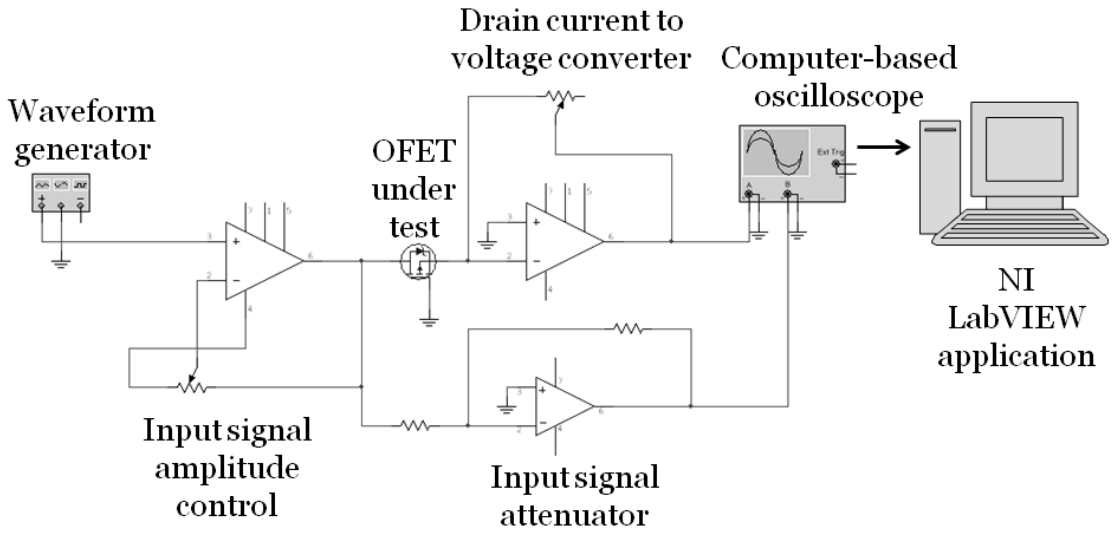

Figure 4-1 – A simplified schematic of the I-V converter characterisation system. The operational amplifier (op-amp) on the LHS acts as a non-inverting high-voltage (±45 V) amplifier of the sinusoidal signal (V_{sig}) generated by the waveform generator. The amplified signal (V_{in}) is inverted and attenuated by the op-amp at the bottom; this signal (-0.1 V_{in}) is fed into the second channel of an oscilloscope connected to a computer running a NI LabVIEW application. V_{in} drives the source of the OFET under test, while its gate is grounded and its drain is connected to the inverting input of a high input-impedance op-amp (shown on the top). The non-inverting input of this op-amp is grounded and thus, its inverting input constitutes a virtual ground. This last op-amp converts the drain current into an inverted output voltage (V_{out}) with the aid of a high-precision feedback resistor. V_{out} is sampled by the first channel of the oscilloscope.

4.1. Operation

The system is designed to rapidly extract the saturated transfer characteristics of an OFET, parametric in time, with the use of a two-channel oscilloscope; the application of a sinusoidal drive allows for the quantification of multiple OFET parameters in a fraction of a second, which serves for the needs of the detection of rapid parameter changes when OFETs are used as sensing transducers. Moreover, the selection of a sinusoidal drive facilitates the use of low-

pass filters while it enhances the long-term stability of an OFET under test by eliminating the common gate-bias stress effects; these advantages are discussed in the following section.

4.1.1. Electronics

Figure 4-1 shows the simplified circuit diagram of this system and Figure 4-2 a photograph of the actual system. This portable system is interfaced to a PC via a USB oscilloscope (*Pico Technology Picoscope 2204* or similar), which acts as both a two-channel digital oscilloscope and a waveform generator. The circuit is mainly based upon three operational amplifiers (op-amps) of different specifications. A high-voltage op-amp (*Texas Instruments OPA445AP*) is used for the amplification of the sinusoidal waveform provided by the Picoscope waveform generator (V_{sig}), which has a limited maximum voltage amplitude of ±2 V; the amplified drive signal (V_{in}) can have a maximum amplitude of ±45 V. The amplitude of V_{sig} can be controlled by the software, while the final amplitude of V_{in} is adjusted by a rotary potentiometer found on the PCB.

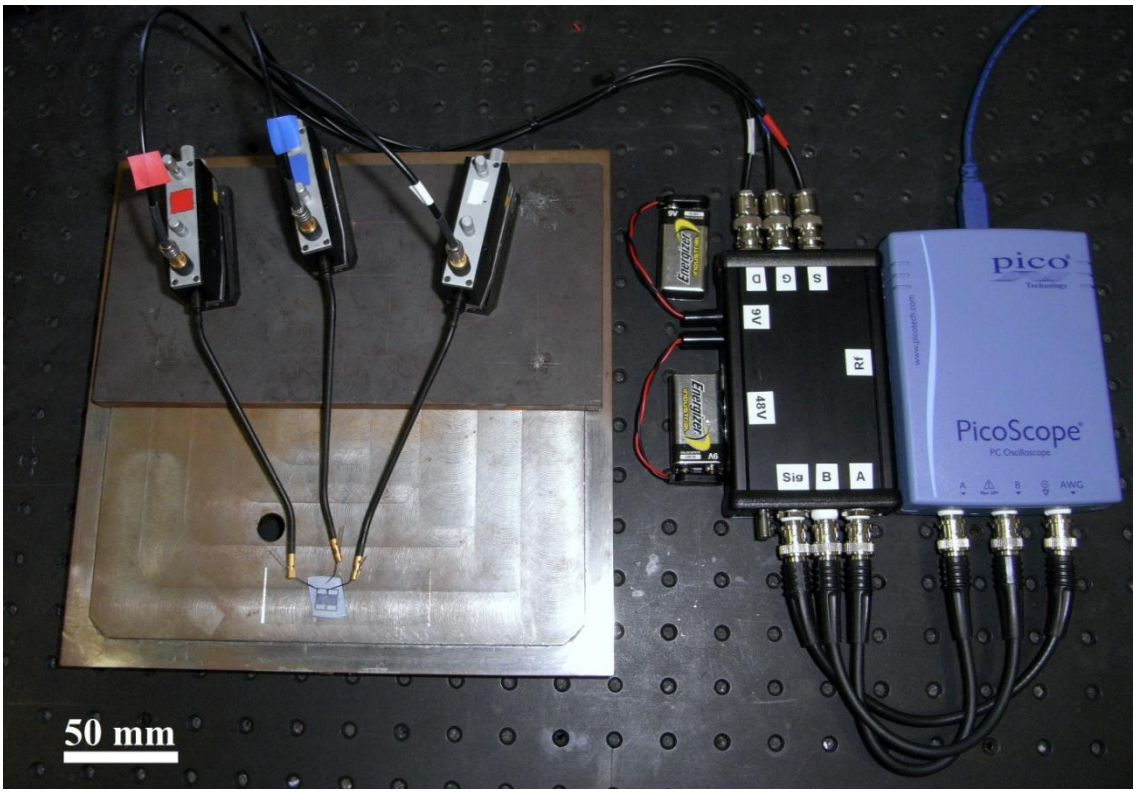

Figure 4-2 – The OFET test bench with the I-V converter system. On the LHS, a substrate with four OFETs is placed on the metal stage, the common gate pad is contacted by the blue-marked probehead. The source and drain of the top-left OFET are contacted by the lateral probeheads. The main I-V converter PCB is enclosed in the black box in the middle.

V_{in} is fed into the source of the OFET under test. The gate of the OFET is connected to the electrical ground and the drain is connected to the inverting input of a high-input-impedance op-amp (*Analog Devices AD549JH*); this input of the op-amp constitutes a virtual ground since the non-inverting input of the same op-amp is connected to the real ground. The output of this op-amp is fed back into the inverting input via a feedback resistance (R_f). The adjustment of R_f can be made using either an external resistance box connected to the circuit through the two coaxial sockets available on the PCB or chosen from five on-board high-precision fixed-value

resistors, covering a range of five orders-of-magnitude, from 100 KΩ to 1 GΩ; a block of DIP (Dual In-line Package) switches serves for this purpose.

The configuration of the second op-amp and R_f constitute a current-to-voltage (I-V) converter, which is the main building block of this system; the op-amp converts the drain current of the OFET into an inverted voltage (V_{conv}) using R_f, as discussed below and described by eq. (4.1). The specifications of the op-amp are appropriate for performing measurements on devices with very low mobility, as its extremely low input bias current (in the fA range) does not compromise the measurements of the, typically, low drain currents (in the nA to µA range).

Also, an appropriate selection of R_f is important so that the converted voltage can be sampled by the oscilloscope with good precision, as discussed below.

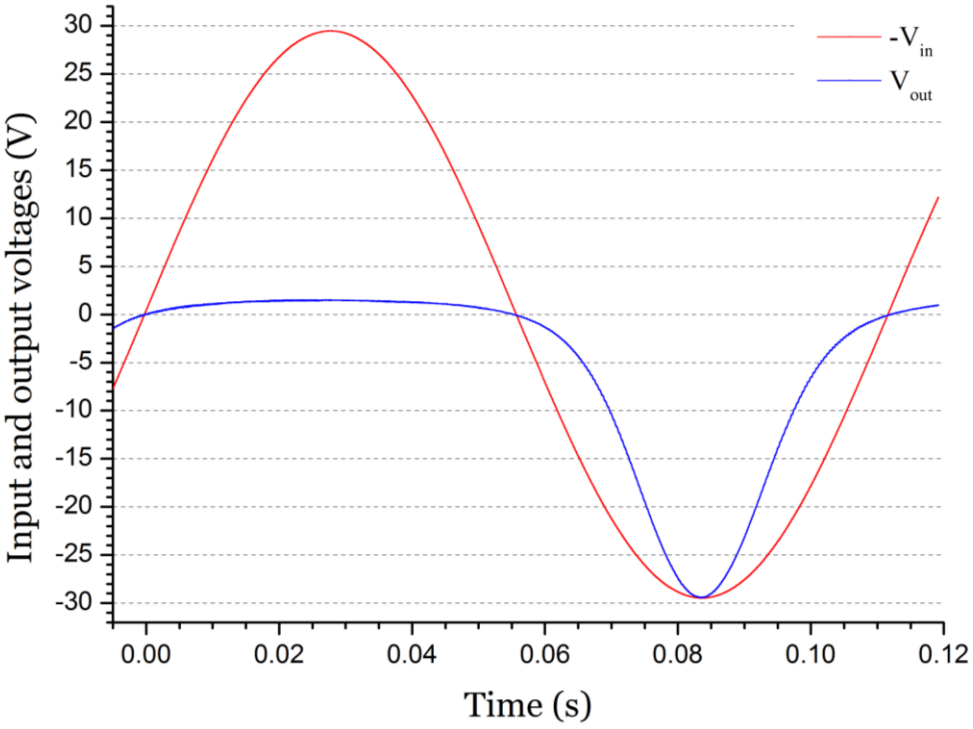

Figure 4-3 – Oscilloscope screenshot for a SiO_2-gated PBTTT p-type OFET. Rf is appropriately adjusted so that the peaks of V_{out} and $-V_{in}$ roughly coincide. The curvature of the output curve over the positive range of $-V_{in}$ (off-state) is an indication of doping.

This OFET driving configuration is equivalent to connecting source to ground and applying $-V_{in}$ to both drain and gate. Considering normally-off (enhancement-mode) OFETs, a hole (or electron) transporting device will turn on for a sufficiently large positive (or negative) V_{in}, and deliver a saturated drain current, $I_{D,sat}(V_G = V_D = -V_{in})$. V_{in} is sufficiently large when its modulus exceeds the modulus of threshold voltage (V_{th}). The resulting saturated drain current is fed into the virtual ground of the described current-to-voltage (I-V) converter, and gets converted into an output voltage (V_{conv}) according to:

$$V_{conv} = -R_f \times I_{D,sat} \quad (4.1)$$

It should be pointed out that V_{sig} and, consequently, V_{in} are zero-offset low-frequency (usually between 6 to 70 Hz) sinusoidal signals. Several studies have demonstrated the effects of gate-bias stress on the threshold voltage of OFETs [104]; for this reason, the application of a

symmetrical bias ensures that the gate dielectric is stressed equally by positive and negative voltages and presumably, the threshold voltage is not affected. Moreover, the single harmonic content of the sinusoidal signal facilitates the use of low-pass filters in both hardware and software for noise mitigation. From a device characterisation perspective, even a single cycle of the sinusoidal drive allows for the extraction of a full set of saturated transfer characteristics with a large number of data points, including both rising and falling voltage sweeps.

The third op-amp (*Linear Technology LT1677*) is a low-noise attenuator and inverter of the input signal (V_{in}), which provides a reference voltage:

$$V_{ref} = -0.1V_{in} \tag{4.2}$$

V_{ref} can be safely sampled by the oscilloscope and is also used to trigger the measurement; the employed oscilloscope has maximum input voltage of 20 V which is lower than the drive requirements of some SiO_2-based OFETs studied here. Also, the inversion of input voltage accounts for the converted drain current, which is also inverted (V_{conv}), as discussed above. This convention serves for a more straightforward representation of the input and output voltages on the oscilloscope screen, as the maxima and minima of both curves appear at the same time (same coordinate of the x-axis).

The output voltage (V_{conv}), which is proportional to $I_{D,sat,}$ and the attenuated and inverted input voltage (V_{ref}) are connected to each of the oscilloscope channels. Together, $V_{conv}(t)$ and $V_{ref}(t)$ represent the OTFTs saturated transfer characteristics, parametric in time. An example from the characterisation of a slightly-doped p-type OFET is given in Figure 4-3. An important remark is that a factor x10 is applied to both voltages by the software; this is to account for the x0.1 attenuation of the drive signal, as described by eq. (4.2). To avoid any confusion, hereafter, the output voltage is defined as:

$$V_{out} = 10V_{conv} = -10\mathrm{R_f} \times \mathrm{I_{D,sat}} \tag{4.3}$$

An important remark is that since the gate electrode is connected to the ground, this system provides no information on gate leakage; any current flow from the source to the gate cannot be observed. However, since drain is connected to a virtual ground and gate is connected to the actual ground, there can be no current flow from the drain to the gate, or vice versa.

4.1.2. Drive considerations and adjustments for water-gated OTFTs

The maximum frequency of the sinusoidal drive is limited by the properties of the device under test. The combination of a typically high channel resistance (in the MΩ to GΩ range) with the presence of parasitic capacitances, due to the structure of the OFETs, makes the device under test resembling an RC network, effectively acting as a low-pass filter. At high operating frequencies, a phase-shift is evident on the oscilloscope screen, with V_{out} lagging behind $–V_{in}$. This condition can compromise the measurement results and lead to significant differences between the values calculated by this method and those measured by conventional DC methods; thus, appropriate selection of drive frequency is necessary. In all measurements discussed in this work, the drive conditions were always adjusted so that no phase-shift occurs. Although AlO_x-gated pentacene devices were successfully tested at frequencies as high as 100 Hz, in most cases the frequency of the drive signal ranged from 6 to 16 Hz.

Moreover, considering that, in the case of AlO_x-gated OFETs, the anodisation voltage for the formation of the AlO_x dielectric layer was 5 V, the amplitude of the drive voltage was accordingly set at 3 V in order to prevent the breakdown of the dielectric, as it has been demonstrated by Majewski *et al.* [51].

As discussed in section 2.4.6, electrolyte- and water-gated devices cannot operate at high frequencies due to the slow motion of ions that form their electric double layers (EDLs) [54]. Moreover, the electrochemical window of water is ~1.23 V [75], which also limits the maximum drive voltage that can be applied to a water-gated OTFT under test.

Several tests were conducted on water-gated devices for the optimisation of their characterisation using the I-V converter method. Considering that the drive signal was used as the trigger source for the oscilloscope, this very low frequency operation fails to trigger and synchronise the sampling process of many oscilloscopes; hence, an appropriate selection of the oscilloscope specifications was necessary for successfully using this characterisation method in order to perform real-time multiparametric measurements on this kind of devices. The typical amplitude of the drive voltage for these devices was 0.5 to 1.0 V, whereas the typical frequency range was from 0.25 to 3 Hz.

Electrical measurements on novel water-gated OTFTs based on organic nanowires were successfully conducted using this system. The results of this study were recently published in the *Organic Electronics* journal [62].

4.2. Parameter calculation

As described above, the $V_{in}(t)$ and $V_{out}(t)$ are simultaneously sampled by the two channels of an oscilloscope; the oscilloscope data from both channels plotted together constitute an alternative representation of the saturated transfer characteristics of an OFET under test, providing the same physical information as the saturated transfer characteristics measured by conventional equipment, as described in section 3.3.

This section describes the conventions and the methodology for the calculation of all the important OFET parameters using the oscilloscope data recorded by the I-V converter system.

4.2.1. Saturated drain current calculation

Based on the convention given in eq. (4.3), the maximum saturated drain current (I_{on}) can be directly calculated from the oscilloscope data according to:

$$\mathrm{I_{on}} = \frac{V_m}{10 \times R_f} \tag{4.4}$$

where V_m is the peak output voltage.

4.2.2. On/off ratio calculation

The on/off ratio of an OFET is easily calculated as the ratio of the positive maximum over the negative maximum for an n-type semiconductor device or inversely for a p-type one:

n-type: $$\frac{I_{on}}{I_{off}} = \left|\frac{\max(V_{out})}{\min(V_{out})}\right| \tag{4.5}$$

p-type: $$\frac{I_{on}}{I_{off}} = \left|\frac{\min(V_{out})}{\max(V_{out})}\right| \quad (4.6)$$

Using these equations, it should be mentioned that I_{on} and I_{off} are defined as the drain current values for $V_{GS}=V_{DS}=\pm V_0$ (where V_0 is the amplitude of the sinusoidal drive), with opposite signs respectively. Thus, deviations from the conventional I_{on}/I_{off} ratios are expected, considering that in most cases found the literature, I_{on}/I_{off} is calculated as the ratio of the I_D at maximum V_{GS} over the I_D at $V_{GS}=0$ for the same V_{DS}, recalling eq. (3.3):

$$\frac{I_{on}}{I_{off}} = \frac{I_{D\left(V_{DS(max)},\ V_{GS(max)}\right)}}{I_{D\left(V_{DS(max)}, V_{GS=0}\right)}} \quad (4.7)$$

4.2.3. Off-current correction / doping compensation

In the presence of dopants, the equivalent circuit of an OFET can be described by a resistor connected in parallel with an ideal OFET. In this case, the total current that flows through the channel of an OFET is defined as the sum of the drain current of the ideal OFET and an ohmic current due to the presence of dopants:

$$I_{D,total} = I_{D,OFET} + I_{ohmic} \quad (4.8)$$

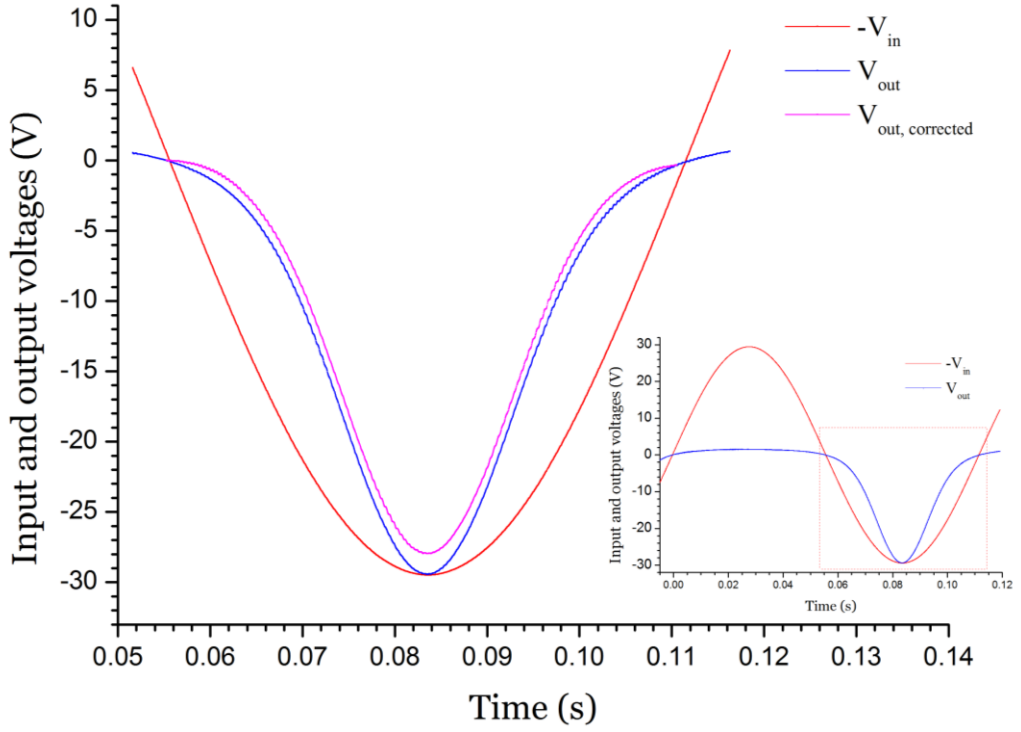

Figure 4-4 – The on-region of the same OFET before (blue curve) and after (purple curve) the off-current correction. The dashed red rectangle in the inset indicates the region of the original where the data of the main graph are taken from.

Generally speaking, the modulus of I_{ohmic} is the same at a given drain voltage, regardless of its polarity. This characteristic allows for the correction of doping effects using the symmetry of the sinusoidal drive; the pure transistor current can be extracted from the saturated transfer characteristics by the application of a point-to-point addition, i.e. subtraction (considering the polarity), of the off-region to the on-region of the OFET. This method can be described as:

$$V_{out,corrected}(\mathrm{t}) = V_{out}(t) + V_{out}\left(t \pm {}^{\mathrm{T}}/_{2}\right) \quad (4.9)$$

Figure 4-4 shows an example of off-current-correction; the off-cycle of the oscilloscope data shown in Figure 4-3 and in the inset of Figure 4-4 were added to the blue curve (V_{out}) resulting in the purple curve ($V_{out,\ corrected}$).

In the following sections, OFET parameters are calculated from both raw (before correction) and off-current-corrected data. This allows for comparisons and a quantification of the effects of doping on parameter calculation.

4.2.4. Threshold voltage and mobility calculation methods

As previously mentioned in section 3.3.2.2, the use of different threshold voltage and mobility extraction methods can result in significant differences in the calculated values [99, 100]. In this section, three different parameter extraction methods, tailored for this characterisation system, are discussed and compared.

4.2.4.1. *Transfer curve conversion and extrapolation method*

Considering that using the I-V converter system, the input and output voltages are plotted parametric in time, the same oscilloscope data can be converted and plotted as standard transfer curves by eliminating the time parameter, i.e. plotting the oscilloscope data in X-Y mode (with input voltage being on the x-axis) and converting the output voltage into drain current according to eq. (4.3).

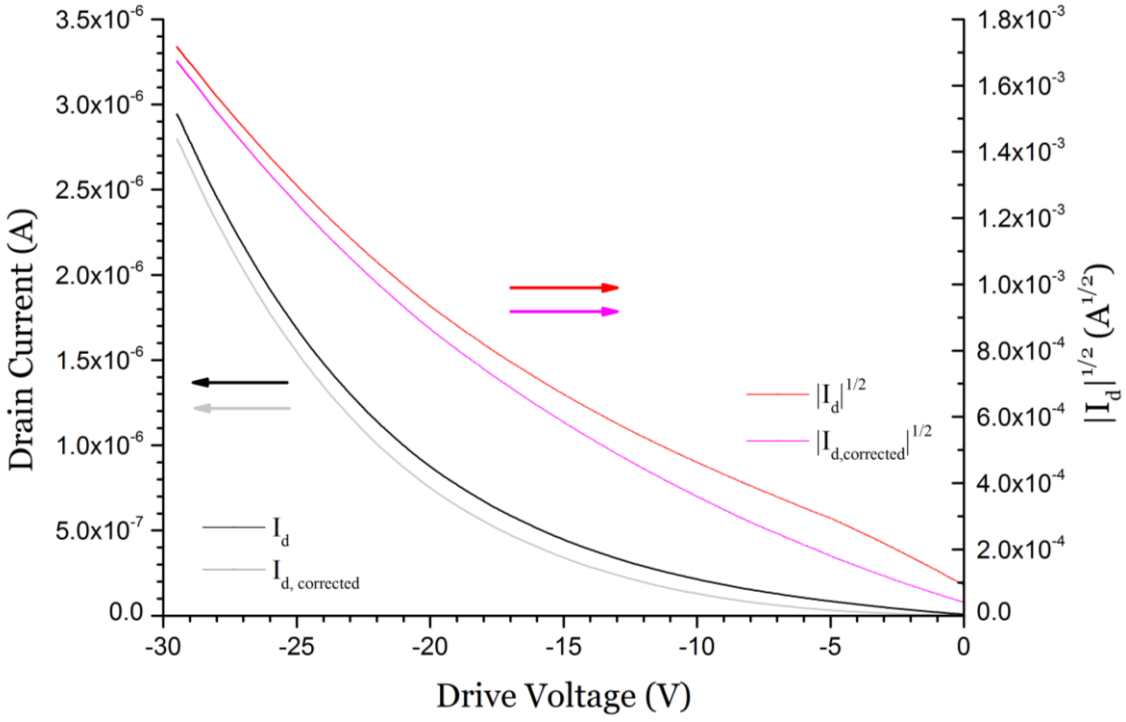

Figure 4-5 – Converted saturated transfer characteristics from the oscilloscope data. Left y-axis: modulus of drain current versus drive voltage with and without off-current correction. Right y-axis: square root of the modulus of drain current versus drive voltage with and without off-current correction.

A significant difference between these converted data and the standard transfer characteristics lies is the fact that, in this case, V_{DS} is not kept constant while the V_{GS} range is swept, but it changes along with V_{GS} so that V_{DS}=V_{GS} at all times. Strictly speaking, since, for a

normally-off OFET, the fundamental condition for saturation, i.e. $|V_{DS}| > |V_{GS} - V_{th}|$, is always satisfied, there should be no dependence of the drain current on the varying drain voltage. However, in reality, this difference can have a minor impact on the measurement results when compared to standard transfer characteristics measured by a semiconductor analyser and can serve for comparisons between the two methods.

Figure 4-5 shows the converted transfer characteristics of the same OFET discussed above. The first suggested parameter extraction method is the same as the ESR (extrapolation in the saturated region) method discussed in section 3.3.2.2. A simple linear regression fit is applied to the square-rooted I_D values and this straight line is extrapolated to the x-axis; the intercept of the straight line with the x-axis reveals the threshold voltage of the device under test (DUT).

The slope of the linear fit can be exploited for the calculation of mobility. Recalling eq. (3.3):

$$\mu = \frac{2L}{C_i W} Slope^2 \tag{4.10}$$

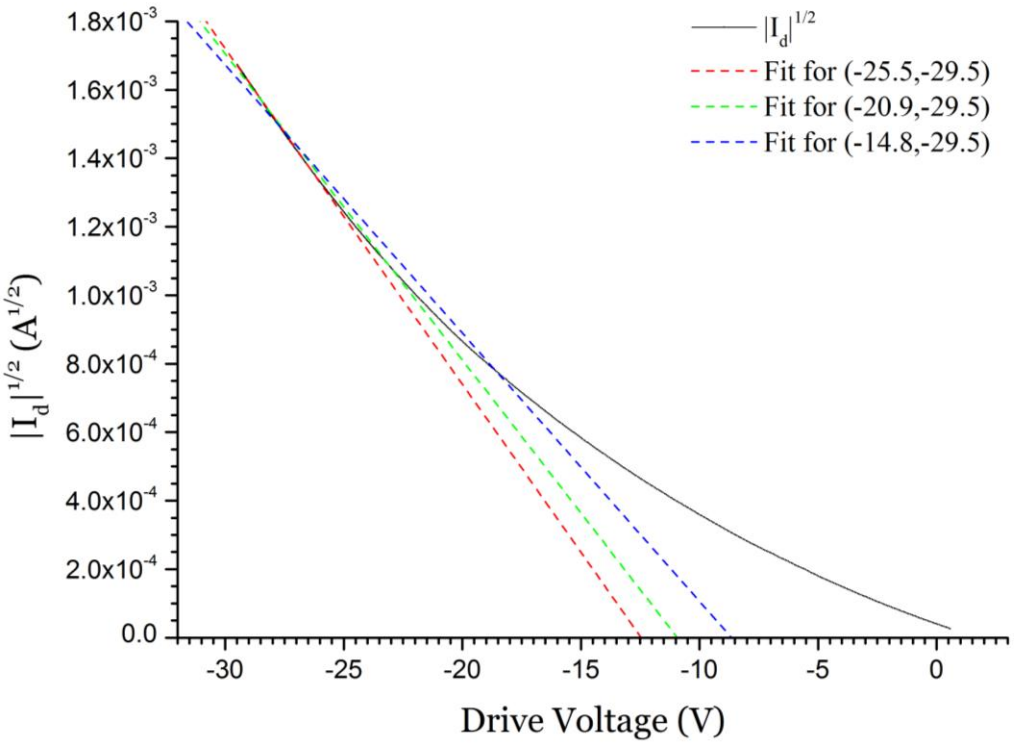

Figure 4-6 – Square root of the modulus of the off-current-corrected drain current versus drive voltage (black curve). Three different simple linear regression fits (dashed red, green and blue straight lines) for three different data ranges.

In practice, a critical detail is the selection of the data range which is considered for the linear regression fit. The range is usually chosen manually and arbitrarily; the fit details are rarely mentioned explicitly in published papers. In fact, this selection can induce wide deviations in the calculated values of V_{th}; an example is given in Figure 4-6 and the respective calculation results are shown in Table 4-I. In this example, three different data regions were used for the application of the linear fit. Additionally, another factor which can yield significantly different results is the off-current-correction, as discussed in the previous section; a comparison between the values extracted from raw and corrected data can also be seen in Table 4-I.

As a general rule, derived from the analysis and comparison of a large amount of measurement data (not shown here), the selected data range affects both parameters; if the selected range results in a fit with comparatively steep slope, this is interpreted as a relatively high mobility at the expense of a higher modulus (a shift towards normally-off behaviour) of threshold voltage. Conversely, when the selected range results in a fit with smaller slope, this induces the opposite results. In the case of off-current-correction, the corrected results always show a larger modulus of V_{th}, but mobility is usually slightly affected.

Table 4-I – Comparison of Vth and μ values for raw and off-current corrected data and different fit data ranges

Fit data region		Raw data		Off-current corrected data	
from	to	V_{th} (V)	μ ($cm^2V^{-1}s^{-1}$)	V_{th} (V)	μ ($cm^2V^{-1}s^{-1}$)
-25.5	-29.5	**-11.5**	**0.01015**	**-12.5**	**0.01069**
-20.9	-29.5	**-9.9**	**0.00836**	**-10.9**	**0.00888**
-14.8	-29.5	**-7.3**	**0.00634**	**-8.7**	**0.00682**

4.2.4.2. *Sinusoidal integration method*

A new numerical method for V_{th} and μ calculation is discussed here. The method exploits the large number of data points exported by the oscilloscope; typical input and output curves, measured by a Picoscope oscilloscope, consist of more than 4500 data points each, which allows for the plotting of smooth curves with good resolution. The curve of V_{out} is integrated over time assuming an ideal sinusoidal drive.

As explained above, according to the circuitry of this system, the following notions apply:

$$|V_D| = |V_G| = |V_0 \sin(2\pi f t)| \tag{4.11}$$

where V_0 is the amplitude of the sinusoidal drive. For an enhancement-mode (normally-off) OFET and for a sufficiently high V_{th}, the saturated region condition is met:

$$|V_D| = |V_G| > |V_G - V_{th}| \tag{4.12}$$

thus the OFET operates in the saturated region. Recalling the drain current equation in saturation:

$$I_d = \mu C_i \frac{W}{2L}(V_G - V_{th})^2 \tag{4.13}$$

and assuming that μ is constant and independent of the drive voltage, a constant k can be defined as:

$$k = \mu C_i \frac{W}{2L} \tag{4.14}$$

Substituting, we get:

$$I_d = k(V_G - V_{th})^2 \tag{4.15}$$

To ensure that the measurement data are taken within the saturated region, the limits of the integral must be defined by making a pragmatic assumption. For the calculations given in the section, it is assumed that:

$$|V_{th}| < 0.5V_0 \tag{4.16}$$

Thus, given the case of an n-type OFET, we can safely integrate in the range $\left(\frac{\pi}{6}, \frac{5\pi}{6}\right)$ since:

$$V_0 sin\left(\frac{\pi}{6}\right) = V_0 sin\left(\frac{5\pi}{6}\right) = 0.5V_0 \tag{4.17}$$

The respective integral limits in the time scale are: $\left(\frac{T}{12}, \frac{5T}{12}\right)$, where T is the period of the sinusoidal drive. Integrating over the negative semi-period $(\pi, 2\pi)$ has no physical meaning. Integrating eq. (4.15) over this time range yields:

$$\int_{t=T/12}^{t=5T/12} I_d(t)dt = \int_{t=T/12}^{t=5T/12} k(V_G - V_{th})^2\, dt \tag{4.18}$$

From the exported measurement data, we also get:

$$\int_{t=T/12}^{t=5T/12} I_d(t)dt = \frac{1}{10R_f}\int_{t=T/12}^{t=5T/12} V_{out}(t)dt = \frac{A}{10R_f} \tag{4.19}$$

where R_f the feedback resistance and A is the area between the output voltage curve and the x axis (in units Vs); an example on a p-type is given in Figure 4-7; in this example, the integral limits are $\left(\frac{7T}{12}, \frac{11T}{12}\right)$ and the grey-shaded region illustrates the area A.

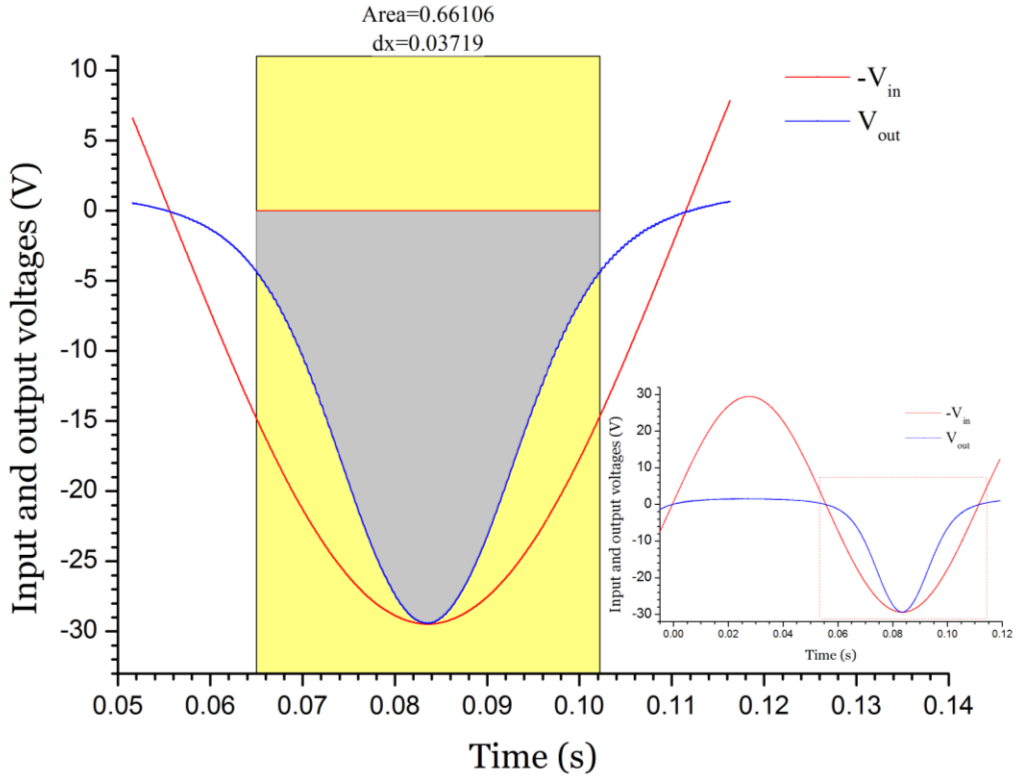

Figure 4-7 – An example of integration of the output voltage curve of a p-type OFET over the (7T/12, 11T/12) range.

Substituting eq. (4.19) into eq. (4.20), we get:

$$\frac{A}{10R_f} = \int_{t=T/12}^{t=5T/12} k(V_G - V_{th})^2 \, dt \tag{4.20}$$

From this equation, it can be derived that:

$$\mathrm{V_{th}} = \frac{V_0}{2}\left(\frac{\left(\frac{3\sqrt{3}}{\pi} - \frac{6A}{TV_m}\right) \pm \sqrt{\left(\left(18 - \frac{63\sqrt{3}}{2\pi}\right)\frac{A}{TV_m} + \frac{27}{\pi^2} - 2 - \frac{3\sqrt{3}}{2\pi}\right)}}{1 - 3\frac{\mathrm{A}}{TV_m}}\right) \tag{4.21}$$

where V_0 is the amplitude of the sinusoidal drive, V_m is the peak of the output voltage, A the area between the output curve and x axis for the range $\left(\frac{\pi}{6}, \frac{5\pi}{6}\right)$ and T the period of the drive. The full derivation is given in Appendix I.1.

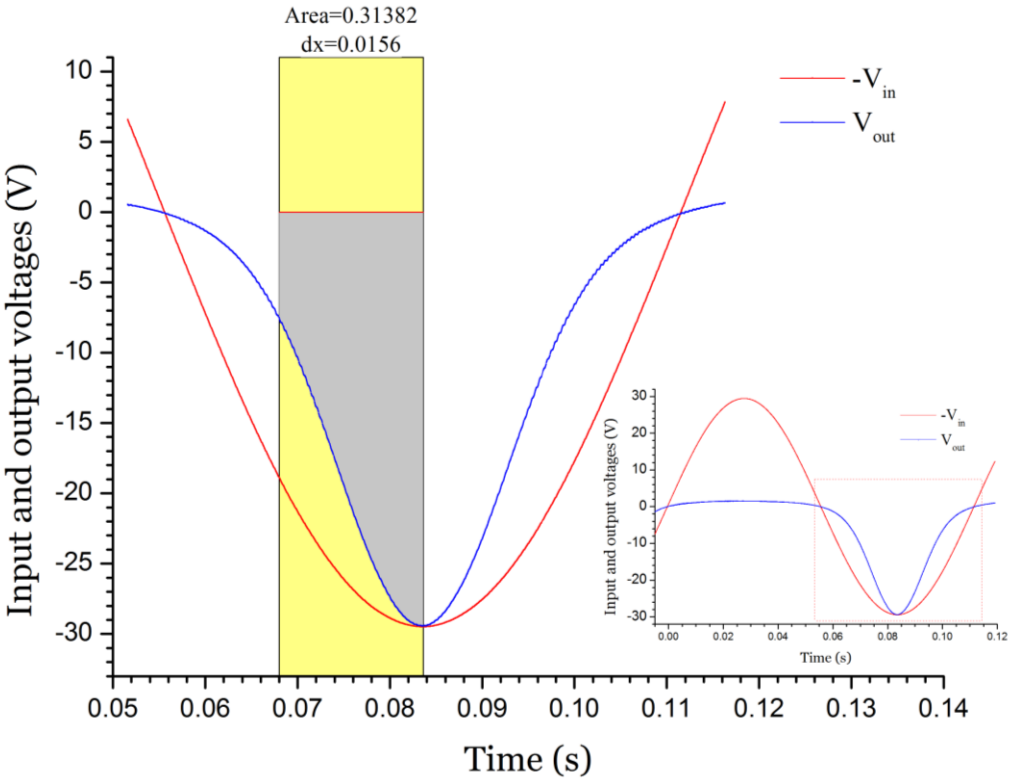

Figure 4-8 – Application of the sinusoidal integration method to the raw measurement data. The grey-shaded region represents the calculated area.

When hysteresis is evident, the rising (turning-on) and falling (turning-off) flanks of V_{out} are not symmetrical; this phenomenon is discussed in section 4.2.5. Hysteresis can introduce calculation errors, thus it can be deliberately omitted by using different integration limits; in this case, only the rising flank of V_{out} can be integrated.

Recalculating the equations given above for the integration limits $\left(\frac{\pi}{4}, \frac{\pi}{2}\right)$ gives the following expression of threshold voltage (derivation given in Appendix I.2):

$$V_{th} = V_0 \left(\frac{2\left(\frac{\sqrt{2}}{\pi} - \frac{4A}{TV_m}\right) \pm \sqrt{\left(12 + \frac{8 - 32\sqrt{2}}{\pi}\right)\frac{A}{TV_m} + \frac{8}{\pi^2} - \frac{1}{\pi} - \frac{1}{2}}}{1 - 8\frac{A}{TV_m}} \right) \quad (4.22)$$

Eq. (4.22) is used for V_{th} calculation in the examples given in Figure 4-8 and Figure 4-9, which show the areas of the raw and off-current-corrected data, respectively.

When V_{th} is extracted, mobility can be calculated using the following equation:

$$\mu = \frac{1}{10R_f C_i} \times \frac{2L}{W} \times \frac{|V_m|}{(|V_0| - |V_{th}|)^2} \quad (4.23)$$

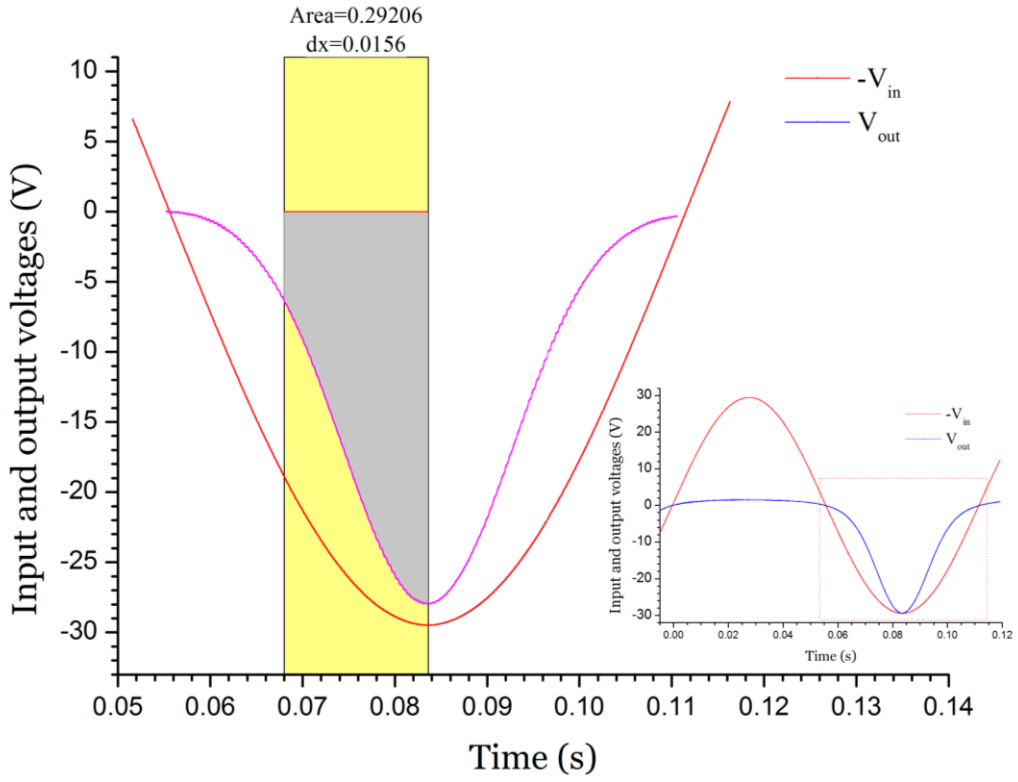

Figure 4-9 – Application of the sinusoidal integration method to the off-current-corrected data. The grey-shaded region represents the calculated area.

The calculation results for both the raw and off-current-corrected data are shown in Table 4-II. Again, off-current-correction was found to significantly alter the results, giving a substantially higher V_{th} modulus in conjunction with a higher μ value.

Table 4-II – The calculated Vth and μ values from sinusoidal integration method for the raw and off-current-corrected data.

Input voltage data region		Raw data		Off-current corrected data	
from	to	V_{th} (V)	μ ($cm^2V^{-1}s^{-1}$)	V_{th} (V)	μ ($cm^2V^{-1}s^{-1}$)
-20.9	**-29.5**	**-7.6**	**0.00677**	**-9.1**	**0.00748**

4.2.4.3. *Non-linear fit / output simulation*

Modern programming languages, as well as data analysis software packages allow for user-defined non-linear fit functions. It is possible to accurately calculate threshold voltage and mobility using such functions.

Given that in the saturated region, the following equations apply:

$$V_{out} = 10R_f I_D = 10R_f \mu C_i \frac{W}{2L}(V_G - V_{th})^2 \tag{4.24}$$

and given that:

$$|\mathrm{V_G}| = |V_0 \sin(2\pi f t)| \tag{4.25}$$

Substituting eq. (4.25) into eq. (4.24) gives:

$$V_{out} = 10R_f \mu C_i \frac{W}{2L}(V_0 \sin(2\pi f t) - V_{th})^2 \tag{4.26}$$

This equation is slightly modified to account for the time offset (Dt) present in the exported data from the oscilloscope. The non-linear fit equation writes:

$$V_{out,fit} = 10R_f \mu C_i \frac{W}{2L}\left(V_0 \sin\left(2\pi f(t + Dt)\right) - V_{th}\right)^2 \tag{4.27}$$

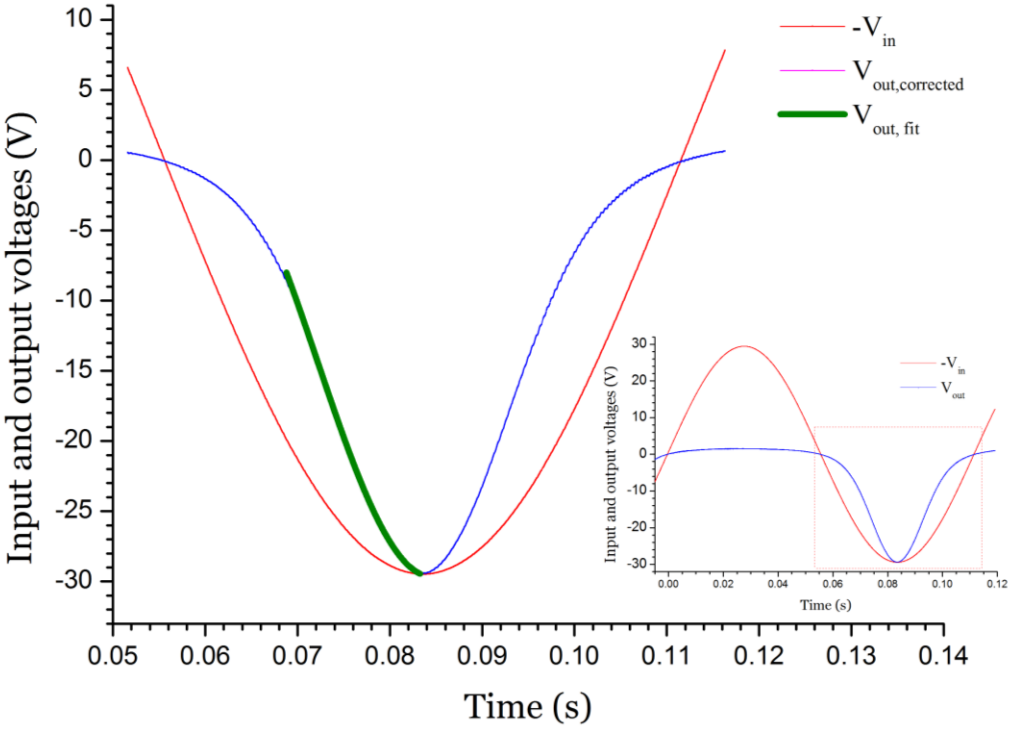

Figure 4-10 – The green curve is the non-linear fit of the output voltage for the selected data range (π/4,π/2)

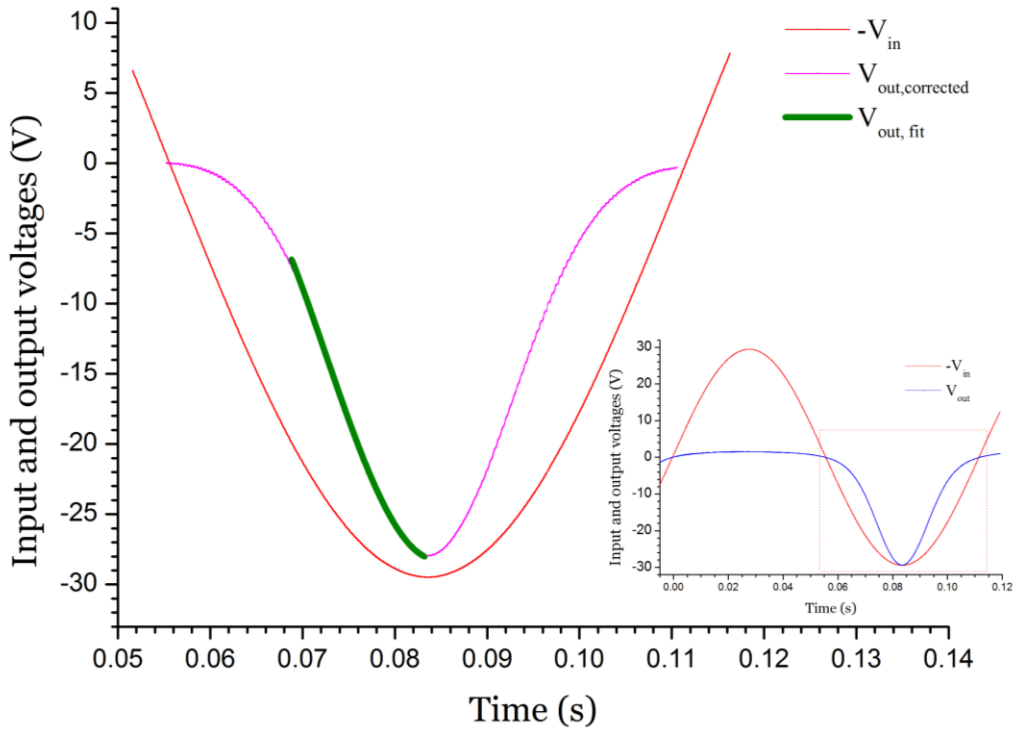

Figure 4-11 – The green curve is the non-linear fit of the off-current corrected output voltage for the selected data range (π/4,π/2)

The selected data region for the non-linear fit was the same as that used in the previous examples, which allows for comparisons. The non-linear fit curves for the raw and the off-current-corrected data are shown in Figure 4-10 and Figure 4-11, respectively; Table 4-III gives a comparison of the calculated V_{th} and μ values in both cases.

Table 4-III – The calculated Vth and μ values from non-linear fit for the raw and off-current-corrected data.

Fit data region		Raw data		Off-current corrected data	
from	to	V_{th} (V)	μ ($cm^2V^{-1}s^{-1}$)	V_{th} (V)	μ ($cm^2V^{-1}s^{-1}$)
-20.9	-29.5	-7.2	0.00658	-8.4	0.00703

4.2.4.4. *Comparison of threshold voltage and mobility calculation methods*

The three different methods described above exemplify the impact of the parameter extraction method, the selection of the data range and the correction for off-current in the calculation of OFET parameters. A comparison of the three methods applied to the same data range is given in Table 4-IV.

Table 4-IV – Comparison of the calculated Vth and μ values using the three different parameter extraction methods for the same data range

Method used	Raw data		Off-current corrected data	
Input voltage data range: (-20.9,-29.5)	V_{th} (V)	μ ($cm^2V^{-1}s^{-1}$)	V_{th} (V)	μ ($cm^2V^{-1}s^{-1}$)
Extrapolation in the saturated region (ESR)	**-9.9**	**0.00836**	**-10.9**	**0.00888**
Sinusoidal Integration (SIM)	**-7.6**	**0.00677**	**-9.1**	**0.00748**
Non-linear fit (NLF)	**-7.2**	**0.00658**	**-8.4**	**0.00703**

In the case of OFETs used as multiparametric sensing transducers, as discussed in Chapter 7, the calculation of V_{th} and μ is of great importance as minor differences can be misinterpreted as sensing responses. It is worth mentioning that, in this case, the most important merit of a characterisation method lies not in the magnitude of the calculated values in absolute terms, but the method's capability of providing consistent results under the same conditions while remaining capable of detecting small changes in the investigated parameters, even in the presence of noise.

Due to the use of two different characterisation methods in this work and in accordance with the majority of published papers on OFET characterisation, the ESR method has been used for both the conventional current-voltage measurements and the measurements taken with the I-V converter system, unless explicitly stated. Moreover, ESR is the method of choice in the case of the automated multiparametric characterisation, described in section 4.3. Multiple tests of the automated system in different laboratories, even in the presence of evident electromagnetic interference (EMI), gave consistent results with insignificant noise effects.

4.2.5. Hysteresis quantification

Hysteresis is an important characteristic in the characterisation of OFETs; although, it is usually an undesired attribute, it can be harnessed for specialised applications, such as memory devices [105].

In conventional output or transfer characteristics, hysteresis manifests itself as a mismatch between the rising and falling current curves under their respective rising and falling voltage sweeps, with the former either preceding or falling behind the latter. Hysteresis is usually only qualitatively discussed but not quantified. There are few methods for hysteresis quantification suggested in the literature; these methods have arbitrary definitions and are based on either C-V measurements [106] or the transfer characteristics of an OFET [107].

A new method for the precise quantification of hysteresis in OFETs is presented here. Two integrals are employed for the evaluation of the symmetry of the output curve and, consequently, the quantification of hysteresis. This can be described by the following expression:

$$Hy = \frac{A_{fall} - A_{rise}}{A_{rise}} \times 100\% \tag{4.28}$$

where A_{rise} and A_{fall} are two symmetrical integrals of $V_{out}(t)$ versus time, with respect to $\frac{T}{4}$ (for an n-type OFET) or $\frac{3T}{4}$ (for a p-type OFET).

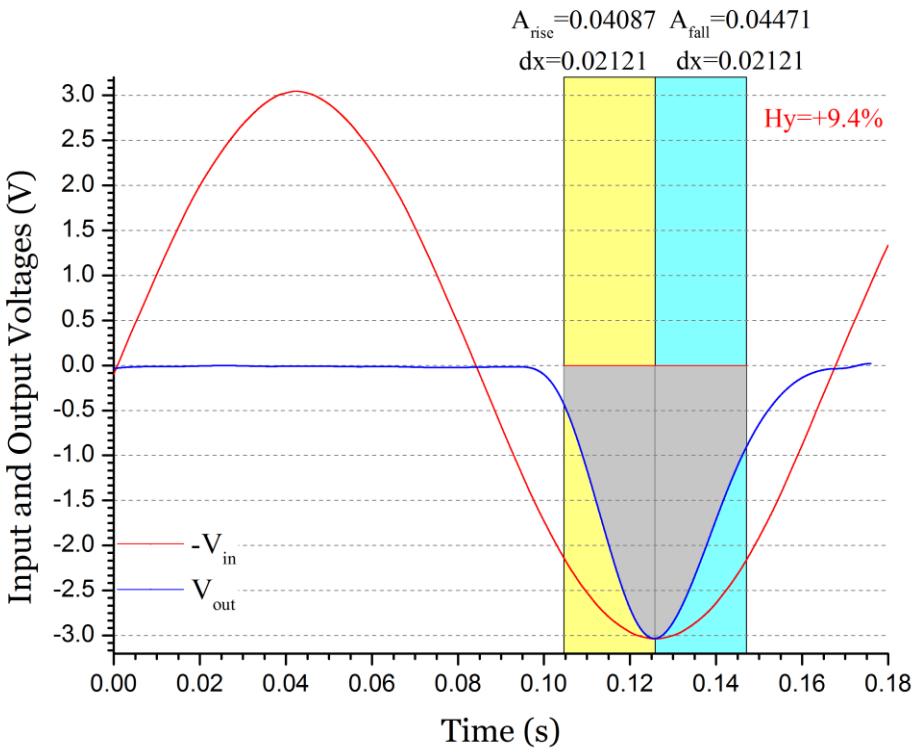

Figure 4-12 – A comparison of two V_{out} integrals for hysteresis quantification. A_{rise} is the grey-shaded region inside the yellow rectangle and A_{fall} the grey-shaded region within the cyan rectangle.

Figure 4-12 gives an example of a p-type OFET with evident hysteresis, manifested by the delayed fall of the V_{out} curve.

In this example, the selected areas for comparison are:

$$A_{rise} = \int_{t=5T/8}^{t=3T/4} V_{out}(t)dt \quad (4.29)$$

and

$$A_{fall} = \int_{t=3T/4}^{t=7T/8} V_{out}(t)dt \quad (4.30)$$

Applying eq. (4.28), the calculated hysteresis is +9.4%. The positive sign indicates that, at a given bias, drain current is higher in the falling flank of the sweep than in the rising, as previously shown in the example of Figure 3-7.

In conclusion, this example suggests that hysteresis quantification can constitute an added value to the electrical characterisation of OFETs. In the particular case of OFETs used as sensing transducers, this method of quantification allows hysteresis to be used as an additional sensing parameter; for instance, hysteresis studies can enhance the detection of analytes (vapour under investigation) which induce charge trapping in an OFET [108].

4.3. Automated electrical characterisation

The capabilities of the I-V converter system have been fully exploited by the development of supporting software that enables a fully-automated characterisation process. A *National Instruments LabVIEW* application was developed for this purpose. The graphical user interface (GUI) of one of the early versions of this application is shown in Figure 4-13.

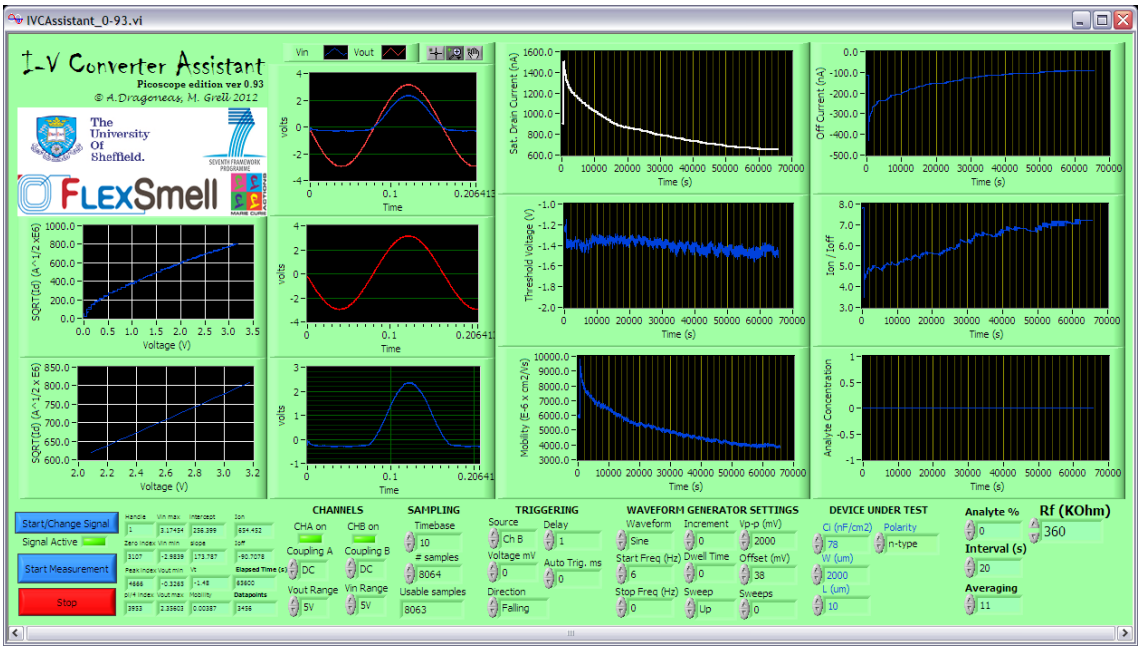

Figure 4-13 – The graphical user interface of the I-V Converter Assistant application

The program communicates with a *Picoscope* oscilloscope via a *Microsoft Windows dynamic-link library* (*DLL*) provided by the manufacturer; the control signals and sampling data are physically transferred between the program and the hardware over a USB connection.

A series of parameters must be defined by the user before the characterisation process is initiated; these include information on the OFET under test (the C_i *of the gate dielectric*, the *channel dimensions* and the *type of semiconductor* used; i.e. n-type or p-type) and the value of the feedback resistance (R_f) used. Changing these parameters during the characterisation is possible, but any changes are applied only to the next measurements.

The oscilloscope initialisation data must also be defined; these include the signal generation settings (*waveform type, frequency, amplitude, DC offset*), as well as the sampling and trigger settings (*time base, input voltage ranges, trigger source, direction and level*, etc.). There are stored default values for all fields, which facilitate this initialisation process.

The OFET parameters are calculated and plotted in a time-resolved manner; the interval between the data points can be defined by the user. Median filters can be applied to all calculated parameters for further noise mitigation. The window size of these filters, i.e. the number of consecutive measurements for each data point, can be also selected by the user using the *Averaging* field. The throughput of this characterisation system depends on the frequency (f) of V_{in}. If no averaging is applied, then one set of OFET parameters can be calculated every 1/f. As previously mentioned, the maximum frequency is mainly limited by the mobility of the semiconductor and the parasitic capacitance of the device under test, as the transistor can be modelled as a RC network which effectively operates as a low-pass filter.

Although tests on pentacene OFETs have shown a good operation for frequencies up to 100Hz, lower frequencies (<10 Hz) are typically chosen for the tests. As discussed in section 4.1.2, water-gated OFETs are typically characterised with frequencies even below 1 Hz.

Each set of data consists of 5 parameters; the maximum (modulus of) saturated drain current (I_{on}), the maximum (modulus of) off-state current (I_{off}), the on/off ratio (I_{on}/I_{off}), the threshold voltage (V_{th}) and the charge carrier mobility (mu). For the calculation of V_{th} and mobility, the transfer curve conversion and the extrapolation in the saturated region method (ESR), described in section 4.2.4.1, is used.

Using this method, the simple linear regression fit is applied to the transfer curve in always the same range of input voltages for consistency. For instance, for p-type OFETs, such as pentacene, making the assumption that the threshold voltage is smaller than the 70% of the amplitude of V_{in}, this range is the [5π/4 , 3π/2] region of the sinusoidal drive. In the example given in Figure 4-14, the negative peak voltage was set at -3V, thus this range equals [-2.12V , -3.00V]; this region is white-shaded in this figure.

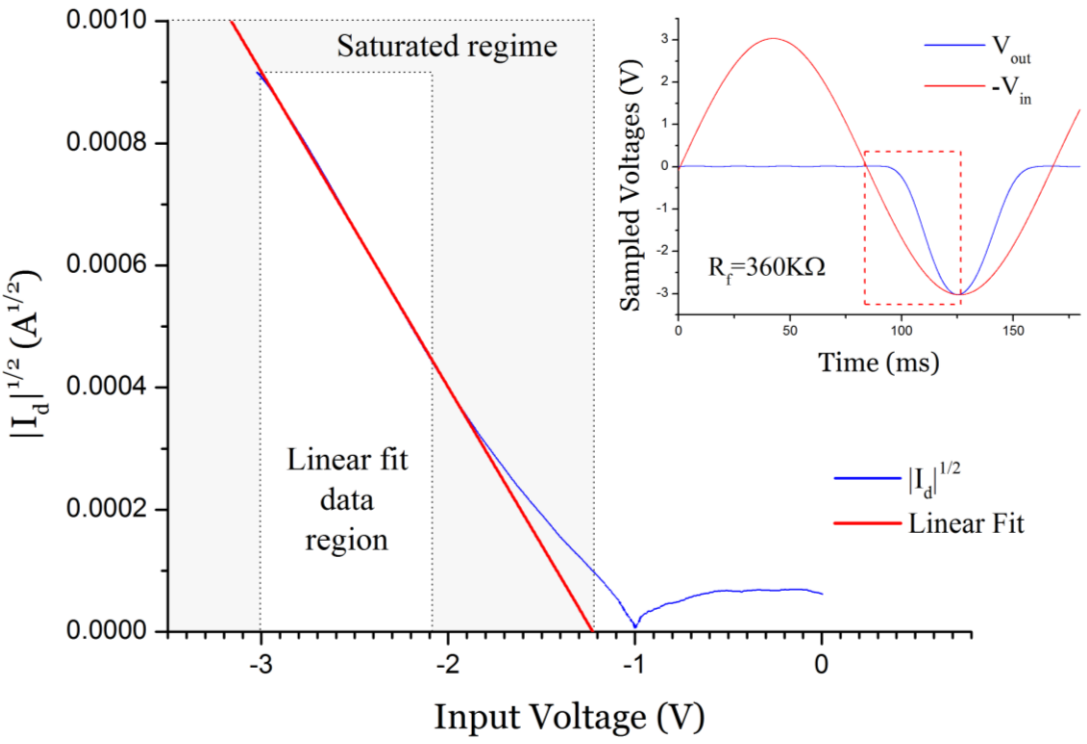

Figure 4-14 – Illustration of the ESR parameter extraction method applied by the automated characterisation software. The inset shows the raw oscilloscope data, the dashed red rectangle indicated the data region which is converted and shown in the main graph. The main graph shows the square root of the modulus of drain current versus $-V_{in}$. The white-shaded region indicates the data region for the application of the simple linear regression fit.

The measurement results can be exported as text files with comma-separated values (.csv) for further analysis. Moreover, oscilloscope screenshots can also be exported as text files while the characterisation process is running.

This system was successfully used for the detection of quick OFET parameter responses in the light-sensitivity tests discussed in section 6.3, as well as in most of the vapour sensing experiments discussed in Chapter 7.

Finally, a different approach to the automated characterisation of organic semiconductor devices has been the miniaturisation of the I-V converter system into a stand-alone handheld characterisation system. An embedded system, based on a RISC microcontroller (*Atmel ATMega644PA*), was designed and a working prototype was built. The source code was written in C language using *AVR Studio 4* and *WinAVR-20100110* C Compiler.

This apparatus incorporates a signal generation unit, signal conditioning circuitry, an embedded analogue-to-digital (ADC) converter and the characterisation logic. Changeable OFET and resistive sensors can be externally connected to a special socket. The characterisation results are displayed on an LCD display and the measurement data can also be sent to a computer over a USB connection in real-time.

This system was tested and used in actual gas sensing measurements with resistive transducers. However, the limited processing power of the employed 8-bit microcontroller (MCU) does not allow for fast multiparametric characterisation on OFETs. For this reason, further development of the I-V converter system focused on the improvement of the LabVIEW platform described above.

It is worth mentioning that the novel sinusoidal integration method for the calculation of threshold voltage and mobility, described in section 4.2.4.2, can be less demanding in processing power than other calculation methods, which employ linear fits. In particular, an MCU with an embedded multiplier-accumulator (MAC) unit can greatly reduce the parameter calculation time using this method.

The circuit schematic of the handheld system and a photograph of one working prototype are shown in Appendix II.8.

Chapter 5. Device characterisation results and discussion

As mentioned before, in this work, organic field-effect transistors (OFETs) and their gas sensing capabilities constitute the main focus of this study. Prior to their exploitation as gas sensing transducers, a good understanding of the operation of these devices in ambient conditions is necessary.

This chapter discusses the results from the characterisation of the fabricated OFETs; this includes their output and transfer characteristics, the quantification of their important parameters, a comparative study of the impact of the gate dielectric in the morphology, performance and the environmental stability of these devices.

Section 5.1 discusses the results from impedance measurements on capacitors based on the dielectrics similar to those used as gate insulators of the fabrication of OFETs. Sections 5.2 to 5.5 discuss the results from the characterisation of pentacene, PDI8-CN_2, tetracene and PBTTT OFETs, respectively. The former two provide comparisons between different dielectric combinations. Finally, section 5.6 gives an overall comparison of the types of fabricated devices.

5.1. Impedance measurements on capacitors

The quantification of the *capacitance per unit area of the gate dielectric (C_i)* is of great importance for OFET characterisation, especially due to the fact that the extraction of field-effect mobility (μ_{eff}), discussed in sections 3.3.2.2 and 4.2.4, is based upon a fixed known value of C_i. For the electrical characterisation of the gate stacks used in the OFET configurations discussed in the following sections, *parallel-plate capacitors* were prepared; these devices were fabricated using the same techniques as those used for the fabrication of the respective gate stacks of low-voltage OFETs, having the same dimensions and combinations of materials. These capacitors were also used in the light sensitivity measurements and served for making comparisons between inorganic oxide and polymeric dielectrics; these results are discussed in section 6.2.

For an ideal and uniform parallel-plate capacitor, capacitance is calculated by:

$$C = \varepsilon_r \varepsilon_0 \frac{A}{t} \tag{5.1}$$

and C_i is consequently expressed as:

$$C_i = \frac{\varepsilon_r \varepsilon_0}{t} \tag{5.2}$$

where ε_r is the *relative static permittivity* of the dielectric material between the plates, which is also denoted by *k* and referred to as the *dielectric constant*, ε_0 is *the vacuum permittivity (~8.854 × 10^{-12} F/m)*, A is the area of overlap of the two plates and t is the thickness of the dielectric material which separates the plates.

Considering several factors, such as the non-uniformity and roughness of the grown (aluminium oxide - AlO_x) or deposited (LDPE) thin film dielectrics, the difficulty in precisely quantifying their thickness, as well as the use of multi-layered structures made of different

materials (aluminium oxide and surface treatment), a numerical calculation of C_i can result in inaccurate values, which in turn, can yield misleading mobility calculation results. Moreover, in the case of thin films, k can be thickness dependent rather than constant. Also, dielectric materials, such as anodised AlO_x, are not stoichiometric [66], which results in variations of their dielectric constant depending on several growth factors. For these reasons, an experimental quantification of the capacitance of these thin-film insulators is advisable.

Furthermore, the need for precise C_i measurements is more imperative when devices with different gate stacks are compared; considering that different gate materials and especially their surface affects the overlaying semiconductor grain formation and their properties [60, 109], a good knowledge of C_i is crucial for the quantification of the actual effects of the dielectric/surface treatment combination on mobility.

5.1.1. Preparation

Three different sets of capacitors were prepared in clean-room facilities; the first employed OTS-treated aluminium oxide (AlO_x), the second AlO_x with an LDPE coating, and the third one was exclusively based on LDPE; hereafter, these capacitors are referred to as *AlOx-OTS*, *AlOx-LDPE* and *LDPE (only)*, respectively. All devices were built on cleaned silicon substrates with a top SiO_2 layer of 100 nm thickness; detailed information on substrate preparation is given in section 2.2.4.

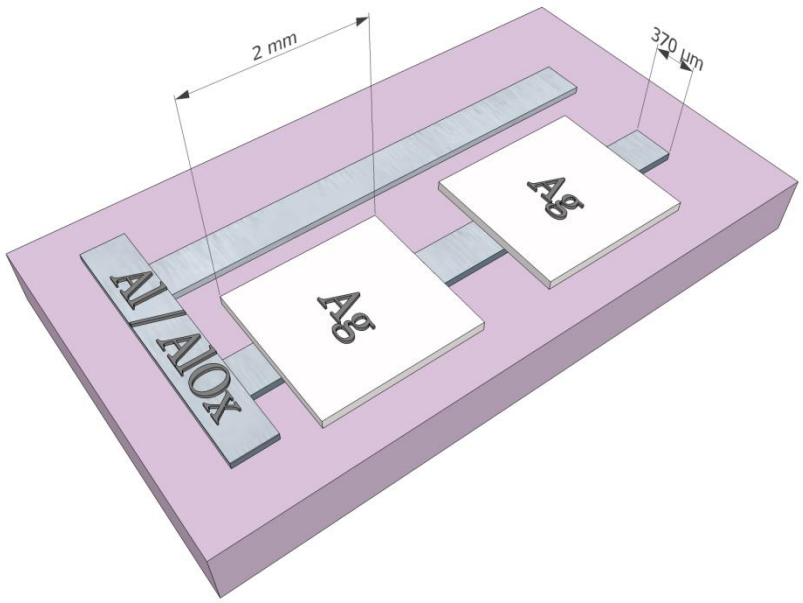

Figure 5-1 – A graphical representation of the AlOx-based capacitors. Area of overlap: 0.74 mm^2

For the AlO_x-based capacitors, an 100-nm-thick film of aluminium was initially deposited on the substrates through shadow masks; this layer served as the bottom electrode of the capacitors. The shadow masks patterned strips (fingers) of aluminium with a width of 370 µm. Each aluminium layer was anodised for the formation of a thin-film of AlO_x, which constituted the dielectric of the capacitor. The applied current was set at 0.95 mA with a voltage limit of 5 V; the current application time to each substrate was 75 seconds. More details on AlO_x formation are given in section 2.4.2.

For the AlO_x-OTS capacitors, the substrates were immersed into a 10 mg/mL cyclohexane solution of OTS. The application time was 10 minutes and the process took place in a nitrogen

glovebox. The substrates were rinsed with clean cyclohexane and let dry on a hot plate. More information on OTS application on oxides is given in section 2.4.3.

For the AlO_x-LDPE capacitors, a 20-nm-thick film of LDPE was deposited on the entire surface of the substrates by thermal evaporation in high vacuum. The starting pressure within the dome of the evaporator was 3.6 x 10^{-7} Torr and it was preserved below 6.3 x 10^{-7} Torr over the course of the deposition process; the deposition rate was roughly 10^{-2} nm/s. In contrast to the LDPE treatment for the OFET gate oxides, the LDPE thin films of these capacitors were not annealed after deposition. As demonstrated by Kanbur et al. [72], the annealing of such thin (20 nm) films of LDPE is advisable for a better coverage of the oxide surface. The impedance results from these devices, as discussed below, indicate a possible penetration of the top electrode metal into the LDPE layer during deposition; this observation can be a result of not annealing these films. More details are given below.

For the LDPE (only) capacitors, silver was selected as the bottom-electrode material. It was thermally evaporated and deposited through shadow masks of the same pattern as the ones used for AlO_x-based devices. On top of silver, a 400-nm-thick film of LDPE was deposited without the use of a shadow mask.

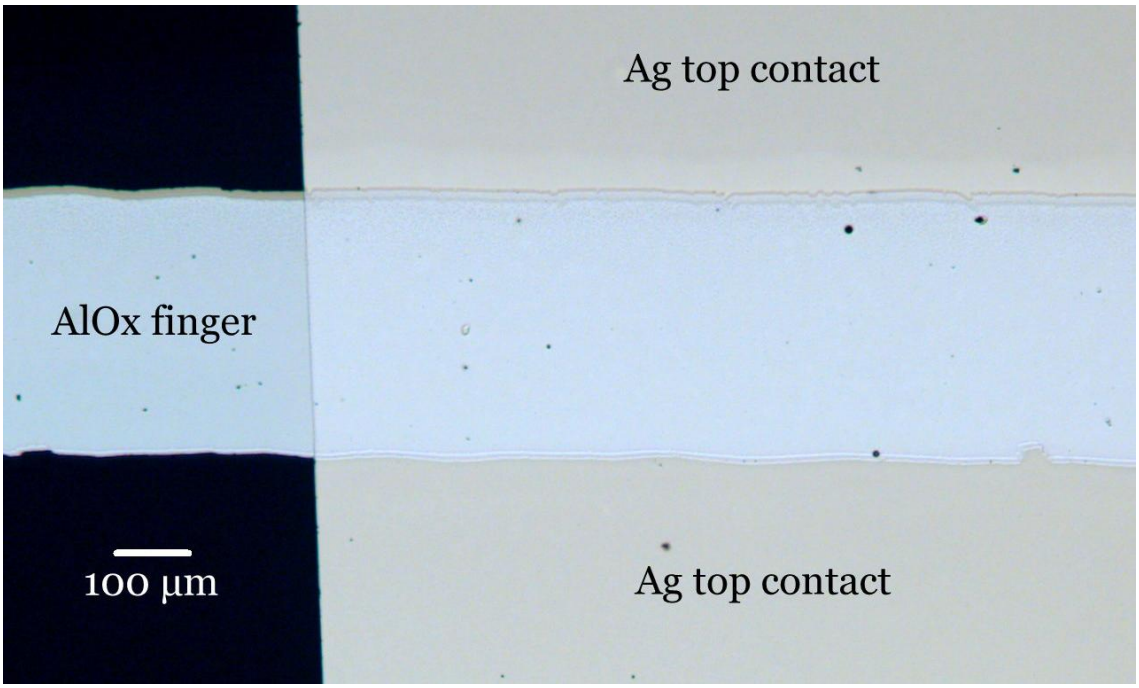

Figure 5-2 – Optical microscope top-down image of an AlO_x-OTS capacitor

Silver was the top-electrode-material of choice for all capacitors; for each substrate, a 40-nm-thick film was deposited through a shadow mask on top of the dielectric. Each top-electrode-pad had dimensions of 2 mm x 2 mm; the dimensions of overlap between each top electrode and the bottom aluminium or silver electrode were 2 mm x 370 µm, which give a total overlap area of 7.4 x 10^{-3} cm^2.

The fact that a few-nm-thick layer of silver is semitransparent makes the selection of top-silver-electrodes appropriate for the study of the effects of illumination on gate capacitance, as discussed in section 6.2.

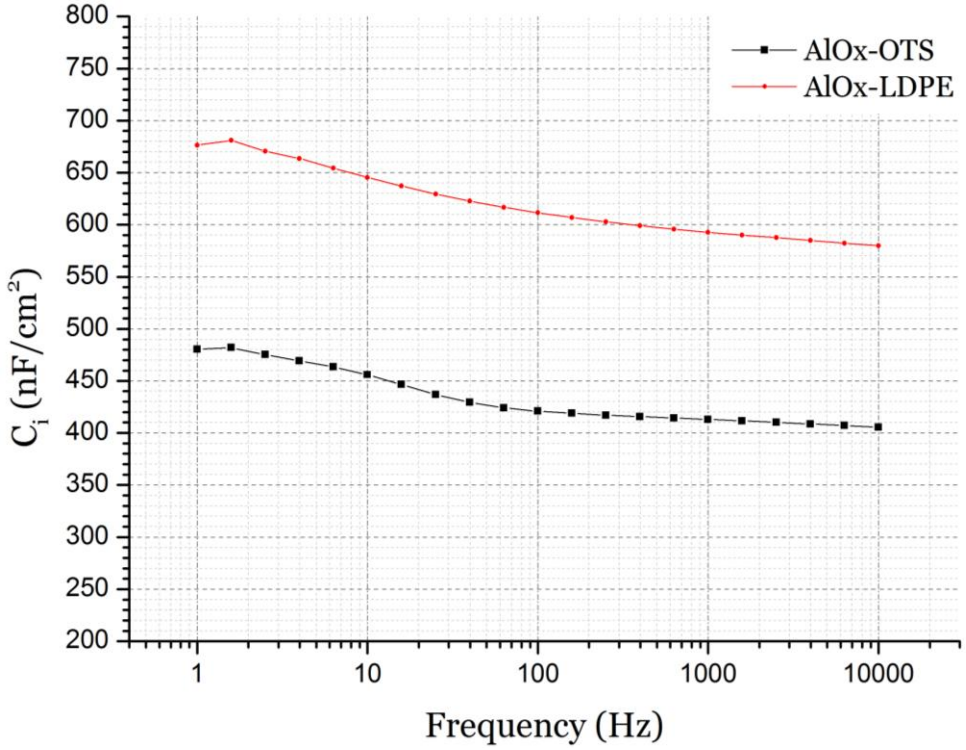

Figure 5-3 – Capacitance per unit area versus frequency for an AlO_x-OTS (black line) and an AlOx-LDPE (red line) capacitor in the dark.

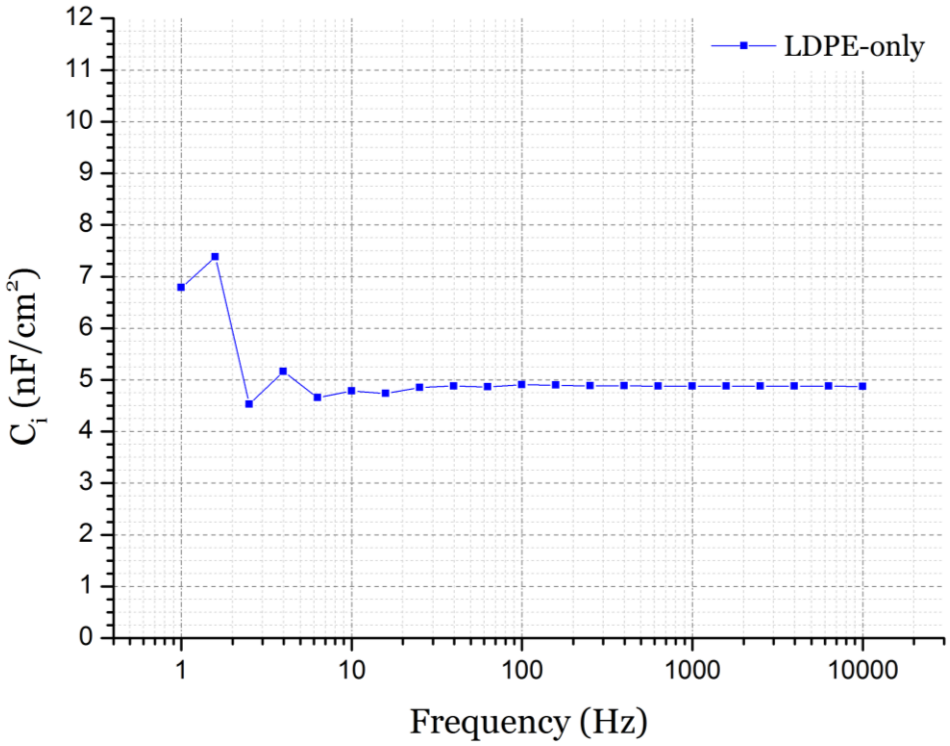

Figure 5-4 – Capacitance per unit area (C_i) versus frequency for an LDPE (only) capacitor in the dark. The dielectric thickness is roughly 400nm. The scattered data points in the frequency range from 1 Hz to 10 Hz are an artefact that was observed in all impedance measurements taken using this instrument; this effect is more pronounced in this example due to the relatively small C_i of the device under test.

The impedance measurement test rig is described in detail in section 3.2. The applied drive was a zero-offset AC drive with an amplitude of 1 V, for a frequency range from 1 Hz to 10 KHz. The leakage current of the capacitors under test was not recorded by the impedance analyser,

thus no results are shown here. However, notable leakage currents were only observed in the output characteristics of very few fabricated OFETs, as discussed in the following sections.

5.1.2. Results and discussion

Figure 5-3 and Figure 5-4 show the capacitance per unit area (C_i) versus frequency for the AlO_x-based and LDPE (only) capacitors, respectively. The frequency of 6.33 Hz was selected as the reference frequency, as most of the real-time measurements using the I-V converter system applied a sinusoidal drive with a frequency of 6 Hz.

At the reference frequency of 6.33 Hz, the LDPE (only) capacitor exhibited a very low C_i of roughly 5 nF/cm^2, which comes in good agreement with numerical calculations based on the reported values of the dielectric constant of LDPE, i.e. 2.2 to 2.35 [110].

At the same frequency, the AlO_x-based capacitors were found to have high C_i values that were in the same order of magnitude as previously reported values [65]. The LDPE-treated oxide exhibited a C_i of 675 nF/cm^2, whereas the value of OTS-treated was 470 nF/cm^2.

However, the value of the LDPE-treated device deviates from the anticipated values; considering that the capacitance per unit area of 20-nm-thick layer alone ($C_{i,LDPE}$) has a value of ~100 nF/cm^2 and that the total C_i of the bilayer can be calculated from:

$$\frac{1}{C_i} = \frac{1}{C_{i,AlOx}} + \frac{1}{C_{i,LDPE}} \tag{5.3}$$

it can be easily deduced that $C_i < 100\ \mathrm{nF/cm^2}$. As mentioned above, the very thin LDPE layers of these capacitors were not annealed after deposition, which probably resulted in an incomplete coverage of the oxide surface; Kanbur *et al.* have underlined this situation with the aid of AFM images [72]. In the same work, the reported value for an annealed 8-nm-AlO_x / 20-nm-LDPE bilayer was 96 nF/cm^2. If we consider that a value of 600 to 700 nF/cm$_2$ for $C_{i,AlOx}$ alone is normal [65], the measured values can be explained by the fact that it is very likely that the silver deposited on top of the LDPE layer actually came in direct contact with the AlO_x layer by penetrating the LDPE layer.

Moreover, in the case of the AlO_x-OTS capacitors, if we assume that the AlO_x layer has a $C_{i,AlOx}$ of ~700 nF/cm^2, that the thickness of a single monolayer of OTS has been reported to be 2.6 to 2.8 nm [71, 111] and that measured value was 470 nF/cm^2, it can be estimated that the actual OTS treatment does not consist of only a single monolayer but a polymerised network of OTS molecules due to the presence of adsorbed humidity on the oxide surface; this situation is discussed in section 2.4.3.

For the mobility calculations discussed in the following sections of this chapter, the measured C_i values for the AlO_x-OTS and the LDPE (only) dielectrics were used, whereas, for the AlO_x-LDPE calculations, a numerically approximated value of C_i (98 nF/cm^2) was used instead. For the OFETs built on the 100-nm- and 300-nm-thick SiO_2 gate dielectrics, the effect of the surface treatment on the C_i of the dielectric is negligible; hence, the numerically calculated values of 27 nF/cm^2 and 9 nF/cm^2, respectively, were used.

5.2. Pentacene OFETs

Pentacene is one of the best studied organic semiconductors. There are numerous published papers on OFETs employing pentacene; these examples include high-performance OFETs with mobility values as high as 8.85 $cm^2V^{-1}s^{-1}$ [79], small integrated circuits such as ring oscillators on flexible substrates [112], as well as temperature, humidity and vapour sensing transducers [83, 113, 114].

Pentacene was the most used organic semiconductor in the work presented here. Several different configurations with various fabrication conditions were tested. This section discusses the results from measurements on representative examples of each configuration. The results have been categorised with respect to the employed gate dielectric.

5.2.1. Silicon-dioxide-gated devices

Silicon dioxide (SiO_2) is by far the most used gate dielectric in both inorganic and organic FETs. In this work, SiO_2 is used as a reference material, as the focus was mainly put on AlO_x and LDPE dielectrics. The fabrication procedure and the characterisation results of SiO_2-based pentacene OFETs with OTS and LDPE surface treatment are presented in this section.

5.2.1.1. *Preparation*

Arsenic-doped silicon substrates with a 100-nm-thick thermal oxide were used. The substrates were initially cleaned by sonication in an alkaline solution and in IPA and UV-ozone treatment. A detailed description on substrate preparation is given in section 2.2.4.

For the OTS-treatment, the cleaned substrates were immersed into a cyclohexane solution of OTS (10 mg/mL) for 60 minutes. The process took place in a nitrogen glove box.

For the LDPE-treatment, a 20-nm-thick film of LDPE was deposited using thermal evaporation; the deposition rate varied between 0.007 and 0.01 nm/s and the pressure within the dome of the evaporator was roughly 8.0 x 10^{-7} Torr. The substrates were annealed at 105 °C in vacuum for 30 minutes.

Pentacene was thermally evaporated and deposited onto both substrate sets. The final film thickness was 50 nm, the deposition rate varied from 0.05 to 0.078 nm/s, while the pressure was roughly 8.5 x 10^{-7} Torr.

Finally, gold was deposited through shadow masks using thermal evaporation. The final thickness of the patterned top electrodes was 50 nm and the dimensions of the channels were 10 µm (length) by 2 mm (width). The deposition rate varied from 0.015 to 0.055 nm/s, while the pressure was limited below 3.3 x 10^{-6} Torr throughout the evaporation process.

5.2.1.2. *Electrical characteristics*

All measurements were taken in ambient conditions, i.e. at room temperature and under usual room light conditions. Figure 5-5 to Figure 5-7 show the output and transfer characteristics of these two devices. The output characteristics from both the OTS- and the LDPE-treated devices show that the curves poorly saturate.

The threshold voltages of both devices were found to be rather low, namely -1.4 V for OTS and -2.4 V for LDPE. The OTS-treated device outperformed the LDPE-treated one in terms of mobility; their calculated values were 0.105 $cm^2V^{-1}S^{-1}$ and 0.057 $cm^2V^{-1}S^{-1}$, respectively.

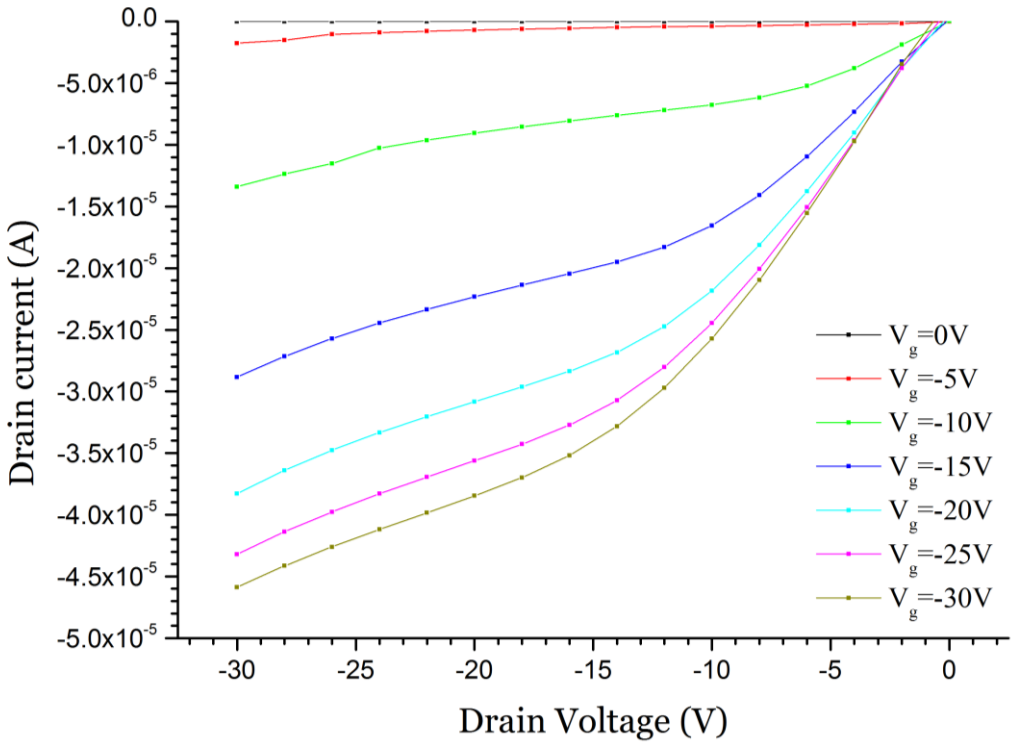

Figure 5-5 – Output characteristics of a top-gold-contact pentacene OFET based on SiO_2-OTS dielectric.

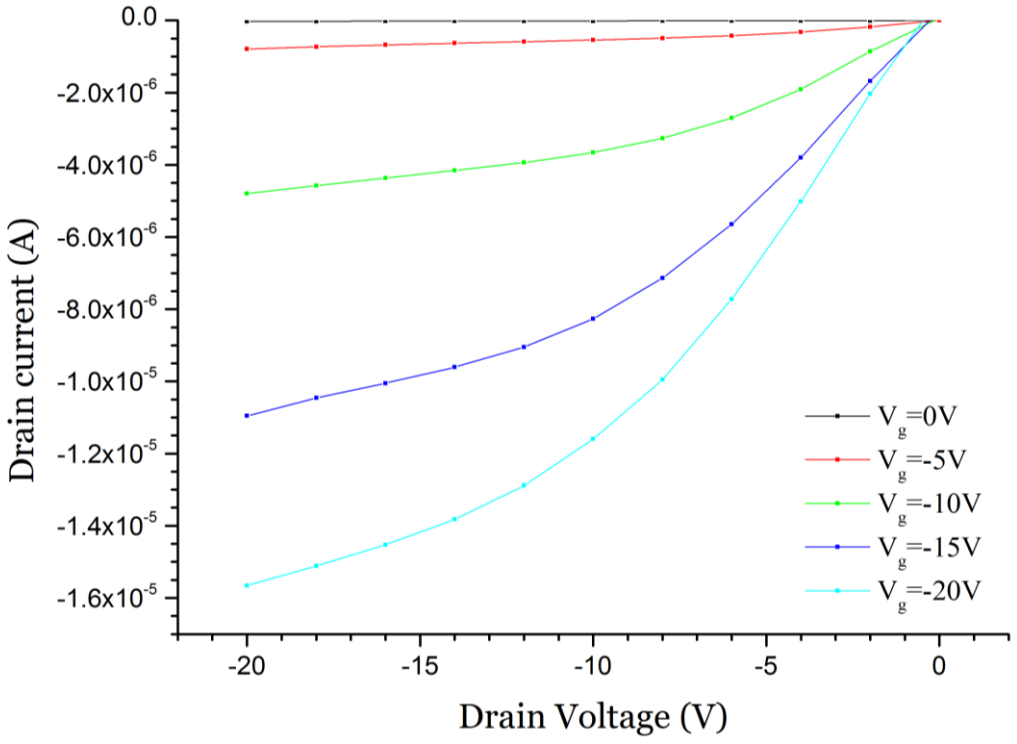

Figure 5-6 – Output characteristics of a top-gold-contact pentacene OFET based on SiO_2-LDPE dielectric.

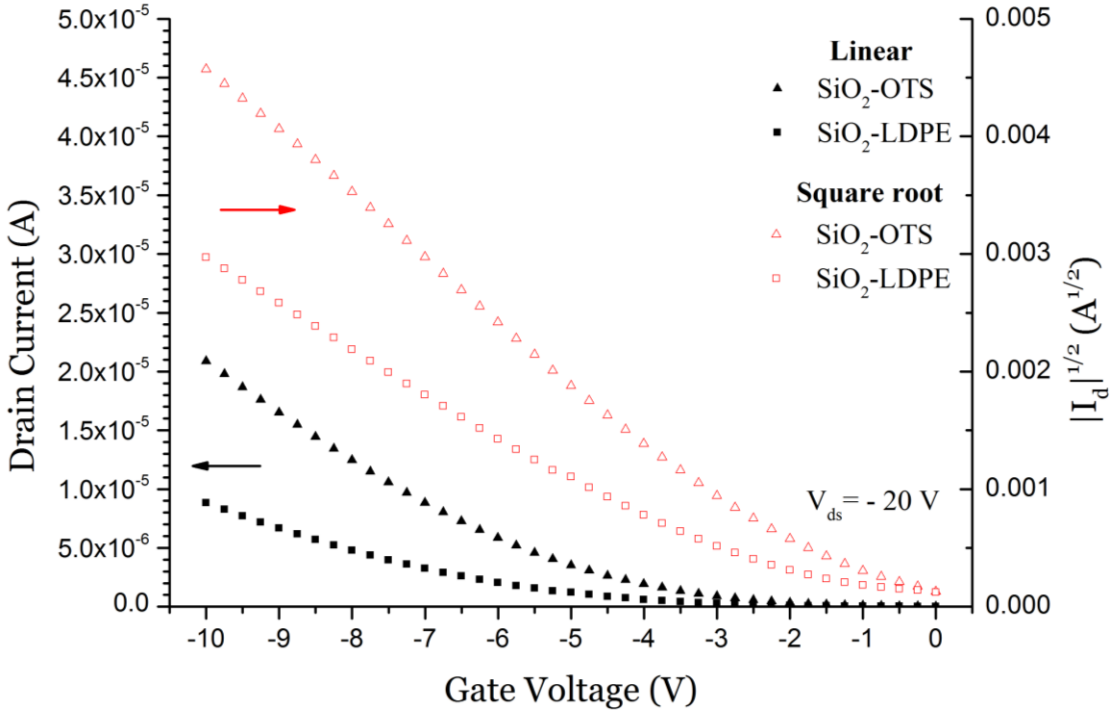

Figure 5-7 – Transfer characteristics of a pentacene OFET with SiO_2-OTS dielectric (triangles) and a pentacene OFET with SiO_2-LDPE dielectric (squares).

5.2.2. Aluminium-oxide-gated devices

In this section, the preparation process for pentacene OFETs, which employ aluminium oxide as their gate dielectric material, is presented. Two different structural approaches were studied; the first batch of devices was based on oxide which was treated with OTS, whereas the second one was based on LDPE-treated oxide. Hereafter, these devices are referred to as AlO_x-OTS and AlO_x-LDPE, respectively.

5.2.2.1. *Preparation*

Silicon substrates bearing an 100-nm-thick oxide were used. They were cleaned by sonication in an alkaline solution and IPA and undergone UV-ozone treatment. A detailed description on substrate preparation is given in section 2.2.4.

An 100-nm-thick aluminium layer was deposited by thermal evaporation through shadow masks in high vacuum. The pressure within the evaporator dome was 6.1 x 10^{-7} Torr in the beginning of the deposition process and reached a maximum of 2.5 x 10^{-6} Torr during the evaporation. The deposition rate was adjusted at roughly 10^{-3} nm/s for the first 10nm and it was then gradually increased up to 5.0 x 10^{-1} nm/s.

The aluminium films were anodised in a 1 mM citric acid solution. The applied current was set at 0.95 mA and the maximum voltage at 5 V. The current application time was 75 seconds. The devices were rinsed with DI water and dried before further process. Detailed information on aluminium anodisation can be found in section 2.4.2.

For the AlO_x-OTS devices, the substrates were immersed into a 10 mg/mL cyclohexane solution of OTS for 10 minutes. This process took place in a nitrogen glove box. Following that, the substrates were thoroughly rinsed with clean cyclohexane and dried on a hot plate. Further details on OTS treatment are given in section 2.4.3.

For the AlO_x-LDPE devices, a 20-nm-thick film of LDPE was deposited on the substrates after the aluminium anodisation process. No shadow masks were used, so LDPE covered the entire surface of the substrates. The starting pressure was 6.3 x 10^{-7} Torr, whereas the maximum pressure during evaporation was 9.5 x 10^{-7} Torr. The deposition rate was being varied between 0.065 and 0.08 nm/s throughout the entire process. These substrates were later annealed at 105 °C in vacuum for 30 minutes. The LDPE-treatment of oxides is discussed in section 2.4.5.

Pentacene was thermally evaporated so that a 50-nm-thick was deposited on the entire surface of all substrates. The pressure ranged from 7.6 x 10^{-7} Torr in the beginning to 8.7 x 10^{-7} Torr during the evaporation. The deposition rate was limited to 5.0 x 10^{-2} nm/s for the first 10 nm and was then increased to 7.8 x 10^{-2} nm/s until the end of the process. The substrates were not further heated during the thin-film deposition.

Gold was also deposited by thermal evaporation though shadow masks. Each substrate was fitted with one mask which patterns four source-drain pairs on the surface of the substrate; the dimensions of the resulting OFET channels are 10 μm (length) x 2 mm (width). The masks were aligned in such a way that the channel overlaps with the underlying gate electrode and oxide. The deposition rate was limited below 0.015 nm/s for the first 10 nm and was then increased to roughly 0.045 nm/s until a final thickness of 50 nm was deposited. The pressure was kept below 3.3 x 10^{-6} Torr.

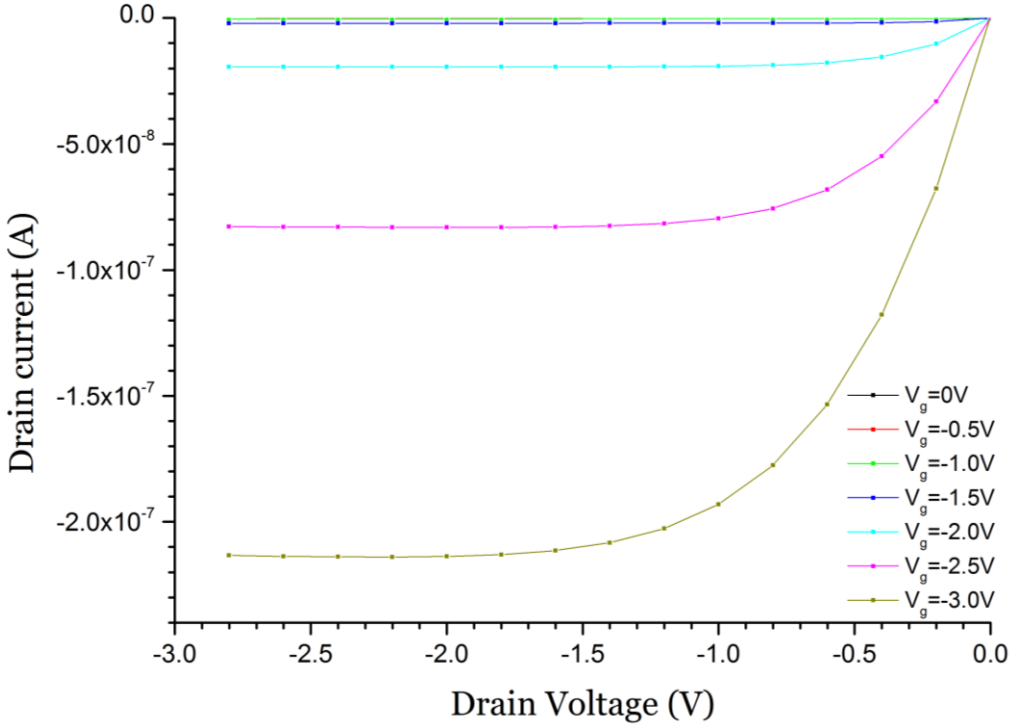

Figure 5-8 – Output characteristics of a top-gold-contact pentacene OFET based on AlO_x-OTS dielectric.

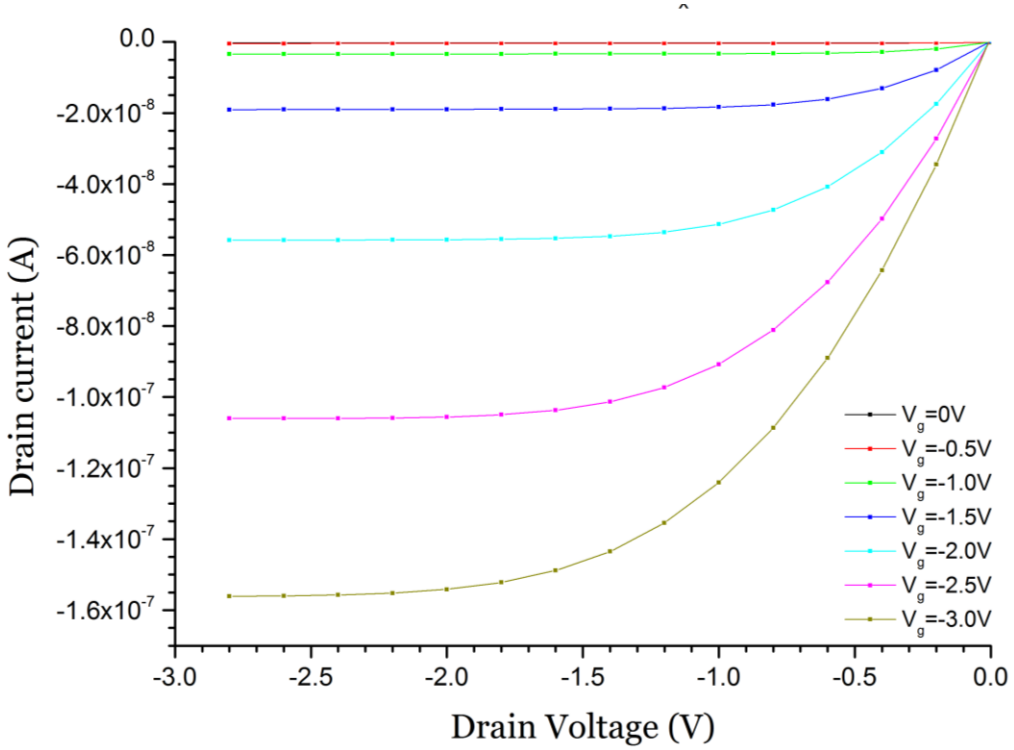

Figure 5-9 – Output characteristics of a top-gold-contact pentacene OFET based on AlO_x-LDPE dielectric.

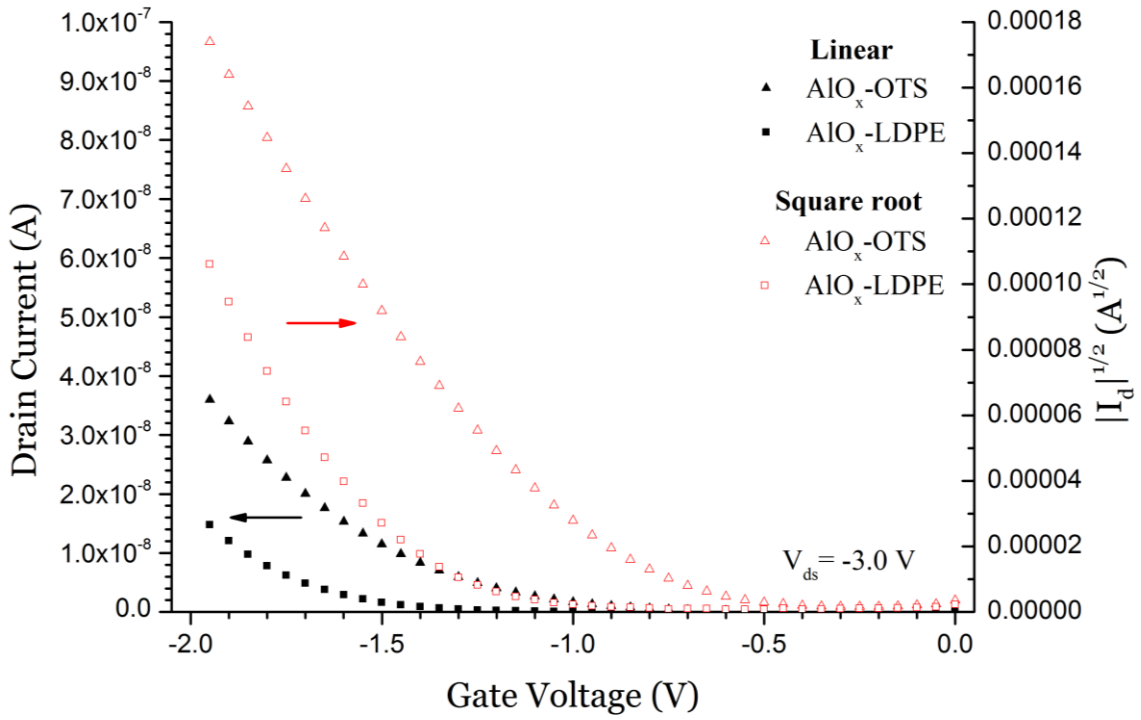

Figure 5-10 – Transfer characteristics of two top-gold-contact pentacene OFETs based on AlO$_x$-OTS (triangles) and AlO$_x$-LDPE (squares).

5.2.2.2. *Electrical characteristics*

All measurements were taken in ambient conditions, i.e. at room temperature and under usual room light conditions. Similar to the SiO_2-gated devices discussed in section 5.2.1, the OTS treatment resulted in better electrical characteristics. The threshold voltage of the AlO$_x$-OTS device was -1.0 V and that of the AlO$_x$-LDPE was slightly higher, at roughly -1.4 V.

The mobility was calculated at 7.0 x 10^{-4} $cm^2V^{-1}s^{-1}$ for the AlO$_x$-OTS OFET and 3.1 x 10^{-3} $cm^2V^{-1}s^{-1}$ for the AlO$_x$-LDPE one; these values are much lower than those of the SiO_2-gated devices, discussed in section 5.2.1; however, mobility values of this order-of-magnitude are common for non-heated substrates [44] and a similar relative decrease in mobility has been reported for *poly(triaryl amine)* (*PTAA*) OFETs built on AlO$_x$ dielectric [51]. An explanation for these relatively low values can be sought in the high surface roughness of both AlO$_x$ surfaces; the AFM images shown in Figure 5-11 and Figure 5-12 illustrate the surface of an area of evaporated aluminium before and after anodisation, respectively, while Figure 5-13 and Figure 5-14 show the pentacene surfaces of the channel areas of the AlO$_x$-OTS and AlO$_x$-LDPE OFETs, respectively.

Despite the higher modulus of V_{th}, the LDPE-treated devices exhibited remarkably higher mobility performance compared to the OTS-treated ones. Moreover, additional comparative studies on the environmental stability of these devices suggest that LDPE can be an excellent candidate for highly stable devices; calculations of their interfacial trap densities are given in section 5.2.2.3, air degradation measurements are discussed in section 5.2.2.4 and a detailed study on light-stability of AlO$_x$-based pentacene OFETs is presented in section 6.3.

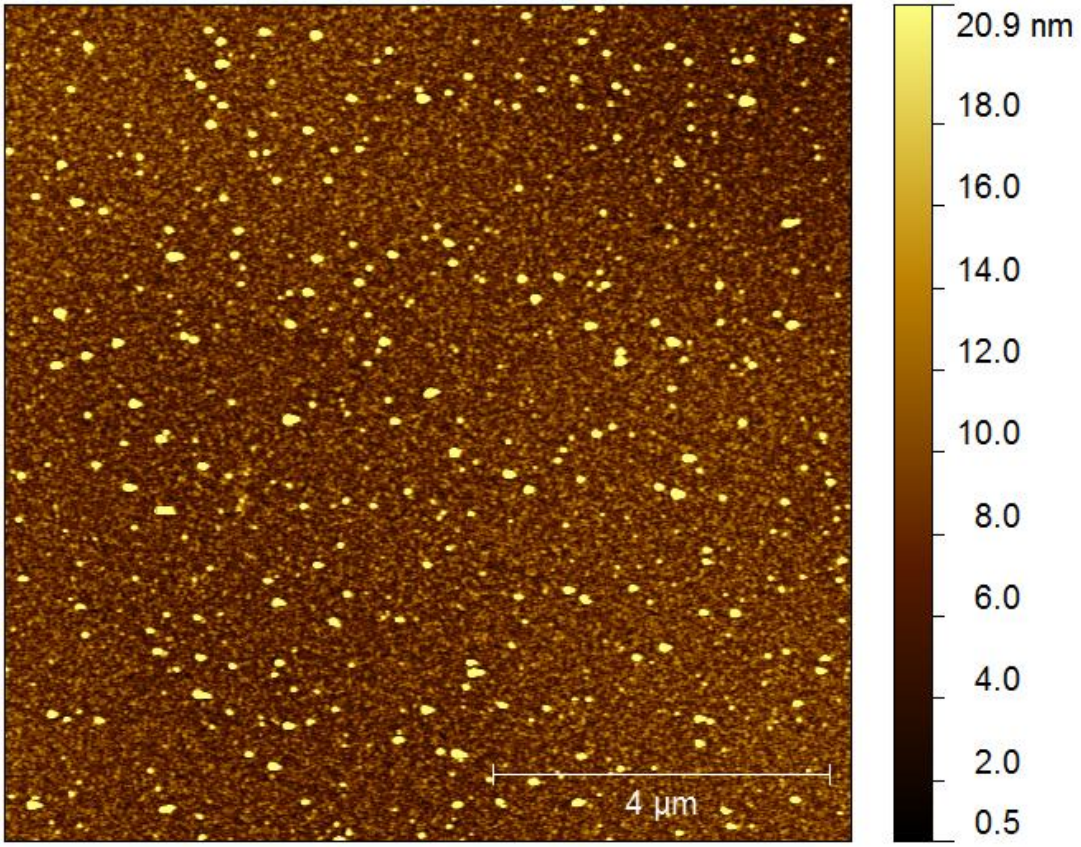

Figure 5-11 – AFM image of an aluminium area deposited on a Si/SiO_2 substrate.

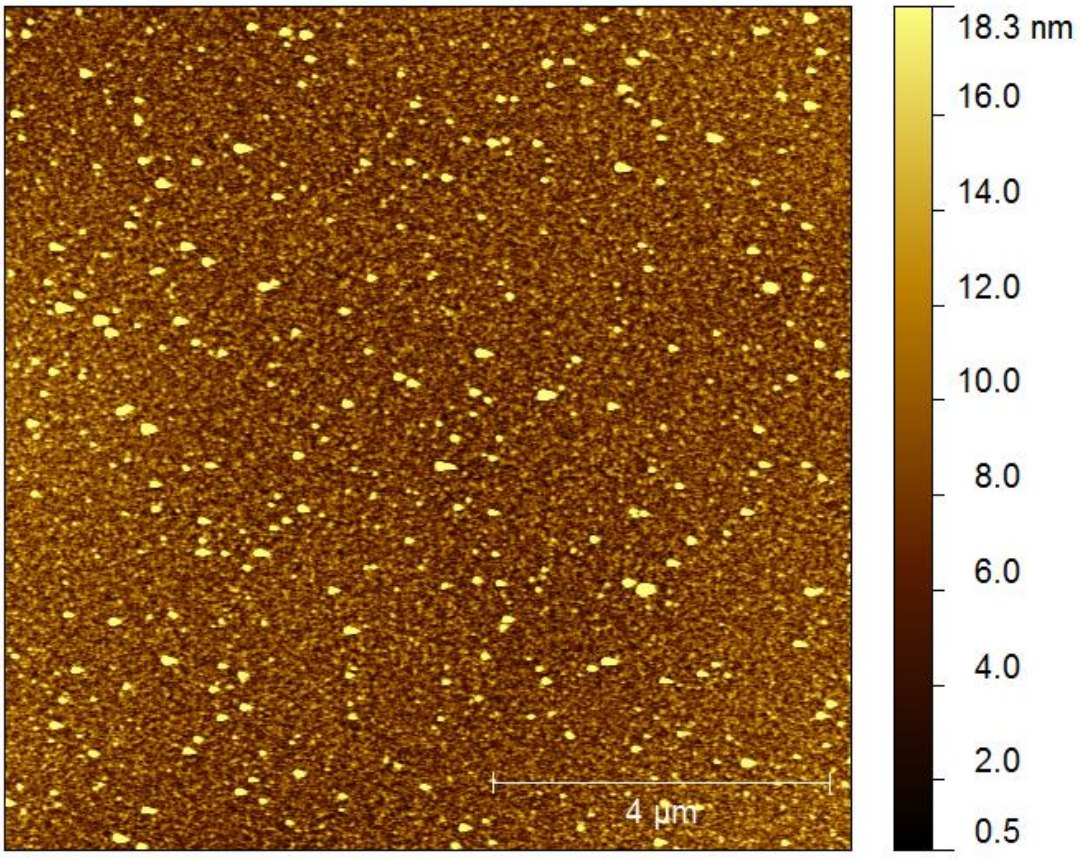

Figure 5-12 – AFM image of an anodised aluminium area deposited on a Si/SiO_2 substrate.

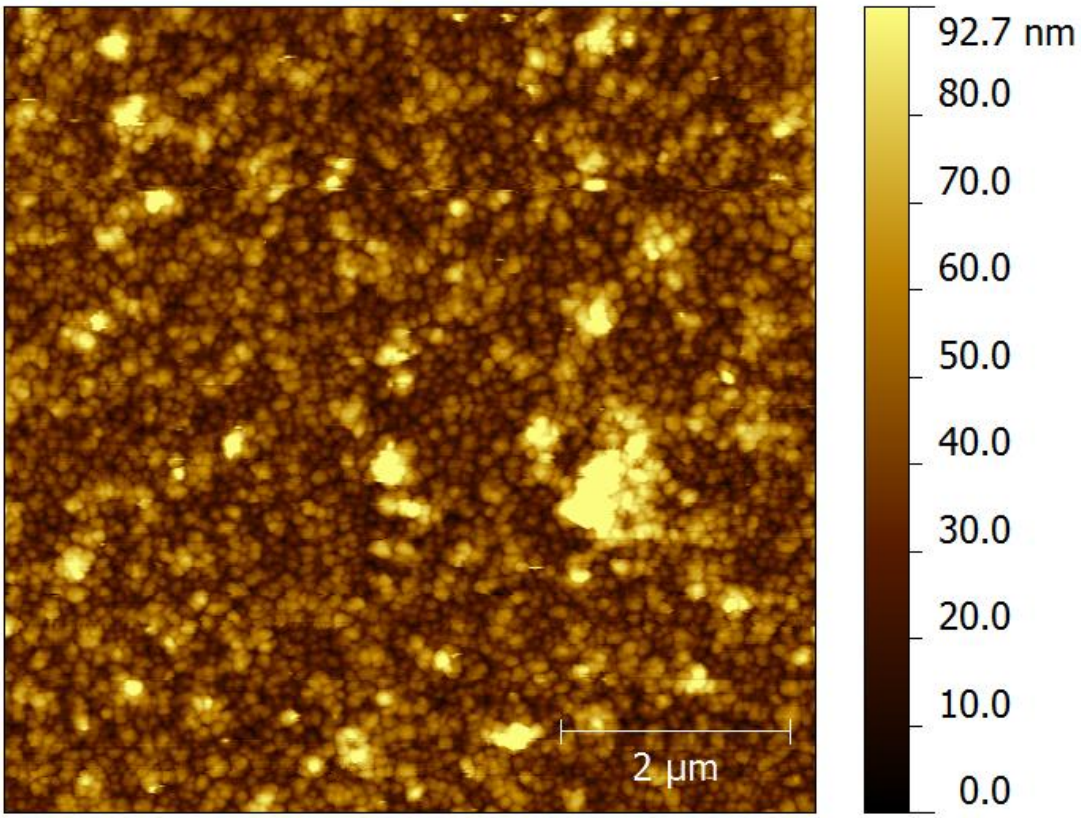

Figure 5-13 – AFM image of the channel area of a pentacene OFET with AlO_x-OTS dielectric

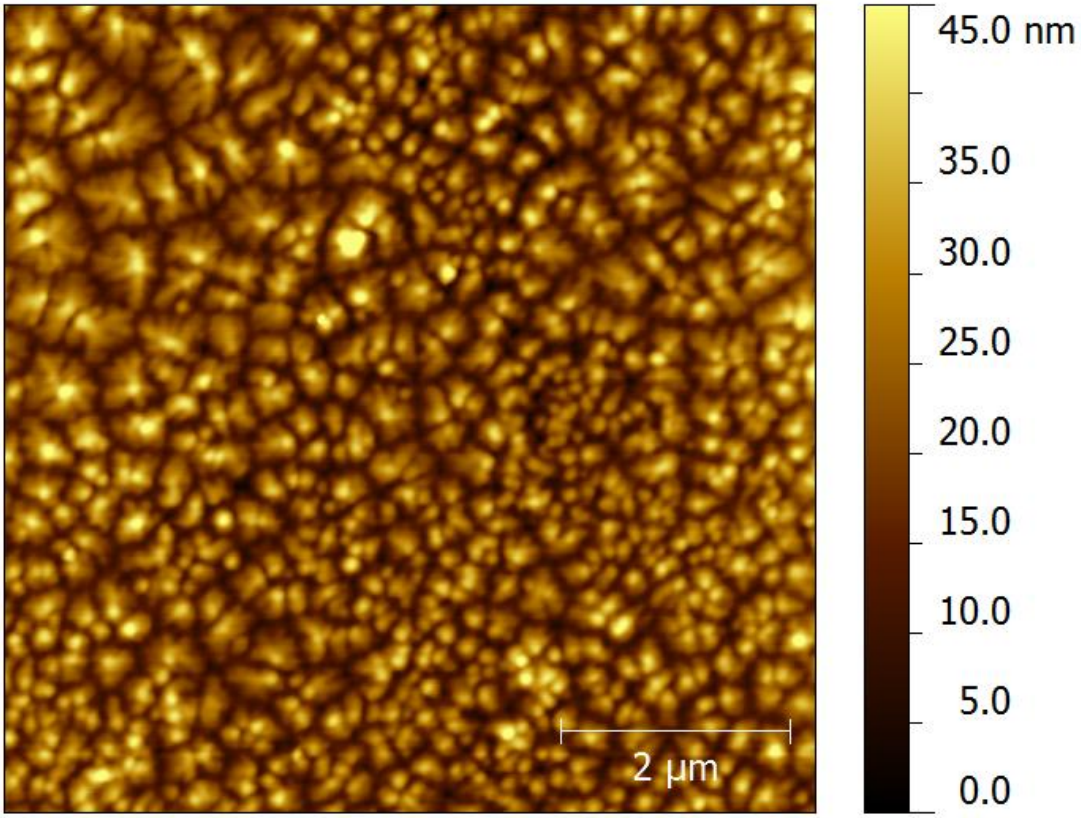

Figure 5-14 – AFM image of the channel area of a pentacene OFET with AlO_x-LDPE dielectric

5.2.2.3. *Oxide surface treatment and traps*

A rough estimation of interfacial trap densities can be derived from the subthreshold transfer characteristics of the two tested devices.

In a variation of eq. (2.6), the subthreshold swing of the two OFETs can be expressed as:

$$S_{AlOx-OTS} = \frac{kT \ln 10}{q}\left[1 + \frac{q^2}{C_{i-AlOx/OTS}} N_{AlOx/OTS}\right] \tag{5.4}$$

and:

$$S_{AlOx/LDPE} = \frac{kT \ln 10}{q}\left[1 + \frac{q^2}{C_{i-AlOx/LDPE}} N_{AlOx/LDPE}\right] \tag{5.5}$$

where C_i is the capacitance per unit area of each combination of dielectrics, q is the elementary charge, ε_s is the dielectric constant of pentacene, N_{bulk} is the density of traps in the bulk of the pentacene film and $N_{AlOx/OTS}$ and $N_{AlOx/LDPE}$ are the total densities of traps, including the bulk traps in the semiconductor film and the traps at the interface of each device. In the absence of traps, the ideal subthreshold swing is approximately 57 mV/dec at room temperature.

Assuming that the bulk trap density is the same for both OFETs, regardless of their dielectric surface treatment, a difference in the total trap densities is exclusively due to a difference in their interface trap densities. The ratio of the two swings is:

$$\frac{S_{AlOx/OTS}}{S_{AlOx/LDPE}} = \frac{1 + \frac{q^2}{C_{i-AlOx/OTS}} N_{AlOx/OTS}}{1 + \frac{q^2}{C_{i-AlOx/LDPE}} N_{AlOx/LDPE}} \tag{5.6}$$

The subthreshold swing values, shown in Figure 5-15 and Figure 5-16, are:

$$S_{AlOx/OTS} = 884\ {}^{\mathrm{mV}}/_{\mathrm{dec}} \tag{5.7}$$

and

$$S_{AlOx/LDPE} = 609\ {}^{\mathrm{mV}}/_{\mathrm{dec}} \tag{5.8}$$

Considering that $S_{AlOx/OTS}$ and $S_{AlOx/LDPE}$ are similar, we can simplify eq. (5.6) by letting:

$$\frac{S_{AlOx/OTS}}{S_{AlOx/LDPE}} \cong 1 \tag{5.9}$$

Substituting into eq. (5.6) yields:

$$\frac{N_{AlOx/OTS}}{N_{AlOx/LDPE}} \cong \frac{C_{i-AlOx/OTS}}{C_{i-AlOx/LDPE}} \tag{5.10}$$

From the impedance measurements and the calculations given in section 5.1:

$$C_{i-AlOx/OTS} = 480\ {}^{\mathrm{nF}}/_{\mathrm{cm}^2} \tag{5.11}$$

and

$$C_{i-AlOx/LDPE} = 98\ {}^{\mathrm{nF}}/_{\mathrm{cm}^2} \tag{5.12}$$

From substitution into eq. (5.10), it can be derived:

$$N_{AlOx/OTS} \cong 5 N_{AlOx/LDPE} \tag{5.13}$$

Thus, the comparison of the respective subthreshold swings and the dielectric capacitances indicates a much higher trap density at the OTS-treated interface as compared to the LDPE-treated one.

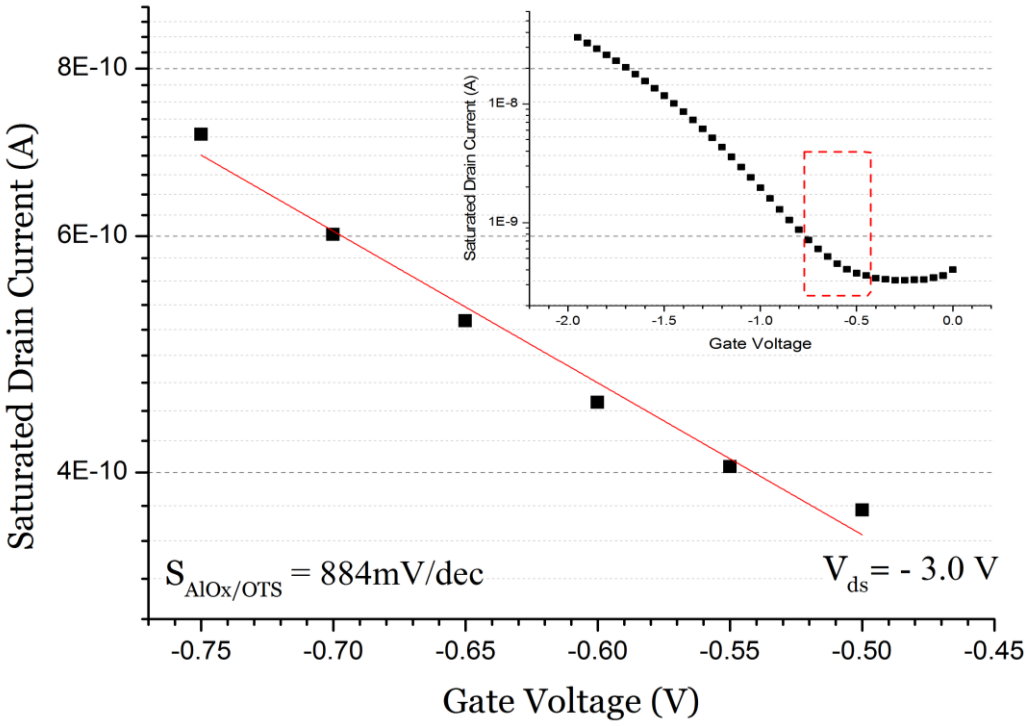

Figure 5-15 – Subthreshold transfer characteristics of a top-gold-contact pentacene OFET based on AlOx-OTS dielectric.

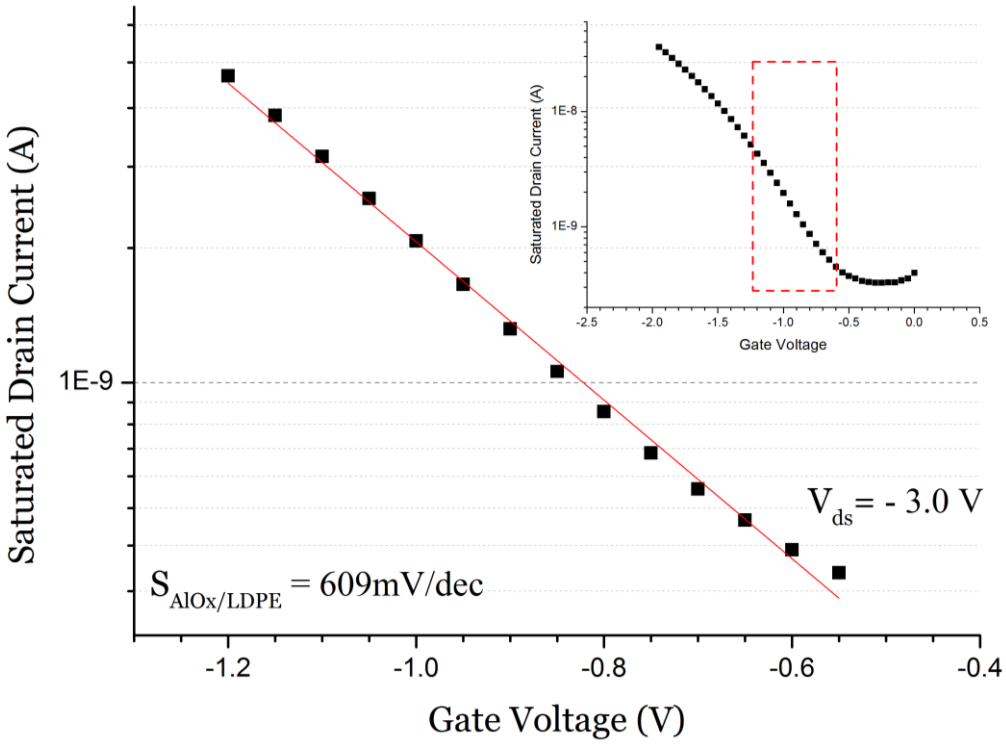

Figure 5-16 – Subthreshold transfer characteristics of a top-gold-contact pentacene OFET based on AlOx-LDPE dielectric.

5.2.2.4. *Air degradation and temperature dependence*

A comparative study on the impact of the two different surface treatments of AlO_x on the OFET air stability was performed. Despite the initial resemblance of the AlO_x-OTS and AlO_x-LDPE devices, in terms of saturated drain current, the devices showed different performance degradation rates in ambient conditions. All devices were stored in ambient air and in dark conditions; their electrical performance was studied with the use of the I-V converter system over the course of 14 days.

As shown in Figure 5-17, after nine days, the LDPE-treated device exhibited a saturated drain current drop of one order-of-magnitude, whereas the decrease of the OTS-treated one was five times larger than that. Figure 5-18 shows multiple plots of the square root of the modulus of drain current versus drive voltage for both devices over several days; these curves clearly show the falling trend of their slopes, which indicate a drop in mobility over time.

Considering that the initial measurements were taken in standard room light conditions and not in absolute dark, the initial drop can be partly attributed to the higher sensitivity of OTS-treated devices to light. However, the further mobility degradation trends reveal that the pentacene film morphology which results from an OTS-treated surface is more susceptible to the ambient conditions than that on an LDPE-treated one.

An explanation can be sought in the AFM images shown in Figure 5-13 and Figure 5-14; the pentacene film surface on OTS-treated AlO_x had a very repeatable pattern with small grains of similar dimensions, whereas its counterpart, built on LDPE-treated AlO_x, had a random grain pattern with much larger aggregates. The repeatable pattern of pentacene grains on an Al_2O_3-OTS dielectric and the resulting enhanced mobility have been previously underlined by Kalb *et al.* [68]; however, this small-grain pattern results in larger total grain boundaries which, in turn, create a larger surface area for interactions between the pentacene molecules and airborne species, such as oxygen [81, 82], water [83], and ozone [82], which reportedly play a role in mobility degradation.

In addition, temperature sensitivity measurements were conducted; an AlO_x-OTS and an AlO_x-LDPE pentacene OFETs were placed on a programmable hot-plate (*Linkam TMS 94*) while their transfer characteristics were evaluated. It is worth mentioning that a temperature sensor which exploited the subthreshold characteristics of a pentacene OFET has previously been demonstrated by Jung *et al.* [113].

Figure 5-19 and Figure 5-20 show the transfer characteristics of the two devices at seven different temperature levels from 25 °C to 55 °C; higher temperatures were not attempted so that major alterations in the grain formation of both the LDPE and the pentacene films were avoided. Threshold voltages were not affected by the elevated temperature in both cases. Interestingly, despite the noticeable differences in pentacene grain formation, the relative mobility dependence on temperature was not affected by the AlO_x surface treatment. As shown by the AFM images in Figure 5-13 and Figure 5-14, for a temperature increase of 30 °C, i.e. from 25 °C to 55 °C, both devices showed a very similar mobility increase. The AlO_x-OTS device exhibited a change of +36.8%, while the change for AlO_x-LDPE one was +35.7%.

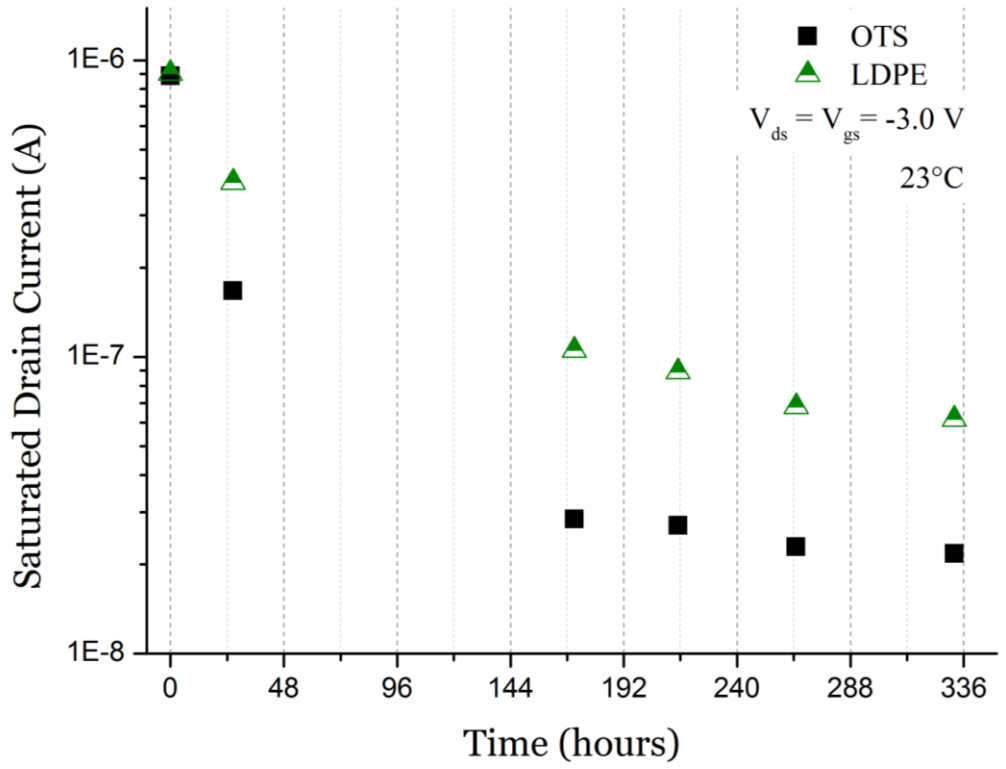

Figure 5-17 – Maximum saturated drain current versus time for two pentacene OFETs, based on AlO_x-OTS (black squares) and AlO_x-LDPE (green triangles) dielectrics.

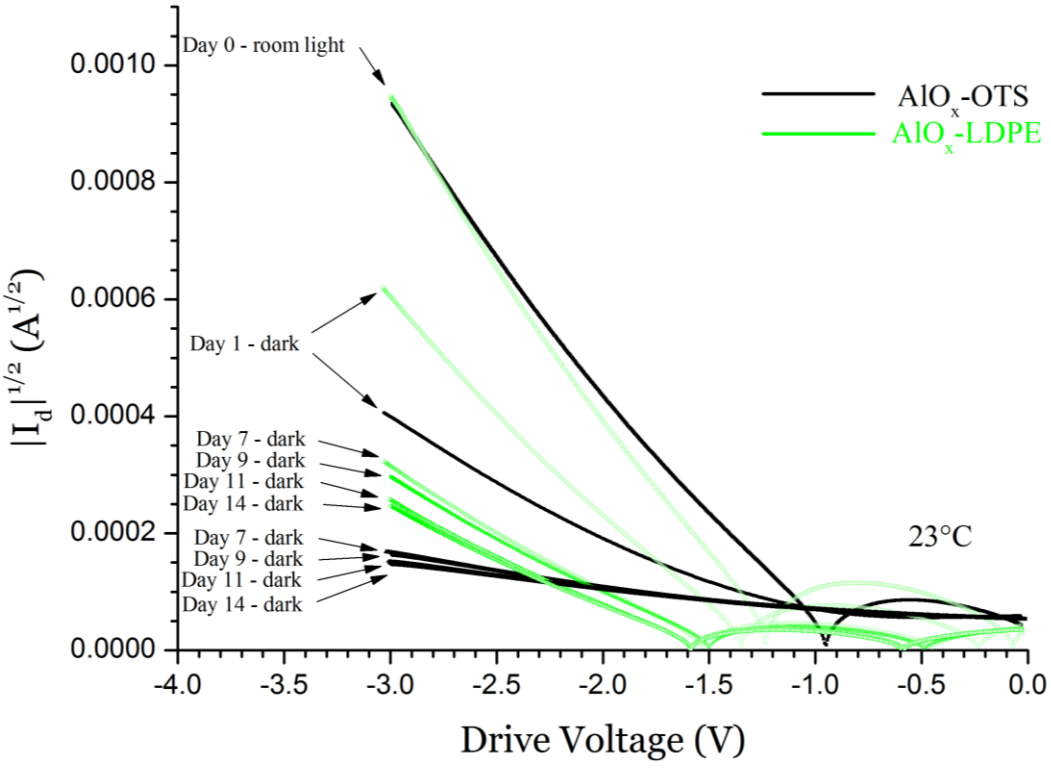

Figure 5-18 – Converted transfer characteristics from the I-V converter measurements on pentacene based on AlO_x-OTS (black curves) and AlO_x-LDPE (green curves) dielectrics over a period of 14 days.

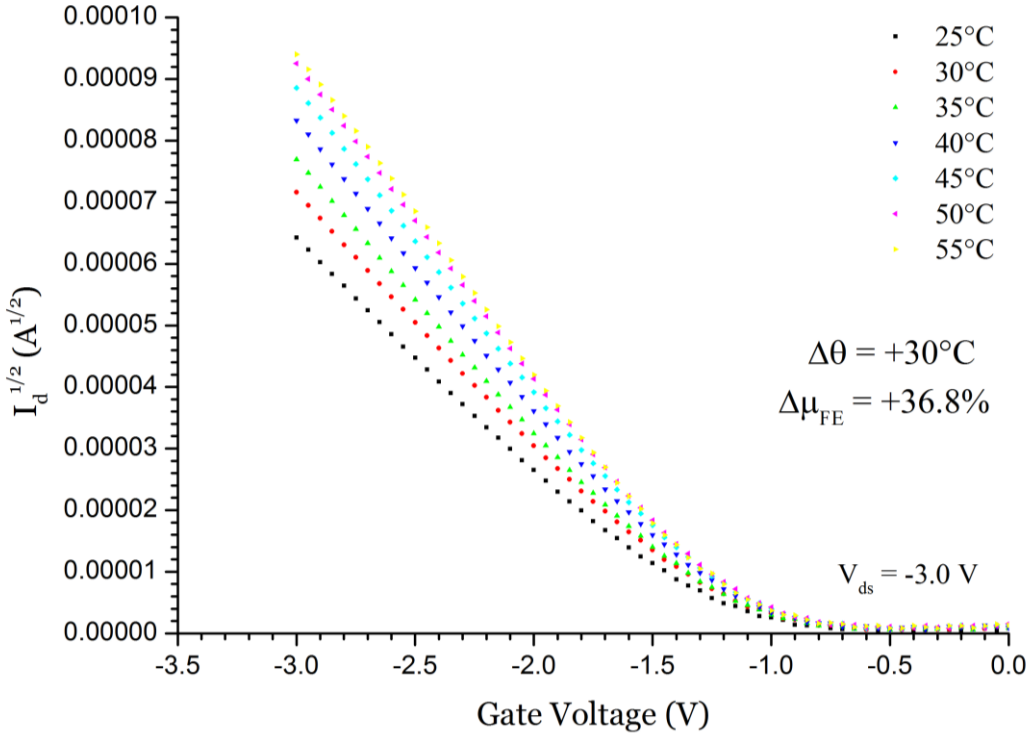

Figure 5-19 – Multiple plots of the square root of drain current versus gate voltage for a top-gold-contact pentacene OFET based on AlO_x-OTS dielectric at various temperatures, ranging from 25 °C to 55 °C.

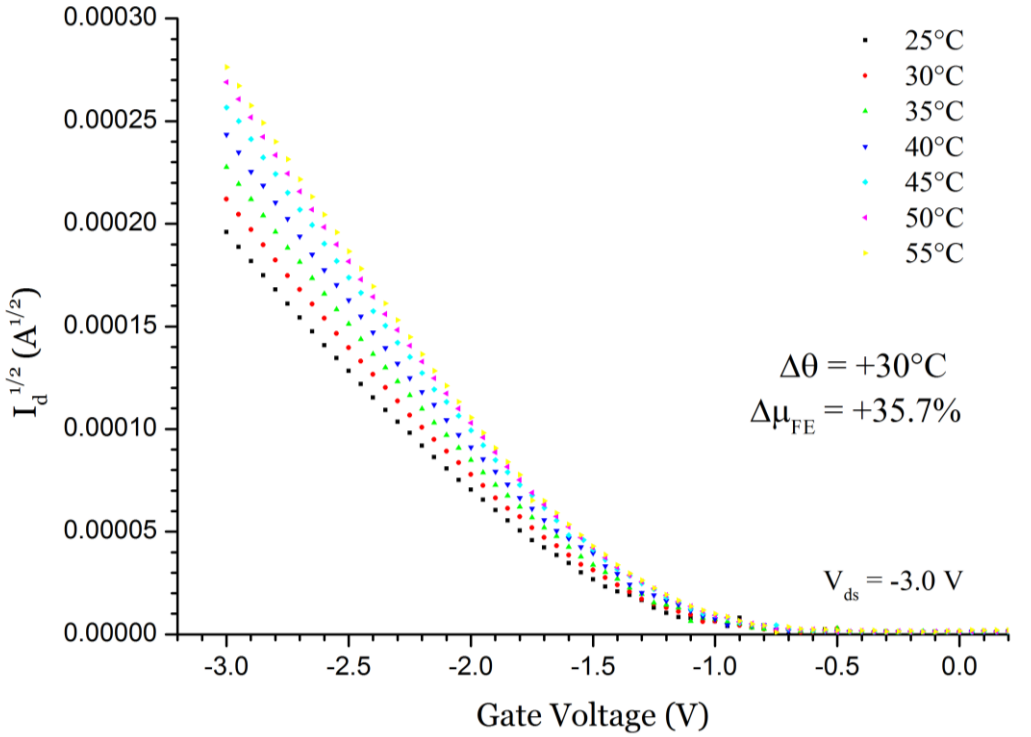

Figure 5-20 – Multiple plots of the square root of drain current versus gate voltage for a top-gold-contact pentacene OFET based on AlO_x-LDPE dielectric at various temperatures, ranging from 25 °C to 55 °C.

5.2.3. Polymer-gated devices

Polymer-gated pentacene devices have previously been demonstrated [115]; however, as of October 2013, there is no published report on pentacene OFETs gated exclusively with evaporated LDPE. Moreover, no p-type OFETs using this gate dielectric have been demonstrated, as the only demonstrated example of LDPE (only) OFET used an n-type semiconductor (C_{60}) [72].

Indeed, the early fabrication attempts of LDPE (only) pentacene OFETs suffered from severe gate leakage. This problem is likely to be related to the penetration of gold into the pentacene and LDPE layers during the deposition of the top source-drain electrodes [116]; it is worth mentioning that no similar problems were observed when silver was used instead of gold. Finally, the optimisation of the gold deposition rate yielded favourable results with low gate-leakage current.

Furthermore, despite the relatively low drain current, as compared to pentacene OFETs built on other dielectric combinations, as discussed above, the electrical characteristics of these devices gave valid indications of ambipolar behaviour, as discussed below.

5.2.3.1. *Preparation*

Pre-cut quartz substrates were used as substrates for these devices. The standard cleaning process was followed; the substrates were sonicated in an alkaline solution and in IPA and a final UV-ozone treatment was applied for 270 seconds. More details on substrate preparation are given in section 2.2.4.

Silver was thermally evaporated and deposited on the substrates through shadow masks for the growth of the patterned gate electrodes. The final thickness was 50 nm, the deposition rate varied from 0.025 to 0.063 nm/s and the pressure in the dome was kept below 5.5 x 10^{-7} Torr throughout the deposition process.

LDPE was evaporated and deposited on the entire surface of each sample. The final thickness of the deposited film was 400 nm, the deposition rate varied between 0.01 and 0.055 nm/s and the maximum pressure was 1.2 x 10^{-6} Torr. The substrates were not annealed after the LDPE deposition.

Pentacene was also evaporated without shadow masks. The thickness of film was 50 nm, the deposition rate varied from 0.03 to 0.078 nm/s and the pressure was limited under 4.2 x 10^{-7} Torr. The substrates were not additionally heated during the pentacene deposition.

Finally, gold was thermally evaporated through shadow masks. The resulting channel dimensions were 10 μm (length) by 2 mm (width). The final thickness of the electrodes was 50 nm. For the mitigation of gold penetration, the deposition rate was adjusted to be about an order-of-magnitude slower than the typical rate used for the most of the device batches presented in this work; it was limited to 0.0035 nm/s for the first 15 nm, and then it was gradually increased to a maximum of 0.009 nm/s until the desired thickness was achieved. The gold deposition process lasted more than 3 hours and then pressure was limited below 1.1 x 10^{-6} Torr throughout this period of time.

5.2.3.2. *Electrical characteristics*

All measurements were taken in ambient conditions, i.e. at room temperature and under usual room light conditions. The calculated characteristics of these all-polymer devices were inferior to those of all other pentacene devices based on different dielectrics. A threshold voltage of -3.2 V, a mobility of roughly 4×10^{-5} $cm^2V^{-1}s^{-1}$, in conjunction with the very low capacitance per unit area (C_i) of the 400-nm-thick LDPE dielectric, which was measured at ~5 nF/cm^2, as discussed in section 5.1, resulted in very low saturated drain current values. The measured drain current for $V_{ds} = V_{gs} = -30$ V was as low as 9 nA. One of the possible reasons for these low mobility value is the, otherwise intentional, limited gold penetration into the semiconductor, as previously reported by Cho *et al.* [116].

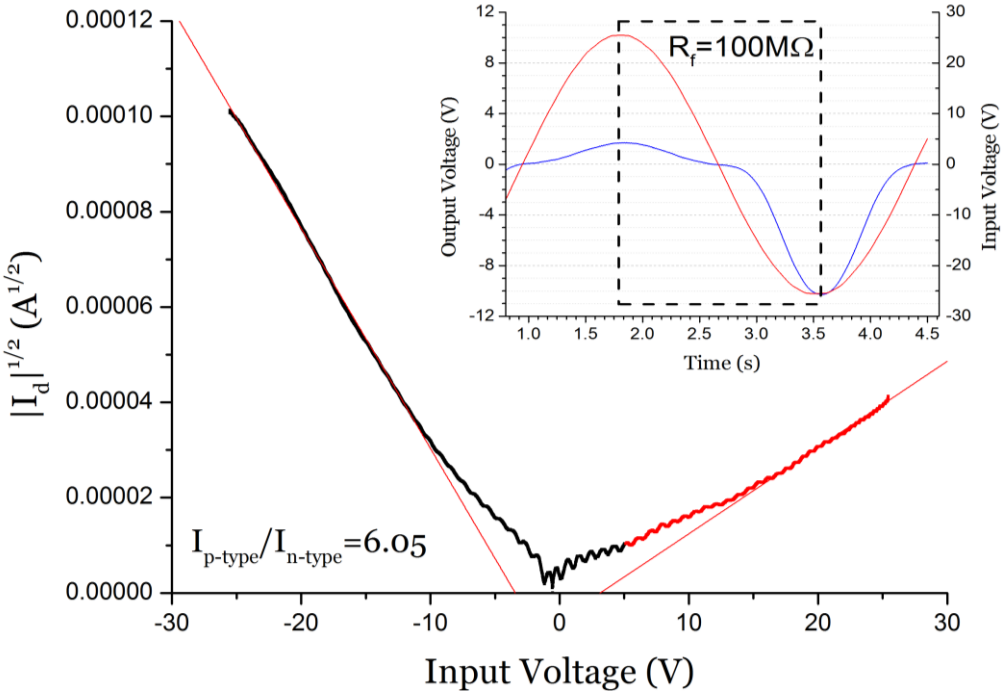

Figure 5-21 – Square root of the modulus of drain current versus input voltage ($V_{in}=V_{gs}=V_{ds}$) for a LDPE (only)-gated pentacene OFET with top gold contacts; converted transfer curve from the AC saturated measurement data enveloped by the dashed rectangle of the inset. Results show a quadratic dependence of drain current on input voltage for both negative and positive bias, which can constitute an indication of ambipolar behaviour.

Nevertheless, the measurements from the I-V converter system, discussed in Chapter 4, revealed a very interesting behaviour under positive bias. Figure 5-21 shows a converted data from the oscilloscope screenshot, shown in the inset, which are presented as the square root of the drain current versus input voltage plot. This graph clearly shows a quadratic dependence of the drain current on the input bias; this dependence can be seen on both negative (p-type) and negative (n-type) directions. These results indicate an ambipolar behaviour of a material which is widely reported as a hole-transporting semiconductor. Ambipolar behaviour of well-known p-type semiconductors has been previously achieved with the application of an appropriate surface treatment on the gate insulator [39]; in particular, OFETs with pentacene deposited on Ta_2O_5 treated with *poly(vinyl alcohol)*, known as *PVA*, have been reported to yield some unconventional n-type output characteristics [117]. In that paper, the ambipolar behaviour and the gate-bias-effects were found to be dependent on factors such as the thickness of the deposited PVA layer, its impurity (Na^+) content and the annealing process; in

some occasions, under n-type operation, increasing gate voltage resulted in a decrease in drain current. Similarly, in the output characteristics shown in Figure 5-22 and Figure 5-23, although the gating-effects in the p-type regime appear common, the n-type characteristics show an inverse dependence on gate bias, with drain current decreasing with increasing gate voltage.

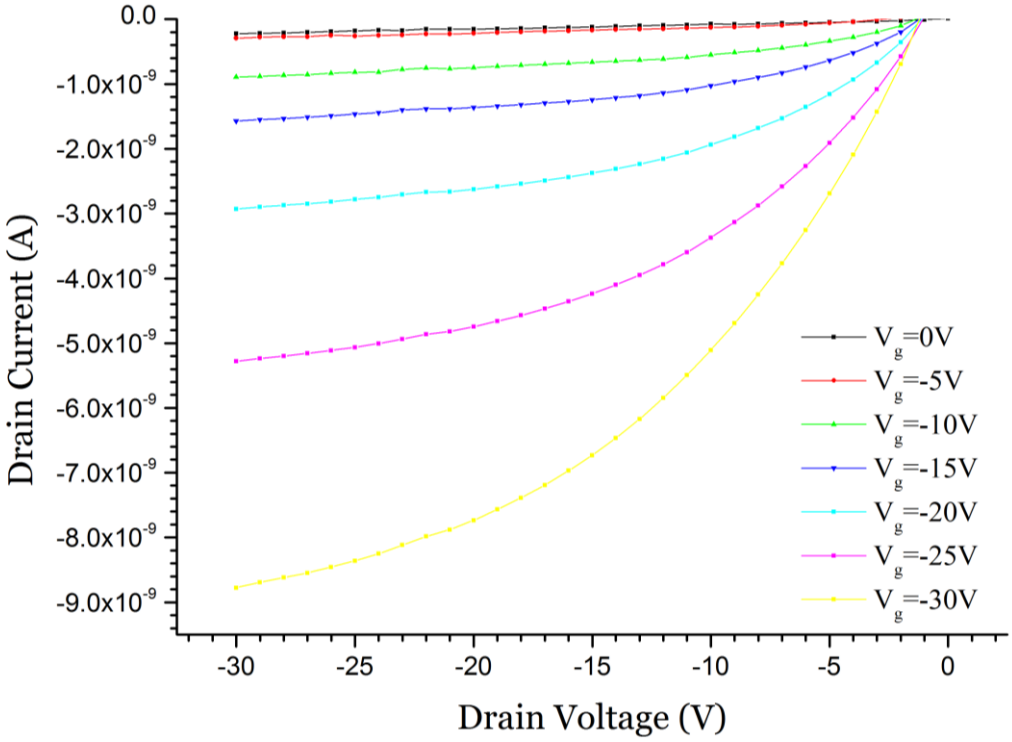

Figure 5-22 – Output characteristics for negative bias (p-type bevaviour) of a LDPE (only)-gated pentacene OFET with top gold contacts.

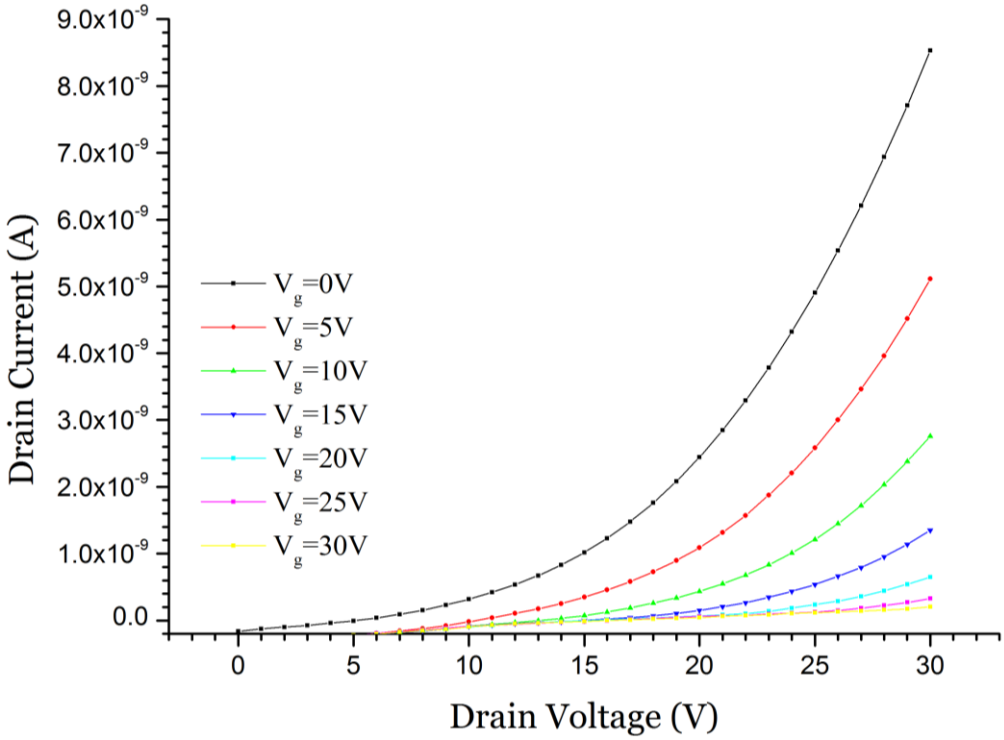

Figure 5-23 – Output characteristics for positive bias (n-type bevaviour) of a LDPE (only)-gated pentacene OFET with top gold contacts. Drain current decreased with increasing gate bias.

5.2.4. Flexible devices

One of the most promising assets of OSCs is their exploitation in the development of flexible electronics on plastic substrates. Flexible pentacene OFETs based on various dielectrics have previously been demonstrated; as early as 2004, Majewski *et al.* demonstrated the development of pentacene OFETs on *Mylar* substrates coated with a *sputtered aluminium* layer which was anodised for the formation of a few-nm-thick aluminium oxide gate insulator [65]. More recently, Graz *et al.* reported on the fabrication of pentacene OFETs and inverters built on *poly(dimethylsiloxane) (PDMS)* substrates employing *parylene C* as their gate dielectric [118].

In this section, the fabrication methodology and the electrical characterisation results from pentacene OFETs built on common plastic substrates are discussed. The substrates were commercially available laser printer transparencies, as discussed in section 2.2.3, the gate electrodes were made of evaporated aluminium and the dielectric was aluminium oxide formed by anodisation of the aluminium electrodes; the dielectric was treated with a layer of evaporated LDPE. This combination of dielectrics has only been demonstrated for pentacene OFETs built on rigid substrates [72].

5.2.4.1. *Preparation*

The substrates were sourced from a common A4-sized laser printer transparency. As discussed in section 2.2.3, while the exact composition of the employed substrate is unknown, it is well-known that the laser printer transparencies are designed to tolerate the high temperatures of the printing process, while most of them bear a special coating on their top side which enhances the adhesion of the toner on the plastic surface [119, 120]; this coating apparently improved the adhesion of the evaporated aluminium films as no delamination problems were experienced during anodisation.

The substrates were cleaned with an alkaline solution and sonicated at 70 °C. No IPA cleaning and no UV-ozone treatment were applied in order to prevent any damage on the coated surface.

An 100-nm-thick aluminium layer was deposited by thermal evaporation through shadow masks in high vacuum. The pressure within the evaporator dome was 7.4 x 10^{-7} Torr in the beginning of the deposition process and reached a maximum of 3.7 x 10^{-6} Torr during the evaporation. The deposition rate was adjusted at roughly 10^{-3} nm/s for the first 10 nm and it was then gradually increased up to 9.0 x 10^{-1} nm/s.

The aluminium films were anodised in a 1 mM citric acid solution. The applied current was set at 0.95 mA and the maximum voltage at 5 V. The current application time was 75 seconds. The devices were rinsed with DI water and dried before further process. Detailed information on aluminium anodisation can be found in section 2.4.2.

A 20-nm-thick film of LDPE was deposited on the substrates after the aluminium anodisation process. No shadow masks was used so the deposited LDPE layer spread over the entire surface of the substrates. The starting pressure was 4.8 x 10^{-7} Torr, whereas the maximum pressure during evaporation was 9.9 x 10^{-7} Torr. The deposition rate was being varied between 0.015 and 0.07 nm/s throughout the entire process. These substrates were later annealed at ~100 °C in vacuum for 30 minutes. The LDPE-treatment of oxides is discussed in section 2.4.5.

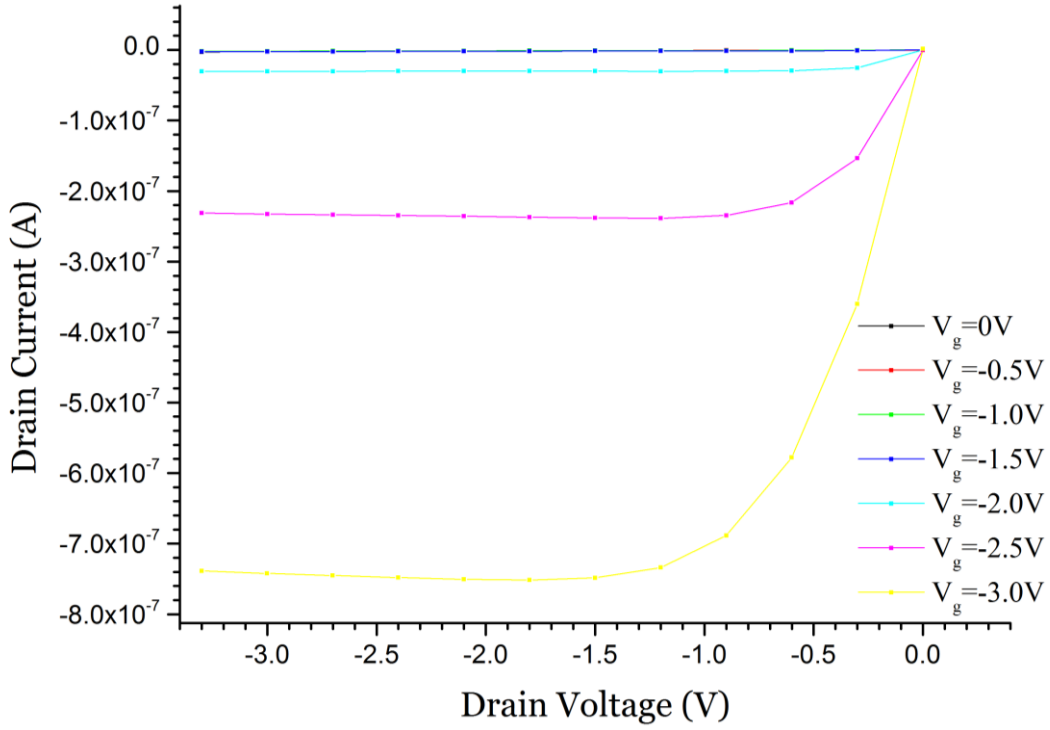

Figure 5-24 – Output characteristics of a flexible top-gold-contact pentacene OFET based on AlO_x-LDPE dielectric.

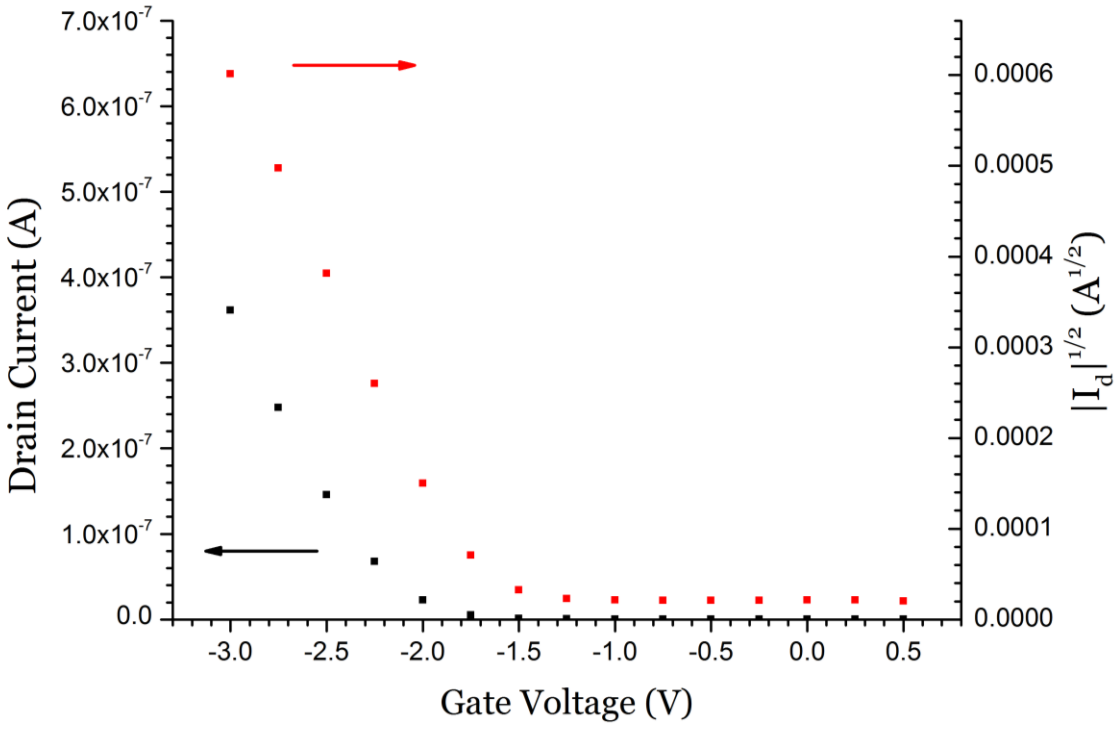

Figure 5-25– Transfer characteristics of a flexible top-gold-contact pentacene OFET based on AlO_x-LDPE dielectric.

Pentacene was thermally evaporated so that a 50-nm-thick was deposited on the entire surface of all substrates. The deposition rate varied from 0.02 to 0.04 nm/s. The pressure inside the dome was roughly 4.0 x 10^{-7} Torr. The substrates were not further heated during the thin-film deposition.

Gold was finally deposited by thermal evaporation though shadow masks. Each substrate was fitted with one mask which patterns four source-drain pairs on the surface of the substrate; the dimensions of the resulting OFET channels are 10 μm (length) x 2 mm (width). The deposition rate varied from 0.05 to 0.08 nm/s while the pressure was kept below 2.0 x 10^{-6} Torr. The final thickness of the top electrodes was 50 nm.

5.2.4.2. *Electrical characteristics*

All measurements were taken in ambient conditions, i.e. at room temperature and under usual room light conditions. The output and transfer electrical characteristics of one of these devices are shown in Figure 5-24 and Figure 5-25, respectively. The threshold voltage of this devices is comparable to its AlO_x-LDPE counterpart, discussed in section 5.2.2.2, which was built on rigid silicon substrate; the V_{th} of the flexible device was calculated to be -1.7 V, whereas the rigid sample gave a value of -1.3 V. Contrarily, the mobility was found to be interestingly higher; the value for the flexible device was ~2.1 x 10^{-2} $cm^2V^{-1}s^{-1}$, whereas the rigid device exhibited a much lower value of ~3.1 x 10^{-3} $cm^2V^{-1}s^{-1}$.

There can be multiple reasons for the much higher mobility value on the plastic substrate. As discussed in section 5.2.2.2, AFM images from the Al and AlO_x surfaces on silicon revealed a high roughness profile which can result in a low mobility of charge carriers; it is possible that the coating of the plastic substrates provides a smoother deposition of aluminium on the plastic substrate. However, there are no comparative AFM images to back this assumption. Another reason can be the somewhat higher gold deposition rate in the case of the flexible devices, which can result in higher mobility according to Cho *et al.* [116].

5.2.5. Comparison and conclusions on pentacene OFETs

Pentacene is a thoroughly studied organic semiconductor and the abundance of published examples of its exploitation in the field of OFETs does not allow for groundbreaking innovations. However, the results from some novel approaches to pentacene OFET fabrication are presented in this section. These examples include the development of pentacene OFETs on common, commercially available, flexible plastic substrates using a combination of AlO_x and LDPE dielectrics which use has only been demonstrated on rigid substrates. Moreover, the fabrication of top-gold-contact pentacene OFETs, exclusively gated by an evaporated LDPE layer, is presented here; as of October 2013, there are no published examples of any p-type semiconductor employed in OFETs based exclusively on an LDPE dielectric layer.

Comparative results from all fabricated OFET architectures are given in Table 5-I. The best charge carrier mobility performance was measured on a SiO_2-gated device with OTS-treated surfaces; the calculated value was roughly 0.1 $cm^2V^{-1}s^{-1}$ with a threshold voltage as low as -1.4V. The SiO_2-LDPE device had a μ value of 5.7 x 10^{-2} $cm^2V^{-1}s^{-1}$ and a V_{th} of -2.4 V. Both SiO_2-gated devices showed poor drain current saturation as revealed by their output characteristics.

Next, the AlO_x-gated devices had slightly lower V_{th} values, but their mobility values were significantly lower than those of the SiO_2-gated devices. The AlO_x-OTS device had a V_{th} of -1.0 V and a μ of 7.0 x 10^{-4} $cm^2V^{-1}s^{-1}$, the AlO_x-LDPE device on a silicon substrate had a V_{th} of -1.4 V and a μ of 3.1 x 10^{-3} $cm^2V^{-1}s^{-1}$ and the AlO_x-LDPE device on a plastic substrate had a V_{th} of -1.7 V and a μ of 2.1 x 10^{-2} $cm^2V^{-1}s^{-1}$. Additional comparative studies on the film morphology, the

environmental stability and the temperature dependence of OFETs built differently treated AlO_x surfaces are discussed in this section. Furthermore, the importance of the surface treatment for the light stability of the fabricated OFETs is highlighted in an extensive comparative study given in section 6.3.

Last, the pentacene OFET gated exclusively by a 400-nm-thick LDPE layer showed inferior electrical characteristics with a V_{th} of -3.2 V and a μ of roughly 4.0 x 10^{-5} $cm^2V^{-1}s^{-1}$. However, the measurements with the I-V converter system, described in Chapter 4, revealed an interesting ambipolar behaviour of this device, as drain current was found to have a quadratic dependence on drive voltage, for both positive and negative polarities.

Table 5-I – Comparison of all fabricated pentacene OFET architectures. The cells highlighted in green colour indicate material combinations that have not been reported in the international literature, as of October 2013.

OSC	Substrate	Dielectric	Treatment	Top-contact material	C_i (nF/cm^2)	V_{th} (V)	μ ($cm^2V^{-1}s^{-1}$)	Comments
Pentacene	**Si/SiO_2**	**SiO_2**	OTS	Au	27	-1.4	0.10537	Poor saturation
			LDPE		27	-2.4	0.05671	
		AlO_x	OTS		480	-1.0	0.00070	
			LDPE		98	-1.4	0.00315	
		LDPE			5	-3.2	0.00004	
	Plastic	**AlO_x**	LDPE		98	-1.7	0.02119	Ambipolar behaviour

5.3. PDI8-CN2 OFETs

N,N'-bis(n-octyl)-x:y, dicyanoperylene-3,4:9,10-bis(dicarboximide), known as PDI8-CN_2, is an n-type semiconductor. There are few published examples of PDI8-CN_2 used as an active material in OFETs. In 2011, Hague *et al.* demonstrated an AlO_x-gated PDI8-CN_2 OFET used as an amine vapour sensor [114]. About a year later, Liscio *et al.* published a detailed study on SiO_2-gated PDI8-CN_2 OFETs [121].

A description of the fabrication methodology and the results from the electrical characterisation of these OFETs is given in this section. Similarly to the study of pentacene devices, discussed in section 5.2, the PDI8-CN_2 OFETs are categorised with respect to their main dielectric; moreover, a separate section is dedicated to devices built on flexible substrates.

5.3.1. Silicon-dioxide-gate devices

A comparison of two different surface treatment of SiO_2 is given in this section; the SiO_2 surfaces were treated with either OTS or LDPE before PDI8-CN_2 deposition. The device fabrication and the measurement results are discussed below.

5.3.1.1. *Preparation*

Arsenic-doped silicon substrates with a 100-nm-thick thermal oxide were used. The substrates were initially cleaned by sonication in an alkaline solution and in IPA and UV-ozone treatment. A detailed description on substrate preparation is given in section 2.2.4.

For the OTS-treatment, the cleaned substrates were immersed into a cyclohexane solution of OTS (10 mg/mL) for 60 minutes. This process was carried out in a nitrogen glove box.

For the LDPE-treatment, a 20-nm-thick film of LDPE was deposited with thermal evaporation; the deposition rate varied between 0.007 and 0.01 nm/s and the pressure within the dome of the evaporator was roughly 8.0 x 10^{-7} Torr. The substrates were annealed at 105 °C in vacuum for 30 minutes.

PDI8-CN_2 was thermally evaporated and deposited onto both substrate sets. The final film thickness was 50 nm, the deposition rate varied from 0.03 to 0.05 nm/s, while the pressure was kept below 8.0 x 10^{-7} Torr.

Finally, gold was deposited through shadow masks using thermal evaporation. The final thickness of the patterned top electrodes was 50 nm and the dimensions of the channels were 10 µm (length) by 2 mm (width). The deposition rate varied from 0.015 to 0.035 nm/s, while the pressure was limited below 2.3 x 10^{-6} Torr throughout the evaporation process.

5.3.1.2. *Electrical characteristics*

All measurements were taken in ambient conditions, i.e. at room temperature and under usual room light conditions. Similarly, the output characteristics of the SiO_2-gated PDI8-CN_2 OFETs with OTS-treated and LDPE-treated surfaces are shown in Figure 5-26 and Figure 5-27, respectively. Regardless of the choice of dielectric treatment, all tested devices showed a normally-on behaviour; similar characteristics can be seen in the plots shown in the work of Liscio *et al.* [121]; nevertheless, this observation is not explicitly discussed in this paper.

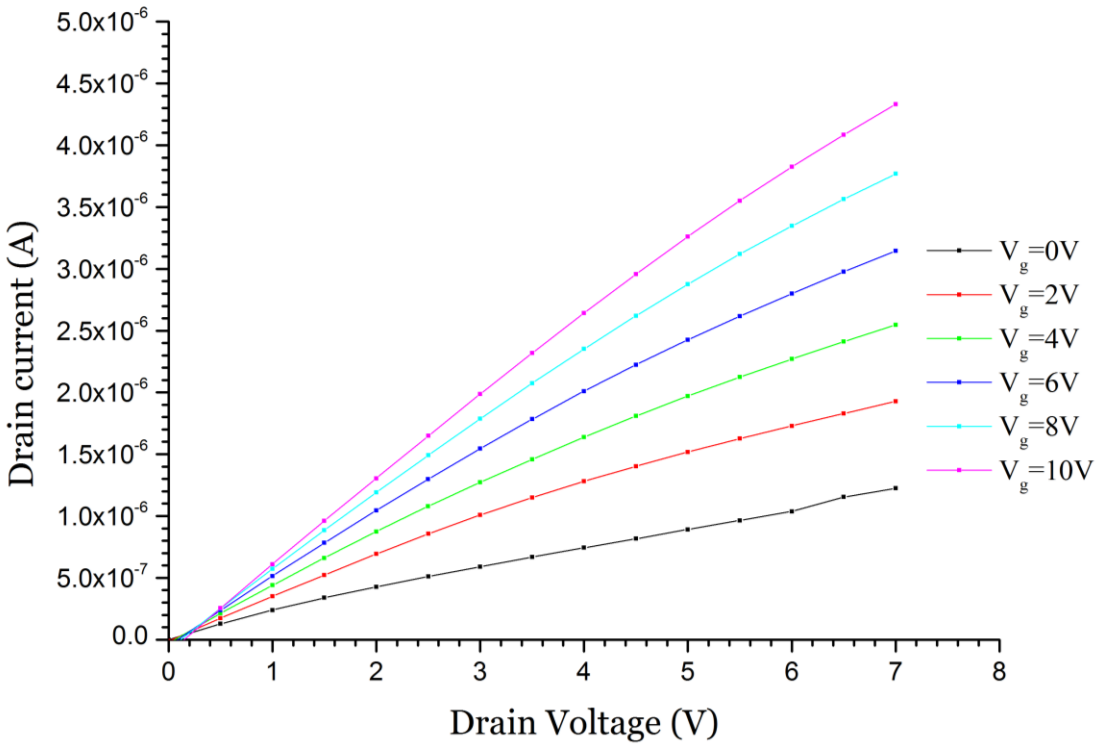

Figure 5-26 – Output characteristics of a top-gold-contact PDI8-CN_2 OFET based on SiO_2-OTS dielectric.

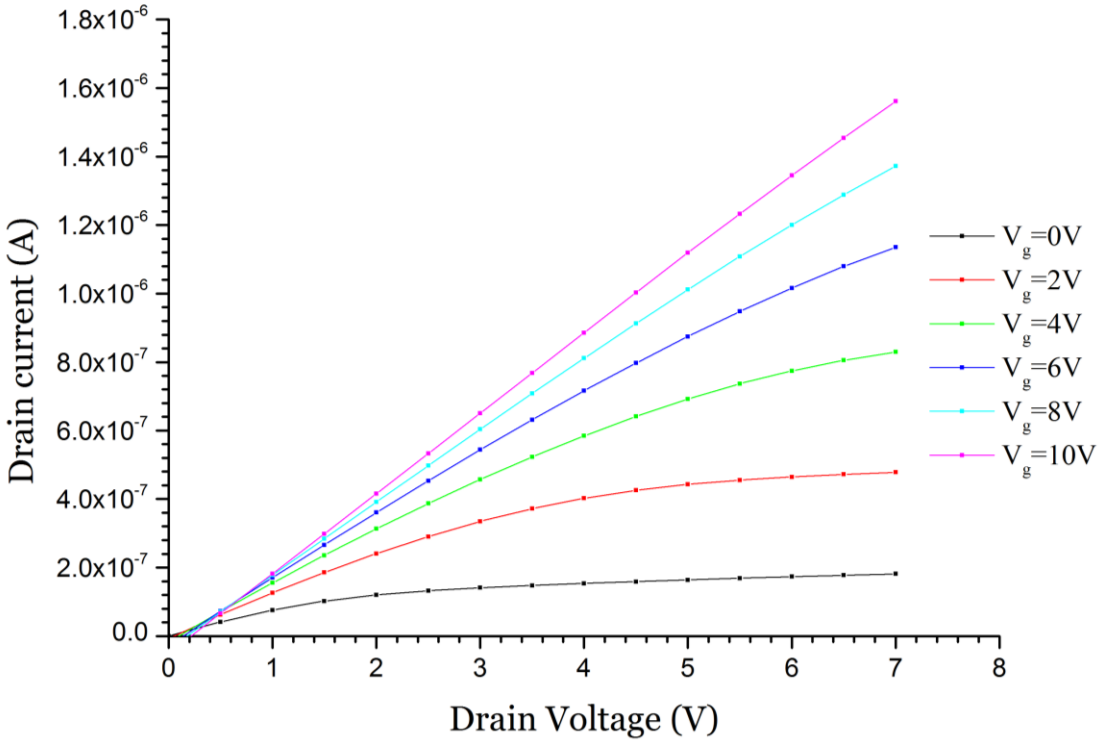

Figure 5-27 – Output characteristics of a top-gold-contact PDI8-CN_2 OFET based on SiO_2-LDPE dielectric.

Figure 5-26 and Figure 5-27 show the output characteristics of the SiO_2-OTS and the SiO_2-LDPE devices, respectively. The SiO_2-OTS device exhibited pronounced doping effects, which are remarkably highlighted by the almost linear dependence of drain current of drain voltage at zero gate voltage. The LDPE-treated device was not found to be significantly doped; however,

the negative V_{th} (normally-on) results in poor saturation at high gate voltages; this is anticipated as the saturated region condition, i.e. $V_{DS} > V_{GS} - V_{th}$, does not hold true at high V_{GS}.

Figure 5-28 gives a comparison of transfer characteristics of the devices built on differently treated oxides, expressed as the root of drain currents versus gate voltage.

The threshold voltages were calculated at -5.8 V and -2.4 V for the SiO_2-OTS and the SiO_2-LDPE devices, respectively, confirming the observed normally-on behaviour. Similarly to the SiO_2-gated pentacene a device, the mobility of the OTS-treated PDI8-CN_2 OFETs was found to be roughly double than that of the LDPE-treated ones; the respective values of mobility were 0.01379 and 0.00755 $cm^2V^{-1}s^{-1}$.

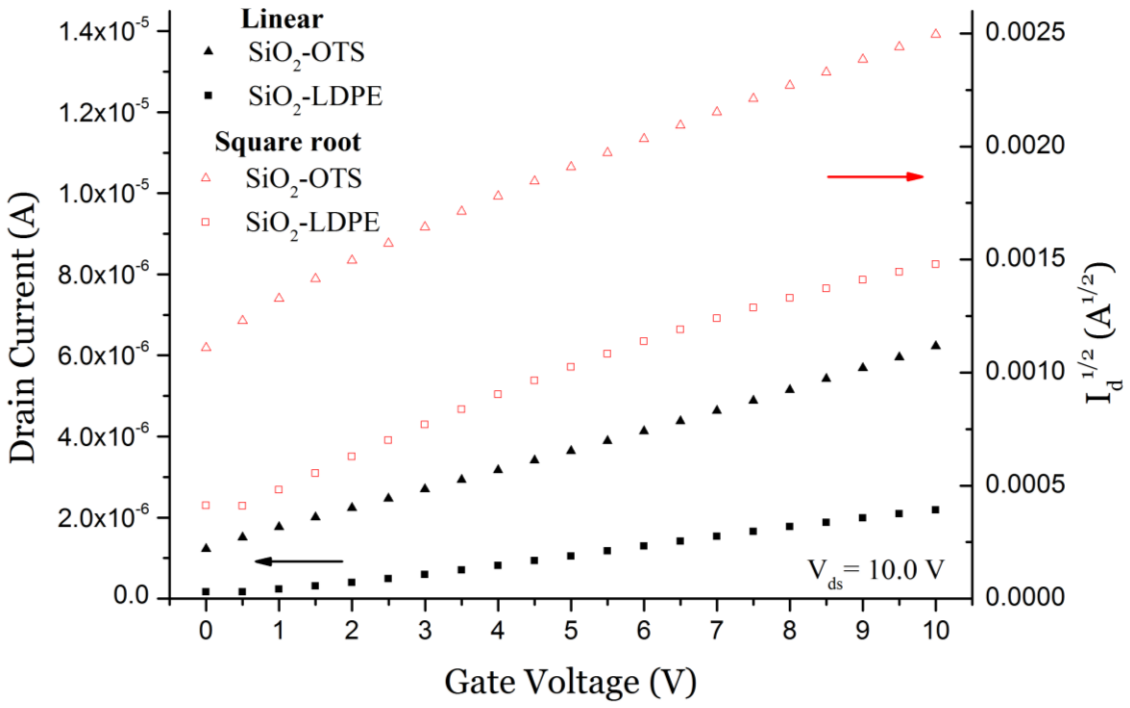

Figure 5-28 – Transfer characteristics of a PDI8-CN_2 OFET with SiO_2-OTS dielectric (triangles) and a PDI8-CN_2 OFET with SiO_2-LDPE dielectric (squares).

5.3.2. Aluminium-oxide-gate devices

PDI8-CN_2 OFETs built on AlO_x dielectric with OTS treatment have been demonstrated by Hague *et al.* [114]. In this section, a comparison between OFETs based on AlO_x dielectrics treated with either OTS or the novel evaporated LDPE approach is given. The details on device fabrication and the results from their electrical characterisation are given below.

5.3.2.1. *Preparation*

Silicon substrates with a 100-nm-thick thermal oxide layer were used. They were cleaned by sonication in an alkaline solution and IPA and undergone UV-ozone treatment. A detailed description on substrate preparation is given in section 2.2.4.

An 100-nm-thick aluminium layer was deposited by thermal evaporation through shadow masks in high vacuum. The pressure within the evaporator dome was 6.1 x 10^{-7} Torr in the beginning of the deposition process and reached a maximum of 2.5 x 10^{-6} Torr during the evaporation. The deposition rate was adjusted at roughly 0.002 nm/s for the first 10 nm and it was then gradually increased up to 0.5 nm/s.

The aluminium films were anodised in a 1 mM citric acid solution. The applied current was set at 0.95 mA and the maximum voltage at 5 V. The current application time was 75 seconds. The devices were rinsed with DI water and dried before further process. Detailed information on aluminium anodisation can be found in section 2.4.2.

For the AlO_x-OTS devices, the substrates were immersed into a 10 mg/mL cyclohexane solution of OTS for 10 minutes. This process was carried out in a nitrogen glove box. Further details on OTS treatment are given in section 2.4.3.

For the AlO_x-LDPE devices, a 20-nm-thick film of LDPE was deposited on the substrates after the aluminium anodisation process. No shadow masks were used; LDPE covered the entire surface of the substrates. The starting pressure was 6.3 x 10^{-7} Torr, whereas the maximum pressure during evaporation was 9.5 x 10^{-7} Torr. The deposition rate was being varied between 0.065 and 0.08 nm/s throughout the entire process. These substrates were later annealed at 105 °C in vacuum for 30 minutes. The LDPE-treatment of oxides is discussed in section 2.4.5.

A 50-nm-thick film of PDI8-CN_2 was deposited on the entire surface of all substrates by thermal evaporation. The deposition rate was varied from 0.03 to 0.05 nm/s. The pressure was kept below 8.0 x 10^{-7} Torr throughout the evaporation process. The substrates were not further heated during the semiconductor deposition.

Gold was finally deposited by thermal evaporation though shadow masks. The dimensions of the resulting OFET channels are 10 µm (length) x 2 mm (width). The final thickness of the deposited electrodes was 50 nm. The deposition rate varied from 0.015 to 0.035 nm/s. The pressure was kept below 3.3 x 10^{-6} Torr.

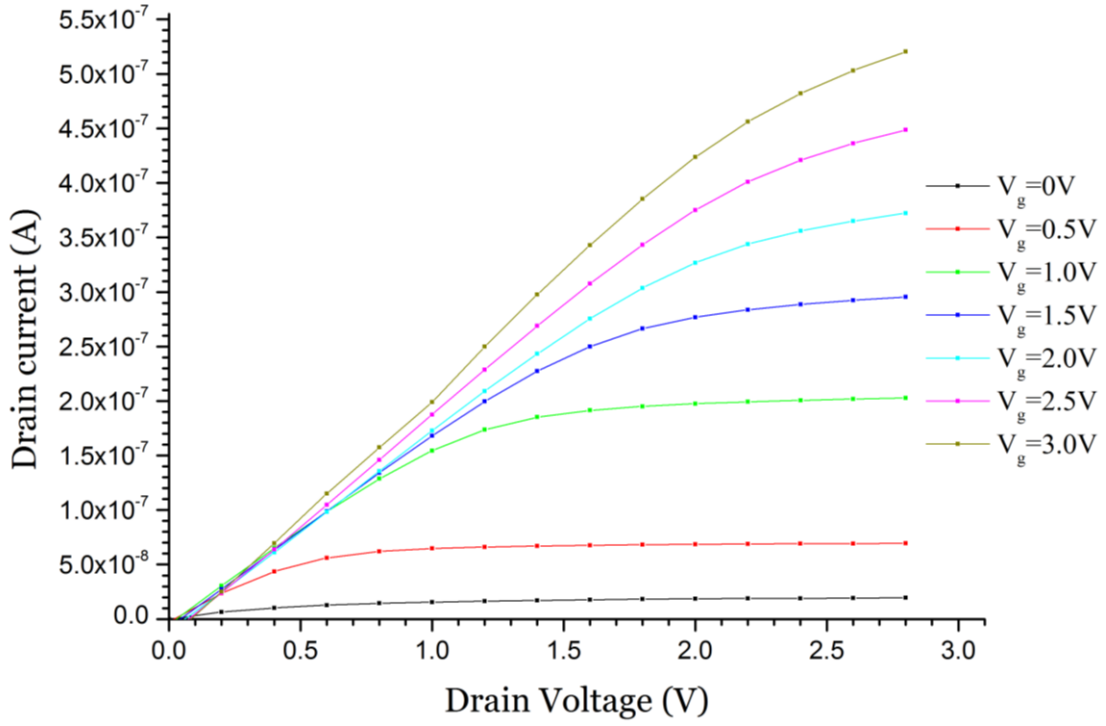

Figure 5-29 – Output characteristics of a top-gold-contact PDI8-CN_2 OFET based on AlO_x-OTS dielectric.

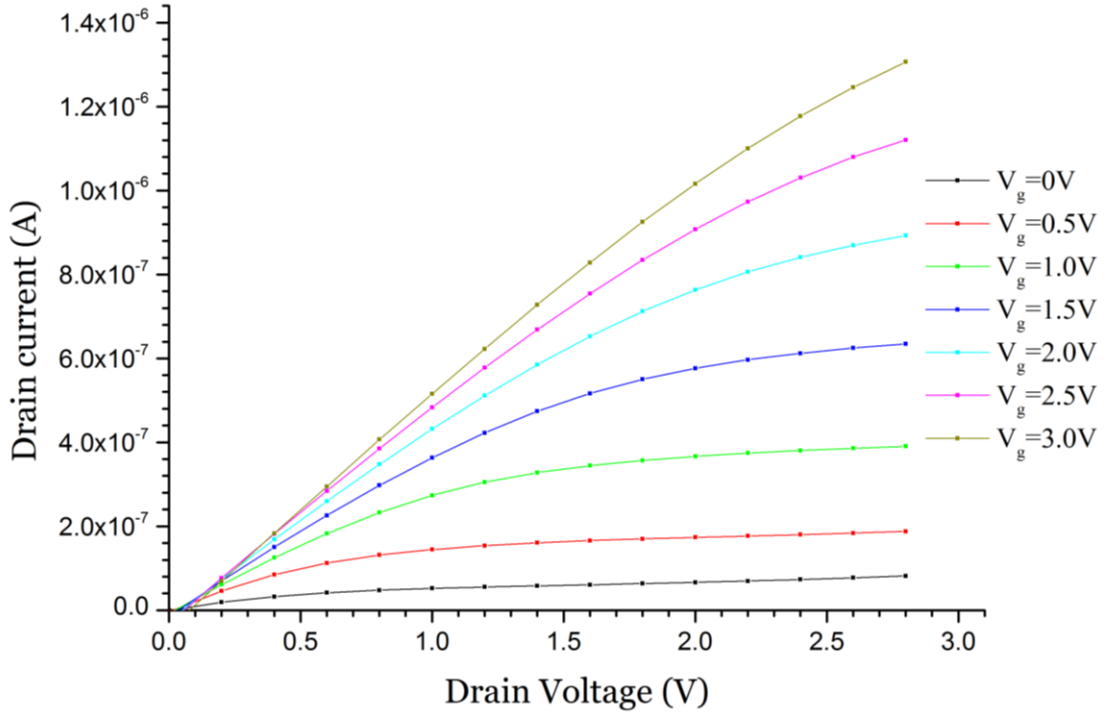

Figure 5-30 – Output characteristics of a top-gold-contact PDI8-CN_2 OFET based on AlO_x-LDPE dielectric.

5.3.2.2. *Electrical characteristics*

All measurements were taken in ambient conditions, i.e. at room temperature and under usual room light conditions. The similarly to the SiO_2-gated PDI8-CN_2 OFETs, both AlO_x-gated devices were also found to have a normally-on behaviour. Figure 5-29 and Figure 5-30 show the output characteristics of the AlO_x-OTS and AlO_x-LDPE devices, respectively. Also, both devices show negligible doping effects; this comes in contrast to the pronounced doping of the SiO_2-OTS device, discussed in section 5.3.1.2.

Figure 5-31 gives a comparison of the transfer characteristics of these devices, expressed as the root of drain currents versus gate voltage. The calculated threshold voltage value of the OTS-treated device was exactly zero volts, whereas the value for the LDPE-treated one was -0.4 V. Similarly to the pentacene devices discussed in section 5.2, the mobility values of PDI8-CN_2 OFETs built on AlO_x dielectrics were found to be lower than those on SiO_2. However, both AlO_x surface treatments yielded comparable results; the AlO_x-OTS device was found to have a mobility of ~2.0 x 10^{-3} $cm^2V^{-1}s^{-1}$, while the mobility of the AlO_x-LDPE device about an order-of-magnitude higher, having a value of ~1.5 x 10^{-2} $cm^2V^{-1}s^{-1}$.

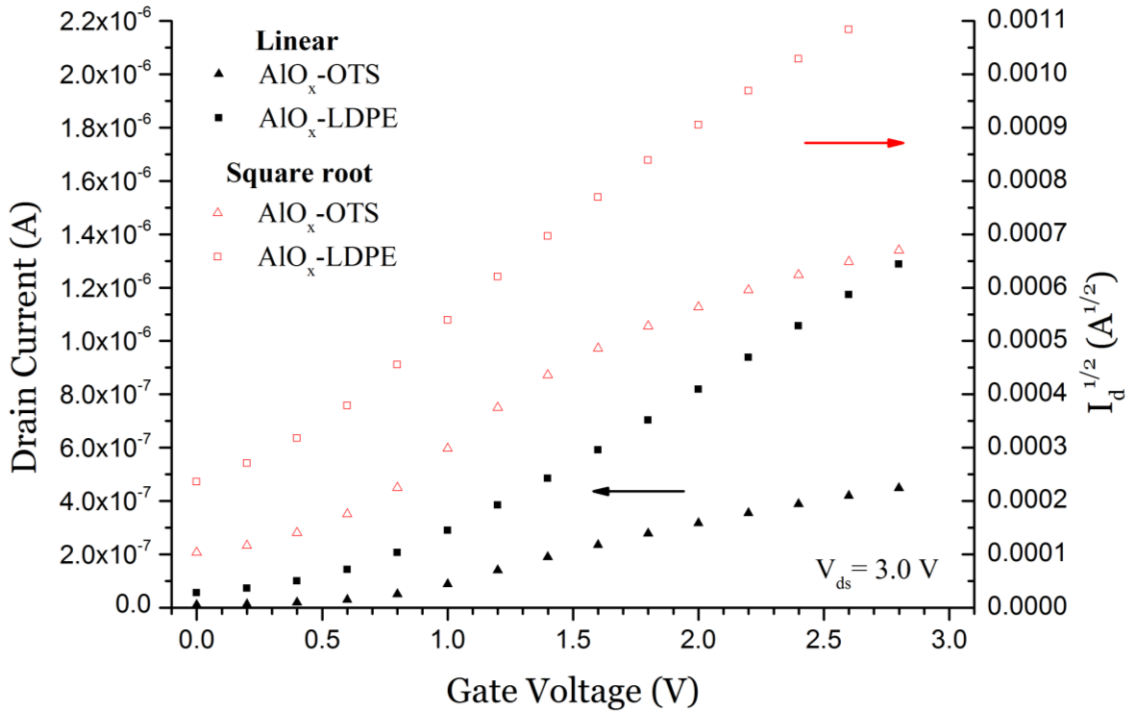

Figure 5-31 – Transfer characteristics of a PDI8-CN_2 OFET with AlO_x-OTS dielectric (triangles) and a PDI8-CN_2 OFET with AlO_x-LDPE dielectric (squares).

5.3.3. Polymer-gated devices

As of October 2013, there are no published examples of PDI8-CN_2 OFETs based on polymer dielectrics. In this section, the fabrication methodology and the electrical characteristics of such OFETs, employing an evaporated LDPE layer as their gate dielectric and silver as their top electrode material, are discussed.

5.3.3.1. *Preparation*

Silicon samples with a 100-nm thermal oxide layer served as the substrates of these devices. The standard cleaning process was followed; the substrates were sonicated in an alkaline solution and in IPA and a final UV-ozone treatment was applied for 270 seconds. More details on substrate preparation are given in section 2.2.4.

Silver was thermally evaporated and deposited on the substrates through shadow masks for the growth of the patterned gate electrodes. The final thickness was 60 nm, the deposition rate varied from 0.05 to 0.08 nm/s and the pressure in the dome was kept below 6.2 x 10^{-7} Torr throughout the deposition process.

LDPE was evaporated and deposited on the entire surface of each sample. The final thickness of the deposited film was 400 nm, the deposition rate varied between 0.01 and 0.13 nm/s and the maximum pressure was 2.2 x 10^{-6} Torr. The substrates were split into two groups; the substrates of one of them were annealed at 100 °C for 20 minutes in a nitrogen glove box, whereas the rest were not annealed before the semiconductor deposition. Figure 5-32 and Figure 5-33 show the optical microscope images of the surfaces of two complete OFETs with a not-annealed and an annealed LDPE dielectric, respectively.

PDI8-CN_2 was also evaporated without shadow masks. The final thickness of deposited films was 50 nm, the deposition rate varied from 0.01 to 0.07 nm/s and the pressure was kept below 4.4 x 10^{-7} Torr. None of the substrates was additionally heated during the pentacene deposition.

Finally, silver was thermally evaporated through shadow masks. The resulting channel dimensions were 10 μm (length) by 2 mm (width). The final thickness of the electrodes was 100 nm. The deposition rate varied from 0.003 to 0.24 nm/s and the pressure reached a maximum of 5.2 x 10^{-7} Torr.

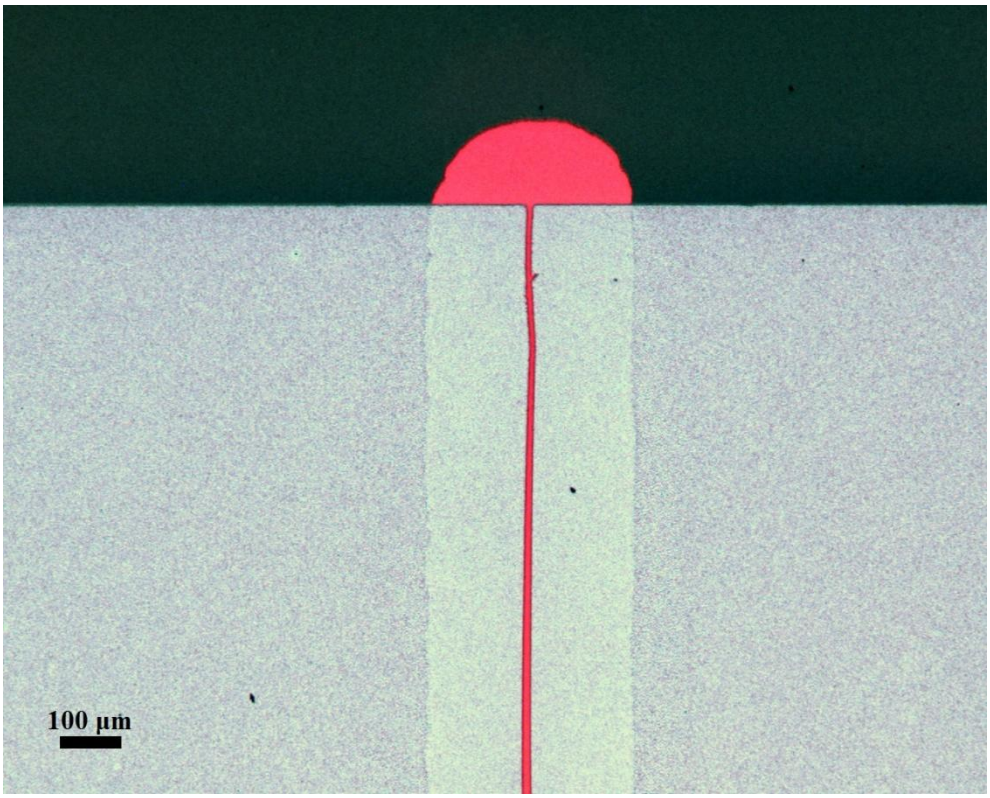

Figure 5-32 – An optical microscope picture from the channel area of a not-annealed PDI8-CN_2 OFET with top Ag contacts. The 10-µm-long channel can be seen as a vertical red line, aligned in the middle of the underlying gate.

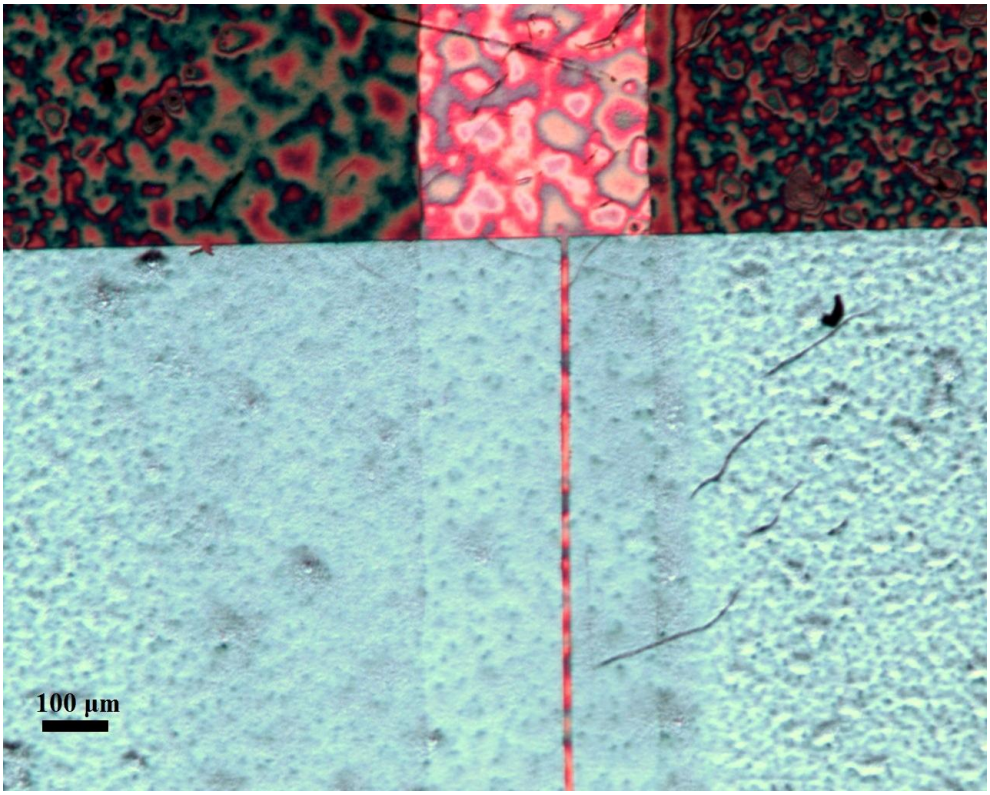

Figure 5-33 – An optical microscope image of the channel area of an annealed PDI8-CN_2 OFET with top Ag contacts. The bright pink area on the top, which extends under the silver electrodes, is the underlying gate electrode. The 10-µm-long channel is clearly shown in the middle.

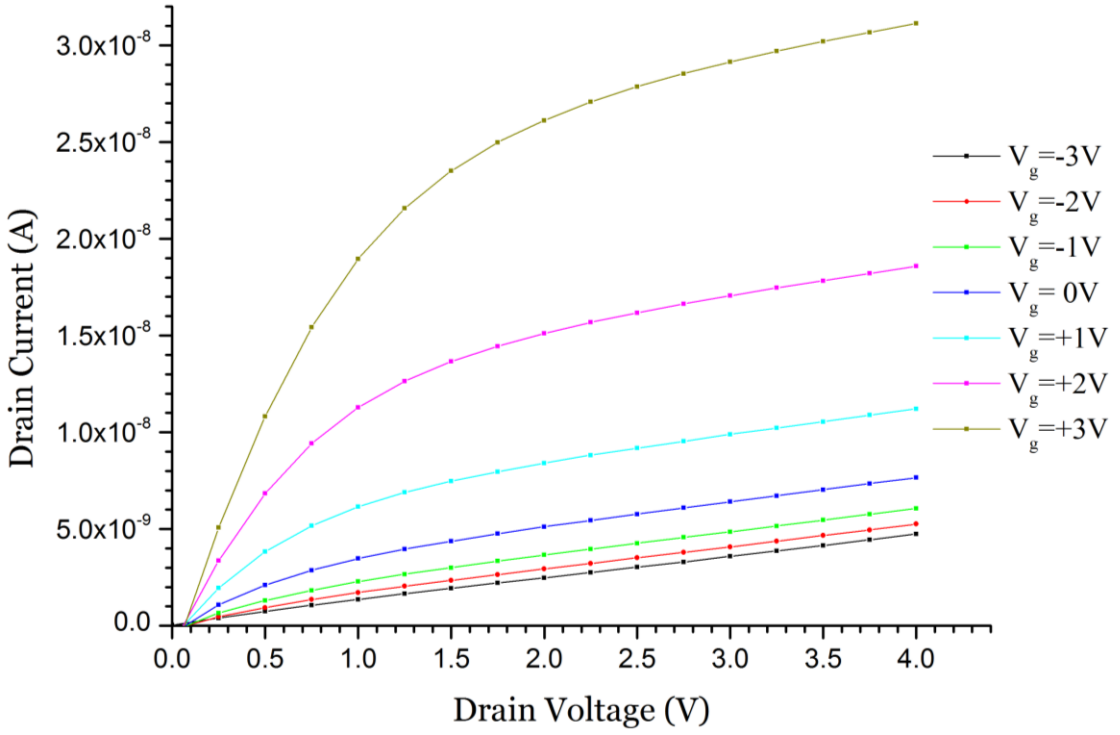

Figure 5-34 – Output characteristics of a not-annealed top-Ag-contact PDI8-CN_2 OFET based on LDPE (only) dielectric.

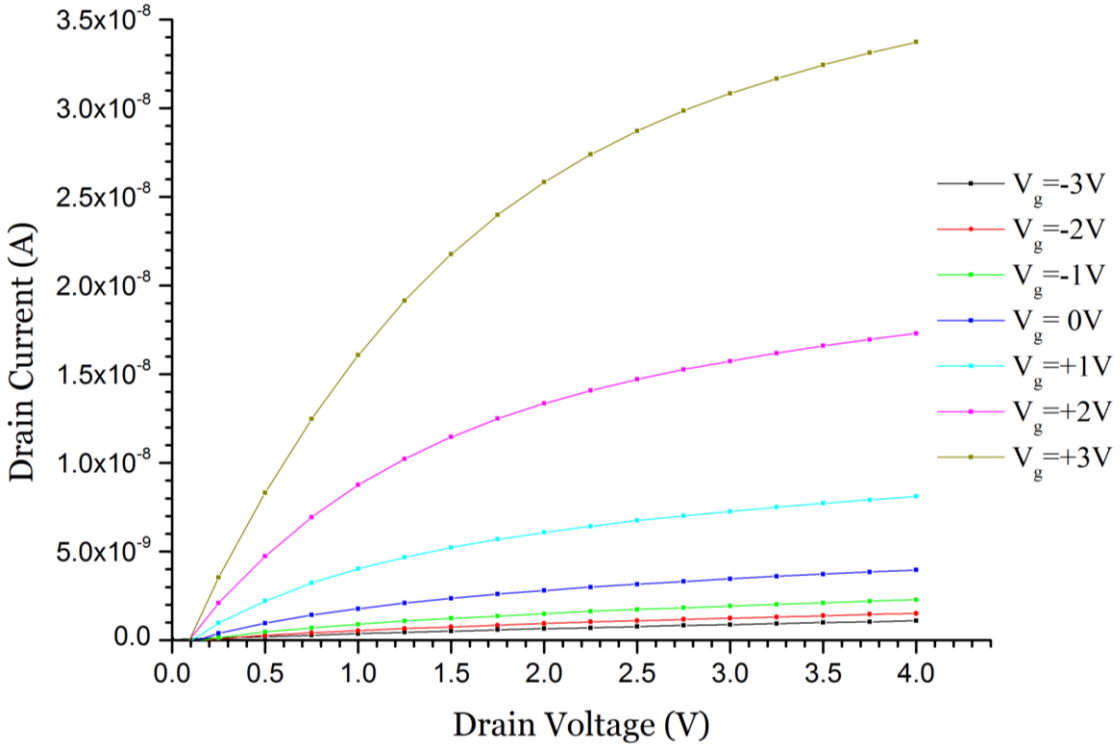

Figure 5-35 – Output characteristics of an annealed top-Ag-contact PDI8-CN_2 OFET based on LDPE (only) dielectric.

5.3.3.2. *Electrical characteristics*

All measurements were taken in ambient conditions, i.e. at room temperature and under usual room light conditions. Figure 5-34 and Figure 5-35 show the output characteristics of the devices with not-annealed and annealed LDPE dielectrics, respectively. Figure 5-36 gives a comparison of the transfer characteristics of the two devices, expressed as the square root of drain currents versus gate voltage.

The dielectric layer annealing was found to significantly affect the off-current and the threshold voltage of the tested devices. Threshold voltages were calculated at -1.7 V and -0.9 V for the devices built on not-annealed and annealed LDPE dielectric, respectively. As it can be seen in Figure 5-36, annealing induced a downward shift in the transfer characteristics, which clearly indicates a reduction in the ohmic (doping) contribution to the drain current.

Contrarily, despite the apparent changes in the grain formation, as revealed by the microscope images in Figure 5-32 and Figure 5-33 and as suggested by Kanbur *et al.* [72], the effect of dielectric annealing on mobility was found to be negligible, as the calculated values for the not-annealed and the annealed devices were 9.5 x 10^{-4} and ~1.0 x 10^{-3} $cm^2V^{-1}s^{-1}$, respectively.

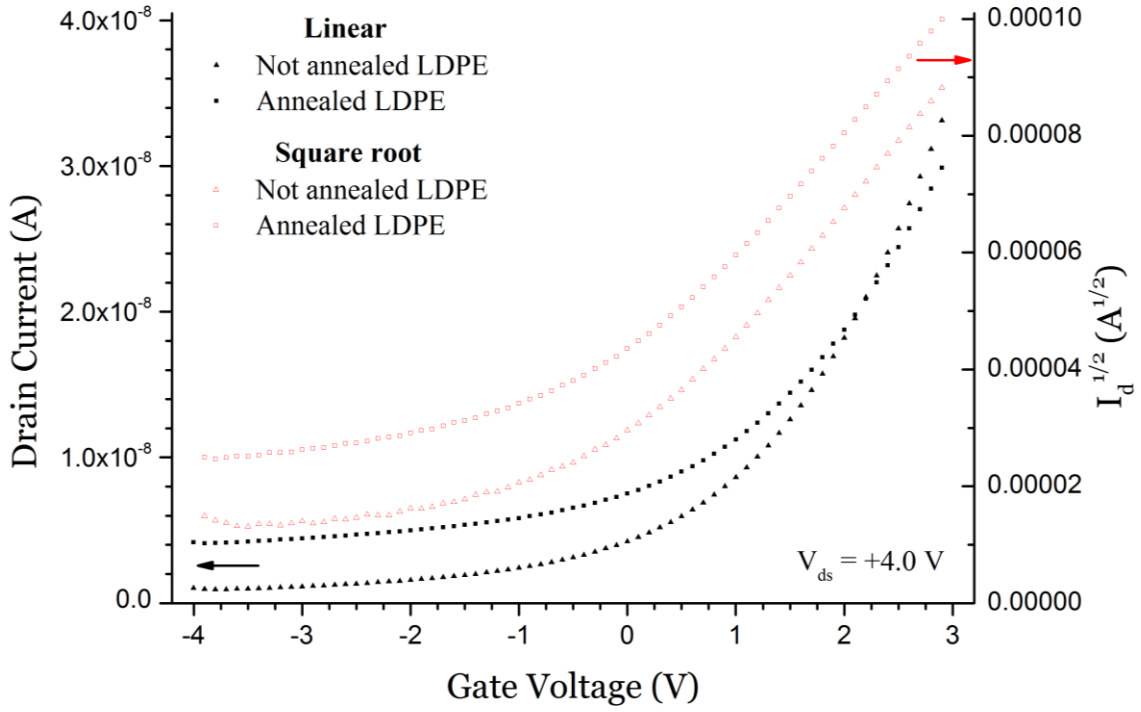

Figure 5-36 – Transfer characteristics of an annealed (squares) and a not-annealed (triangles) top-Ag-contact PDI8-CN_2 OFETs based on LDPE (only) dielectric layers.

5.3.4. Flexible devices

As of October 2013, there are no published examples of PDI8-CN_2 OFETs built on flexible substrates. In this section, the methodology for the fabrication of such devices on plastic substrates and the results from the electrical measurements on them are discussed. Moreover, in section 7.4, the operation of such devices as flexible amine sensors is discussed.

5.3.4.1. *Preparation*

Similarly to the fabrication of flexible pentacene OFETs, described in section 5.2.4.1, the substrates were taken from a common A4-sized laser printer transparency; they were cleaned with an alkaline solution and sonicated at 70 °C. No IPA cleaning and no UV-ozone treatment were applied.

An 100-nm-thick aluminium layer was deposited by thermal evaporation through shadow masks in high vacuum. The deposition rate was adjusted at roughly 0.08 nm/s for the first 10 nm and it was then gradually increased up to 0.5 nm/s. The pressure within the evaporator dome was 7.6 x 10^{-7} Torr in the beginning of the deposition process and reached a maximum of 3.9 x 10^{-6} Torr during the evaporation.

The aluminium films were anodised in a 1 mM citric acid solution. The applied current was set at 0.95 mA and the maximum voltage at 5 V. The current application time was 75 seconds. The devices were rinsed with DI water and dried before further process. Detailed information on aluminium anodisation can be found in section 2.4.2.

For the OTS treatment of the oxide surface, the substrates were immersed into a 10 mg/mL cyclohexane solution of OTS for 10 minutes. This process was carried out in a nitrogen glove box. Further details on OTS treatment are given in section 2.4.3.

A 20-nm-thick film of LDPE was deposited on the substrates after the aluminium anodisation process. No shadow masks were used; LDPE covered the entire surface of the substrates. The deposition rate was limited to 0.005 nm/s for the first 9 nm of thickness and it was then increased to 0.01 nm/s and maintained at this level until the end of the process. The pressure within the dome was kept below 8.0 x 10^{-7} Torr. The substrates were later annealed at 95 °C in ambient atmosphere for 25 minutes. The LDPE-treatment of oxides is discussed in section 2.4.5.

A 50-nm-thick film of PDI8-CN_2 was deposited on the entire surface of all substrates by thermal evaporation. The deposition rate was varied from 0.02 to 0.07 nm/s. The pressure was kept below 8.2 x 10^{-7} Torr throughout the evaporation process. The substrates were not further heated during the semiconductor deposition.

Gold was finally deposited by thermal evaporation though shadow masks. The dimensions of the resulting OFET channels are 10 µm (length) x 2 mm (width). The final thickness of the deposited electrodes was 50 nm. The deposition rate varied from 0.033 to 0.11 nm/s. The pressure was kept below 1.0 x 10^{-6} Torr.

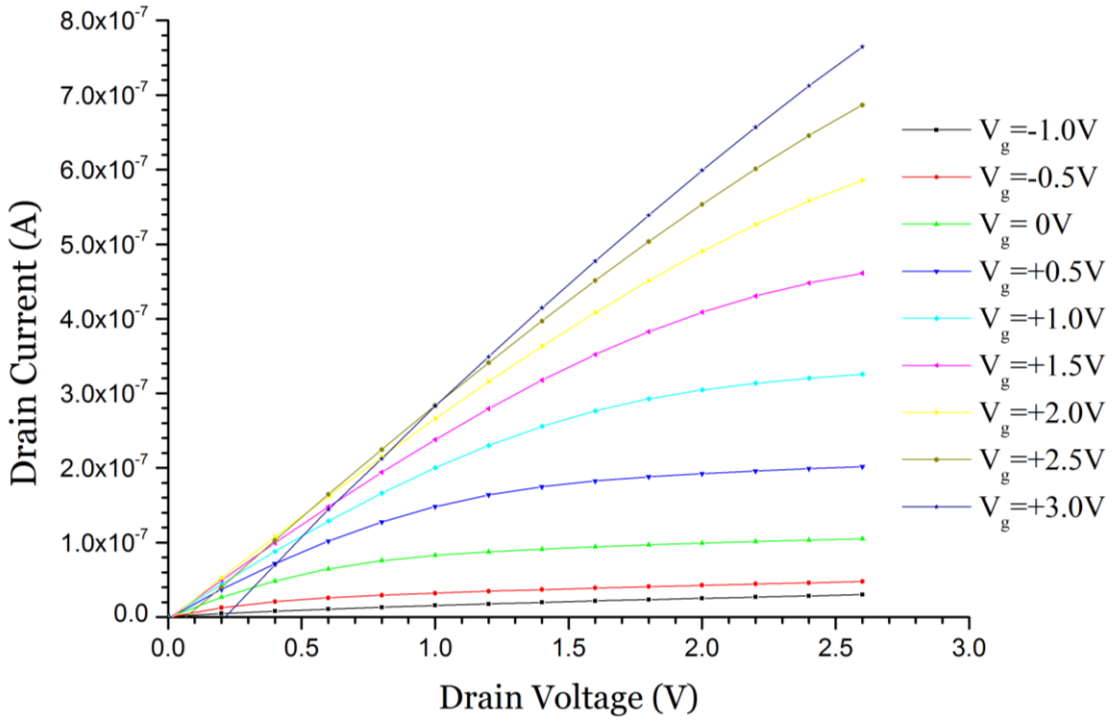

Figure 5-37 – Output characteristics of a flexible top-gold-contact PDI8-CN_2 OFET based on AlO_x-OTS dielectric.

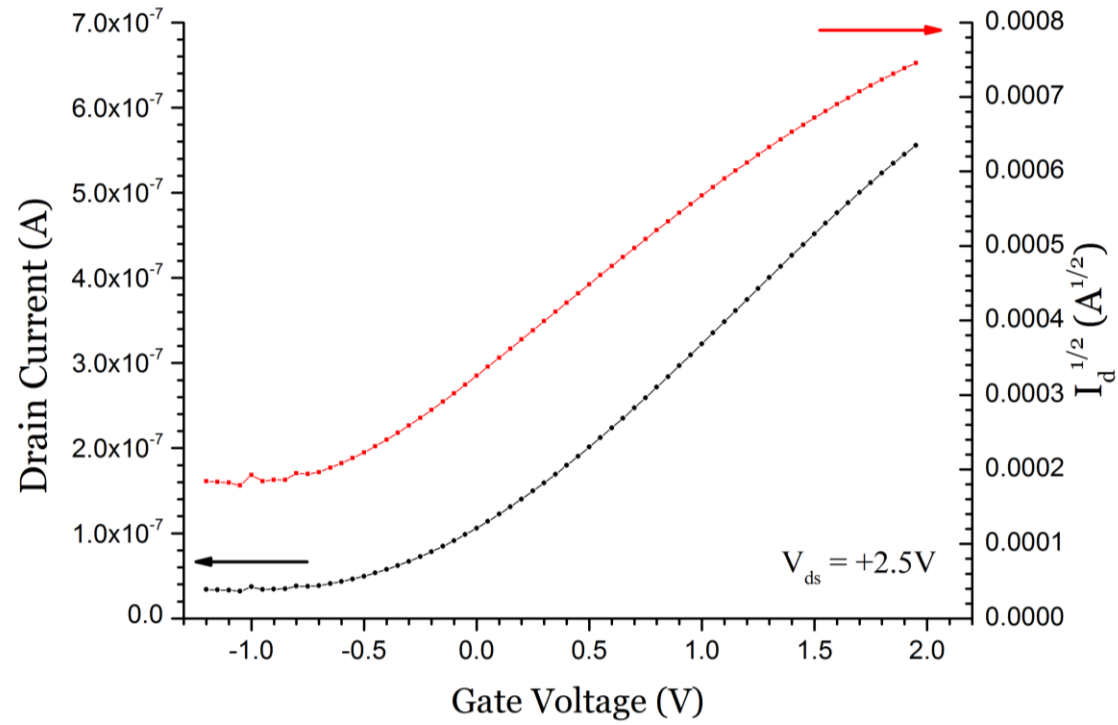

Figure 5-38 – Transfer characteristics of a flexible top-gold-contact PDI8-CN_2 OFET based on AlO_x-OTS dielectric.

5.3.4.2. *Electrical characteristics*

All measurements were taken in ambient conditions, i.e. at room temperature and under usual room light conditions. The electrical characteristics of these devices were comparable with those of the devices built on the same dielectric combination (AlO_x-LDPE) but on rigid substrates, as discussed in section 5.3.2. The threshold voltage of the device under test was found to be -1.3 V, which again indicates a normally-on behaviour; this can be confirmed by both its output and transfer characteristics, shown in Figure 5-37 and Figure 5-38, respectively.

As seen in Figure 5-37, gate leakage was found to start becoming pronounced at V_{ds} = +3 V, which can indicate that the AlO_x dielectric strength is weaker when it is grown on this kind of plastic substrate, as something similar was not observed in the characteristics of the devices with AlO_x-LDPE dielectric which were built on rigid substrates.

The mobility was also found to be comparable; its calculated value was ~1.1 x 10^{-2} $cm^2V^{-1}s^{-1}$. In the deformation tests discussed in section 7.4, it is shown that mobility is highly sensitive to mechanical stress applied to the substrate; this property can potentially be harnessed as a strain sensing parameter.

5.3.5. Comparison and conclusion on PDI8-CN2 OFETs

PDI8-CN_2 is an interesting organic n-type semiconductor with good environmental stability and good mobility [85]. The scarcity of demonstrated examples in the literature gives an additional value to the work presented in this section. The novelties discussed here include the fabrication of OFETs with LDPE-treated SiO_2 and AlO_x dielectrics, OFETs with an all-polymer gate dielectric, as well as flexible OFETs based on this semiconductor; the latter were also used in the mechanical deformation tests and the amine vapour sensing experiments, discussed in section 7.4.

A comparison of the calculated values for all the fabricated PDI8-CN_2 OFET architectures is given in Table 5-II. All investigated OFETs were found to be from largely to marginally normally-on devices. The SiO_2-OTS device had among the highest mobilities, having a value of roughly 1.4 x 10^{-2} $cm^2V^{-1}s^{-1}$, almost double than that of the LDPE-treated one. However, the very negative threshold voltages of both devices make it difficult to switch them off; the SiO_2-OTS device had a V_{th} of -5.8 V, while the SiO_2-LDPE one gave a value of -2.4 V.

AlO_x-OTS on silicon substrate showed a relatively low mobility of roughly 2.0 x 10^{-3} $cm^2V^{-1}s^{-1}$, whereas the values for both AlO_x-LDPE devices were about an order-of-magnitude higher; the device built on silicon had a value of ~1.5 x 10^{-2} $cm^2V^{-1}s^{-1}$ while the value of the device built on a plastic substrate was ~1.1 x 10^{-2} $cm^2V^{-1}s^{-1}$. Regarding threshold voltages, the AlO_x-OTS showed a V_{th} of zero volts, while the rigid AlO_x-LDPE had a V_{th} value of -0.4 V. On the contrary, the AlO_x-LDPE device built on a flexible plastic substrate had an even more negative V_{th} value of -1.3 V.

The investigated PDI8-CN_2 OFETs gated exclusively by an evaporated LDPE layer and employing top silver electrodes showed a slightly lower mobility values than those of the AlO_x-gated devices; the calculated values were roughly 1.0 x 10^{-3} $cm^2V^{-1}s^{-1}$. The annealing of the LDPE insulator prior to the semiconductor deposition was found to affect the off-current and the V_{th} of the devices; the not-annealed device had a V_{th} value of -1.7 V, whereas the value of the annealed device was -0.9 V.

Table 5-II – Comparison of all fabricated PDI8-CN_2 OFET architectures. The cells highlighted in green colour indicate material combinations that have not been reported in the international literature, as of October 2013.

OSC	Substrate	Dielectric	Treatment	Top-contact material	C_i (nF/cm^2)	V_{th} (V)	μ ($cm^2V^{-1}s^{-1}$)	Comments
PDI8-CN_2	**Si/SiO_2**	**SiO_2**	OTS	Au	27	-5.8	0.01369	
			LDPE		27	-2.4	0.00755	
		AlO_x	OTS		480	0.0	0.00196	
			LDPE		98	-0.4	0.01526	
		LDPE		Ag	5	-1.7	0.00095	Not-annealed LDPE
					5	-0.9	0.00106	Annealed LDPE
	Plastic	**AlO_x**	LDPE	Au	98	-1.3	0.01086	Pronounced gate leakage at V_{ds}>+3V

5.4. Tetracene OFETs

The use of tetracene has been demonstrated in the fabrication of OFETs and the organic light-emitting transistors, known as OLETs. Remarkable ambipolar and light emitting properties have been reported for transistors built on tetracene single-crystals in conjunction with a PMMA-treated SiO_2 gate dielectric [77].

In this section, the device fabrication methodology and the results from the electrical characterisation of tetracene OFETs are discussed. As an overall observation, tetracene OFETs were found to have very unstable electrical characteristics when measured in ambient conditions; nevertheless, their interesting light sensitivity can be exploited for specialised applications as discussed in section 6.4.

5.4.1. Aluminium-oxide-gated devices

Tetracene OFETs built on OTS-treated AlO_x dielectric are investigated in this section. The properties of tetracene devices built on SiO_2 dielectric and operated as two-contact devices (with no use of the gate electrode) are discussed in section 6.4.

5.4.1.1. *Preparation*

Silicon substrates with a 100-nm-thick thermal oxide layer were used. They were cleaned by sonication in an alkaline solution and IPA and they were finally treated with UV-ozone. A detailed description of substrate preparation is given in section 2.2.4.

An 100-nm-thick aluminium layer was deposited by thermal evaporation through shadow masks in high vacuum. The pressure within the evaporator dome was 7.4 x 10^{-7} Torr in the beginning of the deposition process and reached a maximum of 3.7 x 10^{-6} Torr during the evaporation. The deposition rate varied from 0.003 nm/s to 0.8 nm/s.

The aluminium films were anodised in a 1 mM citric acid solution. The applied current was set at 0.95 mA and the maximum voltage at 5 V. The current application time was 75 seconds. The devices were rinsed with DI water and dried before further process. Detailed information on aluminium anodisation can be found in section 2.4.2.

For the AlO_x-OTS devices, the substrates were immersed into a 10 mg/mL cyclohexane solution of OTS for 10 minutes. This process was carried out in a nitrogen glove box. Further details on OTS treatment are given in section 2.4.3. These substrates were stored in a dark vacuum oven for several weeks before tetracene deposition.

A 50-nm-thick film of tetracene was deposited on the entire surface of all substrates by thermal evaporation. The deposition rate varied from 0.07 to 0.09 nm/s. The pressure was kept below 3.3 x 10^{-7} Torr throughout the evaporation process. The substrates were not further heated during the semiconductor deposition.

Gold was finally deposited by thermal evaporation though shadow masks. The dimensions of the resulting OFET channels were 10 μm (length) x 2 mm (width). The final thickness of the deposited electrodes was 50 nm. The deposition rate varied from 0.013 to 0.08 nm/s, while the pressure was kept below 1.7 x 10^{-6} Torr.

5.4.1.2. *Electrical characteristics*

The electrical characteristics of the tetracene OFETs with AlO_x-OTS dielectric exhibited significant instability issues; consecutive drain or gate voltage sweeps yielded largely different results, mainly due to pronounced hysteresis. Figure 5-39 shows the oscilloscope screenshot from the I-V converter characterisation system, discussed in Chapter 4; in this plot, hysteresis is clearly observed in the difference between the rising and falling flanks of the output (blue) curve. In addition, even low light intensities had a large impact on the electrical properties of these tetracene devices, as discussed in detail in section 6.4.2.1.

Some representative output characteristics of a tetracene OFET are shown in Figure 5-40. In this graph, at the highest gate bias of -3 V, a curvature and drop of drain current was observed for high drain voltages above saturation. Interestingly, a very similar behaviour can be seen in the graphs given in published work on SiO_2-gated tetracene OFETs with NiO_x top electrodes [122].

The transfer characteristics of the same device are shown in Figure 5-41. The values of threshold voltage and mobility were found to be very similar to those of pentacene devices built on the same dielectric combination (AlO_x-OTS), discussed in section 5.2.2.2; the calculated value of V_{th} was -1.7 V and the value of μ was roughly 6.0 x 10^{-4} $cm^2V^{-1}s^{-1}$.

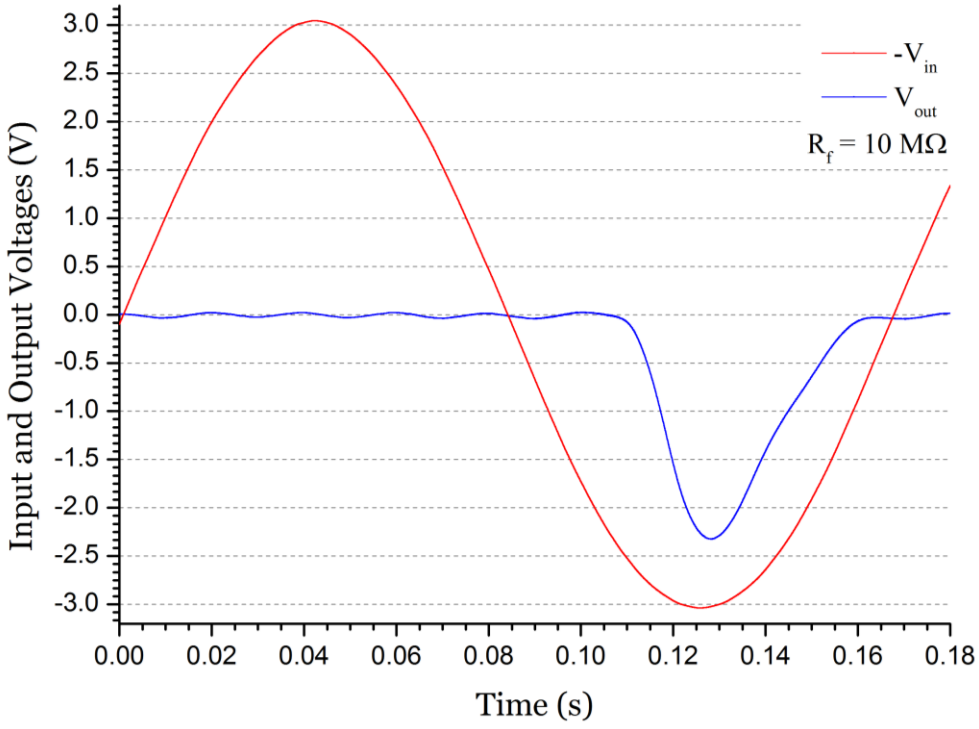

Figure 5-39 – Oscilloscope screenshot of a top-gold-contact tetracene OFET based on AlO_x-OTS dielectric measured with the I-V converter system. The minor oscillation seen in the V_{out} (blue) curve is due to mains pickup (50Hz).

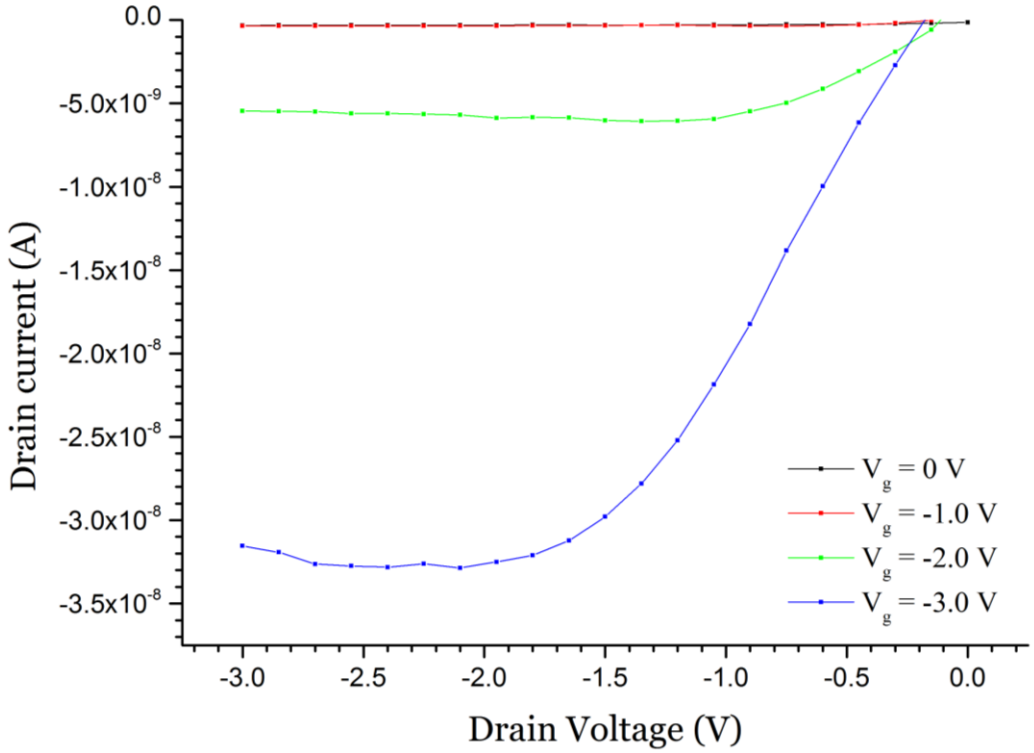

Figure 5-40 – Output characteristics of a top-gold-contact tetracene OFET based on AlO_x-OTS dielectric.

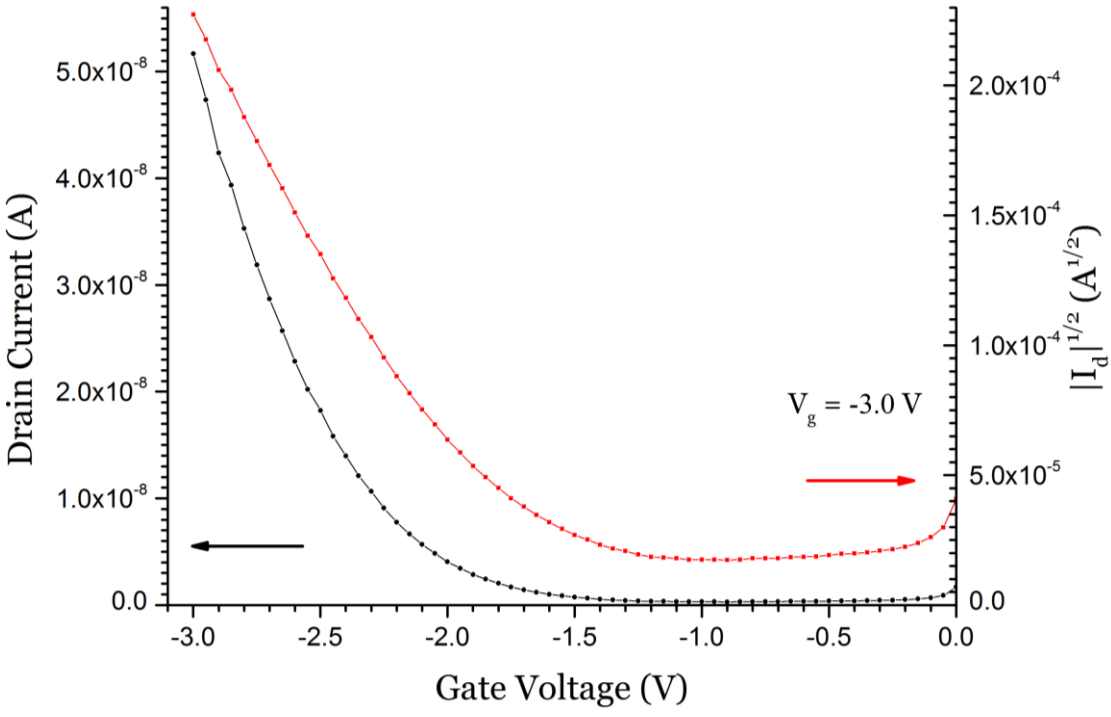

Figure 5-41 – Transfer characteristics of a top-gold-contact tetracene OFET based on AlO_x-OTS dielectric.

5.5. PBTTT OFETs

As discussed in section 2.5.5, a variety of poly(2,5-bis(3-alkylthiophene-2-yl)thieno[3,2-b]thiophenes), known as *PBTTT*, semiconducting polymers with alkyl side chains of different lengths have been developed; examples of their exploitation as active materials in OFETs have shown remarkable charge carrier mobility values and enhanced environmental stability than other common polythiophenes such as P3HT [95, 123].

In this section, the fabrication methodology and the results from the electrical characterisation of SiO_2-gated OFETs based on a PBTTT polymer with a $C_{16}H_{33}$ side chain (PBTTT-C16) are discussed. Devices of this architecture were also used as sensing transducers for the alcohol vapour sensing tests, discussed in section 7.3.

5.5.1.1. *Preparation*

The employed substrates were taken from an arsenic-doped silicon wafer covered with a 300-nm-thick thermal SiO_2 layer. The substrates were cleaned with the standard cleaning process, i.e. they were sonicated in an alkaline solution and in IPA and a final UV-ozone treatment was applied for 270 seconds. More details on substrate preparation are given in section 2.2.4.

No surface treatment was applied to the SiO_2 surfaces. An adhesion-promoting bilayer of patterned aluminium (Al) and chromium (Cr) pads was deposited on the SiO_2 surface; the thickness of each layer was 10 nm for Al and 5 nm for Cr. The shadow masks used were of the same pattern and dimensions as the gold masks discussed below.

PBTTT-C16 was dissolved in 1,2-dichlorobenzene (7.5 mg/mL) and heated at 100 °C. An amount of 50 µL of pre-heated solution was spin cast onto each substrate; the substrates were spun at 1500 rpm for 60 seconds. All substrates were annealed at 95 °C in ambient atmosphere for 45 minutes. All solution preparation, spin coating and annealing processes were conducted in dimmed light conditions.

Gold was deposited with thermal evaporation through shadow masks; the masks were aligned with the previously deposited Al/Cr adhesion promoting pads. The resulting channel dimensions were 5 µm (length) by 1 mm (width); 20 OFETs were made on each substrate. The deposition rate varied from 0.023 to 0.043 nm/s, while the pressure was kept below 2.3×10^{-6} Torr throughout the deposition process.

5.5.1.2. *Electrical characteristics*

All measurements were taken in ambient conditions, i.e. at room temperature and under usual room light conditions.

Figure 5-42 and Figure 5-43 show the output and transfer characteristics of device under test. Similarly to the SiO_2-OTS pentacene devices, the output curves show that drain current did not saturate regardless of the absence of off-current. The threshold voltage was found to have a very low value of -0.5 V and the mobility was calculated at roughly 1.2×10^{-2} $cm^2V^{-1}s^{-1}$. As a reference, mobility values of 0.6 $cm^2V^{-1}s^{-1}$ for PBTTT-C14 OFETs based on OTS-treated SiO_2 dielectric have previously been reported [124]; this significant difference can be attributed to the fact that OTS treatment enhances grain formation and results in higher charge carrier mobility values.

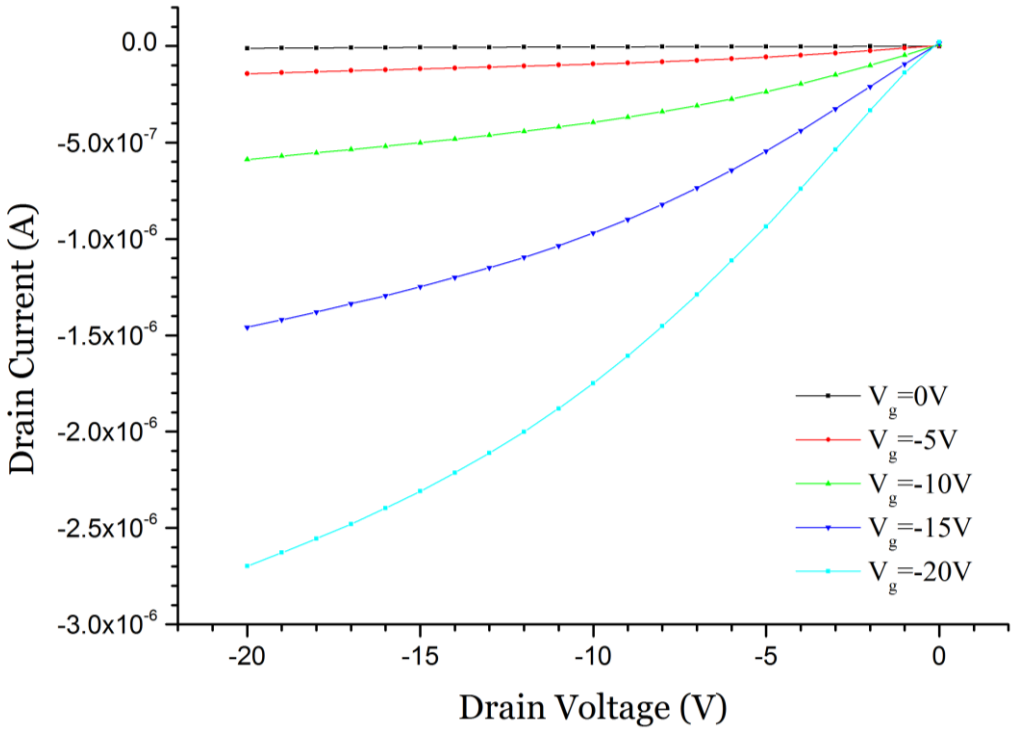

Figure 5-42 – The output characteristics of a top-Au-contact PBTTT OFET built on SiO_2.

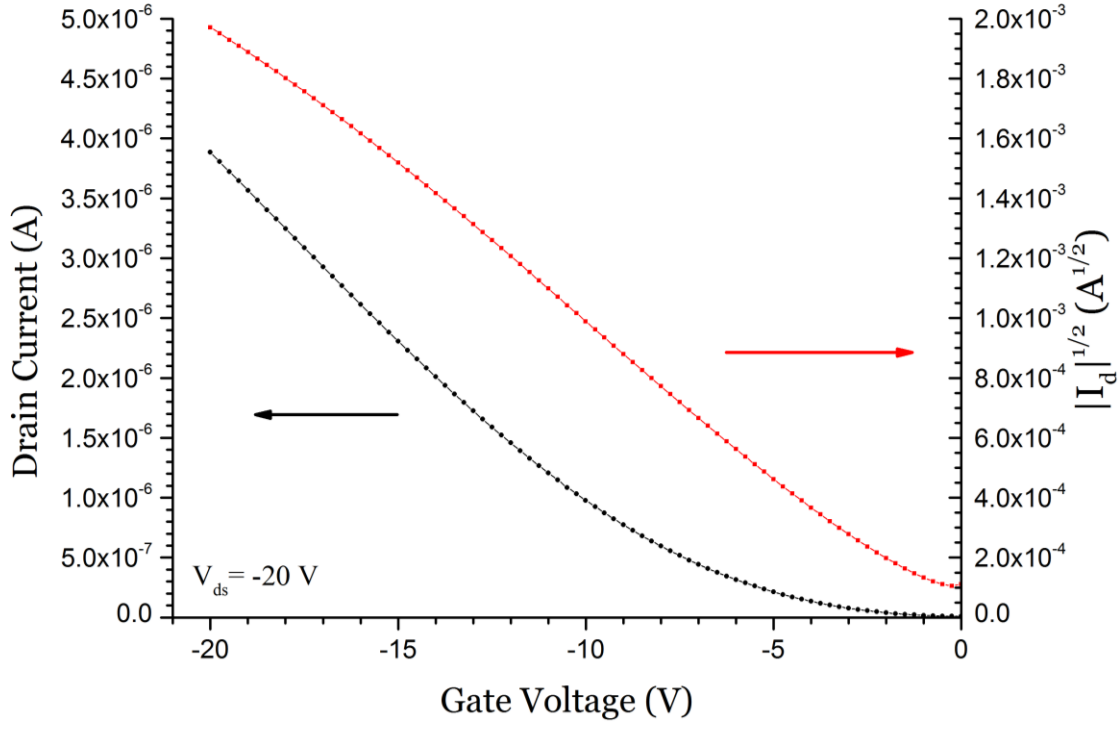

Figure 5-43 – Transfer characteristics of a top-Au-contact PBTTT OFET built on SiO_2. Left y-axis: modulus of drain current versus gate voltage. Right y-axis: square root of the modulus of drain current versus gate voltage

5.6. Overall comparison of fabricated OFETs

The results from the electrical characterisation of all OFETs presented in this section are summarised in Table 5-III. The values extracted from the experimental data reveal the typically low (<1 $cm^2V^{-1}s^{-1}$) charge carrier mobility of organic semiconductors; this performance is inferior to that of inorganic semiconductors. This fact confirms that OSCs are inappropriate for demanding applications where the high output impedance of a semiconductor device would compromise the performance of an integrated system. Nevertheless, the OSCs remain a very competitive and versatile solution for specialised applications, such as the vapour sensing systems discussed in Chapter 7.

Table 5-III – Comparison of OFET electrical characteristics. The cells highlighted in green colour indicate material combinations that have not been reported in the international literature, as of October 2013.

OSC	Substrate	Dielectric	Treatment	Top-contact material	C_i (nF/cm^2)	V_{th} (V)	μ ($cm^2V^{-1}s^{-1}$)	Comments
Pentacene	**Si/SiO_2**	**SiO_2**	OTS	Au	27	-1.4	0.10537	Poor saturation
			LDPE		27	-2.4	0.05671	
		AlO_x	OTS		480	-1.0	0.00070	
			LDPE		98	-1.4	0.00315	
		LDPE			5	-3.2	0.00004	
	Plastic	**AlO_x**	LDPE		98	-1.7	0.02119	Ambipolar behaviour
$PDI8\text{-}CN_2$	**Si/SiO_2**	**SiO_2**	OTS	Au	27	-5.8	0.01369	
			LDPE		27	-2.4	0.00755	
		AlO_x	OTS		480	0.0	0.00196	
			LDPE		98	-0.4	0.01526	
		LDPE		Ag	5	-1.7	0.00095	Not-annealed LDPE
					5	-0.9	0.00106	Annealed LDPE
	Plastic	**AlO_x**	LDPE	Au	98	-1.3	0.01086	Pronounced gate leakage at V_{ds}>+3V
Tetracene	**Si/SiO_2**	**AlO_x**	OTS	Au	480	-1.7	0.00060	
PBTTT-C16	**Si/SiO_2**	**SiO_2**	none	Au	9	-0.5	0.01174	Poor saturation

The highest mobility of 0.105 $cm^2V^{-1}s^{-1}$ was recorded for a pentacene OFET based on SiO_2-OTS dielectric. For both pentacene and $PDI8\text{-}CN_2$ devices with SiO_2 dielectric, the OTS treatment of the oxide resulted in roughly double mobility values than those on LDPE-treated surfaces.

The pentacene devices built on AlO_x dielectric showed significantly lower mobility values; this result comes in good agreement with previously published work on other hole-transporting

semiconductors gated with AlO_x. Interestingly, the electron-transporting PDI8-CN_2 devices showed slightly better mobility characteristics on AlO_x rather than on SiO_2.

The tetracene OFETs on AlO_x-OTS dielectric showed very similar characteristics to the pentacene devices built on the same dielectric combination.

The PBTTT-C16 OFETs built on bare SiO_2 showed very low threshold voltage values and had a mobility of roughly 6.0 x 10^{-3} $cm^2V^{-1}s^{-1}$.

Moreover, the green-shaded cells of Table 5-III show the material combinations which have not been demonstrated in the literature, as of October 2013. An interesting example is the demonstrated pentacene OFET which was exclusively gated by an evaporated LDPE layer; this is the only example of a hole-transporting semiconductor ever reported to operate on this dielectric.

Finally, Figure 5-44 shows two pairs of PDI8-CN_2 and pentacene OFETs built on a plastic substrate with AlO_x-LDPE dielectric, in an early attempt to fabricate a flexible CMOS inverter based on these two semiconductors. All devices operated well when tested individually, but failed to operate as an inverter when appropriately wired as such; this could be due to either the normally-on behaviour of PDI8-CN_2 or the difference in the mobility values of pentacene and PDI8-CN_2 built on the same dielectric. Further optimisation of this approach is suggested as a future goal.

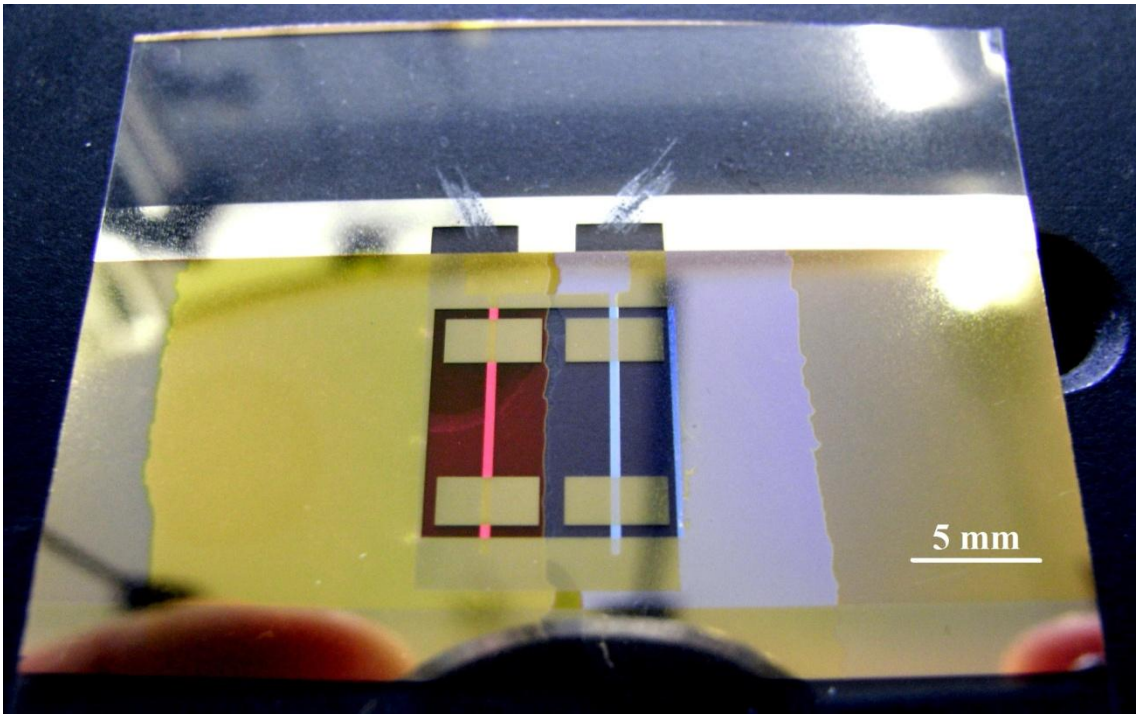

Figure 5-44 – A photograph of two pairs of PDI8-CN_2 (red on LHS) and pentacene (purple on RHS) low-voltage OFETs built on the same plastic substrate.

Chapter 6. **Light sensitivity of organic semiconductor devices**

One of the most attractive potentials of organic semiconductors (OSCs) is their exploitation in optoelectronic applications. Devices such as organic light-emitting diodes (OLEDs) and organic photovoltaics (OPVs) currently are the flagships of organic semiconductor industry; prominent examples are the use of active-matrix OLED (AMOLED) displays in Samsung's top-of-range smartphones [125], and the very recently announced curved smartphone by LG, which employs an 6-inch OLED display built on a plastic substrate [126].

Although the sensitivity of OSCs to light is the operating principle of some devices such as OPVs, this property remains unwanted for several applications in which device stability is of vital importance. OFETs used as sensing transducers fall within this category; the sensitivity of any sensing parameter to environmental conditions can lead to erratic behaviours, which can be misinterpreted as sensing responses. In some device configurations, the light-related problems can be mitigated by the application of opaque encapsulation layers; however, in the case of OFET operating as gas sensing transducers, no encapsulation can be applied to the surface of the semiconductor as it should be exposed to the environment so that an airborne substance can be detected. This fact puts more accent on the value of light stability of OFETs in such applications.

This chapter focuses on the effects of light on several electrical parameters of OFETs. A comprehensive study of the results of different wavelength ranges on the gate capacitance, drain current, threshold voltage and mobility of pentacene and PDI8-CN_2 OFETs is presented in sections 6.1 to 6.3. The tests discussed here include spectral analyses of the emitted (incident) light and the semiconductor film absorption, impedance measurements on capacitors, and real-time multiparametric OFET measurements in bespoke light-exposure test rigs. Moreover, the results from a separate study on tetracene-based devices are discussed in section 6.4.

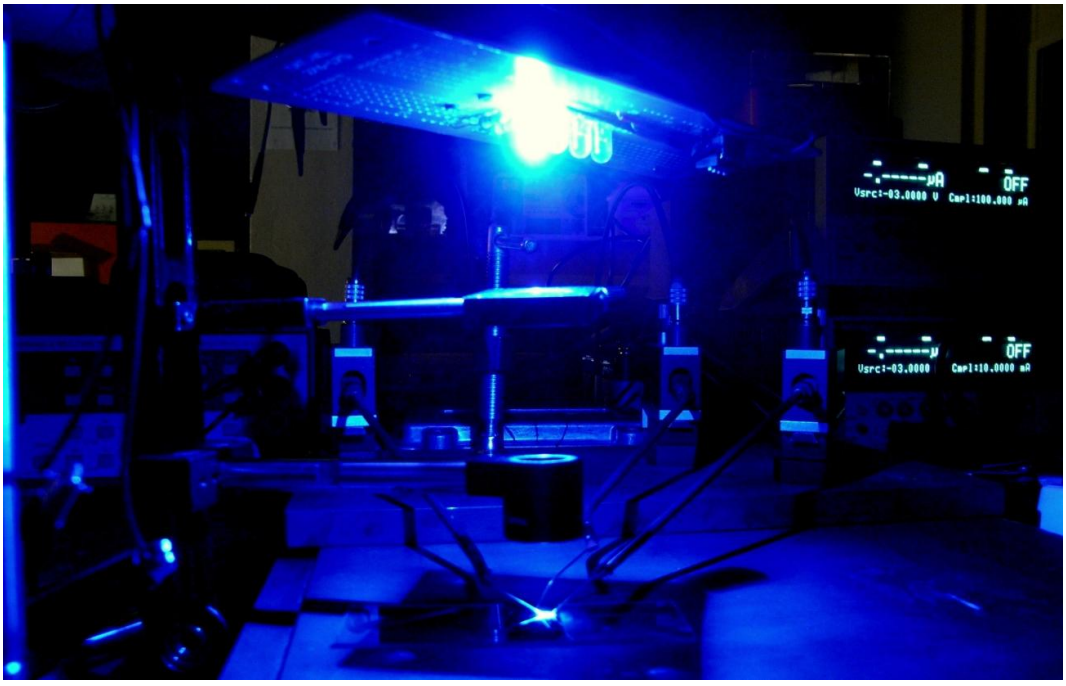

Figure 6-1 – A photograph of an illuminated OFET under test placed on light exposure test rig

6.1. Experimental methods

For the wavelength-dependent light sensitivity measurements on capacitors and OFETs, which are presented in sections 6.2 and 6.3, a special light exposure test rig was built. The light sources were measured and calibrated using a spectrometer. Moreover, the absorption spectra of thin films of pentacene and PDI8-CN_2 were studied. This section describes the methodology followed for the delivery of these measurements.

6.1.1. Thin-film sample preparation

For a deeper understanding of the light-induced phenomena in OFETs, discussed in section 6.3, a study of the absorption spectra of the employed semiconductors was conducted. Thin films of both organic semiconductors studied here were deposited on transparent substrates for later analysis using a spectrometer, as discussed in the following section.

Two sets of round substrates (diameter: 20 mm) made of fused quartz were used for this work; they were initially cleaned by immersion in a Petri-dish filled with IPA and then dried using dry nitrogen. A 50-nm-thick film of pentacene was deposited on the first set of samples using thermal evaporation; the pressure of the evaporator dome was kept below 3.9 x 10^{-7} Torr and the deposition rate was varied from 0.02 to 0.07 nm/s. Similarly, on the second set of samples, 50 nm of PDI8-CN_2 were deposited in a high vacuum with a pressure kept below 6.4 x 10^{-7}; the deposition rate varied from 0.016 to 0.023 nm/s. None of the substrates were additionally heated during the semiconductor evaporation. Additionally, two cleaned blank substrates later served as control samples for the spectral measurements.

6.1.2. Spectral analysis and LED calibration setup

Four commercial high-brightness light-emitting diodes (LED) were used as light sources (Multicomp OVL-5528, OVL-5526, OVL-5524 and OVL-5523). Their nominal peak wavelengths are 465 nm, 520 nm, 589 nm and 625 nm for the blue, green, yellow and red LED, respectively.

For various constant DC current values, over the entire LED operating range, the electroluminescence emission of the LEDs was collected with an optical fibre coupled to a spectrometer (*Andor Shamrock 303i*). Considering their identical emission patterns, as given by their specifications, and due to their high intensity, the LEDs were measured from a fixed position, at a distance of 30 cm from the input of a centrally aligned optical fibre without additional focussing lenses; this approach was followed in order to avoid the saturation of the spectrometer sensor. The aperture (slit) of the spectrometer was set to 10 μm and the exposure time to the minimum setting of 21 ms for all measurements. The LEDs were powered by a programmable current source (*Keithley 2400*) and the total photon counts under various driving forward currents were measured for each of them.

The absorption spectra of the semiconductors were also calculated from transmission measurements; a white light source was used to shine light on one side of the fused quartz samples, described in the previous section, and the input of the optical fibre of the spectrometer was placed on their opposite sides. The absorption spectra were calculated by the spectrometer control software. In addition, measurements on blank control samples were performed for comparison and correction of the results. Figure 6-2 shows the normalised

absorption spectra of pentacene and PDI8-CN_2 along with the emission spectra of the four LEDs, all driven with a DC current of 15 mA.

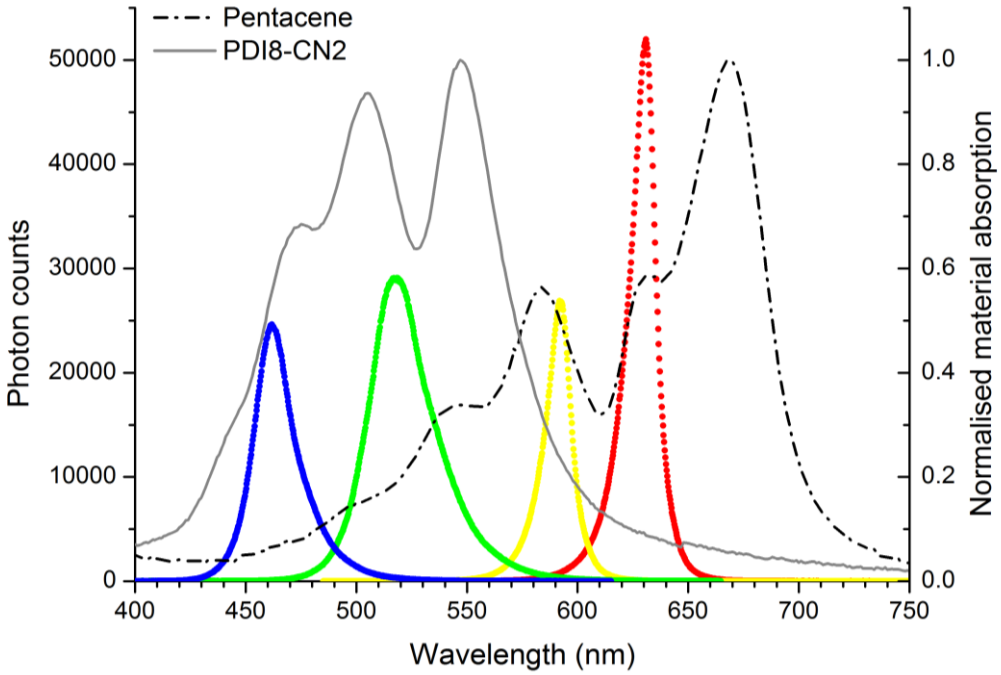

Figure 6-2 – Comparison of the spectra of the four LEDs (coloured curves) with the normalised absorption spectra of a pentacene (dashed black curve) and a PDI8-CN_2 (solid grey curve) films deposited on quartz substrates. Left Y-axis: measured photon counts for I_f=15mA, spectrometer slit diameter: 10 µm and exposure time: 21 ms. Right Y-axis: normalised absorption of the 50-nm-thick pentacene and PDI8-CN_2 films.

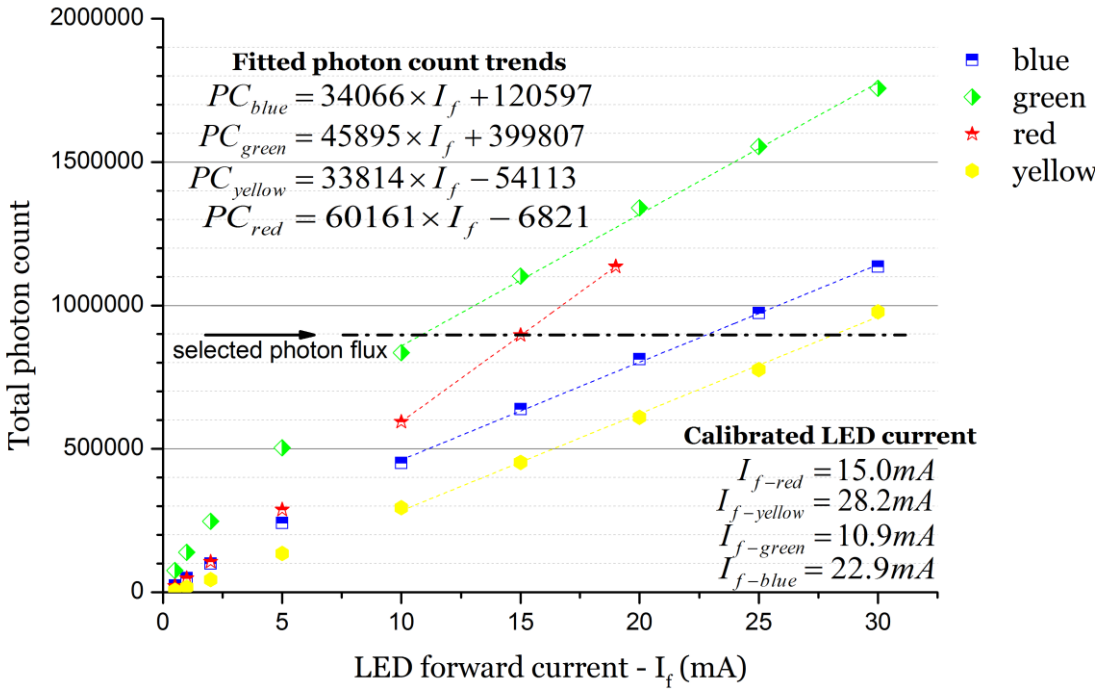

Figure 6-3 – Total photon counts (integrals) of the four LEDs versus forward drive current for the same measurement conditions. Simple linear regression fits for the linear (higher) operating region of each LED are shown as dashed lines. A total photon count value of 9 x 10^5 was selected; this value corresponds to a photon flux of 5.5 x 10^{17} photons x m^{-2} x s^{-1} for the given spectrometer settings. The calibrated drive current values for the selected photon flux are shown on the bottom right.

For reliable comparative tests between different wavelengths of light, the drive voltages which effectively yield the same photon flux were calculated for each LED. As shown in Figure 6-3, for a photon count of 9 x 10^5, which, for the given spectrometer settings, corresponds to a photon flux of 10^{24} photons x m^{-2} x s^{-1}, the LED forward currents (I_f) were calculated to be 22.9 mA, 10.9 mA, 28.2 mA and 15.0 mA, for the blue, green, yellow and red LED, respectively.

6.1.3. Exposure optics setup

Appropriate light exposure and characterisation rigs were built for the tests on capacitors and OFETs. The four LEDs analysed in the previous section were soldered onto a printed-circuit board (PCB) which, in turn, was attached to a horizontal rail at a height of 120 mm from the device under test (DUT). A collimating and a focusing lens were placed between them providing a focused beam which illuminated the entire OFET channel area. Comparing the illuminated area of the sample to the aperture of the spectrometer sensor and assuming that the intermediate lenses do not attenuate the light and that the entire beam shines on the channel area, the calibrated photon flux on the surface of the OFET channel can be estimated to be 7 orders of magnitude higher than the value measured by the spectrometer, i.e. roughly 10^{24} photons x m^{-2} x s^{-1}.

Specific details on the characteristics of the light exposure test rigs for capacitors and OFETs are given in sections 6.2.1 and 6.3.2, respectively.

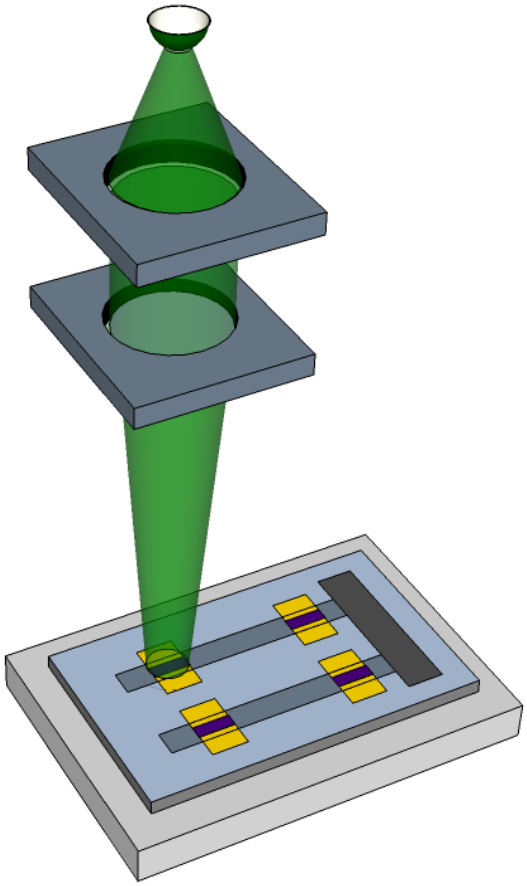

Figure 6-4 – A sketch of the light exposure test rig

6.2. The effect of illumination on gate capacitance

For a comprehensive study of the light sensitivity of devices with complex structure, such as OFETs, it is meaningful to investigate the individual effects that can be induced on each of their building blocks. For this reason, along with the previously discussed investigation of the absorption spectra of the employed semiconductors, a study of the effects of illumination on the gate stack was considered as an important supplement. For this purpose, the capacitors which had been fabricated and served as a tool for the quantification of their dielectric permittivity, as discussed in section 5.1, were then tested under light exposure. In principle, the large energy bandgap of the employed dielectrics, i.e. aluminium oxide (AlO_x) and low-density polyethylene (LDPE), do not absorb light of the wavelengths used for these measurements and thus, they cannot be affected by such illumination. Interestingly, the results from the tests on AlO_x-based capacitors revealed an unusual behaviour, which has not been reported before. The methods used and the results of these series of tests are discussed in this section.

6.2.1. Test methodology

Three sets of capacitors based on three different dielectric configurations, namely: AlO_x-OTS, AlO_x-LDPE and LDPE (only), were used for these tests. The preparation procedure for all sets of capacitors is described in section 5.1.1. The thin silver layers, which served as the top electrodes, were semi-transparent, permitting the incident light to reach the dielectric.

The impedance measurement rig described in section 3.2 was modified for the light sensitivity tests; the metal box lid was removed and the assembly comprising the calibrated LEDs and the lenses, described in sections 6.1.2 and 6.1.3, respectively, was attached to it.

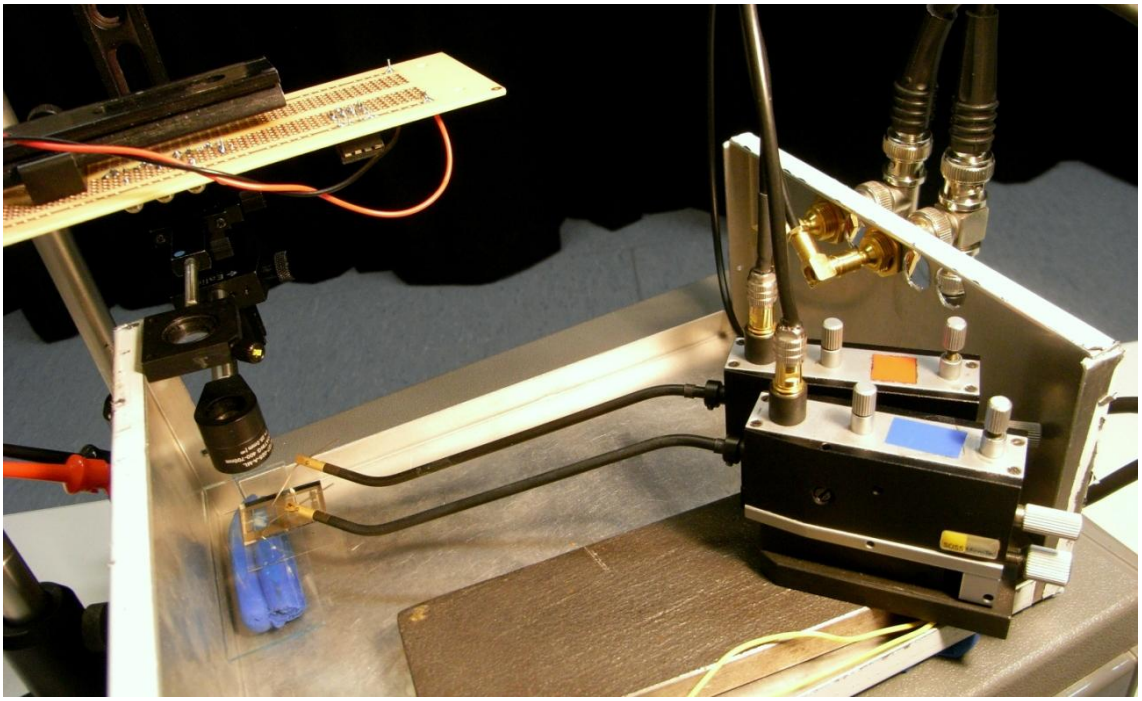

Figure 6-5 – A photograph of the actual light illumination test rig for impedance measurements on capacitors.

The same impedance analyser (*Solartron SI 1260*) was used and the same settings were applied: a frequency sweep from 1 Hz to 10 KHz for a zero-offset AC drive with an amplitude of

1 V. The capacitors were initially measured in the dark and then under red, yellow, green and blue light with interleaving recovery periods in the dark. The capacitors were illuminated for one minute before the measurement sweep was applied and they were left to recover for 5 minutes between illuminations. Control measurements were also taken in the dark during these interleaving recovery periods.

6.2.2. Discovery of photocapacitance

Figure 6-6 to Figure 6-8 show the plots of C_i versus frequency for the three kinds of capacitors under all light conditions. The results from impedance measurements in the dark are also discussed in section 5.1.

Recalling the discussion given in section 5.1.2, the AlO_x-LDPE devices showed an unexpectedly high capacitance, with a C_i of roughly 680 nF/cm^2 in dark conditions. This is explained by the possible penetration of silver into the not-annealed, very thin LDPE layer, which, as demonstrated by Kanbur *et al.* [72], is very like to have voids. Considering that the gate stacks of all AlO_x-LDPE OFETs were annealed, this sample does not represent the actual gate stack of the respective OFETs. However, this capacitor was tested under illumination for comparison with the AlO_x-OTS sample. The values for the AlO_x-OTS device fell in the same order of magnitude with a C_i of 480 nF/cm^2 in the dark. It is worth mentioning that, for both AlO_x-based capacitors, capacitance dropped significantly with increasing frequency.

When exposed to light, both capacitors exhibited a substantial capacitance increase, which was independent of the wavelength of the incident light; all calibrated light sources, which roughly cover the entire visible light spectrum, induced almost identical results. For the reference bias frequency of 6.33 Hz, the relative capacitance changes ($\Delta C_i/C_{i,0}$) varied between 15% to 18.5% for both capacitors and for all wavelength ranges; the comparative results are shown in Figure 6-9. Additional measurements were conducted during the intermediate dark periods; a new measurement sweep was applied one minute after each illumination was switched off. In all cases, the measured capacitance values recovered to their respective pre-exposure levels; however, considering this one-minute-long window, it remains unknown whether this quick recovery is immediate or takes some seconds.

Contrarily, the LDPE (only) capacitor was found to be largely immune to illumination, as no significant capacitance change was measured over the entire range of applied drive frequencies. Neglecting the noisy figures at low frequencies, the capacitance of this all polymer dielectric was insensitive to both light and the frequency of the applied bias. These results nominate an LDPE (only) architecture as a good candidate for a light stable gate stack, at the expense of a much lower C_i. When light stability is of vital importance, a compromise in gate capacitance can be made; besides, low-k dielectrics have been demonstrated as a good choice for OFET dielectric, as they can enhance charge carrier mobility and mitigate its degradation under gate bias thanks to their low polarity [58]. The low polarity of LDPE can be considered as an important factor for the immunity of these capacitors to both high frequencies and illumination.

The phenomenon of dielectric photocapacitance has not attracted significant attention in the literature, as the relevant publications are scarce; there are few published studies on metal-insulator-semiconductor (MIS) devices employing both inorganic [127, 128], and organic semiconductors [129]. The structural differences between these demonstrated examples and the devices presented here do not allow for direct comparisons between them. In the latter

example [129], Watson *et al.* used a well-known photosensitive semiconductor, poly(3-hexylthiophene) (P3HT) for their MIS capacitors; presumably, the detected capacitance changes under illumination were mainly due to the sensitivity of P3HT which overshadowed any sensitivity of the employed dielectric.

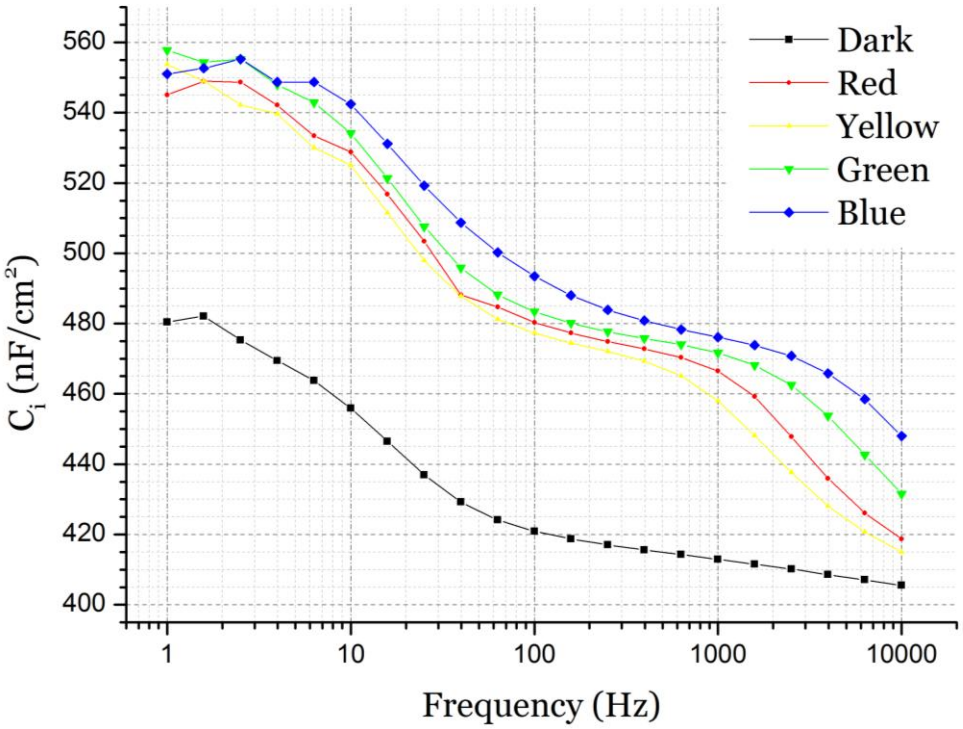

Figure 6-6 – Capacitance per unit area versus frequency for an Al-AlO_x-OTS-Ag capacitor versus frequency in the dark and under red, yellow, green and blue light. AC amplitude: 1 V. DC offset: 0 V.

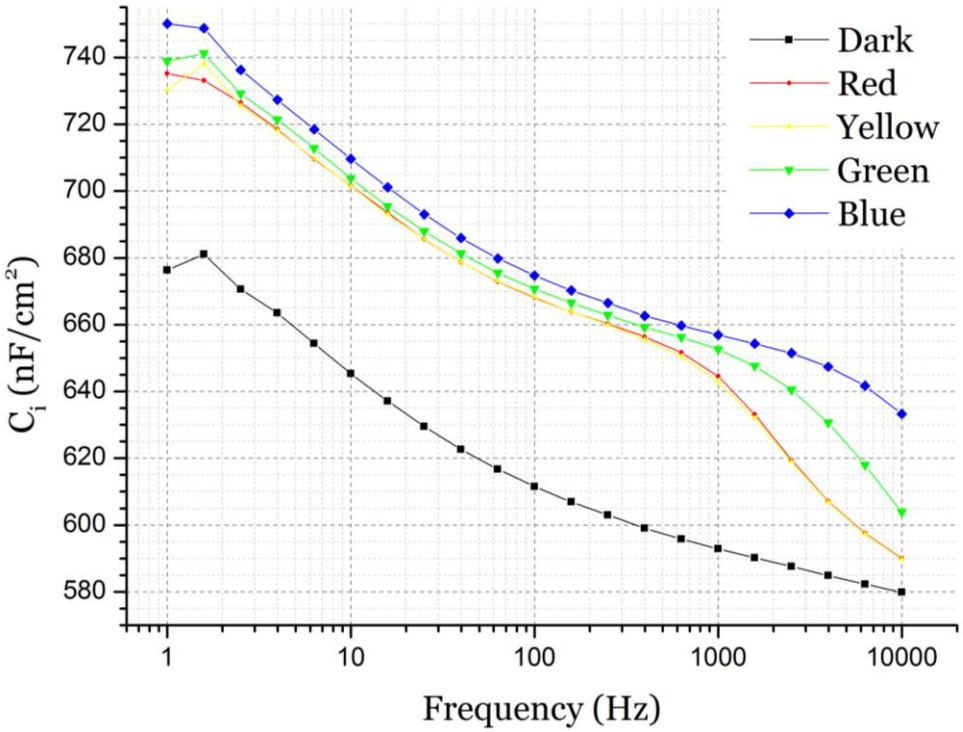

Figure 6-7 – Capacitance per unit area versus frequency for an Al-AlO_x-LDPE-Ag capacitor versus frequency in the dark and under red, yellow, green and blue light. AC amplitude: 1 V. DC offset: 0 V.

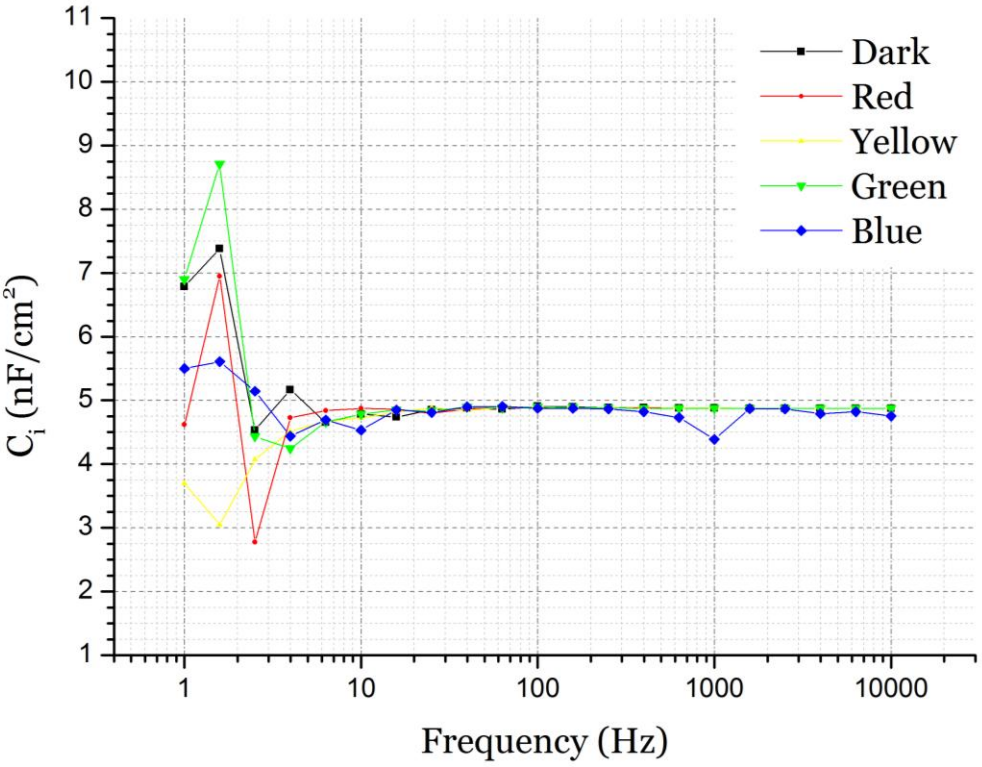

Figure 6-8 – Capacitance per unit area versus frequency for an Ag-LDPE-Ag capacitor versus frequency in the dark and under red, yellow, green and blue light. AC amplitude: 1 V. DC offset: 0 V.

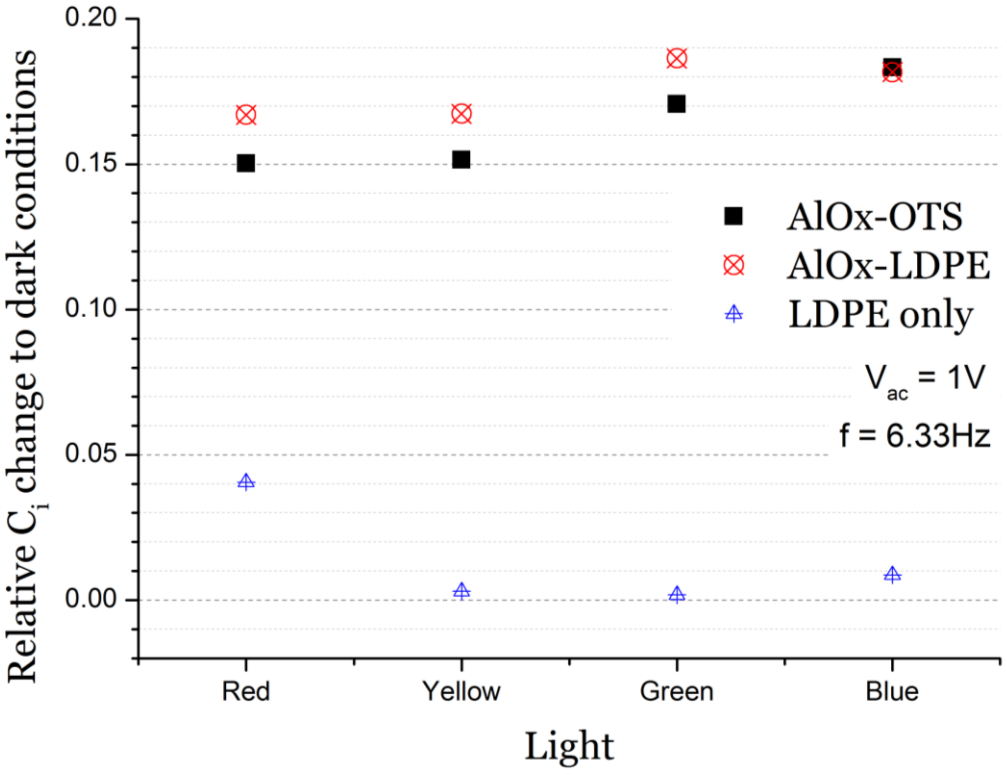

Figure 6-9 – Relative C_i change for AlO_x-OTS (black squares), AlO_x-LDPE (red circles) and LDPE (only) (blue triangles) capacitors under red, yellow, green and blue light illumination.

However, as of October 2013, there are no reports of light-induced capacitance changes in simple capacitor structures, based exclusively on oxide dielectrics. The sensitivity or inertness to illumination can be related to the changes that light can or cannot, respectively, induce on the polarisability and thus, the electric dipole moment of the dielectric; such changes can rationalise a change in the permittivity of the dielectric. The fact that the energy of the incident photons is much lower than the bandgap of the AlO_x dielectric can possibly be explained by the presence of impurities, which introduce allowed energy states within the bandgap, or the fact that anodised AlO_x is not as stoichiometric as alumina made with other techniques, such as magnetron sputtering. The study and analysis of these interesting phenomena extend far beyond the scope of this work; nevertheless, a further investigation of the effects of illumination on anodised AlO_x capacitors and comparison with capacitors made of other oxides is proposed as future work.

6.2.3. Conclusion

Light exposure measurements on capacitors showed that aluminium oxide (AlO_x) capacitors are remarkably susceptible to light as their capacitance increases under illumination. As of October 2013, this behaviour has not been reported in the literature. The fact that this behaviour was observed in capacitors sourced from different device batches and employing differently surface-treated oxides, denotes that the photosensitivity is inherent to the anodised oxide itself rather than the surface treatment material.

According to the wavelength-resolved measurements using calibrated light sources with different emission spectra but the same photon flux, the effect of light on all AlO_x capacitors was found to be independent of the wavelength of the incident light, at least within the visible frequency range. A full and rapid recovery was observed once the capacitors were returned in dark conditions.

Conversely, LDPE capacitors were found to be immune to any of these tested wavelength ranges. This attribute nominates them as a good dielectric candidate for light-stable OFETs.

The findings from the tests on the AlO_x-based devices justify and motivate a further, thorough investigation of the phenomenon of photocapacitance; experiments that confirm these important observations remain to be carried out. Anodised AlO_x capacitors with no surface treatment must be fabricated for the reproduction and confirmation of the results presented here. Then, considering that all four calibrated light wavelength ranges induced very similar changes in capacitance, it is worth investigating the effect of different photon fluxes; this study can provide information on the relation between the photon flux and the induced photocapacitance and whether there is a 'threshold' photon flux, above which the phenomenon occurs. Moreover, a comprehensive comparison of anodised aluminium oxide with stoichiometric Al_2O_3 grown with other techniques, such as magnetron sputtering, can shed light on the nature of this unexpected sensitivity to visible light. Additionally, measurements on capacitors based on other anodised metal oxides, such as titanium dioxide (TiO_2), would confirm whether this behaviour is unique to anodised AlO_x or common for different anodised metal oxides.

6.3. The effect on OFET electrical characteristics

As discussed in section 2.4, the importance of the gate insulator in the performance of OFETs has been emphasised in several published studies. In the pursuit of high gate insulator capacitance, a low thickness of the gate dielectric layer (t_{ox}) is generally desirable, since capacitance is inversely proportional to t_{ox}; however, pinholes and quantum tunnelling are common problems which result in high gate leakage currents when the insulator thickness is minimised. Dielectrics with high permittivity (high-k dielectrics) are suggested as a solution for the mitigation of the severe gate-leakage problems experienced in the modern few-nm-node CMOS technology, which transistors conventionally need extremely thin films of SiO_2 [130]. However, while a number of alternative oxides with high k have been demonstrated, silicon dioxide (SiO_2) remains the prevalent and best studied material.

Apart from determining the drain current of an OFET, as eq. (2.2) and eq. (2.3) describe, the permittivity of the gate dielectric also affects drain current indirectly by having an impact on the threshold voltage (V_{th}) of the OFET, as explained below.

The flat band voltage (V_{FB}) can be approximated by:

$$\mathrm{V_{FB}} = \varphi_{MS} - \mathrm{Q_i}/\mathrm{C_{ox}} \tag{6.1}$$

where ϕ_{MS} is the difference between the work function of the semiconductor and that of the gate metal, Q_i is the trap charge at the semiconductor-dielectric interface and C_{ox} is the gate dielectric capacitance.

V_{th} depends on V_{FB} according to [47, 131]:

$$\mathrm{V_{th}} = \mathrm{V_{FB}} - 2\psi_{\mathrm{B}} + \mathrm{qn_0d}/\mathrm{C_{ox}} \tag{6.2}$$

which, by substituting eq. (6.1), writes:

$$\mathrm{V_{th}} = \varphi_{MS} - \mathrm{Q_i}/\mathrm{C_{ox}} - 2\psi_{\mathrm{B}} + \mathrm{qn_0d}/\mathrm{C_{ox}} \tag{6.3}$$

where ψ_B is the bulk potential, q is the elementary charge (~1.602 x 10^{-19} C), n_0 is the number of free carriers at equilibrium and d is the thickness of the semiconductor.

Eq. (6.3) suggests that a high C_{ox} value eliminates the dependence of V_{th} on factors other than the intrinsic ϕ_{MS}, whereas a high Q_i due to the presence of interface traps can alter V_{th}. The aforementioned high-k dielectrics are usually polar compounds, which are more likely to have many surface trap sites and thus, undesirably high Q_i.

A number of approaches to gate insulators with high C_{ox}, yet low Q_i, have been proposed; these include ultrathin films of polymers that get cross-linked after deposition [132], and thin inorganic oxide films with surface modifications to reduce Q_i, either by the application of self-assembled non-polar monolayers [133, 134], or the physical deposition of non-polar polymer interface layers [135]. Recently, Kanbur *et al.* demonstrated a novel approach, by successfully evaporating low-density polyethylene (LDPE), which can operate as either a stand-alone dielectric or a surface treatment of inorganic oxide layers [72], resulting in OFETs with apparently low interfacial trap density.

Most frequently, C_{ox} and Q_i of an OTFT are qualitatively or quantitatively assessed from purely electrical measurements: C_{ox} is usually measured on a separate parallel-plate capacitor sample, as shown in sections 5.1 and 6.2; information on Q_i can be derived indirectly from subthreshold characteristics, in which the trap density at the semiconductor/dielectric interface (N_t) plays an important role; this is described by a variation of eq. (2.6) [136]:

$$S = \frac{kT}{q} \ln 10 \left(1 + \frac{q^2 N_t}{C_{ox}}\right) \quad (6.4)$$

where S is the subthreshold swing (in mV/dec), k is the Boltzmann constant (~1.3806 10^{-23} JK^{-1}), T is the temperature and N_t is the trap density at the semiconductor-dielectric interface. Sometimes, very low N_t can qualitatively be claimed by the observation of ambipolar behaviour in organic semiconductors, as reported by Kanbur *et al.*, and previously by Chua *et al.* [39].

The presence of charge carrier traps has been correlated with the sensitivity of organic semiconductor devices to light, however the published work on this field of study remains limited. A brief review of published light-sensitivity studies on OFETs follows.

Salleo *et al.* published an early study on the use of illumination as a means of OFET recovery from gate-bias stress [137]. In this study, polyfluorene (F8T2) OFETs with various gate dielectric configurations, based on either an oxide (SiO_2) or a polymer (parylene) dielectric, were used; the SiO_2 oxides were treated with a selection of self-assembled monolayers (SAMs). The devices were first electrically stressed by the application of gate bias and then, their recovery between dark and illuminated conditions was studied; V_{th} was found to recover quickly under illumination. The authors have concluded that the light-induced recovery is irrelevant of the choice of both the dielectric and the dielectric/treatment used; instead, it is suggested that this behaviour is due to the absorption of the semiconductor itself. Moreover, they have suggested that the affected charge traps were located within the semiconductor film and in close proximity to the dielectric, but not at the semiconductor/dielectric interface or within the dielectric itself; they assume that visible light should not affect the traps in the dielectric due to its high bandgap and that if the traps had been located at the interface, the effect of light would have been weaker for the wavelengths absorbed by the semiconductor. All these facts and assumptions constitute key differences between this published work and the findings of the study presented here. Especially, the discovery of capacitance changes under illumination (photocapacitance), discussed in section 6.2.2, shows that even high bandgap materials can be affected by visible light.

Furthermore, a study of the light-induced trap-release in pentacene films was recently published by Smieska *et al.* [138]. In this work, pentacene films with deliberately introduced species that induce charge carrier trapping (trap-precursors) were studied using electric force microscopy; light-wavelength-resolved measurements revealed that the charge trap release rate is higher when the spectrum of the incident light overlaps with the absorption spectra of either the pentacene film or the introduced trap-inducing species.

Feng *et al.* recently demonstrated pentacene OFETs with tunable V_{th}, which incorporate a poly(9,9-dioctylfluorene) (PFO) conjugated polymer film as gate oxide surface treatment [139]. In this study, the polymer film was intentionally employed to enhance charge-trapping and therefore make the threshold voltage more susceptible to illumination. Substantial V_{th} changes towards a normally-on behaviour were observed, whereas hole mobility showed no dependence on illumination.

Very recently, Yang et *al.* demonstrated the detection of either left- or right-handed circularly polarised light using OFETs based on the two different enantiomers of helicene organic

semiconductor; a left-handed (-) and a right-handed (+) one, respectively [140]. The matching of the chirality of the semiconductor with the respective polarisation incident light manifested itself as a change in the subthreshold characteristics of the OFET under test.

In another study, Shang *et al.* also suggested that light-induced V_{th} changes are independent of the dielectric used [141]. However, both employed oxides, i.e. SiO_2 and Al_2O_3, had been treated with an octadecyltrichlorosilane (OTS) SAM prior to the deposition of the semiconductor; therefore, it is very likely that the interfacial trap densities were very similar despite the different underlying oxide.

It is worth mentioning that none of the aforementioned studies considers the phenomenon of *photocapacitance*, i.e. a change of the bulk capacitance of the gate dielectric (C_i) under illumination with photon energies well below the bandgap of the insulator; as mentioned above, Salleo *et al.* even suggested that visible light should have no effect on a material with such a large bandgap. However, the results from the photocapacitance study, discussed in section 6.2, show that AlO_x is highly susceptible to light. This fact adds another important factor into consideration when the light stability of complex devices such as OFETs is under the spotlight.

This section presents the results from the electrical characterisation of OFETs under controlled light-exposure. In contrast to the work demonstrated by Shang *et al.* [141], the study presented here, compares and contrasts pentacene and PDI8-CN_2 OFETs based on the same underlying oxide (AlO_x), but modified with different surface treatments: either an octadecyltrichlorosilane (OTS) self-assembled monolayer (SAM) or an evaporated low-density polyethylene (LDPE) layer. Real-time multiparametric measurements disentangled the trends of V_{th} and μ under illumination, which allows for drawing safe conclusions on the importance of the gate dielectric treatment.

6.3.1. Device preparation

All substrates for the OFETs under test were taken from a silicon wafer with an 100-nm-thick silicon dioxide layer. The substrates were cleaned in an ultrasonic bath twice, using an alkaline detergent with deionized water and IPA, respectively. The final cleaning process was an UV-ozone treatment. More details on substrate preparation are given in section 2.2.4.

Following the common bottom-gate device architecture, an 100-nm-thick layer of aluminium was thermally evaporated through shadow masks at a deposition rate of 10^{-2} nm/s under a high vacuum of 5 x 10^{-7} Torr. The patterned aluminium layer was electrochemically oxidised in a citric acid solution by the application of a constant current of 0.95 mA at a voltage limit of 5 V; the current application time was 75 seconds. More information on aluminium oxide (AlO_x) formation is given in section 2.4.2.

On the first group of samples, an OTS SAM was deposited by immersion of the samples into a cyclohexane solution of OTS for 10 minutes; this process was carried out in a nitrogen glove box. Further details on OTS treatment of oxides are given in section 2.4.3. Hereafter, these samples will be referred to as AlO_x-OTS.

On the second group of samples, a 25-nm-thick layer of low-density polyethylene (LDPE) was thermally evaporated at a low temperature of 300°C-400°C under high vacuum. The deposition rate was in the range of 10^{-2} nm/s. These samples were annealed at 95°C for 20 minutes in

vacuum. Details on LDPE deposition are given in section 2.4.4. Hereafter, this group of samples will be referred to as AlO_x-LDPE.

On sets of devices, 50-nm-thick layers of pentacene and PDI8-CN2 were deposited in high vacuum. The deposition rate was in the range of 5 x 10^{-2} nm/s for both materials. Both of them were used as purchased, without further purification. The substrates were not additionally heated during the evaporation.

Finally, the source and drain top electrodes were deposited by thermal evaporation of gold through shadow masks. The deposition rate was 7 x 10^{-2} nm/s under a high vacuum of 5 x 10^{-7} Torr. The resulting OFET channels had a length of 10 µm and width of 2 mm. After fabrication, the devices were stored in a dark vacuum oven, thermostatically-controlled at 40 °C.

6.3.2. Test methodology

The measurements were taken in ambient air in an air-conditioned laboratory at a stable room temperature of 23 °C. The samples under test were contacted by three *Cascade-Microtech PH100* probe positioners with tungsten needles. The needles were electrically connected to a switch box which could route the source, drain and gate signals to either a set of Keithley 2400 units for the extraction of conventional current-voltage characteristics, as discussed in section 3.3, or the automated real-time characterisation system, described in Chapter 4.

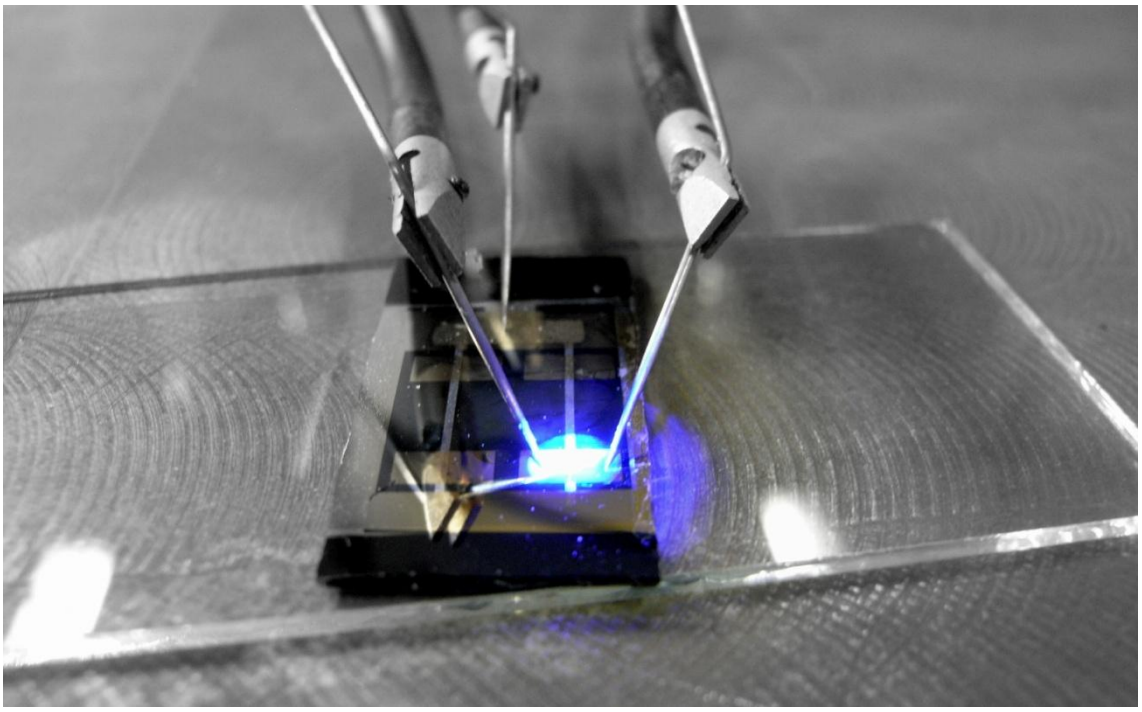

Figure 6-10 – A photograph of a substrate with 4 OFETs placed in the light exposure test rig. A focused beam of blue light illuminates the channel area of the bottom-right device. Substrate dimensions: 12 mm x 24 mm.

For the automated AC measurements, the applied drive was a zero-offset sinusoidal signal with a frequency of 6 Hz and a 3 V (peak) amplitude. Sets of eleven consecutive cycles of the input and output signals were simultaneously sampled every five seconds, and a median filter was applied to all calculated parameters of these sets. More details on the automated electrical characterisation are given in section 4.3.

As a control experiment, an integrated circuit temperature sensor (LM35) was tested in lieu of the samples; the sensor was illuminated by the same focused beams and under the same

conditions as above. For all calibrated light sources, a rapid minor temperature increase of 0.2 °C ± 1% above room temperature was measured. The sensor quickly recovered to room temperature when the illumination was ceased.

6.3.3. Results and discussion

6.3.3.1. *Standard I-V characteristics*

The optical test rig, described in sections 6.1.2 and 6.1.3 , was used for the investigation of the effects of visible light illumination on OFETs. The conventional transfer curves of both the hole-transporting pentacene and the electron-transporting PDI8-CN_2, and for both dielectric combinations are shown in Figure 6-11 to Figure 6-14. The measurements were taken in the dark and under light illumination by the blue LED.

Interestingly, despite the fundamental differences between the two semiconductors, very similar changes in the electrical characteristics of these OFETs were found; both pentacene and PDI8-CN_2 devices with OTS-treated dielectric were found to be more susceptible to light than their LDPE-treated counterparts. In detail, threshold voltage (V_{th}) shifted towards a normally-on (depletion-mode) behaviour in all cases. OTS-treated devices exhibited substantial changes under light with a V_{th} change of +1.05 V for pentacene and -1.15 V for PDI8-CN_2. LDPE-coated devices appeared significantly more stable, with a V_{th} change of +0.3 V for pentacene and -0.35 V for PDI8-CN_2. This finding confirms the dependence of light sensitivity on the employed dielectric treatment.

It is worth noting that while LDPE-treated PDI8-CN_2 OFETs are normally-off (enhancement-mode) devices even in the dark, in the case of OTS-treated dielectric, light exposure caused a transition from enhancement-mode operation to depletion-mode (normally-on) operation as V_{th} became negative. Similar behaviour has been reported by Feng *et al.* for pentacene OFETs with PFO dielectric treatment [139].

In the case of pentacene devices, a safe assumption that the changes are not due to photoconductivity can be made. This is backed partly by the absence of any off-current change under illumination, but mainly by the fact that the absorption of the semiconducting layer is very low in the blue LED emission spectrum, as it can be seen from the spectral analysis in Figure 6-2.

The effects on the calculated mobility were very small; although these changes are not so pronounced in these DC measurements, they constitute a noteworthy behaviour in the case of prolonged and continuous real-time AC measurements, as discussed below.

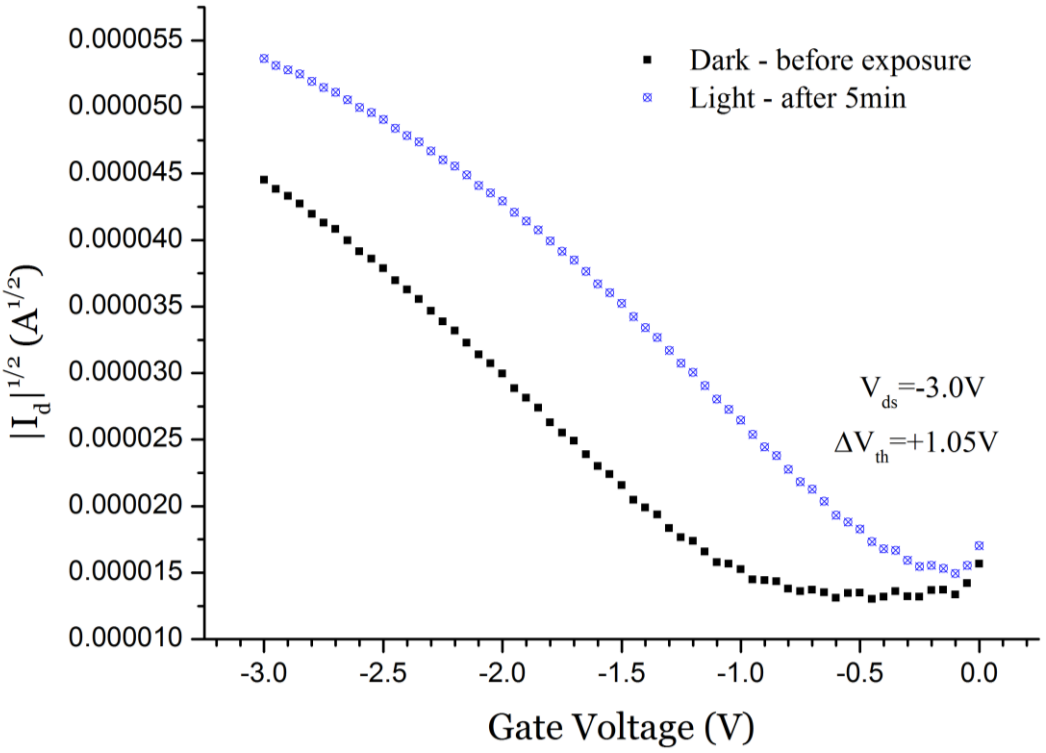

Figure 6-11 – Transfer characteristics of a pentacene OFET built on an AlO_x-OTS dielectric in the dark (black rectangles) and under a 5-min-long period of blue light illumination (light blue rectangles).

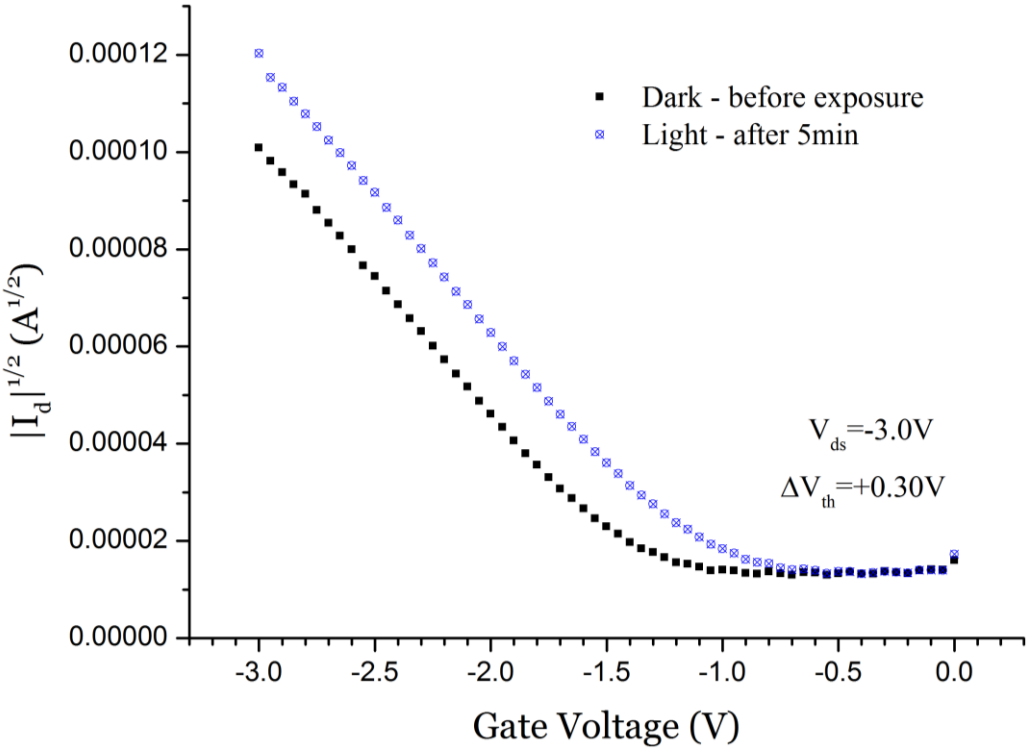

Figure 6-12 – Transfer characteristics of a pentacene OFET built on an AlO_x-LDPE dielectric in the dark (black rectangles) and under a 5-min-long period of blue light illumination (light blue rectangles).

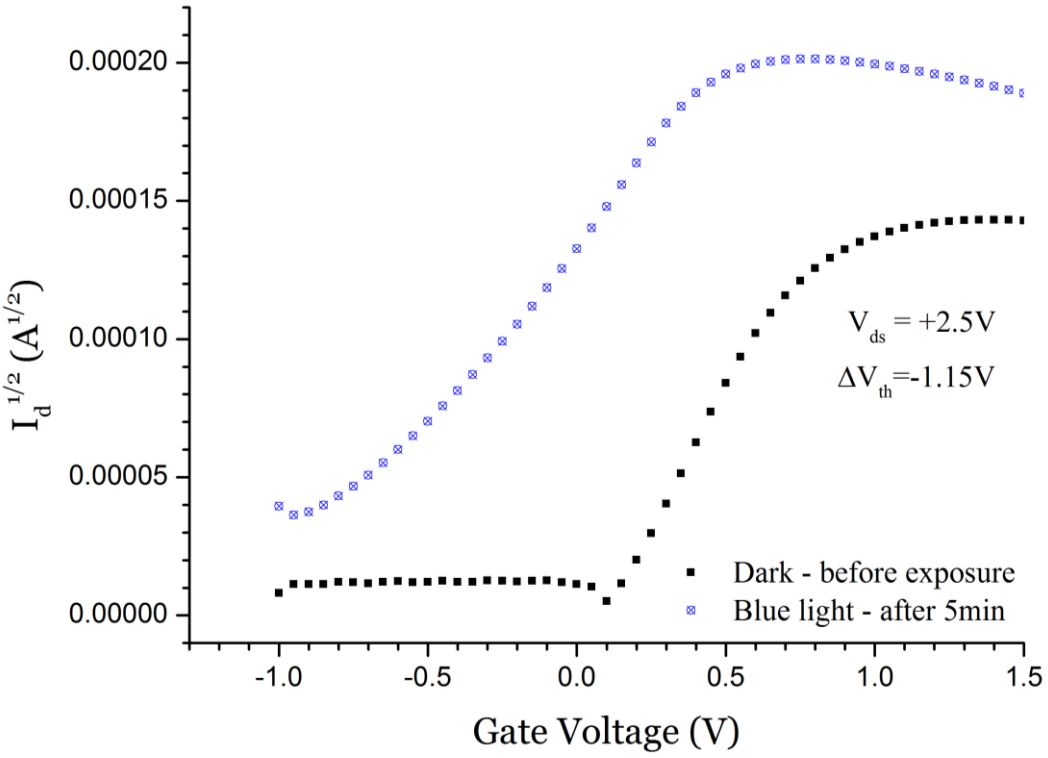

Figure 6-13 – Transfer characteristics of a PDI8-CN_2 OFET built on an AlO_x-OTS dielectric in the dark (black rectangles) and under a 5-min-long period of blue light illumination (light blue rectangles).

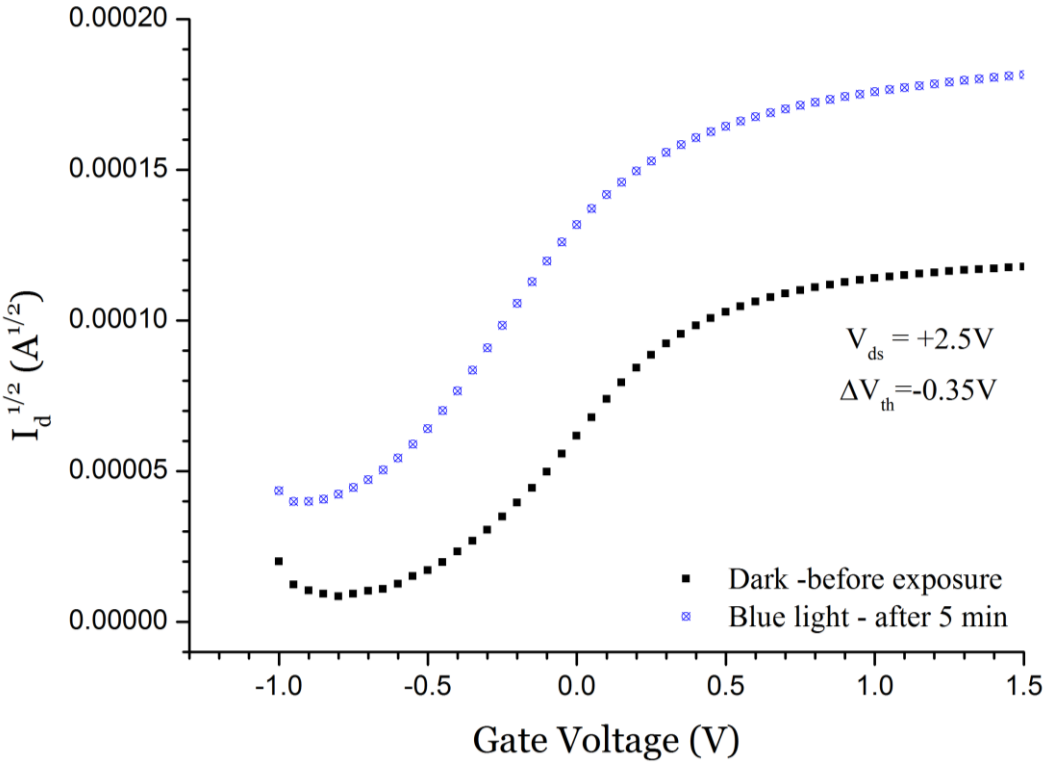

Figure 6-14 – Transfer characteristics of a PDI8-CN_2 OFET built on an AlO_x-LDPE dielectric in the dark (black rectangles) and under a 5-min-long period of blue light illumination (light blue rectangles).

6.3.3.2. *Automated real-time AC measurement results*

The pentacene OFETs with different gate dielectric combinations were further tested with the automated real-time multiparametric characterisation system. The advantages of this characterisation method are versatile; apart from its capability of calculating multiple independent parameters in real time, the symmetrical AC drive can eliminate the gate-bias-stress-related V_{th} shifts [104, 142]; moreover, such driving conditions resemble a more realistic OFET operation cycle with alternating on and off periods.

The four calibrated LEDs were used in this optical test rig to shine light on the channel areas of the devices under test. The same test pattern was applied to both devices under test. The devices were initially characterised in the dark and consequently illuminated by red, yellow, green and blue light for 10-minute-long exposure periods with interleaving recovery periods in the dark.

Figure 6-15 to Figure 6-18 show the effects of light exposure on the saturated drain current, the threshold voltage (V_{th}) and the field-effect mobility (μ) of the two samples. All four different wavelength ranges induced a drain current increase on both devices, regardless of their dielectric surface treatment. However, the magnitude of the effects and the mechanisms which induced these changes exhibited a dependence on the wavelength of the light and the dielectric surface treatment, as discussed below. Moreover, the incident photon energy was found to be an important factor, with blue light illumination resulting in the most remarkable changes. This finding comes in contrast to the photocapacitance results, discussed in section 6.2.2, which showed that the changes in capacitance were independent of the wavelength of the incident light. Therefore, the generally observed increase in drain current under illumination can, at best, only partially be explained by the photo-enhancement of the bulk capacitance of the dielectric itself.

Moreover, Figure 6-2 shows that the emission spectra of the red and yellow LEDs strongly overlap with the pentacene absorption band, the spectrum of the green LED has only a small overlap, and that of the blue LED does not overlap at all; considering these spectra, the photoconductivity of the semiconductor or the release of traps within the bulk of the semiconductor, as suggested in other studies [137, 138], can safely be neglected, as this would lead to stronger, not weaker as observed, current enhancement for the absorbed wavelengths.

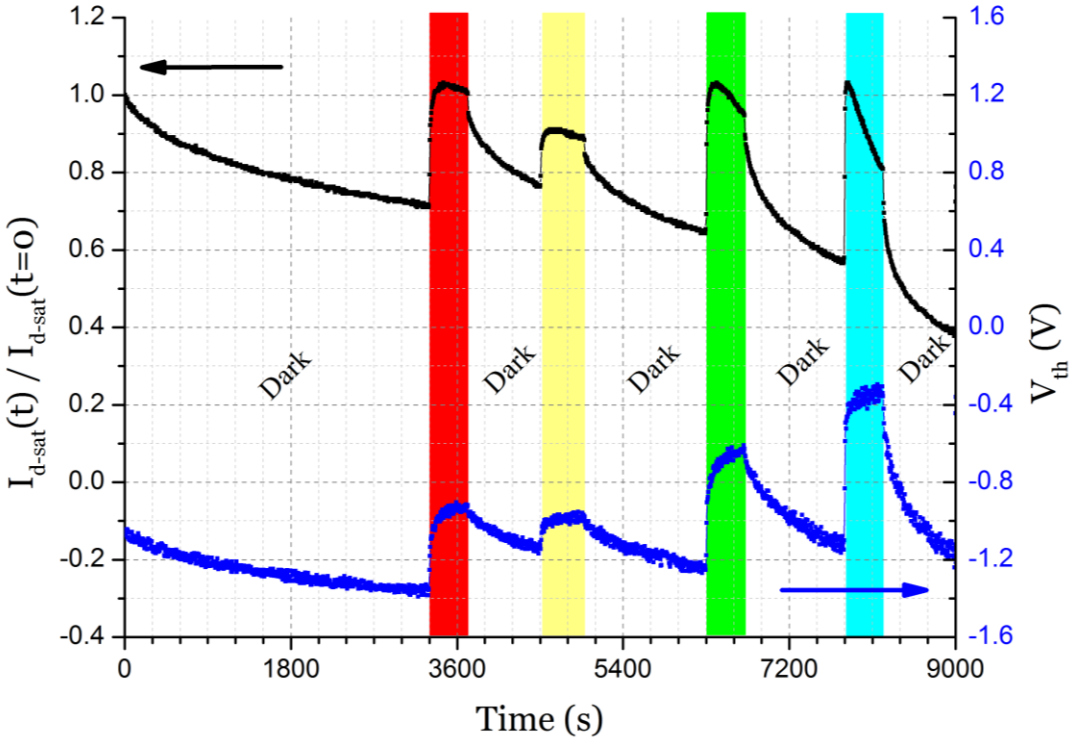

Figure 6-15 – Time-resolved measurements of drain current (black data points) and V_{th} (blue data points) of a pentacene OFET based on AlO_x-OTS dielectric layers. The colour-shaded regions indicate the periods of illumination of the device with light of the respective colour (red, yellow, green and blue).

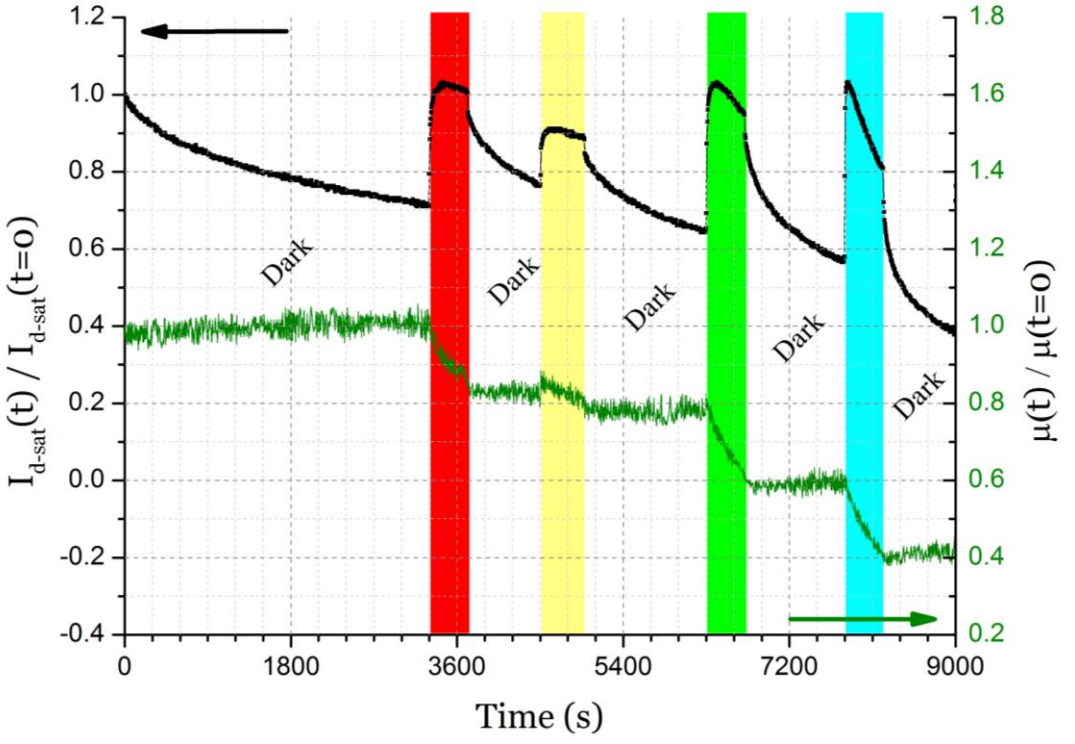

Figure 6-16 – Time-resolved measurements of drain current (black data points) and μ_{FE} (green data points) of a pentacene OFET based on AlO_x-OTS dielectric layers. The colour-shaded regions indicate the periods of illumination of the device with light of the respective colour (red, yellow, green and blue).

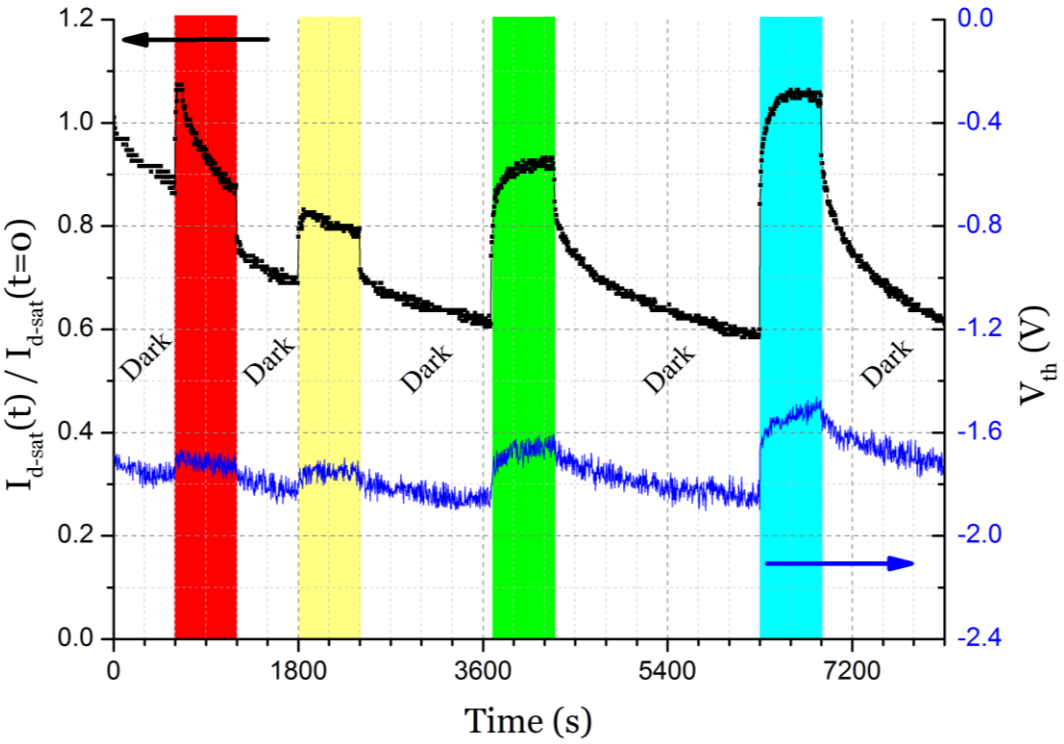

Figure 6-17 – Time-resolved measurements of drain current (black data points) and μ_{FE} (green data points) of a pentacene OFET based on AlO_x-LDPE dielectric layers. The colour-shaded regions indicate the periods of illumination of the device with light of the respective colour (red, yellow, green and blue).

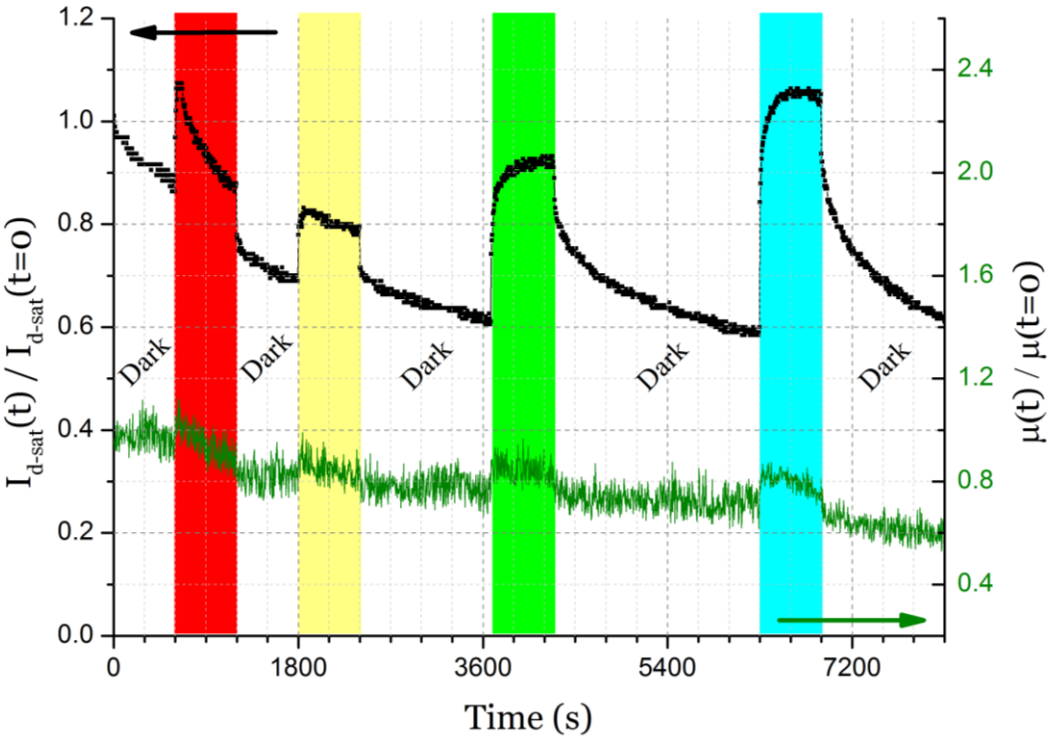

Figure 6-18 – Time-resolved measurements of drain current (black data points) and μ_{FE} (green data points) of a pentacene OFET based on AlO_x-LDPE dielectric layers. The colour-shaded regions indicate the periods of illumination of the device with light of the respective colour (red, yellow, green and blue).

The analysis of the independent OFET parameters can shed more light on the actual effects induced by the illumination. In all cases, threshold voltage (V_{th}) was promptly affected by light,

showing an initial steep positive shift, i.e. towards a normally-on behaviour. This was followed by a further slower increase which resembled an exponential change. The OFET with OTS-coated dielectric was found to be more susceptible; it showed a substantial V_{th} change from -1.4 V, in the dark prior to the first illumination, to -0.35 V under blue light. The LDPE-coated device was remarkably more stable, exhibiting a maximum change from -1.9 V to - 1.5 V under blue light.

Recalling eq. (6.7), it is clear that V_{th} can be significantly affected by the density of traps at the semiconductor-dielectric interface. Also, as discussed in the introduction above, several studies have correlated the illumination of semiconductor devices with trap density reduction; this phenomenon is also referred to as trap-release or trap-filling. Considering these facts along with the trap density analysis, given in section 5.2.2.3, the much higher interfacial trap density of the OTS-treated device, as compared to the LDPE-treated one, can explain its higher susceptibility to light exposure.

Furthermore, the stronger effects induced by the more energetic photons of blue light, as compared to light of longer wavelengths, can be explained by the fact that the release of charge carriers from deep traps requires photons of high energy. An additional explanation can be sought in the spectral analysis, illustrated in Figure 6-2; as discussed above, the absorption of pentacene is stronger in the yellow and red wavelength range, which actually filters the incident photons with the respective energy. It can then be assumed that a portion of the photons emitted by the yellow and red LEDs get absorbed by the semiconductor film and never reach the semiconductor-dielectric interface. However, the actual impact of this attenuation cannot be easily quantified.

It is worth mentioning that the employed V_{th} evaluation algorithm, which is described in section 4.2.4.1, is independent of the magnitude of C_i. Therefore, any light-induced capacitance changes did not compromise the accuracy the calculated results presented here.

The calculated mobility trends differ significantly; the LDPE-coated device showed small increases in mobility at the onset of all illumination periods; these initial changes were followed by slow decreases during and after each illumination. Conversely, the mobility of the AlO_x-OTS device exhibited negligible initial increases followed by steep mobility drops. In this case, the mobility reached a new plateau every time the illumination was ceased and did not recover over the course of each following recovery period in the dark.

A noteworthy remark is that, in contrast to the V_{th} calculation method, mobility is extracted by an algorithm which takes account of the gate dielectric capacitance per unit area (C_i), as described by eq. (4.10). According to this equation, a possible increase in capacitance under illumination can be misinterpreted as a mobility increase since C_i is taken as a constant. Hence, the observed mobility drop under illumination is certainly not an evaluation artefact; contrarily, the calculated μ drop might have slightly been mitigated by a possible light-induced capacitance increase.

Notably, in a very different comparative study between OFETs with bare and SAM-treated alumina dielectrics, Kalb *et al.* have shown that the dependence of mobility on gate bias was related to the surface treatment [68]; although on bare alumina, mobility increased with increasing gate voltage, interestingly, on the SAM-treated alumina, μ showed an initial increase followed by a decrease. This behaviour resembles the behaviour of the OTS-treated

devices under illumination, discussed above; this apparently irrelevant similarity between gate-bias- and illumination-induced changes is discussed and given an explanation in the following section.

6.3.3.3. *Mobility dependence on illumination*

The observed reduction of field-effect mobility under illumination and even more, the dependence of this reduction on the gate dielectric surface treatment cannot be given an explicit explanation. However, there are reports and suggested models of the mobility degradation in OFETs under high electric fields. A closer look at the physics which govern these mobility degradation mechanisms can provide an explanation for the calculated mobility trends, discussed in the previous section.

The effective mobility (μ_{eff}) of carriers of MOSFETs depends on the gate-bias induced field in the channel area. As discussed in 1.3.4.1, the charge carriers are susceptible to various mobility degradation mechanisms, such as Coulomb scattering at the semiconductor-dielectric interface, phonon scattering and surface roughness scattering. In inorganic MOSFETs, a simplified empirical expression of μ_{eff} is given by [33]:

$$\mu_{\mathrm{eff}} = \frac{\mu_0}{1 + \theta \mathrm{E}_{\mathrm{eff}}} \tag{6.5}$$

where θ is an empirical parameter and the effective field E_{eff} can be expressed as [143]:

$$\mathrm{E}_{\mathrm{eff}} = \frac{\mathrm{Q}_{\mathrm{dep}} + \mathrm{nQ}_{\mathrm{inv}}}{\epsilon_{\mathrm{Si}}} \tag{6.6}$$

Where Q_{dep} is the charge per unit area in the depletion layer, Q_{inv} is the charge per unit area in the inversion layer, ε_{Si} is the permittivity of silicon, n is a constant which typical values for a (100) lattice are ½ for electrons and ⅓ for holes, but can vary significantly.

Both charge factors are proportional to gate dielectric capacitance, as described by [144]:

$$\mathrm{Q}_{\mathrm{inv}} = \mathrm{C}_{\mathrm{ox}}\left(\mathrm{V}_{\mathrm{gs}} - \mathrm{V}_{\mathrm{th}}\right) \tag{6.7}$$

and

$$\mathrm{Q}_{\mathrm{dep}} = \mathrm{C}_{\mathrm{ox}}(\mathrm{V}_{\mathrm{th}} - \mathrm{V}_{\mathrm{FB}} - \varphi_{\mathrm{s}}) \tag{6.8}$$

where C_{ox} is the capacitance of the gate dielectric, V_{gs} is the gate bias, V_{th} is the threshold voltage, V_{FB} is the flat band voltage and ϕ_s is the surface potential.

More recently, Mottaghi and Horowitz developed a model for the charge transport in vapour-deposited molecular films such as pentacene [145]. In this model, the stacked monolayers of pentacene are considered as parallel conductors, in which the charge is equally distributed along each layer. According to this approximation, the application of a high gate-induced field results in the accumulation of charge within the lowest, i.e. adjacent to the dielectric interface, monolayer of pentacene which exhibits relatively lower mobility due to the presence of the aforementioned scattering factors. This model assumes V_{th}=0 and gives the following expression of the total charge in the semiconductor film:

$$qn_{tot} = q\sum_{1}^{j} n_i = C_i(V_g - V_0) \quad (6.9)$$

where n_{tot} is the total number of charge carriers, j is the farthest monolayer from the insulator interface, n_i is the number of charge carriers in each monolayer and V_0 is the potential at the insulator-semiconductor interface.

The aforementioned models have been developed for the study of the effect of gate bias on the mobility degradation in both inorganic and organic FETs; all of them assume a constant value of C_i. However, in this study, the photocapacitance measurements presented in section 6.2 revealed that C_i is light-dependent. Moreover, in the measurements presented in this section, V_g was a low-frequency zero-offset symmetric time-varying signal (sine) which equally charged and discharged the gate capacitor, effectively eliminating the accumulation of charge over a full sine period.

From eq. (6.5) to eq. (6.8), another expression of μ_{eff} can be derived:

$$\mu_{eff} = \frac{\mu_0}{1 + \epsilon_{Si}^{-1}\theta E_{eff} C_{ox}(nV_{gs} - \varphi_s - V_{FB} + (1-n)V_{th})} \quad (6.10)$$

According to eq. (6.10) and assuming that n<1, the reduction of the modulus of V_{th}, which was observed when the OFET under test was illuminated, can potentially result in an increase of mobility. Indeed, for the first seconds of illumination mobility showed a small but noticeable increase. However, according to the same equation, the substantial increase in the capacitance of the AlO_x dielectric apparently prevailed after some seconds and the mobility dropped until the illumination was ceased. In addition, the more pronounced mobility degradation in the case of OTS-treated surface can be attributed to the higher density of interfacial traps in the case of the OTS-treated oxide as compared to the LDPE-treated one, as discussed in section 5.2.2.3.

6.3.4. Conclusion

The work presented in this section suggests that the light stability of organic field-effect transistors (OFET) can be controlled by the application of an appropriate surface treatment on their oxide gate dielectric. Environmental stability is of utmost importance for many OFET applications; for instance, when OFETs are used as sensing transducers, the sensitivity of any OFET parameter to light can be misinterpreted as a sensing response.

Backed by the photocapacitance measurements, discussed in section 6.2.2, this study focused on a comparison between two different surface treatments, i.e. an OTS SAM and an evaporated LDPE layer, of a high-k inorganic oxide insulator (AlO_x);

Light exposure induced a drain current increase in these AlO_x-based OFETs. The surface treatment of the oxide dielectric was found to play a key role in the susceptibility of these devices to light. Both p-type (pentacene) and n-type (PDI8-CN_2) OFETs with OTS-treated AlO_x exhibited major threshold voltage changes under illumination, whereas the LDPE-treated ones were slightly affected. Thus, it can be safely assumed that these phenomena are more likely to be related to trap releasing mechanisms at the semiconductor-dielectric interface.

Moreover, in pentacene devices, a comparison of the OFET photosensitivity for particular wavelengths to the absorption spectrum of the semiconductor itself disproved that the measured drain current increase is due to either photoconductivity or trap release within the semiconductor; this assumption is also backed by the insensitivity of the measured off-current to illumination.

Conversely, the light effects were found to be stronger for shorter wavelengths, which are not absorbed by the semiconductor film. This phenomenon can be attributed to the fact that the higher energy of these photons can release charge carrier from deep traps. Moreover, the semiconductor film effectively acts as filter for the incident low-energy photons; i.e. a portion of them never reaches the semiconductor-dielectric interface; however, the contribution of this mechanism cannot be easily quantified.

The pentacene OFETs were further measured with the real-time multiparametric system, described in Chapter 4. The data analysis provided a deeper understanding of the induced changes in a functional OFET under illumination by disentangling rapid mobility and threshold voltage changes in constantly running devices under an AC drive; this straightforward separation of individual parameters was found to work as a good proof-of-concept example for this characterisation system.

Using this system under illumination, the threshold voltage of all devices showed a positive shift, i.e. towards a normally-on behaviour; the changes for the OTS-treated OFETs were more pronounced and induced a rapid initial increase in drain current. However, the same devices suffered from extensive mobility degradation under prolonged illumination while operating under a continuous AC drive. The mobility dependence on illumination was found to be rather small for their LDPE-treated counterparts. A theoretical approach to explaining the possible mobility degradation mechanisms is given in section 6.3.3.3.

Further work for the generalisation of these observations is advisable; in particular, the use of other semiconductor/dielectric combinations is suggested, especially an all polymeric dielectric, which is very likely to yield the best results in terms of light stability. Motivated by these findings, pentacene devices with LDPE (only) dielectric were successfully fabricated, as discussed in section 5.2.3; however, the indications of an ambipolar behaviour complicated their analysis under illumination and consequently, they were finally excluded from this comparative study.

Finally, recalling the conclusions from section 6.2.3, the observed changes in the dielectric constant of anodised aluminium oxide under illumination constitute a remarkable finding; although this photocapacitance had a small contribution in the photosensitivity of the investigated OFETs, it remains a very interesting topic for future investigation.

6.4. Photosensitivity of tetracene devices

The electrical characteristics of tetracene devices are discussed in section 5.4; as mentioned in that section, tetracene OFETs showed a very unstable electrical behaviour while operating in ambient conditions. Nevertheless, light exposure measurements yielded interesting results, which are presented in this section; an OFET with AlO_x/OTS gate dielectric was exposed to white light, while another SiO_2-gated OFET with an unconnected gate electrode was found to operate as a good *metal-semiconductor-metal (MSM) photodetector*. A brief literature review of tetracene optoelectronic applications and MSM photodetectors follows.

First, the photosensitivity of tetracene OFETs has previously been demonstrated. Choi et *al.* have published a comparative study between pentacene and tetracene OFETs exposed to light [122]; in that paper, the photoresponse (I_{light}/I_{dark}) of tetracene OFETs was found to be much higher than that of their pentacene counterparts.

Second, the MSM photodetectors are planar devices with simple structure, consisting of two Schottky (metal-semiconductor) contacts of the same type; they are usually made by deposition of two metal electrodes on top of a semiconductor. The concept of inorganic MSM photodetectors has been adopted for specialised commercial applications, such as high-speed optical-fibre communications; devices based on III-V semiconductors, such as GaAs, have exhibited remarkable characteristics which outperform the conventional photodiodes in terms of response time and low-dark-current capability [146, 147].

Third, tetracene has been employed in the fabrication of heterojunction photodiodes; for instance, Campbell and Crone recently demonstrated a photodiode based on a tetracene/C_{60} heterojunction separated by a thin tunnel barrier made on lithium fluoride (LiF) [148]. However, as of October 2013, there is no published evidence of functional MSM photodetectors made of tetracene or even any other organic semiconductor.

6.4.1. Test methodology

Two devices from different batches were used in the tests presented in this section. The device fabrication procedure for the AlO_x OFET is described in section 5.4.1.1. For the tests on the MSM photodetector, Si substrates with an 100-nm-thick thermal oxide were cleaned with an alkaline solution, IPA and a final UV-ozone treatment. More details on substrate preparation are given in section 2.2.4. The substrates were immersed into a cyclohexane solution of OTS (10 mg/mL) for 60 minutes; details on OTS-treatment of oxides are given in section 2.4.3. Tetracene was thermally evaporated in high vacuum with a pressure of 9×10^{-7} Torr; the deposition rate varied from 0.03 to 0.06 nm/s and the final thickness of the deposited film was 50 nm. Finally, 50-nm-thick top gold electrodes were evaporated through shadow masks; the deposition rate was roughly 0.05 nm/s and the pressure in the dome varied from 4.5×10^{-7} to 4.5×10^{-6} Torr during the evaporation.

The I-V converter system, described in Chapter 4, was used for the electrical characterisation of these devices. The devices were contacted by three *Cascade-Microtech PH100* probe positioners with tungsten needles. The applied drive was a zero-offset sinusoidal signal with an amplitude of 3 V (peak) and a frequency of 6 Hz for the OFET, and 2.5 Hz for the MSM measurements.

Tetracene was also thermally evaporated and deposited onto a fused quartz substrate; a 50-nm-thick film was finally deposited. The absorption spectrum of this film was measured by a spectrometer (*Andor Shamrock 303i)*; the results are shown in Figure 6-19.

Two different light sources were used in these light exposure tests. For the OFET measurements, a common desk lamp with a tungsten-halogen bulb with a power rating of 20 W and a reflector was placed above the device under test; the distance between the bulb and the surface of the sample was roughly 15 cm. For the tests on the MSM photodetector, the blue and green LEDs, discussed in section 6.1.2, were place at a distance of roughly 20 cm above the sample; the LEDs were electrically connected in parallel and powered by a constant current of 30 mA supplied by a Keithley 2400 unit. No focusing lenses were used in both cases.

It is worth mentioning that the work presented here is mainly a qualitative study; neither wavelength- nor intensity-resolved light sensitivity measurements were conducted. The devices were measured in two different states; in the dark and under illumination.

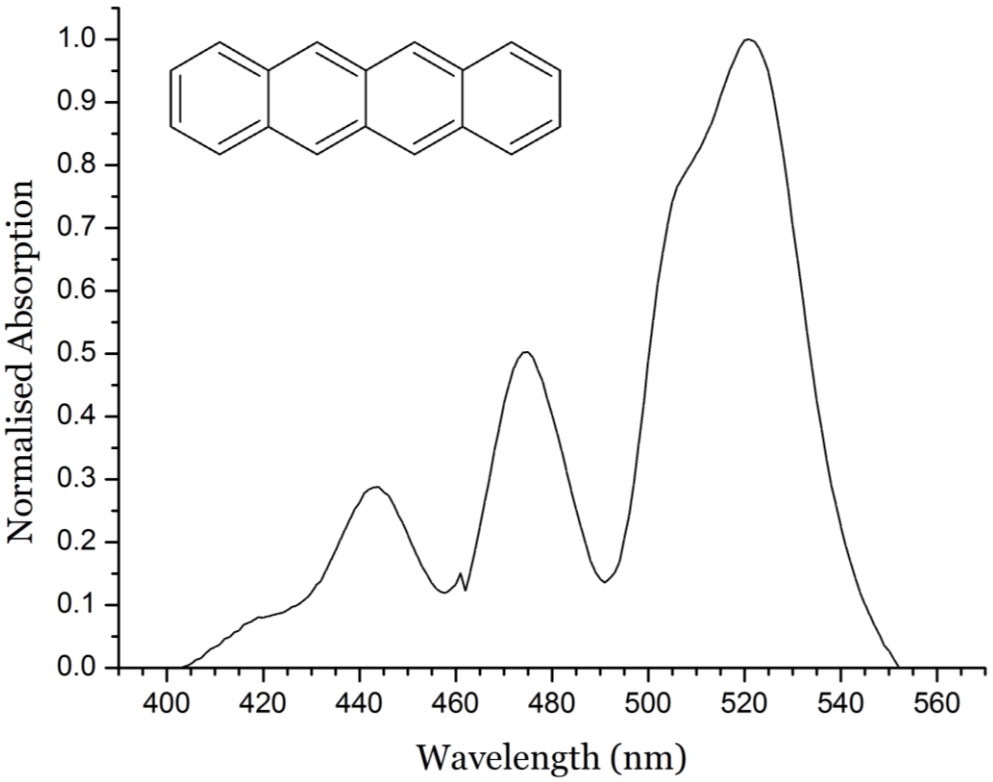

Figure 6-19 – The absorption spectrum of a 50-nm-thick tetracene film

6.4.2. Results and discussion

6.4.2.1. *Illumination effects on tetracene OFETs*

A tetracene OFET with AlO_x/OTS gate dielectric was measured in the dark and under white light illumination from the common tungsten-halogen bulb. The oscilloscope data taken from the I-V converter system, described in Chapter 4, are shown in Figure 6-20. The saturated drain current ($I_{d,sat}$) for $V_{ds} = V_{gs} = 3V$ was 23 μA. Under illumination, the $I_{d,sat}$ tripled, taking a value of ~71 μA. As a reference, Choi *et al.* have previously reported a photoresponse (I_{light}/I_{dark}) of 35%-50% for a tetracene OFET operating in the saturation region and being illuminated by blue light (450 nm) with a power density of ~0.1 mW/cm^2 [122]; however, the differences in the drive conditions, light spectrum and power density do not allow for a valid comparison.

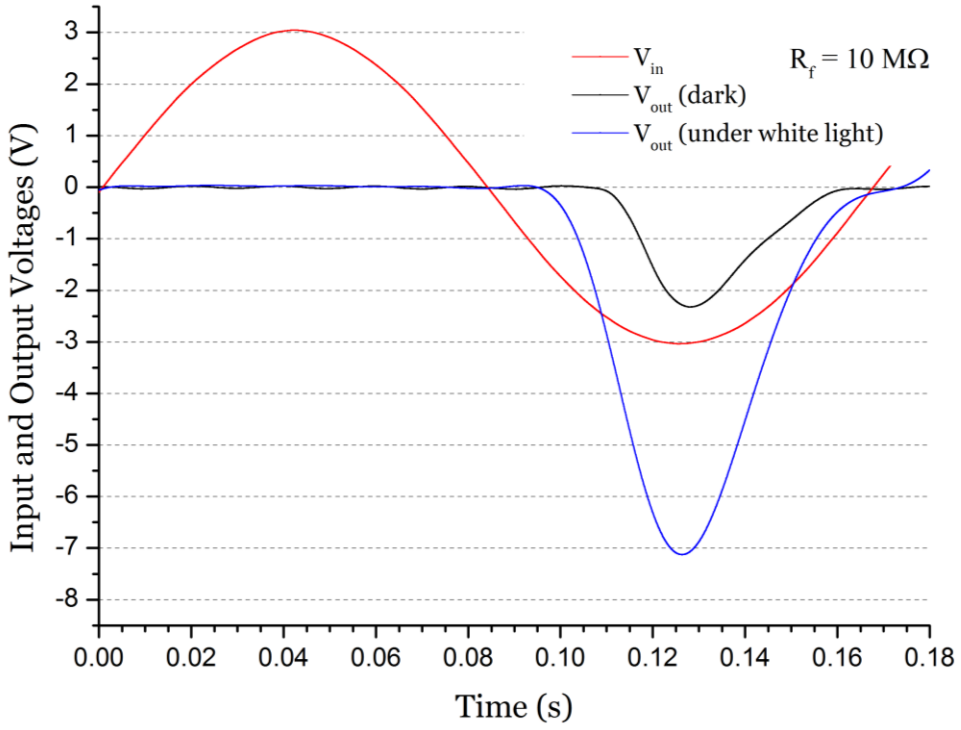

Figure 6-20 – An oscilloscope screenshot from the I-V converter system: drive voltage (red curve), output voltage in the dark (black curve) and output voltage under white light illumination (blue curve).

Both threshold voltage (V_{th}) and mobility (μ) were affected; V_{th} shifted towards a normally-on behaviour, from -2.5 V to -1.8 V, while μ decreased by 21.4%. The positive shift of V_{th} can partly, if not exclusively, be attributed to the trap-releasing mechanisms at the semiconductor-dielectric interface, as discussed in detail in section 6.3. The mobility degradation can also be explained by the theoretical approach given in section 6.3.3.3.

However, considering the absorption spectrum of tetracene, as shown in Figure 6-19, and the fact that tungsten-halogen incandescent lamps have a wide and continuous emission spectrum which covers the entire absorption spectrum of tetracene [149], it can be assumed that these phenomena can also be attributed to the release of trapped charge carriers in the bulk of the semiconductor. This assumption is backed by the findings from the tests on simple two-contact devices, discussed in the following section.

More interestingly, the reduction of the trap density in the bulk of the semiconductor can be confirmed using the novel hysteresis quantification method introduced in section 4.2.5; as mentioned in that section, hysteresis is mainly affected by the presence of traps in the bulk of the semiconductor. Figure 6-21 illustrates a comparison of the calculated hysteresis for the same device between dark and illuminated conditions, the curves are the same as the ones shown in Figure 6-20. These calculations come in good agreement with the light-induced trap-releasing assumptions made above; hysteresis showed a substantial change from +10.2% in the dark down to +3.7% under illumination. This decrease in hysteresis constitutes a strong indication of a decrease in the density of traps.

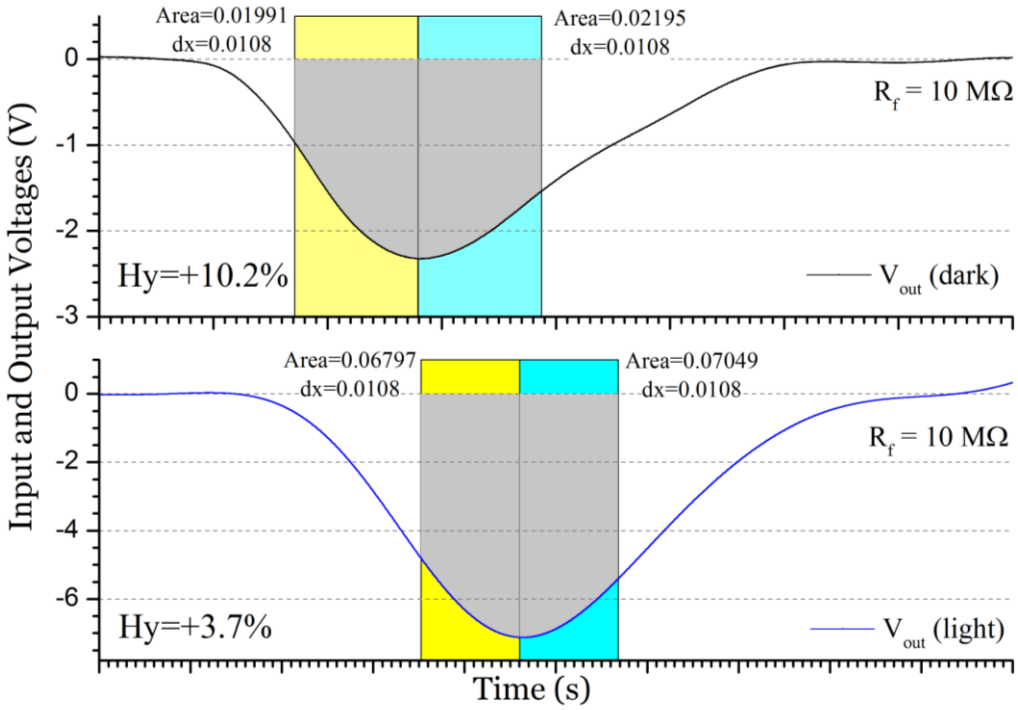

Figure 6-21 – A comparison of the hysteresis of an AlO_x-OTS PBTTT OFET in the dark (top) and under illumination (bottom), using the hysteresis quantification method described in section 4.2.5.

6.4.2.2. *Illumination effects on a tetracene MSM photodetector*

An OFET with SiO_2/OTS dielectric and gold top contacts was used for this light exposure test. All measurements were conducted using the I-V converter system, described in Chapter 4. The gate electrode was left unconnected and thus, the device operated as a simple two-contact device. Assuming that the physical presence of the Si/SiO_2 substrate does not affect the charge transport within the semiconductor film, this layout resembles the structure of a metal-semiconductor-metal (MSM) photodetector; hereafter, it will be referred to as such. However, some peculiar, yet interesting, rectifying properties of this particular device were observed and are discussed in this section.

The electrical characteristics of the device were measured in the dark and under illumination; the employed blue and green LEDs emit light over a wavelength range which coincides with the absorption spectrum of tetracene, as shown in Figure 6-2 and Figure 6-19.

Also, both current flow directions were tested, with the application of a drive voltage to both, the right- and the left-hand-side, electrodes; due to the symmetry of the tested device, these two different configurations are simply referred to as LHS and RHS, with respect to what electrode the output current of the device is taken from; i.e. the drain electrode in an OFET configuration.

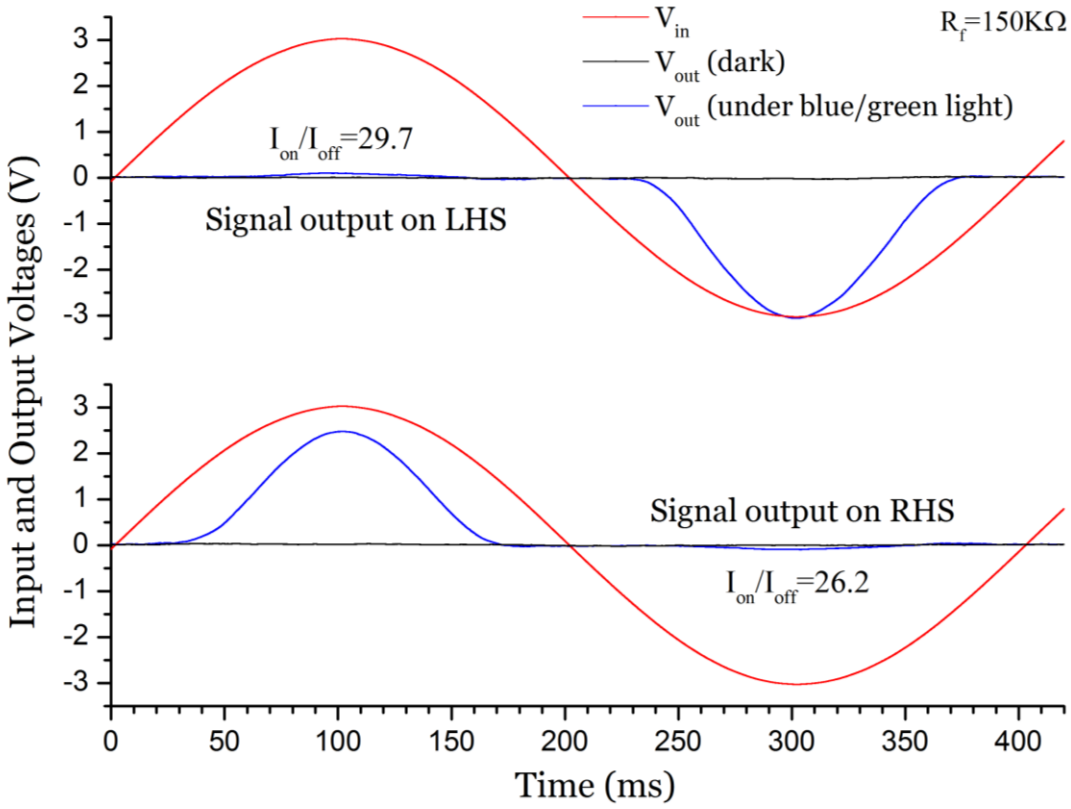

Figure 6-22 – Oscilloscope screenshots for a tetracene OFET with an electrically unconnected gate. Measurements taken in the dark (black curves) and under blue and green illumination (blue curves). The red curves represent the drive voltage.

Starting from an LHS-output configuration in dark conditions, the current flowing through the device was undetectable, as the black curves in Figure 6-22 illustrate. Under illumination, the device was interestingly found to rectify the drive signal; the measured current had a maximum value of roughly 2 μA, whereas its minimum value was limited to roughly 67 nA;

these figures give a rectification ratio (RR) of 29.7. This profile resembles a p-type OFET characteristic, similar to the blue and black curves shown in Figure 6-20; apparently, this fact can lead to the assumption that the presence of the gate stack, even with an unconnected gate electrode, effectively gates the device and amplifies its p-type behaviour.

However, after taking the first set of measurements, the electrical connections to the electrodes were swapped so that the rectification capabilities of the device could be evaluated for both current directions. For this RHS-output configuration, the output current was again undetectable in the dark; nevertheless, when the device was illuminated, the output curve was rectified in the opposite direction; the positive behaviour prevailed. The RR ratio was 26.2. This small difference can be attributed to minor differences in the charge carrier injection from and to the two top electrodes; i.e. a difference in the contact resistance when LHS or RHS configuration is used. Moreover, this finding is opposed to the SiO_2-gating assumption given above; if the Si/SiO_2 stack affected the carrier transport, then the polarity should not be inverted when the electrodes were swapped.

The excellent I_{light}/I_{dark} ratio constitutes a very interesting property, which can be attributed to a high trap density present within the bulk of the semiconductor in the dark, which is drastically reduced under illumination. This phenomenon is also discussed in section 6.4.2.1.

On the contrary, the rectifying properties cannot easily be given an adequate explanation; the absence of a real p-n junction and the symmetry of the device (two identical Schottky-diodes placed back-to-back) do not allow for drawing meaningful conclusions on the mechanisms which enable this one-way rectification.

6.4.3. Conclusion

Tetracene devices were found to give strong responses to light exposure. The illumination of a AlO_x-gated tetracene OFET with white light resulted in an increase of roughly 200% in its drain current, which is much higher than previously reported values.

Furthermore, the tests on a SiO_2-gated OFET with an unconnected gate electrode yielded some remarkable results. First, the device had an excellent light-to-dark current ratio, as its dark current was practically zero. Second, the device acted as an one-way rectifier when illuminated.

The behaviour of the latter device cannot be fully understood and explained by simplified semiconductor physics theory. Considering these interesting characteristics, a further investigation of these structurally simple devices and their sensitivity to light is advisable.

Chapter 7. Vapour sensing with organic semiconductors

This chapter demonstrates the analyte vapour sensing capabilities of organic semiconductor devices. An introduction to gas sensors with a special reference to organic-field effect transistors (OFETs) employed in gas sensing applications is given in section 1.2.

Both resistive (chemiresistors) and OFET transducers were used in the experiments discussed in this chapter. A selection of organic semiconductors, including polythiophene-derivatives (P3HT and PBTTT) and an electron-transporting material (PDI8-CN_2), was employed for the fabrication of these transducers. The analytes into investigation were water vapour, three different alcohols and an amine, all discussed in separate sections. Moreover, in the last section of this chapter, a demonstration of a real flexible OFET sensor is given as a proof-of-concept.

For the delivery of these experiments, the automated characterisation system, discussed in Chapter 4, was upgraded in order to support multiple devices under test and also control the analyte concentration, which the sensors were exposed to. Additionally, a complete gas exposure test rig was built in support of these experiments; this fully-automated sensor characterisation system enables the detection of quick responses of multiple parameters of an OFET sensor, which can hardly be detected using conventional electrical characterisation methods. This capability exploits the actual advantages of OFETs over chemiresistors.

The following sections discuss the experimental methods, including a description of the test rigs and the equipment developed, and provide an analysis of the results of a series of vapour exposure experiments using the aforementioned transducers and analytes.

7.1. Experimental methods

The development of appropriate test rigs is of great importance for performing consistent and quantitative vapour-exposure measurements. Tailor-made gas chambers, device-contacting systems, bespoke driving and multiplexing circuits for the characterisation of multiple sensors, as well as computer-controlled gas-mixing systems were designed and developed by the author in order to meet the requirements of the experiments discussed in this chapter.

These developments were used in conjunction with the automated OFET characterisation system discussed in section 4.3. A LabVIEW application was developed to fully exploit the capabilities of this system; Figure 7-1 shows a screenshot of its graphical user interface (GUI). In addition to the communication with the USB oscilloscope for the acquisition of sensor data, as discussed in section 4.3, this application establishes a bi-directional communication link with a *National Instruments (NI) USB-6008* multifunction data-acquisition (DAQ) instrument and a bespoke microcontroller-based multiplexing unit. The NI USB-6008 unit, underpinned by a bespoke driving circuit, controls the solenoid valves and the flow-mass controllers of the pneumatic system, while it samples the outputs of temperature and humidity sensors fitted inside the exposure chamber. The multiplexing unit can be used to switch between 20 sensors; simultaneous measurements on any four of them are supported by the developed software.

The sub-systems of this gas exposure and sensor characterisation rig are described in the sections 7.1.1 to 7.1.4. The respective schematics and PCB layouts are given in the appendices.

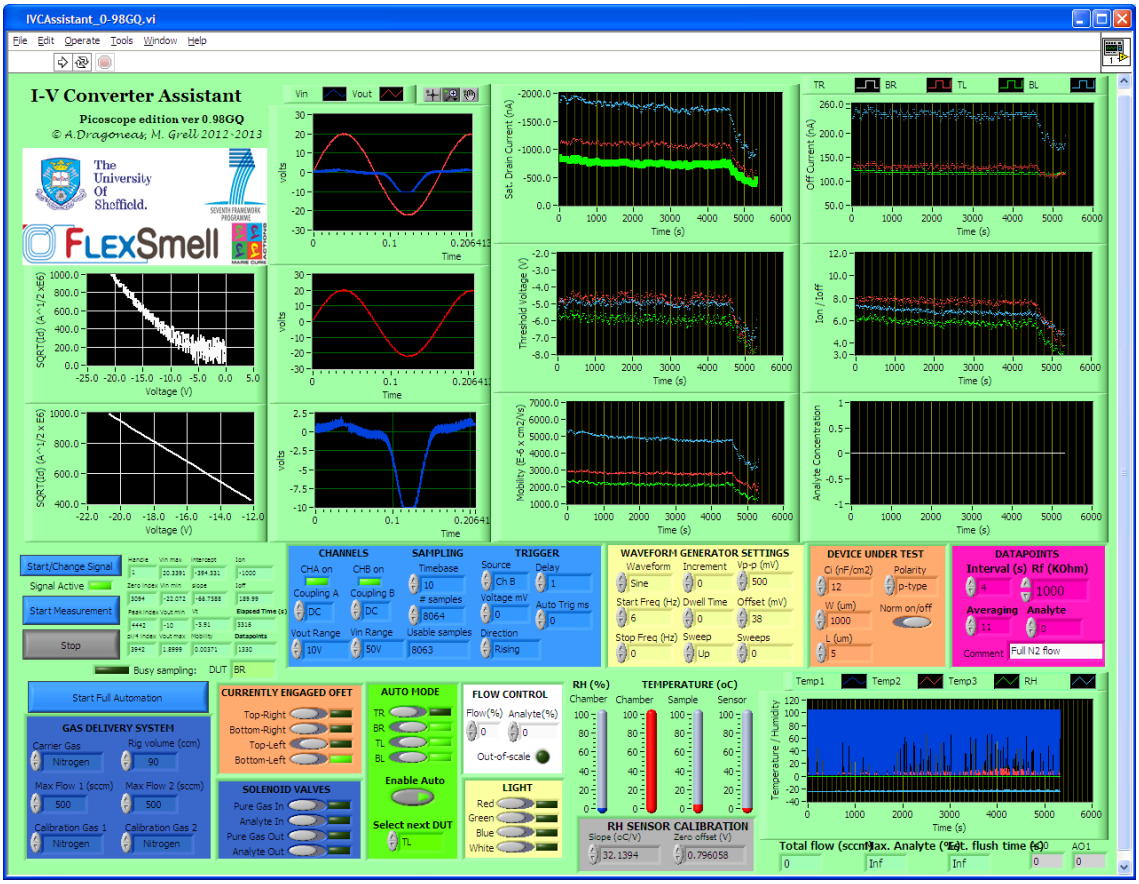

Figure 7-1 – Screenshot of the graphical user interface (GUI) of the LabVIEW application for the control of the gas exposure system and the real-time characterisation of OFET sensors.

7.1.1. Computer-controlled gas-mixing system

Figure 7-2 shows a schematic diagram of the automated gas mixing system and Figure 7-3 is a photograph of one of the two installed systems. The gas delivery is controlled by two voltage-controlled mass-flow controllers (*Tylan FC-260*); one of them regulates the flow of pure nitrogen, while the second one adjusts the flow of nitrogen that gets mixed with the saturated vapour of an analyte. For the majority of the tests, controllers with a full-scale throughput of 500 sccm (standard cubic centimetres per minute) of nitrogen were used. In some experiments, dry synthetic air was used as the carrier gas in lieu of nitrogen.

A solenoid valve is placed before each of the flow-mass controllers and another one on each of the two pipes before the mixing T-junction, as shown on Figure 7-2. These valves serve for securely blocking the small but undesirable gas flow which is admitted through the flow-mass controllers at the minimum setting of their scales. In some experiments, manual valves were used instead of the solenoid valves.

In this setup, the NI USB-6008 unit is used to generate the analogue control signals for the mass-flow controllers; also, it controls the operation of the solenoid valves with the support of a relay-based circuit. The circuit schematic and the respective PCB layout are given in Appendix II.7.

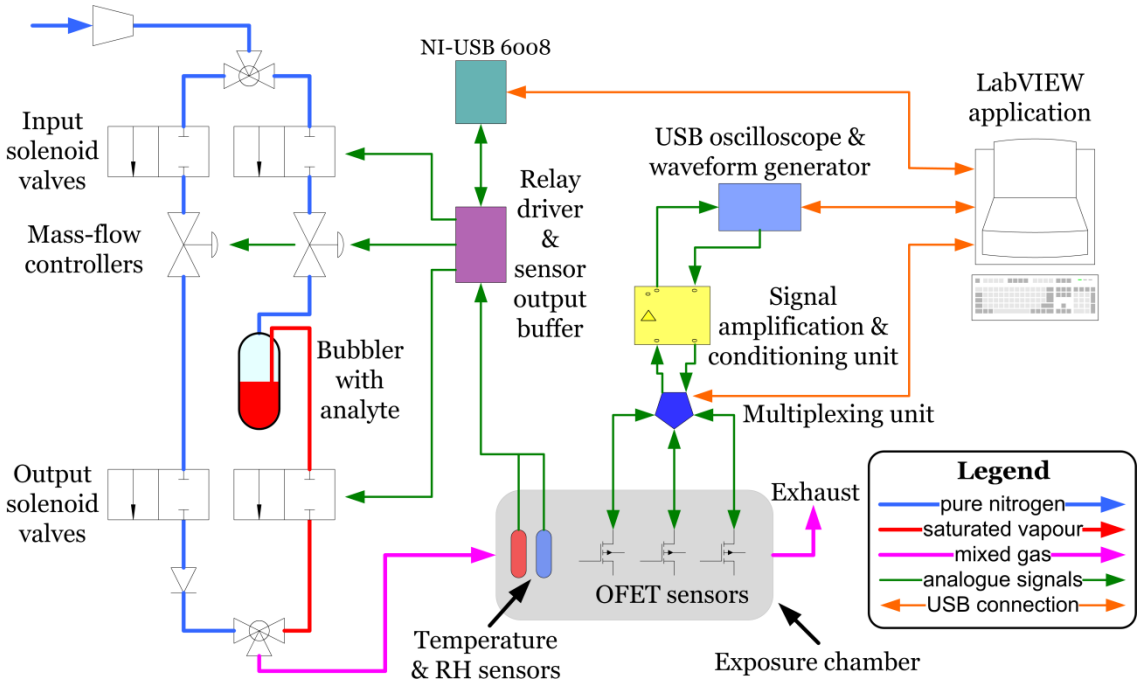

Figure 7-2 – Schematic diagram of the entire automated gas exposure test rig.

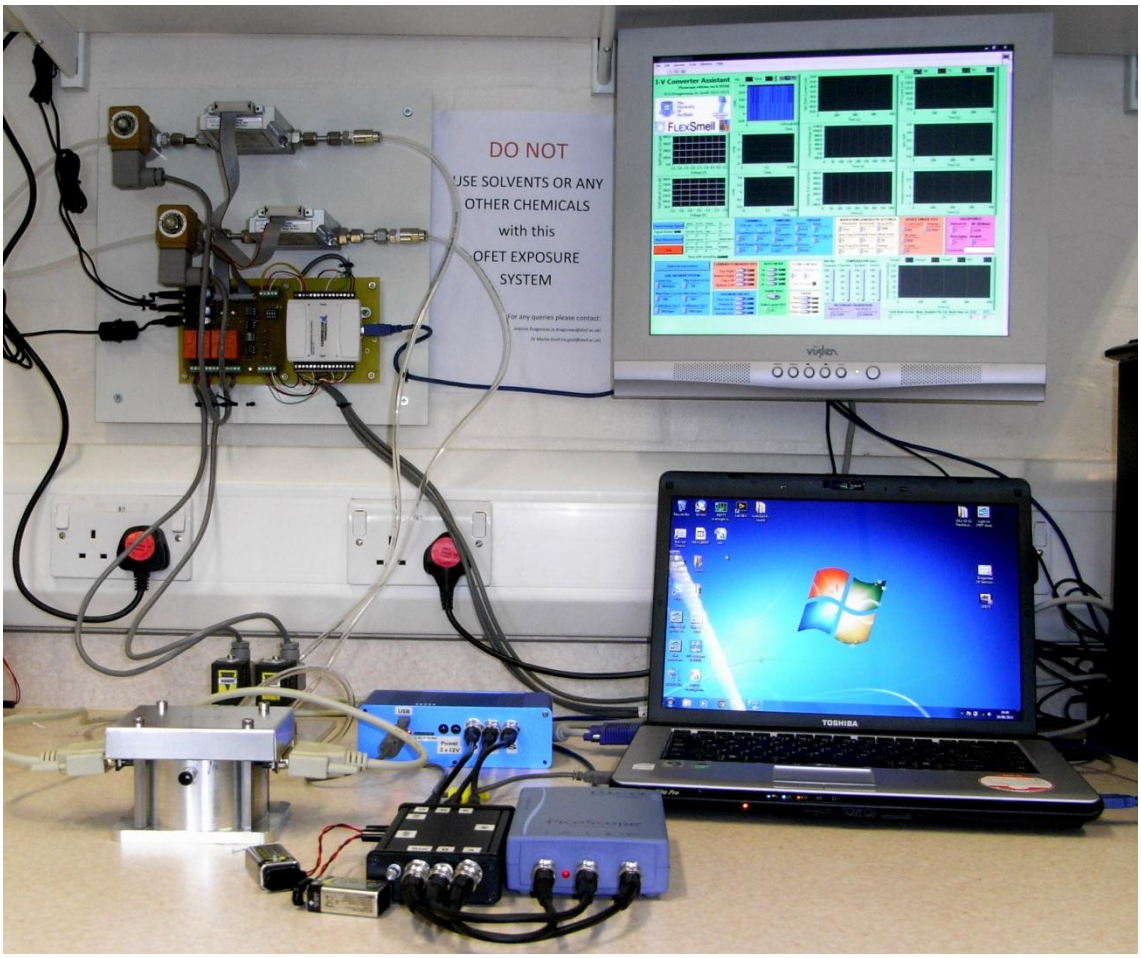

Figure 7-3 – A photograph of one of the automated gas exposure test rigs. Top-left: Input solenoid valves, mass-flow controllers and the corresponding driving PCB bearing the NI USB-6008 DAQ. Rear-left: Output solenoid valves (black with yellow tags). Left: Gas exposure chamber with the 20-DUT contacting lid. Front: I-V Converter system (black box) with a USB-oscilloscope (blue box). Middle: The sold-state multiplexing embedded system (light blue box). Right: Laptop running the LabVIEW control application shown on the external monitor.

The analytes were placed in sealed glass bubblers; the bubblers were either kept at ambient temperature or immersed in a thermostatically-controlled water bath. The control of temperature can effectively control the concentration of the analyte, as discussed in section 7.1.4.2. The second nitrogen line was fed into the bubbler and consequently, the carrier gas was mixed with the saturated vapour of the analyte. This mixture left the bubbler and then was further mixed with the first pure nitrogen line; this final mixture was fed into the exposure chamber. An optional check valve on the pure nitrogen line prevents the analyte vapour from flowing backwards and thus, contaminating the pipes. All pipework and the inside of the chamber were thoroughly flushed with nitrogen before and after each test.

7.1.2. Gas chambers and device contacting systems

A selection of custom-made gas exposure chambers were used for the measurements discussed in this chapter. Each of these assemblies consists of a hollow aluminium cylinder; the inner surface of the cylinder is lined with *polytetrafluoroethylene (PTFE)*, due to its chemical resistance.

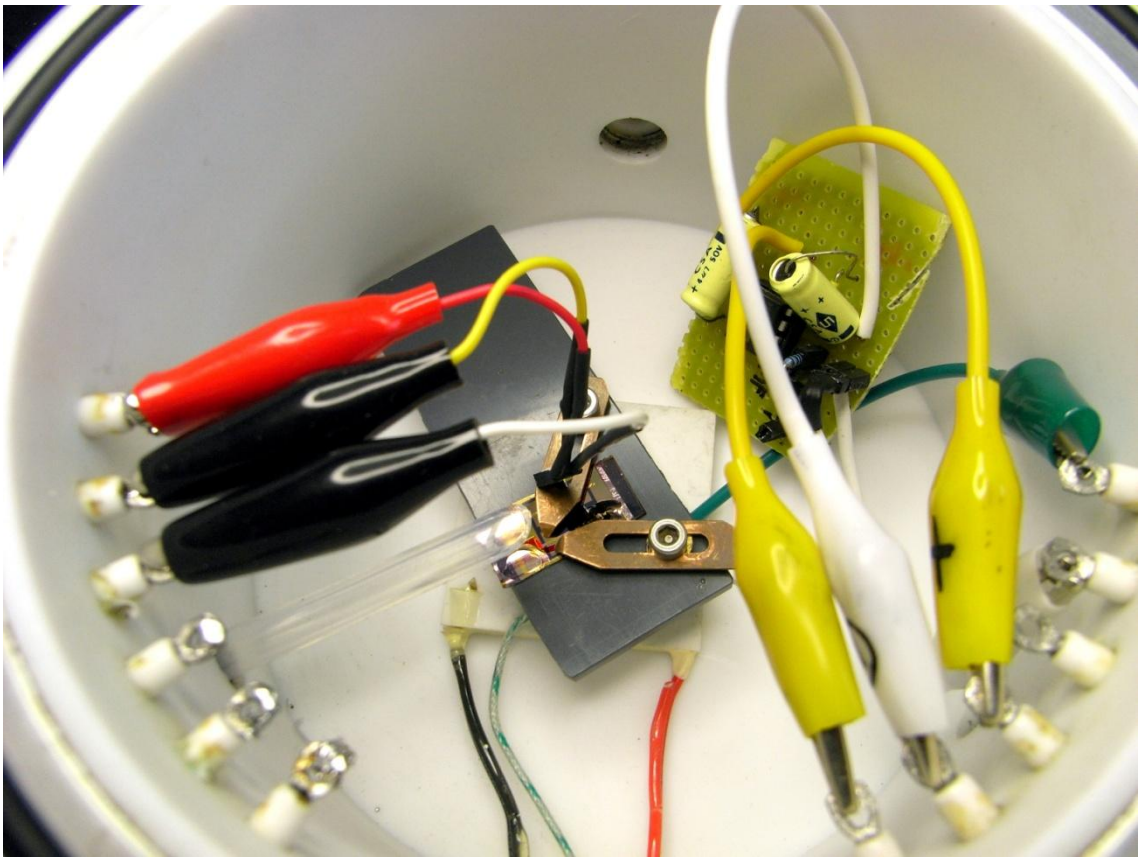

Figure 7-4 – The inner side of a PTFE-lined gas chamber. Middle: A P3HT nanowire chemiresistor placed on a sample holder and contacted by copper probes is shown. A current-to-voltage converter PCB is seen on RHS and a commercial RH sensor hanging over the sample under test. The pipe on LHS supplies the gas mixture into the chamber. Chamber capacity: ~400 cm^3.

Some of the experiments were carried out using a chamber with a capacity of 400 cm^3, approximately. In this case, the sensors were either contacted by copper probes, as shown on Figure 7-4, or using polymer-coated copper wire bonded with carbon-black-based glue (*Fluka Leit-C*, product number: *09929*). Twelve electrical feedthroughs serve for routing the driving signals in and the sensor outputs out of the chamber. The large volume of this type of chamber

can accommodate additional commercial sensors for monitoring the temperature and relative humidity (RH) levels inside the chamber; in some cases, even the amplification circuits were incorporated into the chamber for noise mitigation. An aluminium lid bearing an O-ring seals the top of the cylinder. The lid and the body of the cylinder can be connected to electrical ground, offering good electromagnetic interference (EMI) protection by effectively acting as a Faraday cage.

A later improvement has been the design and construction of a small volume (90 cm^3) chamber with specially designed lids which serve as contacting systems for all the devices built on each substrate. Two different designs were developed. The first of them is capable of contacting four devices under test (DUT) and its design and geometry are based on the layout of the respective evaporation mask; which is mainly intended for low-voltage, aluminium-oxide-gated OFETs. The second design is based on the layout of a commercially available evaporation mask (*Ossila E326*); in this case, twenty devices reside on the same substrate and they are all contacted by the lid.

The lids are tailor-made PTFE-coated printed-circuit boards (PCBs) with a series of special sockets soldered onto them; the sockets can accommodate a selection of commercial spring-loaded test probes. In most cases, gold-plated probes with rounded tips were used to contact devices with top metal contacts, usually made of gold. On the contrary, probes with sharp tips were used to contact the underlying gate electrodes, be they doped silicon, aluminium or silver; these tips could penetrate the deposited semiconductor film and get in direct contact with the gate contact material. A similar type of probe tips was used for devices with bottom source-drain contacts. Figure 7-5 shows a 20-DUT substrate being contacted by this system. Detailed technical information on the contacting lids is given in Appendix II.2 and Appendix II.3.

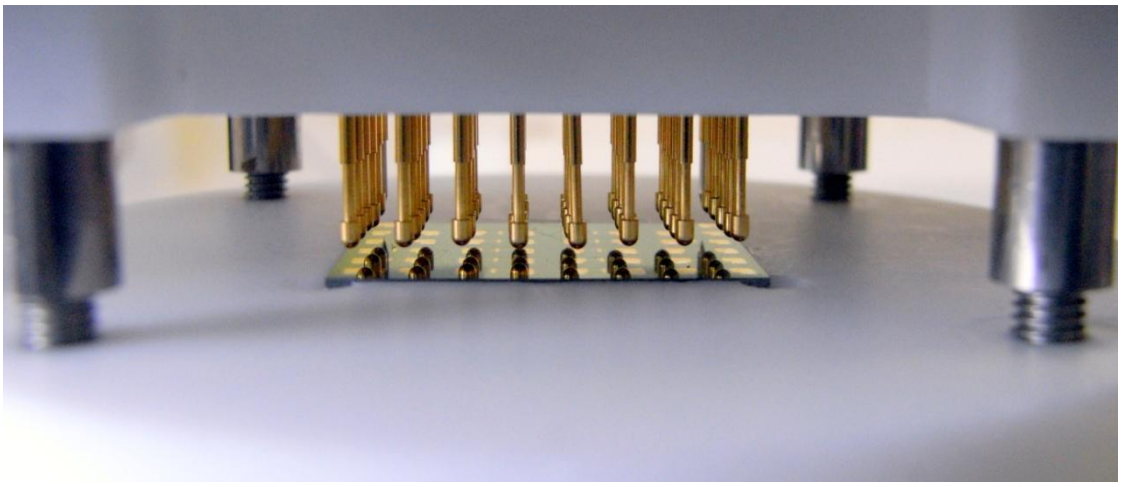

Figure 7-5 – Photograph of the gas exposure contacting system during the assembly. A twenty-OFET substrate is inserted into the recess of PTFE sample holder (bottom). The mating gold-plated probes are suspended over the sample. Distance between adjacent probes: 2.54 mm, total width of the substrate: 20 mm.

7.1.3. Sensor multiplexing systems

The contacting systems presented in the previous section comprise multiple-pin connectors (of D-subminiature type); each of these pins corresponds to one contact of devices-under-test (DUT). For the exploitation of multiple sensors using one set of read-out electronics, the presence of an appropriate multiplexing unit is necessary. For this reason, three different units were built.

In the case of the 4-DUT system, a manual and an automatic unit were designed and made. The manual unit is a PCB with two sets of quadruple DIP switches which allow for routing the source and drain signal lines to any of the four DUT. The automatic unit is a relay-based PCB which is controlled by one of the digital output ports of the NI USB-6008 instrument; as in the operation of the manual unit, four double-pole double-throw (DPDT) relays route the source and drain signal lines to any of the four DUT. Additionally, the PCB has four operational amplifiers (op-amp) which buffer the outputs of the temperature and RH sensors so that they can be sampled by the NI USB-6008 analogue-to-digital converter (ADC). Technical information on these units can be found in Appendix II.4 and Appendix II.5. This system can safely operate with applied voltages which comply with the highest ratings of the I-V converter system, i.e ±45 V.

In the case of the 20-DUT system, a microcontroller-based embedded system with solid-state analogue switches has been designed to multiplex the signals from the twenty sensors. The microcontroller (*Atmel ATMega88*) communicates with the LabVIEW application over a USB connection and controls four integrated circuit (IC) chips (*Analog Devices ADG1606/BRUZ*), which are capable of multiplexing analogue signals. Any DUT can be selected from the graphical user interface (GUI) running on the control computer. Up to four sensors can be tested using virtually simultaneous real-time characterisation. The applied voltages are limited to ±8V due to the limitations of the solid-state switches. The circuit schematic and the PCB layout of this circuit are given in Appendix II.6.

7.1.4. Exposure test methodology

7.1.4.1. *Exposure and recovery periods*

Most of the vapour-sensing measurements were conducted in a time-resolved manner; the sensors were initially pre-conditioned under a constant-flow nitrogen purge while their electrical performance was being monitored and recorded. For some experiments, a pre-conditioning period of up to 3 days was applied. Details are given in the respective experimental sections 7.2, 7.3 and 7.4.

The pre-conditioning phase was followed by analyte exposure periods. During exposure, the flow-mass controllers are commanded to mix the pure carrier gas line with the line delivering the saturated analyte vapour; at the same time, the solenoid (or manual) valves of the analyte line open to permit the gas flow. Using the automated system described in section 7.1.1, the *mixing ratio* of the saturated vapour line to the pure carrier gas line can be selected by the user while the total gas flow is automatically adjusted by the software to ensure that it remains constant. For instance, given that two identical flow-mass controllers are in use and the pre-conditioning phase was set at 100% maximum flow, if a mixing ratio of 40% is selected,

then the pure carrier gas controller will be re-adjusted at 60% maximum flow, whereas the saturated vapour one will be set at 40%, so that the total flow remains as it was initially.

When each exposure was ceased, a recovery period was initiated and the flow-mass controllers were reset; the pure nitrogen line controller alone provided the total flow, whereas the second controller was set to zero; additionally, the solenoid (or manual) valves on the saturated vapour line were closed, in order to block any leakage flow through the controller.

7.1.4.2. *Analyte concentration*

It is a common practice to express the analyte concentration in terms of *parts per million (ppm)*; ppm concentration has several definitions as it can describe ratios of various quantities, such mass-to-mass (m/m), mass-to-volume (m/v) etc. In the work described in this chapter, as in most papers on gas sensors, ppm concentration is defined as the number of analyte molecules in every one million molecules of substances which form a gas mixture. There are two main factors which determine the ppm of an analyte in a vessel; the *(saturated) vapour pressure* of the analyte and the *mixing ratio* of the saturated vapour delivery line to the pure carrier gas one, as mentioned above.

The *saturated vapour pressure* (p_{sat}) of a liquid is the pressure exerted by its vapour when it is in thermodynamic equilibrium with its liquid phase at a given temperature in a closed system. The exponential dependence of p_{sat} on temperature is described by the Clausius-Clapeyron relation. In practice, p_{sat} can be extracted from experimental data taken at different temperatures; an example is given in section 7.3.3, which provides information on the calculation of the vapour pressure for the three analytes used in quantitative measurements.

In the saturated vapour line, the carrier gas molecules are mixed with molecules of the analytes; neglecting the presence of any contaminants, each of the two constituent substances have their own *partial pressures* such that:

$$P = p_{carrier} + p_{analyte} \tag{7.1}$$

where P is the total pressure, $p_{carrier}$ and $p_{analyte}$ are the partial pressures of the carrier gas and the analyte, respectively.

Given that the carrier gas flow is rather slow, it can be assumed that the bubbler resembles a closed system so that the partial pressure of analyte vapour in the mixture, which leaves the outlet of the bubbler, equals its vapour pressure at that temperature:

$$p_{analyte} = p_{sat} \tag{7.2}$$

Also, we take the *ideal gas law*:

$$PV = nRT \tag{7.3}$$

where P is total pressure of the gas, V is volume it occupies, n is the number of mol of the gas, T is the temperature and R is the *ideal gas constant* (8.314 $JK^{-1}mol^{-1}$).

For this gas mixture, eq. (7.3) writes:

$$(p_{carrier} + p_{sat})V = (n_{carrier} + n_{analyte})RT \tag{7.4}$$

where $n_{carrier}$ and $n_{analyte}$ are the number of molecules of the carrier gas and the analyte, respectively.

By its definition, the concentration in ppm can be expressed as:

$$\mathrm{ppm} = \frac{\mathrm{n_{analyte}}}{\mathrm{n_{carrier}} + \mathrm{n_{analyte}}} \times 10^6 \quad (7.5)$$

which, according to (7.4), can write:

$$\mathrm{ppm} = \frac{\mathrm{p_{sat}}}{\mathrm{P}} \times 10^6 \quad (7.6)$$

For all calculations, *the standard pressure* (100 Kpa) has been used as the value of total pressure P, as it serves as a good approximation of the actual ambient pressure in the laboratory.

Equation (7.6) gives the ppm of the analyte in the saturated vapour delivery line. As this line is mixed with the pure carrier gas line before being fed into the exposure chamber, the actual ppm concentration is calculated by:

$$\mathrm{ppm} = \mathrm{MR} \times \frac{\mathrm{p_{sat}}}{\mathrm{P}} \times 10^6 \quad (7.7)$$

where MR is the mixing ratio of the saturated vapour line to the pure carrier gas line (v/v).

However, in some examples given in this text, the analyte concentration (C) is sometimes expressed as a percentage of p_{sat}:

$$\mathrm{C} = \mathrm{p_{sat}} \times \mathrm{MR} \quad (7.8)$$

7.1.4.3. ***Relative Humidity***

In section 7.3, water vapour is the analyte under investigation. In this particular case, the analyte concentration is expressed in terms of *relative humidity (RH)*. RH represents the water vapour content of an air-water mixture as a percentage and it is described by:

$$\mathrm{RH} = \frac{\mathrm{p_w}}{\mathrm{p_{w,sat}}} \times 100\% \quad (7.9)$$

where p_{sat} is the partial pressure of water and $p_{w,sat}$ is the saturated vapour pressure of water, both at a given temperature.

Again, assuming that the analyte vapour delivery line is saturated, i.e. RH = 100 %, the RH of the final mixture, which is fed into the chamber, equals the mixing ratio (MR) of the flow of this line to that of the pure carrier gas line:

$$\mathrm{RH} = \mathrm{MR} \quad (7.10)$$

Roughly speaking, for a given mixing ratio, RH remains constant under room temperature fluctuations.

7.2. P3HT devices under humidity

7.2.1. Introduction

Humidity is a measure of the amount of water vapour in air; it is an important parameter for many meteorological, domestic, medical and industrial applications and several quantification methods and respective transducers have been demonstrated. Most of these sensors are based on metal oxides and polymers [150]; recently, a combination of the two was demonstrated [151]. The transduction is usually electrical with either a resistive or capacitive readout [152-154]; however, surface acoustic wave (SAW) resonators represent an interesting alternative [155].

In the field of organic semiconductors, humidity has been suggested as factor which contributes to the mobility degradation of some OSCs, including pentacene [83]; this phenomenon is attributed to the diffusion of water molecules into the grain boundaries of a semiconductor film. In the case of polythiophenes, P3HT devices are known to increase their conductivity in ambient conditions; this was initially attributed to the formation of a charge transfer (CT) complex with atmospheric oxygen [156, 157]. However, Hoshino *et al.* established that the effect of atmospheric humidity on the conductivity of P3HT is even stronger [158]. Additionally, Leary *et al.* later performed a theoretical study based on quantum chemical computations to shed light on the specific interactions between water and oligothiophene-containing molecules; they provide a model which explains how water vapour effectively gates thiophenes and that the length of the thiophene is crucial for the magnitude of the effects [159]; this phenomenon is not commonly observed in other organic semiconductors.

This specific sensitivity to humidity can induce significant instability issues in thiophene-based devices operating in ambient conditions; however, this property can also be harnessed as a sensing parameter, effectively enabling such devices to operate as humidity sensors. This is the scope of the work presented in this section; two sets of devices based on regioregular-P3HT with different morphologies are compared in terms of their sensitivity to humidity. The compared morphologies are a conventional spin cast thin film, and a mesh of one-dimensional crystals, commonly referred to as nanowires (NW), which are spin cast from an anisole suspension [94, 160]; a further discussion on P3HT and P3HT NW is given in section 2.5.4.

The largely increased semiconductor surface area of the NW-based device, as compared to the conventional thin-film one, is suggested as asset for sensitivity enhancement. In the context of sensor active surface enhancement, there are several documented approaches; for instance, Nomura *et al.* have recently demonstrated a ten-fold sensitivity increase in biomolecular sensors which were built on porous glass substrates, as compared to a non-perforated control [161]. The NW concept can be thought of as the opposite to a porous material, practically having the same result. In a noteworthy similar study, Huang et al. have reported that in a comparison between a device based on conventional polyaniline (PAni) film to one based on PAni nanofibres, which are morphologically very similar to NWs, the electrical resistance of the latter responds much more strongly to hydrochloric acid vapour, which acts as a PAni dopant [162].

Details on device preparation and the test methodology, as well as a discussion on the results of these measurements follow.

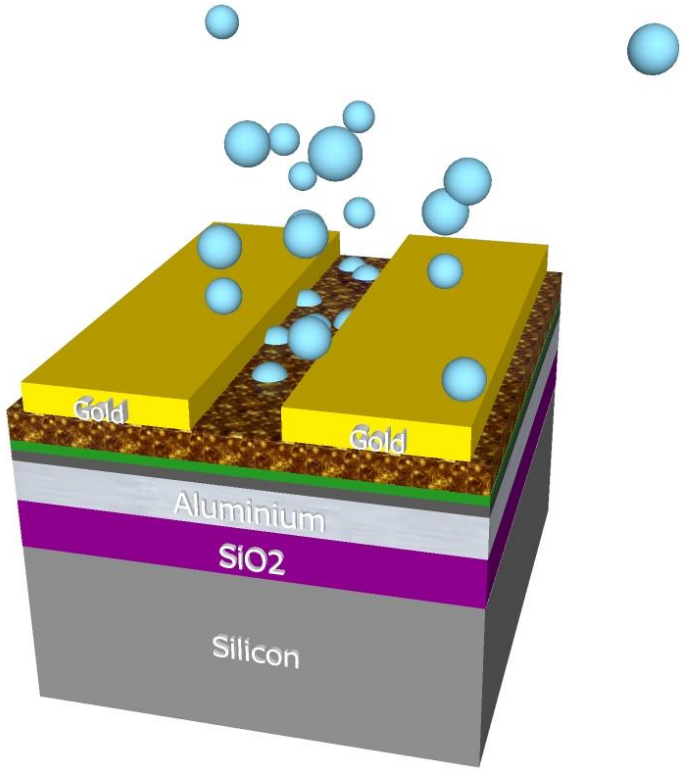

Figure 7-6 – A graphical representation of a P3HT-based sensor under exposure to water vapour (blue spheres). Channel length: 10 µm, channel width: 2000 µm.

7.2.2. Device preparation

The P3HT nanowires were prepared at the University of Cardiff via a variation of the whisker method [94]. P3HT was dissolved in anisole (5.2 mg/mL). The solution was heated to 90 °C until fully dissolved and allowed to cool to room temperature. The solutions were kept in sealed vials and stored in the dark for 3 days for the nanowires to be formed. The conventional P3HT film solution was prepared by dissolving P3HT in chlorobenzene (4.9 mg/mL) at room temperature.

The devices were built on substrates cut from a doped silicon wafer with a 100-nm-thick thermally grown oxide layer. An 100-nm-thick layer of aluminium was thermally evaporated through shadow masks in a high vacuum of $<10^{-6}$ Torr; the deposition rate was roughly 0.1 nm/s. The patterned aluminium stripes were immersed into a 1 mM citric acid solution and then anodised by the application of current, with a constant current density of 5 mA/cm^2 and a voltage limit of 5 V, to form a thin aluminium oxide layer; more details on aluminium oxide formation are given in section 2.4.2.

An octadecyltrichlorosilane (OTS) in cyclohexane solution (10 mg/mL) was prepared in a dry nitrogen glove box and the samples were immersed into the solution for 10 minutes so that OTS monolayers would self-assemble as a hydrophobic surface treatment, more details on OTS treatment of oxides are given in section 2.4.3.

The solutions were spin cast in a spin coater with nitrogen purge. The substrates with the P3HT NW suspension were spun at 6000 rpm for 40 seconds, while the ones with standard P3HT solution at 1200 rpm for 40 seconds. Finally, gold was evaporated through shadow masks in high vacuum; the deposition rate was 0.01 nm/s and the dimensions of the patterned channels were 10 µm (length) and 2 mm (width).

The described device architecture allows the application of a gate voltage for field-effect transistor operation; however, due the highly-doped electrical behaviour of P3HT, the effect of gating was not found to significantly enhance the current flowing through the device, thus the gate contact was left disconnected, as discussed in the next section.

7.2.3. Test methodology

After conducting preliminary tests with both dry nitrogen and dry synthetic air, the latter was selected as the carrier gas for the quantitative humidity exposures; dry air serves as a more pragmatic environment for the operation of an actual sensor. The indifference in the electrical performance of the devices under either nitrogen or dry air is noteworthy, as the oxygen present in the synthetic air mixture was not found to cause any effects.

Deionised water was kept in a bubbler immersed in a water bath which was thermostatically controlled at 25 °C. The carrier gas was fed into the bubbler and injected into the water through a PTFE frit. The samples under test were electrically contacted by copper probes on a small custom-made stage. This assembly was placed inside the chamber and was connected to the I-V converter system, discussed in Chapter 4, by the use of multiple electrical feedthroughs. Additionally, a calibrated commercial relative humidity sensor (*Honeywell HIH-4010*) was also placed inside the chamber; its readings were used for comparison to the nominal mixing ratio. A photograph of this setup is shown in Figure 7-4.

A zero-offset sinusoidal drive was applied to the one of the top contacts of each DUT; the signal frequency was 6 Hz and its maximum voltage was set at 3 V. The gate contact was neither connected to the characterisation system nor grounded, i.e. an electrically floating gate; this configuration made the devices operate as chemiresistors rather than OFETs. The resulting current was fed into the inverting input of a low-bias-current operational amplifier and consequently, converted into an output voltage using a fixed-value feedback resistor of 1MΩ. The input and output voltages were sampled and recorded by an oscilloscope. The tests on the NW sensor were conducted before the development of the automated characterisation system and thus, all measurements and calculations were carried out manually, by exporting the oscilloscope data. The control measurements on the P3HT-film device were taken with the aid of the automated characterisation system, described in section 4.3.

The conductance of the solution-cast P3HT film device in dry conditions, prior to exposure, was 57 nS , which corresponds to a sheet resistance of 3.5 GΩ/□. The values for the P3HT NW chemiresistor were 21 nS and 9.5 GΩ/□, respectively. Considering that these magnitudes of conductance are high enough for low-noise electric measurements and that the application of a gate voltage was not found to substantially increase the observed current, the following measurements were taken in chemiresistor mode. Given that, in this study, the importance of the exposed surface area is under the spotlight, simple chemiresistors can serve for this purpose; the use of the gate electrode would have introduced more sensing parameters which, even being favourable for other experiments (e.g. ethanol vapour detection, discussed in section 7.3.4), do not facilitate the drawing of conclusions in this occasion.

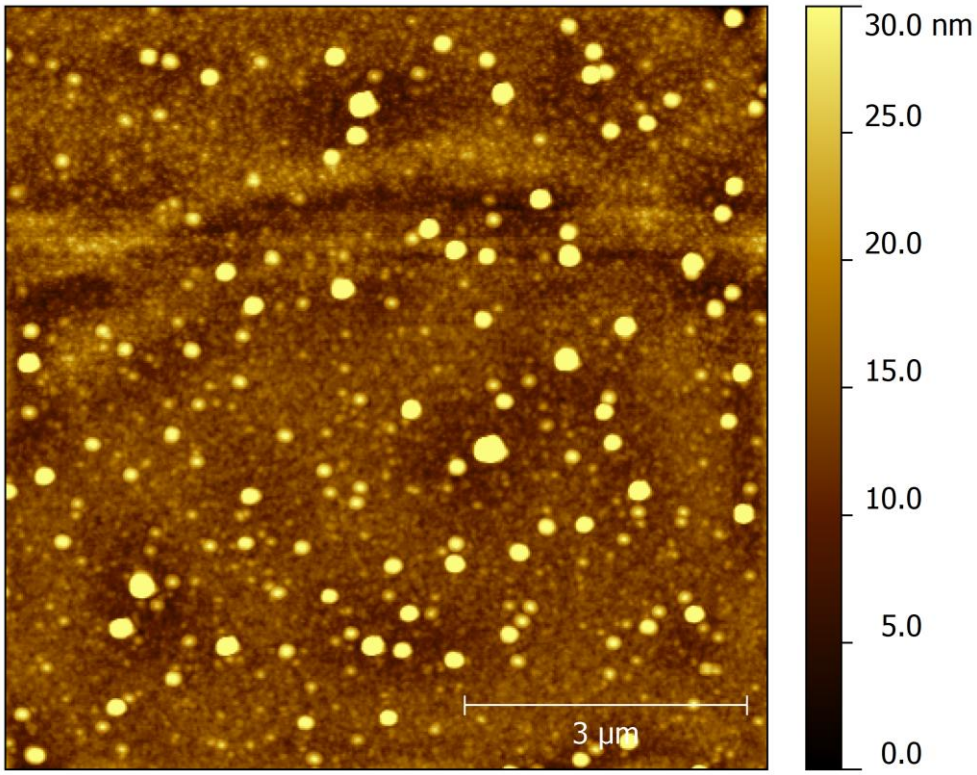

Figure 7-7 – Atomic-force microscope image of the channel area of a P3HT-film chemiresistor

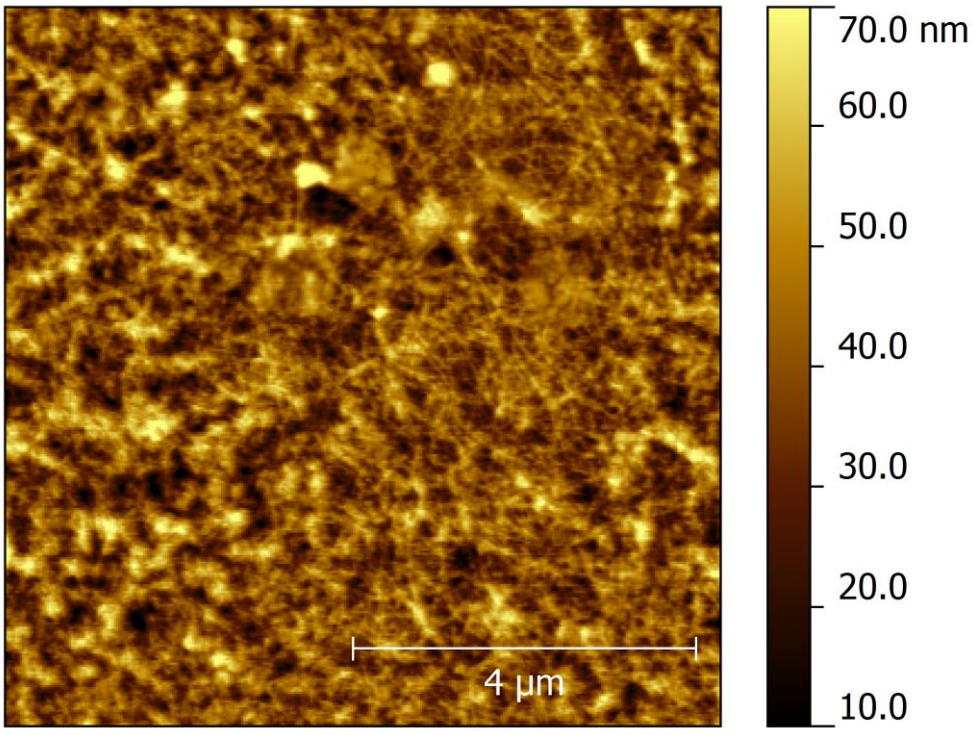

Figure 7-8 – Atomic-force microscope image of the channel area of a P3HT-nanowire chemiresistor

7.2.4. Results and discussion

The morphological differences between the spin-cast film and the nanowires (NW) were confirmed by performing atomic-force microscopy (AFM) on their surfaces, as shown in Figure 7-7 and Figure 7-8; the conventional device had rather low surface roughness, whereas the surface of NW sample was formed by a network, or mesh, of interpenetrating P3HT NW.

Analysis of the AFM data revealed that the dimensions of the NWs on the examined surface are quite uniform; their height varied between 2 and 7 nm, their width was approximately 30 nm and their length was typically in excess of 5 μm, with some extending far beyond 10 μm. Considering that the distance between the top gold electrodes is 10 μm, it is possible for some single NWs to bridge the channel; transistors based on a single NW have been previously demonstrated [163]. Nevertheless, considering the morphology of the NW mesh, it is more likely that several overlapping NW typically serve as the conduction pathways between the contacts.

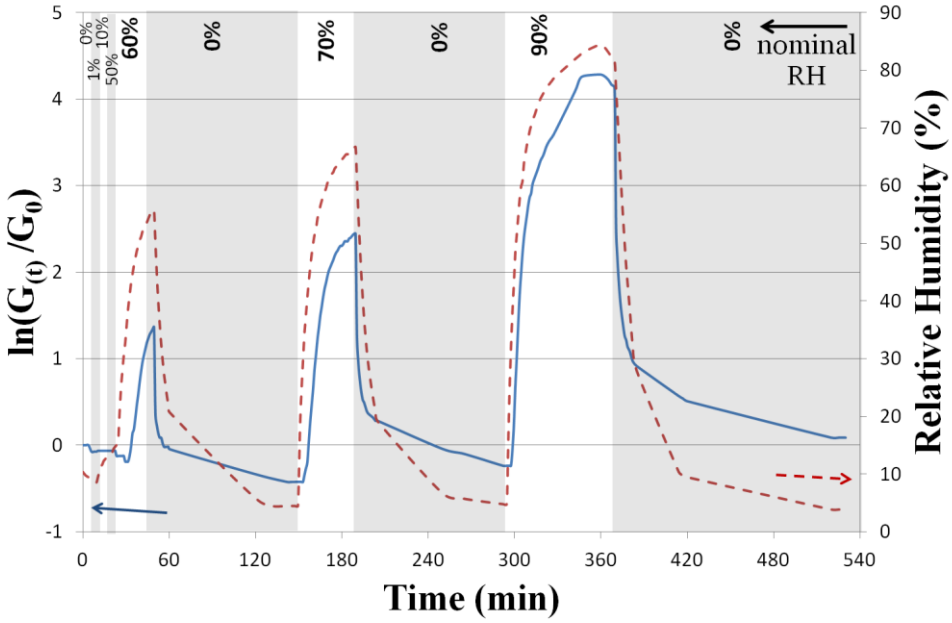

Figure 7-9 – Conductance behaviour of P3HT NW chemiresistors under exposure/recovery cycles to different levels of RH (continuous blue line, scale on the left), shown in a logarithmic metric. Alternating white/shaded regions indicate different RH exposure phases. The percentages shown near the top are nominal RHs, i.e. the mixing ratios between dry carrier gas, and carrier gas saturated with humidity, as established by mass flow controller settings. Also shown are the RH levels measured by a conventional RH meter (dashed red line, scale on the right).

Figure 7-9 illustrates the exposure test of the P3HT NW chemiresistors under exposure/recovery cycles to synthetic air with different RH levels; the pre-conditioning period is excluded from this graph. Due to the large sensitivity of the sensor to humidity, the ratio of conductance at a given time ($G_{(t)}$) to its pre-exposure value at the beginning of the test (G_0), is given in a logarithmic metric. In the same graph, the readings of the commercial humidity sensor are also shown for comparison. Their values were found to fall a few percent behind the nominal RH level; this comes in good agreement with the fact the RH percentage equals the defined mixing ratio of the saturated vapour line to the pure carrier gas one, as discussed in section 7.1.4.3, and confirms the consistency of the humidity delivery system.

During the pre-conditioning period, the conductance showed a substantial decrease while the dry air purge was drying out the chamber from ambient moisture. This drift carried on during the first periods of exposure to a low level of RH (1%). For levels between 10% and 50%, the conductance of the NW sensor remained stable; notwithstanding, the commercial sensor gave a response even for 10% RH.

At 60% RH the NW sensor showed a massive increase in its conductance which was followed by a rapid recovery under dry air; in fact, the response of the NW sensor to humidity showed a initial lag, however its recovery was found to be even faster than that of the commercial sensor. At 70% and 90% RH, the responses of the sensor were even stronger; all values were found to have an exponential dependence on the level of RH with a 30% RH change required for a decade enhancement in conductance, as shown in the inset of Figure 7-10. The sensor recovered from all exposures; however, the recovery time increased with increasing level of RH.

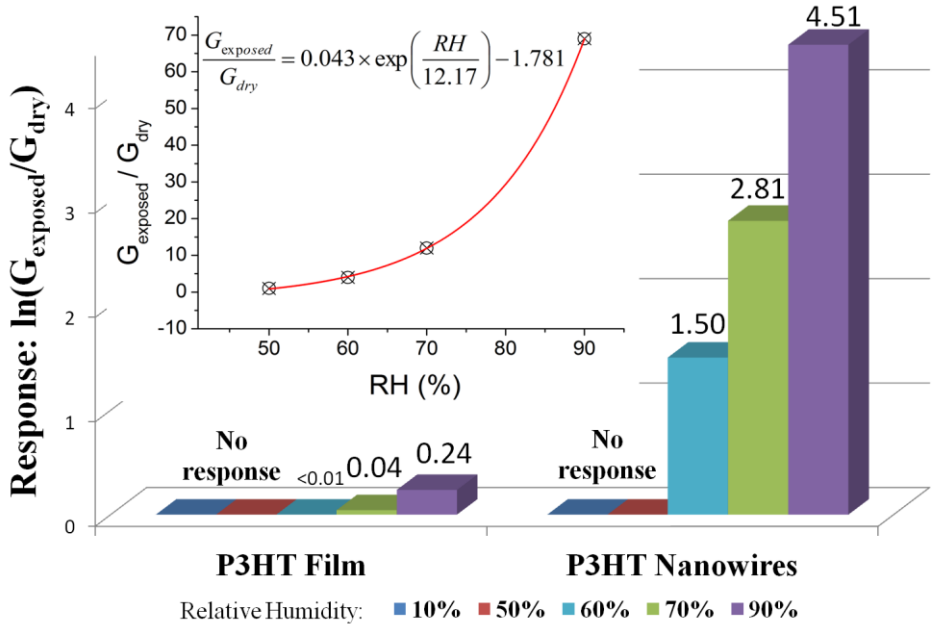

Figure 7-10 – Comparison of chemiresistor responses, expressed as ratios of the maximum conductance under humidity exposure ($G_{exposed}$), over the conductance in dry conditions just before exposure (G_{dry}), for different levels of relative humidity. Left: Response of solution-cast P3HT film. Right: Response of NW 'mesh'. Both responses are shown in a logarithmic metric. Inset: The same figures for the NW 'mesh' device plotted in a linear scale and a non-linear fit shown in red, which is described by the given exponential equation.

The same test pattern was applied to a device with P3HT spin-cast film for comparison. The comparative results from the two tests are shown in Figure 7-10; the responses of the two sensors for different levels of humidity are expressed in a logarithmic metric. It is worth mentioning that the limit of detection (LoD) was the same for both sensors; this threshold of 50% RH was found to be irrelevant to the morphology of the semiconductor and appears to be a characteristic of the material itself. Interestingly, the same threshold has been previously reported for potassium hydroxide (KOH)-H_2O-doped PVA (poly-vinyl alcohol) devices [164].

For water vapour concentrations above threshold, the NW device outperformed the cast film one, in terms of conductivity response. For the highest tested concentration of 90% RH, the P3HT-film sensor exhibited a 25% increase in conductance, relative to its pre-exposure value in dry conditions; respectively, the P3HT-NW sensor showed a more than 75-fold conductance increase. This 300 times stronger response can be attributed to the much larger surface area of the NW device as compared to its film counterpart; the larger the area, the higher the probability of interactions between the semiconductor and the water vapour taking place.

7.2.5. Conclusion

The work presented in this section demonstrates the importance of material preparation in the sensitivity of organic semiconductor sensors. A common organic semiconductor, poly(3-hexylthiophene) (P3HT) was used for the fabrication of chemiresistors. Two different solutions of P3HT were prepared: one of them resulted from simple dissolution of the semiconductor in chlorobenzene, whereas for the preparation of the latter, P3HT was first dissolved in anisole and then, a special physicochemical treatment cycle was applied; this method led to the formation of nanowires in the form of suspension.

The increase in conductivity of P3HT when exposed to atmospheric humidity has been previously reported; however, this study reveals that the much larger surface area of a NW structure constitutes a major advantage over the conventional film device. It was found that that both types of chemiresistors have a limit of detection at roughly 50% relative humidity. Above this threshold, the conductance of both sensors increased. Nevertheless, the response of the NW device far exceeded that of the conventional film; as an example, under exposure to 90% RH, the response of the NW sensor was 300 times stronger than that of the conventional film one.

This finding paves the way for the sensitivity enhancement of other vapour sensors based on organic semiconductors; the development and deposition of the semiconductor in the form of one-dimensional crystals can be favourable for this purpose. The work presented in this section has been published as a research paper in the *Sensor Letters* journal [165].

7.3. PBTTT OFET sensor sensitivity to alcohols

7.3.1. Introduction

Polythiophene-derivates have long been used as active materials for OFET vapour sensors [12]. R. A. Street *et al.* have published a remarkable comparative study on the effects of several organic and inorganic analytes on multiple parameters of *poly(3,3'''-didodecyl-quaterthiophene) (PQT-12)* transistors [166]. In a recent example, Kettle *et al.* used planar OFETs employing *poly(3-hexylthiophene) (P3HT)* as sensors of a selection of volatile analytes including *methanol* and *isopropyl alcohol (IPA)* [167]. Moreover, Torsi *et al.* demonstrated an OFET sensor based on surface-treated SiO_2 gate dielectric with a *α,ω-poly(sexithiophene) (DHαHT)* semiconductor [14]; the sensor showed good sensitivity to *n-butanol* vapours and the effects have been attributed to both channel and contact resistance changes.

In this section, the quantitative exposure of OFET sensors based on either *poly(2,5-bis(3-tetradecylthiophen-2-yl)thieno[3,2-b]thiophene) (PBTTT-C14)* or *poly(2,5-bis(3-hexadecylthiophen-2-yl)thieno[3,2-b]thiophene) (PBTTT-C16)* semiconducting polymers to vapours of three different alcohols is discussed. Two different batches of sensors with similar architecture were tested: the first of them was based on PBTTT-C14 and was fabricated in the laboratories of the University of Bari, Italy; the second was based on PBTTT-C16 and was developed in the University of Sheffield, UK. The former was used to conduct n-butanol exposure tests, which are discussed in section 7.3.6; the latter was used in the more detailed automated measurements under ethanol and n-octanol exposure, which are presented in sections 7.3.4 and 7.3.5, respectively.

Due to the differences in device preparation techniques, experimental methodology and equipment used for the tests described in the aforementioned sections, a separate description of these topics is given for each device batch and the each test performed on them. A comparative discussion of all devices is given in section 7.3.7.

7.3.2. Device preparation

The first batch of devices employed an n-doped silicon wafer as a substrate. A thermally-grown oxide layer with a thickness of 300 nm served as the gate dielectric material. PBTTT-C14 semiconductor was dissolved in chlorobenzene (5 mg/mL) and was heated at 75 °C for several minutes before being spin cast onto the substrates. The substrates were spun at 3000 rpm for 120 seconds in a spin coater with nitrogen purge. Gold was evaporated in high vacuum through shadow masks to pattern the top source and drain electrodes; the deposition rate was set at 0.15 nm/s and the final thickness of the patterned gold electrodes was 100 nm. Each substrate had 40 patterned parallel electrodes; the dimensions of OFET channels, i.e. the areas between two adjacent electrodes, were 200 µm (length) x 4000 µm (width). The substrates were finally annealed at 100 °C for 60 seconds in ambient atmosphere. Devices from this batch were used for the n-butanol vapour exposure tests discussed in section 7.3.6.

The second batch of devices was also built on heavily n-doped Si substrates with a thermally grown oxide with a thickness of 300 nm. The substrates were cleaned with an alkaline solution and IPA before UV-ozone treatment was applied; these cleaning procedures are described in

detail in section 2.2.4. Again, for the sake of reproducibility and simplicity, as well as the exclusion of any additional interactions, no surface treatment was applied to the gate oxide.

PBTTT-C16 was dissolved in dichlorobenzene (7.5 mg/mL) at 100 °C. The solution was spin cast onto the substrates in a spin coater with nitrogen purge. The speed was set at 1500 rpm and the spin time was 60 seconds for each sample. The substrates were annealed at 95 °C for 45 minutes in vacuum. Gold was thermally evaporated through shadow masks in high vacuum of 5 x 10^{-7} Torr. The deposition rate was roughly 0.03 nm/s. The channel dimensions of the devices were 5 µm (length) by 1000 µm (width). Each substrate comprised 20 OFETs. Solution preparation and deposition, substrate annealing, gold deposition, as well as all device measurements were conducted under either dimmed yellow light or in the dark.

7.3.3. Saturated vapour pressure calculation

The saturated vapour pressure (p_{sat}) values at room temperature were calculated by the application of a simple linear regression fit to the vapour pressure versus temperature data taken from the literature [168], as shown in Figure 7-11. The intersection of each fit and the room temperature line yields the p_{sat} of each analyte.

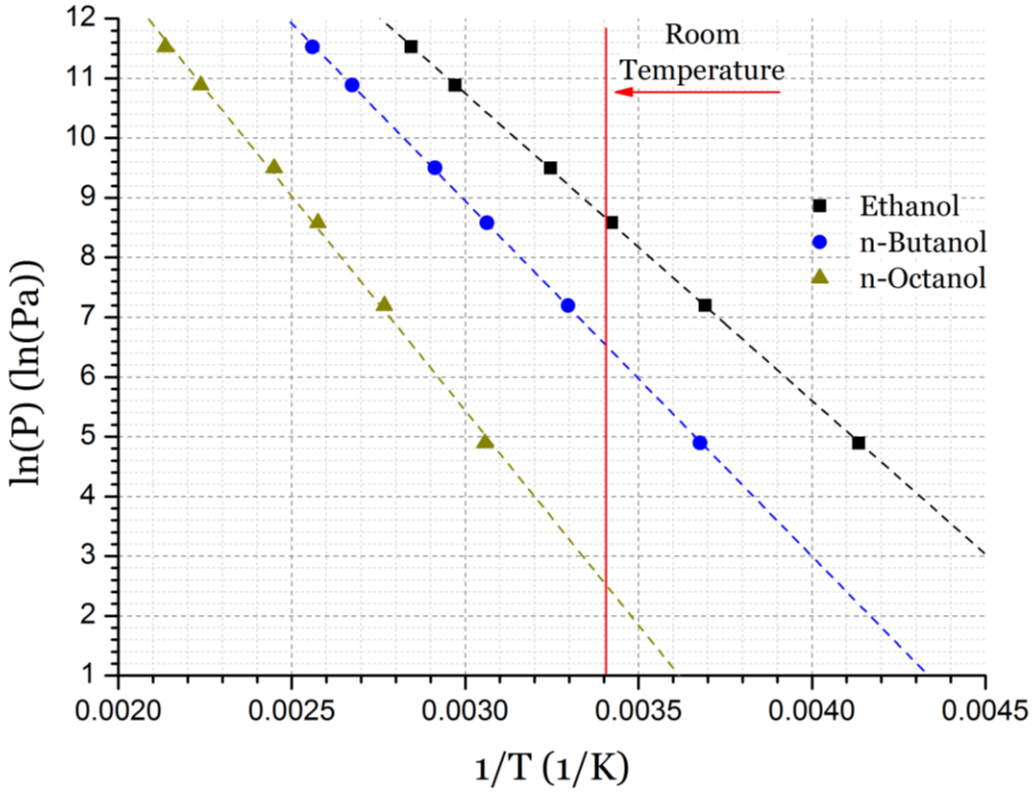

Figure 7-11 – Arrhenius-like plot of vapour pressure versus T^{-1} for the three alcohols used in quantitative exposure measurements. The data points are taken from the literature [168]. The simple linear regression fits to each data set are shown with dashed straight lines. The room temperature (20 °C) is indicated by the vertical red line.

7.3.4. Sensitivity to ethanol

Ethanol (C_2H_6O) was the smallest alcohol molecule used for vapour sensing tests on PBTTT OFET sensors. Ethanol (EtOH) has a molecular mass of 46.07 g/mol, a boiling point 78 °C, a density of 0.789 g/cm3 (at 25 °C) and a vapour pressure of approximately 5.6 KPa, i.e. 55188 ppm (at 20 °C) [168, 169]. This section describes the test methodology and discusses the results of these measurements.

7.3.4.1. *Test methodology*

The devices from the second batch, described in section 7.3.2 (semiconductor: PBTTT-C16, 20 devices per substrate, channel dimensions: 5 µm x 1 mm), were used for these tests; initially, they were electrically characterised in ambient conditions for the extraction of their I-V characteristics. The electrical characteristics of the devices of the second batch are discussed in section 5.5. Most of the devices were found doped in the initial tests.

The fully automated characterisation system, discussed in section 4.3, was used to carry out the measurements discussed here. Prior to the controlled exposure measurements, the sensors were placed in a chamber with constant nitrogen flow for extended periods of time while their electrical performance was being monitored. Figure 7-12 and Figure 7-13 show the trends of saturated drain current (I_{on}) and off-state (I_{off}) current for 3 days of continuous measurements. Doping effects were found to get mitigated over the course of the test as I_{off} decreased dramatically, showing a drop from 200 nA to 65 nA, i.e. 67.5% decrease, after 37 hours and remained at this level for the rest of this preconditioning stage. Due to the dependence of I_{off} on the doping of the semiconductor by extrinsic factors, such as the presence of impurities or humidity [165, 166], it can be assumed that doping effects were annihilated before the beginning of the exposure tests.

The analyte and the sensor were kept at room temperature. The saturated vapour delivery line was mixed with the pure nitrogen line before being fed into the chamber. The selected mixing ratios were 5%, 15% and 45%, which correspond to approximately 2750 ppm, 8250 ppm and 24750 ppm of ethanol in nitrogen, respectively.

The sensor was exposed to the lowest concentration for 5 minutes and left to recover under nitrogen purge for 25 minutes , then it was exposed to the second concentration for 5 minutes and after 20 minutes in nitrogen, it was finally exposed to the highest concentration for 4 minutes.

The automated characterisation system, described in Chapter 4, was used for the delivery of these measurements. The applied drive was a zero-offset sinusoidal signal with a peak voltage of 20 V and a frequency of 6 Hz. Measurement data were acquired every 5 seconds in bursts of 11 continuous measurements; a median filter was applied to each of those sets, i.e. each data point on the graphs represents the median value of 11 consecutive measurements.

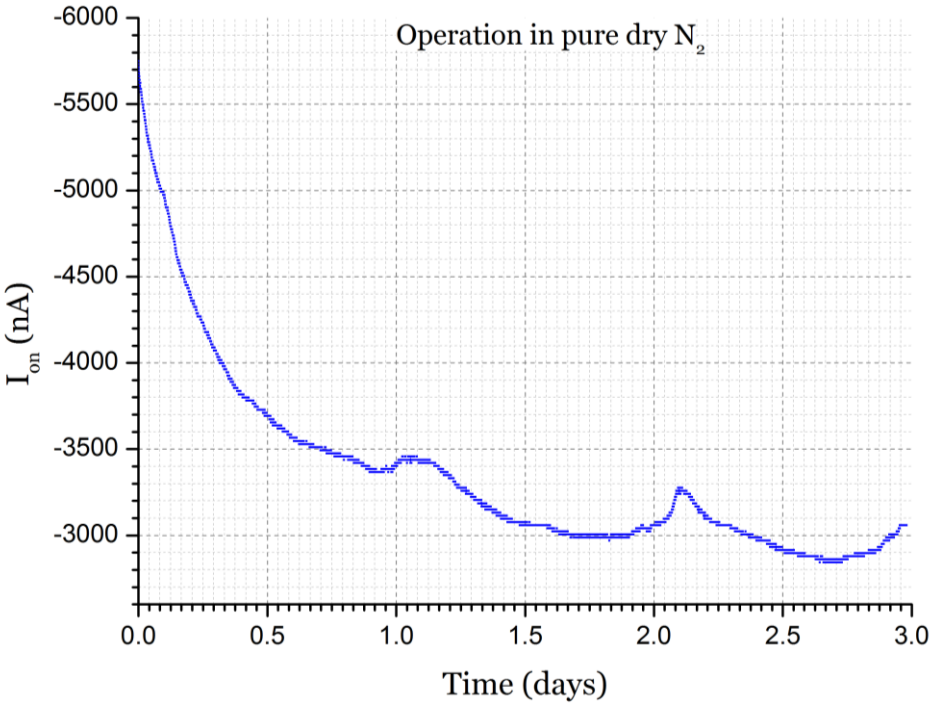

Figure 7-12 – Maximum drain current for a PBTTT OFET sensor under constant nitrogen flow over the course of 3 days. Tested with the application of a sinusoidal drive. Datapoints for Vds= Vgs = -20 V.

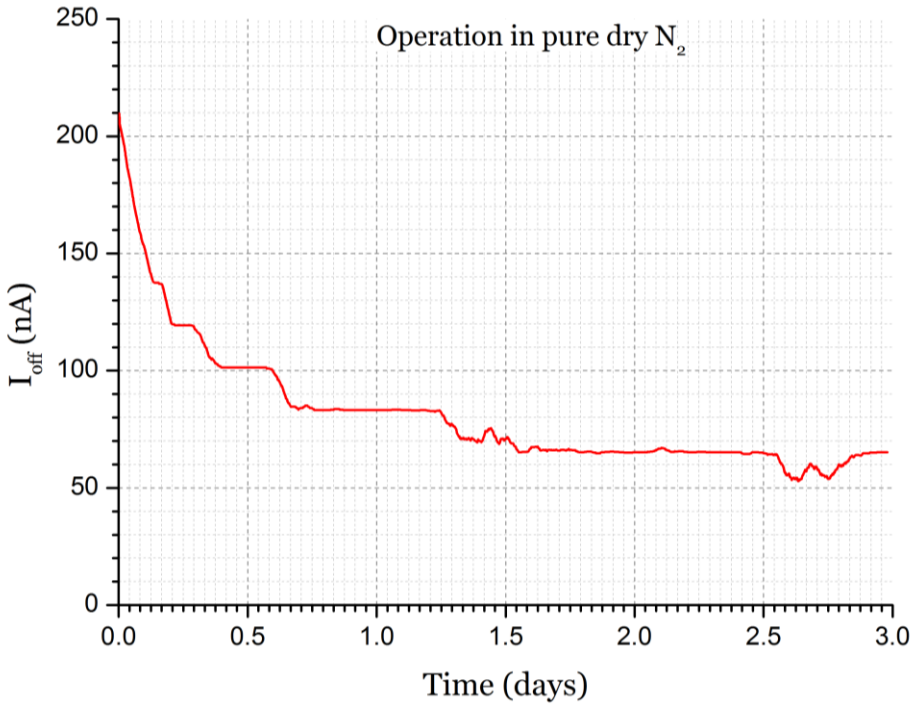

Figure 7-13 – Off-state drain current (I_{off}) for a PBTTT OFET sensor under constant nitrogen flow over the course of 3 days. Tested with the application of a sinusoidal drive. Datapoints for Vds= Vgs = =+20 V.

7.3.4.2. *Results and discussion*

The on- and off-state currents exhibited sensitivity to vapour exposure, as it can be seen in Figure 7-14 and Figure 7-15. For the two lowest concentration levels, the off-state current showed a trivial rise, but remained close to the lowest detectable level; meanwhile, the maximum drain current instantaneously decreased by -1.5 % and -5.2 %, respectively. The

initial steep drop of drain current was followed by a slow recovery during the exposure period. Immediately after the end of exposure, the drain current ramped up to higher level than that it was prior to exposure; the possible reasons for this behaviour are discussed below.

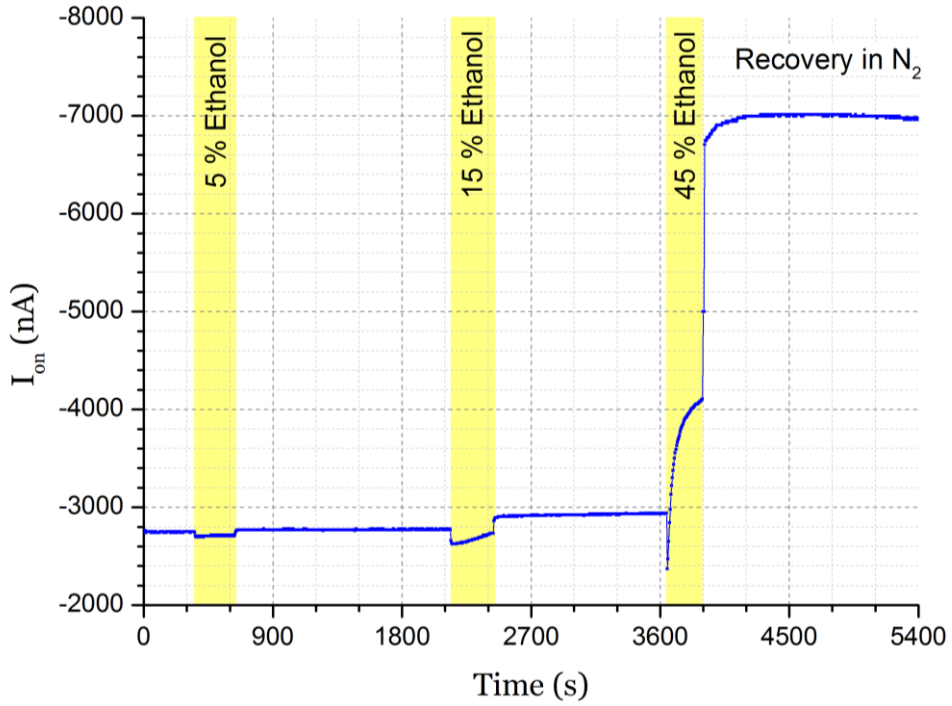

Figure 7-14 – Maximum saturated current (at Vds= Vgs = -20 V) versus time. The yellow-shaded regions indicate the vapour exposure periods; the respective mixing ratios (given in the graph) were 5% (2750 ppm), 15% (8250 ppm) and 45% (24750 ppm).

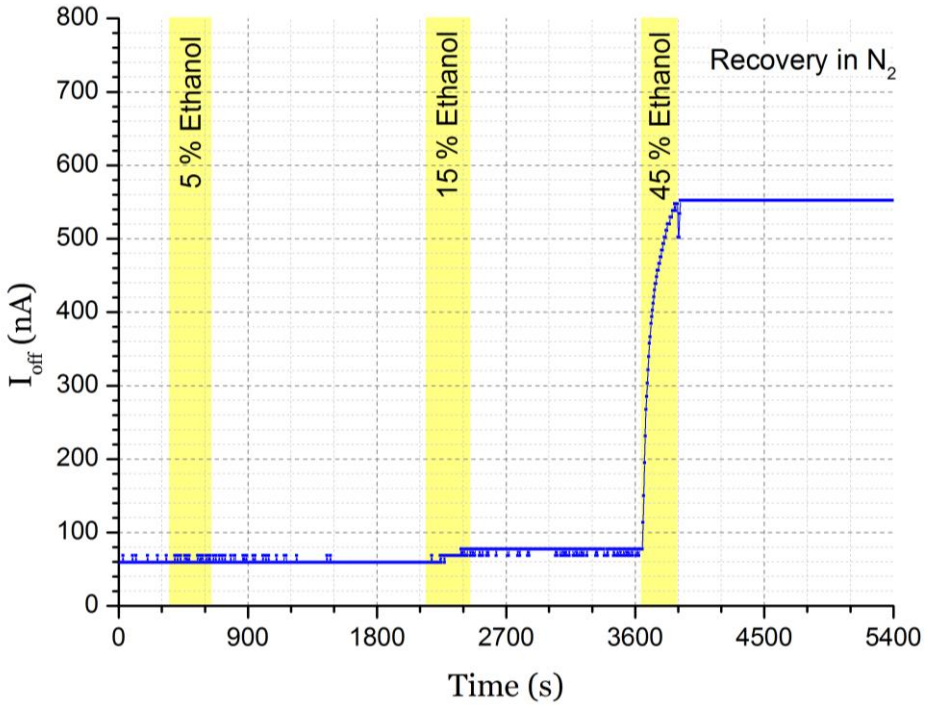

Figure 7-15 – Maximum off-state current (at Vds= Vgs = +20 V) versus time. The yellow-shaded regions indicate the vapour exposure periods; the respective mixing ratios (given in the graph) were 5% (2750 ppm), 15% (8250 ppm) and 45% (24750 ppm).

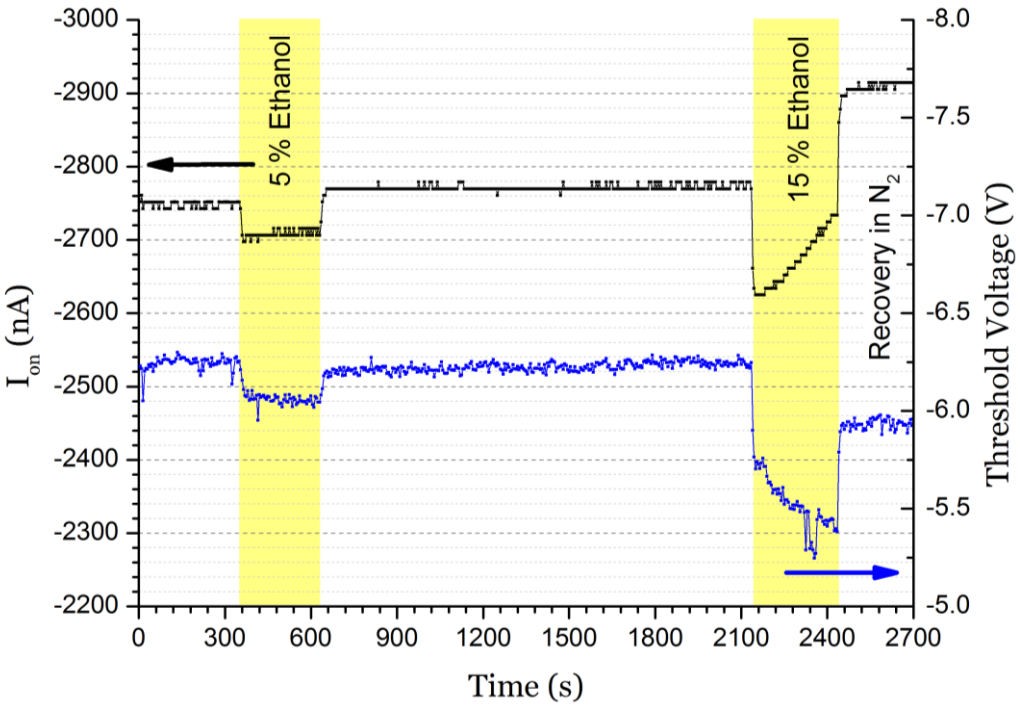

Figure 7-16 – Saturated drain current (I_{on}, black line - left y-axis) for V_{ds} = V_{gs} = -20 V and threshold voltage (V_{th}, blue line – right y-axis) for a PBTTT OFET sensor. The yellow-shaded regions indicate periods of exposure to ethanol vapour; the respective mixing rations of saturated vapour to pure nitrogen are given on the top of each shaded region. White regions indicate periods under nitrogen purge.

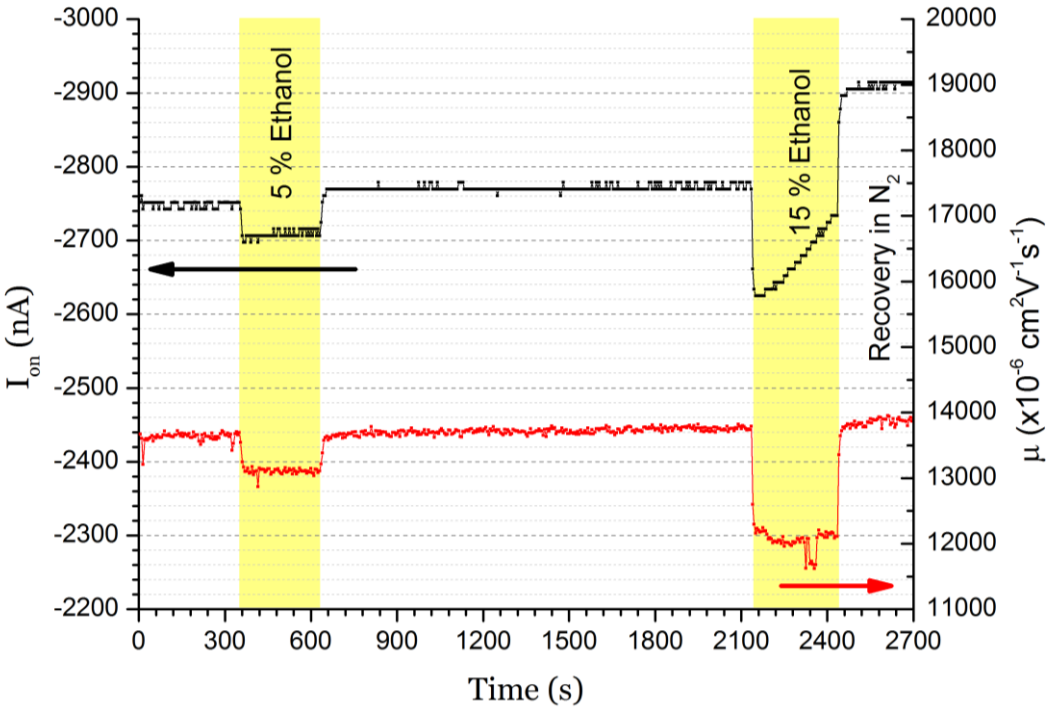

Figure 7-17 – Saturated drain current (I_{on}, black line - left y-axis) for V_{ds} = V_{gs} = -20 V and charge carrier mobility (μ, red line – right y-axis) for a PBTTT OFET sensor. The yellow-shaded regions indicate periods of exposure to ethanol vapour; the respective mixing rations of saturated vapour to pure nitrogen are given on the top of each shaded region. White regions indicate periods under nitrogen purge.

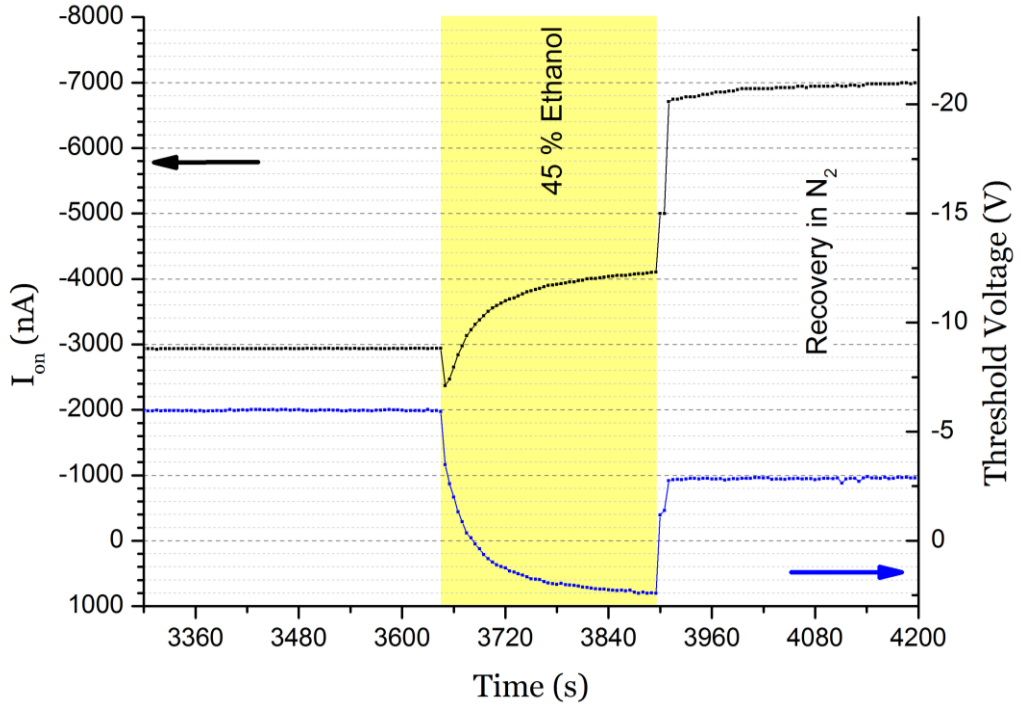

Figure 7-18 – Saturated drain current (black line – left axis) and V_{th} (blue line – right axis) for a PBTTT OFET sensor under exposure to 45% p_{sat} (24750 ppm) of ethanol in dry nitrogen.

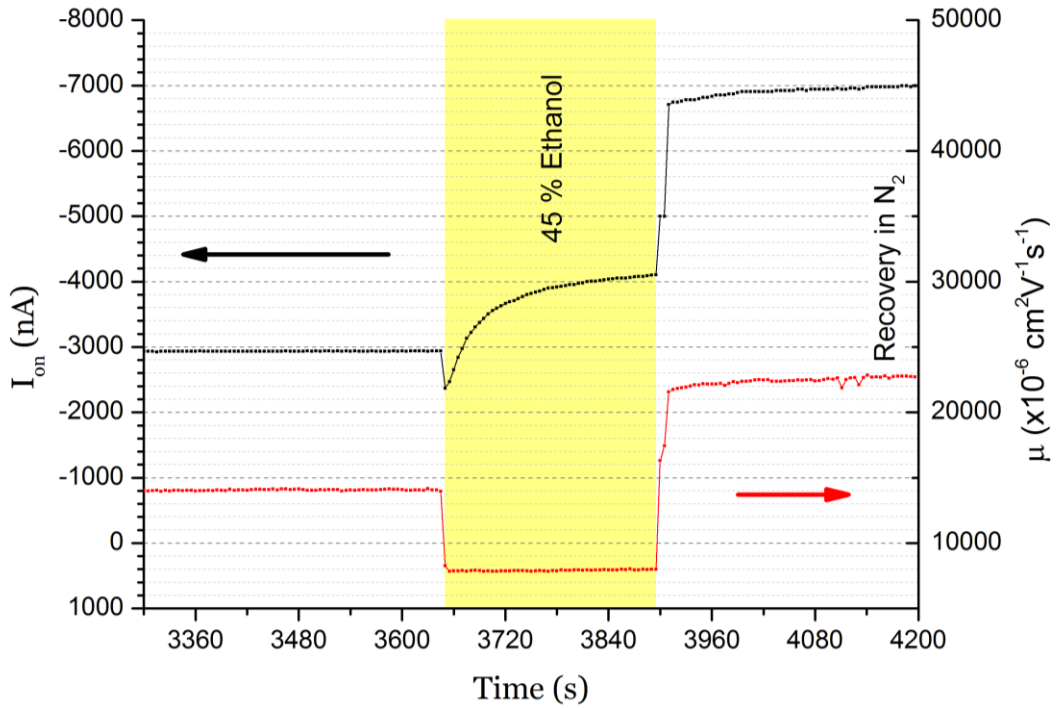

Figure 7-19 – Drain current (black line – left axis) and μ_{FE} (red line – right axis) for a PBTTT OFET sensor under exposure to 45% p_{sat} (24750 ppm) of ethanol in dry nitrogen.

In the case of the highest analyte concentration of 24750 ppm, a remarkable behaviour was observed; again, an initial steep drop of -19.3% in drain current was recorded, but this change was followed by a dramatic increase which quickly surpassed the pre-exposed state. Additionally, off-state current increase dramatically, showing an relative change of more than 700%. When analyte delivery was ceased, off-state current preserved its increased magnitude, while on-state current showed a rapid increase from 4 µA to 7 µA.

The case of ethanol constitutes a very good example of the advantages of OFETs over chemiresistors in gas sensing; moreover, it highlights the importance of real-time multiparametric characterisation. Apparently erratic single parameter, i.e. drain current, behaviours, manifested by the 'zig-zag' trends discussed above, can be rationalised by a closer look at the multiparametric analytical data. The disentanglement of multiple independent OFET parameters, such as threshold voltage (V_{th}) and mobility (μ_{FE}), can shed some light on the actual interactions that occur under exposure.

Figure 7-16 and Figure 7-17 clearly show the V_{th} and μ_{FE} changes of the OFET sensor under the exposure to the two lowest concentrations of ethanol. Both parameters are affected; the modulus of V_{th} is gradually reduced, while mobility immediately drops to a lower level which is preserved throughout the exposure period. According to the saturated drain current ($I_{D,sat}$) notions, as described by eq. (2.3), it can be easily deduced that these trends induce opposite results on $I_{D,sat}$; the change in V_{th} should result in an increase in $I_{D,sat}$, whereas drain current should fall with μ_{FE} due to their proportionality. Consequently, the instant mobility change can justify the initial steep drop of drain current. However, the slower change in V_{th} slowly reversed the drain current trend; this resulted in the $I_{D,sat}$ increase, which followed the swift initial reduction.

Upon analyte delivery termination, mobility quickly recovered and returned to a similar level to that of its pre-exposed state; on the contrary, V_{th} only showed a partial recovery. The overall result of these two separate changes is the steep increase in drain current which occurred immediately after the end of each exposure.

In the case of the highest analyte concentration exposure, the effects were remarkably stronger. Figure 7-18 and Figure 7-19 illustrate these results. Again, mobility showed a step-like response with a quick drop of roughly 50%. The effects on V_{th} were particularly striking; the calculations indicate a transition from enhancement-mode to depletion-mode, as V_{th} becomes positive. This massive V_{th} change quickly caught up with the mobility drop and, finally, the drain current surpassed its pre-exposed magnitude within seconds under exposure. When analyte delivery was terminated, V_{th} quickly became negative but only partially recovered; remarkably, μ_{FE} rose to a value which was roughly three times greater than the exposed state and double the pre-exposed state magnitudes. As a result, drain current increased to a high level which was roughly 230% of its pre-exposed state. Both off-state and on-state currents remained at the same level until the end of test, three hours after the end of the last exposure.

It is worth noting that, due to the attributes of the electrical characterisation system, discussed in section 4.1, the V_{th} and μ_{FE} calculations are based on saturation region notions, i.e. based on the assumption that the OFET under test is a normally-on device (enhancement-mode). If the device becomes of depletion-mode, this assumption no longer holds true; this fact may introduce some error in the calculations. Moreover, the presence of an ohmic contribution due to the doping of the semiconductors, can introduce some small error as no off-state current correction was applied to the results. However, regardless of any possible inaccuracies, the observed trends of V_{th} and μ_{FE} remain valid. The impact of doping on the calculations of V_{th} and μ is extensively discussed in section 4.2.

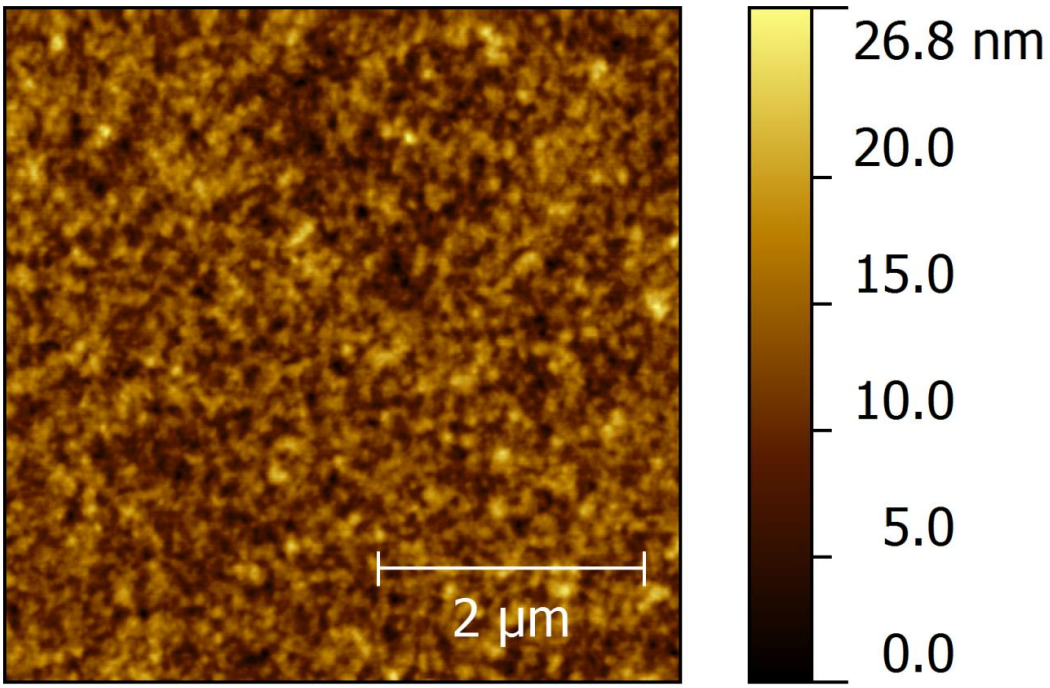

Figure 7-20 – AFM image of the surface of a PBTTT OFET before exposure to any analyte. Root mean square (RMS) roughness: 3.34 nm.

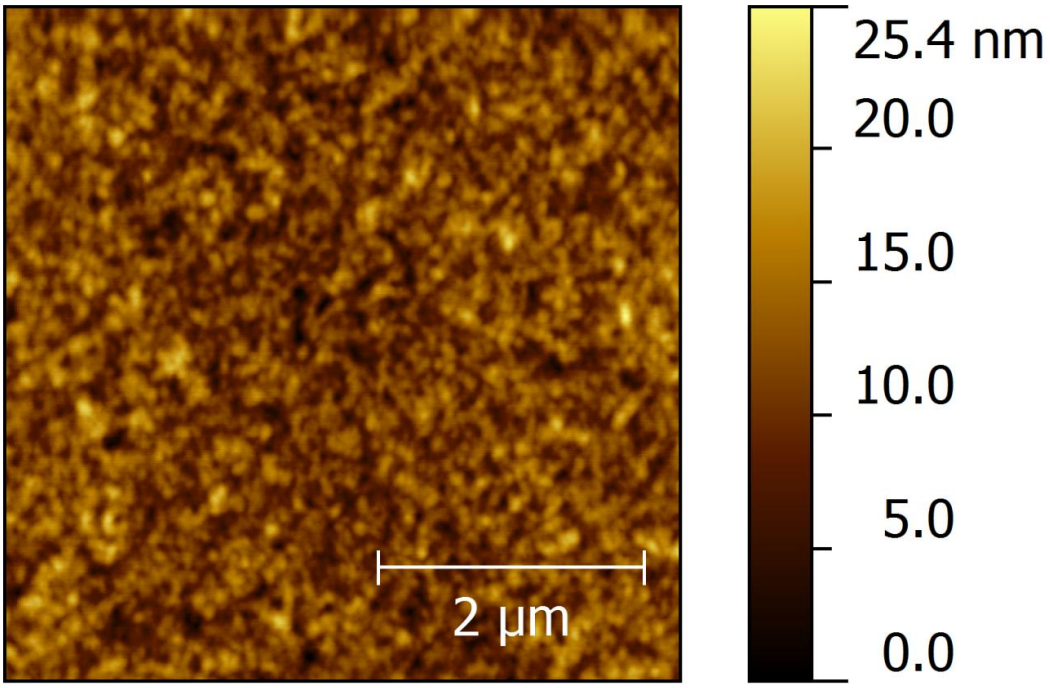

Figure 7-21 – AFM image of the surface of an PBTTT OFET after exposure to ethanol vapour. Root mean square (RMS) roughness: 2.95 nm.

From the effects on V_{th}, it can be safely deduced that due to their small dimensions, ethanol molecules can penetrate through the PBTTT grains and reach the semiconductor-dielectric interface. The presence of polar –OH groups on both the SiO_2 surface [170], and the ethanol molecules can lead to the development of strong hydrogen bonds between them, which can result in threshold voltage changes.

A previous report on ethanol sensing with pentacene OFETs suggests that the polar molecules of the analyte introduce trap sites at the grain boundaries and effectively reduce the mobility of carriers by hindering them from hopping between two adjacent semiconductor grains [13].

This reasoning could explain the observed initial steep drops of μ_{FE} under exposure. However, the enhanced post-exposure mobility remains to be justified; the irreversibility of this change, even after prolonged exposure to a dynamic nitrogen atmosphere, may constitute an indication of permanent changes in the semiconductor film. In another study, Hüttner *et al.* have reported mobility enhancement of *perylene bisimide acrylate (PPerAcr)* polymer films after their exposure to chloroform vapour [171]; it was found that the morphology of the film was affected by the solvent vapour. This treatment is referred to as *solvent vapour annealing* and in this case, it could provide an explanation of the observed mobility enhancement after exposure. In the work presented here, the AFM images of the surfaces of unexposed and exposed PBTTT films, shown in Figure 7-20 and Figure 7-21, reveal a small decrease in surface roughness after exposure to ethanol vapour, with the root mean square (RMS) value dropping from 3.34 nm to 2.96 nm; however, no significant changes in the grain size distribution could be measured. Considering that these images visualise only the surface of the films, this small change in surface roughness provides and indication of possible solvent annealing, but cannot safely confirm any changes in the grain formation due the film exposure to ethanol vapour.

7.3.4.3. *Conclusion*

The selection of ethanol as an analyte for the exposure of PBTTT OFET sensors turned out to be a very good example of real-time multiparametric characterisation using the I-V converter method, discussed in detail in Chapter 4. The automatically calculated measurement data clearly disentangled the trends of individual parameters, i.e. the step-like responses of μ in conjunction with the exponential changes of V_{th}; this provided enough evidence to explain the apparently erratic drain current behaviour during the periods of exposure and recovery.

The limit of detection (LoD) lies below the lowest tested concentration of 2750 ppm. The magnitude of the effects increased with increasing analyte concentration. For all the applied concentrations, mobility exhibited instantaneous step-like drops to values that were preserved throughout each exposure period; this fact justifies the steep initial drop of drain current in all cases. Interestingly, the relative change in mobility was found to be proportional to the analyte concentration.

Meanwhile, the modulus of threshold voltage showed an exponential decay which induces the opposite effects on drain current; the initial drop in drain current was followed by a slower increase. Upon the end of exposure, mobility rapidly increased and reached a new plateau at a level slightly higher than its pre-exposure value, while threshold voltage partially recovered; the combination of these two separate phenomena resulted in a steep rise of drain current to higher levels than the pre-exposure ones. Off-state current (I_{off}) was also affected; an increase was recorded during each exposure period. Both saturated drain current and off-state current showed irreversible changes as they preserved their increased values during all recovery periods, even after 3 hours after the last exposure was ceased.

7.3.5. Sensitivity to octanol

The largest alcohol molecule used for vapour sensing tests on PBTTT OFET sensors was *n-octanol ($C_8H_{18}O$)*. It has a molar mass of 130.23 g/mol, a boiling point 196 °C, a density of 0.827 g/cm^3 (at 25 °C) and a vapour pressure of approximately 12 Pa, i.e. 118 ppm (at 20 °C) [168, 172]. This section describes experimental procedure for the vapour exposure tests and presents their results.

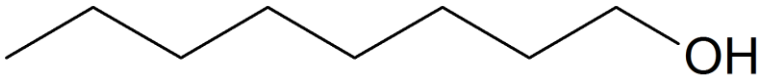

Figure 7-22 – The n-octanol molecule

7.3.5.1. *Test methodology*

The test methodology was very similar to the one previously described in section 7.3.4.1; a substrate from the second batch of OFET sensors, as described in section 7.3.2 (semiconductor: PBTTT-C16, 20 devices per substrate, channel dimensions: 5 µm x 1 mm), was used in the same test rig; the device preparation is described in section 7.3.2 and the gas-exposure system in section 7.1.1. Three sensors were characterised simultaneously using the relay-based multiplexer described in section 7.1.3.

The pre-conditioning stage was much shorter than that of the ethanol-vapour-exposure tests; the devices were measured under nitrogen purge for 30 minutes prior to the first analyte exposure. Both the saturated drain current (I_{on}) and the off-state current (I_{off}) decreased during this stage; however, I_{off} remained at a measurable magnitude. As discussed in section 7.3.4.1, in that case of PBTTT OFET sensor pre-conditioning, I_{off} was found to get eliminated after several hours under nitrogen.

The analyte and the sensor were kept at a room temperature of 20 °C. The saturated vapour delivery line was mixed with the pure nitrogen line before being fed into the chamber. The selected mixing ratios were 1%, 10%, 30% and 60%, which correspond to approximately 1.2 ppm, 12 ppm, 35 and 70 ppm of n-octanol in nitrogen, respectively.

The sensors were exposed to the three lowest concentrations (1%, 10% and 30%) for 5-minute intervals and finally to the highest concentration (60%) for 20 minutes approximately. They were left to recover under nitrogen purge overnight.

The applied drive was a zero-offset sinusoidal signal with a peak voltage of 20 V and a frequency of 6 Hz. Measurement data were acquired every 5 seconds in bursts of 11 continuous measurements; a median filter was automatically applied to each of those sets, i.e. each data point on the graphs represents the median value of 11 consecutive measurements.

7.3.5.2. *Results and discussion*

Figure 7-23 and Figure 7-24 show the saturated drain current (I_{on}) and off-state current (I_{off}), respectively, of the three sensors versus time. The I_{on} of all three sensors showed a steady drop during the pre-conditioning stage which carried on even after I_{off} values got stabilised. For the first three exposure levels (1% to 30% or 1.2 ppm to 35 ppm), both I_{on} and I_{off} appeared unaffected; the trend of I_{off} remained flat while I_{on} continued to drop at a steady pace.

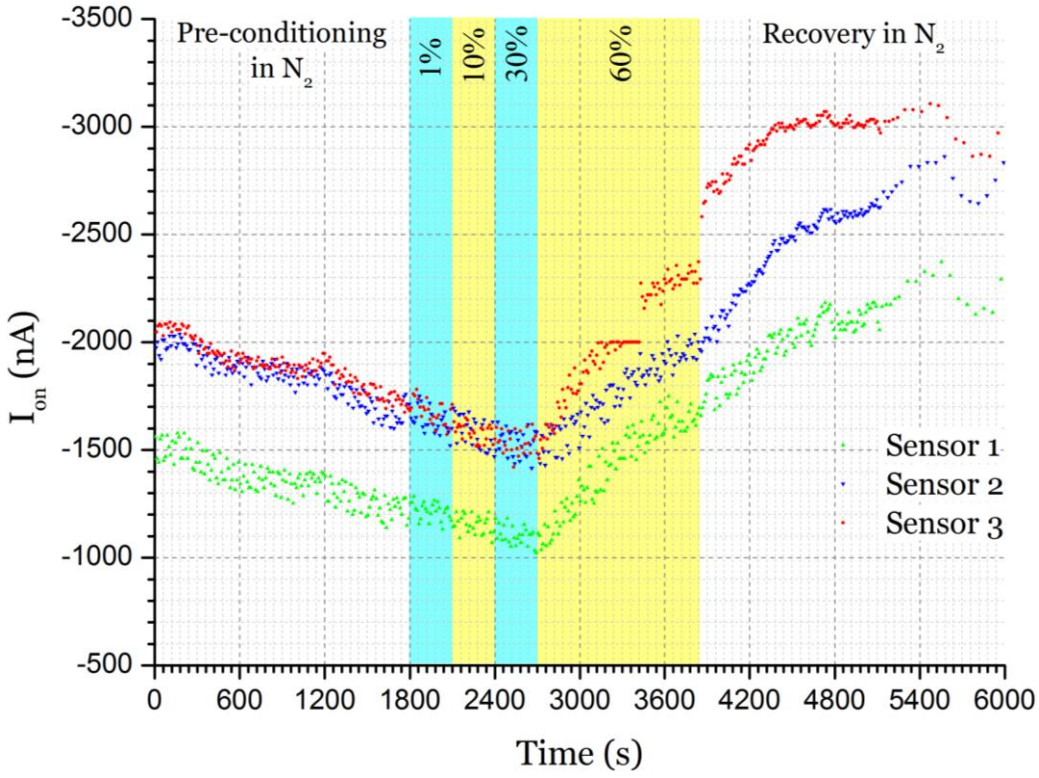

Figure 7-23 – Saturated drain current (I_{on}) at V_{ds} = V_{gs} = -20 V of three PBTTT OFET sensors versus time. The colour-shaded regions represent periods of exposure to different ethanol vapour concentrations. The respective mixing ratios of saturated ethanol vapour to pure nitrogen are given on the top of each region.

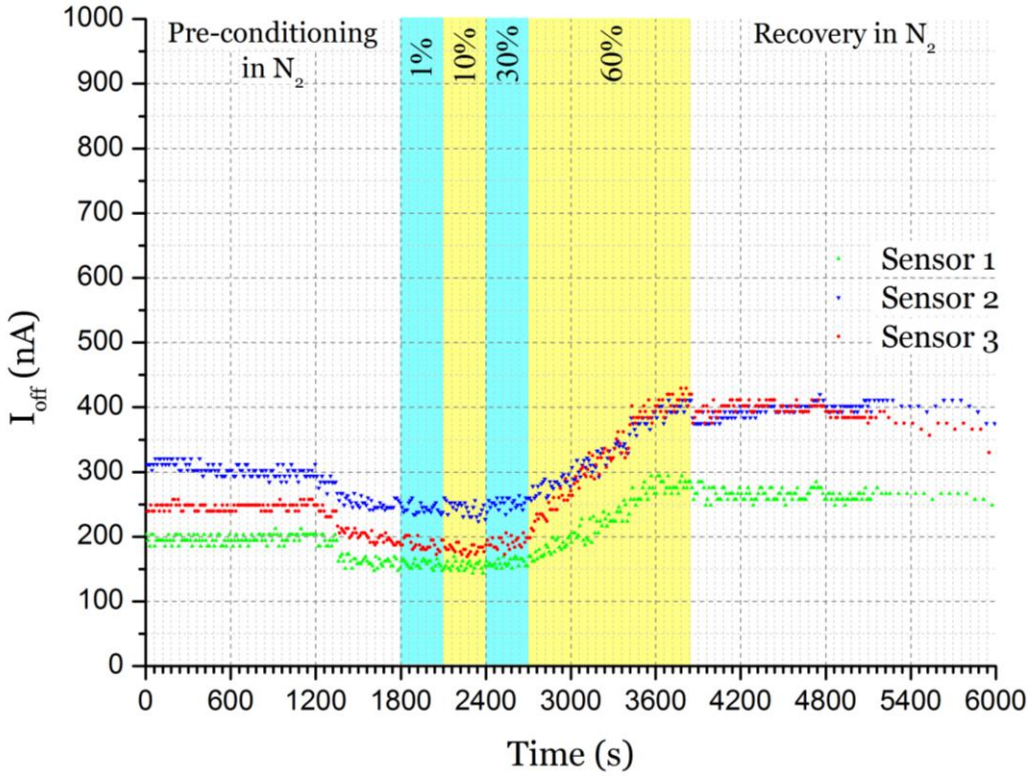

Figure 7-24 – Off-state current (I_{off}) at V_{ds} = V_{gs} = +20 V of three PBTTT OFET sensors versus time. The colour-shaded regions represent periods of exposure to different ethanol vapour concentrations. The respective mixing ratios of saturated ethanol vapour to pure nitrogen are given on the top of each region.

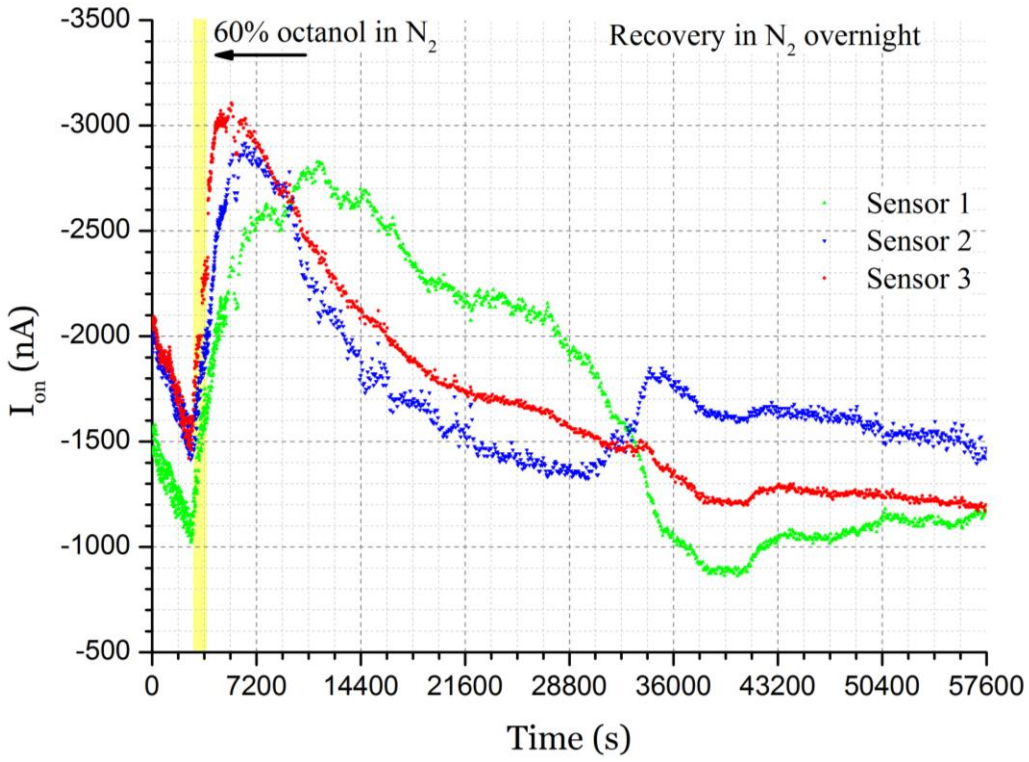

Figure 7-25 – Saturated drain current (I_{on}) at V_{ds} = V_{gs} = -20 V of three PBTTT OFET sensors versus time. The yellow-shaded region represents the period of exposure ethanol vapour with a concentration of 60% p_{sat} (70 ppm). The white regions indicate periods under pure nitrogen purge. The recovery trends of the three sensors varied significantly.

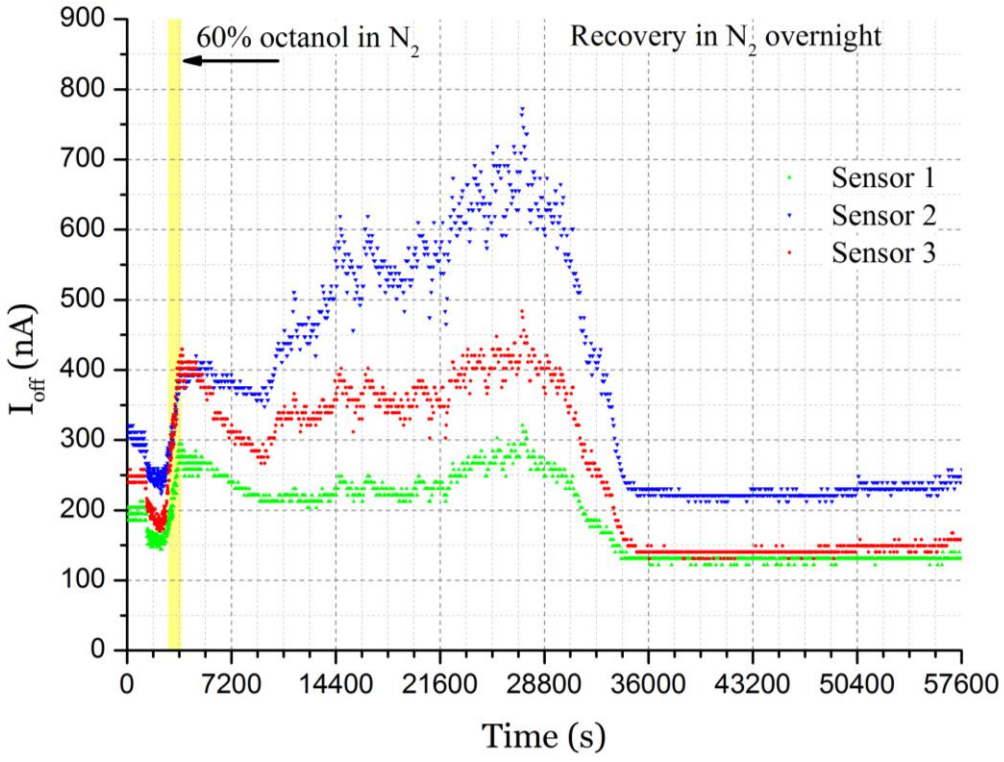

Figure 7-26 – Off-state drain current (I_{off}) at V_{ds} = V_{gs} = +20 V of three PBTTT OFET sensors versus time. The yellow-shaded region represents the period of exposure ethanol vapour with a concentration of 60% p_{sat} (70 ppm). The white regions indicate periods under pure nitrogen purge. The recovery of sensor 2 differed significantly from those of the other two sensors. All sensors reached equilibrium after several hours in nitrogen.

Doubling the analyte concentration to a 60% p_{sat} (70 ppm) had a strong impact on both current quantities; I_{on} exhibited a substantial increase, ranging from +37.0% (sensor 2) to +63.9% (sensor 1), while I_{off} had showed an even larger change, ranging from +84.4% (sensor 1) to +112.1% (sensor 3).

The sensors were left under nitrogen purge for another 15 hours while their electrical characteristics were being calculated and recorded; Figure 7-25 and Figure 7-26 respectively show the I_{on} and I_{off} current trends over the exposure periods and this extended recovery period. The behaviour of both quantities does not allow for the extraction of straightforward conclusions. It was observed that the I_{on} of all sensors kept rising for several minutes after the analyte exposure was ceased; the I_{on} of sensor 1 reached a maximum after 2 hours. The results of I_{off} showed an even longer rising trend; the values for all sensors were increasing for approximately 7 hours. However, after 9 hours all three I_{off} values dropped and remained at relatively low level until the end of test. On the contrary, I_{on} fluctuations carried on for 10 hours since the beginning of the recovery period, before all three values finally came to equilibrium.

More detailed information on the sensitivity of the sensors can be extracted from Figure 7-27 and Figure 7-28, which respectively show the evolution of V_{th} and μ with time. n-octanol vapour was not found to induce abrupt drops in μ, which comes in contrast to the effects of ethanol vapour, presented in section 7.3.4.2. For the three lowest analyte concentrations of 1% p_{sat} (1.2 ppm), 10% p_{sat} (12 ppm) and 30% p_{sat} (35 ppm), μ exhibited a steady falling trend which, in conjunction with the stable V_{th} values calculated throughout these periods, explains the simultaneous I_{on} decrease for all sensors.

For the highest analyte concentration of 60% p_{sat} (70 ppm), the μ trend was reversed for all three devices; the values increased resulting in an increase in the respective I_{on} values. V_{th} was also found susceptible to high vapour concentration; two of the sensors showed a moderate drop of the modulus of V_{th} towards a normally-on behaviour, while the value for sensor 3 dropped to zero. These calculated V_{th} changes could be thought as artefacts of the automated measurement algorithm due to presence of ohmic contribution (doping), which manifests itself in the substantial increase of I_{off} for this analyte concentration, as previously discussed. A detailed discussion on the potential calculation errors introduced by doping is given in section 4.2.

7.3.5.3. *Conclusion*

The limit of detection (LoD) of n-octanol vapour using PBTTT OFET sensors of the given characteristics was found to lie between 35 and 70 ppm. No response was detected for exposure to concentrations below 35 ppm, while the charge carrier mobility was found to steadily drop during these periods; this fact can be attributed to the relatively short, 30-minute-long, pre-conditioning period which did not allow for completely drying out the chamber and purging any pre-existent dopants in the semiconductor film [49, 156-159, 173].

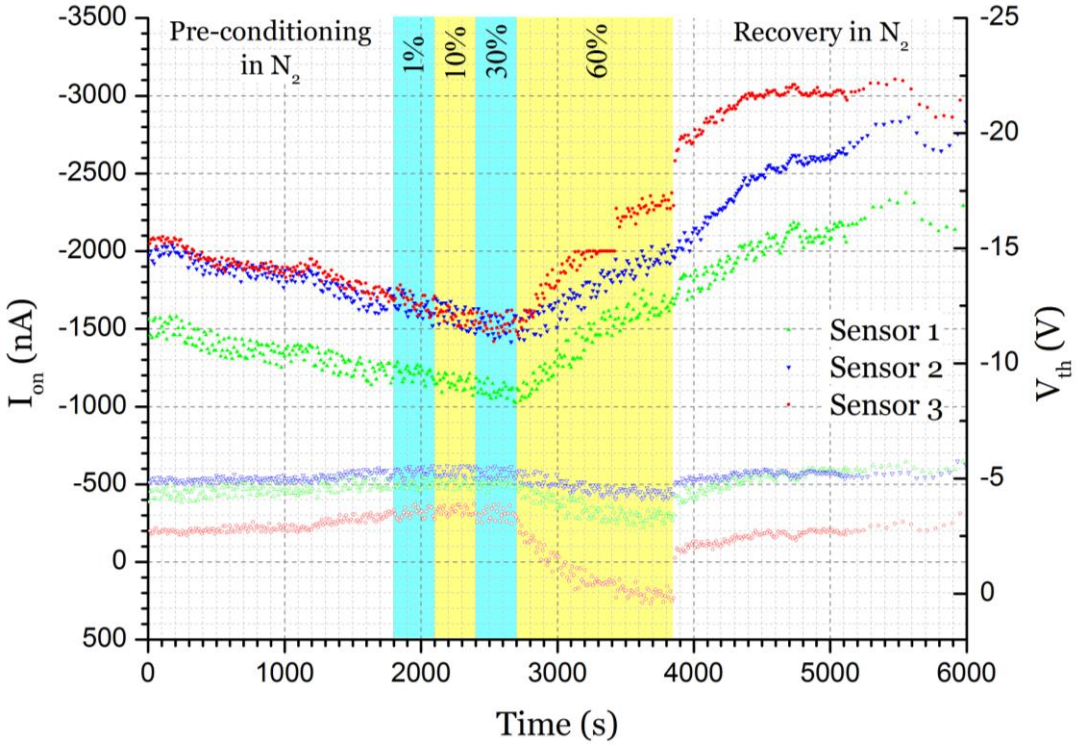

Figure 7-27 – Saturated drain current (I_{on}) at V_{ds} = V_{gs} = -20 V for three PBTTT OFET sensors (top three series, left y-axis), and the threshold voltage (V_{th}) of the same sensors (bottom three series, right y-axis) versus time. Colour-shaded regions indicate the periods of exposure to n-octanol vapour; the respective concentrations appear on the top of each region: 1% p_{sat}, 10% p_{sat}, 30% p_{sat} and 60% p_{sat} (70 ppm). In the region between t = 3150 s and t = 3500 s, the readings from Sensor 3 reached a plateau of -2000 nA; this is a measurement artefact due to fact that the converted output voltage (V_{out}) for the given feedback resistance was out-of-scale. The measurement data returned to their actual values when the oscilloscope scale was manually changed, at t = 3500 s.

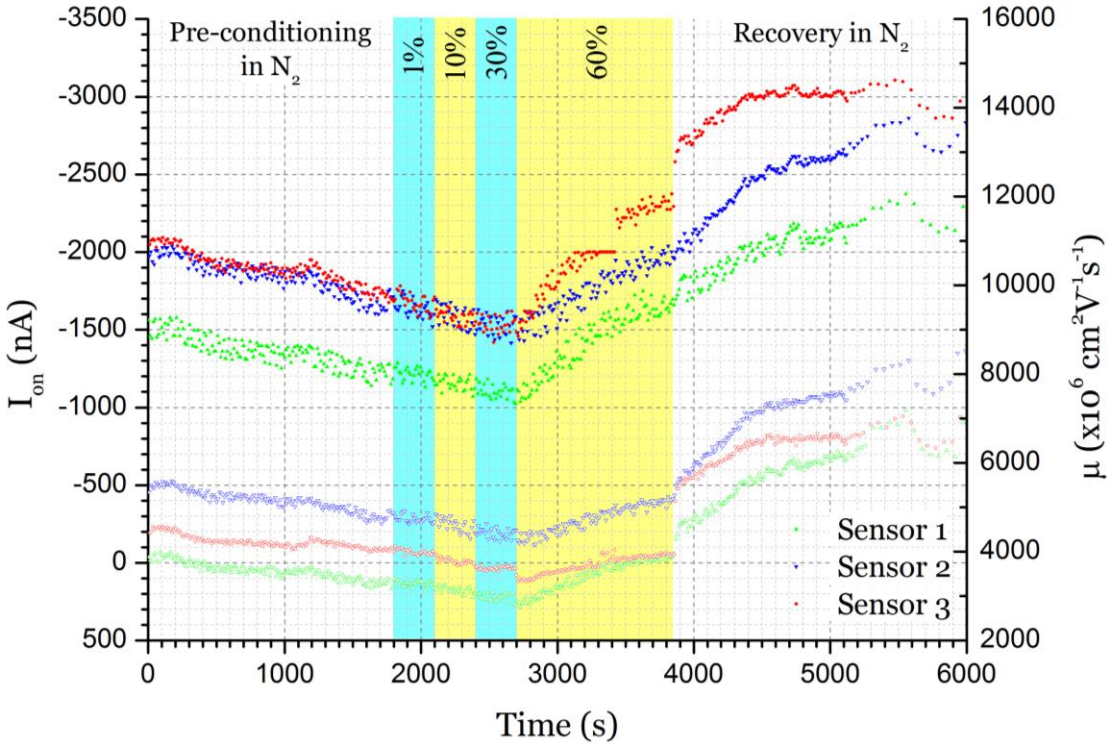

Figure 7-28 – Saturated drain current (I_{on}) at V_{ds} = V_{gs} = -20 V for three PBTTT OFET sensors (top three series, left y-axis), and the carrier mobility (μ) of the same sensors (bottom three series, right y-axis) versus time. Colour-shaded regions indicate the periods of exposure to n-octanol vapour; the respective mixing ratios appear on the top of each region, namely: 1% p_{sat}, 10% p_{sat}, 30% p_{sat} and 60% p_{sat} (70 ppm).

Under exposure to 70 ppm, carrier mobility increased and, consequently, it induced a rise in the saturated drain current. The off-state current was also affected showing a substantial increase. Threshold voltage values were also found to change, exhibiting a drift towards a normally-on behaviour; however, the accuracy of these calculated values might have slightly been compromised by the highly doped profile, which the enhanced off-state current indicates.

As it can be seen in Figure 7-23 to Figure 7-28, the performance and sensing responses of OFET sensors fabricated with the same methodology and exposed to the same conditions can vary significantly. This fact underscores the need for comparative measurements, which can evaluate the consistency and reproducibility of this kind of sensors; this need is satisfied with this system as multiple sensors can be exposed to the same conditions and characterised simultaneously.

7.3.6. **Sensitivity to butanol**

The vapour of *n-butanol ($C_4H_{10}O$)* was used as an analyte on PBTTT OFET sensors. n-butanol (BuOH) has a molar mass of 74.12 g/mol, a boiling point of 116-118 °C, a density of 0.81 g/cm^3 (at 25 °C) and a vapour pressure of approximately 665 Pa, i.e. 6560 ppm (at 20 °C) [168, 174]. In this section, a description of the experimental procedure for the delivery of quantitative measurements on PBTTT OFET sensors exposed to n-butanol vapour is given along with a discussion on their results. The device fabrication and the tests described in this section were carried out in the laboratories of the *Chemistry Department* of the *University of Bari*, Italy. Credits to other contributors are given in the

Acknowledgements.

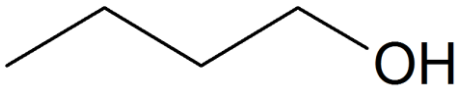

Figure 7-29 – The n-butanol molecule

7.3.6.1. ***Test methodology***

The device under test was a device built on a substrate from the first batch of OFETs, as described in section 7.3.2 (semiconductor: PBTTT-C14, channel dimensions: 200 µm x 4 mm). The sensor under test was electrically contacted by three *Cascade-Microtech PH100* probe positioners with tungsten needles. The electrical characterisation was carried out by an *Agilent 4155C* semiconductor parameter analyser and the I-V converter system, described in detail in Chapter 4.

All device preparation and measurements took place in either dark or dimmed light conditions. The analyte was placed into a bubbler immersed into a thermostatically-controlled bath filled with mixture of water with an antifreeze agent. The gas flow and the mixing ratios were regulated by two mass-flow controllers (*Brooks Instruments 5820s*) of different maximum flow rates (500 ml/min for the pure gas and 100 ml/min for the analyte line); the controllers were connected to a computer via a serial protocol connection. The gas delivery and mixing were implemented in a similar fashion as the one described in section 7.1.1; the first of the controllers regulated the flow of pure nitrogen, while the second one controlled the flow of nitrogen, which was fed into the bubbler and mixed with the saturated vapour of it. The two lines were mixed at a T-junction; the final mixture was then delivered onto the surface of the substrate through a narrow plastic pipe with an open end. The distance between the open end of the pipe and the surface of the substrate was kept to a minimum. The sensor and the contacting probes were not enclosed in a gas chamber as in the previously described experiments; instead, they were placed on a stage lying on the surface of a fume cupboard.

The long comparative measurements between the two characterisation systems were conducted on the same sensor on different days. From the time of its fabrication and between the tests, the substrate was stored in dark ambient conditions. For consistency, the same light and temperature conditions, analyte vapour concentration and exposure/recovery pattern were chosen for all tests. For the tests conducted using the semiconductor parameter analyser, standard transfer measurements were taken every 3 to 4 minutes; a rising and a

falling gate voltage sweep (from +30 V to -30V and then back to +30V) for a constant drain bias of -30V were applied. For the tests conducted using the I-V converter system, a zero-offset sinusoidal drive with V_0 = 30 V and f = 16 Hz was applied. All measurement data were manually exported by saving the oscilloscope data in 4-minute-long intervals.

A pre-conditioning period under nitrogen preceded all exposure tests; the sensor was characterised until the drain current came to equilibrium, thus the length of this period was not exactly the same for all experiments, but exceeded one hour in all cases. The analyte and the room temperature were set at 20 °C. The saturated vapour delivery line was mixed with the pure nitrogen; the selected mixing ratio was 30%, which corresponds to approximately 2000 ppm. The same sequence of long exposure/recovery periods was applied in all tests: a long pre-conditioning period, two sets of 30-minute-long periods of exposure to analyte vapour and equally long periods of recovery under nitrogen, and a final 20-minute-long exposure followed by another recovery period.

7.3.6.2. *Results and discussion*

The device under test showed similar responses in multiple tests when exposed to the same concentration of n-butanol vapour, even several days after their fabrication. Using both the semiconductor parameter analyser and the I-V converter system over a period of two weeks, the response of the sensor, in terms of saturated drain current ($\Delta I_{on}/I_{on,0}$), was found to fall within a range from -25 % to -34 %. The off-state current (I_{off}) was found to be insensitive to analyte exposure in all experiments.

Analysis of the measurement data makes it evident that this drop was the result of two different changes; a drop in mobility (μ) and an increase in the modulus of threshold voltage (V_{th}). An example of converted transfer curves indicating the calculated parameters is shown in Figure 7-30. It is worth mentioning that the manual conduct of measurements does not allow for the analysis of the immediate responses at the onset of the analyte vapour, as it was done in sections 7.3.4.2 and 7.3.5.2.

During the recovery periods, the saturated drain current (I_{on}) showed a fast recovery. However, the 'recovered' state was found to be dependent on the characterisation method; the DC measurements taken by the Agilent analyser showed enhanced I_{on} levels during recovery, as compared to their respective pre-exposure values. On the contrary, the measurements taken under continuous AC operation using the I-V converter system showed a partial recovery of I_{on} under nitrogen. As a control experiment, another set of measurements using the I-V converter system was taken; in this case the AC drive was applied for only a few seconds before and after the data acquisition process, rather than being applied continuously over the course of the test. In this case, the sensor showed a better recovery, as compared to its performance under continuous drive; this behaviour applied to all but one instances, as can be seen in the comparative Figure 7-31.

Looking back at Figure 7-30, the fact that, under AC drive, the drain current only partially recovers can be explained by the irreversible change in V_{th}; in fact, the value of V_{th} was found to be slightly greater during recovery, whereas μ recovered almost completely. Considering that V_{th} is largely dependent on the interactions at the semiconductor-interface, the slow

responses of V_{th} can again be attributed to the slow diffusion of the analyte molecules through the grains of the semiconductor.

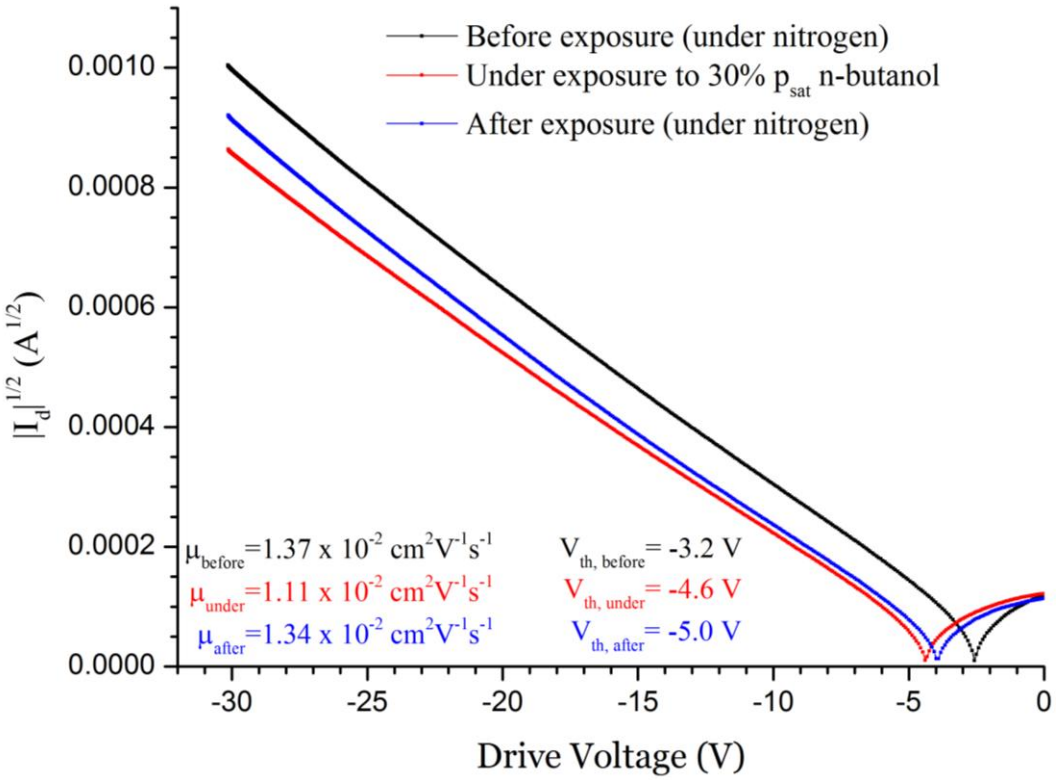

Figure 7-30 – Converted transfer curves from the I-V converter system for a PBTTT-C14 OFET sensor during the pre-conditioning period under nitrogen (black curve), under exposure to 30% p_{sat} n-butanol vapour and during the recovery period under nitrogen (blue curve).

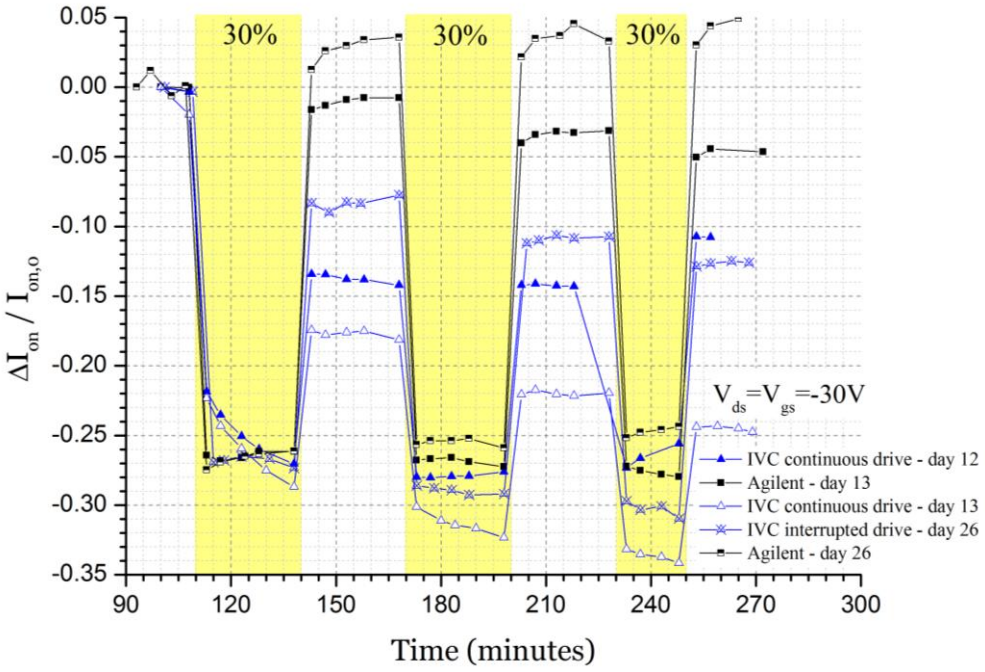

Figure 7-31 – Relative responses (ratio of the change in saturated drain current under exposure to its pre-exposure value) $\Delta I_{on}/I_{on,0}$ versus time. A comparative graph of all n-butanol vapour exposure measurements. Due to the different pre-conditioning period durations, a time offset has been added to some of the curves so that all exposure/recovery periods coincide.

Moreover, an explanation of the clear dependence of I_{on} recovery on the drive signal can be sought in the polar nature of n-butanol molecules; it can be assumed that the symmetry of the zero-offset sine drive inhibits the removal of analyte molecules from the semiconductor-dielectric interface during recovery by electrostatically keeping these dipoles in close proximity to the interface. Conversely, when no drive was applied, the recovery under nitrogen purge was enhanced. Furthermore, in the case of DC measurements, every sweep started with the application of a large reverse gate bias (+30V) which can potentially have a twofold impact: to induce a positive V_{th} shift due to dielectric stress [142] and simultaneously, to repel the analyte molecules from the semiconductor-dielectric surface [12], which together effectively enhance I_{on}, as discussed above.

7.3.6.3. *Conclusion*

The effects of n-butanol vapour on a PBTTT-C14 OFET sensor were studied. The limit of detection (LoD) was found to be lower than the lowest tested concentration of 2000 ppm. Multiple measurements of the same exposure/recovery pattern were taken. Two different methods of electrical characterisation were used; the first one was the extraction of standard transfer characteristics from DC measurements with the aid of a semiconductor parameter analyser, and the second one was based on AC measurements carried out with the I-V converter system, discussed in Chapter 4.

Both threshold voltage (V_{th}) and mobility (μ) were found to get affected by the analyte; both changes induced a drop in the saturated drain current (I_{on}). This decrease in I_{on} was found to be of comparable magnitude for all measurements, regardless of the method used. However, during the sensor recovery periods under nitrogen purge, the DC measurements showed that I_{on} fully recovered or even surpassed its pre-exposure state. On the contrary, measurements under continuous AC drive revealed that the driving conditions play a role in the recovery process; more specifically, while mobility was found to recover to a great extent, V_{th} remained at elevated levels compromising the recovery. The recovery was found to meliorate when short AC pulses were used in place of a continuous drive. This phenomenon can be attributed to the electrostatic effects of the drive voltage on the polar analyte molecules.

7.3.7. Comparison and conclusion on alcohol sensing

First and foremost, the work presented in this section served for the demonstration of the capabilities of the multiparametic characterisation system, discussed in Chapter 4. The quantification of multiple sensing parameters in real-time is an added value to vapour sensing using OFET transducers. In particular, the example of ethanol exposure clearly showed the independent responses of threshold voltage and mobility parametric in time, which both affect drain current inducing competing trends. A manuscript describing these experiments has been accepted for publication in *Sensors and Actuators B* journal.

In detail, the exposure tests on the second batch of PBTTT devices, using ethanol and n-octanol vapour as analytes under real-time automated multiparametric measurements, reveal the effects of the analyte molecules on separate parameters of these OFET sensors. The limited amount of investigated sensors and analytes hinder the extraction of explicit conclusions on the weak and largely reversible ethanol-PBTTT interactions; however, a comparison of the experimental data and a discussion on the possible mechanisms behind the observed changes are given here.

As a general observation, in each exposure test, the analyte concentration played a role in the magnitude of the induced changes; however, when expressed in ppm, the limit of detection (LoD) of ethanol was found to be about two orders-of-magnitude larger than that of n-octanol. An interesting finding is the fact that mobility showed opposite responses under exposure to these two different alcohols. For all exposures, ethanol vapour yielded a step-like μ drop, which was found to be roughly proportional to the respective analyte concentration. Contrarily, exposure to n-octanol induced a gradual increase in mobility, which carried on even after analyte delivery was ceased.

Regarding threshold voltage, all responses were not immediate but followed an exponential decay. However, the V_{th} sensitivity varied; n-octanol vapour generally caused mild decreases in the modulus of V_{th}, whereas the impact of ethanol was more pronounced. Considering that V_{th} is more likely to be affected by the presence of contaminants in the vicinity of the semiconductor-dielectric interface, it can be assumed that the probability of ethanol molecules diffusing through the grains of the semiconductor and reaching the interface is higher due to their much smaller size compared to the n-octanol ones; this fact can explain the stronger effects of ethanol vapour on V_{th}. Nevertheless, the fact that the concentration of ethanol is more than two orders-of-magnitude higher than that of n-octanol can be another contributing factor for the strong effects of the former on V_{th}.

Finally, the differences between the two batches of sensors (different device dimensions, different PBTTT variants, different solvents and deposition conditions, different electrical drive conditions, as well as the fact that the fabrication/characterisation were conducted in different laboratories) obscure any reliable comparison between the aforementioned tests involving ethanol and n-octanol, and the tests with n-butanol. The latter tests mainly served for the study of the effects of different drive conditions on the sensing properties of a particular sensor, as well as its long-term stability and performance. All results are summarised in Table 7-I.

To summarise, the automated vapour sensing system used in this section has strong advantages, which include: *a.* the support of both chemiresistors and OFET sensors, *b.* the

application of a sinusoidal drive that mitigates any bias-stress-related problems, which are usually encountered in OFETs, *c.* the real-time extraction and plotting of all important OFET parameters with data points every less than one second, *d.* the capability of conducting simultaneous measurements on multiple sensors, which can serve for comparisons and consistency/reproducibility tests, as well as the implementation of 'electronic nose' systems, *e.* the control of both the gas-mixing and device characterisation systems from the same graphical user interface. Some of the limitations of this system are: *a.* the support of normally-off (enhancement mode) OFETs only, *b.* the maximum operating voltage of ±45 V (for 4 DUT) or ±8 V (for 20 DUT), and *c.* the manual adjustment of the amplifier gain and oscilloscope input ranges, which may require re-adjustment during the measurement, if massive drain current changes are induced.

Table 7-I – Comparison of alcohol vapour exposure tests on PBTTT OFET sensors

OSC	Analyte	Drive	LoD (ppm)	Concentration (ppm)	ΔI_{on} (%)	ΔI_{off} (%)	ΔV_{th} (V)	$\Delta\mu$ (%)	Exposure/Recovery comments
PBTTT-C16	**ethanol**	AC	<2750	2750	-1.5%	0	~ +0.2	~ -3.8%	**Exposure:** Step-like μ responses, exponential V_{th} changes **Recovery:** I_{on} becomes higher than before exposure, V_{th} recovers partially, μ is higher than before
				8250	-5.2% to -1.1%	~ +10%	+0.5 to +1.0	~ -14.2%	
				24750	-19.3% to +38.9%	+587%	+2.5V to +8.5V	~ -42.8%	
	n-octanol		Between 35 and 70	<35	No response				**Exposure:** μ degradation is the same as before exposure (under nitrogen purge)
				70	+37% to +64%	+84% to +112%	+1.1 to +4.0	+22% to +44%	**Recovery:** μ and I_{on} kept rising for several minutes then dropped and came to equilibrium
PBTTT-C14	**n-butanol**	DC	<1967	1967	~-27%	0	N/A	N/A	**Recovery:** I_{on} can surpass pre-exposure value
		AC contin.			~-27%	0	-1.4	~-11%	**Recovery:** Partial; μ recovers, V_{th} remains increased
		AC interr.			~-27%	0	-1.4	~-10%	**Recovery:** Partial but better than that under continuous AC drive

7.4. Flexible PDI8-CN_2 OFETs as amine sensors

Octylamine has a molar mass of 129.24 g/mol, a boiling point 175-177 °C, a density of 0.782 g/cm^3 (at 25 °C) and a vapour pressure of approximately 133 Pa, i.e. ~1300 ppm (at 20 °C) [175]. Amines are of great interest in food spoilage detection research, mainly due to their occurrence in the breakdown of proteins, as in meat, fish and dairy products [176].

Recently, Hague *et al.* demonstrated a comparative study between a pentacene and a PDI8-CN_2 OFET sensors, both exposed to octylamine vapour [114]. In this work, the n-type semiconductor (PDI8-CN_2) is suggested as a better candidate material for amine sensing than its p-type (pentacene) counterpart. This conclusion is based upon experimental data which confirm that a *Lewis-base*, such as octylamine, acts as an electron-donating agent, which practically dopes an n-type semiconductor; whereas, in the case of a p-type semiconductor, such analyte traps charge carriers, reducing its conductivity. The effects on the drain current of OFETs based on PDI8-CN_2 were found to be much stronger than those on pentacene-based OFETs.

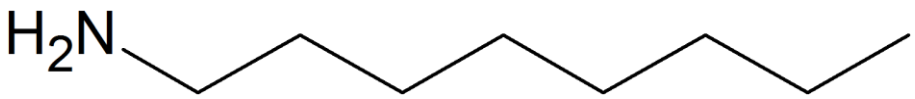

Figure 7-32 – A schematic representation of the octylamine molecule

Additionally, flexible transistors have been demonstrated by several research groups [51, 177-179], and the effects of mechanical stress on their electrical characteristics have been modelled and experimentally tested in some research papers [180]. As of September 2013, there is no published work on either the effects of bending on the sensitivity of flexible OFET sensors, or the real-time multiparametric characterisation of OFETs during deformation.

In the work presented in this section, a flexible PDI8-CN_2 OFET based on LDPE-coated AlO_x dielectric was tested under mechanical stress and exposure to octylamine vapour. Its substrate was deformed so that tensile stress was applied to the length axis of its channel, effectively elongating it. The use of a servo-motorised stage, in conjunction with the I-V converter system, provided for real-time measurements which were taken during the deformation/relaxation cycles. Non-quantitative exposure to octylamine vapour was applied to the sensor in stressed and relaxed conditions.

7.4.1.1. *Test methodology*

A set of four PDI8-CN_2 OFETs was built on a flexible transparent substrate. The procedure of device preparation was identical to the one described in section 5.3.4, except for the size of the substrate; in this case, the selected dimensions were 40 mm x 40 mm and special care was taken during all mask alignments so that the induced deformation stress would later be tensile and transverse to the length of the OFET channel. The gate, source and drain contacts were wire-bonded to flexible tinned copper wires using a special carbon compound (*Fluka Leit-C*, product number: *09929*); the ends of the three wires were soldered to a PCB, through which they were electrically connected to the I-V converter system described in Chapter 4.

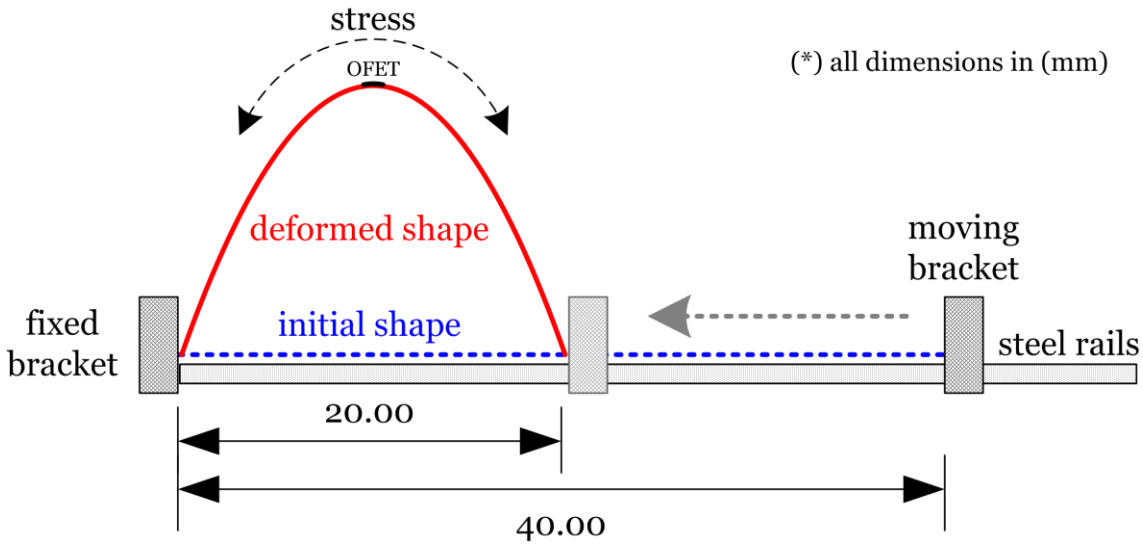

Figure 7-33 – Illustration of the deformation tests on flexible OFETs.

A bespoke test rig based on a programmable syringe pump (*New Era Pump Systems Inc.,* model: *NE-300*) was built. The PCB was attached to the chassis of the pump and the flexible substrate was placed onto the two steel rails which are intended for providing support to a syringe. One side of the substrate was placed against the fixed bracket of the pump, whilst the moving bracket was brought in contact with the opposite side of the substrate, as shown in Figure 7-3. The syringe-diameter and flow-rate settings of the pump were adjusted so that the resulting constant linear speed of the moving bracket would roughly be 0.5 mm/s. During the deformation tests, the bracket compressed the substrate and consequently forced it to bend upwards; given that the OFET was grown on the top surface of the substrate and was properly aligned, the bending induced a tensile stress to the length of the channel by effectively elongating it. The maximum tested deformation was 20 mm (50%).

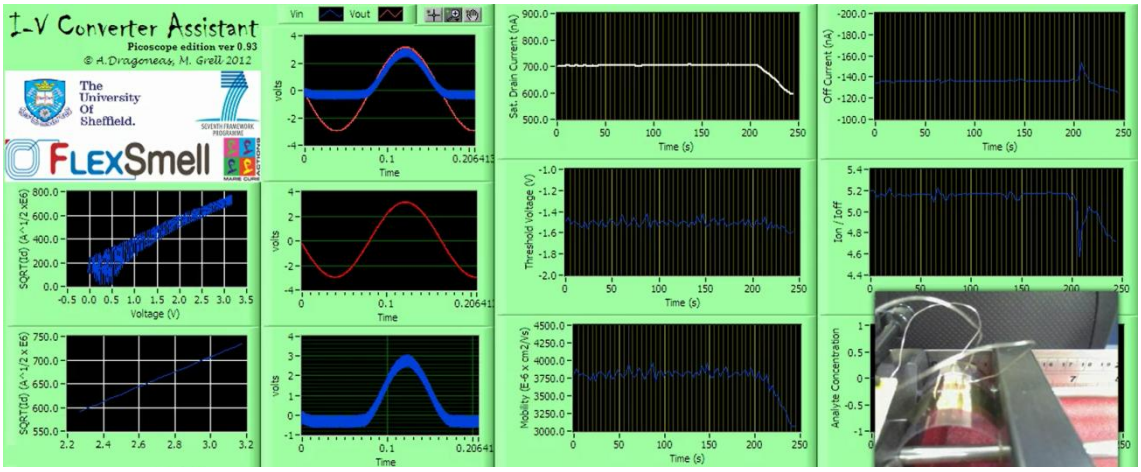

Figure 7-34 – A screenshot of the user interface of the automated real-time characterisation system during deformation of a flexible PDI8-CN_2 OFET. Bottom-right: A video screenshot of the actual deformed OFET lying on the bespoke test rig taken at the same moment.

Qualitative vapour sensitivity tests were performed by bringing a wooden toothpick, which was previously impregnated with octylamine, in close proximity to the channel of the OFET.

The sensor was exposed twice; once under deformation and once after relaxation to its initial shape.

A zero-offset sinusoidal drive with a peak voltage of 3 V and a frequency of 6 Hz was applied to the device under test. The raw data were acquired in sets of 11 consecutive measurements every 3 seconds and a median filter was applied to all calculated parameters in each of those sets; the median value of each parameter was extracted as a data point. More details on the automated characterisation system are given in section 4.3. All measurements were taken in ambient conditions, at room temperature of 23 °C and under artificial white light.

7.4.1.2. *Results and discussion*

In a preliminary test, the device under test showed a very stable performance during the measurements in ambient conditions for several minutes. Following that, two runs of deformation/ relaxation tests were applied; the substrate was bent twice up to a point that its arc had a width of 20 mm, as depicted by the red curve in Figure 7-33; then, it was returned to its relaxed shape.

Both the saturated drain current (I_{on}) and the off-state current I_{off} showed a drop under deformation. Assuming that I_{off} is a purely ohmic current and I_{on} is the sum of the saturated transistor current and an ohmic contribution due to doping, as described by eq. (4.8), both drops can be partly attributed to the elongation of the channel, i.e. the channel length increases and this results in an increase in channel resistance.

Nevertheless, the automated characterisation system calculated a simultaneous mobility (μ) drop under deformation; the precision of this result can be challenged due to the fact that the algorithm for μ calculation takes a constant channel length into account, as eq. (4.10) describes, and the fact that length changes as mentioned above. However, according to the same equation, the elongation of the channel length while its width remains intact should have resulted in an erroneously calculated increase in μ, rather than a drop. This fact alone connotes that deformation actually has a stronger impact on μ than what the calculated data suggest. It can be assumed that the induced tensile stress increases the intergrain distances in the semiconductor film, effectively inhibiting charge carrier hopping between the grains and resulting in a reduction of the overall mobility.

Figure 7-35 shows the I_{on} and μ behaviours during the first 20 minutes of measurements. The initial I_{on} was found to be 700 nA, approximately. The first deformation resulted in an I_{on} decrease of ~120 nA; however, the value of I_{on} recovered completely after the first relaxation. During the second cycle, a larger drop of roughly 140 nA was recorded at maximum deformation and this was followed by a recovery of ~120 nA when the substrate returned to its relaxed shape; as a result, I_{on} finally rested at a lower level than its initial one. The third deformation again yielded an 120 nA drop after an initial overshoot; the I_{on} value stabilised at 560 nA. Mobility was found to be the main factor of the I_{on} change as the trends of μ under mechanical stress were very similar to the ones of I_{on}. Threshold voltage showed negligible sensitivity to any deformation.

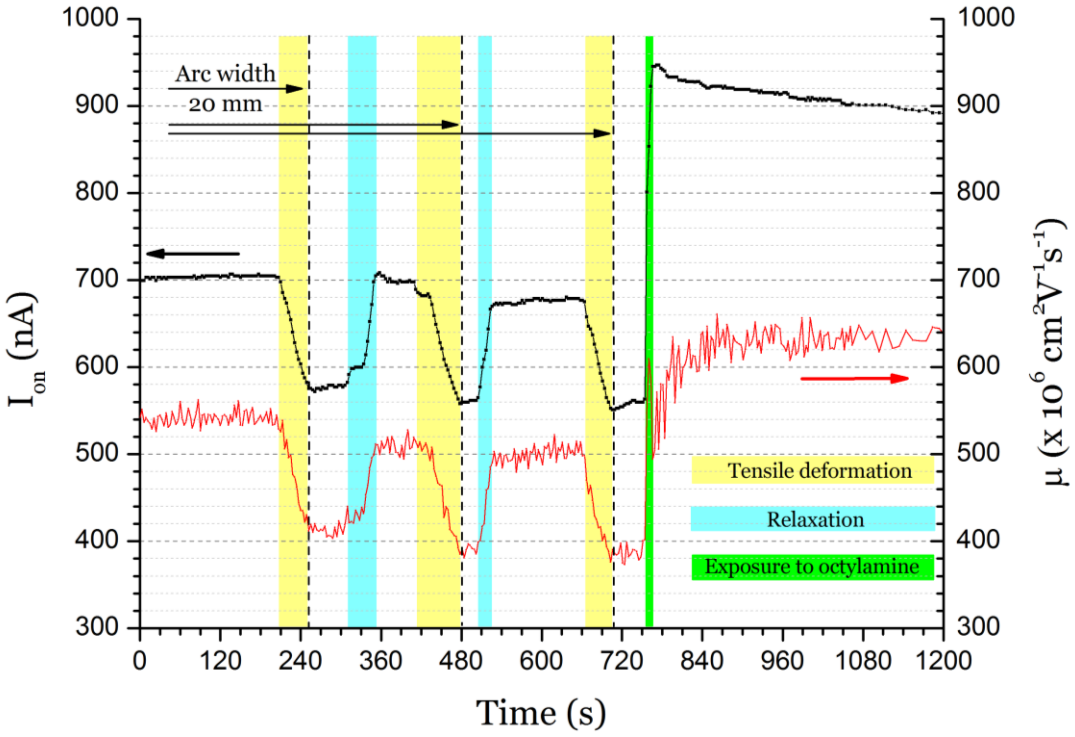

Figure 7-35 – Saturated drain current (top black curve, left y-axis) and charge carrier mobility (bottom red curve, right y-axis) versus time, for a flexible PDI8-CN2 OFET based on AlOx-LDPE dielectric. Colour-shaded regions represent periods of deformation (yellow), relaxation (cyan) and exposure to octylamine vapour (green).

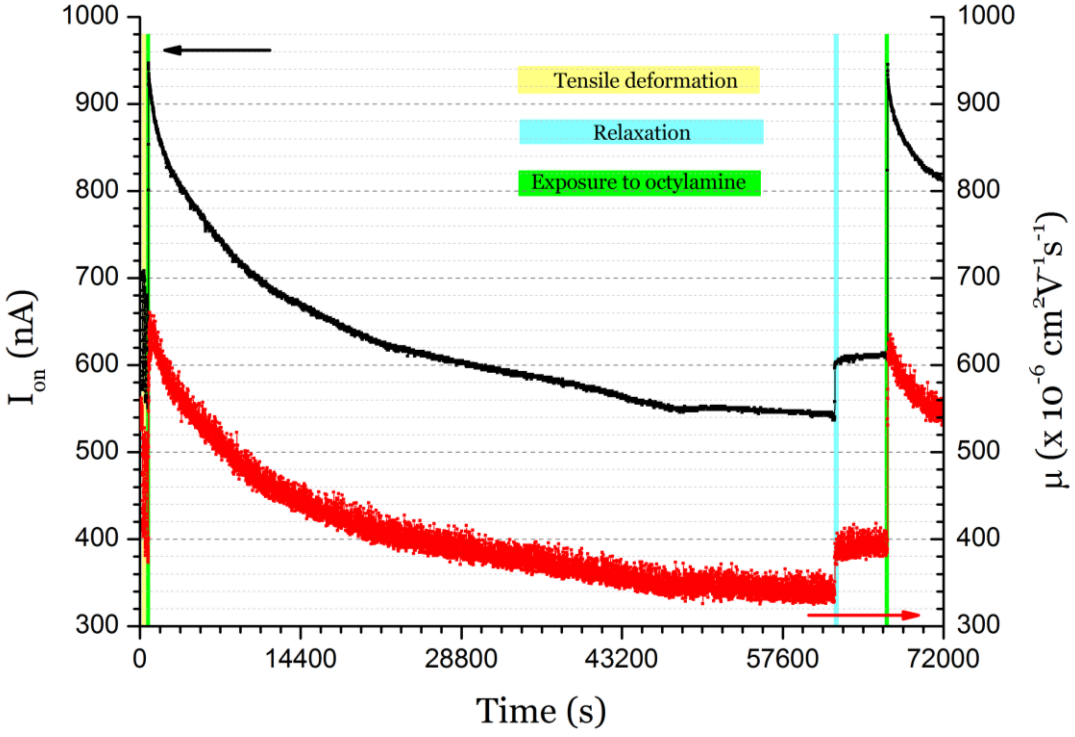

Figure 7-36 – 20-hour-long measurements of saturated drain current (top black curve, left y-axis) and charge carrier mobility (bottom red curve, right y-axis) versus time, for a flexible PDI8-CN2 OFET based on AlOx-LDPE dielectric. Colour-shaded regions represent periods of deformation (yellow), relaxation (cyan) and exposure to octylamine vapour (green).

After the third deformation, the sensor was exposed to octylamine vapour. The response to this brief vapour exposure was immediate; I_{on} increased dramatically to 950 nA, showing a

relative response ($\Delta I_{on}/I_{on,0}$) of ~ 70%. Then, I_{on} exhibited a very slow exponential decrease and after some 15 hours, it returned to its pre-exposure levels, as shown in Figure 7-36. Next, the substrate was returned to its initial shape; I_{on} was found significantly decreased, compared to its initial performance. Interestingly, a second vapour exposure elevated the I_{on} to exactly the same level of 950 nA. The device under test was left in ambient conditions and another exponential decay of I_{on} was recorded until the end of the test.

7.4.1.3. *Conclusion*

It is worth underlining that the main purpose of this test was to serve as a proof-of-concept demonstration of the potentials of low-voltage flexible OFETs as vapour sensors, rather than providing quantitative results on octylamine sensing; the effects of controlled octylamine vapour exposure on rigid PDI8-CN_2 OFETs have already been demonstrated [114].

Here, it was shown that OFETs can be deformed to a large extent and reshaped without significant compromising their electrical performance. The decrease in drain current under deformation can be explained by both the elongation of the conduction path, i.e. the OFET channel length, and the alterations in the intergrain distances of the semiconductor film due to tensile stress; the latter is undoubtedly the main contributing factor. Analyte exposures with no control of the analyte concentration interestingly bore exactly the same elevated value of saturated drain current.

Further investigation of the sensitivity of OFET sensors under deformation is suggested as future work. The effects of other kinds of mechanical stress, such us compressive stress on the length-axis of the OFET channel, can serve for comparisons with the channel elongation tests shown here. Expanding this study using other semiconductor/analyte combinations can generalise the observations of this demonstration and lead to comprehensive conclusions.

Overall conclusion and proposed future research work

The work presented in the previous chapters covers a wide range of experimental work which was conducted following three major objectives, i.e. the optimisation of the fabrication process of organic semiconductor devices with an emphasis on the field of organic field-effect transistor (OFETs), the development of novel methods for the efficient electrical characterisation of OFETs used as gas sensing transducers and finally, the use of the fabricated semiconductor devices as sensing transducers in real vapour exposure experiments with the aid of the characterisation methods developed.

Regarding device fabrication, organic thin-film devices with several material combinations and various architectures were developed and characterised. Devices were built on both rigid and plastic flexible substrates. Both low-molecular weight and polymer organic semiconductors (OSCs) were processed and deposited using vacuum and wet methods, respectively. Organic nanowires were used for the development of vapour sensors with remarkably high sensitivity. Both inorganic oxide and polymer dielectrics were used; the recently introduced method of thermally evaporated low-density polyethylene (LDPE) was adopted, optimised and successfully employed for the fabrication of OFETs with material combinations that have not been demonstrated in the literature.

Regarding device characterisation, the cornerstone of this work was the development of a real-time multiparametric characterisation system, specially designed for measurements on OFETs. Most of the vapour sensing measurements were performed with the aid of this system. Moreover, an entire chapter is dedicated to the study of the light sensitivity of OFETs, providing detailed information on the effects of illumination on multiple device parameters and their evolution with time; the importance of the gate dielectric surface treatment was highlighted by these measurements. The importance of the gate dielectric surface was also studied by a correlation of the electrical characteristics and the air stability of the fabricated devices with the morphology of their semiconductor films using AFM imaging.

Regarding vapour sensing measurements, a complete test rig for the controlled exposure of the fabricated devices to the various analytes was developed; this included an upgrade of the automated characterisation system for the support of multiple sensors. Chemiresistors and OFETs employing a selection of OSCs were used as sensing transducers for the detection of analytes, such as water vapour, alcohols and octylamine. The measurements conducted by the use of the real-time characterisation system provided detailed information on the effects of the analyte vapour on different independent parameters of the OFET transducers, exemplifying their advantages over conventional chemiresistors.

The work presented here was also communicated in a series of presentations and journal publications which are enlisted in the homonymous paragraph below. The most important innovations are summarised here:

a. The development of a novel system for the real-time multiparametric characterisation of OFETs made of various materials, including water-gated devices based on organic nanowires [62]. The operation of this system is described in Chapter 4.
b. The fabrication of OFETs with material combinations which, as of October 2013, have not been reported in the literature. For instance, top-gold-contact pentacene OFETs, gated exclusively by an evaporated LDPE layer were successfully developed; these devices also gave interesting indications of ambipolar charge transport. A summary of the fabricated devices is given in section 5.6.
c. The discovery of photocapacitance, i.e. an unexpected permittivity change of anodised aluminium oxide, which was measured in parallel-plate capacitors exposed to visible light illumination; as of October 2013, this behaviour has never been reported in the literature and needs further attention. These findings are discussed in section 6.2.
d. A detailed investigation of the effects of illumination on multiple OFET parameters, their evolution with time and the great importance of the gate oxide surface treatment in the light-sensitivity of the fabricated OFETs. This study can be found in section 6.3.
e. A demonstration of organic semiconductor sensor sensitivity enhancement with the use of OSCs in the form of nanowires [49]. This work is presented in section 7.2.
f. A demonstration of the capabilities of the real-time characterisation system by the detection and disentanglement of the complex effects of alcohol vapour on different independent parameters of PBTTT OFET sensors. This is given in section 7.3.
g. A proof-of-concept of the operation of flexible OFET gas sensors under mechanical deformation and under exposure to octylamine vapour. This study is presented in section 7.4.

In addition, motivated by the aforementioned findings, as well as other interesting observations, further research work on the following concepts is proposed here:

i. The confirmation of the ambipolar behaviour of commonly either hole- or electron-transporting OSCs by the development of OFETs exclusively gated with evaporated LDPE. This study is motivated by the results discussed in section 5.2.3.
ii. The successful development of organic CMOS inverters on plastic substrates by appropriately tuning the mobility and threshold voltage of the p- and n-type constituent OFETs using appropriate gate dielectric surface treatments. Such an attempt is presented in section 5.6.
iii. The thorough investigation of the phenomenon of photocapacitance. The observation of a dielectric permittivity change under visible light illumination in a wide bandgap insulator has been a very interesting finding, as discussed in section 6.2. Nevertheless, this observation cannot easily be given an adequate explanation. Light-sensitivity tests on capacitors based on untreated aluminium oxide, as well as other oxide dielectrics and especially, sputtered alumina can serve for meaningful comparisons. It is very important to confirm whether this behaviour is unique to aluminium oxide, anodised aluminium oxide in particular or anodised metal oxides in general. Moreover, the study of the relation between the observed photocapacitance and the incident photon flux is equally important. Further control experiments have already been planned.

iv. The use of alternative dielectric and OSC combinations for a comparison with the findings of the OFET light-sensitivity study. It is believed that an all polymer dielectric can effectively enhance the light stability of an OFET, as the devices with LDPE-coated gate oxide have indicated. More details are given in section 6.3.

v. The study of the peculiar behaviour of tetracene under illumination. These phenomena were explained only in part by an apparent reduction of the density of traps in the bulk of the semiconductor due to the illumination. However, the observed response of a tetracene MSM photodetector to illumination, discussed in section 6.4, cannot be adequately explained and needs further investigation.

vi. The preparation of various OSCs in the form of nanowires and their exploitation in the development of sensing transducers. The findings from the tests on P3HT nanowire devices, discussed in section 7.2, suggest that the sensitivity of a sensor can dramatically be enhanced when the OSC is prepared in this form.

vii. A further investigation of the impact of mechanical deformation on the performance and the sensitivity of OFETs built on plastic substrates and used as sensing transducers. A demonstration of this concept is given in section 7.4.

References

[1] FlexSMELL. "FlexSMELL Project Objectives," Nov 21, 2013; http://flexsmell.eu/project-objectives.html.

[2] K. Tsukada, Y. Miyahara, Y. Shibata, and H. Miyagi, "An Integrated Chemical Sensor with Multiple Ion and Gas Sensors," *Sensors and Actuators B-Chemical,* vol. 2, no. 4, pp. 291-295, Oct, 1990.

[3] J. H. Shin, H. J. Lee, C. Y. Kim, B. K. Oh *et al.*, "ISFET-based differential pCO(2) sensors employing a low-resistance gas-permeable membrane," *Analytical Chemistry,* vol. 68, no. 18, pp. 3166-3172, Sep 15, 1996.

[4] T. Doll, J. Lechner, I. Eisele, K.-D. Schierbaum *et al.*, "Ozone detection in the ppb range with work function sensors operating at room temperature," *Sensors and Actuators B: Chemical,* vol. 34, no. 1–3, pp. 506-510, 1996.

[5] A. Oprea, U. Weimar, E. Simon, M. Fleischer *et al.*, "Copper phthalocyanine suspended gate field effect transistors for NO2 detection," *Sensors and Actuators B: Chemical,* vol. 118, no. 1–2, pp. 249-254, 2006.

[6] A. Fuchs, M. Bogner, T. Doll, and I. Eisele, "Room temperature ozone sensing with KI layers integrated in HSGFET gas sensors," *Sensors and Actuators B-Chemical,* vol. 48, no. 1-3, pp. 296-299, May 30, 1998.

[7] M. E. Roberts, A. N. Sokolov, and Z. N. Bao, "Material and device considerations for organic thin-film transistor sensors," *Journal of Materials Chemistry,* vol. 19, no. 21, pp. 3351-3363, 2009.

[8] L. Torsi, M. Magliulo, K. Manoli, and G. Palazzo, "Organic field-effect transistor sensors: a tutorial review," *Chemical Society Reviews,* vol. 42, no. 22, pp. 8612-8628, 2013.

[9] L. Torsi, A. Dodabalapur, L. Sabbatini, and P. G. Zambonin, "Multi-parameter gas sensors based on organic thin-film-transistors," *Sensors and Actuators B-Chemical,* vol. 67, no. 3, pp. 312-316, Sep 1, 2000.

[10] Y. F. Sun, S. B. Liu, F. L. Meng, J. Y. Liu *et al.*, "Metal Oxide Nanostructures and Their Gas Sensing Properties: A Review," *Sensors,* vol. 12, no. 3, pp. 2610-2631, Mar, 2012.

[11] M. C. Carotta, A. Cervi, V. di Natale, S. Gherardi *et al.*, "ZnO gas sensors: A comparison between nanoparticles and nanotetrapods-based thick films," *Sensors and Actuators B-Chemical,* vol. 137, no. 1, pp. 164-169, Mar 28, 2009.

[12] B. Crone, A. Dodabalapur, A. Gelperin, L. Torsi *et al.*, "Electronic sensing of vapors with organic transistors," *Applied Physics Letters,* vol. 78, no. 15, pp. 2229-2231, Apr 9, 2001.

[13] D. Duarte, and A. Dodabalapur, "Investigation of the physics of sensing in organic field effect transistor based sensors," *Journal of Applied Physics,* vol. 111, no. 4, Feb 15, 2012.

[14] L. Torsi, F. Marinelli, M. D. Angione, A. Dell'Aquila *et al.*, "Contact effects in organic thin-film transistor sensors," *Organic Electronics,* vol. 10, no. 2, pp. 233-239, Apr, 2009.

[15] H. AlQahtani, D. Puzzovio, A. Dragoneas, T. Richardson *et al.*, "A swelling-based chemiresistor for a biogenic odour," *Talanta,* vol. 99, pp. 50-54, Sep 15, 2012.

[16] T. Someya, A. Dodabalapur, J. Huang, K. C. See *et al.*, "Chemical and Physical Sensing by Organic Field-Effect Transistors and Related Devices," *Advanced Materials,* vol. 22, no. 34, pp. 3799-3811, Sep 8, 2010.

[17] A. Das, R. Dost, T. H. Richardson, M. Grell *et al.*, "Low cost, portable, fast multiparameter data acquisition system for organic transistor odour sensors," *Sensors and Actuators B-Chemical,* vol. 137, no. 2, pp. 586-591, Apr 2, 2009.

[18] A. N. Sokolov, M. E. Roberts, O. B. Johnson, Y. Cao *et al.*, "Induced Sensitivity and Selectivity in Thin-Film Transistor Sensors via Calixarene Layers," *Advanced Materials,* vol. 22, no. 21, pp. 2349-2353, 2010.

[19] D. C. Wedge, A. Das, R. Dost, J. Kettle *et al.*, "Real-time vapour sensing using an OFET-based electronic nose and genetic programming," *Sensors and Actuators B-Chemical,* vol. 143, no. 1, pp. 365-372, Dec 4, 2009.

[20] intel. "Altera to Build Next-Generation, High-Performance FPGAs on Intel's 14 nm Tri-Gate Technology," Sep 29, 2013; http://newsroom.intel.com/community/intel_newsroom/blog/2013/02/25/altera-to-build-next-generation-high-performance-fpgas-on-intels-14-nm-tri-gate-technology.

[21] Z. Y. Cheng, M. T. Currie, C. W. Leitz, G. Taraschi *et al.*, "Electron mobility enhancement in strained-Si n-MOSFETs fabricated on SiGe-on-insulator (SGOI) substrates," *Ieee Electron Device Letters,* vol. 22, no. 7, pp. 321-323, Jul, 2001.

[22] S. M. Sze, *Semiconductor Devices: Physics and Technology*: Wiley, 2001.

[23] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-κ gate dielectrics: Current status and materials properties considerations," *Journal of Applied Physics,* vol. 89, no. 10, pp. 5243-5275, 2001.

[24] G. Moore, E., "Cramming more components onto integrated circuits," *Electronics*, pp. 114–117, April 19, 1965.

[25] Wikimedia. "Images downloaded from Wikimedia Commons, edited and reused under free licence.," Nov 22, 2013; http://en.wikipedia.org/wiki/Orbital_hybridisation.

[26] G. Kemeny, and Rosenber.B, "Small Polarons in Organic and Biological Semiconductors," *Journal of Chemical Physics,* vol. 53, no. 9, pp. 3549, 1970.

[27] B. Lüssem, M. Riede, and K. Leo, "Doping of organic semiconductors," *physica status solidi (a),* vol. 210, no. 1, pp. 9-43, 2013.

[28] A. Wan, J. Hwang, F. Amy, and A. Kahn, "Impact of electrode contamination on the alpha-NPD/Au hole injection barrier," *Organic Electronics,* vol. 6, no. 1, pp. 47-54, Feb, 2005.

[29] L. Burgi, T. J. Richards, R. H. Friend, and H. Sirringhaus, “Close look at charge carrier injection in polymer field-effect transistors,” *Journal of Applied Physics,* vol. 94, no. 9, pp. 6129-6137, Nov 1, 2003.
[30] P. V. Pesavento, K. P. Puntambekar, C. D. Frisbie, J. C. McKeen *et al.*, “Film and contact resistance in pentacene thin-film transistors: Dependence on film thickness, electrode geometry, and correlation with hole mobility,” *Journal of Applied Physics,* vol. 99, no. 9, May 1, 2006.
[31] M. J. Panzer, and C. D. Frisbie, "Contact Effects in Organic Field-Effect Transistors," *Organic Field-Effect Transistors*, Z. Bao and J. Locklin, eds., pp. 139-157: CRC Press, 2007.
[32] N. Karl, J. Marktanner, R. Stehle, and W. Warta, “High-Field Saturation of Charge Carrier Drift Velocities in Ultrapurified Organic Photoconductors,” *Synthetic Metals,* vol. 42, no. 3, pp. 2473-2481, May 29, 1991.
[33] G. Horowitz, "Charge Transport in Oligomers," *Organic Field-Effect Transistors*, Z. Bao and J. Locklin, eds., pp. 73-101, 2007.
[34] V. Coropceanu, J. Cornil, D. A. da Silva, Y. Olivier *et al.*, “Charge transport in organic semiconductors,” *Chemical Reviews,* vol. 107, no. 4, pp. 926-952, Apr, 2007.
[35] W. Warta, and N. Karl, “Hot Holes in Naphthalene - High, Electric-Field-Dependent Mobilities,” *Physical Review B,* vol. 32, no. 2, pp. 1172-1182, 1985.
[36] H. Bassler, “Charge Transport in Disordered Organic Photoconductors - a Monte-Carlo Simulation Study,” *Physica Status Solidi B-Basic Research,* vol. 175, no. 1, pp. 15-56, Jan, 1993.
[37] L. Hague, D. Puzzovio, A. Dragoneas, and M. Grell, “Simplified Real-Time Organic Transistor Characterisation Schemes for Sensing Applications,” *Science of Advanced Materials,* vol. 3, no. 6, pp. 907-911, Dec, 2011.
[38] W. F. Pasveer, J. Cottaar, C. Tanase, R. Coehoorn *et al.*, “Unified description of charge-carrier mobilities in disordered semiconducting polymers,” *Physical Review Letters,* vol. 94, no. 20, May 27, 2005.
[39] L. L. Chua, J. Zaumseil, J. F. Chang, E. C. W. Ou *et al.*, “General observation of n-type field-effect behaviour in organic semiconductors,” *Nature,* vol. 434, no. 7030, pp. 194-199, Mar 10, 2005.
[40] P. K. Weimer, “Tft - New Thin-Film Transistor,” *Proceedings of the Institute of Radio Engineers,* vol. 50, no. 6, pp. 1462, 1962.
[41] R. R. Søndergaard, M. Hösel, and F. C. Krebs, “Roll-to-Roll fabrication of large area functional organic materials,” *Journal of Polymer Science Part B: Polymer Physics,* vol. 51, no. 1, pp. 16-34, 2013.
[42] B. Servet, G. Horowitz, S. Ries, O. Lagorsse *et al.*, “Polymorphism and Charge Transport in Vacuum-Evaporated Sexithiophene Films,” *Chemistry of Materials,* vol. 6, no. 10, pp. 1809-1815, 1994/10/01, 1994.
[43] C. D. Dimitrakopoulos, and D. J. Mascaro, “Organic thin-film transistors: A review of recent advances,” *Ibm Journal of Research and Development,* vol. 45, no. 1, pp. 11-27, Jan, 2001.
[44] C. K. Song, M. K. Jung, and B. W. Koo, “Pentacene thin film transistor improved by thermal annealing,” *Journal of the Korean Physical Society,* vol. 39, pp. S271-S274, Dec, 2001.
[45] M. J. Joung, C. A. Kim, S. Y. Kang, K.-H. Baek *et al.*, “The application of soluble and regioregular poly(3-hexylthiophene) for organic thin-film transistors,” *Synthetic Metals,* vol. 149, no. 1, pp. 73-77, 2005.
[46] S. M. Sze, *Physics of Semiconductor Devices*: John Wiley & Sons, 1981.
[47] G. Horowitz, R. Hajlaoui, H. Bouchriha, R. Bourguiga *et al.*, “The concept of "threshold voltage" in organic field-effect transistors,” *Advanced Materials,* vol. 10, no. 12, pp. 923, Aug 20, 1998.
[48] M. G. Kane, "Organic Thin-Film Transistors for Flat-Panel Displays," *Organic Field-Effect Transistors*, Z. Bao and J. Locklin, eds., pp. 551-594: CRC Press, 2007.
[49] A. Dragoneas, M. Grell, M. Hampton, and J. E. Macdonald, “Morphology-Driven Sensitivity Enhancement in Organic Nanowire Chemiresistors,” *Sensor Letters,* vol. 11, no. 3, pp. 552-555, Mar, 2013.
[50] Corning, "HPFS® Fused Silica Standard Grade," 2003.
[51] L. A. Majewski, M. Grell, S. D. Ogier, and J. Veres, “A novel gate insulator for flexible electronics,” *Organic Electronics,* vol. 4, no. 1, pp. 27-32, Jun, 2003.
[52] E. F. Runnion, S. M. Gladstone, R. S. Scott, D. J. Dumin *et al.*, “Thickness dependence of stress-induced leakage currents in silicon oxide,” *Ieee Transactions on Electron Devices,* vol. 44, no. 6, pp. 993-1001, Jun, 1997.
[53] M. Koh, W. Mizubayashi, K. Iwamoto, H. Murakami *et al.*, “Limit of gate oxide thickness scaling in MOSFETs due to apparent threshold voltage fluctuation induced by tunnel leakage current,” *Ieee Transactions on Electron Devices,* vol. 48, no. 2, pp. 259-264, Feb, 2001.
[54] L. Kergoat, L. Herlogsson, D. Braga, B. Piro *et al.*, “A Water-Gate Organic Field-Effect Transistor,” *Advanced Materials,* vol. 22, no. 23, pp. 2565-2569, 2010.
[55] L. Kergoat, L. Herlogsson, B. Piro, M. C. Pham *et al.*, “Tuning the threshold voltage in electrolyte-gated organic field-effect transistors,” *Proceedings of the National Academy of Sciences of the United States of America,* vol. 109, no. 22, pp. 8394-8399, May 29, 2012.
[56] R. P. Ortiz, A. Facchetti, and T. J. Marks, “High-k Organic, Inorganic, and Hybrid Dielectrics for Low-Voltage Organic Field-Effect Transistors,” *Chemical Reviews,* vol. 110, no. 1, pp. 205-239, 2010/01/13, 2009.
[57] C. Leroux, J. Mitard, G. Ghibaudo, X. Garros *et al.*, “Characterization and modeling of hysteresis phenomena in high K dielectrics,” *Ieee International Electron Devices Meeting 2004, Technical Digest*, pp. 737-740, 2004.
[58] J. Veres, S. D. Ogier, S. W. Leeming, D. C. Cupertino *et al.*, “Low-k insulators as the choice of dielectrics in organic field-effect transistors,” *Advanced Functional Materials,* vol. 13, no. 3, pp. 199-204, Mar, 2003.

[59] S. C. Lim, S. H. Kim, J. H. Lee, M. K. Kim *et al.*, "Surface-treatment effects on organic thin-film transistors," *Synthetic Metals,* vol. 148, no. 1, pp. 75-79, 2005.

[60] T. W. Kelley, L. D. Boardman, T. D. Dunbar, D. V. Muyres *et al.*, "High-performance OTFTs using surface-modified alumina dielectrics," *Journal of Physical Chemistry B,* vol. 107, no. 24, pp. 5877-5881, Jun 19, 2003.

[61] T. Cramer, A. Campana, F. Leonardi, S. Casalini *et al.*, "Water-gated organic field effect transistors - opportunities for biochemical sensing and extracellular signal transduction," *Journal of Materials Chemistry B,* vol. 1, no. 31, pp. 3728-3741, 2013.

[62] A. Al Naim, A. Hobson, R. T. Grant, A. Dragoneas *et al.*, "Water-gated organic nanowire transistors," *Organic Electronics,* vol. 14, no. 4, pp. 1057-1063, Apr, 2013.

[63] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-kappa gate dielectrics: Current status and materials properties considerations," *Journal of Applied Physics,* vol. 89, no. 10, pp. 5243-5275, May 15, 2001.

[64] W. H. Ha, M. H. Choo, and S. Im, "Electrical properties of Al2O3 film deposited at low temperatures," *Journal of Non-Crystalline Solids,* vol. 303, no. 1, pp. 78-82, May 1, 2002.

[65] L. A. Majewski, R. Schroeder, and M. Grell, "Flexible high capacitance gate insulators for organic field effect transistors," *Journal of Physics D-Applied Physics,* vol. 37, no. 1, pp. 21-24, Jan 7, 2004.

[66] M. G. Mier, and E. A. Buvinger, "A Comparative Study of Anodized, Evaporated, and Sputtered Aluminum Oxide Thin Films," *Journal of Vacuum Science & Technology,* vol. 6, no. 4, pp. 727-730, 1969.

[67] J. W. Diggle, T. C. Downie, and C. W. Goulding, "Anodic Oxide Films on Aluminum," *Chemical Reviews,* vol. 69, no. 3, pp. 365, 1969.

[68] W. Kalb, P. Lang, M. Mottaghi, H. Aubin *et al.*, "Structure-performance relationship in pentacene/Al2O3 thin-film transistors," *Synthetic Metals,* vol. 146, no. 3, pp. 279-282, Nov 3, 2004.

[69] J. Sagiv, "Organized Monolayers by Adsorption .1. Formation and Structure of Oleophobic Mixed Monolayers on Solid-Surfaces," *Journal of the American Chemical Society,* vol. 102, no. 1, pp. 92-98, 1980.

[70] P. Silberzan, L. Leger, D. Ausserre, and J. J. Benattar, "Silanation of Silica Surfaces - a New Method of Constructing Pure or Mixed Monolayers," *Langmuir,* vol. 7, no. 8, pp. 1647-1651, Aug, 1991.

[71] P. Fontaine, D. Goguenheim, D. Deresmes, D. Vuillaume *et al.*, "Octadecyltrichlorosilane monolayers as ultrathin gate insulating films in metal-insulator-semiconductor devices," *Applied Physics Letters,* vol. 62, no. 18, pp. 2256-2258, 1993.

[72] Y. Kanbur, M. Irimia-Vladu, E. D. Glowacki, G. Voss *et al.*, "Vacuum-processed polyethylene as a dielectric for low operating voltage organic field effect transistors," *Organic Electronics,* vol. 13, no. 5, pp. 919-924, May, 2012.

[73] P. P. Luff, and M. White, "The structure and properties of evaporated polyethylene thin films," *Thin Solid Films,* vol. 6, no. 3, pp. 175-195, 1970.

[74] L. Kergoat, B. Piro, M. Berggren, M.-C. Pham *et al.*, "DNA detection with a water-gated organic field-effect transistor," *Organic Electronics,* vol. 13, no. 1, pp. 1-6, 2012.

[75] C. Wessells, R. Ruffo, R. A. Huggins, and Y. Cui, "Investigations of the Electrochemical Stability of Aqueous Electrolytes for Lithium Battery Applications," *Electrochemical and Solid State Letters,* vol. 13, no. 5, pp. A59-A61, 2010.

[76] C. Goldmann, S. Haas, C. Krellner, K. P. Pernstich *et al.*, "Hole mobility in organic single crystals measured by a "flip-crystal" field-effect technique," *Journal of Applied Physics,* vol. 96, no. 4, pp. 2080-2086, Aug 15, 2004.

[77] T. Takahashi, T. Takenobu, J. Takeya, and Y. Iwasa, "Ambipolar Light-Emitting Transistors of a Tetracene Single Crystal," *Advanced Functional Materials,* vol. 17, no. 10, pp. 1623-1628, 2007.

[78] Sigma-Aldrich. "B2403 Aldrich Benz[b]anthracene Product Specifications," Nov 19, 2013; http://www.sigmaaldrich.com/catalog/product/aldrich/b2403?lang=en&region=GB.

[79] C.-Y. Wei, K. Shu-Hao, H. Yu-Ming, H. Wen-Chieh *et al.*, "High-Mobility Pentacene-Based Thin-Film Transistors With a Solution-Processed Barium Titanate Insulator," *Electron Device Letters, IEEE,* vol. 32, no. 1, pp. 90-92, 2011.

[80] H. S. Tan, N. Mathews, T. Cahyadi, F. R. Zhu *et al.*, "The effect of dielectric constant on device mobilities of high-performance, flexible organic field effect transistors," *Applied Physics Letters,* vol. 94, no. 26, Jun 29, 2009.

[81] D. M. Taylor, H. L. Gomes, A. E. Underhill, S. Edge *et al.*, "Effect of Oxygen on the Electrical Characteristics of Field-Effect Transistors Formed from Electrochemically Deposited Films of Poly(3-Methylthiophene)," *Journal of Physics D-Applied Physics,* vol. 24, no. 11, pp. 2032-2038, Nov 14, 1991.

[82] A. Vollmer, H. Weiss, S. Rentenberger, I. Salzmann *et al.*, "The interaction of oxygen and ozone with pentacene," *Surface Science,* vol. 600, no. 18, pp. 4004-4007, Sep 15, 2006.

[83] Z. T. Zhu, J. T. Mason, R. Dieckmann, and G. G. Malliaras, "Humidity sensors based on pentacene thin-film transistors," *Applied Physics Letters,* vol. 81, no. 24, pp. 4643-4645, Dec 9, 2002.

[84] Sigma-Aldrich. "698423 Aldrich Pentacene Product Specifications," Nov 19, 2013; http://www.sigmaaldrich.com/catalog/product/aldrich/698423?lang=en&region=GB.

[85] B. A. Jones, M. J. Ahrens, M. H. Yoon, A. Facchetti *et al.*, "High-mobility air-stable n-type semiconductors with processing versatility: Dicyanoperylene-3,4 : 9,10-bis(dicarboximides)," *Angewandte Chemie-International Edition,* vol. 43, no. 46, pp. 6363-6366, 2004.

[86] Polyera. "ActivInk™ N1200 Info Sheet," Nov 18, 2013; http://www.polyera.com/downloads/Product_Info/InfoSheet-N1200.pdf.
[87] H. Klauk, "Organic thin-film transistors," *Chemical Society Reviews,* vol. 39, no. 7, pp. 2643-2666, 2010.
[88] R. D. Mccullough, R. D. Lowe, M. Jayaraman, and D. L. Anderson, "Design, Synthesis, and Control of Conducting Polymer Architectures - Structurally Homogeneous Poly(3-Alkylthiophenes)," *Journal of Organic Chemistry,* vol. 58, no. 4, pp. 904-912, Feb 12, 1993.
[89] H. Sirringhaus, P. J. Brown, R. H. Friend, M. M. Nielsen *et al.*, "Two-dimensional charge transport in self-organized, high-mobility conjugated polymers," *Nature,* vol. 401, no. 6754, pp. 685-688, Oct 14, 1999.
[90] L. A. Majewski, R. Schroeder, and M. Grell, "Organic field-effect transistors with ultrathin gate insulator," *Synthetic Metals,* vol. 144, no. 1, pp. 97-100, Jul 8, 2004.
[91] A. L. Briseno, S. C. B. Mannsfeld, S. A. Jenekhe, Z. Bao *et al.*, "Introducing organic nanowire transistors," *Materials Today,* vol. 11, no. 4, pp. 38-47, Apr, 2008.
[92] M. D. Curtis, J. Cao, and J. W. Kampf, "Solid-state packing of conjugated oligomers: from pi-stacks to the herringbone structure," *Journal of the American Chemical Society,* vol. 126, no. 13, pp. 4318-4328, Apr 7, 2004.
[93] Sigma-Aldrich. "698989 Aldrich Poly(3-hexylthiophene-2,5-diyl) Specifications," Nov 20, 2013; http://www.sigmaaldrich.com/catalog/product/aldrich/698989?lang=en&region=GB.
[94] K. J. Ihn, J. Moulton, and P. Smith, "Whiskers of Poly(3-Alkylthiophene)S," *Journal of Polymer Science Part B-Polymer Physics,* vol. 31, no. 6, pp. 735-742, May, 1993.
[95] I. Mcculloch, M. Heeney, C. Bailey, K. Genevicius *et al.*, "Liquid-crystalline semiconducting polymers with high charge-carrier mobility," *Nature Materials,* vol. 5, no. 4, pp. 328-333, Apr, 2006.
[96] Ossila. "M141 PBTTT Product Information Page," Nov 19, 2013; http://www.ossila.com/oled_opv_ofet_catalogue3/PCDTBT_P3HT_PCBM_PEDOT_PSS_for_organic_photovoltaics/M141-PBTTT.php.
[97] M. Park, B. D. Chin, J.-W. Yu, M.-S. Chun *et al.*, "Enhanced photocurrent and efficiency of poly(3-hexylthiophene)/fullerene photovoltaic devices by the incorporation of gold nanoparticles," *Journal of Industrial and Engineering Chemistry,* vol. 14, no. 3, pp. 382-386, 2008.
[98] H. Yang, "Scanning Probe Techniques," *Organic Field-Effect Transistors*, Z. Bao and J. Locklin, eds., pp. 301-339: CRC Press, 2007.
[99] K. Terada, K. Nishiyama, and K.-I. Hatanaka, "Comparison of MOSFET-threshold-voltage extraction methods," *Solid-State Electronics,* vol. 45, no. 1, pp. 35-40, 2001.
[100] A. Ortiz-Conde, F. J. G. Sanchez, J. J. Liou, A. Cerdeira *et al.*, "A review of recent MOSFET threshold voltage extraction methods," *Microelectronics Reliability,* vol. 42, no. 4-5, pp. 583-596, Apr-May, 2002.
[101] C. Ucurum, H. Siemund, and H. Göbel, "Impact of electrical measurement parameters on the hysteresis behavior of pentacene-based organic thin-film transistors," *Organic Electronics,* vol. 11, no. 9, pp. 1523-1528, 2010.
[102] S. Y. Park, M. Park, and H. H. Lee, "Cooperative polymer gate dielectrics in organic thin-film transistors," *Applied Physics Letters,* vol. 85, no. 12, pp. 2283-2285, 2004.
[103] IEEE, "IEEE Standard Test Methods for the Characterization of Organic Transistors and Materials," 2004.
[104] U. Zschieschang, R. T. Weitz, K. Kern, and H. Klauk, "Bias stress effect in low-voltage organic thin-film transistors," *Applied Physics a-Materials Science & Processing,* vol. 95, no. 1, pp. 139-145, Apr, 2009.
[105] B. M. Dhar, R. Özgün, T. Dawidczyk, A. Andreou *et al.*, "Threshold voltage shifting for memory and tuning in printed transistor circuits," *Materials Science and Engineering: R: Reports,* vol. 72, no. 4, pp. 49-80, 2011.
[106] Y. H. Noh, S. Y. Park, S. M. Seo, and H. H. Lee, "Root cause of hysteresis in organic thin film transistor with polymer dielectric," *Organic Electronics,* vol. 7, no. 5, pp. 271-275, Oct, 2006.
[107] P. Stallinga, H. L. Gomes, F. Biscarini, M. Murgia *et al.*, "Electronic transport in field-effect transistors of sexithiophene," *Journal of Applied Physics,* vol. 96, no. 9, pp. 5277-5283, Nov 1, 2004.
[108] D. Duarte, D. Sharma, B. Cobb, and A. Dodabalapur, "Charge transport and trapping in organic field effect transistors exposed to polar analytes," *Applied Physics Letters,* vol. 98, no. 13, 2011.
[109] G. Horowitz, M. Mottaghi, P. Lang, F. Rodriguez *et al.*, "On the crucial role of the insulator-semiconductor interface in organic thin-film transistors," *Organic Field-Effect Transistors V,* vol. 6336, pp. U65-U75, 2006.
[110] Goodfellow. "Polyethylene - Low Density. Material Information," Nov 1, 2013; http://www.goodfellow.com/E/Polyethylene-Low-Density.html.
[111] J. Dong, A. Wang, K. Y. S. Ng, and G. Mao, "Self-assembly of octadecyltrichlorosilane monolayers on silicon-based substrates by chemical vapor deposition," *Thin Solid Films,* vol. 515, no. 4, pp. 2116-2122, 2006.
[112] H. Klauk, M. Halik, U. Zschieschang, F. Eder *et al.*, "Pentacene organic transistors and ring oscillators on glass and on flexible polymeric substrates," *Applied Physics Letters,* vol. 82, no. 23, pp. 4175-4177, Jun 9, 2003.
[113] S. Jung, T. Ji, and V. K. Varadan, "Temperature sensor using thermal transport properties in the subthreshold regime of an organic thin film transistor," *Applied Physics Letters,* vol. 90, no. 6, 2007.
[114] L. Hague, D. Puzzovio, T. H. Richardson, and M. Grell, "Discovery of a New Odour Sensing Mechanism Using an n-Type Organic Transistor," *Sensor Letters,* vol. 9, no. 5, pp. 1692-1696, Oct, 2011.

[115] J. Park, S. Y. Park, S. O. Shim, H. Kang *et al.*, "A polymer gate dielectric for high-mobility polymer thin-film transistors and solvent effects," *Applied Physics Letters,* vol. 85, no. 15, pp. 3283-3285, Oct 11, 2004.

[116] J. H. Cho, D. H. Kim, Y. Jang, W. H. Lee *et al.*, "Effects of metal penetration into organic semiconductors on the electrical properties of organic thin film transistors," *Applied Physics Letters,* vol. 89, no. 13, 2006.

[117] S. Takebayashi, S. Abe, K. Saiki, and K. Ueno, "Origin of the ambipolar operation of a pentacene field-effect transistor fabricated on a poly(vinyl alcohol)-coated Ta2O5 gate dielectric with Au source/drain electrodes," *Applied Physics Letters,* vol. 94, no. 8, 2009.

[118] I. M. Graz, and S. P. Lacour, "Flexible pentacene organic thin film transistor circuits fabricated directly onto elastic silicone membranes," *Applied Physics Letters,* vol. 95, no. 24, 2009.

[119] T. hubergroup, "Conventional inks for continuous forms of printing," http://www.hubergroup.info/lang/en/tipdf/3201E.PDF, 2004].

[120] Xerox. "Xerox® Supplies and Specialty Media Portfolio," Oct 25, 2013; http://www.xerox.com/downloads/usa/en/s/Supplies_Specialty_Media_Catalog.pdf.

[121] F. Liscio, S. Milita, C. Albonetti, P. D'Angelo *et al.*, "Structure and Morphology of PDI8-CN2 for n-Type Thin-Film Transistors," *Advanced Functional Materials,* vol. 22, no. 5, pp. 943-953, 2012.

[122] J. M. Choi, J. Lee, D. K. Hwang, J. H. Kim *et al.*, "Comparative study of the photoresponse from tetracene-based and pentacene-based thin-film transistors," *Applied Physics Letters,* vol. 88, no. 4, Jan 23, 2006.

[123] B. H. Hamadani, D. J. Gundlach, I. McCulloch, and M. Heeney, "Undoped polythiophene field-effect transistors with mobility of 1 cm(2) V(-1) s(-1)," *Applied Physics Letters,* vol. 91, no. 24, Dec 10, 2007.

[124] I. McCulloch, M. Heeney, M. L. Chabinyc, D. DeLongchamp *et al.*, "Semiconducting Thienothiophene Copolymers: Design, Synthesis, Morphology, and Performance in Thin-Film Organic Transistors," *Advanced Materials,* vol. 21, no. 10-11, pp. 1091-1109, 2009.

[125] Samsung. "Galaxy S: A New Era in AMOLED Technology," Nov 26, 2013; http://www.samsung.com/uk/article/galaxy-s-a-new-era-in-amoled-technology.

[126] LG. "LG Unveils World's First "Real" Curved Smartphone," Nov 26, 2013; http://www.lgnewsroom.com/newsroom/contents/63988.

[127] S. DasGupta, R. J. Kaplar, S. Atcitty, and M. J. Marinella, "Photocapacitance Decay Technique for Interface Trap Characterization Near Inversion Band in Wide Bandgap MOS Capacitors," *Ieee Transactions on Electron Devices,* vol. 60, no. 8, pp. 2619-2625, Aug, 2013.

[128] M. Marchywka, and D. Moses, "Optical Characterization of Diamond Mis Capacitors," *Ieee Transactions on Electron Devices,* vol. 41, no. 7, pp. 1265-1272, Jul, 1994.

[129] C. P. Watson, M. Devynck, and D. M. Taylor, "Photon-assisted capacitance-voltage study of organic metal-insulator-semiconductor capacitors," *Organic Electronics,* vol. 14, no. 7, pp. 1728-1736, Jul, 2013.

[130] A. I. Kingon, J. P. Maria, and S. K. Streiffer, "Alternative dielectrics to silicon dioxide for memory and logic devices," *Nature,* vol. 406, no. 6799, pp. 1032-1038, Aug 31, 2000.

[131] S. Scheinert, and G. Paasch, "Fabrication and Analysis of Polymer Field-Effect Transistors," *Physics of Organic Semiconductors*, W. Brütting, ed., pp. 343-392: Wiley, 2005.

[132] Y. Y. Noh, and H. Sirringhaus, "Ultra-thin polymer gate dielectrics for top-gate polymer field-effect transistors," *Organic Electronics,* vol. 10, no. 1, pp. 174-180, Feb, 2009.

[133] L. A. Majewski, R. Schroeder, and M. Grell, "One volt organic transistor," *Advanced Materials,* vol. 17, no. 2, pp. 192, Jan 31, 2005.

[134] R. Schroeder, L. A. Majewski, and M. Grell, "High-performance organic transistors using solution-processed nanoparticle-filled high-kappa polymer gate insulators," *Advanced Materials,* vol. 17, no. 12, pp. 1535-1539, Jun 17, 2005.

[135] T. W. Kelley, D. V. Muyres, P. F. Baude, T. P. Smith *et al.*, "High performance organic thin film transistors," *Organic and Polymeric Materials and Devices,* vol. 771, pp. 169-179, 2003.

[136] W. L. Kalb, and B. Batlogg, "Calculating the trap density of states in organic field-effect transistors from experiment: A comparison of different methods," *Physical Review B,* vol. 81, no. 3, Jan, 2010.

[137] A. Salleo, and R. A. Street, "Light-induced bias stress reversal in polyfluorene thin-film transistors," *Journal of Applied Physics,* vol. 94, no. 1, pp. 471-479, Jul 1, 2003.

[138] L. M. Smieska, V. A. Pozdin, J. L. Luria, R. G. Hennig *et al.*, "Following Chemical Charge Trapping in Pentacene Thin Films by Selective Impurity Doping and Wavelength-Resolved Electric Force Microscopy," *Advanced Functional Materials,* vol. 22, no. 24, pp. 5096-5106, Dec 19, 2012.

[139] C. G. Feng, T. Mei, X. A. Hu, and N. Pavel, "A pentacene field-effect transistor with light-programmable threshold voltage," *Organic Electronics,* vol. 11, no. 11, pp. 1713-1718, Nov, 2010.

[140] Y. Yang, R. C. da Costa, M. J. Fuchter, and A. J. Campbell, "Circularly polarized light detection by a chiral organic semiconductor transistor," *Nature Photonics,* vol. 7, no. 8, pp. 634-638, Aug, 2013.

[141] L. W. Shang, Z. Y. Ji, H. Wang, Y. P. Chen *et al.*, "Threshold Voltage Tuning of Low-Voltage Organic Thin-Film Transistors," *Ieee Transactions on Electron Devices,* vol. 58, no. 7, pp. 2127-2134, Jul, 2011.

[142] H. L. Gomes, P. Stallinga, F. Dinelli, M. Murgia *et al.*, "Bias-induced threshold voltages shifts in thin-film organic transistors," *Applied Physics Letters,* vol. 84, no. 16, pp. 3184-3186, Apr 19, 2004.

[143] R. vanLangevelde, and F. M. Klaassen, "Effect of gate-field dependent mobility degradation on distortion analysis in MOSFET's," *Ieee Transactions on Electron Devices,* vol. 44, no. 11, pp. 2044-2052, Nov, 1997.

[144] T. J. Krutsick, and M. H. White, "Consideration of Doping Profiles in Mosfet Mobility Modeling," *Ieee Transactions on Electron Devices,* vol. 35, no. 7, pp. 1153-1155, Jul, 1988.
[145] M. Mottaghi, and G. Horowitz, "Field-induced mobility degradation in pentacene thin-film transistors," *Organic Electronics,* vol. 7, no. 6, pp. 528-536, Dec, 2006.
[146] C. Moglestue, J. Rosenzweig, J. Kuhl, M. Klingenstein *et al.*, "Picosecond Pulse Response Characteristics of Gaas Metal-Semiconductor-Metal Photodetectors," *Journal of Applied Physics,* vol. 70, no. 4, pp. 2435-2448, Aug 15, 1991.
[147] W. C. Koscielniak, J. L. Pelouard, and M. A. Littlejohn, "Dynamic Behavior of Photocarriers in a Gaas Metal-Semiconductor-Metal Photodetector with Sub-Half-Micron Electrode Pattern," *Applied Physics Letters,* vol. 54, no. 6, pp. 567-569, Feb 6, 1989.
[148] I. H. Campbell, and B. K. Crone, "Improving an organic photodiode by incorporating a tunnel barrier between the donor and acceptor layers," *Applied Physics Letters,* vol. 101, no. 2, Jul 9, 2012.
[149] Zeiss. "Tungsten-Halogen Incandescent Lamps," 09 Oct 2013, 2013; http://zeiss-campus.magnet.fsu.edu/articles/lightsources/tungstenhalogen.html.
[150] Z. Chen, and C. Lu, "Humidity sensors: A review of materials and mechanisms," *Sensor Letters,* vol. 3, no. 4, pp. 274-295, Dec, 2005.
[151] D. Patil, and P. Patil, "A Rapid Response Humidity Sensor Based on Poly(2,5-dimethoxyaniline)-tin Oxide Nanocomposite," *Sensor Letters,* vol. 9, no. 4, pp. 1298-1308, Aug, 2011.
[152] A. S. G. Reddy, B. B. Narakathu, M. Z. Atashbar, M. Rebros *et al.*, "Printed Capacitive Based Humidity Sensors on Flexible Substrates," *Sensor Letters,* vol. 9, no. 2, pp. 869-871, Apr, 2011.
[153] Q. Wang, Y. Z. Pan, S. S. Huang, S. T. Ren *et al.*, "Resistive and capacitive response of nitrogen-doped TiO2 nanotubes film humidity sensor," *Nanotechnology,* vol. 22, no. 2, Jan 14, 2011.
[154] K. S. Karimov, M. M. Ahmed, Z. M. Karieva, M. Saleem *et al.*, "Humidity Sensing Properties of Carbon Nano-Tube Thin Films," *Sensor Letters,* vol. 9, no. 5, pp. 1649-1653, Oct, 2011.
[155] S. Lei, D. J. Chen, W. Chen, and Y. Q. Chen, "A Promising Surface Acoustic Wave Humidity Sensor Based on Multi-Walled Carbon Nanotubes/Nafion Composite Film for Low Humidity Detection," *Sensor Letters,* vol. 9, no. 5, pp. 1606-1611, Oct, 2011.
[156] H. H. Liao, C. M. Yang, C. C. Liu, S. F. Horng *et al.*, "Dynamics and reversibility of oxygen doping and de-doping for conjugated polymer," *Journal of Applied Physics,* vol. 103, no. 10, May 15, 2008.
[157] M. S. A. Abdou, F. P. Orfino, Y. Son, and S. Holdcroft, "Interaction of oxygen with conjugated polymers: Charge transfer complex formation with poly(3-alkylthiophenes)," *Journal of the American Chemical Society,* vol. 119, no. 19, pp. 4518-4524, May 14, 1997.
[158] S. Hoshino, M. Yoshida, S. Uemura, T. Kodzasa *et al.*, "Influence of moisture on device characteristics of polythiophene-based field-effect transistors," *Journal of Applied Physics,* vol. 95, no. 9, pp. 5088-5093, May 1, 2004.
[159] E. Leary, H. Hobenreich, S. J. Higgins, H. van Zalinge *et al.*, "Single-Molecule Solvation-Shell Sensing," *Physical Review Letters,* vol. 102, no. 8, Feb 27, 2009.
[160] S. Samitsu, T. Shimomura, S. Heike, T. Hashizume *et al.*, "Effective Production of Poly(3-alkylthiophene) Nanofibers by means of Whisker Method using Anisole Solvent: Structural, Optical, and Electrical Properties," *Macromolecules,* vol. 41, no. 21, pp. 8000-8010, Nov 11, 2008.
[161] K. Nomura, M. Fujimaki, K. Awazu, and T. Komatsubara, "Size control of nanopores formed on SiO2 glass by swift-heavy-ion irradiation and its application to highly sensitive biomolecular detection," *Journal of Vacuum Science & Technology A,* vol. 29, no. 5, Sep, 2011.
[162] J. X. Huang, S. Virji, B. H. Weiller, and R. B. Kaner, "Polyaniline nanofibers: Facile synthesis and chemical sensors," *Journal of the American Chemical Society,* vol. 125, no. 2, pp. 314-315, Jan 15, 2003.
[163] A. L. Briseno, S. C. B. Mannsfeld, X. Lu, Y. Xiong *et al.*, "Fabrication of Field-Effect Transistors from Hexathiapentacene Single-Crystal Nanowires," *Nano Letters,* vol. 7, no. 3, pp. 668-675, 2007/03/01, 2007.
[164] I. Palacios, R. Castillo, and R. A. Vargas, "Thermal and transport properties of the polymer electrolyte based on poly(vinyl alcohol)-KOH-H2O," *Electrochimica Acta,* vol. 48, no. 14-16, pp. 2195-2199, Jun 30, 2003.
[165] A. Dragoneas, M. Grell, M. Hampton, and J. E. Macdonald, "Morphology-Driven Sensitivity Enhancement in Organic Nanowire Chemiresistors," *Sensor Letters,* vol. 11, pp. 552, 2013.
[166] R. A. Street, M. L. Chabinyc, and F. Endicott, "Chemical impurity effects on transport in polymer transistors," *Physical Review B,* vol. 76, no. 4, Jul, 2007.
[167] J. Kettle, S. Whitelegg, A. M. Song, D. C. Wedge *et al.*, "Fabrication of planar organic nanotransistors using low temperature thermal nanoimprint lithography for chemical sensor applications," *Nanotechnology,* vol. 21, no. 7, Feb 19, 2010.
[168] W. M. Haynes, *CRC Handbook of Chemistry and Physics 2011-2012*: Taylor & Francis, 2011.
[169] Sigma-Aldrich. "02854 Fluka Ethanol for HPLC Product Specifications," Nov 20, 2013; http://www.sigmaaldrich.com/catalog/product/fluka/02854?lang=en&region=GB.
[170] S. Takeda, and M. Fukawa, "Surface OH groups governing surface chemical properties of SiO2 thin films deposited by RF magnetron sputtering," *Thin Solid Films,* vol. 444, no. 1–2, pp. 153-157, 2003.
[171] S. Huttner, M. Sommer, A. Chiche, G. Krausch *et al.*, "Controlled solvent vapour annealing for polymer electronics," *Soft Matter,* vol. 5, no. 21, pp. 4206-4211, 2009.

[172] Sigma-Aldrich. "293245 Sigma-Aldrich 1-Octanol Chromasolv® for HPLC Product Specifications," Nov 20, 2013; http://www.sigmaaldrich.com/catalog/product/sial/293245?lang=en&region=GB.

[173] M. Taniguchi, and T. Kawai, "Vertical electrochemical transistor based on poly(3-hexylthiophene) and cyanoethylpullulan," *Applied Physics Letters,* vol. 85, no. 15, pp. 3298-3300, 2004.

[174] Sigma-Aldrich. "1-Butanol (for HPLC) 03-4585 SAJ Product Specifications," Nov 17, 2013; http://www.sigmaaldrich.com/catalog/product/saj/034585?lang=en&region=GB.

[175] Sigma-Aldrich. "Octylamine (≥99.5%) 74988 Product Specifications," 24 Sep 2013, 2013; http://www.sigmaaldrich.com/catalog/product/aldrich/74988?lang=en&region=GB.

[176] M. H. Silla Santos, "Biogenic amines: Their importance in foods," *International Journal of Food Microbiology,* vol. 29, no. 2-3, pp. 213-231, Apr, 1996.

[177] K. H. Lee, K. Lee, M. S. Oh, J. M. Choi *et al.*, "Flexible high mobility pentacene transistor with high-k/low-k double polymer dielectric layer operating at-5V," *Organic Electronics,* vol. 10, no. 1, pp. 194-198, Feb, 2009.

[178] T. Sekitani, U. Zschieschang, H. Klauk, and T. Someya, "Flexible organic transistors and circuits with extreme bending stability," *Nature Materials,* vol. 9, no. 12, pp. 1015-1022, Dec, 2010.

[179] U. Zschieschang, F. Ante, T. Yamamoto, K. Takimiya *et al.*, "Flexible Low-Voltage Organic Transistors and Circuits Based on a High-Mobility Organic Semiconductor with Good Air Stability," *Advanced Materials,* vol. 22, no. 9, pp. 982, Mar 5, 2010.

[180] D. K. Lee, S. C. Lee, Y. G. Seol, J. H. Ahn *et al.*, "Deformation Characteristics of an Organic Thin Film Transistor," *Journal of Nanoscience and Nanotechnology,* vol. 11, no. 1, pp. 239-242, Jan, 2011.

Publications and presentations

Journal publications

L. Hague, D. Puzzovio, A. Dragoneas and M. Grell, "Simplified Real-Time Organic Transistor Characterisation Schemes for Sensing Applications," ***Science of Advanced Materials,*** vol. **3**, no. 6, pp. 907-911, Dec, 2011.

H. AlQahtani, D. Puzzovio, A. Dragoneas, T. Richardson and M. Grell, "A swelling-based chemiresistor for a biogenic odour," ***Talanta,*** vol. **99**, pp. 50-54, Sep 15, 2012.

A. Dragoneas, M. Grell, M. Hampton and J. E. Macdonald, "Morphology-Driven Sensitivity Enhancement in Organic Nanowire Chemiresistors," ***Sensor Letters,*** vol. **11**, no. 3, pp. 552-555, Mar, 2013.

A. Al Naim, A. Hobson, R. T. Grant, A. Dragoneas, M. Hampton, C. Dunscombe, T. Richardson *and M. Grell*, "Water-gated organic nanowire transistors," ***Organic Electronics,*** vol. **14**, no. 4, pp. 1057-1063, Apr, 2013.

A. Dragoneas, L. Hague, and M. Grell, "An electrical characterisation system for the acquisition of multiple independent sensing parameters from organic thin film transistors," (submitted – under review)

Conference and meeting presentations

D. Puzzovio, L. Hague, A. Dragoneas and M. Grell, "Technology platforms for organic transistor sensors," (poster presentation), ***ElecMOL'10****, Grenoble, France*, Dec, 2010

A. Dragoneas, L. Hague, D. Puzzovio and M. Grell, "Characterisation of Organic Sensor Transistors," (poster presentation), ***UK Semiconductors '11****, Sheffield, United Kingdom*, Jul, 2011

D.Puzzovio, L. Hague, A. Dragoneas and M. Grell, "Real-time characterisation schemes for organic transistor-sensor systems," (oral presentation of D. Puzzovio), ***ISFOE11****, Thessaloniki, Greece*, *Jul, 2011*

A. Dragoneas, M. Grell, D. Puzzovio, and L. Hague, "Characterisation of organic transistor gas sensors," (oral presentation), *Seminar talk in* ***École Polytechnique de Montréal****, Montreal, Canada*, Dec, 2011

A. Dragoneas, D. Puzzovio, L. Hague and M. Grell, "Characterisation of organic semiconductor gas sensors," (oral presentation), ***FlexSMELL 2nd Annual Meeting****, Bari, Italy*, Jan, 2012

A. Dragoneas, L. Hague, A.F.M. Al Naim, D. Puzzovio, T. Richardson, M. Grell, K. Manoli, M.Y. Mulla, L. Dumitru, L. Torsi, M. Hampton, J.E. Macdonald, "An electric read-out scheme compatible with sensor TFTs," (oral presentation), ***UK Semiconductors '12****, Sheffield, United Kingdom*, Jul, 2012

A. Dragoneas, L. Hague, D. Puzzovio, M. Grell, M. Hampton, J. E. Macdonald, K. Manoli, L. Torsi, "Organic Semiconductor Devices: Preparation, Characterisation and Sensing Applications," (poster presentation), ***Physics and Astronomy Department****: Posters-out Day, Sheffield, United Kingdom*, Sep, 2012

A. Dragoneas, A. F. M. Al Naim, A. Hobson, T. Richardson, M. Grell, M. Hampton and J. E. Macdonald, "Polythiophene nanowire thin-film devices," (poster presentation), ***MRS Fall Meeting 2012****, Boston, United States*, Nov, 2012

A. Dragoneas, D. Puzzovio, A. Al Naim, R. T. Grant, A. Hobson, N. Christogiannis, M. Grell, M. Hampton, C. Dunscombe, T. Richardson, J. E. Macdonald, K. Manoli, M. Y. Mulla, L. Dumitru and L. Torsi, "An overview of the contribution of USFD to FlexSMELL", ***FlexSMELL 2nd Annual Meeting****, Oulu, Finland*, Jan, 2013

A. Dragoneas, N. Christogiannis and M. Grell, "The dependence of OFET environmental stability on the gate dielectric surface," (oral presentation), ***ISFOE13****, Thessaloniki, Greece*, *Jul, 2013*

A. Dragoneas, L. Hague, A. Hobson and M. Grell, "Alcohol vapour sensing with PBTTT OFETs," (poster presentation), ***Asiasense 2013****, Malacca, Malaysia*, *Aug, 2013*

Awards

Second prize, *UK Semiconductors '11 poster competition, Sheffield, United Kingdom*, Jul, 2011

Best poster award, *Asiasense 2013 poster competition, Malacca, Malaysia*, *Aug, 2013*

Appendices

Appendix I Sinusoidal integration method derivations

Appendix I.1. Integration method for (π/4, 3π/4)

Integrating (4.15) over this time range yields:

$$\frac{A}{R_f} = \int_{t=T/12}^{t=5T/12} k(V_G - V_{th})^2 \, dt \tag{8.1}$$

$$\frac{A}{R_f} = k\int_{t=T/12}^{t=5T/12} \left({V_G}^2 - 2V_G V_{th} + {V_{th}}^2\right) dt \tag{8.2}$$

$$\frac{A}{R_f} = k\left[\int_{t=T/12}^{t=5T/12} {V_G}^2 \, dt - 2V_{th}\int_{t=T/12}^{t=5T/12} V_G dt + \int_{t=T/12}^{t=5T/12} {V_{th}}^2 \, dt\right] \tag{8.3}$$

$$\frac{A}{R_f} = k\left[\left(\int_{t=T/12}^{t=5T/12} (V_0 \sin(2\pi f t))^2 \, dt\right) - \left(2V_{th}\int_{t=T/12}^{t=5T/12} V_0 \sin(2\pi f t)\, dt\right) + \left({V_{th}}^2 [\, t]_{t=T/12}^{t=5T/12}\right)\right] \tag{8.4}$$

$$\frac{A}{R_f} = k\left[{V_0}^2\left(\int_{t=T/12}^{t=5T/12} \sin^2(2\pi f t)\ dt\right) - \left(2V_{th}V_0\int_{t=T/12}^{t=5T/12} \sin(2\pi f t)\, dt\right) + \left({V_{th}}^2 \times \frac{T}{3}\right)\right] \tag{8.5}$$

$$\frac{A}{kR_f} = {V_0}^2\left(\int_{t=T/12}^{t=5T/12} \frac{1}{2}(1 - \cos(2 \times 2\pi f t))\, dt\right) - \left(2V_{th}V_0\int_{t=T/12}^{t=5T/12} \sin(2\pi f t)\, dt\right) + \left({V_{th}}^2 \times \frac{T}{3}\right) \tag{8.6}$$

Let: $z = 2\pi f t$

$$\frac{A}{kR_f} = \frac{{V_0}^2}{2}\left(\int_{t=T/12}^{t=5T/12} (1 - \cos(2 \times 2\pi f t))\, dt\right) - \left(2V_{th}V_0\frac{1}{2\pi f}\int_{z=2\pi f T/12}^{z=2\pi f 5T/12} \sin(z)\, dz\right) + \left(\frac{T}{3}{V_{th}}^2\right) \tag{8.7}$$

$$\frac{A}{kR_f} = \frac{{V_0}^2}{2}\left(\frac{T}{3} - \left(\int_{t=T/12}^{t=5T/12} (\cos(4\pi f t))\, dt\right)\right) - \left(V_{th}V_0\frac{T}{\pi}[-\cos z]_{z=\pi/6}^{z=5\pi/6}\right) + \left(\frac{T}{3}V_{th}\right)^2 \tag{8.8}$$

$$\frac{A}{kR_f} = \frac{{V_0}^2}{2}\left(\frac{T}{3} - \left(\int_{t=T/12}^{t=5T/12} (\cos(4\pi f t))\, dt\right)\right) + \left(\frac{T}{\pi}V_{th}V_0\left(\cos\left(\frac{5\pi}{6}\right) - \cos\left(\frac{\pi}{6}\right)\right)\right) + \left(\frac{T}{3}{V_{th}}^2\right) \tag{8.9}$$

Let: $y = 4\pi f t$

$$\frac{A}{kR_f} = \frac{{V_0}^2}{2}\left(\frac{T}{3} - \frac{1}{4\pi f}\left(\int_{y=4\pi f T/12}^{y=4\pi f 5T/12} (\cos(y))\, dy\right)\right) + \left(\frac{T}{\pi}V_{th}V_0(-\sqrt{3})\right) + \left(\frac{T}{3}{V_{th}}^2\right) \tag{8.10}$$

$$\frac{A}{kR_f} = \frac{{V_0}^2}{2}\left(\frac{T}{3} - \frac{T}{4\pi}[\sin(y)]_{y=\pi/3}^{y=5\pi/3}\right) + \left(\frac{T}{\pi}V_{th}V_0(-\sqrt{3})\right) + \left(\frac{T}{3}{V_{th}}^2\right) \tag{8.11}$$

$$\frac{A}{kR_f} = \frac{{V_0}^2}{2}T\left(\frac{1}{3} - \frac{1}{4\pi}\left(\sin\left(\frac{5\pi}{3}\right) - \sin\left(\frac{\pi}{3}\right)\right)\right) + \left(\frac{T}{\pi}V_{th}V_0(-\sqrt{3})\right) + \left(\frac{T}{3}{V_{th}}^2\right) \tag{8.12}$$

$$\frac{A}{kR_f} = \frac{{V_0}^2}{2}T\left(\frac{1}{3} + \frac{\sqrt{3}}{4\pi}\right) - \left(\frac{T}{\pi}V_{th}V_0(\sqrt{3})\right) + \left(\frac{T}{3}{V_{th}}^2\right) \tag{8.13}$$

$$\frac{T}{3}{V_{th}}^2 - \frac{\sqrt{3}T}{\pi}V_0V_{th} + \frac{\left(\frac{1}{3} + \frac{\sqrt{3}}{4\pi}\right)T}{2}{V_0}^2 = \frac{A}{kR_f} \tag{8.14}$$

$${V_{th}}^2 - \frac{3\sqrt{3}}{\pi}V_0V_{th} + \frac{3}{2}\left(\frac{1}{3} + \frac{\sqrt{3}}{4\pi}\right){V_0}^2 - \frac{3A}{kR_fT} = 0 \tag{8.15}$$

Substituting (4.14) into (8.15):

$${V_{th}}^2 - \frac{3\sqrt{3}}{\pi}V_0V_{th} + \frac{3}{2}\left(\frac{1}{3} + \frac{\sqrt{3}}{4\pi}\right){V_0}^2 - \frac{3A}{\mu C_i\frac{W}{2L}R_fT} = 0 \tag{8.16}$$

Also, at the peak of the output waveform, eq. (4.13) writes:

$$I_d = \frac{V_m}{R_f} = \mu C_i\frac{W}{2L}(V_0 - V_{th})^2 \tag{8.17}$$

$$\mu = \frac{2LV_m}{C_iWR_f(V_0 - V_{th})^2} \tag{8.18}$$

where V_m is the maximum output voltage

Substituting (8.18) into (8.16) yields:

$${V_{th}}^2 - \frac{3\sqrt{3}}{\pi}V_0V_{th} + \frac{3}{2}\left(\frac{1}{3} + \frac{\sqrt{3}}{4\pi}\right){V_0}^2 - \frac{3A}{\frac{2LV_m}{C_iWR_f(V_0 - V_{th})^2}C_i\frac{W}{2L}R_fT} = 0 \tag{8.19}$$

$${V_{th}}^2 - \frac{3\sqrt{3}}{\pi}V_0V_{th} + \frac{3}{2}\left(\frac{1}{3} + \frac{\sqrt{3}}{4\pi}\right){V_0}^2 - \frac{3A(V_0 - V_{th})^2}{TV_m} = 0 \tag{8.20}$$

$${V_{th}}^2 - \frac{3\sqrt{3}}{\pi}V_0V_{th} + \frac{3}{2}\left(\frac{1}{3} + \frac{\sqrt{3}}{4\pi}\right){V_0}^2 - \frac{3A}{TV_m}\left({V_0}^2 - 2V_0V_{th} + {V_{th}}^2\right) = 0 \tag{8.21}$$

$${V_{th}}^2 - \frac{3\sqrt{3}}{\pi}V_0V_{th} + \left(\frac{1}{2} + \frac{3\sqrt{3}}{8\pi}\right){V_0}^2 - \frac{3A}{TV_m}{V_0}^2 + \frac{6A}{TV_m}V_0V_{th} - \frac{3A}{TV_m}{V_{th}}^2 = 0 \tag{8.22}$$

$$\left(1 - \frac{3A}{TV_m}\right){V_{th}}^2 + \left(\frac{6A}{TV_m}V_0 - \frac{3\sqrt{3}}{\pi}V_0\right)V_{th} + \left(\frac{1}{2} + \frac{3\sqrt{3}}{8\pi} - \frac{3A}{TV_m}\right){V_0}^2 = 0 \tag{8.23}$$

$$\Delta = \left(\frac{6A}{TV_m}V_0 - \frac{3\sqrt{3}}{\pi}V_0\right)^2 - 4\left(1 - \frac{3A}{TV_m}\right)\left(\frac{1}{2} + \frac{3\sqrt{3}}{8\pi} - \frac{3A}{TV_m}\right){V_0}^2 \tag{8.24}$$

$$\Delta = \left(36\left(\frac{A}{TV_m}\right)^2 {V_0}^2 - \frac{36\sqrt{3}}{\pi}\left(\frac{A}{TV_m}\right){V_0}^2 + \frac{27}{\pi^2}{V_0}^2\right) + \left(\frac{12A}{TV_m} - 4\right)\left(\frac{1}{2} + \frac{3\sqrt{3}}{8\pi} - \frac{3A}{TV_m}\right){V_0}^2 \tag{8.25}$$

$$\Delta = \left(\left(36\left(\frac{A}{TV_m}\right)^2 - \frac{36\sqrt{3}}{\pi}\left(\frac{A}{TV_m}\right) + \frac{27}{\pi^2}\right) + \left(6\frac{A}{TV_m} + \frac{36\sqrt{3}}{8\pi}\frac{A}{TV_m} - 36\left(\frac{A}{TV_m}\right)^2 - 2 - \frac{3\sqrt{3}}{2\pi} + 12\frac{A}{TV_m}\right)\right){V_0}^2 \tag{8.26}$$

$$\Delta = \left(\left(6 + 12 + \frac{36\sqrt{3}}{8\pi} - \frac{36\sqrt{3}}{\pi}\right)\frac{A}{TV_m} + \frac{27}{\pi^2} - 2 - \frac{3\sqrt{3}}{2\pi}\right){V_0}^2 \tag{8.27}$$

$$\Delta = \left(\left(18 - \frac{63\sqrt{3}}{2\pi}\right)\frac{A}{TV_m} + \frac{27}{\pi^2} - 2 - \frac{3\sqrt{3}}{2\pi}\right){V_0}^2 \tag{8.28}$$

Finally:

$$\mathbf{V_{th}} = \frac{\boldsymbol{V_0}}{\mathbf{2}}\left(\frac{\left(\frac{\boldsymbol{3\sqrt{3}}}{\boldsymbol{\pi}} - \frac{\boldsymbol{6A}}{\boldsymbol{TV_m}}\right) \pm \sqrt{\left(\left(\boldsymbol{18} - \frac{\boldsymbol{63\sqrt{3}}}{\boldsymbol{2\pi}}\right)\frac{\boldsymbol{A}}{\boldsymbol{TV_m}} + \frac{\boldsymbol{27}}{\boldsymbol{\pi^2}} - \mathbf{2} - \frac{\boldsymbol{3\sqrt{3}}}{\boldsymbol{2\pi}}\right)}}{\mathbf{1} - \mathbf{3}\frac{\mathbf{A}}{\boldsymbol{TV_m}}}\right) \tag{8.29}$$

where V_0 is the amplitude of the sinusoidal drive, V_m the peak of the output voltage, A the area between the output curve and x axis for the range $\left(\frac{\pi}{6}, \frac{5\pi}{6}\right)$ and T the period of the input signal.

Appendix I.2. Integration method for (π/4, π/2)

Integrating (4.15) over this time range:

$$\int_{t=T/8}^{t=T/4} I_d(t)dt = \int_{t=T/4}^{t=T/2} k(V_G - V_{th})^2\, dt \tag{8.30}$$

From the exported measurement data, we also have:

$$\int_{t=T/4}^{t=T/2} I_d(t)dt = \frac{A}{R_f} \tag{8.31}$$

where A is the Area between the output voltage curve and the x axis, and R_f the feedback resistance.

Substituting:

$$\frac{A}{R_f} = \int_{t=T/8}^{t=T/4} k(V_G - V_{th})^2\, dt \tag{8.32}$$

$$\frac{A}{R_f} = k\int_{t=T/8}^{t=T/4} \left({V_G}^2 - 2V_G V_{th} + {V_{th}}^2\right) dt \tag{8.33}$$

$$\begin{aligned}\frac{A}{R_f} &= k\left[\int_{t=T/8}^{t=T/4} {V_G}^2\, dt - 2V_{th}\int_{t=T/8}^{t=T/4} V_G dt + \int_{t=T/8}^{t=T/4} {V_{th}}^2\, dt\right]\frac{A}{R_f} \\ &= k\int_{t=T/8}^{t=T/4} \left({V_G}^2 - 2V_G V_{th} + {V_{th}}^2\right) dt\end{aligned} \tag{8.34}$$

$$\frac{A}{R_f} = k\left[\left(\int_{t=T/8}^{t=T/4} (V_0 \sin(2\pi f t))^2\, dt\right) - \left(2V_{th}\int_{t=T/8}^{t=T/4} V_0 \sin(2\pi f t)\, dt\right) + \left({V_{th}}^2 [\, t]_{t=T/8}^{t=T/4}\right)\right] \tag{8.35}$$

$$\frac{A}{R_f} = k\left[{V_0}^2\left(\int_{t=T/8}^{t=T/4} \sin^2(2\pi f t)\ dt\right) - \left(2V_{th}V_0\int_{t=T/8}^{t=T/4} \sin(2\pi f t)\, dt\right) + \left({V_{th}}^2 \times \frac{T}{8}\right)\right] \tag{8.36}$$

$$\frac{A}{kR_f} = {V_0}^2\left(\int_{t=T/8}^{t=T/4} \frac{1}{2}(1 - \cos(2 \times 2\pi f t))\, dt\right) - \left(2V_{th}V_0\int_{t=T/8}^{t=T/4} \sin(2\pi f t)\, dt\right) + \left({V_{th}}^2 \times \frac{T}{8}\right) \tag{8.37}$$

Let: $z = 2\pi f t$

$$\frac{A}{kR_f} = \frac{{V_0}^2}{2}\left(\int_{t=T/8}^{t=T/4} (1 - \cos(2 \times 2\pi f t))\, dt\right) - \left(2V_{th}V_0 \frac{1}{2\pi f}\int_{z=2\pi f T/8}^{z=2\pi f T/4} \sin(z)\, dz\right) + \left(\frac{T}{8}{V_{th}}^2\right) \tag{8.38}$$

$$\frac{A}{kR_f} = \frac{{V_0}^2}{2}\left(\frac{T}{8} - \left(\int_{t=T/8}^{t=T/4} (\cos(4\pi f t))\, dt\right)\right) - \left(V_{th}V_0\frac{T}{\pi}[-\cos z]_{z=\pi/4}^{z=\pi/2}\right) + \left(\frac{T}{8}{V_{th}}^2\right) \tag{8.39}$$

$$\frac{A}{kR_f} = \frac{{V_0}^2}{2}\left(\frac{T}{8} - \left(\int_{t=T/8}^{t=T/4} (\cos(4\pi f t))\, dt\right)\right) + \left(\frac{T}{\pi} V_{th} V_0 \left(\cos\left(\frac{\pi}{2}\right) - \cos\left(\frac{\pi}{4}\right)\right)\right) + \left(\frac{T}{8}{V_{th}}^2\right) \tag{8.40}$$

Let: $y = 4\pi f t$

$$\frac{A}{kR_f} = \frac{{V_0}^2}{2}\left(\frac{T}{8} - \frac{1}{4\pi f}\left(\int_{y={}^{4\pi f T}/_{8}}^{y={}^{4\pi f T}/_{4}} (\cos(y))\, dy\right)\right) + \left(\frac{T}{\pi} V_{th} V_0 \left(-\frac{\sqrt{2}}{2}\right)\right) + \left(\frac{T}{8}{V_{th}}^2\right) \tag{8.41}$$

$$\frac{A}{kR_f} = \frac{{V_0}^2}{2}\left(\frac{T}{8} - \frac{T}{4\pi}[\sin(y)]_{y={}^{\pi}/_{2}}^{y=\pi}\right) + \left(\frac{T}{\pi} V_{th} V_0 \left(-\frac{\sqrt{2}}{2}\right)\right) + \left(\frac{T}{8}{V_{th}}^2\right) \tag{8.42}$$

$$\frac{A}{kR_f} = \frac{{V_0}^2}{2} T\left(\frac{1}{8} - \frac{1}{4\pi}\left(\sin(\pi) - \sin\left(\frac{\pi}{2}\right)\right)\right) + \left(\frac{T}{\pi} V_{th} V_0 \left(-\frac{\sqrt{2}}{2}\right)\right) + \left(\frac{T}{8}{V_{th}}^2\right) \tag{8.43}$$

$$\frac{A}{kR_f T} = \frac{{V_0}^2}{2}\left(\frac{1}{8} + \frac{1}{4\pi}\right) - \left(\frac{1}{\pi} V_{th} V_0 \left(\frac{\sqrt{2}}{2}\right)\right) + \left(\frac{1}{8}{V_{th}}^2\right) \tag{8.44}$$

$$\frac{1}{8}{V_{th}}^2 - \frac{\sqrt{2}}{2\pi} V_0 V_{th} + \left(\frac{1}{16} + \frac{1}{8\pi}\right){V_0}^2 = \frac{A}{kR_f T} \tag{8.45}$$

$${V_{th}}^2 - \frac{4\sqrt{2}}{\pi} V_0 V_{th} + \left(\frac{1}{2} + \frac{1}{\pi}\right){V_0}^2 - \frac{8A}{kR_f T} = 0 \tag{8.46}$$

Substituting (4.14) into (8.46):

$${V_{th}}^2 - \frac{4\sqrt{2}}{\pi} V_0 V_{th} + \left(\frac{1}{2} + \frac{1}{\pi}\right){V_0}^2 - \frac{8A}{\mu C_i \frac{W}{2L} R_f T} = 0 \tag{8.47}$$

Also, at the peak of the output waveform, eq. (4.13) writes:

$$I_d = \frac{V_m}{R_f} = \mu C_i \frac{W}{2L}(V_0 - V_{th})^2 \tag{8.48}$$

$$\mu = \frac{2LV_m}{C_i W R_f (V_0 - V_{th})^2} \tag{8.49}$$

where V_m is the peak of the output voltage.

Substituting (8.49) into (8.47):

$${V_{th}}^2 - \frac{4\sqrt{2}}{\pi} V_0 V_{th} + \left(\frac{1}{2} + \frac{1}{\pi}\right){V_0}^2 - \frac{8A}{\frac{2LV_m}{C_i W R_f (V_0 - V_{th})^2} C_i \frac{W}{2L} R_f T} = 0 \tag{8.50}$$

$$V_{th}{}^2 - \frac{4\sqrt{2}}{\pi} V_0 V_{th} + \left(\frac{1}{2} + \frac{1}{\pi}\right) V_0{}^2 - \frac{8A(V_0 - V_{th})^2}{TV_m} = 0 \tag{8.51}$$

$$V_{th}{}^2 - \frac{4\sqrt{2}}{\pi} V_0 V_{th} + \left(\frac{1}{2} + \frac{1}{\pi}\right) V_0{}^2 - \frac{8A}{TV_m}\left(V_0{}^2 - 2V_0 V_{th} + V_{th}{}^2\right) = 0 \tag{8.52}$$

$$V_{th}{}^2 - \frac{4\sqrt{2}}{\pi} V_0 V_{th} + \left(\frac{1}{2} + \frac{1}{\pi}\right) V_0{}^2 - \frac{8A}{TV_m} V_0{}^2 + \frac{16A}{TV_m} V_0 V_{th} - \frac{8A}{TV_m} V_{th}{}^2 = 0 \tag{8.53}$$

$$\left(1 - \frac{8A}{TV_m}\right) V_{th}{}^2 + \left(\frac{16A}{TV_m} V_0 - \frac{4\sqrt{2}}{\pi} V_0\right) V_{th} + \left(\frac{1}{2} + \frac{1}{\pi} - \frac{8A}{TV_m}\right) V_0{}^2 = 0 \tag{8.54}$$

$$\Delta = \left(\frac{16A}{TV_m} V_0 - \frac{4\sqrt{2}}{\pi} V_0\right)^2 - 4\left(1 - \frac{8A}{TV_m}\right)\left(\frac{1}{2} + \frac{1}{\pi} - \frac{8A}{TV_m}\right) V_0{}^2 \tag{8.55}$$

$$\Delta = \left(256\left(\frac{A}{TV_m}\right)^2 V_0{}^2 - \frac{128\sqrt{2}}{\pi}\left(\frac{A}{TV_m}\right) V_0{}^2 + \frac{32}{\pi^2} V_0{}^2\right) + \left(\frac{32A}{TV_m} - 4\right)\left(\frac{1}{2} + \frac{1}{\pi} - \frac{8A}{TV_m}\right) V_0{}^2 \tag{8.56}$$

$$\begin{aligned}\Delta = \Bigg(&\left(256\left(\frac{A}{TV_m}\right)^2 V_0{}^2 - \frac{128\sqrt{2}}{\pi}\left(\frac{A}{TV_m}\right) V_0{}^2 + \frac{32}{\pi^2} V_0{}^2\right) \\ &+ \left(16\frac{A}{TV_m} + \frac{32}{\pi}\frac{A}{TV_m} - 256\left(\frac{A}{TV_m}\right)^2 - 2 - \frac{4}{\pi} + 32\frac{A}{TV_m}\right)\Bigg) V_0{}^2\end{aligned} \tag{8.57}$$

$$\Delta = \left(\left(48 + \frac{32}{\pi} - \frac{128\sqrt{2}}{\pi}\right)\frac{A}{TV_m} + \frac{32}{\pi^2} - 2 - \frac{4}{\pi}\right) V_0{}^2 \tag{8.58}$$

$$\Delta = 4\left(\left(12 + \frac{8 - 32\sqrt{2}}{\pi}\right)\frac{A}{TV_m} + \frac{8}{\pi^2} - \frac{1}{2} - \frac{1}{\pi}\right) V_0{}^2 \tag{8.59}$$

Finally:

$$\mathbf{V_{th}} = \boldsymbol{V_0}\left(\frac{\mathbf{2}\left(\frac{\sqrt{2}}{\boldsymbol{\pi}} - \frac{\mathbf{4}\boldsymbol{A}}{\boldsymbol{TV_m}}\right) \pm \sqrt{\left(\mathbf{12} + \frac{\mathbf{8} - \mathbf{32}\sqrt{\mathbf{2}}}{\boldsymbol{\pi}}\right)\frac{\boldsymbol{A}}{\boldsymbol{TV_m}} + \frac{\mathbf{8}}{\boldsymbol{\pi^2}} - \frac{\mathbf{1}}{\boldsymbol{\pi}} - \frac{\mathbf{1}}{\mathbf{2}}}}{\mathbf{1} - \mathbf{8}\frac{\boldsymbol{A}}{\boldsymbol{TV_m}}}\right) \tag{8.60}$$

where V_0 is the amplitude of the sinusoidal drive, A is the area between the output curve and x axis for the range $\left(\frac{\pi}{4}, \frac{\pi}{2}\right)$ and T the period of the input signal.

Appendix II Printed Circuit Board (PCB) design

Appendix II.1. The I-V converter main board

Appendix II.1.1. Schematic

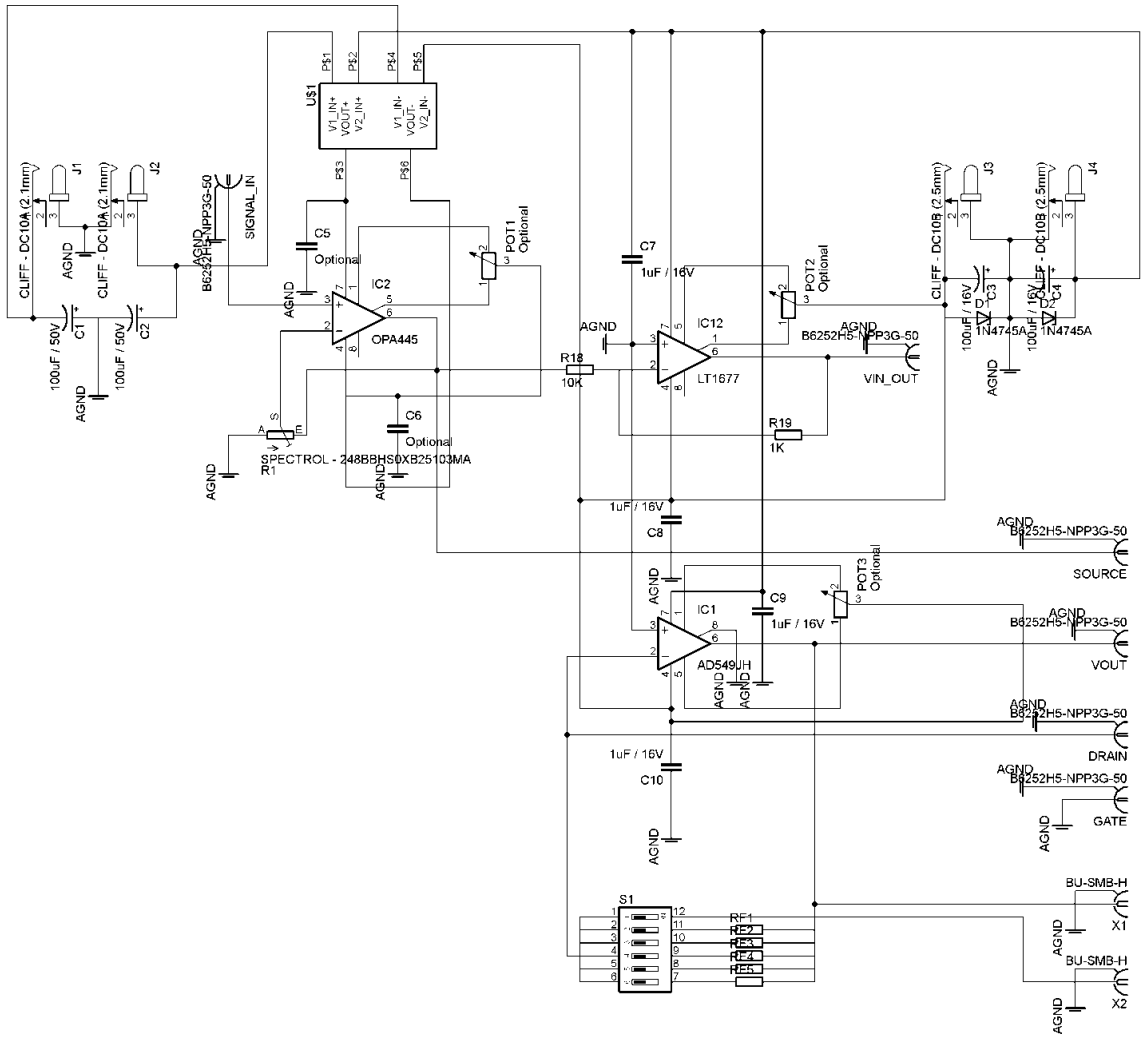

Fig. 1 – The circuit schematic of the last (MK5) version of the I-V converter system including fixed-value feedback resistors

Appendix II.1.2. PCB layout overview

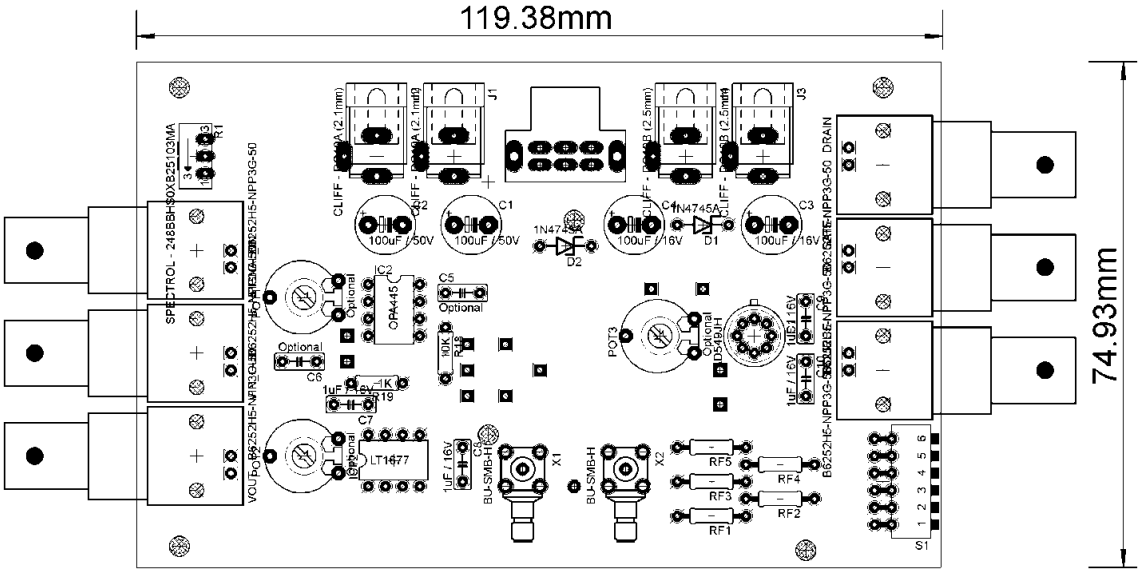

Fig. 2 – Overview of the layout of the PCB in the last version (MK5) I-V converter. Top and Bottom layers are not shown.

Fig. 3 – A photograph of the top side of the prototype PCB.

Appendix II.2. Gas exposure system: OFET probing board (four OFET mask)

Appendix II.2.1. Schematic

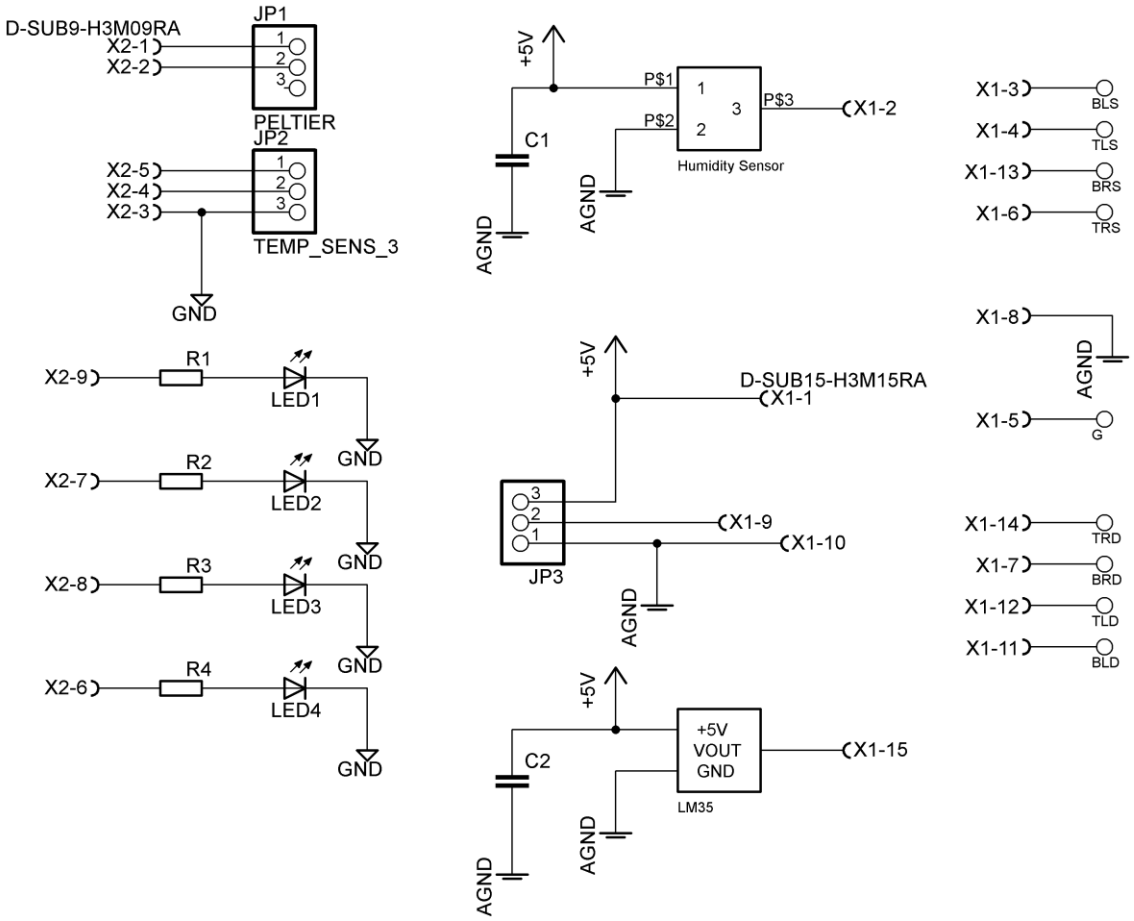

Fig. 4 – The circuit schematic of the OFET probing board for the 4-DUT mask

Appendix II.2.2. PCB layout overview

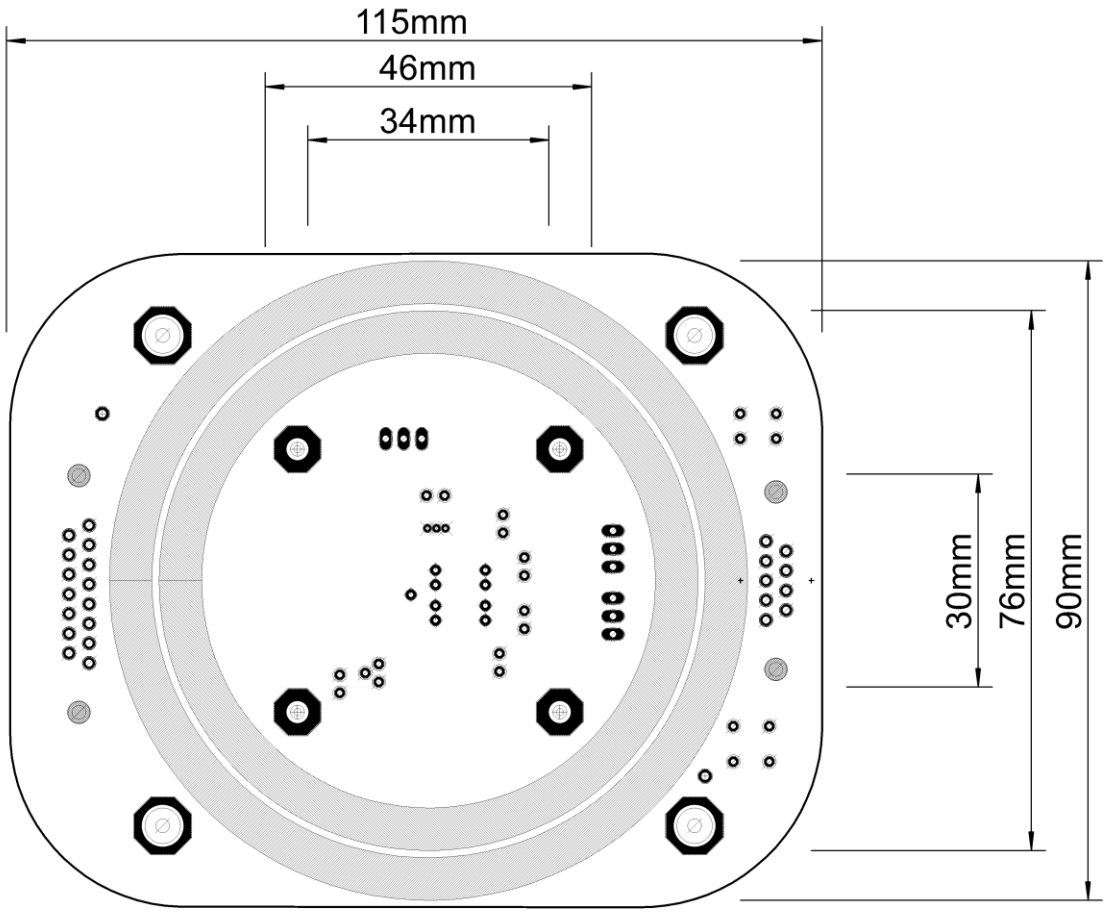

Fig. 5 – The PCB layout of the OFET probing board for the 4-DUT mask

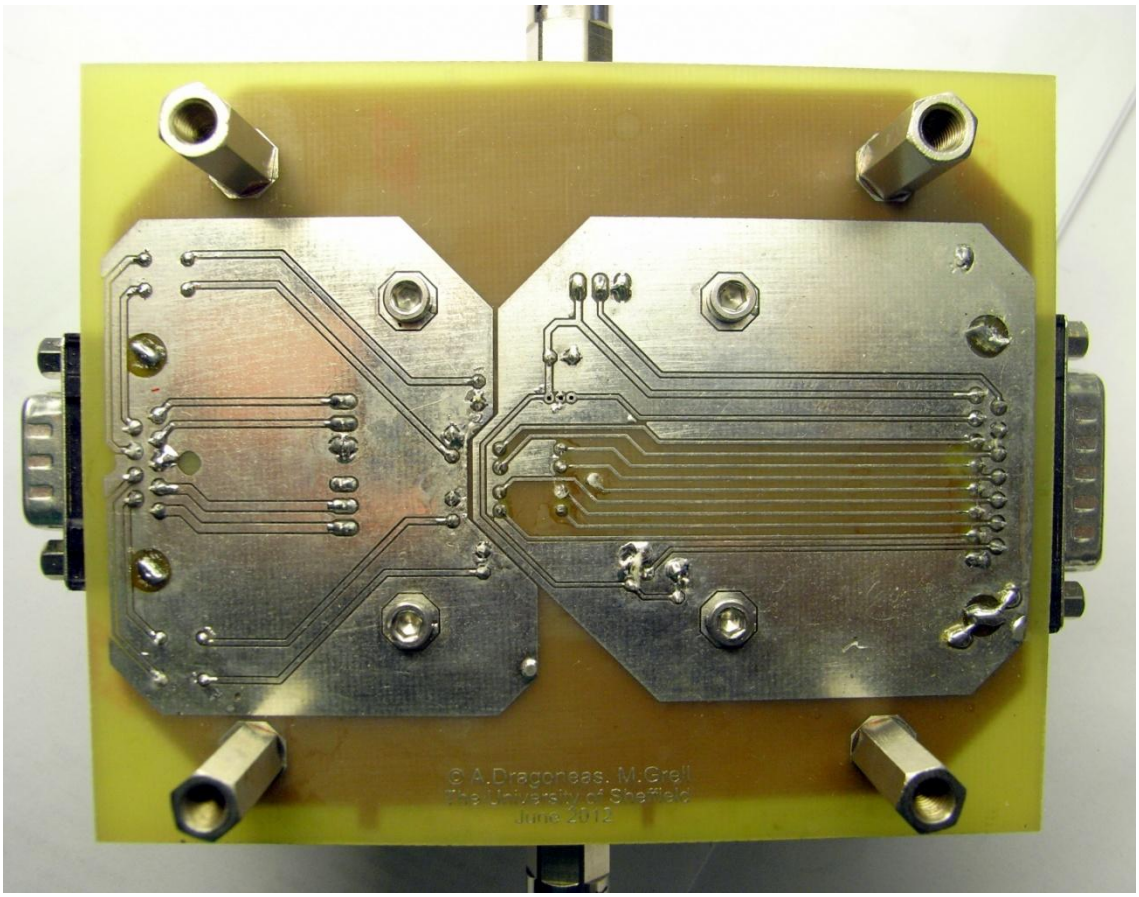

Fig. 6 – A photograph of the bottom side of the OFET probing board for the 4-DUT mask

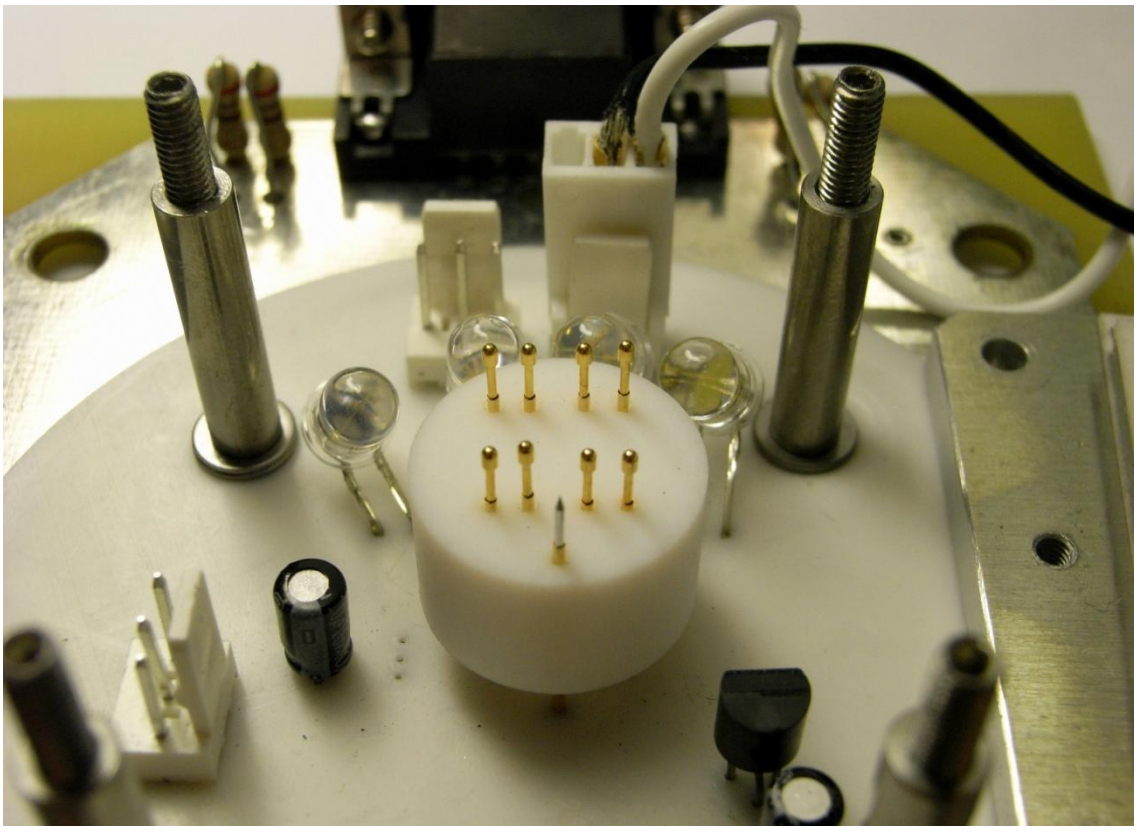

Fig. 7 – A photograph of the top side of the OFET probing board for the 4-DUT mask

Appendix II.3. Gas exposure system: OFET contacting board (twenty OFET mask)

Appendix II.3.1. Schematic

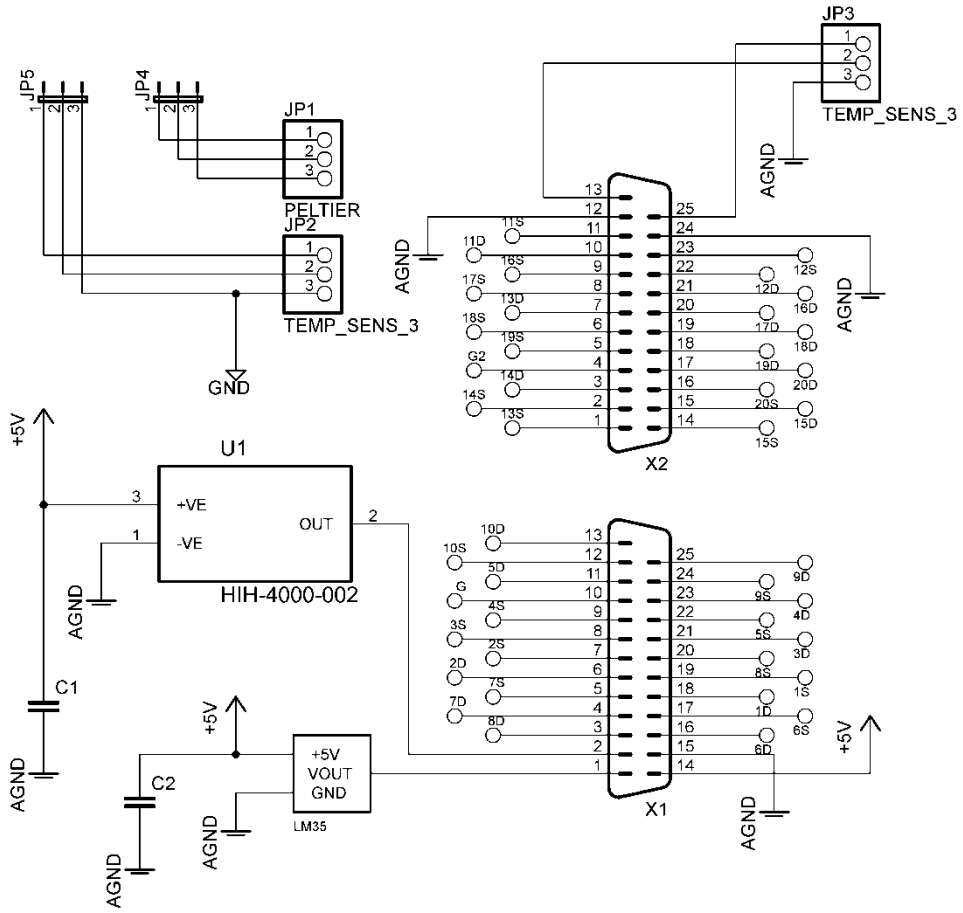

Fig. 8 – The circuit schematic of the OFET contacting board for the 20-DUT mask

Appendix II.3.2. PCB layout overview

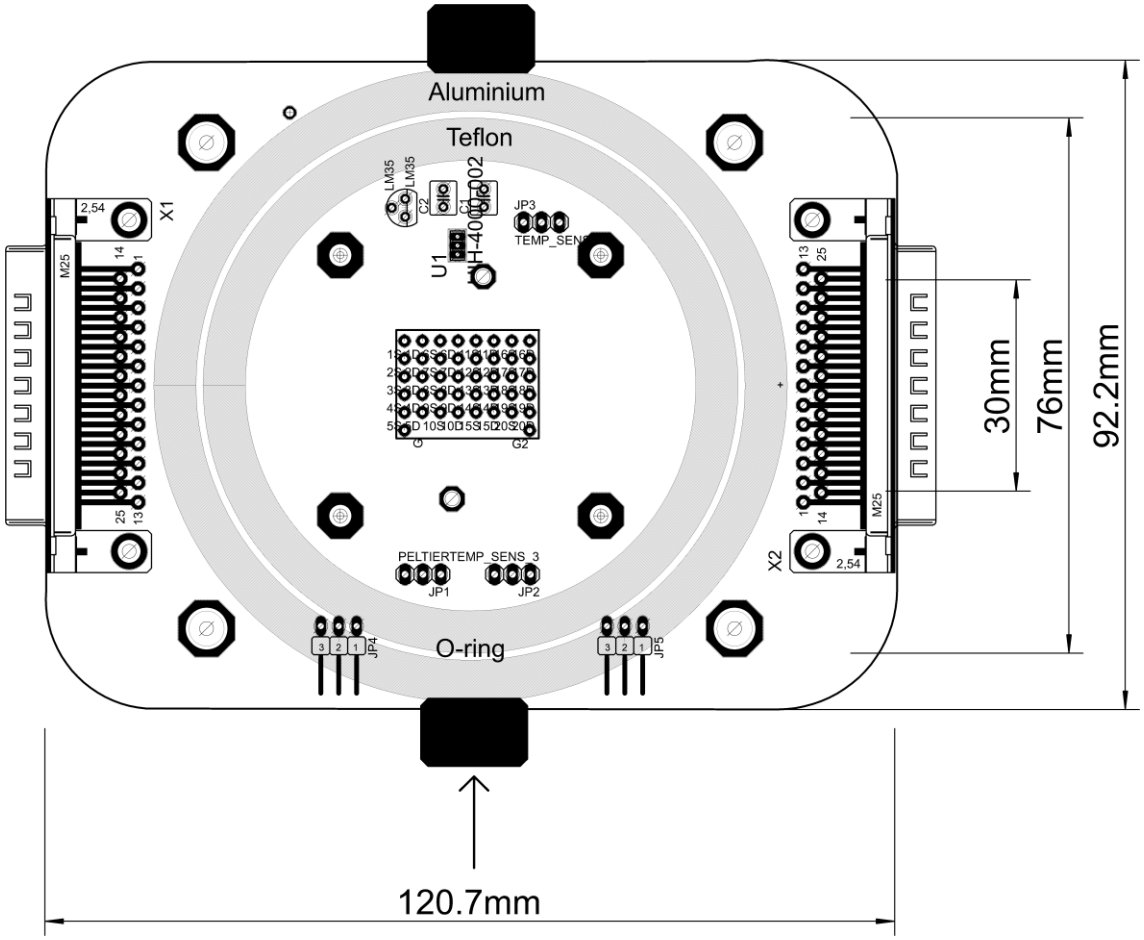

Fig. 9 – The PCB layout of the OFET contacting board for the 20-DUT mask

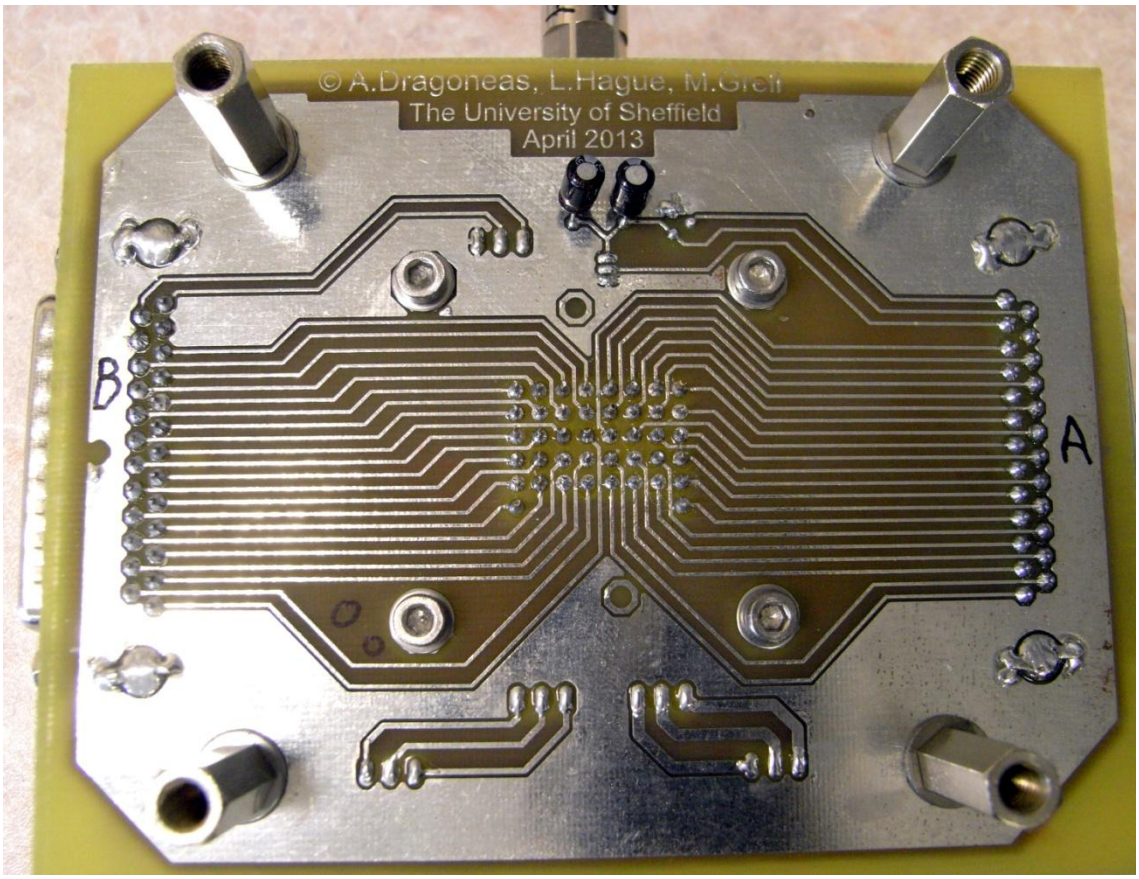

Fig. 10 – A photograph of the bottom side of the OFET contacting board for the 20-DUT mask

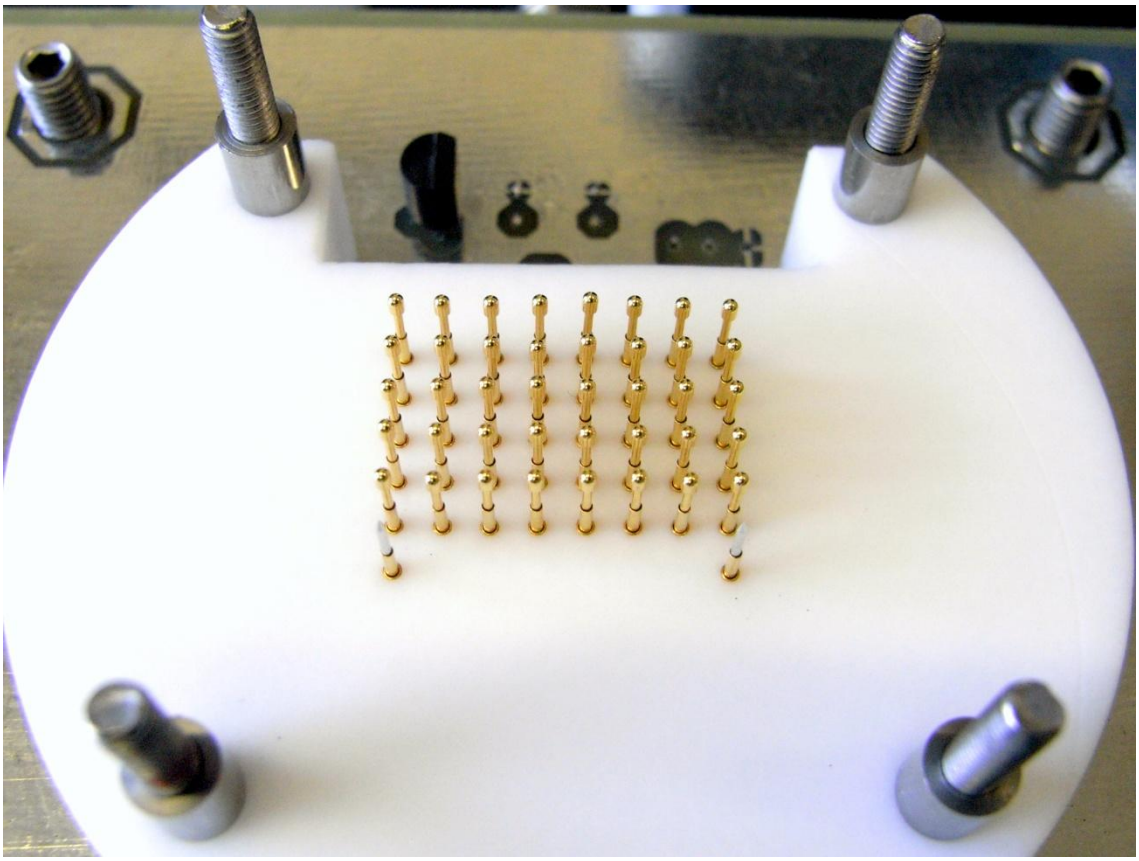

Fig. 11 – A photograph of the bottom side of the OFET contacting board for the 20-DUT mask

Appendix II.4. Gas exposure system: Multiplexing and signal distribution board (manual four OFET system)

Appendix II.4.1. Schematic

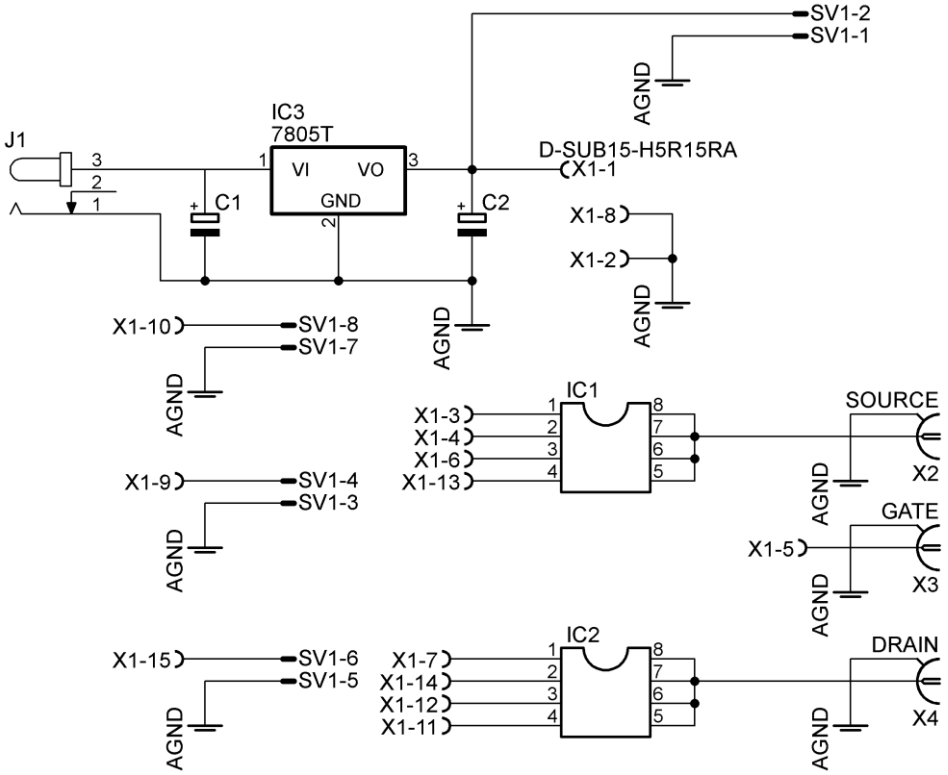

Fig. 12 – The circuit schematic of the manual multiplexing and signal distribution board designed for the 4-DUT mask

Appendix II.4.2. PCB layout

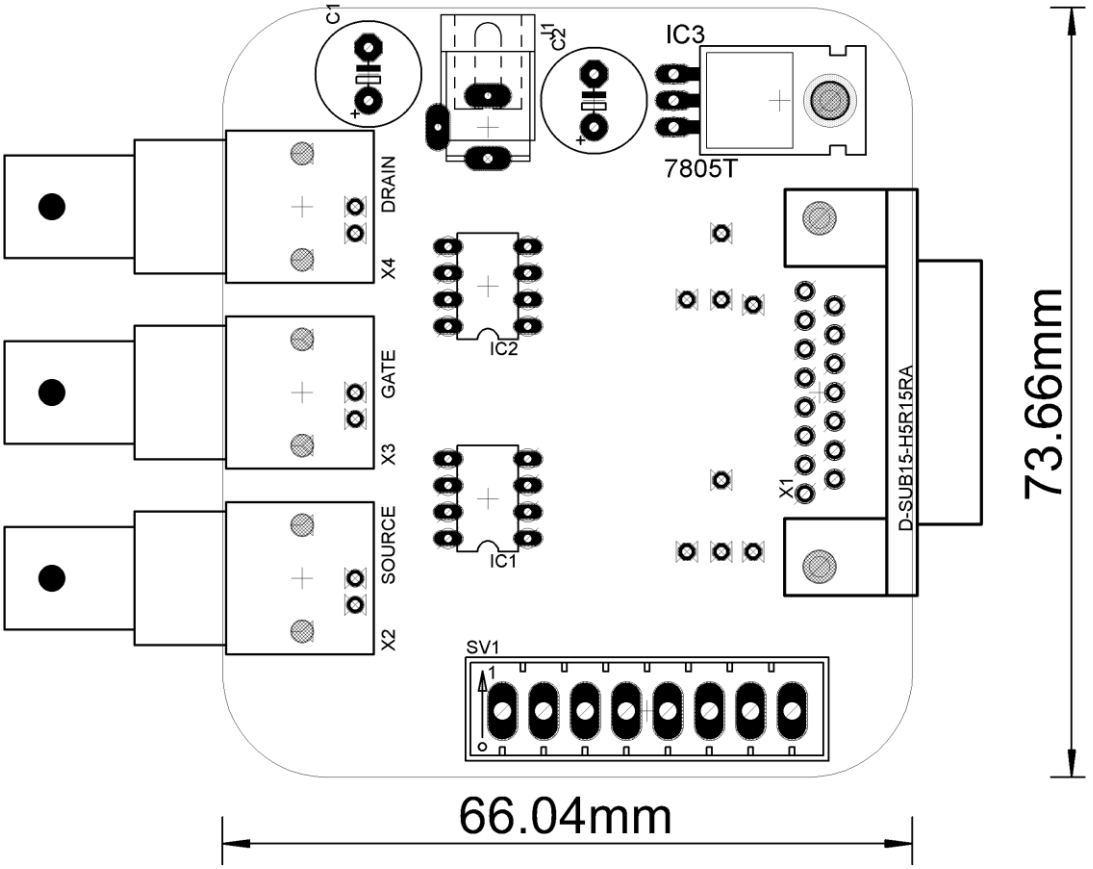

Fig. 13 – The PCB layout of the manual multiplexing and signal distribution board designed for the 4-DUT mask

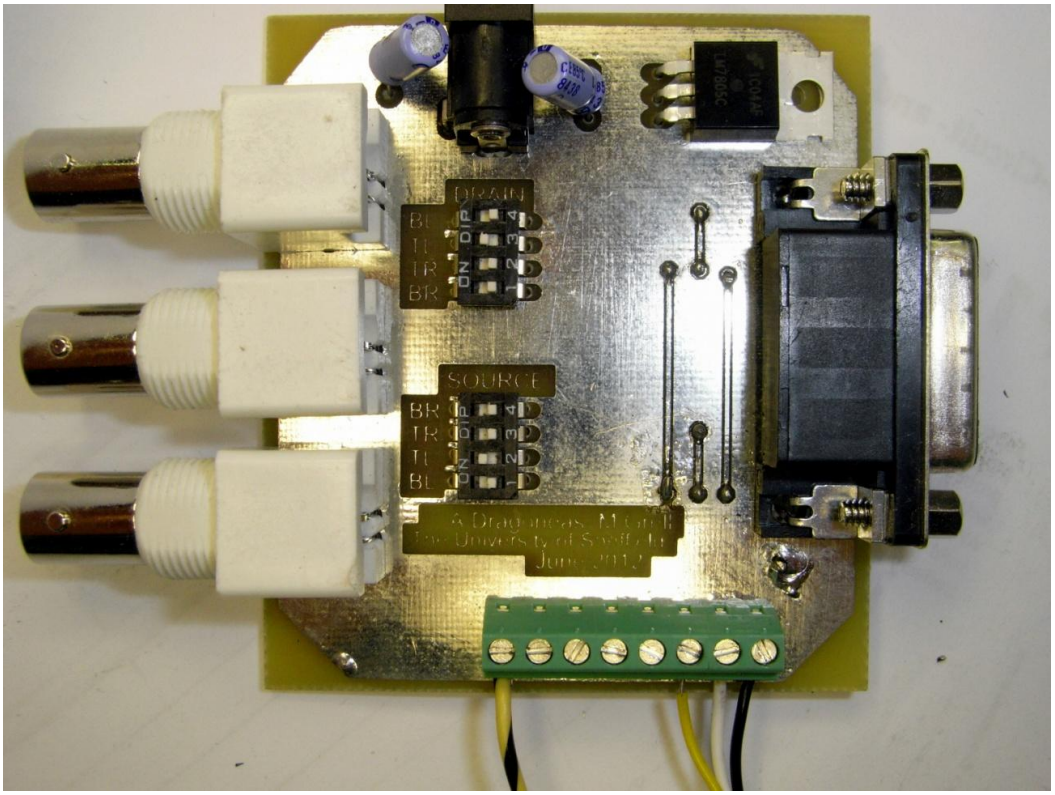

Fig. 14 – A photograph of the top side of the manual multiplexing and signal distribution board designed for the 4-DUT mask

Appendix II.5. Gas exposure system: Multiplexing and signal distribution board (relay-based four OFET system)

Appendix II.5.1. Schematic

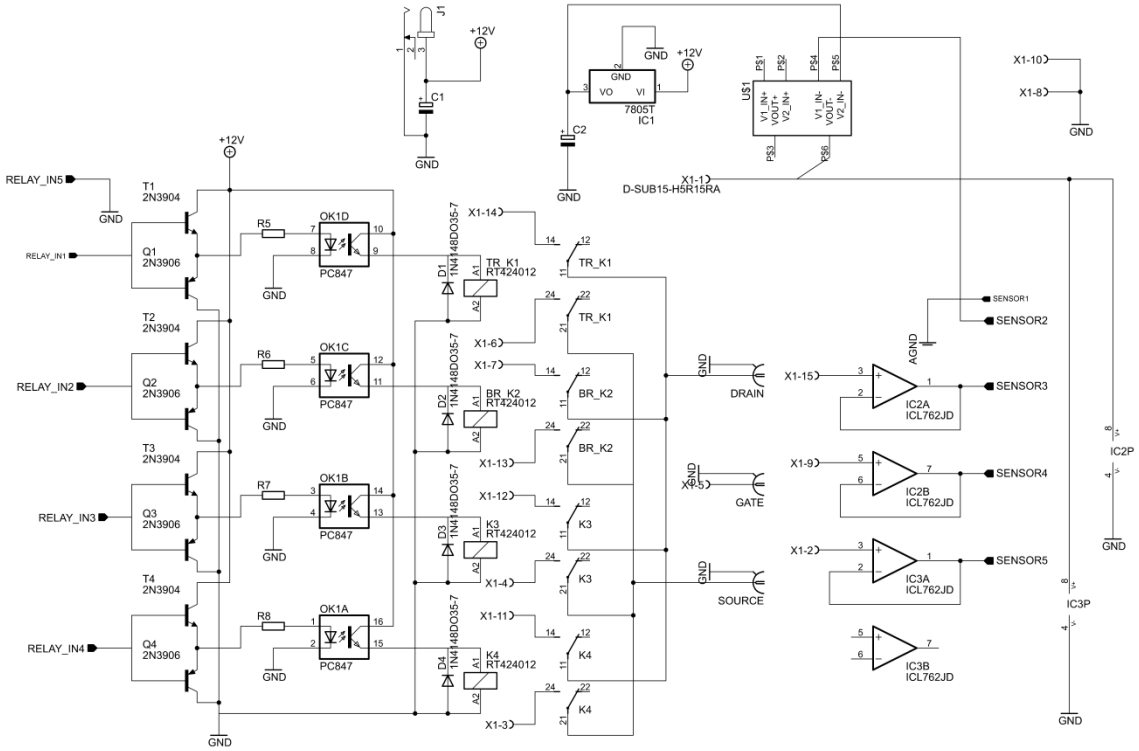

Fig. 15 – The circuit schematic of the relay-based multiplexing and signal distribution board designed for the 4-DUT mask

Appendix II.5.2. PCB layout overview

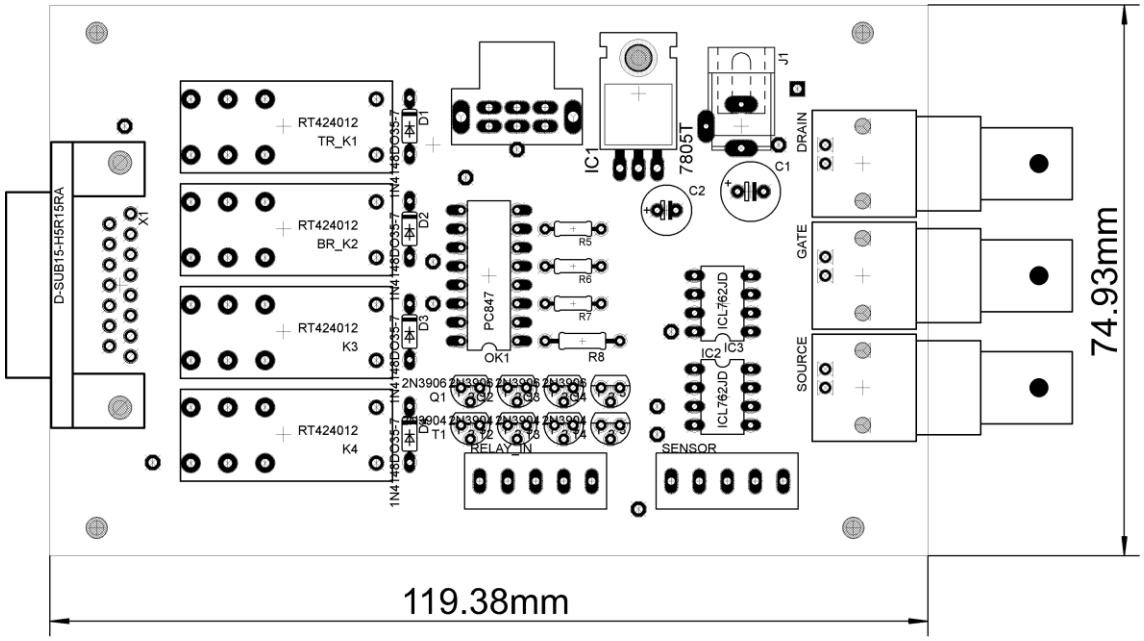

Fig. 16 – The PCB layout of the relay-based multiplexing and signal distribution board designed for the 4-DUT mask

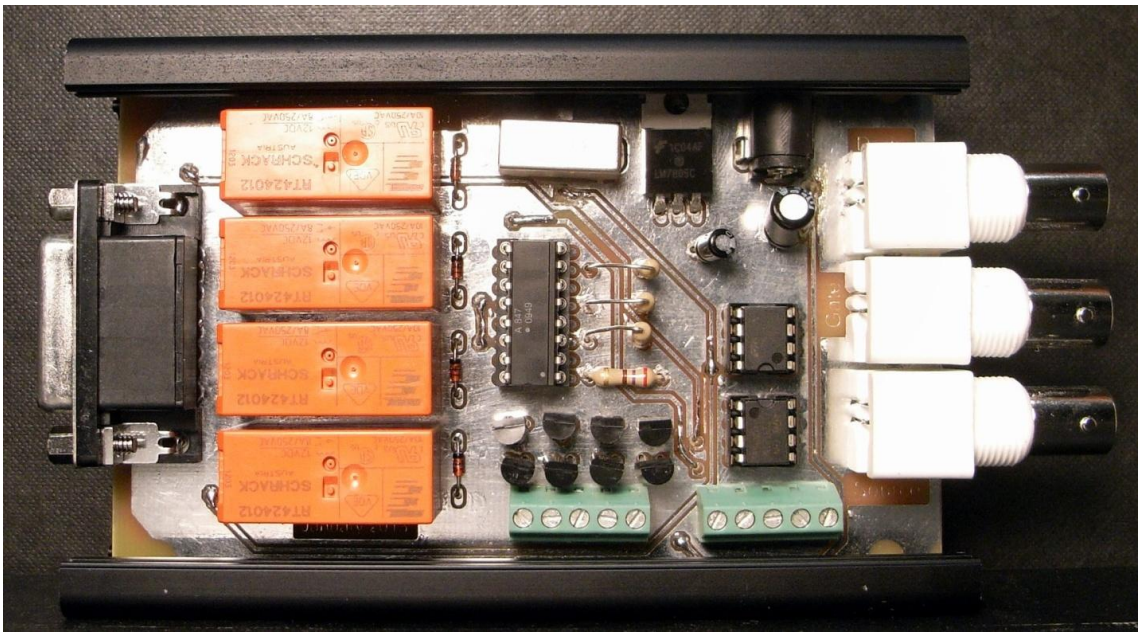

Fig. 17 – A photograph of the top side of the relay-based multiplexing and signal distribution board designed for the 4-DUT mask

Appendix II.5.3. Pinout

	Automatic System		Manual System	
Pin #	**Wire colour**	**Signal**	**Wire colour**	**Signal**
1	white	5 VDC	white	5 VDC
2	white /black	Humidity	white/black	Humidity
3	white / brown	BLS	red/black	BLS
4	white / red	TLS	red/white	TLS
5	white / orange	GATE	orange/black	GATE
6	white / yellow	TRS	green/white	TRS
7	red	BRD	red	BRD
8	orange	GND	orange	GND
9	grey	Temperature 2	blue/white	Temperature 2
10	purple	GND	black/white	Temperature 3
11	blue	BLD	blue	BLD
12	brown	TLD	blue/black	TLD
13	black	BRS	black	BRS
14	green	TRD	green	TRD
15	yellow	Temperature 1	green/black	Temperature 1

Appendix II.6. Gas exposure system: Multiplexing and signal distribution board (twenty OFET system)

Appendix II.6.1. Schematic

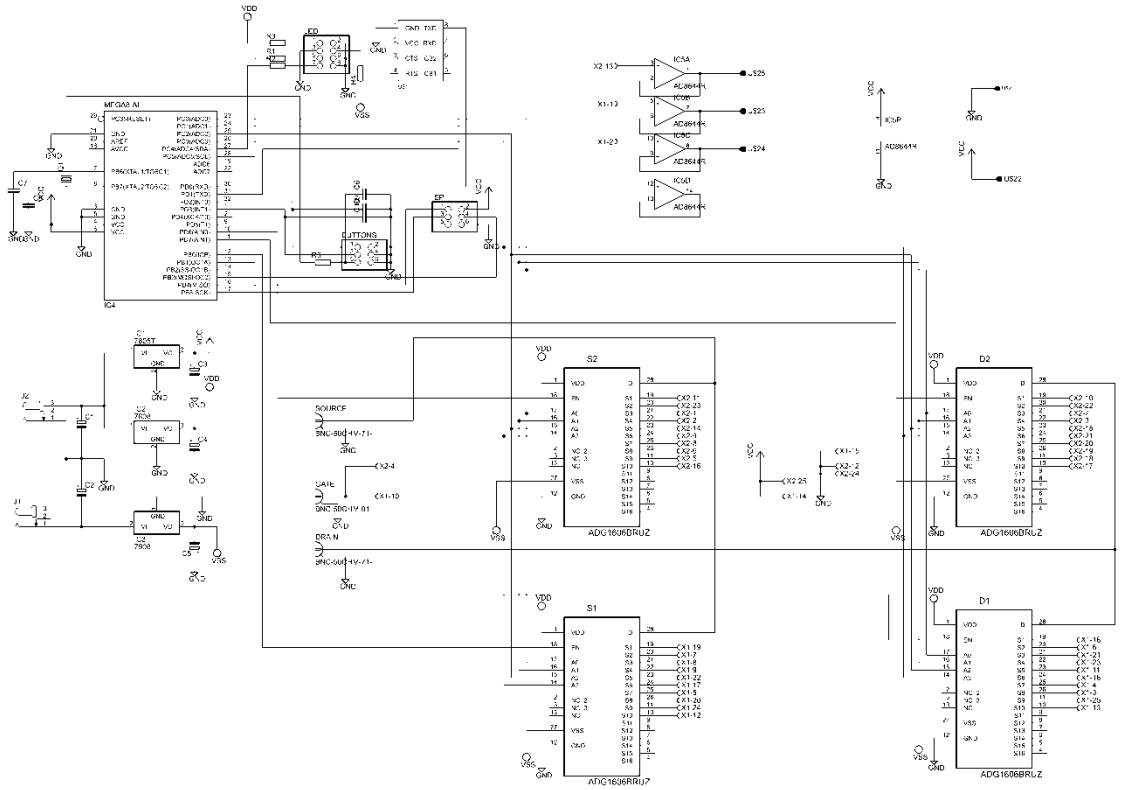

Fig. 18 – The circuit schematic of the solid-state, microcontroller-based multiplexing and signal distribution board designed for the 20-DUT mask.

Appendix II.6.2. PCB layout

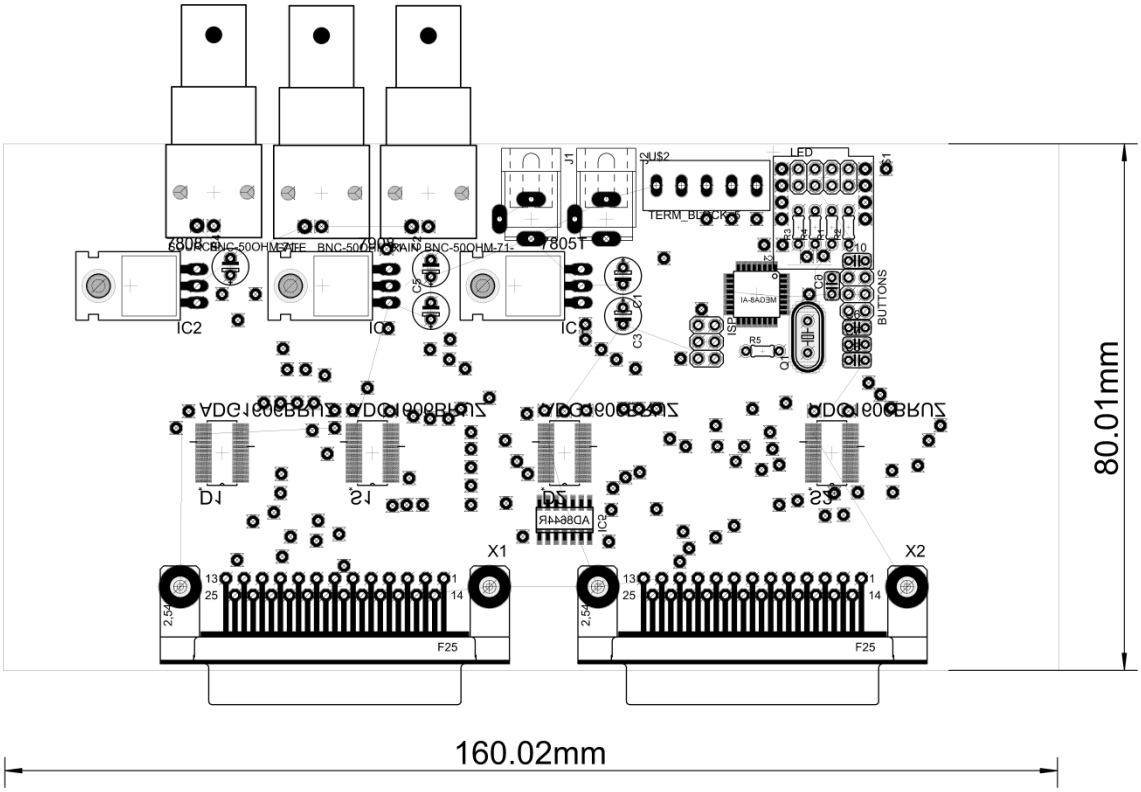

Fig. 19 – The PCB layout of the solid-state, microcontroller-based multiplexing and signal distribution board designed for the 20-DUT mask.

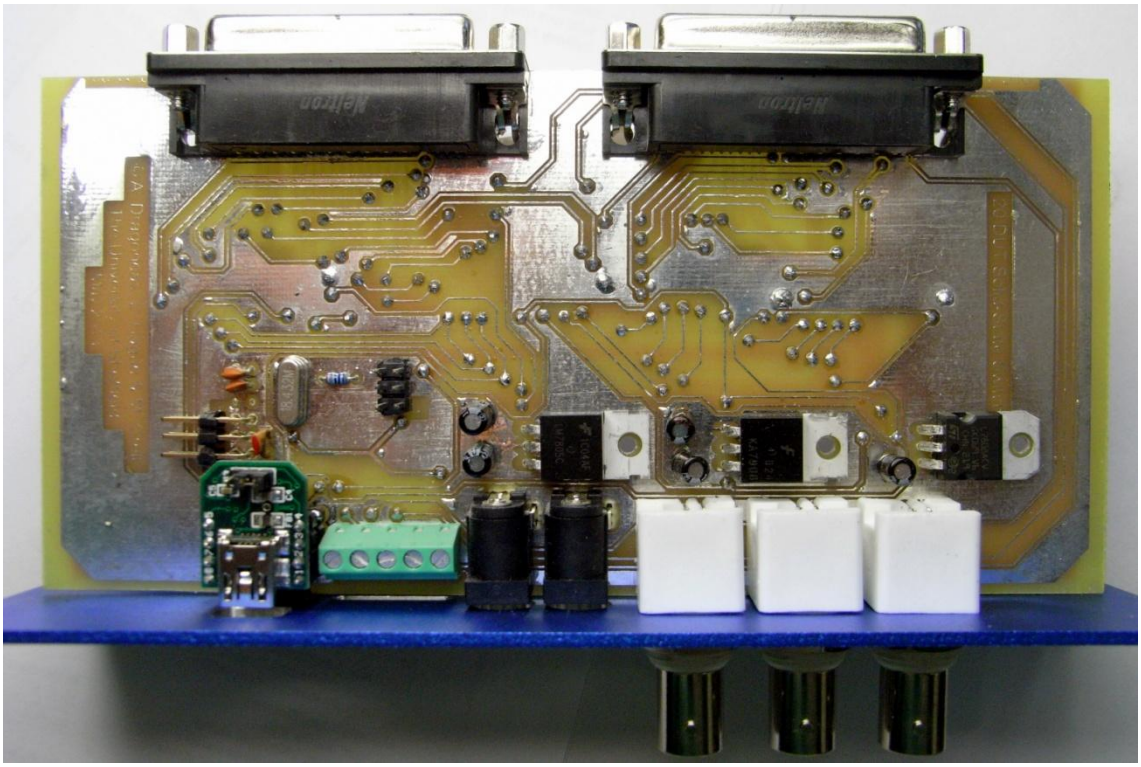

Fig. 20 – A photograph of the top-side of the solid-state, microcontroller-based multiplexing and signal distribution board designed for the 20-DUT mask.

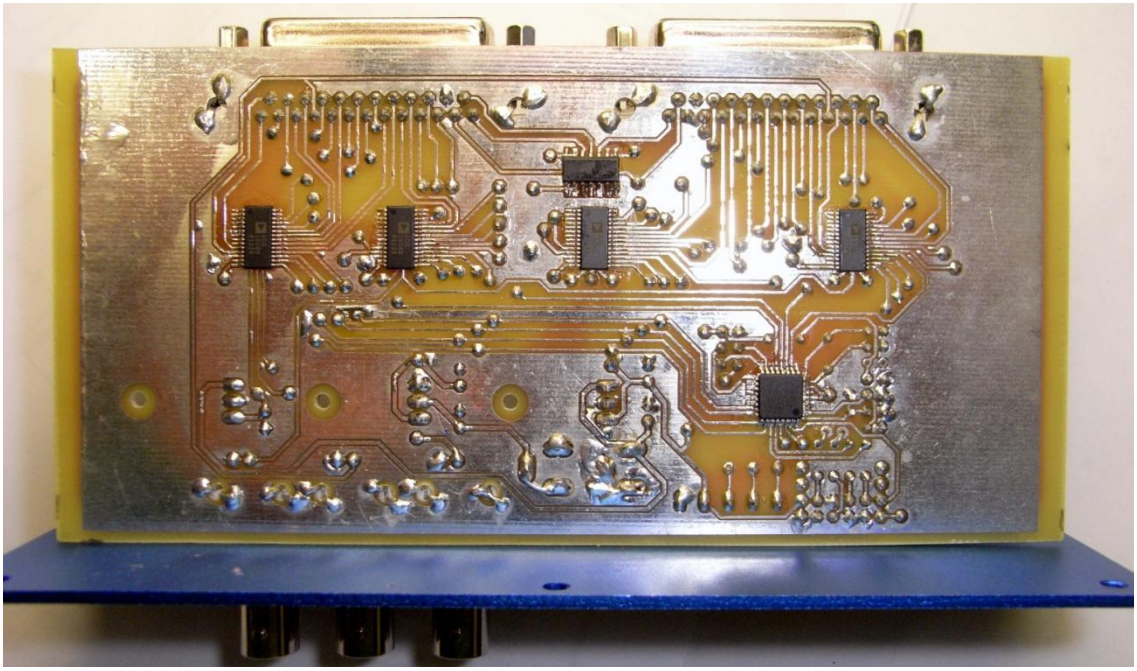

Fig. 21 – A photograph of the bottom side of the solid-state, microcontroller-based multiplexing and signal distribution board designed for the 20-DUT mask.

Fig. 22 – A photograph of the front side of the solid-state, microcontroller-based multiplexing and signal distribution board designed for the 20-DUT mask.

Fig. 23 – A photograph of the rear side of the solid-state, microcontroller-based multiplexing and signal distribution board designed for the 20-DUT mask.

Appendix II.6.3. Pinout and remote commands

Socket	Pin	Design DUT	Actual DUT	Pin	Design DUT	Actual DUT	PC Command
A	19	S1	S16	18	D1	D16	A
A	7	S2	S17	6	D2	D17	B
A	8	S3	S18	21	D3	D18	C
A	9	S4	S19	23	D4	D19	D
A	22	S5	S20	11	D5	D20	E
A	17	S6	S11	16	D6	D11	F
A	5	S7	S12	4	D7	D12	G
A	20	S8	S13	3	D8	D13	H
A	24	S9	S14	25	D9	D14	I
A	12	S10	S15	13	D10	D15	J
B	11	S11	S6	10	D11	D6	K
B	23	S12	S7	22	D12	D7	L
B	1	S13	S8	7	D13	D8	M
B	2	S14	S9	3	D14	D9	N
B	14	S15	S10	15	D15	D10	O
B	9	S16	S1	21	D16	D1	P
B	8	S17	S2	20	D17	D2	Q
B	6	S18	S3	19	D18	D3	R
B	5	S19	S4	18	D19	D4	S
B	16	S20	S5	17	D20	D5	T
					ALL DISCONNECTED		X

Appendix II.7. Gas exposure system: Solenoid valve and mass-flow controller driving board

Appendix II.7.1. Schematic

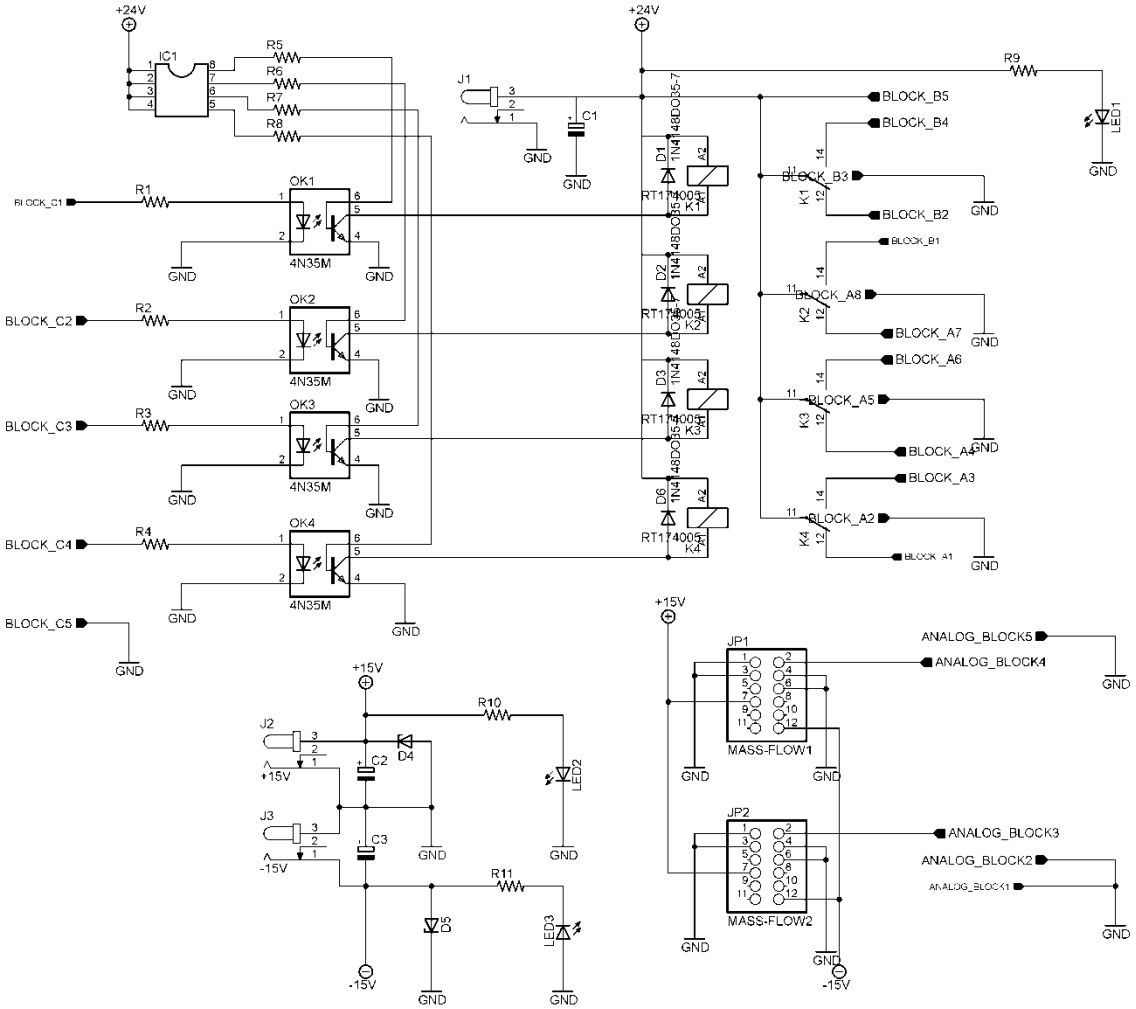

Fig. 24 – The circuit schematic of the solenoid valve and mass-flow controller driving board

Appendix II.7.2. PCB layout

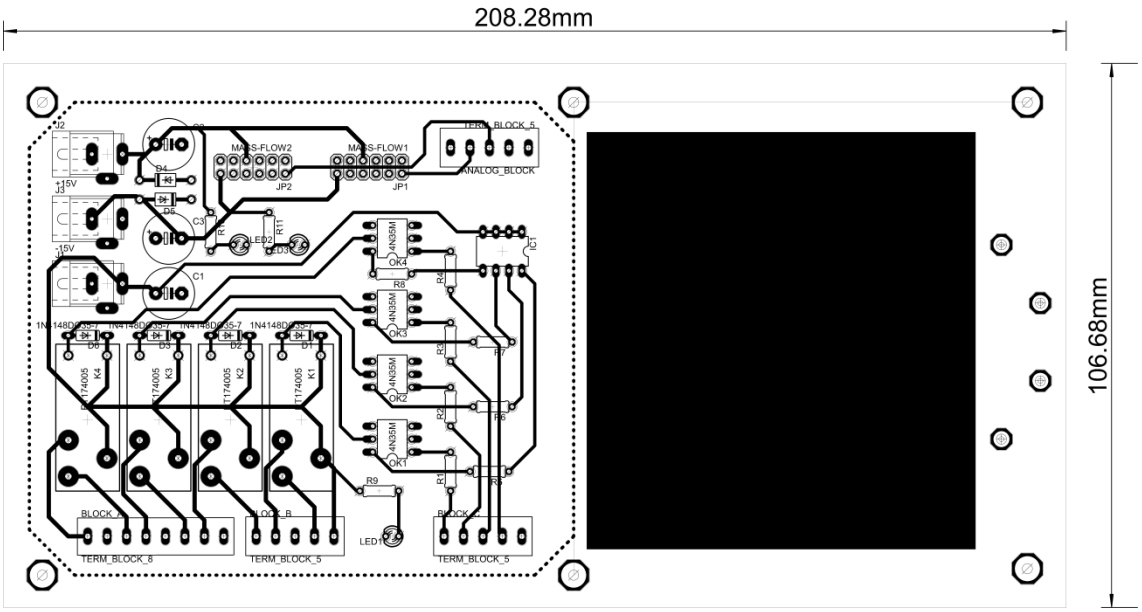

Fig. 25 – The PCB layout of the solenoid valve and mass-flow controller driving board

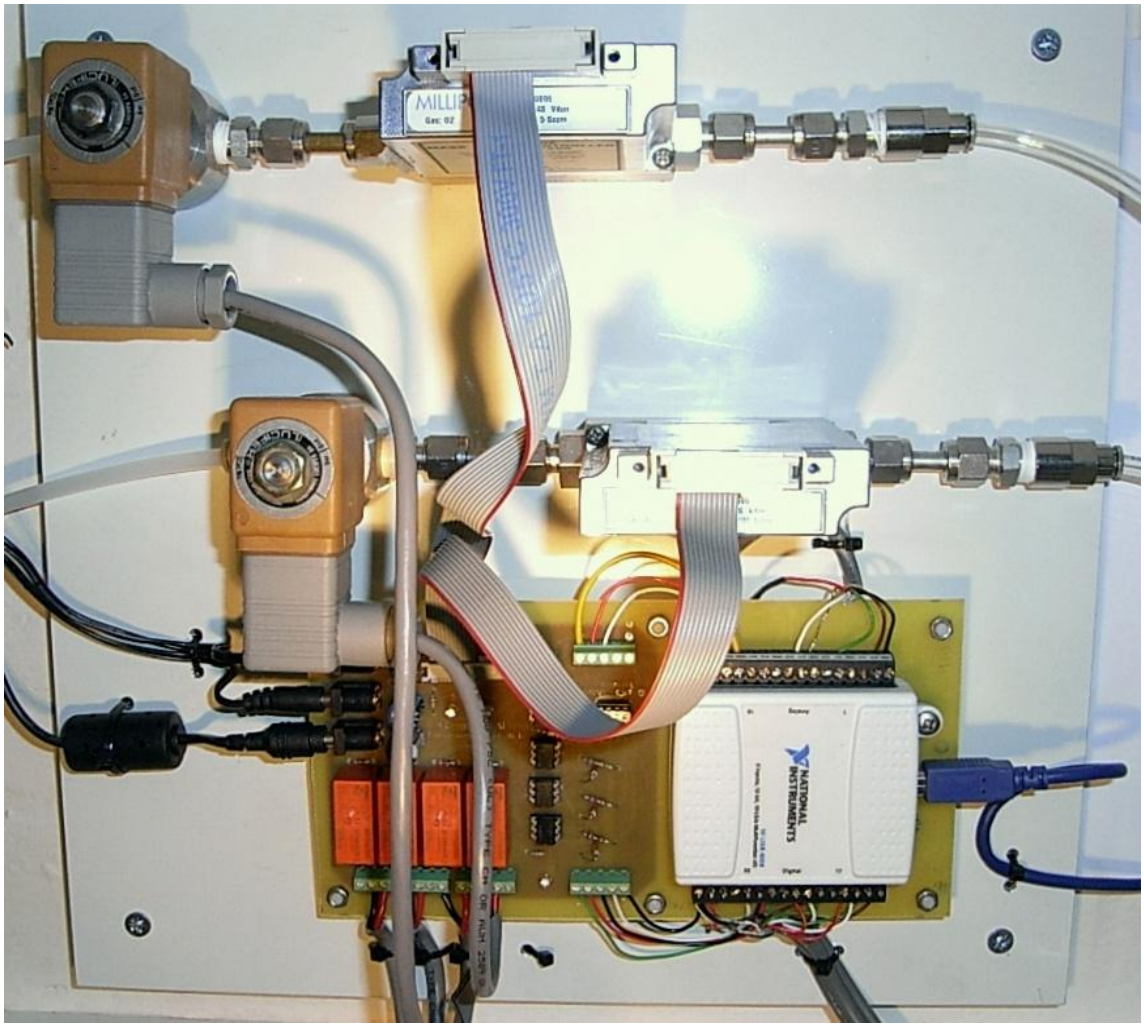

Fig. 26 – A photograph of the solenoid valve and mass-flow controller driving board including the NI USB-6008 unit. The board is connected to two Tylan FC-260 mass-flow controllers and two 24 V DC solenoid valves.

Appendix II.8. Handheld automatic OFET characterisation embedded system

Appendix II.8.1. Schematic

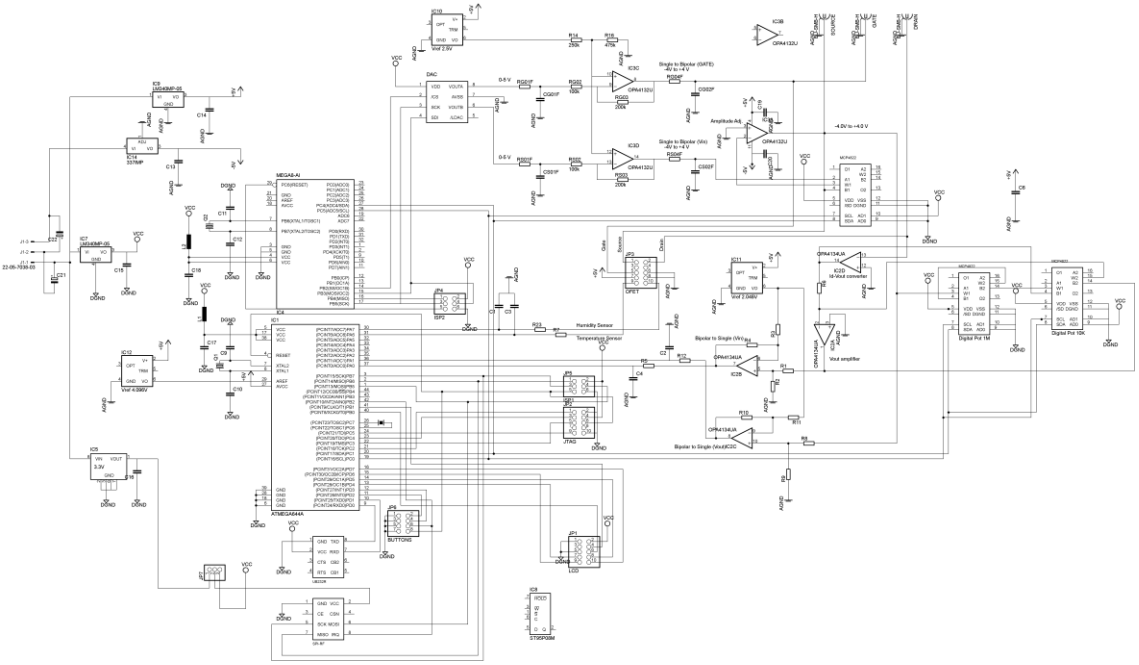

Fig. 27 – The circuit schematic of the handheld automatic OFET characterisation embedded system

Appendix II.8.2. Prototype

Fig. 28 – A photograph of one of the prototypes of the handheld automatic OFET characterisation embedded system. In this photograph, a dummy resistor is being used in the place of an OFET, as seen in the blue IC socket.

Abbreviations, acronyms and symbols

Abbreviation	Meaning
ADC	Analogue-to-Digital Converter
C_i	Capacitance per unit area
DAC	Digital-to-Analogue Converter
DIP	Dual In-line Package
DUT	Device Under Test
EMI	ElectroMagnetic Interference
FET	Field-Effect Transistor
FET	Field-Effect Transistor
IC	Integrated Circuit
I_{off}	Off-state drain current
I_{on}	Saturated drain current (on-state current)
IVC	Current-to-Voltage Converter
L	Channel Length
LCD	Liquid Crystal Display
LDPE	Low-Density Poly(Ethylene)
LED	Light-Emitting Diode
LHS	Left-Hand-Side
LoD	Limit of Detection
MCU	Microcontroller Unit
NW	NanoWire
OFET	Organic Field-Effect Transistor
OLED	Organic Light-Emitting Diode
OLET	Organic Light-Emitting Transistor
op-amp	Operational amplifier
OSC	Organic Semiconductor
OTFT	Organic Thin-Film Transistor
OTS	OctadecylTrichloroSilane
P3HT	Poly(3-HexylThiophene)
PCB	Printed-Circuit Board
ppm	parts per million
PTFE	Poly(TetraFluoroEthylene)
RH	Relative Humidity
RHS	Right-Hand-Side
RISC	Reduced Instruction Set Computing
RT	Room temperature
SAM	Self-Assembled Monolayer
SMD	Surface Mount Device
TFT	Thin-Film Transistor
UV	Ultraviolet (light, radiation)
V_{th}	Threshold Voltage
W	Channel Width
μ	Charge carrier mobility

Acknowledgements

Frankly speaking, I need another 235 pages to describe how lucky and grateful I feel for having the good fortune to have such people around me. I am summarising my gratitude in one page.

First and foremost, I would like to thank my superb supervisor, Martin Grell for giving me this unique opportunity, always being available for a chat, trusting me and letting me take the initiative, while guiding me and calming me down whenever needed. Nothing would have been achieved without Martin and I will always be grateful for everything he has done for me over the course of the last 38 months.

Next, many thanks to the great colleagues I shared my life in Hicks building with. Some special thanks to three people: First, Lee Hague for his endless eagerness to help and his passion for sharing his knowledge and experience; it was a great pleasure to work together and I really owe him a lot. Second, Delia Puzzovio, for sharing her FlexSMELL experience with me and for her excellent support, help and understanding. Third, Nikos Christogiannis for the hundreds of cups of coffee and the uncountable hours of chat we had, for sharing his optoelectronics knowledge with me and getting on my nerves whenever I felt bored.

Also, thanks to: a. Simon Dixon, for his excellent technical support and his smile every time I showed up at the mechanical workshop's threshold, b. Adam Hobson for taking the majority of the AFM images shown in this thesis, as well as for dealing with Lee's chatter, c. Stuart Brittle and Fredo Flores for being great coffee- and lunch-mates, d. Abdullah, Hadi, Krisna, Saud and Talal for joyfully sharing D44 and the labs with me on a daily basis, e. Mark Hampton from the research group of J. Emyr Macdonald in Cardiff University for his flawless collaboration in our joint research work on organic nanowire devices, and f. Christina Skoulikidou from Demokritos, for her persistence in dealing with the SEM imaging of my OFETs.

From my secondment in the University of Bari, many thanks to Kiki Manoli, Liviu Dumitru, Yusuf Mulla and Daniela Angione from the research group of Luisa Torsi for their excellent hospitality and precious help, from our common research work in the lab to our daily life in Bari.

From my life in Sheffield, big thanks to (literally) all my friends who contributed to this work by helping me keep a balance in my life. Special thanks to Nikos Nikogeorgos and Sir Panos Papastergiou for their massive help, hospitality and super cooking skills. Also, many thanks to my good old friends, Panos and Alexandra whose revitalising communication, jokes, visits and hospitality brought a smile to my face during difficult periods.

Of course, thanks to all five magnificent members of my family for always being there and supporting me even not knowing exactly what I have been doing in Sheffield for all this time.

Last but not least at all, it is needless to say that this last bit of my thesis would have never been written without the love, support and care of my partner, Severina. Thanks for making this journey with me, being by my side no matter the distance and doing everything possible to help me and cheer me up every day.

My best wishes to all of you. –