Integrated PV and Multilevel Converter System for Maximum Power Generation under Partial Shading Conditions

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The candidate confirms that the work submitted is his/her own, except where work which has formed part of jointly-authored publications has been included. The contribution of the candidate and the other authors to this work has been explicitly indicated below. The candidate confirms that appropriate credit has been given within the thesis where reference has been made to the work of others.

Publications:

- I. Abdalla, J. Corda, L. Zhang, "Multilevel DC-Link Inverter and Control Algorithm to Overcome the PV Partial Shading," IEEE Transactions on Power Electronics, vol.28, no.1, pp.14-18, 2013.
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Some sections in chapters 3,4,5,7 are based on publications stated above. All the work contained within the publications is directly attributable to the candidate, under the supervision of Dr. L. Zhang and Dr. J. Corda.

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Abstract

The emerging trend towards the harnessing of the electrical power from solar energy has increased the research effort in power electronics applications. To achieve the required voltage level, a number of photovoltaic PV sources (cells/modules) are connected in series. The major challenge here is to deal with the partial shading problem, where the series connected PV sources are exposed to different insolation. The generated current is limited by the current of the shaded PV sources unless those sources are bypassed by diodes, in which case the total DC voltage is reduced and the shaded sources do not contribute to the generated output power. A power electronics approach can be employed to overcome the problem, by enabling both shaded and non-shaded sources to generate their maximum power, thereby and delivering the total generated power to the load. Thus no shaded PV source is bypassed or degrades the power extraction from the other PV sources.

This thesis investigates the PV partial shading problem of individual PV sources which are connected in series. After the review and evaluation of existing methods to overcome this problem, the thesis employs for the first time the multilevel DC-Link inverter to deal with the problem of partial shading by using a novel control algorithm called PV permutation algorithm. The thesis also develops a simplified generalized Integration PWM (IPWM) algorithm which can be used to control higher level inverters. An improved maximum power point algorithm "voltage-hold perturbation and observation (VH-P&O)", which overcomes the major tracking limitations, is developed from the basic P&O algorithm.

Experimental systems of five and seven level DC-link inverters with a DC-DC buck converter system have been implemented. The digital processing unit eZdsp^{TM} F28335 is used to control the PV systems in real time, and Matlab-Simulink Real Time Data Exchange (RTDX) is employed to display the extracted power and to control the system parameters via a designed Graphical User Interface (GUI) window. The simulation and experimental results showed that the series connected PV sources operate at their maximum power points under partial shading conditions without affecting each other.

Table of Contents

List of Tables ix

List of Figures x

Abbreviations xix

Symbols xxi

1 Introduction and Problem Definition 1

1.1 PV fundamentals and cell modelling 2

1.2 Hot-Spots and their Effects 5

1.3 PV Cell Reverse Mode and Shunt Resistance Effect 7

1.4 The Power Reduction 9

1.5 PV Bypass Diode Protection 13

1.6 Worst Case Condition and the Effect of Shaded Cells Number 17

1.7 Solar Cell with Integral Bypass Diode Function 23

1.8 Problems and Challenges 25

1.9 Thesis Aim and Objectives 26

1.10 Structure of the Thesis 27

1.11 Summary 28

2 PV Partial Shading - the Existing Solutions 29

2.1 PV Configuration 29

2.2 PV Switching-Matrix Reconfiguration System 30

2.3 Single PV-Cell DC-DC Converter Module 32

2.4 Series Connected PV DC/DC Converter Modular System 33

2.5 General Control Circuit (GCC) PV system 34

2.5.1 GCC DC/DC Converter PV system 35

2.5.2 GCC Multi-Chopper PV system 37

2.6 Retrofit PV System 43
2.7 PV Multilevel Inverter System 45
2.7.1 PV Multilevel Inverter Topologies 45
2.7.2 PV Multilevel Inverter to Overcome Partial Shading 48
2.8 Summary 49

3 Multilevel DC-Link Inverter System and PWM Switching Techniques 50
3.1 The Proposed PV System 50
3.1.1 Control Principles of PV Multilevel DC-link Inverter System 53
3.2 Multilevel Inverter Switching Techniques 55
3.2.1 Space-Vector PWM (SVPWM) 56
3.2.1.1 Two-Level Based Multilevel SVPWM 61
3.2.2 Generalized Direct Multilevel PWM 64
3.2.3 Integration-Duty Cycle Conversion PWM (IPWM) 64
3.3 Multilevel PWM Simulation Results 67
3.3.1 Generalized Direct PWM Results 68
3.3.2 Generalized Two-level Based SVPWM Results 71
3.3.3 IPWM Results 71
3.4 PWM Control of the DC-link Inverter 74
3.5 Summary 76

4 Maximum Power Point Tracking Techniques 77
4.1 Basic Principle and the Simplest MPPT Scheme 78
4.2 P&O MPPT Algorithm 81
4.3 IncCond MPPT Algorithm 82
4.4 Hill-Climbing MPPT Algorithm 85
4.5 The Voltage-Hold P&O (VH-P&O) MPPT Algorithm 88
4.6 MPPT Simulation and Comparison 90
4.6.1 P&O MPPT Simulation Results 91

4.6.2 Simulation of VH-P&O MPPT and Comparison with the other Algorithms 98

4.7 Summary 103

5 Multilevel DC-Link Inverter to Overcome the PV Partial Shading 104

5.1 State Space Averaging (SSA) Module 104

5.1.1 SSA Module with R Load 104

5.1.2 SSA Module with R-L Load 109

5.1.3 SSA Module with Grid-Connected 111

5.2 PV Permutation Algorithm for Partial Shading Condition 117

5.2.1 Sequential Permutation of PV Sources 118

5.2.2 PV output generation 119

5.3 System Simulation under Partial Shading Conditions 127

5.3.1 Five-level DC-link Inverter under Partial Shading 128

5.3.2 Seven-level DC-link Inverter under Partial Shading 131

5.3.3 Nine-level DC-link Inverter under Partial Shading 132

5.3.4 Eleven-level DC-link Inverter under Partial Shading 133

5.3.5 Dynamic Conditions of the Applied Partial Shading 134

5.4 Summary 136

6 Experimental Implementation 137

6.1 PV Source 137

6.2 Lighting Source 138

6.3 Circuit for Emulation of the PV I-V Characteristic 141

6.4 DC-DC Buck Converter 142

6.4.1 MOSFET and Diode Specifications 142

6.4.2 Current Sensing Circuit 143

6.4.3 Voltage Sensing Circuit 144

6.4.4 MOSFET Driving Circuit 145

6.4.5 DC Power Supplies 146

6.5 DC-link Inverter 146

6.6 Converter Control 150

6.6.1 eZdsp^{TM} F28335 Card 150

6.6.2 Software Overview 150

6.6.2.1 Buck Converter Control Flowchart and ePWM Event Manager 151

6.6.2.2 DC-Link Inverter Control Flowchart and ePWM Event Manager 153

6.6.2.3 Simulink Target Support Package and Real-Time Workshop 155

6.6.2.4 Simulink Real-Time Data Exchange and Graphical User Interface 156

6.7 Summary 160

7 Experimental Results 162

7.1 Light Sources Test 162

7.2 PV Module Test 164

7.3 Buck converter MPPT Results 166

7.4 IPWM Applied for Five-Level DC-Link Inverter 167

7.5 IPWM Applied for Five-Level DC-Link Inverter 170

7.6 PV Permutation Algorithm for Seven-Level DC-Link Inverter 179

7.7 Improved PV Permutation Algorithm for Seven-Level DC-Link Inverter 189

7.8 Summary 192

8 Conclusions and Recommendations 194

8.1 Conclusions 194

8.2 Recommendations for Future Work 196

References 197

Appendix A Improved Output Generation from Three PV Sources 207

List of Tables

1.1 The Effects of the Hot-Spots 7

2.1 GCC Multi Shopper System Parameters 41
2.2 The GCC Results at D=0.38 and D=0.76 41

3.1 Five-level (DC-link) Inverter Switching States 51
3.2 Switch States for Two-level Three-phase Inverter 58
3.3 PWM Parameters 67

4.1 PV System Parameters (MPPT) 91

5.1 Five-level (DC-link) Inverter System Parameters 107
5.2 Seven-level Grid-connected (DC-link) Inverter System Parameters 116
5.3 Nine-level Grid-connected (DC-link) Inverter System Parameters 116
5.4 Output Generation from Two PV Sources 120
5.5 Output Generation from Three PV Sources 123
5.6 Improved Output Generation from Two PV Sources 125
5.7 System Parameters used in Simulation of PV Permutation Algorithm 127
5.8 THD and Fundamental Harmonic of Five-level Voltage by Using PV Permutation Algorithm and the Improved Algorithm 128

6.1 SSP-10W Module Specifications 138
6.2 Bulbs and Their Related Lumens Efficiency 140
6.3 STP24NF10 MOSFET Specifications 143

7.1 Buck Converter System Parameters 166
7.2 Five-Level Inverter System Parameters (IPWM) 168
7.3 Five-Level Inverter System Parameters (PV Permutation Algorithm) 171
7.4 THD and the Fundamental Amplitude of the Load Voltage at Various 191
7.5 Load Power at Various Partial Shading Levels 192

List of Figures

1.1	Silicon crystal lattice and intrinsic conductivity	2
1.2	PV cell semiconductor layers	3
1.3	PV equivalent circuit	4
1.4	Two PV cells/modules connected in series under partial shading	6
1.5	PV cell I-V curve (simulated at R_{sh}=200 Ω)	8
1.6	PV cell I-V curve depicted in 3D-graph as a function of the shunt resistance	9
1.7	18 PV cells connected in series to form a PV module (one shaded cell and 17 non-shaded PV cells)	10
1.8	PV cell I-V and power curves as a function of the irradiance level; the cell is connected in series with 17 non-shaded PV cells	11
1.9	I-V and power curves of 18 PV cells series connection as a function of one cell irradiance level	12
1.10	Two PV arrays with bypass diodes, one PV array is shaded	14
1.11	I-V and power curves of two PV arrays connected in series	15
1.12	I-V and power curves of four PV arrays connected in series	16
1.13	Two PV modules with bypass diodes, one PV cell is shaded	17
1.14	I-V curves of two series connected PV modules as a function of one shaded cell irradiance level	19
1.15	Power curves of two series connected PV modules as a function of one shaded cell irradiance level	20
1.16	I-V and power curves of two PV modules connected in series (one cell is shaded, the other cells are at 1000 W/m^2)	22
1.17	The effect of the shaded PV cell number on the dissipated power in two PV modules with bypass diodes	23
1.18	PV solar cell with discrete bypass diode and integrated bypass diode function	24
1.19	Modular, series and parallel PV configuration	25

2.1	SP, TCT and BL PV configuration	30
2.2	PV switching matrix-connected	31
2.3	Circuit diagram of the single-cell PV module	32
2.4	PV DC/DC converters series connection	33
2.5	Two PV panels represented as current sources connected in series	34
2.6	GCC DC/DC	35
2.7	DC/DC flyback converter	36
2.8	GCC multi-chopper PV System	37
2.9	Two PV sources GCC multi chopper	38
2.10	On and off switching states of two sources GCC multi stage chopper	40
2.11	GCC operating points under different switching duty ratio	41
2.12	GCC power, current, and voltage waveforms as a function of duty ratio	42
2.13	Retrofit PV system	43
2.14	Retrofit and GCC PV systems under same switching states	44
2.15	Retrofit circuit in different switching states	44
2.16	Multilevel inverters	47
3.1	Five-level multiple-source (DC-link) inverter	51
3.2	Switching states and current path of five-level DC-link inverter	52
3.3	Five-level DC-link inverter and control block diagram applied for R and R-L loads	54
3.4	Five-level DC-link inverter and control block diagram applied for grid connected applications	54
3.5	Space-vector representation of reference voltage and switching states and three-phase two-level inverter circuit	57
3.6	Symmetrical SVPWM patterns sequence	59
3.7	Space-vector depiction of 3 and 5 level inverters switching patterns	60
3.8	Sub-vector representation	62
3.9	Vector space divided in to two-level hexagons	62
3.10	Two-level based generalized multilevel SVPWM	63
3.11	Three-phase Direct PWM switching sequence	64
3.12	IPWM reference and output waveforms	65
3.13	Generalized IPWM algorithm	66

3.14 Modified Generalized IPWM algorithm 67
3.15 Three-phase reference waveforms 68
3.16 Direct PWM phase and line waveforms 68
3.17 Direct PWM phase and line voltage THD 69
3.18 Direct PWM 3D phase and line voltage spectra 70
3.19 IPWM phase and line waveforms 72
3.20 IPWM phase and line voltage THD 72
3.21 IPWM 3D phase and line voltage spectra 73
3.22 *n* PV sources DC-Link inverter system 74
3.23 Direct PWM waveforms 75

4.1 I-V PV characteristics and load line 77
4.2 Simple MPPT system with voltage-feedback controller 79
4.3 Simple MPPT system with power-feedback controller 80
4.4 P&O algorithm flowchart 82
4.5 I-V PV power characteristic with d*P*/d*V* changes 83
4.6 IncCond algorithm flowchart 84
4.7 Simple MPPT diagram using HC algorithm 85
4.8 Hill-Climbing algorithm flowchart 85
4.9 PV power characteristic with d*P*/d*D* changes “buck-converter” 86
4.10 Adaptive Hill-Climbed algorithm flowchart 87
4.11 The proposed VH-P&O MPPT algorithm 89
4.12 Buck-converter PV simulated system and on/off states 90
4.13 The MPPT curve shown via (a) PV power curve (b) PV I-V curve 92
4.14 The switching duty ratio and the PV power-difference responses 92
4.15 Extracted PV power waveform 93
4.16 Power converter input and output voltage waveforms 93
4.17 Power converter input and output current waveforms 94
4.18 Irradiance and switching duty-ratio waveforms 94
4.19 PV I-V tracking curve as a result of slow irradiance changes 95
4.20 PV power tracking curve as a result of slow irradiance changes 95
4.21 PV voltage, current, power, impedance and duty ratio waveforms under rapid irradiance changes 96

4.22	PV I-V tracking curve as a result of rapid irradiance changes	97
4.23	PV power tracking curve as a result of rapid irradiance changes	97
4.24	PV voltage waveform with different perturbation step size	98
4.25	P&O and VH-P&O MPPT voltage and power waveforms	99
4.26	Power tracking curves of P&O and VH-P&O algorithms	99
4.27	P&O and VH-P&O MPPT PV voltage waveforms as result of applying rapid irradiance changes	100
4.28	3D PV power tracking curve (P&O MPPT)	101
4.29	3D PV power tracking curve (IncCond MPPT)	101
4.30	3D PV power tracking curve (HC MPPT)	102
4.31	3D PV power tracking curve (VH P&O MPPT)	102
5.1	Five-level DC-link inverter system applied for R and R-L loads	105
5.2	R load output voltage and current waveforms by using five-level DC-Link	108
5.3	The Transient of PV extracted power under 1000 W/m^2 irradiance by using five-level DC-Link inverter with R load	108
5.4	R-L load output voltage and current waveforms (Five-level DC-Link)	110
5.5	The reference voltage, inductor current and voltage waveforms	110
5.6	Grid-connected five-level DC-link inverter system	111
5.7	Grid-connected steady-state waveforms of output voltage and current by using five-level DC-Link inverter	113
5.8	Fundamental harmonic of output voltage, grid voltage, current and voltages across R and L by using five-level DC-Link inverter	113
5.9	Transient response waveforms of fundamental output voltage and current during connection	114
5.10	Transient waveforms of PV extracted power	114
5.11	Grid-connected steady-state waveforms of output voltage and current by using seven-level DC-Link inverter	115
5.12	Grid-connected steady-state waveforms of output voltage and current by using nine-level DC-Link inverter	115
5.13	Fundamental harmonic of output voltage, grid voltage, current and voltages across R and L by using seven-level DC-Link inverter	116

5.14	Fundamental harmonic of output voltage, grid voltage, current and voltages across R and L by using nine-level DC-Link inverter	117
5.15	Seven-level PV DC-link inverter system with PV permutation algorithm	118
5.16	Numerical PV source permutation mechanism	119
5.17	Waveforms of the PV permutation algorithm	121
5.18	Flowchart of the PV permutation algorithm for seven-level inverter	124
5.19	Generalized improved PV permutation algorithm	126
5.20	I-V PV source characteristics for different irradiance levels	127
5.21	Five-level inverter voltage waveforms under different partial shading levels achieved via PV permutation algorithm and the improved algorithm	130
5.22	Transient power waveforms of PV1 and PV2 of the DC-link inverter under different partial shading conditions	131
5.23	Seven-level inverter voltage waveforms under different partial shading levels achieved via PV permutation algorithm and the improved algorithm	132
5.24	Nine-level inverter voltage waveforms under different partial shading levels achieved via the improved PV permutation algorithm	133
5.25	Eleven-level inverter voltage waveforms under different partial shading levels achieved via the improved PV permutation algorithm	134
5.26	Irradiance waveforms, the extracted power of PV1 and PV2, and load power of five-level DC-link inverter	135
5.27	Irradiance waveforms, the extracted power of PV1,2,3, and load power of seven-level DC-link inverter	136
6.1	SSP-10W PV module	138
6.2	Electromagnetic spectrum	139
6.3	Solar spectrum	139
6.4	Spectrum generated by HPS and halogen bulb	140
6.5	Circuit for emulation of PV module I-V characteristic	141
6.6	Circuit of the PV DC-DC buck converter system	142
6.7	Current sensing and interfacing circuits	143
6.8	Voltage sensing and interfacing circuits	144

6.9	Interfacing and MOSFET driving circuits	145
6.10	DC power supply connections	146
6.11	Circuit of the five-level DC-link inverter system	147
6.12	Circuit of the seven-level DC-link inverter system	148
6.13	The overall experimentally implemented DC-link inverter system	149
6.14	The three PV modules and their applied lighting	149
6.15	Buck converter control flowchart	151
6.16	Up counting and the related PWM output	152
6.17	Three PV modules DC-link inverter control flowchart	153
6.18	DSP GIO output signals	154
6.19	Up and down counting and the related PWM output	154
6.20	Buck converter control by using Simulink Target Support Package	155
6.21	Five-level DC-link inverter control by using Simulink Target Support Package with RTDX input and output channels	157
6.22	Seven-level DC-link inverter control by using Simulink Target Support Package with RTDX input and output channels	158
6.23	Matlab GUIDE and the interface elements used to design the GUI window for the seven level DC-link inverter	160
7.1	Short-circuit current of the PV module exposed to 400 W HPS bulb	163
7.2	Short-circuit current of the PV module exposed to 400 W halogen bulb	164
7.3	Short-circuit current of the PV module exposed to 400 W three-phase halogen bulb	164
7.4	MOSFET gate control signal of the I-V display circuit, and the related PV module current and voltage waveforms	165
7.5	I-V characteristic of SSP-10W PV module at different irradiances	165
7.6	PV voltage, PV current, PV power waveforms for P&O MPPT	166
7.7	PV voltage, PV current, PV power waveforms for VH-P&O MPPT	167
7.8	Resistive load voltage waveform and spectra obtained by applying IPWM algorithm	168
7.9	R-L load output voltage and current waveforms obtained by applying IPWM algorithm	169

7.10 Resistive load output voltage waveform at uneven irradiances obtained by applying IPWM algorithm 170

7.11 Five-level output voltage waveform at full irradiances of 1000 W/m^2 obtained by applying PV permutation algorithm 171

7.12 PV modules current and voltage waveforms at G_{pv1}, G_{pv2}=1000 W/m^2 using PV permutation algorithm for two PV sources DC-link inverter 172

7.13 RTDX GUI window for two PV sources DC-link inverter at full irradiance of 1000 W/m^2 achieved by PV permutation algorithm 172

7.14 Five-level output voltage waveform at G_{pv1}=1000 W/m^2, G_{pv2}=700 W/m^2 using PV permutation algorithm 173

7.15 PV current and voltage waveforms at G_{pv1}=1000 W/m^2, G_{pv2}=700 W/m^2 using PV permutation algorithm for two PV sources DC-link inverter 173

7.16 RTDX GUI window for two PV sources DC-link inverter controlled by PV permutation algorithm at G_{pv1}=1000 W/m^2, G_{pv2}=700 W/m^2, and G_{pv1}=700 W/m^2, G_{pv2}=1000 W/m^2 174

7.17 Five-level output voltage waveform at G_{pv1}=1000 W/m^2, G_{pv2}=500 W/m^2 achieved by PV permutation algorithm 175

7.18 PV current and voltage waveforms at G_{pv1}=1000 W/m^2, G_{pv2}=500 W/m^2 using PV permutation algorithm for two PV sources DC-link inverter 175

7.19 RTDX GUI window for two PV sources DC-link inverter controlled by PV permutation algorithm at G_{pv1}=1000 W/m^2, G_{pv2}=500 W/m^2, and G_{pv1}=500 W/m^2, G_{pv2}=1000 W/m^2 176

7.20 Five-level output voltage waveform at G_{pv1}=1000 W/m^2, G_{pv2}=250 W/m^2, achieved by PV permutation algorithm 177

7.21 PV current and voltage waveforms at G_{pv1}=1000 W/m^2, G_{pv2}=250 W/m^2 obtained by PV permutation algorithm for two PV sources DC-link inverter 177

7.22 RTDX GUI window for two PV sources DC-link inverter controlled by PV permutation algorithm at G_{pv1}=1000 W/m^2, G_{pv2}=250 W/m^2, and G_{pv1}=250 W/m^2, G_{pv2}=1000 W/m^2 178

7.23 Three-phase halogen lighting structure 179

7.24 PV modules voltages under identical irradiance of 1000 W/m^2 179

7.25 Seven-level output voltage and current waveforms at G_{pv1}, G_{pv2}, G_{pv3}=1000 W/m^2 obtained by using PV permutation algorithm 180

7.26 PV modules currents under identical irradiance of 1000 W/m^2 180

7.27 RTDX GUI window for three PV sources DC-link inverter controlled by PV permutation algorithm at full irradiance of 1000 W/m^2 181

7.28 R-L load voltage and current waveforms at G_{pv1}, G_{pv2}, G_{pv3}=1000 W/m^2 achieved by PV permutation algorithm for three PV sources DC-link inverter 181

7.29 Voltage waveform of 16.5 Ω at identical irradiance of 1000 W/m^2 obtained using PV permutation algorithm for three PV sources DC-link inverter 182

7.30 Voltage waveform of 4.5 Ω at identical irradiance of 1000 W/m^2 obtained using PV permutation algorithm for three PV sources DC-link inverter 182

7.31 Three PV sources DC-link inverter load voltage, load current, PV currents, and PV voltages waveforms. G_{pv1}=G_{pv3}=1000 W/m^2, G_{pv2}=500 W/m^2, achieved by applying PV permutation algorithm 183

7.32 Three PV sources DC-link inverter controlled by PV permutation algorithm load voltage, load current, PV currents, and PV voltages waveforms. G_{pv1}=G_{pv2}=1000 W/m^2, G_{pv3}=150 W/m^2 184

7.33 Three PV sources DC-link inverter controlled by PV permutation algorithm load voltage, load current, PV currents, PV voltages waveforms. G_{pv1}=1000 W/m^2, G_{pv2}=750 W/m^2, G_{pv3}=250 W/m^2 185

7.34 Three PV sources DC-link inverter controlled by PV permutation algorithm load voltage, load current, PV currents, PV voltages waveforms. G_{pv1}=500 W/m^2, G_{pv2}=1000 W/m^2, G_{pv3}=250 W/m^2 186

7.35 RTDX GUI window for three PV sources DC-link related to Fig.6.31 187

7.36 RTDX GUI window for three PV sources DC-link related to Fig.6.32 187

7.37 RTDX GUI window for three PV sources DC-link related to Fig.6.33 188

7.38 RTDX GUI window for three PV sources DC-link related to Fig.6.34 188

7.39 Load current and voltage waveforms of three PV sources DC-link inverter controlled by improved PV permutation algorithm at irradiances of G_{pv1}=G_{pv3}=1000 W/m^2, G_{pv2}=500 W/m^2 189

7.40 Load current and voltage waveforms of three PV sources DC-link inverter controlled by improved PV permutation algorithm at irradiances of G_{pv1}=G_{pv2}=1000 W/m^2, G_{pv3}=150 W/m^2 190

7.41 Load current and voltage waveforms of three PV sources DC-link inverter controlled by improved PV permutation algorithm at irradiances of G_{pv1}=1000 W/m^2, G_{pv2}=750 W/m^2, G_{pv3}=250 W/m^2 190

7.42 Load current and voltage waveforms of three PV sources DC-link inverter controlled by improved PV permutation algorithm at irradiances of G_{pv1}=500 W/m^2, G_{pv2}=1000 W/m^2, G_{pv3}=250 W/m^2 190

Abbreviations

ADC	Analogy to Digital Converter
ANN	Artificial Neural Network
AM	Air Mass
BL	Bridge Linked
CAN	Controller Area Network
CCS	Code Composer Studio
CMPR	Compare Register
CPU	Central Processing Unit
CTR	Control Register
DF	Distortion Factor
DSP	Digital Signal Processor
ePWM	Enhanced Pulse Width Modulation
FF	Fill Factor
FFT	Fast Fourier Transform
GCC	Generation Control Circuit
GIO	General Input Output
GUI	Graphical User Interface
HC	Hill-Climbing
HPS	High Presser Sodium
IncCond	Incremental Conductance
I/O	Input / Output
IPWM	Integration to Duty Cycle Conversion PWM
JTAG	Joint Test Action Group
LED	Led Emitting Diode
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPPT	Maximum Power Point Tracking
NPC	Neutral Point Clamped
P&O	Perturb and Observe
PD	Photodiode
PI	Proportional Integral

PLL	Phase Locked Loop
PRD	Period Register
PV	Photovoltaic
PWM	Pulse Width Modulation
RAM	Random Access Memory
RES	Renewable Energy Source
RMS	Root Mean Squared
RTDX	Real Time Data Exchange
SP	Series-Parallel
SPI	Serial Peripheral Interface
SPWM	Sine Pulse Width Modulation
SSA	State Space Averaging
SRAM	Static Random Access Memory
STC	Standard Test Condition
SVPWM	Space Vector Pulse Width Modulation
TCT	Total Cross Tied
TTL	Transistor Transistor Logic
THD	Total Harmonic Distortion
UART	Universal Asynchronies Receiver/Transceiver
USB	Universal Serial Bus
VSI	Voltage Source Inverter
VH P&O	Voltage Hold Perturb and Observe

Symbols

Unless otherwise stated

a	Fraction of ohmic current involved in avalanche breakdown
α	Alpha axis
A	Diode ideality factor
A_n	The integration of the reference waveform (V.s)
A_r	Reference voltage amplitude (V)
β	Beta axis
c	Numerical count
C	Perturbation step size (V)
C_{pv}	PV bypass capacitor (F)
D	Duty ratio
E_g	Energy gap (eV)
f_c	Switching frequency (Hz)
f_r	Reference voltage frequency (Hz)
G	Irradiance (W/m^2)
I_d	Diode current (A)
$I_{F(AV)}$	Average forward current (A)
I_L	Inductor current (A)
I_{link}	DC-link current (A)
I_{mpp}	PV maximum power point current (A)
i_{out}	Output current (A)
I_{ph}	PV photocurrent (A)
I_{pr}	Photocurrent at reference temperature (A)
I_{PV}	Photovoltaic current (A)
I_{sat}	PV saturation current (A)
I_{sc}	PV short circuit current (A)
I_{sh}	PV shunt resistance current (A)
I_{sr}	Saturation current at the reference temperature (A)

K	Space sector number
K_I	Cell's photocurrent temperature coefficient
K_i	PI integral constant
K_p	PI proportional constant
L_f	Filter inductance (H)
m	Avalanche breakdown exponent
M_f	Frequency modulation index
M_a	Amplitude modulation index
N	Inverter level
n	PV sources number
N_s	Number of PV cells in series
N_p	Number of PV cells in parallel
P_{mpp}	Maximum power point PV power (W)
P_{PV}	Photovoltaic power (W)
q	Electron charge (C)
R_{pv}	PV resistive (Ω)
R_L	Load resistance (Ω)
R_f	Filter resistance (Ω)
R_p	Pull-up resistance (Ω)
R_{pv}	PV source resistance (Ω)
R_s	PV series resistance (Ω)
R_{sh}	PV shunt resistance (Ω)
$T_{0,1,2,\ldots}$	Switching pattern dwelling time (s)
T_c	Switching time period (s)
T_{cel}	Cell temperature (K)
t_{off}	Switch off time (s)
t_{on}	Switch on time (s)
T_r	Cell Reference temperature (K)
t_{rr}	Reverse recovery time (s)
v_1	50Hz fundamental voltage (V)
$V_{a,b,\text{ or }c}$	a, b or c phase voltage (V)
V_{br}	Junction breakdown voltage (V)

v_{cpv}	PV bypass capacitor voltage (V)
v_D	Diode voltage (V)
V_{dc}	Inverter DC input voltage (V)
V_F	Forward voltage (V)
v_g	Grid voltage (V)
V_j	PV junction voltage (V)
V_l	Level voltage (V)
v_L	Inductor voltage (V)
V_{link}	DC-link voltage (V)
V_{mpp}	PV maximum power point voltage (V)
V_{oc}	PV open circuit voltage (V)
$\vec{V}_{offset}$	Offset vector
V_{oh}	High voltage level (V)
V_{ol}	low voltage level (V)
v_{out}	Output voltage (V)
V_{pv}	Photovoltaic voltage (V)
v_{ref}	Reference voltage (V)
$\vec{V}_{ref}$	Reference voltage vector
V_{RRM}	Maximum repetitive reverse voltage (V)
$\vec{V}_{two}$	Two-level reference voltage vector
V_t	PV thermal voltage (V)
V_α	Alpha component
V_β	Beta component
x	Reference vector angle with α-axis

Chapter 1

Introduction and Problem Definition

Increasing energy demand and the need to find clean and cheap alternative energy sources have led to extensive research in renewable energy sources (RES). The growth in the RES market is also directly related to the development of power electronics [1]. Among several types of RES the photovoltaic (PV) energy source has benefits such as high efficiency, reliability and a long life. In addition, it is also characterized by low cost, freedom from moving components and also easy and quick to setup [2].

In PV power applications, establishing PV arrays with the desired voltage levels involves individual PV modules linked in series. The serious issue in such configurations is to manage the partial shading problem which arises from exposing the series connected PV modules to uneven insolation. The PV partial shading is a consequence of clouds, poles, trees, dust, dirt or any obstacles which cause different levels of irradiance at the surface of the PV modules.

As a result of the PV partial shading, the generated current of the series connected PV modules is limited by that of the shaded PV modules. Consequently, this not only reduces the overall generated power significantly, but also causes a hot-spot effect resulting in damage to some PV cells and malfunction of the PV system. The PV partial shading problem increases the maintenance cost of the PV system, and the power loss makes the PV generated power more expensive than originally planned.

The simplest method to reduce the effects of the PV partial shading problem is connecting a bypass diode across each PV module in the series string. However, more than one power peak (in the PV power curve) can appear and to reach the maximum power a maximum power point (MPP) tracker has to be used. Reaching

the MPP does not mean all the shaded PV modules have to be bypassed, and so the remaining shaded modules still limit the current to a certain extent, but partial shading effects are reduced. Bypassing PV modules from the series PV connection that would otherwise be reverse biased actually raises the total output DC voltage level. In other words, bypassing some shaded PV modules improves the total generated power. Yet that still represents a sort of wasted power, which could potentially be generated from the bypassed modules. Also, even though the system is operated at its MPP, the generated power is still lower than that achievable by the modular configuration (not series connection) due to the mismatch power loss of the series connection [3-5].

1.1 PV fundamentals and cell modelling

The conversion of the solar radiation into electricity is known as the photovoltaic (PV) effect which can be achieved via solar cells. Among semiconductor materials, the crystalline silicon cells are the most widespread PV source and dominate more than 95% of the market. This is due to their high efficiency compared with other materials.

Fig.1.1 shows the silicon crystal lattice, where electron pair bonds are formed and so a stable electron configuration results (the outer shell of the silicon atoms includes eight electrons). Although the applied energy (solar energy) results in an intrinsic conductivity state where free electron and hole result, electrical energy cannot be generated [6].

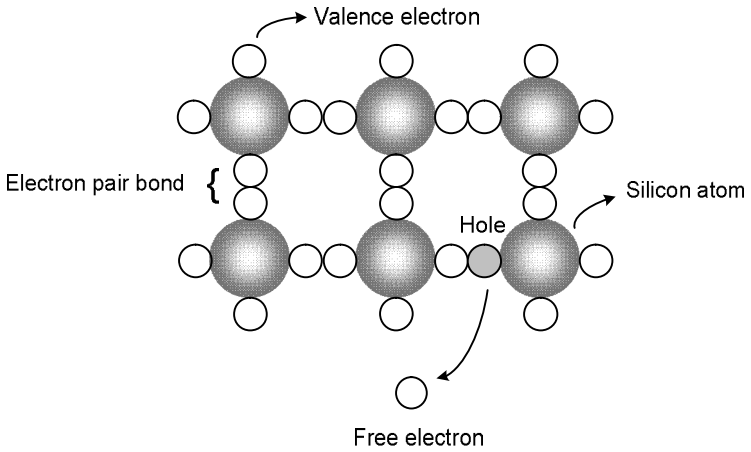


Fig.1.1: Silicon crystal lattice and intrinsic conductivity.

The crystalline silicon solar cell can be achieved by creating semiconductor material with a p-n junction. That is accomplished by adding doping atoms to the silicon crystal lattice, for example, phosphorus atoms to create an n-layer and boron atoms to create a p-layer, where extrinsic conduction results. In between the two layers, a p-n junction is created, and so the free electrons in the n-layer diffuse into p-layer causing a depletion region to be established as shown in Fig.1.2a.

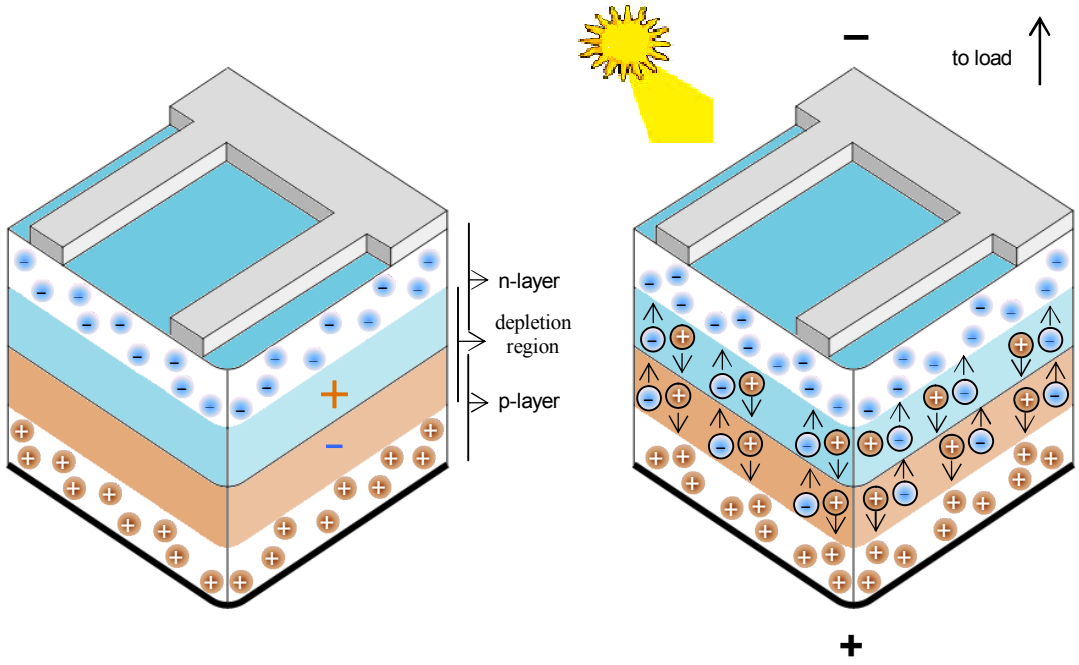


Fig.1.2: PV cell semiconductor layers (a) non-illuminated and (b) illuminated.

As can be seen in Fig.1.2b, when the PV cell is insolated, the electrons in the depletion region are exited where the created bonds are broken. The resultant free electrons are drawn towards the n-layer due to the electrical field, while the holes leave in the opposite direction. That diffusion causes the voltage to arise across the solar cell terminals.

The solar cell can be modelled as shown in Fig.1.3a, the p-n silicon semiconductor is a diode, so under a dark condition the solar cell is represented by a diode (Fig.1.2a). The photovoltaic effect is represented by an irradiance dependent current source which generates photocurrent (I_{ph}) according to the irradiance level. The solar cell losses are represented by two resistances, the series resistance (R_s) and the shunt (R_{sh}) resistance. R_s represents the ohmic resistance losses such as the resistance of the semiconductor, metal contacts, and contacts between them. R_{sh} describes the leakage currents through the edges of the solar cell as well as the p-n

junction (due to material defects). For a more accurate equivalent circuit, another diode can be added in parallel to the first diode. The added diode represents the recombination which happens in the space charge region out of the depletion region. However, for simplicity the additional diode will not be considered in the simulations for this research [7].

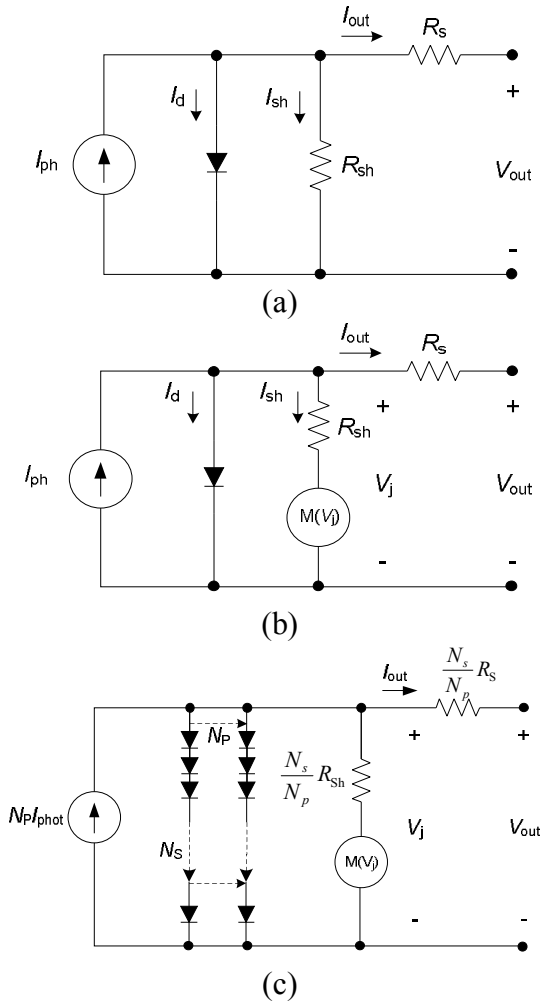


Fig.1.3: PV equivalent circuit (a) cell model, (b) cell model with reverse bias characteristics, and (c) PV array model with reverse bias characteristics.

One of the main causes for electrical mismatching among the serial connected PV cells is due to partial shading, where a different number of carriers are generated according to the cell irradiation level. The carrier difference forces the majority carriers of the shaded cell (the lowest carrier number) to leave the layers, so the depletion region is increased. When the electrical field is significantly increased, more carriers are accelerated and therefore further ionization occurs in the lattice atoms, results in avalanche breakdown. The temperature of the junction is considerably increased due to the avalanche breakdown current causing thermal breakdown of the shaded solar cell [8].

The PV cell model which considers the reverse characteristics was mainly introduced in 1988 by J. W. Bishop [9], and is shown in Fig.1.3b. As seen, this includes a multiplication factor $M(V_j)$ for the leakage current, I_{sh}, to express the avalanche breakdown mechanism. According to this model, I_{sh}, output current I_{out} and voltage V_{out} can be expressed respectively as follows:

$$I_{sh} = \frac{V_j}{R_{sh}}\left[1 + a\left(1 - \frac{V_j}{V_{br}}\right)^{-m}\right] \qquad \ldots\ldots\ldots \quad (1.1)$$

$$I_{out} = I_{ph} - I_{sat}\left[\exp\left(\frac{q\,V_j}{A\,k\,T_{cel}}\right) - 1\right] - I_{sh} \qquad \ldots\ldots\ldots \quad (1.2)$$

$$V_{out} = V_j - I_{out}\,R_s \qquad \ldots\ldots\ldots \quad (1.3)$$

In the case of several PV cells connected in series and parallel to form a PV array, the PV model can be represented as shown in Fig.1.3c. Where, V_j is the junction voltage, V_{br} is the junction breakdown voltage, a is the fraction of ohmic current involved in the avalanche breakdown, m is the avalanche breakdown exponent, I_{ph} is the photocurrent, I_{sat} is the reverse saturation current, q is the electron charge, A is diode ideally factor, k is Boltzmann constant, and T_{cel} is the cell temperature in Kelvin.

By considering the temperature effect, the saturation current and the photovoltaic current can be determined by applying equations 1.4 and 1.5 respectively [10].

$$I_{sat} = I_{sr}\left(\frac{T_{cel}}{T_r}\right)^3 \exp\left(\frac{q\,E_g}{k\,A}\left(\frac{1}{T_r} + \frac{1}{T_{cel}}\right)\right) \qquad \ldots\ldots\ldots \quad (1.4)$$

$$I_{ph} = (I_{pr} + K_i(T_{cel} - T_r)) \times \frac{G}{1000} \qquad \ldots\ldots\ldots \quad (1.5)$$

Where, T_r is the reference temperature, I_{sr} is the reverse saturation current at reference temperature. E_g is the solar cell energy band gab, I_{pr} is the photocurrent at reference temperature, K_i is the photocurrent temperature coefficient at I_{pr}, and G is the irradiance level.

1.2 Hot-Spots and their Effects

Along with the power reduction caused by the shading in a string connection of illuminated PV cells, considerable damage can be done to the shaded cells if bypass

diodes are not employed. When the PV array current is greater than the short-circuit currents (I_{sc}) of the shaded cells/modules, the shaded cells operate in a reverse biased mode, dissipating their generated power in addition to power from other cells in the series connection (operating as a load) [11]. The power is dissipated in the form of heat, and so the surface of the PV array suffers high degrees of temperature concentrated in small areas at the shaded cells (hot-spots).

For illustrative purposes, supposing two PV cells or two PV modules (two groups of PV cells) are connected in series as shown in Fig.1.4. As a PV partial shading example, the first PV module is under full irradiance whereas the second PV module undergoes a certain level of shadowing. In this situation, I_1 is always greater than I_2 and the load current I_L. However, I_2 might be greater or less than I_L according to the load impedance value. Here I_1 and I_2 are the photocurrents (almost the short circuit currents) of the first and the second PV modules respectively. The diode D2 is in the forward biased mode if I_2 is greater than I_L, and so the module voltage V_2 is still positive even though the system is under a partial shading condition. With a decrease in the load impedance, the modules' currents increase as well as the load current and therefore at a specific point I_L will be greater than I_2. At the mentioned point the surplus current (about I_L-I_2) is leaked in reverse through the diode D2 and the shunt resistance. The reverse biasing of D2 means V_2 is negative, so the power is dissipated in the shaded module causing a hot-spot. The reduction of the PV generated power is due to the fact that the reverse current through D2 is strictly limited so the string current is significantly reduced [12].

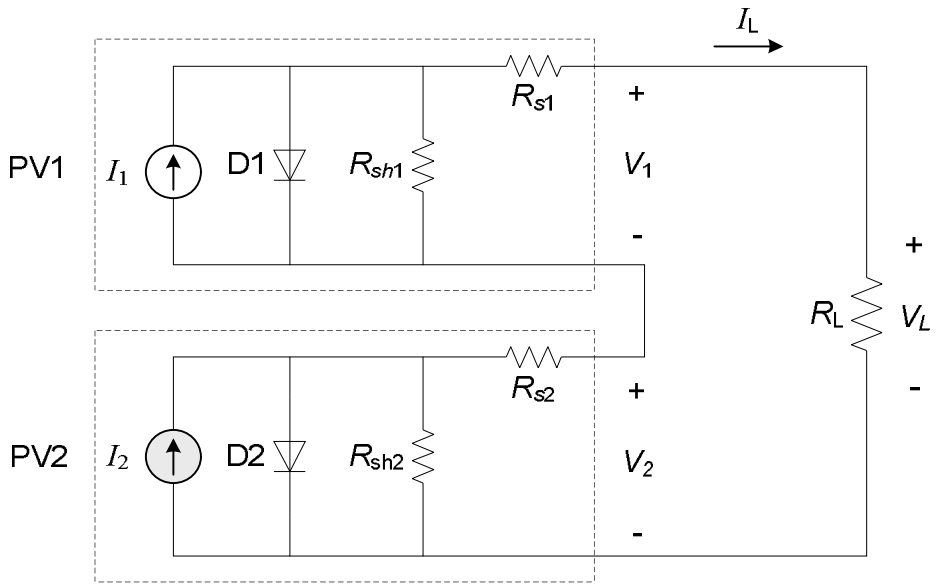


Fig.1.4: Two PV cells/modules connected in series under partial shading.

There are some factors which increase the hot-spot effect, for instance a high ambient temperature, high level of irradiance, low speed of wind, a shadow on a small area of the PV array (number of shaded cells), high reverse current, and poor ventilation of the PV array. According to the results achieved in [13], for a PV cell reverse voltage of -10 V, a high risk of the hot-spot can result if the cell current exceeds 1 A. Table 1.1 describes the forms of damage with the associated effects on the PV array as a result of the hot-spot and according to the level of the PV cell temperature.

TABLE 1.1: The Effects of the Hot-Spots [13]

Temperature (*T*)	**Array damage**	**Consequence**
$T < 150^{o}C$	No damage	No effect
$150^{o}C \leq T < 170^{o}C$	Array encapsulation melting	Delamination of the array heat conducting material
$170^{o}C \leq T < 200^{o}C$	Deterioration of the back sheet	Reduction of the electrical isolation
$T > 200^{o}C$	PV cell p-n junction is destroyed	Loss of the PV operation

Even though the PV partial shading is an incredibly common and frequent problem, it is not the only problem affecting the yielded PV power and leading to hot-spots, these can also be caused by PV cells' manufacturing defects, internal disconnection, cracked PV cells, etc. All the mentioned reasons lead to different current generation between the PV cells in the series connection, so power drop and hot-spots can be a result [11, 14].

1.3 PV Cell Reverse Mode and Shunt Resistance Effect

The I-V characteristic of a PV cell is shown in Fig.1.5, the curve is generated based on the Bishop PV model [9]. As can be seen, in the normal generating operation the PV cell voltage rises to its open circuit voltage (V_{oc}) which is almost 0.6 V. On the other side of the PV curve, the reverse mode of the PV cell is up to the p-n junction breakdown voltage (V_{br}) which can be from 12 to 20 V in poly-Si PV cells, while it can reach 30 V in the mono-Si PV cells [15].

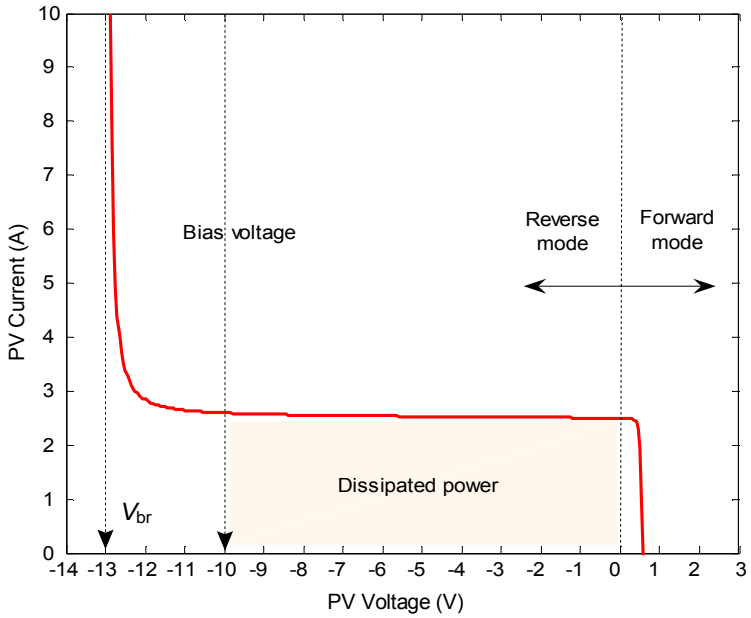


Fig.1.5: PV cell I-V curve (simulated at R_{sh}=200 Ω).

As was previously mentioned, the shaded PV cell is in the reverse biased mode if its short circuit current is lower than the current generated by the non-shaded cells in the string. Fig.1.5 shows a linear region (from 0 V to almost -10 V) within the reverse bias voltage where the current has a linear relation to voltage due to the leakage currents which are assumed to pass through the PV cell shunt resistance R_{sh}. The breakdown of the cell p-n junction occurs due to further increases in the bias voltage when a considerable amount of current is passed. As known, the PV shunt resistance R_{sh} represents the leakage currents due to impurity and defects in the PV cell semiconductor. With increasing impurity concentration, the value of the shunt resistance is decreased, so the break down can occur at lower reverse bias voltages. Around the area where the current exceeds a specific amount it causes permanent damage in the solar cell due to the associated hot-point. In other words, in the forward mode, low R_{sh} results in reducing maximum power point (P_{mpp}), so the fill factor ($FF=P_{mpp}/(V_{oc}.I_{sc})$) is reduced. Also, in the reverse mode, low R_{sh} speeds up any thermal damage to the cell [15].

The simulated I-V characteristics of a PV cell as a function of its shunt resistance are illustrated in Fig.1.6. The 3D graph shows the effect of R_{sh} on the slope of the linear region of the I-V curve as well as the breakdown voltage. PV cells with lower R_{sh} conduct more current in the reverse mode (more dissipated power) along with lower V_{br} than that resulting from PV cells which have relatively high R_{sh}. In the

reverse mode of operation, the shaded PV cells with high R_{sh} reduces the total string current due to the shunt current being low, so the power dissipated in those shaded cells is much lower than the case of low R_{sh} where the shunt current is high.

The effect of the shading level on PV cells with high and low shunt resistance can be found in [16], in the PV cells with high R_{sh}, the worst case condition (largest cell dissipated power i.e. worst hot-spot) occurs at a low shading level. In this case more current is conducted via the shaded cell. However, the worst case condition in PV cells which have low R_{sh} takes place when the shading level is high, where low irradiance level causes more leakage current and consequently more imposed negative voltage and dissipated power.

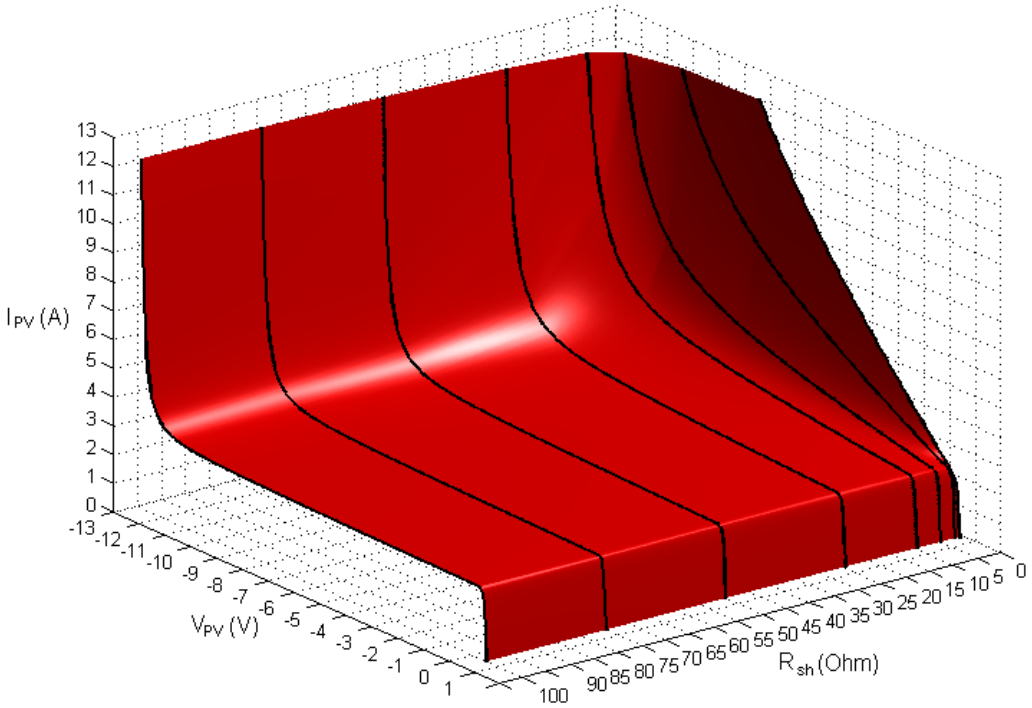


Fig.1.6: PV cell I-V curve depicted in 3D-graph as a function of shunt resistance.

1.4 The Power Reduction

At least one shaded PV cell, in a series connection with illuminated PV cells, can cause significant power reduction in the whole PV system. The shaded PV cell is able to limit the string current to almost its reduced current. For instance, one PV cell operating under various irradiance levels, connected in series with 17 non-shaded cells of (1000 W/m^2), is considered for illustration as shown in Fig.1.7. The I-V

characteristics of the shaded PV cell can be depicted in a 3D graph as shown in Fig.1.8a. The graph is obtained for different irradiance levels (0 to 1000 W/m^2) of the shaded cell (PV1) and the string current is changed from zero to the short circuit current of a PV cell at full irradiance (2.5 A).

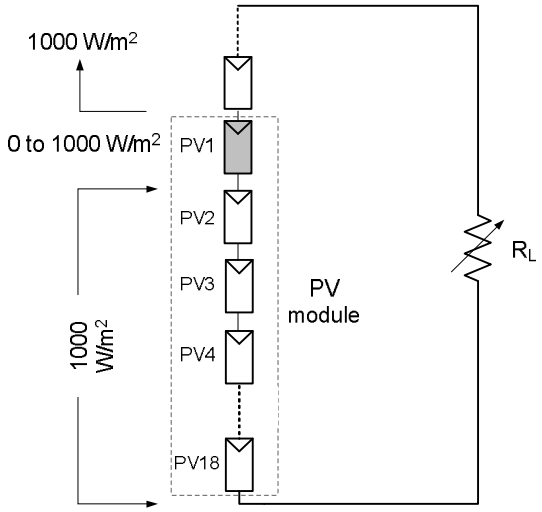


Fig.1.7: 18 PV cells connected in series to form a PV module (one shaded cell and 17 non-shaded PV cells).

As can be seen, at 1000 W/m^2 (no partial shading), the I-V curve of PV1 is only in the positive side where there is no reverse mode of operation. However, the obtained curves under irradiances from 0 to 900 W/m^2 represent different levels of partial shading conditions so the negative side appears. At a given string current, more applied shadow results in more reverse biased voltage across the shaded cell.

The power curve which related to Fig.1.8a is shown in Fig.1.8b. This curve is important in order to indicate the hot-spot raised in the shaded PV cell. For instance, in Fig.1.8b at a given cell reverse voltage of -8 V, more power is dissipated in the shaded cell if G=900 W/m^2 compared with G=100 W/m^2, where 18 W and 3 W are dissipated respectively. It is clear that, the slightly shaded PV cell is more exposed to the risk of damage by the hot-spot.

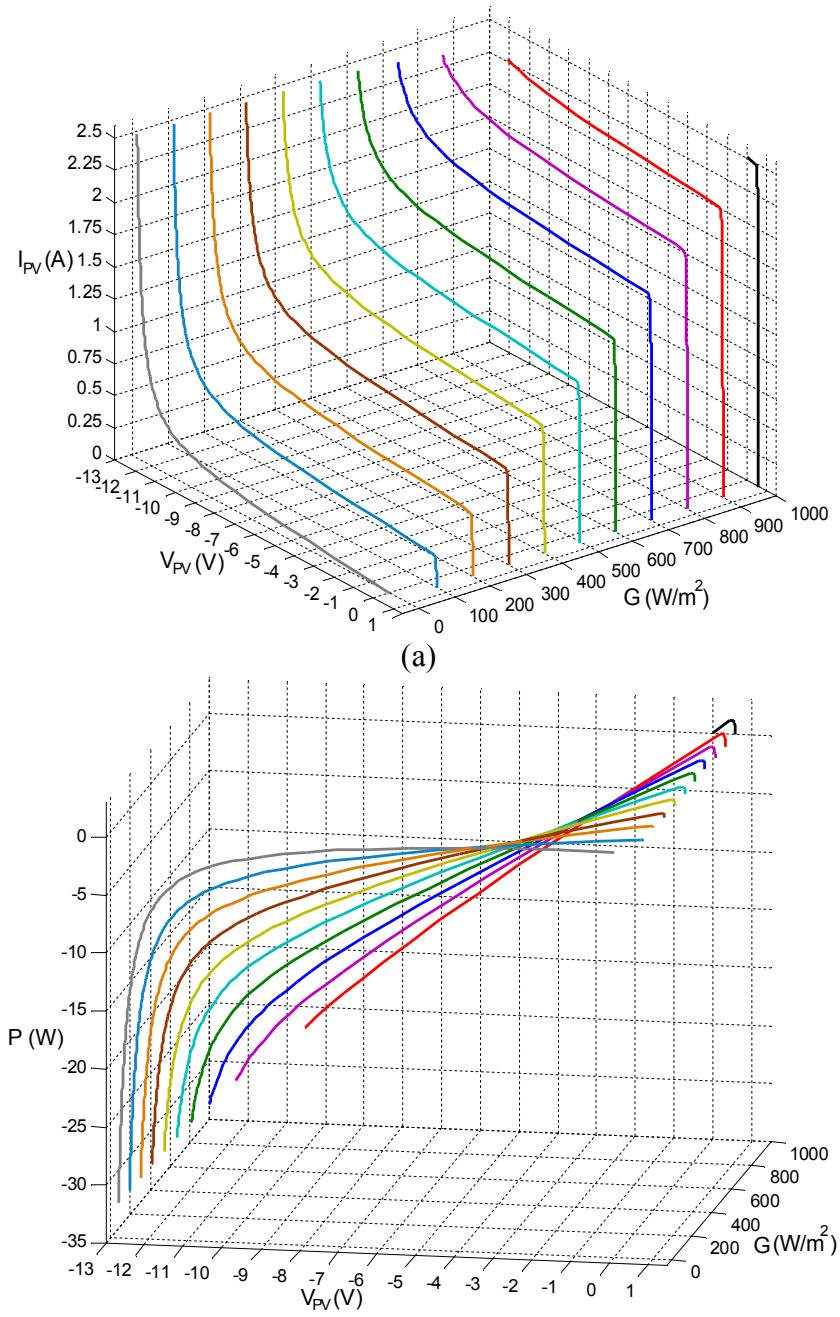
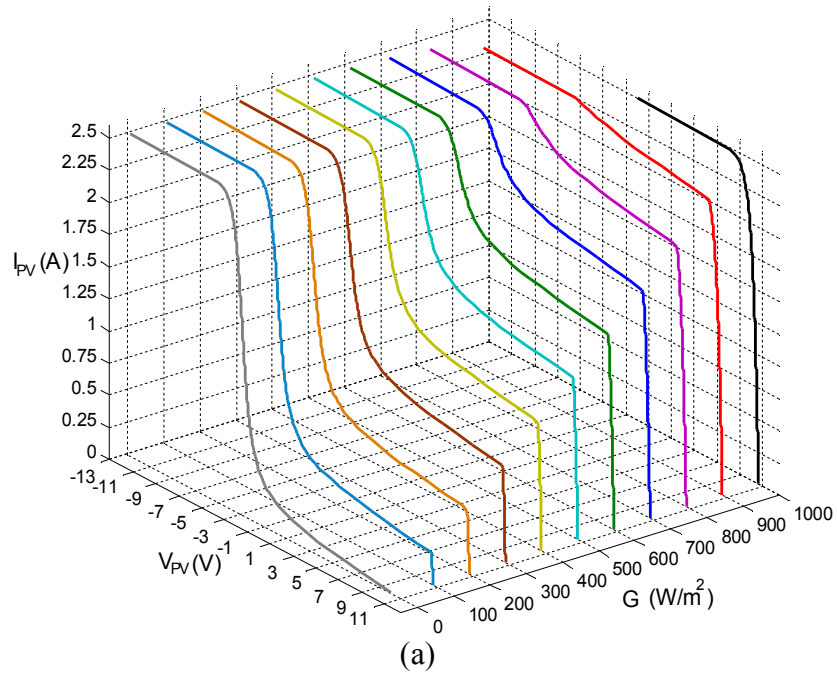


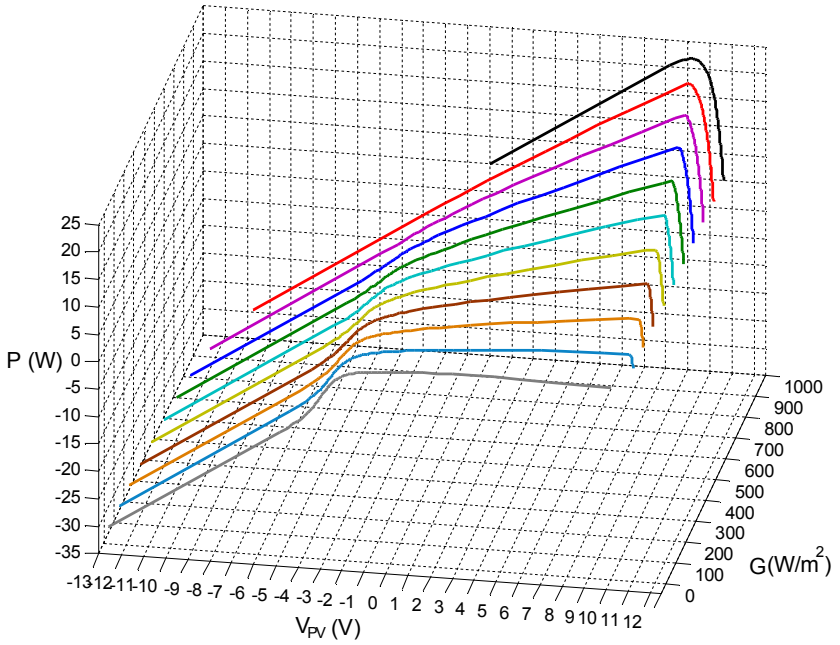
Fig.1.8: PV cell curves as a function of the irradiance level (a) I-V curve and (b) power curve; the cell is connected in series with 17 non-shaded PV cells.

Because the cell reverse voltage is far more than the positive voltage of the non-shaded cells, the effect of one shaded PV cell is considerable. Fig.1.9a illustrates the I-V characteristics of the series connected 18 cells (PV module) as a function of the irradiance level of only one shaded cell, which has the I-V curve shown in Fig.1.8a, in the same series string. Clearly the module current is almost limited to the shaded PV cell current shown in Fig.1.8a. Also, when the module V_{pv} is zero, that means that the negative voltage of the shaded cell is equal to the algebraic summation of the positive voltages generated by the 17 non-shaded cells. When the voltage of the shaded cell

exceeds the bias voltage, towards its break-down voltage, the shaded cell will not limit the current of the other illuminated PV cells in the string any further (so the I-V characteristics of the illuminated cells start to appear as illustrated in the figure) whereas the total module voltage remains negative.



(a)



(b)

Fig.1.9: Curves of 18 PV cells series connection as a function of one cell irradiance level (a) I-V curve and (b) power curve (one cell is shaded the other cells are at 1000 W/m^2).

The power curves of the PV string are illustrated in Fig.1.9b; it is clear how the shaded cell affects the total power generated by the 17 non-shaded cells. In other words, the deeply shaded PV cell can significantly reduce the total generated power.

1.5 PV Bypass Diode Protection

To avoid damage to the shaded PV cells in the series connected string, bypass diodes have been used. The shaded PV cell is reverse biased due to current difference caused by the shaded cell. The current difference caused by partial shading (I_L-I_2 in section 1.2) does not appear because no way to pass through the shaded cell, and so the string current drops down to almost the current of the shaded cell. If a bypass diode is placed across the shaded cell, it will conduct carrying the surplus current, i.e, current difference. Consequently, the dissipated power by the shaded cells/modules is zero, so no hot-spots result.

In PV arrays, the bypass diodes have to be properly allocated for sets of series connected cells (PV modules), so the bypass diode of a PV module which includes the shaded PV cell can turn on before any damage occurs to the shaded cell. The bypass diodes are commonly allocated for each 12 to 18 PV cells in the array. The number of the bypassed series connected PV cells in one set is calculated according to a PV cell worst case condition which is the maximum allowed power dissipation by a shaded PV cell. As soon as the bypass diode of the shaded module (any number of shaded cells in the module) starts to conduct, the shaded module no longer limits the current of the non-shaded modules in the PV array, so the generated power by the PV array is improved. However, a significant reduction in the array voltage results, as the voltage for each conducting diode is about 0.7 V. Such a situation is not recommended in some grid-connected applications where the voltage is the most important factor in delivering the generated power to the grid [15, 17].

The bypass diodes are considered a method for protecting the PV cells from being damaged more than being a method for power improvement. That is because when reaching the required point, which the bypass diode turns on at, a maximum power point tracking (MPPT) system is needed. The MPPT system controls the PV generated current so the operating voltage of the shaded module can be controlled to reach the mentioned point where the bypass diode turns on. For instance, if there are

more than one shaded PV module, not all of them have to be bypassed in order to reach the MPP of the PV array via the MPPT system. The deeply shaded modules are bypassed and the other less shaded ones might be left with the non-shaded modules for seeking the MPP.

As a further illustration for how it works, a simple example of two series connected PV arrays which is presented in [18] is considered here. As can be seen in Fig.1.10, two PV arrays are connected in series - the first one (PV1) is non-shaded, and is exposed to an irradiance of 1000 W/m^2, whereas the second one (PV2) is half shaded. Start with a large resistance value where the open circuit situation can be assumed. The variable resistance is decreased iteratively so the PV current will increase and as a result Point 1 is reached. It is clear from the separated PV curves, at Point 1 the two PV arrays produce power but the MPP has not been achieved yet. By further load resistance decrease, the Point 2 will be reached because of the current increasing. At this point, the MPP of the shaded array, which has the first plus sign in Fig.1.11a, is reached. However, to reach the MPP of PV1 a higher current has to be drawn. Further load resistance decrease will result in a higher load current than the shaded PV short circuit current and also, the PV voltage has just turned negative causing the activation of the related bypass diode. At Point 3, the PV1 yields power while PV2 is bypassed. Further load resistance reduction will lead to a rise in the circuit current so the MPP of PV1 is reached at Point 4 whereas PV2 does not produce power [18, 19]. Fig.1.11b shows the associated power curves.

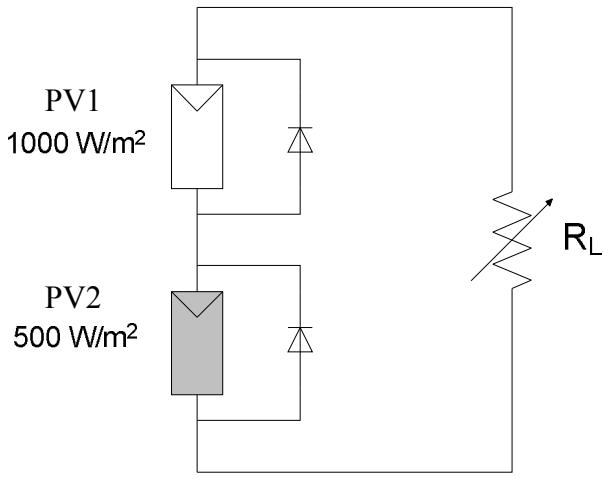


Fig.1.10: Two PV arrays with bypass diodes, one PV array is shaded.

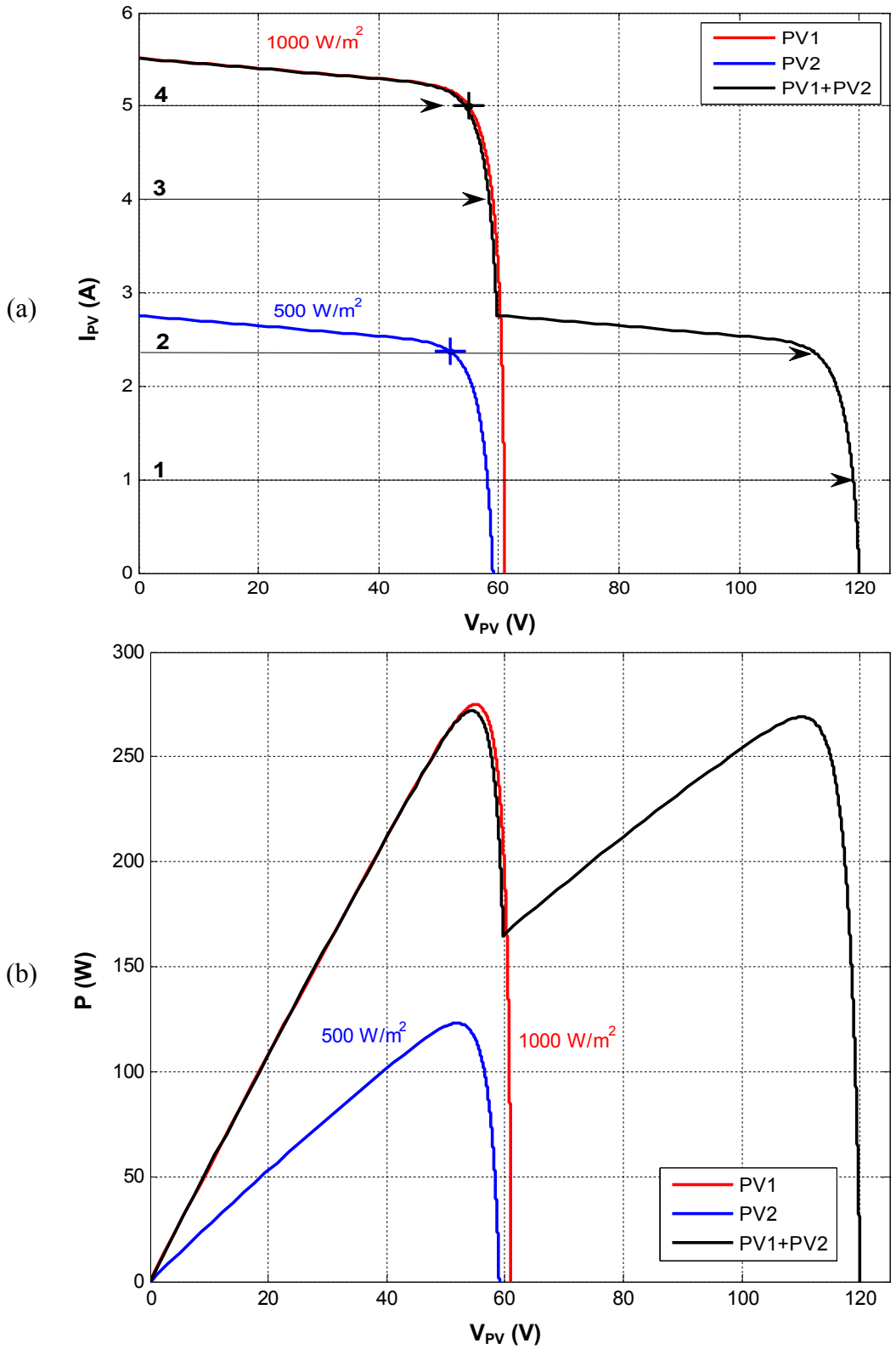
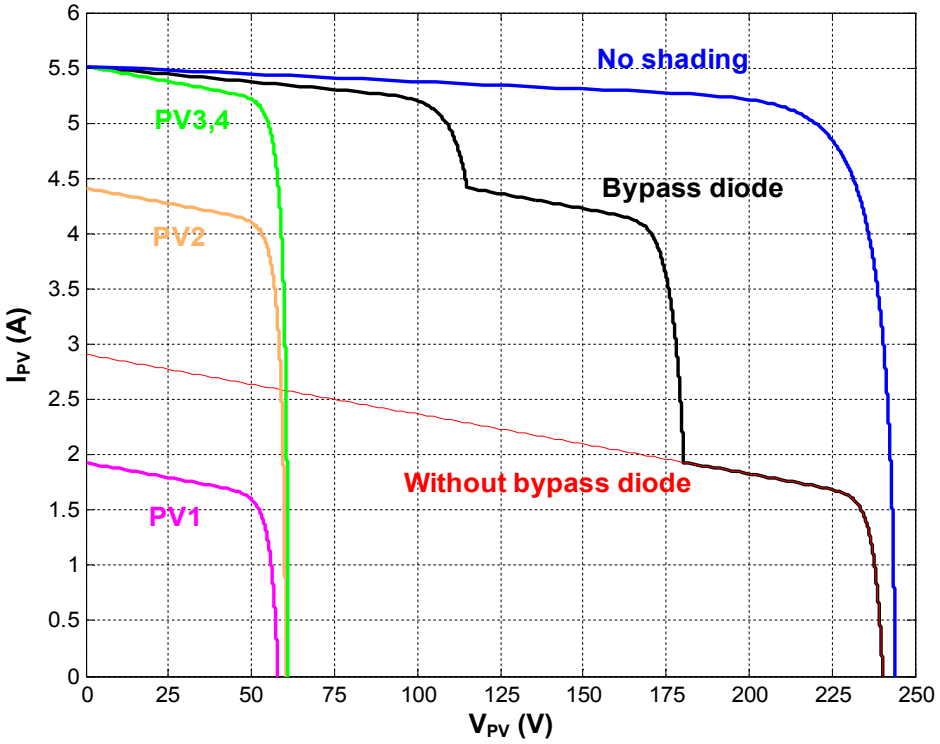


Fig.1.11: Two PV arrays connected in series (a) I-V curves and (b) power curves.

Another case can be considered here for four PV arrays connected in series, two of them are fully illuminated and the other two are shaded at different irradiance levels. As shown in the I-V and the power characteristic curves in Figures 1.12a and 1.12b, at uniform irradiation condition there is only one MPP (the blue curves).

(a)



(b)

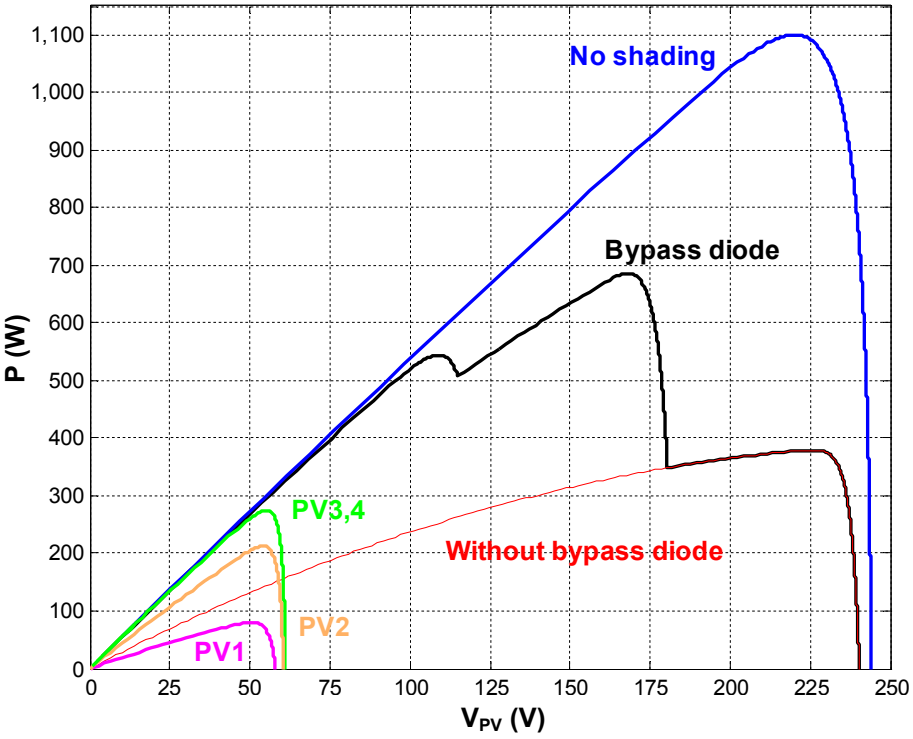


Fig.1.12: Four PV arrays connected in series PV1, 2 at 1000 W/m^2, PV3 at 800W/m^2, PV4 at 350 W/m^2 (a) I-V curves and (b) power curves.

However, for non-even illumination, multiple peak power points are shown on the black curves (three peak power points). It is possible to apply an MPPT algorithm to enable the system to operate at the highest MPP [1, 18, 20], but the output power is still much lower than the total power generated when these modules function independently. If the partial shading issue is overcome, all the PV arrays (shaded and

non-shaded arrays) in the series string could deliver their maximum power to the load without affecting each other.

1.6 Worst Case Condition and the Effect of Shaded Cells Number

According to the maximum power dissipation allowed by a shaded PV cell, the bypass diodes are placed across the set of series connected PV cells to form one or a half PV module with bypass diode protection. Fig.1.13 shows two PV modules, each module includes 18 series connected PV cells, a bypass diode is allocated per set. Assume the first PV module is fully illuminated (1000 W/m^2) while the another module contains one shaded cell (0 to 1000 W/m^2), so the shaded cell reverse voltage required to turn on the bypass diode can be calculated by the $N_i \times V_{PV} + V_{d(on)}$. N_i, V_{PV}, $V_{d(on)}$ are the number of the illuminated PV cells in the PV module, cell voltage (~0.5), the bypass diode turn on voltage respectively [15].

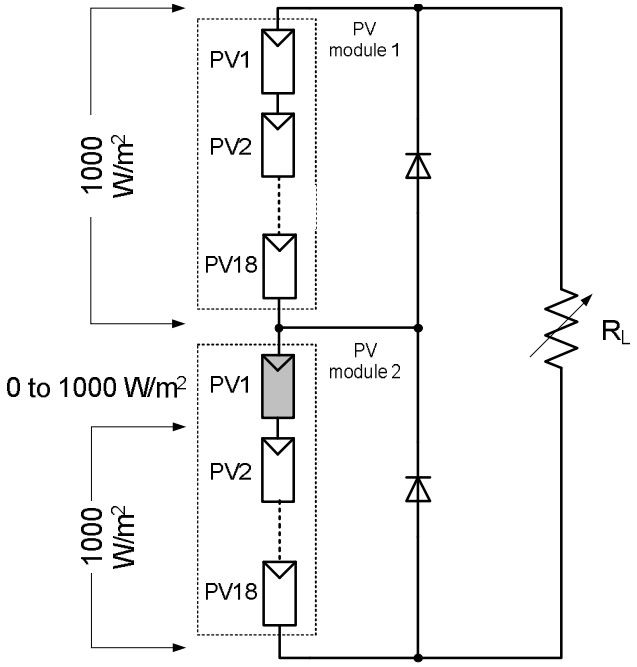


Fig.1.13: Two PV modules with bypass diodes, one PV cell is shaded.

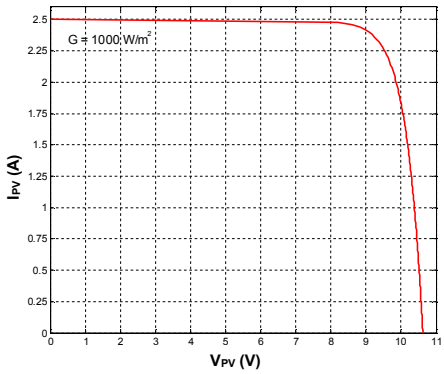
Figures 1.14a and 1.14b show the I-V curves for PV module 1 and module 2 respectively, while Fig1.14c shows the overall I-V curves of the PV system illustrated in Fig.1.13. The related power curves are illustrated in Fig.1.15. As seen, before the bypass diode of module 2 conducts, the shaded cell limits the system current to almost the shaded cell current. The diode conducts when the shaded cell voltage is between -8.75 V and -10.25 V according to the irradiance level of the shaded cell

(PV1), and after this point the system current recovers to the current of the non-shaded module in the string.

With respect to the MPP, there are two MPPs as shown in Fig.1.15c, one when the system current reaches the MPP current (I_{mpp}) of the shaded cell and a second after the bypass diode of the shaded module conducts, i.e., exactly when the system current reaches I_{mpp} of the non-shaded cells. In the power curves for 0 to 400 W/m^2 the second MPPs are the global maxima while the first MPPs are local maxima. The situation reverses above 500 W/m^2, so reaching the highest MPP needs a MPPT system.

If further non-shaded PV cells are added to the 18 series connected PV cells, which includes one shaded PV cell (PV1), more negative voltage is required across the shaded cell to reach the turn on voltage $V_{d(on)}$ of the bypass diode, so more power is dissipated in the shaded cell, possibly causing damaged before the diode is conducts.

(a)



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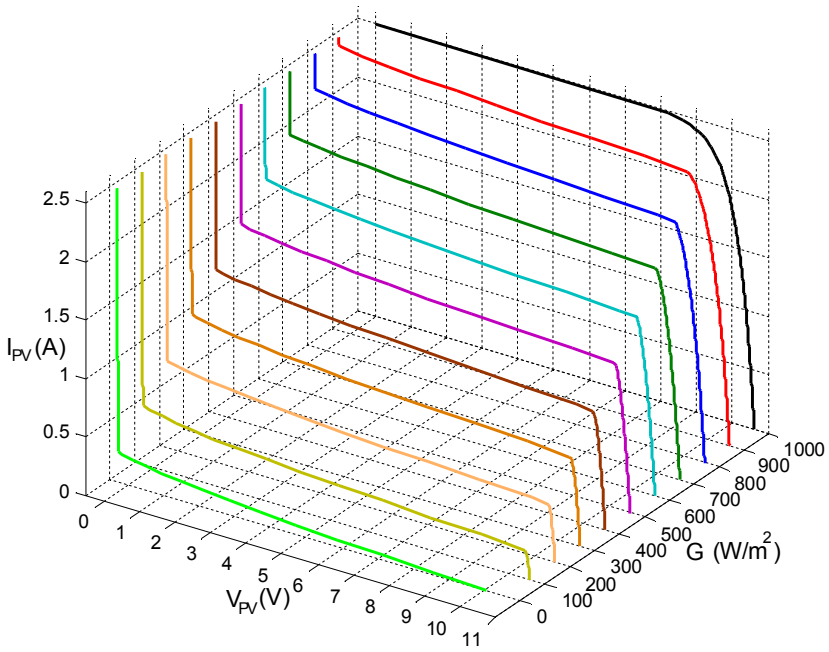
(b)



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(c)

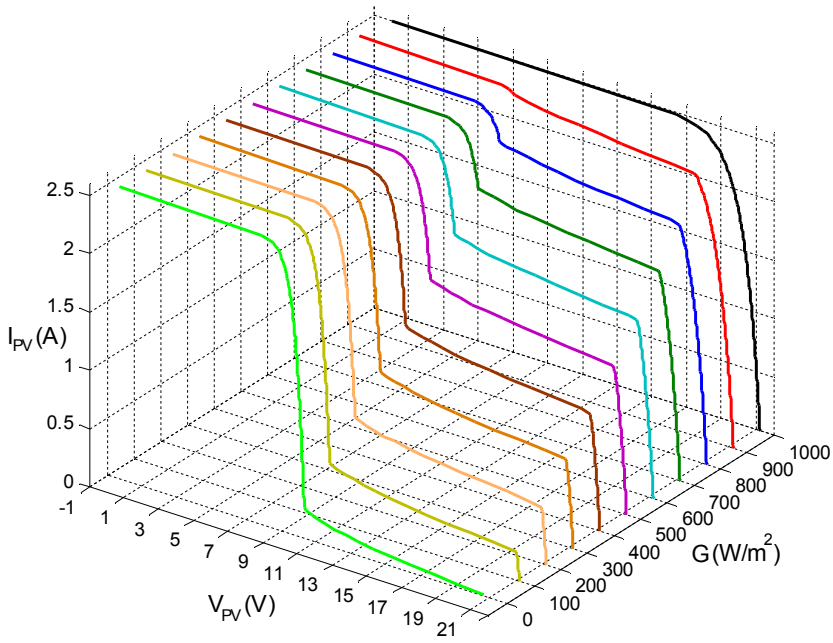
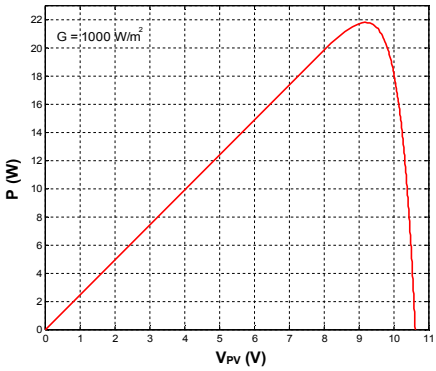


Fig.1.14: I-V curves of (a) PV module 1 at 1000W/m^2, (b) PV module 2, and (c) the two series connected PV modules as a function of one shaded cell irradiance level.

(a)



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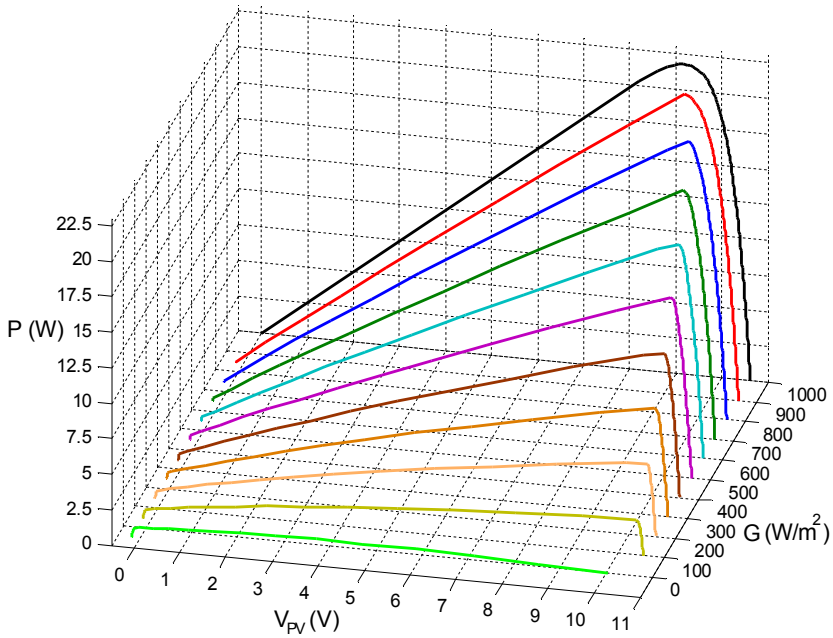
(b)



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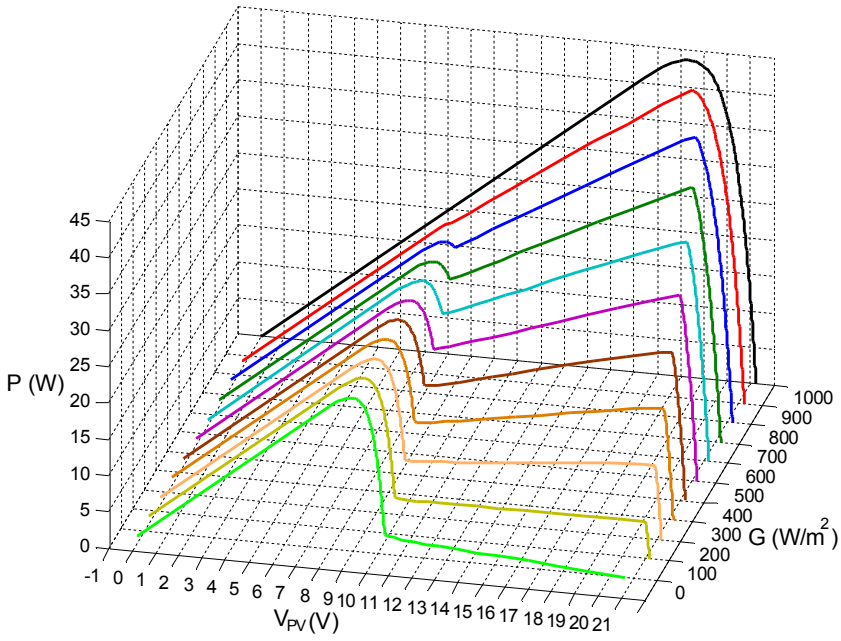


Fig.1.15: Power curves of (a) PV module 1 at 1000W/m^2, (b) PV module 2, and (c) the two series connected PV modules as a function of one shaded cell irradiance level.

With respect to illustrating the turn on points of the bypass diode for different irradiance levels as well as finding the worst case condition of the shaded PV cell, the reverse mode curves of the shaded PV cell are mirrored into the forward mode region, as seen in Fig.1.16. The 2D depiction of Fig.1.14c is shown in Fig.1.16a, where the intersection points between the two curves indicate the turn on points of the PV module bypass diode. For instance, at 0 W/m^2 irradiance of the shaded cell, the bypass diode conducts at a string current of 0.25 A and a reverse voltage of 10.25 V (the shaded cell (PV1) voltage is -10.25 V), and when the shaded cell operates at 900 W/m^2, bypass conduction is at a shaded cell voltage of -8.75 V and a string current of 2.4 A. The worst case condition can be concluded from Fig.1.16, where G is restricted between 800 and 900 W/m^2 and an irradiance level of 875 W/m^2 causes the bypass diode conducting at the I_{MPP} of the fully illuminated cell (2.3 A). After the conduction point, the shaded cell dissipated power and its current remain constant, with further increase in the string current passes through the diode. If there is no bypass diode, the current and dissipated power of the shaded cell are sharply increased.

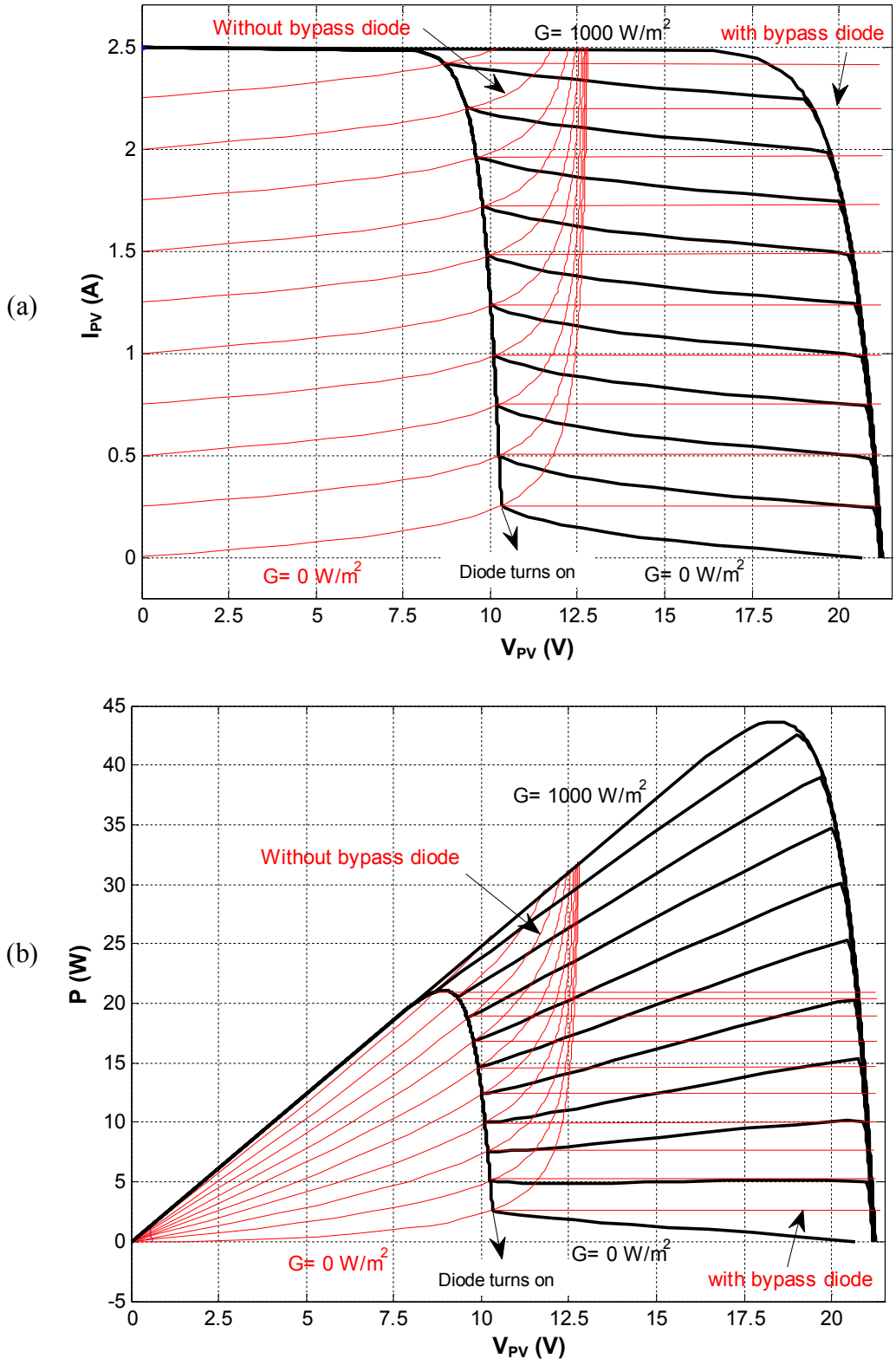


Fig.1.16: Two PV modules connected in series (one cell is shaded, the other cells are at 1000 W/m^2) (a) I-V curves and (b) power curves. The red curves show the mirrored reverse mode of the shaded cell.

Useful simulation results are depicted in Fig.1.17, illustrating the dissipated power of the shaded PV cells at the point which the bypass diode conducts. By using the circuit connection shown in Fig.1.13, when one PV cell (PV1) in PV module 2 is

shaded to 500 W/m^2, the dissipated power in the same cell reaches 14.64 W. With two shaded PV cells the dissipated power drops to 12.43 W (6.21 W for each PV cell). By increasing the shaded cells number the dissipated power gradually decreases, with the dissipated power for each shaded cell decreased considerably. More shaded cells means the dissipated power is divided between the shaded cells, so the hot spot effect is minimized. When the entire PV set (18 PV cells) is shaded, their dissipated power is small and almost equal to the power which is dissipated by the bypass diode.

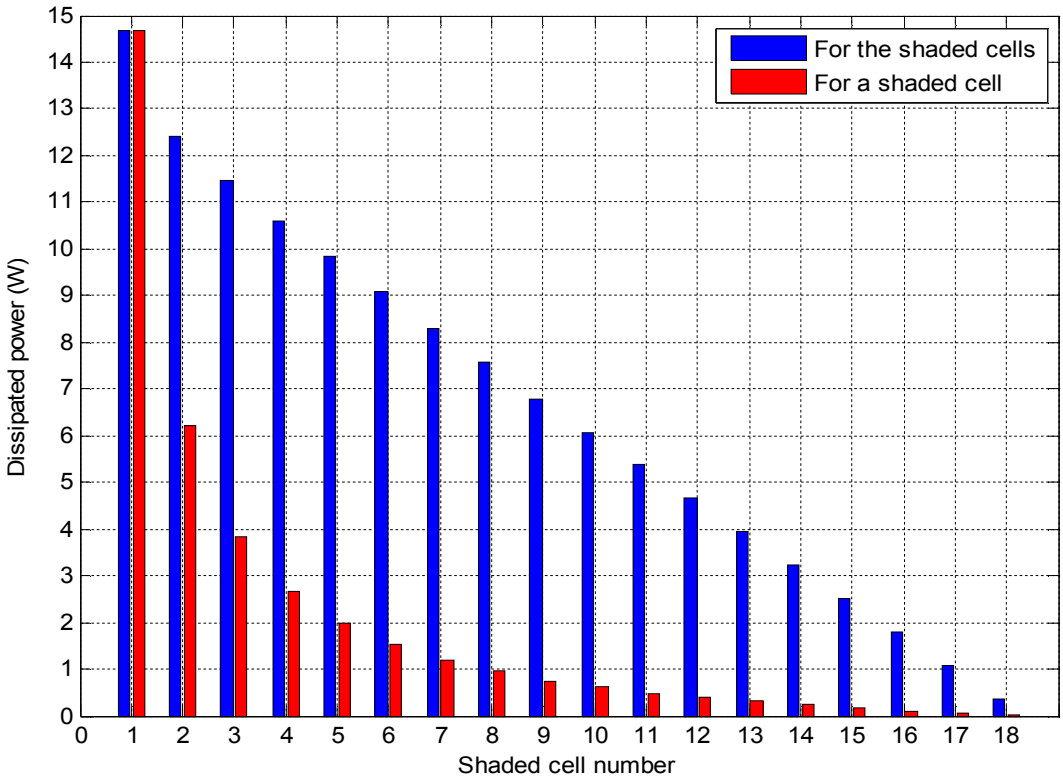


Fig.1.17: The effect of the shaded PV cell number on the dissipated power in two PV modules with bypass diodes, 1 to 18 cell PV are shaded at 500 W/m^2.

1.7 Solar Cell with Integral Bypass Diode Function

The previous figure illustrated that the worst situation is when only one PV cell of the bypassed PV module is shaded. The considerable amount of dissipated power (14.64 W) can be significantly reduced to the amount shown at 18 shaded cells (about 0.4 W), if a bypass diode is placed across the shaded PV cell so it can be bypassed individually without affecting the non-shaded PV cells. However, this requires allocating 18 discrete bypass diodes in the PV module in the given example and 36 diodes for PV modules which include 36 PV cells, so a large number of

diodes are employed in the case of a PV array. The only disadvantage is cost where such a method is too expensive to be implemented, not only with respect to the discrete diodes cost, but also for PV modules-panels-arrays manufacturing where many extra contacts have to be considered for the diodes to be placed [11, 21]. Another disadvantage compared with the modules equipped with bypass diodes can be highlighted here, where not only the voltage generated from the shaded PV cells is lost as a result of their bypass diodes are conducting, also a large negative voltage (shaded cells number × $V_{d(on)}$) is added to the string voltage causing a further voltage drop to the whole PV system.

In [22] an integral diode chip is designed to be attached to the back of the solar cell by soldering or thermal compression, so there is no need for the wiring of the discrete bypass diode. Integrating the bypass diode into the solar cell material during the PV cell manufacturing was presented in [21, 23], where both elements are incorporated into one device and isolated internally. Fig.1.18a shows a PV cell with a discrete bypass diode, while Fig.1.18b shows a PV cell with an integral bypass diode function included.

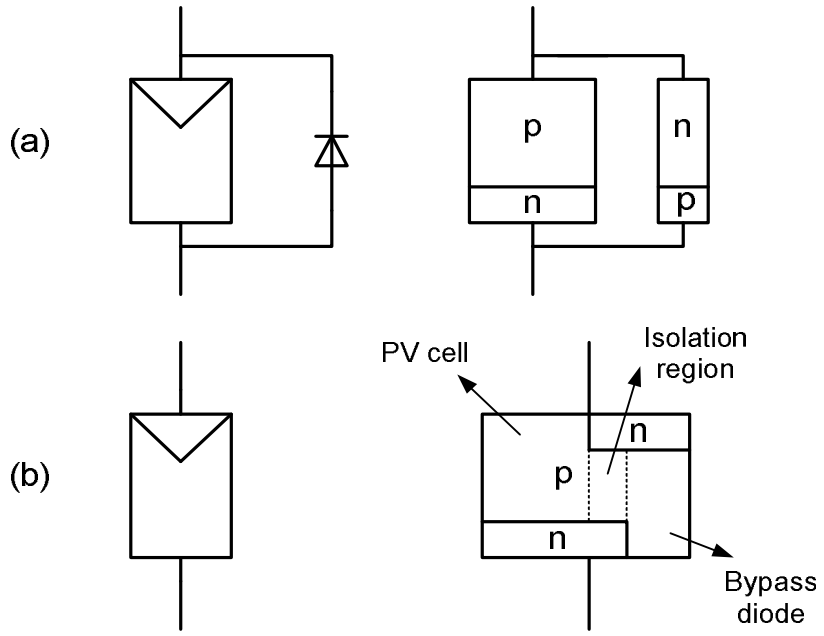


Fig.1.18: PV solar cell with (a) discrete bypass diode and (b) integrated bypass diode function.

Several disadvantages result from integrating the bypass diode into the solar cell, for instance, it adds parasitic shunt and series resistance. In addition to the dissipated power due to the parasitic shunt resistance, additional power is dissipated in the

parasitic series resistance when the bypass diode turns on. Also, some area of the cell substrate is allocated for the bypass diode and the isolation between the PV cell and the diode. Generally, the integral diode reduces the power generated by the PV cell [11, 21].

1.8 Problems and Challenges

In principle, for a given set of identical PV modules operating under the same ambient conditions with proper maximum power point control (MPPT), the maximum generated power should be nearly independent of the its configuration. However, due to non-uniform solar irradiation of PV panels, which causes electrical mismatching of the cells, the output power depends strongly on the way the PV sources are interconnected (PV configuration Fig.1.19) and also depends on the power converter system employed.

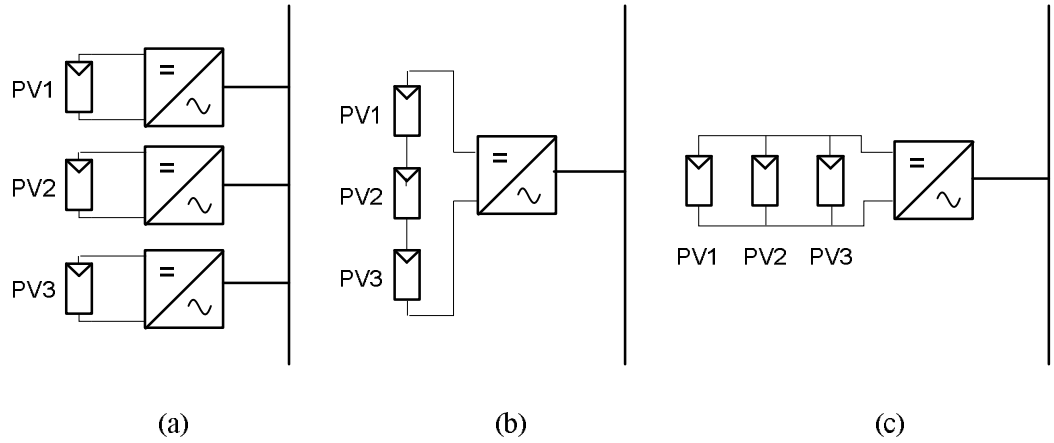


Fig.1.19: (a) modular, (b) series, and (c) parallel PV configuration

The PV configuration is directly related to the application requirements (current and voltage levels). Regarding applications which require the PV sources to be series connected to reach a high voltage, as a result of even one shaded PV source, the current through the series string is reduced, or voltage is decreased in the best case if bypass diodes are used, [24, 25]. Consequently the power generated by a PV system is reduced significantly. The challenges in this thesis is to maintain all the series connected PV sources operating at their maximum power (MPP) according to their irradiance level, as well as delivering that generated power completely to the load.

The required PV modular configuration is such that shaded PV sources do not affect the non-shaded PV sources in the system.

1.9 Thesis Aim and Objectives

The aim of this research is to develop a PV-converter structure and corresponding control scheme such that the maximum power generation of all PV modules in the system is obtained irrespective of the light patterns, partially shaded or not. To achieve this, the following specific objectives are set:

1. Study PV principles and implement the most suitable simulation models. Clarify the PV partial shading problem of series connected PV sources and its effects. Highlight the PV source reverse mode of operation and the incorporation of bypass diode protection;
2. Explore and compare the existing methods to deal with the problem of the PV partial shading including the use of multilevel inverters, as well as highlighting their limitations;
3. Introduce a method to overcome the PV partial shading problem based on multilevel inverters, along with the necessary control algorithms;
4. Investigate and compare different multilevel inverter switching techniques as well as developing a generalized algorithm for any inverter level. Simulation and experimental verification are to support the findings;
5. Examine and compare the common maximum power point tracking (MPPT) systems and algorithms, which are an essential part of any PV system. Highlight their disadvantages and improve a MPPT algorithm to overcome the limitations. Support the investigation and introduced a solution with simulation and experimentation;
6. Integrate the multilevel converter into a PV system, simulate and model the whole multilevel PV system under symmetrical irradiance levels;
7. Implement a complete PV system mathematically and experimentally, including the necessary control algorithms, in order to overcome the PV

partial shading problem. Analyse the achieved results and attempt to improve the output quality.

1.10 Structure of the Thesis

Chapter 1 clarifies the PV partial shading problem and its effects along with the required simulations which specifically highlight the PV source reverse mode of operation and the bypass diode protection.

Chapter 2 investigates and compare the existing solutions for overcoming the PV partial shading problem. Their limitations are also clarified.

Chapter 3 introduces a PV system which is based on a multilevel DC-link inverter to deal with the PV partial shading issue. The circuit principles of operation are presented. Study various multilevel inverter switching techniques and simulate some of them for comparative purposes, as well as introducing a generalized algorithm for implementing Integration-Duty Cycle PWM (IPWM).

Chapter 4 includes study and analysis of the common maximum power point tracking (MPPT) systems and algorithms in order to clarify their limitations and advantages. Also, improvement of the P&O MPPT algorithm is presented along with simulation studies. For comparison purpose, three popular MPPT algorithms are applied to a buck converter model, with gradual and abrupt irradiance changes.

Chapter 5 describes the integration of the chosen multilevel converter (DC-link inverter) into a PV system, where modelling by using state space averaging (SSA) and simulation via Matlab-Simulink of the whole multilevel PV system under even and uneven irradiance levels are presented. Also, the chapter introduces the necessary control algorithms to deal with partial shading conditions and to improve the output quality. The simulation results are presented for five, seven, nine, and eleven level DC-link inverters.

Chapter 6 presents the design and implementation requirements of the experimental systems of five and seven level DC-link inverters together with DC-DC buck converter system. The digital processor eZdsp^{TM} F28335 is used to control the PV systems in a real time mode of operation, and Matlab-Simulink Real Time Data Exchange (RTDX) is employed to display the extracted power and to control the

system parameters via a designed Graphical User Interface (GUI) window. Also, the necessary lighting and I-V curve display circuit for the PV modules are presented.

Chapter 7 presents and analyses the achieved results of the maximum power point algorithms, generalized multilevel IPWM, and the two/three input PV modules DC-link inverters under partial shading conditions along with the improved results. The required analyses for comparison purposes are presented. The required tests of the lighting and the PV modules are presented along with their results.

Chapter 8 concludes the thesis and summarises the accomplishments and contributions presented in the research. Recommendations for future research are also included.

1.11 Summary

This chapter gave an introduction to the partial shading of PV sources connected in series. The effects caused by partial shading such as hot spot and power reduction were investigated in detail along with the bypass diode protection and the worst case condition. The necessary simulation results, which highlight the cell reverse mode and the effects of the PV cell shunt resistance as well as the effects of the shaded cell number, were presented under different levels of irradiance. Thesis aim and objectives as well as the thesis structure were presented.

Chapter 2

PV Partial Shading - the Existing Solutions

As discussed in Chapter 1 the conventional way to reduce the damaging effects of PV partial shading is to use bypass diodes. However, this causes the power which could be yielded from the bypassed shaded PV sources to be completely lost. The application of power electronic converters can solve this problem. The idea is to use power converters to control the shaded PV panels so that they still operate at their maximum power points together with the non-shaded cells. Consequently there is no power reduction at the output as no shaded sources are being bypassed.

A number of methods have been introduced for such a scheme with a common approach based on avoiding the direct connection of individual PV sources. For instance, establishing a series string of PV sources, with one power converter allocated to each of them, enables independent control of each source.

This chapter gives a review of the major existing schemes which use power converters to overcome the problem of partial shading. These schemes are evaluated and compared according to how close operation is to the maximum power point of each PV source in the system.

2.1 PV Configuration

As known, the PV configuration is how the PV panels are connected to each other, and, as mentioned in section 1.8, the amount of generated power under the partial shading condition is strongly related to this. Apart from the voltage and current levels, all the PV configurations should ideally enable individual PV panels (assuming identical) to generate the same amount of power under uniform irradiance. Fig.1.19 shows three basic PV configurations where the modular configuration is the least affected by the partial shading, followed by the parallel and the series configurations.

Other PV configurations were introduced in order to improve the generated power under partial shading situations. Such configurations can be applied to the PV cells to form PV modules or on a large scale where applied to the PV arrays to form PV farms. Fig.2.1a shows the Series-Parallel (SP) configuration where series strings of PV sources are connected in parallel. The Total-Cross-Tied (TCT) configuration is similar to the SP configuration but with ties to form several rows of equal voltage PV sources as shown in Fig.2.1b. The Bridge-Linked (BL) configuration is illustrated in Fig.2.1c where the PV sources are connected in a bridge rectifier fashion [26].

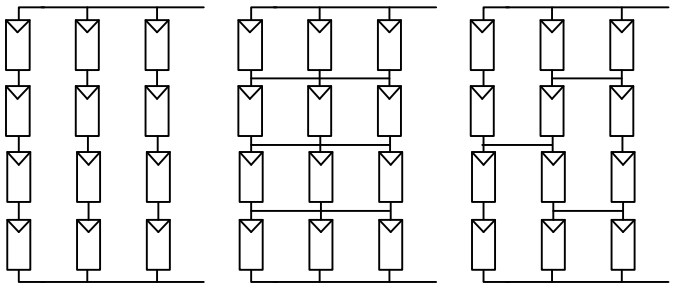


Fig.2.1: (a) SP, (b) TCT, and (c) BL PV configuration.

A comparison has been made in [27] between the three configurations with respect to how they are affected by partial shading. The BL configuration showed lower power reduction than the TCT and SP configurations. The BL and TCT configurations gave similar results and these are far better than the SP configuration.

2.2 PV Switching-Matrix Reconfiguration System

Another approach to deal with the PV partial shading problem was introduced in [24] and implemented experimentally in [28]. The PV sources are connected to a switching matrix, as shown in Fig.2.2a, in order to keep reconnecting them into a series of rows (clusters). Each cluster consists of several PV sources connected in parallel as shown in Fig.2.2b, the configuration is similar to TCT presented in the previous sub-section. The reconnection of the PV sources is according to their irradiance levels, so all established clusters have to generate equal amounts of power (equalization concept).

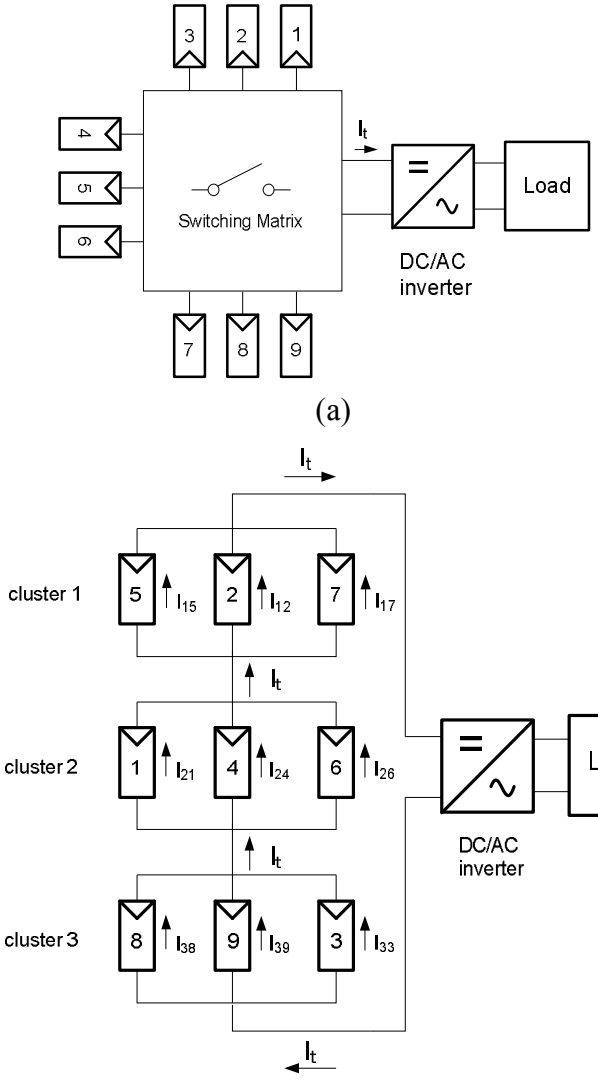


Fig.2.2: PV switching matrix-connected (a) simple circuit diagram and (b) PV modules configuration.

Although tests have shown that this approach results in producing more power than the directly connection of PV sources, it is not always possible to find clusters of equal extracted power. Consequently the cluster which generates the lowest power will be bypassed completely, causing further power dissipation. Also, each cluster includes PV sources under different irradiance levels, so only the PV sources with the highest voltage generates power while other sources in the cluster are reverse biased.

2.3 Single PV-Cell DC-DC Converter Module

A PV module consisting of 18 cells has been emulated in [29] by a single PV cell with an integrated DC-DC boost converter. Fig.2.3a illustrates the PV system which involves the 18 cell module and Fig.2.3b shows the proposed single cell system. The latter relies on an external start-up voltage source for converter switching control, it then boosts the output voltage to the required level. The results showed large differences between the two systems with respect to the consequences of the partial shading conditions. The 18 cell module is affected as described in chapter.1, where one shaded PV cell inhibits the power generated by the entire module. However, the power generated by the single-cell system is approximately proportional to the non-shaded area of the PV cell.

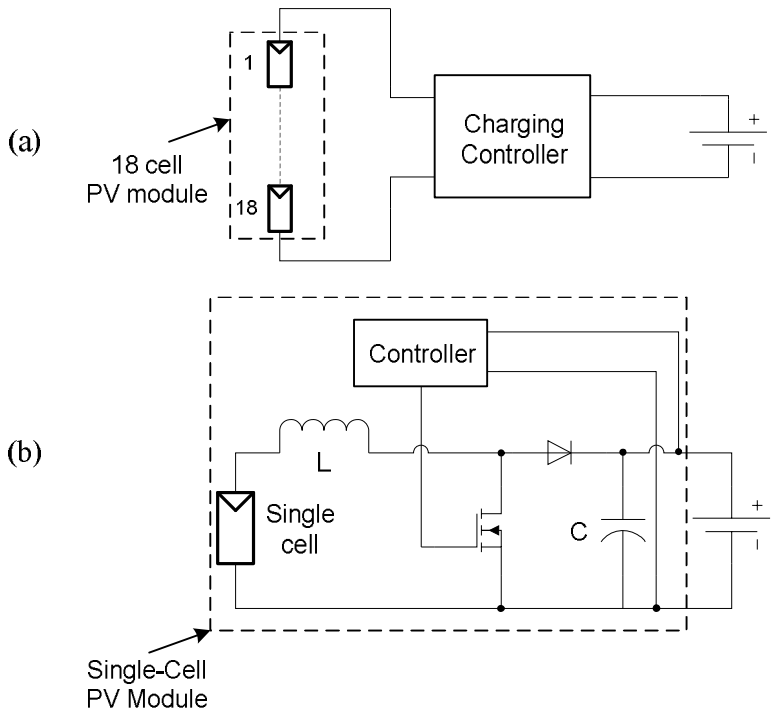


Fig.2.3: Circuit diagram of (a) PV module and (b) single-cell PV module.

In the start up mode, a starting up circuit is used to drive the MOSFET initially by converting the PV cell voltage (0.3 V) to a voltage which is suitable for gate driving. Then, the output voltage of the boost converter is increased and replaces the cell voltage to drive and control the MOSFET via the controller shown in Fig.2.3b.

The single-cell PV module can be a solution for low voltage applications which require the PV module voltage. However, in the case of a desired voltage geater than

is generated by a single-cell PV module, several single-cell PV modules have to be connected in series as described in the next section.

2.4 Series Connected PV DC/DC Converter Modular System

In [25] and [19], the series PV source connection is established via the DC/DC converters, enabling each PV power output to be maximized separately. Fig.2.4 shows how series-connected module-integrated DC/DC converters can be connected to a centralised DC/AC inverter [25]. The same PV configuration was developed in [19] as an intelligent PV modular system where each PV module has an individual DC/DC boost converter employing the MPPT algorithm.

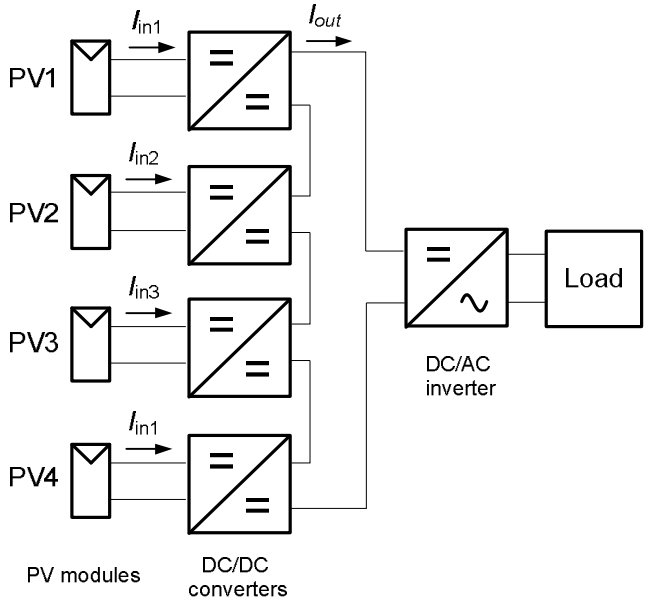


Fig.2.4: PV DC/DC converters series connection.

According to the light levels on the PV sources and the switching duty ratio D, each DC/DC converter has different input and output current I_{in} and I_{out}. In the mentioned modular PV system, if the DC/DC converters are considered to be boost converters, during the continuous conduction mode the relationship $I_{out}= (1- D)\ I_{in}$ will be satisfied. Even though the DC/DC converters in the system shown in Fig.2.4 have different input currents, their output currents have to be equal due to the series output connection. The duty ratio control can compensate the current drop of a shaded source but may not enable it to operate at its MPP. This is because the control of the DC/DC converter is only functional within a restricted range of irradiation drop, below which the current of the shaded source becomes too low.

Duty ratio D cannot be reduced further to maintain I_{out} at the same level as that generated by other non-shaded sources. So if the irradiation is reduced below the minimum level, then the shaded source has to be bypassed to allow the non-shaded sources to operate at the MPP. Thus the PV DC/DC converter modular system cannot keep all PV sources in the series connection operating at their MPP under partial shading conditions [19, 25].

2.5 General Control Circuit (GCC) PV system

Another approach is based on the principle of bypassing the power through converters and is called "Generation Control Circuit" (GCC) scheme introduced by Shimizu et al. [4].

The rationale of this scheme is as shown in Fig.2.5a, where each PV source in this system is represented by a current source. Assume two series connected PV sources are perfectly matched and their short circuit current value under 100% illumination is 5 A. Assume the irradiance on PV2 is reduced to 40%, the PV2 short circuit current drops to about 2 A. As PV1 is generating 5 A its surplus 3 A has to pass through the bypass diode. Though this enables PV1 to operate according to the level of its irradiance which is higher, while preventing PV2 from being damaged, PV2 cannot produce any power due to V_{PV2} being equal to zero. In order to overcome this shortcoming, GCC provides the means to bypass the surplus current while maintaining the operating voltage V_{PV2}, non-zero as illustrated in Fig.2.5b.

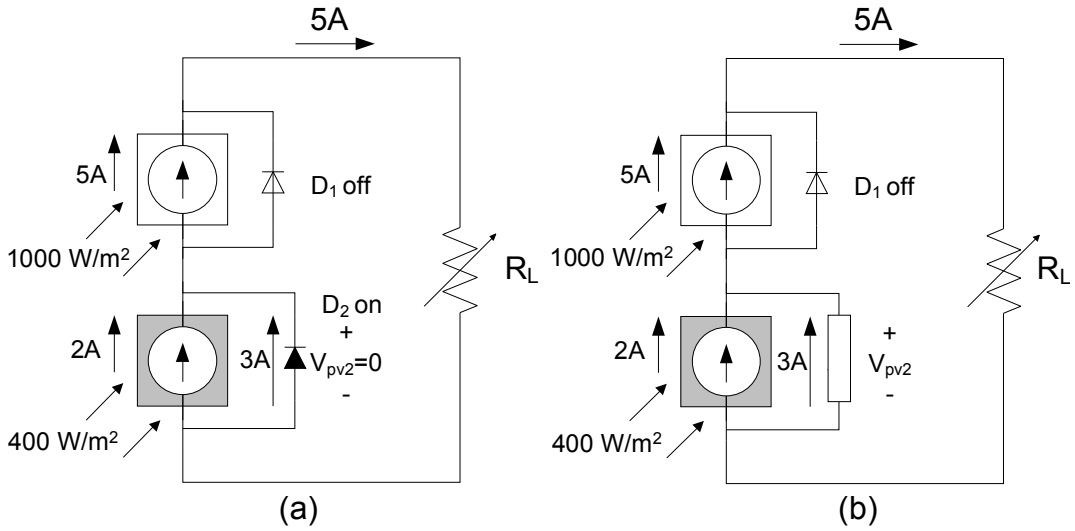


Fig.2.5: Two PV panels represented as current sources connected in series.

2.5.1 GCC DC/DC Converter PV System

In this scheme a bidirectional concept is applied as illustrated in Fig.2.6a. By using power feedback, a DC voltage can be established across each PV source terminals. This voltage source has the ability to pass the surplus current while maintaining the PV module voltage at the required value. In other words, the approach is based on diverting a fraction of the total extracted power into a controlled converter (DC/DC) which supports and maintains the operation of the shaded PV source at its MPP. The method is proposed in [4] only as a concept with the suggested circuit diagram illustrated in Fig.2.6b.

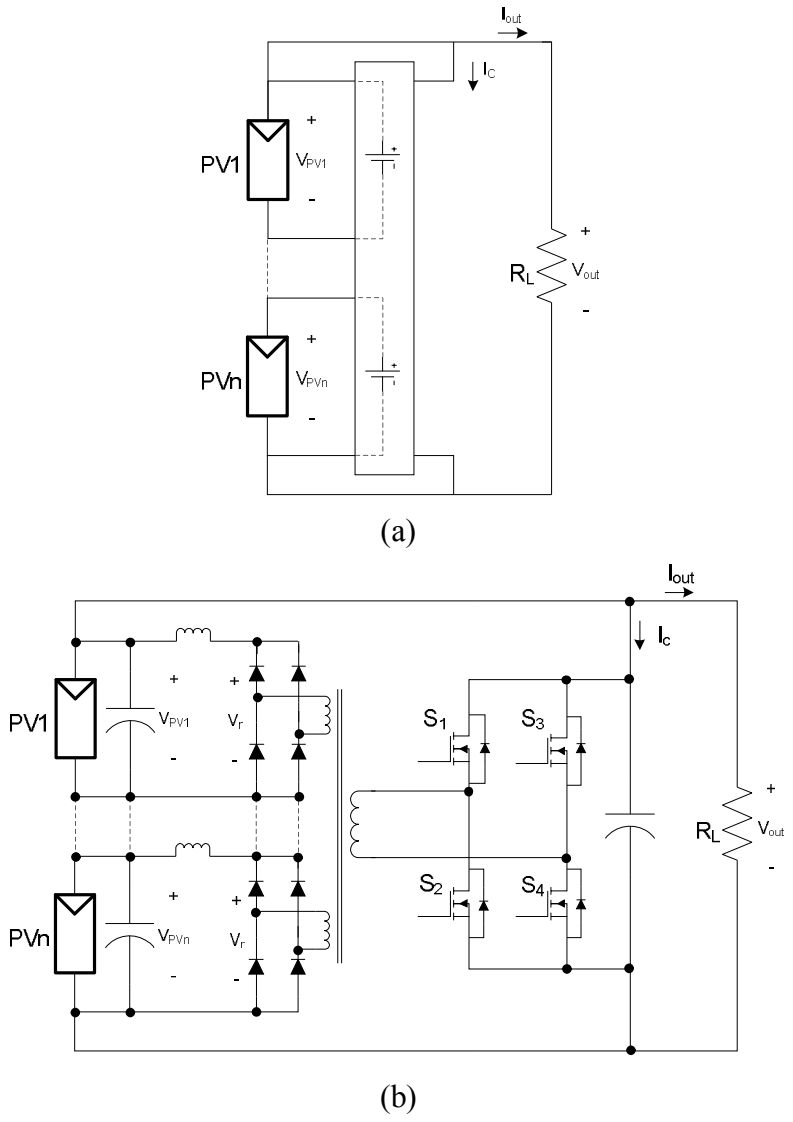


Fig.2.6: GCC DC/DC (a) principle circuit and (b) circuit diagram.

As can be seen on the right-hand side of Fig.2.6b, the DC output voltage is converted to an AC square wave voltage using a full-bridge two-level DC-AC inverter. In order to establish variable DC voltages across the PV sources on the left-hand side of the

circuit, the inverter has to be controlled to generate a variable amplitude AC voltage. A multi-output transformer has to be used in order to achieve isolated AC voltages and, finally, uncontrolled rectifiers are employed to convert the AC voltage to multiple DC voltages V_r according to the number of PV sources. However, there is a limitation; the final conversion stage is not controllable and as a result each PV source cannot operate at its MPP during shading conditions.

The same concept was implemented in [5], but with a fly-back converter allocated to each PV source so the above mentioned drawback is overcome. Fig.2.7 illustrates the circuit which produces variable DC voltages across the PV sources by controlling the switches S1 to Sn.

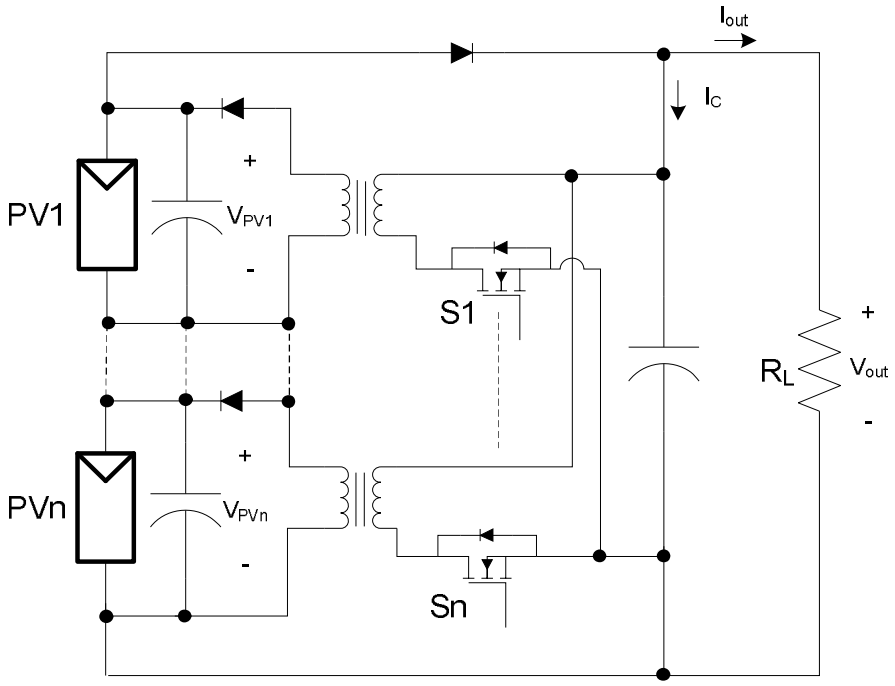


Fig.2.7: DC/DC flyback converter.

Each flyback converter is controlled individually, so the desired MPP voltage can be accomplished for the shaded sources. With respect to the non-shaded sources the related flyback converters are in an off state. Also, for more flexibility another power converter has to be considered at the output load stage for achieving MPPT.

Although the GCC DC/DC Converter scheme can keep each PV source operating at its MPP under partial shading conditions, such an approach degrades the system efficiency because of the power feedback where not all the generated current passes to the load.

2.5.2 GCC Multi-Chopper PV system

In an alternative GCC, also presented in [4], the method is based on the multistage buck-boost converter circuit in order to control the extracted power from the PV sources. Compared with the last topology, the total extracted power is delivered to the load. As can be seen in Fig.2.8a, there is no feedback involved in establishing the required voltages across the shaded PV sources. Fig.2.8b shows the circuit diagram of the GCC multi chopper.

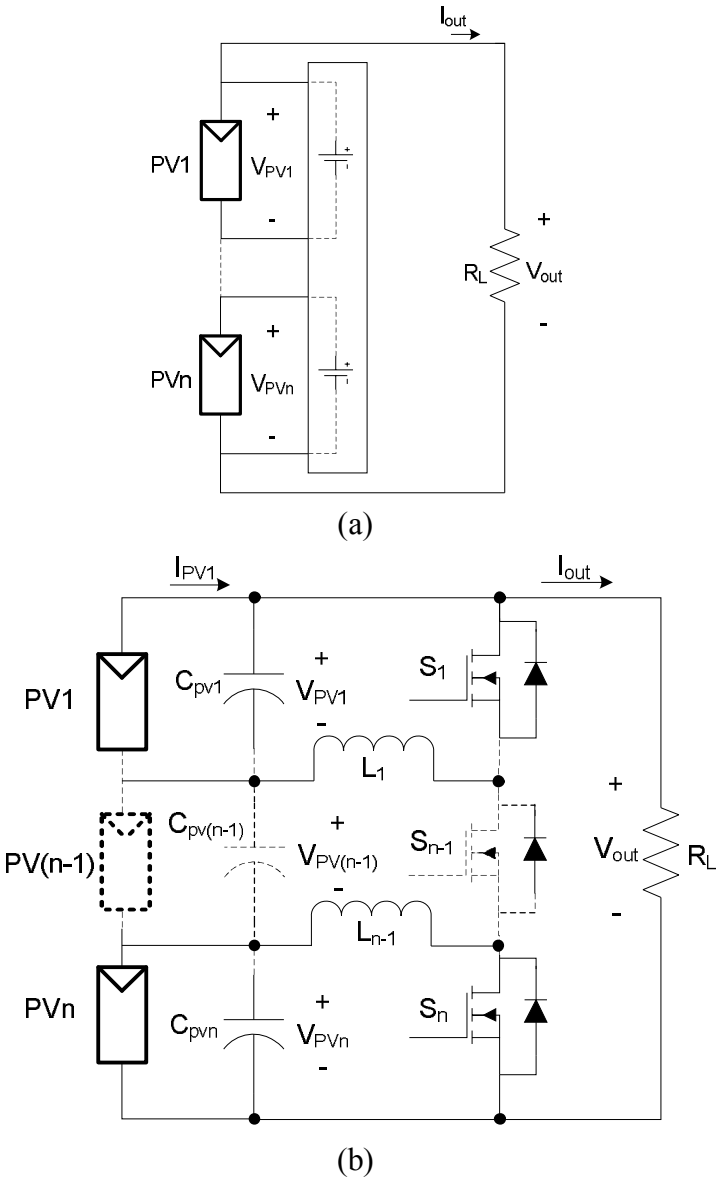


Fig.2.8: GCC multi-chopper PV System (a) principle circuit and (b) circuit.

Fig.2.9a shows the GCC of two PV panels where PV2 is shaded. The waveforms of the switches' control signals as well as the inductor current are shown in Fig.2.9b. When S1 is switched on the surplus current resulting from irradiance difference

between PV1 and PV2 can pass through the inductor while the PV1 voltage will appear across the inductor itself.

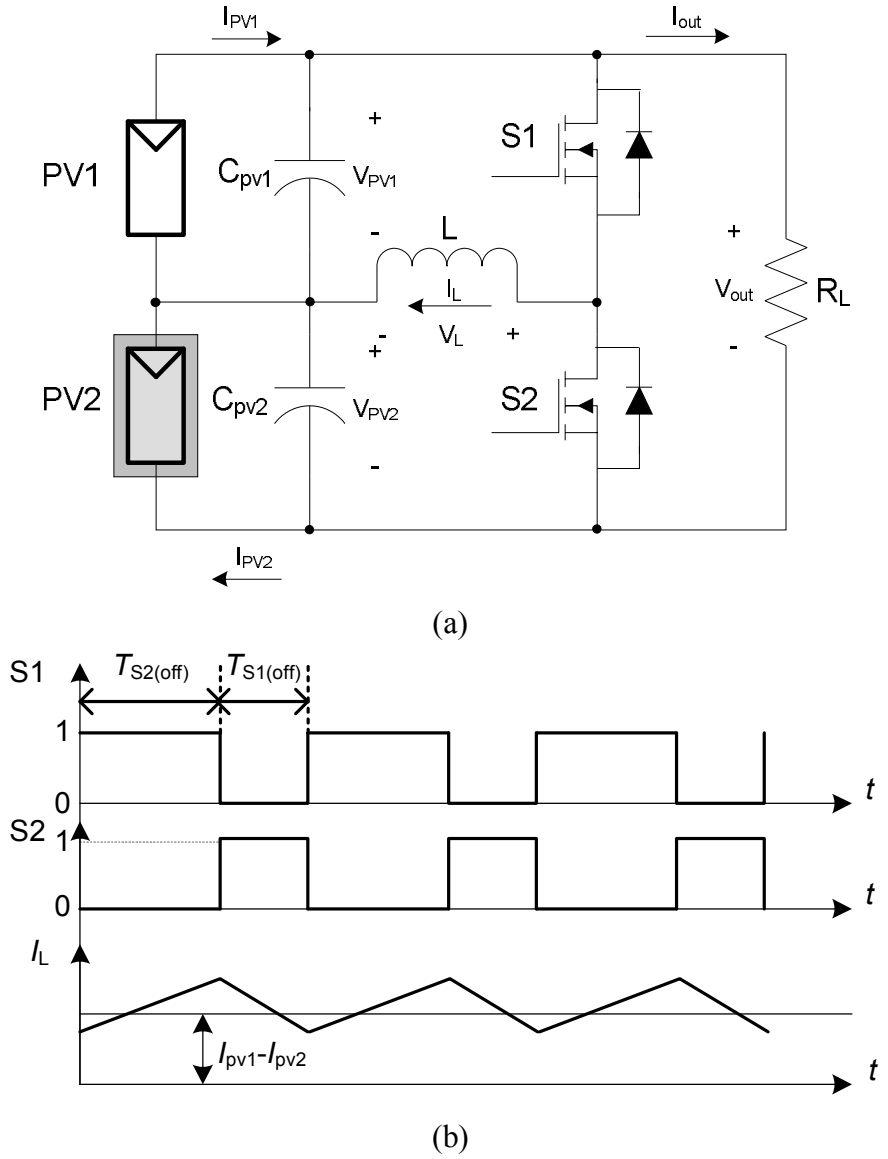


Fig.2.9: Two PV sources GCC multi chopper (a) circuit diagram and (b) switches control and the inductor current waveforms.

Although, in the original paper, it stated that S1 and S2 have to be switched continually in a complementary manner, in fact the switching mechanism is different from what is shown. If the shading situation in Fig.2.9a is considered, only S1 has to be switched on and off whereas the freewheeling diode for S2 will be on if S1 is in the off state in order to conduct the surplus current via the inductor. The only case that S2 can be on is when the synchronous rectification is considered, so the conduction losses of D2 are reduced. The output voltage is always equal to the

algebraic summation of V_{PV1} and V_{PV2}. Equations 2.1 and 2.2 show the general equations to calculate the output current and power for n PV sources [4, 18].

$$I_{out} = \sum_{k=1}^{n} \overline{D}_k I_k \qquad \text{…….. (2.1)}$$

$$P_{out} = \sum_{k=1}^{n} V_k I_k \qquad \text{…….. (2.2)}$$

where $\overline{D} = 1 - D$, $\sum_{k=1}^{n} \overline{D}_k = 1$, and $\overline{D}_1 : \overline{D}_2 : .... : \overline{D}_n = V_1 : V_2 : ..... : V_n$

It is noticeable that at each time there is only one switch in off state while the other switches are bypassed by free-wheeling diodes, so there is a restriction on the non-conduction intervals of other switches. Accordingly each PV source cannot be controlled completely independently without affecting the other PV sources in the circuit. Consequently, finding the MPP of one of the PV sources does not mean the other PV sources are operated at their MPP and therefore an optimal duty ratio has to be found in order to achieve the largest possible power at the load. For more than two PV sources, finding an optimal operation point cannot be done directly using well known MPPT algorithms, and so development of a new method to reach the MPP via tracking only the load power is required.

Overall, each additional PV source causes more complexity, and even though making all the utilized PV sources operate at their MPPs is not possible, all of them generate power and no bypass occurs. Another drawback can be deduced here; if there are no shading cases, the GCC cannot be exploited to reach the operating MPP of the system so another converter stage has to be employed to perform this task. The same principle was introduced in [30], but with a buck-boost, Cuk, or flyback converter allocated for each adjacent pair of the series connected PV sources, bidirectional concept, to bypass power between the PV sources of uneven irradiance.

To confirm the claim that the PV sources do not operate at their individual MPPs at the same time, the simulation results, which were produced by the State Space Averaging (SSA) model of two PV sources operating under the scheme of Fig.2.9a, were simulated. The circuit on/off states illustrated in Fig.2.10a and 2.10b were used to derive the GCC mathematical model which is described by equations 2.3 and 2.4 according to [31].

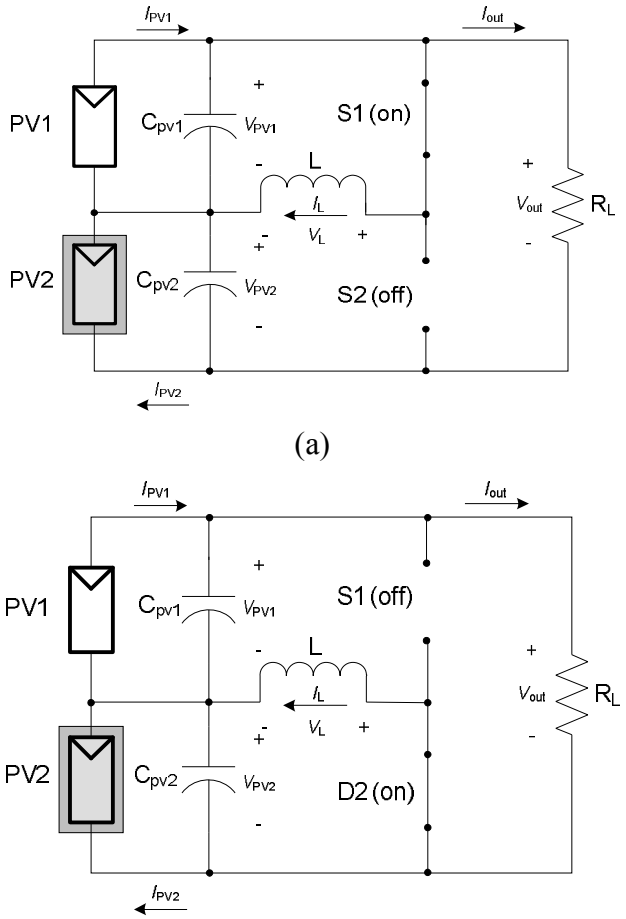


Fig.2.10: Two sources GCC multi stage chopper (a) on state (within *D* time period) and (b) off state (within 1-*D* time period).

$$\begin{bmatrix} \frac{dv_{pv1}}{dt} \\ \frac{dv_{pv2}}{dt} \\ \frac{di_L}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-1}{C_{pv1}R_L} & \frac{-1}{C_{pv1}R_L} & \frac{-D}{C_{pv1}} \\ \frac{-1}{C_{pv2}R_L} & \frac{-1}{C_{pv2}R_L} & \frac{1-D}{C_{pv2}} \\ \frac{D}{L} & -\frac{1-D}{L} & 0 \end{bmatrix} \begin{bmatrix} v_{pv1} \\ v_{pv2} \\ i_L \end{bmatrix} + \begin{bmatrix} \frac{1}{C_{pv1}} & 0 \\ 0 & \frac{1}{C_{pv2}} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i_{pv1} \\ i_{pv2} \end{bmatrix} \quad \ldots\ldots (2.3)$$

$$[v_{out}] = [1 \quad 1 \quad 0] \begin{bmatrix} v_{pv1} \\ v_{pv2} \\ i_L \end{bmatrix} + [0 \quad 0] \begin{bmatrix} i_{pv1} \\ i_{pv2} \end{bmatrix} \quad \ldots\ldots (2.4)$$

As can be seen in Fig.2.11, both PV sources cannot be operated at their MPPs at the same time. The signs × and + indicate to the operating points of the PV sources at switching duty ratios of 0.38 and 0.76 respectively, where the PV sources' MPPs were obtained accordingly. The applied system parameters are listed in Table 2.1 and the achieved results are given in Tables 2.2a and 2.2b.

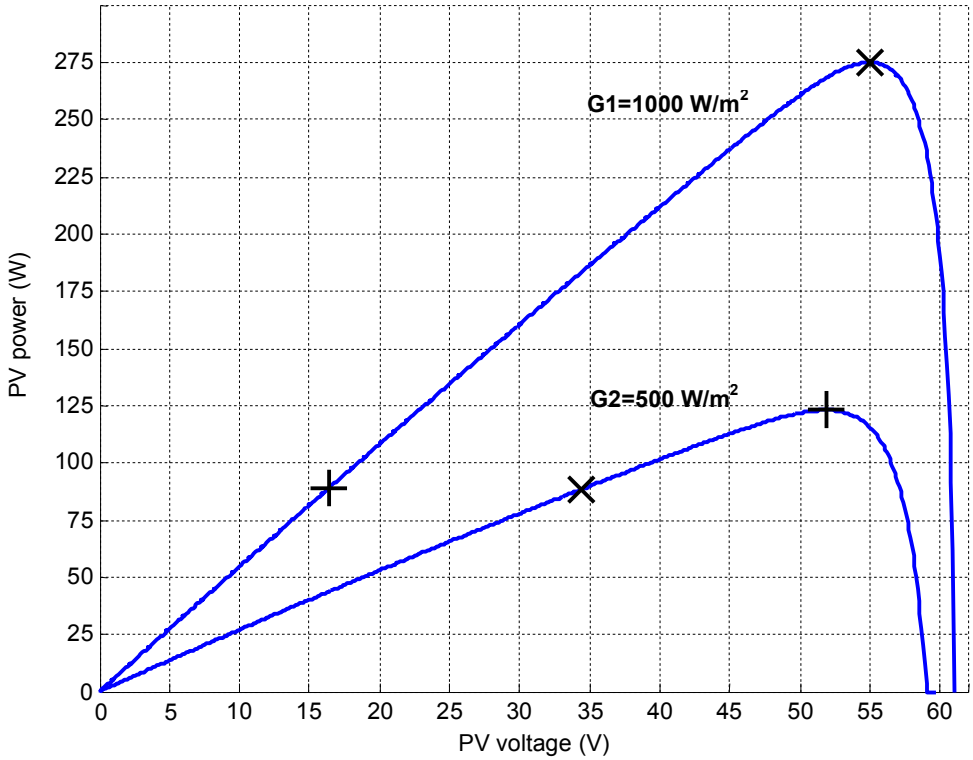


Fig.2.11: GCC operating points under different switching duty ratio ((×) is at D=0.38 and (+) is at D=0.76).

TABLE 2.1: GCC Multi Shopper System Parameters

V_{oc}	61 V	$C_{pv1,2}$	470 µF	$G1$	1000 W/m^2
I_{sc}	5.5 A	R_L	22 Ω	$G2$	500 W/m^2
V_{mpp}	55 V	L	2 mH		

TABLE 2.2a: The GCC Results at D=0.38

P_{PV1}	275 W	V_{pv1}	55 V	I_{pv1}	5 A
P_{PV2}	88.43 W	V_{pv2}	34.43 V	I_{pv2}	2.56 A
I_L	2.43 A	I_{out}	4.06 A	V_{out}	89.42 V

TABLE 2.2b: The GCC results at D=0.76

P_{PV1}	88.89 W	V_{pv1}	16.39 V	I_{pv1}	5.42 A
P_{PV2}	123 W	V_{pv2}	51.89 V	I_{pv2}	2.37 A
I_L	3.05 A	I_{out}	3.10 A	V_{out}	68.28 V

For the light conditions, Fig.2.12a shows the output power waveforms for each PV module and the sum, which are plotted against different switching duty ratios. The

circuit currents and voltages as a function of the switching duty ratio are illustrated in Figures 2.12b and 2.12c respectively.

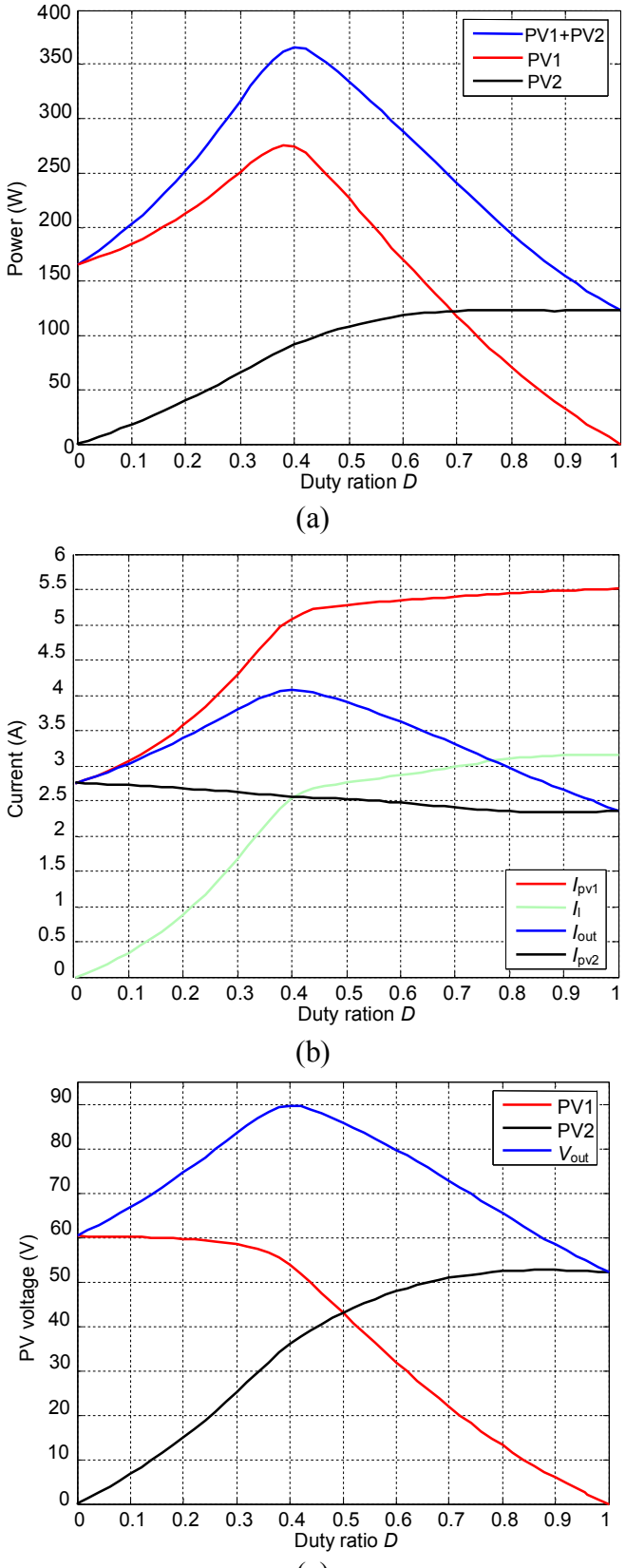


Fig.2.12: GCC (a) power, (b) current, and (c) voltage waveforms as a function of duty ratio.

2.6 Retrofit PV System

The retrofit circuit is based on combining several GCC multi-chopper circuits together to form one system. Fig.2.13 shows one such system where the GCC circuits are connected in series and in parallel [32]. This circuit was not designed properly to overcome the partial shading problem, it is only a modification of the circuit that was introduced in [4] without any improvements or benefits. Also, it cannot be implemented experimentally as will be illustrated.

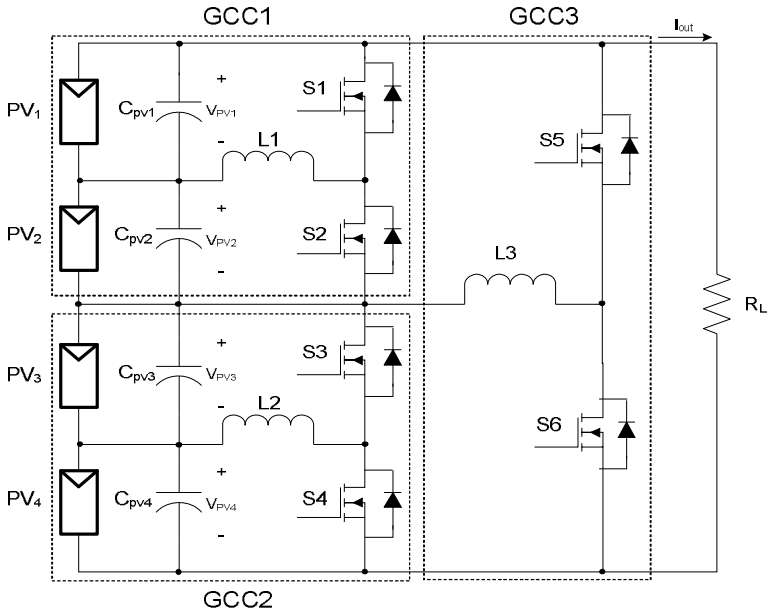
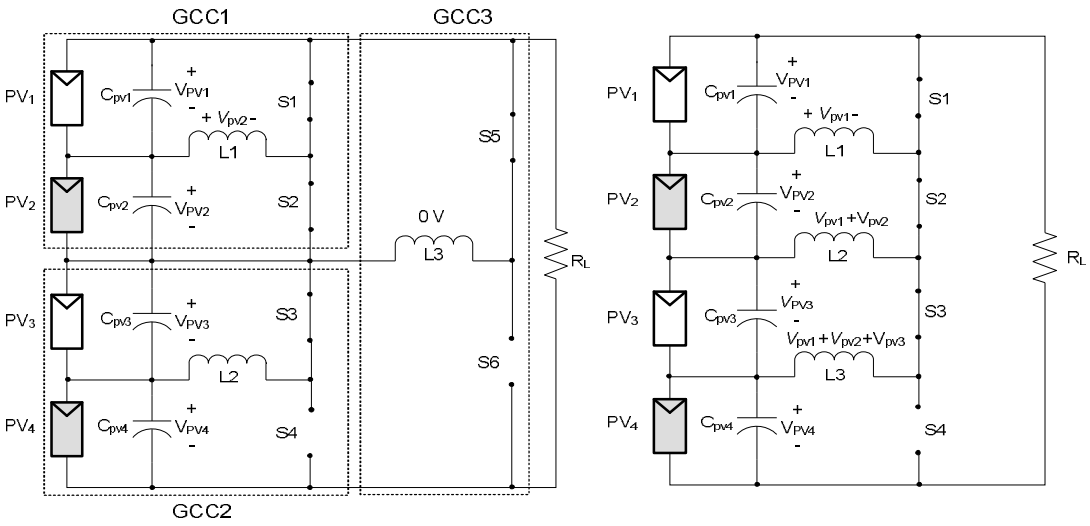


Fig.2.13: Retrofit PV system.

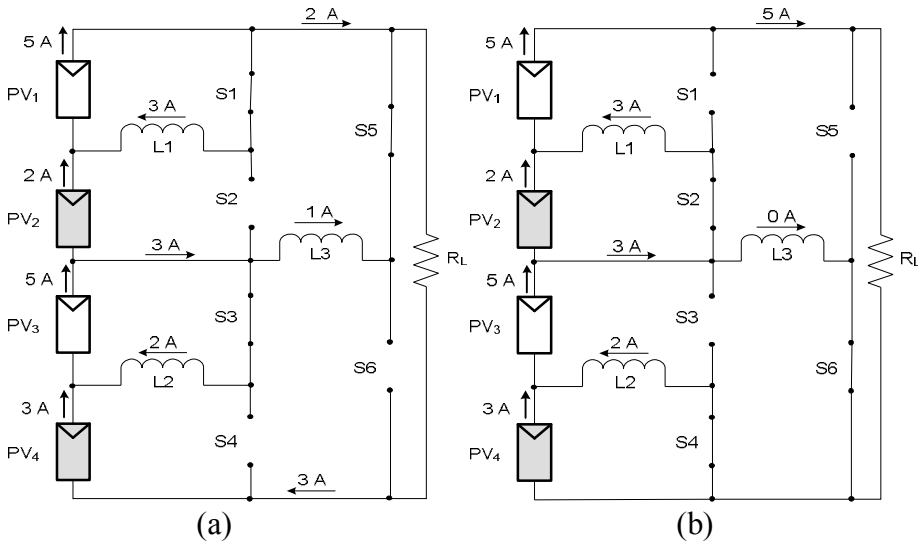
The first problem that can be noticed here is that there is no inductor placed between GCC1 and GCC2 and so according to the GCC control method, if S1 or S2 is off, PV3, PV4, and L3 are bypassed, and if S3 or S4 is off, PV1 and PV2 are bypassed. Also, that might cause problem due to the inductor current. Fig.2.14a and Fig.2.14b illustrate the Retrofit circuit comparing with the GCC multi chopper under one switching state of the control described in section 2.5.



(a) (b)

Fig.2.14: (a) Retrofit and (b) GCC PV system under switching state applied in [4].

As can be seen in Fig.15, other switching states cannot be applied making the implementation of the Retrofit circuit impossible, where the current of L1 and L2 are constant which are the surplus currents between the PV sources. However the current through L3 would be forced to be zero as in Fig.15b not 1 A, the sudden drop of current through the inductor will cause damage to the circuit due to a large increase in the voltage across the inductor.



(a) (b)

Fig.2.15: Retrofit circuit in different switching states.

2.7 PV Multilevel Inverter System

Multilevel converter is the answer to reduce the limitations in the power electronics applications of power rating, switching frequency, and the unwanted harmonics. Nowadays, the multilevel concept is employed in many power applications where high voltage rating, speed and quality are required. The multilevel inverter is mainly based on multi input voltage levels which can be achieved by series connection of voltage sources or capacitors and series connection of self-controlled switches. Due to this structure many advantages can be accomplished over conventional converters. In order to use lower voltage rating switches, switching frequency and achieving higher output quality, more levels can be used. The interpretation of this concept is basically the result of sharing the applied voltage and the switching frequency between the used switches. Also, low harmonic distortion is a consequence of a staircase output voltage which is close to a sine wave.

However, the penalty of using multilevel converters can be summarized as follows, firstly, with each additional level more hardware is required, so the cost is increased gradually. Secondly, unbalanced capacitor voltages, especially in neutral-point clamped and flying-capacitor inverters, might lead to exceeding the rating blocking voltage of some switches and more output harmonic distortion as well. Finally, sophisticated switching algorithms and control are required [33-37].

In addition to the mentioned features, the modular circuit construction of multilevel inverters enables each PV source power to be controlled individually by assigning a MPPT algorithm to each PV source. Consequently, the multilevel inverter can be used to generate high quality controlled AC output voltage while maintaining the input PV sources operating at their MPP under partial shading conditions.

2.7.1 PV Multilevel Inverter Topologies

Irrespective of their use in PV applications, multilevel inverters can be classified as single-source and multi-source multilevel inverters. The common multilevel inverters are shown in Fig.2.16, the first category are Neutral Point Clamped (NPC) Fig.2.16a1 [1], Flying-Capacitor Fig.2.16a2 [38], and NPC with bidirectional switch inverters Fig.2.16a3 [39]. They employ capacitors connected in series (capacitor cells) in order to be operated as equal voltage sources at the inverter input DC side.

The established voltages across the capacitor cells mainly depend on a single input DC source. The disadvantage with this category is the capacitor voltage balancing issue where zero neutral point has to be achieved. With respect to the multilevel PV applications, the capacitor cells are replaced with individual PV sources as illustrated in Fig.2.16.

On the other hand, the second category such as cascaded H-bridge Fig.2.16b1 [20] and multiple-source DC-link inverters Fig.2.16b2 [40] require individual DC sources to be used at the inverter input. As a negative point, the second inverter category does not include a neutral point, so in case of PV transformerless grid-connected applications the surface to ground capacitance current (common mode current), which can affect both equipment and people, cannot be reduced [36]. Fig.2.16c illustrates the general multilevel waveform of the output voltage.

The use of multilevel inverters for PV systems has been reported in various publications. Figure 2.16 gives several examples. Regarding the basic full bridge NPC PV inverter with two PV sources, each inverter leg involves four switches in addition to two diodes which are allocated to find a current path in the case of the zero output voltage level. Another topology shown is the NPC converter with a bidirectional switch PV inverter, which is a development inverter circuit of the conventional NPC inverter. It includes an H-bridge circuit and a bidirectional switch circuit (Fig.2.16a3).

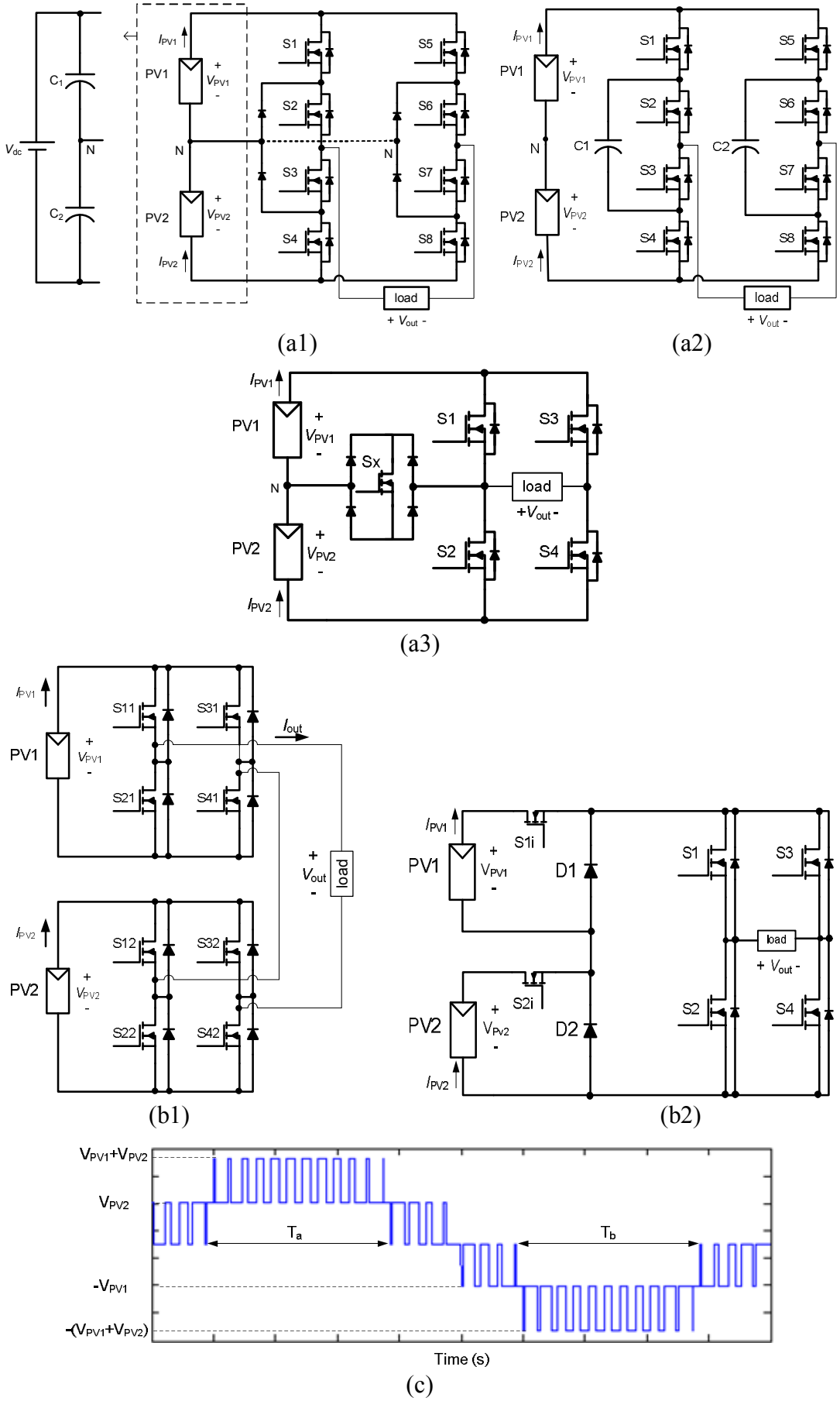


Fig.2.16: Multilevel inverters (a) powered via a single DC source, (b) multiple input DC sources, and (c) a multilevel PWM output voltage waveform.

The bidirectional switch circuit includes one switch and four diodes in order to conduct the current in both directions. Unlike the NPC inverter, the flying capacitor inverter uses floating capacitors to clamp the voltage. Each inverter leg includes four switches in addition to one flying capacitor which is charged to the voltage of a PV source. Regarding the cascaded H-bridge inverter shown (Fig.2.16b1), each PV source is connected to an H-bridge inverter which consists of four switches. The DC-link inverter shown consists of one switch and freewheeling diode allocated to each PV source along with an H-bridge circuit.

The NPC converter with a bidirectional switch inverter has the lowest switch number, five, comparing with six in case of the DC-link inverter and eight in the other inverters. However, the NPC converter with a bidirectional switch inverter does not offer symmetrical AC positive and negative half cycles during the partial shading condition. This is because PV2 is responsible for establishing the first positive voltage level, while only PV1 establishes the first negative level. Consequently, if one of the PV sources is shaded, the inverter will not be able to generate a symmetrical AC voltage waveform.

2.7.2 PV Multilevel Inverter to Overcome Partial Shading

Among all the multilevel inverters, the cascaded H-bridge inverter (Fig.2.16b1) has gained a great deal of research interest in PV applications [20, 41-44]. Due to its modular circuit construction, each PV source power can be maximized individually by allocating a MPPT algorithm to each H-bridge circuit [20, 42]. The concept has been described in [20] using a five-level H-bridge inverter with two PV sources. Since each PV source was emulated by a voltage source connected in series with a resistor, the experiment does not reflect the correct PV response, particularly under shadowing. Otherwise, there is no research based on a cascaded H-bridge inverter that refers to a clear solution regarding the partial shading problem.

A multilevel neutral point clamped inverter (NPC) shown in Fig.2.16a1, is considered in [1] to extract the power from each PV source separately. Although the experimental results showed that power is delivered to the load, it has not been shown whether all PV sources operated at their MPPs. The neutral point clamped with bidirectional switch inverter, illustrated in Fig.2.16a3, was introduced in [39]. Even though the inverter is suggested for PV applications, the presented results

showed that the AC voltage waveform does not have symmetrical positive and negative half cycles.

2.8 Summary

Several PV-converter topologies have been reviewed in this chapter with respect to the main objectives - to control each PV source in the series connection individually and to find a solution to the partial shading problem.

With respect to the switching matrix approach, although the simulation results have shown that the power loss due to the partial shading can be reduced considerably in some shading situations, the system seems to be too sophisticated for practical implementation, and also under certain shading conditions the problem might become worse and an entire PV cluster can be bypassed.

With respect to the single-cell PV module, it can be a solution for a small scale PV system which uses a single PV module but not for larger systems.

Regarding the PV DC/DC modular system, it has the ability to extract the maximum power from each PV module in the series. However, it is not able to sustain this for a wide range of irradiance if at least one PV module has been shaded. Moreover, the system is costly to implement due to each PV source in the string being equipped with a converter.

The generation control circuit (GCC) PV system is a promising idea where the surplus current is passed to the load via an inductor or a DC source, so no PV source is bypassed. In this chapter, the GCC multi chopper system was modelled and simulated. The simulation results confirmed that during the shading situation only one PV source can operate at its MPP, so an operating point can be found where the largest amount of power can be delivered to the load.

The Retrofit circuit was discussed; the circuit analysis showed technical problems that make its implantation practically impossible.

The multilevel inverter PV system has been utilized successfully to control each PV source individually and to achieve its MPP with a high quality output AC voltage waveform. However, there is limited reported research dealing with the shading problem, with no or gives a clear solution to overcome the problem.

Chapter 3

Multilevel DC-Link Inverter System and PWM Switching Techniques

This chapter presents the PV multilevel DC-link inverter system developed by the author to deal with the partial shading problem and to exploit the fact that with varying the irradiance levels of the shaded PV sources the changes in their voltages are significantly less than their current changes, i.e. $\Delta V_{mpp}(G) << \Delta I_{mpp}(G)$, so the total voltage change of the series connected PV sources is low with large irradiance and current changes. The scheme is novel and has the features of simplicity regarding circuit implementation and a low number of switching components. The fundamentals of the multilevel DC-link inverter including the operating principle are presented. A comparative study to some digital multilevel PWM switching techniques is presented including the development of Integration-Duty Cycle Conversion PWM (IPWM) so it can be applied to numerous inverter levels. The chapter ends with applying direct PWM to the DC-link inverter, along with the associated waveforms.

3.1 The Proposed PV System

This thesis presents for the first time the application of the multilevel DC-link inverter for overcoming the problem of partially shaded series connected PV sources. A multilevel DC-link inverter is also called step inverter. The first multilevel DC-link inverter with digitally synthesized output DC bus was introduced in [40], where the input DC sources are binary weighted resulting in 2^n (n is the number of sources) possible switching states and the same number of output levels. In [34], based on equal DC input sources, the same idea was presented again in conjunction with NPC and flying-capacitor concepts to establish the DC bus voltage. In the topology of Fig.3.1, each PV units consists of one PV module, one terminal capacitor, switch and

diode. The PVs series connected and any or all of them can be switched in or out of the chain by turn on or off the associated switch. In the off-state each PV source is bypassed by its diode (switch-diode pair). This allows the generation of multiple voltage levels, which can approximate a sine wave when proper control is applied. The peak output voltage can be raised by increasing the number of series connected units. The H-bridge is only for converting the multilevel DC voltage waveform to AC positive and negative voltage half-cycles.

The switches of each unit (S1i, S2i) operate at a high switching frequency to form the multilevel positive DC-link waveform (V_{link}), while the switches S1 to S4 in the H-bridge operate at low frequency (50/60 Hz) to form the desired AC output voltage, specifically for a positive half cycle, S1 and S4 are on while S2 and S3 are off. To achieve the negative half cycle the complementary switch states are applied. The switching patterns of the inverter are listed in Table 3.1. The switch states are also illustrated by the circuit diagram shown in Fig.3.2 with the current flow corresponding to each state.

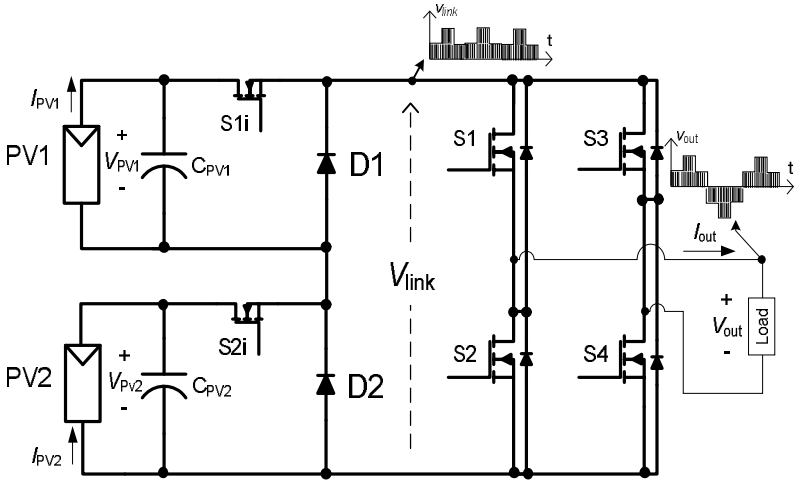


Fig.3.1: Five-level multiple-source (DC-link) inverter.

TABLE 3.1: Five-level (DC-link) Inverter Switching States

Switch state		Diode state		V_{link}
S1i	S2i	D1	D2	
ON	ON	OFF	OFF	$V_{PV1}+V_{PV2}$
ON	OFF	OFF	ON	V_{PV1}
OFF	ON	ON	OFF	V_{PV2}
OFF	OFF	ON	ON	0

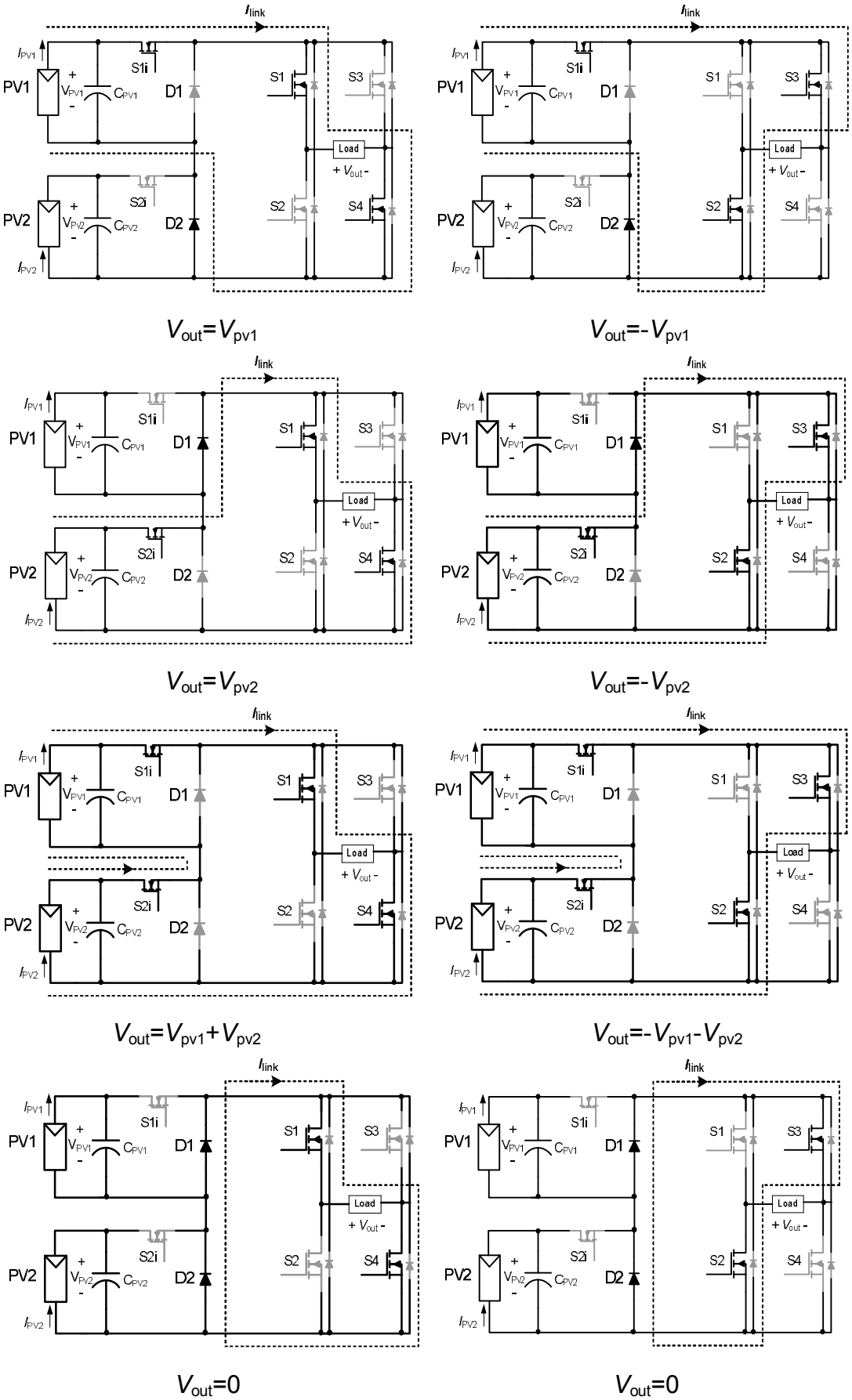


Fig.3.2: Switching states and current path of the five-level DC-link inverter.

3.1.1 Control Principles of PV Multilevel DC-link Inverter System

The proposed PV inverter system can be divided into two parts; the power circuit and the controller parts. The power circuit part, as described, consists of a multilevel DC-link inverter, multiple PV sources, and load which may be R, R-L, or the electricity grid. The controller is mainly a power-feedback regulator which consists of a MPP tracking algorithm and a multilevel PWM algorithm.

The principle of the control scheme, which is similar to that been used in [20, 45] is described here. Fig.3.3 shows the block diagram of the controller for the whole system. The control unit of the PV system includes a Perturbation and Observation (P&O) MPPT block for each PV source. These provide a separate P&O tracking algorithm and the PI control for each PV source. The output signals from these blocks are multiplied by a unity sinusoidal signal to form AC reference signals v_{ref1}, v_{ref2}, … $v_{ref(n)}$ (the PWM reference signals or the modulating signal). These reference signals are used to control the inverter switches by applying the PWM switching technique.

The control block diagram for PV grid-connected system which is based on the feedback current control is illustrated in Fig.3.4. The current and voltage measurements from the PV sources are fed to the P&O algorithm as power feedback to track the maximum power which can be extracted from the sources. The voltage error, which is the difference between the generated voltage from tracking via the MPPT algorithm and the actual PV voltage, is fed to the PI controller. The output of this controller determines the current magnitude at maximum power operation. This current magnitude is then converted into an AC value (current reference signal) by multiplying it with a unity sine signal which is synchronized with the grid voltage via a Phase Locked Loop (PLL) connected to the AC grid. The current error, which is the difference between the current reference signal and the actual current passing through the inverter to the grid, is passed to PI controller (current controller) so the reference voltage signals of the PWM algorithm can be generated. The resultant reference signals are used to generate the necessary control signals, which control the inverter switches, by applying the PWM switching technique.

The main purpose of the control scheme shown in Fig.3.3 is to maintain all the PV sources connected in series at the MPP as well as generating a low distortion

multilevel output voltage waveform via proper controlling of the inverter switches. In this thesis, the system shown in Fig.3.3 is applied in overcoming the PV partial shading via a control algorithm which is introduced to be used with the DC-link inverter for any number of the PV sources.

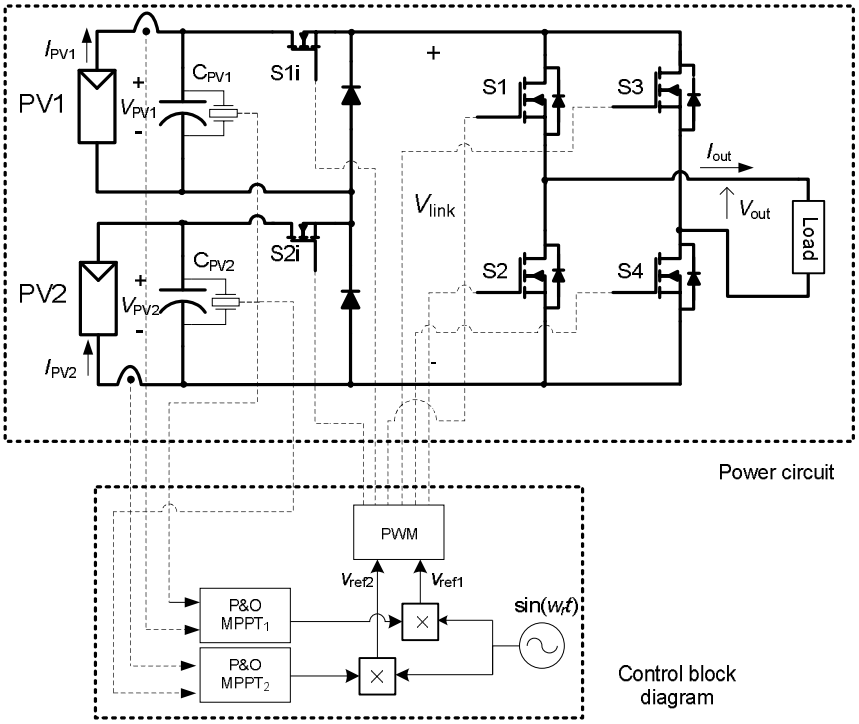


Fig.3.3: Five-level DC-link inverter with control block diagram applied for R and R-L loads.

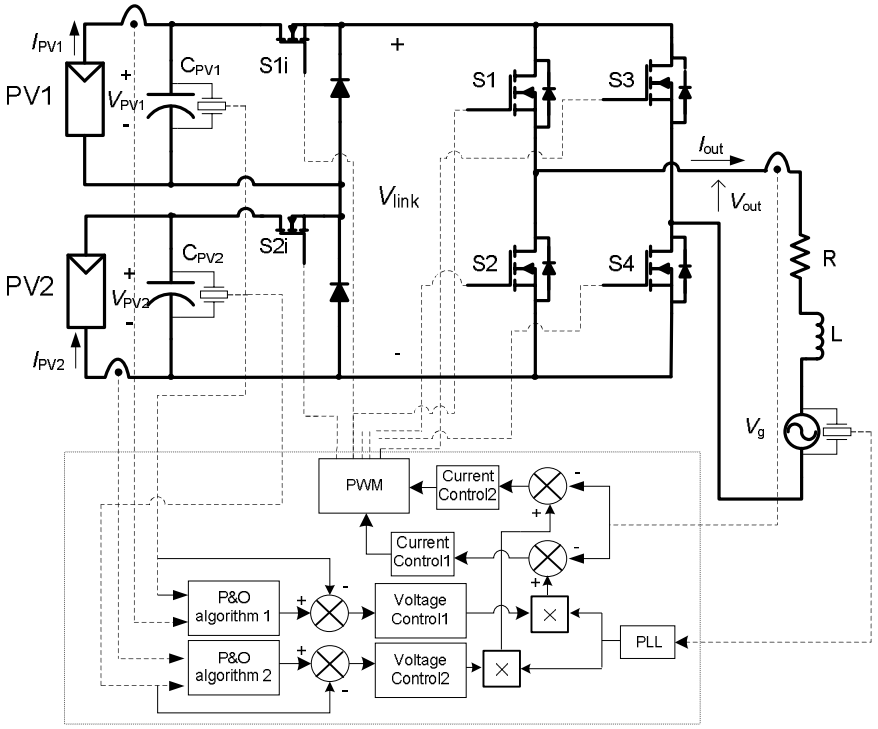


Fig.3.4: Five-level DC-link inverter with control block diagram applied for grid-connected applications.

Two essential parts of the system shown above are the maximum power point tracking (MPPT) algorithm, for tracking the MPP of the PV sources, and the digital pulse width modulation (PWM) to control the inverter switches to form the multilevel output voltage waveform. These parts will be investigated in detail in chapters three and four respectively.

The modelling and simulation of the DC-link inverter will be presented in chapter five, including different inverter levels along with the control methods which are introduced to deal with the partial shading problem.

3.2 Multilevel Inverter Switching Techniques

One of the most important criteria for inverter performance is the output sinusoidal quality, i.e. the levels of unwanted harmonic content. The harmonics result in many problems such as electromagnetic interference, current pulsation and power loss, causing performance deterioration and also equipment damages. Achieving high quality sinusoidal output voltage is mainly based on the inverter switching techniques. Undoubtedly high quality AC output waveform is needed in some applications, especially the high-power and grid-connected applications. In other applications such as AC motor drives, the low-order harmonics are the issue of most concern (the high-order harmonics are easy to filter). Due to the accessibility of high-speed power semiconductor devices, the unwanted output harmonic contents can be minimized considerably by applying adequate PWM schemes to control inverter switches. Consequently, the low-order harmonics will be very small in amplitude and the large amplitude harmonics are shifted to the high-order frequencies [35, 46-48].

Different forms of PWM switching techniques for multilevel inverters have been addressed in the literature [35, 47, 49, 50] in order to control the inverter output voltage frequency and magnitude and reduce the harmonic distortion produced. For Neutral-Point-Clamped and Flying-Capacitor inverters, there is also the issues of establishing capacitor voltage balancing and eliminating the common-mode voltages problem [46]. Even though the PWM techniques which are used to control the multilevel inverters are complicated, they are mainly derived from the basic two-level PWM techniques [51]. The most commonly used PWM schemes are the Sine-triangle PWM and the Space-Vector PWM [49, 52]. Selective-Harmonic-Elimination PWM

is popular for high power and high voltage applications for completely eliminating specific low-order harmonics as well as controlling the inverter output voltage [50].

3.2.1 Space-Vector PWM (SVPWM)

Even though the Sine-triangle PWM (SPWM) switching technique has gained significant attention in the recent past due to its simplicity and low output voltage distortion, it has poor flexibility regarding preserving the inverter capacitor voltage balancing and is less elegant with respect to digital implementation. On the contrary, SVPWM is characterized by high DC-link voltage exploitation and its ability to manage the suitable switching patterns so the DC-link capacitors' charging and discharging can be equally maintained [53]. Moreover, SVPWM is featured by low output voltage distortion, small output current ripple and its ease in digital implementation using the DSP. Consequently, it is one of the most researched PWM schemes and nowadays accounts for the most widely used PWM switching technique [49, 52].

In principle, SVPWM, which has been proposed in [54], is based on representing the desired three-phase reference voltages as a vector in α - β plane as illustrated in Fig.3.5. Using Park's transformation this voltage vector is expressed as [48].

$$\vec{V}_{ref} = V_\alpha + jV_\beta = \frac{2}{3}(V_a + \bar{a}V_b + \bar{a}^2 V_c) \quad \ldots\ldots \quad (3.1)$$

where $\bar{a} = e^{j120^o}$

Referring to the three-phase two-level inverter, there are N^3 (N=2) possible switching patterns which can be depicted into eight individual space vectors. Six of them have equal magnitude of $2/3V_{dc}$ and two are zero vectors having (111), (000) switching states as listed in Table 3.2. Using the same analysis these eight vectors can be applied to approximate the desired three-phase reference voltage $\vec{V}_{ref}$. The α - β coordinate is divided into six sextant of 60^o as illustrated in Fig.3.5. SVPWM strategy can be introduced as follows. Assume that carrier period T_c is small and reference voltage changes are negligible, at each T_c the reference vector $\vec{V}_{ref}$ can be represented only by the two nonzero vectors which form the 60 degree sector the

reference voltage vector resides in. For example, if vector $\vec{V}_{ref}$ exists in the second sector the switching states 110 and 010 plus zero vectors, 000 or 111, can be used to approximate the reference voltage vector within T_c duration based on equation 3.2 [48, 54].

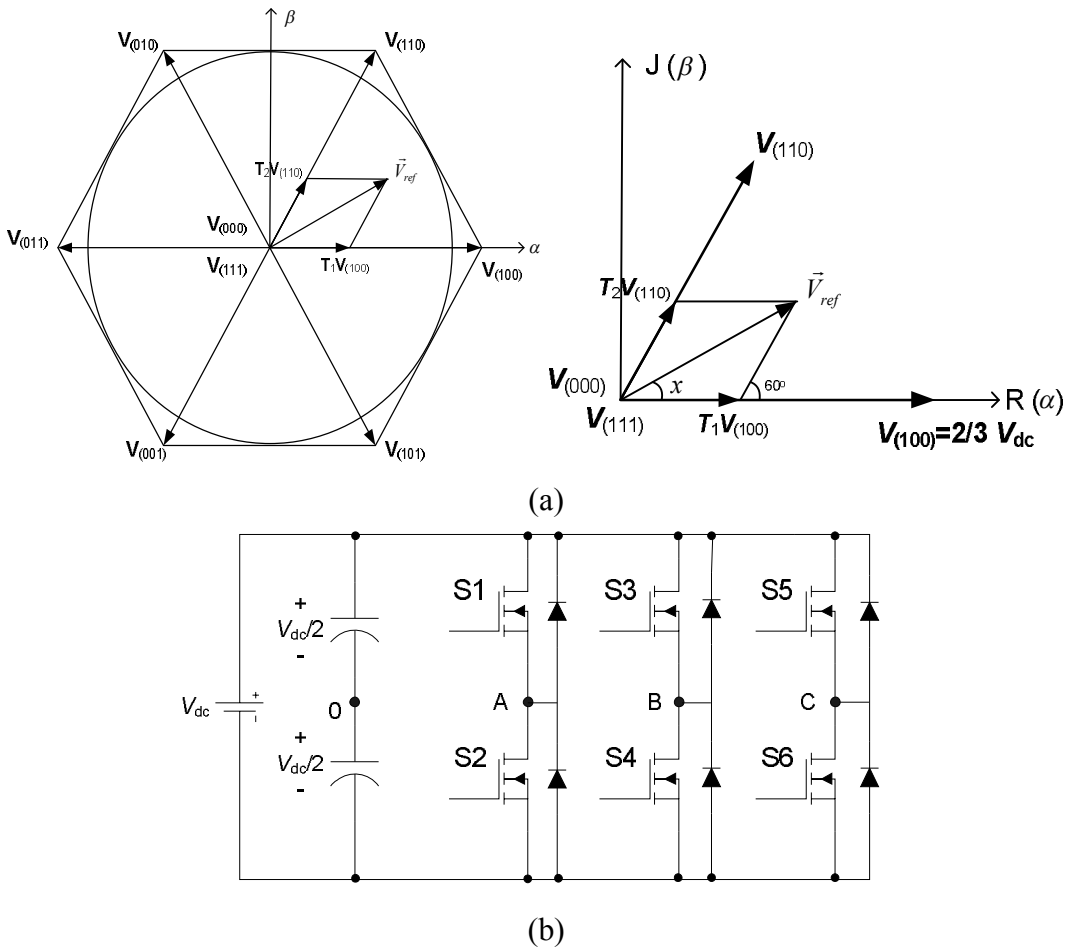


Fig.3.5: (a) Space-vector representation of reference voltage and switching states and (b) three-phase two-level inverter circuit.

$$\vec{V}_{ref}.T_c = \int_{t}^{t+T_c} \vec{V}_{ref}\,dt \approx \vec{V}_{(100)}.T_1 + \vec{V}_{(110)}.T_2 + \vec{V}_{(000\,or\,111)}.T_0 \quad \ldots\ldots\ldots \quad (3.2)$$

where $T_c = T_1 + T_2 + T_0$

Assume that, $\vec{V}_{ref}$ is located in sector number one and has got angle χ with α-axis. By the vector coordinate analysis, T_1 and T_2 can be calculated by using equations 3.3 and 3.4 [48].

$$\left|\vec{V}_{(100)}\right| T_1 + \left|\vec{V}_{(110)}\right| T_2 \cos(\frac{\pi}{3}) = \left|\vec{V}_{ref}\right| T_c \cos(x) \qquad \text{…….} \quad (3.3)$$

$$\left|\vec{V}_{(110)}\right| T_2 \sin(\frac{\pi}{3}) = \left|\vec{V}_{ref}\right| T_c \sin(x) \qquad \text{…….} \quad (3.4)$$

TABLE 3.2: Switch States for Two-level Three-phase Inverter

State No.	Switching state	On state	Off state	V_{ab}	V_{bc}	V_{ca}
1	100	S_1,S_4,S_6	S_2,S_3,S_5	V_{dc}	0	$-V_{dc}$
2	110	S_1,S_3,S_6	S_2,S_4,S_5	0	V_{dc}	$-V_{dc}$
3	010	S_2,S_3,S_6	S_1,S_4,S_5	$-V_{dc}$	V_{dc}	0
4	011	S_2,S_3,S_5	S_1,S_4,S_6	$-V_{dc}$	*0*	V_{dc}
5	001	S_2,S_4,S_5	S_1,S_3,S_6	0	$-V_{dc}$	V_{dc}
6	101	S_1,S_4,S_5	S_2,S_3,S_6	V_{dc}	$-V_{dc}$	0
7	111	S_1,S_3,S_5	S_2,S_4,S_6	0	0	0
8	000	S_2,S_4,S_6	S_1,S_3,S_5	0	0	0

T_1 is the active time for switching state (100), T_2 is that for switching state (110), and T_0 is the time duration for switching state (111) or (000). Equations 3.3 and 3.4 can be rewritten to a generalized form in equations 3.5 and 3.6 [48].

$$T_1 = \frac{\sqrt{3}T_c}{V_{dc}}\left(V_\alpha \sin(\frac{\pi}{3}k) - V_\beta \cos(\frac{\pi}{3}k)\right) \qquad \text{……..} \quad (3.5)$$

$$T_2 = \frac{\sqrt{3}T_c}{V_{dc}}\left(-V_\alpha \sin(\frac{\pi}{3}(k-1)) + V_\beta \cos(\frac{\pi}{3}(k-1))\right) \qquad \text{……..} \quad (3.6)$$

where k=1, 2,…., 6 is the sector number, $V_\alpha = \left|\vec{V}_{ref}\right|\cos(x)$, $V_\beta = \left|\vec{V}_{ref}\right|\sin(x)$

The three determined switching states are applied to the power switches for the durations T_1, T_2 and T_0, respectively in every T_c. The arrangement of the switching patterns applied to the power switches are configured in a manner to reduce the switching power loss and achieving symmetrical PWM, Fig.3.6 illustrates that [47, 48].

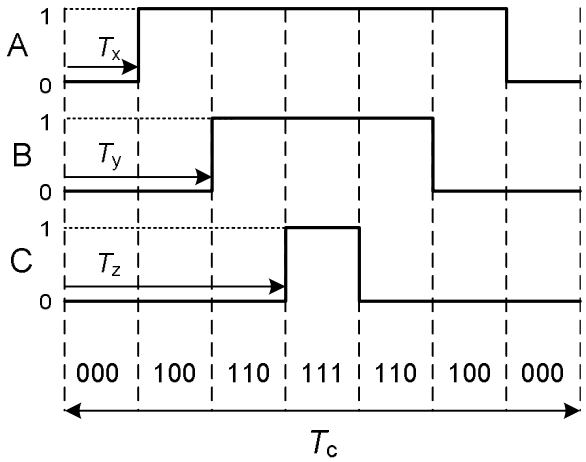


Fig.3.6: Symmetrical SVPWM patterns sequence.

where:

$$T_x = \frac{1}{4}T_0$$

$$T_y = \frac{1}{4}T_0 + \frac{1}{2}T_1$$

$$T_z = \frac{1}{4}T_0 + \frac{1}{2}T_1 + \frac{1}{2}T_2$$

Overall, the SVPWM algorithm can be summarized in three steps. Firstly, the three-phase reference voltages are sampled at every T_c time interval and converted to a reference vector by the space-vector equation 3.1, and so α and β components can be achieved. Secondly; the sector (triangle) number and the corresponding switching states are determined via the angle χ of the reference vector. Finally, the α and β components of the reference vector as well as the sector number, are used in equations 3.5 and 3.6 in order to calculate the switching states active time (dwelling time [55]).

The above explained two-level SVPWM is not a complicated algorithm to be implemented. However, for a multilevel converter, as a consequence of each additional level the complexity will escalate considerably. With respect to the three-level SVPWM, there are 3^3 (27) possible switching states which results in 27 base vectors, eight of them are redundant overlapping vectors, which have the same magnitude, [56]. Fig.3.7 illustrates the space-vector representation for switching vectors of a three-level inverter, as it can be seen, the vector-space is divided into 24 triangles, which can be calculated by $6(N\text{-}1)^2$ [37, 55].

The level of complexity rises from finding the suitable triangle in which the reference vector is located, to determining the proper switching sequence due to the

availability of redundant switching states. With high switching frequency all the mentioned steps have to be carried out within one carrier wave period T_c, therefore developing fast and simplified SVPWM algorithm is an important issue. A part of the five-level inverter space-vector switching states is illustrated in Fig.3.7. In this case there are 5^3 (125) switching states, 64 of them are redundant vectors [56]. Also the vector-space will include 96 triangles, so determining the desired vector is not an easy task [55]. For the Neutral-Point-Clamped and Flying-Capacitor inverters, the redundant switching patterns are employed to ensure the DC-link capacitor voltage balancing [57]. In [58] the three-level inverter space vectors were classified into four groups according to their magnitudes, clearly the zero and the voltage vectors giving full DC-bus voltage have no influence on the capacitor voltage balancing. However, the other voltage vectors affect the capacitor voltage balancing by various levels. Due to this, the vector switching sequence has to be controlled properly to maintain equal capacitor charging and discharging times. Also, keeping the inverter operating at high amplitude modulation index (M_a), which is close to the circle illustrated in Fig.3.5 where the magnitude is $V_{dc}/\sqrt{3}$, will ensure full exploitation of the DC-link voltage.

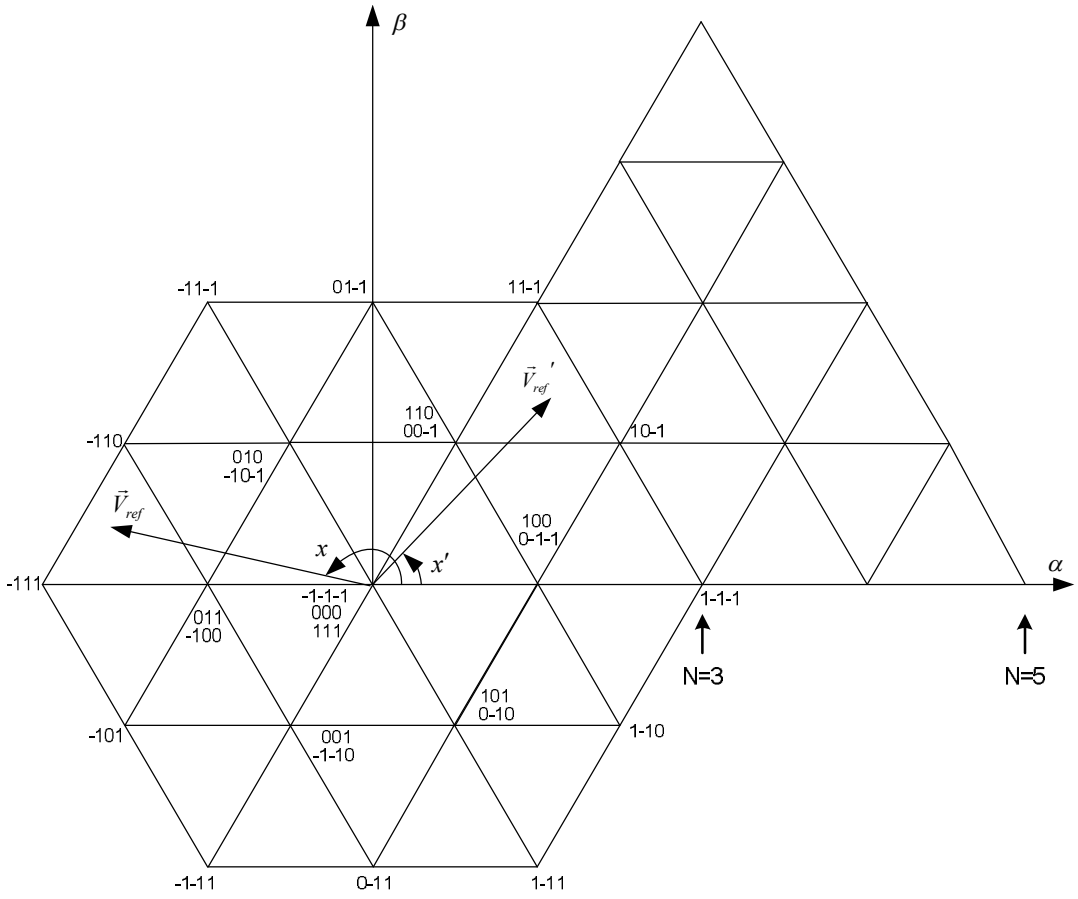


Fig.3.7: Space-vector depiction of 3 and 5 level inverters switching patterns.

This increases the large voltage vectors utilization and has no effect on the capacitor voltage balancing. However, it may cause over modulation of voltage.

Two generalized multilevel PWM algorithms, which have been proposed by Dai et al., are presented in the following sections.

3.2.1.1 Two-Level Based Multilevel SVPWM

Many multilevel SVPWM strategies have been reported in the literature are based on the conventional two-level SVPWM calculations [37, 55, 58, 59]. In [59, 37], determining the desired triangle, which the reference vector is located in, can be achieved via finding the corresponding angular position (x') of the reference vector in the first 60° sector which is used as the reference sector. This is done by, as shown in Fig.3.7, using $x' = rem(x/60^o)$, $x' \le 60^o$ (where "*rem*" refers to division remainder). Then, by comparing α - β components of the corresponding reference vector ($\vec{V}_{ref}'$) with the margins of the triangles, the desired corresponding triangle number is determined. The triangle number and the original section number, which is determined via the integer part $int(x/60^o)+1$, are used to select the right switching states and the applied sequence by employing a look-up table. The dwelling time calculations can be carried out by finding small reference vector (sub-vector $\vec{v}_s$) inside the determined corresponding triangle and applying equations similar to 3.3 and 3.4. The triangles are classified into two types, and accordingly there are two sub-vector positions as shown in Fig.3.8.

Another approach was introduced in [55], as it is clear in Fig.3.9; the vector space is divided into two-level hexagons. The reference vector is represented by another vector which is centralized into the selected two-level hexagon, and then the conventional two-level time calculations can be applied.

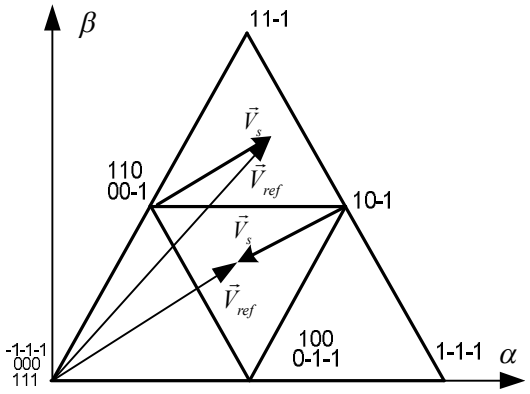


Fig.3.8: Sub-vector representation.

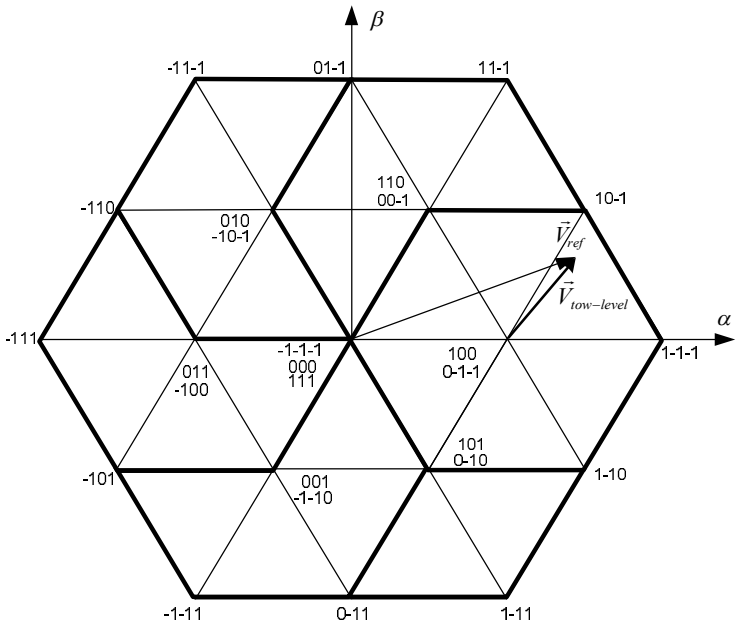


Fig.3.9: Vector space divided in to two-level hexagons.

A generalized and simplified SVPWM strategy has been introduced by Dai et al. in [60], the most important feature is that no patterns look-up table is required. The algorithm steps can be summarized as follows:

1. The three-phase voltage samples are normalized according to the number of converter levels, N, and the magnitude of the DC-bus voltage, V_{dc}, thus the following formula is used:

$$(v_a, v_b, v_c)_{norm.} = \frac{(v_a, v_b, v_c)}{V_{dc}/(N-1)} \qquad \ldots\ldots\ldots (3.7)$$

2. The resulting normalised vector is then decomposed into two components: an offset vector, $\vec{V}_{offset}$ and a two-level vector $\vec{V}_{two}$. The former is found by taking the integer part of the normalised reference vector,

$$\vec{V}_{offset} = (v_{offset,a}, v_{offset,b}, v_{offset,c}) = (S_a, S_b, S_c) = Mod((v_a, v_b, v_c)_{norm}) \quad \ldots. (3.8)$$

Where, the *Mod* function is illustrated in equation 3.9 which includes the function int(v) in order to achieve the integer value of v.

$$\text{Mod}(v) = \begin{cases} \text{int}(v).....v \geq 0 \\ \text{int}(v) - 1.....v < 0 \end{cases} \qquad \ldots\ldots\ldots (3.9)$$

3. The second component, the two-level normalized reference voltages are calculated by using the following equation:

$$\vec{V}_{two} = (v_{two,a}, v_{two,b}, v_{two,c}) = (v_{a,norm} - v_{offset,a}, v_{b,norm} - v_{offset,b}, v_{c,norm} - v_{offset,c}) \ldots\ldots (3.10)$$

As shown in Fig.3.10, $\vec{V}_{two}$ is the representation of the achieved two-level voltage vector in the vector-space and thus corresponds directly to the duty cycles of the corresponding phase switches. The offset vector values indicate the levels in which to switch between. The switching states sequence is carried out according to the directions which are presented in Fig.3.10. For instance, the following sequences are for half-symmetrical PWM cycle as a result of falling $\vec{V}_{two}$ in section number two and five respectively.

Section 2, $(S_a, S_b, S_c), (S_a, S_b + 1, S_c), (S_a + 1, S_b + 1, S_c), (S_a + 1, S_b + 1, S_c + 1)$

Section 5, $(S_a, S_b, S_c), (S_a, S_b, S_c + 1), (S_a + 1, S_b, S_c + 1), (S_a + 1, S_b + 1, S_c + 1)$

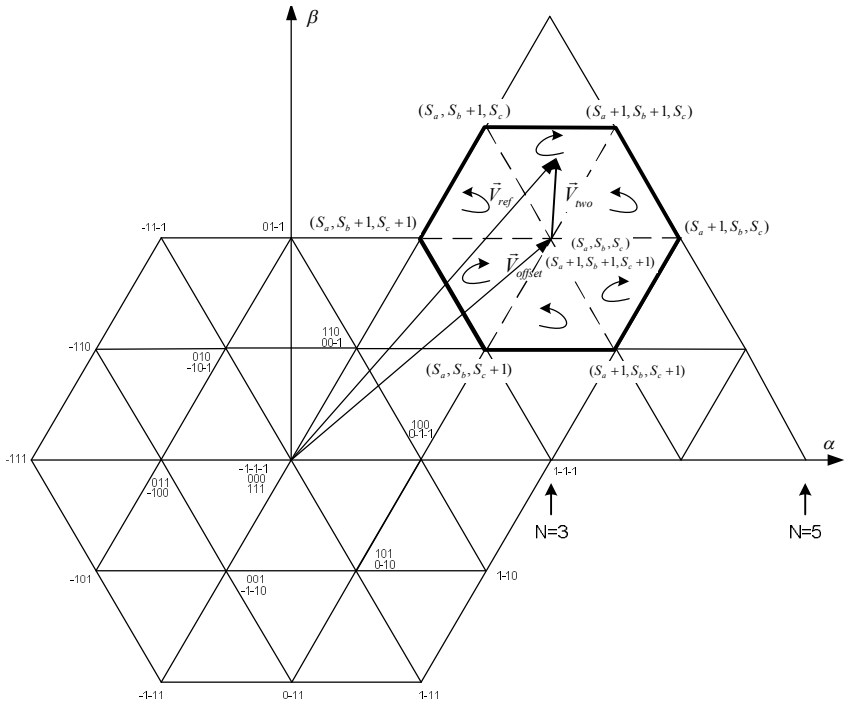


Fig.3.10: Two-level based generalized multilevel SVPWM.

3.2.2 Generalized Direct Multilevel PWM

The computational efforts have been reduced dramatically in [61] where no vector decomposition and dwelling time equations are required. Each phase is processed individually, and that means each phase has only two switching modes S and $S+1$ (off and on states respectively) as shown in Fig.3.11. The three-phase off states (S_a, S_b, S_c) are achieved as in the previous section and t_{off} , t_{on} per each phase can be derived by the same concept in equation 3.2 as following:

$$v_{ref,norm.}.T_c = v_{offset}.t_{off} + (v_{offset}+1).t_{on} \qquad \text{..... (3.11)}$$

By substituting of $t_{off} = T_c - t_{on}$ and $v_{two} = v_{ref,norm.} - v_{offset}$ in equation 3.11, the following equation is obtained:

$$t_{on} = v_{two}.T_c \qquad \text{..... (3.12)}$$

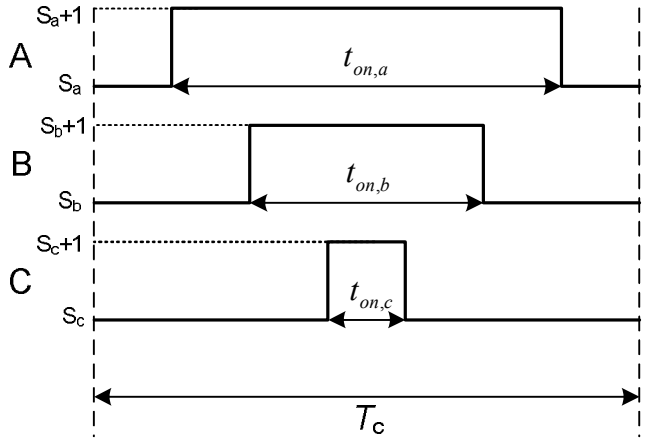


Fig.3.11: Three-phase Direct PWM switching sequence.

3.2.3 Integration-Duty Cycle Conversion PWM (IPWM)

IPWM algorithm is based on integration of the desired reference waveform. The obtained integration is then converted to a time value which is used to generate the inverter control signal. Conditionally the integration of the control signal has to be equal to the integration of the reference waveform over one sample time interval T_c. Overall, the generated control pulses have duty cycles proportional to integrated part of the reference waveform. As shown in Fig.3.12, the time period of the sinusoidal reference signal is divided into M_f parts according to the ratio between the frequency

of carrier wave and that of reference signal. The integration duty cycle of each part (A_n) can be determined by applying equation 3.13 [35].

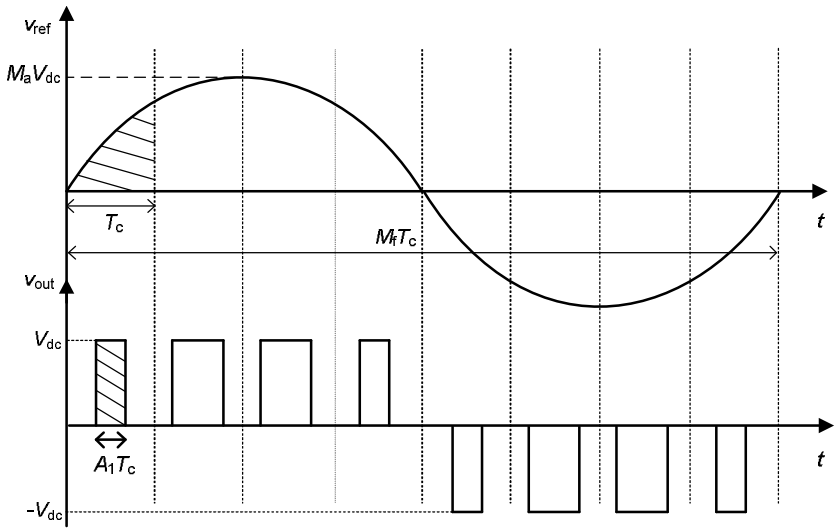


Fig.3.12: IPWM reference and output waveforms.

$$A_n = \frac{1}{T_c}\int_{(n-1)T_c}^{nT_c} M_a \sin(\omega_{ref} t)\cdot dt\,,\ n = 1,2,3,\ldots M_f \quad \ldots\ldots\ldots (3.13)$$

In this thesis the three-level IPWM introduced in [35] is developed to a simplified generalized PWM algorithm, which can be used to control higher level photovoltaic (PV) inverters. The proposed algorithm is implemented experimentally by using DSP unit to control the multi-level DC-link inverter.

In the generalized multilevel IPWM algorithm the integration duty cycle, which is required to determine the high and low level voltage switching activation times (T_{OH}, T_{OL}), can be determined directly via the following equation:

$$A_n = \frac{M_f M_a}{2\pi}\cdot[\cos(\theta_{n-1}) - \cos(\theta_n)] \quad \ldots\ldots\ldots (3.14)$$

It is clear that, by using the present sampling time $\theta_n = n\cdot\omega_{ref}\cdot T_c$ and corresponding reference voltage sample $v_{ref}(nT_c)$, as well as the desired amplitude and frequency modulation indexes M_a and M_f respectively, the required integration over T_c time period can be accomplished easily without establishing a look-up table or any predetermined calculations. Implementation procedure for the proposed generalized IPWM algorithm is illustrated in the flowchart shown in Fig.3.13, where the inverter level voltage V_l is used to modify equation 3.14.

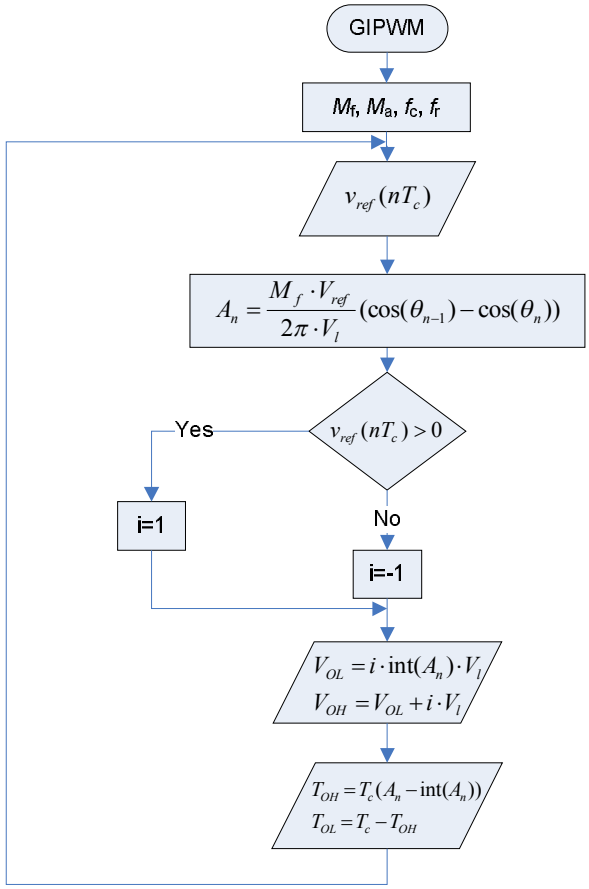


Fig.3.13: Generalized IPWM algorithm.

where $V_l = V_{dc}/2$ for inverter level N=2 and $V_{dc}/(N\text{-}1)$ for N=3 onwards, V_{ref} is the amplitude of the desired reference voltage, V_{OL} and V_{OH} are the inverter output low and high level voltages respectively.

In case of the magnitude V_{ref} is not known such as closed-loop system with variable feedback voltage, V_{ref} can be determined according to the following expression.

$$V_{ref} = \frac{v_{ref}(nT_c)}{\sin(\theta_n)} \qquad \text{..... (3.15)}$$

The only problem which can be noticed in equation 3.15 is when $\sin(\theta_n)=0$, and that can be solved as shown in Fig.3.14.

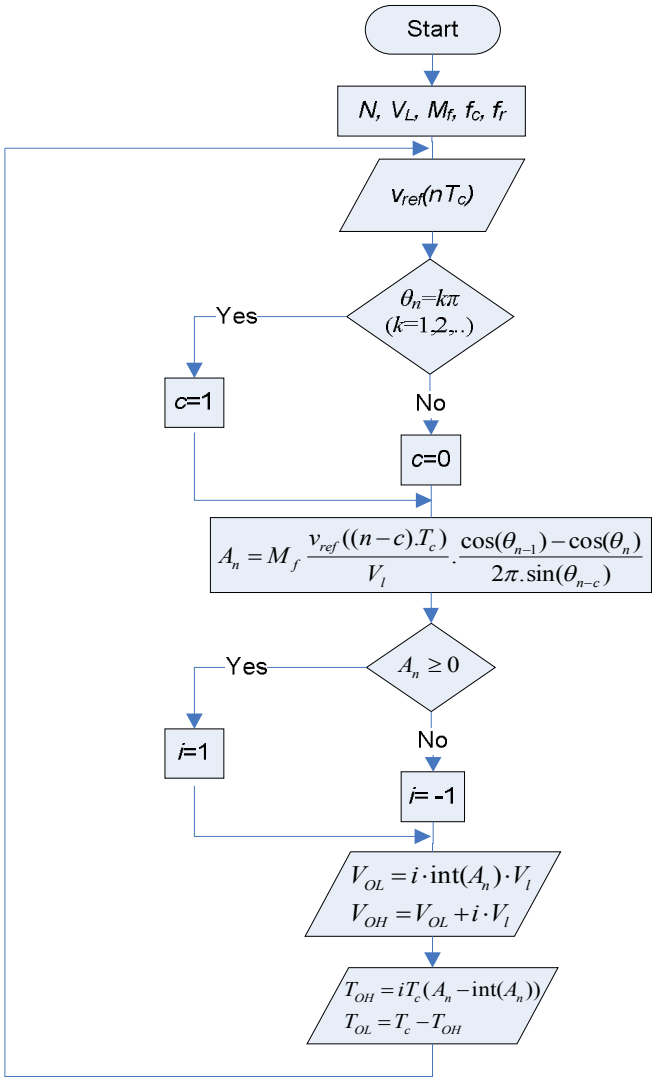


Fig.3.14: Modified Generalized IPWM algorithm.

3.3 Multilevel PWM Simulation Results

Three multilevel PWM switching strategies were simulated by using C++ programming language; the strategies are the generalized two-level based SVPWM, the generalized direct PWM and IPWM. Under different amplitude modulation index M_a. The output phase and line voltage waveforms are analysed by using FFT and the voltage spectra as well as the total harmonic distortion (THD) depictions are presented. Table 3.3 lists the used parameters.

TABLE 3.3: PWM Parameters

V_l	155.56 V	M_f	40
f_r	50Hz	Harmonics No.	100

3.3.1 Generalized Direct PWM Results

The three-phase reference waveforms illustrated in Fig.3.15 are applied to the direct PWM algorithm. The resulted phase and line waveforms are shown in Figures 3.16a and 3.16b for five-level inverter N=5. The achieved THD is shown in Fig.3.17. For further illustration the 3D depiction phase and line spectra are shown in Figures 3.18a and 3.18b respectively.

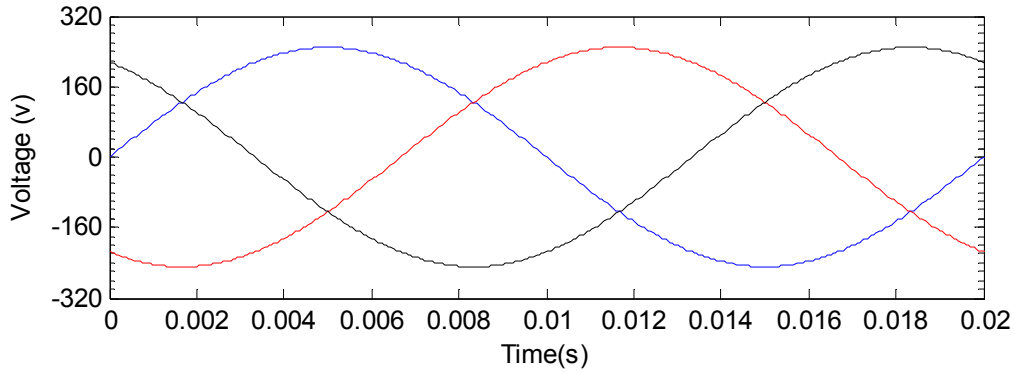


Fig.3.15: Three-phase reference waveforms at M_a=0.8, V_{ref}=248.90 V.

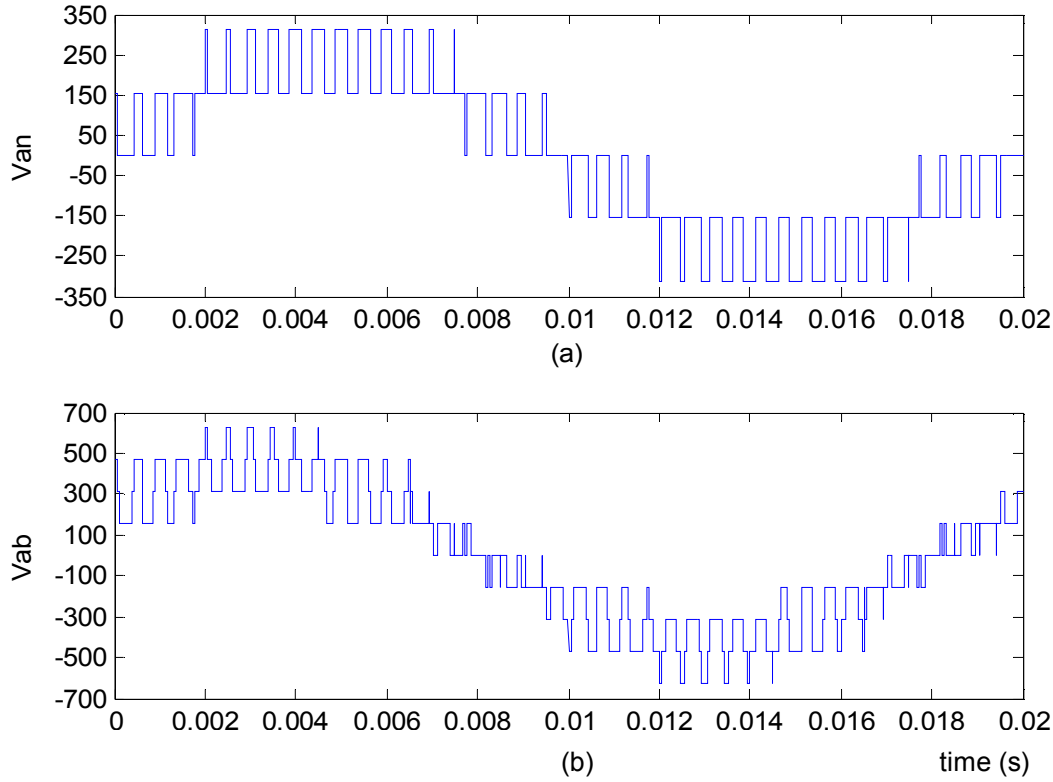


Fig.3.16: Direct PWM (a) phase and (b) line waveforms at M_a=0.8.

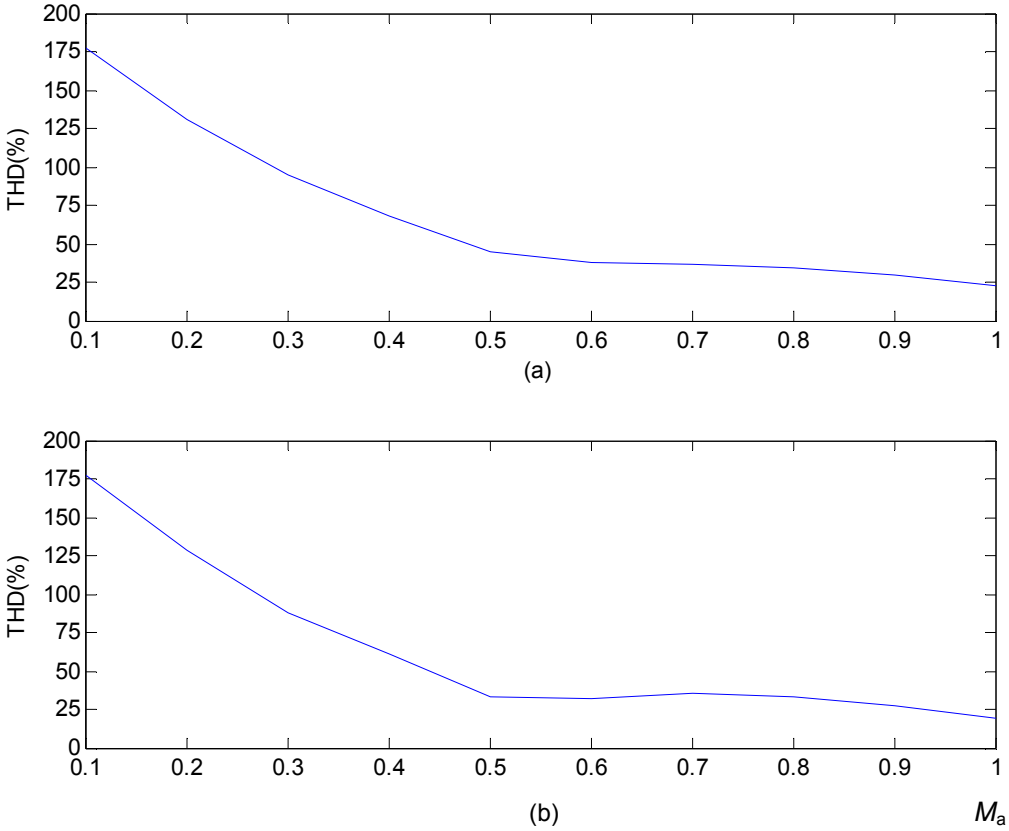
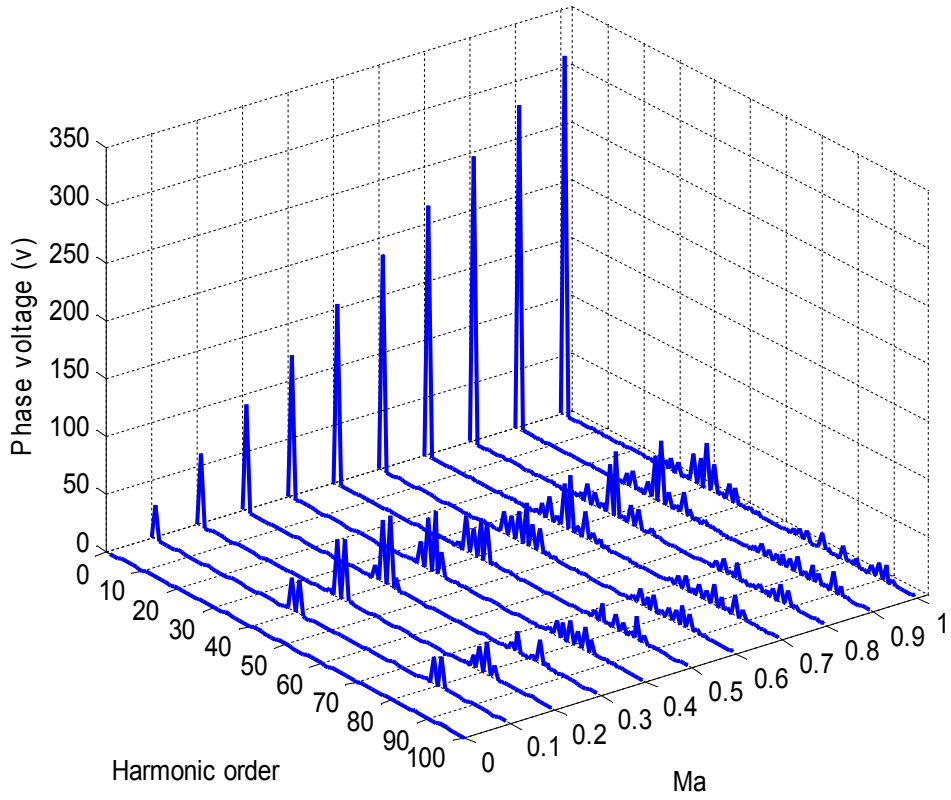
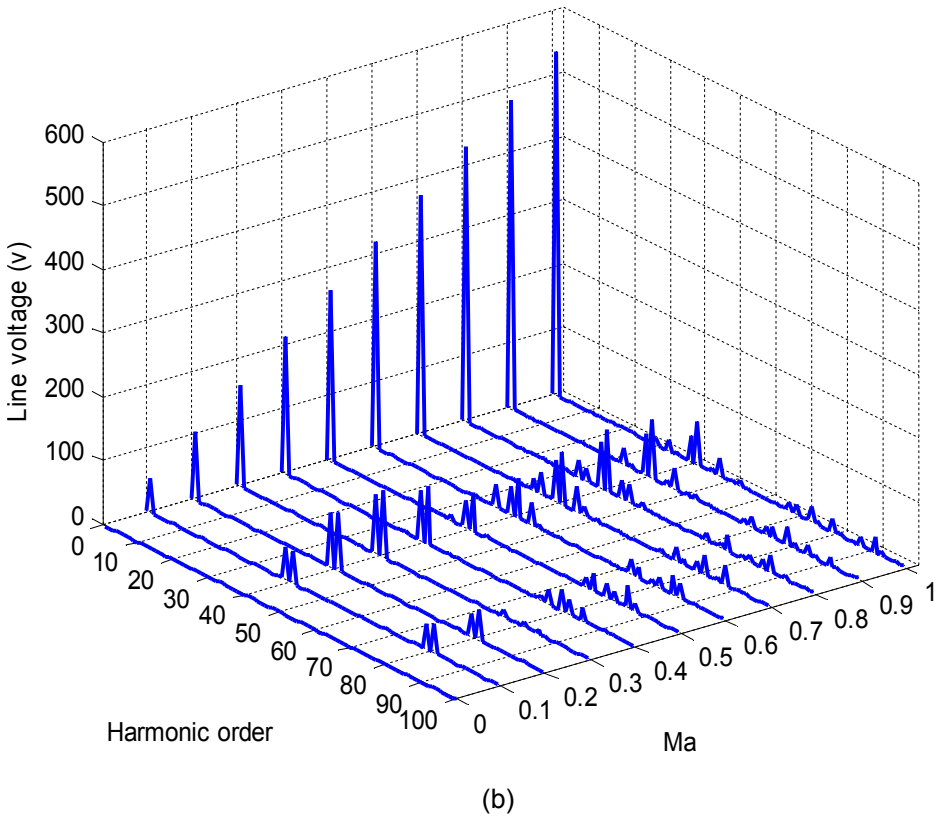


Fig.3.17: Direct PWM (a) phase and (b) line voltage THD at M_a=0.8.



(a)



(b)

Fig.3.18: Direct PWM 3D (a) phase and (b) line voltage spectra

3.3.2 Generalized Two-level Based SVPWM Results

Two-level based SVPWM is applied to achieve PWM output waveform. Approximately the same results of the generalized direct PWM were obtained.

3.3.3 IPWM Results

The generalized IPWM algorithm is applied to generate five-level voltage waveform. As it can be seen, Figures 3.19a and 3.19b show the output phase and line voltage waveforms. The associated THD depictions are illustrated in Figures 3.20a and 3.20b. For various M_a the 3D spectra depictions are presented in Figures 3.21a and 3.21b for the phase and line voltage respectively.

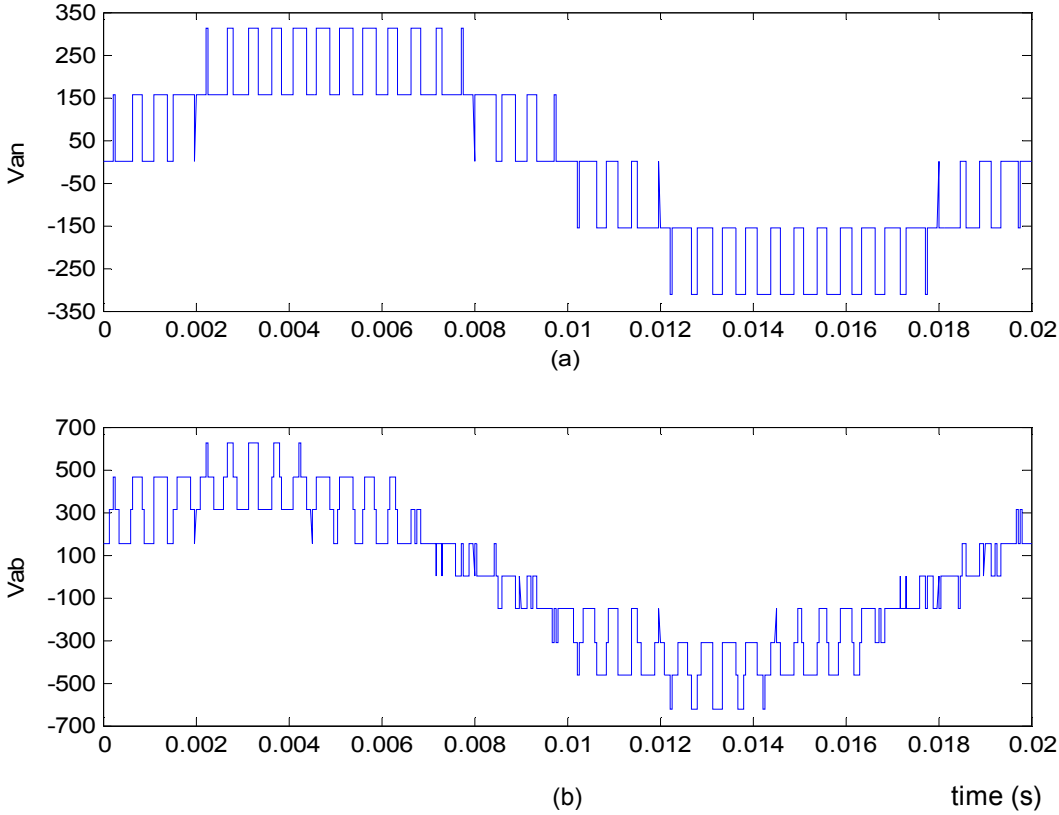


Fig.3.19: IPWM (a) phase and (b) line waveforms at M_a=0.8.

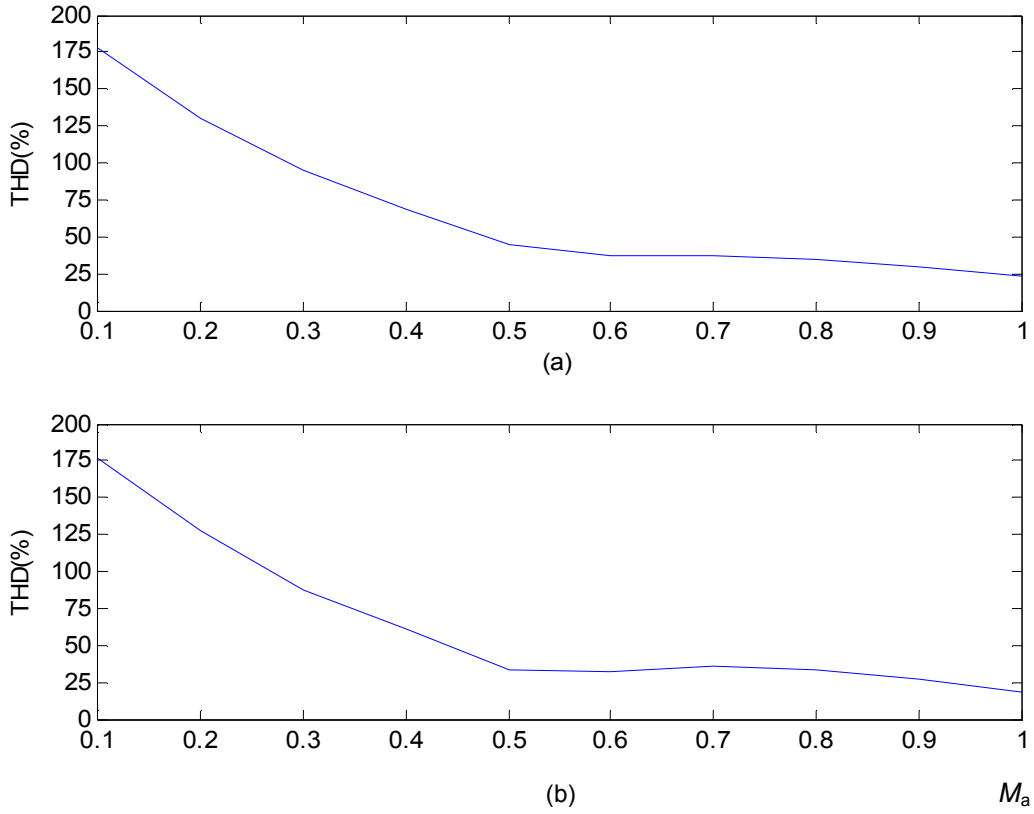
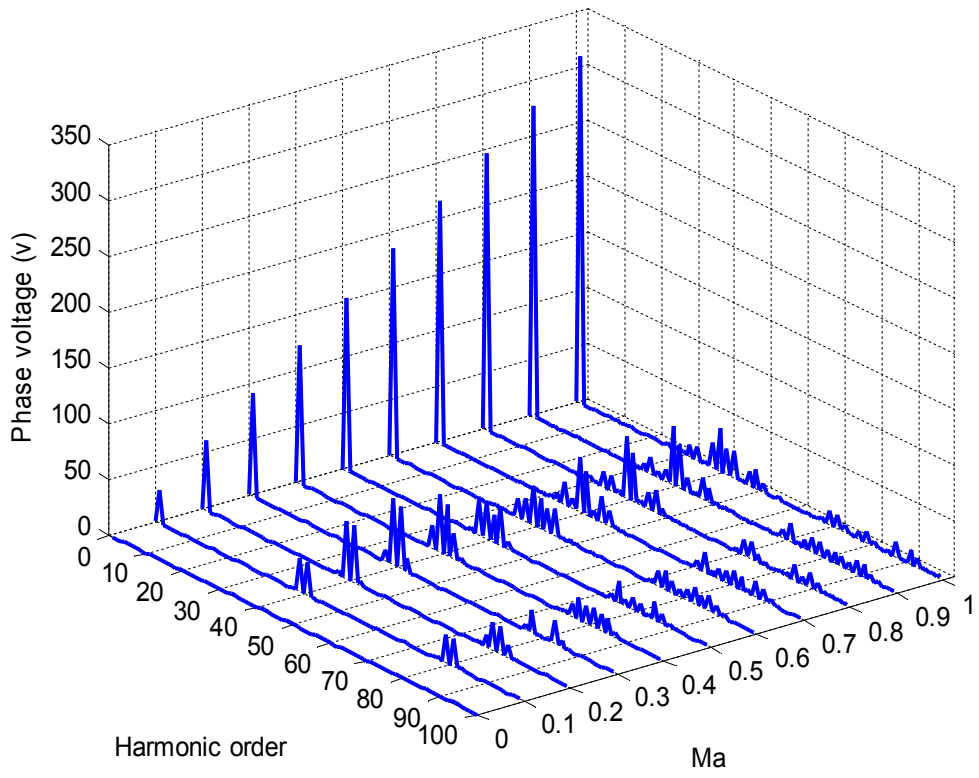
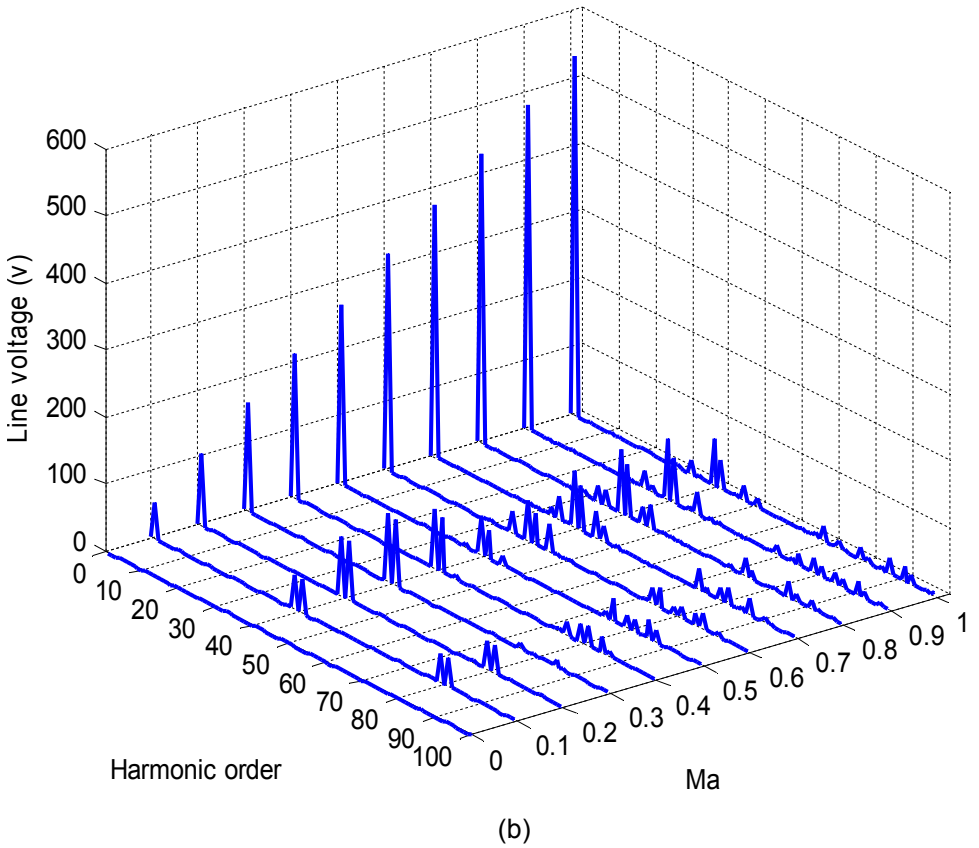


Fig.3.20: IPWM (a) phase and (b) line voltage THD at M_a=0.8.



(a)



(b)

Fig.3.21: IPWM 3D (a) phase and (b) line voltage spectra.

3.4 PWM Control of the DC-link Inverter

As it can be concluded from the results above, the three reviewed multilevel PWM switching techniques give almost the same results regarding the harmonics analysis and the output quality. However, the direct PWM switching technique is the easiest switching method to be implemented as well as the lowest computational efforts comparing with the other stated algorithms so it is applied to the PV system implemented in this thesis. The following Figure shows a generalized DC-link inverter system powered by *n* PV sources. As can be seen, the direct PWM algorithm generates the control signals which are necessary to control the inverter switches.

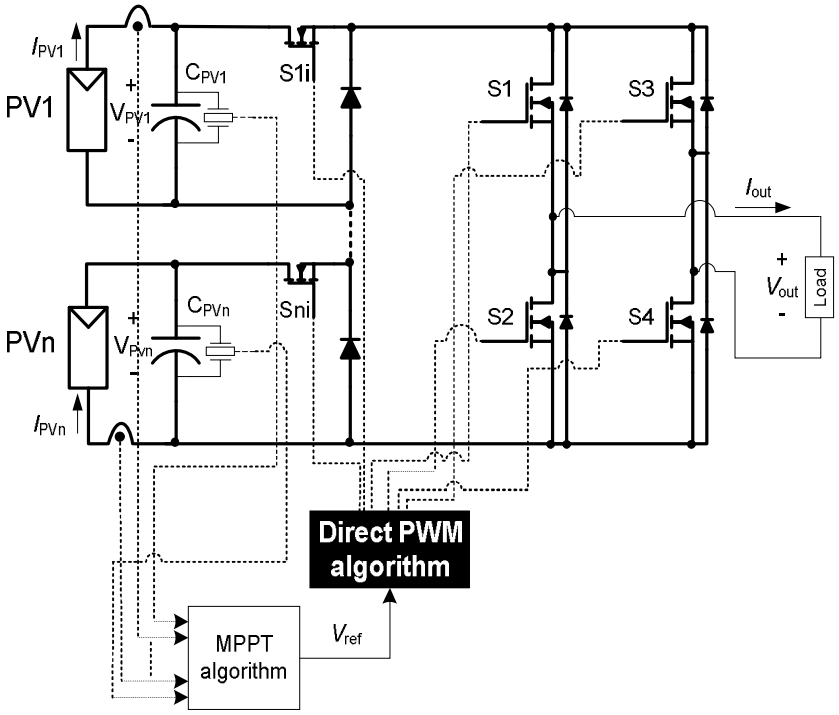


Fig.3.22: *n* PV sources DC-Link inverter system.

Fig.3.23 illustrates the entire process for the direct PWM technique applied to a three PV sources DC-link inverter starting with the desired reference signal, the necessary switching control signal, which is applied to the gate of the inverter switches, and the inverter output voltage waveform.

$v_{ref(i)}$ represents the samples of the desired reference voltage where i=1 to M_f applied every time period of T_r ($1/f_r$). The 1 and 0 of the control signals refer to the switches' states on and off respectively.

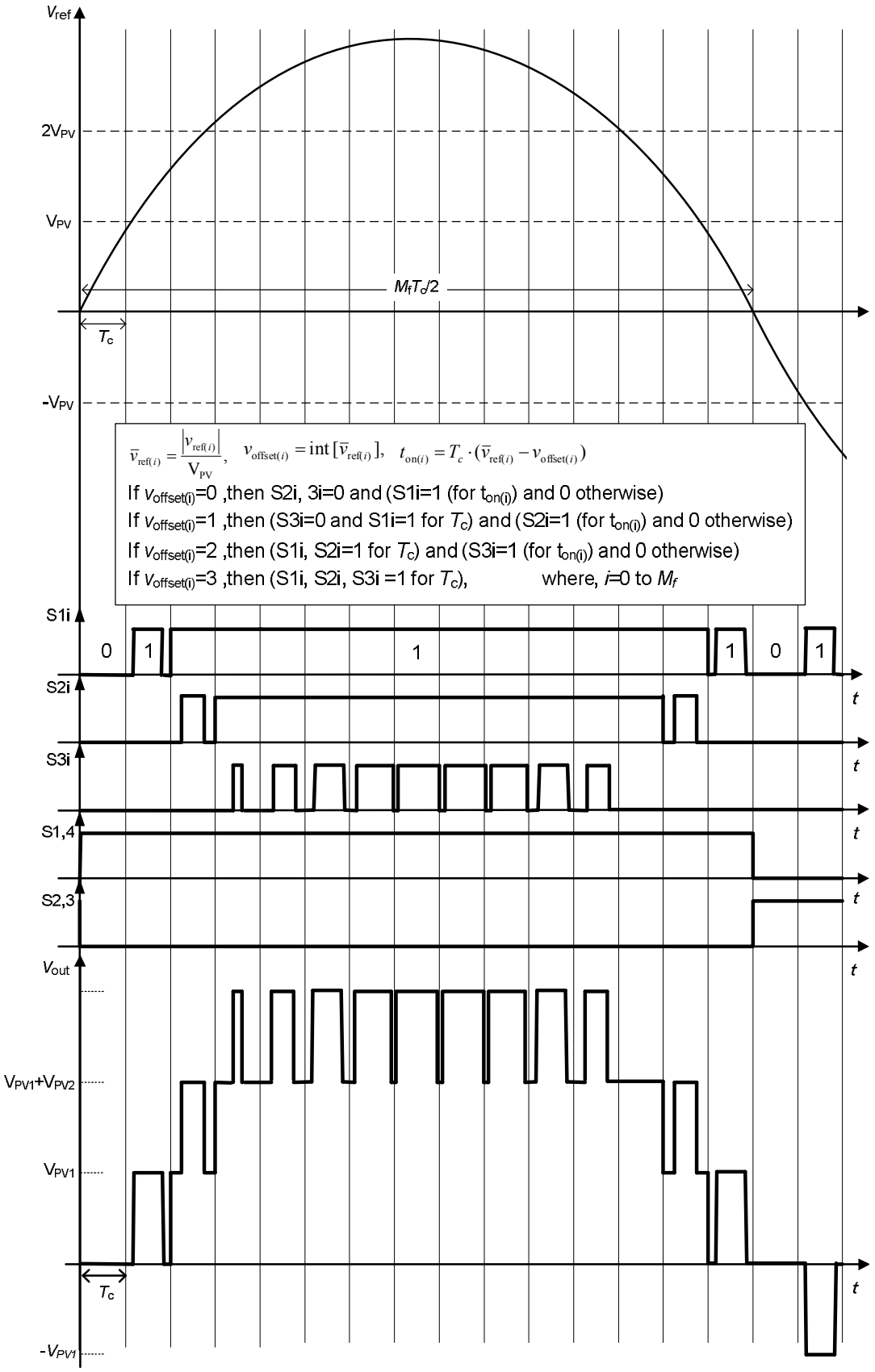


Fig.3.23: Direct PWM waveforms.

3.5 Summary

The multilevel DC-link inverter is suggested to be used in overcoming the PV partial issue, where each PV system can operate at its MPP and the entire extracted power can be delivered to the load. This chapter presented the inverter system and the circuit operation fundamentals. Also, the chapter focused on the comparison of some multilevel switching techniques.

Low harmonic distortion AC output waveform can be achieved via the multilevel PWM switching techniques due to two basic features. Firstly, the PWM pushes the unwanted harmonics towards the easy-filtration region. Secondly, the multilevel mechanism results in a steps waveform which is very close to the pure sinusoidal waveform and that means lower harmonic content. The digital implementation suitability and the algorithm simplicity have to be considered in order to accomplish easier control and lower execution time.

Developing the three-level IPWM algorithm to a generalized IPWM algorithm is accomplished. According to the discussed techniques, the direct PWM strategy is the lowest computational effort algorithm. Overall, the simulation results show that the SVPWM, direct PWM and IPWM have almost the same analytical results. However, more freedom can be achieved specifically by applying the two-level based SVPWM because of using the redundant switching patterns and their dwelling times.

The use of the direct PWM with the DC-link inverter is also presented along with the required switching control waveforms.

Chapter 4

Maximum Power Point Tracking Techniques

In order to extract the maximum PV available power at certain atmosphere and load conditions, maximum power point tracking has to be used. As can be seen in Fig.4.1, the direct connection of the load to the PV source results in the operating point of the PV source being the intersecting point of I-V curve with the load impedance line. However, this point may not be at the location where the PV panel generating the maximum power [62].

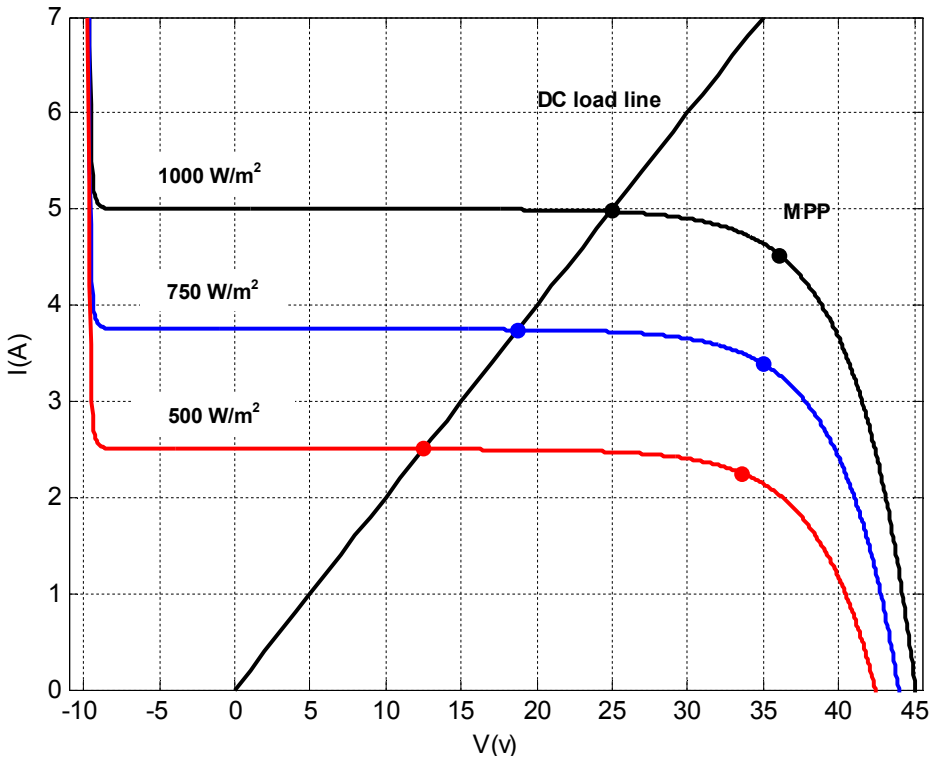


Fig.4.1: I-V PV characteristics and load line.

As illustrated in Fig.4.1, the load line crosses the PV I-V characteristic curves under different irradiance levels at several points. The load impedance at these points is always 5 Ω, while the PV impedances at MPP are 8 Ω at 1000 W/m^2, 10.36 Ω at

750W/m^2 and 15 Ω at 500W/m^2. To achieve the maximum PV power delivered to the load, the load impedance has to be equal to the PV impedance at MPP points and if that condition cannot be obtained by direct load connection, power converters have to be used. Power-converters have not only been used to convert the supplied electric power from one form to another suitable to the load requirements, they can also be used to match the impedances of the PV panel at MPPs with that of the load so that the maximum PV power can be delivered [63].

Even though implementing the MPPT increases the system complexity with regard to the use of digital computing techniques and additional transducers, many benefits can be gained such as high system efficiency hence the total cost can be reduced in some cases by 15% [64] and the efficiency improved by 16% in the worst case. Also, the system is able to generate the maximum possible power regardless of the irradiance and temperature levels [65]. Finally, employing the MPP control can be beneficial for other aspects for example, realizing storage element charging/discharging control so its life time can be extended [64].

This chapter gives a thorough and comprehensive review on the existing MPPT schemes. Their operating principles and features are reviewed along with their limitations. In Section 4.5 a new MPPT algorithm based upon the P&O scheme is proposed. Also, for the comparison purposes, simulation study is presented as well.

4.1 Basic Principle and the Simplest MPPT Scheme

Overall, the MPPT consists of three parts - a power converter, a controller (voltage or power feedback controller) and a MPPT algorithm. The latter represents the core of MPPT technique which continuously monitors the PV power and then consequently controls the power converter in order to ensure that the load works at the maximum possible PV power [65].

With respect to the controller, the voltage-feedback control is mostly used to maintain the PV terminal voltage varying about that corresponding to the MPPs. The simple voltage-feedback controller diagram is shown in Fig.4.2.

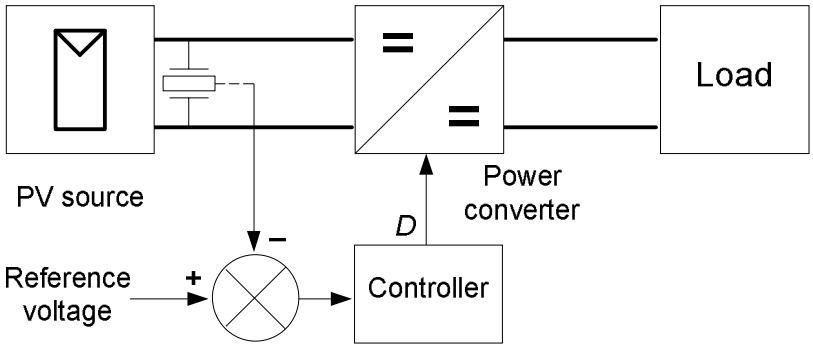


Fig.4.2: Simple MPPT system with voltage-feedback controller.

It can be noticed that in this scheme the reference voltage, i.e. the voltage corresponding to MPP has to be known and set according to predetermined measurements or the data sheet of the PV source, so this technique is called the constant reference voltage MPPT. However in practice it is difficult to obtain the reference voltage values due to changes of weather condition and data sheet may not be available. To avoid the dependency of this technique to the predetermined reference voltage, an improvement is made in order to make it more flexible specifically with respect to the atmosphere changes. The regular changes in the reference voltage due to the changes of irradiance and temperature levels are basically rely on the PV open circuit voltage which is close to the MPP PV voltage (V_{mpp} is almost 68% to 77% of V_{oc}). For every time period, the PV source and load are disconnected regularly, so the open circuit voltage can be sampled. In 1998 this method with the open-circuit voltage measurement was chosen to be used in the integrated maximum power point tracker for PV panels [66, 67]. As a result of repeatedly reset the PV source to its open-circuit voltage (PV output power is equal to zero), considerable amount of energy is lost also the system needs some time to settle down again after each interrupt. Because of that in [68] a pilot model or separated reference solar cell was used instead of interrupting the main PV power flow. Although the pilot model idea improves the system operation and increases the total extracted PV power, the main drawback is that the mismatching between the reference solar cell and the main PV panel may occur due to, for example, dust falling on the reference cell not on the main PV panel and any other different conditions differing between them. If this mismatching is neglected, incorrect information about the MPP voltage may be obtained, resulting in inaccurate or even erroneous control.

Overall, the constant reference voltage technique is a simple and inexpensive MPPT method to implement, but it may not respond to the irradiation and temperature variations correctly. Even though it has been developed to overcome the mentioned problem, it is an inaccurate and unreliable MPPT method [62, 65]. Artificial intelligence has been used to find the desired reference voltage, for instant in [69] the artificial neural networks were trained in order to predict the proper reference values in different load and atmospheric situations. As a result, the PV MPP tracking is improved. However, using the ANN needs a large number of predetermined information patterns in order to improve its feed-forward response and that requires quite long training time especially in the on-line training also it will be difficult to reduce the total squared error so inaccurate reference values are still produced. However, smaller pattern numbers results in the ANN method not being able to respond accurately to the new patterns which it had not been trained to deal with, hence it cannot lead to high performance MPPT [70].

Another simple method uses the power-feedback controller, instead of using the PV voltage as a control variable, the PV power is used to maintain the maximum PV extracted power. This strategy is characterized by the fact that the MPP is actually achieved independently of any PV source characteristics or predetermined reference values. Also, it is able to track the PV MPP efficiently regardless of any atmospheric changes, Fig.4.3 shows the simple power-feedback MPPT [65].

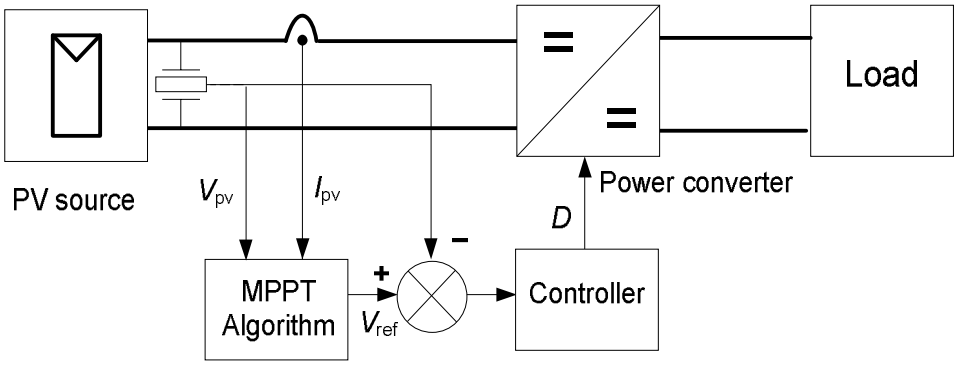


Fig.4.3: Simple MPPT system with power-feedback controller.

There have been many MPPT algorithms in the literature [71]. The most commonly used power feedback MPPT algorithms are Perturbation and Observation (P&O), Hill-Climbing (HC) and Incremental Conductance (IncCond) due to them being efficient, simple and easy to implement.

4.2 P&O MPPT Algorithm

The Perturbation and Observation algorithm is broadly used due to it is simple and easy to construct. According to the flowchart illustrated in Fig.4.4 [72], P&O method basically increases or decreases (the perturbation stage) the controller reference voltage by a step size noted as *C*, hence the PV source terminal voltage, and subsequently estimates the power difference between the present PV power and that before the perturbation (observation stage). If a positive PV power difference is obtained that means the PV power is increased and the tracking is in the right direction, the perturbation direction will be carried on (increase or decrease). On the contrary if power difference is negative, a power reduction is caused due to the perturbation, so the direction of perturbation should be reversed [72, 73].

As a result of continuous perturbation, P&O algorithm may not stop at the desired MPP voltage but oscillates around it, causing PV power loss. One way to minimize the tracking oscillation is to reduce the perturbation voltage step. As a consequence of that, in the constant irradiance state the PV power curve will be smooth with very small ripples. However, the tracking speed will detract causing more power lose and losing the ability to track certainly at the rapid atmospheric changes. Even though choosing a large perturbation step will result in achieving fast tracking response at the suddenly atmospheric changes, in the steady state the mentioned oscillation will be quite considerable [73].

Furthermore, during the transient time of a rapid irradiance change, an incorrect MPP will be tracked, and after that the actual MPP is reached [73, 75, 76]. This issue was raised for the first time in 1995 and the interpretation is that because of a perturbation step is made in a specific direction and then due to the sudden power increase, the perturbation will be kept on in the same direction as that of the previous step which may be the wrong direction of searching, consequently power loss is incurred before reaching the actual MPP [76].

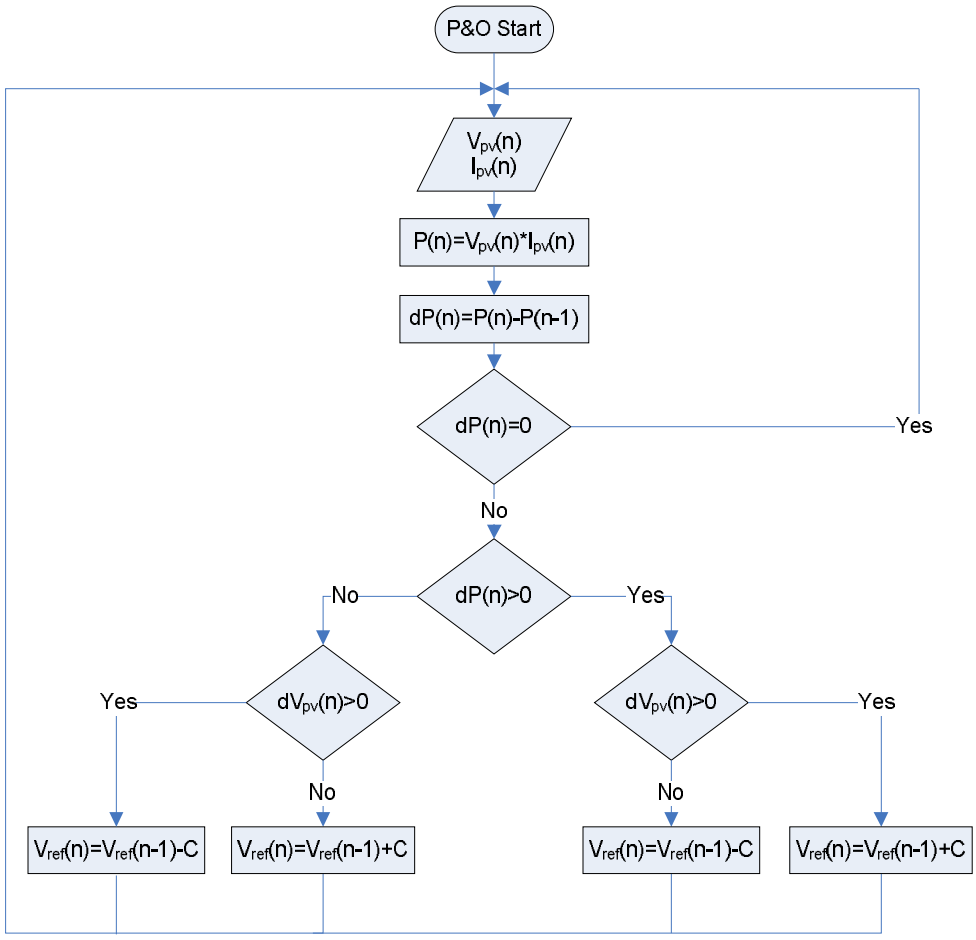


Fig.4.4: P&O algorithm flowchart.

4.3 IncCond MPPT Algorithm

The incremental conductance algorithm was introduced in 1995 in order to overcome the drawback of P&O particularly for the conditions under rapid atmospheric changes [74, 76]. As it is illustrated in Fig.4.5, the PV voltage axis can be divided into three parts. Firstly, before the MPP, the PV panel is operating as a current source. Starting from zero power at the PV short circuit voltage, the PV power is climbing with the increase of PV voltage, and therefore the slope (dP_{pv}/dV_{pv}) is positive. Secondly, at the MPP the maximum PV power is reached the PV power slope (dP_{pv}/dV_{pv}) is zero. Finally, after the MPP, the PV source is working as a voltage source, the PV power is declining with the PV voltage increase until it reaches zero power at the PV open-circuit voltage value. In this part the slope (dP_{pv}/dV_{pv}) is negative.

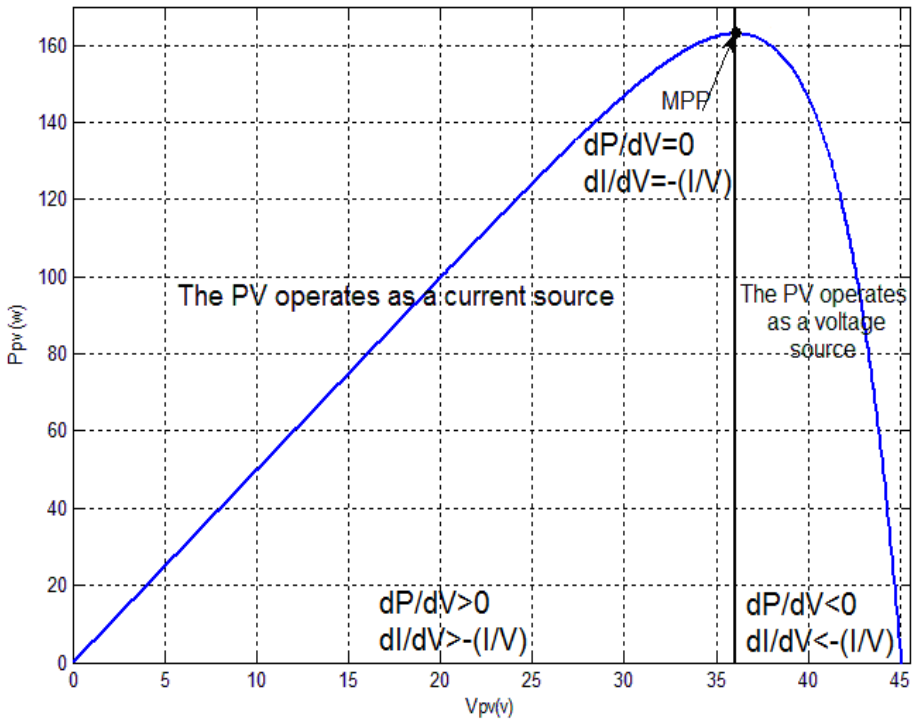


Fig.4.5: I-V PV power characteristic with dP/dV changes.

As shown in the flowchart in Fig.4.6, the IncCond algorithm modifies the reference voltage as a result of the comparison between PV source momentary and changing conductance. This concept was mainly derived from the simple power equation derivative as following [76].

$$\frac{dP_{pv}}{dV_{pv}} = \frac{d(I_{pv} \times V_{pv})}{dV_{pv}} = I_{pv} + V_{pv}\frac{dI_{pv}}{dV_{pv}} = 0 \quad \text{at the MPP}$$

$$\text{then} \quad \frac{dI_{pv}}{dV_{pv}} = -\frac{I_{pv}}{V_{pv}} \qquad \ldots\ldots (4.1)$$

It is clear in the algorithm, if there is not PV voltage change, the PV current has to be checked in order to detect the irradiance changes.

This method is claimed not causing the miss-tracking of the MPP during the irradiance change time as that when P&O is used, so more efficient in reaching the MPP can be achieved. However, in [73] the simulation result showed that the IncCond still getting lost during the rapid irradiance changes. Moreover, the oscillation at the steady state will not be suppressed because equation 4.1 cannot be actually satisfied at the MPP. In order to overcome this limitation, a small amount of

error was acceptable [76]. In addition to that, comparing with P&O algorithm, IncCond algorithm requires more computational effort [73].

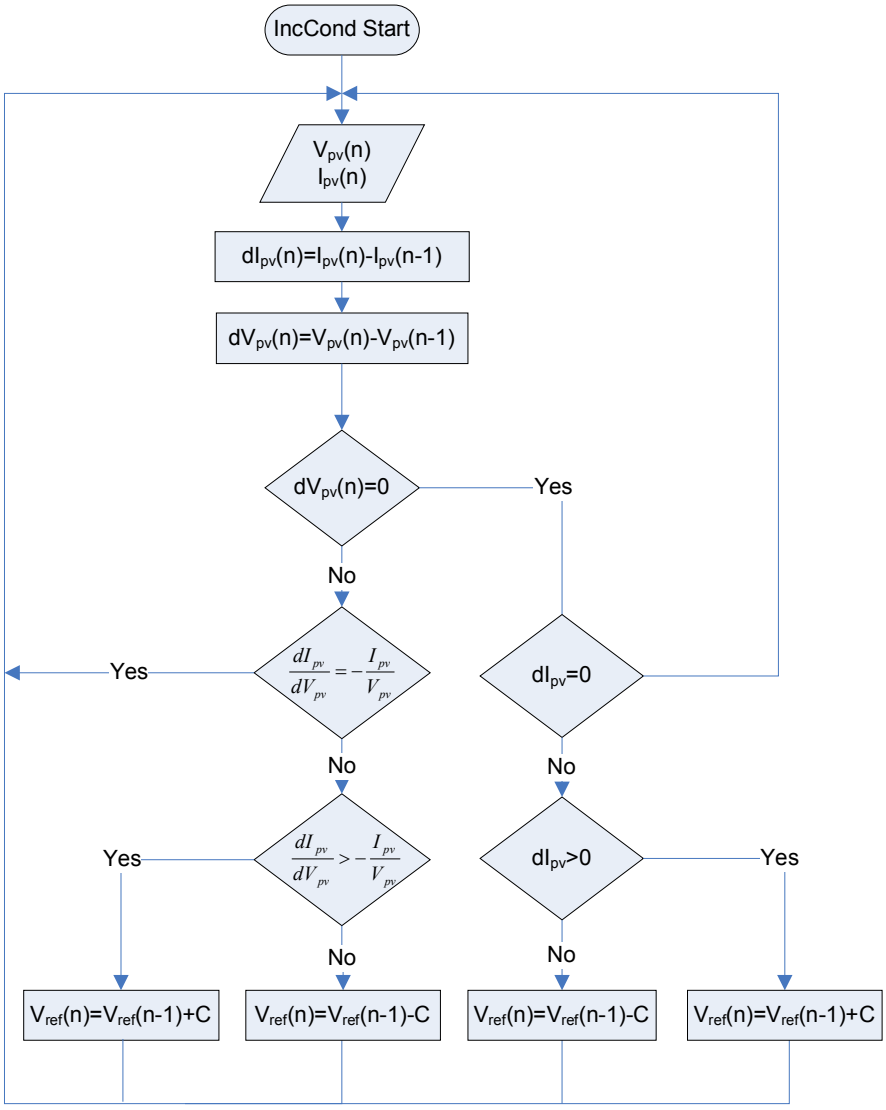


Fig.4.6: IncCond algorithm flowchart.

As claimed in [74], the given experimental results showed that, the efficiencies for MPP searching by the both P&O and IncCond are worse than that was accomplished by using the model-based constant reference voltage method under irradiance up to 30% even though the latter has its drawbacks. For this reason, a new algorithm based on IncCond and constant reference voltage method was introduced in [74]. The algorithm compares the irradiance level as a first condition to decide which algorithm is going to be used to track the MPP. This has resulted in achieving higher efficiency at low irradiance intensity, but additional transducer has to be employed.

4.4 Hill-Climbing MPPT Algorithm

The both P&O and IncCond are based on the adjustment of the reference voltage (V_{ref}) in order to reach the MPP at which dP/dV=0. However, as it is illustrated in Fig.4.7, Hill-Climbing MPPT algorithm adjusts the power converter duty ratio (D) directly instead of using a voltage controller for achieving that. According to Fig.4.8 the switching duty ratio adjustment (buck converter) will be carried on by the HC algorithm until the MPP is achieved. Also, as can be seen in Fig.4.9 at the MPP, dP/dD is equal to zero [75].

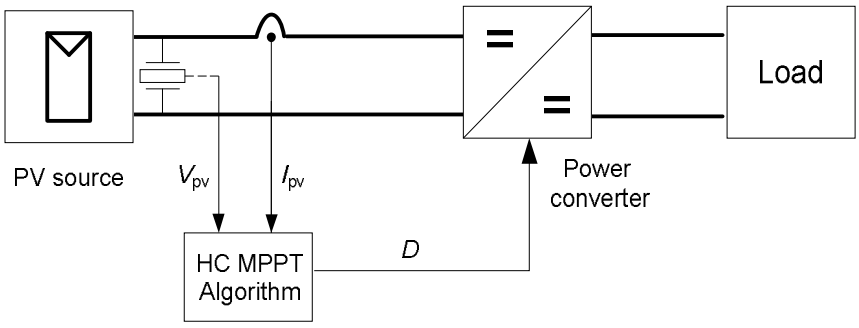


Fig.4.7: Simple MPPT diagram using HC algorithm.

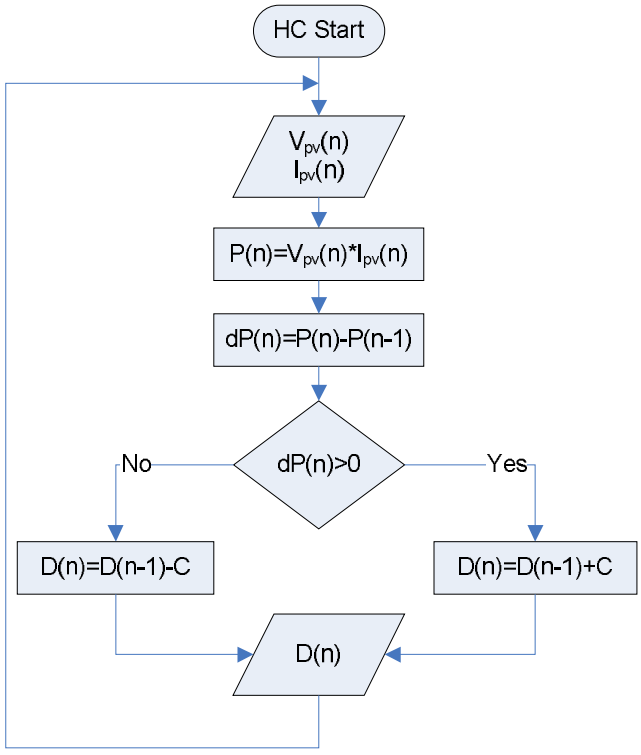


Fig.4.8: Hill-Climbing algorithm flowchart.

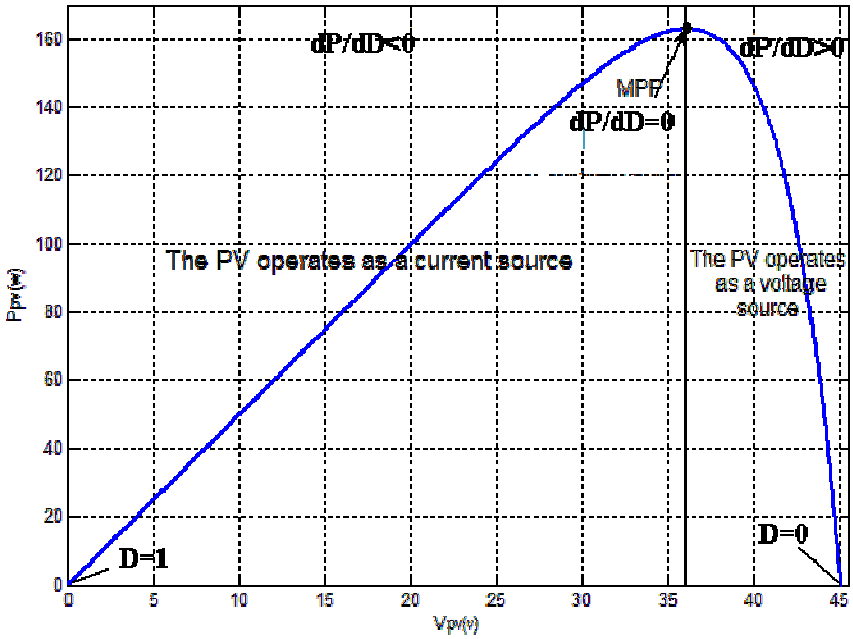


Fig.4.9: PV power characteristic with d*P*/d*D* changes "buck-converter".

The HC algorithm illustrated in Fig.4.8 is used in [64] with a buck-boost converter. The PV power curve given in [64] shows that the tracking process started from the right of the peak power point to the left which means from D=0, when V_{pv} equals to the PV open circuit voltage, to the desired MPP duty ratio. This is because the opposite is not allowed as a consequence of the algorithm limitation. If the algorithm started from the left of the MPP point, in order to reach the MPP, the switching duty ratio has to be decreased at every step. However, according to the HC algorithm shown in the flowchart in Fig.4.8 it will be increased instead.

This unidirectional tracking is not able to cope with the changes of weather condition. In order to find the new MPP when the irradiance level changes the tracking may start from a point which is on the left of the new MPP (lower than previous V_{MPP}). As it can be seen in Fig.4.10, a slope of '-1' is applied in [77] in order to increase D overcome the mentioned drawback, so the tracking can be implemented in both directions.

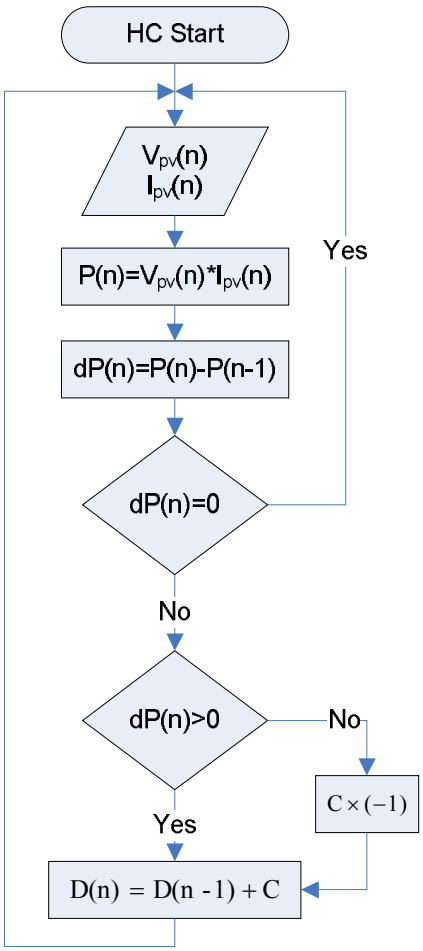


Fig.4.10: Adaptive Hill-Climbed algorithm flowchart.

The simulation results in [75] confirmed that the adaptive HC algorithm can lead the PV output power oscillating around the MPP. Also, during the quick irradiance variations, the PV terminal voltage exceeds the desired MPP voltage under the new weather condition; before finding it. Therefore, it is fair to say that the HC algorithm may not be able to track the MPP within the sudden atmospheric variation time interval.

A comparison was done in 2008 in order to find out which algorithm, P&O or HC, gives quicker response regarding MPPT for a grid-connected PV system. The particular PV system consists of a DC/DC boost converter, a DC/AC inverter, an MPPT algorithm and controllers. The Matlab-Simulink was used to simulate this PV system. The comparison of the simulation results was carried out by imposing identical PV voltage amplitude adjustments on each algorithm in order to ensure that both of them operating at the same conditions. The results illustrated that P&O

algorithm performed better showing a quicker response and more uniformed PV terminal voltage than HC algorithm regarding the rapid atmospheric variations [78].

4.5 The Voltage-Hold P&O (VH-P&O) MPPT Algorithm

The problems occurring during MPPT can be summarized as two; voltage oscillations around a MPP and losing the MPP during the atmospheric changes. The first arises from continuous perturbation and therefore the MPPT algorithm does not stop at the desired MPP voltage, but oscillates around it, hence causing power loss. With respect to the second limitation, during the transient time of irradiance change, an incorrect MPP is tracked. This thesis proposes an algorithm for tracking the maximum power point of a PV source which is based on the voltage-hold perturbation and observation tracking of the maximum power point during atmospheric changes. The algorithm overcomes the major tracking limitations and produces improved results compared with the standard MPPT algorithms which were reviewed in the last sections.

The proposed algorithm is mainly based on the conventional P&O algorithm. The idea was originated by finding that the cause of the wrong MPP tracking during irradiance changes is due to the poor synchronization between the MPPT algorithm, the controller and the system response (V_{Cpv}). For instance, during the irradiance changes the system is forced to follow the reference voltage of MPP algorithm, which does not match with the current practical voltage across the PV capacitor (C_{pv}). The latter is related to the increased/decreased generated PV current (dependent on irradiance) and there is delay between the desired reference voltage and the corresponding controller duty ratio which results in 'confused' tracking behaviour within the transition time.

The proposed VH-P&O algorithm stops the conventional perturbation process during a sudden irradiance changes which can be detected by measurement of power change, but setting the reference voltage to the measured PV capacitor voltage which is the essential tracking parameter in this algorithm. Subsequently the algorithm resumes the perturbation process for searching the MPP voltage along the new I-V characteristic curve. For overcoming the problem of oscillating around the MPP, the new algorithm uses variable searching step size. As soon as the irradiation change

stops, the tracking step size is decreased gradually down to zero when close to MPP. This is implemented by dividing a factor A as shown in the algorithm flowchart shown in Figure 4.11. Afterwards, if any PV power change occurs, the tracking step size will be reset to the initial value and therefore fast tracking is maintained. Through this algorithm, the PV response of a change of irradiance results in a straight-line tracking behaviour which is fast accurate and with suppressed oscillation at the MPP. Fig.4.11 illustrates the flowchart of the proposed algorithm.

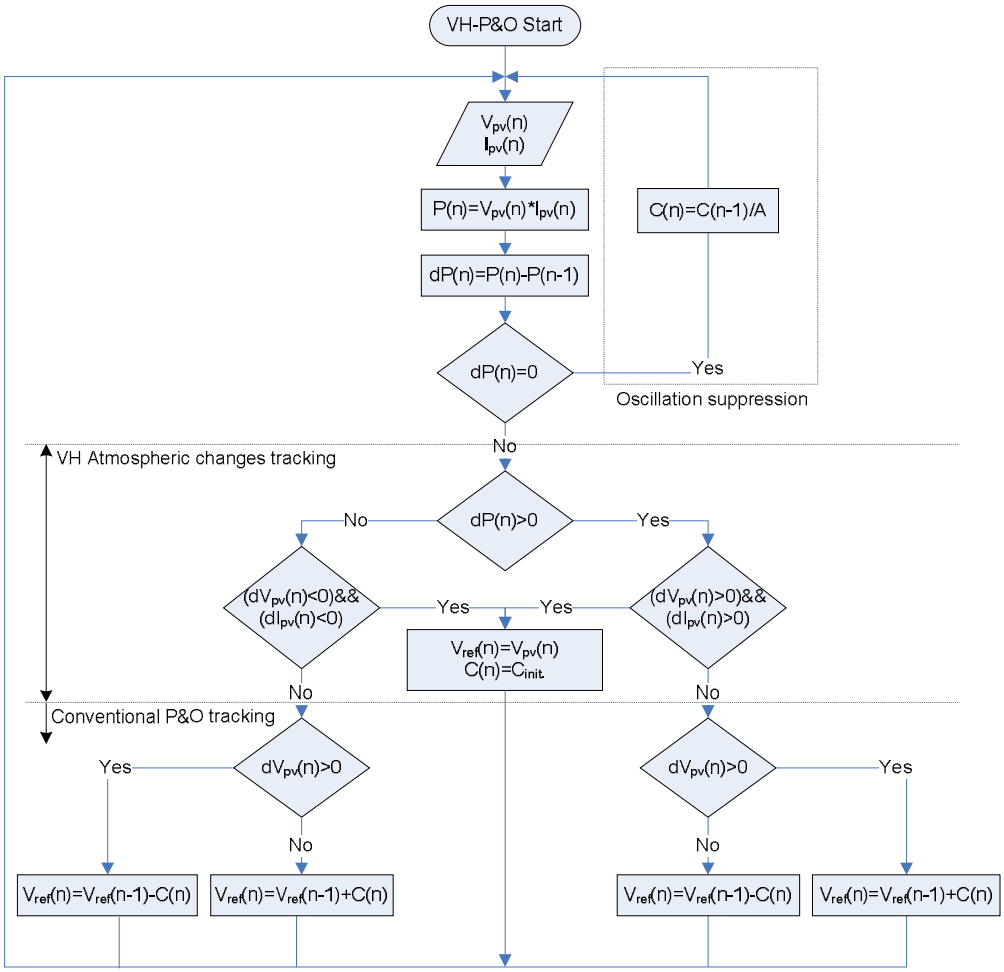
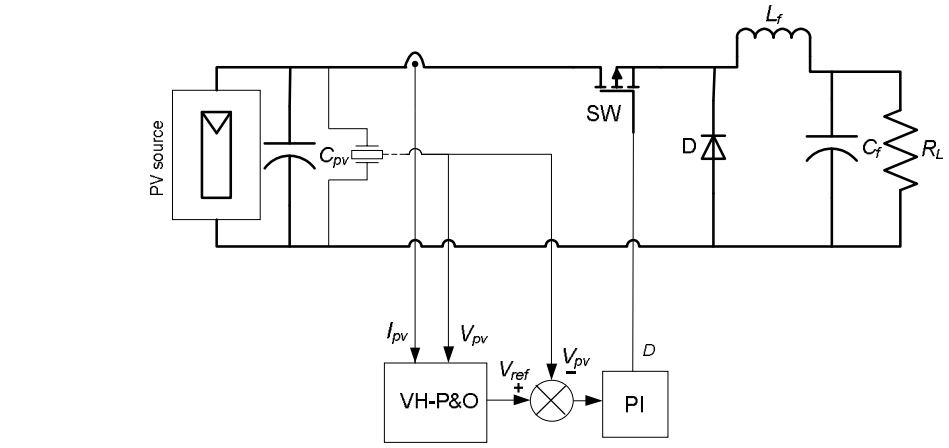


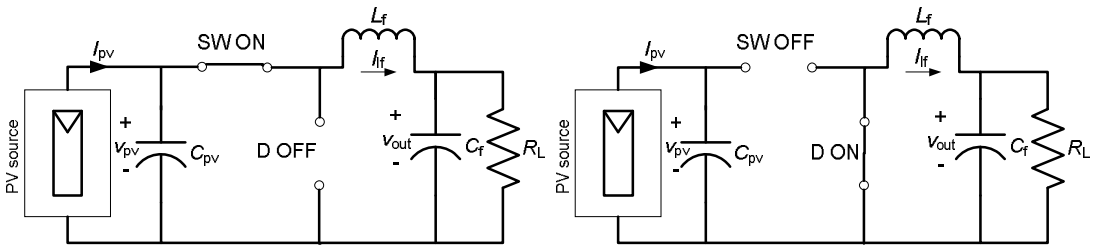
Fig.4.11: The proposed VH-P&O MPPT algorithm.

4.6 MPPT Simulation and Comparison

Matlab-Simulink program is utilized to simulate the proposed algorithm. In this the algorithm is written in a script file and enclosed in an Matlab Sfunction block (VH-P&O block in Fig.4.12a), so it is easy to be linked with the other parts of the simulation program and also for comparing with the other algorithms. The simulated PV system in Fig.4.12a uses a buck-converter as the DC/DC power conditioner. In order to analyse the system transient and steady-state behaviours under different operating conditions, the state-space averaging (SSA) model, which has been introduced in [31], is used. Fig.4.12b illustrates the schematic of the PV system and the buck-converter circuit at both switching on and off states.



(a)



(b)

Fig.4.12: Buck-converter (a) PV simulated system and (b) on/off states.

The buck-converter mathematical model can be achieved by writing the circuit state-space equations as follows:

$$i_{pv} - C_{pv}\frac{dv_{pv}}{dt} - S \cdot i_{L_f} = 0 \qquad \ldots\ldots \quad (4.2)$$

$$i_{L_f} - C_f \frac{dv_{out}}{dt} - \frac{v_{out}}{R_L} = 0 \qquad \ldots\ldots \quad (4.3)$$

$$v_{out} - S \cdot v_{pv} + L_f \frac{di_{L_f}}{dt} = 0 \qquad \ldots\ldots \quad (4.4)$$

The switch state (S) can be replaced with the switching duty ratio (D). The final form of the mathematical model (equation 4.5) is achieved after organizing equations 4.2-4.4 by substituting.

$$\begin{bmatrix} \frac{dv_{pv}}{dt} \\ \frac{dv_{out}}{dt} \\ \frac{di_{L_f}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-D}{C_{pv}} \\ 0 & -\frac{1}{C_f R_L} & \frac{1}{C_f} \\ \frac{D}{L_f} & -\frac{1}{L_f} & 0 \end{bmatrix} \begin{bmatrix} v_{pv} \\ v_{out} \\ i_{L_f} \end{bmatrix} + \begin{bmatrix} \frac{1}{C_{pv}} \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} i_{pv} \end{bmatrix} \qquad \ldots\ldots \quad (4.5)$$

where D denotes the switching duty ratio.

4.6.1 P&O MPPT Simulation Results

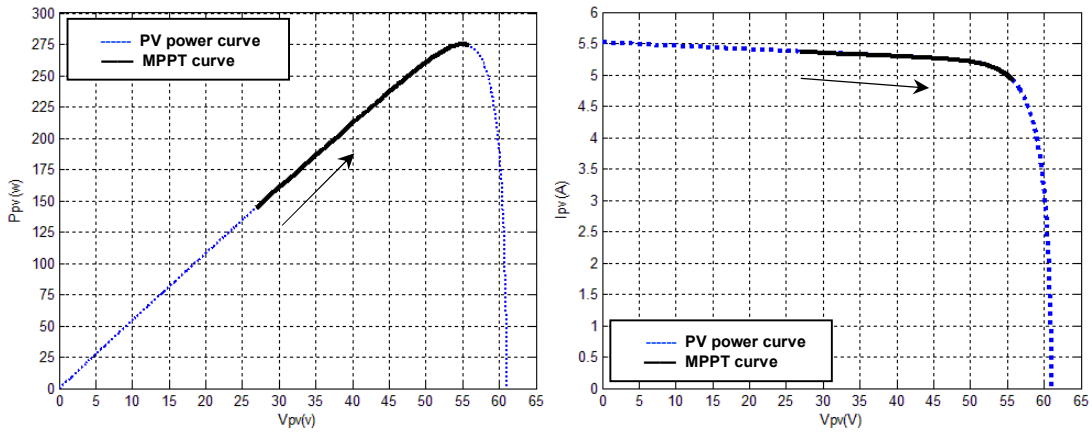
In order to show the superior performance of VH-P&O method, the conventional P&O method is simulated first to show its limitations. The following Figures 4.13-4.18 illustrate the system response with respect to P&O MPPT algorithm and at irradiance of 1000 W/m^2. The system parameters used in this study are shown in Table 4.1.

TABLE 4.1: PV System Parameters (MPPT)

V_{oc}	61V	C_{pv}	400μF	Initial D	1
I_{sc}	5.5A	C_f	800μF	K_p	0.01
V_{mpp}	55V	L_f	2mH	K_i	100
I_{mpp}	5A	R_{pv}	11Ω	R_L	5Ω
P_{mpp}	275W				

Figure 4.13 shows both P-V and I-V curves and the searching direction. Under constant irradiance and starting with an initial switching control duty ratio of 1, the required tracking time in order to reach the desired MPP duty ratio (0.67) was about 0.075s. The elapsed time before getting the MPP is mainly based on the system

parameters and also, as mentioned before the algorithm perturbation step size "*C* or *dv*" which has been set to 0.5 V.



(a) (b)

Fig.4.13: The MPPT curve shown via (a) PV power curve and (b) PV I-V curve.

Fig.4.14 shows the duty ratio variations. As can be seen, there is oscillation around the MPP duty ratio and that is due to the continuous perturbation of 0.5 V step change of reference voltage. The extracted PV power is illustrated in Fig.4.15; the PV power ripple can be also minimized by increasing the PV bypass capacitor C_{pv}. However, the system response will be affected.

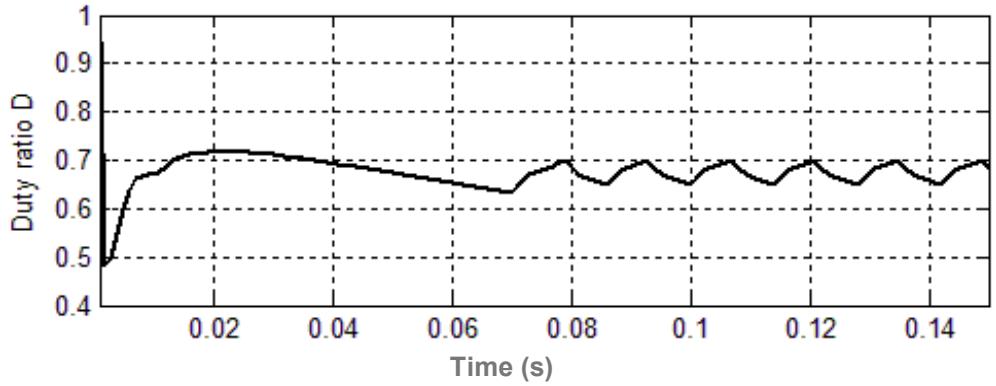


Fig.4.14: The switching duty ratio and the PV power-difference responses.

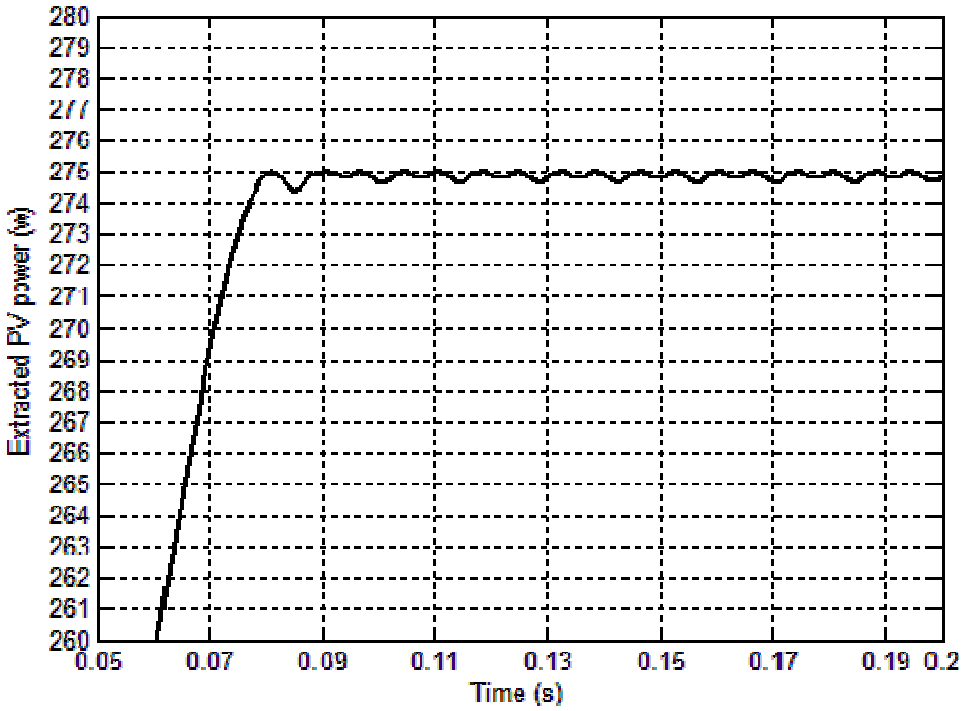


Fig.4.15: Extracted PV power waveform.

Figures 4.16 and 4.17 show the voltage and current waveforms respectively for both PV and the output passive load.

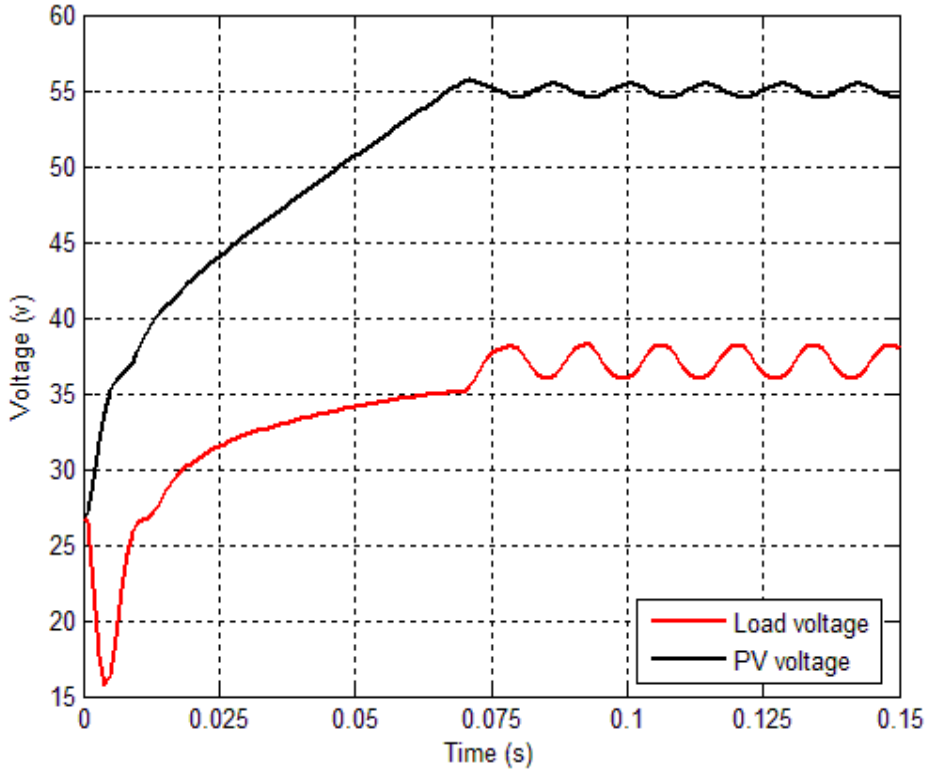


Fig.4.16: Power converter input and output voltage waveforms.

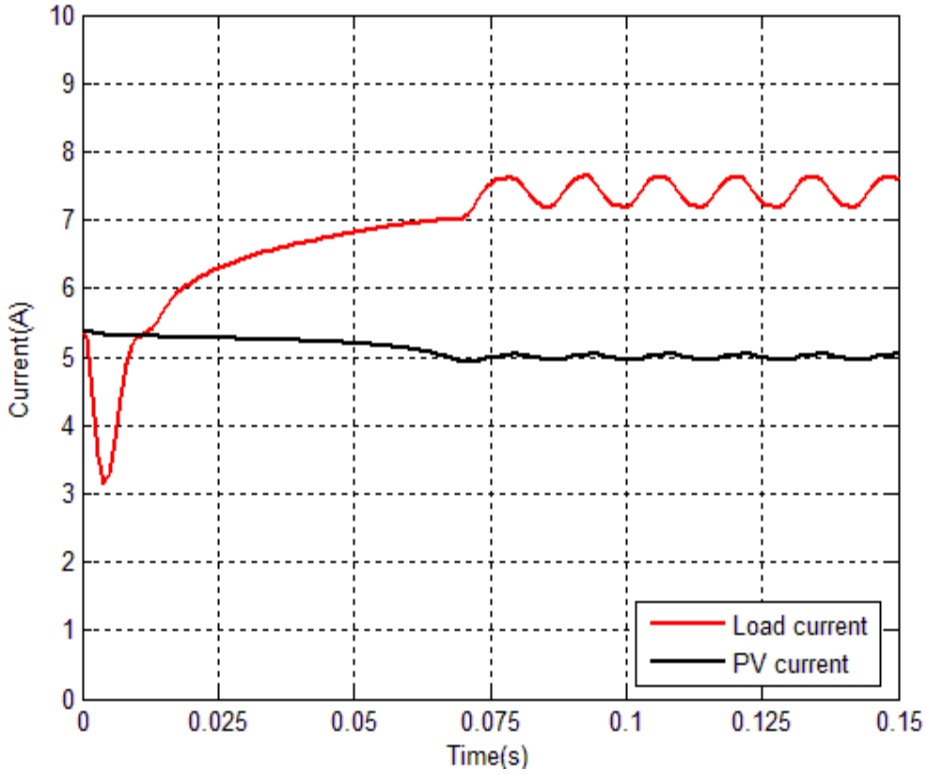


Fig.4.17: Power converter input and output current waveforms.

The Figures 4.18-4.20 show the system response with respect to the gradual irradiance changes. As shown in Fig.4.18, there has been a gradual increase in the switching control signal duty ratio as a consequence of an insolation change from 600 W/m^2 to 1000 W/m^2 within a time period of 0.5s. The tracking has been done with 0.5 V perturbation step size and load resistance of 2.75Ω.

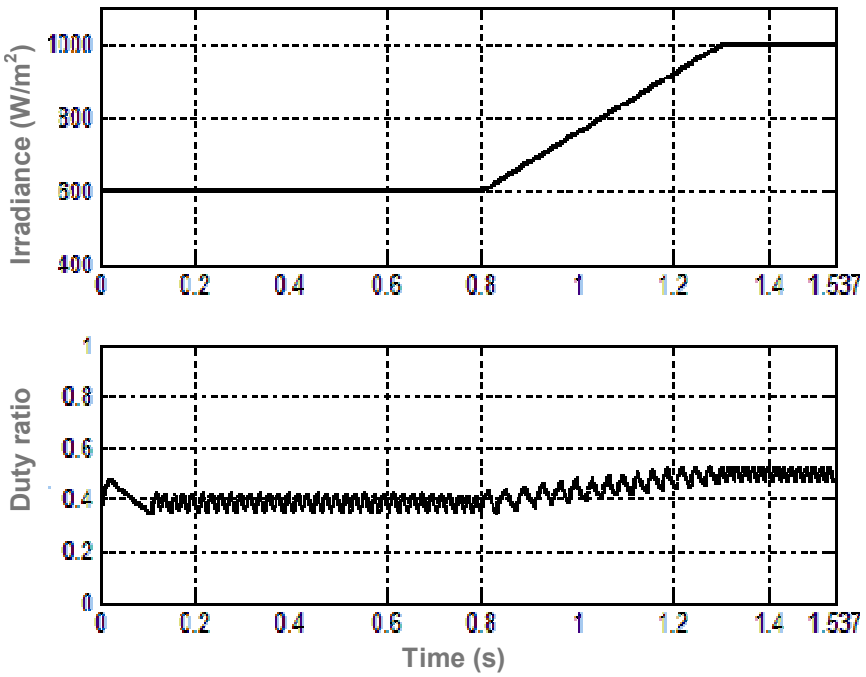


Fig.4.18: Irradiance and switching duty-ratio waveforms.

The gradual atmospheric variation effect can be illustrated from other sides; Figures 4.19 and 4.20 clearly illustrate the associated oscillation regarding the PV current and power respectively.

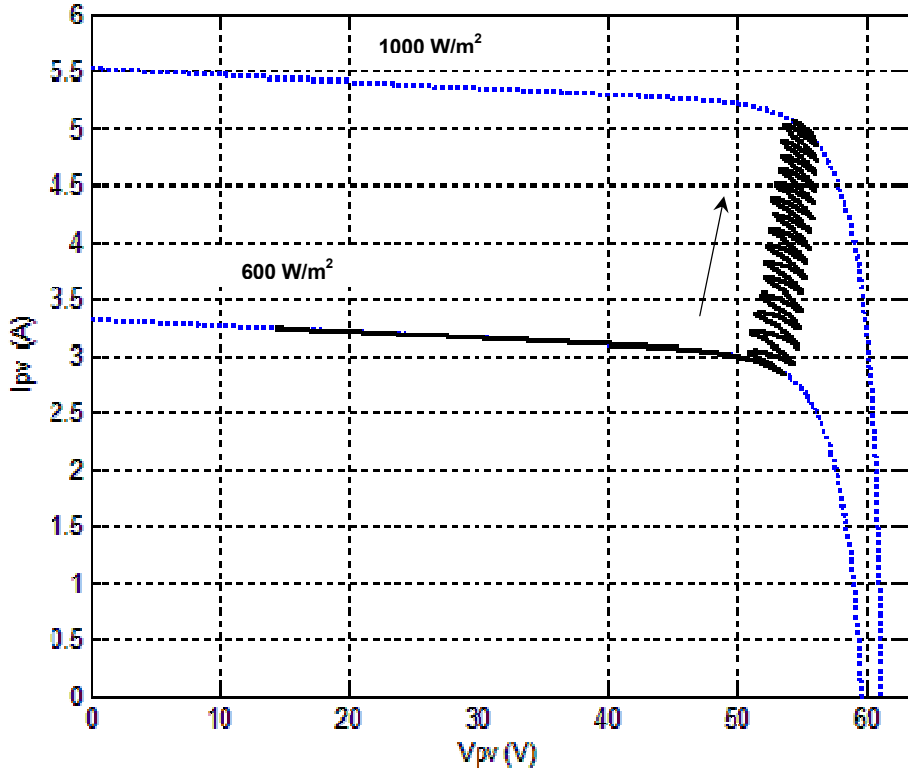


Fig.4.19: PV I-V tracking curve as a result of slow irradiance changes.

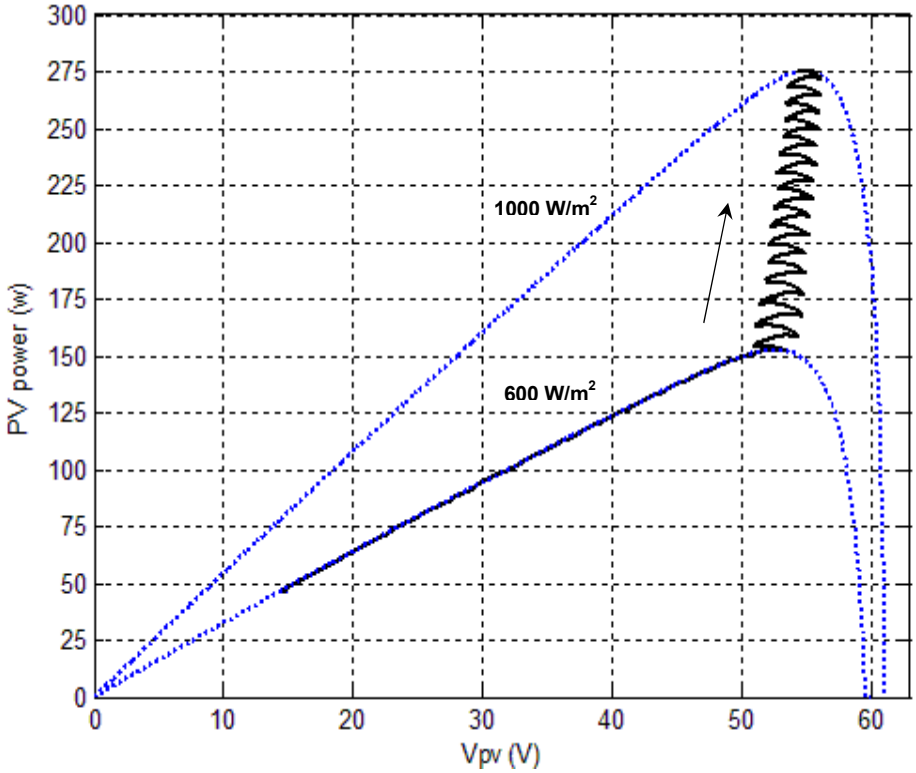


Fig.4.20: PV power tracking curve as a result of slow irradiance changes.

In order to show the performance of the method under sudden atmospheric changes, the irradiance signal which changes from 200 W/m^2 to 1000 W/m^2 and then 500 W/m^2 as shown in Fig.4.21 and is applied to the PV source. The PV voltage, current, extracted power waveforms are also shown in the same Figure.

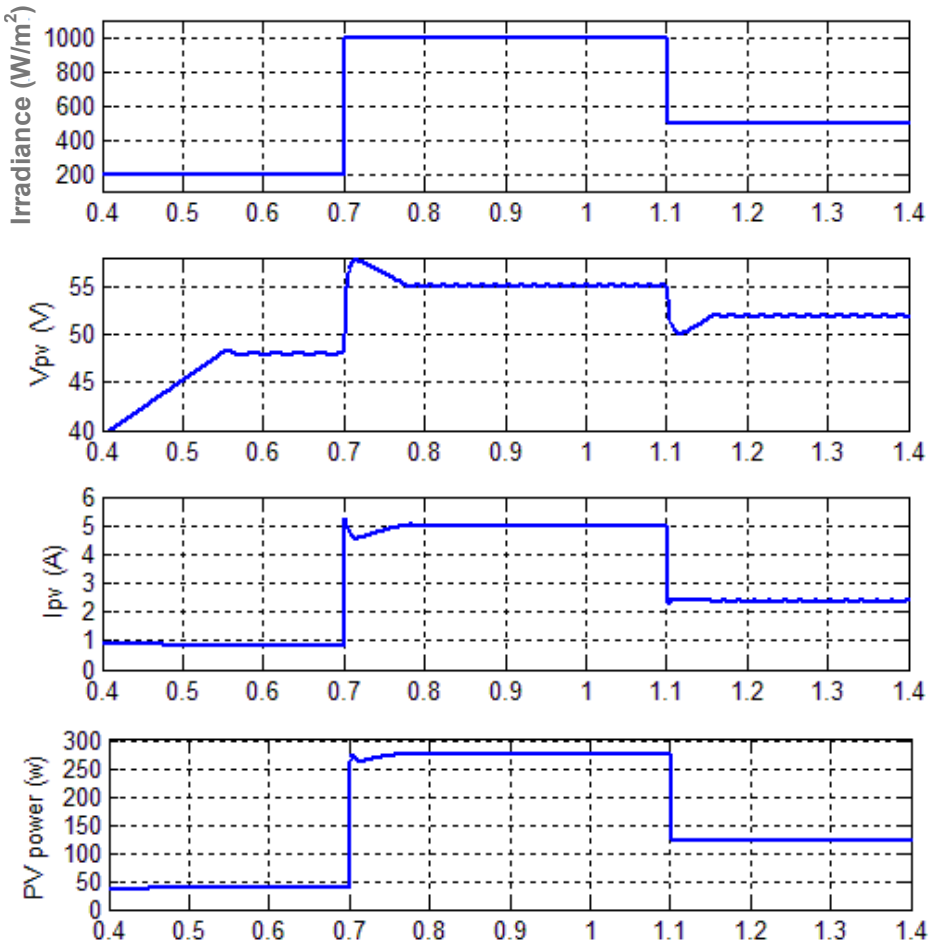


Fig.4.21: PV voltage, current, power, impedance and duty ratio waveforms under rapid irradiance changes.

It can be seen that when the irradiance level changes from 200 W/m^2 to 1000 W/m^2, the algorithm does not find the MPP initially and the voltage diverted from the MPP voltage (55 V), so a power reduction is caused at time point 0.7 second. The bypass capacitor minimizes the instantaneous effect of the voltage deviation as presented in the power waveform.

The resultant tracking curves are also shown using the I-V and the power curves in Figures 4.22 and 4.23 respectively. The MPP tracking has been achieved by 0.1 V perturbation step size and load resistance of 2.75 Ω.

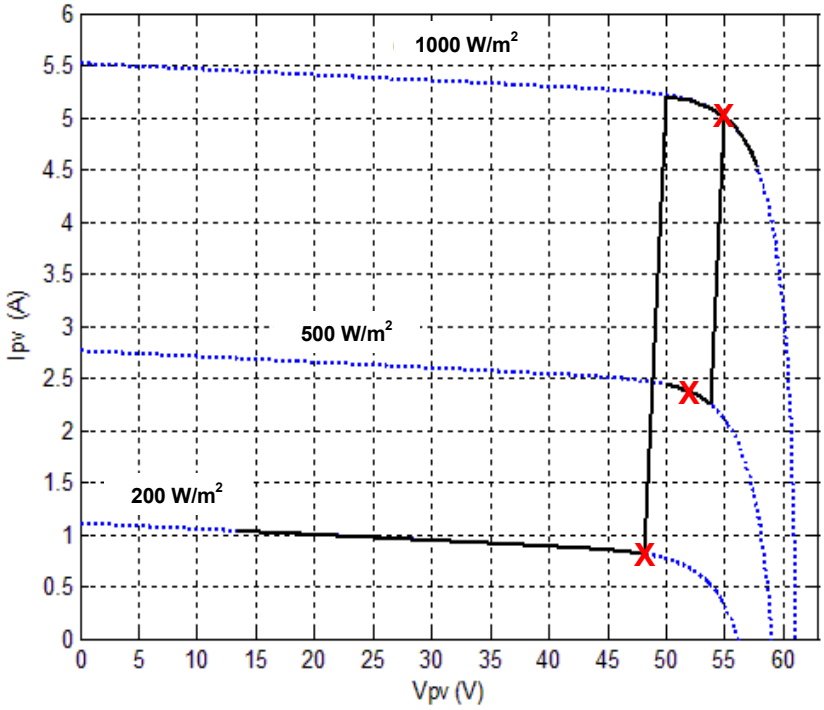


Fig.4.22: PV I-V tracking curve as a result of rapid irradiance changes.

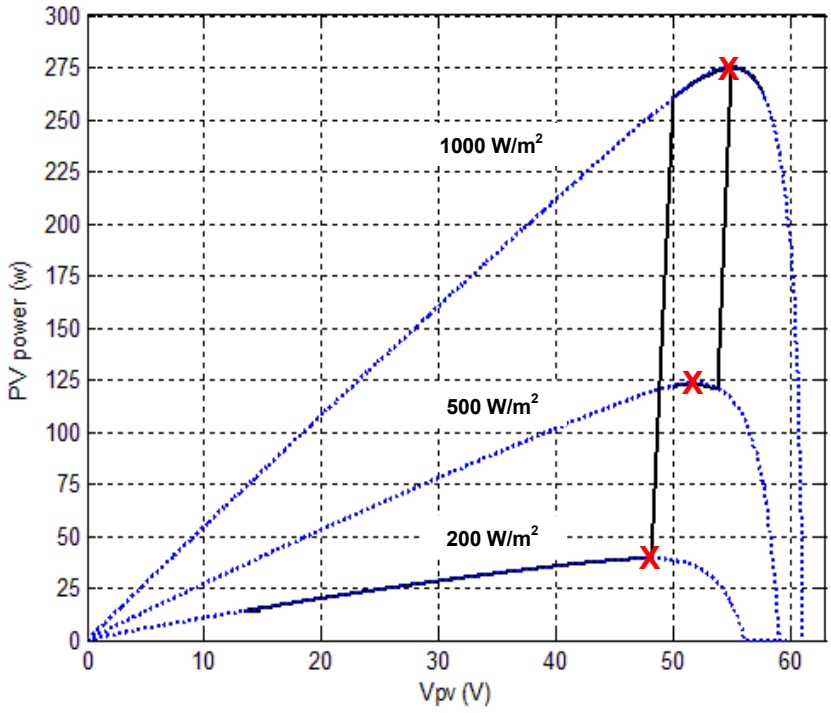


Fig.4.23: PV power tracking curve as a result of rapid irradiance changes.

Both diagrams show clearly that the algorithm tracked away from the MPP, denoted as 'X', when sudden change of irradiance level happens.

As have been mentioned the tracking speed of the P&O is determined also by the voltage step size. Fig.4.24 is accomplished under constant irradiation level of

1000W/m^2 and load resistance of 2.75Ω. The P&O algorithm spent much more time with C=0.1 in order to reach the MPP voltage than that was spent with C=0.5. However, the oscillation which is around the MPP voltage is higher with C=0.5 than that was achieved with C=0.1.

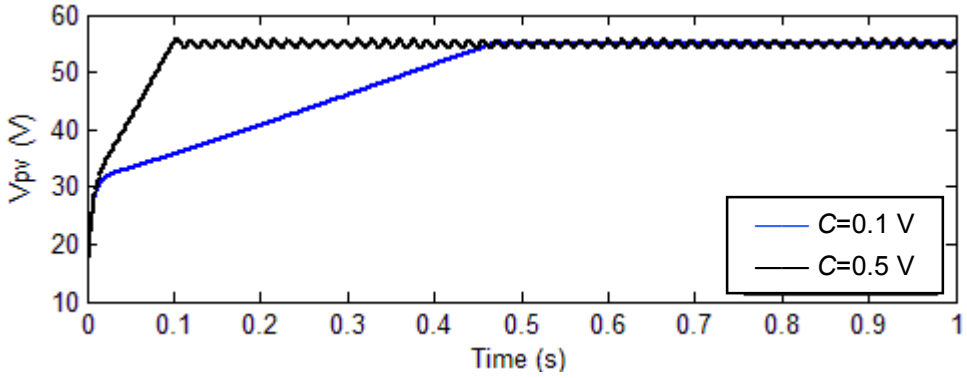


Fig.4.24: PV voltage waveform with different perturbation step size.

4.6.2 Simulation of VH-P&O MPPT and Comparison with the other Algorithms

Simulation of VH-P&O method has been carried out for the same condition and PV panel as that for the P&O case. As a contrast to P&O, the PV voltage and power waveforms shown in Fig.4.25a and Fig.4.25b confirm that VH-P&O algorithm does not cause any oscillation around the MPP at the steady-state time (G=1000 W/m^2).

The slow atmospheric changes are also a serious problem for all the existing tracking methods, because the period of power reduction due to algorithm searching for MPP or wrong tracking can extend for a long time period. On the contrary, the VH-P&O method performs significantly better than all the others. This is shown in the simulation by comparing the responses of the algorithms. The irradiance change is ramped up from 200 W/m^2 to 1000 W/m^2 within a time period of 0.3s (similar to Fig.4.18) is applied to the PV system using the conventional P&O and the VH-P&O. Fig.4.26 shows the resulting power tracking curves.

The drawback of wrong tracking response to the irradiance change, which occurs in conventional P&O algorithm, can be seen in Fig.4.26a. However, in Fig.4.26b which relates to the proposed VH-P&O algorithm, there is no power oscillation and therefore the power loss is minimized.

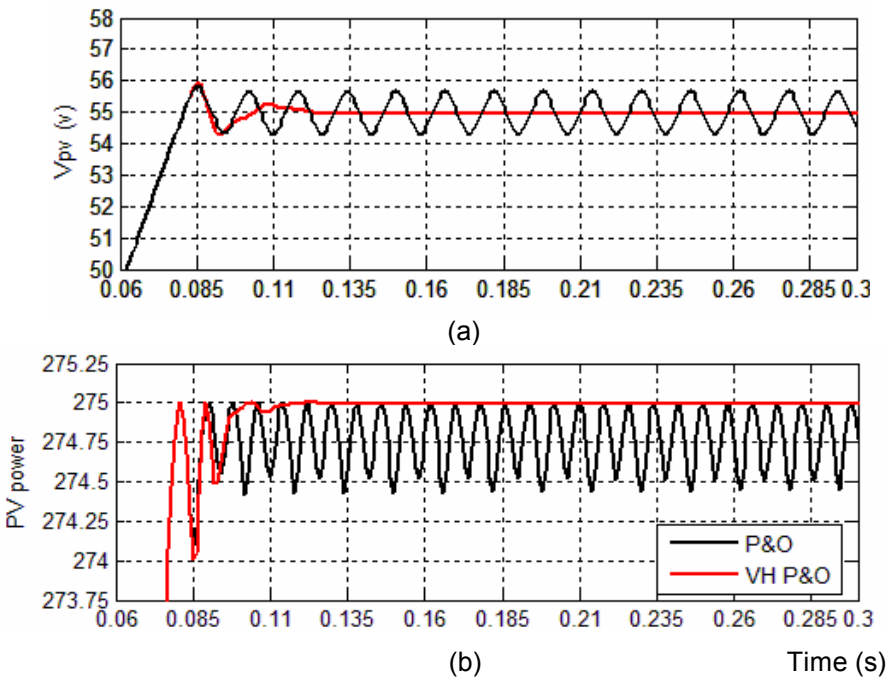


Fig.25: P&O and VH-P&O MPPT (a) voltage and (b) power waveforms.

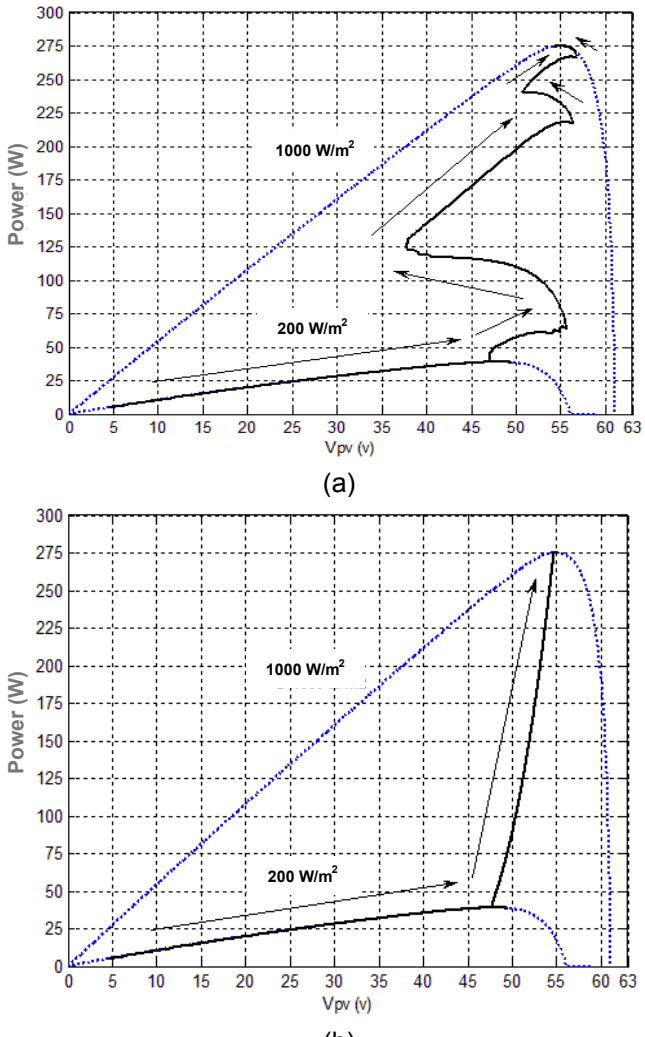


Fig.4.26: Power tracking curves of (a) P&O and (b) VH-P&O algorithms.

The simulated system responses to the rapid changes of irradiance are shown in Fig.4.27, where the PV voltage waveforms are given for both P&O and VH-P&O algorithms. For the latter, the deviations from the MPP voltage at the transition intervals are small. In contrast the P&O method gives oscillatory tracking path which is not acceptable.

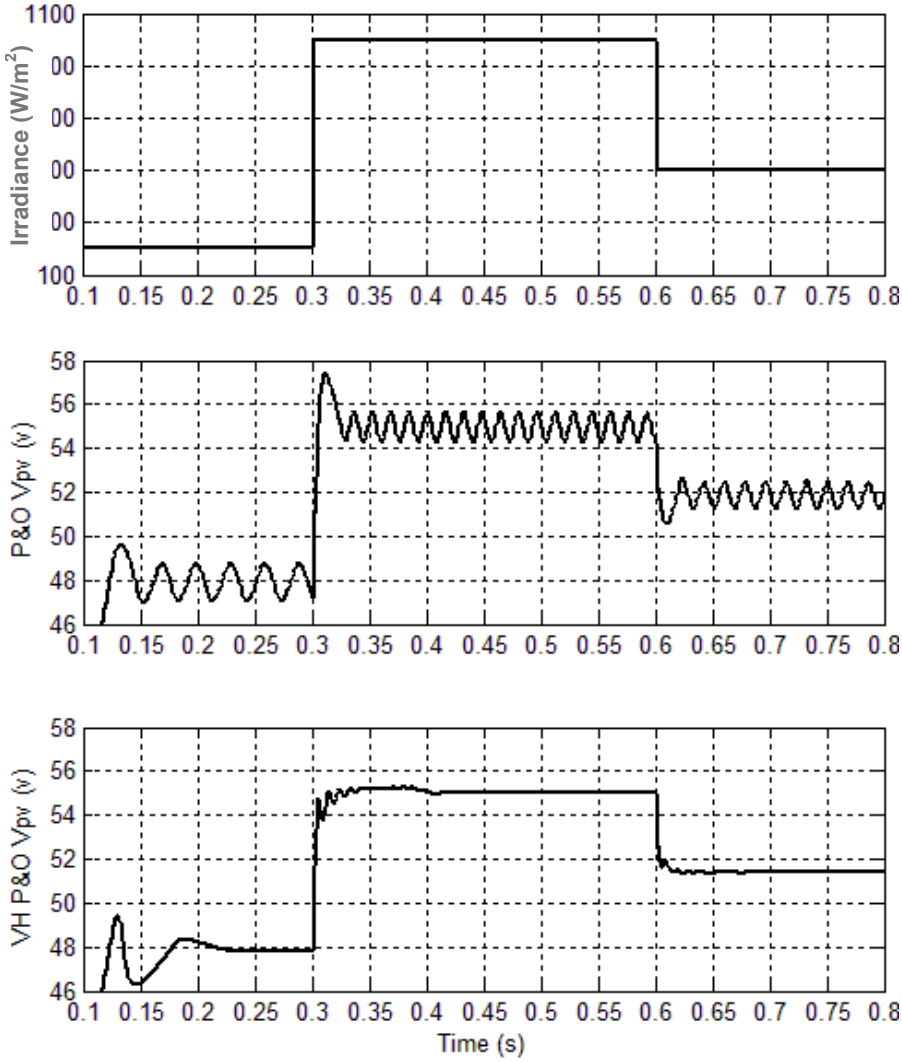


Fig.4.27: P&O and VH-P&O MPPT PV voltage waveforms as result of applying rapid irradiance changes.

The tracking curves for all four algorithms, P&O, IncCond, HC and VH-P&O MPPT, are illustrated in Figures 4.28-4.31 by using 3D graphs. The applied irradiance has been ramped up from 200 W/m^2 to 1000 W/m^2 within a time period of 0.5s.

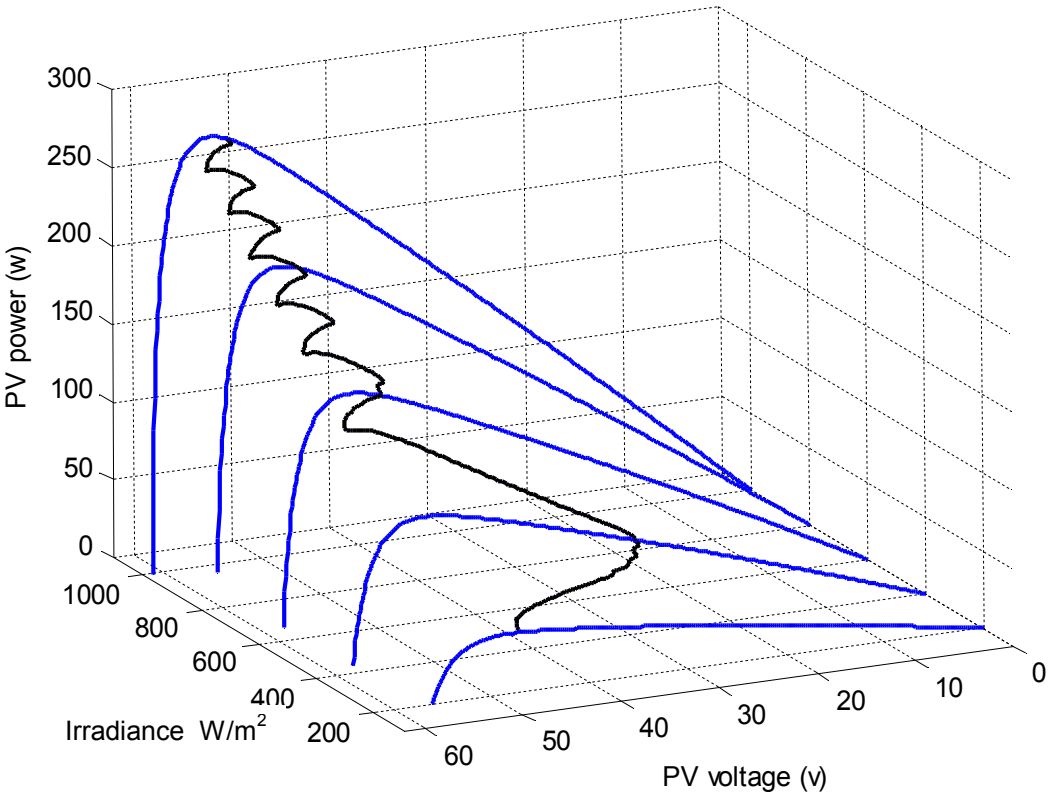


Fig.4.28: 3D PV power tracking curve (P&O MPPT, C=0.5, R_L=2.75Ω).

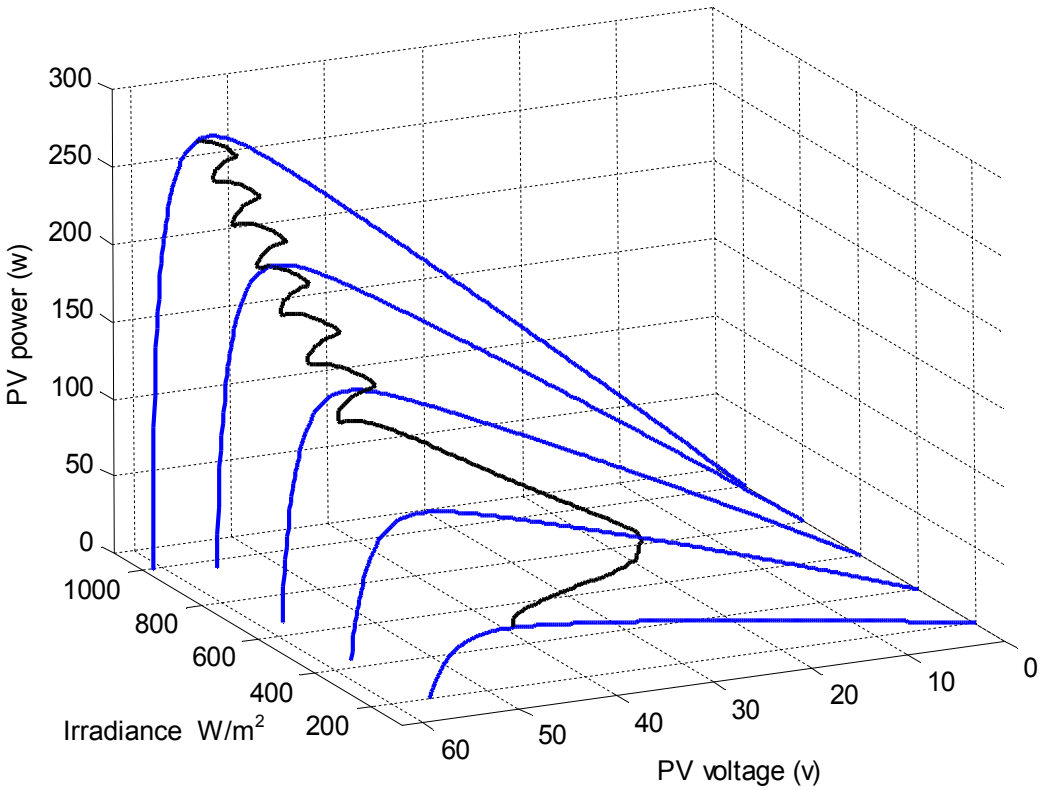


Fig.4.29: 3D PV power tracking curve (IncCond MPPT, C=0.5, R_L=2.75Ω).

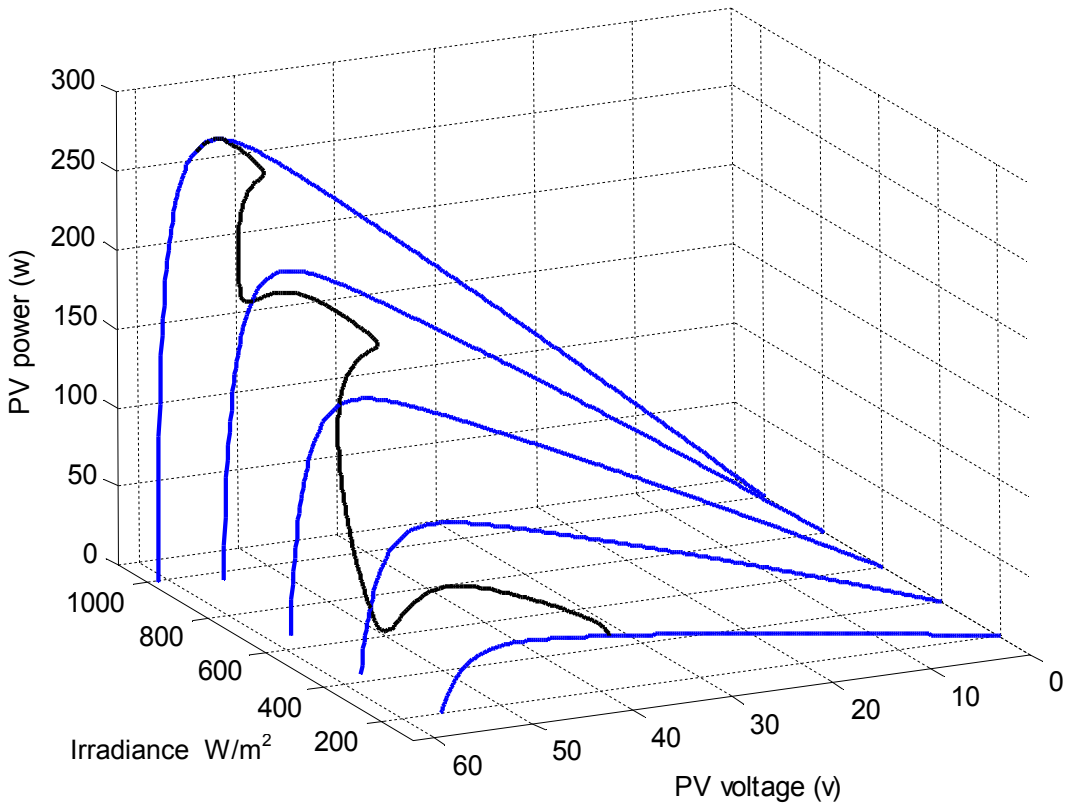


Fig.4.30: 3D PV power tracking curve (HC MPPT, C=0.0015, R_L=2.75Ω).

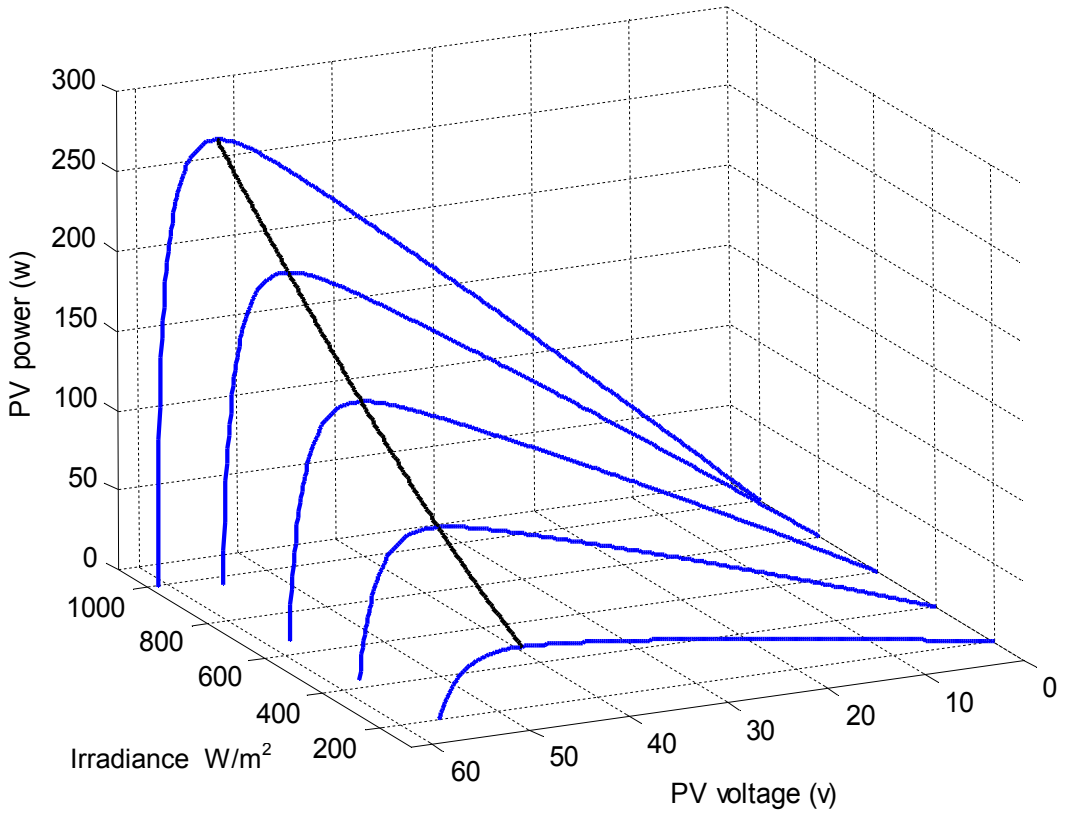


Fig.4.31: 3D PV power tracking curve (VH P&O MPPT, C=0.5, R_L=2.75Ω).

As is noticeable, the results which are achieved by using the IncCond algorithm are similar to those achieved by P&O algorithm, and that confirms the results which have been accomplished in [73].

Slow and poor tracking performance is obtained by the HC algorithm. The step size of C=0.0015 defines that of the duty cycle. This is the minimum value that still enables reaching the MPP within the interval of irradiance change (0.5s), with a penalty of producing a large steady-state oscillation (3V peak-to-peak) around MPP voltage. In addition, due to not using the PI controller in HC method it results in instability during the irradiance changes. A large deviation from the desired MPP occurs especially at rapid irradiance changes.

In contrast as shown in Fig.4.31 VH-P&O algorithm outperforms all the other three in that it can track directly the MPP points within the transient weather changing period with no tendency of diverting away to the wrong power point.

4.7 Summary

In this chapter, three commonly used MPPT algorithms, which are perturbation and observation (P&O), Hill-Climbing (HC) and Incremental Conductance (IncCond), were discussed in details, along with their limitations. MPPT limitations such as the oscillation around the maximum power point as well as losing the maximum power point during the irradiance changes were highlighted and illustrated via simulation results.

In order to extract the maximum possible PV power under different atmospheric variations and overcoming the tracking limitations, “voltage-hold perturbation and observation” (VH-P&O) algorithm was introduced. The PV system was mathematically modelled and controlled using this new proposed algorithm, the simulation results under different irradiance changes were compared with all the conventional algorithms. It is shown that VH-P&O algorithm gives the best performance in terms of low oscillations and correct and fast MPP tracking. This algorithm will be applied experimentally.

Chapter 5

Multilevel DC-Link Inverter to Overcome the PV Partial Shading

This chapter presents the modelling of the PV multilevel DC-link inverter system introduced in Chapter 3 as well as the simulation results achieved under symmetrical irradiance. The use of the this system to overcome the PV partial shading problem is introduced. Control algorithms to extract the maximum power from each PV source to the load under such conditions are presented. Also, a method for improving the inverter waveform quality is discussed.

5.1 State Space Averaging (SSA) Model

In order to simulate the DC-link inverter system and test its dynamic characteristics as well as the response under constant and variable partial shading conditions, the circuit model needs to be developed. The fundamentals of State-Space Averaging (SSA) modelling presented in [31] for DC-DC converters, have been applied to the DC-link inverter in order to derive the necessary mathematical equation required for simulation by assuming the circuit operates in continuous conduction mode.

5.1.1 SSA Module with R Load

In order to write the necessary state-space equations for the five-level inverter with a resistive load, shown in Fig.5.1, the switches states shown in Fig.3.2 can be used. The equations include the state, input and output variables.

The voltages across the diodes (v_{D1}, v_{D2}), which are given in equations 5.1 and 5.2, can be written as a function in the PV voltages (v_{pv1}, v_{pv2}) of PV1 and PV2 sources and the corresponding switching states (S1i, S2i).

$$v_{D1} = S1i \cdot v_{pv1} \quad \ldots\ldots (5.1)$$

$$v_{D2} = S2i \cdot v_{pv2} \quad \ldots\ldots (5.2)$$

The currents flowing through the two capacitors across the PV sources are determined by their respective PV source currents (i_{pv1}, i_{pv2}) and that flowing to the DC-link (i_{link}).

$$i_{c_{pv1}} = C_{pv1}\frac{dv_{pv1}}{dt} = i_{pv1} - i_{link} \cdot S1i \quad \ldots\ldots (5.3)$$

$$i_{c_{pv2}} = C_{pv2}\frac{dv_{pv2}}{dt} = i_{pv2} - i_{link} \cdot S2i \quad \ldots\ldots (5.4)$$

The current to the DC-link, before the output H-bridge, is given as

$$i_{link} = \frac{v_{D1} + v_{D2}}{R} \quad \ldots\ldots (5.5)$$

Naturally the output voltage is determined by the DC-link voltage and switching state of the output H-bridge.

$$v_{out} = (v_{D1} + v_{D2}) \cdot (S1 - S3) = (v_{D1} + v_{D2}) \cdot (2S1 - 1) \quad \ldots\ldots (5.6)$$

where S is the switch state ('0' for off state and '1' for on state). C_{pv1}, C_{pv2} are the bypass capacitors of PV1 and PV2.

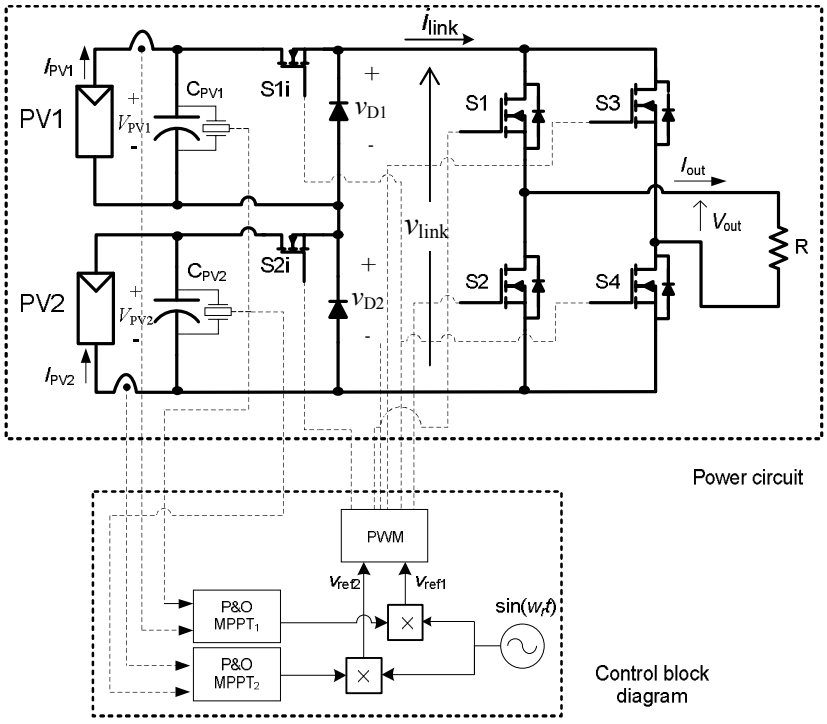


Fig.5.1: Five-level DC-link inverter system applied for R and R-L loads.

Assuming that the switching frequency, f_c, is much greater than the reference signal frequency, f_r, and the switching time, T_c, is much smaller than the time constants associated with the storage elements in the circuit, the switches states, *S,* in above equations 5.1 to 5.6 can be replaced with the duty ratios of the each corresponding switches. For instant $S1i$ is replaced by D_{1i}, and $S2i$ by D_{2i}, subsequently the final form of the SSA model is given below by equations 5.7 and 5.8.

$$\dot{x} = \mathrm{A} \cdot x + \mathrm{B} \cdot i_{in}$$

$$\begin{bmatrix} \frac{dv_{pv1}}{dt} \\ \frac{dv_{pv2}}{dt} \end{bmatrix} = \frac{1}{R} \begin{bmatrix} \frac{-D_{1i}{}^2}{C_{pv1}} & \frac{-D_{1i}D_{2i}}{C_{pv1}} \\ \frac{-D_{1i}D_{2i}}{C_{pv2}} & \frac{-D_{2i}{}^2}{C_{pv2}} \end{bmatrix} \begin{bmatrix} v_{pv1} \\ v_{pv2} \end{bmatrix} + \begin{bmatrix} \frac{1}{C_{pv1}} & 0 \\ 0 & \frac{1}{C_{pv2}} \end{bmatrix} \begin{bmatrix} i_{pv1} \\ i_{pv2} \end{bmatrix} \quad \text{... (5.7)}$$

$$y = C \cdot x + D \cdot i_{in}$$

$$\begin{bmatrix} v_{out} \end{bmatrix} = (2D_1 - 1) \cdot \begin{bmatrix} D_{1i} & D_{2i} \end{bmatrix} \begin{bmatrix} v_{pv1} \\ v_{pv2} \end{bmatrix} + \begin{bmatrix} 0 & 0 \end{bmatrix} \begin{bmatrix} i_{pv1} \\ i_{pv2} \end{bmatrix} \qquad \text{..... (5.8)}$$

where A, B, C and D are the coefficients of the state space equations.

As can be seen the coefficients of the state space equations are not constants, they have variables due to duty ratios of the switches, they vary for every switching period T_c. For the simulation of this inverter, the switches states are not replaced by duty ratios, this enables generating voltage pulses and gaps at different voltage levels at the specific time instant to achieve multilevel voltage waveforms. This cannot be done if duty ratio is used instead as it can only lead to the generation of an averaged value within each switching period T_c. Consequently, the simulation step size has to be small compared with T_c.

The SSA model of the DC-link inverter with resistive load has been derived and presented in a general form which can be used with inverters of any number of levels according to the number of the PV sources (n) connected in series. The generalized SSA model is given in equations 5.9 and 5.10.

$$\begin{bmatrix} \frac{dv_{pv1}}{dt} \\ \frac{dv_{pv2}}{dt} \\ \cdot \\ \cdot \\ \cdot \\ \frac{dv_{pvn}}{dt} \end{bmatrix} = \frac{1}{R} \begin{bmatrix} \frac{-D_{1i}^{\,2}}{C_{pv1}} & \frac{-D_{1i}D_{2i}}{C_{pv1}} & \cdots & \frac{-D_{1i}D_{ni}}{C_{pv1}} \\ \frac{-D_{2i}D_{1i}}{C_{pv2}} & \frac{-D_{2i}^{\,2}}{C_{pv2}} & \cdots & \frac{-D_{2i}D_{ni}}{C_{pv2}} \\ \cdot & \cdot & \cdots & \cdot \\ \cdot & \cdot & \cdots & \cdot \\ \cdot & \cdot & \cdots & \cdot \\ \frac{-D_{ni}D_{1i}}{C_{pvn}} & \frac{-D_{ni}D_{2i}}{C_{pvn}} & \cdots & \frac{-D_{ni}^{\,2}}{C_{pvn}} \end{bmatrix} \begin{bmatrix} v_{pv1} \\ v_{pv2} \\ \cdot \\ \cdot \\ \cdot \\ v_{pvn} \end{bmatrix} + \begin{bmatrix} \frac{1}{C_{pv1}} & 0 & \cdots & 0 \\ 0 & \frac{1}{C_{pv2}} & 0 \cdots & 0 \\ 0 & 0 & \cdot 0 \cdot & \cdot \\ 0 & 0 & 0 \cdot 0 & \cdot \\ 0 & 0 & 0\ 0 \cdot & 0 \\ 0 & 0 & 0\ 0\ 0 & \frac{1}{C_{pvn}} \end{bmatrix} \begin{bmatrix} i_{pv1} \\ i_{pv2} \\ \cdot \\ \cdot \\ \cdot \\ i_{pvn} \end{bmatrix} \quad \text{... (5.9)}$$

$$[v_{out}] = (2D_1 - 1) \cdot [D_{1i} \quad D_{2i} \quad \cdots \quad D_{ni}] \begin{bmatrix} v_{pv1} \\ v_{pv2} \\ \cdot \\ \cdot \\ \cdot \\ v_{pvn} \end{bmatrix} + [0 \quad 0 \quad \cdots \quad 0] \begin{bmatrix} i_{pv1} \\ i_{pv2} \\ \cdot \\ \cdot \\ \cdot \\ i_{pvn} \end{bmatrix} \quad \text{..... (5.10)}$$

Using the above model, the two PV sources system as shown in Fig.5.1 is simulated. The system parameters used in the simulation are listed in Table 5.1, and the information about the PV sources is described in Table.4.1. The results obtained shown in Figures 5.2 and 5.3 are for PV sources under even irradiance condition. Here the switching states S1i and S2i are swapped during each switching time period, thus the PV sources are loaded equally. This scheme also maintains balanced positive and negative voltage even when one of the PV sources is bypassed.

TABLE 5.1: Five-level (DC-link) Inverter System Parameters

G_1	1000 W/m^2	R	10 Ω	f_r	50Hz
G_2	1000 W/m^2	M_f	100	MPPT (C)	1V
K_p	0.01	C_{PV1}	5500μF	C_{PV2}	5500μF
K_i	100				

where f_r is the reference frequency; G_1 and G_2 are the irradiance levels of PV1 and PV2 respectively; K_p, and K_i are the proportional and integral constants of the PI controller; MPPT (C) represents the MPP tracking step size; M_f is the frequency modulation index.

Fig.5.2 shows the resultant load voltage and current simulation waveforms. Note that v_{ref}, denoted in the Figure, represents the PWM reference signal and is equal in amplitude to the summation of v_{ref1} and v_{ref2} shown in the circuit diagram in Fig.5.1. Also, v_{ref} is similar to the fundamental voltage component (v_1) of the output. The

transient responses of power generated from both PV1 and PV2 are shown in Fig.5.3, clearly both operate at their MPP after an elapsed time of 0.3s.

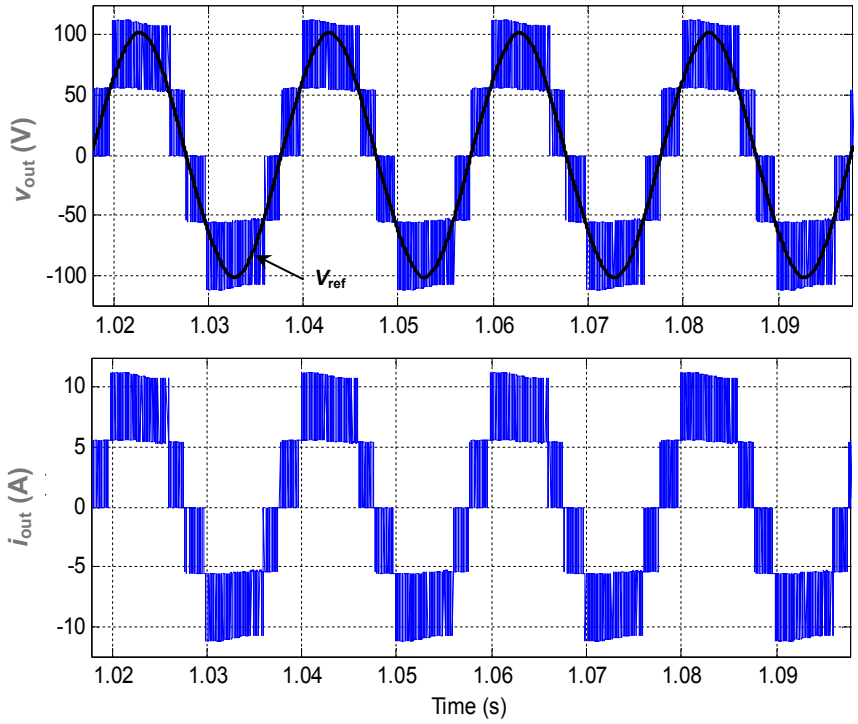


Fig.5.2: R load output voltage and current simulation waveforms by using five-level DC-link.

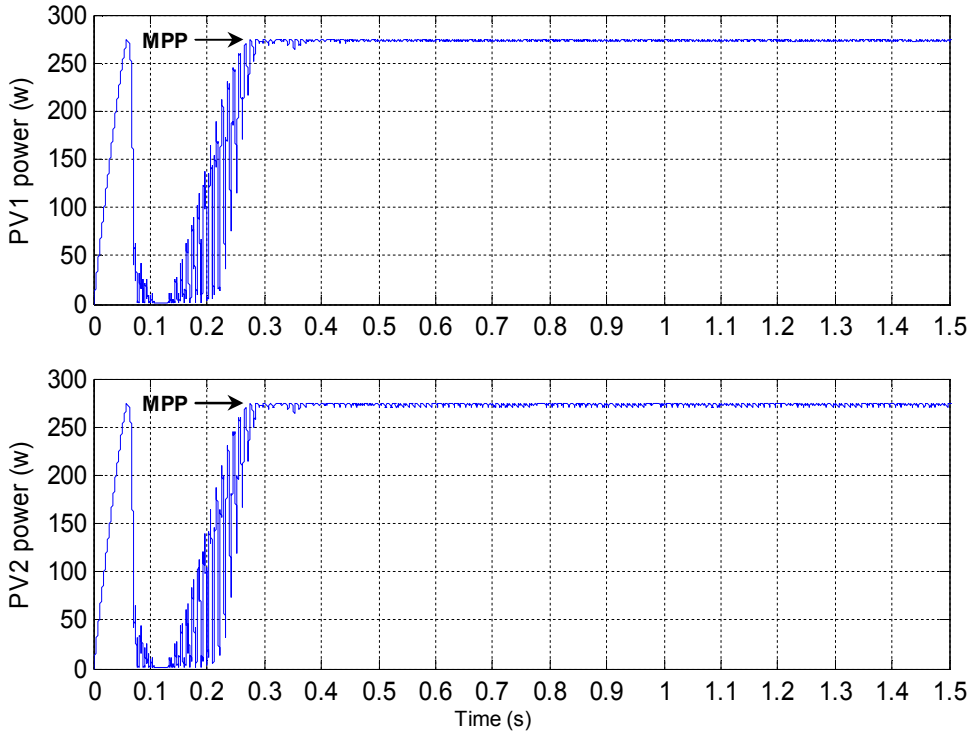


Fig.5.3: The transient of PV extracted power under 1000 W/m^2 irradiance by using five-level DC-link inverter with R load.

5.1.2 SSA Module with R-L Load

The SSA model for two PV modules DC-link inverter with an R-L is the same as that for the previous case with an R load. The circuit diagram of Fig.5.1 is still used but with an R-L load. Equations 5.1-5.4 are still used but including two additional equations:

$$i_{link} = (2S1 - 1) \cdot i_L \qquad \ldots\ldots \quad (5.10)$$

$$v_{out} = L\frac{di_L}{dt} + i_L \cdot R \; = (v_{D1} + v_{D2}) \cdot (2S1 - 1) \qquad \ldots\ldots \quad (5.12)$$

where L is the load inductance and i_L is the load current. The final form of the SSA model is given as in equations 5.13 and 5.14.

$$\begin{bmatrix} \frac{dv_{pv1}}{dt} \\ \frac{dv_{pv2}}{dt} \\ \frac{di_L}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -(2D_1 - 1) \cdot \frac{D_{1i}}{C_{pv1}} \\ 0 & 0 & -(2D_1 - 1) \cdot \frac{D_{2i}}{C_{pv2}} \\ (2D_1 - 1) \cdot \frac{D_{1i}}{L} & (2D_1 - 1) \cdot \frac{D_{2i}}{L} & \frac{-R}{L} \end{bmatrix} \begin{bmatrix} v_{pv1} \\ v_{pv2} \\ i_L \end{bmatrix} + \begin{bmatrix} \frac{1}{C_{pv1}} & 0 \\ 0 & \frac{1}{C_{pv2}} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i_{pv1} \\ i_{pv2} \end{bmatrix} \quad \ldots(5.13)$$

$$\begin{bmatrix} v_{out} \end{bmatrix} = (2D_1 - 1) \cdot \begin{bmatrix} D_{1i} & D_{2i} \end{bmatrix} \begin{bmatrix} v_{pv1} \\ v_{pv2} \end{bmatrix} + \begin{bmatrix} 0 & 0 \end{bmatrix} \begin{bmatrix} i_{pv1} \\ i_{pv2} \end{bmatrix} \qquad \ldots\ldots \quad (5.14)$$

The generalized SSA model for such inverter having any number of levels with R-L load is presented as below in equations 5.15 and 5.16.

$$\begin{bmatrix} \frac{dv_{pv1}}{dt} \\ \frac{dv_{pv2}}{dt} \\ \cdot \\ \cdot \\ \cdot \\ \frac{dv_{pvn}}{dt} \\ \frac{di_L}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \cdot & \cdot & 0 & -(2D_1 - 1) \cdot \frac{D_{1i}}{C_{pv1}} \\ 0 & 0 & 0 & \cdot & \cdot & 0 & -(2D_1 - 1) \cdot \frac{D_{2i}}{C_{pv2}} \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ 0 & 0 & 0 & \cdot & \cdot & 0 & -(2D_1 - 1) \cdot \frac{D_{ni}}{C_{pvn}} \\ (2D_1 - 1) \cdot \frac{D_{2i}}{L} & \cdot & \cdot & \cdot & \cdot & (2D_1 - 1) \cdot \frac{D_{ni}}{L} & \frac{-R}{L} \end{bmatrix} \begin{bmatrix} v_{pv1} \\ v_{pv2} \\ \cdot \\ \cdot \\ \cdot \\ v_{pvn} \\ i_L \end{bmatrix} + \begin{bmatrix} \frac{1}{C_{pv1}} & 0 & \cdot & \cdot & \cdot & 0 \\ 0 & \frac{1}{C_{pv2}} & 0 & \cdot & \cdot & 0 \\ \cdot & 0 & \cdot & 0 & \cdot & \cdot \\ \cdot & \cdot & 0 & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & 0 & \cdot & 0 \\ \cdot & \cdot & \cdot & \cdot & 0 & \frac{1}{C_{pvn}} \\ 0 & \cdot & \cdot & \cdot & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{pv1} \\ i_{pv2} \\ \cdot \\ \cdot \\ \cdot \\ i_{pvn} \end{bmatrix}$$

$\ldots\ldots$ (5.15)

$$\begin{bmatrix} v_{out} \end{bmatrix} = (2D_1 - 1) \cdot \begin{bmatrix} D_{1i} & D_{2i} & \cdot & \cdot & \cdot & D_{ni} \end{bmatrix} \begin{bmatrix} v_{pv1} \\ v_{pv2} \\ \cdot \\ \cdot \\ \cdot \\ v_{pvn} \end{bmatrix} + \begin{bmatrix} 0 & 0 & \cdot & \cdot & \cdot & 0 \end{bmatrix} \begin{bmatrix} i_{pv1} \\ i_{pv2} \\ \cdot \\ \cdot \\ \cdot \\ i_{pvn} \end{bmatrix} \qquad \ldots\ldots \quad (5.16)$$

Simulation study of this case are carried out for PV sources under symmetrical irradiance levels and using the SSA model, with the same system parameters used in the pervious section applied and the R-L load is set as R=5.5 Ω, L=10 mH, and K_p=0.07. The R-L load output voltage and current waveforms are shown in Fig.5.4. The reference voltage, inductor current and inductor voltage waveforms are illustrated in Fig.5.5. The power waveforms are similar to that obtained in Fig.5.3, where the MPPs of the PV sources are achieved.

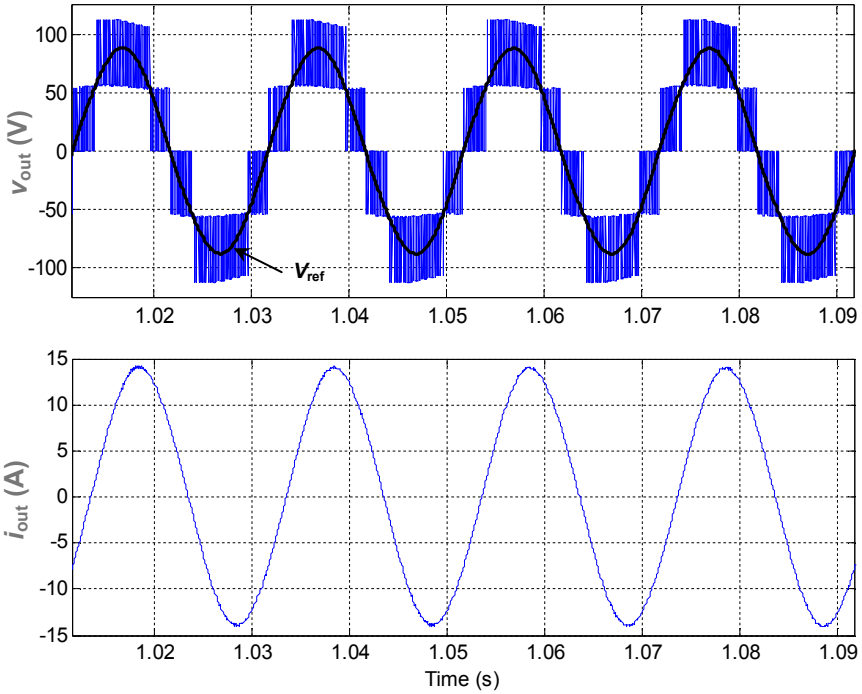


Fig.5.4: R-L load output voltage and current waveforms (Five-level DC-Link)

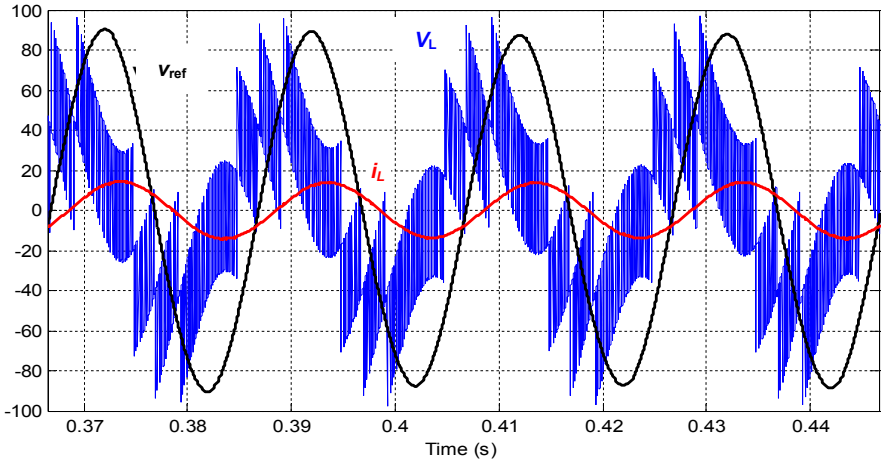


Fig.5.5: The reference voltage, inductor current and voltage simulation waveforms

5.1.3 SSA Module with Grid-Connected

The SSA model for the grid-connected inverter shown in Fig.5.6 is also obtained using the analysis as shown in the previous sections. Components R and L shown in the Figure refer to the filter and equivalent grid impedances in total [79]. The state-space equations derived are the same as equations 5.1-5.4 and 5.11 plus an additional given below:

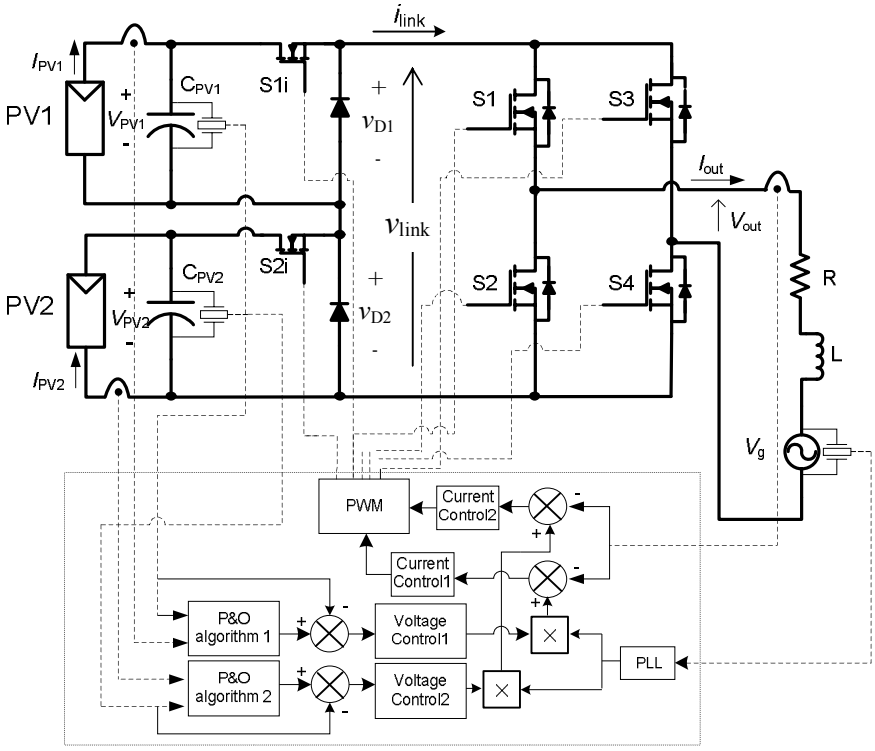


Fig.5.6: Grid-connected five-level DC-link inverter system.

$$v_{out} = L\frac{di_L}{dt} + i_L \cdot R \ + v_g = (v_{D1} + v_{D2}) \cdot (2S1 - 1) \qquad \ldots\ldots \ (5.17)$$

So the SSA model for the two PV sourced grid-connected DC-link inverter can be written as:

$$\begin{bmatrix} \frac{dv_{pv1}}{dt} \\ \frac{dv_{pv2}}{dt} \\ \frac{di_L}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -(2D_1 - 1)\cdot\frac{D_{1i}}{C_{pv1}} \\ 0 & 0 & -(2D_1 - 1)\cdot\frac{D_{2i}}{C_{pv2}} \\ (2D_1 - 1)\cdot\frac{D_{1i}}{L} & (2D_1 - 1)\cdot\frac{D_{2i}}{L} & \frac{-R}{L} \end{bmatrix} \begin{bmatrix} v_{pv1} \\ v_{pv2} \\ i_L \end{bmatrix} + \begin{bmatrix} \frac{1}{C_{pv1}} & 0 & 0 \\ 0 & \frac{1}{C_{pv2}} & 0 \\ 0 & 0 & \frac{-1}{L} \end{bmatrix} \begin{bmatrix} i_{pv1} \\ i_{pv2} \\ v_g \end{bmatrix} \quad \ldots\ldots \ (5.18)$$

$$\begin{bmatrix} v_{out} \end{bmatrix} = (2D_1 - 1) \cdot \begin{bmatrix} D_{1i} & D_{2i} & 0 \end{bmatrix} \begin{bmatrix} v_{pv1} \\ v_{pv2} \\ i_l \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{pv1} \\ v_{pv2} \\ i_l \end{bmatrix} \qquad \ldots\ldots \ (5.19)$$

The generalized SSA module for *n* PV sources grid-connected DC-link inverter is presented as in equations 5.20 and 5.21.

$$\begin{bmatrix} \frac{dv_{pv1}}{dt} \\ \frac{dv_{pv2}}{dt} \\ \cdot \\ \cdot \\ \cdot \\ \frac{dv_{pvn}}{dt} \\ \frac{di_L}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \cdot & \cdot & 0 & -(2D_1-1)\cdot\frac{D_{1i}}{C_{pv1}} \\ 0 & 0 & 0 & \cdot & \cdot & 0 & -(2D_1-1)\cdot\frac{D_{2i}}{C_{pv2}} \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ 0 & 0 & 0 & \cdot & \cdot & 0 & -(2D_1-1)\cdot\frac{D_{ni}}{C_{pvn}} \\ (2D_1-1)\cdot\frac{D_{2i}}{L} & \cdot & \cdot & \cdot & \cdot & (2D_1-1)\cdot\frac{D_{ni}}{L} & \frac{-R}{L} \end{bmatrix} \begin{bmatrix} v_{pv1} \\ v_{pv2} \\ \cdot \\ \cdot \\ \cdot \\ v_{pvn} \\ i_L \end{bmatrix} + \begin{bmatrix} \frac{1}{C_{pv1}} & 0 & 0 & 0 & \cdot & \cdot & 0 \\ 0 & \frac{1}{C_{pv2}} & 0 & \cdot & \cdot & \cdot & 0 \\ \cdot & 0 & \cdot & 0 & \cdot & \cdot & \cdot \\ \cdot & \cdot & 0 & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & 0 & \cdot & 0 & \cdot \\ \cdot & \cdot & \cdot & \cdot & 0 & \frac{1}{C_{pvn}} & 0 \\ 0 & 0 & 0 & \cdot & \cdot & 0 & \frac{-1}{L} \end{bmatrix} \begin{bmatrix} i_{pv1} \\ i_{pv2} \\ \cdot \\ \cdot \\ \cdot \\ i_{pvn} \\ v_g \end{bmatrix}$$

……. (5.20)

$$[v_{out}] = (2D_1-1)\cdot[D_{1i} \quad D_{2i} \quad \cdot \quad \cdot \quad \cdot \quad D_{ni}] \begin{bmatrix} v_{pv1} \\ v_{pv2} \\ \cdot \\ \cdot \\ \cdot \\ v_{pvn} \end{bmatrix} + [0 \quad 0 \quad \cdot \quad \cdot \quad \cdot \quad 0] \begin{bmatrix} i_{pv1} \\ i_{pv2} \\ \cdot \\ \cdot \\ \cdot \\ i_{pvn} \end{bmatrix} \qquad \text{…..... (5.21)}$$

The mathematical model obtained is used in the simulation of a PV-grid connected system. The inverter output and reference voltage waveforms are shown in Fig.5.7 together with the grid voltage and the accompanied output current waveforms. The reference, grid, resistor, inductor voltage waveforms are presented in Fig.5.8 together with the output current waveform. As it is clear in Fig.5.9, the grid had been connected to the system after elapsed time of almost 0.3 sec, and the reason for this the time taken to enable the system voltage reaching the grid voltage level. The power waveforms of the PV sources are shown in Fig.5.10.

The applied parameters are R=2.5 Ω and L=10 mH. The grid amplitude voltage (v_g) is 88 V and the current controller constants are 5 for both of K_p and K_i. The other system parameters are as listed in Table 5.1 and the PV sources parameters are listed in Table 4.1.

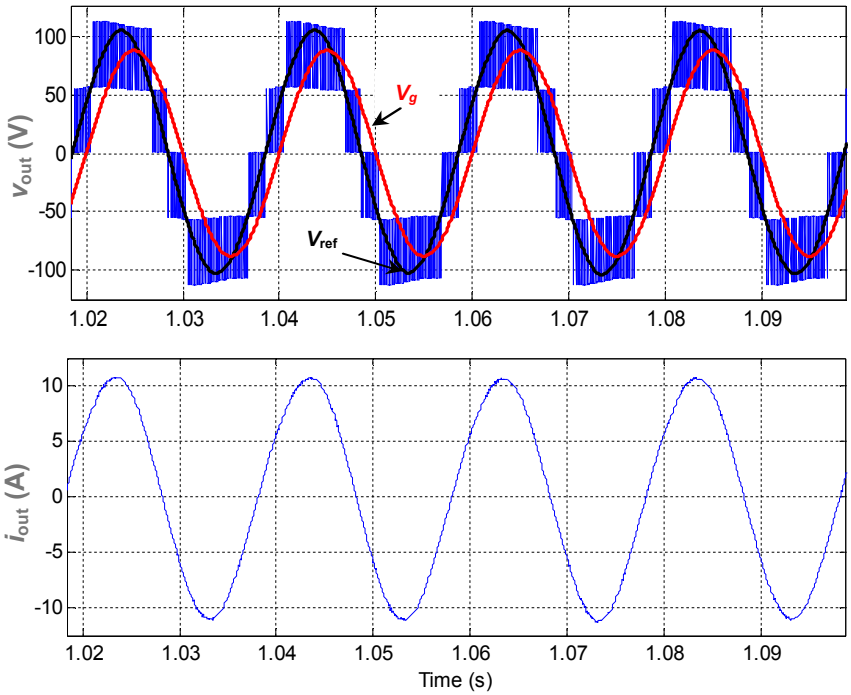


Fig.5.7: Grid-connected steady-state simulation waveforms of output voltage and current by using five-level DC-link inverter.

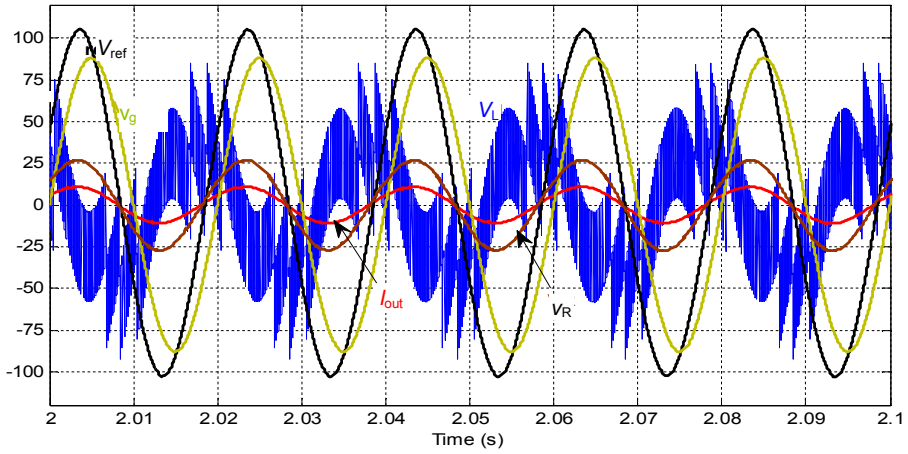


Fig.5.8: Fundamental harmonic of output voltage, grid voltage, current and voltages simulation waveforms across R and L by using five-level DC-link inverter.

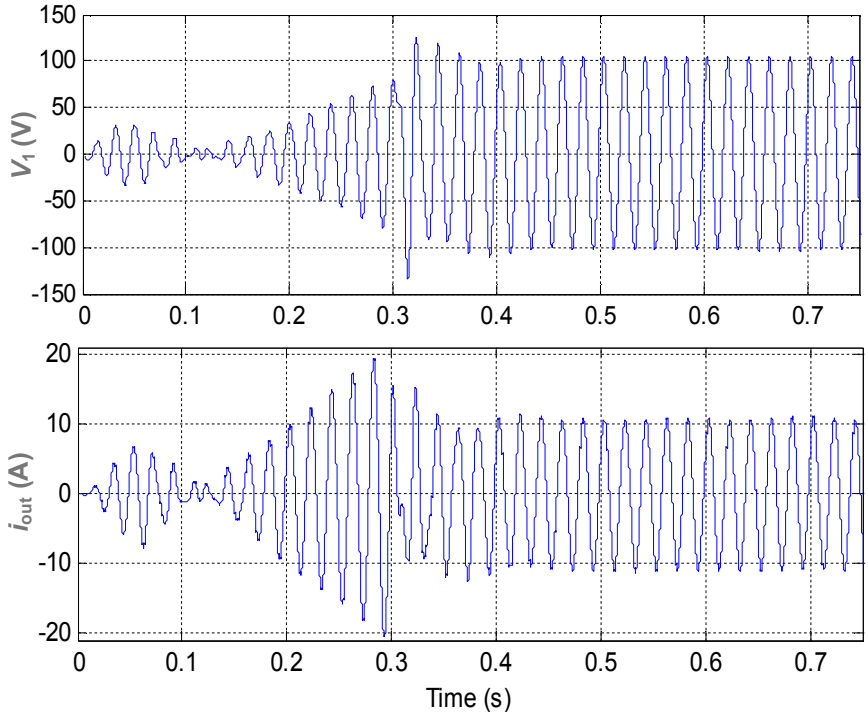


Fig.5.9: Transient response simulation waveforms of fundamental output voltage and current during connection (grid is connected at 0.3s).

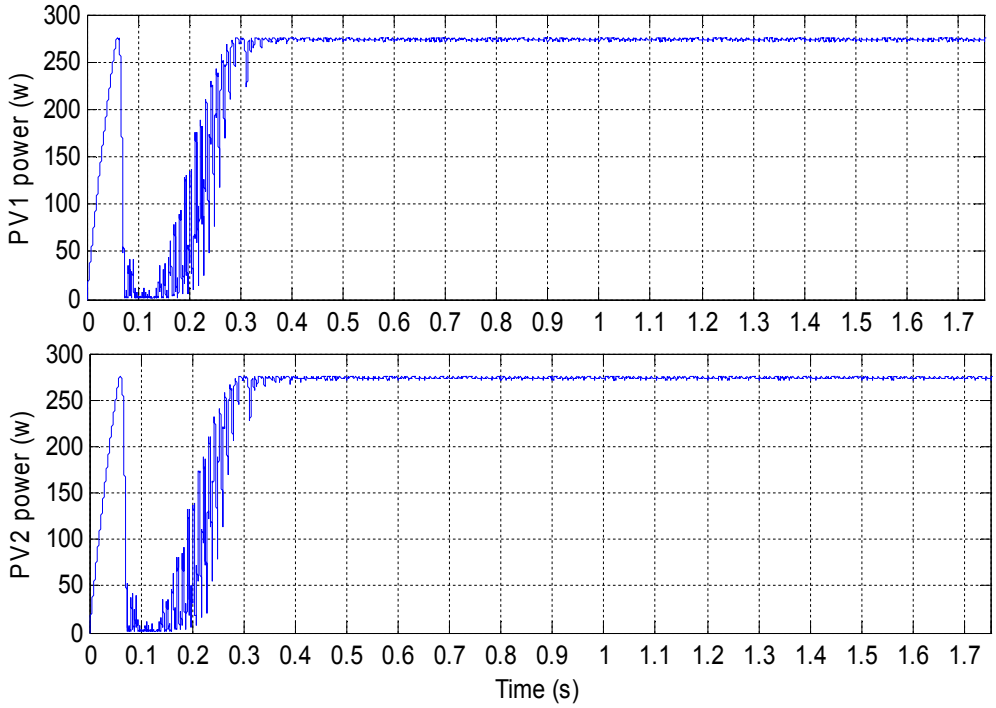


Fig.5.10: Transient simulation waveforms of PV extracted power (grid is connected at 0.3s).

When the grid is connected, the system it showed a correct response, where as shown in Figures 5.9 and 5.10 the current and the voltage amplitudes are adjusted via the control system to maintain delivering the maximum power of the PV sources to the grid.

In order to test the system under different inverter levels, seven-level and nine-level output voltage waveforms were obtained by using three and four input PV sources respectively. The accomplished waveforms are given in Fig.5.11 and Fig.5.12 respectively.

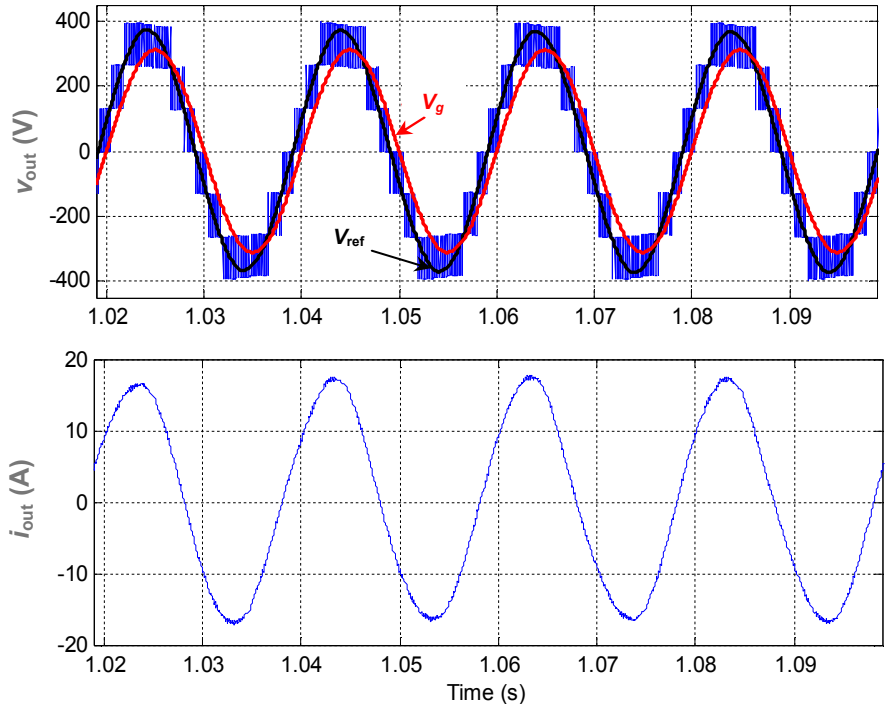


Fig.5.11: Grid-connected steady-state simulation waveforms of output voltage and current by using seven-level DC-link inverter..

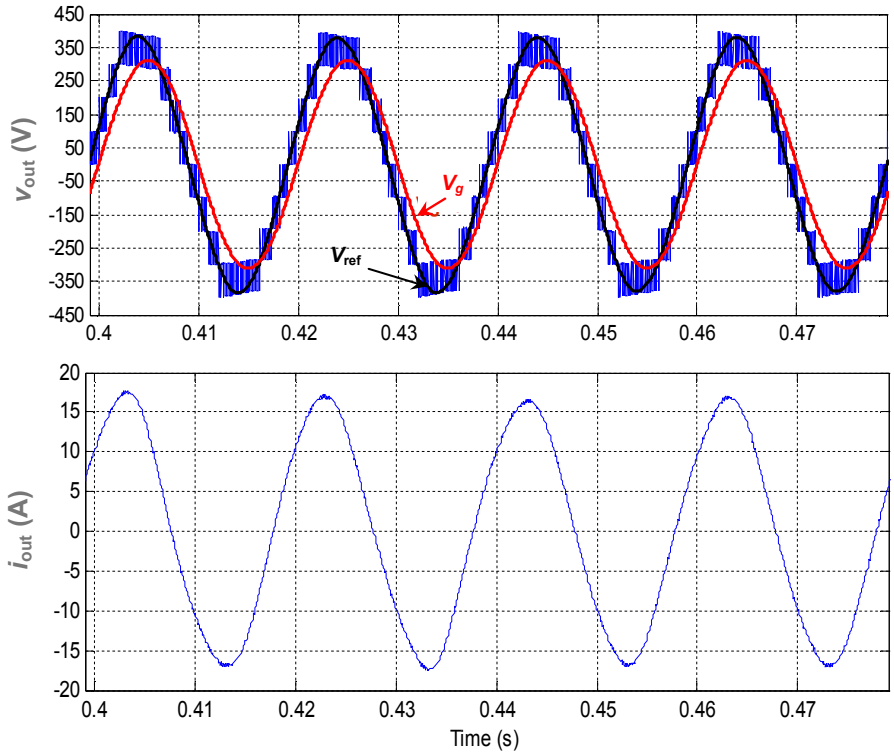


Fig.5.12: Grid-connected steady-state simulation waveforms of output voltage and current by using nine-level DC-link inverter.

The parameters applied for the seven-level grid-connected system are described in Table 5.2. Where, $K_{p,v}$, $K_{p,c}$, $K_{i,v}$, $K_{i,c}$ are the proportional and integral constants of voltage and current PI controllers.

TABLE 5.2: Seven-level Grid-connected (DC-link) Inverter System Parameters

$G_{1,2,3}$	1000 W/m^2	R	5 Ω	f_r	50Hz
V_g	311.1 V	L	10 mH	$K_{i,v}$	100
$K_{p,v}$	0.01	$K_{i,c}$	5	$K_{p,c}$	5
$C_{PV1,2,3}$	5500µF	M_f	100	MPPT (C)	2 V
V_{mpp}	130 V	I_{mpp}	7.5 A	V_{OC}	150 V
I_{SC}	8 A				

With respect to the nine-level grid-connected system, the applied system parameters are as those listed in Table 5.2 with exception of the parameters that are shown in Table 5.3.

TABLE 5.3: Nine-level Grid-connected (DC-link) Inverter System Parameters

R	6 Ω	I_{sc}	8 A	V_{oc}	108 V
L	10 mH	V_{mpp}	97.5 V	I_{mpp}	7.5 A

The reference, grid, resistor, inductor voltage waveforms together with the accompanied output current waveform are all shown in Fig.5.13 and Fig.5.14 for seven and nine level systems respectively.

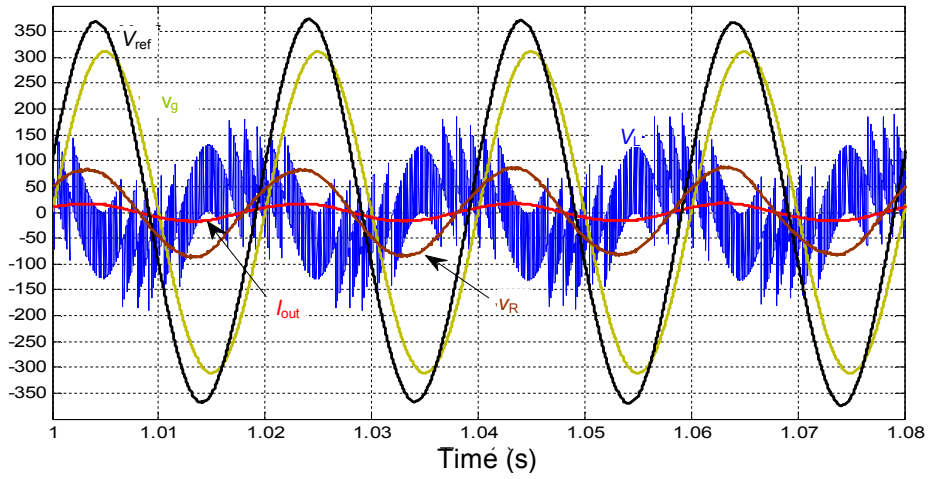


Fig.5.13: Fundamental harmonic of output voltage, grid voltage, current and voltages simulation waveforms across R and L by using seven-level DC-link inverter.

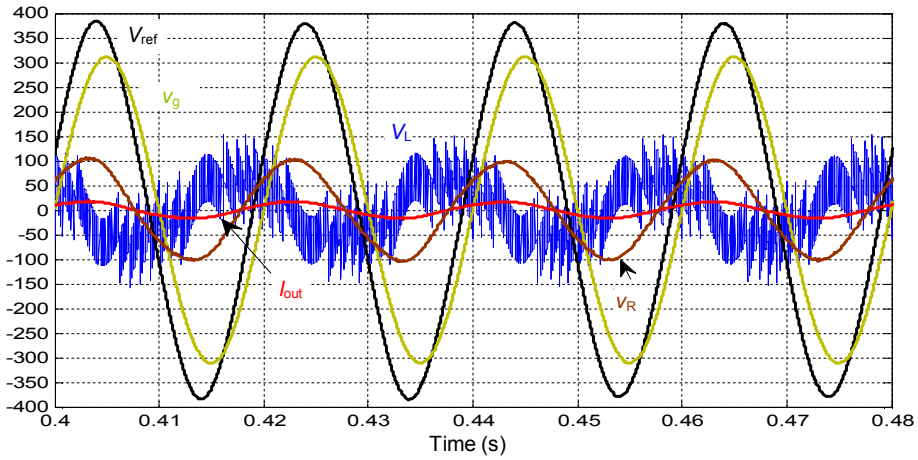


Fig.5.14: Fundamental harmonic of output voltage, grid voltage, current and voltages simulation waveforms across R and L by using nine-level DC-Link inverter.

5.2 PV Permutation Algorithm for Partial Shading Condition

In this section a new control algorithm called 'PV permutation algorithm' is proposed for the PV multilevel DC-link inverter in order to overcome the problem of uneven irradiance on the individual PV modules, namely the partial shading condition. A system consisting of three PV modules with a seven-level DC-link inverter shown in Fig.5.15 is used to demonstrate the principle and application of the method.

The algorithm involves three stages: direct PWM, sequential permutation of PV sources and the output generation. The details of the first stage are described in section 3.2.2. The direct PWM offers the benefit of reducing the computational time compared with the space-vector PWM methods. It is used here for determining the required low and high output voltage levels (V_{ol} and V_{oh}) and their time intervals (t_{off} and t_{on}) within each PWM switching cycle of period (T_c). The second stage, the sequential permutation of PV sources, is based on the work described in [41] for a system having two PV sources. However, its application to systems containing more than two PV sources is more complex and a generalized approach is outlined in section 5.2.1 below. The third stage, the output generation, provides a novel solution to the partial shading and is described in section 5.2.2.

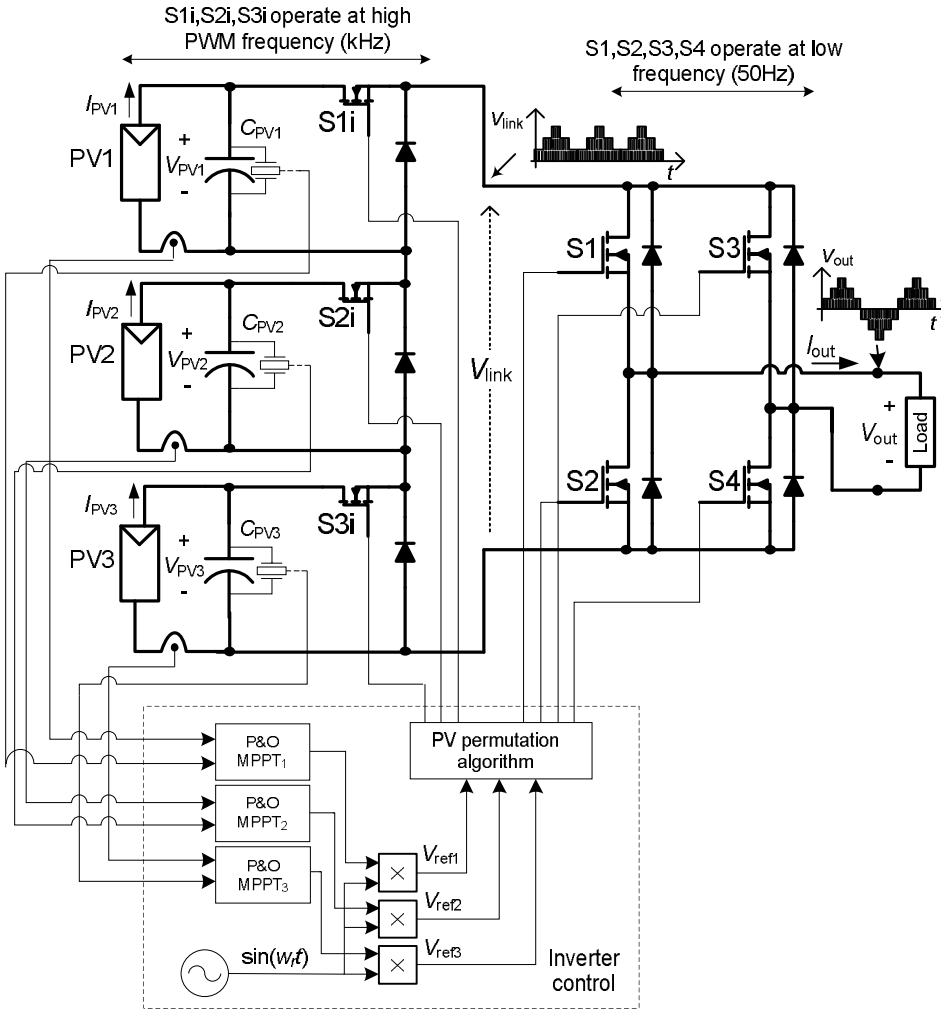


Fig.5.15: Seven-level PV DC-link inverter system with PV permutation algorithm.

5.2.1 Sequential Permutation of PV Sources

Assuming a system having n PV sources to form the output PWM voltage, all of them are sequentially permutated per consecutive PWM switching cycle according to the numerical count c = 1, 2, …n, as shown in Fig.5.16. The PV source which sequentially comes in turn at the highest voltage level is the only one which is controlled at a particular switching cycle, while other sources are used to build the appropriate voltage level determined in the first stage (the direct PWM). The benefits of such a procedure are: (i) all PV sources of the system are used equally, so under symmetrical irradiance of PV sources they produce equal amount of power, and the switching losses of transistors associated with each PV source are equal, (ii) it allows to achieve symmetrical positive and negative half-cycles of the output voltage waveform under partial shading i.e. when PV voltages are different, and (iii) it enables a reduction of the voltage ripple on PV capacitors.

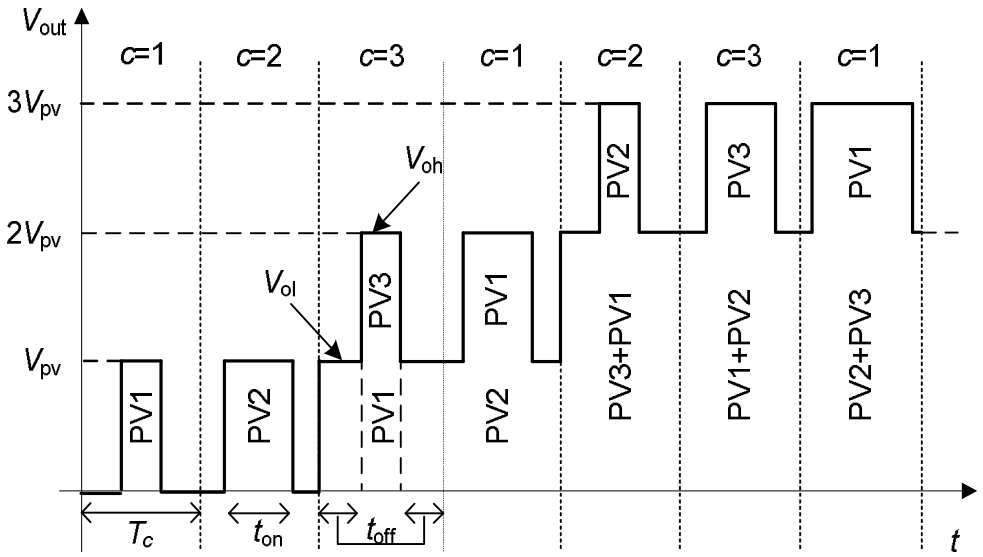


Fig.5.16: Numerical PV source permutation mechanism.

5.2.2 PV Output Generation

As shown in Fig.5.15, the control unit of the PV system includes a Perturbation and Observation (P&O) MPPT block for each PV source. These provide a separate P&O tracking algorithm and the PI control for each PV source. The output signals of these blocks are multiplied by a unity sinusoidal signal to form AC reference signals $v_{ref1}, v_{ref2}, \ldots v_{ref(n)}$. These reference signals are used to control the inverter switches by applying the direct PWM (the first stage in the algorithm) and the output generation. The direct PWM normalized reference voltage is given as

$$\bar{v}_{ref(j)} = \frac{\left| v_{ref(j)} \right|}{V_{mpp} / n} \qquad \ldots\ldots. (5.22)$$

where V_{mpp} is the MPP voltage of a PV source at irradiance of 1000 W/m^2, and n denotes the total number of PV sources.

The integer part of the normalized reference voltage is defined as the normalized offset voltage and it is given as

$$v_{offset(j)} = \text{int}\,[\bar{v}_{ref(j)}] \qquad \ldots\ldots. (5.23)$$

The t_{on} interval of the PV source, which is being controlled at a particular switching period, is given as

$$t_{on(j)} = T_c \cdot (\bar{v}_{ref(j)} - v_{offset(j)}) \qquad \ldots\ldots. (5.24)$$

Equation (5.24) can be derived by equating the approximated volt-time area of the graph 'v_{ref} vs. time' with the corresponding area under the generated pulse within a cycle T_c [61].

Table 5.4 describes the principles of generating the output voltage in a system consisting of two PV sources. As is seen when, the source PV1 is controlled by applying direct PWM to v_{ref1} in order to determine the required t_{on} time. The role of v_{ref2} is to determine V_{ol} by checking $v_{offset2}$. Similarly when c=2, then the PV2 is controlled through v_{ref2}, and v_{ref1} is used to determine the V_{ol}.

TABLE 5.4: Output Generation from Two PV Sources

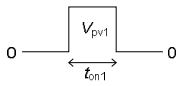
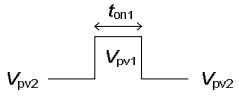
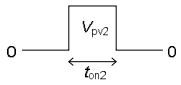
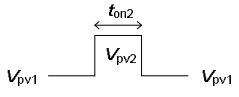
c	$v_{offset1}$	$v_{offset2}$	Output generation per switching period T_c
1	0	0	
	1	0	
	0	1	
	1	1	
2	0	0	
	0	1	
	1	0	
	1	1	

Fig.5.17 illustrates the complete process for the PV permutation algorithm applied to a two PV sources DC-link inverter starting with the reference signals formed through the MPP algorithms, and then the necessary switching control signals which are applied to the gates of the inverter switches. Finally, the resulting output voltage waveform.

In the Figure, $v_{erf(i)}$ represents the samples of the desired reference voltage where i=1 to M_f applied every time period of T_r ($1/f_r$). The 1 and 0 of the control signals refer to the switches states on and off respectively.

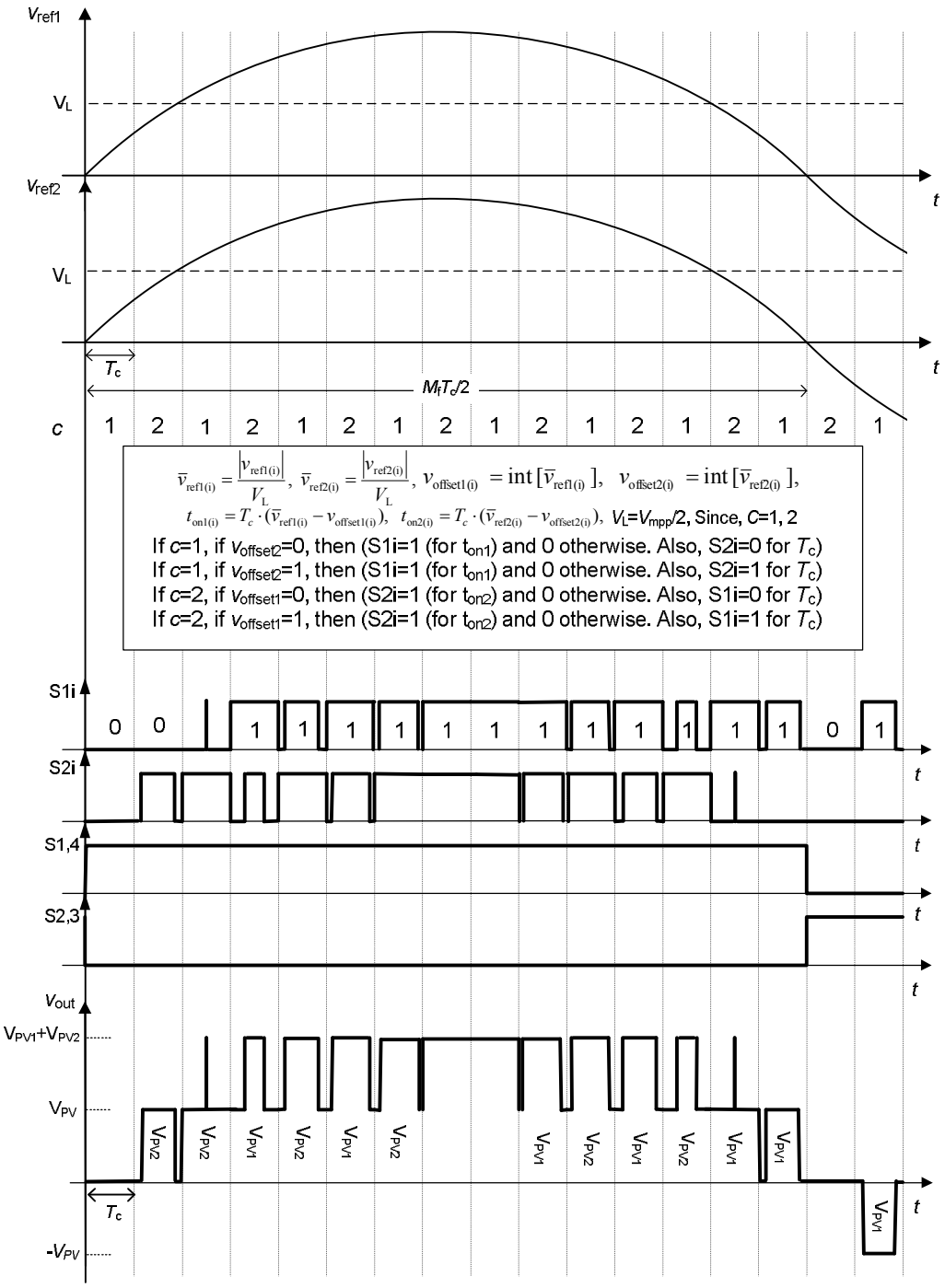


Fig. 5.17: Waveforms of the PV permutation algorithm.

In the case of three PV sources (n=3), the algorithm is accomplished in a similar fashion by applying permutation of the source indices c=1, 2 and 3. Table 5.5 describes the output generation in case of n=3.

Fig.5.18 shows the flowchart of the PV permutation algorithm which is applied to the seven-level inverter operating with three PV sources. The flowchart indicates the main stages in the algorithm including the PV output generation which is described by Table 5.5. In order to ensure a continual sequential permutation, the index c+k (where k=1, 2) of offset voltage or source voltage is reset to c+k–3 if the index value is grater than 3. The algorithm enables each shaded PV source to be recovered to its MPP without affecting other PV sources.

At a given number of PV sources, the flexibility of control is improved by increasing the frequency modulation index M_f (= f_c/f_r, where f_c denotes the switching frequency and f_r is the desired output frequency) as it enables each source to be controlled more frequently within a full AC cycle.

The proposed algorithm has been implemented experimentally by using DSP unit to control five and seven level DC-link inverter under different irradiance levels. In order to improve the quality of the output voltage waveform, the output generation step can be modified. Although the improved step requires more computational efforts comparing with the normal output generation step, considerable waveform improvement can be gained out of it.

TABLE 5.5: Output Generation from Three PV Sources

c	$v_{offset1}$	$v_{offset2}$	$v_{offset3}$	V_{ol}	V_{oh}	t_{on}
1	X(*)	0	X	0	V_{PV1}	t_{on1}
		1	0	V_{PV2}	$V_{PV1}+V_{PV2}$	
		1	1	V_{PV2}	$V_{PV1}+V_{PV2}$	
		1	2	$V_{PV2}+V_{PV3}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
		2	0	V_{PV2}	$V_{PV1}+V_{PV2}$	
		2	1	V_{PV2}	$V_{PV1}+V_{PV2}$	
		2	2	$V_{PV2}+V_{PV3}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
2	X	X	0	0	V_{PV2}	t_{on2}
	0		1	V_{PV3}	$V_{PV2}+V_{PV3}$	
	1		1	V_{PV3}	$V_{PV2}+V_{PV3}$	
	2		1	$V_{PV1}+V_{PV3}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
	0		2	V_{PV3}	$V_{PV2}+V_{PV3}$	
	1		2	V_{PV3}	$V_{PV2}+V_{PV3}$	
	2		2	$V_{PV1}+V_{PV3}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
3	0	X	X	0	V_{PV3}	t_{on3}
	1	0		V_{PV1}	$V_{PV1}+V_{PV3}$	
	1	1		V_{PV1}	$V_{PV1}+V_{PV3}$	
	1	2		$V_{PV1}+V_{PV2}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
	2	0		V_{PV1}	$V_{PV1}+V_{PV3}$	
	2	1		V_{PV1}	$V_{PV1}+V_{PV3}$	
	2	2		$V_{PV1}+V_{PV2}$	$V_{PV1}+V_{PV2}+V_{PV3}$	

(*) Symbol X denotes either state

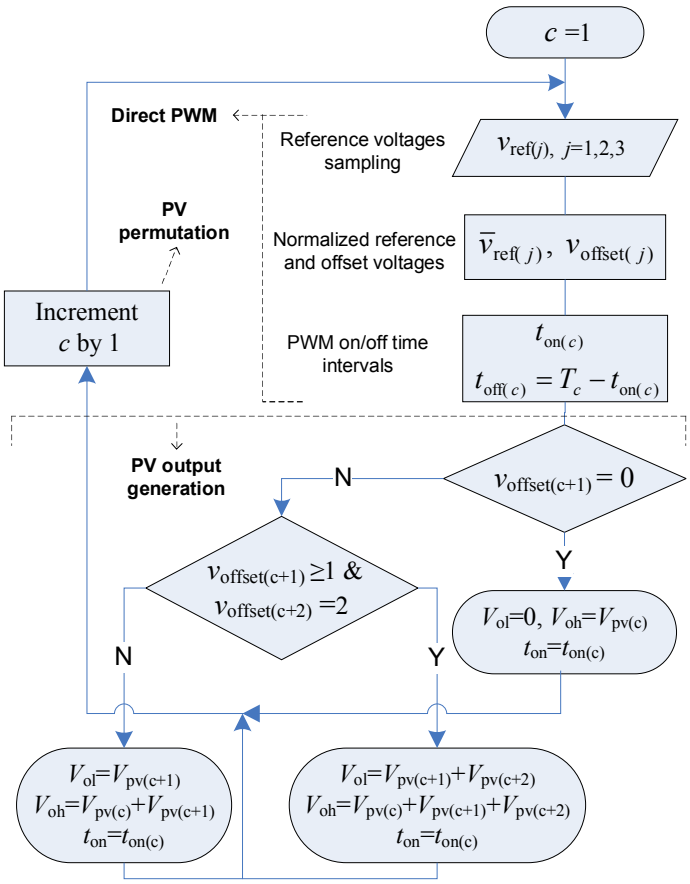


Fig.5.18: Flowchart of the PV permutation algorithm for seven-level inverter.

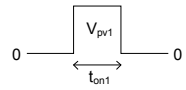
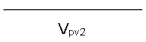
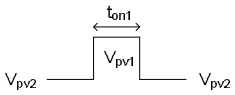
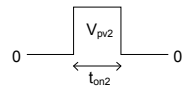
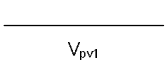
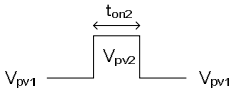
Table 5.6 illustrates the improved output PV generation for two PV sources inverter as a function of c, $V_{offset1}$ and $V_{offset2}$. The improved algorithm enables each shaded PV source to be recovered to its MPP without affecting the other PV sources in the circuit. Unlike the previous algorithm, the improved algorithm does not represent the PV source at the output if its offset voltage is zero except in the case that all the offset voltages are zero, the reason for introducing this exception is to initiate the control and it is also required in the case of low PWM reference signals.

As can be seen in Table 5.6, if c=1, $V_{offset1}$=0 and $V_{offset2}$=1, then the second level (V_{pv1}) will not be presented at the output and the output is only represented by V_{pv2} for T_c time period. Even though there is no control for PV1 source for the mentioned case, the bypass capacitor of PV1 (C_{pv1}) is left charging for the entire T_c giving chance for V_{pv1} to rise up (assume that PV1 is shaded, then connecting it in series with PV2 within the control time t_{on} will drop V_{pv1} down). Fig.5.17 illustrates the generalized improved PV permutation algorithm which can be used for any inverter level. The zero level detection subroutine shown in Fig.5.19 is used to detect the zero level PV source voltages, so they will not be represented at the output. The algorithm

can be applied to any inverter level and improved output voltage waveform can be achieved. Appendix A shows the algorithm output generation in case of three PV sources as a function of the offset voltages.

Some parameters values are helpful in the case of the partial shading, such as the PWM frequency modulation index M_f, it is better to be increased with the increase of the controlled PVs number so more control duties are available to each PV source every output AC time period. Also, selecting high PV capacitors C_{pv} value is better to minimize a 100Hz noise at the input PVs. However, that might slow down the system response. Proper P&O algorithm tracking step size has to be selected for fast tracking of the new MPP of the shaded PVs as well as low oscillation around the desired MPP.

TABLE 5.6: Improved Output Generation from Two PV Sources

c	$v_{offset1}$	$v_{offset2}$	Output generation per switching period T_c
1	0	0	
	1	0	
	0	1	
	1	1	
2	0	0	
	0	1	
	1	0	
	1	1	

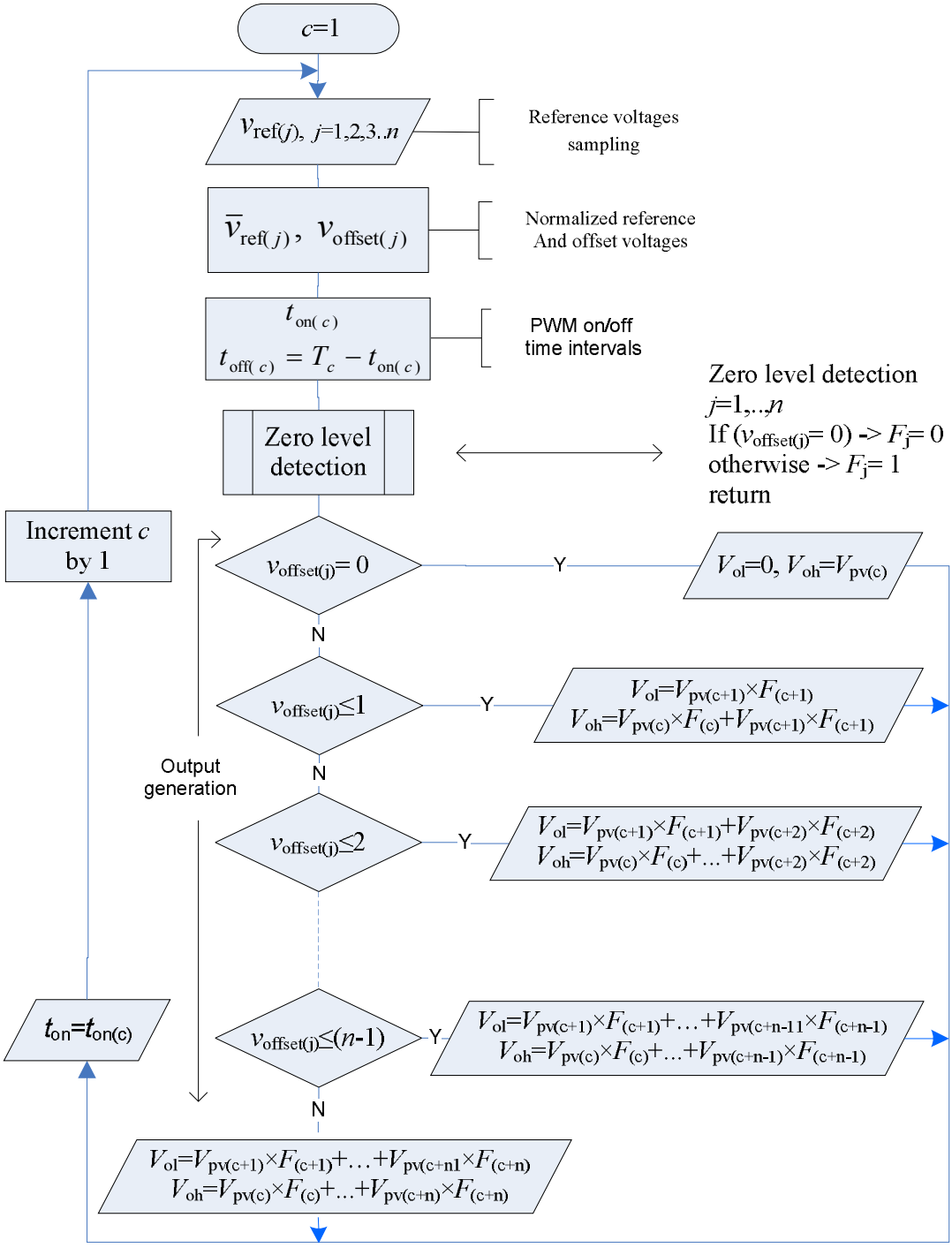


Fig.5.19: Generalized improved PV permutation algorithm.

The partial shading causes current drop in the relevant PV sources, so the inverter switches S1i to Sni are used to achieve two tasks; to track the MPP of each PV source and to establish the multilevel output waveform. The MPPT and PV permutation algorithms have to perform both tasks with asymmetrical currents produced from the PV sources, so it is normal to expect a rise in the unwanted output harmonics. For example, if the load impedance has matched the series connected PV sources under specific partial shading level then the switches S1i to Sni

will be on continually results in square wave output waveform. For that finding an improved algorithm is so important to decrease the consequences of the partial shading problem especially in case of more input PV sources.

5.3 System Simulation under Partial Shading Conditions

The achieved SSA models of the multilevel DC-link inverter are used here as well to show the validity of the presented PV permutation algorithms. Five, seven, nine and eleven level DC-link inverters are simulated under partial shading where the voltage and power waveforms are presented. For comparison purposes, the fast Fourier transform (FFT) is applied to find the voltage spectra and the total harmonics distortion (THD) is calculated for the first thousand harmonics. Fig.5.20 gives the I-V characteristics of the PV sources for different irradiance levels which used in the simulation, the MPP is also presented for each curve. Table 5.7 shows some of the system parameters used.

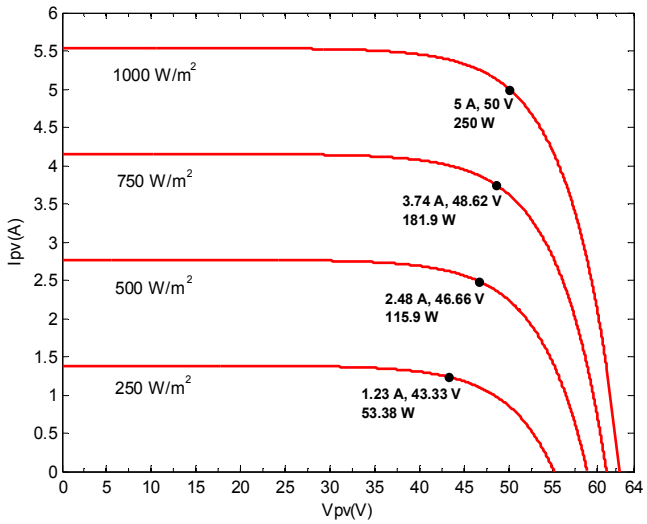


Fig.5.20: I-V PV source characteristics for different irradiance levels.

TABLE 5.7: System Parameters used in Simulation of PV Permutation Algorithm

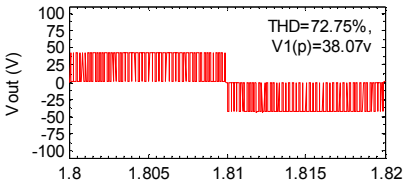
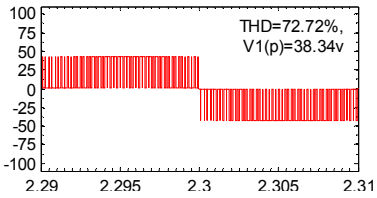
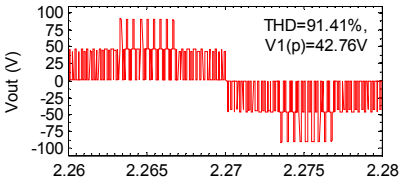
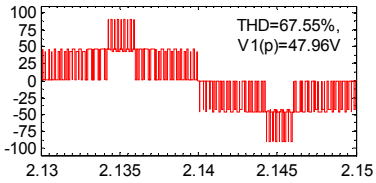
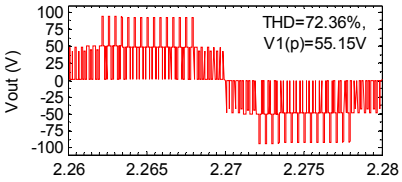
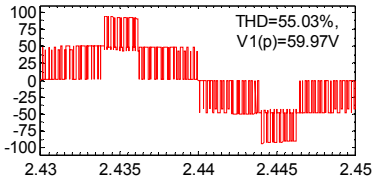
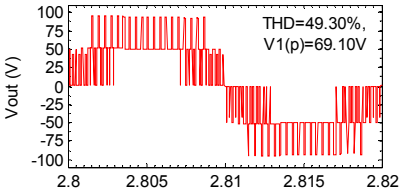
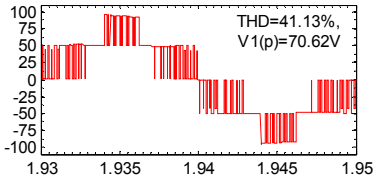
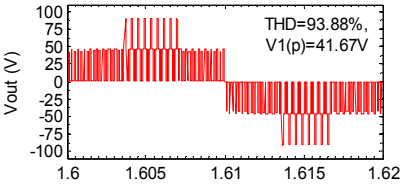
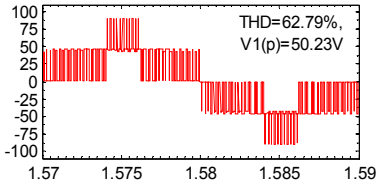
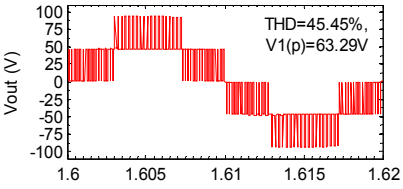
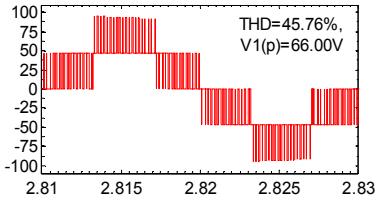
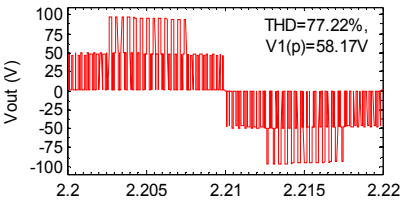
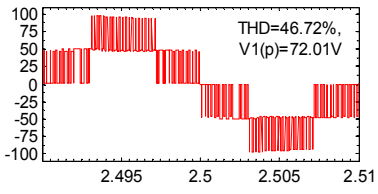
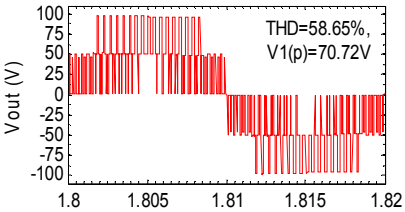
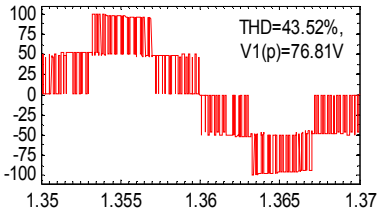
P_{mpp}	250 W	K_p	0.1	K_i	100
$C_{PV1,..,n}$	5500µF	MPPT (C)	0.5 V	f_r	50Hz
R (5-level)	8.5 Ω	R (7-level)	8.5 Ω	R (9-level)	18.5 Ω
R (11-level)	23 Ω	M_f(5-level)	100	M_f(7,9,11-level)	300

5.3.1 Five-level DC-link Inverter under Partial Shading

The PV permutation algorithm as well as the improved algorithm are applied to the two PV sources DC-link inverter with a resistive load. As is shown in Fig.5.21, the improved algorithm gives better voltage waveforms comparing with the conventional results of the PV permutation algorithm under different partial shading conditions. Table 5.8 gives a comparison between the two algorithms in terms of the output quality, where the THD along with the amplitude of 50Hz fundamental harmonic (V_1) are presented. Under partial shading conditions, the two PV sources are operated exactly at the MPP which are pointed out in Fig.5.20, the both algorithms gave the same results with respect to the extracted power. Fig.5.22 illustrates the transient power waveforms of some applied irradiance levels.

TABLE 5.8: THD and Fundamental Harmonic of Five-level Voltage by Using PV Permutation Algorithm and the Improved Algorithm

Irradiance percentage (%)		PV permutation algorithm		Improved PV permutation algorithm	
PV1	PV2	THD (%)	$V1$(p) V	THD (%)	$V1$(p) V
25	25	72.75	38.07	72.72	38.34
25	50	91.41	42.76	67.55	47.96
25	75	72.36	55.15	55.03	59.97
25	100	49.30	69.10	41.13	70.62
50	25	93.88	41.67	62.79	50.23
50	50	45.45	63.29	45.76	66.00
50	75	77.22	58.17	46.72	72.01
50	100	58.65	70.72	43.52	76.81
75	25	72.56	56.71	57.77	57.00
75	50	80.37	57.66	50.07	68.67
75	75	40.52	82.01	40.24	82.72
75	100	52.70	79.85	41.73	82.22
100	25	55.30	69.40	40.62	69.43
100	50	56.59	71.66	46.26	74.51
100	75	52.88	78.52	40.96	82.84

G_1-G_2 (W/m^2)	PV permutation algorithm	Improved PV permutation algorithm
250-250		
250-500		
250-750		
250-1000		
500-250		
500-500		
500-750		
500-1000		

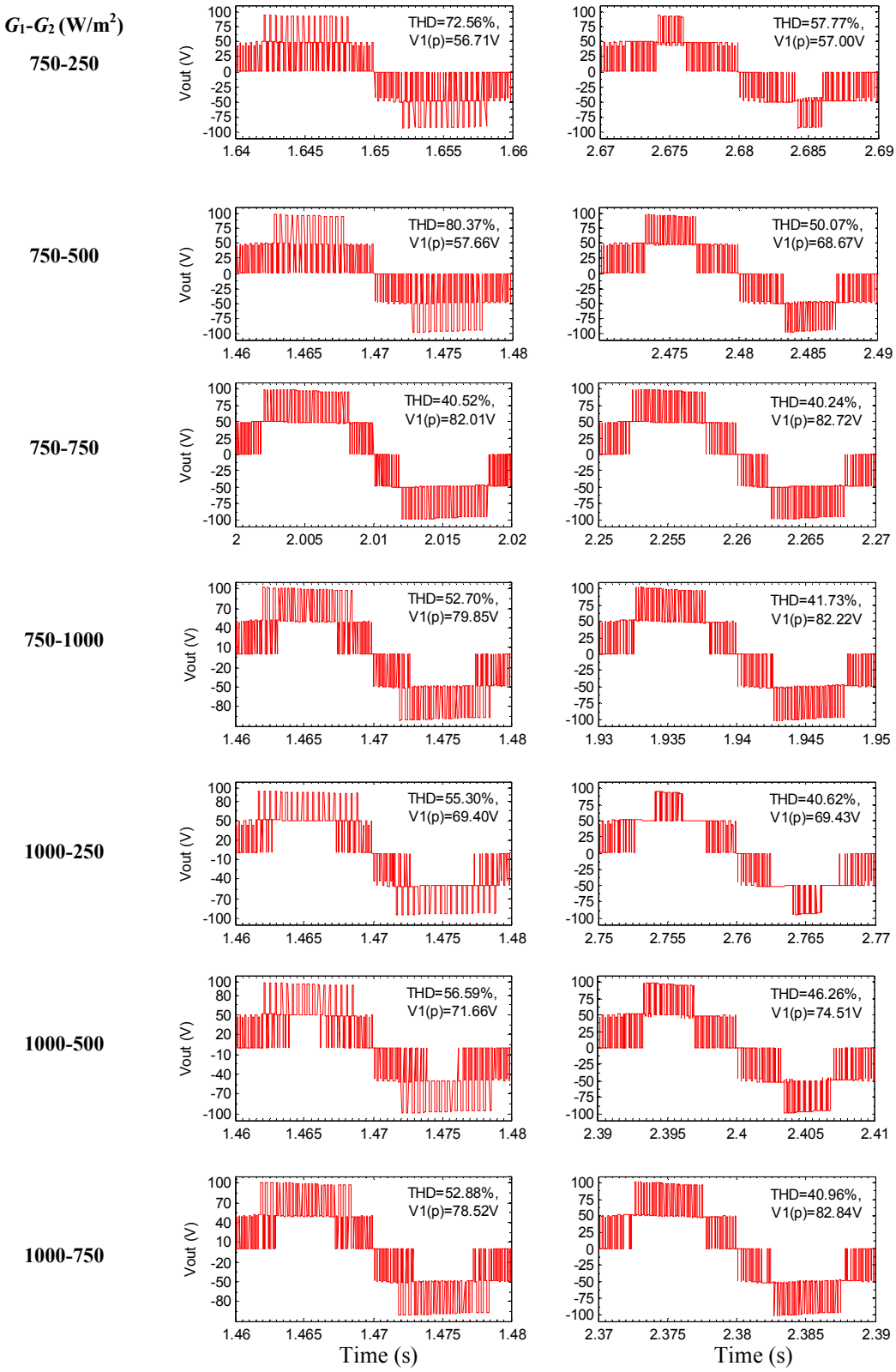


Fig.5.21: Five-level inverter voltage waveforms under different partial shading levels achieved via PV permutation algorithm and the improved algorithm.

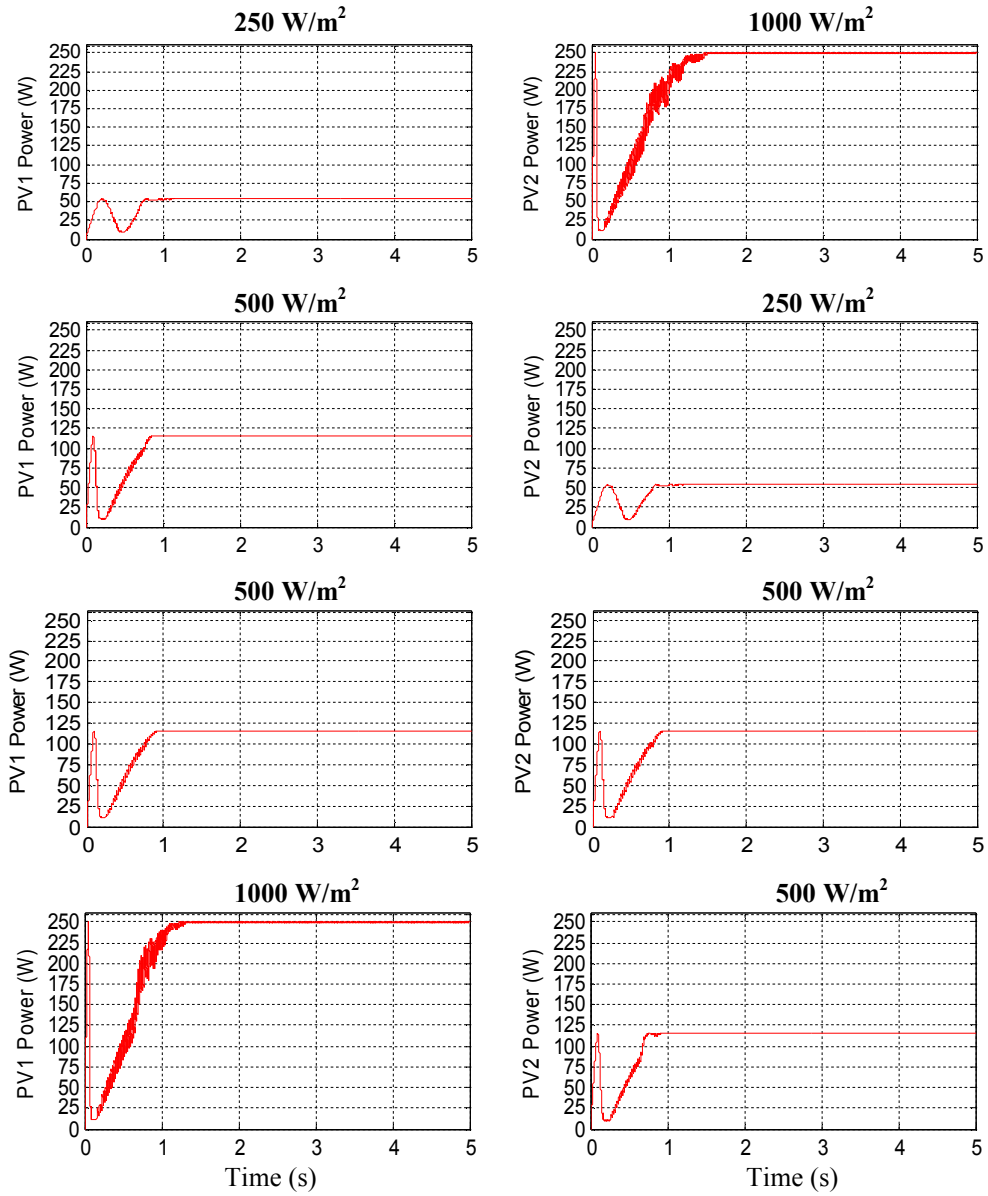


Fig.5.22: Transient power waveforms of PV1 and PV2 of the DC-link inverter under different partial shading conditions.

It is clear in Fig.5.22 that under uneven applied irradiance, each PV source generates its maximum power without affecting another PV source.

5.3.2 Seven-level DC-link Inverter under Partial Shading

Another comparison was made but by using the seven-level inverter with R load where three PV sources are connected. As can be seen in Fig.5.23, at 1000-500-1000 W/m^2 irradiances applied to PV1, PV2 and PV3 respectively, the improved algorithm generates much better output waveform (THD=35.13%, $V_{1(p)}$=110.78V) than that was achieved by the PV permutation algorithm (THD=57.41%, $V_{1(p)}$=95.81V). The

same Figure shows other partial shading conditioned applied. The both algorithms enable the PV sources to be operated at their MPPs.

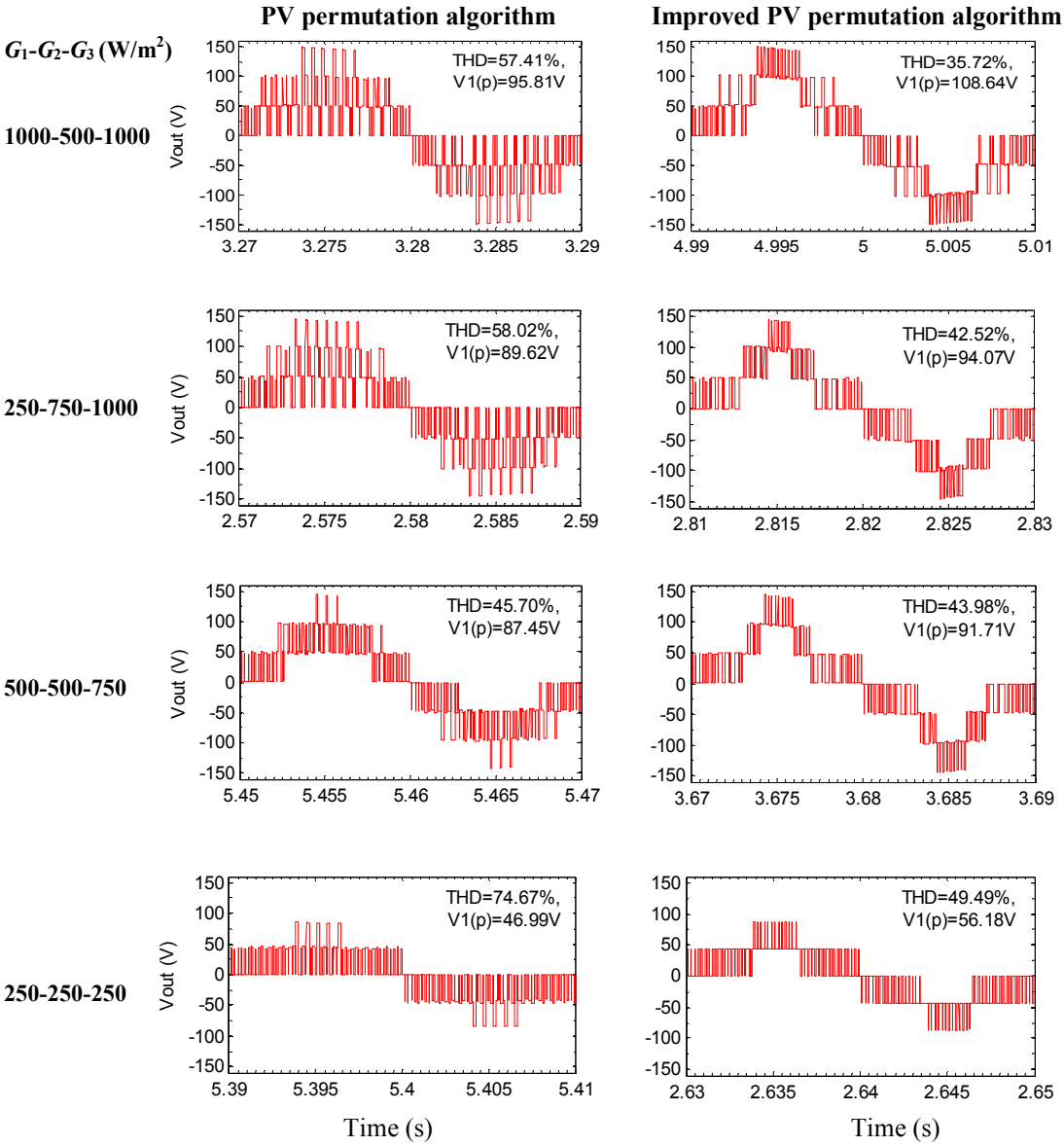


Fig.5.23: Seven-level inverter voltage waveforms under different partial shading levels achieved via PV permutation algorithm and the improved algorithm.

As can be seen, the improved algorithm offers lower distortion than that achieved by the PV permutation algorithm. More results are presented in the next sections for nine and eleven-level inverters.

5.3.3 Nine-level DC-link Inverter under Partial Shading

The results of DC-link inverter supplied by four PV sources, which are exposed to different levels of irradiance, are listed in Fig.5.24. The Figure illustrates the achieved voltage and power waveforms under different irradiance levels. The power

waveforms show that the used PV sources are operated at their MPP under partial shading and the power delivered to the load is the algebraic summation of the extracted power generated by the system PV sources. The THD and the fundamental peak voltage are presented for each voltage waveform.

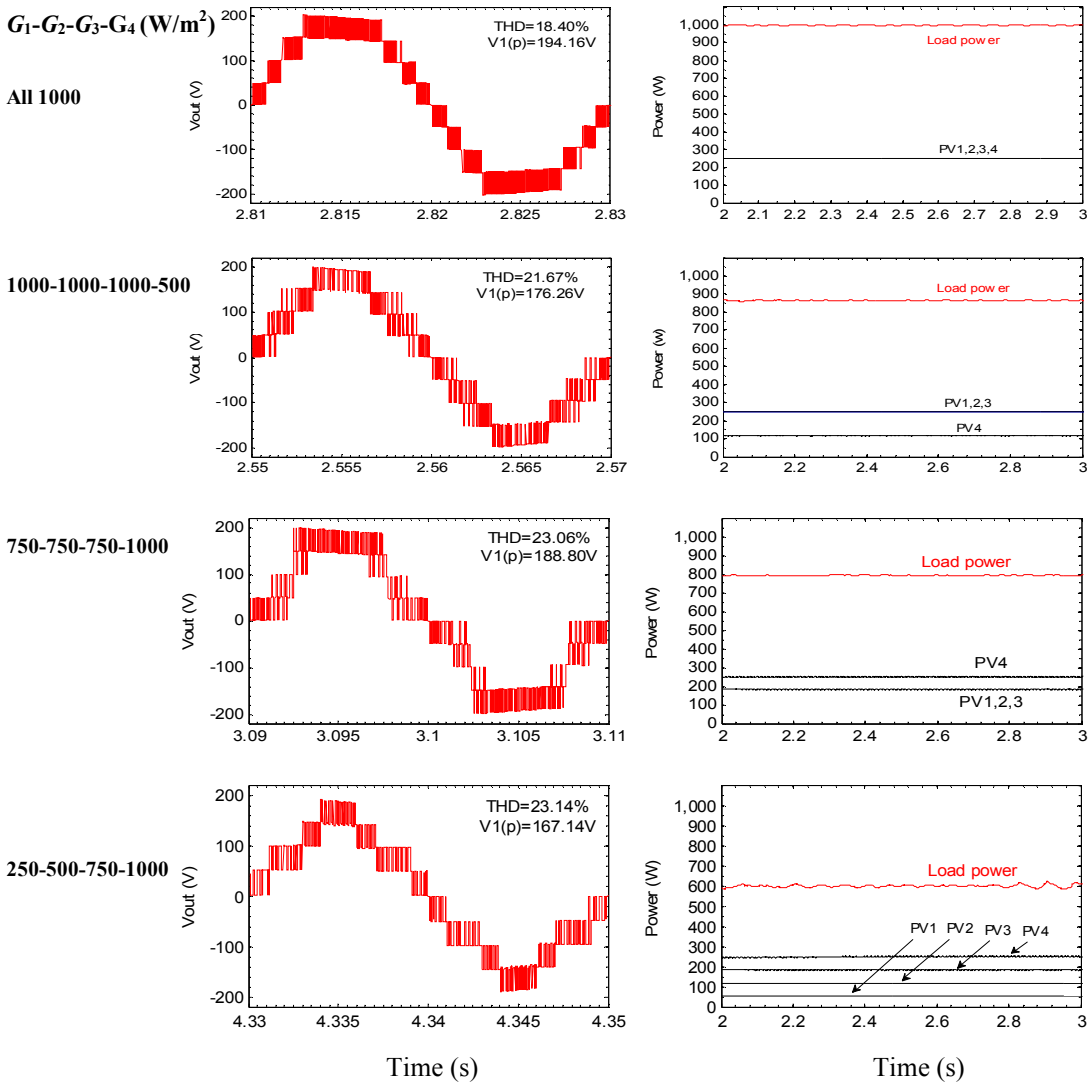


Fig.5.24: Nine-level inverter voltage waveforms under different partial shading levels achieved via the improved PV permutation algorithm.

5.3.4 Eleven-level DC-link Inverter under Partial Shading

To show the validity of the introduced system towards overcoming the PV partial shading problem, five partially shaded PV sources are applied. The output voltage waveforms achieved across a resistive load are shown in Fig.5.25, where several uneven irradiances are applied to the PV sources. The power waveforms show the operating points of the PV sources and by comparing them with Fig.5.20, it is clear that the all the PV sources are operated at their MPPs. Also, the load power shows

that the total extracted power is delivered to the load. Moreover, good quality waveforms are accomplished as is clear from the calculated THD.

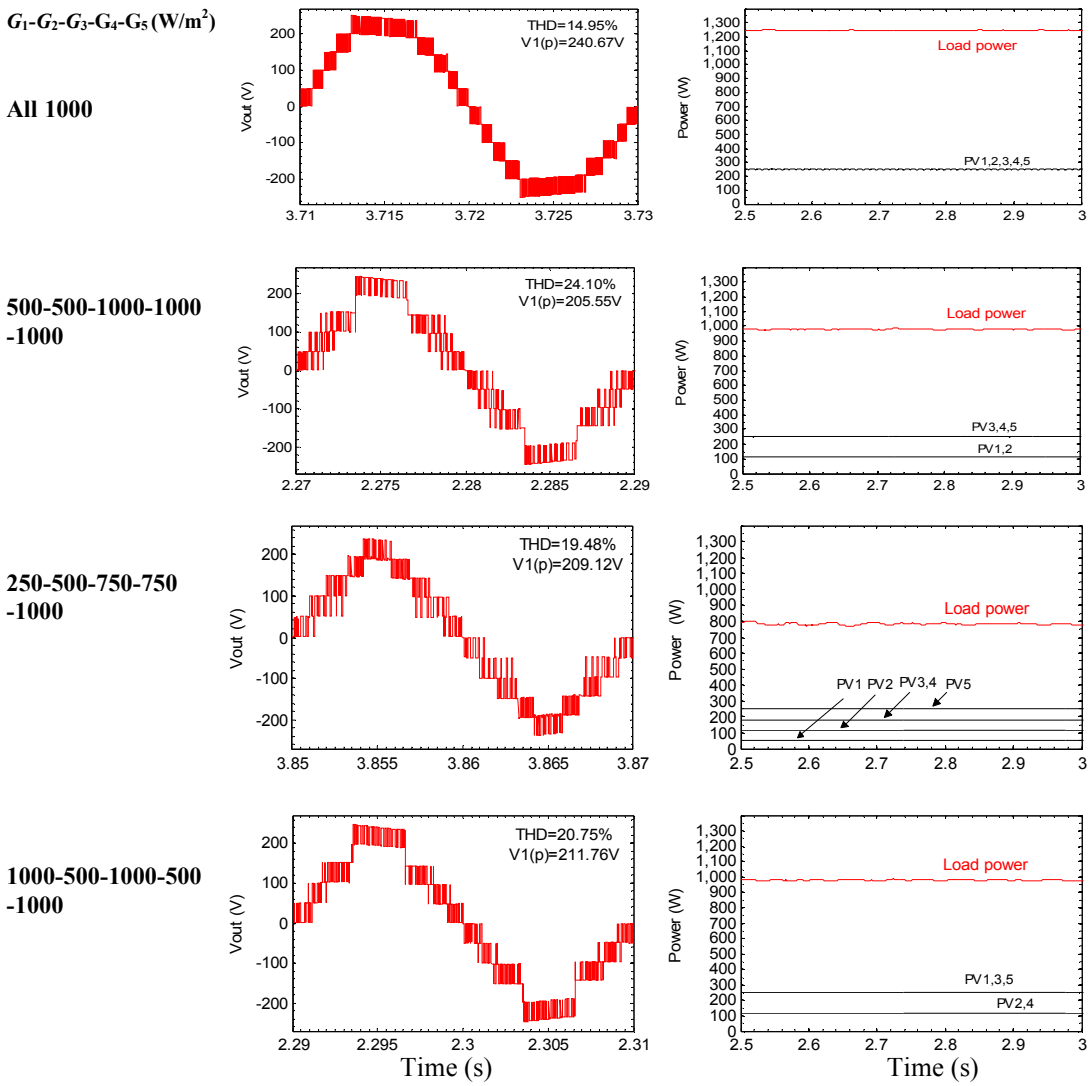


Fig.5.25: Eleven-level inverter voltage waveforms under different partial shading levels achieved via the improved PV permutation algorithm.

5.3.5 Dynamic Conditions of the Applied Partial Shading

Irradiance changes are applied to the PV sources as shown in Fig.5.26, where up to 2s and after 6s time; full irradiance is applied to the both PV sources so the generated power from each source is 250 W. Total power of 500 W is delivered to the load as it is illustrated. Within time between 2s and 6s, 50% of the irradiance is applied to PV2 source while PV1 is at full irradiance. As a result of that shading, PV2 power is dropped down to 116 W which is exactly the PV MPP at 50% shading (500 W/m^2). Moreover, PV1 has never been affected by the shading applied to PV2 and the total delivered power to the resistive load is about 366 W.

Another example is presented here which is for three PV sources system. The applied irradiance waveforms as well as the generated PV power for the sources PV1, PV2 and PV3 are shown in Fig.5.27. It is clear that all the PV panels operate at their MPP and the total delivered power is the summation of the extracted powers.

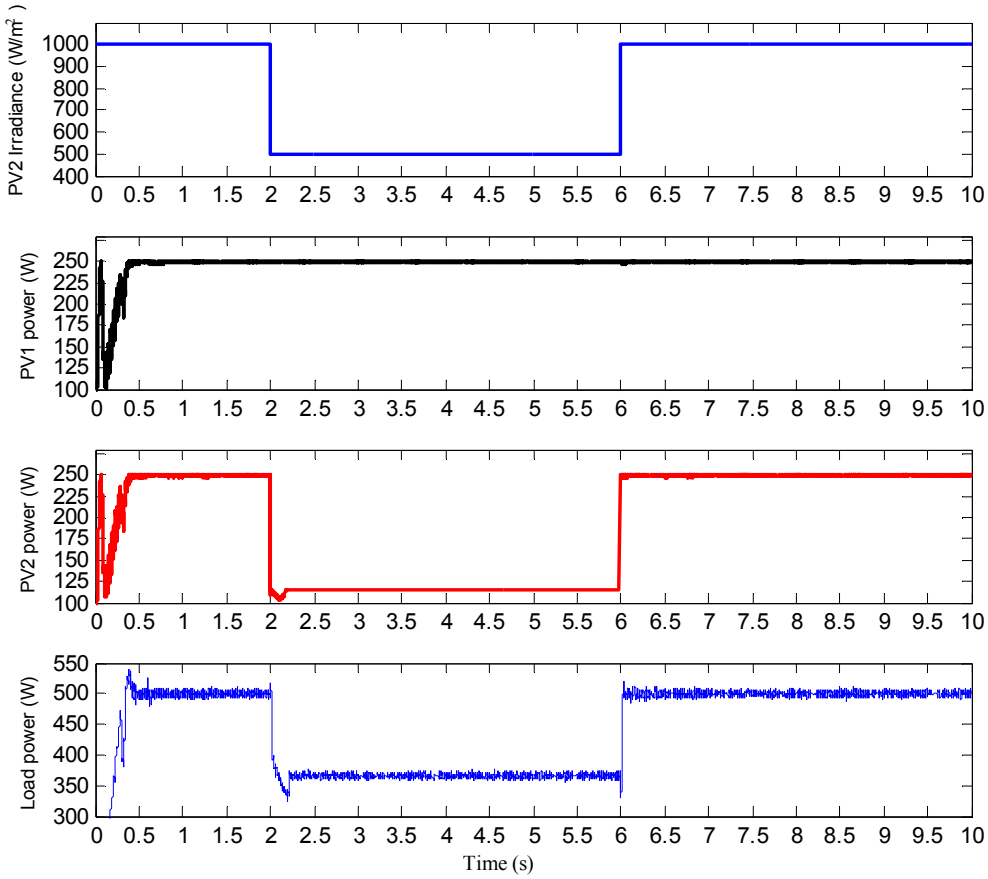


Fig.5.26: Irradiance waveforms, the extracted power of PV1 and PV2, and load power of five-level DC-link inverter.

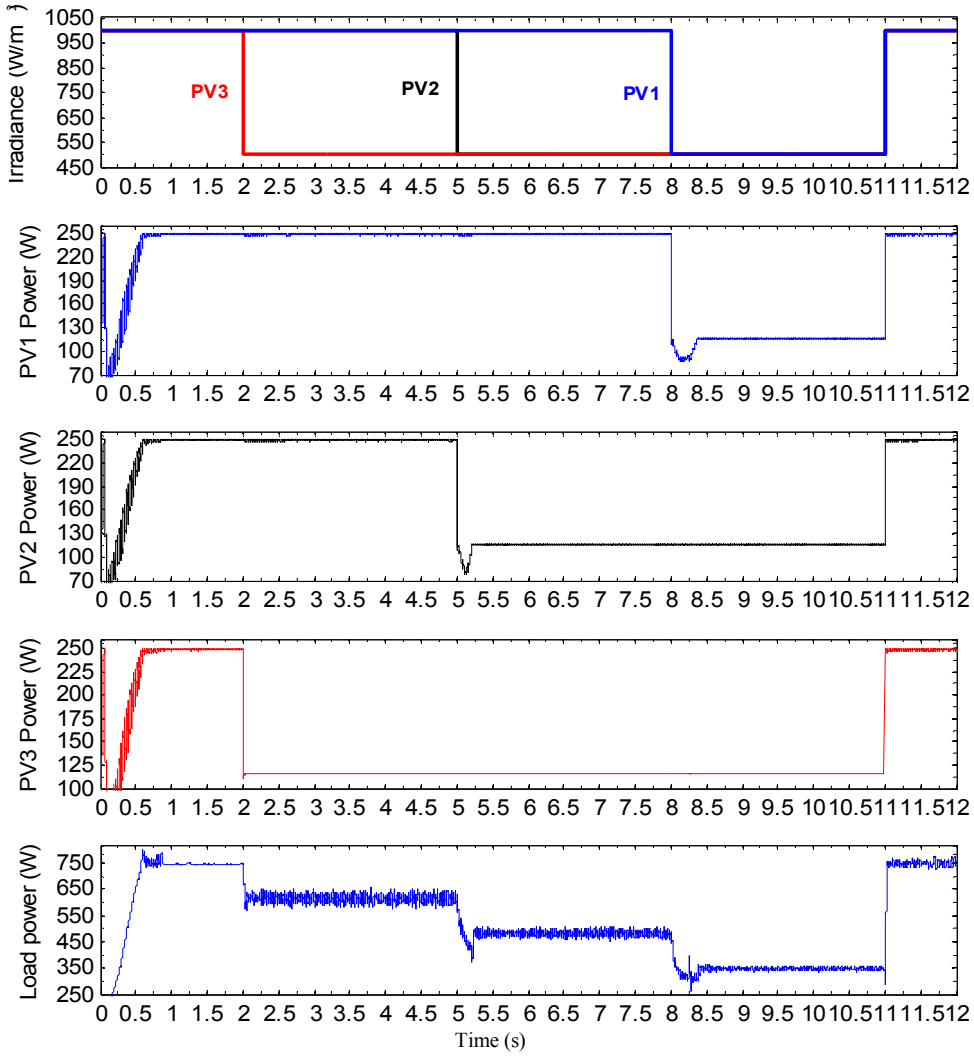


Fig.5.27: Irradiance waveforms, the extracted power of PV1,2,3, and load power of seven-level DC-link inverter.

5.4 Summary

In this chapter, the mathematical modelling of the DC-link inverter circuits were achieved via the state space averaging (SSA), and generalized forms of those modules were accomplished so they can be used with any inverter level.

The achieved SSA models were used in simulation along with the introduced PV permutation algorithm, where the results were achieved for different loads and under even and uneven irradiance conditions. An improved PV permutation algorithm was introduced to improve the AC output waveforms where satisfactory results were accomplished under static and dynamic partial shading conditions.

Chapter 6

Experimental Implementation

The experimental confirmation is a significant factor to verify the introduced ideas of control which were simulated by mathematical modules. This chapter describes the experimental setups for implementation of theatrical studies.

Regarding the controller device, eZdsp^{TM} F28335 is selected to implement the required signal processing, calculations of the control algorithm and to generate the PWM control signals. The used DSP has sufficient memory to deal with long control algorithms and the Real Time Data Exchange (RTDX) with Graphical User Interface (GUI). A satisfactory processing speed shortens the execution time of the control algorithms and the MPPT. Also, it has adequate number of ADC channels and PWM ports to handle the necessary sensing information and switches control signals respectively.

The chapter describes the used PV source and the applied lighting, the multilevel DC-link inverter, dc-dc buck converter and the circuit used in displaying the PV I-V characteristic, along with all necessary interface, driving and control elements. The required low-voltage DC power supply regulators, buffering, opto-isolation, and MOSFET gate driving are also presented. Finally, the RTDX processing and the designed GUI window are presented.

6.1 PV Source

The small solar panel SSP-10W is selected for using in the experimental setup, because of its small size and suitable output voltage. Due to the lack of sunlight on demand, finding another suitable source of lighting is essential to carry on the experimental work. Selecting large PV panel requires more light energy and consequently more electrical power to reach the full irradiance level of 1000 W/m^2

(STC) especially with applications requiring separated PV sources with separated lighting sources.

The SSP-10W module shown in Fig. 6.1 consists of 36 monocrystalline solar cells which are connected in series. The cell dimensions are 12.5×125 mm and the external module dimensions are 340×285×25 mm, so the size of the PV panel is very suitable for multi source applications and lighting environment. Table 6.1 shows the specifications of the used PV source provided by the manufacturer at STC (1000W/m^2, AM 1.5, 25°C).

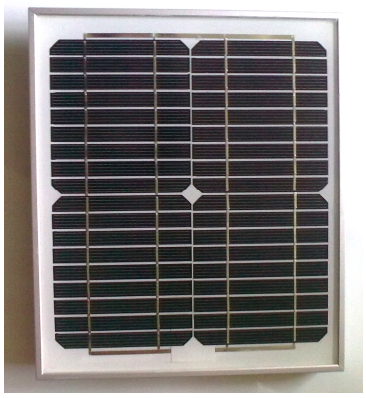


Fig.6.1: SSP-10W PV module

TABLE 6.1: SSP-10W Module Specifications

Quantity	**Value**
Maximum power, P_{mpp}	10 W
Power tolerance	± 5%
Maximum power point voltage, V_{mpp}	17.2 V
Maximum power point current, I_{mpp}	580 mA
Open circuit voltage, V_{oc}	21.6 V
Short circuit current, I_{sc}	690 mA
Cell efficiency	16.8%
Operating temperature range	-40°C to +85°C
Weight	1.3 kg

5.2 Lighting Source

There are different sources of lighting which can be considered to maintain the required irradiance for the experimental work. As illustrated in Fig.6.2, the solar

irradiation can is divided into ultraviolet rays, infrared rays, and visible light. Considerable amount of the sun energy is concentrated in the visible light (Fig.6.3) [80].

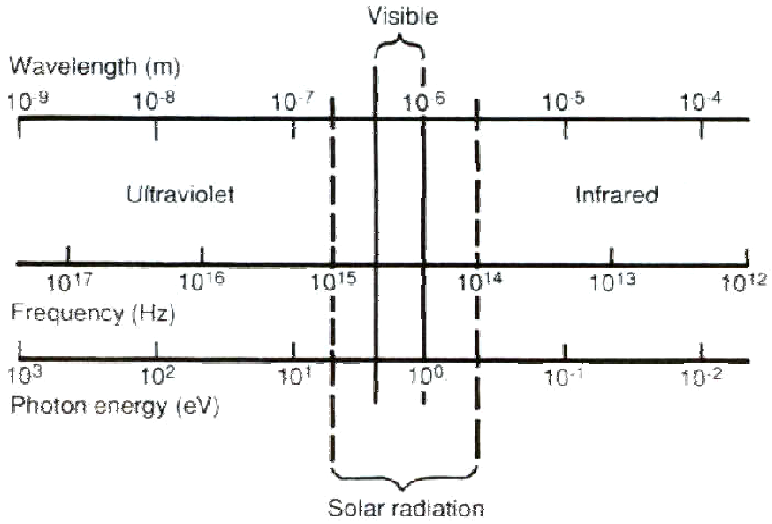


Fig.6.2: Electromagnetic spectrum [80].

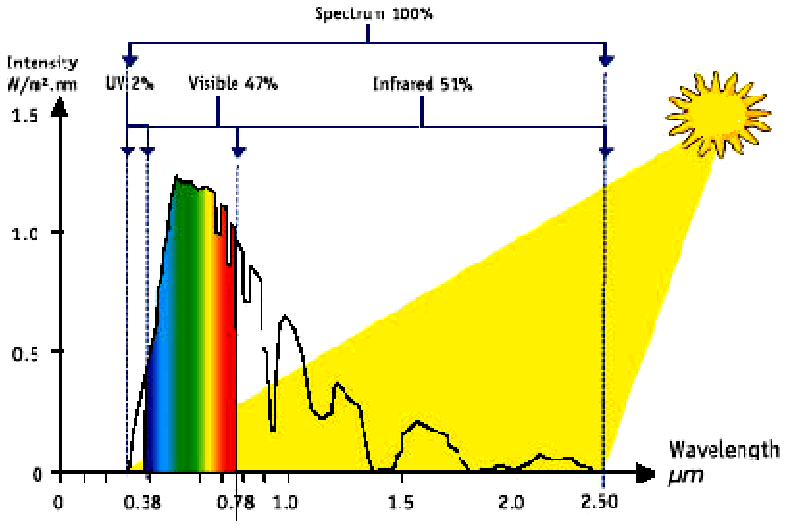


Fig.6.3: Solar spectrum [81].

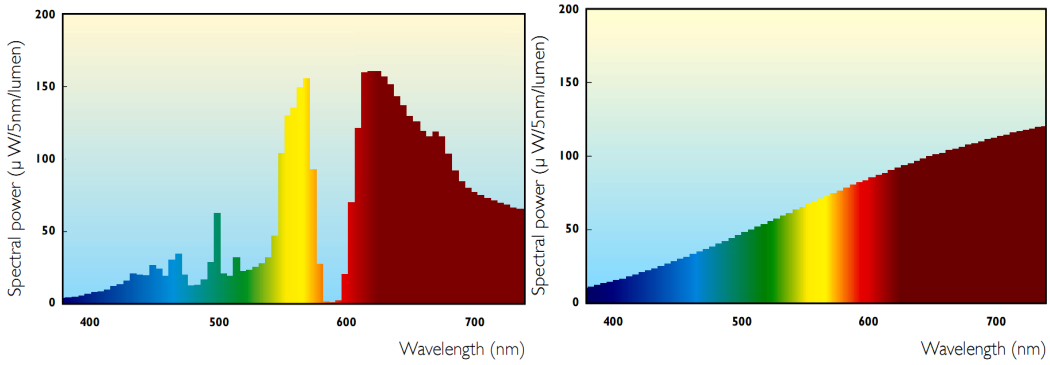
In the monocrystalline silicon PV cells just 15% to 24% of the received solar energy is converted to electrical energy. This is because the energy of solar photons, which have energy smaller than the band gap of the monocrystalline silicon, is reflected out of the cell by the back cell coating. Most the photons energy, which is similar to the energy gap of monocrystalline silicon, will be converted to electricity while any surplus photons energy is wasted as heat. In other words, the peak sensitivity of the monocrystalline silicon cells is for irradiations of 0.8-0.9 μm wavelengths, which unfortunately do not mach the peak of the solar spectrum as it is noticed in Fig.6.3 [82, 83].

It is difficult to simulate the solar radiation by using artificial lighting (bulbs) in particular each bulb type has different radiation spectrum, so mixing different lightings can be helpful in this case. However, apart from the incandescent and the halogen bulbs, the other bulbs types which use ballast and igniter, cannot be dimmed easily causing apply shading during the experiment is not an easy task. Table 6.2 shows different types of bulbs and the associated lumens efficiency.

TABLE 6.2: Bulbs and Their Related Lumens Efficiency [84]

Radiation source	**Lumens per Watt**
Incandescent/halogen	12-26
Metal halide	80-90
High presser sodium	117
Fluorescent	52-84
Mercury vapor	50-60

It is clear from the table that the High Presser Sodium (HPS) bulb has the higher lumens efficiency between the listed bulbs and that can be also shown in Fig.6.4a where the HPS spectrum is close in shape to the solar spectrum. Fig.6.4b illustrates the spectrum produced by the halogen bulb. As can be seen, there is increase in the power towards the infrared wavelengths and that means significant amount of the electricity are converted to heat instead of light. Both the halogen and the HPS bulbs were applied to the SSP-10W PV module and the halogen bulbs is selected according to the results shown in the next chapter and also because of the dimming obstacle associated with the HPS bulbs.



(a) (b)

Fig.6.4: Spectrum generated by 100 W (a) HPS bulb and (b) halogen bulb [85].

6.3 Circuit for Emulation of the PV I-V Characteristic

To achieve the I-V characteristic of a PV source, a variable resistive load is used. In [86], a MOSFET is used to emulate the variable resistive load by controlling the signal applied to its gate. Short and open circuit loads are accomplished by MOSFET saturation and cut-off states respectively, and different impedance values are achieved within the MOSFET linear region. In the linear region the MOSFET will dissipate the generated PV power and therefore the operation in that region has to be as short as possible.

Fig.6.5 illustrates the applied circuit in which a low-frequency AC signal, shifted by a DC offset, drives the gate of the STP24NF10 MOSFET.

With respect to the current sensing, the current generated by the PV module is sensed by means of a non-inductive shunt resistor 15FR100 of 0.1 Ω.

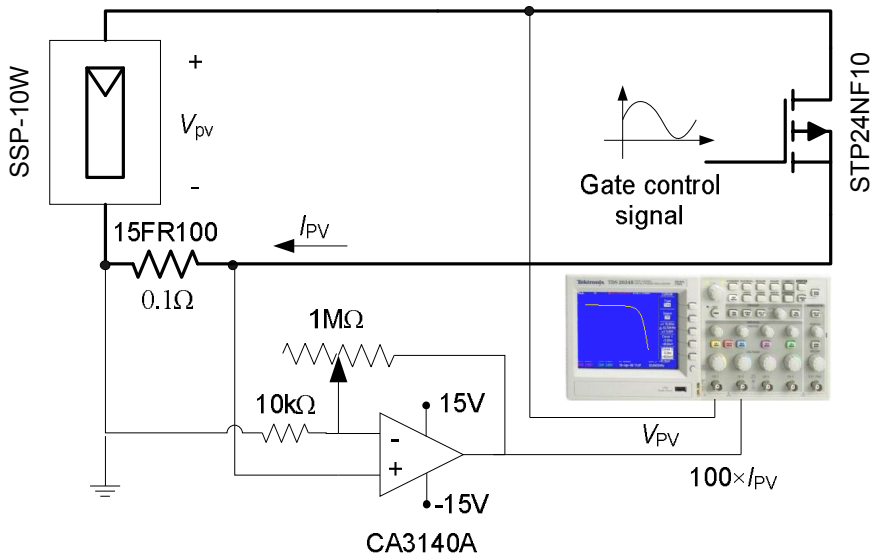


Fig.6.5: Circuit for emulation of PV module I-V characteristic.

The voltage drop across the shunt resistor indicates the extracted currant from the PV module. However, the maximum extracted current of the used PV module is relatively small (0.69 A) and consequently the maximum shunt resistor voltage drop (0.069 V) has to be amplified in order to display the I-V curve on the oscilloscope in XY mode. A non-inverting amplifier (CA3140A) is applied to scale the resulted voltage by a factor of 100.

6.4 DC-DC Buck Converter

A simple one switch buck converter has been implemented to test the closed loop control system, which is controlled by a DSP, and also to test and improve the MPPT algorithm for fast PV power tracking. Fig.6.6 illustrates the connection of the PV buck converter circuit along with the closed loop control. In this section most of the hardware circuits, which are used in the buck converter and the DC-link inverter, are described in detail. The auxiliary circuits of scaling, isolating and filtering, which are necessary for preparing the PV module voltage and current to be sampled via the DSP, as well as the required circuits for buffering, isolating and driving, which are needed to interface the DSP with the power switches, are included.

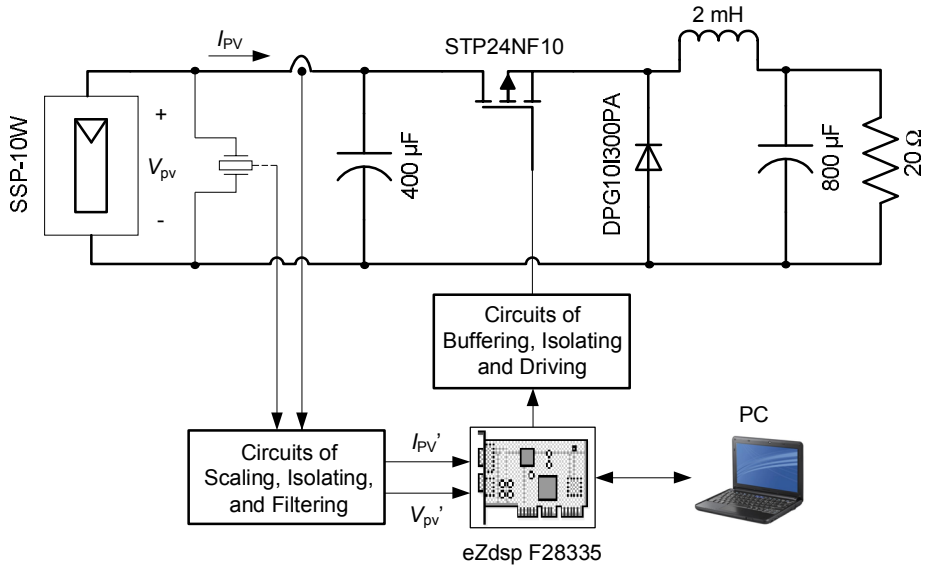


Fig.6.6: Circuit of the PV DC-DC buck converter system.

6.4.1 MOSFET and Diode Specifications

A STP24NF10 MOSFET is used in the experimental implementations, it has voltage and current ratings of 100 V and 26 A respectively. STP24NF10 is characterised with very low saturation resistance (0.055 Ω) and hence low conduction losses achieved. Also, the rise time and fall time are 45 ns and 20 ns respectively results in low switching loss. According to the implemented applications in this work, the voltage and current can reach maximum values of 64.8 V and 2 A respectively, the switching frequency is 5 kHz (i.e. the period of switching cycle is 200 µs), so the implemented converters are suitable to be used with higher ratings PV sources. Table 6.3 [87] describe some of the used MOSFET specifications.

TABLE 6.3: STP24NF10 MOSFET Specifications

Parameters	Value
Maximum drain to source voltage, V_{DS}	100 V
Maximum drain current, I_D	26 A
Maximum total dissipation power, P_{TOT}	85 W
Gate threshold voltage, $V_{GS(th)}$	3 V
Turn-on Delay Time, $t_{d(on)}$	60 ns
Turn-off-Delay Time, $t_{d(off)}$	50 ns

The high performance fast recovery diode DPG10I300PA has been used in the buck converter as well as the DC-link inverter for free-wheeling roles. The maximum repetitive reverse voltage (V_{RRM}) and average forward current ($I_{F(AV)}$) ratings of DPG10I300PA are 300 V and 10 A respectively. It characterized by low reverse recovery time (t_{rr}=35 ns), low forward voltage (V_F) and reverse current (I_R) where their ratings are 1.27 V and 1 μA measured at 25° C and $I_{F(AV)}$=10 A [88].

6.4.2 Current Sensing Circuit

A non-inductive shunt resistor 15FR100 of 0.1 Ω is used to sense the current generated by the PV module. The voltage drop across it will not exceed 0.069 V ($V_{sense}=I_{pv} \times 0.1$). However, the analogue to digital (ADC) of the DSP accepts input analogue signal range from 0 V to 3 V, so in this case a non-inverting amplifier is applied to scale the maximum voltage drop of the shunt resistor to the maximum allowed value of the ADC. The current sensing and scaling circuit is shown in Fig.6.7.

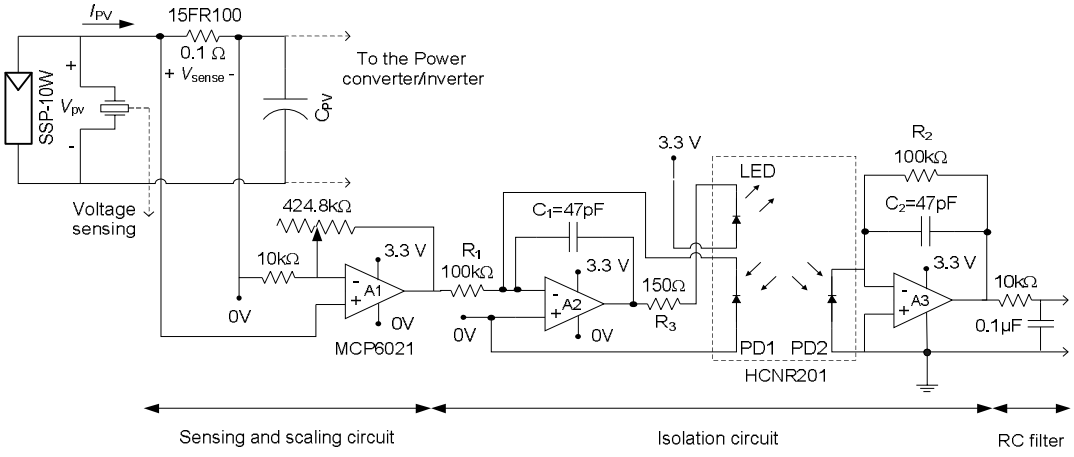


Fig.6.7: Current sensing and interfacing circuits.

The operational amplifier A1 (MCP6021) is used to establish the non-inverting amplifier of gain 43.48. For the isolation purpose between the PV power circuit and the DSP side, the high-linearity analog optocoupler (HNCR201) is employed. The optocupler contains two photodiodes which are illuminated by a LED. The light of the LED can be stabilized via the input photodiodes (PD1) in order to achieve linear LED emission. The generated linear emission resulted in linear photocurrent produced by the output photodiode (PD2).

The gain provided by the isolation circuit is described by the ratio between R_2 and R_1 (here R_1=R_2=100 kΩ). The capacitors C_1 and C_2 are compensation capacitors and they are used to increase the stability of the circuit as well as to provide a bandwidth limitation of almost 10 kHz. The final stage before the ADC of the DSP is a simple RC filter which offers noise suppression especially of that picked up via the wires [89].

6.4.3 Voltage Sensing Circuit

To implement the voltage sensing of the PV module, a similar circuit to the one shown in Fig.6.7 is applied with exception of the sensing and scaling circuit. The voltage sensing can be implemented either by voltage a transducer or simply by voltage divider. In this work 1 MΩ trimming potentiometer (3386G), followed by a unity gain amplifier, is used. It is essential not to load the PV module by the potentiometer, so a high resistance potentiometer is used. Also, the analogue buffer is applied to the output of the potentiometer in order not to load the potentiometer and to provide low output impedance to drive the next circuit. Fig.6.8 shows the voltage sensing circuit along with the interfacing circuit with the ADC of the DSP.

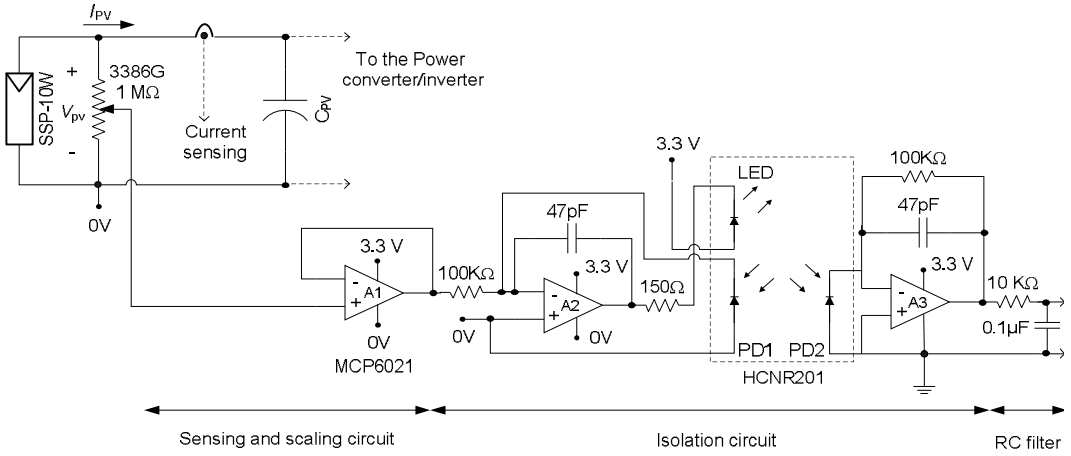


Fig.6.8: Voltage sensing and interfacing circuits.

6.4.4 MOSFET Driving Circuit

The high frequency PWM control signal generated via the DSP is applied to control the power MOSFET. The DSP control signal has to pass through several stages which are the digital buffer, digital optocoupler, and MOSFET driver. The high-speed CMOS logic buffer 74HCT244 is a non-inverting octal buffer with three-state outputs. It is applied directly after the DSP output ports in order to provide the well known buffer advantages. Also, to convert the 3.3 V DSP TTL output voltage to 5 V and as protection of the DSP output ports.

To achieve a digital optical isolation between the DSP side and the power converter side, Avago 6N137 digital optocoupler is applied after the logic buffer. Fig.6.9 illustrates the circuit connection of the optocoupler. A resistor of 470 Ω is used to limit the current of the LED to about 7.5 mA. The output of the optocoupler IC is an open collector Schottky-clamped transistor output, so a pull-up resistor (R_P) of 1 kΩ is used. Also, a decoupling capacitor of 0.1 μF is applied to the optocoupler supply terminals.

Especially under high speed switching, it is essential to provide adequate amount of current to charge the MOSFET gate capacitance as fast as possible. Also, to reach fast MOSFET turning off, the MOSFET gate capacitance has to be discharged quickly. For that reason, the high-speed power MOSFET driver TC4427A is employed. TC4427A is able to charge and discharge a MOSFET gate capacitance of 1000 pF within 30 ns time (the used MOSFET has input capacitance of 870 pF). Also, TC4427A characterized by very low output impedance, so the desired MOSFET state can not be changed by noise or considerable transient states. Fig.6.9 shows the overall interfacing and driving circuit.

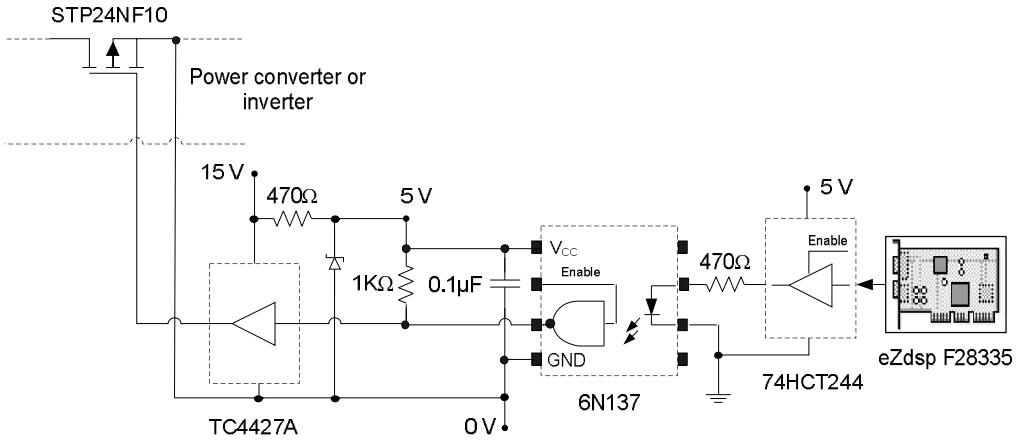


Fig.6.9: Interfacing and MOSFET driving circuits.

6.4.5 DC Power Supplies

The DC power supplies used in the sensing and driving circuits shown before, can be divided into two units which are illustrated in Fig.6.10. The first unit is the power supply related to the DSP side of the optocouplers which applied in the current sensing, voltage sensing and driving circuitries alike; all are powered by a common supply which has a ground connected to the ground of the DSP.

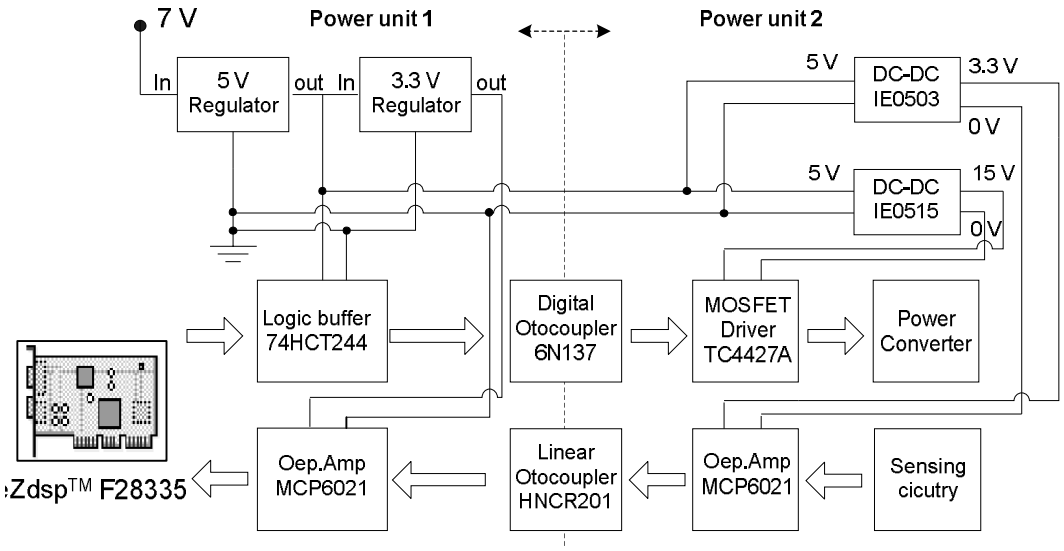


Fig.6.10: DC power supply connections.

The second unit is the power supply related to the power side of the optocoupler, where an isolated supply is allocated for each PV module current and voltage sensing circuitry as well as each MOSFET driving circuit. These individually isolated supplies can be achieved via the 1 Watt DC-DC IE series converters. A IE0503 is used to provide 3.3 V isolated supply for a sensing circuit, whereas a IE0515 is used to offer 15 V isolated supply for a driving circuit and both of them are powered by a common 5 V supply.

6.5 DC-link Inverter

The five-level (two input PV sources) inverter shown in Fig.6.11 as well as the seven-level (three input PV sources) inverter shown in Fig.6.12 are controlled via eZdsp™ F28335 development system to deliver the maximum extracted power and maintaining the PV sources operating at their MPP under the applied irradiance level. As was done with the buck converter, the experimental implementation of the DC-

link inverter involved three main parts. Firstly, the power circuit which includes the PV modules (SSP-10W), the inverter, and R/R-L loads. Secondly, the sensing and interfacing circuitries which contains the voltage/current sensing, scaling, isolating, filtering, buffering, and driving circuits.

Finally, the DSP inverter control which provides the ADC, PI controllers, MPPT algorithms, PV permutation algorithm, and the inverter PWM control signals.

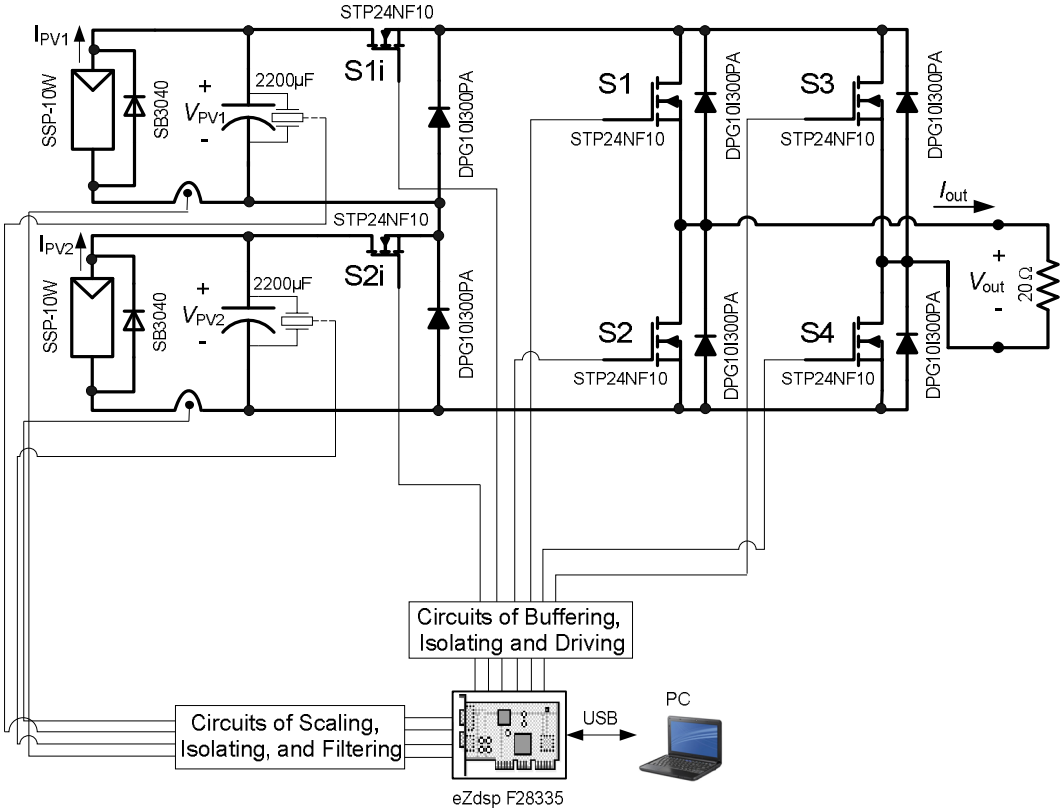


Fig.6.11: Circuit of the five-level DC-link inverter system.

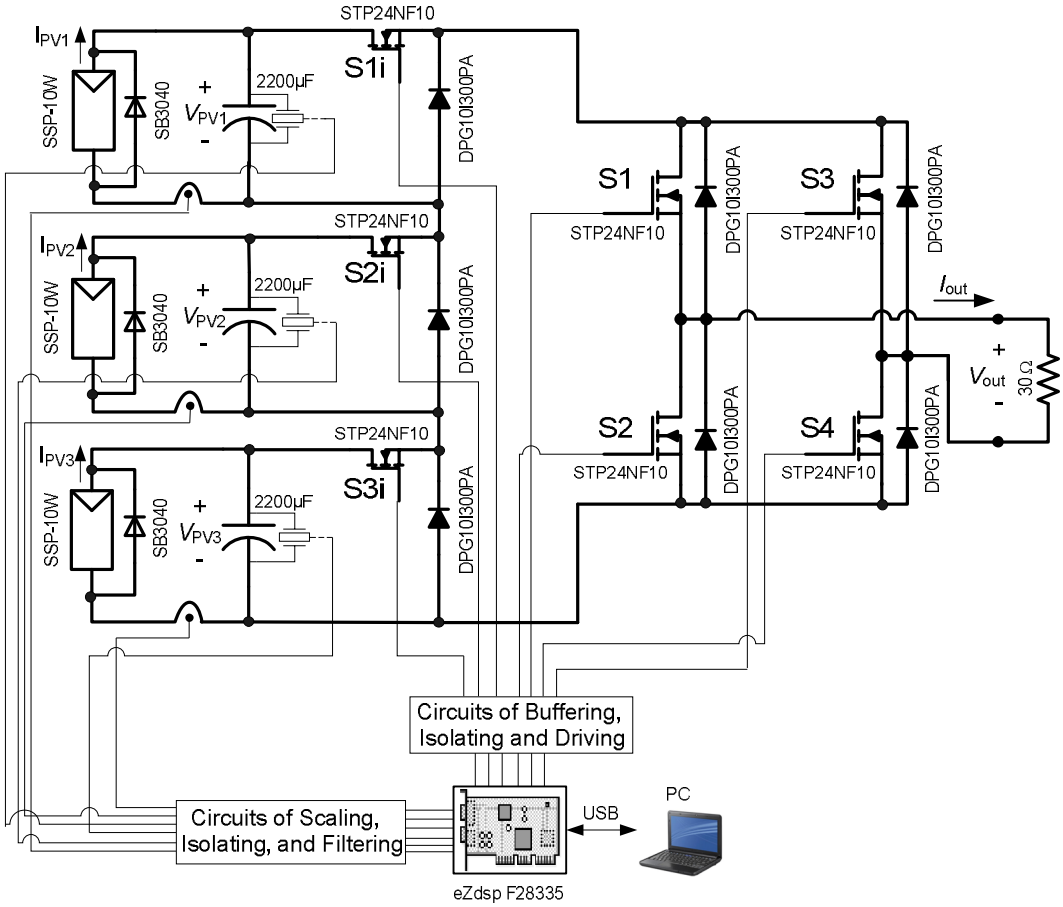


Fig.6.12: Circuit of the seven-level DC-link inverter system.

As can be seen, each PV module is equipped by a SB3040 bypass diode, where it bypasses the shaded PV module in case of the PV module is entirely shaded or for any unexpected experimental error.

The SB3040 Schottky diode characterised by maximum forward voltage of 0.39V and maximum average forward current of 30 A. The 74HCT244 octal buffer IC includes 8 logic buffers, six of them are used in the five-level inverter and seven logic buffers are applied in case of the seven-level inverter. The same circuits descried previously for scaling, isolating, filtering, buffering and driving are applied in the DC-link inverters shown in Figures 6.11 and 6.12. The overall circuit, which is implemented experimentally, of the seven-level inverter is shown in Fig.6.13. Also, the relative three PV modules and their lighting are shown in Fig.6.14.

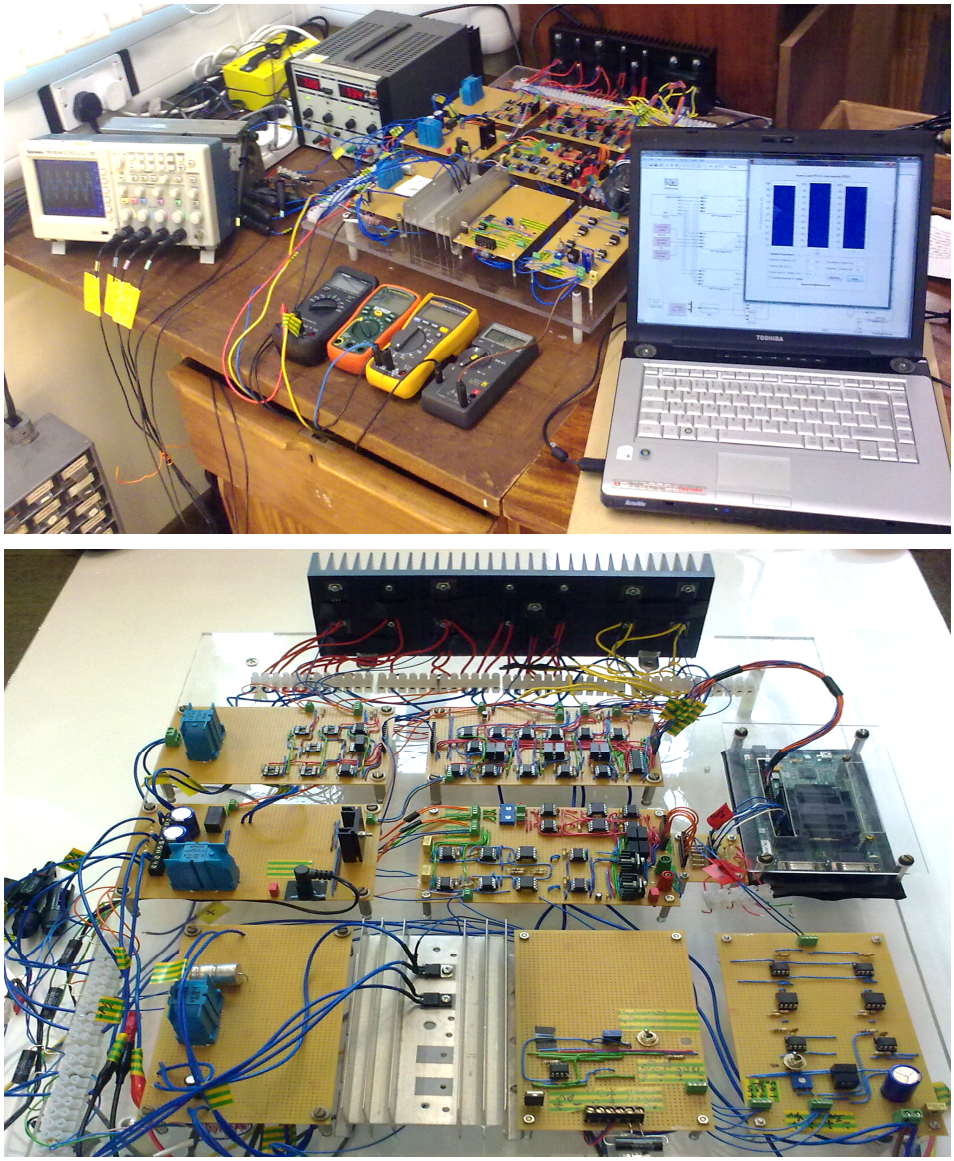


Fig.6.13: The overall experimentally implemented DC-link inverter system.

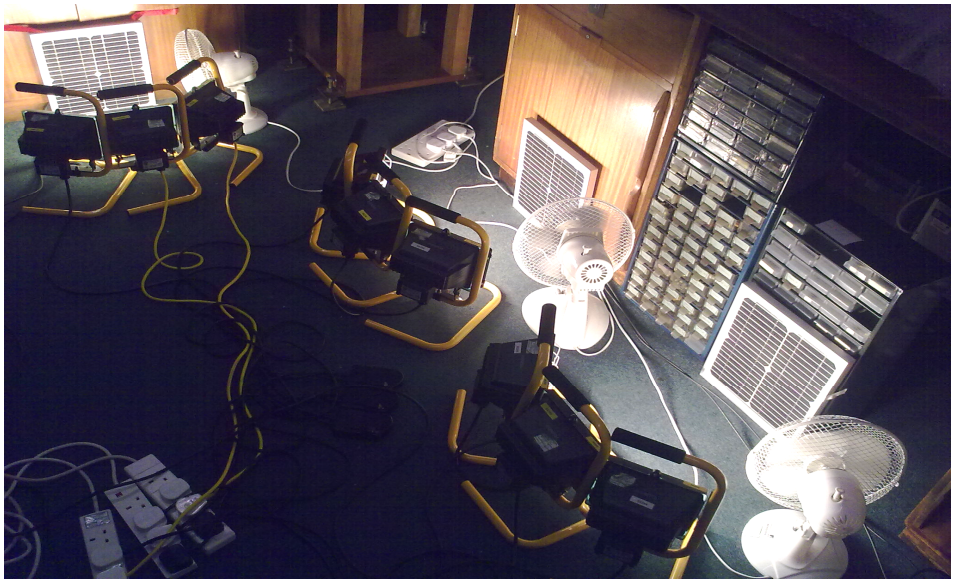


Fig.6.14: The three PV modules and their applied lighting.

6.6 Converter Control

The buck converter and the DC-link inverter presented in this work are controlled via DSP unit. The DSP is capable to carry out the necessary control operations at very high speed, such as performing the PV MPPT algorithms, the PI control, and the digital PWM calculations. Also, the DSP characterized by the on chip ADCs and the PWM output ports. For three PV modules, which are used in experiments, six ADC channels are required and five DSP general I/O pins three of them are configured to generate PWM control signals.

6.6.1 eZdsp™ F28335 Card

Based on the Texas Instruments TMS320F28335 digital signal controller, the eZdsp™ F28335 card can be used to implement the necessary control tasks. eZdsp™ F28335 includes an embedded USB JTAG controller interface, so it can be attached to the host PC via the USB port where the programming software are installed. TMS320F28335 can be programmed via C2000 Code Composer Studio ™ which enables the user to apply a high-level debugging language.

eZdsp™ F28335 operates at high speed (150 MHz) and it includes an on-chip 32-bit floating point unit which provides high accuracy and more computational capability compared with the fixed point DSPs. There are three 32-bit CPU timers. Regarding the eZdsp™ F28335 memory, it contains on-chip 68K bytes RAM, and 512K bytes flash memory. Also, it includes 256K bytes off-chip SRAM.

eZdsp™ F28335 includes up to 88 programmable general input and output pins 18 of them can be set to PWM outputs. Also, there are 12 bit ADC of 16 channels and 80 ns conversion time. Moreover, it contains CAN, UART, and SPI ports. Regarding the voltage levels, the DSP support 3.3 V for the digital input and output data. For the analogue input (ADC), the input range has to be within 0 and 3 V. The DSP is powered via 5 V DC supply [90].

6.6.2 Software Overview

The control programs of the buck converter and the DC-link inverter are written in C language via C2000 Code Composer Studio™ (CCS). The following sections illustrate the basic converter and inverter control flowcharts as well as the related

configuration of the event manager to generate the required PWM control signals. Also, the real-time Matlab Simulink workshop is described along with the RTDX and the GUI.

6.6.2.1 Buck Converter Control Flowchart and ePWM Event Manager

Fig.6.15 illustrates the flowchart main steps of the control program applied to the buck converter. The DSP ADC samples the voltage and current of the PV module simultaneously at 10 kHz, and then the present samples along with the previous samples are used to track the PV MPP by calculating the power difference, so to generate the reference voltage. The error arising from comparing the reference and the actual PV module voltage is applied to the PI controller which regulates the PWM duty ratio. Eventually, the achieved duty ratio is used to update the ePWM module counter-compare register to generate the PWM control signal.

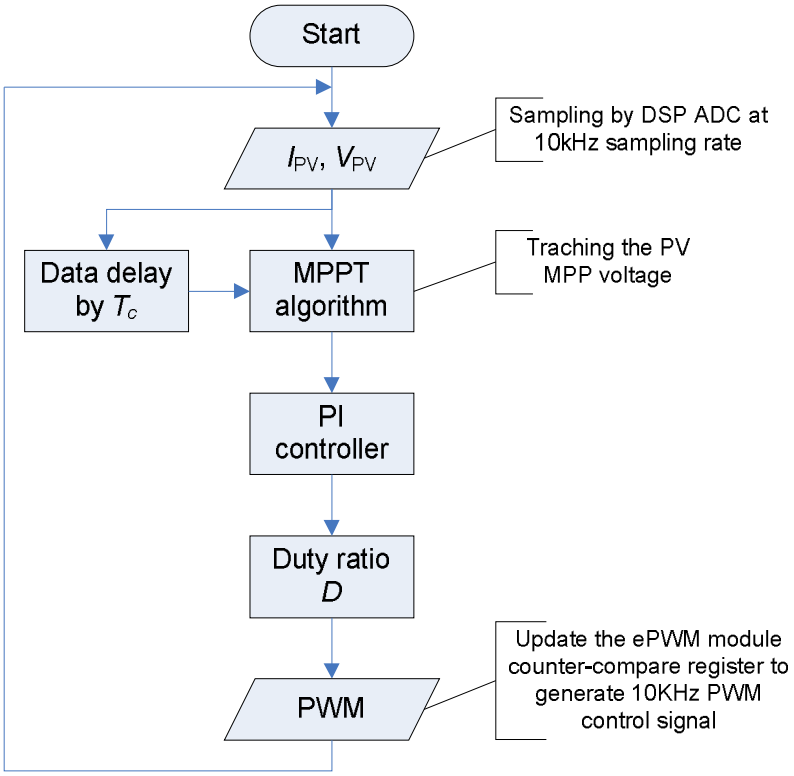


Fig.6.15: Buck converter control flowchart.

The DSP enhanced PWM (ePWM) module is a PWM channel involves two PWM output (ePWMA and ePWMB). There is a time-base submodule (ePWM event manager) related to each ePWM module. The time-base submodule can be used to set the period and frequency of the 16-bit time-base counter, and to place the time-base counter to 'count up and count down' (or vice-versa).

Also, it can be configured to place the phase control, which can be programmed to lead or lag modes with respect to the other ePWM modules. Moreover, via the time-base submodule the ePWM rise and fall edge time can be controlled, so the dead-time can be easily generated. It also can manage the synchronization of the ePWM modules time-base to operate as one system.

With respect to the generated PWM control signal to control the buck converter, the ePWM time-base counter (CTR) is configured to count up via the ePWM event manager. Every 0.1ms the counter-compare register (CMPR) is updated by the calculated duty time *D* which is expressed in percentage form and the ePWM events are generated as illustrated in Fig.6.16.

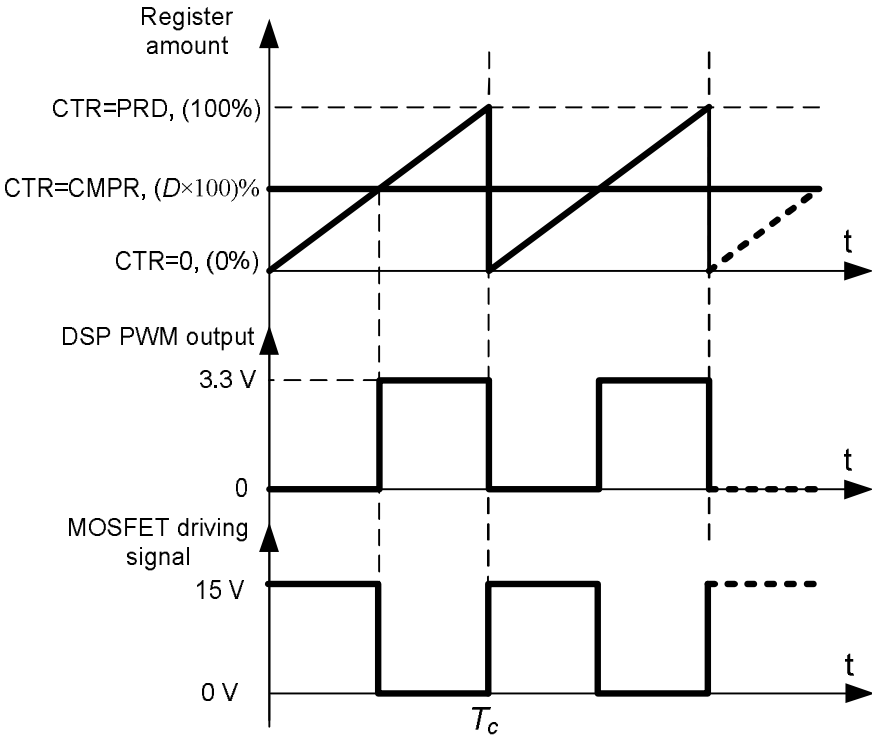


Fig.6.16: Up counting and the related PWM output.

Starting with CTR=0 the output is first reset to low (0 V), then the CTR counts up until it reaches the CMPR value (calculated via the control algorithm) at which the output PWM signal is set to high (3.3 V). After CTR exceeds the value of the period register PRD (T_c), the CTR is reset to zero and then the previous events are repeated. The set and reset events can be configured as required via the ePWM event manager and the output PWM of the DSP generates the complementary of the duty time ((1-D)×T_c), because it will be inverted by the isolating circuit.

6.6.2.2 DC-Link Inverter Control Flowchart and ePWM Event Manager

The control program of the seven-level DC-link inverter can be summarized in the basic flowchart shown in Fig.6.17.

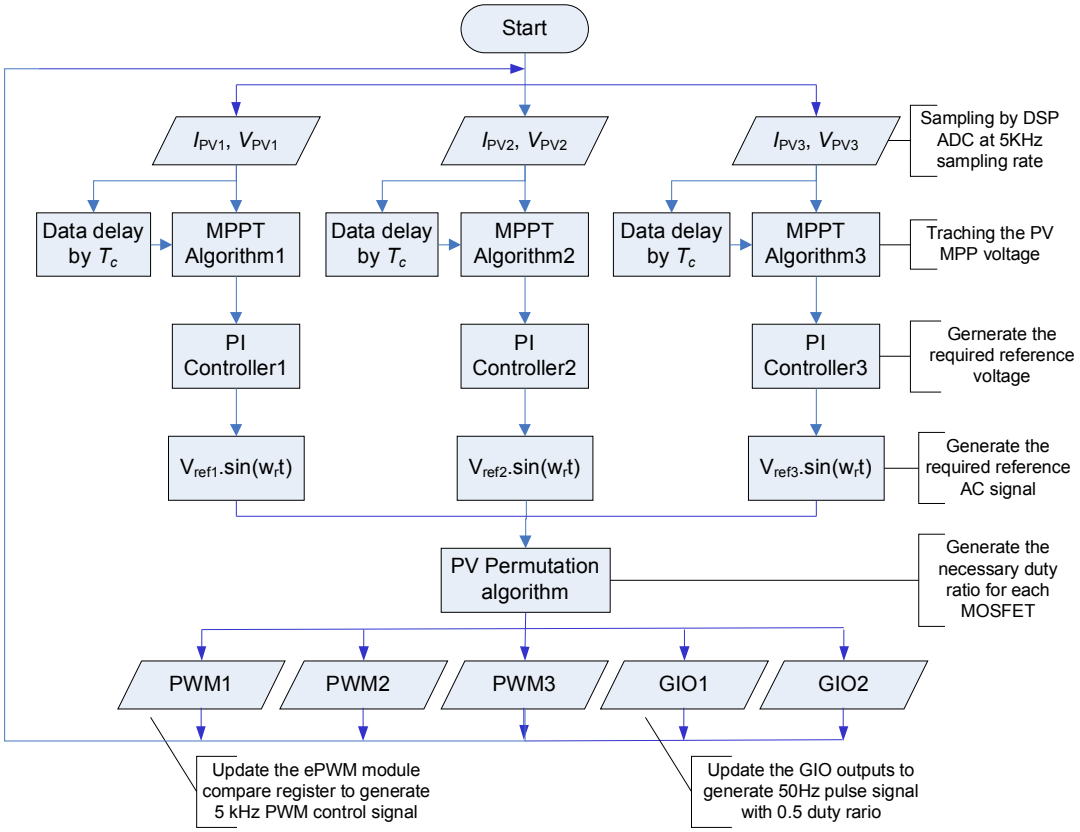


Fig.6.17: Three PV modules DC-link inverter control flowchart.

Six ADC channels are allocated to sample the current and voltage of the three used PV modules (four ADC channels in case of five-level DC-link inverter) at 5 kHz sampling rate. The achieved samples are applied to the MPPT algorithms where one algorithm is allocated for each PV module to track its MPP voltage at the applied irradiance level. For each PV module the tracked MPP voltage is compared with the actual PV voltage and the resulted error is applied to the PI controller, so the desired reference voltage is accomplished. Unity sine waves with the desired reference frequency (f_r) are multiplied with the achieved DC reference voltages in order to convert them to AC form before applying the PV permutation algorithm. The required PWM duty ratios and the instantaneous GIO states are calculated via the PV permutation algorithm, and then the counter-compare registers of the ePWM modules are updated to generate 5 kHz symmetrical PWM control signals, and the GIO outputs are updated to generate 50Hz pulse signal with 50% duty.

The GIO pins are used to control the H-bridge MOSFET switches (S1 to S4) illustrated in Figs 6.11 and 6.12 because those switches are operated at low frequency (50Hz) and fixed duty ratio of 0.5, so no need to use ePWM modules. One GIO pin is used to control S1 and S4, while another GIO pin is allocated for S2 and S3, as illustrated in Fig.6.18.

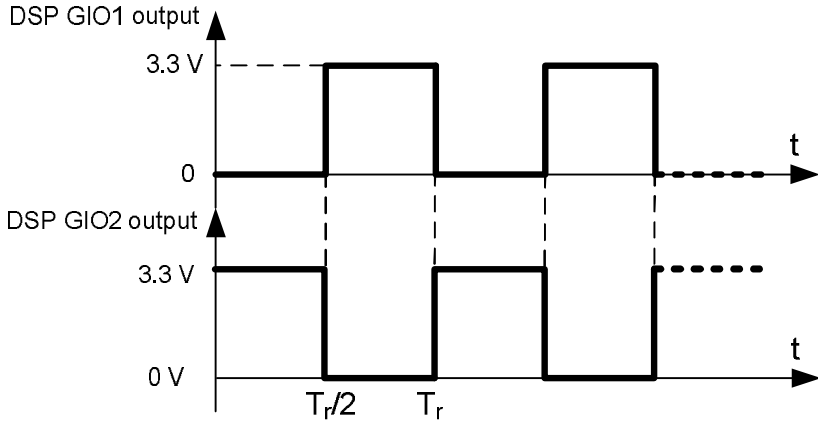


Fig.6.18: DSP GIO output signals to control S1,4 and S2,3 respectively.

The MOSFET switches Si1 to Si3, shown in Fig.6.12, are controlled by synchronized ePWM modules. Through the ePWM event manager, the ePWM time-base counter (CTR) is configured to count up and down. The required ePWM events are generated as illustrated in Fig.6.19.

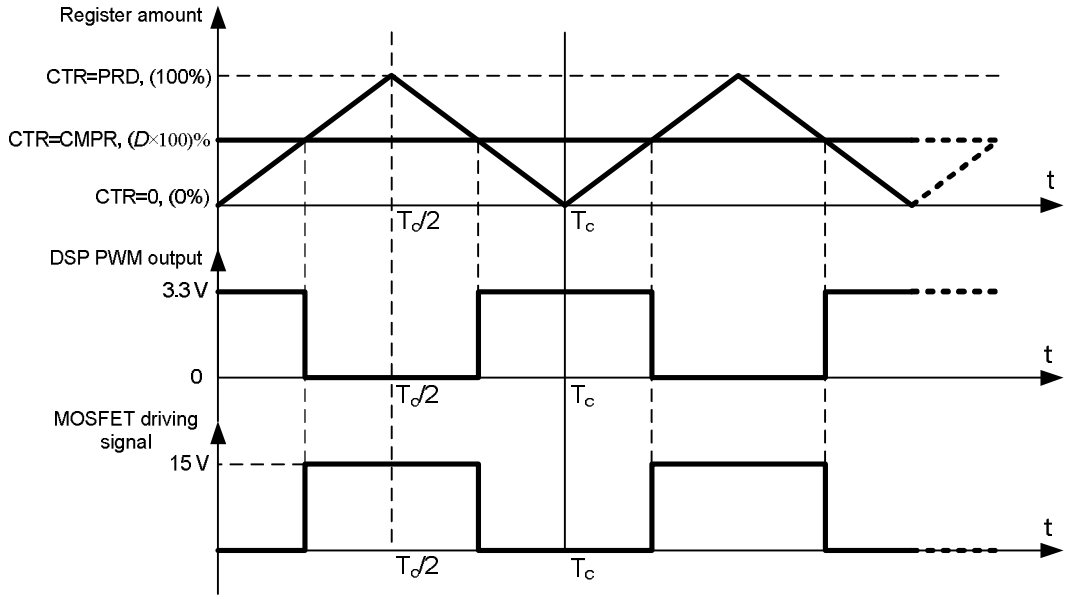


Fig.6.19: Up and down counting and the related PWM output.

The reason for using the count up and down mode is to generate symmetrical PWM over T_c period, and so the CTR period has to be the half of the required PWM switching time (T_c/2) and the total counting up and down time is T_c.

In the counting up stage, starting with CTR=0 the output is set first to high (3.3V), then the CTR counts up until reaches the CMPR value (calculated via the control algorithm) where the output PWM signal is set to low (0 V). After CTR exceeds the value of the period register PRD (T_c/2), the counting down stage is started while the ePWM output is in no change state. When the CTR reaches the CMPR value, the output PWM signal is set to high and then the previous events are repeated.

6.6.2.3 Simulink Target Support Package and Real-Time Workshop

Through the Target Support Package™ software which can be added to Matlab Simulink as a tool box, the implemented Simulink model can be executed on a Texas Instruments DSP. That also requires help of the Real-Time Workshop technology which converts the implemented Simulink models as well as the Embedded MATLAB language subset to C language source code without any need to program in the C language.

By the Target Support Package™ software, the Embedded IDE Link™ software is applied in order to start the compiling and linking the created C language source code inside the CCS, and then it is loaded to the target so it can be executed independently on the target. Fig.6.20 shows the implemented Simulink model by using blocks of the Target Support Package to control the buck converter in the real-time mode [91].

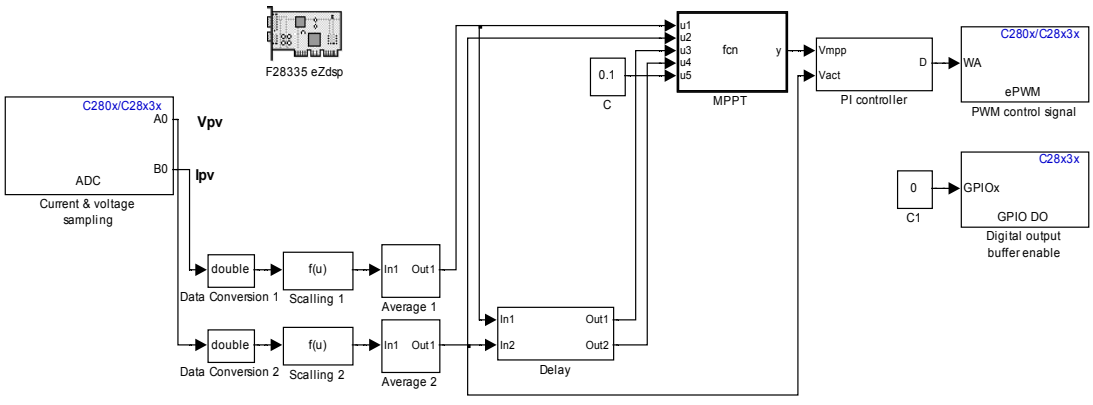


Fig.6.20: Buck converter control by using Simulink Target Support Package.

6.6.2.4 Simulink Real-Time Data Exchange and Graphical User Interface

Real-Time Data Exchange (RTDX) feature is offered by the Target Support Package™ software. RTDX enables sending and receiving data between the target (DSP) and the host (PC) via the USB port in the real-time mode of operation.

The Simulink RTDX involves input and output channels which can be used in the designed Simulink model, RTDX-input channel ("From RTDX" Simulink block) to send data from the host to the target such as manipulating parameters while the target is operating, and the RTDX-output channel ("To RTDX" Simulink block) to receive data from the target to the host so it can be displayed in graphs or for monitoring purpose in the real-time running operation. Fig.6.21 illustrates the implemented Simulink model, where the Target Support Package including the RTDX is employed to control the five-level DC-link inverter in real-time mode of operation. A similar Simulink model for seven-level DC-link inverter is illustrated in Fig.6.22.

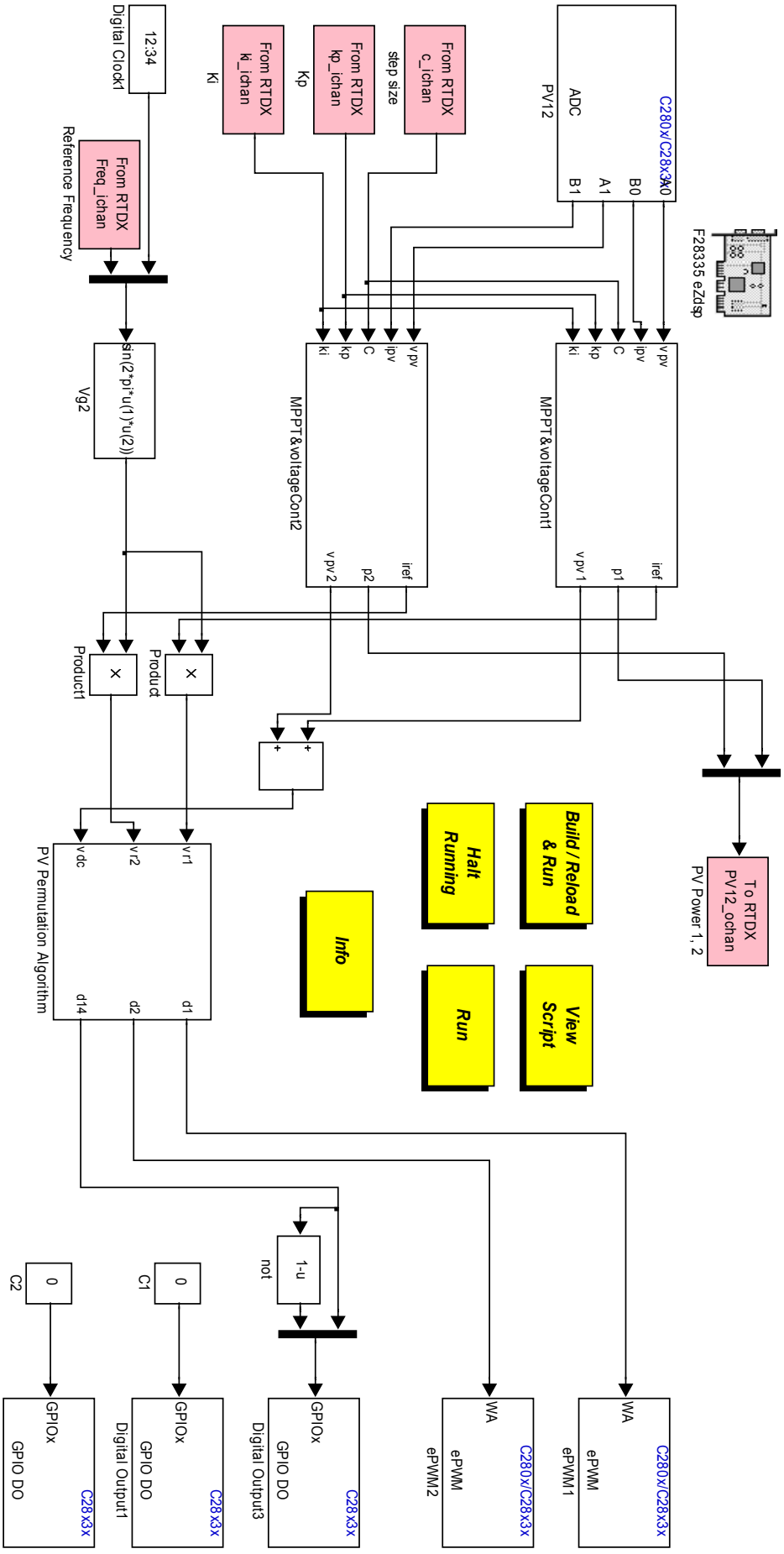


Fig.6.21: Five-level DC-link inverter control by using Simulink Target Support Package with RTDX input and output channels.

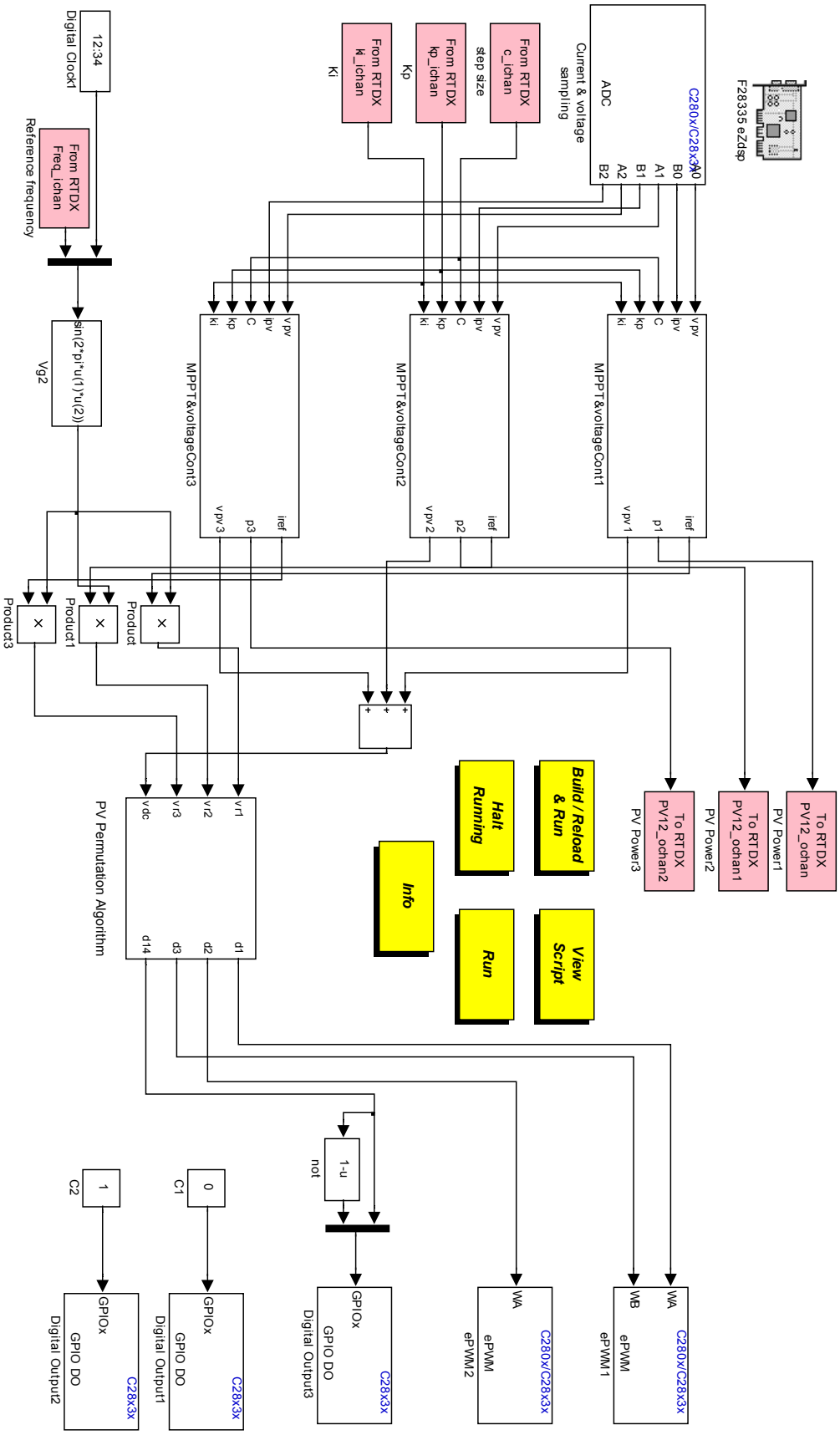


Fig.6.22: Seven-level DC-link inverter control by using Simulink Target Support Package with RTDX input and output channels.

A user interface window can be designed via the Matlab Graphical User Interface (GUI). The GUI window manages sending and receiving the data through the RTDX channels. The user can design the suitable interface window according to the application requirements, so the user can place the system parameters values or manipulate them, and also the DSP feedback information, which is coming via the RTDX-output channels, can be displayed on the same window.

Fig.6.23 illustrates the Matlab GUIDE which is used to design the required GUI window. The implemented window is related to the control model shown in Fig.6.22. There are three axes (axes1, axes2, and axes3) related to the RTDX-output channels shown in Fig.6.22. Each individual axes is allocated to display the power extracted from a single PV module in percentage of the maximum power under full irradiance (1000 W/m^2). With respect to the RTDX-input channels, there are six related interface elements shown in Fig.6.23 (five of them are edit boxes and one is a check box). Similarly, in Fig.6.22 there are six RTDX-input channels; four of them are shown and two are inside the block 'PV Permutation Algorithm'. Through the implemented GUI window, the user can control the inverter output frequency, the PI constants, the step size of MPPT algorithm and the inverter input DC voltage which is used in the direct PWM calculations (by ticking the check box, the measured DC value can be applied). There are also two bottoms shown 'Apply' and 'Halt Demo', the former to apply the entered parameters values and the latter to stop the run of the program on the target.

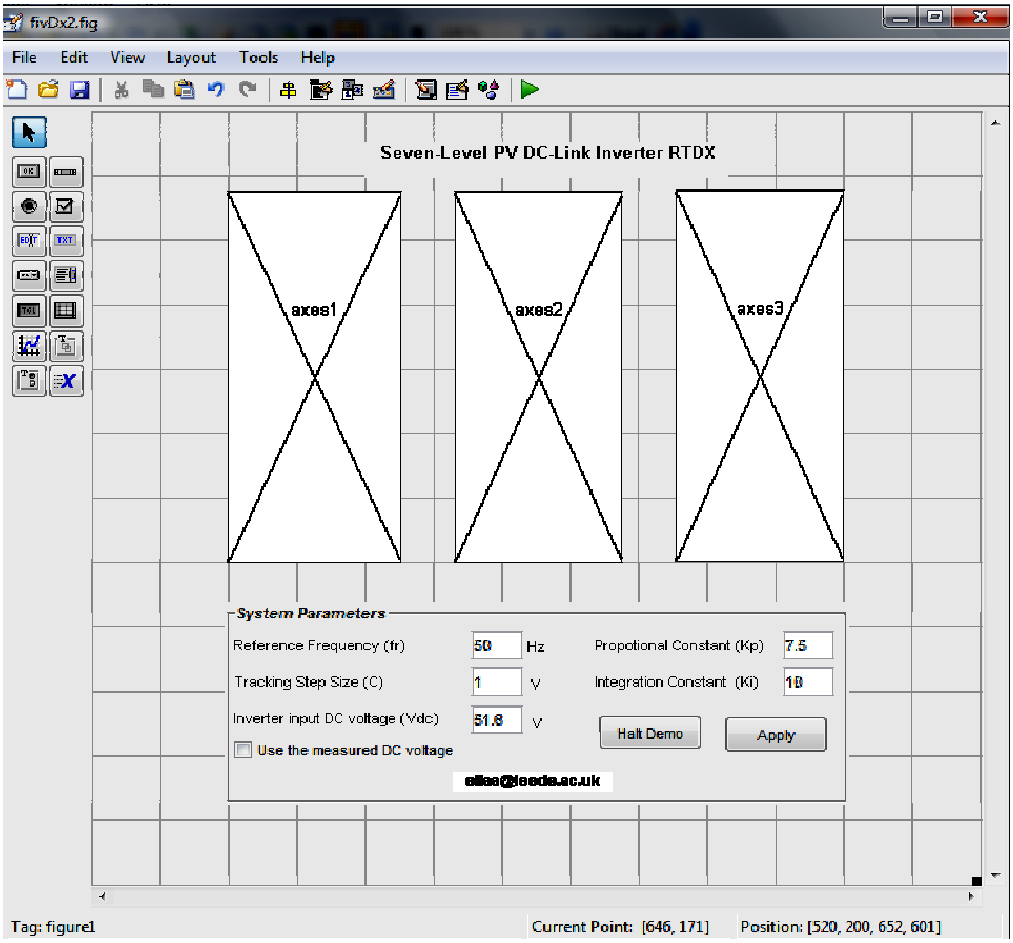


Fig.6.23: Matlab GUIDE and the interface elements used to design the GUI window for the seven-level DC-link inverter.

6.7 Summary

This chapter has presented the design and implementation of the experimental setup for the support of theoretical studies. The system components, control flowcharts and the software used to program the DSP have been described.

The halogen bulbs were chosen as lighting source because of their relatively low light intensity ripple at 50 Hz single phase main supply and the fact that they can be controlled easily. Also, small PV modules of 10 W were used, so providing the required lighting, which is necessary to reach the maximum power generated by the PV source, can be accomplished indoors.

For the testing purposes a MOSFET based variable resistance circuit was implemented for load emulation in order to measure the PV module I-V curve easily under different irradiance levels. The DC-DC buck converter circuit was

implemented and the MPPT algorithm was tested in the real-time closed-loop system. The five-level and seven-level DC-link inverter circuits were implemented along with their closed-loop control for overcoming the PV partial shading problem.

An eZdsp^{TM} F28335 development kit was employed to control the converter and the inverter circuits. The Matlab Simulink software was used to program the DSP unit in the real-time mode of operation. The Real Time Data Exchange (RTDX) feature, available from Texas Instruments, was applied. A graphical user interface window was designed in order to enable the user to access the system parameters and to modify them and to monitor the extracted power of each PV module under real-time mode of operation.

Chapter 7

Experimental Results

This chapter illustrates the results which are accomplished by the experimental setup described in the previous chapter. For selecting the light source, some current waveforms which are generated by the light of halogen and high pressure sodium (HPS) bulbs are presented. The achieved I-V characteristics of the used PV module are presented. The MPPT results, generated via the DC-DC buck converter, are shown for P&O and VH-P&O. The accomplished results produced via the IPWM algorithm are presented for five-level DC-link inverter. For the partial shading experiments, the achieved current and voltage results for five and seven level DC-link inverters are presented along with the THD and the extracted and delivered power measurements. The required measures of the room and PV surface temperatures are shown, where the PV surface temperatures are measured by using an IR thermometer.

7.1 Light Sources Test

The test of the light source is necessary in order to evaluate the effectiveness of using lighting sources which are powered by AC supply. The short circuit current of the PV module is used as a qualitative indicator in comparing the light effects of the halogen and the HPS bulbs. Fig.7.1 shows the waveform of the short-circuit current of the PV module (SSP-10W) achieved when applying a 400 W HPS light source. The distance between the light source and the PV module is 22cm and the room temperature is 20°C. The DC current generated by PV module under the solar radiation is rippleless. However, in laboratory testes when the light source is emulated by electric bulbs supplied from 50 Hz main supply, the generated current waveform contains a 100 Hz ripple. As a result of the HPS spectrum, the short-

circuit current reached about 75% (510 mA) of the short-circuit current at 1000W/m^2 (690 mA) by using a 400 W HPS bulb. However, the amplitude of current ripple is large. The average generated current is 275 mA, and the peak-to-peak ripple has nearly the double value of the average current. In order to avoid the light flickering and to generate a smooth DC current from the PV module, it might seem appropriate to power the HPS bulb via a DC source. However, HPS bulb is not intended to be powered from DC supply due to overheating of which the degradation of the light [92].

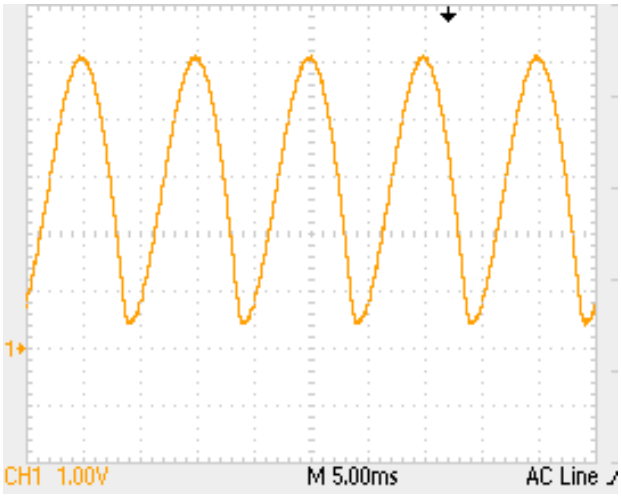


Fig.7.1: Short-circuit current of the PV module exposed to 400 W HPS bulb, module surface temperature of 30°C (100 mA/div).

At the same experiment conditions, the PV module was exposed to irradiation which is generated from 400 W halogen bulb. Even though, the short-circuit current waveform of the PV module exposed to the halogen bulb (Fig.7.2) shows much lower ripple amplitude compared with the HPS, almost 35% (240 mA) of the PV module maximum short-circuit current is achieved compared with 75% by using the HPS lighting bulb. The average generated current is 225 mA, and the peak-to-peak ripple is about 30 mA.

Halogen bulb has lower flickering than the HPS bulb, because its generated irradiation is based on the heating of the filament inside the tube, where the variation of the temperature due to 50 Hz supply frequency is low [93].

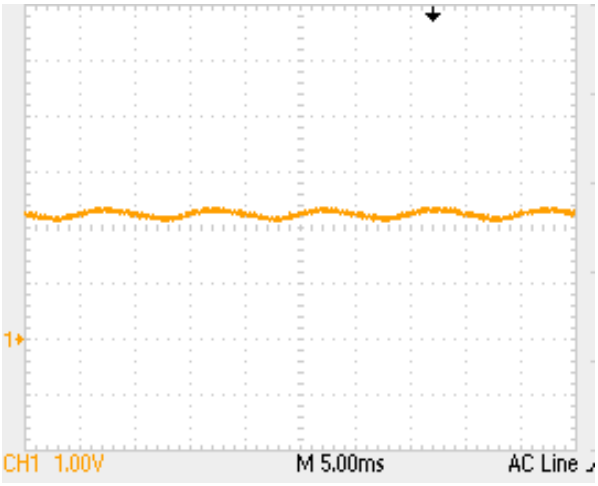


Fig.7.2: Short-circuit current of the PV module exposed to 400 W halogen bulbs, module surface temperature of 34°C (100 mA/div).

The output ripple caused by 50 Hz supply frequency can be significantly decreased by exposing the PV module to a three-phase halogen light source using three halogen bulbs each powered from a different phase. The short-circuit current generated from the PV module under this light source condition is shown in Fig.7.3. The average current is about 240 mA and the peak-to-peak ripple is less than 5 mA. This light source arrangement is therefore used in the experimental work.

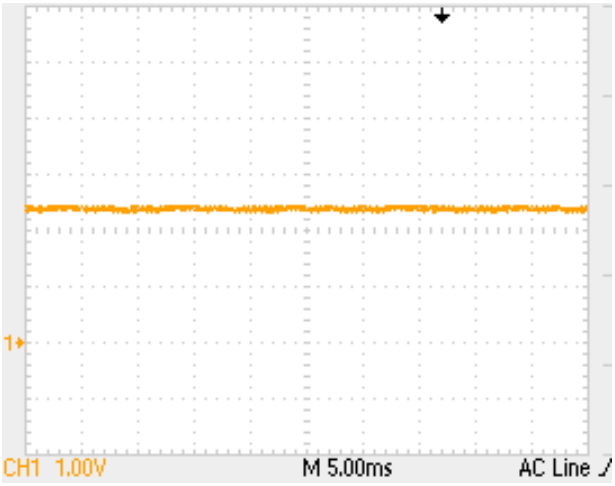


Fig.7.3: Short-circuit current of the PV module exposed to 400 W three-phase halogen bulb, module surface temperature of 34°C (100 mA/div).

7.2 PV Module Test

The PV module (SSP-10W) used in the experimental work was tested in order to achieve the I-V characteristics as well as confirming the specifications listed in the Table.6.1. The circuit shown in Fig.6.5 is used to display the I-V curve of the PV

module, Fig.7.4 shows the waveforms of the MOSFET gate control signal, the PV module current and voltage.

The experiment was carried out at room and surface temperatures of 21°C and 38°C respectively. The measured I-V characteristics of the PV source are shown in Fig.7.5 for different irradiance levels. The predicted I-V curves generated via a Bishop model is presented in the same figure as well.

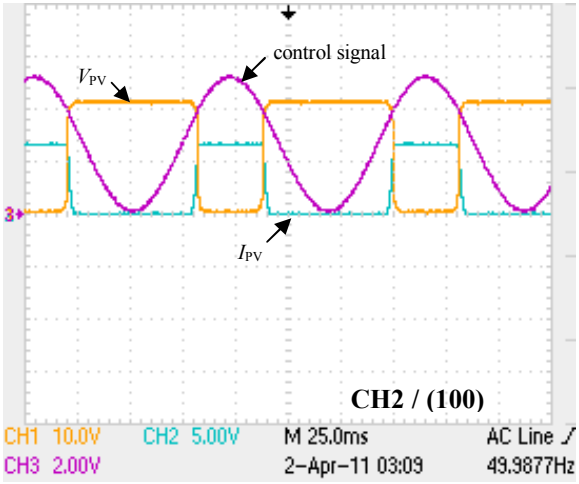


Fig.7.4: MOSFET gate control signal of the I-V display circuit, and the related PV module current and voltage waveforms (I_{PV}, V_{PV}).

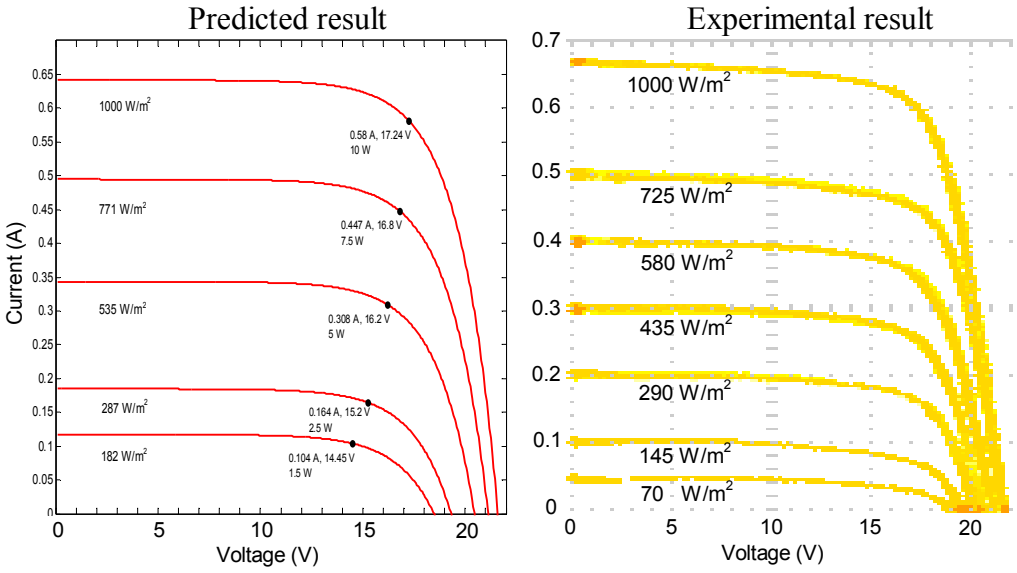


Fig.7.5: I-V characteristic of SSP-10W PV module at different irradiances.

7.3 Buck converter MPPT Results

The DC-DC buck converter circuit shown in Fig.6.6 is used to test the closed-loop system implemented via the DSP including the P&O MPPT algorithm. It is also used to improve the tracking algorithm where VH-P&O MPPT is achieved. Texas Instruments eZdsp^{TM} F28335 development system is employed successfully to implement the closed-loop MPPT of the DC-DC buck converter. The applied system parameters are listed in Table 7.1.

With respect to applying P&O tracking algorithm, Fig.7.6 shows the PV voltage, current and extracted power waveforms as result of the change of the applied irradiance in the range from 175 to 1000 W/m^2 and back, at the PV surface and room temperatures of 25°C and 40°C respectively. As it was mentioned previously, in order to protect the DSP unit, the PV voltage and current signals are scaled not to exceed 3 V. As result the CH1, CH2 and MATH channels have to be rescaled by factors of 21.6/3, 0.690/3 and 1.656 respectively.

TABLE 7.1: Buck Converter System Parameters

Quantity	Value
PI proportional constant, K_P	2
PI integral constant, K_i	4
MPPT algorithm step size, C	0.025 V
ADC sampling frequency	10 kHz
PWM switching frequency	10 kHz

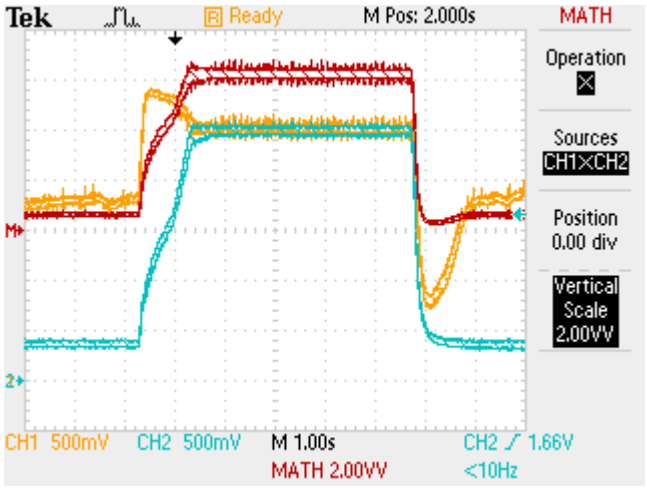


Fig.7.6: CH1 (PV voltage), CH2 (PV current), MATH (PV power) for P&O MPPT under [CH1× (21.6/3), CH2× (0.690/3), and MATH× (1.656)]. PV surface and room temperatures of 25°C and 40°C.

The waveforms in Fig.7.6 show that, at the applied irradiance of 175 W/m^2, the PV module is operated at its MPP of about 1 W (0.3×2×1.656). After applying 1000 W/m^2 irradiance, the PV module reaches the maximum power of 10 W (3×2×1.656). Subsequently, the PV module is shaded again to the initial irradiance level of 175 W/m^2 and consequently, the P&O MPPT algorithm tracked successfully the new MPP of 1 W at that irradiance level.

The improved P&O MPPT algorithm which is called VH-P&O, is applied to the same PV system in a real-time mode of operation and under the same system parameters and operating conditions. As it can be seen in Fig.7.7, the VH-P&O algorithm reached the MPP faster (about three times faster) than the conventional P&O algorithm, and the deviations from the MPP at the transition times are much lower. Also, the achieved power waveform is much smother when the VH-P&O algorithm is used.

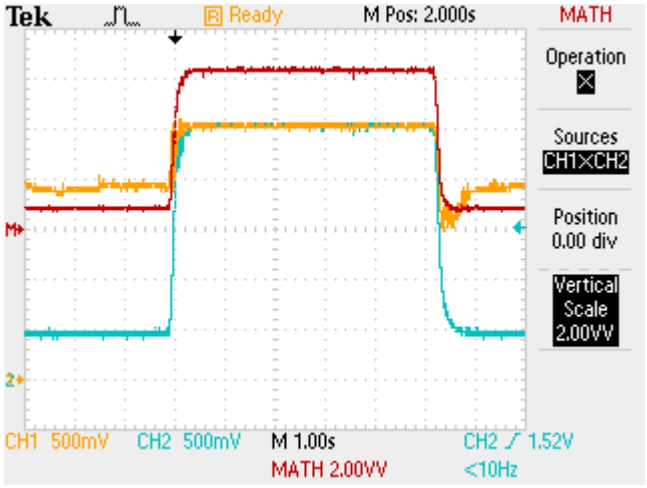


Fig.7.7: CH1 (PV voltage), CH2 (PV current), MATH (PV power) for VH-P&O MPPT under [CH1×(21.6/3), CH2×(0.690/3), and MATH×(1.656)].

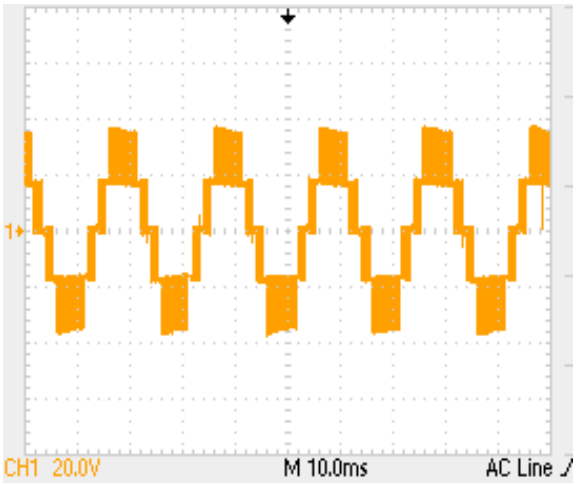
7.4 IPWM Applied for Five-Level DC-Link Inverter

The generalized IPWM algorithm introduced in Fig.3.13 is applied experimentally to control two PV sources DC-link inverter, which is shown in Fig.6.11, in order to generate five-level voltage waveform. The applied system parameters are listed in Table 7.2 and the resulted voltage waveform and the related spectra are shown in Fig.7.8a and Fig.7.8b respectively for resistive load.

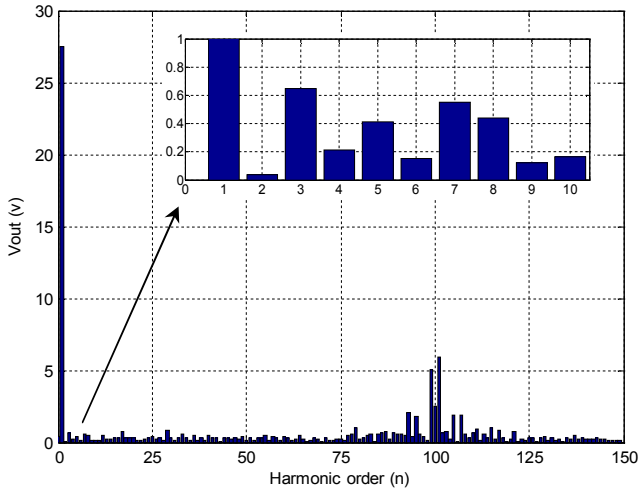
TABLE 7.2: Five-Level Inverter System Parameters (IPWM)

Quantity	Value
PI proportional constant, K_P	2
PI integral constant, K_i	4.5
MPPT algorithm step size, C	0.2 V
Frequency modulation index, M_f	100
Reference frequency, f_r	50 Hz
ADC sampling frequency	5 kHz
PWM switching frequency, f_c	5 kHz

Identical irradiances of 1000 W/m^2 were applied for both of the PV modules, and the resulted amplitude modulation index (M_a) is 0.8 at resistive load of 21 Ω. All the results were taken at room temperature of 22°C and PV surface temperature of 35°C.



(a)



(b)

Fig.7.8: Resistive load: (a) 5-level voltage waveform and (b) voltage spectra obtained by applying IPWM algorithm.

The PV modules are operated at their MPP, and the voltage spectra illustrated in Fig.7.8b shows that all the large amplitude unwanted harmonics are moved towards

the switching frequency. The output voltage THD is 36.5% and the DF is 0.28% (the THD and the DF are calculated for the first 150 harmonics). In grid-connected applications, the low order harmonics have to be each below 1% to comply with the grid-connected code IEEE 519.

As it can be seen, the fundamental amplitude is 27.5 V which is equivalent to $M_a \times V_{dc}$= 0.8×34.4 V (where V_{dc} = 2×17.2 V). Fig.7.9 shows the output voltage and current waveforms for R-L load (R_L=21 Ω, L=2 mH) under the aforementioned conditions.

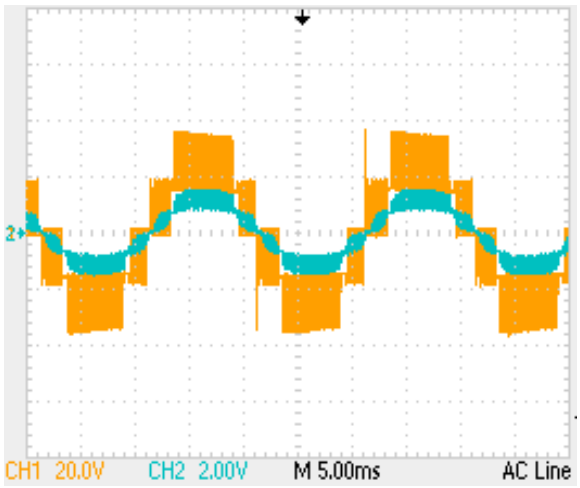
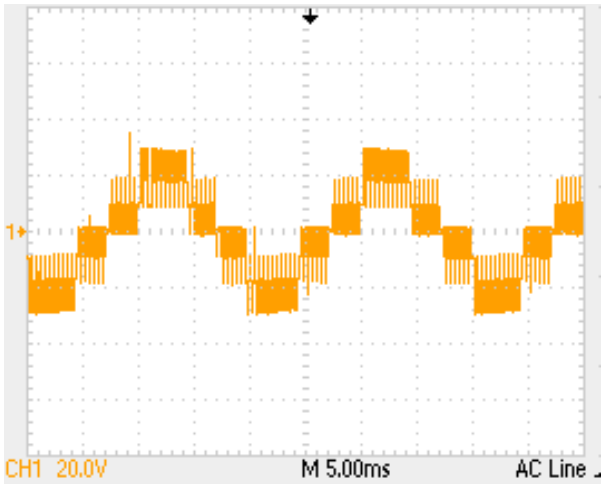


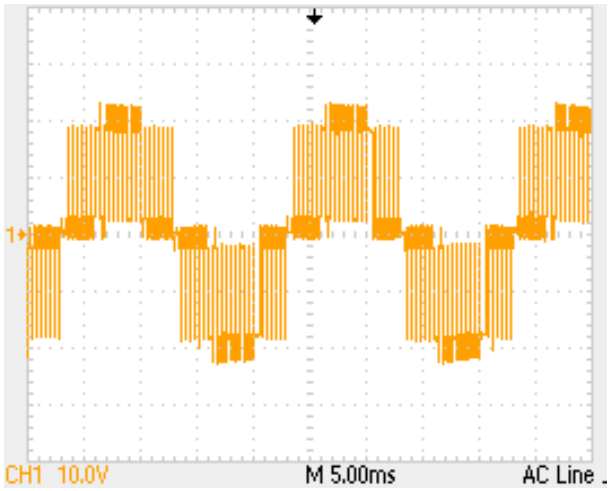
Fig.7.9: R-L load output voltage (CH1) and current (CH2) waveforms obtained by applying IPWM algorithm.

The system was also tested under shading conditions (different irradiance levels (G_{pv1}, G_{pv2}) applied on the PV modules), where Fig.7.10.a is achieved at G_{pv1}=1000W/m^2 and G_{pv2}=500 W/m^2, and Fig.7.10.b is achieved at G_{pv1}=1000 W/m^2 and G_{pv2}=250 W/m^2. The waveforms are obtained by using a resistor load of 17.5 Ω.

The system control does not take into account the PV shading condition, so the PV modules do not operate at their MPPs and that can be noticed in Fig.7.10 where there is a large voltage difference between V_{pv1} and V_{pv2} (5 V and 18 V in Fig.7.10a and Fig.7.10b respectively). For each switching period, the PV modules are utilized alternatively in order to achieve equal PV loading and symmetrical output AC waveform especially under shaded conditions. The results obtained under partial shading with control which enables the system PV modules to be operated at their MPPs and also to deliver the total extracted power to the load, are considered in the next sections.



(a)



(b)

Fig.7.10: Resistive load output voltage waveform at irradiances of (a) G_{pv1}=1000 W/m^2, G_{pv2}=500 W/m^2 and (b) G_{pv1}=1000 W/m^2, G_{pv2}=250 W/m^2 obtained by applying IPWM algorithm

7.5 PV Permutation Algorithm for Five-Level DC-Link Inverter

The PV permutation algorithm is introduced in section 5.2 in order to deal with the PV partial shading problem. The algorithm is applied to the five-level DC-link inverter shown in Fig.6.11, where the system PV modules are partially shaded to varies levels of irradiances so the validity of the algorithm can be confirmed. The inverter control is implemented in real-time, and Matlab-Simulink RTDX with GUI shown in Fig.6.21 is employed. The applied parameters are listed in Table 7.3.

TABLE 7.3: Five-Level Inverter System Parameters (PV Permutation Algorithm)

Quantity	Value
PI proportional constant, K_P	1.6
PI integral constant, K_i	2.0
MPPT algorithm step size, C	0.2 V
Frequency modulation index, M_f	100
Reference frequency, f_r	50 Hz
ADC sampling frequency	5 kHz
PWM switching frequency, f_c	5 kHz

The PV modules are first exposed to a symmetrical irradiance of 1000 W/m^2. Fig.7.11 shows the output voltage waveform obtained at 20 Ω resistive load at room and PV surface temperatures of 20°C and 48°C respectively.

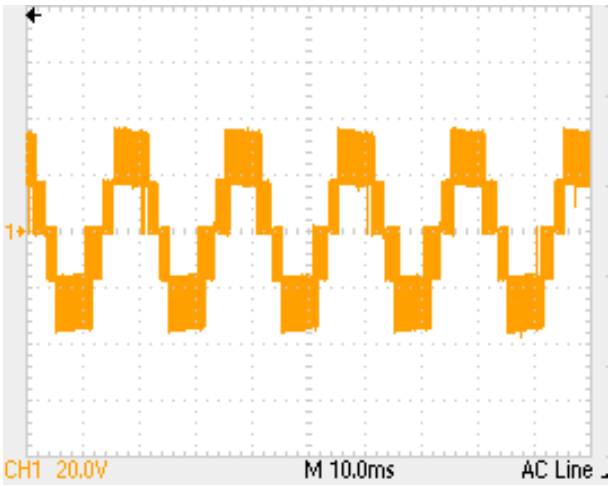


Fig.7.11: Five-level output voltage waveform at full irradiances of 1000 W/m^2 obtained by applying PV permutation algorithm.

The PV1 and PV2 current and voltage waveforms, which are taken before the DSP ADC stage, are shown in Fig.7.12. Both of the PV modules are operated at the same MPP. Also, there is 100 Hz oscillation which can be seen in the current and voltage waveforms alike. The 100 Hz oscillation is a consequence of producing 50 Hz AC waveform at the inverter output. This can be further reduced by increasing the bypass capacitance across each PV module. The graphical user interface (GUI) window in Fig.7.13 shows the generated PV power and the real-time controllable system parameters.

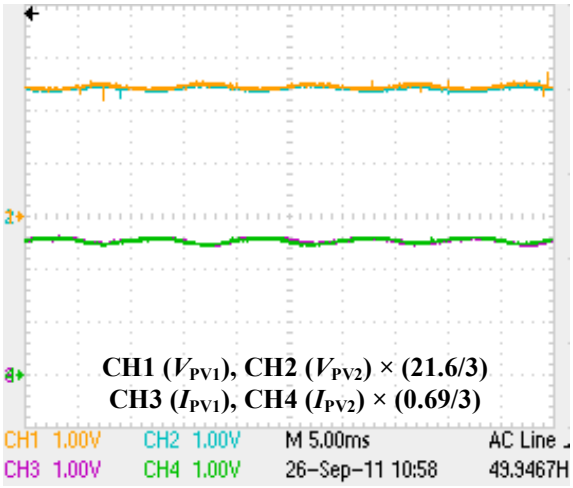


Fig.7.12: PV modules current and voltage waveforms at G_{pv1}, G_{pv2}=1000 W/m^2 using PV permutation algorithm for two PV sources DC-link inverter.

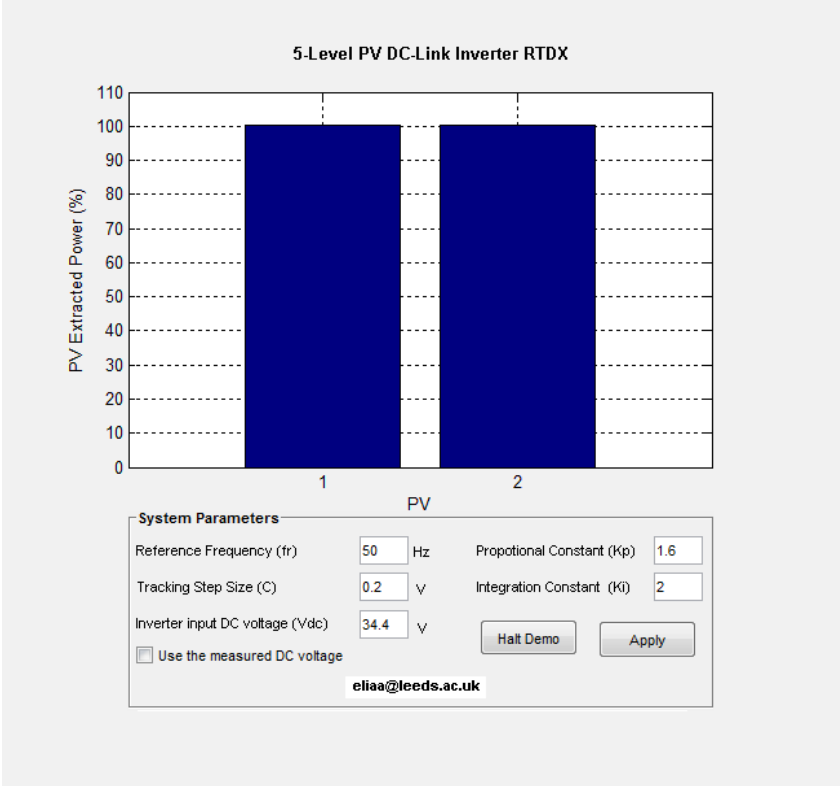


Fig.7.13: RTDX GUI window for two PV sources DC-link inverter at full irradiance of 1000 W/m^2 achieved by PV permutation algorithm.

The output voltage waveform for unsymmetrical irradiance is shown in Fig.7.14, the applied irradiances for the PV modules are G_{pv1}=1000 W/m^2 and G_{pv2}=700 W/m^2. The surface temperatures of the PV1 and PV2 modules are 48°C and 43°C.

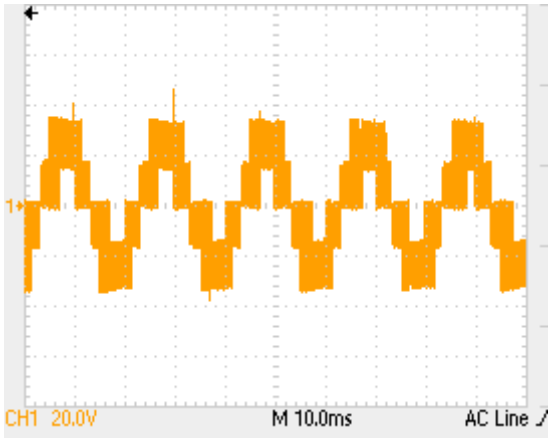


Fig.7.14: Five-level output voltage waveform at G_{pv1}=1000 W/m^2, G_{pv2}=700 W/m^2 using PV permutation algorithm.

Fig.7.15 shows the associated current and voltage waveforms of the PV modules, it is clear that the PV module voltages are almost at the same level of about 17.28V (2.4×21.6/3), while the current of PV1 is about 575 mA (2.5×0.69/3) and the current of the shaded PV module is dropped to about 414 mA (1.8×0.69/3). The same results are obtained when the irradiance levels are swapped (G_{pv1}=700 W/m^2, G_{pv2}=1000 W/m^2).

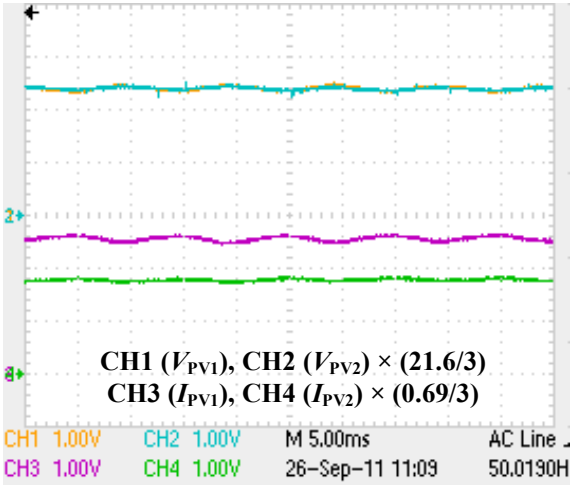
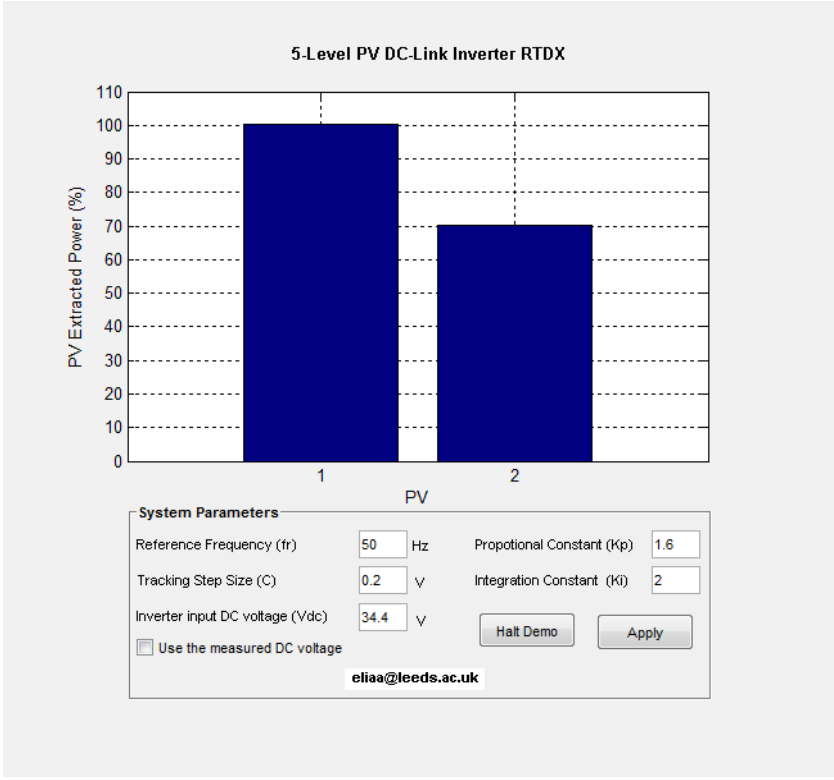
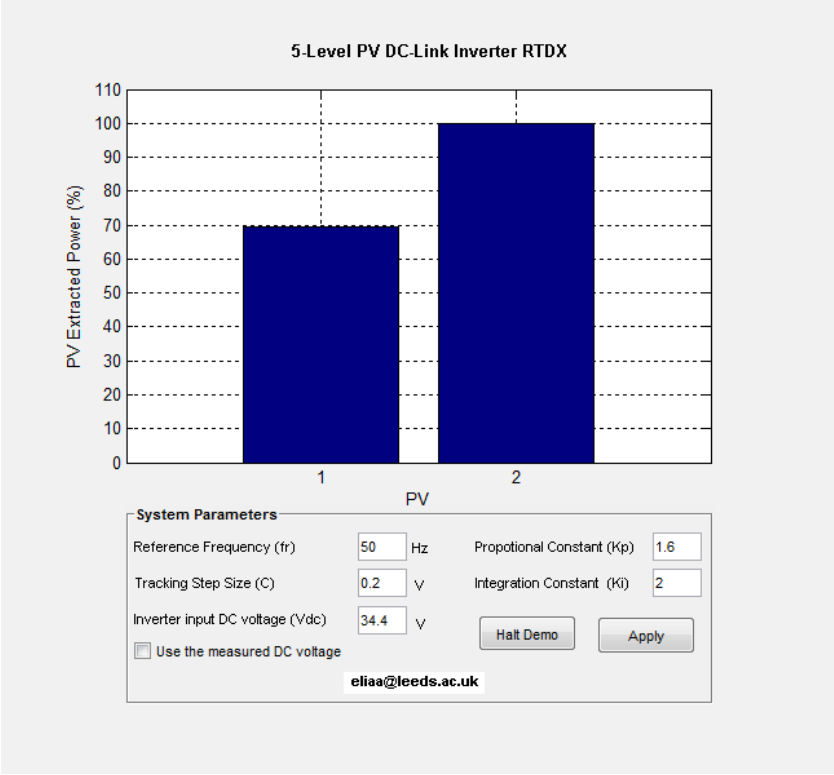


Fig.7.15: PV current and voltage waveforms at G_{pv1}=1000 W/m^2, G_{pv2}=700 W/m^2 using PV permutation algorithm for two PV sources DC-link inverter.

Fig.7.16a and Fig.7.16b show the GUI windows taken in real-time mode of operation, representing the percentage of the generated power.



(a)



(b)

Fig.7.16: RTDX GUI window for two PV sources DC-link inverter controlled by PV permutation algorithm at (a) G_{pv1}=1000 W/m^2, G_{pv2}=700 W/m^2 and (b) G_{PV1}=700 W/m^2, G_{PV2}=1000 W/m^2.

To verify the validity of the system regarding its operation under the PV partial shading, a reduced irradiance of 500 W/m^2 is applied on PV2 while PV1 is in full irradiance. The temperature of PV2 is dropped to 38°C. Fig.7.17 shows the output voltage waveform.

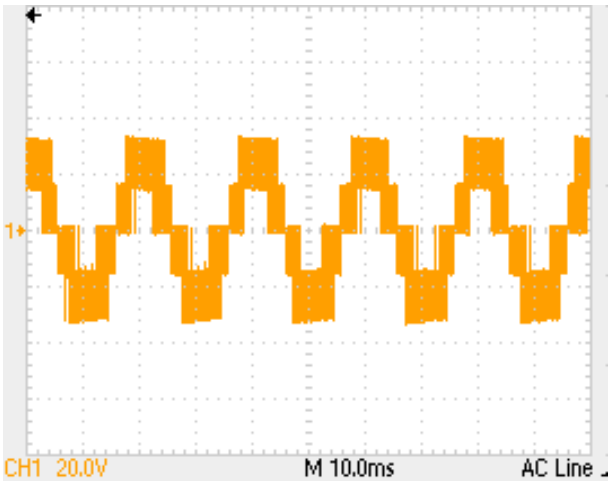


Fig.7.17: Five-level output voltage waveform at G_{pv1}=1000 W/m^2, G_{pv2}=500 W/m^2 achieved by PV permutation algorithm.

The current and voltage waveforms of the PV modules are shown in Fig.7.18 under the above levels of irradiance. The voltage and current values are the same as in the previous case, except for the current of PV2 module, I_{PV2}=288 mA (1.25×0.69/3).

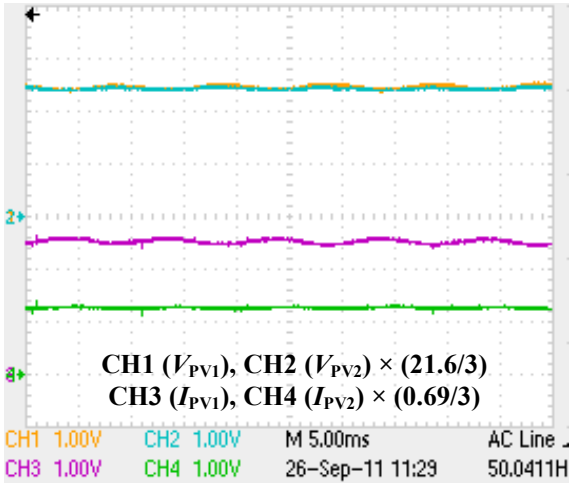
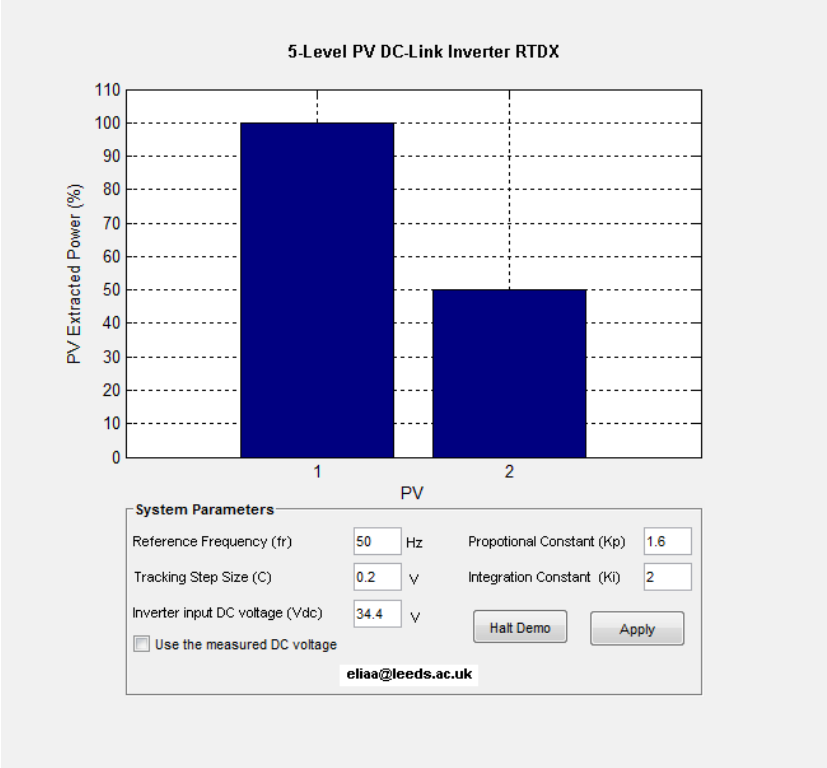
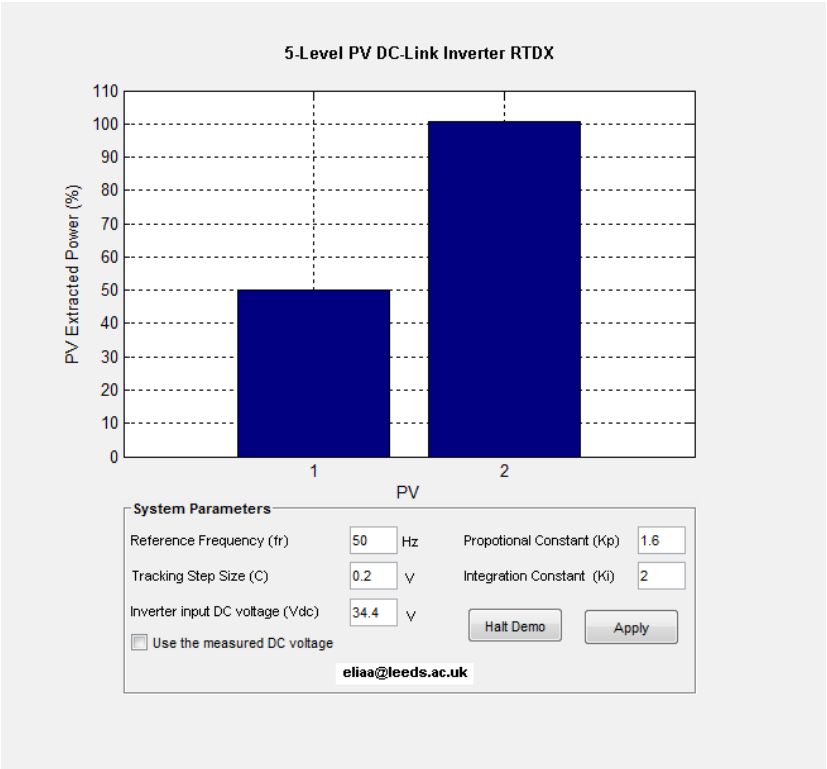


Fig.7.18: PV current and voltage waveforms at G_{pv1}=1000 W/m^2, G_{pv2}=500 W/m^2 using PV permutation algorithm for two PV sources DC-link inverter.

Fig.7.19a and Fig.7.19b show the extracted power of the PV modules, depicted in GUI windows. The measurements are taken at irradiances of 1000 W/m^2 and 500 W/m^2.



(a)



(b)

Fig.7.19: RTDX GUI window for two PV sources DC-link inverter controlled by PV permutation algorithm at (a) G_{pv1}=1000 W/m^2, G_{pv2}=500 W/m^2 and (b) G_{PV1}=500 W/m^2, G_{PV2}=1000 W/m^2.

A further test of the PV permutation algorithm is made when PV2 is exposed to irradiance level of 250 W/m^2 while PV1 is at the same level of irradiance (1000 W/m^2). Fig.7.20 shows the output voltage waveform which is achieved at room temperature of 20°C and PV surface temperatures of 48°C and 31°C for PV1 and PV2 respectively.

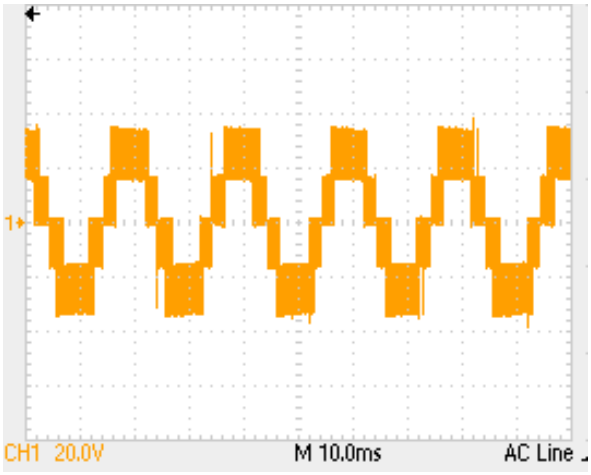


Fig.7.20: Five-level output voltage waveform at G_{pv1}=1000 W/m^2, G_{pv2}=250 W/m^2, achieved by PV permutation algorithm.

Fig.7.21 shows the related current and voltage waveforms of the PV1 and PV2 modules. V_{PV1} and V_{PV2} are almost at the same value of 17.28 V, and I_{PV1} and I_{PV2} are at about 575 mA and 138 mA respectively.

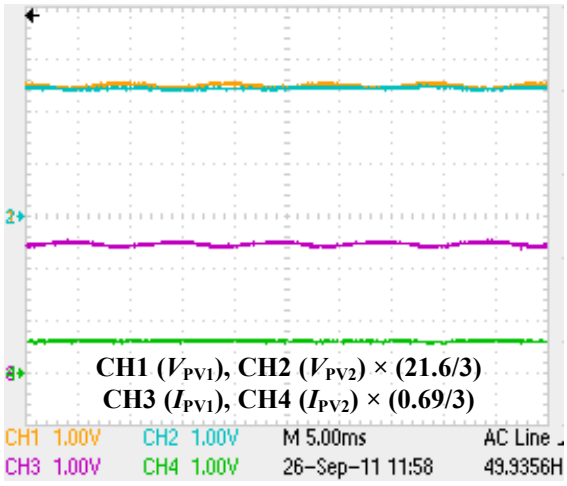
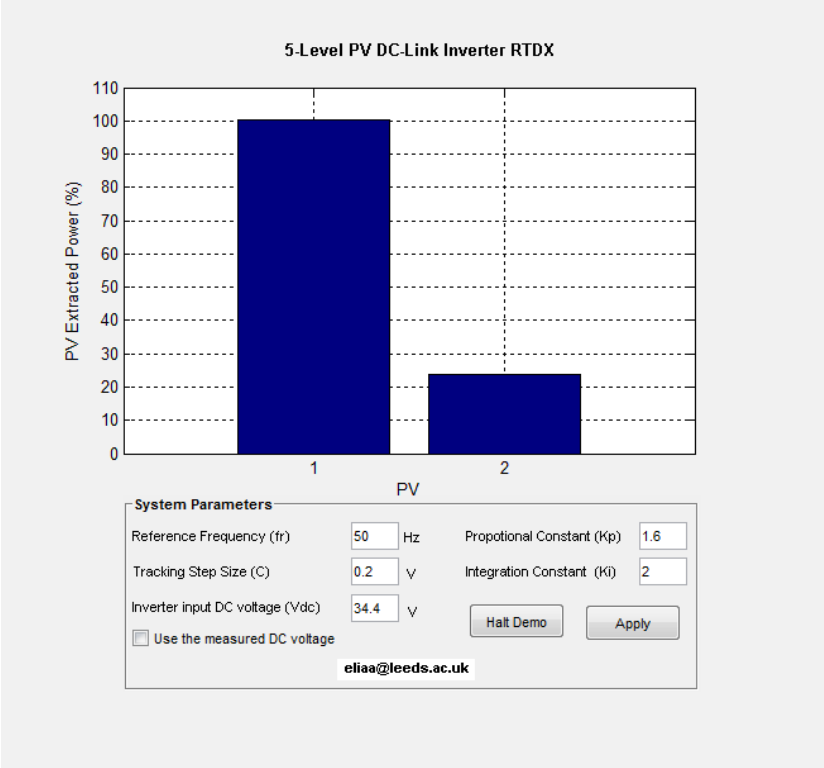
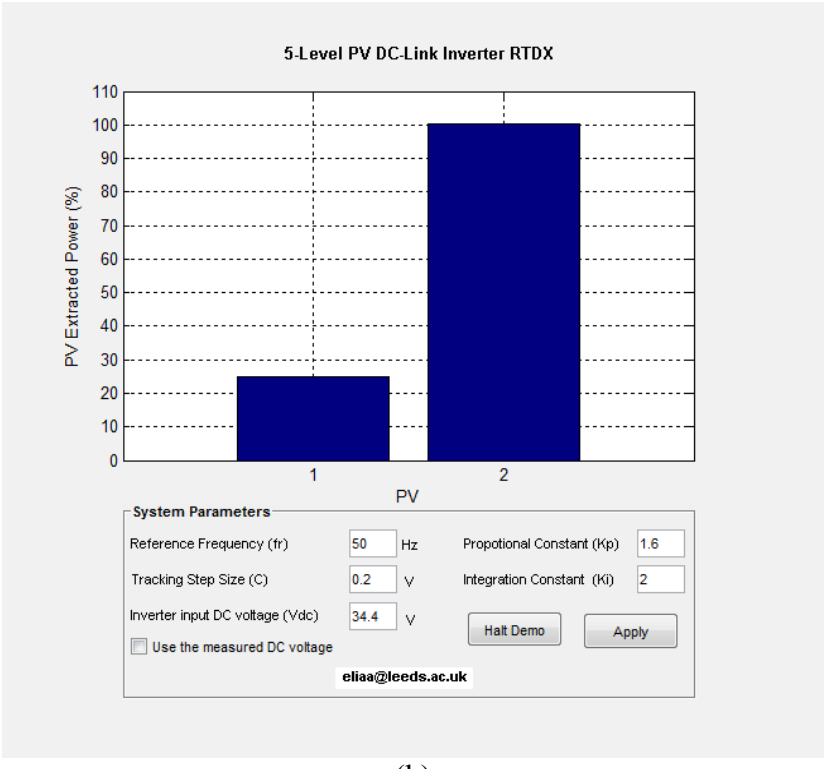


Fig.7.21: PV current and voltage waveforms at G_{pv1}=1000 W/m^2, G_{pv2}=250 W/m^2 obtained by PV permutation algorithm for two PV sources DC-link inverter.

The GUI windows given in Fig.7.22a and Fig.7.22b show the extracted power of PV1 and PV2. Fig.7.22a is at irradiances of G_{pv1}=1000 W/m^2, G_{pv2}=250 W/m^2, while Fig.7.22b is at irradiances of G_{pv1}=250 W/m^2, G_{pv2}=1000 W/m^2.



(a)



(b)

Fig.7.22: RTDX GUI window for two PV sources DC-link inverter controlled by PV permutation algorithm at (a) G_{pv1}=1000 W/m^2, G_{pv2}=250 W/m^2 and (b) G_{PV1}=250 W/m^2, G_{PV2}=1000 W/m^2.

7.6 PV Permutation Algorithm for Seven-Level DC-Link Inverter

The PV permutation algorithm is also applied to the seven-level DC-link inverter shown in Fig.6.12. Under different partial shading conditions, the system are used to overcome the PV shading problem of three PV modules connected in series. The inverter control is carried out in the real-time and Matlab-Simulink RTDX with GUI shown in Fig.6.22 is applied. The system parameters are equal to those listed in Table 7.3 except K_p=0.2 and K_i=2.

The lighting source consists of three groups of halogen bulbs each supplied from a different phase of three-phase main supply as illustrated in Fig.7.23.

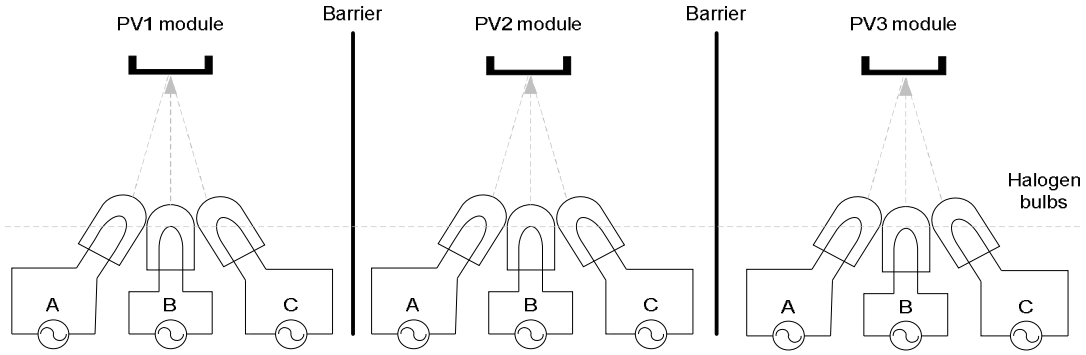


Fig.7.23: Three-phase halogen lighting structure.

To overcome the problem of imbalance in the level of irradiance for all three PV modules, the irradiance meter is used to measure the related irradiance for each PV module. Also, as it can be seen in Fig.7.24, when the three PV modules are connected in series to a load, they operate at the same value of voltage.

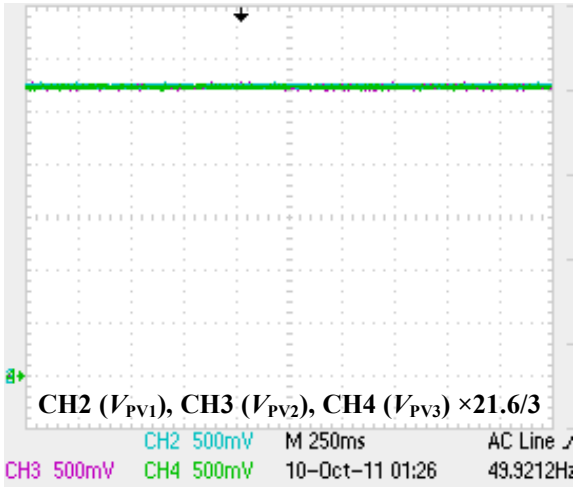


Fig.7.24: PV modules voltages under identical irradiance of 1000 W/m^2 (I_{PV}=670 mA, R_L=40 Ω, room and PV surface temperature of 20°C and 55°C).

Fig.7.25 shows the inverter output voltage and current waveforms achieved by using a 30 Ω load. The results were obtained at the ambient temperature of 18°C and the PV surface temperature is 50°C for the three PV modules under equal irradiances of 1000 W/m^2.

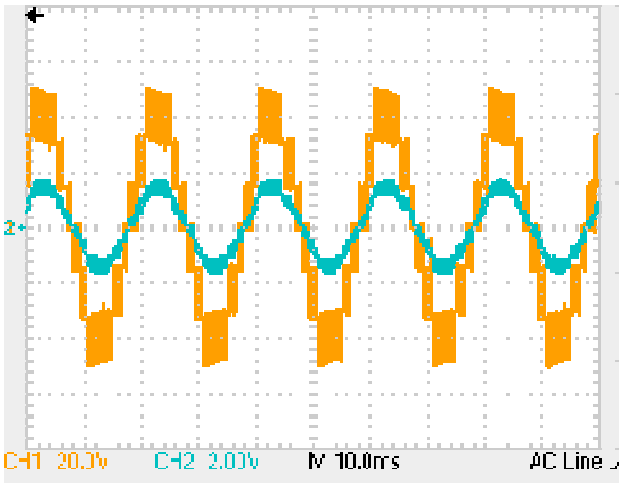


Fig.7.25: Seven-level output voltage (CH1) and current (CH2) waveforms at G_{pv1}, G_{pv2}, G_{pv3}=1000 W/m^2 obtained by using PV permutation algorithm.

The three PV modules generate equal amounts of currents as shown in Fig.7.26. Also, the power levels generated from the PV modules are almost identical to each other as it is presented in the GUI window shown in Fig.7.27.

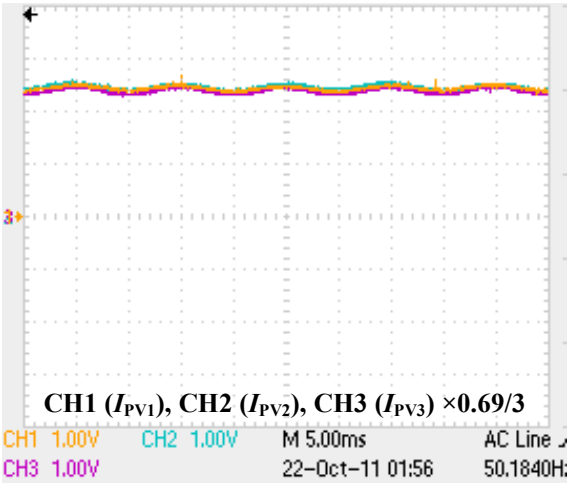


Fig.7.26: PV modules currents under identical irradiance of 1000 W/m^2.

When the inverter is used to supply R-L load of 30 Ω resistance and 2 mH inductance, the accomplished output load current and voltage waveforms are shown in Fig.7.28.

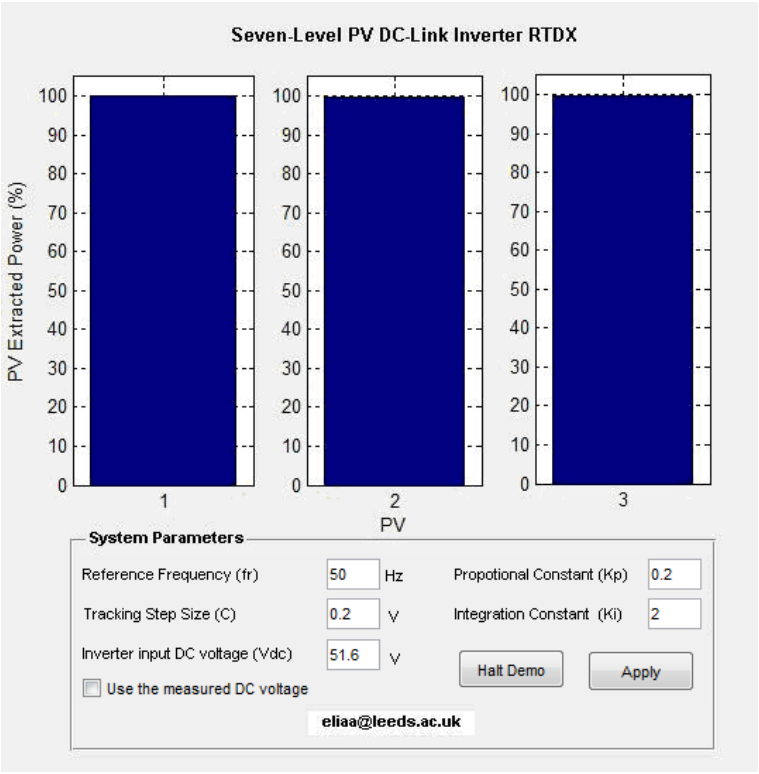


Fig.7.27: RTDX GUI window for three PV sources DC-link inverter controlled by PV permutation algorithm at full irradiance of 1000 W/m^2.

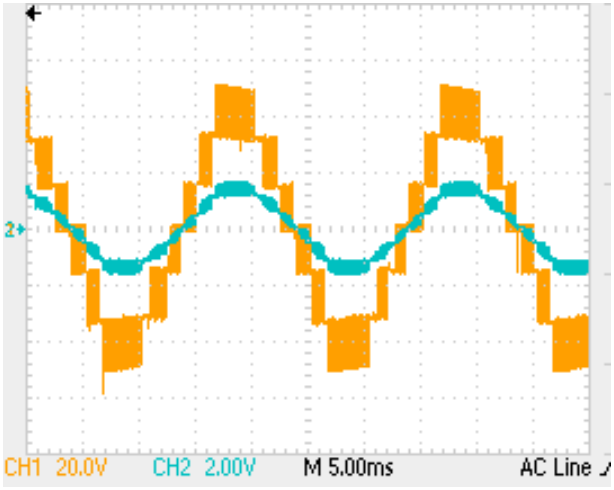


Fig.7.28: R-L load voltage (CH1) and current (CH2) waveforms at G_{pv1}, G_{pv2}, G_{pv3}=1000 W/m^2 achieved by PV permutation algorithm for three PV sources DC-link inverter.

Figures 7.29 and 7.30 show the output voltage waveform at different resistive loads. Fig.7.29 relates to a resistive load of 16.5 Ω, while Fig.7.30 is taken at resistive load of 4.5 Ω. The experiment was carried out at room and PV surface temperature of 18°C and 50°C respectively. The three PV modules are at full irradiance and each operates at the maximum power point of 10 W.

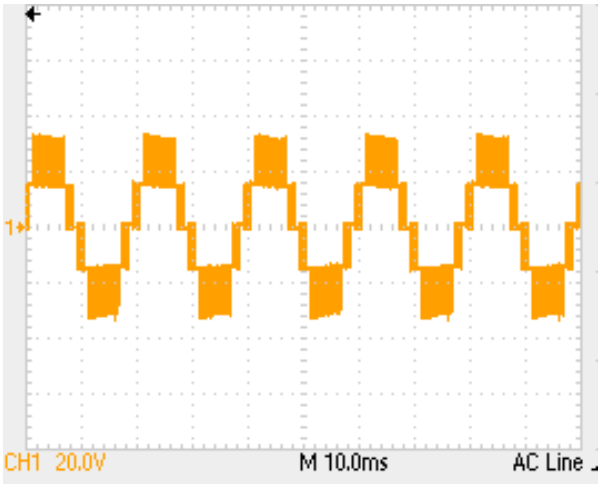


Fig.7.29: Voltage waveform of 16.5 Ω at identical irradiance of 1000 W/m^2 obtained using PV permutation algorithm for three PV sources DC-link inverter

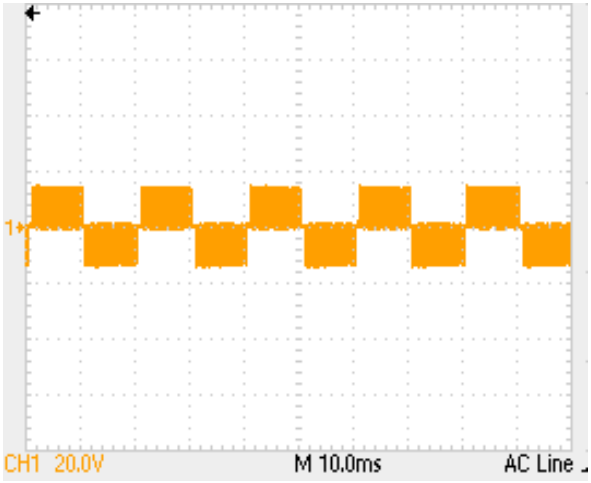
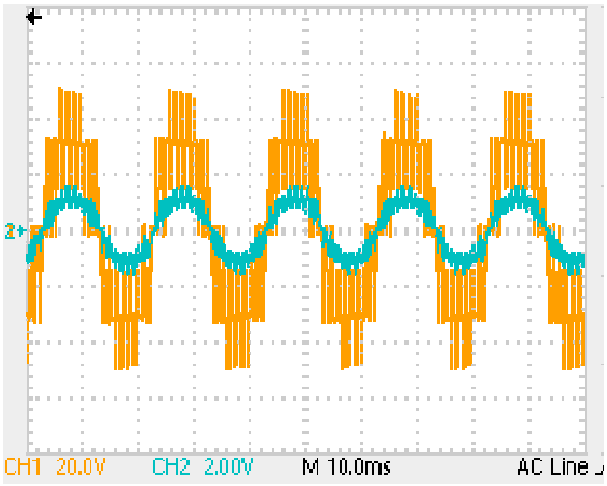


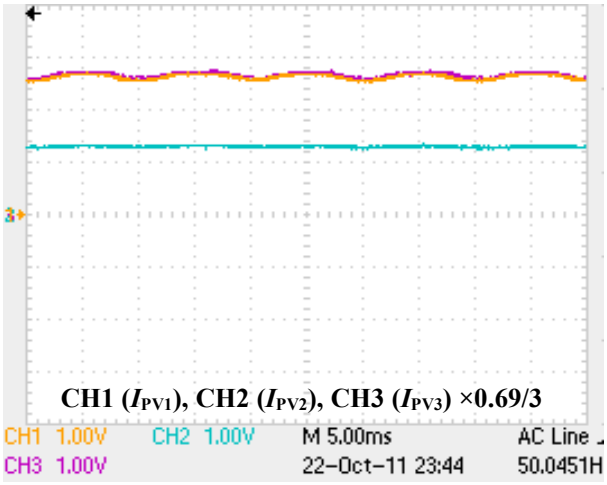
Fig.7.30: Voltage waveform of 4.5 Ω at identical irradiance of 1000 W/m^2 obtained using PV permutation algorithm for three PV sources DC-link inverter.

Figures 7.31-7.38 show the results of applying asymmetrical (unbalanced) irradiances on the system PV modules. Fig.7.31a shows the load current and voltage waveforms at irradiances of G_{pv1}=G_{pv3}=1000 W/m^2, G_{pv2}=500 W/m^2 when the load resistance is 30 Ω. The PV modules current and voltage waveforms are shown in Fig.7.31b and Fig.7.31c respectively. The load current and voltage waveforms which is achieved under irradiances of G_{pv1}=G_{pv2}=1000 W/m^2, G_{pv3}=150 W/m^2 are shown in Fig.7.32a, while Fig.7.32b and Fig.7.32c illustrate the PV modules current and voltage waveforms at the same level of irradiances. The results of applying irradiances of G_{pv1}=1000 W/m^2, G_{pv2}=750 W/m^2, G_{pv3}=250 W/m^2 are shown in Fig.7.33. Also, Fig.7.34 illustrates the obtained results for irradiances of G_{pv1}=500 W/m^2, G_{pv2}=1000 W/m^2, G_{pv3}=250 W/m^2. The surface temperatures are: 50°C at 1000 W/m^2, 40°C at 750 W/m^2, 35°C at 500 W/m^2, 25°C at 250 W/m^2 and 150 W/m^2. (The ambient

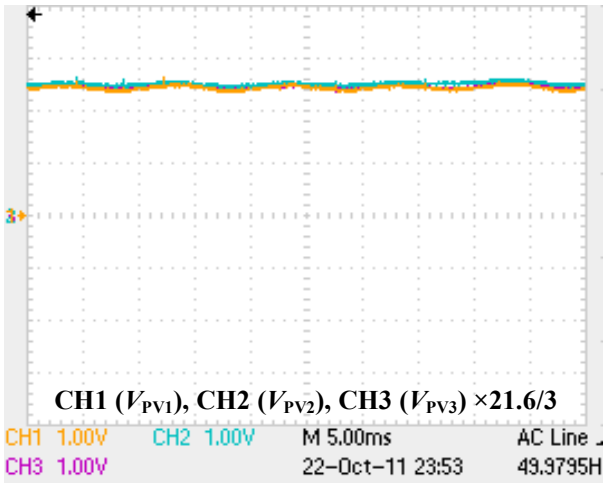
temperature is 18°C). The related PV extracted powers depicted in real-time mode of operation via the RTDX GUI window are shown in Fig.7.35 to Fig.7.38.



(a)

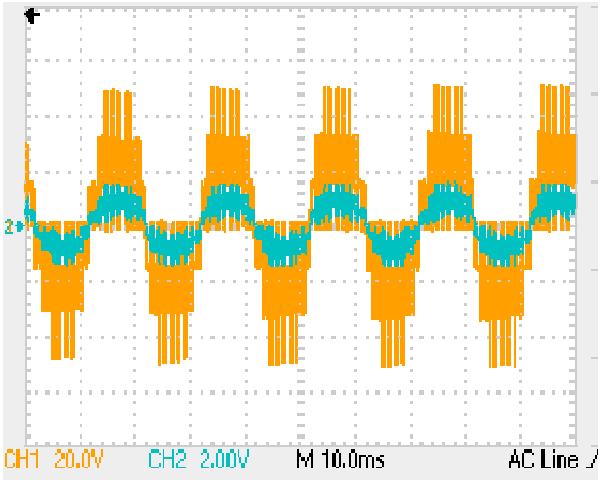


(b)

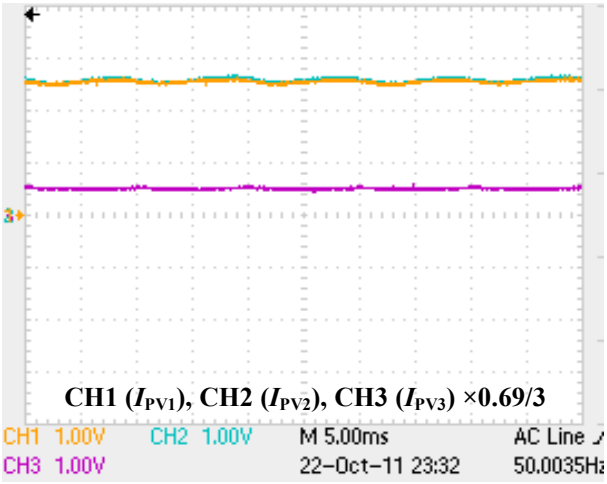


(c)

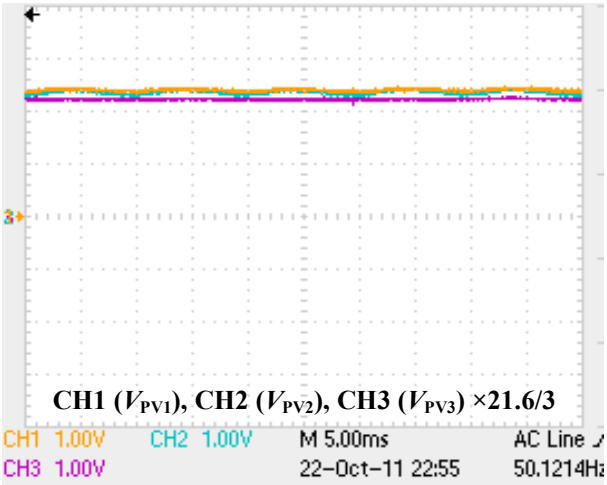
Fig.7.31: Three PV sources DC-link inverter (a) load voltage (CH1) and current (CH2), (b) PV currents, and (c) PV voltages waveforms. G_{pv1}=G_{pv3}=1000 W/m^2, G_{pv2}=500 W/m^2, achieved by applying PV permutation algorithm.



(a)

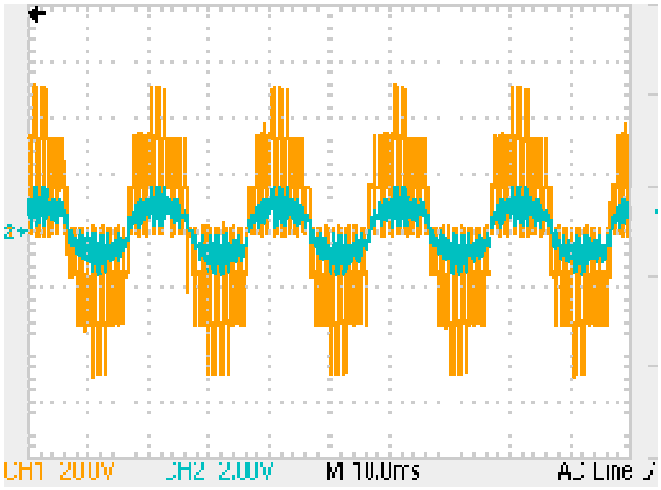


(b)

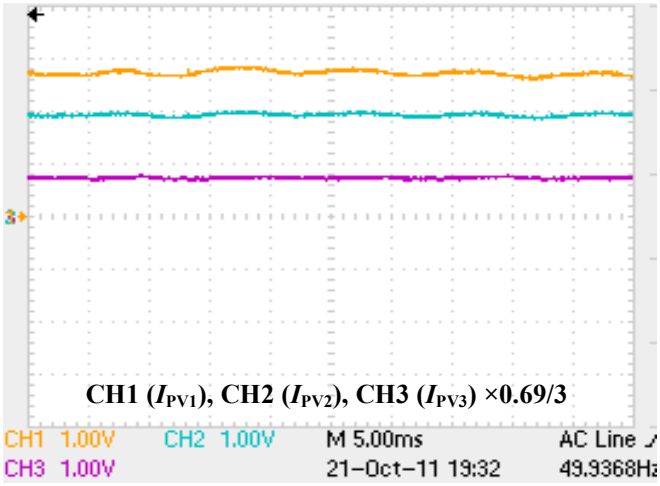


(c)

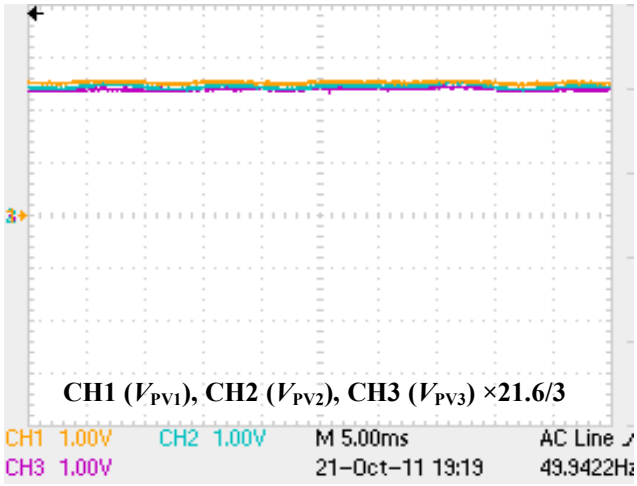
Fig.7.32: Three PV sources DC-link inverter controlled by PV permutation algorithm (a) load voltage (CH1) and current (CH2), (b) PV currents, and (c) PV voltages waveforms. G_{pv1}=G_{pv2}=1000 W/m^2, G_{pv3}=150 W/m^2.



(a)

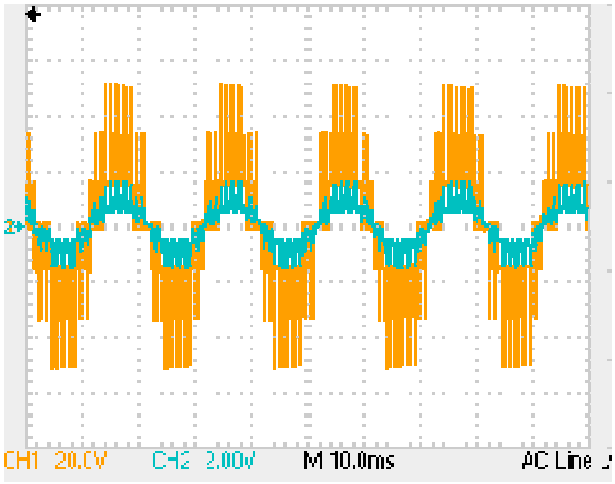


(b)

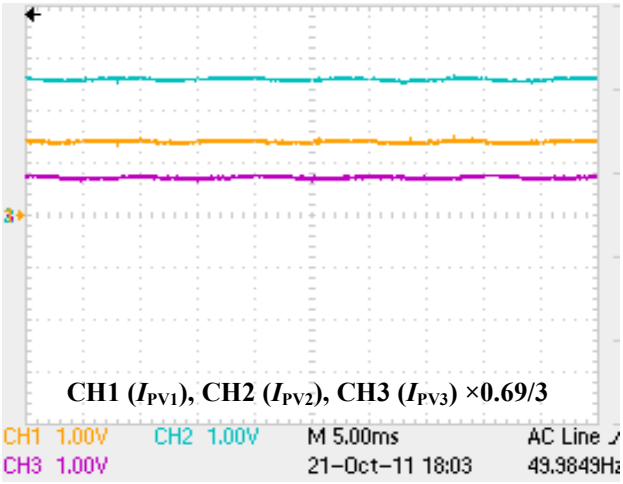


(c)

Fig.7.33: Three PV sources DC-link inverter controlled by PV permutation algorithm (a) load voltage (CH1) and current (CH2), (b) PV currents, and (c) PV voltages waveforms. G_{pv1}=1000 W/m^2, G_{pv2}=750 W/m^2, G_{pv3}=250 W/m^2.



(a)



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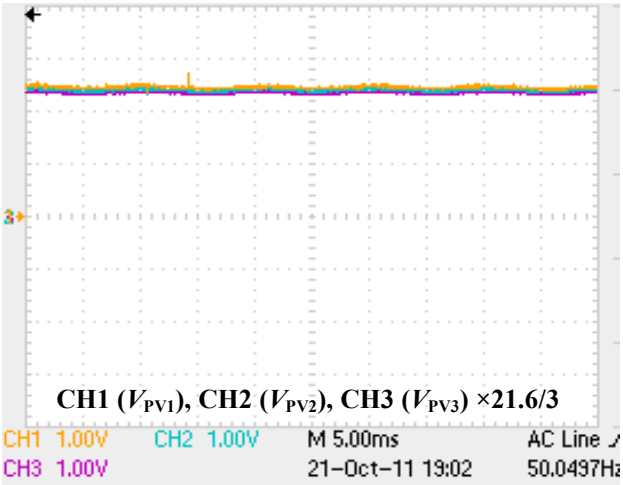

(c)

Fig.7.34: Three PV sources DC-link inverter controlled by PV permutation algorithm (a) load voltage (CH1) and current (CH2), (b) PV currents, and (c) PV voltages waveforms. G_{pv1}=500 W/m^2, G_{pv2}=1000 W/m^2, G_{pv3}=250 W/m^2.

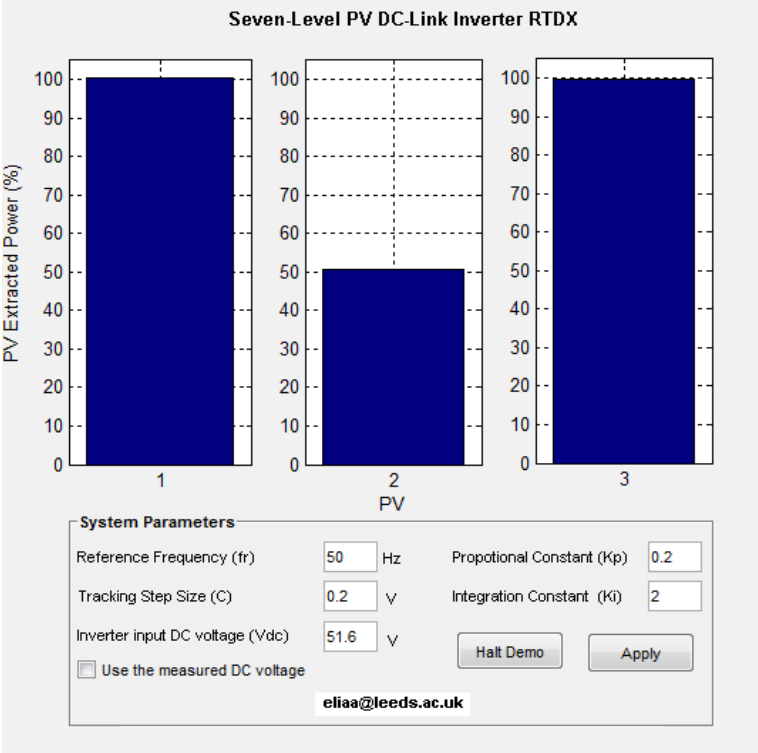

Fig.7.35: RTDX GUI window for three PV sources DC-link related to Fig.6.31.

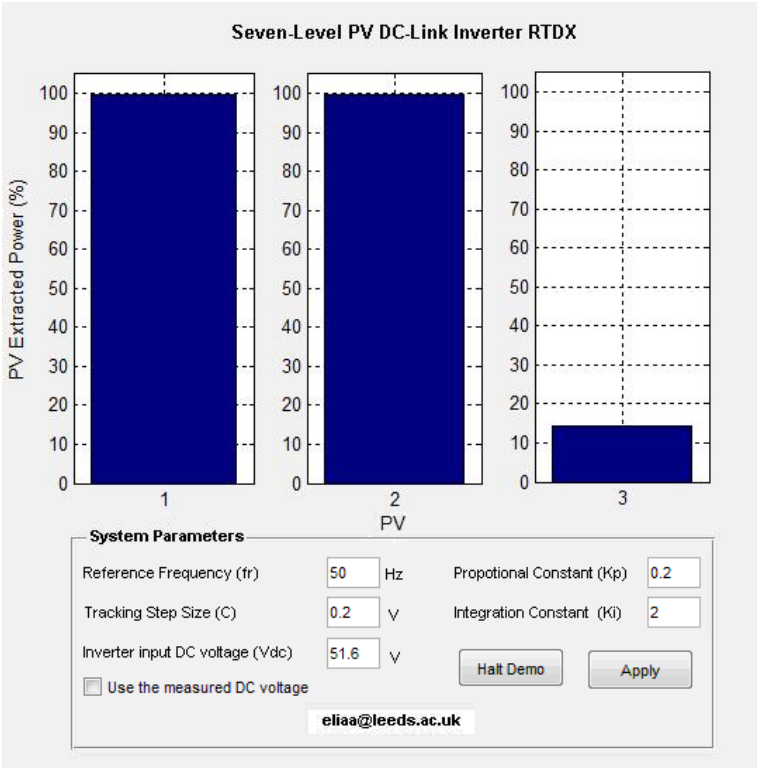

Fig.7.36: RTDX GUI window for three PV sources DC-link related to Fig.6.32.

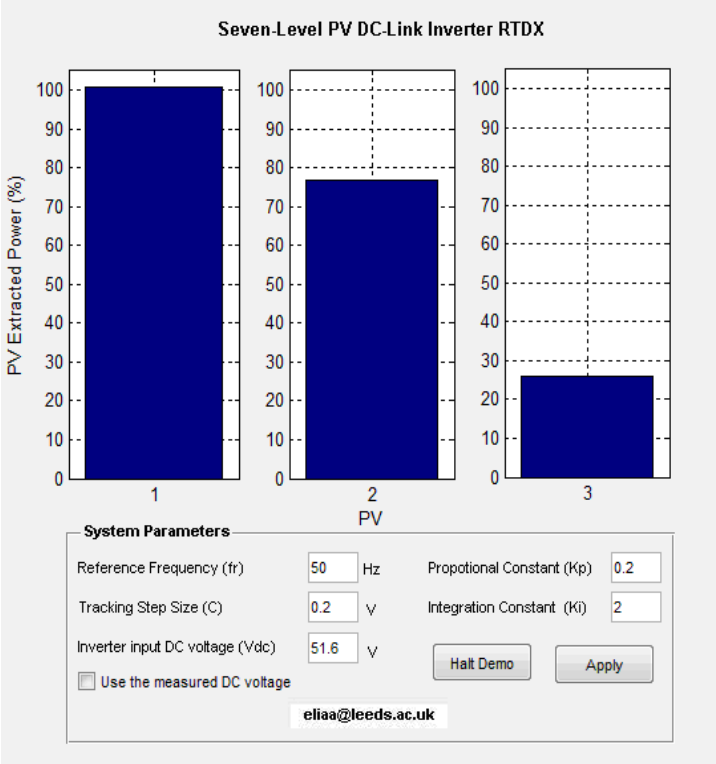

Fig.7.37: RTDX GUI window for three PV sources DC-link related to Fig.6.33.

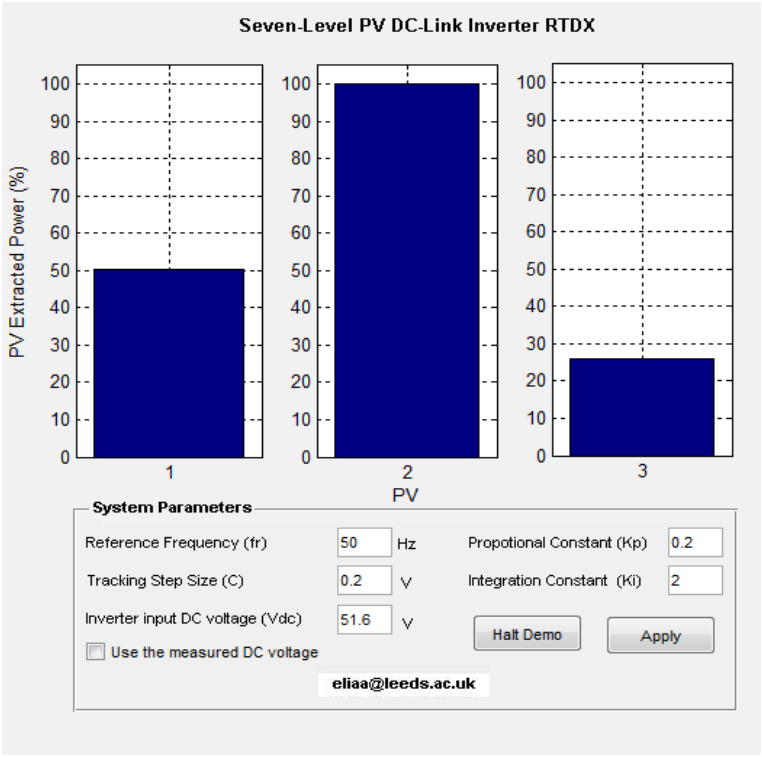

Fig.7.38: RTDX GUI window for three PV sources DC-link related to Fig.6.34.

The presented results for the PV permutation algorithm confirm that the shaded PV sources do not affect the operation of non-shaded sources of the system, so they continue to deliver their maximum power to the load. However, the multilevel

voltage waveforms need to be improved, so the total harmonic distortion can be minimized. The improvement of the output waveform quality is considered in the following section.

7.7 Improved PV Permutation Algorithm for Seven-Level DC-Link Inverter

The generalized improved PV permutation algorithm described in section 5.2 is applied to the seven-level DC-link inverter shown in Fig.6.12. For comparison purpose, the experiment was carried out at same conditions and system parameters as in the previous section. The following figures show the improved load current and voltage waveforms under partial shading conditions. With respect to PV modules current and voltage waveforms and the GUI windows, all are similar to those obtained in the previous section.

As it can be seen in Fig.7.39 to Fig.7.42, the load current and voltage waveforms are much improved compared with the achieved waveforms in Fig.7.31 to Fig.7.34. The predicted results achieved via the SSA module (section 5.1.1) are presented as well, where the applied parameters are similar to those used in the experimental system and the I-V characteristic of the simulated PV module shown in Fig.7.5 under different irradiance levels.

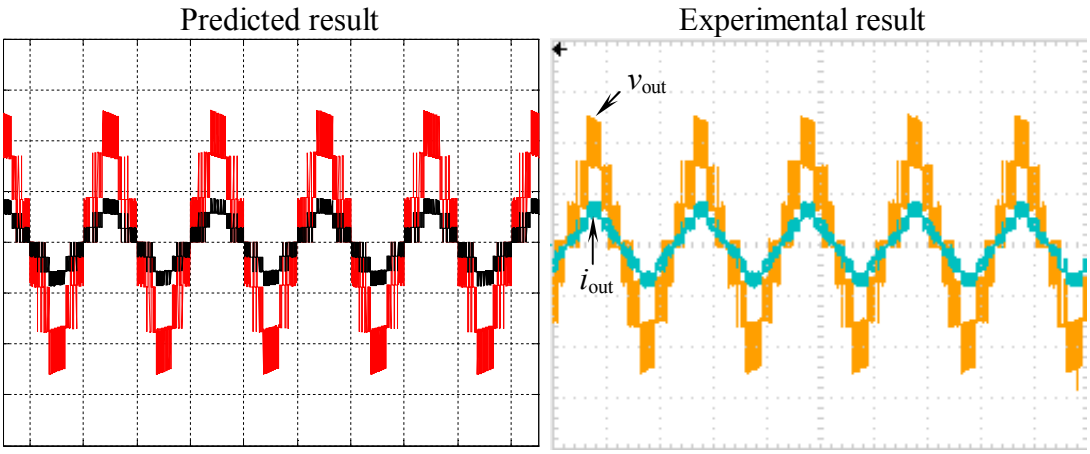

Fig.7.39: Load current and voltage waveforms of three PV sources DC-link inverter controlled by improved PV permutation algorithm at irradiances of G_{pv1}=G_{pv3}=1000 W/m^2, G_{pv2}=500 W/m^2 (v_{out} at 20 V/div, i_{out} at 2 A/div, time at 10 ms/div).

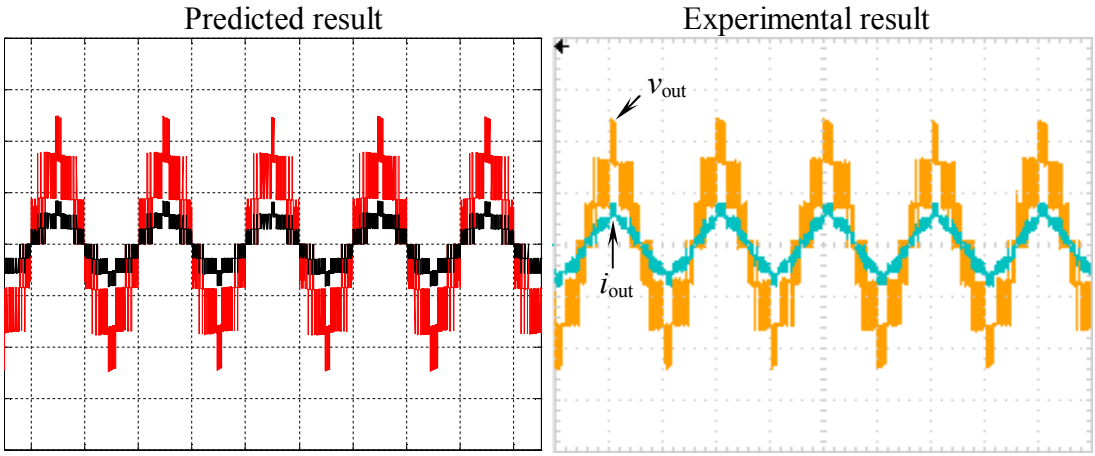

Fig.7.40: Load current and voltage waveforms of three PV sources DC-link inverter controlled by improved PV permutation algorithm at irradiances of G_{pv1}=G_{pv2}=1000 W/m^2, G_{pv3}=150 W/m^2 (v_{out} at 20 V/div, i_{out} at 2 A/div, time at 10 ms/div).

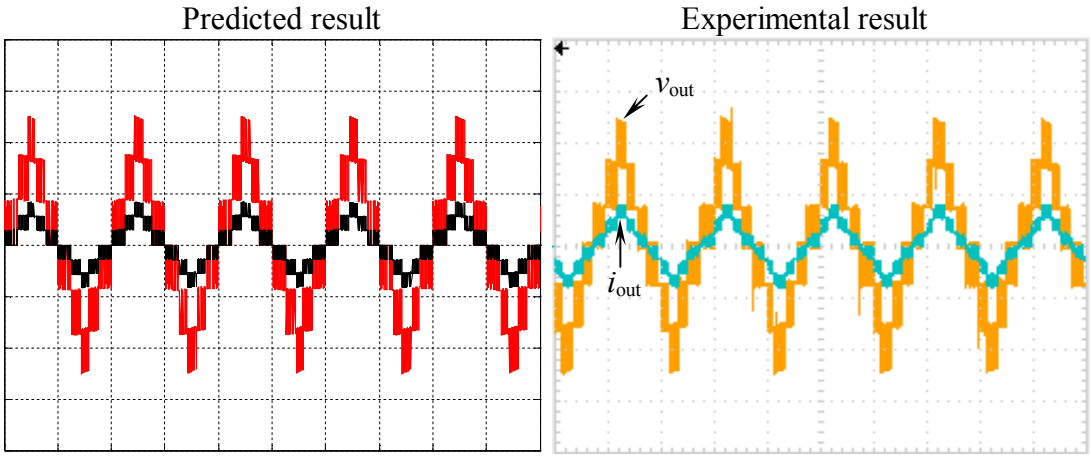

Fig.7.41: Load current and voltage waveforms of three PV sources DC-link inverter controlled by improved PV permutation algorithm at irradiances of G_{pv1}=1000 W/m^2, G_{pv2}=750 W/m^2, G_{pv3}=250 W/m^2 (v_{out} at 20 V/div, i_{out} at 2 A/div, time at 10 ms/div).

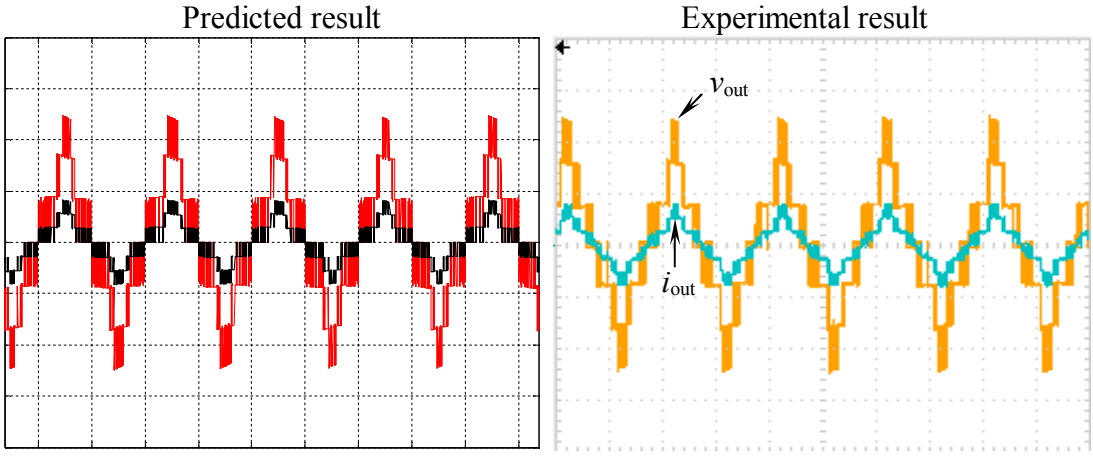

Fig.7.42: Load current and voltage waveforms of three PV sources DC-link inverter controlled by improved PV permutation algorithm at irradiances of G_{pv1}=500 W/m^2, G_{pv2}=1000 W/m^2, G_{pv3}=250 W/m^2 (v_{out} at 20 V/div, i_{out} at 2 A/div, time at 10 ms/div).

The extracted power from each PV source is shown via the GUI window in real-time mode. As can be seen, the shaded PV sources do not affect the operation of the other non-shaded sources and therefore they continue generating their maximum power as illustrated in Fig.7.35-7.38. Even in the case of high shading level, the shaded PV source is not bypassed and continues to generate power as it can be seen in Fig.7.37 where the PV extracted power of the shaded source is 1.5 W.

Table 7.4 describes the THD and the 50Hz fundamental amplitude of the load voltage waveforms (Fig.7.31-7.34 and Fig.7.39-7.42) for both the normal and the improved PV permutation algorithms as a function of the PV extracted power. It is noticeable that the improved PV permutation algorithm resulted in achieving lower output harmonic distortion than that is resulted by applying the normal PV permutation algorithm at the same level of generated power by each PV source, which, the fundamental harmonic (50 Hz) is larger.

TABLE 7.4: THD and the Fundamental Amplitude of the Load Voltage at Various Partial Shading Levels

Extracted power (W)			PV Permutation algorithm (Exp)		Improved PV permutation (Exp)		Improved PV permutation (SSA)	
PV1	PV2	PV3	THD(%)	$V_{1(P)}$(V)	THD(%)	$V_{1(P)}$(V)	THD(%)	$V_{1(P)}$(V)
10	5	10	40.26	35.16	36.00	36.33	34.05	36.23
10	10	1.5	55.21	30.83	34.80	33.26	33.68	34.18
10	7.5	2.5	64.92	29.91	40.50	31.37	42.38	31.80
5	10	2.5	61.22	27.95	38.46	29.07	43.65	29.37

Table 7.5 describes the results of the total power delivered to the load obtained by the mathematical model and that of experiments (Fig.7.39-7.42). Also, the power which is calculated via the 50Hz fundamental component is presented. The simulation and experimental results are close to each other and they show that almost all the extracted power of the PV modules are delivered to the load, so no power is used in feedback to maintain the shaded PV modules operating at their MPP, as it is the case with some other methods of solving the partial shading problem.

TABLE 7.5: Load Power at Various Partial Shading Levels

Extracted power (W)			Mathematical model Total Load Power (W)	Experimental Total Load Power (W)	Experimental $\frac{(V_{1(\text{rms})})^2}{R}$, (W)
10	10	10	29.96	28.89	26.07
10	5	10	24.96	23.81	22.00
10	10	1.5	21.44	21.01	18.44
10	7.5	2.5	19.98	19.34	16.40
5	10	2.5	17.49	17.20	14.08

7.8 Summary

This chapter included the experimental results which confirm the proper operation of the implemented PV systems including the MPPT control and the digital PWM control improvements. Also, the algorithm for partial shading solution has been verified.

The lighting test results showed that halogen lighting causes lower PV current flickering than the high-presser sodium (HPS) lighting. However, more PV power can be achieved via the HPS lighting than by the halogen lighting. The halogen three-phase lighting was chosen for applying in the experiments because of its low flickering effect and also its simplicity of control for emulating the desired shading conditions.

The I-V characteristics of the used PV module were successfully achieved under varies irradiances levels by using a MOSFET as a controllable impedance load.

The MPPT results obtained from the buck converter closed-loop controlled PV system using VH-P&O algorithm showed low oscillations and correct MPP tracking during the irradiance changes compared with the results obtained by the conventional P&O algorithm.

The results of the generalized IPWM algorithm were presented, where five-level AC voltage waveform and a low output harmonic distortion was achieved successfully at the MPP of the PV modules.

The PV permutation algorithm and the improved PV permutation algorithm were successfully applied to the DC-link inverter in order to overcome the PV partial shading problem. The results including the current and voltage waveforms for load and PV modules, as well as the PV extracted power which is displayed via RTDX GUI window, were presented. The results confirmed that by applying the multilevel DC-link inverter controlled by the PV permutation algorithm, the PV sources in the PV string connection can operate at their MPP under unsymmetrical irradiance levels.

The improved PV permutation algorithm enabled a significant improvement of the output voltage waveforms in terms of THD and fundamental harmonic amplitude and also that almost all the PV generated power at MPP was delivered to the load without reduction.

Chapter 8

Conclusions and Recommendations

8.1 Conclusions

The study presented in this thesis was carried out firstly to compare existing (reported) methods used to overcome the problems which arise from partial shading of series connected PV sources and subsequently to investigate a new method to resolve this problem. A multilevel DC-Link inverter is used for the first time to deal with the issue of partial shading and a novel control algorithm, 'PV permutation algorithm', was introduced to control the multilevel DC-link inverter. The proposed system maintains operation of all the series connected PV sources at their maximum power points (MPPs) and delivers the extracted PV power of each PV source to the load irrespective of exposure to asymmetrical irradiance levels. The thesis accomplishments and contributions can be summarized as follows:

- The consequences caused by the partial shading, for instance hot spot and the reduction of generated powers were studied including bypass diode protection and the worst case condition of the shaded PV source, along with the necessary simulation results with emphasizes on the cell reverse mode of operation, the effects of the PV cell shunt resistance, and the shaded cells number. Although the bypass diode across each PV source protects the shaded PV source from being damaged, the extractable power under partial shading is significantly reduced;

- Detailed investigation and comparison of the existing schemes have been introduced to cope with the PV partial shading problem. The investigation covered limitations of different schemes and their qualitative comparison

focused on the ability to provide MPP operation for each PV source in the system and to deliver the total extracted power to the load. The multilevel inverter approach appeared interesting for the research because the circuit topology allows proper control of each PV source to maximize the individual power and to achieve high quality output AC voltage waveform;

- A multilevel DC-link inverter circuit was modelled in generalized forms using a state space averaging (SSA) method. The generalized forms obtained when the inverter supplying R, R-L load or grid-connected can be used for any number of individual PV sources;
- A detailed analysis and comparison of different multilevel inverter switching techniques was accomplished. Three-level Integration Duty Cycle Conversion PWM (IPWM) was applied to a generalized algorithm and implemented experimentally into a five-level DC-link inverter. Although the simulation study proved that Space Vector PWM, direct PWM and IPWM produced the same results in terms of THD, direct PWM is the simplest switching method to implement and requires the lowest computational effort;
- The investigation of the common maximum power point tracking (MPPT) methods highlighted tracking limitations and led to the introduction of an improved tracking algorithm termed 'Voltage-Hold Perturbation and Observation MPPT' algorithm. The simulation and experimental results showed that this algorithm helps overcome tracking limitations which are oscillation around the MPP and MPP loss during irradiance changes;
- Another novel algorithm named PV Permutation has been introduced to control the DC-link inverter under PV partial shading conditions. The algorithm enables maximum power extraction from each PV source to the load while preserving the operation of the series connected PV sources at their individual MPPs, and generation of low THD output voltage waveforms;
- Simulation and experimental tests were performed on the proposed system under varied irradiance conditions. The desired SSA circuit models were used in simulation along with the introduced PV permutation algorithms. The results for different loads and irradiance conditions were obtained for up to

five PV sources (eleven-level) inverter. The experimental implementations included five and seven-level inverters, controlled by using processing unit eZdsp^{TM} F28335. The control was carried out in the real time data exchange (RTDX) via Matlab-Simulink. The output voltage waveforms under various partial shading levels showed low THD. The simulation and the experimental results have confirmed the effectiveness of the introduced system.

8.2 Recommendation for Future Research

- In the transformerless multilevel grid-connected system, it is not possible to boost the voltage generated by the inverter. Consequently, if there is any failure or a significant voltage drop in at least one of its DC inputs, the inverter will not meet the grid voltage requirement. This problem is similar to the PV partial shading issue, where the shaded PV source is bypassed via a diode causing a drop in the inverter output voltage. As seen in Figures 7.31c to 7.34c, the introduced method maintains almost equal voltage for all the PV sources while their currents are varied according to their irradiance levels ($\Delta V_{mpp}(G) << \Delta I_{mpp}(G)$), so the grid voltage requirement can be maintained even under partial shading conditions. This can be a significant advantage for future grid-connected applications.

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Appendix A

Improved Output Generation from Three PV Sources Inverter

c	$v_{offset1}$	$v_{offset2}$	$v_{offset3}$	V_{ol}	V_{oh}	t_{on}
1	0	0	0	0	V_{PV1}	t_{on1}
	0	0	1	0	0	
	0	0	2	V_{PV3}	V_{PV3}	
	0	1	0	V_{PV2}	V_{PV2}	
	0	1	1	V_{PV2}	V_{PV2}	
	0	1	2	$V_{PV2}+V_{PV3}$	$V_{PV2}+V_{PV3}$	
	0	2	0	V_{PV2}	V_{PV2}	
	0	2	1	$V_{PV2}+V_{PV3}$	$V_{PV2}+V_{PV3}$	
	0	2	2	$V_{PV2}+V_{PV3}$	$V_{PV2}+V_{PV3}$	
	1	0	0	0	V_{PV1}	
	1	0	1	0	V_{PV1}	
	1	0	2	V_{PV3}	$V_{PV1}+V_{PV3}$	
	1	1	0	V_{PV2}	$V_{PV1}+V_{PV2}$	
	1	1	1	V_{PV2}	$V_{PV1}+V_{PV2}$	
	1	1	2	$V_{PV2}+V_{PV3}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
	1	2	0	V_{PV2}	$V_{PV1}+V_{PV2}$	
	1	2	1	$V_{PV2}+V_{PV3}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
	1	2	2	$V_{PV2}+V_{PV3}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
	2	0	0	0	V_{PV1}	
	2	0	1	V_{PV3}	$V_{PV1}+V_{PV3}$	
	2	0	2	V_{PV3}	$V_{PV1}+V_{PV3}$	
	2	1	0	V_{PV2}	$V_{PV1}+V_{PV2}$	
	2	1	1	$V_{PV2}+V_{PV3}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
	2	1	2	$V_{PV2}+V_{PV3}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
	2	2	0	V_{PV2}	$V_{PV1}+V_{PV2}$	
	2	2	1	$V_{PV2}+V_{PV3}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
	2	2	2	$V_{PV2}+V_{PV3}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
2	0	0	0	0	V_{PV2}	t_{on2}
	0	0	1	V_{PV3}	V_{PV3}	
	0	0	2	V_{PV3}	V_{PV3}	
	0	1	0	0	V_{PV2}	
	0	1	1	V_{PV3}	$V_{PV2}+V_{PV3}$	
	0	1	2	V_{PV3}	$V_{PV2}+V_{PV3}$	
	0	2	0	0	V_{PV2}	
	0	2	1	V_{PV3}	$V_{PV2}+V_{PV3}$	
	0	2	2	V_{PV3}	$V_{PV2}+V_{PV3}$	
	1	0	0	0	0	
	1	0	1	V_{PV3}	V_{PV3}	
	1	0	2	$V_{PV1}+V_{PV3}$	$V_{PV1}+V_{PV3}$	
	1	1	0	0	V_{PV2}	
	1	1	1	V_{PV3}	$V_{PV2}+V_{PV3}$	
	1	1	2	$V_{PV1}+V_{PV3}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
	1	2	0	V_{PV1}	$V_{PV1}+V_{PV2}$	
	1	2	1	$V_{PV1}+V_{PV3}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
	1	2	2	$V_{PV1}+V_{PV3}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
	2	0	0	V_{PV1}	V_{PV1}	
	2	0	1	$V_{PV1}+V_{PV3}$	$V_{PV1}+V_{PV3}$	
	2	0	2	$V_{PV1}+V_{PV3}$	$V_{PV1}+V_{PV3}$	
	2	1	0	V_{PV1}	$V_{PV1}+V_{PV2}$	
	2	1	1	$V_{PV1}+V_{PV3}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
	2	1	2	$V_{PV1}+V_{PV3}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
	2	2	0	V_{PV1}	$V_{PV1}+V_{PV2}$	
	2	2	1	$V_{PV1}+V_{PV3}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
	2	2	2	$V_{PV1}+V_{PV3}$	$V_{PV1}+V_{PV2}+V_{PV3}$	

c	$v_{offset1}$	$v_{offset2}$	$v_{offset3}$	V_{ol}	V_{oh}	t_{on}
3	0	0	0	0	V_{PV3}	t_{on3}
	0	0	1	0	V_{PV3}	
	0	0	2	0	V_{PV3}	
	0	1	0	0	0	
	0	1	1	0	V_{PV3}	
	0	1	2	V_{PV2}	$V_{PV2}+V_{PV3}$	
	0	2	0	V_{PV2}	V_{PV2}	
	0	2	1	V_{PV2}	$V_{PV2}+V_{PV3}$	
	0	2	2	V_{PV2}	$V_{PV2}+V_{PV3}$	
	1	0	0	V_{PV1}	V_{PV1}	
	1	0	1	V_{PV1}	$V_{PV1}+V_{PV3}$	
	1	0	2	V_{PV1}	$V_{PV1}+V_{PV3}$	
	1	1	0	V_{PV1}	V_{PV1}	
	1	1	1	V_{PV1}	$V_{PV1}+V_{PV3}$	
	1	1	2	$V_{PV1}+V_{PV2}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
	1	2	0	$V_{PV1}+V_{PV2}$	$V_{PV1}+V_{PV2}$	
	1	2	1	$V_{PV1}+V_{PV2}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
	1	2	2	$V_{PV1}+V_{PV2}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
	2	0	0	V_{PV1}	V_{PV1}	
	2	0	1	V_{PV1}	$V_{PV1}+V_{PV3}$	
	2	0	2	V_{PV1}	$V_{PV1}+V_{PV3}$	
	2	1	0	$V_{PV1}+V_{PV2}$	$V_{PV1}+V_{PV2}$	
	2	1	1	$V_{PV1}+V_{PV2}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
	2	1	2	$V_{PV1}+V_{PV2}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
	2	2	0	$V_{PV1}+V_{PV2}$	$V_{PV1}+V_{PV2}$	
	2	2	1	$V_{PV1}+V_{PV2}$	$V_{PV1}+V_{PV2}+V_{PV3}$	
	2	2	2	$V_{PV1}+V_{PV2}$	$V_{PV1}+V_{PV2}+V_{PV3}$	