Transport in gated InAs/GaSb coupled quantum wells: exploring carrier regime crossover and integrating ferromagnetic contacts

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Abstract

This thesis presents the study of carrier dynamics at the boundary of the charge neutral transport regime in InAs/GaSb quantum wells (QWs) and the implementation of integrated ferromagnetic contacts onto InAs/GaSb QW devices. As promising candidate materials for hosting a quantum spin Hall insulator state, InAs/GaSb QWs have been the subject of intensive study for over fifteen years. The conducting helical edge states characteristic of this phase are of particular interest, as the associated spin-momentum locked transport has yet to be measured directly. In this QW structure, the band inversion required to host a quantum spin Hall state is promoted by the broken-gap alignment of the InAs and GaSb. The band alignment can also be tuned by gate voltage application.

The first focus of this thesis is the gate tuning of InAs/GaSb QW Hall bar devices to the boundary of the charge neutral regime, where the Lifshitz-Kosevich model is applied at varying carrier densities in a scan-like approach to determine a breakdown region of (4.3 - 6.8) $\times$ 10^{11} cm^{-2}, in which its associated assumptions no longer apply. The contested existence of a non-trivial Berry phase is also explored, determining that no such phase is present.

The remainder of this thesis is devoted to the fabrication and optimisation of novel micron-scale and nano-scale InAs/GaSb devices with integrated ferromagnetic contacts. First, micron-scale transmission line devices were fabricated, which enabled the refinement of the ferromagnetic contact-(InAs/GaSb) interface to produce a reliably ohmic junction, along with the determination of contact resistance and other characteristics. This established a foundation for the fabrication of transmission line devices with low micron- to nano-scale contact separations. With the design and fabrication adjustments outlined in this thesis, this work provides a platform for future pioneering experiments detecting spin-dependent transport in InAs/GaSb QWs.

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Abbreviations

2DEG	Two Dimensional Electron Gas
AC	Alternating Current
ALD	Atomic Layer Deposition
BNC	Bayonet Neill-Concelman
CNP	Charge Neutrality Point
DC	Direct Current
DI	Deionised
DUV	Deep Ultra-Violet
EBL	Electron Beam Lithography
FFT	Fast Fourier Transform
FM	Ferromagnetic
HF	Hydrofluoric Acid
HMDS	Hexamethyldisilazane
IPA	Isopropyl Alcohol
IQHE	Integer Quantum Hall Effect
LK	Lifshitz-Kosevich
LL	Landau Level
MBE	Molecular Beam Epitaxy
MLA	Maskless Aligner
NMP	N-Methyl-2-Pyrrolidone
PMMA	Poly(Methyl Meth-Acrylate)
Py	Permalloy
QSHE	Quantum Spin Hall Effect
QW	Quantum Well
SdH	Shubnikov de-Haas
TLM	Transition Line Model
TMAH	Tetramethylammonium Hydroxide
UV	Ultra-Violet
UVO	Ultra-Violet Ozone
VTI	Variable Temperature Insert

Chapter 1

Introduction

The groundbreaking discovery of the integer quantum Hall effect (IQHE) in 1980 [10] sparked the exploration of the topological classification of material phases. Some decades later, the QSHE was proposed [11, 12], characterised by an insulating inverted band gap that is bridged by topologically protected, spin-momentum locked conducting states. This lead to the search for 2D semiconductor systems with sufficient spin-orbit coupling strength to exhibit an inverted band gap. InAs/GaSb QWs have been proposed to possess this state [13], specifically formed by the relative alignment of the InAs and GaSb bands inducing mixing of electron and hole states. Whilst characteristics such as the quantisation of QSH states have been confirmed experimentally [14], there is no direct proof of spin-dependent transport.

The relative band alignment in InAs/GaSb QWs is controllable remotely by applying gate voltages to drive carrier populations in the QWs. This technique is utilised in this thesis to drive the carrier population toward charge neutrality in an InAs/GaSb QW Hall bar device. This is the focus of Chapter 4, where carrier dynamics are studied approaching charge neutrality in the first of three types of device featured in this thesis. Specifically, the experimental signatures of the IQHE combined with the semi-classical Lifshitz-Kosevich (LK) model, which has been previously used to describe carrier dynamics distant from charge neutrality [15]. Some studies have also attempted to use the LK model to describe dynamics inside the insulating band gap [16, 17]. Here, I have applied the model in the region approaching the charge neutral regime, determining a carrier density range in which the model breaks down. I also determine that this InAs/GaSb system does not possess a non-trivial Berry phase, the existence of which is contested [18, 19].

The remainder of this thesis is an investigation into the performance of InAs/GaSb devices integrating ferromagnetic (FM) contacts, as they offer the possibility of studying spin-polarised current injection into the edge transport regime in future experiments. This would provide a means to study spin-dependent transport in the QSH phase. Chapter 5 presents the novel fabrication method that produced micron-scale FM contact separations on transmission line devices, outlining the optimisation of the FM contact/(InAs/GaSb) interface to produce a reliably ohmic connection. This provided the groundwork for Chapter 6, which presents the fabrication and resistance measurements of transmission line devices with micron- to nano-scale FM contact separations, the third and final device type featured.

Before this, Chapter 2 provides essential background theory on the IQHE, along with a brief introduction to the QSHE that motivated this work. Chapter 3 then discusses foundational device fabrication concepts in the context of the fabrication of the Hall bar device. The fabrication methods for the FM contact devices are evaluated in their relevant chapters, building on the first fabrication method in Chapter 3 as a reference. This chapter also details general experimental setup features that apply to all device measurements, with device-specific elements covered in the relevant chapter.

Following the experimental results discussed in Chapters 4, 5 and 6, future work is considered. This includes suggestions of design and fabrication changes to the FM con-

tact devices to facilitate gated measurements, which could lead to future spin-dependent transport measurements in the QSH phase.

Chapter 2

Theory and Background

2.1 The Integer Quantum Hall Effect

The IQHE is a topological phase of matter, belonging to a new class of phases defined by the topology of a material's band structure rather than traditional spontaneous symmetry breaking. The discovery of the IQHE has paved the way for a variety of future topological effects of interest, including the QSHE. It also underpins the study of the charge dynamics in InAs/GaSb QWs studied in this thesis, as its experimental signatures and those of the concurrent Shubnikov-de Haas (SdH) effect are utilised for characterisation and measurement in Chapter 4.

2.1.1 Landau Levels

The IQHE was first measured in 1980 by von Klitzing [10] and is a quantised version of the Hall effect. In the classical limit, the Hall effect describes the application of an out-of-plane magnetic field to a current-carrying material, where the resulting Lorentz force drives a voltage perpendicular to the current. This results in a linear relationship between B and the transverse (Hall) resistance, which is the Hall voltage divided by the longitudinal current. In a two-dimensional system with sufficiently high magnetic field and low temperature, quantum effects dominate and the measured resistance departs from its classical linear behaviour to adopt discrete plateaux at predictable quantised values of resistance.

This section considers the Landau levels (LLs) that dictate the resistance quanta and the conditions required to precipitate the IQHE. Here, it will be considered largely spinless for simplicity. The crucial components of the IQHE are a two-dimensional electron gas (2DEG), subjected to low temperatures and a large out-of-plane magnetic field. The 2DEG condition is generated here by the quantum confinement of electrons in a thin film, situated between wider band gap 'barrier' material. The offsets in the conduction bands across the materials act as potential barriers to confine the electrons to the 2D plane of the thin film, forming a QW. Classically, when a 2DEG is exposed to an electric field, the electrons will propagate in the direction of said field. The additional application of a magnetic field will introduce a cyclotron motion component to the carriers' path, with cyclotron frequency

$$\omega_{\mathrm{c}} = \frac{eB}{m^*}, \tag{2.1}$$

where m^* is the effective mass of the electron parallel to the cyclotron orbit. Quantum mechanically, the quantisation of angular momentum requires confined electrons occupy discrete energy levels known as LLs, which are highly degenerate and separated by $\hbar\omega_{\mathrm{c}}$. This is shown by the quantum mechanical treatment of a free electron in the presence of an out-of-plane magnetic field. The magnetic field is introduced using a vector potential $\boldsymbol{A}$, where $B\hat{\boldsymbol{k}} = \nabla \times \boldsymbol{A}$, making the Hamiltonian for a free electron experiencing this field

$$\hat{H} = \frac{1}{2m^*} \left(\hat{\boldsymbol{p}} + e\boldsymbol{A}\right)^2, \tag{2.2}$$

where $\hat{\boldsymbol{p}}$ is the canonical momentum and the negative sign of the electron's charge is included. The Landau gauge is applied here, where $\boldsymbol{A} = Bx\hat{\boldsymbol{\jmath}}$, giving the Schrödinger equation:

$$\frac{1}{2m^*}[\hat{p}_x^2 + (\hat{p}_y + eBx)^2]\psi(x,y) = E\psi(x,y), \tag{2.3}$$

where E is energy.

The Landau gauge is chosen for convenience of calculation. Whilst it breaks translational symmetry in the x-direction during the calculation, the physical result is not dependent on the direction in the x-y plane, consistent with the fact that electrons have rotational symmetry in the out-of-plane magnetic field.

As the Landau gauge does not depend on y, the solution is a plane wave in the y direction. This means that the solution is also an eigenstate of p_y. The ansatz $\psi(x,y) = \phi(x)e^{iky}$ is chosen, and the p_y operator as $-i\hbar\frac{\partial}{\partial y}$, replacing p_y in the Hamiltonian with $\hbar k$. This yields

$$\hat{H} = \frac{p_x^2}{2m^*} + \frac{e^2B^2}{2m^*}\left(x - \frac{\hbar k}{eB}\right)^2, \tag{2.4}$$

which describes a simple harmonic oscillator centred on $x_0 = \frac{\hbar k}{eB}$ with frequency ω_c. The eigenstates are therefore

$$E_n = \left(n + \frac{1}{2}\right)\hbar\omega_\mathrm{c}, \tag{2.5}$$

with $\Delta E_n = \hbar\omega_\mathrm{c}$.

This result implies that the density of states consists of discrete LLs represented by delta functions in energy. In reality, the density of states is broadened into a Lorentzian distribution by impurity scattering. LLs are often labelled by their filling factor, ν. It describes how many LLs are filled at a given magnetic field (and carrier density), by the ratio of electrons to magnetic flux (h/e).

The number of available states is linked to the sample geometry. Continuing in the Landau gauge picture and assuming sample dimensions of $L_x \times L_y$, and following the result in Equation 2.4, the density of states is described by plane waves in the y direction with spacing $\Delta x_0 = \frac{\hbar}{eB}\Delta k$. When applying periodic boundary conditions in the y direction, $\Delta k = \frac{2\pi}{L_y}$. The degeneracy is given by

$$N_0 = \frac{L_x}{\Delta x_0} = \frac{eB}{h}L_xL_y. \tag{2.6}$$

The total number of electrons in the system is

$$N_\mathrm{e} = n_\mathrm{e}L_xL_y, \tag{2.7}$$

where the 2D carrier density is written as n_e. The filling factor is then equal to the number of electrons divided by the number of states available for the electrons to occupy, giving

$$\nu = \frac{N_\mathrm{e}}{N_0} = \frac{n_\mathrm{e}h}{eB}. \tag{2.8}$$

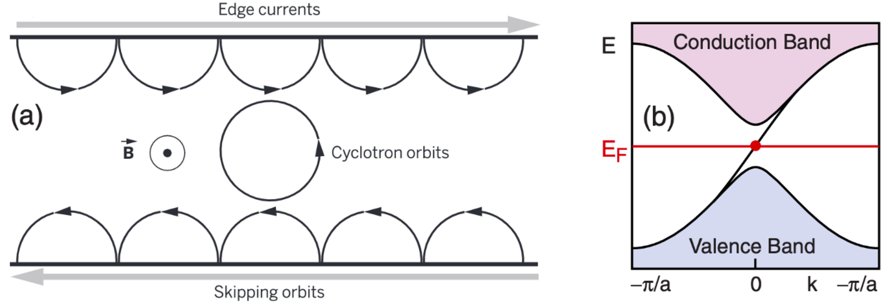

Figure 2.1: **a.** An above view of carrier dynamics within a sample in response to the out-of-plane applied magnetic field, $\vec{B}$. Skipping cyclotron orbits are illustrated at the sample edges, which constitute an edge current on either side. Reproduced from Ref. [1]. **b.** A depiction of the band gap of an IQH insulator, with the bridging edge state and E_F indicated. Reproduced from Ref. [2].

As well as low temperatures and a high magnetic field, the visibility of the IQHE also depends on the presence of impurity scattering. Specifically, $\hbar\omega_\mathrm{c} \gg k_BT$, such that thermal energy does not allow crossing of LLs, and $\hbar\omega_\mathrm{c} \gg \frac{\hbar}{\tau_\mathrm{t}}$, where τ_t is the transport scattering time. This is more commonly expressed as $\omega_\mathrm{c}\tau_\mathrm{t} \gg 1$, meaning that electrons must complete many cyclotron orbits before a scattering event occurs. As $\omega_\mathrm{c}\tau_t = \mu B$, where μ is the carrier mobility, the minimum required B can be estimated by the inverse mobility.

In the bulk, this renders the material an insulator, depicted in Fig. 2.1a, where the bulk electrons complete closed orbits. However, on the edge of a sample, the orbits are incomplete and skip along the edges. This skipping orbit forms a 1D spinless, dissipationless (zero resistance) edge conduction channel, whose chirality depends on the cyclotron orbit direction, generated by the B-field polarity.

Figure 2.2a shows an energy vs. density of states representation of LLs, with broadened distributions centred on filling factors. The Fermi level is also shown, which will pass through successive LLs as an increasing B-field is applied. This is because E_F remains fixed, whilst LLs become more energetically distant in proportion with B. Therefore, when increasing B, we are essentially scanning LLs through a stationary E_F. Each time E_F passes through a LL, the density of states peaks.

The application of the out-of-plane magnetic field establishes the cyclotron motion and Landau quantisation, but the system requires the application of a current to observe the resistance/conductance signatures of the quantisation. Assuming device dimensions of $L_x \times L_y$ and applying the current along L_x, this yields signatures in both the longitudinal (σ_{xx}, along L_x) and transverse (σ_{xy}, along L_y) conductivities. When ν is an integer, E_F is between LLs. This means that the bulk carriers are confined to closed orbits and there are no available states for transport. In the edge regime, there are ν ballistic conduction channels. As the edge transport is dissipationless, it

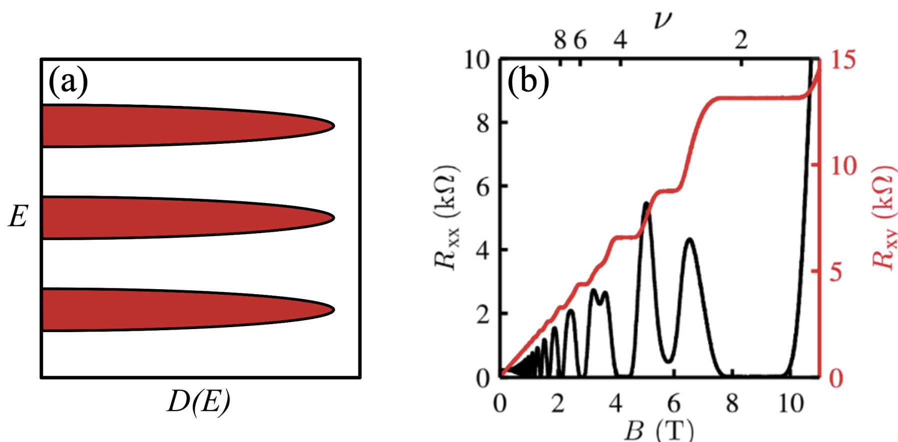

Figure 2.2: **a.** LL occupation in energy (E) against density of states ($D(E)$). Disorder broadens the dispersion from discrete levels. **b.** An example of the longitudinal and Hall response to a varying magnetic field, exhibiting SdH oscillations and the IQHE. At lower fields, the LL spacing has not exceeded the disorder broadening, which is why the longitudinal signal does not reach 0 initially. Zeeman splitting is also present at $B \approx 3.5$ T and $B \approx 6$ T. Panel (b) adapted from Ref. [3].

corresponds to zero resistance ($R_{xx} = 0$) and so a conductivity spike. An example resistance measurement is shown in the graph in Fig. 2.2b.

In the Hall direction (σ_{xy}), there is a constant number (ν) of propagating edge carriers, meaning a constant conductivity. This manifests as plateaux in Hall resistance, R_{xy}, also shown in Fig. 2.2b. R_{xy} is quantised to $\frac{h}{e^2}\frac{1}{\nu}$, where $\frac{h}{e^2}$ is referred to as the von Klitzing constant, R_{K}.

When ν is not an integer, E_{F} is crossing a LL. At this point, there is a surge in availability of bulk conduction states. This corresponds to an increase in R_{xx}, as there is a significant scattering contribution, matched with a steady increase in R_{xy} as the system transitions to the next quantised state. These concurrent resistance signatures can also be seen in the conductivity tensor,

$$\sigma = \begin{pmatrix} \sigma_{xx} & \sigma_{xy} \\ -\sigma_{xy} & \sigma_{xx} \end{pmatrix} = \rho^{-1}, \tag{2.9}$$

which describes the conductivity under a perpendicular B-field. Superficially, this implies that zero bulk conduction occurs simultaneously with zero resistance/dissipation, which appears contradictory. However, as $\rho_{xx} = \frac{\sigma_{xx}}{\sigma_{xx}^2+\sigma_{xy}^2}$, $\rho_{xx} = \sigma_{xx} = 0$ is permitted, provided there is a non-zero transverse conductivity. The oscillatory longitudinal resistance in response to the shifting LLs is periodic in B^{-1}. This is visible in Fig. 2.2b, and is termed the SdH effect.

Whilst the IQHE can be largely considered as spinless, at high fields ($>$ 6.4 T for the QW structure used for this thesis) the spin-degenerate LLs are Zeeman split, by

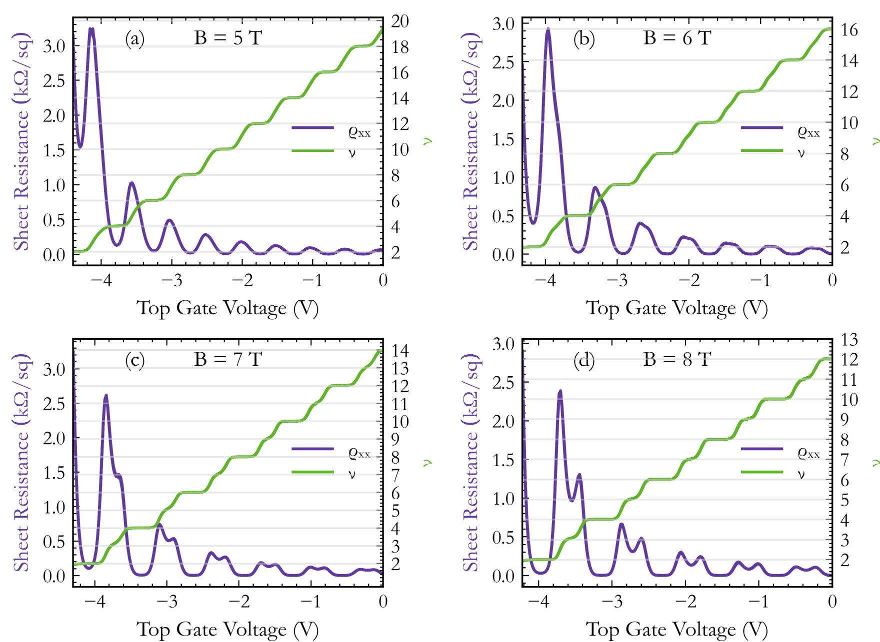

Figure 2.3: My own measurements (of the Hall bar device used in Chapter 4) showing the resolution of Zeeman-split peaks/plateaux at high magnetic fields, measured at 1.7 K. They consist of top gate voltage sweeps at constant magnetic field, with field values of 5 T (**a.**), 6 T (**b.**), 7 T (**c.**) and 8 T (**d.**). **c.** and **d.** show clear Zeeman splitting in the SdH peaks and IQH plateaux. **b.** shows signs of Zeeman splitting, however they are not clearly resolved, and **a.** shows no Zeeman splitting.

$\Delta = g\mu_B B$, where g is the Landé g-factor and μ_B is the Bohr magneton. Signs of this Zeeman splitting resolving are present in Fig. 2.2b. Due to the maximum B-field in this thesis being 8 T, the passing of this threshold can be more easily seen by sweeping a gate voltage at a constant field, which is similar to the measurement in Fig. 2.2b, but E_F is being swept through LLs, rather than LLs being shifted over E_F. Figure 2.3 shows this measurement for the device featured in Chapter 4, at 5 T to 8 T. The 5 T and 6 T signals show only single peaks in the longitudinal signal, and the Hall plateaux are visible on the spin degenerate even filling factors. On the other hand, at maximum field, every peak shows signs of splitting, and the Hall signal is resolving odd filling factors.

2.1.2 The Quantum Spin Hall Effect

The QSHE stems from the development of the IQHE theory, and is relevant to this thesis owing to its potential observation in the inverted band structure of InAs/GaSb QWs. Chapters 5 and 6 tell of the fabrication and optimisation of InAs/GaSb devices with integrated FM contacts, which offer the possibility of observing the spin-momentum locked edge channels characteristic of the QSHE. Therefore, a brief summary is presented.

The discovery of the IQHE led to the 1988 Haldane model [20], a 'toy model' derived from the chiral nature of the IQHE, which serves as a useful bridge between the theory of the IQHE and the QSHE. In short, the model sought to explore the quantum Hall effect without the existence of LLs, meaning no external magnetic field. In the context of symmetry breaking, the IQHE arises from the breaking of time-reversal ($\mathcal{T}$) symmetry by the large magnetic field. In short, this ensures its non-zero Chern number, which topologically classifies its quantised states. As Haldane's model lacked LLs, one would naturally expect a lack of $\mathcal{T}$ symmetry breaking. However, Haldane determined that some $\mathcal{T}$ symmetry breaking was still required, instead employing the intrinsic $\mathcal{T}$ symmetry breaking of the band structure in honeycomb, graphene-like lattices [21]. This model understandably influenced the first prediction of the QSHE, on graphene lattices in the absence of an applied magnetic field [11]. Thus, the QSHE effect is often described as two conjugate copies of the Haldane model (for spin-up and spin-down), but with the distinction that $\mathcal{T}$ symmetry is preserved.

As the QSHE lacks an external magnetic field, the effect is an intrinsic result of the material band structure. In the IQHE, topological conducting edge states cross the bulk insulating band gap. These quantised states are topologically protected by the fact that they cannot be altered without closing the bulk insulating gap. The QSHE describes conducting edge states that bridge a so-called inverted band gap, which is topologically non-trivial. Its inverted property comes from the relative positions of the highest valence band and lowest conduction band in the material, where the valence band lies above the conduction band on the energy scale. Combined with spin-orbit coupling, this leads to the opening of a new insulating gap. This is illustrated in Fig. 2.4. Panel (a) shows the band alignment in which the AlSb wide band gap confines the carriers

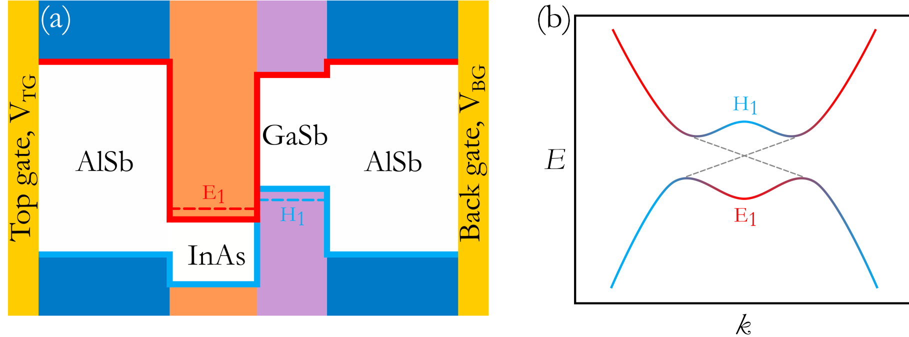

Figure 2.4: **a.** Band gap diagram for an InAs/GaSb QW with AlSb barriers, showing the broken gap alignment. The first InAs electron state (E_1) and first GaSb hole state (H_1) are shown. The top and back gates are also visualised. **b.** The band dispersion relation where E is the energy and k is the wave vector. The conduction band adopts a hole-like dispersion and the valence band adopts an electron-like dispersion. The edge conducting states are indicated with grey dashed lines.

within the InAs and GaSb QWs. The band gaps of InAs and GaSb form a broken gap alignment, where the bottom of the conduction band in InAs overlaps the top of the valence band in GaSb. Panel (b) shows the band inversion. High in the conduction band, the dispersion relation is parabolic. With decreasing k, the wave vector, the conduction band adopts a hole-like dispersion. Likewise, the valence band acquires an electron-like dispersion. This is a consequence of electron-hole hybridisation. The gap opens due to the process of avoided crossing, with hybridised states of equal energy repelling one another.

The intrinsic spin-orbit coupling of the material is the cause of band inversion. Relativistic electrons orbiting a nucleus generate a magnetic field in two ways - through their spin moment and orbital moment. In the rest frame of an electron, the stationary electric field through which it is orbiting is perceived as an effective magnetic field, which is proportional to the electric field and the electron's orbital velocity. The effective magnetic field generated by this orbital motion interacts with the spin magnetic moment. This coupling is termed spin-orbit coupling, and the opposing spin directions involved in the coupling lift spin degeneracy in the band structure, which can promote band inversion.

Similarly to the IQHE, this inverted bulk insulating band gap is bridged by edge conducting states. Due to the spin-orbit coupling, carriers of opposing spin experience effective opposing magnetic fields, causing spin-up carriers to propagate in the opposite direction to spin-down. This is called spin-momentum locking, and leads to a key transport feature called helicity. As spin-up electrons are locked to one direction and spin-down locked to the opposite direction, the carrier motion propagates akin to two conjugate chiral channels, such as those in the IQHE/Haldane model. This leads to a net charge Hall conductivity of zero, but a net spin Hall conductivity that is non-

zero and quantised. As there are two counter-propagating channels, the conductivity is quantised to $2e^2/h$. In the absence of magnetic impurities, which break $\mathcal{T}$ symmetry, they are helical channels of ballistic transport. $\mathcal{T}$ symmetry must be preserved, and a backscattering event requires a spin-flip, which violates this.

The effect was first theorised in 2005, by Kane and Mele [22], and Bernevig and Zhang [12] simultaneously. Neither theory has been experimentally realised since, presumed to be due to insufficient spin-orbit coupling strength to promote band inversion. This led to the prediction of the QSHE in HgTe QWs by Bernevig, Hughes and Zhang in 2006 [23], which was verified by König in 2008 [24]. This was shown in a CdTe/HgTe/CdTe QW, where HgTe thicknesses above a threshold of 6.3 nm lead to an inverted band gap.

Since then, InAs/GaSb QWs have been proposed as a candidate material [13], although there have been conflicting reports on its verification [14, 25]. Section 2.2 below discusses why this system is of particular interest.

2.2 InAs/GaSb Coupled Quantum Wells

2.2.1 Band Structure and Gate Tuning

The QW structure used throughout this thesis consists of 12.5 nm/8 nm InAs/ GaSb layers situated between two 50 nm AlSb QW barriers. Figure 2.4 showed an example band gap arrangement along the layers of an InAs/GaSb QW. As expected, the AlSb barrier layers have the largest band gap, confining carriers to the InAs QW and GaSb QW layers. The interesting quality about InAs/GaSb QWs is the relative band alignment of the heterojunction. As shown in Fig. 2.4a, for the right InAs and GaSb layer thicknesses, they possess a broken-gap band alignment. This is an inverted band structure produced by the inversion of the bottom of the InAs conduction band with the top of the GaSb valence band. This produces a hybridised band gap, where the wave functions of the electron-like states in the InAs and hole-like states in the GaSb mix, which could support a QSH state.

This system is more attractive than the previous HgTe system, crucially because the band inversion is provided by two different materials. Whilst both systems require a specific range of QW thicknesses to achieve the necessary extent of band crossing, the band inversion in InAs/GaSb QWs can also be controlled in-situ. The presence of two materials means that gating to alter carrier densities via the field effect can be employed to shift the relative position of the InAs conduction band and GaSb valence band, allowing precise tunable control of the band inversion. For particular combinations of top and back gate voltages, the topologically protected inverted state can be induced or destroyed at will.

Tunability is useful for accessing the QSH state, as it negates the vulnerability of a QW thickness-based system to defects. There is only a small window of band inversion for which the QSHE can be measured (only a few meV [4, 14]), as too much inversion can re-introduce significant bulk interference.

As well as making the topological state easier to access, the gate tunability is also promising for future device applications, such as easy switching between the inverted and non-inverted state in proposed 'topological field-effect transistors' [26]. Additionally, InAs/GaSb belongs to the well-established III-V semiconductor family, and is routinely grown to high precision by molecular beam epitaxy (MBE).

This dual gating system is represented again in Fig. 2.5a, with the precise material and fabrication details provided in Chapter 3. Applying a gate voltage introduces an electric field across the structure. Depending on the polarity of the gate voltage, the field can alter the electrostatic potential within each QW. A negative top gate voltage in this QW structure reduces the electron density, which raises the conduction band of InAs. A negative gate voltage would also lower the valence band of GaSb, however, the response from the electrons in the separate InAs layer screens the top gate's effect from the GaSb layer. For this reason, the back gate is employed to provide control over the hole population in GaSb, which in turn screens that gate's effect from the InAs [27]. In practice, this effect is not perfect and the screening is partial [28].

The band inversion landscape accessed by dual gate tuning is shown in Fig. 2.5. Panels (b) and (c) show how the top and back gate voltages can be scanned to shift the Fermi level position and access different degrees of band inversion. Applying different voltages to the two gates sets up a vertical electric field across the heterostructure, E_z. This shifts the conduction and valence bands in relation to one another, corresponding to scanning horizontally across panel (b). Applying the same voltage to the two gates allows E_{F} to be scanned, corresponding to the vertical direction in panel (b). The charge neutral region corresponds to points B, E and H in the phase diagram, where the Fermi level lies within the bulk insulating gap, which occurs for both the trivial and topological case.

2.2.2 Motivation

Following its prediction by Liu et al. in 2008 [13], the initial observation of the QSHE in InAs/GaSb was made by Knez et al. in 2011 [14], when they demonstrated quantised, dimension-independent transport separate to residual bulk conduction. The quantised conductance was then confirmed to reside in the sample edge via asymmetric current path measurements [29]. Despite multiple claims of observing the QSHE in InAs/GaSb coupled QWs, there exists no direct proof of the spin-momentum locked transport in the helical edge states. Without direct confirmation of spin-momentum locking, the helical property is only confirmed by inference from the edge conductance quantisation. This is in contrast to the status of HgTe/CdTe experiments, where spin-dependent edge transport was detected by employing HgTe's intrinsic spin Hall effect as a spin current detector [30]. For this reason, the aim of this project is to fabricate InAs/GaSb coupled QW devices with FM contacts attached to the edge regime, as this type of junction is promising for future experiments measuring the spin-momentum locked edge transport. This junction is the focus of Chapters 5 and 6. The carrier region approaching charge neutrality has also been extensively studied in Chapter 4. Before this, the main device

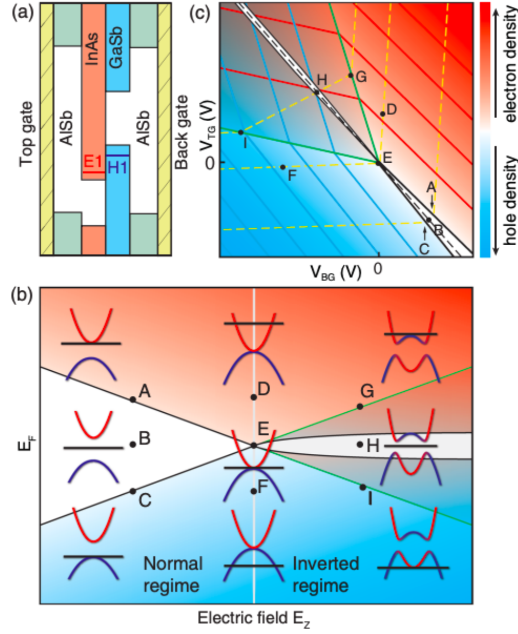

Figure 2.5: **a.** The simplified QW band structure, with the InAs electron QW and GaSb hole QW between the AlSb barrier layers. The band inversion is also indicated, marked by E1, the lowest occupied state of the conduction band, and H1, the top state of the valence band. **b.** The phase diagram with respect to the electric field, E_z, and the Fermi level, E_{F}, altered by the application of top and back gate voltages. The band diagram corresponding to each zone is indicated, where the red area is in the electron regime, the blue area is in the hole regime, and the white area is in the charge neutral regime. The white line in the centre indicates the transition from the normal to the inverted regime (i.e., the topologically trivial to non-trivial insulating phase). H is the point of interest, where the Fermi level is situated within the inverted band gap. **c.** The phase diagram with respect to V_{BG}, the applied back gate voltage, and V_{TG}, the applied top gate voltage. The same crucial points are indicated, where the top left charge neutral gap is topologically non-trivial, and that of the bottom right is trivial. The blue and red lines signify constant electron and hole densities respectively. The yellow dashed lines indicate constant band separation (or constant band overlap in the inverted regime). The black dashed line indicates charge neutrality, whilst the green line encases the region in which only one carrier type is present. Reproduced from Ref. [4].

fabrication process is given, which primarily concerns the InAs/GaSb QW Hall bar device featured in Chapter 4. It is presented as a standard process, and any deviations from this process to construct the devices featured in Chapters 5 and 6 are clearly outlined and discussed in those respective chapters.

Chapter 3

Fabrication Techniques

This chapter introduces crucial concepts regarding device fabrication throughout this thesis, in the context of the fabrication process for the Hall bar device featured in Chapter 4. The subsequent device fabrications in Chapters 5 and 6 are treated with this initial process as a reference. The general MBE-grown wafer structures used for every device are also introduced in this chapter. The complete, reproducible device processing methods for all device types used are given in the Appendices.

3.1 Wafer Growth and Structure

3.1.1 Molecular Beam Epitaxy Process

The QW structures featured in this thesis were grown by MBE by Dr Lianhe Li, School of Electronic and Electrical Engineering, University of Leeds. MBE is a precise growth technique by which monolayer films of atoms are deposited at a slow rate (200 - 700 nm per hour for this QW) onto a heated substrate under ultra-high vacuum conditions. The structure grows epitaxially, which means that the atomic arrangement of a layer matches the crystal orientation of the previous layer.

When changing materials, it is important to consider the lattice constants of each material in the stack, as significant mismatch will introduce strain (affecting quantum confinement conditions in the layers of interest and possibly introducing defects). Devices were fabricated using a variety of wafer structures. The preferred structure, given below in Section 3.1.2, contains one or more InAs, GaSb, AlSb and $AlAs_{0.029}Sb_{0.971}$ layers. InAs, GaSb and AlSb are of zinc-blende crystal structure and have lattice constants around 6.1 Å [31, 32]. Applying Vegard's law [33] to the 300 K lattice constants of AlAs and AlSb [32] with the $AlAs_{0.029}Sb_{0.971}$ composition also gives a lattice constant of 6.1 Å.

The interface type between layers can be controlled by the method of transition between differing layers. This is of particular importance at the InAs/GaSb interface, as different methods will introduce different extents of strain. In turn, this affects the likelihood of defects, as well as the mobility, which influences visibility of magnetic field dependent SdH oscillations. Here, an In-Sb interface was grown, by running Sb only, once the 8 nm GaSb layer was complete, followed by In only, before beginning the 12.5 nm InAs layer. This has demonstrated better crystallographic order than Ga-As like interfaces [34].

The MBE process involves heating the required elements/molecules, which are situated in individual crucibles, to produce a beam directed towards a substrate. The ultra-high vacuum conditions prevent collisions of the intended atoms/molecules with those in air. The heating of the substrate ensures that incident atoms/molecules have enough mobility to arrange themselves according to the substrate lattice.

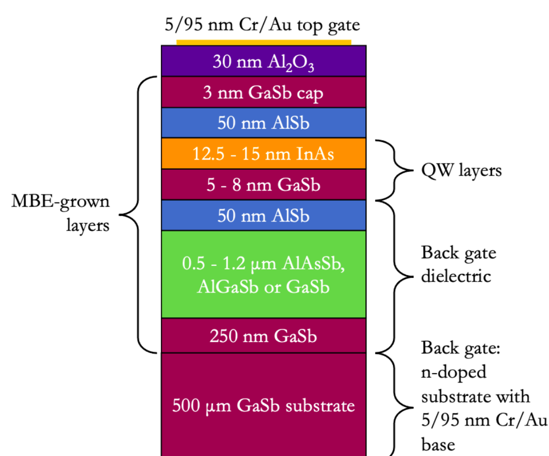

Figure 3.1: General wafer structure, where QW layer thicknesses vary, along with buffer layer type and thickness. A variety of combinations were fabricated and tested to assess which harboured the lowest carrier density. The uppermost MBE-grown layer is the GaSb cap, which covers the QWs, which are sandwiched between two AlSb barriers. The MBE layers are grown on a highly n-doped GaSb substrate, allowing it to act as a back gate, whilst the layers between the GaSb and the conducting QW channel act as the gate dielectric. The purpose of the additional layer of GaSb above the substrate is to smooth the surface before deposition. The top gate is formed during device fabrication, with 30 nm Al_2O_3 deposited by atomic layer deposition and 5 nm/95 nm Cr/Au thermally evaporated to form the top gate electrode. An additional layer of 5 nm/95 nm Cr/Au is also thermally evaporated onto the base.

3.1.2 Wafer Structure

As previously mentioned, this thesis concerns a QW stack structure containing 12.5 nm InAs and 8 nm GaSb, sandwiched between AlSb QW barrier layers of 50 nm. This structure, complete with the remaining layers, is shown in Fig. 3.1. The design was inspired by the GaSb substrate structure in Ref. [35], with the AlAsSb and AlGaSb substrates added by Dr Lianhe Li, School of Electronic and Electrical Engineering, University of Leeds. The diagram also shows the 30 nm Al_2O_3 gate dielectric layer and Cr/Au top and back gate electrodes, which were fabricated by myself after the wafer structure had been grown. This fabrication is discussed in Section 3.2.

In terms of the MBE growth, it begins with a 500 µm GaSb substrate. Above this, a further 250 nm GaSb is grown to level out possible manufacturing defects. The substrate is highly n-doped so that it can act as a back gate.

To reduce the effects of lattice mismatch and insulate this back gate from the active QW layers, a buffer layer is grown. To select this buffer layer and 12.5 nm InAs/8 nm GaSb QW ratio, transport measurements were performed on a variety of QW buffer layer compositions (0.5 - 1.2 µm AlAsSb, AlGaSb and GaSb), along with varying QW thickness ratios (12.5 - 15 nm InAs and 5 - 8 nm GaSb), to determine which combination was most capable of crossing the charge neutral regime. The active QW layers encased in the AlSb barrier layers are situated above this, with a final 3 nm GaSb cap grown on top to protect the layer below from oxidation.

The two main desirable features in the prospective optimal wafers were a low carrier density (meaning less gate voltage driving of carrier density would be required to reach charge neutrality) and a resistance to gate leakage at higher voltages. Defects in the dielectric between a gate and the QW channel can allow leakage currents to diffuse, via pinhole sites. The objective was to establish a device capable of reaching charge neutrality before dielectric breakdown of either gate. Many devices were tested due to the random nature of pinhole defects.

3.2 Dual Gated Hall Bar Device Fabrication

This section will outline the fabrication method for the micron-scale Hall bar device featured in Chapter 4. This method introduces fabrication concepts that are fundamental throughout this thesis, and the fabrication methods for later devices were formulated with this original method as a reference. Therefore, this standard method is presented here on its own, and the modifications to the procedure to produce the devices featured in Chapters 5 and 6 are addressed in their respective chapters, along with their patterns. Appendix A.1 contains the comprehensive instructions corresponding to the methods presented here.

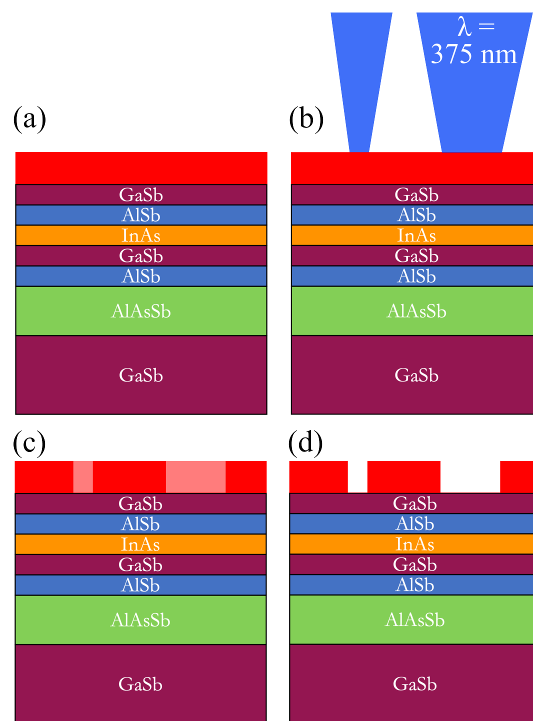

Figure 3.2: **a.** S1805 positive photoresist is deposited. **b.** 375 nm UV light is applied by MLA. **c.** The exposed resist is now soluble in the appropriate photoresist developer. **d.** After developing, resist remains only in the areas in which the layers are to be preserved.

3.2.1 Photolithography Process

The first step of fabricating a complete dual gated Hall bar device from a QW wafer is forming the mesa, which consists of the principal Hall bar channels. The channels are composed of the InAs/GaSb QW, the QW barriers and tens of nm of the insulating buffer layer to isolate the conducting channel. This mesa is formed by chemically wet etching into the MBE-grown wafer, to remove the excess material that will not form the mesa. The chosen pattern to etch is defined by photolithography. For this particular device, the pattern was designed using KLayout [9] by Dr Mark Rosamond, Leeds Nanotechnology Cleanroom, University of Leeds. The Hall bar dimensions are 750 μm × 50 μm, as a varied range of Hall bar dimensions was patterned and the particular device with these dimensions demonstrated the best charge neutrality-reaching capabilities. This means a central channel 750 μm in length, with a Hall probe separation of 50 μm. The device contains 8 contacts, with 3 longitudinal contacts on each side at 250 μm separation, and 2 contacts at either end of the main channel. The device geometry is explained further in Section 4.2.2.

Figure 3.2 outlines the basic mesa patterning steps. The photolithography process involves first coating the surface of the clean wafer in a thin layer of S1805 positive photoresist (from the Microposit S1800 Series Photo Resists).

A photoresist is a substance primarily composed of a solvent, a photosensitive polymer resin, and a sensitiser. It contains a solvent to allow it to be spun onto a substrate (at 3000 rpm for this S1805 process) to produce a thin, even layer. The sample is then soft-baked on a relatively low heat (115 °C for S1805) to remove the solvent and harden the photoresist. Fig. 3.2a corresponds to this stage.

Regarding the exposure step, which defines the intended device pattern, there are two main types of photoresist: positive and negative. Positive photoresist (like S1805 used here) becomes highly soluble in a specified developer substance in areas exposed to a particular wavelength of light, whilst unexposed areas (typically those concealed under a mask) retain their original solubility, which is far less than that of the exposed area. Negative photoresist follows the opposite principle, where the photoresist is soluble to begin with, drastically decreasing in solubility in the areas that are exposed to light. In that case, the mask is the inverse of the intended pattern.

The positive resist exposure process here is shown in panels (b) and (c) in Fig. 3.2. For this process in particular, the 375 nm ultra-violet (UV) exposure was performed using a Heidelberg Instruments MLA 150 Advanced Maskless Aligner (MLA). Maskless here refers to the lack of a physical mask to block exposure to certain areas of the photoresist, instead replicating the effect by dividing the sample into a series of exposed or unexposed cells, following a digital pattern input. This is the preferred method when testing a variety of patterns, as fabrication of a new physical mask is not required for each pattern.

Upon exposure, the photosensitiser component of the photoresist absorbs photons of a specified wavelength and breaks down to produce reactive products, such as free radicals. These products decompose the resin, making it more soluble in a given developer

(as opposed to promoting cross-linking in the resin molecules in negative photoresists).

After the exposure, the sample is soaked in a developing solution. The composition of said solution, along with the soaking time, is specific to the photoresist used. Deionised (DI) H_2O:Microposit 351 Developer 3.5:1 was used here. This developer dissolves the areas of the photoresist coating that were rendered highly soluble. In certain cases, including here, the developer may also attack materials found in the wafer. If the reactive layer is situated within the wafer (not on the top or bottom surfaces) or very thick, this is not an issue, as exposure is limited by the fact that development times are relatively short.

In this process, the developer attacks GaSb and AlSb. These layers, amongst others, will be eventually completely dissolved in the subsequent wet etch process, meaning the loss of a particular layer is not harmful in itself. However, if the developer is going to attack material layers, it is important that this occurs uniformly. Specifically, the surface to be etched needs to be composed of the same material (no residue of other materials), so that wet etch occurs more consistently across the sample. Ordinarily, the time spent in the developer solution is determined by the compromise between clearing the soluble resist, whilst not over-developing to begin attacking the outer edges of the unexposed (less soluble) area, as this limits resolution. In this instance, there was an additional condition of fully clearing the GaSb cap layer to produce a uniform AlSb surface, without excessively attacking the AlSb barrier. This was due to problems caused by residual GaSb at the wet etch stage, discussed in Section 3.2.2.

The optimal developing time to satisfy these conditions was 60 s. Devices developed for less than 50 s produced an uneven surface, where parts of the GaSb cap layer remained. Said devices did not prove satisfactory for use in transport measurements, due to highly inconsistent etch results causing electrical shorts across device components. Developing times exceeding 60 s etched needlessly far into the AlSb barrier, and compromised the resolution.

After the developing stage, there is the possibility for a hard-bake. This is a secondary bake at a higher temperature or longer duration to further adhere the photoresist to the sample surface, in the event that a strong etch solution could begin to lift the photoresist coating. Whilst this was not necessary for this particular process, this step is implemented in later devices. Figure 3.2d shows a schematic of the finished photoresist coating.

3.2.2 Wet Chemical Etching

The next stage is to soak the sample in a wet etch solution, which will gradually remove areas that are not protected by photoresist. It is worth noting that the photoresist contains an adhesion promoting component, to prevent delamination during the wet etch process. This component is generally optimal for Si substrates. For sample surface materials other than Si, it is recommended to prime the surface before depositing photoresist for improved adhesion. Here, SurPass 4000 adhesion promoter was used immediately before the photoresist was deposited, also by spin coating at 3000 rpm,

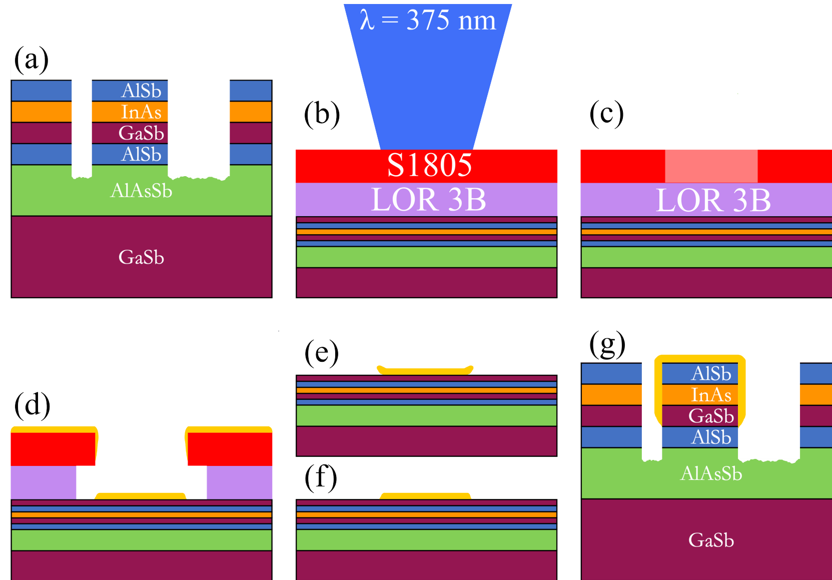

Figure 3.3: **a.** The result after etching. It is shown without the GaSb cap, due to its solubility in the developer solution. **b.** The result of the etch is approximated as a flat surface for the sake of the lithography explanation. The lift-off resist is deposited, followed by the usual S1805 positive photoresist. The photoresist is exposed with the same light as for the mesa patterning, exposing the areas on which the ohmic contacts are deposited. **c.** The exposed areas in the S1805 become more soluble. **d.** The resist is developed, which removes the soluble areas of the S1805, and the lift-off resist below. The lift-off resist dissolves faster than the S1805, leading to an undercut. This undercut creates a discontinuity in the subsequent metal deposition. The metal is then deposited by thermal evaporation. **e.** The lift-off result for single-layer resist processes. The lack of undercut leaves 'wings' at the edges of the metal layer. **f.** The lift-off result for a bilayer resist process, with clean edges. **h.** The thickness of the metal evaporation is such that the ohmic contact is able to connect to the conducting channel via the edges of the mesa.

followed by an isopropyl alcohol (IPA) jet in the final 20 sec of the spin. This creates a cationic monolayer on the sample surface, which reduces the effect of electrostatic imperfections and strongly bonds to the organic photoresist molecules. This lessens the likelihood of delamination during the wet etch process, leading to more successful wet etch results.

For this wet etch process, an etchant comprising citric acid, hydrogen peroxide, phosphoric acid and DI water was used; a combination capable of attacking all layers within the wafer. The sample remained in the etch solution until it had etched down to the insulating buffer layer, so that what remained was a series of Hall bars composed of the isolated QW layers (after cleaning the photoresist in acetone). Etch depths were tracked by removing samples every 3 to 5 minutes and measuring the offset of the top of the resist to the bottom of the etched area with a KLA-Tecnor Alpha-Step IQ Surface Profilometer. As the Hall bar mesa must contain the conducting QW channel, etch depths of 180-200 nm were aimed for, to ensure conduction was confined to the desired geometry. To achieve this depth, a total etch time of $\sim$ 13 min was required. Upon testing other wafer compositions, it became clear that over-etching or salt formation (causing net under-etching) was possible. This is explained further in Section 3.2.5. Due to this risk, the gradual etching technique remained a part of the standard procedure throughout every fabrication in this thesis. This is because under-etching risks unwanted conductive material residue that can cause shorts, and over-etching can compromise the structural integrity of the top gate electrode once it is deposited. See Fig. 3.3a for the etch result schematic.

3.2.3 Bilayer Photolithography Process and Ohmic Contact Metallisation

Once the basic Hall bar channels had been constructed, ohmic contacts for measurements were fabricated. 5 nm Cr (for adhesion purposes) and 95 nm Au are thermally evaporated onto the areas indicated in Fig. 3.3, using an Edwards Auto306 Thermal Evaporator. There is sufficient metal coverage to bridge a connection to the conducting channel below (see Fig. 3.3g). The patterning is performed by photolithography again, this time using a bilayer lift-off method.

Metal is evaporated uniformly across the sample surface, adhering to the areas which are not coated in photoresist. Whilst this process can be completed with a single photoresist layer, similarly to the previous S1805 process, the edge definition of the metallic pattern is greatly improved by the implementation of a bilayer process. This process consists of an initial lift-off resist layer, followed by the usual S1805 photoresist layer. This is shown in Fig. 3.3b. The lift-off resist used here is MicroChem LOR Lift-Off Resist 3B (deposited at 3000 rpm). The S1805 photosensitive layer is exposed by 375 nm light again, and the lift-off resist layer below is soluble in the same developer. Given the appropriate developing time, the exposed photoresist dissolves, followed by the lift-off resist directly below (Fig. 3.3c and d). Ideally, the area of lift-off resist dissolved is slightly larger than that of the photoresist (by tens of nm), due to the

increased solubility of the lift-off resist. This additional area is referred to as the undercut.

Thermal evaporation involves placing the material to be deposited in a crucible through which a current is applied to resistively heat the material to vaporisation. This is performed under high vacuum to ensure the metal atoms reach the target substrate without being scattered by air molecules.

During the thermal evaporation, Cr and Au are uniformly evaporated over the entire top of the sample. How this coverage applies to the ohmic contacts is depicted in Fig. 3.3e and f, for single-layer and bilayer resist processes respectively. The undercut beneath the photoresist in the bilayer process causes discontinuities in the metal layer deposited above. With the application of a resist stripper, the excess metal and resist layers are stripped from the entire sample, leaving behind ohmic contacts with a smoother edge finish than if they were formed by a single layer photolithography process. Fig. 3.3g shows the finished result, where the thickness of the Au evaporation, is sufficient to cover the sides of the mesa to make contact with the QW channel, confirmed by continuity measurements across the Cr/Au top gate electrode (in the following step), which is of identical thickness. Every contact edge also extends beyond the mesa boundary by 4 - 5 μm.

3.2.4 Top and Back Gating

As the back gate is already built into the wafer structure, a simple 5 nm Cr and 95 nm Au uniform thermal evaporation onto the back of the sample was sufficient. This approach has proven statistically more reliable than applying silver paint directly to the substrate for measurement purposes [15]. The top gate requires the deposition of a dielectric on the top of the sample, followed by the gate electrode and connected contact pads (Cr/Au 5 nm/95 nm). A 30 nm Al_2O_3 dielectric layer was formed by atomic layer deposition (ALD) using a Veeco Fiji 200 ALD System, and the 5 nm/95 m Cr/Au top gate was thermally evaporated.

ALD is a highly controlled method of deposition, capable of producing uniform near-monolayer films. In brief, it is performed by exposing a vacuum chamber containing the substrate to a cycle of ‘precursor’ gases and ‘purge’ processes. The precursor gases react with the sample surface in a self-limiting reaction, depositing the relevant layer of atoms, and the purge process employs argon to pump the chamber clear of by-products. In the case of Al_2O_3, the precursors are water vapour and trimethylaluminium ($Al(CH_3)_3$). The $Al(CH_3)_3$ reacts with surface hydroxyl groups to form O-$Al(CH_3)_2$, with a CH_4 by-product (which is pumped way during the purge). The water vapour is then introduced, which replaces the -CH_3 bonds with -OH, completing the cycle with another by-product CH_4 purge.

The photolithography patterning was a bilayer process again, owing to the sensitivity of Al_2O_3 to the resist developer. The steps are outlined in Fig. 3.4. A layer of Poly(Methyl Meth-Acrylate) (PMMA) resist (specifically PMMA 495K A8) was deposited before the photoresist to protect this dielectric layer. The standard 375 nm

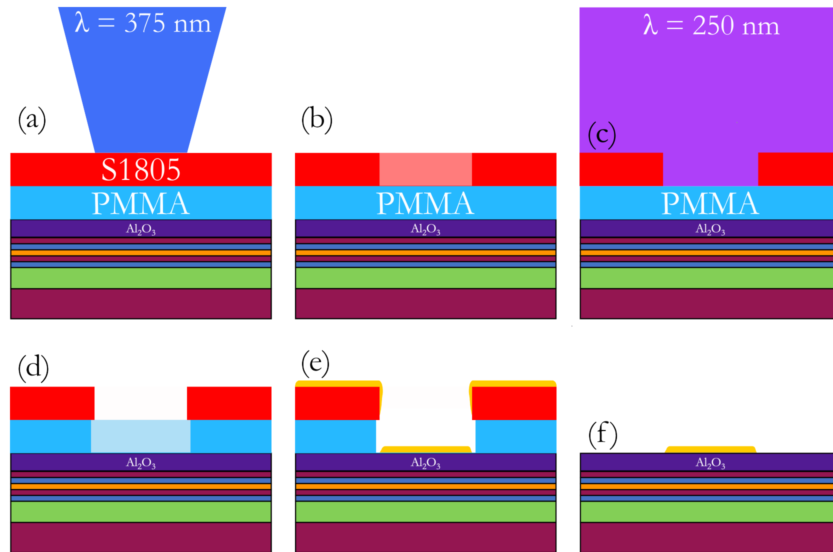

Figure 3.4: **a.** Approximating the sample as a flat surface again, 30 nm Al_2O_3 dielectric is deposited by ALD. PMMA and S1805 bilayer resist coats are deposited, followed by the usual photoresist exposure of 375 nm light. **b.** The upper photoresist is exposed. **c.** This dissolves in the developer as usual, and the PMMA is insoluble in the developer, protecting the dielectric layer from the photoresist developer. Upon exposure to the 250 nm UV light, the upper intact layer of photoresist acts as a mask, as it is not reactive to light of this wavelength. **d.** The PMMA is exposed and now soluble in its own particular developer, a solution of DI water and IPA. **e.** The resist profile resulting from the developer. 5 nm Cr and 95 nm Au are thermally evaporated onto the sample surface. **f.** After stripping both resist layers, the metallic top gate remains. The dielectric layer covering the ohmic contacts below is not an issue, as the wire bonding method used to connect to the contacts will break through the top gate dielectric and make contact.

exposure and develop was completed, leaving the top gate pattern cut into the top layer of resist (Fig. 3.4a to c). This also exposes the PMMA layer, however, it remains intact due to not being photosensitive to 375 nm light, nor dissolvable in MF351 developer. This ensured protection of the dielectric layer, but the subsequent thermal evaporation stage required that the PMMA layer be cleared in order to deposit Cr/Au onto the Al_2O_3. The PMMA is reactive to 250 nm light, which was administered by UVO (UV-Ozone)-Cleaner to clear the PMMA layer. In this instance, the upper S1805 resist layer acts as the mask, and does not react to the 250 nm light nor the developer specific to the PMMA (Fig. 3.4d). Once the PMMA layer had been developed (in IPA:$H_2$0 7:3), the previous thermal evaporation and lift-off technique (in acetone) was completed, leaving the result in Fig. 3.4f. The finished samples were scribed (with a JFP Microtechnic S100 Scriber) and diced into roughly 3 mm $\times$ 3 mm chips.

3.2.5 Complications

This method has undergone considerable refinement over time to achieve its current standard, nevertheless, there continued to be pitfalls in the earlier fabrication stages, which must be acknowledged. As mentioned in Section 3.2.1, issues with the partial development of the GaSb cap along with exposed resist meant an optimal developing time needed to be determined, separate to a standard time for that photoresist/developer combination. If GaSb cap residue had been left on the surface, this would take a significantly longer time to wet etch than subsequent layers (beyond the time taken to achieve desired etch depth elsewhere). This may be due to surface oxide formation over time, forming a significantly less soluble oxide compound. This theory is supported by the fact that the GaSb QW layer further into the wafer etched at a similar rate to the overall sample.

In addition to the GaSb cap inhibiting etching, some buffer layers tested were also prone to what may have been salt formation. This includes AlAsSb, which was the preferred buffer layer material. Whilst this did not pose an issue overall, it is worth noting, as it can cause intermediate etch depth measurements to report a growth in the height of the etched area. Unlike the GaSb cap, these growths would dissolve again in a reasonable timescale (within the overall $\sim$ 13 min etch time).

A further point to note about the etch solution is that it would rapidly lose potency over time. The etchant mixing process involved leaving 10 min for the solution to stabilise in temperature. After this time was complete, the etch rate appeared to decrease by around half every 20 min, possibly owing to the etchant's volatility and the presence of strong extractor fans. Covering the etch solution container with a lid helped maintain a stable etch rate.

3.3 Device Preparation for Measurement

The specific measurement setup and device cooling method differs between devices, therefore, each case is introduced separately in its respective chapter.

The preparation stages between completing a $\sim$ 3 mm $\times$ 3 mm chip of fabricated devices and setting up a measurement are the same for all devices featured in this thesis. In order to load an InAs/GaSb chip into a cryostat and/or connect electronic measurement instrumentation, ceramic chip carriers are used. They have an Au coated centre on which to mount a chip, and 20 Au contact pads around the centre. These surface contact pads are connected to an equal number of contacts at the reverse of the chip carrier. This allows it to be positioned onto the same number of conducting pins in a holder. This holder connects to a probe stick, which can be lowered into a cryostat or He bath for low temperature measurements, with monitoring provided by a Cernox temperature sensor. Each of the 20 pins in the holder can connect to measurement instrumentation via wires up the interior of the measurement stick.

The chip containing devices is affixed to the centre of the chip carrier with conducting silver paint. The Cr/Au device contact pads are connected to the 20 outer Au contact pads on the chip carrier by wedge bonding Al wire using a Kulicke and Soffa Industries Model 4526 wedge bonder. The ultrasonic pulse generated to melt the Al into the bond location is also sufficient to locally break through the Al_2O_3 gate dielectric layer to bond to the ohmic contacts in the Hall bar device described previously.

3.4 Data Acquisition and Processing

Experimental control and measurement data acquisition for all devices was carried out by a LabVIEW program developed by Prof. Gavin Burnell, School of Physics and Astronomy, University of Leeds. The resulting data files were processed and analysed by myself using Python 3.12.0. All graphical results presented, unless stated otherwise, were created using the StonerPlots package, also created by Prof. Gavin Burnell [36].

Chapter 4

Probing Carrier Dynamics Approaching Charge Neutrality

4.1 Introduction

This chapter centres on the charge neutral point (CNP) observed in a 12.5 nm/8 nm InAs/GaSb QW Hall bar device of 750 μm × 50 μm. This point was initially identified by a resistance peak consistent with a negative to positive switch of the Hall coefficient, where the system passes from the electron regime to the beginning of the hole regime.

I have studied the charge carrier dynamics in close proximity to charge neutrality under Lifshitz-Kosevich (LK) formalism and a Dingle analysis procedure derived from this formalism, both of which follow the temperature dependent damping of SdH oscillations. Previously, this model has successfully described approximate single carrier systems, deducing effective mass and scattering times [15]. This application relies on being distant from the CNP, which is the simple system that the application here departs from. Some studies have also reported failure of the model to represent carrier dynamics within an insulating band gap, where anomalous oscillations that cannot be described by the LK model have been reported [16, 17]. Here, I focus on the carrier density region approaching charge neutrality, from the electron dominant direction.

Currently, there lacks a systematic scan-like approach to determine a breakdown threshold carrier density at which the LK model no longer holds. Here, I show that this breakdown exists between (4.3 - 6.8) $\times$ 10^{11} cm^{-2} for this device. At lower carrier densities, the single, non-interacting carrier assumptions of the LK model become invalid. Clearly, this threshold is sample dependent, as it is dictated by the extent of band inversion. For context, this is compared to particular charge neutrality signatures: the sheet resistance maximum, the Hall mobility minimum, and the departure from linearity of the Hall resistance. At the lower end of the range, it is still $\sim 2 \times 10^{11}$ cm^{-2} from the mobility minimum, and at least 1.6×10^{11} cm^{-2} from the sheet resistance maximum and the departure from linearity in the Hall resistance.

Following this, the phase parameter in the LK model is considered in greater detail. There is currently contention as to the presence of a non-trivial Berry phase in InAs/GaSb QWs [18, 19]. In this chapter, through index plot analysis at varying gate voltages, I observe no definitive indication of a Berry phase. This is the result even when approaching charge neutrality, contrary to Ref. [18], in which a Berry phase is acquired in this region.

4.2 Hall Bar Device Experimental Setup

Before presenting the results, the relevant cryostat and measurement setup are introduced.

4.2.1 Low Temperature Measurement Setup

Low temperature conditions were achieved using an Oxford Instruments continuous flow ^{4}He cryostat. It comprises a liquid He bath containing a superconducting solenoid and a variable temperature insert (VTI). The He bath is shielded by an outer liquid N_2 bath

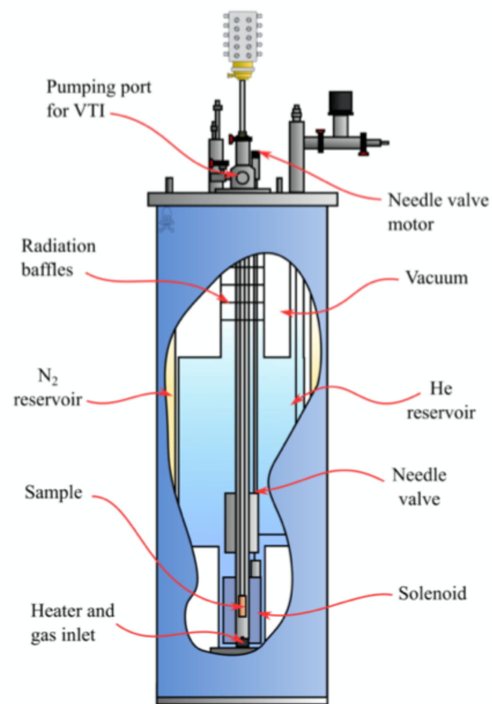

Figure 4.1: A diagram of the interior of the Oxford Instruments cryostat used for Hall bar device measurements. Reproduced from Ref. [5].

to reduce boil off, and there are radiation buffers to prevent boil off due to radiative heating. The setup is shown, with components labelled, in Fig. 4.1. The sample space within the VTI is pumped by a rotary pump, promoting a continuous flow of He gas through an inlet for He between the inside of the VTI and the He bath outside. The amount of gas drawn in can be controlled externally by a motorised needle valve, which can be opened or closed to varying degrees to cool the sample. The He drawn in also acts as an exchange gas between the heater and the sample, allowing temperature control. Submersion in a liquid ^{4}He bath can achieve temperatures down to 4.2 K. Evaporative cooling is used to cool beyond this point, where pumping removes He gas from the sample space above the liquid. This lowers the vapour pressure of the He, which reduces the boiling point, leading to a lower temperature of liquid He. The lowest achievable temperature is limited by the exponential scaling of pressure in temperature, requiring a large amount of pumping power at low temperatures for a comparatively small change. The formation of a Bose-Einstein condensate at 2.1 K is also a limiting factor, as it ascends the sides of the sample space to warmer areas, where it evaporates and further increases the load on the pump.

Low temperatures ($\leq$ 2 K) were maintained for most measurements. However, owing to potential needle valve blockage, a reliably steady He flow was not always possible. To cool devices, this was overcome by applying a cycle of closing and opening the needle valve. The closing would decrease the pressure in the VTI, encouraging flow when the needle valve was reopened. For this reason, the lowest temperatures ($\sim$ 1.5 K under optimal conditions) were not always achievable. The stable measurement temperature is indicated for each result throughout this chapter.

As described in Section 3.3, an InAs/GaSb chip containing devices is attached to a ceramic chip carrier, which is inserted into a holder capable of connecting to external measurement apparatus. The holder is the brass-coloured object at the bottom of the schematic in Fig. 4.1 (labelled 'Sample'), situated inside the VTI at the end of the probe stick and connected to the external measurement wiring. The holder pins are oriented such that the chip sits horizontally in the cryostat. This orientation means that the $\pm$ 8 T magnetic field produced by the NbTi superconducting solenoid (at the bottom of the cryostat, cooled by the He bath) is out-of-plane with respect to the measurement.

4.2.2 Transport Measurements

The completed Hall bar device used throughout this chapter is shown in Fig. 4.2a. To measure the SdH oscillations in the longitudinal resistance and IQH plateaux in the transverse resistance, a Keithley 6221 current source drove a 100 nA AC current down the length of the Hall bar (labelled in Fig. 4.2a). This current was confirmed not to induce Joule heating effects by temperature dependent measurements.

The current also acts as the reference signal for two Stanford Research Systems Model SR830 DSP lock-in amplifiers, which are connected to measure the longitudinal and transverse voltage drop in the device. The lock-ins measure the voltage response

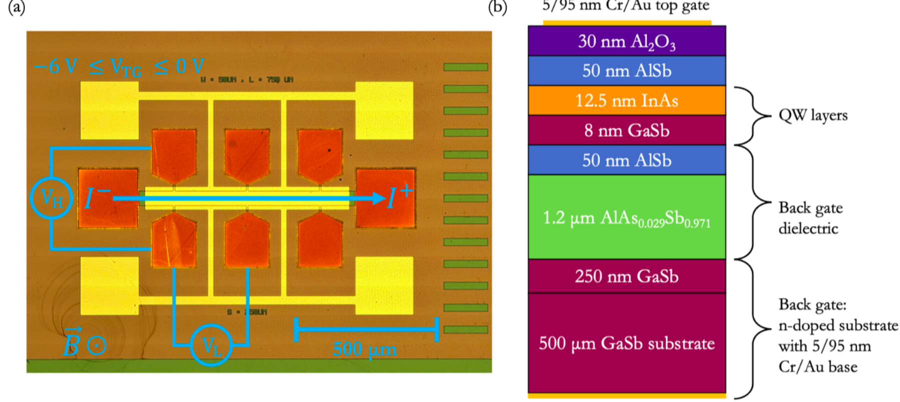

Figure 4.2: **a.** Optical micrograph of the 750 µm × 50 µm Hall bar. The Cr/Au top gate appears yellow, with the Hall bar conducting channels visible underneath. There are multiple connections for the top gate, for the purposes of ensuring continuity across the electrode and providing spare connections should a bond break upon cooling. The measurement setup is labelled. **b.** The complete layer structure for this device. The purpose of each feature is described in the MBE information in Section 3.1.1. The important distinction for this device is that it has a 12.5 nm/8 nm InAs/GaSb QW with a 1.2 µm $AlAs_{0.029}Sb_{0.971}$ buffer.

to the AC signal, oscillating at the same frequency, and noise oscillating at different frequencies. The chosen AC frequency is 119.77 Hz, which is different to known noise frequencies like the 50 Hz mains electricity and its harmonics. This means that the measurement can remain distinct from noise, as the noisy input signal is multiplied by the reference frequency, by the lock-in amplifier's phase-sensitive detector. This shifts the signal to DC, while the oscillating noise frequencies are suppressed by a low-pass filter. This filter uses a time constant of 100 ms, meaning the amplitude of the signal is attenuated by 3 dB at 1.6 Hz. There is a total of 4 low-pass filters, meaning the signal is attenuated at 24 dB/octave beyond this point. The recommended settle time for these settings is 10 time constants, which was reduced to 8 here for faster measuring, assuming that the continuous nature of the signal results in a sufficiently accurate settled value.

From the lock-in output signal, the longitudinal resistance ($R_{xx} = V_{\mathrm{L}}/I$) and transverse resistance ($R_{xy} = V_{\mathrm{T}}/I$) are calculated. The sheet resistance in Ω/sq, written as ρ_{xx} due this being a 2D system, is calculated by multiplying R_{xx} by W/L, where W is the width of the channel (50 µm here) and L is the channel length between the R_{xx} measurement probes (250 µm here). Out-of-plane magnetic fields between -8 T and 8 T were applied, along with top gate voltages of -6 V to 0 V using a Keithley 2400 Source Meter. The voltage high was connected to the top gate electrode and the voltage low was grounded. Negative voltages were applied to decrease the electron population in InAs, driving the system from electron dominance toward hole dominance. This range

was sufficient to reach charge neutrality, and a simultaneous back gate voltage was not required, so the back gate remained grounded during every measurement. The top gate dielectric breakdown occurred past -5 V, but the range was extended further in case there was a sign of carrier crossover. This is worth taking into account for data displaying the full -6 V to 0 V sweep range. In the voltage range that is the main focus of this chapter (approaching charge neutrality), the current leakage does not exceed 20 % of the 100 nA driving current.

4.3 Device Characteristics

All results presented in this chapter were obtained from the same 750 μm × 50 μm Hall bar device, shown in Fig. 4.2a. Panel (b) shows the wafer structure, which has a 12.5 nm/8 nm InAs/GaSb QW thickness. Before gating is applied and at $T = 2$ K, the Hall bar has a carrier density of (7.3 ± 0.2) × 10^{11} cm^{-2} (electron dominance), from a weighted average of fast Fourier transform (FFT) SdH frequency peak-derived and single carrier Hall signal gradient-derived densities. The peak frequency is multiplied by $2e/h$ to determine carrier density. With zero gate voltage applied, the system is sufficiently distant from charge neutrality to use the single carrier Hall slope (gradient in $R_{xy}(B)$). This is supported by the strong agreement between the carrier densities, with that of the Hall slope falling within error of that from the SdH frequency. The single carrier Hall slope is equal to R_{H}, the Hall coefficient, and the Hall carrier density is $n_{\mathrm{H}} = 1/(R_{\mathrm{H}}e)$. The Hall slope also gives a mobility of (36,400 ± 400) cm^2 V^{-1} s^{-1}. The literature lacks mobility values for structures with an $AlAs_{0.029}Sb_{0.971}$ buffer layer, but the value here is in the same order of magnitude as QWs with an $Al_{0.8}Ga_{0.2}Sb$ buffer and GaAs substrate [37]. The mobility, in cm^{-2} V^{-1} s^{-1}, can be found by $\mu = 1/(e \times \rho_{xx}(B=0) \times n_{\mathrm{H}})$.

Figure 4.3 shows the sheet resistance fan diagram obtained from a series of full -6 V to 0 V top gate sweeps, each taken at a constant magnetic field value. The field values range between -0.20 T and 8.00 T, taken at 0.25 T increments between 0.00 T and 8.00 T. These data were supplemented by additional top gate voltage sweeps, taken at -0.2 T and 0.2 T, and increments of 0.1 T between 6 T and 7 T. The former was due to ± 0.2 T being a routine measurement for establishing R_{H}, and the latter finer increments as this is the B range in which Zeeman splitting becomes visible. The trenches in sheet resistance are marked with the LL filling factor, ν, that they correspond to, converging in the region of charge neutrality.

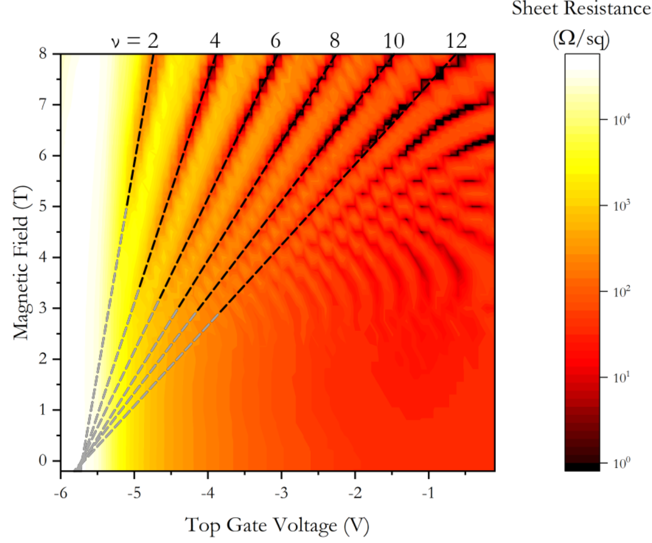

Figure 4.3: Fan diagram constructed from multiple top gate voltage sweeps held at constant magnetic field. The sheet resistance is plotted on the coloured $\log_{10}$ scale and all measurements were recorded at $T = 3.8$ K. Trenches in sheet resistance are labelled with their corresponding ν value, and traced with black dashed lines. The traces are also extended in grey, showing convergence in the charge neutral region. Created with OriginPro [6].

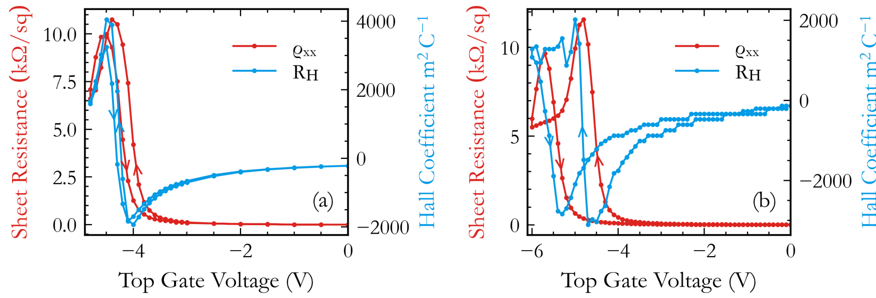

Figure 4.4: Sheet resistance responses to varying top gate voltage at $B = 0$ T and $T = 2.0$ K, with corresponding Hall coefficient sign changes indicated, as determined by the $\pm$ 0.2 T Hall resistance gradient. The back gate electrode was grounded. **a.** Top gate voltage sweep at 1.8 K for a voltage range of 0 V to -4.8 V to 0 V. The resistance peak is matched by a change-of-sign in the Hall coefficient, signalling a change from electron to hole carrier dominance. Some hysteresis is also present. **b.** Top gate voltage sweep at for a voltage range of 0 V to -6 V to 0 V. Considerably more hysteresis is present than in the more limited voltage sweep.

4.4 Transport in the Electron Dominant Regime

4.4.1 Reaching Charge Neutrality

The Hall Coefficient

A simple signature of charge neutrality and a possible hybridised insulating band gap in InAs/GaSb is a sheet resistance maximum [38, 39]. Figure 4.4 shows this maximum occurring as a function of top gate voltage, for two different gate voltage sweeps. The first, in panel (a), is a sweep from V_{TG} = 0 V to V_{TG} = -4.8 V, back to 0 V. The second, in panel (b), is a larger sweep of 0 V to -6 V, back to 0 V. The differences between the measurements as a result of changing the sweep range are discussed further below. In the meantime, it is important to note that both measurements exhibit a sheet resistance maximum in the -4 V to -5 V range, which is matched by a negative-to-positive switch of the Hall coefficient as the gate voltage is driven to more negative values. This demonstrates a carrier dominance switch from electrons, to charge neutrality ($n \sim p$), toward holes, and indicates that the Fermi level is between the outermost conduction and valence bands. Here, the Hall coefficient, R_{H}, is the gradient of the Hall (transverse) resistance, as the single-carrier approximation is valid for the majority of the sweep. The crossing of the insulating gap is also matched by a mobility minimum, shown later in Section 4.5. Although, it must be noted that the nature of the gap remains unconfirmed; namely, whether the dispersion of these bands is of topologically non-trivial origin or not, which cannot be determined from the sheet resistance maximum alone.

The charge neutral peak was accessed solely by the application of a top gate voltage. For this device, simultaneous back gate voltage application only drove the system further away from the region of interest. For this reason, the resistivity peak witnessed here should correspond to points B, E or H in the phase diagram in Fig. 2.5, where the Fermi level is situated in the centre of the insulating gap.

Figure 4.4 exhibits some discrepancy in the V_{TG} value at which the sheet resistance maximum is observed and the value at which $R_{\mathrm{H}} = 0$. This is due to the mixed carrier populations present when approaching charge neutrality. When the system is distant from charge neutrality, the single-carrier assumption is valid and provides an estimate of carrier population. Once the system is approaching charge neutrality, electron and hole populations become comparable, and so a two-carrier model of their behaviour is applicable. The two-carrier Hall coefficient can be given as

$$R_{\mathrm{H}} = \frac{p\mu_{\mathrm{h}}^2 - n\mu_{\mathrm{e}}^2}{|e|\left(p\mu_{\mathrm{h}} + n\mu_{\mathrm{e}}\right)}, \tag{4.1}$$

where n and p are the electron and hole carrier populations respectively, μ_{e} and μ_{h} are their respective mobilities, and e is the elementary charge. At charge neutrality, where $n = p$, it is not possible to also have $R_{\mathrm{H}} = 0$. This is because $\mu_{\mathrm{e}} \neq \mu_{\mathrm{h}}$, as electrons and holes possess different effective masses and therefore different mobilities. This means that, even in the two-carrier model, it is possible to have a non-zero Hall slope where

$n = p$, therefore tracking carrier density changes is difficult when only considering the sign change.

Hysteresis and System Resetting

The data in Fig. 4.4 also exhibit hysteresis between the negative-going and positive-going voltage sweeps, for both voltage ranges. It is caused by charge trapping and de-trapping at defect sites at the interface between the channel and the dielectric, thereby altering the carrier density of the channel. Defects in the lattice and, particularly, at an interface lead to dangling bonds in the dielectric compound, which act as trapping centres for either electrons or holes. Oxide dangling bonds act as hole traps, which have been shown to have the most substantial effect in Al_2O_3 and other oxide dielectrics [40, 41]. The hysteresis is amplified by the application of a stronger voltage, as the enhanced electric field can lower the energy barrier for trapping, hence the more pronounced hysteresis in the broader gate voltage sweep. The sheet resistance peak in the positive-going direction is also smaller than that of the negative-going direction. This is consistent with previous studies, and occurs as a result of charge traps acting as charged defects, shortening the quantum scattering time [42].

To maintain consistency between measurements, the system was reset by performing the 0 V to -6 V to 0 V top gate sweep. All measurements with a constant gate voltage apply to the negative-going gate voltage direction only, meaning that the voltage was always started at 0 V and swept to the necessary value, then reset after the measurement. The back gate was always grounded, using a BNC 50 Ω terminator, and a consistent thermal history was maintained.

Another observed behaviour which occasionally required resetting was a surge in carrier density upon connecting the system to the gate voltage source. At $V_{\mathrm{TG}} = 0$ V, before connecting the voltage source, the gate would be grounded by a BNC 50 Ω terminator, which was the case whenever there was no gate voltage applied. At this point, the carrier density was as previously mentioned ($\sim 7 \times 10^{11}$ cm^{-2} at 2 K). Upon connecting, it would jump to around 28×10^{11} cm^{-2} (despite no application of a voltage). At $V_{\mathrm{TG}} =$ -1 V it was driven down to $\sim 22 \times 10^{11}$ cm^{-2}, then to $\sim 16 \times 10^{11}$ cm^{-2} at -2 V. The top gate and source meter were both connected to ground. Once -2.5 V was applied, the system would approach its original state (before the voltage source was introduced), so the CNP was still accessible at more negative voltages. As the region of interest is near charge neutrality, the carrier behaviour in this high density region is of less concern here. It is only worth noting to explain why, in carrier density-dependent data, the 0 V signal exhibits behaviour more similar to that of the -2.5 V to -3 V range. This is because all 0 V gate measurements were performed with the top gate electrode grounded, without a connection to the source meter.

Whilst it is of little importance in the study of transport near the CNP, it is worth recording the details of this behaviour in case future devices from this QW structure exhibit a similar behaviour. Once the carrier number had risen, as a result of being connected to the source meter, a thermal reset (full heating and cooling cycle) would

be required to return the system to its original carrier density, suggesting the presence of thermally dependent traps.

4.4.2 The Lifshitz-Kosevich Model

The Lifshitz-Kosevich Equation

Further characterisations can be made under the single carrier assumption, such as the application of LK theory [43] to determine effective mass, which assumes a temperature-invariant effective mass that pertains to a single carrier system. The carriers are assumed to be non-interacting, and the band dispersion to be largely parabolic. LK theory is summarised by the LK equation, which exists in multiple forms depending on the nature of the system it is applied to, but the basic framework describes the normalised oscillating amplitude in terms of the product of three factors in inverse magnetic field, two of which are damping factors.

The two damping factors are generally denoted as R_{T} and R_{D}, representing the temperature damping and Dingle damping factors respectively. The temperature damping factor can be given as

$$R_{\mathrm{T}} = \frac{\Psi}{\sinh \Psi}, \tag{4.2}$$

where

$$\Psi = \frac{2\pi^2 k_{\mathrm{B}} T m^*}{\hbar e B}. \tag{4.3}$$

This describes the suppression of the oscillating amplitude with increasing temperature, with k_{B} as the Boltzmann constant, T the temperature, m^* the effective mass, and $\hbar$ Planck's constant divided by 2π. This arises from the thermal broadening of the Fermi-Dirac statistics that describe the Fermi surface, in line with $k_{\mathrm{B}}T$. Rather than a simple binary description of a state being occupied or unoccupied, the Fermi surface becomes a superposition of oscillations, the interference of which leading to a damping of the SdH oscillation [44].

The Dingle damping factor can be given as

$$R_{\mathrm{D}} = \exp\left(\frac{-\pi m^*}{e B \tau_{\mathrm{q}}}\right), \tag{4.4}$$

where τ_{q} is the single particle momentum relaxation time/quantum lifetime. This describes the impurity scattering of electrons, which leads to the broadened distribution of LL states mentioned in Chapter 2. The varying temperature and magnetic field effects in the above damping factors are also routinely used to extract m^*, the Dingle temperature T_{D}, and the Dingle ratio α (which is the ratio of the classical Drude scattering time to the quantum lifetime). This type of extraction, referred to as Dingle analysis here, is explored alongside analysing the complete LK behaviour (explained in Section 4.4.2 below).

The final factor is an oscillating term, which can be given as

$$C \cos\left(\frac{2\pi^2\hbar n}{eB} + \phi\right), \tag{4.5}$$

where C and ϕ are fitting constants, the latter accounting for phase offset. This has been linked to a Berry phase, which is explored later in Section 4.6. This factor describes the inverse B periodicity due to the LL position, with an n-dependent frequency from the E_F position.

There is also an optional third damping term, the spin damping term (R_S), which arises in some forms of the LK equation. It is given by

$$R_\mathrm{S} = \cos\left(\frac{\pi g m^*}{2m_0}\right), \tag{4.6}$$

where g is the Landé g-factor and m_0 is the electron rest mass. It is also an oscillating term, and applies to systems with Zeeman-split spin populations. The spin-up and -down electrons oscillate out-of-phase to one another, destructively interfering and damping the overall oscillation. It is essential to note that this damping term is not included here. The onset of Zeeman splitting for this device was between B = 6 and 7 T. Given that the maximum field applied was 8 T, there was insufficient Zeeman-split data to apply the spin-dependent model in a quantitatively rigorous manner. The higher field spin-split data was cut before analysis.

Combining the two spin-independent damping terms and applying $C = 4$ as the fitting constant [15] yields

$$\frac{\Delta\rho_{xx}(B)}{\rho_{xx}(0)} = 4\cos\left(\frac{2\pi^2\hbar n}{eB} + \phi\right)\exp\left(\frac{-\pi m^*}{eB\tau_\mathrm{q}}\right)\frac{\Psi}{\sinh(\Psi)}. \tag{4.7}$$

$\Delta\rho_{xx}(B)/\rho_{xx}(0)$ is the quadratic background corrected sheet resistance, normalised by the zero-field sheet resistance to give a dimensionless amplitude. ϕ remained a free parameter, as it quickly became apparent that the phase was not constant in temperature. The origin and behaviour of this phase are discussed further below, but it is worth noting that this form of the LK equation also appears in Refs. [45] and [46], with ϕ fixed at $-\pi$ in the latter.

The quadratic background correction is performed by averaging the peak and trough points of the uncorrected oscillation and performing a quadratic fit to the resulting line. This quadratic function is subtracted from the raw sheet resistance, illustrated in Fig. 4.5. The result was then divided by $\rho_{xx}(0)$, the zero-field sheet resistance, for the normalised amplitude. Refs. [45, 46] achieve the same result by normalising the resistance instead of the sheet resistance.

By first refining an LK equation fit to a zero-voltage oscillation, and then applying it to oscillations taken at more negative top gate voltages (approaching the CNP), it was possible to determine a breakdown region in carrier density, at which the LK equation can no longer describe the system.

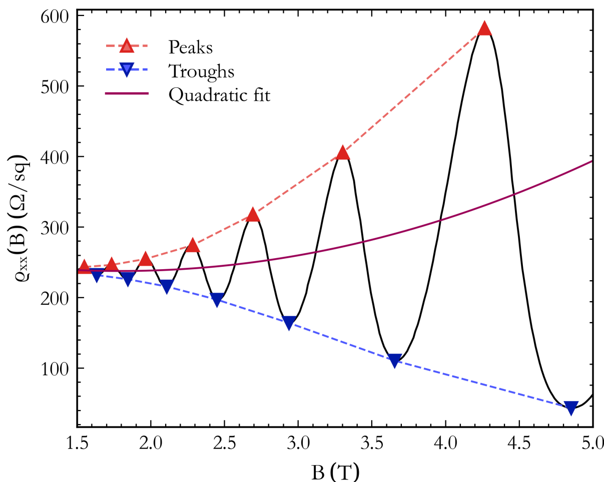

Figure 4.5: An example $V_{\text{TG}} = 0$ V oscillation before quadratic background correction. A quadratic fit is made to the average of peak and trough points, and subtracted from the raw signal.

The Dingle Plot Method

The first attempt at applying the model to the zero-field oscillation was unsuccessful, owing to the correlation between the two unknown terms in the Dingle damping term - m^* and τ_{q} - and the insufficient strength of the $\Psi/\sinh(\Psi)$ component at high fields to resolve m^*. As m^* and τ_{q} appear as a ratio, they are highly correlated and unresolvable for the magnetic field range measured here, as many values of m^* and τ_{q} could satisfy the ratio. The m^* term is also contained within Ψ, however $\Psi/\sinh(\Psi) \approx 1$ for $B > 0.2$ T, which means that the temperature damping factor also cannot resolve m^* for most of the magnetic field range. It is possible to extend the B range for which $\Psi/\sinh(\Psi)$ does not approximate 1, by measuring at a higher T. For example, raising T to 15 K extends the most active range of the $\Psi/\sinh(\Psi)$ function to $B \approx 1$ T. Although, it was not possible in this instance to produce very low field data, or higher temperature and low field data, with sufficient precision and resistance to thermal noise to determine a value for m^*. Therefore, an alternative method of determining m^* was required, and the chosen approach was to construct a Dingle plot. Forms of a Dingle plot vary slightly, but the basic structure is a plot of the natural log of the normalised quantum oscillation amplitude $(\Delta\rho_{xx}(B)/\rho_{xx}(0))$ divided by R_{T}, the temperature damping factor, as a function of inverse field [47]. The form implemented here consists of

$$\ln\left(\frac{\Delta\rho_{xx}(B)}{\rho_{xx}(0)}\frac{\sinh(\Psi)}{\Psi}\right) \tag{4.8}$$

on the ordinate axis, against

$$\frac{1}{\mu_{\text{H}}B} \tag{4.9}$$

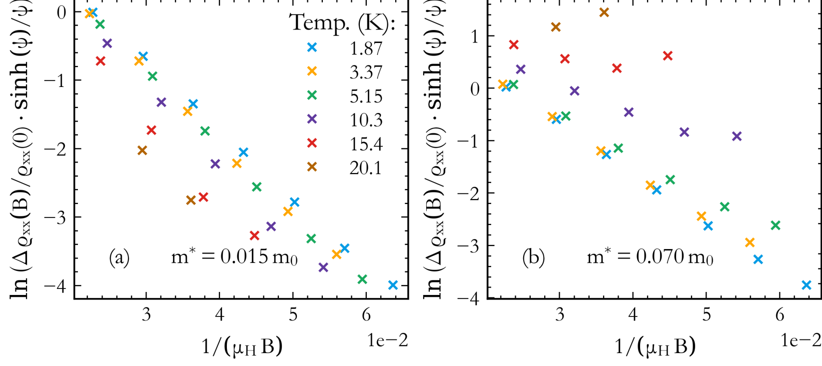

Figure 4.6: Dingle plots for m^* values below (**a.**) and above (**b.**) the final value, both of which are significantly less linear than the final plots in Fig. 4.7.

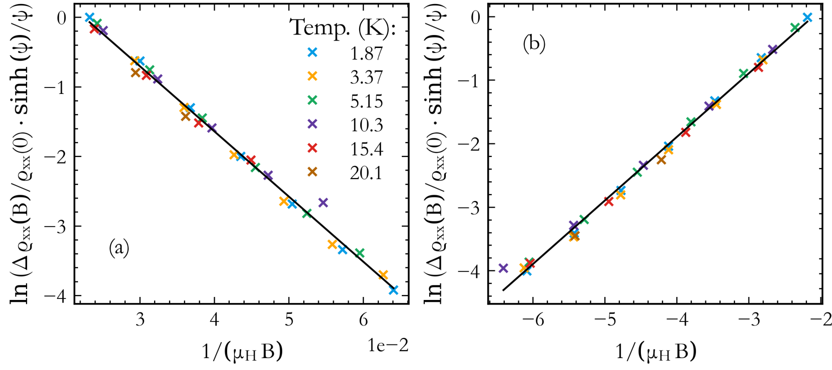

Figure 4.7: Initial Dingle plot (**a.**) and consistency check plot (**b.**) for $V_{\mathrm{TG}} = 0$ V, yielding an m^* of (0.041 ± 0.002) m_0 and an α of 25 ± 1.

on the abscissa axis, where μ_{H} is the Hall carrier mobility. The gradient is $-\alpha/\pi$. To form the linear equation, the cosine term is maximised by selecting the amplitude peaks in the oscillation for a range of temperatures, which are given in Table 4.1. The Drude mobility is substituted to contain the m^* dependence within the ordinate axis term, in Ψ. The correct m^* value is determined by an iterative process, trialling multiple values of m^*. As m^* shifts towards increasingly accurate values, the position of the differing temperature data points in relation to each other drifts from a sprawl to a negative linear formation, meaning the optimal Dingle plot is that with the most linear least squares first order polynomial fit, quantified by the lowest standard deviation. Figure 4.6 shows an example of poor m^* choices for this data, showing a lower and higher result than the final m^* value.

Here, I iterated through 100 m^* values, between 0.03 m_0 and 0.05 m_0. The optimal plot is shown in Fig. 4.7a, with the gradient divided by $-\pi$ giving the Dingle ratio,

$\alpha = \tau_t/\tau_q$. In order to ensure reliability of the result, and determine the uncertainty in m^*, I performed a self-consistency check in accordance with the method in Ref. [15]. This consisted of a similar plot, using a rearrangement of the original linear equation, with

$$\ln\left(\frac{\Psi}{\sinh(\Psi)}\right) - \frac{\pi\alpha}{\mu_H B} \tag{4.10}$$

on the ordinate axis, and

$$\ln\left(\frac{\Delta\rho_{xx}(B)}{\rho_{xx}(0)}\right) \tag{4.11}$$

on the abscissa axis, shown in Fig. 4.7. The values of m^* and α inputted should produce a linear relationship with a gradient of 1. The same 100 m^* values generated previously were inputted along with their corresponding α values, producing a final answer of (0.041 ± 0.002) m_0 and $\alpha = 25 \pm 1$. The errors were determined by the relative uncertainty of the gradient used to screen the results in the self-consistency check, and the standard error in the original Dingle plot respectively. This result for effective mass falls within the range of previous values for a single InAs QW (0.032 - 0.047) m_0 [48, 49], and is within error of that measured for an InAs/GaSb double QWs with the same thickness of InAs QW [50], in the system's electron dominant regime. This demonstrates that, as expected, this system is within its electron dominant regime before the application of a gate voltage.

These values can be inputted back into the LK model as fixed parameters, with n (which is previously known from SdH analysis) bounded within its uncertainty range. This yielded a quantum lifetime value of (0.119 ± 0.008) ps, given a variable phase in the cosine term of the fitting equation. The upper and lower m^* uncertainty values were fitted to determine its uncertainty.

4.5 Breakdown of the Lifshitz-Kosevich Model Near Charge Neutrality

Dingle Plots with Top Gate Voltage Applied

In order to push the LK model toward breakdown, the method outlined in the previous section was applied to data acquired at gate voltages of -3 V and -4 V. Again, this required repeated measurements across a range of temperatures to resolve the correlated m^* and τ_q parameters in the LK equation. Accumulating SdH oscillation data at an adequate temperature range for constructing a Dingle plot requires substantial measurement time, which is the reason for the selective voltage range. -3 V and -4 V in particular were chosen due to their proximity to the CNP without excessively inhibiting quantum oscillation visibility (which decreases as the mobility minimum of the CNP is approached, due to the $\omega_c\tau_t \gg 1$ condition).

The range of measurement temperatures was altered to favour lower temperatures, to accommodate for the decreased visibility, and are shown in Table 4.1. There is

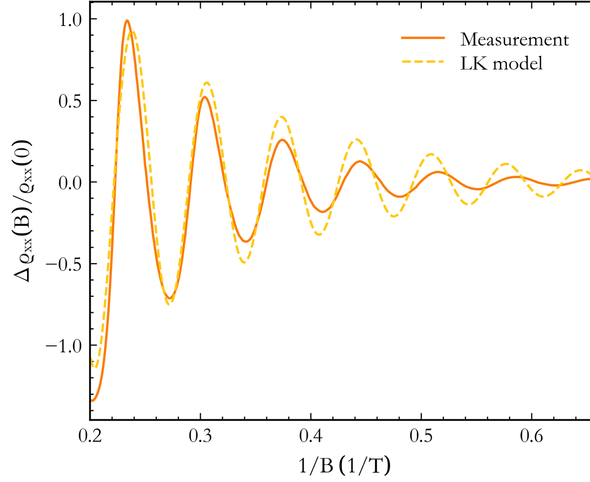

Figure 4.8: LK model (dashed line) applied to the background corrected V_{TG} = 0 V oscillation at 1.87 K. The frequency depends on n, which is bounded between its uncertainty range. m^* and α are fixed parameters, allowing the model to return a τ_{q} value of (0.119 ± 0.008) ps, given a variable ϕ parameter. The upper and lower m^* uncertainty values were fitted to determine the uncertainty in τ_{q}.

subtle variation in the precise temperatures at which the system was stabilised for a given measurement, and measurements taken above 10.1 K for -4 V did not produce discernible oscillations. The m^* range that was iterated through was widened to accommodate the change, whilst maintaining the same resolution in m^* values as before and avoiding zero-divide errors. For V_{TG} = -3V, a range of (0.1 - 1) $\times 10^{-31}$ kg was applied, with 600 iterations; for V_{TG} = -4V, a range of (0.0015 - 0.9) $\times 10^{-31}$ kg was applied, with 599 iterations. The resulting Dingle plots are shown in Fig. 4.9. For V_{TG} = -3 V, this resulted in an m^* value of (0.049 ± 0.005) m_0, and an α value of 31 ± 2. For V_{TG} = -4 V, a breakdown in the model was detected, via the inability to determine a reasonable value for the effective mass.

Limitation of the Model

The Dingle analysis method that was applied to the 0 V and -3 V data was unable to determine a reasonable range of values for the effective mass in the -4 V data, with the result being that any value within the range $0 < m^* \leq (0.08\ m_0)$ satisfied the Dingle analysis equation.

As the Dingle analysis equation is derived from the LK equation, it is built upon the same principles. Assumptions that are expected to become invalid approaching charge neutrality are: the numerous single carrier assumption, as electrons and holes become more comparable in number, and non-interacting charge carriers. This is a particularly poor approximation if electron-hole hybridised states are present. Likewise,

Table 4.1: Temperatures at which Dingle plot analysis was performed for each gate voltage, including those at 0 V. In reality, a broader selection of temperatures was used, however, higher temperatures did not yield sufficiently strong oscillations for analysis. This suppression is exacerbated when approaching charge neutrality, so the temperatures used for V_{TG} = -3 V and -4 V were altered to increase the selection of lower temperatures.

Temperature (K)		
V_{TG} = 0V	V_{TG} = -3V	V_{TG} = -4V
1.87	1.40	1.52
3.37	3.36	3.36
5.15	5.55	5.54
10.3	7.05	7.05
15.4	10.1	10.1
20.1	12.2	
	15.3	

the well-defined, mostly parabolic energy dispersion would be further violated by a non-parabolic hybridised gap [51].

As the carrier density is driven from (6.6 ± 0.2) × 10^{11} cm^{-2} to (4.5 ± 0.2) × 10^{11} cm^{-2} (between V_{TG} = -3 V and -4 V), the band dispersion deviates from the model such that the effective mass becomes indeterminable. This carrier density range of around 2 × 10^{11} cm^{-2} is sample dependent. Different QW structures will possess different band structures, since even structures of identical design may have varying interfacial defects, which can impart strain and affect band inversion.

This range can be put into perspective by considering its proximity to CNP signatures. As shown in Fig. 4.4b, the sheet resistance maximum occurs at -4.8 V. This is at least 0.8 V beyond the breakdown of the LK model. It was not possible to determine a precise corresponding carrier density due to the suppression of SdH oscillations and discontinuity in the Hall signal. Figure 4.10a shows the determinable carrier densities, obtained from the SdH oscillation analysis and ± 2 T Hall signal gradient, from 0 V to -4.5 V. The uncertainties are determined from the FFT frequency peak resolution and the 1 % error in B respectively.

The Hall carrier density it limited by the departure from linearity of the Hall resistance, which becomes discontinuous between -4.5 V and -5 V. The mobility as a function of carrier density is shown in Fig. 4.10b, with the mobility minimum occurring at -4.5 V, within this measured range. This corresponds to a Hall carrier density of (2.27 ± 0.02) × 10^{11} cm^{-2} and a SdH carrier density of (1.8 ± 0.2) × 10^{11} cm^{-2}.

By modelling the varying gate voltage and the conducting QW channel as a parallel plate capacitor system, an average dielectric constant for the layers between can be determined. When discounting the 3 nm GaSb cap layer dissolved in the developer solution (discussed in Section 3.2), this results in an average dielectric constant of 4.

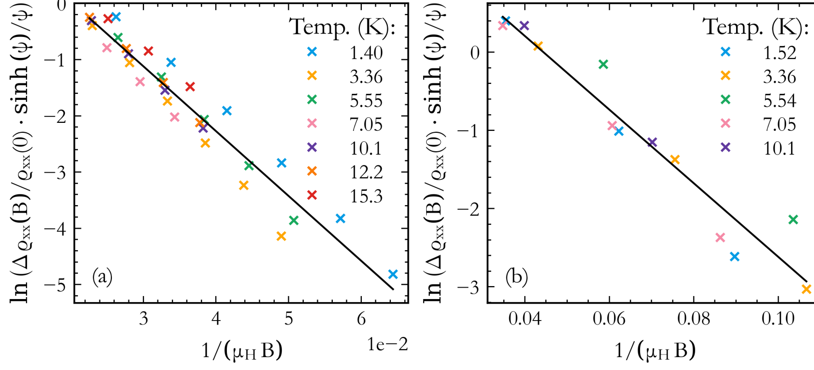

Figure 4.9: **a.** Dingle plot for V_{TG} = -3 V, yielding an m^* of (0.049 ± 0.005) m_0 and an α of 31 ± 2. **b.** Dingle plot for V_{TG} = -4 V, giving $0 < m^* \leq 0.08\ m_0$ and $\alpha = 15 \pm 1$. The points for ∼ 12 K and ∼ 15 K are non-existent due to the oscillations being too suppressed to produce discernible peaks.

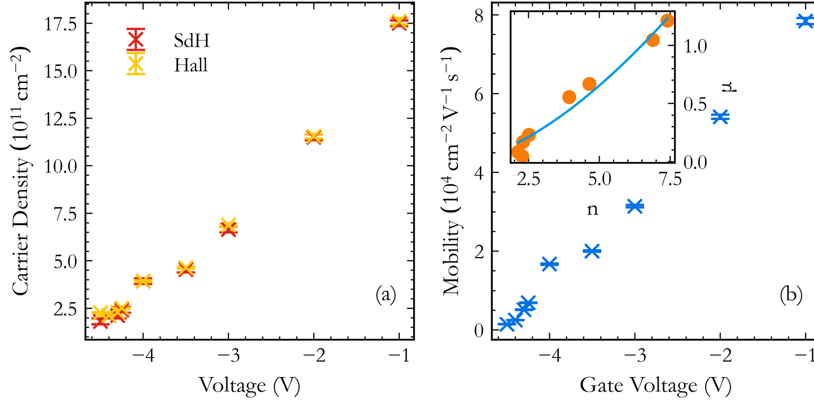

Figure 4.10: **a.** Carrier density as a function of top gate voltage at (1.39 - 1.52) K, including both the FFT-determined result from the SdH oscillation and the Hall resistance gradient for ± 2 T. The uncertainty in the SdH result is from the resolution of the FFT frequency peak, and the uncertainty in the Hall result is from the 1 % uncertainty in B. **b.** The Hall mobility as a function of top gate voltage. The μ against n (n from the Hall resistance) relation is given in the inset for the $< 8 \times 10^{11}$ cm^{-2} carrier density range, as it is the range studied in this chapter. This is fitted to $\mu \propto n^{\beta}$, where β is 1.6 ± 0.2, indicating the the principal scattering mechanism is Coulombic remote impurity scattering [7]. The n and μ units match those in panels (a) and (b) respectively.

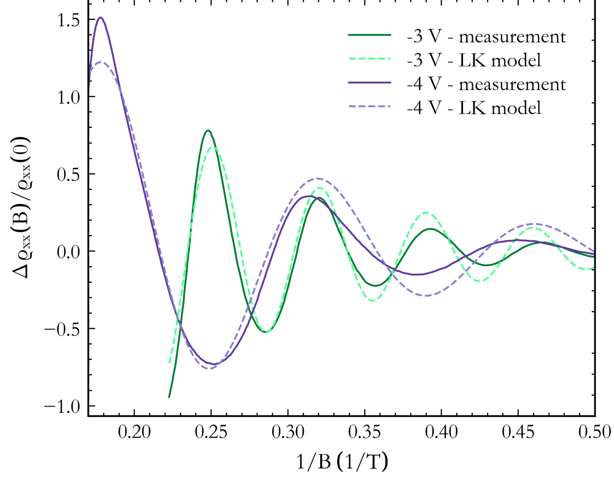

Figure 4.11: The background corrected, normalised measured oscillations and LK model fit oscillations for V_{TG} = -3 V and -4 V at 1.40 K and 1.52 K respectively. For -3 V, n was bounded within its uncertainty range as determined by SdH oscillation frequency analysis. m^* was a fixed parameter, whilst ϕ and τ_{q} were variable parameters. This resulted in a τ_{q} value of (0.12 ± 0.01) ps, with the uncertainty determined by fitting the upper and lower bounds of m^*. For V_{TG} = -4 V, the fit shown uses the maximal m^*, 0.08 m_0. Fits were possible at regular 0.01 m_0 intervals between 0 and 0.08 m_0. This does not include 0 itself, for which the model is invalid.

This is lower than the average dielectric constant calculated from literature values, which is 10 [52, 53]. When considering carrier densities more distant from charge neutrality ($V \geq$ -3.5 V), the result is closer, at 8. It is understandable that the results are not in agreement, as the literature values originate from bulk samples at room temperature.

The inset of Fig. 4.10b shows mobility as a function of Hall carrier density. This is fitted as $\mu \propto n^{\beta}$, where β is an asymptotic density scaling exponent that indicates the dominant scattering mechanism in the system. Here, at 1.6 ± 0.2, it indicates that Coulomb scattering due to remote impurities is the main mechanism [7].

Applying the Lifshitz-Kosevich Equation Near Charge Neutrality

Once m^* and α were determined from the Dingle analysis for V_{TG} = -3 V, they were incorporated into the LK model as fixed parameters for the base temperature oscillation for both gate voltages (as was the method for V_{TG} = 0 V). For each gate voltage, a fit was performed, with phase and τ_{q} set as free parameters. This method was also applied to the -4 V oscillation to the best degree possible, by using the m^* range and the α value of 15 ± 1 that the method determined, despite the breakdown.

The fits to the model are shown in Fig. 4.11, and the m^*, α and τ_{q} results for

Table 4.2: m^* and α values determined by the Dingle analysis, applied to the LK model to determine τ_q. At V_{TG} = -4 V, the method breaks down and is unable to determine a range of m^* more specific than 0 to 0.08 m_0 (not including 0 itself, as the LK equation becomes undefined). A fit was still possible at $m^* = 0.08\ m_0$ (and at regular intervals in the $0 < m^* \leq 0.08$ range), meaning that an equally broad value of τ_q could be produced.

V_{TG} (V)	m^* (m_0)	α	τ_q (ps)
0	0.041 ± 0.002	25 ± 1	0.119 ± 0.008
-3	0.049 ± 0.005	31 ± 2	0.12 ± 0.01
-4	≤ 0.08	15 ± 1	≤ 0.21

all voltages are collected in Table 4.2. This high initial (0 V) value of the Dingle ratio indicates that the dominant scattering mechanism is long-range scattering from remote or interface Coulombic impurities, in agreement with the exponent determined previously. This is due to remote Coulombic scattering perturbing the quantum phase coherence (which reduces τ_q), whilst having a lesser effect on the momentum relaxation (which determines τ_t).

As the carrier density is driven down at V_{TG} = -3 V, the Dingle ratio takes a slightly higher value. This suggests an increase in τ_t, possibly due to a reduced carrier density meaning less impurity ionisation scattering events within the channel. It appears to be less affected by a decrease in τ_q (which could be due to the decreased carrier number reducing the screening from the remote/interface impurities). This is seen by the change in τ_q between the 0 V result and the -3 V result in Table 4.2. Within the uncertainty ranges, the quantum scattering time remains unchanged. Conversely, substituting these values into α to determine τ_t yields (3.0 ± 0.3) ps and (3.7 ± 0.6) ps for 0 V and -3 V respectively. Whilst the uncertainty ranges do just overlap, they are considerably more separate than for τ_q. The m^* value has also drifted further from the aforementioned literature values for single InAs QWs of (0.032 - 0.047) m_0 [48, 49]. The lower uncertainty bound still lies within the reported values, however, the increase indicates that the band structure is becoming less akin to that of an InAs 2DEG. The fact that m^* is increasing as E_F is scanned down the conduction band also indicates that the dispersion is not perfectly parabolic, as described by

$$m^* = \hbar^2 \left(\frac{\mathrm{d}^2 E}{\mathrm{d}k^2} \right)^{-1}, \tag{4.12}$$

where E is the carrier energy and k is the wave vector [54] (as in Fig. 2.4b).

At -4 V, as the system is driven closer to charge neutrality, α decreases significantly - to around 50 % of what it was at -3 V. Despite 15 ± 1 still being sufficiently high to signal remote/interface impurity scattering dominance, a decrease in τ_t and/or an increase in τ_q is evident. A decrease in τ_t is not consistent with the increase observed in -3 V (which was related to the lower carrier number), meaning an additional scattering

mechanism may have come into effect. There is no clear explanation on the basis of these data alone. Due to the breakdown of the LK model, it was not possible to resolve α into its constituent scattering times and determine a cause, as τ_q could only be narrowed down to a large range.

4.6 Berry Phase Detection

4.6.1 Changes in Phase and Frequency

Whilst setting the ϕ parameter as variable was a convenient feature to facilitate fitting to the LK model, it would be unwise to ignore the physical significance. As this phase parameter is linked to a Berry phase [55, 56], the variation in this phase is considered. Monitoring this phase also exposed the fact that the oscillations used for LK/Dingle analysis were not precisely periodic in $1/B$, with such frequency drifts also considered below. This lead to the construction of a Landau index fan diagram, a typical method for determining Berry phase.

A Berry phase is acquired by the wave function of a system when its parameters are varied adiabatically in a closed loop in some parameter space, such as momentum or magnetic field. It can be linked to chiral or helical quantised conduction, and give local indications of topology. It can be detected from phase shifts in quantum oscillations, hence why it is considered a possible cause of the seemingly varying ϕ values here. For materials such as graphene, a Berry phase of π is well established and reflects its topologically non-trivial band structure [56]. The presence of a Berry phase in InAs/GaSb is not as thoroughly studied and a matter of contention [18, 19].

The quantum oscillation phase parameter ϕ, from Equation 4.7 in the previous section, can be directly related to a Berry phase. Typically, this is done using an alternative form of the LK equation [55] to that used here, which is

$$\rho_{xx} \sim \cos\left\{2\pi\left(\frac{f}{B} \pm \frac{1}{2} + \gamma\right)\right\}, \tag{4.13}$$

where f is the oscillation frequency and γ is related to the Berry phase by

$$\gamma = \frac{\Phi_B}{2\pi}, \tag{4.14}$$

where Φ_B is the Berry phase [56]. In this form, a γ value of 0 or 1 would lead to a trivial (zero) Berry phase, while a γ of $1/2$ would lead to a Berry phase of π. Variations of this form occur for two main reasons: the first is sign changes in the components due to the cyclical nature, and the second is how γ is defined in relation to Φ_B. Here, γ is given by the linear relation of ν to inverse B, $\nu = a/B + \gamma$. This is utilised in the Landau index plot analysis, which is introduced and discussed below. What is important to note here is that this linear equation corresponds to the minima in ρ_{xx} for integer ν values. In some studies, the ρ_{xx} maxima are referenced instead, which will shift Equation 4.13 by half a cycle, omitting the $1/2$ [55].

Table 4.3: ϕ parameters from LK model, referred to as global phase to distinguish them from local peak-to-peak phases considered below. *This ϕ value is from the average across a range of m^* values $\leq$ 0.08 m_0.

V_{TG} (V)	ϕ
0	$(0.84 \pm 0.02)\ \pi$
-3	$(0.92 \pm 0.03)\ \pi$
-4	$(1.31 \pm 0.06)\ \pi$*

Relating Equation 4.13 to Equation 4.7, one can deduce that a ϕ value of $\pm\ \pi$ yields a trivial Berry phase of zero [45–47, 57]. As previously mentioned, in order to successfully fit data to the LK model, a free phase parameter was required. Table 4.3 shows the phase parameters on which the fit settled, which are referred to here as the 'global phase'. The result for the V_{TG} = -3 V fit is close to π, however, this is not supported by the 0 V oscillation, which superficially suggests a non-trivial Berry phase.

Whilst the global phase allows the fit to be made, it is not descriptive of the phase behaviour throughout the oscillation. This can clearly be seen in the LK fits for V_{TG} = 0 V (Fig. 4.8) and -3 V (Fig. 4.11), where phase coherence is seen for one peak in each case. On either side of this peak, the coherence is quickly lost. This lack of $1/B$ periodicity in the measurement oscillation is suggestive of a non-constant carrier density during the magnetic field sweep, which may be due to charge trapping/detrapping occurring over time.

In addition to this, the SdH oscillations recorded at varying temperatures (for the Dingle analysis) showed phase shifts between these temperatures. The V_{TG} = 0 V oscillations are shown in Fig. 4.12a as an example. The shifting does not follow a particular direction with temperature, and the pattern was not repeated in the -3 V and -4 V signals (they exhibited different shifts). Panel (b) shows the temperature evolution of the Hall carrier density. This appears to loosely correlate with the extents of the shifts.

Panel (a) also indicates the peaks in each oscillation with markers and vertical lines. Along with these indicators, there is also a series of thicker grey dashed lines to indicate the peaks of a reference cosine function. This cosine function has a frequency determined by the SdH carrier density, such is the case with the LK equation, and serves as a reference signal of constant frequency. Differences between peak pairs within the same oscillation are not visually obvious. Further, when comparing successive peak-to-peak separations in $1/B$, the changes do not exceed 3 %. However, the inconsistency becomes very clear when compared with the peak positions of the reference signal. By taking the difference between a reference frequency peak and a measurement peak, a local phase can be determined. The local phases for the peaks labelled in panel (a) are shown in panel (c), to demonstrate the phase shifts between temperatures and how much this varies between peaks in the same oscillation. This also shows no known correlation, with local phase points spreading and contracting seemingly

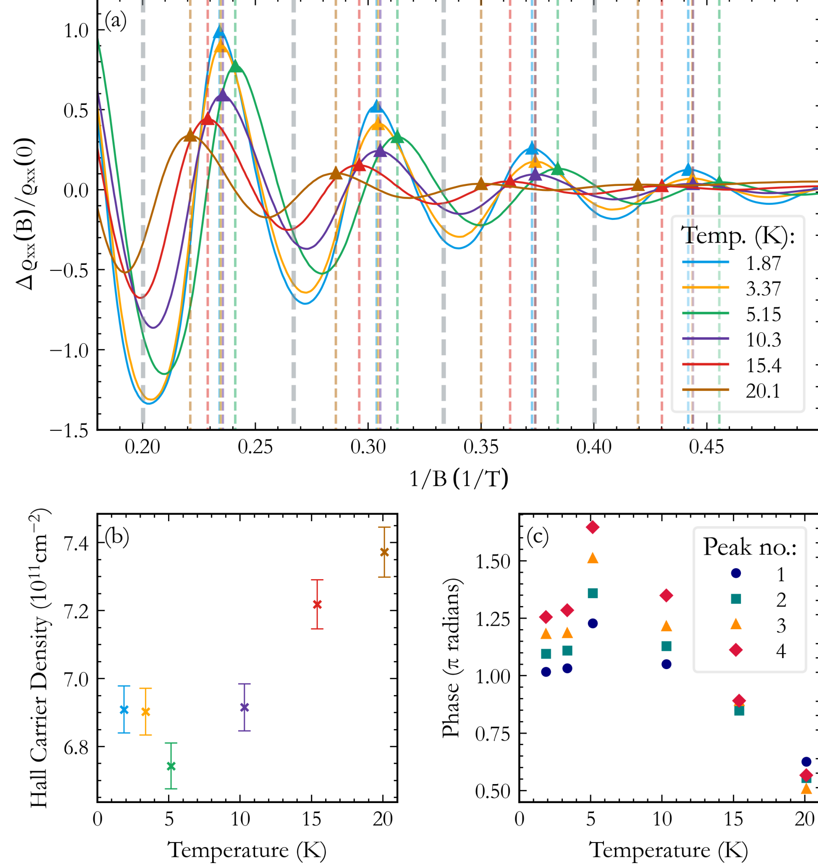

Figure 4.12: **a.** $V_{\mathrm{TG}} = 0$ V oscillations at varying temperature, showing phase drift. Four peaks per oscillation are present, indicated by triangular markers. They are also marked by vertical dashed lines, to facilitate tracking in $1/B$. The thicker grey dashed line corresponds to the peaks of a reference cosine function, with the known SdH carrier density inputted to determine the frequency. The extent of deviation from this reference line indicates the phase shift in the LK model. **b.** The Hall carrier density varying in temperature, colour coded to match panel (a). For the first and second peak in panel (a), the Hall carrier density exhibits similar shifts. **c.** The local phase shift for each of the four peaks shown in panel (a), measured from the reference cosine function peaks.

randomly at each temperature. The shifts in peak-to-peak period cannot be linked to gate voltage (for the -3 V and -4 V measurements, where it is stable with an uncertainty of 0.02 % + 600 μV), nor the temperature, where the maximum temperature deviation (at zero-field) was 1 % of the settled value, and for most measurements it was below 0.2 %.

The changing frequency could be a result of Zeeman interference. It was acknowledged in Section 2.1.1 that the visible onset of Zeeman splitting occurs between 6 and 7 T for this device. Whilst this is the visible onset of the splitting, there may be earlier interference at B values where there is not a well resolved peak, which could introduce phase inconsistencies. The form of the LK equation that accounts for Zeeman interference was not employed here due to lack of evidence of Zeeman splitting at fields below -6 T, as mentioned in Section 4.4.2.

Another possible cause is an interfering hole frequency that may still be present at the carrier densities measured at. However, the amount by which the periods change across an oscillation does not change significantly between $V_{\mathrm{TG}} = 0$ V and $V_{\mathrm{TG}} =$ -3 V, varying within a range of 0.06 and 0.07 T^{-1}. Although, for $V_{\mathrm{TG}} =$ -4 V, the variation in period length doubles from that of 0 V and -3 V, meaning perhaps the more comparable electron and hole populations.

Having established that both global and local phase variations occur without a clear physical origin, and considering the requirement of a phase parameter of $\phi \neq \pi$ in the LK fitting process, this naturally led to the consideration of a Berry phase in InAs/GaSb QWs, for which I constructed a Landau index plot.

4.6.2 Landau Index Plot

A standard method for determining the existence of a Berry phase is to construct a Landau index fan diagram, in which the integer ν values are plotted in $1/B$. The integer points are determined by the ρ_{xx} minima, and the intercept gives γ. If n is proportional to gate voltage (meaning it is constant for each fan segment), ν will be linear in $1/B$. This is in accordance with the equation $\nu = a/B + \gamma$, where $a = (nh/e)$ and γ continues to relate to the Berry phase through $\gamma = \Phi_{\mathrm{B}}/2\pi$.

The plot is repeated for various gate voltages, shown in Fig. 4.13, producing a fan-like dispersion and yielding a γ value for each gate voltage. Generally, the average of this γ value across the varying gate voltages is indicative of the Berry phase of the system, however, it can be considered on an individual basis for each gate voltage as charge neutrality is approached. A non-trivial intercept implies a LL at zero energy, which is a signature of a non-trivial Berry phase.

For InAs/GaSb QWs, the interpretations of γ are less conclusive. Ref. [18] reports γ values that lie within error of zero for gate voltages distant from charge neutrality. However, for a gate voltage with confirmed electron/hole hybridisation, they report a γ value of 0.33 ± 0.05, which they attribute to a non-zero Berry phase acquired in the carrier cyclotron orbits. On the other hand, Ref. [19] also reports non-zero γ for low carrier density gate voltages, but crucially does not attribute the result to a non-trivial

Berry phase.

They observe a similar pattern to Ref. [18], in that a seemingly non-trivial intercept emerges close to charge neutrality. Instead of interpreting this as a non-trivial Berry phase, they argue that treating the $\nu(1/B)$ data for each gate voltage as a single linear relationship with a common intercept is not always suitable and can erroneously predict a non-trivial Berry phase. In their study, it was clear that a piecewise linear fit was appropriate. This was also emphasised by the matching piecewise parity changes in their ν values. Here, there was no such behaviour and no obvious indication that the Landau index plots ought to be considered piecewise. Nevertheless, the implications are important, as multiple linear functions will have individual gradients, which are proportional to the carrier density. As discussed previously, the carrier density here is seemingly not constant across an oscillation. The piecewise changes in carrier density in Ref [19] show up to a 5 % change, and the changes in frequency in the base temperature oscillations in Figs. 4.12 are up to 4 %. The difference in the oscillations here is that the frequency does not clearly vary in a piecewise manner, and instead varies more continuously across the oscillation. Again, this does not provide a strong case for segmenting the index plots, meaning that all plots were treated as having single intercept (see Fig. 4.13). For clarity, the n values determined from each single gradient were in excellent agreement with their corresponding FFT-derived n values.

The inset of Fig. 4.13 shows the γ results across the gate voltages, with an average of -0.01 $\pm$ 0.05. This average is consistent with there being no non-trivial Berry phase across the gate voltage range. Evidently, only V_{TG} = -2.0 V and -3.5 V span a range that includes $\gamma = 0$. Although, $\gamma_{-1\mathrm{V}}$ and $\gamma_{-4\mathrm{V}}$ are relatively close. The largest deviation from $\gamma = 0$ is at V_{TG} = -3.0 V, at 0.21 $\pm$ 0.04. In isolation, this could be interpreted as the signature of a non-trivial Berry phase, although V_{TG} = -3.0 V is still relatively distant from charge neutrality. Furthermore, the next result at V_{TG} = -3.5 V covers $\gamma = 0$.

The γ value for V_{TG} = -4.0 V does not span $\gamma = 0$, however, upon comparison with other γ values, it is clearly not convincing evidence of a Berry phase near charge neutrality, unlike that observed in Ref. [18], where their non-trivial γ observation near charge neutrality was the only result that did not span $\gamma = 0$.

4.7 Concluding Remarks

In summary, the LK model and its derivative Dingle analysis have been applied to the InAs/GaSb QW system at varying top gate voltages to scan for a breakdown point. I have determined a breakdown region of (4.3 - 6.8) $\times$ 10^{11} cm^{-2}, within which the Dingle plot method fails to determine a precise value for m^*, only narrowing it to a range of $0 < m^* \leq 0.08\ m_0$.

The SdH oscillations in $1/B$ for various gate voltages and temperatures have shown variable phase values that suggest the presence of a non-trivial Berry phase. The period also varies across an oscillation in $1/B$. The frequency variation shows a correlation

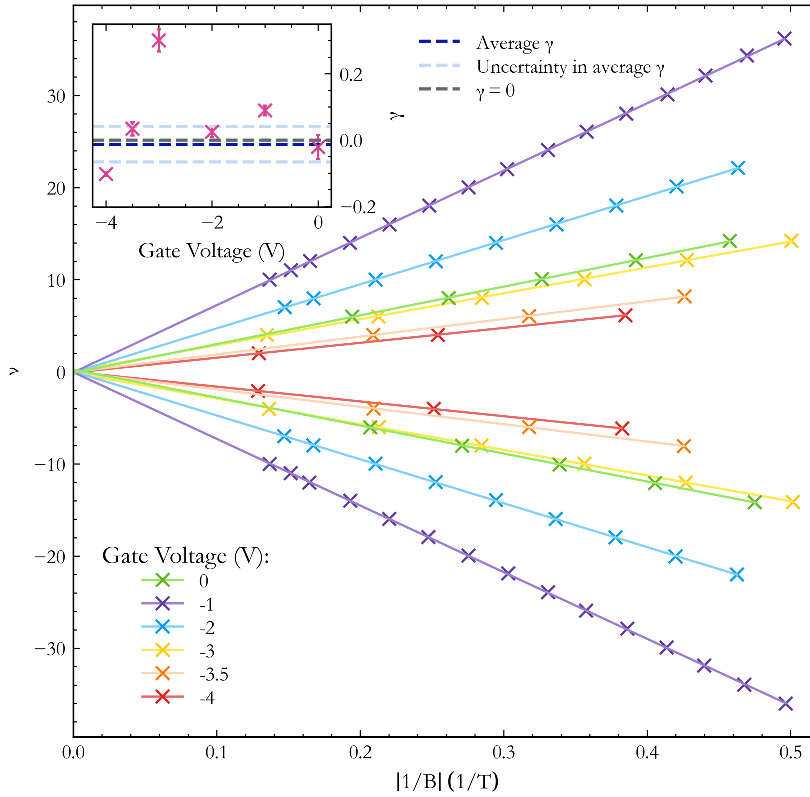

Figure 4.13: The Landau index plots for varying gate voltages, plotted in $|1/B|$ to visualise both polarities of magnetic field. The temperatures for each plot ranged between 1.39 and 1.52 K, apart from the 0 V plot, which was at 2.12 K. The value of ν at the intercept of each plot is equal to γ. These values of γ are plotted in the inset, the uncertainty range of which is determined by the standard deviation in the weighted linear least squares fits, with a weighted average over results for both B polarities. $\gamma = 0$ is marked, along with the average γ result (and its uncertainty boundaries), which is -0.01 $\pm$ 0.05.

with the Hall carrier density, and remains relatively close to the SdH FFT frequency peak. The frequency changes do not occur in discrete segments over $1/B$, meaning that the Landau index plots in gate voltage were each fitted with a unified gradient and intercept. The Landau index plots did not comprehensively support a non-trivial Berry phase near charge neutrality, contrary to Ref. [18], and across the gate voltage range produced an average γ of -0.01 $\pm$ 0.05.

Chapter 5

InAs/GaSb Devices with Integrated Ferromagnetic Contacts: Micron-Scale Transmission Lines

Following the investigation into carrier dynamics nearing charge neutrality provided in Chapter 4, the principal aim was to study the fabrication and behaviour of FM/(InAs/GaSb) junctions. Through in-depth fabrication tests and many iterations of InAs/GaSb QW devices integrating FM contacts, I have optimised the ohmic performance of FM/(InAs/GaSb) QW junctions and characterised their resistances. Two types of devices were fabricated: the first of these was a micron-scale transmission line-type device, the purpose of which was to determine the FM contact resistance and whether this contact could reliably be made through the edge of the InAs/GaSb QW channel. This initial micron-scale device, numerous fabrication tests conducted during its optimisation, and its final I-V performance are the focus of this chapter. The second type of device, a transmission line-type device containing nanoscopic features, is presented in Chapter 6.

5.1 Introduction

5.1.1 Motivation

The injection of spin-polarised currents into the edge transport regime of coupled InAs/GaSb QWs would offer the possibility of studying the spin-momentum locking in QSH conduction channels, via the deflection ratio of injected carriers by the two possible transport directions. Such an experiment could be realised by attaching FM contacts to the edge of an InAs/GaSb QW device tuned to the band inverted phase. As the application of FM contacts to InAs/GaSb QWs is novel, it is important to first establish the behaviour of the contacts at an FM/InAs and FM/GaSb interface. Primarily, this concerns the nature of the interface barrier and the specific contact resistance. Ideally, the barrier is ohmic. For this reason, the first devices I fabricated were transmission line model (TLM) devices, not to be confused with the 'transfer length method', which is a different contact resistance measurement technique, and also abbreviated to TLM. The chosen FM material was the alloy $Ni_{0.8}Fe_{0.2}$, commonly known by its trade name Permalloy (Py). This was primarily due to it being a FM material readily available in our cleanroom facility, in addition to its relatively low coercivity. This would aid control of magnetisation and, in turn, spin current polarisation for injection in future devices. Whilst Py/(InAs/GaSb) junctions have not been previously studied, Py/InAs junctions have been successfully fabricated [58], and earlier experiments involving superconductor/semiconductor junctions have demonstrated transition metal contact fabrications onto InAs QWs [59], InAs-AlSb QWs [60] and InAs/GaSb QWs [61, 62], also providing fabrication techniques that were implemented here.

The successful fabrication of these devices sought to complete three objectives. The first of these was to determine the specific plasma etching and metal deposition techniques needed to produce a clean semiconductor/Py interface, capable of demonstrating consistent ohmic behaviour. A variety of oxygen and argon plasma ash interface cleaning combinations were trialled, as outlined in Section 5.3.2, where the corresponding I-V performance is assessed. The second was to determine where connection to the

channel could be reliably established: would placing Py contacts along the outer area of the device connect exclusively via a direct contact with the edge of the QW, or also through the top of the AlSb barrier via pinhole sites? To establish this, three different TLM contact geometries were fabricated, each contacting the top and/or side of the main transmission line in a different manner. The third objective was to deduce a contact resistance for the device, by performing a series of I-V measurements between Py contact pairs at various separations, and applying the results to the TLM equation explained in Section 5.1.2 below. Applying the model also determined additional information about charge transport between the Py contacts.

5.1.2 Ohmic Contacts and the Transmission Line Model

In order to ascertain the I-V behaviour of the Py/semiconductor interface and its specific contact resistance, micron-scale TLM devices were fabricated. The measured resistances are expected to scale linearly with contact separation, and the true contact resistance is determined from

$$R_{\text{measured}} = \frac{R_{\text{sheet}}}{W} l + 2R_{\text{contact}}, \tag{5.1}$$

where R_{measured} is the raw two-terminal resistance between a given pair of contacts, R_{sheet} is the sheet resistance of the semiconductor between that pair of contacts, W is the width of the channel connected to the contact (see Fig. 5.1), l is the contact separation, and R_{contact} is the true contact resistance. If a plot of measured resistance against l is made, the real contact resistance can be extracted from the intercept of a linear fit. The result assumes that the contact resistance is the same for all contacts.

Another purpose of these devices was to determine whether or not the contacts are indeed ohmic, as determined by the extent of linearity in the I-V signal for a ± 20 μA range. The I-V relationship is determined by the band structure at the metal/semiconductor junction. As the InAs layer is n-type and the GaSb layer is p-type, there are two junctions with the Py to consider. Ideally, the Py/(InAs/GaSb) forms a contact of low resistance relative to the junction materials, through which carriers can flow back and forth, leading to constant resistance and linear I-V measurement. Metal-semiconductor interfaces can also form a Schottky barrier, pictured in Fig. 5.2 for an n-type semiconductor. When there is a voltage bias across the junction, charge transfer is promoted (forward bias) or suppressed (reverse bias), resulting in a diode-like I-V response.

The diagram in Fig. 5.2b implies that a comparison of bulk work functions can indicate whether the metal and semiconductor form an ohmic or Schottky junction. In the n-type case, $\phi_{\text{metal}} < \phi_{\text{n}}$ would lead to an ohmic junction, and $\phi_{\text{metal}} > \phi_{\text{n}}$ would lead to a Schottky junction (and vice-versa for the p-type case). In this instance, the bulk comparison is an oversimplification. There also appears to be no reported thin film work function value for Py in the literature for any Ni/Fe composition. Regardless, this value would be highly dependent on interface quality, which varies between surface

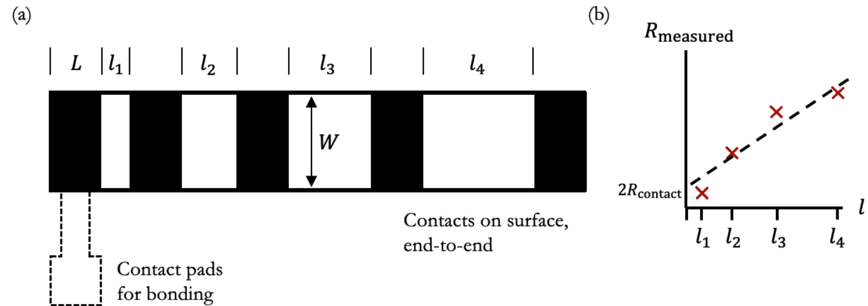

Figure 5.1: **a.** General transmission line layout, where metal contacts in black lie on top of the semiconductor mesa strip in white. The width of the mesa is given by W, and the contacts are of dimensions $W \times L$. The separations between each contact pair are given as l, and increase in size down the length of the mesa. The dotted line shows that the primary contacts, whose resistances are being tested by the transmission line, will have additional contacts with pads attached for measurements. **b.** The illustrative plot demonstrates a linear fit of measured resistance against contact separation l, where the y-intercept is twice the true contact resistance.

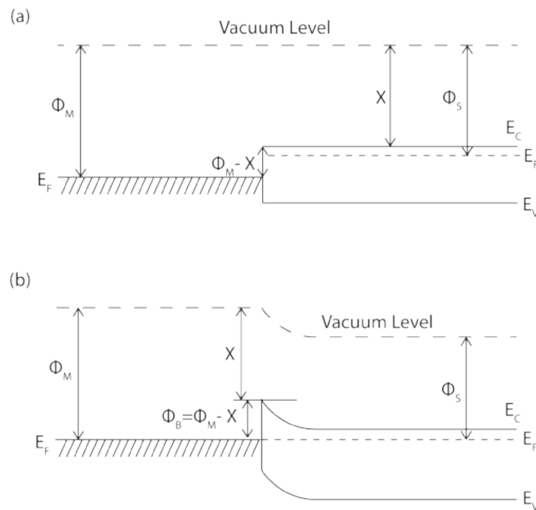

Figure 5.2: Metal-semiconductor (n-type) junction, with the metal on the left and the semiconductor on the right. **a.** shows the junction before thermal equilibrium and **b.** shows the junction in thermal equilibrium. The metal work function (Φ_M) is greater than the semiconductor work function (Φ_S). E_C and E_V are the conduction and valence band energies respectively, χ is the electron affinity and Φ_B is the Schottky barrier height. Retrieved from [8].

preparation and deposition methods. Likewise, the work functions of InAs and GaSb are highly dependent on such factors, rendering any attempt to determine a difference futile. Moreover, it has been found that junctions with a III-V semiconductor component are less dependent on the work functions of the materials, due to Fermi level pinning by interfacial defects such as lattice mismatch and oxides [63]. This is why it is paramount to establish the optimum interface preparation during fabrication and characterise its contact resistance.

When one measures the resistance across a semiconductor between a pair of contacts, one measures the sum of multiple resistance components: the resistance of the semiconductor between the contact pair, the resistance of the metal that constitutes the rest of the contact, the actual contact resistance (which includes a small portion of the metal and semiconductor resistances), and any further resistance introduced by the measurement setup. This can be written as

$$R_{\text{measured}} = 2\left(R_{\text{metal}} + R_{\text{contact}}\right) + R_{\text{semiconductor}} + R_{\text{setup}}, \tag{5.2}$$

where the 2 accounts for the pair of contacts, and R_{metal} refers to the contact material above the interface. The setup resistance includes any sources of background resistance included in the measurement setup, which is typically the resistance of the cables in which the current source and voltage measurement are combined. This is generally small compared to the contact resistance. Often, R_{metal} is also negligible compared to R_{contact} and can be ignored. The contact resistance itself is complicated, as it includes resistances from the metal immediately above the interface, the semiconductor immediately below the interface, and the interface itself. The interface resistance can be affected by defects, dangling bonds, and interfacial oxides, but it is possible to use Equation 5.2 to determine this contact resistance.

This is not the only information contained within the model. The ideal contact required in the description above does not account for current crowding. An ideal contact would only pass current into the semiconductor at the very end of the contact. Figure 5.3 shows a more accurate depiction of where the current enters and leaves the semiconductor, which is not confined to the contact edge, and not uniform throughout the contact. Instead, it is mostly concentrated at the expected edge, but also occurs throughout the rest of the contact area, decreasing close to exponentially with the distance from the edge point. This distance along the contact where the current flow is decreasing is known as the transfer length, L_{T}. This is the distance through which the carrier is continuing to travel through the semiconductor, beneath the contact, before passing into the contact. This value is used to estimate a more accurate ‘effective’ area of a contact, where current flow is occurring rather than the physical contact area given by $L_{\text{T}}W$. To insert it into the linear fit, we take

$$L_{\text{T}} = \sqrt{\frac{\rho_{\text{contact}}}{R_{\text{sheet}}}}, \tag{5.3}$$

with the conversion

$$R_{\text{contact}} = \frac{\rho_{\text{contact}}}{L_{\text{T}}W}, \tag{5.4}$$

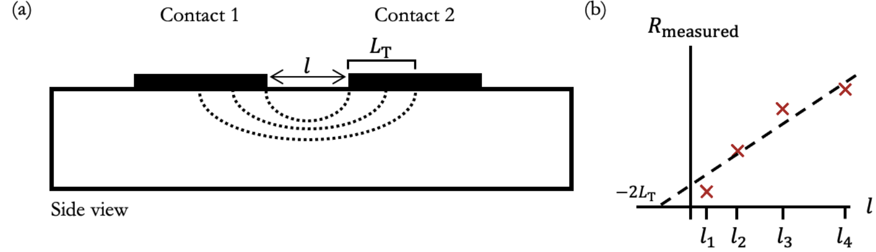

Figure 5.3: **a.** A side view of a pair metallic contacts (black) positioned over the semiconductor mesa (white), separated by length l. The dotted lines show a more realistic representation of where current enters and leaves the semiconductor, which is not exclusively at the contact edges such as in the idealised situation. In reality, the current is expected to flow through points along a distance known as the transfer length (labelled as L_{T}), with current flow decreasing almost exponentially with distance. **b.** The illustrative plot depicts the x-intercept, which is equal to $-2L_{\mathrm{T}}$.

to arrive at

$$R_{\text{contact}} = \frac{L_{\mathrm{T}} R_{\text{sheet}}}{W}. \tag{5.5}$$

As $2R_{\text{contact}}$ is the R_{measured}-intercept, setting it to be negative and dividing through by the gradient, R_{sheet}/W, yields a separation intercept of $-2L_{\mathrm{T}}$. The overall fit is shown pictorially in Fig. 5.3b.

In a similar vein to the effective area, the effective width as determined by the gradient is considered in Section 5.3.4, as a method to understand the different locations at which contact can be made (through the top, such as in a typical TLM, or the edge, where spin-polarised transport is expected).

5.2 Device Geometries and Fabrication

5.2.1 Ferromagnetic Contact Positioning: Top vs. Side Contact

In Section 3.2, it was noted that a 5/95 nm Cr/Au thermal evaporation forms the ohmic contacts on the Hall bar devices. This thickness is applied to ensure that there is sufficient Au to continuously cover the sides of the mesa, directly making contact with the conducting QW channel. However, it is also important to note that this is the assumed manner in which the ohmic contacts connect to the channel. It has not been explicitly ruled out that current also passes through pinholes in the AlSb barrier. Therefore, it is not clear how significant either the direct or pinhole contributions are. This is a far more important consideration for the Py contacts, the purpose of which is to connect to the edge transport regime of the QW. For this reason, I designed (using KLayout [9]) and fabricated multiple types of TLM contacts, to determine whether current still passes when there is no direct connection to the QW. Figure 5.4 outlines

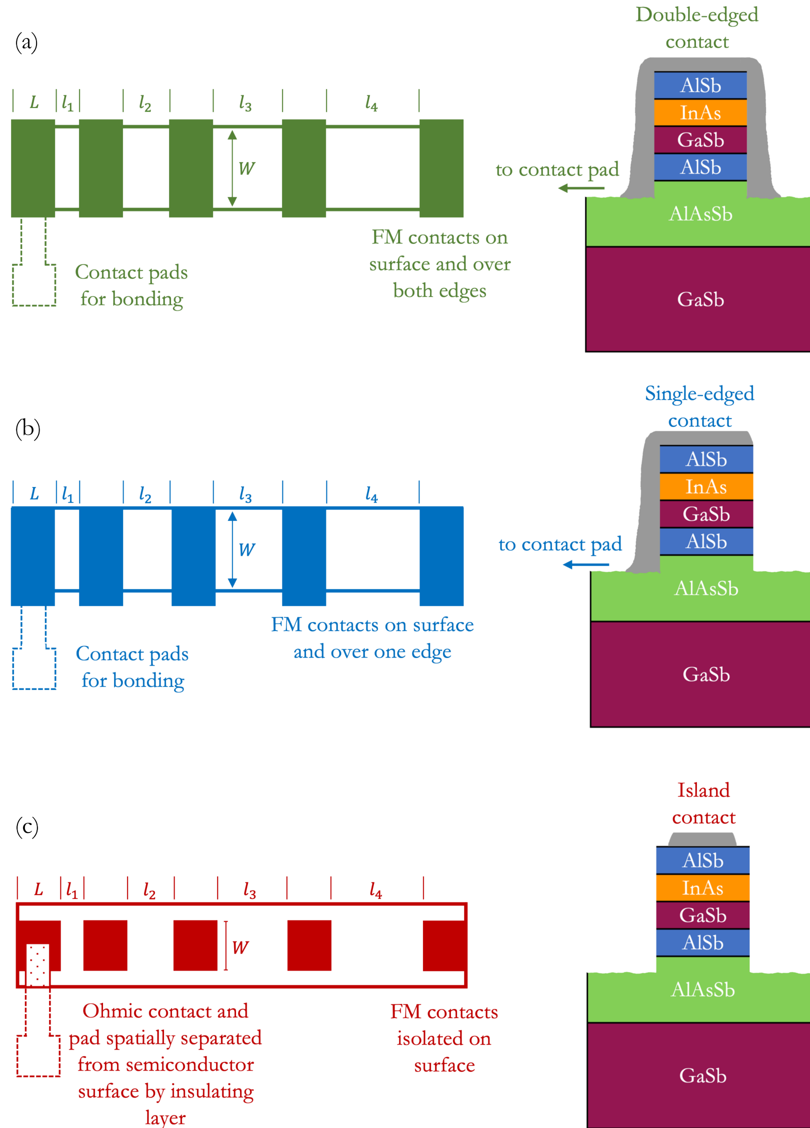

Figure 5.4: The three TLM contact types, which differ from the typical setup described in Section 5.1.2. They share the same semiconductor mesa strip, but the mesas fabricated in this project contain an upper 50 nm AlSb QW barrier above the InAs/GaSb. The QW channel can be accessed from the edge. **a.** Double-edged contact: the contacts here are situated on top of the mesa, similarly to the traditional fashion, and extend over both edges. **b.** Single-edged contact: similar to the first type, but only one edge has Py coverage. **c.** Island contact: the contacts are isolated to the top of the mesa and no edge contact is made. This means that there is a smaller value for W, which usually matches the width of the mesa. An insulating layer is required to isolate the contact leads and pad from the top of the mesa.

Table 5.1: A summary of contact dimensions and separations for each contact type. For the double- and single- edged contact types, the contact dimensions refer to the area where the Py overlaps the mesa.

Contact Type	Dimensions (μm)	Separations (μm)
Double-edged	30 × 200	40, 80, 100, 200, 400, 800
Single-edged	30 × 200	150, 330, 400, 800
Island	30 × 140	40, 80, 100, 200, 400, 800

these types. The first type (double-edged contact) shows the Py contact situated on the top of the mesa and over both edges, in contact with the AlSb on the top of the mesa and the QW. The second type (single-edged contact) is almost identical but with one edge covered by Py. The third type (island contact) is isolated to the top of the mesa, which will expose the extent of pinhole connections, and may further assist in resolving the edge contact resistances in the preceding device geometries. The contact dimensions and separations corresponding to each contact type is also summarised in Table 5.1.

5.2.2 Device Fabrication

TLM Device Mesa

The first step to forming a TLM structure, as with the Hall bar devices, is to construct the mesa. For a TLM, this is a straight line mesa, with dimensions here of 1830 μm × 200 μm. As before, the mesa must comprise the conducting InAs/GaSb material and AlSb QW layers, isolated with some buffer material, meaning the mesa etch process was identical to that of the Hall bar devices. Due to a shortage of the preferred 15 nm/8 nm InAs/GaSb QW material with $AlAs_{0.029}Sb_{0.971}$ buffer (discussed in Section 3.1.1 and used in Chapters 4 and 6), the QW structure used here differed by an additional 2.5 nm InAs (giving 15 nm/8 nm InAs/GaSb) and a 1.2 μm $Al_{0.9}Ga_{0.1}Sb$ buffer.

Permalloy Contact Deposition

The next stage of fabrication is depositing the Py contacts, using an Angstrom NexDep Physical Vapour Deposition Platform electron beam evaporator and $Ni_{0.8}Fe_{0.2}$. This is technically a form of thermal evaporation, where the deposition material is loaded into a crucible and heated by an electron beam. The beam is formed by applying a high voltage to a tungsten filament, the Joule heating of which thermionically emits electrons. The electrons are focused into a beam by the large potential difference between an anode and the filament, and an applied magnetic field directs the beam towards the crucible. The direct nature of the material heating via the beam and the water cooling of the crucible ensure that surrounding components are not heated, reducing the risk of contaminants also being evaporated and condensed. There is also

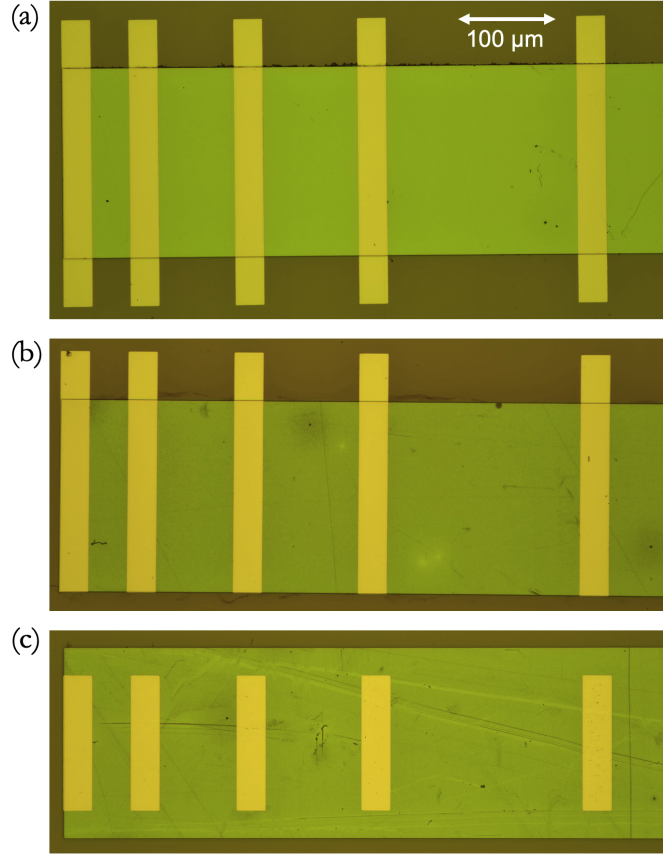

Figure 5.5: Micrographs of the result of Py deposition and lift-off. The green-tinted area is the mesa surface, the yellow areas are the Py contacts, and the brown background is the rest of the chip, where the upper wafer layers have been etched away to reveal the buffer layer. **a.** The double-edged contacts, where the entire TLM mesa width is covered, along with an additional ± 50 µm above and below the width, covering both edges to access the exposed InAs/GaSb. Edge coverage is enhanced by a ± 30 ° tilted evaporation. The total contact area is 30 µm × 300 µm, with 30 µm × 200 µm in contact with the top of the mesa. **b.** The single-edged contacts, where the top edge has 50 µm extra coverage in the vertical direction. The edge contact benefits from the same tilted evaporation as for the double-edged contact type. The total contact area is 30 µm × 250 µm, with 30 µm × 200 µm situated on top of the mesa. **c.** The island contact, where 30 µm × 140 µm of Py is contained within the top of the mesa and does not reach the edges.

reduced risk of heat damage to samples, as compared to traditional thermal evaporation. The samples are loaded into a load lock before being pumped to vacuum pressure, allowing switching between evaporations without unloading and exposing samples. It is possible to apply an Ar plasma etch step before the Py evaporation as a surface preparation method, the results of which will be discussed later in the chapter. This process is applied in-situ, meaning that the devices remain under vacuum conditions throughout, preventing the formation of interface oxides.

The Py contact deposition stage required additional testing to determine the best method by which to prepare the surface for Py deposition. The Py contact patterning uses a bilayer resist process, identical to the PMMA/S1805 process in Section 3.2, except filtered MAA 8.5 MMA EM11 is used in place of PMMA. Following this, the surface on which the Py contact will lie must be prepared to provide a clean metal/semiconductor interface. An additional, pre-loading step of O_2 plasma ashing is generally advisable to remove any unwanted resist residue from the area on which the contact is to be deposited, thus improving the semiconductor/metal interface. Although, surface oxidation can prove detrimental to an interface, which is why determining the optimal combination of O_2 and Ar plasma ashing is one of the objectives outlined at the beginning of this chapter.

The term ashing refers to the ash that forms from the photoresist residue upon exposure to the plasma, which is an oxygen plasma in this case. O_2 gas is exposed to radio waves under vacuum pressure, forming the plasma and ionising the gas. This ionisation causes free radicals of monatomic oxygen to etch the exposed organic photoresist residue, breaking it down into 'ash', which is pumped away.

O_2 molecules are relatively large and therefore highly effective at dislodging organic residue as compared with other plasma etchants. However, the plasma deposits a monolayer of oxygen onto the surface during the process, which can present issues with highly oxidisable surface materials. To prevent this oxidation, for substances that are known to be prone to oxidation (such as metals), some processes apply Ar gas with the O_2, as the Ar strips the oxygen molecules from the surface. Due to laboratorial constraints, this was not possible here. For this reason, the initial process involved only the O_2 plasma ash, on the assumption that the benefits of cleaning the resist residue would outweigh the drawbacks of surface oxidation, however this was eventually proven false. In the end, a combination of O_2 and Ar plasma ashing was required, with the Ar plasma administered at a separate fabrication step to the O_2.

The full extent of the surface cleaning is discussed in Section 5.3.2, where the optimised method of a 1 min O_2 ash (using a Diener Pico plasma asher) followed by the in-situ Ar plasma exposure for 80 s was determined. In-situ here means the Ar plasma ash was performed within the Angstrom NexDep Physical Vapour Deposition Platform immediately before the Py evaporation. Following this, 60 nm Py was deposited by a tilted evaporation, meaning that the sample was rotated on an axis in line with the longer edge of the contact. The samples were continuously tilted back and forth during the evaporation, over a $\pm$ 30 $^\circ$ range, at a rate of 5 $^\circ$/s. This was to maximise coverage

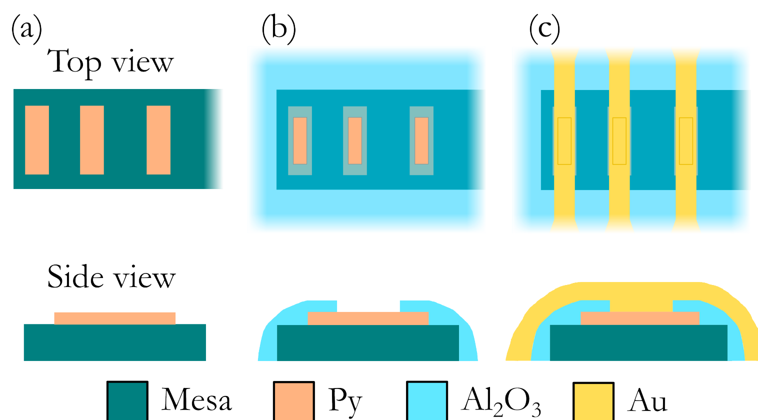

Figure 5.6: Top and short side views of mesa after Py contact deposition, when 30 nm Al_2O_3 is added to isolate the semiconductor mesa from Au ohmic contacts. The fabricated contacts were 30 µm × 140 µm. **a.** The semiconductor mesa in green, after Py contacts have been evaporated and excess Py lifted off. **b.** The mesa after the Al_2O_3 (blue) has been deposited over the entire sample surface. This also covers the Py contacts, but they are exposed in the areas where a window has been selectively wet etched by HF. The real window dimensions were 17 µm × 120 µm, and windows were centralised over the Py contact. **c.** The mesa after Au ohmic contact deposition, where sufficient Au is deposited to fill the 30 nm deep window and form a bridge to contact pads.

on the contact edges, which can be lacking when the mesa casts a shadow. The resist lift-off was then completed in acetone. Figure 5.5 shows the result, where the first type is the double-edged contact from Fig. 5.4a. The overall contact dimensions are 30 µm × 300 µm, with 30 µm × 200 µm overlapping the mesa. Figure 5.5b shows the single-edged contact result. The total contact area is 30 µm × 250 µm, with only one side harbouring 30 µm × 50 µm surplus contact with mesa edge coverage. Figure 5.5 shows the island contact position on top of the mesa, with dimensions of 30 µm × 140 µm.

Al_2O_3 Deposition and Hydrofluoric Acid Etch

The isolated contact type introduced in Section 5.2.1 creates additional complications. As the standard Au contact leads and pads must partly be positioned over the mesa to access the isolated contact, there is a substantial area of the mesa that would be in direct contact with the Au, interfering with the resistance readings for the Py contacts. This means an insulating layer is needed between the exposed mesa and the Au leads. This was achieved by depositing 30 nm Al_2O_3 by ALD. As ALD creates a uniform insulating oxide layer across the sample surface, this results in the Py contacts becoming covered in the process. Holes in the oxide layer are required, so that a thicker ($>$ 30 nm) application of Au can both form the contact pads and leads, and fill the holes in

the oxide to connect to the Py contacts. These holes can be formed by optically patterning areas to access the contacts in S1805 via the MLA, similar to the previous mesa etch process. This allows a secondary etch process, where the majority of the device is protected by a layer of photoresist, apart from a selection of rectangular holes positioned above the Py contacts. This process is summarised in Fig. 5.6. Panel (a) shows the semiconductor mesa in green, with Py contacts deposited on top. Figure 5.6b shows a uniform layer of Al_2O_3 deposited over the entire surface. The Py contacts are also shown to be covered by this oxide layer, apart from the central 17 μm × 120 μm windows where the oxide has been etched away. Figure 5.6 shows the positioning of the Au ohmic contacts on top, which are sufficiently deep to contact the exposed Py, and remain isolated from everywhere else by the oxide layer.

A buffered hydrofluoric acid (HF) etch is required to remove Al_2O_3. Due to the highly corrosive nature of the HF, a different photoresist priming approach is required to ensure the S1805 does not delaminate. The adhesion promoter used is hexamethyldisilazane (HMDS), which works by chemically bonding its own silicon atoms to oxides on the sample's surface (standard oxides formed by atmospheric levels of moisture). HMDS requires the sample surface to be highly dehydrated to strongly adhere the photoresist, as it has a tendency to bond to water molecules, which will evaporate during subsequent baking stages. The intention is for the HMDS ($[(CH_3)_3Si]_2NH$) to bond its $Si(CH_3)_3$ molecules to the surface O (rather than OH), forming a hydrophobic monolayer for improved photoresist adhesion. Meanwhile, the remaining ammonia evaporates.

Due to the need for dehydrated conditions, the preferred primer deposition method is to vapour deposit the HMDS under vacuum (in a vapour prime oven). It is not typically advised to spin-coat HMDS, since this deposits a thicker film which harbours residual moisture and is not chemically bonded to the surface oxide to form the desired monolayer. The excess HMDS means that substantial ammonia will evaporate upon the soft-bake instead, diffusing through the resist and chemically modifying the resin component near the substrate surface. This creates a film of undeveloped photoresist, leading to a failed resist process or unpredictable exposure results with compromised resolution.

Due to the implementation of a vapour prime oven not being possible in our laboratory, the process outlined here relies on a workaround whereby the HMDS deposition is performed in the usual spin-coater, which is as follows:

1. Pre-bake sample at 120 °C for 1 minute, to dehydrate the surface.

2. Allow sample to cool.

3. Spin coat 2-3 pipette drops of HMDS at 4000 rpm.

4. Bake sample at 120 °C for 1 minute, to drive off unbonded HMDS.

5. Allow sample to cool.

Table 5.2: Hard-bake temperature and duration combinations tested on S1805 (with HMDS primer) for HF etch.

Combination	Temp. (°C)	Duration (min)
1	130	5
2	130	10
3	135	15
4	145	15
5	145	20

6. Apply jet of IPA during 4000 rpm spin, to remove HMDS residue that is harmful to subsequent resist coating.
7. Bake sample at 120 °C for 1 minute.
8. Allow sample to cool.
9. Thoroughly clean spin coater with IPA.
10. Spin coat S1805 at 3000 rpm and bake at 115 °C for 1 minute.

Following resist exposure and developing, a further post-bake step was employed to harden the resist for additional protection against delamination and damage to the Al_2O_3 layer below. In general, a higher post-bake temperature and/or longer duration will improve the strength of the resist coating when submerged in the HF. However, the limiting factor is the ease of removal following the HF etch. To determine the ideal process, temperatures between 130 °C and 145 °C, and durations between 5 minutes and 20 minutes were tested on Si wafer with a 30 nm Al_2O_3 surface. The combinations are given in Table 5.2.

The Si samples were etched in buffered HF for 30 s (the required etch time for the devices), after which the resist was cleared in acetone at 45 °C. Combinations 4 and 5 resulted in irremovable resist coatings. Combination 3 required $\sim$ 1 hour of soak time to remove the coating, which was not a practical timescale. Neither combination 1 nor combination 2 showed visible damage to the Al_2O_3 layer (at 100 $\times$ zoom), therefore, combination 2 was chosen as it offered the most security without compromising the resist removal.

In order to ensure that the Al_2O_3 on the combination 2 sample had sustained no damage and no resist delamination had occurred, this sample was subjected to an SF_6 plasma etch. Applying SF_6 under high pressure causes F radicals to etch isotropically, amplifying any pre-existing holes in the Al_2O_3. This was performed in a PlasmaTherm Vision 310, operated by Dr Mark Rosamond, Leeds Nanotechnology Cleanroom, University of Leeds. The purpose of this machine is to conduct plasma-enhanced chemical vapour deposition rather than plasma etching, but the system is configured with SF_6 as a cleaning gas which was preferable for this purpose. This

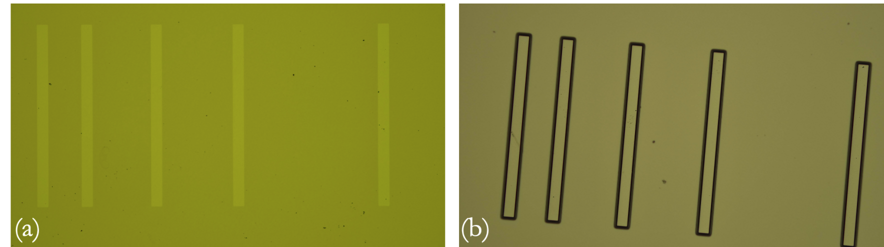

Figure 5.7: Before and after SF_6 plasma etch micrographs of the Al_2O_3-coated Si test sample. The rectangular HF etched areas are 17 µm × 288 µm. **a.** Si sample surface after HF etch and resist strip in acetone. The lighter sections are where Al_2O_3 has been etched away by HF. Samples were studied at 100 × zoom and under dark field, and there was no visible damage to the areas that were covered by resist. **b.** The Si sample after SF_6 plasma etching. This process also did not reveal any damage to the resist-covered areas.

was due to the setup of the system, in which the substrate is located on a grounded electrode, which is not the case with purpose-built reactive ion etch systems. This meant that the sample did not sustain ion bombardment, which would have physically etched the surface, reducing the contrast between the potentially HF damaged areas and the undamaged areas.

Following this process, there continued to be no visible damage to the resist-covered areas, so it was concluded that the altered HMDS prime process combined with the combination 2 hard-bake was successful, and this process was applied to the InAs/GaSb device fabrication. The samples were then etched in buffered HF etch. Given that the buffered HF has an etch rate of 1.2 nm/s, the samples were etched for 30 s to ensure the Al_2O_3 had been completely removed in the chosen windows, without delaminating the resist. The results are shown in Fig. 5.8. The other contact types, which do not necessarily require an insulating layer, also received the Al_2O_3 layer. This was due to ease of fabrication, as it facilitated device processing in batches on the same wafer sample. In this instance, windows were etched 6 µm and 6.5 µm from the short and long Py contact edge respectively.

Ohmic Contact Deposition

Ohmic contacts were then patterned following the same bilayer lift-off process as with the Py contacts, with the Al_2O_3 ensuring spatial separation from the semiconductor mesa. To ensure that there was sufficient Au to fill the windows in the Al_2O_3 and make contact with the Py contacts, a larger amount of Au was thermally evaporated. This was dictated by the maximum amount of Au that could be loaded into the thermal evaporator, making the new deposition 5 nm/(130 - 160) nm Cr/Au. The final result is shown in Fig. 5.9.

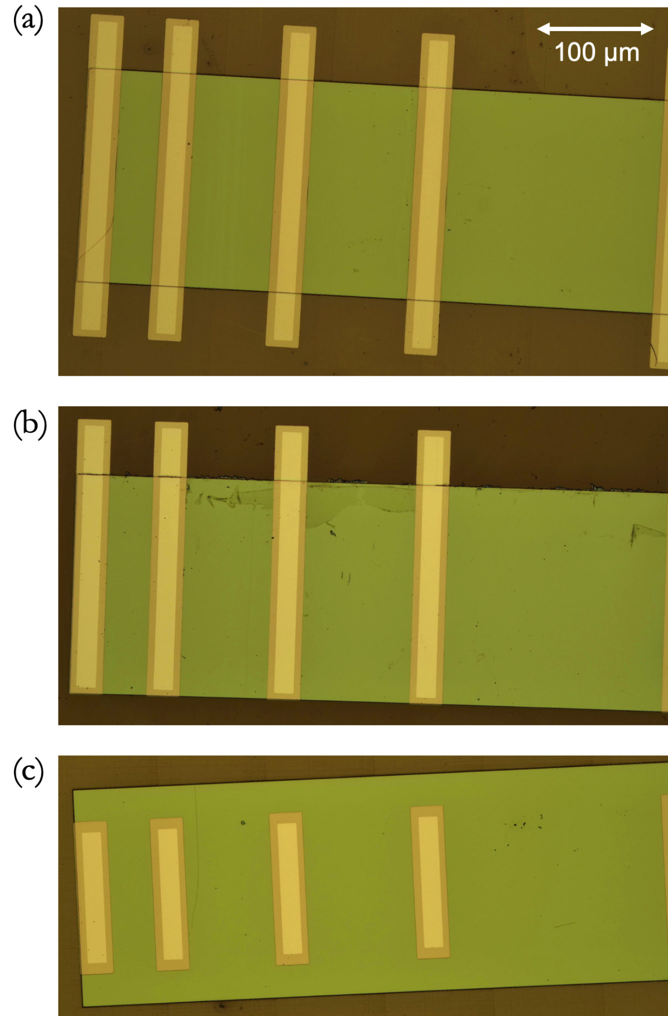

Figure 5.8: Micrographs of the result after Al_2O_3 deposition and HF etch, with scale shown. The darker yellow colour is the Py covered by a layer of Al_2O_3, and the lighter yellow is the exposed Py, after having been wet etched. In each case, there is a border of unexposed Py. For every device, this border is 6 µm from the lower and upper contact edges, and 6.5 µm from the side edges. **a.** The double-edged contact type, with Py extending over the top of the mesa and down both edges. **b.** The single-edged contact type, with Py extending over the top of the mesa and down one edge. **c.** The island contact type, with the Py confined to the top of the mesa only.

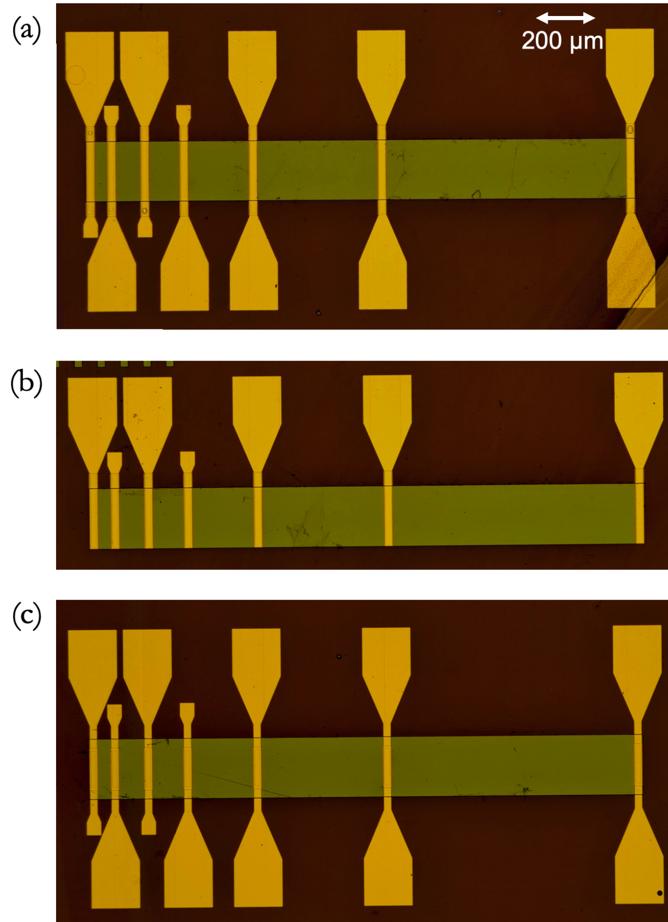

Figure 5.9: Micrographs to show the final result of device fabrication for each contact type. For the double-edged and island contact types, two-sided contact pads were fabricated to measure continuity. Where possible, these pads were fabricated to the dimensions required for accurate wire bonding. Where space was limited, smaller contact pads were fabricated, should further measurements be required and implemented by alternative methods. In each case, the definition from the Py contacts and windows through the Al_2O_3 can be seen through the definition in the Au. **a.** The double-edged contacts type - the outline of the Py contact underneath can be seen at the narrowest part of the tapered lead to the contact pad. This contact harbours the double-sided contact pads for continuity checks. **b.** The single-edged contacts, which also have single-edged contact pads. This is due to the Py contact only running up the top edge of the mesa. As a precaution, the contact pads were not extended to the lower edge, since no edge contact is supposed to be made here. This was also to conserve space on the chip. **c.** The island contact - the outer side edges of Py can be seen under the Al_2O_3.

5.3 Transmission Line Model Results

5.3.1 Experimental Setup

Measurement Setup

The resistance measurements between increasing contact separations were performed with a Keithley 6221 current source and a Keithley 2182 voltmeter in a two-probe setup. As mentioned in Section 3.3, the samples were mounted onto ceramic chip carriers and connected to the measurement apparatus via the brass holder and probe stick. Low temperatures were achieved by positioning the probe stick into a dewar containing liquid helium (dip probe setup). It was positioned so that the sample was situated in the cold gas above the liquid He surface, with measurements occurring at 4.3 - 4.8 K.

Specific Transmission Line Setup

An important consideration is the extent to which the classic TLM described in Section 5.2.1 relates to the actual geometry. This description concerns a semiconductor strip with metal contacts bridging the entire width. This, for the most part, maintains a 1D system with current flow and transfer length in the same direction. However, it becomes a higher-dimensional system when considering the contact geometries used here.

As previously mentioned, these geometries were deliberately implemented to deduce whether current is reliably confined to the edge junctions, or if there is also a significant conduction contribution from the top, via pinhole sites in the AlSb. Therefore, it is worth considering the extent to which the standard TLM does not apply here. Even in physical systems that aim to replicate the standard TLM geometry, it is recognised that the transmission line width will not equal the fabricated contact width, which will manifest in the characteristic values derived [63]. The model can be used to calculate an 'effective width', which gives a more accurate depiction of how connected the contacts are to the channel, by substituting measured results into Equation 5.1 and solving for W (which originally referred to the fabricated width). In this setup, this is a more important consideration.

The double- and single-edged contact types are comparatively similar to the simple TLM, but the situation is complicated by the edge connection of the contacts. This introduces an effective contact in another plane. Nevertheless, the fact that the TLM devices are ungated, and therefore very distant from charge neutrality in the electron dominant regime, ensures that the primary transport is not edge transport. This means that the edge contact should not be exposed to a significantly larger charge density than that of a contact through the top of the transmission line. Although, one must recall that there is 50 nm AlSb at the top junction. If any significant current flow is occurring through this path, it is still likely to be through defect sites. With charge transfer confined to pinhole defects above and junctions in a different plane to that of the model, any derived values ought to be interpreted as a guideline. In the case of

contact confined to the side(s), the 'effective width' becomes a measure of maximum current dispersion perpendicular to the flow between contacts.

I have been unable to find a similar model that serves these constraints. That is not to say that 2D TLMs have not been formulated: there exist a number of 2D models, where current flow perpendicular to the contact area is accounted for, but they still do not suit systems with junctions in the perpendicular plane [63]. As for the top island contacts fabricated here, the situation continues to be complicated by the fact that any conduction present is expected to be defect-based.

Overall, the traditional TLM setup introduced in Section 5.1.2 remains the most relevant geometry to the devices presented here. Depending on whether edge or top conduction is assumed, the effective width term may be better interpreted as a measure of current dispersion, or proportion of width affected by pinhole defects. The I-V behaviour of the island contact devices compared with the side contact devices gives insight into the dominant conduction path.

5.3.2 I-V Characteristics of Contacts and Interface Quality

Whilst the overall TLM analysis comprises the average resistance for many contact pairs, the I-V behaviour of a single contact pair is the first indicator of the metal to semiconductor interface quality, which was needed to ascertain which combination of semiconductor surface cleaning methods was optimal for Py contact deposition.

Semiconductor/Py Interface Tests

As mentioned in Section 5.2.2, a key target of the device fabrication was to produce a clean Py/semiconductor interface, which can be hindered by oxidation and resist residue. It was also mentioned that optimisation of the correct O_2 and Ar plasma etch process was required, which involves the balancing of effective resist residue cleaning by O_2 molecules with the subsequent oxidation this causes, by following the O_2 plasma ash stage with an Ar ion etch under vacuum. To determine how detrimental possible photoresist residue or oxidation were, and to determine the best method(s) for producing a clean interface, a variety of semiconductor surface preparations were carried out before the Py deposition.

It was initially thought that the standard procedure of applying an O_2 ash before metal contact deposition would clear photoresist residue to improve the Py to semiconductor interface, however, this has the potential to promote unwanted surface oxidation, leading to interface oxide impurities. For this reason, devices were fabricated both with and without the O_2 ashing step. It was also acknowledged in Section 5.2.2 that a higher standard of ashing procedure exists, which administers an Ar plasma during the O_2 plasma ash. Whilst this was not possible in our laboratory, it was possible to replicate the effect by exposing the devices to Ar plasma during the usual deposition of the Py in the electron beam evaporator. In fact, this method involving two individual ashing procedures was reported in Ref. [62], to fabricate Ta/(In/As) junctions. Here, this was

Table 5.3: An outline of the four possible ashing combinations tested, with sample labels given for ease of reference.

Sample	O_2 Plasma	Ar Plasma
A	No	No
B	Yes	No
C	No	Yes
D	Yes	Yes

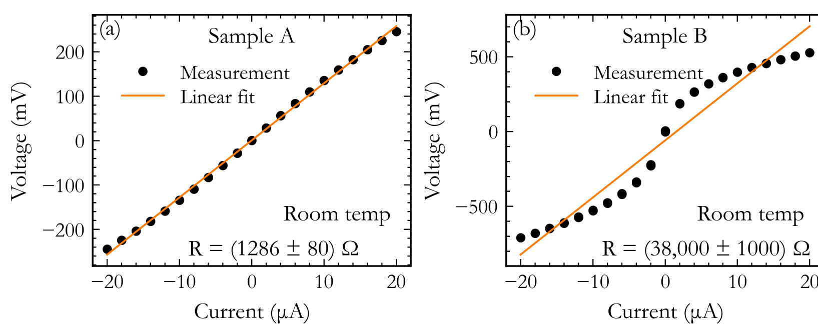

Figure 5.10: 400 µm contact separation I-V curves for different sample preparations at room temperature. The raw I-V data is plotted in black, and the linear fit plotted in orange. It is a least squares fit, with uncertainties from the standard deviation. I-V curves shown in this section were not derived from the island type of contact. **a.** Sample A preparation, with no ashing steps. This is demonstrably better than the interfaces yielded from the O_2 ash only preparation, however, the result still shows some visible non-linearity in the plot. **b.** Sample B preparation, employing the O_2 ash step. This produces a highly non-ohmic junction, making it the worst preparation and confirming that oxidation from the O_2 plasma ash is more damaging than allowing resist residue and atmospheric oxidation to remain (as a result of no surface cleaning methods).

applied for 80 s immediately before the Py deposition began, maintaining the vacuum conditions. Devices were also tested with and without this procedure, meaning a total of 4 combinations (with/without O_2 ash and with/without Ar plasma) tested on the Py contacts. The combinations are also given in Table 5.3.

Reference devices with Au contacts throughout (no Py contacts) were also fabricated, to ensure that the method applied to the Py contact devices is capable of producing a functional TLM device. For the reference devices, both the O_2 ash and in-situ Ar plasma etch were applied to prepare the semiconductor surface before the Au deposition (which was performed at the same thickness and tilt conditions as the Py deposition). The results of the Au reference devices are discussed at the end of this subsection.

The I-V results for 2-probe measurements between contact pairs, for both island

Table 5.4: Average proportional resistance uncertainty at room temperature and low temperature for each sample.

Sample	Average Proportional Resistance Uncertainty (%)	
	Room Temp.	Low Temp.
A	0.5	
B	2	
C	0.007	0.7
D	0.04	0.4

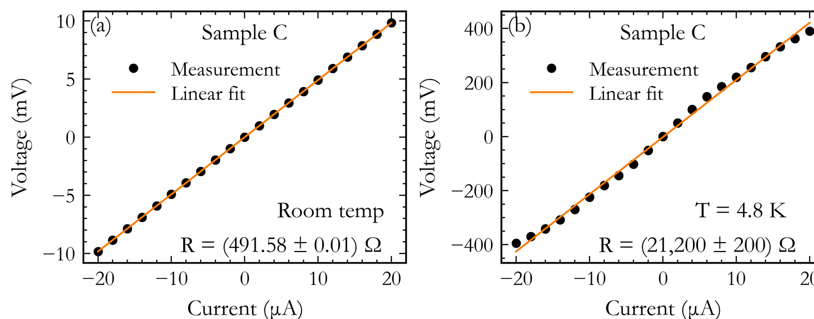

Figure 5.11: 400 μm contact separation I-V curves resulting from Sample C preparation. **a.** Room temperature I-V sweep, showing strong linearity. **b.** 4.8 K I-V data, showing deviation from linearity at lower temperature, likely due to fewer available conduction channels.

contacts and edge contacts, were analysed to assess the resulting quality of interfaces. An example I-V result for Sample A is shown in Fig. 5.10a. The result of this interface preparation method proved to be reasonable but not optimal, as shown by the relatively clear non-linearity, which was shown by all results for this preparation to some extent. For the sake of testing the relationship between contact separation and resistance in this device, resistances were calculated from a linear fit, which understandably carries a high level of uncertainty when non-linearity is strong. When comparing the resistances for different separations along a device, there was no clear relationship of note, indicating that interface contaminants and/or atmospheric oxygen exposure dominate the resistance measured.

Figure 5.10b shows an example I-V result for Sample B, where only O_2 plasma ashing was applied. Perhaps surprisingly, the ohmic performance is visibly worse for this interface preparation, revealing that O_2 ash cleaning alone oxidises the surface to a degree that is more detrimental to the ohmic behaviour than allowing organic residue on an atmospherically oxidised surface. In short, preparing the surface by oxygen plasma ashing is worse than doing nothing, although neither result is exemplary.

Sample C demonstrated the most ohmic interface at room temperature of all pre-

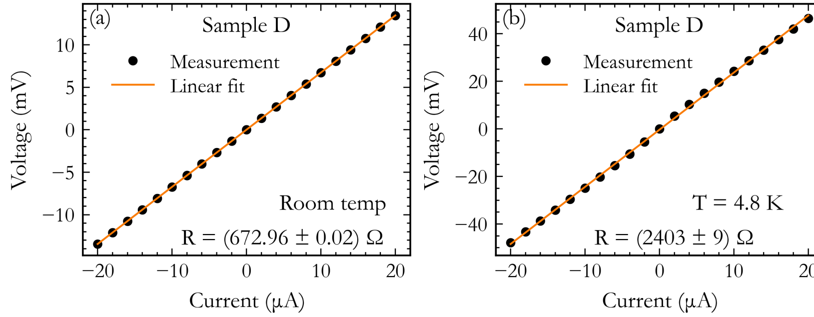

Figure 5.12: 400 μm contact separation I-V curves resulting from Sample D preparation. **a.** Room temperature result, showing high linearity. **b.** 4.8 K result, showing a small deviation from the linear fit (corresponding to 0.4 % standard uncertainty here). This result confirms that the O_2 and Ar plasma ash combination produces the best ohmic performance, particularly as low temperature performance is the priority.

parations, with an example shown in Fig. 5.11a. The average proportional resistance error, derived from the standard deviation in the linear gradient and averaged across all I-V measurements apart from the island type of contacts, was 0.007 %. This is shown in Table 5.4 amongst the uncertainties of the other samples. The I-V traces measured for this interface preparation also yielded resistances in a more repeatable range than the previous two preparations. However, upon cooling to T = 4.8 K, the result is not as favourable, displaying visible non-linearity. This is likely due to the current paths present at room temperature being unstable, and is the reason for first confirming a reasonably ohmic I-V at room temperature before committing to cooling the device.

Sample D I-V results are shown in Fig. 5.12. Focusing first on the room temperature result in panel (a), it is visibly linear and the gradient has a standard uncertainty of 0.002 %. The average uncertainty for all Sample D measurements at room temperature, given in Table 5.4, was 0.04 %. This is a good result compared to Samples A and B, and it would suggest that the Sample C surface treatment makes a better ohmic contact, were it not for Sample C's poorer performance at low temperatures. Sample D shows the highest linearity under low temperature conditions, as confirmed by its average uncertainty of 0.4 %, and demonstrated by an example I-V result in Fig. 5.12. Sample D's resistances also showed the most convincing linear dependence on contact separation. For these reasons, the O_2 ash followed by the physical vapour deposition in-situ Ar ion ash became the standard surface preparation procedure for Py contact depositions.

Clearly, the duration of both ashing stages is also important, as it can affect the cleanliness of the result, the possibility of unintentional etching (caused by the O_2), and the extent of oxidation immediately before the Py is deposited. Ideally, extensive testing on the respective exposure durations of each plasma would have taken place (were this not an expensive and time-consuming process), to ensure that they were optimal for

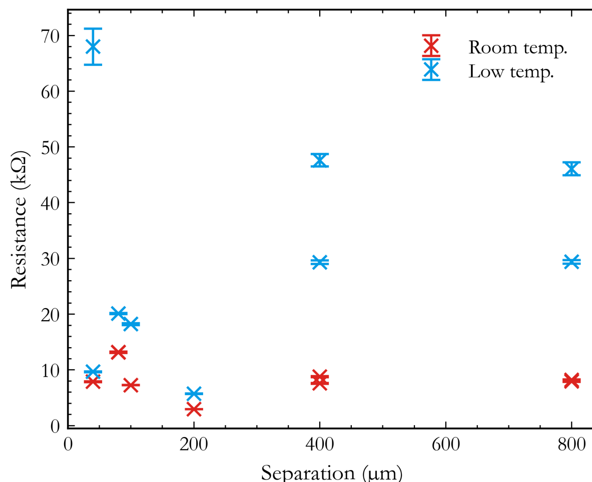

Figure 5.13: Contact separation dependent resistance results for the island contact measurements, at room temperature and 4.8 K. It is lacking a convincing correlation with separation, meaning that the resistances have far greater dependence on the extent of pinhole sites. The resistances are considerably higher than their edge contact counterparts in the same temperature conditions. For the low temperature results, the vast majority of resistances are in the tens of kΩ range, compared with the single-edged contact results (Fig. 5.15b), which fall primarily in the > 3 kΩ range. Some points here are overlapped.

our particular situation. In future, some adjustment of the plasma ash timings would be advisable, in case the Py/semiconductor interface quality can be optimised further. However, as it stands, I have ensured that the specific O_2/Ar process followed yields higher quality interfaces at low temperatures than processes omitting either (both) constituent step(s).

5.3.3 Location of Contact

Various contact geometries were constructed to ascertain whether contact is made primarily through the edge of the mesa, directly into the InAs/GaSb QW layers, or whether the conduction through pinhole defects in the AlSb barrier is more significant. The island type of contact, where the Py is isolated to the top of the mesa, was the most revelatory of the geometries tested with regard to contact location.

Figure 5.13 shows the resistance measured for each of the contact separations for the isolated contact type (fabricated following the optimal interface preparation method determined in Section 5.3.2). The results are generally high, and absent from the plot are a quarter of the I-V results (from both temperatures) that could not be plotted, as they showed an open circuit. The wire bonds to these contact pairs were re-bonded and tested repeatedly, indicating that the broken connection was due to the device

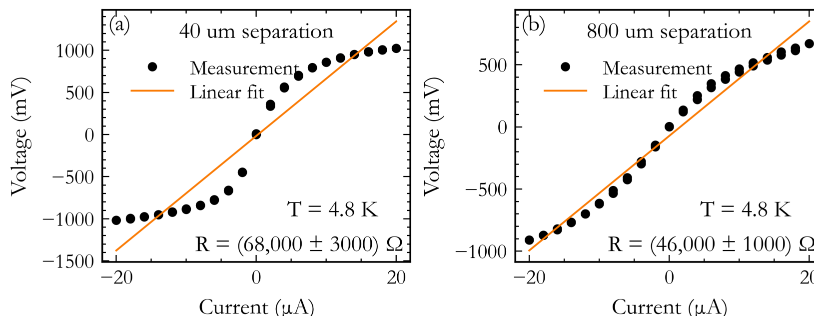

Figure 5.14: Island contact type I-V curves (using Sample D optimal interface preparation) measured at 4.8 K. **a.** 40 μm contact separation, showing strong non-linearity. The resistance is higher than that of the 800 μm separation measurement in panel (b), indicating that the limited conduction through the AlSb barrier is the main influence on I-V performance. **b.** 800 μm contact separation. The result is more linear than that for the 40 μm separation, as well as lower resistance, suggesting that there are more pinhole defect channels available

itself. Those that retain their connection display high resistances, which don't display an obvious separation dependence, and highly non-linear I-Vs, as shown in Fig. 5.14. When combined with the loss of connection for many contact pairs, this illustrates that contact is not made reliably through the AlSb barrier. Although, this is not to say that contact through the top of the channel is non-existent. Not every contact was electrically cut off from the channel upon cooling, and high resistance results persist in the contacts that cover the mesa edge. This suggests that connection is reliably, but not exclusively, made directly to the QW at the mesa edge.

5.3.4 Contact Resistance Results

Once it was determined that the combined O_2 and Ar plasma ash process produced the most reliable interface, and the interface of note was located at the QW edge, these conditions were combined to determine a contact resistance. The measurements were performed on the single- and double-edged contact types. The measured resistance results span separations of 40 μm, 80 μm, 100 μm, 150 μm, 200 μm, 330 μm, 400 μm and 800 μm.

The separation-dependent analysis was performed on the single-edged contact type only, for both room temperature and (4.3 - 4.8) K. As explained in Section 5.1.2, a linear fit applied to these results will provide an average contact resistance, which is half of the measured resistance intercept value for a single contact.

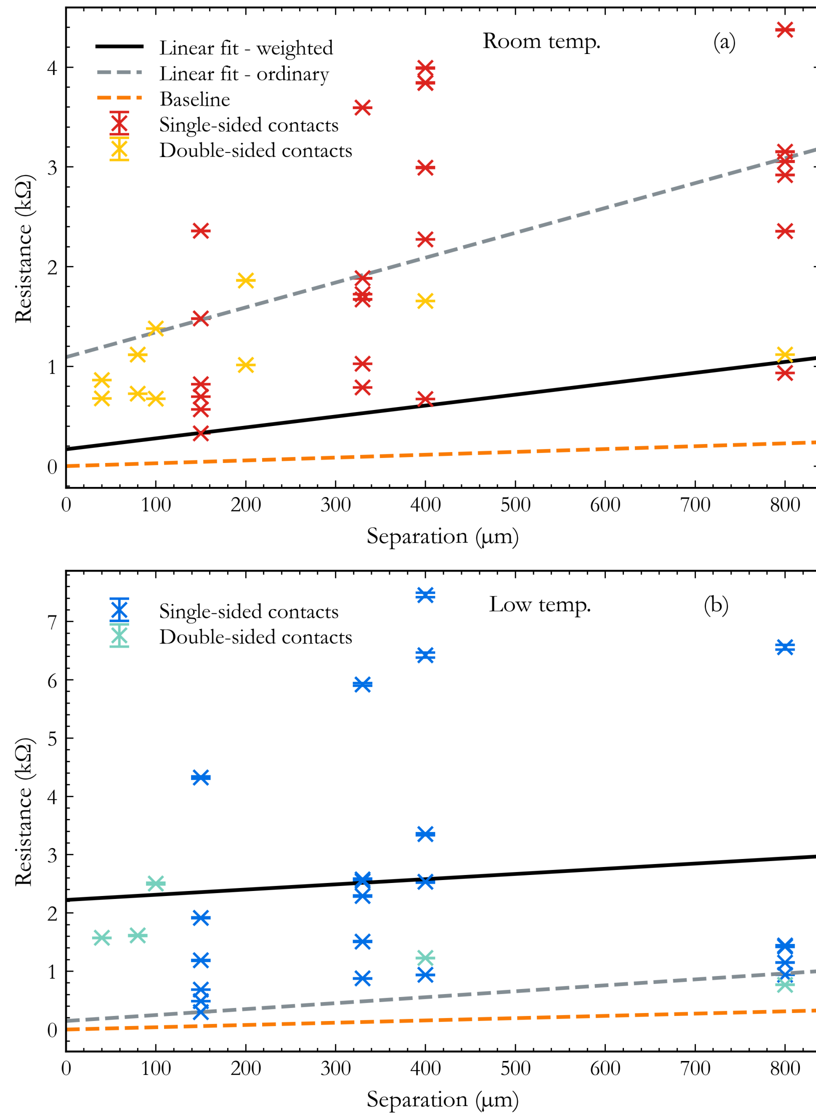

Figure 5.15: Weighted and ordinary linear fits for room temperature (**a.**) and (4.3 - 4.8) K (**b.**) conditions. The line key applies to both plots. The baseline is determined by the estimated resistance of the channel and does not include the contacts. The corresponding resistances are given in Table 5.5.

Table 5.5: Summarised least squares linear regression results of resistance-separation TLM graphs for room temperature and low temperature (4.3 - 4.8 K), where contact resistance is determined via the resistance axis intercept. Effective width and transfer length are also given, as determined by the gradient and separation axis intercept respectively.

Temp. Range	Fit Type	R_{contact} (Ω)	W_{eff} (μm)	L_{T} (μm)
Room	Weighted	80 ± 10	52 ± 7	80 ± 10
	Ordinary	500 ± 200	23 ± 9	200 ± 100
Low	Weighted	70 ± 10	76 ± 9	70 ± 10
	Ordinary	1100 ± 500	100 ± 200	1000 ± 3000

Double-Edged Contact Results

Presented in Fig. 5.15 are the room and low temperature results for both the double- and single-edged contact types. The best fit lines (discussed below) are derived only from the single-edged contacts. This is because the double- and single-edged contact data are not directly comparable with one another, given that the double-edged type has twice the edge contact area.

The data for the double-edged contact is lacking due to material scarcity. For this reason, I have not applied its own TLM analysis. However, the individual resistances are worth considering. Assuming no pinhole conduction through the AlSb layer and consistent resistances across the Py/(InAs/GaSb) barrier, these resistances should be half of the corresponding resistances for the single-edged contact. Primarily due to the difference in separations tested for each contact type, it is difficult to make a direct resistance comparison. In the 400 nm and 800 nm cases, where there are resistances for both contact types, it is still difficult due to the wide spread the resistances occupy. Although, in a qualitative sense, the result is consistent with the prediction, in that the resistances are generally lower and do not exceed the highest single-edged contact resistances.

Single-Edged Contact Results

As previously mentioned, the single-edged contact resistances were processed as per the TLM model to determine an average contact resistance. The effective width and transfer lengths were also determined from the gradient and separation-axis intercept.

Multiple approaches to fitting the data were applied, as it was not obvious where the best fit would lie. These results are presented in Table 5.5. The first approach I tested was a statistical treatment of the data, applying an inverse variance-weighted fit, with the variance derived from the standard deviation in each individual linear I-V fit that constitutes a point on the wider separation-dependent data. This line is shown in Fig. 5.15, and results in an average contact resistance of (80 ± 10) Ω at room temperature,

and (70 ± 10) Ω at 4.8 K. The best fit line is situated at lower resistance values due to the uncertainties of which being in the order of 0.01 %, which is considerably smaller than those of the higher resistance points, which are in the order of up to 1 %. This result indicates the successful fabrication of relatively low resistance Py contacts. The very slight decrease in resistance upon cooling indicates a close balance between the semiconducting and metallic parts of the conduction path.

Further to this, the gradient of the fit, along with the known sheet resistances, can be used to determine an effective contact width, in line with Equation 5.1. This is the width perpendicular to the direction of current propagation that gives insight into current dispersion and/or the extent of contact made with the channel, depending on which conduction sites are acknowledged. In an idealised situation, and crucially for the traditional TLM which does not apply here, W in Equation 5.1 would equal the fabricated width. Assigning W_{eff} to avoid confusion, and applying the gradient from each weighted fit, yields W_{eff} values of (52 ± 7) μm and (76 ± 9) μm for room and low temperatures respectively. As the nature of the weighting gives precedence to the lower resistance values, which are deemed a result of connection at the QW edge, this W_{eff} value appears to signify the extent of current dispersion in the W direction. The method returns reasonable values for this, given that they lie within the confines of the TLM device channel width. Were this W_{eff} more similar to a measure of conduction coverage from above, it would be expected to diminish at low temperatures, along with the availability of pinhole defect conduction sites. This is consistent with the fact that the weighting favours the lower resistances, assumed to be a result of edge-confined conduction.

One pitfall of the statistical approach is that, by using the size of the standard deviation as a measure of reliability, it treats data with a larger uncertainty as a 'bad straight line' rather than a non-ohmic relationship, which is physically valid and describes a different type of barrier. For this reason, weighting the result towards the lower resistances may not be the most appropriate representation of the contact resistance, since even contact isolated to the QW edge is not guaranteed to be completely ohmic. The ordinary (unweighted) fit result for the room temperature data gives a contact resistance of (500 ± 200) Ω, and for the 4.8 K data it gives (1100 ± 500) Ω. The higher contact resistance value for the low temperature data is expected when more weight is given to resistances from pinhole site conduction. However, if two distinct sources of resistance are to be considered, an equal weighting of every data point is also not a solution. This is reflected particularly in the effective width of the low temperature contact, which is (100 ± 200) μm, beyond the constraints of the transmission line. The transfer length results are also included in Table 5.5, and indicate that these results cannot be the perfect description of the contact behaviour without resolving the conduction via the AlSb barrier from the conduction at the QW edge.

As a reference point, both plots also include a 'Baseline'. This is where the TLM fit would fall were the contacts zero-resistance (therefore, zero-intercept), meaning it is derived from an estimate of the resistance of the channel. The gradient is calculated

by dividing the known sheet resistance of the channel by W, the fabricated contact width. For this reason, it is not fully representative of the system, as it follows the same assumptions as the standard TLM layout. However, it gives perspective to how high the measured resistances are.

Au-Based Devices

For the sake of comparison, full Au replicas of the Py devices described here were also fabricated. This followed an identical fabrication procedure until the Py contact evaporation stage was reached. At this point, 60 nm Au was deposited in the same tilted manner as described previously, using the same electron beam evaporator. The same O_2 ash and in-situ Ar plasma etch applied to the Py/semiconductor interface were applied to the Au/semiconductor interface. Following this, the fabrication procedure continued to be identical to that of the Py devices.

The purpose of the Au-based devices was to establish whether the fabrication method was capable of producing TLM devices with repeatable resistances that were linear in contact separation. Fig. 5.16 shows the room and low temperature results, which were considerably more consistent and linear than the Py results, meaning that the wide spread of Py resistances is not a result of issues with the device itself.

In the room temperature case (Fig. 5.16a), both the weighted and ordinary linear fits are shown. These fits apply to the single-edged contacts only, for consistency. The resulting contact resistances were (-15 $\pm$ 2) Ω and (20 $\pm$ 20) Ω respectively. The negative result in the weighted fit demonstrates an underestimation of the uncertainty by the method applied to the Py contacts, which uses the standard deviation in the individual I-V results. The double-sided contact resistances also lie between the weighted and ordinary fit lines, which is unusual given the resistance ought to be halved. This demonstrates that the optimised interface preparation method could still be improved upon, with extended Ar plasma ashing being the most obvious potential improvement.

The low temperature result (Fig. 5.16b) shows a similar situation, with a negative intercept for both the weighted and ordinary linear fits. This lead to a weighted fit contact resistance of (-17 $\pm$ 4) Ω and an ordinary fit contact resistance of (-11 $\pm$ 4), an unphysical result both in terms of the negativity in resistance and the fact that the baseline channel resistance exceeds it. Again, this suggests that a greater source of uncertainty than the standard deviation in the I-V curves is present. Despite the lack of a consistent, physically valid contact resistance, all measured resistances fall considerably nearer to the estimated channel resistance (marked as 'Baseline'), demonstrating low resistance TLM contacts with linear resistance-separation behaviour.

5.3.5 Conclusions

This chapter demonstrates successful fabrication of novel Py/(InAs/GaSb) junction transmission line devices, where I have also optimised the Py deposition process to produce reliably ohmic contacts. These contacts appear to be confined to the edge

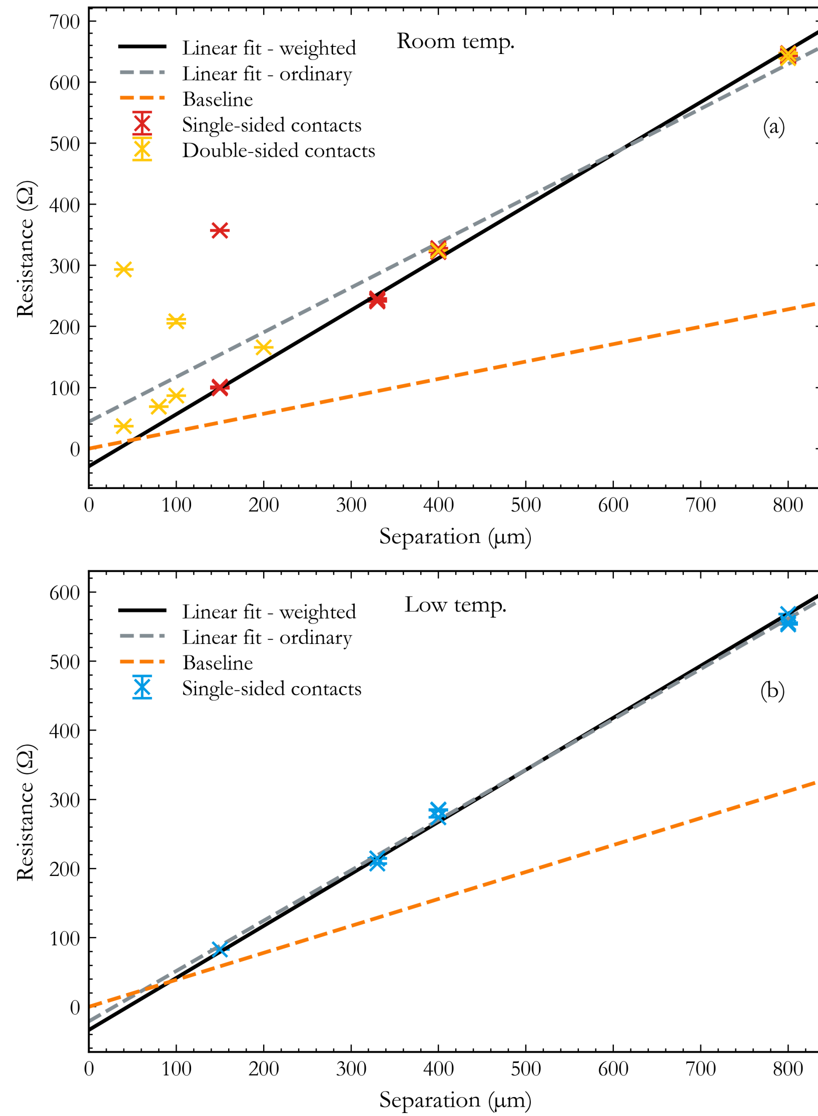

Figure 5.16: Room temperature (**a.**) and (4.3 - 4.8) K (**b.**) resistance measurements in separation, displaying a more consistent and linear result than that of the Py contacts in both instances, confirming that this fabrication method is capable of producing linear TLM behaviour.

when in the < 10,000 Ω resistance range, with the standard TLM linear equation applied to determine average contact resistances. This was a promising result for future fabrication of Py/(InAs/GaSb) junctions in smaller device setups, such as that given in Chapter 6.

Chapter 6

InAs/GaSb Devices with Integrated Ferromagnetic Contacts: Nano-Scale Transmission Lines

This chapter follows the fabrication and implementation of the final type of device in this thesis, through which I have demonstrated successful Py contact fabrication at the mesa edge, with roughly 10 µm × 15 µm Py in contact with the mesa, situated at 20 µm down to nano-scale separations. These devices were another set of TLM-style devices, the purpose of which was to investigate contact resistances and other transport characteristics of smaller Py contacts confined to the edge. The average edge contact resistance is estimated to be (240 ± 40) Ω for (4.3 - 4.6) K. Contacts with few micron- and nano-scale separations are more akin to contacts required for possible spin-polarised current injection experiments in the future.

I present the novel fabrication procedure, including details of refinements. Throughout the method, I also propose easily implemented changes to the procedure that ought to improve the statistical success of functioning contact pairs. My design includes trial features, which can benefit future experiments using Py/(InAs/GaSb) junctions. The success of these features is discussed in the context of future work in Chapter 7.

6.1 Design Features

The devices were fabricated on the same wafer as that of the Hall bar devices in Chapter 4 (12.5 nm/8 nm InAs/GaSb with $AlAs_{0.029}Sb_{0.971}$ buffer). The crucial design differences between the final devices presented here and the larger TLM-style devices in Chapter 5 are:

1. **Smaller contact separations:** contact separations in Chapter 5's devices were largely in the hundreds of microns. The contact separations in the design here begin at the nanoscale, covering separations of 200 nm, 400 nm, 600 nm, 800 nm, 1 µm, 2 µm, 4 µm, 10 µm and 20 µm.

2. **Smaller contact area:** the contact areas for the previous devices were relatively large, with (4200 - 6000) µm^2 fabricated onto the mesa. By contrast, the contacts here are identical to each other and have a total contact area of 360 µm^2, with 95 µm^2 overlapping the mesa. Although, in both cases, the effective areas are as small as 0.205 µm^2 if there is negligible contact through the top of the mesa.

3. **Future device features:** the TLM devices presented here contain additional fabrication features that could be applied to future devices for detecting spin-momentum locking in the QSH edge transport regime. The first of these is double-pointed 'boat' shaped contacts (see Fig. 6.1), for magnetisation control, and the second is a trial top gate, which would be used to tune the system towards the QSH state and is discussed in Chapter 7 regarding future work.

4. **Voltage probes closer to contacts:** as shown in Fig. 6.1, the voltage probes remain connected to the current probes, but are spatially separated from them. This differs from the setup of the previous TLM devices, which used a 2-probe

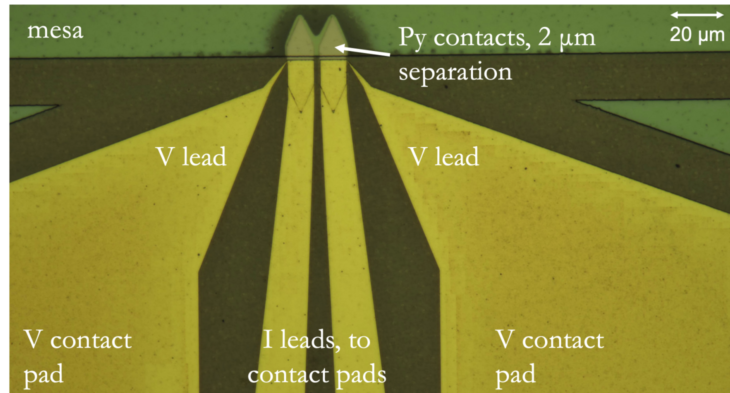

Figure 6.1: Optical micrograph of Au current and voltage leads connecting to the Py contacts, which in turn connect to the mesa. The voltage leads are positioned very close to the mesa, with 1 µm distance along the Py contact between them and the mesa edge.

setup, with voltage and current probes connected to the same single pair of contacts. The adapted setup yields a greater accuracy in the measured resistance, as the current and voltage leads remain separate until they reach the Py contacts, where they meet at a point 1 µm away from where the Py contact pair meet the semiconductor bridge. In the standard 2-probe setup used in the previous TLM devices, the current source and voltmeter connect at a breakout box and share the same path down to the device, meaning that the cable resistance offsets the y-intercept in a TLM plot and overestimates the contact resistance. Whilst this is assumed to be a very small resistance contribution in comparison to the contact resistances (and especially their uncertainty), it provides additional security in the accuracy of the measurement.

Following the new contact pad setup, I-V measurements were conducted across each contact pair for a ± 1 µA range. The resulting resistances were collated and analysed in the same manner as the larger contact devices above. The fabrication process for this type of device required extensive optimisation, in particular due to standard methods conflicting with electron beam lithography (EBL) resists and developers, which is a requirement for contact-related steps since they contain sub-micron features. It ought to be noted that the MLA, which was used for all micron-scale photolithography processes in previous chapters, ceased to function while optimisation and fabrication were ongoing. This meant that the micron-scale layers also had to be produced by EBL, with further resist/developer optimisation and compromise required. This section will focus on the EBL-based approach, as this yielded the final devices used for measurement. Both the refined EBL-based method and intended original method using a mixture of photolithography and EBL are given in Appendices A.3 and A.4 as comprehensive instructions. The EBL exposures following my pattern designs were completed using

a Jeol JBX-6300FS EBL System by Dr Mark Rosamond and Dr Rory Gilroy, Leeds Nanotechnology Cleanroom, University of Leeds.

This chapter will first outline specific features in the device pattern, some of which were added to aid the many EBL-patterned layers, and some of which relate to the pilot features mentioned in items 3 and 4 of the feature list above. Following this, an in-depth summary of the fabrication procedure is presented, optimised for EBL of up to macroscopic scale features. Subsequent to that, there will be a discussion of the separation dependent resistance results, where a variety of linear fit approaches are applied to derive low contact resistances and reasonable effective widths. The performance of the adjusted contact geometry and top gate is considered in the context of future work in Chapter 7, with respect to what fabrication improvements will be necessary to produce QSH state-detecting devices.

6.2 Pattern Design

6.2.1 Principal Features

The device is composed of a rectangular mesa that contains the conducting QW channels, which is formed by wet etching in the same manner as all previous devices, and is 2392 μm × 200 μm. Joined to the edge of the mesa are pairs of Py contacts, separated by distances of 200 nm to 20 μm. The Py contacts are in the elongated hexagonal 'boat' shapes shown in Fig. 6.1 for control of magnetisation orientations, allowing both parallel and anti-parallel alignments for the contact pairs [64]. They are 10 μm wide and have a tip-to-tip length of 36 μm (this is the W direction in the TLM convention). The extent of contact with the mesa is 15 μm. Cr/Au ohmic contact leads and pads are connected to the Py contact pairs for TLM measurements. This separated I and V lead layout differs slightly from previous TLM devices. Each Py contact has one current lead and pad, and one voltage lead and pad. The voltage leads are positioned so that there is a 1 μm space between the lead and the point where the Py contact meets the mesa. This is to ensure lithography alignment error does not cause a short to the mesa.

6.2.2 Additional Features

Aside from the main functional features of the devices, there was a series of additional features spanning an entire chip of devices, which were not featured on previous fabrications. These features were either to aid the planned EBL steps, or were added as a result of the additional EBL processes for micro- and macroscopic components. The features are:

1. **Metallic alignment crosses:** distinct from standard alignment crosses formed during the mesa etch stage. Metallised markers were proven to be necessary for precise alignment during EBL. They are shown in the pattern diagram in Fig. 6.2.

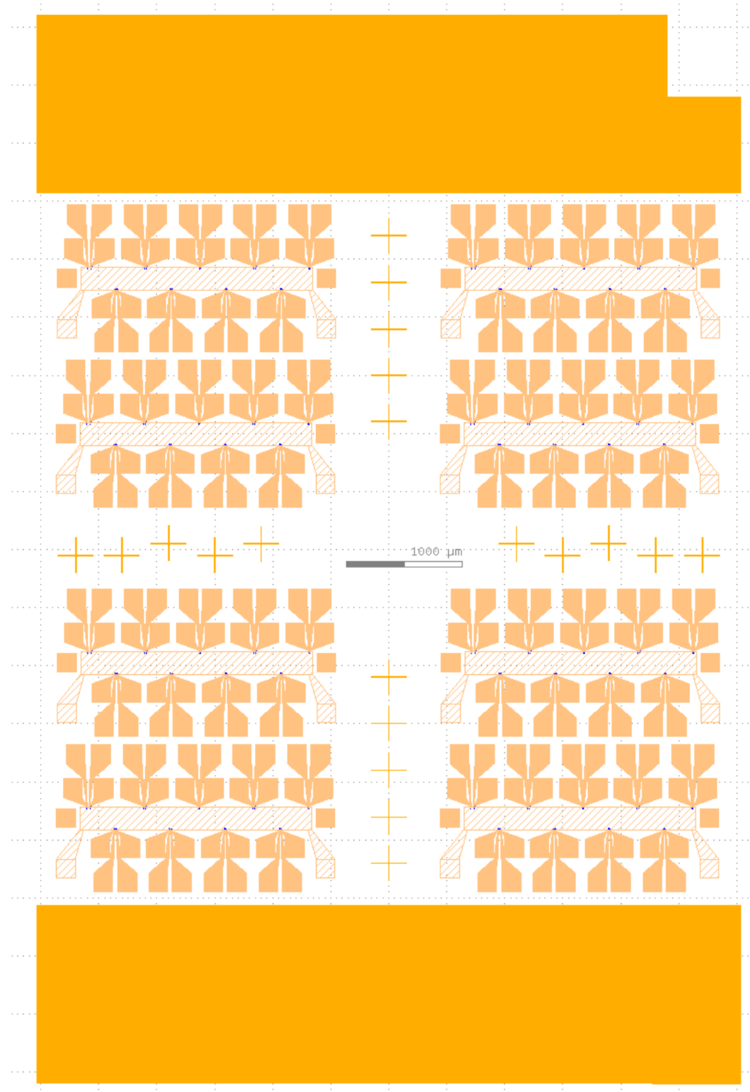

Figure 6.2: Pattern diagram, showing the first, third and fourth exposure layers. The second exposure layer, which defines the mesas and protects metallic features, is not shown due to this obscuring the principal features. The four sets of alignment crosses are visible between blocks of devices and the two large metal blocks are seen at the top and bottom of the design. The device design is treated in Section 6.3. Produced using KLayout [9].

2. **Metallic layer in free space:** two large rectangles of Ti/Au/Ti to prevent pattern distortion by scattered electrons. A cut-out on the upper right corner is included for chip alignment purposes, which can also be seen in Fig. 6.2.

3. **Etched borders:** instead of wet etching everywhere apart from the pattern features (typically the mesa, traditional alignment markers and etch depth measurement features), only a small area surrounding pattern features was etched away. It it covered in greater depth in Section 6.3.2.

6.3 Fabrication Optimisation

6.3.1 Alignment Markers

As with any multi-layered lithography process, alignment markers are needed to maintain correct alignment across fabrication layers. The clarity of alignment markers is of greater concern for EBL, as the markers need to be easily detectable by the beam to avoid the unwanted exposure of device features when searching for them. The markers also need to be easily distinguishable from one another to aid searching, which was achieved by adding random offsets between alignment crosses in a set. For this fabrication in particular, it was beneficial to also include more than the necessary number of sets, as crosses can be lost to fabrication issues, such as patches of failed metal lift-off.

To achieve detectable crosses, I first tested the quality of crosses produced by etching compared to those produced by metallisation and lift-off. Etched crosses would allow this fabrication stage to be combined with the mesa etch stage, making it the preferred result for the sake of efficiency. However, in practice, the etched crosses were not easily detected. Successful detection relies on the electron backscatter contrast between the cross surface and the background, which depends on the atomic number differences. The metallic crosses provided a more detectable contrast, so this became the standard procedure.

During EBL, scattered electrons can cause a build up of surface charge, which deflects the beam and disrupts the exposure. One potential solution is to move exposure areas further apart [65], as it is a solution that does not require a change to the wafer structure. However, due to material scarcity, the chip size and hence the feature spacings could not be amended. Charge dissipation polymers are also available to negate this issue, but those available ran the risk of causing damage to the wafer material. For this reason, during the metallic alignment cross deposition, two metallic rectangles of around 6000 μm $\times$ 1600 μm were deposited above and below the main design. The rectangles were situated in the excess space above and below the main design. This excess space only existed to ensure that the chip was large enough to support itself when mounted in the EBL, therefore, no design space was lost to accommodate the metallic rectangles. The purpose of the rectangles was to connect to the earthing pins of the EBL mount, redirecting any surface charges. This feature is the reason for the Ti/Au/Ti evaporation at this stage, rather than a simple Ti/Au. As such a substantial

Figure 6.3: Clusters of drifted Au squares that appeared in subsequent fabrication stages, after the partial lift-off result. In total, only a small number of squares drifted across the chip, and usually not in clusters. However, there were occasional clusters or single squares that affixed to Py contacts, resulting in the rejection of otherwise well-fabricated contacts.

area of the chip was covered by this metal, an additional 5 nm Ti with its native oxide provided a more wettable surface, leading to more uniform resist distribution during subsequent exposures than an Au surface would have provided.

As this step was also completed by EBL for the final optimised devices here, the solid blocks of metal were changed to grid patterns of metal instead, to reduce the write time. This grid pattern was formed by a mixture of 5 μm × 5 μm squares, either containing metal or free space. The resist was UV60-0.58 with pre- and post-exposure bakes (further detail in Section 6.3.2), with Microposit MF CD-26 developer. The lift-off was completed in acetone.

A key observation from the updated grid design was the partially failed lift-off of the many 5 μm × 5 μm Ti/Au/Ti squares. This proved to be a problem throughout subsequent fabrication stages, when stray squares had drifted and affixed to other fabrication features, and is therefore not recommended. Of course, typically, EBL is not required to form macroscopic features, and so no measures would need to be taken to reduce write time. Figure 6.3 shows an example of drifted squares further into the fabrication process, where they have affixed themselves to an area intended for ohmic contact deposition. Overall, there were not many problematic drifted squares, as most squares travelled alone to inactive sites of the chip, or remained local to the Au rectangles. However, during some fabrication stages, squares had drifted in clusters or single squares and settled on Py contact areas, leading to the rejection of otherwise faultless contact pairs. As this fabrication layer contains only larger features (alignment crosses and the rectangular blocks), the original method employed standard bilayer resist photolithography.

6.3.2 Mesa Wet Etch Process

Patterning

As with previous fabrications, the mesa is formed by wet etching the surrounding areas to isolate it. UV60-0.58 was chosen for the mesa patterning, as the higher resolution provided by ZEP520A (the other resist used in this fabrication) was not needed at this stage. The issue of the UV60-0.58's TMAH (tetramethylammonium hydroxide)-based developer attacking the primary layers of the wafer structure was also not a concern, as it is an inverted exposure.

The 0.58 in UV60-0.58 refers to its ~ 0.58 μm thickness when spun under standard conditions. It ought to be noted that it is actually a deep ultra-violet (DUV) photoresist, but it is frequently repurposed as an EBL resist, given the appropriate exposure. Through dose-defocus tests, this was determined to be 25 μC cm^{-2} for the scale of features needed here.

UV60-0.58 is a positive resist, meaning the electron beam causes scissions in the polymer chains, making them more soluble in the appropriate developer. It is also preferable here due to its lower dose requirement of 25 μC cm^{-2}, compared to the 165 μC cm^{-2} dose determined for ZEP520A (used in subsequent steps). Another difference is the fact that UV60-0.58 is a chemically amplified resist. This means that, upon exposure, an acid is released in addition to the breaking of polymer bonds. This acid acts as a catalyst to the bond breaking reaction, which requires a 130 °C post-exposure bake to activate. Another crucial detail is that this post-exposure bake is highly time sensitive. As soon as the sample is removed from the vacuum chamber used for EBL, impurities in the air begin neutralising the acid, inhibiting the amplification and hence a successful develop. For this reason, all post-exposure bakes were performed within 5 minutes of chamber venting completion.

Developing

Microposit MF CD-26 is the matching developer, which is a TMAH-based developer. This means that certain layers of the wafer structure can be dissolved by it, namely the GaSb and AlSb layers (although dissolution of the buffer layer has not been ruled out). During this step, this attacking of the upper layers is not an issue, as it is an inverted exposure and the mesas are protected by resist. The InAs layer is not attacked by the developer, meaning that the developer would stop at this layer. This raises the question of whether a typical developing time is appropriate, or a deliberate over-developing to reach the InAs layer would be preferable, as it would offer a smooth start to the wet etching process. A variety of developing times were tested, to ascertain which surface preparation yielded the most practical etch result, without compromising resolution. The optimal developing time was 90 s, corresponding to developing down to the first AlSb layer. Shorter durations would risk leaving patches of GaSb cap (which was discussed in Section 3.2, due to its apparent oxidation). Longer durations (> 110 s), for which the InAs cap had been reached, appeared to rapidly oxidise and caused salt

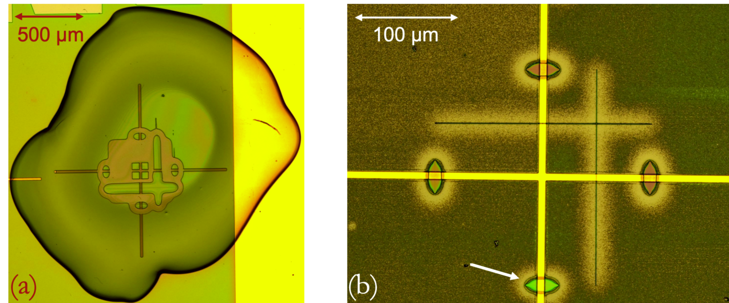

Figure 6.4: **a.** A micrograph to illustrate the manual painting of resist onto exposed metallic areas. The exposed areas are where the EBL has searched for the cross edges, and in doing so has exposed the resist in that area. **b.** An example of over-exposure sustained whilst searching for the cross, where the over-exposed areas show iridescence. The over-exposure re-hardens the resist, making it once again protective of the metallic area.

formation issues during the etch, similarly to those seen in Section 3.2.

Exposed Metal

Due to the metallic elements deposited in the previous step, the mesa pattern requires additional features to maintain consistency in the wet etch result. Firstly, no metal should come into contact with the etchant, as it may affect the result. For this reason, the mesa pattern contains large areas of unexposed resist to cover the large Ti/Au/Ti areas for the surface charges, and the alignment crosses.

The process of aligning the mesa pattern to the first set of alignment markers will expose additional areas of resist, leaving small amounts of Ti/Au/Ti exposed to the etch solution. To negate this, I hand-painted chilled S1805 photoresist onto the exposed alignment markers. An example is given in Fig. 6.4a. Whilst this was largely successful, it is an intricate task and resist can easily spread to devices and prevent them from etching. A possible solution would be to apply very high EBL exposure doses to the exposed alignment crosses, once correct alignment has been established. During the searching of alignment markers, areas of resist that received greater exposure would effectively invert their resist properties. This is referred to as an inversion of the tone of the resist, and has been studied in PMMA and ZEP resists [66, 67]. As UV60-0.58 is a positive resist, the areas exposed to the electron beam weaken and dissolve during development. However, higher dose exposure areas can behave as a negative resist. This is because the reaction of this resist to the electron beam is a combination of two major processes. The first is the typical breaking of polymer chains for developer solubility, and the second is a simultaneous cross-link formation. For relatively low doses, the bond breaking process is dominant; past a threshold dosage, the cross-link formation dominates. For this reason, deliberate over-exposure of what would be

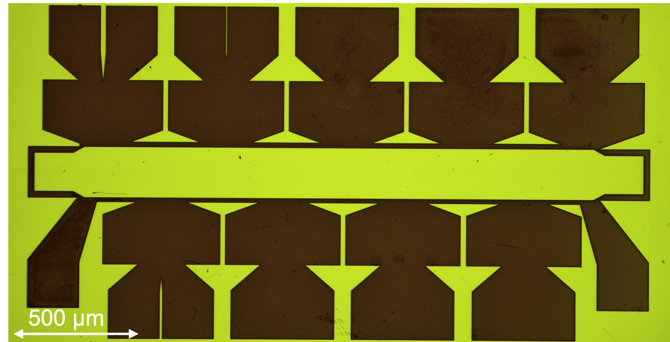

Figure 6.5: Optical micrograph of the mesa etch result. As mentioned previously, amendments were made to this pattern to reduce EBL write time, wherein the areas surrounding future device features were etched instead of the entire surface (excluding mesas).

developed and exposed areas of metal could be a more reliable method of protecting the etchant, without risking accidental resist spread to devices. An example of inverted resist properties is shown in Fig. 6.4b.

Wet Etching

Once the patterning was complete, the wet etch was performed using the same formula as all previous etches, containing citric acid, hydrogen peroxide and phosphoric acid. The etch behaved similarly to that in previous optical lithography processes, with the initial etch rate performing less predictably, as the various layers of the wafer are passed. Once the second AlSb and buffer layer were reached, the etch rate stabilised to $\sim$ 12 nm/min. The result is shown in Fig. 6.5, where entire sample surface excluding the mesa is no longer etched, to conserve EBL write time. This etch geometry forms a 20 µm border around subsequent device features.

Similarly to previous etch processes in this thesis, the GaSb cap still proved problematic, even using the optimised surface preparation with 90 s developing time. In a number of well-defined areas covering portions of a device, the GaSb cap appeared to remain intact despite the TMAH exposure. Combined visual and surface profilometer inspection confirmed negligible etching in these areas. This is most likely due to traces of oxidised GaSb cap remaining after developing, which have proven to be, effectively, impossible to etch (within the limits of the rest of the sample etching to the substrate, using this etch solution).

There are two major ways that this could be avoided. The first would be to perform rigorous surface profilometry measurements following the usual 90 s developing time, to complement the optical inspection, and continue developing for (90 - 110) s, with the intention of clearing the GaSb cap but remaining within the AlSb barrier. Alternatively, the second approach would be to develop for $>$ 110 s to reach the InAs layer across the

sample. This makes for a more time consuming and less predictable wet etch rate, but may be preferable when the cap layer is proving problematic.

6.3.3 Permalloy Contact Deposition

Patterning

As they contain $\geq$ 200 nm features, and require a lift-off process, the Py contacts are patterned by using ZEP520A and a 165 μC cm^{-2} exposure dose, as determined by dose-defocus tests. ZEP520A is a positive photoresist, like UV60-0.58, but without the same chemical amplification acid component. Notably, this is also a single-layer resist pattern, compared to the bilayer system used for optical metal depositions in previous chapters. This was also the case for the first metal deposition, which was the Ti/Au/Ti alignment markers and grounding rectangles. A single layer of ZEP520A is sufficient for lift-off because forward scattering of electrons entering the resist ensures that the beam is broadened by the time it reaches the bottom. This results in re-entrant sidewalls, which cause a discontinuity in the metal deposition similar to that seen in bilayer resist processes.

The Py evaporation was performed under identical conditions to those described in Section 5.2.2. Namely, the O_2 plasma ash, in-situ Ar ion etch and tilted 60 nm Py evaporation followed the same specifications.

NMP Damage Test

The lift-off was performed using Shipley Microposit Remover 1165, the principal ingredient of which is the solvent N-methyl-pyrrolidone (NMP). Initially, acetone and SVC-14 were trialled for the lift-off, as they have been routinely used throughout this thesis and have therefore demonstrated their compatibility with the layer structures used here. In this case, these methods proved unsuccessful, leaving a visible residue behind.

The possible damaging effects of NMP on the wafer were tested thoroughly, during which I soaked a plain sample for 1 hour, applying 45 °C heat. This time is significantly longer than what is required (a few minutes). The sample I had selected also included the MBE growth edge, where lower layers of the wafer were exposed. Upon comparison with an unsoaked sample, there was no visible damage to any part. For this reason, the result of a $<$ 5 min application of NMP to the devices during Py lift-off was surprising, as described below.

Mesa Discolouration

The result of the $<$ 5 min application of NMP during Py lift-off indicates that NMP combined with resist has a significant effect on the sample surface appearance, compared to no visible change when tested in the absence of resist. As shown in Fig. 6.6, darker areas developed in places where the upper wafer layers were still intact. At

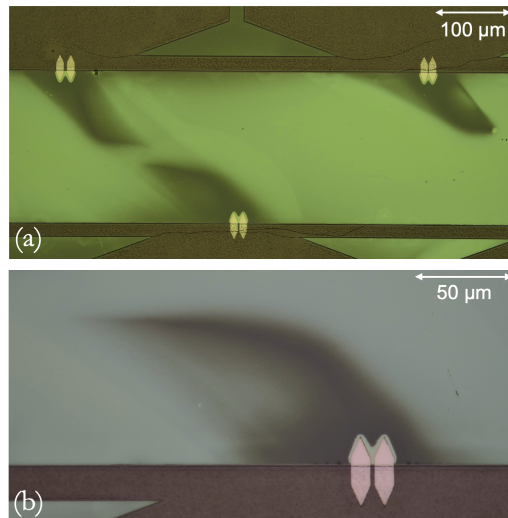

Figure 6.6: **a.** A micrograph of the top of the mesa following Py contact (small, yellow boat-shaped pairs) deposition and subsequent lift-off, using NMP-based resist remover. **b.** A closer micrograph, showing the border around the contacts where discolouration did not occur.

times, this discolouration followed a consistent pattern/direction. Another observation is that the mesa surface directly adjacent to the Py contacts did not suffer the same discolouration. Different samples exhibited different extents of discolouration, which did not appear to correlate with anything. This result also clearly requires the combination of the ZEP520A resist and NMP, since the plain sample soaking did not yield this discolouration. Lastly, the discolouration was not visible until the samples were removed from the NMP. Ultimately, a definitive source could not be identified by this information alone.

6.3.4 Ohmic Contacts and Pads Deposition

As the ohmic contacts and pads pattern contains nanoscale features in order to connect to the Py contacts, it must be at least a partial EBL procedure. The standard ZEP520A process was employed again, despite the features not being as small as those in the previous ZEP520A step. The first reason for this is that the two exposed contact pad areas on each mesa would be attacked by a TMAH-based developer. The second reason is that the extent to which a TMAH-based developer would attack the exposed buffer layer surface (which is what surrounds most of the Py contacts) is unknown. Attacking this area by any amount would risk increasing the original 60 nm height difference between the surface of the Py contact and the sample surface, which is the thickness of the Py contacts. A significantly taller ledge here could create difficulties when trying to attach Cr/Au ohmic contacts.

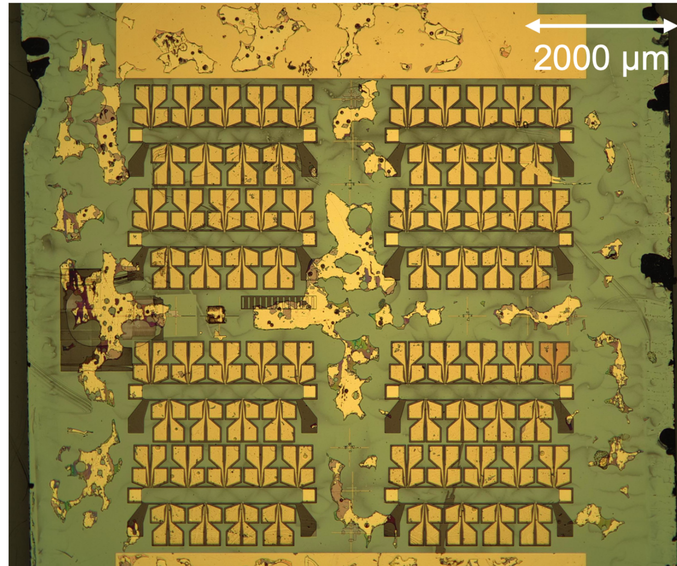

Figure 6.7: An example of poor ohmic contact lift-off on a trial chip. This appeared to be a result of the thermal evaporation unintentionally hard-baking the resist. After this, electron beam evaporation was employed for the ohmic contact and top gate deposition.

The ohmic contact composition was 5 nm/160 nm Cr/Au. The Cr layer is again used for improved adhesion, as per the standard Au contact procedure in this thesis. As previously noted, the change to Ti/Au/Ti in the alignment cross layer was due to an upper layer of Ti being beneficial to resist spreading. The relatively thick layer of Au accounts for the usual $\sim$ 100 nm ohmic contact height and the 60 nm Py contact height. For this resist/developer combination, electron beam evaporation (using a Leybold Univex 350) proved more successful than the usual thermal evaporation by achieving a clearer lift-off result. The thermal evaporation resulted in poor lift-off in many areas (see Fig. 6.7), despite an $\sim$ 18 hour soak time. This created multiple visible shorts across contacts. This is thought to be due to the prolonged heating sustained during this relatively long thermal evaporation, which may have caused a hard-bake effect.

Whilst the electron beam evaporation result was significantly improved, it was not flawless, and some features were occasionally lost to failed lift-off patches. An alternative resist and developer combination may provide a more reliable result. For instance, the S1805 resist-based thermal evaporation methods (following photolithography) used previously in Sections 3.2 and 5.2.2 were not prone to an over-baking effect. For this device, the need for an EBL resist is unavoidable, due to the smaller features in the Au leads near the Py contacts. In future, a different EBL resist process may prove more heat resistant.

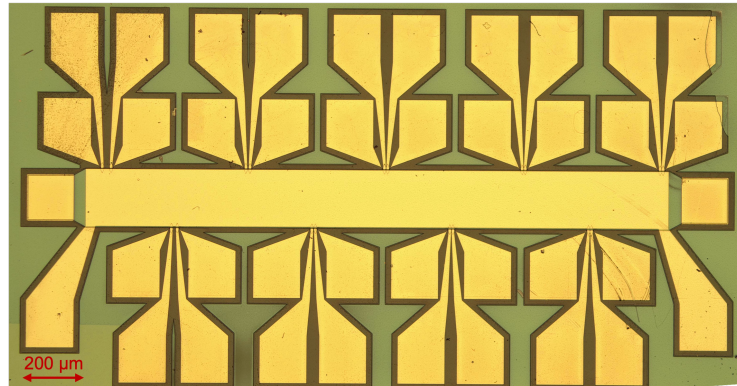

Figure 6.8: A completed device, where the Cr/Au ohmic contacts can be seen within etched borders. There are two additional ohmic contacts at either end of the mesa, which were included in the design should any current biasing be required. They were not used in the measurements presented here. The top gate can also be seen along the top of the mesa, with two connecting contact pads for continuity measurements and/or a spare connection. The ohmic contact layer is covered by 30 nm Al_2O_3, with the top gate situated above.

6.3.5 Top Gate and Back Gate Formation

As previously mentioned, gating was trialled for these devices. The back gate was capped with Cr/Au in the same manner as with the Hall bar devices in Chapter 4. Following this, a top gate dielectric of 30 nm Al_2O_3 was deposited by ALD. The top gate metallisation followed the same process as the ohmic contact deposition above, but with a 5 nm/95 nm Cr/Au thickness. Thanks to the oxide layer, the mesa below was protected and did not sustain any further reactions with the NMP soak. As the Cr/Au thickness is significantly less than that of the ohmic contacts, the lift-off result was clean (however, an overnight soak was required to achieve this). Once the devices were complete, they were diced and mounted with conducting silver paint onto the Au chip carriers used for all previous devices. A completed device is shown in Fig. 6.8.

6.4 Measurements and Results

6.4.1 Experimental Setup

The experimental setup for these measurements differs slightly from both the setup for the Hall bar devices in Chapter 4 and the previous larger TLM devices in Chapter 5. The devices were measured in the quasi 4-probe shown in Fig. 6.1, using a Keithley 6221 current source, a Keithley 2182 voltmeter and a Keithley 2400 source meter to test trial top gate function. Devices were cooled to (4.3 - 4.6) K in a Cryogenic Ltd. continuous flow ^{4}He cryostat, which is a different model to that used in the Hall bar measurements. It cools by the same principle of attaching the measurement holder to

the end of a probe stick and inserting it into the sample space, which is pumped on to draw in He gas.

6.4.2 Contact Resistance

The resistance results from the Py contact pairs at room temperature and low temperature are considered in this section. Resistance was calculated for ± 1 μA current and collated to resistance-separation plots in the same manner as in Chapter 5. These results are shown in Fig. 6.9.

Naturally, the act of cooling caused losses of connections that were present at room temperature, as observed in the larger TLM devices, but with a higher proportion of lost connections. In total, 26 pairs were tested at low temperature. Of this 26, 7 lost connection and 8 formed very unstable connections, where unstable refers to highly fluctuating and non-reproducible resistances. This increased rate may be due to the reduced contact area giving less opportunity for stable connections or pinhole sites; effectively, an exaggerated version of the loss of connection seen in the larger TLM devices. The nature of this measurement, in that it requires the connection of four current and voltage probes, is also more prone to failure. In addition, the probes are as thin as 0.5 μm in places, making them considerably more sensitive to fabrication defects than the much larger leads in the previous devices.

Nonetheless, the devices that were connected showed highly ohmic behaviour. Only one result showed considerable non-linearity (quantified by a 3 % standard deviation in the resistance), and this was omitted from the overall plot. The remaining I-V data averaged 0.1 % resistance deviation.

As with the previous TLM devices, the separation-dependent resistance results are subjected to a linear fit to determine a contact resistance. The grey line in both panels of Fig. 6.9 show the weighted least squares linear fits for all plotted resistances. Again, the weighting is determined by the inverse of the standard deviation in the I-V fits. Applying an ordinary least squares fit to each data selection consistently gave unphysical results, in that they produced a negative gradient, resulting from the large variation in measured resistance.

In the room temperature case in 6.9a, the fit yields a contact resistance of (14 ± 6) Ω. The corresponding effective width and transfer length are (40 ± 30) μm and (11 ± 9) μm respectively. When considering the uncertainty ranges of both values, they appear to be physically reasonable, albeit widely spread, as their lower bounds fit within the dimensions of the contact. A reminder of the dimensions is given in Fig. 6.10. It is important to recall that the TLM geometry here, as with that of the previous TLM devices, is not traditional. This is due to the AlSb barrier layer above the mesa, meaning that resistances may contain pinhole conduction contributions as well as InAs/GaSb edge contact. A baseline fit assuming the classic TLM setup (where the contact is not separated from the mesa) is plotted in Fig. 6.9 for both temperature cases. This is a line with a zero-intercept and a gradient determined by the predicted channel resistance, which was converted from the known sheet resistance by the fabricated,

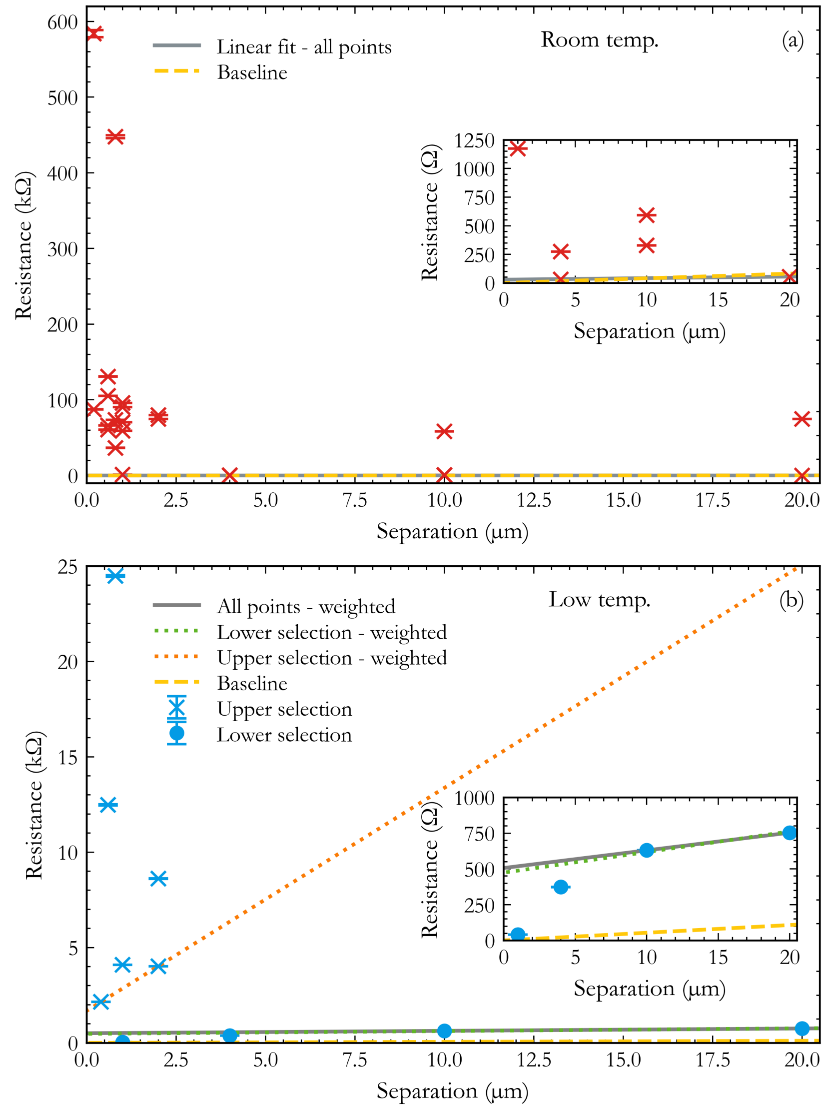

Figure 6.9: Resistance against contact separation results for the smaller TLM devices. A weighred linear fit is applied to both temperature cases, which lies preferentially with lower resistances derived from more ohmic I-V results. The baseline channel resistance, determined by the known sheet resistance, is also plotted. The insets both show a close-up of lower resistance data, given in Ω. **a.** Room temperature. **b.** (4.3 - 4.6) K, where the data are also divided into upper and lower resistance sections, and fitted separately.

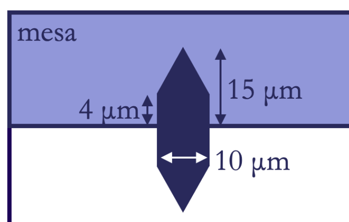

Figure 6.10: Py contact dimensions, where the contact is partially situated over the mesa. The total point-to-point contact width is 36 µm.

idealised contact width. This serves as a comparison to the high resistances measured when contact is confined to the channel edge and possible defect sites. The lack of a clear relationship between most of the individual resistances suggests that interface contamination dominates many measurements.

This contact resistance is lower than that of the larger TLM contact results from the previous chapter (in Section 5.3) at room temperature. This response is anomalous when considering the simple case of constricting the current path leading to increased resistance. It may be a result of improved interface quality between the contact and QW channel, demonstrated by the aforementioned increase in overall I-V linearity. Although, the I-V range tested was smaller in this case (to avoid thermal damage to the smaller contacts), which means less ohmic behaviour may be present at wider ranges. There were also no changes to the Py deposition process. The transfer length corroborates the improved interface quality when considering edge contact. Despite being $\sim$ 100 % of the contact length, that of the larger contact was as great as 3 $\times$ the fabricated length.

In the low temperature case, the fit produces a contact resistance of (250 $\pm$ 50) Ω. This is higher than the low temperature (weighted) contact resistance in the larger contacts in Chapter 5, which is the expected trend for a simple edge junction. This is accompanied by an effective width of (7 $\pm$ 4) µm. This is a reasonable result when considering the reduced phonon scattering compared to the room temperature case, where the current dispersion was spread further into the transmission line, quantified by the (40 $\pm$ 30) µm effective width. The inset shows a close-up of the lower resistance results, where a linear trend is also observed.

The transfer length result corresponds to twice the fabricated distance, which may suggest reduced edge junction quality. If the Py/(InAs/GaSb) junctions still harbour some oxides, the reduced thermal energy could inhibit the passing of small potential barriers. If there is a pinhole conduction contribution at room temperature, the availability of those channels may have diminished with decreasing thermal energy, which could also have contributed to the increased resistance and perceived worse contacts. These results, along with those from the room temperature case, are presented in Table 6.1.

Regarding these low temperature data in Fig. 6.9b, it could be argued that the

Table 6.1: Summarised weighted least squares fit results of resistance-separation TLM plots for room temperature and (4.3 - 4.6) K, where contact resistance is determined via the resistance-axis intercept. Effective width and transfer length are also given, as determined by the gradient and separation-axis intercept respectively. A data selection column is included to account for the high and low resistance divided data for the low temperature case.

Temp. Range	Data Selection	R_{contact} (Ω)	W_{eff} (μm)	L_{T} (μm)
Room	All	14 ± 6	40 ± 30	11 ± 9
Low	All	250 ± 50	7 ± 4	20 ± 10
	Lower	240 ± 40	6 ± 2	16 ± 7
	Upper	840 ± 1	0.0693 ± 0.0002	0.719 ± 0.002

data are divisible into two regimes of high and low resistance, with the boundary lying around 2500 Ω. The division of data into the two regimes is indicated by the marker used for each data point, with crosses assigned to high resistances and circles assigned to low resistances. The results of each of these fits are also included in Table 6.1.

With respect to the lower selection, its significant overlap with the overall fit indicates that it contains some of the most ohmic I-V results, as they are the most influential in the fits (where the weighting was inverse variance-derived). If the upper resistance selection does correspond to more pinhole site-dominated conduction, this is well reflected in its low effective width, which may be a result of suppressed defect conduction paths at low temperature, meaning very limited current passing into the transmission line to disperse. Whether dividing the low temperature data or assessing it as a whole, the resistance is dominated by the semiconducting part of the conduction path, as there is a substantial increase upon cooling.

6.5 Conclusion

This chapter has presented the successful fabrication of reliably ohmic Py contacts positioned at low micron- to nano-scale separations. The contacts are significantly smaller than those in Chapter 5, meaning proportionally more of the contact to the conducting mesa channel is formed at the InAs/GaSb QW edge if pinhole conduction through the top is a factor. The individual resistances continue to show variability, with many not conforming to an idealised linear TLM pattern. Nevertheless, the overall extracted characterisations are largely physically reasonable.

The low temperature resistances suggest a possible division into lower resistance, edge-dominated contact, and higher resistance, defect-dominated contact. Following this approach yields an edge contact resistance of (240 ± 40) Ω.

A novel fabrication method was devised to construct these devices, which is prom-

ising for future experiments involving gate voltages, to drive the system towards charge neutrality for spin-dependent transport detection.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

In this thesis, I have presented transport measurements on a gated InAs/GaSb QW Hall bar device capable of reaching the charge neutral regime, which was the focus of Chapter 4. The carrier density region approaching charge neutrality has been studied under the LK formalism and its derivative Dingle analysis, which study the temperature dependence of SdH oscillations. A breakdown in the LK model's ability to describe the system occurred in the carrier density region of (4.3 - 6.8) $\times$ 10^{11} cm^{-2}, as charge neutrality was being approached. Following this, the phase dependence of SdH oscillation minima was studied in the context of a Landau index plot, to study the presence of the contested Berry phase in InAs/GaSb [18, 19]. This plot did not exhibit a non-trivial Berry phase.

The fabrication of novel Py/(InAs/GaSb) junctions was studied in Chapter 5, with a detailed report of techniques and refinements. In particular, the semiconductor surface preparation prior to the Py deposition was optimised to form a reliably ohmic interface. The junctions were formed by fabricating TLM devices with Py contacts, which provided contact resistance estimates, along with other characterisations. Varying device geometries determined that the resistance was dominated by conduction at the TLM device edge in the $<$ 10,000 Ω resistance range, where the Py/(InAs/GaSb) junction is located.

The results of Chapter 5 provided the groundwork for optimising low micron- to nano-scale Py contact devices in Chapter 6, which were also a TLM setup. These device dimensions are more consistent with those required for spin dependent transport measurements in the InAs/GaSb edge conduction regime.

7.2 Future Work

Throughout this thesis, I have highlighted persistent difficulties with the wet etch process for the InAs/GaSb QW wafer structures. When growing new structures for the purpose of integrating Py contacts, or for any purpose, an InAs cap may prove more functional. This material is also capable of oxidising, however, it is the apparent unevenness in the GaSb-capped structures used here that presented issues. Another suggestion would be to formulate a gradual etch process, where a separate chemical etch solution is applied to selectively etch each specific layer in turn. The main drawback of this solution is time inefficiency, both in the formulation and testing of the separate etch solutions, and in the implementation. Although, selective etching of the present materials is well established [68, 69].

It was acknowledged in Chapter 6 that the device design contained additional trial features that would lend themselves to future experiments in detecting spin-dependent transport in the edge regime. These features were the elongated hexagonal geometry of the Py contacts and the inclusion of a top gate. The former was to control magnetisation alignment of the contact pairs [64] and the latter was to provide a means to tune the

system towards the charge neutral regime, where spin-dependent edge transport would become dominant if a QSH state were present. Unfortunately, none of the top gates fabricated on each device proved suitable. The dielectric performance was tested and all gate electrodes had a short of (300 - 400) Ω to the rest of the device below the dielectric layer.

When compared to the more successful gated Hall bar devices, there are various fabrication and design differences in these devices which may be to blame. One possible cause is the repeated use of electron beam evaporation to deposit the Au features, rather than the previous thermal evaporation technique. This switch was necessary due to the EBL resists seemingly hardening due to excessive heating, yielding inadequate lift-off results. For the top gate electrode deposition in particular, the use of electron beam evaporation may have carried a damaging side-effect for the Al_2O_3 dielectric layer below, whereby x-rays emitted during the deceleration of electrons contacting the metal target adversely affect the gate dielectric. X-rays incident on the dielectric layer can ionise atoms or break bonds, with resulting dangling bonds acting as charge traps - both of which are detrimental to the layer's insulating capabilities [70]. Unfortunately, if this effect is to blame, it is indirectly due to the unavailability of the MLA for photolithography and could not have been avoided under the circumstances. This proposed reason for the dielectric failure stands as an additional reason why Au layers should be fabricated using photolithography techniques, further to the obvious reasons regarding write time and familiarity of the procedure.

An alternative (or additional) reason for the top gate failure may relate to the geometry of the Py contacts, which was chosen for flexibility in contact magnetisation alignment, which could have undergone preliminary testing had the top gate performed as hoped (although, this would have been very limited testing due to the time constraints). Generally, it is not advisable to construct sharp, pointed features in devices harbouring a gate. Pointed features, such as the tips of the Py contacts, can generate localised electric fields about the point, due to electrostatic repulsion confining electrons to the constriction. This localised field can induce dielectric breakdown [71]. For this reason, the primary fabrication improvement to facilitate top gate usage would be to alter the Py contact shape design to give a more rounded shape at either end. With these fabrication-based issues overcome, it will be possible to test the hypothesis of spin-momentum locked transport in helical edge states.

Appendices

Appendix A

Device Fabrication Methods

A.1 InAs/GaSb QW Hall Bar Device Fabrication Method

1. Sample Cleaning:
   (a) Clean in acetone, isopropyl alcohol (IPA) and twice in deionised (DI) water, agitating by hand as the wafers are sensitive to even low ultrasonic powers.
   (b) Store sample in a desiccator when not in use.
2. Mesa Patterning:
   (a) Spin-coat SurPass 4000 Adhesion Promoter at 3000 rpm for 40 s, cleaning with IPA when $\sim$25 s remain.
   (b) Spin-coat S1805 Positive Photoresist at 3000 rpm for 40 s.
   (c) Bake at 115 °C for 1 min.
   (d) Expose mesa pattern on Maskless Aligner (MLA) (inverted so that mesa is unexposed) - dose: 90 J/cm^2, focus: manual.
   (e) Develop in H_2O:MF 351 (3.5:1) for 60 s (this ensures oxidised cap is completely removed). Rinse in DI water $\times$ 2.
3. Mesa Etch:
   (a) 13.75 g citric acid + 13.75 ml DI water: gradually add citric acid to DI water on 130 °C hot plate, stirring occasionally until dissolved.
   (b) Measure 110 ml DI water.
   (c) Add 2.5 ml H_2O_2 to DI water.
   (d) Add 1.5 ml H_3PO_4 to DI water/H_2O_2 mix.
   (e) Add citric acid solution, stir and measure temperature.
   (f) Leave mixture for 10 min to ensure temperature is constant. Be aware that etch rate rapidly decreases when etch mixture is left for +10 min. A 5 min pilot is always recommended to estimate etch rate. Etch rates for the structures used here typically fell in the 8-12 nm range, with the lower rates applying for the upper layers of the wafer structure.
   (g) Clean sample with acetone, IPA and DI water.
4. Ohmic Contact Deposition:
   (a) Spin-coat SurPass 4000 Adhesion Promoter at 3000 rpm for 40 s, cleaning with IPA when $\sim$25 s remain.
   (b) Spin-coat LOR 3B at 3000 rpm for 40 s.
   (c) Bake at 180 °C for 3 min.
   (d) Spin-coat S1805 Positive Photoresist at 3000 rpm for 40 s.

(e) Bake at 115 °C for 1 min.
(f) Expose ohmic contact pattern on MLA, ensuring correct orientation of sample and alignment of pattern. Dose is typically higher for bilayer resist (100-120 J/cm^2). 90 J/cm^2 and 120 J/cm^2 have both been successful previously.
(g) Develop in H_2O:MF 351 (3.5:1) for 2 min. Rinse in DI water $\times$ 2.
(h) Thermally evaporate Cr/Au (5/95 nm).
(i) Lift-off in SVC-14 at 70 °C for $\sim$20 mins, followed by gentle agitation with pipette.
(j) Clean with acetone, IPA and DI water.

5. Back Gate and Top Gate Dielectric Deposition:
   (a) Spin-coat a light bubble of PMMA (PMMA 950 K A2 used previously) at 3000 rpm onto top of sample for protection.
   (b) Bake at 180 °C for 1 min.
   (c) Check back of sample for splashes of resist, etc. and clean if necessary.
   (d) Thermally evaporate Cr/Au (5/95 nm) onto back of sample.
   (e) Soak sample in acetone for 5 min to clear PMMA layer.
   (f) Visually inspect - if PMMA remains, soak in SVC-14.
   (g) Clean with acetone, IPA and DI water.
   (h) Deposit 30 nm Al_2O_3 thermally (water precursor) by ALD, 200 °C for 300 cycles.

6. Top Gate Deposition:
   (a) Spin-coat PMMA 495 K A8 at 3000 rpm for 40 s.
   (b) Bake at 180 °C for 2 min.
   (c) Spin-coat S1805 Positive Photoresist at 3000 rpm for 40 s.
   (d) Bake at 115 °C for 1 min.
   (e) Expose top gate pattern on MLA, ensuring correct orientation of sample and alignment of pattern. Assume process for single layer resist, meaning 90 J/cm^2 dose and manual focus.
   (f) Develop in H_2O:MF 351 (3.5:1) for 60 s. Rinse in DI water x2.
   (g) Expose in UVO for 30 min to expose remaining PMMA layer in top gate pattern. Once exposed, wait 5 min before removing sample to avoid ozone.
   (h) Mix IPA:H_2O 7:3.
   (i) Develop in IPA/water mix for 2 min, then IPA rinse for 1 min. DI water rinse and inspect.
   (j) Thermally evaporate Cr/Au (5/95 nm).
   (k) Lift-off in acetone at 45 °C for around 15 min, then gently agitate with a pipette.

A.2 Micron-Scale Py Contact on InAs/GaSb QW TLM Device Fabrication Method

1. Sample Cleaning:

   (a) Clean in acetone, isopropyl alcohol (IPA) and twice in deionised (DI) water, agitating by hand as the wafers are sensitive to even low ultrasonic powers.

   (b) Store sample in a desiccator when not in use.

2. Mesa Patterning and Wet Etch:

   (a) Spin-coat SurPass 4000 Promoter at 3000 rpm for 40 s, cleaning with IPA when ∼25 s remain.

   (b) Spin-coat S1805 Positive Photoresist at 3000 rpm for 40 s.

   (c) Bake at 115 °C for 1 min.

   (d) Expose mesa pattern on MLA (inverted so the mesa is unexposed, increasing exposure boundaries) - dose: 90 mJ cm^{-2}, focus: manual.

   (e) Develop in H_2O:MF351 3.5:1 for 60 s (this ensures oxidised GaSb cap is sufficiently removed). Rinse in DI water × 2.

   (f) Etch following the same method as with previous devices (Appendix A.1 step 3), with 13.75 g citric acid dissolved in 13.75 ml DI water, with 100 ml DI water, 2.5 ml hydrogen peroxide and 1.5 ml (ortho)phosphoric acid. Covering etchant when not in use is recommended.

3. Py Contact Deposition:

   (a) Spin-coat MAA 8.5 MMA EM11 Photoresist (filtered) at 3000 rpm for 40 s.

   (b) Bake at 180 °C for 2 min.

   (c) Spin-coat S1805 Positive Photoresist at 3000 rpm for 40 s.

   (d) Bake at 115 °C for 1 min.

   (e) Expose mesa pattern on MLA - dose: 90 mJ cm^{-2}, focus: manual.

   (f) Develop in H_2O:MF351 3.5:1 for 60 s. Rinse in DI water × 2.

   (g) Expose MMA layer in UVO for 30 min, + 5 min wait to reduce ozone.

   (h) Develop in IPA:H_2O (7:3) for 2 min, followed by IPA rinse for 1 min. Rinse in DI water.

   (i) O_2 ash for 1 min (50 W).

   (j) Electron-beam evaporate 60 nm Py (with tilt where necessary), applying in-situ 80 s Ar ion etch before evaporation. Lift-off in acetone at 45 °C.

4. Atomic Layer Deposition:

(a) Deposit 30 nm Al_2O_3 thermally (water precursor) by ALD, 200 °C for 300 cycles.

(b) HF etch through dielectric:

5. HF Etch through Dielectric:

    (a) Deposit HMDS primer:

        i. Bake at 120 °C for 1 min.
        ii. Cool.
        iii. Spin-coat HMDS primer at 4000 rpm.
        iv. Bake at 120 °C for 1 min.
        v. Cool.
        vi. IPA jet at 4000 rpm.
        vii. Bake at 120 °C for 1 min.
        viii. Cool.

    (b) Spin-coat S1805 Positive Photoresist at 3000 rpm for 40 s.

    (c) Bake at 115 °C for 1 min.

    (d) Expose mesa pattern on MLA - dose: 90 mJ cm^{-2}, focus: manual.

    (e) Hard-bake at 130 °C for 10 min.

    (f) Develop in H_2O:MF351 3.5:1 for 60 s. Rinse in DI water × 2.

    (g) Etch in buffered HF for 30 s (etch rate: 1.2 nm/s).

    (h) Clear resist pattern in acetone.

6. Cr/Au Contact Deposition:

    (a) Spin-coat MAA 8.5 MMA EM11 Photoresist (filtered) at 3000 rpm for 40 s.

    (b) Bake at 180 °C for 2 min.

    (c) Spin-coat S1805 Positive Photoresist at 3000 rpm for 40 s.

    (d) Bake at 115 °C for 1 min.

    (e) Expose mesa pattern on MLA - dose: 90 mJ cm^{-2}, focus: manual.

    (f) Develop in H_2O:MF351 3.5:1 for 60 s. Rinse in DI water × 2.

    (g) Expose MMA layer in UVO for 30 min, + 5 min wait to reduce ozone.

    (h) Develop in IPA:H_2O (7:3) for 2 min, followed by IPA rinse for 1 min. Rinse in DI water.

    (i) Thermally evaporate 5/95 nm Cr/Au.

    (j) Lift-off in acetone.

A.3 Nano-Scale Py Contact on InAs/GaSb QW TLM Device Fabrication Method: EBL Version

1. Sample Cleaning:
    (a) Clean in acetone, isopropyl alcohol (IPA) and twice in deionised (DI) water, agitating by hand as the wafers are sensitive to even low ultrasonic powers.
    (b) Store sample in a desiccator when not in use.
2. Alignment Marker Patterning:
    (a) Spin-coat UV60-0.58 Positive DUV Photoresist at 3000 rpm for 40 s.
    (b) Bake at 130 °C for 1 min.
    (c) Expose alignment cross pattern by electron beam - dose: 25 µC cm^{-2}.
    (d) Post-exposure bake immediately after removing sample from vacuum, at 130 °C for 1 min.
    (e) Develop in Microposit MF CD-26 for 90 s, with strong agitation.
    (f) O_2 plasma ash for 30 s at 50 W power.
    (g) Thermally evaporate Ti/Au/Ti at thicknesses of 5/60/5 nm.
    (h) Lift-off in acetone.
3. Mesa Patterning and Wet Etch:
    (a) Spin-coat UV60-0.58 Positive DUV Photoresist at 3000 rpm for 40 s.
    (b) Bake at 130 °C for 1 min.
    (c) Expose mesa pattern by electron beam - dose: 25 µC cm^{-2}.
    (d) Post-exposure bake immediately after removing sample from vacuum, at 130 °C for 1 min.
    (e) Develop in Microposit MF CD-26 for 90 s, with strong agitation.
    (f) Cover exposed metallic alignment crosses to protect etchant. If covering manually, use chilled S1805 resist. Alternatively, over-expose area in EBL to use negative property of UV60-0.58.
    (g) Etch following the same method as with previous devices (Appendix A.1 step 3), with 13.75 g citric acid dissolved in 13.75 ml DI water, with 100 ml DI water, 2.5 ml hydrogen peroxide and 1.5 ml (ortho)phosphoric acid. Covering etchant when not in use is recommended.
4. Permalloy Contact Deposition:
    (a) Spin-coat ZEP520A resist at 2000 rpm for 40 s (500 nm thickness).
    (b) Bake at 180 °C for 2 min.

(c) Expose Py contact pattern by electron beam with dose of 165 μC cm^{-2}.

(d) Develop in ZED-N50 for 90 s, with IPA rinse followed by DI water.

(e) O_2 plasma ash for 30 s at 50 W power.

(f) Ar plasma ash for 80 s.

(g) Deposit 60 nm $Ni_{0.8}Fe_{0.2}$ by electron beam evaporation (1.5 Å/s deposition rate), with a ± 30 ° tilt along the length of the NiFe contact to improve mesa edge coverage, tilting at a rate of 5 °/s.

(h) Lift-off in Microposit Remover 1165 (NMP), and rinse with a double IPA bath followed by DI water.

5. Cr/Au Ohmic Contact Deposition:

   (a) Spin-coat ZEP520A at 2000 rpm for 40 s (500 nm thickness).

   (b) Bake at 180 °C for 2 min.

   (c) Expose ohmic contact pattern by electron beam - dose: 25 μC cm^{-2}.

   (d) Develop in Microposit MF CD-26 for 90 s, with strong agitation.

   (e) Electron beam evaporate Cr/Au at a thickness of 5/60 nm.

   (f) Lift-off in Microposit Remover 1165 (NMP), and rinse with a double IPA bath followed by DI water.

6. Back Gate and Top Gate Deposition:

   (a) Spin-coat PMMA 495 K A8 at 3000 rpm for 40 s.

   (b) Bake at 180 °C for 1 min.

   (c) Electron beam evaporate Cr/Au 5/95 nm to the back of the sample.

   (d) Clean PMMA in acetone.

   (e) Deposit 30 nm Al_2O_3 thermally (water precursor) by ALD, 200 °C for 300 cycles.

   (f) Spin-coat ZEP520A at 2000 rpm for 40 s (500 nm thickness).

   (g) Bake at 180 °C for 2 min.

   (h) Expose top gate pattern by electron beam - dose: 25 μC cm^{-2}.

   (i) Develop in Microposit MF CD-26 for 90 s, with strong agitation.

   (j) Electron beam evaporate Cr/Au at a thickness of 5/95 nm.

   (k) Lift-off in Microposit Remover 1165 (NMP), and rinse with a double IPA bath followed by DI water.

A.4 Nano-Scale Py Contact on InAs/GaSb QW TLM Device Fabrication Method: Photolithography and EBL Version

1. Sample Cleaning:
   (a) Clean in acetone, isopropyl alcohol (IPA) and twice in deionised (DI) water, agitating by hand as the wafers are sensitive to even low ultrasonic powers.
   (b) Store sample in a desiccator when not in use.
2. Alignment Marker Patterning:
   (a) Spin-coat SurPass 4000 Adhesion Promoter at 3000 rpm for 40 s, cleaning with IPA when ∼25 s remain.
   (b) Spin-coat LOR 3B at 3000 rpm for 40 s.
   (c) Bake at 180 °C for 3 min.
   (d) Spin-coat S1805 Positive Photoresist at 3000 rpm for 40 s.
   (e) Bake at 115 °C for 1 min.
   (f) Expose alignment cross pattern on MLA - dose: 100 J/cm^2.
   (g) Develop in H_2O:MF 351 (3.5:1) for 2 min. Rinse in DI water × 2.
   (h) O_2 plasma ash for 30 s at 50 W power.
   (i) Thermally evaporate Ti/Au/Ti at thicknesses of 5/60/5 nm.
   (j) Lift-off in acetone.
3. Mesa Patterning and Wet Etch:
   (a) Spin-coat SurPass 4000 Promoter at 3000 rpm for 40 s, cleaning with IPA when ∼25 s remain.
   (b) Spin-coat S1805 Positive Photoresist at 3000 rpm for 40 s.
   (c) Bake at 115 °C for 1 min.
   (d) Expose mesa pattern on MLA (inverted so the mesa is unexposed, increasing exposure boundaries) - dose: 90 mJ cm^{-2}, focus: manual.
   (e) Develop in H_2O:MF351 3.5:1 for 60 s (this ensures oxidised GaSb cap is sufficiently removed). Rinse in DI water × 2.
   (f) Etch following the same method as with previous devices (Appendix A.1 step 3), with 13.75 g citric acid dissolved in 13.75 ml DI water, with 100 ml DI water, 2.5 ml hydrogen peroxide and 1.5 ml (ortho)phosphoric acid. Covering etchant when not in use is recommended.
4. Permalloy Contact Deposition:

(a) Spin-coat ZEP520A resist at 2000 rpm for 40 s (500 nm thickness).
(b) Bake at 180 °C for 2 min.
(c) Expose Py contact pattern by electron beam with dose of 165 μC cm^{-2}.
(d) Develop in ZED-N50 for 90 s, with IPA rinse followed by DI water.
(e) O_2 plasma ash for 30 s at 50 W power.
(f) Ar plasma ash for 80 s.
(g) Deposit 60 nm $Ni_{0.8}Fe_{0.2}$ by electron beam evaporation (1.5 Å/s deposition rate), with a ± 30° tilt along the length of the NiFe contact to improve mesa edge coverage, tilting at a rate of 5 °/s.
(h) Lift-off in Microposit Remover 1165 (NMP), and rinse with a double IPA bath followed by DI water.

5. Cr/Au Ohmic Contact Deposition:

   To reduce exposure time, it is possible to divide the ohmic contact step into a two-step process, where the nano-scale features are formed by electron beam lithography and the larger features are added after as a photolithography process. In this instance, the ohmic contact pattern would require splitting into two patterns (a nano-scale layer and a micron-scale layer). The nano-scale layer would follow the main process outlined below, and the micron-scale layer would follow the optional steps (g) to (p).

   (a) Spin-coat ZEP520A at 2000 rpm for 40 s (500 nm thickness).
   (b) Bake at 180 °C for 2 min.
   (c) Expose ohmic contact pattern by electron beam - dose: 25 μC cm^{-2} (or nano-scale features of ohmic contact pattern if following the two-step process).
   (d) Develop in Microposit MF CD-26 for 90 s, with strong agitation.
   (e) Electron beam evaporate Cr/Au at a thickness of 5/60 nm.
   (f) Lift-off in Microposit Remover 1165 (NMP), and rinse with a double IPA bath followed by DI water.

   Optional (if micron-scale features have been patterned on separate layer):

   (g) Spin-coat MAA 8.5 MMA EM11 Photoresist (filtered) at 3000 rpm for 40 s.
   (h) Bake at 180 °C for 2 min.
   (i) Spin-coat S1805 Positive Photoresist at 3000 rpm for 40 s.
   (j) Bake at 115 °C for 1 min.
   (k) Expose second ohmic contact pattern on MLA - dose: 90 mJ cm^{-2}, focus: manual.
   (l) Develop in H_2O:MF351 3.5:1 for 60 s. Rinse in DI water × 2.
   (m) Expose MMA layer in UVO for 30 min, + 5 min wait to reduce ozone.

(n) Develop in IPA:H_2O (7:3) for 2 min, followed by IPA rinse for 1 min. Rinse in DI water.

(o) Electron beam evaporate 5/160 nm Cr/Au.

(p) Lift-off in acetone.

6. Back Gate and Top Gate Deposition:

   (a) Spin-coat PMMA 495 K A8 at 3000 rpm for 40 s.

   (b) Bake at 180 °C for 1 min.

   (c) Electron beam evaporate Cr/Au 5/95 nm to the back of the sample.

   (d) Clean PMMA in acetone.

   (e) Deposit 30 nm Al_2O_3 thermally (water precursor) by ALD, 200 °C for 300 cycles.

   (f) Spin-coat MAA 8.5 MMA EM11 Photoresist (filtered) at 3000 rpm for 40 s.

   (g) Bake at 180 °C for 2 min.

   (h) Spin-coat S1805 Positive Photoresist at 3000 rpm for 40 s.

   (i) Bake at 115 °C for 1 min.

   (j) Expose second ohmic contact pattern on MLA - dose: 90 mJ cm^{-2}, focus: manual.

   (k) Develop in H_2O:MF351 3.5:1 for 60 s. Rinse in DI water $\times$ 2.

   (l) Expose MMA layer in UVO for 30 min, + 5 min wait to reduce ozone.

   (m) Develop in IPA:H_2O (7:3) for 2 min, followed by IPA rinse for 1 min. Rinse in DI water.

   (n) Electron beam evaporate 5/95 nm Cr/Au.

   (o) Lift-off in acetone.

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