Fabrication and Characterisation of Buffer Layers in AlGaN/GaN on Si Power Devices

BY

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AUTHOR'S DECLARATION

I declare that the work in this dissertation was carried out in accordance with the requirements of the University's Regulations and Code of Practice for Research Degree Programmes and that it has not been submitted for any other academic award. Except where indicated by specific reference in the text, the work is the candidate's own work. Work done in collaboration with, or with the assistance of others, is indicated as such. Any views expressed in the dissertation are those of the author.

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ABSTRACT

While silicon (Si) is reaching its performance limits, gallium nitride (GaN) has become the preferred choice for power electronics due to its superior properties. Carbon (C) doping is widely used to achieve high buffer resistivity, yet its intrinsic charge transport behaviour remains insufficiently understood. This thesis systematically investigates the role of carbon doping in GaN buffer structures.

A detailed analysis of carbon-doped GaN (CGaN) layers revealed a monotonic relationship between positive charge storage and carbon concentration. For the first time, dynamic R_{ON} was found to decrease with increasing carbon, contradicting prior assumptions. This was attributed to the evolution of prominent vertical leakage paths along the dislocation. Additionally, carbon incorporation was observed to enhance crystal quality.

The impact of CGaN thickness was further examined. While thicker buffers are conventionally favoured for high breakdown voltage, this study found that thinner CGaN layers improve crystal quality and exhibit lower dynamic R_{ON}. High-resolution X-ray diffraction (HRXRD) analysis indicated dislocation segregation as a key factor.

The effect of varying carbon concentration in the strain relief layer (SRL) was also investigated. Wafers with lower SRL carbon exhibited gap dependency due to enhanced lateral leakage, whereas those with higher carbon showed dominant vertical leakage, indicating weakly gap-dependent behaviour. The highest SRL carbon concentration resulted in the highest positive charge storage and the lowest dynamic R_{ON}. At high substrate bias, electron injection was more prominent in wafers with lower SRL carbon, reinforcing the need for high SRL resistivity.

Finally, a C-Si co-doped buffer layer was introduced. While the Si incorporation improved the crystal quality, an increased substrate leakage and dynamic R_{ON} degradation can be observed with increasing Si. These findings offer critical insights into GaN buffer design, reinforcing the need for highly resistive buffer structures.

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1. Introduction

1.1 Background and State of the Art

As of 2025, the demand for high-power electronic solutions is accelerating due to the rise of AI-driven servers and the rapid expansion of electric vehicles (EVs). Existing power grids and server infrastructures are struggling to keep up with these growing requirements, necessitating the adoption of more efficient semiconductor technologies [1] [2]. Benefitting from the momentum, Gallium Nitride (GaN)-based high-electron-mobility transistors (HEMTs) have emerged as a disruptive technology, redefining power and radio frequency (RF) applications by pushing the limits of efficiency and performance. This advancement is particularly crucial for 5G commercial wireless infrastructure and military radar applications, where GaN's superior power density and high-frequency capabilities provide a competitive advantage over traditional silicon (Si) and silicon carbide (SiC)-based devices [3].

Beyond power electronics, GaN is revolutionising optoelectronics, with GaN-based micro-LEDs rapidly gaining traction in display technologies, automotive lighting, and visible light communication (VLC). The superior energy efficiency and longevity of GaN LEDs are driving the replacement of traditional fluorescent and incandescent lighting solutions, further cementing their role in everyday applications [4] [5] [6].

While SiC is expected to capture approximately 25% of the power electronics market share by 2028 [6], GaN offers distinct advantages. As a material, GaN has inherited higher electron mobility (up to 2000cm^2/Vs), a larger saturation velocity (2.5x10^7cm/s), a wider bandgap, and a greater critical electric field strength, making it an ideal candidate for high-temperature (HT) and high-power applications [2] [7] [8]. Wide-bandgap semiconductors, such as GaN and SiC, also exhibit lower intrinsic carrier concentrations, allowing them to operate efficiently under extreme thermal conditions. Building on these intrinsic properties, GaN-based devices have been shown to perform reliably in high-temperature environments, including geothermal energy exploration, jet engines, hypersonic vehicles, and space applications, where operational capabilities beyond 300°C are required. Indeed, state-of-the-art GaN devices have demonstrated stable operation up to 500°C [9] [8]. Conversely, while the intrinsic material properties of GaN remain largely unchanged with temperature, GaN-based devices that exploit the 2DEG channel exhibit remarkable performance improvements at cryogenic temperatures. In such devices,

reduced carrier scattering enhances threshold voltage stability and significantly lowers on-resistance[10], underscoring the distinction between bulk material properties and device-level behaviour.

While many argue that both GaN and SiC are well-suited for overlapping applications in automotive and high-power electronics, GaN technology's advantages extend beyond its fundamental material properties. It offers higher power density (exceeding 10 kW), faster switching speeds, and greater efficiency, with switching energy approximately 50% lower than that of SiC [11], directly translates to reduced power losses. Additionally, GaN devices benefit from zero reverse recovery charge due to their lateral structure, which lacks both P and N junctions. A key advantage of GaN is its lower upfront cost, making it an attractive choice for next-generation power applications [11]. Although the number of devices per wafer depends on wafer size, the substrate cost is a major differentiator between GaN and SiC. GaN benefits from growth on widely available silicon substrates, significantly lowering manufacturing costs compared to SiC [9] [8]. Recently, Infineon has introduced 8-inch (200 mm) GaN-on-silicon wafer production, further enhancing cost efficiency and scalability for high-volume applications. Furthermore, GaN's ability to operate at high temperatures with minimal degradation underscores its potential for long-term reliability in extreme environments [9] [11] [8].

The transition of GaN from academic research to commercial adoption has taken nearly two decades, with extensive collaboration between academia and industry driving its maturation. Over the past decade, 650V lateral enhancement-mode GaN-on-Si and cascode devices have gained substantial market share, particularly in consumer electronics. The highest commercially available breakdown voltage for lateral GaN devices currently stands at 1250 V, further demonstrating the rapid advancements in GaN technology [8] [12]. Since the early 2010s, GaN's presence has also expanded into low-voltage applications, fuelling further research into its integration into compact, high-performance power solutions.

Despite these advantages, GaN still faces significant challenges. Trapping-related issues remain a major barrier, affecting threshold voltage stability and dynamic R_{ON} (also known as current collapse), driven by surface traps, buffer traps, hot electrons, or interface traps [13] [8]. While vertical GaN devices promise superior high-voltage blocking capabilities, lateral GaN HEMTs continue to dominate due to their high electron mobility and the formation of a two-dimensional electron gas (2DEG), which is crucial for efficient switching applications. To fully realise GaN's potential, minimising current collapse

through improved buffer layer engineering is essential. Addressing dislocation densities and optimising thermal performance will be key to enhancing breakdown voltage and long-term reliability.

However, industrial applications continue to push for higher breakdown voltages and improved high-temperature performance. One of the primary reasons behind the current collapse and the resulting reduction in breakdown voltage is the high density of threading dislocations in GaN when grown on foreign substrates, which impacts device reliability and performance [8] [14]. Additionally, GaN's relatively low thermal conductivity leads to localised hotspots, affecting long-term reliability [2]. While native GaN substrates can mitigate some of these challenges, their highcost limits widespread adoption in mass production. As a result, research into alternative substrates such as Si, SiC, sapphire (Al_2O_3), diamond [15] [16], bulk aluminium nitride (AlN) [17], and gallium oxide (Ga_2O_3) continues to evolve. By 2028, the substrate market for GaN devices is expected to reach $264.5M, underscoring the growing focus on improving GaN crystal quality and thermal management [6].

1.2 Motivations for Thesis

Power GaN HEMTs are conventionally capable of sustaining higher electric fields during OFF-state operation. One of the key points reiterated throughout the preceding chapters is that nitride-based semiconductors such as GaN, AlGaN, and AlN offer significant advantages, including the ability to withstand high off-state voltages, support high power densities, and maintain low on-resistance [18] [19]. Exposure to high electric fields can induce both vertical (between the drain and the substrate) and lateral (between the drain and the source) breakdown, as well as charge trapping effects. Notably, vertical breakdown is strongly influenced by buffer composition, thickness, and crystal quality.

A typical GaN-on-Si epitaxial growth process begins with an AlN nucleation layer, followed by a strain relief layer (SRL), a carbon-doped GaN buffer layer, a UID layer, and an AlGaN barrier. The AlN nucleation layer primarily mitigates the detrimental effects arising from the significant lattice and thermal expansion coefficient mismatch between GaN and the substrate. As mentioned before, this mismatch can introduce threading dislocation densities (TDDs) [14], and the unwanted diffusion of Si into the epitaxial layers [19] [20] [21] [22]. Additionally, a phenomenon known as the GaN "melt-back" can occur if GaN is grown directly on a Si substrate at high temperatures. This results from the reaction between the GaN precursor reacting with Si, forming a Ga-Si eutectic

mixture, with a relatively lower melting point than Si, with no dissolved GaN. A thin AlN layer acts as an effective barrier, preventing this eutectic reaction.

To address these challenges, thick buffer layers are commonly employed. However, increasing the buffer layer thickness raises epitaxial growth costs due to longer processing times. In most commercial devices, the "buffer" is not a single layer but rather a combination of a strain relief layer and a carbon-doped GaN (CGaN) layer. An ideal buffer structure should maximise voltage blocking capability, ultimately defining the device's critical electric field while minimising leakage currents.

While carbon is not the only dopant incorporated into the buffer, it is widely used in high-voltage power applications to create an isolating layer and electrically separate the active layers from the substrate [23]. However, despite its intended benefits, carbon doping introduces significant challenges, particularly dynamic R_{ON} degradation, which leads to switching-related issues and long-term reliability concerns. Although numerous strategies have been explored to mitigate these effects, further investigation is required to fully understand and optimise buffer design for improved performance and reliability in high-voltage GaN power devices.

1.3 Thesis Outline

The primary focus of this thesis is on the buffer layer of AlGaN/GaN high-electron-mobility transistors (HEMTs) and its impact on improving dynamic R_{ON}. The buffer layer plays a crucial role in voltage blocking, reducing leakage currents, limiting threading dislocation propagation, and mitigating charge trapping effects, all of which influence charge transport under high-voltage off-state operation.

Chapter 1 provides a state-of-the-art overview of GaN technology, outlining its current advancements and the key challenges it faces, particularly in power electronics.

Chapter 2 introduces the fundamental physics of GaN as a semiconductor material, including the formation of the two-dimensional electron gas (2DEG), various growth techniques, and commonly used doping strategies. The functionality of each layer in a GaN HEMT structure is detailed, followed by a discussion of fabrication and characterisation techniques. Additionally, the TCAD simulation methodology, which is employed throughout this work, is introduced.

A key aspect of this research is that all devices studied in the following chapters were fabricated at the University of Sheffield cleanroom using commercially grown MOCVD

GaN-on-Si wafers from the same manufacturer. One specific wafer, with a carbon doping concentration of 1×10^{19} cm^{-3}, is consistently shared across Chapters 3, 4, and 5. Various experimental techniques, including substrate ramp measurements, substrate transients, high-resolution X-ray diffraction (HRXRD), and TCAD simulations, have been employed to interpret the results.

Core Research Contributions

Chapter 3 represents the core of this thesis, investigating the impact of varying carbon doping concentrations (2×10^{18} cm^{-3}, 6×10^{18} cm^{-3}, and 1×10^{19} cm^{-3}) in the carbon-doped GaN (CGaN) layer on dynamic R_{ON}. Electrical characterisation was carried out using transfer length method (TLM) structures, along with ring-shaped ohmic structures to examine contact resistance. Substrate ramp measurements were performed on three wafers at –300 V and –550 V with a 10 µm gap, allowing for the identification of dominant leakage paths and an analysis of charge transport mechanisms along dislocations.

Chapter 4 extends this study by exploring the influence of CGaN buffer layer thickness and undoped GaN (UID) layer thickness on device performance. Eight wafers, all with the same carbon doping concentration, were investigated in two groups:

1. Group A - Wafers with varying C-GaN layer thicknesses
2. Group B - Wafers with variations in both C-GaN and UID layer thicknesses

The impact of dislocation propagation due to these structural variations is also discussed in detail. Electrical characterisation was performed using a TLM gap of 15 µm for comparison, maintaining the same substrate ramp and transient biasing conditions as in Chapter 3.

Chapter 5 shifts focus to the strain relief layer (SRL) and examines the impact of carbon doping concentration variations within this layer. Similar to Chapter 4, gap 15 µm structures were used for comparison, and the substrate ramp and transient biasing conditions remained the same as in the previous chapters to ensure consistency in evaluating charge transport behaviour.

Chapter 6 explores the effects of silicon and carbon co-doping in the buffer. A carbon doping concentration of 2×10^{19} cm^{-3} was used, with Si concentrations of 5×10^{16} cm^{-3}, 1×10^{17} cm^{-3}, and 2×10^{17} cm^{-3}. The results provide insight into the complex interplay between carbon and silicon in modifying electrical properties.

Chapter 7 summarises the key findings of this thesis and discusses potential directions for future research to optimise buffer layer design further and enhance the performance of GaN power devices.

1.4 References

[1] C. Restrepo, “RENEWABLE ENERGY - Smaller Size • Higher Efficiency • Lower System Cost,” gansystems.com, 2019.

[2] J. Mendes, M. Liehr and C. Li, “Diamond/GaN HEMTs: where from and where to?,” Materials 2022, vol. 15, p. 415, 2021.

[3] F. Iucolano and T. Boles, “GaN-on-Si HEMTs for wireless base stations,” Materials Science in Semiconductor Processing, vol. 98, pp. 100-105, 2019-08.

[4] Z. Xu, W. Niu, Y. Liu, X. Lin, J. Cai, J. Shi, X. Wang, G. Wang, J. Zhang, F. Jiang, Z. He, S. Yu, C. Shen, J. Zhang and N. Chi, “31.38 Gb/s GaN-based LED array visible light communication system enhanced with V-pit and sidewall quantum well structure,” Opto-Electronic Science, vol. 2, no. 5, pp. 230005-230005, 2023-07.

[5] G. Verzellesi, “Wide Bandgap Based Devices - Design, Fabrication and Appliocations, Volume ii,” Micromachines, vol. 13, p. 403, 2022.

[6] www.smeicondcutor-today.com, “Market Focus : Substrates (Emerging substrates market growing at 27% CAGR to over $264m by 2028),” SemiconductorsTODAY, vol. 18, no. 5, pp. 88-89, 2023.

[7] M. A. Alim, C. Gaquiere and G. Crupi, “ An experimental and systematic insight into the temperature sensitivity for a 0.15-μm gate-length HEMT based on the GaN technology,” Micromachines (Basel), vol. 12, no. 5, p. 549, 2021-05.

[8] M. Meneghini, C. De Santi, I. Abid, M. Buffolo, M. Cioni, R. A. Khadar, L. Nela, N. Zagni, A. Chini, F. Medjdoub, G. Meneghesso, G. Verzellesi, E. Zanoni and E. Matioli, “GaN-based power devices: Physics, reliability, and perspectives,” Journal of applied physics, , vol. 130, no. 18, p. 181101, 2021.

[9] J. Niroula, M. A. Taylor, Q. Xie, P. Yadav, S. Luo, Y. Zhao and T. Palacios, “Record High Temperature Performance in Scaled AlGaN/GaN-on-Si HEMTs up to 500°C,” in 2024 Device Research Conference (DRC),, College Park, MD, USA, 2024.

[10] L. Nela, N. Perera, C. Erine and E. Matioli, “Performance of GaN Power Devices for Cryogenic Applications Down to 4.2 K,” IEEE transactions on power electronics, vol. 36, no. 7, pp. 7412-7416, 2021-07.

[11] M. Beheshti, “Wide-bandgap semiconductors: Performance and benefits of GaN versus SiC,” Analog Design Journal - Texas Instruments , vol. ADJ 4Q , pp. 1-6, 2020.

[12] K. Varadarajan, “Reaching Beyond 1200 V: Lateral GaN HEMTs for High-Reliability EV and Industrial Applications,” Power Integrations, San Jose, California, 2024.

[13] K. B. Lee, R. T. Green, P. A. Houston, W. S. Tan, M. J. Uren, D. J. Wallis and T. Martin, “Bi-layer SixNy passivation on AlGaN/GaN HEMTs to suppress current collapse and improve breakdown,” Semiconductor science and technology, vol. 25, no. 12, p. 125010, 2010-12.

[14] C. A. Robertson, K. S. Qwah, Y.-R. Wu and J. S. Speck, “Modeling dislocation-related leakage currents in GaN p-n diodes,” Journal of applied physics,, vol. 126 , no. 24, p. 245705, 2019-12.

[15] M. Malakoutian, D. E. Field, N. J. Hines, S. Pasayat, S. Graham, M. Kuball and S. Chowdhury, “Record-Low Thermal Boundary Resistance between Diamond and GaN-on-SiC for Enabling Radiofrequency Device Cooling,” ACS applied materials & interfaces, vol. 13, no. 50, pp. 60553-60560, 2021-12.

[16] “14 - GaN-on-diamond materials and device technology: A review,” Francis, Daniel,; Kuball, Martin.;, vol. Thermal Management of Gallium Nitride Electronics, pp. 295-331, 2022.

[17] M. Miyoshi, S. Tanaka, T. Kawaide, A. Inoue and T. Egawa, “DC and Pulse I–V Characteristics of Strain-Engineered AlGaInN/GaN HEMTs fabricated on Single-Crystal AlN Substrate,” Physica status solidi. A, Applications and materials science, vol. 220, no. 16, p. 2200733, 2023-08.

[18] F. Medjdoub, J. Derluyn, K. Cheng, M. Leys, S. Degroote, D. Marcon, D. Visalli, M. Van Hove, M. Germain and G. Borghs, “Low On-Resistance High-Breakdown Normally Off AlN/GaN/AlGaN DHFET on Si Substrate,” IEEE electron device letters, , Vol, p.111-113, Article 5378574, vol. 31, no. 2, pp. 111-113, 2010-02.

[19] K. J. Chen, O. Haberlen, A. Lidow, C. L. Tsai, T. Ueda, Y. Uemoto and Y. Wu, “GaN-on-Si Power Technology: Devices and Applications,” IEEE transactions on electron devices, vol. 64, no. 3, pp. 779-795, 2017-03.

[20] Y. Lin, M.-L. Kao, Y.-C. Weng, C.-F. Dee, S.-C. Chen, H.-C. Kuo, C.-H. Lin and E.-Y. Chang, “Buffer Traps Effect on GaN-on-Si High-Electron-Mobility Transistor at Different Substrate Voltages,” Micromachines (Basel), vol. 13, no. 12, p. 2140, 2022-12.

[21] H.-P. Lee, J. Perozek, L. D. Rosario and C. Bayram, “Investigation of AlGaN/GaN high electron mobility transistor structures on 200-mm silicon (111) substrates employing different buffer layer configurations,” Scientific reports, vol. 6, no. 1, pp. 37588-37588, 2016-11.

[22] T. Hamachi, T. Tohei, Y. Hayashi, M. Imanishi, S. Usami, Y. Mori and A. Sakai, “Comprehensive analysis of current leakage at individual screw and mixed threading dislocations in freestanding GaN substrates,” Scientific reports, vol. 13, no. 1, pp. 2436-2436, 2023-02.

[23] M. Singh, M. J. Uren, T. Martin, S. Karboyan, H. Chandrasekar and M. Kuball, “"Kink” in AlGaN/GaN-HEMTs: floating buffer model,” IEEE Transactions on Electron Devices, vol. 65, no. 9, pp. 3746-3753, 2018.

[24] S. Yang, S. Han, K. Sheng and K. J. Chen, “Dynamic On-Resistance in GaN Power Devices: Mechanisms, Characterizations, and Modeling,” IEEE journal of emerging and selected topics in power electronics, vol. 7, no. 3, pp. 1425-1439, 2019-09.

[25] S. Lee, M. S. Abbas, D. Yoo, K. Lee, T. G. Fabunmi, E. Lee, H. I. Kim, I. Kim, D. Jang, S. Lee, J. Lee, K.-T. Park, C. Lee, M. Kim, Y. S. Lee, C. S. Chang and Y, “Pulsed-mode metalorganic vapor-phase epitaxy of GaN on graphene-coated c-sapphire for freestanding GaN thin films,” Nano letters, , vol. 23, no. 24, pp. 11578-11585, 2023-12.

[26] M. Meneghini, D. Bisi, D. Marcon, S. Stoffels, M. Van Hove, T.-L. Wu, S. Decoutere, G. Meneghesso and E. Zanoni, “Trapping and reliability assessment in D-mode GaN-based MIS-HEMTs for power applications,” IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2199-2207, 2013.

2. Theoretical Background

This chapter examines the exceptional properties of gallium nitride (GaN) that make it a promising material for high-power electronic applications. The growth techniques used to produce high-quality GaN crystals and the typical epitaxial structure of a lateral GaN high-electron-mobility transistor (HEMT) are explored. To establish a solid foundation for the following chapters, key semiconductor physics concepts relevant to GaN devices are discussed. Additionally, the fabrication techniques used to produce GaN-based devices and the measurement methods employed to evaluate their performance are outlined.

2.1 Gallium Nitride (GaN)

2.1.1 Material properties

III-Nitride materials, such as GaN, exhibit a distinct crystal structure compared to other III-V compound semiconductors, such as indium phosphide (InP) and gallium arsenide (GaAs). GaN predominantly exists in the wurtzite crystal structure, which is thermodynamically more stable than zinc-blende or rock salt structures, making it ideal for electronic components.

The wurtzite structure of GaN features alternating layers of gallium (Ga) and nitrogen (N) atoms arranged in a hexagonal pattern. Each Ga atom is bonded to four N atoms and vice versa, forming a tetrahedral arrangement as presented in Figure 2.1(a). The crystal structure can be defined by two key lattice constants: **a**, which corresponds to the in-plane distance between the atoms in the basal plane and **c**, which represents the height of the hexagonal prism along the c-axis (0001) [4]. However, the layers are slightly misaligned, with a displacement of 5/8 of the lattice constant c along the c-axis (0001) [3].

Two primary faces are considered in wurtzite GaN: Ga-faced and N-faced (Figure 2.1). Crystals grown along the c-axis (0001) direction are termed Ga-polar, with the vector perpendicular to the hexagonal column. Conversely, N-polar crystals are grown in the opposite direction (000_1), resembling a mirror image of the Ga-faced crystals [3].

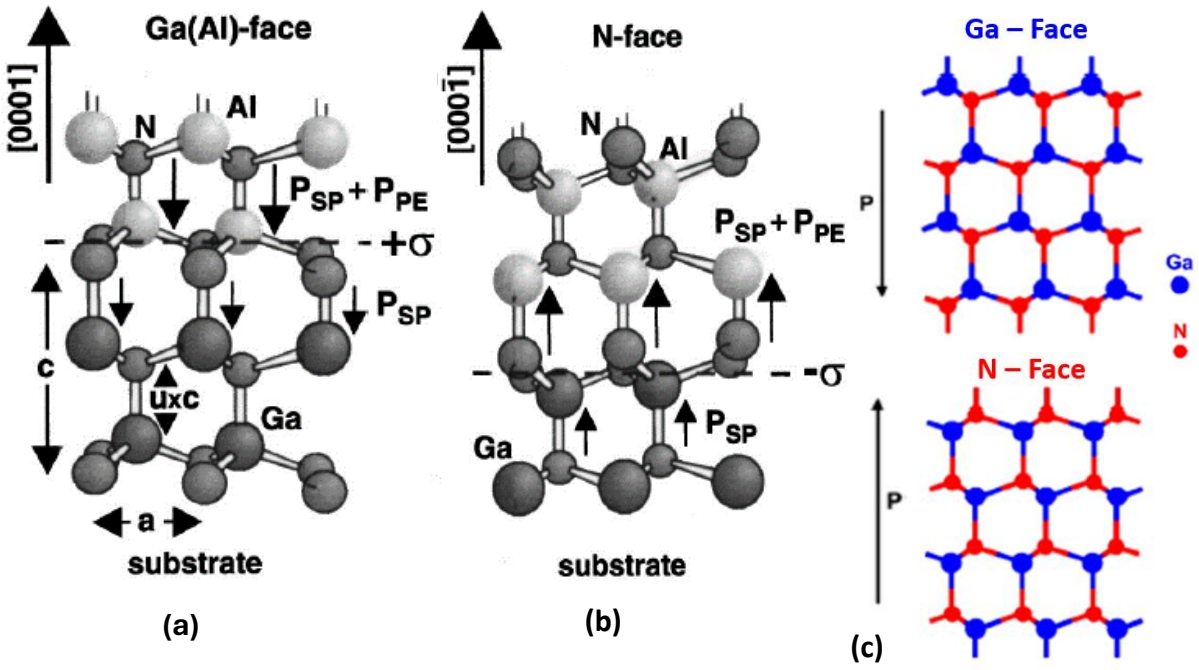

Figure 2-1 - 3D prospective view of the of AlGaN/GaN wurtzite crystal structure (a) Ga – face (b) N – face polarity [1] (c) indicates the more simplified view of the bonds [2]

The Ga-N bond is partially ionic due to the significant electronegativity difference between Ga and N atoms. Nitrogen is approximately 70% more electronegative than Ga, creating a dipole moment. In the wurtzite crystal structure of GaN, these dipoles align along the c-axis, giving rise to a net polarisation, as illustrated in Figure 2.1(a) and (b). Notably, the wurtzite structure inherently lacks inversion symmetry due to its atomic arrangement [3]. Consequently, even if the structure is inverted along the c-axis, the resulting configuration is not identical to the original.

2.1.2 Origin of the 2DEG and Polarisations

(a) Spontaneous Polarisation

As mentioned in the previous section, N has a higher electronegativity compared to the Ga atoms. As a result, both atoms exhibit anionic (-) and cationic (+) characteristics, leading to a bond with an uneven distribution of charge. In essence, the Ga–N bond is partially ionic, with the more electronegative N atom pulling electron density away from the Ga nuclei. However, the presence of spontaneous polarisation (P_{SP}) in wurtzite GaN is not solely due to this electronegativity difference. It also stems from the intrinsic asymmetry of the crystal structure, particularly the non-ideal c/a ratio, which distorts the tetrahedral coordination and leads to a net dipole along the c-axis [4]. In summary, even in the absence of external strain, the spontaneous polarisation exists in the wurtzite

crystal structure due to both the nature of the chemical bonds and the geometry of the crystal as observed in the untrained crystals.

The direction of the net polarisation depends on the polarity of the material and the P_{SP}. For the Ga-face structures, as illustrated in Figure 2.2 (a), the P_{SP} of both the AlGaN barrier layer and the GaN layer is negative, thus always pointing towards the substrate. Similarly, for the N-face structures, the direction of polarisation is inverted, pointing away from the substrate. In summary, the P_{SP} vector along the (0001) direction points from the Ga atom towards the nearest N atom [2] [4].

The spontaneous polarisation along the (0001) direction can be denoted as:

$$\overrightarrow{P_{SP}} = P_{SP} * z \tag{1}$$

Where z is the unit vector in the z direction.

(b) Piezoelectric Polarization

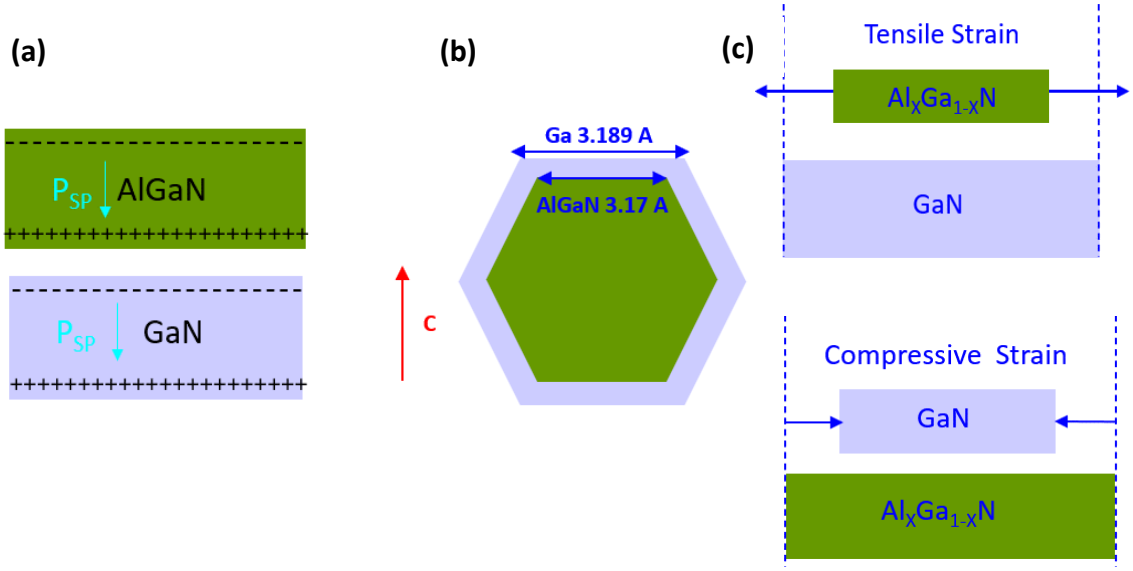

Figure 2-2 - (a) Spontaneous polarisation in Ga-face relaxed GaN and AlGaN (b) Lattice mismatch between AlGaN and (c) GaN: tensile strain in AlGaN grown on relaxed GaN and compressive strain in GaN grown on relaxed AlGaN

As seen in Figure 2.2(c), when an AlGaN layer is grown on top of a relaxed GaN layer, the AlGaN layer will be under tensile strain due to its inherently smaller lattice constant. The piezoelectric polarisation (P_{PZ}) arises from the strain or stress in the AlGaN barrier layer caused by the lattice mismatch between the AlGaN and GaN layers. The piezoelectric polarisation induced along the c-axis can be defined as:

$$P_{PZ(AlGaN)} = e_{33}\epsilon_x + e_{31}(\epsilon_x + e_y) \tag{2}$$

where $\epsilon_x = \frac{(c - c_0)}{c_0}$ is the strain along the c-axis, and the isotropic in-plane strain $\epsilon_x = \epsilon_y = \frac{(a - a_0)}{a_0}$. The piezoelectric coefficients e_{33} and e_{31}, a and c are the lattice constants, and c_{13}, c_{33} are the elastic constants of the strained layer [1]. The relationship between the lattice constants in the (0001) direction can be denoted as:

$$\epsilon_x = \frac{(c - c_0)}{c_0} = 2\frac{c_{13}}{c_{33}} . \frac{(a - a_0)}{a_0} \quad (3)$$

Using Equation (2) , the relationship between the lattice constants, elastic constants and the P_{PZ} in the (0001) direction can be expressed as:

$$P_{PZ} = 2\frac{(a - a_0)}{a_0}(e_{31} - e_{33}\frac{c_{13}}{c_{33}}) \quad (4)$$

The magnitude of P_{PZ} is strongly influenced by the Al content (x) in the $Al_xGa_{1-x}N$ barrier layer, as further discussed in Section 2.3.4. In particular, higher Al reduces the lattice constant, thereby increasing the built-in strain and, consequently, the P_{PZ}. However, when the AlGaN barrier layer thickness exceeds a critical value, strain relaxation may occur, diminishing the polarisation effect. The polar nature of the Al-N bond, driven by the greater electronegativity difference between Al and N compared to Ga-N, further enhances the overall polarisation in AlGaN.

P_{PZ} exists parallel to the P_{SP}, and in the absence of an external electric field, the total polarisation (P) of the GaN/AlGaN layer is the sum of both the P_{SP} and P_{PZ} [2];

$$P = P_{PZ} + P_{SP} \quad (5)$$

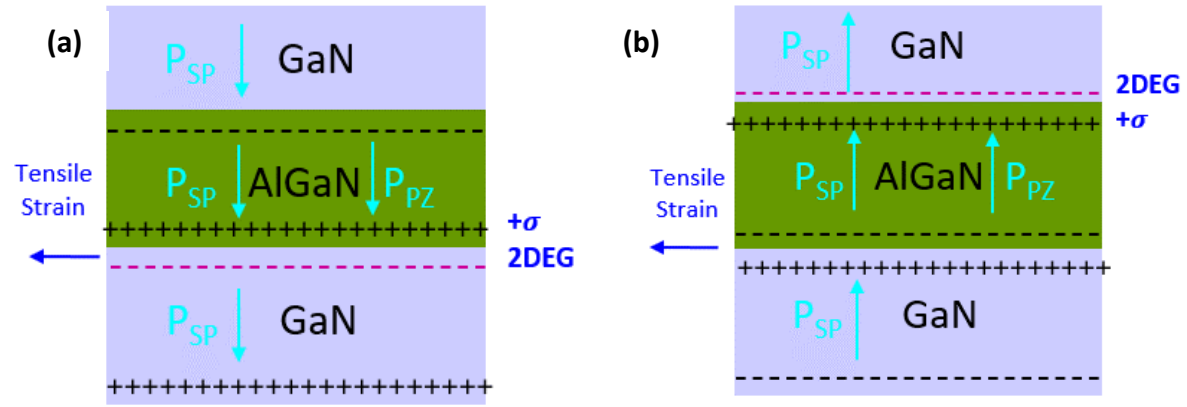

Figure 2-3 - Polarisation effect in (a) Ga-face and (b) N-face AlGaN/GaN heterostructure. Induced tensile strain due to the lattice mismatch between the AlGaN layer grown on the relaxed GaN for Ga-face epitaxies.

As illustrated in Figure 2.3, in Ga-faced structures, P_{PZ} vector points from the AlGaN surface towards the substrate, whereas in N-faced structures, the direction is reversed, pointing away from the substrate. Consequently, in Ga-faced AlGaN/GaN heterostructures, both the spontaneous and piezoelectric polarisation vectors align in the same direction, creating a strong net polarisation field.

This results in the accumulation of fixed positive polarisation charge at the bottom of the AlGaN layer, which attracts free electrons to the heterointerface, thereby leading to the formation of a 2DEG within the GaN layer.

The charge neutrality of the epitaxy under no bias is expressed as [5]:

$$\sigma_{surface} = qn_s \tag{6}$$

Where the, $\sigma_{surface}$, q, n_s, represent the ionised donor like surface states, the charge of an electron and 2DEG density, respectively.

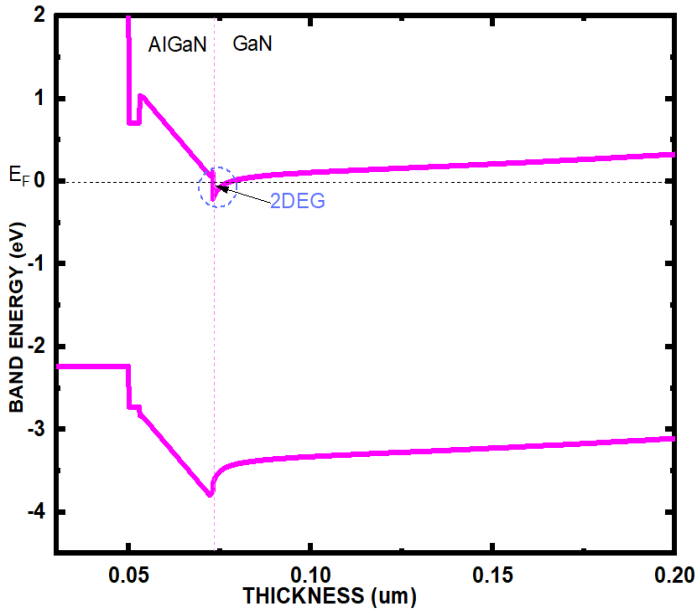

Figure 2-4 - Schematic band diagram of the AlGaN/GaN heterointerface highlighting the electron confinement in a well-defined quantum well.

The source of the electrons in the 2DEG, is believed to originate from donor-like surface states in the AlGaN barrier [4]. The 2DEG density can vary depending on the Al composition and the barrier thickness of the AlGaN layer. As electrons are released from these donor states, they populate the heterointerface, with the Fermi level becoming pinned at the energy level of the surface donor states. This creates a potential well, often referred to as a 'quantum well,' which confines the electrons.

The 2DEG density discussed in the thesis is in the range of ~10^{13} cm^{-2} attributed to an AlGaN barrier with 20% Al composition and 20nm thickness.

Typically, both GaN and the AlGaN barrier layers remain undoped to mitigate the electron scattering due to the impurities. Hence, the undoped GaN (UID) layer often indicates an n-type conductivity, with a background dopant density in the range of 10^{15} – 10^{16} cm^{-3}. This may vary depending on the quality of the epitaxy.

2.2 Epitaxial Growth Techniques & GaN Lateral Transistor Device Architecture

A typical lateral GaN transistor device consists of several epitaxial layers, which will be discussed in detail in this section. This stack of materials, comprising a wider bandgap layer and a lower bandgap layer, forms a 2DEG channel at the heterojunction interface. This 2DEG exists naturally due to polarisation effects within the structure, eliminating the need for intentional doping, unlike traditional silicon MOSFETs.

The presence of the 2DEG makes GaN HEMTs inherently "normally-on" devices, meaning a channel exists even without an applied gate voltage. While this simplifies device operation, it also raises safety concerns, especially for high-voltage applications, as it requires negative supply voltages to turn the device off.

2.2.1 Epitaxial Growth Techniques

The choice of growth technique depends on various factors, such as the desired material quality, growth rate, and, not least, the associated cost. MOCVD is the most commonly used technique due to its versatility and ability to grow GaN films on a large-area substrate [7]. However, MBE and Hydride Vapour Phase Epitaxy (HVPE) are also suitable for specific applications, such as research and development of high-performance devices. Regardless of the choice of the technique, in order to grow high-quality epitaxy with a smooth surface morphology, numerous parameters such as temperature, pressure, gas flow rate and the (V/III) molar ratio must be precisely tuned [6].

(a) Metal Organic Chemical Vapour Depostion (MOCVD)

Typically, MOCVD relies on higher growth temperatures, ranging from 1000°C to 1100°C for GaN growth, as specific chemical reactions [6], particularly the decomposition of ammonia (NH_3), require high temperatures. During the growth process, Ga, Al and indium (I) are incorporated into the system via metal-organic compounds such as

trimethylgallium (TMG), trimethylaluminum(TMA) and trimethylindium(TMI), respectively [8]. Hydrogen (H_2) and nitrogen are typically used as carrier gases to transport these precursors to the heated reaction zone, where a series of gas-phase and surface reactions take place, ultimately leading to GaN film formation [6].

The fundamental reaction responsible for GaN deposition is:

$$Ga(CH_3)_3 + NH_3 \rightarrow GaN + 3CH_4$$

This reaction takes place on the surface of a heated substrate. The substrate is usually placed on a susceptor, which ensures a uniform temperature during growth. In the gas phase, the metal-organic compound (e.g., trimethylgallium) can first react with ammonia to form intermediate compounds, which are then transported to the heated area where GaN is formed. To reduce unwanted side reactions, the process is usually carried out at low pressure [6].

The surface of the substrate plays a vital role in determining how well the GaN grows. The quality and growth rate of the film depend on factors like temperature, the type of carrier gas used, and how many active sites are available on the surface. For example, using hydrogen as the carrier gas at high temperatures can slightly etch the surface, which may affect the growth rate. Carefully controlling these surface conditions helps produce smooth and high-quality GaN layers.

Tokuda. Et al. [10] and Hirero et al.[11] identified three dominant traps in MOCVD-grown n-type GaN samples : two electron traps and one hole trap. They concluded that the concentration of both electron traps and hole traps varies more with the growth technique than with the substrate. Furthermore, any trap with an activation energy of E_V + 0.86 eV [10] is attributed to carbon-related defects, irrespective of the growth technique. Hirero et al. further suggested that these defects behave as significant recombination centres, capturing both electrons and holes. In MOCVD-grown n-type GaN, they proposed that V_{Ga} or V_{Ga}-H complexes are likely to be the negatively charged state, supporting their results at E_V + 0.87eV [11].

(b) Molecular Beam Epitaxy (MBE)

MBE has been widely favoured for growing optoelectronic devices rather than HEMTs, primarily due to its ability to offer precise control over layer thickness, well-defined, sharp interfaces, and highly controlled impurity-free growth. These characteristics are especially critical for optoelectronic applications such as quantum wells and LEDs, where

carrier recombination dynamics and emission properties are susceptible to interface quality and layer uniformity. Operating under ultra-high vacuum conditions, MBE facilitates growth at low temperatures, typically between 600°C and 800°C for GaN, further reducing the formation of defects and dislocations. The low growth temperatures in MBE also minimise the diffusion of certain elements and intermixing at heterojunction interfaces. However, for commercial GaN HEMT production, at high volumes, the high-growth-rate capabilities of other techniques often take precedence over atomic-level precision.

In contrast to MOCVD, MBE uses a Ga effusion cell and a plasma discharge or radio frequency nitrogen source, which generates reactive nitrogen atoms or ions by passing N_2 flow [12] [13]. Solid Ga metal is heated to produce a beam of gallium atoms; thus, these atoms then travel in a vacuum to a heated substrate where they bond with nitrogen to form GaN [12]. The typical GaN growth rate in an MBE system lies approximately within 0.5-1 µm/hr, which is relatively slower compared to MOCVD, making the technique a rather more costly option. Nevertheless, it's widely used in academic research due to the high quality of the resulting material.

In the context of commercial GaN HEMT production, however, where device performance is generally more tolerant of slight interface roughness or impurity levels, high-throughput and cost-efficiency are prioritised. As such, techniques like MOCVD offering considerably higher growth rates are more commonly adopted, despite their somewhat lower atomic-scale precision. While high-quality interfaces remain essential for achieving high electron mobility and minimising scattering in HEMTs, the stringent structural requirements seen in optoelectronic devices are less critical.

Godejohann et al. [7] experimentally demonstrated the contrasting adverse effects of the HEMT samples grown by MBE and MOCVD. They also found that Al distribution is influenced by the growth temperature and the subsequent steps. Using MBE, they successfully achieved a nearly pure AlN barrier and an abrupt junction, resulting in a much lower sheet resistance (R_S) of 200 Ωsq^{-1}. In contrast, the MOCVD-grown sample exhibited a significant amount of Ga diffusion into the AlN layer, leading to a sheet resistance that was twice as high, attributed to the higher growth temperature. Consequently, they concluded that MOCVD could enhance the 2DEG mobility over MBE by a minor change, slightly reducing the growth temperature, at the expense of a slight deterioration of the crystalline quality.

However, with recent advancements such as in-situ reflection high-energy electron diffraction (RHEED) monitoring, etc. [9], MBE is capable of growing fragile epitaxial layers with greater quality [8]. Despite the enhanced crystal quality, GaN growth on non-GaN substrates remains prone to the structural defects due to the lattice mismatch.

(c) Hydride Vapor Phase Epitaxy (HVPE)

HVPE is a chemical vapour deposition (CVD) growth technique which uses hydride (AsH_3, PH_3, NH_3) and chloride (GaCl, $GaCl_3$, InCl) as source materials for the reaction [14]. Particularly, for GaN growth, gallium chloride (GaCl (g)) is produced by reacting Ga (l) with HCl at high temperature, decomposing NH_3 to produce ionised N atoms, which then allows GaCl to react with N_2. H_2 or N_2 are used as the carrier gas [9][13]. Conventionally, this technique is often employed to grow GaN on substrates such as sapphire, silicon carbide (SiC), or GaN templates [9].

HVPE growth reactors typically contain multiple temperature growth zones, ranging from low to high temperatures. The overall operating temperature spans approximately between ~850°C - 1050°C, which is indeed much higher than that of MBE. HVPE has gained prominence in GaN growth due to its ability to grow high-quality, thick layers at a faster growth rate and at substantially lower cost [14]. Consequently, HVPE is frequently used for the growth of bulk GaN substrates [14] [9].

Moreover, a thick GaN template layer (which often acts as a foundation or base layer for further growth processes), grown on a sapphire (Al_2O_3) substrate by HVPE, is a highly popular application. While HVPE is attractive due to its high growth rates and cost-effectiveness, several challenges hinder its suitability for large-scale GaN substrate production. These include controlling self-separation without inducing cracks, whereby the grown GaN layer spontaneously detaches from the seed crystal, typically driven by thermally induced stress during cooldown. This process is desirable as it avoids the need for mechanical slicing, but it must be carefully managed to prevent damage. Other issues involve mitigating impurity incorporation and ensuring consistent crystalline quality over thick layers. Additionally, morphological instabilities such as V-pits and surface roughness can arise during rapid growth, while scaling to larger diameters with uniform quality remains a technical hurdle.

2.3 AlGaN/GaN Epitaxy

The AlGaN/GaN epitaxial wafers on 6-inch Si used in this project were supplied by Nexperia UK Ltd. The epitaxial structure consists of a GaN cap (3 nm), an AlGaN barrier (20 nm), a UID GaN (0.5 µm), a carbon-doped GaN (CGaN) layer (1 µm), an AlN/GaN superlattice (SL) strain relief layer (SRL) buffer (3.3 µm) and an AlN nucleation layer (~140 nm) on a Si substrate (Figure 2.5). This section highlights the role of each individual layer in the epitaxial stack.

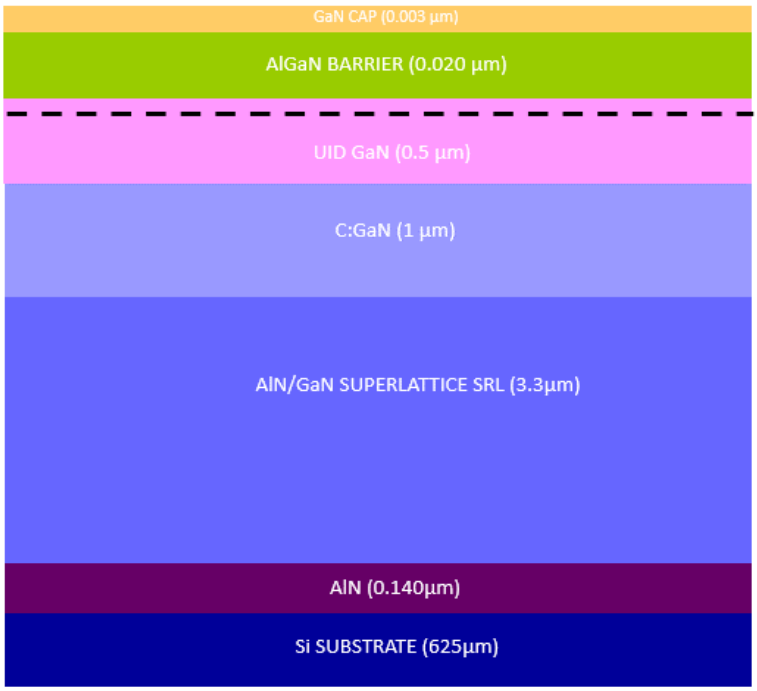

Figure 2-5 - Epitaxial layers of the herein used AlGaN/GaN HEMT

2.3.1 Substrates

While GaN on GaN offers the ideal theoretical lattice match, the scarcity and high cost of native GaN substrates have led to the exploration of foreign substrates for GaN growth. Several potential substrates have been investigated for growing GaN HEMTs, including sapphire (Al_2O_3), Si, SiC, diamond, and freestanding GaN. Table 2.1 presents a comparison of these substrates based on their key parameters. Each substrate has its own advantages and disadvantages, and the optimal choice depends on the specific application and desired properties.

Properties	GaN	Si	SiC	Sapphire	Diamond
Bandgap (eV)	3.42	1.11	3.26	9.9	5.45
Thermal Conductivity at 300K k(W/cm-K)	2	1.5	4.9	0.35	180
Lattice mismatch with GaN (%)	0	17	3.5	14	89
Thermal expansion coefficient (x 10^{-6} K^{-1})	5.5	2.6	4.46	7.5	1.0
Substrate size	30	300	150	150	10
Substrate cost	Very High	Very Low	High	Medium	Extremely High

Table 2.1 - Comparison of the available substrates and their material characteristics [15] [16]

Diamond offers the best thermal conductivity but suffers from the worst lattice mismatch with GaN. The associated high cost and the limited availability of large-area substrates make its integration at larger scales challenging [17]. SiC exhibits the smallest lattice mismatch with GaN among other foreign substrates, resulting in the lowest threading dislocation (TD) density. In addition, SiC offers excellent thermal conductivity [18]. However, due to its high cost, GaN on SiC is primarily used in RF applications [19]. GaN on sapphire, while being a low-cost solution compatible with existing manufacturing processes, has the poorest thermal conductivity, making it unsuitable for high-power applications [20]. However, studies by Saito et al. [2] have shown that thinning the wafer can enhance the thermal conductivity of GaN on sapphire [19].

In contrast to other substrates, Si offers the most cost-effective approach for commercialisation, especially on a large diameter substrate, as the GaN epi-wafers grown on Si can be processed using existing Si fabrication facilities [21] [17] [2]. Si also exhibits good thermal conductivity. However, suppressing lateral and vertical leakage remains a significant challenge due to high dislocation density, cracks, and pits caused by lattice and thermal mismatch [21].

2.3.2 Nucleation layer (NL)

Many GaN-on-Si structures, including those used in our experiments, utilise an AlN nucleation layer (NL) to prevent Ga melt-back etching into the Si substrate [6]. The AlN NL effectively constrains most of the dislocations caused by lattice and thermal mismatch between Si and GaN, minimising cracks and wafer bowing [21] [2] [22].

Koleske et al. [23] concluded in their study that introducing multilayer AlN can lead to the cancellation of dislocations with opposite Burgers vectors. This suggests that the AlN layer acts as a barrier for certain types of dislocations, potentially improving the crystal quality by reducing the overall dislocation density. Yamaoka et al. [24] investigated the correlation between TDs and vertical leakage in AlN layers. They found that screw-type TDs in the AlN layer are the primary source of vertical leakage current [23] [24]. Additionally, both the thickness of the AlN nucleation layer and the AlN growth temperature can influence both vertical leakage [24] and breakdown characteristics [21]. [2]

2.3.3 Buffer layer and Doping

While a semi-insulating GaN buffer is the foundation of most nitride-based devices, lateral conduction structures typically include a semi-insulating buffer layer beneath the channel region to isolate the underlying layers electrically. An unintentionally doped GaN layer grown by MOCVD typically exhibits n-type conductivity due to residual impurities such as Si, oxygen (O), or hydrogen (H) [25] [26]. In contrast, the semi-insulating buffer often exhibits p-type conductivity, resulting in the formation of a p–n junction between the buffer and the channel layer. Conduction across this junction can occur via dislocation-assisted paths, particularly in regions with high threading dislocation density. This behaviour is well captured by the leaky dielectric model proposed by Mike Uren [82].

GaN buffer layers grown over the selected strain relaxation layer (SRL), intentionally doped with deep-level dopants like carbon, Si, magnesium (Mg) or iron (Fe), primarily function as an insulation layer. Semi-insulating properties are achieved by compensating the residual donors with deep-level acceptors [25]. This helps to suppress off-state leakage currents and achieve higher breakdown voltage (BV) [25]. Highly insulating buffer layers can also prevent short-channel effects like drain-induced barrier lowering (DIBL), where the threshold voltage may decrease with increasing drain bias due to the reduction of the depletion region under the gate, and punch-through effects, where the drain electric field penetrates deeply into the channel, leading to off-state conduction through the buffer layer.

As mentioned before, GaN layers are often contaminated with Si impurities, unintentionally incorporated during the growth process [27] [28]. This leads to their inherent n-type conductivity. The reported level of unintentionally doped Si can vary between 10^{15} and 10^{17} cm^{-3} [28]. Silicon is an amphoteric impurity, capable of behaving as

either an acceptor or a donor. Under N-rich growth conditions, Si impurities predominantly substitute Ga atoms (Si_{Ga}) due to the similarity in their atomic radius [30] [31]. This results in shallow donor behaviour with a Fermi level located at E_C - 30meV [28] [32]. The relatively low formation energy of Si_{Ga} contributes to its high solubility in GaN [33]. At room temperature (RT), Si_{Ga} impurities are expected to have 100% ionisation; however, the activation energy may vary at different temperatures. In contrast, silicon substituting at the nitrogen site (Si_N) behaves as a shallow acceptor. However, its relatively higher formation energy makes it less likely to form [33]. In HEMT structures, carbons are incorporated into the Si-doped GaN layer to create a semi-insulating layer. This co-doping technique, where the doping concentration of carbons exceeds both the background impurity and Si concentration, will be discussed further in a later chapter.

Although Mg in GaN has not been extensively studied as other p-type dopants, it remains the most commonly used p-type dopant, typically grown using MOVPE [34] [35] or MOCVD [36] [29] to achieve semi-insulating properties. Owing to its lower formation energy at the Ga-site (Mg_{Ga}) compared to the N-site, Mg preferentially occupies Ga sites in GaN [36] [37], acting as a shallow acceptor [38]. In Mg:GaN layers, two mechanisms can limit the hole concentration and thereby contribute to increased resistivity:

a) **Mg passivation**: Mg atoms can be passivated by residual H atoms, forming Mg-H complexes that effectively neutralise some of the hole contribution from Mg. This phenomenon is activated by post-growth thermal annealing [38] [29], leading to the formation of Mg-H defect complexes and also the eventual removal of H from the crystal by reversing the passivation [16]. The concentration of H saturates at a Mg concentration of $2x10^{19}$ cm^{-3}, preventing further increases in hole concentration beyond this level [38]. Once this saturation point is reached, self-compensation of Mg acceptors becomes significant.

b) **Self-compensation**: When the hole concentration ceases to increase, self-compensation of Mg acceptors can occur. Unlike C:GaN samples, O and Si are not considered the primary compensating elements in the epitaxy. Nitrogen vacancies (V_N) and their complexes, such as Mg-V_N and H-decorated native defects like V_N-H, can act as donors, leading to self-compensation. This results in the weakly p-type behaviour observed in Mg:GaN layers. The Mg-H complex formed during growth pins the Fermi level at E_V + 0.25 eV [35] [37].

The long-term memory effect observed in Mg-doped GaN is attributed to electron trapping [39]. Mg atoms can act as scattering centres if they are redistributed into the channel region [27]. While various growth factors can contribute to the memory effect, Köhler et al. [40] suggested that growth at elevated temperatures can lead to increased Mg atom diffusion into the channel region. Memory effects can pose challenges for both power and RF devices. As a solution, Green et al. [36] proposed growing a Mg:GaN layer on top of a GaN wetting layer (an undoped GaN layer). They observed a polarity shift to N-faced GaN under N-rich growth conditions [36].

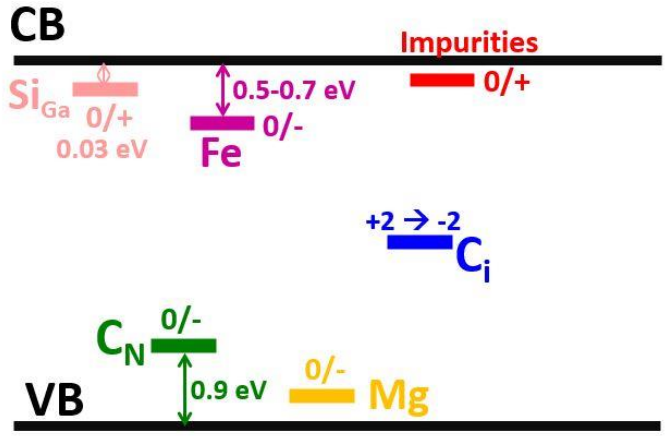

Figure 2-6 - Band profiles of the most common extrinsic dopants incorporated into the GaN buffer layer.

As illustrated in Figure 2.6, Fe behaves solely as an acceptor, with its Fermi level pinned slightly above the midgap at 0.5–0.7 eV below the conduction band, substituting the N atoms [26] [28] [41]. Heikman et al. [42] found that Fe-incorporated GaN (Fe:GaN) layers are relatively insensitive to growth conditions [25] and exhibit a memory effect similar to Mg-doped GaN [42]. This insensitivity can be advantageous for achieving reproducible high-resistivity buffer layers, but it also implies limited tunability of the compensation behaviour. Additionally, they observed that intentionally incorporated Fe atoms segregate and diffuse to the top surface of the buffer layer, redistributing into the adjacent undoped GaN layers [27] [42]. This phenomenon is attributed to the high mobility of Fe atoms. To mitigate the movement of Fe atoms into the top layers, the UID GaN layer thickness is typically grown thicker [25].

Leone et al. [25] reported that growing a GaN layer doped with smaller elements, such as carbon, can enhance the compressive strain on the top Fe:GaN layer, thereby preventing Fe atoms from penetrating these layers. An AlN layer above the Fe-doped buffer region can also restrict Fe atom diffusion into the undoped GaN layers, as

demonstrated by Köhler et al. [40]. This technique can similarly be applied to reduce Mg atom diffusion. It is important to emphasise that Fe atoms must be kept away from the 2DEG. Consequently, the thickness of the Fe: GaN layer must be carefully controlled to prevent epitaxial cracking, which could pose a significant limitation for high-voltage devices that require thicker buffers. The highest achievable breakdown voltage for epitaxies with Fe:GaN buffers has been reported as 2457 V [26].

Among several impurities, such as Si, carbon is an impurity that is inherently present in GaN, often incorporated during the growth process. It is a highly preferred choice for high-voltage GaN HEMT structures due to its enhanced insulating properties and is typically incorporated at densities exceeding $1x10^{18}$ cm^{-3}. When intentionally doped, carbon acts as a deep acceptor, compensating the n-type conductivity of GaN and resulting in highly resistive p-type C:GaN. This will be discussed in detail in Chapter 3.

Unlike other impurities, carbon does not exhibit a memory effect and is relatively easy to incorporate. However, carbon is known to cause current collapse [30]. To mitigate this effect, it is often used in conjunction with other dopants, such as Fe or Si, to create a semi-insulating co-doped buffer layer [43].

2.3.4 AlGaN Barrier

One of the primary advantages of AlGaN/GaN HEMTs is their high electron mobility (up to 2000 cm^2/Vs) channel [2], also known as the 2DEG. The 2DEG is confined to a narrow quantum well at the AlGaN/GaN heterojunction, formed due to band bending [2] [44]. In the absence of an applied voltage, the 2DEG channel exists between the ohmic contacts, resulting in "normally-on" transistor behaviour, which will be discussed throughout the chapters. The 2DEG electron density, typically in the range of 10^{13} cm^{-2}, is strongly influenced by surface charge, Al composition [45], AlGaN barrier thickness, and intrinsic polarisation charge [8]. An Al mole fraction of 0.2 to 0.4 is sufficient to induce adequate polarisation charge and create enough conduction band discontinuity at the AlGaN/ GaN heterointerface, ensuring effective 2DEG confinement [2].

In general, the correlations can be described by the following Equation 7 [1]:

$$n_s = \frac{\sigma}{q} - \frac{\varepsilon_0 \varepsilon_{AlGaN}}{t_{AlGaN} q^2} (\phi_b + E_F + \Delta E_C) \quad (7)$$

The symbols σ, ε_{AlGaN}, t_{AlGaN}, φ_b, E_F and ΔE_C represent the polarisation charge, AlGaN dielectric constant, AlGaN barrier thickness, surface potential, Fermi level and

conduction band offset between AlGaN and GaN, respectively [1]. Figure 2.7 (a) presents simulated and experimental results showing the influence of AlGaN barrier thickness on 2DEG density. The simulation predicts a minimum AlGaN barrier thickness of approximately 5 nm, below which the 2DEG ceases to exist. This critical thickness arises because the polarisation-induced charges at the AlGaN/GaN interface are insufficient to bend the bands strongly enough to form a confined quantum well for the 2DEG. Once this threshold is exceeded, the 2DEG density increases rapidly before eventually saturating at higher thickness. In contrast, the Hall mobility exhibits an opposite trend, decreasing as the AlGaN barrier thickness increases. Helkman et al.[46], concluded from their TEM analysis that an increased AlGaN barrier thickness leads to greater lattice relaxation in the barrier, resulting in a reduction in piezoelectric polarisation [46].

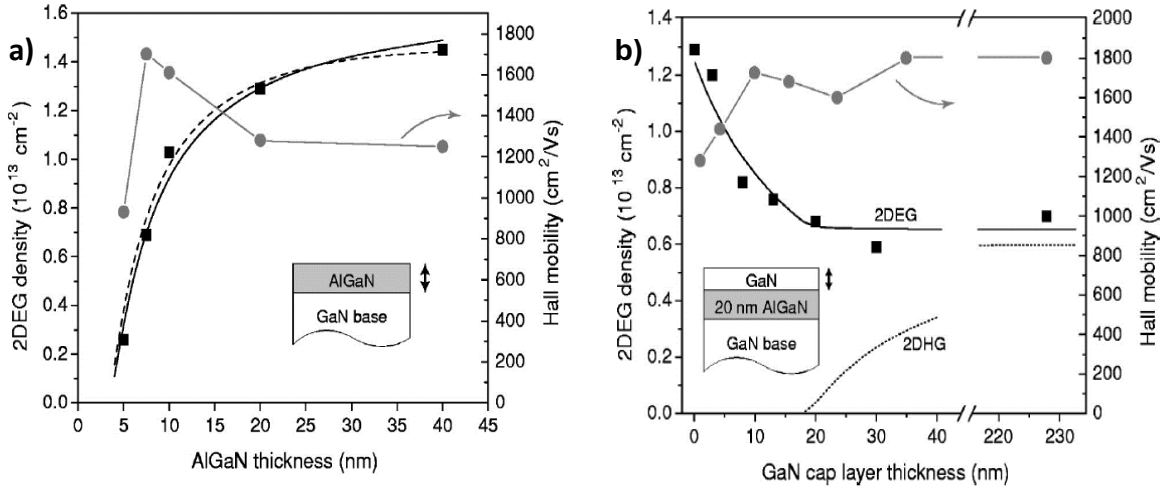

Figure 2-7 - a) 2DEG density and Hall mobility as a function of $Al_{0.32}Ga_{0.68}N$ barrier thickness b) 2DEG density and Hall mobility as a function of GaN cap thickness when the AlGaN barrier thickness was 20nm (both black lines indicate the simulation data while the markers indicating the experimental results). Figure was adapted from [46].

Chu et al. [47] report that background dopants can significantly influence 2DEG density but may also compromise quantum confinement [47], highlighting the importance of precise control over unintentional doping levels during epitaxial growth to maintain the optimal balance between 2DEG density and confinement [47].

2.3.5 GaN Cap

A thin (2-35 nm) [48] undoped GaN layer is typically deposited on top of the $Al_xGa_{1-x}N$ barrier. This GaN cap layer is expected to mitigate surface oxidation, provide a smoother surface morphology, and minimise surface-related current collapse by reducing surface donor state generation [49].

Figure 2.7 (b) illustrates the correlation between GaN cap thickness and its effects on the 2DEG concentration and Hall mobility. When the GaN cap thickness exceeds a critical value, it can deteriorate the 2DEG electron density [46] [50]. This phenomenon is likely attributed to the introduction of additional negative polarisation charges at the GaN cap/AlGaN barrier interface, coupled with associated changes in the barrier electric field [15] [51].

Regardless of the additional polarisation charge, Waltereit et al [51] observed a significant drop in the contact resistance (R_C), ultimately leading to reduced gate leakage currents and improved gain with increasing GaN cap thickness, compared to epitaxies without a capping layer. Furthermore, they concluded that the enhanced electric field strength in the AlGaN barrier exhibits a proportional relationship with the GaN cap thickness [51].

2.3.6 Ohmic Contacts

An ideal ohmic contact exhibits low R_C, which is crucial in minimising the total on-resistance (R_{ON}) in the GaN HEMTs. Typically, ohmic contacts are formed using a stack comprising multiple metals, which will be further discussed in Section 2.4. To facilitate efficient electron extraction or injection from the 2DEG into the external circuit, the contact must penetrate the barrier layer and establish a direct interface or contact with the 2DEG during the annealing process [52].

Figure 2.8 illustrates the structure of the ohmic contact stack, emphasising the diffusion of titanium (Ti) into the 2DEG during the annealing process. The interaction between the metal layers and the 2DEG, as shown in the figure, is critical for achieving low-resistance ohmic contacts, which are essential for optimal device performance.

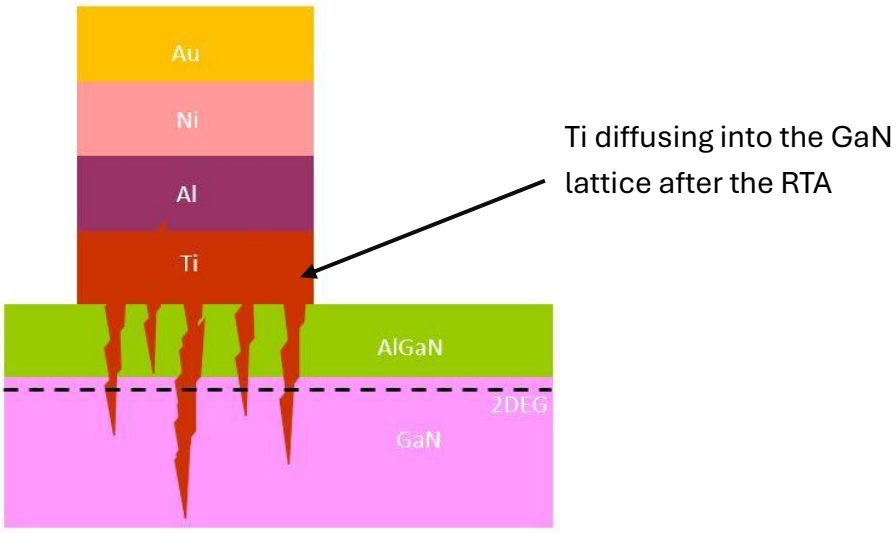

Figure 2-8 - Ohmic contact metal stack, emphasising the diffusion of Ti diffusion into the 2DEG during the rapid thermal annealing (RTA) process

Titanium (Ti): is a common material choice for contact stacks due to its ability to diffuse into the GaN lattice and form titanium nitride (TiN), as illustrated in Figure 2.8. This process facilitates tunnelling beneath the ohmic contacts, which is essential for lowering the R_C [52] [44]. This tunnelling mechanism will be discussed in greater detail in later chapters, particularly in relation to leakage paths. The Ti layer plays a crucial role in forming the contact by diffusing into the underlying GaN layer, establishing an intimate connection with the 2DEG as well as lowering the R_C. However, Ti contacts are prone to adhesion issues when oxidised, which ultimately can degrade the contact quality. To address this, these ohmic contacts are annealed at 900°C [52], which helps reduce the GaN native oxide (Ga_2O_3).

Aluminium (Al): is added to the stack to reduce the reactivity of Ti [44]. Literature suggests that Ti/Al contacts can be prone to oxygen contamination during alloying, even at low oxygen concentrations, which can lead to degraded surface morphology and potentially higher contact resistance [53]. To minimise oxidation, metals such as gold (Au) or nickel (Ni), which have lower reactivity with oxygen, are often introduced on top of Ti/Al contacts [52] [54].

Diffusion barrier metals: such as Ni, molybdenum (Mo), palladium (Pd), platinum (Pt), or Ti, are used between Al and Au to prevent the formation of Au_3Al, a highly insulating compound known as "pink plague" that can hinder ohmic contact formation [3]. In this study, Ni was used as the diffusion barrier.

Gold (Au): can enhance overall contact resistance by mitigating further oxidation during rapid thermal annealing (RTA) [53]. However, its use in mass production silicon foundries is limited due to contamination concerns and its higher cost compared to alternative materials [44].

2.3.7 Passivation Layer

A typical passivation layer consists of a thin layer of silicon nitride (SiNx) film, which encapsulates the surface donor-like states, preventing them from depleting the 2DEG. Meaning the trapped electrons on the surface are likely to deplete the 2DEG, ultimately leading to issues such as current collapse and increased dynamic $R_{ON,}$ among other reliability concerns. In-situ passivation layers are grown simultaneously with other epitaxial layers [55], offering improved surface quality, minimised surface contamination, and reduced off-state leakage [56]. Koehler et al. [56] further demonstrated that the intrinsic properties of the SiN_X layer, and consequently its impact on dynamic $R_{ON,}$ depend on its growth conditions.

Conventionally, ex-situ SiN_X layers are deposited using plasma-enhanced chemical vapour deposition (PECVD) [56] [55] or low-pressure chemical vapour deposition (LPCVD) techniques. In contrast, in-situ SiN_X is deposited via MOCVD directly after the GaN cap growth, thereby minimising interface contamination and ensuring a cleaner, more abrupt transition between the GaN cap and the passivation layer.

2.4 Device Fabrication

The device fabrication techniques discussed in this section outline the steps involved in fabricating a transfer length method (TLM) structure on AlGaN/GaN HEMTs. These structures are used to measure 2DEG channel sheet resistance, ohmic contact resistance, substrate ramp and substrate transient measurements.

2.4.1 Sample Cleaving and Cleaning

Wafer packaging typically includes a protective layer of photoresist to safeguard the epitaxial layer during storage and transportation. To prepare for device fabrication, the wafer is cleaved into smaller sample pieces, typically measuring approximately 35mm x 20mm. The protective photoresist layer is then removed through a three-step process: immersion in a warm (100 ^{0}C) resist stripper solution (EKC830) for 2 minutes, warming on a hot plate, followed by an ultrasonic bath for 5 minutes. The sample is then cleaned thoroughly with deionised (DI) water and finally rinsed with the solvents.

2.4.2 Photolithography

The mask pattern is transferred onto the samples using a photolithography process, where this pattern serves as a guide for subsequent fabrication steps, such as mesa isolation, ohmic contact deposition and bond pad deposition.

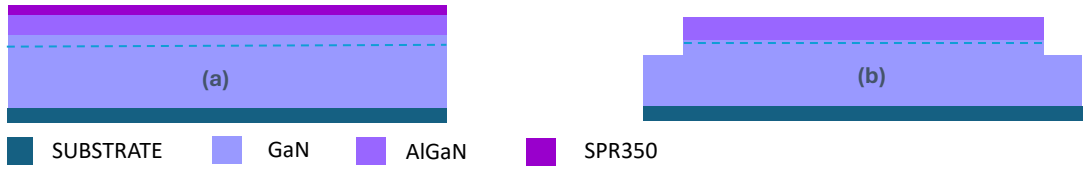

Figure 2-9 - (a) Application of photoresist (b) post ICP etch and cleaning.

To prepare the sample for photolithography, it is pre-baked for 10 seconds to remove any moisture and then allowed to cool. The photoresist (SPR350) is spin-coated onto the sample at 4000 rpm for 30 seconds. The pattern from the chromium mask is transferred onto the sample by exposing the photoresist to UV light using a Karl Suss mask aligner. The exposed photoresist is subsequently developed with a resist developer (MF26A), leaving behind a pattern that corresponds to the exposed areas. The developed patterns are then inspected under an optical microscope.

2.4.3 Mesa Isolation

After defining the desired mesa regions using the photolithography process described in section 2.4.2, inductively coupled plasma (ICP) etching was employed to create mesa structures in the GaN samples, as shown in Figure 2.9(b). The etching process utilised a gas mixture of Cl_2/Ar/$SiCl_4$, with RF power set at 25W and ICP power at 250W. The highly energetic ionised plasma generated in the ICP chamber selectively etched the unprotected GaN regions, resulting in a mesa with a depth of approximately 600nm. This depth was chosen to ensure complete removal of the AlGaN/GaN interface in the etched regions, thereby eliminating the 2DEG channel and providing effective electrical isolation between adjacent devices. The etch depth was measured using a surface profiler tool, Dektak.

2.4.4 Metal Deposition - Ohmic Contacts

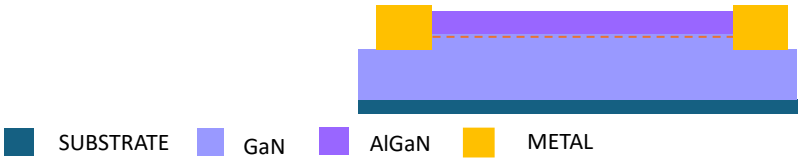

Figure 2-10 - Ohmic metal deposition.

After defining the patterns for the ohmic contacts (Figure 2.9) using the photolithography process described in section 2.4.2, a Ti/Al/Ni/Au metal stack (20 nm/120 nm/20 nm/45 nm) was deposited using thermal evaporation. To promote metal diffusion through the AlGaN barrier and achieve good ohmic contact to the 2DEG channel, post-metal deposition thermal annealing was carried out at 775°C for 60 seconds using an RTA.

Each metal in the stack serves a specific purpose, as explained in detail in the previous section 2.3.6. Au acts as a protective barrier, minimising the oxidation of the underlying metals [44], while Ni prevents Au-Al aggregation and diffusion into the channel region [44]. Al minimises the reactivity of Ti, thereby limiting the formation of Ni-Al alloy [54]. Following diffusion, Ti/Al forms TiN/AlN, which facilitates ohmic properties and behaviour.

2.5 GaN Reliability

Even though most lateral GaN HEMT devices are still in their infancy, they are already commercially available and widely adopted as replacements for conventional Si-based MOSFETs in both RF and high-power applications. Ideally, these devices should withstand high off-state electric fields, exhibit infinite off-state resistance, and achieve zero on-state resistance with no power losses. However, in reality, this is rarely the case.

Despite two decades of optimisation efforts by scientists worldwide, focusing on growth parameters, substrate templates, buffer designs, strain engineering and epitaxial structures to fully realise the potential of the lateral GaN devices, many challenges remain unresolved. These efforts have aimed to strive for simultaneously low on-resistance, high voltage, and high current capabilities. However, key reliability concerns such as premature breakdown, virtual gate effect, contact degradation, surface trapping, interface trapping, barrier trapping and buffer trapping phenomena continue to hinder the device performance (Figure 2.10), with the latter being the central focus of this thesis. This section delves into these reliability issues, their impact on dynamic R_{ON}, the associated performance degradation, and potential avenues for improvement.

2.5.1 Current Collapse in GaN HEMT

One of the significant topics extensively discussed in the later chapters is 'defects' and current collapse, also known as dynamic R_{ON}, which limits a device's ability to achieve its optimum or rated output power. In a D-mode (normally-on) HEMT, during the off-state, the device can operate under two configurations: either the substrate is negatively biased, as will be discussed throughout this thesis, or in a three-terminal GaN HEMT, the gate is at a negative potential while the drain is at a large positive potential (not covered in this thesis). Due to the high potential difference between the terminals, 2DEG electrons may gain sufficient energy to tunnel or leak into adjacent regions such as the buffer layer, or trap-rich interfaces, where they subsequently become trapped.

Current collapse occurs primarily due to these hot carriers from the 2DEG leaking into, particularly the buffer region, which contains a high density of deep-level traps. These trapped carriers form a population of negatively charged states in the vicinity of the 2DEG, either below or above the channel. This depletion of the 2DEG in the channel reduces its conductivity.

When the device is turned back on at 0V, the 2DEG does not immediately recover to its initial state. While some devices may gradually recover over time as defect states

thermally de-trap, others may retain trapped carriers below the channel that were trapped during the off state. This residual trapping, which persists even after the device is switched back to the on-state, is known as current collapse.

The presence of trapped carriers also induces a large transverse electric field, leading to the degradation of the I-V characteristics. Observable effects include an increase in knee voltage and reduced drain currents [59]. These are the direct electrical signatures of current collapse, which arises from the trapped charges depleting the 2DEG, as discussed previously. In other words, while current collapse describes the underlying physical mechanism of hot-carrier trapping in the buffer or surface states, the increase in knee voltage and reduction in drain current represent its measurable impact on the output characteristics. It remains relatively complex to isolate the contributions of buffer-induced current collapse versus surface trapping based solely on I-V characteristics [60], adding complexity to the understanding of this phenomenon.

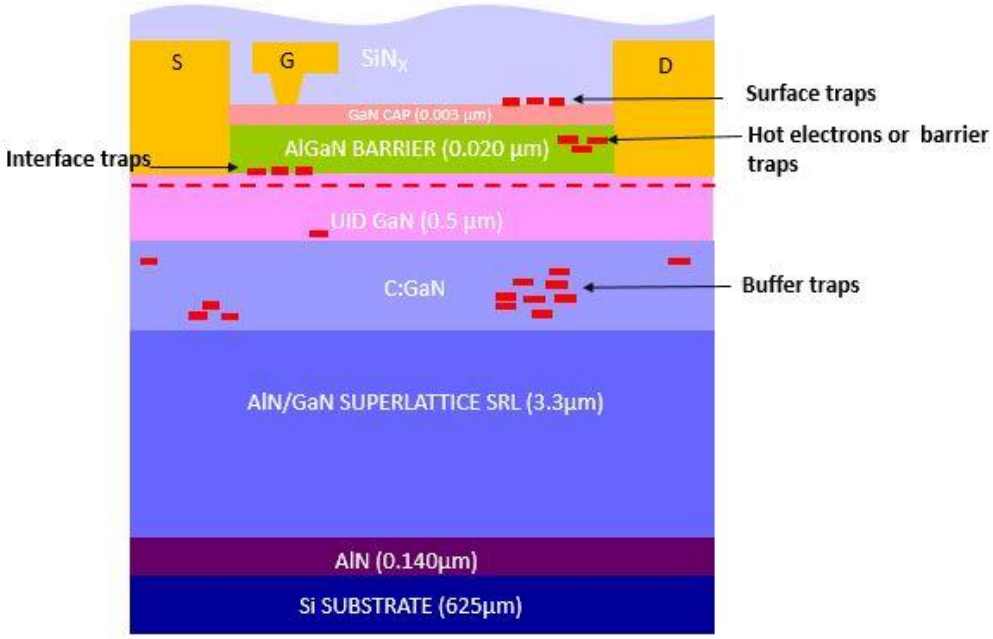

Figure 2-11 - The main trapping related mechanisms associated with the GaN HEMTs reliability.

In this section, we discuss the main degradation processes that can occur under these off-state operation.

2.5.2 Trapping in GaN HEMT

Traditionally, full width at half maximum (FWHM) values obtained from X-ray rocking curves have been used to analyse the crystal quality of wafers following growth, while transmission electron microscopy (TEM) is employed to evaluate defect propagation and distribution [61]. Both techniques will be discussed in detail in Section 2.6. GaN inherently contains a wide range of defects, including crystal defects such as threading dislocations, point defects such as vacancies and interstitials, and substitutional defects such as those associated with impurities [2][12]. This extensive list further includes surface defects, buffer-related defects, substrate-related defects, and barrier-related defects.

Electrically, the energy levels of these defect states exist within the band gaps of both GaN and its alloys, often acting as recombination centres or carrier traps [2] [62]. It is therefore crucial to identify the properties of these specific defect states, including their capture cross-section, energy level, concentration, and whether the trap state functions as a donor or acceptor.

In the case of lateral GaN HEMTs, the presence of traps can lead to various adverse effects, such as an increase in dynamic R_{ON}, threshold voltage instability, the kink effect, and current collapse [2]. To mitigate these issues, a range of characterisation techniques is typically employed to identify and analyse the quantity, nature, and degradation mechanisms of these defects, as well as their impact on the static and dynamic performance of the device.

Deep Level Transient Spectroscopy (DLTS) is a powerful technique that facilitates the detection and characterisation of deep levels located approximately 1 eV below the conduction band minimum (CBM) and above the valence band maximum (VBM) [12]. GaN also exhibits multiple photoluminescence (PL) bands associated with various impurity-related point defects, making PL analysis a complementary tool for identifying and studying defect states. Furthermore, electrical characterisation methods, such as drain current transient measurements, pulsed current-voltage characterisation, and gate frequency sweeps, are routinely employed to investigate trapping effects and their impact on device performance [2]. These techniques provide critical insights into dynamic behaviours such as current collapse and threshold voltage shifts.

The thesis will primarily focus on two types of defects: "native crystal" defects, such as threading dislocations (TDs), and "impurity-related" defects [2]. Within the latter category, two main types of traps will be discussed: shallow traps and deep traps. Shallow traps typically exist a few millielectron volts (usually ≤0.2 eV) from the corresponding band edges [2] [63]. In contrast, deep traps reside further away from the band edges, usually over 0.2 eV [2] [63]. At RT, these traps can exist in neutral or empty states.

As illustrated in Figure 2.6, traps located near the upper region of the bandgap, closer to the conduction band minimum (CBM), are termed donor-like traps. These traps remain neutral when empty and become positively charged upon losing an electron. Conversely, traps located near the lower region of the bandgap, closer to the valence band maximum (VBM), are referred to as acceptor-like traps. These traps remain neutral or become negatively charged when occupied.

2.5.3 Native Defects

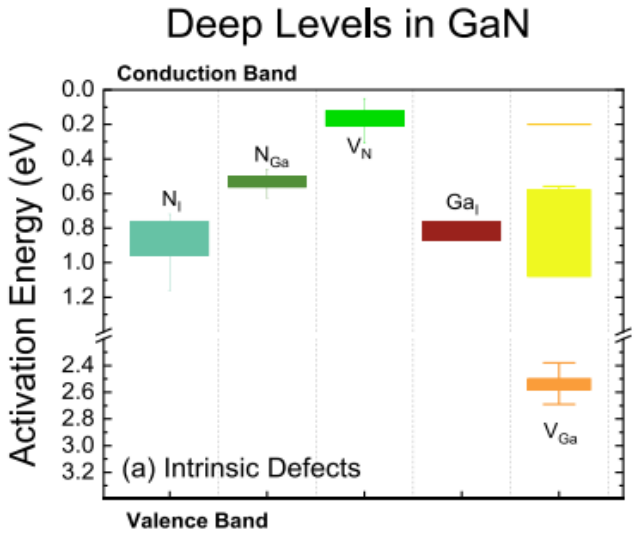

Figure 2-12 - Energy positions of the intrinsic defects commonly observed in the GaN [63]

GaN lattice typically includes various native defects involving both nitrogen and gallium vacancies, antistites and interstitials, such as:

a) **Nitrogen interstitials (N_i)** - are native defects characterised by their preferred energy positioning of trap states, typically observed between E_C−1.02 eV and E_C - 0.89 eV [2] [64]. These defects are often located within the carbon doped GaN (CGaN) buffer layer. Boturchuk et al. [65] proposed that at high temperatures, nitrogen interstitials can form defect complexes such V_{Ga}-$Vi^{-1/-2}$ which are also associated with extended defects [2].

Among all nitrogen-related native defects, interstitial nitrogen demonstrates the highest activation energy, making it particularly stable at low temperatures [2] [63]. However, at elevated temperatures, the thermal energy can surpass this activation barrier, enabling the ionisation of these defects. Once ionised, nitrogen interstitials may act as traps or recombination centres, thereby influencing the electrical and optical properties of GaN-based devices [63] [64] [65].

b) **Nitrogen Antisites (N_{Ga})** – are native defects where a nitrogen atom occupies a gallium site in the crystal lattice. According to the literature, there is no observed correlation between nitrogen antisites and extended defects [63]. These defects are typically located within the energy range $E_C - 0.65$ eV and $E_C - 0.50$ eV [63], influencing the electronic properties of GaN-based materials and devices.

c) **Nitrogen Vacancies (V_N)** - are among the most common intrinsic traps observed in GaN, where they typically behave as donors [66]. These vacancies are located at $E_C - 0.24$ eV and are often found near interfaces [2] [66]. The literature indicates that V_N defects tend to associate closely with both point and extended defects [63] [67] [68], often forming vacancy clusters [2] [63]. Additionally, trap states with similar activation energy and cross-sections, such as nitrogen complexes, nitrogen vacancies, or triply ionised nitrogen vacancies, have been observed to cluster together [2].

d) **Gallium interstitials (Ga_i)** - are not widely reported in the literature [2]. However, their associated energy levels have been identified at $E_C - 0.91$ eV [4] and $E_C - 0.8$ eV [69], particularly when forming defect complexes. These Ga_i interstitials are possibly located in the buffer layer, although their exact role and prevalence remain areas of ongoing investigation [2].

e) **Gallium Vacancies (V_{Ga})** - are observed in significant concentrations in n-type GaN, whereas their formation energy in p-type GaN is considerably higher [66] [70]. A formation energy of $E_C - 0.6$ eV has been reported [10]. Additionally, V_{Ga} vacancies often form complexes with [O] and [Si] atoms, resulting in $(V_{Ga}– Si)^{-2}$ and $(V_{Ga}–O)^{-2}$ complexes [2] [70]. These complexes exhibit charge states located $E_V + 0.92$ eV and $E_V + (1.1$ eV to 1.2 eV) , respectively.

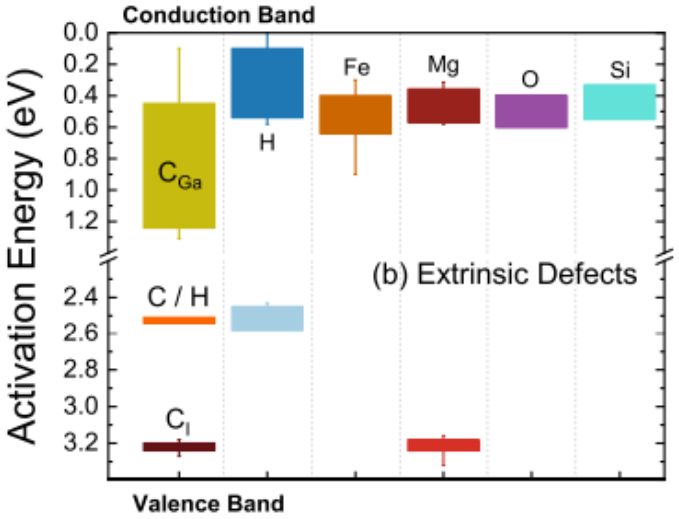

Figure 2-13 - Energy positions of the impurity related defects and their complexes, commonly observed in the GaN [63]

2.5.4 Impurity Related Defects

In addition to the aforementioned native defects, extrinsic defects arising from impurity incorporation are also significant. These impurities may be introduced intentionally as dopants or unintentionally as contaminants during the growth process. Commonly observed dopants include Si and Mg, which coexist alongside residual impurities such as O and H atoms. Additionally, elements such as carbon and Fe are often incorporated to compensate for the n-type conductivity of GaN, as discussed in Section 2.3.3.

The table below summarises impurity-related defects, highlighting their energy levels relative to the conduction and valence band edges, and their specific charge states in GaN [63].

Type of Impurity	Physical Origin	Reported Activation Energy (E_a) eV
Si	Si-related	E_C - 0.11eV
Mg	Shallow acceptor (Mg - H) complexes) Mg - V_{Ga}	E_V + (0.16 – 0.24) E_v + 0.08 E_C - 0.44
H	H-V_{Ga} complexes C-H complexes	E_C - (2.62–2.47) E_C – (0.578 and 0.49)
O	O–V_{Ga} complexes O_N	E_C – 1.118, 0.642, and 0.599 E_C – 0.44 and 0.01
C	$(C_N)^0$ $(C_N)^{-1}$ C_{Ga} C- or H complexes	E_C – (3.31–3.22) E_V+ (0.8-0.9) E_C – (0.11-0.4) E_C – (0.578 and 0.49)
Fe	Fe^{2+} or Fe^{3+} related Fe-related	E_C – 0.34 E_V + 3

Table 2.2 - Energy positions of the extrinsic deep levels associated with gallium nitride [2] [63].

2.5.5 Barrier Traps and Hot Electrons

As illustrated in Figure 2.11, deep-level traps can exist within the AlGaN barrier under the gate region, at the surface, or the AlGaN/GaN interface [71]. During off-state operation, electrons tunnel from the gate into the AlGaN barrier, where they get trapped. When the device transitions to the on-state, these trapped electrons are gradually released back into the 2DEG, restoring conduction. Additionally, hot electrons from the 2DEG, if sufficiently energised, may also become trapped in these states [2] [72].

The AlGaN barrier traps are critical in influencing reverse gate currents through mechanisms such as trap-assisted tunnelling [73], one-dimensional variable-range hopping conduction [74], or direct tunnelling via deep traps distributed across the AlGaN layer [73]. These phenomena are predominantly governed by the electric field, which impacts both trapping and emission processes. Trap-assisted tunnelling describes an

electron conduction mechanism facilitated by deep traps under strong electric fields, affecting both electron capture and release dynamics [2] [71].

The outcomes of these trapping mechanisms include [2],

1. A positive shift in the threshold voltage (V_{TH}) due to altered charge distribution under the gate.

2. An increase in resistance in the gate-drain region caused by localised charge trapping within the barrier [2].

2.5.6 Surface Trapping

Surface states play a crucial role in the dynamic performance degradation of GaN-based devices, particularly by interacting with free carriers and reducing the 2DEG density in the gate-drain region [2] [75] [76]. These traps can act as either electron or hole traps, with their state determined by their energy levels relative to the conduction or valence band. This positioning dictates whether the traps behave as donor-like or acceptor-like states.

As shown in Figure 2.13, a schematic representation of surface traps is depicted across the entire source-drain region. Electrons flowing from the gate contact traverse the barrier via hopping, becoming captured by surface traps in the gate-drain region, where a high electric field at the gate edge of the drain side plays a significant role [2]. This process is highly non-linear, likely occurring through the Poole-Frenkel effect, where the electric field reduces the energy barrier, facilitating electron movement between the traps.

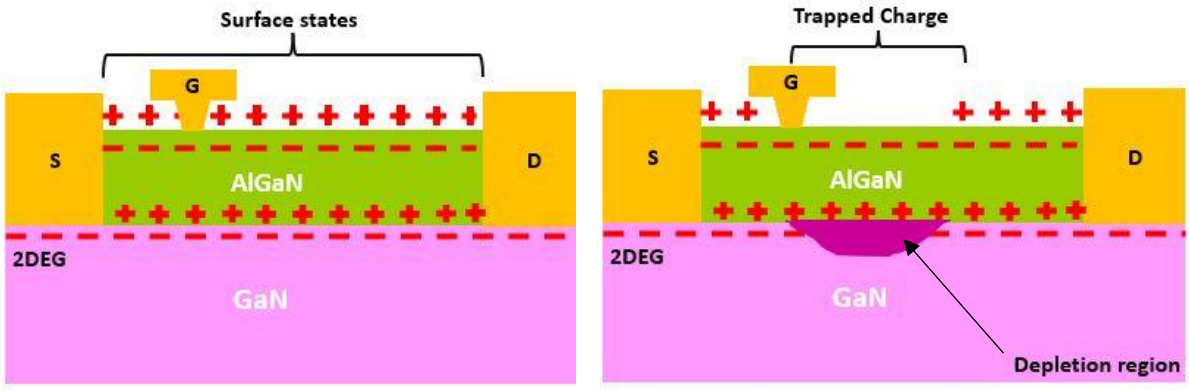

Figure 2-14 - Schematic representation of surface states and the impact of an electric field, leading to the formation of a depletion region and the virtual gate effect. Surface states, depicted in red "+" symbols on the top of the AlGaN barrier, represent unoccupied trap states capable of capturing electrons. Once the electrons are trapped, these states become neutral.

Trapped charge near the gate creates a localised depletion region, represented as the "purple region" in the 2DEG beneath the gate, which effectively acts as a "virtual gate." This phenomenon reduces the carrier density in the 2DEG, leading to a decrease in current flow and altering the electric field distribution at the surface.

Upon removal of the electric field, the trapped charge gradually discharges, releasing the electrons back to the 2DEG. Similarly, the built-in field induced by the trapped charge also dissipates over time. However, the device's recovery to its ideal state may depend on whether the surface traps are deep-level traps. If so, the electrons may remain trapped for an extended period, resulting in a slower recovery.

The presence of "hot electrons" offers an alternative mechanism for charging the surface traps. When these electrons gain sufficient energy, they can overcome the barrier and charge the traps [2] [77]. Regardless of the charging method, both mechanisms contribute to surface current collapse, leading to reduced output power. Therefore, suppressing surface traps is crucial. To mitigate this, device designs are often optimised with high-quality passivation layers and field plate introduction. In most state-of-the-art devices, surface current collapse is no longer a significant issue.

2.5.7 Buffer Trapping

Unlike surface current collapse, buffer traps or buffer-related current collapse have remained an unresolved yet detrimental issue for over two decades. The buffer is central to the device's operation, and buffer trap effects are associated with various trapping mechanisms, particularly under off-state bias conditions [78]. Buffer traps are localised energy states in the buffer region beneath the 2DEG, and as previously mentioned, their corresponding trap states depend on their energy levels relative to either the conduction or valence band.

The literature describes multiple scenarios in which buffer traps become charged under off-state conditions. At moderate drain voltages, electrons can leak via source–drain leakage current [79] or gate-to-drain leakage current [80]. Additionally, at very high drain voltages, substrate leakage and hot electrons contribute to electron trapping in the buffer region, particularly beneath the gate–drain region [81].

The unique behaviour of carbon-doped GaN buffer trapping and its impact on dynamic R_{ON} are explained by Uren et al. [82] This model highlights charge injection into and out of the buffer region, as well as positive charge storage due to hole accumulation at the bottom of the GaN buffer region [82]. The origins of these so-called buffer traps include intrinsic defects and intentional dopants incorporated to make the buffer semi-insulating by suppressing the n-type conductivity of the GaN buffer layer. These traps may also be associated with defects, impurities, or dislocations [83]. However, specifics of these topics will be discussed in detail in subsequent chapters.

Traditionally, Fe and carbon have been the most widely used dopants in power GaN devices. Fe is typically utilised in RF transistors, with a dominant energy level at $E_C - 0.5$ eV to $E_C - 0.6$ eV[63], behaving as an acceptor [2]. Conversely, for MOCVD-grown GaN layers under nitrogen-rich growth conditions, carbon prefers to occupy nitrogen sites, replacing N atoms, thereby leading C_N to act as an acceptor as well. Carbon-doped buffer layers exhibit weakly p-type conductivity, where the majority carriers are holes and are highly resistive [82]. Even with heavy carbon doping in the range of $10^{19}\,cm^{-3}$, the resistivity of the layer is typically in the range of 10^{12}–$10^{14}\,\Omega cm$ [82].

This resistivity effectively isolates the highly resistive GaN buffer from the 2DEG by forming a reversed-biased p-n junction during off-state operations [82]. This configuration allows the buffer to float and act as a reservoir for time-dependent charge storage [82].

Moens et al. [84] discuss the impact of carbon-doped buffer layers, buffer leakage, and their influence on dynamic R_{ON} in commercial 650 V-rated devices. The study highlights that the dynamic R_{ON} of these devices is highly voltage-dependent, driven by the interplay between the dynamic properties of the C_N traps and the space-charge-limited currents defining the leakage paths. Their findings further point out that the ON-state recovery transient, monitored over 1000 seconds, revealed a 25% increase in dynamic R_{ON} between 100 V and 200 V. This sudden increase in R_{ON}, upon transitioning the device to ON-state from OFF-state, has been reported by [79][85]. However, this behaviour significantly improved at higher voltages, with almost no dynamic R_{ON} being observed at the device's maximum specified voltage. Similarly, the process of trapping during the off-state also occurs on a similar timescale, indicating symmetry in the dynamics of charge trapping and detrapping [83] [86].

Even though much of the behaviour of an epitaxy can be explained using this model, the significant variability observed between different epitaxies necessitates cautious interpretation. The model also emphasises the critical importance of having vertical leakage paths to suppress dynamic R_{ON}, which presents a trade-off between achieving high breakdown voltage and minimising dynamic R_{ON} [82] [84].

2.5.8 Device Breakdown

Lateral GaN HEMTs do not exhibit avalanche breakdown behaviour, as they lack a p-n junction as the blocking layer, unlike conventional semiconductors [2] [62][87]. Instead, when these HEMTs are subjected to voltages exceeding their breakdown voltage (BV), dielectric breakdown can occur. This phenomenon is irreversible and typically results in catastrophic device failure [2]. Under off-state conditions, a high electric field can develop across the epitaxial structure, making both lateral and vertical breakdown mechanisms feasible. In practice, the BV of AlGaN/GaN HEMTs on Si is determined by the dominant leakage path, which may be lateral or vertical depending on the device design and buffer thickness [88].

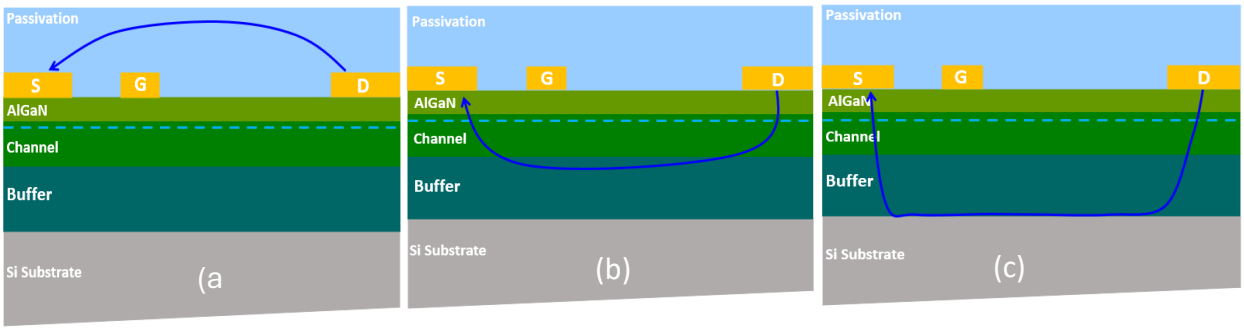

Figure 2-15 - illustrates the schematic representation of the three primary leakage mechanisms leading to device breakdown [2]

Figure 2.15 provides a simplified illustration of the leakage mechanisms associated with device breakdown. Figures 2.15 (a) and 2.15 (b) depict the leakages related to lateral device breakdown: surface leakage occurring through the passivation layer due to surface conduction within the gate-drain region, and conduction between the buffer and 2DEG resulting from electron injection, respectively [2]. Figure 2.15 (c) illustrates the vertical leakage path occurring between the substrate and the top layers. It should be noted that additional leakage contributions, such as those through the AlGaN barrier or vertical leakage between the drain and substrate, are not represented in the figure but also play a role in overall device behaviour.

a) Lateral breakdown

In a typical lateral three-terminal GaN HEMT, the peak electric field is often concentrated at the gate edge on the drain side [89]. The gap between the drain and gate is much larger than the gate-source gap to accommodate the larger electric field at the gate edge. Hence, the distance between the gate and drain is conventionally designed to

mitigate this effect. However, field plates are typically introduced in the device design to further control and redistribute the peak electric field from the gate edge to the edge of the field plate instead [89]. Since the field is spread over a larger area, the intensity of the field remains much lower, acting as a protective mechanism that enhances the device's reliability by reducing stress-related degradation [89]. Moreover, the longer the field plate, the larger the electric field reduction; however, this increases the gate-drain capacitance [89], which in turn slows down the charging and discharging dynamics during switching.

De Santi et al. [89] suggest that the degradation in GaN HEMTs is attributed to the dielectric breakdown of the SiN_x passivation layer, where the SiN_X dielectric deteriorates under prolonged stress. Their conclusions were based on the observation that the peak electric field at the gate edge on the drain side reached 6 MV/cm, which aligns with the breakdown strength of SiNx [89][90].

In essence, the lateral breakdown voltage is influenced by the device's geometry and is proportional to the distance between the gate and drain terminals [2][89]. Therefore, the design of the field plate and the passivation layer are critical factors in device performance. There exists a trade-off between improving lateral electric field management and optimising overall device performance.

b) Vertical Breakdown

The vertical breakdown (drain-to-substrate) is directly attributed to the high potential difference between the substrate and the drain, as well as the drain-to-substrate leakage [81] [91], as depicted in Figure 2.15 (c). Essentially, the breakdown mechanism is heavily dependent on the properties and quality of the epitaxial layers. Consequently, the terms vertical breakdown and vertical leakage are closely related and play a critical role in understanding this phenomenon.

Buffer structures are typically doped with impurities such as carbon, Fe, Mg, or Si to achieve semi-insulating properties by reducing the background carrier concentration [92], while simultaneously enhancing the breakdown voltage by mitigating parasitic leakage paths. For instance, carbon-doped buffer structures have garnered significant interest due to their high resistivity. However, it is undeniable that carbon doping also introduces challenges, including current collapse and trapping effects.

Lu et al. [91] observed that distinct leakage mechanisms are at play depending on the polarity of the substrate voltage. When the drain-to-substrate voltage is forward biased, hole accumulation occurs at a bias voltage of approximately 150 V. For a typical epitaxial

stack, as illustrated in Figure 2.15 (c), the high potential difference between the substrate and the drain can cause buffer impurity defects, such as C_N, to ionise, thereby leading to vertical leakage currents [90] [91]. Furthermore, in the voltage regime beyond 150 V, they suggested that electron injection from the silicon substrate into the buffer layer occurs. They concluded that forward (drain-to-substrate) vertical breakdown is primarily attributed to a combination of hole accumulation and electron injection from the substrate. In contrast, reverse (source-to-substrate) breakdown was attributed to the mechanism of impact ionisation [91].

Aligning with the hypothesis presented in [91], Zhou et al. [81] concluded that forward drain-to-substrate leakage current is predominantly driven by trap-assisted leakages, where donor/acceptor traps and intrinsic dislocations play a significant role in the conduction process. Borga et al. [90] further demonstrated that the trap levels associated with these mechanisms lie at energy depths of E_V + 0.85 eV to 0.95 eV, and that hole accumulation, combined with electron transport to the 2DEG, is likely facilitated by the Poole-Frenkel effect. This phenomenon arises due to the presence of a high electric field corresponding to elevated drain voltages [21].

Ramesh et al. [93] demonstrated an increase in lateral breakdown voltage as the C:GaN, carbon doping concentration increased from 3×10^{18} cm^{-3} to 1×10^{19} cm^{-3}, followed by a decrease as carbon concentration exceeded this range. In contrast, their experiments indicated no significant enhancement in vertical breakdown voltage with increasing carbon concentration. Through temperature-dependent experiments, they attributed the buffer leakage currents to hopping transport mechanisms, noting that the increased buffer leakage currents at concentrations beyond 1×10^{19} cm^{-3} were caused by shallow donors. These shallow donors were identified as carbon atoms occupying Ga sites, C_{Ga}. Ultimately, their findings suggest that the optimum lateral breakdown voltage is achieved at a carbon doping density of 1×10^{19} cm^{-3} [24].

Alternatively, backside field plates were proposed by Hikita et al. [94], leveraging the conductive Si substrate to achieve higher breakdown voltages, despite the trade-off with increased switching losses caused by gate-to-substrate parasitic capacitance. Building on this concept, Choi et al. [95] introduced a Fe-doped GaN buffer on an n-type semi-insulating Si substrate, achieving more consistent and enhanced breakdown voltages.

Ming et al. [96] successfully demonstrated a 125 nm thin, partially Mg-doped GaN buffer on Si, achieving substantial BVs. Similarly, Wang et al. [97] reported comparable

BVs for a 1 μm Mg-doped GaN buffer, with the highest recorded BV of 104 V for Mg-doped GaN on Si.

High breakdown voltages have been reported for AlGaN/GaN HEMTs on alternative substrates, such as 2449 V on SiC achieved using triple field plates [98], and 1412 V on sapphire [99]. With enhancements in material quality through intentional carbon doping in the GaN buffer layer, a BV of approximately 1400 V has also been achieved for devices on sapphire substrates [9].

Moving beyond doping-based structural optimisation techniques, Umeda et al. [100] proposed the insertion of two p-type GaN regions at the resistive Si substrate and AlN heterojunction. This approach reduced vertical leakage currents by forming a wider depletion region. Their method successfully increased the vertical breakdown voltage of the device from 760 V to 1340 V [100].

Tajalli et al. [101] demonstrated a vertical breakdown voltage of 1200 V by incorporating an AlGaN multilayer SL in the buffer structure. This method did not introduce additional trapping effects, unlike conventional step-graded AlGaN-based buffers. Back-gating transient measurements confirmed significantly lower dynamic R_{ON}, further validating the reduced trapping effect of the superlattice design.

Local substrate removal (LSR) beneath the gate-drain region was investigated by Herbecq et al. [102] as a technique to minimise the vertical leakage path between the substrate and the 2DEG. In this approach, the removed substrate region was replaced with a wide bandgap material, such as AlN. This method successfully demonstrated a BV of 3000 V. However, subsequent studies by other groups indicated that while effective for enhancing BV, this method adversely affects thermal dissipation, presenting a trade-off in device performance [62].

In summary, the leakages associated with overall device breakdown can be mitigated through several approaches:

- **High-Quality Passivation**: Using a high-quality dielectric material for passivation helps minimise surface leakage.
- **Optimising Gate-Drain Distance**: As pointed out before, BV is directly influenced by the distance between the gate and drain terminals, with lateral BV being proportional to this distance [62] [89]. Meneghini et al. [62] [103] observed BV

saturation for gate-drain distances exceeding 15 μm. While increasing this distance initially reduces the intensity of the lateral electric field and improves BV, the improvement becomes limited as vertical leakage pathways start to dominate.

- **Buffer Layer Engineering**: Enhancing BV requires careful design of the buffer layer. Doping the buffer with elements such as Fe or carbon [95] reduces carrier injection from the substrate and increases resistivity [91] [104]. Buffer layer thickness also plays a crucial role in mitigating leakage.

Maintaining high crystal quality is essential, as defect density in the epitaxial layers significantly impacts BV by creating leakage pathways.

2.6 Characterisation Techniques

Understanding a device behaviour under bias requires a wide range of experimental techniques and computational modelling. This section focuses on the electrical, structural, and morphological characterisation techniques, along with the equipment which were used during all the experiments. The electrical measurements described in this thesis were performed on unpackaged devices directly fabricated on the wafers. To minimise the potential unknown effects of ambient light on device performance, particularly photoexcitation of carriers, all electrical measurements were conducted in the dark.

Both two-terminal and three-terminal current-voltage (IV) measurements were used to characterise the DC performance of AlGaN/GaN HEMTs. Depending on the type of measurement, a maximum of two source-measure units (SMUs) were used.

2.6.1 Instrumentations and Capabilities

A probe station equipped with a microscope, chuck, and probe needles, is an essential tool for performing electrical measurements and characterisation of micro/nano-scale devices, including GaN devices on bare die.

(a) Probe Station

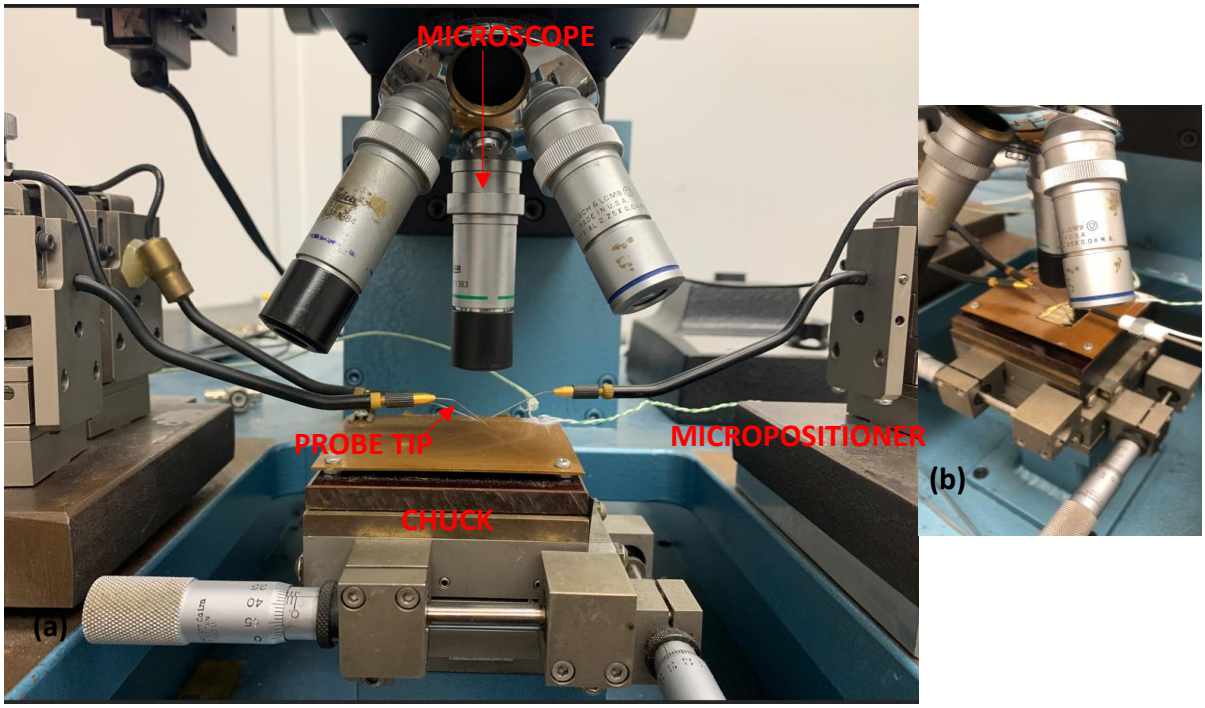

Figure 2-16 - (a) Probe station setup with the microscope, chuck, micro positioner and probe tips with (b) sample placed on the chuck

The probe station, depicted in Figure 2.16 (a), consists of several components. The sample is placed on a metal chuck, which is grounded during two-terminal measurements. However, for substrate ramp and substrate transient measurements (to be discussed later), a higher bias is applied to the chuck.

An optical microscope, positioned above the chuck (Figure 2.16 (b)), facilitates precise visual alignment of the probe needles with the small contact pads on the device under test (DUT). Typically, high magnification is often necessary to accurately probe devices with very small contact pads, ensuring that the probes are placed correctly without damaging the sample or causing short circuits.

Fine conductive probe needles are positioned over the contact pads of the DUT to make temporary electrical contact. The probes are attached to micro positioners, allowing for fine, controlled adjustments in the X, Y, and Z axes to ensure stable electrical contact with specific contact pads.

(b) Measuring Equipment

These SMUs used in the setup (Figure 2.17 (a)) are capable of sourcing voltage or current while simultaneously measuring the desired parameters. The measurement setup consists of

- A 20W high voltage (1100 V) single-channel Keithley SMU 2410
- A 40W dual channel high current (3A) Keithley SMU 2602B
- Self-designed LabVIEW programmes for each measurement

The LabVIEW programs interface with the SMUs (Figure 2.17 (b)), enabling the execution and automation of measurement routines. All SMUs are equipped with a general-purpose interface bus (GPIB) enabling the external control and seamless integration with the LabVIEW programs to commission the required measurements. All Keithley SMUs undergo annual calibration to ensure accuracy and maintain measurement sensitivity, thereby guaranteeing the reliability and reproducibility of the acquired data.

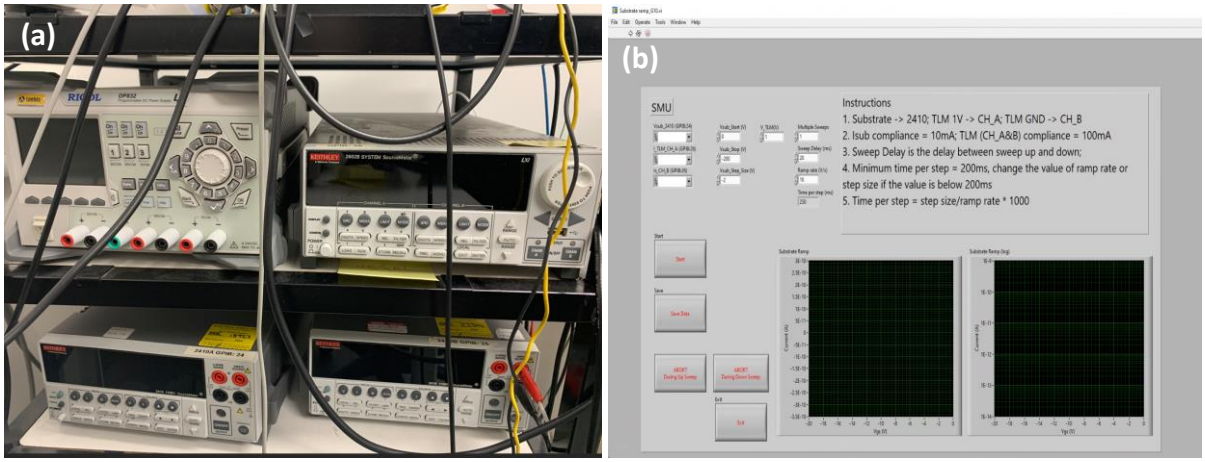

Figure 2-17 - (a) Keithley 2410 (b) LabVIEW platform for substrate ramp measurements

For the Keithley 2410:

- Voltage accuracy (1000 V range): ± (0.02% of reading + 100 mV)
- Current accuracy (20 mA range): ± (0.045% of reading + 4 μA)

  (1 μA range): ± (0.035 % of reading + 600pA offset).

The Keithley 2410 source meter, used throughout this study, specifies accuracy limits that differ significantly between the current ranges relevant to our measurements. For channel currents of TLM gap spacing 15μm, typically in the range of 8–10 mA, the applicable accuracy is ±(0.045% of reading + 4 μA), which corresponds to an error of approximately with a smaller relative error of ±8.5 μA at 10 mA (0.085% relative). This is basically negligible compared to the signal.

In contrast, for substrate leakage measurements, the Keithley 2410 was operated on the 1 μA current range, for which the manufacturer specifies an accuracy of ±(0.035% of reading + 600 pA). At nanoampere-level currents, this specification is dominated by the fixed 600 pA offset. For instance, a measured leakage of 1.0 nA carries an uncertainty of approximately ±0.6 nA (≈60% relative), while much smaller currents (for instance, ≲0.3 nA) remain below the offset limit and should be interpreted with caution. These considerations mean that, while the absolute substrate leakage values reported here are limited by instrument uncertainty at the smallest currents. However, the data remains useful for identifying relative trends such as the leakage reductions with the decreasing CGaN thickness. The noise is not expected to introduce a systematic bias across different wafers, meaning that comparative analysis is still valid.

These limitations, together with a more detailed consideration of noise and error propagation in substrate ramp measurements, are discussed further in the latter chapters .

2.6.2 DC Measurements (contact resistance, sheet resistance)

Transmission Line Method (TLM) is used to characterise the contact resistance (R_C) and sheet resistance (R_{sheet}) of the devices. As one of the first measurements performed after device fabrication, TLM provides immediate feedback on the quality of the ohmic contacts and the GaN layer. This early characterisation helps to identify any issues with ohmic contacts before further processing.

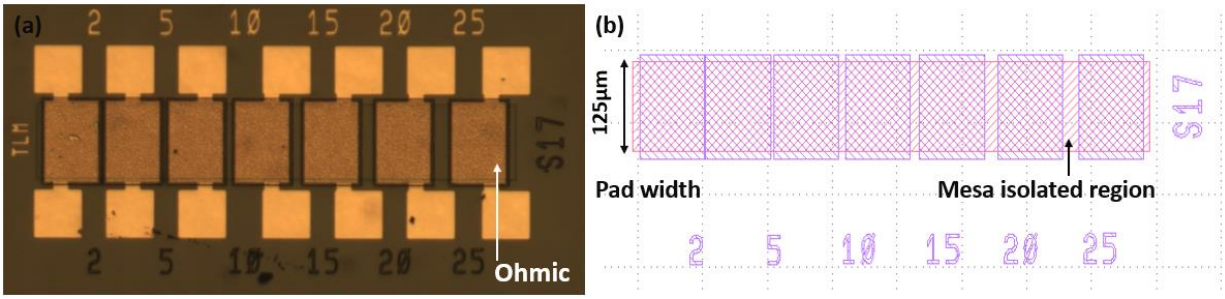

Figure 2-18 - (a) Top view of the TLM structures fabricated and (b) the mask used. The structure consists of a series of ohmic contacts with varying gap spacing, all within the same electrically isolated mesa region.

As shown in Figure 2.18, the TLM structure consists of a series of ohmic contacts placed adjacent to each other, with varying gap spacing between them. The width of the ohmic contact pads for the TLM structure is 125 µm (Figure 2.18 (b)), and the gap spacing varies from 2 µm to 25 µm. These contacts are connected through the 2DEG.

The resistance between two adjacent ohmic contact pads was obtained by sweeping a voltage from -2 V to +2 V across the pads and measuring the current (Figure 2.19 (a)) using SMU 2410, while grounding the other ohmic pad. The measured total resistance (R_{TOTAL}) between any two contacts is the sum of the R_C and R_{sheet}.

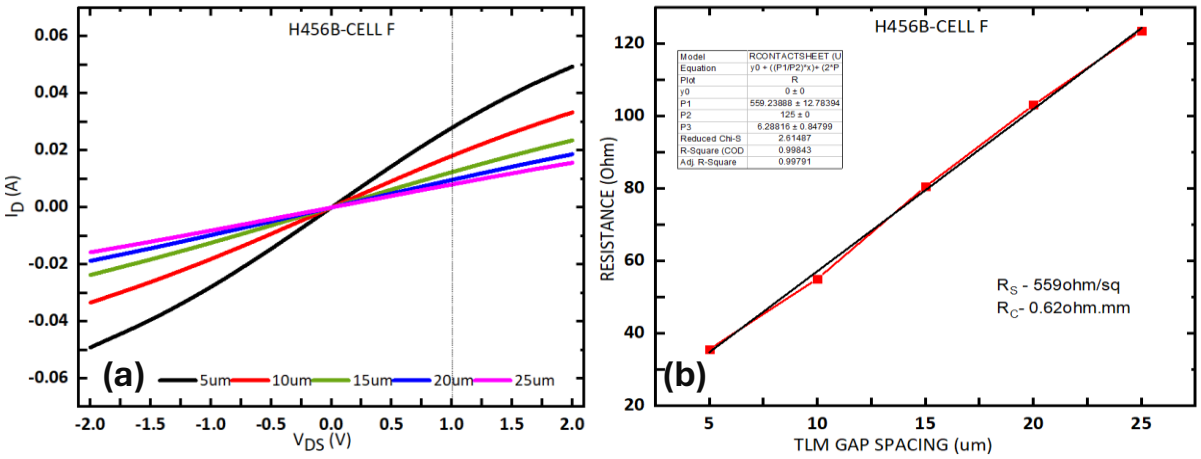

Figure 2-19 - (a) Measured channel currents (I_D) for varying TLM gap spacings. Resistance of each gap spacing was extracted at 1 V (b) Typical plot of resistance vs gap spacing with the linear straight line fit.

By plotting the resistance between ohmic contact pairs against the gap spacing (as illustrated in Figure 2.19 (b)), and using Equation 8, R_C and R_{sheet} can be determined. The R_{TOTAL} is given by:

$$R_{TOTAL} = 2R_C + R_{Sheet} * \frac{L}{W} \quad (8)$$

Where R_{Sheet}, R_C, L and W represent sheet resistance, contact resistance, the corresponding gap spacing between the ohmic pads and the width of the ohmic pads, respectively. The R_{sheet} (units in Ω/sq) typically represents the resistance of 2DEG between and beneath the ohmic pads. Similarly, R_C (units in Ω.mm) corresponds to the resistance of the metal stacks and can be extracted from ½ y-axis intercept of the TLM plot shown in Figure 2.19 (b). This value is often multiplied by W to provide the resistance per unit width. Typical values of R_S ~700 Ω/sq and R_C 1Ω.mm were extracted from the GaN-on-Si wafers in this study.

A higher R_C can adversely affect device performance as it would increase R_{ON}, thereby reducing the output I_D. This phenomenon leads to an elevated knee voltage of the device, which further diminishes the output power and significantly limits the RF performance.

2.6.3 Capacitance Voltage (C-V)

CV measurements are a valuable technique for determining the capacitance (C) of a device, which can be used to simply extract information about the 2DEG density, doping profiles, and barrier height. In this work, CV measurements were performed to evaluate the 2DEG charge concentration using a large gate area field effect transistor structure (FATFETs) to ensure a good signal-to-noise ratio and measurable capacitance values.

CV measurements were carried out using an Agilent 4284A LCR meter by sweeping a small signal voltage between -4V and 0V at a fixed frequency of 1 MHz. By varying the DC bias, both the depletion width and the capacitance can be obtained as a function of the voltage. The associated LabVIEW software, designed explicitly for CV measurements, was used to collect data on capacitance, phase angle, and impedance. To obtain a valid CV profile, the phase angle must be close to 90 degrees, indicating negligible leakage current through the device.

Capacitance was plotted against voltage (V) (Figure 2.20), and the charge (Q) was determined by integrating the area under the curve. Equation 9 relates the capacitance, voltage, and total charge.

$$Q = CV = \text{Area under the curve} \tag{9}$$

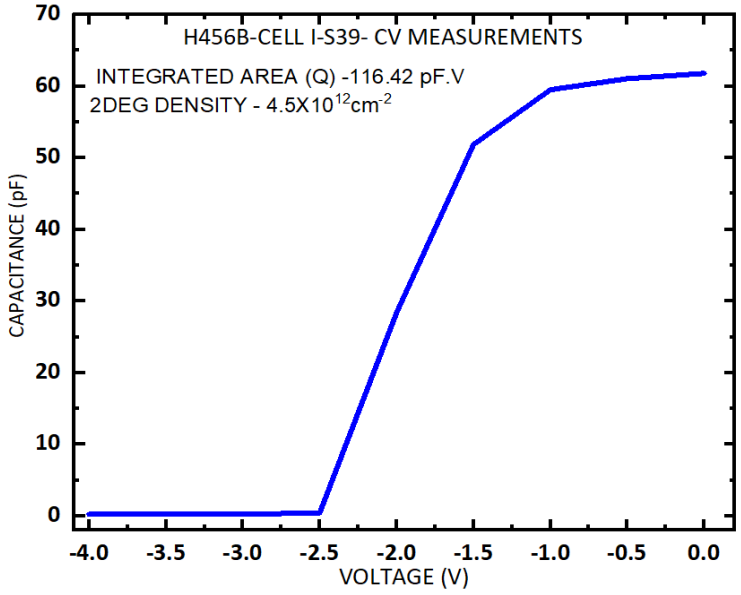

Figure 2-20 - Capacitance as a function of the voltage of the reverse biased FATFET

2DEG density (η_{2DEG}) can be calculated using the Equation:

$$\eta_{2DEG} = \frac{CV}{qA} \tag{10}$$

where q, A represents the electron charge and the area under the gate of the FATFET respectively. For simplicity, Q was extracted at -1 V.

2.6.4 Substrate Ramp Measurement

As observed by Moen et al. [84] and others, a sudden increase in the measured on-state resistance following the stress in the off-state is attributed to charge accumulation in the C:GaN buffer region [78] [82]. While the ability to distinguish surface traps from buffer traps remains a topic of ongoing debate, buffer charging can be unequivocally identified through substrate ramp measurements. This technique, also referred to as the backgating or back biasing, involves modulating the buffer via the substrate while the surface remains under low field conditions. It is primarily used to evaluate the effect of the GaN buffer trapping on the channel conductivity, which ultimately contributes to the dynamic R_{ON}. Consequently, the results are relatively insensitive to the surface charge and predominantly reflect the impact of the buffer charging on channel conductivity, which ultimately manifests as an increase in the dynamic R_{ON}.

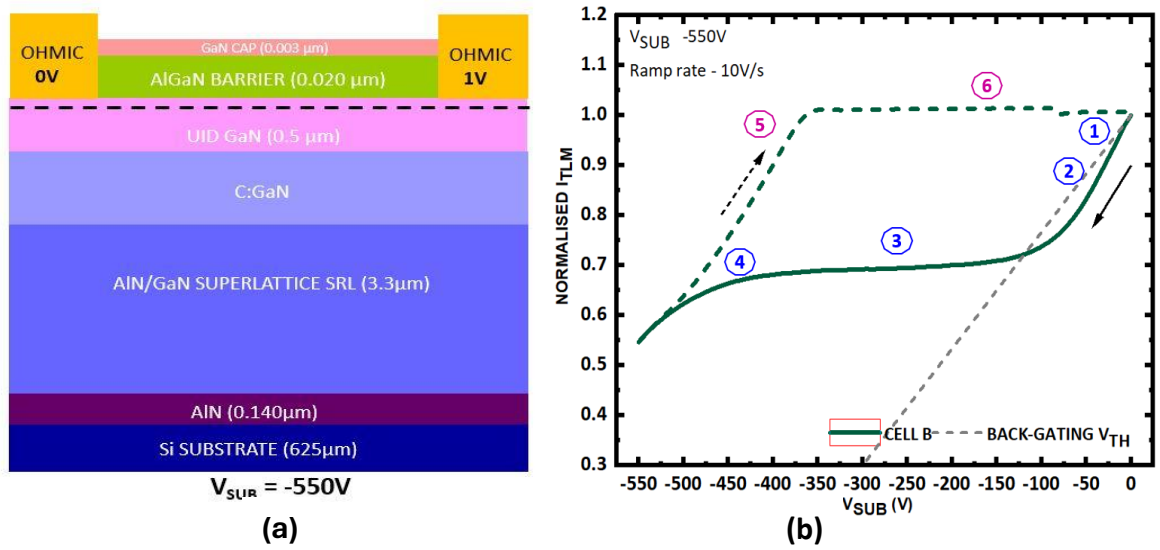

Figure 2-21 - (a) Schematic of the AlGaN/GaN epitaxy under study as well as the measurement configuration. A small sensing voltage of 1V was applied between the Ohmic contacts to sense the change changes in the 2DEG while the V_{SUB} is swept from 0V to a chosen voltage at a constant sweep rate. (b) bidirectional substrate ramp sweep.

As illustrated in Figure 2.21 (a), substrate ramp measurements involve monitoring the channel conductivity by applying a small sensing bias of 1 V between the two ohmic contacts while ramping the substrate bias (V_{SUB}) from 0 V to -550 V (forward sweep) and then sweeping it back to 0 V (return sweep). This technique leverages the conductive properties of the Si substrate, which acts as a back gate [82] [106]. During these

experiments, a typical voltage sweep rate of 10 V/s is used. Applying a negative V_{SUB} or back-gating replicates the OFF-state device conditions by pinching off the 2DEG channel [107]. This specific polarity of V_{SUB} ensures that the device operates under OFF-state conditions [108].

A typical bidirectional substrate ramp sweep is depicted in Figure 2.21 (b). The solid line represents the forward sweep, while the short-dashed line represents the return sweep. Channel currents are normalised to the currents at substrate bias of 0V. Assuming the R_C is within reasonable margins (0.75 Ω.mm in our experiments), this value supports adequate device performance for the intended application; the magnitude of the currents depends on the 2DEG density.

Under ideal circumstances, where the epitaxial layers act as an ideal dielectric and there is no trapping or charge storage in the buffer, the reduction in I_D in response to an applied negative V_{SUB} exhibits a linear relationship. This behaviour can be explained by simple capacitive coupling between the substrate and the 2DEG [5]. Specifically, the 2DEG density should decrease at a rate proportional to the capacitance and the V_{SUB} per unit area (following the equation $\Delta Q=CV$, where Q is the charge density).

Typical substrate ramp curves are compared against a reference line, often depicted in this thesis as a grey short-dashed line, which represents the "capacitive coupling line." This line is sometimes referred to as the backgating threshold voltage (V_{TH}). By definition, V_{TH} is the voltage at which the predicted channel current completely diminishes if the substrate is used as a back gate to deplete the 2DEG fully. In our case, V_{TH} is calculated to be approximately −428.75 V as shown in Figure 2.21(b). This value will be consistent with the wafers discussed in Chapters 3, 5 and 6. This value represents the point where the applied substrate bias is sufficient to deplete the 2DEG entirely under ideal capacitive coupling conditions. It serves as a benchmark for distinguishing the effects of buffer trapping from ideal capacitive coupling.

To calculate the V_{TH}, it was assumed that the epitaxial layers (UID GaN, C:GaN, SRL and nucleation layers) behave like an ideal capacitor with uniform dielectric properties. The dielectric constant of the epitaxial layers is taken as $\varepsilon_r = 9$ [109], and the distance between the plates d = 4.8 µm (total thickness of the epitaxial layers). The conductive Si substrate serves as one of the capacitor plates while the 2DEG acts as the other. ε_o is the permittivity of the vacuum (8.85×10^{-12} Fm^{-1}). In that case, the total capacitance (C_{TOT}) of this epitaxy can be calculated as:

$$C_{TOT} = \frac{\varepsilon_r . \varepsilon_o}{d} \quad (11)$$

V_{TH} can be determined using the total capacitance of the epitaxial layers and the charge density in the 2DEG. It is calculated as:

$$V_{TH} = \frac{-q * \eta_s}{C_{TOT}} \quad (12)$$

Where q, η_s, and C_{TOT} represent the elementary charge (q = 1.6 x 10^{-19}C), 2DEG carrier density (η_s was previously calculated using Equation 7), and the total capacitance of the epitaxial structures, respectively.

Any deviation from the theoretical back-gating V_{TH} line indicates the presence of charge storage or trapping within the buffer layers [110]. This technique provides valuable quantitative insight into the charge storage/trapping and electrical properties of the buffer structures.

As mentioned in section 2.5.6, once the C:GaN is intentionally doped with a higher carbon doping concentration, it makes the buffer layer weakly p-type [82]. Consequently, an equivalent circuit presentation of the entire epitaxial layers, based on the vertical structure of the device, has been used to understand the charge storage in the device structures [82] [110] [111] [112]. The epitaxial layers have been considered as a "leaky dielectric stack" [82], where charge is accumulated at each heterojunction where distinct layers connect. With the application of an electric field, positive charge accumulates at the top of the stack of layers and negative charge at the opposite side [82].

The normalised channel conductivity of gap spacing, as indicated in Figure 2.21 (b), reflects the changes in the 2DEG in response to the substrate voltage. The corresponding regions represent different behaviours, as follows :

Region 1 up to |-27V|: The normalised conductivity follows the back-gating V_{TH}, and the structure exhibits a behaviour of an insulator. Under low substrate bias, the capacitor is charging, resulting in a high displacement current, which is much higher than any leakages across the layers. Hence, no significant conduction is observed.

Region 2: Beyond |-27V| to |-125V|, a minor deviation from the capacitive coupling line can be observed, attributed to a decrease in the channel conductivity. This behaviour arises due to charge redistribution within the C:GaN region [82], caused by the ionisations of the C_N acceptors that accumulate on the top of the C:GaN layer [106], as the V_{SUB}

further increases. The negatively charged ionised C_N resides close to the 2DEG, while the positive charge will be swept to the bottom of the layer [82] [113].

Region 3: From |-125| to |-400V|, the channel conductivity begins to saturate, indicating that the 2DEG no longer changes with the increasing V_{SUB}. Negative charge in the valence band of the CGaN layer, starts to flow into the 2DEG via trap-assisted tunnelling mechanism through the UID layer [82] [114], as it begins to conduct along the dislocations. In return, a free hole is released to the valence band, which is subsequently pushed towards the bottom of the CGaN layer by the electric field. The accumulation of this positive charge at the CGaN/AlGaN SRL interface forms a 2-dimentional hole gas (2DHG), which neutralises the ionised acceptors, thereby screening the negative substrate bias [115]. This process is known as positive charge storage [113].

Region 4: At higher negative V_{SUB}, leakage begins to occur throughout the epitaxy, exceeding the displacement current in all layers [82]. Electron injection from the substrate leads to increased vertical leakage.
Beyond V_{SUB} = -425V, any further increase in V_{SUB} will lead to a complete depletion of the 2DEG, and the channel becomes completely depleted. This voltage is also referred to as the backgating V_{TH}.

Region 5: In the return sweep from |-550V| to |-350V|, conductivity appears to follow the back-gating V_{TH}, with the return sweep currents parallel to the capacitive coupling line, indicating that the structures behave like an insulator. In fact, positive charge no longer accumulates, but instead remains at the C:GaN/AlGaN buffer interface [82].

Region 6: From |-350V| to 0V return sweep, normalised conductivity is higher than the initial density observed during the forward sweep, indicating a slightly higher 2DEG density. However, the stored positive charge will reverse the electric field, causing the N-P junction between the UID and the weakly p-type C:GaN region to become forward biased [82]. The saturation observed in the return sweep occurs as the negative charge begins to move back into the C:GaN region from the 2DEG. At the completion of the return sweep, net positive charge storage should ideally be suppressed.

However, some of the positive charge remains trapped within the structure, particularly at the C:GaN/AlGaN interface, preventing complete neutralisation. This residual charge leads to a higher 2DEG density and thus higher currents upon completion

of the return sweep. Therefore, at the completion of the return sweep, net positive charge storage is not entirely suppressed, and the remaining charge influences the conductivity.

In the substrate ramp measurements presented here, twelve cells were measured for each wafer, with no repeat measurements performed. For consistency, the median value from these twelve measurements was taken as representative of each sample. This approach has been applied uniformly across all chapters, unless explicitly stated otherwise. Furthermore, across each wafer set, only subtle variation was observed throughout the samples, suggesting that the possibility of variability within the wafer and between the fabricated TLM structures across the sample can be treated reliably. This supports the reliability of using median values and confirms that the reported trends are robust.

2.6.5 Substrate Transient Measurements

Substrate ramp measurements offer valuable insight into the charge transport mechanisms and charging-discharging behaviour within the C:GaN buffer. However, for more detailed dynamics such as response time, additional measurements, such as substrate transient measurements, are required.

These quick complementary measurements allow us to capture the time response of the CGaN buffer, allowing us to establish the buffer charge storage dynamics that are in play. Electrically, the measurement setup is similar to the substrate ramp configuration shown in Figure 2.21 (a), and the principle behind the transient measurements is identical to the conventional transient measurement technique. The sample is stressed to a particular state for a given time. Then, the channel currents are monitored as the stress is abruptly removed. The measurements conducted during the experiments consist of two phases, where:

Stress Phase: channel currents were measured by applying a sensing voltage of 1 V between the ohmic contacts while a constant off-state stress, V_{SUB} of -300 V was applied to the Si substrate for 10 seconds.

Recovery Phase: On the on-state recovery channel currents were measured for 300 seconds upon removal of the stress substrate voltage.

When the V_{SUB} of -300 V was applied to the device for 10 seconds, a positive-going current transient was observed (Figure 2.22), indicating an increase in the channel

currents. This behaviour aligns with the current saturation observed during the substrate ramp measurements, as shown in Figure 2.22(b). It is associated with the positive charge storage phenomena occurring at -300V, in the substrate ramp curve shown in Figure 2.21 (b).

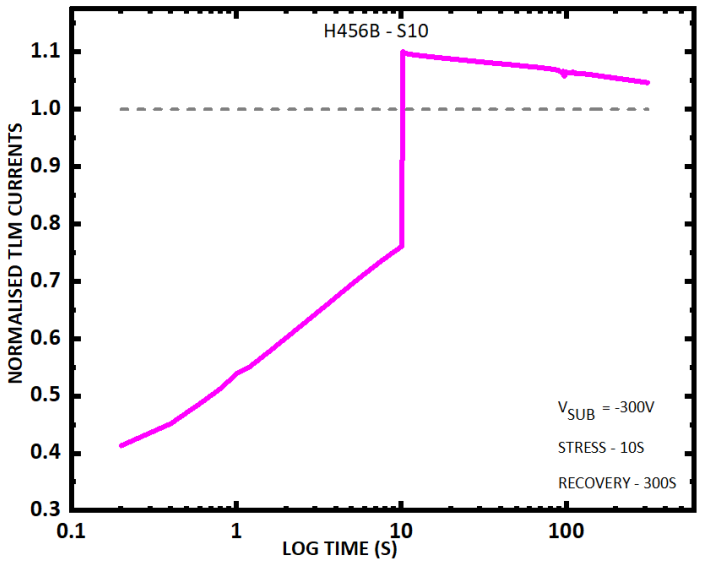

Figure 2-22 - Normalised substrate transient current for S10 structure where the gap spacing between the ohmic contacts is 10µm. The grey dashed line shows the 0V channel current for reference.

During the subsequent recovery phase, which was recorded immediately after removing the V_{SUB}, a negative-going (decreasing) transient can be observed. This is attributed to the gradual removal of the stored positive charge, where the electrons in the 2DEG begin to diffuse into the CGaN layer. However, as for the recovery phase, the transient indicates that the channel current did not fully return to its initial state, suggesting that some positive charge remains trapped in the structures. The recovery time duration during the experiment is likely insufficient to capture the charge removal dynamics.

2.6.6 High Resolution X-Ray Diffraction (HR-XRD)

High-resolution X-ray Diffraction (HR-XRD) is a characterisation technique used to investigate the crystalline quality, strain, and thickness of GaN and other compound semiconductors [61]. It is particularly valuable for evaluating the structural properties of GaN-based heteroepitaxial structures grown on foreign substrates such as sapphire, silicon, or SiC. Additionally, it enables the assessment of strain distribution and epitaxial

quality. From a device perspective, it has been shown that threading dislocations (TDs) are a pathway for leakage currents in AlGaN/GaN HEMTs grown on foreign substrates [61].

XRD primarily provides insight into the crystal structure along the growth plane [116], providing us with details to estimate the TD density roughly. For GaN, ω/2θ scans and rocking curves are commonly employed. In this thesis, rocking curves have been used to estimate dislocation densities by measuring the full width at half maximum (FWHM) of diffraction peaks, an indicator of crystalline quality. These measurements were performed using a Bruker D8 Discover system (Figure 2.23).

In addition to threading dislocation densities, several other factors can contribute to the broadening of the rocking curves. Instrumental effects, such as beam divergence, monochromator imperfections, and detector resolution, can artificially increase the measured FWHM. Sample-related factors, including surface roughness and wafer curvature (bow), also play a significant role. In heteroepitaxial GaN layers, thermal expansion mismatch between GaN and the substrate can introduce residual stress during cool-down, leading to inhomogeneous strain distributions that broaden the rocking curve. Mosaic tilt and twist further complicate interpretation, since they affect the symmetric and asymmetric reflections differently. As a result, while FWHM values are widely used as qualitative indicators of crystalline quality, care must be taken in attributing peak broadening solely to dislocation density, and comparisons are most meaningful when samples are measured under identical instrumental conditions.

The FWHM of the symmetric (0 0 0 2) reflection is primarily influenced by the screw dislocations, whereas the asymmetric (1 0 $\bar{1}$ 2) ω scan contributes to the edge and mixed TDs [83] [116] [117], and the FWHM values are typically expressed in degrees. Narrower FWHM values generally indicate higher crystalline quality, as they represent lower levels of lattice distortions and dislocations, whereas the wider FWHM corresponds to the lowest crystalline order [61].

The screw dislocation density (T_{screw}) and the edge dislocation density (T_{edge}) are calculated using the following equations [117] [61]:

$$T_{screw} = \frac{\beta_{0002}^2}{4.35 b_{screw}^2} \tag{13}$$

$$T_{edge} = \frac{\beta_{1012}^2 - \beta_{0002}^2}{4.35 b_{edge}^2} \tag{14}$$

Where β_{0002} and β_{1012} are the FWHM of the ω (0002) and $(1\ 0\ \bar{1}\ 2)$ values in radian, respectively. The Burger vector lengths (b_{screw} and b_{edge}) for screw type TDs and edge TDs are 0.5185nm and 0.3189nm [61][117]. These parameters are critical for calculating dislocation densities and understanding the nature of defects in the material.

Figure 2-23 - Bruker HRXRD – University of Sheffield

2.6.7 Transmission Electron Microscope (TEM)

The transmission electron microscope (TEM) is a crucial tool for analysing dislocations in semiconductors. However, sample preparation for TEM is extremely challenging and time-consuming, making the analysis both extremely complex and costly [118]. While TEM experiments were conducted at Integrity Scientific Ltd, Warwick, this section provides a brief overview of the steps involved in performing such experiments.

The surface of the die or device must be free of contaminants, coatings, or photoresist to avoid the need to drill through a passivation layer [118]. Typically, a Xe+ plasma-focused ion beam (PFIB) is used to mill a section of the bare die. This approach prevents the introduction of artefacts or unwanted conduction paths that may result from Ga+ ion milling [64]. The ion beam drills through the GaN cap layer, after which metal (typically tungsten) is deposited using electron-beam-induced deposition (EBID) or ion-beam-induced deposition (IBID) [64]. This metal deposition not only protects the area of interest from damage but also provides structural support.

The plasma FIB is used to cut the lamella, which is then lifted out with a micromanipulator. In the context of TEM, a lamella refers to a very thin, precisely

prepared slice or layer of material, now supported by the deposited metal. Finally, the sample is thinned and polished with a low-energy ion beam (12 keV, 100 pA) to clean the surface [118].

Once prepared, the lamella was analysed using both bright-field (BF) and dark-field (DF) TEM imaging modes. BF imaging provides an overall view of the crystalline lattice and allows for the visualisation of dislocation contrast as dark lines against a lighter background. In comparison, DF imaging enhances the visibility of specific defect types by selecting diffracted beams, which highlights strain fields around dislocations. By tilting the sample and applying different diffraction conditions (the so-called g.b analysis, where g is the diffraction vector and b is the Burgers vector of the dislocation), it is possible to distinguish between different types of dislocations [127]. The diffraction vector is generally selected to obtain the clearest image based on the strength of the diffraction x-rays.

To further distinguish the types of dislocations, the invisibility criterion g.b = 0 was applied. By carefully choosing two-beam conditions, it is possible to suppress or highlight particular dislocation types selectively. The (0002) reflection is parallel to the c-axis and thus suppresses edge-type dislocations while revealing screw dislocations, whose Burgers vector lies along [0001]. In contrast, the $(1\bar{2}0)$ or (0110) reflection lies in the basal plane, suppressing screw dislocations while making edge and mixed dislocations visible [128]. In this study, DF TEM images were obtained using g = (0002) and g = $(0\bar{1}0)$ for comparisons.

These imaging methods provide direct insight into TDD and the nature of extended defects within the GaN layers. However, due to the limited area sampled and the complexity of lamella preparation, TEM analysis is best considered complementary to statistical techniques such as HRXRD.

2.6.8 Atomic Force Microscopy (AFM)

The surface morphology of GaN/AlGaN samples is typically analysed using Atomic Force Microscopy (AFM), a high-resolution scanning probe technique used to investigate surface topography. AFM is beneficial for examining surface roughness, morphology, and other nanoscale features critical for GaN HEMT structures, providing high-resolution images of small surface areas (5 μm × 5 μm scans) [61]. In this study, AFM measurements were performed using an FSM 1000 Nanoview AFM, in tapping mode (also referred to as dynamic AFM, or intermittent-contact mode), which is commonly used for GaN surfaces as it minimises tip-induced damage and simultaneously reduces lateral forces, thereby providing reliable roughness values while preserving surface integrity.

In addition to roughness evaluation, AFM images can also be employed to estimate defect densities by counting the number of etch pits visible on the scanned surface. Each pit is typically associated with a threading dislocation intersecting the surface, allowing a statistical estimate of the dislocation density. The density of threading dislocations N_D, can be calculated using:

$$N_D = \frac{N}{A}$$

Where N is the total number of pits counted in the AFM scan area, and A is the scanned area (cm^2). As the samples used are in the size of 5 μm × 5 μm, the scan corresponds to the area of 25 μm^2, or 2.5×10^{-7} cm^2.

However, AFM is inherently limited to surface analysis and does not penetrate deeper regions, such as the GaN buffer layer, which is approximately 0.6 μm below the surface for the here in used samples. Given that this study focuses on the GaN buffer layer, AFM is not typically employed for in-depth analysis of this deeper region. The AFM images were analysed and quantified using Gwyddion software, which provides advanced tools for extracting average root-mean-square (RMS) surface roughness and other quantitative features using the AFM scanned data.

2.6.9 Computational Simulation

While electrical characterisation provides valuable insights into the performance and nature of the device, it has limitations in understanding the underlying mechanisms or physics responsible for the observed behaviour. To bridge this gap, the structures discussed in this thesis will be modelled using Synopsys Sentaurus TCAD. This tool enables the investigation of the physical phenomena underlying the observed results.

Sentaurus TCAD is specifically designed to model the electrical characteristics of GaN-based devices and simulate semiconductor processes. This physics-driven simulation approach incorporates fundamental device physics, advanced numerical methods, and material-specific models. At its core, TCAD primarily uses the drift-diffusion model to solve the carrier transport equations for both electrons and holes, alongside the Poisson equation and the continuity equation.

$$J_e = q(n_e \mu_e E + D_e \nabla n_e) \quad (12$$

Where Je, q, n_e, μ_e, E and D_e represent the electron current density, elementary charge, electron concentration, electric field, electron mobility, and the electron diffusion coefficient, respectively. Consequently, this equation applies to holes as well, with the corresponding parameters substituted appropriately. For holes, the parameters include p for hole density, μ_h for hole mobility and D_h for the hole diffusion coefficient.

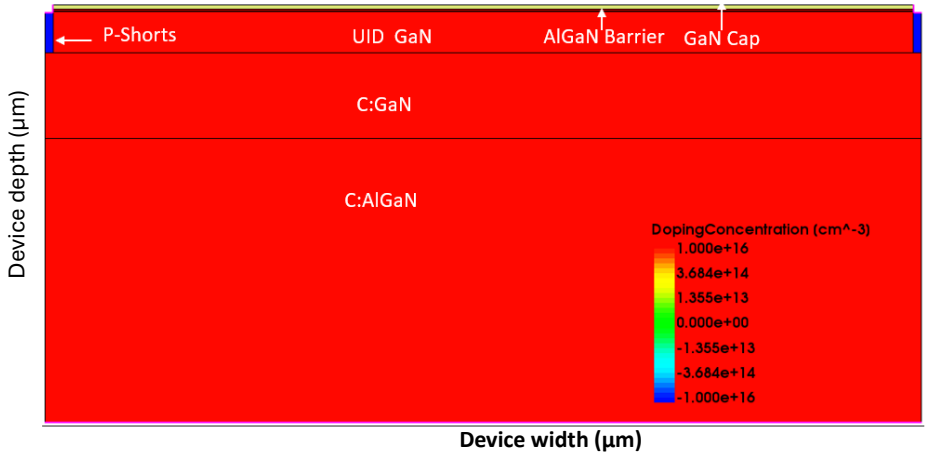

Figure 2-24 - Simulation cross section of TLM gap 10 µm. Simulated GaN on Si epitaxy consists of a GaN cap, AlGaN barrier layer, GaN channel, UID GaN layer, C:GaN buffer and C:AlGaN buffer on SI Substrate. Underneath the ohmic contacts, 2 x p-shorts are included.

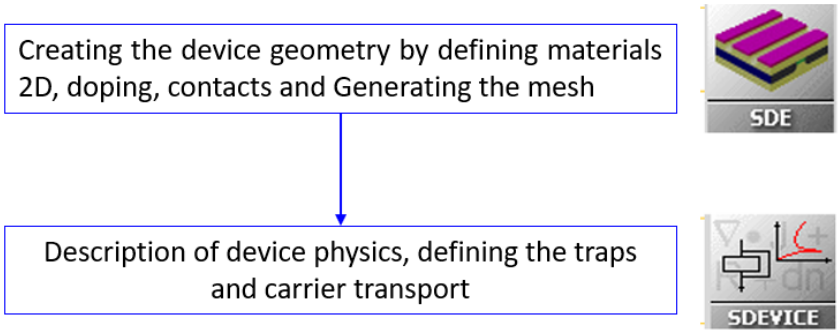

Figure 2-25 - TCAD Simulation Flow

The initial step involves simulating the 2D device geometry of the AlGaN/GaN HEMT using Sentaurus Structure Editor (SDE). This tool facilitates the definition of device materials, geometry, doping profiles, and electrical contacts. A representative cross-section of the device structure utilised in this study is depicted in Figure 2.24. For accurate finite element computations, an appropriate meshing strategy must be defined for the device layers. In regions with heterojunctions, where material properties change abruptly, or under conditions of high electric fields, a dense mesh is essential to ensure numerical accuracy while preventing convergence issues, which could halt the simulation. Although coarser meshes may still yield results, these are prone to significant errors. Therefore, the simulations in this work employ a finer mesh for enhanced accuracy. However, it is essential to note that finer meshes increase computational complexity, leading to longer simulation runtimes.

The Sentaurus Device (SDEVICE) module models specific material parameters, such as hole capture cross-sections, alongside the electrical, thermal, and optical behaviours of semiconductor materials. It enables detailed simulation of device performance, including I-V characteristics, breakdown mechanisms, and carrier transport, using advanced models like drift-diffusion and hydrodynamic approaches. Furthermore, SDEVICE allows for in-depth investigation of critical physical phenomena such as charge trapping, hot carrier effects, doping profiles, and material properties. These capabilities make it an indispensable tool for understanding and optimising device behaviour.

Given the focus of this thesis, key parameters such as bandgap, electron, and hole mobility, electron-hole capture cross-sections, and the conduction and valence bands, along with their corresponding electric fields, are of critical importance for this D-mode GaN/AlGaN HEMT. These parameters are particularly significant as the device operates under substrate biasing conditions. The buffer dopants in the structure are defined as traps, characterised by their energy levels, densities, and electron-hole capture cross-

sections. Additionally, in the simulation model, predefined carrier generation and recombination mechanisms are incorporated, including the Shockley–Read–Hall (SRH) process, alongside transport models that are critical for accurate device simulation.

The model consists of a 3.3 µm AlGaN layer, which serves as the SRL, a 1 µm CGaN layer, a 0.5 µm UID GaN layer, followed by a 10 nm GaN channel, a 20 nm $Al_{0.20}Ga_{0.80}N$ barrier, and a 3 nm GaN cap. The AlGaN top barrier surface charge was set to 5×10^{12} cm^{-2} to bring the simulated 2DEG density in line with the measured value of 5×10^{12} cm^{-2}. The epitaxy contains background doping levels of 1×10^{16} cm^{-3}, and these impurities have been modelled as shallow donor traps (N_D) with an energy level of 0.65 eV [115] below the conduction band [108]. The carbon acceptors in the CGaN layer have been modelled as acceptor traps (N_A) of 1×10^{19} cm^{-3} at 0.9 eV above the valence band [82] [108].

For simplicity, complete ionisation of the dopants at room temperature is assumed, and the superlattice SRL layer is modelled as an AlGaN layer containing C_N of 2×10^{19} cm^{-3}. Both the CGaN and SRL capture acceptor and donor cross-sections are 1×10^{-15} cm^2 [27] and 1×10^{-16} cm^2 [82], respectively. All samples were simulated with $N_D/N_A = 0.6$. The choice of this compensation ratio was determined based on comparison between the experimental substrate bias results and the simulation, aiming to achieve the optimum fit. Specifically, for a carbon level of 1×10^{19} cm^{-3}, a compensation ratio of 0.6 effectively suppressed the formation of the 2DHG at the CGaN/SRL interface, and the simulation results, as illustrated in Figure 2.26, demonstrate good qualitative agreement with experimental measurements.

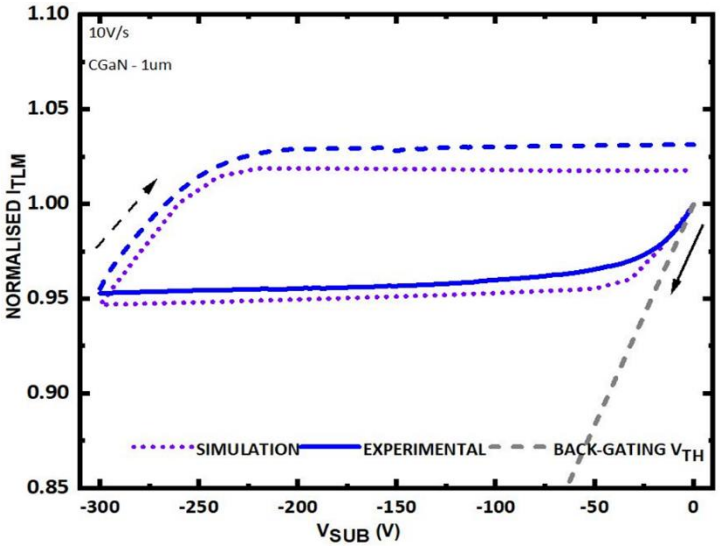

Figure 2.26 - Optimum fit between the TCAD simulated substrate ramp response with experimental results

The incorporation of p^+ shorts serve a dual purpose by modelling both the dislocations in the GaN crystal lattice beneath the contacts and the diffusion of ohmic metal along those dislocations. Additionally, the presence of p^+ shorts facilitate the modelling of the pathway for hole current at the bottom of the CGaN layer [82] [86] [108]. The leakage path along the dislocations between the ohmic contacts has not been incorporated into the model.

2.7 References

[1] O. Ambacher, B. Foutz, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, A. J. Sierakowski, W. J. Schaff, L. F. Eastman, R. Dimitrov, A. Mitchell and M. Stutzmann, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures," Journal of applied physics, vol. 87, no. 1, p. 334–344, 2000.

[2] M. Meneghini, C. De Santi, I. Abid, M. Buffolo, M. Cioni, R. A. Khadar, L. Nela, N. Zagni, A. Chini, F. Medjdoub, G. Meneghesso, G. Verzellesi, E. Zanoni and E. Matioli, "GaN-based power devices: Physics, reliability, and perspectives," Journal of applied physics, , vol. 130, no. 18, p. 181101, 2021.

[3] H. Morkoç, Nitride Semiconductor Devices, Fundamentals and Applications, Weinheim: WILEY-VCH Verlag GmbH & Co.KGaA, 2013.

[4] O. Ambacher, B. Foutz, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, A. J. Sierakowski, W. J. Schaff, L. F. Eastman, R. Dimitrov, A. Mitchell and M. Stutzmann, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures," Journal of applied physics, vol. 87, no. 1, p. 334–344, 2000.

[5] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck and U. K. Mishra, "Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors," Applied physics letters, vol. 77, no. 2, p. 250–252 , 2000.

[6] B. Liu, M. Lachab, A. Jia, A. Yoshikawaa and K. Takahashi, "MOCVD growth of device-quality GaN on sapphire using a three-step approach," Journal of crystal growth, vol. 234 , no. 4, p. 637–645, 2002.

[7] B. Godejohann, E. Ture, S. Müller, M. Prescher, L. Kirste, R. Aidam, V. Polyakov, P. Brückner, S. Breuer, K. Köhler, R. Quay and O. Ambacher, "AlN/GaN HEMTs grown by MBE and MOCVD: Impact of Al distribution," Physica Status Solidi (B) Basic Research, vol. 254, no. 8, 2017.

[8] U. K. Mishra, L. Shen, T. E. Kazior and Y.-F. Wu, "GaN-Based RF Power DevicesAmplifiers," Proceedings of the IEEE, vol. 96, no. 2, p. 287–305, 2008.

[9] B. Gill, Low Dimentional Nitrdie Semicondcutors, New York: Oxford University Press Inc., 2002.

[10] U. Honda, Y. Yamada, Y. Tokuda and K. Shiojima, "Traps in MOCVD n-GaN Studied by Deep Level Transient Spectroscopy and Minority Carrier Transient Spectroscopy," Japanese Journal of Applied Physics, vol. 51, no. 4, pp. 04DF04-04DF04-4, , 2012.

[11] A. Hierro, M. Hansen, L. Zhao, J. Speck, U. Mishra, S. DenBaars and S. Ringel, “Carrier Trapping and Recombination at Point Defects and Dislocations in MOCVD n-GaN,” Physica Status Solidi (B) Basic Research, vol. 228, no. 3, p. 937–946, 2001.

[12] T. Narita and T. Kachi, Characterization of defects and deep levels for GaN power devices, Melville, New York: AIP Publishing Books AIP Publishing LLC, and American Institute of Physics,, 2020..

[13] M. Henini, “Molecular beam epitaxy from research to mass-production — Part 1,” Elsevier B.V, vol. 9, no. 3, p. 32–34, 1996.

[14] J. Hu, H. Wei, S. Yang, C. Li, H. Li, X. Liu, L. Wang and Z. Wang, “Hydride vapor phase epitaxy for gallium nitride substrate,” Journal of semiconductors, vol. 40, no. 10, p. 101801, 2019.

[15] F. Medjdoub, K. Iniewski, Gallium Nitride (GaN), physics, devices, and technology [electronic resource] : Boca Raton, FL: CRC Press, 2016.

[16] A. C. Liu, P. T. Tu, C. Langpoklakpam, Y. W. Huang, Y. T. Chang, A. J. Tzou, L. H. Hsu, C. H. Lin, H. C. Kuo and E. Y. Chang, “The Evolution of Manufacturing Technology for GaN Electronic Devices,” Micromachines (Basel), , vol. 12, no. 7, p. 737, 2021-06.

[17] L. Pan, X. Dong, Z. Li, W. Luo and J. Ni, “Influence of the AlN nucleation layer on the properties of AlGaN/GaN heterostructure on Si (1 1 1) substrates,” Applied surface science, vol. 447, p. 512–517, 2018.

[18] J. Felbinger, M. Chandra, Y. Sun, L. Eastman, J. Wasserbauer, F. Faili, D. Babic, D. Francis and F. Ejeckam, “Comparison of GaN HEMTs on Diamond and SiC Substrates,” IEEE electron device letter, vol. 28, no. 11, pp. 948-950, 2007-11,.

[19] W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, I. Omura and T. Ogura, “High breakdown Voltage undoped AlGaN-GaN power HEMT on sapphire substrate and its demonstration for DC-DC converter application,” IEEE transactions on electron devices, vol. 51, no. 11, p. 1913–1917, 2004.

[20] Y.-F. Wu, B. Keller, S. Keller, D. Kapolnek, P. Kozodoy, S. Denbaars and U. Mishra, “High power AlGaN/GaN HEMTs for microwave applications,,” Solid-state electronics, vol. 41, no. 10, p. 1569–1574, 1997.

[21] J. J. Freedsman, A. Watanabe, Y. Yamaoka, T. Kubo and T. Egawa, “Influence of AlN nucleation layer on vertical breakdown characteristics for GaN-on-Si,,” Physica status solidi. A, Applications and materials science, vol. 213, no. 2, p. 424–428, 2016.

[22] L. Pan, X. Dong, Z. Li, W. Luo and J. Ni, “Influence of the AlN nucleation layer on the properties of AlGaN/GaN heterostructure on Si (1 1 1) substrates,” Applied surface science, vol. 447, p. 512–517, 2018.

[23] D. D. Koleske, M. E. Twigg, A. E. Wickenden, R. L. Henry, R. J. Gorman, J. A. Freitas and M. Fatemi, “Properties of Si-doped GaN films grown using multiple AlN interlayers,” Applied physics letters, vol. 75, no. 20, p. 3141–3143, 1999.

[24] Y. Yamaoka, A. Ubukata, Y. Yano, T. Tabuchi, K. Matsumoto and T. Egawa, “Effect of threading dislocation in an AlN nucleation,” Semiconductor science and technology, vol. 34, no. 3, p. 35015, 2019.

[25] S. Leone, F. Benkhelifa, L. Kirste, C. Manz, S. Mueller, R. Quay and T. Stadelmann, “Suppression of Iron Memory Effect in GaN Epitaxial Layers,” Physica Status Solidi (B) Basic Research, vol. 255, no. 5, 2018.

[26] K.-P. Chang, P.-J. Lin, R.-H. Horng and D.-S. Wuu, “Growth characteristics of Fe-doped GaN epilayers on SiC (001) substrates and their effects on high breakdown voltage devices,” Materials science in semiconductor processing, vol. 119, p. 105228, 2020.

[27] Y. Oshimura, T. Sugiyama, K. Takeda, M. Iwaya, T. Takeuchi, S. Kamiyama, I. Akasaki and H. Amano, “Low leakage current in AlGaN/GaN HFETs with preflow of Mg source before growth of u-GaN buffer layer,”,” Physica status solidi. A, Applications and materials science, vol. 208, no. 7, p. 1607–1610, 2011.

[28] H. Tokuda, K. Suzuki, J. T. Asubar, M. Kuzuhara, “Electron concentration in highly resistive GaN substrates co-doped with Si, C, and Fe,” Japanese Journal of Applied Physics, vol. 57, no. 7, p. 71001, 2018.

[29] A. Klump, M. P. Hoffmann, F. Kaess, J. Tweedie, P. Reddy, R. Kirste, Z. Sitar and R. Collazo, “Control of passivation and compensation in Mg-doped GaN by defect quasi Fermi level control,”,,” Journal of applied physics, vol. 127., no. 4, p. 045702, 2020.

[30] M. L. Colussi, R. J. Baierle and R. H. Miwa, “Doping effects of C, Si and Ge in wurtzite [0001] GaN, AlN, and InN nanowires,” Journal of applied physics, vol. 110, no. 3, pp. 033709-033709–9, 2011.

[31] J. Yuan, J. Du, Y. Hou, F. Chen and Q. Li, “Carbon and Silicon Impurity Defects in GaN: Simulating Single-Photon Emitters by First Principles,” Materials, vol. 17, no. 15, p. 3788, 2024.

[32] M. A. Reshchikov and H. Morkoç, “Luminescence properties of defects in GaN,” Journal of applied physics, vol. 97, no. 6, pp. 061301-061301–95, 2005.

[33] G. W., N. Johnson, C. Chen, H. Lie, C. Kuo and I. W., “Activation energies of Si donors in GaN,” Appl. Phys. Lett., vol. 68, p. 3144–3146, 1996.

[34] X. Wang, Z.-Y. Lin, Y.-H. Sun, L. Yue, Y.-M. Zhang, J.-F. Wang and K. Xu, “Suppression of the regrowth interface leakage current in AlGaN/GaN HEMTs by Fe doped GaN substrate,” Science China. Information sciences, vol. 67, no. 6, p. 169403, 2024.

[35] T. Liu, H. Watanabe, S. Nitta, J. Wang, G. Yu, Y. Ando, Y. Honda, H. Amano, A. Tanaka and Y. Koide, “Suppression of the regrowth interface leakage current in AlGaN/GaN HEMTs by unactivated Mg doped GaN layer,”,” Applied physics letters, vol. 118, no. 7, pp. 072103-(1-6), 2021.

[36] D. S. Green, E. Haus, F. Wu, L. Chen, U. K. Mishra, and J. S. Speck, “Polarity control during molecular beam epitaxy growth of Mg-doped GaN,” Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structure, vol. 21, no. 4, p. 1804–1811, 2003.

[37] W. Götz, N. M. Johnson, J. Walker, D. P. Bour and R. A. Street, “Activation of acceptors in Mg-doped GaN grown by metalorganic chemical vapor deposition,” Applied Physics Letter, vol. 68, p. 667–669, 1996.

[38] W. Gotz, N. Johnson, D. Bour, M. McCluskey and E. Haller, “Local vibrational modes of the Mg–H acceptor complex in GaN,” Appl. Phys. Lett., vol. 69, p. 3725–3727, 1996.

[39] F. M. Barradas, L. C. Nunes, T. R. Cunha, P. M. Lavrador, P. M. Cabral and J. C. Pedro, “Compensation of Long-Term Memory Effects on GaN HEMT-Based Power Amplifiers,” Compensation of Long-Term Memory Effects on GaN HEMT-Based Power Amplifiers,” IEEE transactions on microwave theory and techniques, vol. 65, no. 9, pp. doi: 10.1109/TMTT.2017.2671368., vol. 65, no. 9, p. 2017, 3379–3388.

[40] K. Köhler, T. Stephan, A. Perona, J. Wiegert, M. Maier, M. Kunzer and J. Wagner, “Control of the Mg doping profile in III-N light-emitting diodes and its effect on the electroluminescence efficiency,” Journal of applied physics, vol. 97, no. 10, pp. 104914-104914–4, 2005.

[41] M. Meneghini, I. Rossetto, D. Bisi, A. Stocco, A. Chini, A. Pantellini, C. Lanzieri, A. Nanni, G. Meneghesso and E. Zanoni, “Buffer Traps in Fe-Doped AlGaN/GaN HEMTs: Investigation of the Physical Properties Based on Pulsed and Transient Measurements,” IEEE transactions on electron devices, vol. 61, no. 12, p. 4070–4077, 2014.

[42] S. Heikman, S. Keller, S. P. Denbaars and U. K. Mishra, “Growth of Fe doped semi-insulating GaN by metalorganic chemical vapor depostion,” Applied physics letters, vol. 81, no. 3, pp. 439–441,, 2002.

[43] A. Lesnik, M. P. Hoffmann, A. Fariza, J. Bläsing, H. Witte, P. Veit, F. Hörich, C. Berger, J. Hennig, A. Dadgar and A. Strittmatter, "Properties of C-doped GaN," Physica Status Solidi (B) Basic Research, vol. 254, no. 8, 2017.

[44] M. Hajlasz, After defining the patterns for the ohmic contacts using the photolithography process described in section 2.2.2, a Ti/Al/Ni/Au metal stack (20nm/120nm/20nm/45nm) was deposited using thermal evaporation. To facilitate metal diffusion through the AlGaN bar, Twente: Material Innovation Institue (M2i), Netherlands, 2018.

[45] G. LIU, J. WU, Q. ZHU, Z. WANG, Y. LU, B. ZHANG, C. LI, L. SANG, Y. SONG, K. SHI, X. LIU and S. YANG, "A Theoretical Calculation of the Impact of GaN Cap and AlxGa1—xN Barrier Thickness Fluctuations on Two-Dimensional Electron Gas in a GaN/AlxGa1—xN/GaN Heterostructure,," IEEE transactions on electron devices, vol. 58, no. 12, p. 4272–4275, 2011.

[46] S. Heikman, S. Keller, Y. Wu, J. S. Speck, S. P. DenBaars and U. K. Mishra, "Polarization effects in AlGaN/GaN and GaN/AlGaN/GaN heterostructures," Journal of applied physics, vol. 93, no. 12, p. 10114–10118, 2003.

[47] R. M. Chu, Y. G. Zhou, Y. D. Zheng, P. Han, B. Shen and S. L. Gu, "Influence of doping on the two-dimensional electron gas distribution in AlGaN/GaN heterostructure transistors," Applied physics letters, vol. 79, no. 14, p. 2270–2272, 2001.

[48] K. Ahmeda, B. Ubochi, M. Alqaysi, A. Al-Khalidi, E. Wasige and K. Kalna, "The role of SiN/GaN cap interface charge and GaN cap layer to achieve enhancement mode GaN MIS-HEMT operation," Microelectronics and reliability, vol. 115, pp. 113965, , 2020, doi: 10.1016/j.microrel.2020.113965..

[49] K. Ahmeda, B. Ubochi, M. H. Alqaysi, A. Al-Khalidi, E. Wasige, K. Kalna, " The role of SiN/GaN cap interface charge and GaN cap layer to achieve enhancement mode GaN MIS-HEMT operation," Microelectronics and reliability, vol. 115 , 2020.

[50] G. Liu, J. Wu, Y. Lu, B. Zhang, C. Li, L. Sang, Y. Song, K. Shi, X. Liu, S. Yang, Q. Zhu and Z. Wang, "A theoretical calculation of the impact of GaN cap and Al xGa1-xN barrier thickness fluctuations on two-dimensional electron gas in a GaN/AlxGa1-xN/GaN heterostructure," IEEE transactions on electron device, vol. 58, no. 12, p. 4272–4275, 2011.

[51] P. Waltereit, S. Müller, K. Bellmann, C. Buchheim, R. Goldhahn, K. Köhler, L. Kirste, M. Baeumler, M. Dammann, W. Bronner, R. Quay and O. Ambacher, "Impact of GaN cap thickness on optical, electrical, and device properties in AlGaN/GaN high electron mobility transistor structures," Journal of applied physics,, vol. 106, no. 2, p. 023535, 2009.

[52] A. Motayed, R. Bathe, M. C. Wood, O. S. Diouf, R. D. Vispute and S. Noor Mohammad, “Electrical, thermal, and microstructural characteristics of Ti/Al/Ti/Au multilayer Ohmic contacts to n-type GaN,” Journal of applied physics, vol. 93, no. 2, p. 1087–1094, 2003.

[53] R. Gong, J. Wang, Z. Dong, S. Liu, M. Yu, C. P. Wen, Y. Hao, B. Shen, Y. Cai, B. Zhang and J. Zhang, “Analysis on the new mechanisms of low resistance stacked Ti/Al Ohmic contact structure on AlGaN/GaN HEMTs,” Journal of physics. D, Applied physics,, vol. 43, no. 39, p. 395102–395102, 2010.

[54] B. Van Daele, G. Van Tendeloo, W. Ruythooren, J. Derluyn, M. R. Leys and M. Germain, “The role of Al on Ohmic contact formation on n -type GaN and AlGaN ⁄ GaN,” Applied physics letters, vol. 87, no. 6, pp. 061905-061905–3, 2005.

[55] T. Huang, A. Malmros, J. Bergsten, S. Gustafsson, O. Axelsson, M. Thorsell and N. Rorsman, “Electron-Mobility Transistors Using Bilayer SiNx Grown by Low Pressure Chemical Vapor Deposition,” IEEE electron device letters, vol. 36, no. 6, pp. 537-539, 2015-06.

[56] A. D. Koehler, M. J. Tadjer, T. J. Anderson, P. Chojecki, K. D. Hobart and F. J. Kub, “Advances in AlGaN/GaN HEMT Surface Passivation,” ECS Transactions, vol. 75, no. 12, p. 99–105, 2016.

[57] M. Gassoumi, A. Helali, M. Gassoumi, C. Gaquiere and H. Maaref, “High Frequency Analysis and Small-Signal Modeling of AlGaN/GaN HEMTs with SiO2/SiN Passivation,” SILICON, vol. 11, no. 1, p. 557–562, 2019.

[58] S. D. Gupta, V. Joshi, R. R. Chaudhuri and M. Shrivastava, “Novel Surface Passivation Scheme by Using p-Type AlTiO to Mitigate Dynamic ON Resistance Behavior in AlGaN/GaN HEMTs-Part II,” IEEE transactions on electron devices, vol. 68 , no. 11, pp. 5728-5735, 2021-11.

[59] P. B. Klein, S. C. Binari, K. Ikossi, A. E. Wickenden, D. D. Koleske and R. L. Henry, “Current collapse and the role of carbon in AlGaN/GaN high electron mobility transistors grown by metalorganic vapor-phase epitaxy,” Applied physics letters, vol. 79, no. 21, pp., vol. 79, no. 21, p. 3527–3529, 2001.

[60] T. Luan, Q. Jiang, S. Huang, X. Wang, H. Jin, F. Guo, Y. Yao, J. Fan, H. Yin, K. Wei, Y. Li, H. Jiang, J. Li and X. Liu, “Investigation of trapping/de-trapping dynamics of surface states in AlGaN/GaN high-electron mobility transistors based on dual-gate structures,” Elsevier B.V - Microelectronic engineering, vol. 269, p. 111916, 2023-01.

[61] H.-P. Lee, J. Perozek, L. D. Rosario and C. Bayram, “Investigation of AlGaN/GaN high electron mobility transistor structures on 200-mm silicon (111) substrates employing different buffer layer configurations,” Scientific reports, vol. 6, no. 1, pp. 37588-37588, 2016-11.

[62] M. Meneghini, C. De Santi, G. Meneghesso and E. Zanoni, “GAN POWER TRANSISTORS: DEVICES, TECHNOLOGY AND RELIABILITY,” in Power America 2021, North Carolina, USA, 2022.

[63] M. Fregolent, F. Piva, M. Buffolo, C. D. Santi, A. Cester, M. Higashiwaki, G. Meneghesso, E. Zanoni and M. Meneghini, “Advanced defect spectroscopy in wide-bandgap semiconductors: review and recent results,” Journal of physics. D, Applied physics, vol. 57, no. 43, p. 433002, 2024-11.

[64] A. Y. Polyakov, N. B. Smirnov, A. V. Turutin, I. S. Shemerov, F. Ren, S. J. Pearton and J. W. Johnson, “Deep traps and instabilities in AlGaN/GaN high electron mobility transistors on Si substrates,” Journal of vacuum science and technology. B, Nanotechnology & microelectronics, vol. 34 , no. 4, p. 4953347, 2016-07.

[65] I. Boturchuk, L. Scheffler, A. N. Larsen and B. Julsgaard, “Evolution of Electrically Active Defects in n-GaN During Heat Treatment Typical for Ohmic Contact Formation,” Physica status solidi. A, Applications and materials science, , vol. 215, no. 9, pp. 1700516 1-6, 2018.

[66] A. Y. Polyakov and I.-H. Lee, “Deep traps in GaN-based structures as affecting the performance of GaN devices,” Materials science & engineering. R, Reports : a review journal,, vol. 94, pp. 1-56, 2015-08.

[67] S. Chen, U. Honda, T. Shibata, T. Matsumura, Y. Tokuda, K. Ishikawa, M. Hori, H. Ueda, T. Uesugi and T. Kachi, “As-grown deep-level defects in n-GaN grown by metal-organic chemical vapor deposition on freestanding GaN,” Journal of applied physics, vol. 112 , no. 5, p. 053513, 2012-09.

[68] U. Honda, Y. Yamada, Y. Tokuda and K. Shiojima, “Deep levels in n-GaN Doped with Carbon Studied by Deep Level and Minority Carrier Transient Spectroscopies,” apanese Journal of Applied Physics, Vols. 51 (4), p., no. 4, pp. 04DF04-04DF04-4, 2012-04.

[69] A. Hierro, A. R. Arehart, B. Heying, M. Hansen, U. K. Mishra, S. P. Denbaars, J. S. Speck and S. A. Ringel, “Impact of Ga/N flux ratio on trap states in n-GaN grown by plasma-assisted molecular-beam epitaxy,” Applied physics letters, vol. 80, no. 5, pp. 805-807, 2002-02.

[70] J. L. Lyons, A. Alkauskas, A. Janotti and C. G. Van de Walle, “First-principles theory of acceptors in nitride semiconductors,” Physica Status Solidi (B) Basic Research, vol. 252, no. 5, pp. 900-908, 2015-05.

[71] A. Wang, S. Martin-Horcajo, M. J. Tadjer and F. Calle, “Simulation of temperature and electric field-dependent barrier traps effects in AlGaN GaN HEMTs,” Semiconductor science and technology, vol. 30, no. 1, p. 15010, 2015, doi: 10.1088/0268-1242/30/1/015010..

[72] M. Grupen, “Reproducing GaN HEMT Kink Effect by Simulating Field-Enhanced Barrier Defect Ionization,” IEEE transactions on electron devices, vol. 66, no. 9, pp. 3777-3783, 2019-09.

[73] S. Karmalkar, D.M. Sathaiya, M.S Shur, “Mechanism of the reverse gate leakage in AlGaN/GaN high electron mobility transistors,” Applied physics letters, vol. 82, no. 22, p. 3976–3978, 2003.

[74] H. Zhang, E. J. Miller and E. T. Yu, “Analysis of leakage current mechanisms in Schottky contacts to GaN and Al0.25Ga0.75N⁄GaN grown by molecular-beam epitaxy,” Journal of applied physics, vol. 99, no. 2, 2006-01.

[75] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck and U. K. Mishra, “Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors,” Applied physics letters, vol. 77, no. 2, pp. 250-252, 2000-07.

[76] G. Koley and M. G. Spencer, “On the origin of the two-dimensional electron gas at the AlGaN/GaN heterostructure interface,” Applied physics letters, vol. 86, no. 4, pp. 1-42107, 2005-01.

[77] E. Zanoni, F. Rampazzo, C. De Santi, Z. Gao, C. Sharma, N. Modolo, G. Verzellesi, A. Chini, G. Meneghesso and M. Meneghini, “Failure Physics and Reliability of GaN-Based HEMTs for Microwave and Millimeter-Wave Applications: A Review of Consolidated Data and Recent Results,” Physica status solidi. A, Applications and materials science, vol. 219, no. 24, p. 2100722, 2022-12.

[78] B. Butej, V. Padovan, D. Pogany, G. Pobegen, C. Ostermaier and C. Koller, “Method to Distinguish Between Buffer and Surface Trapping in Stressed Normally-ON GaN GITs Using the Gate-Voltage Dependence of Recovery Time Constants,” IEEE transactions on electron devices, vol. 69, no. 6, pp. 3087-3093, 2022-06.

[79] E. Bahat-Treidel, F. Brunner, O. Hilt, E. Cho, J. Wurfl and G. Trankle, “AlGaN/GaN/GaN:C back-barrier HFETs with breakdown voltage of over 1 kV and low RON × A,” IEEE transactions on electron devices, vol. 57, no. 11, pp. 3050-3058, 2010-11.

[80] M. Faqir, G. Verzellesi, A. Chini, F. Fantini, F. Danesin, G. Meneghesso, E. Zanoni and C. Dua, “Mechanisms of RF Current Collapse in AlGaN-GaN High Electron Mobility Transistors,” IEEE transactions on device and materials reliability, vol. 8, no. 2, pp. 240-247, 2008-06.

[81] C. Zhou, Q. Jiang, S. Huang and K. J. Chen, “Vertical Leakage/Breakdown Mechanisms in AlGaN/GaN-on-Si Devices,” IEEE electron device letters, vol. 33, no. 8, pp. 1132-1134, 2012-08.

[82] M. J. Uren, S. Karboyan, I. Chatterjee, A. Pooth, P. Moens, A. Banerjee and M. Kuball, “Leaky Dielectric” Model for the Suppression of Dynamic R} in Carbon-

Doped AlGaN/GaN HEMTs," IEEE transactions on electron devices, vol. 64, no. 7, p. 2826–2834, 2017.

[83] A. Tajalli, M. Meneghini, S. Besendörfer, R. Kabouche, I. Abid, R. Püsche, J. Derluyn, S. Degroote, M. Germain, E. Meissner, E. Zanoni, F. Medjdoub and G. Meneghesso, "High breakdown voltage and low buffer trapping in superlattice gan-on-silicon heterostructures for high voltage applications," Materials, vol. 13, no. 19, pp. 4271,, 2020-09, Vol.13 (19).

[84] P. Moens, A. Banerjee, M. J. Uren, M. Meneghini, S. Karboyan, I. Chatterjee, P. Vanmeerbeek, M. Casar, C. Liu, A. Salih, E. Zanoni, G. Meneghesso, M. Kuball and M. Tack, "Impact of buffer leakage on intrinsic reliability of 650V AlGaN/GaN HEMTs," in IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 2016.

[85] C. Poblenz, P. Waltereit, S. Rajan, S. Heikman, U. K. Mishra and J. S. Speck, "Effect of carbon doping on buffer leakage in AlGaN/GaN high electron mobility transistors," Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, vol. 22, no. 3, pp. 1145-1149, 2004-05.

[86] M. J. Uren, M. Caesar, S. Karboyan, P. Moens, P. Vanmeerbeek and M. Kuball, "Electric Field Reduction in C-Doped AlGaN/GaN on Si High Electron Mobility Transistors," IEEE electron device letters, vol. 36, no. 8, pp. 826-828, 2015-08,.

[87] S. R. Bahl and P. Brohlin, "A New Approach to Validate GaN FET Reliability to Power-Line Surges Under Use-Conditions," in IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, 2019.

[88] C. Zhou, Q. Jiang, S. Huang and K. J. Chen, "Vertical Leakage/Breakdown Mechanisms in AlGaN/GaN-on-Si Devices," , doi: 10.1109/LED.2012.2200874," IEEE electron device letters, vol. 33, no. 8, p. 1132–1134, 2012.

[89] C. De Santi, M. Buffolo, I. Rossetto, T. Bordignon, E. Brusaterra, A. Caria, F. Chiocchetta, D. Favero, M. Fregolent, F. Masin, N. Modolo, A. Nardo, F. Piva, F. Rampazzo, C. Sharma, N. Trivellin, G. Zhan and M. Meneghini, "Review on the degradation of GaN-based lateral power transistors," e-Prime, vol. 1, p. 100018, 2021.

[90] M. Borga, M. Meneghini, I. Rossetto, S. Stoffels, N. Posthuma, M. Van Hove, D. Marcon, S. Decoutere, G. Meneghesso and E. Zanoni, "Evidence of Time-Dependent Vertical Breakdown in GaN-on-Si HEMTs," IEEE transactions on electron devices, , vol. 64, no. 9, pp. 3616-3621, 2017-09.

[91] B. Lu, E. Piner and T. Palacios, "Breakdown mechanism in AlGaN/GaN HEMTs on Si substrate," in 68th Device Research Conference, IEEE,, Notre Dame, IN, USA, 2010, pp. 193–194. doi: 10.1109/DRC.2010.5551907.

[92] M. Knetzger, E. Meissner, J. Derluyn, M. Germain and J. Friedrich, “Correlation of carbon doping variations with the vertical breakdown of GaN-on-Si for power electronics,” Microelectronics and reliability, vol. 66, pp. 16-21, 2016-11.

[93] N. Remesh, N. Mohan, S. Raghavan, R. Muralidharan and D. N. Nath, “Optimum Carbon Concentration in GaN-on-Silicon for Breakdown Enhancement in AlGaN/GaN HEMTs,” IEEE transactions on electron devices, , vol. 67, no. 6, pp. 2311-2317, 2020-06.

[94] M. Hikita, M. Yanagihara, K. Nakazawa, H. Ueno, Y. Hirose, T. Ueda, Y. Uemoto, T. Tanaka, D. Ueda and T. Egawa, “AlGaN/GaN power HFET on silicon substrate with source-via grounding (SVG) structure,” IEEE transactions on electron devices, vol. 52, no. 9, p. 1963–19689, 2005.

[95] Y. C. Choi, M. Pophristic, H.-Y. Cha, B. Peres, M. G. Spencer and L. F. Eastman, “The Effect of an Fe-doped GaN Buffer on off-State Breakdown Characteristics in AlGaN/GaN HEMTs on Si Substrate,” IEEE transactions on electron devices, vol. 53, no. 12, p. 2926–2931, 2006.

[96] M. Li, Y. Wang, K. M. Wong and K. M. Lau, “Low-leakage-current AlGaN/GaN HEMTs on Si substrates with partially Mg-doped GaN buffer layer by metal organic chemical vapor deposition,” Chinese physics B, vol. 23, no. 3, pp. 038403-1-038403–5, 2014.

[97] Y. Wang, N. Yu, D. Deng, M. Li, F. Sun and K. M. Lau, “Improved AlGaN/GaN HEMTs grown on Si substrates by MOCVD,” in 2010 Academic Symposium on Optoelectronics and Microelectronics Technology and 10th Chinese-Russian Symposium on Laser Physics and Laser Technology, Harbin, China, 2010.

[98] S. Nandi, S. K. Dubey, M. Kumar and A. Islam, “Design and electrical modelling of a depletion-mode P-type triple-field-plated AlGaN/GaN on SiC HEMT with 2.45 kV breakdown voltage,” Microsystem technologies：sensors, actuators, systems integration, 2024.

[99] J. Cui, Y. Wu, J. Yang, J. Yu, T. Li, X. Yang, B. Shen, M. Wang and J. Wei, “Method to Study Dynamic Depletion Behaviors in High-Voltage (BV=1.4kV) p-GaN Gate HEMT on Sapphire Substrate,” in 35th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Hong Kong, 2023.

[100] H. Umeda, A. Suzuki, Y. Anda, M. Ishida, T. Ueda, T. Tanaka and D. Ueda, “Blocking-voltage boosting technology for GaN transistors by widening depletion layer in Si substrates,” IEDM Tech. Dig.,, pp. 20.5.1-20.5.4, 2010-12.

[101] A. Tajalli, M. Borga, M. Meneghini, C. D. Santi, D. Benazzi, S. Besendörfer, R. Püsche, J. Derluyn, S. Degroote, M. Germain, R. Kabouche, I. Abid, E. Meissner, E. Zanoni and Medjdou, “Vertical leakage in GaN-on-Si stacks investigated by a

buffer decomposition experiment," Micromachines (Basel),, , vol. 11, no. 1, p. 101, 2020-01.

[102] N. Herbecq, I. Roch-Jeune, A. Linge, B. Grimbert, M. Zegaoui and F. Medjdoub, "GaN-on-silicon high electron mobility transistors with blocking voltage of 3 kV," Electronics letters, vol. 51 , no. 19, pp. 1532-1534, 2015-09.

[103] Y. C. Choi, M. Pophristic, B. Peres, H.-Y. Cha, M. G. Spencer and L. F. Eastman, "High breakdown voltage C-doped GaN-on-sapphire HFETs with a low specific on-resistance," Semiconductor science and technology, vol. 22, no. 5, p. 517–521, 2017.

[104] F. Medjdoub, M. Zegaoui, B. Grimbert, N. Rolland and P.-A. Rolland, "Effects of AlGaN Back Barrier on AlN/GaN-on-Silicon High-Electron-Mobility Transistors," Applied physics express, vol. 4, no. 12, pp. 124101-124101–3, 2011.

[105] D. K. Schroder, Semiconductor Material and Device Characterization, Piscataway, NJ: IEEE Press ; Wiley, 2006.

[106] M. Singh, S. Karboyan, M. J. Uren, K. B. Lee, Z. Zaidi, "Lateral charge spreading and device-to-device coupling in C-doped AlGaN/GaN-on-Si wafers," Microelectronics Reliability, vol. 95, pp. 81-86, 2019.

[107] M. J. Uren, M. Casar, M. A. Gajda and M. Kuball, P.A. Houston, M. Kuball, "Buffer transport mechanisms in intentionally carbon doped GaN heterojunction field effect transistors," APPLIED PHYSICS LETTERS, vol. 104, no. 26, p. 263505, 2014.

[108] M. J. Uren, M. Cäsar, M. A. Gajda and M. Kuball, "Buffer transport mechanisms in intentionally carbon doped GaN heterojunction field effect transistors," Applied physics letters, vol. 104, no. 26, pp. 1077-3118, 2014.

[109] M. Hibberd, V. Frey, B. Spencer, P. Mitchell, P. Dawson, M. Kappers, R. Oliver, C. Humphreys and D. Graham, "Dielectric response of wurtzite gallium nitride in the terahertz frequency range," Solid state communications, vol. 247, pp. 68-71, 2016.

[110] W. Waller, M. A. Gajda, S. Pandey, J. J. Donkers, D. Calton, J. Croon, J. Sonsky, M. Uren and M. Kuball, "Control of Buffer-Induced Current Collapse in AlGaN/GaN HEMTs Using SiNx Deposition," IEEE TRANSACTIONS ON ELECTRON DEVICES, vol. 64, no. 10, pp. 4044-4049, 2017.

[111] M. J. Uren, M. Silvestri, M. Casar, G. A. M. Hurkx, J. Croon, J. Sonsky and M. Kuball, "Intentionally Carbon-Doped AlGaN/GaN HEMTs:Necessity for Vertical Leakage Paths," IEEE ELECTRON DEVICE LETTERS, vol. 35, no. 3, pp. 327-330, 2014.

[112] I. Chatterjee, M. Uren, S. Karboyan, A. Pooth, P. Moens, A. Banerjee and M. Kuball, "Lateral Charge Transport in the Carbon-Doped Buffer in AlGaN/GaN-on-

Si HEMTs," IEEE TRANSACTIONS ON ELECTRON DEVICES, vol. 64, no. 03, pp. 977-983, 2017.

[113] A. Nardo, C. De Santi, C. Koller, C. Ostermaier, I. Daumiller, G. Meneghesso, E. Zanoni and M. Meneghini, "Positive and negative charge trapping GaN HEMTs: Interplay between hermal emission and transport-limited processes," Microelectronics and reliability, vol. 114, 2020.

[114] C. Koller, G. Pobegen, C. Ostermaier, and D. Pogany, "Effect of carbon doping on charging/discharging dynamics and leakage behavior of carbon-doped GaN," IEEE Transactions on Electron Devices, vol. 65, no. 12, pp. 5314-5321, 2018.

[115] S. Yang, C. Zhou, S. Han, J. Wei, K. Sheng and K. J. & Chen, "Impact of substrate bias polarity on buffer-related current collapse in AlGaN/GaN-on-Si power devices," IEEE Transactions on Electron Devices, vol. 64, no. 12, pp. 5048-5056, 2017.

[116] J. Bai, T. Wang, P. Parbrook, K. Lee and A. Cullis, "A study of dislocations in AlN and GaN films grown on sapphire substrates," Journal of crystal growth, vol. 282, no. 3-4, pp. 290-296, 2005.

[117] Y. Cai, C. Zhu, L. Jiu, Y. Gong, X. Yu, J. Bai, V. Esendag and T. Wang, "Strain analysis of GaN HEMTs on (111) silicon with two transitional AlxGa1− xN layers," Materials, vol. 11, no. 10, p. 1968, 2018.

[118] W. A. Hubbard, "Imaging Electronic Degradation in a Stressed GaN HEMT," in 2024 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), 2024, Sinagapore , 2024.

[119] Y. Wang, S. Huang, Q. Jiang, X. Wang, F. Guo, C. Feng, J. Fan, H. Yin, X. Gao, K. Wei, Y. Zheng and X. Liu, "Gate Leakage Suppression and Threshold Voltage Stability Improvement in GaN-Based Enhancement-Mode HEMTs on Ultrathin-Barrier AlGaN/GaN Heterostructures with a p-Doping-Free GaN Cap," Journal of electronic materials, vol. 53, no. 7, p. 3926–3932, 2024.

[120] S. Heikman, S. Keller, S. P. DenBaars, U. K. Mishra, F. Bertram and J. Christen, "Non-planar Selective Area Growth and Characterization of GaN and AlGaN," Japanese Journal of Applied Physics, vol. 42, no. 10, pp. 6276–6283, , 2003.

[121] M. Wu, K. Cheng, L. Yang, B. Hou, X.-C. Zhang, P. Wang, M. Zhang, Q. Zhu, X.-F. Zheng, Y.-S. Hu, X.-H. Ma and Y. Hao, "Structural and thermal analysis of polycrystalline diamond thin film grown on GaN-on-SiC with an interlayer of 20 nm PECVD-SiN," Applied physics letters, vol. 120, no. 12, p. 121603, 2022.

[122] M. A. Reshchikov, D. O. Demchenko, A. Usikov, H. Helava and Y. Makarov, "Carbon defects as sources of the green and yellow luminescence bands in undoped

GaN," Physical review. B, Condensed matter and materials physics, vol. 90, no. 23, 2014.

[123] Y. Cordier, M. Hugues, F. Semond, F. Natali, P. Lorenzini, Z. Bougrioua, J. Massies, E. Frayssinet, B. Beaumont, P. Gibart and J.-P. Faurie, "Structural and electrical properties of AlGaN/GaN HEMTs grown by MBE on SiC, Si(1 1 1) and GaN templates," Journal of crystal growth, vol. 278, no. 1, p. 383–386, 2005.

[124] H. Amano, N. Sawaki, I. Akasaki and Y. Toyoda, "Metalorganic vapor phase epitaxial growth of a high quality GaN film using an AlN buffer layer," Appl. Phys. Lett. , vol. 48, p. 353–355, 1986.

[125] C. Koller, L. Lymperakis, D. Pogany, G. Pobegen, and C. Ostermaier, "Mechanism leading to semi-insulating property of carbon-doped GaN: Analysis of donor acceptor ratio and method for its determination," Journal of Applied Physics, vol. 130, no. 1, 2021.

[126] J. Manuel, F. Morales, R. García, R. Aidam, L. Kirste and O. Ambacher, "Threading dislocation propagation in AlGaN/GaN based HEMT structures grown on Si (111) by plasma assisted molecular beam epitaxy," Journal of crystal growth, vol. 357, pp. 35-41, 2012.

[127] M. Kanechika, S. Yamaguchi, Y. Kishida, K. Kitazumi, K. Isegawa, and Y. Kimoto, "A study on the classification of threading dislocations in GaN substrate by spot size using X-ray topography high-resolution image," *JAPANESE JOURNAL OF APPLIED PHYSICS*, vol. 64, no. 3, pp.031001, 2025.

[128] J. L. Rouviere, M. Arlery, B. Daudin, G. Feuillet, and O. Briot, "Transmission electron microscopy structural characterisation of GaN layers grown on (0001) sapphire," Materials science & engineering. B, Solid-state materials for advanced technology, vol. 50, no. 1, pp. 61–71, 1997.

3. Dynamics of Carbon doping in the C:GaN Buffer Layer

3.1 Introduction

As discussed in Chapter 2, among commercially available substrates, Si (111) presents an attractive option for the growth of wurtzite GaN, despite the inherent challenges posed by lattice and thermal expansion coefficient mismatches. These mismatches inevitably lead to TDs and other structural defects. These defects act as strain-relieving mechanisms, accommodating the thermal and lattice mismatches between different layers [3].

Carbon is the most widely employed dopant in power GaN devices to achieve a highly resistive buffer layer, as it effectively suppresses buffer leakage and enhances breakdown characteristics. Typical carbon doping concentrations range around ~10^{19} cm^{-3} for power GaN devices and ~10^{18} cm^{-3} for RF devices [4] [5] [6]. The key objective is to pin the Fermi level towards the valence band, thereby making the material semi-insulating [7]. However, whether incorporated intentionally or unintentionally, carbon significantly influences the device's electrical and optical performance, as well as its overall reliability [8] [9].

Uren et al. [4] [5] extensively discussed the role of carbon in modulating dynamic R_{ON} in GaN-on-Si devices. In [10], they compared two wafers, one exhibiting clear gap dependence and the other showing a weaker gap dependence, which was attributed to a vertical leakage path across the entire contact gap spacing. However, they did not disclose the exact carbon concentrations in the two wafers.

Cioni et al. [6] proposed that increasing carbon doping decreases dynamic R_{ON}, based on their study using simulations, pulsed I-V, capacitance, and dynamic R_{ON} measurements. They concluded that higher carbon doping leads to increased donor compensation, reducing the net acceptor concentration, thereby limiting the depletion of the two-dimensional electron gas (2DEG). Other studies, such as [11], emphasise that higher donor compensation in heavily carbon-doped GaN layers enhances semi-insulating behaviour. Koller et al. [7] investigated a range of carbon concentrations (~10^{18} cm^{-3}, 1×10^{19} cm^{-3}, and 7×10^{19} cm^{-3}) and argued that higher carbon concentrations lead to a wider depletion region, restricting vertical charge transport between the UID/CGaN. This behaviour was attributed to increased donor compensation, effectively reducing the acceptor density, reinforcing their previous findings in [11].

Scales et al. [12] studied the impact of carbon on electrical behaviour using techniques such as conductive atomic force microscopy (C-AFM) and electron beam-induced current

(EBIC). Their findings revealed that all electrically active dislocations exhibited carbon enrichment, implying carbon segregation around dislocations. Based on the observed behaviours in our study, we bridge the gap between carbon concentration, carbon segregation, and the dominant leakage mechanism.

The aim of this study is to investigate the impact of the carbon incorporation on dynamic R_{ON}. A unique and distinct result was observed from the electrical characterisation obtained via substrate ramp measurements. Nuances arising due to variations in carbon concentration and the corresponding transport mechanisms were further analysed using XRD. While precisely identifying the individual contributions of leakage pathways may not be critical, understanding these mechanisms is essential for explaining the rapid device recovery during transitions between the off-state and on-state. This study proposes a new interpretation of the implications of incorporated carbon and intrinsic defects within the lattice structure on dynamic R_{ON}.

3.2 Experimental Methods

3.2.1 Samples

The AlGaN/GaN epitaxial structures used in this section were as described in Section 2.3. The epitaxial stack consists of a 140 nm AlN NL, followed by a 3.3 µm AlN/GaN superlattice (SRL), a 1 µm CGaN layer, a 0.5 µm UID GaN layer, a 20 nm AlGaN barrier layer with 20% Al composition, and a 3 nm undoped GaN cap grown on a 625 µm Si substrate. Three wafers with nominally identical epitaxial layers, but varying carbon doping concentrations in the CGaN layer, were studied. The carbon doping concentration in wafers A, B, and C are 2×10^{18} cm^{-3}, 6×10^{18} cm^{-3}, and 1×10^{19} cm^{-3}, respectively. The SRL was also carbon-doped, with a concentration of 2×10^{19} cm^{-3}. A 2DEG density of $5\text{x}10^{12}$ cm^{-2} was extracted from the capacitance-voltage measurements on the wafers, and R_{Sheet} was approximately 710 Ω/square.

All experiments were performed on the TLM structures, depicted in Figure 2.17, and ring-shaped ohmic contact structures used for isolating the one-dimensional (1D) conduction (Figure 3.2(b)). The test structure consists of a large circular mesa with two concentric ohmic contacts: a large outer ring and a smaller central disk. When V_{SUB} is applied to the substrate, the current primarily flows vertically through the epitaxial layers beneath the contacts. Since the lateral distance between the two ohmic contacts is minimal, the potential lateral leakage path is extremely short, making lateral leakage

negligible. As a result, conduction is predominantly 1D, meaning the measured leakage is dominated by the vertical transport properties.

In the ring-shaped structure, the outer ring disk has a width of 500 µm, while the smaller central disk has a radius of 40 µm. The separation between these two rings remains constant at 10 µm, allowing for a direct comparison to the TLM structure with a similar gap spacing. Meanwhile, the TLM structures had gap spacings ranging from 5 µm to 25 µm, with a fixed ohmic contact width of 100 µm. The fabrication methods for both TLM and ring-shaped structures are outlined in Chapter 2.

3.2.2 Measurement Techniques

High Resolution X-Ray Diffraction (HR-XRD) rocking curve measurements were carried out to evaluate the crystal quality and TDD, as discussed in detail in section 2.6.6. FWHM values of (0 0 0 2) and (1 0 $\bar{1}$ 2) ω scans have been used to estimate the densities of edge and screw dislocations. Additionally, cross-sectional TEM imaging of Wafer C was conducted, offering a detailed visualisation of the dislocation propagation within the crystalline lattice, particularly the CGaN and the SRL. These images further complement the XRD analysis by providing information on the distribution of the defects as well as the dominant dislocation types within the heterostructure.

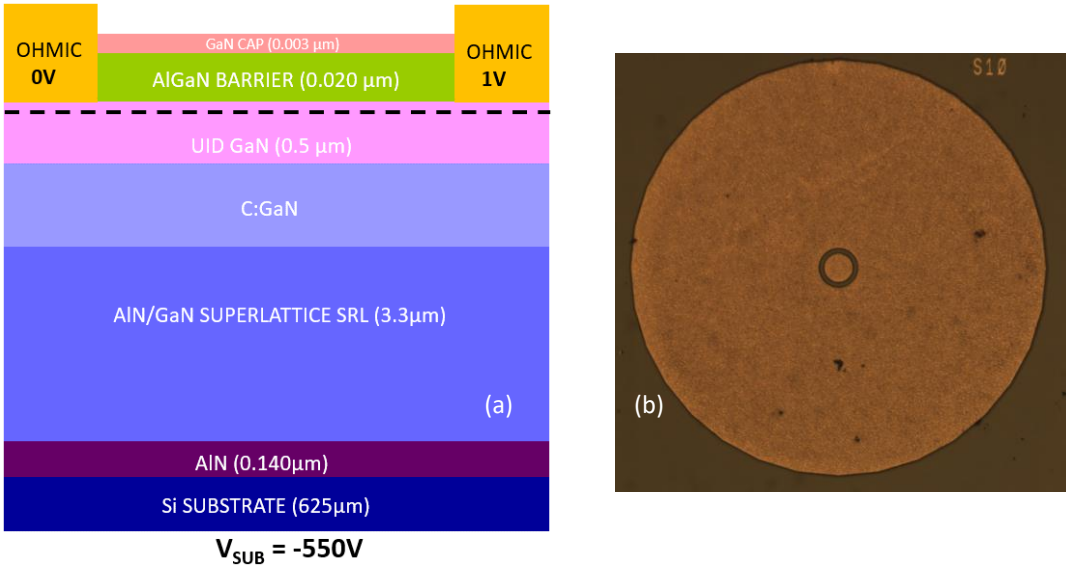

Figure 3-1 - (a) Schematic of the AlGaN/GaN epitaxy under biasing conditions. (b) A central disk surrounded by 500 µm-wide ring-shaped ohmic contacts with a separation of 10 µm between the contacts. This S10 structure is specifically designed for vertical leakage current measurements.

The buffer current-voltage (IV) characteristics were studied using substrate bias measurements. Channel currents were monitored by applying a sensing voltage of 1 V (Figure 3.1 (a)) between the ohmic contacts to minimise surface state effects and self-heating phenomena [23] [24]. The V_{SUB} was ramped up to -300 V, -450 V, and -550 V, then swept back to 0 V at a ramp rate of 10 V/s. Measurements at -450 V are not included, as the observed trends were consistent with those at -550 V. As explained in section 2.6.4, this polarity of the V_{SUB} ensures the OFF-state conditions of the HEMT [25].

The substrate transient measurements, as detailed in Section 2.6.5, were also employed to evaluate the charging and discharging behaviours in the CGaN buffer, excluding surface effects [23]. During the stress phase, a constant substrate voltage V_{SUB} of -300V was applied for 10 s, while channel currents were measured by applying a sensing voltage of 1 V between the ohmic contacts [5] [26], similar to the substrate ramp measurements. During the recovery phase, channel currents were measured for 300 s, allowing the device to return to equilibrium after the immediate removal of the stress bias. The time constant (τ) was extracted using exponential fitting [27].

All measurements were performed at room temperature and in the dark. Multiple identical structures across the sample were measured to account for variations across each wafer. The average results were then used for analysis.

3.3 Results

The wafers used in this study were grown using MOCVD, a widely adopted technique for producing high-quality GaN at industrial scales by NXP Semiconductors. However, this method is known to be susceptible to unintentional carbon incorporation, resulting in the formation of point defects such as tri-carbon complexes or interstitials, primarily due to the reactor's memory effect [1] [28] [29].

Wurtzite c-plane GaN [0 0 0 1] films typically exhibit three types of threading dislocations, each aligned parallel to the c-axis. These dislocations are categorised as edge, mixed, and screw dislocations, distinguished by their respective Burger vectors [30]. The calculation of the corresponding dislocation densities has been detailed in section 2.6.6. Table 3.1 summarises the TD densities for Wafers A, B, and C.

Wafer	A	B	C
FWHM ω 002 (arcsec)	786.6	704.88	605.16
FWHM ω 102 (arcsec)	1958.04	1295.64	1235.52
T_{screw} (cm^{-2}) x10^8	12.4 ± 0.83%	9.9 ± 0.49%	7.35 ± 0.90%
T_{edge} (cm^{-2}) x10^9	17.0 ± 1.72%	6.25 ± 2.26%	6.15 ± 3.01%
Defect density(cm^{-2}) via AFM	4.72 x10^8	3.80 x 10^8	-
Surface Morphology (RMS)	0.26nm	0.253nm	2.2nm

Table 3.1 - Calculated Edge and Screw Dislocation Densities from HRXRD and RMS Values from AFM

Each of these TD types is associated with local lattice distortions. Edge-type dislocations, which run parallel to the [0001] axis, are primarily linked to lattice twists and are represented by the FWHM of the (1 0 $\bar{1}$ 2) plane. Screw dislocations accommodate lattice tilts, represented by the FWHM of the (0002) plane, while mixed dislocations involve both twists and tilts [30] [31]. Table 3.1 illustrates a monotonic increase in the FWHM of rocking curves with decreasing carbon doping concentrations across all investigated GaN wafers.

Wafer A, characterised by the lowest carbon doping concentration, exhibits the highest TDD, primarily due to its edge dislocation density, which slightly exceeds the typical reported range of ~10^9 cm^{-2} [5]. This results in the lowest crystal quality among the three wafers. In contrast, wafers B and C demonstrate TDD values approximately an order of magnitude lower than wafer A. This indicates that crystal quality improves as carbon doping concentration increases, despite the dominance of edge-type dislocations in the TDD across all samples.

Figure 3.2 (a) - (c) shows the 5 x 5μm^2 AFM images of Wafer A, B and C, respectively. The root mean square (RMS) roughness values were obtained as 0.26nm, 0.253nm and 2.3nm, respectively [32]. The pits (visible as black dots on the surface) are clearly observed in (a) and (b), and in contrast, (c) displays rather intriguing surface morphology, resulting from contamination or the photoresist layer not being properly stripped off.

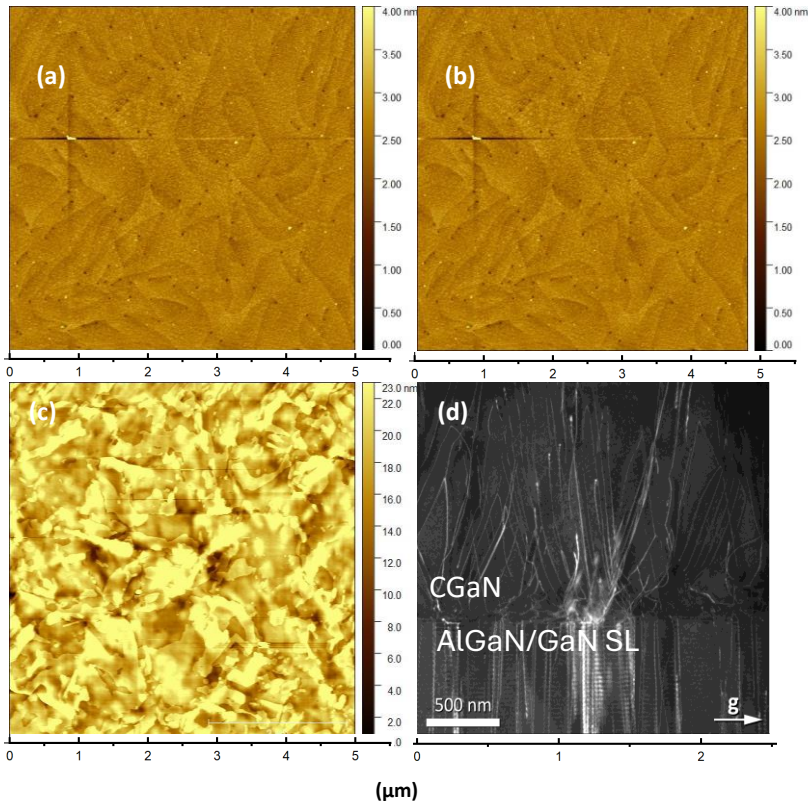

Figure 3-2 - (a) - (c) shows the 5 x 5µm² AFM images of wafer A, B and C respectively (d) The cross-sectional image indicates edge type TDs threading upwards parallel to the (0001) direction, resulting larger distance between the dislocation. Edge dislocations are observed to bundle up together, forming into one large dislocation, which contribute to enhanced crystal quality.

Previously reported RMS values for carbon-doped GaN are in the range of 0.13nm – 2.4nm [33] [34] [35] [36] [37]. Our results fall within this reported range, even though the RMS value for wafer C is significantly higher compared to wafers A and B.

The dislocation density for Wafer A and Wafer B was also estimated using AFM images by counting the pit density. As the edge dislocation pits are too small to be resolved at the magnification used, this method provides an estimate of the screw-component dislocation density, comparable to values derived from the (0002) FWHM in XRD. The estimated values were 4.42 x 10^8 cm^{-2} for Wafer A and 3.80×10^8 cm^{-2} for Wafer B. These results follow the same trend as observed in the XRD analysis, where the dislocation density decreases between Wafer A and Wafer B, although the AFM-derived values are approximately one-third of those obtained from XRD. For Wafer C, however, pit counting could not be carried out because the AFM image was unclear, possibly due to surface contamination.

A further inconsistency arises when comparing the AFM and XRD results for Wafer C. The highest RMS value for wafer C, as estimated by AFM, is notably greater, likely being

overlooked, while the TDD estimated by XRD is the lowest among the three wafers. Clearly, these figures differ significantly. Oliver et al. [38] pointed out that AFM primarily reveals surface features, such as pits associated with screw or mixed dislocations, while edge-type dislocations also produce pits, but these are often too small to be reliably detected with AFM [38]. In contrast, TEM provides detailed visualisation of the entire dislocation network, including buried defects, offering a more accurate assessment of overall crystal quality. This distinction is likely attributed to the clustering of edge-type TDs at heterojunctions, as seen in Figure 3.2 (d). Since the X-ray penetration depth is roughly 5 μm [39], XRD provides a comprehensive measurement of the bulk GaN crystal quality, while TEM complements this by visualising buried defects. Together, these methods give a complete picture for evaluating bulk crystal quality, which is crucial for our study.

Figure 3.3 shows the normalised channel currents for the bidirectional substrate ramp sweeps of Wafer A, Wafer B, and Wafer C, highlighting the effect of carbon concentration in the CGaN layer. Several cells from each wafer were measured as the devices were ramped from 0 V to -300 V and back at 10 V/s. All currents were normalised to the 0 V channel conductivity before bias application and are plotted against $V_{SUB.}$ The forward sweep from 0V to -300 V and the return sweep are indicated by solid and dashed black arrows, respectively, a convention maintained throughout this chapter.

The theoretical capacitive coupling line represents the back-gating threshold voltage (V_{TH}) required to pinch off the 2DEG channel, assuming an ideal dielectric buffer, where the channel currents is ideally expected to decrease linearly with V_{SUB} [5] [26]. The light grey dashed line indicates the back-gating V_{TH} of -428.75 V for wafers A, B, and C, which share the same stack thickness. However, deviations from this linearity occur if conduction arises in an intermediate layer, shifting conductivity above or below the theoretical line [5].

Figure 3.3(a) compares the 10 μm TLM gap spacing of Wafers A, B, and C. Hysteresis is observed in all three wafers, consistent with previously reported GaN-on-Si epitaxies, indicating the presence of trapping effects [10] [5]. Notably, Wafer A exhibits greater hysteresis, suggesting a more pronounced trapping effect compared to Wafer C. Upon displaying the capacitive behaviour up to -10 V, all normalised currents can be seen further deviating below the capacitive coupling line as the carbon concentration decreases. This suggests an increase in transconductance beyond the theoretical prediction, meaning lower carbon concentrations result in higher transconductance. As V_{SUB} increases, Wafer

C, with the highest carbon concentration, reaches current saturation first at -25 V, followed by Wafer B at approximately -60 V, and finally Wafer A at -100 V. Additionally, the return sweep currents for all three wafers remain higher than their initial 0 V currents, indicating an increase in the 2DEG compared to the forward sweep at 0 V.

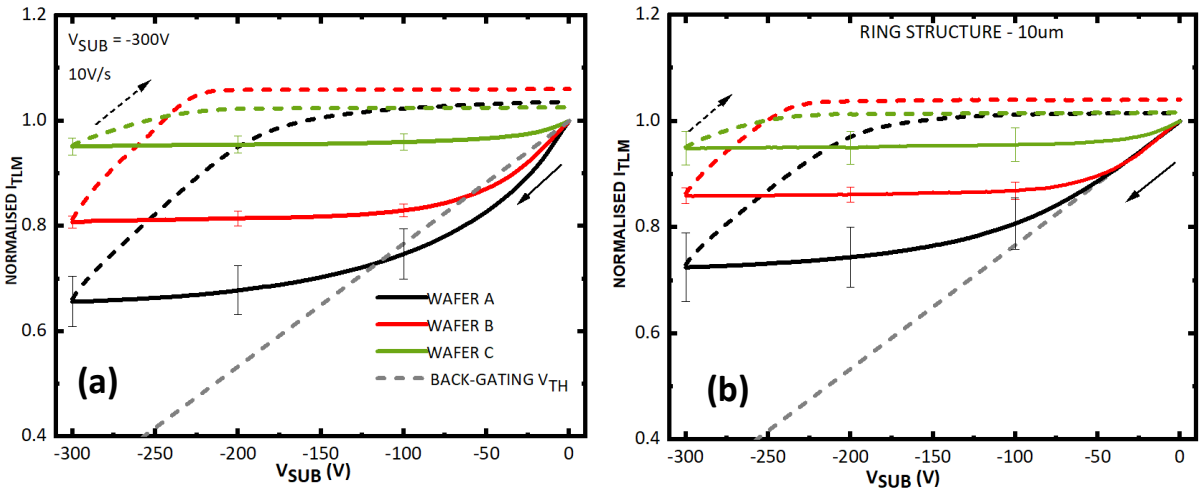

Figure 3-3 - Normalised channel currents of the wafers A, B and C. (a) TLM gap spacing 10um (b) ring shaped ohmic contact structures where the lateral leakage is insignificant with a dominant vertical leakage path. A substrate bias ramp rate 10V/s was used. The forward sweep from 0V to -300 V and the return sweep are indicated by a solid and dashed arrows respectively. The grey dashed line represents the capacitive coupling line.

Figure 3.3(b) presents the normalised substrate ramp curves for the larger ring-style outer ring and disk-style ohmic structures. In contrast to Figure 3.3(a), where deviations below the capacitive coupling line were observed, all normalised currents in this case are bounded by the capacitive coupling line. Despite this difference, the overall trend remains consistent with that observed in Figure 3.3(a), indicating a similar response across both structures. The error margins for Wafers A, B and C in (a) are approximately ±4.6%, ±1.2% and ±1.6% while (b) are approximately ±5.1%, ±1.44% and ±3.15%, respectively.

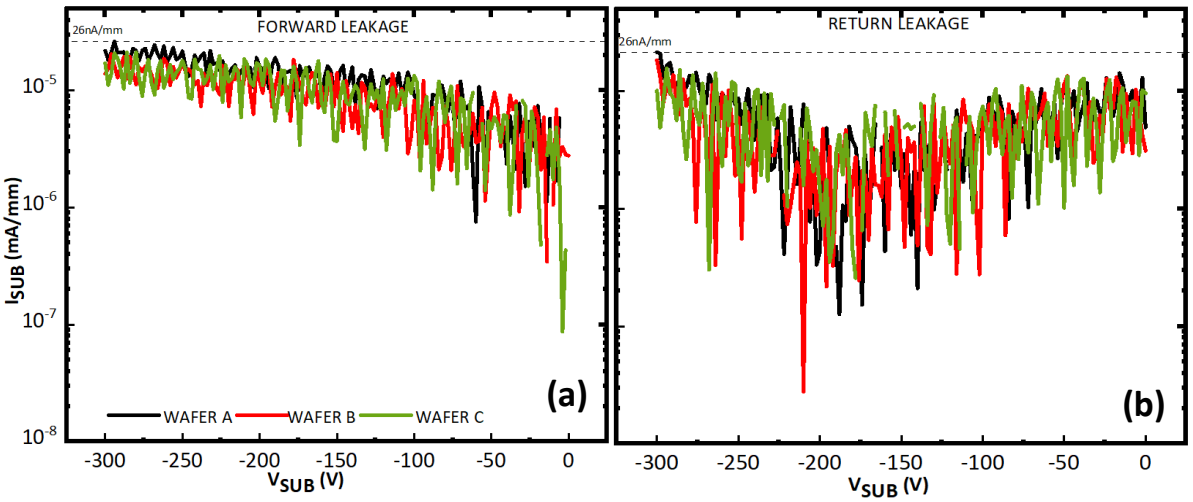

Figure 3-4 - Substrate leakage currents of the Bi-directional substrate ramp characteristics for TLM with gap spacing 10 µm, of Wafer A, B and C, at a sweep rate of 10 V/s. (a) forward sweep from 0 V to -300 V and (b) return sweep.

The substrate leakage currents (I_{SUB}) during the forward sweep, shown in Figure 3.4 (a), reveal slightly higher leakage current for wafer A compared to that of wafer C, particularly for V_{SUB} greater than -200 V. However, as illustrated in Figure 3.4(b), the return sweep leakage currents for both wafers remain comparable.

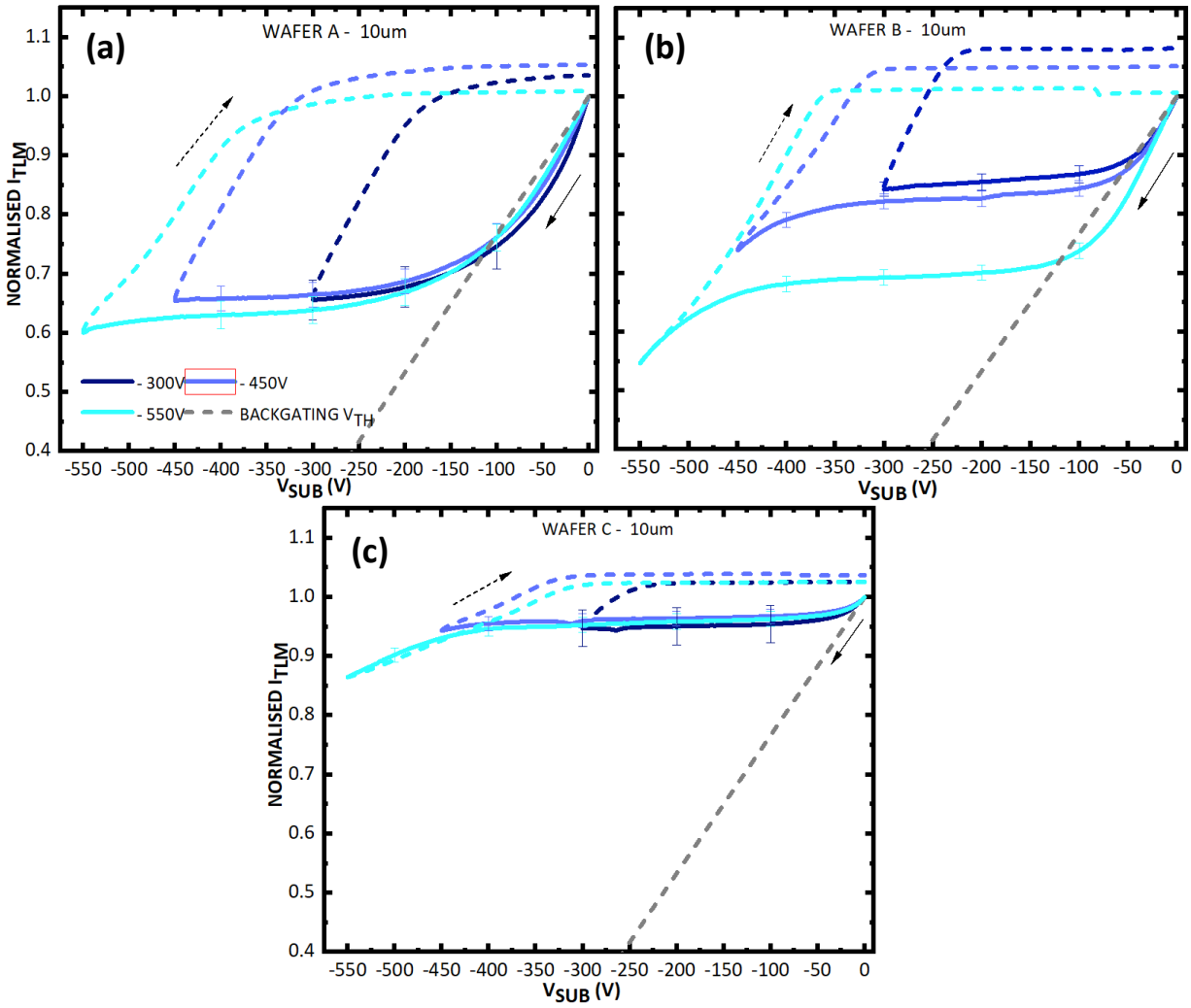

Figure 3-5 - Normalised channel currents of the (a) wafer A (b) wafer B (c) wafer C at V_{SUB} = -550 V. TLM gap spacing 10 µm has been used for consistency. The forward sweep from 0V to -550 V and the return sweep are indicated by a solid and dashed line respectively. The grey dashed line represents the capacitive coupling line.

Figure 3.5 presents the current-voltage characteristics of the 10 µm TLM structures for the three wafers as V_{SUB} is swept from 0 V to -550 V and back to 0 V. Understanding carrier transport at V_{SUB} = -550 V is crucial, as it approaches the nominal breakdown voltage (600 V) of the epitaxy used in this study. Compared to the -300 V current profile, noticeable changes are observed. The plateau region ends first for Wafer C at -400 V, followed by Wafer B at -450 V, and Wafer A at -550 V. Beyond this point, positive charge accumulation ceases, with any remaining charge retained within the CGaN layer [5] [35]. The error margins at specific substrate voltages were also evaluated. For Wafer A, the errors at –300 V, –450 V, and –550 V are approximately ±5.1%, ±3.1%, and ±2.3%, respectively. For Wafer B, the corresponding values are ±1.44%, ±1.6%, and ±1.3%, while for Wafer C they are ±3.15%, ±1.25%, and ±1.32%.

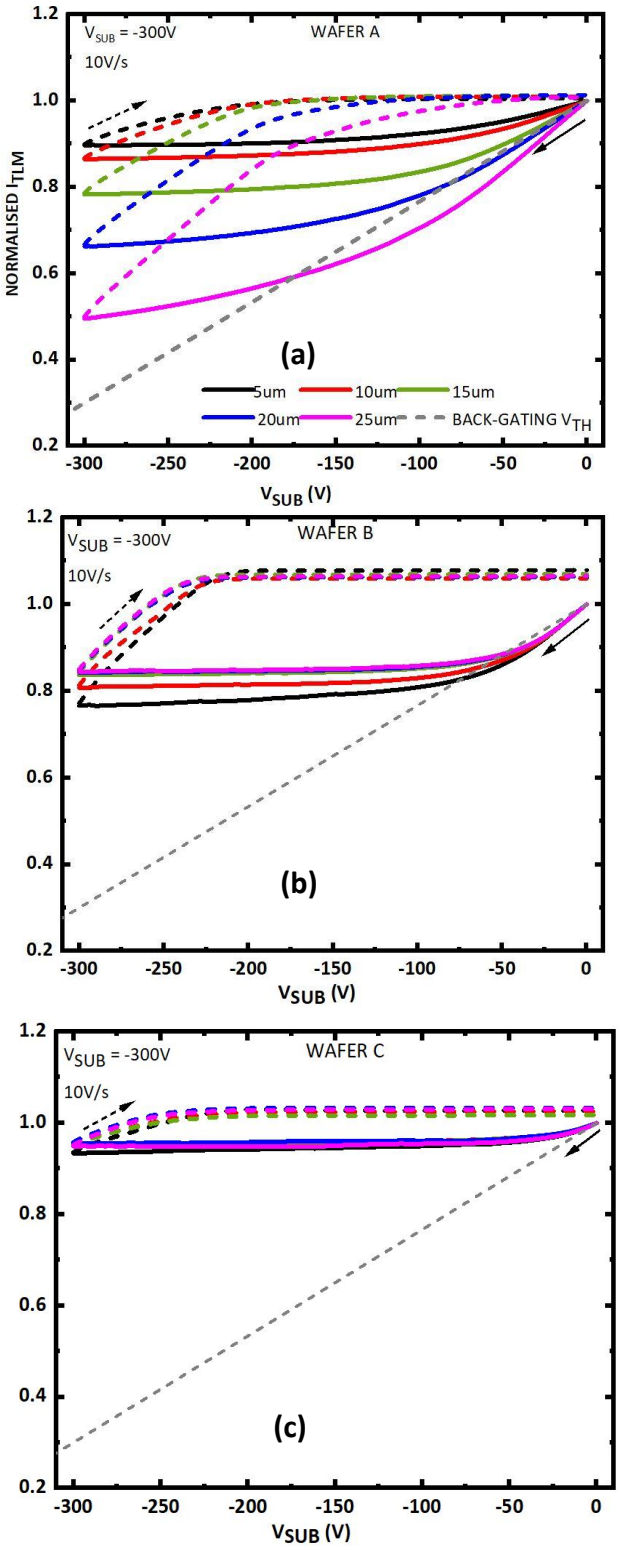

Figure 3-6 - Normalised channel conductivity of different TLM gap spacing from 5µm - 25 µm, as a function of the V_{SUB} for: (a) wafer A (b) wafer B and (c) wafer C. The grey dashed line (ideal line) represents the capacitive coupling line and the forward sweep, and the return sweep normalised currents are represented by a black solid line arrow and a black dashed line arrow respectively.

Figure 3.6 (a), (b), and (c) present the bidirectional substrate ramp measurements performed on TLM gap spacings ranging from 5 µm to 25 µm for Wafers A, B, and C, respectively. Multiple cells from each wafer were measured to evaluate the variation within each sample. As observed in Figure 3.6(a), Wafer A exhibits a strong gap dependence, while Wafer C shows a much weaker dependence, with Wafer B displaying an intermediate behaviour.

Figure 3.7 illustrates the substrate bias and time dependence of the stress and recovery phases for the three wafers. Figure 3.7(a) shows the stress phase, where a transient response was observed under a V_{SUB} of -300 V, while Figure 3.7(b) corresponds to the recovery phase following the removal of V_{SUB}. All currents are normalised to the current at V_{SUB} = 0 V.

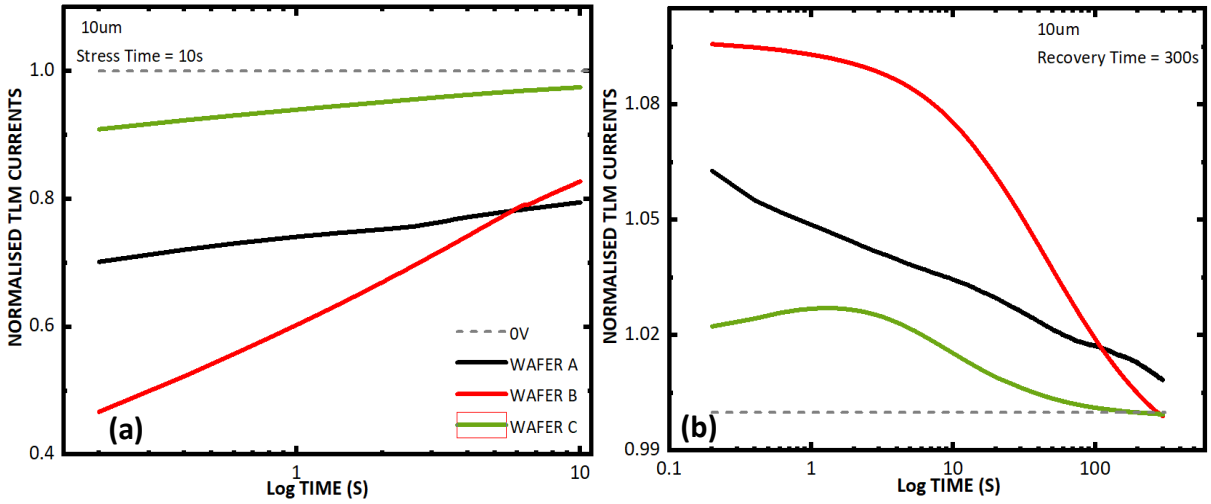

Figure 3-7 - Normalised channel currents for 10 µm TLM structures of Wafer A, Wafer B and Wafer C, during the (a) stress phase (b) recovery phase of the substrate transient measurements. A V_{SUB} of -300 V was applied for 10 seconds, followed by a 300-second measurement of the channel current at 0 V after the bias was removed All currents are normalised to the 0V DC currents. Error margins were determined to be ±1.22%, ± 1.46% and ±1.65% for Wafer A, B and C, respectively.

Upon the application of an off-state stress (V_{SUB} = -300 V), the normalised current levels are 0.7 for Wafer A, 0.47 for Wafer B, and 0.91 for Wafer C, attributed to the backgating effect. In an ideal structure with no trapping, the channel currents should immediately drop to 0.3 when subjected to V_{SUB} = -300 V, as predicted by the theoretical substrate V_{TH} line observed in the substrate ramp graphs. However, in all three wafers, the current levels exceed this predicted value, indicating the presence of positive charge storage. Wafer B exhibits a more substantial backgating effect compared to both Wafer A and Wafer C, which is inconsistent with the behaviour observed in the substrate ramp measurements. Positive-going current transients are observed, implying increasing

channel currents, which suggests continued accumulation of positive charge within the CGaN layer [40].

The recovery transient response, shown in Figure 3.7(b), exhibits elevated channel currents for all three wafers, exceeding the 0 V equilibrium current level, as indicated by the grey dashed line. This behaviour is a direct consequence of the backgating effect. In the absence of the substrate bias, a gradual decrease in channel currents is observed, indicating that the channel is returning to equilibrium. This current reduction is primarily attributed to electron diffusion from the 2DEG into the CGaN, which plays a significant role in discharging the previously accumulated positive charge.

Figure 3.8 presents the extracted time constants (τ) alongside their respective exponential curve fitting [27]. All transient responses exhibit multi-exponential behaviour, indicating that a single exponential function would not provide an accurate fit. Furthermore, the initial few seconds of the transient response were excluded from the fitting process, as they may involve rapid trapping and detrapping effects that are not well captured within the primary relaxation trends [41]. Similarly, the final few seconds were omitted from extrapolations, as long-term relaxation mechanisms could dominate at later times, diverging from the primary exponential decay behaviour, as previously discussed by Bisi et al. [41]. The chosen interval of 100s–200s was selected as it demonstrates a relatively stable exponential decay trend, with all three slopes maintaining consistency with the dominant transient behaviour.

The extracted time constants for Wafer A, Wafer B, and Wafer C are 206.5 s ±9.09, 140.16 s ±0.44, and 73.13 s ±6.447, respectively, indicating that Wafer C, which has the highest carbon concentration, undergoes the fastest recovery compared to the other two samples.

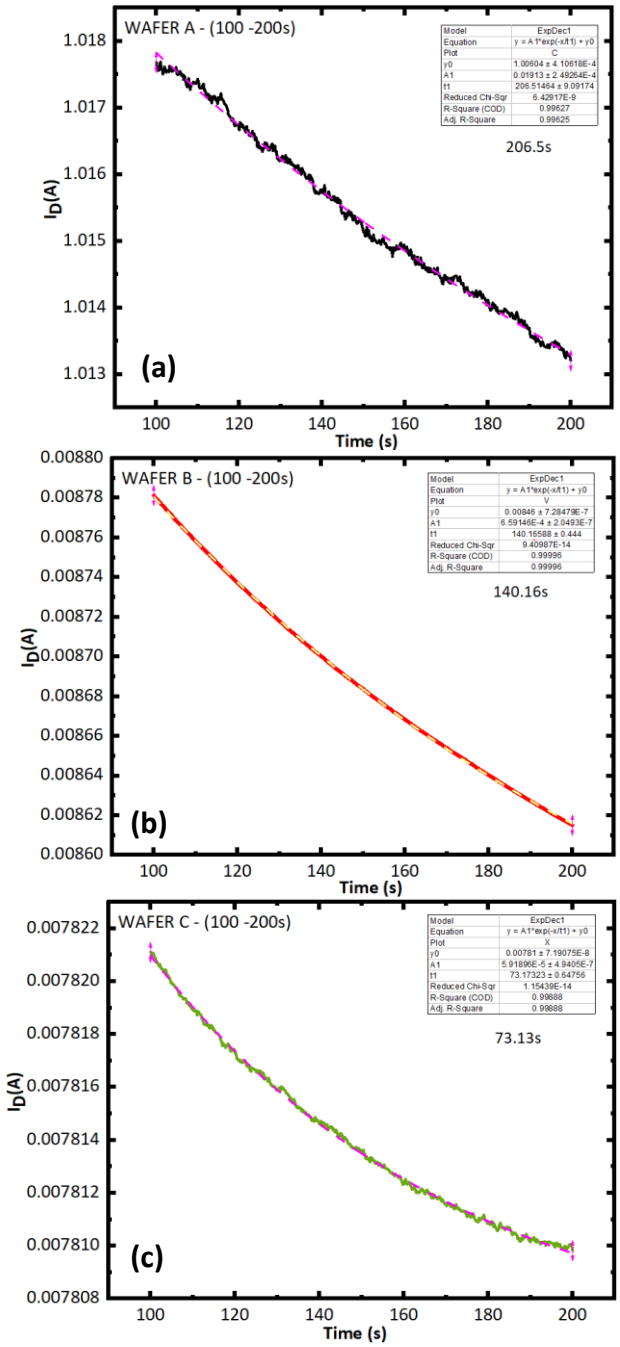

Figure 3-8 - Extracted time constants of the (a) Wafer A (b) Wafer B and (c) Wafer C, using the exponential curve fitting to the channel current decay. The fitted equation follows the $y = y_0 + Ae^{t/\tau}$.

To further investigate the trapping and detrapping dynamics influenced by varying carbon doping concentrations in the CGaN layer, experimental results were compared with TCAD simulations to understand better the mechanisms governing the observed dynamic R_{ON} behaviour. As illustrated in Figure 3.9, the simulated substrate ramp curves partially capture the trend among Wafers A, B, and C, each exhibiting distinct saturation behaviours.

3.4 Substrate Ramp Simulation

The epitaxial layers shown in Figure 2.4 were simulated using Sentaurus TCAD to interpret the experimental results. The model assumes a CGaN carbon concentration of 2×10^{18} cm^{-3}, 6×10^{18} cm^{-3} and 1 x 10^{19}cm^{-3} representing Wafer A, Wafer B and Wafer C, respectively. The parameters used in this model have been discussed in the previous chapters.

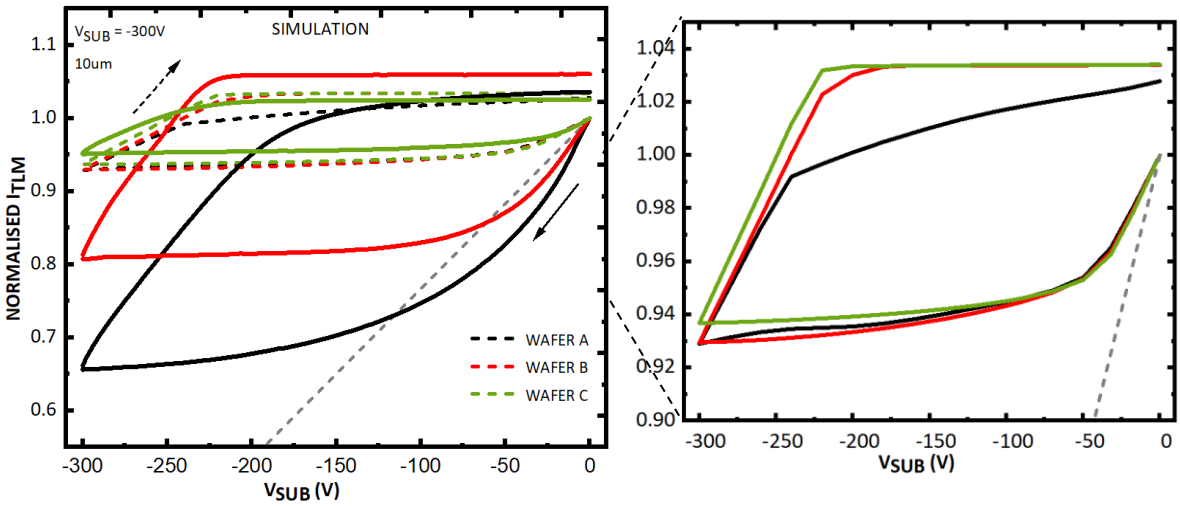

Figure 3-9 - Simulated substrate ramps for Wafers A, B and C, compared with experimental measurements at a ramp rate of 10 V/s. The black, red and green lines correspond to Wafers A, Wafer B and Wafer C, respectively, while the small, dashed lines indicate their simulated counterparts. The solid black arrow denotes the forward sweep (0 V to -300 V), and the dashed black arrow represents the return sweep (-300 V to 0 V).

Figure 3.9 compares the simulated and experimental substrate ramp curves for all three samples. The simulations have partially captured the qualitative trends observed in the experimental measurements. Notably, both exhibit hysteresis, a key characteristic of charge trapping and detrapping dynamics, confirming that trapping occurs in both structures, even though with more pronounced hysteresis in the experimental curves.

In the voltage range of 0 V to -50 V, the simulated substrate ramp curves are positioned to the left of the capacitive coupling line, whereas in the experimental curves, the currents deviate further below this line. This reduction in current is attributed to charge redistribution occurring at varying capture rates across the experimental wafers. In contrast, the simulated curves largely overlap, suggesting a similar degree of charge redistribution. The saturation behaviour is also reflected in the simulations, with Wafer C reaching saturation earlier than Wafer B. However, Wafer A exhibits an intermediate response overall.

Figure 3.10 (a) – (d) compare the simulated conduction band energy, vertical electric field at the UID/CGaN interface, hole density, and space charge region at the UID/CGaN and CGaN/SRL interfaces for Wafers A, B and C at V_{SUB} = -300 V. This voltage corresponds to the plateau region at -300 V in the substrate ramp graph (Figure 3.9).

At V_{SUB} = −300 V, all wafers exhibit the expected upward band bending. However, Wafer A shows more pronounced band bending compared to Wafer C, indicating that a higher carbon concentration in the CGaN layer results in reduced band bending, as shown in Figure 3.10 (a) [47].

Figure 3.10(b) presents the corresponding vertical electric field distribution at the space charge region at the UID/CGaN interface, which aligns well with Figure 3.10(e). During charge redistribution, the negatively charged ionised acceptors accumulate at the top of the CGaN layer, while the positively charged ionised donors accumulate at the bottom of the CGaN layer [21] [5]. The relationship between carbon concentration, depletion width, and the space charge region at the UID/CGaN interface can be understood using the PN junction. In a weakly p-type material, the ionised acceptor density is inversely proportional to the depletion width. As the carbon concentration increases, the depletion width decreases, confining the negatively charged acceptors into a smaller spatial region. Upon completion of the substrate ramp at -300 V, the peak electric field across all three wafers appears similar. However, as seen in Figure 3.10(b), Wafer A exhibits a broader electric field distribution over a larger depletion region, whereas in Wafer C, the peak electric field is confined to a much narrower depletion region due to its higher carbon doping.

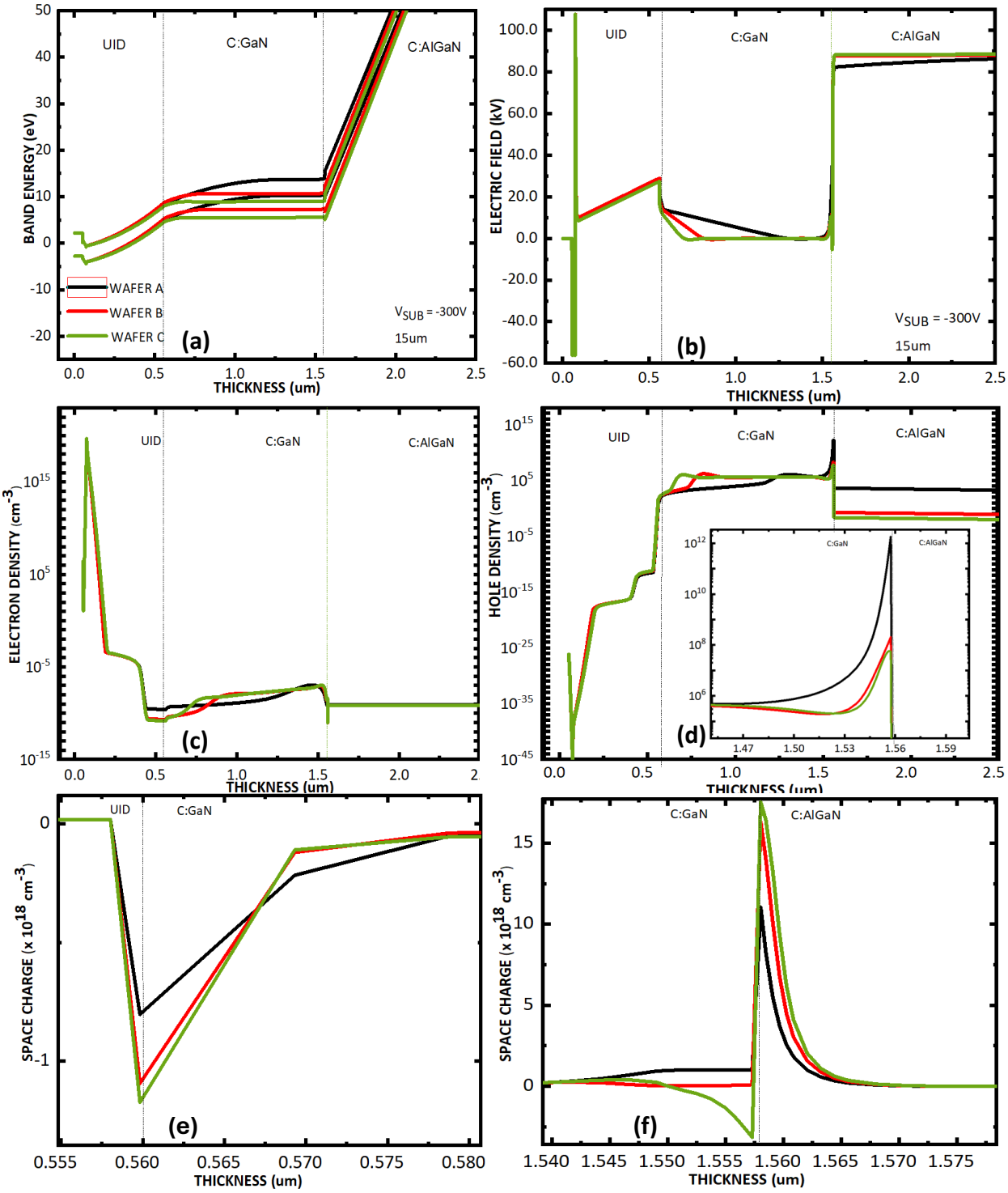

Figure 3-10 - Comparison between the simulated (a) conduction band energy (b) electric field at the UID/CGaN heterojunction (c) hole density (d) the space charge region at the at the UID/CGaN heterojunction and (e) the space charge region at the CGaN/SRL heterojunction of Wafer A, Wafer B and Wafer C, at V_{SUB} = -300 V.

Similarly, Figure 3.10(f) illustrates the P/P++ depletion region at the CGaN/C:AlGaN interface, where Wafer C exhibits a higher density of ionised donors in the CGaN layer bottom compared to the other wafers. Figure 3.10(d) shows the hole density as a function

of stack thickness, highlighting hole accumulation at the CGaN/C:AlGaN heterojunction. Wafer A exhibits the highest hole density, while Wafer C shows the lowest. Figure 3.10(c) indicates that the Wafer C 2DEG density is greater than the other two wafers.

The underlying mechanism behind the positive charge accumulation observed in Figure 3.9 can be further elaborated as follows:

Observed positive charge storage at −300V occurs only if the UID layer resistivity is lower than that of the CGaN, allowing electrons to leak into the 2DEG. This leakage process simultaneously leads to hole accumulation, which is then swept towards the bottom of the CGaN layer [5] [4]. As seen in Figure 3.10(b), this behaviour is well accounted for in the model, where the UID electric field of Wafer C is the lowest among the three wafers. This reduction in the electric field at the UID region is attributed to the electron leaking into the 2DEG.

The electric field distribution at the top of the CGaN layer indicates that the peak electric field remains similar for all three wafers. However, in theory, an increase in ionised acceptor density leads to a reduction in the depletion width, which in turn should result in a higher peak electric field. Meaning, for Wafer C, the electric field is lower than expected. This suggests that the accumulated positive charge storage influences the field distribution at the top of the CGaN as well as the UID region.

The electric field distribution at the top of the CGaN layer indicates that the peak electric field remains similar for all three wafers. However, theoretically, an increase in ionised acceptor density should lead to a reduction in depletion width, which in turn should result in a higher peak electric field. This means that for Wafer C, the peak electric field is lower than expected. This suggests that the accumulated positive charge storage influences the electric field distribution at the top of the CGaN layer as well as in the UID region. The additional positive charge effectively screens the 2DEG from the applied negative V_{SUB}, altering the expected field profile.

As shown in Figure 3.10(d), Wafer C, which exhibits the highest positive charge storage, shows the lowest hole density. However, at the P/P++ region at the CGaN/C:AlGaN interface, a much higher density of ionised donors can be observed. This implies that these positive charges also screen the applied negative substrate bias, further reducing the effective electric field observed in the structure.

Figure 3.11 presents the simulated TLM gap spacings ranging from 5 μm to 25 μm for Wafer A, Wafer B, and Wafer C. The simulated substrate ramps for the TLM gaps of the

three wafers reveal a pronounced gap-dependent hysteresis, which becomes increasingly dominant as the carbon concentration rises. This also suggests that larger gap spacings exhibit more significant hysteresis effects. In contrast, the experimental results shown in Figure 3.6 indicate that gap dependency is somewhat suppressed as the carbon concentration increases.

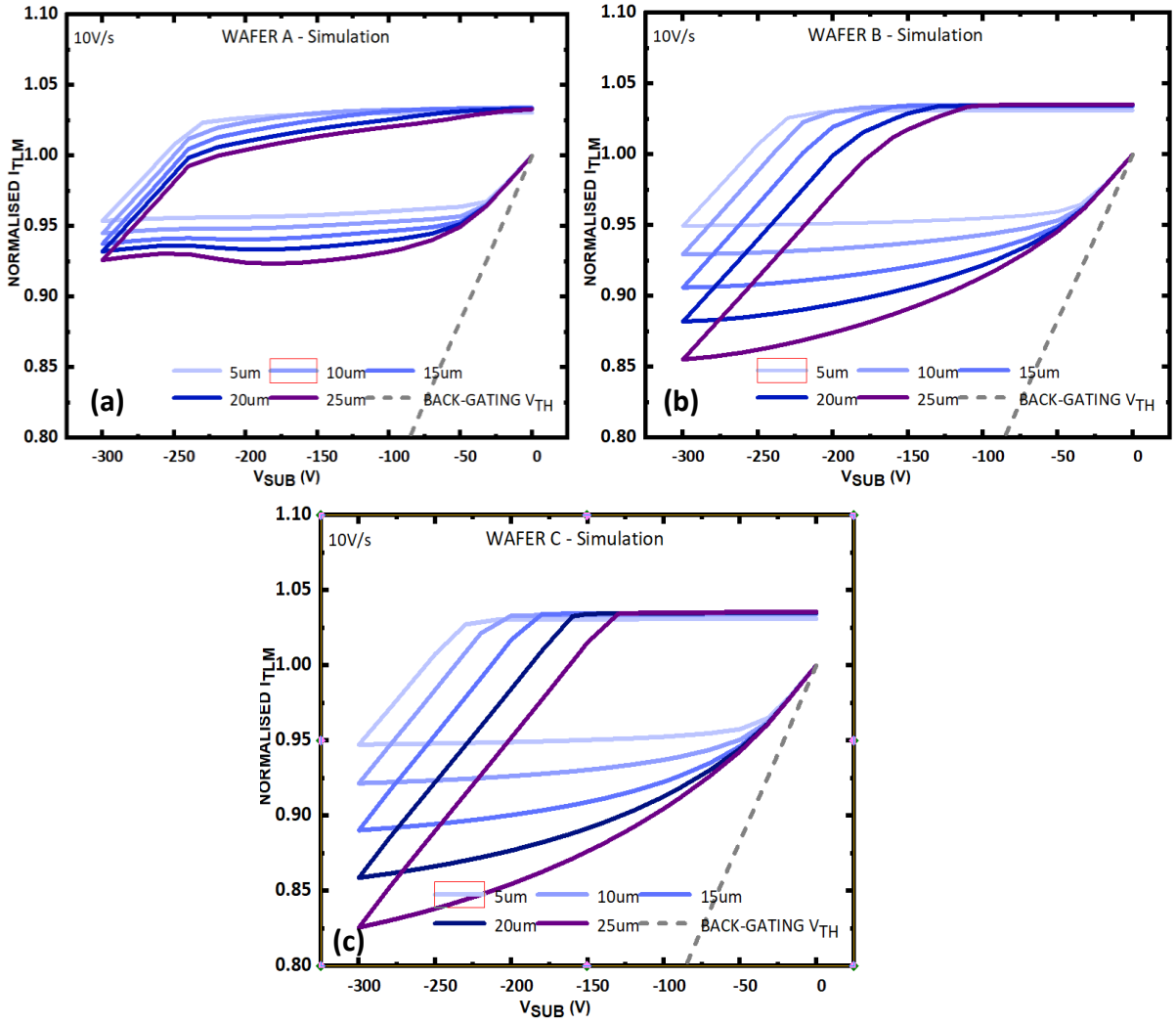

Figure 3-11 - Simulated substrate ramp bi-directional curves at a ramp rate of 10 V/s. The plots depict the normalised channel conductivity for TLM gap spacings of 5 µm to 25 µm for (a) wafer A, (b) wafer B, and (c) wafer C. All samples exhibit gap dependency behaviour. The drain current I_D is normalised to its value at V_{SUB} = 0V.

Additional distinctions observed in Figure 3.6(a) include the deviation of channel currents further below the capacitive coupling line at low V_{SUB} as the gap spacing increases. Meanwhile, in Figure 3.6(c), where Wafer C exhibits much weaker gap dependency, the currents during the charge redistribution phase remain above the capacitive coupling line. Conversely, in the simulations, the decreasing curves during the

charge redistribution phase for all wafers are positioned to the left of the capacitive coupling line.

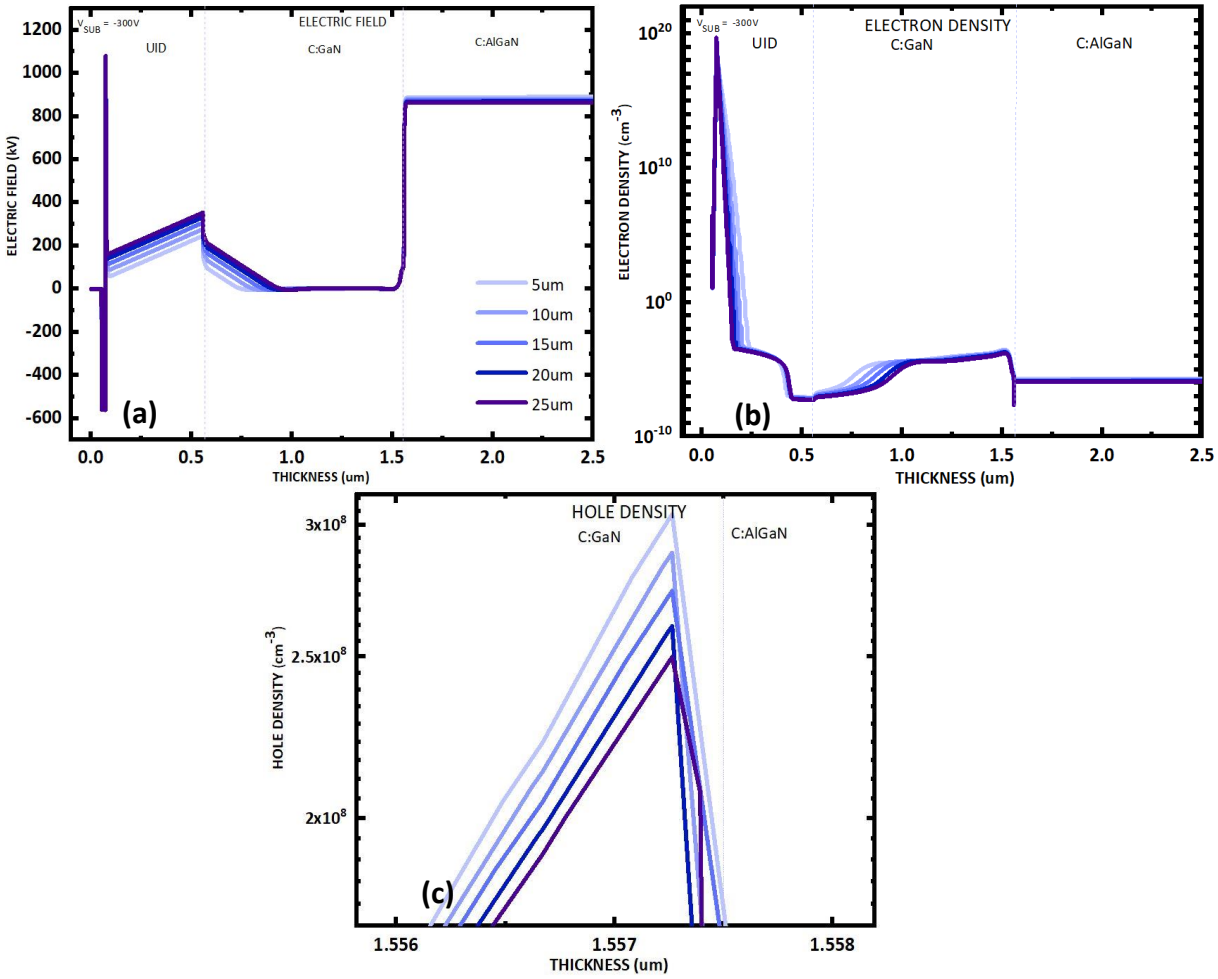

Figure 3-12 - TCAD simulation results demonstrating the gap dependency at the ramp rate of 10V/s. Cutline long x = 2.5µm at V_{SUB} = -300V. (a) Electric field (b) electron density (c) hole density of the TLM gap spacing 5 µm-25 µm during the phase where we observe the current saturation

As discussed in Chapter 2, the simulation does not account for vertical leakage along conducting dislocations across the entire ohmic contact gap spacing. To address this, P++ shorts are placed beneath the ohmic contacts to simulate the dislocation path, providing a leakage pathway between the 2DEG and the CGaN. These P++ shorts not only facilitate the vertical leakage but also contribute to lateral hole conduction within the structure [5] [10]. As a result, the gap dependency observed in Figure 3.12 remains unavoidable for all three simulated wafers.

Figure 3.12(a) presents the peak electric field distribution at a position 2.5 µm away from the left ohmic contact for gap spacings ranging from 5 µm to 25 µm. As the gap between the ohmic contacts increases, the electric field also increases. The depletion

region, which is well represented by the electric field profile, is observed to be wider for larger gap spacings and narrower for smaller gap spacings.

This suggests that the depletion region extends laterally between the ohmic contacts, with its width being influenced by the gap spacing. Since doping concentrations remain constant across all gap spacings, the observation that a larger depletion region corresponds to a larger gap spacing implies that the UID region is more depleted, leading to a higher lateral resistivity. This increase in lateral resistivity results in electric field redistribution.

For charge transport, the UID region must have a lower resistivity than the CGaN to allow electron leakage into the 2DEG, thereby enabling hole accumulation at the bottom of the CGaN layer. As seen in Figure 3.13(c), the 5 μm gap exhibits the highest hole density, which corresponds to a smaller depletion region, lower UID electric field, and lower resistivity, allowing more electrons to leak into the 2DEG.

3.5 Discussion

Carbon incorporation in GaN is known to affect its electrical properties by interacting with the lattice, potentially introducing non-radiative defects. Many studies suggest that carbon degrades crystal quality [35] [48] [49] [50]. Kaneko et al. [3], for instance, reported that carbon incorporation can deteriorate crystal quality while promoting leakage paths. However, the findings of this study present a contrasting trend, challenging the widely accepted view that carbon invariably degrades crystal quality. XRD results show a gradual decrease in FWHM with increasing carbon concentration, with TDD values of 1.827×10^{10} cm^{-2}, 7.24×10^{9} cm^{-2}, and 6.88×10^{9} cm^{-2} for wafers A, B, and C, respectively, indicating an improvement in crystal quality, consistent with previous observations [8] and [19]. Richter et al. [8] observed no significant change in lattice constants with carbon doping, supporting this notion. If carbon introduces tensile strain, the lattice constant should increase, while compressive strain would reduce it. Meaning the unchanged lattice constant across the entire carbon doping range suggests minimal or no strain in this case.

Despite the pronounced edge dislocation density observed in all samples, as illustrated in Figure 3.2(d), the presence of dislocation bunching is also evident (to be discussed in more detail in the next chapter). This suggests that the improvement in crystal quality may, at least in part, be attributed to this phenomenon, consistent with the findings of Barchuk et al. [39] [51], who reported that dislocation bunching effectively reduces the number of dislocations. However, as a TEM image is only available for Wafer C, additional TEM analysis would be required to evaluate the impact of carbon on dislocation bunching in Wafers A and B. Nevertheless, based on the observed screw and edge dislocation densities, it may be speculated that the bunching effect increases with greater carbon incorporation.

In this thesis, strain refers to localised deformation within a material, confined to specific areas, and caused by factors such as lattice distortions from impurities or defects. In contrast, residual stress in this thesis is defined as a more uniform, large-scale effect that remains within the entire epitaxial layer after growth. It arises due to various factors, including thermal expansion mismatch between GaN and the substrate, affecting the entire epitaxy as a whole [39] [52] [53]. The strain field refers to the region surrounding the dislocation. These terms will be frequently used throughout this thesis.

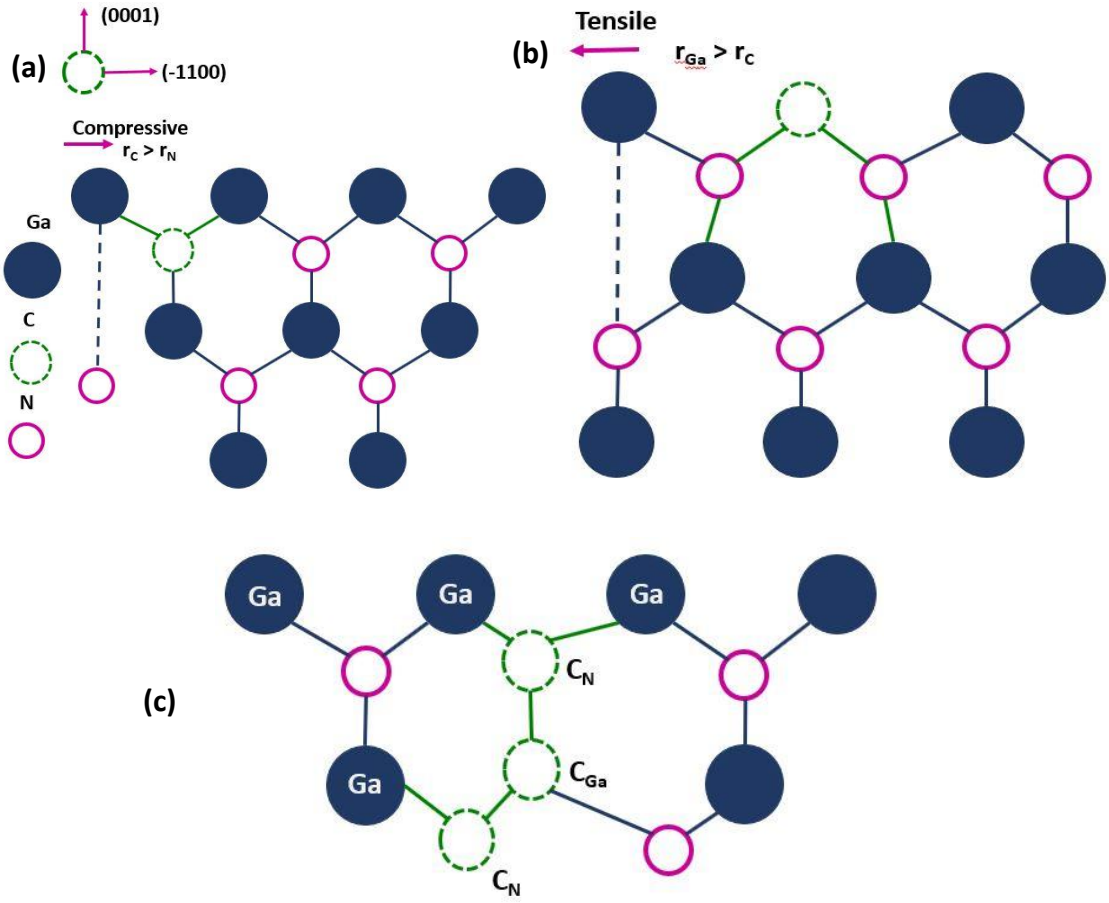

Figure 3-13 - the strain stress generation of due to the incorporation of [C] atoms (a) A carbon atom replacing the [N] atom indicating the compressive strain (b) carbon atom replacing the Ga atom indicating the tensile strain (c) atomic configuration of the axial type tri-carbon defect C_N-C_{Ga}-C_N

Carbon incorporation in the CGaN layer is governed by formation energy, which determines the types of defects that are most likely to form. A defect or defect complex with a lower formation energy is more energetically favourable and, therefore, exists in higher concentrations. At low carbon concentrations, such as in Wafer A, the formation energies of both C_N (carbon substituting nitrogen) and C_{Ga} (carbon substituting gallium) are relatively high, meaning that single-carbon defects such as C_N and C_{Ga} dominate [9] [17] [54]. Carbon incorporation also affects strain within the CGaN layer. C_N introduces compressive strain (−ε) due to its carbon's larger atomic radius (Figure 3.13(a)). In contrast, C_{Ga} can introduce tensile strain (+ε) (Figure 3.13(a)).

Conversely, at higher carbon concentrations, the formation energies of these defects decrease, promoting the incorporation of more complex defect structures, such as tri-carbon defects [1] [9]. These defects form due to Coulomb interactions between oppositely charged defects, where C_N acts as an acceptor and C_{Ga} as a donor, leading to the clustering of these defects in a nearest-neighbour configuration [55] [56]. At high carbon

concentrations, where carbon atoms are abundant, these tri-carbon defects become more prevalent. The inward relaxation of C_N atoms around C_{Ga} helps counterbalance tensile strain within the CGaN layer, potentially mitigating the residual stress in the material.

Residual stress in epitaxy exhibits a monotonic relationship with threading dislocations, meaning that as the density of threading dislocations increases, residual stress also increases [39]. However, this increase in residual stress is also influenced by uncompensated strain fields. As previously discussed, tri-carbon defects provide significant strain field compensation compared to single-carbon defects. Therefore, it can be speculated that increasing carbon incorporation in the CGaN layer may help balance compressive strain, thereby improving crystal quality [50]. In highly carbon-doped GaN, where the strain fields of carbon defects play a critical role, controlling strain through carbon incorporation could reduce threading dislocations, enhancing both structural and electrical properties.

Focusing back on the substrate ramps, a comparison between Wafer A, Wafer B, and Wafer C (Figure 3.3(a)) reveals that during the charge redistribution phase, the normalised channel currents deviate below the capacitive coupling line as the carbon concentration decreases. In other words, transconductance increases as carbon concentration decreases. This indicates that the displacement currents in the CGaN layer of Wafer A are significantly higher than those in Wafer B, which, in turn, are higher than those in Wafer C. Moreover, the displacement currents in Wafer A exceed the corresponding leakage currents in the CGaN layer. This suggests that Wafer A exhibits the highest charge redistribution, followed by Wafer B, with Wafer C showing the lowest redistribution. As explained in Chapter 2, during this phase, the resistivity of the CGaN layer is lower than that of the UID layer [4]. However, based on the observed trend, it can be speculated that the resistivity of the CGaN layer increases with rising carbon concentration, thereby limiting charge redistribution.

During the forward sweep, the highest positive charge storage is observed in Wafer C, followed by Wafer B, and finally Wafer A. Wafer C reaches current saturation at a much lower V_{SUB} of -25 V, compared to -60 V for Wafer B and -100 V for Wafer A. As illustrated in Figure 3.6(c), Wafer C exhibits a pronounced vertical leakage across the ohmic gap spacing, in contrast to Wafer B and Wafer A [21] [57].

As shown in Table 3.1, the dislocation density decreases with increasing carbon concentration. However, the prominent vertical leakage path observed across the entire

ohmic gap spacing is likely enhanced by segregated carbon or tri-carbon defects decorating the threading dislocations (TDs), rather than being solely attributed to the number of dislocations themselves [16] [58] [59]. In other words, Wafer A, with fewer carbon atoms segregating at closely spaced dislocations, may exhibit less dominant vertical leakage, with charge preferentially following the less resistive lateral path, which correlates with the lowest positive charge storage. Wafer B showed an intermediate behaviour.

Figure 3.5 presents substrate ramp measurements up to V_{SUB} = −550 V, highlighting the effects of high-voltage exposure. The plateau region ends first for Wafer C at -400 V, followed by Wafer B at -450 V, and finally Wafer A at -550 V. The reduction in channel currents is attributed to electron injection from the substrate [60] [61].

As shown in the simulation in Figure 3.10(e), at -300 V, the depletion region in Wafer C during the saturation phase, exhibits a higher ionised acceptor density compared to Wafer B and Wafer A. This suggests that during the charge redistribution phase, ionisation might have occurred most rapidly in Wafer C, at a moderate rate in Wafer B, and slowest in Wafer A. Conversely, the P/P++ junction depletion region in Figure 3.10(f) illustrates a higher density of ionised donors, indicating that in Wafer C, these ionised donors have already screened the negative electric field. As a result, they no longer contribute to further screening, leading to the early reduction of channel current at -400 V. In contrast, in Wafer B and Wafer A, the ionisation process continues at higher voltages, meaning that donors are ionising more gradually, alongside ongoing band-to-band leakage. This allows the positively charged donors to progressively screen the electric field, as carbon donor atoms continue ionising. Consequently, in Wafer B and Wafer A, screening occurs more gradually, delaying electron injection from the substrate and pushing the saturation point to higher voltages.

A comparison of substrate ramp measurements between the three wafers was conducted using ring-shaped structures, as illustrated in Figure 3.3(b). Interestingly, all three wafers exhibit nearly identical trends for both TLM (10 µm) and ring-shaped structures, with one key exception: in the ring-shaped structures, the normalised channel currents follow the capacitive coupling line, indicating near-ideal capacitive behaviour before current saturation [5] [57]. As discussed earlier in this chapter, these structures primarily exhibit 1D vertical conduction, with lateral current flow being relatively insignificant. Given that the gap spacing between the ohmic contacts in both the TLM and S10 ring structures is 10 µm, and both are subjected to the same biasing conditions, the observed behaviour suggests that the hypothesis of dominant vertical conduction holds

across all three wafers. However, while lateral conduction may be present, its contribution appears minimal in this configuration.

Figure 3.6 shows that Wafer A exhibits strong gap dependency, whereas Wafer C displays weaker gap dependency, indicating a correlation between decreasing carbon concentration and increasing gap dependency. While the simulation captures the electron-hole profile associated with gap dependency, it does not fully reproduce the weakening dependency with increasing carbon. However, the general trend with increasing gap spacing has been discussed.

As suggested by Barchuk et al. [51], at high TDDs, the mean distance between adjacent dislocations decreases, leading to overlapping strain fields and partial compensation. Partial compensation refers to the phenomenon where the strain fields of closely spaced dislocations or impurity-induced defects interact and cancel each other out, reducing the overall lattice distortion in localised regions. This effect is particularly pronounced in Wafer A, where a high density of non-interacting TDs and carbon-related defects (C_N and C_{Ga}) introduces localised strain. When these strain fields overlap, they minimise strain variations in the CGaN layer, creating locally more uniform lattice regions. However, this does not necessarily improve the overall crystal quality or reduce residual stress. Additionally, impurity-induced strain fields from C_N and C_{Ga} may further contribute to partial compensation, leading to a reduction in carrier scattering. Lower scattering results in decreased resistivity, forming a more conductive lateral path in the CGaN layer.

This increased interaction of strain fields in Wafer A could explain its enhanced lateral leakage. In contrast, Wafer B and Wafer C, with lower TDDs and greater mean dislocation spacing, experience less strain compensation, resulting in higher resistivity and reduced lateral leakage.

How efficiently an epitaxial layer can discharge trapped charge and suppress dynamic R_{ON} is a crucial factor in determining the most suitable dopants, as well as the optimal doping concentrations for insulating the buffer. This was evaluated using substrate transient measurements (Figure 3.7), where Wafer C exhibited the fastest recovery, followed by Wafer B, and then Wafer A, with time constants of 73.13 s, 140.16 s, and 206.5 s, respectively. The differences in these time constants may be attributed to the preferred leakage paths. In Wafer C, the vertical leakage path across the contact spacing appears to be dominant due to the increased carbon decoration of dislocation cores, allowing electrons to return to the CGaN layer and neutralise the accumulated positive charge

more rapidly. This also explains why the longest recovery time was observed in Wafer A, despite the lowest positive charge storage, where the dominant lateral leakage path along the dislocations beneath the contacts results in a slower discharge process.

Overall, these findings indicate that carbon incorporation and dislocation interactions play a key role in shaping the leakage characteristics of the buffer layer. Higher carbon concentrations promote vertical leakage by modifying dislocation structures, while lower carbon concentrations and high dislocation densities favour lateral conduction pathways, leading to slower charge neutralisation.

3.6 Conclusion

This study provides new insights into the impact of V_{SUB} on the characteristics of the CGaN buffer in lateral HEMTs, challenging the conventional belief that carbon incorporation degrades crystal quality. Unlike previous reports, our findings demonstrate that increasing carbon concentration correlates with improved structural properties, as evidenced by reductions in FWHM and threading dislocation density (TDD) across the studied wafers. Notably, edge dislocation density was found to be greater than screw dislocation density, with high carbon concentration suppressing edge dislocation formation and enhancing crystal quality. This phenomenon is likely due to the increasing presence of tri-carbon defects alleviating overall strain.

The impact of carbon incorporation on the dynamic buffer properties was investigated using substrate ramp and transient measurements. Specifically, the study examined how carbon doping concentration in the CGaN layer influences dynamic R_{ON} across two distinct voltage regimes: a low substrate bias of -300 V and a higher bias of -550 V. Understanding carrier transport at -550 V is particularly crucial, as it approaches the nominal breakdown voltage of 600 V for the epitaxy used in this study.

- Wafer C, with the highest carbon concentration (1×10^{19} cm^{-3}), exhibited the highest positive charge storage, whereas Wafer A (2×10^{18} cm^{-3}) showed the lowest. This suggests that increasing carbon doping concentration induces a dominant vertical leakage path extending across the UID/CGaN layers, promoting weak gap-dependent behaviour, whereas in Wafer A, lateral leakage currents were more prominent.

- The effectiveness of vertical leakage is determined by how dislocation cores are decorated with segregated carbon impurities. While this hypothesis is plausible, further experimental validation is needed to confirm the underlying mechanisms. Ultimately, this suggests that dislocation density alone is not sufficient to modulate the leakage behaviours; carbon impurities also play a crucial role.

- Substrate transient measurements revealed that Wafer C, with the highest carbon concentration, exhibited a swift recovery, whereas Wafer A demonstrated the longest time constant. Wafer B displayed intermediate behaviour. This phenomenon is likely due to variations in the dominant leakage mechanisms present in each wafer.

Overall, this study provides new insights into the role of carbon incorporation in GaN, demonstrating that controlled carbon doping can enhance structural properties, alter charge storage characteristics, and influence leakage behaviour. Furthermore, it has been observed that increasing carbon concentration helps to minimise dynamic R_{ON} when a negative substrate voltage is applied. However, it is essential to carefully control growth parameters during doping incorporation to optimise dynamic R_{ON} performance.

3.7 References

[1] F. Zimmermann, J. Beyer, C. Röder, F. C. Beyer, E. Richter, K. Irmscher and J. Heitmann, “Current Status of Carbon-Related Defect Luminescence in GaN,” Physica status solidi. A, Applications and materials science,, vol. 218, no. 20, p. 2100235, 2021.

[2] S. Y. Karpov, “Gallium Nitride Doping with Carbon: A Thermodynamic Analysis,” Physica Status Solidi (B) Basic Research, vol. 258, no. 6, p. 202100066, 2021.

[3] R. Kaneko, H. Yoshida, A. Yoshioka, T. Hikosaka and S. Nunoue, “Impact of Carbon Doping on Vertical Leakage Current in AlGaN-Based Buffer Layer Grown on Silicon Substrate,” Physica status solidi. A, Applications and materials science, p. 202400035, 2024-04.

[4] M. J. Uren and M. Kuball, “Impact of carbon in the buffer on power switching GaN-on-Si and RF GaN-on-SiC HEMTs,” Japanese Journal of Applied Physics, vol. 60, p. Article SB0802, 2021-05,.

[5] M. J. Uren, S. Karboyan, I. Chatterjee, A. Pooth, P. Moens, A. Banerjee and M. Kuball, “Leaky Dielectric” Model for the Suppression of Dynamic Ron in Carbon-Doped AlGaN/GaN HEMTs,” IEEE transactions on electron devices, vol. 64, no. 7, p. 2826–2834, 2017.

[6] M. Cioni, A. Chini, N. Zagni, G. Verzellesi, G. Giorgino, G. Cappellini, C. Miccoli, G. Toulon, T. Wakrim, M. Eloisa Castagna, A. Constant and F. Iucolano, “On the Dynamic RON, Vertical Leakage and Capacitance Behavior in pGaN HEMTs With Heavily Carbon-Doped Buffers,” IEEE electron device letters, vol. 45, no. 8, pp. 1437-1440, 2024-08.

[7] C. Koller, G. Pobegen, C. Ostermaier and D. Pogany, “Effect of carbon doping on charging/discharging dynamics and leakage behavior of carbon-doped GaN,” IEEE Transactions on Electron Devices, vol. 65, no. 12, pp. 5314-5321, 2018.

[8] E. Richter, F. C. Beyer, F. Zimmermann, G. Gärtner, K. Irmscher, I. Gamov, J. Heitmann, M. Weyers and G. Tränkle, “Growth and Properties of Intentionally Carbon-DopedGaN Layers,” Crystal research and technology (1979), , vol. 55, no. 2, p. 1900129, 2020-02 .

[9] A. Honda, H. Watanabe, W. Takeuchi, Y. Honda, H. Amano and T. Kato, “Investigation of carbon-related complexes in highly C-doped GaN grown by metalorganic vapor phase epitaxy,” Japanese Journal of Applied Physics, vol. 63, no. 4, p. 41005, 2024-04.

[10] M. J. Uren, M. Silvestri, M. Casar, G. A. M. Hurkx, J. A. Croon, J. Sonsky and M. Kuball, “Intentionally Carbon-Doped AlGaN/GaN HEMTs: Necessity for Vertical Leakage Paths,” IEEE electron device letters, vol. 35, no. 3, p. 327–329, 2014.

[11] C. Koller, L. Lymperakis, D. Pogany, G. Pobegen and C. Ostermaier, “Mechanism leading to semi-insulating property of carbon-doped GaN: Analysis of donor acceptor ratio and method for its determination,” Journal of Applied Physics, vol. 130, no. 1, 2021.

[12] Z. F. Scales, C. Koller, L. Lymperakis, M. Nelhiebel and M. Stoeger-Pollach, “The role of carbon segregation in the electrical activity of dislocations in carbon doped GaN,” Journal of applied physics, vol. 136, no. 4, p. 045704, 2024-07.

[13] I. Gamov, E. Richter, M. Weyers, G. Gärtner and K. Irmscher, “Carbon doping of GaN: Proof of the formation of electrically active tri-carbon defects,” Journal of applied physics, vol. 127 , no. 20, 2020-05.

[14] A. Armstrong, A. R. Arehart, D. Green, U. K. Mishra, J. S. Speck and S. A. Ringel, “Impact of deep levels on the electrical conductivity and luminescence of gallium nitride codoped with carbon and silicon,” Journal of applied physics, vol. 98, no. 5, p. 053704, 2005-09.

[15] T. Tanaka, N. Kaneda, T. Mishima, Y. Kihara, T. Aoki and K. Shiojima, “Roles of lightly doped carbon in the drift layers of vertical n-GaN Schottky diode structures on freestanding GaN substrates,” Japanese Journal of Applied Physics, vol. 54 , no. 4, pp. 41002-1-041002-7, 2015-04.

[16] P. Bogusławski and J. Bernholc, “Doping properties of amphoteric C, Si, and Ge impurities in GaN and AlN,” Acta physica Polonica, vol. 90, no. 4, pp. 735-738, 1996-10,.

[17] M. Matsubara and E. Bellotti, “A first-principles study of carbon-related energy levels in GaN. II. Complexes formed by carbon and hydrogen, silicon or oxygen,” Journal of applied physics, vol. 121, no. 19, p. 195702, 2017-05.

[18] J. L. Lyons, A. Janotti and C. G. Van de Walle, “ Carbon impurities and the yellow luminescence in GaN,” Applied physics letters, vol. 97, no. 15, pp. 152108-152108-3, 2010.

[19] A. Lesnik, M. P. Hoffmann, A. Fariza, J. Bläsing, H. Witte, P. Veit, F. Hörich, C. Berger, J. Hennig, A. Dadgar and A. Strittmatter, “Properties of C-doped GaN,” Physica Status Solidi (B) Basic Research, vol. 254, no. 8, 2017.

[20] Z. Shen, X. Yang, S. Wu, H. Huang, X. Yan, N. Tang, F. Xu, X. Wang, W. Ge, B. Huang and B. Shen, “Mechanism for self-compensation in heavily carbon doped GaN,” AIP advances, vol. 13, no. 3, pp. 035026-035026-5, 2023-03.

[21] F. Wach, M. J. Uren, B. Bakeroot, M. Zhao, S. Decoutere and M. Kuball, “Low Field Vertical Charge Transport in the Channel and Buffer Layers of GaN-on-Si High Electron Mobility Transistors,” IEEE Electron Device Letter, vol. 41, no. 12, p. 1754–1757, 2020.

[22] J. W. Hsu, M. J. Manfra, R. J. Molnar, B. Heying and J. S. Speck, “Direct imaging of reverse-bias leakage through pure screw dislocations in GaN films grown by molecular beam epitaxy on GaN templates,” Applied physics letters, vol. 81, no. 1, pp. 79-81, 2002-07.

[23] C. Zhou, Q. Jiang, S. Huang and K. J. Chen, “Vertical Leakage/Breakdown Mechanisms in AlGaN/GaN-on-Si Devices,” IEEE electron device letters, vol. 33, no. 8, p. 1132–1134, 2012.

[24] M. Marso, M. Wolter, P. Javorka, P. Kordoš and H. Lüth, “Investigation of buffer traps in an AlGaN/GaN/Si high electron mobility transistor by backgating current deep level transient spectroscopy,” Applied physics letters, vol. 82, no. 4, p. 633–635, 2003.

[25] M. J. Uren, M. Cäsar, M. A. Gajda and M. Kuball, “Buffer transport mechanisms in intentionally carbon doped GaN heterojunction field effect transistors,” Applied physics letters, vol. 104, no. 26, pp. 1077-3118, 2014.

[26] S. Yang, C. Zhou, S. Han, J. Wei, K. Sheng and K. J. Chen, “Impact of substrate bias polarity on buffer-related current collapse in AlGaN/GaN-on-Si power devices,” IEEE Transactions on Electron Devices, vol. 64, no. 12, pp. 5048-5056, 2017.

[27] D. Bisi, M. Meneghini, C. de Santi, A. Chini, M. Dammann, P. Bruckner, M. Mikulla, G. Meneghesso and E. Zanoni, “Deep-Level Characterization in GaN HEMTs-Part I: Advantages and Limitations of Drain Current Transient Measurements,” IEEE transactions on electron devices, vol. 60, no. 10, pp. 3166-3175, 2013-10.

[28] J. Bai, T. Wang, P. Parbrook, K. Lee and A. Cullis, “A study of dislocations in AlN and GaN films grown on sapphire substrates,” Journal of crystal growth, vol. 282, no. 3-4, pp. 290-296, 2005.

[29] A. Hierro, M. Hansen, L. Zhao, J. Speck, U. Mishra, S. DenBaars and S. Ringel, “Carrier Trapping and Recombination at Point Defects and Dislocations in MOCVD n-GaN,” Physica Status Solidi (B) Basic Research, vol. 228, no. 3, pp. 937-946, 2001-12.

[30] M. A. Moram and M. E. Vickers, “X-ray diffraction of III-nitrides,” Reports on progress in physics, vol. 72, no. 3, pp. 036502-036502, 2009-03.

[31] H. Heinke, V. Kirchner, S. Einfeldt and D. Hommel, “X-ray diffraction analysis of the defect structure in epitaxial GaN,” Applied physics letters, vol. 77, no. 14, pp. 2145-2147, 2000-10.

[32] L. Liu and J. Edgar, “Substrates for gallium nitride epitaxy,” Materials science & engineering. R, Reports : a review journa, vol. 37, no. 3, p. 61–127, 2002.

[33] Y. C. Weng, M. Y. Hsiao, C. H. Lin, Y. P. Lan and E. Y. Chang, “Effect of High-Pressure GaN Nucleation Layer on the Performance of AlGaN/GaN HEMTs on Si Substrate,” Materials, vol. 16, no. 9, p. 3376, 2023.

[34] G. Jiang, Y. Lv, Z. Lin, Y. Liu, M. Wang and H. Zhou, “The relationship between AlGaN barrier layer thickness and polarization Coulomb field scattering in AlGaN/GaN heterostructure field-effect transistors,” Superlattices and microstructures, vol. 156, p. 106987, 2021-08.

[35] J. Zhang, Q. Wu, Z. Luo, M. Zhang and Y. Liu, “Alleviation of the on-state dynamic conductance decline in a GaN high electron mobility transistor with heavy carbon doping,” Japanese Journal of Applied Physics, vol. 63, no. 4, p. 44002, 2024-04.

[36] X. Li, J. Bergsten, D. Nilsson, O. Danielsson, H. Pedersen, N. Rorsman, E. Janzén and U. Forsberg, “Carbon doped GaN buffer layer using propane for high electron mobility transistor applications: Growth and device results,” Applied physics letters, vol. 107, no. 26, p. 262105, 2015.

[37] J. Su, N. Posthuma, D. Wellekens, Y. N. Saripalli, S. Decoutere, R. Arif and G. D. Papasouliotis, “Growth and Implementation of Carbon-Doped AlGaN Layers for Enhancement-Mode HEMTs on 200 mm Si Substrates,” Journal of electronic materials, vol. 45, no. 12, p. 6346–6354, 2016.

[38] R. A. Oliver, M. J. Kappers, J. Sumner, R. Datta and C. J. Humphreys, “Highlighting threading dislocations in MOVPE-grown GaN using an in situ treatment with SiH4 and NH3,” Journal of crystal growth, vol. 289, no. 2, p. 506–514, 2005.

[39] M. Barchuk, C. Röder, Y. Shashev, G. Lukin, M. Motylenko, J. Kortus, O. Pätzold and D. Rafaja, “Correlation between the residual stress and the density of threading dislocations in GaN layers grown by hydride vapor phase epitaxy,” Journal of crystal growth, vol. 386, no. 2014-01, p. 1–8, 2014.

[40] A. Nardo, C. De Santi, C. Koller, C. Ostermaier, I. Daumiller, G. Meneghesso, E. Zanoni and M. Meneghini, “Positive and negative charge trapping GaN HEMTs: Interplay between thermal emission and transport-limited processes,” Microelectronics Reliablity, vol. 126, p. 114255, 2021.

[41] D. Bisi, M. Meneghini, C. de Santi, A. Chini, M. Dammann, P. Bruckner, M. Mikulla, G. Meneghesso and E. Zanoni, “Deep-Level Characterization in GaN HEMTs-Part I: Advantages and Limitations of Drain Current Transient Measurements,” IEEE transactions on electron devices, vol. 60, no. 10, pp. 3166-3175, 2013-10.

[42] M. Singh, M. J. Uren, T. Martin, S. Karboyan, H. Chandrasekar and M. Kuball, ""Kink" in AlGaN/GaN-HEMTs: floating buffer model," IEEE Transactions on Electron Devices, vol. 65, no. 9, pp. 3746-3753, 2018.

[43] B. Rackauskas, M. J. Uren, S. Stoffels, M. Zhao, S. Decoutere and M. Kuball, "Determination of the Self-Compensation Ratio of Carbon in AlGaN for HEMTs," IEEE transactions on electron devices, vol. 65, no. 5, p. 1838–1842, 2018.

[44] W. Cao, C. Song, H. Liao, N. Yang, R. Wang, G. Tang and H. Ji, "Numerical simulation analysis of carbon defects in the buffer on vertical leakage and breakdown of GaN on silicon epitaxial layers," Scientific reports, vol. 13, no. 1, pp. 14820-14820, 2023.

[45] M. Singh, M. J. Uren, T. Martin, S. Karboyan, H. Chandrasekar and M. Kuball, "Kink' in AlGaN/GaN-HEMTs: Floating Buffer Model," IEEE transactions on electron devices, vol. 65, no. 9, p. 3746–3753, 2018.

[46] M. J. Uren, J. Moreke and M. Kuball, "Buffer Design to Minimize Current Collapse in GaN/AlGaN HFETs," IEEE transactions on electron devices, vol. 59 , no. 12, pp. 3327-3333, 2012.

[47] M. Millesimo, M. Borga, L. Valentini, B. Bakeroot, N. Posthuma, A. Vohra, S. Decoutere, C. Fiegna and A. N. Tallarico, " Role of the GaN-on-Si Epi-Stack on Δ R ON Caused by Back-Gating Stress," IEEE transactions on electron devices, vol. 70, no. 10, pp. 5203-5209, 2023-10.

[48] H. Yacoub, T. Zweipfennig, G. Lukens, H. Behmenburg, D. Fahle, M. Eickelkamp, M. Heuken, H. Kalisch and A. Vescan, "Effect of Carbon Doping Level on Static and Dynamic Properties of AlGaN/GaN Heterostructures Grown on Silicon," IEEE transactions on electron devices, vol. 65, no. 8, p. 3192–3198, 2018.

[49] M. R. Ramdani, M. Chmielowska, Y. Cordier, S. Chenot and F. Semond, "Effect of carbon doping on crystal quality, electrical isolation and electron trapping in GaN based structures grown silicon substrates," Solid-state electronics, vol. 75, p. 86–92, 2012.

[50] Y. Ni, L. Li, L. He, T. Que, Z. Liu, L. He, Z. Wu and Y. Liu, "Dependence of carbon doping concentration on the strain-state and properties of GaN grown on Si substrate," Superlattices and microstructure, vol. 120, p. 720–726, 2018-08.

[51] M. Barchuk, V. Holý and D. Rafaja, "Density of bunched threading dislocations in epitaxial GaN layers as determined using X-ray diffraction," Journal of applied physics , vol. 123, no. 16, p. 161552, 2018.

[52] Y. Zhou, S. Zhou, S. Wan, B. Zou, Y. Feng, R. Mei, H. Wu, N. Shigekawa, J. Liang, P. Tan and M. Kuball, "Tuning the interlayer microstructure and residual stress of

buffer-free direct bonding GaN/Si heterostructures," Applied physics letters, vol. 122, no. 8, p. 082103, 2023-02.

[53] L. Ravikiran, K. Radhakrishnan, N. Dharmarasu, M. Agrawal and S. Munawar Basha, "Strain states of AlN/GaN-stress mitigating layer and their effect on GaN buffer layer grown by ammonia molecular beam epitaxy on 100-mm Si(111)," Journal of applied physics, , vol. 114, no. 12, p. 123503, 2013-09.

[54] K. Irmscher, I. Gamov, E. Nowak, G. Gärtner, F. Zimmermann, F. C. Beyer, E. Richter, M. Weyers and G. Tränkle, "Tri-carbon defects in carbon doped GaN," Applied physics letters, vol. 113, no. 26, 2018.

[55] B. E. Gaddy, Z. Bryan, I. Bryan, J. Xie, R. Dalmau, B. Moody, Y. Kumagai, T. Nagashima, Y. Kubota, T. Kinoshita, A. Koukitu, R. Kirste, Z. Sitar, R. Collazo and D. Irving, "The role of the carbon-silicon complex in eliminating deep ultraviolet absorption in AlN," Applied physics letters, vol. 104, no. 20, p. 202106, 2014-05.

[56] J. Neugebauera and C. Van de Walle, "Gallium vacancies and the yellow luminescence in GaN," Applied physics letters, vol. 69, no. 4, pp. 503-505, 1996-07.

[57] W. M. Waller, M. Gajda, S. Pandey, J. J. T. M. Donkers, D. Calton, J. Croon, J. Sonsky, M. J. Uren and M. Kuball, "Control of Buffer-Induced Current Collapse in AlGaN/GaN HEMTs Using SiNx Deposition," IEEE transactions on electron devices, , Vol.), p., Article 8013764, vol. 64, no. 10, pp. 4044-4049, 2017-10.

[58] A. G. Chynoweth and G. L. Pearson, "Effect of dislocations on breakdown in silicon p-n junctions," Journal of applied physics, vol. 29, no. 7, pp. 1103-1110, 1958-07.

[59] L. Sang, B. Ren, M. Sumiya, M. Liao, Y. Koide, A. Tanaka, Y. Cho, Y. Harada, T. Nabatame, T. Sekiguchi, S. Usami, Y. Honda and H. Amano, "Initial leakage current paths in the vertical-type GaN-on-GaN Schottky barrier diodes," Applied physics letters, vol. 111, no. 12, p. 122102, 2017-09.

[60] I. Chatterjee, M. J. Uren, S. Karboyan, A. Pooth, P. Moens, A. Banerjee and M. Kuball, "Lateral Charge Transport in the Carbon-Doped Buffer in AlGaN/GaN-on-Si HEMTs," IEEE transactions on electron devices, vol. 64, no. 3, p. 977–983, 2017.

[61] I. Chatterjee, M. Uren, A. Pooth, S. Karboyan, S. Martin-Horcajo, M. Kuball, K. Lee, Z. Zaidi, P. Houston, D. Wallis, I. Guiney and C. Humphreys, "Impact of Buffer Charge on the Reliability of Carbon Doped AlGaN/GaN-on-Si HEMTs," in 2016 IEEE INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM (IRPS), Pasadena, USA, 2016.

[62] N. Zagni, A. Chini, F. M. Puglisi, P. Pavan and G. Verzellesi, "Collapse, and Dynamic On-Resistance Recovery in AlGaN/GaN High Electron Mobility Transistors on Semi-Insulating SiC Substrates," Physica status solidi. A, Applications and materials science, , vol. 217, no. 7, p. 1900762, 2020-04.

[63] S. Yang, S. Han, K. Sheng and K. J. Chen, “Dynamic On-Resistance in GaN Power Devices: Mechanisms, Characterizations, and Modeling,” IEEE journal of emerging and selected topics in power electronics, vol. 7, no. 3, pp. 1425-1439, 2019-09.

[64] K. J. Chen, O. Haberlen, A. Lidow, C. L. Tsai, T. Ueda, Y. Uemoto and Y. Wu, “GaN-on-Si Power Technology: Devices and Applications,” IEEE transactions on electron devices, vol. 64, no. 3, pp. 779-795, 2017.

[65] R. Kabouche, I. Abid, R. Püsche, J. Derluyn, S. Degroote, M. Germain, A. Tajalli, M. Meneghini, G. Meneghesso and F. Medjdoub, “Low On-Resistance and Low Trapping Effects in 1200 V Superlattice GaN-on-Silicon Heterostructures,” Physica status solidi. A, Applications and materials science, vol. 217, no. 7, pp. 1900687 1-6, 2020-04.

4. Fine-Tuning Dynamic On-Resistance: Unravelling the Impact of Thickness Variations in Heavily Carbon Doped GaN Layer

4.1 Introduction

As previously discussed, the choice of buffer layer is crucial to device performance, as it significantly influences breakdown voltage (BV) and leakage currents. Particularly in the context of minimising leakage currents and increasing the BV, enhancing buffer resistivity initially appeared to be a promising solution. This has been achieved through intentional doping of the buffer layer with elements such as Fe or carbon as explored extensively in earlier chapters. While carbon doping enhances the BV, a heavily carbon-doped buffer, also referred to as CGaN, can contribute to increased dynamic R_{ON} [1] [2].

A common design strategy in device fabrication is to position the CGaN region farther from the 2DEG to minimise electron trapping in the CGaN. Simulation-based studies by Joshi et al. [2] demonstrated that increasing the thickness of the UID layer improves dynamic R_{ON} and supports excellent transport properties between the UID and CGaN layers. However, increasing the UID thickness significantly deteriorated BV [2]. Additionally, Joshi et al. observed that thinner UID layers exhibit a broader buffer doping concentration range, although this comes at the cost of higher dynamic R_{ON}, compared to devices with thicker UID layers. Similarly, experimental studies by Putcha et al. [3] confirmed this hypothesis, demonstrating that thinner UID layers lead to increased dynamic R_{ON}.

Shanbang et al. [4] further investigated the relationship between UID thickness and carbon doping concentration in CGaN. Contrary to [2] and [3], they concluded that increasing the UID thickness does not significantly impact the carbon doping concentration in the CGaN region. These findings underscore the importance of both tCGaN and UID thickness, as the latter acts as a screening layer, shielding the 2DEG from carbon acceptors and playing a pivotal role in mitigating dynamic R_{ON}.

Recent work by Liu et al. [1] highlighted that dynamic R_{ON} in GaN-on-Si structures can be substantially reduced by increasing buffer thickness. This is attributed to reduced leakage along defect bands formed by carbon doping, as well as overall reductions in leakage currents.

Despite these insights, there are limited studies in the literature addressing the interplay between tCGaN and UID thickness for wafers with the same carbon doping concentration in the CGaN layer. This chapter addresses this gap by investigating the exclusive variation of tCGaN and the simultaneous variation of both UID and CGaN thicknesses. The focus is on their combined impact on trapping effects and dynamic R_{ON}.

This study establishes the relationship between threading dislocations, vertical leakage, and dynamic R_{ON} in the AlGaN/GaN HEMTs. A comparative analysis of structural and electrical characteristics is presented. Simulations from the previous chapter highlighted the role of the off-state electric field in the CGaN buffer, attributed to carbon doping concentration, in supporting vertical leakage mechanisms. Here, the impact of thickness variations on the vertical electric field between the UID and CGaN layers was studied and supported by simulated results.

The correlation between CGaN thickness, dynamic R_{ON}, and BV is delicately balanced. While increasing CGaN thickness may enhance BV, this optimisation does not necessarily guarantee improved dynamic R_{ON} performance. This chapter provides a detailed analysis to inform device design strategies aimed at achieving an optimal balance between these competing parameters.

4.2 Experimental methods

4.2.1 Samples

The samples investigated in this study were fabricated on commercial GaN-on-Si epitaxial wafers provided by NXP Semiconductors, grown via MOCVD. The specific growth conditions for each wafer were not documented, and therefore, possible variations within the series can neither be confirmed nor excluded: however, the growth parameters are assumed to be the same for all wafers unless stated otherwise. However, the manufacturer's specifications indicate a clear trend: as the GaN layer thickness increases, wafer bow also increases. This observation is consistent with the expectation that thicker GaN layers experience greater curvature due to accumulated strain from lattice and thermal expansion mismatch with the silicon substrate [52]. Furthermore, the manufacturer's data also report an increase in HRXRD FWHM values for both the (0002) and (1 0 $\bar{1}$ 2) ω reflections with increasing GaN thickness, suggesting that the structural quality and dislocation densities are influenced alongside the bowing behaviour. Although

the precise impact of these factors on the present study cannot be directly quantified, they are important to bear in mind when interpreting results.

All wafers share nominally identical doping levels and epitaxial structures, as illustrated in Figure 2.14. The epitaxial structure comprises a 140 nm AlN nucleation layer, a 3.3 µm AlN/GaN superlattice SRL, a CGaN layer, a UID GaN layer, a 20 nm AlGaN barrier layer with 20% Al composition, and a 3 nm undoped GaN cap. The carbon doping concentration in the CGaN and SRL layers is $1x10^{19}$ cm^{-3} and $2x10^{19}$ cm^{-3}, respectively.

Two groups of wafers were studied. In Group A, the CGaN thickness tCGaN was varied between 0.5 µm and 1.25 µm, while the UID thickness was fixed at 0.5 µm. For Group B, both the UID and CGaN thicknesses were simultaneously varied, while maintaining the total epitaxial thickness constant at 1.5 µm. Further details regarding the two groups are outlined in Table 4.1 and Table 4.2, respectively.

WAFER	UID thickness	CGaN thickness
A1	0.5 µm	0.5 µm
A2	0.5 µm	0.75 µm
A3 (B2)	0.5 µm	1 µm
A4	0.5 µm	1.25 µm

Table 4.1 - **Group A :** UID GaN and C:GAN Buffer Thickness

WAFER	UID thickness	CGaN thickness
B1	0.25 µm	1.25 µm
B2 (A3)	0.5 µm	1 µm
B3	0.75 µm	0.75 µm
B4	1 µm	0.5 µm
B5	1.25 µm	0.25 µm

Table 4.2 - **Group B:** UID GaN and C:GAN Buffer Thickness

All measurements were conducted on linear ungated TLM structures with spacings ranging from 2 to 25 µm, as detailed in Chapter 2. The width of the ohmic contacts was 100 µm. Mesa isolation was achieved using chlorine-based ICP etching to a depth of approximately 600 nm. Ohmic contacts were deposited with Ti/Al/Ni/Au (20/40/120/25 nm)

and annealed at 775°C in a nitrogen ambient, followed by Ti/Au probe pads. The estimated 2DEG density for all wafers is 5 x 10^{12}cm^{-2}, with a sheet resistance of approximately 710 Ω/square.

4.2.2 Measurement Techniques

To investigate the AlGaN/GaN HEMT structures on Si, various characterisation techniques were employed, including HRXRD, TEM, substrate ramp, and substrate transient measurements.

The crystalline quality was assessed using HRXRD rocking curve measurements, as detailed in Section 2.6.6. TDD, as well as the individual edge and screw dislocation components, were extracted using the FWHM values of the (0002) and (1 0 $\overline{1}$ 2) ω scans, respectively [5] [6] [7]. A TEM analysis was conducted on the Group A wafers to visually analyse the dislocation propagation and distribution within the CGaN buffer and at the CGaN/SL interface.

Substrate ramp and substrate transient measurements were conducted following the same biasing conditions described in Chapter 3 (or as explained in Chapter 2). In this chapter, the focus is specifically on 15 µm structures for comparative analysis. Substrate ramp measurements were performed over both low and high V_{SUB} regimes, while transient measurements included a stress phase followed by a recovery phase to monitor charge dynamics.

All measurements were carried out at RT and in the dark. Multiple identical structures across the sample were tested to account for variations within each wafer. For the final analysis, the average results for 15 µm TLM structures from both substrate ramp and transient measurements were used to highlight the distinctions between the samples.

4.3 Results

Table 4.3 and Table 4.4 present the FWHM of the symmetric (0 0 0 2) and the asymmetric (1 0 $\bar{1}$ 2) ω scan for Group A and Group B wafers, respectively.

Wafer	A1	A2	A3 (B2)	A4
FWHM ω 002 (arc.sec)	990 ±0.26%	651.6 ±0.18%	603.4 ±0.36%	599.4 ± 1.14%
FWHM ω 102 (arc. sec.)	1294.6 ±0.45%	1230.5 ±0.33%	1224 ±0.14%	1258.2 ±3.31%
T_{screw} (cm^{-2})	1.97 x 10^9	8.52 x 10^8	7.31 x 10^8	7.21 x 10^8
T_{Edge} (cm^{-2})	3.68 x 10^9	5.78 x 10^9	6.01 x 10^9	6.48 x 10^9

Table 4.3 - FWHM of (002) and (102) reflections obtained from the HRXRD scans on Group A wafers.

Wafer	B1	B2 (A3)	B3	B4	B5
FWHM ω 002 (arc. sec.)	625.3 ±0.27%	603.4 ±0.36%	600.5 ± 0.32%	564.5 ±0.7%	555.1 ±0.63%
FWHM ω 102 (arc. sec.)	1296.8 ± 0.49%	1224 ±0.14%	1202.4 ±0.47%	1202 ±0.55%	1067 ±1.85
T_{screw} (cm^{-2})	7.85 x 10^8	7.31 x10^8	7.24 x 10^8	6.4 x 10^8	6.23 x 10^8
T_{Edge} (cm^{-2})	6.84 x 10^9	6.01 x 10^9	6.21 x 10^9	5.96 x 10^9	4.40 x 10^9

Table 4.4 - FWHM of (002) and (102) reflections obtained from the HRXRD scans on Group B wafers.

Additionally, FWHM (0002) exhibits a pronounced sensitivity to the screw component of the TDs [7], while the edge component of the TDs notably contributes to the broader (1 0 $\bar{1}$ 2) [5] [6] [7]. Corresponding screw and edge dislocation densities, estimated via the equations discussed in Section 2.6.6, reveal that the edge dislocation density is an order of magnitude higher than the screw dislocation density. This suggests that the TDD of all wafers is predominantly governed by the edge dislocations. Consequently, a decreasing trend in TDD is observed in Group A wafers as the tCGaN decreases, and similarly in Group B wafers with increasing UID layer thickness.

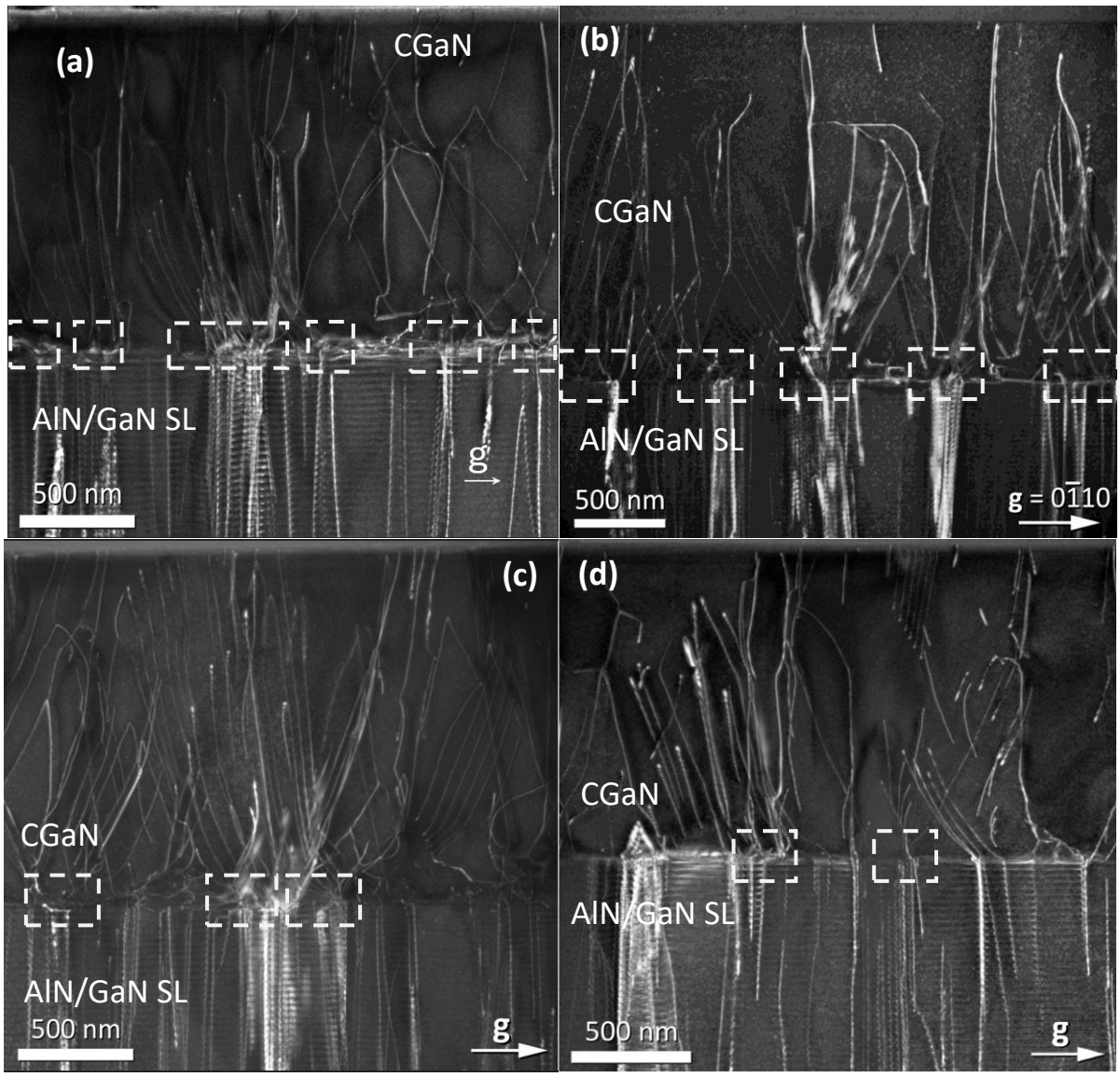

Figure 4-1 - The cross-sectional TEM (XTEM) (0110) reflection focuses on the CGaN buffer layer and the CGaN/AlN/GaN superlattice heterojunction of the wafers (a) A1 (b) A2 (c) A3 and (d) A4, highlighting the vertical propagation of threading dislocations and dislocation bunching. White lines indicate the edge dislocations.

Figure 4.1 reveals the edge dislocation microstructure, appearing as lines originating from the bottom of the CGaN layer and threading vertically upwards towards the top layers, parallel to the (0001) direction of GaN. The TEM images (a)–(d) were taken under g = 0110 diffraction conditions, which primarily highlight edge dislocations while suppressing the visibility of screw dislocations [12]. Across all four samples, a decreasing bunching effect of edge dislocations is observed, as indicated by the highlighted regions.

Notably, image (a) exhibits a pronounced bunching effect of edge dislocations on both sides of the CGaN/superlattice interface, whereas image (d) shows minimal bunching, with distinct lines observed on either side of the interface. Dislocation bunching occurs parallel to the c-plane, with multiple dislocations bundles propagating laterally at the bottom of the CGaN layer [13].

The dislocation structures observed here also highlight limitations of the mosaic block model, which underpins the extraction of dislocation densities from HRXRD. This model assumes a random, homogeneous distribution of threading dislocations within mosaic blocks, with tilt and twist between domains giving rise to line broadening [53]. In contrast, the TEM images in Figure 4.1 clearly reveal bunching, where dislocations group into correlated arrays rather than being randomly distributed [53]. Such behaviour has been reported in reciprocal space mapping studies, where distinct intensity maxima were attributed to non-uniform dislocation distributions, with higher densities at grain boundaries and lower densities in the interiors [53]. This may have implications for the accuracy of the dislocation densities derived from HRXRD in this chapter.

Barchuk et al. [53] demonstrated that when dislocation bunching occurs, the overlap and partial compensation of strain fields from neighbouring dislocations can reduce the apparent broadening of reciprocal lattice points. As a result, the dislocation densities estimated by HRXRD using a standard mosaic model are systematically underestimated compared with the true microstructure. He further demonstrated that the Monte Carlo simulations confirming the mosaic-derived values usually fall between the densities of bunched and non-bunched dislocations, meaning that HRXRD numbers are best viewed as effective averages rather than absolute measures. The discrepancy is particularly pronounced at lower overall dislocation densities (as in thicker GaN films), where bunching creates dislocation-poor interiors alongside dislocation-rich boundaries, further exaggerating the underestimation [53].

In our samples, the wafer specifications show that increased GaN thickness correlates with larger bow and broader (0002) and (1 0 $\overline{1}$ 2) reflections. Thus, the observed increase in FWHM suggests that strain accumulation leads to the generation of additional dislocations in the thicker samples. In contrast, the inhomogeneity was more pronounced in the samples with thinner CGaN, where dislocation bunching was stronger, leading to overall lower density. By contrast, the thicker samples exhibited a higher dislocation density, but with a more uniform spatial distribution. This indicates that while increasing CGaN thickness aggravates strain relaxation through the formation of new dislocations,

it simultaneously reduces localised bunching effects, resulting in comparatively more homogeneous defect networks.

The normalised channel currents have been plotted against V_{SUB} and compared with the substrate threshold voltage (V_{TH}) line, illustrated by the light grey dashed line. An increase in the overall stack thickness, driven by the increased tCGaN, results in an elevated substrate V_{TH}, which has been calculated using the equations in Chapter 2. The corresponding substrate V_{TH} values for wafers A1, A2, A3, and A4 are -384.2 V, -401.9 V, -428.8 V, and -450.9 V, respectively. The V_{TH} line, also referred to as the capacitive coupling line, serves as a reference for an ideal scenario where no trapping occurs, and the structure behaves like an ideal dielectric capacitor [14].

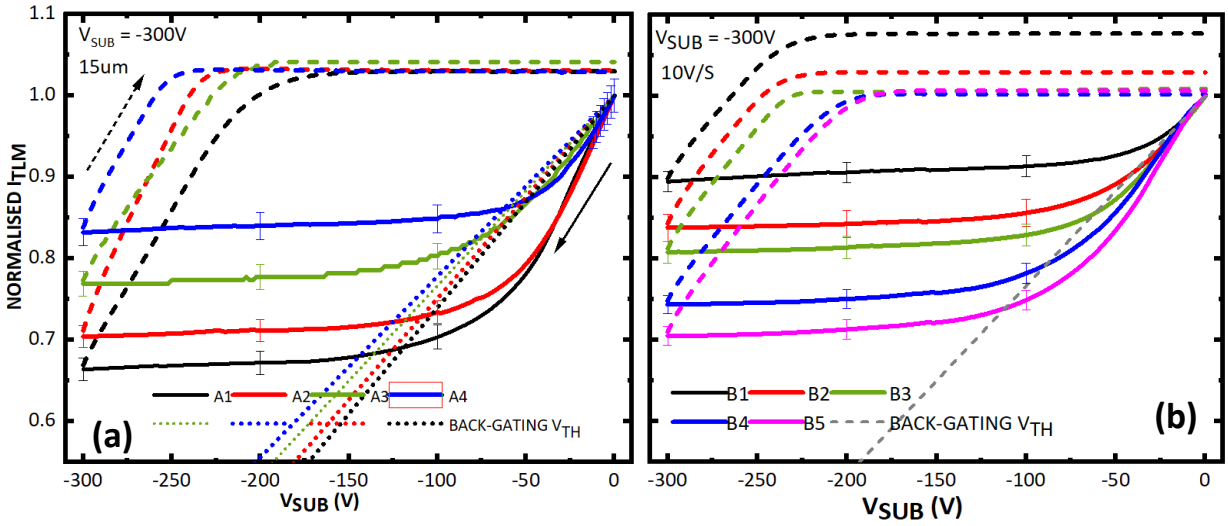

Figure 4-2 - Bi-directional substrate ramp characteristics on TLM with gap spacing 15 µm, of the eight wafers, at a sweep rate of 10V/s for (a) Group A and (b) Group B. The forward sweep from 0V to -300V and the return sweep are indicated by a solid and dashed arrows respectively. The dotted lines represent the capacitive coupling lines, illustrating the behaviour of an ideal dielectric for each tCGaN.

Figure 4.2 compares the substrate ramp characteristics of the TLM gap 15 µm for (a) Group A and (b) Group B, where the hysteresis was observed during the substrate ramps. This behaviour is consistent with previous reports on GaN-on-Si epitaxial structures with a CGaN layer, indicating the presence of trapping effects [8] [9] [15]. For Group A, Wafer A1 exhibits a more pronounced trapping effect, as evidenced by the larger hysteresis compared to Wafer A4. Similarly, in Group B, Wafer B5 also shows greater hysteresis than Wafer B1.

In Figure 4.2 (a), at low V_{SUB} (up to -50 V), a minor deviation in the normalised channel current is observed, deviating below the capacitive line before reaching current saturation.

This deviation is consistent across all four samples and associated with the transconductance (g_m) [8]. The extracted g_m values for Group A wafers are 0.0165 mS, 0.0218 mS, 0.0593 mS, and 0.0366 mS for Wafers A1, A2, A3, and A4, respectively. For Group B wafers, the values are 0.0111 mS, 0.0593 mS, 0.0166 mS, 0.028 mS, and 0.0406 mS for Wafers B1, B2 (A3), B3, B4, and B5, respectively. Notably, Wafer A3 (B2) behaves as an outlier, as evident in Figure 4.2(a).

The deviation of these currents below the capacitive line is attributed to the vertical charge redistribution within the CGaN layer. Specifically, the ionisation of C_N acceptors, which are negatively charged, accumulating at the top of the CGaN layer, while the positively charged ionised donor accumulates at the bottom of the CGaN, influencing the observed deviation [8]. A clear trend is observed: as the thickness of the CGaN decreases, g_m increases, and the deviation below the capacitive coupling line becomes more pronounced. This suggests that charge redistribution intensifies as the CGaN layer is thinned, reinforcing the relationship between g_m and vertical charge transport dynamics.

As V_{SUB} continues to increase, current saturation is observed, where the channel conductivity becomes largely independent of V_{SUB}. This behaviour is attributed to the UID layer beginning to conduct along the dislocations, leading to the accumulation of positive charge at the CGaN/AlGaN SRL interface, which neutralises the ionised acceptors [8] [16]. Notably, the observed 2DEG current saturation initiates at lower V_{SUB} as the CGaN layer thickness increases. As shown in Figure 4.2(a) Wafer A4 with the thickest CGaN layer, reaches saturation at a lower voltage compared to Wafer A1. Interestingly, as shown in Figure 4.2 (b), the Group B wafers also exhibit a similar trend as observed in the Group A wafers. In particular, the wafer with the thickest CGaN layer (and correspondingly the thinnest UID layer) reaches channel current saturation at lower V_{SUB}. The reduction in UID thickness is offset by the increased CGaN thickness, maintaining a consistent total thickness across the combined UID-CGaN layers.

During the return sweep, where V_{SUB} is swept back from -300 V to 0 V, the 2DEG becomes forward biased relative to the CGaN layer, enabling electrons from the 2DEG to inject into the CGaN layer and neutralise the accumulated positive charge. The overall return characteristics of the wafers in both groups not only appear slightly above the forward sweep characteristics but also demonstrate that a decrease in CGaN thickness results in increased hysteresis. The initial phenomenon, marked by a higher 2DEG density than the initial currents at 0 V before the substrate sweep, is referred to as

positive charge storage [8]. This indicates the presence of residual positive charge in the CGaN buffer, which may not immediately return to its initial state during the sweep.

Beyond -200 V, Group A wafers exhibit a comparable discharging rate, as evidenced by the convergence of the return currents, suggesting a uniform charge release process. Conversely, for Group B wafers, the disparity between the initial 0 V and return 0 V currents increases with CGaN thickness. This increasing disparity can be attributed to variations in the time constants among the wafers, leading to prolonged response times. These trends highlight the influence of UID and CGaN thickness on the response time to V_{SUB}.

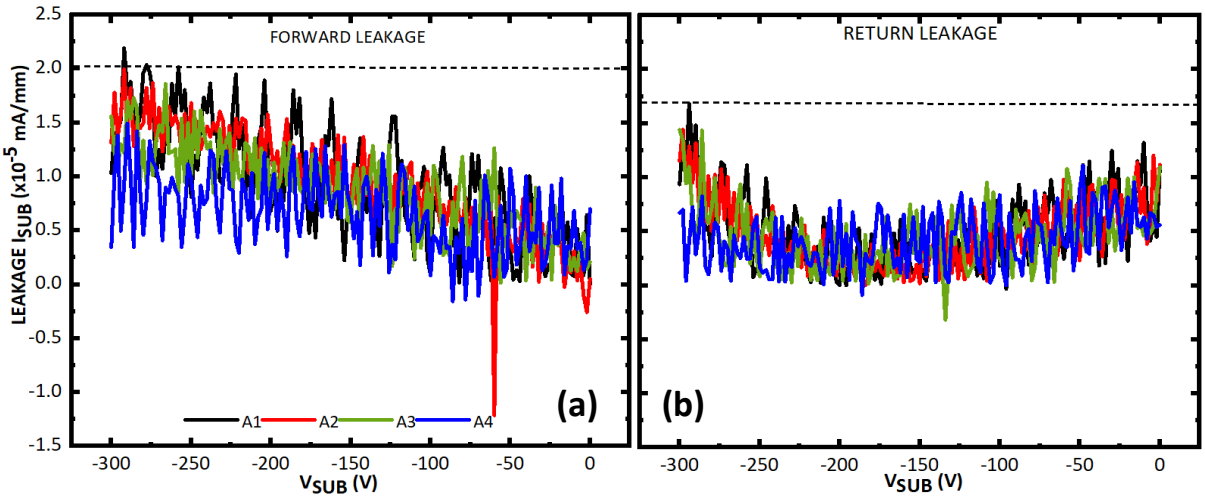

Figure 4-3 - Substrate leakage currents of the Bi-directional substrate ramp characteristics on TLM with gap spacing 15 µm, Group A wafers, at a sweep rate of 10 V/s. (a) forward sweep from 0 V to -300 V and (b) return sweep.

The substrate leakage currents (I_{SUB}) of Group A wafers during the forward sweep, as presented in Figure 4.3(a), exhibit a slight decrease in leakage current as the CGaN thickness increases. However, as shown in Figure 4.3(b), the return sweep leakage currents show a decreasing trend between -300 V and -220 V, after which the wafers exhibit comparable leakage behaviour. As discussed in Section 2.6, where the characteristics and accuracy limits of the Keithley 2410 source meter are detailed, the relative error in these leakage currents is higher than for the channel currents, particularly at nanoampere-level measurements, due to the fixed offset of approximately ±0.6 nA. This consideration regarding measurement uncertainty applies throughout all subsequent chapters, unless stated otherwise, and does not affect the identification of relative trends across the wafers.

I_{SUB} of Group B wafers during the forward sweep, as shown in Figure 4.4(a), exhibit a gradually decreasing trend as the CGaN thickness decreases. A similar trend is observed in the return sweep leakage currents, as presented in Figure 4.4(b).

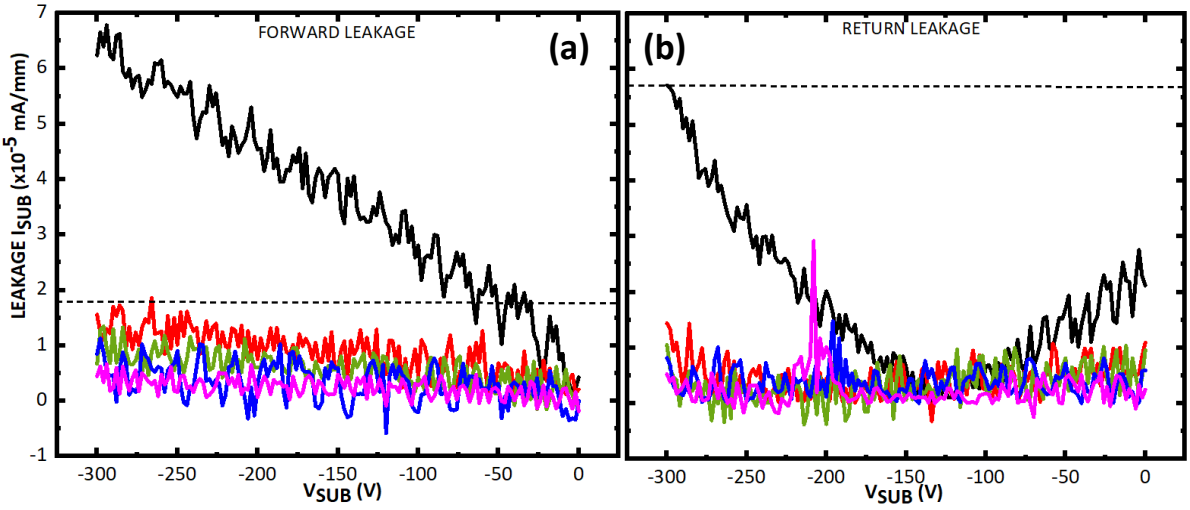

Figure 4-4 - Substrate leakage currents of the Bi-directional substrate ramp characteristics on TLM with gap spacing 15 µm, Group B wafers, at a sweep rate of 10 V/s. (a) forward sweep from 0 V to -300 V and (b) return sweep.

Figure 4.5 presents the substrate ramp characteristics for both Group A and Group B wafers when subjected to a high V_{SUB} of -550 V, applied to analyse carrier transport under conditions approaching the nominal breakdown voltage of 600 V for the epitaxy used in this study. Beyond -300 V, an additional feature emerges in the normalised channel current profile, particularly noticeable at $V_{SUB} > |-450\ V|$. At $V_{SUB} = -450$ V, the plateau region ceases, and the channel currents begin to decrease due to electron injection from the substrate. These injected electrons contribute to the formation of a resistive path within the structure, leading to increased leakage through the SRL and CGaN layer [8] [17] [14]. This also marks the point where the positive charge accumulation stops, and any remaining positive charge is retained within the epitaxy. For Group A (high voltage), the calculated error margins are ±2.1%, ±1.81%, ±1.67%, and ±2.0% for samples A1, A2, A3, and A4, respectively. For Group B, the corresponding error margins are ±1.44%, ±1.66%, ±1.67%, ±1.55%, and ±1.64% for samples B1, B2, B3, B4, and B5. These error margins are represented in the figure as error bars for each sample.

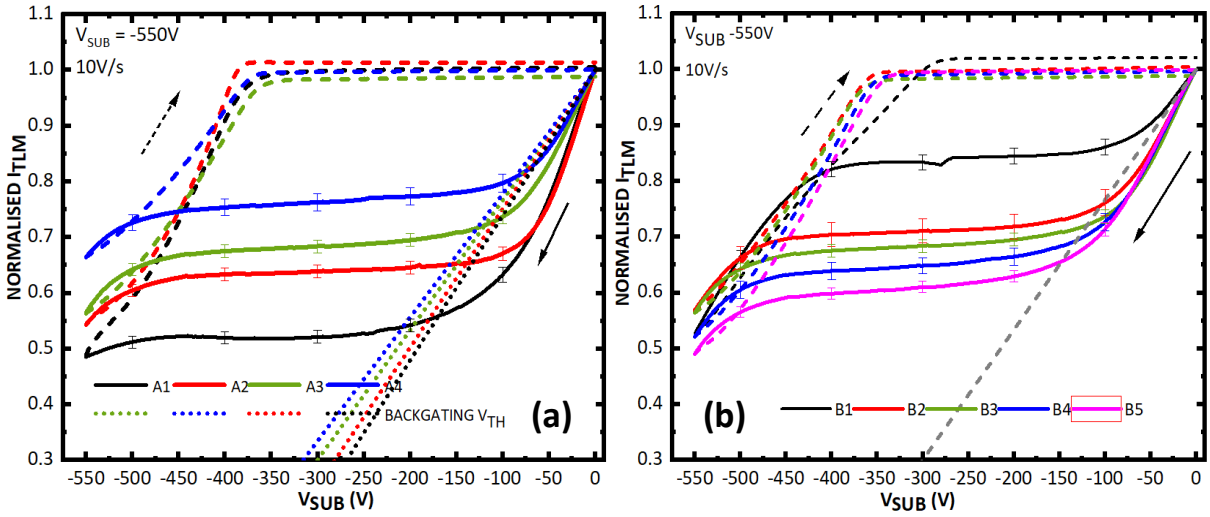

Figure 4-5 - Bi-directional substrate ramp characteristics on TLM with gap spacing 15 µm at a sweep rate of 10 V/s for (a) Group A and (b) Group B. The forward sweep from 0V to -550 V and the return sweep are indicated by a solid and dashed arrows respectively. The dotted lines represent the capacitive coupling lines, illustrating the behaviour of an ideal dielectric for each tCGaN.

Adding complexity to the charge dynamics, in contrast to the behaviour observed under low V_{SUB} conditions of -300 V, the return sweep under high V_{SUB} conditions reveals full recovery of the channel currents. Upon removing the bias, the return currents at 0 V align closely with the initial channel currents at 0 V. This behaviour indicates an absence of charge storage, suggesting that any residual positive charge dissipates effectively in the absence of bias.

Initially, the return sweep conductivity of both groups follows the capacitive coupling line, suggesting that the epitaxy behaves as an insulator [8] [18] [14]. At -400 V, the current begins to saturate, and this saturation persists until the completion of the ramp. Typically, charge dissipation occurs due to electron injection from the 2DEG to the CGaN layer, neutralising the stored positive charge via the forward-biased N-P junction between the effectively n-type UID region and the weakly p-type CGaN region [14] [19]. By forward biasing, the existing N-P depletion region is thinned, allowing for rapid electron injection [20] [21] [22].This process is likely driven by a combination of mechanisms, including electric field-assisted transport, such as trap-assisted tunnelling, as well as diffusion-driven charge transport [23]. Additionally, hot electrons may contribute to charge redistribution if they gain sufficient energy to overcome the AlGaN barrier [22] [24]. The high electric field at V_{SUB} = -550 V is expected to enhance these mechanisms, leading to a faster discharge compared to the -300 V case.

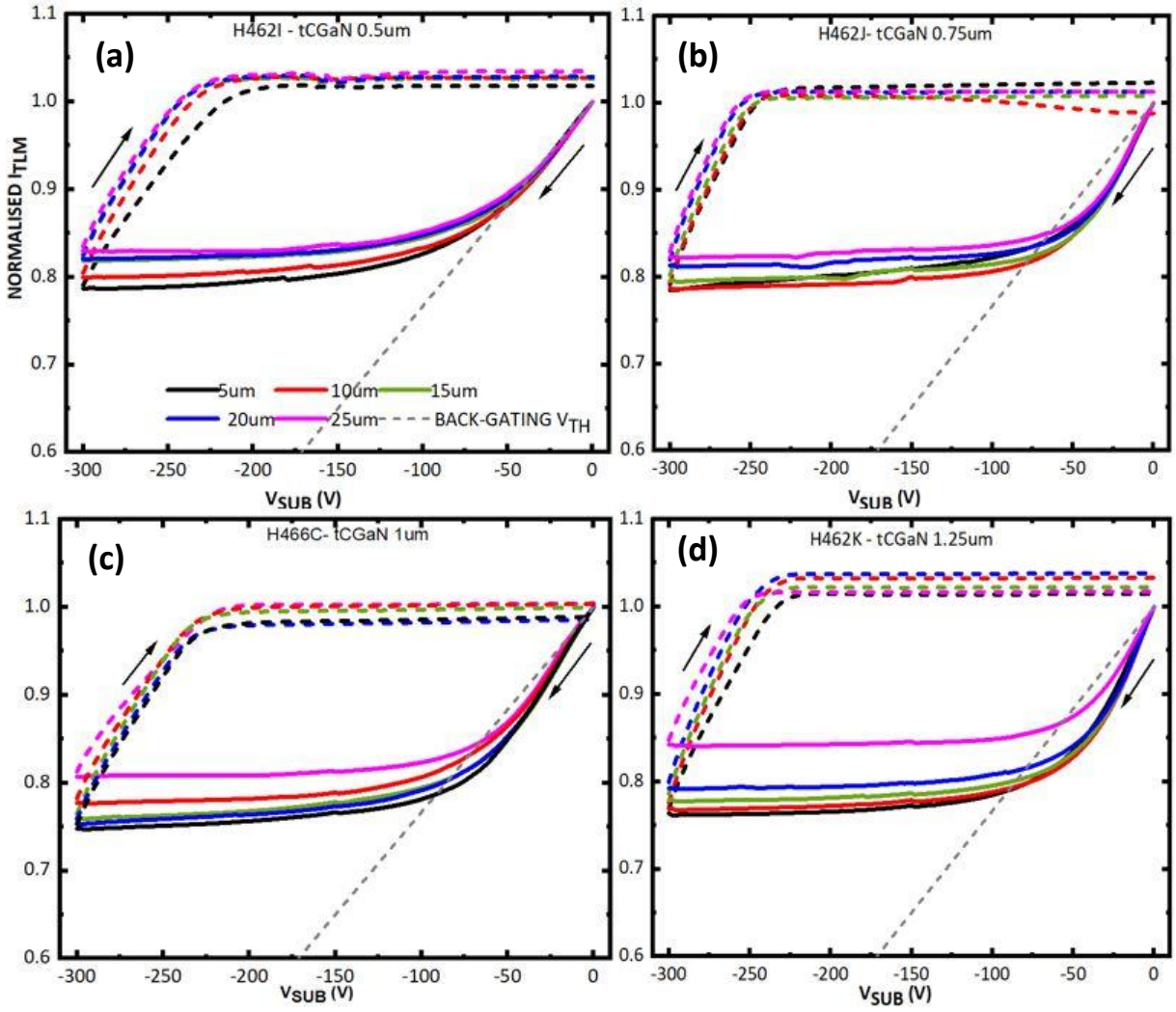

Figure 4.6 - Bidirectional substrate ramp curves of Group A wafers with a tCGaN of (a) 0.5 µm (b) 0.75 µm (c) 1 µm (d) 1.25 µm encompasing the TLM gap spacings of 5, 10, 15, 20 and 25 µm. V_{SUB} was ramped from 0V to -300V which is represented by the solid line and the return sweep where the V_{SUB} was swept back from -300V to 0V. Light grey dashed line represents the V_{TH} of each wafer. For the set of different gap spacings, which all exhibit comparable characteristics and similar current values, the overall error margin can be reasonably approximated as ±3.11%.

Figure 4.6 illustrates the bi-directional substrate ramp sweeps conducted on **Group A** wafers across various TLM gap spacings, ranging from 5 µm to 25 µm. During the measurement, V_{SUB} was swept from 0 V to -300 V and then returned to 0 V. The solid and dashed lines follow the same arrow convention as the substrate ramp, indicating the forward and return sweeps, respectively. The grey line corresponds to the respective backgating V_{TH} line. All wafers in Figures 4.6(a), (b), (c), and (d) exhibited weakly gap-dependent behaviour with a similar hysteresis effect across all gap spacings.

As illustrated in Figure 4.7 (a), (b),(c), (d) and (e), Group B also exhibited a similar weakly gap dependent hysteresis effect across all gap spacings.

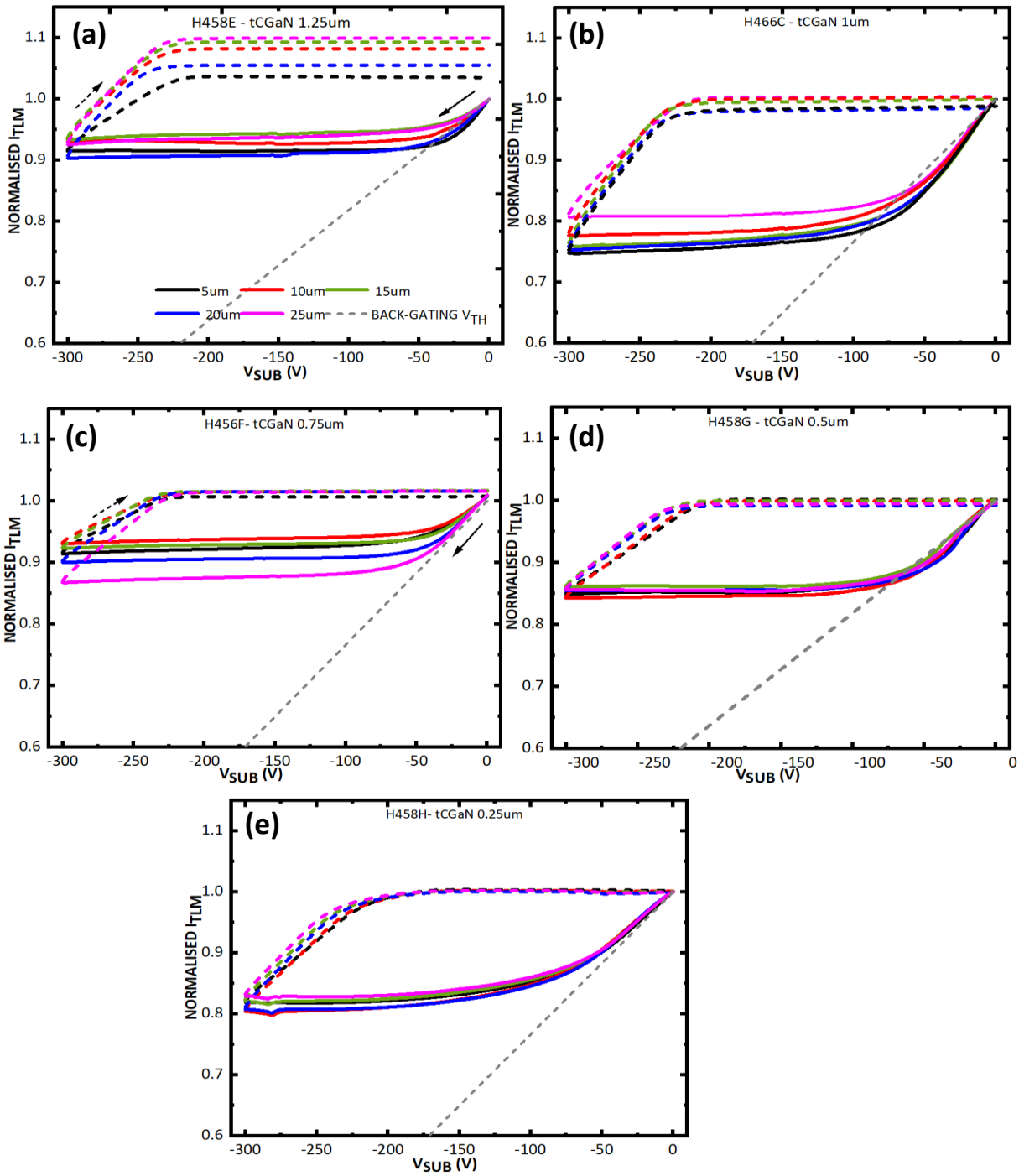

Figure 4-6 - Bidirectional substrate ramp curves of Group B wafers with a tCGaN of (a) 1.25 µm (b) 1 µm (c) 0.75 µm (d) 0.5 µm (e) 0.25 µm encompasing the TLM gap spacings of 5, 10, 15, 20 and 25 µm. For Group B, the error margins were determined to be ±3.01, ±3.11, ±3.14, ±1.84, and ±3.07 for samples B1, B2, B3, B4, and B5, respectively.

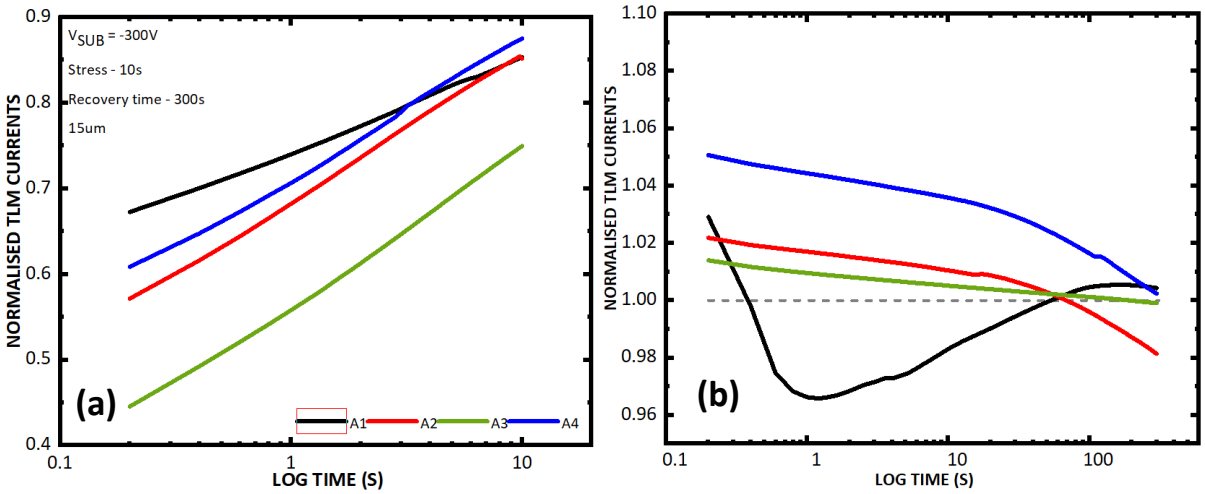

Figure 4-7 - Normalised channel currents for 15 µm TLM gap of Group A, during the (a) stress phase and (b) recovery phase of the substrate transient measurements. A substrate voltage of -300V was applied for a duration of 10 seconds and the channel current was measured at 0 V for 300 seconds after the bias was removed.

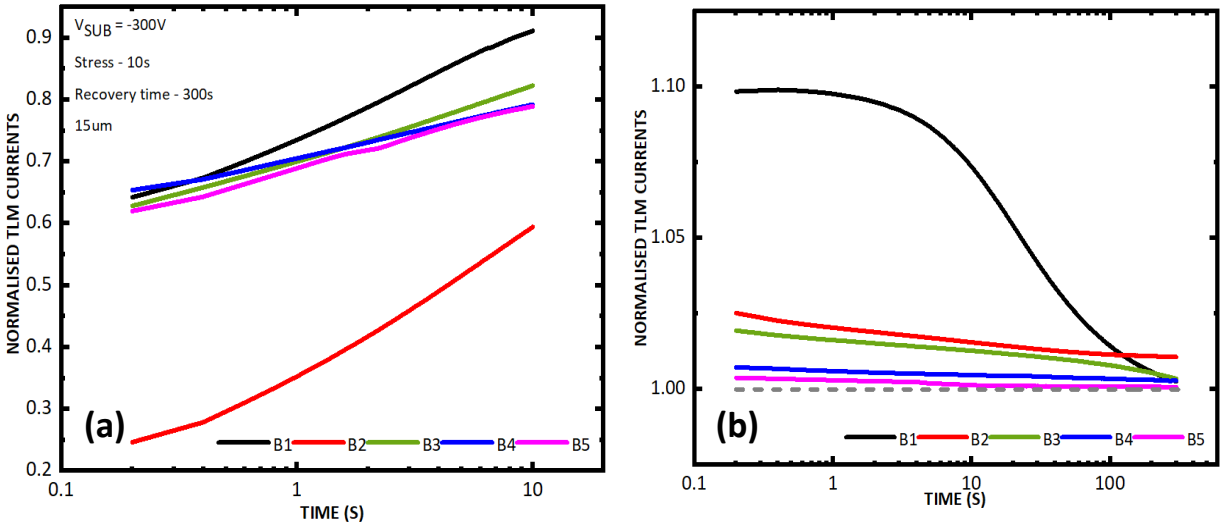

Figure 4-8 - Normalised channel currents for 15 µm TLM gap of Group B, during the (a) stress phase and (b) corresponding recovery phase of the substrate transient measurements. A substrate voltage of -300V was applied for a duration of 10 seconds and the channel current was measured at 0 V for 300 seconds after the bias was removed.

Normalised backgating transient currents under negative V_{SUB} stress for Group A and Group B are shown in Figure 4.8 and Figure 4.9, respectively. In both figures, (a) represents the stress phase, where the transient current response is measured during the application of a V_{SUB} of -300 V, while (b) corresponds to the recovery phase, observed after the substrate bias is reset to 0 V.

As shown in Figures 4.8(a), upon the application of an off-state stress, the normalised current levels are 0.67, 0.57, 0.44 and 0.61 for Wafer A1-A4 respectively, attributed to the backgating effect. In an ideal structure with no trapping, the channel currents should immediately drop to 0.2, 0.25, 0.30 and 0.35 respectively, when subjected to V_{SUB} = -300 V, as predicted by the theoretical backgating V_{TH} line. Similarly, Figure 4.9(a) shows that the normalised current levels for Wafer B1-B5 are 0.64, 0.69, 0.63, 0.61, whereas the theoretical backgating V_{TH} line predicts a drop at 0.30. The higher current values observed in both groups indicate the presence of positive charge storage. Subsequently, this is indicated by the positive-going transient (increasing channel current), suggesting continued accumulation of the positive charge storage within the CGaN layer [25], a trend that remains consistent across all wafers in this study.

However, the magnitude of the current at the end of the stress phase transients does not correlate with the substrate ramp curves, where clear trends of the backgating effect were observed as the CGaN thickness increased. This feature was evident in both groups. Notably, the stress phase transient of the shared wafer between the two groups, A3 (B2), exhibits a distinct transient behaviour with a different slope, as observed in Figure 4.8(a) and Figure 4.9(a). This difference may be attributed to variations in measurement conditions, as the transient measurements for each group were conducted separately, following the -300 V substrate ramp measurements.

The negative going (decreasing) recovery transients, depicted in Figures 4.8(b) and 4.9(b), were recorded after substrate bias was set to 0 V. The removal of the stress resulted in an immediate elevation of the channel currents for wafers in both Group A and Group B, which exceed the 0 V equilibrium level and remain above the grey dashed line. This behaviour is a consequence of the backgating effect. The increased currents in Group A exhibit no clear linear dependence on tCGaN, whereas Group B indicates a distinct linear relationship with tCGaN, as the initial currents at 20 ms decrease with a reduction in tCGaN. The overall increase in currents is followed by a gradual return to equilibrium. During the recovery phase, in the absence of substrate bias, electron diffusion from the 2DEG to the CGaN may contribute significantly to the gradual reduction of the positive charge stored in the CGaN [25].

The extracted time constants for Group A wafers are 58.4s, 100s, 101s, and 120s for wafers A1–A4, respectively. Similarly, for Group B, the time constants are 143s, 101s, 38s, 30s, and 7s for wafers B1–B5. These results suggest that wafers with the thinnest CGaN layer exhibit the fastest recovery.

To gain insight into the trapping and detrapping dynamics influenced by variations in CGaN layer thickness, as well as the combined effects of UID and CGaN while maintaining a consistent stack thickness, experimental results were complemented with TCAD simulations. This approach aimed to better understand the mechanisms underlying the observed dynamic R_{ON} behaviour. As shown in Figure 4.2, substrate ramp measurements reveal a clear trend across both groups, where distinct saturation behaviours emerge as the CGaN thickness varies. Wafers with the thickest CGaN layer exhibit the highest positive charge storage, indicating a strong correlation between CGaN layer thickness and charge accumulation.

The simulation results qualitatively capture this trend, demonstrating how CGaN thickness influences both charge accumulation and the electric field distribution. However, while the overall behaviour aligns with experimental observations, some discrepancies remain, as previously discussed in Chapter 3. A more detailed comparison between experimental and simulated results, along with an analysis of these differences, is provided in the following section.

4.4 Substrate Ramp Simulation

As discussed at the beginning of this chapter, the study focuses on two groups of wafers. Group A highlights the impact of varying CGaN layer thickness, while in Group B, both the UID and CGaN thicknesses were varied, maintaining a total UID/CGaN thickness of 1.5 µm. The model was adjusted accordingly to account for these variations, while all other parameters remained consistent with those detailed in the previous chapter.

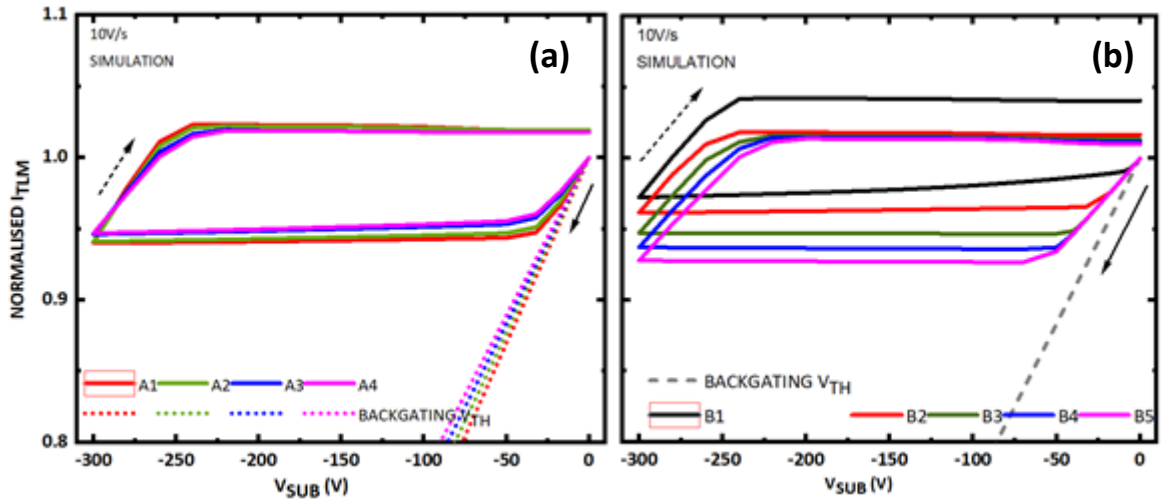

Figure 4-9 - Simulated bi-directional substrate ramp on wafers from (a) Group A and (b) Group B. V_{SUB} was swept from 0 V to -300 V at a ramp rate of 10 V/s. The arrow with the solid line indicates the forward sweep, while the dashed line arrow represents the return sweep. In (a), the dotted lines correspond to the capacitive coupling lines for each wafer in Group A, while in (b), the grey dashed line represents the capacitive coupling line for Group B wafers, where the total epilayer thickness of all five wafers are the same.

The simulated substrate ramp results for Group A and Group B are presented in Figure 4.10, as they qualitatively capture the trends observed in the substrate ramp experiments. The simulated plots exhibit hysteresis, similar to the experimental results in Figure 4.2, indicating that charge trapping and detrapping mechanisms are effectively captured. Both simulation and experiment demonstrate a trend of positive charge storage leading to saturation, particularly in wafers with the thickest CGaN layers, which exhibit the highest positive charge storage. Additionally, in both cases, the return sweep 0V current is higher than the initial 0V current, suggesting that residual trapped charge and discharging mechanisms are also partially accounted for.

Despite capturing the overall trends, the simulated plots are shifted towards the right of the capacitive coupling threshold line, indicating that the g_m of all eight wafers is significantly lower than that observed in the experimental curves. This suggests that the

simulation may underestimate charge redistribution within the CGaN layer or overestimate positively charged ionised donor accumulation, leading to a lower reduction in the 2DEG current than predicted by the backgating V_{TH} line. Additionally, the saturation effect in the simulations appears more pronounced than in the experimental results. In Group A, wafer saturation begins at -25 V, whereas in Group B, Wafer B1 starts at -15 V and B5 at -50 V. In both cases, the experimental curves required a relatively higher V_{SUB} to reach saturation. These discrepancies could also be attributed to simplifications in the charge trapping model, particularly the omission of vertical leakage pathways along threading dislocations through the reverse-biased depletion region between the UID and CGaN layers [9] [26].

Figure 4.11 (a)–(d) illustrates the simulated conduction band energy, hole density, electric field at the UID/CGaN interface, and electron density at of the Group A wafers at V_{SUB} = -300 V, respectively. This voltage point corresponds to the plateau region at -300 V in the substrate ramp graph (Figure 4.2 (a)).

Under a negative V_{SUB} of -300 V, as expected, all wafers exhibit upward band bending. Despite having the same CGaN layer doping concentration, Wafer A1 demonstrates a more pronounced upward band bending than Wafer A4, as shown in Figure 4.11(a) [27]. This indicates that the electric field stored in the C:AlGaN region of Wafer A1 is higher, whereas the corresponding field in the CGaN region is lower, in contrast to Wafer A4. This trend is also evident in Figure 4.11(b). Figure 4.11(b) further illustrates the vertical electric field distribution and the extent of the space charge region at the UID/CGaN interface. Notably, Wafer A4 exhibits a higher peak electric field than Wafer A1. Meanwhile, Figure 4.11(e) highlights the depletion region at the UID/CGaN heterojunction, revealing that Wafer A4 has a thinner charged space charge region, where a higher density of ionised C_N acceptors accumulates [8] [28]. The depletion region expands as the C:GaN thickness decreases, with Wafer A1 displaying a significantly wider depletion region compared to Wafer A4.

Figure 4.11(d) illustrates the hole density profile along the vertical cutline through all layers, highlighting hole accumulation at the C:GaN/C:AlGaN interface. Notably, the increase in the hole density between Wafers A1 and A4 appears relatively minor. Meanwhile, the corresponding electron profile in Figure 4.11(c) shows that Wafer A4 exhibits the highest 2DEG density among the four wafers analysed.

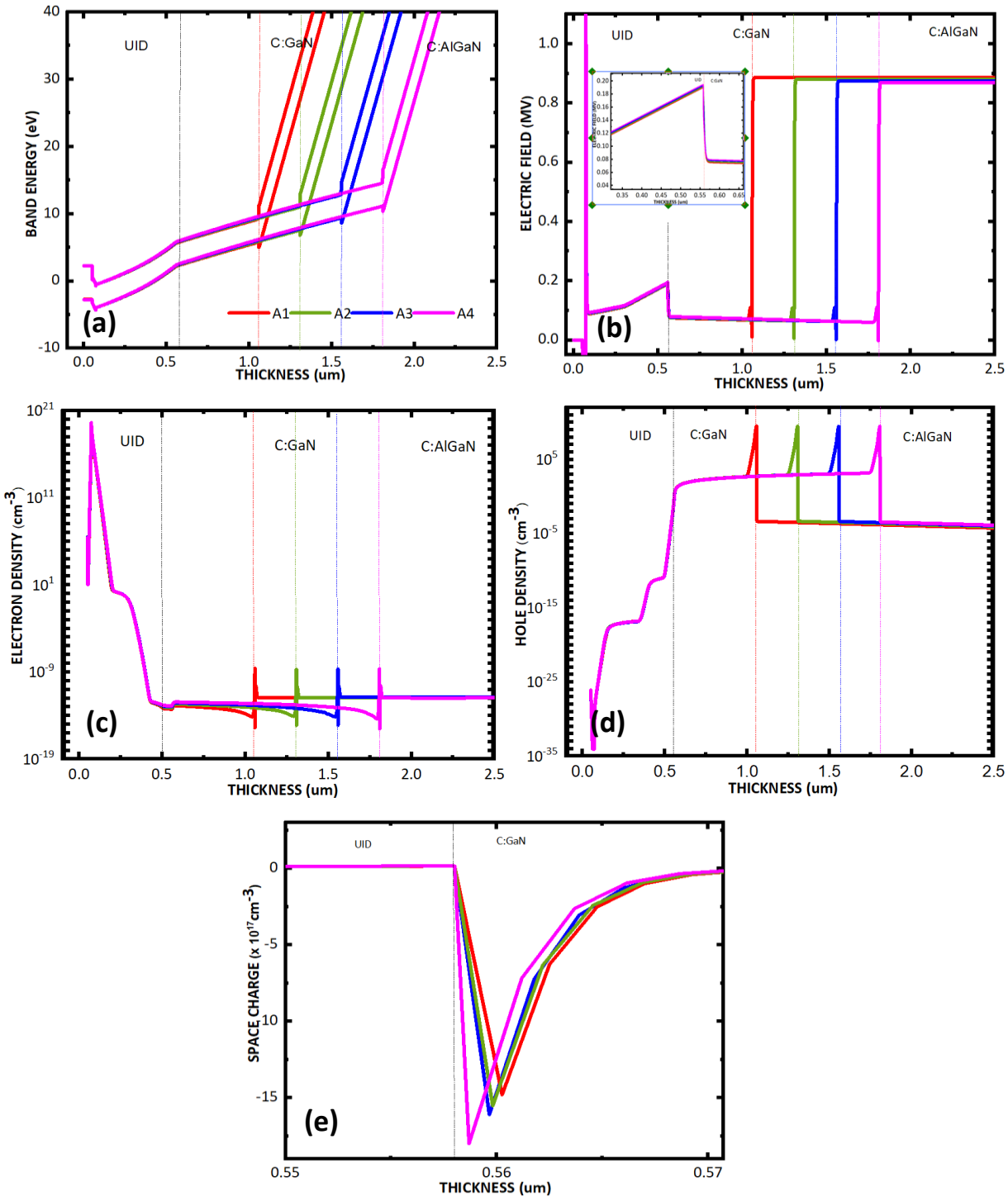

Figure 4-10 - Comparison between the simulated (a) conduction-valence band energy, (b) hole density (c) electric field at the UID/CGaN interface (d) electron density (e) space charge region at the UID/CGaN heterojunction, of the Group A wafers at V_{SUB} = -300V.

Focusing on the -300V bias point of the simulated substrate ramp curves as illustrated in Figure 4.10, where saturation is observed, the underlying mechanism can be summarised as follows:

A thicker C:GaN layer should result in a smaller C:GaN capacitance (C_{CGaN}), while the capacitance of the C:AlGaN SRL layer (C_{SRL}) should remain consistent across the wafers [29]. Using the capacitance voltage divider principle, the voltage drop across the C:AlGaN SRL (V_{SRL}) when V = V_{SUB} can be expressed as:

$$V_{SRL} = V_{SUB} * C_{CGaN}/ (C_{SRL} + C_{CGaN})$$

Similarly, the voltage drop across the CGaN layer is given by

$$V_{CGaN} = = V_{SUB} * C_{SRL}/ (C_{SRL} + C_{CGaN})$$

For Wafer A4, C_{CGaN} is expected to be the smallest due to the greater thickness of the CGaN layer. This results in a lower voltage drop across the C:AlGaN SRL and, correspondingly, a greater voltage drop across the CGaN layer. Conversely, for Wafer A1, where C_{CGaN} is much larger due to the thinner CGaN layer, the voltage drop across the CAlGaN SRL is expected to be significantly higher than that of Wafer A4, leading to a lower voltage drop across the CGaN layer. This behaviour is reflected in the electric field distribution shown in Figure 4.11(b).

In the UID region, the peak electric field increases with CGaN thickness, as evidenced by the steeper rise in its magnitude, visible in Figure 4.11(b). According to the capacitance voltage divider principle, Wafer A4 is expected to exhibit a higher electric field in the UID region than Wafer A1.

However, as discussed in Chapter 3, the observed positive charge storage is typically attributed to the lower resistivity of the UID layer compared to the CGaN layer. This lower resistivity allows more electrons to leak into the 2DEG, facilitating the accumulation of holes at the bottom of the C:GaN layer. This mechanism has been linked to trap-assisted tunnelling or hopping along dislocations, as reported in [8] [27] and [30]. Given the high electric field observed in the UID region, it is doubtful that conduction between the UID and CGaN layers is responsible for the increased positive charge storage seen in Wafer A4 (Figure 4.10(a).

The depletion region, depicted in Figure 4.11(e), demonstrates that as the CGaN thickness increases, the depletion region at the top of the CGaN layer becomes thinner due to an increased density of ionised acceptors. To maintain charge neutrality, an

equivalent number of ionised donors must accumulate at the bottom of the CGaN layer [8]. This increased donor density effectively reduces the electric field strength, screening the 2DEG and thereby limiting depletion. Furthermore, the relatively minor increase in hole density across Wafers A1–A4 could suggest that the observed positive charge storage in the simulated substrate ramp curves is primarily driven by electric field screening from the increased ionised donor density, rather than by electron leakage through the UID layer into the 2DEG, which would otherwise cause hole accumulation at the bottom of the C:GaN layer.

On the other hand, the stronger electric field in the CGaN may also enhance the tunnelling effect via the dislocations simulated using the p++ shorts, facilitating the electron transport towards the 2DEG, and resulting in a higher accumulation of electrons in the 2DEG (Figure 4.11(c)). Based on Figure 4.10(a), the variation in the saturated current levels across Wafers A1–A4 suggests that the change in positive charge storage is relatively minor. This could be attributed to the slight increase in accumulated hole density at the bottom of the C:GaN layer (Figure 4.11(d)), which enhances the effectiveness of positive charge storage.

Although the simulation does not incorporate a trap-assisted tunnelling model across the entire gap spacing, nor explicitly account for TDs, which would provide a more accurate representation of vertical leakage paths, the experimental results exhibit similar trends. This reinforces the conclusion that C:GaN thickness plays a crucial role in charge dynamics and contributes to the behaviour observed in Figure 4.10(a). Furthermore, it leaves room for interpretation that C:GaN thickness modulates the electric field within the epitaxial structure.

Figure 4.12 (a) - (d) illustrates the conduction and valance band energies, electric field distribution, hole density and the space charge region at the C:GaN/C:AlGaN P/P++ region of Group B, respectively. Similar to the observations in the Group A simulated structure, these simulations, where both the UID and C:GaN thicknesses vary, further emphasise how layer thickness influences the electric field distribution within the epitaxy and impacts charge transport. Additionally, Figure 4.12(e) compares the band-to-band tunnelling barrier width for Wafer B1 and B5, highlighting the effect of layer thickness on tunnelling characteristics.

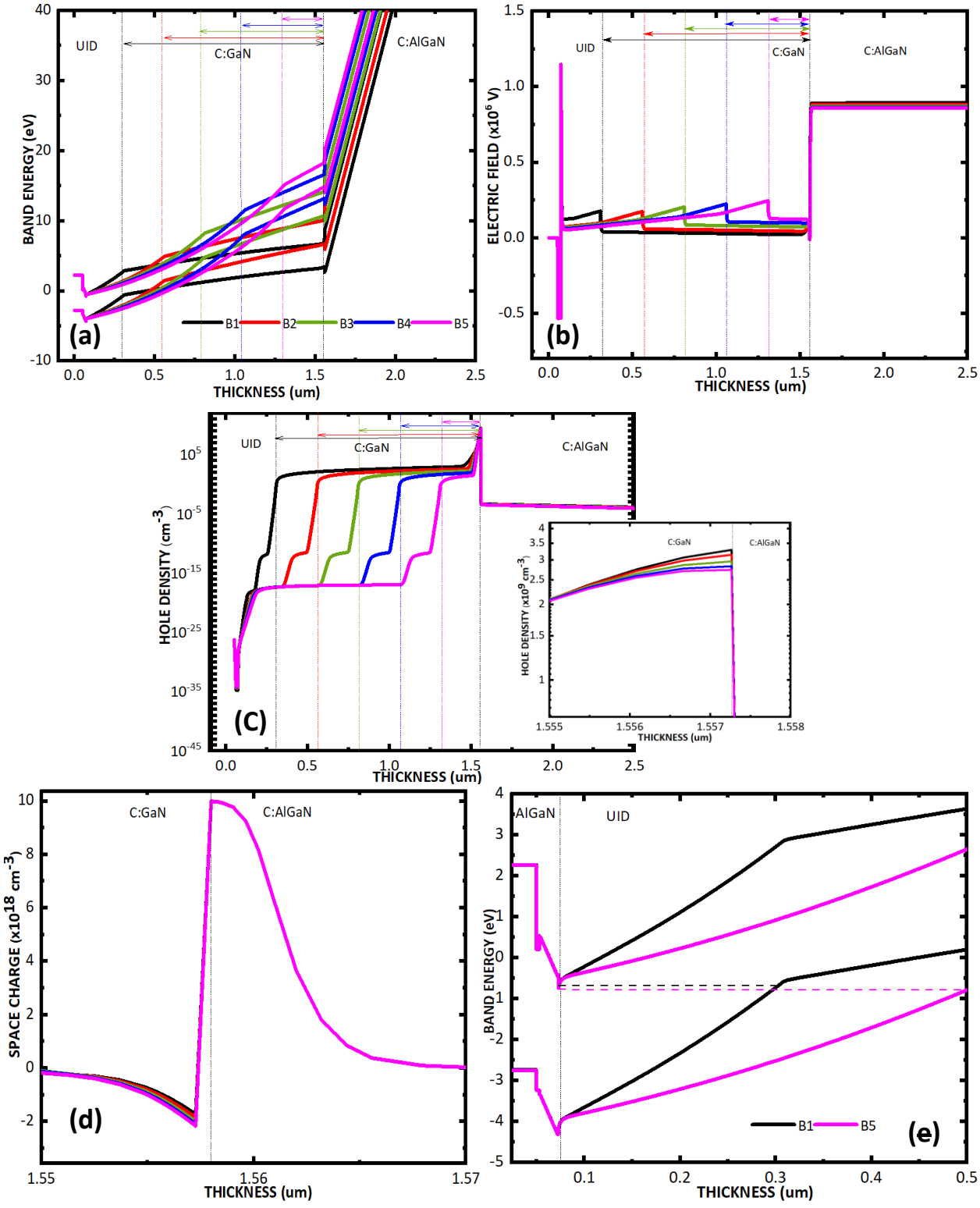

Figure 4-11 - Simulated (a) conduction band energy, (b) hole density profile, (c) electric field distribution, and (d) P/P++ space charge region at the C:GaN/C:AlGaN interface for Group B wafers at V_{SUB} = -300V. (e) Comparison of band-to-band tunnelling barrier width for Wafer B1 and B5.

Figure 4.12(a) indicates that more prominent band bending occurs in the CGaN and UID regions. In Wafer B1, represented by the black line, where the CGaN layer is thickest and the UID layer is thinnest, the band bending in CGaN is less pronounced than in Wafer B5. In contrast, Wafer B1 exhibits more significant band bending in the UID region.

As shown in Figure 4.12(b), the electric field in the CGaN region of Wafer B5 is significantly higher than that of Wafer B1. Wafer B5 also exhibits the highest peak electric field in the UID region, with a decreasing trend observed up to Wafer B2. Interestingly, Wafer B1 and Wafer B2 show similar electric field levels in the UID region. The highest electric field in the CAlGaN region is observed in Wafer B1, while Wafer B5 exhibits the lowest.

Figure 4.12(c) illustrates hole accumulation, where Wafer B1 exhibits the highest hole density among the five wafers, consistent with previously observed charge storage trends. The P/P++ space charge region at the CGaN/CAlGaN interface is shown in Figure 4.12(e), where Wafer B1 exhibits the widest depletion region, in contrast to Wafer B5, which has the narrowest. This suggests a higher density of ionised donors in Wafer B5, attributed to the thinner depletion region.

Figure 4.12(e) illustrates the band bending at the AlGaN barrier /UID interface, highlighting the inter-band barrier width between the conduction band, valence band, and the 2DEG. This indicates that the band-to-band tunnelling in Wafer B1 is higher than in Wafer B5. The dashed pink and black lines represent band-to-band leakage path, which facilitates charge leakage through the reverse-biased PN junction [8]. The injection of electrons into the 2DEG from the valence band is also easier in Wafer B1 compared to Wafer B5. This suggests that band-to-band leakage could be more prevalent when the UID layer thickness is reduced [3].

Extending the analysis applied to Group A is more complex in this case, as the capacitance of both the UID and CGaN layers varies. As previously mentioned, the resistivity in the UID region should be lower than that of the CGaN to facilitate positive charge storage [8] [19]. The electric field profile indicates a relatively decreasing electric field in the UID region, supporting the requirement for a UID region with lower resistivity compared to the other samples. Hence, the higher positive charge storage in Wafer B1 is likely attributed to enhanced band-to-band leakage along dislocations, leading to higher hole accumulation at the bottom of the CGaN layer. Another possible explanation is that

the closer spatial proximity between the 2DEG and CGaN regions, due to the reduced UID thickness, enables more efficient charge transport along the p++ shorts, ultimately leading to higher positive charge storage in Wafer B1.

While electric fields induce classical band bending due to depletion regions, mechanisms such as band-to-band tunnelling can also alter the band profile. A key consideration in this analysis is that conduction band bending is not solely attributed to the electric field but also influenced by enhanced charge movement due to positive charge storage.

4.5 Discussion

The substrate ramp measurements on the Group A and Group B wafers not only indicate the presence of positive charge storage but also provide complementary insights into the hypothesis that the CGaN layer thickness alone is not responsible for the observed dynamic R_{ON} in the GaN HEMTs.

In a study by Liu et al. [1], it was concluded that a thinner buffer layer correlates with greater positive charge storage up to V_{SUB} = -400 V. When the two wafers were exposed to V_{SUB} of -800V, the electron injection from the substrate was dominant with the thinner 4.2 µm buffer compared to the 5 µm buffer. Hence, they proposed that dynamic R_{ON} decreases as buffer thickness increases, attributed to reduced conduction along the defect band due to the diminished electric field within the buffer layer. However, a key distinction between their study and the present work is the significantly thicker CGaN layer in their structure, and the thickness of their SRL was not disclosed. The thicker CGaN in Liu et al.'s work may influence charge trapping dynamics differently, potentially altering the extent of positive charge storage and electric field redistribution within the buffer. In contrast, this study suggests that layers beyond just CGaN thickness, such as UID resistivity and charge transport pathways, contribute to the observed dynamic R_{ON}, highlighting the need for a more comprehensive approach to understanding charge storage mechanisms in GaN HEMTs.

The substrate ramp measurements for Group A wafers, shown in Figure 4.2(a), indicate that Wafer A4, which has the thickest CGaN layer, exhibits the highest positive charge storage. Similarly, in Group B, the substrate ramp results presented in Figure 4.2(b) show that Wafer B1, with the thickest CGaN layer and the thinnest UID layer combination, demonstrates the highest positive charge storage. These findings differ from prior studies, necessitating further analysis incorporating structural properties to explain the observed behaviour.

To this end, dislocation densities were extracted alongside the electrical characteristics to provide additional insight. The HRXRD data in Table 4.3 reveal that in Group A, crystal quality deteriorates with increasing CGaN thickness, as evidenced by a higher TD density. A similar trend is observed in Group B, as shown in Table 4.4, where Wafer B1, with the thickest CGaN layer, exhibits the highest TDD. This suggests that in both groups, Wafers A4 and B1 not only have the thickest CGaN layers but also exhibit the highest TDD,

indicating that increased dislocation density may be a key factor contributing to the enhanced positive charge storage observed in these wafers.

In Chapter 3, the influence of carbon doping concentration was examined, revealing that it not only served as a dominant vertical leakage path but also exhibited a weak gap dependence, particularly at the highest doping concentration of 1×10^{19} cm^{-3}. Notably, all eight wafers in this study contain this same carbon doping level. As shown in Figures 4.6 and 4.7, none of the wafers displayed TLM gap dependency in the substrate ramp measurements. This suggests that the observed positive charge storage is primarily governed by vertical leakage paths extending across the entire gap spacing [8] [30], while lateral conduction within the CGaN layer over a few microns of gap spacing remains negligible in comparison. Thus, while carbon doping concentration determines the dominant leakage mechanism, the contribution of dislocations remains significant.

Both groups exhibit the screw dislocation and the edge dislocations at densities of approximately ~10^9 cm^{-2}, which is slightly below the upper margin of the commonly reported TD density in [8] [31] [32] and [33]. While most prior studies clearly indicated that enhanced leakage caused by TDs reduces the breakdown voltage, some literature suggested that TDs can act as electrical shorts in Schottky devices, facilitating vertical leakage along their dislocation lines [34] [35] [36]. These findings further indicate the importance of understanding the nature of the conduction mechanisms associated with different types of dislocations.

The electrical activity of TDs is highly sensitive to local and structural variations, particularly the thicknesses of the layers, growth method, and growth conditions [35] [36]. As it is widely suggested, screw-type dislocations are primarily responsible for reverse leakage in AlGaN/GaN HEMTs. However, relatively few follow-up studies have evaluated the core structures of edge dislocations and their electrical behaviours. Hsu et al. [36] suggest that the dominance of edge dislocation core structures depends on background dopants and growth stoichiometry, with similar effects also expected for screw dislocations. Additionally, Kamimura et al. [54] and Yokoyama et al. [55] proposed that edge dislocations can serve as conduction paths, with conduction being anisotropic and varying depending on the direction, relative to the dislocation line. In contrast, Doding et al. [38] suggest that edge dislocations preferentially conduct along the same direction as the dislocation line, particularly parallel to the dislocation rather than in the perpendicular direction.

As observed in the TEM imaging (Figure 4.1(a)-(d)), edge dislocations are predominantly formed at the bottom of the CGaN layer and thread upwards. TEM images visually demonstrate a reduction in edge dislocation bunching [6] as the CGaN thickness increases, consistent with the trends observed in the XRD analysis. When dislocations bunch together, they may annihilate one another or form larger defects, effectively contributing to this effect, reducing the overall number of dislocations threading upward in the epitaxial layers [6] [7]. This suggests that the leakage paths along dislocations are potentially limited with the decreasing CGaN thickness, leading to reduced vertical conduction between the UID and CGaN regions. Consequently, this scenario provides a plausible explanation for the observed decrease in positive charge storage with decreasing CGaN thickness in the substrate ramp measurements, as shown in Figure 4.3(a). Conversely, the highest positive charge storage in Wafer A4 likely results from the increased number of dislocations facilitating vertical leakage.

Simulated electric field profiles (Figure 4.11b) indicate that the electric field across the UID/CGaN junction is highest in Wafer A4. However, it is important to note that the simulation does not incorporate explicit dislocation paths across ohmic contacts. In reality, Wafer A4 exhibits the highest dislocation density, meaning its leakage mechanisms are likely underestimated in the model.

Robertson et al. [23] reported that the depletion region width in a GaN p-n junction decreases near dislocation lines, locally altering the electric field opposing charge movement. They also found that dislocation-induced band bending leads to an asymmetric reduction in the diffusion barrier for electrons and holes, influenced by doping levels. Since the diffusion barrier is directly related to the built-in potential, this suggests that charge carriers experience different resistance levels when moving across heavily p-doped and lightly n-doped regions. This effect could contribute to additional leakage currents. However, Robertson et al.'s conclusions assume that TD traps behave similarly in both p-type and n-type GaN.

Even though the simulation (Figure 4.10 (a)) qualitatively replicates experimental trends without incorporating dislocation-induced leakage paths, it provides key insights into the electric field distribution (Figure 4.11(b)) under V_{SUB} = -300 V as the CGaN layer thickness increases. From the experimental substrate ramp comparison in Figure 4.2(a) and the simulated electric field profile, it is plausible that the increased number of TDs in real structures reduces the effective electric field in the UID region. This reduction likely facilitates higher vertical leakage through the narrowed depletion region,

enhancing carrier transport. Notably, while a higher electric field in the top layers is generally undesirable, the presence of dislocations could help mitigate excessive field concentrations. This highlights the dual role of dislocations—not only as contributors to leakage currents but also as factors influencing the overall electric field distribution in real devices.

The same hypothesis can be extended to explain the highest positive charge storage observed in Wafer B1, where the increasing CGaN thickness correlates with the highest TDD density. As seen in Figure 4.2(b), the experimental trends for Group B align with the explanation used for Group A, suggesting that the increased number of dislocations enhances vertical leakage.

As with Group A, the Group B simulation lacks vertical leakage paths along the ohmic gap spacing, likely underestimating dislocation-related leakage. However, it still captures the experimental trend of the highest positive charge storage in Wafer B1, highlighting the crucial role of UID and CGaN layer thickness in charge storage and transport.

The simulated electric field for **Group A** clearly showed an increase in the UID layer's electric field (Figure 4.11(b)) as the CGaN thickness increased, while the observed positive charge storage was likely facilitated by the screening effect from the ionised donor density. In contrast, the **Group B** simulations indicated a decrease in the UID electric field (Figure 4.12(b)) when both UID and CGaN thicknesses were altered. However, the increasing hole density (Figure 4.12(c)) at the bottom of the CGaN layer suggests that charge transport between the UID and CGaN occurred in this case. These findings highlight the crucial role of UID and CGaN layer thicknesses in charge transport, as their variation significantly influences the electric field distribution, the depletion region, and overall carrier dynamics. Therefore, careful optimisation of these thicknesses is essential to achieve controlled electrical behaviour and minimise unwanted leakage pathways.

The normalised channel current profile for the wafers in both groups (Figure 4.5(a) and (b)), particularly at V_{SUB} >|-450 V|, reveals a decrease in the channel current with increasing substrate voltage due to electron leakage from the substrate through the SRL [8], a trend consistently observed across all eight wafers. As previously explained, this phenomenon occurs when the positive charge accumulated in the buffer becomes insufficient to further screen the applied potential, leading to a gradual decrease in the 2DEG current. As discussed in Chapter 3, wafer with the highest CGaN layer carbon doping concentration of $1 \times 10^{19} cm^{-3}$ exhibited a reduction in the substrate voltage at which

the entire structure begins to leak, demonstrating the impact of carbon. However, the substrate voltage at which the channel current begins to decrease appears to be independent of the thickness of the UID GaN and CGaN in the wafers from both Groups A and B. This suggests that the observed behaviour is primarily influenced by the carbon concentration rather than the UID or CGaN thickness.

As shown in the recovery transient currents in Figure 4.8(b) and Figure 4.9(b), the fastest recovery in Group A samples was observed in A1, while in Group B, B5 exhibited the swiftest recovery. Both wafers had the thinnest CGaN layers and the highest-quality epitaxy within their respective groups. The observed trend of increasing time constants with CGaN thickness suggests that electron diffusion is progressively hindered as the CGaN layer becomes thicker.

Kumakura et al. [42] observed that the minority carrier diffusion length in a GaN PN diode depends on two factors: doping concentration and dislocation density. They also suggested that, for a relatively high doping concentration (particularly in the range of 10^{19} cm^{-3}), the diffusion length drastically decreases with increasing dislocation density [42]. All samples in the study had a doping level of 1×10^{19} cm^{-3}, implying that the impurity defect band remained consistent [43]. In Group A, as the CGaN thickness decreased, we observed a reduction in the edge dislocation trend due to dislocation bunching, thus improving crystal quality. This suggests that the reduction in dislocation density led to an enhanced diffusion length, with minimal impact on electron mobility, resulting in faster recovery. A similar interpretation applies to Group B, where Wafer B5 exhibited the lowest dislocation density among its counterparts. This confirms that dislocation density strongly influences the recovery transient, as improved crystal quality enhances charge carrier mobility and reduces scattering, collectively facilitating faster current recovery.

Another critical factor affecting the dynamic R_{ON} in Group B is the proximity between the 2DEG and the CGaN layer, particularly as UID thickness decreases. This aligns with Kim et al. [45], who studied variations in UID and CGaN thickness while maintaining a total buffer thickness of 1.3 µm. They observed that wafers with thinner CGaN layers (i.e., thicker UID layers) exhibited higher positive charge storage and faster transient recovery. Their findings suggested that a thinner UID layer contributes to higher dynamic R_{ON}.

Conversely, Treidel et al. [46] reported that increasing UID thickness from 35 nm to 100 nm increased reverse bias leakage currents, implying that dynamic R_{ON} rises with

UID layer thinning. Similarly, Putcha et al. [3] varied UID thickness while keeping CGaN thickness constant and noted no clear trend among buffer layers of 2.5 µm, 1.8 µm, and 1.3 µm. However, the 1.8 µm buffer layer exhibited the highest dynamic R_{ON}, attributed to its increased dislocation density. Alian et al. [47] also concluded that thinning the UID layer increases dynamic R_{ON}, due to its impact on 2DEG proximity and charge trapping.

Group A presents a different trend regarding substrate leakage, where the I_{SUB} decreased with increasing CGaN thickness. Particularly, Wafer A4 exhibits the lowest I_{SUB} (Figure 4.3). In contrast, Group B showed decreasing I_{SUB} as CGaN thickness decreased (UID thickness increased), with Wafer B5 displaying the lowest I_{SUB} (Figure 4.4). This suggests that for a fixed UID thickness, CGaN resistivity influences vertical leakage currents, in agreement with classical leakage suppression by a thicker CGaN layer. However, Wafer B1 exhibited the highest vertical leakage despite having the same CGaN thickness as Wafer A4, supporting prior findings [3] [47] [46] that a thinner UID layer leads to increased leakage. The relatively low I_{SUB} in Wafer B5 may be attributed to reduced TD density [48], though additional experimental validation is needed. This highlights that substrate leakage mitigation in these epitaxies is not solely dependent on the CGaN layer thickness alone.

For high-power switching applications, a high-quality, thick UID layer is generally preferred due to its role as a blocking layer [46]. Ensuring a low dislocation density in the UID layer enables intrinsic point defects to compensate for residual n-type donors such as oxygen or silicon, thereby reducing leakage paths [46]. While the overall dislocation density affects device performance, leakage pathways are not necessarily detrimental, as they facilitate controlled charge dissipation. Moreover, although breakdown voltage (V_{BR}) is not explicitly analysed in this study, various findings contribute indirectly to its understanding. Yu et al. [49] found that reducing the UID layer thickness increases V_{BR} by lowering buffer leakage, a conclusion that differs from previous studies, perhaps due to their use of GaN-on-SiC with Fe doping instead of carbon. Conversely, Alian et al. [47] determined that UID thickness has no significant effect on V_{BR}.

These findings demonstrate that simply varying CGaN thickness is not sufficient to achieve an optimised dynamic R_{ox} device. Instead, careful adjustment of both CGaN and UID layer thicknesses is necessary to balance leakage suppression, transient recovery, and overall device performance.

4.6 Conclusions

This study systematically examined the impact of varying CGaN and UID thicknesses on defect evolution, charge storage, substrate leakage, and transient behaviour, ultimately influencing dynamic R_{ON}.

Despite consistent carbon concentrations, increasing CGaN thickness led to higher TD density and crystal quality deterioration in both groups, reinforcing the strong interplay between layer thickness and dislocation behaviour. TEM analysis confirmed TD bunching, effectively reducing the effective number of dislocation density observed with decreasing CGaN thickness.

At V_{SUB} of -300 V, higher CGaN thickness correlated with increased positive charge storage, likely due to enhanced vertical leakage attributed to the increased TD density. This supports the hypothesis that increased dislocation density reduces the depletion width and diffusion barrier, facilitating greater electron leakage into the 2DEG along the reverse-biased PN junction.

The return sweep 0 V currents in Group A remained higher than the initial 0 V currents, indicating residual positive charge in the epitaxy. In contrast, for Group B, this difference decreased as UID thickness was increased.

During substrate transient measurements, faster recovery was observed with increasing UID thickness in Group B, while in Group A, wafer A1 exhibited the swiftest recovery. Notably, both wafers with the smallest time constants shared a key characteristic, as they had the lowest TD density, resulting in superior crystal quality. This highlights a critical conclusion: electron diffusion-based recovery is strongly influenced by dislocation density, where lower TD density enhances charge transport and accelerates transient recovery.

All 8 wafers exhibited weakly gap-independent behaviour, indicating that gap dependence is primarily influenced by carbon doping concentration (consistent with conclusions from Chapter 3) rather than CGaN or UID thickness. The bias point where electron injection begins after current saturation remained consistent across all wafers, reinforcing the conclusion that carbon doping concentration, rather than UID or CGaN layer thickness, is the dominant factor.

For Group B, thinner UID layers led to enhanced charge trapping, resulting in a higher dynamic R_{ON}, which is consistent with previous studies.

The substrate leakage behaviour further highlighted distinct trends, where in Group A, substrate leakage currents decreased with increasing CGaN thickness, whereas in Group B, leakage currents increased with increasing CGaN thickness, suggesting that UID resistivity plays a crucial role in vertical leakage suppression.

Simulations conducted at -300V during current saturation revealed that:

For Group A, increasing CGaN thickness resulted in a higher electric field in the UID region, whereas for Group B, increasing CGaN thickness led to a lower electric field in the UID region. Additionally, these variations in UID and CGaN layer thickness were found to influence the SRL region as well, emphasising the need for precise electric field optimisation when designing these structures.

Finally, Wafer A1 with the thinnest CGaN layer and Wafer B5 with the thickest UID layer exhibited the least degradation in dynamic R_{ON}. This highlights a clear trade-off between UID thickness, CGaN thickness, and dynamic R_{ON}, emphasising the necessity of carefully optimising these parameters to achieve superior device performance.

4.7 References

[1] J. Liu, W. Zou, J. Chen, M. Hua, D. Lu and J. Ma, "The impact of buffer thickness upon the transport-limited buffer trapping effects in carbon-doped power GaN-on-Si devices," Applied physics letters, vol. 123 , no. 11, p. 112105, 2023-09.

[2] V. Joshi, S. D. Gupta, R. R. Chaudhuri and M. Shrivastava, "Interplay of Device Design and Carbon-Doped GaN Buffer Parameters in Determining Dynamic in AlGaN/GaN HEMTs," IEEE transactions on electron devices, vol. 69, no. 11, pp. 6035-6042, 2022-11.

[3] V. Putcha, L. Cheng, A. Alian, M. Zhao, H. Lu, B. Parvais, N. Waldron, D. Linten and N. Collaert, "On the impact of buffer and GaN-channel thickness on current dispersion for GaN-on-Si RF/mmWave devices," in IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 2021.

[4] A. Shanbhag, S. M P, F. Medjdoub, A. Chakravorty, N. DasGupta and A. DasGupta, "Optimized Buffer Stack with Carbon-Doping for Performance Improvement of GaN HEMTs," in IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), Monterey, CA, USA, 2021.

[5] J. Bai, T. Wang, P. Parbrook, K. Lee and A. Cullis, "A study of dislocations in AlN and GaN films grown on sapphire substrates," Journal of crystal growth, vol. 282, no. 3-4, pp. 290-296, 2005.

[6] M. Barchuk, C. Röder, Y. Shashev, G. Lukin, M. Motylenko, J. Kortus, O. Pätzold and D. Rafaja, "Correlation between the residual stress and the density of threading dislocations in GaN layers grown by hydride vapor phase epitaxy," Journal of crystal growth, vol. 386, no. 2014-01, p. 1–8, 2014.

[7] A. Wickenden, D. Koleske, R. Henry, M. Twigg and M. Fatemi, "Resistivity control in unintentionally doped GaN films grown by MOCVD," Journal of crystal growth, vol. 260, no. 1, p. 54–62, 2004.

[8] M. Uren, S. Karboyan, I. Chatterjee, A. Pooth, P. Moens, A. Banerjee and M. Kuball, "Leaky Dielectric" Model for the Suppression of Dynamic Ron in Carbon-Doped AlGaN/GaN HEMTs," IEEE Transactions on Electron Devices, vol. 64, p. 2826–2834, 2017.

[9] M. J. Uren, M. Silvestri, M. Casar, G. A. M. Hurkx, J. A. Croon, J. Sonsky and M. Kuball, "Intentionally Carbon-Doped AlGaN/GaN HEMTs: Necessity for Vertical Leakage Paths," IEEE Electron Device Letters, vol. 35, no. 3, pp. 327-329, 2014.

[10] M. Singh, S. Karboyan, M. J. Uren, K. B. Lee, Z. Zaidi, P. A. Houston and M. Kuball, "Lateral charge spreading and device-to-device coupling in C-doped AlGaN/GaN-on-Si wafers," Microelectronics Reliability, vol. 95, pp. 81-86, 2019.

[11] M. J. Uren, M. Cäsar, M. A. Gajda and M. Kuball, “Buffer transport mechanisms in intentionally carbon doped GaN heterojunction field effect transistors,” Applied physics letters, vol. 104, no. 26, pp. 1077-3118, 2014.

[12] J. Rouviere, M. Arlery, B. Daudin, G. Feuillet and O. Briot, “Transmission electron microscopy structural characterisation of GaN layers grown on (0001) sapphire,” Materials science & engineering. B, Solid-state materials for advanced technology, vol. 50, no. 1, pp. 61-71, 1997-12.

[13] A. Sakai, H. Sunakawa, A. Kimura and A. Usui, “Self-organized propagation of dislocations in GaN films during epitaxial lateral overgrowth,” Applied physics letters, vol. 76, no. 4, pp. 442-444, 2000-01.

[14] S. Yang, C. Zhou, S. Han, J. Wei, K. Sheng and K. J. Chen, “Impact of substrate bias polarity on buffer-related current collapse in AlGaN/GaN-on-Si power devices,” IEEE Transactions on Electron Devices, vol. 64, no. 12, pp. 5048-5056, 2017.

[15] I. Chatterjee, M. J. Uren, S. Karboyan, A. Pooth, P. Moens, A. Banerjee and M. Kuball, “Lateral Charge Transport in the Carbon-Doped Buffer in AlGaN/GaN-on-Si HEMTs,” IEEE transactions on electron devices, vol. 64, no. 3, p. 977–983, 2017.

[16] P. Moens, A. Banerjee, M. J. Uren, M. Meneghini, S. Karboyan, I. Chatterjee, P. Vanmeerbeek, M. Casar, C. Liu, A. Salih, E. Zanoni, G. Meneghesso, M. Kuball and M. Tack, “Impact of buffer leakage on intrinsic reliability of 650V AlGaN/GaN HEMTs,” in IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 2016.

[17] P. Moens, P. Vanmeerbeek, A. Banerjee, J. Guo, C. Liu, P. Coppens, A. Salih, M. Tack, M. Caesar, M. J. Uren, M. Kuball, M. Meneghini, G. Meneghesso and E. Zanoni, “On the impact of carbon-doping on the dynamic Ron and off-state leakage current of 650V GaN power devices,” in 2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD), HK, China, 2015.

[18] H. Chandrasekar, M. J. Uren, A. Eblabla, H. Hirshy, M. A. Casbon, P. J. Tasker, K. Elgaid and M. Kuball, “Buffer-Induced Current Collapse in GaN HEMTs on Highly Resistive Si Substrates,” IEEE electron device letters, vol. 39, no. 10, pp. 1556-1559, 2018-10.

[19] W. M. Waller, M. Gajda, S. Pandey, J. J. T. M. Donkers, D. Calton, J. Croon, J. Sonsky, M. J. Uren and M. Kuball, “Control of Buffer-Induced Current Collapse in AlGaN/GaN HEMTs Using SiNx Deposition,” IEEE transactions on electron devices, , Vol.), p., Article 8013764, vol. 64, no. 10, pp. 4044-4049, 2017-10.

[20] A. Pooth, M. J. Uren, M. Cäsar, T. Martin and M. Kuball, “Charge movement in a GaN-based hetero-structure field effect transistor structure with carbon doped buffer under applied substrate bias,” Journal of applied physics, vol. 118, no. 21, p. 215701, 2015-12.

[21] Y. Lin, M.-L. Kao, Y.-C. Weng, C.-F. Dee, S.-C. Chen, H.-C. Kuo, C.-H. Lin and E.-Y. Chang, “Buffer Traps Effect on GaN-on-Si High-Electron-Mobility Transistor at Different Substrate Voltages,” Micromachines (Basel), vol. 13, no. 12, p. 2140, 2022-12.

[22] D. Bisi, M. Meneghini, M. Van Hove, D. Marcon, S. Stoffels, T.-L. Wu, S. Decoutere, G. Meneghesso and E. Zanoni, “Trapping mechanisms in GaN-based MIS-HEMTs grown on silicon substrate,” physica status solidi (a), vol. 212, no. 5, pp. 1122-1129, 2015.

[23] C. A. Robertson, K. S. Qwah, Y.-R. Wu and J. S. Speck, “Modeling dislocation-related leakage currents in GaN p-n diodes,” Journal of applied physics,, vol. 126 , no. 24, p. 245705, 2019-12.

[24] B. Butej, V. Padovan, D. Pogany, G. Pobegen, C. Ostermaier and C. Koller, “Method to Distinguish Between Buffer and Surface Trapping in Stressed Normally-ON GaN GITs Using the Gate-Voltage Dependence of Recovery Time Constants,” IEEE transactions on electron devices, vol. 69, no. 6, pp. 3087-3093, 2022-06.

[25] A. Nardo, C. De Santi, C. Koller, C. Ostermaier, I. Daumiller, G. Meneghesso, E. Zanoni and M. Meneghini, “Positive and negative charge trapping GaN HEMTs: Interplay between thermal emission and transport-limited processes,” Microelectronics Reliablity, vol. 126, p. 114255, 2021.

[26] M. Singh, M. J. Uren, T. Martin, S. Karboyan, H. Chandrasekar and M. Kuball, “"Kink" in AlGaN/GaN-HEMTs: floating buffer model,” IEEE Transactions on Electron Devices, vol. 65, no. 9, pp. 3746-3753, 2018.

[27] M. Millesimo, M. Borga, L. Valentini, B. Bakeroot, N. Posthuma, A. Vohra, S. Decoutere, C. Fiegna and A. N. Tallarico, “ Role of the GaN-on-Si Epi-Stack on Δ R ON Caused by Back-Gating Stress,” IEEE transactions on electron devices, vol. 70, no. 10, pp. 5203-5209, 2023-10.

[28] F. Wach, M. J. Uren, B. Bakeroot, M. Zhao, S. Decoutere and M. Kuball, “Low Field Vertical Charge Transport in the Channel and Buffer Layers of GaN-on-Si High Electron Mobility Transistors,” IEEE electron device letters, vol. 41, no. 12, pp. 1754-1757, 2020-12.

[29] C. Koller, G. Pobegen, C. Ostermaier, M. Huber and D. Pogany, “The interplay of blocking properties with charge and potential redistribution in thin carbon-doped GaN on n-doped GaN layers,” Applied physics letters, , vol. 111, no. 3, p. 032106, 2017-07.

[30] F. Wach, M. J. Uren, B. Bakeroot, M. Zhao, S. Decoutere and M. Kuball, “Low Field Vertical Charge Transport in the Channel and Buffer Layers of GaN-on-Si High Electron Mobility Transistors,” IEEE Electron Device Letters, vol. 41, no. 12, pp. 1754-1757, Dec. 2020.

[31] P. Dalapati, S. Urata and T. Egawa, “Investigation of AlGaN/GaN high electron mobility transistors on Silicon (111) substrates employing multi-stacked strained layer superlattice structures,” Superlattices and Microstructures, vol. 147, p. 106709, 2020.

[32] J. Manuel, F. Morales, R. García, R. Aidam, L. Kirste and O. Ambacher, “Threading dislocation propagation in AlGaN/GaN based HEMT structures grown on Si (111) by plasma assisted molecular beam epitaxy,” Journal of crystal growth, vol. 357, pp. 35-41, 2012.

[33] D. F. Storm, D. S. Katzer, S. C. Binari, B. V. Shanabrook, L. Zhou and D. J. Smith, “Effect of Al/N ratio during nucleation layer growth on Hall mobility and buffer leakage of molecular-beam epitaxy grown AlGaN/GaN heterostructures,” Applied physics letters, vol. 85, no. 17, pp. 3786-3788, 2004-10.

[34] J. Wang, H. You, H. Guo, J. Xue, G. Yang, D. Chen, B. Liu, H. Lu, R. Zhang and Y. Zheng, “Do all screw dislocations cause leakage in GaN-based devices?,” Applied physics letters, vol. 116, no. 6, p. 062104, 2020-02.

[35] C. L. Reynolds, J. G. Reynolds, A. Crespo, J. K. Gillespie, K. D. Chabak and R. F. Davis, “Dislocations as quantum wires: Buffer leakage in AlGaN/GaN heterostructures,” Journal of materials research, vol. 28, no. 13, pp. 1687-1691, 2013-07.

[36] J. W. Hsu, M. J. Manfra, D. V. Lang, S. Richter, S. N. Chu, A. M. Sergent, R. N. Kleiman, L. N. Pfeiffer and R. J. Molnar, “Inhomogeneous spatial distribution of reverse bias leakage in GaN Schottky diodes,” Applied physics letters, vol. 78, no. 12, pp. 1685-1687, 2001-03.

[37] W. Shockley, “Some predicted effects of Temperature Gradients on Diffusion in Crystals,” Phys Review , pp. 1563-1564, 1953.

[38] G. Döding and L. R., “Anisotropic conductivity of CdS after plastic deformation and conduction along dislocations: II. Measurements on a microscopic scale†,” Physica status solidi (a), vol. 68, no. 2, pp. 469-476, 1981.

[39] J. A. Grenko, C. W. Ebert, C. L. Reynolds Jr, G. J. Duscher, D. W. Barlage, M. A. L. Johnson, E. A. Preble, T. Paskova and K. R. Evans, “Optimization of homoepitaxially grown AlGaN/GaN heterostructures,” Physica status solidi. A, Applications and materials science, , vol. 207, no. 10, pp. 2292-2299, 2010-10.

[40] J. A. Grenko, C. L. Reynolds, D. W. Barlage, M. A. L. Johnson, S. E. Lappi, C. W. Ebert, E. A. Preble, T. Paskova and K. R. Evans, “Physical Properties of AlGaN/GaN Heterostructures Grown on Vicinal Substrates,” Journal of electronic materials, vol. 39, no. 5, pp. 504-516, 2010-05.

[41] W. Knap, C. Skierbiszewski, K. Dybko, J. Łusakowski, M. Siekacz, I. Grzegory and S. Porowski, “Influence of dislocation and ionized impurity scattering on the electron

mobility in GaN/AlGaN heterostructures," Journal of crystal growth, vol. 281, no. 1, pp. 194-201, 2005-07.

[42] K. Kumakura, T. Makimoto, N. Kobayashi, T. Hashizume, T. Fukui and H. Hasegawa, "Minority carrier diffusion length in GaN: Dislocation density and doping concentration dependence," American Institute of Physics, vol. 86, no. 5, pp. 052105-052105-3, 2005.

[43] C. Koller, G. Pobegen, C. Ostermaier and D. & Pogany, "Effect of carbon doping on charging/discharging dynamics and leakage behavior of carbon-doped GaN," IEEE Transactions on Electron Devices, vol. 65, no. 12, pp. 5314-5321, 2018.

[44] M. Borga, M. Meneghini, D. Benazzi, E. Canato, R. Püsche, J. Derluyn, I. Abid, F. Medjdoub, G. Meneghesso and E. Zanoni, "Buffer breakdown in GaN-on-Si HEMTs: A comprehensive study based on a sequential growth experiment," Microelectronics Reliability, Vols. 100-101, p. 113461, 2019.

[45] H.-S. Kim, M. J. Uren, H. Hirshy, A. Withey, R. Harper, S. Evans and M. Kuball, "Dynamic Ron in AlGaN/GaN Structure with Different Layer Thickness," in CS MANTECH Conference, Monterey, CA, 2022.

[46] E. Bahat-Treidel, F. Brunner, O. Hilt, E. Cho, J. Wurfl and G. Trankle, "AlGaN/GaN/GaN:C Back-Barrier HFETs With Breakdown Voltage of Over 1 kV and Low R} \times A," IEEE transactions on electron devices, vol. 57, no. 11, pp. 3050-3058, 2010-11,.

[47] A. Alian, R. Rodriguez, S. Yadav, U. Peralagu, A. Hernandez, P. V. M. Zhao, R. ElKashlan, B. Vermeersch, H. Yu and E. Bury, "Impact of channel thickness scaling on the performance of GaN-on-Si RF HEMTs on highly C-doped GaN buffer," in 52nd European Solid-State Device Research Conference (ESSDERC)-IEEE, Milan, 2022.

[48] A. Tajalli, M. Meneghini, S. Besendörfer, R. Kabouche, I. Abid, R. Püsche, J. Derluyn, S. Degroote, M. Germain, E. Meissner, E. Zanoni, F. Medjdoub and G. Meneghesso, "High breakdown voltage and low buffer trapping in superlattice gan-on-silicon heterostructures for high voltage applications," Materials, vol. 13, no. 19, pp. 4271,, 2020-09, Vol.13 (19).

[49] Q. Yu, S. Wu, M. Zhang, L. Yang, X. Zou, H. Lu, C. Shi, W. Gao, M. Wu, B. Hou, G. Qiu, X. He, X. Ma and Y. Hao, "The Effect of Channel Layer Thickness on the Performance of GaN HEMTs for RF Applications," Micromachines (Basel), vol. 16, no. 1, 2024-12.

[50] Y. Ikuhara, "Nanowire design by dislcoation technology," Progress in materials science, vol. 54, no. 6, pp. 770-791, 2009-08.

[51] D. Li, H. Chen, H. B. Yu, H. Q. Jia, Q. Huang and J. M. Zhou, "Dependence of leakage current on dislocations in GaN-based light-emitting diodes," Journal of applied physics, vol. 96, no. 2, pp. 1111-1114, 2004-07.

[52] M. Kaminski, S. Podsoadlo, K. Wozniak, L. Dobrzycki, R. Jakiela, A. Barcz, M. Psoda, J. Mizera, "Growth and structural properties of thick GaN layers obtained by sublimation sandwich method", Journal of Crystl Growth, vol 303, no 2, 395-399, 2007-05

[53] M. Barchuk. V. Holv, D. Rafaja, "Density of bunched threading dislocations in epitaxial GaN layers as determined using X-Ray diffraction.", Journal of applied physics, vol 123, no 16, Art.no. 161552, 2018.

[54] Y. Kamimura, T. Yokoyama, H. Oiwa, K. Edagawa, and I. Yonenaga, “Electrical conduction along dislocations in plastically deformed GaN,” IOP conference series. Materials Science and Engineering, vol. 3, no. 1, Art. no. 012010, 2009

[55] T. Yokoyama, Y. Kamimura, K. Edagawa, and I. Yonenaga, “Local current conduction due to edge dislocations in deformed GaN studied by scanning spreading resistance microscopy,” European physical journal. Applied physics, vol. 61, no. 1, Art. no. ap120318, 2013

5. Interplay between the Carbon doping concentration, threading dislocations and Dynamic R_{ON} in the C:GaN/AlN superlattice

5.1 Introduction

As an alternative, various strategies have been proposed to enhance epitaxial quality, including step-graded/single AlGaN layers [1] [4] [6], AlN/GaN or AlGaN/AlN superlattice (SL) buffers [7] [8] [9] [10] and multiple AlN nucleation layers [11]. GaN epitaxial layers grown on Si substrates typically experience tensile strain arising not only due to lattice mismatch but also from the large differences in the thermal expansion coefficient between GaN and Si. Incorporating a superlattice SRL, consisting of alternating layers of wide-bandgap materials, can introduce compressive strain to counteract this tensile strain [8].

Early research by Jakstas et al.[7] demonstrated that a buffer incorporating a SL structure enhances breakdown voltage, as the SL can sustain a higher electric field, twice that of the reference sample with no SL. However, the improvement of the SL also led to increased leakage currents. Their study compared two samples with identical top layers, one with an additional GaN layer and the other with an SL consisting of five pairs of AlGaN/GaN layers. The researchers attributed the increased leakage currents to a high density of TDDs, as the SL structure raised the TDD density by an order of magnitude. Similarly, Medjdoub et al. [1] reported that increasing the thickness of the AlGaN SRL enhances the breakdown voltage but with a minimal impact on the dynamic R_{ON}.

Tajalli et al. [14] compared substrate ramp results of carbon-doped SL SRLs and step-graded SRLs, concluding that the SL-based sample exhibited lower buffer trapping. They attributed this to C_N-related trap states [14], highlighting the importance of carbon concentration in SL structures. However, they also observed a reduction in trap signatures in wafers with SL buffers, likely due to either reduced vertical leakage or lower carbon incorporation. Heuken et al. [15] demonstrated a state-of-the-art SL SRL with a high breakdown voltage, achieved through intentional carbon doping. Their findings suggest that optimising SL growth conditions is crucial for reducing buffer trap densities, which play a significant role in dynamic R_{ON} degradation. Their results showed that the normalised conductivity of the carbon-doped SRL closely followed the capacitive coupling line, indicating minimal hysteresis, while the reference CGaN buffer exhibited stronger hysteresis and a greater deviation from the coupling line. While their work focuses on SL

structures, the reduction in trap-related degradation aligns with some of the findings discussed in this chapter. Ultimately, they emphasised that optimising SL growth conditions is key to reducing buffer trap densities, as dynamic R_{ON} degradation originates from buffer-related traps [15]. They also highlighted that a high-quality, highly resistive layer minimises buffer leakage, leading to improved dynamic R_{ON}.

A study by Lin et al. [3] further explored the effects of both positive and negative V_{SUB} on charge trapping and detrapping dynamics in AlGaN/GaN HEMTs with a 3.25 μm SL transition layer. Their research provided insight into why the SL structure is effective, observing an increase in ionised donor and acceptor concentrations under negative V_{SUB} of -200V, which alters the local electric field distribution and shifts the conduction and valence band energies. They concluded that electron injection into the buffer region during OFF-state high bias conditions is hindered due to the SRL. Specifically, in an AlN/GaN superlattice, the alternating layers create periodic potential barriers for electrons due to the conduction band offset between AlN and GaN. This effect will be further discussed in later sections.

Although the exact layer structure including the loop number of alternating III-N layers, and Al composition of the AlN/GaN SRL wafers used in this study has not been disclosed by the wafer supplier/manufacturer, previous research has explored the influence of SRL thickness, different III-N layer compositions [16], Al compositions, and SL pair counts [15] [17]. However, the impact of extrinsic doping on SL performance has been less extensively studied. The two wafers analysed in this chapter were grown under identical conditions, with the only difference being the carbon concentrations in the SRL.

To examine OFF-state trapping effects under the same negative V_{SUB} conditions as previous chapters, substrate ramp experiments were conducted alongside HRXRD to extract structural dislocation densities. The findings reinforce that neither total dislocation density nor any single type of dislocation is solely responsible for degradation; rather, the way dislocation cores are decorated plays a key role. Additionally, extrinsic carbon incorporation into the SL SRL primarily influences charge transport pathways rather than directly altering trap concentration.

5.2 Experimental Methods

5.2.1 Samples

The study was conducted on TLM structures fabricated on commercial GaN-on-Si epitaxial wafers, grown via MOCVD. Both wafers share a nominally identical layer structure, with the only difference being the carbon concentration in the superlattice (SL) strain relief layer (SRL), as shown in Figure 5.1, marked with a yellow dashed box. The epitaxial structure consists of a 140 nm AlN nucleation layer, a 3.3 µm AlN/GaN superlattice SRL, a CGaN layer, a UID GaN layer, a 20 nm AlGaN barrier layer with 20% Al composition, and a 3 nm undoped GaN cap. The intentional carbon doping concentration in the CGaN layer is 1 x 10^{19} cm^{-3}, while the background doping concentration in wafers C and D is 1 x 10^{16} cm^{-3}, respectively. Despite the difference in carbon doping concentration in the SL SRL, both wafers contain an identical number of SL pairs, however, the exact pair count has not been disclosed by the manufacturer.

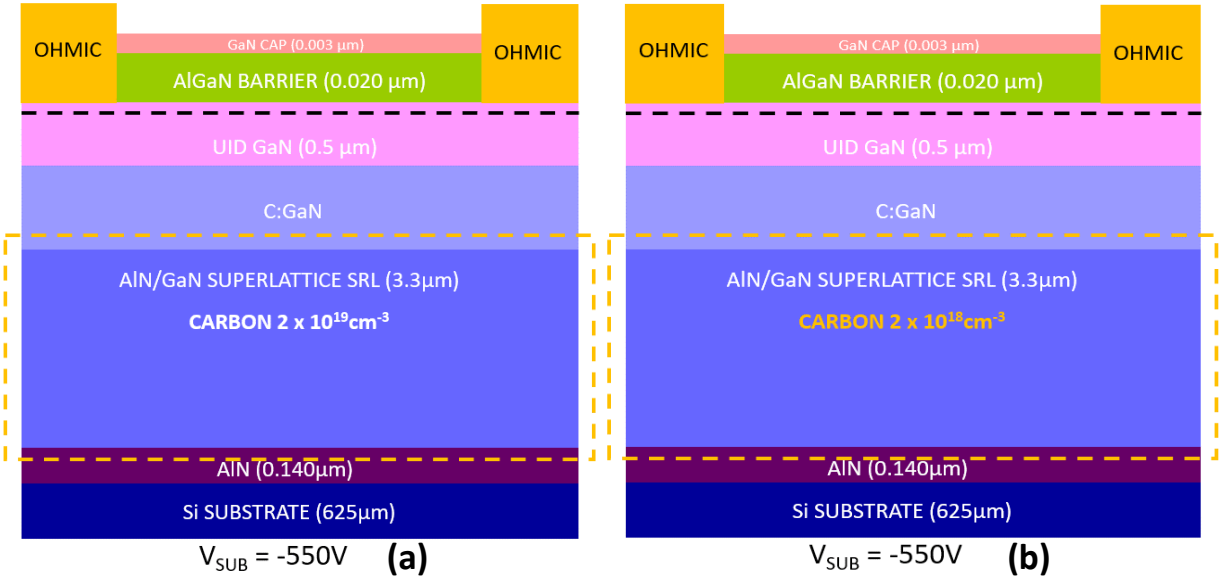

Figure 5-1 - Detailed epitaxial layer structures of (a) Wafer C and (b) Wafer D, highlighting the carbon doping concentration in the AlN/GaN superlattice strain relief layer.

All electrical measurements were conducted on linear, ungated TLM structures, as illustrated in Figure 2.17. The gap spacings ranged from 5 µm to 25 µm, while the width of the ohmic contacts remained constant at 100 µm. Ohmic contacts were formed using a Ti/Al/Ni/Au stack (20/40/120/25 nm) and annealed at 775°C in a nitrogen ambient, followed by the deposition of Ti/Au probe pads. The step-by-step fabrication process for the TLM structures is detailed in Chapter 2. The estimated 2DEG density for all wafers was 5 × 10^{12} cm^{-2}, with a sheet resistance R_{Sheet} of approximately 710 Ω/square.

5.2.2 Measurements Techniques

This study focuses on investigating the effect of carbon doping concentration in the AlN/GaN superlattice. Three characterisation techniques were employed: HRXRD, substrate ramp measurements and substrate transient measurements. The HRXRD rocking curve measurements and the extraction of the TDD have already been discussed in previous chapters and will not be reiterated here.

To ensure consistency, substrate ramp and substrate transient measurements were conducted following the same biasing conditions described in Chapter 3 (or as explained in Chapter 2). Substrate ramp measurements were performed over both low and high V_{SUB} regimes, while transient measurements included a stress phase followed by a recovery phase to track the charge dynamics.

All measurements were conducted at RT and in the dark, with multiple identical structures tested across the sample to account for wafer-level variations. Final analysis, the average results from 15 μm TLM structures, obtained from both substrate ramp and transient measurements, were used to highlight the differences between the samples.

5.3 Results

Table 5.1 presents the FWHM values of the symmetric (0002) and asymmetric (1 0 $\overline{1}$ 2) ω-scans for Wafer C and Wafer D. The corresponding screw (T_{screw}) and edge (T_{Edge}) dislocation densities were estimated using the equations outlined in Section 2.6.6. As observed in previous chapters, the edge dislocation density in both wafers remains higher than the screw dislocation density. However, in contrast to Wafer C, Wafer D exhibits an increase in the screw dislocation density by a factor of less than a twofold increase. This distinction highlights the impact of variations in the carbon doping concentration within the AlN/GaN superlattice strain relief layer on the dislocation characteristics of the wafers.

Wafer	**WAFER C**	**WAFER D**
SRL Carbon Doping (cm^{-3})	$2x10^{19}$	**$2x10^{18}$**
FWHM ω 002 (arc.sec)	603.4 ± 0.15%	793.4 ± 0.41%
FWHM ω 102 (arc. sec.)	1224 ± 0.23%	1373 ±0.24%
T_{screw} (cm^{-2})	7.31 x 10^{8}	1.26 x 10^{9}
T_{Edge} (cm^{-2})	6.01 x 10^{9}	6.65 x 10^{9}

Table 5.1 - FWHM of (002) and (102) reflections obtained from the HRXRD scans on Group A wafers

Figure 5.2 presents the normalised channel currents for the bi-directional substrate ramp sweeps of Wafer C and Wafer D, measured at a 15 μm TLM gap spacing. The V_{SUB} was swept from 0 V to -300 V and back, with the normalised channel currents plotted against V_{SUB}. The light grey dashed line represents the substrate threshold voltage (V_{TH}), also referred to as the capacitive coupling line. This line serves as a reference for an ideal scenario where no trapping occurs, and the structure behaves purely as a dielectric capacitor [22] [23]. Since both wafers have the same stack thickness, they share the same V_{TH} value of -428.7 V, as detailed in the equations in Chapter 2. For clarity, the solid line, marked with a downward arrow, represents the forward sweep (0 V to -300 V), while the dashed line indicates the return sweep. This convention will be consistently followed across all substrate ramp results.

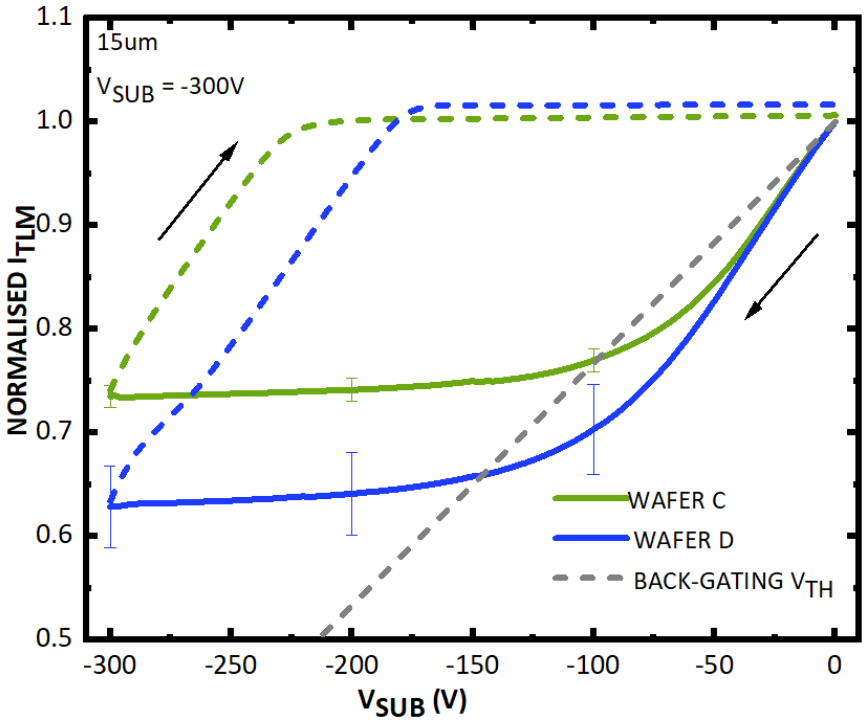

Figure 5-2 - Bi-directional substrate ramp characteristics on TLM with gap spacing 15 µm, of both wafers, at a sweep rate of 10 V/s. The forward sweep from 0V to -300 V and the return sweep are indicated by a solid and dashed arrows, respectively. The grey dashed line represents the capacitive coupling line. Determined error margins are ±1.32% and ±6.22% for Wafer C and Wafer D, respectively.

As shown in Figure 5.2, hysteresis was observed in both wafers during the substrate ramp sweeps at a 10 V/s. This behaviour aligns with previous reports on GaN-on-Si epitaxial structures with a CGaN layer, indicating the presence of trapping effects [18] [19] [24]. Notably, Wafer D exhibits a more pronounced trapping effect, as evidenced by the larger hysteresis compared to Wafer C. At low V_{SUB} (up to -20 V), the normalised channel currents of both wafers initially follow the capacitive coupling line before deviating below it. This deviation is attributed to charge redistribution within the CGaN layer, a phenomenon discussed in the previous chapters. The extracted g_m values are 0.0278 mS and 0.0281mS for Wafer C and Wafer D, respectively. As V_{SUB} continues to increase, channel current saturation is observed. Wafer C begins to reach saturation at approximately -80 V, whereas Wafer D requires a higher V_{SUB} of around -125 V to reach saturation.

Notably, the return sweep currents of Wafer D remained slightly higher than the initial 0V currents, indicating an increased 2DEG density compared to the forward sweep. In contrast, the return currents of Wafer C closely matched the initial currents at 0V, suggesting minimal change in 2DEG density.

The I_{SUB} during the forward sweep, presented in Figure 5.3 (a), exhibit a slightly higher leakage current for wafer D compared to that of wafer C, especially at V_{SUB} greater than -100 V. However, as shown in Figure 5.3(b), the return sweep leakage currents for both wafers remain comparable.

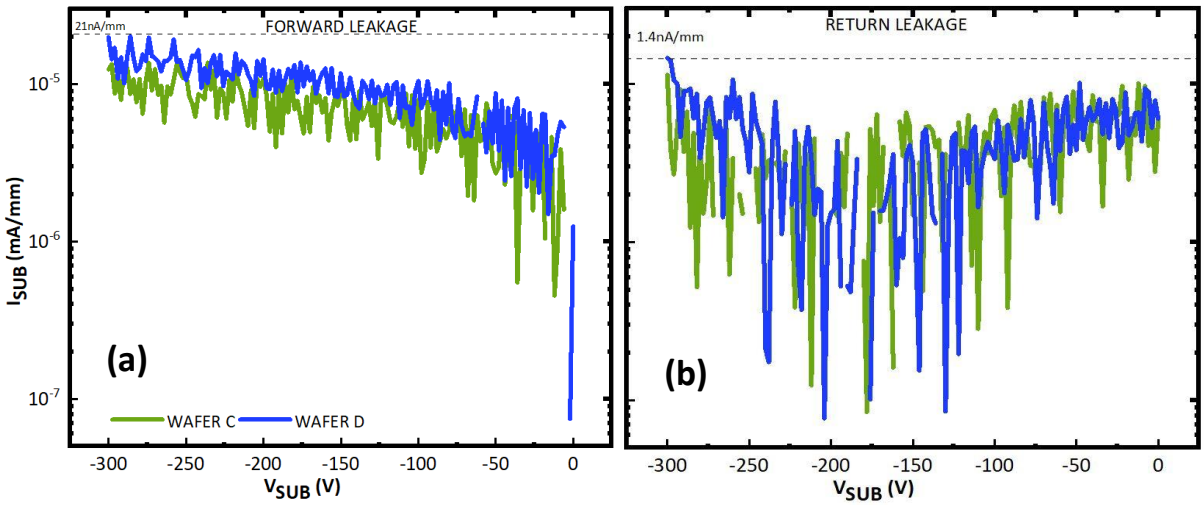

Figure 5-3 - Substrate leakage currents of the Bi-directional substrate ramp characteristics on TLM with gap spacing 15 µm, of both wafers, at a sweep rate of 10 V/s. (a) forward sweep from 0 V to -300 V and (b) return sweep.

Figure 5.4 presents the bidirectional substrate ramp characteristics for the 15 µm TLM structures of Wafer C and Wafer D as V_{SUB} was swept from 0 V to -550 V and back to 0 V. As previously discussed, understanding carrier transport at a high V_{SUB} of -550 V is essential, as it approaches the nominal breakdown voltage of 600 V for the epitaxy used in this study.

Unlike the behaviour observed at a moderate voltage of -300 V in Figure 5.2, significant changes in the channel current profile emerge, particularly as the currents no longer deviate below the capacitive coupling line at any point during the ramp. This suggests that, at higher voltages, the influence of charge redistribution within the CGaN layer differs from that at lower voltages. Interestingly, between -100 V and -150 V, the normalised channel currents decrease linearly with the V_{SUB}, following the capacitive coupling line, indicating that the leakage currents within the CGaN layer are now equivalent to the displacement currents [18] [23] [25].

At high voltages, the same positive charge storage trends can be observed up to the V_{SUB} of -250 V. This contrasts with Figure 5.2, where the positive charge storage persisted up to -300 V. Wafer C demonstrates the highest positive charge storage, whereas in Wafer D, the plateau region ceases at V_{SUB} = -250 V, where the channel currents begin to

decrease. For Wafer D, this marks the point where positive charge accumulation stops, and any remaining positive charge is retained within the system.

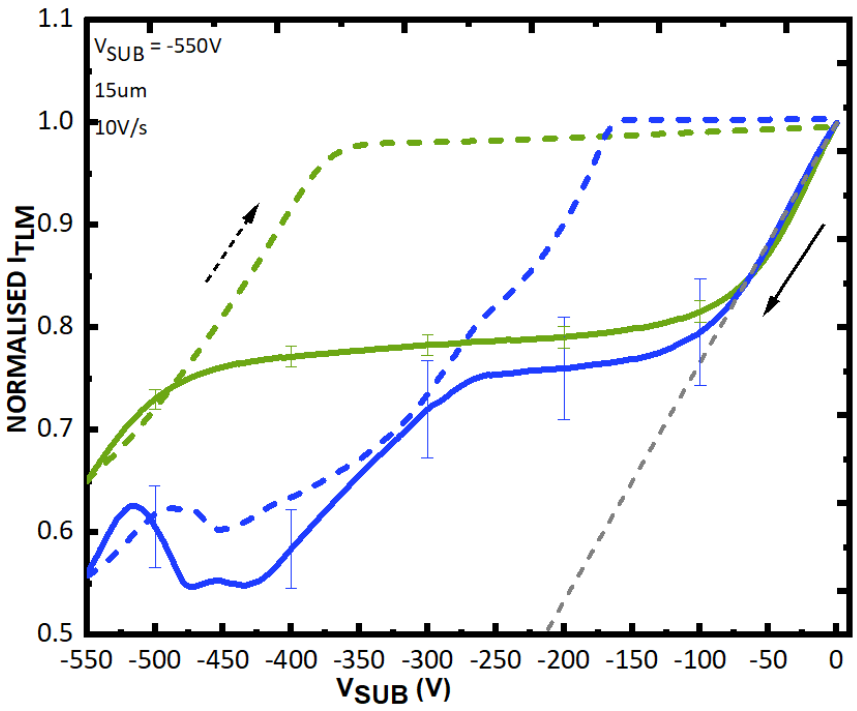

Figure 5-4 - Bi-directional substrate ramp characteristics on TLM with gap spacing 15 µm, of both wafers, at a sweep rate of 10 V/s. The forward sweep from 0V to -550 V and the return sweep are indicated by a solid and dashed arrows respectively. The grey dashed line represents the capacitive coupling line. Error margins were determined to be ±1.32% and ±6.58% for Wafer C and Wafer D, respectively.

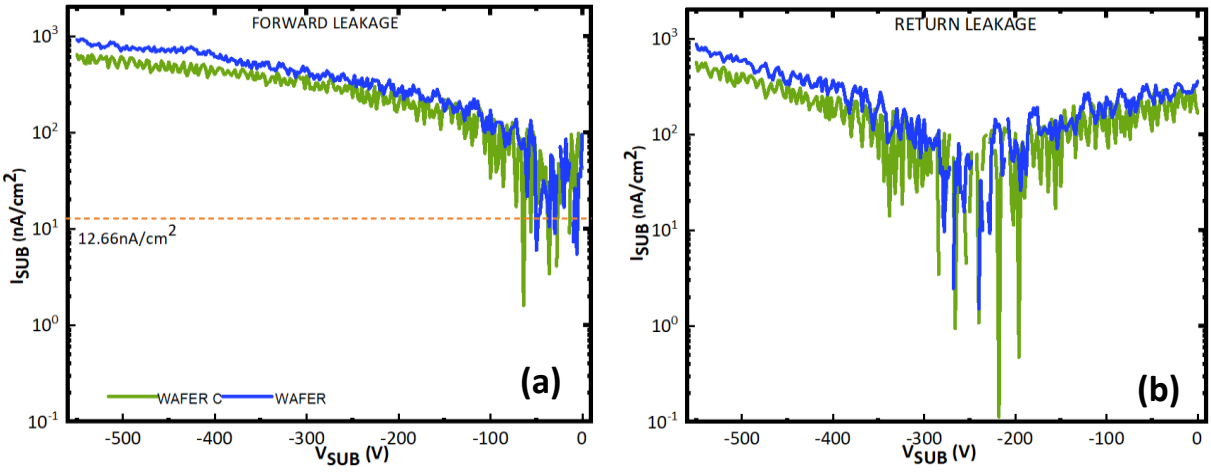

Figure 5-5 - Substrate leakage currents of the Bi-directional substrate ramp characteristics on TLM with gap spacing 15 µm, of both wafers, at a sweep rate of 10 V/s. (a) forward sweep from 0 V to -550V and (b) return sweep.

Figure 5.5 presents the I_{SUB} for both wafers during the forward sweep, where the substrate voltage was swept from 0 V to -550 V, as shown in Figure 5.5(a). Similar to the

leakage current trends observed in Figure 5.3(a), I_{SUB} for Wafer D remains consistently higher than that of Wafer C. However, beyond V_{SUB} = -250 V, the difference in leakage currents between the two wafers becomes more pronounced. This transition coincides with the shift from an initial noise-dominated leakage profile to a more well-defined current response, suggesting the onset of dominant charge transport mechanisms. Figure 5.5(b) shows the return sweep leakage currents, where both wafers exhibit comparable behaviour, suggesting that the asymmetry in leakage currents primarily occurs during the forward sweep.

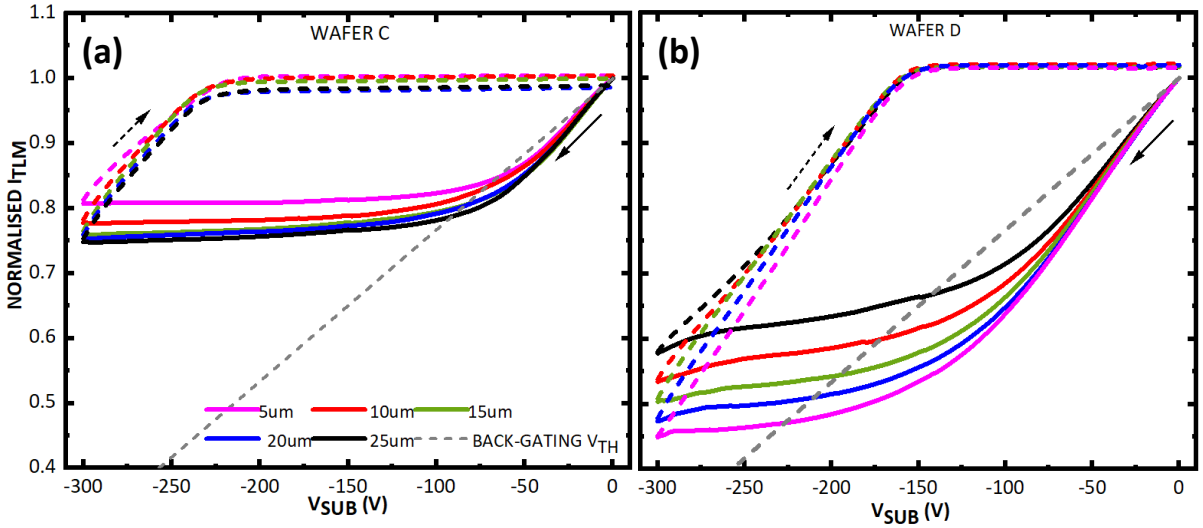

Figure 5-6 - Bidirectional substrate ramp characteristics of (a) Wafer C and (b) Wafer D, covering TLM gap spacings of 5, 10, 15, 20, and 25 µm. V_{SUB} was ramped from 0 V to -300 V, represented by the solid line, followed by the return sweep from -300 V back to 0 V. Error margins determined to be ±1.67% and ±5.71%

To further investigate the reasons behind the current collapse, additional measurements were conducted using different TLM gap spacings for both wafers. As observed in Figure 5.6(a), Wafer C exhibits no gap dependence, with similar hysteresis observed across all gap spacings. Alternatively, in contrast to Wafer C, Figure 5.6(b) shows that Wafer D exhibits increased hysteresis and a strong gap dependence.

Normalised backgating transient currents under negative V_{SUB} stress for Wafer C and Wafer D are presented in Figure 5.7. Figure 5.7(a) illustrates the stress phase, where the transient current response is measured during the application of V_{SUB} = -300 V, while Figure 5.7(b) corresponds to the recovery phase, observed after the substrate bias is reset to 0 V.

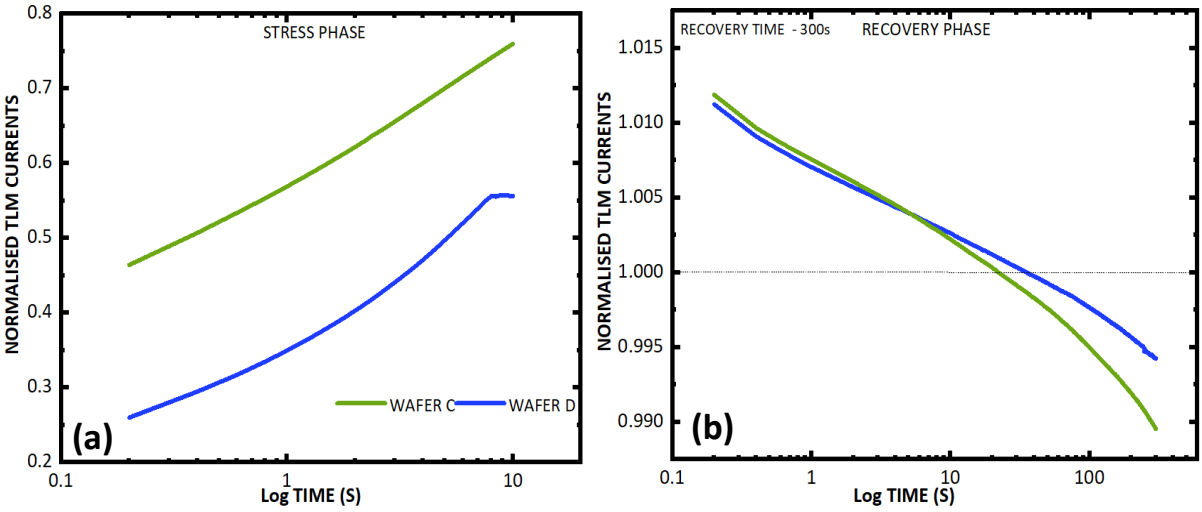

Figure 5-7 - Normalised channel currents for 15 µm TLM structures of Wafer C and Wafer D during the (a) stress phase and (b) recovery phase of the substrate transient measurements. A substrate voltage of -300 V was applied for 10 seconds, followed by a 300-second measurement of the channel current at 0 V after the bias was removed. Error margins were determined to be ±1.47% and ±3.13% for Wafer C and Wafer S, respectively.

Upon the application of an off-state stress V_{SUB} of -300 V, the normalised current levels are 0.55 for Wafer C and 0.25 for Wafer D, attributed to the backgating effect. In an ideal structure with no trapping, the channel currents should immediately drop to 0.3 upon being subjected to V_{SUB} = -300 V, as predicted by the theoretical backgating V_{TH} line. However, in both wafers, the current levels exceed this predicted value, indicating the presence of positive charge storage. Wafer D exhibits a stronger backgating effect compared to Wafer C, consistent with the behaviour observed in the substrate ramp measurements. Additionally, a positive-going current transient (i.e., increasing channel currents) is observed, suggesting continued accumulation of positive charge within the CGaN layer [26].

The negative-going (decreasing) recovery transient response, shown in Figure 5.7(b), was recorded after the V_{SUB} was reset to 0 V. Immediately upon the removal of the stress voltage, both wafers exhibit elevated channel currents, which exceed the 0 V equilibrium level and remain above the grey dashed line. This behaviour is a direct consequence of the backgating effect. Interestingly, the difference in initial current levels is minimal. In the absence of the substrate bias, a gradual decrease in channel currents is observed, signalling that the channel is returning to equilibrium. This reduction is primarily attributed to electron diffusion from the 2DEG into the CGaN, which plays a significant role in discharging the previously stored positive charge [26].

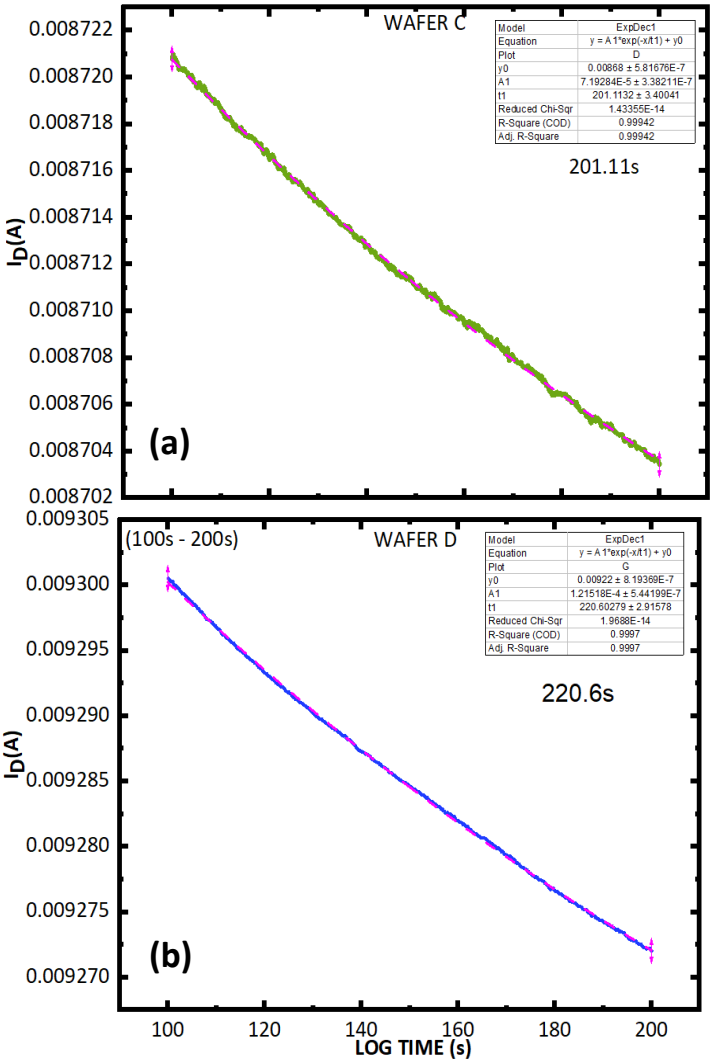

Figure 5-8 - Extracted time constants of the (a) Wafer C (b) Wafer D using the exponential curve fitting to the channel current decay. The fitted equation follows the $y = y_0 + Ae^{t/\tau}$

The ideal approach for extracting time constants from transient measurements involves selecting a fitting time frame that captures the dominant trapping behaviour while avoiding distortions from both very fast and very slow transients. As Bisi et al. [27] highlight, the early stage of a transient may be influenced by fast trapping, while the later stage could be dominated by slow-decaying components, which can artificially extend the extracted time constant. Therefore, it is crucial to select a fitting window that balances these effects, typically within the mid-range of the transient. However, a single fitting time frame cannot be universally applied across all studies. The optimal time range depends on the specific trap dynamics of each wafer set, meaning that different studies within this thesis may use different fitting windows. The chosen time frame for this study is 100 s to 200 s, as it provides the best overall fit for all wafers involved in this analysis (Figure 5.8). This variability must be acknowledged to ensure valid comparisons between

each dataset. By carefully selecting time frames suited to the specific dynamics of each case, a more accurate and representative analysis of transient behaviour is achieved.

The extracted time constants for Wafer C and Wafer D are 201.11 ±2.915s and 220.6 ± 3.401s, respectively, indicating that Wafer C recovers slightly faster than Wafer D.

As shown in Figure 5.7, the current transient exhibits different time constants across various time ranges. One might question whether the observation from the 150 s–250 s window still holds. For instance, in the 10 s–50 s range, the extracted time constants are 25.58 s for Wafer C and 28.21 s for Wafer D. This confirms that the overall trend remains consistent.

To gain insights into the trapping and detrapping dynamics influenced by varying carbon doping concentrations in the SRL, experimental results were complemented with TCAD simulations to better understand the mechanisms behind the observed dynamic R_{ON} behaviour. As shown in Figure 5.2, the substrate ramp measurements capture a clear difference between Wafers C and D, exhibiting distinct saturation behaviours, where Wafer C reaches saturation at a lower substrate bias than Wafer D.

The simulation results capture this behaviour, demonstrating how SRL resistivity influences both charge accumulation and leakage pathways. However, while the overall behaviour aligns well with experimental observations, some deviations are present. These discrepancies arise primarily due to limitations in simulating dislocation-assisted vertical leakage pathways and the fact that the superlattice structure itself was not explicitly modelled. A more detailed comparison between experimental and simulated results, along with discussions on these differences, is provided in the following section.

5.4 Substrate Ramp Simulation

As this chapter focuses on the superlattice SRL layers, it is important to note that, for simplicity, the SRL is modelled as a carbon-doped, Al-rich AlGaN layer rather than an explicit superlattice. The model assumes a carbon concentration of 2×10^{19} cm^{-3} and 2×10^{18} cm^{-3} in the SRL, representing Wafer C and Wafer D, respectively. The parameters used in this model have been discussed in previous chapters.

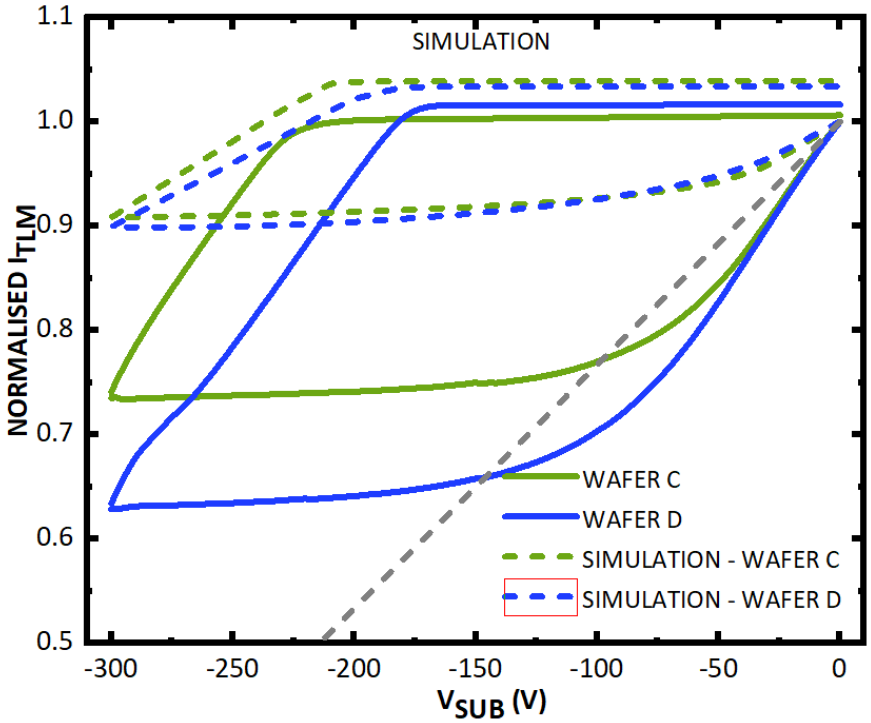

Figure 5-9 - Simulated substrate ramps for Wafers C and D, compared with experimental measurements at a ramp rate of 10 V/s. The green and blue lines correspond to Wafers C and D, respectively, while the small, dashed lines indicate their simulated counterparts. The solid black arrow denotes the forward sweep (0 V to -300 V), and the dashed black arrow represents the return sweep (-300 V to 0 V).

As shown in Figure 5.9, the simulation qualitatively captures the trends observed in the experimental substrate ramp measurements. Both experimental and simulated curves exhibit hysteresis, a key characteristic of charge trapping and detrapping dynamics, confirming that trapping occurs within both structures. The saturation behaviour is also reflected, with Wafer C saturating earlier than Wafer D, suggesting that the model partially accounts for the role of SRL carbon in charge accumulation.

However, some discrepancies are evident. In the experimental substrate ramp curves, between 0 to -80 V region of Wafer C and the 0V to -150V region of Wafer D, the current initially decreases more rapidly, appearing right-shifted from the capacitive coupling line.

In contrast, the simulation shows both decreasing curves positioned on the left-hand side, likely indicating that electron trapping in carbon acceptors, previously discussed as charge redistribution phenomena within the CGaN layer, occurs at a different capture rate in the model [18]. As discussed in Chapter 3, charge redistribution in the CGaN layer arises from various mechanisms, including hopping conduction, Poole-Frenkel (PF) emission, or tunnelling effects [21] [28]. One or multiple of these mechanisms may be responsible, but whichever is dominant, the model fails to capture these behaviours accurately. Since these mechanisms are absent in the simulation, the model fails to capture the leakage currents within the CGaN layer, leading to the observed mismatch between simulation and experimental results.

Additionally, the simulated curves saturate at a higher normalised current compared to the experimental results, in contrast to the experimental results, where saturation occurs at much lower values.

Figure 5.10(a) – (d) compare the simulated conduction band energy, vertical electric field at the UID/CGaN interface, hole density, and space charge region at the UID/CGaN and CGaN/SRL interfaces for Wafers C and D at V_{SUB} = -300 V. This voltage point corresponds to the plateau region at -300 V in the substrate ramp graph (Figure 5.8).

Under a negative V_{SUB} of -300 V, as expected, both wafers exhibit upward band bending. Despite having the same CGaN layer doping concentration, Wafer D shows a more pronounced upward band bending than Wafer C, as seen in Figure 5.10 (a) [29]. Figure 5.10 (b) presents the corresponding vertical electric field distribution and space charge region at the UID/CGaN interface. A relaxation of the peak electric field is observed for Wafer C, while Wafer D exhibits a more pronounced electric field.

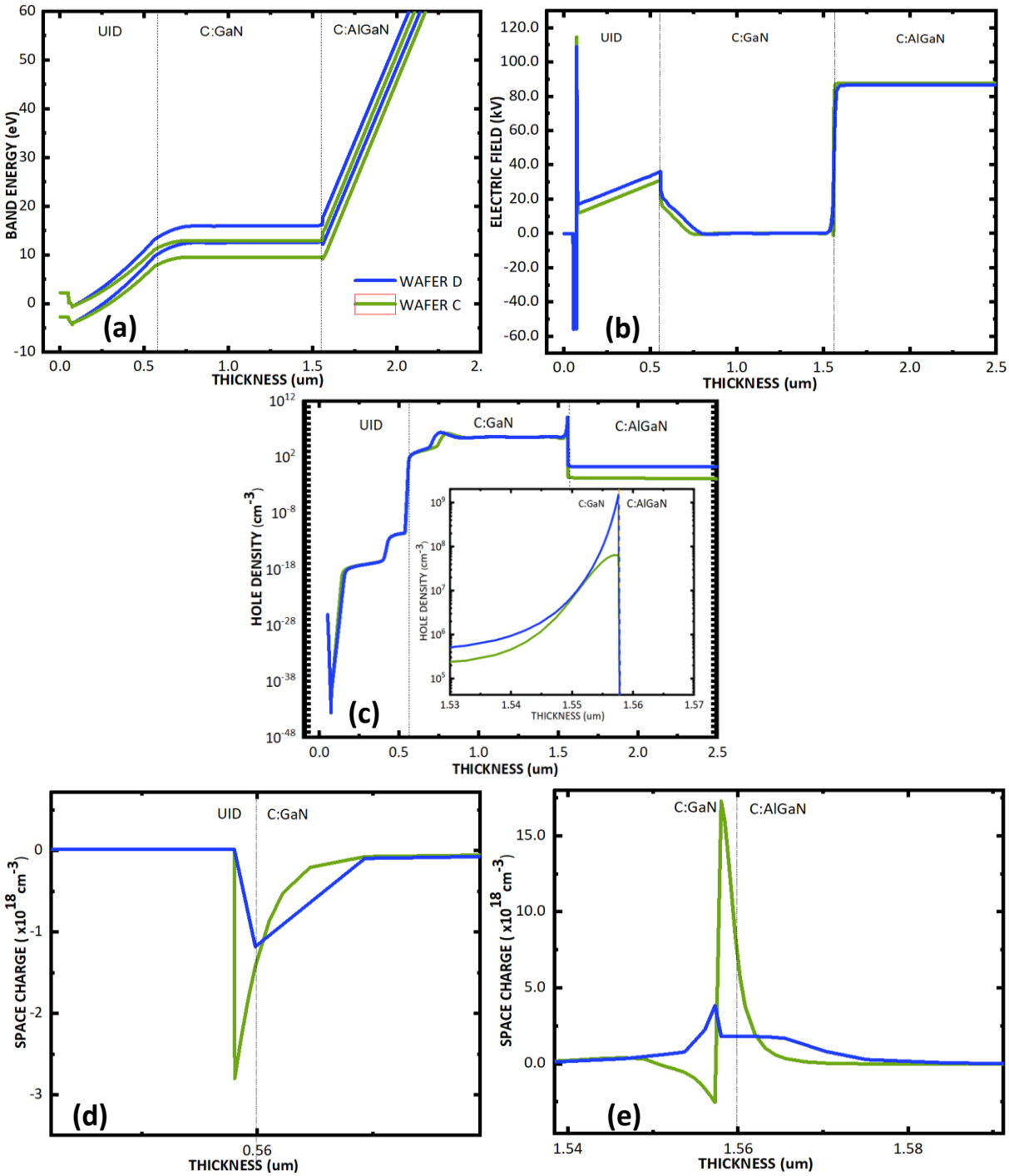

Figure 5-10 - Comparison between the simulated (a) conduction band energy (b) electric field at the UID/CGaN heterojunction (c) hole density (d) the space charge region at the at the UID/CGaN heterojunction and (e) the space charge region at the CGaN/SRL heterojunction of Wafer C and Wafer D, at V_{SUB} = -300 V.

It is important to reiterate that a significant charge resides in the depletion regions at the UID/CGaN interface, as previously highlighted. This is attributed to charge redistribution and current flow within the CGaN, leading to negative charge

accumulation at the top of the CGaN and positively charged ionised donors at the bottom, forming a dipole [18] [28]. However, the depletion region at the UID/CGaN interface, as seen in Figure 5.10 (d), exhibits a notable contrast: Wafer C has a thinner depletion region compared to Wafer D. This suggests that the density of ionised acceptors at the top of the CGaN region is higher in Wafer C than in Wafer D. Similarly, the depletion region at the CGaN/SRL interface, shown in Figure 5.10 (e), reveals striking differences between the two wafers. Wafer C forms a P/P++ junction, whereas Wafer D forms a P++/P junction.

Figure 5.10(c) illustrates the hole density as a function of depth along the vertical cutline, representing all layers in the stack. This highlights hole accumulation at the CGaN/AlGaN interface. Notably, Wafer D exhibits a higher CGaN hole density, approximately an order of magnitude greater than that of Wafer C.

Focusing on the -300V bias point of the simulated substrate ramp curves illustrated in Figure 5.8, where saturation is observed, the underlying mechanism can be summarised as follows:

As previously explained, this phenomenon occurs only if the resistivity of the UID layer is lower than that of the CGaN, allowing electrons to leak into the 2DEG and enabling hole accumulation at the bottom of the CGaN. This has been attributed to trap-assisted tunnelling or hopping along dislocations, as discussed in [18] [28] [29]. These accumulated holes can either neutralise the ionised acceptors at the top of the CGaN or remain as free charge. Overall, this positive charge screens the 2DEG from the applied negative V_{SUB}, causing the 2DEG to remain independent of the negative bias.

As indicated in Figure 5.10(b), the higher observed positive charge storage in Wafer C likely reduces the electric field across the UID region. This is attributed to the electrons leaking into the 2DEG through p-shorts under the ohmic contacts in the simulations.

The electric field distribution in the SRL of Wafer C appears higher than that of Wafer D. This could be attributed to the differences in the SRL resistivity, which can be explained using the " leaky dielectric model". This model [18] provides a useful framework for understanding how voltage is distributed across different layers in these structures.

In this model, the epitaxial stack is represented as a parallel resistor-capacitor (RC) network, where each layer is modelled as a combination of a capacitor accounting for displacement currents and a resistor representing leakage conduction through defects, traps, or impurities [28]. This forms a potential divider, with the voltage drop across each

layer depending on its resistivity. For Wafer C, the measured electric field (E = V/d) as shown in Figure 5.10(b) suggests a higher voltage drop across the SRL compared to Wafer D, despite both having the same SRL thickness. This indicates that the SRL in Wafer C has a higher resistivity, leading to a greater proportion of the applied voltage dropping across it, thereby increasing the local electric field. Conversely, the lower SRL resistivity in Wafer D results in more voltage being distributed across the upper GaN layers, modifying the overall field distribution. Hence, this distinction in electric field distribution could potentially be linked to the incorporated carbon doping concentration in SRL.

Interestingly, while Wafer D exhibits a higher overall hole density than Wafer C at CGaN/C:AlGaN interface (Figure 5.10 (c)), even though the substrate ramp curve indicates lower positive charge storage, which appears contradictory. The depletion regions at both the top (Figure 5.10(d)) and bottom of the CGaN (Figure 5.10(e)) differ significantly between the two wafers, suggesting that charge distribution follows a different pattern in Wafer D. Based on the depletion region profile at the UID/CGaN interface, it is likely that Wafer D contains a lower density of positively charged ionised donors at the CGaN/SRL interface. This implies that there are fewer fixed positive charges available to screen the negative – V_{SUB}.

5.5 Discussion

Table 5.1 presents the FWHM values of the symmetric (0002) and asymmetric (1 0 $\bar{1}$ 2) ω-scans for Wafer C and Wafer D. The total TDD increases monotonically as the SRL carbon concentration decreases. Specifically, when the carbon concentration in the SRL is reduced to 2 x 10^{18} cm^{-3}, which is 10% of the doping concentration in the reference Wafer C, the total TDD increases by 17.35%. Additionally, the density of screw dislocations rises by an order of magnitude.

In many previous studies [35] [41], higher carbon concentrations have been linked to increased threading dislocation densities, ultimately deteriorating crystal quality, irrespective of whether it is in C:GaN or AlN/GaN SL. However, both Chapter 3 and this chapter present evidence that carbon incorporation has improved crystal quality by reducing the TDD. Notably, Wafer C, with a higher carbon doping in the SRL, exhibits lower TDD, likely due to carbon-related defect complexes alleviating strain accumulation and promoting defect clustering. Regardless of discrepancies between this study and others, it is evident that carbon incorporation is closely related to the formation of TDs. Dislocations play a crucial role in both electrical and structural properties, and as concluded in Chapter 3, the interaction between carbon incorporation and dislocation density affects both vertical leakage current and charge trapping dynamics, influencing overall device performance.

The comparison of substrate ramp sweeps for Wafer C and Wafer D, following the adjustment of carbon doping concentration in the SRL (Figure 5.2), reveals that both normalised channel currents deviate below the capacitive coupling line, as the transconductance is greater than the capacitive coupling line. As discussed in Chapter 3, during the charge redistribution phase, leakage currents within the C:GaN layer exceed displacement currents, leading to an increase in transconductance [18] [23], which is attributed to an increasing number of ionised acceptor traps [3]. Notably, in the voltage range of 0 V to -30 V, both wafers exhibit overlapping normalised currents, indicating that their transconductance is nearly identical. This is further reflected in the extracted transconductance values of 0.0278 mS for Wafer C and 0.0281 mS for Wafer D. Ultimately, this also suggests that the charge redistribution behaviour in both wafers is also largely similar at this voltage range.

As both wafers have a similar C:GaN layer, it can be speculated that whichever is the dominant charge transport mechanism during the charge redistribution phase, at low V_{SUB}, is similar in both cases. Although this work does not provide conclusive evidence of the exact dominant mechanism, Watch et al. [28] suggest that the charge redistribution phase can be best described by 3D range hopping.

Following charge redistribution, current saturation is observed beyond $V_{SUB} = -100$ V for Wafer C, whereas Wafer D reaches saturation at $V_{SUB} = -150$ V. This indicates that charge transport between the UID and C:GaN layer occurs at a lower voltage in Wafer C compared to Wafer D. This behaviour is likely attributed to the electric field distribution across each layer, which can be well explained using the simulated electric field distribution shown in Figure 5.10(b). As discussed in previous chapters, during current saturation, the resistivity of the UID layer should be lower than that of the C:GaN layer [18] [23]. In Wafer C, the stronger electric field in the SRL, resulting from the higher potential drop (E=V/d), leads to a lower voltage drop across the top layers. Conversely, in Wafer D, the voltage drop across the SRL is lower, resulting in a comparatively higher voltage drop across the top layers. This effect is clearly reflected in the electric field distribution at the UID region.

Figure 5.6 presents substrate ramp measurements for varying gap spacings. Wafer C exhibits gap-independent behaviour (Figure 5.6(a)), whereas Wafer D shows a more pronounced gap dependence (Figure 5.6(b)). As discussed in Chapters 3 and 4, the gap-independent behaviour of Wafer C suggests that vertical leakage path along the dislocations is the dominant transport mechanism across the entire ohmic gap spacing. In contrast, the gap dependence observed in Wafer D indicates that lateral leakage plays a more significant role in charge transport.

In Chapter 4, the TEM image of Wafer C revealed that the majority of TDs propagating from the bottom layers to the top layers were annihilated at the top of the SRL, specifically at the SRL side of the C:GaN/SRL heterojunction. However, as no TEM imaging is available for Wafer D, it is difficult to determine whether this dislocation annihilation within the SRL is directly attributed to the higher carbon concentration or how it induces the lateral leakage path. Interestingly, despite the overall increase in total TD density, there is a notable increase, by an order of magnitude, in the density of screw dislocations as carbon concentration decreases. Ramdani et al. [12] concluded based on their experiments and previous studies that carbon plays a crucial role in influencing

dislocation behaviour, affecting whether dislocations bend, recombine to form buried loops, or continue propagating through the epitaxial layers. Hence, the substrate bias gap dependency observation clearly suggests that the presence of carbon in the SRL impacts the lateral resistivity of epitaxy, inducing lateral leakage rather than a vertical leakage path. This aligns with the observations in Chapter 3, where the wafer with the lowest carbon concentration of 2 x $10^{18}cm^{-3}$, in the C:GaN layer, exhibited a dominant lateral leakage path, resulting in gap dependency.

Figure 5.3(a) and (b) illustrate the I_{SUB} when the substrate was ramped from 0 V to -300 V and back. Wafer D exhibits a relatively higher I_{SUB} compared to Wafer C, which is likely attributed to the increased SRL resistivity suppressing the leakage currents. Heuken et al. [36] investigated the effect of varying carbon concentrations in AlGaN/AlN from 3.8×10^{18} cm^{-3} to 1.7×10^{18} cm^{-3}, using substrate ramp measurements. Their findings showed that higher-carbon samples exhibited smaller hysteresis and remained closer to the capacitive coupling line, whereas lower-carbon samples displayed increased hysteresis and a stronger deviation. This behaviour was attributed to the suppression of charging and discharging paths at higher carbon concentrations. Additionally, they observed that higher-carbon samples had lower buffer leakage compared to lower-carbon samples. This trend is consistent with the observations here (Figure 5.3a), where lower-carbon Wafer D exhibits stronger leakage characteristics.

Figure 5.4 presents the substrate ramp measurements up to $V_{SUB} = -550$ V, illustrating the effects of high-voltage exposure. Wafer D exhibits a decrease in channel current at approximately −250 V, suggesting electron injection from the substrate at a lower V_{SUB}, which further depletes the 2DEG [47] [48]. In contrast, Wafer C maintains current saturation up to $V_{SUB} = -475$ V. This trend is highlighted in Figure 5.5(a), where a noticeable increase in I_{SUB} beyond −250 V indicates enhanced substrate leakage of Wafer D.

The earlier onset of electron injection in Wafer D could be primarily attributed to the lower SRL resistivity, resulting from its lower carbon doping concentration. Alternatively, this behaviour may be a combined effect of both low resistivity and threading dislocation-induced leakage paths, facilitating electron injection into the CGaN layer. In contrast, the SRL in Wafer C, with higher carbon content and lower dislocation density, may serve to mitigate this effect, thereby reducing substrate leakage.

Another possible explanation for this behaviour is that the increased negative V_{SUB} raises the energy barrier of the Si sufficiently for electrons to accumulate at the Si substrate/AlN nucleation layer interface at lower V_D. As discussed by Li et al. [3], further increasing the V_{SUB} or drain bias can enhance band bending, increasing the energy barrier. Joh et al. [49] proposed a related hypothesis that hot electrons may be injected into the SRL under high bias. If carrier generation in the Si substrate dominates the current-limiting process, the rate at which these electrons enter the C:GaN region is likely dictated by the density of dislocations and impurity segregation, which enhance leakage paths [50] [51]. Once electrons overcome the AlN energy barrier, they gain sufficient energy to inject into the superlattice transition layer, resulting in an increase in electron injection into the C:GaN region. This leads to the observed decrease in normalised channel current (Figure 5.5) and increased leakage across all bias conditions [3] [52].

An alternative explanation considers inhomogeneities in dopant distribution and dislocation density within the SRL. Edge dislocations may act as electron traps, capturing carriers injected from the substrate and accumulating them at the top of the strain relief layer as negatively charged acceptors [38] [53]. While edge dislocations contribute minimally to relieving lattice or thermal mismatch [54] [55] [56], under high bias conditions, they can behave as negatively charged acceptors, potentially influencing the observed electrical behaviour [42].

Interestingly, while some studies, such as [47], observed no pronounced trapping effects even at $V_{SUB} = -1300$ V during bi-directional substrate ramp sweeps, attributing this to lower carbon incorporation in the SL buffer. The findings in this chapter suggest a different mechanism in play. Overall, the low I_{SUB} of 21nA/mm as shown in Figure 5.3(a), observed for both wafers during the forward sweep, further supports the idea that the AlN/GaN SRL provides superior voltage-blocking properties even with low carbon concentration at low V_{SUB} of -300V. More crucially, to suppress dynamic R_{ON}, the key factor is how efficiently the epitaxy can discharge trapped charge.

This was verified through substrate transient measurements, as shown in Figure 5.7(b), where Wafer C exhibited a faster recovery than Wafer D, with time constants of 201.11 s and 220.6 s, respectively. The difference in time constants could likely be attributed to the dominant leakage pathway. Specifically, in Wafer C, vertical leakage across the gap spacing results in a relatively faster recovery, whereas Wafer D exhibits a dominant lateral leakage path beneath the contacts, leading to a slower recovery.

These findings also suggest that regardless of impurity decoration at the dislocation core, TDs inherently function as microscopic leakage pathways [35]. Consequently, an increased TD density enhances these leakage paths, potentially impacting the high-voltage performance of Wafer D.

5.6 Conclusion

This study examined the impact of carbon doping concentration in the SRL on the dynamic R_{ON} of MOCVD-grown AlGaN/GaN HEMTs. Experimental results, supported by HRXRD, substrate ramp, transient measurements, and simulations, indicate that increased carbon doping improves vertical isolation and reduces trapping effects, thereby enhancing device recovery.

The observed increase in both FWHM (0002) and (1 0 $\overline{1}$ 2) suggests a correlation with the carbon concentration in the SRL, as discussed in Chapter 3. This chapter further reinforces the influence of carbon concentration on TDD density, with HRXRD analysis indicating improved crystal quality in Wafer C compared to Wafer D. Despite both wafers having similar carbon concentration in their CGaN layers, variations in screw dislocation density by an order of magnitude highlight the impact of carbon on lattice distortion and defect behaviour.

However, several uncertainties remain, including the precise number of AlN/GaN pairs. This study highlights the following key findings:

At 0 V – 30 V, the overlapping normalised currents suggest that charge redistribution at low voltages is independent of the SRL carbon doping concentration.

The lower positive charge storage in Wafer D can be attributed to an enhanced lateral leakage path, whereas Wafer C exhibits a more pronounced vertical leakage path across the ohmic gap, facilitating greater electron leakage into the 2DEG.

Simulated electric field analysis indicates that a highly resistive SRL leads to a larger potential drop across the SRL, thereby reducing the electric field in the upper layers of the device. This suggests that carbon doping plays a key role in modulating electric field distribution and, consequently, leakage behaviour.

Unlike Wafer C, Wafer D demonstrates gap dependency, which is attributed to carbon-induced lateral leakage. However, the precise mechanism responsible for this lateral leakage remains unclear. Further experimental investigation is required.

Substrate transient measurements indicate that increasing the carbon doping concentration to 2×10^{19} cm^{-3} accelerates device recovery. Wafer C, with a dominant vertical leakage path, recovers faster, while Wafer D, exhibiting lateral leakage, shows prolonged recovery and increased dynamic R_{ON}.

Electron injection from the substrate occurs at -250V for Wafer D, while for Wafer C, it occurs at -475V. This is likely due to the lowered resistivity of the SRL in Wafer D, coupled with a higher density of threading dislocations (TDs).

Minimising current collapse in a HEMT involves reducing the electric field in the top layers, ensuring the majority of the electric field is dropped at the device's bottom region. As the simulation highlights, highly resistive SRL certainly help reduce the electric field in the top layers, particularly the UID and the channel region. Therefore, selecting the optimal carbon concentration in the SRL is critical, as it influences dislocation formation and leakage paths. The best trade-off between breakdown voltage, dynamic R_{ON} and leakage currents depends on the specific application requirements.

5.7 References

[1] F. Medjdoub, J. Derluyn, K. Cheng, M. Leys, S. Degroote, D. Marcon, D. Visalli, M. Van Hove, M. Germain and G. Borghs, "Low On-Resistance High-Breakdown Normally Off AlN/GaN/AlGaN DHFET on Si Substrate," IEEE electron device letters, , Vol, p.111-113, Article 5378574, vol. 31, no. 2, pp. 111-113, 2010-02.

[2] K. J. Chen, O. Haberlen, A. Lidow, C. L. Tsai, T. Ueda, Y. Uemoto and Y. Wu, "GaN-on-Si Power Technology: Devices and Applications," IEEE transactions on electron devices, vol. 64, no. 3, pp. 779-795, 2017-03.

[3] Y. Lin, M.-L. Kao, Y.-C. Weng, C.-F. Dee, S.-C. Chen, H.-C. Kuo, C.-H. Lin and E.-Y. Chang, "Buffer Traps Effect on GaN-on-Si High-Electron-Mobility Transistor at Different Substrate Voltages," Micromachines (Basel), vol. 13, no. 12, p. 2140, 2022-12.

[4] H.-P. Lee, J. Perozek, L. D. Rosario and C. Bayram, "Investigation of AlGaN/GaN high electron mobility transistor structures on 200-mm silicon (111) substrates employing different buffer layer configurations," Scientific reports, vol. 6, no. 1, pp. 37588-37588, 2016-11.

[5] T. Hamachi, T. Tohei, Y. Hayashi, M. Imanishi, S. Usami, Y. Mori and A. Sakai, "Comprehensive analysis of current leakage at individual screw and mixed threading dislocations in freestanding GaN substrates," Scientific reports, vol. 13, no. 1, pp. 2436-2436, 2023-02.

[6] Y. Yao, S. Huang, Q. Jiang, X. Wang, L. Bi, W. Shi, F. Guo, T. Luan, J. Fan, H. Yin, K. Wei, Y. Zheng, J. Shi, Y. Li, Q. Sun and X. Liu, "Identification of Semi-ON-State Current Collapse in AlGaN/GaN HEMTs by Drain Current Deep Level Transient Spectroscopy," IEEE electron device letters, vol. 43, no. 2, pp. 200-203, 2022-02.

[7] V. Jakštas, V. Janonis, A. Bi i nas, R. Aleksiej nas, A. Kadys, T. Malinauskas and I. Kašalynas, "Impact of a superlattice on electrical properties of AlGaN GaN sapphire 2DEG structures," Journal of Physics: Conference Series, vol. 647 , no. 1, p. 12055, 2015-10.

[8] T. Egawa, "Heteroepitaxial growth and power electronics using AlGaN/GaN HEMT on Si," in International Electron Devices Meeting 2012 , Nagoya, 2012.

[9] P. Xu, Y. Jiang, Y. Chen, Z. Ma, X. Wang, Z. Deng, Y. Li, H. Jia, W. Wang and H. Chen, "Analyses of 2-DEG characteristics in GaN HEMT with AlN/GaN super-lattice as barrier layer grown by MOCVD," Nanoscale research letter, vol. 7 , no. 1, pp. 141-141, 2012-02.

[10] F. Benkhelifa, S. Müller, V. M. Polyakov, S. Breuer, H. Czap, C. Manz, M. Mikulla and O. Ambacher, "Vertical Buffer Leakage and Temperature Effects on the

Breakdown Performance of GaN/AlGaN HEMTs on Si Substrate," ECS Transactions, vol. 69, no. 11, pp. 65-70, 2015-09.

[11] M. Zhu, G. Li, H. Li, Z. Guo, Y. Yang, J. Shang, Y. Feng, Y. Lu, Z. Li, X. Li, F. Gao, W. Wei and S. Li, "Challenges and advancements in p-GaN gate based high electron mobility transistors (HEMTs) on silicon substrates," Journal of materials chemistry. C, Materials for optical and electronic devices, , Vol.12 (4), p, vol. 12, no. 4, pp. 16272-16293, 2024-10.

[12] M. Ramdani, M. Chmielowska, Y. Cordier, S. Chenot and F. Semond, "Effect of carbon doping on crystal quality, electrical isolation and electron trapping in GaN based structures grown silicon substrates," Solid-State Electronics, vol. 75, pp. 86-92, 2012-09.

[13] M. Cioni, A. Chini, N. Zagni, G. Verzellesi, G. Giorgino, G. Cappellini, C. Miccoli, G. Toulon, T. Wakrim, M. Eloisa Castagna, A. Constant and F. Iucolano, "On the Dynamic RON, Vertical Leakage and Capacitance Behavior in pGaN HEMTs With Heavily Carbon-Doped Buffers," IEEE electron device letters, vol. 45, no. 8, pp. 1437-1440, 2024-08.

[14] A. Tajalli, M. Meneghini, S. Besendörfer, R. Kabouche, I. Abid, R. Püsche, J. Derluyn, S. Degroote, M. Germain, E. Meissner, E. Zanoni, F. Medjdoub and G. Meneghesso, "High breakdown voltage and low buffer trapping in superlattice gan-on-silicon heterostructures for high voltage applications," Materials, vol. 13, no. 19, pp. 4271,, 2020-09, Vol.13 (19).

[15] L. Heuken, M. Kortemeyer, A. Ottaviani, M. Schroder, M. Alomari, D. Fahle, M. Marx, M. Heuken, H. Kalisch, A. Vescan and J. N. Burghartz, "Analysis of an AlGaN/AlN Super-Lattice Buffer Concept for 650-V Low-Dispersion and High-Reliability GaN HEMTs," IEEE transactions on electron devices, vol. 67, no. 3, pp. 1113-1119, 2020-03.

[16] H. Itakura, T. Nomura, N. Arita, N. Okada, C. M. Wetzel, T. P. Chow and K. Tadatomo, "Effect of InGaN/GaN superlattice as underlayer on characteristics of AlGaN/GaN HEMT," AIP advances, vol. 10, no. 2, pp. 025133-025133-5, 2020-02.

[17] S. Moench, S. Müller, R. Reiner, P. Waltereit, H. Czap, M. Basler, J. Hückelheim, L. Kirste, I. Kallfass, R. Quay and O. Ambacher, "Monolithic Integrated AlGaN/GaN Power Converter Topologies on High-Voltage AlN/GaN Superlattice Buffer," Physica status solidi. A, Applications and materials science, vol. 218, no. 3, p. 2000404, 2021-02.

[18] M. Uren, S. Karboyan, I. Chatterjee, A. Pooth, P. Moens, A. Banerjee and M. Kuball, "Leaky Dielectric" Model for the Suppression of Dynamic Ron in Carbon-Doped AlGaN/GaN HEMTs," IEEE Transactions on Electron Devices, vol. 64, p. 2826–2834, 2017.

[19] M. J. Uren, M. Silvestri, M. Casar, G. A. M. Hurkx, J. A. Croon, J. Sonsky and M. Kuball, "Intentionally Carbon-Doped AlGaN/GaN HEMTs: Necessity for Vertical Leakage Paths," IEEE Electron Device Letters, vol. 35, no. 3, pp. 327-329, 2014.

[20] M. Singh, S. Karboyan, M. J. Uren, K. B. Lee, Z. Zaidi, P. A. Houston and M. Kuball, "Lateral charge spreading and device-to-device coupling in C-doped AlGaN/GaN-on-Si wafers," Microelectronics Reliability, vol. 95, pp. 81-86, 2019.

[21] M. J. Uren, M. Cäsar, M. A. Gajda and M. Kuball, "Buffer transport mechanisms in intentionally carbon doped GaN heterojunction field effect transistors," Applied physics letters, vol. 104, no. 26, pp. 1077-3118, 2014.

[22] S. Yang, C. Zhou, S. Han, J. Wei, K. Sheng and K. J. Chen, "Impact of substrate bias polarity on buffer-related current collapse in AlGaN/GaN-on-Si power devices," IEEE Transactions on Electron Devices, vol. 64, no. 12, pp. 5048-5056, 2017.

[23] W. M. Waller, M. Gajda, S. Pandey, J. J. T. M. Donkers, D. Calton, J. Croon, J. Sonsky, M. J. Uren and M. Kuball, "Control of Buffer-Induced Current Collapse in AlGaN/GaN HEMTs Using SiNx Deposition," IEEE transactions on electron devices, , Vol.), p., Article 8013764, vol. 64, no. 10, pp. 4044-4049, 2017-10.

[24] I. Chatterjee, M. J. Uren, S. Karboyan, A. Pooth, P. Moens, A. Banerjee and M. Kuball, "Lateral Charge Transport in the Carbon-Doped Buffer in AlGaN/GaN-on-Si HEMTs," IEEE transactions on electron devices, vol. 64, no. 3, p. 977–983, 2017.

[25] M. Wohlfahrt, M. Uren, Y. Yin, K. Lee and M. Kuball, "Vertical field inhomogeneity associated with threading dislocations in GaN high electron mobility transistor epitaxial stacks," Applied Physics Letters, vol. 119, no. 24, 2021.

[26] A. Nardo, C. De Santi, C. Koller, C. Ostermaier, I. Daumiller, G. Meneghesso, E. Zanoni and M. Meneghini, "Positive and negative charge trapping GaN HEMTs: Interplay between thermal emission and transport-limited processes," Microelectronics Reliablity, vol. 126, p. 114255, 2021.

[27] D. Bisi, M. Meneghini, C. de Santi, A. Chini, M. Dammann, P. Bruckner, M. Mikulla, G. Meneghesso and E. Zanoni, "Deep-Level Characterization in GaN HEMTs-Part I: Advantages and Limitations of Drain Current Transient Measurements," IEEE transactions on electron devices, vol. 60, no. 10, pp. 3166-3175, 2013-10.

[28] F. Wach, M. J. Uren, B. Bakeroot, M. Zhao, S. Decoutere and M. Kuball, "Low Field Vertical Charge Transport in the Channel and Buffer Layers of GaN-on-Si High Electron Mobility Transistors," IEEE electron device letters, vol. 41, no. 12, pp. 1754-1757, 2020-12.

[29] M. Millesimo, M. Borga, L. Valentini, B. Bakeroot, N. Posthuma, A. Vohra, S. Decoutere, C. Fiegna and A. N. Tallarico, " Role of the GaN-on-Si Epi-Stack on Δ R

ON Caused by Back-Gating Stress," IEEE transactions on electron devices, vol. 70, no. 10, pp. 5203-5209, 2023-10.

[30] A. V. Kuchuk, S. Kryvyi, P. M. Lytvyn, S. Li, V. P. Kladko, M. E. Ware, Y. I. Mazur, N. V. Safryuk, H. V. Stanchu, A. E. Belyaev and G. J. Salamo, "The Peculiarities of Strain Relaxation in GaN/AlN Superlattices Grown on Vicinal GaN (0001) Substrate: Comparative XRD and AFM Study," Nanoscale research letters,, vol. 11, no. 1, pp. 252-252, 2016-12.

[31] J. Neugebauer and C. G. Van De Walle, " Hydrogen in GaN: Novel aspects of a common impurity," Physical review letters, vol. 75, no. 24, pp. 4452-4455, 995-12.

[32] I. Aleksandrov, T. Malin, K. Zhuravlev, S. Trubina, S. Erenburg, B. Pecz and Y. Lebiadok, "Diffusion in GaN/AlN superlattices: DFT and EXAFS study," Applied Surface Science, vol. 515, p. 146001, 2020-06.

[33] P. Bogusławski, N. G. Szwacki and J. Bernholc, "Interfacial segregation and electrodiffusion of dopants in AlN/GaN superlattices," Physical review letters, , vol. 96, no. 18, p. 185501, 2006-05.

[34] J. B. Webb, H. Tang, S. Rolfe and J. A. Bardwell, "Semi-insulating C-doped GaN and high-mobility AlGaN/GaN heterostructures grown by ammonia molecular beam epitaxy," Applied physics letters, vol. 75, no. 7, pp. 953-955, 1999-08.

[35] S. Besendörfer, E. Meissner, T. Zweipfennig, H. Yacoub, D. Fahle, H. Behmenburg, H. Kalisch, A. Vescan, J. Friedrich and T. Erlbacher, "Interplay between C-doping, threading dislocations, breakdown, and leakage in GaN on Si HEMT structures," AIP advances, vol. 10, no. 4, pp. 045028-045028-6, 2020-04.

[36] L. Heuken, M. Kortemeyer, A. Ottaviani, M. Schroder, M. Alomari, D. Fahle, M. Marx, M. Heuken, H. Kalisch, A. Vescan and J. N. Burghartz, "Analysis of an AlGaN/AlN Super-Lattice Buffer Concept for 650-V Low-Dispersion and High-Reliability GaN HEMTs," IEEE transactions on electron devices, vol. 67, no. 3, pp. 1113-1119, 2020-03.

[37] H. Heinke, V. Kirchner, S. Einfeldt and D. Hommel, "X-ray diffraction analysis of the defect structure in epitaxial GaN," Applied physics letters, vol. 77, no. 14, pp. 2145-2147, 2000-10.

[38] J. H. You and H. T. Johnson, "Effect of screw dislocation density on optical properties in n -type wurtzite GaN," Journal of applied physics, vol. 101, no. 2, p. 023516, 2007-01.

[39] T. Yokoyama, Y. Kamimura, K. Edagawa and I. Yonenaga, "Local current conduction due to edge dislocations in deformed GaN studied by scanning spreading resistance microscopy," European physical journal. Applied physics, , vol. 61, no. 1, p. 10102, 2013-01.

[40] O. BAYAL, E. BALCI, A. BİLGİLİ, M. ÖZTÜRK, S. ÖZÇELİK and E. ÖZBAY, "Analysis of Dislocation Density for GaN Based HEMTs in Screw Mod," GU J Sci, Part A, 10(2): , vol. 10, no. 2, pp. 131-139, 2023.

[41] Y. Ni, D. Zhou, Z. Chen, Y. Zheng, Z. He, F. Yang, Y. Yao, G. Zhou, Z. Shen, J. Zhong, Z. Wu, B. Zhang and Y. Liu, "Influence of the carbon-doping location on the material and electrical properties of a AlGaN GaN heterostructure on Si substrate," Semiconductor science and technology , vol. 30, no. 10, p. 105037, 2015-10.

[42] S. Besendörfer, E. Meissner, F. Medjdoub, J. Derluyn, J. Friedrich and T. Erlbacher, "The impact of dislocations on AlGaN/GaN Schottky diodes and on gate failure of high electron mobility transistors," Scientific Reports, vol. 10, no. 1, pp. 17252-17252, 2020-10.

[43] F. C.-P. Massabuau, S. L. Rhode, M. K. Horton, T. J. O'Hanlon, A. Kovács, M. S. Zielinski, M. J. Kappers, R. E. Dunin-Borkowski, C. J. Humphreys and R. A. Oliver, "Dislocations in AlGaN: Core Structure, Atom Segregation, and Optical Properties," Nano letters, vol. 17, no. 8, pp. 4846-4852, 2017-08.

[44] S. Besendörfer, E. Meissner, A. Lesnik, J. Friedrich, A. Dadgar and T. Erlbacher, "Methodology for the investigation of threading dislocations as a source of vertical leakage in AlGaN/GaN-HEMT heterostructures for power devices," Journal of applied physics, vol. 125, no. 9, p. 095704, 2019-03.

[45] V. G. S. C. R. a. S. M. Joshi, "Interplay of device design and carbon-doped GaN buffer parameters in determining dynamic in AlGaN/GaN HEMTs," IEEE Transactions on Electron Devices, vol. 69, no. 11, pp. 6035-6042, 2022.

[46] E. Fabris, M. Borga, N. Posthuma, M. Zhao, B. De Jaeger, S. You, S. Decoutere, M. Meneghini, G. Meneghesso and E. Zanoni, "Vertical stack reliability of GaN-on-Si buffers for low-voltage applications," in IEEE International Reliability Physics Symposium (IRPS), 2021.

[47] R. Kabouche, I. Abid, R. Püsche, J. Derluyn, S. Degroote, M. Germain, A. Tajalli, M. Meneghini, G. Meneghesso and F. Medjdoub, "Low On-Resistance and Low Trapping Effects in 1200 V Superlattice GaN-on-Silicon Heterostructures," Physica status solidi. A, Applications and materials science, vol. 217, no. 7, pp. 1900687 1-6, 2020-04.

[48] P. Moens, A. Banerjee, M. J. Uren, M. Meneghini, S. Karboyan, I. Chatterjee, P. Vanmeerbeek, M. Casar, C. Liu, A. Salih, E. Zanoni, G. Meneghesso, M. Kuball and M. Tack, "Impact of buffer leakage on intrinsic reliability of 650V AlGaN/GaN HEMTs," in IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 2016.

[49] J. Joh and J. Del Alamo, “Critical Voltage for Electrical Degradation of GaN High-Electron Mobility Transistors,” IEEE electron device letters, vol. 29, no. 4, pp. 287-289, 2008-04.

[50] M. Borga, C. De Santi, S. Stoffels, B. Bakeroot, X. Li, M. Zhao, M. Van Hove, S. Decoutere, G. Meneghesso, M. Meneghini and E. Zanoni, “ Modeling of the Vertical Leakage Current in AlN/Si Heterojunctions for GaN Power Applications,” IEEE transactions on electron devices, vol. 67, no. 2, pp. 595-599, 2020-02.

[51] Y. Yamaoka, A. Ubukata, Y. Yano, T. Tabuchi, K. Matsumoto and T. Egawa, “Effect of threading dislocation in an AlN nucleation layer and vertical leakage current in an AlGaN/GaN high-electron mobility transistor structure on a silicon substrate,” Semiconductor science and technology, vol. 34, no. 3, p. 35015, 2019-03.

[52] N. Zagni, A. Chini, F. M. Puglisi, P. Pavan and G. Verzellesi, “The effects of carbon on the bidirectional threshold voltage instabilities induced by negative gate bias stress in GaN MIS-HEMTs,” Journal of computational electronics, vol. 9, no. 4, p. 1555–1563, 2020.

[53] J. C. Moore, J. E. Ortiz, J. Xie, H. Morkoç and A. A. Baski, “Study of leakage defects on GaN films by conductive atomic force microscopy,” Journal of Physics: Conference Series, vol. 61, no. 1, pp. 90-94, 2007-03.

[54] R. Groger, L. Leconte and A. Ostapovets, “Structure and stability of threading edge and screw dislocations in bulk GaN,” COMPUTATIONAL MATERIALS SCIENCE , vol. 99, pp. 195-202, 2015-01.

[55] S. I. Kim, K. H. Lee, H. A. Mun, H. S. Kim, S. W. Hwang, J. W. Roh, D. J. Yang, W. H. Shin, X. S. Li, Y. H. Lee, G. J. Snyder and S. W. Kim, “Dense dislocation arrays embedded in grain boundaries for high-performance bulk thermoelectrics,” Science (American Association for the Advancement of Science), , vol. 348, no. 6230, pp. 109-114, 2015-04.

[56] K. Termentzidis, M. Isaiev, A. Salnikova, I. Belabbas, D. Lacroix and J. Kioseoglou, “Impact of screw and edge dislocations on the thermal conductivity of individual nanowires and bulk GaN: A molecular dynamics study,” Physical chemistry chemical physics : PCCP, , vol. 20, no. 7, pp. 5159-5172, 2018.

[57] H. Itakura, T. Nomura, N. Arita, N. Okada, C. M. Wetzel, T. P. Chow and K. Tadatomo, “Effect of InGaN/GaN superlattice as underlayer on characteristics of AlGaN/GaN HEMT,” AIP advances, vol. 10, no. 2, pp. 025133-025133-5, 2020-02.

[58] N. Ikeda, Y. Niiyama, H. Kambayashi, Y. Sato, T. Nomura, S. Kato and S. Yoshida, “GaN Power Transistors on Si Substrates for Switching Applications,” Proceedings of the IEEE, vol. 98, no. 7, pp. 1151-116, 2010-07.

[59] T. P. yaw, V. Egorkin, V. Korneev and M. M. Thant, “Simulation of the Effect of GaN Buffer Layer Doped with Iron Fe and Carbon C on the DC Static Characteristics of

Normally Open HEMT AlGaN/AlN/GaN Transistor," in 2021 IEEE Conference of Russian Young Researchers in Electrical and Electronic Engineering (ElConRus), 2021, p.2604-2609, Article 9396691, St. Petersburg, 2021.

[60] S. Li, M. E. Ware, J. Wu, V. P. Kunets, M. Hawkridge, P. Minor, Z. Wang, Z. Wu, Y. Jiang and G. J. Salamo, "Polarization doping: Reservoir effects of the substrate in AlGaN graded layers," Journal of applied physics, vol. 112, no. 5, pp. 053711 1-5, 2012-09.

[61] F. D., M. M., H. Behmenburg, M. Kortemeyer and M. Heuken, "Buffer development for GaN power electronic applications using extrinsic carbon doping for a super-lattice structure," in CSMANTECH, Minneapolis, Austin TX, 2019.

[62] J. Su, N. Posthuma, D. Wellekens, Y. N. Saripalli, S. Decoutere, R. Arif and G. D. Papasouliotis, "Growth and Implementation of Carbon-Doped AlGaN Layers for Enhancement-Mode HEMTs on 200 mm Si Substrates," Journal of electronic materials, vol. 45, no. 12, pp. 6346-6354, 2016-12.

[63] M. J. Uren and M. Kuball, "Impact of carbon in the buffer on power switching GaN-on-Si and RF GaN-on-SiC HEMTs," Japanese Journal of Applied Physics, vol. 60, p. SB0802, 2021.

[64] W. Sun, C.-K. Tan and N. Tansu, "AlN/GaN Digital Alloy for Mid- and Deep-Ultraviolet Optoelectronics," Scientific reports, vol. 7, no. 1, pp. 11826-8, 2017-09.

6. Impact of Si Co-Doping on Dynamic R_{ON} in Heavily Carbon-Doped GaN Buffer Layers

6.1 Introduction

This chapter examines the effect of incorporating silicon (Si) doping incorporation into a heavily carbon-doped GaN buffer layer. Carbon, being an amphoteric impurity, can behave as an acceptor when substituted at the nitrogen site (C_N) or as a donor when substituted at the gallium site (C_{Ga}) [1] [2]. Similarly, Si is an n-type dopant commonly used to achieve n-type conductivity in GaN [3] [4]. However, when Si is intentionally incorporated into a p-type C:GaN layer, C_N acts as acceptors while both C_{Ga} and Si_{Ga} act as donors, reducing the effective hole density and increasing the resistivity of the layer [1] [5] [4] [3].

Carbon is typically the primary dopant in these layers, with carbon acceptors often being passivated by background donors as well as C_{Ga} [3]. Some studies suggest that Si incorporation into a carbon-doped GaN layer can shift the Fermi level [6] [7]. However, with carbon concentrations two orders of magnitude higher than Si concentrations, the Fermi level remains pinned close to the valence band [5] [4], maintaining a nominally p-type character [3].

Agrawal et al. [8] and Lesnik et al. [3] concluded that Si doping can offer flexibility in controlling the n-type conductivity and doping profile. They noted, however, that low levels of Si doping are often influenced by growth conditions. Lesnik et al. [5] further demonstrated that in Si-carbon co-doped GaN, when [C] > [Si], the sample will always exhibit a p-type behaviour, with the compensation properties being largely governed by the carbon acceptors. By co-doping with both C and Si, it is possible to control free carrier concentration and charge balance. Tokuda et al. [9] also highlighted that although it is challenging to reduce residual Si impurities, Si incorporation can be an effective method to enhance the resistivity of GaN layers.

Despite these findings, limited literature is available on the impact of Si and carbon co-doping on the dynamic R_{ON} in GaN devices. This study aims to fill this gap by analysing the dynamic R_{ON} of Si-doped carbon-doped GaN (CGaN) using experimental methods and TCAD simulations. Substrate biasing, transient techniques, and HRXRD analysis are employed to explore the critical role of the CGaN layer in mitigating dynamic R_{ON}. While higher carbon doping (~10^{19} cm^{-3}) is typically introduced to enhance breakdown voltage [1] [10], it has also been observed that the dynamic properties of devices degrade with

higher carbon levels [5][8]. This chapter will specifically examine the effect of Si doping at varying concentrations in a heavily carbon-doped CGaN buffer layer (2 x 10^{19} cm^{-3}) on both dynamic R_{ON} and crystal quality.

6.2 Experimental Methods

6.2.1 Wafer Details

The AlGaN/GaN HEMTs investigated in this study were commercially grown on a Si substrate using MOCVD provided by Nexperia (processed by NXP semiconductors). The three wafers in this study have a nominally identical epitaxial layer structure, as previously illustrated in Figure 2.14, with variations in Si doping concentration in the C:GaN layer. The epitaxial structure consists of a 140 nm AlN nucleation layer, a 3.3 µm AlN/GaN superlattice SRL, a 1.0 µm C:GaN layer, a 0.5 µm UID GaN layer, a 20 nm AlGaN barrier layer with 20% Al composition, and a 3 nm undoped GaN cap. The carbon doping concentration in both the C:GaN and SRL layers is 2 x 10^{19} cm^{-3}, while the background dopant concentration in all layers is approximately 1 x 10^{16} cm^{-3}. Figure 6.1 illustrates the nominal Si concentrations incorporated into the C:GaN buffer of Wafers S1, S2, and S3.

	Carbon (cm^{-3})	Si (cm^{-3})
Wafer S1	2 x 10^{19}	5 x 10^{16}
Wafer S2	2 x 10^{19}	1 x 10^{17}
Wafer S3	2 x 10^{19}	5 x 10^{17}

Table 6.1 - Carbon and the Si concentrations in the CGaN buffer layer of the studied wafers S1, S2 and S3

All electrical experiments were conducted on TLM structures with gap spacings ranging from 5 µm to 25 µm, while the width of the ohmic contacts remained constant at 100 µm, as depicted in Figure 2.17. This setup is the same as the approach discussed in previous chapters. The fabrication methods for the TLM structures are detailed in Chapter 2. A 2DEG density of 5.1 x 10^{12} cm^{-2} was extracted from capacitance-voltage measurements on the wafers, and the sheet R_{Sheet} was approximately 750 Ω/square.

6.2.2 Measurement Techniques

The crystalline quality of the wafers was assessed through HRXRD rocking curve measurements, as detailed in Section 2.6.6. Threading dislocation density (TDD), along with the individual edge and screw dislocation components, was extracted using the FWHM values of the (0002) and (1 0 $\bar{1}$ 2) ω scans, respectively [11] [12] [13].

Substrate ramp measurements were performed by applying a small sensing voltage of 1 V between the ohmic contacts to monitor 2DEG conductivity [14] [15]. The biasing conditions have been extensively discussed in previous chapters. These measurements were also carried out across both low and high V_{SUB} regimes, ramped from 0 V to -300 V and -550 V, before being swept back to 0 V at a ramp rate of 10 V/s. The bidirectional voltage sweeps simultaneously recorded the substrate leakage current (I_{SUB}), which corresponds to the total vertical leakage current.

During substrate transient measurements, the three terminals were biased identically to the substrate ramp measurements, as previously detailed. The focus remained on 15 µm structures for comparative analysis.

All measurements were carried out at RT and in darkness. Multiple identical structures across the sample were tested to account for variations within each wafer. For the final analysis, the average results for 15 µm from both substrate ramp and transient measurements were used to highlight the distinctions between the samples.

6.3 Results

FWHM ω rocking curve reflection [0002] and [1 0 $\bar{1}$ 2] have been used as a measure of the crystal quality. Table 6.2 presents the corresponding screw (T_{screw}) and edge (T_{Edge}) dislocation densities for Wafers S1, S2, and S3, estimated using the equations outlined in Section 2.6.6.

Wafer	**Wafer S1**	**Wafer S2**	**Wafer S3**
FWHM ω 002 (arc.sec)	645.8 ± 3.6%	631.4 ± 0.10%	571.7 ± 0.16%
FWHM ω 102 (arc. sec.)	1413.0 ± 0.8%	1281.6 ± 0.51%	1246.0 ±0.11%
T_{screw} (cm^{-2})	8.37 x 10^8	8.00 x 10^8	6.56 x 10^8
T_{Edge} (cm^{-2})	8.36 x 10^9	6.60 x 10^9	6.50 x 10^9

Table 6.2 - FWHM of (0002) and (1 0 $\bar{1}$ 2) reflections obtained from the HRXRD scans

As observed in the previous chapters, the edge dislocation density in all three wafers remains an order of magnitude higher than the screw dislocation density. A reduction in the TDD, along with both the screw and edge components, is observed as the Si doping concentration increases. This trend indicates that variations in the Si doping concentration within the CGaN layer influence the dislocation characteristics of the wafers.

Figure 6.1 presents the normalised channel currents for the bi-directional substrate ramp sweeps of Wafers S1, S2, and S3, measured at a TLM gap spacing of 15 µm. The V_{SUB} was swept from 0 V to -300 V and back, with the normalised channel currents plotted against V_{SUB}. The light grey dashed line represents the substrate threshold voltage (V_{TH}) also referred to as the capacitive coupling line. This line serves as a reference for an ideal scenario in which no trapping occurs, and the structure behaves purely as a dielectric capacitor [22] [23]. Since all wafers have the same stack thickness, they share the same V_{TH} value of -428.7 V. For clarity, the solid line, marked with a downward arrow, represents the forward sweep (0 V to -300 V), while the dashed line indicates the return sweep. This convention will be consistently followed across all substrate ramp results.

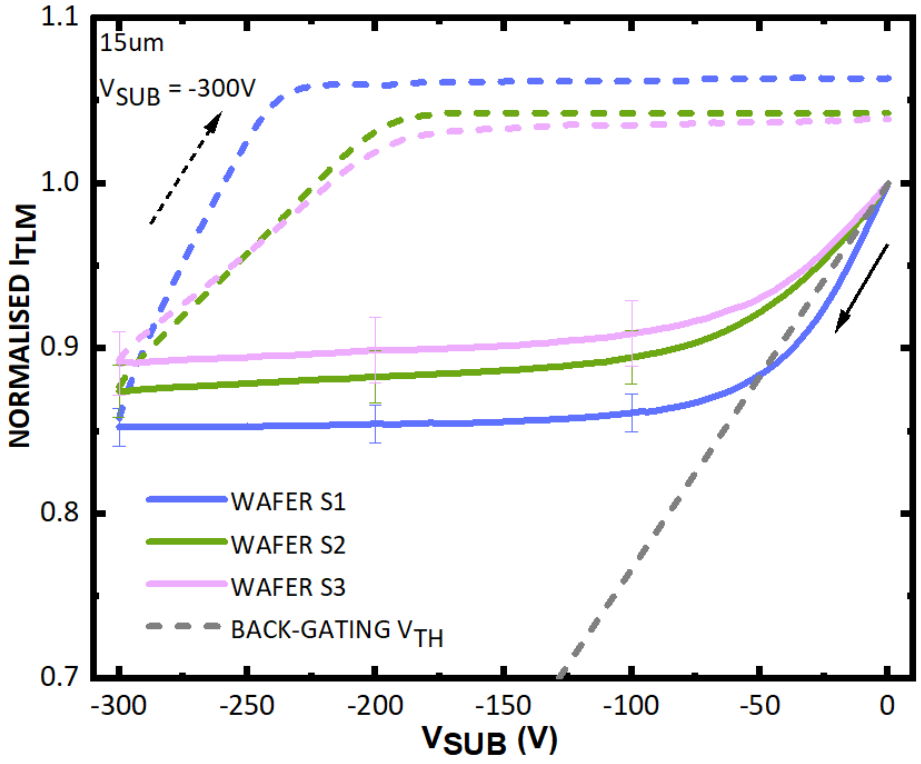

Figure 6-1 - Bidirectional substrate ramp characteristics on TLM with gap spacing 15 µm, of Wafer S1, S2 and S3, at a sweep rate of 10 V/s. The forward sweep from 0V to -300 V and the return sweep are indicated by solid and dashed arrows, respectively. The grey dashed line represents the capacitive coupling line. Error margins were determined to be ±1.34%, ±1.8% and ±2.18%, for Wafer S1,S2, and S3, respectively.

As shown in Figure 6.1, hysteresis was observed in all three wafers during the substrate ramp sweeps. This behaviour is consistent with previous reports on GaN-on-Si epitaxial structures with a CGaN layer, as well as the findings discussed in earlier chapters, indicating the presence of trapping effects [14] [15] [16].

Notably, Wafer S1 exhibits a more pronounced trapping effect, as indicated by its larger hysteresis compared to Wafer S3. At low V_{SUB} (up to −20 V), the normalised channel currents of all wafers initially follow the capacitive coupling line before deviating. Specifically, Wafer S1, which has the lowest Si concentration, deviates below the capacitive coupling line, whereas Wafers S2 and S3 shift towards the left. The extracted g_m values are 0.0475 mS, 0.0124 mS, and 0.00891 mS for Wafer S1, Wafer S2, and Wafer S3, respectively. As discussed in previous chapters, this leftward shift of the normalised currents from the capacitive coupling line is attributed to decreasing transconductance. This suggests that charge redistribution within the C:GaN layer decreases as Si concentration increases.

As V_{SUB} continues to increase, channel current saturation is observed. Wafer S3 reaches saturation at approximately −55 V, followed by Wafer S2 at −65 V, while Wafer S1 requires a slightly higher V_{SUB} of around −70 V to saturate. Overall, the return sweep currents of all wafers remain slightly higher than their initial values at 0 V, suggesting an increased 2DEG density compared to the forward sweep [14]. Additionally, the gap between the 0 V initial currents and the 0 V return currents increases as Si concentration decreases. This growing disparity can be attributed to variations in the time constants among the wafers, leading to prolonged response times with decreasing Si concentration. These trends emphasise the impact of Si doping on the response time to V_{SUB}.

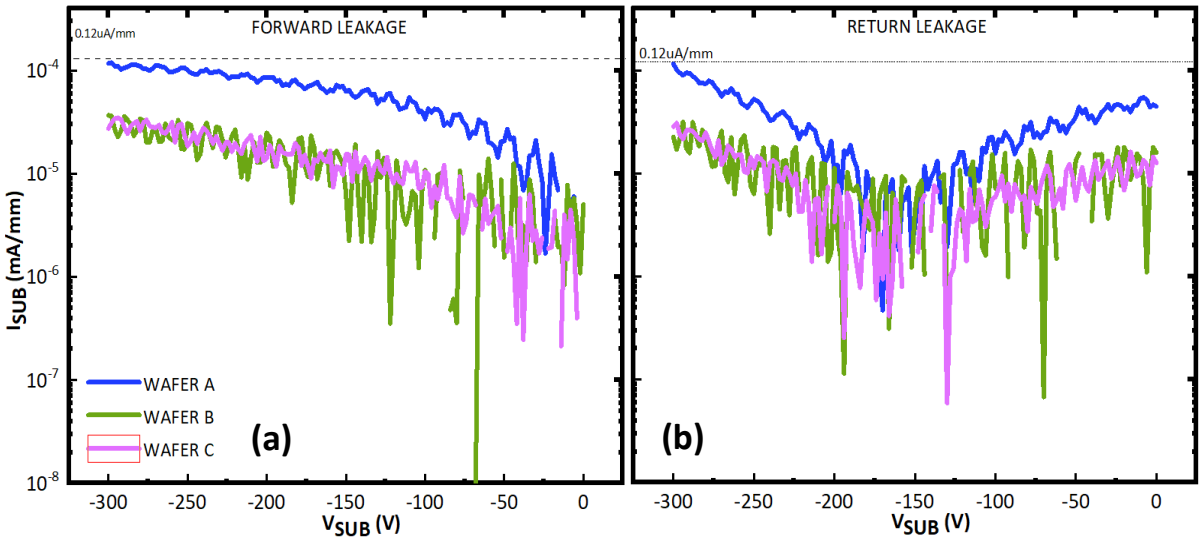

Figure 6-2 - Substrate leakage currents of (a) forward sweep from 0 V to -300 V and (b) return sweep from -300V to 0 V of the bi-directional substrate ramp characteristics on TLM with gap spacing 15 µm, of the three wafers, at a sweep rate of 10 V/s.

Figure 6.2 presents the substrate leakage currents (I_{SUB}) during the forward and return sweeps. In both sweeps, Wafer S1 consistently exhibits a higher leakage current compared to Wafers S2 and S3. In contrast, Wafers S2 and S3 demonstrate relatively lower and similar leakage characteristics.

Figure 6.3 presents the bidirectional substrate ramp characteristics for the 15 µm TLM structures of Wafers S1, S2, and S3, as V_{SUB} was swept from 0 V to -550 V and back to 0 V. As previously discussed, understanding carrier transport at a high V_{SUB} of -550 V is essential, as it approaches the nominal breakdown voltage of 600 V for the epitaxy used in this study.

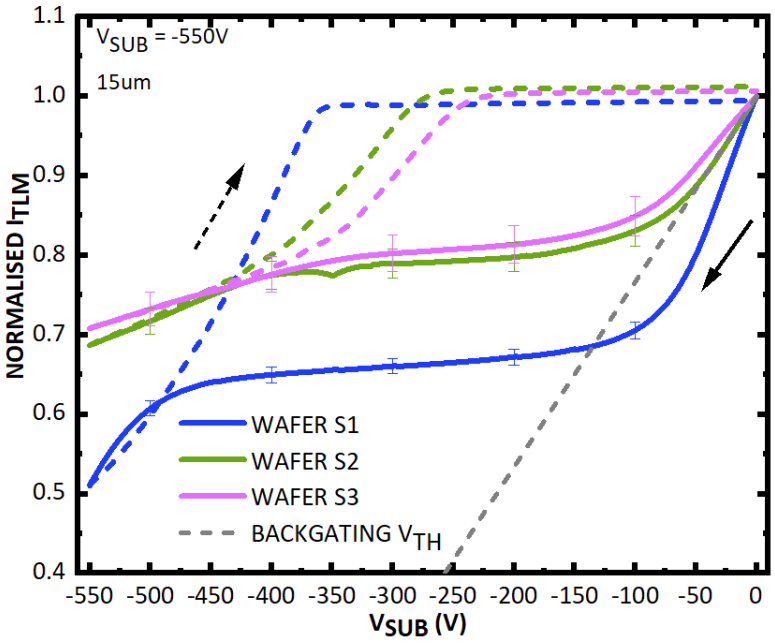

Figure 6-3 - Bi-directional substrate ramp characteristics on TLM with gap spacing 15 µm, of the three wafers, at a sweep rate of 10 V/s. The forward sweep from 0V to -550 V and the return sweep are indicated by a solid and dashed arrows respectively. The grey dashed line represents the capacitive coupling line. Error margins were determined to be ±1.5%, ±2.3%, ±2.9%, for Wafer S1, S2 and S3, respectively

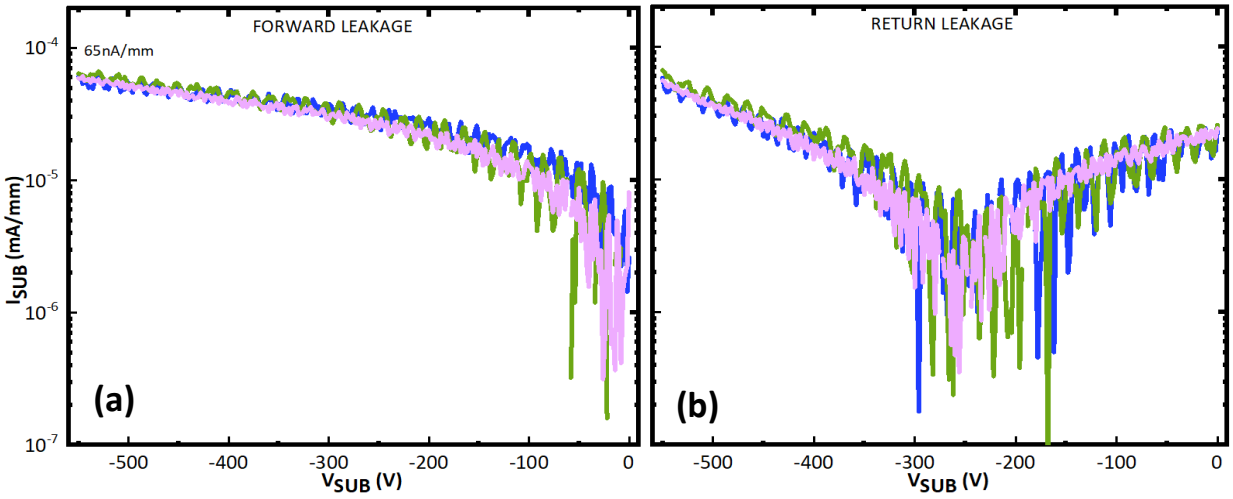

Figure 6-4 - Substrate leakage currents of (a) forward sweep from 0 V to -550 V and (b) return sweep from -550V to 0 V of the bi-directional substrate ramp characteristics on TLM with gap spacing 15 µm, of the three wafers, at a sweep rate of 10 V/s.

Wafer S3 in Figure 6.3 continues to exhibit the highest positive charge storage, while Wafer S1 shows the lowest, with Wafer S2 displaying an intermediate behaviour. However, in contrast to the behaviour observed at a moderate voltage of -300 V, notable differences in the channel current profile emerge at higher V_{SUB}. The plateau region, where the channel current exhibits minimal variation before a noticeable decrease, ceases

at V_{SUB} = − 325 V for Wafer S3, -375 V for Wafer S2, and -450 V for Wafer S1. This transition marks the point at which positive charge accumulation ceases, with any remaining charge being retained within the epitaxial structure. In essence, an increase in Si concentration leads to subtle shifts in the specific bias point at which positive charge storage ends.

Figure 6.4 (a) and (b) present I_{SUB} during both the forward and return sweeps at V_{SUB} = -550 V, respectively. Similar trends to those observed at -300 V are evident, with Wafer S3 exhibiting the lowest leakage compared to Wafer S1.

Additionally, the return sweep 0 V channel currents for all three wafers have nearly returned to their initial values, suggesting that at higher V_{SUB}, the discharging mechanisms in these wafers differ from those observed at -300 V.

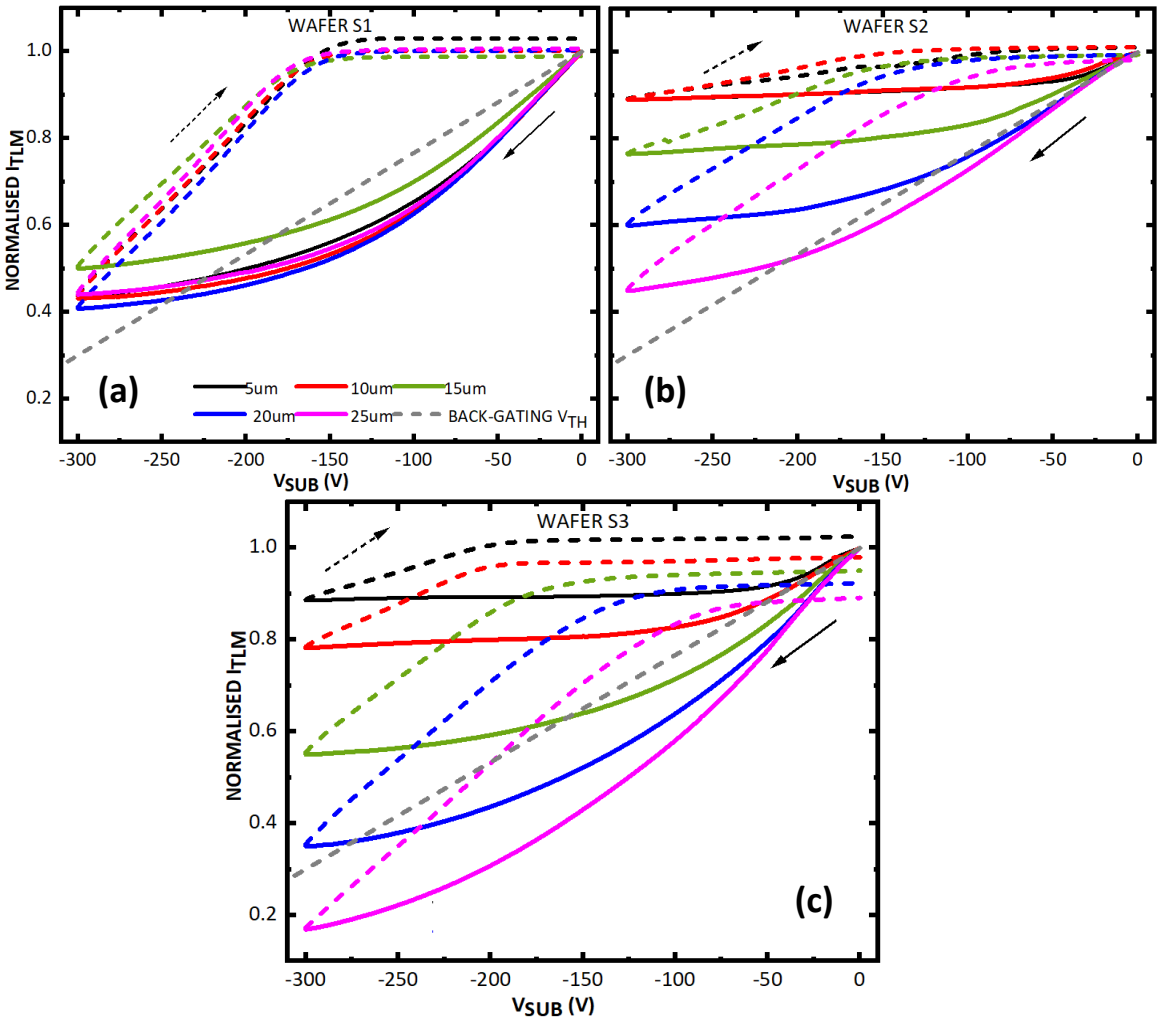

Figure 6-5 - Bidirectional substrate ramp characteristics of (a) Wafer S1 (b) Wafer S2 and (c) Wafer S3, covering TLM gap spacings of 5, 10, 15, 20, and 25 µm. V_{SUB} was ramped from 0 V to -300 V, represented by the solid line, followed by the return sweep from -300 V back to 0 V. The error margins were determined to be ±3.15%, ±5.71% and ±6.04% for samples S1, S2 and S3, respectively.

Additional measurements were conducted using different TLM gap spacings for all three wafers. As observed in Figure 6.5(a), Wafer S1 exhibits minimal gap dependence, with similar hysteresis observed across all gap spacings. In contrast, Wafer S3 in Figure 6.5(c) displays increased hysteresis and a pronounced gap dependence. Moreover, Figure 6.5(c) also reveals an anomaly in the return sweep, where the channel currents is less than their initial values at 0 V as the gap spacing increases. This deviation suggests an underlying charge trapping, which is not observed in Wafer S1.

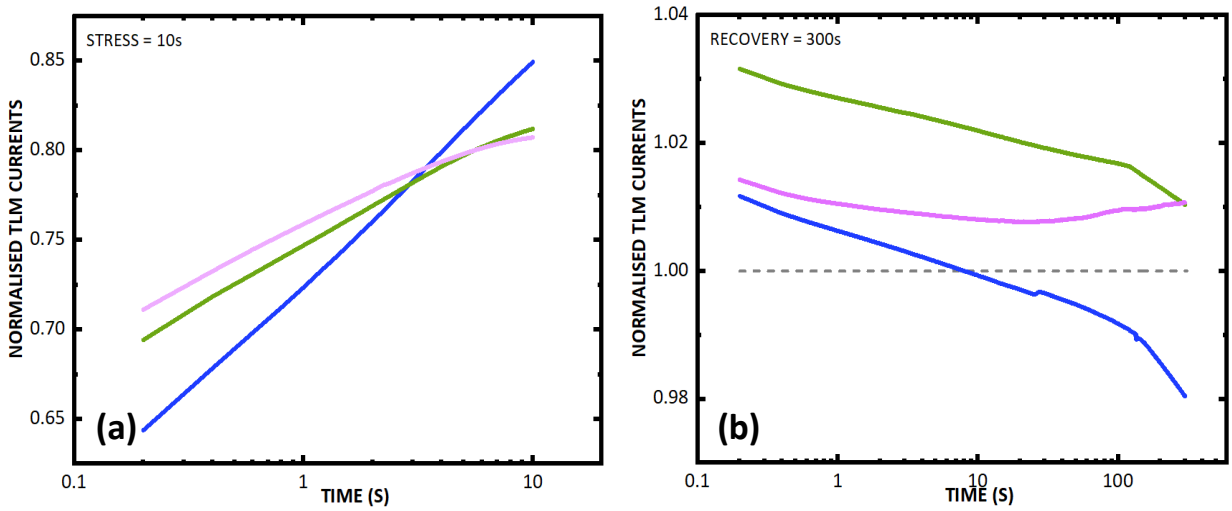

Figure 6-6 - Normalised channel currents for 15 µm TLM structures of Wafer S1, S2 and S3, during the (a) stress phase and (b) recovery phase of the substrate transient measurements. A substrate voltage of -300 V was applied for 10 seconds, followed by a 300-second measurement of the channel current at 0 V after the substrate bias was removed. Error margins were determined to be ±0.78%, ±2.1% and ±3.1% for samples S1, S2 and S3, respectively

Normalised backgating transient currents under negative V_{SUB} stress for all three wafers are presented in Figure 6.6. Figure 6.6 (a) illustrates the stress phase, where the transient current response is measured during the application of V_{SUB} = -300 V, while Figure 6.6 (b) corresponds to the recovery phase, observed after the substrate bias is reset to 0 V.

Upon the application of an off-state stress V_{SUB} of -300 V, the normalised current levels are 0.64 for Wafer S1, 0.69 for Wafer S2, and 0.72 for Wafer S3, which can be attributed to the backgating effect. In an ideal structure with no trapping, the channel currents of all three wafers should immediately drop to 0.3 upon exposure to V_{SUB} = −300 V, as predicted by the theoretical backgating V_{TH} line. However, the observed current levels of all three wafers, exceed this predicted value, indicating the presence of positive charge storage. This behaviour is subtly consistent with the trends observed in the substrate

ramp measurements. Additionally, a positive-going current transient (i.e. increasing channel current over time) is observed, suggesting continued accumulation of positive charge within the CGaN layer [17].

The negative-going (decreasing) recovery transient response, shown in Figure 6.6 (b), was recorded after V_{SUB} was reset to 0 V. Immediately upon the removal of the stress voltage, all wafers exhibit elevated channel currents that exceed the 0 V equilibrium level, remaining above the grey dashed line, this is a direct consequence of the trapping effect. Notably, similar behaviour was also observed in wafers discussed in previous chapters that did not incorporate co-doping.

In the absence of a substrate bias, both Wafer S1 and Wafer S2 exhibit a gradual decrease in channel current, indicating that the channel is progressively returning to equilibrium. In contrast, while Wafer S3 initially follows a similar decreasing trend towards the reference value (the grey dashed line), it then begins to increase again. This initial reduction is primarily attributed to electron diffusion from the 2DEG into the CGaN, which plays a significant role in discharging the previously stored positive charge [17]. However, the recovery dynamics differ among the wafers, as the channel currents of both Wafer S2 and Wafer S3 do not return to equilibrium within the 300 s measurement window, indicating prolonged recovery times and particularly complex discharging behaviour in Wafer S3.

Figure 6.7 illustrates the extracted time constants (τ) along with their respective curve fittings. When analysing multi-exponential current transients, such as those in Figure 6.6, careful selection of the fitting region is crucial to ensure accurate extraction of the time constant. While extracting a time constant may appear straightforward, choosing the appropriate time window is essential to avoid interference from multiple overlapping trapping effects. Since the transient exhibits multi-exponential behaviour, the selected region must provide both an optimal fit and a single dominant time constant [18].

The extracted time constants for Wafer S1, S2, and S3 are 44.5 s ± 3.875, 58.5 s ±1.04, and 110.8 s ±8.95%,respectively, based on the 40–90 s region. The τ associated with this emission process depends on the nature of the trap states, with fast traps releasing carriers rapidly and deep traps retaining charge for extended periods [18] [19]. Therefore, the first and last 40 s were excluded to avoid distortions from these extreme trapping behaviours.

To ensure a reliable extraction of the time constant, a specific time window was carefully selected to balance contributions from different trapping mechanisms. This chosen range is crucial as it provides a consistent fit across all measured transients while avoiding distortions caused by fast transient effects at short timescales and prolonged deep trap retention at extended timescales [18]. Notably, the alternative time regions of 90–140 s and 140–260 s were unsuitable due to poor curve fitting across all three wafers. Similarly, the 100–200 s range, which was used in previous chapters, was not adopted here, as no single time window within this interval provided a universally consistent fit across all datasets. Hence, the middle time range was selected, as it is mutually shared among the transients, ensuring optimal curve fitting while minimising the influence of extreme trapping behaviours [18]. This approach allows for a more representative and physically meaningful extraction of the time constant.

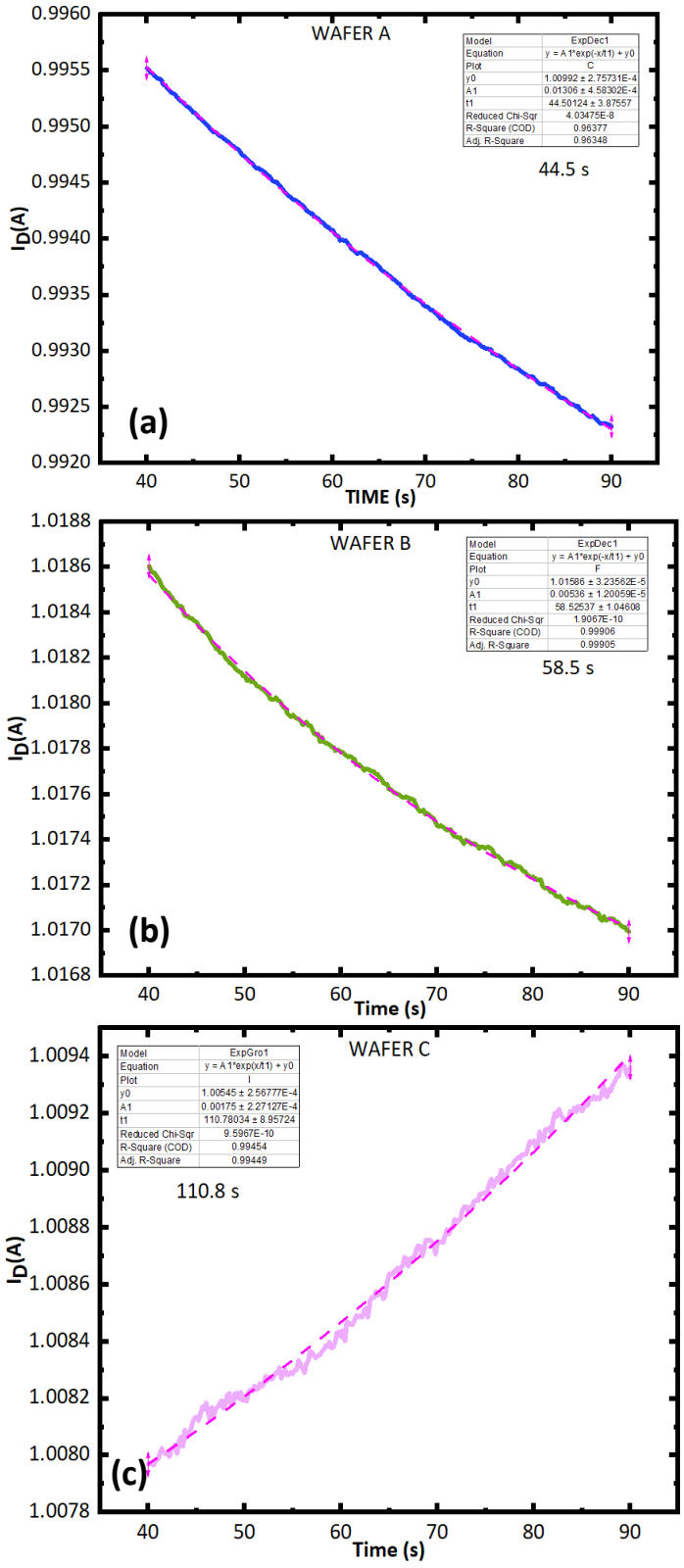

Figure 6-7 - Extracted time constants of the (a) Wafer A (b) Wafer B and (c) Wafer C, using the exponential curve fitting to the channel current decay. The fitted equation follows the $y = y_0 + Ae^{t/\tau}$

6.4 Simulations

To gain insight into the trapping and detrapping dynamics influenced by Si doping in the CGaN layer, two sets of simulations have been conducted. The first set compares the backgating response of a structure with 2×10^{19} cm^{-3} carbon doping but without Si-doping in the CGaN (referred to as the "REF wafer") and Wafer B, which has been co-doped with 1×10^{17} cm^{-3} Si. In the second set of simulations, Wafer S1 and Wafer S2, both featuring C:Si co-doped GaN layers, have been compared to understand the effect of different Si doping concentrations in the CGaN.

The parameters used in this TCAD model have been discussed in Chapters 2. In this model, Si in the CGaN layer is incorporated as a shallow donor with an energy level of Ec – 0.03 eV [20] [21]. In the second set of simulations examines, the Si donor concentration is varied from 5×10^{16} cm^{-3} (Wafer S1) to 1×10^{17} cm^{-3} (Wafer S2) while maintaining a fixed compensation ratio (N_D/N_A) between C_N and C_{Ga}. At room temperature, Si doping within the CGaN buffer is expected to be fully ionised, as it acts as a shallow donor [7].

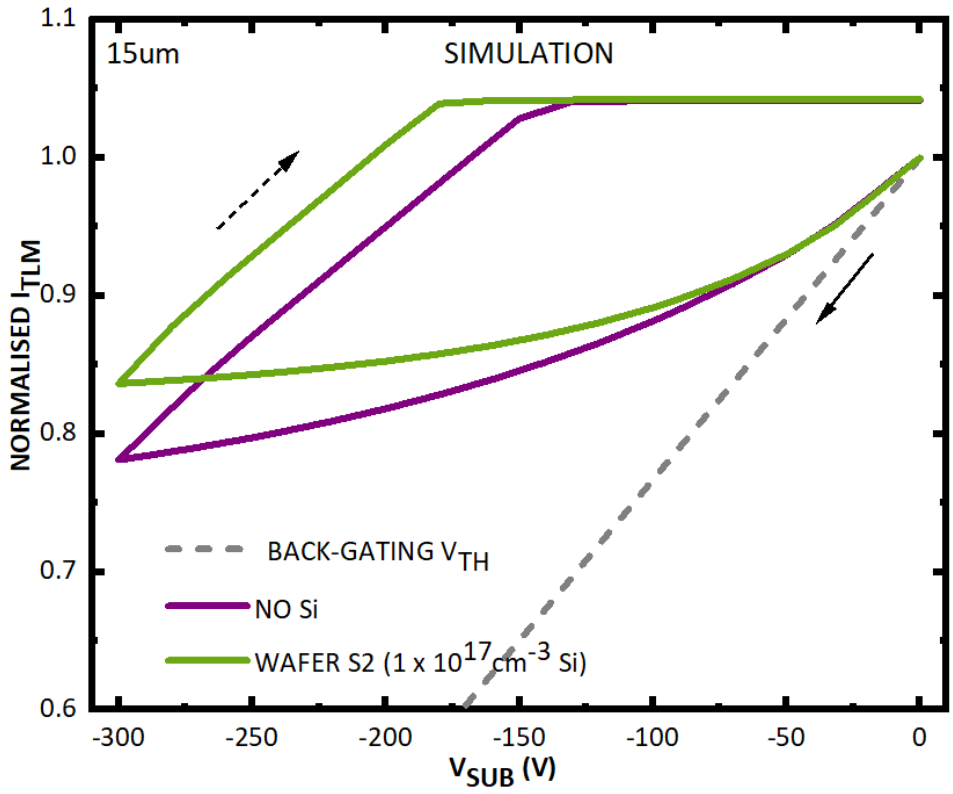

Figure 6-8 - The simulated substrate ramps of REF wafer and Wafer B with a 1×10^{17} cm^{-3} Si co-doping. The solid black arrow indicates the forward sweep (0 V to -300 V), while the dashed black arrow represents the return sweep (-300 V to 0 V).

Figure 6.8 compares the simulated substrate ramp sweeps of two structures: the REF wafer, with 2×10^{19} cm^{-3} carbon doping, and Wafer S2, which incorporates 1×10^{17} cm^{-3} Si alongside 2×10^{19} cm^{-3} carbon. Both simulated curves exhibit hysteresis, confirming the presence of charge trapping and detrapping behaviour in both structures. From 0 V to -60 V, the decreasing currents overlap, this suggests that the g_m of these normalised currents are similar indicating that the charge redistribution is pretty much the same. The reasons for this behaviour in the simulated curves were discussed in Chapter 5. Beyond -60 V, Wafer S2 reaches saturation, whereas in the REF wafer, the currents continue to decrease further until saturation occurs at approximately -150 V. The return curves for both wafers converge, exhibiting similar current levels at 0 V.

Figure 6.9 (a) – (f) compare the simulated conduction band energy, vertical electric field at the UID/CGaN interface, electron density, hole density, and space charge region at the UID/CGaN and CGaN/C:AlGaN interfaces for the REF wafer and Wafer S2, at V_{SUB} = -300 V. At V_{SUB} of -300 V, as expected, both wafers exhibit upward band bending, as discussed in previous chapters. Despite having a similar carbon doping concentration in the CGaN layer, the REF wafer (with no Si) shows a more pronounced upward band bending than Wafer S2, as seen in Figure 6.9 (a) [22]. Figure 6.9(b) further illustrates the vertical electric field distribution and the extent of the space charge region at the UID/CGaN interface. Notably, Wafer S2 exhibits a higher peak electric field in the UID layer than the REF Wafer.

Figure 6.9 (c) presents the electron density distribution along the vertical cutline across all layers in the stack. Wafer S2 exhibits a higher electron density within the CGaN region, along with an increased 2DEG density at the CGaN/C:AlGaN interface, in contrast to the REF wafer. Conversely, Figure 6.9 (d) illustrates the hole density profile, where a notably higher hole concentration is observed in the CGaN/C:AlGaN regions for Wafer S2.

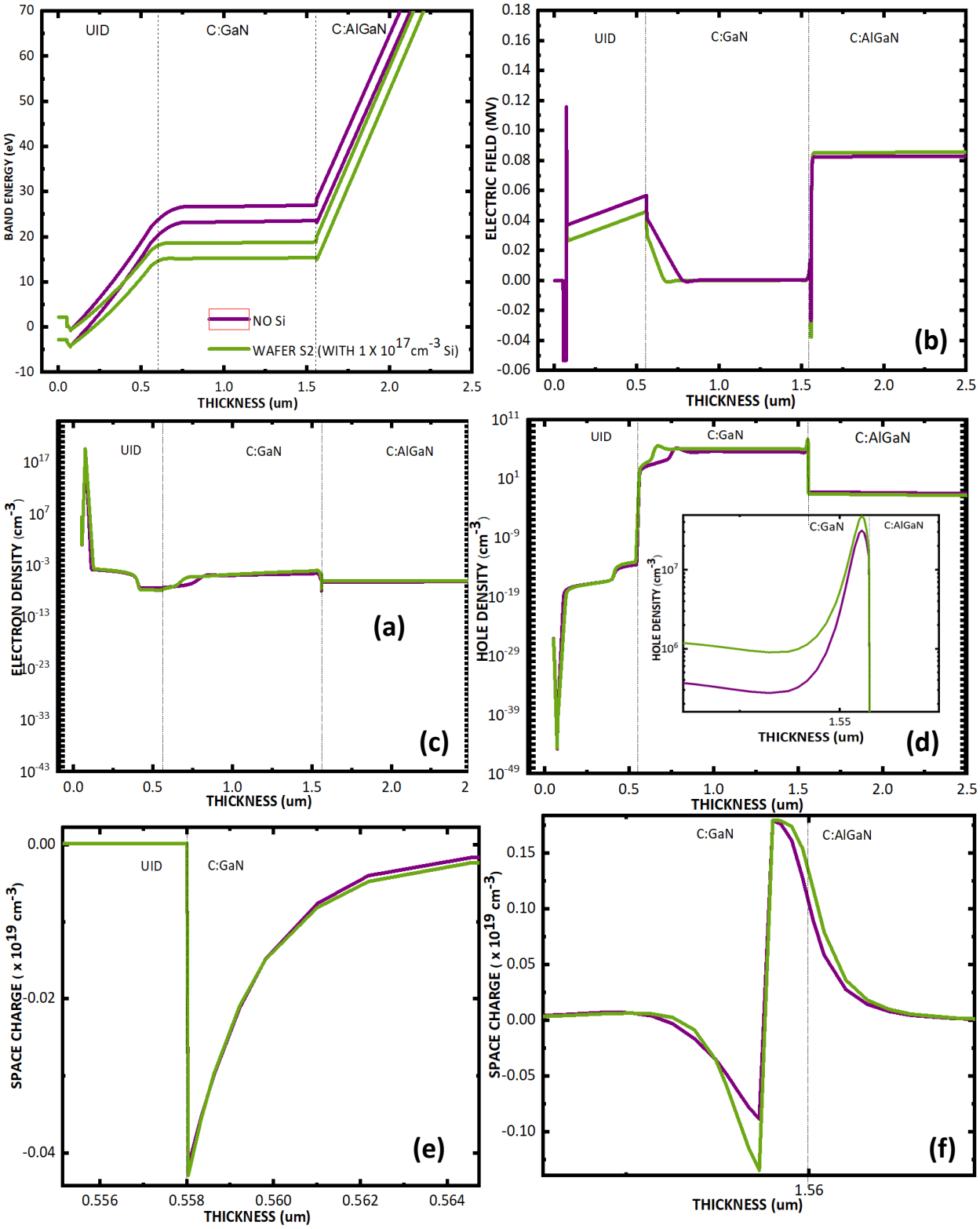

Figure 6-9 - Comparison between the simulated (a) conduction band energy (b) electric field at the UID/CGaN heterojunction (c) electron density (d) hole density (e) the space charge region at the at the UID/CGaN heterojunction and (f) the space charge region at the CGaN/C:AlGaN heterojunction of the REF wafer and Wafer S2 , at V_{SUB} = -300 V.

Figures 6.9 (e) and 6.9 (f) depict the depletion regions at the UID/CGaN and CGaN/C:AlGaN heterointerfaces, respectively. As discussed in previous chapters, the space charge distribution at the UID/CGaN interface results from charge redistribution and current flow within the CGaN layer, leading to negative charge accumulation at the top of the CGaN and positively charged ionised donors at the bottom, forming a dipole [14] [23]. Figure 6.9 (e) shows that the depletion region at the UID/CGaN interface is narrower in Wafer S2 compared to the REF wafer, indicating a higher density of ionised acceptors at the top of the CGaN region in Wafer S2. Similarly, the depletion region at the CGaN/C:AlGaN interface, shown in Figure 6.9 (f), highlights comparable trends. Wafer S2 shows a greater density of ionised donors at the bottom of the CGaN region, whereas the REF wafer exhibits a lower density of ionised donors. These findings further reinforce the impact of Si doping on charge redistribution within the CGaN layer.

The underlying mechanism behind the current saturation observed at the -300 V bias point in the simulated substrate ramp curves (Figure 6.8) can be summarised as follows:

As previously explained, this phenomenon occurs only if the resistivity of the UID layer is lower than that of the CGaN, allowing electrons to leak into the 2DEG and enabling hole accumulation at the bottom of the CGaN. In these experimental results, this behaviour is typically attributed to trap-assisted tunnelling or hopping along dislocations, as discussed in [14] [22] [23]. However, while these mechanisms are absent in the simulation, the leakage path between the CGaN and the 2DEG is instead modelled using p++ shorts [14].These accumulated holes can either neutralise the ionised acceptors at the top of the CGaN or remain as free charge. In either case, the resulting positive charge screens the 2DEG from the applied negative V_{SUB}, causing the 2DEG to remain independent of the negative bias [19].

As shown in Figure 6.9 (b), the greater positive charge storage in Wafer S2 likely reduces the electric field across the UID region, allowing more electrons to leak into the 2DEG through p-shorts beneath the ohmic contacts in the simulations. This hypothesis is further supported by Figure 6.9 (d), which indicates a higher hole density accumulated at the bottom of the CGaN layer, and Figure 6.9 (c), which shows an increased electron density in the 2DEG region. These findings highlight the key charge transport mechanisms between the UID and CGaN layers, suggesting that the incorporation of Si has facilitated additional electron leakage into the 2DEG. This may also be attributed to the shallow donor states of Si, contributing extra electrons to the system.

Another notable feature is the higher distribution of free holes and electrons within the CGaN region in Wafer S2, as indicated by the simulations, which suggests a reduction in the resistivity of the CGaN layer.

Additionally, the depletion regions of Wafer S2 exhibit a higher density of ionised acceptors at the top, while the bottom of the CGaN region contains a greater density of ionised donors. In contrast, the REF wafer shows a wider depletion region with a lower density of ionised charge. This difference in charge distribution suggests a distinct screening effect in Wafer S2, which likely influences the response to negative V_{SUB}.

Wafer S2 has been chosen for comparison to better highlight the impact of Si incorporation, as the differences between the carbon-only structure and Wafer S1 (5×10^{16} cm^{-3} Si) were relatively minor.

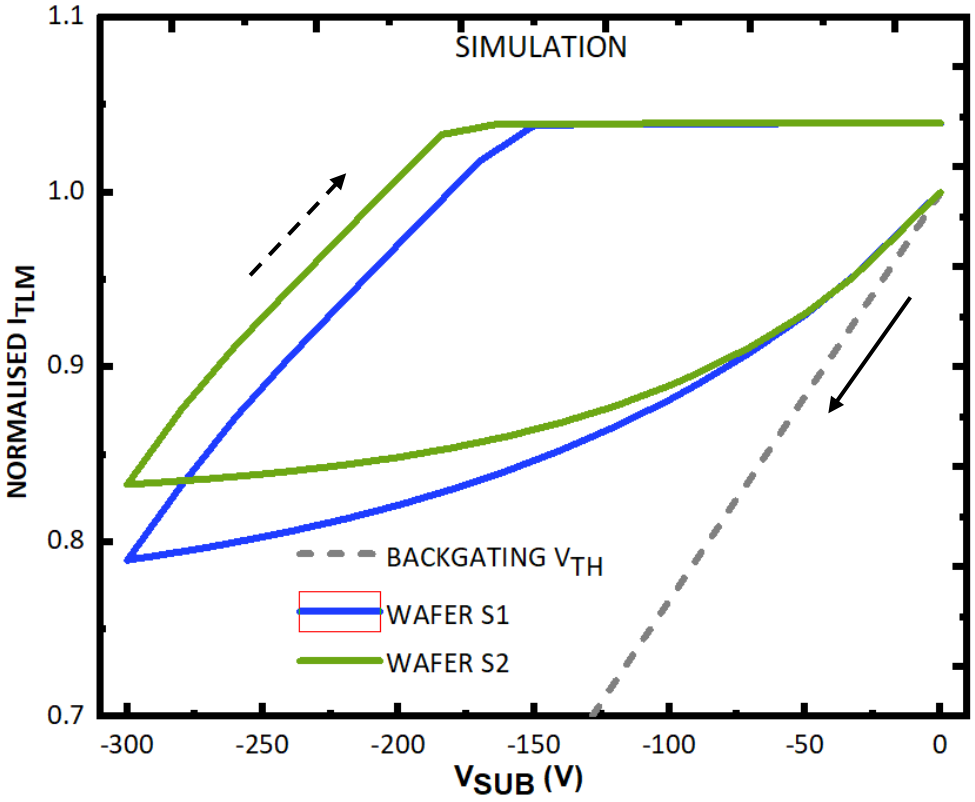

Figure 6-10 - Comparison of simulations between Wafer S1 and Wafer S2. The dashed grey line represents the capacitive coupling line. The solid black arrow indicates the forward sweep (0 V to -300 V), while the dashed black arrow represents the return sweep (-300 V to 0 V).

Figure 6.10 presents the simulated results for Wafers S1 and S2, capturing the qualitative trends observed in the experimental substrate ramp measurements. The results indicate that Wafer S2 exhibits a higher positive charge storage than Wafer S1. This suggests that although the Si doping concentration is two orders of magnitude lower than the carbon doping concentration, the model partially accounts for the contribution of Si to positive charge storage. In contrast to Figure 6.8, at -300 V, the saturated current level of Wafer S1 is slightly higher than that of the REF wafer. This indicates that as Si concentration increases, positive charge storage also increases.

Figure 6.11 (a)–(f) compare the simulated conduction band energy, vertical electric field at the UID/CGaN interface, electron density, hole density, and space charge region at the UID/CGaN and CGaN/C:AlGaN interfaces for Wafers S1 and S2 at V_{SUB} = -300 V. This voltage point corresponds to the plateau region at -300 V in the substrate ramp graph (Figure 6.10).

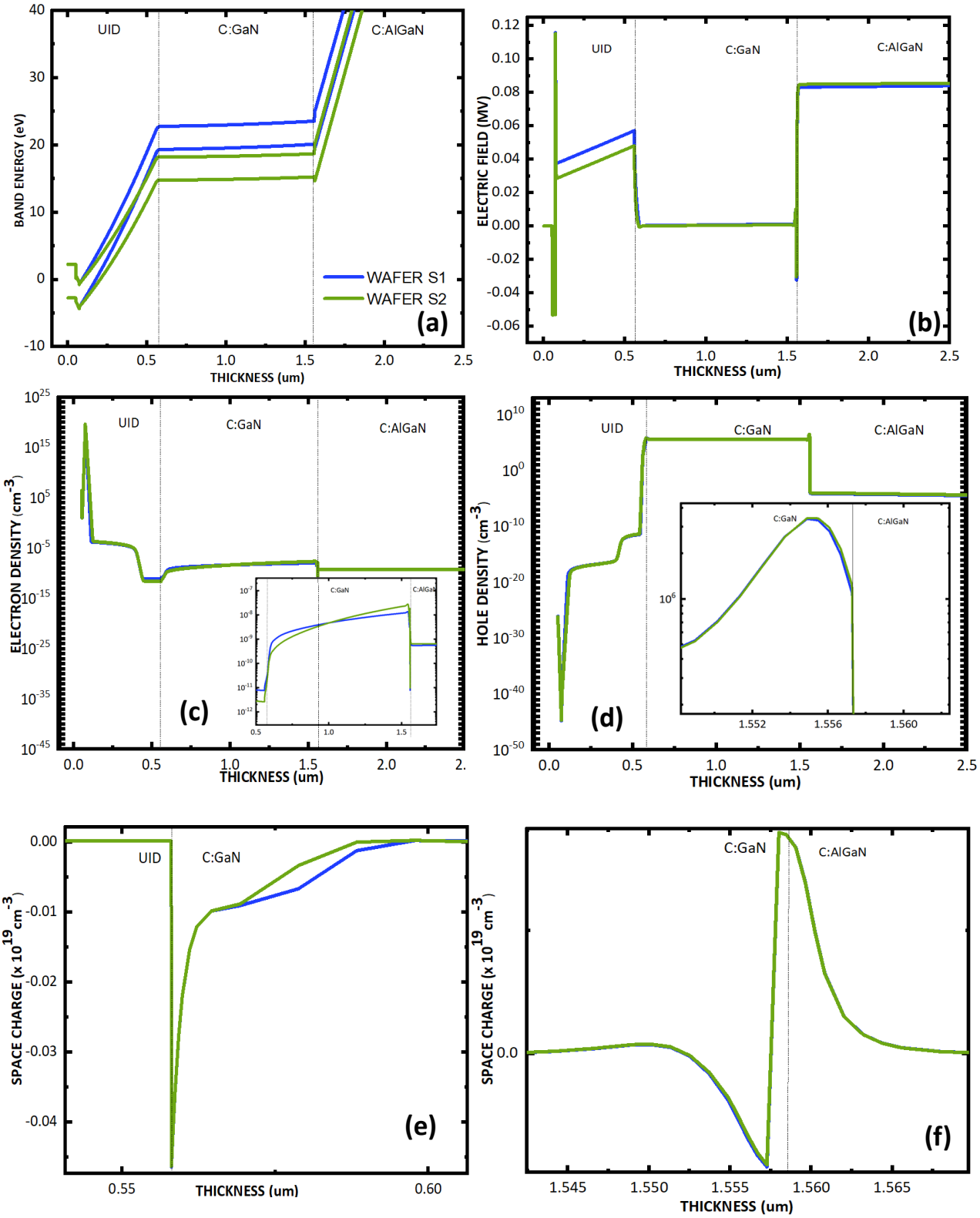

Figure 6-11 - Comparison between the simulated (a) conduction band energy (b) electric field at the UID/CGaN heterojunction (c) electron density (d) hole density (e) the space charge region at the at the UID/CGaN heterojunction and (f) the space charge region at the CGaN/C:AlGaN heterojunction of the Wafer S1 and Wafer S2 , at V_{SUB} = -300 V.

Figure 6.11 (a) and (b) illustrate the band diagrams and electric field profile, showing similar trends to those observed in the first set of simulations (Figure 6.9) without Si incorporation. The reduction in the electric field within the UID region is attributed to enhanced positive charge storage.

Only minor changes can be observed in the electron and hole profiles. Figure 6.11 (c) shows that the 2DEG electron density is higher in Wafer B compared to Wafer S1, which accounts for the observed increase in positive charge storage. Meanwhile, Figure 6.11 (d) indicates a slight increase in hole density at the bottom of the CGaN layer in Wafer S2.

The depletion region at the UID/CGaN interface, as seen in Figure 6.11 (e), reveals a negligible increase in ionised acceptor density, further thinning the depletion region. However, at the CGaN/C:AlGaN heterointerface, an inconsistency is observed—Wafer S1 exhibits a higher ionised donor concentration than Wafer B. One possible explanation is that in Wafer S2, the electron distribution partially shifts towards the bottom of the CGaN layer, leading to neutralisation of some ionised donors.

6.5 Discussion

By combining the experimental results and simulations presented in this chapter, further insight is gained into the impact of Si incorporation on the electrical and structural properties of the CGaN region.

Figure 6.1 illustrates the comparison between the substrate ramp sweeps of Wafers S1, S2, and S3. Prior to current saturation, the normalised channel currents in Wafer S1 are observed below the capacitive coupling line, whereas in both Wafer S2 and S3, the currents move further towards the left side of the capacitive coupling line. Based on the extracted g_m values, Wafer S1 exhibits the highest g_m in comparison with Wafers S2 and S3. As explained in previous chapters, this observed phenomenon of Wafer S1, where the current movement below the capacitive coupling line can be interpreted as the leakage currents within the CGaN layer, is greater than the displacement currents. Conversely, the opposite, where the lower transconductance or left shift of the channel currents is attributed to the leakage currents being lower than the displacement currents.

Charge redistribution within the CGaN layer occurs due to dominant charge transport mechanisms such as hopping conduction, Poole-Frenkel (PF) emission, or tunnelling. While Watch et al. [23] suggest that 3D variable-range hopping best describes this process, the exact mechanism may vary. However, displacement current is fundamentally a function of the capacitance (C) of each layer, given by $C=\varepsilon/d$ [14] [24]. Since the thicknesses of all three wafers remain consistent while all other parameters are similar, the capacitance is expected to remain largely unchanged across the wafers. This means that the displacement currents should also be similar across the wafers.

Figure 6.2 shows that Wafer A exhibits significantly higher leakage currents than the other two wafers. Charge redistribution is driven by charge movement, which is influenced by transport mechanisms such as hopping conduction or PF emission. While it is not entirely certain which layer contributes most to this leakage, the only structural difference among the wafers is the Si concentration in the CGaN layer. Since all other parameters remain consistent, it is plausible that Si doping plays a major role in the increased leakage currents. The observed difference in g_m suggests that the leakage currents are the primary factor driving the variation in transconductance. This further indicates that, in Wafer S1, the leakage currents associated with charge redistribution are greater than the displacement current, compared to the other wafers.

However, the simulated substrate ramp comparison between Wafer S1 and Wafer S2 does not fully capture this distinction observed in the experimental results. The simulations show overlapping normalised channel currents, suggesting that both wafers should exhibit similar transconductance. A plausible explanation for this discrepancy, as discussed in Chapter 5, is that the simulations do not account for charge transport mechanisms such as PF emission or hopping conduction within the epitaxy, leading to an underestimation of leakage currents in the epitaxial layers [23].

One of the key observations is the pronounced gap dependence with increasing Si doping concentration, as shown in Figure 6.5. While the lowest Si doping concentration in Wafer S1 exhibited no clear TLM gap dependence, Wafer S3 demonstrated a pronounced gap dependence in the substrate ramp measurements. Referring to the findings in Chapter 3, it was observed that increasing carbon concentration led to a more pronounced gap independence, implying that vertical leakage across the ohmic contacts became more dominant. However, the wafers examined in this chapter contain a significantly higher carbon doping level (~2×10^{19} cm^{-3}), which is twice the amount used in Chapter 3. This suggests that Si incorporation impacts the lateral resistivity, allowing charge to spread laterally and leak through dislocation paths beneath the contacts. Nevertheless, the exact mechanism behind this increase in lateral resistivity remains unclear at this stage and requires further investigation.

Beyond its influence on lateral resistivity, Si incorporation also appears to impact charge storage behaviour, as seen in the experimental data in Figure 6.1, where Wafer S3 exhibits a higher positive charge storage than Wafer S1:

A possible explanation for the higher positive charge storage in Wafer S3 relates to the observations in Chapter 3. In that chapter, Wafer S3, which had the highest carbon doping concentration, exhibited the lowest overall dislocation density yet showed the highest positive charge storage. It was previously hypothesised that carbon segregation at dislocations enhances vertical leakage paths, facilitating charge transport in the vertical direction and influencing charge storage behaviour.

Applying the same hypothesis to this study, with Si incorporation, it is possible that Si doping similarly enhances the leakage by decorating the dislocations, leading to the higher positive charge storage observed in Wafer S3. However, Figure 6.4 appears to contradict this hypothesis, as it indicates a significantly dominant lateral leakage path, which enhances the gap dependency in Si:C-doped Wafer S3. This suggests that the

positive charge storage in Wafer S3 is more likely facilitated by a dominant lateral leakage path beneath the contacts rather than a vertical leakage path.

This behaviour differs notably from the observations in previous chapters, where charge transport was primarily influenced by vertical leakage through threading dislocations. However, if the proportion of lateral leakage in Si:C Wafer S3 is significantly higher compared to the other wafers, this explanation remains plausible. In contrast, Wafer S1, which exhibits a dominant vertical leakage path across the contacts and has the highest TD density, shows lower positive charge storage. This discrepancy suggests that, irrespective of the number of TDs inherently present in the structure, impurity segregation could also play a crucial role in enhancing the leakage path.

From the perspective of charge storage, the relative resistivity of the upper layers can also be inferred. As discussed in previous chapters, the positive charge storage phenomenon is primarily attributed to leakage between the C:GaN layer and the 2DEG. This implies that the UID layer must have a lower resistivity than the CGaN layer to support this leakage. Based on the trend of increasing positive charge storage with increasing Si concentration, it follows that Wafer S3's UID layer has the lowest resistivity, while Wafer S1's UID layer has the highest resistivity.

However, Figure 6.2 presents an interesting contrast: Wafer S1, which has the lowest Si doping concentration, exhibits the highest substrate leakage, whereas Wafer S3, with the highest Si concentration, shows the lowest substrate leakage currents. This suggests that increasing Si concentration enhances the resistivity of the CGaN layer. Therefore, despite Wafer S3 having the lowest UID resistivity, it paradoxically has the highest CGaN layer resistivity among the three samples.

Above a substrate bias of -300 V, both Wafer S2 and Wafer S3 exhibit a decrease in channel current at approximately -375 V and -325 V, respectively, while Wafer S1 shows a decrease at -450 V, as illustrated in Figure 6.3. This suggests that the bias point at which electron injection from the substrate begins decreases as the Si doping concentration increases. Furthermore, beyond these voltage thresholds, positive charge storage ceases. With a heavy carbon doping level of 2×10^{19} cm^{-3}, the buffer resistivity is primarily governed by carbon. As indicated in Figure 6.4, at a substrate bias of -550 V, the I_{SUB} trends observed in the low-voltage regime persist, with Wafer S3 exhibiting the lowest substrate leakage.

However, based on charge neutrality, the number of negatively charged ionised acceptors at the top of the CGaN layer (-Q) must be equal to the number of positively charged ionised donors (+Q) at the bottom of the CGaN layer [26]. When these accumulated ionised donors are insufficient to screen the increasing V_{SUB}, electron injection into the CGaN buffer may continue [19] [25]. As observed in Figure 6.11 (f), the density of ionised positively charged donors follows a decreasing trend with increasing Si doping concentration. This suggests that Wafer S3, with the highest Si doping concentration, is likely to have the lowest density of ionised donors. Consequently, electron injection may commence at a relatively lower voltage for Wafer S3 compared to Wafer S1.

How efficiently the epitaxial layer can discharge trapped charge and suppress dynamic R_{ON} is a crucial factor in determining the most suitable dopants for insulating the buffer. This was evaluated using substrate transient measurements, where Wafer S1 exhibited the fastest recovery (Figure 6.6(b)), followed by Wafer S2 and then Wafer S3, with time constants of 44.5 s, 58.5 s, and 110.8 s, respectively. The differences in time constants may be attributed to the preferred leakage paths. In Wafer S3, the lateral leakage path appears to be dominant due to the increased Si concentration, requiring a longer time for electrons to return to the CGaN layer and neutralise the accumulated positive charge.

Beyond the electrical characteristics, the correlation between buffer properties and Si incorporation also highlights structural changes. The observed variation in TDD strongly suggests that increasing Si doping concentration influences the structural properties and, consequently, the crystal quality. As shown in Table 6.2, the FWHM values decrease with increasing Si doping concentration, indicating an improvement in crystal quality. Although the overall Si doping levels remain significantly lower than the total carbon concentration, the observed reduction in dislocations with increasing Si concentration suggests that Si plays a role in mitigating dislocation propagation. A plausible explanation is that the tensile strain introduced by Si incorporation counterbalances the existing compressive strain. Dadgar et al. [25] reported that Si doping generates strong tensile stress in the epitaxial layer, primarily dictated by edge dislocation density. Similarly, Moram et al. [7] observed significantly higher dislocation densities in Si-doped GaN films, concluding that Si influences dislocation distribution due to the tensile strain it introduces. A common factor in these studies is the comparison of Si-doped GaN with unintentionally doped GaN, supporting the conclusion that Si incorporation leads to additional dislocations due to tensile strain. Since Si preferentially substitutes Ga atoms

in GaN [2], and has a smaller atomic radius ($r_{Si} < r_{Si}$), the lattice undergoes contraction, introducing tensile strain.

In this study, TD densities of the wafers do not show a dramatic variation compared to carbon-doped wafers in Chapter 3. This suggests that changes in the intrinsic lattice parameter, due to intentional carbon and Si incorporation, may be an alternative source of tensile stress in the C-Si co-doped GaN layer. With a high carbon concentration of 2×10^{19} cm^{-3}, tri-carbon defect formation is likely [26] [27] [10], and could help counterbalance the tensile stress [26] [28]. Additionally, the presence of Si can lead to the formation of stable Si_{Ga} defects. Irmscher et al. [27], further emphasised that tri-carbon defect complexes primarily consist of acceptor-like C_N–C_{Ga}–C_N, with no other impurity species involved.

Carbon is not a dominantly electrically active impurity, and C_N defects are not only passivated by background shallow donors but also influenced by C_{Ga} and Si doping concentrations. Richter et al [26] concluded that the resistivity reaches a maximum at an optimal carbon concentration of ~ 1 x $10^{19}cm^{-3}$ then it saturates, beyond which the donor compensation becomes significant, meaning the balance between these acceptor or acceptor complexes and donor type defects varies depending on the carbon concentration (which was explained in Chapter 3). While both C_N and the C_N-C_{Ga}-C_N complexes act as acceptors, C_{Ga} and the Si_{Ga} substitutionally incorporated at the Ga site form the donors, leading to the self-compensation.

Si_{Ga} and C_{Ga}, both replacing Ga atoms in the lattice, are prominent donor-like defects. Si_{Ga} is a shallow donor, while C_{Ga} is a deep donor. As Si_{Ga} has a much lower formation energy than C_{Ga}, Si is more likely to occupy Ga sites [2] [27]. In heavily carbon-doped GaN, C_{Ga} formation energy decreases, increasing its likelihood of C_{Ga} being formed, however, Si_{Ga} still maintains a lower formation energy. Thus, increasing Si doping concentration favours Ga site occupancy, reducing C incorporation at Ga sites [9].

Although the Si doping concentrations used in this study are relatively low, they may influence the contribution of C_{Ga} donors to the overall compensation ratio. This suggests that even small amounts of Si incorporation can alter the compensation mechanism and, consequently, affect the buffer resistivity. The experimental results in this chapter demonstrate that increasing Si doping concentration enhances buffer resistivity, likely due to increased donor compensation particularly for high carbon concentration such as 2x$10^{19}cm^{-3}$. This is further supported by the observation that, during the -300 V substrate

ramp, charge redistribution was progressively suppressed as Si concentration increased. However, while Wafer S3 exhibits the most resistive C:GaN buffer characteristics, it also shows the poorest dynamic R_{ON} performance. This trade-off suggests that while higher Si doping can enhance buffer insulation, it may also introduce limitations in charge transport dynamics, adversely impacting dynamic R_{ON} behaviour.

6.6 Conclusions

This study examined the impact of Si co-doping in the CGaN layer on the dynamic R_{ON} of MOCVD-grown AlGaN/GaN HEMTs on Si substrate. Experimental results, supported by HRXRD, substrate ramp, and transient measurements, indicate that increased Si doping prolongs recovery times, thereby increasing dynamic R_{ON}.

The findings suggest that increasing the Si doping concentration in heavily carbon-doped CGaN does not negatively impact the lattice constant or deteriorate crystal quality. HRXRD results indicate that higher Si concentrations show resilience to forming high dislocation densities, whereas dislocation density remains a significant factor limiting charge transport in these wafers. This implies that Si incorporation does not introduce new dislocations but instead mitigates dislocation propagation. A plausible explanation is that the tensile strain induced by Si counterbalances the existing compressive strain from carbon impurities, thereby reducing the formation of new dislocations.

A monotonic relationship between Si doping concentration and positive charge storage was observed, with Wafer S3 exhibiting the highest positive charge storage during the substrate ramp. This is likely due to an increased ionised donor density accumulating at the bottom of the CGaN layer, which screens the electric field and prevents 2DEG depletion. Alternatively, it is also plausible that a dominant lateral leakage path facilitates efficient charge transport between the CGaN layer and the 2DEG, allowing electrons to leak into the 2DEG. Although this hypothesis appears to contradict findings from previous chapters, it remains unclear whether lateral leakage could also contribute to charge transport in this scenario. The precise mechanism underlying this enhanced positive charge storage remains uncertain and requires further investigation.

In both low and high V_{SUB} regimes, Wafer S3 exhibited the lowest leakage currents, indicating that the CGaN layer in Wafer S3 has higher resistivity than that of Wafer S1. Additionally, in terms of crystal quality, Wafer S3 demonstrates superior structural properties compared to Wafer S1, which may further contribute to reduced substrate leakage currents.

At a high V_{SUB} of -550 V, Wafer S3 exhibited an earlier reduction in channel current compared to the other wafers, likely due to insufficient ionised donor accumulation at the bottom of the CGaN layer to effectively screen the electric field.

Wafer S3 exhibited a pronounced gap dependence, suggesting enhanced lateral charge transport, likely due to Si doping reducing lateral resistivity and thereby promoting a dominant lateral leakage path. In contrast, Wafer S1 showed no such dependence, indicating that its primary leakage mechanism occurs uniformly across the entire ohmic gap spacing. This observation aligns with findings from Chapter 3, reinforcing the initial hypothesis. Notably, the Si concentration in Wafer S1 is comparable to the expected background doping level, whereas in Wafer S3, it is an order of magnitude higher. However, definitive conclusions cannot be drawn without further experimental verification to determine whether a specific Si doping threshold influences dynamic R_{ON} due to the prevalence of lateral leakage.

Wafer S2 and Wafer S3 did not fully recover to their initial state within the measurement time window, suggesting prolonged recovery times. This is likely due to reduced vertical conduction along dislocations, potentially influenced by the increased resistivity of the CGaN layer.

These findings indicate that while intentional Si doping does not degrade crystal quality and is beneficial for controlling the n-type conductivity of the GaN layer, it is not suitable at high densities for incorporation into the CGaN buffer as a co-dopant to control the compensation ratio and resistivity. Instead, high-density Si doping primarily alters vertical conductivity, which enhances lateral conduction but also negatively impacts overall device performance by exacerbating dynamic R_{ON}.

6.7 References

[1] Z. Shen, X. Yang, S. Wu, H. Huang, X. Yan, N. Tang, F. Xu, X. Wang, W. Ge, B. Huang and B. Shen, "Mechanism for self-compensation in heavily carbon doped GaN," AIP advances, vol. 13, no. 3, pp. 035026-035026–5, 2023-03.

[2] J. Neugebauera and C. Van de Walle, "Gallium vacancies and the yellow luminescence in GaN," Applied physics letters, vol. 69, no. 4, pp. 503-505, 1996-07.

[3] A. Lesnik, M. P. Hoffmann, A. Fariza, J. Bläsing, H. Witte, P. Veit, F. Hörich, C. Berger, J. Hennig, A. Dadgar and A. Strittmatter, "Properties of C-doped GaN," Physica Status Solidi (B) Basic Research, vol. 254, no. 8, 2017.

[4] B. E. Gaddy, Z. Bryan, I. Bryan, J. Xie, R. Dalmau, B. Moody, Y. Kumagai, T. Nagashima, Y. Kubota, T. Kinoshita, A. Koukitu, R. Kirste, Z. Sitar, R. Collazo and D. Irving, "The role of the carbon-silicon complex in eliminating deep ultraviolet absorption in AlN," Applied physics letters, vol. 104, no. 20, p. 202106, 2014-05.

[5] A. F. Wright, "Substitutional and interstitial carbon in wurtzite GaN," Journal of applied physics, vol. 92, no. 5, pp. 2575-2585, 2002-09.

[6] T. Mattila and R. M. Nieminen, "Point-defect complexes and broadband luminescence in GaN and AlN," Physical review. B, Condensed matter, vol. 55, no. 15, pp. 9571-9576, 1997-04.

[7] M. A. Moram, M. J. Kappers, F. Massabuau, R. A. Oliver and C. J. Humphreys, "The effects of Si doping on dislocation movement and tensile stress in GaN films," Journal of applied physics, vol. 109, no. 7, pp. 073509-073509-7, 2011-04.

[8] A. Agarwal, C. Gupta, Y. Enatsu, S. Keller and U. Mishra, "Controlled low Si doping and high breakdown voltages in GaN on sapphire grown by MOCVD," Semiconductor science and technology, vol. 31, no. 12, p. 125018, 2016-11.

[9] H. Tokuda, K. Suzuki, J. T. Asubar and M. Kuzuhara, "Electron concentration in highly resistive GaN substrates co-doped with Si, C, and Fe," Japanese Journal of Applied Physics, vol. 57, no. 7, p. 71001, 2018.

[10] A. Honda, H. Watanabe, W. Takeuchi, Y. Honda, H. Amano and T. Kato, "Investigation of carbon-related complexes in highly C-doped GaN grown by metalorganic vapor phase epitaxy," Japanese Journal of Applied Physics, vol. 63, no. 4, p. 41005, 2024-04.

[11] J. Bai, T. Wang, P. Parbrook, K. Lee and A. Cullis, "A study of dislocations in AlN and GaN films grown on sapphire substrates," Journal of crystal growth, vol. 282, no. 3-4, pp. 290-296, 2005.

[12] M. Barchuk, C. Röder, Y. Shashev, G. Lukin, M. Motylenko, J. Kortus, O. Pätzold and D. Rafaja, "Correlation between the residual stress and the density of threading dislocations in GaN layers grown by hydride vapor phase epitaxy," Journal of crystal growth, vol. 386, p. 1–8, 2014.

[13] A. Wickenden, D. Koleske, R. Henry, M. Twigg and M. Fatemi, "Resistivity control in unintentionally doped GaN films grown by MOCVD," Journal of crystal growth, vol. 260, no. 1, p. 54–62, 2004.

[14] M. Uren, S. Karboyan, I. Chatterjee, A. Pooth, P. Moens, A. Banerjee and M. Kuball, "Leaky Dielectric" Model for the Suppression of Dynamic Ron in Carbon-Doped AlGaN/GaN HEMTs," IEEE Transactions on Electron Devices, vol. 64, p. 2826–2834, 2017.

[15] M. J. Uren, M. Silvestri, M. Casar, G. A. M. Hurkx, J. A. Croon, J. Sonsky and M. Kuball, "Intentionally Carbon-Doped AlGaN/GaN HEMTs: Necessity for Vertical Leakage Paths," IEEE Electron Device Letters, vol. 35, no. 3, pp. 327-329, 2014.

[16] I. Chatterjee, M. J. Uren, S. Karboyan, A. Pooth, P. Moens, A. Banerjee and M. Kuball, "Lateral Charge Transport in the Carbon-Doped Buffer in AlGaN/GaN-on-Si HEMTs," IEEE transactions on electron devices, vol. 64, no. 3, p. 977–983, 2017.

[17] A. Nardo, C. De Santi, C. Koller, C. Ostermaier, I. Daumiller, G. Meneghesso, E. Zanoni and M. Meneghini, "Positive and negative charge trapping GaN HEMTs: Interplay between thermal emission and transport-limited processes," Microelectronics Reliablity, vol. 126, p. 114255, 2021.

[18] D. Bisi, M. Meneghini, C. de Santi, A. Chini, M. Dammann, P. Bruckner, M. Mikulla, G. Meneghesso and E. Zanoni, "Deep-Level Characterization in GaN HEMTs-Part I: Advantages and Limitations of Drain Current Transient Measurements," IEEE transactions on electron devices, vol. 60, no. 10, pp. 3166-3175, 2013-10.

[19] F. M. Watch, "Electrical and Thermal Characterisation of GaN-based Devices for RF and Power," University of Bristol , Bristol, 2022.

[20] M. L. Colussi, R. J. Baierle and R. H. Miwa, "Doping effects of C, Si and Ge in wurtzite [0001] GaN, AlN, and InN nanowires," Journal of applied physics, vol. 110, no. 3, pp. 033709-033709-9, 2011-08.

[21] S. Mu, M. Wang, J. B. Varley, J. L. Lyons, D. Wickramaratne and C. G. Van de Walle, "Role of carbon and hydrogen in limiting n -type doping of monoclinic (AlxGa1–x)2O3," Physical review. B,, vol. 105, no. 15, p. 155201, 2022-04.

[22] M. Millesimo, M. Borga, L. Valentini, B. Bakeroot, N. Posthuma, A. Vohra, S. Decoutere, C. Fiegna and A. N. Tallarico, " Role of the GaN-on-Si Epi-Stack on Δ R ON Caused by Back-Gating Stress," IEEE transactions on electron devices, vol. 70, no. 10, pp. 5203-5209, 2023-10.

[23] F. Wach, M. J. Uren, B. Bakeroot, M. Zhao, S. Decoutere and M. Kuball, “Low Field Vertical Charge Transport in the Channel and Buffer Layers of GaN-on-Si High Electron Mobility Transistors,” IEEE electron device letters, vol. 41, no. 12, pp. 1754-1757, 2020-12.

[24] W. M. Waller, M. Gajda, S. Pandey, J. J. T. M. Donkers, D. Calton, J. Croon, J. Sonsky, M. J. Uren and M. Kuball, “Control of Buffer-Induced Current Collapse in AlGaN/GaN HEMTs Using SiNx Deposition,” IEEE transactions on electron devices, , Vol.), p., Article 8013764, vol. 64, no. 10, pp. 4044-4049, 2017-10.

[25] A. Dadgar, P. Veit, F. Schulz, J. Blasing, A. Krtschil, H. Witte, A. Diez, T. Hempel, J. Christen, R. Clos and A. Krost, “MOVPE growth of GaN on Si – Substrates and strain,” Thin Solid Films, vol. 515, no. 10, pp. 4356-4361, 2007-03.

[26] E. Richter, F. C. Beyer, F. Zimmermann, G. Gärtner, K. Irmscher, I. Gamov, J. Heitmann, M. Weyers and G. Tränkle, “Growth and Properties of Intentionally Carbon-DopedGaN Layers,” Crystal research and technology (1979), , vol. 55, no. 2, p. 1900129, 2020-02 .

[27] K. Irmscher, C. Hartmann, C. Guguschev, M. Pietsch, J. Wollweber and M. Bickermann, “Identification of a tri-carbon defect and its relation to the ultraviolet absorption in aluminum nitride,” Journal of applied physics, vol. 114, no. 12, p. 123505, 2013-09.

[28] I. Gamov, E. Richter, M. Weyers, G. Gärtner and K. Irmscher, “Carbon doping of GaN: Proof of the formation of electrically active tri-carbon defects,” Journal of applied physics, vol. 127, no. 20, pp. 205701-8, 2020-05.

[29] S. Ito, H. Kobayashi, K. Araki, K. Suzuki, N. Sawaki, K. Yamashita, Y. Honda and H. Amano, “Resonant Raman and FTIR spectra of carbon doped GaN,” Journal of Crystal Growth, vol. 414, pp. 56-61, 2015.

[30] Y. Xu, X. Yang, P. Zhang, X. Cao, Y. Chen, S. Guo, S. Wu, J. Zhang, Y. Feng, F. Xu, X. Wang, W. Ge and B. Shen, “Influence of intrinsic or extrinsic doping on lattice locations of carbon in semi-insulating GaN,” Applied physics express, vol. 12, no. 6, pp. 61002,, 2019-06.

[31] M. Singh, S. Karboyan, M. J. Uren, K. B. Lee, Z. Zaidi, P. A. Houston and M. Kuball, “Lateral charge spreading and device-to-device coupling in C-doped AlGaN/GaN-on-Si wafers,” Microelectronics Reliability, vol. 95, pp. 81-86, 2019.

[32] M. J. Uren, M. Cäsar, M. A. Gajda and M. Kuball, “Buffer transport mechanisms in intentionally carbon doped GaN heterojunction field effect transistors,” Applied physics letters, vol. 104, no. 26, pp. 1077-3118, 2014.

[33] S. Yang, C. Zhou, S. Han, J. Wei, K. Sheng and K. J. Chen, “Impact of substrate bias polarity on buffer-related current collapse in AlGaN/GaN-on-Si power devices,” IEEE Transactions on Electron Devices, vol. 64, no. 12, pp. 5048-5056, 2017.

[34] R. Kabouche, I. Abid, R. Püsche, J. Derluyn, S. Degroote, M. Germain, A. Tajalli, M. Meneghini, G. Meneghesso and F. Medjdoub, “Low On-Resistance and Low Trapping Effects in 1200 V Superlattice GaN-on-Silicon Heterostructures,” Physica status solidi. A, Applications and materials science, vol. 217, no. 7, pp. 1900687 1-6, 2020-04.

7. Conclusions & Future Work

This thesis encompasses mask design, device fabrication, device modelling, and the structural and electrical characterisation of the AlGaN/GaN HEMT structure. The primary focus is to investigate how various buffer parameters influence the dynamic R_{ON} of AlGaN/GaN HEMTs on Si. A combination of experimental techniques including substrate ramp and transient measurements, HRXRD, and TEM alongside TCAD simulations, has been employed to analyse the underlying mechanisms contributing to dynamic R_{ON}. This chapter summarises the key findings of these chapters and the future work.

7.1 Dynamics of Carbon Doping in the C:GaN Buffer Layer

Carbon has been extensively studied and widely used in GaN power devices; however, many of its behaviours remain insufficiently understood. This chapter investigates the influence of varying carbon doping concentrations in the CGaN buffer layer of a 650V-rated AlGaN/GaN HEMT, linking the charge transport mechanisms and crystal quality.

HRXRD analysis revealed that crystal quality improved with increasing carbon doping concentration (2×10^{18} cm^{-3} to 1×10^{19} cm^{-3}), challenging prior studies that suggested higher carbon incorporation degrades material quality. A key observation was that edge dislocations were more dominant than screw dislocations, with the overall reduction in dislocation density. This reduction is likely facilitated by tri-carbon defect formation, which alleviates strain and reduces threading dislocations. Substrate ramp measurement revealed that higher carbon concentrations enhanced vertical leakage pathways, attributed to impurity segregation at dislocation cores, even as dislocation density decreased. Substrate transient measurements further demonstrated faster recovery dynamics within the measurement time, with increased carbon content, indicating that carbon does not degrade dynamic R_{ON}. This is the first study to show that increasing carbon doping does not degrade dynamic R_{ON}.

Finally, high-voltage measurements approaching nominal breakdown voltage revealed that the wafer with the highest carbon doping exhibited electron injection from the substrate at a lower substrate voltage than the other two wafers. This behaviour suggests that highly doped wafers reach charge storage saturation sooner, preventing further accumulation, while wafers with lower carbon concentrations continue storing positive

charge until they reach saturation, at which point electron injection from the substrate begins.

Together, these results highlight that leakage and dynamic behaviour are governed not solely by dislocation density, but by the complex role of carbon in mediating charge transport along extended defects.

7.2 Fine-Tuning Dynamic On-Resistance: Unravelling the Impact of Thickness Variations in Heavily Carbon-Doped GaN Layer and the UID layer

This study specifically investigates how these thickness variations influence dynamic R_{ON}. Two groups of wafers were examined to gain insights into the role of both the UID layer and C:GaN buffer layer thickness.

- Group A: Only the C:GaN thickness was varied.
- Group B: Both UID and C:GaN thicknesses were adjusted while maintaining a constant total stack thickness.

HRXRD analysis revealed that increasing CGaN thickness led to higher TD density and deterioration of crystal quality in both groups, reinforcing a strong correlation between layer thickness and dislocation behaviour. TEM analysis confirmed that TD bunching effects became more prominent as the CGaN thickness decreased, effectively reducing the observed dislocation density.

Substrate ramp measurements revealed that the wafer with the thickest CGaN layer for both groups exhibits the highest positive charge storage, but at the expense of slower recovery and degraded dynamic R_{ON}, particularly when combined with a thin UID layer. This behaviour suggests that increased dislocation density enhances the vertical leakage currents, aligning with the expected dominant vertical leakage path. As all wafers exhibited weakly gap-dependent behaviour, this further reinforces the hypothesis that gap-dependent behaviour is primarily linked to carbon doping concentration rather than thickness variations. A plausible additional contributing mechanism is that increased dislocation density effectively reduces the depletion region at the UID/CGaN interface, lowering the diffusion barrier and facilitating higher electron leakage into the 2DEG along the reverse-biased PN junction.

Transient measurements demonstrated that the wafers with lower dislocation density exhibited a faster recovery and improved dynamic performance, underscoring the role of

dislocations as leakage pathways. The worst dynamic R_{ON} was consistently observed in wafers, with the thickest CGaN layer, with Group B, further highlighting the detrimental effect of combining a thin UID with a thick C:GaN, likely due to the closer proximity of the 2DEG to the UID/CGaN space charge region.

Overall, while thicker C:GaN buffers help suppress leakage and improve breakdown characteristics, they do not necessarily optimise dynamic R_{ON}. Instead, UID resistivity and dislocation density together determine the balance between breakdown robustness and dynamic performance. Simulations supported these findings by showing how thickness variations reshape capacitance and electric field distribution, illustrating the inherent trade-offs in buffer design.

7.3 Interplay between the Carbon Doping Concentration, Threading Dislocations and Dynamic R_{ON} in the C:GaN/AlN superlattice

While the CGaN layer remains the primary focus of this thesis, it is equally important to examine how charge storage is influenced by the properties of neighbouring layers, such as the UID, as explored in the previous study. This study investigated the impact of carbon doping concentration in the SRL on dynamic R_{ON}, demonstrating its role in vertical isolation, leakage behaviour and charge trapping.

HRXRD analysis revealed that the SRL with higher carbon concentrations (approximately $2x10^{19}cm^{-3}$) exhibited superior crystal quality, despite similar C:GaN carbon levels in both wafers. Interestingly, substrate ramp measurements showed distinct transport behaviours: the wafer with higher SRL carbon displayed a dominant vertical leakage path and greater positive charge storage, while the wafer with lower SRL carbon exhibited more lateral leakage and lower charge storage. Notably, the lower-carbon ($2x10^{18}cm^{-3}$) wafer also showed higher leakage currents overall and electron injection from the substrate at relatively low voltages, consistent with its reduced SRL resistivity and higher dislocation density.

The TCAD simulation model showed that a highly resistive SRL reduces the electric field in the upper device layers, as the larger field drop occurs in the SRL. This confirms the critical role of carbon in leakage behaviour, enhancing the resistivity of the bottom layers. It is also widely known that higher electric fields in the top layers can lead to current collapse; therefore, it is crucial to ensure that the majority of the electric field is

dropped at the SRL. This emphasises the importance of selecting an optimal carbon concentration, not only for CGaN but also for the SRL.

7.4 Impact of Si Co-Doping on Dynamic RON in Heavily Carbon-Doped GaN Buffer Layers

The final chapter presents the first experimental evidence of how silicon incorporation into heavily carbon-doped buffer influences on dynamic R_{ON}, based on substrate ramp and substrate transient measurements. Three nominally identical wafers with varying Si doping concentrations ($5 \times 10^{16} cm^{-3}$, $1 \times 10^{17} cm^{-3}$ and 5×10^{17} cm^{-3}) were studied, while the carbon doping concentration remained constant at $2 \times 10^{19} cm^{-3}$.

A reduction in the TDs was observed with increasing Si doping concentration, demonstrating that Si incorporation into a heavily carbon-doped CGaN layer does not negatively impact the lattice constant or degrade crystal quality. It may, in fact, alleviate carbon-induced strain by partially compensating compressive stress.

Substrate ramp measurements highlighted that the higher Si doping levels exhibit the greater positive charge storage and a pronounced gap dependence, suggesting enhanced lateral leakage pathways and modified charge transport between the CGaN buffer and the 2DEG. Furthermore, the highest Si concentration resulted in the lowest leakage currents, indicating higher buffer resistivity compared to the wafer with the lowest Si content, as well as superior crystal quality. Under a high substrate voltage of -550 V, however, high Si doping concentration led to electron injection from the Si at lower voltages. This may be due to insufficient ionised donor accumulation at the bottom of the CGaN layer, preventing effective screening of the electric field, as predicted by the simulation.

Substrate transient analysis indicated that the wafer with the lowest Si concentration recovered to its initial state, whereas the wafer with higher Si concentration required prolonged recovery times. The rapid recovery of the lowest Si wafer could be due to the dominant vertical leakage path, while the incomplete recovery of the higher-Si wafers points to reduced vertical conduction along dislocations and the increased resistivity of the C:GaN layer.

Overall, these findings suggest that Si incorporation into a carbon-doped buffer can improve crystal quality and resistivity, but at the expense of stable dynamic R_{ON}

performance. Optimisation of co-doping therefore requires balancing the benefits of higher resistivity with the drawbacks of enhanced charge trapping and slower recovery.

In summary, the results of this thesis collectively indicate that no single buffer parameter alone determines dynamic R_{ON} performance in GaN-on-Si HEMTs. Rather, it is the interplay between doping, thickness, and strain management across multiple layers that governs device behaviour. The optimal buffer, based on the combined evidence, would likely consist of a moderately carbon-doped GaN layer (sufficient to enhance resistivity without excessive vertical leakage), supported by a well-engineered superlattice strain relief layer with carefully balanced carbon incorporation to control dislocation density and electric field distribution. Co-doping strategies, such as the inclusion of Si at controlled concentrations, show promise for reducing dislocation densities and improving resistivity, but must be tuned to avoid excessive charge storage and dynamic R_{ON} degradation. An optimum design, therefore, involves a balance: high resistivity in the lower buffer to suppress leakage, controlled dislocation densities to enhance recovery dynamics, and tailored doping profiles that maintain crystal quality while mitigating trapping.

7.5. Future work

This study has explored not only buffer trapping but also defect densities and their impact on charge transport. Understanding how dislocations influence charge movement beyond the surface is particularly crucial in relation to silicon and carbon doping in the CGaN and SRL layers. Advanced characterisation techniques such as Conductive Atomic Force Microscopy(CAFM) will be instrumental in mapping dislocations and visualising their effect on leakage paths at the nanoscale. Additionally, cross-sectional TEM will provide direct insight into dislocation interactions with dopants, clarifying their role in charge trapping and vertical leakage. These techniques will complement the HRXRD findings by offering a more comprehensive understanding of strain distribution and relaxation processes.

Moreover, this study lacks thermal characterisation, which is an essential part of extracting activation energies of dominant trapping mechanisms and understanding the behaviour of incorporated dopants, key factors influencing dynamic R_{ON} recovery. Temperature-dependent transient measurements will further clarify charge redistribution under varying voltage conditions, reinforcing the relationship between doping concentration, leakage behaviour, and the long-term reliability of GaN HEMTs. Additionally, the TCAD model used in this study requires refinement to incorporate

additional vertical leakage mechanisms, such as Poole-Frenkel emission, to better align with experimental observations and improve predictive accuracy.

Looking forward, based on the observations in this study, industry research in buffer structures for power HEMT devices should prioritise:

- Developing co-doping strategies and their compensation mechanisms that simultaneously enhance buffer resistivity while minimising the associated structural defects.
- Dislocation engineering, refining buffer designs (such as superlattices, compliant substrates, hybrid nucleation/buffer stacks, or hybrid multi-doped buffer structures) to achieve an optimal balance between resistivity and dislocation filtering, alongside investigations of vertical conductivity within the device, which this study has shown plays a crucial role in achieving stable dynamic R_{ON} characteristics.
- Advanced characterisation, employing a combination of nanoscale techniques such as conductive AFM (CAFM), scanning transmission electron microscopy with electron energy loss spectroscopy (STEM/EELS), atom probe tomography, and time-resolved or in-situ methods (e.g. deep-level transient spectroscopy, scanning probe spectroscopy under bias) to directly correlate trap states with dopant distributions and device behaviour.
- Thermal reliability studies systematically evaluating the trapping and detrapping dynamics across both high-temperature and cryogenic regimes, as well as under high-field operation, to inform the design of buffer structures with long-term electrical and structural stability.

These directions will not only address the immediate challenge of dynamic R_{ON} but also underpin the development of GaN buffers capable of supporting the higher voltages and reliability standards demanded by next-generation power electronics.