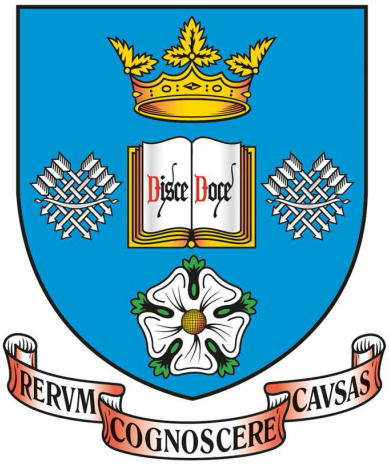
Power Semiconductor Devices and Technologies for High Power Density and Efficiency Converters



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A Thesis submitted for the Degree of

Doctor of Philosophy

in the Faculty of Engineering

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to my family

Acknowledgement

As the writing of this thesis is coming to an end, I would like to dedicate a few lines for people who made this journey pleasant and insightful and to reflect on this wonderful experience. This PhD has been one of my most enriching and challenging experiences that I have ever undertaken.

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Alireza Sheikhan, July 2025

Sheffield, United Kingdom

Abstract

The emergence of wide bandgap power semiconductor device technologies has paved the path toward higher power densities and efficiency across a broad spectrum of applications. One of the leading device candidates is gallium nitride (GaN) based high electron mobility transistor (HEMT). The ability to grow high quality GaN epitaxial layers on inexpensive large diameter foreign wafers such as sapphire or silicon has made lateral GaN power devices an attractive choice for power devices.

This thesis presents for the first time the device physics, detailed characteristics, and circuit performance of high voltage GaN HEMTs based on a new technology referred to as polarisation superjunction (PSJ). The PSJ technology permits the design of high-voltage, high-performance diodes and switches with the prospective blocking voltage of up to 10 kV in a cost-effective manner.

According to the experimental results, PSJ devices offer an on-state resistance beyond the one-dimensional material limit but without the limitations of conventional HEMTs such as dynamic on-resistance. This is because of the uniformly distributed electric field due to the charge balance arising from the coexistence of positive and negative polarisation charges in a double heterojunction. PSJ GaN devices can operate effectively across a broad spectrum of conditions which renders them suitable for a variety of power electronic applications. One of the challenges in GaN HEMTs is their normally-on characteristic which is not desirable from a fail-safe requirements point of view. Thus, methods of normally-off configurations have been explored using cascode and direct drive configurations.

Additionally, detailed analysis of hybrid power switches (HPS) based on the latest silicon (Si), silicon carbide (SiC), and GaN technologies have been presented. The HPS is designed to provide high performance at a competitive cost, by combining the advantages of bipolar and unipolar device technologies. The results show that the HPS can effectively offer MOSFET-like switching performance while having the high current capability of the IGBT.

Contents

List of Publications

Parts of the content presented in this thesis have been disseminated in the following publications:

1. **A. Sheikhan**, G. Narayanankutty, E. M. S. Narayanan, H. Kawai, S. Yagi and H. Narui, "Analysis of 1.2 kV GaN polarisation superjunction diode surge current capability," Japanese Journal of Applied Physics, vol. 62, no. 1, p. 014501, 2023. DOI: https://doi.org/10.35848/1347-4065/aca853

2. **A. Sheikhan**, G. Narayanankutty, E. M. S. Narayanan, H. Kawai, S. Yagi and H. Narui, "Erratum: Analysis of 1.2 kV GaN polarization superjunction diode surge current capability [Jpn.J. Appl. Phys. 62 014501 (2023)]," Japanese Journal of Applied Physics, vol. 62, no. 3, p. 039401, 2023. DOI: https://doi.org/10.35848/1347-4065/acb819

3. **A. Sheikhan**, E. M. S. Narayanan, H. Kawai, S. Yagi and H. Narui, "Evaluation of turn-off dV/dt controllability and switching characteristics of 1.2kV GaN polarisation superjunction HFETs," Japanese Journal of Applied Physics, vol. 62, p. 064502, 2023. DOI: https://doi.org/10.35848/1347-4065/acd975

4. **A. Sheikhan** and E. M. S. Narayanan, "Evaluation of characteristics and turn-off dV/dt controllability of 1.2 kV SiC Si hybrid power switch," in 16th International Seminar on Power Semiconductors (ISPS), Prague, 2023. DOI: https://doi.org/10.14311/isps.2023.010

5. **A. Sheikhan,** E. M. S. Narayanan, H. Kawai, S. Yagi and H. Narui, "Evaluation of a 3 kV Polarization Superjunction GaN HEMT," in International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM), Nuremberg, 2024. DOI: https://doi.org/10.30420/566262068

6. **A. Sheikhan** and E. M. S. Narayanan, “Evaluation of a Hybrid Power Switch Based on Trench Clustered IGBT and SiC MOSFET,” in International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM), Nuremberg, 2024. DOI: https://doi.org/10.30420/566262364

7. **A. Sheikhan** and E. M. S. Narayanan, “Characteristics of a 1200 V Hybrid Power Switch Comprising a Si IGBT and a SiC MOSFET,” in Preprint, 2024. DOI: https://doi.org/10.20944/preprints202409.2085.v1

8. **A. Sheikhan** and E. M. S. Narayanan, “Characteristics of a 1200 V Hybrid Power Switch Comprising a Si IGBT and a SiC MOSFET,” Micromachines, vol. 15, no. 11, p. 1337, 2024. DOI: https://doi.org/10.3390/mi15111337

9. **A. Sheikhan**, E. M. S. Narayanan, H. Kawai, S. Yagi and H. Narui, “Evaluation of a 1200 V Polarisation Super Junction Cascode GaN Field-Effect Transistor,” Electronics, vol. 14, no. 3, p. 624, 2025. DOI: https://doi.org/10.3390/electronics14030624

10. **A. Sheikhan** and E. M. S. Narayanan, “Evaluation of a 650 V Hybrid Power Switch Combining GaN Si SiC Technologies,” in International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM), Nuremberg, 2025. DOI: https://doi.org/10.30420/566541022

11. **A. Sheikhan** and E. M. S. Narayanan, “Performance of 1.2 kV Field Stop Trench Clustered IGBTs in Hybrid Power Switch Configuration,” in 17th International Seminar on Power Semiconductors (ISPS), Prague, 2025. (Accepted for publication)

12. **A. Sheikhan**, E. M. S. Narayanan, H. Kawai, S. Yagi and H. Narui, “1.2 kV Hybrid Power Switch Consisting of a PSJ GaN HEMT, a Si IGBT and a SiC Diode,” in Solid State Devices and Materials (SSDM), Yokohama, 2025. (Accepted for publication)

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List of Abbreviations

Abbreviation	Definition
2D	Two Dimensional
2DEG	Two Dimensional Electron Gas
2DHG	Two Dimensional Hole Gas
AC	Alternating Current
Al	Aluminium
Al_2O_3	Aluminium Oxide - Sapphire
AlGaN	Aluminium Gallium Nitride
BJT	Bipolar Junction Transistor
BPS	Bidirectional Power Switch
CCM	Continuous Current Mode
CIGBT	Clustered IGBT
D-Mode	Depletion Mode
DA	Dynamic Avalanche
DBC	Direct Bond Copper
DC	Direct Current
DCM	Discontinuous Current Mode
DCR	Direct Current Resistance
DUT	Device Under Test
E-Mode	Enhancement Mode
EOL	End of Life
ESR	Equivalent Series Resistance
EST	Emitter Switched Thyristor

EV	Electric Vehicle
F	Fluorine
FET	Field Effect Transistor
FS-IGBT	Field Stop IGBT
Ga	Gallium
GaAs	Gallium Arsenide
GaN	Gallium Nitride
Ge	Germanium
GFP	Gate Field Plate
GIT	Gate Injection Transistor
GTO	Gate Turn-Off Thyristor
HEMT	High Electron Mobility Transistor
HFET	Heterostructure FET
HPS	Hybrid Power Switch
HVDC	High Voltage Direct Current
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
JFET	Junction FET
LED	Light Emitting Diode
LSI	Large Scale Integration
MBE	Molecular-Beam Epitaxy
MCT	MOS controlled Thyristor
Mg	Magnesium
MOCVD	Metal-Organic Chemical Vapour Deposition
MOSFET	Metal Oxide Semiconductor FET
MPS	Merged PiN Schottky

N	Nitrogen
NTC	Negative Temperature Coefficient
PSJ	Polarisation Super Junction
PTC	Positive Temperature Coefficient
PWM	Pulse Width Modulation
RB-IGBT	Reverse Blocking IGBT
RC-IGBT	Reverse Conducting IGBT
RF	Radio Frequency
RT	Room Temperature
SFP	Source Field Plate
Si	Silicon
Si_3N_4	Silicon Nitride
SiC	Silicon Carbide
SJ	Super Junction
SMPS	Switched Mode Power Supplies
SOA	Safe Operating Area
TEG	Test Element Group
UIS	Unclamped Inductive Switching
UVLO	Under-Voltage Lockout
ZTC	Zero Temperature Coefficient
ZVS	Zero Voltage Switching

Chapter 1

Introduction

1.1 General Background

Power semiconductor devices have revolutionised engineering and technology, driving innovations in power electronics in a range of industries including automotive, consumer appliances, energy distribution, marine, and aerospace electronics. Bipolar junction transistors (BJTs) and thyristors were amongst the first power semiconductor devices invented in the 1950s. Soon after their initial introduction, solid state devices had quickly replaced power hungry and bulky vacuum tubes due to the many advantages they offer. Despite their growth to higher current and voltage capabilities, these devices suffered from cumbersome control circuits. Since then, silicon has served as the base material for the majority of semiconductor components.

The emergence of MOS technology for digital electronics was another milestone which then made its way through power devices. The power MOSFET was commercialised in 1970 by International Rectifier which is now part of Infineon technology followed by several other companies. MOSFETs offer high input impedance which means that the gate drive requirements are significantly reduced and simpler compared to their BJT predecessors. While

their switching time is extremely fast owing to the absence of bipolar carriers, the on-state resistance of FETs increases rapidly as breakdown voltage increases [1]. This problem was partially resolved by the employment of superjunction (SJ) technology which has enabled low loss power MOSFET designs up to 900 V [2].

In 1979, MOS and bipolar technologies were combined to create a highly successful, insulated gate bipolar transistor (IGBT) [3] that rapidly established its success in the medium to high power application market including industrial motor drives, automotive, etc. Their success can be attributed to high input impedance, low conduction losses due to huge power gain, moderately fast switching transitions and a wide safe operating area (SOA).

As the demand for greater efficiency and higher power densities continues to rise, new wide bandgap materials have become the focus of extensive research in recent times. Amongst these candidates, gallium nitride (GaN) and silicon carbide (SiC) are the two frontrunners for the replacement of Si. SiC devices have the capability to withstand high voltages and currents and can be fabricated using a similar technology to conventional silicon devices. Nevertheless, the cost associated with epitaxial growth of SiC crystals has been a major concern regarding the acceptance of the technology. On the other hand, GaN devices utilise completely different technology that is based on the polarisation properties of the material. GaN can offer potential cost savings because of the ability to fabricate thin layers of GaN on cheap and widely available substrates including silicon and sapphire.

In this thesis, the aims and objectives are divided into two folds; First, an evaluation of the performance of high voltage GaN power diodes and transistors is conducted to gain an in-depth knowledge of how the technology can be used to contribute to the development of higher power density power electronics. Also presented are the limitations and challenges hindering the

progress towards higher power density operation. The second part of this thesis is aimed at high voltage SiC unipolar and Si bipolar devices for high power applications. Hybrid configurations of these technologies are investigated in order to optimise the performance gain under partial and full load conditions without significant addition to costs.

1.2 Trend in Power Electronics

The development trend in power electronic converters and systems is driven by the growing demand for higher efficiency, higher power density, higher reliability, and higher sustainability without compromising the cost-performance [4] [5] which are illustrated in Fig. 1-1.

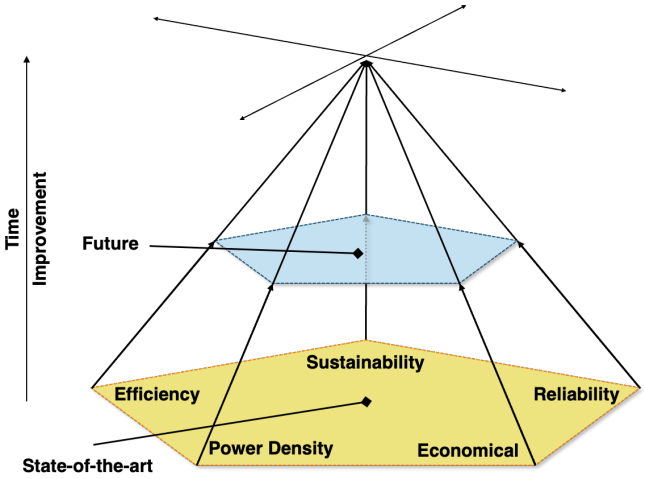


Fig. 1-1. General development trend in power electronic systems.

High power density and efficiency are amongst the key development factors in power electronic applications especially in mobile applications where space and energy are limited such as in automotive, information technology, and satellite industries. In such applications, more compact design contributes to a reduction in capital cost of infrastructure and also permits more flexible design [4]. Smaller size and lower weight converters can simplify installation and maintenance. The power density of converters has increased by a factor of two every decade since 1970 which coincides with the introduction of the power MOSFET [5]. This is

primarily attributed to the increased frequency domain of power semiconductor devices, which has enabled higher switching speeds [6]. However, passive components, packaging, and cooling systems are imposing a significant barrier on this trend [5]. To overcome these barriers, ultra-low loss, high speed power semiconductors are a necessity [6]. The ability of power semiconductor devices to switch at higher speeds is limited by the technological capabilities and inherent characteristics of the material used which is illustrated in Fig. 1-2.

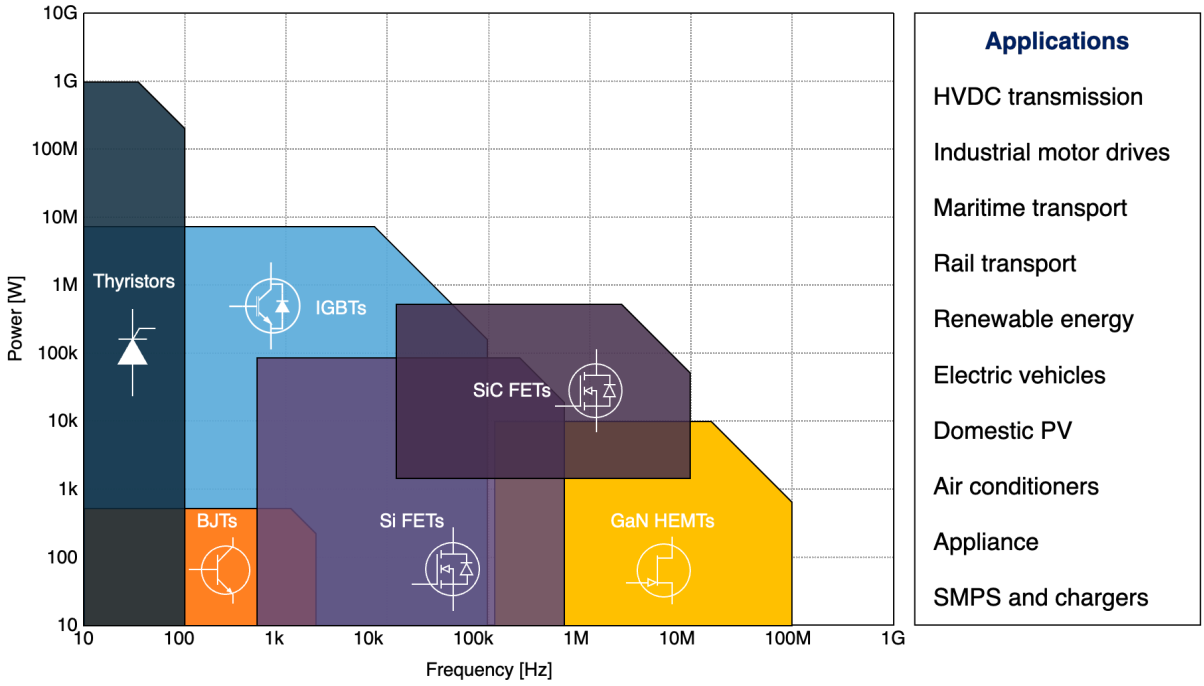


Fig. 1-2. Applications of major controllable power semiconductor devices in relation to operating power and frequency.

Thyristor type devices can handle large amounts of current and are typically employed in applications handling high-power at low-frequency such as in high voltage direct current (HVDC) transmission lines and smart grids. In medium power applications at voltage levels exceeding 900 V, such as electrical machines and drives and electric vehicles (EVs), IGBTs are the preferred choice because of their bipolar current carrying capability which permits for low on-state losses. Si unipolar devices like power MOSFETs are capable of operating at higher

frequencies; however, their ability to handle large power is limited by the on-state resistance. Due to unipolar current flow, these devices switch at much higher speeds achieving higher efficiency [7] [8]. Meanwhile, unipolar devices based on SiC offer superior on-resistance for a given device area because of the high critical electric field tolerance and wide bandgap. However, their performance to cost ratio is hindered by the material processing factors which add to their overall cost. High frequency GaN HEMTs have gained significant market acceptance particularly in power conversion systems due to their inherent material merits. To improve the performance in power devices, a number of techniques are used such as optimisation of charge distribution in the active layers, LSI microfabrication technology, and introduction of large area wafers [9].

1.3 Evolution of Silicon Transistors

Silicon technology has formed the foundation for the majority of electron devices currently available. However, the development of Si devices is approaching the one-dimensional material limit. Small improvements in performance result in significant fabrication and development costs. This occurs because the on-resistance increases substantially with the blocking voltage in unipolar devices. In order to withstand high voltages, a wider drift region with a light doping profile is necessary which significantly adds to the resistance. The resistance of power semiconductor devices is composed of several elements associated with each layer in the current flow path. The contribution of each element to the on-state resistance in power MOSFETs for different voltage classes is shown in Fig. 1-3.

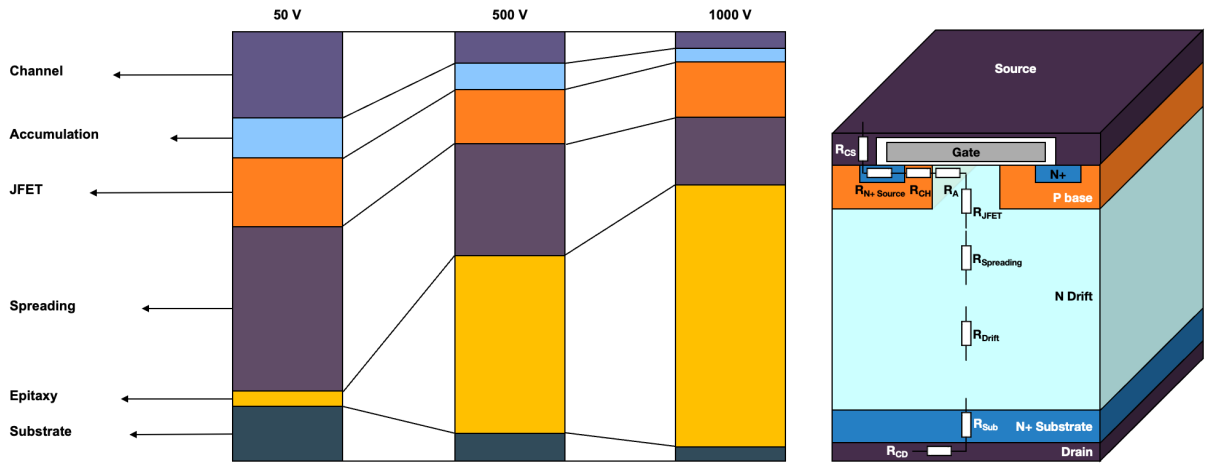


Fig. 1-3. Relative contributions of the on-state resistance components in a planar gate power MOSFET [10] and cross-sectional view of the device highlighting the integral resistances.

Source resistance: Electrons entering the device from the source electrode flow in the N+ source regions before entering the channel. The length and sheet resistance of the source region determine its resistance.

Channel resistance: The channel is responsible for controlling the current flow. Several factors affect the channel resistance including channel length, carrier mobility, applied gate bias, gate threshold and oxide layer thickness. The channel resistance is mostly important in low voltage devices where its contribution is noticeable.

Accumulation layer resistance: The current after leaving the channel enters the accumulation region beneath the gate before entering the bulk. When a positive gate voltage is present, electrons accumulate in this region reducing the resistance.

JFET resistance: After passing the accumulation layer, the incoming electrons flow vertically via the JFET region before entering the drift layer. Although the contribution to the resistance associated with the JFET region can be mitigated by extending the width of the gate, the

accumulation and channel resistances are adversely impacted. The JFET region can be removed in MOSFETs employing trench gate configuration.

Spreading resistance: After leaving the JFET region, electrons can spread in the bulk and flow under the MOS cells.

Epitaxial layer resistance: The doping profile and the length of the drift layer are governed by the required blocking voltage rating. For high voltage devices, a large drift region with light doping is required to support the rated voltage which accounts for the largest contribution to overall on-state resistance.

Substrate resistance: Eventually, the charge carriers reach the end of the drift layer where they are subsequently distributed rapidly within the heavily doped N+ substrate.

Bond wires, leads resistance: The contact resistance is made up of drain and source metallisation which is determined by the type and contact area. In a packaged device, the bond wires and leads contribute to on-resistance by a few micro-ohms to milli-ohms.

The total on-resistance is therefore given by the sum of its constituting elements as given by Eq. (1-1).

$$R_{\mathrm{DS.ON}} = R_{\mathrm{Source}} + R_{\mathrm{Ch}} + R_{\mathrm{A}} + R_{\mathrm{JFET}} + R_{\mathrm{Spr}} + R_{\mathrm{Epi}} + R_{\mathrm{Sub}} + R_{\mathrm{Contact}} \qquad (1\text{-}1)$$

The power MOSFET was first commercialised using a planar gate (D-MOSFET) structure that is depicted in Fig. 1-4. The parasitic JFET region resistance, as previously discussed, has been a major contributor to the on-state resistance.

Further development to minimise the on-state resistance resulted in the introduction of the trench gate (U-MOSFET) structure that leads to the elimination of the JFET region and carrier

spreading allowing a higher channel density [1]. One of the drawbacks of the trench gate approach is the additional input capacitance (C_{GS}) which leads to slower switching. Despite this, trench gate devices gained popularity due to overall performance gain compared to planar gate MOSFETs.

The quest for further reduction of on-state resistance has led to major breakthroughs in power MOSFET performance. In 1990, based on the 2D charge coupling concept, a new architecture known as split gate (GD-MOSFET) using deep source electrodes was introduced [11]. The concept has become popular for blocking voltage of up to 150 V, mainly targeting power supply applications in the computer industry.

The most recent advancement which paved the way for low resistance devices is the concept of superjunction which was introduced in 1999 [2] [12] [13]. Superjunction devices utilise stripes of precisely doped P-type pillars implemented in the N-type drift region to realise a charge balance condition that leads to a box-like electric field profile. The technology has become popular for 600 V to 900 V class devices. However, to realise higher voltage devices, deeper and longer P-type and N-type pillars are required which adds to the processing complexity and costs [14].

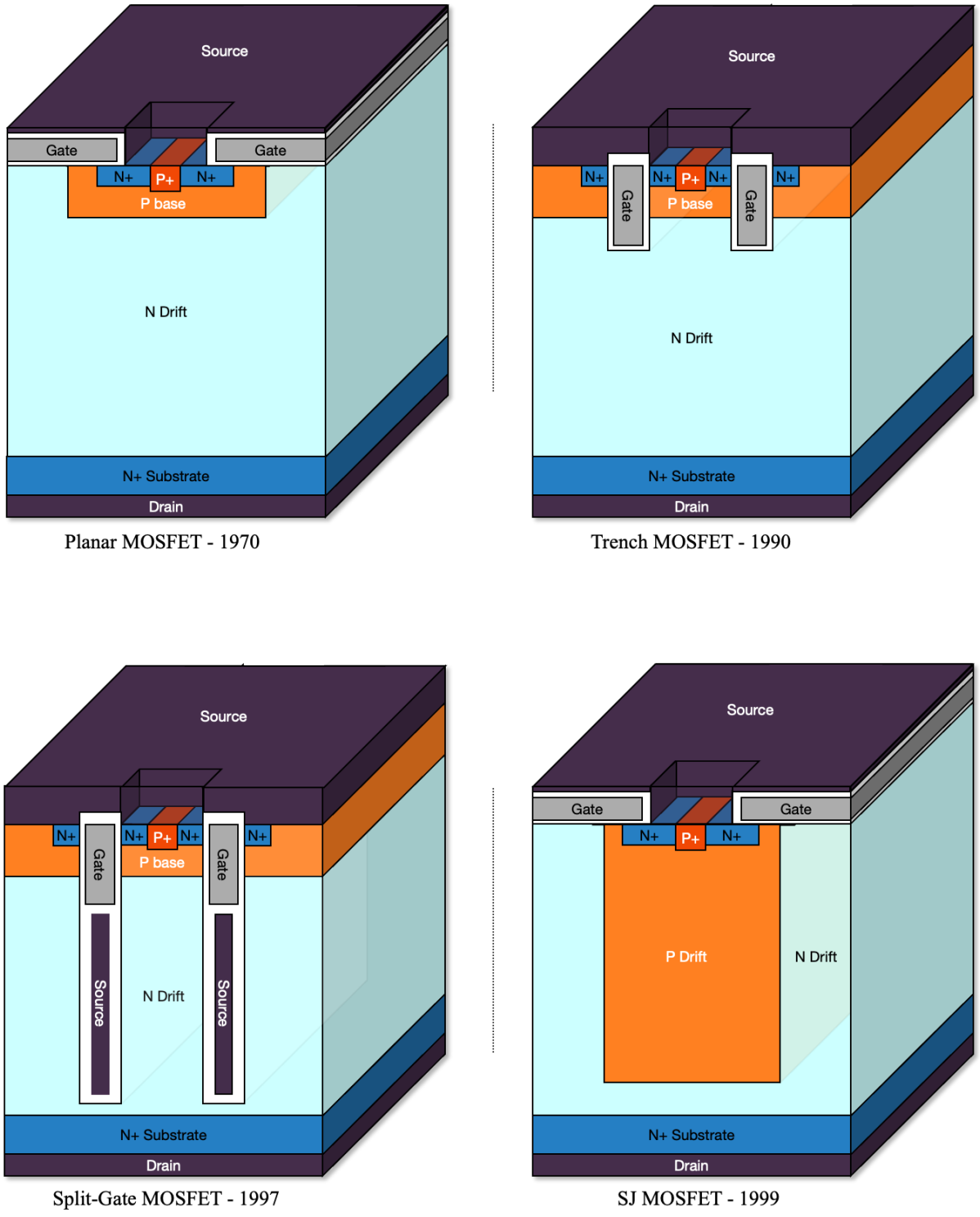


Fig. 1-4. Evolution of power MOSFET technology.

Bipolar devices including power IGBTs and thyristors can overcome the on-state resistance barrier of unipolar devices. IGBTs utilise conductivity modulation schemes to lower the resistance contribution of the N-drift region enabling devices that have the capability to operate beyond the one-dimensional material limit. IGBTs are primarily implemented for high voltage devices of above 650 V. This is because the voltage drop due to the inherent built-in potential corresponding to the anode P-N junction results in a diode-like on-state behaviour that limits their low current capability. The development of IGBTs has been devoted to minimising the on-state losses and improving the switching speed efficiency. However, despite significant improvements in switching speed, bipolar devices exhibit switching speed that is an order of magnitude slower than that of unipolar FETs. Furthermore, high speed operation of IGBTs is limited by dynamic avalanche (DA) which can pose reliability risks [15].

Another approach to go beyond the one-dimensional limitation of Si is to replace it with materials that have a wide bandgap, such as SiC or GaN. On account of the superior material properties including higher critical electric field and wider bandgap, these materials can withstand higher blocking voltages with thinner drift region lengths. Consequently, a substantial reduction in specific on-resistance can be made. Fig. 1-5 shows the one-dimensional material limits of GaN, SiC, and Si.

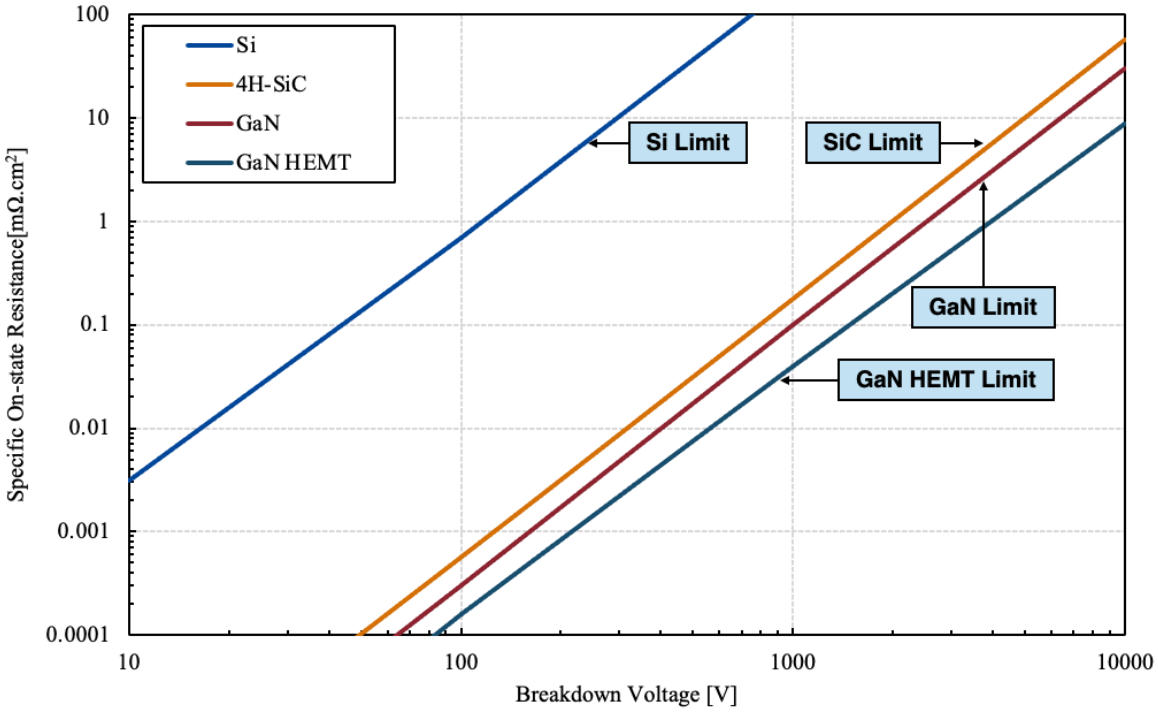


Fig. 1-5. Comparison of the specific on-resistance of GaN, SiC, and Si. Adapted from [16].

GaN HEMTs utilising polarisation have higher mobility than doped GaN where the mobility is limited due to impurity scattering. Therefore, GaN HEMTs show superior performance in terms of specific on-resistance.

1.4 Wide Bandgap Semiconductor Devices

As previously mentioned, materials exhibiting a wide bandgap such as GaN and SiC, offer outstanding material merits compared to Si. Table 1-1 lists a comparative summary of the key physical properties across various semiconducting materials.

Table 1-1. Physical properties of different materials for power semiconductor devices.

Properties / Materials	Si	GaAs	4H-SiC	GaN	Diamond
Energy Band Gap [eV]	1.11	1.42	3.26	3.45	5.47
Critical Electric Field [$MV.cm^{-1}$]	0.3	0.4	3	3.5	5.6
Thermal Conductivity [$W.\ cm^{-1}.\ K^{-1}$]	1.6	0.46	4.9	2.3	20
Saturated Electron Velocity [$10^6.cm.sec^{-1}$]	10	12	22	25	27
Electron Mobility [$cm^2.V^{-1}.sec^{-1}$]	1450	8500	900	2000	1800

The material properties of SiC are favourable over Si for high voltage devices because of a wider bandgap and improved critical electric field strength. The first 4H-SiC MOSFET with a 1200 V rating was first commercialised by CREE in 2011. A key advantage of SiC is its similarity to the well-established Si MOSFET technology in terms of structure and packaging.

The drive for GaN material research is attributed to the successful development of the first GaN based light emitting diode (LED) emitting blue colour by Nakamura [17] and Maruska [18]. GaN, due to its superior material properties, is promising for power dense power electronic applications. This is because GaN epitaxial layers with exceptional quality can be grown over cheaply available, large diameter Si (300 mm) and sapphire as well as SiC substrates. The first lateral GaN HEMT fabricated on sapphire was introduced in 1993 [19] and the first GaN homojunction diode was reported in 1989 [20]. Because of the lateral nature of GaN devices, multiple power transistors, logic and control circuits can be fabricated on the same chip which can improve the power density. One of the challenges in GaN devices is that

they typically exhibit normally-on behaviour. Various methods have been researched to improve the characteristics of GaN HEMTs and achieve normally-off operation as shown in Fig. 1-6. However, many of these attempts come at the expense of additional resistance and lower reliability. One of the recent innovations in GaN device technology was the implementation of the superjunction concept based on the polarisation effect which is known as PSJ. This new concept enables GaN devices to support higher blocking voltage expanding to 10 kV and beyond because of the even distribution of electric field.

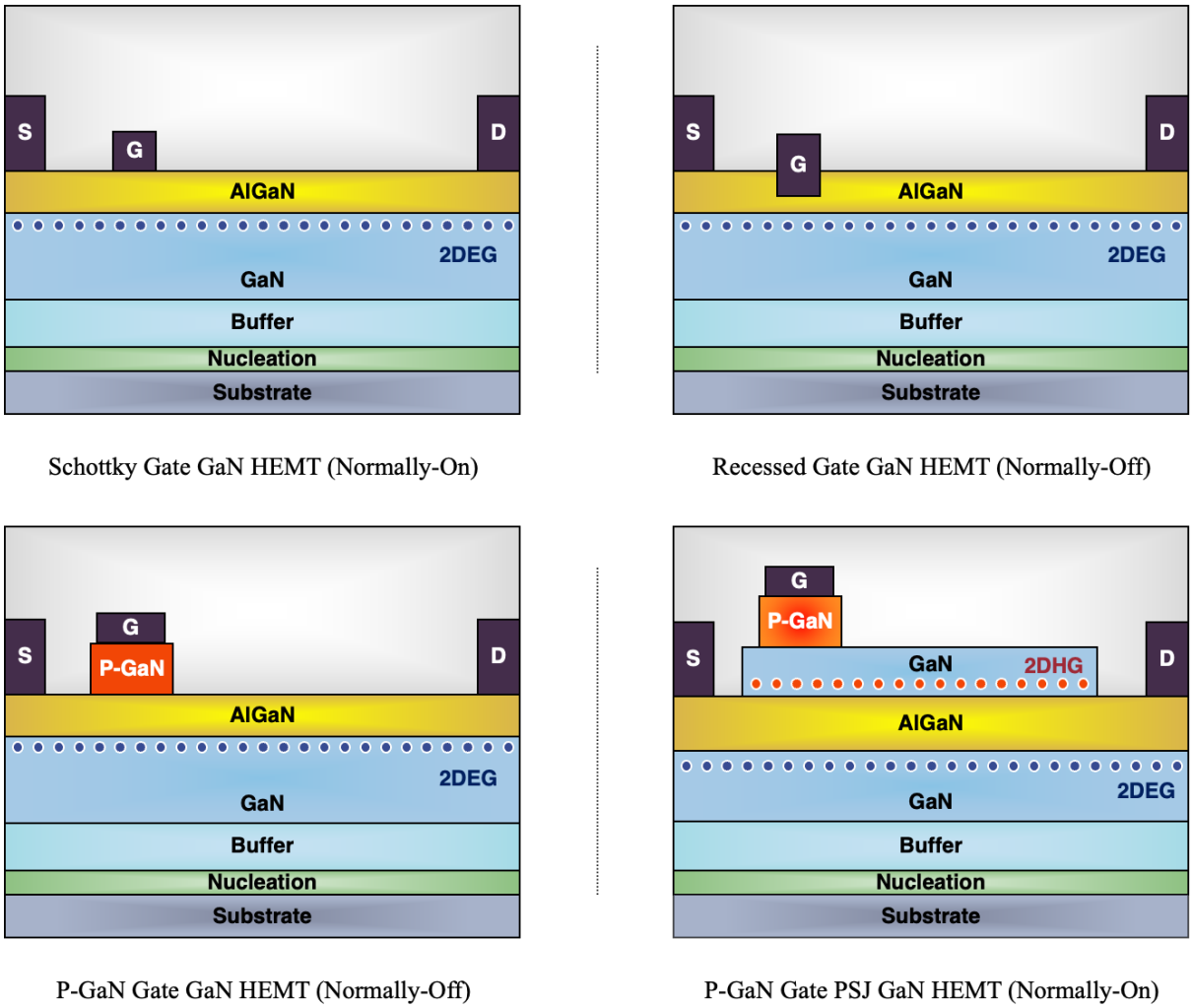


Fig. 1-6. Development trend of lateral GaN HEMTs.

Another way to realise normally-off operation is to implement a cascode structure which works by the addition of a low voltage Si MOSFET configured in series with a high voltage GaN HEMT. Other topologies such as direct drive are also considered which provides a fail-safe mode of operation in case of fault. The operating physics of cascode and direct drive will be further discussed in Chapter 5. Currently, GaN devices are facing huge competition with SiC devices due to overlapping applications. However, the costs associated with GaN are predicted to be lower than SiC in the long term.

1.5 Structure of this Thesis

This thesis is organised as follows based on the given background introduced above.

Chapter 2 In this chapter, the physics and working mechanism of lateral gallium nitride device technology will be discussed in detail. The challenges associated with the fabrication of high voltage devices and ways to mitigate them will be presented. The concept of polarisation superjunction will also be introduced.

Chapter 3 The characteristics and surge current capability of PSJ GaN diodes will be studied extensively and the results are compared with the latest SiC MPS diodes of equivalent ratings. The reverse recovery characteristics will be measured experimentally. It will be concluded that lateral GaN diodes based on the PSJ technology can provide an effective low-cost alternative solution for high voltage diodes without compromising the performance.

Chapter 4 The performance of PSJ GaN HEMTs will be evaluated through experimental measurements of static and dynamic characteristics. The controllability will be investigated,

and the switching losses will be analysed. It will be shown that the PSJ technology enables the fabrication of high performance and high voltage GaN HEMTs.

Chapter 5 This chapter discusses the fundamentals of normally-off GaN HEMTs using cascode and direct drive configurations. A 1200 V cascode PSJ GaN FET is made, and its performance will be studied for the first time. Based on the measured characteristics, associated power loss contributions in a converter application will also be presented.

Chapter 6 The concept, physics of operation, and switching characteristics of hybrid power switches (HPS) will be discussed in detail. Although the concept of HPS has existed for some time, this chapter provides detailed characteristics on device performance under different conditions and methods for improvements. The impact of intelligent gate drive on device performance will be evaluated. The advantages of dual gate design are empirically confirmed. The short-circuit capability of the HPS at elevated temperatures is demonstrated experimentally. The HPS is shown to exhibit superior cost-to-performance characteristics compared to standalone devices. With an intelligent gate drive, the HPS virtually has low power losses as its integral MOSFET.

Chapter 7 In this chapter, a new hybrid power switch based on the state-of-the-art field stop (FS) trench clustered IGBT (CIGBT) and the latest SiC MOSFET technology will be presented. The design, operating principle, and characteristics of 1200 V trench CIGBTs will be discussed and analysed. It will be shown that the CIGBTs can effectively operate at higher current densities compared to conventional IGBTs and therefore are suitable for integration in HPS.

Chapter 8 A HPS consisting of a GaN FET, Si IGBT, SiC Schottky diode will be demonstrated for the first time. The device is assessed experimentally through measurement of characteristics. It will be demonstrated by utilising the superior characteristics of GaN technology, significant performance gain can be achieved.

Chapter 9 Conclusion of this work will be given.

Chapter 2

Physics of Gallium Nitride Device Technology

GaN offers unique material properties which are promising for high power density, high efficiency next generation power semiconductor devices. GaN has attracted vast interest in recent years due to the broad range of applications which it covers [21]. One of the major applications of GaN is its role in the development of white LEDs which have replaced traditional incandescent and fluorescent lights leading to substantial cost and energy savings. Because of the ability to fabricate high quality GaN devices on low-cost foreign substrates, GaN is now expanding towards power conversion applications. In this chapter, the physical properties and operating physics of high voltage GaN devices will be presented. Various device structures and approaches for high operating voltage will also be discussed. The challenges hindering widespread progress of GaN into power applications will be addressed.

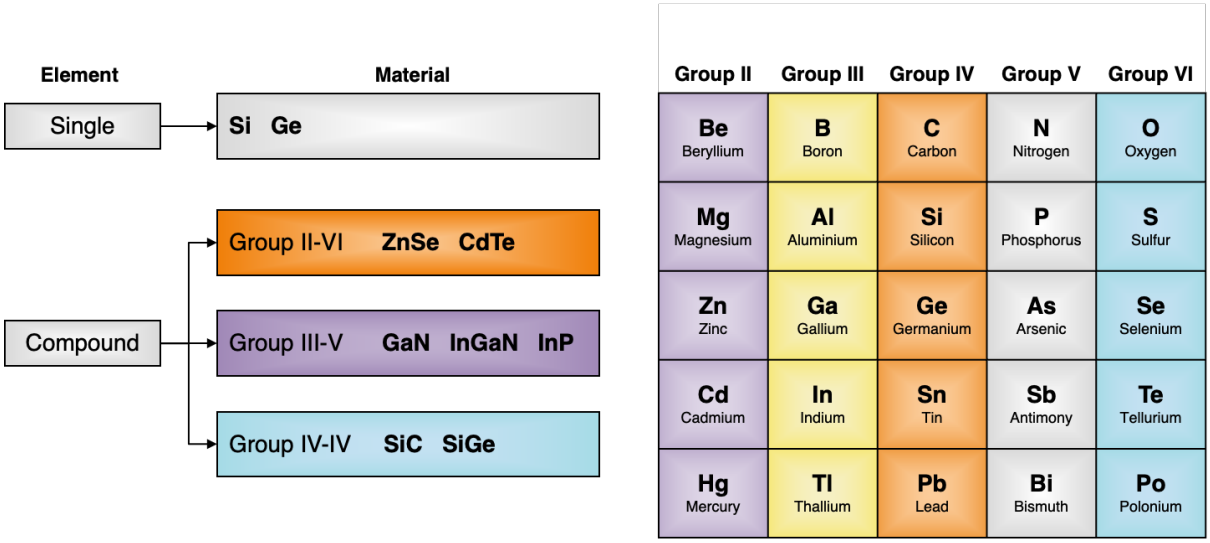


Fig. 2-1. Group II-IV semiconductor materials.

2.1 Origin of Electrical Charges in GaN Devices

In pure crystal form, intrinsic semiconductors such as Si are close to insulators. Adding impurities (dopants) to semiconductors results in a change in their electrical characteristics and a reduction in resistance. Based on the type of dopant that is used, P-type and N-type semiconductors can be realised where holes and electrons are majority carriers respectively. The primary dopant for P-type GaN is magnesium (Mg), while Si is used for N-type GaN. Semiconductor devices can be made of a single element such as Si or Ge or several elements (known as compounds) such as those in group II-VI as shown in Fig. 2-1.

The crystal structure has a key impact on the determination of material properties and device performance. There are three different crystal structures that exist for GaN that include: wurtzite, zinc blend, and rock salt [22] [23]. GaN, under normal ambient conditions, forms a wurtzite crystal structure [24] which is illustrated in Fig. 2-2.

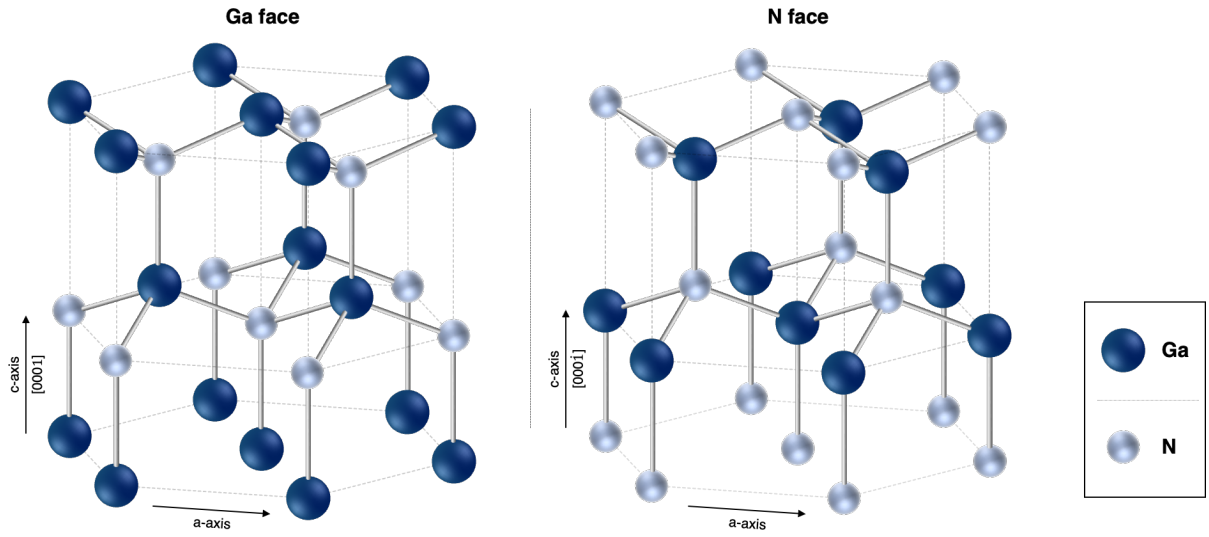


Fig. 2-2. Hexagonal wurtzite crystal structure of gallium nitride.

Each Ga atom is surrounded by four equidistant N atoms in a tetrahedral arrangement and vice versa. The Ga face is typically grown on c-plane sapphire using a metal organic chemical vapour deposition (MOCVD) reactor while the N face is achieved under controlled conditions by molecular beam epitaxy (MBE) [25]. Because of the higher electronegativity of nitrogen compared to gallium, Ga and N have cationic and anionic properties which leads to electrical charge polarisation [26]. While the net charge inside the material is neutral, polarisation charges arise from asymmetrical cuts along the c-axis which lead to spontaneous polarisation. Meanwhile, mechanical stress arising from the variation in lattice constant between epitaxial layers gives rise to another type of polarisation charges known as piezoelectric polarisation. The total polarisation (P_{Total}) in an AlGaN or GaN layer corresponds to the sum of spontaneous polarisation (P_{SP}) and piezoelectric polarisation (P_{PE}) in the absence of an external electric field [27]. The magnitude of the polarisation induced charge density at the heterointerface depends on factors such as alloy composition (x) and tensile stress [28]. Therefore, in a heterojunction based on III-V compounds, free charge carriers are generated at heterointerfaces to counter and neutralise the polarisation charges leading to the formation of two-dimensional electron gas

(2DEG) and two-dimensional hole gas (2DHG). Due to the absence of impurities, polarisation based charges have higher mobility compared to charge carriers arising from doping the material. The formation of polarisation based charges at the heterointerface with high mobility and high conductivity enables the design of low resistance high electron mobility transistors (HEMTs).

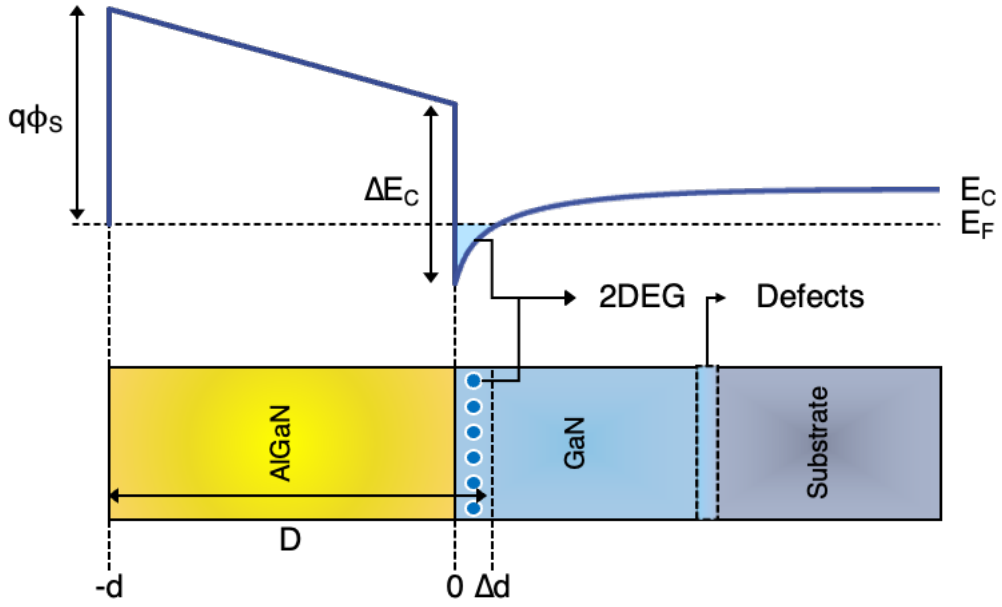


Fig. 2-3. Basic AlGaN/GaN heterostructure and the corresponding energy band diagram. Adapted from [29].

Fig. 2-3 shows the basic cross-section of an AlGaN/GaN heterostructure and its band diagram. Due to the lattice mismatch between the substrate and GaN layers, a highly defective region is formed in between. The charge density (N_S) of the 2DEG is determined by Eq. (2-1) [29].

$$N_S = \frac{Q_\pi . d_{AlGaN} - \varepsilon_S . \left(\phi_S - {\Delta E_C}/{q}\right)}{qD} \qquad (2\text{-}1)$$

where Q_π is the net polarisation charge induced, d_{AlGaN} corresponds to the AlGaN barrier thickness, ϕ_S denotes Schottky barrier height, and ΔE_C is the offset difference between conduction bands of AlGaN/GaN, D is the depth of 2DEG, and q is the charge of an electron.

2.2 AlGaN-GaN HEMTs

GaN has become a key material in the semiconductor industry because of the wide spectrum of applications it covers. The majority of power GaN devices currently available are based on lateral AlGaN/GaN topologies. Vertical topologies remain in the research and development phase because of the challenges hindering their large-scale fabrication and more importantly because of the higher costs pertaining to substrate material [29] [30]. The key distinction of GaN HEMTs is that they can utilise the high density and mobility of 2DEG and 2DHG arising from the polarisation properties of the material for low resistance, high voltage devices. The first GaN HEMTs fabricated on sapphire were introduced in 1993 [19] and the first p-n junction in 1989 [20]. Due to the presence of an uninterrupted channel formed by the 2DEG between drain and source, the current can flow at zero gate bias and therefore GaN HEMTs demonstrate normally-on (depletion mode) operation that is characterised by a negative threshold voltage ($V_{GS\text{-}TH}$) which is undesirable in several applications.

2.2.1 Threshold voltage

Power transistors demonstrating a positive threshold are preferred to guarantee system safety in case of a fault such as losing the gate drive circuit. A positive threshold results in the device failing in an open state and therefore the current can be interrupted. Otherwise, a short circuit can result in catastrophic current flow and destruction. The threshold voltage (V_{TH}) of GaN HEMTs can be described as follows (Eq. (2-2)) [26].

$$V_{\mathrm{th}} = \emptyset_{\mathrm{S}} - \Delta E_{\mathrm{c}} - V_{\mathrm{AlGaN}} = \emptyset_{\mathrm{S}} - \Delta E_{\mathrm{c}} - \frac{qN_{\mathrm{s}}d_{\mathrm{AlGaN}}}{\varepsilon_0 \varepsilon_{\mathrm{AlGaN}}} \qquad (2\text{-}2)$$

where $\varepsilon_{\mathrm{AlGaN}}$ represents the AlGaN relative dielectric constant. The equation indicates that the threshold voltage depends on the following parameters:

(1) AlGaN barrier thickness.

(2) Al to GaN ratio in AlGaN (mole fraction).

(3) Work function of the gate contact material.

By manipulating the above parameters, a positive threshold can be obtained leading to the enhancement mode of operation. Using a recessed gate structure (Fig. 1-6), the AlGaN barrier layer thickness underneath the gate is made narrower, which leads to a localised depletion of the 2DEG contributing to a positive threshold voltage. The e-mode operation can also be realised via controlling the work function associated with the gate material by using P-type GaN or AlGaN that can effectively alter the threshold voltage into a positive regime. An example of this method is known as gate injection transistor (GIT) which is based on injection of holes [31]. Another approach is to introduce negatively charged fluorine ions (F-) through plasma treatment which can shift the threshold voltage positively [32]. Such methods, however, result in a compromise in the on-resistance of the device because they remove or reduce 2DEG. Normally-off operation can also be emulated through the use of hybrid configurations of HEMTs in the form of cascode or direct drive which will be discussed further in detail in Chapter 5.

2.2.2 Blocking voltage

Under off-state blocking mode, the 2DEG is depleted enabling the device to withstand high voltages. The maximum blocking voltage capability of GaN HEMTs fabricated on semi-insulating substrates such as Si is limited in two directions. In the lateral direction, the electric field is distributed over the span of the drift region alongside the surface between drain and gate terminals. In an ideal condition, the breakdown takes place when the peak electric field approaches the critical electric field threshold which is 3 $MV.cm^{-1}$. However, as a result of non-uniformity in the electric field within the drift layer, the breakdown occurs at an average electric field of 1 $MV.cm^{-1}$ [29]. The electric field peaks can be suppressed by incorporating field plates attached to the gate (GFP) or attached to the source (SFP) [33]. The use of gate field plates, however, can affect the switching performance because of its contribution to a larger gate-drain capacitance. Although the source field plate is preferred because it does not change the switching characteristics, it is not as effective as the gate field plate in suppressing electric field peaks. Typically, a combination of gate and source field plates is used to fabricate GaN HEMTs [34] [35].

In the vertical direction, an electric field is developed vertically which can result in the breakdown between the drain and the substrate. Research shows that the breakdown voltage rises with the thickness of the epitaxial layer [34]. This matter can be mitigated by the use of insulating substrates such as sapphire.

In GaN HEMTs, the device faces catastrophic breakdown when the peak electric field approaches its critical value. Avalanche energy in GaN HEMTs is dissipated in the form of capacitive stored energy. A capacitive dielectric breakdown occurs when operating close to the breakdown point [29].

2.3 Substrate Material

The selection process of the substrate material is ultimately determined by the device topology, cost, and the intended end application. Historically, GaN devices were developed on foreign substrate materials such as sapphire because of the lack of availability of native GaN substrates. Currently, a diverse range of substrates are available for epitaxial growth of GaN, which are listed in Table 2-1 along with their key parameters.

Table 2-1. Comparison of various substrate materials for GaN epitaxial growth [36] [37].

	GaN	**Si**	**SiC**	**Sapphire**	**Diamond**
Lattice mismatch [%]	0	-17	3.1	16	11.8
Linear thermal expansion coefficient [$x10^{-6}.K^{-1}$]	5.6	2.6	4.4	7.5	4.4
Current cost	Expensive	Cheap	Moderately Expensive	Cheap	Very Expensive
Thermal Conductivity [$W.cm^{-1}.K^{-1}$]	2.3	1.6	4.9	0.25	20

Despite significant progress in manufacturing, native GaN substrates are still in scarcity and very expensive to fabricate [38]. High quality GaN substrates with low threading dislocation have become a focal point in efforts to fabricate vertical power devices [39]. Nevertheless, despite the advantages that GaN substrates provide, commercial viability has hindered the acceptance of the technology.

Si has drawn significant attention because of the abundant supply of large diameter bulk wafers (up to 12 inches) with a very low cost. However, because of the substantial lattice mismatch between the two materials and to prevent vertical breakdown, thick buffers and transitional layers are needed which can result in wafers to crack and bow formation [40]. Substantial optimisation of the process is therefore required to minimise bow levels [41]. Also, because of the semi-insulating nature of Si, the vertical breakdown is influenced by the thickness of the buffer layers [34]. For this reason, insulating substrates are used for high voltage device fabrication.

SiC offers good lattice mismatch difference and excellent thermal conductivity which is desired for transistor applications. However, currently available SiC wafers are limited to 6 inches and are significantly more expensive than Si and sapphire. Various factors such as manufacturing complexity which includes more expensive and complex techniques as well as specialised equipment and lower yield due to challenges in high quality crystals result in higher costs. Hence, SiC is mostly employed for RF purposes where it can be most beneficial.

Sapphire is particularly interesting for high voltage devices because of its inherently insulating properties. While the thermal resistance of the material is noticeably higher, this can be mitigated by using thin substrate material. Other techniques such as flip-chip can be used for cooling the devices as well. Overall, sapphire is favoured for high voltage device fabrication due to its excellent cost-to-performance ratio.

Diamond is an exceptional conductor of heat which is ideal for extreme temperature environments. However, the cost is exceptionally high because of the material's hardness and difficulty in producing synthetic diamond wafers.

2.4 Current Collapse

One of the fundamental issues associated with GaN heterostructures such as HEMTs is the presence of imperfections and defects within the lattice (shown in Fig. 2-4), which affect device dynamic properties.

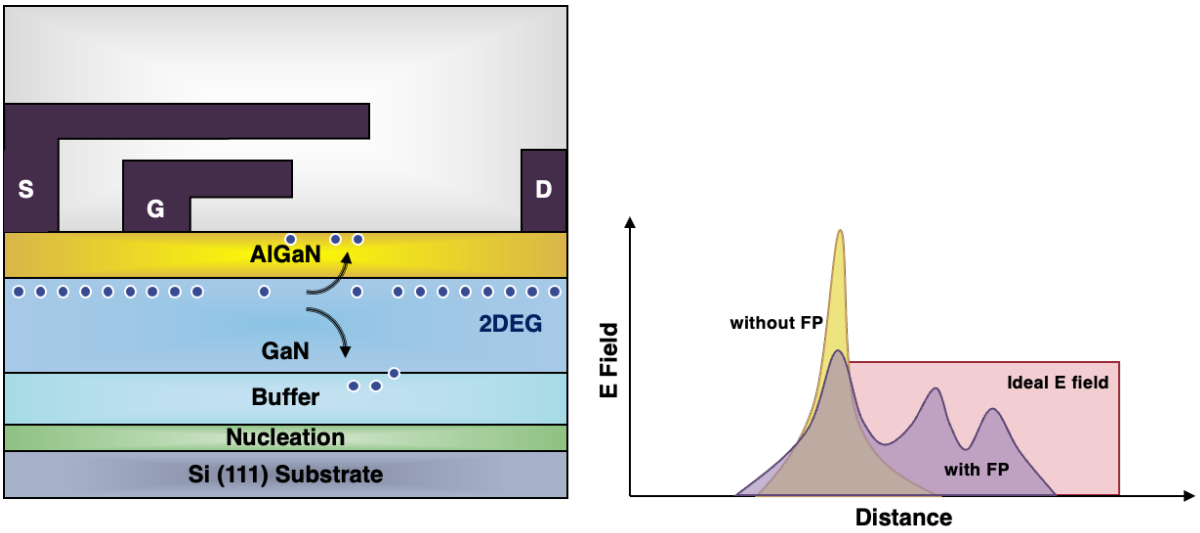


Fig. 2-4. Schematic of an AlGaN/GaN HEMT. Because of the trapped charges, the channel density is affected.

This is particularly visible when high electric field peaks are present under off-state conditions. Parasitic electrons can be captured by these traps which exist in the bulk GaN buffer layer or at epitaxial surfaces which are responsible for the formation of the 2DEG channel. Trapped electrons at the heterojunction surface cause partial depletion of the 2DEG which suppresses mobile carrier concentration leading to current collapse phenomena and dynamic on-state resistance. Fig. 2-5 illustrates the effect of dynamic on-resistance on output I-V characteristics after application of a stress voltage.

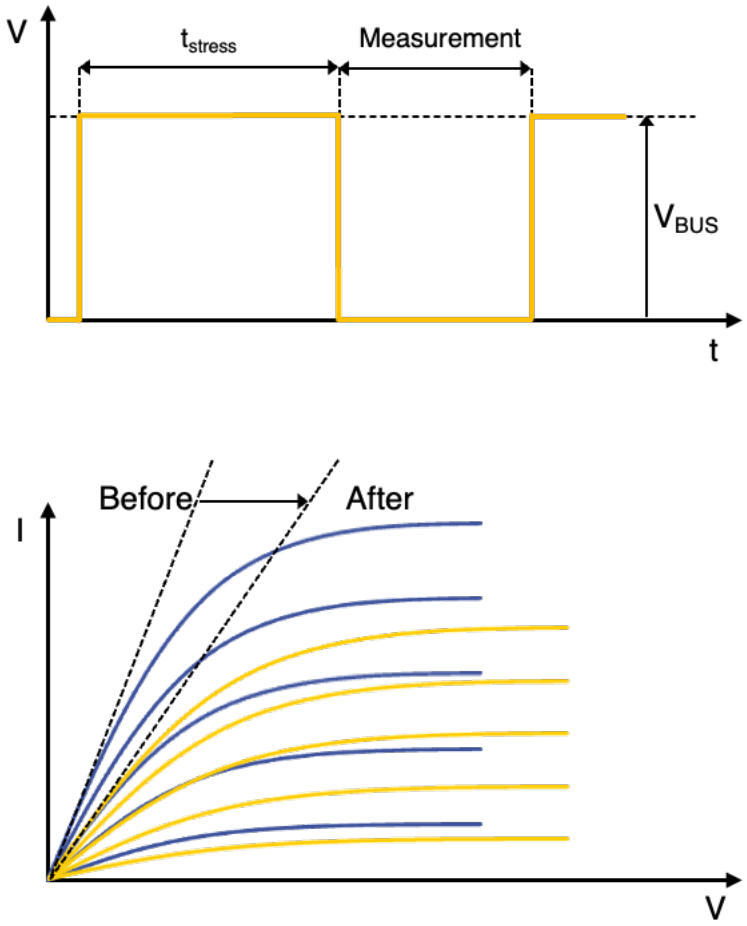


Fig. 2-5. Illustration of degradation in the output characteristics of GaN HEMTs due to current collapse.

This behaviour was first observed in microwave GaN transistors reported in [42]. To mitigate current collapse various techniques are employed such as the utilisation of multiple field plates [43] [44] and surface passivation using silicon nitride (Si_3N_4) [45]. The extent of current collapse strongly depends on the applied electric field uniformity and could be mostly suppressed by the field plate structure which levels the electric field [46]. The silicon nitride passivation method works by preventing electrons from being captured in the surface donor states [47]. The passivation buries the surface traps making them inaccessible [47].

2.5 Super Junction by Polarisation

Engineering electric field is a critical task in power semiconductor devices to meet the required ratings and to have reliable operation. One of the foremost concerns in the development process of high voltage GaN HEMTs is the uneven spreading of electric fields which limits the breakdown voltage and leads to current collapse phenomena. Field plates are commonly used to suppress the electric field and distribute it along the drift region. The implementation of field plate structure adds to the number of fabrication process steps and requires additional time which contributes to higher development costs. Also, electric field peaks remain present near the gate terminal which penalises performance. In conventional Si devices, a superjunction is realised by precise control over the doping of opposite charges in P-type and N-type pillars that are implanted in the drift region [2] [12] [48]. Therefore, an even distribution of electric field can be achieved which has enabled Si MOSFETs to have lower on-resistance beyond the material limit.

A novel device concept known as polarisation superjunction was reported in [49] for GaN HEMTs. The PSJ concept enables the construction of high voltage GaN diodes and transistors that can potentially operate beyond the one-dimensional material limit where the breakdown voltage scales linearly with the length of the drift region. PSJ GaN devices work in a similar manner to conventional superjunction except that the charge balance originates from the polarisation based charges inherent to the material and no impurity doping is involved. Polarisation charges of opposite type but equal charge density can coexist in a double heterostructure formed by GaN/AlGaN/GaN (grown along 0001 crystal axis) to form the superjunction which results in a uniform spreading of electric field [50] [51]. Unlike conventional superjunction, PSJ can be scaled without a significant increase in cost for high voltage devices because of the natural charge balance between opposite polarisation charges

[40]. A basic overview of GaN/AlGaN/GaN PSJ structure and the corresponding band diagram is depicted in Fig. 2-6.

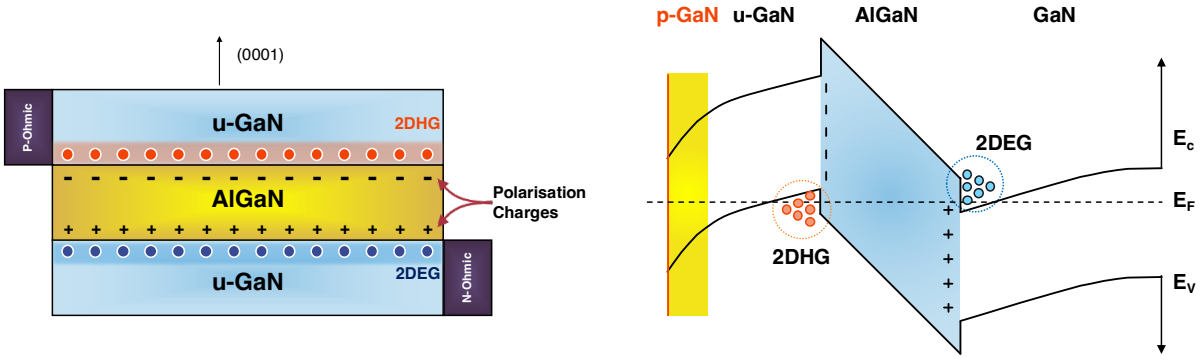


Fig. 2-6. Basic PSJ structure formed by GaN/AlGaN/GaN double heterojunctions and the corresponding energy band diagram. [52]

The 2DHG and 2DEG are confined in GaN/AlGaN/GaN quantum wells [28] and exhibit high mobility because of negligible impurity scattering [50]. Fig. 2-7 shows the measured hole density of 2DHG and Mg doped P-GaN using the Van der Pauw technique [40] [53].

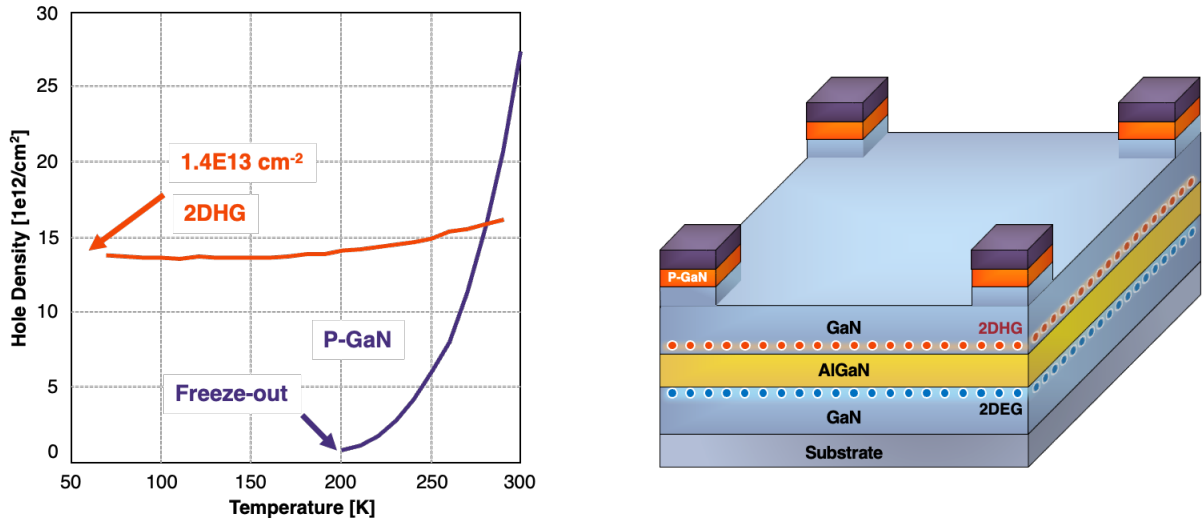


Fig. 2-7. Measured hole density of 2DHG and P-type GaN using the Van der Pauw hall measurement method. [40]

The measurement results indicate that the holes in the PSJ structure are originated from the polarisation and not from the Mg doped P-GaN. Along with high carrier mobility, the density

of polarisation based holes and electrons does not change drastically with temperature whereas the holes that are originated from the Mg doped P-GaN freeze out at 200 K (-73˚C). This indicates the possible potential of PSJ GaN devices for operation at cryogenic temperatures.

The PSJ can be implemented for a broad spectrum of power devices including transistors, diodes, and bidirectional power switches. A cross-sectional view of a GaN HEMT developed based on the PSJ technology is shown in Fig. 2-8.

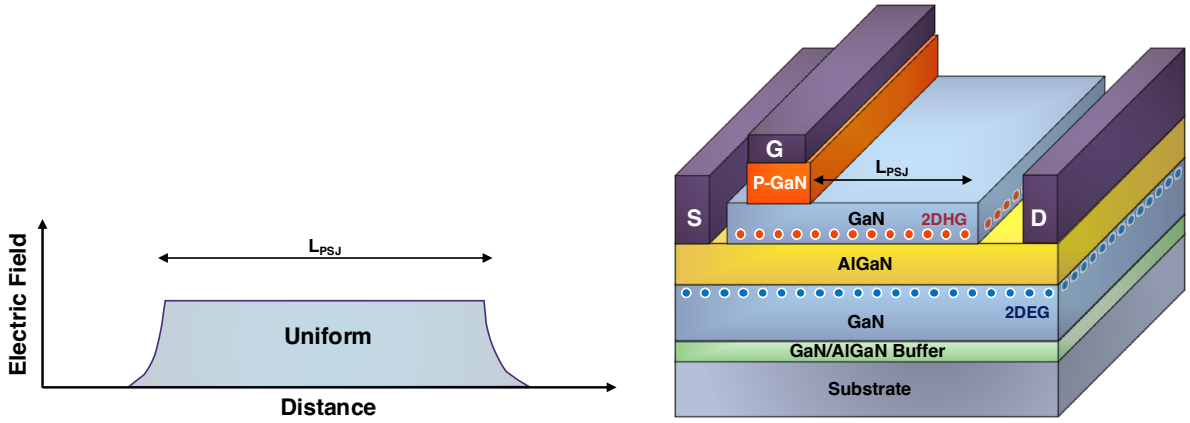


Fig. 2-8. Cross-sectional diagram of PSJ GaN HEMTs and the electric field spreading under blocking-mode conditions.

The on-state operation of PSJ GaN HEMTs is similar to conventional normally-on GaN HEMTs. The current can flow via the high density and mobility 2DEG channel between drain and source in either polarity. Under off-state conditions, at $V_{GS} < V_{TH\text{-}GS}$, the 2DHG and 2DEG are removed via the gate and drain terminals, respectively [40]. As drain voltage increases, all 2DHG and 2DEG are depleted resulting in an intrinsic semiconductor drift region [49]. Due to the charge balance between positive and negative polarisation charges, a flat distribution of the electric field is realised over the span of the drift area. The schematics of the PSJ GaN HEMT under on-state and off-state conditions are shown in Fig. 2-9.

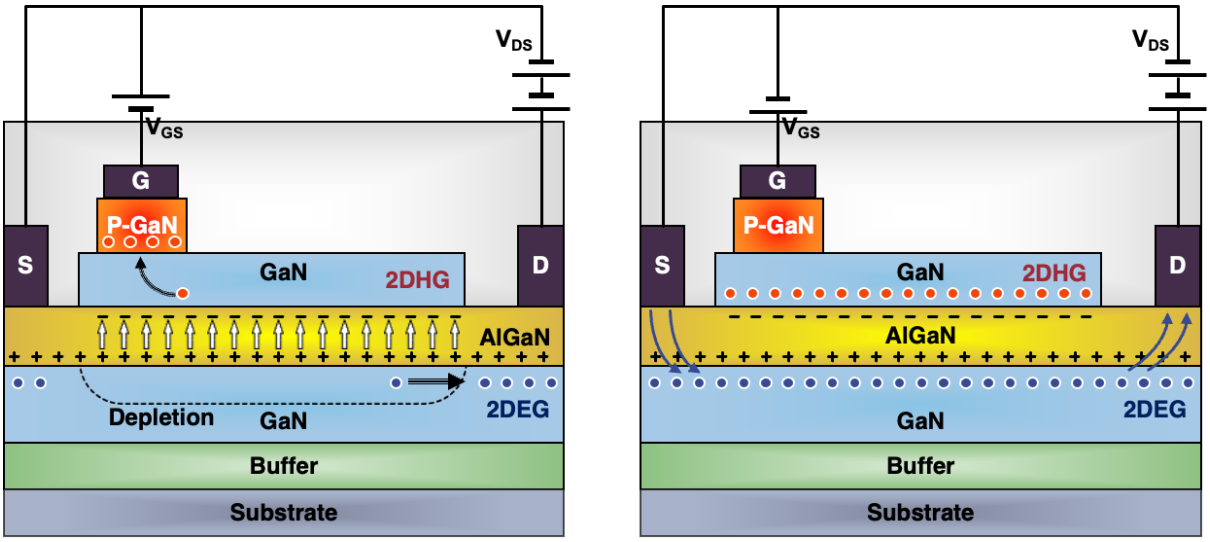


Fig. 2-9. Schematic of PSJ GaN HEMTs illustrating off-state (left) and on-state (right) modes of operation.

Based on the measurement results of various PSJ devices with different drift lengths, the specific on-state resistance versus the maximum supported voltage are plotted in Fig. 2-10 alongside the material limit of GaN, SiC, and Si.

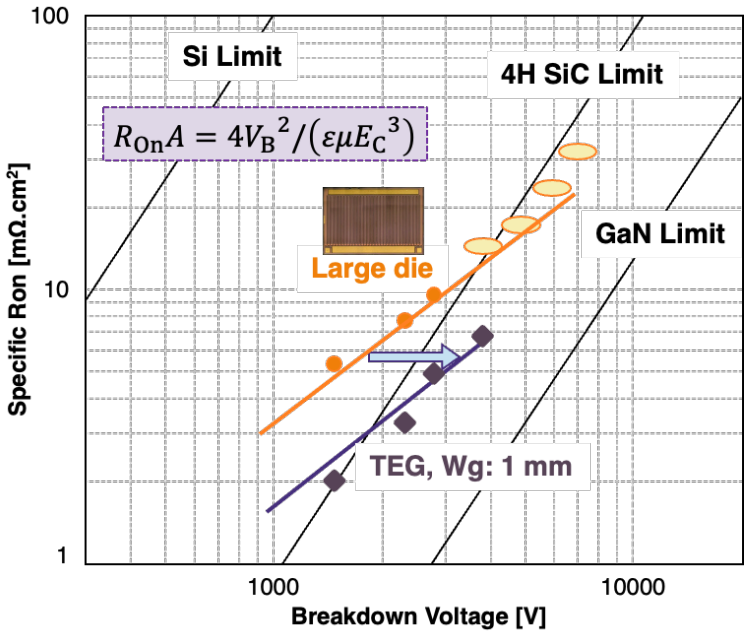


Fig. 2-10. Specific on-state resistance versus breakdown voltage of PSJ GaN devices. Adapted from [40].

PSJ devices demonstrate performance beyond the one-dimensional material limit of Si and SiC. In conventional devices, the specific on-resistance increases in proportion to the second order of breakdown voltage while in devices utilising superjunction, the specific on-resistance is directly proportional [1]. It can also be observed that small area devices (TEG) show further reduction in specific on-resistance. However, in large area devices, the performance is constrained by the fabrication and design rules which can be improved. It is important to note that, unlike conventional SJ where complexity increases with increase in breakdown voltage due to the requirement of precise control over doping, in PSJ devices the breakdown can easily be extended. This is because of the inherently balanced polarisation charges.

2.6 Avalanche Breakdown in GaN HEMTs

The highest voltage a device can handle is constrained by the on-set avalanche breakdown. For a stable and reliable operation, a margin of safety for breakdown voltage is implemented in power devices. Additionally, power devices are required to exhibit avalanche capability under surge voltage conditions. In conventional Si devices, the failure mechanisms under avalanche conditions are attributed to (1) high cell current density and (2) thermal runaway and current filamentation [54] [55]. However, research shows that conventional GaN HEMTs have a destructive avalanche breakdown once the electric field passes the critical electric field threshold [55] [56]. For this reason, manufacturers incorporate a large margin of safety which is usually over 2-3 times the rated voltage. This large margin of breakdown voltage adversely impacts the on-state performance as the drift region must be enlarged for the purpose of supporting the extra voltage. The absence of avalanche capability in GaN HEMTs is attributed to holes that are generated due to impact ionisation causing current filament formation [55] [57].

As shown in Fig. 2-11 under surge voltage conditions in an unclamped inductive switching (UIS) setup, a high voltage is developed across the device rapidly as the device turns off. Initially, the surge energy is absorbed by the device capacitance which results in a negative current flow once the voltage passes its peak. In avalanche capable devices, once the device passes its breakdown point, the surge voltage is clamped, and the energy is dissipated resistively.

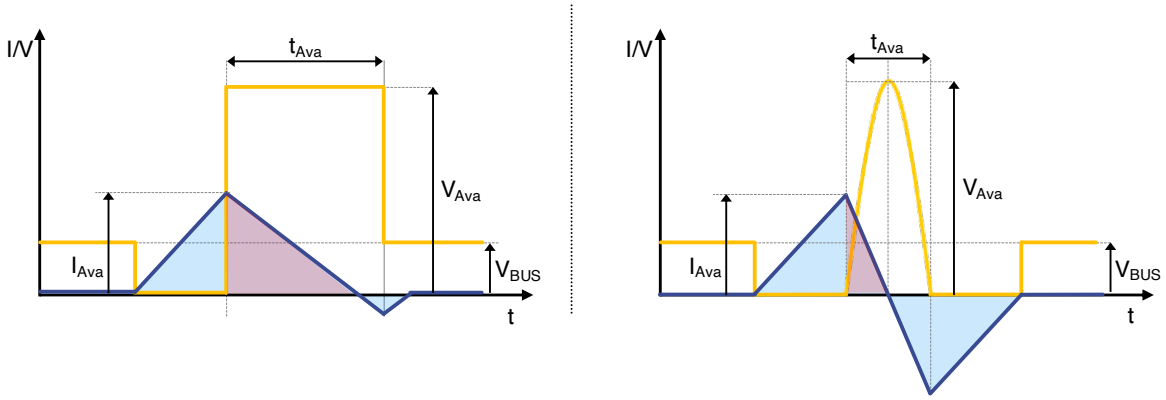


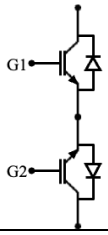
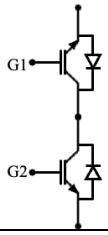
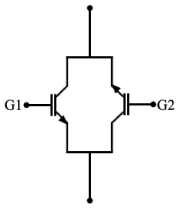
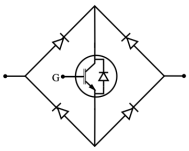
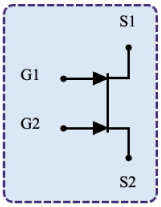
Fig. 2-11. Typical UIS waveforms of conventional power MOSFETs (left) and GaN HEMTs (right).

Conversely, in GaN HEMTs, the voltage increases across the device until it reaches the failure depending on the surge energy. Before the failure, the energy is mostly absorbed by device capacitances and dissipated via L-C resonance response. Due to this behaviour, a large margin of safety for breakdown voltage is generally implemented in GaN HEMTs.

2.7 Bidirectional Power Switches

Bidirectional power switches (BPS) are capable of four-quadrant operation that allows the device to block voltage and conduct current in either polarity direction. Full four-quadrant operation, however, is not possible in conventional FETs and IGBTs as standalone devices. Therefore, various configurations can be utilised to enable them to be used as BPS. A brief summary of various BPS configurations is outlined in Table 2-2.

Table 2-2. Comparative evaluation of bidirectional power switches.

#	Symbol	Features & Description	On-state Voltage Drop [V]	Number of Devices
A		Common source/emitter configuration One gate driver can be used.	1x IGBT + 1x diode → 3.3 V	4 (2 + 2)
B		Common drain/collector configuration Two gate drivers are required.	1x IGBT + 1x diode → 3.3 V	4 (2 + 2)
C		Requires RB-IGBTs or series connected FET with diode. [58]	1x RB-IGBT→ 2.6 V	2
D		Only one switch needs to be controlled. Simple drive requirements. [59]	1x IGBT + 2x diodes→ 5.0 V	4+1
E		True monolithic GaN BPS FET.	1x GaN BPS→ 1.0 V	1

Please note that the IGBTs in Table 2-2 can be swapped with FETs or BJTs except in ‘C’ configuration where additional series diodes are needed to prevent reverse conduction. There are other BPS configurations based on reverse conducting IGBTs (RC-IGBT) and gate turn-off thyristor (GTOs). Using RC-IGBTs eliminates the need for additional anti-parallel diodes.

The multi-device configurations of BPS contribute to additional conduction and switching losses and circuit complexity [60] [61]. A true bidirectional power switch can overcome such limitations by design. GaN HEMTs are particularly attractive for integration in BPS because of their low on-resistance in lateral device configuration [62] especially in the form of PSJ technology [63]. This is because the drift region can be shared between the constituents making its resistance ½ lower compared to discrete solutions. A cross-sectional diagram of the GaN PSJ BPS is sketched in Fig. 2-12.

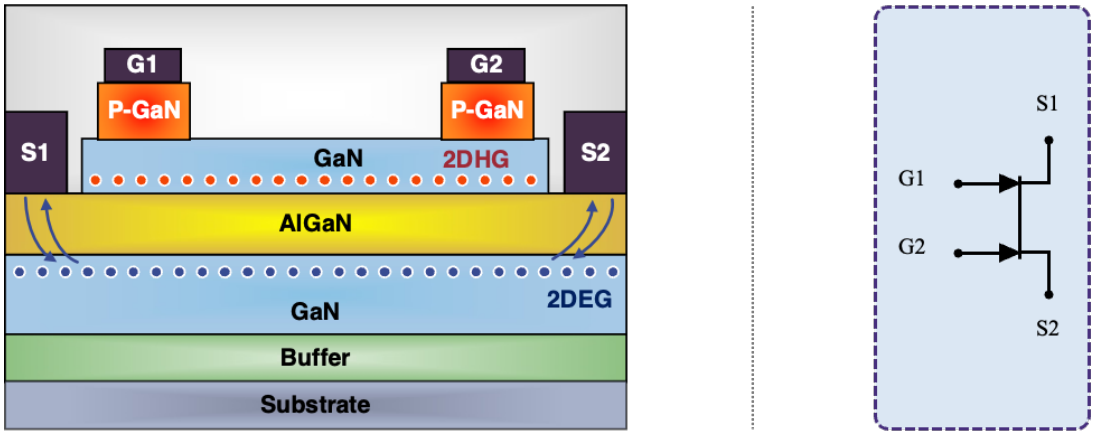


Fig. 2-12. Cross-sectional view of a BPS using PSJ concept configured as common drain (left) and circuit symbol (right).

The operating principle of GaN BPS is essentially the same as conventional HEMTs where each gate needs to be driven accordingly with respect to their corresponding source potential (i.e., G1 - S1 and G2 - S2). GaN BPS can facilitate various applications such as matrix converters and solid-state DC circuit breakers which require bidirectional switching capability.

2.8 Chapter Conclusion

Significant progress has been made towards improving voltage blocking and on-resistance of GaN devices to approach the material limit. The high density and high mobility of 2D electrons gas created at the heterointerface enables the design of transistors and diodes with minimal

on-resistance and extremely fast switching speed suitable for high power density efficient power electronics integration. The PSJ concept is essential to effectively exploit the full potential of GaN technology for the next generation devices in a cost-effective manner. PSJ devices can overcome several hurdles associated with GaN HEMTs and are ideal for usage in extreme environments such as aerospace, transport, and marine applications. While normally-off configurations have been previously demonstrated, their performance usually involves trade-offs. Further work needs to be done to minimise such performance losses. Additionally, GaN HEMTs fabricated on insulating substrates are ideal for the development of power integrated circuits and bidirectional switches.

Chapter 3

Polarisation Super Junction GaN Diodes

Power diodes are amongst critical active components used in the conversions and control of electrical power in a wide range of applications. Power diodes are categorised as PiN, Schottky, and merged PiN Schottky (MPS) in terms of device structure. PiN diodes belong to the bipolar device category, whereas Schottky diodes are unipolar devices. The MPS structure is attractive for high voltage diode construction due to its advantageous attributes inherited from Schottky and PiN diodes. In this chapter, for the first time, a comprehensive analysis of the 1.2 kV PSJ GaN Schottky diodes is presented. The device operating physics is discussed, and its characteristics are experimentally evaluated. Additionally, the surge current handling capability of the device is investigated.

3.1 Structure and Physics of Operation

PSJ GaN diodes utilise a hybrid design similar to that of the merged PiN and Schottky structure to offer high voltages and fast switching. The cross-sectional and top view of a 1.2 kV PSJ GaN diode are provided in Fig. 3-1.

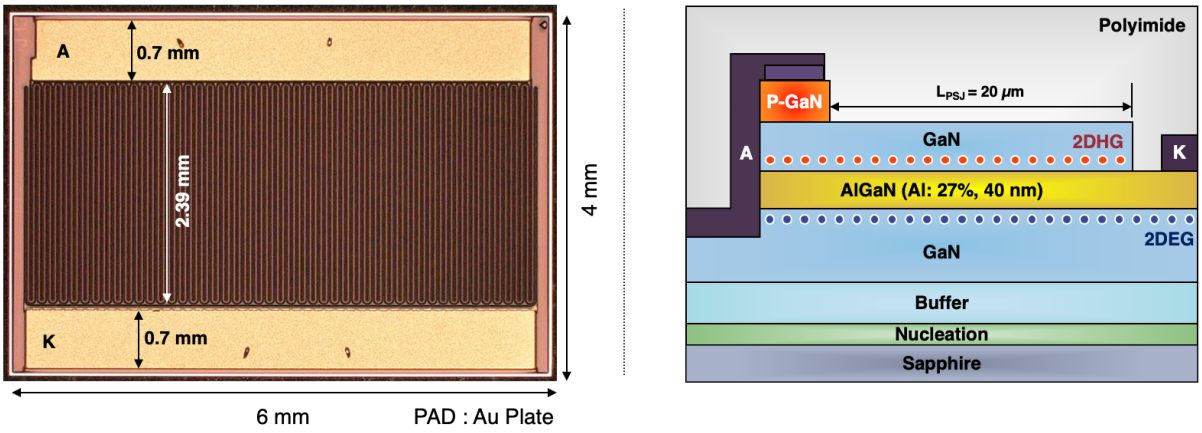


Fig. 3-1. Top view and cross-sectional view of a 1.2 kV PSJ GaN diode. The anode and cathode are marked as 'A' and 'K' respectively.[1]

The diode has many similarities to the PSJ GaN HEMT that is discussed in Chapter 4. The key distinction between the PSJ diodes and HEMTs is that, in PSJ diodes, the gate and source electrodes are joined to form the anode contact. The anode consists of a Schottky contact with 2DEG and an ohmic contact to 2DHG. Consequently, a parallel PiN diode is formed, comprising the P-GaN, 2DHG, and 2DEG layers. Under normal operating conditions, the total current passes through the Schottky region of the diode due to its lower voltage drop compared to the PiN region. Under reverse bias state, a depletion is formed by the removal of 2DHG via the P-GaN and 2DEG via the cathode terminal that shields the anode when subjected to a strong electric field. Consequently, due to the charge balance, the electric field spreading is even over the length of the drift layer, which enables the diode to withstand high voltage with minimal leakage current.

The devices used in this chapter (and future chapters) are assembled using a wedge manual wire bonder (F&K delvotec 5430) on gold plated direct bond copper (DBC) substrates. The

[1] Published in (1)

bond wire used to connect the device to the substrate is aluminium heavy wire. A photograph of an assembled device is provided in Fig. 3-2.

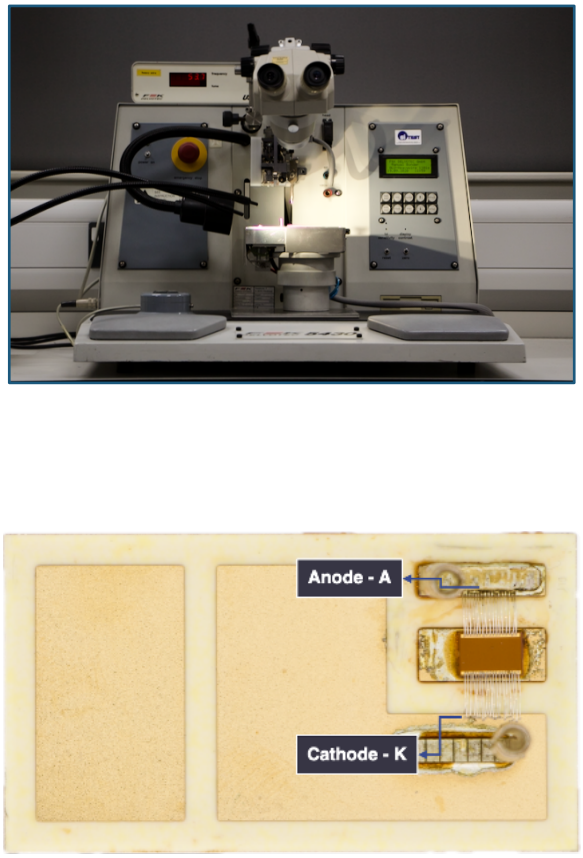


Fig. 3-2. Photograph of the F&K5430 heavy wire bonder and a 1.2 kV PSJ GaN diode assembled on DBC substrate.

3.2 Device Characteristics

3.2.1 Forward characteristics

The forward bias characteristics of the 1.2 kV PSJ GaN diode were measured at different temperatures in a controlled temperature oven using the Tektronix 371B high power curve

tracer and are shown in Fig. 3-3. The measurements were carried under pulse mode conditions to avoid self-heating effects.

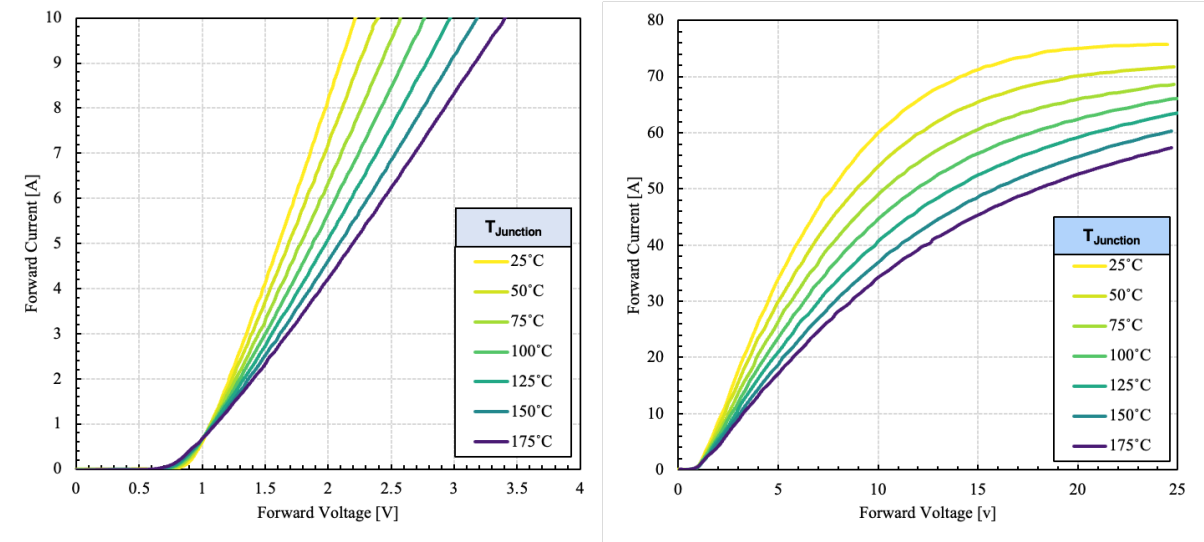


Fig. 3-3. Forward bias I-V characteristics of the 1.2 kV PSJ GaN diode at different junction temperatures. The pulse width is 250 µs.[2]

The slope resistance at 25˚C is equal to 120 mΩ which is comparable to the resistance of the 1.2 kV PSJ GaN HEMTs (at V_{GS} = 0 V) that is discussed in Chapter 4. This similarity arises due to the identical drift region length between both devices. The knee voltage decreases from ~ 0.8 V at 25˚C to ~ 0.6 V at 175˚C. The zero temperature coefficient (ZTC) point occurs at 0.7 A and 1.0 V. The diode exhibits a positive temperature coefficient (PTC) of forward voltage drop, which can be observed in Fig. 3-4.

[2] Published in (1).

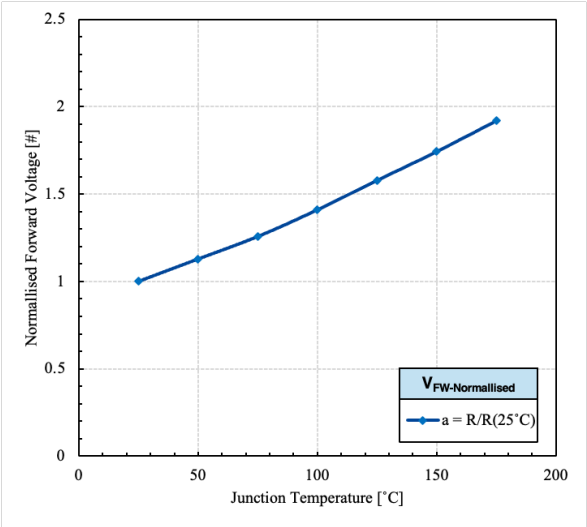


Fig. 3-4. Normalised forward voltage drops at different junction temperatures. The anode current is 5 A.

Although the PSJ GaN diode has a merged PiN Schottky structure, the device exhibits a unique current saturation behaviour at around 76 A. This phenomenon originates from the short minority carrier lifetime in GaN heterostructures along with the high bipolar on-set voltage associated with the GaN PiN region. Under extreme operating conditions such as a surge current transient, it is possible for the bipolar mode to be activated, which leads to injection of holes and possible degradation or failure of the diode. The operating performance of the PSJ GaN diodes under surge current conditions is discussed further in detail in Sect. 3.3.

3.2.2 Capacitance versus reverse voltage

The junction capacitance (C_J) as a function of cathode voltage ($V_{K\text{-}A}$) was measured using an Agilent B1505 power device analyser and is shown in Fig. 3-5.

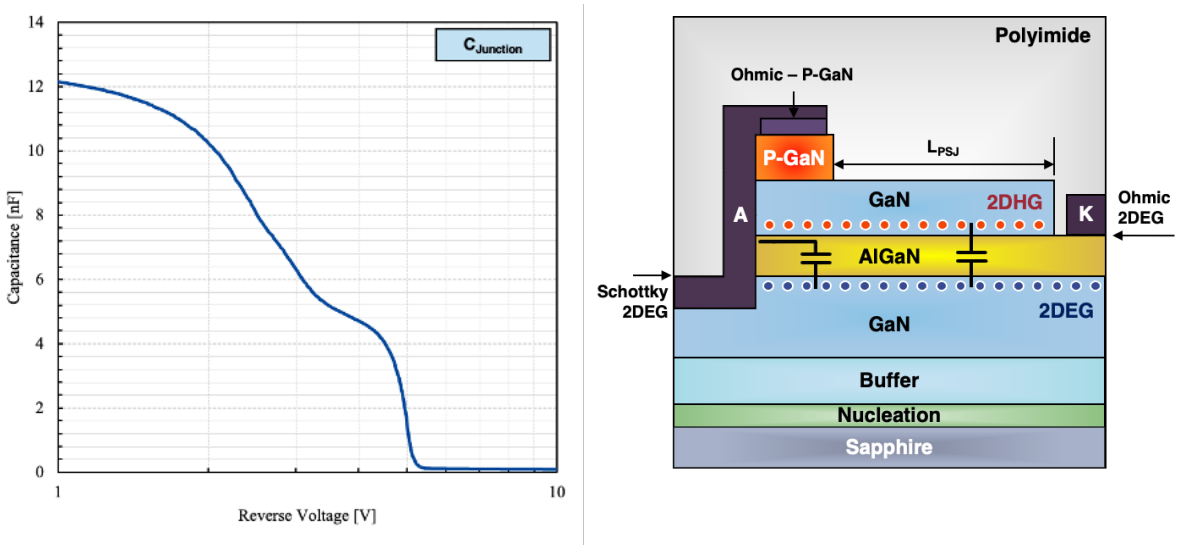


Fig. 3-5. Measured C-V characteristics of the 1.2 kV PSJ GaN Schottky diode at RT and cross-sectional view of the device highlighting the capacitances.[3]

Two humps can be observed in the C-V characteristic, which corresponds to the depletion of the 2DHG followed by the second depletion due to the 2DEG. The initial depletion occurs beneath the Schottky region at 3.3 V followed by another depletion at 5.5 V corresponding to the ohmic contact. Similar behaviour has been reported for small area PSJ diodes [64]. In conventional GaN diodes, one step depletion process occurs due to the absence of 2DHG [64].

3.3 Surge Current Capability

Power diodes often are required to withstand surge current transients several times higher than their nominal current rating for a short period and therefore, it is regarded as a reliability factor [65] [66]. Surge current typically occurs under specific circumstances such as circuit power-up sequence with a large inrush current transient or under fault conditions [67]. Several studies have demonstrated surge current behaviour of Si and SiC diodes [65] [68] [69] [70] [71] [72]. For SiC diodes, many reports show that the MPS structure protects the Schottky interface by

[3] Published in (1).

reducing the stress due to high electric field which improves their blocking voltage along with the surge current capability [71] [73] [74]. In this section, for the first time, the surge current capability of the 1.2 kV PSJ GaN diode is experimentally analysed.

3.3.1 Experimental setup

To assess the surge current capability, an experimental test bench was constructed as depicted in Fig. 3-6.

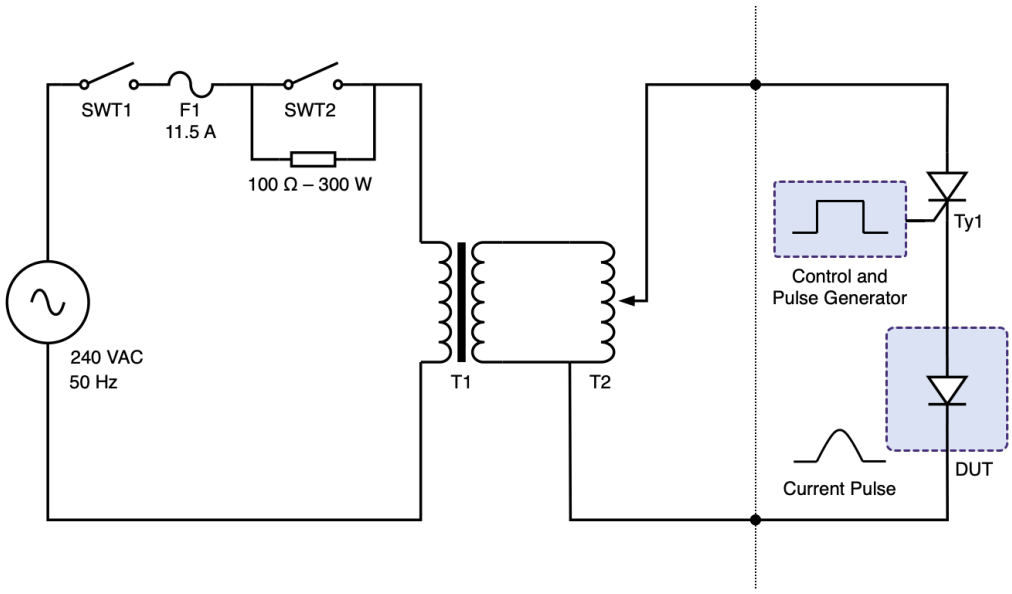


Fig. 3-6. Circuit diagram of the surge current test setup. Once the control signal is triggered, a 10 ms half-sine current pulse is imposed on the DUT.

The power is supplied via the mains AC at 240 V and 50 Hz via an isolation transformer (T1) that is used to isolate the device under test for safety purposes. The test voltage across the device under test (DUT) is adjusted via an autotransformer (T2) to control the desired surge current flow. The purpose of the R1 resistor is to limit the inrush current which occurs during the power-up of the system and magnetisation of the transformers. The switch – SWT2 is a bypass mechanism once the circuit is powered up. A thyristor is used as the trigger mechanism which is connected to a synchronous pulse generator as illustrated in Fig. 3-7 and Fig. 3-8.

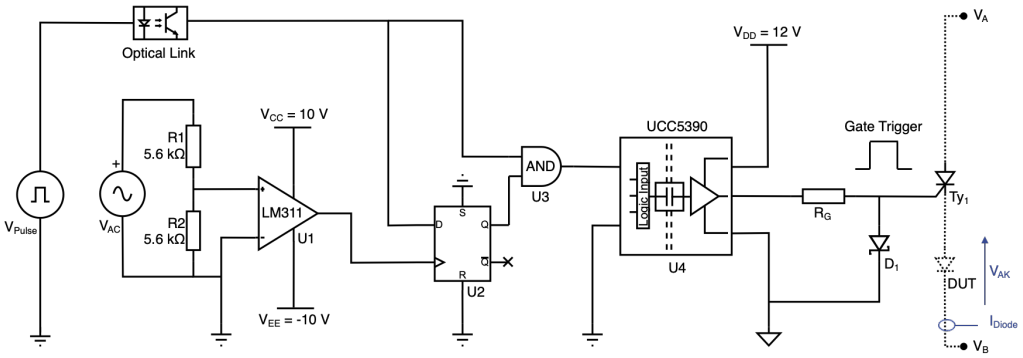


Fig. 3-7. Simplified circuit diagram of the synchronous pulse generator.

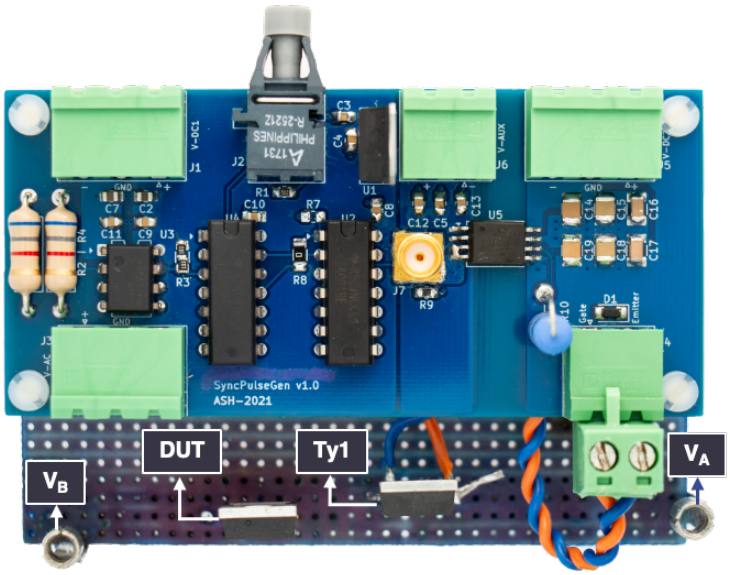


Fig. 3-8. Photograph of the practical implementation of the surge current test board.

The pulse generator is designed to output a trigger signal that is synchronised with the 50 Hz input AC source to drive the thyristor. To achieve this, a differential comparator (LM311) is used to create a synchronised square wave signal with the input AC source. The comparator monitors its input and compares it to the reference voltage (0 V). When the input voltage is positive, the comparator outputs a high state, and when the input voltage is below zero, it outputs a low state. A resistor divider circuit consisting of R1 and R2 is used to attenuate the input AC source. The output of the comparator is connected to the clock input of a D-type

flip-flop (CD4013B) which is responsible for detecting the user input via the optical link (for safety reasons) and generating the trigger signal. Finally, an AND logic gate (CD4081) is employed to prevent false triggering by comparing the output of the flip-flop to the user input and passing the signal only if both inputs are in a high state. Once the thyristor turns on, a half-cycle sine wave current pulse is applied to the DUT.

To establish the maximum surge current handling capability of the device, a 10 ms pulse which corresponds to the 50 Hz input frequency is applied to the DUT at different current levels until device failure. The tests are carried out at room temperature. The forward voltage across (V_{AK}) and current through (I_{Diode}) the device are monitored using a differential voltage probe and a clamp current probe, respectively. A number of end-of-life (EOL) criteria and ageing mechanisms including an increase in forward voltage drop, a change in leakage current, and premature failure were studied to determine the impact of surge current on the device. The device characteristics were measured prior to the test and also after every 10 A current step to monitor any changes or degradation in performance.

3.3.2 Surge current capability of PSJ GaN diodes

The test was carried out to determine the maximum surge current capability of the PSJ GaN diodes. A 10 ms half-sine current pulse was applied to the DUT at different current levels as depicted in Fig. 3-9 along with the corresponding surge current I-V characteristics.

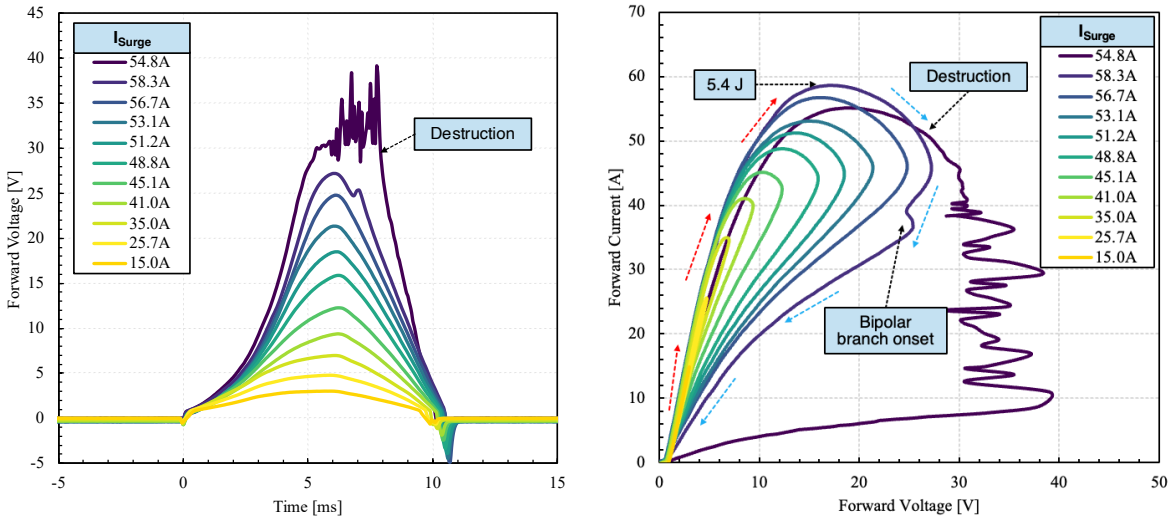


Fig. 3-9. Voltage waveforms and surge current I-V characteristics of the 1.2 kV PSJ GaN diode under surge current events. The pulse width is 10 ms. T_{amb} = 25˚C.[4]

The surge current increases with the applied voltage until the device fails, which occurs at ~ 30 V. The diode survived a surge current pulse of nearly 60 A. The maximum deposited energy during the last surge current pulse was measured to be 5.4 J. Looking at the surge current I-V curves, a loop is formed at higher surge current levels with distinct forward (rising) and return (falling) branches. As a result of the positive temperature coefficient of the resistance, the current in the return branch is lower and the dissipated heat results in an increase in the junction temperature and higher resistance. Prior to the failure, at 58.3 A pulse, a second peak is observable on the voltage waveform, indicating the activation of the bipolar mode of operation. The increase in voltage leading to the triggering of the bipolar mode only occurs in the return branch because of the thermal dependency of the bipolar on-set voltage. The heat produced because of the surge current event reduces the built-in potential of the PiN region, along with the decreased mobility of the 2DEG beneath the P-GaN region. This results in higher resistance and a larger voltage drop across the PiN diode that is sufficient to trigger the

[4] Published in (1).

bipolar current conduction and the injection of minority carriers from the P-GaN layer. In the rising branch at 25 V, no sign can be observed which is due to the likely thermal effect on the device. It should be noted that such behaviour is not observable on the extended forward characteristics presented before in Fig. 3-3 due to the shorter pulse width of 250 µs used for the measurements, which does not contribute to a significant increase in temperature. Eventually, the destruction occurred at approximately 60 A due to the high magnitude of current. In the final surge current pulse, at 54.8 A, a significant degradation can be seen on the rising branch before failure due to partial impact caused by the preceding surge event.

3.3.3 Surge current capability of MPS SiC diodes

For the purpose of comparison, a 1200 V SiC MPS diode [75] with comparable rating was tested under the same conditions presented in the preceding section. The measured surge current waveforms of the SiC diode are presented in Fig. 3-10.

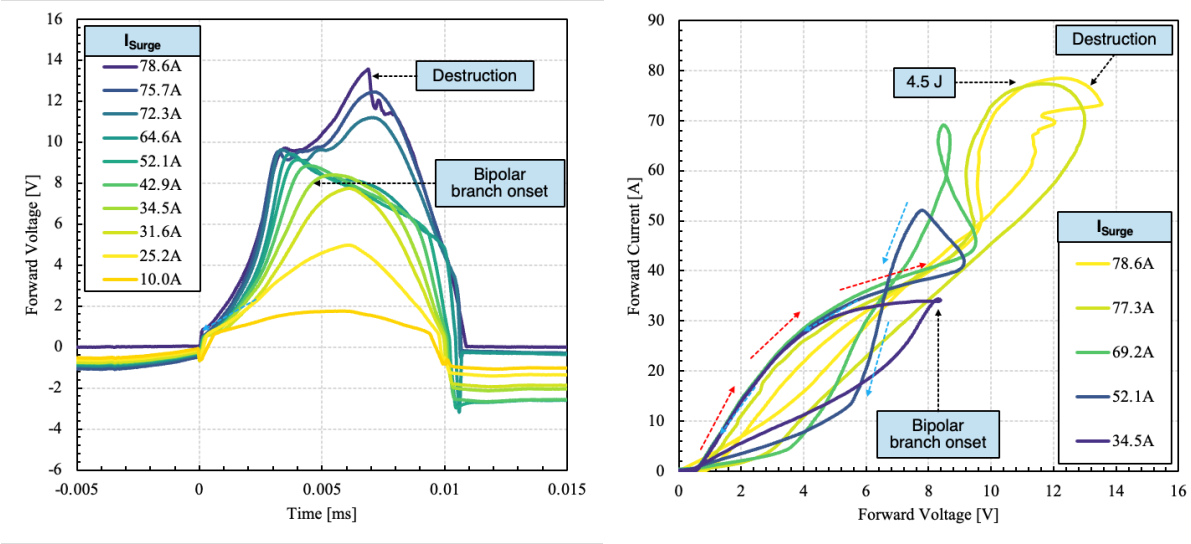


Fig. 3-10. Voltage waveforms and surge current I-V characteristics of the1.2 kV SiC MPS diode under surge current events. The pulse width is 10 ms. T_{amb} = 25˚C.

Similar to the GaN diode, due to an increase in temperature, a loop is formed separating the return branch and rising branch. The SiC MPS diode clearly shows the activation of the bipolar

mode at approximately 8 V, which can be seen as the 'twisted' I-V curve that leads to the formation of a second loop. Due to the activation of the PiN regions, holes are injected into the drift layer modulating its resistance, evident by the change in the slope of the I-V curves. The bipolar current flow results in a change in the peak voltage and the formation of a second peak before failure. This behaviour is not evident in the GaN diode until the destruction. Before the failure, a third loop appears in the surge current I-V curves at about 69 A. This is likely due to thermal runaway, which eventually leads to breakdown. Previous studies on surge current handling in SiC MPS diodes have reported similar performances [65].

3.3.4 Influence of surge current and ageing mechanism

The static characteristics were monitored for variation in the device's performance. The characteristics before the test and before the failure (after the 50 A surge current pulse) are shown in Fig. 3-11.

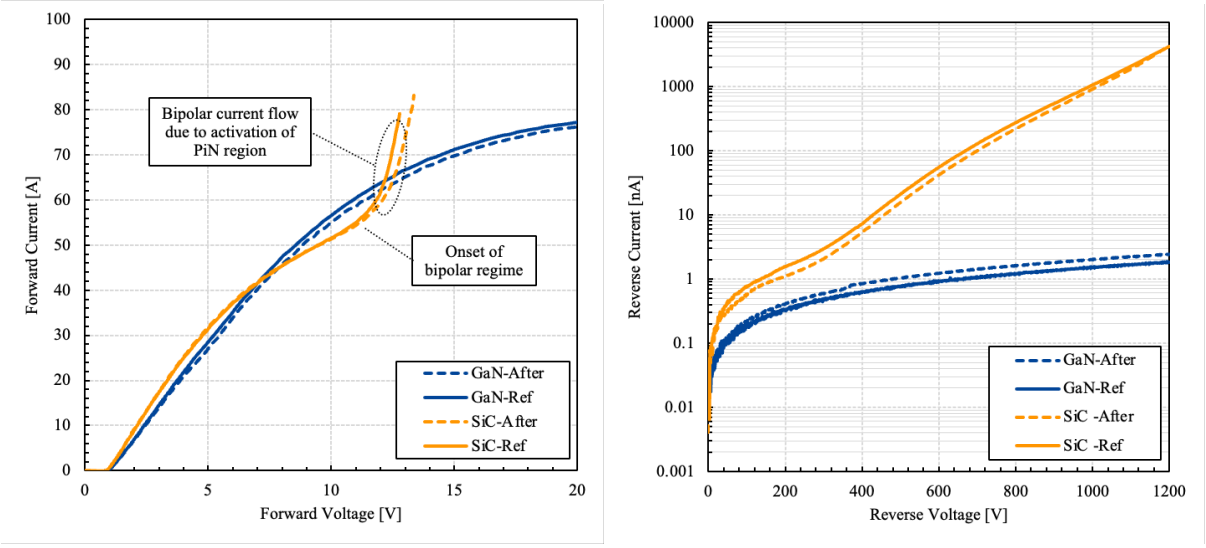


Fig. 3-11. Forward characteristics and reverse characteristics of the PSJ GaN diode and the SiC MPS diode prior to the test (solid line) and before the failure after the 51 A and 70 A surge current pulses (dashed line).

The GaN diode shows a minor shift in forward voltage, which is particularly noticeable at higher currents. Similarly, the reverse leakage current shows a minor increase in magnitude before failure.

3.3.5 Failure mechanism and analysis

The device finally broke down after the surge current pulse of nearly 60 A due to the high magnitude of current in the open-circuit state. A photograph of the device showing the burnt region due to the destructive surge is provided in Fig. 3-12.

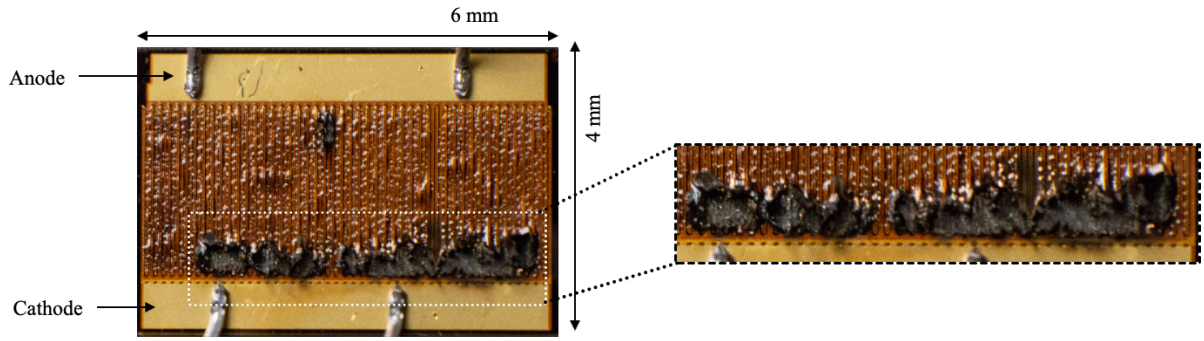


Fig. 3-12. Photograph of the PSJ GaN diode after the failure due to the surge current. The failure spots can be observed in the highlighted region distributed uniformly across the device.[5]

The failure spots are consistently observed on the anode fingers in close proximity to the cathode terminal distributed evenly across the device showing that the current flow was uniform prior to the failure. The failure is caused by the activation of the P-GaN contact close to the anode, where the impact of failure is visible. The injection of high energy minority carriers from the P-GaN region may lead to lattice damage and subsequent device failure.

[5] Published in (1).

3.4 Reverse Recovery

Power diodes experience reverse recovery when transitioning from on-state conduction to off-state blocking mode. The stored charge carriers that are present within the drift region should be extracted before the diode can regain its blocking capability which results in reverse recovery current flow [76]. The reverse recovery loss in diodes is frequency dependent and limits high operating frequency operations. Bipolar PiN diodes, in particular, show high reverse recovery current and charge compared to Schottky counterparts. This is attributed to the additional charge carriers injected due to conductivity modulation into the drift region. Schottky diodes do not suffer from such a recovery mechanism and the only reverse current flow is initiated by the capacitively stored charges [77]. MPS diodes are effectively the same as pure Schottky diodes because they operate in the unipolar regime under normal operating conditions and no conductivity modulation is involved. This section will cover the reverse recovery performance and mechanism of the PSJ GaN diodes.

3.4.1 Reverse recovery experimental setup

To evaluate the reverse recovery characteristics, a clamped inductive switching test bench, commonly referred to as a double pulse test, as shown in Fig. 3-13, was used.

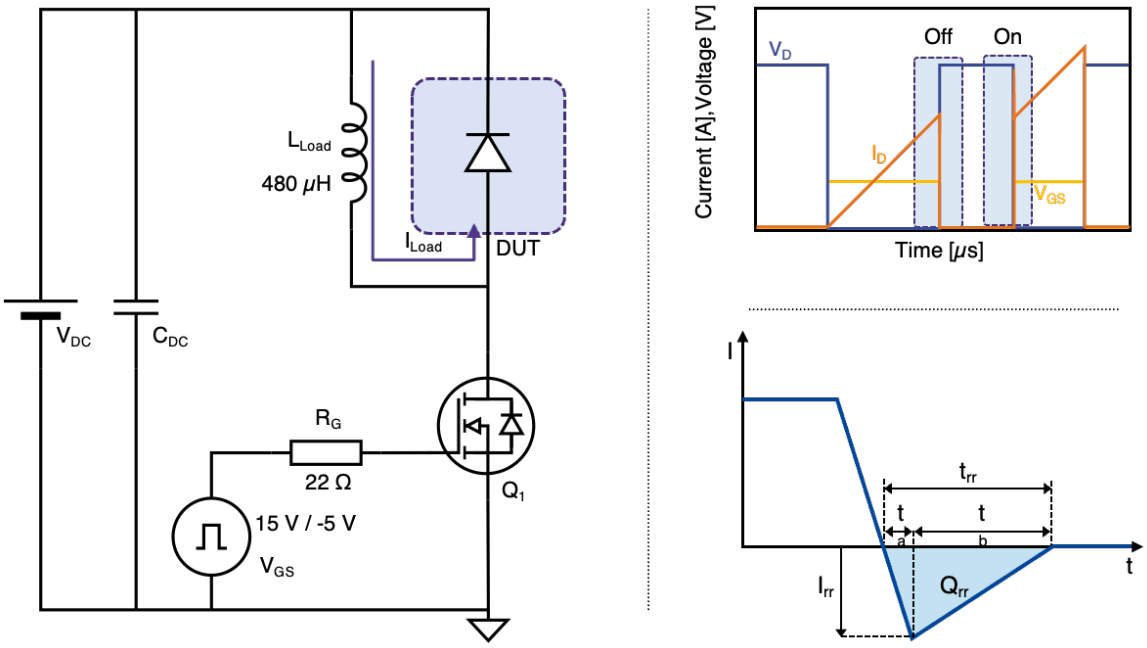


Fig. 3-13. Test circuit for measuring diode reverse recovery characteristics and typical waveforms.

Fig. 3-14. Photograph of the practical implementation of the double pulse tester for diode reverse recovery measurements.

An inductive load of 480 µH is used in the setup. To ensure a stable input DC voltage, a set of 20 µF capacitors is used in parallel with the DC source. An isolated gate driver board (based on the UCC5390E) is used to provide the required gate voltage of 15 V and -5 V for turn-on and turn-off, respectively, for the main switch. As the diode transitions from forward

conduction to reverse bias state, the reverse recovery occurs. The reverse recovery charge (Q_{rr}) corresponds to the highlighted area in Fig. 3-13 and can be calculated as given by Eq. (3-1).

$$Q_{\mathrm{rr}} = \int_{t0}^{t_0+t_{\mathrm{rr}}} i.dt. \qquad (3\text{-}1)$$

The ratio of fall time (t_b) to rise time (t_a) of the current waveform determines the softness factor (S) of the reverse recovery that is given by Eq. (3-2).

$$\text{Softness factor} = \frac{t_{\mathrm{b}}}{t_{\mathrm{a}}}. \qquad (3\text{-}2)$$

The soft recovery process happens when the softness factor is more than 1. Otherwise, the term “snappy” is used when the softness factor is less than 1.

3.4.2 Reverse recovery results

Using the circuit presented in Fig. 3-13, the reverse recovery of the diode was measured at different current levels as shown in Fig. 3-15. The current was gradually raised by incrementally increasing the voltage from 50 V to 300 V in steps of 50 V.

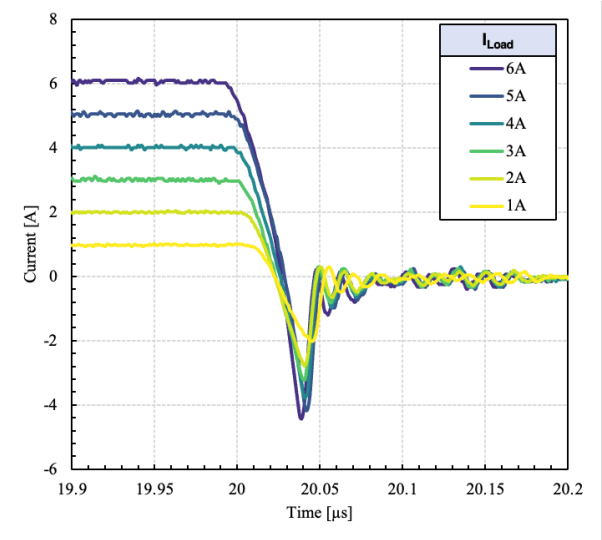


Fig. 3-15. Reverse recovery waveforms of the 1.2 kV PSJ GaN diode as a function of load current and voltage. T_{amb} = 25˚C.[6]

The measured charge (Q_{rr}) associated with the reverse recovery of the device is 45 nC at I_{Load} of 6 A. The reverse recovery time (t_{rr}) corresponds to 20 ns. The diode has snappy recovery with a 0.6 softness factor. The peak reverse recovery current ($I_{rr\text{-}peak}$) saturates at about - 4.35 A.

3.5 Chapter Conclusion

In this chapter, the performance, working mechanism, and surge current capability of PSJ GaN diodes have been investigated for the first time. According to the results, the PSJ diode can survive a surge current event 8 times above its rated current. Notably, a distinct behaviour has been observed where no bipolar current flow occurs until failure. The maximum energy dissipated due to the surge current before failure was measured to be 5.4 J. The failure mechanism is associated with the injection of high energy minority and high surge current levels. Meanwhile, the SiC MPS diode with similar ratings exhibited 4.5 J of surge current energy before failure. The results presented in this chapter show that GaN diodes can be an

[6] Published in (1).

alternative solution to SiC MPS diodes at a lower cost without compromising performance. PSJ GaN diodes are an ideal candidate for integration in advanced power electronic designs that require high efficiency and high frequency.

Chapter 4

Polarisation Super Junction GaN HEMTs

The PSJ concept can be used to design high performance HEMTs with high breakdown voltages and low resistances that can potentially perform beyond the one-dimensional material limit. In this chapter, the characteristics of 1.2 kV and 3.0 kV PSJ GaN HEMTs will be experimentally evaluated and analysed to gain an insight into their in-application performance. The turn-off dV/dt will also be investigated to further understand the device capability and performance for motor drive applications.

4.1 Physics of Operation

The cross-sectional and top view of 1.2 kV PSJ GaN HEMTs are illustrated in Fig. 4-1.

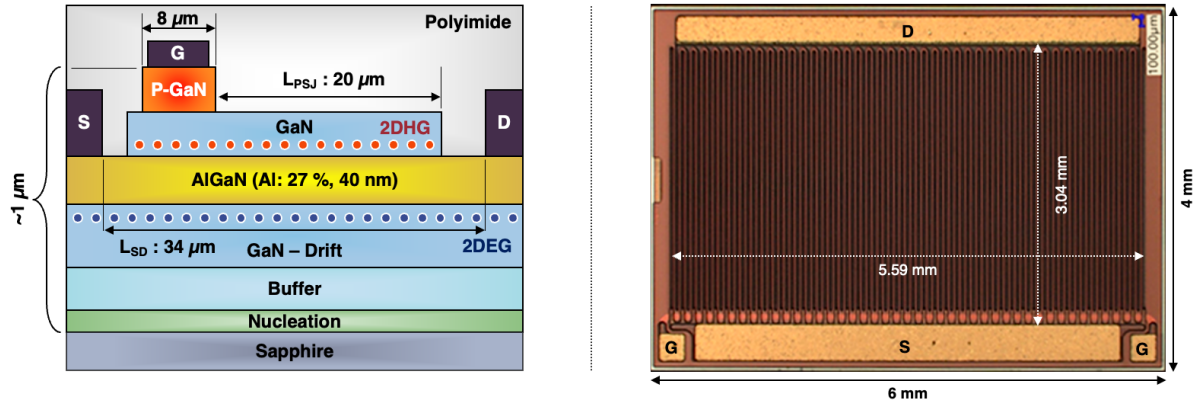


Fig. 4-1. Cross-sectional view (left) and top view (right) of 1.2 kV GaN PSJ HEMTs. Gate, drain, and source terminals are marked as G, D, and S respectively.[7]

The active area of the device is 17 mm^2. The number of fingers connected to the source and drain terminals are 44 and 43, respectively. The GaN drift region length (L_{PSJ}) between drain and gate is 20 µm which enables the device to support over 3 kV under off-state conditions. The large margin of safety is required because GaN HEMTs are susceptible to irreversible avalanche breakdown. The presence of an uninterrupted 2DEG channel between drain and source provides a direct route for the current flow at 0 V gate bias in either polarity. The P-GaN gate structure provides an ohmic connection to the 2DHG, and it is critical for device performance. The P-GaN enables injection and extraction of holes which allows the device to have uniform electric field distribution and collapse free operation. The gate structure also forms two PN junction diodes between gate drain D_{GD} and gate source D_{GS}. This imposes a limit on the maximum allowable gate voltage that, if exceeded, results in a large leakage current flow. A negative gate bias larger than its threshold is needed to deplete the 2DEG channel beneath the gate, and consequently, turn off the device.

[7] Published in (3).

4.2 Static Characteristics

4.2.1 On-state characteristics

The output (I-V) characteristics of the device at different gate voltages were obtained in pulse mode as given in Fig. 4-2.

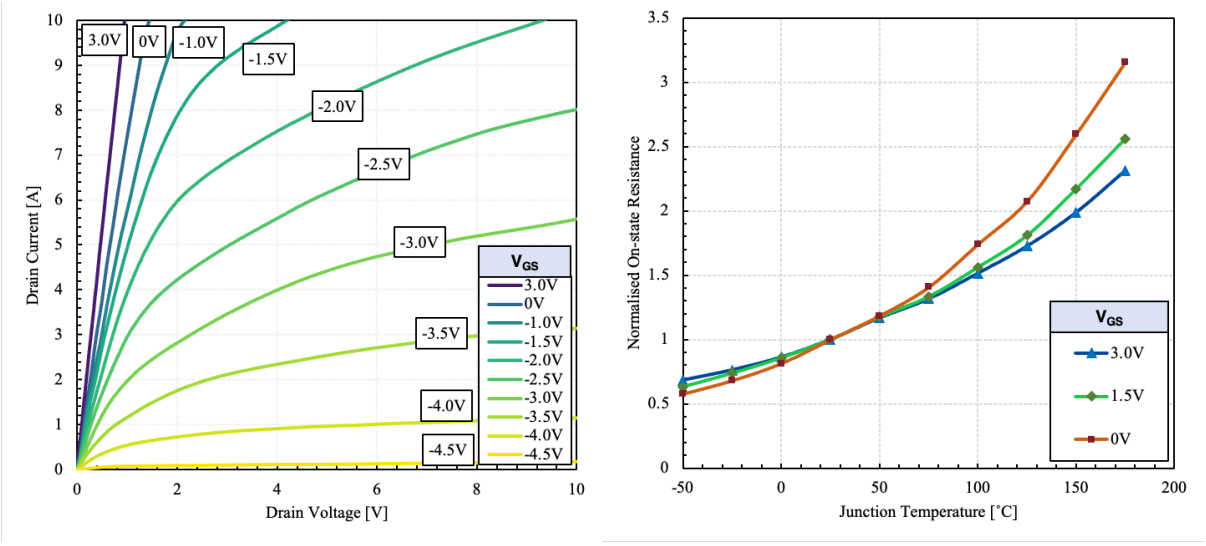


Fig. 4-2. Forward bias output characteristics of the 1.2 kV PSJ GaN HEMT at RT (left) and its normalised on-resistance at different temperatures and gate voltages (right). The pulse width is 250 µs.[8]

The on-state resistance is responsible for on-state conduction losses, which are load dependent. The on-resistance at RT can be derived from measured I-V curves which correspond to 93 mΩ and 140 mΩ at V_{GS} of 3 V and 0 V, respectively. Higher gate bias results in the accumulation of additional charge carriers within the 2DEG channel that lowers the on-resistance. However, the upper limit of the positive gate voltage that can be applied is determined by the two diodes which are formed between gate-drain (D_{GD}) and gate-source (D_{GS}) with ~ 3.5 V bipolar on-set voltage. Exceeding this limit will forward bias these diodes and excessive gate leakage current occurs. The normalised on-state resistance of the device

[8] Published in (3).

was obtained from the measured I-V characteristics at varying junction temperatures and gate voltages as plotted in Fig. 4-2. The on-resistance increases with the rise in temperature due to lattice scattering and reduced mobility. The HEMT maintains a positive temperature coefficient of on-resistance which is essential for stable operation across a broad range of operating conditions. This is particularly important in the case of effective parallel operation and even current sharing between multiple devices. The PTC is also essential for a single chip reliable operation and preventing thermal runaway. Meanwhile, it should be noted that wide bandgap SiC MOSFETs exhibit a negative coefficient of temperatures (NTC) at low temperatures, which puts GaN in an advantageous position for low temperature applications.

The transfer characteristics were measured at a drain voltage of 10 V at different junction temperatures, as illustrated in Fig. 4-3.

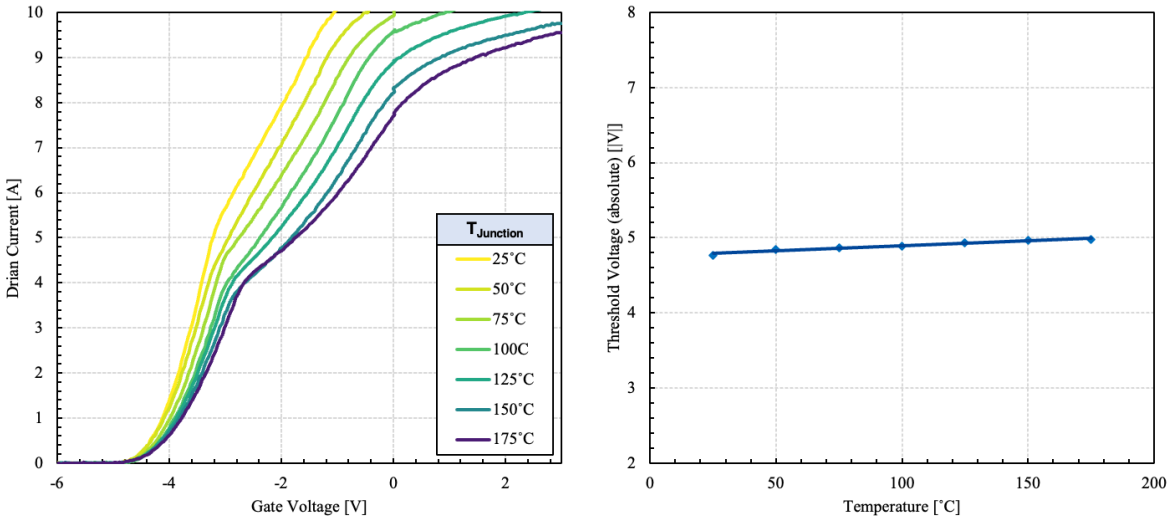


Fig. 4-3. Transfer characteristics measured at V_{Drain} = 10 V and threshold voltage of the 1.2 kV PSJ GaN HEMT at different junction temperatures.

The threshold voltage corresponds to -4.8 V at RT (I_{DS} = 1mA). The variation in threshold voltage at high temperature is negligible indicating a 5% increase at 175˚C. It is also noted that the threshold voltage for the 1.2 kV (L_{PSJ} = 20 µm) and 3.3 kV (L_{PSJ} = 40 µm) devices is

effectively identical, suggesting that the drift region length has no impact on threshold voltage, as expected.

4.2.2 Off-state characteristics

Low leakage current is an important parameter, particularly for high voltage devices because the dissipated power due to the product of leakage current and off-state blocking voltage can be substantial. The off-state leakage current characteristics of the 1.2 kV PSJ GaN HEMTs were measured at different temperatures and are shown in Fig. 4-4.

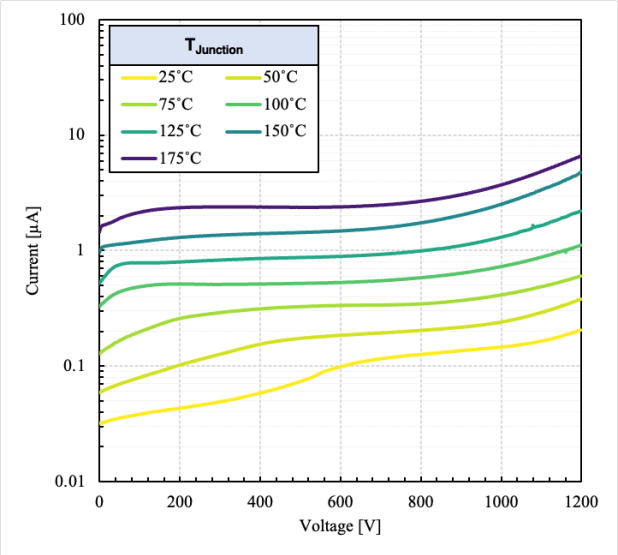


Fig. 4-4. Leakage current characteristics of the 1.2 kV PSJ GaN HEMT at different junction temperatures. V_{GS} = -10 V.

As observed, the leakage current at RT corresponds to approximately 0.2 μA at full blocking voltage and does not considerably rise with the temperature. The primary component in the leakage current of PSJ HEMTs is due to the gate leakage. Si bipolar devices with similar ratings show much higher leakage current especially at high temperatures.

4.2.3 Capacitance characteristics

The switching characteristic of FETs is determined by the internal parasitic capacitances which are inherent to their structure. Fig. 4-5 shows measured capacitances of the 1.2 kV PSJ GaN HEMT at 1 MHz frequency.

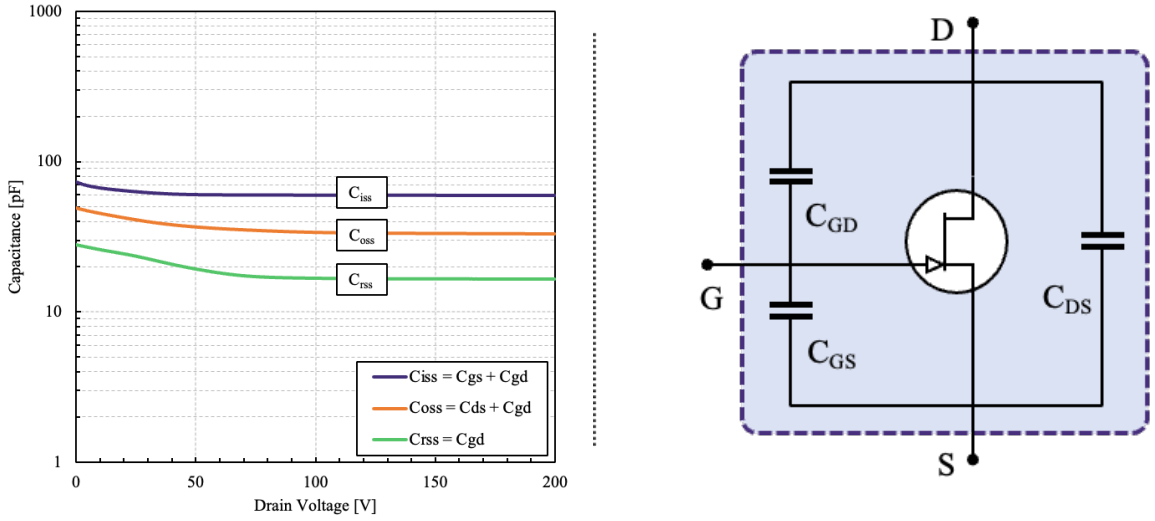


Fig. 4-5. Measured internal capacitances of the 1.2 kV PSJ GaN HEMT at 1 MHz frequency. T_{amb} = 25°C.[9]

Similar to other FETs, the capacitance decays with the increase in the drain voltage (V_{DS}). The impedance and current source/sink capability of the gate drive circuit determine the rate at which these capacitances are charged and discharged, and therefore the switching behaviour of the device is affected. However, the maximum dV/dt occurs during the Miller transient, which can be calculated in Eq. (4-1).

$$\frac{dV_{\mathrm{DS}}}{dt} = \frac{I_{\mathrm{G}}}{C_{\mathrm{GD}}} = \frac{V_{\mathrm{G}}}{R_{\mathrm{G}}.C_{\mathrm{GD}}} \qquad (4\text{-}1)$$

[9] Published in (3).

In the present PSJ configuration, the 2DHG acts as an extension to the P-GaN gate. Therefore, the gate-drain capacitance is influenced by the overlap of 2DHG and 2DEG which is optimised for a wide range of dV/dt controllability.

4.3 Dynamic Switching Characteristic

The switching losses are predominantly influenced by the dynamic characteristics of the device. Switching losses are frequency dependent and impose a limit on high frequency operation. Thus, for efficient and high-power density operation, fast switching with minimal losses is required. However, in a number of applications, such as motor drives, the sharp switching edges of GaN HEMTs can be problematic, and dV/dt may need to be reduced.

4.3.1 Experimental setup

To evaluate the switching performance of the PSJ GaN HEMTs, a clamped inductive test bench was used as depicted in Fig. 4-6.

The setup uses a 1.185 mH inductor along with a 1.2 kV SiC MPS freewheeling diode. The gate driver provides the required gate bias, which can be adjusted accordingly. The rise time and fall time are measured as the change in the drain voltage from 10% to 90% of its maximum value. In each switching cycle power is dissipated as heat because of the overlap of the drain voltage and current. The area beneath the curve produced by the product of voltage and current ($P = I.V$) represents the dissipated energy which corresponds to the integration of the dissipated power as given by Eq. (4-2).

$$E_{\mathrm{SWT}} = E_{\mathrm{Off}} + E_{\mathrm{On}} = \int V_{\mathrm{Drain}}.I_{\mathrm{Drain}}.dt \qquad (4\text{-}2)$$

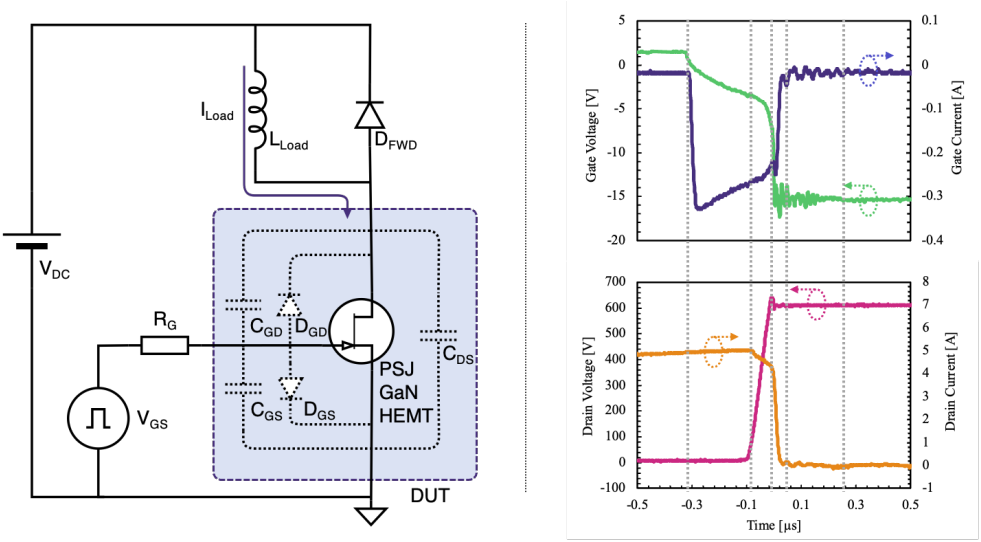


Fig. 4-6. Experimental setup for evaluation of PSJ GaN HEMTs (left) and the typical turn-off switching waveforms (right).[10]

The integration is performed over the duration of turn-on and turn-off switching events. The test has been conducted under various conditions to determine the device switching behaviour.

At the end of the turn-off switching cycles, an overshoot voltage transient occurs due to the presence of various parasitic inductances as given by Eq. (4-3).

$$V_{\text{overshoot}} = L_{\text{stray}} \cdot \frac{dI_{\text{Drain}}}{dt} \qquad (4\text{-}3)$$

It is essential to reduce parasitic inductances to avoid large overshoot voltage, which can be detrimental to the device.

4.3.2 Influence of gate drive on turn-off dV/dt

Depending on the application, the dV/dt may need to be limited, especially during turn-off cycles. As the device turns off, a large overshoot transient develops across the drain-source

[10] Published in (3).

terminals under high-speed switching operation due to the presence of stray inductances. This overshoot voltage can be detrimental to the device or the load if the maximum ratings are exceeded. For example, in motor drive applications, fast switching edges can lead to degradation of winding insulation, induce detrimental bearing current, and premature failure, which limits the useful lifespan [78] [79] [80] [81] [82]. GaN HEMTs offer high speed switching and commercial devices do not show slew rates below 20 kV μs^{-1} [83], which limits their scope of application.

In conventional devices, the slew rate may be set by the selection of an appropriate external gate resistor. To determine the controllability of the PSJ GaN HEMTs, turn-off switching characteristics were obtained at a voltage of 600 V and current of 5 A, utilising different gate voltages and resistances at RT as shown in Fig. 4-7.

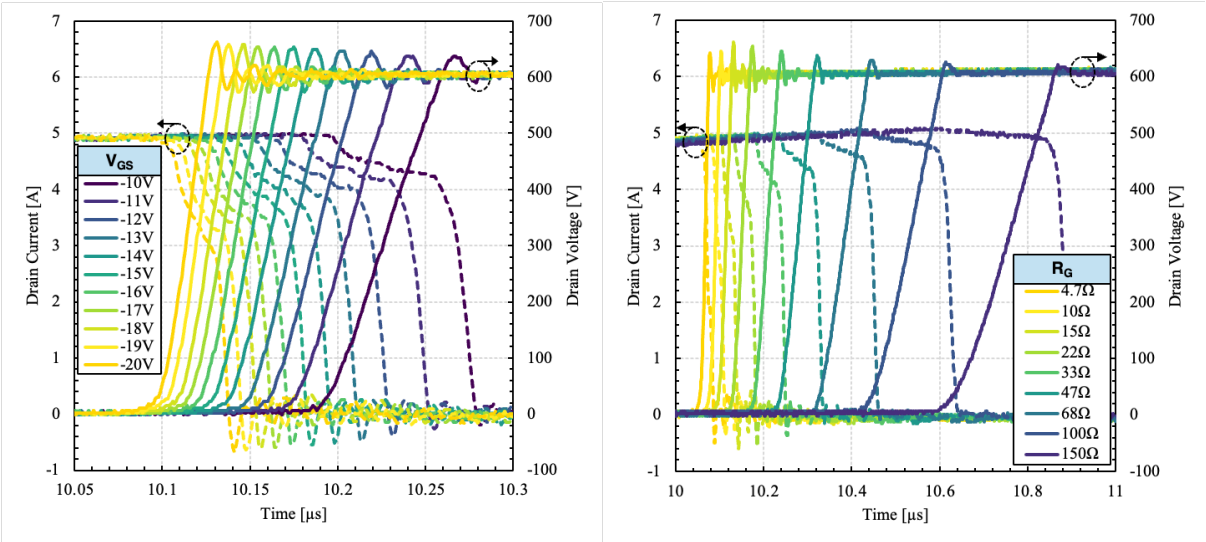


Fig. 4-7. Turn-off switching waveforms of the 1.2 kV PSJ GaN HEMT at different gate voltages and R_G = 22 Ω (left) and at different gate resistances and V_{GS} = -15 V (right). $V_{GS\text{-}ON}$ = +2 V and T = 25°C.[11]

[11] Published in (3).

It is evident that with an increase in negative gate voltage the slew rate changes. Similarly, at lower gate resistances faster switching transitions can be observed. This is because gate voltage and gate resistance control the gate current and therefore the rate at which the gate capacitances are charged/discharged. High gate resistance values limit the gate current, resulting in a slower switching slew rate. Also, it can be observed that at low gate resistances (R_G < 10 Ω), the overshoot decreases despite faster dV/dt. This can be attributed to the ringing that leads to a large transient leakage current that coincides with the overshoot period resulting in the peak voltage to be suppressed. The corresponding turn-off dV/dt and rise time along with the dissipated energy are provided in Fig. 4-8.

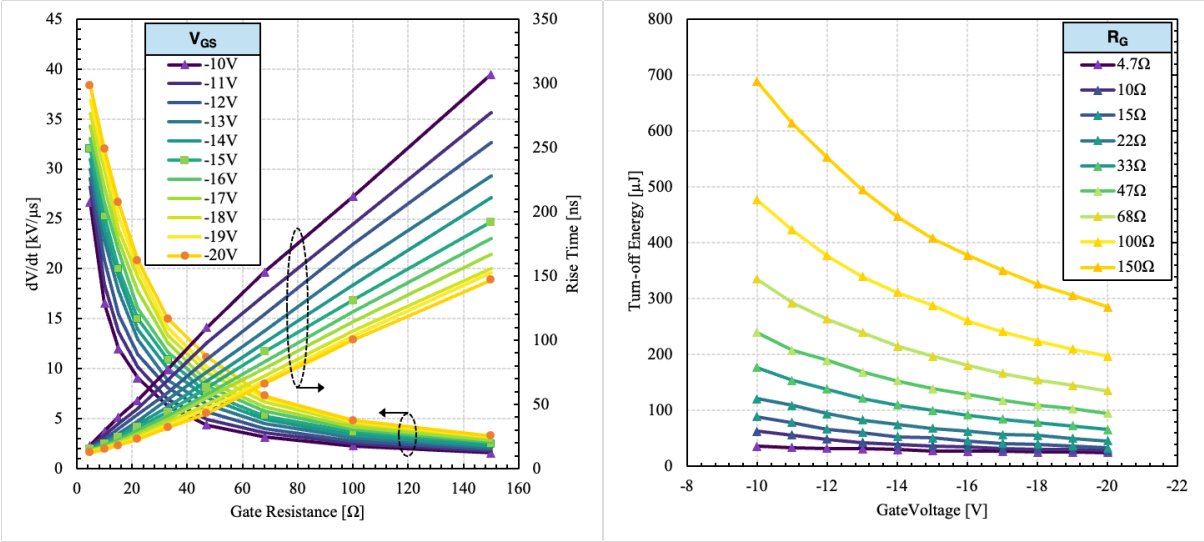


Fig. 4-8. Measured turn-off dV/dt and rise time (left) of the 1.2 kV PSJ GaN HEMT and the corresponding turn-off energy at different gate voltages and gate resistances (right). T_{amb} = 25˚C, V_{DS} = 600 V, and I_D = 5 A.[12]

The maximum attainable dV/dt is approximately 40 kV μs^{-1} at a gate resistance of 4.7 Ω. This value can be reduced to as low as 1 kV μs^{-1} by increasing gate resistance to 150 Ω.

[12] Published in (3).

However, as expected, the turn-off switching energy increases at higher gate resistance because of longer switching transitions.

4.3.3 Influence of voltage and current on turn-off dV/dt

To fully understand the turn-off dV/dt mechanism, the effect of supply voltage and switching current has also been investigated. Therefore, the experiment was performed at different drain voltages and currents varied from 100 V to 800 V and 1 A to 8 A, respectively, as shown in Fig. 4-9. The gate drive voltage is set to -15 V / +2 V, and the gate resistance is 22 Ω for this experiment.

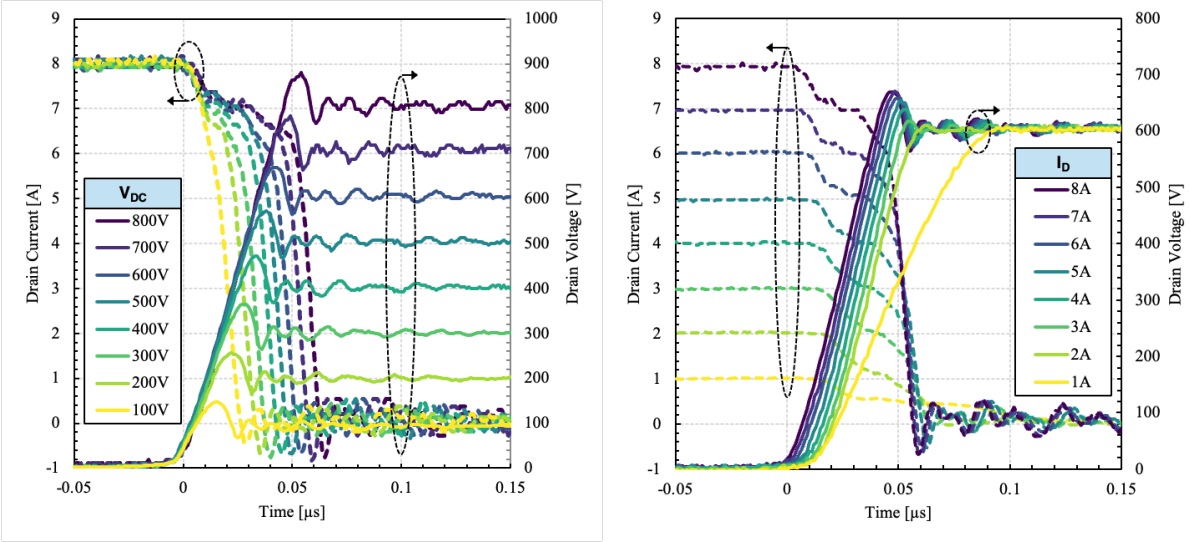


Fig. 4-9. Turn-off switching waveforms of the 1.2 kV PSJ GaN HEMT at various drain voltages (left) and currents (right). R_G = 22 Ω, V_{GS} = +2 V / -15 V, T_{amb} = 25°C.[13]

The impact of variations in switching voltage and current on slew rate and dissipated energy is presented in Fig. 4-10. The magnitude of the electric field directly impacts the turn-off and therefore dV/dt increases with the voltage.

[13]Published in (3).

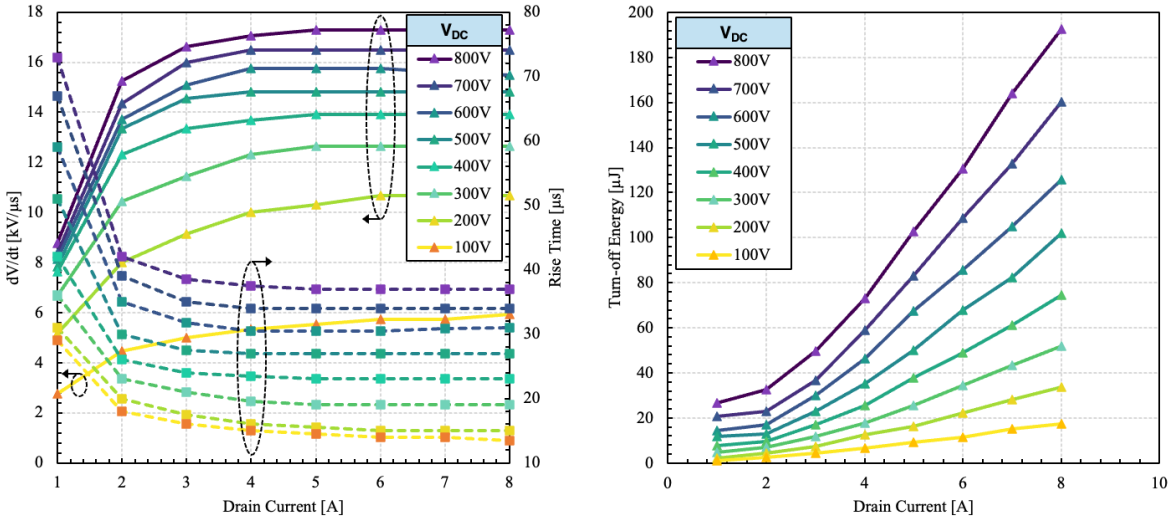


Fig. 4-10. Measured turn-off dV/dt, rise time (left) and turn-off energy (right) of the 1.2 kV PSJ GaN HEMT as a function of load current and switching voltage.[14]

The dV/dt initially increases with the load current and eventually levels off. This is due to the impact of parasitic capacitances present in the measurement setup and the device. At low current values, these capacitances are charged at a slower rate which limits the slew rate. The effect of supply voltage on slew rate diminishes as the voltage increases.

The dissipated energy rises due to the higher voltage and current levels switched by the device. However, the dissipated power is lower by an order of magnitude than those observed in Si devices.

4.3.4 Impact of gate drive on turn-on characteristics

Fig. 4-11 illustrates the impact of positive gate voltage and gate resistance on turn-on switching waveforms.

[14] Published in (3).

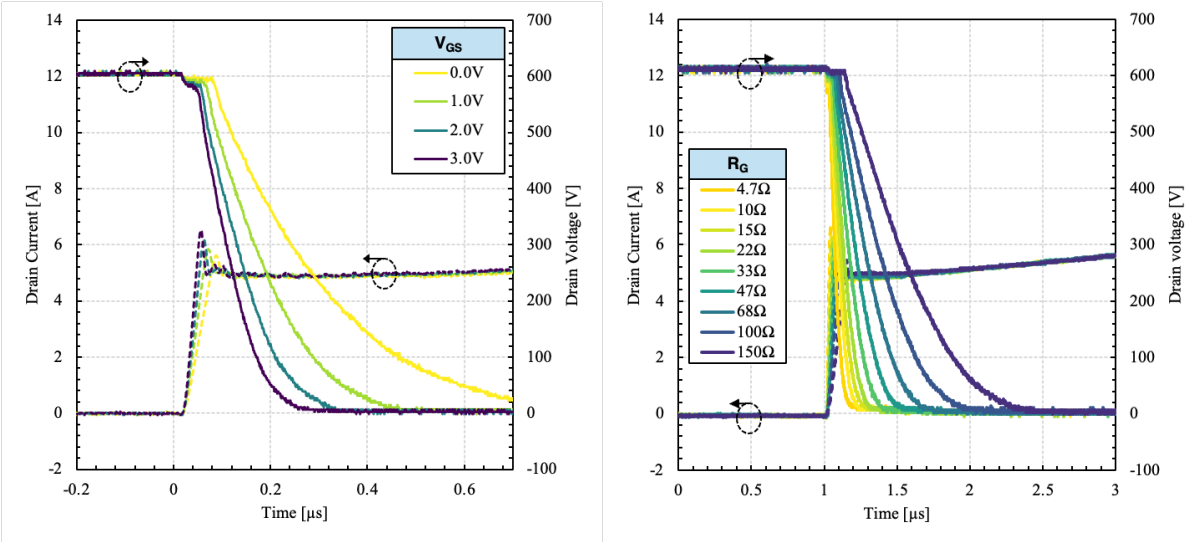


Fig. 4-11. Turn-on switching waveforms of the 1.2 kV PSJ GaN HEMT as a function of different gate voltages at $R_G = 22\ \Omega$ (left) and gate resistances at $V_{GS} = 2$ V (right). $T_{amb} = 25^{\circ}C$ and $V_{GS(OFF)} = -15$ V.

Application of a positive gate voltage can accelerate the turn-on process leading to reduced turn-on losses. This is because the gate capacitance can be charged at a faster rate. Meanwhile, the slew rate can be adjusted through variation of gate resistance R_G. The minimum fall time corresponds to 60 ns contributing to 119 µJ.

4.3.5 Influence of temperature on switching

Power semiconductor devices often are required to operate under higher ambient temperature conditions. Thus, it is essential to understand the influence of temperature on switching performance. The high temperature switching characteristics of the PSJ GaN HEMT were evaluated at 1000 V drain voltage and 5 A as presented in Fig. 4-12. This test has been performed using a 3 kV PSJ GaN HEMT. It is evident that the temperature has a negligible effect on turn-off as the waveforms remain unaffected. The turn-on slows down as the temperature rises which can be attributed to the reduced transconductance at higher temperatures previously shown in Fig. 4-3.

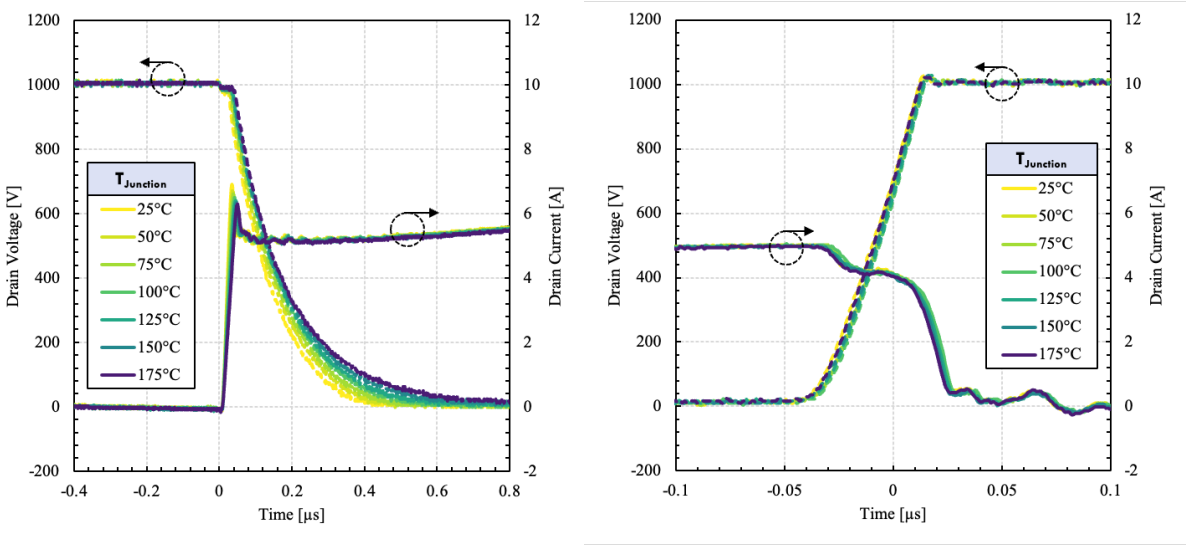


Fig. 4-12. Measured turn-on (left) and turn-off (right) switching transitions of the 3 kV PSJ GaN HEMT at different junction temperatures. R_G = 15 Ω and V_{GS} = +2/-15 V.[15]

The corresponding rise time and fall time as well as dissipated switching energy were obtained from the measured switching waveforms as presented in Fig. 4-13.

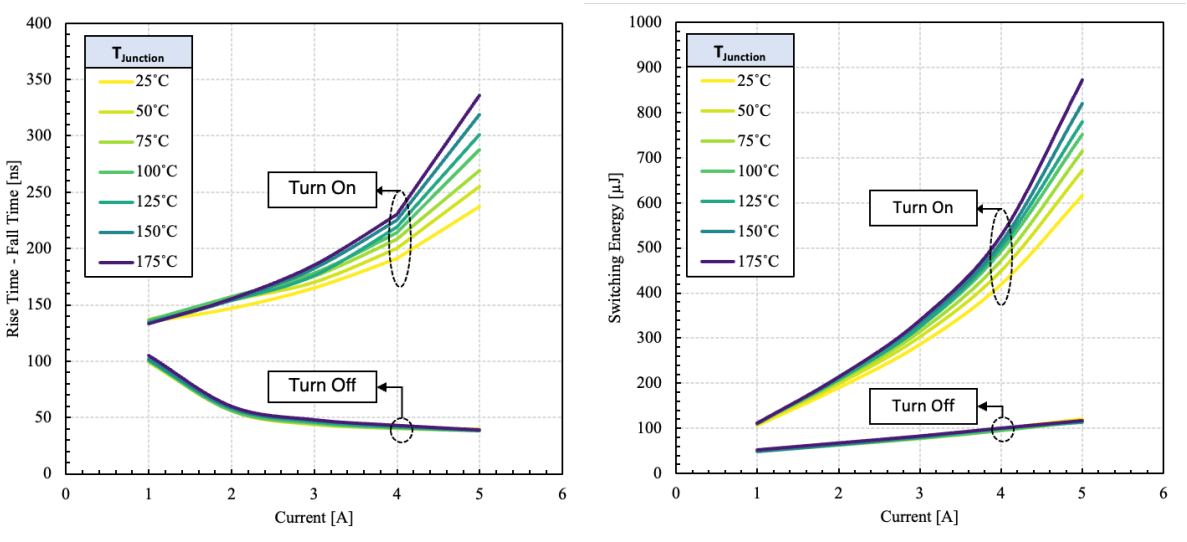


Fig. 4-13. Switching transition time (left) and dissipated switching energy (right) of the 3 kV PSJ GaN HEMT as a function of load current at different junction temperatures.[15]

[15] Published in (5).

The turn-off energy remains unaffected by the junction temperature and rises with the load current. The turn-on energy is higher due to a longer transition time and a slower turn-on dV/dt at higher temperatures. This behaviour can be attributed to the reduced transcendence at elevated temperatures.

4.3.6 Influence of the drift region length

To understand the effect of the drift region on device performance, two devices with different nominal breakdown voltages of 1.2 kV and 3.0 kV were analysed [84] [85]. The respective devices have a drift region length of 20 µm and 40 µm. Both devices share an identical die size. The on-state resistance was observed to be doubled for the 3.0 kV device which is due to the longer channel length that is twice as large compared to the 1.2 kV device. It should be noted that the absolute breakdown voltage of both devices is much higher than the specified breakdown voltage. The switching performance is observed to be comparable because of the similar capacitance characteristics. It is worth noting that while the drift region is doubled, the total gate drain capacitance is maintained at a similar level because of a larger spacing between drain and source terminals (fingers).

4.4 Unclamped Inductive Switching

Power devices are often used in circuits that require switching of inductive loads, that can lead to the development of surge voltage across the devices. Therefore, an in-depth understanding of the device performance in such conditions is critical. In this section, the unclamped inductive switching (UIS) capability and mechanism of PSJ GaN HEMTs will be investigated experimentally.

4.4.1 UIS Experimental Setup

The experimental configuration designed to evaluate the UIS capability is shown in Fig. 4-14.

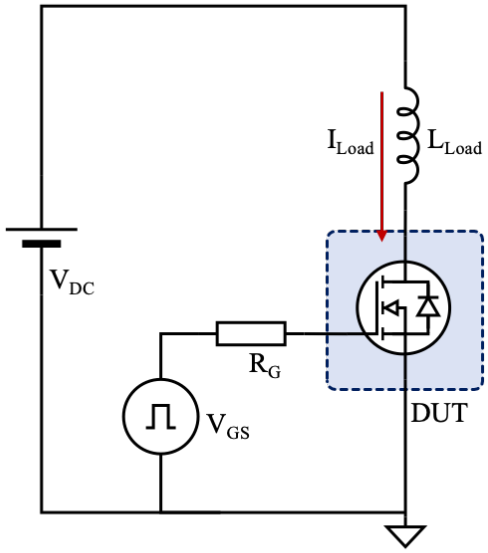


Fig. 4-14. Unclamped inductive switching test setup.

This setup is similar to the previously presented circuit in Fig. 3-13 without the freewheeling diode. A 440 µH inductor is connected in series with the DUT. The DC resistance (DCR) of the inductor is about 90 mΩ. The gate driver provides +2 V for the turn-on and -15 V for the turn-off. The UIS energy (E_{AV}) applied to the DUT is proportional to the stored energy in the load inductor as given by Eq. (4-4).

$$E_{\mathrm{AV}} = \frac{1}{2}.L.I^2 \qquad (4\text{-}4)$$

where L is the inductor value, and I is the inductor current.

4.4.2 UIS capability in PSJ GaN HEMTs

The DUT was subject to UIS at different pulse widths until failure. The UIS waveforms before and after the failure are presented in Fig. 4-15.

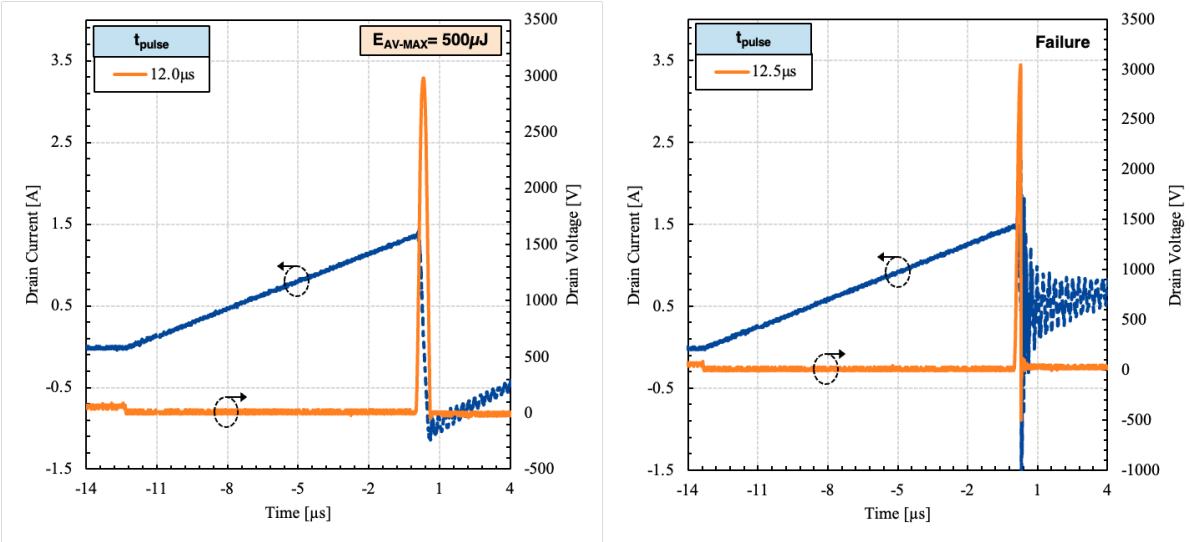


Fig. 4-15. UIS waveforms of the 1.2 kV PSJ GaN HEMT before and after failure. $R_G = 51\ \Omega$, $T_{amb} = 25°C$.[16]

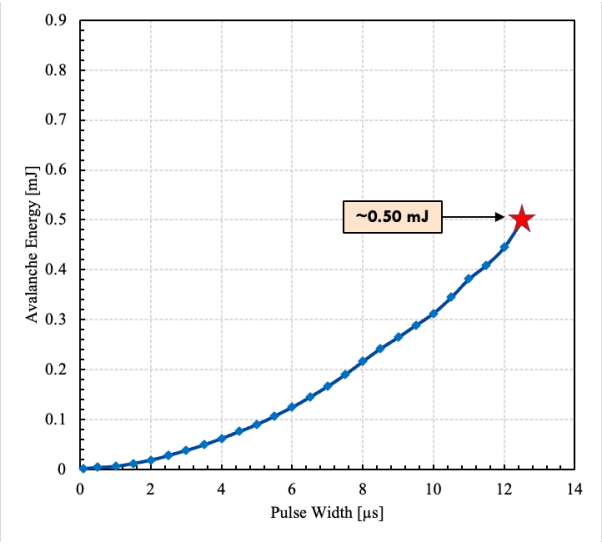


Fig. 4-16. Measured UIS energy of the 1.2 kV PSJ GaN HEMT as a function of the pulse width. $T_{amb} = 25°C$.

The device eventually failed at a surge voltage of 3.1 kV and a pulse width of 12.5 µs. A negative current flow is visible due to the capacitive response of the device under the UIS

[16] Published in (5).

condition. Similar to conventional GaN HEMTs, the device fails as the drain voltage exceeds the breakdown.

The absorbed energy due to the UIS is about 0.5 mJ in the last pulse before failure which is primarily related to the absorbed energy by the device's capacitance.

4.5 Dynamic On-State Resistance

As mentioned previously, GaN HEMTs are susceptible to dynamic characteristics. The magnitude of the on-resistance can rise depending on the applied voltage. In PSJ GaN devices, the electric field is inherently uniform under off-state conditions and electric field peaks are suppressed. The dynamic on-resistance performance of a 1.2 kV PSJ GaN HEMT is illustrated in Fig. 4-17.

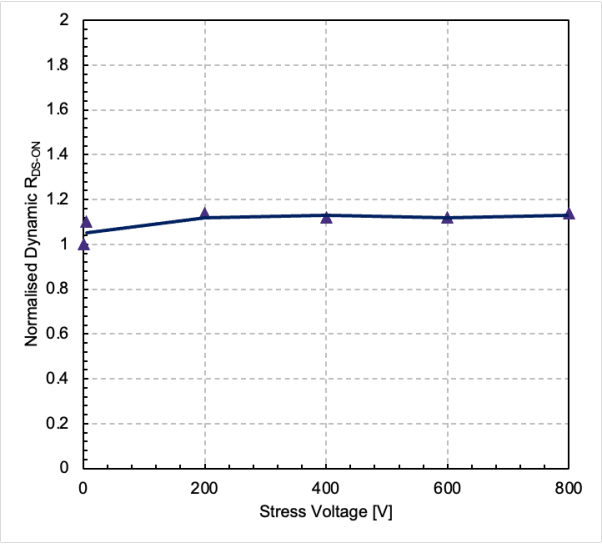


Fig. 4-17. Normalised dynamic on-state resistance of the 1.2 kV PSJ GaN HEMT. The stress time is 10 s and the on-time is 5 µs. [85]

It is evident that the on-state resistance does not change significantly with the applied voltage confirming the effectiveness of the PSJ technology to suppress the dynamic on-resistance behaviour.

4.6 Chapter Conclusion

In this chapter, the operating physics, characteristics, and switching performance of large area PSJ GaN HEMTs have been presented and analysed. Based on the results, PSJ GaN HEMTs exhibit highly versatile performance which makes them suitable for a wide range of applications. The device can operate at a wide range of slew rates which can be set by intelligent control of the gate driver to fulfil various application requirements while maintaining a low power loss profile. At high operating temperatures, the turn-on shows a small increase in switching time. Meanwhile, the turn-off virtually is not affected by the temperature. In terms of UIS capability, the device mostly absorbs the energy in capacitive form. The device achieves an avalanche breakdown of over 3.1 kV with the drift region of 20 μm. However, the normally-on nature of GaN HEMTs is not desirable from a power electronic application standpoint. Normally-off approaches are necessary for a wider scale adaptation of the technology. Overall, PSJ GaN HEMTs have been shown to be an exceptional choice for high voltage, high power density requirements.

Chapter 5

Cascode GaN FETs

The normally-on characteristic of GaN HEMTs is one of the major hurdles obstructing their widespread applications in power electronic systems. It is highly preferable to have a switch that fails safe when the gate drive is lost. As mentioned in Chapter 2, various methods exist to alter the threshold voltage into the positive regime to obtain enhancement mode of operation. Similarly, the 'normally-off' mode of operation can be realised by external circuit configuration. In this chapter, normally-off configuration of GaN HEMTs based on cascode and direct drive are discussed. A cascode GaN FET based on the PSJ GaN HEMT will be presented. The cascode GaN FET is evaluated through experimental measurements of its performance. Also, a power loss analysis is presented for converter applications based on cascode technologies.

5.1 Direct Drive and Cascode GaN HEMTs

Normally-off behaviour can be achieved by using hybrid configurations of d-mode GaN HEMTs placed in series with e-mode MOSFETs. There are two approaches that result in normally-off switches that are known as cascode and direct drive as shown in Fig. 5-1. In both

configurations, the voltage is supported by the high voltage d-mode GaN switch which protects the low voltage MOSFET from destruction.

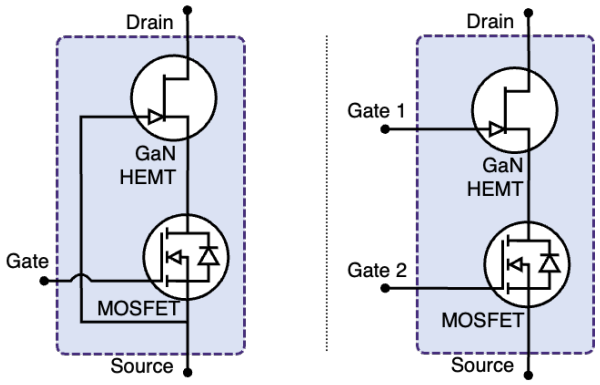


Fig. 5-1. Cascode (left) and direct-drive (right) configurations.

Each configuration has its own benefits. Cascode offers a standard MOS gate, which makes the device compatible with widely available drivers used for conventional MOSFETs. However, the key limitation is that the gate of the HEMT cannot be controlled directly and therefore the switching cannot be optimised. Direct drive, on the other hand, offers the same level of control similar to standalone d-mode HEMTs as the gate is directly controlled by the driver. In the direct drive arrangement, under normal operating conditions, the MOSFET is merely a small series resistance and does not affect the device performance. The downside of the direct drive approach is the special gate driver requirements. For this reason, currently available direct drive GaN switches are offered as GaN power ICs which integrate the gate drive and other functionalities within the same package [86].

5.1.1 Gate drive and working mechanism

Cascode and direct drive configurations emulate normally-off in different ways. The cascode gate drive requirement is MOS compatible and therefore many gate driver choices are

available. Direct drive GaN FETs require a more complex gate drive. The basic gate drive strategy for each configuration is shown in Fig. 5-2.

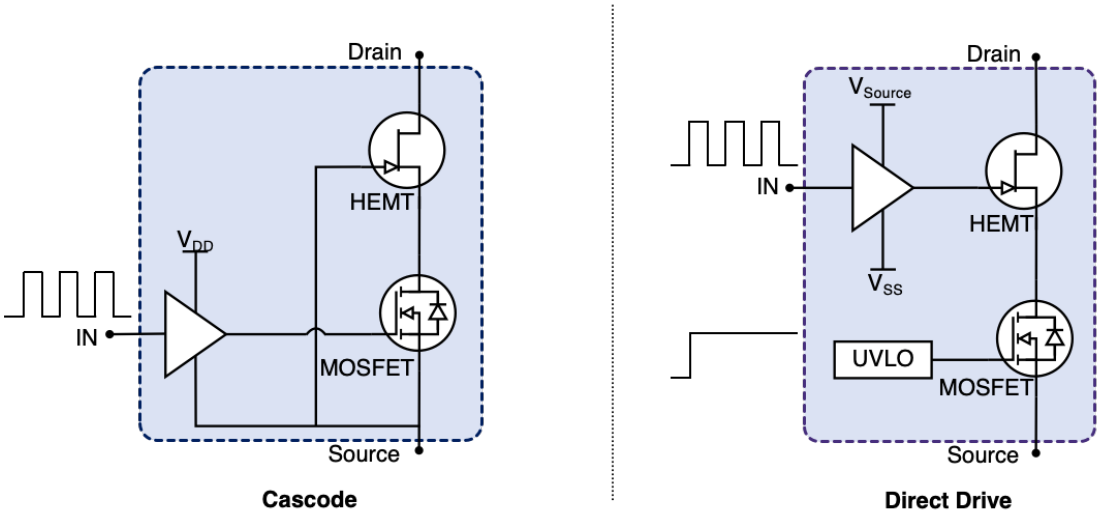


Fig. 5-2. Basic gate drive circuits for direct drive and cascode configurations.

In the cascode configuration, a positive gate potential above the threshold of the MOSFET results in the gate of the d-mode HEMT to be shorted to its source which leads to the device turn-on. The turn-off occurs when the gate bias is removed, and the gate-source potential becomes zero (V_{GS} = 0 V). Once the voltage of the MOSFET's drain surpasses the threshold of the HEMT, both devices are turned off. The cascode exhibits a larger combined capacitance during the switching cycles as the combined gate-source capacitance of the HEMT and output capacitance of the MOSFET should be charged and discharged to switch the device. Since the gate of the HEMT is linked to the source of the MOSFET, no dV/dt controllability can be achieved through external gate control [87]. Under off-state conditions, the voltage distribution can lead to an avalanche of the MOSFET [88]. This can happen because the output capacitance of the HEMT and MOSFET are in series connection that forms a capacitive voltage divider. To mitigate this issue, a capacitor or resistor can be placed in parallel with the LV MOSFET.

The direct drive configuration requires a negative drive voltage (V_{SS}) to turn off the d-mode HEMT. The MOSFET is always-on and driven via the under-voltage lockout (UVLO) circuit and has no impact on the switching performance. In case of power failure, the UVLO is triggered which disables the LV MOSFET and turns it off. Once the MOSFET is turned off, the drain potential rises which emulates a negative gate bias for the GaN HEMT.

Each device permits reverse current flow in a different way. The cascode permits reverse current flow through the LV MOSFET body diode when the V_{GS} is 0. The MOSFET turns on when a gate voltage higher than its threshold is applied that enables the current to pass through the channel without a diode voltage drop. Thus, in every switching cycle, a reverse recovery occurs because of the utilisation of the Si body diode. In the direct drive, the body diode is not activated as the MOSFET is always on, and therefore, no reverse recovery occurs.

5.2 Evaluation of PSJ Cascode GaN FETs

In this section, the characteristics of a cascode GaN FET comprising a 1.2 kV PSJ GaN HEMT and a 30 V Si MOSFET are presented, and the results are discussed.

5.2.1 Current voltage characteristics

The output characteristics were measured in pulse mode at different gate voltages and temperatures as presented in Fig. 5-3.

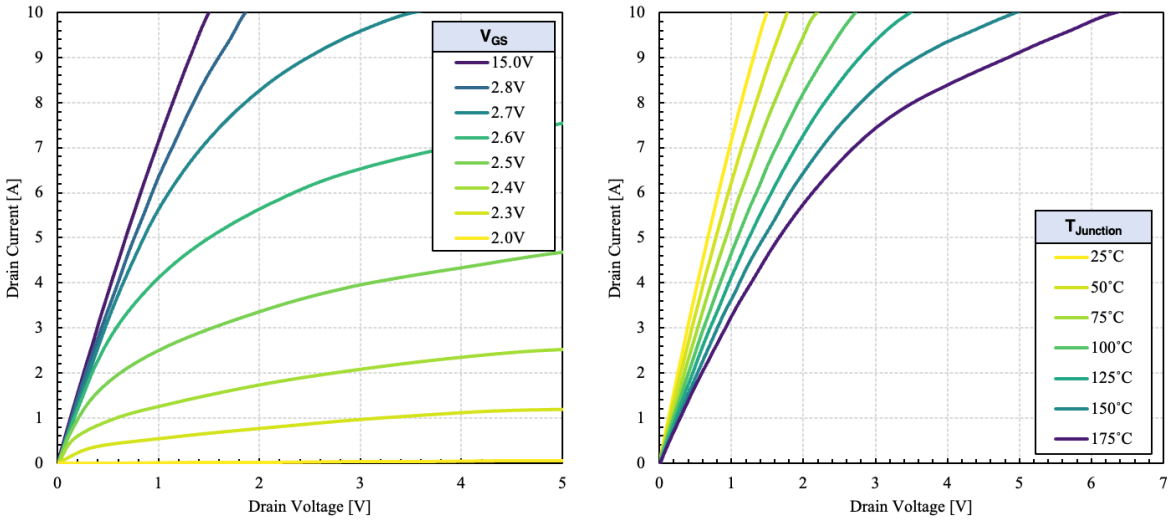


Fig. 5-3. Output characteristics of the 1.2 kV cascode PSJ GaN FET at RT (left) and at different temperatures and V_{GS} of 15 V (right).[17]

The on-state resistance of the PSJ cascode corresponds to about 125 mΩ at V_{GS} of 15 V which is similar to the d-mode device due to the negligible MOSFET on-resistance contribution of 5 mΩ. Higher gate voltages do not significantly impact the on-resistance because the major contribution is made due to the GaN HEMT. One limitation of cascode switches is that the HEMT's turn-on gate voltage is set to zero (gate and source shorted), which adversely impacts the on-resistance. In e-mode or d-mode devices, a positive gate bias can be provided to modulate the resistance of the channel. Based on the measurement, the normalised on-resistance at different temperatures as well as the transfer characteristics are illustrated in Fig. 5-4.

[17] Published in (9).

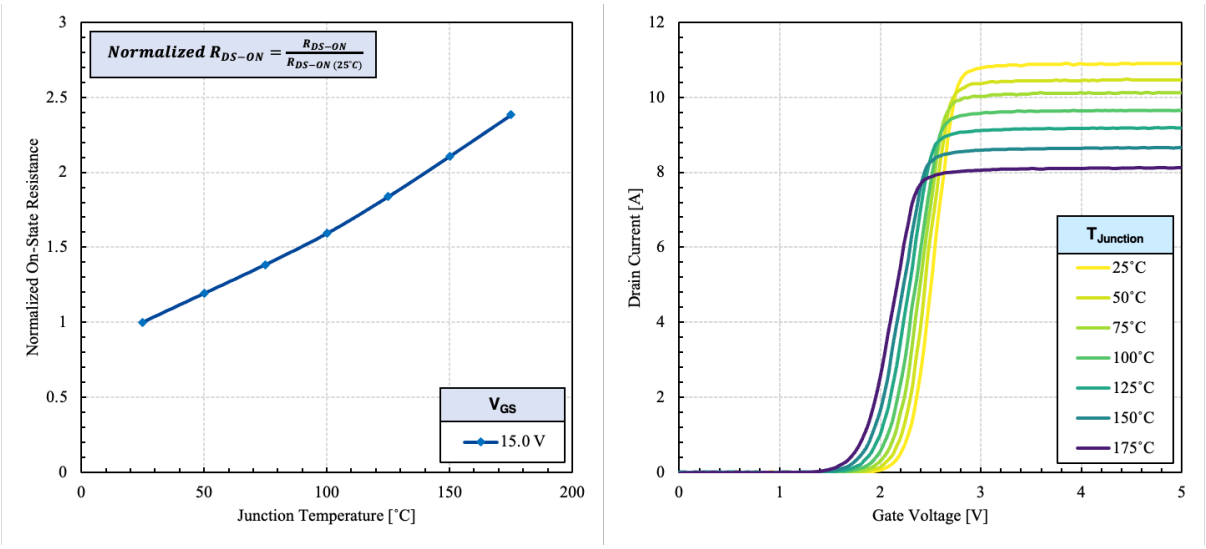


Fig. 5-4. Normalised on-resistance (left) and transfer characteristics (right) of the 1.2 kV cascode PSJ GaN FET at different junction temperatures. V_{DS} = 10 V.[18]

Both constituents of the cascode have a positive temperature coefficient of on-state resistance which is essential for thermal stability purposes.

The reverse I-V characteristics as a function of different gate voltages are shown in Fig. 5-5. In the reverse conduction mode, the cascode behaves similarly to conventional power MOSFETs. In the absence of gate bias, the current flows through the body diode of the LV MOSFET to the GaN HEMT. By applying a positive gate bias, the conduction threshold is lowered, resulting in the entire current to flow through the channel, effectively bypassing the body diode.

[18] Published in (9).

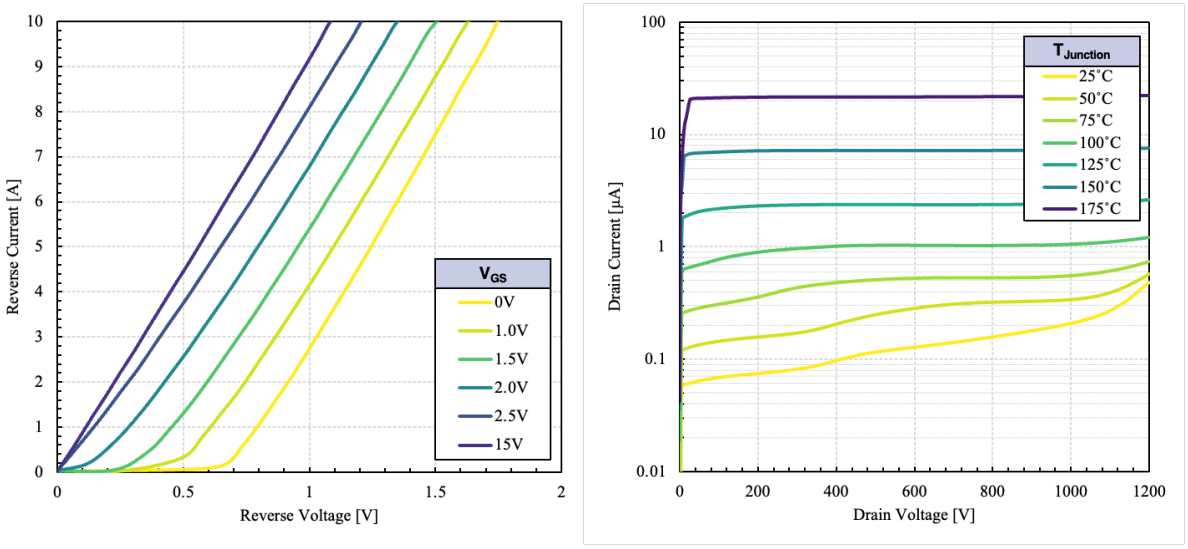


Fig. 5-5. Reverse I-V characteristics at different gate voltages and 25˚C (left) and off-state leakage current I-V characteristics at different temperatures and V_{GS} = 0 V (right) of the 1.2 kV cascode PSJ GaN FET. [19]

The off-state leakage current characteristics were measured as a function of different temperatures at a gate-source voltage of 0 V, as shown in Fig. 5-5. The device exhibits a very small leakage current of less than 0.5 µA at 25˚C which increases to 20 µA at 175˚C. It is important for the GaN HEMT to have low leakage current to prevent the avalanche breakdown of the low voltage MOSFET under switching conditions.

5.2.2 Capacitance characteristics

The measured capacitance characteristics of the 1.2 kV PSJ GaN FET are presented in Fig. 5-6.

[19] Published in (9).

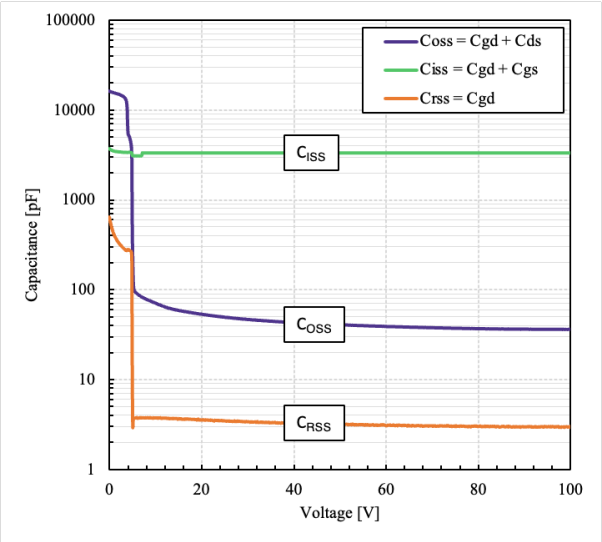


Fig. 5-6. Capacitance versus voltage characteristics of the 1.2 kV PSJ GaN FET. Freq = 100 kHz, V_{GS} = 0 V, T_{amb} = 25˚C.

The capacitance curves of C_{OSS} and C_{RSS} show a sharp fall at drain voltage of about 5 V. This corresponds to the internal threshold voltage of the GaN HEMT. The gate drain capacitance of the device appears to be lower than that of its constituent HEMT. The switching characteristics, however, are determined by the internal HEMT which has a larger C_{GD} and therefore limits the speed.

5.2.3 Turn-Off dV/dt controllability

In conventional GaN HEMTs, dV/dt can be manipulated by the virtue of gate drive voltage and external gate resistance. This behaviour was also observed for d-mode PSJ GaN HEMTs, as demonstrated in Chapter 4. The influence of gate resistance on the turn-off dV/dt of the cascode PSJ GaN FET is illustrated in Fig. 5-7.

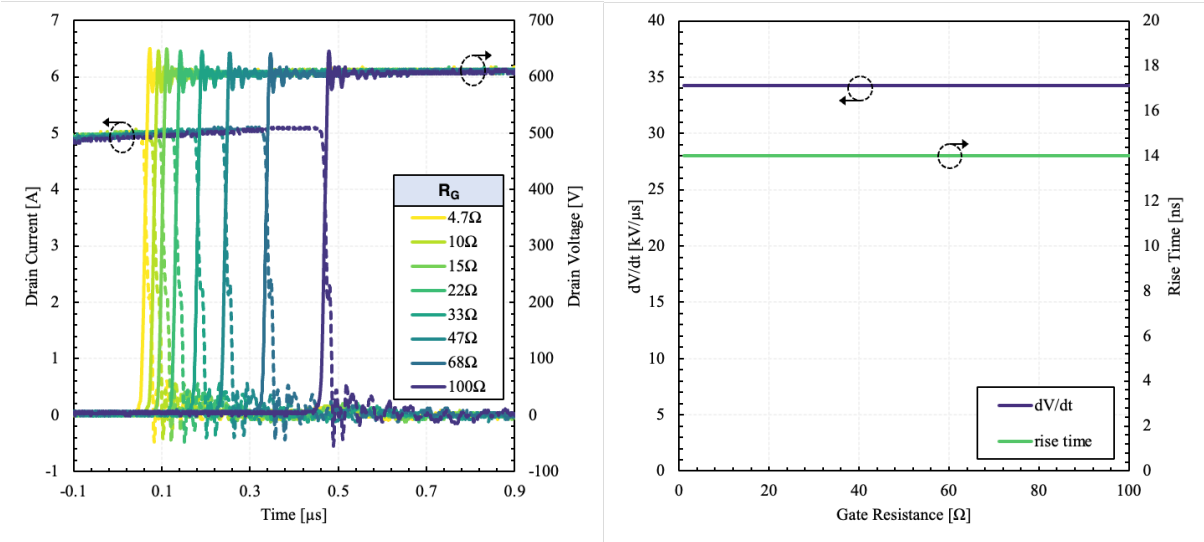


Fig. 5-7. Turn-off waveforms of the 1.2 kV cascode PSJ GaN FET at different gate resistances and corresponding dV/dt and switching time. V_{GS} = 15/0 V, T_{amb} = 25˚C.[20]

As it can be observed the dV/dt is virtually independent of gate resistor value. This behaviour is undesirable where slower dV/dt values are required to meet the requirements or dampen oscillations due to parasitic elements. In order to control the slew rate, external measures need to be implemented such as a snubber circuit in parallel with the device or a ferrite bead to prevent oscillation on the gate. As shown in Chapter 4, the direct control of PSJ GaN HEMT permits a wide range of dV/dt.

5.2.4 Switching Characteristics

The switching waveforms of the cascode PSJ GaN FET were obtained at different load currents and 600 V via an inductive switching test (presented in the previous chapters, Fig. 3-13) and are shown in Fig. 5-8. It is important to carefully design the layout of the circuit with minimal parasitics to avoid oscillation.

[20] Published in (9).

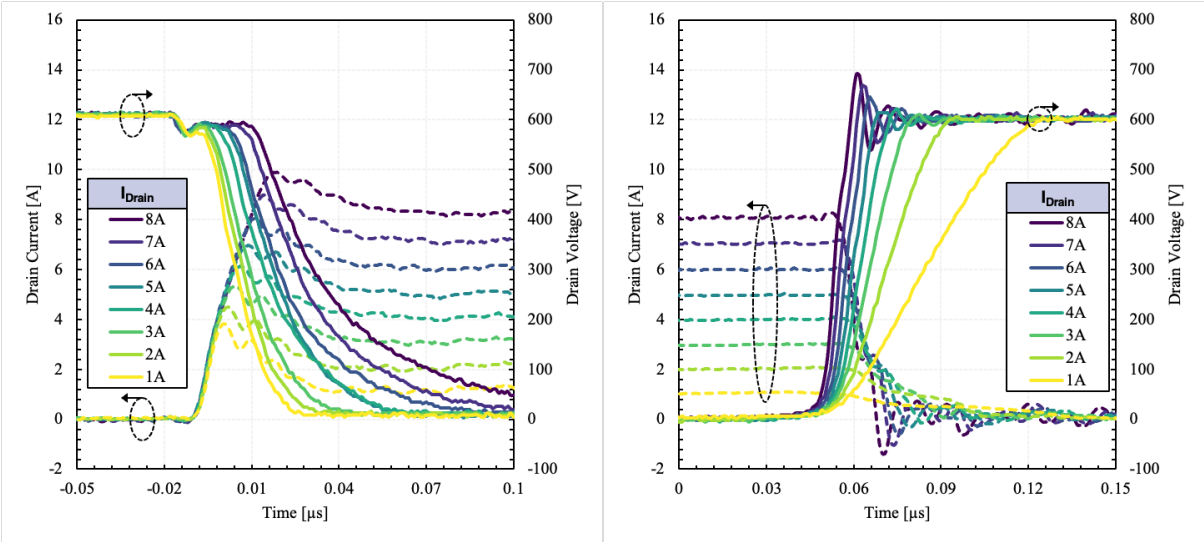


Fig. 5-8. Turn-on (left) and turn-off (right) switching waveforms of the 1.2 kV cascode PSJ GaN FET at different load currents. R_G = 22 Ω, T_{amb} = 25˚C, V_{GS} = 15/0 V.[21]

Based on the measured waveforms, the corresponding switching energy dissipated during the turn-on and the turn-off at different load currents are plotted in Fig. 5-9.

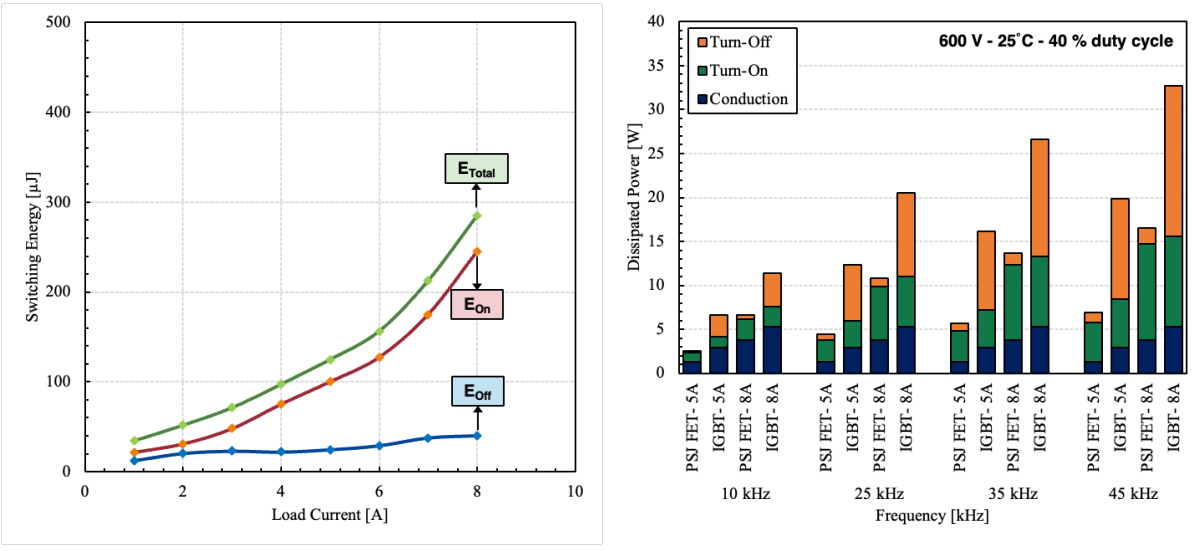


Fig. 5-9. Measured switching energy losses of the 1.2 kV PSJ cascode GaN FET at different current levels (left) and comparison of the contribution of power loss components at different load currents and frequencies (right). V_{SWT} = 600 V, $V_{GS(GaN)}$ = 15 V, $V_{GE(IGBT)}$ = 15/-5 V, R_G = 22 Ω, T_{amb} = 25˚C.

[21] Published in (9).

The contribution of power loss components in the GaN FET as a function of load current and switching frequency are also presented in Fig. 5-9. For comparison purposes, an IGBT-7 [89] with a similar rating is selected and evaluated under the same setup. The power losses in the GaN FET are significantly lower across the frequency and load current range.

5.3 Power Loss Analysis

One of the fundamental applications of power semiconductor devices is power conversion applications, which have faced a significant increase in demand for more efficient, power dense designs. Power semiconductor devices play a key role in determining these factors and therefore need to be carefully selected for optimal operation. In this section, a step-down power converter application will be discussed focusing on power loss contribution from the semiconductor switches based on the measurement presented in this chapter.

5.3.1 DC-DC step-down buck converters

Buck converters are one of the simplest, yet extensively employed in a diverse range of applications to convert an input voltage to a reduced regulated output voltage. Buck converters belong to the non-isolated converter category with two main configurations: (1) asynchronous and (2) synchronous, which are presented in Fig. 5-10 and Fig. 5-11 respectively.

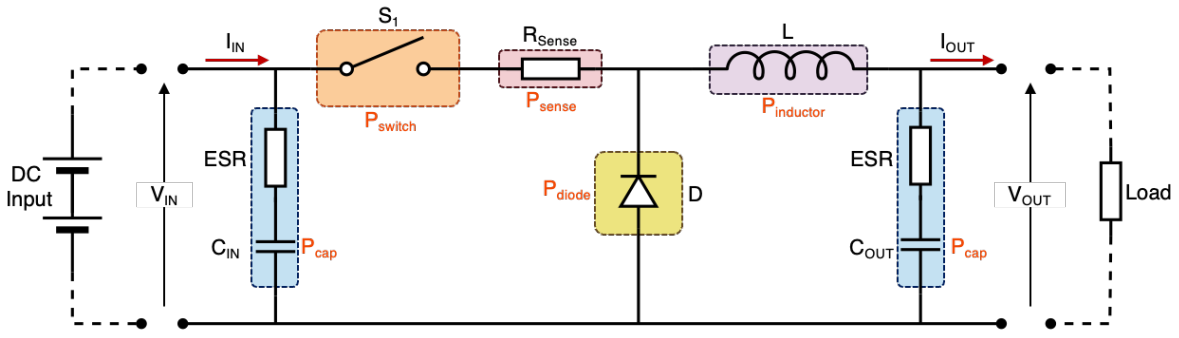


Fig. 5-10. Asynchronous buck converter circuit diagram.

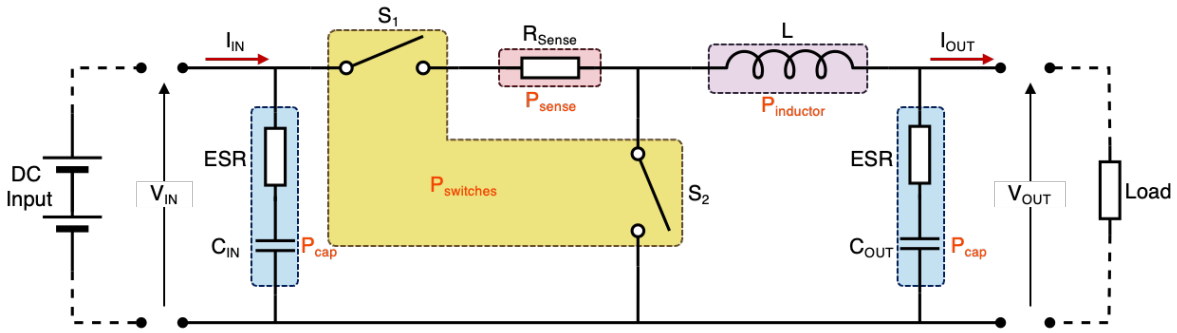


Fig. 5-11. Synchronous buck converter circuit diagram.

The basic operating theory is as follows: The primary switch (S1) operates at high frequency to chop down the DC input to create a rectangular waveform which is then fed to a low pass LC filter involving the inductor L and output capacitor C_{Out}. The low pass filter produces a DC voltage that is applied to the load, corresponding to the average voltage of the rectangular waveform at the switching node. When the primary switch is on, the diode is in reverse bias mode and the energy flow takes place from the input through the inductor to the load. Once the switch turns-off, the inductor resists the change in current, and the diode turns on to recirculate the inductor current. The key difference between the two configurations is that the diode is replaced with a synchronous switch S2 which aims to reduce the diode related losses. Typical switching waveforms of buck converters are illustrated in Fig. 5-12.

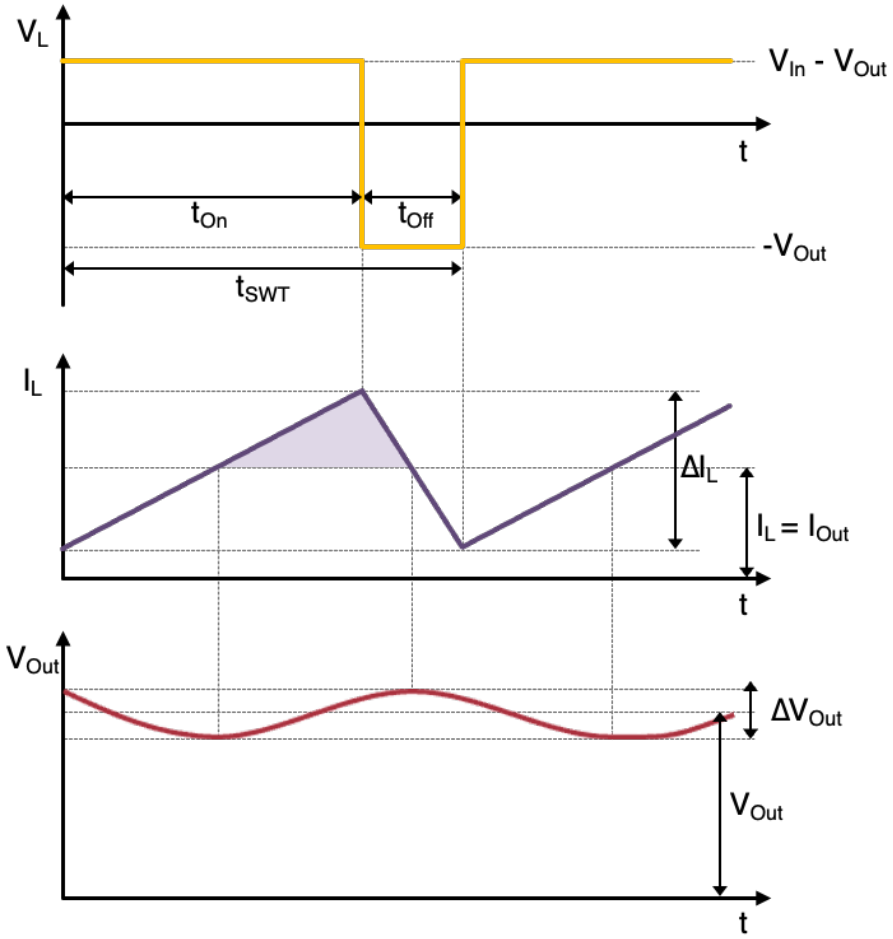


Fig. 5-12. Typical switching waveforms of a buck converter under CCM operation.

The output voltage of the converter is controlled by the product of duty cycle ($\frac{t_{\mathrm{on}}}{T}$) and the input voltage as given by Eq. (5-1).

$$V_{\mathrm{Out}} = \frac{t_{\mathrm{On}}}{T} . V_{\mathrm{In}} \qquad (5\text{-}1)$$

5.3.2 Origin of power losses

The power losses in a buck converter can be categorised as follows, assuming a steady-state operating temperature.

I. **Conduction losses** – occur due to conduction of current through a resistive medium.

II. **Switching losses** – occur due to simultaneous presence of positive voltage and current during switching cycles.

III. **Fixed losses** – design dependent.

Lower power losses can facilitate the design of more compact converters with small cooling requirements as well as contributing to lower manufacturing and operating costs. A breakdown of these losses is presented as follows:

On-state conduction loss – Power is dissipated due to the finite on-state resistance associated with semiconductor switches.

Diode conduction loss – In the synchronous mode of operation, a deadtime is necessary to prevent both high side switch and low side switch from being simultaneously on by implementing a deadtime where both switches are off. During the deadtime, the current passes through the copacked or body diode of the low side switch, generating conduction losses.

Off-state leakage current loss – Under off-state conditions, a finite current flows through the closed switch. The leakage current varies depending on design, operating conditions, and material properties of the used semiconductor device. Wide bandgap devices such as PSJ GaN FETs exhibit low leakage current particularly at elevated temperatures in the order of a few micro amperes which are essential for efficient operation. The leakage current losses can be significant at high switching voltages.

Inductor losses – Conduction losses in inductors are caused by direct current resistance (DCR) of the winding. Also, inductors exhibit power loss caused by their core magnetic properties which is classified as switching loss. These losses include hysteresis, eddy current, and residual losses.

Switching losses – Because of the simultaneous overlap of current and voltage, power is dissipated during the switching cycles. Switching losses are one of the limiting factors in achieving higher power densities.

Output capacitance loss – During switching cycles, power is dissipated due to charging the output capacitance of the switch.

Reverse recovery – a negative current runs through the device as the minority and stored charge carriers are swept out from the drift layer when the diode is switching from conduction mode to reverse bias state which results in reverse recovery losses.

Gate drive – The process of switching the MOSFETs requires their gate capacitances to be charged which leads to gate charge losses.

Input/output capacitor losses – The loss mechanism in a capacitor consists of several components including leakage current, series resistance and dielectric losses. These can be simplified by considering the equivalent series resistance (ESR).

Fixed power losses – are made up of several sources such as power consumed by various controllers, gate drivers, and protection ICs. While these losses are often small and can be ignored, in applications with limited power sources they can be significant in the long term and in idle mode.

Therefore, the efficiency (η) and the dissipated power of the converter can be derived from the ratio of the output power to the input power as given by Eq. (5-2).

$$\eta = \frac{P_{\mathrm{Out}}}{P_{\mathrm{In}}} = \frac{P_{\mathrm{Out}}}{P_{\mathrm{Out}} + P_{\mathrm{Loss}}} \qquad (5\text{-}2)$$

5.3.3 Power loss contribution of the PSJ GaN FET

To investigate the in-circuit behaviour of the device, a buck converter application is considered and simulated via SPICE. The converter consists of a cascode PSJ GaN FET as the primary switch (high side) and a SiC MPS diode as the secondary rectifier (low side). The converter is assumed to operate under continuous current mode (CCM) of operation determined by the minimum output current of 1 A.

Table 5-1. Design parameters of the step-down converter.

Parameter	Symbol	Value
Input voltage	V_{IN}	600 V
Output voltage	V_{OUT}	300 V
Minimum output current	$I_{OUT\ (MIN)}$	1 A
Frequency	f	40 kHz
Duty cycle	δ	50 %
Ripple voltage	$V_{Ripple\text{-}Max}$	1% of V_{DC}
Inductor – (Minimum)	L	1.5 mH
Capacitor – (Minimum)	C_{OUT}	42 μF

Based on the design parameters listed in Table 5-1, a buck converter circuit as presented in Fig. 5-13 was simulated in SPICE.

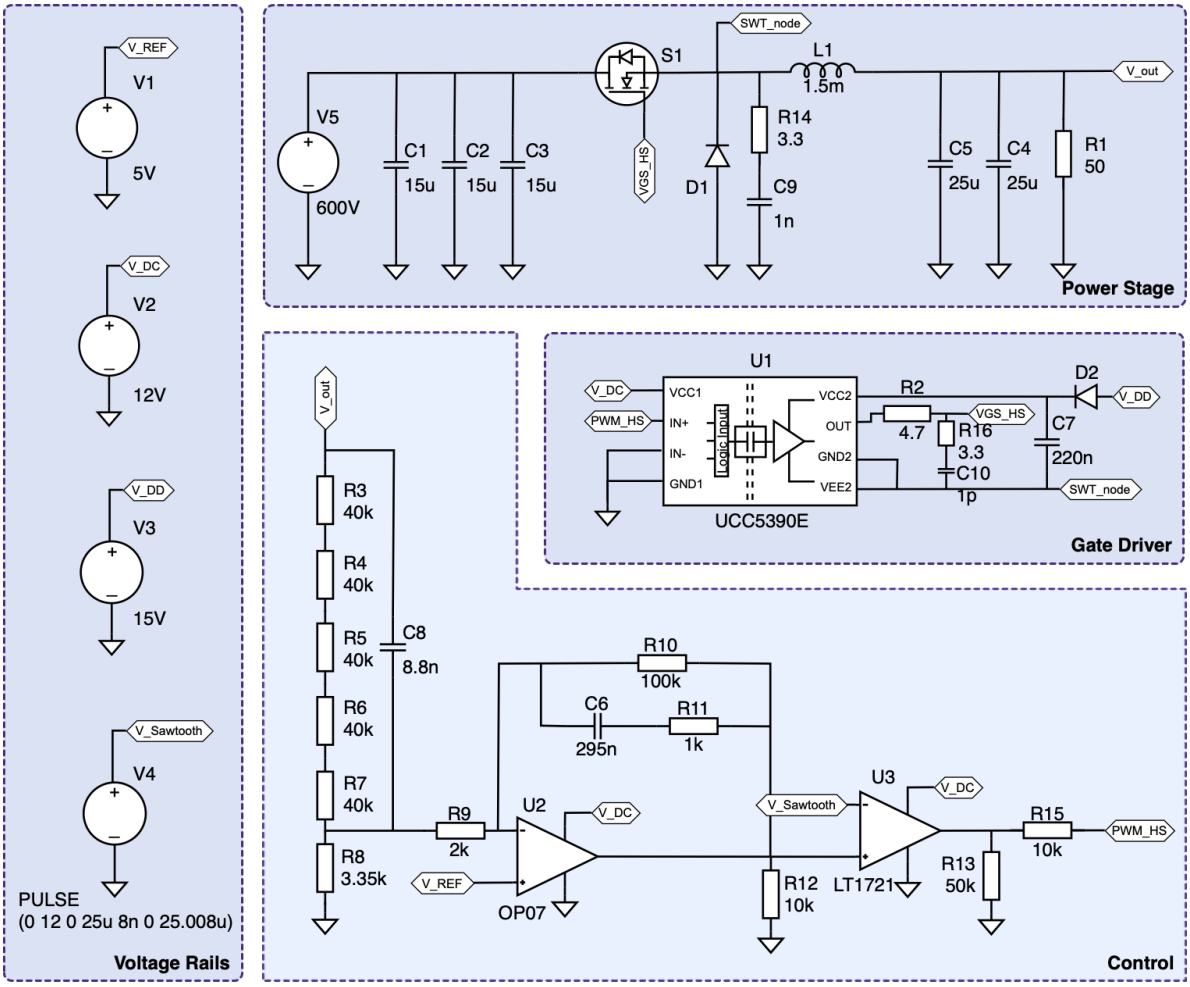


Fig. 5-13. Circuit diagram of the buck converter in SPICE.

The converter employs a closed-loop control mechanism that regulates the output voltage under different load conditions. This is accomplished by comparing the reduced output voltage to a reference voltage of 5 V by the op amp (U2). Consequently, an error signal is generated which indicates the difference between the output voltage and the target voltage. The signal is then fed to the comparator (U3) which produces a pulse width modulated (PWM) signal. The output of the comparator is connected to an isolated gate driver (U1) providing the required gate voltage to drive the power device. To prevent overshoot during the circuit power-up a soft start mechanism is implemented by adding a capacitor (C8) in the feedback loop. To meet the

required specifications, an inductor of 1.5 mH with 2 mΩ direct current resistance is selected. For the input capacitor three 15 µF capacitors (C4AQJBU5150M12J – [90]) are employed and for the output capacitor two 25 µF capacitors (C4AQGBU5250P12K – [91]) are selected. To achieve good simulation, a SPICE model was developed for the cascode GaN FET which is detailed in the Appendix B. The simulation was performed for the cascode GaN FET and compared with the 1.2 kV IGBT-7 [89] of similar power ratings. The converter waveforms and efficiency performance using the devices were extracted at different load conditions and are presented in Fig. 5-14.

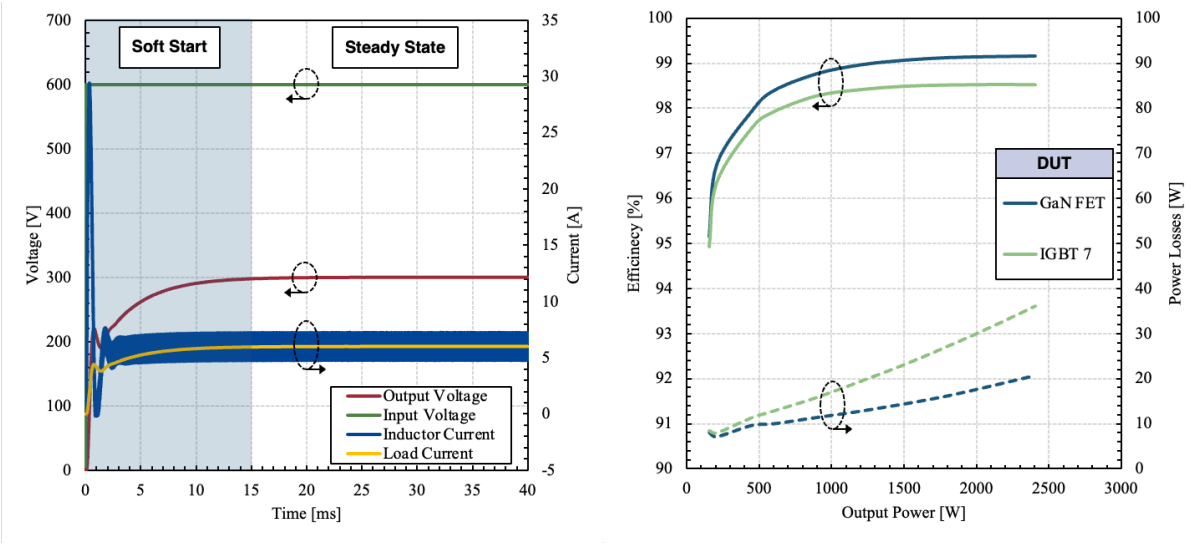


Fig. 5-14. Simulated converter waveforms at a load current of 6 A (left) and efficiency and power losses as a function of the output power (right).

The efficiency and power losses are assessed under steady state conditions. Based on the results, the converter employing the GaN FET delivers a high efficiency of about 98.8% at 1 kW output power. Meanwhile, the IGBT based approach results in a lower efficiency which is attributed to high switching losses. It is clear that the GaN FET is suitable for higher frequency and higher power density operation.

5.4 Chapter Conclusion

This chapter has presented a comprehensive evaluation of 1.2 kV PSJ cascode GaN FETs for the first time. Cascode configuration simplifies the gate drive design allowing the use of standard MOS compatible gate drivers. However, the ease of gate drive comes at the expense of controllability and flexibility. Therefore, cascode devices are well-suited for applications where the design does not require precise gate control. However, if it is required, the switching can still be controlled by additional external circuits and snubbers. On the other hand, direct drive can offer superior flexibility which can be suitable for a wider spectrum of applications. Future works need to be done to develop dedicated gate drivers for direct drive to simplify their applications. Additionally, it has been demonstrated that high conversion efficiency can be achieved by utilising PSJ GaN devices.

Chapter 6

Hybrid Power Switches Using IGBT

Hybrid power switches (HPS) integrate the advantages of bipolar and unipolar devices. One of the earliest demonstrations of the hybrid power switch concept was introduced in 1983 [92]. The concept originally was based upon the combination of a FET and a bipolar junction transistor (BJT) in order to optimise switching efficiency, current handling capability, and to simplify gate drive design [93]. Since then, BJTs have been superseded by superior performance IGBTs. Modern hybrid power switches aim to integrate the advantages of Si IGBT and SiC FET technologies to offer optimal switching performance under a diverse set of operating conditions. To this date, several hybrid device configurations have been reported in the literature [7] [94] [95] [96] [97] [98] [99] [100] [101]. Despite previous studies highlighting the advantages that HPS can offer, the impacts of gate drive mechanisms and strategies have not been fully explored. Therefore, in this chapter, a HPS based on the latest Si IGBT and SiC MOSFET technologies is presented to further gain insight into the working mechanisms of the device. The device is evaluated through experimental measurements of its static and dynamic characteristics. The effect of gate driver on device optimisation is also investigated.

6.1 Structure and Working Mechanism

The HPS presented in this chapter consists of a Si IGBT (IGBT7 – IKW50N120CS7 – Infineon [102]) and a SiC MOSFET (CoolSiC – IMW120R030M1H – Infineon [103]) in parallel arrangement as depicted in Fig. 6-1. The devices were decapsulated to measure the device area by mechanical means. The measured chip area of Si and SiC is about 35 m^2 and 11.8 m^2, respectively, which results in a ratio of 3:1 (excluding the diode).

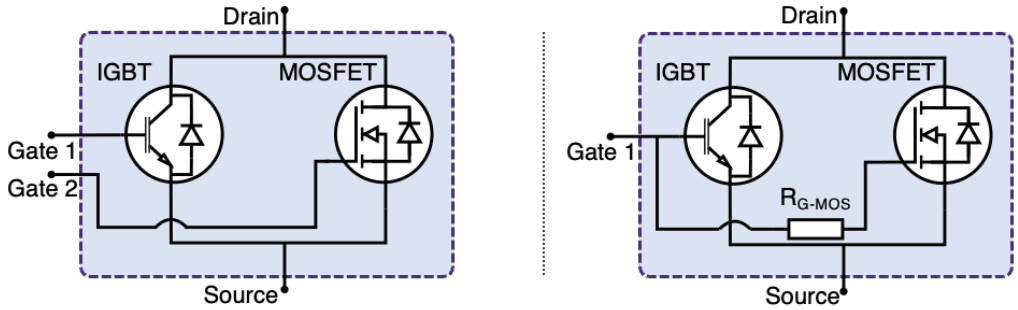


Fig. 6-1. Schematic of the HPS dual gate (left) and single gate (right) configurations.

The HPS can be configured as a three-terminal (single gate) or a four-terminal (dual gate) device depending on the mission profile. The single gate configuration aims to offer improved characteristics with simple gate drive requirements compatible with existing standalone modules. However, IGBTs and MOSFETs exhibit different switching characteristics. IGBTs generally have longer switching delay and transition time due to their inherent bipolar nature. In parallel operation, this behaviour leads to the IGBT turning off after the MOSFET. To mitigate the switching time mismatches and to fully optimise the device, the dual gate configuration enables individual control over the switching performance. Typical gate drive strategies for the dual gate HPS are shown in Fig. 6-2.

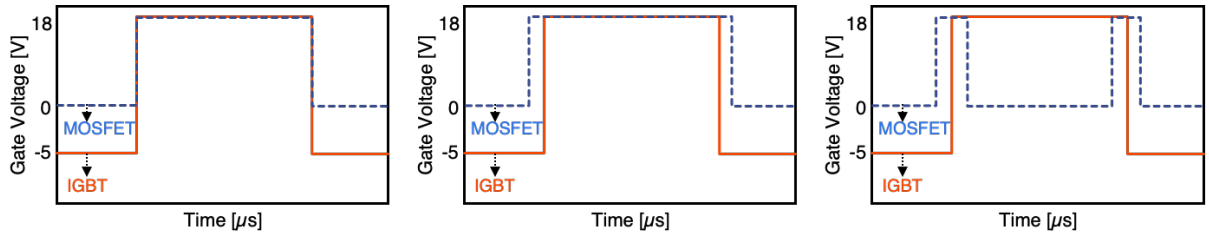


Fig. 6-2. Typical gate drive strategies for the HPS.

In an attempt to minimise the switching losses and fully utilise the device capability, the switching transitions must be in unipolar mode. This can be achieved by imposing a delay on the MOSFET turn-off in such a way to guarantee that the IGBT is switched off in advance of the MOSFET. The addition of delay, however, is not always needed for turn-on cycles because the MOSFET naturally turns on first due to its shorter delay time. During the delay, the entire IGBT current is diverted through the MOSFET. The MOSFET remains in the on-state as the IGBT switches which enables the IGBT to achieve a zero voltage switching (ZVS) transition.

6.2 Current Voltage Characteristics

The output characteristics (forward bias) of the HPS and its constituent components and their parallel arrangements are shown in Fig. 6-3.

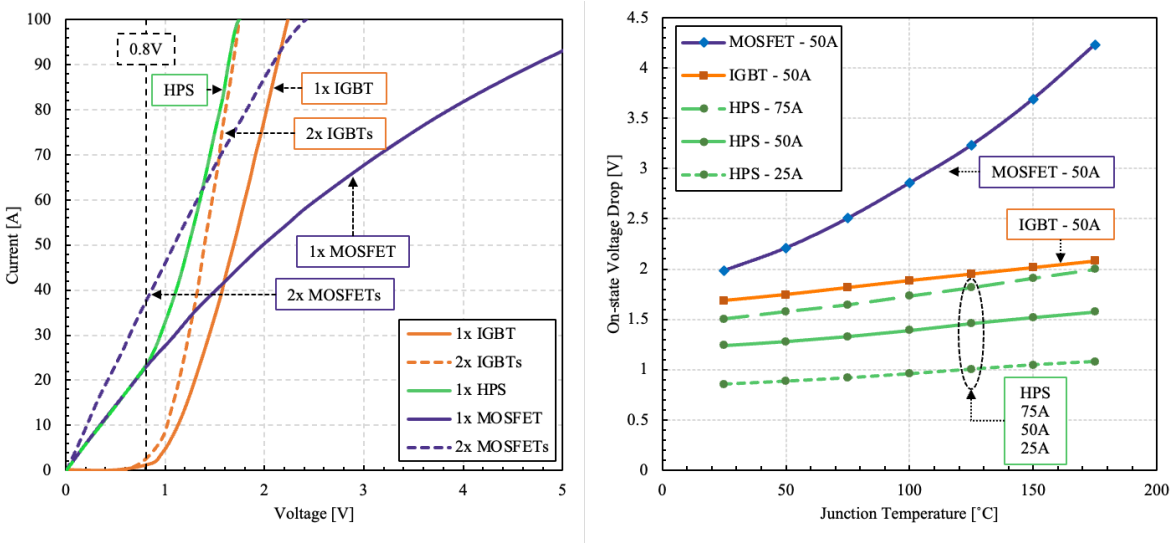


Fig. 6-3. Comparison of the output characteristics (forward bias) of the HPS and its constituents at RT (left) and on-state voltage drop at different junction temperatures (right). V_{GS} = 18 V.[22]

It is evident that the HPS I-V curve initially follows its constituent MOSFET as it offers the path of least resistance. The increase in forward current leads to a higher differential voltage across the devices beyond the bipolar on-set voltage of the IGBT, activating the bipolar mode of operation. In the bipolar regime, the on-resistance is modulated because of the conductivity modulation effect in IGBTs.

The HPS shows a mild positive temperature coefficient of on-state voltage that is similar to the constituent IGBT. The increase in temperature results in the bipolar on-set to be lowered and the on-resistance associated with the MOSFET to be increased. Consequently, the excess current is diverted to the IGBT, and the unipolar current is clamped. This unique dual mode of operation allows the HPS to maintain a low power loss profile over a wide range of temperatures. In this case, the boundary between the bipolar and unipolar mode is about 25 A at RT.

[22] Published in (8).

6.2.1 Reverse I-V characteristics

In several applications, reverse current flow is an essential requirement [104]. Conventional field stop IGBTs are not capable of reverse conduction and therefore, an anti-parallel diode is generally copacked with the device. RC-IGBTs, on the other hand, have a monolithic body diode built into the device. Meanwhile, MOSFETs are capable of reverse current flow via their body diode or their channel when a positive gate potential exceeding the threshold is present. In this HPS, multiple paths exist to facilitate reverse current flow which are illustrated in Fig. 6-4.

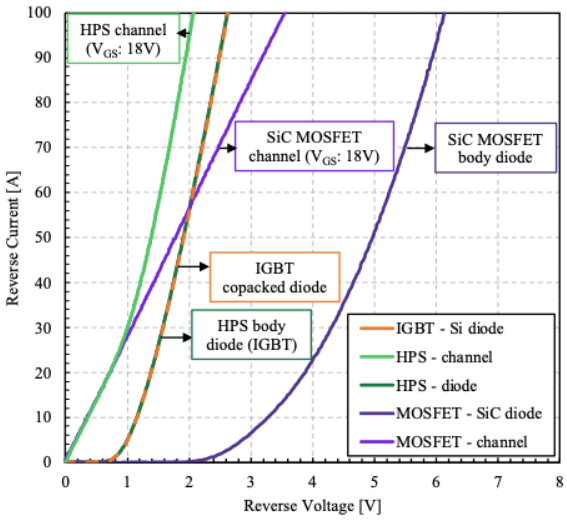


Fig. 6-4. Reverse output I-V (diode) characteristics of the HPS and its constituents at RT. The pulse width is 250 µs. [23]

The available paths for reverse current flow depend on the gate voltage. In the absence of gate bias, the only paths for reverse current are through the copacked diode or the body diode of the SiC MOSFET. However, in typical operating conditions, the current is handled by the copacked Si diode without any contribution by the SiC body diode because of its extremely

[23] Published in (4).

high bipolar on-set voltage. Meanwhile, when a gate bias over the threshold is supplied, the current can also flow through the MOSFET channel from the source to drain. The Si diode is activated at higher current (~ 25 A). It should be noted that other types of diodes including SiC MPS or GaN diodes can be integrated in the HPS to improve performance.

6.2.2 Capacitance characteristics

The capacitance characteristics of the HPS including the IGBT and MOSFET are presented in Fig. 6-5.

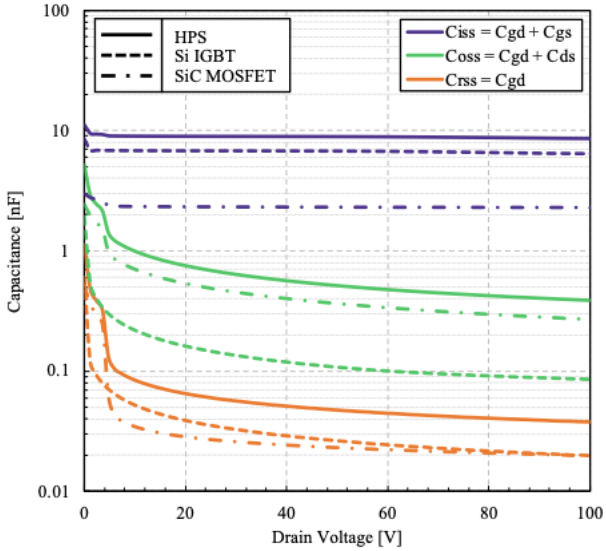


Fig. 6-5. Measured capacitance versus voltage of the HPS and its constituents at 100 kHz frequency. T_{amb} = 25°C. [24]

In the dual gate configuration, the effective capacitance of the HPS at the instance of switching is defined by its constituent MOSFET. This is because the IGBT is in off-mode while the device is switching. The output capacitance of the IGBT acts as a small parallel capacitance with minor impact on switching performance.

[24] Published in (8).

6.3 Switching Performance

This section provides a detailed evaluation of the HPS switching performance including its constituent components under various conditions.

6.3.1 Experimental setup

The switching performance of the HPS was assessed using a clamped inductive switching test bench as depicted in Fig. 6-6 and Fig. 6-7.

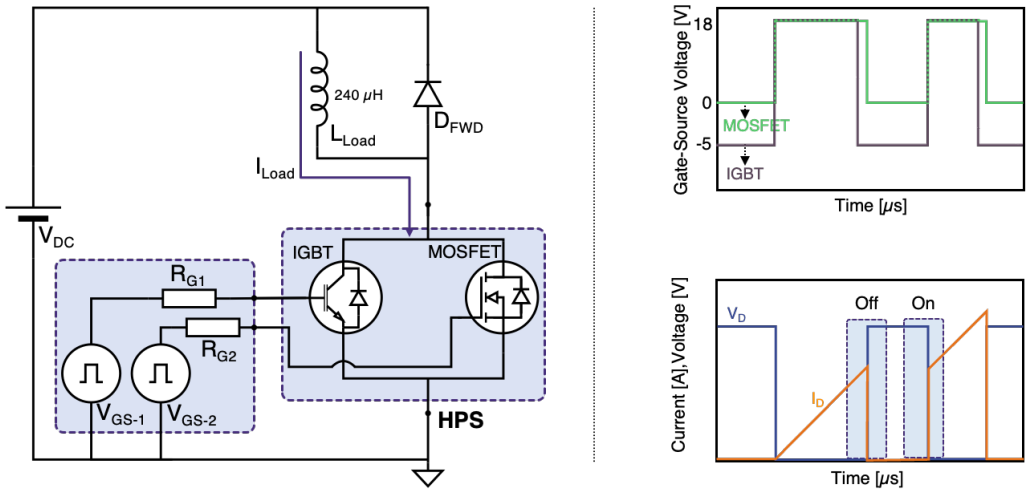


Fig. 6-6. Schematic of the experimental setup and typical switching waveforms.[25]

[25] Published in (8).

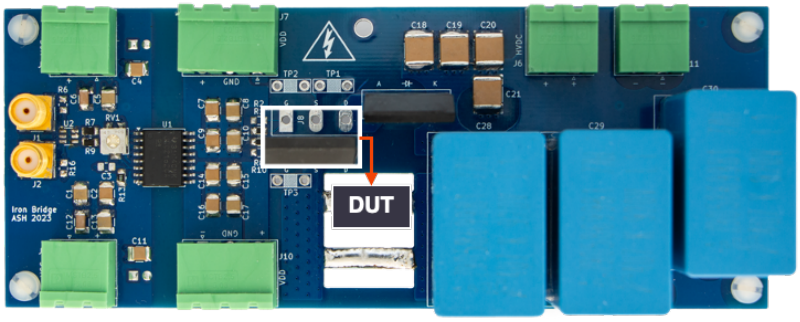


Fig. 6-7. Photograph of the practical implementation of the HPS experimental setup.

Two independent channels gate driver (based on the UCC21520) is used to drive the HPS dual gate configuration. Both gate drivers supply 18 V for turn-on. The turn-off gate voltage is maintained at 0 V and -5 V for the constituent MOSFET and IGBT respectively. In case of the single gate configuration, the applied gate voltages are 18 V and -5 V for turn-on and turn-off, respectively. The load inductor (L_{Load}) is 240 µH and a 1200 V SiC Schottky freewheeling diode (D_{FWD}) is used. The gate resistance for the IGBT is fixed at 47 Ω and 15 Ω for the turn-on and turn-off, respectively. For the purpose of comparison, two paralleled MOSFETs (2x MOSFETs) and two paralleled IGBTs (2x IGBTs) were tested. In case of the 2x MOSFETs, a 10 Ω current sharing gate resistor was used to prevent gate oscillations.

6.3.2 Influence of delay on switching performance

The delay time governs the switching characteristics and therefore, it is important to understand its influence. The test was conducted to evaluate the HPS switching performance under different delay times as shown in Fig. 6-8. The current flow through each constituent was monitored using a Rogowski current probe to visualise the current sharing mechanism between the MOSFET and IGBT.

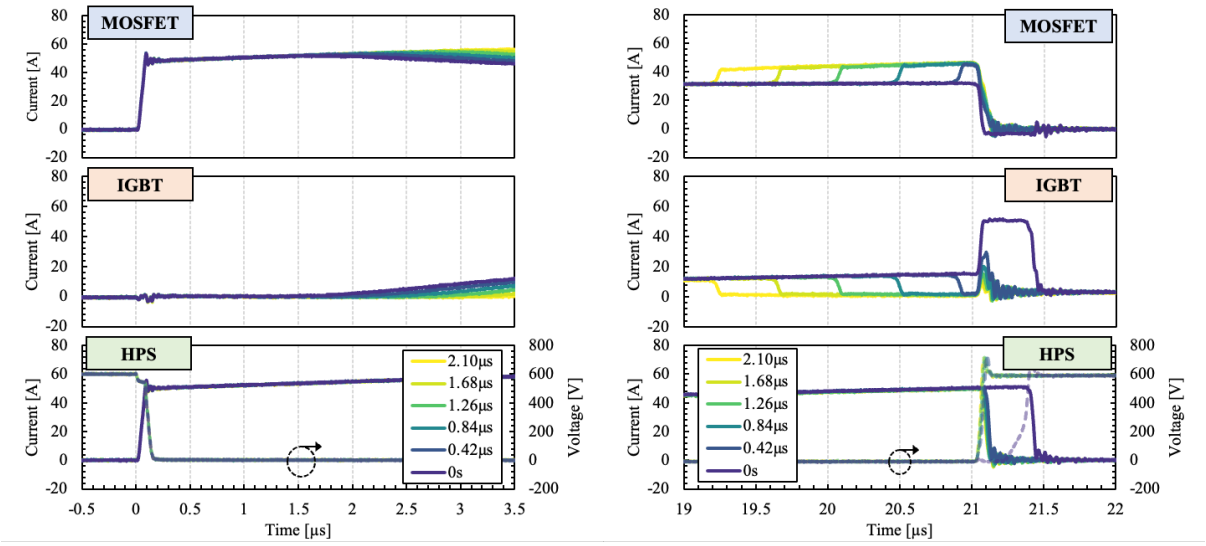


Fig. 6-8. Turn-on (left) and turn-off (right) switching waveforms of the HPS and its constituents at different time delays. $V_{GS\text{-}MOS}$ = 18 / 0 V, $V_{GS\text{-}IGBT}$ = 18 / -5 V, $R_{G\text{-}MOS}$ = 22 Ω, $R_{G(ON)\text{-}IGBT}$ = 47 Ω, $R_{G(OFF)\text{-}IGBT}$ = 15 Ω, T_{amb} = 25°C.[26]

It can be observed that the delay does not affect the turn-on waveforms because the IGBT naturally has a longer delay. Thus, the turn-on delay can be eliminated in most scenarios. Meanwhile, in turn-off, the delay affects the switching waveforms. It is clear that without a delay (0 s), the IGBT current persists after the MOSFET turn-off which negatively impacts the switching. Therefore, a delay is necessary to ensure optimal switching performance under unipolar conditions. A secondary hump can be seen in the IGBT current waveforms during the turn-off which is attributed to the parasitic capacitances being discharged.

To further optimise the switching, the IGBT gate resistance can be adjusted to lower values which helps to improve the IGBT switching speed. However, this will not affect the switching losses as it was observed that the switching characteristics are predominantly determined by the MOSFET.

[26] Published in (8).

6.3.3 Single gate switching

The single gate HPS is aimed at existing applications where pin-for-pin compatibility is a requirement. The switching waveforms of the single gate HPS at different gate resistances are shown in Fig. 6-9.

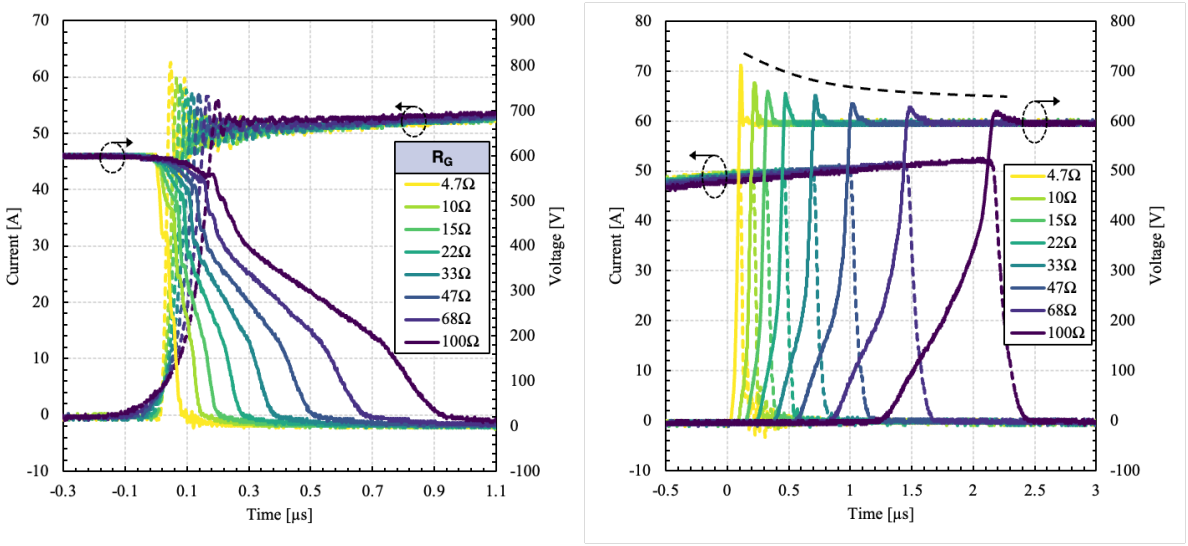


Fig. 6-9. Turn-on (left) and turn-off (right) switching performance of the single gate HPS at different gate resistances. R_G = 15 Ω, T_{amb} = 25˚C.[27]

It is noticeable that the voltage waveforms are similar to that of an IGBT with 'S' shape slope at high gate resistances. This indicates the IGBT is not fully off during the switching transitions and therefore contributes to the switching losses. At high gate resistances, this becomes clearer as the slope decreases.

6.3.4 Dual gate switching

The dual gate configuration provides additional levels of controls with options to fully optimise the performance. The corresponding turn-on and turn-off switching events at different gate

[27] Published in (8).

resistances are illustrated in Fig. 6-10. A delay of 1 µs is imposed between the gates during the turn-off.

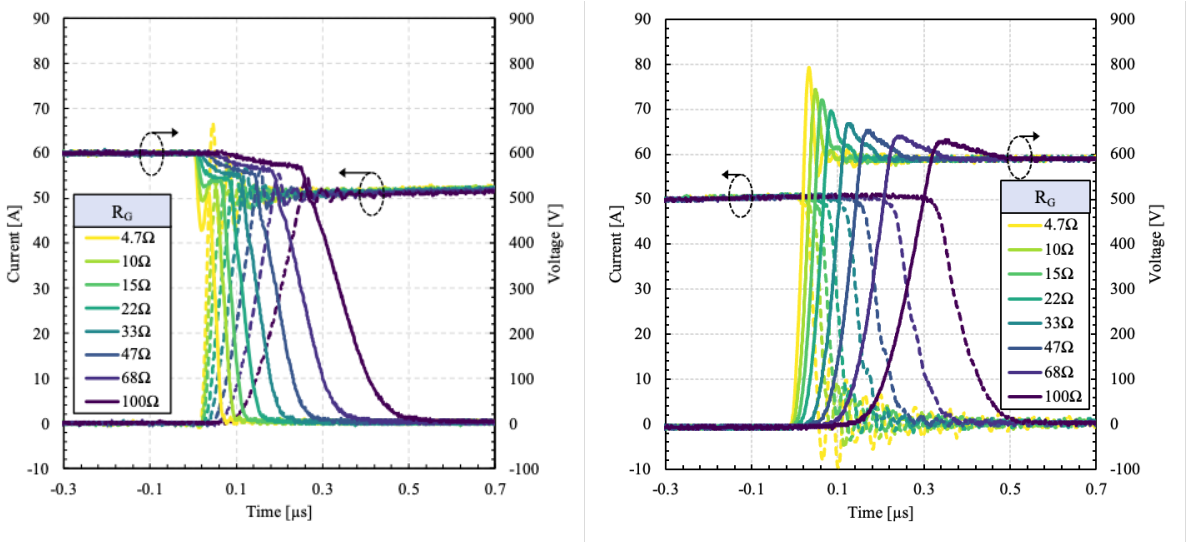


Fig. 6-10. Turn-on (left) and turn-off (right) switching performance of the HPS at different gate resistances. $R_{G(ON)\text{-}IGBT}$ = 47 Ω, $R_{G(OFF)\text{-}IGBT}$ = 15 Ω, $t_{delay\text{-}on}$ = 0 s, $t_{delay\text{-}off}$ = 1 µs, T_{amb} = 25°C.[28]

The switching waveforms are similar to FETs and no tail current can be observed. One of the advantages of the dual gate HPS is the suppression of dynamic avalanche (DA) as the IGBT undergoes a ZVS transition (and dV/dt is zero). Therefore, the integral IGBT can be operated at higher current densities and switching speeds.

Based on the measurements, the turn-on dV/dt, fall time and turn-on energy have been extracted as presented in Fig. 6-11.

[28] Published in (8).

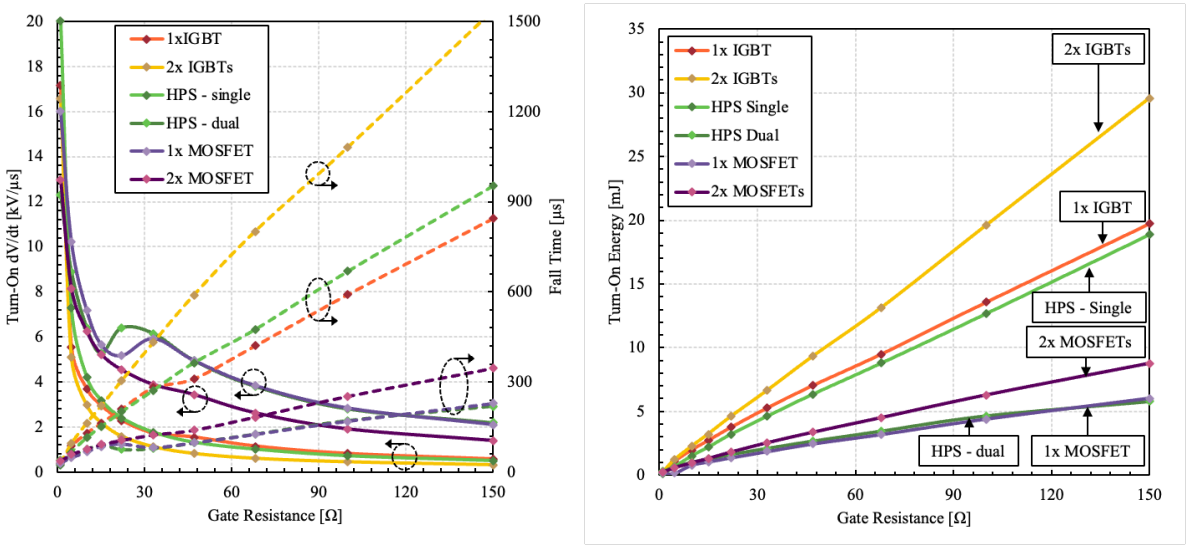


Fig. 6-11. Measured turn-on dV/dt and fall time (left) and turn-on energy (right) at different gate resistances. T_{amb} = 25˚C.[29]

The dissipated energy of the HPS – dual gate is almost identical to that of the 1x MOSFET and lower than the 2x MOSFETs. The single gate HPS has noticeably higher power losses and slower switching than the dual gate because the current is not fully handled under unipolar mode. However, the losses associated with the single gate HPS are lower than the 1x IGBT and significantly lower than that of the 2x IGBTs. Similar to the turn-on, the turn-off dV/dt, rise time and turn-on energy have been extracted as presented in Fig. 6-12.

[29] Published in (8).

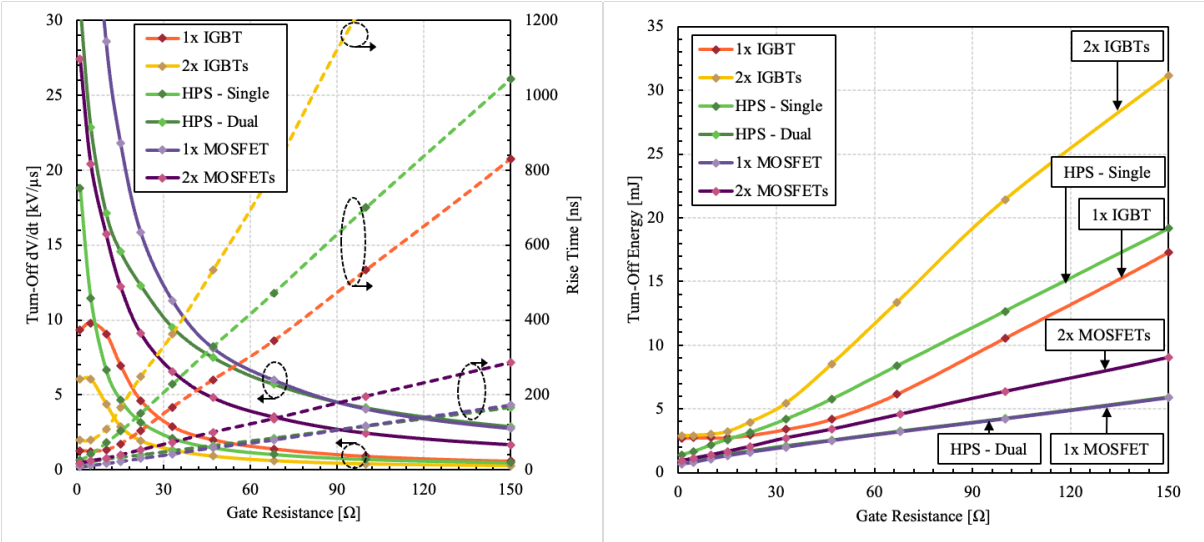


Fig. 6-12. Measured turn-off dV/dt and rise time (left) turn-off energy (right) at different gate resistances. T_{amb} = 25°C.[30]

The dual gate HPS has almost identical switching characteristics as the 1x MOSFET. This confirms that the entire switching current is handled by the consistent MOSFET in unipolar mode. In addition, the single gate configuration exhibits lower switching losses than equivalent 2x IGBTs. Due to the DA effect, a plateau can be observed in the turn-off dV/dt and energy losses of the 1x IGBT and the 2x IGBTs at low gate resistances of below 15 Ω. DA in IGBTs occurs during high dV/dt, high current turn-off switching transitions leading to constraints on power losses and switching controllability and reliability in the long term [15] [105]. Such behaviour is suppressed in the HPS because the current is fully commuted to the MOSFET and the IGBT undergoes a zero-voltage switching transition (and dV/dt = 0).

6.3.5 Impact of load current on the switching characteristics

The switching performance of the dual-gate HPS was evaluated at 600 V and different load currents from 10 A to 100 A as presented in Fig. 6-13.

[30] Published in (8).

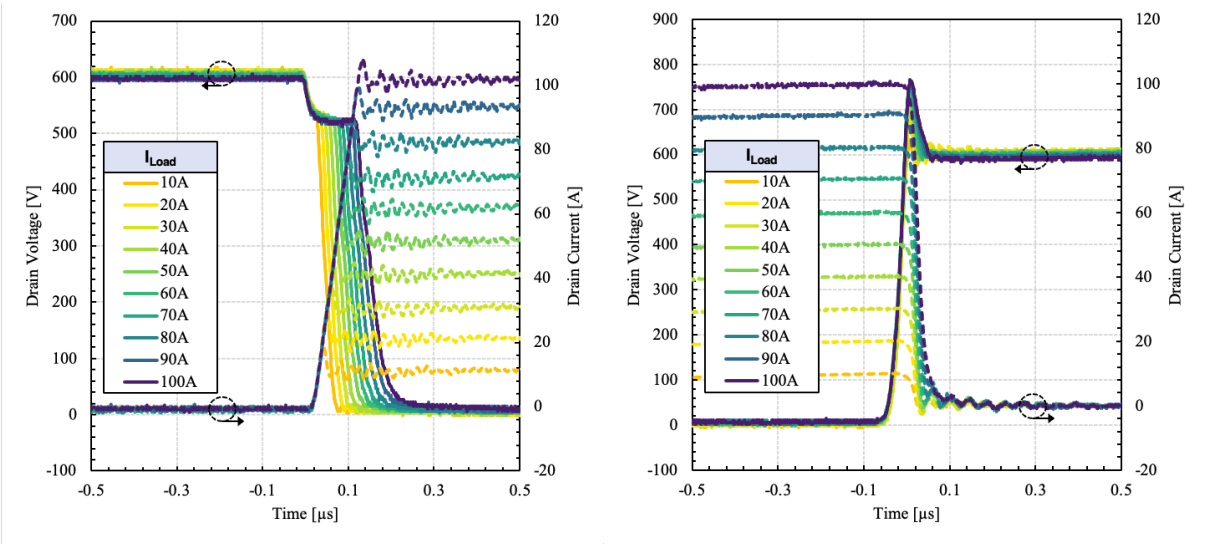


Fig. 6-13. Turn-on (left) and turn-off (right) switching waveform of the HPS at different load currents. $R_{G(ON)\text{-}IGBT} = 47\ \Omega$, $R_{G(OFF)\text{-}IGBT} = 15\ \Omega$, $t_{delay\text{-}on} = 0$ s, $R_{G\text{-}FET} = 22\ \Omega$, $t_{delay\text{-}off} = 1$ µs, $T_{amb} = 25$°C.[31]

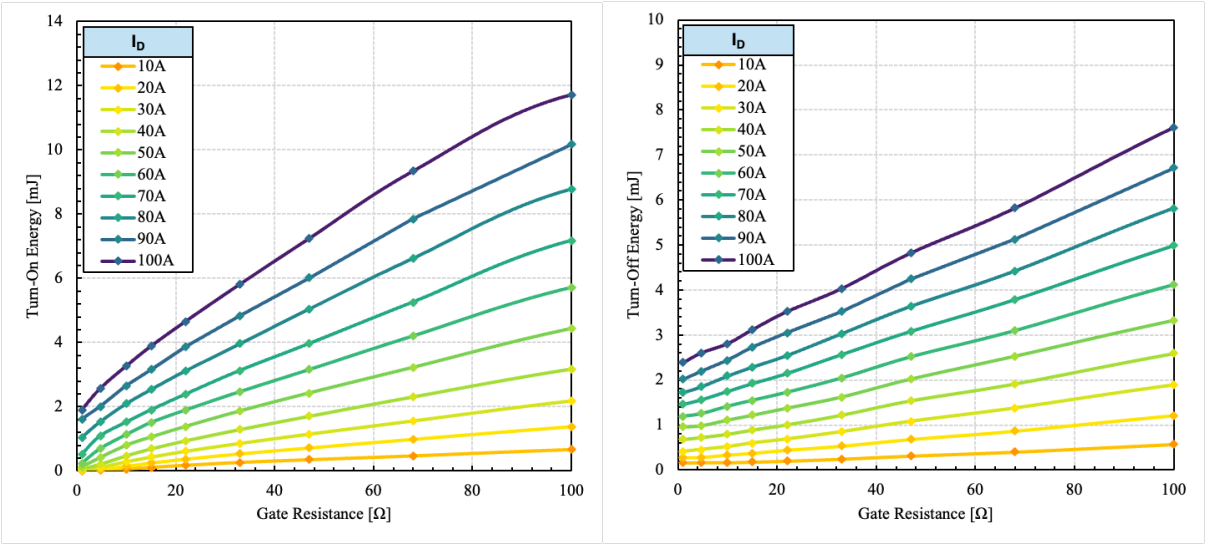


Fig. 6-14. Measured switching energy during turn-on (left) and turn-off (right) of the HPS as a function of load current at different gate resistances. $R_{G(ON)\text{-}IGBT} = 47\ \Omega$, $R_{G(OFF)\text{-}IGBT} = 15\ \Omega$, $t_{delay\text{-}on} = 0$ s, $t_{delay\text{-}off} = 1$ µs, $T_{amb} = 25$°C.[23]

The switching energy increases in a linear manner with the gate resistance. Using an intelligent gate drive allows the IGBT to remain off at low current levels, as the MOSFET fully

[31] Published in (8).

controls the current flow. It is therefore possible to operate at higher switching frequency based on the current levels.

6.4 Power Loss Analysis

A breakdown of power losses associated with the HPS and its equivalent constituent at different operating frequencies is provided in Fig. 6-15.

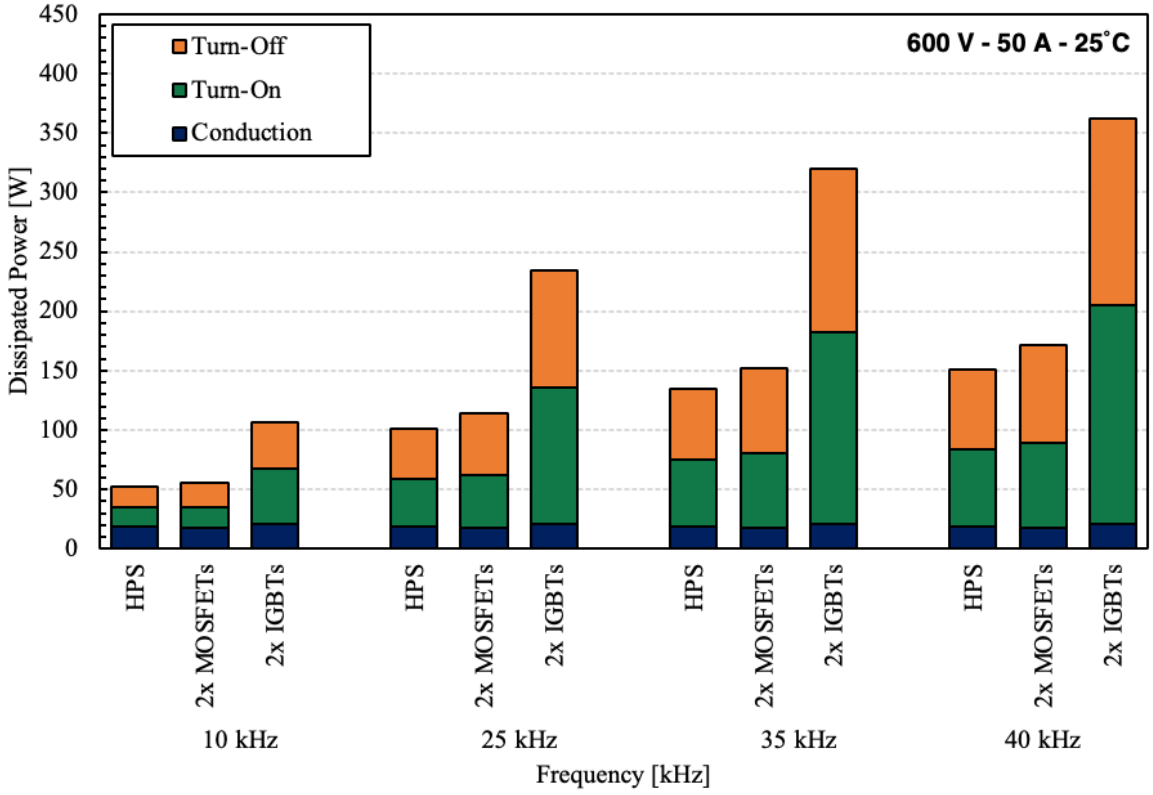


Fig. 6-15. Comparison of contributions of the power loss components relative to the switching frequency. V_{SW} = 600 V, I_{Load} = 50 A, T_{amb} = 25 ˚C, Duty cycle = 30 %.[32]

[32] Published in (8).

The total power loss associated with the dual gate HPS is lower than the equivalent MOSFET and IGBT solutions. This can be achieved thanks to the MOSFET-like switching behaviour and IGBT-like conduction.

6.5 Short Circuit Capability

One of the key parameters indicating reliability and ruggedness of a power semiconductor device is its ability to survive short circuit fault conditions. The worst case scenario in HPS happens when all the integral components are simultaneously subject to short circuit for an equal period. To determine the short circuit performance, the HPS was subjected to a short circuit fault for 3 µs at 600 V supply voltage as presented in Fig. 6-16. The gate voltage for its constituents was set at 15 V based on the manufacturer's recommendation. Higher gate voltages adversely affect the short circuit performance due to a higher saturation current.

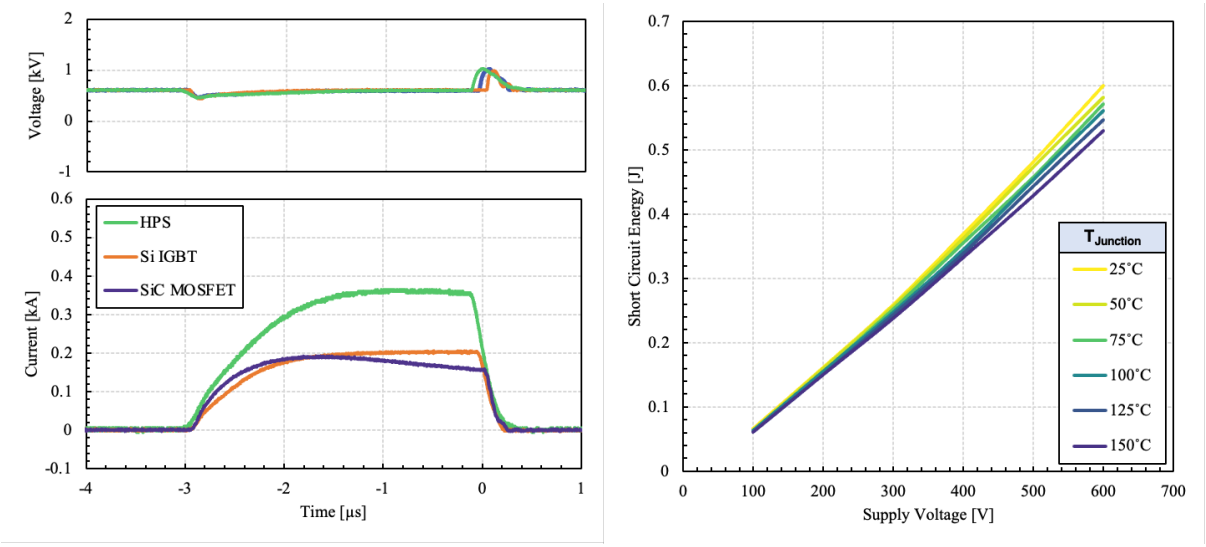


Fig. 6-16. Short circuit waveforms of the HPS and its constituents at 150˚C (left) and the dissipated energy as a function of supply voltage at different junction temperatures (right). V_{GS} = 15 V and R_G = 22 Ω.[33]

[33] Published in (8).

The current passing through the HPS when subjected to short-circuit conditions is equivalent to the sum of its individual components. The limiting factor in the HPS is determined by the component with the lower short circuit withstanding capability. In this configuration, the SiC MOSFET offers a lower short-circuit performance as stated by the manufacturer. The dissipated short circuit energy was extracted at different junction temperatures as shown in Fig. 6-16. The dissipated energy increases linearly with the supply voltage. Conversely, the saturation current exhibits a positive temperature coefficient which results in a decrease in the dissipated energy at elevated temperatures.

6.6 Chapter Conclusion

In this chapter, the performance of HPS consisting of Si IGBT and SiC MOSFET technology has been comprehensively studied. The HPS offers an economical option for power demanding applications requiring maximum efficiency over a wide range of operating conditions. Unlike full SiC only solutions, the HPS maintains low on-state losses even at high temperatures due to its mild PTC. With an intelligent gate driver, the switching performance can be fully optimised and switching losses as low as its constituent SiC MOSFET can be achieved. The switching characteristic of the HPS is exclusively determined by its constituent MOSFET when an appropriate gate drive strategy is used. The optimal delay depends on the switching characteristics of the constituent components of the HPS. Despite the very fast switching performance, one of the limitations of the HPS is the maximum operating frequency which is restricted by its integral IGBT. Meanwhile, it is possible to vary the frequency depending on the load conditions. Under low current conditions, the frequency can be increased beyond the IGBT limit because there is no bipolar current flow. This feature can be of interest in several applications.

Chapter 7

Hybrid Power Switches Using CIGBT

IGBTs long dominance in medium power applications is attributable to their excellent performance, affordability and wide SOA. The development trend in IGBTs has been focused on achieving higher current densities along with lower voltage drop in on-state. Nevertheless, conventional IGBTs have a number of limitations such as dynamic avalanche which limits their performance. In this chapter, a new 1200 V HPS concept utilising the trench clustered IGBT (CIGBT) which aims to overcome some of the limitations of conventional IGBTs and SiC MOSFET technology will be introduced. The device physics of operation are discussed, and its characteristics are evaluated through experimental measurements.

7.1 Physics of Operation

CIGBTs are aimed at as a chip-for-chip but more efficient replacement of IGBTs [106]. Cross-sectional diagrams of the trench CIGBT and the conventional trench IGBT are provided in Fig. 7-1.

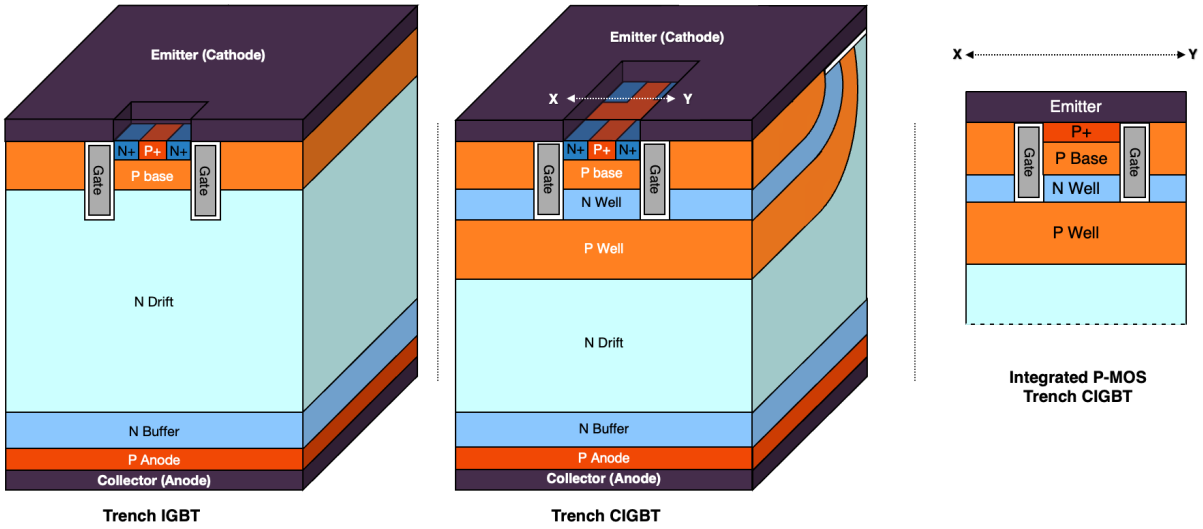


Fig. 7-1. Three dimensional structures of the trench IGBT and the trench CIGBT. The X-Y cutline shows the integrated P-MOS structure used to extract holes.

The main structural distinction between the CIGBTs and conventional IGBTs is the addition of a highly conductive N-well layer on top of a floating P-well layer which produces a MOS controlled thyristor action [107]. Consequently, a lower on-state voltage can be attained which enables the device to handle higher current densities compared to conventional field stop IGBTs. During the on-state, the PN junction that is formed by the P-base/N-well layers is reversed biased which leads to a depletion region expanding toward the P-well layer. At a preset potential which is referred to as ‘self-clamping voltage’, the N-well layer is punched through which leads to the voltage across the gate to be clamped and therefore protecting the trench gates from extreme electric fields [108] [109]. A P-type MOSFET constituting the P-base/N-well/P-well is also integrated in the design which facilitates the removal of holes alongside the gate, suppressing the dynamic avalanche effect. Akin to applying a negative gate bias, the rise in the voltage of the N-well region turns on the P-MOS which provides a direct route for the removal of holes and therefore DA is avoided.

7.2 Static Characteristics

7.2.1 Output characteristics

The measurement results of the output characteristics of the 1.2 kV FS trench CIGBT as a function of gate voltage and junction temperatures are presented in Fig. 7-2.

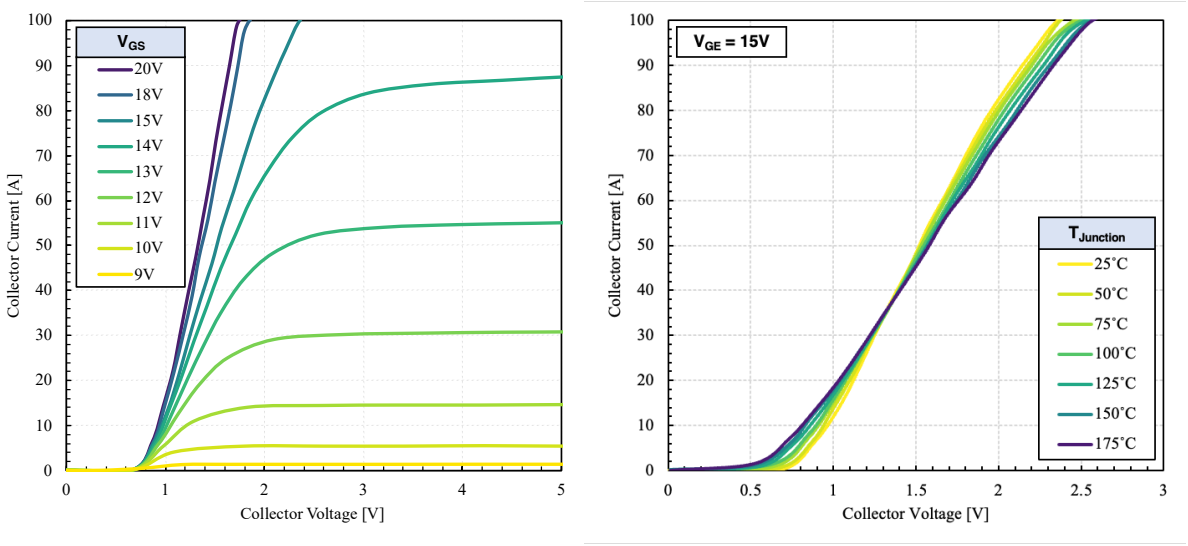


Fig. 7-2. Output characteristics of the 1.2 kV trench CIGBT at RT (left) and elevated temperatures (right). The pulse width is 250 µs.

The output characteristics of the CIGBT are similar to standard IGBTs. The measured on-state voltage drop is near 1.5 V at 50 A and a gate voltage of 15 V. The collector emitter saturation voltage of the CIGBT as a function of load current at temperatures ranging from 25˚C to 175˚C is presented in Fig. 7-3.

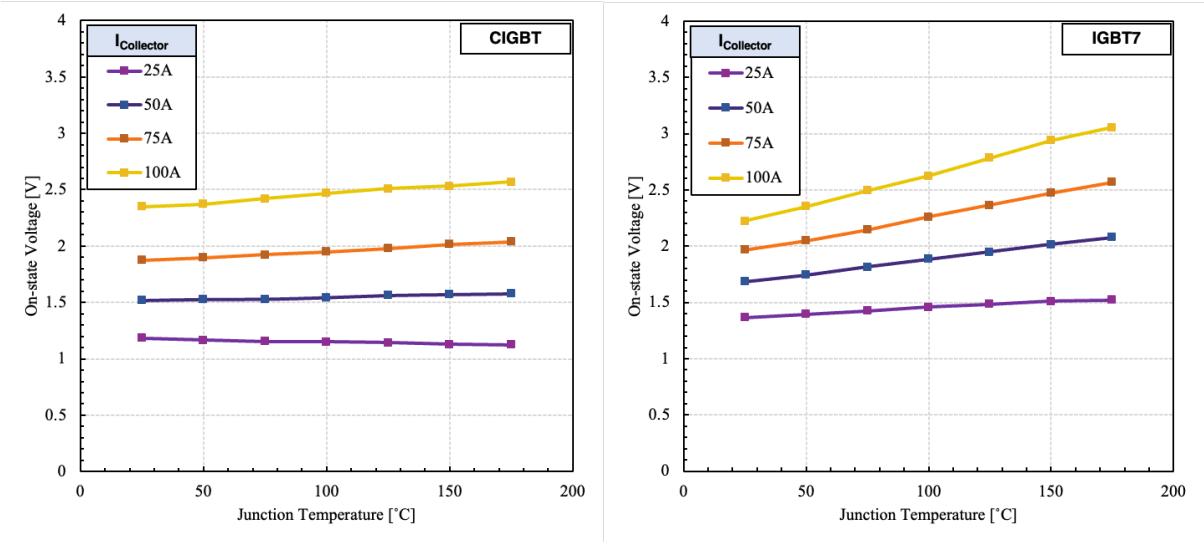


Fig. 7-3. On-state voltage drop of the 1.2 kV CIGBT and the IGBT7 measured at different junction temperatures and load currents. The gate voltage is 15 V.

The voltage drop of the CIGBT under on-state is observed to be smaller compared to the latest IGBT counterparts [102] which leads to a substantial reduction in on-state losses. This is due to the effective utilisation of thyristor conduction mode resulting in strong conductivity modulation. Considering their similar active area, CIGBT can operate at higher current densities compared to the IGBT.

7.3 Switching Performance

The typical turn-on and turn-off switching performances of the 1.2 kV trench CIGBT are presented in Fig. 7-4.

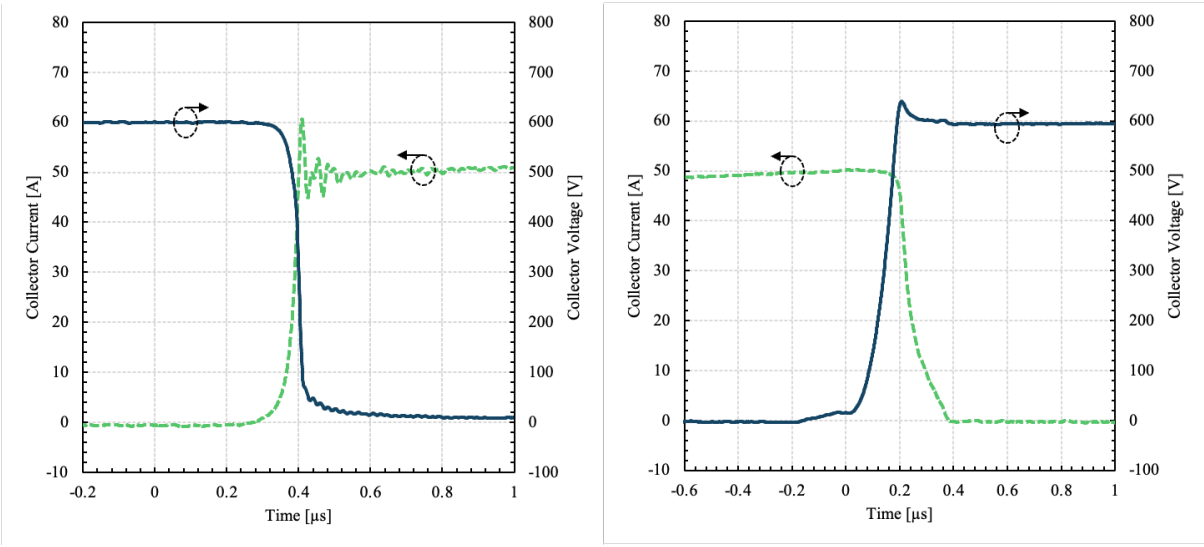


Fig. 7-4. Typical switching waveforms of the 1.2 kV CIGBT at turn-on (left) and turn-off (right). V_{GE} = 15 V, T_{amb} = 25˚C.

The test was performed using the circuit presented in Chapter 6. In terms of switching, the CIGBT is similar to conventional IGBTs. Due to the bipolar nature of the device, a small tail current can be observed at the turn-off. A detailed comparison of switching performance will be presented in the next section.

7.4 CIGBT in Hybrid Power Switch Configuration

In the previous chapter, the concept of HPS has been discussed based on the IGBT technology. In this part, a new dual gate HPS based on the latest 1.2 kV FS trench CIGBT and SiC MOSFET (CoolSiC – IMW120R030M1H – Infineon [103]) technologies is presented. These devices are housed in TO-247 packages and share similar power ratings to those presented in the previous chapter. The experimental methodology is the same as in Chapter 6.

7.4.1 On-state performance

The performances of the HPS and its constituents under on-state condition are characterised by the measured output I-V curves presented in Fig. 7-5.

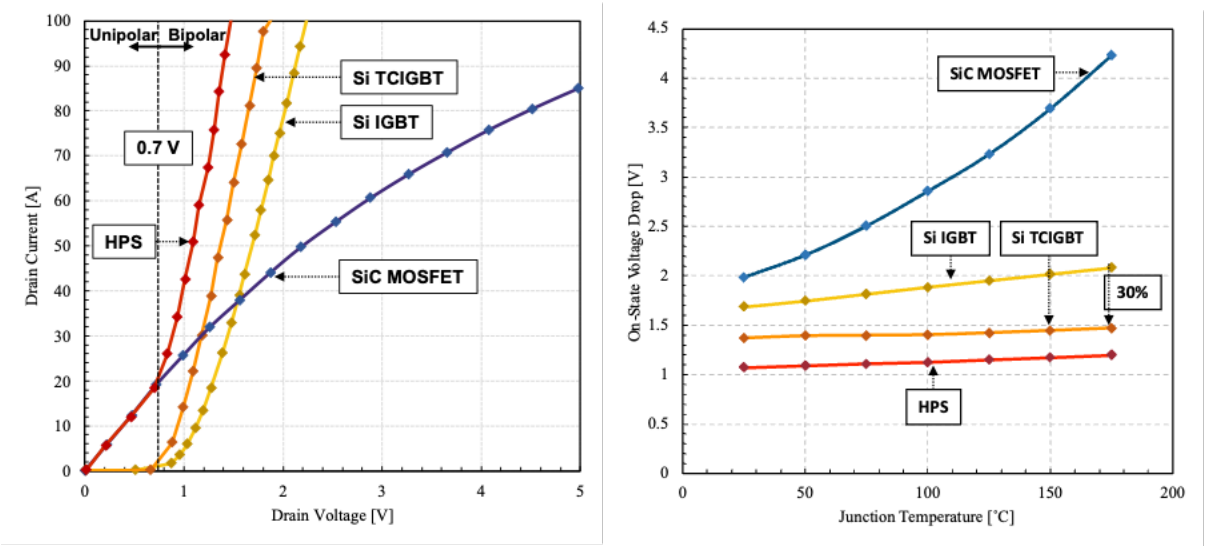


Fig. 7-5. Comparison of the output I-V curves at RT (left) and the on-state voltage drop at different junction temperatures and 50 A load current (right). The pulse width is 250 µs and V_{GS} is 18 V.[34]

The boundary current magnitude between unipolar and bipolar modes is about 20 A at RT. The use of CIGBT results in a 30 % performance gain in on-state voltage drop at maximum rated junction temperature which can improve the current density in the HPS.

7.4.2 Switching characteristics

The switching performance of the HPS was tested at 600 V and 50 A at different gate resistances as plotted in Fig. 7-6. The turn-on and turn-off gate resistances of the constituent CIGBT are fixed at 47 Ω and 15 Ω, respectively.

[34] Published in (6).

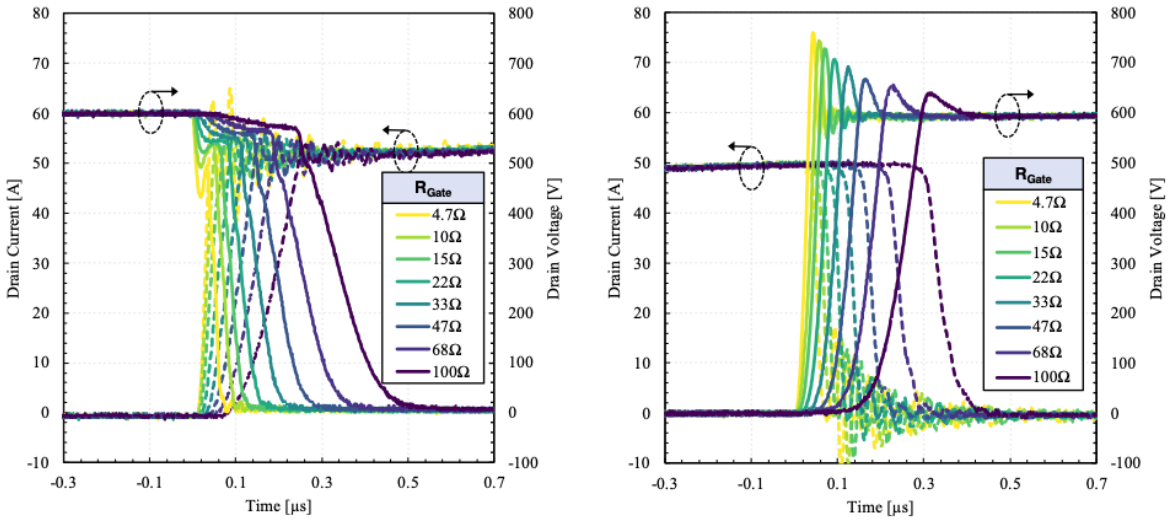


Fig. 7-6. Turn-on (left) and turn-off (right) switching events at different gate resistances. $R_{G(ON)\text{-}CIGBT}$ = 47 Ω, $R_{G(OFF)\text{-}CIGBT}$ = 15 Ω, $t_{delay\text{-}on}$ = 0 s, $t_{delay\text{-}off}$ = 2 µs, T_{amb} = 25°C.[35]

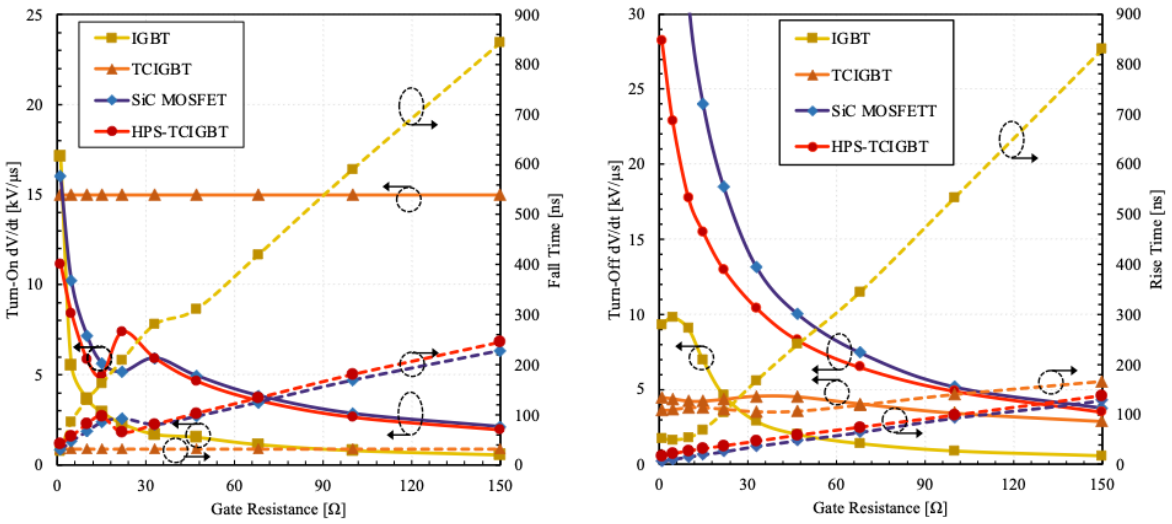


Fig. 7-7. Measured dV/dt and switching time at different gate resistances.[27]

The HPS switching performance is similar to the constituent MOSFET. It can be noted that the switching time and the slew rate of the CIGBT are flat and are not affected by varying the external gate resistor. The flat dV/dt response is attributed to the gain of the constituent thyristor which determines the switching performance, and the effect of gate resistance is nominal. A

[35] Published in (6).

detailed analysis of the CIGBT switching is reported in [110]. It is also evident that the turn-off dV/dt in the conventional IGBT reaches a plateau at low gate resistances ($R_G < 22\ \Omega$) due to the DA effect. In the CIGBT, DA is suppressed by design and the effective use of P-MOS.

7.4.3 Power loss analysis

According to the measurements, the constituent elements of power loss associated with the HPS are presented in Fig. 7-8.

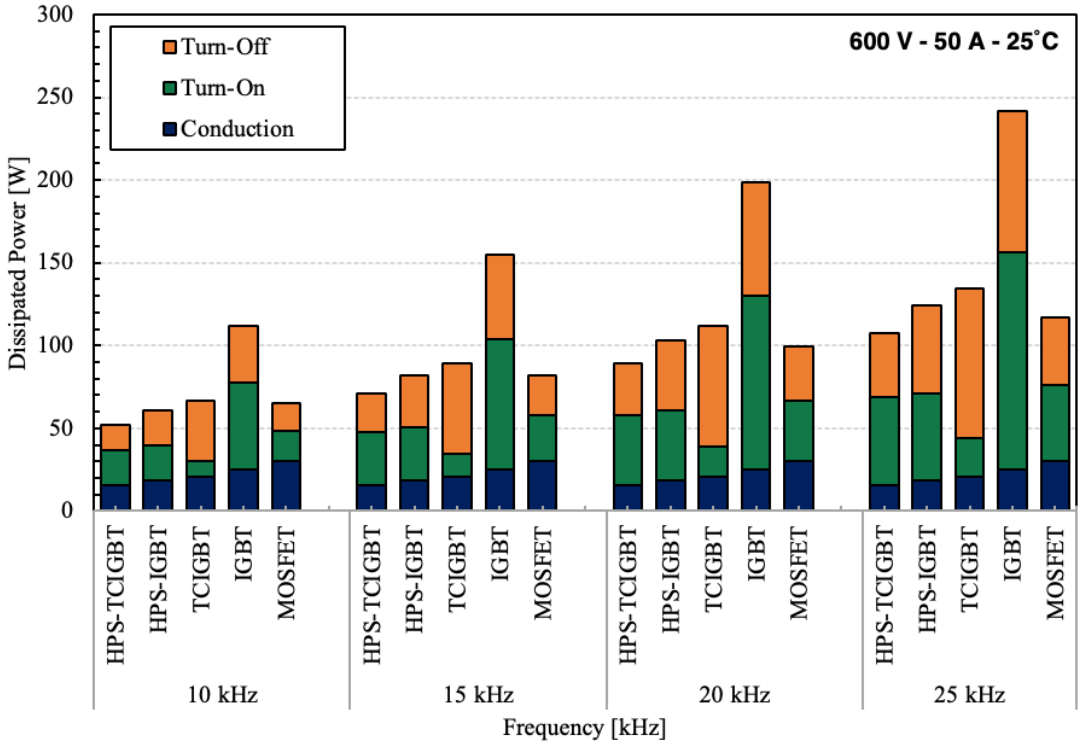


Fig. 7-8. Power loss comparison of the HPS, CIGBT, IGBT, and MOSFET at different frequencies. V_{SW} = 600 V, I_{Load} = 50 A, T_{amb} = 25 ˚C, Duty cycle = 30 %.

The HPS shows the lowest power loss because of unipolar switching characteristics while benefiting from the high current capability of CIGBT. The overall power losses of CIGBT are lower than the latest IGBT7 technology because of its superior characteristics, making it suitable for integration in the HPS.

7.5 Chapter Conclusion

In this chapter, the device physics, characteristics and switching performance of 1.2 kV CIGBTs in discrete and HPS configurations have been analysed in detail and compared with the latest IGBT technology. According to the results, CIGBTs exhibit improved characteristics compared to conventional IGBTs. The unique self-clamping mechanism of CIGBTs permits the device to reliably handle high current densities and more efficiently without DA. Meanwhile, the HPS constructed based on the CIGBT shows a lower power loss compared to that of conventional IGBTs because of the superior on-state performance of the CIGBT.

Chapter 8

Hybrid Power Switches Using Cascode GaN FET

In the previous chapters, the HPS were demonstrated using the SiC MOSFET and Si IGBT technologies. GaN devices can potentially offer faster switching speed and power lower losses which makes them suitable for their heterogeneous integration in the form of HPS. In this chapter, for the first time, a HPS concept comprising a cascode GaN FET, a Si IGBT, and a SiC merged PiN Schottky (MPS) diode is presented, and its characteristics are evaluated experimentally.

8.1 GaN-Si-SiC HPS Concept

The internal circuit diagram of the proposed HPS in single gate and dual gate configurations is illustrated in Fig. 8-1.

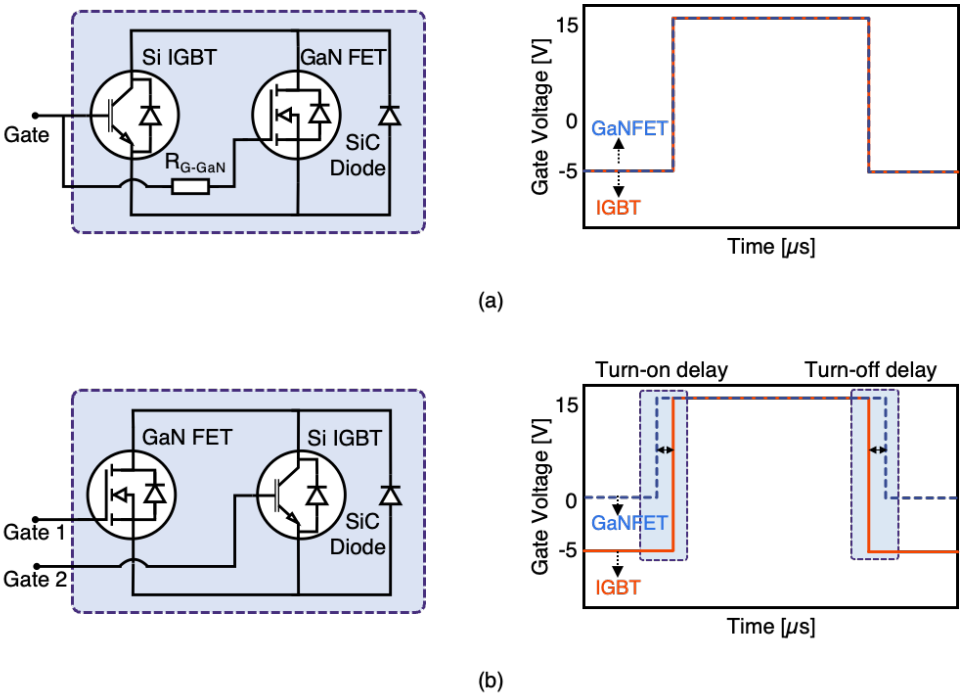


Fig. 8-1. Schematic of the cascode GaN Si SiC HPS and gate drive strategy.

The HPS is formed by a parallel configuration of a GaN FET [111], a Si IGBT [112] and a SiC Schottky diode [113] which are rated for 650 V and housed in a TO-247 package. The device is configured in a dual gate mode in order to fully exploit the device performance by allowing the GaN FET to control the switching characteristics. Because GaN FETs switch faster than IGBTs and have smaller switching times, a delay is necessary to fully optimise the performance. Both internal switches have compatible gate voltage requirements which can simplify the gate drive design.

8.2 Static Characteristics

8.2.1 On-state characteristics

The measurement results of the output I-V characteristics of the HPS and its constituent components are illustrated in Fig. 8-2.

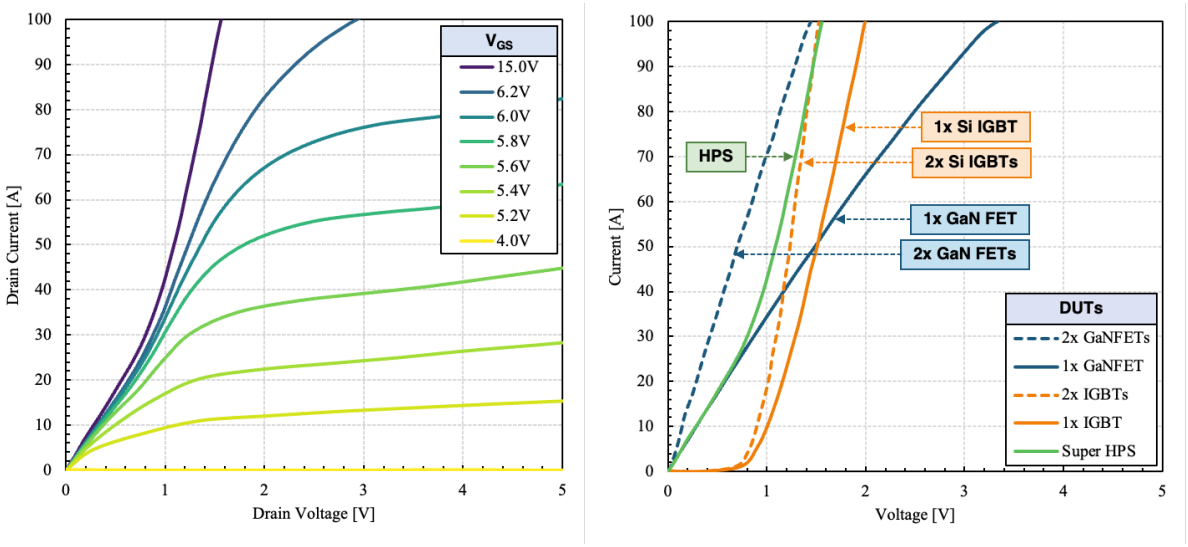


Fig. 8-2. Output I-V characteristics of HPS at different gate voltages (left) and comparison of the measured output I-V curves of the HPS and its constituents at $V_{GS} = V_{GE} = 15$ V (right). $T_{amb} = 25^{\circ}C$. [36]

The HPS delivers 100 A at 1.5 V which is lower than any of its individual components. Similar to the previous HPS, this configuration initially follows the GaN FET until the voltage drop is sufficiently high to overcome the bipolar on-set voltage of the IGBT. The boundary between bipolar and unipolar mode is about 28 A at RT and V_{GS} of 15 V.

The I-V measurements were repeated at different temperatures and the corresponding on-state voltage drops were extracted as a function of current as presented in Fig. 8-3.

[36] Published in (10).

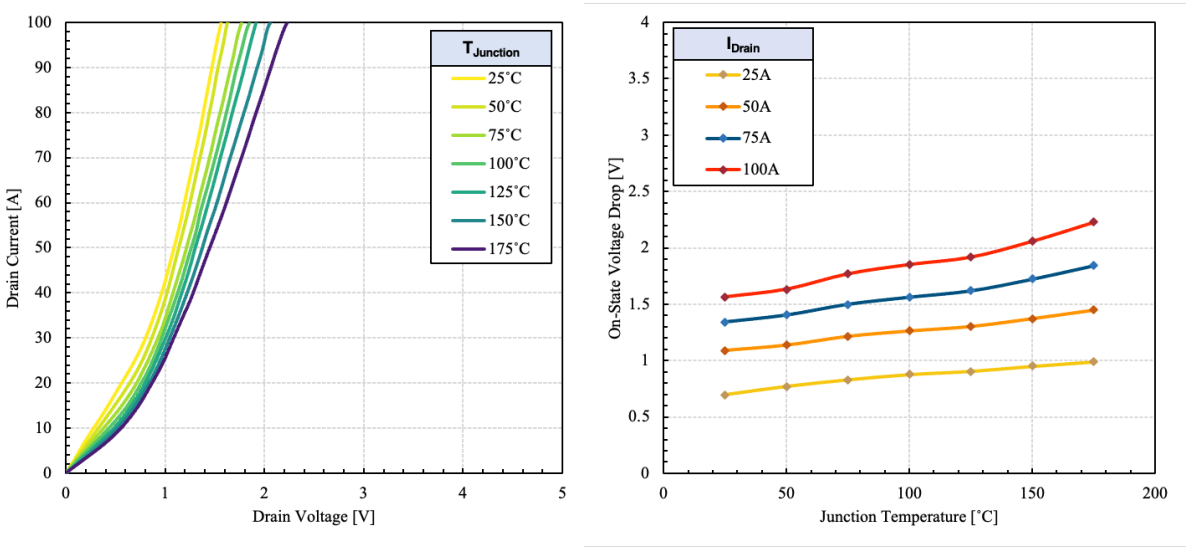


Fig. 8-3. Output I-V curves at different temperatures (left) and the on-state voltage drop of the HPS at different load currents and temperatures (right). V_{GS} = 15 V.[37]

The HPS delivers low power losses through different load conditions with a mild PTC of on-state voltage drop similar to the IGBT as the excess load is diverted through the internal IGBT.

8.2.2 Reverse characteristics

The measured reverse characteristics (source-drain) of the HPS and its constituents are shown in Fig. 8-4.

[37] Published in (10).

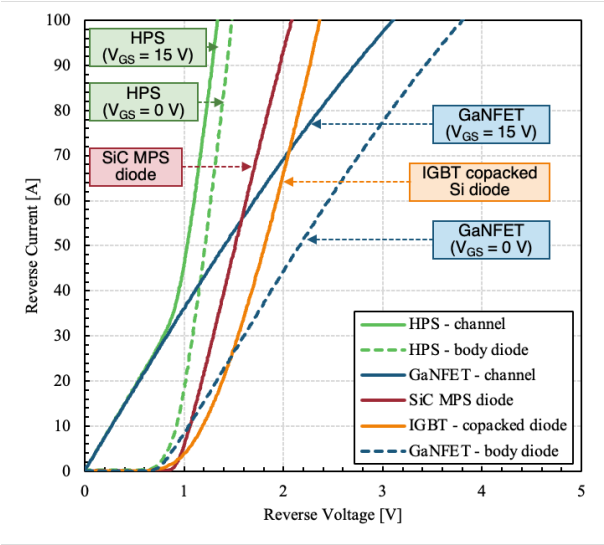


Fig. 8-4. Reverse I-V characteristics of the HPS and its constituent measured at RT. [38]

The current can flow through various paths provided by the HPS under reverse bias conditions. The reverse conduction takes place primarily via the two discrete Si soft recovery and SiC Schottky diodes when the V_{GS} is 0 because of their similar thresholds. Although the internal GaN FET has a body diode, it contributes less to the conduction because of its higher slope resistance. The corresponding slope resistance of the HPS body diode is ~ 6 mΩ. A positive gate bias above the turn-on gate threshold of the cascode GaN FET provides an additional path via the MOSFET channel which reduces the resistance significantly by bypassing its body diode. In this mode, the current is initially handled through the GaN FET until 30 A at 25˚C and above this point the discrete diodes also contribute and take over the excess load. Ultimately, the choice of diode depends on the mission profile and can be selected accordingly.

[38] Published in (10).

8.2.3 Off-state characteristics

The measured off-state leakage current I-V characteristics of the HPS are shown in Fig. 8-5.

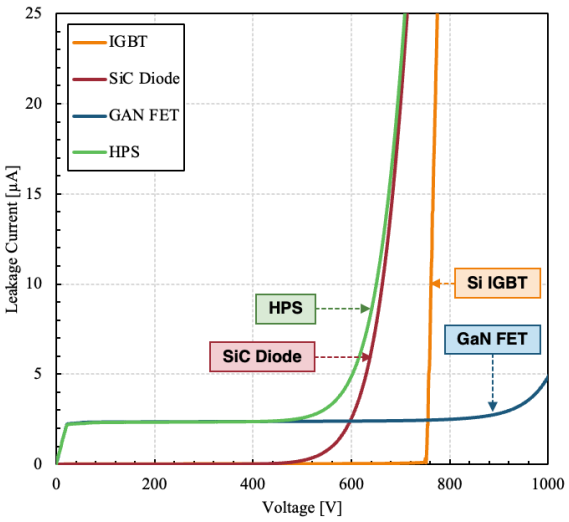


Fig. 8-5. Off-state I-V characteristics of the HPS and its constituents at RT. V_{GS} = 0 V.[39]

The leakage current in the HPS is mostly due to the cascode GaN FET until the breakdown. The reason for the higher leakage current is attributed to the internal cascode structure. In conventional devices, a margin of 20 % is generally used for the breakdown voltage. However, in GaN FETs, this margin is significantly higher due to the absence of avalanche ruggedness. Amongst the constituents of the HPS, the SiC Schottky diode is selected to have a lower avalanche breakdown voltage. Conversely, the GaN FET incorporates a substantial margin of breakdown voltage above its rating which leads to higher on-resistance and higher capacitance. Therefore, under surge voltage transients, the excess voltage across the HPS is clamped by the SiC diode. This mechanism protects the switch and enables the HPS to withstand avalanche breakdown without destruction. As a result, the GaN FET can be designed with a lower margin of breakdown voltage which leads to reduced on-resistance and improved switching

[39] Published in (10).

performance. This could also potentially bring cost advantages as the GaN FET can be fabricated on smaller and more power dense dies. Both devices are supplied with 15 V turn-on gate voltage. For the IGBT a negative gate voltage of -5 V is used.

8.3 Switching Characteristics

Using the same circuit presented in Chapter 6, the switching performance of the HPS has been assessed across different current levels from 10 A to 100 A in 10 A steps at 600 V as presented in Fig. 8-6.

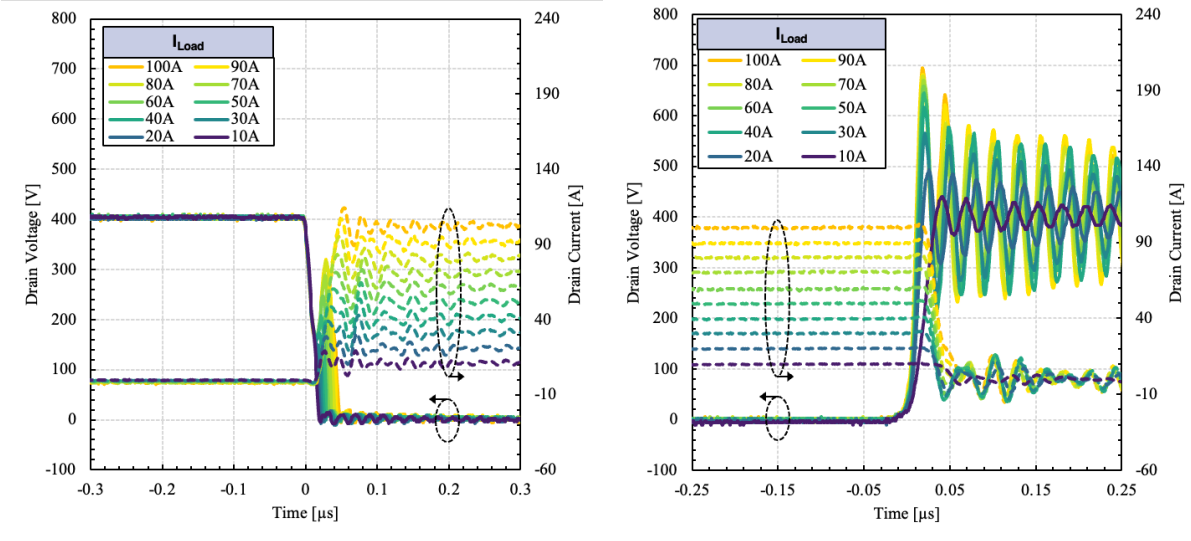


Fig. 8-6. Turn-on (left) and turn-off (right) switching waveforms of the HPS at different current levels. $T_{delay\text{-}on}$ = 0 µs, $T_{delay\text{-}off}$ = 1 µs, $R_{G(ON)\text{-}IGBT}$ = 15 Ω, $R_{G(OFF)\text{-}IGBT}$ = 4.7 Ω, $R_{G\text{-}GANFET}$ = 33 Ω, T_{amb} = 25°C.[40]

The device switches in unipolar mode via the GaN FET which results in sharp switching edges. The oscillation appearing in the turn-off cycle is attributed to the high-speed switching transition and parasitic inductances present in the measurement circuit and the device packaging. In the turn-on, during the voltage falling edge, a spike is also visible for the same reasons. The switching energy losses of the HPS at different load currents were extracted from

[40] Published in (10).

the measured data as presented in Fig. 8-7 along with the power loss contributions analysis as a function of switching frequency.

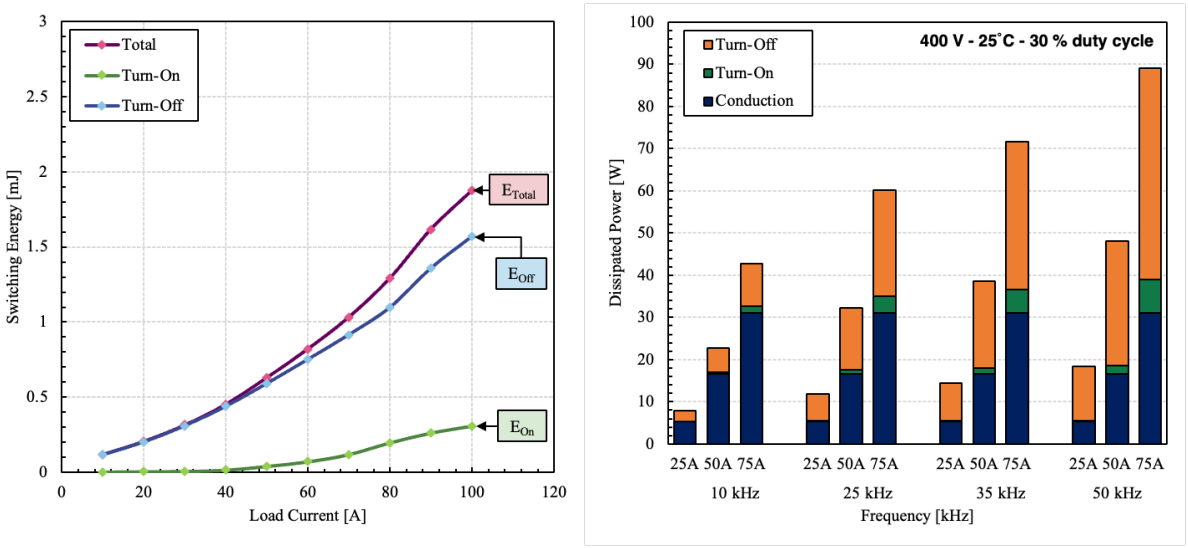


Fig. 8-7. Switching energy losses (left) and the power loss contribution of the HPS as a function of load current at different frequencies (right). V_{DS} = 400 V, T_{amb} = 25°C.[41]

The switching losses increase with the load current as expected. The turn-off losses are the dominant factor in the overall switching losses. For comparison purposes, two similarly rated devices of different technologies (Trenchstop IGBT [114] and CoolMOS [115]) were selected and experimentally evaluated under the same test conditions as the HPS. A comparison of the switching losses and the overall power losses contribution analysis of these devices with the proposed HPS are presented in Fig. 8-8.

[41] Published in (10).

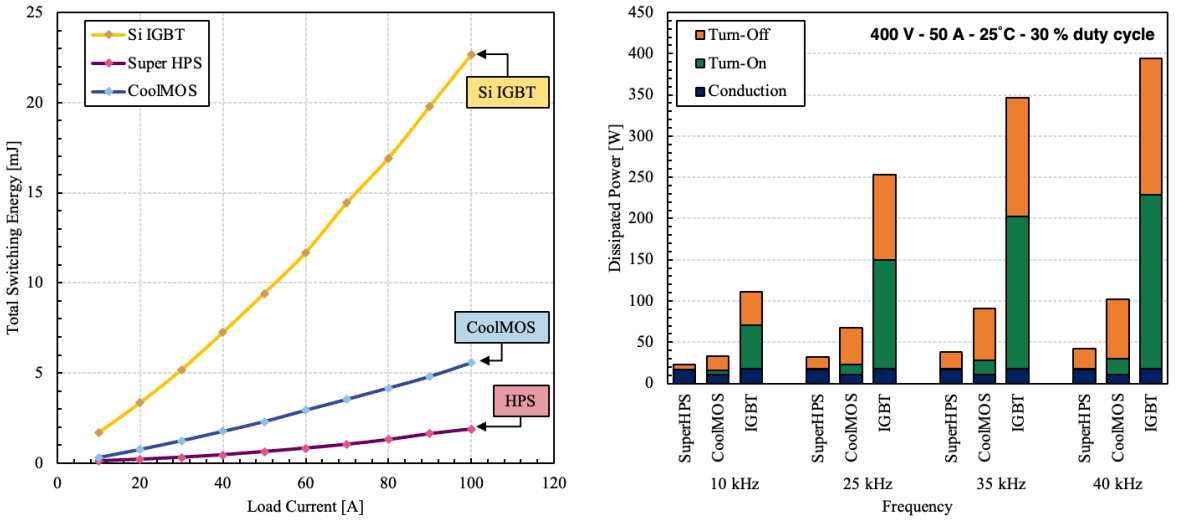


Fig. 8-8. Comparison of the total measured switching energy losses at different load currents (left) and contributions of power loss components as a function of switching frequency in the HPS and competitor devices (right). R_G = 33 Ω, V_{DS} = 400 V, T_{amb} = 25˚C.

As evident based on the results, the HPS achieves lower losses than both IGBT and MOSFET technologies. This advantage is attributed to the fast switching performance of the internal GaN FET combined with the high current capability of the IGBT. Therefore, the proposed solution can contribute to significantly smaller and more power dense power electronic design with high efficiency.

8.4 Chapter Conclusion

In this chapter, a new HPS concept consisting of the GaN, SiC, and Si technologies has been presented for the first time. The HPS exhibits very low power losses due to its unipolar switching mode as well as low conduction losses under varying load conditions thanks to the extremely fast switching of the GaN FET and the high current capability of the IGBT. Compared to conventional IGBT and MOSFET technologies, a significant reduction in power losses is observable due to the extremely fast switching of the GaN FET. A key advantage of the proposed configuration is its ability to withstand avalanche transients due to the addition

of the SiC diode which was selected to have a lower avalanche breakdown voltage, thereby protecting the device from detrimental surge voltage transients. Therefore, the GaN component of the HPS can be designed with a lower margin of breakdown voltage which simultaneously improves the on-resistance, switching performance and potentially costs. Overall, the HPS is a cost-effective solution for high power density and efficiency applications where optimal performance is required.

Chapter 9

Conclusions

This chapter presents a summary of the key findings and contributions of the work presented in this thesis. Subsequently, an overall conclusion is provided based on the previous chapters, collectively. Finally, the outlook for future research works is laid out and discussed.

9.1 Results of This Thesis

This thesis has explored and evaluated various aspects of power semiconductor device technologies for high power density and high efficiency power electronic applications. Power semiconductor devices are amongst the key building blocks of modern power electronics and their performance directly affects power density and efficiency. Increased switching frequencies result in smaller magnetic and capacitive components, leading to smaller form factors and reduced costs. However, the increase in switching frequencies adds to switching losses in power semiconductor devices, eventually reaching a maximum limit. Therefore, an understanding of device characteristics is an essential prerequisite that facilitates optimisation of the power semiconductor technologies.

In Chapter 2, the theoretical foundation of this research has been laid out. The device physics, operating principles, and various structures of GaN devices have been discussed in detail. The

key limiting factors of the existing device technologies have been identified. The inherently superior material properties of GaN enable the design of high voltage low resistance devices that are capable of operating at high frequencies. However, due to the long absence of native GaN substrates and difficulty in the processing, GaN devices are fabricated on foreign substrates such as silicon and sapphire in a lateral configuration, which are not as area efficient as vertical counterparts. One of their key limitations is the lack of avalanche ruggedness, which necessitates overdesigned devices with a large margin of breakdown voltage to prevent premature failure in case of transient surge voltage conditions. This large margin of breakdown voltage has led to an unnecessary increase in on-resistance and capacitance as well as design complexity and costs. This chapter also introduces the polarisation superjunction concept which aims to enhance the breakdown voltage for a given drift region. Additionally, the potentials of lateral GaN HEMTs have been discussed for applications requiring bidirectional power switches.

In Chapter 3, the performance of Schottky diodes utilising PSJ technology has been described for the first time. The static and dynamic characteristics of the device have been experimentally measured and the results are comprehensively discussed. A unique current saturation behaviour has been observed in the forward characteristics which is attributed to the short minority carrier lifetime and high bipolar on-set voltage in GaN heterostructures. Furthermore, the surge current capability of the PSJ GaN diode has been investigated and the results are compared with a SiC MPS diode of similar power ratings. It was found that PSJ GaN Schottky diodes, unlike SiC counterparts, do not exhibit bipolar conduction until failure. Additionally, these diodes can withstand high surge current events outperforming SiC counterparts. The findings of this chapter provide an in-depth insight into the device performance and can play a vital role in future developments of the technology.

Chapter 4 presents for the first time the performance of the 1.2 kV PSJ GaN HEMTs through comprehensive measurements of their static and dynamic characteristics. It has been shown that PSJ GaN devices with high breakdown voltage can be designed with small on-resistance because of the inherent material merits associated with GaN and the uniform distribution of electric field due to the simultaneous co-existence of positive and negative polarisation charges in a double heterostructure. Based on the UIS experimental data, it was determined that the device can withstand more than 3 kV before the onset of avalanche breakdown. The device demonstrated to have a wide range of dV/dt controllability which is achieved through adjustments of gate drive parameters. The ability to design large area GaN devices on low-cost substrates is one key factor in the success of the technology. However, one limitation of GaN devices that are currently available is their relatively low power handling capability. Specifically, in the context of high voltage devices, it is reasonable to assume a high current requirement. Despite this, the potential of the technology is evident based on the results.

Because of the normally-on nature of GaN switches, their widespread application has been limited. Cascode configuration is an effective solution to achieve normally-off mode of operation which enables the use of standard MOS compatible gate drivers. In Chapter 5, a 1.2 kV cascode GaN FET using the PSJ GaN HEMT presented in the previous chapter has been designed and experimentally evaluated for the first time. The device exhibits very low power losses under various conditions. In terms of dV/dt controllability, the cascode device switches at very high slew rates without any noticeable changes even when the gate resistance changes. Therefore, external circuitry and snubbers may be added if lower dV/dt is required. Additionally, the losses of the GaN FET were measured experimentally and compared with an IGBT of similar power rating. Subsequently, a SPICE model based on the measured characteristics was developed and used for a converter simulation. The simulation results also

show improvements in efficiency and power losses. Although the true breakdown of the GaN FET is over 3 kV, the device shows improvement in overall power losses compared to the IGBT which is attributed to the low on-resistance and faster switching of the GaN FET. Overall, cascode GaN FET technology is promising for a wide range of applications operating at high frequency and high efficiency.

Meanwhile, hybrid power switches combining unipolar and MOS bipolar device technologies exhibit near ideal device performance for their target applications which are primarily motor drives, traction inverters and EV markets. In Chapter 6, the operating physics and performance of a HPS utilising the latest SiC MOSFET and Si IGBT technologies have been investigated in detail. It has been demonstrated that utilising a proper gate drive strategy leads to a significant reduction in switching losses that can be as low as the constituent MOSFET while the device is capable of carrying at least twice as much current. The utilisation of HPS facilitates the development of more power dense, efficient designs, thereby reducing overall system costs and infrastructure outlay. With intelligent control, the switching frequency can be dynamically adjusted and optimised depending on the operating conditions. For example, under a low load regime where the IGBT is not in conduction mode, the operating frequency can be increased. The HPS concept is mainly suited for high voltage applications of above 650 V. At lower voltages, Si power MOSFETs offer superior performance and costs.

Further improvements in HPS can be achieved by replacing the constituent with superior technologies. Therefore, in Chapter 7 a novel dual gate HPS concept utilising trench CIGBTs instead of IGBTs has been presented. The physics and characteristics of trench CIGBTs have also been comprehensively and experimentally demonstrated. CIGBTs achieve increased power density by effective use of MOS-controlled thyristor action. CIGBTs also bring

additional advantages overcoming some of the shortcomings of IGBTs such as DA free operation which enhances reliability thanks to the unique self-clamping features. The significantly lower on-state losses and superior overall performance make CIGBTs suitable for integration in HPS applications. Overall, the HPS is particularly promising for various applications and especially for traction inverters where it can maintain high efficiency and low cost by utilising less SiC chip area.

Hybrid power switches commonly utilise Si and SiC technologies. In Chapter 8, for the first time, a HPS configuration employing cascode GaN FET, Si IGBT and SiC Schottky diode has been proposed. GaN switches have extremely high switching slew rates and can offer lower switching losses than SiC counterparts. As mentioned in the first part of this thesis, the lack of avalanche robustness is a key limitation of GaN devices which has necessitated a large margin of safety to mitigate surge voltage transients. In the proposed HPS, the SiC Schottky diode is selected to have a lower avalanche breakdown than other constituents. Therefore, under surge voltage transients, the voltage is clamped by the SiC diode, thereby protecting the switch. As a consequence, GaN FETs can be optimised for HPS integration which leads to significant improvements in on-state performance, lower switching losses and device cost. GaN based HPS can bring pivotal advantages for high power density and high efficiency power electronic applications.

9.2 Outlook and Future Works

Power semiconductor devices are continuously evolving to meet the demands for lower power consumption and higher current density. Transition to sustainable forms of energy will require significant improvement in power semiconductor technologies. The research presented in this thesis could form the basis of improvements and optimisations in the design of power

semiconductor device technologies. The following points are important areas of consideration for further research toward the development of power semiconductor devices.

9.2.1 Design optimisation in GaN HEMTs

GaN HEMTs exhibit high performance beyond the limit of conventional Si unipolar devices, duly facilitated by their inherent material characteristics. However, currently available lateral GaN HEMTs have generally lower current handling capability. Therefore, improvement in current handling needs to be prioritised for high voltage devices.

One of the key limitations of currently available GaN devices is the lack of avalanche withstanding capability which is one of the fundamental parameters that limits the performance for higher power density operation as these devices are designed with huge margins that adversely affect their performance. Therefore, it will be a key achievement in the design of avalanche rugged GaN devices whether by the design or by their heterogenous integration with other power devices such as HPS.

9.2.2 Hybrid Power Switches

Hybrid power switches bridge the performance gap between bipolar and unipolar device technologies. HPS can offer low cost and high performance simultaneously across various load conditions. Emerging technologies such as CIGBT and GaN FETs can offer greater performance and further reduction in costs. The improvement from the low power loss profile offered by the device also impacts the overall system cost in a positive way.

Further research can be done to understand the performance of Si IGBT to SiC MOSFET ratio in dual gate HPS especially from a reliability point of view. This is because during the delay period the entire current is handled by the SiC MOSFET which already is utilised for

handling light loads. Therefore, it is important to ensure the device operates within the safe operating area and reliably over the range of load conditions.

Short-circuit protection is a key design parameter for reliable and safe operation. In HPS, short circuit protection can be challenging due to different characteristics of the constituents. Therefore, an investigation into the suitability of existing protection mechanisms for HPS is necessary. Furthermore, research can be done to develop a dedicated scheme for these devices.

9.2.3 Packaging Improvement

In addition to semiconductor technology, improvements in packaging contribute significantly to device performance as power devices are getting more power dense and handling large power levels. The packaging technology is critical for improved thermal management, increased reliability, and insulation voltage as well as low inductances for high frequency devices. Additionally, in HPS packaging multiple semiconductor dies with different geometries and sizes can lead to additional complexity. Thus, further investigation into packaging technology is key to fully exploit the advantages and performance of these devices.

Appendix A

Summary of Power Semiconductor Switches

Bipolar Transistor basic three-layer PNP or NPN devices. A base current is required to control the collector current. BJTs key shortcomings include the need for a base drive current, negative temperature coefficient that gives rise to thermal instability if not managed properly, and poor current gain at high current densities.

Power MOSFET are unipolar devices characterised by their high switching speed. The drain current is controlled via the MOS channel. The current flow is facilitated by majority carriers. Resulting from the lack of carrier storage effect in the N drift, power MOSFETs can achieve high switching speeds. The on-state resistance is limited by drift region length and doping concentration.

HEMTs also known as Heterostructure FET (HFET) which incorporates materials with different bandgaps such as GaN and AlGaN. The control method depends on the gate structure. The on-resistance is limited by the length of the drift region, similar to power MOSFETs. Key challenges in HEMTs involve managing the lateral and vertical electric field, achieving normally-off behaviour, and lacking avalanche capability.

IGBT a MOSFET with a conductivity modulated drift region as an equivalent circuit. In the basic form, IGBTs have a MOSFET structure where the heavily doped N+ drain layer is replaced with a P or P+ collector. IGBTs offer low resistance and are suitable for high voltage medium to high power applications.

Thyristors have a four-layer NPNP structure. Under on-state, charge carriers are injected from the P and N regions. Thyristors cannot interrupt current flow by external control. These devices are primarily used for high power applications. Based on the thyristor concept, various devices including MOS controlled thyristors (MCTs) [116], Gate turn-off thyristors (GTOs) and emitter switched thyristors (ESTs) have been created.

Clustered IGBT is a new class of MOS controlled devices which exhibits thyristor-like on-state behaviour but without their limitations. CIGBTs are considered as a more efficient chip-for-chip IGBT replacement.

Table A-1. Summary of major power semiconductor devices.

Device	On-resistance	Switching frequency	Control mechanism	Conduction Type
BJTs	Medium	slow	Current gate	Bipolar
MOSFETs	High	Very fast	MOS Gate	Unipolar
GaN HEMTs	Medium-High	Very fast	Schottky, MIS*	Unipolar
IGBTs	low	Medium	MOS Gate	Bipolar
Thyristor	Very low	Very slow	Current gate	Bipolar

Appendix B

Simulation Model of PSJ GaN FET

In this section, the simulation model of the PSJ GaN FET that is used in Chapter 5 converter simulation is presented.

B.1 PSJ GaN FET SPICE Model

```
**********************************************************************
* ver 3.0, By Alireza Sheikhan
**********************************************************************
**********************************************************************
*****
* The model is an approximation of the device.
**********************************************************************
**********************************************************************
.subckt PSJ_GaNFET_TO247 drain gate source

*saturation current parameters
.param fsat1={30} fsat2={3.56} fsat3={2.26}

*on-state resistance parameters
.param frp1={1.09} frp2={6} frp3={2.90} frp4={0.487}

*reverse conduction (diode) mode parameters
.param frev1={30} frev2={0.67} frev3={0.7}

*parasitic capacitance parameters
.param fgd1={18}
.param fsd1={18}
```

```
.param fgs1={2800}

*Parasitic characteristics inductance and resistance of the device
Ls source 101 1.5n
Rls 101 S 0.01m
Lg gate 201 2.5n
Rlg 201 G 0.01m
Ld drain 301 1.5n
Rld 301 D 0.01m

*Leakage current paths represented by large resistances.
Rgs G S 1e8
Rgd G D 1e8
Rds D S 1e8

*Gate source capacitance
Cgs G S {fgs1*1e-12}
*Gate drain and drain source capacitance of the hemt
Csd1 S 105 {fsd1*1e-12}
Rdss 105 D 4
Cgd1 G D {fgd1*1e-12}

*Parasitic series resistances of source drain and gate.
Rs S S1 0.1m
Rd D D1 0.1m
Rg G G1 0.1m

*Saturation current function
.func Idsat(t) if(V(G1,S1) < fsat3, 0, if ( V(G1,S1) < fsat2,
fsat1*(V(G1,S1)-fsat3)/(fsat2-fsat3), fsat1))

*Resistance function
.func Rp(t) (frp1*((1/(1+exp(frp2*(V(G1,S1)-frp3))))) + frp4)

*drain source current as a function of drain/gate voltage
bchnl D1 S1 I = {if ( V(G1,S1) > fsat3, 2*Idsat(time)*((1/(1+exp(-
Rp(time)*V(D1,S1)))) - (0.5)), 0)}

*reverse (diode) current as function of drain source voltage
bdiode D1 S1 I = if ( V(D1,S1) < -frev3, -2*frev1*((1/(1+exp(-
frev2*(abs(V(D1,S1))-frev3))))-0.5), 0)
**********************************************************************
.ends PSJ_GaNFET_TO247
```

B.2 Current Voltage Characteristics

Based on the model presented above, the basic characteristics of the device were simulated to verify the approach. A comparison of the measured and simulated output characteristics and transfer characteristics are presented in Fig. B-1.

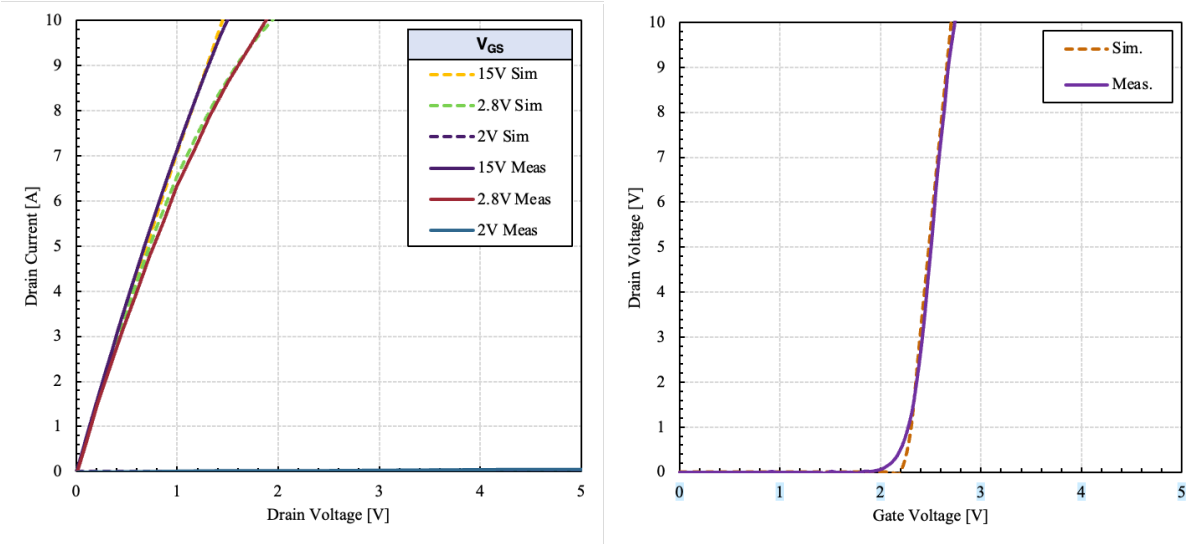


Fig. B-1. Comparisons of the measured and simulated output (left) and transfer (right) I-V characteristics. T_{amb} = 25˚C.

The slope of the output I-V characteristics determines the on-resistance of the device. As it can be observed a good fit between the measured and simulation data has been achieved. The measured and simulated transconductance and threshold voltage also show a good match. The measured and simulated reverse diode I-V characteristics of the device are presented in Fig. B-2.

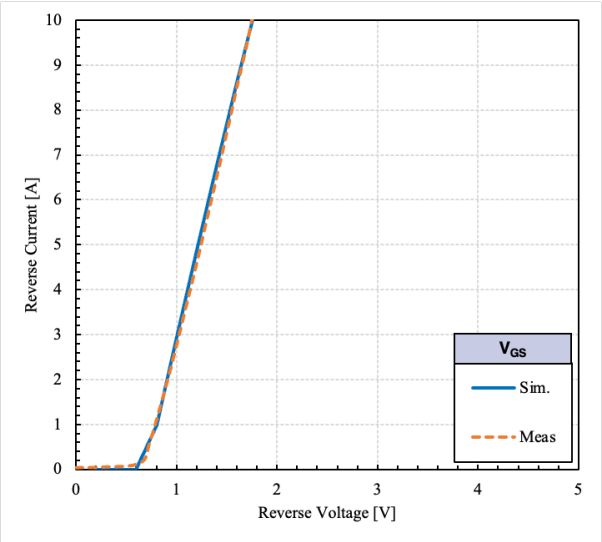


Fig. B-2. Comparisons of the measured and simulated reverse (diode) I-V characteristics. T_{amb} = 25˚C.

A good fit between the measured and simulated data is also observable for the diode characteristics.

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