# Modularized Partial Power Processing DC–DC Converters

**Yuwei Liu**

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# Abstract

The partial power processing (PPP) technique for power converters is widely used in renewable energy, electric vehicles, and dc microgrids due to its high power density and efficiency. Conventional PPP topologies are typically designed for either photovoltaic strings or two dc ports, with this research expanding the latter. The existing PPP two-port scheme connects one dc–dc converter port in series between the source and load, allowing only partial power to be processed while the rest is delivered directly, reducing converter size and power losses. However, existing two-port PPP schemes are limited in handling complex, multiport, or buck-boost applications.

This thesis extends the basic PPP two-port design by introducing modular PPP topologies. It splits the isolated dc–dc converter into two modules: one series-connected between the source and load, and the other parallel to either the source or load. The series and parallel modules handle partial power caused by voltage and current difference between the source and load. A general derivation principle is proposed for PPP multiport structures, requiring at least one series-connected module for each pair of dc ports and one parallel-connected module for all the dc ports, ensuring voltage and current balance. Based on this principle, nine PPP three-port dc–dc structures are derived, with a methodology for selecting the appropriate topology for specific applications.

The thesis also presents a PPP single-input/output N-outputs/inputs dc–dc converter with N+1 radial connection modules. A single-input dual-output converter with active bridge modules is constructed and measured. Additionally, a novel T-shaped PPP buck-boost dc–dc converter is proposed, featuring a central parallel module for intermediate voltage regulation and two series modules with opposite polarities for buck-boost operation. This design allows for buck-boost operation within a narrow voltage gain range without polarity reversal. Experiments validate the theoretical analysis of both the three-port and buck-boost converters.

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# Acknowledgement

Too be honest, my journey through the PhD process has been far from smooth. From the isolation of quarantine during the pandemic to changing supervisors, I've experienced some of the lowest points in my trust in people. In my research, I also have to spend an entire year building an experimental platform from scratch. I often felt anxious about slow progress, constantly battling self-doubt, but in the end, I've emerged as a better version of myself.

Looking back, those negative emotions have faded into the background, replaced by a deep sense of gratitude for the many people who supported me along the way.

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# Declaration

I declare that this thesis is a presentation of original work, and I am the sole author. This work has not previously been presented for a degree or other qualification at this University or elsewhere. All sources are acknowledged as references.

The following publications have resulted in part of this work:

## Publications:

- Y. Liu, Y. Hu, G. Chen and H. Wen, "Partial Power Processing Multiport DC–DC Converter with Radial Module Connections," *IEEE Trans. Power Electron.*, vol. 37, no. 11, pp. 13398-13412, Nov. 2022.
- Y. Liu and G. Chen, "A Partial Power Processing Buck-Boost DC-DC Converter Without Polarity Reversal," in *IECON 2023- 49th Ann. Conf. of the IEEE Ind. Electron. Soc., Singapore*, 2023, pp. 1-6.

## Publications Planned:

- "Principle and Topology Derivation of Partial Power Processing Three-Port DC-DC Converters" based on the content of Chapter 2.
- "Integrated Partial Power Processing Three-Port DC-DC Converter" based on the further work.

Yuwei Liu

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# Chapter 1

# Introduction

## 1.1 Research Background and Motivation

Due to the concerns about the non-renewable energy systems, sustainable power sources and the rational use of the electric energy are of increased interest [1-3]. Since energy is clean and easy to transmit electrically, it has become the first choice for converting renewable energy such as solar energy, wind energy, and hydropower into secondary energy [4-7]. The corresponding storage systems and loads also developed during the last years [8-11]. This trend is forcing power distribution grids toward more complex architectures capable of interconnecting the increasing number of decentralized energy sources and handling the increasing electrical power demand.

AC systems are well-established globally with extensive infrastructure and compatibility, because AC can be easily stepped up to high voltages using transformers, reducing energy losses over long distances. In addition, AC generation, transmission, and distribution are generally cheaper due to mature technology and economies of scale. However, with the development of renewable energy sources like solar panels produce DC, traditional AC systems require inverters to convert DC to AC, reducing overall efficiency. Moreover, many modern devices and energy storage systems require DC, necessitating AC–DC conversion, which results in power losses. Furthermore, the AC systems require precise frequency and phase synchronization, which can complicate grid stability. Facing renewable DC sources, DC loads, and DC storages, a DC system eliminates the need for conversions between DC and AC, improving efficiency. Since DC systems can bypass several conversion steps, they may require fewer components, such as transformers and converters, reducing both initial setup costs and maintenance demands. In addition, DC systems can offer improved stability for certain applications because they do not suffer from problems related to frequency stability and phase synchronization necessary in AC systems. While DC systems face challenges in long-distance transmission due to the high cost

of voltage converters, they show great potential in regional power grids powered by renewable energy sources. This has led to growing research interest in DC microgrids [12-14]. In order to handle and connect the various dc elements in a microgrid, dc–dc converter technology plays an important role and has been widely researched by scholars at home and abroad [15, 16].

Given the high power processed through the dc–dc converters in these microgrids, increasing the power density and reducing the power losses by decreasing the power level of the converter are critical. To achieve this, the concept of partial power processing (PPP) is proposed for dc–dc converters which is intended to process only a part of the total power flowing between the two dc ports which it is interconnecting, and the rest of power is delivered directly [17, 18].

Since only a portion of the total power is processed by a PPP converter, most of the power flows directly from the input to the output without passing through a conversion stage. The efficiency of the PPP converter applies only to the part of the power that is processed by the converter, since only the processed power can be subject to conversion losses. Accordingly, the efficiency of the total system is not directly decided by the efficiency of the converter like that of full power processing converters, but is only partially dependent on it, allowing then for a higher overall system efficiency. Moreover, the introduction of PPP brings a voltage/current reduction of the applied converter, so lower rated components can be used. This extends the range of components which are suitable for the application, while downsizing converters, resulting in more cost-effective solutions.

Due to the aforementioned advantages, PPP has become a topic of interest [19-24], allowing dc microgrids in renewable systems to be more competitive with their non-sustainable counterparts. However, the existing PPP converters are more commonly applied to two-port structures or the series-connected multiport applications. In this thesis, to meet the demand of the market scalability request, it is expected to be expanded to more PPP-based structures such as multiport and buck-boost. The expansion is achieved by exploring the essence of PPP that PPP is rather to process the partial power caused by voltage and current difference between the source and load than to simply modify the connection between a two-port dc-dc converter and the source and load. By following this essence, multiport and buck-boost structures can be derived.

## 1.2 Concept of Partial Power Processing

The concept of PPP is proposed that there is a part of the power that will be delivered directly at an efficiency of 100% if the conduction losses of the cabling are ignored, while another part will be transmitted by the converter at an efficiency $\eta_c$, which is smaller than 100%. According to this, the schematic diagram of PPP concept is shown in Figure 1.1. By combining the efficiencies of the converter and the direct power path together, the global efficiency $\eta$ of PPP scheme must be larger than $\eta_c$, which is improved when compared with the traditional method of processing the full power through the dc–dc converter. The concept of PPP was firstly applied to realize maximum power point tracking (MPPT) and battery charging for a standalone photovoltaic (PV) power system, as shown in Figure 1.2 [17]. From Figure 1.2, a capacitor is added in series with PV array and battery bank, and the power electronic converter is applied to only regulate the capacitor voltage to control the PV output voltage and realize MPPT. The capacitor voltage, which is one port voltage of the converter, only represents the voltage difference between the PV array and battery, and another port of the converter only processes the current difference. In this connection, only the partial power will be converted from the PV array to the battery, while the rest of the PV power will be supplied directly to the battery. A clearer demonstration of the directly power delivery path as the series boost units is given in [18], as shown in Figure 1.3. Unlike the traditional full power converter (FPC) whose input and output ports are both connected in parallel with the source and the load, in the PPP scheme in Figure 1.3, one port of the dc–dc converter is changed to be connected in series between the source and load and the other remains in a parallel connection. The connection between Figure 1.2 and Figure 1.3 are similar, and a direct power delivery path can be seen clearly in Figure 1.3. Moreover, from Figure 1.3, the dc–dc converter only processes the current/voltage difference between the source and load in this arrangement, which successfully reduces the power handling requirement of the converter. Due to these advantages, PPP is an attractive technique which is classified into two main categories.

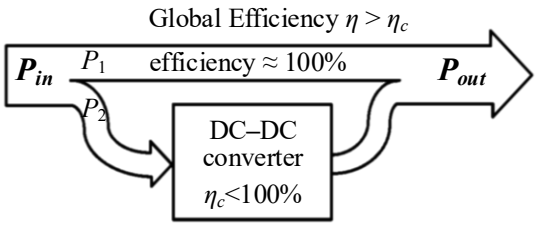



Figure 1.1 Schematic diagram of PPP concept.

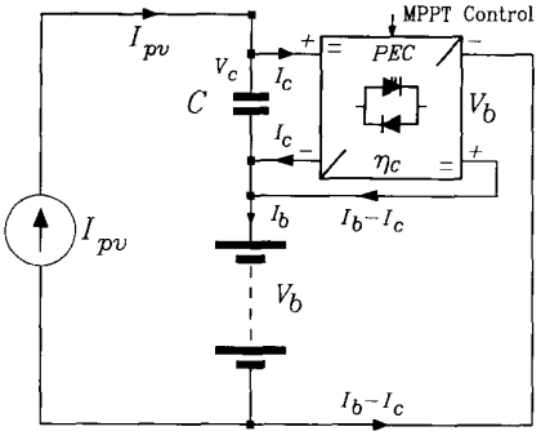



Figure 1.2 Novel MPPT, employing a capacitor in series with PV array and battery from [17].

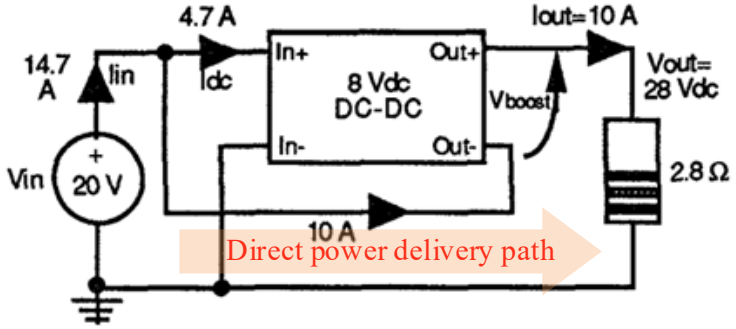



Figure 1.3 A series connected boost unit, showing the output port of the dc–dc converter is connected in series between $V_{in}$ and $V_{out}$ from [18].

The first type is differential power processing (DPP). It is used to process the mismatched power among the multiple series connected ports in applications such as solar energy generation systems [25-31], thermoelectric generation systems [32-34], and data centres [35, 36]. For example, the power available from PV panels in a string will fluctuate due to uneven lighting, causing the power mismatching among the panels. To balance the mismatched power, the DPP converters are applied to only process the differential power caused by the current difference among the series connected PV panels, so that the PV panels can be connected with a matched string current.

The second type is PPP, in which two ports of an isolated dc–dc converter are respectively parallel or series connected with source and load, is shown in Figure 1.3. From Figure 1.3, although the voltages of the source and load are 20 V and 28 V, respectively, the output voltage of the dc–dc converter only equals to their voltage difference, which is 8 V. Similarly, the input current of the dc–dc converter equals to 4.7 A, which is the difference between the source and load currents. In this way, only the partial power caused by the voltage difference and current difference between the source and load, which are respectively 8V×10A=80W and 20V×4.7A=94W will be processed by the isolated dc–dc converter. Compared with the total power, which is the sum of the input and output power 20V×14.7A+28V×10A=574W, the partial power processed by the converter is only 174W, and the rest part is delivered directly. The power loss of the converter is 94W−80W=14W, so the efficiency of the converter is 80W÷90W=85.1%, while the global efficiency of the PPP system is 280W÷294W=95.2%. Compared with DPP, the partial power of the PPP comes from the voltage and current difference between two independent dc ports rather than the mismatched power among multiple series connected dc ports.

## 1.3 Differential Power Processing Structures

In a PV power systems, the PV panels, sub-panel strings, or individual PV cells are connected in series to obtain higher voltages for later stage applications [37-39]. However, if even a small part of PV elements is prevented from generating power due to the partial shading, dust accumulation, or cell degradation, the generation power of the PV system is decreased disproportionately. This greater than expected decrease occurs because PV elements which do not receive adequate light cannot operate on the normal operating point, but rather operate as loads because they will operate in the reverse bias region and consume power. To solve the power mismatch in PV strings and avoid this severe power decrease, individual converters are connected to each of the PV elements [40-44], as a dc optimizer, as shown in Figure 1.4. This can help achieve MPPT for each of the PV elements by processing the full PV power, which is referred to as full power processing (FPP). Although FPP converters are effective against mismatch, the corresponding losses are proportional to the produced PV power, which is inefficient. To improve it, a method that has lower power losses has been introduced, i.e.,

differential power processing.

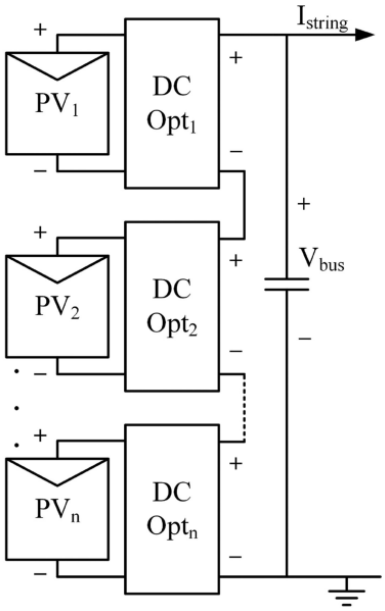



Figure 1.4 PV system using dc optimizers for each PV panel [44].

DPP converters only process the mismatch power between a PV element and adjacent elements, while maintaining individual control of the PV elements. Therefore, less power will flow through the DPP converter, and the power loss can be reduced when compared to the FPP scheme. According to different objects the PV elements is connected to via the DPP converters, the corresponding DPP architectures can be further divided into PV connected to bus [45-51], PV connected to PV [46, 52-61], and PV connected to virtual bus [62-65].

By connecting each PV element to the system bus with a DPP converter, as shown in Figure 1.5, the DPP converters can supply or remove the current for maximum power point operation of the PV element [45-49]. To implement this architecture, the flyback converter [45], bidirectional flyback converter [46, 47], stacked LLC resonant converter [48] and multi-stacked SEPIC converter [49] are used for DPP converters. In [50, 51], an extra string converter is added to control the PV string current so that the bus string current and the PV string current can be decoupled.

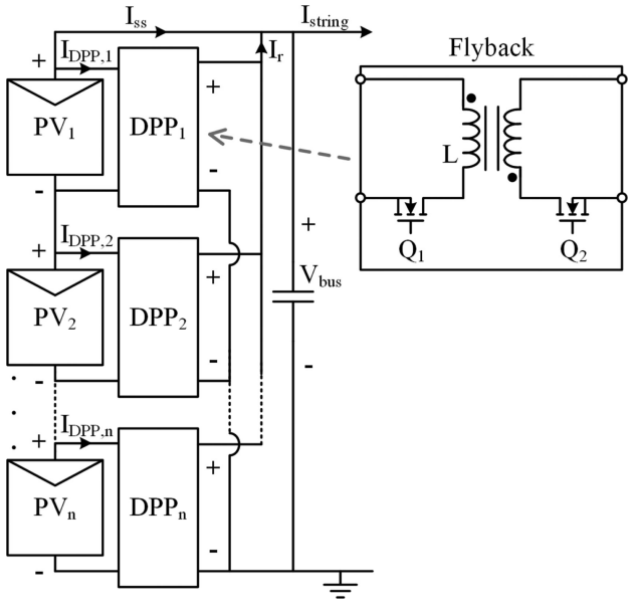



Figure 1.5 Series DPP PV-bus architecture with flyback converters [44].

In PV-PV architecture, the DPP converter is connected between two adjacent PV elements, as shown in Figure 1.6. It is used to process the mismatch current between two PV elements, thereby achieving MPPT. For this architecture, the bidirectional switched-inductor is commonly used [46, 52-57]. In addition, the resonant switched-capacitor converter is also used [58-61], which allows soft switching over a wide operating range.

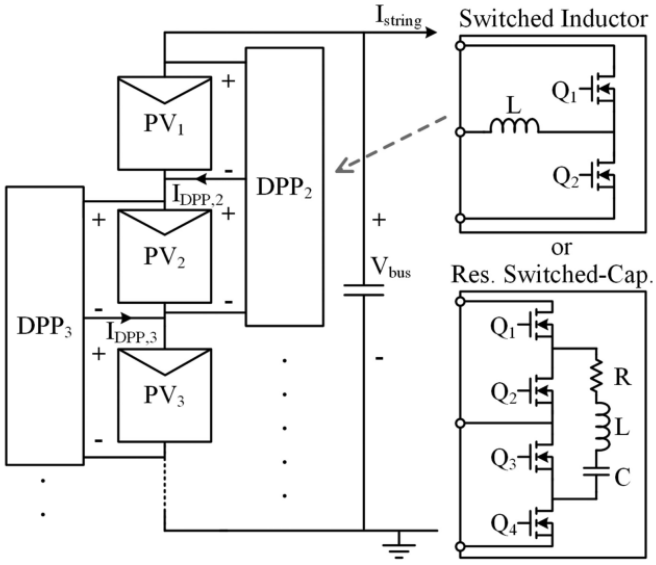



Figure 1.6 Series DPP PV-PV architecture with switched inductor or resonant switched-capacitor converters [44].

In the PV to virtual bus architecture, also called PV to isolated port, DPP converters are used to connect PV elements to an independent isolated port, or a virtual bus [62-65], as shown in

Figure 1.7 In this connection, the power of PV elements can be delivered to or from the virtual bus to achieve MPPT. The power flowing through the virtual bus must be balanced that the sum of the power must equal to zero.

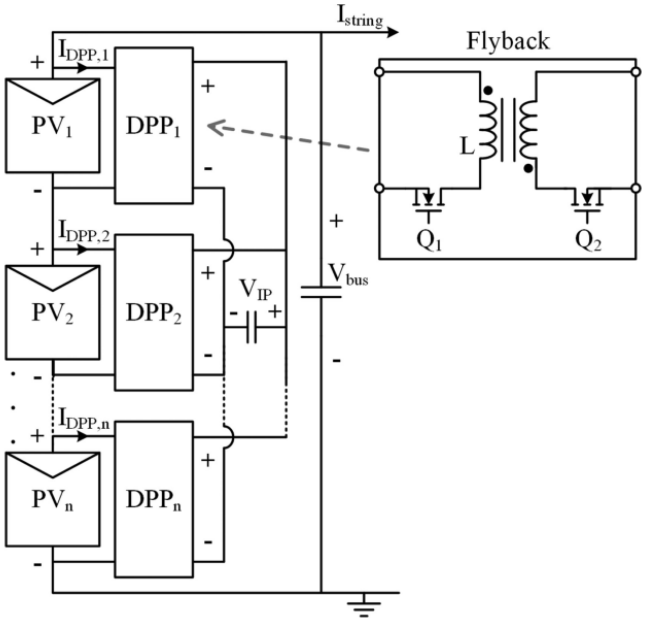



Figure 1.7 Series DPP PV-Isolated Port architecture with flyback converters [44].

# 1.4 Partial Power Processing Structures

Compared to the DPP scheme that processes the mismatch power in series-connected multiport applications, such as PV strings, PPP aims to process the partial power caused by voltage/current difference between two individual dc ports. One of the typical PPP structures can be found in Figure 1.3 [18], where the output port of the dc–dc converter is series connected between the positive terminals of the source and battery, and the input port of the dc–dc converter keeps the parallel connection with the source. In this connection, the input current of the dc–dc converter is equal to the current difference between the source and load, and its output voltage is only the voltage difference. Therefore, the power flowing through the dc–dc converter is only the partial power, and both the voltage and current handling requirements of the converter are reduced.

### 1.4.1 Typical PPP Two-Port Structures

Although the PPP structure in Figure 1.3 only shows a boost solution, the PPP structures can be further expanded to four typical PPP two-port dc–dc structures by changing the connections and polarities of the dc–dc converter [66, 67], as shown in Figure 1.8.

It can be seen from Figure 1.8, the connections between the input/output ports and the dc–dc converter are flexible. In Figure 1.8(a), node *a* is connected to node *d*; therefore, port *cd* is in series connection between the input port and output port, and port *ab* is in parallel with input port $V_i$. This structure is named as input-parallel output-series (IPOS). Similarly, node *ab* is connected in series between the input and output, and node *cd* is connected in parallel with output in Figure 1.8(c), constructing the input-series output-parallel (ISOP) structure. Moreover, considering the buck and boost functions, four typical four typical PPP two-port dc–dc structures can be derived. These are IPOS step-up, IPOS step-down, ISOP step-down, and ISOP step-up. In addition, in Figure 1.8, the positive and negative nodes of the input port of the dc–dc converter

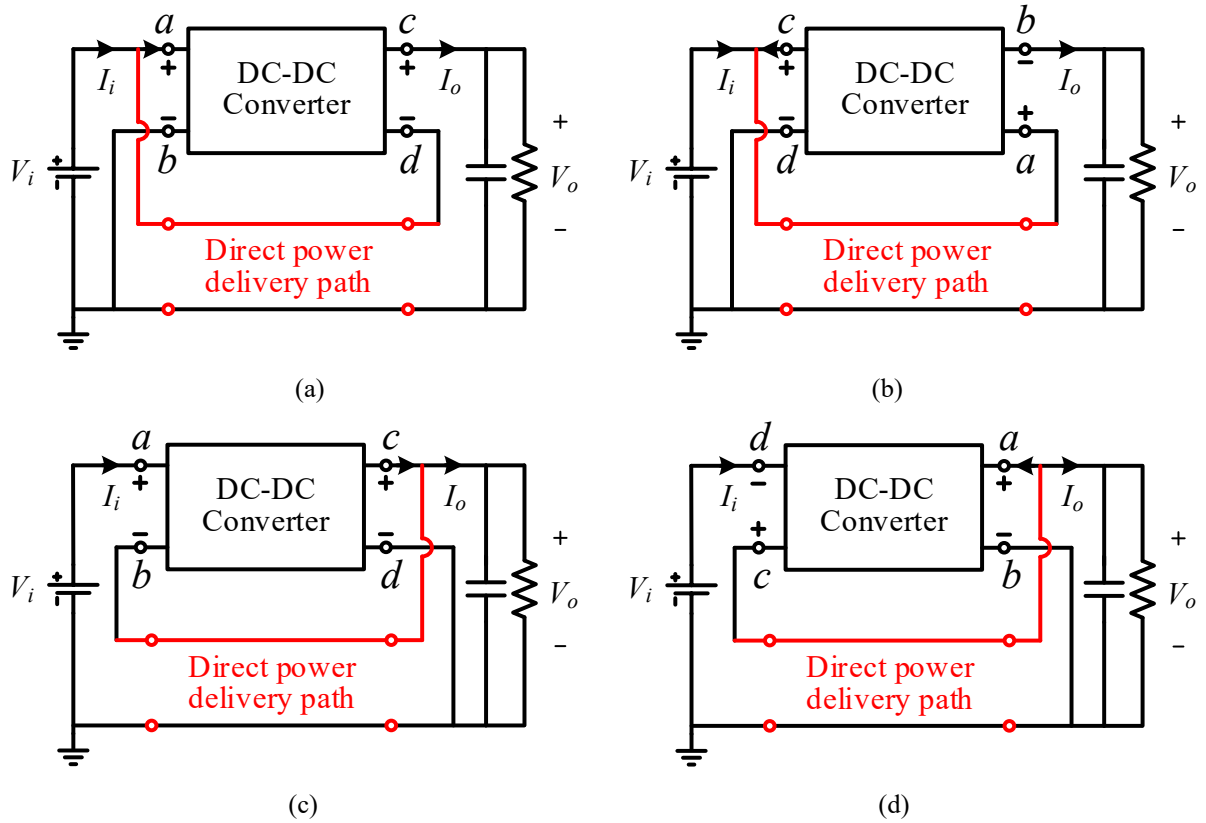



Figure 1.8 Four typical PPP two-port dc–dc structures. (a) Input-parallel output-series step-up. (b) Input-parallel output-series step-down. (c) Input-series output-parallel step-down. (d) Input-series output-parallel step-up.

are designated as $a$ and $b$, respectively, and that of the output are $c$ and $d$. Take Figure 1.8(a) as an example, according to the voltage relationship, $V_i$ is lower than $V_o$, so the corresponding current $I_i$ is larger than $I_o$, and the current difference $I_o$–$I_i$ will flow into the positive node $a$. Therefore, the left port of the dc–dc converter is input. Similarly, when the polarity of series-connected port is reversed in Figure 1.8(b), the current difference will flow out of node $c$, so the left port of the dc–dc converter is output in Figure 1.8(b). The input and output ports of the dc–dc converter can be determined in the same way in Figure 1.8(c) and (d).

Based on these four typical PPP structures, a variety of PPP two-port dc–dc converters have been explored by using different isolated dc–dc converters, such as push-pull converters [68, 69], where a three-winding transformer is used for the push-pull forward converter in Figure 1.9 [68], phase-shifted full/half-bridge converters in Figure 1.10 [70-75], flyback converters in Figure 1.11 [76-80], LLC converters in Figure 1.12 [81, 82], and dual active bridge (DAB) converter in Figure 1.13 [83-86]. According to the polarity of the series-connected port of the dc–dc converter, the topologies in [68, 70-72, 83, 84] are able to realize voltage step-down, while voltage step-up is achieved in [69, 73-82, 85, 86]. The voltage step-up or step-down depends on the polarity of the converter port which is series-connected between the source and load.

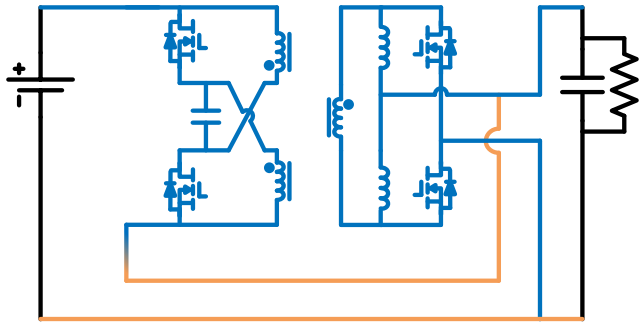


Figure 1.9 PPP two-port dc–dc structure using push-pull forward converter from [68].

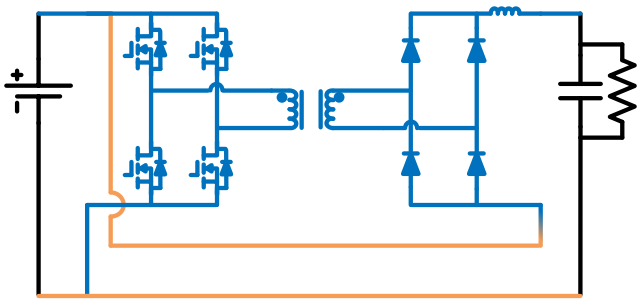


Figure 1.10 PPP two-port dc–dc structure using full bridge converter.

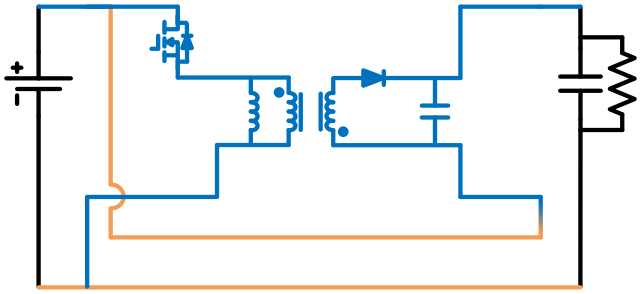


Figure 1.11 PPP two-port dc–dc structure using flyback converter.

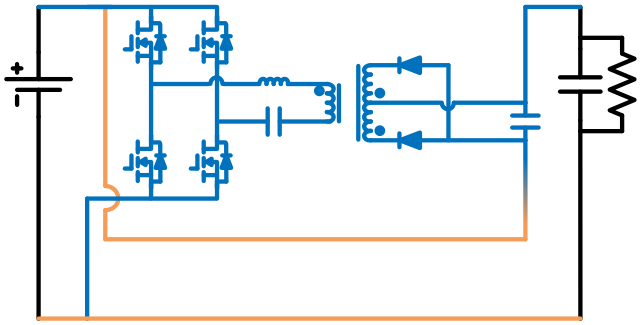


Figure 1.12 PPP two-port dc–dc structure using full bridge LLC converter.

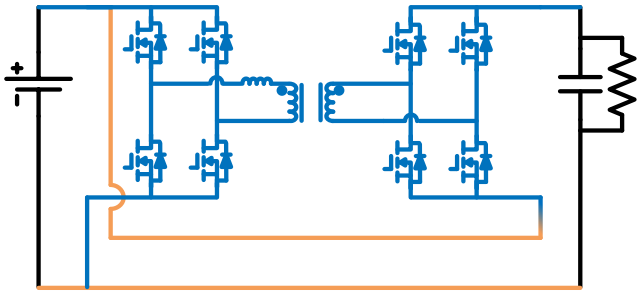


Figure 1.13 PPP two-port dc–dc structure using DAB converter.

## 1.4.2 PPP Multiport DC–DC Structures

Considering the applications with multiple dc ports such as renewable energy storage systems [87, 88], electric vehicles [89, 90], and electric aircrafts [91-93], the multiple dc ports are connected by multiple two-port dc–dc converters to achieve conversion of different voltage levels in traditional method. The use of multiple dc–dc converters causes large system size and cost. To reduce the number of components and obtain higher power density, multiport dc–dc converters are investigated to better integrate them together. Given the aforementioned advantages of PPP, several authors have developed PPP multi-port dc–dc converters. In [94, 95],

PPP is used for electric vehicle (EV) charging, as shown in Figure 1.14. The isolated FPP three-port dc–dc converters can be either triple active bridge (TAB) converter [94] or triple active half bridge converter [95]. By applying the typical PPP two-port structure, the power transmission from battery storage system to EV is PPP. However, PPP only exists between two ports rather than three ports, which is not optimal.

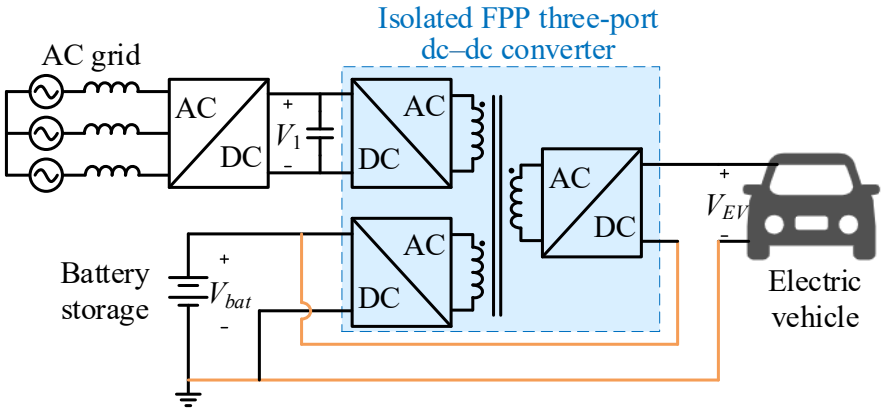



Figure 1.14 Configuration of electric vehicle charger with integrated battery storage system using PPP structure.

In [96, 97], the three-port converters draw on the concept of PPP, which is the reduction of the current or the voltage by connecting the ideal ports in parallel/series, respectively. For example, in [96], as shown in Figure 1.15, the battery $V_{bat}$ is charged by both high voltage $V_H$ through the two-port dc–dc converter and low voltage $V_L$, rather than only the high voltage $V_H$. Therefore, the current stress of the two-port converter is decreased. However, the low voltage port $V_L$ is actually directly in parallel connection with the battery $V_{bat}$, which means only two rather than three voltages are regulated independently. Therefore, although three ports $V_H$, $V_L$ and $V_{bat}$ are presented, it cannot be defined that PPP is realized among three independent dc ports. Similarly, the three-port converter in [97] uses one coupled inductor (CI) and two CI-based voltage multipliers, and the CI-based voltage multipliers are connected in series with the output voltage. So, facing the high voltage gain, the voltage stresses of the corresponding semiconductors can be reduced. Nevertheless, the input and battery are connected in series, and PPP is only achieved between their sum and the output voltage, so it still cannot be defined as a standard three-port PPP structure.

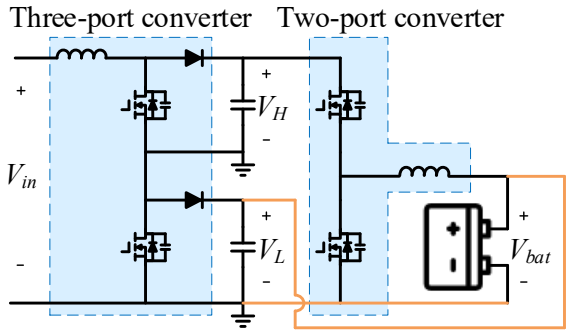



Figure 1.15 Three-port converter combining PPP, realizing current stress reduction.

The typical input-parallel-output-series PPP structure is flexibly combined with three-port dc–dc converter in [98, 99], as re-drawn in Figure 1.16(a) and Figure 1.16(b), respectively. As can be seen in Figure 1.16(a), the isolated three-port in blue rectangle frame, regarded as two isolated modules, is connected in typical input-parallel-output-series PPP structure. Nevertheless, there is no PPP function when the power flows between the PV panel and the battery. Similarly, the isolated Sepic converter is also applied with the typical PPP connection as shown in Figure 1.16(b). However, the PPP function is only activated under surge loading, and the isolated Sepic converter will only process the partial power between the supercapacitor $V_{sc}$ and the output port $V_{out}$.

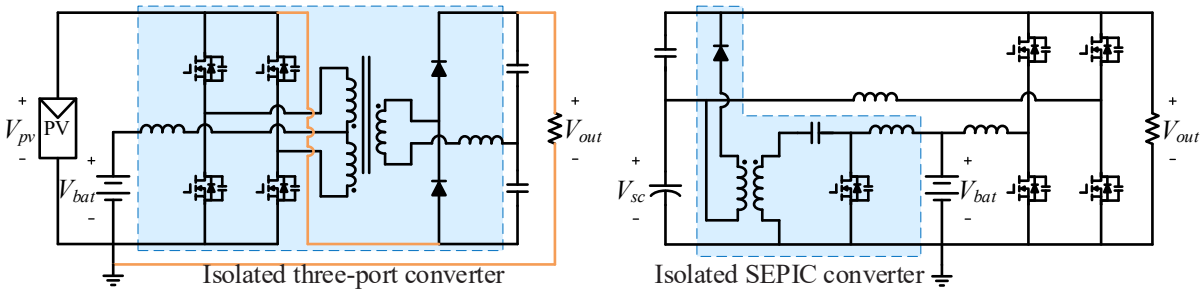



Figure 1.16 Three-port converter combining typical input-parallel-output-series PPP structure. (a) [98]. (b) [99].

The above converters have made some attempts to combine multiport with PPP and have maintained the advantages of PPP to a certain extent. However, although three dc ports are presented, some are not independently regulated. Alternatively, in the most of existing PPP three-port topologies, the reduction of current/voltage stresses brought by typical PPP connection is only achieved between two of the three ports. In addition, they only give a very limited number of PPP three-port topologies with the specific structure, which cannot meet the needs for practical applications.

### 1.4.3 PPP Buck-Boost DC–DC Structures

In a general PPP two-port scheme, one port of the FPP dc–dc converter is changed to be connected in series between the source and load, and the other port remains in a parallel connection. However, the polarities of the series-connected port voltage are fixed, which means the derived two-port partial power converters (PPCs) cannot be buck and boost. This is not applicable for its introduction into applications such as electrical vehicle [100-102], DC microgrid [103, 104], where output voltages vary and can be lower or higher than input. To realize PPCs capable of voltage step-up and step-down and expand their application areas, previous researchers have tried to make the series-connected port voltage bi-polar [105-118], or used two-stage step-up/down PPCs [119, 120].

#### 1.4.3.1 Polarity reversal schemes

To realize polarity reversal of the series-connected port, which is named as $V_s$ in Figure 1.17, thereby achieving a buck-boost PPC, one of the main methods is adding extra switches in series connection with the original semiconductors in the isolated modules of the FPCs. The bi-polar FPCs can be derived from full-wave centre-tapped [105-107], half bridge [107], full bridge

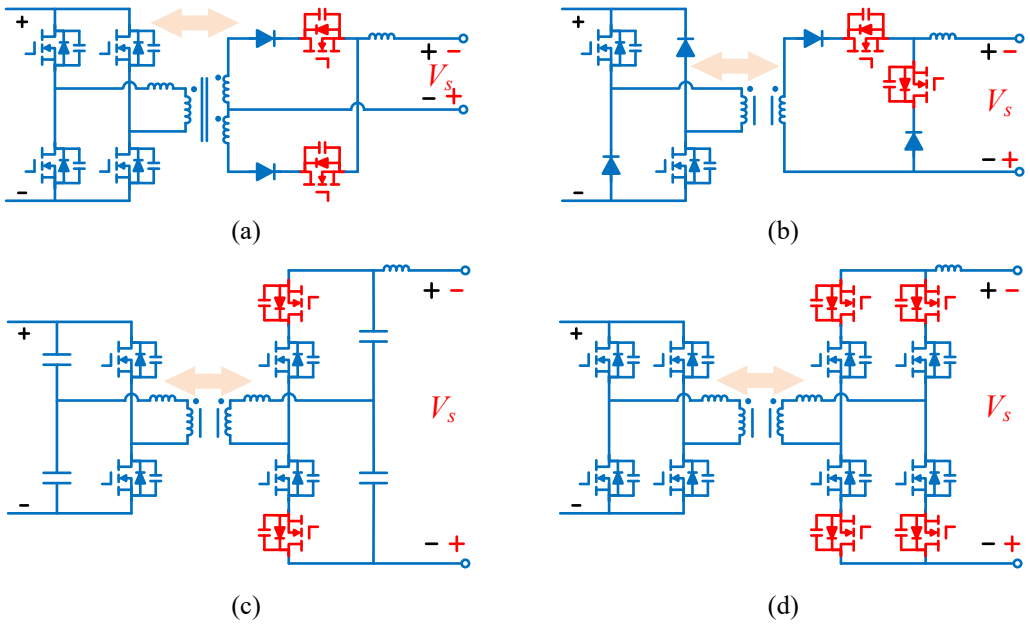
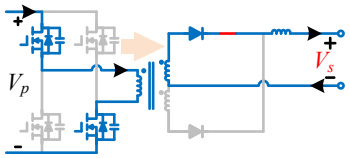
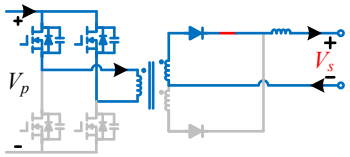


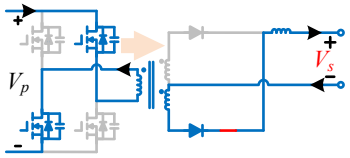

Figure 1.17 Bi-polar isolated FPCs with extra switches. (a) Push-pull converter. (b) Forward converter. (c) Half-bridge converter. (d) Full-bridge converter.



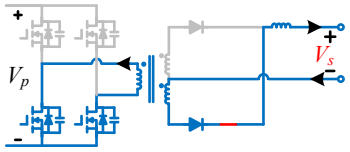

(a) state 1




(b) state 2

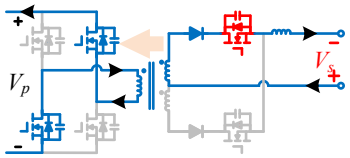



(c) state 3

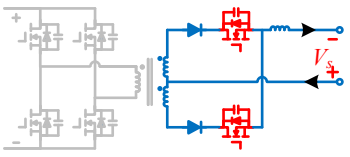



(d) state 4

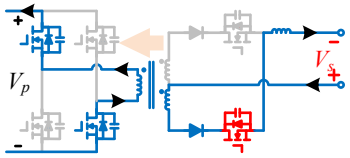
Figure 1.18 Operational equivalent circuits of the bi-polar push-pull converter when $V_s$>0.



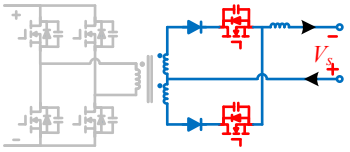

(a) state 1




(b) state 2




(c) state 3



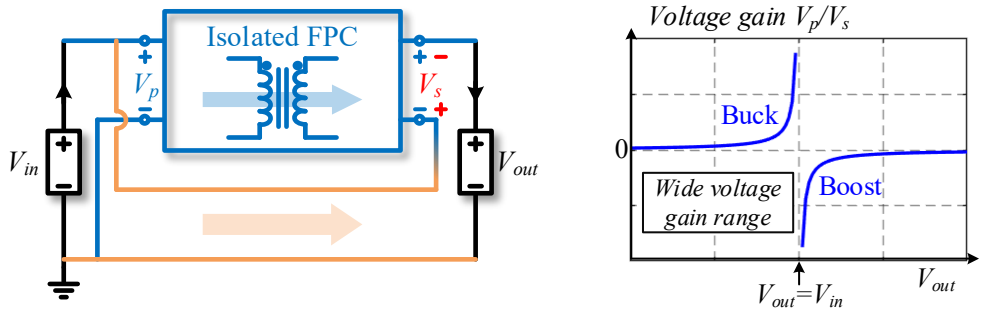

(d) state 4

Figure 1.19 Operational equivalent circuits of the bi-polar push-pull converter when $V_s$<0.

[108-111], active bridge [112, 113], and forward converter [114], as shown in Figure 1.17 (a), (b), (c) and (d), respectively. From Figure 1.17, the base circuits are illustrated in blue, while the additional switches are highlighted in red for enhanced clarity. After adding the extra switches, the ports voltage $V_s$ can be reversed.

To better illustrate how the added switches help reverse the polarity, the push-pull converter in Figure 1.17(a) is taken as an example. Its operational equivalent circuits for conditions where $V_s$>0 and $V_s$<0 are shown in Figure 1.18 and Figure 1.19, respectively. In these illustrations, components that are inactive in their respective operational modes are indicated by gray markings. From Figure 1.18, the added switches remain turned on, functioning similarly to a regular wire, and is therefore represented by red lines in the mode of $V_s$>0. In this mode, $V_s$ acts as an output port. By contrast, from Figure 1.19, the polarity of $V_s$ is inverted through the coordinated control of the additional switches, while the current direction remains consistent. This enables power to flow from $V_s$ to $V_p$. The operational principles are similar for the other bi-polar FPCs in Figure 1.17.

However, in the polarity reversal scheme with the help of added switches, as the output voltage changes from lower to higher than the input voltage, the corresponding series-connected port voltage $V_s$ will decrease to zero and then increase in the opposite direction. Take the input-parallel-output-series step-up PPC in Figure 1.20(a) as an example, its voltage relationship is $V_{out} = V_p+V_s$, where $V_p = V_{in}$. With output voltage $V_{out}$ increases from buck to boost, the voltage gain of the corresponding FPC is then drawn in Figure 1.20(b). From Figure 1.20(b), as the output voltage $V_{out}$ approaches the input voltage $V_{in}$ infinitely, the voltage gain will theoretically tend to infinite. Accordingly, the voltage gain of the FPC will vary over a wide range when the output voltage needs to be regulated continuously between buck and boost, such as self-regulating power supplies, PV chargers, and adaptive control applications. Within a wide voltage gain range, the performance degradation of the FPC is inevitable. For example, when applying a conventional LLC converter, its switching frequency range will be extra wide if it is deployed in wide gain range applications. This leads to drawbacks of constrained soft switching range, increased core size of transformer, and limited light-load regulation ability [121-123]. For a DAB converter, when the turns ratio of the transformer is fixed, the wide voltage range application leads in unmatched voltage gain, which will result in a drop of efficiency due to hard switching and large circulating current [124-127].




(a) (b)

Figure 1.20 The example buck-boost PPC and its voltage gain range. (a) Input-parallel-output-series buck-boost PPC. (b) Voltage gain range of the corresponding FPC.

Another method to reverse the polarity is adding an H-bridge circuit after $V_s$ [115-118]. According to [26], the H-bridge circuit is used to determine the polarity of the series-connected port voltage $V_s$, as shown in Figure 1.21. Therefore, the voltage relationship is $V_{out} = V_p \pm V_H$, where $V_p = V_{in}$ and $V_H = \pm V_s$. When $V_{out}$ approaches $V_{in}$, $V_H$ approaches zero, so large voltage

gain $V_p/V_H$ is still required, which is similar with Figure 1.20(b). This means, a wide voltage gain range is still inevitable due to this input-parallel-output-series PPC structure. When the absolute value of $V_H$ decreases to a threshold voltage, the H-bridge part will also work as a quadrant chopper, so FPC only needs to decrease $V_p$ to $V_s$ and then the H-bridge will further reduce $V_s$ to $V_H$. Hence, the wide voltage gain requirement for the isolated FPC in Figure 1.20(b) is alleviated to a certain extent.

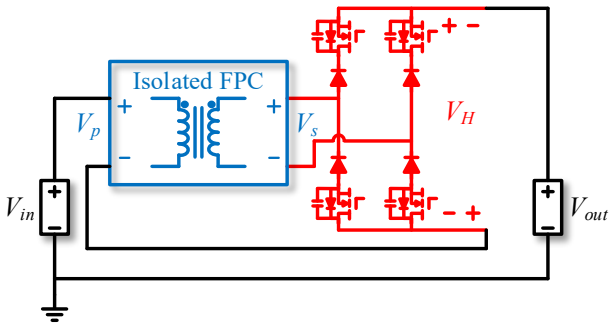



Figure 1.21 PPP buck-boost structure using a polarity reversal H-bridge circuit.

### 1.4.3.2 Two-stage schemes

To avoid a wide voltage gain range in a polarity reversal scheme, a two-stage step-up/down PPC concept is proposed in [119], as shown in Figure 1.22. This method does not involve inverting the voltage of $V_s$; rather, the input voltage $V_{in}$ is initially increased to an intermediate voltage $V_{int}$ and then decreased to $V_{out}$ with the help of two connected PPCs. The voltage relationships in two PPCs are $V_{int} = V_{in}+V_{s1}$ and $V_{out} = V_{int}-V_{s2}$, respectively. By regulating the voltage relationships of two PPCs separately, the buck-boost can be realized. However, two FPCs are used in this scheme, causing extra cost and power losses. Similarly, in [120], both PPP step-up and step-down stages are used to realize buck-boost.

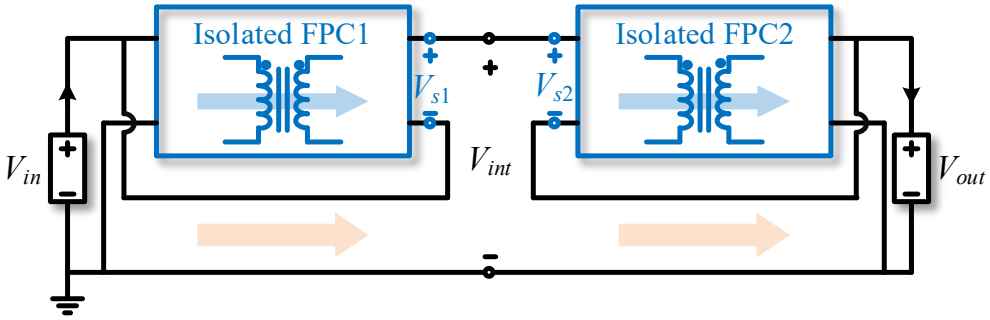



Figure 1.22 The diagram for the two-stage step-up/down PPC concept.

## 1.5 Research Hypothesis and Thesis Overview

In Section 1.4, a PPP scheme for independent dc ports reduces the voltage and current stresses on the converter, allowing for downsizing the converter and enhancing overall system efficiency. Additionally, a range of isolated dc–dc converters can be applied into the PPP two-port structures, offering flexibility for diverse industrial applications. This thesis proposes that the typical PPP two-port structures can be expanded to accommodate more complex applications by incorporating multiport and buck-boost functionalities. While some multiport PPP converters and buck-boost schemes have been explored, current three-port converters either achieve PPP between only two of the three ports or lack a versatile structure that can adapt different converters for varied applications. Moreover, existing buck-boost schemes often face challenges such as wide voltage gain ranges or unnecessary complexity.

To address these limitations, this paper presents the following three key innovations:

(1) The novel modularized derivation method of the PPP multiport dc–dc structure is proposed.

This thesis first introduces the modularization of typical PPP two-port structures. In these structures, the isolated two-port dc–dc converter is conceptualized as two coupled modules. By treating the converter as a modular system, it becomes possible to clarify how PPP reduces power transmission requirements by processing only the power difference in voltage and current due to series and/or shunt modules. By modifying the connections between modules rather than the converters themselves, the PPP structure can be expanded to support multiple ports while maintaining voltage and current reduction. Using Kirchhoff's laws, only N modules are required for an PPP N-port structure. For example, nine general PPP three-port structures can be derived by varying the connections of three modules. Then, when facing a specific application, their characteristics are compared, and the optimal one can be selected and applied.

(2) The general PPP multiport dc–dc structure with radial module connections is proposed.

Following the modularized derivation method, a PPP single-input(or output) N-output(or input) dc–dc structure, featuring radial module connections, is selected from the derived general PPP multiport structures. This radial configuration connects a single input/output, with a parallel-connected module, to N−1 outputs/inputs via series-connected modules, respectively. As a

demonstration, three active bridge modules are implemented in a PPP single-input dual-output (SIDO) dc–dc structure. Detailed characteristics and calculations are provided, and a prototype circuit is built to verify the feasibility and performance of the proposed PPP dc–dc converter, particularly in reducing both voltage and current stresses, which contributes to a high efficiency.

(3) A novel PPP buck-boost dc–dc structure is proposed.

In addition to the general PPP multiport structure, this thesis also proposes a novel PPP buck-boost structure based on the modularized derivation principle established in previous chapters. This design aims to mitigate the issue of wide voltage gain ranges in traditional PPP buck-boost converters with bipolar modules. The proposed scheme connects two series modules of opposite polarity between the positive terminals of the input and output ports, and an intermediate capacitor equipped with a parallel-connected module is placed between them. The input and output voltages are determined by the sum of the intermediate and series-module voltages, enabling voltage regulation without the need to alter module polarity. By setting the intermediate voltage to approximately half of the input or output voltage, the voltage gain of the three modules can be kept at approximately 1:1:1, thus avoiding the wide voltage gain range. Furthermore, the voltage stress on each module is reduced to about half of the input or output voltage, preserving PPP's voltage reduction feature. Additionally, the parallel-connected module processes only the current difference between the input and output, achieving current decreasing. A prototype circuit is constructed to validate the buck-boost function and the associated voltage and current decreasing.

# Chapter 2

# Principle and Topology Derivation of Generalized PPP Multiport DC–DC Structures

From the literature review in Section 1.4.2, researchers have made some attempts to develop PPP multiport dc–dc converters [94-99]. However, these studies primarily achieve the reduction of current and voltage stresses between only two of the three ports, limiting the full potential of PPP systems. Furthermore, the proposed PPP three-port topologies are restricted to a few specific configurations, lacking the flexibility of the general PPP two-port structures which allow for the integration of various converters. This limited flexibility hinders the existing designs to meet the diverse requirements encountered in real-world implementations, such as different power level regulation, bi-directional power transmission, costs, efficiency, voltage gain range, and so on.

In this chapter, I will demonstrate that it is feasible to implement PPP across all dc ports. Additionally, the aim is to develop a general structure rather than focusing on a specific converter, enabling the general PPP multiport dc–dc structures tailored to different applications. To achieve this, I first introduce the modularization of the existing typical PPP two-port structures. Building upon these PPP modules, a novel derivation method for PPP three-port dc–dc structures is presented. By configuring the modules in series or parallel with each dc port, the partial power resulting from the voltage and current differences among the three dc ports can be processed. After further eliminating the redundant modules, a PPP three-port structure is derived, requiring only three isolated modules. This approach is both straightforward and effective, yielding nine distinct PPP three-port topologies. Furthermore, a systematic methodology is provided to assist in selecting the most appropriate topology for specific three-port applications. Finally, based on the derivation principles used for the PPP three-port topologies, potential PPP four-port and five-port dc–dc structures are also outlined.

## 2.1 Modularization of the PPP Two-Port Structures

According to the literature review presented in Section 1.4.1, it was shown that there are four typical PPP two-port dc–dc structures. From Figure 2.1, the input and output ports of the isolated FPC are defined as $V_i$ and $V_o$, and the real source and load are $V_{in}$ and $V_{out}$, respectively. Unlike the traditional full power processing structures where $V_i$ and $V_o$ are both parallel connected to the $V_{in}$ and $V_{out}$, in a PPP scheme, one port of FPC, i.e., $V_i$ or $V_o$, is changed to be series connected to $V_{in}$ or $V_{out}$, and the other port remains connected in parallel. In this arrangement, the PPP two-port structures are therefore classified as IPOS step-up/down and ISOP step-up/down, as shown in Figure 2.1.

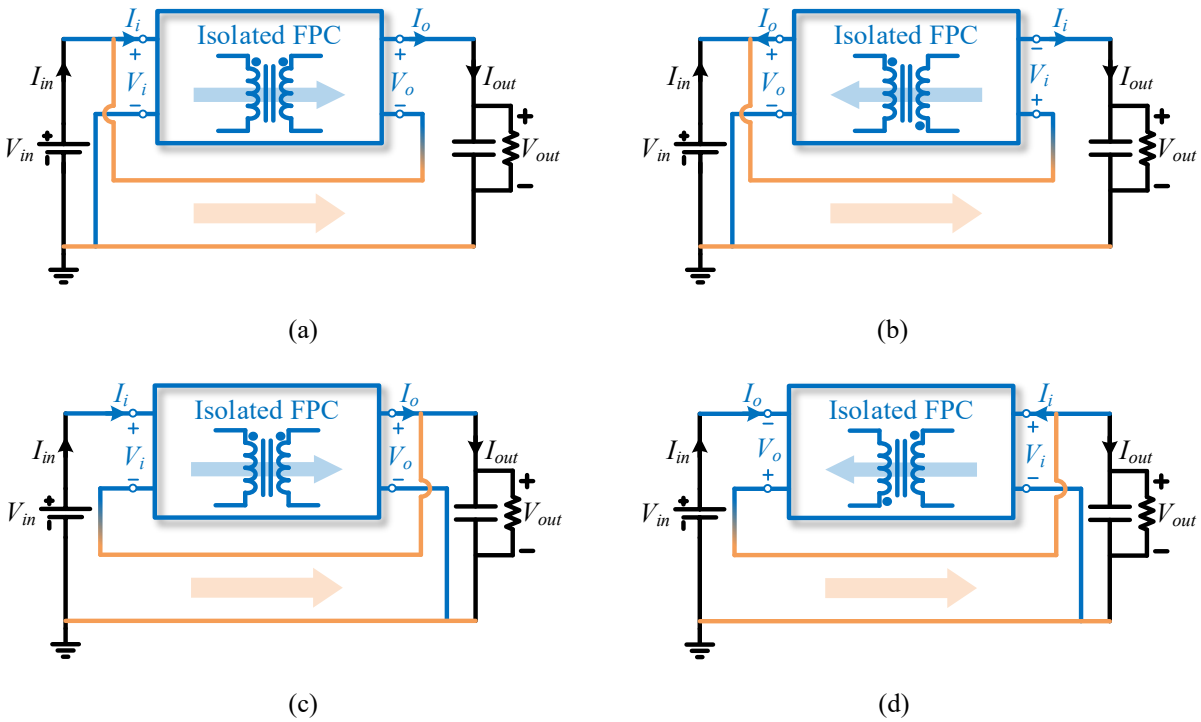



Figure 2.1 Four typical PPP two-port dc–dc structures. (a) Input-parallel output-series step-up. (b) Input-parallel output-series step-down. (c) Input-series output-parallel step-down. (d) Input-series output-parallel step-up.

Take Figure 2.1(a) as an example, the input port $V_i$ of the isolated FPC is connected to source $V_{in}$ in parallel, and $V_o$ is connected between $V_{in}$ and $V_{out}$ in series. In this connection, the input current of FPC $I_i$ is reduced to $I_{in}$–$I_{out}$, and the voltage of $V_o$ is reduced to $V_{out}$–$V_{in}$. This achieves current/voltage reduction of FPC, and FPC in this connection only processes the partial power.

However, in this configuration, the reduction of current/voltage is not obvious until conducting the calculation. Moreover, due to the nature of the connection approach, where the two ports of the converter are simply reconfigured to be in series or parallel with the source and load, it is difficult to envision how this method could be effectively extended to multiport systems. As the number of ports increases, reconfiguring the connection between a N-port converter and N dc ports to realize PPP become increasingly complex and challenging.

To give a clearer view of the PPP structure showing that the isolated FPC only needs to withstand the current/voltage differences between source and load, modularization is explored in this section. The corresponding isolated FPC is firstly modularized into two isolated parts. They are named Module *P* and Module *S*, depending on the series or parallel connection, as shown in Figure 2.2. The IPOS and ISOP step-up/down PPP two-port dc–dc structures in Figure 2.1 can be then re-constructed into modular connections, as shown in Figure 2.3.

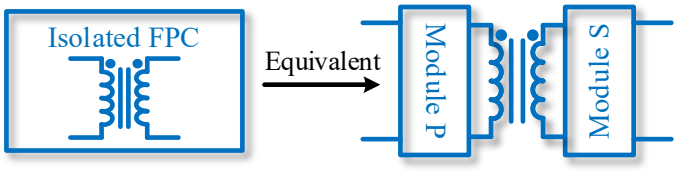



Figure 2.2 Modularization of the isolated full power converter.

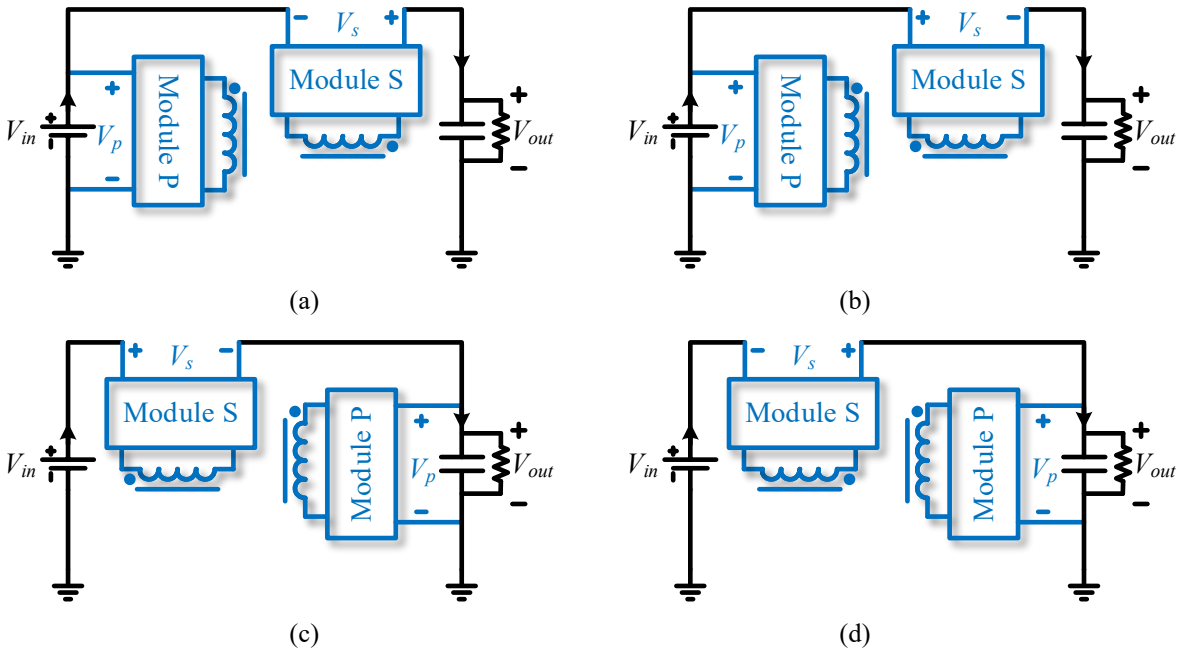



Figure 2.3 Re-constructed two-port dc–dc structures. (a) Input-parallel output-series step-up. (b) Input-parallel output-series step-down. (c) Input-series output-parallel step-down. (d) Input-series output-parallel step-up.

The PPP two-port dc–dc structures in Figure 2.3. are functionally identical to those of Figure 2.1, except that the isolated FPC processing the partial power in Figure 2.1 is re-constructed into the two isolated modules in Figure 2.3. Compared with the structures in Figure 2.1, the module based structures in Figure 2.3 give a clearer voltage and current relationship. From Figure 2.3, the series-connected Module *S* is connected between two dc ports, processing the voltage difference between $V_{in}$ and $V_{out}$. Another parallel-connected Module *P* can be either connected to the input $V_{in}$ or output $V_{out}$, so that it could supply or absorb the current difference between the source and load, processing the partial power caused by current difference.

After observing this structure from a modularization perspective, the essence of PPP can be concluded that voltage/current decreasing is achieved for Module *S*/Module *P*, thereby bringing power reduction, i.e., partial power processing. The specific example calculation was demonstrated based on Figure 1.3. By maintaining and using this essence, PPP is hoped to be expanded.

## 2.2 Modularization-Based PPP Principle and Topology Derivation of the PPP Three-Port Structures

In this section, I will give a more general perspective showing that the module connections satisfy Kirchhoff's laws, which ensures voltage/current balance between every pair of dc ports. Based on this principle of PPP implementation, the novel derivative scheme of the general PPP three-port structure is proposed.

### 2.2.1 PPP Principle

#### 2.2.1.1 Two-port

The four modularized PPP two-port dc–dc structures in Figure 2.3 are further refined and summarized in Figure 2.4 which shows that the left and right dc ports can be either source or load, so the ports are named $V_l$ and $V_r$ rather than $V_{in}$ and $V_{out}$. Looking at these structures from the perspective of Kirchhoff's laws, it's clear that whether in a $V_l$-parallel-$V_r$-series connection or

in a $V_l$-series-$V_r$-parallel connection, there is always an isolated module series connected between ports $V_l$ and $V_r$, which is named Module $S$. Module $S$ is used to balance the voltage difference caused partial power, which equals to $|V_l-V_r|\times I_r$ and $|V_l-V_r|\times I_l$ in Figure 2.4(a) and Figure 2.4(b), respectively. In addition, Module $P$ is in parallel connection with $V_l$ or $V_r$ and processes the partial power caused by current difference, which equals to $|I_l-I_r|\times V_l$ and $|I_l-I_r|\times V_r$, respectively. The setting of the dc ports $V_l$ and $V_r$ to be input or output will only influence the direction of the power flow in the circuit. For example, when $V_l$ is input, $V_r$ is output, the power to be directly delivered flows from $V_l$ to $V_r$, and the partial power through modules flows from Module $P$ to Module $S$. The situation reverses when $V_l$ is output and $V_r$ is input. The direction of power flow in Figure 2.4 is consistent with that shown in Figure 2.1.

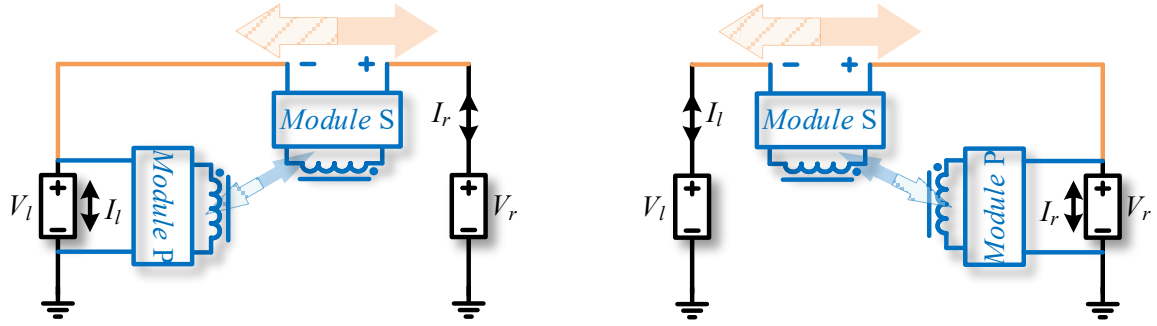



Figure 2.4 More generalized PPP two-port dc–dc structures. (a) $V_l$-parallel-$V_r$-series. (b) $V_l$-series-$V_r$-parallel.

Comparing the two structures in Figure 2.4, the partial power ratio will be one of the main indicators of selecting the configuration. The partial power ratio here is defined as the partial power processed by modules divided by the total power which is the sum of both input and output power, as shown in (2.1). Due to the polarity of series-connected Module $S$, the voltage and current relationships are $V_l<V_r$ and $I_l>I_r$, respectively. Then, the partial power ratio of two structures is calculated in (2.1). From (2.1), the ratio of the partial power $P_{p(a)}$ to the total power $P_t$ in Figure 2.4(a) is always smaller than one, which means the power processed by the isolated module is always lower than the equivalent full power converter. However, in Figure 2.4(b), the power ratio $P_{p(b)}/P_t$ may be larger than 1 when $V_rI_l$ is far larger than $V_lI_l$, losing PPP. Therefore, when facing various applications, the structure in Figure 2.4(a) is optimal when only considering the partial power ratio.

$$\begin{cases} \dfrac{P_{p(a)}}{P_t} = \dfrac{|V_l - V_r| I_r + V_l |I_l - I_r|}{|V_l I_l| + |V_r I_r|} = \dfrac{P_t - 2V_l I_r}{P_t} < 1 \\ \dfrac{P_{p(b)}}{P_t} = \dfrac{|V_l - V_r| I_l + V_r |I_l - I_r|}{|V_l I_l| + |V_r I_r|} = \dfrac{2V_r I_l - P_t}{P_t} \end{cases} \tag{2.1}$$

### 2.2.1.2 Three-port

The principle of PPP two-port dc–dc structure is that PPP between two dc ports can be achieved by two isolated modules, where Module *S* and Module *P* are applied to process the partial power caused by voltage and current difference, respectively. This can be extended to three ports as shown in Figure 2.5. From Figure 2.5, every dc port is equipped with a parallel connected Module *P* and a Module *S* in series connection with another dc port. The voltage relationship among three dc ports varies when the polarities of Module *S* are changed. In this connection, the isolated modules only process the partial power caused by voltage or current difference, which successfully keeps the function of PPP. However, some of the modules are redundant, causing high costs and large power loss, which undermines the advantage of PPP. To optimize the topology, further simplification is required. The following derivation will be demonstrated based on the voltages $V_l$, $V_m$ and $V_r$, where the polarities of the series connected modules are fixed as shown in Figure 2.5. It should be noted that Figure 2.5 can represent all the preliminarily three-port structures, because this triangular connection structure is symmetrical such that the topologies are equivalent even if the polarities of Module *S* are changed.

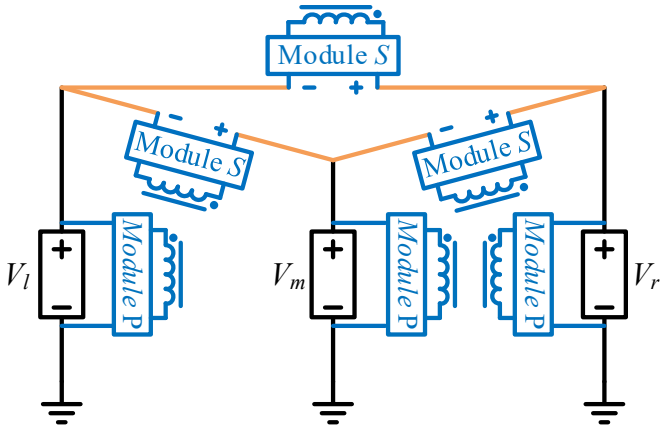
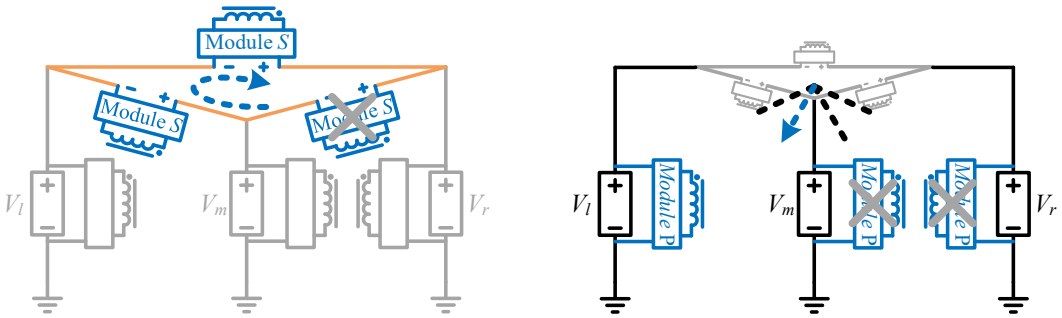



Figure 2.5 The preliminary extension of the PPP structure to three ports.

### 2.2.2 Derivation of the PPP Three-Port DC–DC Topologies

To reduce the number of the isolated modules in Figure 2.5, Module *S* and Module *P* are now considered separately due to their different functions. Based on Figure 2.5, the partial power caused by voltage difference among $V_l$, $V_m$ and $V_r$ is processed by three series connected modules (Module *S*). When one of the three modules is removed as shown in Figure 2.6(a), there is still at least one or two Module *S* being series connected between any two dc ports and the voltage balance is still retained. Therefore, the number of the series connected modules can be reduced to two. Similarly, because all the positive terminals of the three dc ports are connected together via Module *S* as shown in Figure 2.6(b), the partial power caused by current differences among the three dc ports can be processed by only one parallel connected module (Module *P*). Accordingly, the three Module *P* can be reduced to one.




(a) (b)

Figure 2.6 Further simplifications of isolated modules used for voltage and current balance. (a) Voltage balance. (b) Current balance.

Based on the preliminary structure in Figure 2.5 and the aforementioned derivation, nine feasible PPP three-port dc–dc topologies can be derived after removing the redundant series and parallel connected modules, as shown in Figure 2.7. Because the polarities of Module *S* are fixed in Figure 2.7, when different Module *S* are removed, the corresponding nine topologies are unique. The topologies in (a)~(c), (d)~(f) and (g)~(i) of Figure 2.7 are classified as *A*, *B* and *C*, respectively. In type *A*, *B* and *C*, the voltage relationships are $V_l<V_m<V_r$, $V_m>V_l\&V_r>V_l$, and $V_l<V_r\&V_m<V_r$, respectively. In addition, depending on the voltage of the dc port $V_l$, $V_m$, and $V_r$ where Module *P* is in parallel, the second given labels of the corresponding topologies are *l*, *m* and *r*. According to the classification, as an example, the topology of Figure 2.7(a) is named as

*Al* because the Module *S* between $V_l$ and $V_r$ is removed, and the Module *P* is in parallel connection with $V_l$.

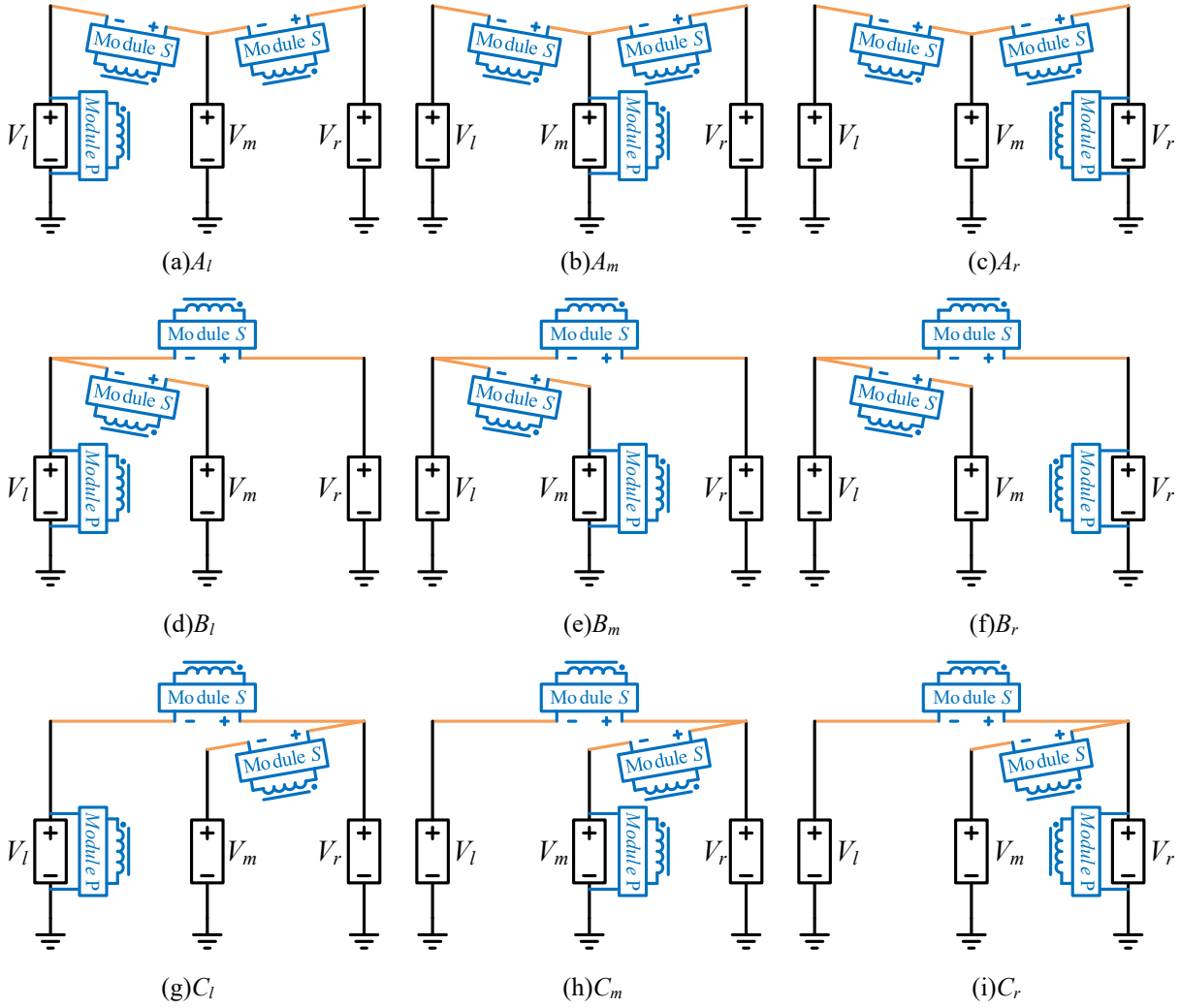



Figure 2.7 The derived nine PPP three-port dc–dc topologies.

## 2.3 Analysis and Comparison of the Nine PPP Three-Port DC–DC Topology

Although all the derived nine three-port dc–dc topologies can realize PPP with the smallest number of the isolated modules, their characteristics differ under various operating conditions. In this section, an analysis and comparison will be conducted in detail to help engineers pick out the best topology for a specific application.

### 2.3.1 Partial Power Calculation and Comparison

From the partial power point of view, if the efficiency of the power conversion of each isolated module is fixed, the smaller the partial power processed by the modules, the higher the global efficiency. Hence, the partial power needs to be compared to providing a basis for selection.

The positive directions and simplified names of the currents and voltages are firstly specified in Figure 2.8 to calculate the sum of the partial power processed by the isolated modules. From Figure 2.8, the currents/voltages of the series connected modules $M_{ml}$, $M_{rl}$, and $M_{rm}$ are named as $I_{ml}/V_{ml}$, $I_{rl}/V_{rl}$ and $I_{rm}/V_{rm}$, respectively. In addition, the currents/voltages of the parallel connected modules $M_{pl}$, $M_{pm}$, and $M_{pr}$ are named as $I_{pl}/V_l$, $I_{pm}/V_m$ and $I_{pr}/V_r$, respectively. According to Section 2.2.2, the redundant isolated modules will be removed. Considering the differences in how isolated modules are removed in nine topologies, $k_{xx}$ is used to demonstrate whether the isolated module $M_{xx}$ is removed or retained, where $xx$ represents $ml$, $rl$, $rm$, $pl$, $pm$, or $pr$. When $k_{xx} = 1$, the corresponding module is retained, and it is converse when $k_{xx} = 0$. The values of $k_{xx}$ corresponding to the topologies in Figure 2.7 are shown in Table 2.1.

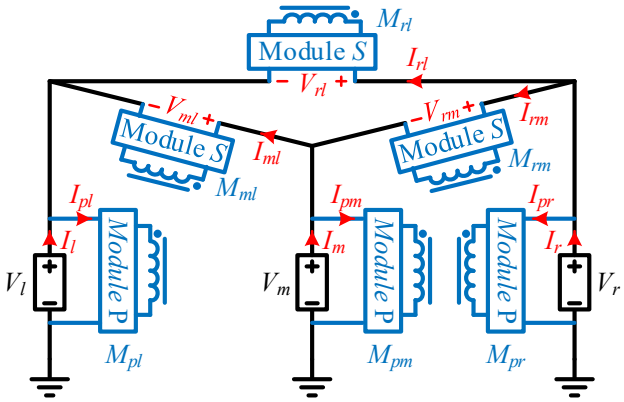



Figure 2.8 Specified positive directions of currents and voltages in the PPP three-port dc–dc topology.

Table 2.1

VALUE OF $K_{XX}$ CORRESPONDING TO TOPOLOGIES (A)~(I) IN FIGURE 2.7

| | *Al* | *Am* | *Ar* | *Bl* | *Bm* | *Br* | *Cl* | *Cm* | *Cr* |
|---|---|---|---|---|---|---|---|---|---|
| $k_{ml}$ | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| $k_{rm}$ | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| $k_{rl}$ | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| $k_{pl}$ | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| $k_{pm}$ | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| $k_{pr}$ | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |

Subsequently, the general expressions of the parallel and series connected module currents can be obtained in (2.2) and (2.3), respectively. In addition, the general expression of the partial power $P_p$ is shown in (2.4), which is the sum of the power processed by three modules.

$$k_{pl}I_{pl}+k_{pm}I_{pm}+k_{pr}I_{pr}=I_l+I_m+I_r=I_{sum} \tag{2.2}$$

$$\begin{cases} I_{ml}=\left[k_{rm}\left(I_m-k_{pm}I_{pm}+I_r-k_{pr}I_{pr}\right)+k_{rl}\left(I_m-k_{pm}I_{pm}\right)\right]k_{ml} \\ I_{rm}=\left[k_{rl}\left(I_l-k_{pl}I_{pl}+I_r-k_{pr}I_{pr}\right)+k_{ml}\left(I_r-k_{pr}I_{pr}\right)\right]k_{rm} \\ I_{rl}=\left[k_{rm}\left(I_m-k_{pm}I_{pm}+I_r-k_{pr}I_{pr}\right)+k_{ml}\left(I_r-k_{pr}I_{pr}\right)\right]k_{rl} \end{cases} \tag{2.3}$$

$$P_p=\left|V_m-V_l\right|\times\left|I_{ml}\right|+\left|V_r-V_m\right|\times\left|I_{rm}\right|+\left|V_r-V_l\right|\times\left|I_{rl}\right|+\left(k_{pl}V_l+k_{pm}V_m+k_{pr}V_r\right)\times\left|I_{sum}\right| \tag{2.4}$$

Substituting the values in Table 2.1 into (2.2), (2.3) and (2.4), the specific expressions for the nine topologies can be obtained. Based on Table 2.1 and (2.2), the currents of parallel connected modules $I_{pl}$, $I_{pm}$ or $I_{pr}$ are always equal to the sum of the port currents in any of the nine topologies, which is $I_{sum}$, because only one parallel module needs to be retained in one topology. In addition, the currents of the series connected modules corresponding to nine topologies are shown in Table 2.2. According to Table 2.1, Table 2.2 and (2.4), the sum of the partial power $P_{ij}$($i$=*A*, *B or* C, $j$=*l, m or r*) of the nine topologies can be easily obtained.

Table 2.2

CURRENT VALUES OF SERIES CONNECTED MODULES CORRESPONDING TO TOPOLOGIES (A)~(I) IN FIGURE 2.7

| (a)~(c) | $I_{ml}$ | $I_{rm}$ | (d)~(f) | $I_{ml}$ | $I_{rl}$ | (g)~(i) | $I_{rm}$ | $I_{rl}$ |
|---|---|---|---|---|---|---|---|---|
| *Al* | $I_m$+$I_r$ | $I_r$ | *Bl* | $I_m$ | $I_r$ | *Cl* | $-I_m$ | $I_m$+$I_r$ |
| *Am* | $-I_l$ | $I_r$ | *Bm* | $-I_l$–$I_r$ | $I_r$ | *Cm* | $I_l$+$I_r$ | $-I_l$ |
| *Ar* | $-I_l$ | $-I_l$–$I_m$ | *Br* | $I_m$ | $-I_l$–$I_m$ | *Cr* | $-I_m$ | $-I_l$ |

The partial power comparisons will be conducted when the connections of Module *S* and Module *P* are fixed, respectively. When the position of Module *P* is fixed, the partial power under different connections of Module *S* is compared in (2.5) and (2.6). Because the sum of the absolute values of any two real numbers is greater than or equal to the absolute value of their sum, and the difference between the absolute values of any two numbers is less than or equal to the absolute value of their sum, the differences in (2.5) and (2.6) are always larger than zero. This indicates that topology *Aj*($j$=*l, m or r*) always processes a smaller partial power than topologies *Bj* and *Cj*.

$$\begin{cases} P_{Bl}-P_{Al}=(V_m-V_l)\left(|I_m|+|I_r|-|I_m+I_r|\right)\geq 0 \\ P_{Bm}-P_{Am}=(V_m-V_l)\left(|I_r+I_l|+|I_r|-|I_l|\right)\geq 0 \\ P_{Br}-P_{Ar}=(V_m-V_l)\left(|I_m+I_l|+|I_m|-|I_l|\right)\geq 0 \end{cases} \tag{2.5}$$

$$\begin{cases} P_{Cl}-P_{Al}=(V_r-V_m)\left(|I_m+I_r|+|I_m|-|I_r|\right)\geq 0 \\ P_{Cm}-P_{Am}=(V_r-V_m)\left(|I_l+I_r|+|I_l|-|I_r|\right)\geq 0 \\ P_{Cr}-P_{Ar}=(V_r-V_m)\left(|I_l|+|I_m|-|I_l+I_m|\right)\geq 0 \end{cases} \tag{2.6}$$

When the connections of Module *S* are fixed, the partial power differences between various positions of Module *P* are shown in (2.7), (2.8), and (2.9). They are always larger than zero because the relationships $(a+b+c)^2\geq(|a+b|-|c|)^2$ or $(a+b+c)^2\geq(|a|-|b+c|)^2$ are always satisfied for any three real numbers *a*, *b* and *c*. Therefore, the value of the partial power tends to be smaller if module *P* is in parallel connection with the dc port with smaller voltage.

$$\begin{cases} P_{Am}-P_{Al}=(V_m-V_l)\left(|I_{sum}|+|I_l|-|I_m+I_r|\right)\geq 0 \\ P_{Ar}-P_{Am}=(V_r-V_m)\left(|I_{sum}|+|I_l+I_m|-|I_r|\right)\geq 0 \end{cases} \tag{2.7}$$

$$\begin{cases} P_{Bm}-P_{Bl}=(V_m-V_l)\left(|I_{sum}|+|I_l+I_r|-|I_m|\right)\geq 0 \\ P_{Br}-P_{Bl}=(V_r-V_l)\left(|I_{sum}|+|I_l+I_m|-|I_r|\right)\geq 0 \end{cases} \tag{2.8}$$

$$\begin{cases} P_{Cr}-P_{Cl}=(V_r-V_l)\left(|I_{sum}|+|I_l|-|I_m+I_r|\right)\geq 0 \\ P_{Cr}-P_{Cm}=(V_r-V_m)\left(|I_{sum}|+|I_m|-|I_l+I_r|\right)\geq 0 \end{cases} \tag{2.9}$$

To better understand the partial power relationships of the nine topologies, a matrix diagram with the arrows is illustrated in Figure 2.9. The direction of the arrow represents the partial power relationship between two topologies, and the type of the arrow indicates different comparisons when the connection of Module *S* and Module *P* are respectively fixed. More specifically, the partial power corresponding to the starting point of the arrow is less than that of the ending point. According to Figure 2.9, no matter how large the port voltages or currents are, and no matter what the port type is, the partial power processed in topology *Al*, which is $P_{Al}$, is always the smallest. Therefore, from the partial power point of view, topology *Al* is preferred.

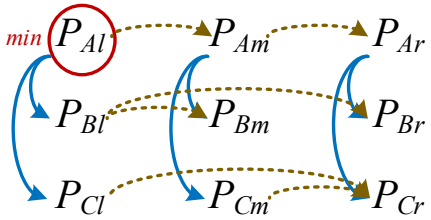



Figure 2.9 Summarization of the partial power relationships among the nine topologies.

In addition, the relationships of the ranges in the partial power ratios are consistent with Figure 2.9. Again, the partial power ratio is defined as the sum of the partial power processed by three modules divided by the total power which is the sum of the power flowing through three dc ports. To simply verify this, a system parameter $V_l$ = 200 V, $V_m$ = 240 V, and $V_r$ = 300 V is taken as an example. According to (2.4) and the expression in (2.10), the ratios of the partial power to the total power changing with the port currents $I_l$ and $I_r$ can be obtained in Figure 2.10. From Figure 2.10, $I_l$ varies from −2.5 A to 2.5 A to simulate both source and load conditions, while $I_r$ ranges from −6 A to 6 A, allowing for the observation of the partial power ratio region within the example $I_l$ range. The partial power ratio of topology *Al*, which is named $R_{Al}$, is drawn in Figure 2.10(a). From Figure 2.10(a), when $I_l$ and $I_r$ are positive or negative at the same time, the corresponding partial power ratio is smaller. Moreover, although the ratio $R_{Al}$ changes with the port currents $I_l$ and $I_r$, it is fixed to a range. The limitation of the partial power ratio is determined by the topology itself. Under identical system parameters, the characteristics of different topologies dictate their respective power ratio ranges, as shown in Figure 2.10(b). The ranges of partial power ratio $R_{ij}$($i$=*A*, *B or* C, $j$=*l, m or r*) of the nine topologies are summarized in Figure 2.10(b). From Figure 2.10(b), the boundary lines of the partial power ratio ranges corresponding to the nine topologies overlap. Therefore, bidirectional arrows are used to distinguish the specific ranges. The range of $R_{Al}$ corresponding to topology *Al* is the smallest among that of the nine topologies. This result is the same as that of the comparisons among the partial power $P_{ij}$.

$$R_{ij} = \frac{P_{ij}}{|V_l I_l| + |V_r I_r| + |-V_l I_l - V_r I_r|}, (i = A, B, C; j = l, m, r) \tag{2.10}$$

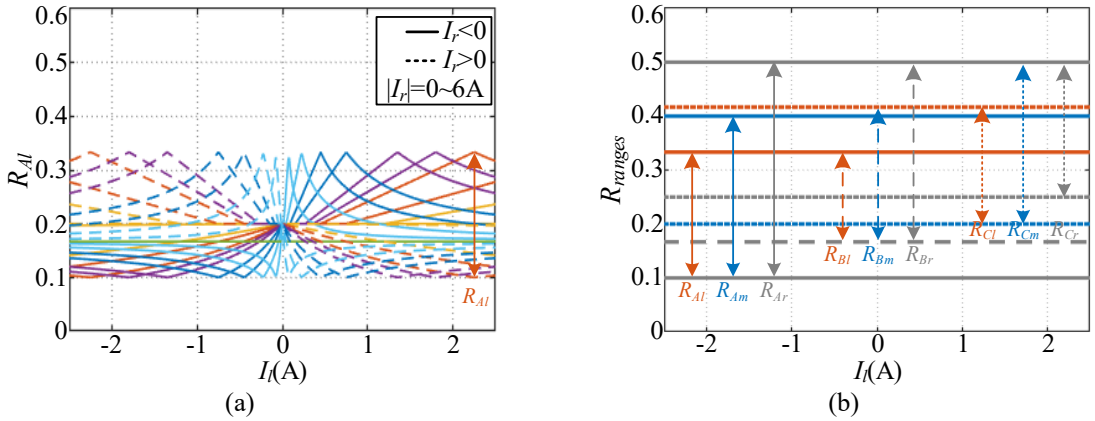



Figure 2.10 The ratio of the partial power to the total power with the example parameters. (a) Ratio of topology *Al*. (b) Ratio ranges of the nine topologies.

### 2.3.2 Voltage Gains of the Three Isolated Modules

In addition to considering the ratio of the partial power to the total power, the voltage gain of the three isolated modules is another important parameter for selection. As the three isolated modules are coupled using a three-winding transformer, the voltage ratio of the isolated modules determines the turns ratio or vice versa. Assuming that the voltage gains are proportional to the turns ratio, if the voltage ratio is far from 1:1, then a large number of coil turns is required, resulting in large size, reduced power density, and higher leakage inductance.

To provide a reference for selection, the voltage gains of topologies *Al*, *Bl* and *Cl* based on the example parameters $V_m$ = 240 V, $V_l$ = 0~240 V, $V_r$ = 240~480 V are shown in Figure 2.11. Because Module *P* is in parallel connection with $V_l$ in topologies *Al*, *Bl* and *Cl*, the voltage gains can be expressed by $V_l/V_{ml}$, $V_l/V_{rm}$, and $V_l/V_{rl}$ according to Figure 2.8. When $V_r$ is fixed to 300V, $V_l/V_{ml}$ and $V_l/V_{rl}$ changing with $V_l$ can be obtained in the left of Figure 2.11. Similarly, when $V_l$ is fixed to 200 V, $V_l/V_{rm}$ and $V_l/V_{rl}$ changing with $V_r$ are drawn in the right of Figure 2.11. Moreover, the trends of the voltage gains in the other six topologies are similar with Figure 2.11 because they only change the position of the parallel connected Module *P*.

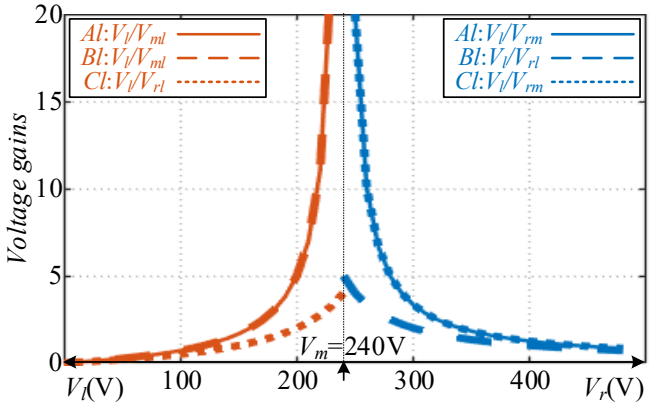



Figure 2.11 Voltage gains comparisons among topologies *Al*, *Bl*, and *Cl*: $V_l/V_{ml}$ and $V_l/V_{rl}$ changing with $V_l$ when $V_r$ = 300 V, and $V_l/V_{rm}$ and $V_l/V_{rl}$ changing with $V_r$ when $V_l$ = 200 V.

To reduce the size of the transformer, it is better if the voltage gains are small. From Figure 2.11, when the values of $V_l$ and $V_r$ are close to $V_m$, the voltage gains in topology *Al* can easily exceed 10, which is unfavorable. On the contrary, the voltage gain can be successfully suppressed under 5 in topology *Bl* and *Cl* even if $V_r$ and $V_l$ are close to $V_m$, respectively. The situations are

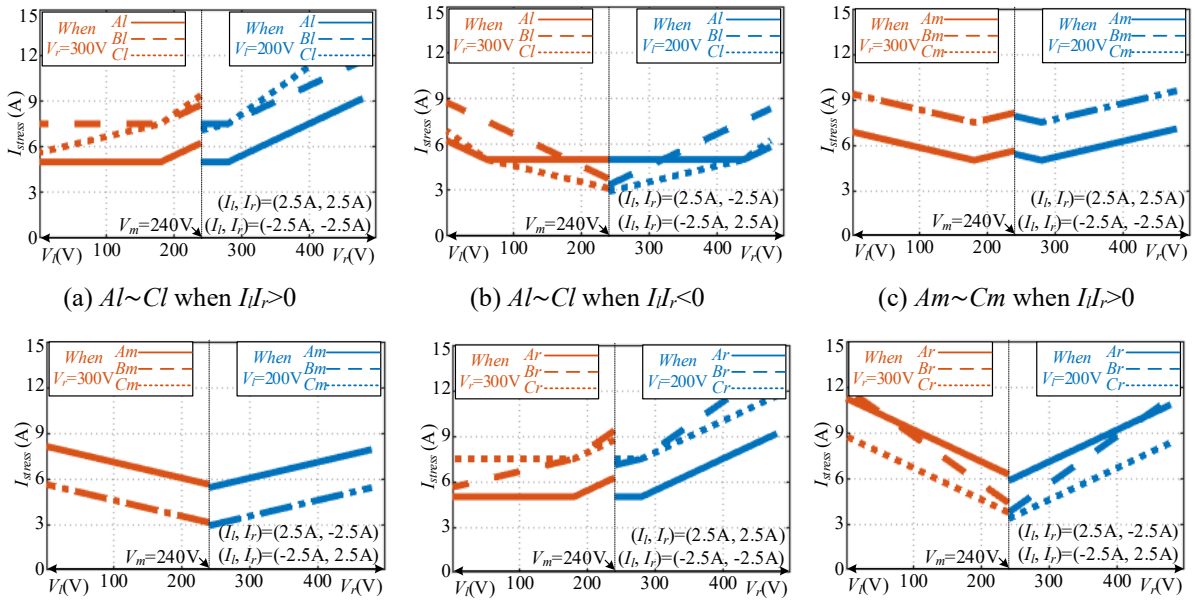
similar in topologies *Bm*, *Br*, *Cm* and *Cr*. Therefore, from the voltage gain point of view, topologies *Bj* and *Cj* (*j=l, m or r*) are preferred when $V_l$ and $V_r$ are close to $V_m$.

### 2.3.3 Current Stresses

The conduction losses in power conversion are predominantly governed by the root mean square (RMS) value of the current flowing through the three isolated modules. Since a specific converter (full bridge, DAB and so on) has not been designated for the modules, the average current for each module is defined as the current stress for the purposes of this section. The subsequent discussion will illustrate how the chosen topology affects these current stresses. Based on (2.2), (2.3) and Table 2.1, the sum of the module current stresses are calculated in (2.11), which is $I_{stress}$.

$$I_{stress} = I_{ml} + I_{rm} + I_{rl} + I_{sum} \tag{2.11}$$

Similarly, using the system parameter $V_m$ = 240 V, $V_l$ = 0~240 V, $V_r$ = 240~480 V, $|I_l|$ = 2.5 A and $|I_r|$ = 2.5 A as an example, the current stress $I_{stress}$ as a function of the port voltages is shown in Figure 2.12. When $V_r$ and $V_l$ are fixed at 300 V and 200 V, respectively, the influence of $V_l$ and $V_r$ on $I_{stress}$ is shown on the same axis. Figure 2.12(a) compares the current stress $I_{stress}$




(a) *Al*~*Cl* when $I_lI_r$>0 (b) *Al*~*Cl* when $I_lI_r$<0 (c) *Am*~*Cm* when $I_lI_r$>0

(d) *Am*~*Cm* when $I_lI_r$<0 (e) *Ar*~*Cr* when $I_lI_r$>0 (f) *Ar*~*Cr* when $I_lI_r$<0

Figure 2.12 Current stress $I_{stress}$ changing with $V_l$ when $V_r$ = 300 V and $I_{stress}$ changing with $V_r$ when $V_l$ = 200 V in different topologies.

across topologies *Al* to *Cl* when $I_l$ shares the same sign as $I_r$. In contrast, Figure 2.12(b) presents a comparison of current stresses for the same topologies when $I_l$ and $I_r$ exhibit opposite signs. In addition, similar comparisons are conducted in Figure 2.12(c)~Figure 2.12(f), which correspond to the different topologies *Am*~*Cm* and *Ar*~*Cr*.

From Figure 2.12(a), Figure 2.12(c) and Figure 2.12(e), although $I_{stress}$ fluctuates with the changing of $V_l$ or $V_r$, when $I_l$ has the same sign as $I_r$, the current stresses in topology *Aj* (*j=l, m or r*) are always smaller than that in *Bj* and *Cj*. However, when $I_l$ and $I_r$ have different signs, $I_{stress}$ in topology *Cj* is the smallest according to Figure 2.12(b), Figure 2.12(d) and Figure 2.12(f). As a result, from the efficiency of the partial power conversion point of view, topology *Aj* is preferred when $I_lI_r>0$, while topology *Cj* is better when $I_lI_r<0$.

### 2.3.4 Fault Tolerance Consideration

Fault Tolerance refers to the ability of a system to continue operating properly in the event of a failure or fault in one or more of its components. In applications such as renewable energy, electric vehicles, and industrial automation, multiport dc–dc converters play a critical role. Given their importance, fault tolerance is essential to ensure uninterrupted operation, minimize downtime, and reduce maintenance costs. This capability allows the system to maintain functionality and reliability even when components fail, thereby enhancing overall performance and safety.

Given the modularized design of PPP three-port dc–dc topologies, the discussion on fault tolerance in this section focuses specifically on the interactions and impacts between modules, rather than on detailed circuits or individual components. Furthermore, prior to determining the specific circuit configuration, the modules are assumed to operate independently, meaning that the failure of one module does not affect the operation of the others.

Taking the single-input dual-output application as an example, the topology *Al* can be categorized into three distinct structures, as illustrated in Figure 2.13. These structures are differentiated by the arrangement of the single input, which is positioned as $V_l$, $V_m$, and $V_r$, respectively. In the configuration shown in Figure 2.13(a), when Module $S_1$ fails, despite the operational status of Module $S_2$ and Module *P*, the input power from $V_l$ cannot be transferred to

either $V_m$ or $V_r$ due to the failure of Module $S_1$. As for the configuration in Figure 2.13(b), while the input power of $V_m$ can be transferred through Module $S_2$ to $V_r$, the failure of Module $S_1$ affects $V_l$, which in turn impacts Module $P$. Consequently, the current balance between $V_m$ and $V_r$ cannot be maintained. Furthermore, the failure of Module $P$ disrupts all current balances, thereby affecting all dc ports. The remaining scenarios can be analyzed in a similar manner.

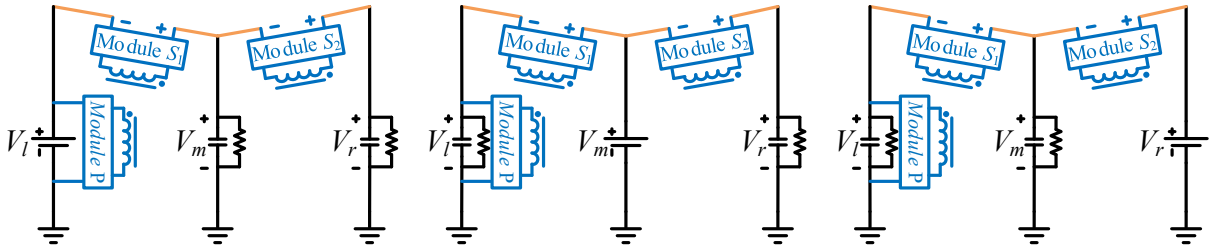



Figure 2.13 The derived PPP three-port dc – dc structures with single input and dual outputs for topology *Al*.

Table 2.3

THE DC PORTS IMPACTED BY THE FAILURE OF DIFFERENT MODULES

| **Failure Module** | **Figure 2.13(a)** | **Figure 2.13(b)** | **Figure 2.13(c)** |
|---|---|---|---|
| **Module $S_1$** | $V_m$ and $V_r$ | $V_l$ and $V_r$ | $V_l$ and $V_m$ |
| **Module $S_2$** | $V_r$ | $V_r$ | $V_l$ and $V_m$ |
| **Module *P*** | *All* | *All* | *All* |

## 2.3.5 Summary

For a specific application, the selection of the optimal PPP three-port topology can be based on the partial power ratio, the voltage gain and current stress. According to the analysis and the comparisons above, the selection preference of the nine derived topologies for different situations is summarized in Table 2.4, where *i=A*, *B*, *or* C, *j=l*, *m*, *or r*.

Table 2.4

SUMMARY OF THE PREFERRED SELECTIONS OF THE NINE DERIVED PPP THREE-PORT TOPOLOGIES CONSIDERING PARTIAL POWER, VOLTAGE GAIN AND CURRENT STRESS

| **Factors** | *Partial power* | *Voltage gain* | | *Current stress* | |
|---|---|---|---|---|---|
| **Conditions** | All | $V_l$ close to $V_m$ | $V_r$ close to $V_m$ | $I_lI_r$>0 | $I_lI_r$<0 |
| **Preferred** | *Aj* > *Bj*&*Cj*<br>*il* > *im*&*ir* | *Cj* | *Bj* | *Aj* | *Cj* |

From Table 2.4, topologies *Aj*(*j*=*l*, *m*, *or r*) and *il* (*i*=*A*, *B*, or *C*) are preferred when considering the partial power ratio. In addition, topologies *Cj* and *Bj* are better when $V_l$ and $V_r$ are close to $V_m$, respectively, when the factor of the voltage gain matters. Moreover, topologies *Aj* and *Cj* are advantageous to retain a relatively small current stress under conditions of $I_lI_r>0$ and $I_lI_r<0$, respectively. In practical applications, these factors need to be comprehensively considered, and the final selection will be made according to the trade-off among them. In the following section, the example specific application will be taken, according to which the most suitable topology will be selected. In addition, the PPP three-port dc–dc converter will be designed, and the experiment will be conducted to verify the feasibility and rationality of the proposed topology.

## 2.4 Selection Considerations

To illustrate how to select a preferred topology, let us consider an application such as a three-port dc microgrid. The corresponding system parameters are shown in Table 2.5.

Table 2.5
SYSTEM PARAMETERS

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| DC bus $V_{i1}$ | 400V | Switching period $T_s$ | 10μs |
| DC load 1 $V_{o1}$ | 320V | Output current $I_{o1}$ | 2.5A |
| DC load 2 $V_{o2}$ | 480V | Output current $I_{o2}$ | 2.5A |

According to the system parameters in Table 2.5, the nine PPP three-port topologies are compared considering the power ratio range, voltage gain, current stress, and fault tolerance capability, as shown in Table 2.6. A lower partial power ratio is advantageous as it contributes to reducing the size of the power converter and its power losses. We also expect a voltage gain approaching 1:1:1 to limit the turns of the transformer windings within a reasonable range. Furthermore, minimizing current stress, which is the sum of average currents for three modules, is essential for decreasing conduction losses. Fault tolerance is also a critical consideration in single-input dual-output applications.

To better compare the partial power ratios, the topologies *Al*~*Cl* and *Al*~*Ar*, as their ratios vary with output currents $I_{o1}$ and $I_{o2}$, are compared in Figure 2.14. From Figure 2.14(a), it is evident that the partial power ratio for *Al* consistently remains lower than that of topologies *Bl*

Table 2.6
COMPARISONS AMONG THE NINE TOPOLOGIES

| Topology | Power Ratio Range | Voltage Gain | Current Stress | Fault Tolerance |
|---|---|---|---|---|
| *Al* | 0.1~0.2 | 1:1:4 | 5 | weak |
| *Am* | 0.1~0.25 | 1:1:5 | 5 | strong |
| *Ar* | 0.1~0.3 | 1:1:6 | 5 | weak |
| *Bl* | 0.2~0.33 | 1:2:4 | 7.5 | weak |
| *Bm* | 0.2~0.33 | 1:2:5 | 7.5 | strong |
| *Br* | 0.2~0.4 | 1:2:6 | 7.5 | weak |
| *Cl* | 0.2~0.4 | 1:2:4 | 7.5 | weak |
| *Cm* | 0.17~0.5 | 1:2:5 | 7.5 | strong |
| *Cr* | 0.2~0.5 | 1:2:6 | 7.5 | weak |

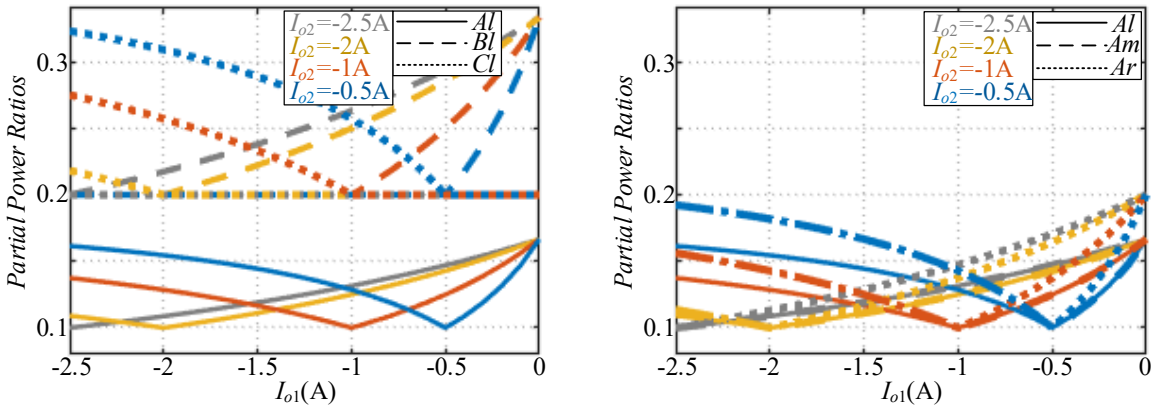



Figure 2.14 Partial power ratio comparisons based on the example parameters. (a) Comparisons among topologies *Al*, *Bl*, and *Cl*. (b) Comparisons among topologies *Al*, *Am*, and *Ar*.

and *Cl*. Figure 2.14 (b) indicates that the partial power ratio for *Ar* is the highest, whereas the ratio for *Al* is either smaller than or equal to that of topology *Am*. Consequently, when considering the range of partial power ratios, topology *Al* emerges as the most applicable choice, followed by topology *Am*. On the other hand, as presented in Table 2.6, topology *Al* is the optimal from the perspective of voltage gain. The current stress associated with topologies *Al*, *Bl* and *Cl* are the lowest when compared to the rest of the topologies. Furthermore, given the single-input dual-output application where the input port is positioned at $V_m$, the topology exhibits stronger fault-tolerant capabilities if Module *P* is connected to $V_m$. This configuration ensures that even if one Module *S* fails, the output port connected to the other Module *S* remains operational, thereby maintaining system functionality. For instance, in a system implementing topology *Al*, as illustrated in Table 2.5, $V_l$ and $V_r$ serve as the outputs while $V_m$ is the input. If the series-connected

module associated with $V_l$ fails, it directly impacts the output $V_l$. Worse more, since Module *P* is connected to $V_l$, this current difference processing module will also be affected, subsequently influencing the other output. In contrast, in topology *Am*, where Module *P* is connected to $V_m$, the failure of one output due to the failure of the corresponding series-connected module does not necessarily compromise the functionality of the other output port. Consequently, topologies *Am*, *Bm* and *Cm* exhibit strong fault tolerance in this application. After comprehensively evaluation of the advantages and disadvantages outlined in Table 2.6, topology *Am* in Figure 2.7(b) is ultimately selected for the example application.

If the active bridge module is chosen as the specific circuit to substitute the isolated module, the TAB-based PPP three-port dc–dc converter can be derived from the selected dc–dc topology, i.e., *Am* in Figure 2.7(b), as shown in Figure 2.15.

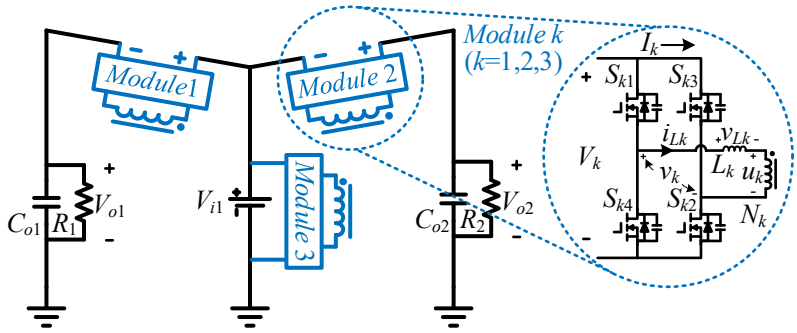


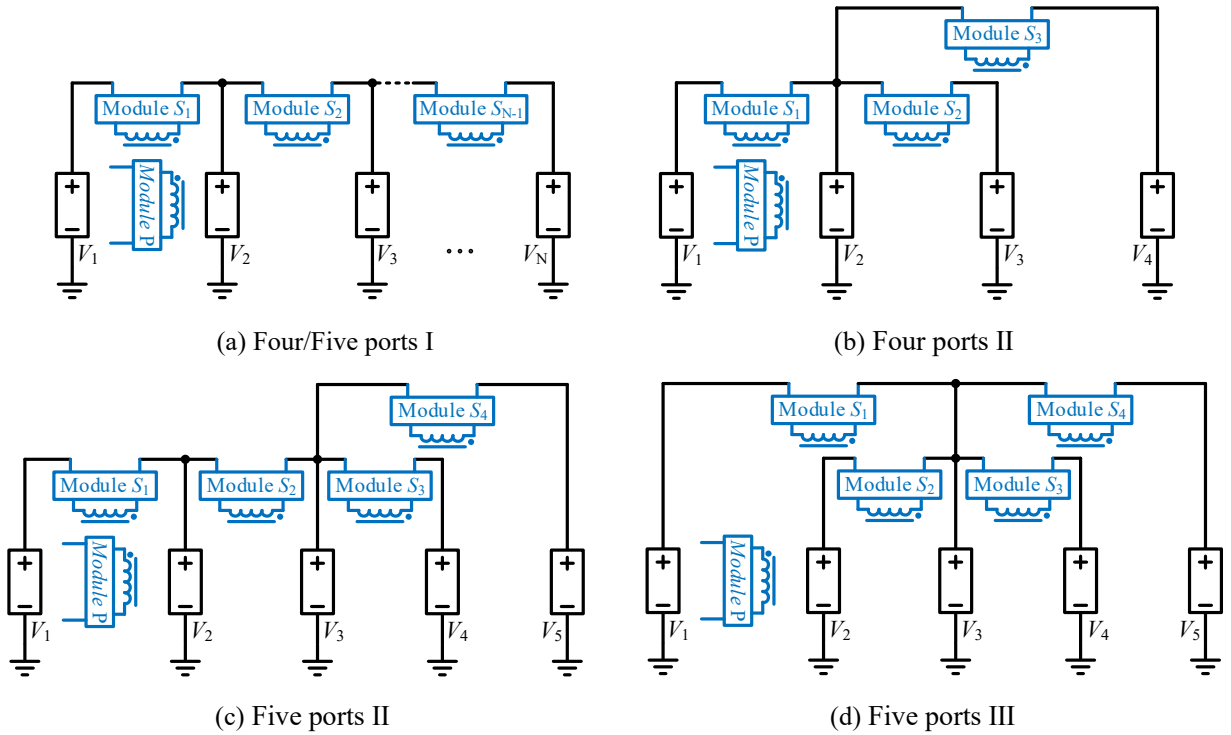

Figure 2.15 The selected TAB-based PPP three-port dc–dc converter.

## 2.5 Expanding To More Ports

In addition to the derived PPP three-port dc–dc structures, this thesis also explores possible PPP architectures with more ports. According to the PPP principle, Module *S* and Module *P* are utilized to manage the partial power caused by voltage and current differences, respectively. Each pair of dc ports must be equipped with at least one series-connected Module *S* to handle the partial power generated by the voltage difference. Furthermore, since all the positive terminals of the dc ports are interconnected through the series-connected modules, only one Module *P*, connected in parallel with one dc port, is required to maintain current balance in PPP more-port architectures.

Following this derivation principle, the PPP four and five ports dc–dc architectures are presented in Figure 2.16. These configurations do not specify the polarity of Module $S_1$~$S_{N-1}$(N

= 4 or 5), the position of Module *P*, and whether ports $V_1$~$V_N$(N = 4 or 5) are input or output. Figure 2.16 illustrates the minimal connection structures that adhere to the PPP principles while using the fewest modules. Based on this approach, the number of the PPP four-port and five-port dc–dc structures can be further expanded by allowing the dc ports to be either inputs or outputs, defining the polarities of Module $S_1$~$S_{N-1}$(N = 4 or 5), and selecting which dc port should be connected in parallel with Module *P*. As long as voltage and current balance are maintained, the derived topologies for both the PPP four-port and five-port configurations are similar to those of the three-port topology family.




(a) Four/Five ports I

(b) Four ports II

(c) Five ports II

(d) Five ports III

Figure 2.16 PPP more-port configurations.

## 2.6 Conclusions

This chapter introduces a novel modularized derivation method for the general PPP three-port dc–dc topology, designed to deliver a wide array of highly efficient configurations suitable for various applications. The foundational concept begins with the two-port isolated dc–dc converter within a typical PPP two-port structure, which can be conceptualized as two isolated modules: one connected in series between the source and load, and the other in parallel with either the

source or the load. This framework allows for a re-interpretation of the essential principles of PPP, where the series-connected module is responsible for processing the partial power resulting from the voltage difference between the source and load, while the parallel-connected module addresses the current imbalance.

Building on this modular interpretation, the derivation method for the three-port topology is established, stipulating that at least one series module is required for each pair of dc ports to manage voltage discrepancies, in addition to one parallel module for all dc ports to maintain current balance. This methodology is both straightforward and effective.

Following the proposed principles, nine distinct PPP three-port topologies have been derived. A thorough comparison of these topologies was undertaken, emphasizing selection criteria based on critical performance metrics such as partial power ratio, voltage gain, and current stress. The analysis indicates specific preferences for topology selection under varying operational conditions. For instance, topologies *Aj*(*j=l, m or r*) and *il* (*i=A*, *B* or *C*) are recommended when focusing on the partial power ratio. Additionally, topologies *Aj* and *Cj* are advantageous to retain a relatively small current stress under conditions of $I_lI_r>0$ and $I_lI_r<0$, respectively. In practical applications, it is imperative to consider these factors holistically, with the final topology selection involving a careful trade-off among the aforementioned criteria. An example application has been provided, guiding the selection of the most suitable topology based on these considerations.

Moreover, the proposed derivation principle indicates the potential for extending the PPP framework from three ports to four, five, or more ports. Subsequent work will involve designing the selected PPP three-port DC-DC converter and conducting experiments to verify the feasibility and rationality of the proposed topology. Through this comprehensive approach, this chapter lays the foundation for future advancements in multiport power processing systems, addressing both theoretical and practical challenges.

# Chapter 3

# PPP Multiport DC–DC Converter with Radial Module Connections

Building on the novel PPP derivation principle introduced in Chapter 2, several PPP multiport structures have been derived. For the example SIDO application, the topology shown in Figure 2.15 was selected. In this chapter, the selected topology will be expanded into a multiport structure with radial module connections. Detailed analysis of the PPP multiport dc–dc converter with radial module connections for single-input multi-output (SIMO) and multi-input single-output (MISO) applications will be provided. The connection schemes, TAB-based operational principles of the PPP-SIDO dc–dc converter, calculations, design considerations, and experimental verifications will be shown in the following sections.

## 3.1 Proposed PPP Multiport DC–DC Architecture with Radial Module Connections

Following the modularization, principle and selection criteria described in Chapter 2, a SIMO dc–dc architecture with radial module connections is shown in Figure 3.1(a). Similarly, a PPP-MISO dc–dc architecture is also shown in Figure 3.1(b).

More specifically, from Figure 3.1, N+1 magnetically linked modules are employed to give N+1 ports. One terminal of all modules $M_1 \sim M_{N+1}$ is connected to a centre point, resulting in a radial architecture. The other terminals of modules $M_1 \sim M_N$ are connected to the positive pole of outputs (inputs) $V_{o1} \sim V_{oN}$($V_{i1} \sim V_{iN}$). In addition, module $M_{N+1}$ is in parallel with the single input(output) $V_{i1}$($V_{o1}$). All input and output share a common ground. In this radial structure, the number of outputs in Figure 3.1(a) and inputs in Figure 3.1(b) can be flexibly added or reduced, and the implementation of the modules can be selected based on the application requirements. Moreover, the output(input) voltage $V_{o(i)k}$($k$ = 1, 2, …, N) can be designed to be greater or smaller

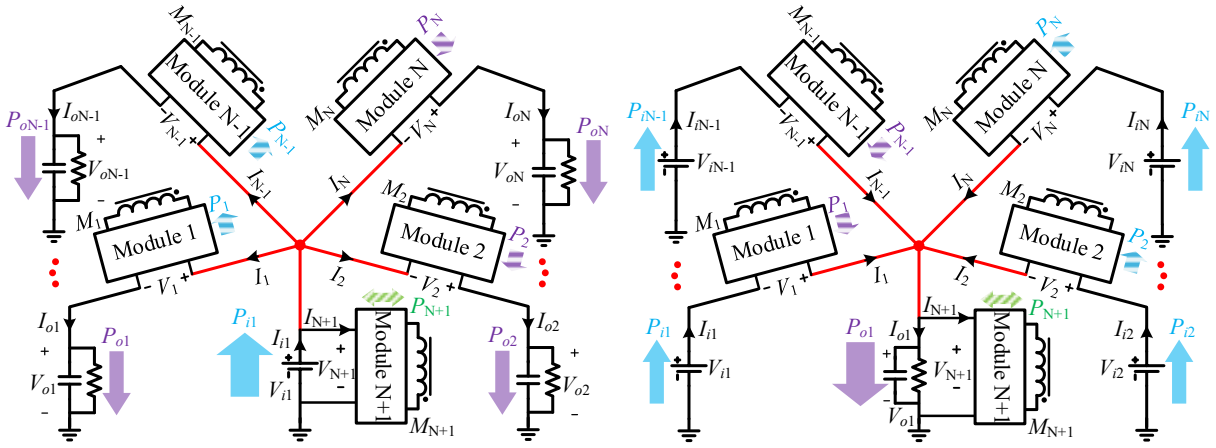



Figure 3.1 Proposed PPP dc–dc architecture with radial module connections. (a) Single-input multi-output. (b) Multi-input single-output.

than the single input(output) voltage $V_{i1}$($V_{o1}$) by adjusting the polarity of the module voltage $V_k$($k$ = 1, 2, …, N). In addition, voltage/current reduction is achieved for all the modules, and only a part of the system power is processed through modules, contributing to high efficiency and high-power density. As a result of the radial module connections, the two architectures in Figure 3.1 are equipped with strong fault tolerance capability that the damage of a certain series-connected module will only affect the output(input) port connected to it, while the other outputs(inputs) has the possibility of continuing to work.

Take Figure 3.1(a) as an example to explain the favorable PPP merit of the proposed architecture. The currents of the modules, output ports and input port are defined as $I_1$~$I_{N+1}$, $I_{o1}$~$I_{oN}$ and $I_{i1}$, respectively. The power processed by module $M_k$($k$ = 1, 2, …, N) is calculated in (3.1). When $V_{ok} < V_{i1}$, $P_k$ flows out of the module. In contrast, $P_k$ flows into the module when $V_{ok} > V_{i1}$. In addition, the processed power $P_k$ decreases with reduced module voltage, resulting from the reduced voltage difference between input $V_{i1}$ and output $V_{ok}$. Therefore, if the values of $V_{ok}$ approach $V_{i1}$, the required processing power of module $M_k$ is reduced, and under this condition, the sum of output currents $I_{o1}$~$I_{oN}$ is also near the input current $I_{i1}$ according to the power balance principle. Hence, the power processed by module $M_{N+1}$ is also small, as shown in (3.1). With different load conditions, $P_{N+1}$ is bidirectional. The ratio of the module power $P_p$ to the total system power $P_t$ is expressed in equation (3.2) using absolute values. To illustrate this relationship, consider a single-input dual-output system with the following parameters $V_{i1}$ = 400

V, $V_{o1}$ = 320 V and $V_{o2}$ = 480 V. Based on (3.2), the variation of the power ratio $P_p/P_t$ as a function of output currents $I_{o1}$ and $I_{o2}$ is demonstrated in Figure 3.2, where the current values are normalized with a per-unit base current of 2.5 A. From Figure 3.2, the maximum value 0.25 is achieved for $P_p/P_t$ when $I_{o2}$ = 0 A, which is much smaller than 1. Moreover, a minimum value of 0.1 is obtained when $(V_{i1}-V_{o1})\times I_{o1}$ equals $(V_{o2}-V_{i1})\times I_{o2}$. Therefore, only a small part of the power needs to be processed by modules $M_1 \sim M_{N+1}$, especially when the difference between the input voltage and output voltage is small. Hence, the voltage or current stresses of the components in these modules are successfully reduced, contributing to low cost and high-power density.

$$\begin{cases} P_k = V_k I_k = (V_{i1} - V_{ok}) I_{ok}, k = 1, 2..., N \\ P_{N+1} = V_{N+1} I_{N+1} = V_{i1} (I_{i1} - \sum_{k=1}^{N} I_{ok}) \end{cases} \tag{3.1}$$

$$\frac{P_p}{P_t} = \frac{\sum_{k=1}^{N} |P_k| + |P_{N+1}|}{\sum_{k=1}^{N} |P_{ok}| + |P_{i1}|} = \frac{\sum_{k=1}^{N} |V_{i1} - V_{ok}| I_{ok} + V_{i1} \left| I_{i1} - \sum_{k=1}^{N} I_{ok} \right|}{2 V_{i1} I_{i1}} \tag{3.2}$$

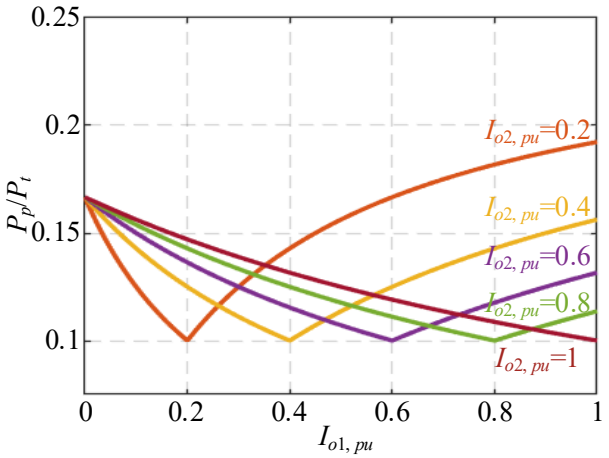



Figure 3.2 Relationship among output currents $I_{o1}$, $I_{o2}$ and the power ratio $P_p/P_t$ in the example single-input dual-output system.

Due to the PPP ability, the efficiency of the proposed multiport architecture should also be high. The power transmission efficiency of the modules and the PPP converter are defined as $\eta_p$ and $\eta_t$, respectively. Because only the partial power is processed by modules, while the other is delivered directly through wire with nearly 100% efficiency, the total efficiency $\eta_t$ are calculated in (3). From (3), $\eta_t$ is always larger than $\eta_p$ since $P_p$ is smaller than $P_t$. Moreover, the smaller the ratio $P_p$ to $P_t$ is, the higher the global efficiency $\eta_t$ that can be attained.

$$\eta_t = \frac{P_p\eta_p + P_t - P_p}{P_t} = \eta_p + \frac{\left(P_t - P_p\right)\left(1-\eta_p\right)}{P_t} > \eta_p \tag{3.3}$$

## 3.2 Operational Principle of An Example TAB-Based PPP-SIDO DC–DC Converter

To better understand the operational principle of the proposed PPP multiport dc–dc architecture with radial module connections in Figure 3.1, a SIDO example with three active bridge modules $M_1$~$M_3$ as in Figure 3.3 will be introduced in detail. It has an input port $V_{i1}$, two output ports $V_{o1}$~$V_{o2}$, and it is assumed that $V_{o1} < V_{i1} < V_{o2}$. Each module $M_i(i = 1, 2, 3)$ consists of four switches $S_{i1}$~$S_{i4}(i = 1, 2, 3)$, an inductor $L_i(i = 1, 2, 3)$ and a winding of the transformer with turn numbers $N_i(i = 1, 2, 3)$. $M_1$ and $M_2$ are connected in series, and $M_3$ is connected in parallel with $V_{i1}$. In addition, the positive terminal of $M_1$ and the negative terminal of $M_2$ are connected to the positive terminal of $M_3$. Owing to this structure, only a small partial power $P_1$~$P_3$ is converted through modules $M_1$~$M_3$, while the other large part of the power is delivered directly from $V_{i1}$ to $V_{o1}$ and $V_{o2}$.

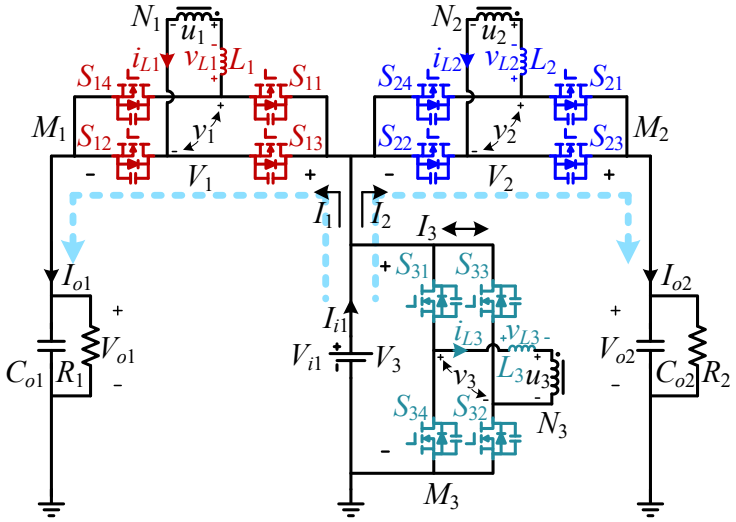



Figure 3.3 Circuit diagram of the proposed TAB-based PPP-SIDO dc–dc converter.

### 3.2.1 TAB-Based Analysis and Calculations

The following analysis and calculations related to the TAB converter are based on references [128, 129]. From Figure 3.3, the structure of the three-winding transformer with series inductors

is re-drawn in Figure 3.4(a), where $v_1$~$v_3$ are the square waves controlled by the phase shift angles $\varphi_{12}$ and $\varphi_{13}$, which are shown in Figure 3.5. Figure 3.5 presents the drive signals of switches $S_{i1}$~$S_{i4}$($i$ = 1, 2, 3) are $v_{gsi1}$~$v_{gsi4}$($i$ = 1, 2, 3), respectively. $S_{i1}$ and $S_{i2}$ are switched synchronously, as are $S_{i3}$ and $S_{i4}$. Moreover, $S_{i1}$ and $S_{i3}$ are activated in a complementary fashion with a 50% duty cycle. The phase shift angles of $v_{gs21}$ and $v_{gs31}$ with respect to $v_{gs11}$ are defined as $\varphi_{12}$ and $\varphi_{13}$, respectively. The phase shift angles $\varphi_{12}$ and $\varphi_{13}$ in radians are employed to regulate the power flows among the three modules $M_1$~$M_3$.

To conveniently calculate the inductor voltage $v_{Li}$($i$ = 1, 2, 3), the corresponding star-equivalent transformation is given in Figure 3.4(b) [128], where $v'_2 = v_2 \times N_1/N_2$, $v'_3 = v_3 \times N_1/N_3$, $L'_2 = L_2 \times N_1^2/N_2^2$ and $L'_3 = L_3 \times N_1^2/N_3^2$, which represent the primary referred values of voltages $v_2$ and $v_3$, and the inductances $L_2$ and $L_3$, respectively. In addition, the triangle-equivalent model can be derived from the star-equivalent model, as shown in Figure 3.4(c) [128], where $L_{12} = L_1+L'_2+L_1L'_2/L'_3$, $L_{13} = L_1+L'_3+L_1L'_3/L'_2$, and $L_{23} = L_2+L'_3+L_2L'_3/L'_1$.

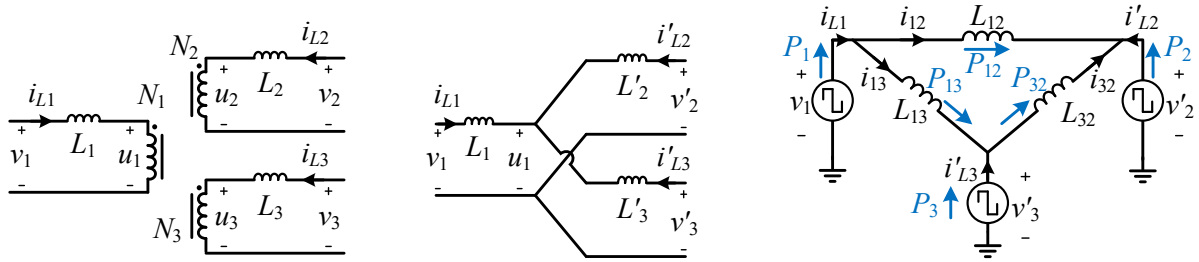



Figure 3.4 Structure of a three-winding transformer with series inductors [128]. (a) Re-drawn structure. (b) Its star-equivalent model. (c) Its triangle-equivalent model.

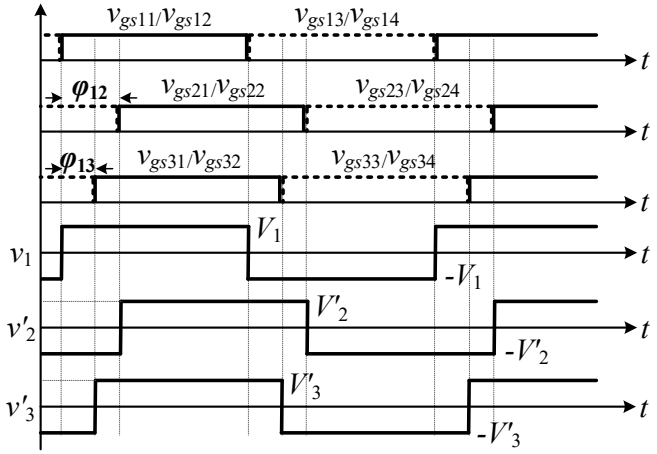



Figure 3.5 Key waveforms showing the phase shift angles of the drive signals among three active bridges.

Based on the star-equivalent model shown in Figure 3.4(b) and the superposition theorem, the voltages $u_i(t)(i = 1, 2, 3)$ are calculated in (3.4), where the voltage $v_i(t)(i = 1, 2, 3)$ is decided by on/off switching modes, as shown in (3.5). When switch $S_{i1}$ is turned on, $v_i(t) = V_i$, while $v_i(t) = -V_i$ when $S_{i1}$ is turned off. According to (3.4) and (3.5), the inductor voltages $v_{Li}(t) = v_i(t) - u_i(t)(i = 1, 2, 3)$ are finally calculated in (3.6). The calculation of the inductor voltage $v_{Li}(t)$ will help directly show the currents trend of inductors in different working states of a switching period. In addition, when the voltage ratios and inductance ratios align with the transformer turns ratio, specifically $N_1:N_2:N_3 = V_1:V_2:V_3$ and $N_1^2:N_2^2:N_3^2 = L_1:L_2:L_3$, the parameters $m_1 \sim m_3$ in equation (3.4) can be simplified to 1/3. This significantly streamlines both the calculations and the analysis.

$$\begin{bmatrix} u_1(t) \\ u_2(t) \\ u_3(t) \end{bmatrix} = \begin{bmatrix} m_1 & m_2 N_{12} & m_2 N_{13} \\ m_1 N_{21} & m_2 & m_3 N_{23} \\ m_1 N_{31} & m_2 N_{32} & m_3 \end{bmatrix} \begin{bmatrix} v_1(t) \\ v_2(t) \\ v_3(t) \end{bmatrix} \tag{3.4}$$

where $m_1 = \dfrac{L_2' L_3' / (L_2' + L_3')}{L_1 + L_2' L_3' / (L_2' + L_3')}$, $m_2 = \dfrac{L_1 L_3' / (L_1 + L_3')}{L_2 + L_1 L_3' / (L_1 + L_3')}$, $m_3 = \dfrac{L_1 L_2' / (L_1 + L_2')}{L_3 + L_1 L_2' / (L_1 + L_2')}$, and $N_{xy} = N_x / N_y, (x, y = 1, 2, 3)$.

$$\begin{cases} v_i(t) = q_i(t) \times V_i, i = 1, 2, 3 \\ q_i(t) = \begin{cases} 1, S_{i1} = on \\ -1, S_{i1} = off \end{cases} \end{cases} \tag{3.5}$$

$$v_{Li}(t) = q_i(t) V_i - \sum_{k=1}^{3} \frac{N_i}{N_k} m_k q_k(t) V_k, (i = 1, 2, 3) \tag{3.6}$$

The expressions derived from star-equivalent model in Figure 3.4(b) heavily depend on the turns ratios $N_1 \sim N_3$, the inductances $L_1 \sim L_3$, and the combined effect of three voltages $v_1 \sim v_3$. If the voltages $v_1 \sim v_3$ and the inductances $L_1 \sim L_3$ do not correspond to the turns ratios $N_1 \sim N_3$, the parameters $m_1 \sim m_3$ in equation (3.4) cannot be simplified to the fixed value of 1/3, resulting in overly complex calculations and analyses. By contrast, based on the triangle-equivalent model Figure 3.4(c), the analysis of the inductor $L_{12}$, as an example, will only need to consider two voltages and one phase shift angle, ignoring the matching of parameters, which is similar to the traditional dual active bridge circuit. Then, the actual inductor current $i_{L1}$ can be obtained by simply adding the $i_{L12}$ and $i_{L13}$ together. A more detailed operational principle and analysis based on traditional DAB model and triangle model will be illustrated as follows [129].

According to Figure 3.5, the phase shift between $v_1$ and $v_2$ is $\varphi_{12}$. Then the traditional DAB model based on $L_{12}$ in triangle model of Figure 3.4(c) can be obtained in Figure 3.6.

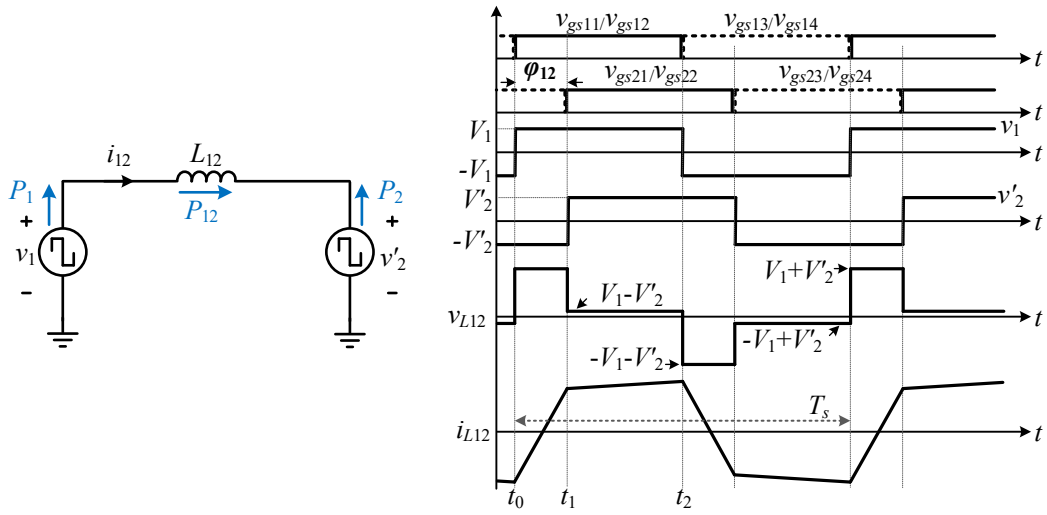



Figure 3.6 Fundamental model for the DAB converter with phase shift $\varphi_{12}$.

In the first half switching cycles, i.e., $t_0$~$t_2$, the inductor current $i_{L12}$ can be expressed as

$$\begin{cases} i_{L12}(t_1) = i_{L12}(t_0) + \dfrac{V_{s1} + V'_{s2}}{\omega_s L_{12}} \cdot \varphi_{12} \\ i_{L12}(t_2) = i_{L12}(t_1) + \dfrac{V_{s1} - V'_{s2}}{\omega_s L_{12}} \cdot (\pi - \varphi_{12}) \end{cases} \tag{3.7}$$

where $\omega_s = 2\pi/T_s$.

Due to the symmetry of DAB that the average current of the inductor over one switching period should be zero, giving formula (3.8). Combining (3.7) and (3.8), we can get $i_{L12}(t_0)$ in (3.9).

$$i_{L12}(t_0) = -i_{L12}(t_2) \tag{3.8}$$

$$i_{L12}(t_0) = -\frac{1}{2}\left( \frac{V_{s1} + V'_{s2}}{\omega_s L_{12}} \cdot \varphi_{12} + \frac{V_{s1} - V'_{s2}}{\omega_s L_{12}} \cdot (\pi - \varphi_{12}) \right) \tag{3.9}$$

In traditional DAB model, the phase shift of $v_{gs21}$ with respect to $v_{gs11}$ is $\varphi_{12}$. If $\varphi_{12}$ is larger than zero, the power is transferred from $v_1$ to $v_2$, and it is defined as $P_{12}$. $P_{12}$ can be obtained by firstly calculating the average current $I_{12}$, as shown in (3.10). Then the power $P_{12}$ is expressed in (3.11).

$$I_{12}=\frac{\int_0^{\varphi_1-\varphi_2}\left(i_{L12}(t_0)+\frac{V_{s1}+V'_{s2}}{\omega L_{12}}\theta\right)d\theta+\int_{\varphi_1-\varphi_2}^{\pi}\left(i_{L12}(t_1)+\frac{V_{s1}-V'_{s2}}{\omega L_{12}}\theta\right)d\theta}{\pi}$$
$$=\frac{V'_{s2}}{\omega L_{12}}\varphi_{12}\left(1-\frac{\varphi_{12}}{\pi}\right) \tag{3.10}$$

$$P_{12}=V_{s1}\cdot I_{12}=\frac{V_{s1}V'_{s2}}{\omega L_{12}}\varphi_{12}\left(1-\frac{\varphi_{12}}{\pi}\right)=\frac{V_{s1}V_{s2}N_1}{\omega L_{12}N_2}\varphi_{12}\left(1-\frac{\varphi_{12}}{\pi}\right) \tag{3.11}$$

Applying the abovementioned analysis into the triangle-equivalent model in Figure 3.4(c), three virtual equivalent power $P_{12}$, $P_{13}$ and $P_{32}$ can be obtained in (3.12).

$$\begin{cases} P_{12}=-P_{21}=\dfrac{V_1V_2N_1}{\omega L_{12}N_2}\varphi_{12}\left(1-\dfrac{\varphi_{12}}{\pi}\right) \\ P_{13}=-P_{31}=\dfrac{V_1V_3N_1}{\omega L_{13}N_3}\varphi_{13}\left(1-\dfrac{\varphi_{13}}{\pi}\right) \\ P_{32}=-P_{23}=\dfrac{V_3V_2N_1^2}{\omega L_{32}N_3N_2}(\varphi_{12}-\varphi_{13})\left(1-\dfrac{(\varphi_{12}-\varphi_{13})}{\pi}\right) \end{cases} \tag{3.12}$$

Based on the power direction defined in Figure 3.4(c), the final practical port power $P_1$~$P_3$ can be expressed in (3.13). The practical inductor current can be obtained similarly after superposition, as shown in (3.14).

$$\begin{cases} P_1=P_{12}+P_{13} \\ P_2=-P_{12}-P_{32} \\ P_3=-P_{13}+P_{32} \end{cases} \tag{3.13}$$

$$\begin{cases} i_{L1}=i_{L12}+i_{L13} \\ i_{L2}=(-i_{L12}-i_{L32})N_1/N_2 \\ i_{L3}=(-i_{L13}+i_{L32})N_1/N_3 \end{cases} \tag{3.14}$$

### 3.2.2 Operational Principle of the Proposed TAB-Based PPP-SIDO DC–DC Converter

To demonstrate the waveforms of each working mode more intuitively, and due to the matched parameters $N_1$:$N_2$:$N_3$ = $V_1$:$V_2$:$V_3$ and $N_1^2$:$N_2^2$:$N_3^2$ = $L_1$:$L_2$:$L_3$, contributing to simplified calculation and analysis, the expressions derived from star-equivalent model in Figure 3.4(b) will be used in this section.

The key operation waveforms of the TAB-based PPP-SIDO dc–dc converter are shown in Figure 3.7. The drive signals $v_{gsi1}$~$v_{gsi4}$($i$ = 1, 2, 3) are the same as those presented shown in Figure 3.5, with the addition of dead time to prevent shorting the power supply and to facilitate soft switching. The phase shift angles of $v_{gs21}$ and $v_{gs31}$ with respect to $v_{gs11}$ are defined as $\varphi_{12}$ and $\varphi_{13}$, respectively.

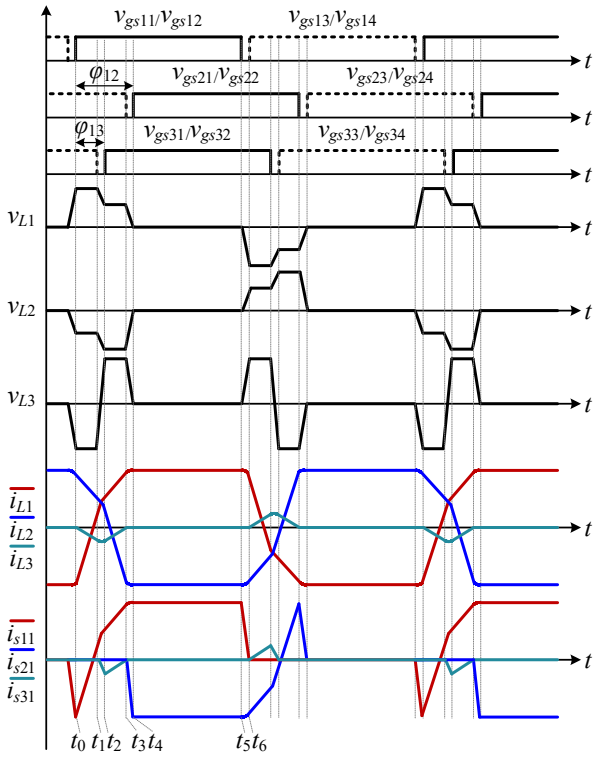



Figure 3.7 Key operation waveforms of the proposed TAB-based PPP-SIDO dc–dc converter.

From Figure 3.7, the half switching period $T_s/2$ of $v_{gs11}$ can be divided into six states ($t_0$~$t_6$) with phase shift relationships $\pi/2 > \varphi_{12} > \varphi_{13} > 0$. The corresponding values of $q_i(t)$($i$ = 1, 2, 3) in different states are given in Table 3.1 and the equivalent circuits of six states ($t_0$~$t_6$) are also shown in Figure 3.8.

Table 3.1

VALUES OF $q_i(t)$($i$ = 1, 2, 3) IN DIFFERENT STATES

| Value | ($t_0$~$t_1$) | ($t_2$~$t_3$) | ($t_4$~$t_5$) |
|---|---|---|---|
| $q_1(t)$ | 1 | 1 | 1 |
| $q_2(t)$ | −1 | −1 | 1 |
| $q_3(t)$ | −1 | 1 | 1 |

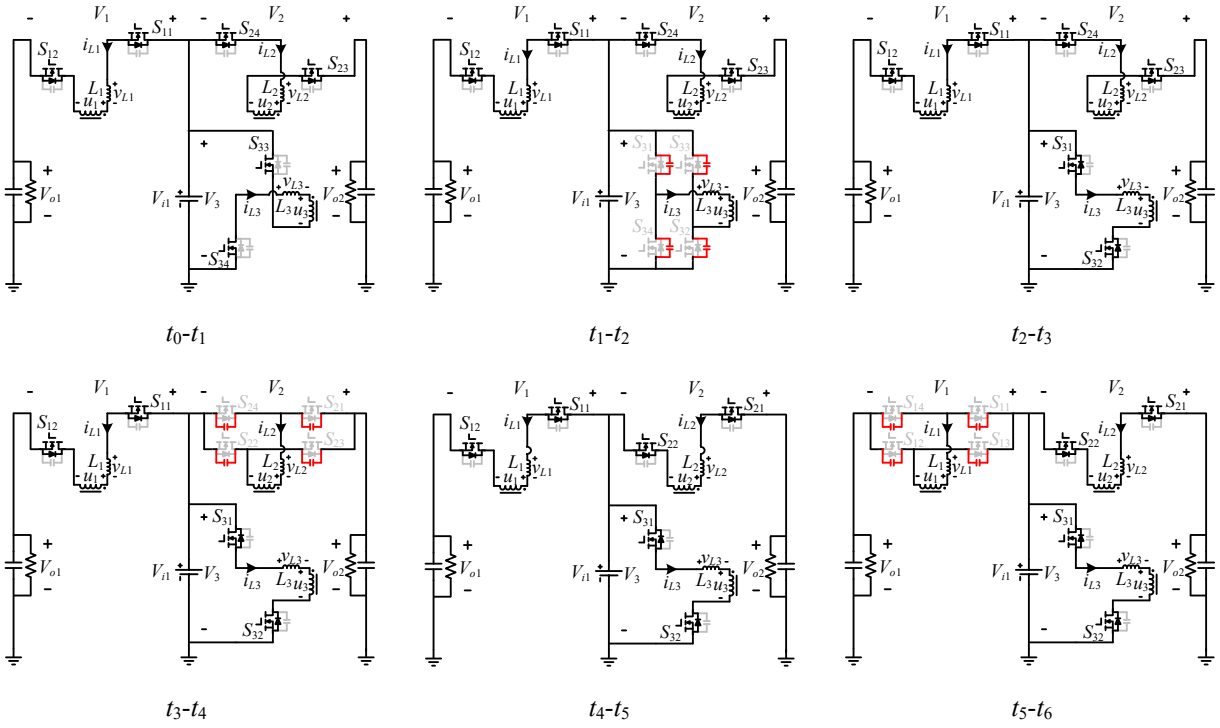



Figure 3.8 Equivalent circuits of six states $t_0$-$t_6$. $t_0$-$t_1$ $t_1$-$t_2$ $t_2$-$t_3$ $t_3$-$t_4$ $t_4$-$t_5$ $t_5$-$t_6$.

1) State 1 ($t_0$~$t_1$): $S_{11}$ and $S_{12}$ are turned ON at $t_0$. In addition, $S_{23}$, $S_{24}$, $S_{33}$, and $S_{34}$ also remain conducting in this state. According to (3.6) and Table 3.1, the three inductor voltages are $v_{L1} = 4\times V_1/3$, $v_{L2} = -2\times V_2/3$ and $v_{L3} = -2\times V_3/3$. Hence, the inductor current $i_{L1}$ increases, while $i_{L2}$ and $i_{L3}$ decrease linearly, as calculated in (3.15). Accordingly, $V_{i1}$ charges $V_{o1}$, $V_{o2}$ and $L_1$ at the same time, while inductors $L_2$ and $L_3$ are discharged.

$$\begin{cases} i_{L1}(t) = i_{L1}(t_0) + \dfrac{4}{3}\cdot\dfrac{V_1}{L_1}(t-t_0) \\ i_{L2}(t) = i_{L2}(t_0) - \dfrac{2}{3}\cdot\dfrac{V_2}{L_2}(t-t_0) \\ i_{L3}(t) = i_{L3}(t_0) - \dfrac{2}{3}\cdot\dfrac{V_3}{L_3}(t-t_0) \end{cases} \tag{3.15}$$

2) State 2 ($t_1$~$t_2$): $S_{33}$ and $S_{34}$ are turned OFF at $t_1$. Subsequently, the inductor $L_3$ starts to resonate with the parasitic capacitors $C_{s31}$~$C_{s34}$ of switches $S_{31}$~$S_{34}$, as illustrated in (3.16), where the drain-to-source voltages $v_{s31}(t)$ and $v_{s32}(t)$ are decreased.

$$\begin{cases} (C_{s31}+C_{s34})\dfrac{dv_{s31}(t)}{dt} = (C_{s32}+C_{s33})\dfrac{dv_{s32}(t)}{dt} = i_{L3}(t) \\ -L_3\dfrac{di_{L3}(t)}{dt} = v_{s31}(t) + v_{s32}(t) + u_3(t) - V_3 \end{cases} \tag{3.16}$$

3) State 3 ($t_2$~$t_3$): After discharging of $C_{s31}$ and $C_{s32}$, the body diodes of switches $S_{31}$ and $S_{32}$ conduct; thereby, their drain-to-source voltages are clamped to zero. Switches $S_{31}$ and $S_{32}$ are turned ON at $t_2$, which indicates that zero-voltage-switching (ZVS) turn-ON is achieved. In this state, $v_{L1} = 2\times V_1/3$, $v_{L2} = -4\times V_2/3$ and $v_{L3} = 2\times V_3/3$. The corresponding inductor currents are given in (3.17). Therefore, $V_{o1}$, $V_{o2}$, $L_1$ and $L_3$ are charged by $V_{i1}$, while $L_2$ is discharged.

$$\begin{cases} i_{L1}(t) = i_{L1}(t_0) + \dfrac{4}{3}\cdot\dfrac{V_1}{L_1}\cdot\dfrac{\varphi_{13}}{2\pi}\cdot T_s + \dfrac{2}{3}\cdot\dfrac{V_1}{L_1}(t-t_1) \\ i_{L2}(t) = i_{L2}(t_0) - \dfrac{2}{3}\cdot\dfrac{V_2}{L_2}\cdot\dfrac{\varphi_{13}}{2\pi}\cdot T_s - \dfrac{4}{3}\cdot\dfrac{V_2}{L_2}(t-t_1) \\ i_{L3}(t) = i_{L3}(t_0) - \dfrac{2}{3}\cdot\dfrac{V_3}{L_3}\cdot\dfrac{\varphi_{13}}{2\pi}\cdot T_s + \dfrac{2}{3}\cdot\dfrac{V_3}{L_3}(t-t_1) \end{cases} \tag{3.17}$$

4) State 4 ($t_3$~$t_4$): $S_{23}$ and $S_{24}$ are turned OFF at $t_3$, and the resonance among inductor $L_2$ and parasitic capacitors $C_{s21}$~$C_{s24}$ begins. The resonance formula is shown in (3.18), where $C_{s21}$ and $C_{s22}$ are discharged, while $C_{s23}$ and $C_{s24}$ are charged.

$$\begin{cases} (C_{s21}+C_{s24})\dfrac{dv_{s21}(t)}{dt} = (C_{s22}+C_{s23})\dfrac{dv_{s22}(t)}{dt} = i_{L2}(t) \\ -L_2\dfrac{di_{L2}(t)}{dt} = v_{s21}(t) + v_{s22}(t) + u_2(t) - V_2 \end{cases} \tag{3.18}$$

5) State 5 ($t_4$~$t_5$): When $v_{s21}$(t) and $v_{s22}$(t) drop to zero, the corresponding body diodes conduct; therefore, these two drain-to-source voltages are clamped to zero before $t_4$. ZVS turn-ON of switches $S_{21}$ and $S_{22}$ is realized when they are turned ON at $t_4$. Subsequently, the inductor voltages are all changed to zero such that their inductor currents are constant, as shown in (3.19). In this state, $V_{i1}$ only charges $V_{o1}$ and $V_{o2}$.

$$\begin{cases} i_{L1}(t) = i_{L1}(t_0) + \dfrac{4}{3}\cdot\dfrac{V_1}{L_1}\cdot\dfrac{\varphi_{13}}{2\pi}\cdot T_s + \dfrac{2}{3}\cdot\dfrac{V_1}{L_1}\dfrac{(\varphi_{12}-\varphi_{13})}{2\pi}\cdot T_s \\ i_{L2}(t) = i_{L2}(t_0) - \dfrac{2}{3}\cdot\dfrac{V_2}{L_2}\cdot\dfrac{\varphi_{13}}{2\pi}\cdot T_s - \dfrac{4}{3}\cdot\dfrac{V_2}{L_2}\dfrac{(\varphi_{12}-\varphi_{13})}{2\pi}\cdot T_s \\ i_{L3}(t) = i_{L3}(t_0) - \dfrac{2}{3}\cdot\dfrac{V_3}{L_3}\cdot\dfrac{\varphi_{13}}{2\pi}\cdot T_s + \dfrac{2}{3}\cdot\dfrac{V_3}{L_3}\dfrac{(\varphi_{12}-\varphi_{13})}{2\pi}\cdot T_s \end{cases} \tag{3.19}$$

6) State 6 ($t_5$~$t_6$): $S_{11}$ and $S_{12}$ are turned OFF at $t_5$. Parasitic capacitors $C_{s11}$ and $C_{s12}$ are charged during resonance, as calculated in (3.20). Because $C_{s11}$ and $C_{s12}$ are charged, the drain-to-

source voltages $v_{s11}(t)$ and $v_{s12}(t)$ are increased. When $v_{gs13}$ and $v_{gs14}$ turn positive at $t_6$, the half switching period ends.

$$\begin{cases} \left(C_{s11}+C_{s14}\right)\dfrac{dv_{s13}(t)}{dt}=\left(C_{s12}+C_{s13}\right)\dfrac{dv_{s14}(t)}{dt}=-i_{L1}(t) \\ L_1\dfrac{di_{L1}(t)}{dt}=v_{s13}(t)+v_{s14}(t)-u_1(t)-V_1 \end{cases} \tag{3.20}$$

# 3.3 Characteristic Analysis and Design Considerations

Based on the operational principle of the proposed TAB-based PPP-SIDO dc–dc converter in Figure 3.3, the characteristics analysis and design considerations are introduced in this section based on the system parameters in Table 3.2. The transformer turns ratio is configured as $N_1$:$N_2$:$N_3$=1:1:5, which is determined by the voltage relationship ($V_{i1}$−$V_{o1}$):($V_{o2}$−$V_{i1}$):$V_{i1}$, to maintain consistency with the module voltage ratio, simplifying the parameters $m_1$∼$m_3$ in equation (3.4). The power gains will be calculated at first. Subsequently, the power flowing through three active bridge modules will be calculated and compared with the total system power. In addition, the hardware design will be given considering voltage and current stresses, working areas, and ZVS operation. Finally, small signal modeling and control design are also presented.

Table 3.2
SYSTEM PARAMETERS

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| Input Voltage $V_{i1}$ | 400 V | Output Current $I_{o1,\max}$ | 2.5 A |
| Output Voltage $V_{o1}$ | 320 V | Output Current $I_{o2,\max}$ | 2.5 A |
| Output Voltage $V_{o2}$ | 480 V | Turns Ratio $N_1$:$N_2$:$N_3$ | 1:1:5 |
| Switching Period $T_s$ | 10 $\mu$s | Series Inductance Ratio $L_1$:$L_2$:$L_3$ | 1:1:25 |

## 3.3.1 Power Calculation

The three active bridge modules in the proposed example PPP-SIDO converter construct a TAB converter. Combining the TAB-based calculations in (3.12) and (3.13), and the proposed PPP structure in Figure 3.3, the output power $P_{o1}$ and $P_{o2}$ controlled by phase shift angles $\varphi_{12}$

and $\varphi_{13}$ can be derived in (3.21) and (3.22). Amongst the expressions, $P_{12}$, $P_{13}$, and $P_{32}$ are virtual power flows according to the triangle-equivalent model in Figure 3.4(c).

$$\begin{cases} P_{12} = -P_{21} = \dfrac{(V_{i1} - V_{o1})(V_{o2} - V_{i1})N_1}{\omega L_{12} N_2} \varphi_{12}\left(1 - \dfrac{\varphi_{12}}{\pi}\right) \\ P_{13} = -P_{31} = \dfrac{(V_{i1} - V_{o1})V_{i1}N_1}{\omega L_{13} N_3} \varphi_{13}\left(1 - \dfrac{\varphi_{13}}{\pi}\right) \\ P_{32} = -P_{23} = \dfrac{V_{i1}(V_{o2} - V_{i1})N_1^2}{\omega L_{32} N_3 N_2}(\varphi_{12} - \varphi_{13})\left(1 - \dfrac{(\varphi_{12} - \varphi_{13})}{\pi}\right) \end{cases} \tag{3.21}$$

$$\begin{cases} P_{o1} = V_{o1} I_{o1} = V_{o1} \dfrac{P_{12} + P_{13}}{(V_{i1} - V_{o1})} \\ P_{o2} = V_{o2} I_{o2} = V_{o2} \dfrac{P_{12} + P_{32}}{(V_{o2} - V_{i1})} \end{cases} \tag{3.22}$$

Based on (3.21), (3.22) and the system parameters in Table 3.2, phase shift angles $\phi_{12}$ and $\phi_{13}$ under different output currents $I_{o1}$ and $I_{o2}$ are illustrated in Figure 3.9, where $\phi_{12}$ and $\phi_{13}$ are the angles corresponding to radians $\varphi_{12}$ and $\varphi_{13}$, and the per-unit current is set as 2.5A. From Figure 3.9, with the rise of $\phi_{12}$, both $I_{o1}$ and $I_{o2}$ are increased. When $\phi_{13}$ rises, $I_{o1}$ is increased while $I_{o2}$ is reduced. In short, the power flows of the proposed TAB-based PPP-SIDO dc–dc converter can be effectively controlled by phase shift angles $\phi_{12}$ and $\phi_{13}$.

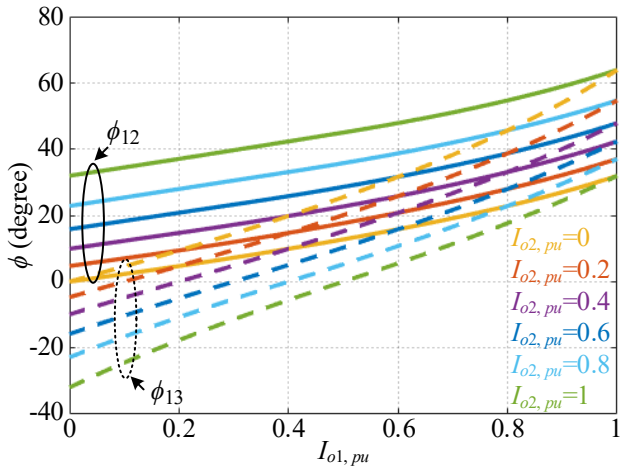



Figure 3.9 Graph showing the change of phase shift angles $\phi_{12}$ and $\phi_{13}$ with loads $I_{o1}$ and $I_{o2}$.

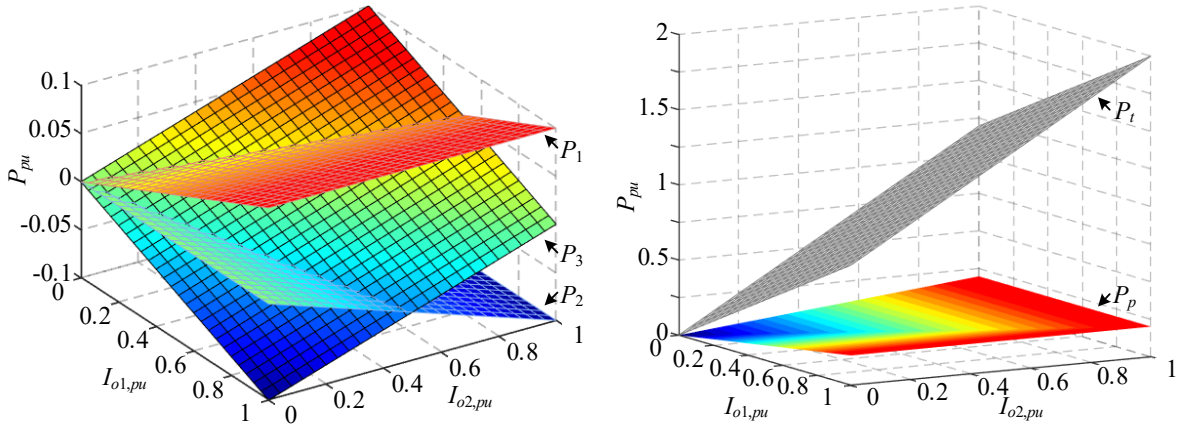
## 3.3.2 PPP-Based Power Flow Analysis

According to (3.1) and specific circuit in Figure 3.3, the partial powers $P_1$~$P_3$ flow through active bridge modules are given in (3.23). The sum of the partial power $P_p$ and the total system

power $P_t$ are also calculated in (3.24). Based on (3.23) and (3.24), the relationships among output currents and module powers $P_1$~$P_3$, i.e., partial powers, are presented in Figure 3.10(a), where the per-unit current and power are, respectively, 2.5 A and 2000 W. From Figure 3.10 (a), $P_1$ is always positive, $P_2$ is negative, and $P_3$ is bidirectional, which is decided by load conditions. Their maximum absolute values are 200 W, which is much smaller than the maximum output power $P_{o1}$ = 800 W, $P_{o2}$ = 1200 W and the maximum input power $P_{i1}$ = 2000 W. In addition, Figure 3.10 (b) also demonstrates the partial power $P_p$ and the total power $P_t$ under different output currents $I_{o1}$ and $I_{o2}$. Note that the partial power $P_p$ processed by modules is effectively reduced in comparison with the total power $P_t$ for any load condition.

$$\begin{cases} P_1 = V_1 I_1 = (V_{i1} - V_{o1}) I_{o1} \\ P_2 = V_2 I_2 = (V_{i1} - V_{o2}) I_{o2} \\ P_3 = V_3 I_3 = V_{i1} (I_{i1} - I_{o1} - I_{o2}) \end{cases} \tag{3.23}$$

$$\begin{cases} P_p = |P_1| + |P_2| + |P_3| \\ P_t = V_{i1} I_{i1} + V_{o1} I_{o1} + V_{o2} I_{o2} \end{cases} \tag{3.24}$$




(a) (b)

Figure 3.10 Relationships among $I_{o1}$, $I_{o2}$ and different power flows. (a) $P_1$~$P_3$ processed by modules $M_1$~$M_3$. (b) Partial power $P_p$ and total power $P_t$.

### 3.3.3 Hardware Design Considerations

First, for selecting the suitable semiconductors matching the system parameters, the RMS value of their current and the maximum value of voltage will be calculated. Due to symmetry, the absolute values of inductor currents $i_{Li}(t)$ and $i_{Li}(t+T_s/2)$ are equal, i.e., $i_{Li}$ $(t_0) = -i_L(t_6)$ in

Figure 3.7. According to (3.19), the inductor currents at $t_0$ are calculated in (3.25). Based on (3.25) and (3.15), the RMS currents $I_{si1,\mathrm{rms}}$ of switches $S_{i1}(i = 1, 2, 3)$ are calculated in (3.26). In addition, the corresponding voltage are shown in (3.27). In each active bridge module $M_i(i = 1, 2, 3)$, the RMS currents and the maximum voltages of the four switches are equal. Based on equations (3.26), (3.27), and system parameters in Table 3.2, the maximum RMS currents and voltages are 2.21 A and 400 V, respectively. Accordingly, MOSFET IPW60R180P7, with a drain-to-source voltage rating of 650 V, a pulsed drain current of 53 A, and a maximum on-state resistance of 180mΩ, is selected for switches $S_{i1}$~$S_{i4}$ in the prototype circuit. Although the maximum RMS current of the switch is less than 3 A, this MOSFET was chosen because it was the smallest current-rated switch tube available at the time of selection.

$$\begin{cases} i_{L1}(t_0) = \left(-\dfrac{1}{3}\varphi_{12} - \dfrac{1}{3}\varphi_{13}\right)\cdot\dfrac{V_1 T_s}{2\pi L_1} \\ i_{L2}(t_0) = \left(\dfrac{2}{3}\varphi_{12} - \dfrac{1}{3}\varphi_{13}\right)\cdot\dfrac{V_2 T_s}{2\pi L_2} \\ i_{L3}(t_0) = \left(-\dfrac{1}{3}\varphi_{12} + \dfrac{2}{3}\varphi_{13}\right)\cdot\dfrac{V_3 T_s}{2\pi L_3} \end{cases} \tag{3.25}$$

$$I_{si1,rms} = \sqrt{\frac{3\pi - 2\varphi_{12}}{6\pi} i_{Li}^2(t_0) + \frac{\varphi_{12}}{6\pi} i_{Li}^2(t_1) + \frac{2\varphi_{13} - \varphi_{12}}{6\pi} i_{Li}(t_0) i_{Li}(t_1)} \tag{3.26}$$

$$\begin{cases} V_{s11} = V_{i1} - V_{o1} \\ V_{s21} = V_{o2} - V_{i1} \\ V_{s31} = V_{i1} \end{cases} \tag{3.27}$$

The working areas and peak current are also considered for the design of the inductances. According to (3.12), (3.13) and system parameters in Table 3.2, the available ranges of power flows ($P_1$, $P_2$) in terms of the series inductance $L_1$ are generated in Figure 3.11, where $P_1$ is always positive, while $P_2$ is negative. $P_3$ is then decided by $-P_1-P_2$ due to power conservation. In addition, because the series inductance ratio is fixed by the voltage ratio, once inductance $L_1$ is decided, the other two inductances $L_{2,3}$ are also derived. From Figure 3.11, the smaller the inductance $L_1$ is, the larger the power range. On the other hand, the maximum absolute values of inductor currents $|i_{L1}|_{\max}$~$|i_{L3}|_{\max}$ occur in (3.28), which are derived from (3.15), (3.17), and (3.19). According to (3.28), the variation curve of the maximum absolute inductor currents $|i_{L1}|_{\max}$~$|i_{L3}|_{\max}$ as a function of the series inductance $L_1$ is shown in Figure 3.12. As $L_1$ decreases,

these currents also decrease, which negatively impacts the achievement of the ZVS operation for the switches. Therefore, the series inductance $L_1$ is ultimately set to 20 $\mu$H after a comprehensive consideration of both the power range and the ZVS operation.

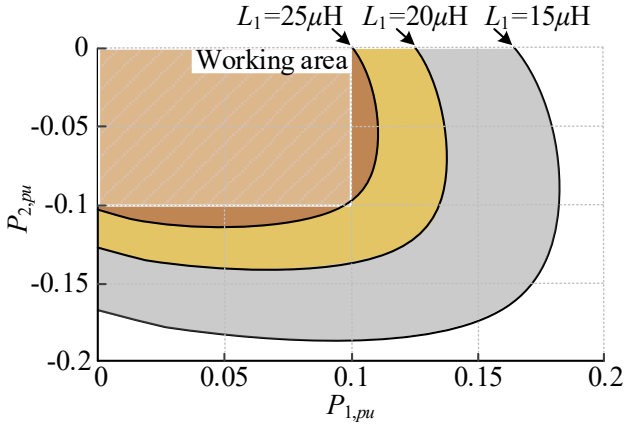



Figure 3.11 Feasible range of power flow ($P_1$, $P_2$) determined by inductance $L_1$ variations.

$$\begin{cases} i_{L1}(t_5)=\left(\dfrac{1}{3}\varphi_{12}+\dfrac{1}{3}\varphi_{13}\right)\cdot\dfrac{V_1T_s}{2\pi L_1}>0 \\ i_{L2}(t_3)=\left(-\dfrac{2}{3}\varphi_{12}+\dfrac{1}{3}\varphi_{13}\right)\cdot\dfrac{V_2T_s}{2\pi L_2}<0 \\ i_{L3}(t_1)=-\dfrac{1}{3}\varphi_{12}\cdot\dfrac{V_3T_s}{2\pi L_3}<0 \end{cases} \tag{3.28}$$

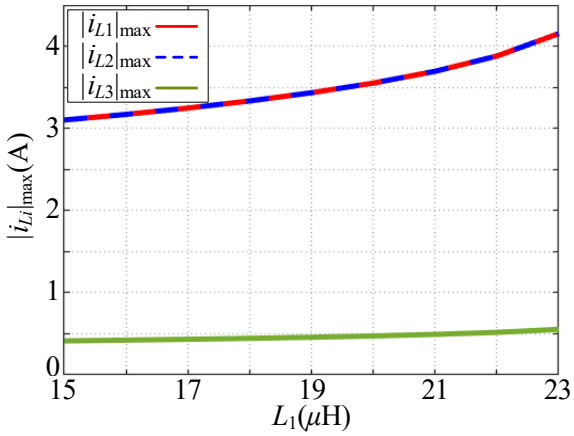



Figure 3.12 Maximum absolute inductor currents $i_{L1,max}$~$i_{L3,max}$ in terms of series inductance $L_1$.

Finally, ZVS operation is designed. From the analysis in Section 3.2.2, switches $S_{11}$, $S_{12}$, $S_{23}$, $S_{24}$, $S_{33}$, and $S_{34}$ are turned ON before $t_1$, and the inductor current $i_{L3}(t_1)$ is calculated in (3.28), which is negative. When $S_{33}$ and $S_{34}$ are turned OFF at $t_1$, the inductor $L_3$ will resonate with the

parasitic capacitors $C_{s31}$~$C_{s34}$, as shown in Figure 3.13. The capacitors $C_{s31}$~$C_{s32}$ are discharged, while $C_{s33}$~$C_{s34}$ are charged. According to Figure 3.13 and (3.4), the expression of $u_3$(t) during $t_1$ to $t_2$ is calculated in (3.29). Combining with (3.16), the drain-to-source voltage $v_{s31}$(t) is calculated in (3.30).

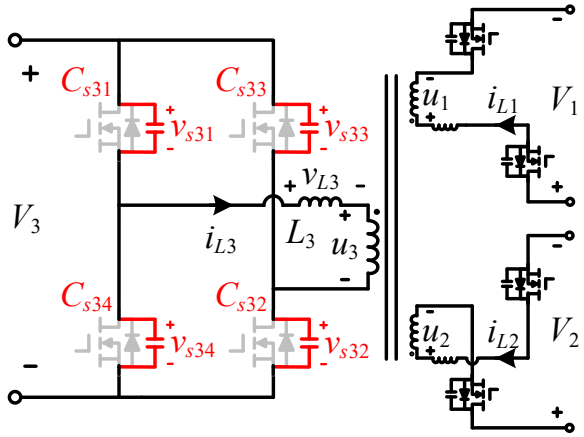



Figure 3.13 Resonance process during $t_1$~$t_2$.

$$u_3(t)=\frac{N_3}{3}\left(V_1-\frac{V_2}{N_2}+\frac{-v_{s31}(t)+V_3-v_{s32}(t)}{N_3}\right) \tag{3.29}$$

$$v_{s31}(t)=A_{13}\cos\left(\omega_3\left(t-t_1\right)\right)+A_{23}\sin\left(\omega_3\left(t-t_1\right)\right)+A_{33} \tag{3.30}$$

where $A_{13}=\dfrac{V_3/3+\mathrm{N}_3V_1/3}{C_sL_3\omega_3^2}$, $A_{23}=\dfrac{i_{L3}(t_1)}{\omega_3C_s}$, $A_{33}=V_3-A_{13}$, and $\omega_3=\sqrt{4/(3C_sL_3)}$.

Similarly, the inductor currents $i_{L2}(t_3)$ and $i_{L1}(t_5)$ are also given in (3.28), and they are negative and positive, respectively. The corresponding resonances occur in modules $M_2$ and $M_1$ during $t_3$~$t_4$ and $t_5$~$t_6$, respectively. During resonances, the parasitic capacitors $C_{s21}$ and $C_{s13}$ are discharged, and the corresponding drain-to-source voltages $v_{s21}(t)$ and $v_{s13}(t)$ are calculated in (3.31).

$$\begin{cases} v_{s21}(t)=A_{12}\cos\left(\omega_2\left(t-t_3\right)\right)+A_{22}\sin\left(\omega_2\left(t-t_3\right)\right)+A_{32} \\ v_{s13}(t)=A_{11}\cos\left(\omega_1\left(t-t_5\right)\right)+A_{21}\sin\left(\omega_1\left(t-t_5\right)\right)+A_{31} \end{cases} \tag{3.31}$$

where $A_{12}=\dfrac{V_2/3+\mathrm{N}_2V_1}{C_sL_2\omega_2^2}$, $A_{22}=\dfrac{i_{L2}(t_3)}{\omega_2C_s}$, $A_{32}=V_2-A_{12}$, $A_{11}=0$, $A_{21}=\dfrac{-i_{L1}(t_5)}{\omega_1C_s}$, $A_{31}=V_1$,

$\omega_2=\sqrt{\dfrac{4}{3C_sL_2}}$ and $\omega_1=\sqrt{\dfrac{4}{3C_sL_1}}$.

According to (3.30), (3.31) and the system parameters in Table 3.2, the drain-to-source voltages $v_{s13}(t)$, $v_{s21}(t)$ and $v_{s31}(t)$ are shown in Figure 3.14. From Figure 3.14, both $v_{s13}(t)$ and $v_{s21}(t)$ can drop to zero quickly. After they drop to zero, their body diodes will conduct; therefore, the ZVS turn-ON of switches $S_{13}$ and $S_{21}$ is realized if their drive signals turn positive. Nevertheless, $vs_{31}$(t) decreases slowly and requires a large amount of time to reach zero, which is much larger than the practical dead time. To improve this, an inductor $L_4$ is added to connect with the drain terminals of switches $S_{32}$ and $S_{34}$. Accordingly, the resonance expression of $v_{s31}(t)$ is changed from (3.30) to (3.32), where $i_{L4}(t_1) < 0$. Because $B_1 > A_{13}$, while $B_2 < A_{23}$, $v_{s31}(t)$ drops faster after adding the parallel inductor $L_4$, which is also shown in Figure 3.14. The ZVS turn-ON of switch $S_{31}$ can also be obtained. With the decrease in $L_4$, the resonance time will be reduced, but the extra conduction losses will increase. Therefore, the inductance $L_4$ is finally designed as 300 $\mu$H after establishing a tradeoff between the ZVS realization and conduction loss.

$$v_{s31}(t) = B_1 \cos\left(\omega_3 \left(t - t_1\right)\right) + B_2 \sin\left(\omega_3 \left(t - t_1\right)\right) + B_3 \tag{3.32}$$

where $B_1 = \left(N_3 V_1/3 + \left(1/3 + L_3/L_4\right)V_3\right) \Big/ \left(L_3 C_3 \omega_3^2\right)$, $B_2 = \left(i_{L3}\left(t_1\right) + i_{L4}\left(t_1\right)\right) \Big/ \left(\omega_3 C_s\right)$, $B_3 = V_3 - B_1$, $i_{L4}\left(t_1\right) = -V_3 T_s \Big/ \left(4L_4\right)$.

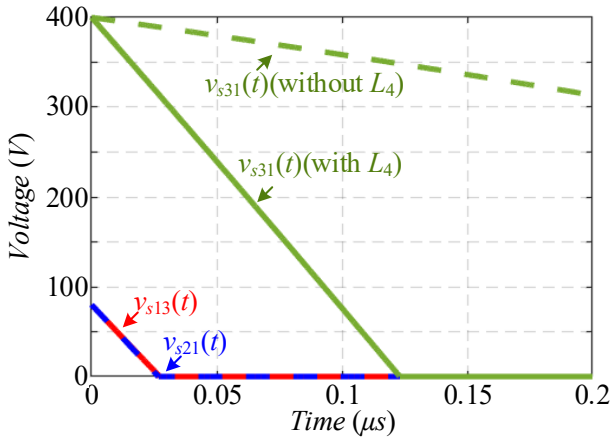



Figure 3.14 Resonance waveforms of drain-to-source voltages $v_{s13}$, $v_{s21}$, and $v_{s31}$.

The deadtime is set to 0.167 $\mu$s, and the ZVS operation fails if $v_{s13}(t)$, $v_{s21}(t)$, and $v_{s31}(t)$ cannot drop to zero before the deadtime end. Based on (3.31), (3.32) and the system parameters in Table 3.2, the ZVS ranges within load conditions $I_{o1}$ = 0~2.5 A and $I_{o2}$ = 0~2.5 A are presented

in Figure 3.15, where the per-unit current is set as 2.5 A. From Figure 3.15, switches in modules $M_1$ and $M_2$ will lose the ZVS operation under light loads. Switches in $M_3$ can always realize ZVS operation throughout the load ranges.

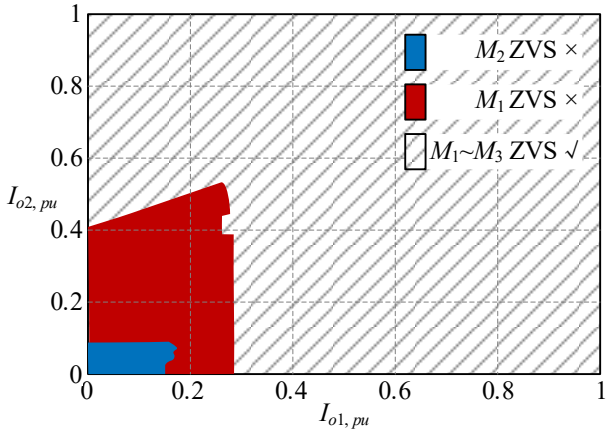



Figure 3.15 ZVS ranges of switches in isolated modules $M_1$~$M_3$.

### 3.3.4 Small Signal Modeling and Control Design

In addition to steady-state analysis, the dynamic characteristic of the proposed example TAB-based PPP-SIDO dc–dc converter is also explained by small signal modeling in this section. Subsequently, the control scheme is designed. According to the operational principle, the average state space equation of the proposed PPP-SIDO converter is given in (3.33). The average values $\langle i_1(t)\rangle_{T_s}$ and $\langle i_2(t)\rangle_{T_s}$ represented by other variables without substantial ripples, as shown in (3.34). These are derived from (3.21) and (3.22) by dividing power flows by voltages. Subsequently, average values equal to the corresponding quiescent values plus small ac variations are assumed, which are $\langle v_{o1}(t)\rangle_{T_s} = V_{o1} + \hat{v}_{o1}(t)$, $\langle v_{o2}(t)\rangle_{T_s} = V_{o2} + \hat{v}_{o2}(t)$, $\langle \phi_{12}(t)\rangle_{T_s} = \Phi_{12} + \hat{\phi}_{12}(t)$ and $\langle \phi_{13}(t)\rangle_{T_s} = \Phi_{13} + \hat{\phi}_{13}(t)$. Replacing these and (3.34) into (3.33), and neglecting both dc terms and higher order nonlinear terms, we can obtain the small-signal model linearized equation in (3.35). In addition, after converting the expression from the time domain to the s domain, we output expressions related to the phase shift angles in (3.36) and the corresponding transfer functions in (3.37).

$$\begin{cases} C_{o1}\dfrac{d\langle v_{o1}(t)\rangle_{T_s}}{dt} = \langle i_1(t)\rangle_{T_s} - \dfrac{\langle v_{o1}(t)\rangle_{T_s}}{R_1} \\ C_{o2}\dfrac{d\langle v_{o2}(t)\rangle_{T_s}}{dt} = -\langle i_2(t)\rangle_{T_s} - \dfrac{\langle v_{o2}(t)\rangle_{T_s}}{R_2} \end{cases} \tag{3.33}$$

$$\begin{cases} \langle i_1(t)\rangle_{T_s} = f_1\left(v_{o2}, v_{i1}, \phi_{12}, \phi_{13}\right) \\ = \dfrac{\langle v_{o2}(t) - v_{i1}(t)\rangle_{T_s}}{N_2\omega_s L_{12}} \cdot \dfrac{\phi_{12}(t)\pi}{180^\circ} \cdot \left(1 - \dfrac{\phi_{12}(t)}{180^\circ}\right) \\ + \dfrac{\langle v_{i1}(t)\rangle_{T_s}}{N_3\omega_s L_{13}} \cdot \dfrac{\phi_{13}(t)\pi}{180^\circ} \cdot \left(1 - \dfrac{\phi_{13}(t)}{180^\circ}\right) \\ \langle i_2(t)\rangle_{T_s} = f_2\left(v_{o1}, v_{i1}, \phi_{12}, \phi_{13}\right) \\ = -\dfrac{\langle v_{i1}(t) - v_{o1}(t)\rangle_{T_s}}{N_2\omega_s L_{12}} \cdot \dfrac{\phi_{12}(t)\pi}{180^\circ} \cdot \left(1 - \dfrac{\phi_{12}(t)}{180^\circ}\right) \\ + \dfrac{\langle v_{i1}(t)\rangle_{T_s}\pi}{N_2 N_3\omega_s L_{23}} \cdot \left|\dfrac{\phi_{13}(t)}{180^\circ} - \dfrac{\phi_{12}(t)}{180^\circ}\right| \cdot \left(1 - \left|\dfrac{\phi_{13}(t)}{180^\circ} - \dfrac{\phi_{12}(t)}{180^\circ}\right|\right) \end{cases} \tag{3.34}$$

$$\begin{cases} C_{o1}\dfrac{d\hat{v}_{o1}(t)}{dt} + \dfrac{\hat{v}_{o1}(t)}{R_1} = k_1\hat{v}_{o2}(t) + k_2\hat{\phi}_{12}(t) + k_3\hat{\phi}_{13}(t) \\ C_{o2}\dfrac{d\hat{v}_{o2}(t)}{dt} + \dfrac{\hat{v}_{o2}(t)}{R_2} = -m_1\hat{v}_{o1}(t) - m_2\hat{\phi}_{12}(t) - m_3\hat{\phi}_{13}(t) \end{cases} \tag{3.35}$$

where $\begin{cases} k_1 = \dfrac{df_1}{dv_{o2}}\Big|_{v_{o2}=V_{o2}} = \dfrac{\pi}{N_2\omega_s L_{12}} \cdot \left(\dfrac{\Phi_{12}}{180^\circ} - \dfrac{\Phi_{12}^2}{180^{\circ 2}}\right) = m_1 \\ k_2 = \dfrac{df_1}{d\phi_{12}}\Big|_{\phi_{12}=\Phi_{12}} = \dfrac{(V_{o2} - V_{i1})\pi}{N_2\omega_s L_{12}} \cdot \left(\dfrac{1}{180^\circ} - \dfrac{2\Phi_{12}}{180^{\circ 2}}\right) \\ k_3 = \dfrac{df_1}{d\phi_{13}}\Big|_{\phi_{13}=\Phi_{13}} = \dfrac{V_{i1}\pi}{N_3\omega_s L_{13}} \cdot \left(\dfrac{1}{180^\circ} - \dfrac{2\Phi_{13}}{180^{\circ 2}}\right) \\ m_2 = \dfrac{df_2}{d\phi_{12}}\Big|_{\phi_{12}=\Phi_{12}} = \dfrac{(V_{o1} - V_{i1})\pi}{N_2\omega_s L_{12}} \cdot \left(\dfrac{1}{180^\circ} - \dfrac{2\Phi_{12}}{180^{\circ 2}}\right) + m_3 \\ m_3 = \dfrac{df_2}{d\phi_{13}}\Big|_{\phi_{13}=\Phi_{13}} = \dfrac{V_{i1}\pi}{N_2 N_3\omega_s L_{23}} \cdot \left(\dfrac{1}{180^\circ} - \dfrac{2(\Phi_{13} - \Phi_{12})}{180^{\circ 2}}\right) \end{cases}$.

$$\begin{cases} \hat{v}_{o1}(s) = G_{vd12}\hat{\phi}_{12}(s) + G_{vd13}\hat{\phi}_{13}(s) \\ \hat{v}_{o2}(s) = G_{vd22}\hat{\phi}_{12}(s) + G_{vd23}\hat{\phi}_{13}(s) \end{cases} \tag{3.36}$$

$$\begin{cases} G_{vd12} = \hat{v}_{o1}(s)/\hat{\phi}_{12}(s) = \dfrac{A_1B_2 + A_2B_0}{A_0B_0 - A_1B_1} \\ G_{vd13} = \hat{v}_{o1}(s)/\hat{\phi}_{13}(s) = \dfrac{A_1B_3 + A_3B_0}{A_0B_0 - A_1B_1} \\ G_{vd22} = \hat{v}_{o2}(s)/\hat{\phi}_{12}(s) = \dfrac{A_2B_1 + A_0B_2}{A_0B_0 - A_1B_1} \\ G_{vd23} = \hat{v}_{o2}(s)/\hat{\phi}_{13}(s) = \dfrac{A_3B_1 + A_0B_3}{A_0B_0 - A_1B_1} \end{cases} \tag{3.37}$$

where $A_0 = sC_{o1}+1/R_1$, $A_i = k_i (i = 1,2,3)$, $B_0 = sC_{o1}+1/R_1$, $B_i = -m_i (i = 1,2,3)$.

The bode plots of the control-to-output transfer functions are shown in Figure 3.16 based on (3.37) and the system parameters in Table 3.2. Note that the phase of $G_{vd23}$ is larger than 0° from Figure 3.16; therefore, the voltage error of the control system for output $V_{o2}$ is designed as $v_{o2}-V_{ref2}$ rather than $V_{ref2}-v_{o2}$ to realize negative feedback closed-loop control. Accordingly, the control block diagram is designed as shown in Figure 3.17. As shown in the figure, the two output voltages $v_{o1}$ and $v_{o2}$ are sampled independently, and two reference voltages $V_{ref1}$ and $V_{ref2}$ are compared to obtain the voltage errors. Subsequently, two separate PI controllers are employed to achieve constant voltage control by adjusting the phase shift angles $\phi12$ and $\phi13$. Finally, the phase shift PWM module generates three pairs of complementary square waves with the required phase shifts, providing driving signals for three active bridges.

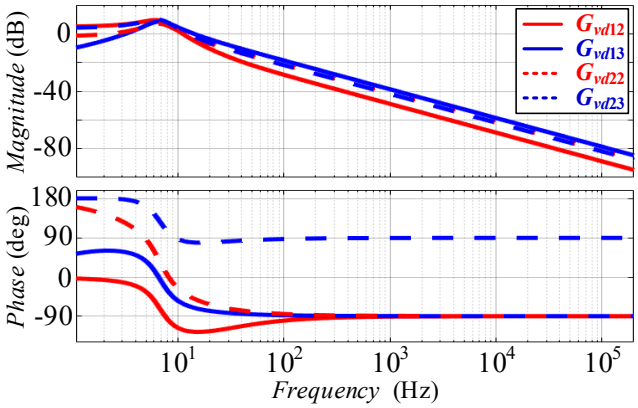



Figure 3.16 Bode plots of the control-to-output transfer functions $G_{vd12}$, $G_{vd13}$, $G_{vd22}$, and $G_{vd23}$ obtained by the theoretical analysis.

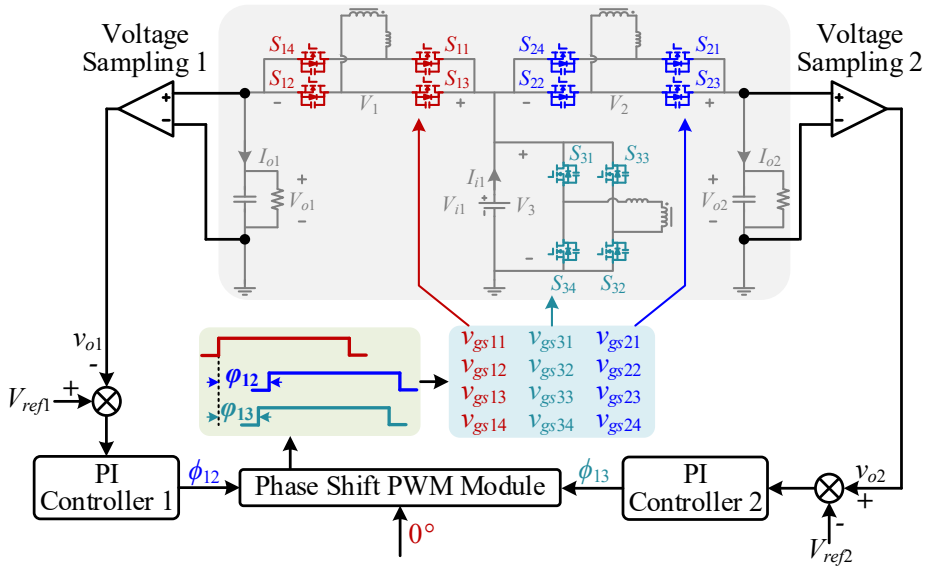



Figure 3.17 The control block diagram of the proposed TAB-based PPP-SIDO dc–dc converter.

Based on the control-to-output transfer functions shown in Figure 3.16 and the control block diagram presented in Figure 3.17, the closed-loop control system is further developed as illustrated in Figure 3.18. The PI controllers shown in Figure 3.17 correspond to the compensators $G_{c1}$ and $G_{c2}$ in Figure 3.18, which are designed as equation (3.38). The bode plots of the open-loop transfer functions $G_{op1} = G_{vd12} \times G_{c1}$ and $-G_{op2} = -G_{vd23} \times G_{c2}$ are shown in Figure 3.19. From Figure 3.19, it can be observed that both the magnitude values of $G_{op1}$ and $G_{op2}$ at 0 Hz are large due to their −20 dB/dec slopes. This ensures zero steady-state error and eliminates the deviation between the actual and reference output voltages. Moreover, the phase margins of $G_{op1}$ and $G_{op2}$ are approximately 90°, ensuring the stability of the closed-loop system. In addition, their crossover frequencies are approximately 300 Hz, which contributes to quick responses. In other words, the closed-loop system obtains both good steady-state accuracy and dynamic performance after adding the compensators. It should be noted that the voltage-loop-only control strategy presented in this section is specifically designed for preliminary validation of the proposed TAB-based PPP-SIDO dc–dc converter. While this simplified control approach serves its purpose for basic verification, it exhibits inherent limitations: the absence of current feedback restricts the system's ability to monitor instantaneous power flow, consequently reducing both phases and gain margins. Therefore, for practical applications demanding rapid load changes, precise bidirectional power management, or fault handling capabilities, the implementation of an additional current control loop becomes essential.

$$\begin{cases} G_{c1} = \dfrac{120s + 16000}{s} \\ G_{c2} = \dfrac{60s + 6000}{s} \end{cases} \tag{3.38}$$

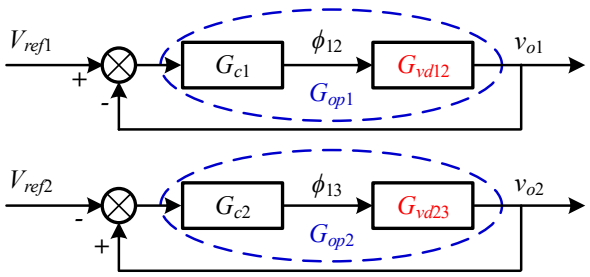
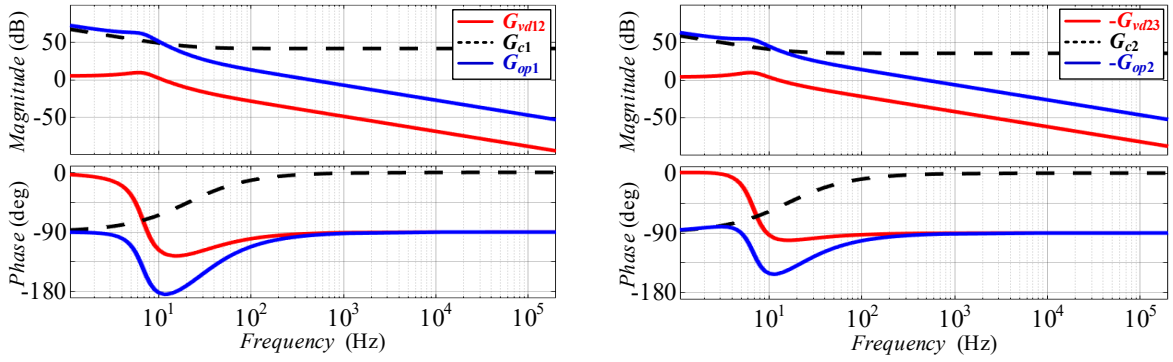



Figure 3.18 Closed-loop control system with separate compensators.




(a) (b)

Figure 3.19 Bode plots. (a) $G_{vd12}$, $G_{c1}$, $G_{op1}$ and (b) $-G_{vd23}$, $G_{c2}$, $-G_{op2}$.

# 3.4 Experimental Verification

## 3.4.1 Prototype

Based on the circuit of the proposed TAB-based PPP-SIDO dc–dc converter in Figure 3.3, the system parameters Table 3.2 and design considerations in Section 3.3.3, a prototype circuit is established, as shown in Figure 3.20.

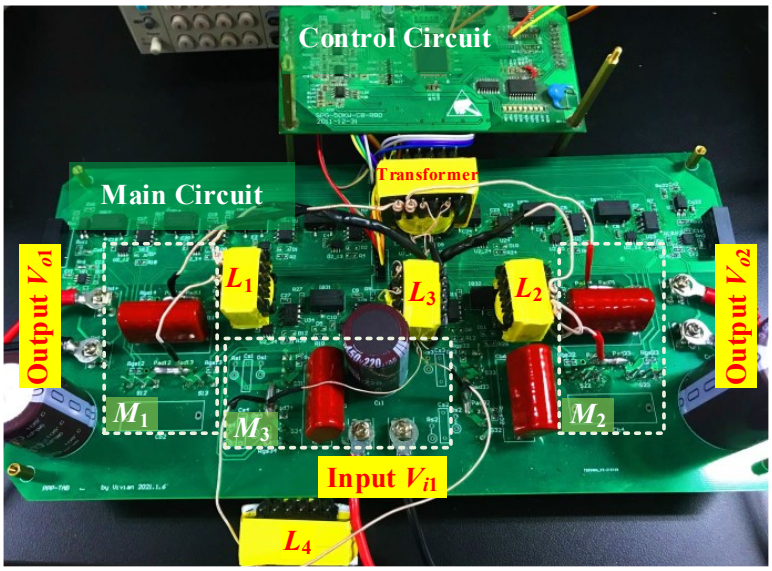



Figure 3.20 Photograph of the prototype circuit.

In Figure 3.20, the main circuit is self-designed, and the control circuit uses the purchased DSP controller based on TMS320F28335. The corresponding PCB layout of the main circuit is shown in Figure 3.21. From Figure 3.21, there are three active bridges with twelve MOSFETs,

and every MOSFET is equipped with an independent and isolated drive circuit. Two sample circuits are respectively connected to two outputs for constant voltage control.

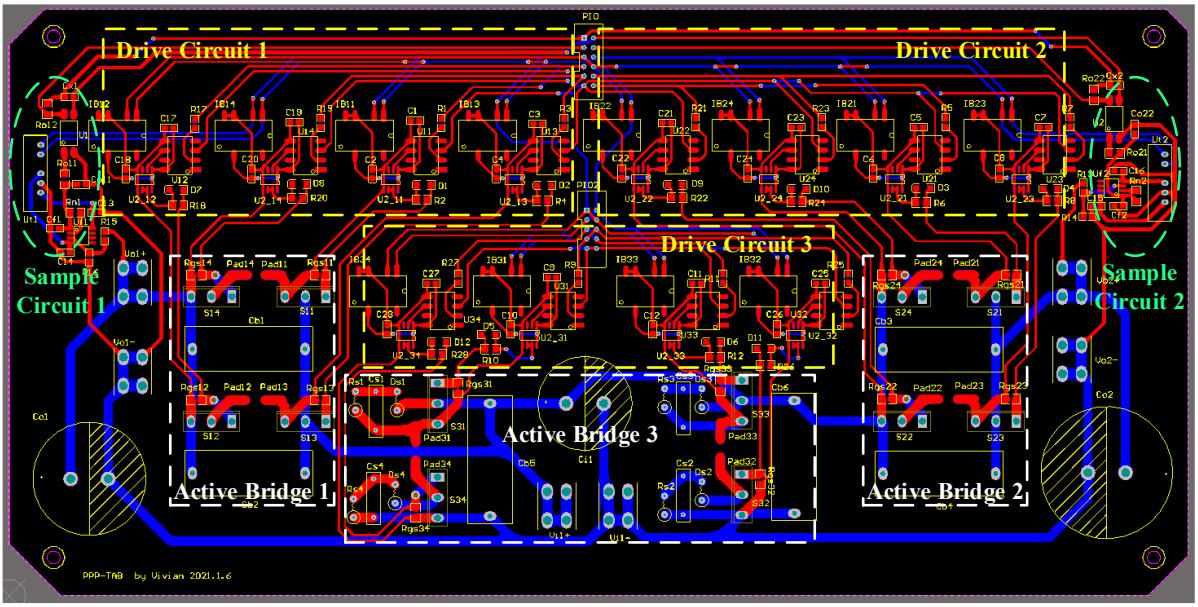



Figure 3.21 PCB layout of the prototype main circuit.

The detailed implementation of the active bridge module is illustrated in Figure 3.22, which demonstrates the correspondence between the functional prototype, its PCB layout, and the theoretical circuit schematic. From Figure 3.22, the MOSFETs are mounted on the reverse side of the PCB to optimize thermal management and space utilization. Furthermore, a $10\mu F$ CBB capacitor $C_{b1}$ is placed between the two bridge arms to suppress high-frequency noise and mitigate voltage spikes during switching transitions, ensuring stable operation. The inductor $L_1$ and one winding of the transformer are interfaced through external PCB pads.

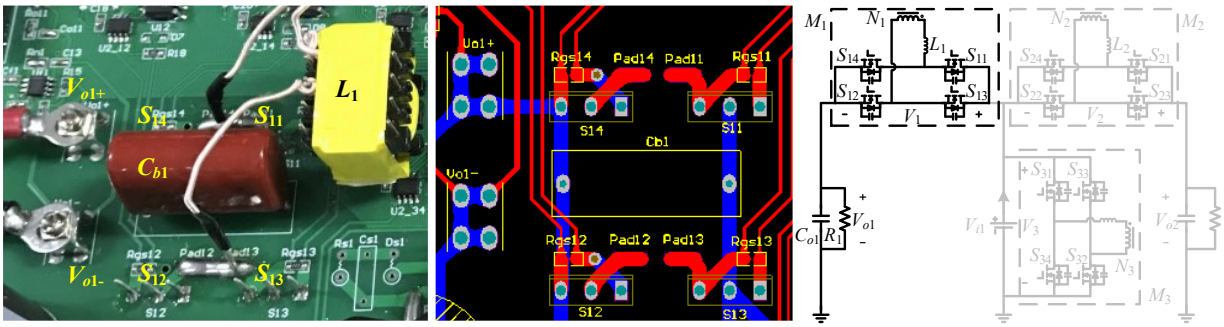



Figure 3.22 One active bridge module: prototype implementation, PCB design, and theoretical circuit.

The remaining two active bridge modules are implemented similarly as the design shown in Figure 3.22. These three modules are interconnected according to the PPP configuration,

realizing power transmission between the single input $V_{i1}$ and two outputs $V_{o1}$ and $V_{o2}$. For experimental validation, a dc power supply is utilized to provide $V_{i1}$, while two electronic dc loads, configured in constant resistance mode, are employed to emulate the output loads at $V_{o1}$ and $V_{o2}$. Every dc port is equipped with an electrolytic capacitor to filter out the noise and provide a smoother dc voltage. The detailed schematic of the drive circuits and voltage sampling circuits are provided in Appendix A for reference. Additionally, a comprehensive list of key components used in the implementation is summarized Table 3.3.

Table 3.3
KEY COMPONENTS LIST

| Components | Details |
|---|---|
| Switches $S_{i1}$~$S_{i4}$($i$ = 1, 2, 3) | MOSFET IPW60R180P7, 600 V, 18 A, 0.18 ohm, N-Channel |
| Output capacitors $C_{o1,2}$ | Electrolytic Capacitor, 220 $\mu$F, 500 V |
| Transformer core | Ferrite core EE 42/21/20 |
| Transformer winding ($N_1$:$N_2$:$N_3$) | Litz wire with turns of 9:9:45 |
| Inductors $L_1$/$L_2$/$L_3$/$L_4$ | 20/20/500/300 $\mu$H |
| Drive circuit | Gate drive optocoupler HCPL-3120 + MOSFET driver MIC4420 |
| Sample circuit | Operational amplifiers TL082 + Optocoupler HCPL-817-50BE |

## 3.4.2 Experimental Results

The experimental waveforms of port voltages $V_{i1}$, $V_{o1}$, $V_{o2}$, and module voltages $V_1$~$V_3$ of $M_1$~$M_3$ are shown in Figure 3.23. From Figure 3.23, the output voltages $V_{o1}$ and $V_{o2}$ are regulated to 320 and 480 V, respectively. The module voltage $V_3$ of $M_3$ is equal to the input voltage $V_{i1}$ = 400 V. The module voltages $V_{1,2}$ of $M_{1,2}$ are 80 V, which is the difference between the input and output voltages. Therefore, the voltage stresses of modules $M_{1,2}$ are effectively reduced.

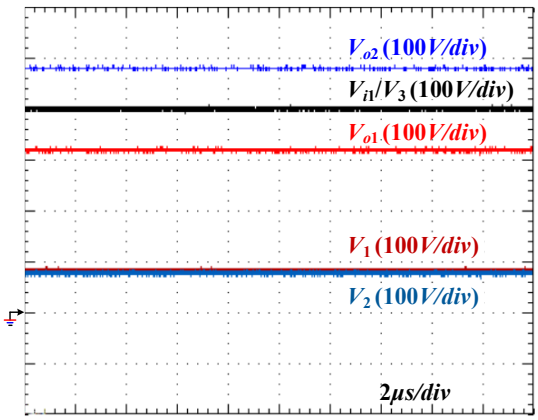



Figure 3.23 Experimental waveforms of port voltages $V_{i1}$, $V_{o1}$, $V_{o2}$, and module voltages $V_1$~$V_3$.

In addition, Figure 3.24~Figure 3.26 demonstrate key experimental waveforms and ZVS realization under three conditions of ($I_{o1}$, $I_{o2}$), which are (2.5 A, 2.5 A), (2.5 A, 0.5 A), and (0.5 A, 2.5 A), respectively. According to Figure 3.24(a)~Figure 3.26 (a), the phase shifts $\phi_{12}$ and $\phi_{13}$ are (63.9°, 31.95°), (37°, 54.7°), and (37°, −17.6°), respectively, which coincide well with the theoretical results in Figure 3.9. Moreover, with the measured values of $I_{i1}$, $I_{o1}$, and $I_{o2}$, the average current $I_3$ of module $M_3$, which is equal to $I_{i1}-I_{o1}-I_{o2}$, is 0, −0.4, and 0.4 A under three load conditions. Therefore, the current stress of module $M_3$ is also reduced in the proposed converter when compared with the conventional TAB converter.

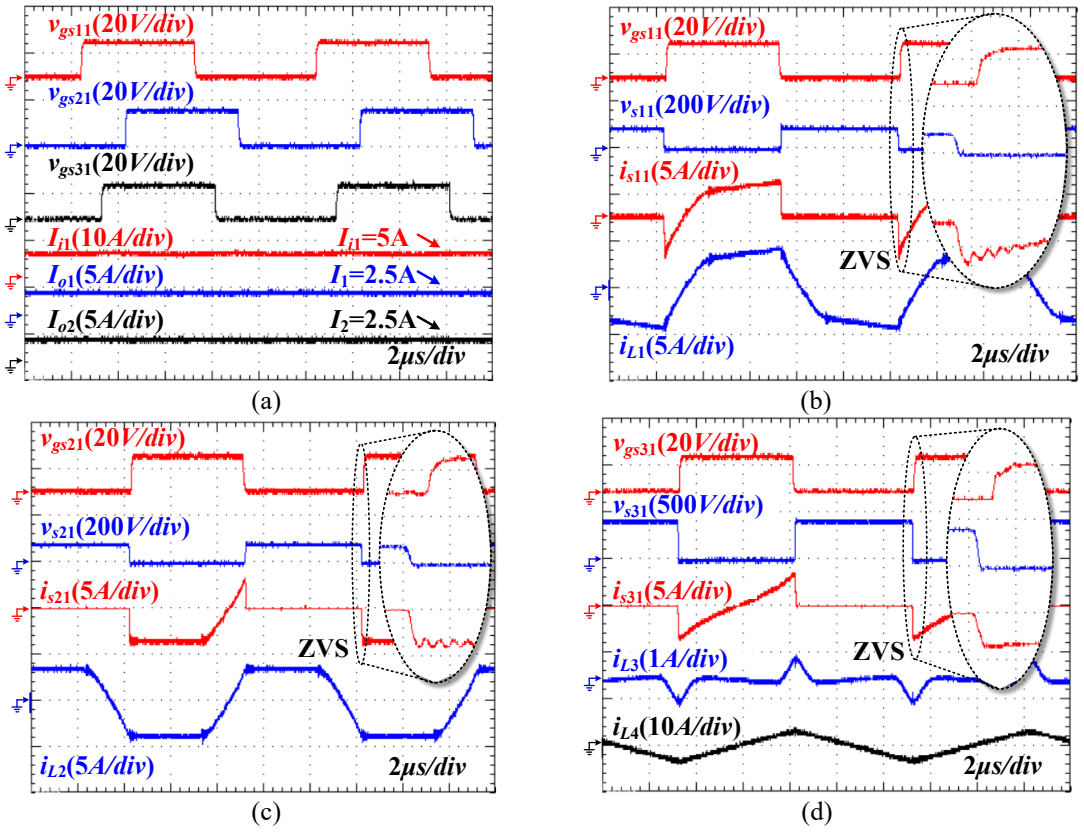



Figure 3.24 Key experimental waveforms under load conditions $I_{o1}$ = 2.5 A, $I_{o2}$ = 2.5 A. (a) Drive signals $v_{gs11}$~$v_{gs31}$, and port currents $I_{i1}$, $I_{o1}$, and $I_{o2}$. (b) Drive signal $v_{gs11}$, drain-to-source voltage $v_{s11}$, drain-to-source current $i_{s11}$, and inductor current $i_{L1}$. (c) Drive signal $v_{gs21}$, drain-to-source voltage $v_{s21}$, drain-to-source current $i_{s21}$, and inductor current $i_{L2}$. (d) Drive signal $v_{gs31}$, drain-to-source voltage $v_{s31}$, drain-to-source current $i_{s31}$, and inductor currents $i_{L3}$ and $i_{L4}$.

Moreover, from Figure 3.24(b), the inductor current $i_{L1}$ is negative before switch $S_{11}$ is turned ON. Hence, the parasitic capacitor of switch $S_{11}$ will be discharged, and its drain-to-source voltage $v_{s11}$ will be decreased after $S_{13}$ is turned OFF. Once $v_{s11}$ drops to zero, the inductor current $i_{L1}$ will flow through the source terminal to the drain terminal of switch $S_{11}$, effectively clamping

the drain-to-source voltage $v_{s11}$ to zero before the drive signal $v_{gs11}$ activates. This sequence ensures that the ZVS operation of $S_{11}$ is achieved, provided that $v_{s11}$ reaches zero before $v_{gs11}$ rises. Similarly, from Figure 3.24(c), (d), Figure 3.25(b)~(d), and Figure 3.26(b)~(d), all the switches can successfully achieve ZVS operation under these three load conditions. Comparing Figure 3.24~Figure 3.26, the maximum absolute value of the inductor currents $i_{L1}$ is increased with the rising load currents $I_{o1}$; therefore, the ZVS operation of switches in module $M_1$ is correspondingly easier. Module $M_2$ obtains a similar trend when $I_{o2}$ increases. On the other hand, the ZVS operation of switches in module $M_3$ is almost unaffected by load conditions because it is mainly influenced by the additional inductor current $i_{L4}$ rather than $i_{L3}$.

In addition, the dynamic response under the output resistance variation is presented in Figure 3.27. The dynamic response waveform is captured using an oscilloscope by setting two different resistance values on the electronic load for before and after the load switching, then initiating the switch. As seen in Figure 3.27, when the output resistance changes, the output voltage initially fluctuates but quickly returns to its rated value.

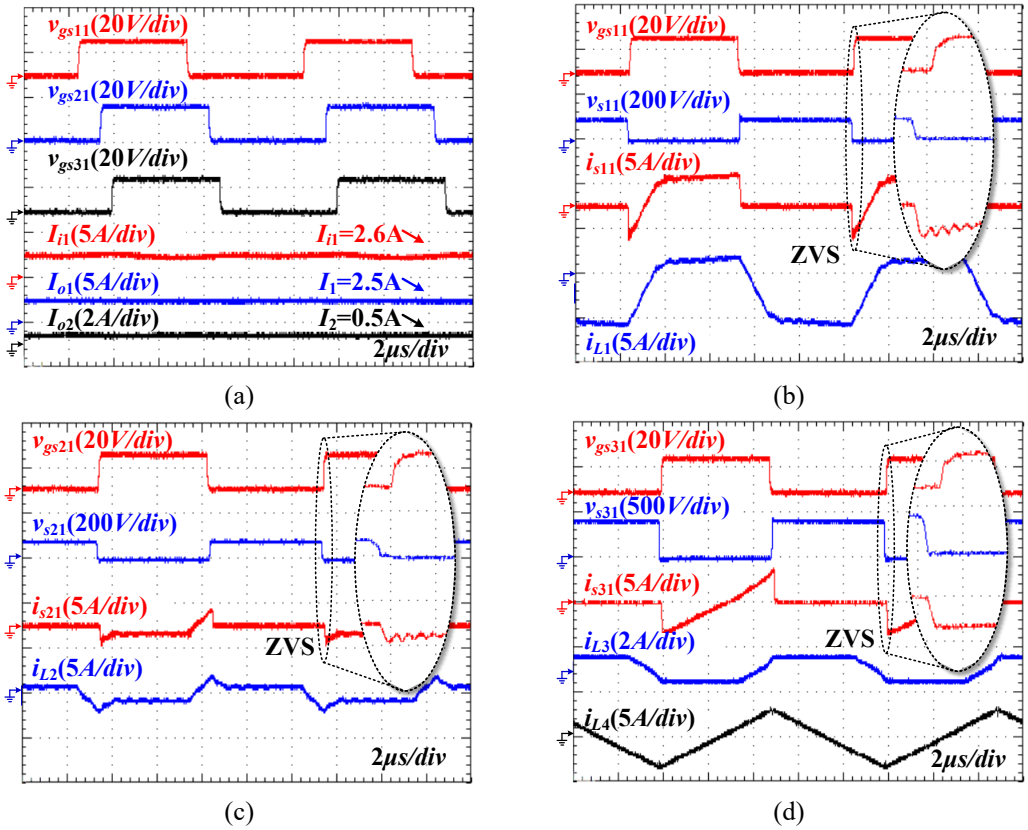



Figure 3.25 Key experimental waveforms under load conditions $I_{o1}$ = 2.5 A, $I_{o2}$ = 0.5 A.

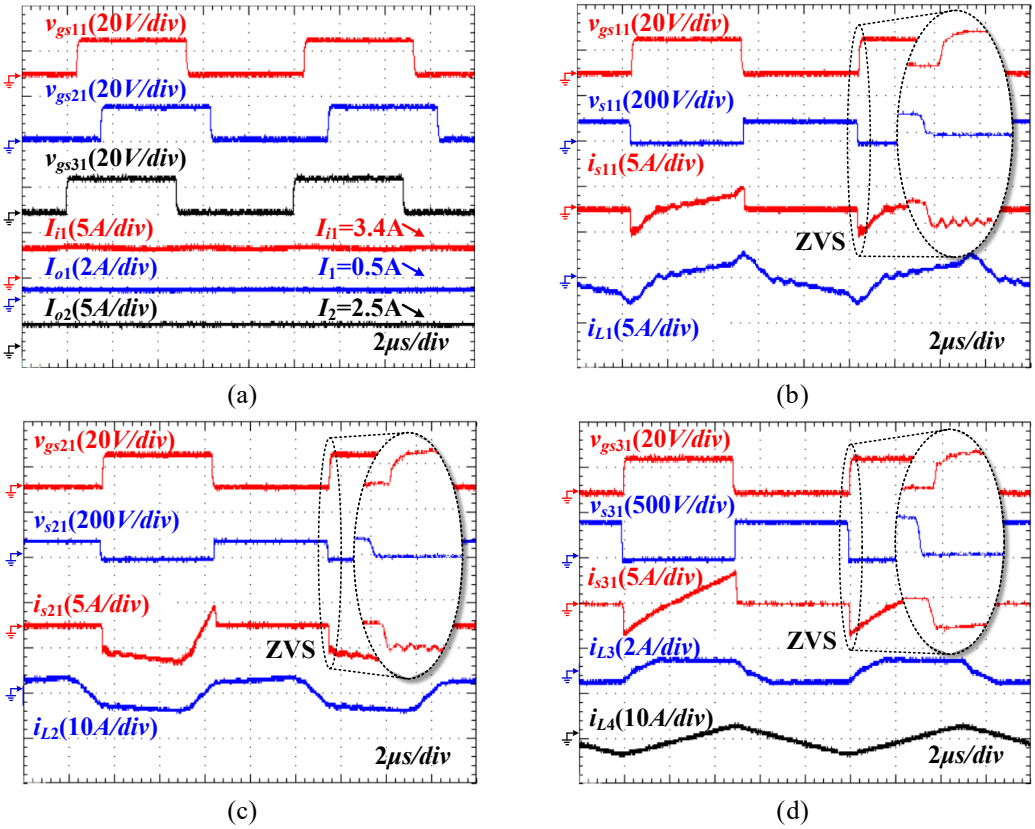



Figure 3.26 Key experimental waveforms under load conditions $I_{o1}$ = 0.5 A, $I_{o2}$ = 2.5 A.

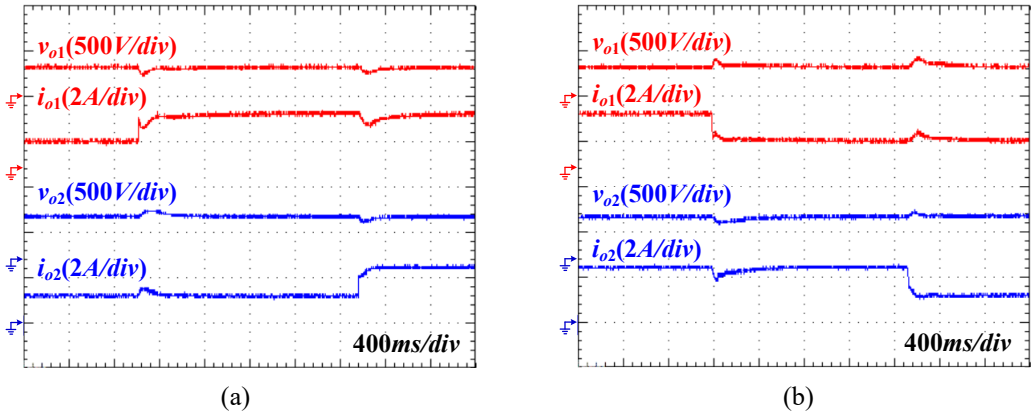



Figure 3.27 Dynamic response when output resistance $R_1$ is changed between 256 and 128Ω, and $R_2$ is changed between 384 and 192Ω, respectively. (a) Output resistances decrease. (b) Output resistances increase.

According to the measured module voltages $V_1$~$V_3$ and calculated average module current $I_1$~$I_3$, the corresponding powers ($P_1$, $P_2$, $P_3$) being processed by three modules $M_1$~$M_3$ are equal to (200 W, −200 W, 0 W), (200 W, −40 W, −160 W), and (40 W, −200 W, 160 W), respectively, under three load conditions (2.5 A, 2.5 A), (2.5 A, 0.5 A), and (0.5 A, 2.5 A). They only account for 10%, 19.23%, and 14.7% of the practical power of the input and output ports, and the remaining power is transferred from input to output directly. Therefore, their corresponding

efficiencies are high at 98.87%, 98.40%, and 98.86%, respectively. In the prototype circuit, the power loss is mainly caused by conduction losses of both semiconductors and magnetic components, while switching loss and magnetic core loss can almost be ignored entirely due to the realization of ZVS and small magnetizing current. To justify the efficiencies, the detailed loss analysis of three load conditions ($I_{o1}$, $I_{o2}$) = (2.5 A, 2.5 A)/(2.5 A, 0.5 A)/(0.5 A, 2.5 A) is conducted as follows.

According to Figure 3.7, expression of switch currents $I_{si1,\mathrm{rms}}(i = 1, 2, 3)$ in (3.26), and the system parameters in Table 3.2, we can obtain RMS current values of switches $I_{si1,\mathrm{rms}}(i = 1, 2, 3)$ under three load conditions in (3.39). The RMS values of the series and parallel connected inductor currents $I_{Li,\mathrm{rms}}$ ($i$ = 1, 2, 3) and $I_{L4,\mathrm{rms}}$ can also be obtained in (3.40) and (3.41), respectively.

$$\begin{cases} I_{s11,rms} = 2.21A/\,2.17A/\,0.62A \\ I_{s21,rms} = 2.21A/\,0.62A/\,2.17A \\ I_{s31,rms} = 0.12A/\,0.34A/\,0.34A \end{cases} \tag{3.39}$$

$$I_{Li,rms} = \sqrt{2}\cdot I_{si1,rms} \tag{3.40}$$

$$I_{L4,rms} = \frac{1}{\sqrt{3}}\cdot\frac{V_3 T_s}{4L_4} = 1.92A \tag{3.41}$$

Based on the datasheet of MOSFET IPW60R180P7, the drain-to-source ON-state resistance is $R_{ds}$ = 0.18Ω. Therefore, the conduction losses of switches under three load conditions are calculated in (3.42). In addition, because the three windings of the transformer are in series with inductors $L_1$~$L_3$, their sums of resistances are $R_{m1}$ = 0.33Ω, $R_{m2}$ = 0.31Ω, and $R_{m3}$ = 6.98Ω, respectively. The resistance of the parallel connected inductor $L_4$ is $R_{L4}$ = 0.74Ω. The conduction losses of the magnetic components under three load conditions are obtained in (3.43). According to (3.42) and (3.43), the sum of the conduction losses is $P_{c,loss}$ = 17.81 W/13.42 W/13.25 W. We can thus obtain estimated efficiencies of 99.11%/98.71%/99.03%. Compared with the measured efficiencies of 98.87%/98.40%/98.86%, the estimated efficiencies are basically consistent with the measured efficiencies. Their small differences are caused by other losses and measurement errors.

$$P_{s,loss} = 4 \cdot R_{ds} \cdot \left[ I_{s1,rms}^2 + I_{s2,rms}^2 + \left( I_{s3,rms} + \frac{1}{\sqrt{2}} I_{L4,rms} \right)^2 \right] = 8.62W / 5.74W / 5.74W \quad (3.42)$$

$$P_{L,loss} = \sum_{i=1}^{3} R_{mi} I_{Li,rms}^2 + R_{L4} I_{L4,rms}^2 = 9.19W / 7.68W / 7.51W \quad (3.43)$$

In addition, the efficiencies across the full-load range were measured and are presented in Figure 3.28. The efficiencies were calculated based on the measured input and output voltage and current values. These measurements were obtained using two methods: readings from the power supply and electronic load indicators, and direct measurements from an oscilloscope equipped with voltage and current probes. The final efficiency values presented are the average of these two methods. Although minor discrepancies exist due to inherent errors in the measuring instruments, Figure 3.28 primarily serves to illustrate the efficiency trends across the entire load range, demonstrating the consistently high efficiency of the system.

From Figure 3.28, it can be observed that the implementation of PPP results in relatively low partial power ratio across the entire load range. This, in turn, leads to reduced power losses. The primary sources of losses in the system include conduction losses in the switches and inductors, while the switching losses during transitions are almost negligible due to realization of soft switching. Owing to the small partial power ratios enabled by PPP, these losses are minimized. As a result, the measured efficiencies remain high throughout the load range, with the minimum efficiency reaching 98.13%.

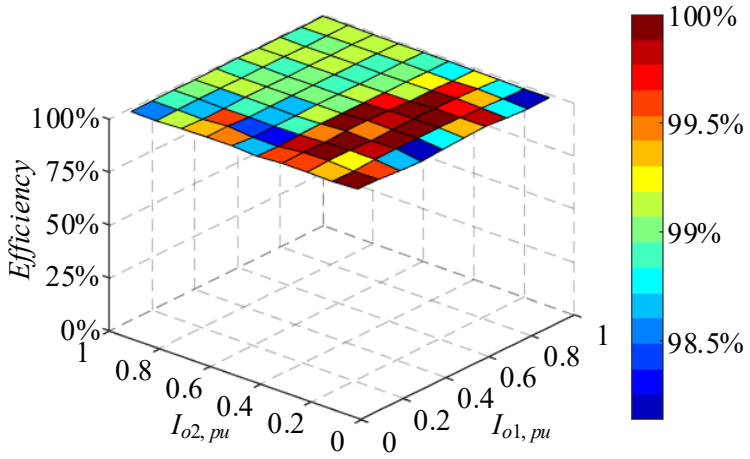



Figure 3.28 Measured efficiencies of the proposed example TAB-based PPP-SIDO dc–dc converter over the whole load range.

## 3.5 Conclusions

In this chapter, the novel PPP multiport dc–dc architecture with radial module connections is presented, specifically designed for SIMO and MISO applications. This architecture is an advancement derived from the general PPP multiport dc–dc architectures in Chapter 2, effectively extending the capabilities of the PPP from traditional two-port structures to accommodate multiple ports.

In the proposed architecture, each series-connected module is responsible for processing only the partial power generated by the voltage difference between the single input and each individual output. Furthermore, a single parallel module, connected to the input, handles the partial power caused by the current differences across all the dc ports. The remaining portion of the total power is transmitted directly, without requiring additional processing. Therefore, this design significantly decreased voltage, current and power ratings of the converter, improving both efficiency and power density.

To provide a more comprehensive understanding of the proposed architecture, this chapter also explores replacing the modules with a specific isolated converter. As a case study, the example PPP-SIDO dc–dc converter using three active bridge modules $M_1$~$M_3$ is analyzed in detail. Owing to the realization of PPP, the voltage stresses are effectively reduced within modules $M_1$~$M_2$, while the current stress is reduced in $M_3$. These stress reductions allow for the use of lower power-rate components. The reduced power rating not only minimizes component size but also lowers losses, which in turn enhances system efficiency.

The efficacy of the proposed design is further demonstrated through the construction and testing of a 2000W prototype based on a TAB-based PPP-SIDO dc–dc converter. The experimental results confirm the theoretical predictions, showing that the architecture achieves both reduced power ratings and high efficiency. These findings substantiate the practical viability of architecture and its potential for real-world applications in high-performance power conversion.

# Chapter 4

# PPP Buck-Boost DC–DC Converter

Although the proposed PPP multiport dc–dc converter in Chapter 3 is capable of stepping up the voltage for certain ports and stepping down the voltage for others, it lacks the flexibility to provide a buck-boost function between an input and an output due to the fixed polarity of the series-connected modules. Furthermore, as highlighted in Section 1.4.3 of the literature review, existing PPP buck-boost schemes face significant limitations. These include difficulties in managing a wide voltage range or inefficiencies caused by the excessive use of PPP conversion modules, leading to redundancy.

To address these challenges and improve the versatility of PPP-based dc–dc converters in meeting the requirements of complex applications, this chapter will present a novel PPP buck-boost dc–dc converter. By building upon the modularization concept introduced in Chapter 2, the principles of existing PPP buck-boost schemes will be re-evaluated, culminating in the development of the proposed buck-boost topology. Furthermore, replacing the isolated modules with active bridge modules will facilitate a comprehensive analysis to enhance the understanding of the converter's operational principles. Finally, simulation and experimental results will be provided to validate the effectiveness of the proposed approach.

## 4.1 Modularization and Derivation of the Proposed PPP Buck-Boost Structure

### 4.1.1 Modularization of the Existing PPP Buck-Boost Structures

As described in Section 2.1, the isolated converter applied to the PPP structure can be modularized into two isolated parts, which are named as Module *P* and Module *S*. Module *P* is connected in parallel with either the input or output. Module *S* is in series connection between

the input and output. According to the polarity of the Module *S*, the PPP two-port structures can realize voltage step-up or down.

Based on the modularized PPP two-port structure, the existing two PPP buck-boost schemes in the literature review can be reinterpreted from a new perspective. For example, the key principle behind polarity reversal schemes is to make the series-connected Module *S* bi-polar, as shown in Figure 4.1(a). In this configuration, the polarity of Module *S* alone determines the voltage relationship between the source and load, which is $V_{out} = V_{in} \pm V_s$, while the connection of Module *P* to either $V_{in}$ or $V_{out}$ does not influence the buck or boost functionality.

Moreover, we can see it clearer that when $V_{out}$ reaches to $V_{in}$, $V_s$ reaches to zero, resulting in a large voltage gain ratio $V_p/V_s$. This means, when $V_{out}$ changing between buck and boost mode, a wide voltage gain range of $V_p/V_s$ is inevitable, followed by performance degradation which is already explained in Section 1.4.3.1. As for the two-stage scheme in Figure 1.22, it can be modularized and re-constructed, as shown in Figure 4.1(b). It actually integrates one step-up PPC in Figure 2.2(a) and one step-down PPC in Figure 2.2(c). The original output of the previous PPC and the input of the latter is integrated into an intermediate voltage $V_{int}$. This means, the input $V_{in}$ of Figure 4.1(b) is firstly stepped up to $V_{int}$ and then to be stepped down to $V_{out}$. By regulating the voltage relationships between $V_{s1}$ and $V_{s2}$ rather than reversing the polarity, both

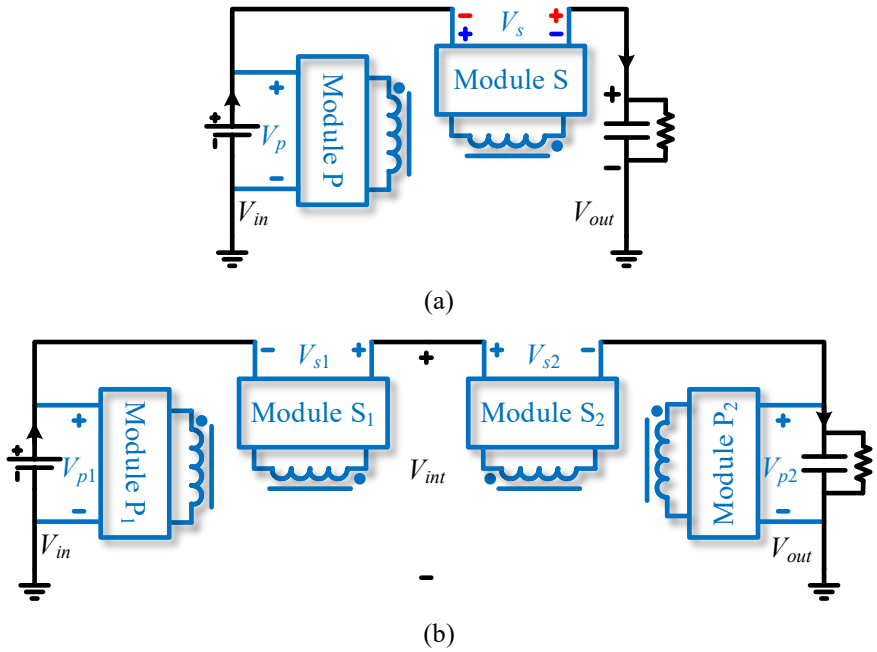



Figure 4.1 Modularized two existing PPP buck-boost schemes. (a) Polarity reversal scheme. (b) Two-stage scheme.

buck and boost function between $V_{in}$ and $V_{out}$ can be achieved. Compared to the polarity reversal scheme, the two-stage scheme can obtain reasonable voltage gain ratios among Module $S_{1,2}$ and Module $P_{1,2}$ even when $V_{in} = V_{out}$. However, the use of two PPP two-port converters, comprising a total of four PPP modules, introduces redundancy, which leads to increased costs and power losses.

### 4.1.2 Derivation of the Proposed PPP Buck-Boost Structure

Although the two-stage scheme in Figure 4.1(b) realizes buck-boost without polarity reversal and maintains a reasonable voltage gain range, it employs two PPCs consisting of four isolated modules, one of which is redundant. To save costs, the novel PPP buck-boost structure using only three modules is proposed in this section.

Drawing on the two-stage method, the two series-connected modules with opposite polarity are retained between the input and output ports to enable both voltage step-up and step-down operations. As discussed in Chapter 2, only one parallel-connected Module $P_1$ is required to balance the current difference between ports. Consequently, the potential topology options for a PPP buck-boost structure with only three isolated modules are illustrated in Figure 4.2. In Figure 4.2(a) the intermediate voltage $V_{int}$ is always the smallest, while in Figure 4.2(b), $V_{int}$ is the biggest. Module $P_1$ can be parallel connected to any of the voltages $V_{in}$, $V_{int}$ and $V_{out}$, depending on the configuration.

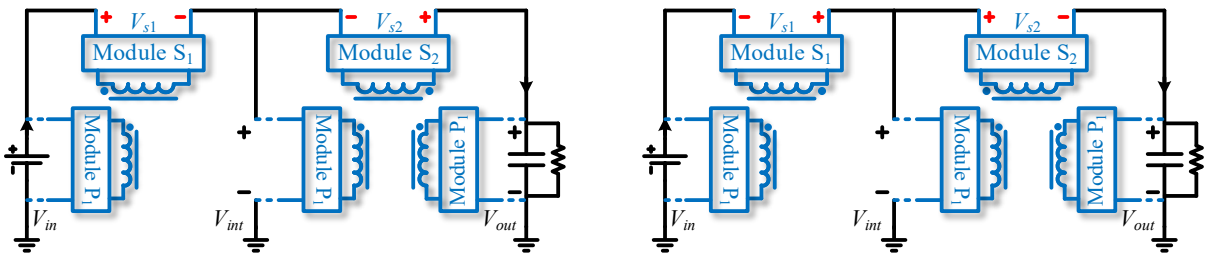



Figure 4.2 Potential topology options for PPP buck-boost structure with only three isolated modules. (a) $V_{in}>V_{int}$ and $V_{out}>V_{int}$. (b) $V_{in}<V_{int}$ and $V_{out}<V_{int}$.

Based on the comparative analysis in Chapter 2, the smallest partial power ratio is obtained when Module $P_1$ is connected to the port with the lowest voltage. To minimize the amount of

power processed by the modules, connecting Module $P_1$ to either port $V_{in}$ or $V_{out}$ is not optimal, as in a buck-boost converter, $V_{in}$ or $V_{out}$ will not always be the lowest voltage. Therefore, the structure where Module $P_1$ is connected to the lowest voltage $V_{int}$ is selected from Figure 4.2(a), as shown in Figure 4.3. From Figure 4.3, a centre capacitor is added at the intermediate voltage $V_{int}$ to mitigate voltage fluctuations, ensure greater stability, and reduce noise. Theoretically this capacitor does not consume energy. According to this connection, the intermediate voltage $V_{int}$ is equivalent to both the capacitor voltage $V_c$ and the voltage across the parallel module $V_{p1}$. From Figure 4.3, the voltage relationships are given by $V_{in} = V_c+V_{s1}$, $V_{out} = V_c+V_{s2}$. By appropriately setting the capacitor voltage $V_c$ and regulating $V_{s1}$ and $V_{s2}$, the buck-boost conversion can be achieved.

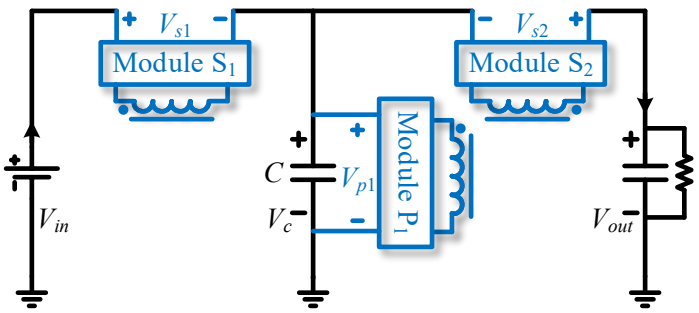



Figure 4.3 The proposed PPP buck-boost structure with only three isolated modules.

# 4.2 The Proposed PPP Buck-Boost Structure

The characteristics and advantages of the proposed PPP buck-boost structure will be illustrated in detail in this section, including partial power processing analysis, voltage gain range calculation, operational principle of the PPP buck-boost dc–dc converter based on TAB and so on.

## 4.2.1 Partial Power Processing

In full power processing, the source $V_{in}$ and load $V_{out}$ are connected in parallel with the input and output ports of the isolated dc–dc converter, i.e., two Module $P_{1,2}$, as shown in Figure 4.4(a). The total power $P_t$ flowing through the two parallel-connected modules can be then calculated in (4.1), which is the sum of both input and output power.

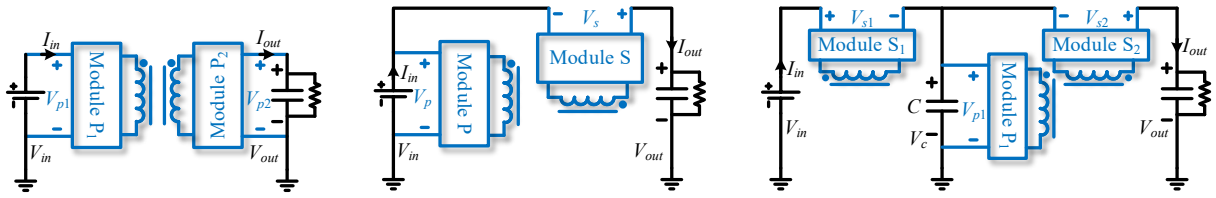



Figure 4.4 Two-port dc–dc converters using isolated modules. (a) Full power processing. (b) Partial power processing boost. (c) The proposed partial power processing buck-boost.

In the two-port PPC structure shown in Figure 4.4(b), one module is changed to be connected in series between the source and load. This module processes the power associated with the voltage difference, given by $|V_{in}-V_{out}|I_{out}$. Meanwhile, the power arising from the current difference is handled by the parallel-connected module, which is $|I_{in}-I_{out}|V_{in}$. This process is defined as partial power processing, on the one hand, only a portion of the total power is processed by modules, which can be expressed as $P_{p1}$ in (4.2). On the other hand, because the module voltage/current stresses, i.e., the average current/voltage of the modules, are decreased compared to the full power processing case. By reducing the voltage/current stresses and the amount of power processed by the modules, several losses, such as switching, conduction, and core losses, are mitigated. As a result, system efficiency is enhanced because a portion of the power bypasses the converter and flows directly to the load.

In the proposed PPP buck-boost dc–dc structure illustrated in Figure 4.4(c), the intermediate voltage $V_c$ is designed to always be smaller than both $V_{in}$ and $V_{out}$. Despite utilizing three modules, the current and voltage stresses in the system are still significantly reduced. The partial power caused by the current difference is processed by Module $P_1$, while the voltage differences between $V_c$ and $V_{in}/V_{out}$ is processed by two series-connected Module $S_1$ and Module $S_2$, respectively. Moreover, the sum of the partial power $P_{p2}$ flowing through the three isolated modules is calculated in (4.3). By comparing (4.1) and (4.3), the power processed by three modules in Figure 4.4(c) is also smaller than that of Figure 4.4(a). This indicates that, even with the inclusion of three isolated modules, the partial power processing function is effectively maintained.

$$P_t = V_{in}I_{in} + V_{out}I_{out} \tag{4.1}$$

$$P_{p1} = |V_{in} - V_{out}| \cdot I_{out} + |I_{in} - I_{out}| \cdot V_{in} \tag{4.2}$$

$$P_{p2} = (V_{in} - V_c) \cdot I_{in} + (V_{out} - V_c) \cdot I_{out} + |I_{in} - I_{out}| \cdot V_c \tag{4.3}$$

Furthermore, varying the settings for the intermediate voltage $V_c$ will affect the ratio of the partial power $P_{p2}$ to the total power $P_t$. Take the application of $V_{in}$ = 120 V, $I_{in}$ = 2 A and $V_{out}$ = 110 V∼130 V as an example, the partial power ratio $P_{p2}/P_t$ changing with the intermediate voltage $V_c$ is drawn in Figure 4.5. From Figure 4.5, the ratio $P_{p2}/P_t$ remains consistently less than 1 in both buck and boost modes, indicating that only a portion of the total power is processed by the power conversion modules, which in turn reduces power losses. In terms of PPP, the larger the intermediate voltage $V_c$ is, the smaller partial power ratio $P_{p2}/P_t$.

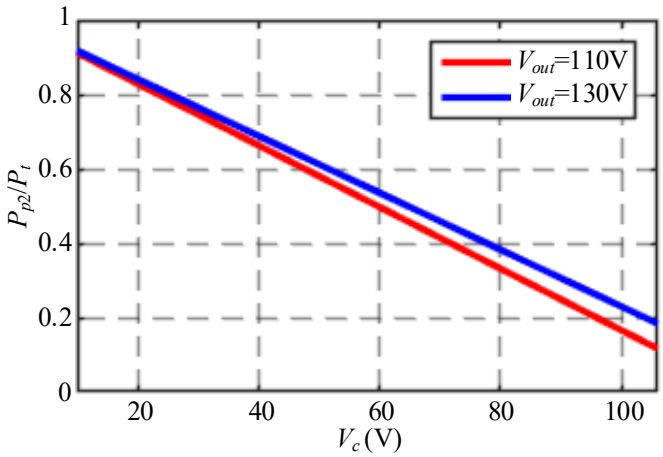
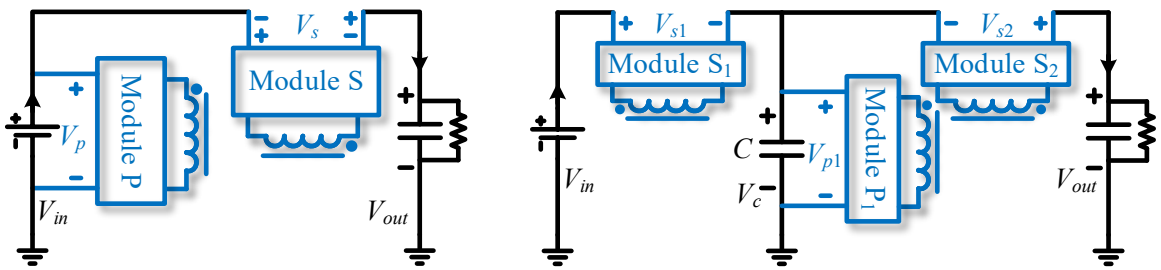



Figure 4.5 The partial power ratio $P_{p2}/P_t$ changing with the intermediate voltage $V_c$.

## 4.2.2 Voltage Gain Range

When we discuss the limitation of the existing PPP buck-boost dc–dc structure based on two modules in Figure 4.6(a), the main concern is the wide voltage gain range requirement facing the buck and boost variation. When the isolated modules are operated in a wide voltage gain range, the fixed hardware design cannot always ensure a relatively good performance within the wide range.

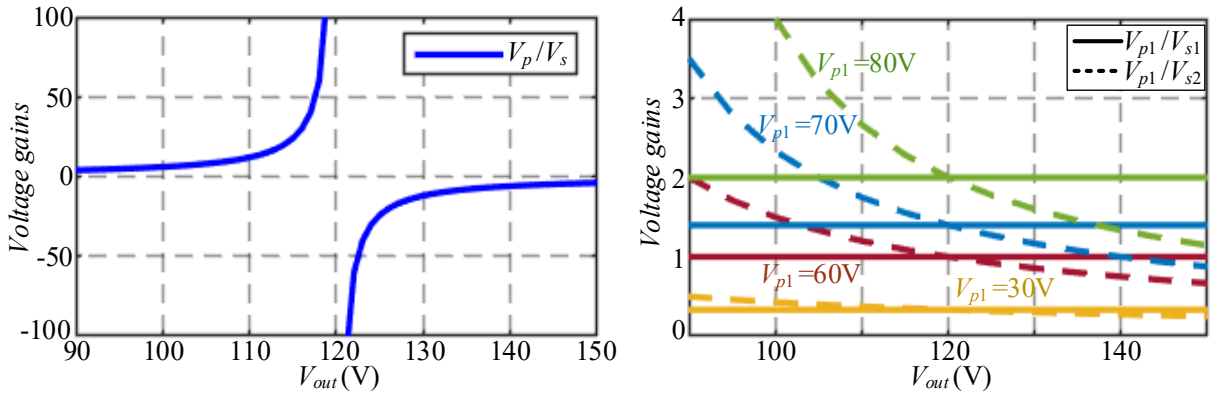
To prevent a wide voltage gain range during the transition from buck to boost mode, the proposed PPP buck-boost structure in Figure 4.6(b) uses two series-connected modules with polarity reversal. The corresponding voltage relationship is $V_{out} = V_{in}+V_{s1}-V_{s2}$. Therefore, even when the output voltage $V_{out}$ reaches the input voltage $V_{in}$, $V_{s1,2}\neq 0$ can be ensured so that the voltage gain between the isolated modules can be successfully limited to a reasonable range.




(a) (b)

Figure 4.6 Two types of two-port PPP buck-boost dc–dc structures. (a) Based on two isolated modules with polarity reversal scheme. (b) Based on three isolated modules without polarity reversal.

More specifically, the application of $V_{in}$ = 120 V, $I_{in}$ = 2 A and $V_{out}$ = 110 V∼130 V is still taken as the example, and the voltage gain ranges for both two PPP buck-boost dc–dc structures are drawn in Figure 4.7. From Figure 4.7(a), the PPP buck-boost structure with two isolated modules faces a wide range of voltage gain, which is over −100 to 100. This is because when $V_{out}$ approaches $V_{in}$, the series-connected module voltage $V_s$ approaches 0, leading a large voltage gain $V_p/V_s$. Within this wide variation range, a fixed hardware design cannot always ensure a good performance of power transmission between two modules, which may be large circulating current, increased power loss and so on. By contrast, from Figure 4.7(b), when the intermediate voltage $V_{p1}$ is fixed, the voltage gain of $V_{p1}/V_{s1}$ is also fixed although the output voltage is rising. In addition, the voltage gain of $V_{p1}/V_{s1}$ decreases slowly within a narrow range especially compared to the trends in Figure 4.7(a). Moreover, the changing of the voltage gain in Figure 4.7(b) is very smooth when switching between the buck and boost modes, which is no sudden




(a) (b)

Figure 4.7 The voltage gains between the parallel-connected module and the series-connected module. (a) PPP buck-boost dc–dc structures with two modules. (b) The proposed PPP buck-boost dc–dc structures with three modules.

changes shown in Figure 4.7(a). Both the narrow range and smooth change contribute to a simple control and a steady performance for power transmission among isolated modules. Furthermore, under differing intermediate voltage $V_{p1}$, the voltage gain ranges can be influenced. According to this, the settings of the intermediate voltage $V_{p1}$ can be further designed according to the specific applications.

## 4.3 The Proposed TAB-Based PPP Buck-Boost DC–DC Converter

To demonstrate how three isolated modules of the proposed PPP buck-boost structure in Figure 4.3 operate together to achieve both buck and boost functionality, they are replaced by a TAB converter. This means, the TAB-based PPP buck-boost dc–dc converter is derived, as shown in Figure 4.8. From Figure 4.8, three modules are labeled $M_1$~$M_3$, where each module $M_k(k = 1, 2, 3)$ functions as an active bridge. Each active bridge consists of four switches $S_{k1}$~$S_{k4}(k = 1, 2, 3)$, one series-connected inductor $L_k(k = 1, 2, 3)$, and one side of the winding in a three-winding transformer, with a turns ratio of $N_k(k = 1, 2, 3)$. The three modules are connected in a T-shaped configuration: two series-connected modules with opposite polarity are placed between the input and output, while the parallel-connected module is linked to the intermediate voltage at the centre.

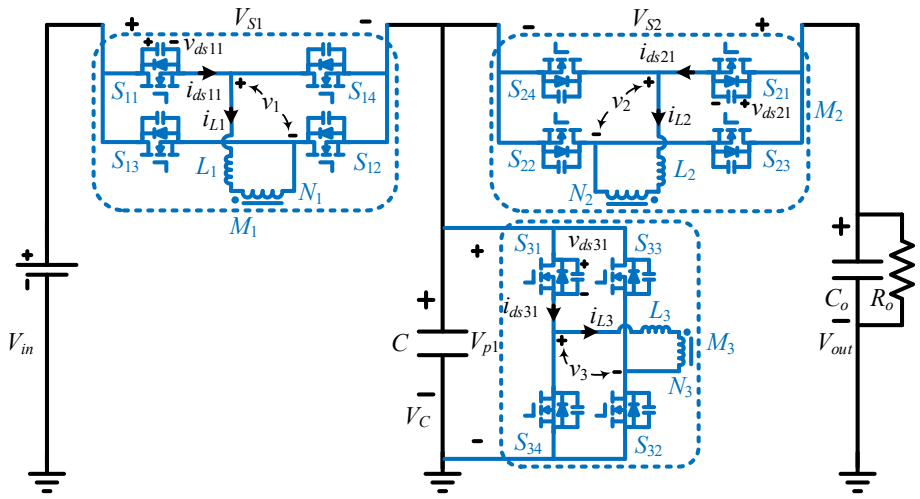



Figure 4.8 A schematic of the proposed PPP buck-boost dc–dc converter showing the triple active bridge components.

### 4.3.1 Operational Principle of the Proposed TAB-Based PPP Buck-Boost

Because the proposed TAB-based PPP buck-boost dc–dc converter only changes the connections between the input/output port and the traditional TAB, the operational principle of TAB will be demonstrated at first. The sketch showing the idealized waveforms of the active bridge modules is shown in Figure 4.9. With reference to Figure 4.8 and Figure 4.9, the drive signals of the switches $S_{k1}$~$S_{k4}$($k$ = 1, 2, 3) are $v_{gsk1}$~$v_{gsk4}$($k$ = 1, 2, 3), respectively. $S_{k1}$ and $S_{k2}$ are switched synchronously, as are $S_{k1}$ and $S_{k2}$. In addition, $S_{k1}$ and $S_{k3}$ are turned on complementarily with a 50% duty cycle. The phase shift angles of $v_{gs11}$ and $v_{gs21}$ with respect to $v_{gs31}$ are defined as $\varphi_1$ and $\varphi_2$ in radians, respectively. According to the relative position of $v_{gs11}$~$v_{gs31}$, $\varphi_1$<0 and $\varphi_2$>0.

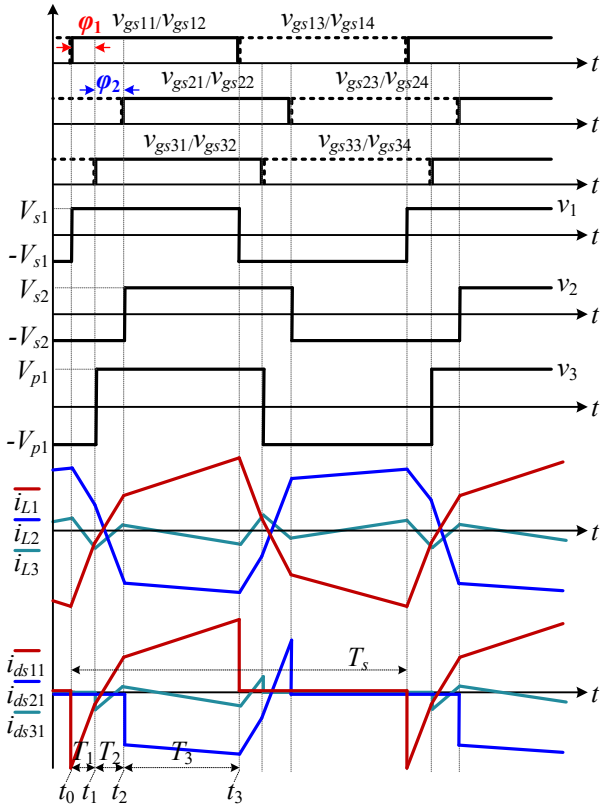



Figure 4.9 Idealized waveforms of the traditional TAB dc–dc converter.

According to TAB-based analysis in Section 3.2.1, TAB can be analyzed and calculated based on either star-equivalent or triangle-equivalent model as shown in Figure 3.4. In this chapter, the

TAB is applied to regulate the module voltages for the buck-boost application. This means that the module voltages $V_{s1}$, $V_{s2}$ and $V_{p1}$ will fluctuate, resulting in an amplitude change of $v_1$~$v_3$. In this situation, the fixed value of the transformer turns ratio $N_1$~$N_3$ and the series-connected inductance $L_1$~$L_3$ cannot always match the voltage ratios of $v_1$~$v_3$. The unmatched value will make the calculation and analysis much more complicated if applying the star-equivalent model which is used in Chapter 3. To simplify the calculation, the triangle-equivalent model in Figure 3.4(c) is used. Based on the triangle-equivalent model and power expressions in (3.12) and (3.13), the virtual power controlled by $\varphi_1$ and $\varphi_2$ can be re-expressed in (4.4), and the actual power can be obtained by adding the virtual power together as shown in (4.5). Similarly, when the virtual inductor currents $i_{L12}$, $i_{L13}$ and $i_{L32}$ are superimposed in pairs, the idealized waveforms of the active bridge modules can be obtained in (4.6).

$$\begin{cases} P_{12} = -P_{21} = \dfrac{V_{s1}V_{s2}N_1}{\omega L_{12}N_2}(\varphi_2 - \varphi_1)\left(1 - \dfrac{(\varphi_2 - \varphi_1)}{\pi}\right) \\ P_{13} = -P_{31} = \dfrac{V_{s1}V_{p1}N_1}{\omega L_{13}N_3}(-\varphi_1)\left(1 - \dfrac{(-\varphi_1)}{\pi}\right) \\ P_{32} = -P_{23} = \dfrac{V_{p1}V_{s2}N_1^2}{\omega L_{32}N_3N_2}\varphi_2\left(1 - \dfrac{\varphi_2}{\pi}\right) \end{cases} \tag{4.4}$$

$$\begin{cases} P_1 = P_{12} + P_{13} \\ P_2 = -P_{12} - P_{32} \\ P_3 = -P_{13} + P_{32} \end{cases} \tag{4.5}$$

$$\begin{cases} i_{L1} = i_{L12} + i_{L13} \\ i_{L2} = (-i_{L12} - i_{L32})N_1/N_2 \\ i_{L3} = (-i_{L13} + i_{L32})N_1/N_3 \end{cases} \tag{4.6}$$

### 4.3.2 Phase Shift Angles

By combining (4.4) and (4.5), the phase shift $\varphi_1$ and $\varphi_2$ can be calculated out with the given input/output power and the hardware parameters. Take the system parameters $V_{in}$ = 120 V, $I_{in}$ = 2 A, $V_{out}$ = 110~130 V as an example, the phase shift $\phi_1$ and $\phi_2$ in angles changing with the output voltages are drawn in Figure 4.10. In Figure 4.10, the intermediate voltage $V_{p1}$ is set as 65 V with the series-connected inductances $L_1 = L_2 = L_3$= 18 $\mu$H.

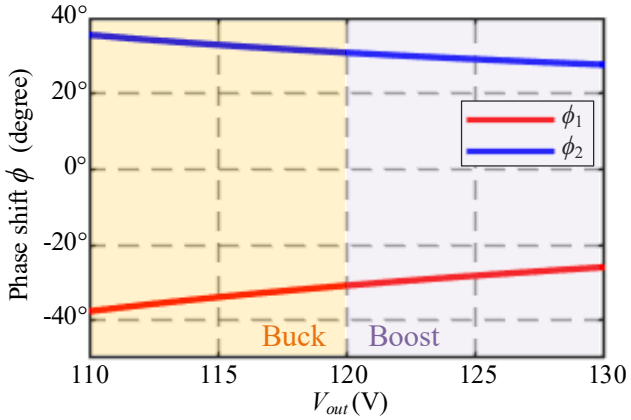



Figure 4.10 Phase shift angles $\phi_1$ and $\phi_2$ changing with the output voltages $V_{out}$ = 110~130 V.

From Figure 4.10, the output voltage $V_{out}$ can be smoothly regulated between buck and boost modes through the phase shift angles $\phi_1$ and $\phi_2$. Moreover, different settings of the intermediate voltage $V_{p1}$, still allow for effective voltage regulation via the phase shift angles.

### 4.3.3 Settings For the Intermediate Voltage $V_{p1}(V_c)$

The intermediate voltage $V_{p1}$, which corresponds to $V_c$ as shown in Figure 4.8, significantly influences both the voltage gains among the three modules and the partial power ratio $P_{p2}/P_t$. Generally, maintaining a narrow voltage gain range is essential for ensuring optimal performance within a fixed hardware design when the output voltage transitions between buck and boost modes. Specifically, when the turns ratio of the transformer and the series-connected inductances are aligned with the voltage gain, a small circulating current can be sustained, which typically results in a low RMS inductor current in the TAB circuit. Conversely, if the voltage gains deviate from the fixed transformer ratio as the output voltage varies, the RMS inductor current will increase, leading to substantial conduction losses. Therefore, from a performance standpoint, it is desirable for the intermediate voltage setting to facilitate a narrow voltage gain range. Additionally, minimizing the partial power ratio is expected to enhance overall system efficiency.

The voltage gains and partial power ratio changing with the intermediate voltage $V_{p1}(V_c)$ are illustrated in Figure 4.11(a) and Figure 4.11(b), respectively. From Figure 4.11(a), it can be observed that the voltage gain of $V_{p1}/V_{s2}$ varies with the different output voltages. When the intermediate voltage $V_{p1}(V_c)$ is set to 65 V, the voltage gain $V_{p1}/V_{s2}$ is 1.44 and 1 when output voltage is 110 V and 130 V, respectively, indicating that the voltage gain range is close to 1. From

Figure 4.11(b), a larger intermediate voltage $V_{p1}(V_c)$ results in a smaller partial power ratio $P_{p2}/P_t$ will be. Specifically, when $V_{p1}(V_c)$ is set to 65 V, the partial power ratio $P_{p2}/P_t$ is 0.46 and 0.5 for output voltages $V_{out}$ of 110 V and 130 V, respectively.

To minimize the circulating current thereby reducing conduction losses, it is essential for the fixed turns ratio and the series-connected inductance to consistently align with the fluctuating voltage gains. Therefore, 65 V is identified as the optimal intermediate voltage $V_{p1}(V_c)$, as it ensures that the voltage gains oscillate around unity, facilitating a transformer turns ratio design of 1:1:1. Simultaneously, this configuration allows approximately half of the total power to be processed by the converter, achieving effective power reduction. While selecting a higher intermediate voltage $V_{p1}(V_c)$ could obtain a smaller partial power ratio, it would inevitably result in a broader voltage gain range. This discrepancy in parameters heightens the risk of losing soft switching, leading to increased switching losses. Considering these risks of elevated losses that compromise the high efficiency of PPP, a balanced trade-off leads to the selection of 65 V as the optimal intermediate voltage $V_{p1}(V_c)$.

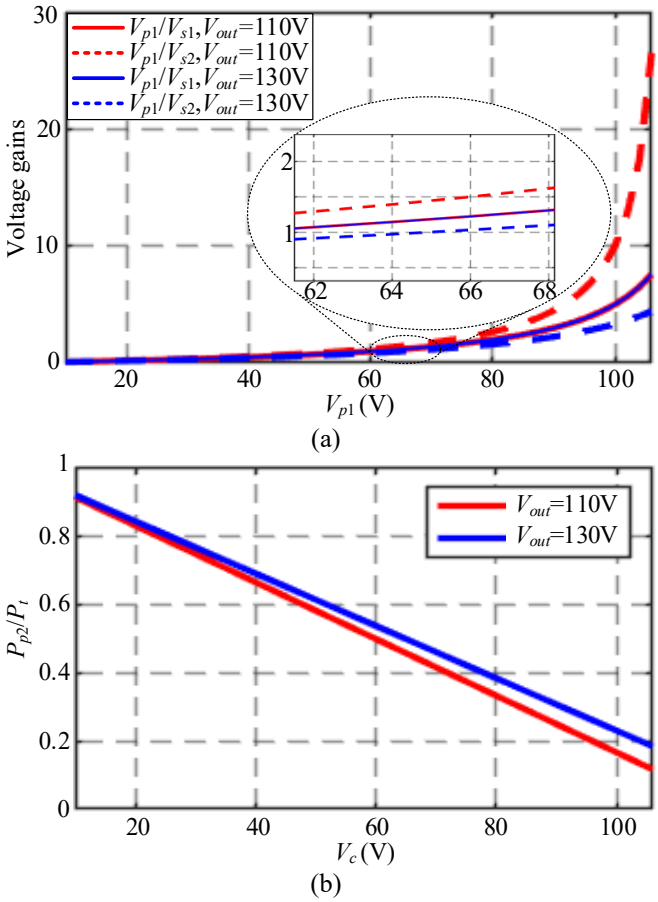



Figure 4.11 Intermediate voltage $V_{p1}(V_c)$ influences both voltage gains and partial power ratio $P_{p2}/P_t$.

### 4.3.4 Voltage And Current Stresses

According to Figure 4.9, which is partly redrawn in Figure 4.12, the module voltages $V_{s1}$, $V_{s2}$ and $V_{p1}$ are regarded as voltage stresses, and the RMS currents $I_{dsk1,\mathrm{rms}}$ of switches $S_{k1}$($k$ = 1, 2, 3) are defined as current stresses.

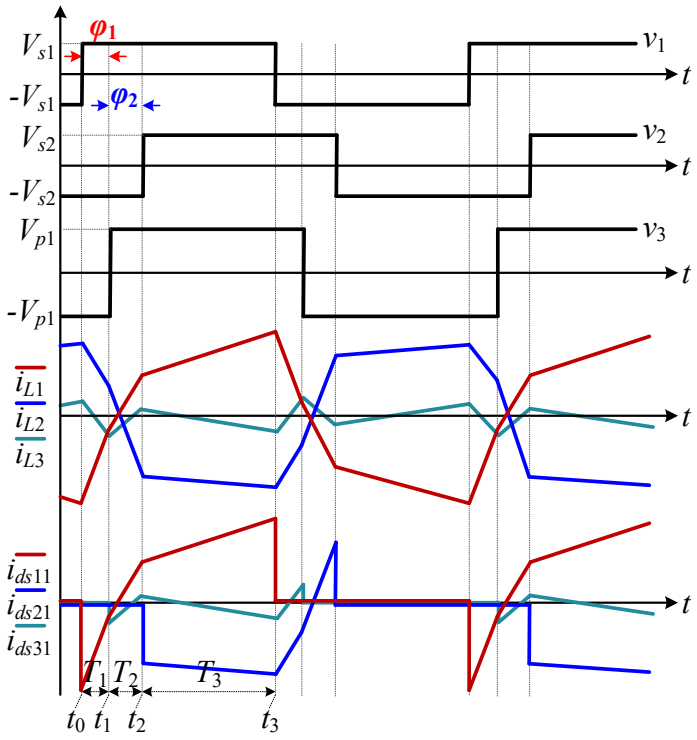



Figure 4.12 Key waveforms of the traditional TAB dc–dc converter helping calculated voltage/current stresses.

Under the system parameters $V_{in}$ = 120 V, $I_{in}$ = 2 A, $V_{out}$ = 110~130 V, when the intermediate voltage $V_{p1}(V_c)$ is set as 65 V, the voltage stresses are shown in (4.7). By setting the intermediate voltage $V_{p1}(V_c)$ to around half of the input/output voltage, all the voltage stresses of three modules are significantly reduced, maintaining the benefit of PPP.

$$\begin{cases} V_{p1} = 65V \\ V_{s1} = 55V \\ V_{s2} = 45V \sim 65V \end{cases} \tag{4.7}$$

According to the basic calculation based on DAB in (3.7), (3.9) and the superposition based on the triangle-equivalent model as shown in (4.6), the inductor current $i_{Lk}$ ($k$ = 1, 2, 3) at $t_0$~$t_3$ can be easily obtained. Then the current stresses can be given as follows:

$$I_{dsk1,rms}=\sqrt{\frac{1}{3T_s}\left(A_{Lk}+B_{Lk}+C_{Lk}\right)} \tag{4.8}$$

where $\begin{cases} A_{Lk}=\left(i_{Lk}^2(t_0)+i_{Lk}^2(t_1)+i_{Lk}(t_0)\cdot i_{Lk}(t_1)\right)\cdot T_1 \\ B_{Lk}=\left(i_{Lk}^2(t_1)+i_{Lk}^2(t_2)+i_{Lk}(t_1)\cdot i_{Lk}(t_2)\right)\cdot T_2 \\ C_{Lk}=\left(i_{Lk}^2(t_2)+i_{Lk}^2(t_3)+i_{Lk}(t_2)\cdot i_{Lk}(t_3)\right)\cdot T_3 \end{cases}$ and $\begin{cases} T_1=0.5T_s\cdot|\varphi_1|/\pi \\ T_2=0.5T_s\cdot|\varphi_2|/\pi \\ T_3=0.5T_s-T_1-T_2 \end{cases}$.

It noteworthy that if the turns ratio of the transformer and the inductance matches the port voltage gain, which is $V_{s1}/V_{s2}/V_{p1}$ = $N_1/N_2/N_3$ and $N_1^2/N_2^2/N_3^2$ = $L_1/L_2/L_3$, then the inductor voltage $V_{Lk}(t_2\sim t_3)=0$ ($k$ = 1, 2, 3). This means the inductor current is constant during $t_2\sim t_3$. On the contrary, as the voltage gains changes away from the transformer turns ratio $N_1/N_2/N_3$, the inductor current slope during $t_2\sim t_3$ becomes steeper and its current spike gets larger if the power through the inductor is fixed, resulting in an increase of the current stress. Therefore, both the transformer turns ratio and inductances will be designed to be as close to the voltage gain range as possible. Accordingly, based on (4.7), the transformer turns ratios will be given as $N_1/N_2/N_3$ = 1:1:1. Moreover, according to the design considerations in Section 3.3.3, the smaller the value of the series-connected inductance, the larger the power can be processed by the isolated modules. However, as the value of the inductance decreases, smaller phase shift angles are required for the same power level. If the phase shift value is too small, it may cause control issues. By taking the above restrictions into consideration, the inductances for $V_{p1}(V_c)$ = 65 V are designed as $L_1$ = $L_2$ = $L_3$ = 18 $\mu$H. Based on the designed parameters and expression in (4.8), the corresponding current stresses $I_{dsk1,\mathrm{rms}}$ ($k$ = 1, 2, 3) changing with the output voltage $V_{out}$ is drawn in Figure 4.13.

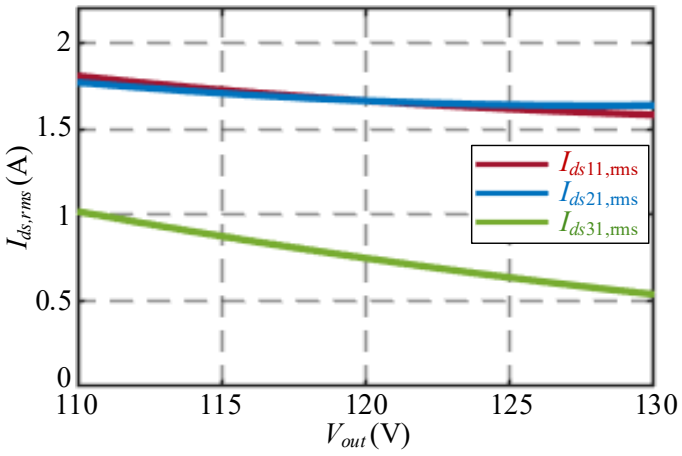



Figure 4.13 Current stresses $I_{ds,\mathrm{rms}}$ changing with the varying output voltage $V_{out}$ = 110~130 V.

From Figure 4.13, when $V_{out}$ = 110 V, the current stresses ($I_{ds11,rms}$, $I_{ds21,rms}$, $I_{ds31,rms}$) = (1.81 A, 1.77 A, 1.02 A). When $V_{out}$ = 130 V, ($I_{ds11,rms}$, $I_{ds21,rms}$, $I_{ds31,rms}$)=(1.58 A, 1.64 A, 0.54 A). Given the input current is 2 A, the current stresses of three modules are reasonable. Moreover, owing to the PPP connection, the current stress $I_{ds31,rms}$ of the parallel-connected module is relatively smaller than the other two.

### 4.3.5 Soft Switching Considerations

To prevent hard switching and minimize switching losses, achieving soft switching is also a key objective of the proposed TAB-based PPP buck-boost dc–dc converter. ZVS is realized by introducing a practical dead time between complementary drive signals. Take switch $S_{11}$ as an example, to achieve ZVS turn-on, one condition is that its drain-to-source current $i_{ds11}$ is negative during the dead time between $v_{gs13}$ drops and $v_{gs11}$ rises. Another condition is that the parasitic capacitance of the switch must be discharged, allowing the drain-to-source voltage $v_{ds11}$ to drop to zero before the dead time ends. Once $v_{ds11}$ reaches zero, the body diode conducts due to the negative drain-to-source current $i_{ds11}$, clamping the drain-to-source voltage $v_{ds11}$ at zero for the remainder of the dead time. Then, with the drive signal $v_{gs11}$ rises up, the ZVS turn-on of the switch $S_{11}$ is achieved. In addition, due to the symmetry of TAB, $i_{ds11}$ is positive when the switch $S_{11}$ is turned off, thereby avoiding reverse-recovery issues.

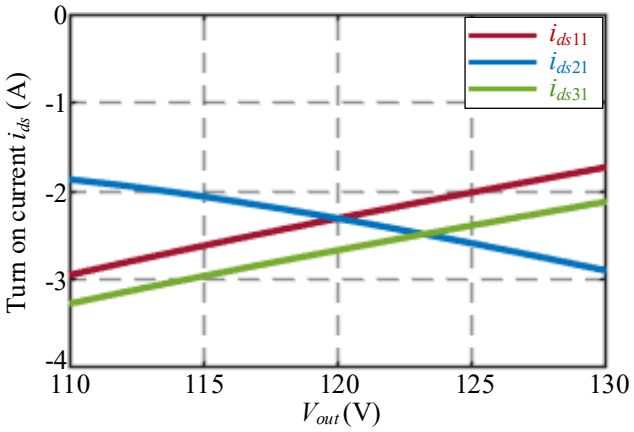



Figure 4.14 Drain-to-source currents $i_{ds11}$~$i_{ds31}$ of switches $S_{11}$~$S_{31}$ when they are turned on.

To help determine whether the circuit can achieve soft switching, the drain-to-source currents $i_{ds11}$~$i_{ds31}$ when the corresponding switches are turned on are drawn in Figure 4.14. From Figure

4.14, the drain-to-source currents ($i_{ds11}$, $i_{ds21}$, $i_{ds31}$) = (−2.95 A, −1.87 A, −3.28 A) and (−1.73 A, −2.90 A, −2.12 A) when $V_{out}$ = 110 V and $V_{out}$ = 130 V, respectively. Because the currents are all negative, it is possible to realize soft switching.

Another condition for achieving ZVS turn-on is whether the parasitic capacitor can fully discharge, allowing the drain-to-source voltage to drop to zero during the dead time. Both the discharge voltage and discharge current, represented by $V_{ds}$ and $I_{ds}$ in (4.7) and Figure 4.14, respectively, influence the discharge rate. The smaller the discharge voltage and the larger the discharge current, the easier it is to complete the discharge within the dead time. The realization of ZVS under these conditions will be verified through subsequent simulations and experiments.

# 4.4 Simulation and Experiment Verification of the Proposed TAB-Based PPP Buck-Boost DC–DC Converter

To verify the validation of the proposed TAB-based PPP buck-boost dc–dc converter, both simulation and experiment are conducted under the designed parameters, as shown in Table 4.1.

Table 4.1
SYSTEM PARAMETERS

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| Input Voltage $V_{in}$ | 120 V | Output Power $P_{out}$ | 240 W |
| Output Voltage $V_{out}$ (buck) | 110 V | Switching Period $T_s$ | 10 $\mu$s |
| Output Voltage $V_{out}$ (boost) | 130 V | Series Inductances ($L_1$/$L_2$/$L_3$) | 18/18/18 $\mu$H |
| Intermediate voltage $V_c$ | 65 V | Turns Ratio $N_1$:$N_2$:$N_3$ | 1:1:1 |

## 4.4.1 Simulation Settings Based On SIMULINK/MATLAB Software

To demonstrate the advantages of partial power processing in the proposed TAB-based PPP buck-boost dc–dc converter, the simulation focuses on key power losses, including conduction losses, switching losses, and core losses.

Specifically, the MOSFET model of IMBG120R060M1H from the SIMULINK library, which is behavioral model, is used for the switches in the converter. Its built-in mathematical equations

enable tracking of conduction and switching losses, which vary with drain-to-source voltage and current, using ideal gate drive signals. Additionally, a series resistor of 0.1Ω is included in the simulation to model the conduction losses of the inductors, with this value determined through physical testing of the inductor. The skin effect is negligible in the following physical experiment due to the use of Litz wire. Its multiple insulated strands ensure even current distribution across the cross-section, reducing AC resistance and effectively minimizing the skin effect at high frequencies.

Furthermore, an equivalent circuit of the transformer is provided by SIMULINK, as shown in Figure 4.15. This model is based on a physical three-winding transformer, where the primary, secondary, and tertiary windings share a common magnetic core, exhibiting nonlinear magnetic properties under varying loads and excitation conditions. The model incorporates nonlinear magnetization curves to accurately represent the core's B-H relationship, accounting for saturation effects and harmonic distortions. The transformer is designed to operate within the saturation region to reflect real-world behavior. As shown in Figure 4.15, a magnetization resistor ($R_m$) is included in the three-winding transformer model, along with other magnetization parameters, to simulate the ferrite core's characteristics. The leakage inductances, resistances, and parasitic parameters are idealized for simplicity. To approximate the core losses, which are influenced by the power processed by the transformer, the core loss is calculated using the formula $P_{core\ loss} = V_{prim}^2/R_m$. This simplifies the representation of complex transformer parameter curves. Based on the system parameter $V_{s1}$ = 55 V and an expected core loss of approximately 0.3 W (based on practical experience), the magnetization resistor $R_m$ is set to $R_m$ = $55V^2/0.3W \approx 10000\Omega$ in the simulation.

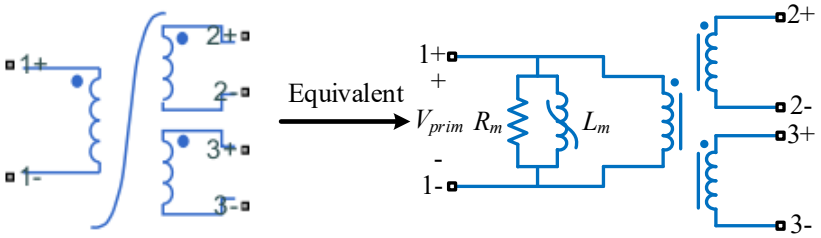


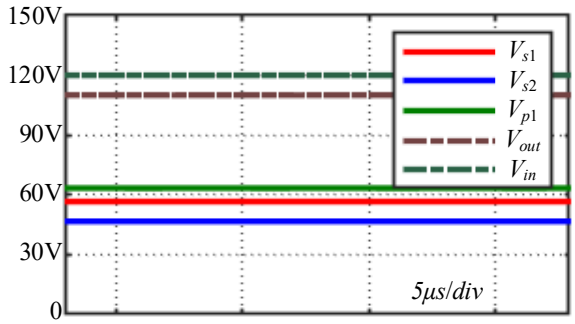

Figure 4.15 Equivalent circuit topology of the three-winding transformer with a nonideal core.

### 4.4.2 Simulation Results

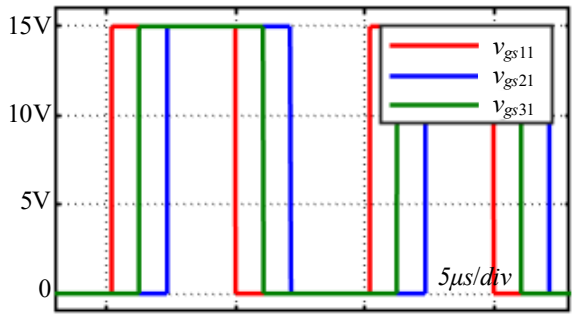
When the intermediate voltage $V_{p1}(V_c)$ is set as 65 V with the series inductances $L_1 = L_2 = L_3$ = 18 $\mu$H, the simulation results for both buck ($V_{out}$ = 110 V, $R_{out}$ = 50.4Ω) and boost ($V_{out}$ = 130 V, $R_{out}$ = 70.4Ω) modes are presented in Figure 4.16∼Figure 4.19. Among them, Figure 4.16 and Figure 4.17 demonstrate port voltages $V_{s1}$, $V_{s2}$, $V_{p1}$, $V_{in}$ and $V_{out}$, along with the drive signals $v_{gs11}$∼$v_{gs31}$, and the inductor currents $i_{L1}$∼$i_{L3}$ for both buck and boost modes, respectively. Figure 4.18 and Figure 4.19 show the drain-to-source current $i_{ds}$, drain-to-source voltage $v_{ds}$, and the corresponding complementary drive signals, which include a 200ns dead time, to verify whether ZVS is achieved for switches $S_{11}$∼$S_{31}$ in both buck and boost modes.

As illustrated in Figure 4.16 and Figure 4.17, the key waveforms for both buck and boost modes exhibit similar behavior. As can be seen from Figure 4.16(a) and Figure 4.17(a), it is evident that in buck mode, $V_{s1}$ is larger than $V_{s2}$, while in boost mode, the opposite occurs. The transition between buck and boost modes can be easily achieved by adjusting the phase shift angles, as demonstrated in Figure 4.16(b) and Figure 4.17(b), corresponding to phase shift angles ($\phi_1$, $\phi_2$) = (−37.2°, 34.7°) for buck mode and ($\phi_1$, $\phi_2$) = (−26.9°, 28.1°) for boost mode.

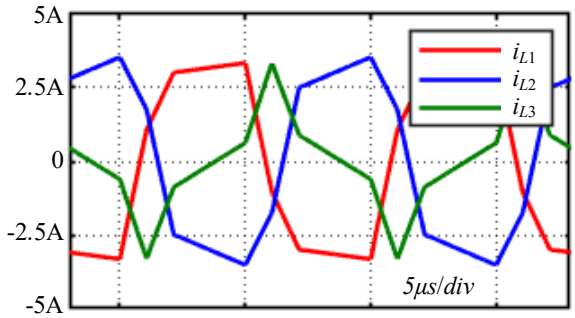
In addition, the module voltages $V_{s1}$, $V_{s2}$ and $V_{p1}$ remain consistently around 60 V, which ensures stable voltage gains with a ratio of 1:1:1. This is in alignment with the transformer's turns ratio design of 1:1:1, helping to minimize current spikes and reduce current stress, as shown in Figure 4.16(c) and Figure 4.17(c). Additionally, owing to the PPP-based structure design and the setting of $V_{p1}(V_c)$ at 65 V, the voltage stress on all three modules is reduced to approximately half of the input and output voltages. Despite the ideal designed total power is 480W, which is the sum of both input and output power, only 220.8W and 240W of partial power is processed by the power conversion modules $M_1$∼$M_3$ in buck and boost modes, respectively. The reduced voltage stress, combined with partial power processing, significantly contributes to lower overall power losses.




(a) port voltages

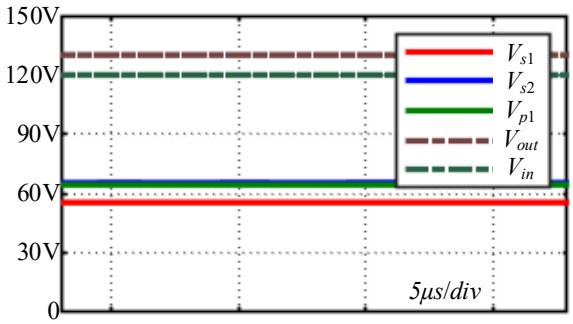



(b) drive signals

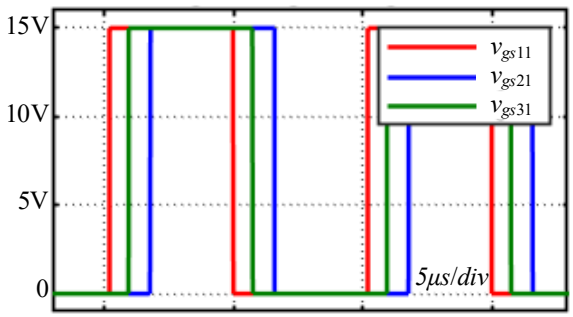



(c) inductor currents

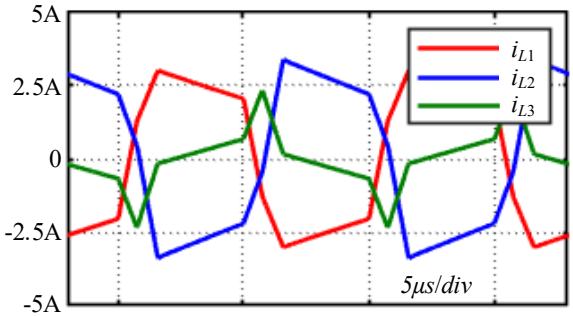
Figure 4.16 Simulation results when $V_c$ = 65 V in buck mode ($V_{out}$ = 110 V).




(a) port voltages



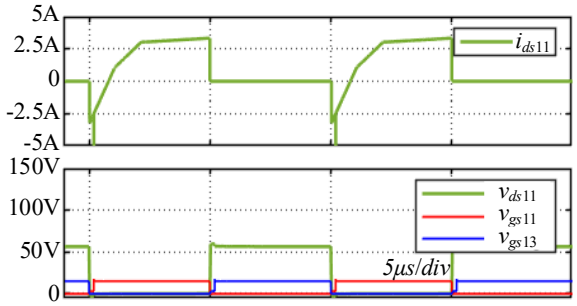

(b) drive signals



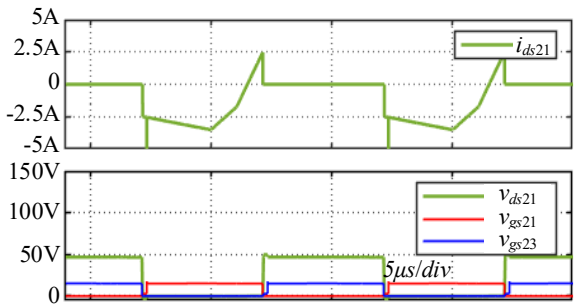

(c) inductor currents

Figure 4.17 Simulation results when $V_c$ = 65 V in boost mode ($V_{out}$ = 130 V).

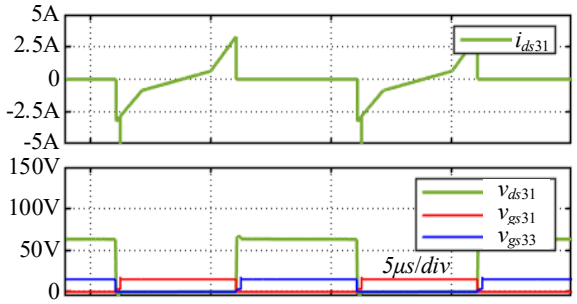
From Figure 4.18 (a), the drain-to-source voltage $v_{ds11}$ of switch $S_{11}$, for instance, begins to decrease as $v_{gs31}$ drops. Due to the low discharge voltage $V_{ds11}$ and high discharge current $i_{ds11}$, $v_{gs31}$ successfully drops to zero before its drive signal $v_{gs11}$ rises, thereby achieving ZVS turn-on. In addition, $i_{ds11}$ remains positive when $S_{11}$ is turned off, which means no current flows through its body diode. Therefore, there is no reverse recovery problem, and the reverse recovery loss is avoided. Overall, soft switching is successfully realized for $S_{11}$. Due to symmetricity, all the switches in Module 1 can realize ZVS operation. Similarly, from Figure 4.18 and Figure 4.19, all the switches across three modules can successfully realize soft switching in both buck and boost modes.




(a) ZVS of $S_{11}$

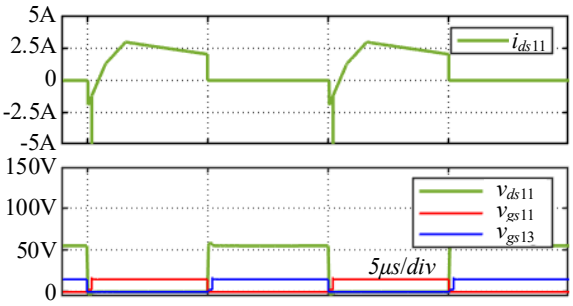



(b) ZVS of $S_{21}$

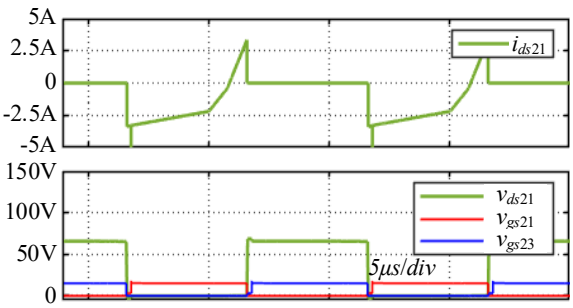



(c) ZVS of $S_{31}$

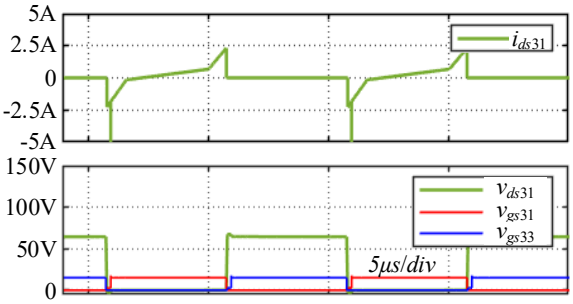
Figure 4.18 ZVS realization of three modules in buck mode ($V_{out}$ = 110 V).




(a) ZVS of $S_{11}$




(b) ZVS of $S_{21}$




(c) ZVS of $S_{31}$

Figure 4.19 ZVS realization of three modules in boost mode ($V_{out}$ = 130 V).

Attributing to low current and voltage stresses, small partial power and soft switching, the efficiency of the proposed TAB-based PPP buck-boost dc–dc converter is high. The power loss distribution and the efficiencies are also given by the simulator, which are concluded in Table 4.2. From the simulation results, the RMS values of the inductor currents across the three modules are $I_{L1,\mathrm{rms}}/I_{L2,\mathrm{rms}}/I_{L3,\mathrm{rms}}$ = 2.57/2.53/1.38 A in buck mode and $I_{L1,\mathrm{rms}}/I_{L2,\mathrm{rms}}/I_{L3,\mathrm{rms}}$ = 2.2/2.37/0.84 A in boost mode. Combining the series resistor of 0.1Ω, the sum of the conduction losses for inductors are 1.49 W in buck mode and 1.11 W in boost mode. Because the currents stresses in buck mode are larger than that of boost mode, both conduction losses of switches and inductors in the former are larger. In addition, the core loss in buck mode is smaller than that of

the boost mode because the partial power flowing though the transformer in buck mode is smaller, which can be corresponds to the theoretical results in Figure 4.11(b). Moreover, the switching losses are ignored due to ZVS realization. To achieve output powers of 240.4 W and 240.3 W, the actual input powers are 245.87 W and 244.66 W in buck and boost modes, respectively, resulting in efficiencies of 97.77% and 98.22%.

Table 4.2
POWER LOSSES DISTRIBUTION AND EFFICIENCIES UNDER DIFFERENT PARAMETERS

| **Power losses and efficiencies** | **$V_c$=65V buck** | **$V_c$=65V boost** |
|---|---|---|
| Conduction losses (switches) | 3.82W | 2.96W |
| Switching losses | 0 | 0 |
| Conduction losses (inductors) | 1.49W | 1.11W |
| Core losses | 0.19W | 0.26W |
| Input power | 245.87W | 244.66W |
| Output power | 240.4W | 240.3W |
| Efficiencies | 97.77% | 98.22% |

### 4.4.3 Experimental Settings

The experimental setup, as shown in Figure 4.20, comprises an oscilloscope, a low voltage power supply, a high voltage power supply, an electronic dc load, and the experimental circuit housed within a high-temperature enclosure. The high dc voltage power supply, EA-PS 9500-06 T, serves as the input source $V_{in}$ of the circuit. This dc power supply supports a rated voltage of up to 500 V, with a voltage measurement accuracy of 0.5 V (less than 0.1% of the rated value), and a rated current capacity of 6 A, with a measurement accuracy of 0.012 A (less than 0.2% of the rated value). For the electronic dc load, which is connected to the output $V_{out}$, EA-EL-9360-10 DT was utilized, featuring a rated voltage measurement capacity of 360 V with an accuracy of 0.36 V (less than 0.1% of the rated value), and a current capacity of 10 A, with a measurement accuracy of 0.02 A (less than 0.2% of the rated value). Based on this setup, the input and output power can be directly measured using the power supply and the electronic dc load, allowing for the calculation of the efficiency. The oscilloscope, connected with current/voltage probes, is employed to monitor key waveforms. The low voltage power supply is utilized to energize the drive circuit for the MOSFET.

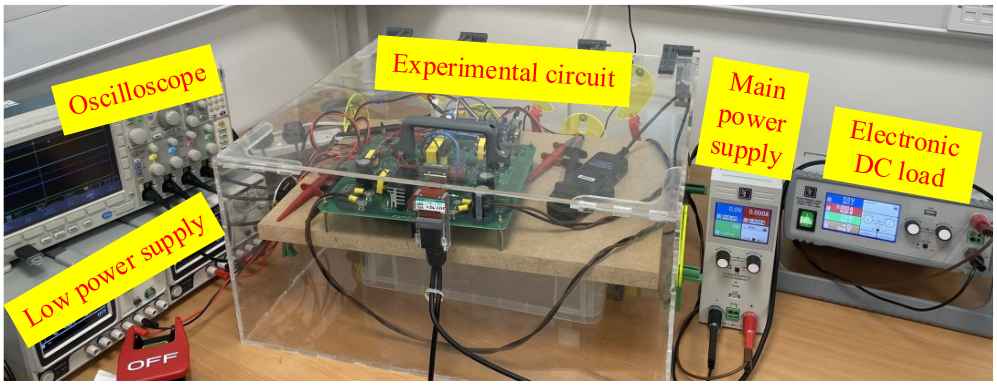



Figure 4.20 The experimental platform arrangement.

The photograph of the prototype circuit is presented in Figure 4.21, with the corresponding components details in Table 4.3. The main circuit is divided into two sections: the upper part constitutes the drive circuit, while the lower part comprises the power circuit. The low voltage power supply shown in Figure 4.20 is utilized to energize the drive circuit, whereas the main power supply serves as the input source for the power circuit. The DSP controller based on TMS320F28335 is used to provide drive signals. From Figure 4.21, the power circuit consists of three active bridge modules, whose MOSFETS are inserted above or below the board with separate heat sinks. The design of the active bridge modules follows a similar approach to that described in Section 3.4.1. Their corresponding layout is similar to that of the prototype in Figure 3.20, but the connections are different, thus achieving buck-boost function. For further details on the drive circuits, refer to the schematic provided in Appendix A.

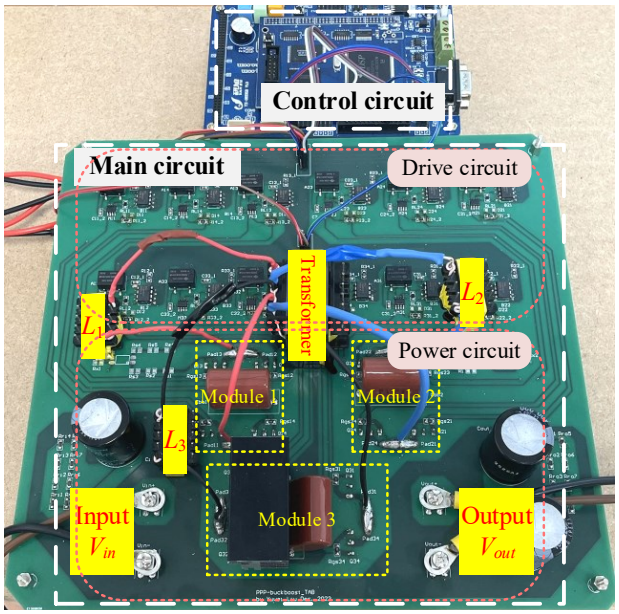



Figure 4.21 Photograph of the prototype circuit.

Table 4.3
KEY COMPONENTS LIST

| Components | Details |
|---|---|
| Switches $S_{i1}$~$S_{i4}$($i$ = 1, 2, 3) | MOSFET IPP114N12N3GXKSA1, 120 V, 75 A, 0.011Ω, N-Channel |
| Intermediate capacitors $C$ | Electrolytic Capacitor, 220 $\mu$F, 400 V |
| Transformer core | Ferrite core EE 42/21/20 |
| Transformer winding ($N_1$:$N_2$:$N_3$) | Litz wire with turns of 9:9:9 |
| Inductors $L_1$/$L_2$/$L_3$(tested) | 18/17.7/18.2 $\mu$H |
| Drive circuit | Gate drive optocoupler HCPL-4504 + MOSFET driver MAX4420 |

From Table 4.3, the three-winding transformer is constructed using a ferrite core with a size of EE42/21/20. The designation "EE" refers to the core's shape, which consists of two E-shaped halves that form a rectangular structure when assembled. The numbers 42/21/20 represent the core's width/height/depth in millimeters (mm). Litz wire is utilized for the transformer windings due to its multiple insulated strands, which ensure uniform current distribution across the cross-section, thereby reducing AC resistance and effectively minimizing the skin effect at high frequencies. In this experiment, Litz wire composed of $N$ strands of 0.1mm insulated strands is selected. For the transformer windings $N_1$/$N_2$/$N_3$, the number of strands $N$ is chosen as 100/80/40, corresponding to maximum currents of 3.5/2.82/1.41 A, respectively.

The open-loop control block diagram of the proposed PPP buck-boost dc–dc converter is illustrated in Figure 4.22. To regulate output voltage $V_{out}$, the corresponding voltages $V_{s1}$ and $V_{s2}$ are determined by selecting an appropriate intermediate voltage $V_c$($V_{p1}$). Based on these voltages, the phase shift angles $\varphi_1$ and $\varphi_2$ are calculated using equations (4.4) and (4.5). These calculated

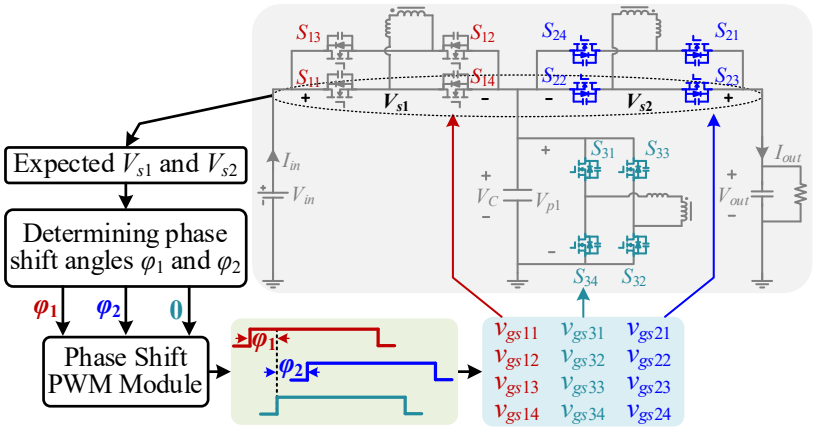



Figure 4.22 The open-loop control block diagram of the proposed PPP buck-boost dc–dc converter.

phase shift angles are then fed into the Phase Shift PWM Module, which generates the drive signals for the three active bridge modules. This Phase Shift PWM Module is implemented through the control circuit shown in Figure 4.21.

### 4.4.4 Experimental Results

The experiment is conducted according to the system parameters listed in Table 4.1. Both buck and boost modes are tested with the fixed output power of 240 W. The experimental waveforms for boost mode are shown in Figure 4.23 and Figure 4.24, while those for buck mode are presented in Figure 4.25 and Figure 4.26.

The experimental waveforms of port voltages $V_{in}$, $V_{out}$ and module voltages $V_{s1}$, $V_{s2}$ and $V_{p1}$ of $M_1$~$M_3$ in boost mode are shown in Figure 4.23. From Figure 4.23, although the input and output voltages are 120 and 130 V, respectively, the module voltages are reduced to approximately half of the port voltages. This indicates a significant reduction in voltage stress across all modules $M_1$~$M_3$. Furthermore, despite the close proximity of $V_{out}$ and $V_{in}$, which would typically result in a large voltage gain in conventional PPP buck-boost structures, the voltage gain among the three modules is maintained at roughly1:1:1 in the proposed PPP buck-boost dc–dc converter. Additionally, $V_{s2}$ is 10 V greater than $V_{s1}$, thus achieving the boost function.

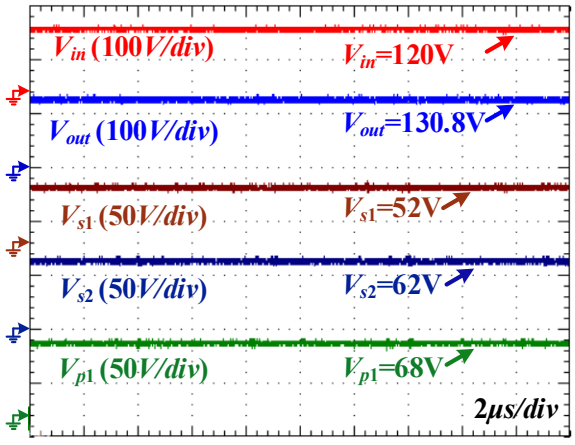



Figure 4.23 Experimental waveforms of port voltages $V_{in}$, $V_{out}$, and module voltages $V_{s1}$, $V_{s2}$ and $V_{p1}$ in boost mode.

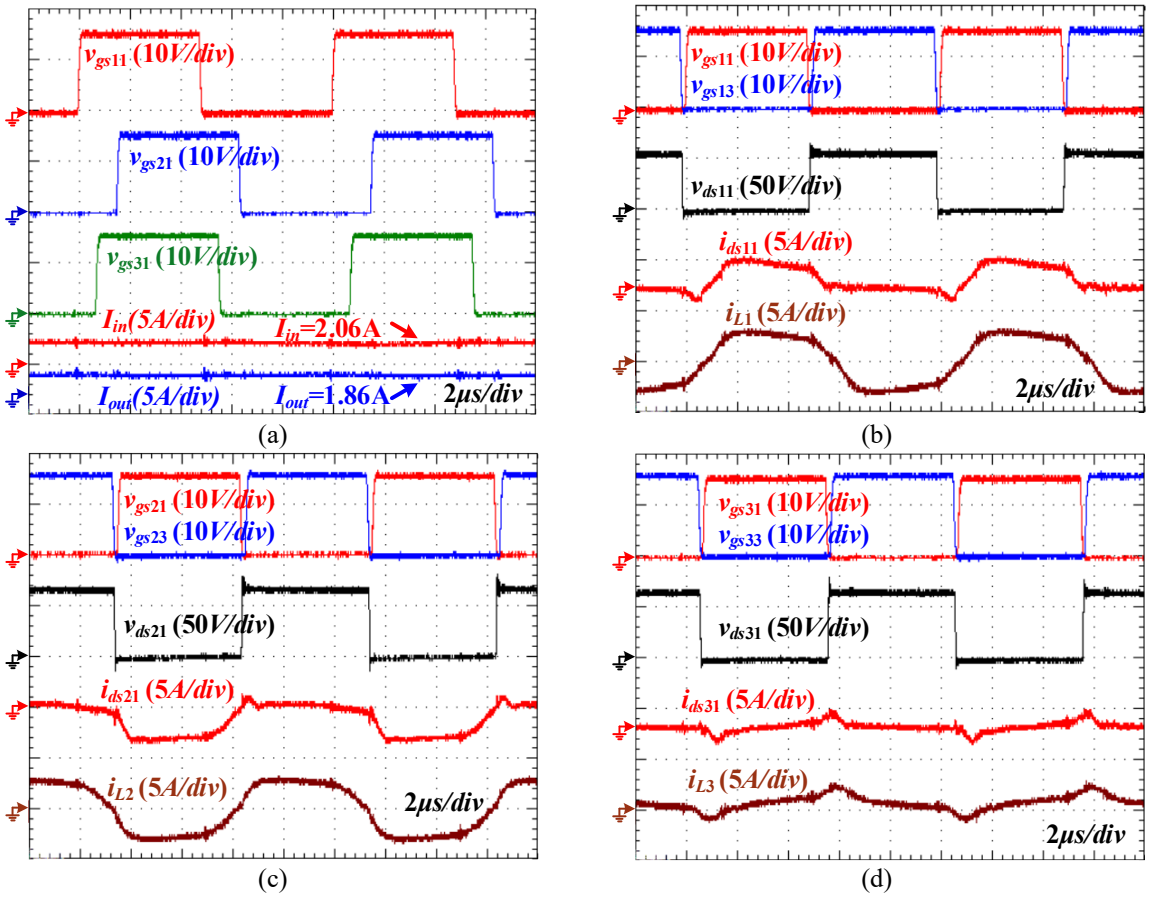



Figure 4.24 Key experimental waveforms in boost mode. (a) Drive signals $v_{gs11}$ ~ $v_{gs31}$, and port currents $I_{in}$, $I_{out}$. (b) Drive signals $v_{gs11}$ and $v_{gs13}$, drain-to-source voltage $v_{ds11}$, drain-to-source current $i_{ds11}$, and inductor current $i_{L1}$. (c) Drive signals $v_{gs21}$ and $v_{gs23}$, drain-to-source voltage $v_{ds21}$, drain-to-source current $i_{ds21}$, and inductor current $i_{L2}$. (d) Drive signals $v_{gs31}$ and $v_{gs33}$, drain-to-source voltage $v_{ds31}$, drain-to-source current $i_{ds31}$, and inductor current $i_{L3}$.

Figure 4.24 demonstrates additional key experimental waveforms in boost mode. In Figure 4.24(a), the phase shifts $\phi_1$ and $\phi_2$ are set to (−26.88°, 28.1°) to realize voltage step-up. According to the measured input current $I_{in}$ = 2.058 A and output currents $I_{out}$ = 1.858 A, the average value of the current flow through module $M_3$ can be calculated as $I_3 = I_{in} - I_{out}$ = 0.2 A, which is relatively small. According to the experimental results and the partial power expression in (4.3), the power processed by three modules is 236 W, and the total power is 480 W (sum of the ideal input and output power), which means, the partial power processing is achieved. Figure 4.24(b)~(d) demonstrate the ZVS operation of three modules. Take Figure 4.24(b) as an example, the inductor current $i_{L1}$ is negative when the drive signal $v_{gs13}$ of $S_{13}$ drops to zero. Before $v_{gs11}$ rises up, the parasitic capacitor of switch $S_{11}$ is discharged, and the corresponding drain-to-source voltage $v_{ds11}$ decreases. When $v_{ds11}$ decreases to zero, the negative inductor current $i_{L1}$ flows

through the body diode of switch $S_{11}$, clamping drain-to-source voltage $v_{ds11}$ to zero during the remaining dead time. When $v_{gs11}$ rises up, the ZVS turned ON of $S_{11}$ is achieved. Similarly, according to Figure 4.24(c) and (d), inductor currents $i_{L2,3}$ are both negative when drive signals $v_{gs23,33}$ drop, allowing the drain-to-source voltages $v_{ds21,31}$ to fall to zero before drive signals $v_{gs21,31}$ rise up. Thanks to partial power processing and soft switching, the efficiency in boost mode is measured at 98.32%. This is determined using the measured input voltage $V_{in}$ = 120.1 V, input current $I_{in}$ = 2.058 A, output voltage $V_{out}$ = 130.8 V, and output current $I_{out}$ = 1.858 A. The efficiency is calculated by dividing the output power (243.03 W) by the input power (247.17 W).

The key experimental waveforms for buck mode are shown in Figure 4.25 and Figure 4.26. In Figure 4.25, voltage step-down is achieved by regulating $V_{s2}$ to be 10 V smaller than $V_{s1}$. The intermediate voltage $V_{int}(V_p)$, is still set around 65 V, ensuring the voltage gain remains approximately 1:1:1. Therefore, the designed turns ratio of the three-winding transformer remains valid. In Figure 4.26, the phase shifts $\phi_1$ and $\phi_2$ are set to (−37.15°, 34.65°), leading to $I_{in}$ = 2.05 A, $I_{out}$ = 2.19 A. Under this load condition, the average value of the module current $I_3$ is calculated as $I_3 = I_{out} - I_{in}$ = 0.14 A, which remains relatively small. Due to the reduced voltage and current stresses, the power processed by the three modules is only 224.5 W, out of the ideal total power of 480 W. In addition, ZVS operation is also realized in buck mode. Combined with the reduced voltage and current stresses due to PPP, this leads to an efficiency of 98.17%. The efficiency is calculated based on the measured input voltage $V_{in}$ = 120.1 V, input current $I_{in}$ = 2.048 A, output voltage $V_{out}$ = 110.3 V, and output current $I_{out}$ = 2.189 A, with the output power (241.45 W) divided by the input power (245.96 W).

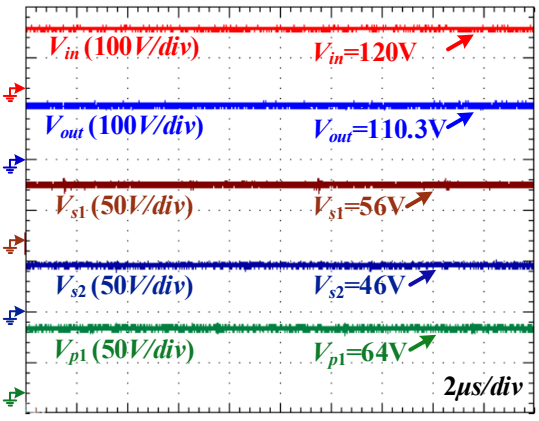



Figure 4.25 Experimental waveforms of port voltages $V_{in}$, $V_{out}$, and module voltages $V_{s1}$, $V_{s2}$ and $V_{p1}$ in buck mode.

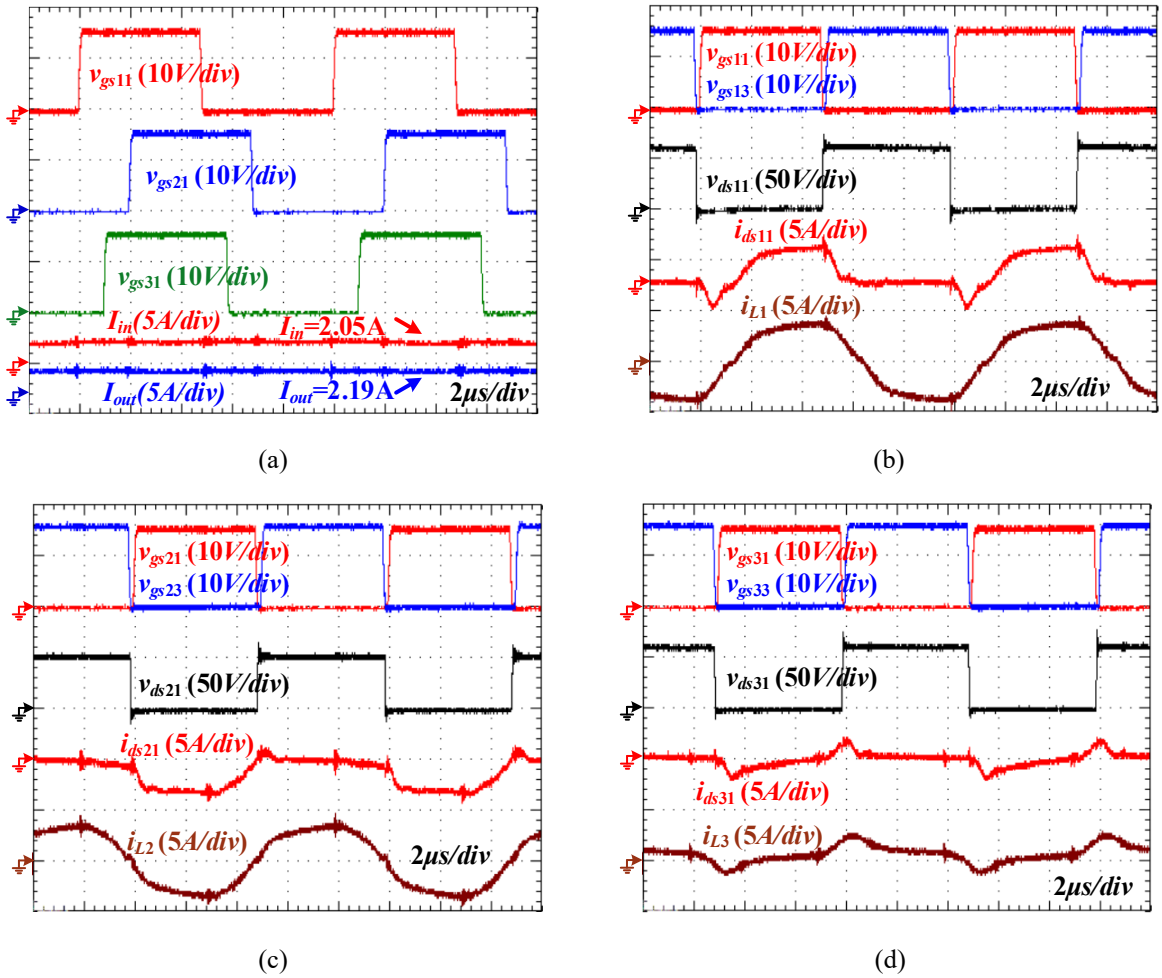



Figure 4.26 Key experimental waveforms in buck mode. (a) Drive signals $v_{gs11}$～$v_{gs31}$, and port currents $I_{in}$, $I_{out}$. (b) Drive signals $v_{gs11}$ and $v_{gs13}$, drain-to-source voltage $v_{ds11}$, drain-to-source current $i_{ds11}$, and inductor current $i_{L1}$. (c) Drive signals $v_{gs21}$ and $v_{gs23}$, drain-to-source voltage $v_{ds21}$, drain-to-source current $i_{ds21}$, and inductor current $i_{L2}$. (d) Drive signals $v_{gs31}$ and $v_{gs33}$, drain-to-source voltage $v_{ds31}$, drain-to-source current $i_{ds31}$, and inductor current $i_{L3}$.

A comparison between the simulation and experimental results reveals an interesting observation: the experimental efficiency (98.17% in buck mode and 98.32% in boost mode) is slightly higher than the simulation efficiency (97.77% in buck mode and 98.22% in boost mode). This discrepancy arises because the drain-source on-state resistance $R_{DS(on)}$ of the MOSFET IPP114N12N3GXKSA1 used in the experiment ($R_{DS(on)}$ = 0.01Ω) is lower than MOSFET IMBG120R060M1H from the SIMULINK library ($R_{DS(on)}$ = 0.06Ω). As a result, the conduction losses of the switches in the simulation are higher. Since the SIMULINK library does not provide a model for MOSFET IPP114N12N3GXKSA1, MOSFET IMBG120R060M1H was selected as a substitute to quickly simulate power loss trends rather than to estimate efficiency with high accuracy. Furthermore, both the simulation and experimental results consistently show that the

efficiency in boost mode is higher than in buck mode. This is because the current stresses $I_{dsk1,\mathrm{rms}}$ ($k$ = 1, 2, 3) shown in (4.8) are consistently lower in boost mode, leading to reduced conduction losses in both the switches and inductors, as illustrated in Table 4.2. Consequently, the simulation and experimental results exhibit the same trends, validating the consistency of the findings.

# 4.5 Conclusions

In this chapter, a novel partial power processing buck-boost dc–dc converter is proposed. It is designed to mitigate the challenges associated with wide voltage gain ranges typically encountered in existing buck-boost PPCs that utilize bi-polar modules. The proposed converter presents several key advantages:

1) Modular design: The buck-boost configuration is fundamentally derived from the modularization principles and multiport derivation concepts discussed in Chapter 2. By incorporating three modules into this architecture, the proposed converter effectively upholds the principles of partial power processing. This design not only preserves the efficiency of power conversion but also offers flexibility in implementing specific module circuits tailored to various application requirements.

2) Elimination of polarity reverser: The proposed scheme connects two series-connected modules of opposite polarity between the positive terminals of the input and output ports, with an intermediate capacitor and a parallel-connected module positioned between them, forming a T-shaped configuration. In this arrangement, the input and output voltages are determined by the sum of the intermediate capacitor voltage and the voltages of the series-connected modules. This configuration enables effective voltage regulation without requiring any changes in module polarity, thereby avoiding the higher costs, reduced performance, and switching losses associated with polarity reversal. By eliminating the need for polarity reversal, the design also avoids the inclusion of additional switches and control variables, thereby simplifying the overall control strategy. This streamlined approach enhances operational efficiency and reduces complexity.

3) Narrowed voltage gain range and reduced voltage stresses: Thanks to the T-shaped configuration of the three modules, the input and output voltages are each the sum of the intermediate voltage and the voltages of the two series-connected modules. By allowing flexible

adjustment of the intermediate voltage, the voltage gain can be maintained around a 1:1:1 ratio. As a result, the voltage gain range is significantly narrowed compared to existing buck-boost PPP converters that utilize bi-polar modules. This narrower voltage gain range facilitates design optimization, particularly during output mode transitions, resulting in improved overall performance. Furthermore, the design effectively reduces the voltage stresses on all modules to approximately half of the input/output voltage. This reduction in voltage stress not only contributes to improved system reliability but also allows for the selection of components with lower voltage ratings, enhancing both cost-effectiveness and performance.

To validate the aforementioned advantages, three active bridge modules are utilized as an example to implement the proposed PPP buck-boost structure. The system is both simulated with an output power of 240W and experimentally tested using a prototype developed specifically for this chapter.

# Chapter 5

# Conclusions and Future Work

## 5.1 What Is Accomplished

By processing only a portion of the power through a converter while delivering the remainder directly, PPP topologies offer significant advantages in reducing power losses and minimizing converter size. These features make PPP highly appealing to both academic researchers and industry practitioners. Current PPP two-port schemes provide general topologies that allow for the integration of different converters, enabling their adaptation to a variety of applications. However, relatively little research has been conducted on PPP three-port dc–dc converters, and a comprehensive general topology has yet to be developed. Additionally, the primary existing PPP buck-boost schemes, which involve polarity reversal, encounter challenges in achieving a wide voltage gain range. These limitations hinder the broader adoption of PPP in applications that require more complex architectures and diverse performance demands. To address these challenges, this thesis focuses on expanding PPP methodologies into general multiport structure and improved buck-boost schemes, with the goal of facilitating their integration into practical applications.

The key contributions of this thesis are summarized as follows:

**1) Modularized Derivation Method of the PPP Multiport DC–DC Structure**

The first major contribution of this work is the development of a modularized derivation method for general PPP three-port dc–dc topologies. This method begins by modularizing the converter used in PPP two-port structures into two isolated modules. The typical PPP two-port structure, where one port of the converter is connected in series between the source and load while another remains in parallel, is reinterpreted: one module is series-connected, and the other

is connected in parallel to either the source or load. Based on this, Chapter 2 establishes the core PPP principle: the series-connected module manages the voltage difference between the source and load, while the parallel-connected module processes the partial power arising from the current difference. This approach enables a systematic design process for PPP multiport structures by incorporating both series and parallel modules to balance voltage and current differentials across dc ports. Nine distinct PPP three-port structures were derived and thoroughly compared based on key performance indicators, such as partial power ratio, voltage gain, and current stress. These results offer valuable guidance for selecting optimal topologies under various operating conditions. Furthermore, the modular derivation principles established in this work provide a foundation for extending the PPP framework to more complex multiport systems, with potential applications in four-port, five-port, and higher-order configurations.

**2) Analysis, Design and Implementation for the Selected PPP-SIDO DC–DC Converter**

Building on the foundation of modularized PPP multiport structures, this thesis also introduces a novel PPP multiport dc–dc architecture with radial module connections, specifically designed for SIMO and MISO applications. Its connection and partial power characteristics are thoroughly analyzed. To further illustrate its operation, three active bridge modules are used as an example to replace the three isolated modules in the proposed PPP-SIDO dc – dc structure. A comprehensive analysis of the operational principles, calculations, design considerations, and experimental validation demonstrates the practical implementation of this PPP architecture. By distributing the power processing tasks between series-connected and parallel-connected modules, the proposed architecture significantly reduces voltage, current, and power stresses, enhancing both system efficiency and power density. The design was validated through the development and testing of a 2000W prototype, which exhibited low power ratings and high efficiency, confirming its practical viability.

**3) A Novel PPP Buck-Boost DC–DC Structure**

Finally, a novel PPP buck-boost dc – dc structure is proposed to address the challenges associated with wide voltage gain ranges in existing buck-boost converters that rely on polarity

reversal. The proposed converter utilizes a modular design with a T-shaped configuration that eliminates the need for polarity reversal, streamlines the control strategy, and reduces system complexity. Moreover, the T-shaped configuration also helps narrow the voltage gain range and reduce voltage stresses across the modules. The former ensures consistent converter performance, and the latter facilitates the selection of lower-voltage-rated components, further contributing to the overall efficiency and practicality of the design. To validate the design, a TAB circuit is used to implement the proposed PPP buck-boost structure, with both simulations and experiments conducted at a 240W output power.

In summary, the novel methodologies and architectures presented in this thesis provide significant advancements in the design of PPP dc–dc converters. The proposed solutions offer modularity, efficiency, and scalability, making them well-suited for a wide range of applications, from renewable energy systems to electric vehicles and industrial power distribution. Future work will involve further optimization of these designs, as well as experimental verification in more complex multiport configurations, ensuring that the principles and designs introduced here can be effectively applied to next-generation power conversion technologies.

## 5.2 Continuation of This Work

In this section, a number of recommendations for future research are proposed, building upon the findings of this dissertation. These recommendations could be pursued in the following areas:

- **Module Decoupling**

As discussed in Chapter 2, the proposed general PPP dc–dc structure the proposed PPP dc–dc structure has been extended from a two-port configuration to three or more ports, enabling broader applications in multi-port power systems. Theoretically, the number of ports can be increased by adding modules coupled through a multi-winding transformer, offering a scalable solution for complex power management.

However, this approach presents challenges. The modules share a common magnetic core, and as the number of windings grows, the complexity of energy transfer increases, leading to stronger interactions between modules. This complicates independent control, causing cross-regulation

issues and limiting autonomous control of each module. Such interdependence hinders precise power regulation, especially in systems requiring independent control of multiple sources and loads. In addition to the regulation challenges, modifying the system configuration, such as adding or removing modules, is not straightforward due to the shared transformer. This reliance on a common magnetic core makes the system less flexible and adaptable to changing requirements, thereby limiting its scalability in real-world applications.

To address these issues and enable truly independent regulation across multiple ports, decoupling the modules from one another is a critical step. Decoupling would also simplify the process of adding or removing modules, enabling the system to be more modular and scalable in practice. Therefore, future research should focus on developing techniques for module decoupling that preserve the benefits of multi-winding transformers while minimizing the complexity of inter-port energy coupling. This will be key to advancing the proposed PPP dc–dc structure for broader, more flexible applications in multiport power systems.

- **Fault Tolerance**

One of the key reasons for selecting the PPP-SIMO dc–dc converter with radial module connection is its inherent potential for fault tolerance. This capability is primarily derived from its structural design, where parallel modules are connected to a single input port. In the event of a failure in one series-connected module, which may affect the output port associated with it, the other output ports remain functional. This is made possible by the fact that each output port is equipped with an independent series-connected module, allowing the unaffected modules to continue operating, thereby enhancing the reliability of the system.

For future work, a comprehensive analysis and experimental verification of the fault tolerance capabilities of this converter should be pursued. This investigation could explore critical aspects such as module isolation and decoupling, ensuring that faults in one module do not propagate through the system. Additionally, fault management strategies and system reconfiguration techniques should be studied to maintain operational continuity during failures. The robustness of the control system will also be an essential focus, ensuring that the converter can adapt to faults and maintain stability under varying conditions. These studies would significantly advance

the practical implementation and reliability of the PPP-SIMO dc–dc converter in real-world applications.

◆ **Module Integration**

In addition to the expansion of multiport and buck-boost functionality based on PPP, another important area for future research lies in the integration of converter modules. Specifically, for the PPP-SIDO dc–dc converter presented in Chapter 3, the two series-connected modules could be integrated into a single, hybrid module, thereby reducing the number of components and associated costs. This integration can be achieved by merging Module 1 and 2, as illustrated in Figure 2.15, into a unified structure where components are shared, as shown in Figure 5.1. Such a design would streamline the system and offer economic benefits due to the lower component count. Moreover, despite the integration, the overall PPP configuration would remain unchanged, as the hybrid module continues to be connected in series between two output ports. This ensures the voltage reduction feature. Module 3 keeps parallel connection with $V_{o1}$, still processing the partial power caused by the current difference.

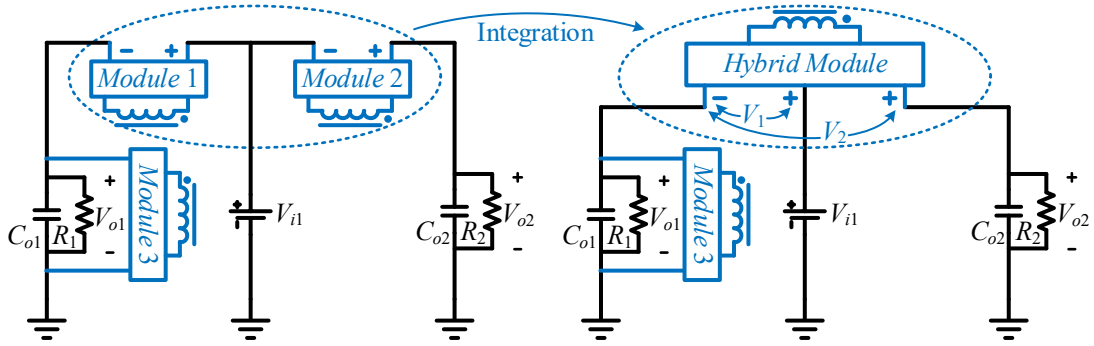



Figure 5.1 Module integration based on the selected PPP three-port dc–dc structure.

According to reference [130, 131], the bidirectional buck-boost converter and the full-bridge converter are integrated to generate a combined three-port converter, as shown in Figure 5.2. From Figure 5.2, the bidirectional buck-boost in the primary side will regulate the voltage relationship between $V_1$ and $V_2$ by employing the duty cycle $D$ of the upper switches $S_1$ and $S_3$, as shown in Figure 5.3. The phase shift angle between the phase legs $S_1S_2$ and $S_3S_4$ is kept as 180°. Then the phase voltage difference $v_{ab}$ of the phase legs $S_1S_2$ and $S_3S_4$ can be obtained in Figure 5.3. The duty cycles of the secondary side switches are fixed as 0.5, where $S_5$ and $S_8$, $S_6$

and $S_7$, are turned on in pairs, respectively, and the two pairs are activated complementarily. In addition, there is a phase shift angle $\varphi$ between the primary and secondary side, deciding the phase shift between the phase voltage differences $v_{ab}$ and $v_{cd}$. This phase shift is adopted as another control freedom to achieve voltage regulation of $V_3$, which is similar with the DAB control. In this PWM plus secondary side phase-shift control scheme, the primary power MOSFETs are shared by the bidirectional buck-boost converter and the full-bridge converter to simplify the circuit structure, which improves the power density and saves the costs.

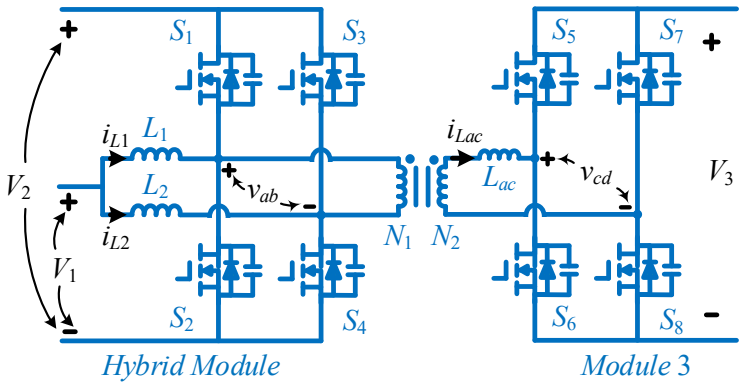



Figure 5.2 The combined three-port dc–dc converter.

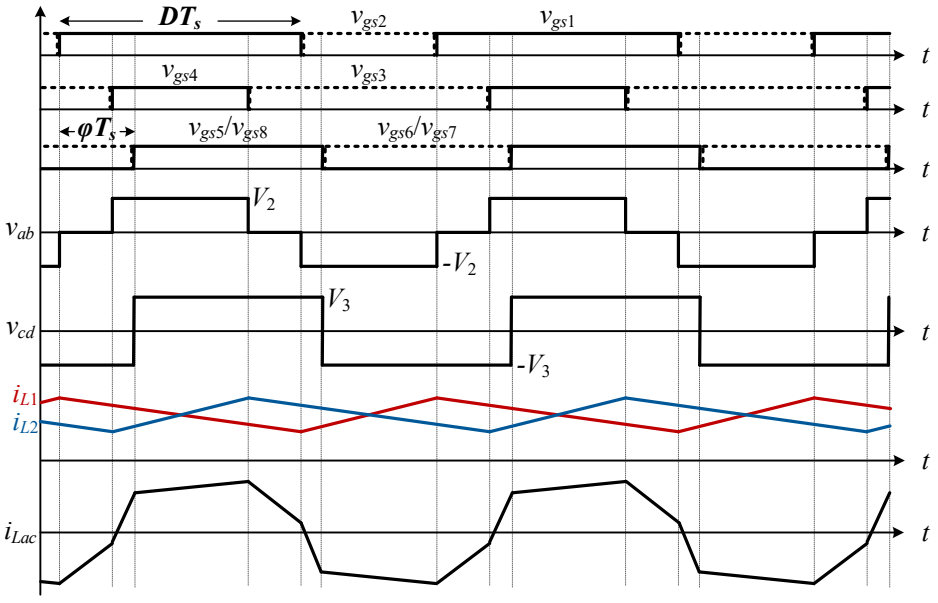



Figure 5.3 Key waveforms of the combined three-port dc–dc converter.

Combining the integrated PPP three-port dc–dc structure in Figure 5.1 with the specific three-port dc–dc converter in Figure 5.2 together, the integrated PPP three-port dc–dc converter is

derived, as shown in Figure 5.4. Compare it with the selected TAB-based PPP three-port dc–dc converter in Figure 2.15, only eight rather than twelve MOSFETs are applied after integration, which largely reduces the costs and help improve the power density.

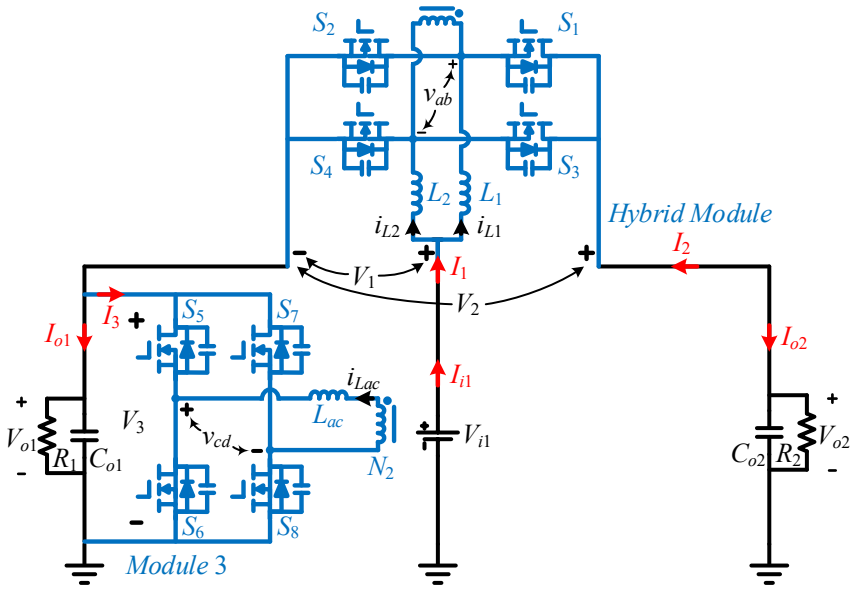



Figure 5.4 The proposed integrated PPP three-port dc–dc converter.

From Figure 5.4, the voltage and current relationships between modules and dc ports can be calculated in (5.1) and (5.2), respectively. Accordingly, the power processed by the modules $P_p$ and the total power $P_t$ can be compared, as shown in (5.3). From (5.3), the partial power $P_p$ minus the total power $P_p$ is always smaller than zero, which means $P_p$ is always smaller than $P_p$, ensuring the power reduction. Therefore, after circuit integration, PPP function is still maintained.

$$\begin{cases} V_1 = V_{i1} - V_{o1} \\ V_2 = V_{o2} - V_{o1} \\ V_3 = V_{o1} \\ V_{o1} < V_{i1} < V_{o2} \end{cases} \tag{5.1}$$

$$\begin{cases} I_1 = I_{i1} \\ I_2 = -I_{o2} \\ I_3 = I_{i1} - I_{o1} - I_{o2} \end{cases} \tag{5.2}$$

$$\begin{aligned} P_p - P_t &= \left(|V_1 I_1| + |V_2 I_2| + |V_3 I_3|\right) - \left(V_{i1} I_{i1} + V_{o1} I_{o1} + V_{o2} I_{o2}\right) \\ &= \left[\left(V_{i1} - V_{o1}\right) I_{i1} + \left(V_{o2} - V_{o1}\right) I_{o2} + V_{o1} \left|I_{i1} - I_{o1} - I_{o2}\right|\right] - \left(V_{i1} I_{i1} + V_{o1} I_{o1} + V_{o2} I_{o2}\right) \\ &= V_{o1}\left[\left|I_{i1} - I_{o1} - I_{o2}\right| - \left(I_{i1} + I_{o1} + I_{o2}\right)\right] < 0 \end{aligned} \tag{5.3}$$

For the future continuation of this research, it is essential to perform further in-depth calculations and comprehensive analyses to validate the proposed theoretical models and establish an experimental prototype. Specifically, one area that warrants significant exploration is the potential efficiency improvements resulting from the integration of the proposed PPP three-port dc–dc converter in Figure 5.4. While this work has demonstrated cost savings due to the reduction in the number of components, the author seeks to further investigate whether this integration will lead to an overall improvement in efficiency when compared to the non-integrated converter architecture, as presented in Chapter 3.

Future work should therefore not only focus on optimizing the converter's performance metrics but also on understanding the trade-offs between integration and non-integration, considering factors such as operating conditions, reliability and design flexibility. The exploration of these aspects will contribute to a more comprehensive understanding of the feasibility and practicality of the integrated PPP three-port converter for various industrial applications, further advancing the state of the art in dc–dc converter design.

# Acronyms

| | |
|---|---|
| **CI** | Coupled Inductor |
| **DAB** | Dual Active Bridge |
| **DPP** | Differential Power Processing |
| **EV** | Electric Vehicle |
| **FPC** | Full Power Converter |
| **FPP** | Full Power Processing |
| **IPOS** | Input-Parallel Output-Series |
| **ISOP** | Input-Series Output-Parallel |
| **MISO** | Multi-Input Single-Output |
| **MPPT** | Maximum Power Point Tracking |
| **PPP** | Partial Power Processing |
| **PPC** | Partial Power Converter |
| **PV** | Photovoltaic |
| **RMS** | Root Mean Square |
| **SIDO** | Single-Input Dual-Output |
| **SIMO** | Single-Input Multi-Output |
| **TAB** | Triple Active Bridge |
| **ZVS** | Zero-Voltage-Switching |

# Appendix A

The schematic diagrams of the PCB layout for the proposed TAB-based PPP-SIDO dc–dc converter in Section 3.4 and the TAB-based PPP buck-boost dc–dc converter in Section 4.4 are presented below:

For the proposed TAB-based PPP-SIDO dc–dc converter, Figure A. 1 illustrates the voltage sampling circuit for both output voltages, $V_{o1}$ and $V_{o2}$, connected to the DSP controller. Figure A. 2 shows the drive circuit for switch $S_{11}$, with a total of twelve such circuits used in the TAB configuration. Figure A. 3 depicts the connection of the proposed TAB-based PPP-SIDO dc–dc converter, utilizing three active bridges configured in a PPP arrangement.

For the TAB-based PPP buck-boost dc–dc converter, the drive circuit is similar to that shown in Figure A. 2. Its main power circuit is shown in Figure A. 4.

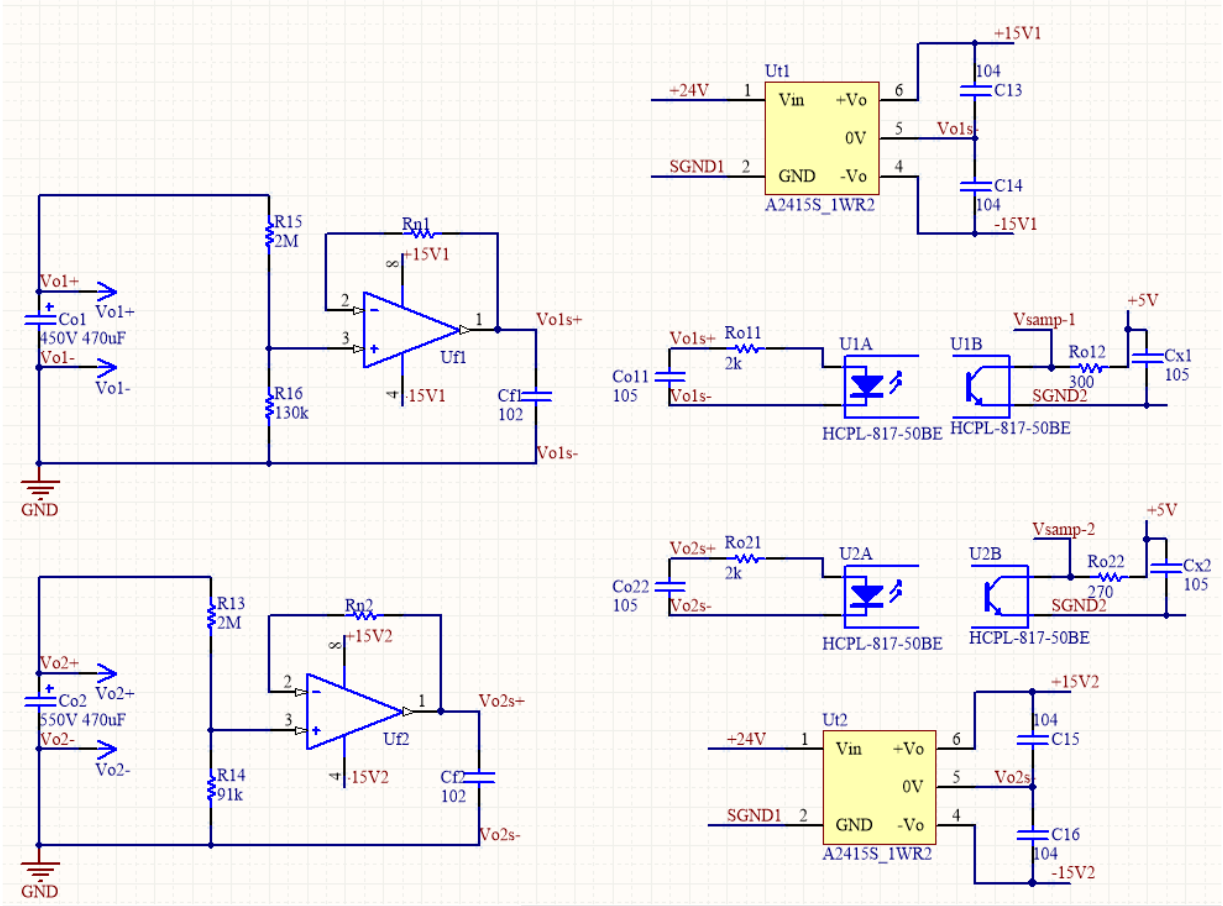



Figure A. 1 Schematic diagram of the voltage sampling circuit for two outputs.

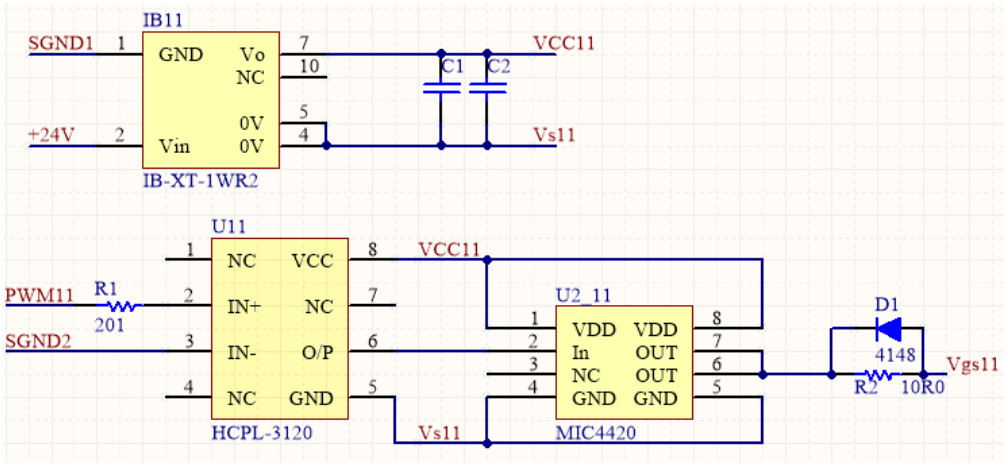



Figure A. 2 Schematic diagram of driver circuit for switch $S_{11}$.

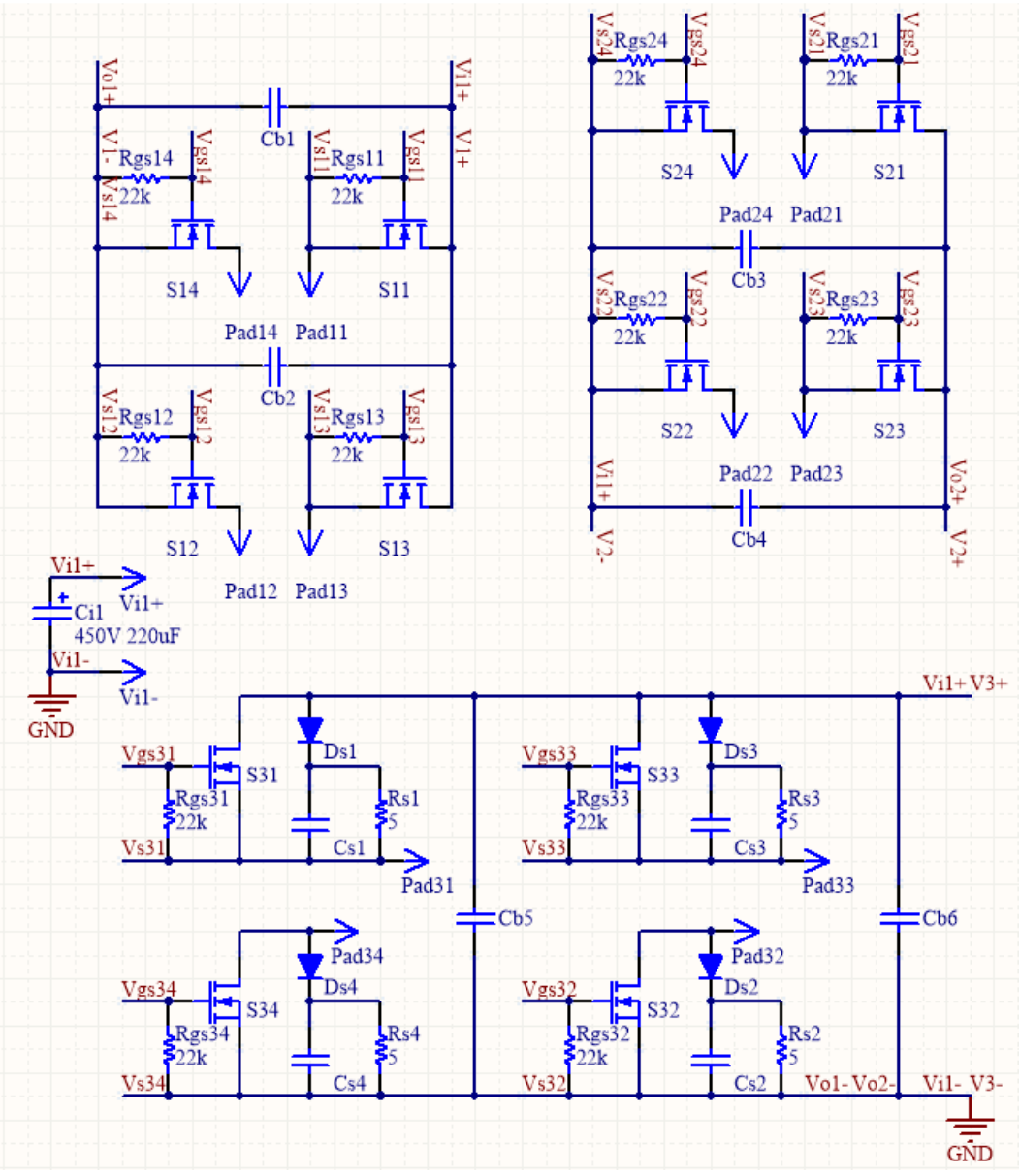



Figure A. 3 Schematic diagram of the TAB-based PPP-SIDO dc–dc converter.

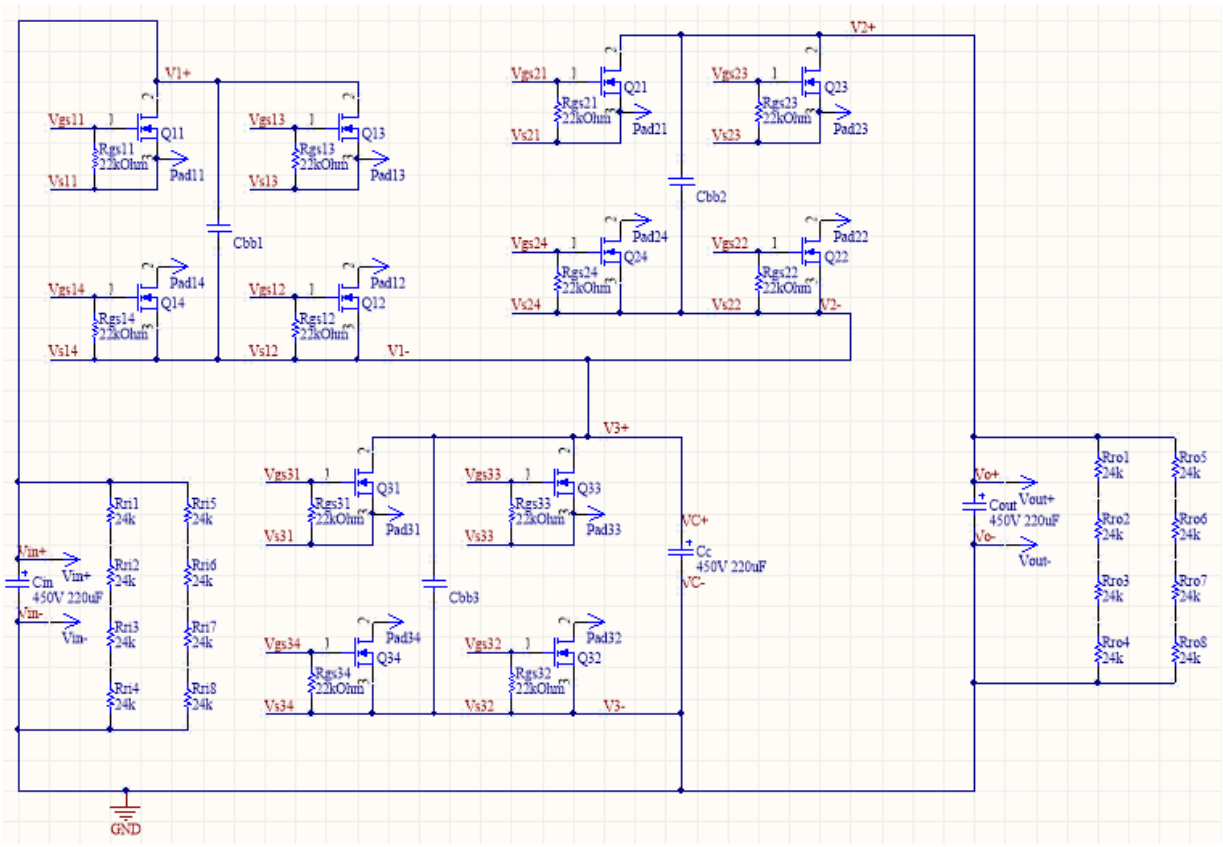



Figure A. 4 Schematic diagram of the TAB-based PPP buck-boost dc–dc converter.

# Appendix B

The functional code blocks for the proposed TAB-based PPP-SIDO dc–dc converter in Section 3.4 are illustrated below:

### (1) PI Controller

```
% Initialize parameters:
Sample1=0;
Sample2=0;
eo1=0;
eo11=0;
eo2=0;
eo21=0;
vo1=0;
vo2=0;
kp1=0.1;
ki1=0.001;
kp2=0.1;
ki2=0.001;

}
interrupt void ISREPwm1_Zero(void)
{
vref1=10.35;
vref2=10.32;
Sample1=((AdcRegs.ADCRESULT0)>>4);
Sample2=((AdcRegs.ADCRESULT1)>>4);

samp_v1=0.000736*(float)(Sample1);
samp_v2=0.000736*(float)(Sample2);

% Map the sampled actual values to the theoretical values:
vo1=(4.93-samp_v1)*910/(270*1.1)+1.145;
vo2=(4.93-samp_v2)*910/(270*1.1)+1.145;

% Formulate the PI control logic:
eo1=vref1-vo1;
if (eo1>1)
{
```

```
eo1=1;
}
if (eo1<-1)
{
eo1=-1;
}
deltae1=eo1-eo11;

eo2=vo2-vref2;
if (eo2>1)
{
eo2=1;
}
if (eo2<-1)
{
eo2=-1;
}
deltae2=eo2-eo21;

u1=kp1*deltae1+ki1*eo1+u11;
u2=kp2*deltae2+ki2*eo2+u21;

% Limit the range of the control values:
if (u1>70)
{
u1=70;
}
if (u1<50)
{
u1=50;
}

if (u2>40)
{
u2=40;
}
if (u2<25)
{
u2=25;
}

u11=u1;
eo11=eo1;
u21=u2;
```

```
eo21=eo2;

f11=u1;
f12=u2;

% Map the output values to the PWM phase shift angles:
if (f11>0)
{
F11=EPWM_PERIOD*(1-(f11/360));
}
else
{
F11=EPWM_PERIOD*(-f11/360);
}

if (f12>0)
{
F12=EPWM_PERIOD*(1-(f12/360));
}
else
{
F12=EPWM_PERIOD*(-f12/360);
}

EPwm1Regs.TBPHS.half.TBPHS = 0;
EPwm2Regs.TBPHS.half.TBPHS = F11;
EPwm3Regs.TBPHS.half.TBPHS = F12;

EPwm1Regs.CMPA.half.CMPA = 750;
EPwm1Regs.CMPB = 750;
EPwm2Regs.CMPA.half.CMPA = 750;
EPwm2Regs.CMPB = 750;
EPwm3Regs.CMPA.half.CMPA = 750;
EPwm3Regs.CMPB = 750;
```

### (2) PWM Generation Module

```
InitEPwm1Gpio()
EPwm1Regs.TBPRD = EPWM_PERIOD;
EPwm1Regs.TBPHS.half.TBPHS = 0;
EPwm1Regs.TBCTR = 0x0000;

EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;
EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;
```

```
EPwm1Regs.TBCTL.bit.PRDLD = TB_SHADOW;
EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;
EPwm1Regs.TBCTL.bit.SYNCOSEL = TB_CTR_ZERO;
EPwm1Regs.TBCTL.bit.PHSDIR = TB_UP;

EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
EPwm1Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;

EPwm1Regs.CMPA.half.CMPA = 500;
EPwm1Regs.CMPB = 500;
EPwm1Regs.AQCTLA.bit.ZRO=AQ_SET;
EPwm1Regs.AQCTLA.bit.CAU=AQ_CLEAR;
EPwm1Regs.AQCTLB.bit.ZRO=AQ_CLEAR;
EPwm1Regs.AQCTLB.bit.CBU=AQ_SET;

EPwm1Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
EPwm1Regs.DBCTL.bit.POLSEL =DB_ACTV_HIC;
EPwm1Regs.DBCTL.bit.IN_MODE = DBA_ALL;
EPwm1Regs.DBRED = 25.1;
EPwm1Regs.DBFED = 25.1;

InitEPwm2Gpio();
EPwm2Regs.TBPRD = EPWM_PERIOD;
EPwm2Regs.TBPHS.half.TBPHS = 0;
EPwm2Regs.TBCTR = 0x0000;

EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;
EPwm2Regs.TBCTL.bit.PHSEN = TB_ENABLE;
EPwm2Regs.TBCTL.bit.PRDLD = TB_SHADOW;
EPwm2Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
EPwm2Regs.TBCTL.bit.CLKDIV = TB_DIV1;
EPwm2Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN
EPwm2Regs.TBCTL.bit.PHSDIR = TB_UP;

EPwm2Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm2Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
EPwm2Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
EPwm2Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;

EPwm2Regs.CMPA.half.CMPA =500;
EPwm2Regs.CMPB =500;
```

```
EPwm2Regs.AQCTLA.bit.ZRO=AQ_SET;
EPwm2Regs.AQCTLA.bit.CAU=AQ_CLEAR;
EPwm2Regs.AQCTLB.bit.ZRO=AQ_CLEAR;
EPwm2Regs.AQCTLB.bit.CBU=AQ_SET;

EPwm2Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
EPwm2Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
EPwm2Regs.DBCTL.bit.IN_MODE = DBA_ALL;
EPwm2Regs.DBRED = 25.1;
EPwm2Regs.DBFED = 25.1;

InitEPwm3Gpio();
EPwm3Regs.TBPRD = EPWM_PERIOD;
EPwm3Regs.TBPHS.half.TBPHS = 915;
EPwm3Regs.TBCTR = 0x0000;

EPwm3Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;
EPwm3Regs.TBCTL.bit.PHSEN = TB_ENABLE;
EPwm3Regs.TBCTL.bit.PRDLD = TB_SHADOW;
EPwm3Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
EPwm3Regs.TBCTL.bit.CLKDIV = TB_DIV1;
EPwm3Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;
 EPwm3Regs.TBCTL.bit.PHSDIR = TB_UP;

EPwm3Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm3Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
 EPwm3Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
EPwm3Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;

EPwm3Regs.CMPA.half.CMPA =500;
EPwm3Regs.CMPB =500;
EPwm3Regs.AQCTLA.bit.ZRO=AQ_SET;
EPwm3Regs.AQCTLA.bit.CAU=AQ_CLEAR;
EPwm3Regs.AQCTLB.bit.ZRO=AQ_CLEAR;
EPwm3Regs.AQCTLB.bit.CBU=AQ_SET;

EPwm3Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
EPwm3Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
EPwm3Regs.DBCTL.bit.IN_MODE = DBA_ALL;
EPwm3Regs.DBRED = 25.1
EPwm3Regs.DBFED = 25.1
```

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