University of Sheffield

IntegraBrain – A Multi-modal Neural Interface for the Detection and Suppression of Focal Epilepsy.

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Abstract

Focal cooling has been demonstrated as a promising treatment strategy for patients with medically intractable epilepsy. Cooling actuation is achieved via an invasive interface positioned in direct contact with neural tissue of the epileptic foci. Seizure suppression by focal cooling has been demonstrated extensively. However, pre-clinical proof-of-concept systems that have been produce thus far are too bulky and mechanically stiff. Long-term implantation of these devices would risk inducing significant compression injury and localised glial scaring over time.

In this thesis presents the efforts to assemble a miniaturised, multimodal interface that is capable of simultaneously performing electrocorticography (ECoG) recording, temperature monitoring and focal cooling. Comprising of a solid-state thermoelectric element, a microfluidic heat management system, integrated thermocouples, ECoG electrodes and supporting electronic circuitry, a systemic implementation approach was used to produce a tightly integrated system.

The Interface consists of discreate electronic components embedded in a mechanically soft matrix with the dimensions 9.5 x 9.5 x 2.5mm. This is realised through the leveraging of direct ink writing (3D printing) biocompatible silicones and electrically conductive Graphite-PDMS composites. Integration of composite electrodes allows for ECoG sensing whilst maintain device softness.

In Vitro interface systems verification was conducted using hydrogel-based neural tissue thermal models. At the interface-model tissue boundary, rapid cooling rates of ~3°Cs^{-1} were achieved during 14°C ΔT cooling runs. System power consumption is recorded to peak at 7.84W on cooling start and 2.6W during steady state of a 15°C ΔT cooling run. System maturation presented the opportunity to conduct acute *In Vivo* animal studies using the 4-AP seizure model. Initial data collected demonstrate reliable cortical tissue cooling down to 18°C. Comparison of nominal seizure recordings to those during active cooling indicate successful seizure suppression with seizure activity suppression increasing as cooling temperature decreases. A ~67% reduction in broadband seizure magnitude (0-30Hz) was recorded when cooling to 18°C.

Work presented here represents an evolution in focal cooling interface design beyond the existing solutions and a step towards a clinically viable device for patients.

Declaration

I, Spencer Ryan Moore, hereby declare that the works presented within this thesis are entirely produced by myself. Any work not original to this thesis its attributed to its author. The In Vivo work presented in Chapter 6 was undertaken in collaboration with Dr Jason Berwick, Dr Thomas Paterson, Naomi King.

In memory of family that passed during this PhD
Samantha
Auntie Faye
Uncle Gerry

Curious to no end and soon turned
To ponder distant Stars at night

We dream of reaching new worlds
Together we toil to take flight

A future that’s soon to be unfurled
Beyond the speed of light

TWRP

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Embarking on a PhD is never an easy quest but starting this one in February 2020 certainly made it an interesting one. With lockdowns a plenty and then Ukrainian invasion threatening access to a crucial Interface component, and then being diagnosed with ADHD in 2023 – there was never a dull moment.

The largest thank you is warranted for my supervisor - Prof Ivan Minev. Your guidance and support over the past 4 years has been central in allowing me to take on this project and take my first steps along the research career path. I'm forever grateful for you being quick to respond to a random student's email asking for advice in relation to an expired PhD advert.

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List of Abbreviations

3D	Three Dimensional
4-AP	4-Aminopyridine
ADC	Analogue to Digital Converter
AED	Anti-Epileptic Drug
AMRC	Advance Manufacturing Research Centre
ASIC	Application-Specific Integrated Circuit
C	Capacitor
CAD	Computer Aided Design
CMRR	Common-Mode Rejection Ratio
COM	Communication
COP	Coefficient of Performance
COTS	Commercial-Off-The-Shelf
CS	Chip Select
CSF	Cerebrospinal Fluid
DAC	Digital to Analogue Converter
DAQ	Data Acquisition
DBS	Deep Brain Stimulation
ΔT	Temperature Differential
DFP	Device Firmware Package
DIW	Direct Ink Writing
DMA	Direct Memory Access
DSP	Digital Signal Processing
ECoG	Electrocorticography
EDA	Electronic Design Automation
EEG	Electroencephalogram
EMF	Electromotive Force
EMG	Electromyography
EMI	Electromagnetic Interference
FBC	Focal Brain Cooling
FEM	Finite Element Modelling
FIFO	First In First Out
FPU	Floating Point Unit
FS	Full Speed
FSR	Full Scale Range
G-PDMS	Graphite PDMS Composite
GUI	Graphical User Interface
HAL	Hardware Abstraction Layer
HMI	Human Machine Interface
Hz	Hertz
I_{tec}	TEC Current

IC	Integrated Circuit
ID	Inner Diameter
IDE	Integrated Development Environment
ILAE	International League Against Epilepsy
In-amp	Instrumentation Amplifier
IO	Input/Output
ISR	Interrupt Service Routine
JTAG	Joint Test Action Group
kB	Kilo Byte
L	Inductor
LDO	Low-dropout
LFP	Local Field Potential
LT	Linear Technology
LSB	Least Significate Bit
LVTTL	Low Voltage Transistor-Transistor Logic
MB	Mega Byte
Mbps	Megabits per second
μC	Microcontroller
min	Minutes
MISO	Main In/Sub Out
MOSI	Main Out/Sub In
MPa	Megapascals
MPS	Monolithic Power Systems
MRI	Magnetic Resonance Imaging
MSI	Multi-Speed Internal
Mux	Multiplexer
NICE	National Institute for Health and Care Excellence
NN	Neural Network
NTC	Negative Temperature Coefficient
NVIC	Nested Vectored Interrupt Controller
OD	Outer Diameter
Op-amp	Operational Amplifier
PBF	Powder Bed Fusion
PBS	Phosphate-buffered solution
PC	Personal Computer
PCB	Printed Circuit Board
PDMS	Polydimethylsiloxane
PID	Proportional Integral Differential
PLA	Polylactic Acid
PLL	Phase-Lock Loop
PSD	Power Spectral Density
PSM	Printer Slide Mount
PSRR	Power Supply Rejection Ratio
PTC	Positive Temperature Coefficient
PWM	Pulse Width Modulation

R	Resistor
R_{sense}	Current Sense Resistor
RNS	Responsive Neurostimulation
RTD	Resistant Temperature Detector
Rx	Receive Line
s, sec	Seconds
SCK	Serial Clock
SCL	Serial Clock Line
SDA	Serial Data Line
SPI	Serial Peripheral Interface
ST	STMicroelectronics
SWD	Serial Wire Debug
TBI	Traumatic Brain Injury
TEC	Thermoelectric Cooler
THT	Through-hole
TI	Texas Instruments Inc
Tx	Transmit Line
UART	Universal Asynchronous Receiver/Transmitter
USART	Universal Synchronous Asynchronous Receiver Transmitter
VI	Virtual Instrument
VNS	Vagus Nerve Stimulation
wt%	Percentage by Mass

Chapter 1

Introduction

Effecting more than 50 million people worldwide, epilepsy is a neurological condition that can present highly invasive symptoms during a patient's life [1]. The first route for seizure prevention is anti-epileptic drugs (AEDs). However, one-third of patients demonstrate a partial or complete resistance to pharmacological treatment options. This is seen to persist even with the introduction of new AEDs [2, 3].

Alternative clinical treatment strategies for intractable epilepsy are available to patients. These include surgical intervention [4, 5], vagus nerve stimulation (VNS) [6, 7], deep brain stimulation (DBS) [8, 9], or responsive neurostimulation (RNS) [10, 11]. Whilst the treatments stated have found clinical success, follow up studies involving patient groups have shown the efficacy of seizure occurrence reduction to vary within treatment groups [12].

Jane de Tisi et al estimate that 54% of patients that had surgery remained seizure free after 5 years - with this reducing to 47% after 10 years [4]. Likewise, Skrehot, Englot and Haneef's meta-analysis of electrical stimulation-based treatments indicates that the highest mean seizure reduction efficacy of these treatments - achieved with RNS implants - to be ~73% 3 years post-implantation [13]. Adverse effects from stimulation therapies have also been reported from patients which include headaches, depression, and memory impairment [7, 8, 14, 15].

The search then remains for new treatment strategies that is able provide ongoing relief for patients from epileptic seizures. In that endeavour, alternative neuromodulation modalities are now being explored. Focal cooling is one such neuromodulation technique that is being presented as a viable option for clinical deployment.

Use of cooling as a medical therapy has begun to find traction over the past two decades. Groups have been exploring its utilisation in the management of chronic pain and its use as a neuroprotective agent in ischemic events or after traumatic brain injuries [16, 17, 18, 19, 20]. For the suppression of epileptiform activity, focal brain cooling (FBC) has continued to show promise for clinical translation with consistent therapeutic responses across multiple animal and seizure models [21, 22, 23, 24, 25].

Focal cooling is hypothesised to be a multi-action therapy when applied to neural tissue experiencing epileptiform activity. The act of cooling is described to disrupt the neural network synchrony necessary for epileptiform activity to develop, cause a reduction in spike frequency due to the delayed depolarisation of neurons, and suppress the release of excitatory and inhibitory neurotransmitters [26, 27, 28, 29, 30]. These actions, alongside the highly localised nature of focal cooling, provides for a targeted and transient therapy action that is inherently non-destructive [31, 32].

With the miniaturisation of electronic devices alongside the availability of small, energy dense batteries, the technological conditions are suitable for the clinical translation of focal cooling therapies. Groups across the globe have proposed devices to achieve this clinical leap – though none have achieved thus far. It is concluded that these proposed systems are currently too large; constructed from mechanically non-compliant materials; and are designed with the focal cooling's application being reliant on the patient's discretion or 'open-loop'. This project's focus will be on addressing these areas that hinder the realisation of chronic focal cooling devices within the clinical environment.

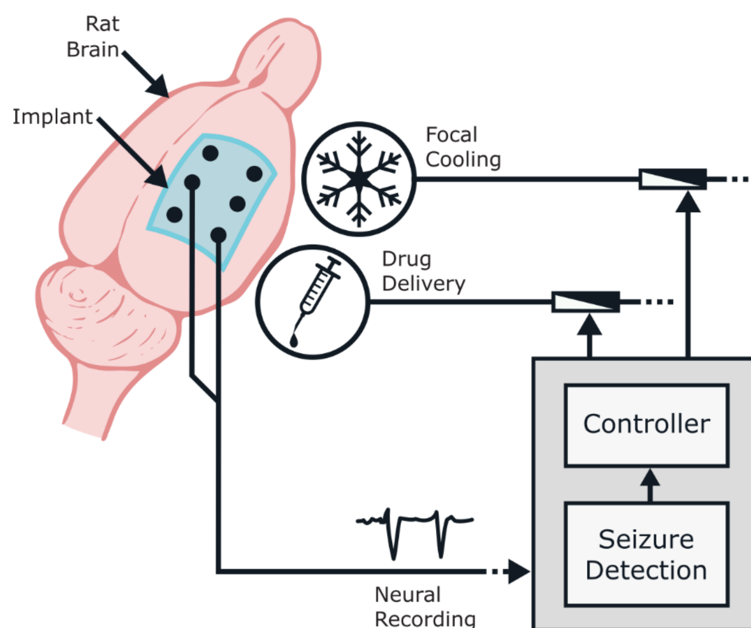

Figure 1.1 System concept for the multi-modal implantable system.
Output consists of the interface that integrates focal cooling, drug delivery, and neural recording onto a single device. External to the interface is the support hardware that monitors and actuates the various modalities upon detection of seizure activity.

1.1 Project Aim & Objectives

This research's aim is to produce a soft, multimodal interface that will have the capability to monitor neural activity for seizure events and utilise focal cooling as its primary actuation in suppressing the seizure activity. A systemic approach will be taken in the implementation of the interface and its support hardware (Figure 1.1). This should result in a highly integrated suite of electronic systems, embedded firmware, and interface hardware. The objectives of this projects work are then focused on the follow four area:

- Leverage 3-Dimentional (3D) printing technologies to produce an implantable and modular platform that can host multiple treatment modalities. Printable silicone inks will be used to form the bulk material of these interfaces to enable soft and flexible designs.

- Implementing focal cooling as the primary treatment modality hosted on the interface. Cooling efficacy shall be determined via *In Silico* simulations and using an *In Vitro* thermal model. Cooling rate and steady-state stability metrics are to be calculated for comparison to the state-of-the-art.

- Closing the loop in seizure detection and suppression by designing the device firmware to host a seizure detection algorithm to allow for the hands-free and real-time treatment of epileptic seizures. Runtime testing will confirm the viability of real-time detection for this system.

- Demonstrating the seizure suppression, actuated by the combined interface systems, within in *In Vivo* epilepsy model. Successful reduction of epileptiform activity will establish the effectiveness of the interface and support electronics. This *In Vivo* data will evidence the future clinical suitability of this system architecture.

1.2 Thesis Chapter Structure

This thesis is comprised of eight chapters that detail the work undertake for this PhD. In addition, a set of appendices are included to cover supplementary information that supports the main body of work. This introductory chapter (Chapter 1) provides an overview of the Thesis structure, motivation for conducting the research, and the working outputs of the PhD. A summary for each subsequent chapter's content is detailed as follows:

Chapter 2: Background & Literature. An exploration of the state-of-the-art in the medical application of global and focal cooling. Use of this treatment modality in the context of suppressing epilepsy will be the primary discussion focus. Technologies utilised to achieve focal cooling and integrate multi-modal treatment systems onto a single device will be examined for suitability for this research project. Other medical cooling technologies that have been investigated in the treatment of cancerous tumours, brain ischemia, and traumatic brain injuries (TBIs) will also be considered to applicability.

Chapter 3: Interface Design & Development. A chronological description of the interface evolution over the research project that results in a 3D printable, multi-modal platform that can be rapidly adapted to meet patient needs. Five major design revisions were produced. Iterations in the interface design were guided by *In Silico* finite element modelling (FEM), bench-top electrical testing, and *In Vitro* thermal tissue modelling.

3D bioprinting techniques implemented for the fabrication of the interface are covered. The bulk interface body consisted of the printable, two-part silicone - SE1700. An electrically conductive graphite-polydimethylsiloxane (PDMS) composite, specifically developed for the 3D printing process, was used in the production of the neural recording electrodes. Focal cooling was achieved through an electronics package embedded into the interface's body. It consisted of a miniature thermoelectric cooler (TEC), temperature sensors, and thermal management system.

Processes developed to reduce Interface printing error and increase process accuracy are detailed. These processes include the manual G-code alteration of the interface pathing to a custom framework, and a custom python scripts to automatically modify generated G-code to provide continuous printing.

Chapter 4: Electronic Systems for Modality Support A suite of electronic hardware is presented to support the interface function during *In Vitro* and *In Vivo* experimentation. The development process for this hardware is laid out chronologically. Prototype boards, designed around the STM32L476 Nucleo-64 board, are first described. This hardware supported interface testing during its *In Vitro* experiments.

Upon the move towards *in Vivo* verification, an investigation into the thermal management hardware was performed. Performance issues with the centrifugal pump system resulted in a redesign and the adoption of a piezoelectric air pump driven design.

To allow for tighter support hardware integration, a monolithic printed circuit board (PCB) was produced. Where made, circuit design improvements are detailed. Opportunity to migrate to a more powerful microcontroller type, STM32U585, was also taken.

Chapter 5: Embedded Firmware & Visualisation Software Details of the software developed to run on the interface support hardware and support data collection are given. Firmware, written in C99, enables the stand-alone functionality of the interface during use. Live experimental data visualisation and logging is achieved through a suite of custom LabVIEW VI's that are ran on a host personal computer (PC). These LabVIEW VIs also allow for high-level control over the interface's function during experimentation. Towards the project's end, a study was undertaken to assess the integration viability of a seizure detection algorithm into the interface support hardware's firmware. Software flow diagrams are used throughout to aid in description of the designed systems.

Chapter 6: In Vivo Verification of Focal Cooling on Epileptiform Activity. With the interface and support systems reaching an appropriate readiness level, In Vivo experimentation was undertaken to confirm seizure suppression capabilities via focal cooling. Described are the initial experimental work undertaken during this PhD. Epileptiform activity was emulated in a rat model through the perfusion of 4-Aminopyridine (4-AP). Focal cooling was achieved reliably to 18°C with the interface mounted on the rat model's brain surface. The pair of printed interface electrodes are shown to be able to reliably record the ongoing neural activity at a comparable quality to a commercial recording system. Preliminary results are presented and indicate the incited epileptiform activity being suppress by the IntegraBrain system over 60s cooling runs.

Chapter 7: Conclusion A summary of the main body of work completed over this PhD is compared to the initial aims stated in the introduction chapter. Key details and achievements are reiterated in a condensed form as a review of the research conducted.

Chapter 8: Future Works This final chapter ponders the potential future development of implantable medical devices related to the suppression of epileptiform activity. Research challenges left unanswered from this body of work will be commented upon. How these and wider field challenges on the road to a clinically viable system could be solved are discussed.

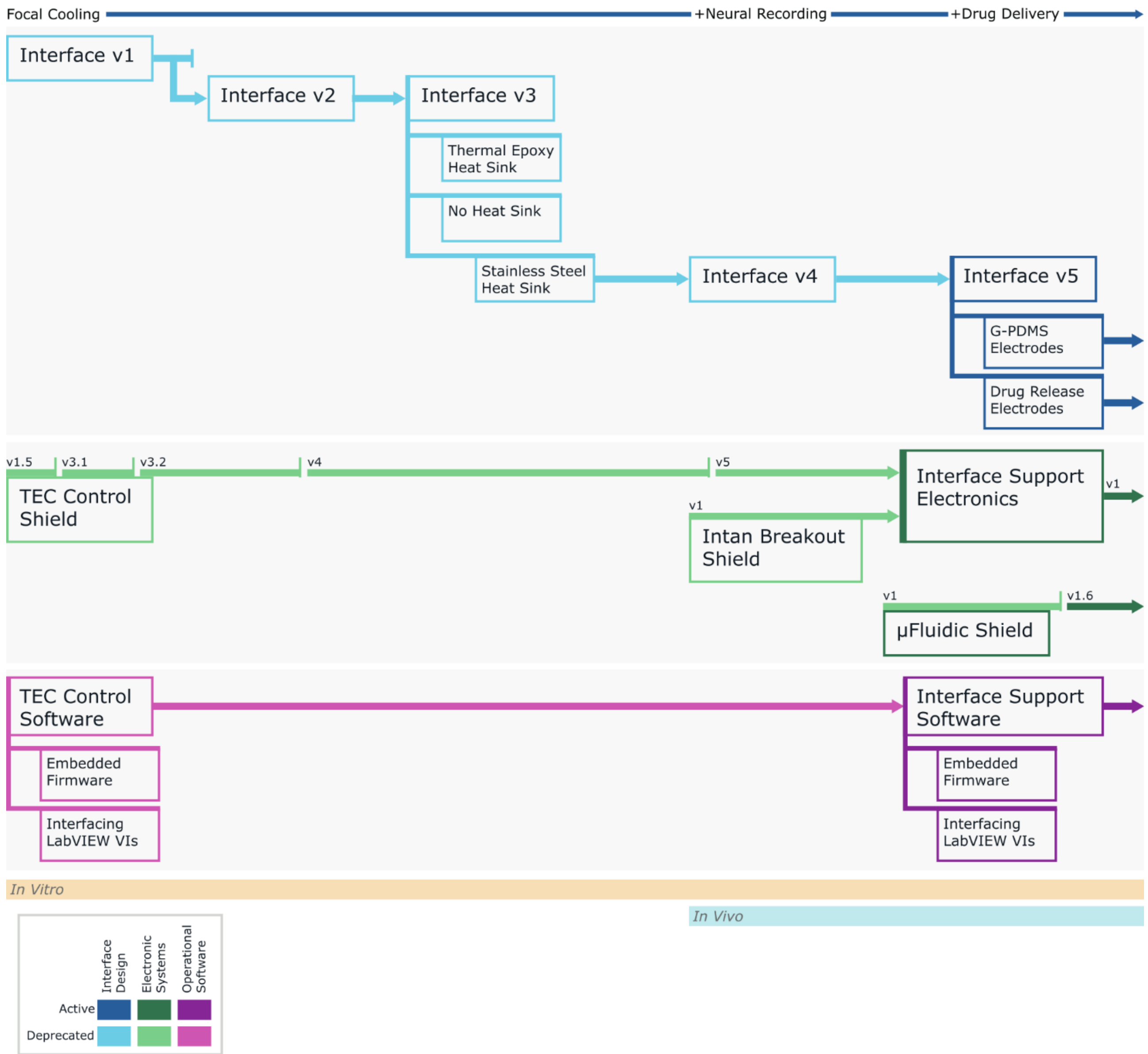

Figure 1.2 Chronological research map from this PhD.
The work is mapped relative to the modalities introduced and experimental type indicated on the top and bottom of the map respectfully. A Literature review was conducted before research was undertaken and not indicated on this map. Interface design & development is displayed in blue. Electronic hardware for Interface support is displayed in green. Embedded firmware & visualisation software is detailed in purple.

1.3 Thesis Research Map

Due to the diverse range of disciplines involved in this projects research, the chapters have been written to isolate these disciples into their broadly separate blocks. This format was constructed to aid in the readability of the research produced. Though the literature review was conducted before any experiments were performed, experimental research detailed within Chapters 3 through to 6 was undertaken in parallel with each other.

The experimental chapters work is described in a chronological order local to that chapter's work. To provide clarity in how the research in these chapter's overlay with one another, a research map is supplied (Figure 1.2). This map provides reference for the research each chapter contains in the context of the project's global chronological order.

1.4 Research Novelty

This research presents an evolution of the existing focal cooling solutions with a systematic implementation of new technologies. This evolution will provide a solution to the shortcomings in the current state-of-the-art devices presented in literature. It is within this that the research novelty exists, and the following identifies that novelty:

- Leveraging the 3D printing technology of direct ink writing (DIW), to manufacture a soft multimodal Interface using silicones and novel silicone composites. In doing so an Interface will be produced that reduced mechanically damage and glial scar tissue build up at the site of implantation.

- Systemically integrating the Interface systems to manufacture a comprehensive set of stand-alone hardware and software to support the remote function of the Interface.

- Design of the Interface should remain compact with the aim for it to fit with the intracranial space to bring the device in line with anticipated requirements for clinical translation

- Have the Interface support a multimodal approach to epilepsy seizure monitoring and suppression. The primary modality will be focal cooling alongside neural recording with the Interface then design to support future integration of local drug delivery.

- Implement an accurate and rapid focal cooling system for the quick attenuation of seizure activity. Cooling rates of >2°Cs^{-1} are desired coupled the ability to produce a minimum of 12°C temperature difference from nominal

1.5 Research Contributions

This PhD project has produced multiple opportunities to disseminate the research conducted during it. The following are those that were undertaken by this author:

1.5.1 Conferences

- S. R. Moore, "Modelling and prototyping of thermoelectric system for focal brain cooling," poster in *BioMedEng21*, Sheffield, UK, Sep. 6-7, 2021.

- S. R. Moore, "Implantable technologies for epileptic seizure detection and suppression," oral presentation in *ACSE PGR Symp.*, Sheffield, UK, Mar. 24, 2022.

- S. R. Moore, "Materials and technologies for implantable focal brain cooling system," oral presentation in *MRS Spring Meeting & Exhib.*, Honolulu, HI, USA, May. 9-13, 2022.

- S. R. Moore, "Towards an implantable focal brain cooling system for the suppression of intractable epilepsy," poster in *Cambridge Bioelectron. Symp.*, Cambridge, UK, Jun. 15-16, 2023.

1.5.2 Publications

- T.E Paterson, N. Hagis, D. Boufidis, Q. Wang, S. R. Moore, A. C. da Silva, R. L. Mitchell, J. J. Alix, and I. R. Minev, "Monitoring of hand function enabled by low complexity sensors printed on textile," *Flexible and Printed Electronics*, vol. 7, no. 3, pp. 035003, Jul 2022.

Chapter 2

Background & Literature

The International League Against Epilepsy (ILAE) defines Epilepsy as “a characteristic cluster of clinical and electroencephalographic features, often supported by specific etiological findings (structural, genetic, metabolic, immune, and infectious)” [33]. These features are further defined by the ILAE as “a transient occurrence of signs and/or symptoms due to abnormal excessive or synchronous neuronal activity in the brain” otherwise referred to as an epileptic seizure [34]. It is the duty of the health regulator within each country to adapt the ILAE guidelines and definition into practical diagnosis criteria. In the UK, the National Institute for Health and Care Excellence (NICE) recommends a combination of electroencephalogram (EEG) recordings [35, 36], neuroimaging [37, 38], and genetic testing [39, 40] is utilised as diagnostic tools to discount other seizure inducing conditions and confirm epilepsy [41, 42]. It’s during this diagnosis process that the patient’s seizure type, epilepsy syndrome, and etiology is attempted to be classified by the clinician [43, 44]. This classification has a significant impact on the range of treatment options available to the patient.

Epileptogenesis is the process during which brain structures undergo alterations so that they become capable of producing spontaneous seizure activity within patients. This alteration process is still not yet fully understood and can occur at any point within a patient’s life [45]. Etiology of epilepsy can be the result of one or more factors including genetic predisposition [[39, 46]], traumatic brain injury [47, 48], and illness [49, 50, 51]. These factors are hypothesised to cause a structural change in neural tissue that results in an imbalance between the excitatory and inhibitory activity of the tissues network [45, 52, 53, 54, 55, 56]. With it comes an increased chance of excessive, synchronised neuron firing that impacts and recruits surrounding networks.

Availability of effective treatment options to a patient can enable them to go about their lives with relative normalcy. Patients with epilepsy who been provided support to successfully manage their symptoms are reported to score their quality of life close to the level of the general population [57]. However, untreated epilepsies can lead to increase rate of injury among individuals [58] and uncontrolled seizure activity increase mortality rate [59, 60, 61, 62].

The primary treatment vector for epilepsy in AEDs. More than 20 AEDs have been certified for treating epilepsy and provides scope for tailored treatment regimens designed specific to the patient's condition [63, 64]. However, AEDs aren't a suitable option for all. Even with new AEDs being approved for clinical use, there persists a reported ~30% of patients that present drug-resistant epilepsies [2, 3, 65, 66]. An alternative – and sometimes primary – treatment option for drug resistant is surgical resections [5, 67]. Surgical treatment options involve either the removal of neural tissue or the slicing of tissue to selectively disconnect neural structures [68]. This option has found success in patient groups with 38-47% of patients estimated to remain seizure free after 10 years[4, 69]. However, this treatment option is not available to for all.

The final selection of clinically available treatment options for patients are a suite of implantable neurostimulation devices [70]. These electrotherapeutic devices provide either VNS [6, 7], DBS [8, 9], or RNS [10, 11] as a treatment strategy. Requirements for clinical approval of this class of device is a highly regulated process. As such, very few options for sourcing these devices exist. For VNS, Livanova PLC, UK produce the AspireSR and the SenTiva devices [71]. For DBS, Medtronic, USA produce the Percept PC neurostimulator [72]. For RNS, Neuropace, USA produce the RNS System [73].

Whilst the treatments stated have found clinical success, follow up studies involving patient groups have shown the efficacy of seizure occurrence reduction to vary within treatment groups [12]. Adverse effects from stimulation therapies have also been reported from patients which include headaches, depression, and memory impairment [7, 8, 14, 15].

So, what future neuromodulation therapeutics can be brought forward towards the clinical environment that could help those patients that still struggle to manage their epilepsy. Focal cooling is presented one of primary methods that could make an impact on the lives of patients with intractable epilepsy.

2.1 The Cool Side of History

Hypothermia has been a recognised method of neuromodulation since the turn of the 20th Century. These first experiments by Stefani in 1895 and Deganello in 1900 noted the rapid increase in heart rate within the canine models when cooled saline solution (25-30°C) was injected intravenously [74, 75]. Advances in cooling technology and surgical techniques came a greater understanding the application of both systemic and local hypothermia.

In 1956, Baldwin recorded a reduction in induced epileptic activity due to acute hypothermia in a primate test subject [76]. Achieved using the combination of a waterbed and icepacks, this non-invasive cooling technique reduced the primates core temperature to 25°C to investigate if hypothermia would have any effect on epileptiform activity. Subsequent researchers then used this information to further research hypothermia's effect on neural and epileptic activity. The central nervous systems tolerance to hypothermia and general effect it has on all neural tissues was demonstrated by V. H Mark and J. Siegfried using a hollow stainless-steel probe flushed with the refrigerant Freon 12 [77, 78].

Other groups sort the use of ventricular and extra-ventricular perfusion methods to produce localised brain cooling to suppress epileptic activity [79, 80, 81, 82]. It was these methods that Sourek and Travnicek emulated, in conjunction with external forced air cooling, to induce hypothermia within human subjects with intractable epilepsy. This study recorded temperatures down to 19°C on the surface of subject's brains. Results from the experiment suggested that a one-off deep hypothermia treatment could reduce long term seizure frequency and intensity [83].

Though it was deduced that hypothermia could be used as a treatment for intractable epilepsy, little was understood about its mechanisms and safety limits. Whilst cooling was used to extensively research brain function, research into FBC stalled [84]. It was Sartorius and Berger's use of FBC to terminate induced seizures, instead of antiepileptic barbiturates, during human patient brain mapping procedures, and then first demonstration of a thermoelectric cooler suppressing seizures by Hill et al around the turn of the 21st century that led to the renewed research focus into FBC therapies [85, 86].

A variety of research groups have taken up the challenge of producing a system for the treatment of intractable epilepsy. Though there has been progress made in the design of FBC systems over the past 20 years, their translation into the clinical environment has lacked progress and will be explored later.

2.2 Focal Brain Cooling

The temperature limits at which an epileptic seizure is sufficiently suppressed is the key specification for cooling system design. Yang and Rothman suggested cooling down to 20-25°C would be enough to shorten seizures, as shown in their 4-AP rat seizure model, and reduce the frequency and intensity of post-cooling seizure occurrence [87, 88]. It was in rat models with Penicillin G induced seizures that Kida et al recognised cooling to 15°C would be required to attenuate the full range of spectral powers [89].

Cooling safely below 15°C has been demonstrated by Fujii et al but it was noted that significant, but reversible, deterioration to the hosts sensorimotor function was caused by temperatures below 15°C [90]. This suggests that 15°C be the lower limit for FBC devices. Whilst it is recommended that the target temperature for FBC be 15-20°C, Motamedi et al demonstrated that seizure suppressant temperature is also closely linked to the rate of cooling. It was shown that devices with rapid cooling rates (2-5°Cs^{-1}) were required a actuate a smaller temperature drop for seizure suppression than devices with slow cooling rates (0.1-1°Cs^{-1}) [91].

FBC is also seen as potentially potent neuroprotective for patients who suffer from ischemic and traumatic brain injuries. Protection mechanisms are reported to be multi-faceted including; apoptosis prevention, reduction of neural damage from exotoxins, and the creation of favourable conditions for neural tissue repair [17, 92, 93, 94, 95]. Pre-clinical studies have also shown some successes in reducing the effects of secondary brain injuries in patients [16, 18]. Further clarification on the neuroprotective mechanisms of therapeutic hypothermia is required before this treatment can be translated into clinical practice [96, 97].

However, as opposed to cooling devices for seizure suppression, hypothermic therapies developed for the treatment of these injury types are designed to be placed externally on the body for rapid deployment in non-invasive manner [98, 99, 100]. The therapeutic temperatures these devices are designed to achieve is ≈30-34°C [100, 101, 102]. As such, the technology developed for treating TBI shall not be considered further for application to this research unless the designs present viable translation to treat intractable epilepsy.

2.3 Technologies

To induce focal cooling in the treatment for intractable epilepsy there are two mature methods commonly utilised: Liquid cooling and Peltier based cooling. Though these two systems achieve the same objective, there materials and deployment strategy diverge. Whilst both have been demonstrated as effective in providing focal cooling treatment, neither have yet made the leap to clinical deployment.

2.3.1 The True Original in Focal Cooling

Various forms of liquid cooling have been utilised in the research hypothermia therapies. Cooling is managed by the flow of a coolant over the target site where a heat exchange between the site and coolant takes place via convection and conduction - the coolant is then used to transport the excess heat away. All liquid cooling systems have the root system architecture consisting of a liquid reservoir, liquid cooling device, a pump and a heat exchanger at the epileptic focus. This cooling method can be structured in either an open loop system or a recirculating close loop system [103, 104].

Multiple materials have been employed to ensure that the heat exchanger can efficiently cool brain tissue at the focal site. For the acute experiments that Bakken et al preformed on human models, a stainless steel block with a monolithic cavity that covered a fixed circular area of 20mm diameter for cooling was used [105]. Some researchers, including Yang et al, and Clark and Colbourne, opted to use piping or medical-grade needles that could be warped into curved shapes allowing them to conform to specific cooling sites [32, 101, 106]. Whilst recently research groups have been focusing on using polymers in the construction of cooling bladders or tube-based systems whose properties are mechanically closer to the brain so as to reduce secondary injuries [103, 107, 108]. However, even with polymers having an elastic modulus closer to that of the brain, metal-based heat exchanger designs for clinical practice still persist due to polymers intrinsic thermal conductivity being low compared to metals [25, 104]. This gap in thermal conductance is being reduced through research into doping polymers with nanofibers or conductive nanoparticles [109, 110].

Most liquid systems use water or a water-based fluid including ringers or saline solution as the coolant that is cooled using a Peltier chip device. Though for some systems ethanol has been utilised as the coolant [103]. Non-water coolant systems are designed to cool the liquid using a <0°C cooling device – i.e. dry ice - thus it is required that the coolant does not freeze within the piping. This enables higher cooling rates and lower stable cooling temperature but, due to ethanol's toxicity in high concentration, use as a coolant cannot be deployed in clinical devices [111].

Liquids cooling effectiveness is primarily related to the input coolant temperature of the heat exchanger. The input temperature directly effects the cooling rate and steady-state temperature required for the system – it is used as the actuation variable when PID control is implemented [108]. Temperatures down to 0°C have been recorded in use to cool the brain, with ≈11°C 1mm being recorded below the brains surface in human patients [105]. After conducting simulations, Hata et al concluded that, although the input coolant temperature is crucial in achieving the target temperature, the heat exchanger channel design also has an effect on the temperature profile under the exchanger. The study found that a heat exchanger with a high density of internal channels produced a more homogenous cooling profile on the brains surface [112]. There is also scope to produce custom cooling patterns on the cortex surface by shaping the cooling channels within the heat exchanger.

Even with an optimised system, Hata et al and Smyth et al both recognised that heat exchange between the coolant, during transit to the heat exchanger, and atmosphere surrounding the external tubing was a problem [107, 112]. Smyth recorded the greatest coolant temperature differential of 15-20°C between the cooler and heat exchanger. They both summarised that to reduce its affects the coolant travel distance would have to be shorter and the transport piping had to be made thicker to insulate the coolant. However, this heat gain will still persist and is dependent on the local temperature surrounding the piping which in clinical practice will vary by location and time.

Cooling rates of ≈0.04 – 0.37°Cs^{-1} have been simulated and achieved experimentally but this is below what is considered 'rapid cooling' [113]. Smyth et al demonstrated that altering coolant perfusion rate directly affected the cooling rate [107]. Flow rates of liquid cooling device vary from ≈0-200ml/min and the flow rate limit is related to the material of the heat exchanger with metal based devices able to sustain higher flow rates [103, 104]. Though, even with a higher flow rate, cooling will not be instantaneous with this technology because of the perfusion dead time, and the coolant and heat exchange material specific heat difference [106].

2.3.2 Thermoelectric Cooling

A Peltier chip is a thermoelectric device that utilises the Peltier effect where a heat flux is produce at a junction between two conductively dissimilar materials when a current flows through it. Constructed out of p-type and n-type semiconductors that are connected in series and sandwiched between to ceramic plates, Peltier chips are capable of producing a heat differential between the two sides that is directly proportional to the applied DC current [114]. These cooling devices are a relatively modern development compared to other cooling methods due to the semiconductor materials required in their construction. The resultant devices are solid-state, conducive to miniaturisation and can be built to a required 2D shape [115].

One of the first uses of a Peltier chip device was recorded by Yang and Rothman in 2001 during which they were able to 'rapidly' cool the exposed sensorimotor cortex of a rat model to 20-25°C [87]. This was achieved with a pair of Peltier devices placed in series that where sized 3.5 x 3.5 x 2.4mm each. Current small size Peltier chips that measure down to 1 x 1 x 0.7mm (TEC Microsystems, Germany) can be found commercially allowing for compact and targeted focal cooling systems to be reproduced without custom tooling requirements. These could be deployed individually or in an array to cover a larger area while conforming to the surface of the brain. Alternately, large monolithic chips can be used for cooling large brain sections.

The combination of direct surface cooling and current control enable Peltier chips to have a levels of cooling control that other methods are unable to match. A common accuracy of around ±1°C the target temperature has been demonstrated [116, 117]. With a properly tuned PID controller Fujioka et al achieved an accuracy of ±0.05°C [20]. The rate of cooling is able to be controlled with ease through the current supplied to the chip. Cooling rates of up to ≈1°Cs^{-1} have been recorded in rat models [32, 116]. Greater cooling rates can be attained; however, this would require a higher DC current (>2A) being allowed. With this DC current being transported in close proximity to the brain, it poses a potential danger to the host if the wiring became exposed. Current limiting hardware are commonly employed to ensure the current is controlled and kept within safe limits [31, 89].

Commercial Peltier chips are built with materials that are non-toxic to the body thus off the shelf components can be placed in direct contact with the cortex's surface. Even so, interfacing material is commonly used to enhance or augment properties of the cooler. To increase the biocompatibility of the device, Fujii et al placed a silver interface between the cold side and the brains surface [90]. Tanaka et al focused-on cooling Temporal Lobe epilepsy whose focal point originates below the brain's surface. To target this point, a copper needle was produced that would be mounted on the cold side and inserted into the brain. Silicone surrounded the needle until the tip to maintain thermal efficiency [117]. Smyth and Rothman have also proposed heatpipe-based design for depth cooling in the brain [21]. This device allows for near instantaneous cooling of deep epileptic focal points. Shown to be an effective way of cooling sub-surface epilepsy, an array of needles or heat pipes at variable depths could be designed to allow for custom 3-dimensional cooling patterns. Though care will have to be taken with the size and insertion of the needles as to not damage the host tissue.

2.3.3 The Thermal Elephant in the Room

Though cerebral tissue can survive being cooled to 0°C without presenting irreversible histological changes, it is exceptionally sensitive to temperature increases [31]. An increase of 3-4°C above the normal core brain temperature can cause structural changes to the cerebral tissue. Due to this, thermal management is a crucial design factor for chronically implantable devices that have focal cooling elements.

The problem of thermal management is exclusive to those implants which implement a Peltier chip as their cooling device. There have been multiple systems designed to handle the excess heat generated by the hot side [20, 29, 87, 117]. Liquid cooling is the current prevalent system that is in use for implementation of Peltier systems. This system design functions similar to the direct brain liquid cooling systems. However, it differs through the placement of the heat exchanger on the hot-side of the Peltier chip and the requirement for powering two separate Peltier chips.

It was these elements that hinders the translation of this technology to clinical use as the resultant designs are generally too bulky for chronic implantation and require recharging at least once a day [112].

To solve this issue Hilderbrand has proposed the development of a flexible heat pipe solution to enable the Peltier chip to maintain a cold side temperature of approximately 20°. The system would transfer heat from the Peltier chip to a highly vascular area such as the dura, scalp or skull [21, 118]. This passive cooling method relies on the on the body's selective brain cooling ability to ensure that the heat is dissipated away from the sensitive cerebral tissue [119, 120]. A copper prototype was constructed that met the set cooling specification and was also malleable to human touch. Whilst this system is relatively flexible compared to what came before, a chronic system would require a young's modulus closer to that of brain tissue. This could be provided by a heat pipe produced with a polymer. Oshman et al have made steps that could address this problem with research into polymer-based heat pipes. They have produced pipes using liquid crystal polymer with copper filled thermal vias to decrease the thermal resistance inherent in polymers [121]. Effective at varying orientations and accelerations, this technology has the potential to be adapted for use in a chronic implant.

2.4 What else works?

Whilst thermoelectric and liquid cooling are the most mature technologies used in focal brain cooling, there are other options that have yet to be fully explored or adapted to focal cooling requirements.

2.4.1 A Passive Aggressive Focal Cooling Therapy

Passive cooling was first suggested as a method to induce mild hypothermia for the treatment of post-traumatic epilepsy by D'Ambrosio et al. The rostral parasagittal fluid percussion injury model was used to incite post-traumatic epilepsy in rat models. After which a section of the skull was removed and replaced with a steel cooling rod that made contact with the brains surface. The hypothesis was that the metal element would increase the convective and radiative losses from the brain to the surrounding environment. Over the course of the cooling, they recorded a near complete prevention of ictal activity over a 5.5 week period. Ictal activity that did occur was seen at a reduced frequency and length [23]. Only thermal imaging temperature measurements were taken over the course of this study leading to just the surface temperatures being recorded at 2°C below baseline. Depth temperatures were extrapolated for this experiment using lab data garnered from previous studies.

To understand the depth of cooling produced by passive cooling elements, Smyth et al conducted an experiment using volunteer human test subject that were undergoing epilepsy related resection surgery. A stainless-steel probe was utilised as the passive cooling element. Placed in contact with the cortex surface, temperature data was collected from the surface to a depth of 15mm at 5mm intervals. Levels of cooling at 15mm were ≈1°C with surface cooling at ≈8°C [107]. No ECoG data was collected during the passive cooling so this cooling method's effectiveness in the prevention of seizures could not be gathered.

Passive cooling is reliant on a negative temperature differential between the cortex surface and the external environment. As this type of cooling is not active, the efficiency of the device is reliant on factors outside the control of human influence (i.e. weather or atmospheres temperature). This can result in the passive element temperature increasing beyond limits that would result in cell apoptosis or necrosis.

Passive cooling works as a treatment to reduce the frequency of ictal activity occur rather than suppressing ongoing seizures. If deployed within a focal cooling system, it would have to be paired with an active cooling element to handle the suppression of seizures. However, this potential implementation of a passive cooling element is based off very limited data set. Further research would be required into the effectiveness of passive cooling in the treatment of epilepsy and how external factors affect the coolers efficiency.

2.4.2 Freeze Your Way to Focal Cooling

A cryogenic technology that has the potential to be ported over for use in focal cooling therapies is cryoablation. Cryoablation is a method of destroying tissue by reducing its temperature to below freezing. It is a common treatment used in the removal of cancerous tumours [122]. The rapid cooling within these devices is achieved by means of the Joule-Thompson effect. This effect occurs when a gas undergoes adiabatic expansion which results in a temperature drop for most gases. To achieve these temperature drops, high pressure gas is passed through a small nozzle or porous material into a chamber. This allows the gas to adiabatically expand and produce the required temperature drop to provide cooling of the chamber walls via convection and conduction. It is the pressure differential and the initial gas temperature that dictates the overall temperature drop [123].

The ability to change the cooling magnitude through input pressure control makes it a suitable candidate for adaption to focal cooling treatments. Cooling rates of 3-5.5°Cs^{-1} have been recorded in low cost cryoablator designs that substitute CO_2 for the more commonly used Argon [124]. The probes sizes of systems commercially available start at a 1.7mm diameter which make within the size range of more mature focal cooling devices which have been demonstrated in vivo [125]. With system designs that are already available, including those that incorporate compliant polymer tips on their probes, there is the potential for a research group to adapt one of these systems to assess the viability of translating this technology for focal cooling systems [126, 127].

Whilst the technology is mature and in use for tumour removal, it is not designed for chronic implantation. Multiple design questions would need to be answered before this technology could be ported over. The major question is the required pressure change to achieve the level of cooling required for FBC and how it limits the materials that can be used. This will enable an understanding into its potential for chronic implantation and the size of the support hardware. However, the work towards these questions is beyond the scope of this work.

Chapter 3

Interface Design & Development

This chapter covers the research undertaken for the development of the Implantable Interface section of the IntegraBrain system. With the aim for the Interface to host multiple modalities in a modular manner, 3D printing fabrication processes were utilised to provide design flexibility and rapid prototyping capabilities. Of these previously described modalities, focal cooling was the main consideration in the Interface design. Cooling efficacy can be highly sensitive to the local thermal environment. Controlling these thermal dependencies through Interface design is imperative in ensuring innate safety and correct function of the Interface.

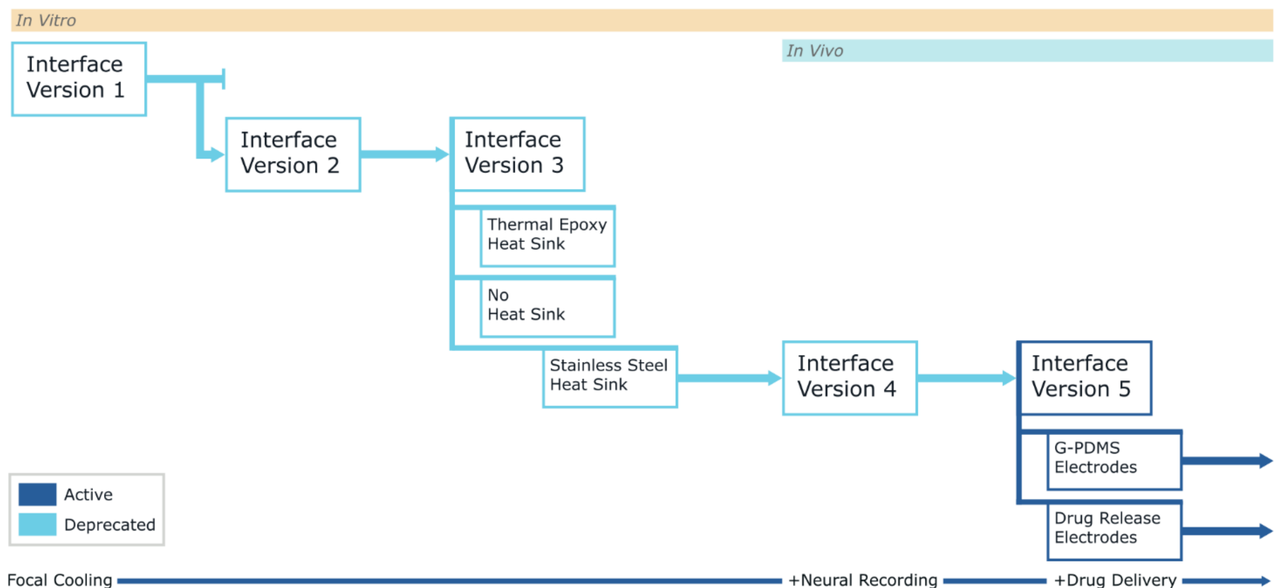

Figure 3.1 Interface design & development timeline.
Line colour indicates the Interface version design status. Experimental usage of each design is detailed at the top. Details at the bottom show at which design stage each of the modalities are added to the Interface.

The following sections will describe the iterative processes undertaken to develop the necessary fabrication processes, implement each modality, and verify Interface function. Experimentation to quantify and guide this process involved a mixture of *In Vitro* bench top testing and *In Silico* simulation. Thermal profiling and system limits were required to be understood before the Interface could be validated within an *In Vivo* epilepsy model.

In total, there were five major Interface design milestones. The research that led to each milestone is split into its own section of this chapter. Each of these sections are indicated by a chronologically ordered Interface version numbering structure (e.g. Version 1, Version 2, etc). Some Interface versions required sub-variants to be fabricated for design experimentation purposes. Figure 3.1 presents the Interface Version map with numbering order and variant naming. The purpose for each variant's name will be discussed within its respective section.

3.1 Thermoelectric Cooler

TECs are solid-state electronics devices that produce a temperature differential (ΔT) between the TEC's two opposing ceramic plates when a potential is applied across its terminals. To cause this heat pump action, the TEC exploits the Peltier effect which describes that when a current flows across the junction between two dissimilar conductors, heat energy transportation will occur at that junction (Figure 3.2). A junction's heat energy transfer rate due to the Peltier effect is given by:

$$\dot{Q} = (\Pi_A - \Pi_B) \times I \qquad 3.1$$

where I is the measured current flow from conductor A to conductor B, and Π_A and Π_B the conductors respective Peltier coefficients. It shows that heat energy transfer direction is dependent on current flow direction and the conductor junction order. This relationship provides an isolated look at the Peltier effect to understand its function. By chaining many of these junctions together, the amount of heat energy being transferred can be increased. The is how TECs exploit the Peltier effect in a usable fashion. In order to simulate a TEC other thermoelectric effect have to be considered such as joule heating, the Seebeck effect, and the Thomson effect.

In order to utilise the Peltier effect in a tangible way, the junction conductors need to have both a high electrical conductivity and a low thermal conductivity. A small group of semiconductors, including Bismuth Telluride and Silicone-Germanium, have been found to have the appropriate properties that means are able to induce the Peltier effect at a useable magnitude. The core two material properties that allow this are the semiconductors' thermally resistive internal structure and their high charge density.

Whilst using a TEC enables cooling in a compact form and opportunity for precise temperature control, a large issue with their use stems from their cooling efficiency or, more specifically, its coefficient of performance (COP) value. A TEC's COP is calculated by dividing the heat absorbed on the TEC cold-side by the input electric power to achieve this. The COP value is highly dependent on the TEC current magnitude and the ΔT between the TEC's hot and cold side. That dependency is one that is negatively correlated. Thus, it is important that the thermal environment and ΔT requirements are understood to ensure that the TEC being used will be suitable for tasks demands.

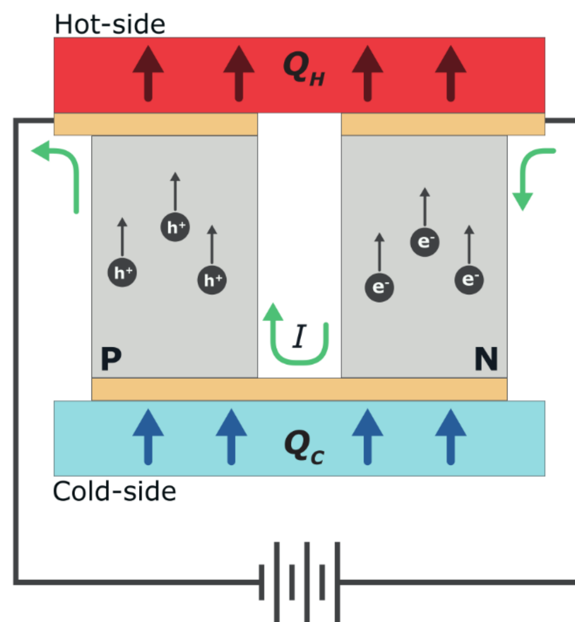

Figure 3.2 A single TEC junction functional theory.
Constructed typically from a p-type and n-type semiconductor. When a potential difference is applied across it, the current, I, flows across the junction indicated by the green arrows. The conductor's charge carriers transport heat energy from one side of the junction to the other. The absorbed heat on the 'cold-side' is given by Q_C and the dissipated heat on the 'hot-side' is given by Q_H.

3.2 TEC Hot Side Cooling

An important consideration whilst the TEC is actively cooling is the management of the pumped heat on the TECs hot-side. This heavily dictates the overall efficiency of the system and, in turn, determines how large the temperature difference a TEC can induce at in a stable way. The first step in producing the interface is to provide an adequate heat management solution for the TEC hot-side. This must be compact and of low complexity in nature for the ease of interface manufacture.

3.2.1 Thermal Modelling of Biological Systems

To determine a suitable solution, a study was undertaken to compare different potential forms of cooling the TEC hot-side. These studies were performed In Silico using the multiphysics simulation software, COMSOL 5.5 [128]. The Heat Transfer Module and the Computer Aided Design (CAD) Import Module were utilised in building the thermal model and study physics.

Pennes' Bioheat Equation

Conducting simulations that involve biological tissues involves the use of the Pennes' Bioheat equation [129]. This equation provides a framework for modelling the thermal system of any tissue, wherever it be hard or soft. It describes the combine effects that blood perfusion, tissue thermal properties and metabolic energy production has on the biological thermal system. In doing so, it creates a general model of a tissue's heat flux due to conductive and convective action occurring within the system. Thus, it can be used to simulate a tissue's thermal dynamic in response to an induced temperature change. The Pennes' Bioheat equation is described as follows:

$$\rho C_p \frac{\partial \mathrm{T}}{\partial \mathrm{t}} + \nabla \cdot \mathbf{q} = \rho_b C_{p,b} \omega_b (T_b - T) + Q_{met} \quad 3.2$$

Where ρ is the tissue density, C_p is the tissues specific heat capacity, $\mathbf{q}$ is the heat flux via conduction within the tissue, ρ_b is the blood density, $C_{p,b}$ is the bloods specific heat capacity, ω_b is the bloods perfusion rate, T_b is the perfused blood temperature, T is the tissues absolute temperature, and Q_{met} is the metabolic heat source.

Cooling Modes

Due to the anticipated amount of heat that needs to be removed during a cooling event, the TEC hot-side cooling method needed the ability to support this. Four heat management options were considered at the start of the In Silico study:

- Passive Cooling Reservoir
- Cerebral Spinal Fluid Flow
- Flexible Heat Pipe to Inner Skull
- Active Microfluidic Coolant Flow

Out of these four, the Passive Cooling Reservoir was immediately dismissed. The idea would have been to have 'thermal battery' mounted to the TEC hot side. During cooling operation, this Cooling Reservoir would absorb the excess heat from the TEC and then slowly dissipate it out to the surrounding tissue once cooling had finished. The Cooling Reservoir would have had to consist of a material with a high thermal capacity. It would also need to be able to modify its thermal conductivity to be high during cooling and low during thermal release. Whilst they system may have been physical viable, having the cooling length dependant on seizure occurrence provides little certainty in the maximum quantity of heat energy needed to be stored. If one were to account for long runs, the design would be larger than the space available to the Interface. This was the main reason for dismissal.

The Flexible Heat Pipe options was also dismissed early. This system would have connected the TEC hot-side to the inner face of the skull. It would transport excess heat to the skull during active cooling using it act as a pseudo-heat sink. The skull is known to be heavily perfused with blood which would theoretically distribute the excess heat throughout the rest of the body. A heat pipe used in this system would have to be flexible to prevent potential damage to the brain and soft surrounding tissues once implanted. Flexible designs of heat pipes have been previously proposed by groups, but a viable option for this purpose has yet to be proposed [118, 121]. It was deemed beyond the scope of this research for a heat pipe development due to the anticipated time requirement. Upon discounting the Passive Coolant Reservoir and Flexible Heat Pipe solutions, simulations for the CSF and microfluidic coolant solutions were undertaken.

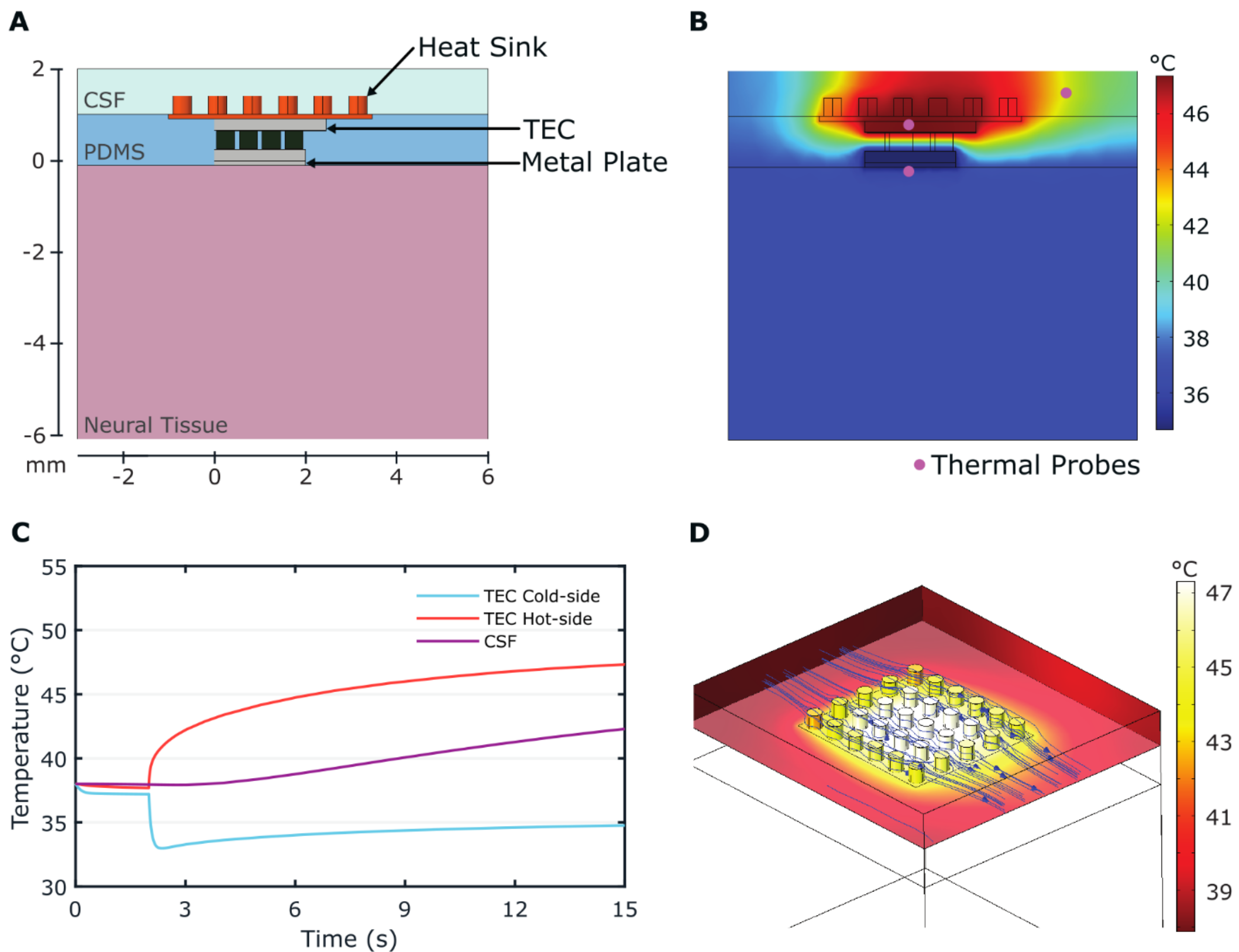

Figure 3.3 In Silico study of a CSF TEC system coolant.
A. Centre slice view of the CSF Coolant *In Silico* model. It consists of 3 material layers: Neural Tissue, PDMS, and CSF. A micro-TEC is embedded within the PDMS layer. It has a stainless-steel plate on its cold-side and a stainless-steel heat sink on its hot-side. The heat sink protrudes into the CSF flow with cylinder fins in a 6 x 5 grid. **B.** Heat map of the system 15s into the simulation after 13s of TEC function. Simulated thermal probes are indicated by purple points. **C.** The distribution of heat at the boundary between the heat sink and CSF flow plotted at 15s into the simulation. Flow lines mapped onto the simulation indicate the CSF flow direction over the heat sink. **D.** Thermal probe plot comparing the TEC cold-side, TEC hot-side, and CSF downstream temperatures over the simulation run time.

Cerebrospinal Fluid Coolant Simulation

Investigation into the validity of using Cerebrospinal fluid as the TEC hot side coolant was conducted first. A simulation model of an implant was built within COMSOL (Figure 3.3A). During this *In Silico* experiment, selection of the physical Interface TEC had not yet been complete. However, the intended dimensional range of the TEC was understood so a TEC replica was built of the dimensions 2 x 2.5 x 0.8mm.

This simulated TEC model was embedded within a PDMS block (8 x 9 x 1.12mm). Attached to its hot-side is a heat sink with a 6 by 5 array of cylindrical fins. Cylinders were selected instead of straight plate with the understanding that the CSF flow vector over the heat sink is brain location dependant. They could also help to support the dura matter at the implant location, providing a constant cavity size for the CSF to flow over the Heat Sink. On the TEC cold-side there is placed a 0.1mm metal plate. This is to account for the situation where the TEC ceramic plates required a biocompatible buffer material. Placed above the PDMS block is a 1mm thick CSF layer and below it is a 6mm thick layer of neural tissue.

The COMSOL stock bismuth telluride material properties were allocated to TEC semiconductor elements and the stock aluminium nitride properties were allocated to the TEC ceramic plates. For the PDMS block, thermal properties from the MIT materials database were used [130]. The heat sink and cold-side metal plate were both allocated the thermal properties of stainless steel 316L – a type commonly found in medical devices. Thermal properties for both the CSF and the neural tissue (using average Brain tissue values) were sourced from the IT'IS Foundation website [131]. The IT'IS Foundation maintains a database on the human tissue properties using up-to-date measurements reported in literature for the purpose of reliable *In Silico* model. CSF flow rate data was collated from reported measurements determined using Magnetic Resonance Imaging (MRI) techniques [132, 133].

To model the thermodynamics of the system, the Heat Transfer in Solid & Fluid physics were used with the CSF allocated the fluid material type and all else being allocated solid. The Thermoelectric Multiphysics was used to model TEC function with the bismuth telluride material properties providing the Seebeck coefficient. Joule heating caused in the TEC is modelled by the Electromagnetic Heating physics. The neural tissue is allocated the Biological Tissue property in which applies the Pennes' Bioheat equation during simulation.

Laminar flow physics was used in modelling the CSF. The assumption of laminar - rather than turbulent flow - was primarily from the need to reduce computation time. All simulations were to be carried out on mid-range laptop hardware so model simplifications were desired. This simplification was anticipated to have a low impact on the inferences drawn from the simulation data. With the low measured CSF flow rate (~0.304mm/s) and the small characteristic dimension of the flow space, the CSF Reynolds number can be estimated to be below the threshold of turbulent flow conditions (~0.55). If the initial simulation results indicate viability of using CSF as a heat dissipation method, then more complex flow regimes will be implemented in the future.

With the model geometry and materials set, a mesh was generated of the system. A custom meshing operation was used. The COMSOL's built-in auto meshing function would provide low quality mesh elements (<0.01) which caused system warnings. Implementing custom operation, the minimum element quality was 0.1318. The final mesh contained a total element count of 925,686.

The study was set to simulate a 15 second period. The TEC was kept inactive for the first 2s to allow the thermal environment to settle from the initial conditions. A 0.2A current source is then applied to the TEC at 2s until the study end point. The total time taken for the simulation to complete was 2hr 43min.

A cross-sectional heat map of the simulation at 15s detail that no successful cooling of the neural tissue below nominal temperature was achieved by the CSF cooled TEC (Figure 3.3B). The TEC does exhibit a temperature differential between the TEC hot-side and cold-side. However, it stems from the excess heating of the hot-side as opposed to the cooling on the cold-side. Heat is being successfully transferred to the CSF but the indicated temperatures are too high for safe biological function. Using thermal probes at points indicated in the model, the temperature of the TEC cold-side, TEC hot-side, and downstream CSF were plotted over the simulation (Figure 3.3**C**). The cold-side temperature initially cooled down to 32.9°C, providing a -4.2°C max temperature difference. But, with the continuous heat increase in TEC hot-side, the TEC cold-side cooling ability diminishes leading to a 34.7°C final temperature. The TEC hot-side probe confirms that heat build-up to a maximum of 47.4°C was achieved by the simulations end. After a time lag, this heat was observed to transfer into the CSF flow. The downstream CSF probe temperature stays close to nominal until the 4s mark. After this the heat transferred into it via the heat sink induces a temperature increase in the CSF to 42.5°C by the studies end.

This high finishing temperature was found to not be contained to the where the cross-sectional heat map of the TEC hot-side and heat sink is located. Through viewing the boundary between the heat sink and CSF in 3D, it is seen that the majority of the heat sinks surface temperature is above 43°C (Figure 3.3D). The central section of the heat sink has managed to heat up to ~47°C. Blue flow lines show the CSF flow path through the cylindrical fins. However, it is evidenced that this flow is neither great enough or at a low enough temperature to be able to sustain the required cooling.

Heat produced on the TEC hot-side is above the thermal limit for which permanent brain cells damage begins to occur. As this heat is then being transferred to the CSF, potential damage is not limited to the direct area around the cooling device. The reason for this temperature excess is that the CSF is unable to dissipate the heat at a fast enough rate. Combination of the small temperature difference between the cooling system and CSF, and the slow CSF flow rate over the heat sink causes this ineffective heat removal. From this it can be determined that CSF cooling of the TEC hot-side would not be a safe method to use with the temperature differences this Interface is required to produce. It is then determined that an active microfluidic coolant system is the only viable choice at present to enable the required Interface specifications.

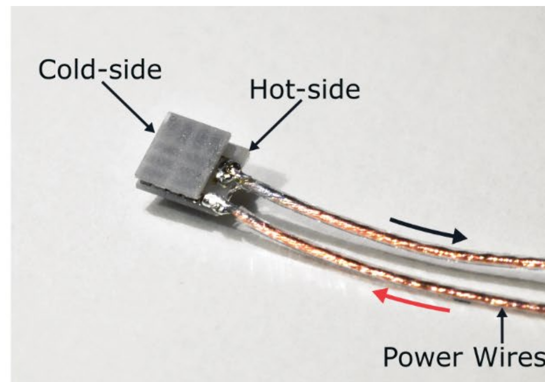

Figure 3.4 The 1TC17-16178-1617.H TEC unit for focal cooling.
TEC face orientation is labelled with the application of power indicated. The red arrow corresponds to Ve+ and black arrow corresponds to Ve-.

3.2.2 Interface TEC Unit

TEC selection involved ensuring that the device was capable of reaching and maintaining the minimum temperature difference of 17°C and that it remained in a compact size with an ideal thickness <2mm. Through an investigation of potential sources, it was decided that the 1TC17-16178-1617.H (TECmicrosystems GmbH, Germany) would be used to enable the cooling modality within the Interface. This device, pictured in Figure 3.4, measures 3.2 x 3 x 0.85mm. It is able to provide direct cooling over a 2.5 x 3mm area on its cold-side.

Electrically, the TEC is specified to handle an I_{max} = 2.4A, a V_{max} = ~1.4V and a maximum power throughput of 2W in dry conditions at 50°C. A maximum temperature difference of 70°C can be achieved by this TEC under these conditions. This will provide sufficient head room for this research's needs.

3.2.3 TEC Temperature Sensing

For accurate temperature control of the TEC during cooling, feedback on the systems thermal state will be required. Independent thermal sensors will have to be placed on both the TEC hot-side and cold-side. Ideal placement for these sensors is the centre of each side's ceramic face. Sensor limitations are primarily on its size as to not increases to system thickness by a significant margin. Dimensional restrictions will limit the sensor head diameter to by no greater than 36AWG (0.127mm). Commercial-Off-The-Shelf (COTS) temperature sensors will be purchased to reduce development time. To develop an in-house specifically for the Interface is beyond this research projects scope at this current stage so is not a viable or implementable solution.

Thermal Sensor Types

Thermal sensing is primarily achieved through the use of one of three different sensor types. Hardware requirements for sensor data acquisition can differ greatly between the sensor types and are generally not interoperable. Selection of the specific sensor type will have to be determined now to prevent design ambiguity during Interface support electronics development. The three potential sensor types are as follow:

Thermocouples

Thermocouples senses temperature by taking advantage of the Seebeck Effect produced at the junction of two dissimilar metals. This produces a temperature dependant potential difference. Different metal combinations allow for a wide selection of temperature measurement ranges. They are an active sensor which requires no additional potential source to provide measurements. Each metal combination has a defined temperature sensing sensitivity value (μV/°C) that is chosen based on sensing requirement.

Over their entire sensing output range, thermocouples present a non-linear potential profile. However, regions of the sensing profiles can be approximated to linear. These linear regions are used to define the temperature sensing range of each thermocouple type. A temperature sensing tolerance of 1% can be achieved with specific thermocouple types.

Thermistors

Thermistors provide temperature sensing through having a resistor produced with a material that has temperature dependant resistance value. These are passive devices that require an external current to provide detectible sensing voltage. However, this current can lead to self-heating of the sensor. The sensing material is formulated with either a negative temperature coefficient (NTC), where temperature increase produces a resistance decrease, or a positive temperature coefficient (PTC) which produces the opposite relationship.

Thermistors are commonly produced using metal oxides encapsulated within a protective polymer, glass or ceramic structure. The relationship between thermistors temperature and resistance values is non-linear but repeatable. Sensing accuracies as low as ±0.1°C can be reliably achieved with high resolution temperature calibration.

Resistant Temperature Detectors (RTDs)

RTDs present as a similar device to thermistors with a temperature sensed through a temperature dependant resistance value. The difference lies in the materials used for sensor construction. RTDs are produced using pure metals that are either wound around an insulating core or deposited on a non-conductive material.

International standards existing for platinum, nickel, and copper. Temperature sensing tolerances for RTDs have a temperature dependency. Referenced to 0°C, the most accurate of these is ±(0.15 + 0.002|T|)°C defined by the DIN Class A. RTDs manufactured to a known standard provides linear and repeatable relationship between resistance and temperature. These sensors are passive so do also require an external current source to produce a voltage reading.

Temperature Sensor Selection

Thermal sensing accuracy requirements for the Interface development (<±0.5°C) means all sensor types present tolerances within acceptable ranges. Selection of the sensor type then primarily was down to the size requirements and sensing action. Of the options presented, thermocouples provide the only easily accessible COTS sensor type within the size limitations stated. With them being an active sensor, it also removes the issue of sensor self-heating and reduces the chances of an exposed sensors causing conditions for unwanted neural stimulation.

Thermocouples shall then be used for the thermal sensing of the TEC hot-side and cold-side. T-type thermocouple will be chosen as the primary type for use in the Interface. This thermocouple type, made from a junction of copper and constantan, presents the highest sensing accuracy of the standard thermocouples available. However, due to the material makeup of a T-type thermocouple being non-biocompatible, the sensing tip will have to encapsulated in a biocompatible medium for implementation.

3.3 General Interface Design

The general structure of each Interface design can be broken down into four discrete parts. The Base Section, the TEC Assembly, the Heat Sink layer, and the Microfluidic Loop. Placement of these parts are visually demonstrated in Figure 3.5. The Base Section makes up the bulk of the Interface's volume. Its purpose is to act as the carrier for the neural sensing and modulation components. Cooling actuation will be achieved via the TEC Assembly. Enabling the cooling neuromodulation, this part consists of a TEC and the thermal sensing components. Placed above the TEC Assembly is the Heat Sink layer. Its aim is to enhance thermal dissipation from the TEC hot-side during active cooling modulation. The top part, the Microfluidic Loop, will be a hollow, printed structure that will cover the Heat Sink. Its function is to guide perfused coolant over the Heat Sink to remove excess heat pumped from the TEC Assembly. Discussion involving Interface development directly will use these labels throughout the Thesis as reference to maintain readability.

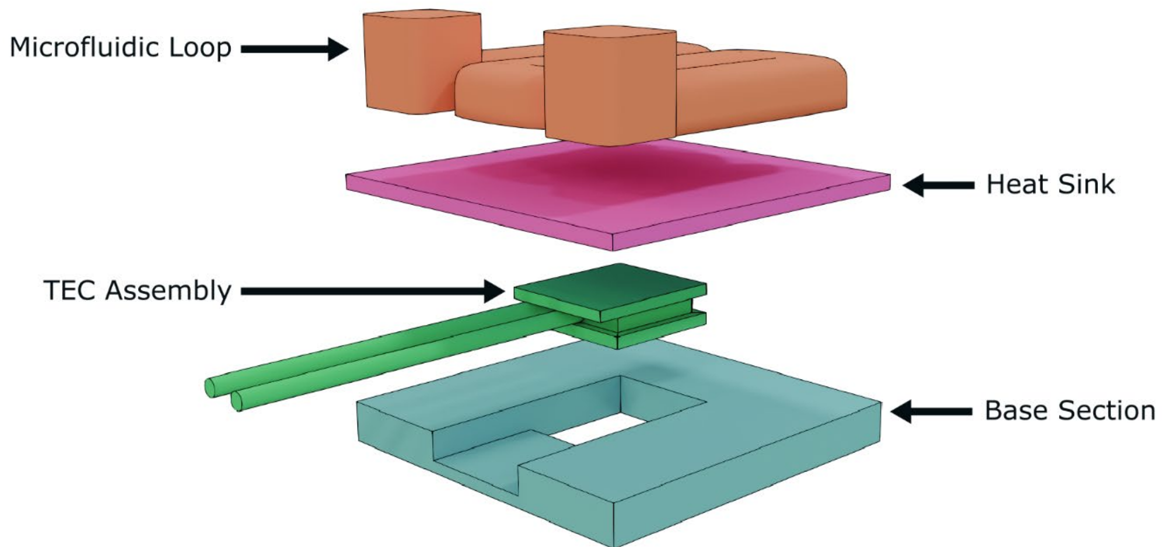

Figure 3.5 General Interface structure diagram.
A visualisation of the four general sections that are stacked to create the Interface. Each section is labelled with its reference name that is used throughout this thesis.

3.4 Bio 3D Printing

The 3D Discovery G5 bioprinter (regenHU, Switzerland) was used to enable the manufacture of the Interface. One of the main differentiators between this printer and other commercially available 3D printer is that the printhead axis movements are achieved through pneumatic actuation. Printing movements are able to be performed with less vibrational noise compared to a stepper motor actuated counterpart. Reduction in system wide vibration prevents extra mechanical stress being imparted on the uncured printed material and reduces system-induced printing failures.

The 3D Discovery platform furnishes the user with the option of using of multiple printing techniques for a single design. Performing mixed print techniques in quick succession without the need for downtime to swap hardware or materials. This allows for a reduction in overall processing time and the creation of more complex geometries. Figure 3.6*A-B* is the 3D Discovery printer's printhead set up that was used over the course of this Thesis's work with each printheads function labelled. All Interface manufacture utilises DIW techniques. DIW is an extrusion-based additive manufacturing method where viscoelastic materials are deposited layer-by-layer in set patterns that result in the construction of complex 3D structures. Printed structures can then require post-print curing, via heat or UV exposure, to set the print material. The complexity of printable geometry achievable with DIW is dependent on the printed material viscosity and print resolution. Print resolution is set by the internal nozzle diameter that the material flows through and the print path spacing.

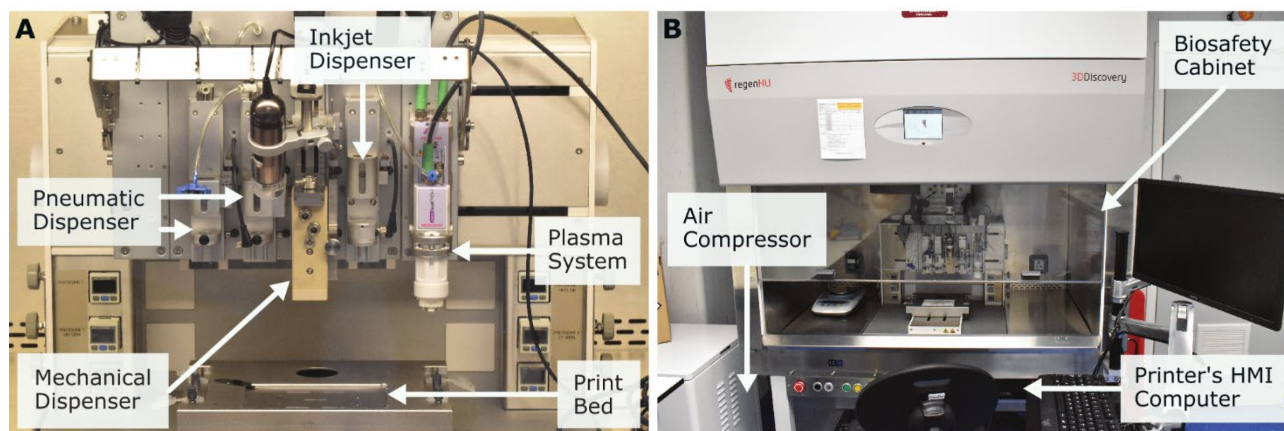

Figure 3.6 The RegenHU 3D Discovery G5 bioprinter for Interface fabrication.
A. Six printheads are available to mount systems on. The 5 labelled prints are occupied in this setup. Include are two pressure dispensing systems (DD-135N, regenHU), one volumetric dispensing system (HPD-100, regenHU), one inkjet system (CF-300N, regenHU), and one cold plasma system (PZ3-i, Reylon Plasma). **B.** The 3D Discovery is mounted within a Biosafety cabinet with an external air compressor for the pneumatic systems and a human-machine interface (HMI) computer that hosts the printer control software.

For the bulk of the Interface's printed parts, the material to be used is SE1700. SE1700 is a two-part Polydimethylsiloxane adhesive whose combined high viscosity and shear thinning behaviour makes it a suitable material for processing via DIW. Printing of this and other silicone composite materials is enabled by the pneumatic "Time-Pressure" dispensing system, DD-135N (regenHU, Switzerland), and the mechanical actuated, volumetric dispensing system, HPD-100 (regenHU, Switzerland) on the 3D Discovery.

3.4.1 Pathing Design Software Flow

The vector-based drawing and g-code generation software, BioCAD, is supplied with the 3D Discovery printer to provide an out-of-the-box path design and processing solution. Initial use of this software for creating and testing simple structures and path design showed it to be a powerful tool. However, as the project's designs got more complex and required greater drawing accuracy, performance limitations within the software became a hindrance to the research. These limitations included items such as the marked reduction in software performance when grid size was set small (~0.230mm square grid), and the software instability upon using the undo function which would lead to crashing.

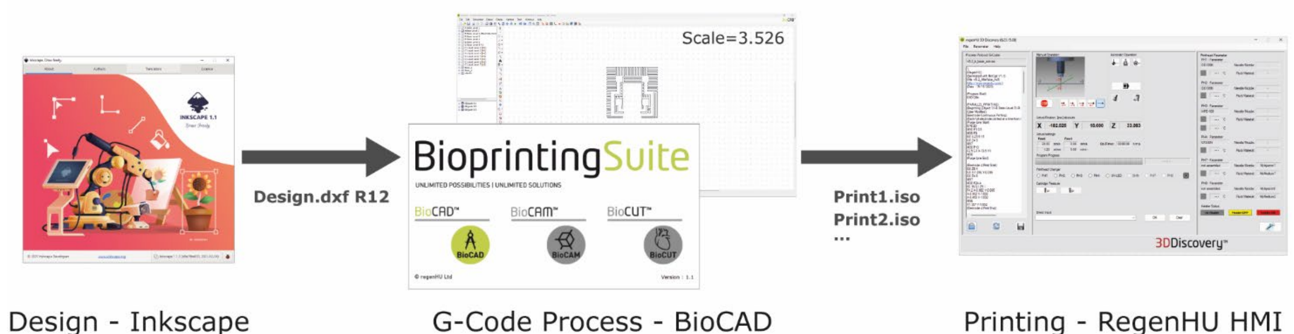

Figure 3.7 Software flow for manufacturing on the RegenHU 3D Discovery.
BioCAD and the HMI are both proprietary software provided by RegenHU for use with the 3D Discovery Printer. Inkscape is an open-source vector graphic software in which the Interface designs are drawn ensuring they can be ported to other 3D printer workflows if required.

An optimal research design flow was found by decoupling the pathing design from BioCAD (Figure 3.7). Instead the interface pathing design was produced within the Inkscape [134], an open-source vector drawing software. This software provided an expanded drawing functionality compared to BioCAD (multi-grids, custom templates, guides, etc) with reduced performance issues. Print path designs would be exported from Inkscape in the DXF R12 format to then be imported into BioCAD. This file format retains the layer order and naming convention, but the design scale is not retained by the transfer. After BioCAD's importing process had been completed, the paths would be required to be scaled by a factor of 3.526[1]. This scale factor was found to be constant for all DXF R12 imports into BioCAD. It should then be assumed to always have been applied when discussing path importing into BioCAD.

The primary tasks undertaken within BioCAD was the material/printhead allocation for each layer, and modifying the print order of the paths. Material properties would include the extrusion rates, nozzle dimensions, and any movement start delay to account for material compressibility (Appendix B). These properties would be coupled to the use of a specific printhead. It was through this allocation process that the multi-material aspect of the bioprinter was implemented.

Both path print order and path printing direction was set on an individual basis. It provided full flexibility over print head movements which was used to enhance print output reliability. Path layers would end up separated in Groups within BioCAD. Groups contain all the path layers that need to be printed on the same z-plane. Each group was given the appropriate z-axis offsets to account for sections printed underneath them. From these formatted groups, BioCAD could then generate the G-Code to be processed by the 3D Discovery's HMI. The methodology utilised for this process is described in more depth as part of the Interface construction methods in Appendix A.

[1] Import scaling issue known to be specific to BioCAD 1.1-17. Some earlier BioCAD versions do not exhibit this behaviour when importing the DXF R12 format. However, at which version this bug was introduced is unknown.

3.5 Interface Version 1

The first iteration of the Interface design would consist only of the cooling modality. This system would be the first trial for combining the printed silicone material and the electronic hardware. Process experience was one of the primary outcomes from the Interface Version 1. Knowledge on the 3D Discovery's printing capabilities would be crucial for the producing reliable printed structures. If a functional Interface V1 is produced then that would enable the collection of *In Vitro* thermal performance data to help refine *In Silico* simulation parameters - increasing model accuracy.

Print path routing was structured to conform around the chosen TECmicrosystems unit. The resultant pathing could be used to predict the geometry of the Interface (Figure 3.8A). The Base Section and Microfluidic Loop will be printed with SE1700 at a 0.430mm path resolution using a 0.437mm ID Nozzle. The TEC Assembly would be bonded to the Base Section with the Heat Sink printed atop it (Figure 3.8). Material for the TEC heat sink had yet to be finalised for the system. In order to retain Interface softness and flexibility a thermal silicone composite was developed to construct a 3D printable heat sink design.

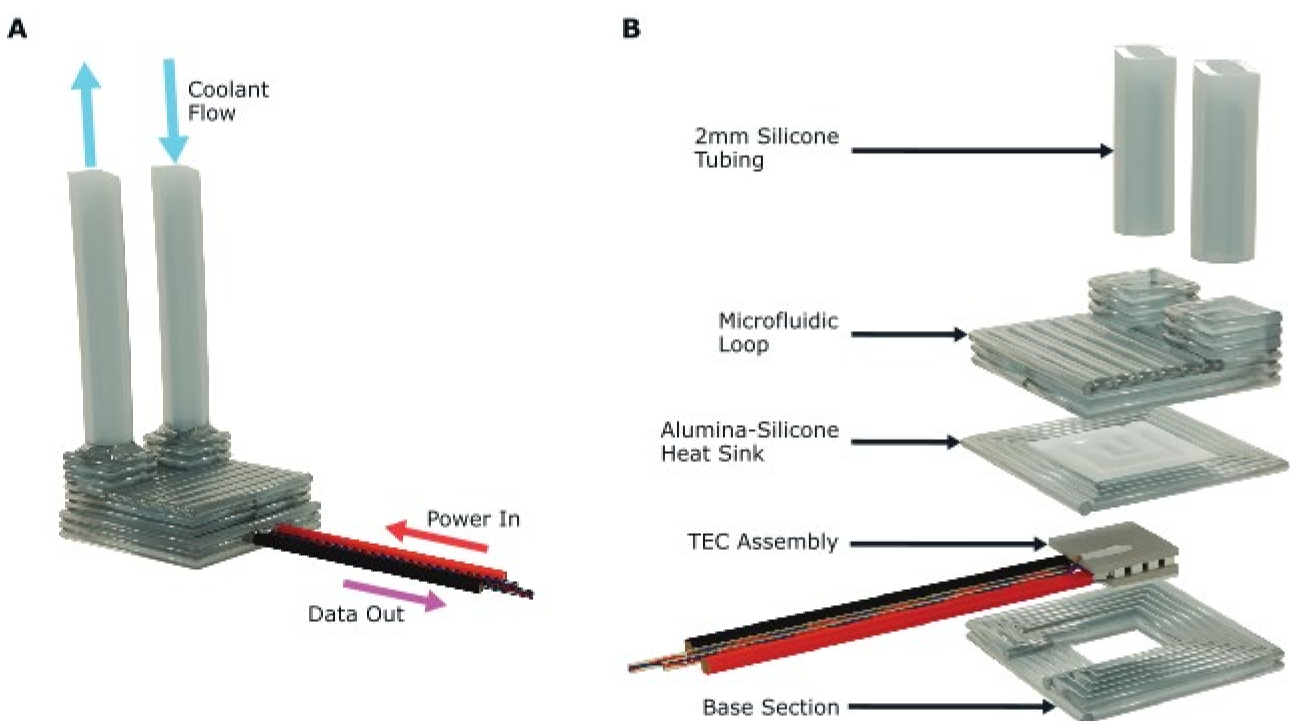

Figure 3.8 3D Visualisations of the Interface Version 1 design.
A. Render of the print paths for the Interface V1 providing a predictor of the Interface's geometry. This model provides the anticipated dimensions of 7.5 x 7.5 x 3.96mm (not including coolant tubing). **B.** Three printed sections are layered to produce the Interface V1 design with the TEC Assembly electronics bonded into the Base Section.

3.5.1 Thermal Silicone Composite

Producing a thermal silicone composite that was both thermally conductive and an electrical insulator was the desired outcome of this material exploration. The electrically insulating specification was included to ensure that any misprinting or material flow before curing. Either situation could cause short-circuit conditions to arise within the Interface electrical components. The particle size was also to be kept in the micron scale as to prevent any material leech being able to pass through cell walls.

This specification immediately removed any electrically conductive materials from the list. This includes any metal, graphite, and graphene-based materials. The focus is then narrowed on using ceramic materials. Aluminium Oxide (Al_2O_3), also known as Alumina, is an electrically non-conductive material that, when compared to other ceramics, presents a high thermal conductivity (30 $Wm^{-1}K^{-1}$). Crucially, it has been demonstrated to be biocompatible - having been used in medical implants [135]. Alumina powder with a mean particle size of 45μm (AL606010, Goodfellows) will be used in the creation of the Thermal Silicone Composite.

Initial work focused on finding a suitable mixture composition and tuning its viscosity to allow printing with the 3D Discovery. Whilst the SE1700 and PDMS silicones allow for the final materials viscosity to be fine-tuned, the main influence on material viscosity would be from the alumina's inclusion as a percentage of total material mass (wt%). This mass percentage will be bound by an upper and lower limit. The lower limit will be determined by the percolation threshold of the alumina particles suspended within the silicone matrix. Once this percolation limit is reached, continuous thermal paths will be formed in the silicone matrix through touching alumina particles. As the material's alumina wt% increases, the quantity of thermal paths grows that it, in turn, increases its bulk thermal conductivity. This idea is demonstrated in Figure 3.9A where the material's alumina wt% is such that many continuous thermal pathways are formed between the TEC hot side and the coolant flow. The limiting factor for the material's upper alumina wt% value, is the ability to deposit the material using the DIW techniques used by the SE1700 printed sections. The anticipated reduction in viscosity is likely to cause nozzle clogging and reduced flow during printing. Finding this upper limit shall be attained through trialling the material samples with the printing process.

First, trials were conducted to discover the upper mix ratio limit. Alumina powder was mixed with both pure PDMS and pure SE1700 in ratios of 10wt% up to 60wt%. With the pure PDMS samples, it was found that the alumina particles would settle towards the bottom of the extruded composite and produce an internal alumina density gradient. It was theorised that this occurs due to the alumina's particle weight and shape allowing it to fall within the low viscosity conditions whilst suspended in uncured PDMS. In using pure SE1700, the printable composite percentage of alumina is limited to 40wt%. Composites mixtures with larger alumina wt% would result in material viscosities that caused nozzles to quickly clog resulting in discontinuous extrusions.

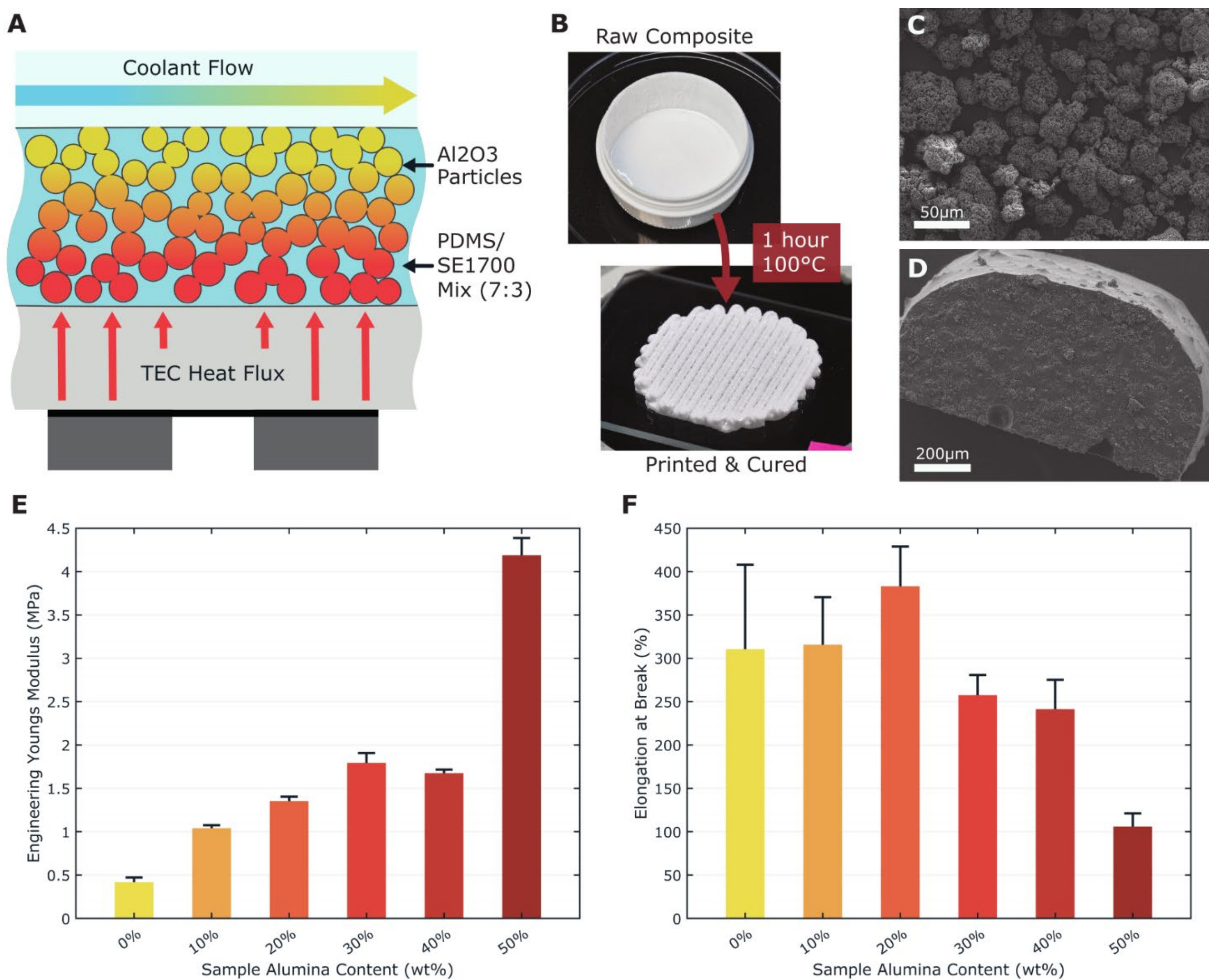

Figure 3.9 Thermal silicone composite material for 3D printing.
A. Theory of the Thermal Composite function. Thermal paths are created by contacting Aluminium Oxide (AL_2O_3) particles suspended with a PDMS/SE1700 silicone (7:3 mix ratio). **B.** The uncured thermal silicone composite of 50wt% alumina that is printed into a multi-layer pyre structure. The cured article demonstrates material stability. **C.** SEM image of the AL_2O_3 particulates procured for composite testing. **D.** A sliced cross-sectional SEM image of the 50wt% Alumina thermal composite mix indicating uniform dispersal through the silicone matrix. **E.** Averaged engineering young's modulus of the thermal composite material dog bone samples. Sample alumina content ranged from 0wt% to 50wt%. The sample's standard deviation is indicated by an error bar for each value. **F.** The thermal composite sample's averaged elongation-till-break represented as a percentage of its start length. The sample's standard deviation is indicated by an error bar for each value. Thermal composite sample set sizes for the young's modulus and extension are: 0wt% alumina (N=4); 10wt% alumina (N=3); 20wt% alumina (N=3); 30wt% alumina (N=3); 40wt% alumina (N=5); 50wt% alumina (N=5).

After testing mixtures involving SE1700, PDMS and alumina, the most promising ratio were found to be 3.5:1.5:5 respectively. This represents a 50wt% alumina thermal composite mixture. The silicone component is composed of a 7:3 ratio of SE1700 and PDMS respectively. This composite ratio was able to be mixed into a homogenous material and still presented the shear thinning properties conductive to DIW manufacturing. Using a 0.854mm nozzle, geometrically stable 3D structures could be printed and cured without displaying post-disposition material flow (Figure 3.9B).

SEM imaging of the raw Alumina powder verifies that the geometric profiles of the particles was visible consistent within the specified 45µm scale stated from the manufacturer (Figure 3.9C). Visual analysis of the sliced 50wt% Alumina sample indicates a well distributed particle density across the sliced face (Figure 3.9D). This suggests that continuous thermal paths are likely to have formed throughout the silicone matrix. In this sample, much of the surface is covered in a silicone skin that is pocketed with small patches of alumina particles breaking through. This skin would then be expected to be present across the printed Heat Sink surface. This would function as a thermal insulator between the bulk Alumina inside the silicone matrix and the coolant flow. The only solution to reduce this insulating effect would be to agitate the cured Heat Sink surface with a scalpel. Agitation of this type would cause skin layer removal and fissures to form across the printed materials surface. Both outcomes would expose more alumina particles to the coolant flow and would be of benefit to the Heat Sink function.

Tensile testing was conducted on thermal composite samples to profile its mechanical changes as the alumina wrt% is increased. Five dog bone samples were fabricated for each composite composition from 0wrt% to 50wt% alumina content. The 0wt% alumina sample was the silicone matrix mixture in a pure state. Testing was undertaken using the Z3 Tensile Tester (AML Instruments, UK) mounted with a 100N load cell. The stress-strain data output from the tensile test was used to calculate the individual samples engineering young's modulus and elongation-to-break as a percentage of the sample's original length. Within each Composite alumina wrt% sample set, the young's modulus and elongation values were averaged together and their standard deviations calculated. Any sample that prematurely fractured due to air cavities in the material was removed from the averaged value. This causes the sample set size for each alumina wrt% as follows: N=4 (0wt%); N=3 (10wt%); N=3 (20wt%); N=3 (30wt%); N=5 (40wt%); N=5 (50wt%).

Increasing the alumina wt% of the Thermal Silicone Composite does result in an increase of the materials engineering young's modulus (Figure 3.9E). 50wt% alumina presents the largest engineering modulus of 4.19MPa (±0.197MPa). When compared to the average 0wt% value of 0.418MPa (±0.053MPa), the addition of 50wt% alumina to the silicone matrix results in the materials modulus increase of a factor of 10. This engineering modulus increase translates to a decrease in sample elongation before destruction (Figure 3.9F). With the 0wt% alumina sample's average elongation being 310% (±97.4%) of its original length and the 50wt% alumina samples only achieving an average elongation of 105% (±15.5%).

However, even with 50wt% alumina samples, the material modulus range (~0.4-4.2MPa) can still be considered a mechanical soft material when compared to other flexible interface construction materials, such as polyimide (~3-6GPa) [136]. This data provides evidence that the thermal silicone composite conforms to the desire that the Interface is to be constructed out of soft and flexible materials. Further mechanical testing would be suggested if this material is used for all Interface designs to increase modulus precision. This would need to be performed alongside an improved experimental design to capture a samples cross-sectional deformation that occurs during testing due to silicone's elastic properties. In doing so, this can be included in the material modulus calculation and increasing its accuracy.

3.5.2 Print Paths

Version 1 was constructed out of the core three sections where the Base Section was produced simultaneously with the TEC Assembly. Once these two sections were adhered, the Heat Sink would be printed atop. Then the Microfluidic Loop was constructed on the Heat Sink. The Base Section, Heat Sink and Microfluidic Loop are 3D printed whilst the TEC section was constructed using of discrete components. SE1700 was extruded through the 0.437mm tip in this design. The thermal silicone composite was required to be extruded through a 0.857mm tip.

Base Section

Constructed out of two 0.457mm layers of SE1700, the Base Section is designed to mount the TEC assembly within. The print paths are designed in a spiral pattern to allow uninterrupted material deposition (Figure 3.10A). Layer 1 starts from the outside and works inwards. This print direction ensures the external dimensions remain consistent through each print. Layer 2 is then printed in a zig-zag pattern around the void for the TEC Assembly. Due to the pathing on this layer, a separate extrusion path has to be placed around the internal perimeter of TEC Assembly void and interconnect channel. These two layers combine give the Base Section a total height of ~0.914mm with a printed example pictured in Figure 3.10B.

Heat Sink

Printing the Heat Sink required the use of two pneumatic printheads within the 3D Discovery. One mounted with a syringe of SE1700 and the other mounted with a syringe of the thermal silicone composite. These were mounted on printheads 1 & 2 respectively. The thermal silicone composite was printed through a 0.857mm to prevent nozzle blockage occurrence. To ensure a consistent layer height, the layer thickness for the thermal silicone composite material is set to 0.400mm to conform with the SE1700 print layer.

Heat Sink print paths are separated into the two separate material paths (Figure 3.10C). The thermal silicone composite is printed first with the extrusion starting on the outer perimeter and spirals inwards. The external SE1700 guard ring is printed similar fashion with the extrusion following a spiral path inward. The resultant layer, in isolation, is pictured in Figure 3.10D. Thermal silicone composite can be seen printed uniformly as the central heat sink. The SE1700 material then form a 'guard ring' around the composite to prevent any pre-cured material flow and act as thermal isolation barrier to the environment.

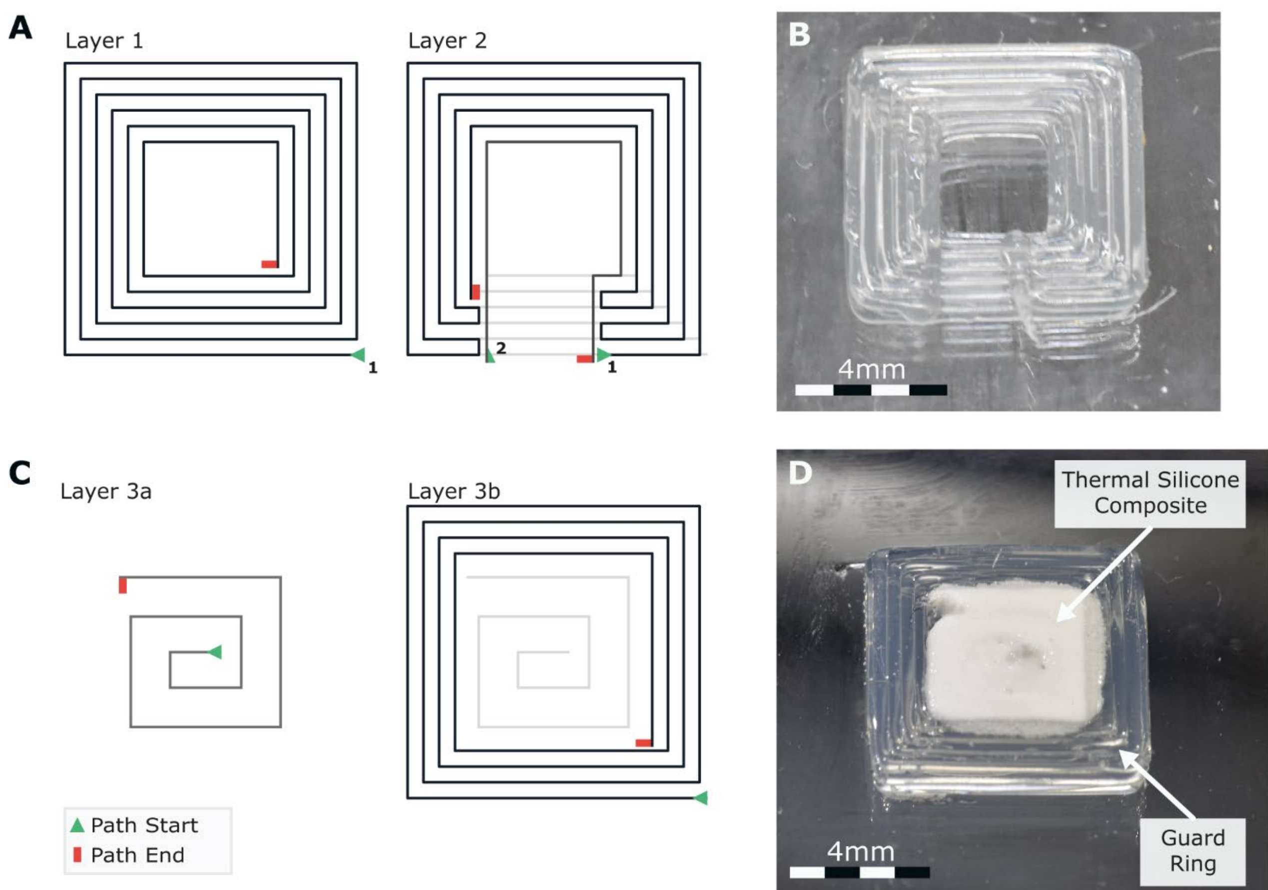

Figure 3.10 Interface Version 1 Base Section and Heat Sink pathing design.
A. Base Section print paths for Layers 1 and 2. Path markers are used to indicate path start, end, and print order. **B.** Base Section sample of the Version 1 print paths pictured in isolation. Base Section dimensions measure 8mm x 7.8mm x 0.920mm. **C.** Heat Sink layer print paths. Layer 3a is printed with the Thermal Silicone Composite and layer 3b is printed with SE1700. Print path Start and End are indicated. A printed Heat Sink sample – **D.** – shows the printed Thermal Silicone Composite material surrounded by a perimeter of SE1700 material.

Microfluidic Loop

As both the Heat Sink and Microfluidic Loop are printed sections, they were able to be printed in one process. Thus, after the Heat Sink is printed, the Microfluidic Loop is immediately printed on top. This increases material adhesion between the two sections which reduces potential of inter-layer gaps forming that would cause coolant leaks.

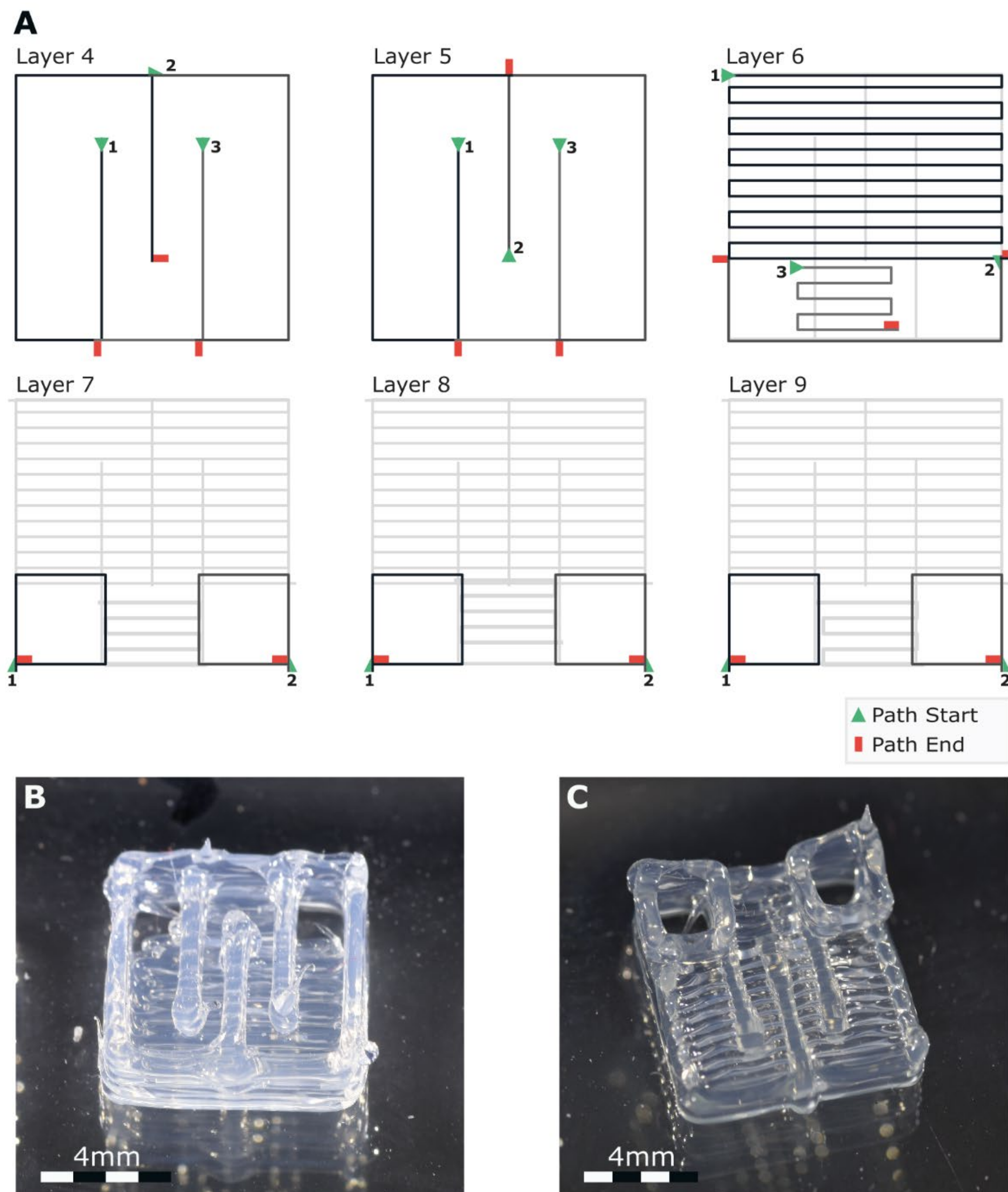

Figure 3.11 Microfluidic Loop design for the Interface Version 1.
A. Print layers of the Microfluidic Loop for the Interface Version 1. Each layer is comprised of multiple discontinuous paths that intersect with themselves or another to reduce path delamination. Print path markers indicate path start, end and order. **B.** Inverted Microfluidic Loop sample displaying the internal channel meandering flow path. Layers 4 to 6 are printed in reverse for channel spacing calibration. **C.** Sample prints of the Microfluidic Loop section. Layers 7 to 9 create an insert to support vertical attachment of 2mm O/D silicone tubing. Post-curing, the channel roof is prone to slumping down into the flow channels.

Formed of 6 layers, the Microfluidic Loop presents the majority of the Interface's total z-height (Figure 3.11A**)**. The channel design is a meandering zig-zig with three internal u-bends to direct the flow over the Heat Sink surface (Figure 3.11B). This meander covers the entire section of the thermal silicone composite with the Microfluidic Loop's inlet and outlet placed on the same edge. The inlet and outlet are sized to mount 2mm outer diameter silicone tubing within (Primasil Silicones, UK). Multiple printed layers are stacked to make a sleeve that supports the mounting of the silicone tubing. This is performed after the Microfluidic Loop has been cured (Figure 3.11C). SE1700 is smeared around the tubing's external face before being fed into the inlet/outlets opening. This SE1700 bonds silicone parts and provides a seal for the coolant flow. Once bond these tubes exit out of the Interface vertically.

3.5.3 TEC Assembly

TEC unit requires additional processing before its permanently adhered into the Base Section. The units purchased were specified to have wires pre-soldered to them during production. This left only the Thermocouples that needed to be adhered to the TECs hot-side and cold-side. A thermal epoxy (MED-T7110, Epotek) was used as the adhesive. It is a two-part epoxy that has certification for both short-term and long-term implantation. The type used for this project was certified for short-term implantation as this project only includes scope for terminal *In Vivo* verification experiments.

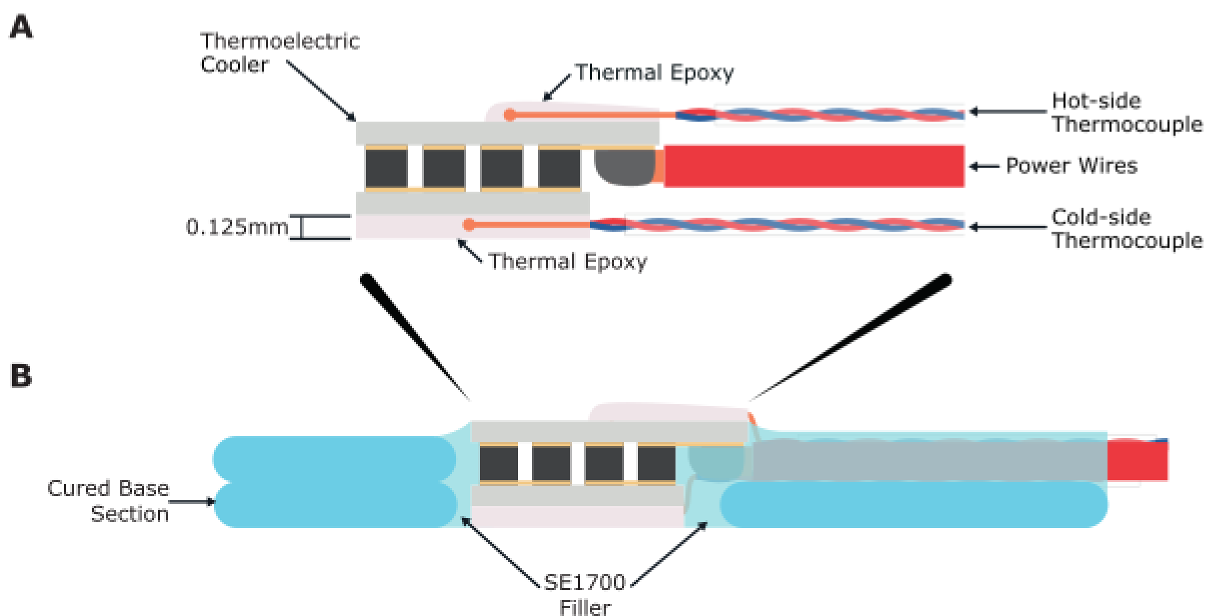

Figure 3.12 TEC Assembly setup for the Interface Version 1.
A. Slice through of a TEC Assembly. Thermocouples are bonded to the hot side and cold side using a Thermal Epoxy. On the cold side, the Thermal Epoxy forms a 0.125mm layer in which the thermocouple is embedded. On the hot side, the thermocouple only adherence before is covered in the Thermal Silicone Composite. **B.** Diagram of TEC Assembly bonding into a cured Base Section via a layer of SE1700. All voids are filled to be in line with the Base Sections top surface.

A 40AWG thermocouple (IT-1E, Physitemp) is adhered to the centre of each TEC face. The hot-side thermocouple is only required to be tacked onto the hot-side as it will be encased in the Heat Sink material. The cold-side is designed to have a flat face that sits flush with the underside of the Base Section. To allows this, the cold-side thermocouple has to be embedded within a layer of the thermal epoxy (Figure 3.12A). A custom produced jig was used to cast a ~0.125mm layer of thermal epoxy on the TEC's cold-side. This jig holds the thermocouple securely against the TEC face whilst creating a well above the TEC cold-side. This well structure ensures that dimensional accuracy in maintained across samples during the curing process. Curing the MED-T7110 thermal epoxy requires 4 hours at 60°C.

With the thermocouples attached, the TEC assembly is then bonded into the Base Section. Bonding is achieved by applying SE1700 around the perimeter of the TEC Assembly and then firmly inserting it into the Base Section (Figure 3.12B). By applying slightly more SE1700 than the space allows, the chance of forming air voids in the bonding material is reduced. Any excess SE1700 is squeezed out in the direction of the hot-side to be wiped away. The interconnect channel, where the TEC wires are routed out of the interface, is also filled with SE1700 at this point. The channel is filled until the SE1700 is level with the Base Section's top surface. The Interface is then inserted into the oven again for 1 hour at 100°C for the SE1700 to cure.

3.5.4 Interface v1 Design Flaws

From the aforementioned Interface Version 1 print paths, a test model was manufactured (Figure 3.14A). The TEC Assembly can be seen mounted within the Interface's printed body. Connection with the TEC and thermocouples is achieved through interconnect wires that exit the Interface parallel to the underside face and TEC cold-side. TEC power wires terminate to pin connections and the thermocouples terminate to Mini T-type thermocouple connectors. This Interface was designated non-functional post manufacture due having a single functional thermocouple. Thus, it was never put through any *In Vitro* verification testing. In Figure 3.14B, there is seen to be only partial thermal epoxy coverage of the TEC cold-side. Whilst being handled post-curing, the thermal epoxy fractured and detached from the TEC cold-side surface. Large air cavities were observed in the cured thermal epoxy and it was these cavities that cause the epoxies detachment and destruction of the thermocouple embedded within. In the future, the thermal epoxy will be deposited in the jig using a syringe rather than with a spatula to reduce air entrapment via material agitation.

Upon further inspection of this sample, it was decided that this would be the only one produced of the Interface Version 1 design. Two issues within the pathing design informed this decision - one that impacts the Microfluidic Loop print reliability, and a second that involves the path print resolution. On the Microfluidic Loop, post-cured loop of this design always required at least one remedial correction to be done to prevent coolant leakage. The unreliability of the printing was understood to be caused by the pathing of the loop coupled with the loop architecture.

Discontinuous pathing is prevalent throughout this loops design. At the end to each path, the printhead stops extruding, raises its height by a predefined quantity, moves to the new position and lower itself down before starting the next path. This process of lifting leads to layer delamination which causes leaks to occur on the Microfluid Loop's perimeter paths. The gaps produced are commonly too small to catch with a visual inspection before curing and can only be noted during post-curing coolant perfusion.

Another problem with the Microfluidic Loop was the channel roof in Layer 6. The channels are sealed via a solid zig-zag pattern printed across the channel walls. However, the distance between these was is large enough that the material bows into the channel. This inconsistent bowing effect causes gaps to appear. As this bowing is also extrusion rate dependant, this would have to be tuned independently for each batch of SE1700 mixed and continuously adjusted over the course of its work time to adjust for the lower viscosity of the part cured material.

The nozzle print resolution also presents a potential future issue with the adaptability of the Interface design. Pathing modifications will be required in the Base Section to accommodate the additional modalities. With the current path resolution, adding in these features would require increasing the Interface's external dimensions. The current pathing design is not flexible enough to add channels easily into the Interfaces form factor.

Both of these issues impede the future development of the Interface. That is why it was decided to perform a complete redesign of the Microfluidic Loop for more intrinsic print reliability. Alongside this, the SE1700 print resolution will be increased from 0.437mm to 0.234mm.

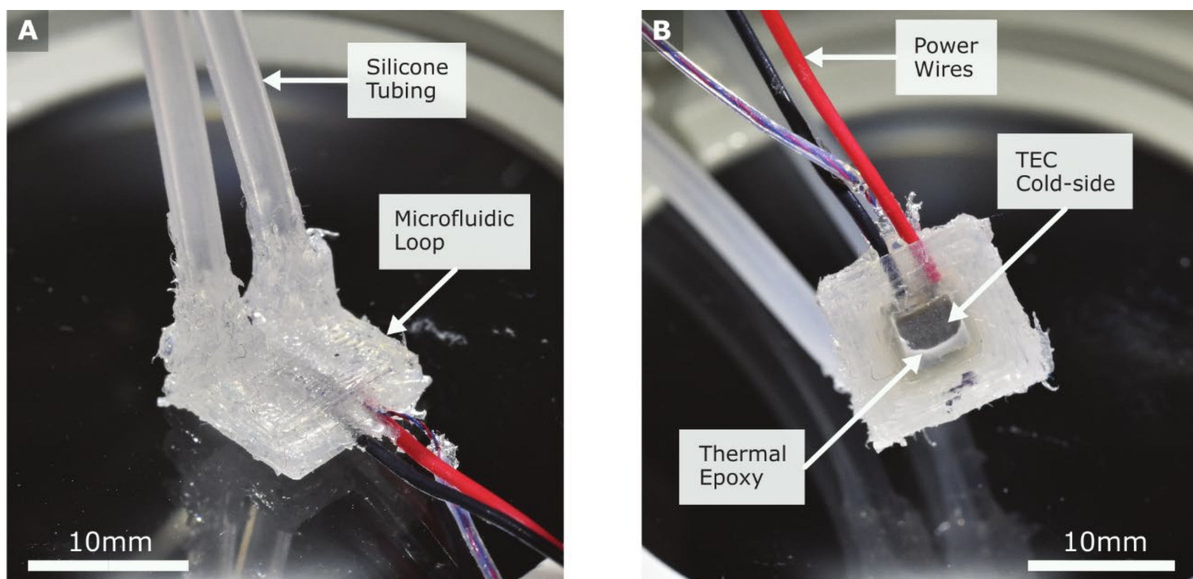

Figure 3.13 Manufactured sample of an Interface Version 1 design.
A. Image of the completed Interface Version 1 system. Silicone tubes attached to the Microfluidic Loop provide inlet and outlet flow paths for the coolant. The red and black sheathed wires provide a power connection to the TEC. The clear sheath wire is the IT-1E thermocouple for TEC hot-side temperature sensing. **B.** Underside of the Interface Version 1 shows the TEC cold-side as only partially covered in the thermal epoxy due to a manufacturing issue. No cold-side temperature sensing is achievable.

3.6 Interface Version 2

To solve the design flaws present in the previous Interface design, the Interface Version 2 was produced. The aims of this design version were: to develop a Microfluidic Loop that could be reliably printed with a low failure rate; to contain a functional cooling modality to test *In Vitro*; and to increase the print resolution of the path design. These were formulated to directly address the issues of the previous design to enable a viable Interface to be manufactured.

For printing, the SE1700 print nozzle extrusion diameter was reduced to 0.234mm. The distance between print paths was set to 0.228mm which provides a ~2.6% path overlap. A complete Microfluidic Loop redesign was undertaken. A new meandering channel design was coupled with modifications to the Loop's G-Code to enable a more repeatable printing output. The design of the TEC cold-side and hot-side epoxy curing jig was altered to reduce potential damage to the thermocouples when the cured device is removed.

This section will discuss the implementation of these changes and results they produced. Print paths for the Interface Version 2 result in the anticipated design visualised in Figure 3.14A. The individual Interface sections, seen in the exploded view (Figure 3.14B), help demonstrate the increase print resolution of the pathing. This pre-visualisation of the Interface Version 2 design gives the Interface dimensions of 9.5 x 9.5 x 2.5mm.

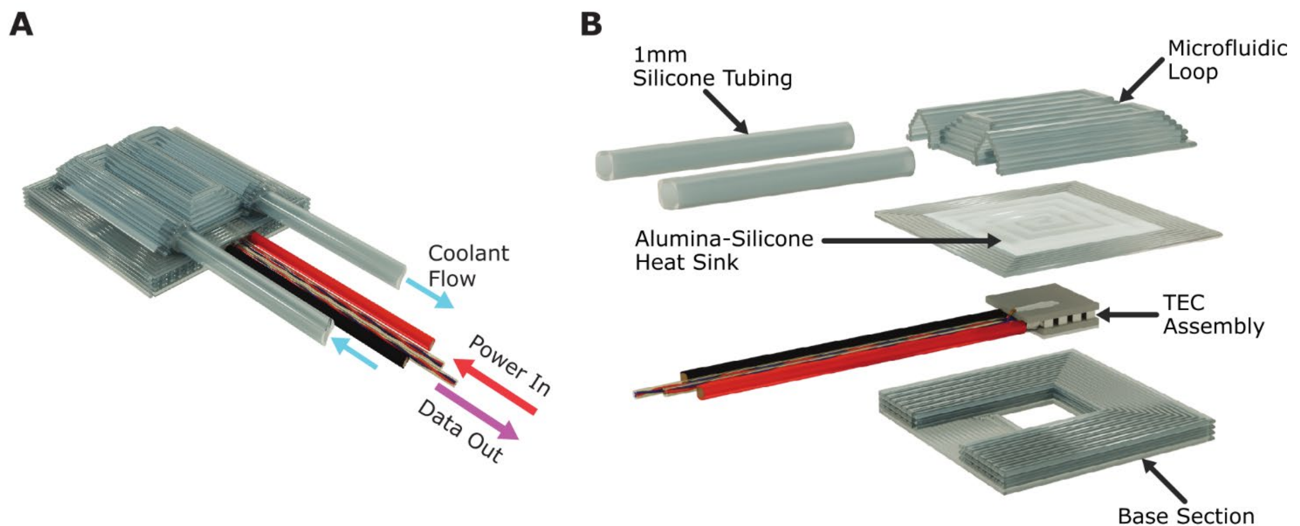

Figure 3.14 Interface Version 2 visualisations.
A. Render of the Interface Version 2 print path design. Print resolution and Microfluidic Loop changes provide for a compact interface. **B.** An exploded view of the Interface Version 2. Internal design changes to each section can be compared to the previous Interface design.

3.6.1 Continuous Printing for Reliable Microfluidics

The primary aim of the new Microfluidic Loop is to have its design be intrinsically reliable so as to reduce remedial work performed post-curing to seal leaks. Inspired by the 3D printed microfluidic channel system published by Ruitao Su et al [137], a study was undertaken to understand if similar unsupported overhanging structures could be produced with SE1700. Printed structures the paper produced uses acetoxy silicone (SI 595 CL, Loctite) – a one-part and fast curing RTV-type silicone. This material presents differing dynamics to SE1700 when the printing as, unlike the acetoxy silicone (working time ≤45minutes), SE1700 cures at a significantly slower rate at room temperature (working time <8 hours). SE1700 can then be considered to be in its uncured state over a standard printing session[2]. Sagging or wall collapse during the printing process is then more of a concern for Microfluidic Loop structures before it is heat cured. To understand this difference, isolated walls prints were produced using SE1700.

Feasibility of Overhang Walls Printed with SE1700

To be able to design the print paths for overhanging walls, print path translations with reference to the previous print layer had to be calculated using trigonometry (Figure 3.15A). Calculations had to fit the constraint of ensuring at least a ~2.6% print path overlap. This is to ensure all overhang angles maintain a minimum confidence in inter-path adhesion. Modification in the horizontal (x/y-axis) and vertical (z-axis) axis of the print paths were implemented at separate stages in Interface design flow. The horizontal path translation is modified during path drawing within Inkscape. By altering the document grid from 0.228mm to the desired overhang angle's horizontal translation distance, the correctly spaced paths can be drawn and aligned with the layers below. Vertical path translation is achieved using a paths material assignment within BioCAD. A material's nozzle diameter property dictates the printhead z-axis offset from the previous layer otherwise known as the layer height. A BioCAD material can only have one nozzle diameter per material instance. Thus, every desired overhang print angle is required to have separate material instances with the its required nozzle diameter.

Five overhang angles were trialled - 90°, 75°, 60°, 45°, and 37°. The relative path horizontal and vertical print path translations were calculated for each of these overhang angles (Figure 3.15B). 6 layer, 12mm long 'wall' samples were draw for each overhang angle as separate print instance on a single glass slide. 2g of SE1700 was mixed just before printing to ensure the material was at its least cross-linked state and thus at its lowest mechanical stability. Walls were printed from largest to smallest overhang angle and were cured simultaneously using the standard SE1700 heat curing protocol (1hr @ 100°C).

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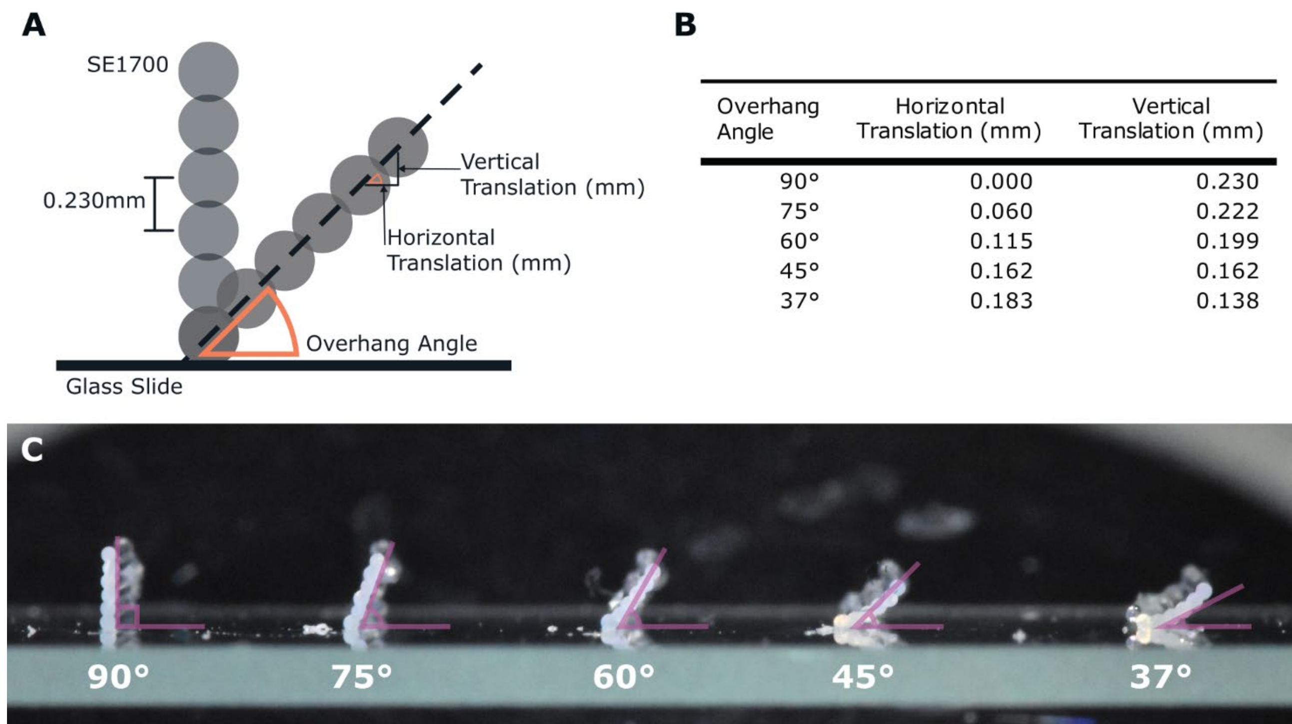
[2] Standard printing session is the amount of time required to print the longest Interface Section printing instance. Its start is defined as the moment the SE1700 part A & part B are first mixed together and its end is defined as the printer completes the printing instance by raising the printhead up.

Post-curing, every wall was vertically sliced at its midpoint. This was performed to expose a wall section not influenced by the increased local bending moment from the potential excessive SE1700 deposited at the print path's start and end points. The resultant wall profiles (Figure 3.15C) indicate no significate wall sagging on the 90°, 75° and 60° overhang walls. Only once the overhang angle reaches 45° does the bending moment increase enough to cause significate wall sagging. However, even with the sagging, both shallow angle walls were successfully printed without complete print collapse.

Results from the overhang wall print testing gave confidence in using overhang angles down to 60° all structural cases up to 6 layer high. For the 45° and 37° overhang printing can't be used for similar isolated wall structures that are dimensionally accurate. However, since these overhang angles didn't completely collapse it is hypothesised that they could be used in printing closed structures without collapse. In closed structures – like the microfluidic channels – the bending moment force would be distributed over the entire wall section and be further supported by wall sections that are attached but their rotational axis offset (around the z-axis). This bend in the structure would create tension in the outer wall of the bend and compression in the inner wall of the bend. These additional forces that could contribute towards stabilising shallower overhang print sections and reducing the severity of wall sagging.



Overhang Angle	Horizontal Translation (mm)	Vertical Translation (mm)
90°	0.000	0.230
75°	0.060	0.222
60°	0.115	0.199
45°	0.162	0.162
37°	0.183	0.138

Figure 3.15 Unsupported wall printing for improved Microfluidic Loop fabrication
A. Reference diagram for the Overhanging Wall prints. All print paths are extruded with a constant 0.230mm diameter. Using the constant extrude diameter and the desired overhang angle, the vertical and horizontal translations where calculated. **B.** Table of translational distance value pairs for each wall overhang angle. **c.** Printed samples of 90°, 75°, 60°, 45° and 37° wall overhang angles. A purple overlay gives comparison to the ideal wall alignment. Material sagging is evident on the 60°, 45° and 37° samples. No wall collapse was observed.

Continuous Printing

On top of the Microfluidic Loop redesign, two other design elements were investigated to enhance print quality with the first being the design of pathing on each layer and the second being the inter-layer behaviour during printing. In the Version 1 paths, no heed was paid to what effect the fractured pathing would have on the resultant print quality. As observed previously, it was clear that having discontinuous pathing within a single layer exacerbated print errors. To counter this, a design rule was established that every layer would consist only of one continuous print path. Discontinuous pathing would only be used in carefully considered cases. This will remove any discontinuity in materials dispensing within a layer and prevent print imperfections forming due to them.

Layer path continuity then leaves inter-layer transitions as the only point where there is material dispensing discontinuity. BioCAD automatically adds in an extrusion stop command and a z-axis retraction before any inter-layer movements are carried out by the printhead. Placement of these commands exists to prevent the nozzle or extruding material impacting the already deposited material during printhead travel to the next layers path start location. BioCAD still inserts these commands even if the end point of the current layer's path and the start point of the next layer's path overlap exactly.

These z-axis movements can be minimised through the manipulation of object properties in BioCAD. However, this did not remove the pauses in material extrusion. There were no options within BioCAD to remove the inter-layer material extrusion halt or the z-axis retraction post-extrusion halt. This left two options going forward: manually perform G-code alterations every time a new print file was synthesised or write a script to automatically process the G-code. The latter option was chosen to make the workflow more efficient for future print file processing.

Inter-Path Command Replacement

Understanding of what BioCAD synthesises for the inter-layer G-code is important as, whilst basic G type codes are standardised, machine specific M codes are specified by the manufacturer. Consultation of both RegenHU suppled documentation and the G-code itself provided clarity in understanding the purpose of each inter-layer command. An example of the BioCAD standard G-code output for the inter-layer behaviour is as follows:

```
44 X-4.946 Y-4.796
45 X-5.76 Y-4.796
46 M96
47 G0 Z5.1
48 (Ending [Object 01-Group 01-Level 01-Layer 1])
49
50 (Beginning [Object 01-Group 01-Level 02-Layer 2])
51 G0 Z5.328
52 G0 X-5.76 Y-4.796
53 G0 Z5.228
54 M97
55 M30 P5.4
56 G1 X-6.411 Y-4.796
57 X-6.411 Y6.435
58 X-3.319 Y6.435
```

where the orange commands highlight those required for transition from the first layer to second layer. The black commands correspond to the individual layer's printing movements. These transition movements and how they relate to the commands are visualised in Figure 3.17A. G-code commands M96 and M97 instruct the printer to stop extrusion and start material extrusion respectively. The M30 command instructs a programme delay with the P(x) value dictating delay time in seconds where the total delay time is equal to [x * 1/18s]. G0 instructs linear movement from the current printhead location to the given coordinates at the maximum system movement speed. This movement can be dictated to take place in a single dimension, as with the z-axis move, or the path can be linearly interpolated to multi-dimensional coordinate demonstrated in the x/y-axis move.

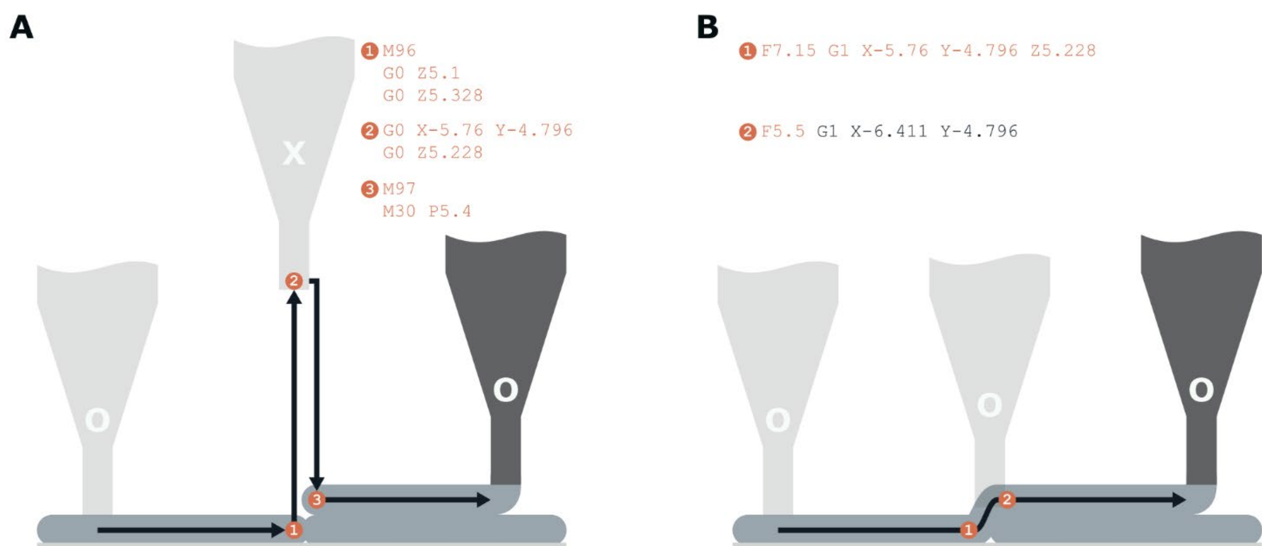


Figure 3.16 Nozzle movements and extrude states during inter-layer transition.
The raw BioCAD G-code output (**A.**) and the devised replacement 'continuous printing' G-code output (**B.**). Each number relates to the G-code line number in the related code segment. The nozzle movement paths follow the arrows with the lighter nozzles showing intermediate positions. Extrude state is dictated by the X or O on each nozzle instance.

All orange highlighted G-code commands are required to be removed to alter the default inter-layer behaviour. The BioCAD inter-layer command set is consistent for all instances so the M96 and M30 commands can be used as bounding markers for the codes to be removed. Any replacement command/s will only be required to instruct the printhead movement from the current layer's path end point to the next layer's path start point. To achieve this only the coordinates from line 52 and 53 G0 commands are required to be spliced together into a new G1 command. This new G1 command gives rise to true 3D printing within the Interface pathing.

An F(x) command was the only addition command required to complete the new instruction. This alters the printing head's feed rate[3] when used in combination with G1. It was found that excess material would be deposited during the inter-layer transition if the printhead feed rate was kept constant. There is a reduced free path volume to occupy for the newly extruded material due to there already being deposited material present at the point of the inter-layer transition. The solution was to increase the printhead feed rate for the transition movement using the F(x) command before returning to the next print path material's value. Transitional feed rate optimisation converged on an ideal feed rate increase factor of 1.3. Thus, the replacement inter-layer G-code of the previous code block would look like:

```
44 X-4.946 Y-4.796
45 X-5.76 Y-4.796
46
47 (Beginning [Object 01-Group 01-Level 02-Level 2])
48
49 (Continuous Printing Input - BioCAD Interlayer Code Replacement)
50 F7.15 G1 X-5.76 Y-4.796 Z5.228
51
52 F5.5 G1 X-6.411 Y-4.796
53 X-6.411 Y6.435
54 X-3.319 Y6.435
```

where the replacement inter-layer commands are highlighted in orange. Visualisation of how the new inter-layer transition pathing is performed by the print head is seen in Figure 3.17B.

To complement the new commands, a restriction to the layer path design was required. This rule was that the start point of the next layer's path must have less than 0.1mm colinear, horizontal offset from the end point of the current layer's path. Having this in place was to ensure that new commanded movement does not impact previously deposited material whilst transitioning. If the distance of the two transition points was greater than 0.1mm colinear to the current path, the material would be unintentionally printed through deposited path. The resultant print would have excess material would be these paths and the overall print becoming unusable.

[3] The 3D Discovery equates feed rate to printhead velocity. To then deposit less material, the feed rate parameter has to be increased. To deposit more material, the feed rate has to be decreased.

Python Script

Python (3.9.2) was chosen as the scripting language to process the G-code files. It enables quick prototyping functionality and code portability due it being an interpreted language. This will ensure a quick development process with an easy-to-use output. The NumPy, re, and sys modules were included to provide mathematical functions, regulation expression comparison operations, and command line argument read/write functions respectively.

The scripts operational process would be to first open the BioCAD .iso file containing the G-code. At the start, the programme locates the printhead feed rate and stores it (assuming that only one material is used for the print). It then performs a line-by-line scan of each command set to find the inter-path movement marker, M96. Once found, the programme steps through each line, saving the X, Y, and Z coordinates of the next layers start point whilst deleting the original G-code commands. After it reaches the end of the inter-layer code, marked by M97/M30, it constructs the new continuous print command out of the saved coordinate data and feed rate value. It adds this new command into the G-code with a 1.3 multiplier on the feed rate value. The programme then adds a F(x) command to reset the feed rate to the base value (x) on the first G1 movement line of the subsequent layer. It then repeats the line-by-line search for the next inter-layer section.

BioCAD G-code files have a consistent command pattern at the end of the printing files that is added into every synthesised instruction set. The continuous printing script monitors the commands read for the start of this pattern to prevent inter-layer replacement activating as the end command set contains the M96 command. Once the end pattern is detected, the altered G-code file is saved under a new, user designated name to prevent overwriting the original G-code .iso file.

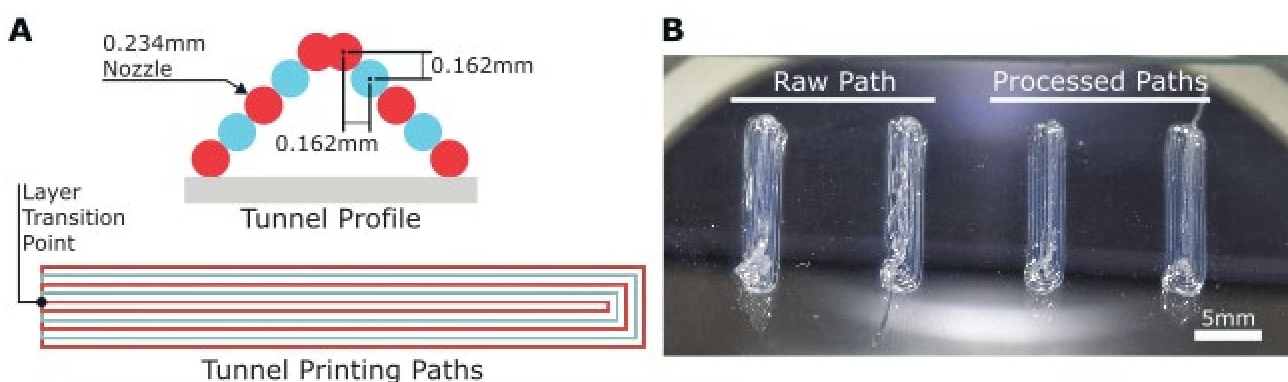


Figure 3.17 Implementation of the inter-layer continuous printing process.
A. Pathing of a simple channel design to test the continuous printing python script. All layer paths begin and end at the same marked point for the script to implement layer transitions correctly. Channel side profile indicate the pathing translations used to produce the 45° wall overhang. **B.** Printed examples of the channels. BioCAD's raw G-code output was used to print the two lefthand samples. Continuous Printing processed G-code was used to print the two righthand samples.

As some prints may require a mix of standard and continuous printed inter-layers, an 'Ignore inter-layer' functionality was implemented. For inter-layer that is required to be retained, a pair of '$' characters can be used to bound these sections. By doing so, the commands within are hidden from the processing script by forcing the script to disable the inter-layer command searching logic as it processes those hidden commands.

Running of the Continuous Printing script is achieved through the Command Prompt (Windows) or Terminal (Linux). Two input arguments are needed for it: the original G-code file path and the user designated name for the processed G-code file. Both names need to include the ".iso" file type in the name for it to be loaded/saved correctly.

To test the Continuous Printing script and identify the print improvements it presents, a simple test print object was produced. The object profile and pathing design is of a single, enclosed channel that would be representative of the next Microfluidic Loop's intended design (Figure 3.18A). A total of four channels were printed. Two were of the raw BioCAD output G-code and two were of the Continuous Printing processed G-code (Figure 3.18B). All channels were printed within a 2-minute window using the same batch of SE1700 to provide comparable printing conditions. Through the implementation of the Continuous Printing a more consistent volume of SE1700 deposition and cleaner print quality can be seen to have been achieved. These prints were produced without optimisation of the pneumatic pressure to the printhead, thus further print quality improvements will be achieved as more printing is performed.

Improved Microfluidic Loop Design

Using the new continuous printing strategy, the improved Microfluidic Loop design can be produced. To fulfil the design rules that have been proposed, the loop will have to be printed as a closed structure and the inlet/outlet of the loop is sliced open once the printed loop has been cured. Inlet/Outlet orientation is adjusted so that the silicone tubes lie parallel to the TEC interconnect wires. The coolant connection tubing diameter was reduced from the previous 1mm ID/2mm OD to a smaller 0.4mm ID/1.1mm OD silicone tubing. The combination of these alterations will help to achieve a loop design that is more robust with a lower size profile than previous.

Channel profile of the new Microfluidic Loop uses a combination vertical and 45° Overhang paths (Figure 3.19A). The cross section is sized to be larger than the updated silicone tubing. The resultant outer dimension of the loop cross section would be 1.7 x 1.3mm. This provides allowance for tube diameter variation whilst also providing space for a sealing layer of SE1700 around the entire tubing. A loop prototype that implements a single bend was manufactured to confirm the new loop channel profile print stability and to assess techniques for the tube insertion processing (Figure 3.19B).

BioCAD material profiles were created specifically for the synthesis of the Microfluidic Loop G-code. These used feed rate parameters optimised during the manufacture of test channel sections[4]. Success in the prototype Microfluidic Loop printing and subsequent refinement gave way to the printing of a more complex microfluidic designs (Figure 3.18C). This Microfluidic Loop design directs the coolant in a meandering path over the Heat Sink (Figure 3.18D). Complete coverage of the Heat Sink prevents hot spots developing providing more consistent heat removal as opposed to having a monolithic chamber design.

Due to the need for the silicone tubes to exit in the same direction, the loop needs to have an odd number of u-bends in its meander. This restricts the width of the loop to approximately $((2 \times Bend\ Quantity) + 1) \times Channel\ Width$. With the overall Interface width limited to 10mm, the maximum amount of loop bends is three. Using this constraint, the new Microfluidic Loop print paths were drawn (Figure 3.20A).

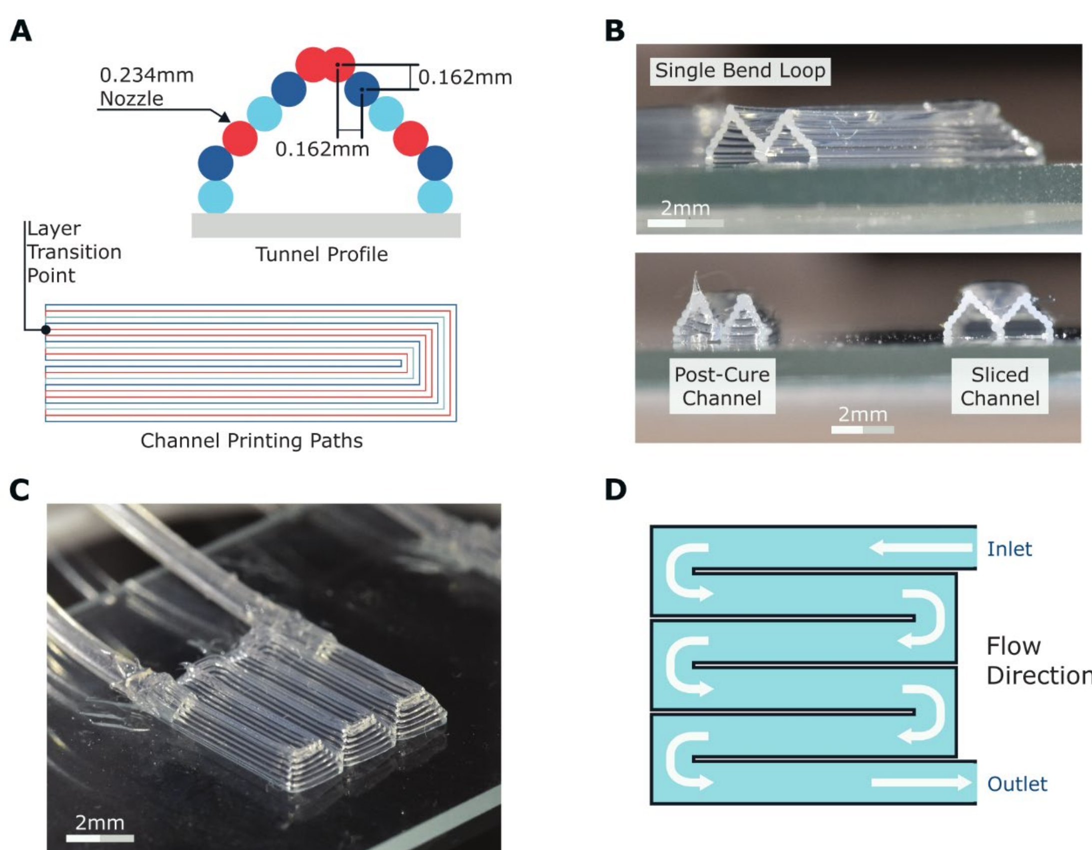


Figure 3.18 Microfluidic Loop channel profile design.
A. Redesigned tunnel profile that increases channel flow cross-sectional area. **B.** Printed articles of the u-bend style channel design with the top picture giving a lengthwise view channel. In the bottom picture, the post-cured channel ends are seen on the left demonstrating the un-interrupted inter-layer pathing of the continuous printing process and, on the right, is a sliced cross section of the printed channel. **C.** Expanding the channel complexity, a scalable Microfluidic Loop can be implemented which follows a meandering flow profile (**D**).

[4] Specific material values can be found in Appendix B under the names SE1700 [90°] and SE1700 [45°].

Anticipated print dimensions of the new loop design were 6.6mm x 8.9mm x 1.3mm. Rendered 3D view of the loop's cross section gives a mock-up of the internal structure of the Interfaces Microfluidic Loop (Figure 3.20B). Channel profile design is maintained from the earlier loop prototypes. For the internal Microfluidic Loop channel walls, it was necessary to place the paths closer together than the nominal 0.228mm. To maintain a continuous print pathing rule and minimise the inter-channel wall thickness these paths are spaced 0.162mm apart.

Microfluidic loop manufacture now consists of three stages (Figure 3.19C). First, the Microfluidic Loop paths are printed in one continuous motion onto the Interface. This is performed in the same printing instance as the heat sink. It is then thermally cured for 1 hour at 100°C. Post curing, a scalpel is used to remove the printed walls that cap the Microfluidic Loop's inlet and outlet. The cut is made so only the capping wall is removed which leaving a small protruding lip at the inlet and outlet. For the last step, two 100mm lengths of the 1mm OD silicone tubing are cut. SE1700 is applied externally at one end of each tube and is carefully inserted ~2mm into the inlet and outlet openings. Care must be taken to not block the silicone tubing with the uncured SE1700. A final thermal curing is undertaken with the same parameters as before. Each loop is then perfused with deionised water using a manual syringe to check for leaks. If any are found, remedial work is undertaken to repair them using additional SE1700.

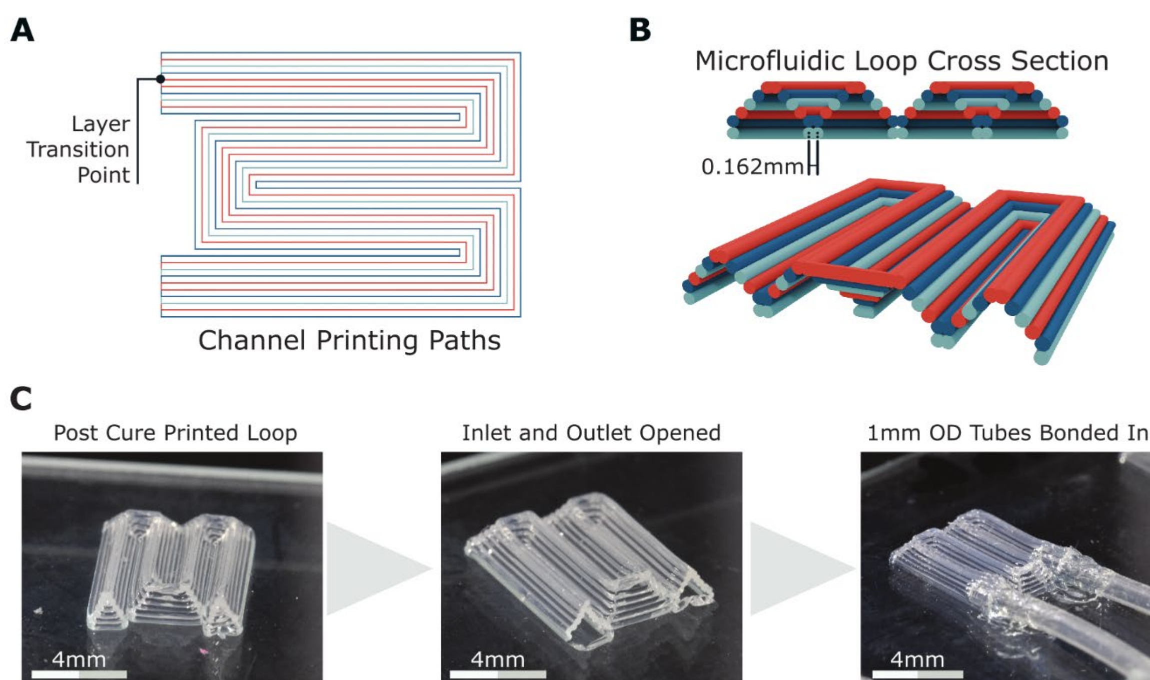


Figure 3.19 Microfluidic Loop design for the Interface Version 2.
A. Print path design for the Microfluidic Loop that is to be implemented on the Interface V2 design. Consisting of 6 layers using the channel profile previously tested. **B.** Renders of the complete microfluidic coolant loop cross section. The inter-channel wall paths are spaced out at a reduced distance (0.162mm) as opposed to the nominal 0.228mm spacing. **C.** Post-print process flow that is required to complete the Microfluidic Loop construction.

Upon implementation of the continuous printing processing and pathing design, the print failure rate was of the loops was significantly reduced. 25% of printed articles (N=15) required remedial action to fix leaks compared to 100% of the previous design (n=18). These repairs were either at the boundary between the substrate and first loop layer, or at the silicone tube bonding boundary. These leaks are mainly attributed to human manufacturing errors. First loop layer/substrate boundary leaks are the result of incorrect z-axis offsets from the print bed. Leaks at the tube bonding sites are formed through not applying enough SE1700 to the tubing before insertion into the inlet/outlet. Both can then be minimised through Interface manufacturing experience and demonstrates the inherent robust nature of the new Microfluidic Loop design.

3.6.2 Interface Print Paths

The increase in print path resolution led to the need in redrawing all print paths. This change also required an increase in print layers to maintain the correct heights of the Interface sections.

Base Section

Four, 0.228mm high layers now make up the Base Section that results in total Base Section height of ~0.920mm (Figure 3.20A). SE1700 is used in printing all paths. Each layer's path has a path end point that overlap with the path start point of the layer above. With this, the Continuous Printing process can be used on the Base Section to improve its print quality.

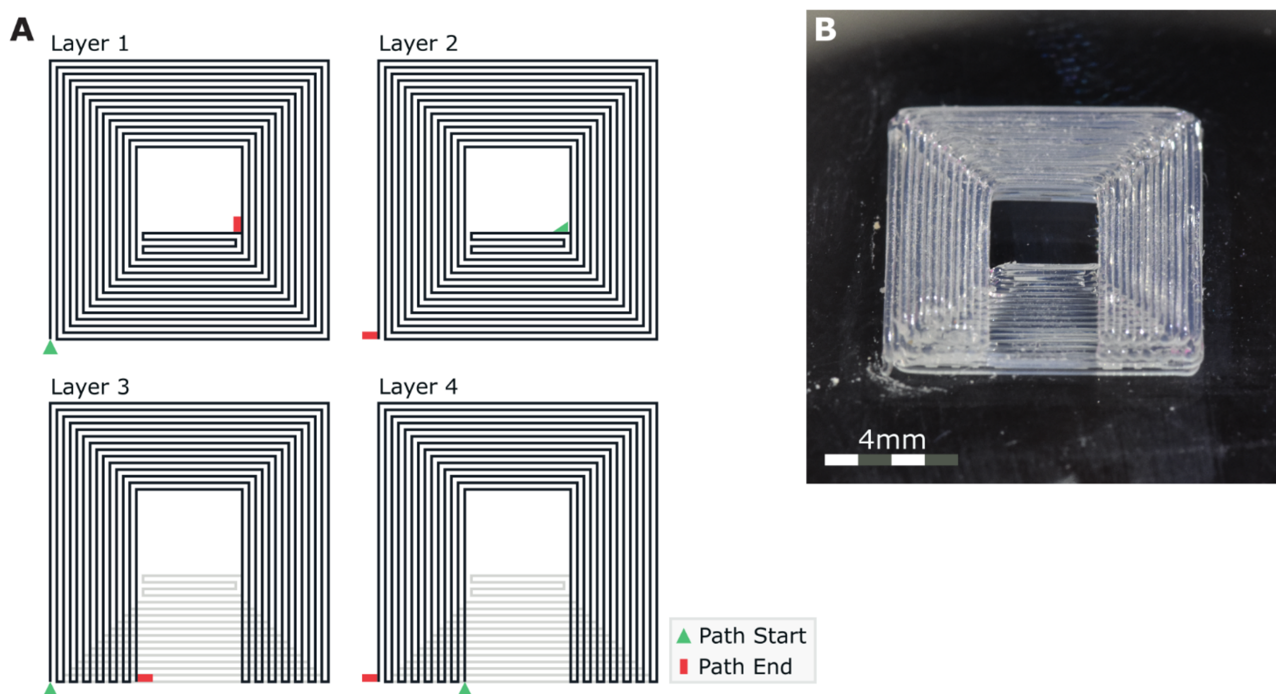


Figure 3.20 Interface Version 2 Base Section design.
A. The Base Section's print paths for all four layers. Stacked incrementally with layer path in black and the previous layer paths in grey. Path-start and path-end points are marked with a green triangle and red rectangle respectively. **B.** Resultant Base Section post-curing. Ready for the TEC Assembly to be inserted.

In order to accommodate the future addition of printed electrodes, it was necessary to increase the Base Section length and width dimensions to 9.5 x 9.5mm. This will proved suitable facilities to allow isolation between electrodes regardless of their composition. Once cured, the Base Section paths are ready to for the TEC Assembly to be bonded to it with a channel for the TEC interconnect wires to be routed through (Figure 3.20B).

Heat Sink

As in the Interface Version 1, the Heat Sink consists of an SE1700 guard ring and the Thermal Silicone Composite interior. Print order of these elements has been reversed with the guard ring printed first before switching to the Thermal Silicone Composite for printing the internal path (Figure 3.21A). This switch was implemented to bound the Thermal Composite better and prevent under guard ring material creep that was identified with the previous print order. Layer height has been reduced for the Thermal Composite to 0.220mm though nozzle size is kept the same (0.857mm). To compensate to the layer height reduction, the Thermal Silicone Composite feed rate was increased to deposit less material during extrusion. These improves to the Heat Sink result in the print sample shown in Figure 3.21B.

Microfluidic Loop

The work describing the design of the Microfluidic Coolant Loop has been discussed extensively previously. Pathing that was used to print the Microfluidic Loop onto the Interface Version 2 design can be seen in Figure 3.22A. There were two alterations to the Microfluidic Loop paths whilst being integrated into the Interface design. First was the addition of a third SE1700 [90] layer which enlarges the flow channel volume. This extra layer was added to reduce the pinching force that the printed channel was exerting on the silicone tubing.

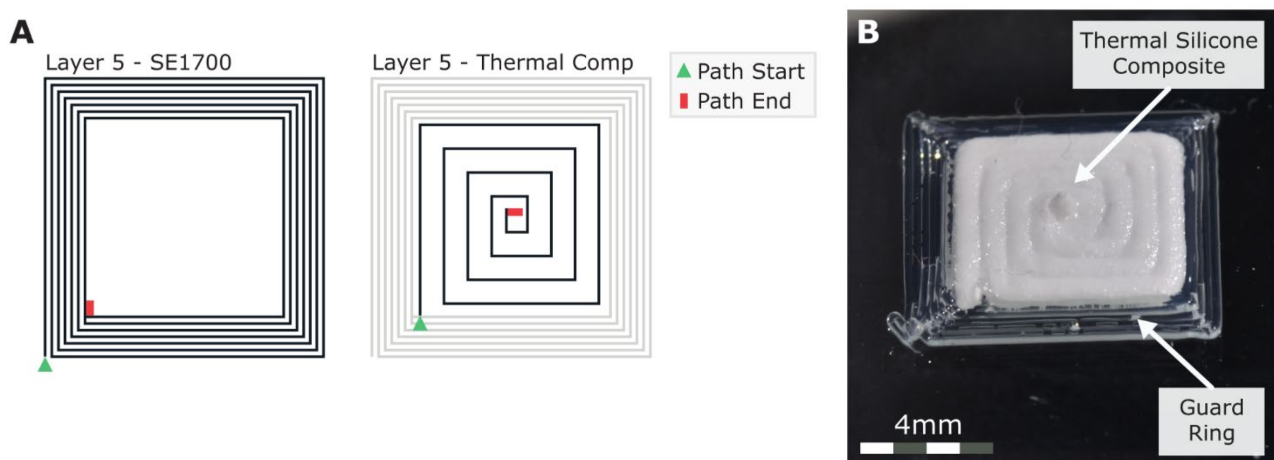


Figure 3.21 Interface Version 2 Heat Sink with the Thermal Silicone Composite.
A. Print Paths of the TEC hot-side printed heat sink. Order for printing is from left to right with the outer SE1700 guard ring printed first and then the Thermal Silicone Composite printed second. Path-start and path-end points are marked with a green triangle and red rectangle respectively. **B.** Shown in isolation; an image of the Heat Sink printed on a glass slide.

The loop's cross section was sized to only just fit the tube so any variation in printing that causes material over-extrusion makes it difficult to mount the inlet and outlet silicone tubes. The extra loop channel height removes the effect of print variation whilst maintaining loop reliability. The second, was the extra perimeter path on layer 6. This is aimed at reducing leakages brought about by manufacturing error from setting the z-axis offset incorrect or having under-extrusion conditions occur. The Heat Sink and Microfluidic Loop are both still printed in the same manufacturing sequence like in Version 1. Printed test pieces of the two parts were printed in isolation to tune out any manufacturing inconsistencies before a complete interface was constructed (Figure 3.22B). Both the additional layer and the new perimeter paths on Layer 6 were found to have their intended effects.

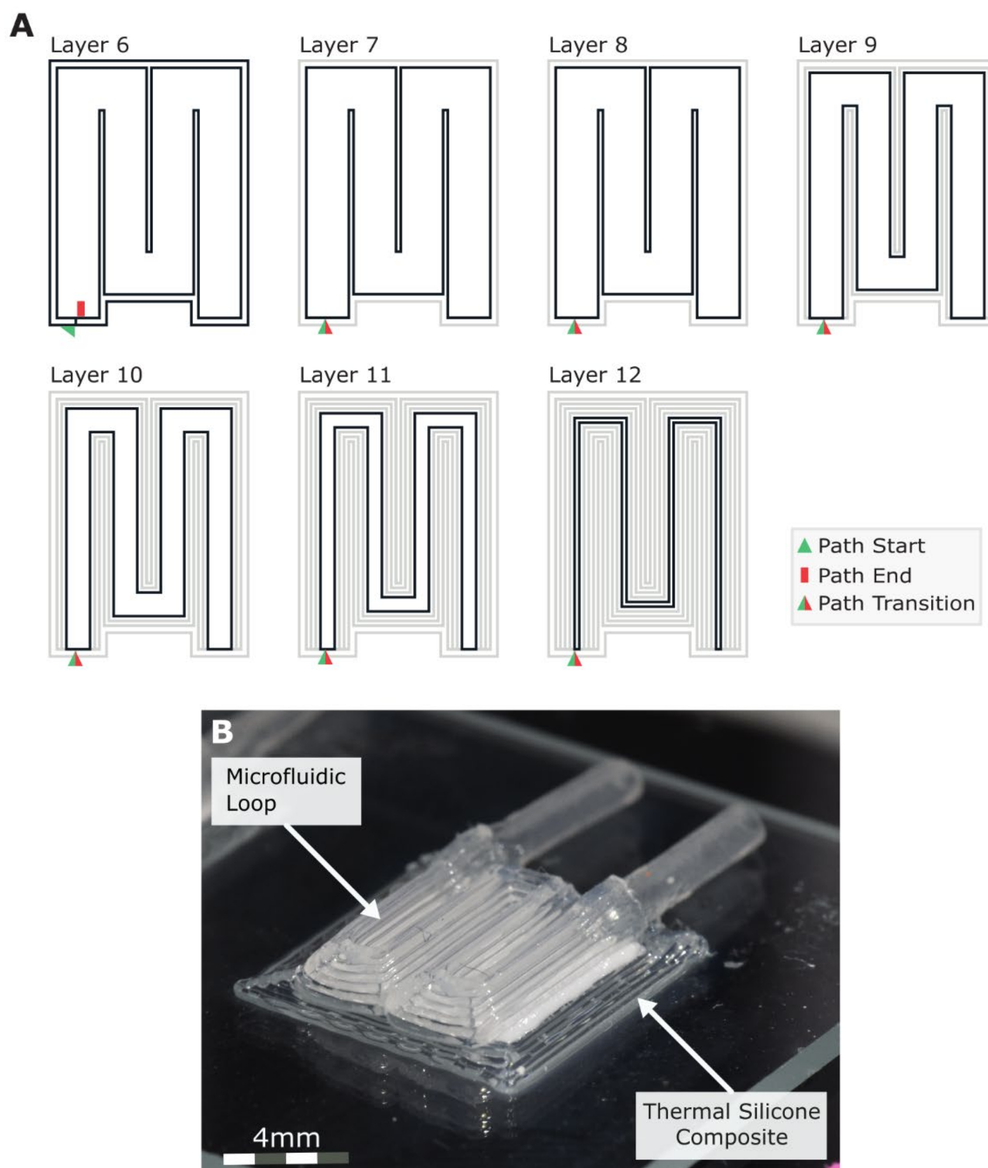


Figure 3.22 Microfluidic Loop design pathing for the Interface Version 2.
A. The seven layers that make up the Microfluidic Loop. The labelled layers path is marked in black with the previously printed layers marked in grey. Path-start and path-end points are indicated with a green triangle and red rectangle respectively. Path-transition points for Continuous Printing as indicated with a green-red triangle. **B.** A printed test version of the Microfluidic Loop and Heat Sink layer in isolation on a glass slide.

Printed Interface

A complete functional Interface of the Version 2 design was manufactured for *In Vitro* trials (Figure 3.23A). The Microfluidic Loop was printed without the need for any remedial corrections post curing. As was the Heat Sink of which the Thermal Silicone Composite is visible through the SE1700 printed material. During manufacture, it was noted that if there is a small shift in position of the Interface during manufacture then thin sections of the Thermal Silicone Composite can be exposed. Remedial work to apply SE1700 over this exposed material was taken if required. To provide a processing fix to reduce manufacturing misalignment potential, a glass slide holder was manufactured to provide consistent positioning during printing.

Both the TEC cold-side and interconnect wires can be seen in on the Interfaces cooling face (Figure 3.23B). In the cooling face centre, the TEC cold-side covered in a layer of thermal epoxy within which the cold side thermocouple is embedded. The TEC power wires and the IT-1E thermocouples are internally routed through the interconnect channel in the Base Section. This is potted with SE1700 during the TEC Assembly bonding process to the base to prevent fluid ingress into the electronics. Exit direction of the wires is parallel to the silicone tubing. Having all fluid and wired connections exit the Interface out of the same plane provides a lower Interface profile and eases external interconnect routing within experimental setups. Damage to the thermal epoxy on the top right of the TEC cold-side is present resulting from Interface testing. However, that damage does not impede Interface functionality.

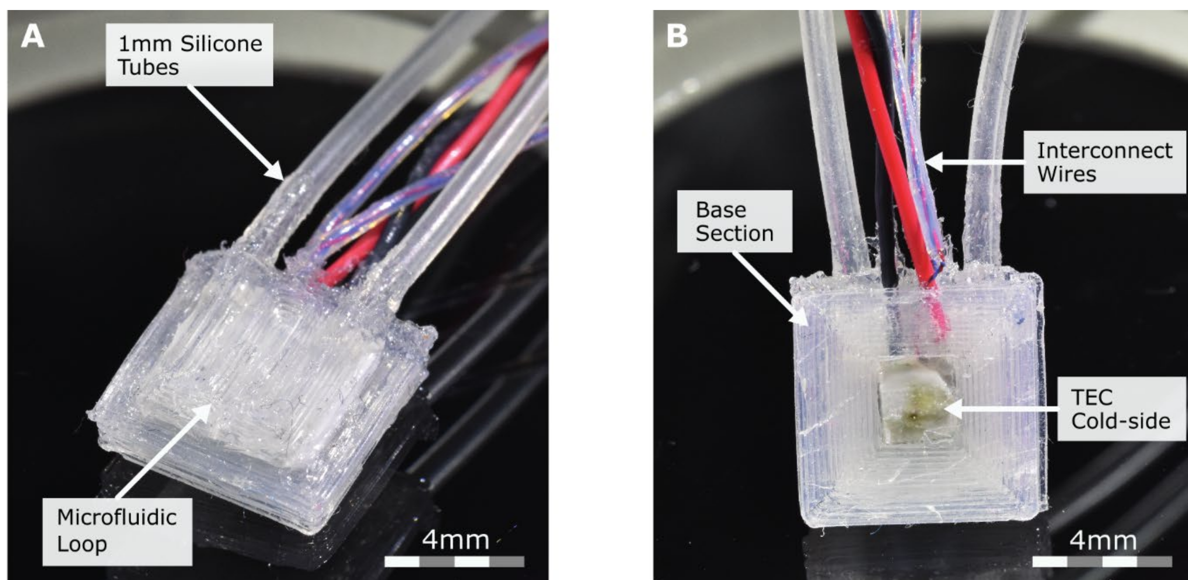


Figure 3.23 Manufactured sample of the Interface Version 2.
A. A functional Interface Version 2 design viewed from the above where the Microfluidic Loop and Heat Sink can be seen. **B.** View of the Interface Version 2 cooling face. From this orientation the TEC Assembly can be seen placed centrally in the face and how the power and IT-1E thermocouple wires are routed internally.

3.6.3 *In Vitro* Cooling Performance

Understanding the Interface design's viability for suppressing seizures required testing in a thermal environment similar to that found at the brain's surface. To perform this, a thermal model was designed to emulate this environment *In Vitro*. Through placing the Interface within the resultant setup, multiple cooling runs were undertaken to profile its cooling capability together with testing the TEC Control PCB hardware.

In Vitro Thermal Brain Model

A water-agar gel is intended be used in lieu of neural tissue. To determine if a water-agar gel will be an appropriate thermal model for testing, a water-agar gel thermal conductivity function presented by Zhang et al, was used [138]. This experimentally derived function describes the relationship between the agar powder concentration in distilled water and the resultant gel's thermal conductivity. At 311.15K (38°C), the water-agar gel thermal conductivity was determined to be 0.4672 W/m·K. This value indicates the gel is a close approximation to neural tissue's averaged thermal conductivity of 0.51 W/m·K [131]. Thus, it was determined to be a suitable *In Vitro* model substitute.

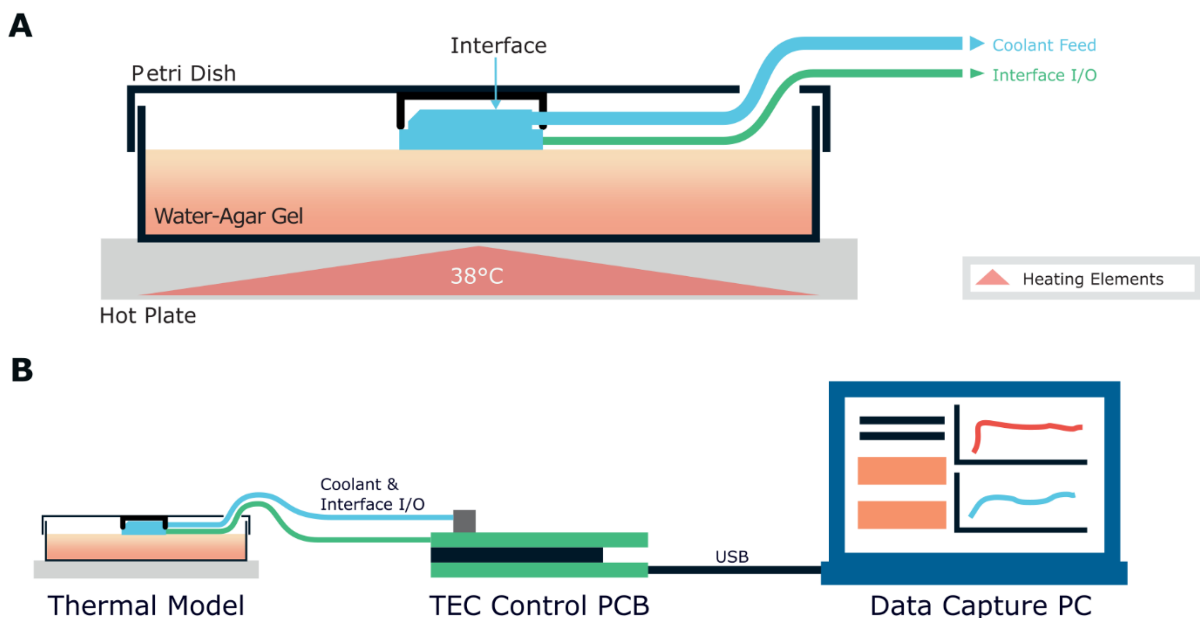


Figure 3.24 In Vitro thermal model to profile Interface function.
A. A cross-section of the *In Vitro* Thermal Brain model. This setup consists of 50ml water-agar gel cast into a petri dish and placed atop a hot-plate. This hot plate is set to provide a constant heat flux into the gel. The petri dish lid holds the Interface against the gel's surface. **B.** Hardware setup required to support Interface operation and data capture during In Vitro experimentation.

Figure 3.24A gives a cross-sectional look at the *In Vitro* thermal model setup used in the Interface Version 2 testing. 50ml of water-agar gel is cast into a 150mm petri dish. Cooling of the gel layer's thermal mass underneath the Interface will allow initial determination of the improved design's functionality. Heat flux into the system is provided by a Hot Plate (HS-W-Pro+, VWR) that the water-agar gel is placed upon. A mounting plate on the petri dish lid holds the Interface against the water-agar gel. A 10 x 5mm hole is cut into the petri dish lid for routing the Interface wires and silicone tubing out to the supporting hardware.

Figure 3.24B demonstrates how the hardware and Interface Support systems are linked. Operation of the Interface is controlled using the TEC Control Hardware, as described in Section 4.4.8. This supporting hardware is then connected to a PC via USB-serial link. On the PC, a custom LabVIEW VI for live system control and data acquisition is used during the *In Vitro* experiment.

Cooling Performance – Interface Version 2

The *In Vitro* thermal model was setup with an Interface Version 2 sample. The hot-plate was set to heat the water-agar gel to between 37°C – 38°C and maintain it for the duration of the Interface testing. Monitoring of the water-agar gel was done through the reading the TEC cold-side thermocouple. The initiation of a cooling run was conditional on the TEC cold-side thermocouple reaching a steady-state temperature between the aforementioned model temperature range. In the first instance, cooling runs were undertaken to verify system function as this was the first experiment involving a completed interface and support hardware.

Temperature sensor ingest; TEC driving signal generation; support hardware output data stream; and support hardware electronic components were all successfully tested as isolated systems and whilst functioning together. Operational test runs were performed with the TEC driver output hard limited to 10% of the maximum TEC current. This was to prevent the possibility of thermal runaway events during individual systems testing that could of potential damaged the hardware (e.g. when conducting isolated TEC driver tests whilst the microfluidic pump was disabled). All cooling run control was provided by the TEC Control LabVIEW VI on the host PC.

Upon successful completion of systems verification, another set of cooling runs were conducted with a 10°C ΔT cooling target from Interface ambient. These runs are the initial gauging of the interface's maximum cooling capability and to find if the design is able to reach near the threshold for suppressing on epileptiform activity. The PID controller was set to proportional mode by setting the integral gain (K_I) and differential gain (K_D) gains to zero. Proportional gain (K_P) was initialised to 15 for the first cooling run and would be tuned until TEC cooling stability is achieved.

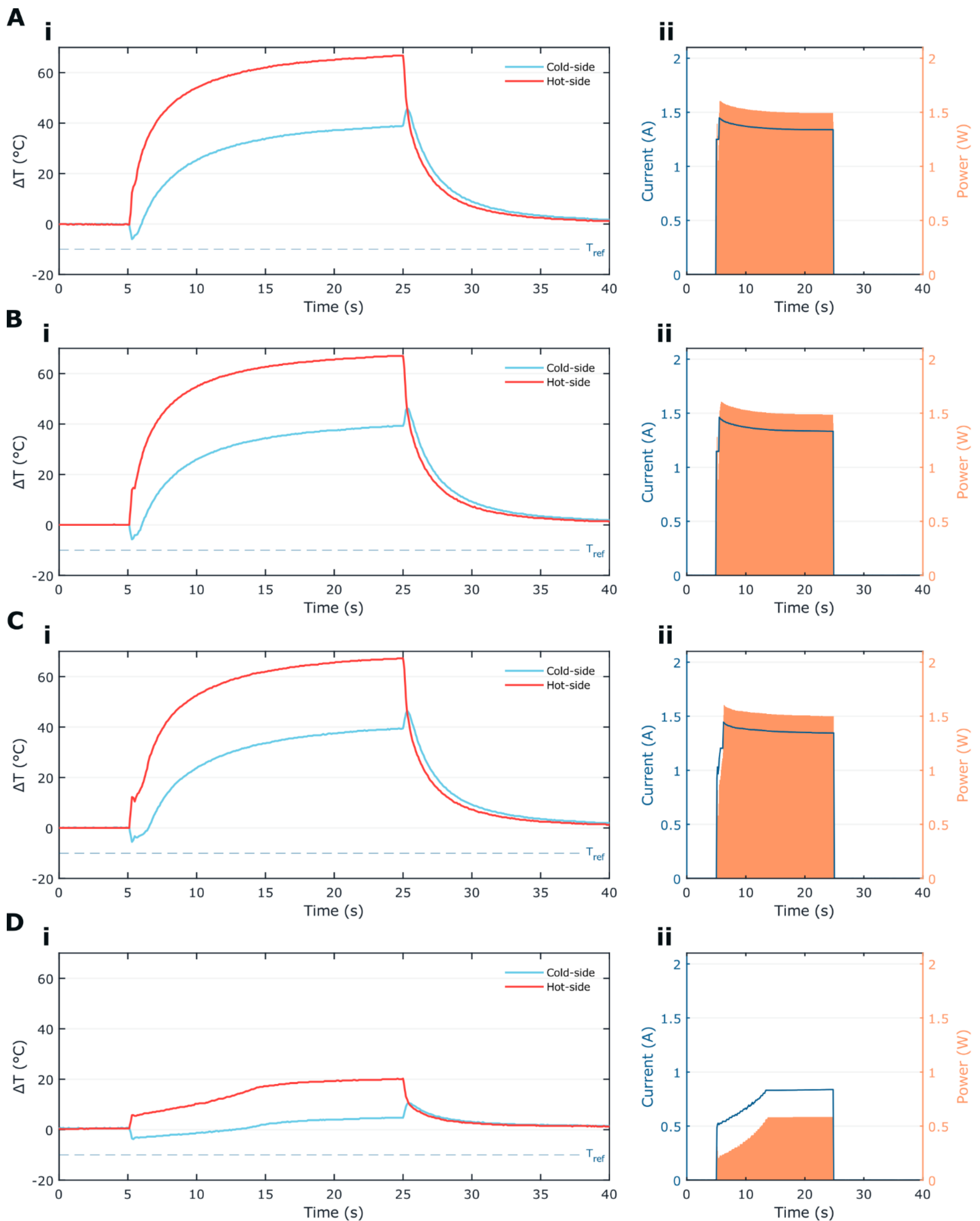


Figure 3.25 In Vitro data of the profiled Interface Version 2 design.
Cooling run data presented for **A.** K_p = 5, **B.** K_p = 10, **C.** K_p = 13, and **D.** K_p = 15. Each graph pair first shows the Interface TEC cold-side and hot-side temperature difference (ΔT) relative to Interface ambient temperature (**i**). Then the TEC driver current profile and TEC power usage during the cooling run is mapped (**ii**).

The cooling program was set to run for 40s total. Upon starting there would be a 5s delay before cooling activation to ensure a valid data stream. The Interface cooling, via the TEC, would then be activated for a 20s period. After this period, all the cooling is deactivated. System data is then collected for another 15s before a complete VI halt at 40s. The microfluidic cooling system would remain activate only during the period of TEC cooling. The coolant used was distilled water and was kept at room temperature (~20°C).

Version 2 Thermal Instability

Throughout these cooling runs, the Interface had difficulties reaching stability near the 10°C temperature reference. At the initialised K_p = 15, the Interface produced the ΔT cooling profile (Figure 3.25Ai) alongside its power use (Figure 3.25Aii). This shows that cooling from Interface ambient was achieved in the first instance. However, as the transported heat build-up on the TEC hot-side, the cooling system began to thermally collapse and that excess heat was reflected onto the TEC cold-side. The Interface power profile gives indication that controller was instantly hitting maximum driver output in attempting to cooling. Reducing the K_p through 13, 10, and then 5 produces the cooling run profiles shown in Figure 3.25Bi-ii, Figure 3.25Ci-ii, and Figure 3.25Di-ii respectively. The instability onset became more delayed and less pronounced but occurred none the less. Reducing K_p gain towards zero did not yield a system that would be able to reach thermal stability with a usable cooling range.

The occurrence of this instability was hypothesised to be a multi-factor issue within the Interfaces thermal design. It was believed that the thermal resistance of the heat dissipation system attached to the TEC hot-side was too high to transfer heat away effectively during operation. Slow heat transfer then leads to a heat build-up that is eventually 'reflected' back into the TEC causing the entire Interface to heat up.

Consideration of this issue points to the Heat Sink as being the main contributing factor. Wherever the Heat Sink design, the Thermal Silicone Composite, or both is the dominate influence needs to be understood. It was decided that a new Interface design will be produced to test if the Heat Sink is the cause of instability and explore potential solutions.

3.7 Interface Version 3

As the Thermal Silicone Composite Heat Sink is hypothesised to be the primary cause of the Interface thermal instability, two alternate options for the heat sink design were explored. The two Heat Sink design options were to either; replace the Thermal Silicone Composite with the thermal epoxy used to attach the thermocouple to the TEC cold-side; or remove the Heat Sink layer and directly expose the TEC hot-side to the flowing coolant.

Data gathered through the implementation of these Heat Sink design changes will be used to determine the origin of the TEC thermal bottleneck and which design direction to take. Pathing changes for the no Heat Sink, and the thermal epoxy Heat Sink variants are visualised in Figure 3.26*A* and Figure 3.26B respectively. A test article of each Heat Sink variant was fabricated. Both of these design fall under the Interface Version 3 labelling.

One Interface with no heat (Figure 3.26C), and the other with the thermal epoxy Heat Sink (Figure 3.26D) were deployed for *In Vitro* testing. Variant specific manufacturing changes were required to accommodate the new Heat Sink designs. The following section describes these changes, the *In Vitro* testing, and the resultant development.

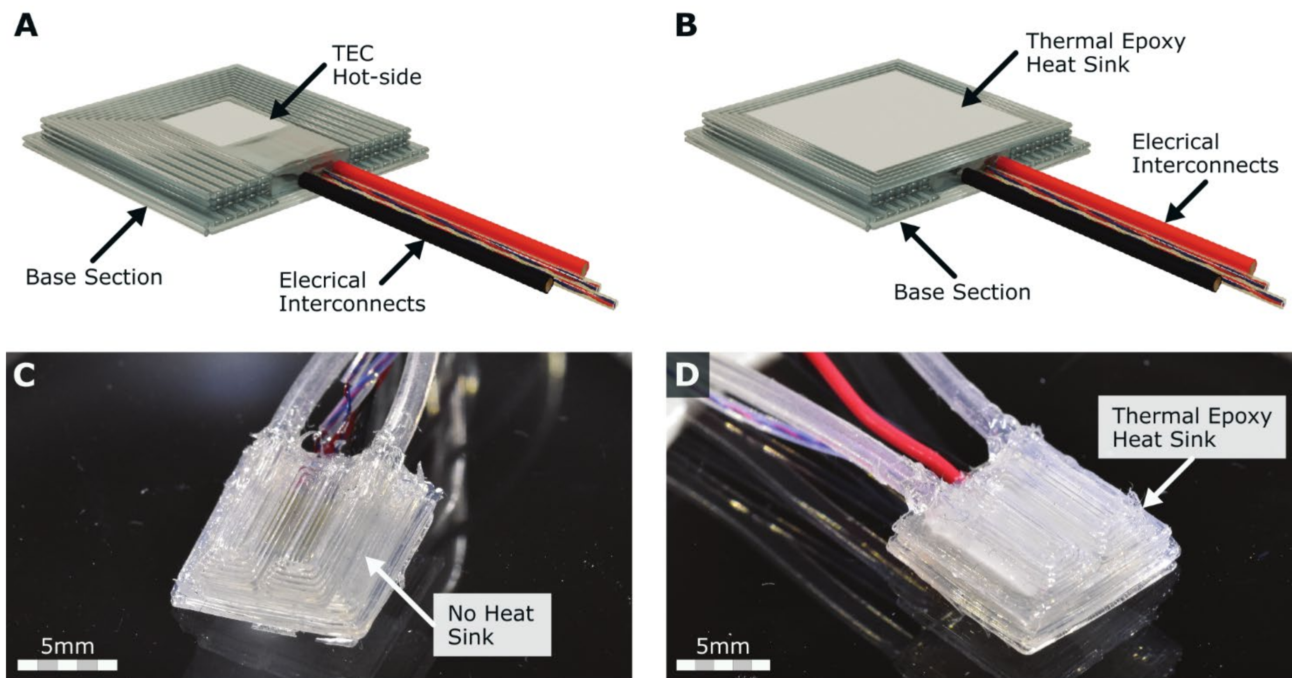


Figure 3.26 Heat Sink variant Interface designs.
Presentation of two potential future Heat Sink designs with **A.** having no Heat Sink and **B.** having the Thermal Silicone Composite replaced with thermal epoxy. Images of the two fabricated Interface Heat Sink variants where, **C.**, has no heat sink on the TEC hot-side, and, **D.**, has the thermal epoxy Heat Sink.

3.7.2 Version 3 Heat Sink Variants

For the no Heat Sink version, manufacturing alterations were required for both the Base Section and the TEC Assembly. On the TEC hot-side, a layer of thermal epoxy now encapsulates the hot-side thermocouple with the same thickness as what was already implemented on the TEC cold-side (Figure 3.27A). This was added in so that the hot-side thermocouple would have more reliable protection from the coolant flow compared to the previous 'tacking on' attachment method provides. This adds an extra ~0.13mm to the TEC Assembly height. To accommodate this height increase, the print pathing for the Heat Sink was replaced with a copy of pathing on Base Section Layer 4 (Figure 3.27B). This results in the Base Section's top now sitting flush with the top of the TEC Assembly. It also means that layer 5 can now be printed in the same instance of the Base Section. With it also being path copy, can be included in the continuous printing processing of the Base Section.

With the thermal epoxy Heat Sink variant, the previous SE1700 'guard ring' path was retained from the version 2 Thermal Silicone Composite Heat Sink. Two of the ring's outer paths were removed due to modification to the Base Section that will be discussed in Section 3.7.3. The printed guard ring creates a well for the thermal epoxy to be potted into. This produces an 8.41mm x 8.41mm heat sink that will be the same thickness as the guard ring (Figure 3.29A). The thermal epoxy's viscosity is not conducive to it being 3D printed with used methods and needed to be hand filled. This then had a knock-on effect to the manufacturing process. It would not be possible to print the Heat Sink and the Microfluidic Loop in one print instance, or - as with the no Heat Sink variant - print layer 5 in the Base Section printing instance. Layer 5 would now have to be in its own discrete manufacturing step (Figure 3.29B).

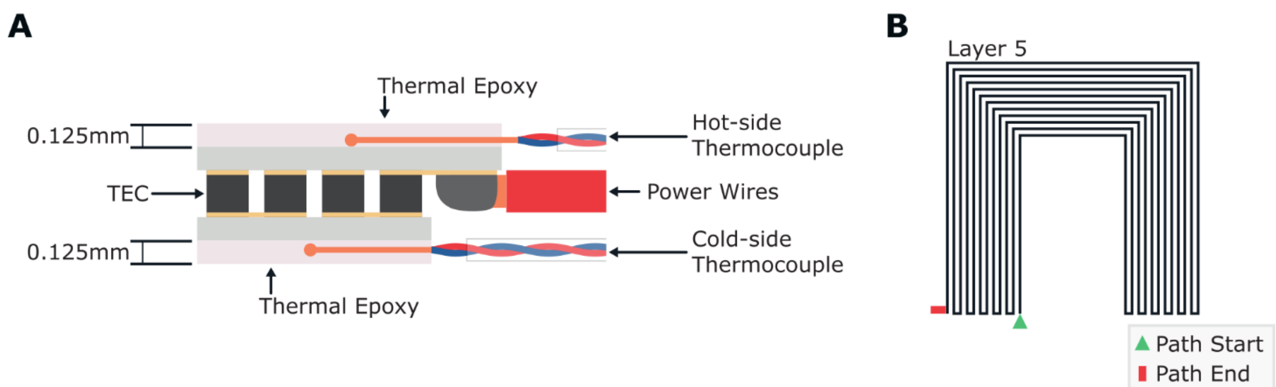


Figure 3.27 No Heat Sink TEC Assembly and print paths.
A. TEC Assembly diagram with the new Thermal Epoxy layer on the hot-side to fully encapsulate the thermocouple and protect it from the coolant flow. **B.** The new pathing for Layer 5. Being a copy of Layer 4, it is included in the Base Section's continuous printing set up. Print markers indicates the paths start and end points.

3.7.4 Version 3 Common Print Paths

Between the two Interface Version 3 variants, only layer 5 required modification to accommodate both design changes. The Base Section and Microfluidic Loop section was the same design for both. Minor pathing changes were made going from the previous Interface version to this version's pathing designs and are detailed as follows.

Base Section

Four layers are again used to construct the Base Section with similar pathing to Version 2 (Figure 3.29A). Differences in the pathing from Version 2 to Version 3 are due to changes in layer 2 and layers 3 & 4. In layer 2, the pathing was swapped to the path used in Version 2's Layer 3. The Base Section channel is made deeper to better accommodate the TEC Assembly wires as there were issues fitting the TEC Assembly flush with the glass slide printing base due to the TEC wires occupying more volume than anticipated.

After consultation with collaborators involved with the future *In Vivo* work, it was suggested that a small lip around the Base Section would aid in Interface placement during these experiments. With the lip being placed underneath the skull edge to anchor the Interface in place or having the Base Section lip as a location to safely loop sutures through. Implementing this suggestion was achieved by removing two outer paths – reducing the paths area without impacting the other Interface sections. Continuous printing can still be applied to the Base Section layers; however, this can only be applied between layer 2 to layer 4. Path start/stop direction has an impact on the final layer print quality for the first layer.

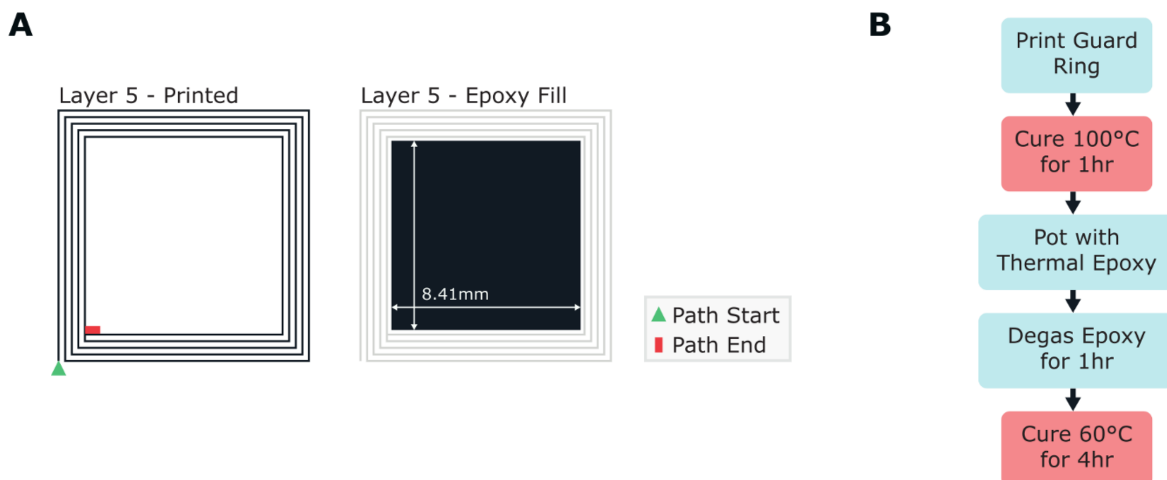


Figure 3.28 Thermal epoxy Heat Sink print path and manufacture.
A. Layer 5 print paths. The printed part is retained from the Version 2 Heat Sink. The printed part is cured before the epoxy fill is cast. Print path markers indicate the path's start and end points. **B.** New manufacturing flow required for the thermal epoxy Heat Sink to be fabricated. An Interface should have the TEC Assembly bonded and cured to the Base Section to start this process.

When printing starts from the inside point on layer 1, there is no supporting material around the 180° zig-zag corners to provide a stabilising adherence. Not having the support material around causes a higher pathing failure rate than if layer 1 was printed from the outside point in. To conform to the continuous printing requirements, the stop point on layer 2 is shortened to overlap with the smaller layer above.

Microfluidic Loop

The Microfluidic Loop layers and print method is near identical to that of the Interface Version 2. The only pathing change is in layer 6 (Figure 3.29B). The outer loop that was put in place as a caution against leaking was removed. Removal was down to the reduce space on the Base Section. This was decided to be acceptable as the Microfluidic Loop already had a low print failure rate before the loops introduction.

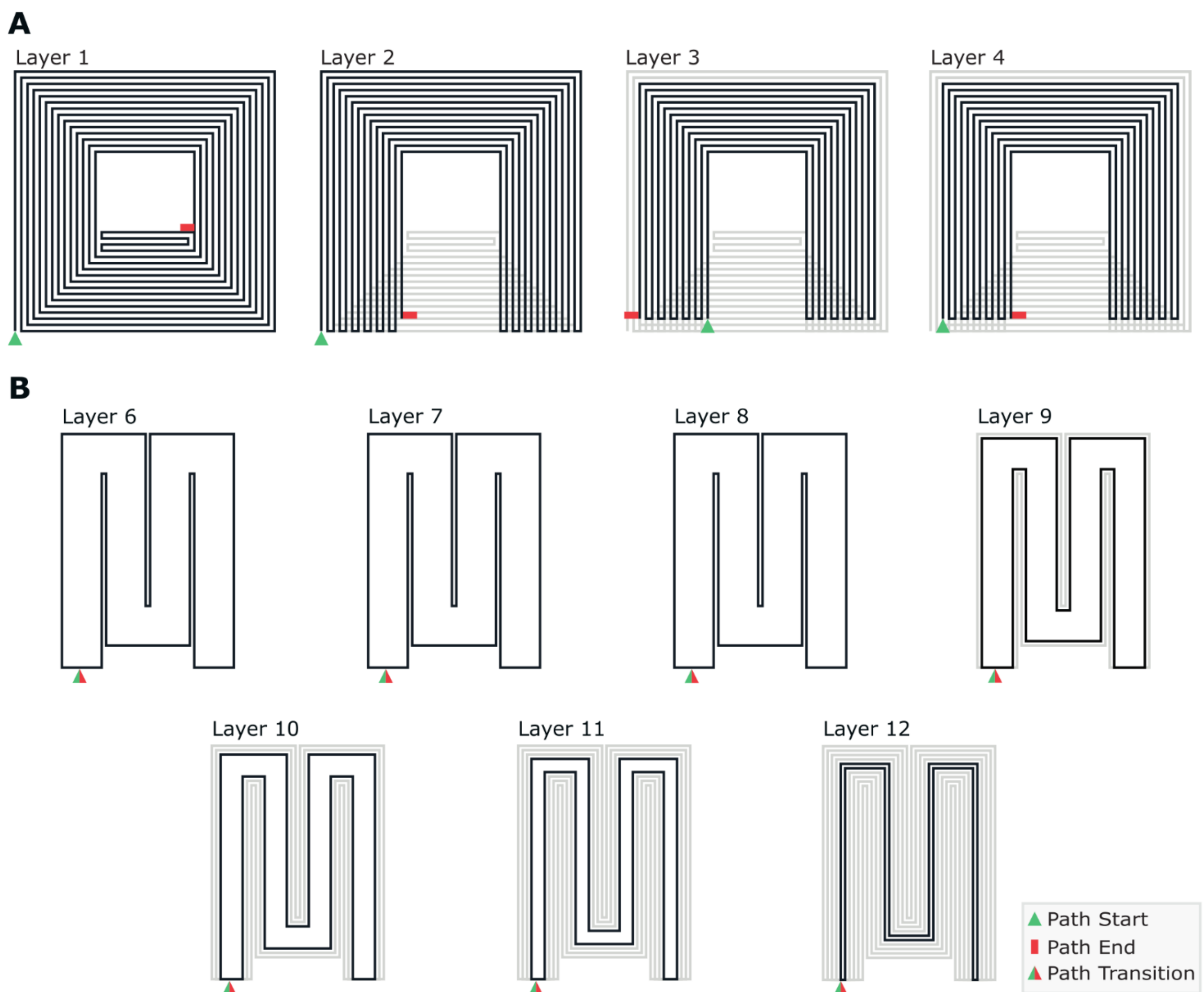


Figure 3.29 Interface Version 3 Base Section & Microfluidic Loop print paths.
A. Constructed with four printed SE1700 layers using the 0.234mm nozzle. Base Section dimensions are 9.80mm x 9.80mm x 0.920 mm. Print path markers dictate the paths start and end. **B.** Modification of the Base Section led to the removal of the extra layer 6 perimeter loop. Print path markers indicate path start and stop locations.

3.7.5 In Vitro Variant Testing

Thermal testing of the two Version 3 variants was undertaken using the same *In Vitro* setup, documented in Section 3.6.3. Both Interface variants had the TEC PID Controller set to proportional mode. The K_p value was set to 5 for their runs to enable comparison to the version 2 data while reducing the risk of system instability. Temperature reference for the Controller was set to achieve a 10°C ΔT. Each cooling run was performed over a 40s window. The TEC was activated a 5s and deactivated at 25s.

Cooling runs undertaken by both designs don't mirror the instability of the Thermal Silicone Composite Heat Sink; though both were unable to reach the set 10°C ΔT. Through comparison of the Interfaces' cooling and power data, the no Heat Sink variant (Figure *3.32*Ai-ii) performs better than the thermal epoxy variant (Figure 3.32Bi-ii). The thermal epoxy variant TEC cold-side temperature was higher on average, and its TEC hot-side temperature was trending upward over the 20s cooling run duration. Based on this hot-side creep upwards, it is predicted that the thermal epoxy heat sink would reach unstable thermal conditions if the run continued. This upwards trend is mirrored in the thermal epoxy variant's power data. On the other hand, the no Heat Sink Interface was able to produce a stable TEC cold-side temperature for the duration of cooling. This variant also required less power to produce this cooling level.

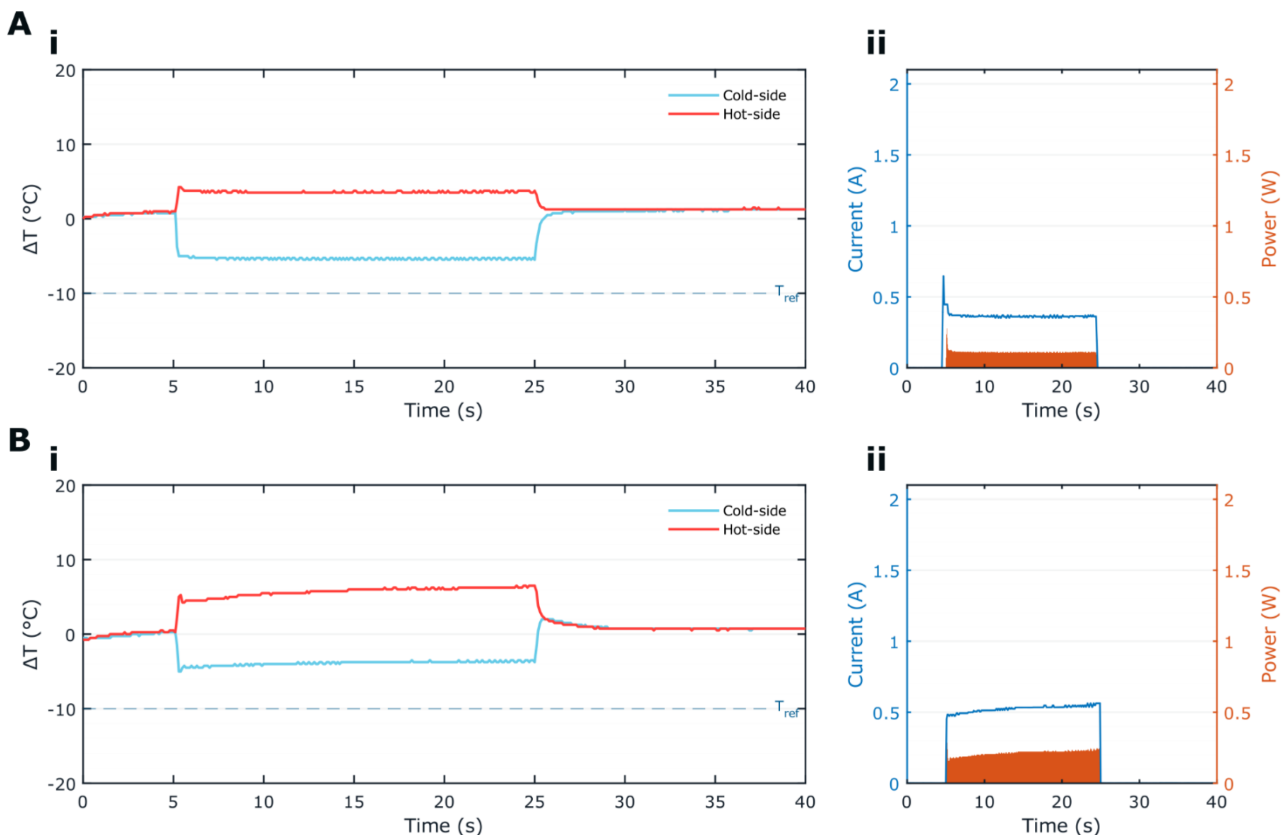


Figure 3.30 Interface Version 3 Heat Sink variant In Vitro profiling.
A. Temperature profiles (**i**) and the power consumption (**ii**) the no Heat Sink design. **B.** Temperature profiles (**i**) and the power consumption (**ii**) the thermal epoxy Heat Sink design. TEC Controller mode is in proportional only for each run with a K_p = 5.

It has then been determined that the Thermal Silicone Composite was major contributing factor in the Interface Version 2's thermal instability. Replacing that Heat Sink material or removing it completely produced two Interfaces that were able to remain thermally stable over the duration of a 20s cooling run. However, both Interfaces were unable to reach the commanded T_{ref}. The TEC Controller was an influencing factor in this, having only been set to use the proportional gain. However, it was determined that an in-depth investigation into the Heat Sink design was needed. For that, *In Silico* experimentation through COMSOL was be undertaken to explore design and materials in a time efficient manner.

3.7.6 Heat Sink Material Consideration

In shifting back to FEM simulation in COMSOL, a new model would be required to be built for exploring the Heat Sink design. Having now access to the TEC technical drawings means that a dimensionally correct version can be reproduced in COMSOL. This reproduction can then be used alongside an imported CAD model of the printed Interface Sections to produce a complete replica Interface in COMSOL. Simulation data calculated with this model would be more representative of the physical system.

In Silico TEC Model Optimisation

Verification of this virtual TEC against a physical TEC would be required to gauge its behavioural accuracy. To achieve this, a setup was devised to operate the TEC in isolation with a hot-side thermal load that would allow the TEC to cool unimpeded.

Physical System

Figure 3.31A demonstrates how this system is setup. A PDMS block is cast from a 3D printed PLA negate to form a mounting point for the TEC sample. In doing so creates a hot-side/cold-side thermal coupling reminiscent of an ideal Interface. Thermal grease (2.9W/m·K) is applied to the TEC cold-side to improve the thermal connection to the PDMS block and encapsulated a thermocouple. Likewise, it is applied to the TEC hot-side for thermocouple encapsulation and to also support a good thermal connection to an aluminium heat sink mounted upon it. This heat sink is held in place using a recess in the cast PDMS.

An FDM-printed superstructure surrounding the PDMS block holds a small 30mm x 30mm fan directly above the heat sink. Constant air flow over the heat sink is driven by this fan at a 6.8m^3/h rate. Thermal data collection and TEC cooling actuation was performed by the TEC Control PCB connected to a PC hosting the relevant LabVIEW control VI. The firmware has a Direct TEC Driver PWM manipulation functionality command coded into it. Direct PWM manipulation facilitates the ability to drive a constant power output to the TEC.

Simulation Model

This entire setup was then replicated within COMSOL. Figure 3.31B displays a captured sliced and 3D model view of the setup. The heat sink was recreated using the CAD software, Fusion360, before being imported into COMSOL via its CAD Import module. The TEC, thermal grease layers, and large block material geometries were created using COMSOL's built-in Geometry creation function. Th fan and the physical setup superstructure were not geometrically replicated. To simulate the fan, the top of the air block was selected as an input that would provide a constant 6.8m³/h flow rate that was derived from the physical fans datasheet. The other four external walls were allocated outlets to mirror the superstructure's open design.

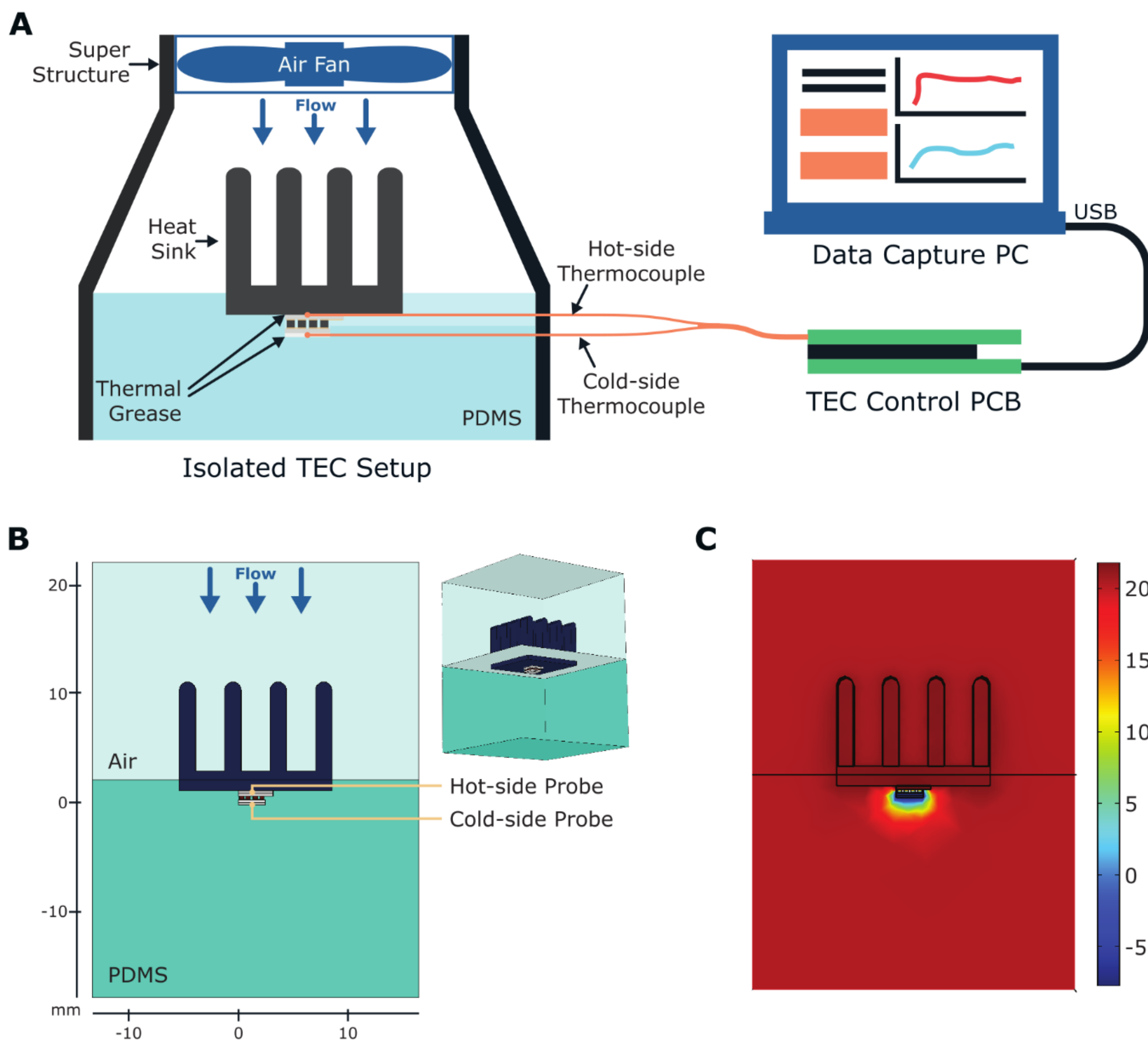


Figure 3.31 TEC System Setup for In Silico optimisation.
A. The physical system setup of the isolated TEC system. Data is collected using the TEC Control PCB and its complimentary LabVIEW data capture system. **B.** Side profile view to of the COMSOL replica isolated TEC system alongside a 3D thumbnail view. Probe locations are labelled. The fan is modelled by an Input Boundary with a constant flow on the Air domains top face. C**.** A heat map output with the TEC input potential set to 0.4V. General function of the system is verified through this.

The custom mesh settings, as used during the CSF simulations, were implemented for this simulation model. Meshing using these settings created a model mesh containing 599877 elements that had a 0.07047 minimum element quality. Air flow was modelled using the Low-Reynolds Number Turbulent Flow physics. All domains were included within the Heat Transfer in Solids and Fluids physics. Each simulation run took ~35 minutes to complete. Base physics setup was verified though running the system with arbitrarily chosen TEC input potentials (0.2V, 0.5V, 0.8V). Figure 3.31C provides a view of the heat map gained from the 0.5V input potential that displays the TEC thermoelectric action being correctly simulated.

System Optimisation and Verification

Tuning the model to fit the physical system was conducted by modifying two bismuth telluride (Bi_2Te_3) material properties – its Seebeck Coefficient and its Thermal Conductivity. Variation of these properties will have a direct influence on the model's function. The Seebeck Coefficient can be used to alter the ΔT the TEC model produced from its driving current, and the Thermal Conductivity will affect the thermal coupling strength between TEC hot-side and TEC cold-side. Both values are temperature dependant so are derived by COMSOL during the simulation. To influence these derived values, a 'Corrective Factor' is added to both properties in the simulation's material section. Through this factor, the properties can be scaled up by the user manually or altered by a parameter sweep during simulation.

To begin the optimisation process, a set of cooling runs were undertaken on the physical TEC system. The cooling runs would last for 40s total - with the TEC being activated at 5s and deactivated at 25s. TEC driver output potential was incremented each run providing cooling sets to provide data sets for 0.2V, 0.4V, 0.6V, and 0.8V. Data from these runs provide the base behaviour of the isolated TEC system. The 0.4V Cooling data set is given in Figure 3.32A. All temperature data collect was done at a 10Hz sample rate from the thermocouples.

A potential sweep within the simulation that used the same TEC potential set as the physical runs was conducted. All potential values produced successful outputs with an example shown in Figure 3.32B – the 0.4V unoptimised TEC model run. Total simulation run time was 2 hours 28 minutes. This run time total lead to the decision to reduce the overall scope of the model optimisation. In proceeding with the current method and under the assumption that a single run would continue to take ~35mins, the next planned simulation run had the potential to take upwards of 12 hours. This would only be the first stage of refinement. The time-cost of tuning every TEC input potential outweighed the gain from achieving a generalised TEC simulation model. A modification was made to the tuning method going forward – the TEC model would only be tuned for one input potential. This potential was chosen to be 0.4V as this was close to the average TEC input potential when testing n Heat Sink TEC (0.31V) and thermal epoxy (0.42V) Interface v3 variants.

Going forward with the 0.4V TEC potential tuning, the next step was to complete two separate simulation runs where each properties Corrective Factor was swept from 1→0 in 0.2 increments. These sweeps determined that the altering the Bi_2Te_3 Thermal Conductivity modified the temperature curves of both TEC sides but did not impact the ΔT in the desired manner. Altering the Bi_2Te_3 Seebeck Coefficient did have a large effect on the ΔT value as expected. Through an iterative simulation process, the Seebeck Coefficient's Corrective Factor converged on 0.35 to produce the temperature profile in that is visually closer to the physical model's profile (Figure 3.32C).

Comparisons were performed between the physical system and the unoptimised simulation to quantify the TEC model's divergence from the physical sample. The temperature error, in °C, was calculated for the TEC hot-side, and the TEC cold-side temperature profiles. Figure 3.32D is the relative temperature error of the unoptimised TEC model to the Physical system. Large temperature profile divergence is seen with a 6.21°C mean hot-side temperature error and a 15.04°C mean cold-side temperature error over the cooling period. The graph also reveals how the temperature profile shaping is not consistent between the systems. This is especially pronounced at the start of cooling on the hot-side and once the cooling period ends on both TEC sides.

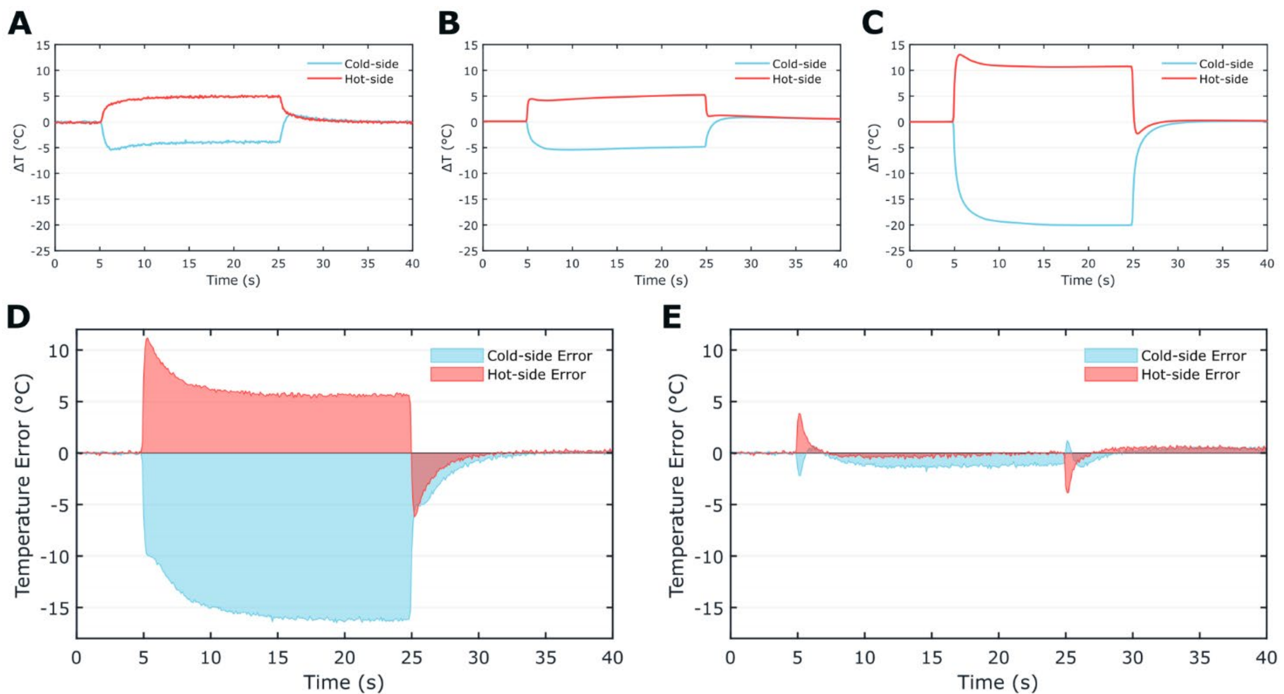


Figure 3.32 Thermal simulation data of the In Silico TEC model optimisation.
A. TEC temperatures recorded from the physical setup with the TEC Driver set to provide a constant 0.4V. This cooling run was replicated in the COMSOL setup with hot-side and cold-side temperatures shown for the: **B.** Unoptimised TEC model, and **C.** Optimised TEC Model. Temperature error of the simulated setup compared to the physical setup before tuning - **D. –** and after tuning – **E.** – the TEC model.

Once the Corrective Factor is set and the resultant data compared to the physical system, the temperature error between the systems becomes Figure 3.32E. Producing a mean temperature error during the cooling run of -0.04°C for the hot-side and -1.07°C on the cold-side. There still exists a multiple temperature profile deviations within the simulation data with temperature error spikes around the cooling run's beginning (3.85°C) and end (-3.86°C). Even with these error spikes, the optimised TEC *In Silico* model represents an improvement in the simulated system achieving near physical system temperature parity.

Limitations of this optimised model should be considered in its future use. The restricted tuning scope results in a system optimised for a specific use case and TEC potential input. It is not a model that could not be used for performing input potential sweeps. Any input potentials (other than 0.4V) will produce temperature profiles of unknown divergence from the physical TEC model. It should also be noted that the physical tuning data was not produce by a perfect isolated TEC system. This system still had external thermal pathways between the TEC hot-side and cold-side through the PDMS block. However, this is representative an ideal in-Interface mounted TEC system making it a use-case specific TEC model. This then makes the model sufficient for producing simulated temperature profiles that can be compared to those previously recorded from the Heat Sink Interface variants.

Metal Heat Sink Simulation

The Heat Sink materials used thus far have not able to provide enough dissipative performance to allow either stable TEC function or for it to reach the minimum required ΔT. Relaxing the Heat Sink material restrictions to now include metals was necessary to find a suitable replacement. Stainless-steel and titanium were chosen as potential replacement materials for the Heat Sink. These two metals are widely utilised medical implants due to their biocompatibility. A new simulation model of a replica Interface Version 3 was built for testing these materials as the Heat Sink. It was designed to combine the previous TEC model tuning with COMSOL geometric elements and imported Microfluidic Loop structure (imported from Fusion360) to produce the 3D system (Figure 3.33A). The overall simulation environment setup mirrors that of the In Vitro setup.

Coolant flow through the loop is modelled using the Laminar Flow physics to reduce computation time. Built-in COMSOL water material properties were used for the coolant. The coolant flow rate was kept constant throughout the simulation at 3.5ml/min. This value was derived from flow measurements taken during *In Vitro* Interface testing using the Microfluidic Centrifugal Pump system (Section 4.7.1). The inlet coolant temperature was 20°C. To replicate the In Vitro setup, the simulation system's initial temperature was set to 37°C. The simulation study timing parameters were kept the same as the previous *In Silico* experiments.

Using the model system described, three separate models were constructed to model the individual Heat Sink types. The first model was the no Heat Sink Interface variant that provides a baseline comparison for the subsequent Heat Sink designs (Figure 3.33B). The second model will simulate a flat metal plate as the Heat Sink – both titanium and stainless-steel materials were tested (Figure 3.33C). In the third model, a finned Heat Sink was implemented in the simulation to discover if the increased surface area would cause an increase in heat transfer rate into the coolant (Figure 3.33D). The fins on this Heat Sink design run parallel to the Loop channels down their centre (length = 5mm). Each fin is 0.64mm tall with a 0.3mm wall thickness. Only titanium was used to simulate this variant as a physical article could be manufactured. Thermal material properties for the 316L stainless-steel alloy and titanium beta-21S were used for modelling their respective simulation runs.

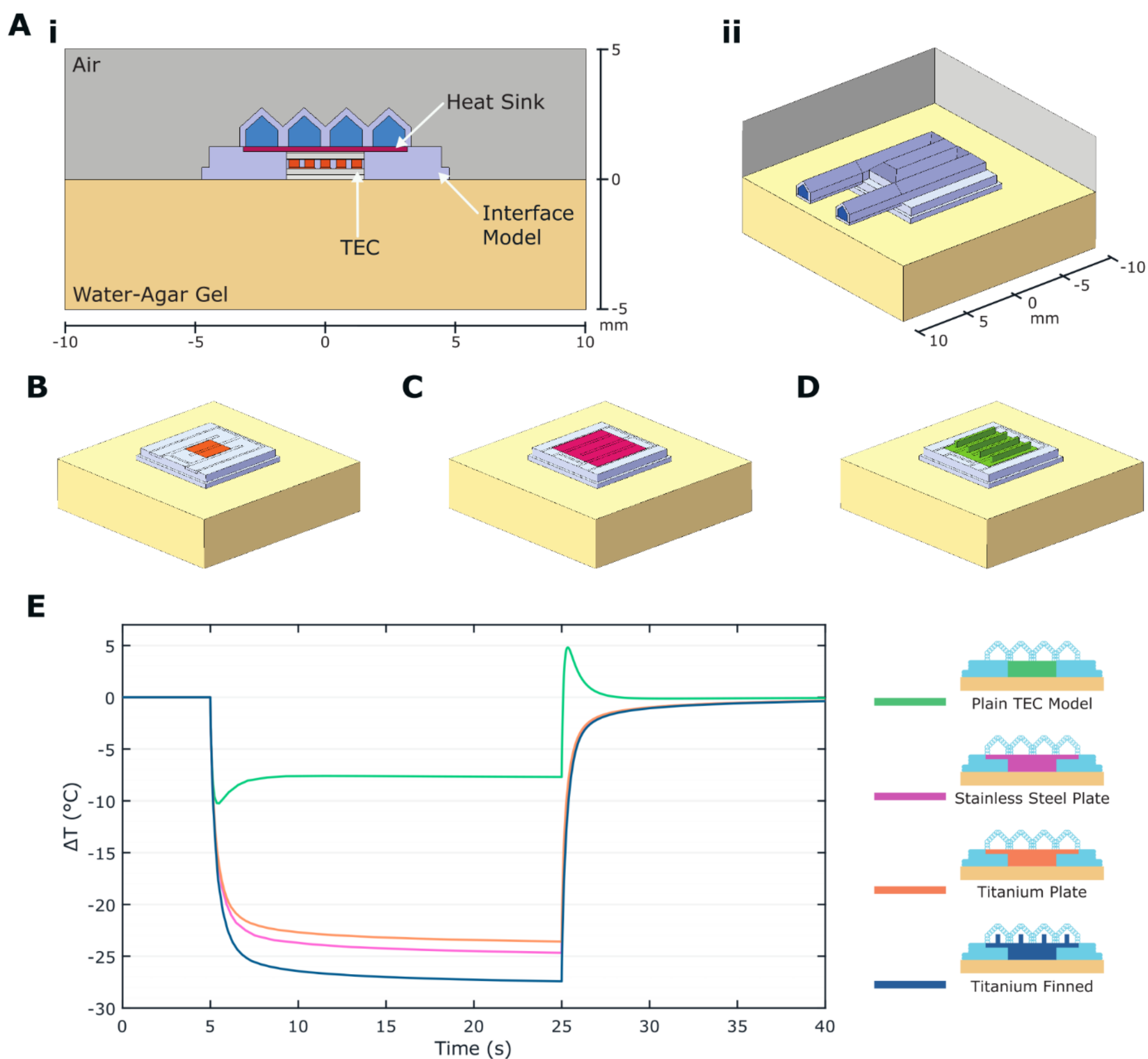


Figure 3.33 In Silico simulation of alternative Interface Heat Sink designs.
A. A cross sectional and 3D view of the Interface simulation model in COMSOL. Labelling indicates the heat sink location used in the stainless-steel and titanium studies. Three Interface model variants used for simulation: **B.** plain TEC model, **C.** metal plate heat sink, and **D.** finned heat sink. **E.** TEC Cold-side temperature profile outputs from the simulation runs. Graph legend is accompanied by an Interface cross sectional diagram of that study's Heat Sink setup.

Of the four simulated system, the maximum mesh element count was 480377 and the minimum mesh element quality value was 0.028. The longest simulation took 1 hour 22 minutes to compute. The metal heat sink group is demonstrated to provide a >15°C ΔT increase in cooling performance on the TEC cold-side compared with the no Heat Sink model within the *In Silico* conditions (Figure 3.33E). This increase could be attributed to the disparity in thermal conductivities between the metal materials (stainless-steel = 14.5W/m·K, titanium = 7.5W/m·K) and the thermal epoxy (1.3W/m·K) on the no Heat Sink model. Though a cold-side performance increase of this magnitude was not noted between the titanium and stainless-steel even though there is a doubling of the thermal conductivity property from the former to the latter. This could indicate that the Interface Heat Sink performance is reaching the limit in the ΔT performance increase that a material modification can achieve.

As this Heat Sink material limit is reached, other aspects of the thermal system design start to become the dominant limiting factor. These elements could include coolant flow rate over the Heat Sink and/or the heat transfer efficiency from the Heat Sink to the liquid coolant. The effect of increased heat transfer efficiency is demonstrated in the titanium finned Heat Sink output. The fins increase the contact surface area between the Heat Sink and the liquid coolant that results in an increase in heat transfer efficiency. This increase translates to a 3.85°C ΔT gain on the TEC cold-side compared to the titanium plate design.

Simulation results give a clear indication that moving to using metal in the Interface Heat Sink design will provide substantial increase in achievable ΔT compared to that of the no Heat Sink Interface design. Due to the simplified nature of the *In Silico* study, the simulated achievable ΔT performance of the metal Heat Sink Interfaces cannot be expected to be realised 1:1 once a physical model has been produced. However, due to the magnitude of the ΔT performance increase, there is an error buffer of 7°C between the *In Silico* Interface and *In* Vitro Interface's thermal responses. This performance buffer gives confidence that an Interface manufactured with a metal Heat Sink can achieve the minimum specified Interface ΔT.

3.7.7 Metal Heat Sink Fabrication

With the *In* Silico study validating that metal-type heats sinks, realising this in the Interface design required an adjustment to the print paths around Heat Sink, and the TEC Assembly. The initial implementation of a metal heat sink would use the plate design. The plate was 6.2 x 6.2mm and ~0.2mm thick. On layer 5, an extra two path loops were added to the interior as shown in Figure 3.34A. Adding thickness to this 'guard ring' around the metal Heat Sink provides a greater safety margin for reliable encapsulation by the printed SE1700 – preventing it from being exposed to the external environment.

For this Interface test sample, the Heat Sink would be manufactured out of 0.2mm Type 304 Stainless Steel foil (Fisher Scientific, UK). This particular formulation of stainless-steel has a thermal conductivity of 16.5W/m·K. Using a pair of tin snips, stainless steel plates were hand cut out from a sheet to the required size. Through the gradual removal of excess material, a ±0.15mm tolerance could be achieved (n=8). The plates are bonded flush to the TEC hot-side surface using the thermal epoxy. The hot-side thermocouple had to be relocated to the position marked in Figure 3.34B. Having the thermocouple located against the Heat Sink, the thermocouple's exposed tip had to be pre-treated with a thin layer of thermal epoxy to electrically isolate it. When the TEC Assembly was to be bonded into the Base Section, the SE1700 would now have to cover the Heat Sink's underside face - where the thermocouple attached - to prevent air voids. The 0.2mm plate height ensures that, once the layer 5 guard ring is printed, the plate's top face would sit flush with the top of the guard ring (Figure 3.34C).

This first Heat Sink design used stainless-steel due to the ease of processing within the lab. Whilst the metal Heat Sink sample was being fabricated, an exploration was performed into the manufacture of the finned heat sink - if it were to be implemented in the future. Machining the finned heat design out of stainless steel or titanium at the 100μm scale presents a challenging endeavour due to the materials hardness. However, advances in metal-based 3D printing technologies could potentially remove this challenge.

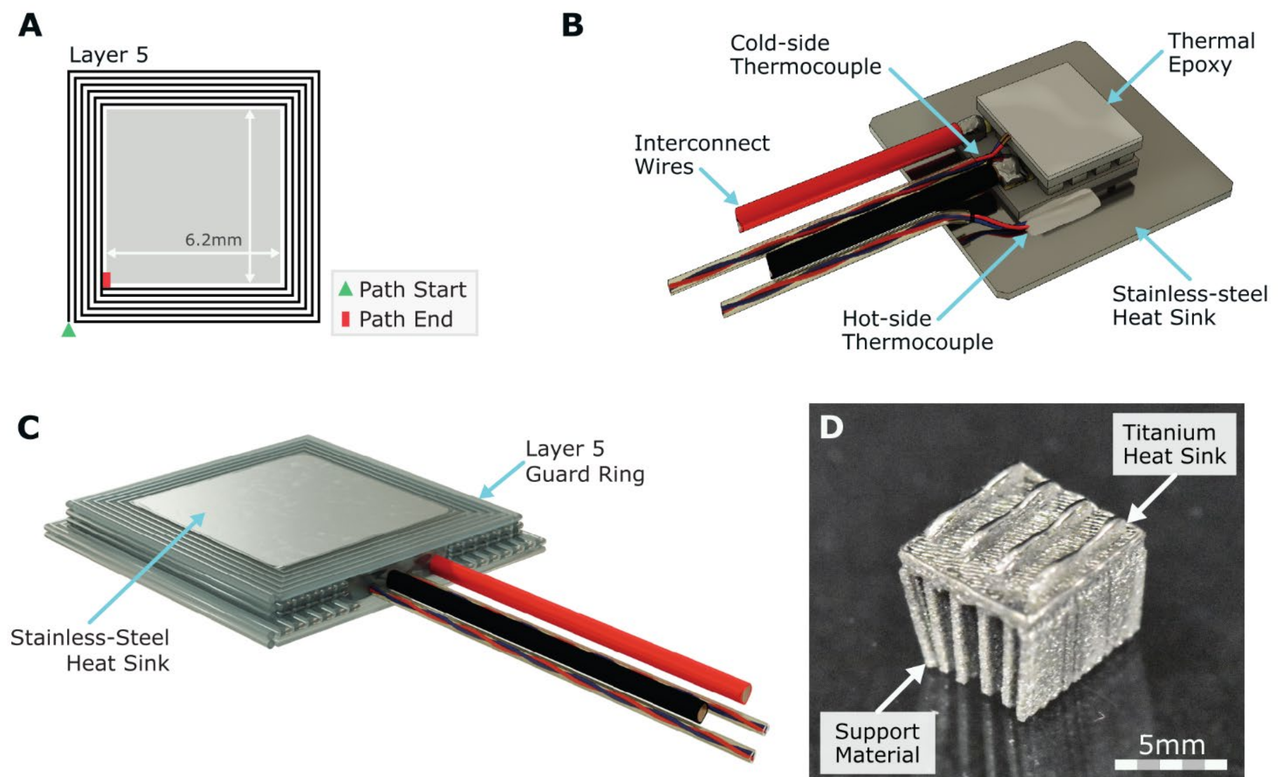


Figure 3.34 Stainless-steel Heat Sink for the Interface Version 3.
A. Layer 5 print path alteration to spiral print to the Heat Sink 6.3mm x 6.2mm dimensions. **B.** Altered TEC hot-side thermocouple location as indicated on the new TEC Assembly's design render. **C.** Base Section render with the TEC Assembly bonded into it. The metal heat sink face will sit flush with the Layer 5 guard ring that is printed after the TEC Assembly is bonded in. **D.** A finned Heat Sink sample that has been 3D printed out of a titanium alloy using Powder Bed Fusion techniques.

In collaboration with the Advance Manufacturing Research Centre (AMRC) at the University of Sheffield, Powder Bed Fusion (PBF) 3D printing techniques was used to produce a titanium alloy prototype, finned Heat Sink (Figure 3.34D). This sample piece's minimum feature size is at the lower limit of the what the AMRC printers can reliably achieve (~100µm); however, this fabricated output is confirmation of this process's validity. With further printing optimisation, this process is a potential future direction for investigation into Heat Sink manufacture and thermal optimisation.

The final fabricated test sample of the Interface Version 3 variant with the stainless-steel Heat Sink in pictured in Figure 3.35A. Dimensionally there are no changes from the previous Version 3 variants. An additional TEC hot-side thermocouple had to be remedially added to this sample after the original hot-side thermocouple malfunctioned after TEC Assembly bonding to the Base Section. Alignment of the stainless-steel Heat Sink under the Microfluidic Loop was checked post-manufacture through underside illumination (Figure 3.35B). This visual inspection indicates good alignment that ensures coolant will flow over the majority of the heat sinks face bar the surface area taken up by the printed channel wall footprint.

In Vitro Testing

The Interface Version 3 stainless-steel Heat Sink variant was mounted in the *In Vitro* thermal testing setup and ran through a series of cooling runs to gauge it maximum achievable ΔT. These cooling runs replicate those ran for the previous Interface variants. The runs provided validation of the stainless-steel Heat Sink design with a maximum -17°C ΔT achieved from system ambient by the TEC cold-side (Figure 3.36A). It is seen to reach this ΔT rapidly after the TEC On event at 5s and is maintained in a stable fashion until the TEC is turned off at 25s.

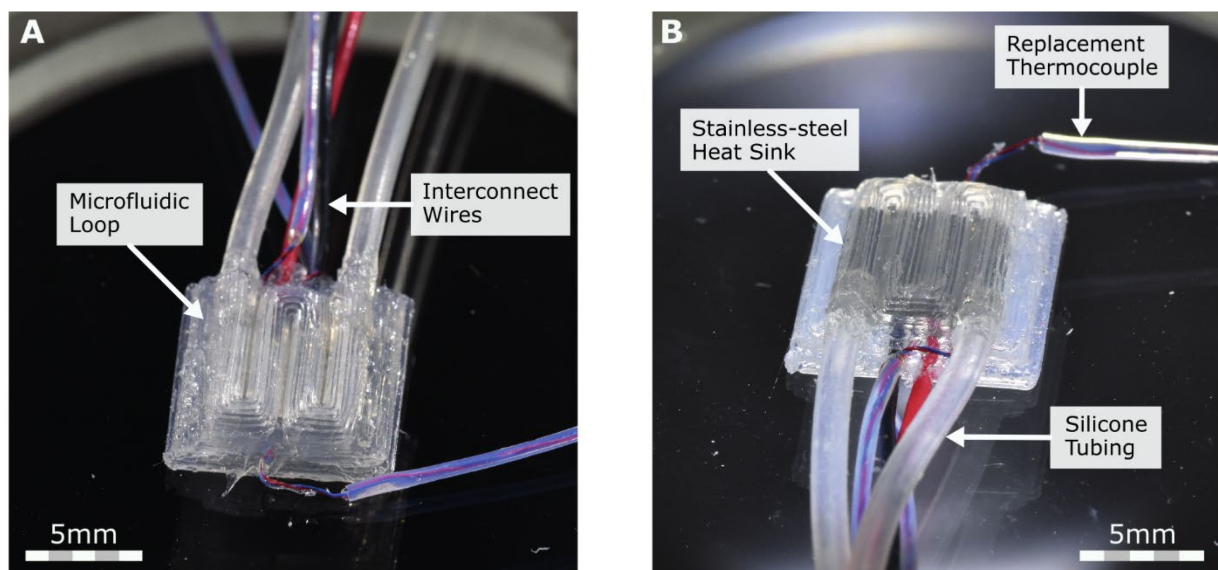


Figure 3.35 Interface Version 3 with a stainless-steel Heat Sink.
A. The completed Interface sample. An replacement thermocouple has been inserted due to a malfunctioning hot-side thermocouple. **B.** An under-lit Interface view where the new stainless steel Heat Sink silhouette can be seen encapsulated within the printed Interface body.

To reach the maximum ΔT, the K_p value was adjusted up to 20. This meant that the TEC ended up being supplied the maximum output from the TEC Control PCB during the entire activation period (Figure 3.36B). Even so, the TEC hot-side was seen to also have its temperature reduced below the system nominal. This meant that only a ~9°C ΔT was achieved between the TEC hot-side and cold-side. From this smaller than expected TEC cold-side/hot-side temperature difference, it was surmised that a fabrication defect could have caused a greater thermal coupling between the two TEC ceramic plate. The culprit was likely to be the thermal epoxy. Application of the epoxy in future Interface fabrication will have to be carefully monitored to prevent this issue occurring in future samples.

Implementation of the stainless-steel Heat Sink has allowed a stable 12°C ΔT performance increase over the Interface Version 3 no Heat Sink TEC variant. Future Interface designs will integrate this metal Heat Sink into the TEC hot-side heat dissipation system. Adding a metal plate into the Interface will reduce bulk Interface flexibility and ability of it to conform to variable surface geometry. However, with the metal plate being embedded within soft silicone material, there would be no direct contact with surrounding biological tissue. Having the silicone still being the main Interface/tissue boundary material should still provide a reduction glial scar build up at the implantation site during its lifetime.

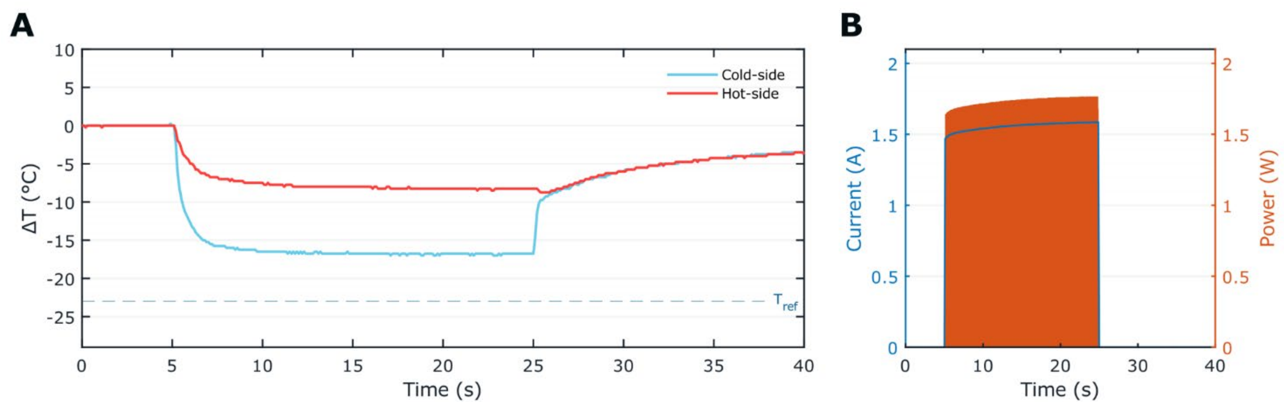


Figure 3.36 In Vitro profiling of the stainless-steel Heat Sink Interface.
A. Temperature profiles recorded during the *In Vitro* testing of the stainless-steel Heat Sink variant of the Interface v3 design. T_{ref} = 23°C and K_p = 5. **B.** Power consumption over this 20s cooling period.

3.8 TEC Power Wire Selection

Up until this point, the TEC units used during Interface construction were pre-soldered with 40mm long, 0.7mm OD wires on the TEC+ and TEC- pads by the manufacturer. These wires were too short and rigid for future Interface testing within a *In Vivo* experimental setup. An alternative wire type was needed as a replacement.

The replacement wire would be required to support the TEC's maximum input (I_{max} = 2.4A, V_{max} = 1.4V). Wire selection must then be carefully considered as the intention was to have the wire be thin and flexible to prevent cable size creep effecting the Interface. With that desire came the issue of joule heating, as a wire's resistance is inversely proportional to its diameter. To prevent thermal damage to tissue surrounding the Interface, the allowable temperature increase that the TEC wire can exhibit would have to be strictly bound. The specification set for wire selection is that a 2A, steady state current should not cause a temperature increase of more than 2°C. This was to keep the wire temperature within the normal physiological range for neural tissues [139].

Seven candidate wire types were procured for testing. This selection contained four different wire core materials, and five different wire gauges (Table 3.1). To test this selection, a 2A constant-current source was built specifically to undertake the TEC wire testing process safely. As a safety measure, the source would switch to be constant-voltage source if a 5V potential was unable to produce a 2A current flow through the wire sample. The constant-current source electronics were mounted into a 3D printed enclosure on which two insulated crocodile clips were mounted 50mm apart.

Table 3.1 TEC power wire candidate selection and performance details.
The platinum iridium wire was procured from Alleima, Sweden (formerly Sandvik Materials Technology) and the other wire samples procured from Cooner Wire, USA.

Wire Type	Core Material	Size (AWG)	Peak Current (A)	Wire Temperature (°C)		Temperature Difference (°C)
				0s	5s	
Pl/Ir	Platinum Iridium	38	1.05	20.4	59.7	+39.3
AS155-28 Blk	Silver-Plated Copper	28	1.946	20.5	20.9	+0.4
CZ1105	Copper	28	1.946	20.8	22.3	+1.5
CZ1320	Copper	30	1.945	19.9	21.7	+1.8
AS816	Stainless Steel	28	1.05	19.7	54.2	+34.5
AS814	Stainless Steel	30	1.45	20.5	60.1	+39.6
AS636	Stainless Steel	32	1.45	20.7	59.4	+38.7

The wire study was undertaken by first cutting 60mm lengths of each wire and stripping 5mm of insulation from each end of the wires. These were then sequentially mounted onto the crocodile clips for recording its thermal output. A multimeter (U1241C, Keysight Technologies) was linked in series with the wire to measure the wires current flow and a thermal camera (FLIR C5, Teledyne Flir) was set up 300mm away from the setup to measure the wire's temperature. Thermal images were captured at a 10Hz rate during recordings. When testing a wire, the current source was activated at 4s into recording. It was left on for a ~30 second period. After this period, it was switched off. In the case of extreme temperature increases, the constant-current source was switched off earlier.

The thermal image set from each recording were used to compile a heating profile for each wire (Figure 3.37A). Through these images it is seen that wire heating does occur evenly across each wire sample. Once the maximum wire temperature per frame is plotted, it can immediately be recognised that the stainless-steel and the platinum iridium wire were unsuitable for use (Figure 3.37B). The lowest temperature during active current flow within this group was 54.2°C – representing a +34.5°C ΔT from ambient. On the other hand, the highest temperature change produced in the copper-core wires was +1.8°C. All copper-core wire samples then remained below the specified maximum temperature increase and can be considered for use.

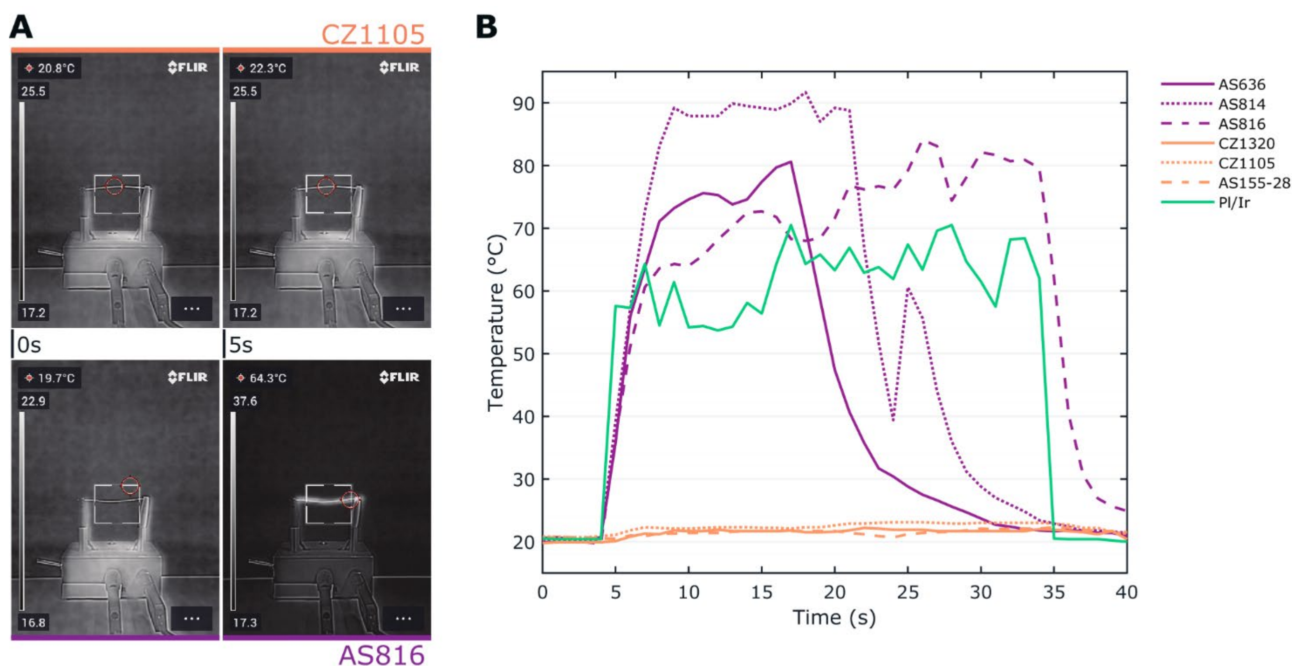


Figure 3.37 Thermal profiling of prospect Interface power wires.
A. Thermal images pairs for a copper cored wire (CZ1105) and stainless-steel wire (AS816). These pairs display the maximum wire temperature before the application of current and after 5s of current flow. Maximum temperatures sensing is restricted to the marked box over the wire to prevent reading contamination. **B.** Graphed wire temperature profiles over a 30s supplication of the maximum specified current draw by the TEC model used in the Interface. Temperatures were logged from each frame over the current application period.

Utilisation was considered of the CZ1105 and AS155-28 wires. Both recorded the lowest temperature increase of +1.5°C and +0.4°C respectively. They were used to produce two Interface Version 3s (stainless-steel Heat Sink) to check the wires manufacturing compatibility. The Interface wire channel has a 0.69mm x 3.43mm cross section that must accommodate all current and future Interface interconnect wiring. During the Interface sample fabrications, it was noted that the AS155-28's nominal wire diameter of 0.889mm made it difficult to place within the wire channel's restricted space. There being no such issue when using the CZ1105. As wires for the Interface Electrodes are still to be added to the interconnect wire bundle, the decision was taken to use the CZ1105 for the TEC power delivery wires.

However, it is noted that copper is not suitable for long-term implantation. System prototyping will maintain the use of copper-core wires over the Interfaces development. It is planned that these TEC power wires will be replaced with gold-core wires once the entire system's viability is proven. The conductivity of gold (4.11×10^7 S/m) is still comparable to that of copper (5.96×10^7 S/m). Gold is commonly used in electronics as a non-corrosive and low reactive replacement for copper. A gold wire fabricated using the CZ1105 stranded specification is calculated to present ~0.271 Ω/m. Since the CZ1105 presents 0.197 Ω/m and the CZ1320 presents 0.361 Ω/m, it is then estimated that a gold wire around the cross-sectional size of these wires would produce a temperature increase within specification.

3.9 Interface Version 4

The Interface Version 4 design is primarily a refinement of the Interface Version 3 metal Heat Sink variant. The focal cooling aspect of the Interface was deemed to be mature enough to begin the steps towards integrating the electrocorticography (ECoG) neural recording functionality. This resulted in four printable electrodes being deployed in an X configuration across the TEC cold-side face. Using the hardware described in Section 4.5 , these printed electrodes are utilised in a bipolar configuration for recording neural signals.

Alongside the electrode integration, smaller design refinements were undertaken to ease Interface handling and construction. A connector was added onto the Interface interconnect wires to shorten the interconnect wire lengths hard-wired onto the Interface. The IT-1E (Physitemp, USA) thermocouples were replaced with 5TC-TT-TI-40 (OMEGA, USA) thermocouple. These replacements were the same T-type sensors but easier to source and were supplied without the mini thermocouple connectors that the previous sensors had. These changes are visualised through the Interface Version 4 render in Figure 3.38.

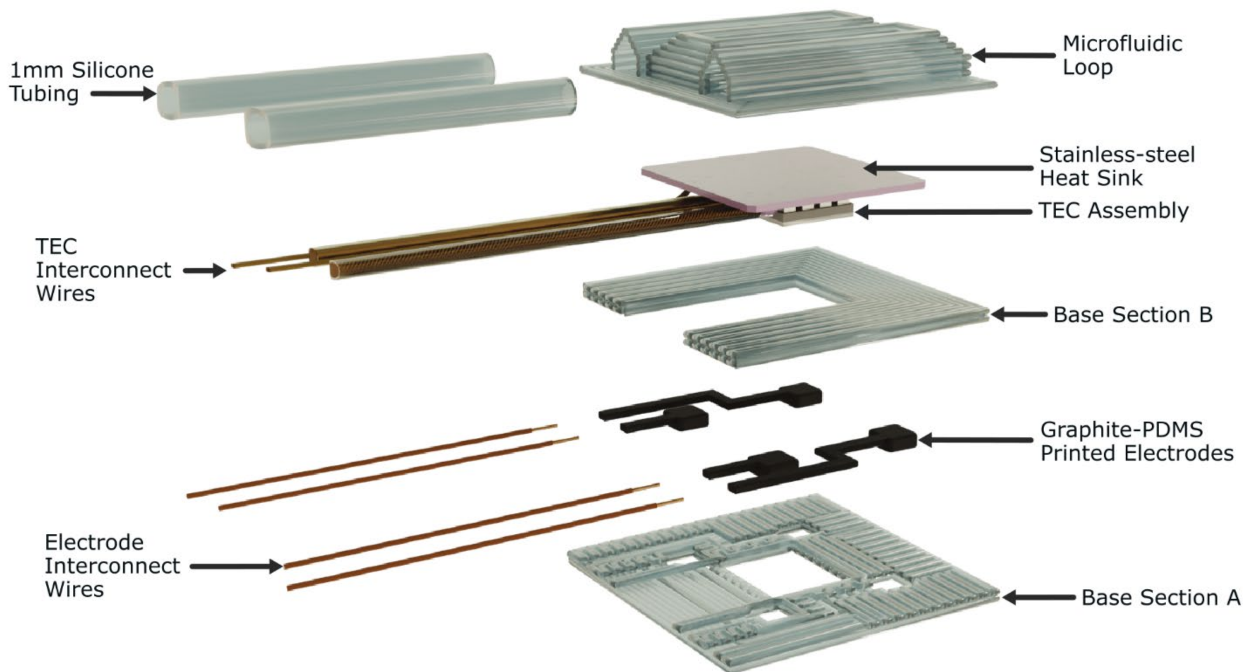


Figure 3.38 Interface Version 4 design visualisations.
TEC Assembly for Version 4 uses the stainless-steel Heat Sink design. Changes to the Base Section are noted due to introduction of the neural recording modality via printed Graphite-PDMS composite electrodes.

A total of twelve Version 4 Interfaces were produced for experimentation (Figure 3.39). With the integration of the neural recording modality, the Interface design reached the stage where it was viable to undertake *In Vivo* testing. As progression was made onto this next verification stage, the Interfaces were now allocated numbers to help with logging during use. Interface 8 was the first Interface of the Version 4 series to be used *In Vivo*. Interface's 10, 11, and 12 were the other fabricated Interface that were also used for *In Vivo* studies.

3.9.1 ECoG Electrode Integration

In producing an Interface that could achieve the temperature differences specified, it was now required to integrate electrodes into the design to accommodate the neural recording modality. The intention was for the Interface electrodes to be 3D printed within the same print instance as the Base Section. Producing the electrode in this manner would prevent major disruptions to the current Interface design and construction flow.

To allow this the Graphite-PDMS Composite (G-PDMS), developed in lab for 3D printing purposes, will be utilised [140]. G-PDMS is an electrically conductive material that presents greater mechanical compliance than metal-based electrodes do. This increased compliance tends to result in the slower formation of shear-induced scar tissue build up around an electrode as compared to using a mechanical stiffer materials [141].

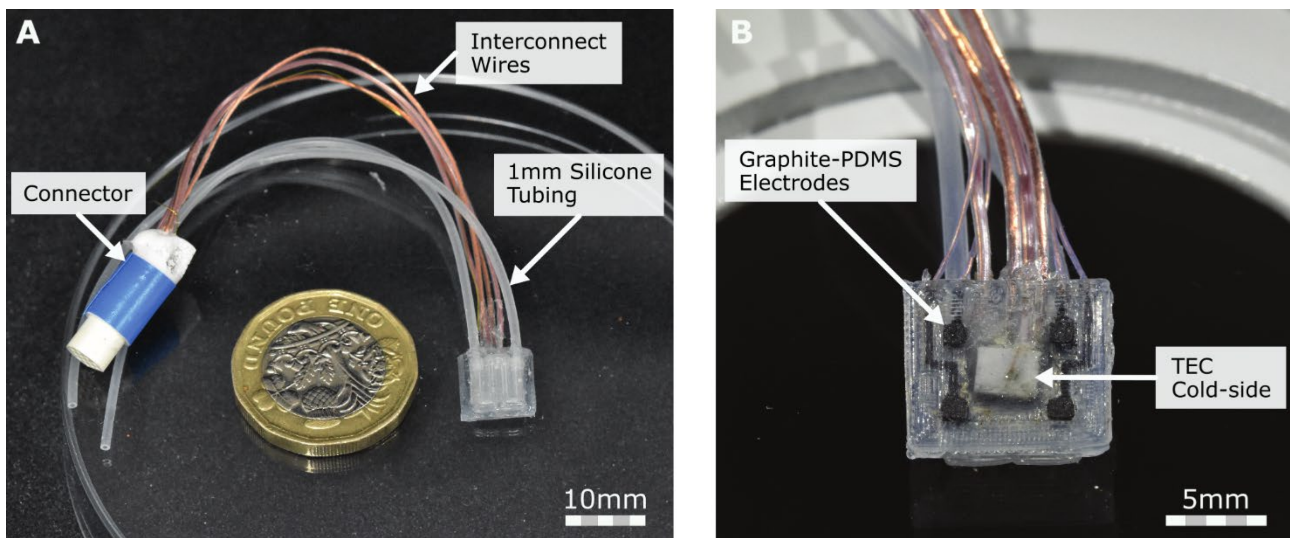


Figure 3.39 Fabricated sample of the Interface Version 4 for In Vivo Study
A. A full Interface sample view with an attached Omnetics connector. The printed Interface measures ~9.5mm x 9.5mm x 2.3mm. Scale is provided through comparison to a £1 UK coin. **B.** The underside of the Interface Version 4. Displaying the central placed TEC cold-side surrounded by four graphite-PDMS electrodes at each of the TEC's corners.

Electrode Configuration

Electrodes for neural recording are commonly presented in two configurations – unipolar and bipolar. Consideration of both is required as it will affect the dominate information contained within the captured signals and will inform the electrical hardware require to record the signals.

Unipolar recording is performed using a single electrode at the site of interest. Recording of the desired signal is achieved through point samples of the electrode's potential that is reference to another electrode (Figure 3.40A). This reference electrode is generally located in an area of low electrical activity to provide a stable biological grounding reference. Signals recorded from a unipolar setup are directionally non-specific and contain information of both local and far-field signal components. However, unipolar electrodes are susceptible to electrical noise due to having no way to reject it. This noise has to be removed during processing using of signal filters.

On the other hand, bipolar electrodes use an electrode pair located close together at the site of interest. For this configuration, recording is achieved by sampling the difference between the two electrodes potentials that is referenced to the biological grounding reference (Figure 3.40B). Any common-mode signal components sampled on the electrodes are attenuated whilst differential-mode components are retained. This results in a signal that – ideally - only contains the local signal components. Though in a practical system the common-mode signals are just greatly attenuated compared to the differential signal.

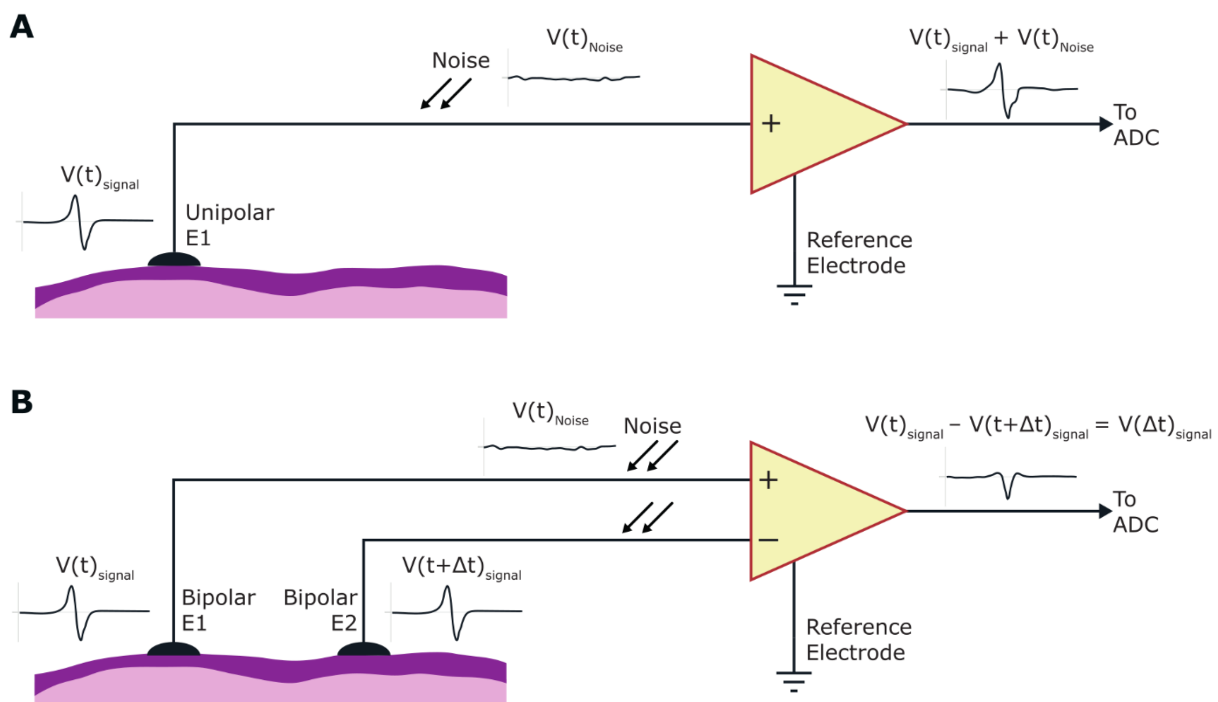


Figure 3.40 Electrophysiological electrode recording configurations.
A. Unipolar recording setup. Only one electrode is sampled in reference to an electrode placed on electrically quiet tissue. Output is the recorded activity plus system noise. **B.** Bipolar recording setup. Two electrodes are used to sample offset signals in the same area. The difference of the signals is taken to retain the local components and reject common-mode signal components including noise. All signals are recorded in reference to an electrode placed on electrically quiet tissue.

Bipolar electrodes then provide excellent electrical noise rejection properties without requiring signal filters. However, this configuration is highly directional. As the direction a signal travel tends toward being perpendicular to the bipolar electrode axis, it becomes more common-mode until it is fully rejected. Depending on the signals required, this behaviour can be a positive or negative.

For the Interface electrodes, a bipolar configuration was chosen. One of this PhD's aims is to produce a system with a high degree of clinical readiness. In the clinical environment, noise conditions aren't as manageable or controllable when compared those in experimental setups. Thus, having a robust recording system with innate noise rejection presents the preferred route.

When integrating the Interface electrodes, the intended 3D printed fabrication imposes limitations on electrode placement locations. Areas directly under the TEC are unavailable and, to ensure electrical isolation, the electrodes have to maintain at least one SE1700 layer from the external perimeter and the internal TEC insert perimeter (Figure 3.41A). There also must be at least one SE1700 path barrier between each electrodes printed material. With the aid of Dr Thomas Paterson, a four-electrode layout that fit these rules was produced (Figure 3.41B). Each electrode is placed at one of the four TEC cold-side corners to form a symmetrical pathing pattern across the Interfaces centreline. The electrodes are designed to be recorded in diagonal bipolar pairs that form an X pattern across the TEC cold-side face. These near perpendicular pairs ensure that all local directional components are recorded during signal.

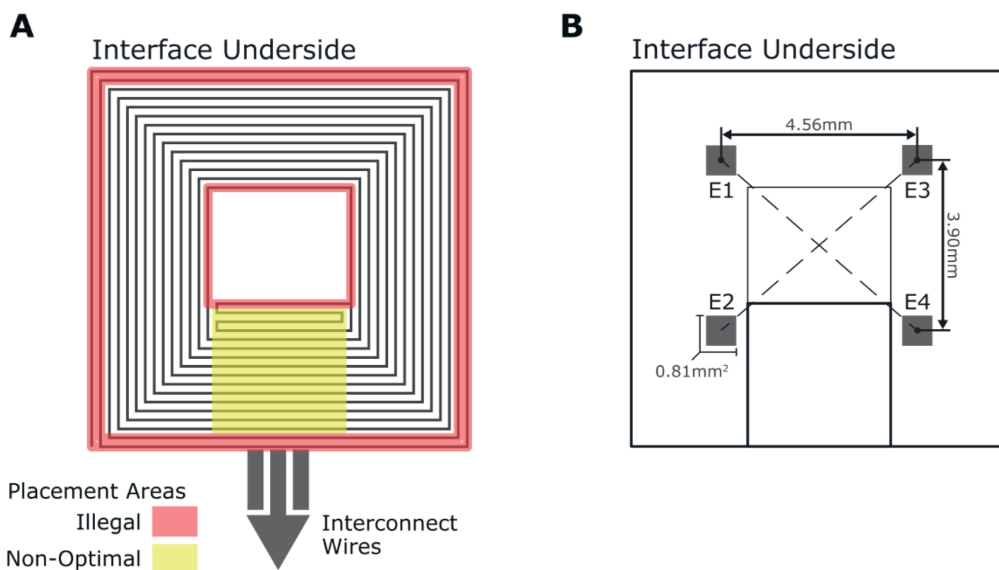


Figure 3.41 Interface electrode placement and dimensions.
A. Regions of layer 1 where the Electrode cannot be placed (the red, illegal zone) or would require careful consideration (yellow, non-optimal zone). Non-highlighted areas indicate potential electrode location. **B.** The locations of the four Interface electrodes. Four 0.81mm^2 electrodes form a 4.56mm x 3.9mm square relative to its centre points. These form two pairs, E1-E4 and E2-E3, to record across the TEC Cold-side face.

Printed Electrode Fabrication

To integrate the electrodes into the Interface, the pathing for them is required to be placed on both Base Section layer 1 and layer 2. These two layers underwent major re-pathing to accommodate the electrodes whilst retaining a single continuous layer print path (Figure 3.42A). For the electrode print paths, three separate paths are printed over layer 1 and layer 2 as demonstrated in Figure 3.42B. First, on layer 1, a single G-PDMS loop is deposited in the electrode void to produce the electrode face. On layer 2, a second loop is printed to fill the remaining electrode void volume. To then connect these printed electrode faces to the interconnect wires, G-PDMS is used to fill the internal electrode print channel that ends at the edge of the Interface. By having this internal channel of conductive material on the second layer, it remains insulate from the surrounding neural tissue and prevents biological noise being added to the recorded signal.

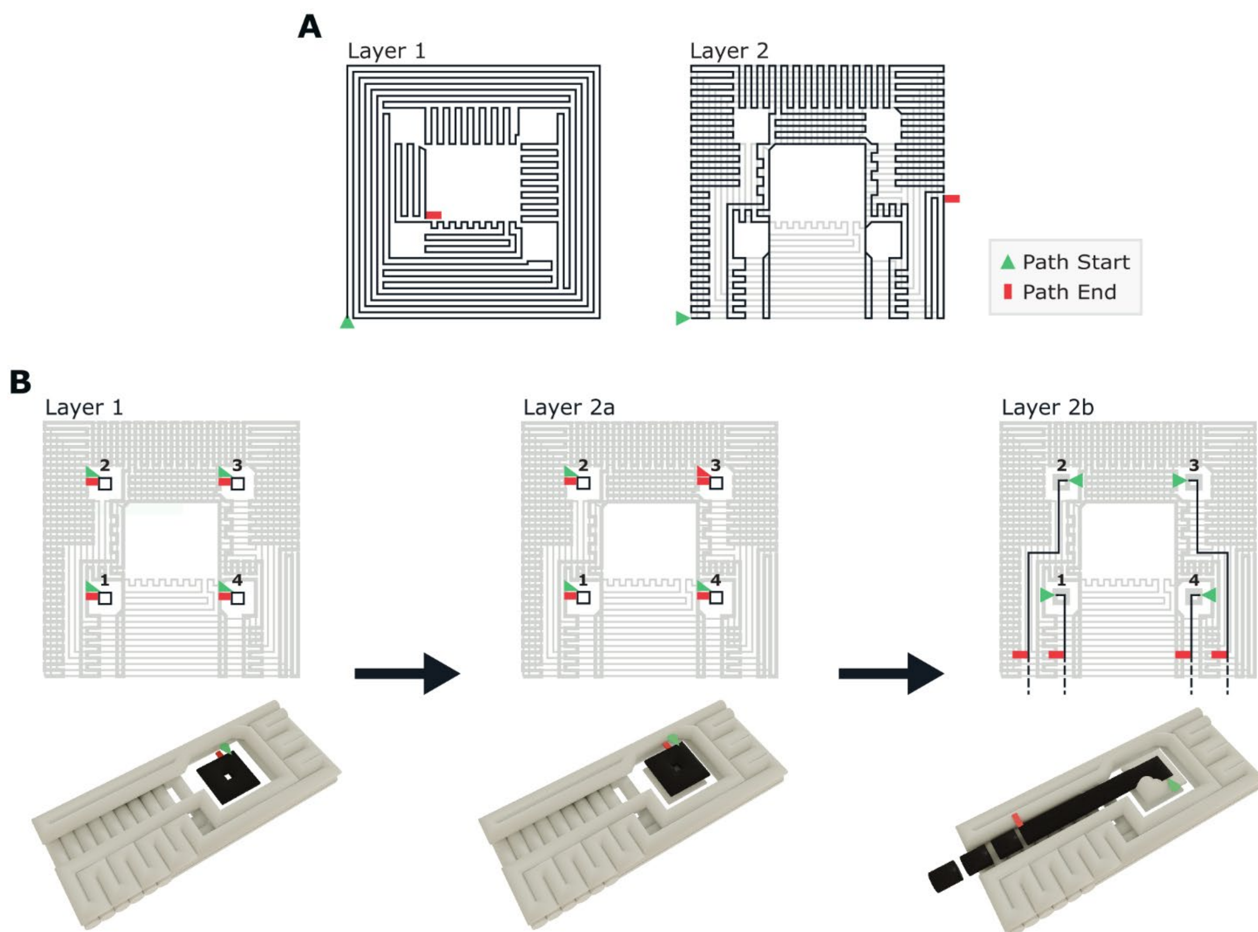


Figure 3.42 Pathing and manufacturing of the Interface electrodes.
A. Base Section layer 1 & 2 pathing modifications necessary to form the electrodes. Layer 1 has the square electrode face void printed within it. Layer 2 has the internal electrode print channels to route the electrode connections to the Interface edge. Each layer is still pathed with one continuous path. **B.** Print paths for the four electrodes. Print order is marked for each electrode. Renders of each print stage provide the 3D context to the electrode printing into the part-cured Base Section layers (in grey). Coloured markers indicate the start and stop of each path. The dashed path on the electrode Layer 2b is the programmed nozzle travel direction when materials extrusion is stopped to reduce electrode material delamination during printing.

The 50wt% Graphite PDMS Composite mix was selected for the printed electrodes. This G-PDMS mix exhibits the highest conductivity whilst retaining the ability to be printed at the Interface resolution. The viscosity of this mix required the use of a 0.457mm dispensing nozzle on the 3D Discovery's volumetric printhead to achieve consistent extrusion behaviour. A 0.230mm layer height can still be retained with the larger nozzle diameter without issue - as was with the Thermal Composite printing.

Bridging the printed electrode to the recording hardware necessitated the use of thin interconnect wires. These would be installed into the electrode channels once the Base Section layers 1 & 2 had been partially cured at 100°C for 40 minutes (Figure 3.43). The partially cured SE1700 has a tacky surface which is used to hold the interconnect wires in place whilst the electrodes are printed. This tackiness also provided better adhesion characteristics between the Base Section layers and electrode material. Once the Interface is full constructed, the electrode interconnect wires can be soldered into the Interface connecter. All electrodes are tested for continuity after they are fabricated to allow for any remedial action to be taken if any wire connection faults are discovered.

To prevent damage to the electrode face's when an Interface is removed from the glass slide it was printed on, a layer of a silicone-based conformal coating was now applied to slide pre-printing. This conformal coating allowed an Interface to be easily removed post-fabrication rather than the scalpel slicing method utilised previously. The peel force required for Interface removal exceeds any force experienced by the Interface during printing. This ensures that the print location will remain consistent during the fabrication process.

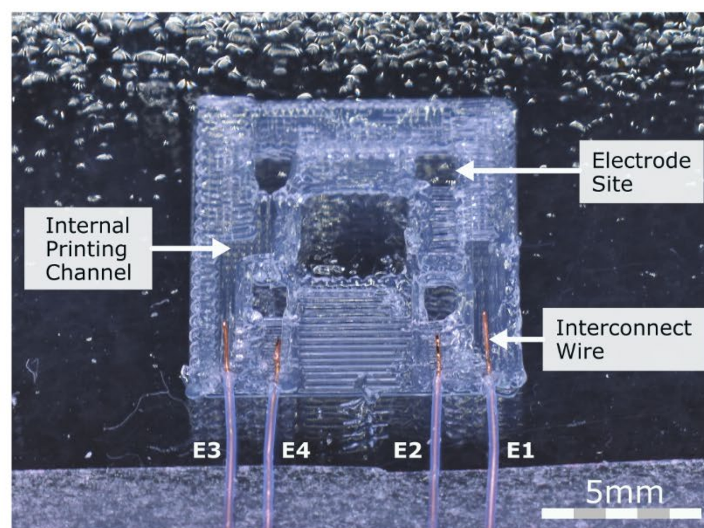


Figure 3.43 Interface Version 4 electrode interconnect wire fabrication.
Interconnect wires are placed in whilst the SE1700 is still tacky after a reduced curing time (40 minutes) at 100°C. The interconnect wires are 36AWG single core copper wires with a clear PFA coating.

3.9.2 Continuously Printed Electrodes

After the fabrication of multiple Interface Version 4 samples using the previously described electrode print path design, it was found that there was poor consistency in the print quality of the electrode faces whilst also producing inconstant electrode-interconnect wire connections (Figure 3.44A). All Interfaces fabricated using the original electrode print design would regularly result in only one electrode pair working. The majority of the electrodes would require remedial work - both during and after printing - to ensure a better connection. It was decided that applying the continuous printing method to the electrode print paths would be a suitable solution to the print quality issue. This resulted in a greater consistency in electrode printing. Both the electrode face and internal electrode printed wires were reproduceable across fabricated Interfaces (Figure 3.44B).

The improvement in electrode consistency due to the altered fabrication method was quantified through measuring the electrode's average resistance. This resistance was measured between the electrode face and the end of the internal printed electrode wire (Figure 3.44C). The original electrode's print paths had an average resistance of 21.69kΩ (±14.37kΩ). For the continuously printed electrode's print paths, the average resistance measured was 2.83kΩ (±1.69kΩ). This represents a factor of 10 decrease in the average electrode resistance post-fabrication. The next section will detail how the continuous printing process was applied to the electrodes to produce this performance gain.

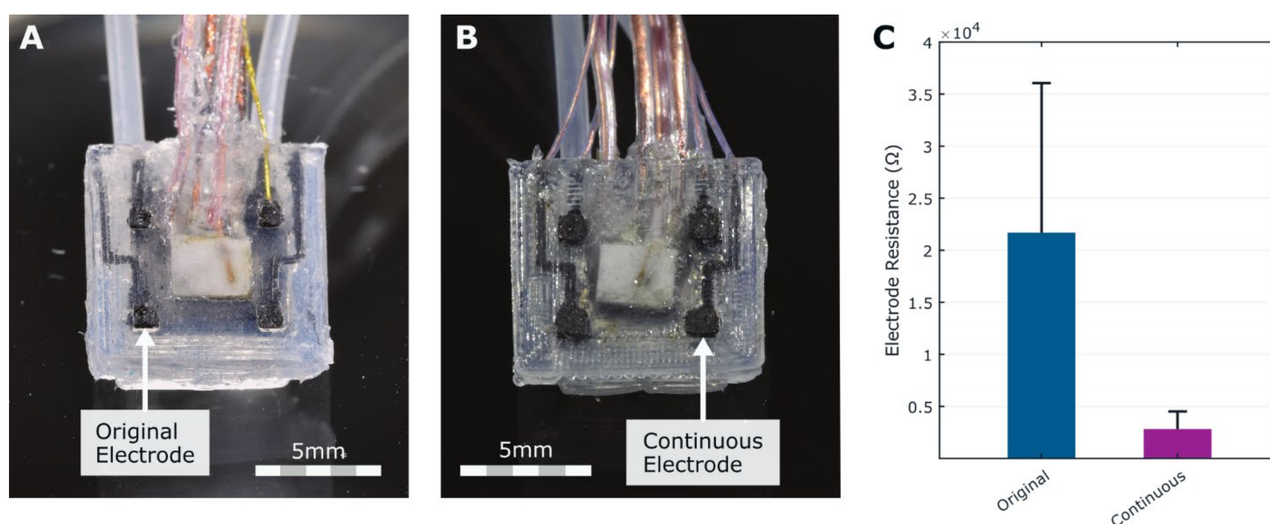


Figure 3.44 Printed electrode design comparison.
Pictures that visually compare the electrode face of the original design, **A.**, and continuous design, **B.**, indicate improvement in print uniformity. **C.** The difference in the average electrode resistance measured after fabrication using the original (n=9) and continuous (n=30) electrode printing techniques. Error bars indicate the standard deviation of the electrode designs.

Continuous Electrode Pathing

At first, the idea was to retain the original print paths and to try tuning the material print parameters. However, it was found that the optimisation of the G-PDMS material print parameters did not produce a noticeable reduction in the electrode print failure rate. It was deemed that the major contributing factor to these failures was the BioCAD synthesised inter-layer actions of the nozzle during electrode printing.

G-PDMS's viscosity is at the boundary of the what the 3D Discovery's technology is capability of dispensing. This causes large variation in the flow characteristics of the material – especially during beginning of an extrusion event. Any pause or material retraction during the electrode printing process is highly vulnerable to becoming a failure point. As there is currently three such events in the electrode pathing, the likelihood of reducing this issue is untenable. A new electrode print path design would be required.

The new electrode printing design is based on the continuous printing technique used with the Microfluidic Loop paths. Specifically, how the print path is instructed to translate in z-axis whilst extruding so that the print takes place in one movement. Electrode print pathing was adapted to enable this for each electrode (Figure 3.45A). These new electrode paths are drawn onto layer 2 as a single line in Inkscape; however, these only exist on a 2D plane instead of the 3D pathing that is required. From a Z/X-axis view, the print paths will need to be configured to have the deposition begin at the bottom of the electrode void and then rise out vertically (Figure 3.45B). It is not possible for this action to be output from BioCAD natively – nor is it simple to draw the points necessary to run this through the continuous printing script.

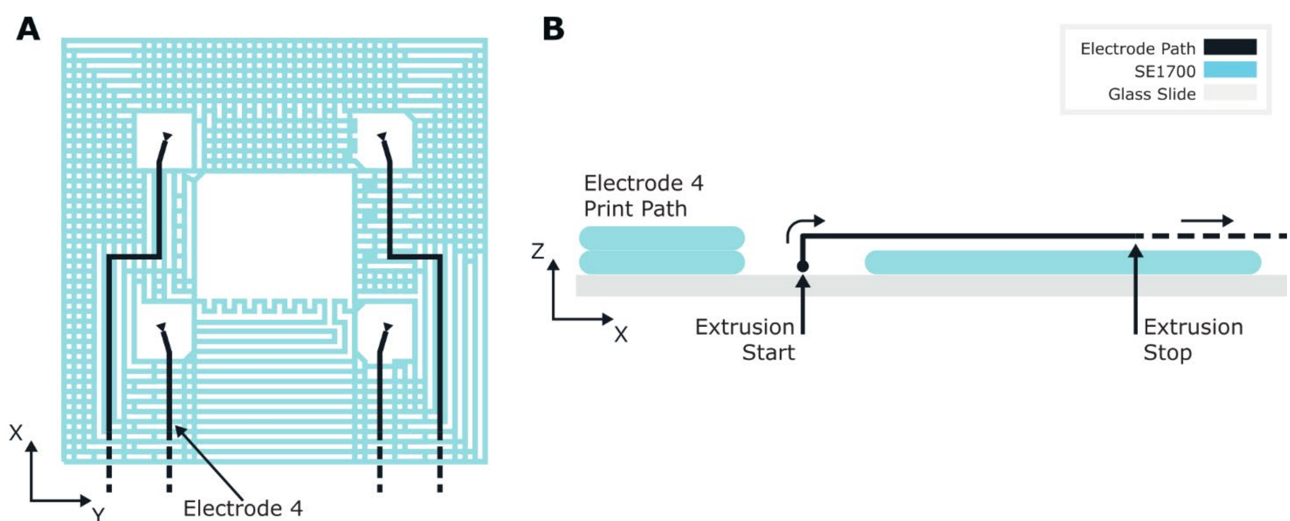


Figure 3.45 Print paths for the continuously printed Interface electrodes.
A. Print pathing of the continuously printed electrodes within Inkscape. Paths are placed on layer 2. Viewed in the X/Y plane. **B.** The Z/X-axis plane view of an electrode's printing path. Modifications to the BioCAD generated G-code are required to achieve this pathing. The extrusion start and stop points are indicated. Smaller arrows dictate the nozzle travel direction.

Electrode G-code Processing

Using the pathing commands for electrode 4 as an example, the G-code that is required to be outputted for then processing into continuous print pathing is the following:

```
1  (Electrode 4 Print Start)
2  G0 X-1.096 Y-0.095
3  G0 Z5.29
4  M97
5  M30 P3.6
6  F4 G1 X-0.982 Y-0.665
7  X-0.982 Y-1.692
8  X-0.754 Y-1.692
9  M96
10
11 G0 Z5.39
12 G0 X-0.74 Y-1.69
13 G0 Z5.29
14 M97
15 M30 P3.6
16 G1 X1.357 Y-1.692
17 M96
18 (Electrode 4 Print End)
```

where lines 2 to 9 describe the instructions for the printhead to move to the electrode paths start point (line 2 & 3). Lines 4 & 5 starts the printhead extrude but with a programmed movement delay. The printhead then begins to move along the print path commanded in lines 6 to 9 until the extrusion stop point. Lines 11 to 17 describe the instructions for the last section of printhead movement. First, as it is a separate line, the printhead performs a Z-axis retraction from and to the same Layer height (lines 11 to 13). The printhead then starts to extrude again with a delay (line 14 & 15). Line 16 makes the printhead move to the final location and then extrusion is stopped (line 17).

This output is designed to be synthesised directly from BioCAD in a form that contains the instructions required for the implementation of the continuously printed electrodes. However, the G-code output still contains instructions that are redundant. These instructions need to either be modified (highlighted in green) or need to be removed (highlighted in red).

For the instructions to be modified:

- Line 3 → the Z-axis translation needs to be lowered to the layer 1 height value.
- Line 5 → the P code delay time will need to be extended to allow face void filling.

Instructions that are marked in red are simply deleted from the file as the inter-layer Z-axis movement (Figure 3.17B) and the toggling of printhead material extrusion is not desired.

Action on these lines of code results in the continuous Electrode instruction set for Electrode 4 to be:

```
20 (Electrode 4 Print Start)
21 G0 Z5.4
22 G0 X-1.096 Y-0.095
23 G0 Z4.8
24 M97
25 M30 P24.4
26 F0.15 G1 Z5.1
27 F4.5 X-0.982 Y-0.665
28 X-0.982 Y-1.692
29 X-0.754 Y-1.692
30 M96
31 X1.357 Y-1.692
32 (Electrode 4 Print End)
```

The nozzle now moves into position above the electrode site and Z-axis translates to same height as layer 1 (line 21-23). Extrusion is started with the printhead movement being delayed for 1.525s (line 24 & 25). A new instruction was inserted on line 26 to command the printhead Z-axis translation up to layer 2 (line 26). The Z-axis translation is performed at a slow feed rate which was tuned to allow for the electrode void to be filled completely but without overspill.

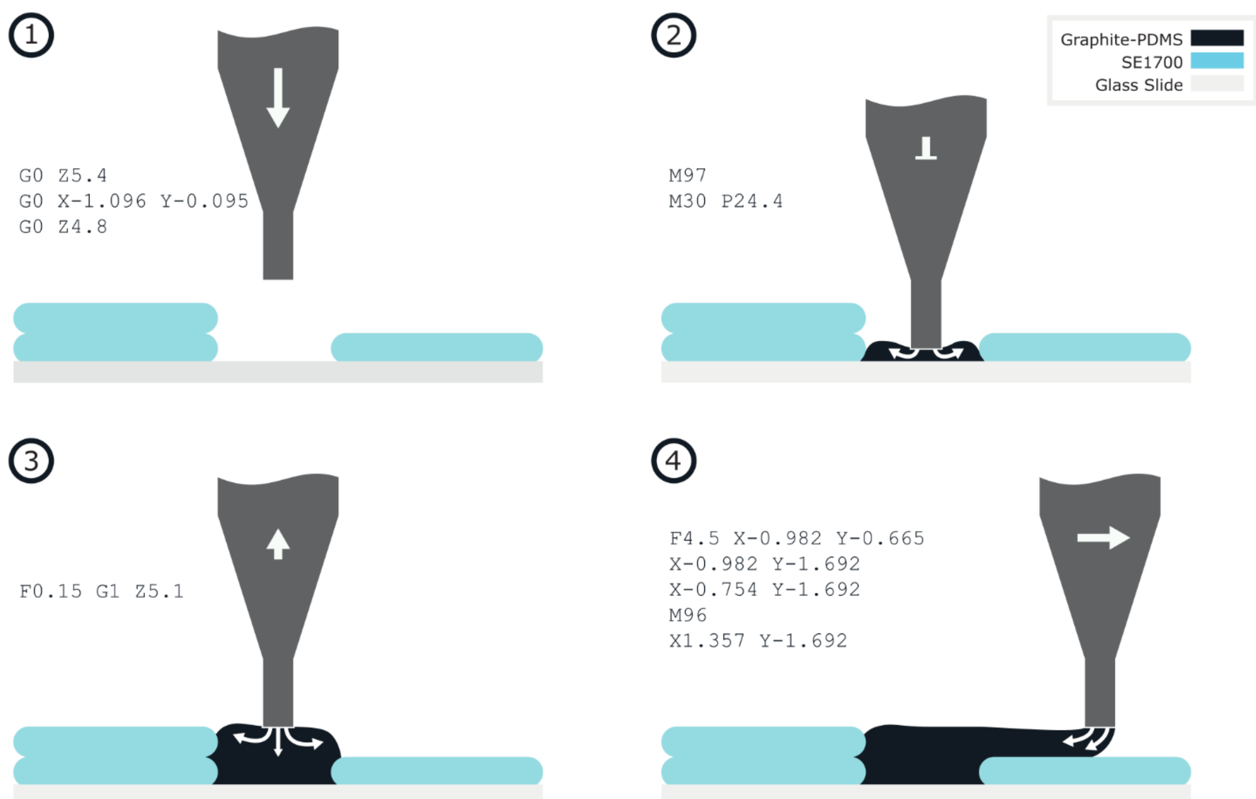


Figure 3.46 Continuously printed electrode G-Code instruction flow.
(**1**) Nozzle translates down to approximately the same layer height as layer 1. (**2**) Extrusion starts but movement is delayed for 1.525s. (**3**) Nozzle slowly lifts out of the electrode void to layer 2 height whilst continuously extruding. (**4**) Nozzle translates along internal electrode print channel and extrusion is stopped before the last translation is instructed. Material colour legend is given in the top right-hand corner. Symbols on the nozzle indicate movement state; arrows indicate directional movement; the blunted line indicates no movement. Small arrows in the G-PDMS represent material flow direction.

The nozzle then begins the X/Y-axis translation to print in the internal electrode print channel at an increased feed rate (line 27-29). Extrusion is then stopped near the end of the print path to prevent the G-PDMS material from extending outside the electrode boundary where the interconnect wires are located (line 30 & 31) (Figure 3.46).

This processing is applied identically to all four Interface electrode paths. The only differences between them are the electrode print location coordinates and that electrode 1 and electrode 3 have two more internal electrode channel movement commands due to their greater pathing complexity. Processing of the electrodes G-code was performed manually whenever a new design had its G-code synthesised from BioCAD. Due to time constraints, it was deemed that manual alterations would be the 'go to' process rather than writing and debugging a new python script to automate it.

3.9.3 Version 4 Pathing

As previously mentioned, integrating the electrodes into the Base Section required it to be being split into two separate printing instances. These instances are named Base Section A, Figure 3.47A, and Base Section B, Figure 3.47B. Base Section A contains layers 1 & 2 that form the internal electrode channels and the TEC mounting area. Base Section B contains the continuous print electrode paths that are print out of G-PDMS over layers 1 & 2. The printhead then switches to SE1700 to then print layers 3 & 4. Unaltered from the Interface Version 3 Base Section, layers 3 & 4 encapsulate the internal electrode material to provide isolation from one another and from the external environment to prevent noise ingress.

Once the Base Section is cured, the TEC Assembly is bonded into position. SE1700 is applied around the TEC exterior (bar the TEC cold-side face) and over the Heat Sink's underside. It is inserted into the TEC mounting location. A second glass slide is used to clamp the TEC Assembly in place during its curing. A conformal silicone coating is applied to this second glass slide's face to allow easy post-cure removal if any excess SE1700 was to bond the Heat Sink to the clamping glass slide. To cure, the Interface is placed in the oven at 100°C for 1 hour.

The Heat Sink guard ring and Microfluidic Loop are printed last. These sections are printed in one print instance (Figure 3.47). They are effectively identical to the paths designed for the Interface Version 3 Metal Heat Sink variant. Once printed, the Interface is cured at 100°C for 1 hour before the Loop silicone tubes are adhered into the printed loop using SE1700. This then completes the Interface printing process with it being ready for testing and connectorisation.

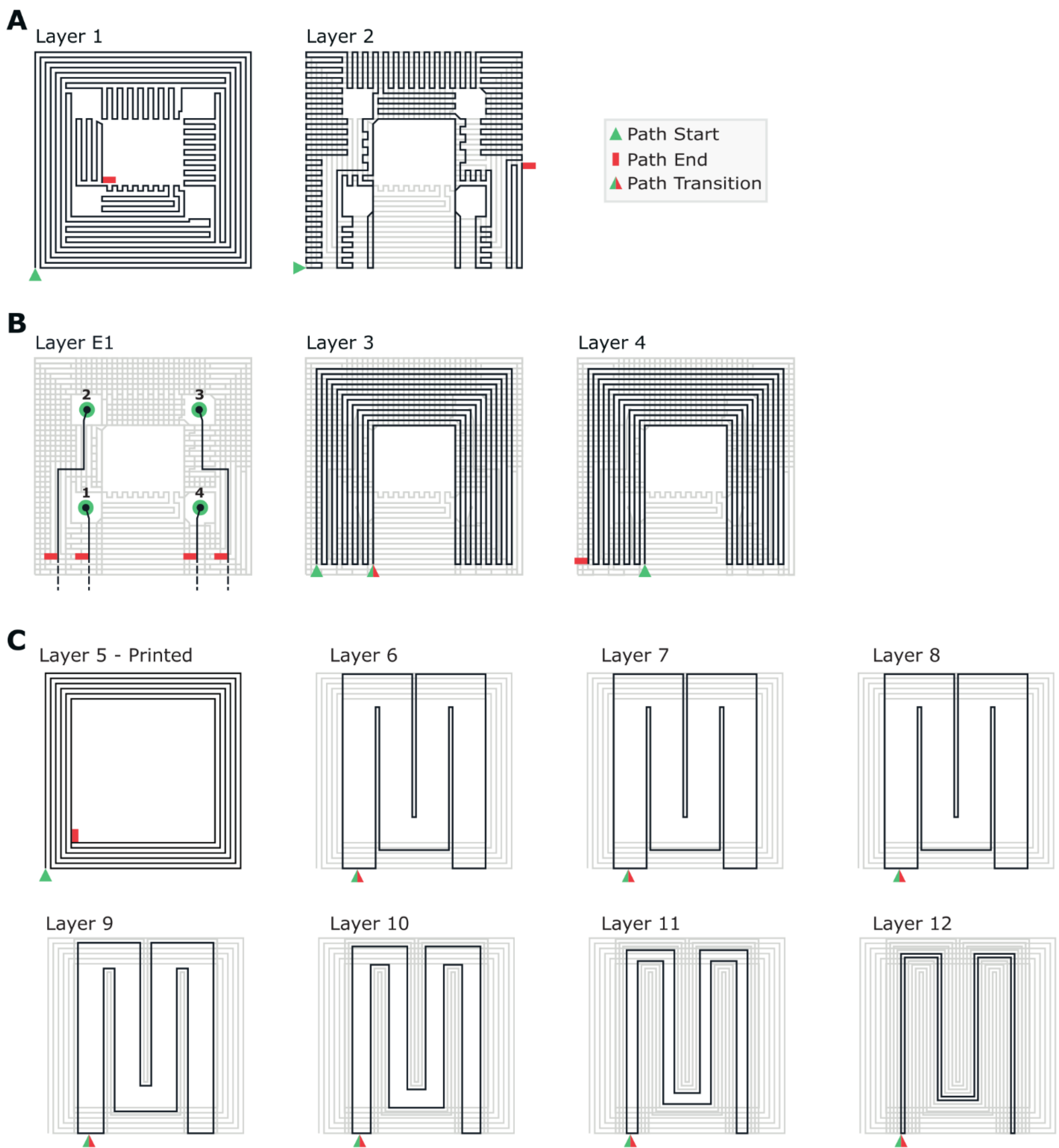


Figure 3.47 Complete print paths for the Interface Version 4.
A. Base Section A print paths that form the Electrode printing channels. These are part-cured at 100°C for 40min before wires are inserted and Base Section B is printed. **B.** Base Section B print paths containing the continuously printed Electrode paths and the upper two Base Section layers. **C.** Microfluidic Loop print paths that have been processed through the continuous printing script. Legend for the print path markers is provided.

3.9.4 Interface Omnetics Connector

For the Interface to progress towards *In Vivo* use, it needed to become easier to handle in regards to the Interface interconnect wiring. Previous Interface versions were monolithic units that had the Interface-Electronics interconnect cable hardwired onto the Interface. Having this setup causes the Interface to have an effective length greater than 350mm. Maintaining accurate Interface positioning during study setup, wherever it be *In Vitro* or *In Vivo*, is made difficult due to the cable wrangling.

To solve this issue, an intermediary connector was introduced to shorten the hardwired Interface interconnect cable to a more manageable 100mm length. The connector system used is 12pin micro360 circular connector (Omnetics, USA) (Figure 3.48A). This system fulfils the requirements that the connector must achieve. These being:

- No more than a 10mm^2 connector face.
- Contacts rated to at least 3A current.
- At least 11 connector contacts (2x TEC, 4x Thermocouple, 4x Electrode, 1x GND)

Solder cup variants of the micro360 connectors were sourced for use due to wire size limitations using the crimp connector variant – the thermocouple 40AWG wires are below the crimping lower wire limit. Thus, integrating this connector into the Interface interconnect cabling required hand soldering. The Interface wires were soldering in a pre-determined order to prevent excess mechanical stress breaking the smaller wires. The soldering order was: TEC wires -> Electrode wires -> Thermocouple wires. To mechanically strengthen and electrically insulate the soldered joints, the thermal epoxy was used to pot them. The potted material shape was guided by a PDMS cylindrical mould created from casting PDMS around a micro360 socket connector. The result of the connector processing is pictured in Figure 3.48B, where the wires are seen potted by the thermal epoxy. Total connector length after potting is ~8mm.

Wire connection layout for this connector was standardised (Figure 3.48C). Consideration was given to the potential cross-talk between the each of the components signal lines. Placement also prioritises electrode isolation from the TEC signal lines to prevent chance of stimulation through the electrodes if the solder connections are bridged. The overall layout presents a symmetrical wire placement for ease of construction and to provide consistent noise influence across the interconnect wiring in case of unavoidable external noise occurrence.

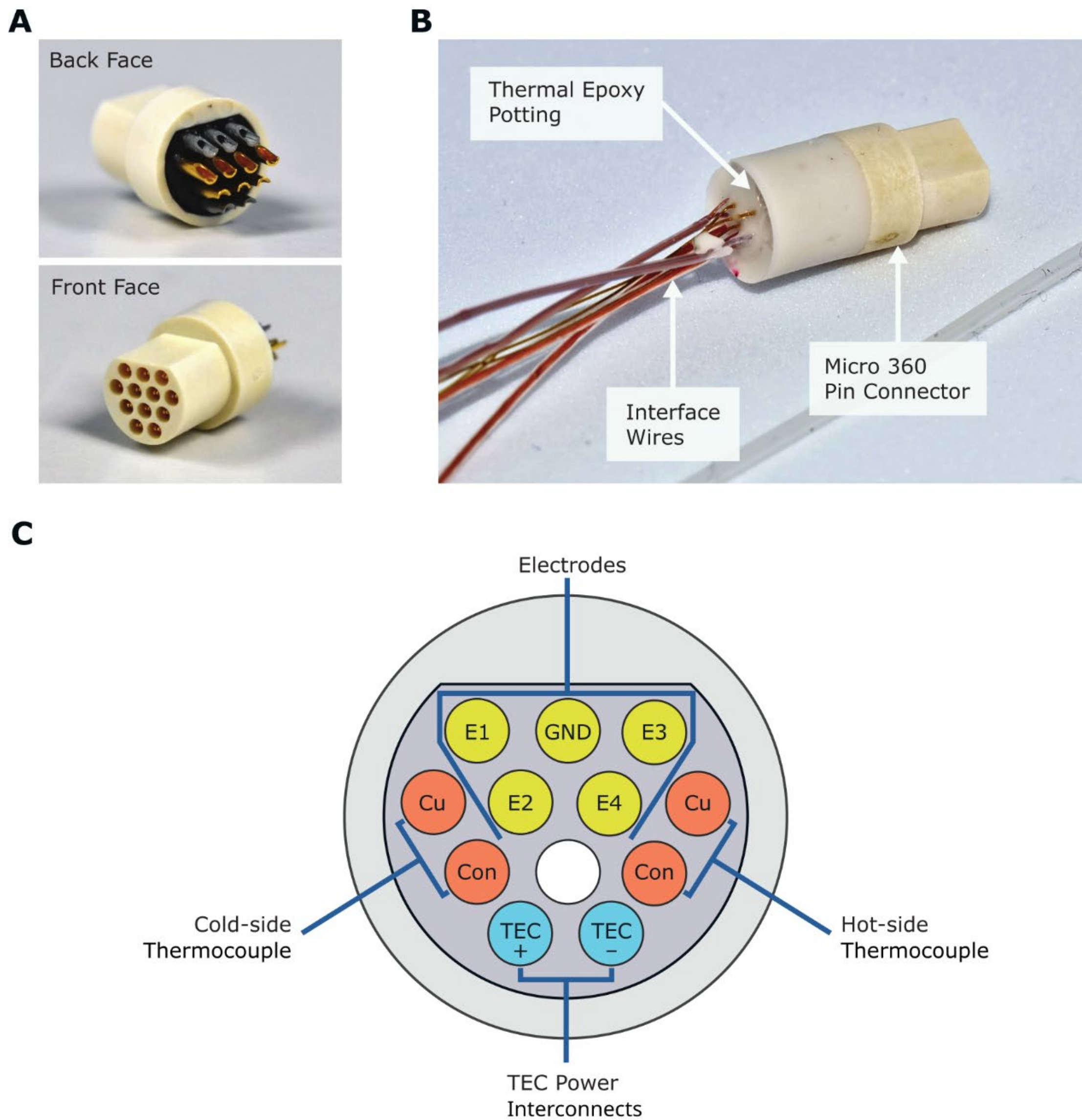


Figure 3.48 Omnetics Connector for the Interface interconnect wiring.
A. The font and back face of the micro360 Pin Omnetics connector solder cup variant. This will be hand soldered to the Interface interconnect wiring. **B.** An integrated 12-pin connector on the Interface's interconnect wiring. Wires soldered and then potted with a non-electrically conductive epoxy. **C.** Connector wiring diagram for the 12-pin micro360 type connector. Electrodes are clustered at the top of the connector with scope for adding a reference electrode to Intan GND. Thermocouple wires are symmetrically on the connectors side cups. The wore polarity in stated in terms of the t-type thermocouple conductor material. TEC power interconnects are soldered to the bottom two positions.

3.9.5 *In Vitro* System Profiling

Production of a stable Interface design allowed for the Interface's focal cooling capabilities and behaviour to be profiled within the *In Vitro* thermal model. The previous thermal model, utilised for Interface profiling, was deemed to be limited in its scope as a representation of the true implant environment. Thus, research was first conducted on devising a more representative thermal model to produce greater profiling accuracy within the *In Vitro* experimental setups.

In Vitro Thermal Model

Like the previous model, the bulk material used to simulate tissue was a water-agar gel. Within this new model, the gel completely encapsulates the Interface to increase the thermal capacity of the surrounding neural tissue mock. This water-agar gel block was cast within a container constructed from two petri dishes bonded together to form a clam-shell structure. A hole was made in the gel container's top for interconnect cable and silicone tubing routing. The gel is cast to form a 15mm thick layer below the Interface and form a have a 10mm thick gel layer above.

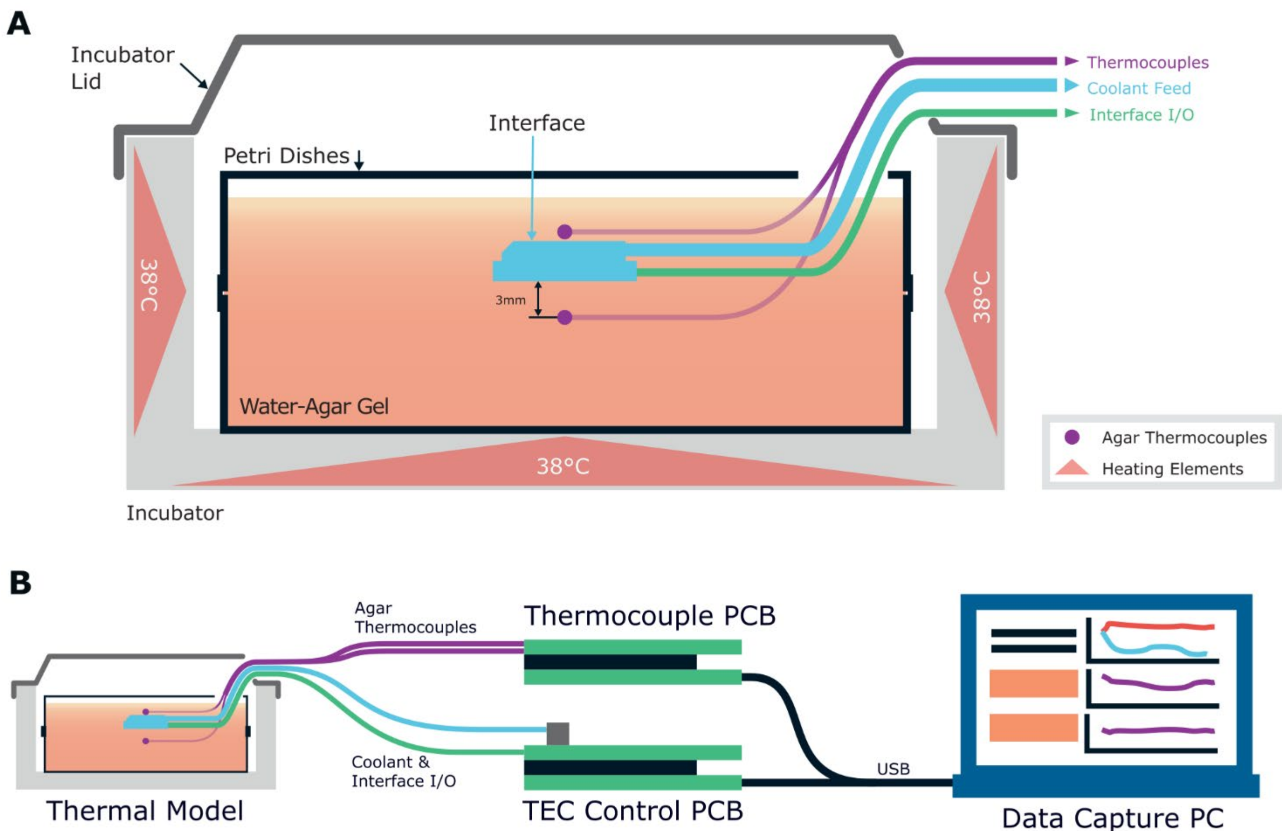


Figure 3.49 In Vitro thermal model for Interface Version 4 verification.
A. Cross-section of the thermal model setup. A water-agar gel, with a 1% Agar concentration, is cast around an Interface v4 within two bonded petri dish halves. Two thermocouples are embedded in the water-agar gel. One is directly atop the Microfluidic Loop external face and another 3mm below the TEC cooling face. The block is placed inside an incubator that is set to maintain a 38°C model temperature. Interface interconnect cabling and thermocouple connections exit through a gap in the incubator lid. A legend describes system objects. **B.** System flow for the *In Vitro* data collection. Thermal model thermocouple wires and Interface interconnect cabling connect to two instances of the TEC Control hardware that support data collection and control of the system. A data capture PC logs data from the two hardware instances using a custom LabVIEW VI.

The water-agar gel container was housed within an incubator (Challenger MX25, Dip-slides.com). The incubator's function is to inject heat into the model in leu of biological processes (Figure 3.49A). Heating elements line the base and sides of the incubator to provide a more uniform heat flux distribution in the model. The incubator lid aids in system temperature stability during function. Interface interconnect cabling and silicone tubing are routed through a gap between the incubators body and lid.

Two thermocouples are embedded within the water-agar gel to supply data of the Interface's cooling effect on surrounding 'tissue'. One was placed directly at the shortest thermal path possible from the TEC hot-side to the surrounding 'tissue'. This is located within the central valley of the Microfluidic Loop. Temperature change here would indicate if any excess heat from the TEC is leaked into the external environment. The other was placed 3mm below the TEC's cooling face. It was orientated to be located in the face's centre point and would provide spatial temperature data. Thermal data from this sensor would indicate wherever the cooling is reaching affecting this 'tissue' depth and, if it does, what temperature change is achieved.

External to the thermal model, the TEC Control hardware used to support the function of the Interface during these experimental runs. To enable data collection of the model thermocouples, a second TEC Control hardware instance is utilised. This instance was configured to only ingest the thermocouple data and have all other hardware disabled. Both hardware instances were connected to a single data capture PC. A LabVIEW data collection VI was written to simultaneously monitor and control both data streams in one environment.

Interface v4 *In Vitro* Profiling Method

To profile Interface function, a set of cooling runs were conducted. Cooling runs would be initiated and controlled via the data capture PC's LabVIEW VI. Upon initiating the cooling run, a pre-cooling delay (5s) is performed to allow data stream integrity verification. At 5 seconds, the TEC and microfluidic pump is activated for a 60s period. At 65 seconds, the TEC would cease cooling but the microfluidic pump remains active (30s). This is to continue the removal of remaining pumped heat to prevent any hot-side heat dump onto the cold-side. At 95 seconds, the cooling sequence ends with the microfluidic pump being deactivated. The *In Vitro* system then returns to its nominal monitoring state.

Starting with a reference temperature of 35°C, each cooling run was performed and then the reference temperature was decremented 2°C. The TEC's PID controller refence temperature was lowered until 23°C was reached. These runs were conducted with the nominal thermal model temperature of 37°C. After every run, a 5-minute intermission was inserted to allow the model temperatures to return to the nominal level.

For these cooling runs, the Microfluidic Loop flow was actuated by the centrifugal pump system. As is outlined in Section 4.7.1, this pumping system required flushing every three runs to remove trapped air in the system and prevent it from degrading cooling performance. Room temperature, de-ionised water was used as the coolant during the experimental runs (20°C).

Interface v4 In Vitro Results

Interface Version 4 demonstrates the capability of attaining a -14°C ΔT from the nominal model temperature (Figure 3.50A). This surpassed the specified benchmark ΔT of -12°C that is the minimum temperature difference required to produce an observable reduction in seizure activity [87, 88]. TEC hot-side temperatures were maintained below the nominal system temperature for the majority of the cooling run after an initial spike up to 42°C. This transient hot-side spike was not observed to cause an external temperature increase on the external thermocouple above the Microfluidic Loop. This data is a good indication that the coolant and current Interface structure provides enough insulation around the TEC hot-side to prevent external heat leakage.

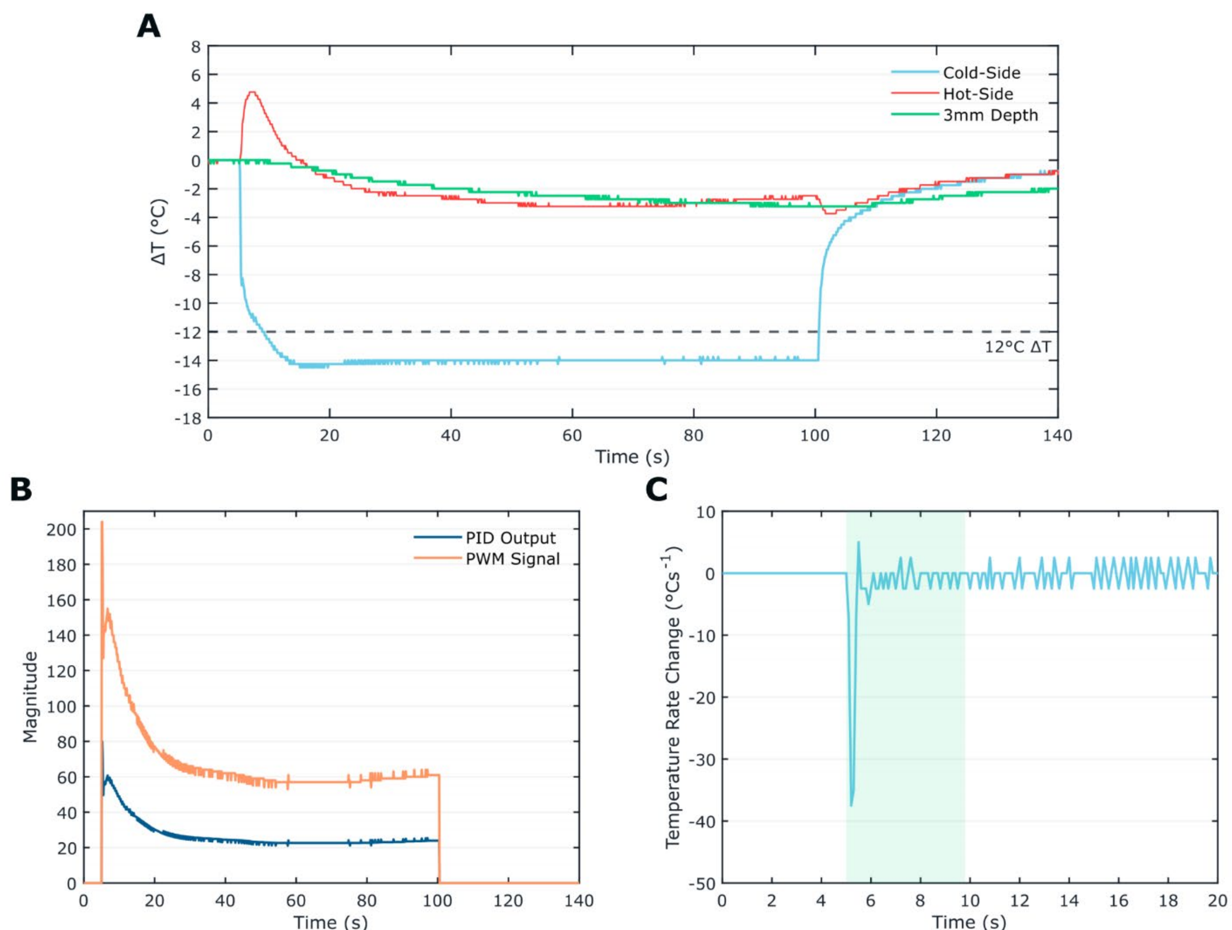


Figure 3.50 Interface Version 4 focal cooling In Vitro performance.
A. Cooling run profile using 23°C set point temperature reference. Recorded temperatures are plotted as ΔT from nominal (37°C). The cold-side ΔT is observe to pass the minimum ΔT required for seizure suppression. Cooling is recorded at 3mm below the TEC cold-side with an approximate -3°C ΔT. **B.** PID and PWM outputs for the TEC controller. Output magnitudes of both profiles align with them having the 80% output limiter. **C.** TEC cold-side cooling rate during the run's initial 20s. The time taken for the cold-side to reach 80% of the temperature set point – over which the rate of cooling average is calculated – is highlighted.

The 3mm depth temperature sensor profile Figure 3.50A demonstrates that the Interface is able to induce cooling within the 'tissue' bulk. At the 23°C T_{ref}, the 3mm depth thermocouple observed a ΔT of approx. -3°C. The magnitude of this ΔT would be hypothesised to be lower in a biological model due to the increased thermal buffer effect from blood flow and localised metabolic heat production. Both of these were not modelled in this setup. Though the Interface's ability to produce a depth cooling effect in a thermal tissue model, with lower thermal conductivity than neural tissue, indicates promise when translation to *In Vivo* work occurs.

TEC cold-side temperature rate of change at the cooling run's start indicates rapid cooling is achieved with this Interface design (Figure 3.54B). The large rate spike at 5s is induced when the TEC activates and correlates with the temperature reduction observed in the cooling run temperature profile. This represents an instantaneous cooling rate spike of -37.5°Cs^{-1}. Averaging the cooling rate from TEC activation to the cold-side reaching 80% of the T_{ref}, results in a cooling rate of -3.07°Cs^{-1}. This being within the bounds to class the Interface as rapid focal cooling device which can perform more efficient seizure suppression than slower cooling systems [91].

TEC controller output was also seen to perform robustly (Figure 3.50C). The PID controller output conforms to the 80% limiter that is imposed on it due to hardware constraints. Translation of this controller output to the PWM value for the TEC driver signal is performed as expected with it too conforming to the control limit in place for the system.

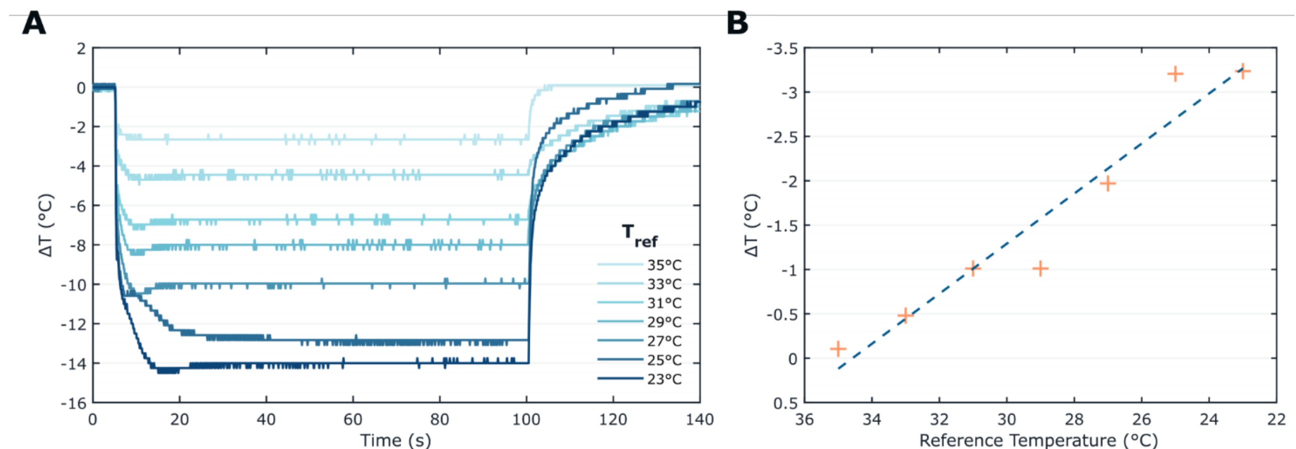


Figure 3.51 Interface Version 4 cooling performance from 35°C to 23°C.
A. TEC cold-side cooling profiles starting from 35°C to 23°C. Each run decrements by 2°C each time.
B. Temperature difference of the 3mm thermocouple between the start and end temperature for each cooling run. A 1st order line of best fit indicates a positive correlation between 3mm temperature difference and the set temperature reference.

One of the benefits with having a TEC as the primary cooling element is the fine temperature control it enables. Profiles from the performed cooling runs demonstrate the Interface's ability to rapidly reach each temperature whilst also maintaining stable steady-state control around a run's T_{ref} (Figure 3.51A). Across these runs, observed cooling at the 3mm depth sensor is also achieved (Figure 3.51B). A positive correlation is observed between a cooling run's T_{ref} and the ΔT observed at 3mm below the TEC cooling face. One where the lower the temperature reference is set results in a larger temperature difference observed at the 3mm thermocouple. These results demonstrate that the Interface design is capable of achieving cooling depth and rates that would indicate it is able to hypothetically suppress epileptic seizure activity. This is shown with reaching a >12°C ΔT and having a cooling rate >2°C.

3.10 Interface Version 5

This Interface version is defined by the refinements made to the electrode to produce a more resilient and reliable implementation. This is achieved through alterations to the electrode channel pathing and electrode production (Figure 3.52). In addition to these alterations, a new electrode processing step was added. Taking place before an *In Vivo* experiment, the electrodes are exposed to a cold plasma for >20s. This treatment enhances the electrode wettability to quicken neural signal acquisition and is demonstrated through its reduction in water droplets contact angle on printed electrode material.

This is the final Interface version produced for this research project and is its culmination. There exists two electrode-setup configurations of this Interface. The first configuration has all four electrodes being printed from G-PDMS ones – identical to Version 4 electrode setup. This configuration is the primary one used in the testing of this Interface version and can be assumed to be used in all *In Vitro* and *In Vivo* studies presented in this section (Figure 3.53A-C).

The second configuration replaces one G-PDMS electrode pair with Pl/Ir wires. These wires are designed to protrude from the cooling face forming 2mm long barbs to act as a test bed for introducing the drug delivery modality to the Interface. Two Interfaces, in this configuration, were manufactured to test the feasibility of its design. The initial implementation of this configuration is discussed in Section 3.10.4

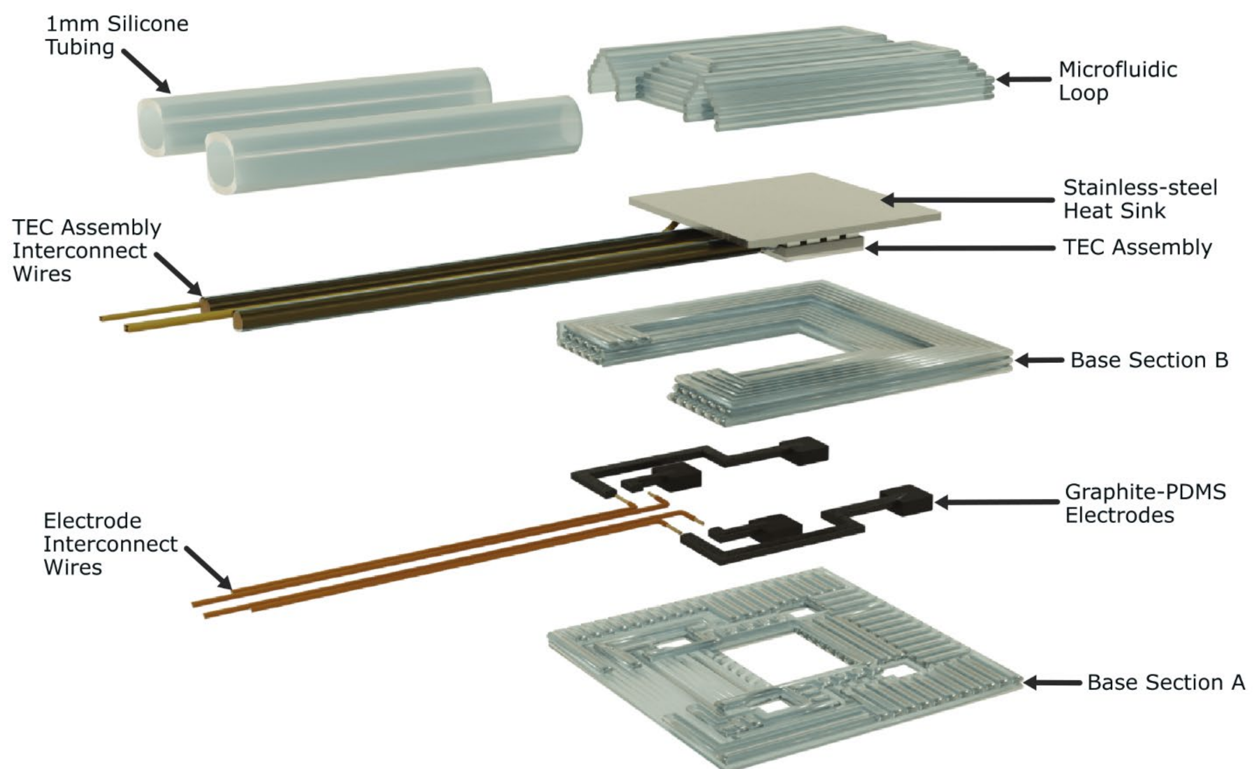


Figure 3.52 Interface Version 5 design visualisation.
Each Interface section and part is labelled accordingly. Connection to the Interface Support Electronics is provided through the interconnect wires from the TEC Assembly and the electrodes.

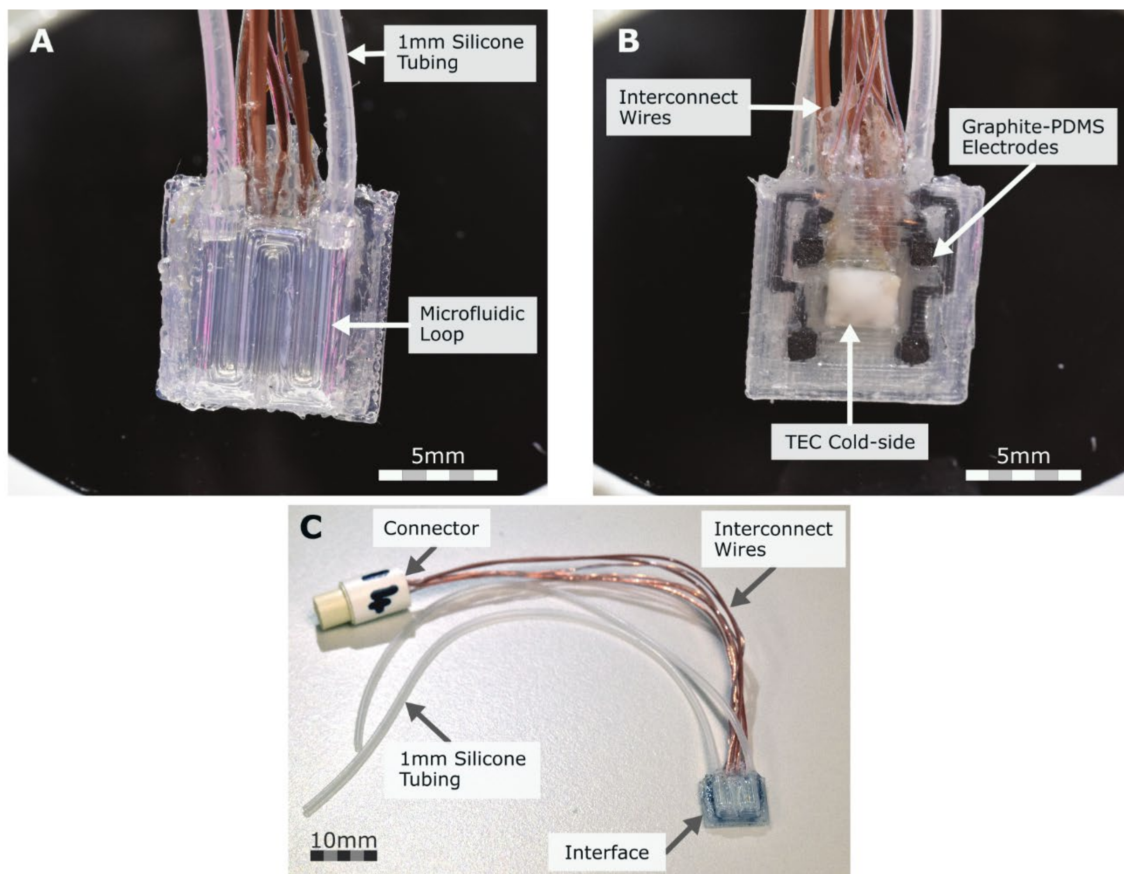


Figure 3.53 Fabricated Interface Version 5 sample.
A. View of the Microfluidic Loop printed atop the Interface. **B.** Interface underside showing the exposed TEC cold-side area for cooling and the printed G-PDMS electrode array. **C.** Interface 14 fabrication sample with the Omnetics 12pin micro360 connector mounted on the end of the Interface interconnect wires.

3.10.1 Electrode Surface Wettability Modification

Over the course of multiple *In Vivo* experiments, it was noted that the time to acquire a nominal neural signal was >20mins after an Interface had been mounted on the Rat Model. It is hypothesised that the PDMS within the conductive composite was causing the unpredictable signal acquisition delay. PDMS is inherently hydrophobic which results in the reduction of the electrodes wettability. Even if the electrodes are placed correctly, they will still exhibit a large contact impedance until surface wetting is achieved. Other current electrode process, such as the mechanical electrode surface abrasion, did not provide a noticeable reduction in the wetting delay. It was necessary to find a suitable surface modification method that would alter the electrodes to be less hydrophobic.

Methods for modifying surface wettability include plasma treatment [14, 15], UV exposure [16], or polymer deposition [17-19]. As the increase in wettability is only required to decrease the initial time to wetting, a permanent electrode surface modification is not required. A desire for a simple processing solution and the potential impact on biocompatibility from new materials, surface modification through plasma treatment was selected for investigation.

Mounted on the 3D Discovery printhead 5 was a PiezoBrush PZ3-i cold plasma unit (Relyon Plasma, Germany). Its Nearfield Module was installed in the PiezoBrush for all treatments as it is specifically designed for use on electrically conductive surfaces. Integration with the printer allows for the PiezoBrush unit to access the printhead controlled air supply and allow homogenous surface treatment through repeatable pathing at programmable speeds. Plasma power output level control (18W maximum) is achieved with a variable 0-10V analogue signal via a potentiometer. The 0-10V signal is direct mapped to percentage power with a minimum PiezoBrush power output of 30%. The power output values stated for the experiments should be treated as the intended treatment power. Due to the plasma power control interface, the actual plasma power output has an accuracy of ±5% of the desired power.

Wettability characteristics will be recorded by measuring the water contact angle of droplets on printed Graphite-PDMS Composite samples. Sample plasma exposure time was varied to gauge a minimum exposure time required to produce an observable wettability increases. It is also imperative that any other effects due to the plasma treatment are noted as this material has not yet been tested under these conditions. 8mm x 8mm, single layer Graphite-PDMS Composite samples were printed in pairs on glass slides (Figure 3.54A). The Nearfield Module was placed 2mm above and centred on the samples (Figure 3.54B).

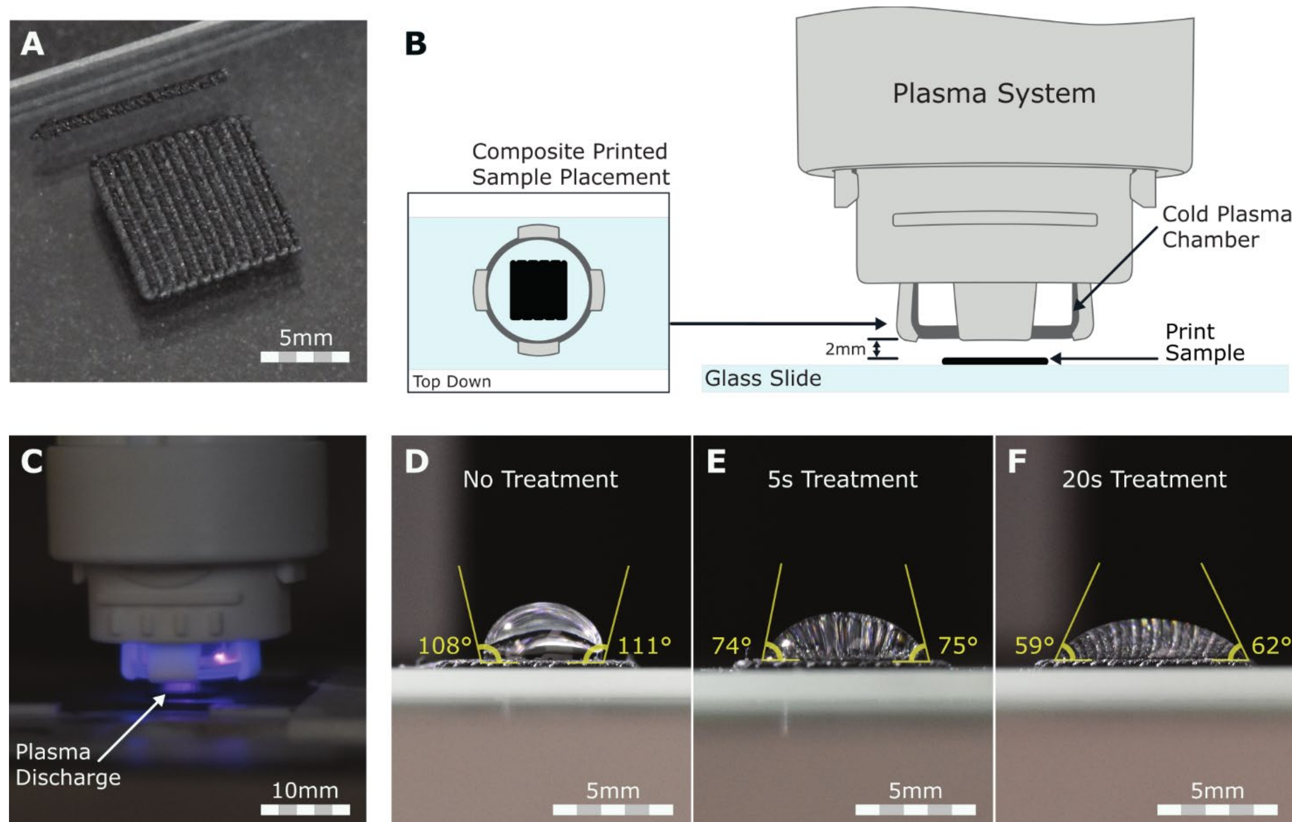


Figure 3.54 Electrode surface modification for improved electrode wetting.
A. 8mm x 8mm Graphite-PDMS Composite samples printed as a single layer square. **B.** PiezoBrush orientation and positioning relative to the printed samples for all plasma treatments. **C.** Plasma activation undertaken by the PiezoBrush during a 20s treatment length at 80% plasma power. Surface contact angle of deionised water droplets on a sample with (**D**) no treatment, (**E**) a 5s treatment time, and (**F**) 20s treatment time (right).

For all samples, the plasma power was kept constant at 80% (±5%) and the air feed was set to 0.150MBar. Sample were produced of an untreated electrode surface, 5s of plasma exposure and 20s of plasma exposure. These exposure lengths would help explore if they are able to induce significate surface activation whilst minimising Interface plasma exposure in case of potential damage. Ongoing plasma treatment, pictured in, can be seen to have plasma discharge nearer the edges of the head (Figure 3.54C).

Once plasma treated, an average droplet volume of 33µL was manually deposited on a sample's surface. The droplet profile was then imaged using a D3500 SLR (Nikon, Japan) with a 105mm F2.8 Macro Lens (Sigma, Japan). The samples were positioned against a high contrast background. Contact angle measurements were performed using the vector graphics software (Inkscape) (Figure 3.54D). The untreated material sample had an average water contact angle of 112° (±5.3°, n=4). Samples that were plasma treated for 5s had an average water contact angle of 78° (±4.3°, n=4). Samples that were treated for 20s had an average water contact angle of 60° (±2.0°, n=4).

There is a clear decrease in water contact angle observed when the samples are exposed for 5s. Prolonging plasma treatment only further decreases the water contact angle of the sample droplets. This provides evidence that this surface modification would be a suitable solution for activating the Graphite-PDMS Composite electrodes. No other visible changes to the material were noted during treatment.

It is of note that the plasma discharge was not uniform over the sample materials located under the plasma unit. Contact angle measurements on multiple droplet samples reflected this by forming non-uniform water contact angles around the droplet's perimeter. This non-homogenous discharge behaviour is in line with information provided by Relyon Plasma. It is then required that the plasma unit be moved over the Interface's surface during treatment to ensure a more homogeneous surface activation is achieved.

3.10.2 Electrode Interconnect Wires

The electrode interconnect wiring placement in the interface V4 design was found to cause mechanical faults. During *In Vitro* experimental use, there were cases of the interconnect wires becoming dislodged from the printed electrode material and rendered them inoperable. Having the interconnect wire connections located at the Interface's edge resulted in there being minimal support material surrounding this connection - making it mechanical weak. The wire could be removed with ease when a tensional force was applied to the wire parallel to its mounting direction. The only way to resolve this issue on the Interface V4 units was to apply super glue to reenforce the wire connection point. However, this would be detrimental if the issue arose during an *In Vivo* experiment or on a chronically implanted Interface.

The solution to this issue was found through redesigning the internal electrode channel routing, through the Base Section A, to increase the innate mechanical strength of this connection. Modification to the layer 2 print paths were performed to manipulate the internal electrode channel's shape (Figure 3.55A). These channels are now designed to exit into the central TEC Assembly interconnect wiring channel instead of the Interface's edge.

Having the electrode interconnect wires exit with TEC Assembly interconnect wire bundle ensures that any tensional force applied to the wiring would now be distributed evenly over the whole bundle as opposed to an isolated electrode interconnect wire. These paths also grant a greater contact surface area between the electrode interconnect wires and the printed Interface material. This provides increased mechanical strength for these connections points without having to change the bonding material. However, the primary increase in connection strength comes from having interconnect wires connecting perpendicular to the internal electrode channel entrances (Figure 3.55B). With the wires bonded at a 90° to the Interface exit, torsional force applied to the individual electrode wires is now distributed over a larger surface which increases the wires resilience to accidental force applications during handling.

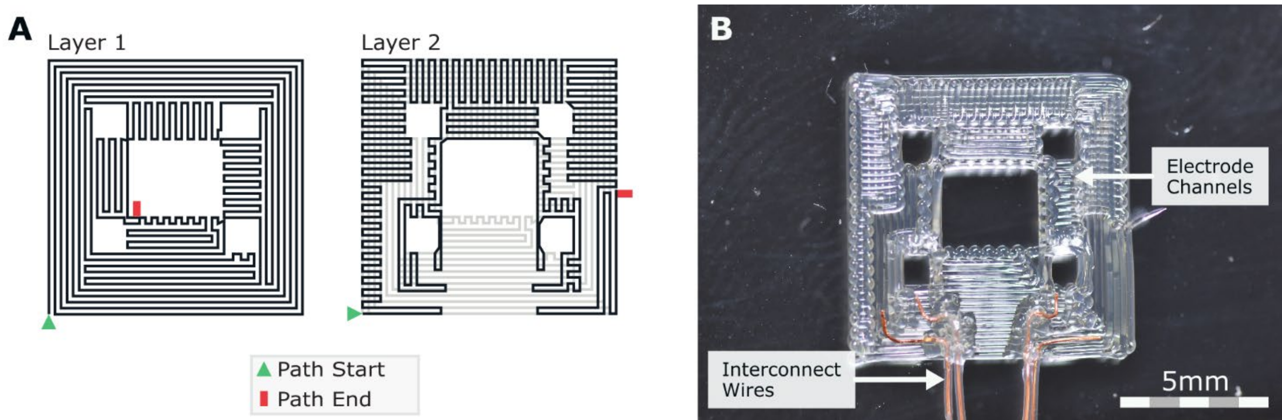


Figure 3.55 Base section A alteration for improved electrode wire bonding strength.
A. Print paths for layer 1 & 2 with the internal electrode print channel changes presented primarily on layer 2. **B.** A printed example of the updated Base Section A paths with the electrode interconnect wires bonded into the internal electrode print channels perpendicular to the direction of TEC Assembly interconnect wire channel.

3.10.3 Print Pathing Alterations

Three modifications to the Interface print paths were required to integrate the electrode interconnect wire connection rework and to improve the TEC Assembly bonding alignment. Base Section B pathing contain the majority of these modifications (Figure 3.56A).

In layer E1, the electrode print paths were altered to conform with the new internal electrode channel design in Base Section A. An extra 90° corner was added to each internal electrode channel with the G-PDMS extrusion halting 0.250mm before the TEC Assembly wire channel edge. The printhead then continues to travel towards the TEC Assembly wire channel centre line before the printhead transitions to the next print path. This mixed extrusion behaviour continues to be implemented to prevent short circuit occurrence between the four electrodes and the TEC Assembly electronics from excess conductive composite deposition.

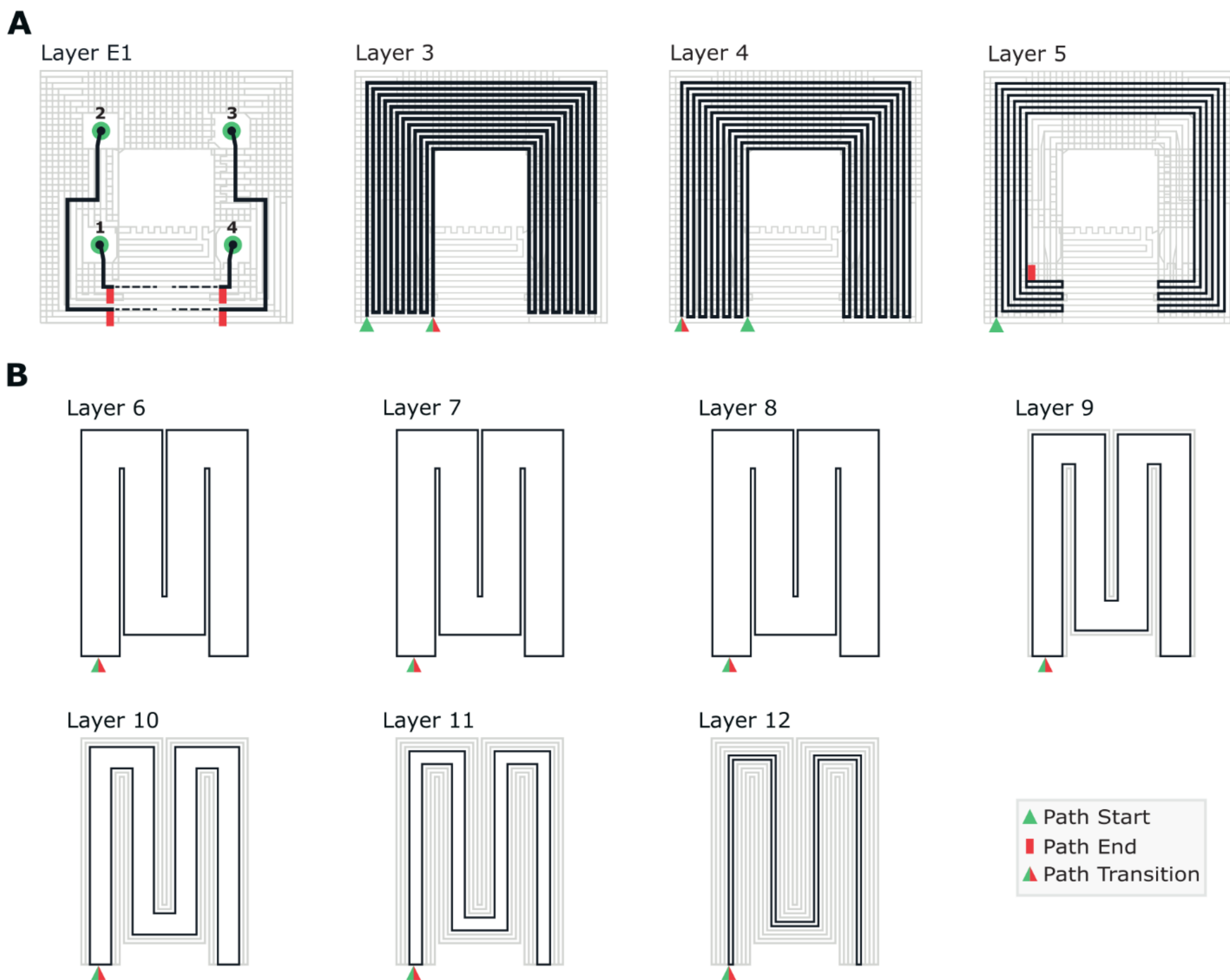


Figure 3.56 Base Section B & Microfluidic Loop pathing for the Interface V5.
A. Layers E1 through to layer 5 are all printed during the Base Section B print instance. The dashed section on each electrode path dictates printhead movements whilst material extrusion is disabled. Microfluidic Loop paths from layer 6 to layer 12 are printed in a single instance. Layer 5 is now printed as part of the Base Section B print instance. Colour markers indicate path start, stop, and continuous print layer transitions.

The electrode pathing change means that the internal channels of electrode 2 & 3 now have an extended section that is located close to an Interface's outer edge. Exposure of this printed electrode section to the external environment becomes a possibility if the SE1700 is under-extruding on the layer above. To reduce the risk of this occurring, the layer 3 & 4 paths above affected internal electrode channel section were extended to be closer to the Interface edge. Electrode encapsulation by these layers could then be guaranteed during any expected material extrusion rate variance experienced during a nominal Interface print instance.

The last pathing alteration was moving layer 5 from the Microfluidic Loop print instance to the base section B print instance (Figure 3.56B). It was found that, when adhering the TEC Assembly to the Base Section, maintaining consistent Assembly alignment across Interface fabrications was difficult to achieve. Printing the layer 5 Heat Sink guard ring was moved to Base Section B print instance. Printing this prior to TEC Assembly bonding provides a built-in alignment guide for the bonding process. The layer 5 pathing was adapted to account for the TEC Assembly interconnect wire channel not being pre-filled before its printing. Other than the layer 5 removal, no changes were made to the Microfluidic Loop paths. The final Interface 3D printing manufacturing process is present in three films (Appendix D). Each film demonstrates the 3D printing fabrication process of the Base Section A; the G-PDMS electrodes and Base Section B; and the Microfluidic Loop.

3.10.4 Local Drug Delivery Electrodes

The last modality to be investigated for Interface design, during this research project, was electronically-control local drug delivery. It is intended to function in collaboration with the focal cooling to enhance long-term seizure suppression and occurrence reduction post-cooling. Through application of an anti-epilepsy drug locally, this system will be able to bypass the blood-brain barrier. This can allow for the use of anti-epilepsy pharmaceuticals that are usually ineffective due to being taken orally. As this modality is still in the preliminary stage of integration, only the electrode fabrication will be explored in this section with a brief contextual explanation of the releasing mechanism's theory.

Implementation of localised drug delivery is to be achieved via the encapsulation of the anti-epilepsy drug in PEDOT. This PEDOT encapsulated drug is electrochemically deposited onto a pair of the electrodes. Drug release rate by the PEDOT is then controlled through the application of a negative potential to the electrodes [142]. Rate of release can be tuned by varying the magnitude of the applied potential between -1.6V → 0V. As this material is electroactive, once the all the drug is released, the electrodes can be switched to and utilised for neural signal acquisition.

To support the deposition of the PEDOT encapsulated drug, the electrode design had to be altered. This was to fulfil two requirements that the G-PDMS type electrode could not. First was that the drug electrodes required a repeatable PEDOT deposition behaviour that allows for the quantity of encapsulate drug to be consistent between systems. The second was that, for the *In Vivo* experiments, the rat model's dura mater remains intact and hinders the diffusing of the released drug into the neural tissue. Due to this, the drug electrode needs to be able to pierce through the dura mater to enable direct contact with the neural tissue. With this specification it was decided to introduce the Pl/Ir wires back into the electrode design.

Fabrication of Interface samples to test viability, electrode sites E1 & E4 would have its G-PDMS electrodes replaced with the Pl/Ir wire electrodes (Figure 3.57). A 2mm exposed end of the Pl/Ir wire would extrude perpendicular from the Interface's cooling face. It is this section that would have the PEDOT encapsulated drug deposited on. It is designed to puncture a hole through the dura mater when the Interface is mounted during the *In Vivo* experiments. Achieving this setup requires the Pl/Ir wire to be mounted into the Interface base when the G-PDMS electrodes are printed in. Four manufacturing steps were devised for the drug delivery electrode integration (Figure 3.58A).

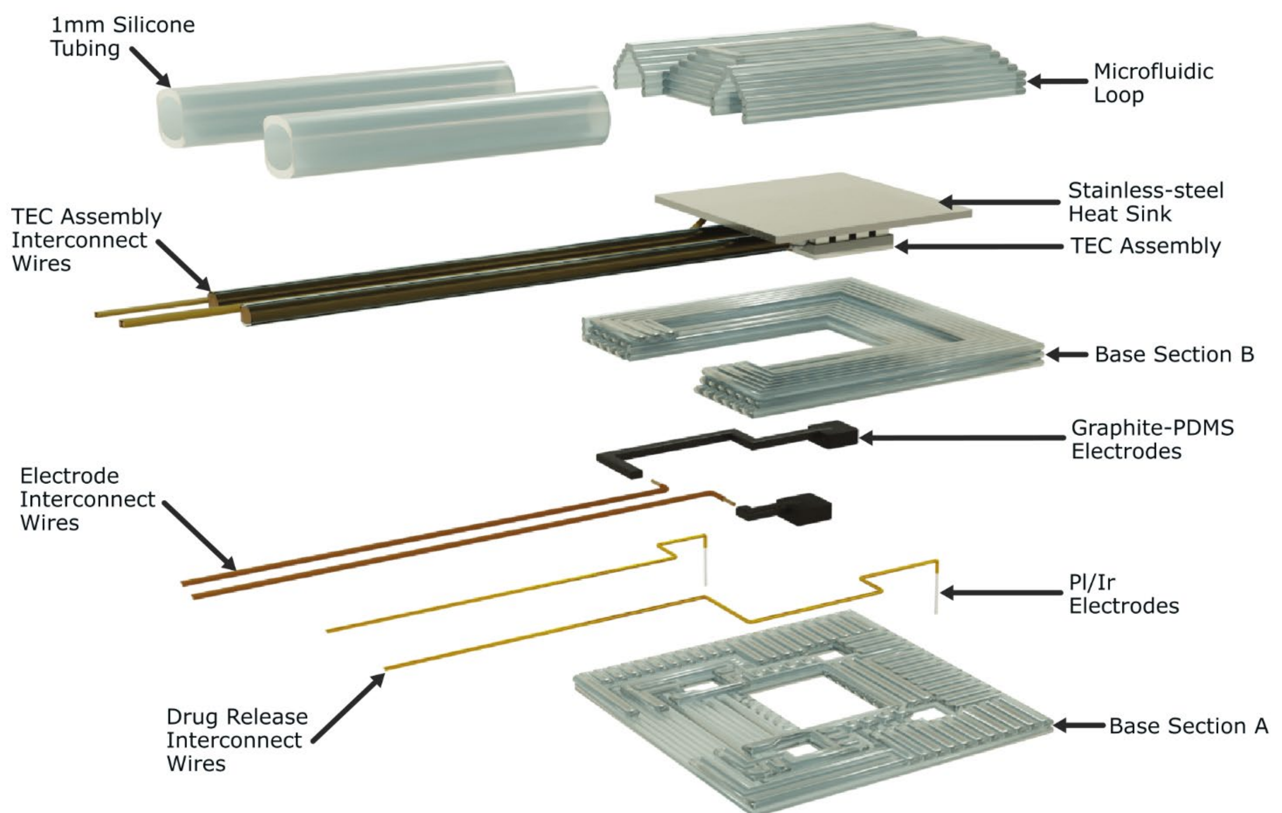


Figure 3.57 Interface Version 5 local drug delivery variant visualisation.
Two G-PDMS electrodes are replaced with Pl/Ir wires to support localised drug release through electro-active hydrogels. Each Interface section is labelled accordingly. Connection to the Interface Support Electronics is achieved through the interconnect wires from the TEC Assembly, Graphite-PDMS electrodes, and drug release electrodes.

The sheath around the Pl/Ir wire electrode end has to be pre-measured and removed before it is slid between the printing glass slide and layer 1. The internal Interface Pl/Ir wire section is shaped to conform with E1 & E4 internal electrode print channels and are routed out of the Interface to be integrated with the Interface connector (Figure 3.58B). Before the E3 & E2 G-PDMS electrodes are printed with the Base Section B, the Pl/Ir internal electrode channels are filled level to the top of Layer 2 with SE1700 to secure the wire in place. No further processing is then required until the Interface fabrication is complete when the Pl/Ir Electrodes are soldered into the Interface connector, the exposed tips are mechanically abraded to remove any thin-film silicone skins that could have formed on its surface, and the tips are bent out to be perpendicular to the Cooling face.

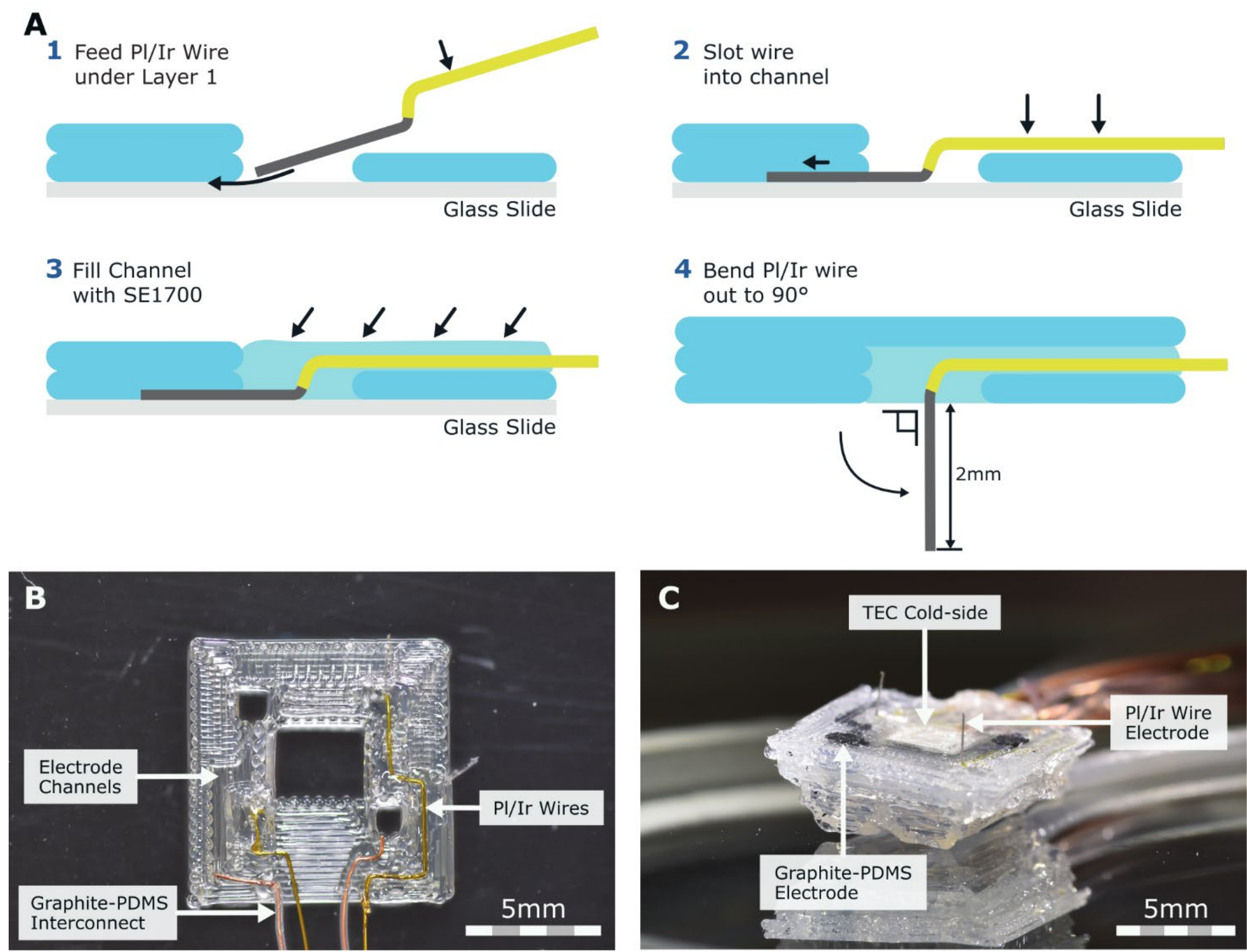


Figure 3.58 Electrode modifications to enable local drug delivery.
A. Construction flow of the Pl/Ir Electrode. (**1**) The Pl/Ir wire is bent to the internal electrode print channel form and its 2mm exposed tip is inserted between Layer 1 and the glass slide. (**2**) The wire is placed into the channel so that it sits flush against the printed material. (**3**) Electrode channel is hand filled with SE1700 to encapsulate the Pl/Ir wire before curing. (**4**) After the fabricated Interface is removed from the glass slide, the 2mm exposed Pl/Ir wire is bent into a position perpendicular to the cooling plane. **B.** Pl/Ir wire mounted into the electrode 1 & 4 positions. The internal electrode print channels for these have been filled with SE1700 and cured. **C.** Final drug release electrode positioning post Interface fabrication. Once erect, the electrodes are ready to have the PEDOT encapsulated drug deposited on the its surface.

This fabrication flow was successfully implemented with the production of an Interface v5 sample with the drug delivery electrodes (Figure 3.58C). The localised drug delivery modality only progressed to this state of completion by the PhD projects end. The next intended step would have been to test PEDOT deposition onto these electrodes and, with the drug release hardware in Section 4.8.8, to demonstrate drug releasing both in *In Vitro* studies before being combine with the other modalities within *In Vivo* studies.

3.10.5 Interface Power Consumption

Production of the prototype Interface Support hardware and the inclusion of wider system power monitoring now enabled better system profiling of this area. Current sense resistor placement at the battery terminal, uFluidic shield connection, and on the TEC Driver produced the data necessary to breakdown systems power usage.

Profiling of this was undertaken with an Interface v5 in an improved *In Vitro* thermal model (Figure 3.59A). A main change to the thermal model was the addition of a 3D printed Polylactic Acid (PLA) frame. The frame gives better control over the thermocouple placement accuracy relative to the cooling face through mounting points in the frame.

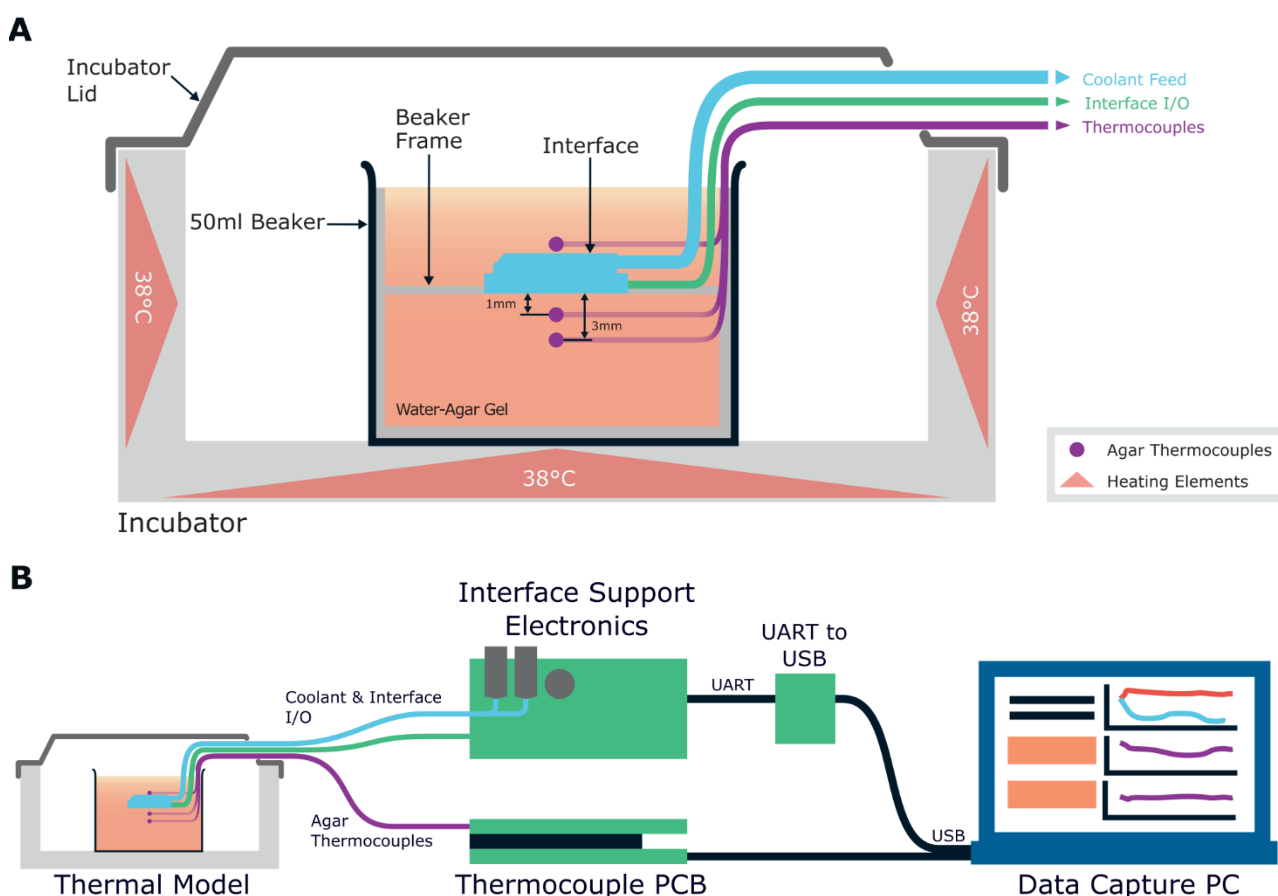


Figure 3.59 In Vitro Hardware setup with the Interface Support electronics.
A. A thermocouple PCB can be used to monitor two of the three sensors in a variation on the previously presented In Vitro thermal model using the incubator. **B.** Full *In Vitro* experimental setup of the hardware to support data ingest and Interface control.

The thermal model is now housed within a 50ml glass beaker to make the model production process easier. With the addition of the PLA beaker frame, care had to be taken when casting the water-agar gel. Before the water-agar solution is poured into the beaker, the solution is left to cool down to 55°C. This prevents the PLA frame from breaking due to the PLA being heated pasted its glass transition temperature (~60°C). This set of *In Vitro* experiments also used the updated Interface Support hardware detailed in Section 4.8. The thermal model thermocouples are still required to use a TEC Control hardware to support their use (Figure 3.59B).

The aim of this study was to perform a set of cooling runs to determine the system power consumption during the nominal Interface function and how that consumption changes upon the activation of a focal cooling run. Current and voltage data is recorded for the overall system, the uFluidic shield, and TEC driver output. Using the overall system and uFluidic shield data both the TEC system and the core system power consumption can be calculated. The TEC system differs from the TEC driver output. The driver output is the down regulated, voltage signal driven through the TEC whereas the TEC system is the summation of the power consumed by the TEC, the TEC driver, and the TEC regulator from the battery. The core system represents the power that is consumed by all electronics excluding the uFluidic system and TEC system.

Two representative cooling runs are provided to show the power consumption differences between two temperature reference cooling runs (Figure 3.60A). The first cooling run produces a -15°C ΔT and the second produces a -10°C ΔT. Alongside these cooling run temperature profiles, the power consumption breakout is provided (Figure 3.60B).

Throughout the study, in both its idle state and during cooling, the core systems power consumption stays at a constant level with it drawing an average of 0.465W. The uFluidic Sheild power consumption, as expected, increases during a cooling event when compared to the system idle state. Whilst the system is idle, the uFluidic shield consumes a constant 0.127W. The primary consumer is the SPM-041 shield which exclusively controls the piezoelectric air pump. Onboard it contains a microcontroller, supporting electronics, and LED indicators that is expected to draw the majority of the power recorded. During a cooling event, there is a large increase in uFluidic shield power consumption to 1.44W. The majority of this increase is required to actuate the air pump. This stays constant over cooling run until the pump is deactivated. This behaviour is expected as it is programmed to operate at a single power level.

There is scope for optimising the operation of the pump during cooling event which could lower the total energy consumed by the system. These optimisations would entail implementing a relation between piezoelectric pump power and the level of heat dissipation required. This would manifest as varying the pump power level depending on what cooling stage is currently occurring or modulating the pump power based on the depth of cooling that is required to be achieved. Another route for optimisation, is utilising the SPM-041's onboard pump PID controller. This controller can be set to regulate the pumps power based on either a desired set point pressure, or a desired coolant flow rate through connecting in a flow meter sensor to the SPM-041 shield.

TEC system power consumption is only observed during cooling events – as designed. The system presents the largest variation in power consumption of all of the systems. It results in the largest peak power recorded – being 5.96W – that is observed in the 15°C and 10°C ΔT runs. However, after the initial power spike, the TEC power consumption reduces and levels out once the TEC cold-side reaches its temperature reference point.

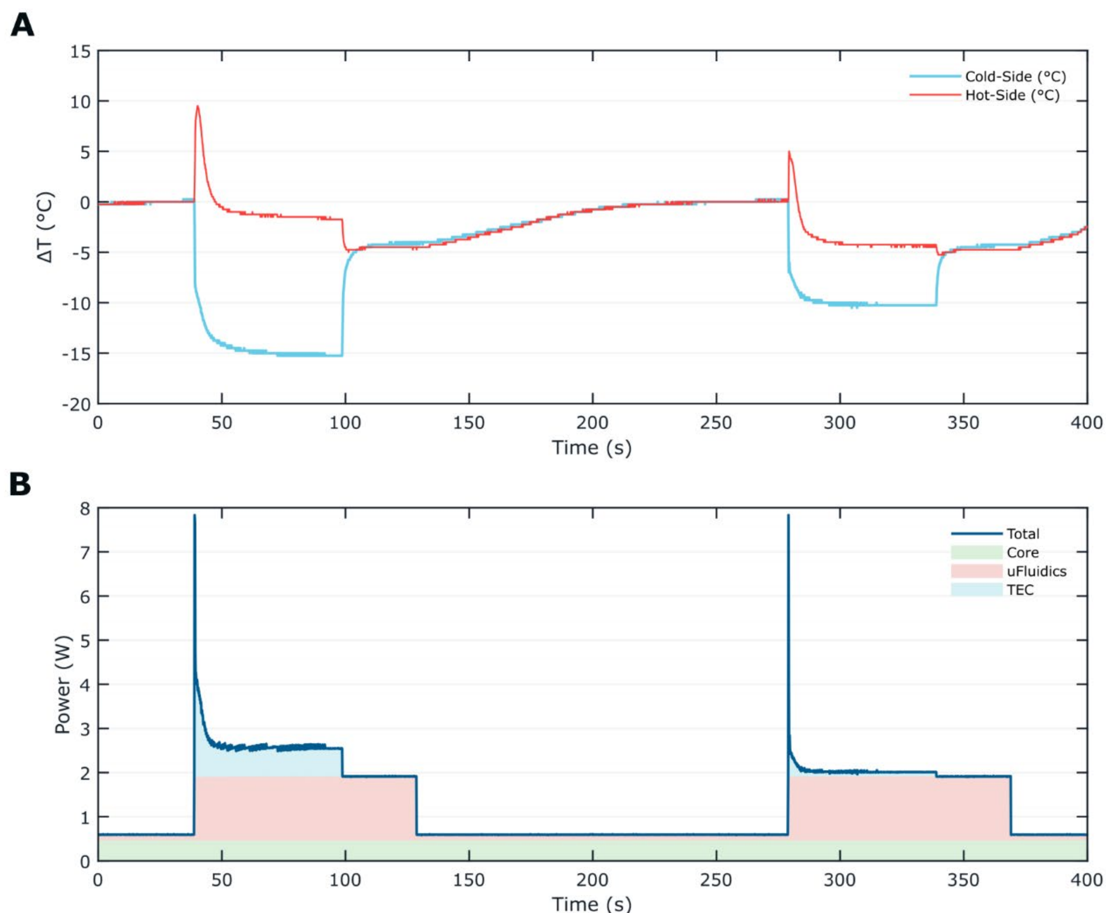


Figure 3.60 Interface Version 5 power profiles over two cooling runs.
A. TEC hot-side and cold-side temperature profiles during a 15°C ΔT, and a 10°C ΔT cooling run. Use of the prototype Interface Support Electronic and the piezoelectric pump actuated microfluidics produce an improved cooling performance. **B.** Power draw of the complete Interface system during the two cooling runs. Total power draw is colour coded to denote individual system consumption. The TEC colour includes the TEC, the TEC driver, and TEC power regulator; the uFluidics colour include the piezoelectric air pump and shield, fluid flow meter, and reservoir air valves; and the Core colour includes all other systems on the digital and analogue power rails (microcontroller, sensing ICs, etc).

The average TEC system power over the last 30s of each cooling run was 0.659W for a 15°C ΔT, and 0.103W for a 10°C ΔT. This presents an unexpected outcome of the TEC system on average consuming the least amount of power during steady-state cooling in the 10°C ΔT cooling run when compared to the other systems. During the 15°C ΔT cooling run, the TEC system consumed more power than the core systems but did still consume less than the uFluidic shield.

Monitoring of the TEC Driver output is an important function during a cooling event to ensure safety whilst operating. Figure 3.61A provides the voltage profile recorded out of the TEC Driver during the same cooling events displayed in Figure 3.60. With the TEC specified maximum voltage being 1.4V, a step-down buck regulator was implemented on the Interface Support hardware to supply this from a nominal 7.4V battery input. This step-down regulator means the peaks in the TEC current profile doesn't translate to larger power spike in the power drawn from the battery (Figure 3.61B). This is due to the regulator performing power conversion akin to how a transformer functions rather than expending used power as heat as the previous LDO TEC regulator did.

Of note is the TEC Driver voltage profile during the idle state. This steps up to the required voltage during a cooling run but after there is a slow reduction in the TEC voltage after the cooling run has ended. This slow reduction in TEC potential could be attribute to the LC filter used to smooth out the voltage and current ripples in the supplied TEC power. Energy is stored within these components during active cooling to function. However, when the driver is halted, the driver's TEC I/O pins are set to a high-Z state. Any energy left in the filters has no 'easy' discharge path. Thus, the system can only slowly discharge over time due to system losses between cooling runs. Now observed, future works have to have a focus on reducing this stored charge in the filters if this hypothesis is proved correct.

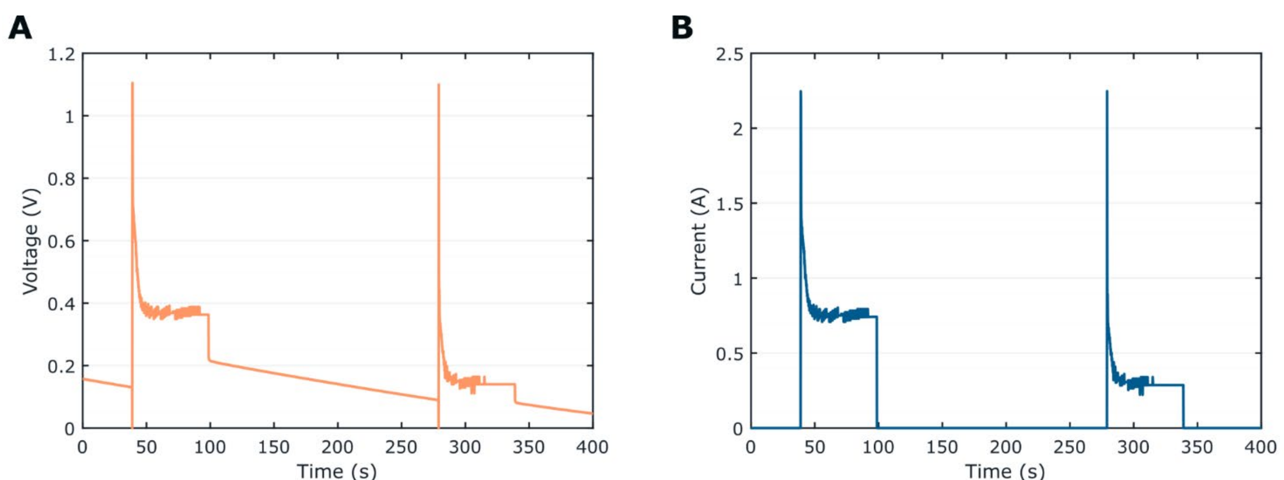


Figure 3.61 TEC Driver power profiles of the Interface Version 5 cooling runs
A. TEC Driver voltage profile during cooling runs to a 15°C ΔT and a 10°C ΔT. **B.** TEC Driver current draw profiles over the same set of cooling runs.

3.11 Interface Design Summary

This chapter focused on the development of the soft, multimodal neural Interface. The intention was to produce an implantable device that can neuromodulate through focal cooling, record neural signals and provide localised drug delivery at the site of an epileptic foci. The Interface structure was primarily designed to support the focal cooling modality enabled by a micro-TEC element. With its challenging thermal design, heat dissipation modes were investigated *In Silico* where it was determined that removing TEC pump heat could not be sustained by CSF flow. Thus, an active Microfluidic Loop design would be required.

The TEC Assembly enables complete support for the focal cooling modality. It is constructed from a micro-TEC element, thermocouple temperature sensors, and a Heat Sink. These parts are bonded together using a biocompatible thermal epoxy. *In Silico* modelling was used to optimise the thermal throughput of the Assembly. Studies specifically focused on the Heat Sink design. Initially constructed it was printed using a Thermal Silicone Composite developed during this research. However, after proving ineffective, it was replaced with a stainless-steel plate Heat Sink.

3D printing techniques were implemented to dispense SE1700 silicone for the manufacture the Interface's body using the 3D Discovery Bioprinter. This bulk silicone structure is used to integrate the separate modalities together. The Base Section supports the TEC Assembly and the printed Graphite-PDMS Composite electrodes. A Microfluidic Loop is printed atop the TEC Assembly to guide coolant flow over its Heat Sink and remove excess system heat during cooling. Applying continuous printing techniques to the Microfluidic Loop and the electrodes enhanced print consistency and reliability. The completed Interface unit is 9.5 x 9.5 x 2.3mm.

An *In Vitro* thermal model was produced to replicate the thermal environment present at the intended site of implantation. Water-agar gel was used as a neural tissue thermal proxy. Profiling of the Interface demonstrated that the system is able to produce localised cooling with a >-15°C ΔT from nominal at cooling rates >3°Cs^{-1}. Meeting the literature derived requirements for a focal cooling device to be able to have a suppressing effect on seizure activity. The system is able to achieve this cooling through consuming an instantaneous peak power of ~7.8W at the onset of cooling and then maintaining a -15°C ΔT whilst consuming only ~2.6W of power.

Work began to integrate the localised drug delivery modality into the Interface structure. Platinum Iridium wires are used to replace a pair of printed electrodes to support the deposition of PEDOT encapsulated anti-epileptic drugs. Manufacturing of these drug delivery electrode was demonstrated with testing of the system discussed for future work.

Chapter 4

Electronic Hardware for Interface Support

With the unique nature of the Interface's multimodal functionality, an equally unique electronic hardware suite was required to support it. Hardware for the Interface served two purposes: to enable Interface testing during *In Vitro* and *In Vivo* studies, and to demonstrate the potential for a portable system that could function within the clinical setting. Size and mass of the electronic hardware were to be kept as small and lightweight as possible with the aim for the electronic hardware revisions to tend towards modern smartphone size.

This chapter will cover the details of the electronic hardware that were developed for this PhD. General systems information from the development process will be covered first. Details of the tools used and core design elements will be followed by a breakdown of the electronic hardware (Figure 4.1).

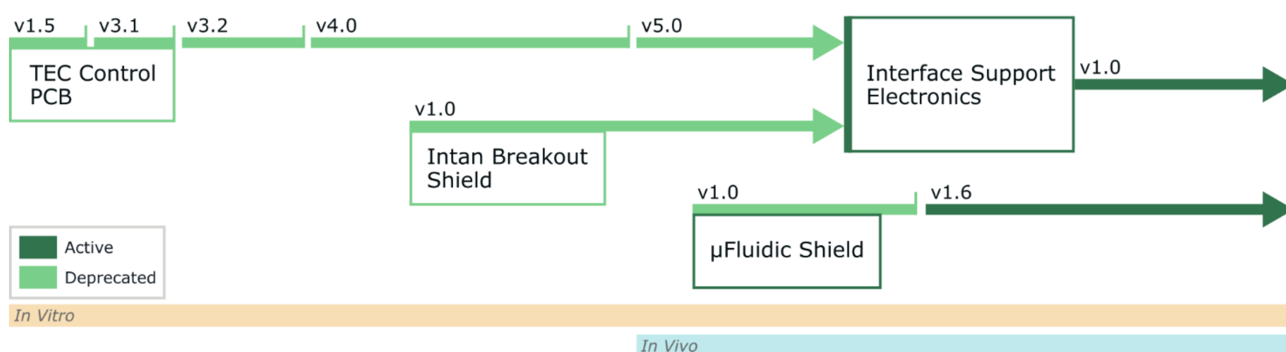


Figure 4.1 Electronic hardware development timeline.
Development order is from left to right. Line colour indicate current status of the electronic hardware as either active or deprecated. Experimental use is marked by the *In Vitro* & *In Vivo* timeline along the bottom. System versions not displayed were not used for either *In Vitro* or *In Vivo* studies.

4.1 Schematic & PCB Design

Design and production of PCBs is commonly undertaken using an Electronic Design Automation (EDA) package. EDAs integrate multiple software tools, needed for PCB production, into an all-in-one solution that streamlines the hardware production flow. The main software tools supplied within these packages are the schematic capture tool and a PCB layout tool.

Schematic capture is for the initial circuit design stage. Within this tool, all circuits are laid out diagrammatically. Components are assigned values and labels. Connections from these components are either wired together or allocated 'not connected' label. This tool provides a clean circuit layout view for the designer. It abstracts away component package details in favour of human-readability. The PCB layout tool is the final circuit design stage. It is used to set the physical PCB layer options on which the component footprints and interconnect wires are arranged. Mechanical elements are defined on the board to dictate the PCB edges, routed inserts, and/or drilled holes. Layout design can be reviewed by conducting design rule checks. These checks compare the PCB layout against a PCB manufacturer's production specification to verify in will meet fabrication tolerances. Apart from these two tools, EDA vendors can choose to add more specialised tool capabilities within their own suite.

For this project, the KiCAD EDA is utilised to design all PCBs (Figure 4.2). KiCAD is an open-source EDA software suite released under the GNU General Public License v3. It provides professional grade PCB design capabilities alongside an ecosystem of user developed add-ons that can expand its base functionality. Release version 5.1.6 was used to design the TEC Control shield and the Intan Breakout shield. Release version 7.0.5 was used to design the Interface Support PCB and the µFluidic shield. PCB manufacture was conducted by Beta Layout GmbH based in Germany.

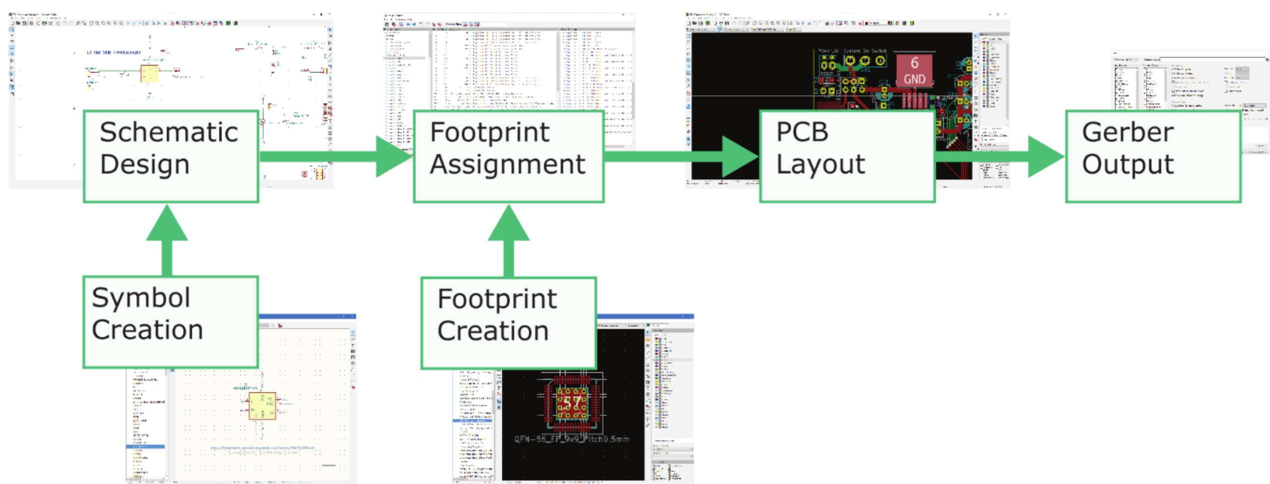


Figure 4.2 PCB hardware design flow using the KiCAD EDA suite.
All electronic hardware produced was designed using this system. Custom symbols and footprints were derived from a component datasheet as required. Hardware schematics available on request.

4.2 Microcontroller

At the heart of the Interface Support hardware is a microcontroller (μC) platform. Microcontrollers are programmable computational devices that are packaged into a single, small integrated circuit (IC). These ICs contain the processor, memory, and input/output (IO) peripherals. The IO peripherals provide a means of communicating with other discrete ICs and interfacing with the surrounding electronic architecture. With a microcontroller at its core, a stand-alone system can be produced where Interface control and monitoring can be achieved in a closed loop.

Computational capabilities of microcontrollers are highly variable and the selecting one is application dependant. IO count, computational power and the occurrence of hardware-accelerated functionality is unique to each model. The chosen microcontroller for supporting the Interface will require tight integrated into a portable device requiring the support of potential online seizure detection. This translates into the requirement for a low power consumption μC that has a hardware-accelerated digital signal processing (DSP) block within it. Options that align with these system requirements lie in the ARM Cortex-M Microcontroller range.

4.2.1 ARM Cortex-M

ARM is a processor IP licensing company that has produced a variety of microcontroller architectures within its Cortex-M range. These architectures enable scalable solutions in terms of power efficiency and processing performance. As part of this ecosystem, Arm provides CMSIS (Common Microcontroller Software Interface Standard) - a standardise set of system and peripheral register access labels for all Cortex-M processors. This simplifies porting code between processor versions. For this project it means that if the seizure detection algorithm requires greater computation power to complete processing neural data within allocated timings, the microcontroller will be easily upgraded to a more powerful version.

4.3 Electronic Systems

A general set electronic sub-systems are required to support the base functionality of the Interface (Figure 4.3). These systems were determined after the Interface cooling modality requirements were finalised. For the electronics, at least two separate power regulators will be required; a 3.3V regulator for component operation and a TEC regulator capable of handling its non-standard power requirements. Each modality will have individual electronic hardware needs – with the TEC requiring a high-current driver and a microfluidic pump system; the neural recording electrodes requiring signal conditioning and digitisation; and the drug delivery requiring a high-accuracy pump or voltage control circuit. At its core will be the microcontroller to monitor and control these systems in a safe manner.

Power for the electronics is intended to be supplied by a portable battery source. It removes system complexity that would arise from sourcing power from a mains power grid connection. This simplifying both the power input power regulation and *In Vivo* study design especially concerning the potential for grounding loops and noise production. Having the electronics battery powered also aligns with the systems final intended use as a portable device that patients would carry with them daily. To that end, power efficiency and system size should be considered throughout the electronic design process. The final and expanded block diagram for the Interface Support hardware can be found in Appendix E.

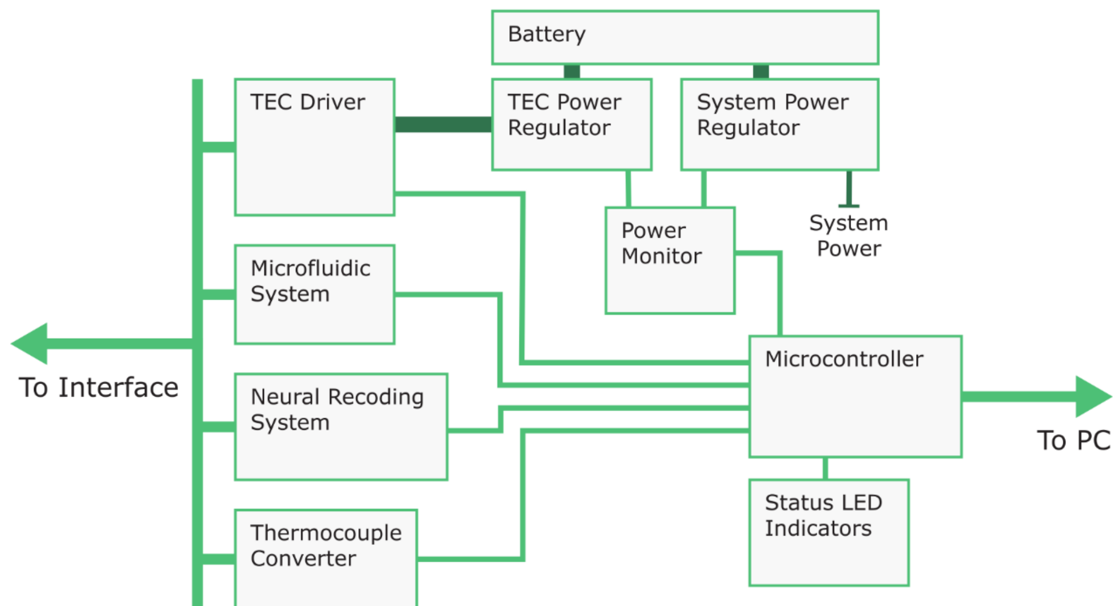


Figure 4.3 Electronics overview block diagram.
Gives a general understanding of the electronic systems required to support Interface functionality. This is used as the base design structure for all PCBs developed for the Interface.

4.4 TEC Control Shield

This section details the first set of experimental electronic hardware developed to support Interface modality function and data collection. A custom shield was designed to be compatible with the STM32L476 Nucleo-64 board and to only support the focal cooling modality. Systems required for this involved: supplying a controllable power signal to the micro-TEC, monitoring the TEC Assembly thermocouples, and driving the microfluidic impeller pump.

This custom shield was designated the name "TEC Control" shield. Its series consisted of five incrementing design versions labelled v1 through to v5. Boards were marked with version numbering in the form $a.b$ where a is the major design versions in which significate layout changes or electronic system additions were performed, and b indicates minor design revisions involving small layout corrections or component alterations[5]. The TEC Control hardware series supported the operation of Interface Versions 1, 2, 3, and 4. The series primarily facilitated *In Vitro* studies – driving Interface evolution until Version 4. TEC Control v5 shield was used in conjunction with the Intan Breakout shield (Section 4.5.2) during the initial *In Vivo* experimentation for setup verification. Circuit and component information within the following sections will primarily focus on those found in the v5 shield systems as the most mature design.

It was eventually necessary to develop a highly integrated, monolithic PCB that was used to continue with the *In Vivo* studies. This occurred concurrently with the introduction of the Interface Version 5 design. The discussion on the motives for this development will be in Section 4.6.

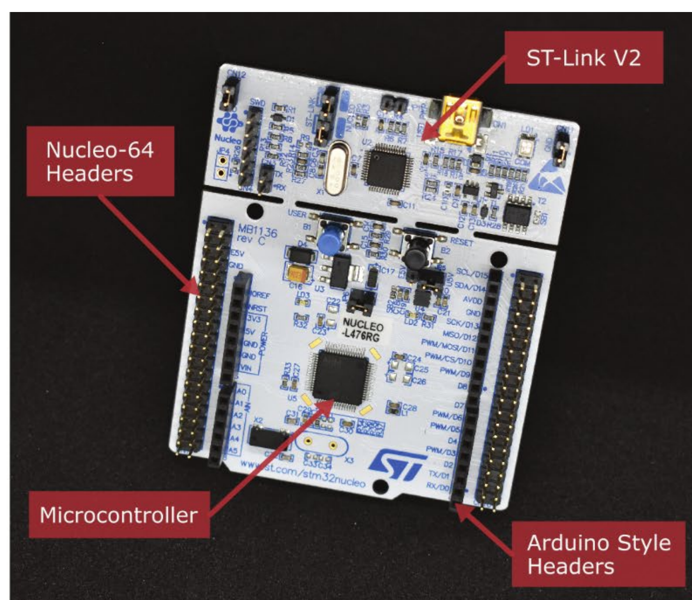


Figure 4.4 An example Nucleo-64 board with the STM32L476RTG.
The labelled Nucleo-64 headers is mirrored across the board to provide a standard hardware layout template for the TEC Control PCB development.

[5] Component changes are largely attributed to post-pandemic silicon production shortages. This is discussed in the sections effected.

4.4.1 Development Board – STM32L476

Selection of the microcontroller for hosting the system firmware and the seizure detection algorithm revolved around finding the balance between power efficiency and computational power. For supporting the potential seizure detection algorithm computation, there is the requirement for having a Floating-Point Unit (FPU) and a DSP as discrete hardware modules within the microcontroller. These modules accelerate non-integer calculations and signal processing functions through dedicated hardware. They reduce the number of instructions required for the calculations and off loads it processing from the central processor.

The STM32L476RTG microcontroller (STMicroelectronics, Switzerland) was selected as the primary processor to host the system firmware and support the TEC Control shield development. The L476RTG is a silicon implementation of the ARM Cortex-M4 processor architecture. It was designed as a low power variant within the M4-based chipset, the processor has both discrete FPU and DSP hardware modules. It is capable at operating with a 80MHz core clock frequency and has 1MB Flash Memory with 128KB SRAM. This microcontroller should provide suitable overhead for Interface Firmware to operate and support future software expansion.

Initial hardware development would require incremental implement of each hardware sub-system and will require extensive testing to ensure reliability. To make this process smoother, the STM32L476 microcontroller was sourced in the Nucleo-64 development board format (Figure 4.4). The board has a built-in ST-LINK V2 debugger that is accessible through a Universal Serial Bus (USB) cable. Operational function can be modified on the board through several header pin sets and solder bridge pads.

The Nucleo-64 format provides a standardise header template to design the TEC Control shield with. Access to the microcontrollers GPIO pins is granted through two sets of header pins. One provides an Arduino Uno-style header layout. This layout limits GPIO access in favour of being compatible with Arduino's popular shield ecosystem. The other set is the Nucleo-64 specific header layout. It grants access to all GPIO pins available on the STM32L476's 64-pin LQFP package. This allows the PCB to be easily ported to another Nucleo-64 boards if required. However, a limited selection of pin allocations does vary between boards which must be observed if this was to be required.

4.4.2 TEC Control Power Supplies

To have all sub-circuits on the TEC Control shield operational, three independent power rails were required. Each have to be regulated to different voltage levels. Regulation of these rails is achieved using low-dropout (LDO) regulators set to specified voltage output. This regulator type provides a low complexity solution which reduced time spent needing to locate and debug any power related errors. As there is no switching component to the voltage regulation, they also provide an innately low noise power signal. LDO voltage regulators use a resistive divider at its output to provide output-relative feedback. That voltage allows the LDO regulator to self-correct if there is any output deviation from the desired voltage value.

Each LDO regulator is located as close to its respective sub-system as can be achieved on the shield PCB to keep track length short. These locations are marked on Figure 4.5. Description for the TEC regulator is provided a separate Section 4.4.4. For the centrifugal pump regulator, details are found in the Section 4.7.1.

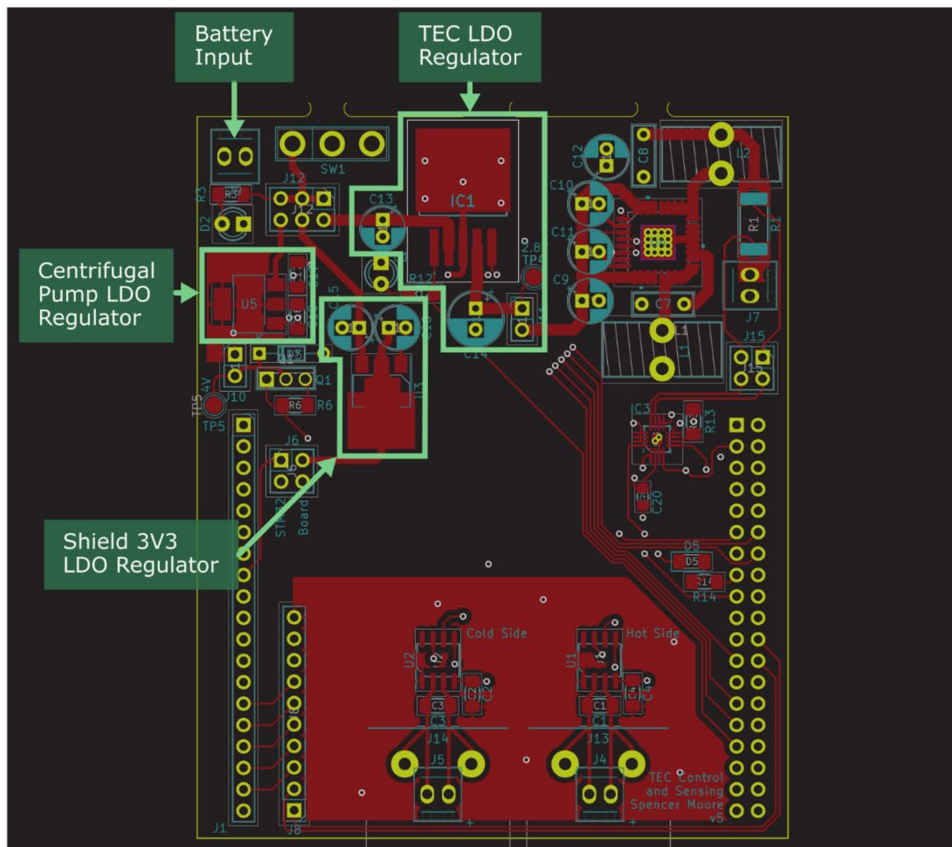


Figure 4.5 Locations of the three regulators on the TEC Control shield.
These LDOs service the microfluidic centrifugal pump, the TEC, and the general shield 3.3V voltage rails.

General Systems LDO Regulator

General systems on the shield require a 3.3v voltage to function. These systems include the Nucleo-64 board, thermocouple amplifiers, and the power monitor. Fixed, 3.3v LDO regulators are readily available due to the voltage being widely implemented in the electronic sector due to the LVTTL standard. A fixed regulator means that the resistive voltage divider is built into the regulator IC – reducing the required component count. The Microchip TC2117 3.3v Regulator was chosen for use. The IC is rated to supply 800mA. Figure 4.6 provides a guide to the circuit used for this voltage regulator for the PCB.

Battery Pack

These voltage regulators will be supplied power by a battery source. The battery pack used is an Ansmann 2S2P lithium-ion battery pack with a 7.2V nominal voltage (part number 2447-3049-01). The pack can provide up to a 5A constant discharge current. This lies beyond the absolute maximum board current draw of 3.4A and provides suitable safety overhead.

Ground Layout

Supporting the Interface cooling modality required the use of components that sample analogue signals. These systems involve the conversion of them into the digital domain. The conversion process can be sensitive to the high frequency noise which is commonly a side effect from digital circuitry. To prevent digital signal noise in the analogue circuitry – specifically for the thermocouple amplifiers – a split ground plane was employed. Digital noise impacts analogue circuit when the current return paths overlap or cause ground loops. Split grounding layout prevents digital and analogue current return paths from influencing each other by physically separating their grounding paths. It is achieved by having two component types on two isolated planes that join at a single point (referred to as the 'Star point'). This single point is commonly the circuit power input ground. On the TEC Control shield, the star-point is located in the centre of the shield PCB to allow for communications routing to happen in a more accessible fashion.

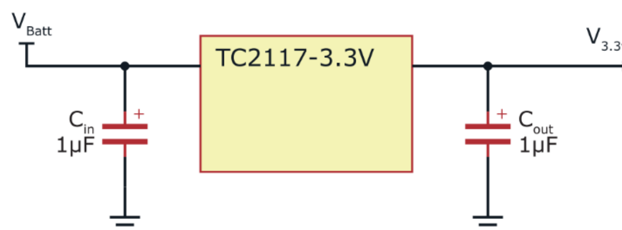


Figure 4.6 Shield 3V3 LDO regulator circuit diagram using the Microchip TC2117.

4.4.4 Data Retrieval – USART

Data generated by the firmware and Interface would be useless without a retrieval method from the hardware. This data could either be stored locally on the TEC Control hardware or it could be sent off to a connected host PC. Concerning development and experimental setup needs, the latter option was the most preferable. This allows real-time monitoring of the systems alongside the ability to establish a command system to alter firmware parameters and control Interface function.

Since the Nucleo-64 board is orientated for systems development, it contains a pre-configured Universal Synchronous Asynchronous Receiver Transmitter (USART) to USB converter within the ST-Link V2. The USB connection to the board can then simultaneously support data output and firmware debugging. A USB cable is the only extra hardware needed to allow the TEC Control hardware to send structured data packets to a host PC.

4.4.5 TEC Driving Hardware

TEC operation required hardware that could supply the necessary power in a digitally controllable manner. It had to be able to supply a DC source with an I_{max} = 2.4A at a U_{max} = 1.4V. These specifications are provided by the 1TC17-16178-1617.H datasheet to produce its maximum temperature difference.

Control of the supplied TEC power was achieved using a Pulse Width Modulation (PWM) signal output by the microcontroller. This PWM signal provides the ability to vary the level of TEC cooling from 0% to 100%. Directly driving the TEC using PWM from the microcontroller IO pins was untenable due to their inability to supply the minimum current magnitude. Thus, a TEC specific driver and power system will have to be implemented to handle these higher currents (Figure 4.7).

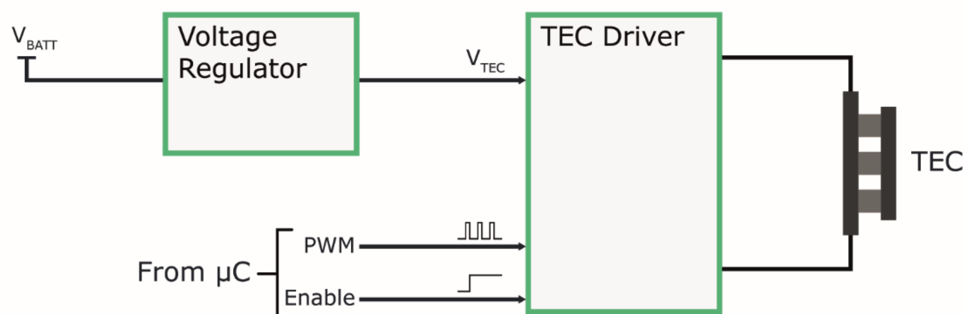


Figure 4.7 TEC power regulation and driver circuit block diagram.

TEC Power Supply

The LDO regulator utilised for the TEC was the MIC29312WU produced by Micrel INC. With a maximum supply current of 3A, it could supply the required 2.4A maximum current. Having this 0.6A capacity overhead reduced the potential for performance reductions due to component self-heating. Figure 4.9 is diagram of the circuit used to produce a 2.81V DC regulated output for the TEC driver. Resistive divider values of R1 = 156Ω, R2 = 123Ω provide the voltage reference of 1.24V into the regulator's Adj pin. The resistors were valued such that they drew the minimum specified 10mA required to sustain the regulator within its proper operational range. Doing so prevents the regulator output being unknown during operation.

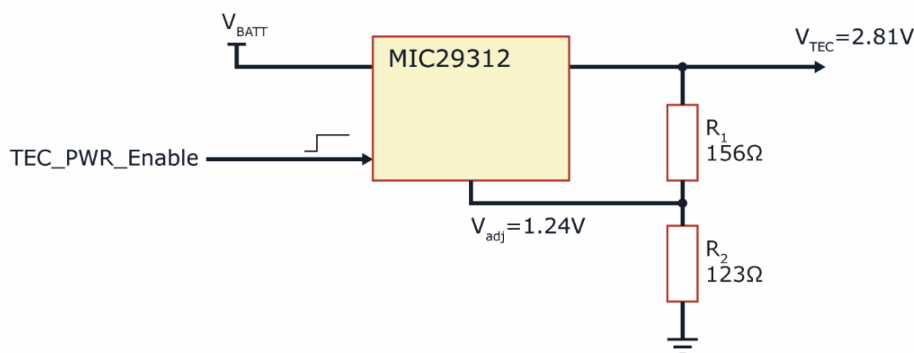


Figure 4.8 LDO regulator circuit for the TEC driver supply.
Resistive divider feedback maintains the 2.81V at the regulator output. Regulator enabling is controlled via a GPIO logic input from the Microcontroller.

TEC Driver Control

As incidence of TEC deployment within cooling instruments has increased over the past 20 years, a number of application specific integrated packages (ASIC) packages have emerged to simplify TEC driver electronic design. A high-current, TEC specific H-Bridge was selected for the TEC driver IC (DRV592, Texas Instruments). It is capable of driving a ±3A maximum current that is controlled through a PWM interface. This provides suitable performance overhead to prevent operational throttling. Other logic input control device shutdown, and driving output Hi-Z states. Combined with fault monitoring outputs, precise control and monitoring of the TEC could be achieved. However, the minimum specified driver supply voltage was 2.8V but the TEC is rated for a maximum of 1.4V. To prevent over-driving the TEC, the PWM control signal from the microcontroller will have an upper duty cycle limit of 50% initially hardcoded into the firmware before fully system limits could be tested.

For optimal TEC perform and longevity, only a DC control signals should be used to drive the TEC. An AC driving signal would cause the TEC to continuously flip which direction it pumps heat. This would result in an 0W average heat transfer between the TEC plates during function in an ideal system. Thus, any amount of AC within the TEC driving current will cause a performance loss. These AC signals found within a DC signal are commonly referred to as ripple currents. The ratio of ripple current in the TEC driving signal can be used to approximate performance loss:

$$\Delta T = \frac{1}{(1 + N^2)} \times \Delta T_{max} \qquad 4.1$$

where ΔT_{max} is the TEC's maximum specified temperature differential, ΔT is the predicted lossy temperature differential, and N is the ripple current to DC current ratio [143]. Ripple currents with peak-to-peak magnitudes greater than 10% of the DC magnitude are generally not recommended by manufacturers for driving TECs. Inputting the interface's TEC specifications into Equation (4.1) yields ~0.75°C performance loss when a 10% ripple current existing in the maximum driving signal magnitude. Reducing performance losses in the TEC is important to prevent permeant reductions in system robustness.

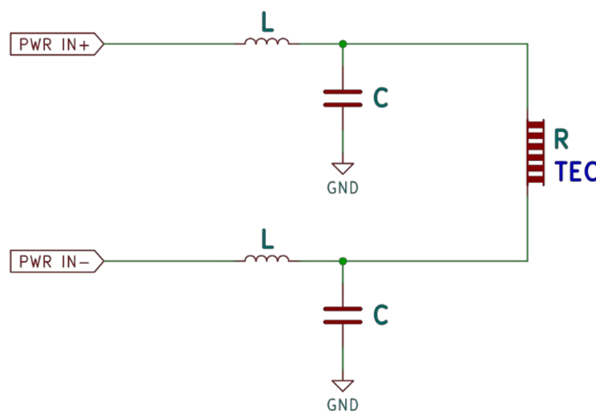


Figure 4.9 RLC low pass filter design for smoothing TEC driving signal.
Design for the attenuation of ripple currents within the TEC driving signal to prevent system cooling inefficiencies.

A low pass filter can be used to smooth out and reduce the magnitude of ripple currents within the TEC driving signal. A filter is constructed using an inductor (L) in series, a capacitor (C) in parallel and the internal resistance of the TEC element (R) in series (Figure 4.9). This forms a 2nd order passive RLC low pass filter. The frequency domain represented of this filter is given by the equation:

$$H(j\omega) = \frac{1}{-\left(\frac{\omega}{\omega_0}\right)^2 + \frac{1}{Q}\frac{j\omega}{\omega_0} + 1} \tag{4.2}$$

Where Q is the filters quality factor, ω is the PWM switching frequency, and ω_0 is the filters cut off frequency equal to $1/\sqrt{LC}$. Full derivation of this equation is found in Appendix E. Since it is the attenuation magnitude that is of concern, Equation (4.2) can be simplified down to just its real domain components. Whilst also converting from radians to Hertz, the resultant equation is:

$$|H_{LP}|_{dB} = -40\log\left(\frac{f_s}{f_0}\right) \tag{4.3}$$

where

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{4.4}$$

and

$$f_s = PWM\ Frequency \tag{4.5}$$

where f_0 is the circuits resonant frequency, f_s is the control PWM signal frequency, L is the filter inductance, and C is the filter capacitance. 312.5kHz was chosen as the TEC control PWM signal frequency. This value provides a balance between a high switching frequency and microcontroller timer resolution limits. A suitable target for the filter's resonant frequency is typically an order of magnitude lower than the PWM switching frequency at a minimum. This then gives the filter resonant frequency target to be a maximum of 31.25kHz.

An iterative process was conducted to select a pair of inductor and capacitor values using Equation (4.3). A range of standard component values were paired, and the ripple current outputs calculated until a suitable magnitude was determined. 43μH and 22μF were chosen from this process as the inductor and capacitor values respectively. The filter resonant frequency is 5.17kHz with a -71dB attenuation at 312.5kHz. It produces a 768μA ripple current in the driving signal which translates to a ripple current ratio of 0.032%. Only ~0.0767°C would then be lost from the TECs maximum temperature differential.

For the hardware implementation of the LC filter, through-hole (THT) components were used. This allowed the circuit to be prototyped on a bread board first. Low power test runs of the TEC control system on the breadboard provided the opportunity to efficiently debug the circuit design through quick component swapping and easy re-configuration without needing to de-solder. Toroidal inductors were selected for to their characteristically lower electromagnetic interference (EMI), and polymer capacitors were selected due to the need for both high capacitance and a non-polarised construction.

4.4.6 TEC Power Monitoring

Gathering power use data during TEC cooling allows for the cooling device condition to be monitored in real-time and provide a warning if there was a malfunction with the TEC during experiments. These data sets can then be used to optimise future battery capacity selection – particularly for the potential chronic *In Vivo* studies.

Enabling TEC power monitoring required a current sensing resistor (R_{sense}) to be put in series with the TEC. The voltage that develops across this resistor is directly proportional to the TEC current. By sampling this voltage, the TEC current could then be calculated from a known R_{sense} value. Changes in the TEC current over time could then continuously logged and used to calculate the total power use of the TEC element throughout use.

INA233 Power Monitor

For sampling the voltage, various manufacturers have developed discrete ICs for power monitoring applications. These ICs are designed to continuously log the voltage, current, and power values of the monitored circuit. These values can then be accessed via data bus. For the TEC Control shield, the INA233 (TI, USA) was selected for its flexible resistor placement and its I^2C bus interface.

Next the R_{sense} value had to be determined. The resistance select is dependent on the maximum current it is expected to measure and the sampling ADC's input range. The INA233 sensed voltage input range of R_{sense} is -81.92mV to 81.9175mV. Overrating the maximum expected TEC current (I_{tec}) to 2.8A provided a R_{sense} = 29.26mΩ. Rounding this to a standard resistor value of 30mΩ gives a maximum sense current = 2.73A that still provides a 10% safety margin. The TEC current resolution attained by the INA233 16-bit ADC is 83.3µA per bit. Again, using the maximum sense current = 2.8A and maximum sense voltage = 81.9175mV, the maximum expected power dissipated in R_{sense} is 229mW. This means that the current sense resistor had to be rated to handle ≥300mW.

This resistor was placed on the high-side of the TEC (Figure 4.11). The INA233 has two inputs (IN+ & IN-) for the current sensing resistor to sample the voltage. A separate input exists for monitoring the TEC bus voltage directly. A connection from the current sense resistors high-side to the VBUS input allows this measurement. This circuit was utilised for the TEC Control shield V1 & V2. However, with the silicone supply issues that occurred due to the pandemic, the INA233 IC became unavailable for use. A redesign of the TEC monitoring circuit was required.

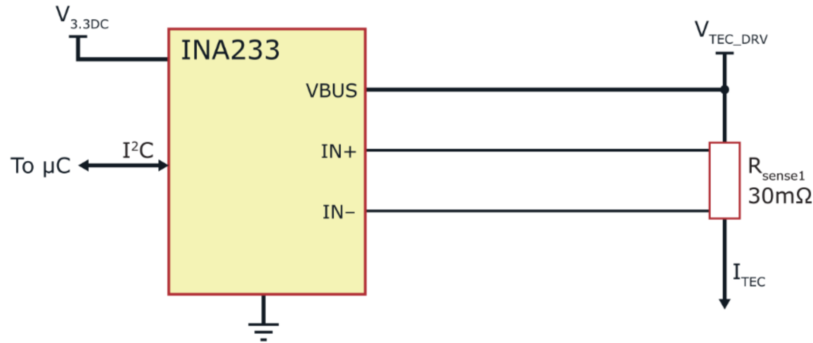


Figure 4.10 Block circuit layout of the INA233 power monitor IC.
The INA233 provides the ability to monitor the power of one input and communicate the results on request via I^2C. This circuit design was used on TEC Control shield V1 and V2

PAC1944 Monitor

The replacement power monitor IC was the PAC194x series. This IC range can have up to four independent R_{sense} inputs to monitor. It uses the I^2C bus as the INA233, but the programmed setup commands and data unpack functions would need to be re-written to accommodate the different IC. The PCB footprint had to be altered to fit the PAC194x pin layout. PAC194x series give the option to choose how many the inputs the IC supports – designated by the x (1-4). All sense inputs have their pins pre-allocated no matter which of the four versions is purchased. This provides a buffer against future shortage issues when they occurred and provides the ability to increase systems monitored in future hardware designs.

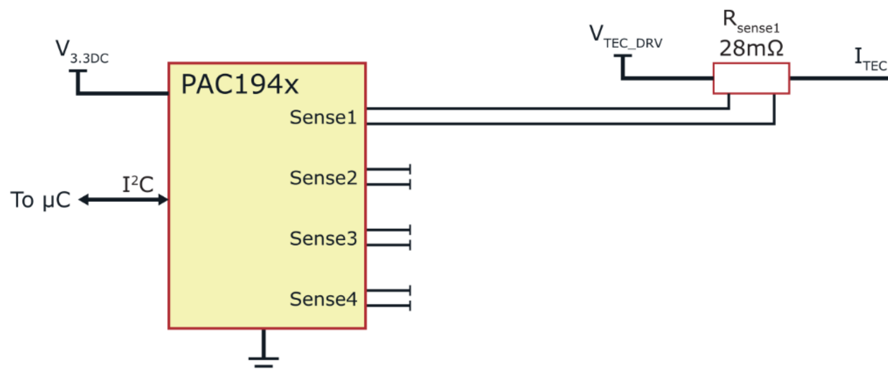


Figure 4.11 Block circuit diagram of the PAC1944 power monitor.
Used as a replacement for the INA233 IC. This IC has the ability to monitor up to four inputs. Data communication with the central processor is done via I^2C at request.

The last change to this circuit was the current sense resistor value (Figure 4.11). This change mainly came about due to a resistor package change. A THT bare-element resistor was used in the INA233 setup. This part specifications meant its power rating was >400% of the calculated requirement due to extreme caution when selecting components. Now the TEC driver circuit had been tested, the choice was made to replace this sense resistor with an SMD variant. The closest value found was a 28mΩ, 500mW resistor.

With a current sense resistance of 28mΩ and the PAC194x maximum voltage input from R_{sense} being 100mV, the maximum current that can sensed was 3.57A. The PAC194x 16-bit ADC gave a sensed current resolution of 108.9µA using the ±100mV full scale range (FSR) option. The PAC194x gives two FSR options for each input: 100mV or ±100mV. Which to select is use case dependant. If there is an expectation of current reversal or the desire for accuracy around 0V, then the ±100mV option would be chosen. If accuracy around 0V is not needed but an increase in current sense resolution is, then the 100mV option would then be more suitable.

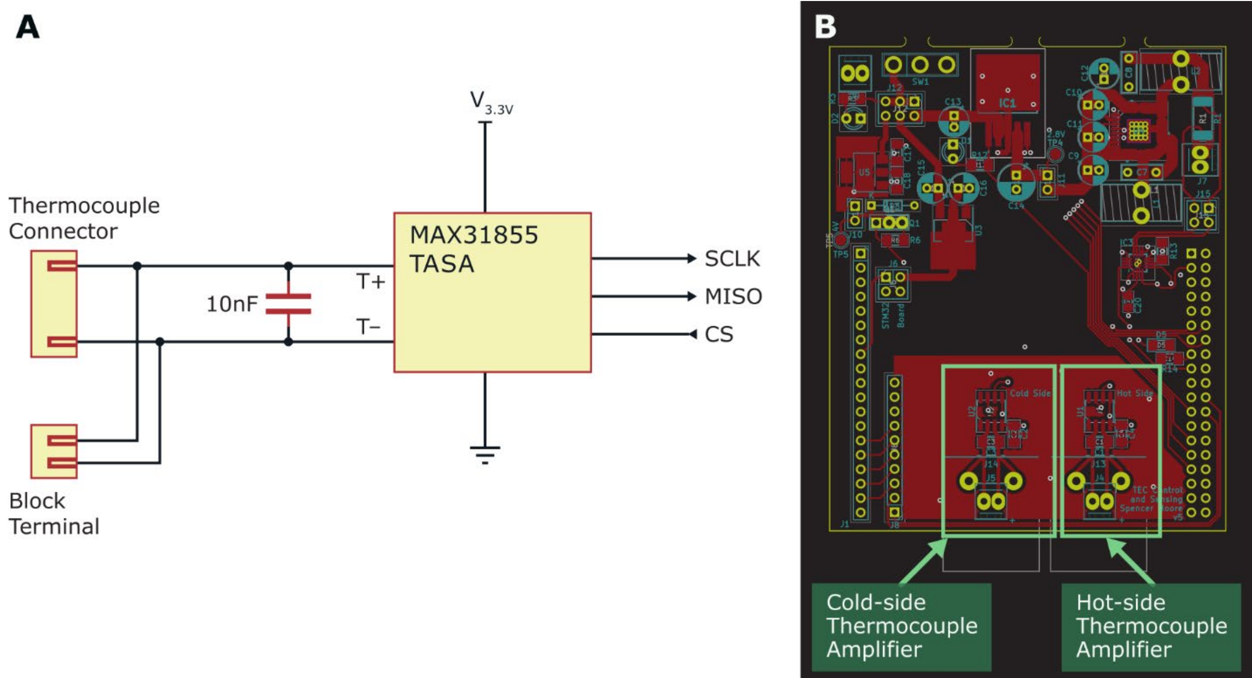


Figure 4.12 Thermocouple amplifier circuitry on the TEC Control shield.
A. Implementation of the MAX31855 thermocouple amplifier. The data is retrieved from the IC through the SPI bus and only provides data output. The 10nF differential capacitor on the input filters noise from thermocouple signals. **B.** Thermocouple amplifier location indicated on the TEC Control shield v5 schematic. A large local ground plane and being placed away from high-current circuitry provides thermal protection for the thermally sensitive inputs.

4.4.8 Thermocouples Data Acquisition

Reading the temperature from the two T-type thermocouples on the Interface relies on sensing a voltage that develops across their standardised metal junction. For a T-type thermocouple, the junction is formed from Copper and Copper-Nickel – also known as Constantan. Voltage signals created by this junction need be converted to the digital domain. The thermocouple could be connected directly to an Analogue-to-Digital Converter (ADC) to perform this operation. However, there are elements of thermocouple implementation that have to be considered before the signal interface electronics are designed.

T-type thermocouples present very small signal to be measured. This thermocouple type has a junction sensitivity of 42μV/°C. Converting signals this small requires either the use of an ADC with a high bit resolution, or using an amplifier to boast the signals level before conversion takes place. Implementing these solutions would require careful PCB layout and component noise control.

Another consideration, specific thermocouple sensor implementation, is how the signal wires are connected to the shield before conversion. Junctions of dissimilar metals are formed at these connection points that can create parasitic electromotive force (EMF) that will add measurement errors to the temperature reading. These junctions are referred to as 'cold junctions'. Compensation for this parasitic EMF noise is derived from monitoring this junction's temperature. If the junction's temperature is known and under the assumption that the junction is made from the thermocouple wire attached to copper, the magnitude of this noise can be calculated and removed from the recorded thermocouple signal.

To then fulfil the thermocouple conversion role, the MAX31855 (Analog Devices, USA) was chosen. The TASA IC version the specifically tuned to the correct conversion requirements for T-type thermocouples. This IC simplified the thermocouple signal conversion process by combining signal gaining, digitisation, and cold junction compensation into one package. Temperature data is then made accessible via a SPI bus connection to the microcontroller (Figure 4.12A).

This ICs were intentionally placed away from the high-current TEC circuitry to avoid any possible joule heating contaminating the cold junction compensation (Figure 4.12B). Connecting the thermocouples onto the shield required two mounting options to accommodate thermocouple sourced from different manufactures. The connector setup was consistent from Interface Version 1 to 3. However, a design change during the development of Version 4 required an alteration to the thermocouple connection schema.

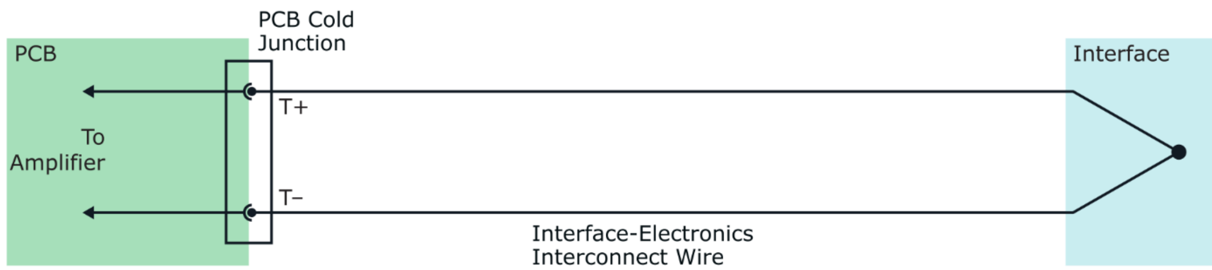


Figure 4.13 Initial thermocouple temperature sensor interconnect setup.
Thermocouples are continuous until reaching the TEC Control shield – indicated by the T+ & T-. Connection is achieved through a Miniature Thermocouple Connector (T-type). This layout occurred in Interface Version 1 to 3 setups.

Interface Version 1 to 3 Connection

Interfaces Versions 1 to 3 use the IT-1E (Physitemp, USA) T-type thermocouple to sense the TEC's hot-side and cold-side. Consisting of a 40AWG twisted wire pair with an exposed tip, the non-welded thermocouple ends are terminated with a T-type miniature connector. A counterpart to this connector enables it to be plugged directly into the TEC Control shield. This connection then contains only one cold junction that needs to be accounted for (Figure 4.13).

Interface Version 4 & 5 Connection

In the move to the Interface Version 4 design, a 12pin Micro 360 connector from Omnetics was introduced into the system. This made the miniature thermocouple connection on the IT-1E thermocouple redundant. This resulted in a shift to using the 5TC-TT-TI-40 T-type thermocouple (OMEGA, USA). The new setup now had two cold junctions – one at the shield and one at the Interface connector (Figure 4.14). Whilst the MAX31855 provides compensation for the shield junction, it won't be able to do the same for the Interface connector. It was then important to quantify the error that this would introduce into the temperature reading to gauge effect.

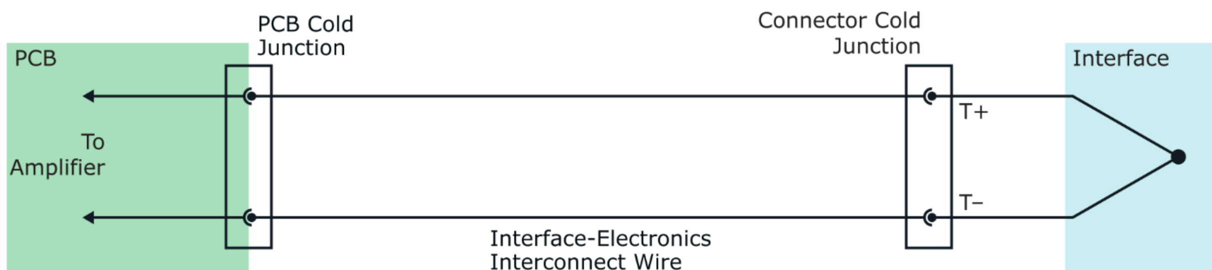


Figure 4.14 Final thermocouple temperature interconnect setup.
Thermocouples are continuous until the Interface connector – indicated by the T+ & T-. Introduction of the Omnetics connector in the Interface has resulted in a second, none compensated cold junction in the thermocouple interconnect wiring. This layout occurred in Interface Version 4 and 5 setups.

To calculate the error that the Interface connector could introduce, the connector setup was approximated into four copper-gold junctions. Copper-Gold junctions have an approximate Seebeck Coefficient of 0.5μV/°C. It can then be estimated that the four junctions would produce a maximum parasitic EMF of 2.0μV/°C per thermocouple. If this maximum parasitic EMF was experienced on a thermocouple during operation, the resultant temperature reading error induced would be approximately ±0.05°C. With the MAX31855 amplifier data output resolution being 0.25°C, this error is large to induce a reading error of ±0.30°C. However, since the PID controller temperature references are on the 1°C scale, it should not pose an operational significate effect on the dynamic cooling control. It is when in the steady-state cooling control, where this temperature error would show as an offset, that this error would become more apparent.

To achieve greater accuracy in the temperature measurements, there are two main options that could be implemented in future systems. One option would be to have the 12-pin Omnetics connector pins used for the thermocouple interconnects modified. Instead of the current gold interconnects, the relevant pins would be replaced with copper and constantan variants. This was considered when the Omnetics connector system was introduced. However, manufacturing and shipping led times during that period (+6 months) to get them produced would have led to large project delays. The other option would be to move to a different temperature sensing system type that doesn't experience this specific behavioural error. This was also considered during the connector introduction but dismissed due to time constrains.

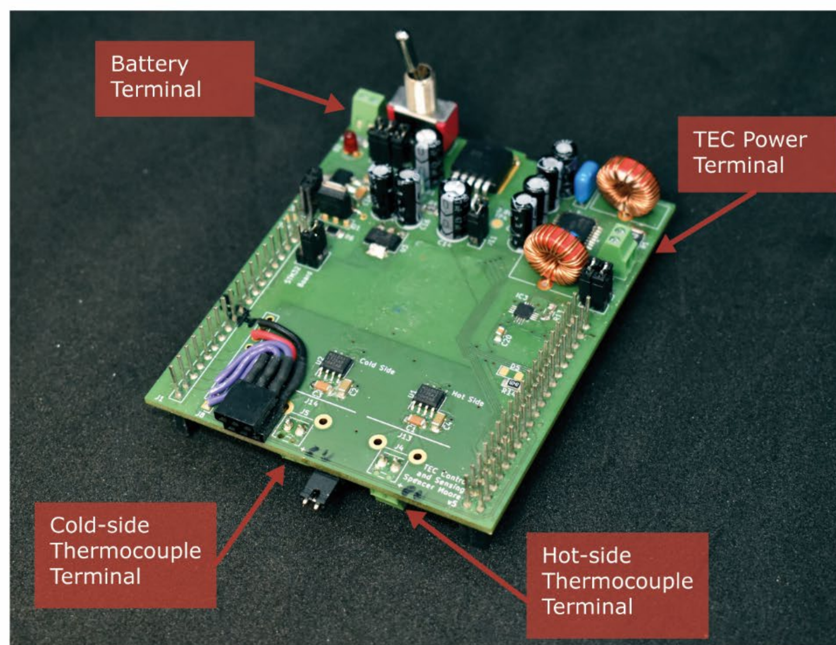


Figure 4.15 Terminal block connectorson the TEC Control shield v5.
These provide connection points of the labelled sub-systems to the Interface and the battery.

4.4.9 Interface-Shield Connection

As alluded to in the previous discussions, there were two versions of the Interface-shield interconnect cable produced for the TEC Control hardware. Since the second version has superseded the first, it will be the only one described going forward.

The connection into the TEC Control shield is achieved through a series of 2-pin terminal blocks. These terminals conform to the 2.54mm pin spacing standard and the have screw operated locking actions for each input. This simplifies connection onto the shield by not using proprietary connector types – especially with component alterations during development. On the TEC Control shield there were three Interface facing block terminals: one at the TEC driver output and two at the thermocouple amplifier inputs (Figure 4.15). A fourth terminal block connection was used to connect a battery or power supply to the shield.

To connect the Interface to the shield, an Interface-shield interconnect cable was produced. On the Interface facing end was the 12-pin Omnetics connector (Section 3.9.4). On the shield facing end, all wires were terminated with pin connectors that allowed easy mounting into the terminal blocks. The interconnect cable consisted of nine discrete wires – TEC power+, TEC power-, electrode 1, electrode 2, electrode 3, electrode 4, GND, thermocouple cold-side, and thermocouple hot-side. The thermocouple wires were 36AWG and have two cores to support the T+ and T– connections. The TEC power wires had a stranded 22AWG core. The electrode and GND all use the Cooner AS155-28AWG wire.

4.4.10 TEC Control Shield Setup

As the TEC Control shield was designed to be mounted atop a development board, it is unable to function without a Nucleo-64 format host board. Figure 4.16 is an instance of the TEC Control v5 shield being used during an *In Vitro* study. The microfluidic pump system, to be described in Section 4.7 , is mount atop the shiels using a custom 3D printed holder. The pumps closed metal casing reduces electrical noise emission to the surrounding systems. This pump is connected to the shield via a 2-pin header located next to its mount point. The battery input is seen with a 3D printed adapter to provide support for the 4mm banana plugs attachment. Having this adapter enables the use of power supplies whose outputs terminate with 4mm banana plugs. This was the case for the bench top power supplies and the sourced battery. Data flow into and out of the system was supported by the Nucleo-64’s Serial-to-USB interface. This required the use of a cable supporting a USB Mini-B to USB A connection.

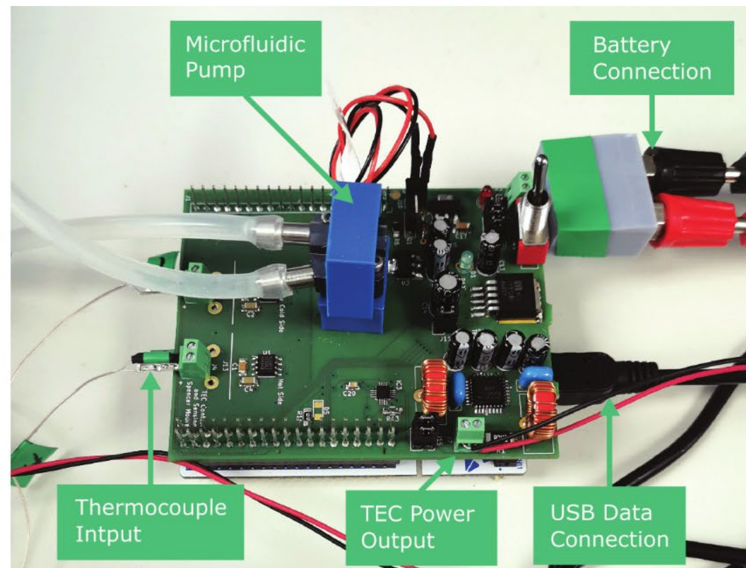


Figure 4.16 Example setup of the TEC Control v5 hardware.
The TEC Control shield is mounted atop an STM32L476 Nucleo-64 development board. Boxed labels identify systems including the custom battery adapter, microfluidic pump and USB connection.

4.5 Neural Signal Acquisition

Integration of the neural recording electrodes onto the Interface Version 4 design instigated the process for the development of the hardware to support its function. The process of neural signal acquisition requires careful consideration due to its μV scale amplitudes. Appropriate hardware must be sourced as to not distort the signal with electrical or environmental noise.

As the electrodes were designed to be used in a bipolar configuration, this innately provides robustness against common-mode noise induced on the electrode signal paths. However, it does add to the electronic potential hardware required to support this electrode layout as, unlike unipolar electrode which require (N+1) signal inputs, bipolar setups require (2N + 1) signal inputs to support the same number of channels. A generic description of the hardware flow for bipolar electrode ingestion is displayed in Figure 4.17.

The first section in this flow is designed to condition the input signal so it is optimised for minimal information loss when digitised. This starts with an instrumentation amplifier (In-amp). An in-amp circuit contains a differential amplifier that has an operational amplifier (Op-amp) buffering each of its inputs. This removes the need to provide a balance load which would be needed for a standalone differential amplifier. Manufacturers provide this circuits in single IC packages that contain laser-trimmed precision resistors to obtain optimal operating specifications. The main two specifications this resistor balancing effects is the Common-Mode Gain and the Common-Mode Rejection Ratio (CMRR). Both impact the common-mode noise retained from the input signals. Ideally the Common-Mode Gain would tend toward zero whilst the CMRR tends towards infinity.

After signal differentiation the signal is then needed to be amplified. Increasing the desired signal amplitudes helps to lessen the effect of process noise added later by another components. It also ‘stretches’ the signal amplitude to better fit the ADCs input range enabling increased signal fidelity. The gaining process can involve a single or double staged approach. Choice on which approach to use depends on how much gain to apply to the signal and on the selected amplifier gain limits. The in-amp stage is also capable amplifying the signal alongside the differentiation so can fulfil both functions.

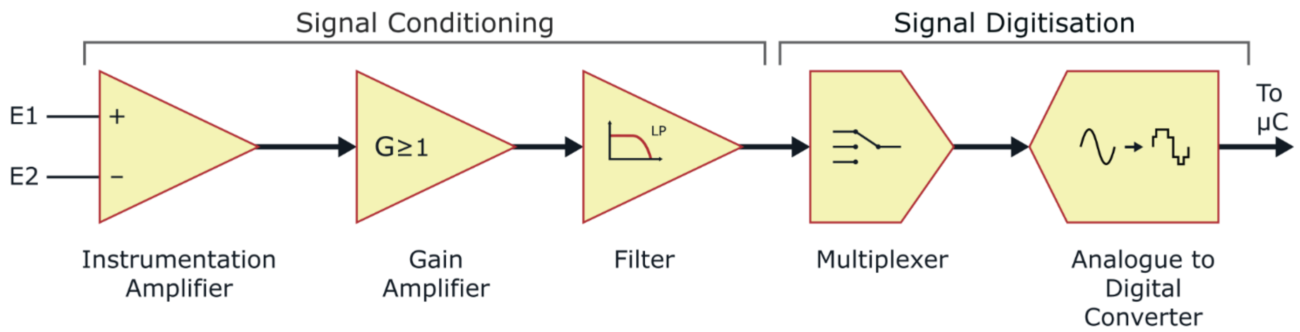


Figure 4.17 Generic hardware flow for bipolar electrode electrophysiological recording.
Instrumentation amplifier produces the differential signal from the two electrode inputs. Next the signal is amplified by gain G to use the fully Analogue to Digital Converter range. A filter is used, commonly low pass to remove frequency components greater than half the sampling frequency. If there are multiple bipolar pairs, a multiplexer is used to select the channel to sample. The signal is transformed into the digital domain by an ADC. ADC bit value and sampling reference voltage determine the signal resolution achieved.

The last signal conditioning stage is the application of a filter. Whilst some signal acquisition systems relegate this to software implementation, having at least a low-pass filter is recommended. In the signal conditioning flow, this low-pass filter has its cut-off frequency set to half the signal sampling rate – otherwise known as the Nyquist frequency. This removes any higher frequency component from being sampled and causing temporal aliasing. A type of aliasing that happens when the frequency components existing above the Nyquist frequency overlap those below it which causes the formation of distortions in the sampled signal.

The last section handles the transformation of the signal to the digital domain via an ADC. An ADC converts an analogue signal, formed by a current or voltage, into a discrete numerical value. This conversion takes place relative to a static reference signal that defines what signal magnitude is represented by the maximum discreate numerical value – thus the conversion range. Any input signal with magnitudes beyond this reference value saturate the ADC numerical output and the data is lost. ADC resolution is dictated by the 2s compliment bit value the ADC is specified to output. For example, a 16-bit ADC can output 2^{16} discrete values from 0→65,535. Calculating the ADC resolution is then the reference signal magnitude divided by the maximum bit value – this is also referred to as the Least Significate Bit (LSB) value.

If there is the intention to handle multiple electrode pair inputs, then a multiplexer (MUX) can be employed to control the input cycling. Using a MUX is normally preferred over the use of multiple ADCs due to component cost and the additional circuit complexity it entails. Whereas a MUX is more than capable of switching at a frequency required for neural signal acquisition.

4.5.1 Intan ANSIC IC

In order to have a compact system and achieve smooth neural sensing integration, it was decided that the ECoG signal acquisition would be handled by a commercially available IC as opposed to an in-house developed solution. This discrete system was the Intan RHD2216 Electrophysiology Interface Chip. The Intan IC combines all of the previously described signal acquisition hardware into a single ASIC package.

The RHD2216 is the bipolar electrode input variant of the chipset family. It is capable of sampling up to 16-channels and supporting a maximum 1.05MSamples per second sample rate on its 16-bit ADC. Whilst this was more than required for the current 2 electrode pairs on the Interface, it would allow for future Interface recording expansion without needing extensive system redesign. The LSB voltage step size of the ADC is 0.195μV where the typical amplifier input noise on a sampled channel is $2.4\mu V_{rms}$.

Communication with the chip is granted via the integrated Serial Peripheral Interface (SPI) controller. The Intan IC offers the ability to customise its function via on-board registers to suit the use case. These registers provide user control of the on-chip programmable input bandpass filter. Both the upper and lower cut off frequency can be tuned to meet the desired Nyquist frequency requirements.

4.5.2 Nucleo-64 Breakout Board

Addition of the Intan chip directly onto the TEC Control shield was not undertaken to ease Intan firmware development. Instead, a separate shield board was designed (Figure 4.18A-B). This shield’s main objects were to grant access to all of the Intan electrode channel inputs, connect the SPI pins through to the Nucleo-64 board, and conform to the Nucleo-64 development board header scheme. Conforming to the Nucleo-64 header scheme not only simplified the connection to the microcontroller but also allows the shield to be stacked atop the TEC Control shield. This ability results in the two Interface modalities these shields support being able to be used in tandem during experimentation. Hardware setup then established the foundation for the Interface’s closed-loop seizure detection and control.

The manufacture shield was able to be mounted on the Nucleo-64 development board for firmware development (Figure 4.18C). Electrode inputs In0 to In7 were routed to terminal blocks at the shield's edge and were the main input channels. In8 through to In15 were routed to a header block to allow if they had been required for other studies. Like the TEC Control v5 shield, the Intan Breakout shield consisted of four copper layers in the top-down order – Signal; GND; Power; Signal. The ground layer is linked to the analogue ground of the TEC Control shield and that of the Nucleo-64 development board. Power supply for the Intan IC can either be drawn from the TEC Control shield's 3.3V system regulator or from the Nucleo-64 board to allow for adaptable hardware configuration during integration testing. Having the Intan shield conform to the layer system as the TEC Control v5 shield allowed for PCB panelisation so as to allow for manufacture of both PCBs as a single unit to be separated post-manufacture.

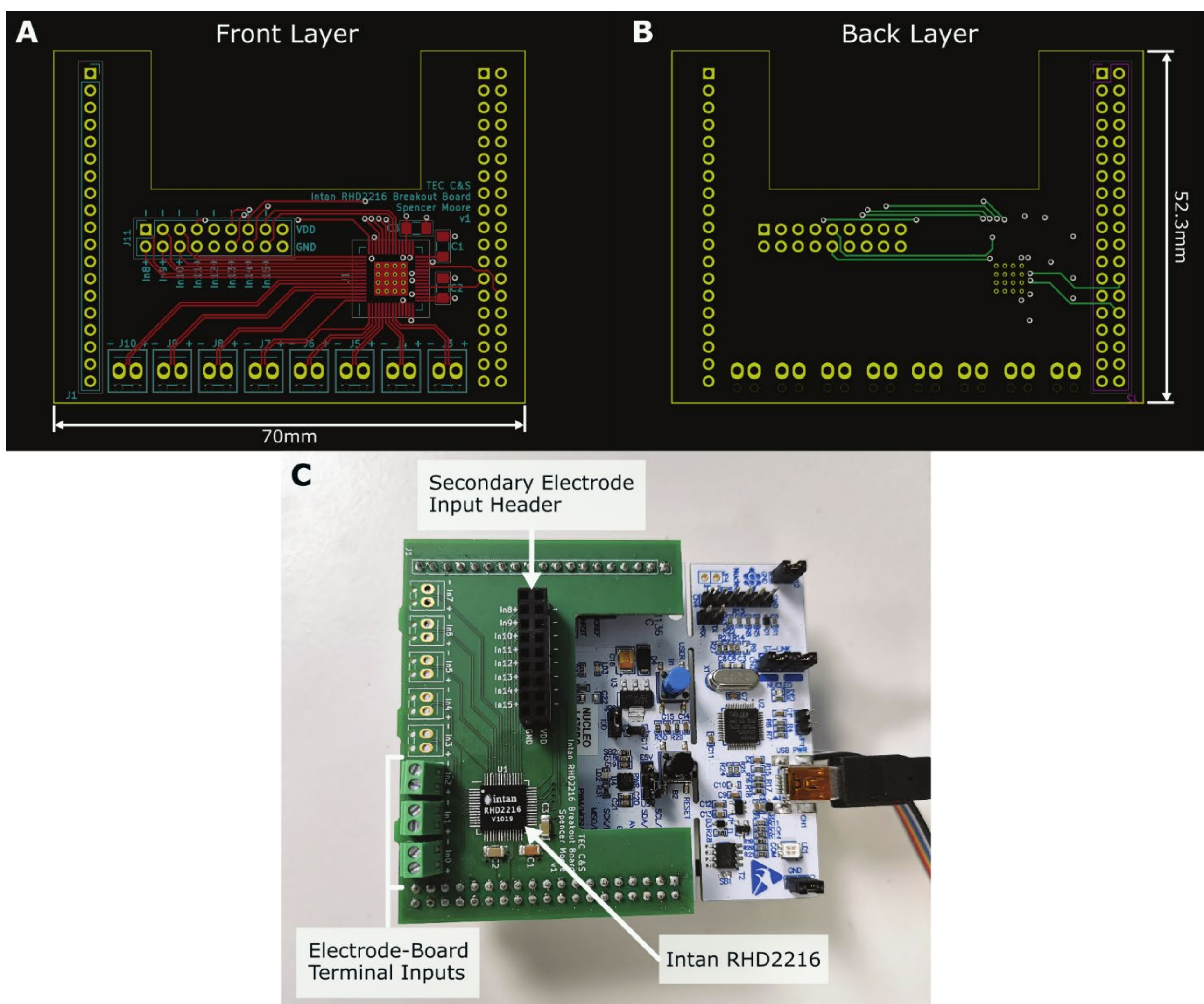


Figure 4.18 Breakout shield for the Intan RHD2216 electrophysiology chip.
PCB schematics of the top (**A.**) and bottom (**B.**) signal layers of the Intan Breakout shield. The RHD2216 uses an 8mm x 8mm QFN footprint for mounting. Board size is 70mm x 52.3mm. A cut-out in the shield, making it form a U shape, is there accommodate the microfluidic pump mount on the TEC Control v5 shield **B.** A fabricated Intan Breakout shield mounted on the Nucleo-64 board. Electrode input terminal blocks and header pins are soldered to provide quick access to the RHD2216 pins.

4.6 TEC Control Shield *In Vivo* Stack Setup

Having electronic hardware to support the focal cooling and neural recording modalities now meant that *In Vivo* studies could now be undertaken. Alongside the Interface Version 4, the first opportunities to develop the *In Vivo* experimental setup and protocol were undertaken. The full shield stack setup was used during these experiments (Figure 4.19A). Each custom designed shield conforms exactly to the Nucleo-64 header format. Feed-through headers were installed on the TEC Control v5 shield provided a mountable location for the Intan Breakout shield and to presenting the Intan shield access to its required information and power buses.

For the *In Vivo* setups, the studies were to occur within a faraday cage to prevent environmental noise from influencing the neural recording systems used. Faraday cage construction, in this case, resulted in all internal cage surfaces being metallic. To then prevent the bridging between the exposed GPIO pins on the Nucleo-64 development board, a case to house the system stack was 3D printed from PLA (Figure 4.19B). This case also contains an attached section to mount the microfluidic reservoirs into and provided a stable platform for the microfluidic system to function from without risk of coolant spills.

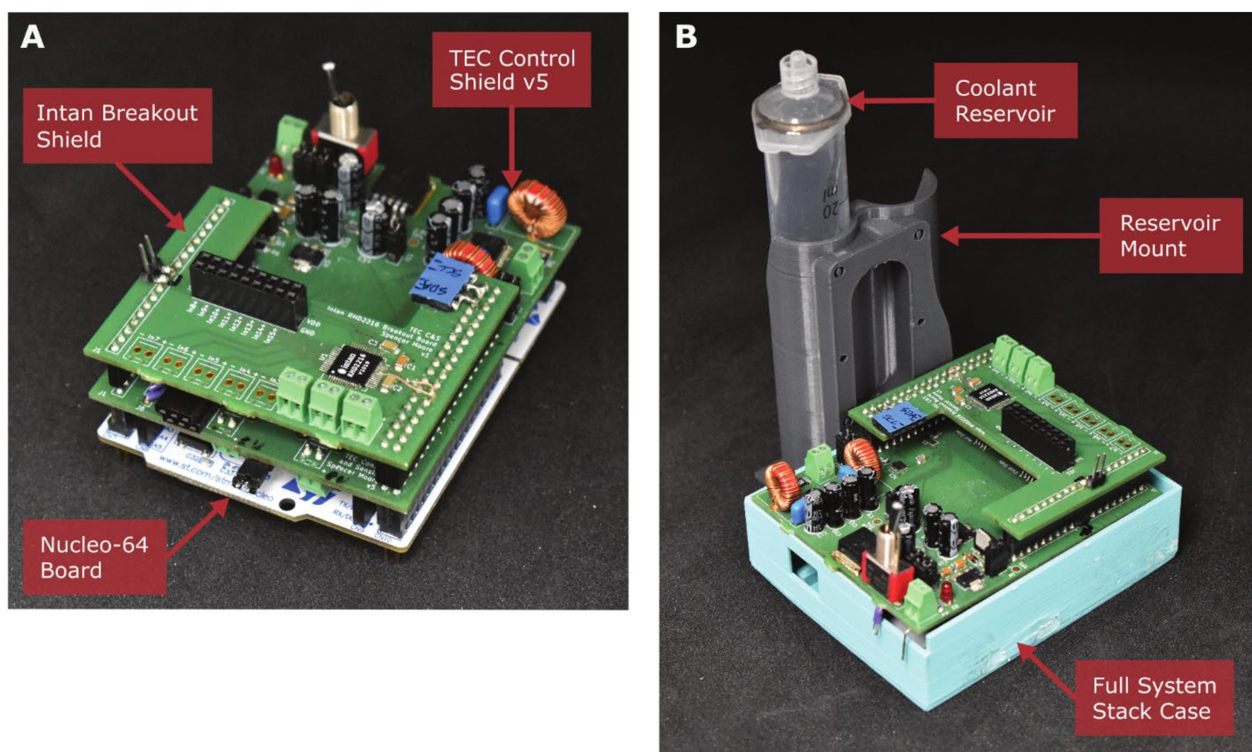


Figure 4.19 Stacked TEC Control hardware to support Interface function
This stack consisted of the TEC Control v5 shield, Intan Breakout shield, and the Nucleo-64 Development board. **A.** View of the stack boards where all three component boards are defined. **B.** The system stack mounted in its case to prevent the Nucleo-64 header pins from exposure the metal surfaces found in the *In Vivo* workspace. Attached to the side is the Coolant Reservoir mount and an example Coolant Reservoir.

4.6.1 TEC Control Stack Limitations

As progress was made in the gaining *In Vivo* setup experience, it became apparent that the current TEC Control hardware design was trending towards becoming an issue. Design issue occurred from three areas – function expansion, Interface-shield connection, and signal noise.

As the Interface-shield connections requirements had become standardised by Interface Version 4, there was now no need to facilitate the generic terminal blocks. These had served their intended adaptable-use purpose during development. But this was at the cost of having connections that only allow orientation specific mating. Having a single way to orientate the hardware connection reduces the risk of hardware damage and miss-setup. Ideally this would have to be introduced as a single connection onto the hardware. However, the distributed layout of the hardware would prevent this from being implemented in the current design scheme.

On the other hand, whilst the Interface-shield connections were now standardised, the number modalities on the Interface had not. Expanding hardware functionality to accommodate this in the current setup would result in additional shields. Further shield stacking would add to the already complicated hardware setup. Further increasing signal flow through more connectors and longer signal paths create ideal conditions for increased noise entry. Using the Nucleo-64 board had now started to be in contention with the requirement to for compact design. Progressing away from this form factor would allow for greater layout optimisation opportunities.

During neural signal recordings, it was noted that periodic noise was present in the within these signals. Cause of this noise was traced to the shield stack grounding organisation and to the thermocouple amplifiers function in particular. The current ground layout provides routes in for the built-in thermocouple amplifier diagnostic pulses to be introduced as noise in the neural recordings. This diagnostic feature pulses a voltage signal through the attached thermocouple to check for open-loop or closed-loop conditions. The feature performs the action every time a temperature sample is taken or at ~14Hz sample rate – the exact frequency the neural signal noise presents. This feature is automatic and the amplifier does not present an ability to disable it. As finding a replacement amplifier IC was difficult under the current industry supply state, the only solution would fix the ground design to prevent its influence.

The conclusion that was reached from the three issues was that a system layout redesign had to be performed. This redesign would combine the current hardware – the TEC Control v5 shield, the Intan Breakout shield, and the Nucleo-64 Development board – onto a monolithic PCB. In doing so, the format restrictions imposed by the Nucleo-64 board are removed. Sub-system circuits could be rearranged for signal routing optimisation and new sub-systems to support known future Interface modalities could be introduced. Ground layout would be simplified through it being turned into a single grounding plane. Designated the Interface Support hardware – work undertaken to design this board is discussed in Section 4.8.

4.7 Microfluidic Coolant System

Coolant flow over the TEC hot-side is required to support the heat pumping mechanism that a TEC uses to induce cooling and reach the intended temperature differential. System design for the flow actuator has to follow the hardware requirement for low power and miniaturised systems. A pump, a coolant reservoir, and a flow sensor are the base components needed to construct the system and enable to function in the required way.

During the Interface and electronic support hardware development, two microfluidic systems were designed to support the coolant flow over the TEC's Heat Sink. The first was based around a centrifugal pump. Whilst this pump proved functional for short length *In Vitro* studies, issues related to inconsistent flow over longer Interface studies led to its replacement with a system based around a piezoelectric air pump. This section will provide a discussion of these two systems and the reasoning for the adoption of the piezoelectric air pump.

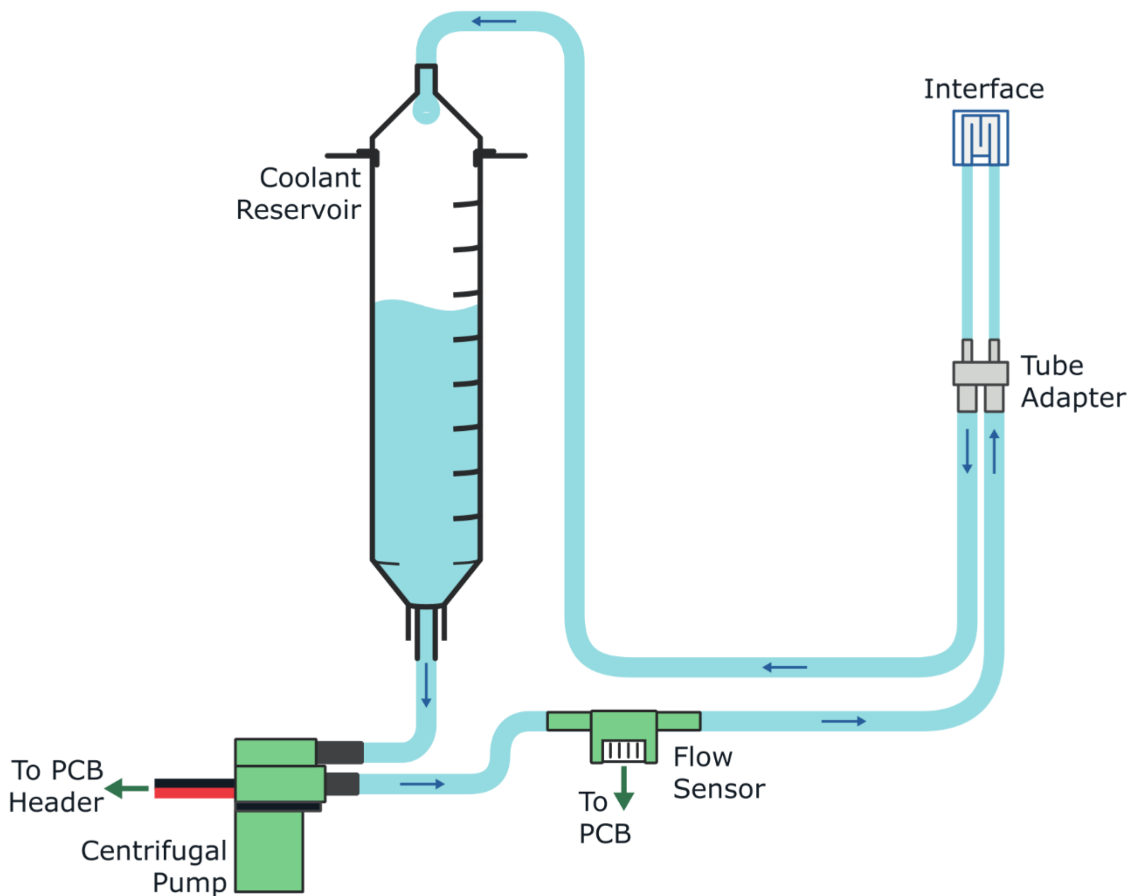


Figure 4.20 Layout of the centrifugal pump-driven microfluidic system.
The centrifugal pump rate is controlled via an on/off signal from the microcontroller. It is activated only during a cooling event. Coolant fluid will be stored within a reservoir that directly feeds into the pump. A flow sensor enables the monitoring of flow characteristic through an Interface giving feedback on system status and efficacy. Blue pathing represents coolant flow and green items represent the system electronics. Arrows indicate flow direction in the system.

4.7.1 Centrifugal Pump System

One of the simplest ways to drive fluid flow is use of a centrifugal pump. This pump type houses an impeller within a sealed case to directly drive a pressure differential in the fluid coolant. The developed pressure difference between the pumps inlet and outlet causes the fluid to flow. A micro-centrifugal pump (480-122, RS Components, UK) was sourced that could be driven by a 0V to 4V input voltage and is specified to be able to a produce fluid flow up to 450ml/min.

Setup of the centrifugal pump-based microfluidic system involves all basic hardware elements (Figure 4.20). It creates a closed-loop, unidirectional coolant flow path that requires no replenishment of coolant during operation. A mixture of off-the-shelf and custom components were used in building this.

To ease of prototyping, coolant reservoirs were manufactured using 20ml syringes with leur lock ends. Using them as reservoirs required two syringes for their construction. With one syringe the plunger is completely removed from the syringe body. Using another syringer, the leur lock end is cut off where the 1ml mark is located. This cut end is then mounted onto the open end of the first syringes body using an epoxy adhesive. The leur lock allows for 3mm ID silicone tubing to be directly attached without further modification. The majority of the systems tubing is 3mm ID except for the Interface silicone tubing that is 0.4mm ID. Connecting the two tubing sizes together was managed using a custom designed tubing adapter that was 3D printed with a resin 3D printer (Sonic Mini 4k, Phozen, Taiwan).

A SLF3S-1300B (Sensirion, Switzerland) flow sensor is placed in-line with the microfluidic pump's outlet. This flow sensor is capable of sensing coolant flow rate, coolant temperature, and trapped air occurrence. A 5pin Picoblade connector (Molex, USA) is used to link the electronic hardware to the sensor. Sensor communication is achieved via I^2C.

Pump Control & Electronics

Electronic control of the coolant flow was implemented using a transistor switch type circuit. The microcontroller GPIO pins are unable to source the ≤600mA current required to operate the pump. Having the transistor switch in-line with the pump's power supply provides the means for the GPIO pin to control the pump independently from its power source. This setup provides the potential for a binary on/off or PWM-based control signal. During system testing, it was determined that the pump would be required to be ran at its maximum flow output to provide the required coolant flow for Interface cooling. Thus, a simple on/off control signal was used.

Power for the pump it supplied by a LDO regulator (NCP1117, Onsemi) those output is regulated to the pump's V_{max} of 3.88V. This circuit is implemented on the TEC Control v5 shield (Figure 4.21A). Connection of the pump to the shield is through a 2pin, 2.54mm pitch female header. The pump's positive and negative wires are terminated to the male header pins of the same specification. A schematic of the described centrifugal pump power regulator is displayed in Figure 4.21B and control circuitry for the centrifugal pump is arranged in Figure 4.21C.

Centrifugal Coolant Flow Issues

Throughout studies undertaken which used the microfluidic system, cases of thermal instability were experienced during cases of heavy repeated cooling runs. Even after the move to the stainless-steel Heat Sink, instability whilst the running the microfluidic system over long periods still persisted. These instabilities did not present the same behaviour as what caused the Heat Sink related issues. Rather, they were intermittent instabilities that would regularly manifest during sets of cooling runs at unpredictable points and would cause a previously stable thermal system to suddenly enter thermal instability. The root of this issue was discovered to be caused by flow inefficiencies from the centrifugal pump.

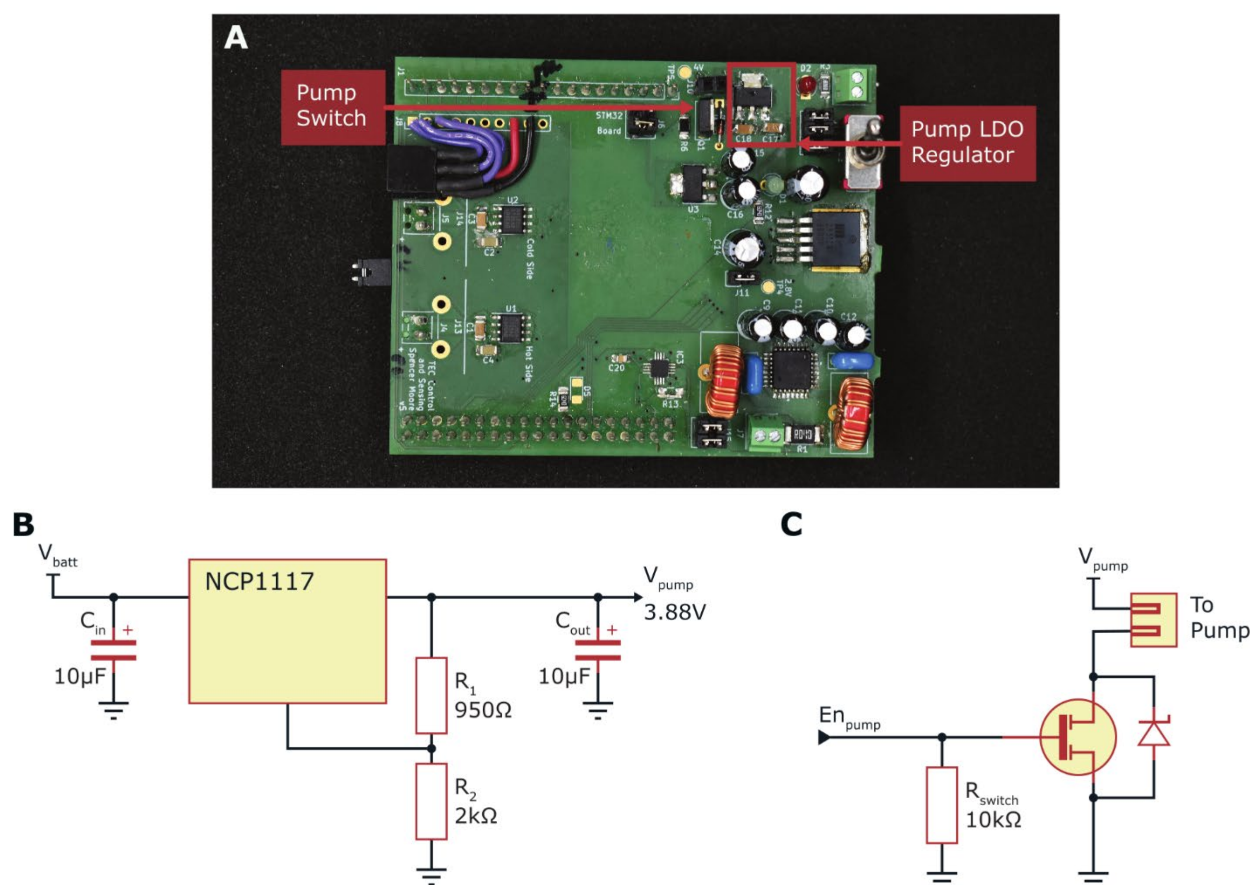


Figure 4.21 Description of the centrifugal pump electronics.
A. Location of the centrifugal pump circuitry on the TEC Control v5 shield **B.** Centrifugal pump power regulation circuit formed using the NCP1117 LDO set to regulated output of 3.88V. **C.** Centrifugal pump control circuit consists of just an N-Type MOSFET. It enables functional control of the pump via a microcontroller GPIO pin.

First, it was realised that when the centrifugal pump ran during multiple consecutive cooling runs, trapped air would build up in the centrifugal pump's impeller housing. To function correctly, a centrifugal pumps impeller element is required to be fully submerged in the fluid at all times. Air within the housing would continue to build up which would lead to a gradual reduction in pumping efficacy. It became the case that after every three 60s cooling runs the microfluidic system would have to be manually purged of air to support the next set of cooling runs. Experiencing this initiated further investigation into long term pump action and microfluidic function.

Results of the further investigation revealed flow rate noise that the centrifugal pump imparted into the fluid flow. Flow recordings detail erratic flow noise during pump activation and over, what should be, steady-state fluid flow (Figure 4.22A). This noise within the flow would induce mechanical noise in the Interface. These induced micro-vibrations are likely to be recorded in the electrode signals through cause material strain, and could result in accelerated neural tissue fibrosis at the implant site. Once the flow noise was cleaned up using a 20-sample traveling average window, the average pump flow rate was determined as ~2.1ml/min. This is substantially below the manufacturers specified flow rate.

A study was performed to test if the orientation of the centrifugal pump's inlet and outlet would produce any improvement in steady-state flow rate of the system. Previously, the pump had been mounted upright with the inlet/outlet at the top and they protruded from the pump body parallel to the ground. After recording pump flow rates with the pump in multiple orientations, it was found that the pump placed on its longest side with the inlet/outlet protruding from the body directly up relative to the ground produced the greatest improvement to flow rate. This centrifugal pump orientation led to a doubling of flow rate to 5.4ml/min (Figure 4.22B).

During this orientation study, another issue was discovered with heat produced by the centrifugal pump during operation. Coolant temperature profiles indicated that heat produced by the centrifugal pump was being transferred into the coolant. This would produce a notable rise in coolant temperature over the course of its operation. This temperature increase was then exacerbated by a large heat dump occurring when the pump is deactivated (at approximately 125s). This produces an ~1°C increase in temperature from coolant nominal. As the pump is located before the Interface in the system, heat added by the pump would be directly affecting heat removal efficacy by the coolant due to decreased temperature differential to the Heat Sink. Any solution to this issue were not able to be implement with the current hardware and system requirements (i.e. reducing pump power). Most would have resulted in a reduction in cooling efficiency of the TEC hot-side. Overall, the combination of these uncovered issues led to the decision to find a replacement for the centrifugal pump.

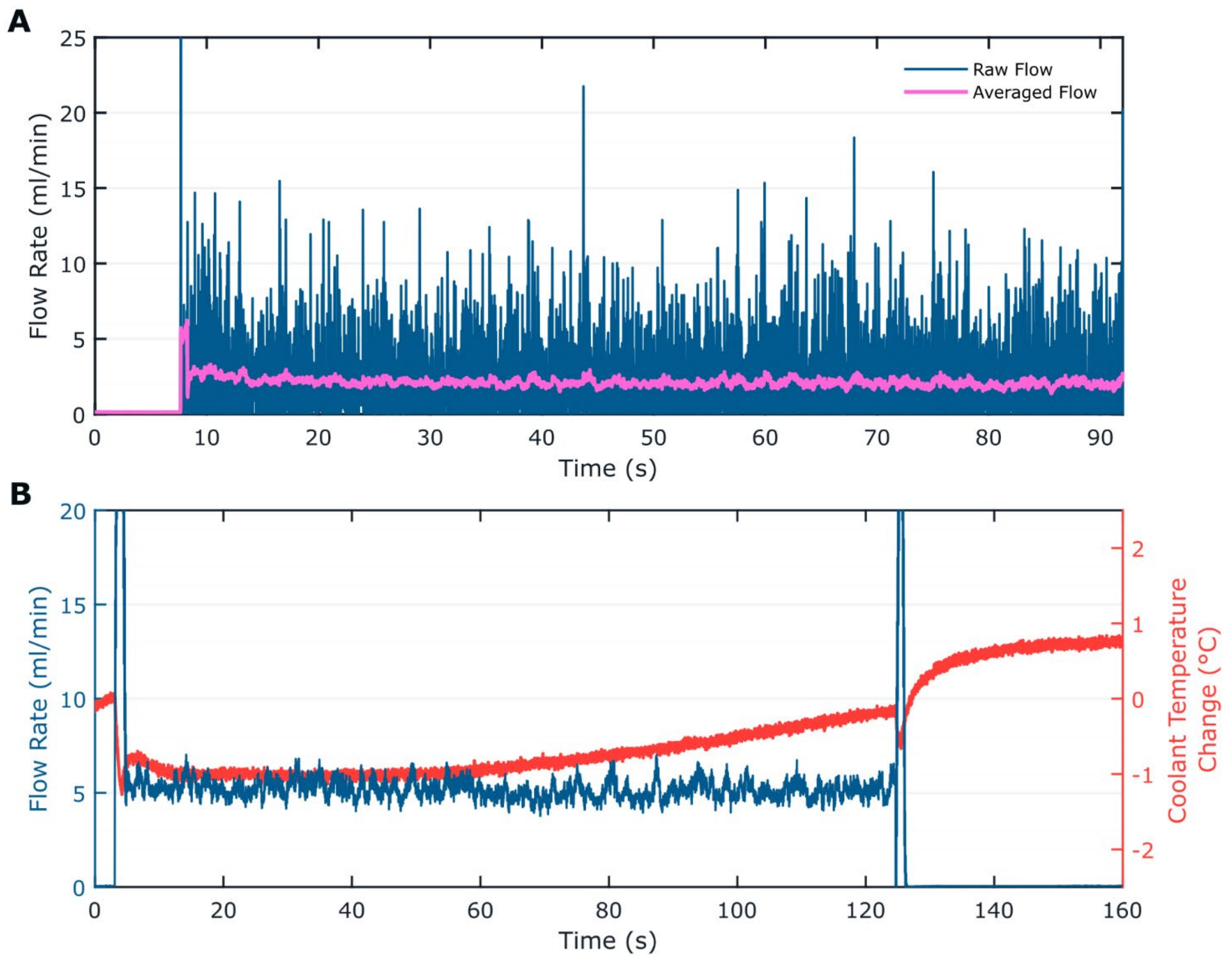


Figure 4.22 Centrifugal pump flow and coolant temperature data.
A. A 60s recording of the raw flow data driven by the pump. A 20-sample moving average was used to calculate the predicated average flow value (~2.1ml/min). **B.** Recording flow of an improved centrifugal pump setup that provides and averaged flow rate of the on period of 5.4ml/min. The coolant temperature profile is displayed in red indicating a +1°C coolant temperature increases after pump shutdown.

4.7.2 Piezoelectric Air Pump System

To prevent the centrifugal pump issues arising occurring again, a pump that is isolated from the main coolant flow was chosen as the flow actuator. This would be in the form of a piezoelectric air pump. A piezoelectric pump takes advantage of the piezoelectric effect to move air. A train of large potential pulses are applied to a thin sheet of piezoelectric material at a high frequency. This causes the piezoelectric sheet to continually flex back and forth. By encasing this movement within a sealed chamber with directional flow valves, local pressure differentials can be formed to draw air in through one valve and push air out through the other. This system works as a diaphragm-type pump were the repeated push-pull actions sustain a continual flow of air.

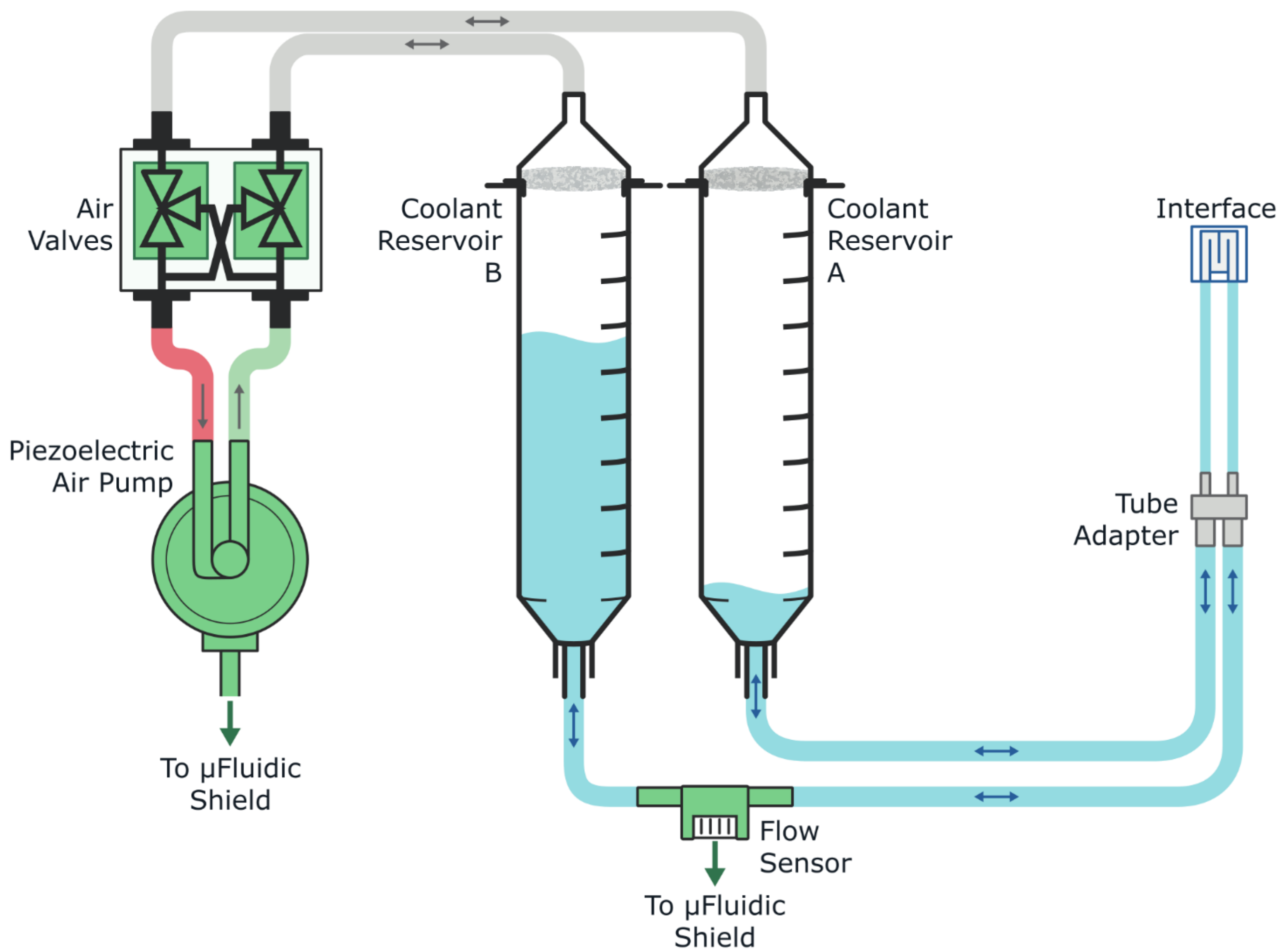


Figure 4.23 Layout of the piezoelectric air pump microfluidic system.
The piezoelectric air pump actuation provides both a positive pressure output and a negative pressure output. Application of these differing pressures into two reservoirs causes coolant flow. Flow direction is dictated by a pair of air valves. By switching valve positions, the coolant flow can be directed into a 'see-saw' motion between the reservoirs. Switching flow direction as one reservoir gets near empty provides a pseudo-circulatory behaviour. Blue represents the coolant fluid and green elements represent the systems electronic components. Arrows indicate potential flow direction.

Flow actuation with piezoelectric pumps produce a low noise system in both the sound during operation, and the variance in the flow output. The actuating piezoelectric material in these pumps are often left exposed to the worked medium being driven (i.e. air, water, etc). This setup prevents losses in pumping efficiency; however, it also means that the usable working medium has to be restricted as not damage the pump's piezoelectric material. In this case the pumping medium is restricted to air. Due to this, an indirect, air pressure driven fluid flow will have to be utilised to provide coolant flow.

The new microfluidic system was based around the UXPB5401200A (The Lee Company, USA) piezoelectric air pump. It was provided mounted on their Smart Pump Module System (SPM-041). These small, lightweight pumps will allow for a high level of integration into the electronic systems whilst the SPM-041 module provides the pump driving signals and control interfacing via I2C or UART allowing for drop in functionality with the current hardware (Figure 4.24).

Air Valves

Flow from the piezoelectric air pump is unidirectional in the model acquired. The pump's internal valves are orientated to have a fixed flow direction. System fluid would then have to flow in a non-circulatory manner. This would have resulted in the need to have either one large coolant reservoir that is filled at the start of a study, or having multiple smaller reservoirs that are continuously reloaded between runs. To circumnavigate both of these two options, two air valves were introduced into the microfluidic system enable control air flow direction into two reservoirs.

These valves would have to be able to receive the two air flow outputs from the piezoelectric pump and independently direct them to one of two coolant reservoirs. Switching the direction of air flow into the reservoirs would cause a 'see-saw' type flow motion through the microfluidic system. Two 3-way valves will be used in tandem to fulfil input/output demands through their controllable valve states (Figure 4.24A). They connection of the reservoirs to either the positive pump air flow or the negative pump air flow but never both.

The two-valve setup provides 4 potential system states (Figure 4.24B). Two of the valve system states allow for coolant flow by applying the positive or negative pump air pressure to the reservoirs. Which pressure is applied to which reservoir dictates the fluid flow direction. The other two valve system states grant the ability to equalise the pressure within the reservoirs to halt immediately halt flow in the system. Care must be taken to prevent pump activation during these pressure equalisation valve system states. In these states, either the piezoelectric air pump's inlet or it's outlet would effectively be sealed. Pump activation would cause stress on the pumping elements as it encounters high levels of resistance which would reduce the lifetime of the pumping element without providing any useful work to the microfluidic system.

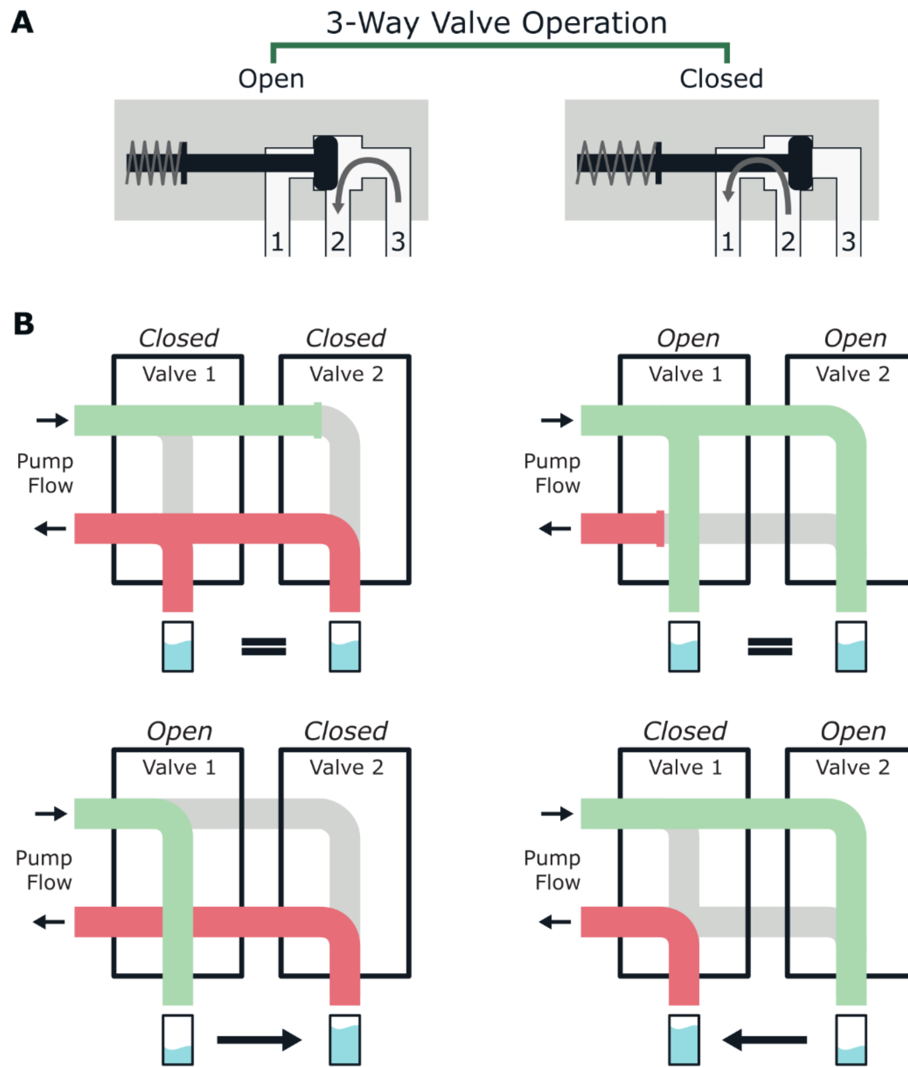


Figure 4.24 Microfluidic system air valve actuation and control states.
A. Two valve states can be set by applying either a positive or negative potential over the valve input terminals. Channel 1 is connected to the pump's negative air flow. Channel 3 is connected to the pump's positive pump air flow. Channel 2 is connected to one of the reservoirs. This enables full control over air flow direction from the pump. **B.** The dual valve system air routing state options. The Open/Closed and Closed/Open states produce active coolant flow through the microfluidic system. Open/Open and Closed/Closed states allow for reservoir pressure equalisation and are the default state in idle operation conditions.

The Series 188 3-way Solenoid Valve (18801105, Emerson) was selected to enable this setup. These valves offer a compact size, with 27mm x 18.7mm x 10mm dimensions, and are low power - the series variant selected are rated at 1W. Latched solenoid valve actions are built into these valves that provides mechanical valve state memory during operation. Setting the valve state then only requires a single control pulse of ~10ms to perform valve state switching before power is removed in the idle condition. Control of the valve switching was performed by reversing the applied voltage polarity across the valve's input terminals.

As the valves are specified to need a 12v control pulse for switching, they are unable to be directly GPIO pin driven. A h-bridge was required to enable valve actuation by acting as a control interface between the microcontroller and the valve. On the h-bridge IC, a set of logic inputs are exposed to connect the GPIO pins to. A boost converter had to be implemented to increase the shield supply voltage to the level required for the valves.

Modified Coolant Reservoirs

Two reservoirs were required for the piezoelectric air pump driven system to allow the 'see-saw' type flow. As with the previous system reservoir, modified 20ml syringes were used. A new resin 3D printed reservoir cap was design to replace the previous cut syringe end cap (Figure 4.25A). To provide protection to the piezoelectric pump, the new cap design allows for an air filter to be inserted before it is bonded on to the syringe (Figure 4.25B). This disk is composed of a porous PTFE (PF100, ADVANTEC) that allows air to freely move through but provides resistance to liquid flow due to its 100μm average pore size. This will prevent liquid ingest towards the pump and block any debris from entering either the valves or pump.

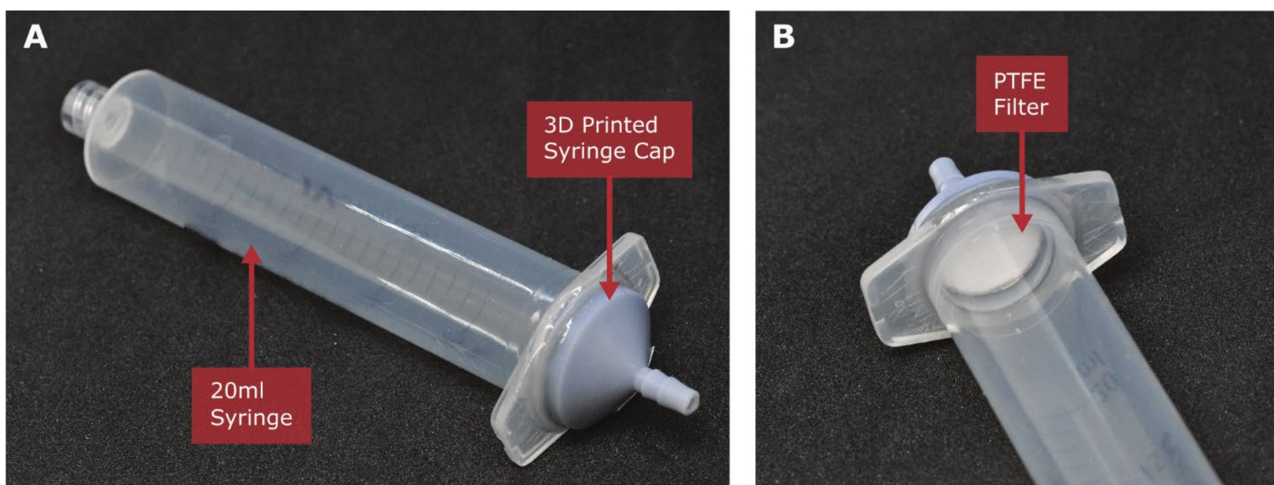


Figure 4.25 Reservoir modifications for the air-driven microfluidic system.
A. The 3D printed syringe cap adhered to the open end of a 20ml syringe. **B.** A porous PTFE filter disc, cut to the diameter of the syringe inner bore, is glued into the ledge mount within the 3D printed syringe cap to protect the valves and pump from unwanted liquid ingress or debris.

μFluidic Shield

Integration of the SPM-041 module and the valves together with the electronics to support the systems function required custom microfluidic shield to be fabricated – named the μFluidic shield. It was a four-layer PCB that conforms to the layering order found on the TEC Control v5 shield (as with the Intan breakout shield). The shield hosts an independent set of power supplies and electronic hardware that is host board agnostic (Figure 4.26A). A 10pin Picoblade connector (Molex, USA) is the shields interface to external hardware. This connector includes the shield board power input (7.2V-8.4V), feed-through to the SPM-041 I^{2}C bus, and logic inputs for the valve h-bridge.

The Piezoelectric SPM-041 module and valve block are provided with mounting points that let the separate hardware be combined into one hardware block (Figure 4.26B). Having it all mounted on a shield provided ease of handling when designing the setup of studies and experiments. A separate array of drilled holes in the μFluidic shield enable the shield to be mounted onto structures or other boards. For experimental use with the TEC Control v5 shield, the μFluidic shield was mounted on to the back of the 3D printed reservoir structure.

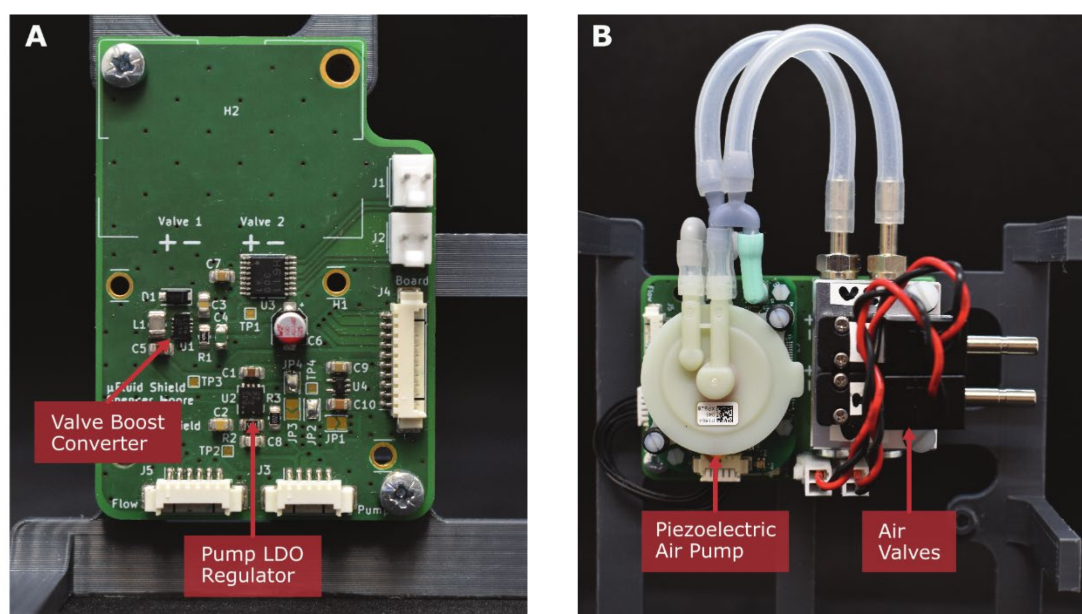


Figure 4.26 Images of the fabricated μFluidic Shield.
A. Front panel of the Shield where the soldered electronics for Microfluidic systems regulation and control are exposed. Picoblade Molex connectors provide access to off board systems. Working around anti-clockwise, these connector link to the Flow Meter, the Piezoelectric Pump module, and the controlling hardware. **B.** The full constructed Shield board with the Piezoelectric pump on the left and the air valves on the right. 3mmID silicone tubing connects the systems together to enable air flow control.

µFluidic Shield Performance

Performance of the revised microfluidic system using the µFluidic shield was tested on the bench top using an Interface v4 in the loop. The SPM-041 module enables accessible pump driving power control through the I^2C bus. Using this functionality, a pump power step test was conducted. The pump power level was incremented by 10% every 10s. The pump's initial state was 0% power and the power was incremented until it reached 100% pump driving power. The piezoelectric air pump was able to drive an average coolant flow rate of ~71ml/min whilst at the maximum pump driving power level (Figure 4.27A). This represents a 34x increase in flow rate capability over the centrifugal pump setup. Even at a 10% pump driving power level, the µFluidic shield was able to maintain an ~11ml/min average coolant flow rate – this being a 5x increase in performance over the centrifugal pump system.

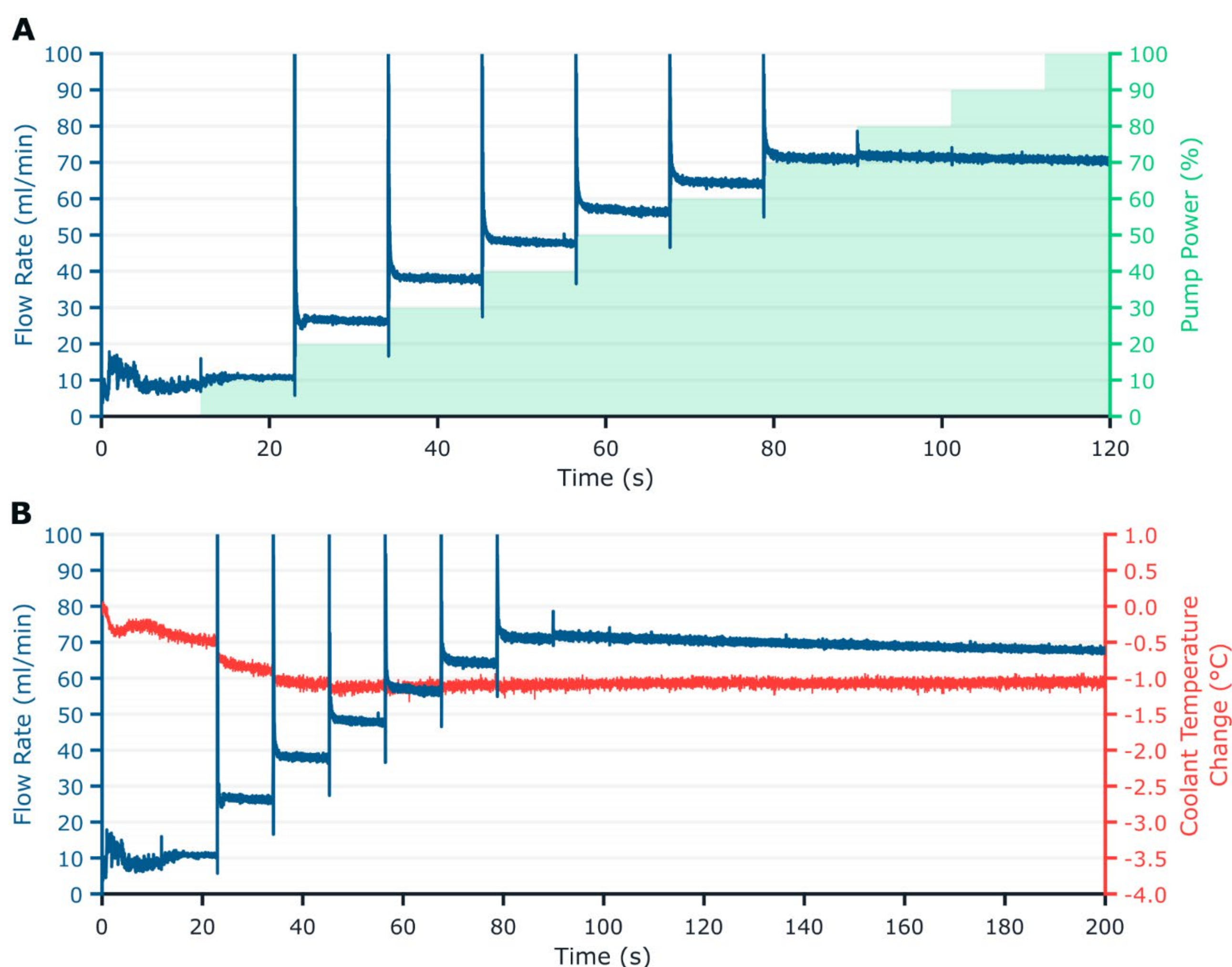


Figure 4.27 Coolant flow performance of the piezoelectric air pump.
A. Coolant flow rate increases as the pump driving power is incremented by 10% over a 100s period. Flow rate increases approximately in equal steps until the driving power reaches 70% and then plateaus.
B. Coolant temperature during the incremented pump power testing provides no indication of heat injection via the microfluidic system's driving elements.

Coolant temperature was also monitored during this step experiment to verify to no additional heat was being 'dumped' into the coolant fluid by the microfluidic system's driving elements (Figure 4.27B). Coolant fluid temperature was monitored over a 200s period during which the piezoelectric air pump step testing took place and a 100% pump driving power was maintained once it was reached. The microfluidic systems coolant fluid was de-ionised water and was held at room temperature over during the study. It was observed that recorded fluid temperature remained below a 0°C ΔT during the step testing and maintained a -1°C average ΔT whilst the pump was in the 100% pump driving power state. This steady state ΔT does not waver during pump function as was seen with the centrifugal pump setup. No heat from the microfluidic system driving elements was imparting heat into the coolant fluid during flow actuation. Thus, the system alterations have solved the heating issue that occurred in the centrifugal pump system.

The µFluidic shield was able to outperform the centrifugal pump setup whilst solving the both the pump related coolant heating and coolant noise issues present in the system. It was also able to perform this whilst consuming less power than its centrifugal pump counterpart. The centrifugal pump required 2.6W to provide its maximum coolant flow rate. On the other hand, at 10% pump driving power the piezoelectric air pump was able to best the centrifugal pump's performance whilst just using 0.1-0.14W. At steady state driving power of 100%, only 1W was required for the piezoelectric air pump to produce the ~71ml/min maximum flow rate. Maximum power consumption by microfluidic systems had been reduced by 88% from the previous system.

4.8 Interface Support Hardware

As described in the limitations of the TEC Control hardware system design, a new monolithic PCB was to be fabricated. The aim of it was to merge all shield architectures together, reducing noise occurrence in recorded signals, and implementing new hardware to support greater Interface modality function. The Interface Support hardware was the result of the work undertaken towards those aims (Figure 4.28A-B). The PCB was a 4-layer design that measured 160mm x 72.7mm. The PCB layer order from the top is: Signal; GND; Power; Signal. Component hardware was distributed across the front and back of the fabricated board (Figure 4.28C-D).

The Interface Support hardware introduced a range of layout and component updates to improve noise rejection and adapt the systems to operate more consistent during *In Vivo* studies. It's hardware systems are capable of providing support for the focal cooling modality, the neural signal recording modality, and the local drug delivery modality (Figure 4.29). Central system control is enabled by the on-board microcontroller. In designing this layout, consideration was taken to the interaction of each systems return current path to reduce ground plane noise influencing the analogue electronic function.

Instead of a split ground plane designed, that was implemented on the TEC Control v5 shield stack, a monolithic ground plane was select for implementation on the Interface Support PCB ground layer. A single continuous ground plane is one which does not exhibit any sectioning or isolation of ground planes areas. Having a solid ground plane reduces current loop instances from being formed through current path bottle necks. These bottle necks can form on split ground planes due to the single point of connect between all isolated plane sections. Ideally, all signal routes that flow from one ground plane section to another need to be routed through this single ground plane connection point. Bottle necks are especially prevalent in systems with large amounts of mix signal pathing and connections between the analogue and the digital domains – like in this system. On a single ground plane, component organisation requires greater though. Digital and high frequency components ideally should be positioned closer to the board input terminal and the analogue systems placed further away whilst taking care of current return paths. Other ground plane noise reduction strategies were enacted on the new hardware including localised system faraday cages soldered on the PCB.

Only one version of Interface Support hardware has fabricated. This system provided native support for Interface Version 4 and Version 5 function. Electronic hardware additions and alterations enacted to integrate all previous systems together will be covered within this section.

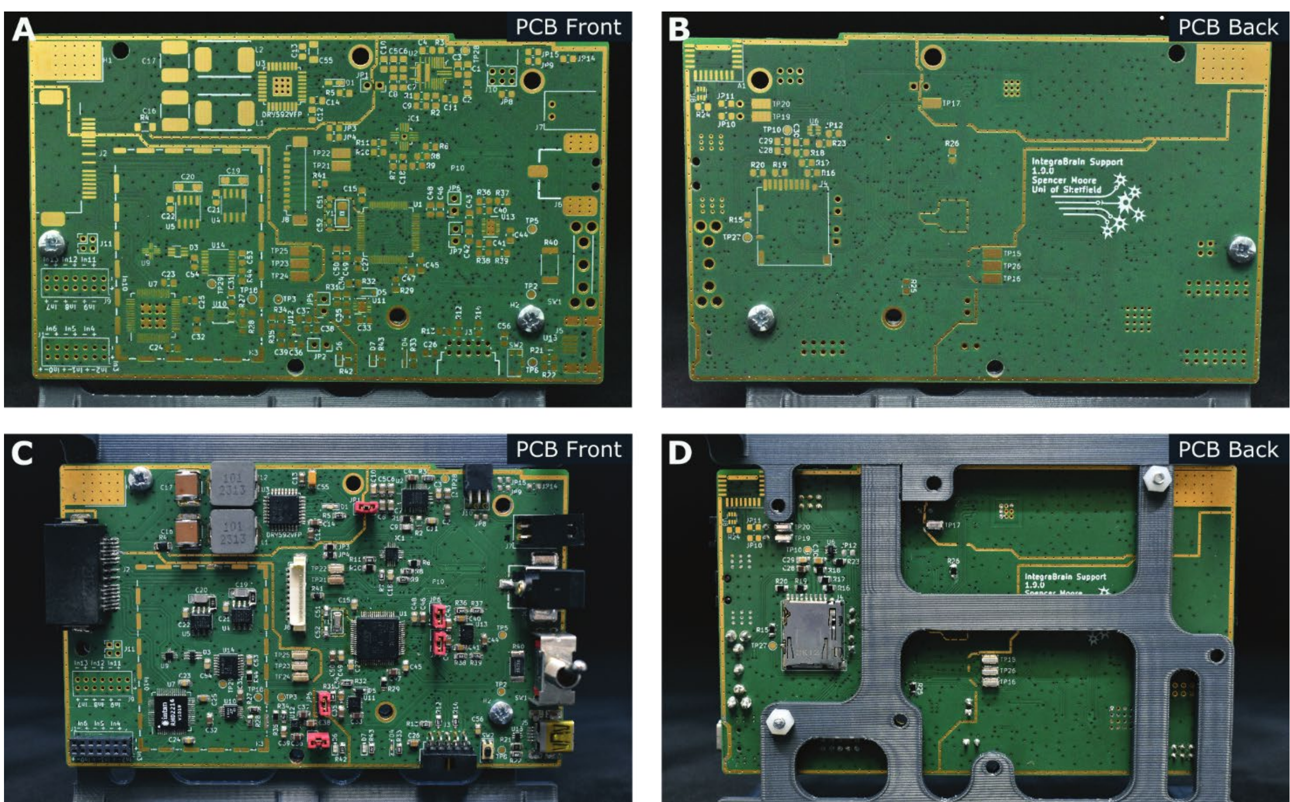


Figure 4.28 Fabricated Interface Support hardware.
The clean received PCB displaying the pad arrangement and markings on the front side (**A.**) and back side (**B.**). Post-soldering images of the Interface Support hardware with all components installed to ensure support for every Interface modality on its front (**C.**) and back (**D.**).

4.8.1 Microcontroller - STMU585

The merging of the microcontroller hardware with the modality support system provided the opportunity to upgraded the microcontrollers design to a newer ARM Cortex architecture. At the time of design, STMicroelectronics had recently released their implementation of Arm's Cortex-M33 core with their STMU5 series. This chance to move over to the newer processor architecture was undertaken to provide further computational buffer for new firmware additions. Code adaption to this hardware change would involve the alteration of pin allocations and some internal naming convention refactoring. It was predicted that alterations required for a new µC pin layout implementation would be approximately equal the alterations required to implement the previous µC. This would be due to pin remapping being required in both cases whilst the internal firmware functioning relies on standardised register naming that is near platform agnostic in the STM microcontroller range.

From the STMU5 series, the U585RI microcontroller was selected for the new architecture. This microcontroller contains additional mathematical hardware acceleration units (such as a CORDIC) on top of the discrete hardware modules that were found in the previous µC. The U585 has an increased flash memory of 2MB and 786kB of SRAM. Core clock frequency could now be programmed to 160MHz. Combining these upgrades together, moving to the U585 platform provides a 19% performance increase over the L476: giving the firmware more processing overhead for the seizure detection algorithm integration.

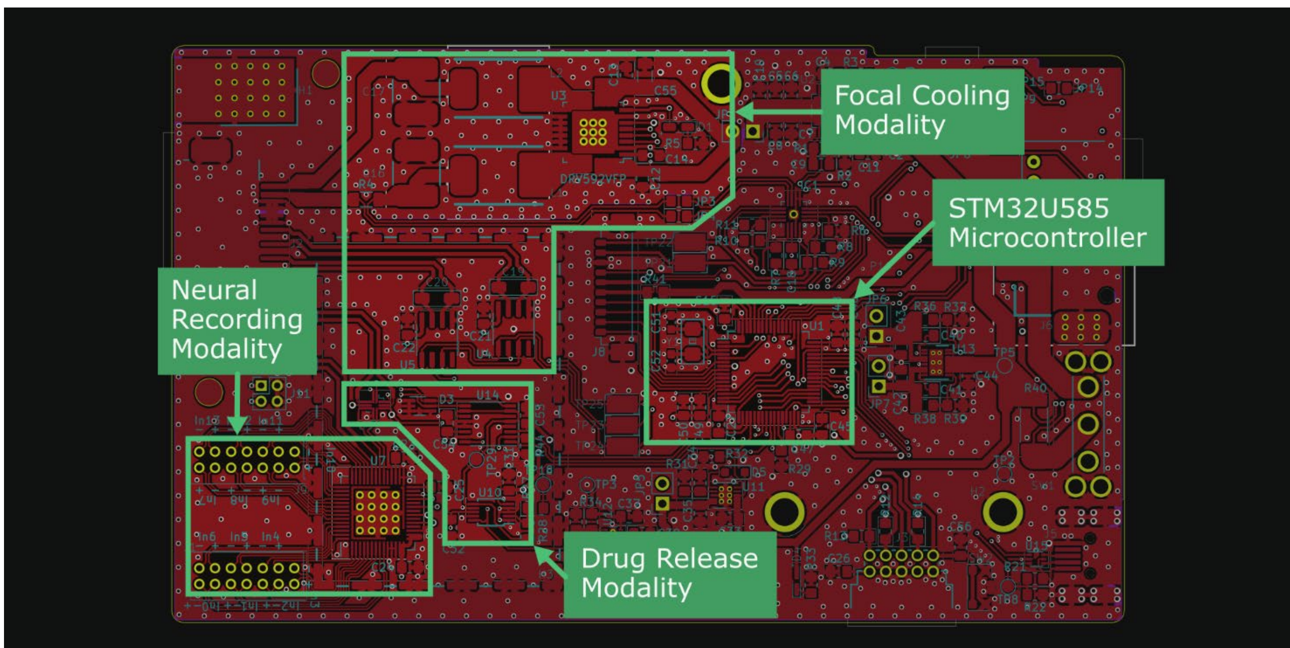


Figure 4.29 Modality electronic layout on the Interface Support hardware.
The neural recording, local drug release, and focal cooling electronic hardware sections are indicated in green alongside the placement of the microcontroller.

The U585 was sourced in its LQFP64 package – the same package that the L476RTG was the Nucleo-64 board. Having the similar package as before was an intentional choice to maintain backwards compatibility with the original microcontroller if porting to the new model began to negatively affect research progression. Pin allocation on both packages was near identical. Peripheral access to mirrored package pins was prioritised in the circuit layout so that, in the event of switching back, no functionality was lost e.g. ensuring SPI bus pins were the same on each setup. Logic GPIO pin functions were mapped to any un-used pin after peripheral allocation due to their location agnostic nature.

4.8.2 Intan RHD2216 Integration

With the Intan RHD2216 chip requiring very few external components, a direct port of the Intan breakout shield circuit design could be done to integrate it onto the Interface Support PCB. Previously indicated in Figure 4.29, the RHD2216 is placed close to the Interface-electronics interconnect board connector. This allowed short PCB track that quickly route away from the thermocouple signal lines. Alongside the move to the monolithic ground plane design, these design choices were enacted to help remove the 14Hz noise found injected into the neural signal recording by the thermocouple amplifier.

To also provide access to the spare 14 other bipolar channels found on the Intan IC, a set of two header pins were designed onto the PCB. This pair of 2x7 pin, 1.27mm pitch headers had Intan channels In2 to In15 routed out to them. Intan channels In0, designated Channel A, and In1, designated Channel B, were the bipolar channel inputs for the Interface electrodes.

4.8.3 Board Power Scheme

Power distribution and regulation on the Interface Support hardware received an overhaul form the previous designs. As the modality systems operation had been verified on the TEC Control hardware, time was spent reviewing the power system implementation to increase system efficiency. A new power scheme for Interface Support hardware was produced to architectural guide for the new blocks to be included (Figure 4.30A). Four separate power conditioning ICs would be deployed. A system 3.3V power rail would be regulated by a dual rail output, low noise LDO (LT3029, Linear Technology (LT), USA). Supply of the positive 3.3V rail for the analogue systems regulated by the ultra-low noise linear regulator LT3045 (LT, USA) and the negative analogue rail regulated by the LM27761 (Texas Instruments (TI), USA). TEC power would now be provided by the step-down power module MPM3650 from Monolithic Power Systems (MPS).

These power regulation systems serve greater power control flexibility during operation through power enable switch potential on each IC. They also provide cleaner regulation specifications for the analogue circuitry than the previous hardware. This was all achieved with circuit footprint area approximately the same as the previous power system set up (Figure 4.31B). Brief for each of these new systems is provided in the following sections.

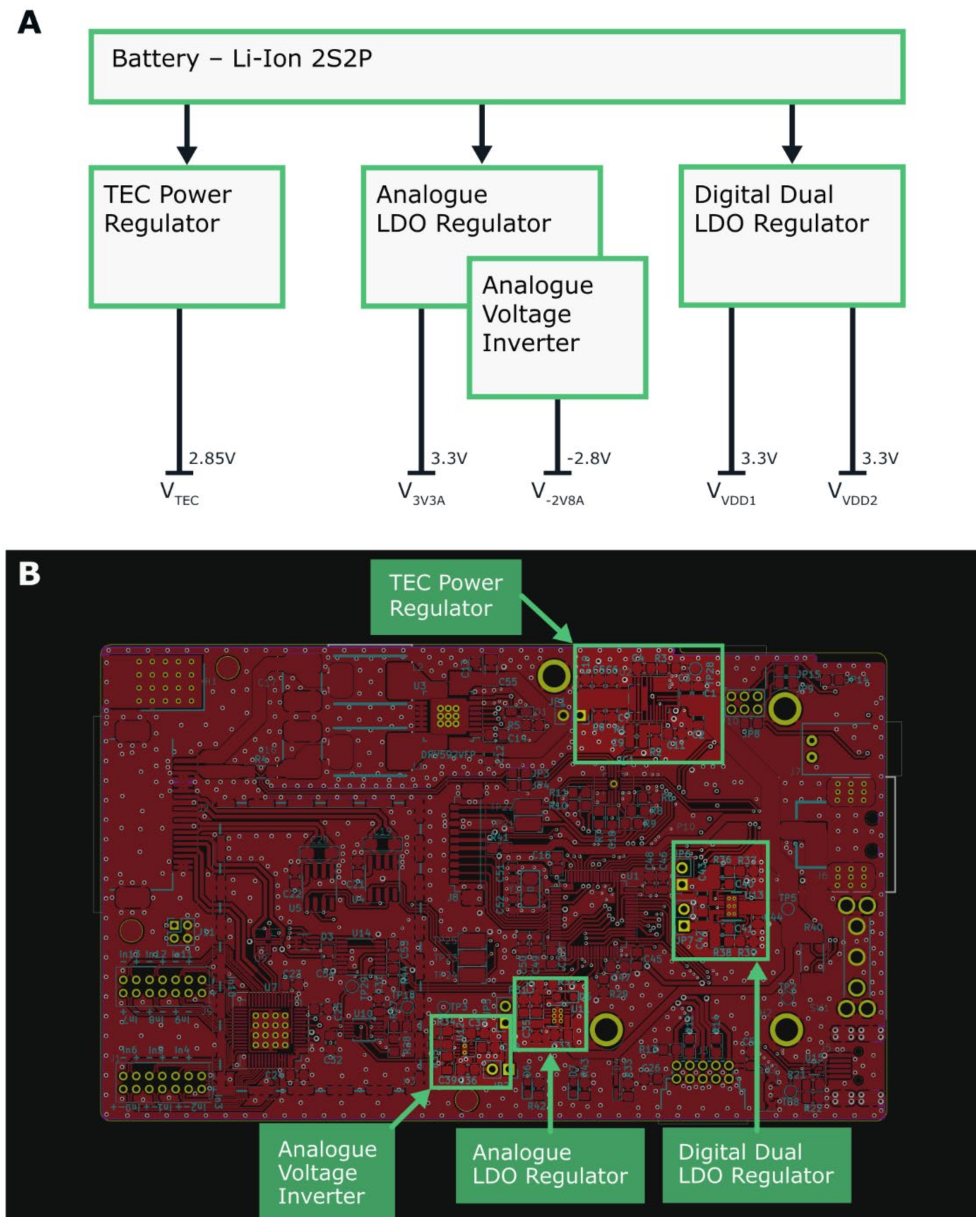


Figure 4.30 Power scheme for the Interface Support hardware.
A. Block diagram of the board's four power regulation rails that are designed support the differing modalities power requirements. **B.** Locations of the power regulating and conditioning circuits on the PCB layout design.

TEC Power Supply

Operation of the TEC Driver has been thoroughly validated through experimental operation. As the TEC can demand large instantaneous and steady-state power draws, having greater power efficiency in the regulator supply design was imperative. The previous LDO power regulator presented a power efficiency of between 34-40% during operation. The low power inefficiency of the LDO design stems from power lost as heat from the down regulation components because, at its core, the LDO is a voltage divider that relies on resistance for regulation.

Replacing this regulator design with a buck converter was the solution to the power efficiency issue. Unlike the LDO regulation through resistive power loss, switching power supplies use an inductive element to step-down the line voltage from the input value to the desired output. Feedback voltage sampled from the output rail enables active line regulation. Due to the inductive element of the supply using a DC-AC-DC conversion process to produce the voltage step-down, regulation can be performed with high power efficiency as there is no intentional power loss through resistive heating. With this regulator using a power conversion process, rather than a power loss process, it also enables the support higher current draws from its output rail than the regulator itself draws from its input rail supply.

In the case of the TEC driver regulator, the MPM3650 (Monolithic Power Supplies, USA) was selected. It is a variable output voltage buck regulator that can supply up to 6A with a power efficiency between 70% – 95%. This regulator is designed to need a low number of external components to reduce required layout space (Figure 4.32). This power module has an internal switching inductor which removes a normally large external component. Output feedback of voltage divider sets the rail voltage to 2.85V for the TEC Driver to use. A software limit was still in place for the TEC driver output because of the TEC specifications. However, TEC power profiling has allowed the limit to be raised to 80%. An enable input gave the µC control of the TEC system's powered state. Allowing power consumption reduction and additional safety in case of TEC Driver failure.

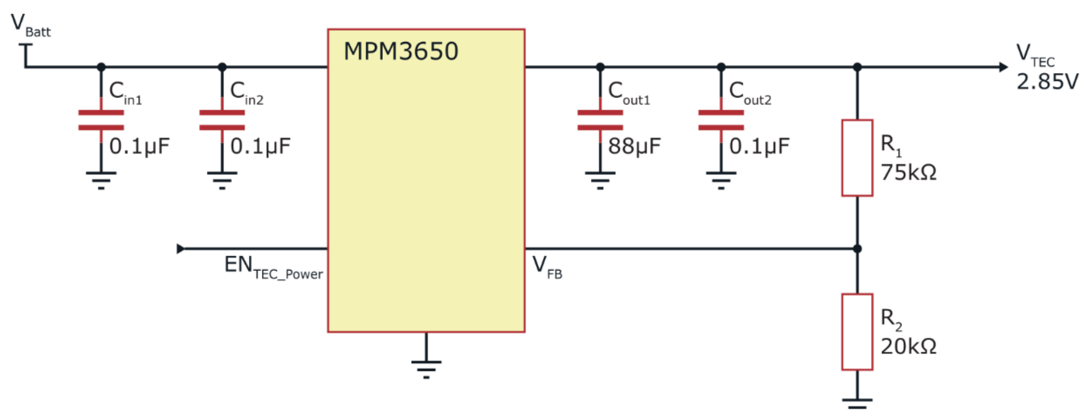


Figure 4.31 Simplified circuit diagram of updated TEC driver power supply.
A MPM3650 (MPS, USA) is set to regulate its output rail to 2.85V for the DRV592 TEC driver IC. V_{batt} input voltage is rated to 7.2-8.4V for expected operational behaviour.

Analogue Electronics Power Regulation

The increase in digital systems and the addition of the local drug delivery electronics warranted the inclusion of a separate power regulator system for the analogue electronics. These electronics include the Intan IC, drug delivery signal conditioning, thermocouple amplifiers, and electrode multiplexing. This system was designed to supply both a general +3.3V rail and a drug delivery specific -2.8V rail (Figure 4.32A).

The LT3045 (TI, USA) is an ultralow noise, linear regulator that was used to provide the +3.3V analogue rail. It is capable to supplying up to 500mA whilst imparting only 0.8μV_{rms} of noise into the regulated output rail (10Hz to 100kHz). To reduce feedthrough noise from its input supply, the LT3045 has a high average Power Supply Rejection Ration (PSRR) being 76dB at 1MHz. Both specifications remove the need to worry about the power supply rail being a vector for noise injection into neural recordings – with correct layout implementation. Instead of a voltage divider on the regulators output, a separate SET pin and single resistor required to set the output voltage (Figure 4.32B).

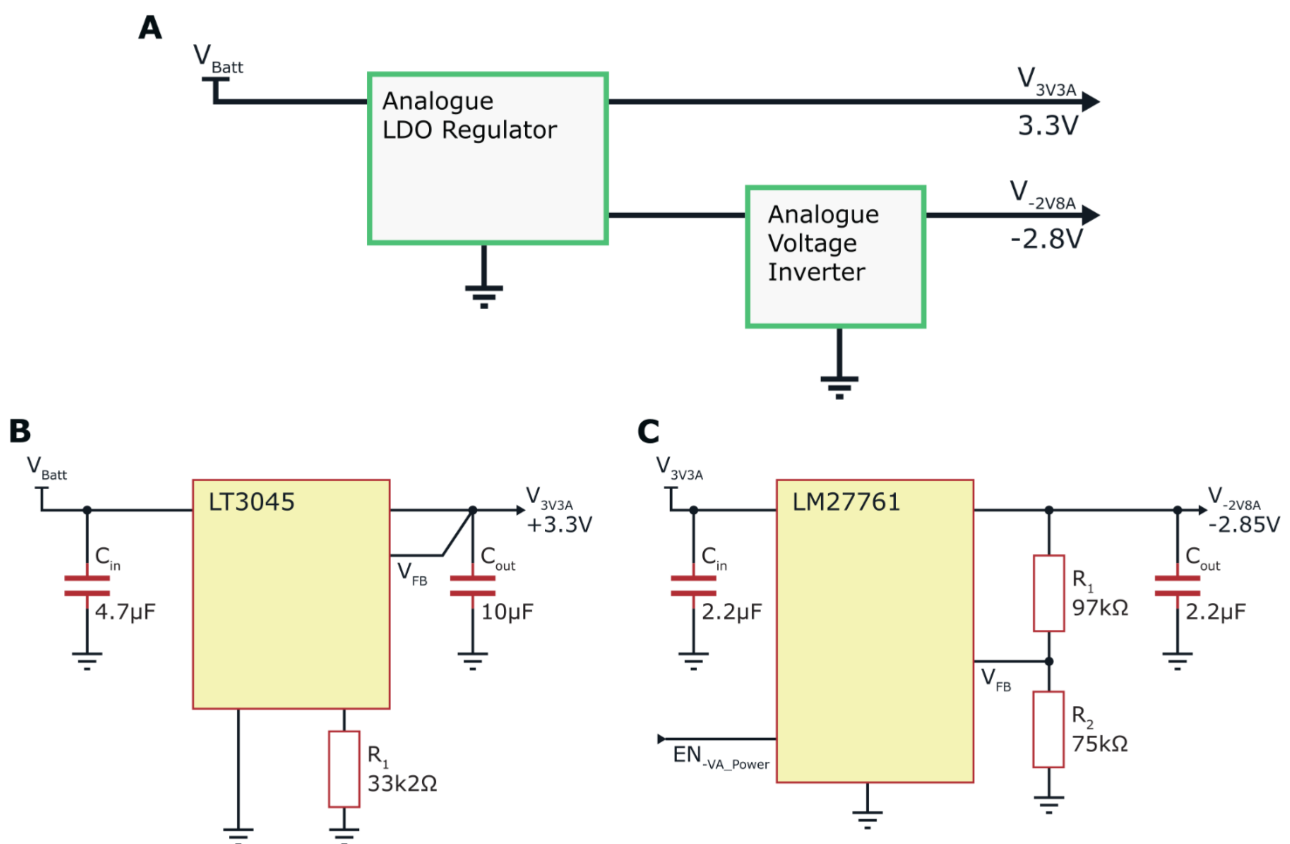


Figure 4.32 Updated analogue power regulation systems.
A. Block diagram for the power regulation and conditioning components required to support the analogue circuitry. An expanded description of the circuitry setup for the (**B.**) LT3045 to supply the 3.3v analogue rail, and the (**C.**) LM27761 to supply the inverted -2.8V analogue rail.

As will be discussed in Section 4.8.8 , the drug delivery modality requires a negative voltage rail to support its hardware requirements. To achieve this, a voltage inverter LM27761 (TI, USA) was deployed. This system utilises a switch-capacitor circuit to invert a positive voltage input to a negative voltage with respect to system ground. For this instance, the converter draws its input from the LT3045 +3.3V rail and inverts it to supply -2.8V on its output. Through internal IC buffering of the charge-pump output, this regulator is able to achieve 20μV_{rms} noise on its output. Ensuring that ultralow rail noise conditions are maintained. Regulation is managed by a voltage divider on the output rail (Figure 4.32C).

Digital System Power Supply

The digital electronics on the Interface Support hardware maintains the +3.3V rail requirements as before. However, to expand overall hardware functionality new digital systems were introduced including a micro-SD card slot and support for a Bluetooth module. As implementation of these systems were untested, they both needed to be on a isolated supply rail.

Providing this functionality is the LT3029 (LT, USA)– a low noise, dual output LDO linear regulator that is capable of supplying 500mA from each output. Both outputs were regulated to +3.3V. This regulator provided the ability to toggle each outputs supply. The primary supply rail was set by constantly enabled whenever power was applied to the regulator's input ensuring constant μC function. The new, untested hardware was placed on the second supply rail whose activation state is managed by the μC (Figure 4.33).

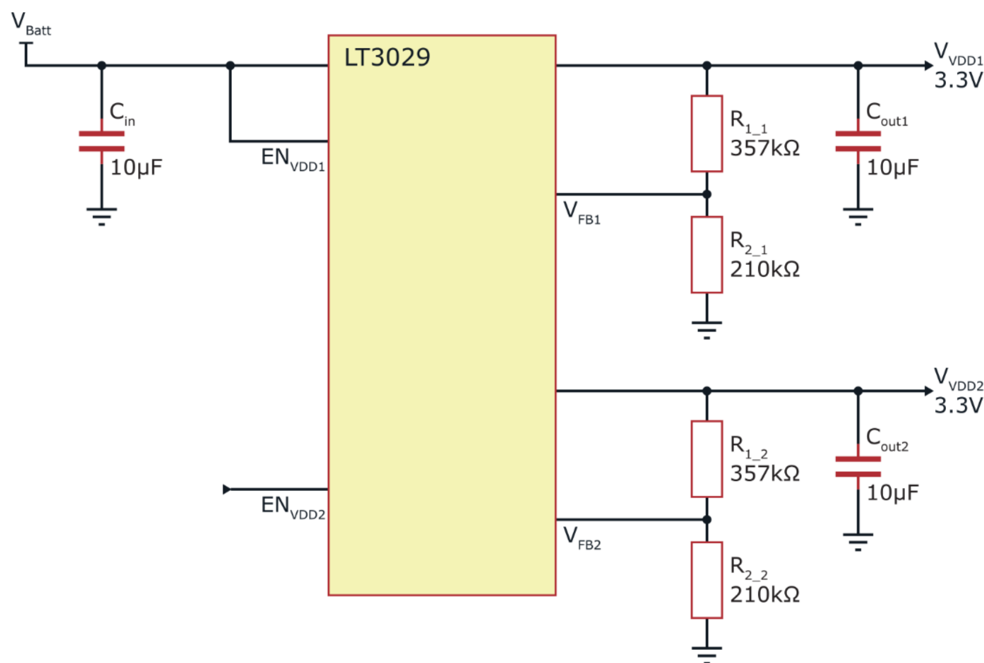


Figure 4.33 Circuit description for regulated +3.3V rails.
A dual output, linear regulator had both supply rails set to +3.3V. V_{VDD1} supplies the μC, power monitor, and the TEC driver digital logic. Its output permanently enabled. V_{VDD2} supplies the Bluetooth module and SD card slot. Output status of the V_{VDD2} is manually controlled via the μC.

4.8.4 Focal Cooling Electronics

The TEC driver and thermocouple amplifier circuitry was largely retained from the previous hardware design as it had been verified to function reliably. The input/output of both systems was placed close to the Interface-electronics board connector to provide the shortest signal path possible. For the thermocouple amplifiers, this was to ensure that the cold junction compensation was valid during temperature sampling. For the TEC driver, this was to reduce the occurrence joule heating in the board interconnects during high current driving of the TEC.

Only two aspects of the focal cooling circuitry were altered when porting it to the Interface Support hardware – the circuit layout, and the TEC driver output filter component values. Layout changes were to be expected due to the new placement of surrounding elements and layout requirements. However, the choice was made to investigate altering the TEC driver filter components as is discussed in the following section.

TEC Current Source Filter

When deciding on the TEC LC filter component values for the previous hardware setup, the limiting factor on its implementation was the requirement to use THT components for breadboard testing. The transfer to the monolithic PCB design provides the opportunity to replace these THT filter components with SMD mounted variants. This allows access to a more diverse range of components values that enables for further filter refinement. An investigation was then conducted into updating the filter components to lower layout area needs and improve filter function.

Using Equations (3-5), an iterative process was again conducted in the same manner as when the values were first calculated. With access to the larger component value range, large component values in small packages could be sourced. From the iterative process, the values of L = 100μH, C = 68μF were selected. The filters f_0 was now 1.93kHz and causes an attenuation of -88dB at 312.5kHz. The maximum ripple current within the TEC driving signal would now be 106μA. This translated to a 0.0045% ripple current ratio and, using equation (1), would only causes a ~0.0015°C reduction of the TEC's maximum specified temperature difference. This smaller ripple current further decreases the effects of TEC degradation due to the AC components in the driving signal.

Components selected to implement these new filter values were both SMD. The selected package for the inductor was a shielded vertical core coil power inductor in a low profile 10 x 11 x 5.1mm package (SRP1050WA-101M, Bourns). For the capacitor. a dual parallel ceramic capacitor with a X7R dialectic and in a 6.1 x 5.3 x 6.4mm package was chosen (KRM55 series, Murata).

4.8.5 System Power Monitoring

Power monitoring within the integrated systems was expanded to provide finer consumption details. Using the same PAC194x series IC, an additional two sense resistors were added to monitor the total system power drawn from the battery, and the power drawn by the µFluidic shield (Figure 4.34). All current sense resistors are placed on the high-side of the systems they were designed to monitor as specified in the PAC194x layout guide. The µFluidic shield sense resistor is place on the Interface Support hardware PCB on the power supply rail of the board-to-shield connector.

For the TEC current sensing, the sense resistor value was decreased to 40mΩ from 28mΩ. This reduced the maximum sense current to 2.5A but increased the current sense resolution to 76.3µA per bit using the ±100mV full scale range. The lower sense resistance as reduced power loss due to joule heating in the TEC driving signal.

For the µFluidic shield current sensing, the full-scale range was set to 100mV. Sensing accuracy around 0V is not desired for this input as there was a minimum current draw by the SPM-041 when idle. The sense resistor value of 125mΩ was calculated that allowed a maximum sense current of 0.8A. This is above test measurements taken during stand-alone tests of µFluidic shield. Sense resistor needed a ≥100mW power rating. The sensed current resolution was 12µA.

For the total system input current sensing, the FSR was set to ±100mV so all potential current flow conditions could be sensed. The maximum calculated expected current draw by whole system was ~3.2A. This estimate was then scaled to provide the 10% safety overhead to make the required sense resistor value be 28mΩ. This would provide a full-scale current range of 3.57A and provided a 108.9µA sense resolution. The estimated maximum current draw through the sense resistor required it to have power rating of ≥450mW.

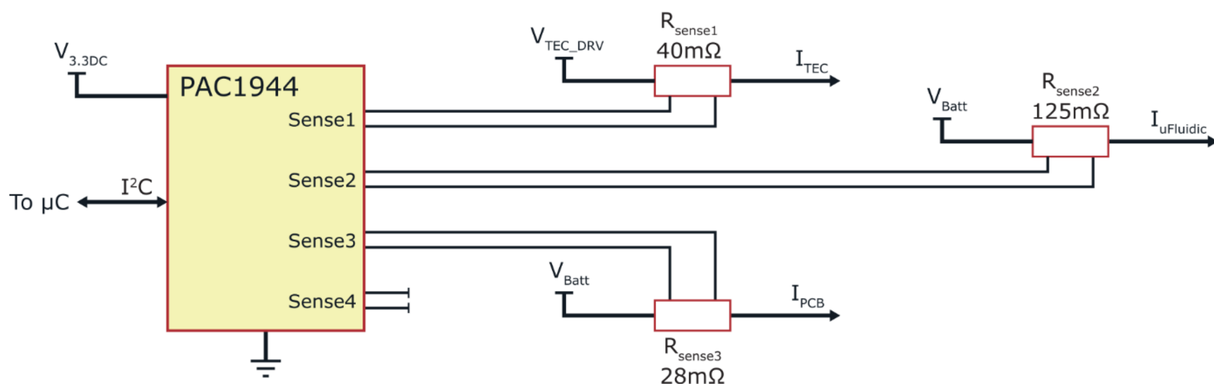


Figure 4.34 Circuit diagram of the PAC1943/4 on the Interface Support hardware.
Three sense input are now used on the PAC194x IC thus either the PAC1943 or the PAC1944 had to be used. Sense1 input monitors the TEC driver current. Sense2 input monitors the µFluidic shield current draw. Sense3 monitors the total system current drawn from the Interface Support power source.

4.8.6 Interface-PCB Connection

A desire to simplify the Interface-electronics connection led to the introduction of a monolithic, uni-orientation interconnect cable connection to the Interface Support hardware. This was achieved through the Mini Dynamic connector system (TE Connectivity, USA). Located on the opposing edge to the board power input, a 16-pin Mini Dynamic connector was mounted flush to the edge of the PCB board (Figure 4.35A).

The high pin quantity provided the means to spread the Interface-electronic interconnect cable pin locations out to ease PCB track routing from its footprint (Figure 4.35B). Space between the TEC driver connections and the thermocouple connection lessens the potential influence of high-current joule heating at the amplifier's cold junction. Spacing of the between the thermocouple and electrode pins is part of the continuing effort to reduce possible thermocouple noise influence on the neural signal recordings.

Extra pin locations, that were not utilised for Interface modality control or sensing, were all connected to ground to prevent them from forming floating potentials. These extra pins also enabled the addition of grounded shielding to be added around the Interface-electronics interconnect cable. This shielding was formed from a woven fibreglass-steel wire mesh. The interconnect cable wires were fed the mesh before they were mounted into the Mini Dynamic connector. The raw shielding end at the Omnetics connector end of the cable was bonded to the connector using the thermal epoxy – preventing it from riding down the cable during use. At the board connection end of the interconnect cable, sections of the steel wire was gathered from the mesh weave and crimped into a pin for mounting into a Grounded location on the Mini Dynamic

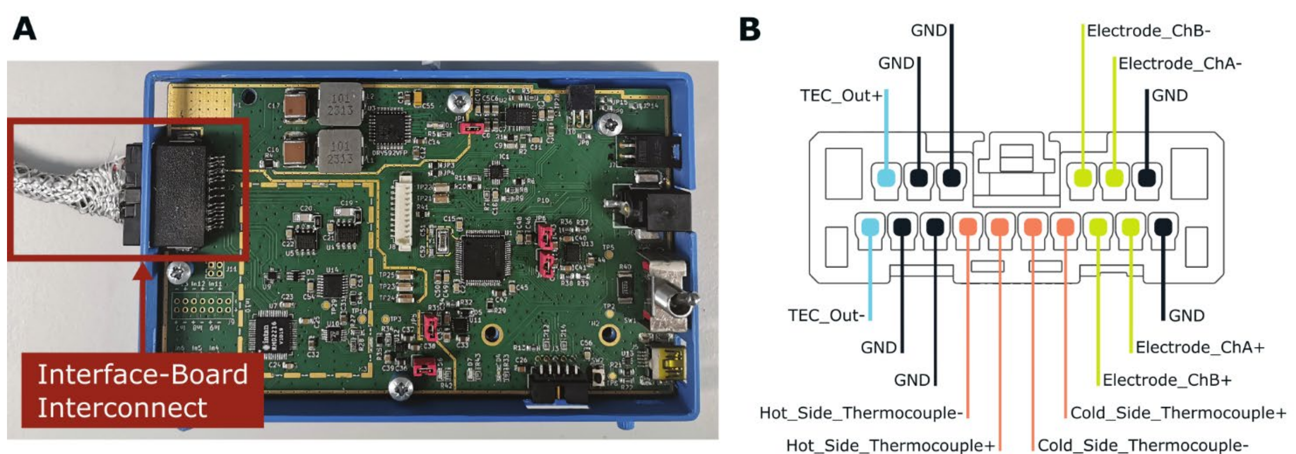


Figure 4.35 The monolithic Interface-electronic board connector.
A. Location of the connector when mounted on the Interface Support hardware. **B.** The connector pin allocation description where the locations of the TEC power, thermocouple, and electrode interconnect wire pins are located. All spare pins are connected to board ground or are utilised to provide a ground connection to the shielding to the Interface-electronics interconnect cable.

connector

4.8.7 µFluidic Shield Support

Having the monolithic Interface Support hardware PCB being designed post-development of the µFluidic shield board meant native support for it could be designed into the PCB layout. To ease hardware testing, the circuitry of the µFluidic systems remained as a shield board for this hardware iteration. Instead, the shield's mounting holes pattern was copied onto the PCB layout and a vertical 10-pin Picoblade connector was added (Figure 4.36). 8mm high stand-offs could then be used to mount the µFluidic shield directly to the board during studies – if that layout is desired.

The shield connection was mounted onto the Interface Support hardware PCB to provide a direct shield-compatible connection. This enabled a tight system coupling between the main board and µFluidic shield during *In Vivo* experiment and easy system deconstruction post-experiment. When directly mounted to the main board, rubber gaskets installed at the shield's connection to the stand-offs to attenuate high frequency vibration from the pumping hardware. Stand-offs mounting holes on the main board PCB are metallised and linked to the boards ground plane to prevent stand-offs floating if supplied in a conductive material. The shield's board mount holes are not metallised. Instead, shield ground is linked to the main board via the 10-pin Picoblade ribbon cable connection. PCB layer order of both boards is identical thus the µFluidic shield layouts can be ported to the main Interface Support hardware board to reduce system size in future iterations.

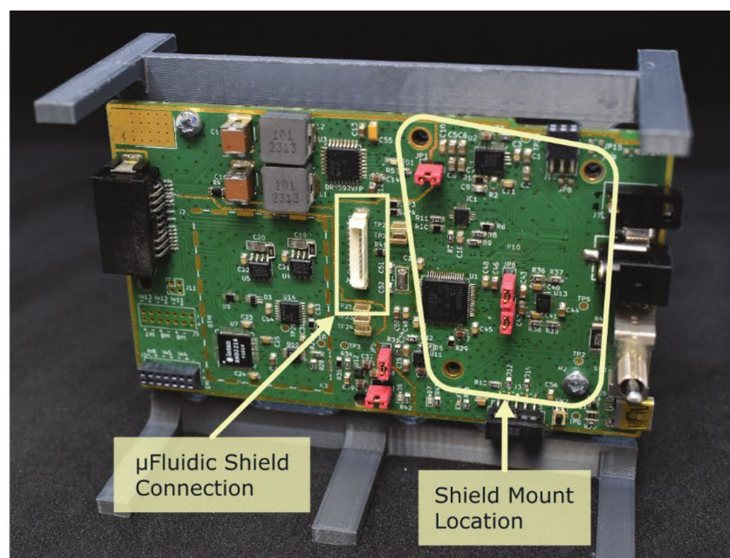


Figure 4.36 µFluidic shield interfacing on the main Interface Support board.
A 10-pin vertical Picoblade connector (Molex, USA) provides a shield-compatible power and system communication link to the µFluidic systems. Mounting holes on the main board mirror those of the shield's

4.8.9 Drug Release Hardware

As a preface to this modalities hardware discussion – this system was in preparation to undergo testing during the writing of this thesis. This section will then focus on providing a circuit design overview and release control mechanisms available from the setup. During the Interface Support hardware development, it was established that the drug release would involve the encapsulation to drug molecules within a PEDOT matrix allowing the local release of drug to be electrically actuated.

To release the drug, a negative potential needed to be applied to the PEDOT material. Magnitude of this potential would control the drugs release rate. The maximum applied potential was limited to -1.6V to prevent hydrolysis within neural tissues. The circuit requirements were thus:

- To able to supply potential that can be varied from 0V to -1.6V.
- To apply this potential to the drug delivery electrodes in controllable combinations.

A circuit design to satisfy these requirements was designed (Figure 4.37). Control over the output potential's magnitude would be provided by the µC's onboard Digital to Analogue converter (DAC). The 12-bit DAC on the STMU585 can be setup to output a potential between 0V and +3.3V. Implementation of a software limiter to restrict the DAC output to a 1.6V maximum would be required. To invert the DAC signal output, the high-precision and zero output drift op-amp (LTC2057, LT) is used. The DAC output would be routed into the inverting input of the op-amp which then would outputs the negative mirror of this signal. The negative supply rail enables the op-amp to develop negative potentials.

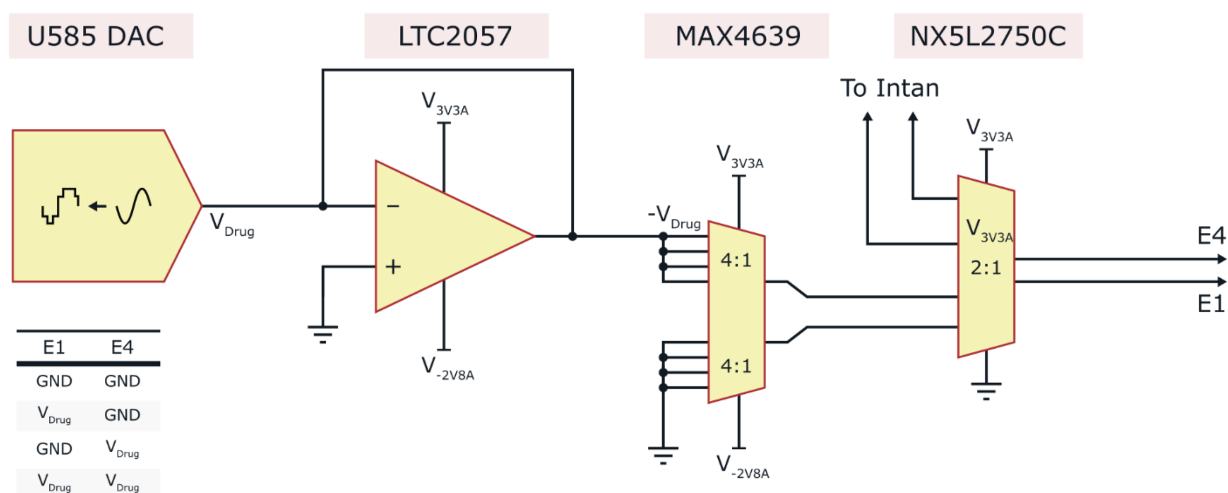


Figure 4.37 Overview circuit design for the drug delivery modality.
The system is designed to provide robust control over the potential applied to the drug loaded electrodes. The µC DAC supports an output potential range of 0-1.6V. The LTC2057 inverts the signal to a negative potential with unity gain. Feeding this into the MAX4639 dual 4:1 multiplexer enabled applied electrode potential patterns – electrode potential output matrix table is in the bottom left corner. A NX5L2750C switch allows for the electrode pair to reused as neural recording electrodes in release idle periods.

The op-amp would be set to unity gain; thus, it also seconds as a buffer between the μC and electrodes. Any current that would be source by the drug laded electrodes supplied via the op-amp. The inverted control signal would then be routed into dual 4:1 multiplexer (MAX4639, Maxim Integrated). At this point in the research project the required configuration or control of the electrode potentials is unknown. Having this multiplexer in the electrode signal path provides the means to implement all possible drug delivery electrode ground/potential application schemes. Control of this would be achieved programmatically via the Interface firmware.

After the multiplexer for the drug delivery electrodes, the drug release control signals would route through another multiplexer (NXK2750C, NXP). This multiplexer would provide control over which modality system is connected to the drug delivery electrodes. As the PEDOT material presents conductive properties, the drug delivery electrode could also provide neural recording capabilities. This switch would enable this to occur without both systems concurrently vying for use of the electrodes. In theory, the electrodes could then be utilised for neural recording purposes when drug release is not required or after the loaded drug had been depleted. As the drug electrodes are to be constructed using Pl/Ir wire, even if the drug loaded hydrogel were to degrade, the wire would still be able to record neural signals.

4.8.10 Data Output and Debugging

To ease introduction of the Interface Support hardware, the system was still designed to interface with the host PC over USART. There was no native USART-to-USB hardware implemented directly in the PCB design. Instead, the raw USART output from the μC was routed to a connector header. The USART signal pair would need to be linked to the ST-LINK V2 debugger on a Nucleo-64 board. The Serial Wire Debugger (SWD) and USART-to-USB converter hardware within the debugger are exposed for external hardware connections. It is these two features that are utilised to interface with the Interface Support hardware providing the ability to flash the hardware with updated firmware and collect experimental data.

Utilisation of this Nucleo-64 feature did smooth the transition over to the new hardware. However, the Nucleo-64's USART-to-USB converters maximum baud rate of 115200 had begun to impede the quantity of live data that could be streamed during experiments. In anticipation of this occurrence, multiple options were built into the Interface Support hardware design that could be implemented when needed. These include a USB 2.0 interface, a Bluetooth module, and a microSD card slot. However, due to time constraints and limited deployment experience with the required SD storage and USB standards, these data solutions have yet to be developed. As an intermediary, study specific data packet structures were hardcoded into the firmware so that the data deemed necessary for that study would be streamed live whilst un-needed data remains on μC.

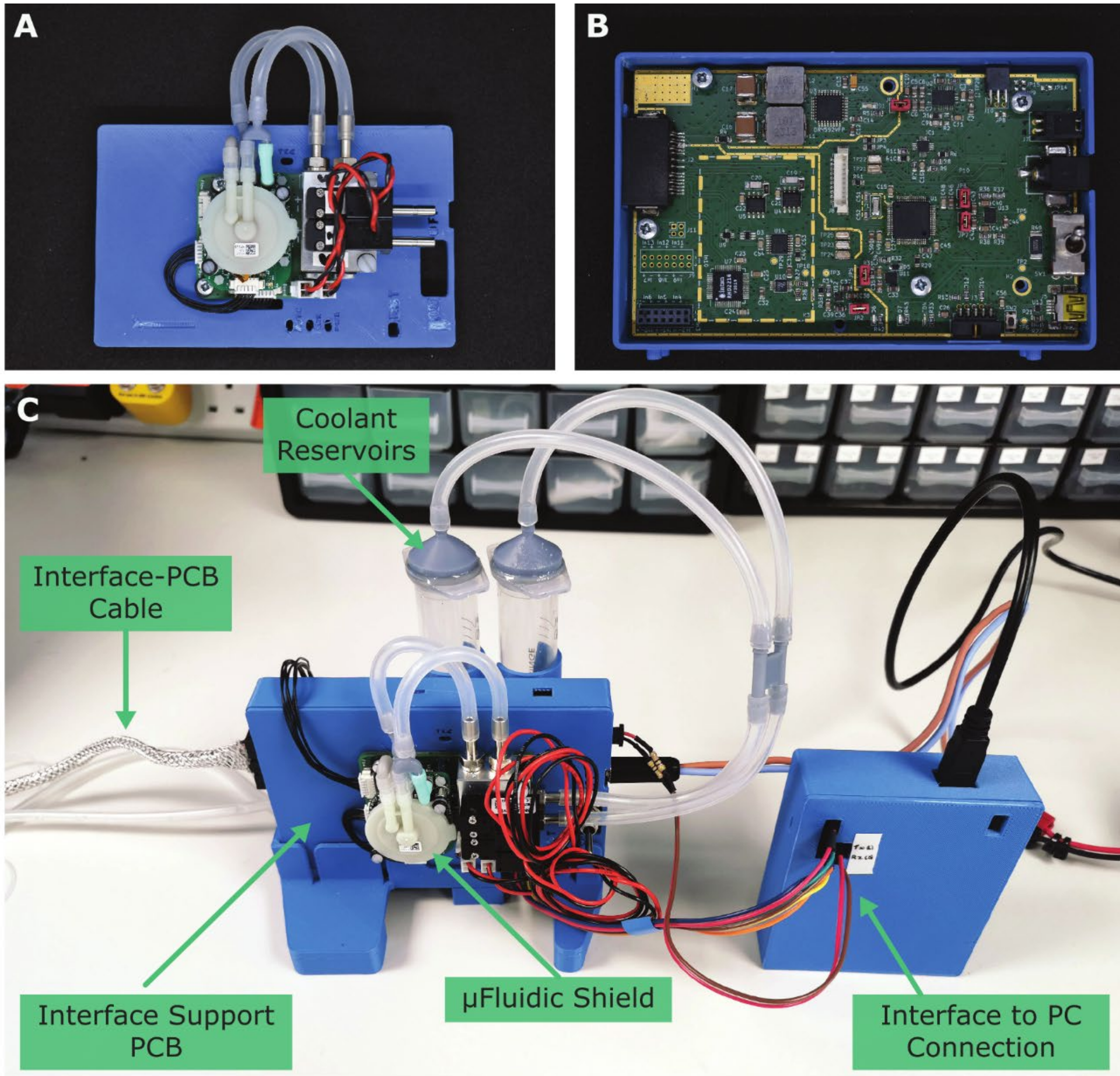


Figure 4.38 Experimental Interface Support hardware in a 3D printed housing.
3D printed housing for the Interface Support hardware provided external mounting for the µFluidic shield (**A.**) and internal mounting for the main board (**B.**). **C.** In the full study setup, the Interface Support hardware is orientated upright with access to microfluidic system tubing and all board connections. Microfluidic coolant reservoirs are mounted upright. Secondary hardware for interfacing the Interface Support hardware with the host PC is contained within a separate case.

4.8.12 Experimental Setup

To protect the Interface Support hardware during experimental use, a suite of 3D printed cases and stands were fabricated out of PLA. The main board and μFluidic shield were mounted to the same printed case. The shield had a mounting point on the case lids surface whilst the main board was mounted - via 3mm screw – inside of the case's body (Figure 4.38A-B). The case provided electrical isolation for the main board, preventing electrostatic discharge from occurring near the board's ICs. Externally mounting the μFluidic shield provided ease of access to the microfluidic system connection points for attaching the system's silicone tubing. Experience gained through setup and breakdown during studies lead to this mounting preference over direct mounting the shield onto the main board. A slot in the lid provided routing access for the board-μFluidic shield's ribbon cable link. The case lid was held in place through internal wall clips and the boards power toggle switch threaded shaft. This case resulted in the Interface Support hardware size being 75 x 130 x 50mm.

This case can then be slotted into a 3D printed stand (Figure 4.38C). This mount held the Interface Support hardware case upright along the case's longest side. Mount clips and alignment posts securely held the case in place. At one end, access to the Interface-electronic interconnect cable connector was presented. At the opposite end, access to the power barrel connector, USART header and SWD header are presented. Locations of these connections differentiates the Interface facing end and the Host PC facing end. This helps guides whomever was setting the system up as to where the required cables connection points were located and makes cable management simpler during experiments. On the back of the stand were two locations in which the microfluidic reservoirs can be placed and will maintain them in the necessary upright orientation. There was a clip mount which held the flow meter during experiments.

Since the Nucleo-64 development board was still required during experiments, a separate case was fabricated for it. The board was fixed into the case with 3mm mount screws. Slots in the lid of the case was designed to only expose the pin headers of the debugger and the UART-to-USB converter. A slot in the cases body presented access to the development boards USB connection to link to the host PC. During *In Vivo* studies, this USB connection was bridged via a USB cable with a built in opto-isolator. Isolating the animal model from mains supplied equipment is crucial for the animal's safety. Electrical isolation prevents ground loops from forming in the equipment and animal model. Ground loop formation can result in the unwanted currents flows, system noise, and potential electrocution of the model. A battery pack was always used to supply the Interface Support hardware with the required power during *In Vivo* studies to maintain this isolation.

4.9 Summary

The multimodal nature of the constructed Interface's required custom electronic hardware to be able to support modality function. This hardware was based around an ARM-based microcontroller core which would be flashed with a firmware to control and monitor Interface function. Using a STM32L476 Nucleo-64 development board, the TEC Control shield was fabricated to support the focal cooling modality. Two T-type thermocouple amplifiers enabled temperature sensing with an ±0.25°C resolution. To manage the potential <2.4A TEC driving signal, was DRV592 IC was selected and controlled via a PWM signal. 2nd order passive RLC low pass filters placed on its output to reduce AC ripple currents and improve TEC cooling performance.

Coolant fluid flow through the Interface's Microfluidic Loop was supported by a centrifugal pump that was enabled during cooling runs to prevent thermal runaway. A flow meter, located in line with the fluid flow, recorded a maximum achieved fluid flow rate of ~5.4ml/min by the centrifugal pump. Issues with trapped air formation in the pump housing and the pump adding heat to the coolant fluid led to the implementation of a piezoelectric air pump system. Though it was of greater complexity, requiring air valves and an additional coolant reservoir, it presented a marked increase in performance over the pervious system. The maximum achievable flow rate with the new pump was ~71ml/min whilst recording no rise in coolant temperature due to the pumping system.

The printed electrodes introduced in the Interface Version 4 required neural recording hardware to enable this modality. An Intan RHD2216 ASIC was sourced to convert the bipolar electrode signal to the digital domain. A Intan breakout shield was designed exposed the electrode input pins and link to the I^{2}C bus on the TEC Control shield.

The final step was to integrate all tested modality layouts and microcontroller into a single piece of hardware. A PCB was designed to allow this and the integration of hardware to support a future drug release modality. TEC driver filter components were recalculated to further reduce ripple current inefficiencies in the TEC driving signal. The previous microcontroller model was upgraded to a STM32U585 that presented a 19% increase in computational power to support future firmware additions. Power regulation circuits were replaced with low noise regulators for the analogue domain, a segmented regulator with enable control for the digital domain, and a power efficient step-down converter for the TEC driver system. Housed within a 3D printed, PLA case for protection, the Interface Support hardware could be mounted with a stand for ease of use and access during experimental session. This hardware demonstrates the ability to create a highly integrated suite of systems to support the Interface's function whilst also providing a route to further miniaturisation on the path to clinical deployment.

Chapter 5

Embedded Support Firmware

This chapter covers the software developed over the course of this research – specifically the firmware deployed on the microcontroller hardware, and the data collection graphical user interface (GUI). All firmware produced for the microcontroller was written in the C programming language using the ISO/IEC 9899:1999 standard. The PC GUIs is constructed using the graphical programming environment, LabVIEW, using its proprietary visual programming language - G (National Instruments, USA). LabVIEW programme development was conducted in the 2022 Q3 version.

Content is ordered to aid in understanding the building of the project's software. Information is provided to give context of language used for those reading from out of field. Discussion then turns to the implementation of the TEC controller both in theory and with a pseudo-code version in C. The main Interface Support firmware flow and system timings are then described.

The rest of the chapter covers the interfacing LabVIEW suite of virtual instruments (VIs) that were developed specifically to be deployed in tandem with the Interface Support firmware. These VIs provided data collection and hardware control services in experiments. Toward the end, a section covers the initial integration of a seizure detection algorithm into the code base with performance testing to gauge full deployment suitability. All software presented is the version used with the Interface Support hardware. The firmware has just undergone continual refinement over the course of this research project to support continual integration of new Interface modality support.

5.1 Integrated Development Environments

To write, debug and deploy code intended for a microcontroller platform, an integrated development environment (IDE) was used. IDEs for embedded systems generally provide all of the tools required for creating embedded firmware within a single utility. These IDEs can be intended to target a specific hardware series or instruction set families. For the ARM-based microcontrollers used during this project, an appropriate IDE was µVision (ARM Keil, Germany). Software names and versions used over the firmware development are listed on Table 5.1.

The nature of IDE design means that the workflow flow is contained to a single programme (Figure 5.1). Code is written and revised in the IDE's source editor. Once the code is ready to test on hardware, it needs to be compiled from C into machine readable code. The source and header files are passed through the compiler that creates an object file for each input. These object files contain the machine code (or binaries). Optimisation options in the compiler allow the tuning of code size or speed. A linker is then used to link the object files together based on header file descriptions – including any specified user or 3rd party libraries – to create a single executable.

Table 5.1 Software tools used during the development of the embedded firmware.

Software Type	Software Name	Vender	Version
IDE	µVision	ARM Keil	5.38.0.0
Compiler	ArmClang	ARM	6.19
Linker	ArmLink	ARM	6.20
Hex Converter	FromElf	ARM	6.21
Software API	CMSIS_CORE	ARM	5.9.0
Device Firmware Package	STM32L4xx_DFP	STMicroelectronics	2.6.1
	STM32U5xx_DFP	STMicroelectronics	2.1.0

Hooking up the target hardware to a PC via a debugging tool (hardware integrated or discrete) provides the physical connection that the IDE's flasher uses to upload the executable to the hardware. Once uploaded, debugging mode can be entered on the IDE. It is common for an IDE to have a separate layout or window to display debugging specific information. This can include the display of register values, memory locations, variables, timing analyser, and more. Debugging functionality and information visualisation is dependent on IDE options and what debug related pins are exposed for connection. The two industry dominant protocols for debug connection are Joint Test Action Group (JTAG) and SWD. Over this project, SWD was the default debugging interface utilised.

5.2 Microcontroller Registers

Control over a microcontrollers internal hardware and peripheral function is achieved through the manipulation of registers. Each microcontroller sub-system has a discrete register set that allows the programmer to setup internal hardware (Clocks, memory, cache's, etc) and to interact with peripherals (GPIO, Timers, USART, etc.). Register function, layout and options are supplied by the microcontroller manufacturer. These are generally termed "Reference Manuals" that are released alongside a microcontroller's datasheet.

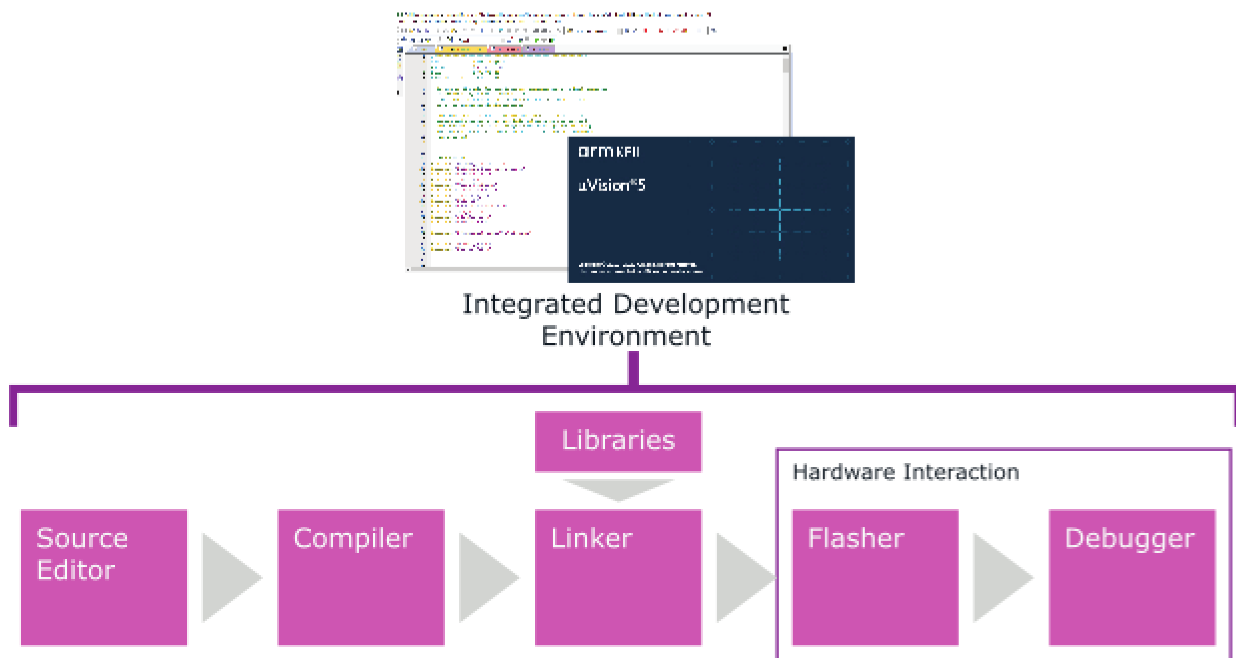
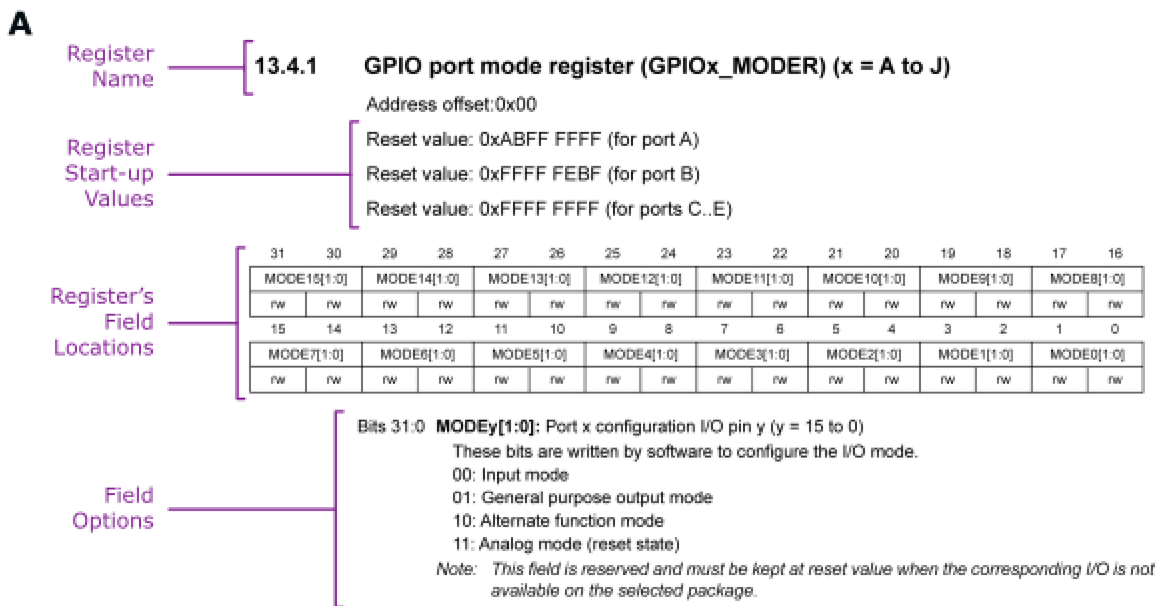


Figure 5.1 Tool Workflow of the Keil µVision v5 integrated development environment (IDE).

Every register has a full name and a short-hand name (Figure 5.2A). This short-hand version can be used as a human readable reference when coding. What is contained within that register is described in the field options section. Here the fields name, bit size, location in array, value options, and function is detailed. In this case, the register fields set the GPIO pin mode and provide four available modes to choose. Th bit width of these fields vary with its function. Location of the fields in the register are also visually represented and are labelled with the fields access rights. The default register field states – on start-up or after reset – are provided that relays the default peripheral behaviour if no field changes are made.

Manipulation of these register from their default state is how the desired behaviour is achieved (Figure 5.2B). Here the register, GPIOA_MODER, is being manipulated to alter PA2 and PA3 modes from a default value of [1 1] to [1 0]. It is now in the alternate function mode for use as USART pins. Other register access – to complete the GPIO setup – is then detailed in the subsequent lines. The field labels within this code are from the device's header file within the device firmware package (DFP) that is supplied by the microcontrollers manufacturer through the IDE.



B

```
54    /*-- GPIO Setup - Rx & Tx --*/
55    GPIOA->MODER     &=  ~(GPIO_MODER_MODE2_Msk  |              // Clear PA2 & PA3 MODE Bits
56                            GPIO_MODER_MODE3_Msk  );
57    GPIOA->MODER     |=   (GPIO_MODER_MODE2_1  |                // PA2 - Alternative Function Mode
58                            GPIO_MODER_MODE3_1  );              // PA3 - Alternative Function Mode
59
60    GPIOA->OSPEEDR   |=   (GPIO_OSPEEDR_OSPEED2_1  |            // PA2 - High Speed GPIO
61                            GPIO_OSPEEDR_OSPEED3_1  );          // PA3 - High Speed GPIO
62
63    GPIOA->AFR[  0]   |=  (  0x7  <<  GPIO_AFRL_AFSEL2_Pos);   // PA2 Alt Function 7 USART2_TX
64    GPIOA->AFR[  0]   |=  (  0x7  <<  GPIO_AFRL_AFSEL3_Pos);   // PA3 Alt Function 7 USART2_RX
```

Figure 5.2 Microcontroller register description for peripheral control.
A. GPIO port mode register description sourced from the STM32U5xx Reference Manual [144]. Section labels of the descriptor indicate their function. **B.** An example of GPIO control derived from the Interface Support firmware demonstrating setting GPIO pins to their alt function through register manipulation.

5.3 Embedded Firmware File Structure

To make the embedded firmware more human readable, navigable and easier to debug, the whole firmware is broken down into source files, .c, and header files, .h. These two files are core to writing legible C-based programs. They both work in tandem to describe the programmes' structure, function, and output. .h files normally contain the programmes declaration statements. These inform the compiler that the stated object will exist and are assigned a specific label or name. With this, it also declares object type it is (struct, function, macro, etc.). Whereas .c files contain the definitions of those declared objects. These definitions describe to the compiler what the programme logic of the object – what it was created to perform.

By grouping like-function definitions and declarations, they can be compartmentalising into sets of .c and .h file pairs. Through this, non-local access to functions and other definitions can be strictly controlled. External access to the .c definitions can be granted by having a '#include .h' statement within a source's file.

For the Interface Support firmware, the system declarations and definitions are currently sorted into groups based on their peripheral attribute. For instance, all functions related to using the SPI peripheral (RHD2216, thermocouple amplifier) are contained within one .c file whereas all that need the I^{2}C peripheral are in another (Figure 5.3).

As this firmware is written for a highly specialised purpose, a generic function access coding style was not implemented. Instead, all the functions are highly coupled and only present input/outputs to satisfy the required intra-firmware operability. Comments are heavily utilised throughout the code to describe its function and purpose. The Interface Support firmware is available through a GitHub repository.

Interface Support Firmware v1

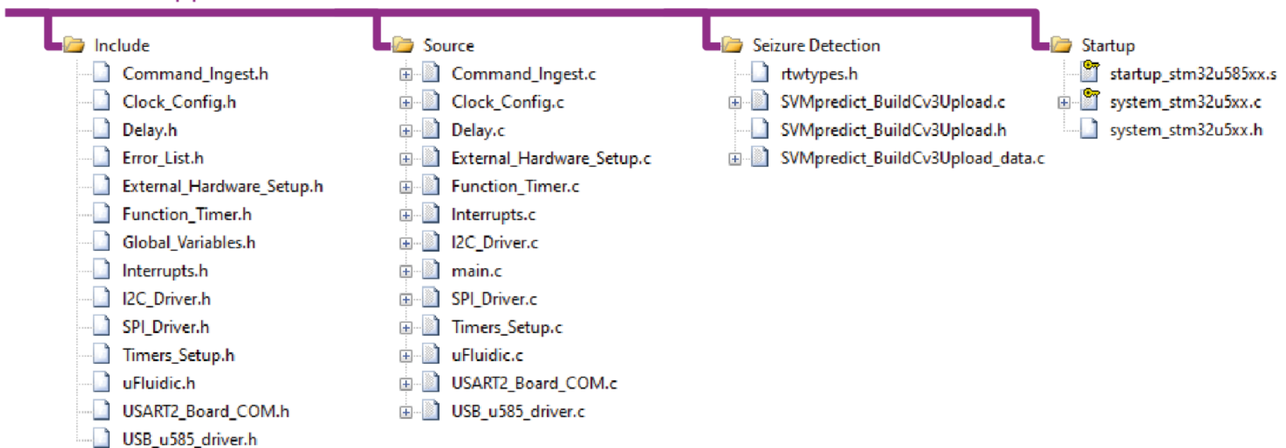


Figure 5.3 Interface Support Firmware v1 file structure.
Include and Source folders contain the main elements to operate the focal cooling and neural recording modality hardware. The seizure detection folder isolates the algorithm files as they are updated with regular occurrence. Startup contains the code for microcontroller hardware initialisation. These are vendor supplied for the microcontroller.

5.4 Bus Communication Types

Information flow around the electronic hardware is achieved through communication buses that are regulated by the microcontroller. To enforce component interoperability, a number of bus architectures have been widely adopted and standardised by industry. This greatly simplified both the hardware and software implementation in communicating data. The main bus architecture utilised by this system were UART, SPI, and I^2C. The following are brief descriptors of these protocols and their utilisation.

5.4.1 UART

Universal Asynchronous Receiver/Transmitter (UART) is an early serial architecture that is still utilised today. It provides a simple form of serial communication, requiring only two interconnect wires to establish communication (full duplex) and a light message frame protocol. The two wire lines are referred to as Tx (Transmit line) and Rx (Receive line). There is no shared clock between the devices using UART so bus speed and data frame format must be known beforehand. Data sent over the bus must conform to the set frame protocol to be understood. The base frame format requirement consists of 1 start bit, 8 data bits, and 1 stop bit. This framing instructs the receiver on how the sent data is to be sliced and read.

On the Interface Support system, UART was used for routing data out to the host PC during experiments. This was performed at a 115.2k baud rate (or bit/s) which is the upper limit imposed by the Nucleo-64 hardware utilised for its UART-to-USB converter. A major pitfall of using UART is that it has no built-in bulk data transfer protocol that codifies a standard message start/stop delimiter. Thus, for messages with more than one frame, a marker protocol and command sorting function was required for robust data flow control Interface Support systems and the host PC. This is further discussed in Section 5.6.3.

5.4.2 SPI

SPI is a pseudo-standard synchronous serial architecture developed to enable high-speed data transfers. Communication flow through SPI is achieve by a controller/peripheral system – to be referred to as main and sub respectively. The main is always in full control of the data bus and must specify which sub it wants to communicate with. A full duplex SPI connection consists of four wires:

- Serial Clock (SCK) – for the main to supply a clock signal to the subs.
- Main Out/Sub In (MOSI) – for the data that flows from the main to a sub.
- Main In/Sub Out (MISO) – for the data that flows from the sub to the main.

- Chip Select (~CS) – specify to which sub the main is communicating with.

In a multi-device system, every sub is attached to the same MOSI, MISO, and SCK in parallel. However, every sub must have a sperate ~CS line – unless simultaneous communication is desired. This demand puts a pseudo-restriction on the number of devices that one main can handle based on the availability of GPIO pins. The strict control over data transfer start, transfer stop, and transfer window length allows for the offloading of bulk data frames between the main and a sub.

For the Interface Support system, only the thermocouple amplifiers and the Intan RHD2216 support the SPI bus architecture. Communication was achieved at two rates. For the RHD2216 it was 20MHz and for the amplifiers it was 5MHz (due to hardware limitation). During normal operation, the SPI bus was maintained at the 20MHz clock frequency due the majority of the data transfer being with the Intan IC. At the point when the amplifiers needed to be sampled, the SPI clock frequency was temporarily switched to 5MHz until the temperature data is collected. It was then shifted back to the 20MHz before returning to the regular software flow.

5.4.3 I2C

I^2C is an architecture primarily design for use in embedded systems where the interconnect distances are short. It functions via a synchronous, multi-controller/multi-target design for low-speed data transfers. I^2C only requires two wires for operation. These two are called the Serial Data Line (SDA) and the Serial Clock Line (SCL). Having only one data line means that data transfer is bi-directional. Establishing who is the intended target for communication is performed through the sending of a 7-bit address at the start of a message. Data flow on the bus is directed through a read/write bit attached to the target address. Each device on the bus is required to have a unique address to prevent arbitration issues.

Unlike other bus architectures, I^2C lines are not push/pull driven but rather are controlled via an open-drain switch configuration. This is enabled through each line being constantly held high by a pull-up resistor to the system supply voltage. It helps to prevent short circuits occurring in the case that multiple controllers and/or targets are trying to simultaneously begin a transmission request sequence.

On the Interface Support system, an I^2C bus was used by the power monitor, SPM-041, and the flow sensor to communicate with the microcontroller. The bus frequency was set to 400kHz to support all of the target's bus controller specifications.

5.5 PID Controller for TEC Function

To ensure reliable and stable TEC cooling control, a controller with closed-loop feedback was required. A commonly deployed type of controller is a proportional, integral, and derivative (PID) controller. It is an effective control solution which presents relatively low complexity when it comes to implementation in software. The PID controller is described by

$$u(t) = K_p e(t) + K_i \int_0^t e(t)\, dt + K_d \frac{de(t)}{dt} \quad (5.1)$$

Where $e(t)$ is the control variable error calculated from the difference between the measured process variable and set point (reference process variable). K_p is the proportional term gain that scales the current system error. K_i is the integral terms gain that scales the accumulation of past system error. K_d is the differential terms gain that scales the system error's rate of change. $u(t)$ is the sum of the three terms that make up the controller.

By adjusting the control gain magnitudes, the system output can be tuned to produce the desired controlling behaviour. In effect, the PID controller is altering the control output by collating a review of the system's past state, a snapshot of its current state, and a prediction of its future state.

5.5.1 Controller Design

The desire for the TEC controller was for it to have a low programming complexity and one that is computationally light. This was to ensure there was enough free computational time for the seizure detection algorithm to complete its calculation within strict time limits. The base PID controller schematic to be implemented in the code invoked a bare controller structure (Figure 5.4). An anti-windup limiter was added to the integral term to prevent its oversaturation effecting controller behaviour during potential setpoint changes.

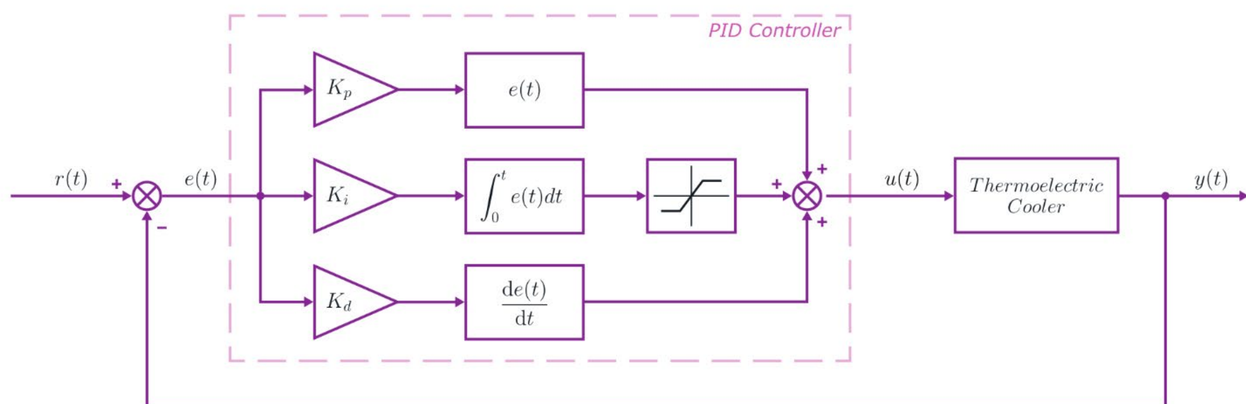


Figure 5.4 PID controller schematic for TEC cold-side temperature control.
Anti-windup for the integral term is placed to limit the terms magnitude during function. System signals are labelled with r(t) being the setpoint value, e(t) being the error signal, u(t) being the controller output signal, and y(t) being the resultant TEC output based on the u(t) input.

The setpoint signal, r(t), input was limited to be between the values of 10°C to 37°C. TEC current was restricted to flow in a single direction so only cooling actuation was possible. The PID controller outputs a value between 0 and 100. This output was then interpreted by the system as a percentage to set the PWM control signal, u(t), duty cycle magnitude. This signal was output by the µC into the DRV592. This control signal directly modulates the power output driven through the TEC and influenced the depth of cooling achieved by the cold-side. It is this temperature of the TEC cold-side, the y(t) signal, that is sensed by the thermocouples and is used to evaluate the systems error from setpoint.

The TEC control loop – which the PID controller was within – was set to update at an 8Hz rate. Loop refresh rate was hard limited by the maximum sampling rate specified for the MAX31855 thermocouple amplifier that are used. These ICs exhibit a maximum potential sampling time of 100ms (10Hz). In order to collect the temperature data reliably, the control sample time had to be no more than this. An 8Hz rate was chosen to satisfy this need and to fit in with the interrupt timings of the other systems (Section 5.6.2).

5.5.2 Simple PID Controller Implementation

The TEC controller implemented for cooling control was a simple discrete-time version of the TEC's PID controller design (Figure 5.4). The controllers pseudo-code structure was thus:

```
static float      Error_Prior       = 0;
static float      Integral_Prior    = 0;
static float      Interval_Time     = 0.125f;

/* Set Point Error */
Error                        = Cold_Side - *T_Ref_P;


/* KP Calculation */
Proportional                 = (*KP_Gain_P * Error);

/* KP Saturation Limiter */
if(Proportional > 100){
      Proportional           = 100;
}


/* KI Calculation */
Integral                     = (Integral_Prior + (Error * Interval_Time));

/* Anti-Windup & Anti-Super Saturation */
if(((*KI_Gain_P * Integral) >= 40)){
      Integral               = 40;
      Integral_Prior         = Integral;
}
else if(*KI_Gain_P <= 0){
      Integral               = 0;
}
else{
      Integral_Prior         = Integral;
      Integral               = (*KI_Gain_P * Integral);
}
```

```
/* KD Calculation */
Derivative              = *KD_Gain_P * ((Error - Error_Prior)/Interval_Time);
Error_Prior             = Error;


/* PID Controller Summation [0->100] */
PID_Output              = Proportional + Integral + Derivative;


/* PID Output Limiter - Hardware Maximum Output = 80% */
if(PID_Output < 0) {
      PID_Output        = 0;
}
else if(PID_Output > 80){
      PID_Output        = 80;
}

/* PID Controller Output to PWM Conversion */
PWM_Value               = ((uint16_t) (256 * PID_Output)/100);
TIM1->CCR1              = PWM_Value;
```

The PID function required only the TEC cold-side temperature as the input process variable. The set point error was calculated before the controller terms are sequentially solved. The forward Euler method was used to approximate the integral and differential terms in this discrete implementation. The sum of all PID terms is calculated at the functions end. This summation is interpreted as a 0-100% value that dictates have much power to drive to the TEC. To convert this to the TEC Driver control signal, the product of the TEC driving PWM duty cycle resolution (256) and the PID output percentage was calculated. The resultant duty cycle is then inputted into the required TIM1 register to present that change in the TEC driver control signal.

Multiple saturation limiters were imposed within the controller's setup. These exist on the proportional term, the integral term, and the PID summation. The term-based limits are to prevent each of them from overwhelming the controller output and to reduce the instability in the TECs performance during cooling runs. Limiter values were developed through a trial-and-error process during Interface performance testing. Limiting of the summed PID value is to account for the discrepancy in the TEC maximum specified input voltage and the TEC Driver's minimum supply voltage. This results in the need to reduce the maximum TEC control signal duty cycle to 80% power. Duty cycle resolution was reduced to ~204 discrete power levels as a result.

5.5.3 Controller Limitations

Whilst use of the PID controller was sufficient for the control of the TEC during this project, it is not the optimal solution. The elephant in the room of implementing this system was that a PID controller functions best for physical systems that displays linear behaviour and have symmetrical control actuation. Neither of these conditions are fulfilled by the TEC system dynamics. Thus, the controller's performance can be seen as degraded as a direct result.

Firstly, a TEC is an inherently non-linear system. Dynamics that TECs exhibit, such as the Peltier effect and joule heating coupled with the device's temperature dependant physical properties, all contribute to this significate non-linearity. Secondly, the TEC actuation is intentionally set to have asymmetric actuation as a safety mechanism – performing only active cooling and never reversing to produce active heating. This prevents neural tissue from ever being directly heat by the TEC in the case of unexpected disturbances that could cause controller instability.

To alleviate the performance degradation of using a basic PID controller design, modifications or alternate controllers were sought. Cascading a PID controller with a feedforward controller [145] has been proposed to improve base PID controller performance which introduces a system model to account to a TEC's behaviour [146, 147]. The effectiveness of the model-based feedforward controller is sensitive to the accuracy of the system model. Fuzzy logic-based control has been shown to provide effective and robust control options, but determination system appropriate initial membership functions and fuzzy rules can present difficulties [148, 149, 150]. More complex forms of gain scheduling/tuning have been achieved with the deployment of a neural network (NN). These NN controller are designed to perform online optimisation of controller gains through repeated controller-system function [151, 152]. Though demonstrated performance gains come at the cost of increased controller complexity and computational load.

Whilst these controller alterations were explored through literature exploration, none found implementation within this work beyond that. Research time dedicated to controller performance improvement – beyond the PID controller gain scheduling – was limited and would benefit from dedicated development in future work on this system.

5.6 Interface Support Firmware

Through this section, the Interface Support firmware will be described. This programme is written to support the multimodal functionality of the Interface through software control of the Interface Support hardware. This firmware has been in continuous development over the duration of this research. New code function was added whenever there was modality additions or alterations were made to the Interface or electronic systems. Initial deployment was targeted toward the STM32L476 microcontroller used for the TEC Control hardware. This was then superseded by the Interface Support hardware which required the firmware to be refactored for deployment on the STM32U585.

The firmware was written using a bare-metal programming style. In which direct register manipulation, as described in Section 5.2 , was used as opposed to using vendor produced code abstraction libraries, such as Hardware Abstraction Layer (HAL) from STM. The primary driver for using this programming style is ensuring that all sampling times are accurate. The generalised nature of HAL functions means would be difficult to optimise towards achieving hard real-time code execution where the sampling intervals exhibit little-to-no deviation. Direct register interaction allows for the fine trimming of internal hardware clocks that control the data sampling rates. However, by choosing to programme bare-metal and application specific, the firmware could be seen as 'locked' to the hardware setup. This is somewhat alleviated by having CMSIS reduced that effect as found when porting the firmware to the STM32U585.

5.6.1 Programme Flow

Structure of the firmware was split into the main programme flow and the interrupt service routine. The main programme flow was the default state that the firmware operates within (Figure 5.5). Upon the applying power to the microcontroller, the firmware begins by initialising the internal microcontroller peripherals and clocks, and then the external ICs. The microcontroller core clock was the first system to be set. The core clock is altered, from its default of 4MHz, to 80MHz. It used the Multi-Speed Internal (MSI) clock set to 16MHz and a Phase-Lock Loop (PLL) to increase the core clock to 80MHz. An external 32.768kHz crystal was used to automatically trim the MSI oscillator output during run-time.

After the core clock, all required microcontroller bus clocks and peripheral clocks were enabled. Microcontroller peripherals – UART, SPI, Timers, etc - are then enabled and set. A Direct Memory Access (DMA) buffer is setup for the UART to automate the exchange of data with the host PC. Using the activated communication buses, the external ICs are communicated with to modify their internal registers for the correct function. Upon completion of hardware setup, the final firmware initialisation action is to enable the Nested Vectored Interrupt Controller (NVIC). Enabling NVIC allows the firmware to begin servicing of all unmasked interrupts that would now occur.

Moving into the main programme loop of the firmware, it was formed of a single, infinite while() loop that contained the TEC PID controller update function and the thermal data output function calls. Calling either of these functions is conditional to the current firmware state - that is indicated by two boolean flags. One flag is set when there was new thermocouple sensor data available to service by the thermal modality functions. The other is the TEC control system flag. This flag indicates wherever a cooling run was currently been undertaken. User sent commands to the hardware, via the host PC, is the only way to toggle the TEC control system on. The TEC PID controller update call is conditional to both new sensor data being available and the TEC control system being active. The thermal data out function only requires the new sensor data flag to be set. After the data is processed for sending to the host PC, the new thermocouple data available flag is flipped to zero to indicate the data has been serviced and to prevent the same data being sent out in duplicate.

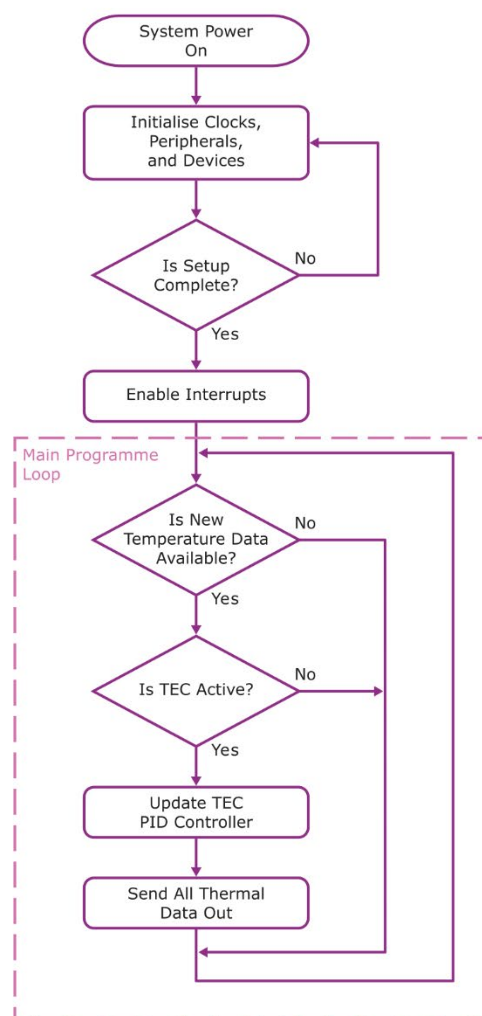


Figure 5.5 Main firmware programme flow.
System performs a single initialisation of the microcontroller systems before interrupts are enabled and the main programme loop is entered.

5.6.2 Interrupts

Interrupt Service Routines (ISR) are used to breakout from the normal programme flow to service an event that has occurred. Once the event is serviced, the normal programme flow is resumed at the breakout point. Interrupts are used for event-driven function calls that are needed to be executed as soon as the event flag is raised. Interrupts are especially useful for time critical operations and can be used to emulate hard-time code execution within a soft-time system. The NVIC handles the monitoring of system interrupt flags and calls the flagged routines for servicing on the STM32 chipsets hardware.

Within this firmware, three interrupts are enabled for servicing. These, in order of highest priority to lowest, are:

- EXTI15_10
- TIM3
- UART2

UART2 Interrupt

The UART2 ISR function was to notify the system that a message has been received from the host PC over the UART and was ready to be processed. Trigger event for this interrupt to flag was for the UART line to transition into the Idle state after a message was received. Upon entering the ISR, the UART Idle flag is first checked to verify that a valid ISR call was made. If it was not valid, then all UART interrupt flags were reset and the ISR routine exited. If it was valid, the UART ISR calls the UART input processing function. This function was written to service the input data and interpret its command. It was the main function in the suite developed for commanding the Interface system that is discussed in Section (5.6.4). After processing the input message, the UART ISR resets all UART interrupt flags before the main programme flow is returned to.

TIM3 Interrupt

The TIM3 ISR controls the systems data sampling timings. This ISR takes presidents over all other interrupts – apart from those that handle system errors – to achieve a pseudo hard real-time operation. This ensures that all data samples are taken at constant sampling intervals. TIM3 is a general purpose 32-bit timer on the STMU585. It was pre-scaled from the main system clock to an 8MHz rate. The internal counter was loaded to update at 256Hz rate. This update produces a flag that is used to trigger the TIM3 ISR call. Within this routine, the update flag is first checked to ensure a valid ISR call. If valid, the Intan IC is commanded to produce a neural signal sample from electrode Channel A & B (Figure 5.6). Once the Intan samples are received by the microcontroller, the microfluidic coolant system, and the thermal systems are checked if they require sampling.

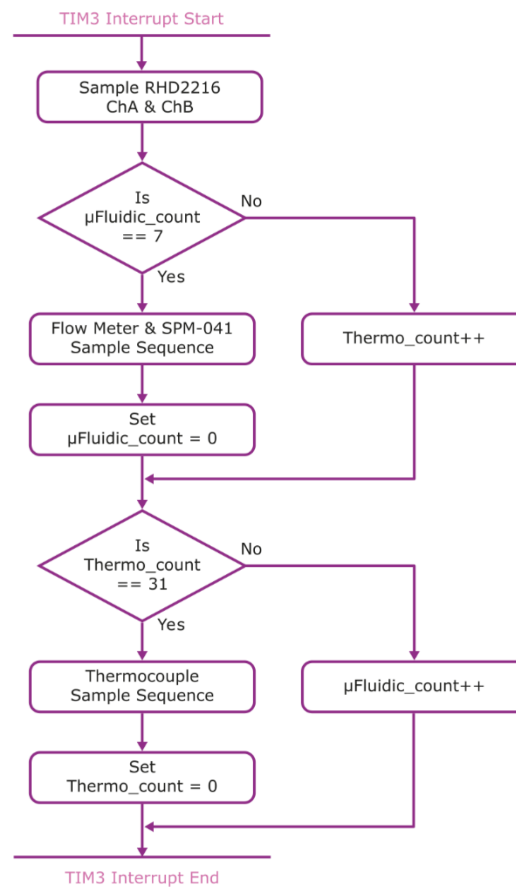


Figure 5.6 Data sampling interrupt triggered by the TIM3 clock.
Intan, uFluidic and thermal sampling was performed at a 256Hz, 32Hz, and 8Hz rate respectively.

256Hz was chosen as the sample rate to satisfy the seizure detection algorithm design constrains. This provides the 0Hz to 128Hz frequency band that the algorithm can monitor for seizure activity occurrence. To support this, the Intan IC has internal filters that are set to have high-pass cut off at 0.5Hz and a low-pass cut off at 128Hz in order to prevent aliasing. Programming the Intan IC filters takes place in the hardware initialisation portion of the main programme flow.

Sample rates for the microfluidic and thermal systems were dictated by two counts within the ISR – the μFluidic_count and thermal_count respectively. These counts enable the different hardware systems to be sampled at dissimilar rates whilst contained within a single ISR call. Sampling limitation are imposed on the rates. These are that the hardware specified sampling rates that sets the upper/lower bounds that they can support, and that the sampling rate must be a factor of 256. These led to the microfluidic hardware being sampled at a 32Hz rate and the thermal hardware being sampled at an 8Hz rate. Run time triggering of the TIM3 interrupts was monitored within the debugging environment to trim the interrupt clock to produce the correct sampling rates (Figure 5.7).

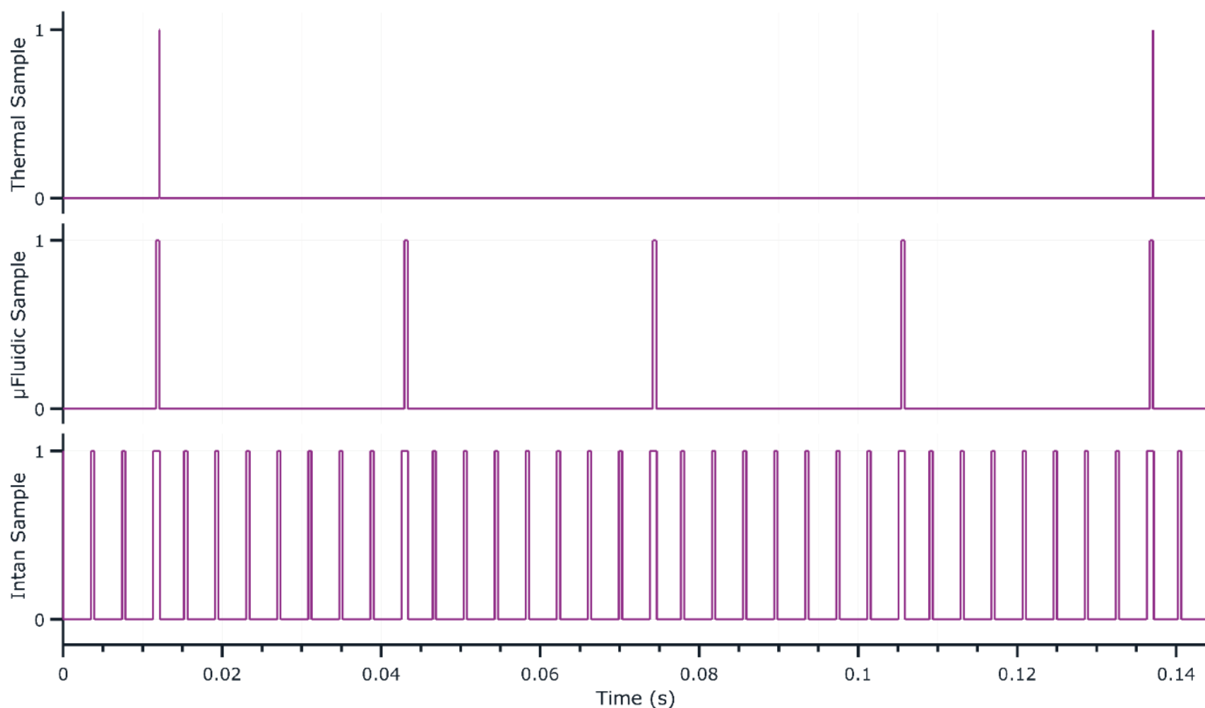


Figure 5.7 Runtime operation of the TIM3 IRQ data sampling interrupt.

EXTI15_10 Interrupt

EXTI15_10 ISR was assigned the highest priority of the user-defined interrupts. This interrupt function centred on providing a safe route for the Interface and Support hardware to shutdown during fault cases or software errors. Whilst in the imposed hardware shutdown state, the error handler would try to locate and resolve the cause before resting back to the main programme flow. Error occurrence is tracked so that if a specific error was to trigger more than three times during a single powered state then the system remains in shutdown mode until the operator conducts a hardware power cycle. This preserves the system state that caused the trigger conditions to aid debugging and prevents damage to the experimental model.

Triggers for the EXTI15_10 ISR could originate from external sources or from systems within the firmware. External triggers stem from dedicated fault GPIO pins that exist on the DRV592 TEC driver and the PAC1944 power monitor. The GPIO pins these signals are routed to on the microcontroller are mapped, by the software, to trigger the ISR call automatically on specified signal edge conditions. These allow faults in the TEC or the driving hardware to be near instantly handled due to response time being independent of the sensor polling rates. On top of the external triggers, the firmware is able to trigger the error handling ISR call by monitoring fault conditions sent within sensor data packets. This is specific to the thermocouple data packets which, along with the temperature data, returns the thermocouple sensor status. This data packet contains a flag to signal the general fault status with subsequent flags specifying the type of fault e.g. open-circuit, short to GND, etc. Being contained within the sensor data packet, the response time to the thermocouple faults can be up to 0.125s (1/8s) given by the poling frequency.

5.6.3 Data Output

Over the course of this research project, data collection from the hardware is achieved via USART. All streamed data was output directly after the sensor was sampled from a hardware system (thermal system, neural system, and microfluidic system). The general structure of the data output flow first consists of the data collection for that system (Figure 5.8A). This data was stored in separate data structs for each system in numeric data types. After data collection, the specified data that was to be sent out are selected and converted into UTF-8 char strings. These strings are pushed into a FIFO-type DMA buffer in the intended data output order. With the conversions buffered, the DMA controller is activated and the data starts to automatically load into the UART output register one byte at a time. This loading was independent of the main firmware flow as to not consume processing time with manual data output loading.

All output data frames were formatted in the same frame structure (Figure 5.8B). This provides the host PC with a common frame standard to decompose that is designed to reduce missing data point occurrences. Each hardware system was allocated a data marker that dictates the frames data system relation. The necessity of these markers stems from the variable sampling rate that each system has. Neural data is marked with an 'I', thermal data is marked with a 'T', and μFluidic data is marked with an 'F'.

In addition, two other markers are used for indicating command responses, 'C', and system error code outputs, 'Error' or 'E'. These markers always take the first position in the data frame and are followed by a space ('\s'). The frame's data then follows. '\s' characters are interspaced between the data are to delimit the frame's data. A data frame was ended with a carriage return character ('\n') which was used to delimit the whole frame as well as providing the host PC with built in data frame formatting if the stream is saved using its raw state.

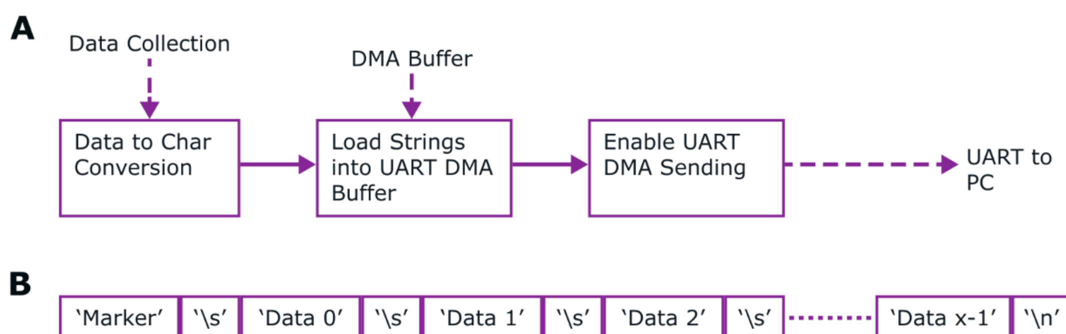


Figure 5.8 Interface Support Hardware data output structure.
A. Programme flow of data conversion and output using the UART2 peripheral in combination with the DMA controller to send data independently from the core processor. **B.** General data frame structure that all UART output adheres to.

UART Data Output

Whilst using the UART does provide the simplest solution to data transfer between the Interface Support hardware and the host PC, its implementation imposes limits on the data output rates. The data output setup requires all sampled data to be sent before the next sampling trigger – restricting the maximum frame size to the smallest sampling time period. The smallest sample period is 3.906ms (256Hz) of the neural system. Hardware restrictions limit the UART baud rate to 115200. Given that the UART frame for each char consists of 10bits, a maximum of 45 characters can be sent out between neural data samples. This enforces restrictions on the quantity of outputted data points and each point's significate figure value.

For the *In Vitro* testing, this data bandwidth restriction did not hamper data collection during experiments. *In Vitro* experiments would be designed to isolate select systems for thorough testing thus only that systems data would be outputted. However, upon moving to *In Vivo* experiments, this posed an issue. Ideally all system data points would be collected during the cooling runs to allow a complete experimental picture. A restricted data set had to be formulated to ensure the maximum data was streamed to compact to just the critical modulation data (Table 5.2).

Table 5.2 UART data frame content output during In Vivo experiments.

Data Marker	Data Order	Base Type	UTF-8 Length
I	Channel A	uint16_t	6 Bytes
	Channel B	uint16_t	6 Bytes
	Seizure Confidence	float	3 Bytes
T	Cold Side Temperature	float	5 Bytes
	Hot Side Temperature	float	5 Bytes
	TEC Currrent	uint16_t	5 Bytes
	PID Proportional Value	uint16_t	4 Bytes
	PID Integral Value	uint16_t	6 Bytes
	PID Differential Value	uint16_t	3 Bytes
	TEC PWM Magnitude	uint8_t	3 Bytes

Data Output Issue Solutions

Solutions to overcome this data streaming limitation were formulated once other UART optimisation routes had been expended. One would be to switch out the UART serial protocol for USB communication. The STM32U585 contains the peripheral hardware to natively support USB Full Speed (FS). This FS setup could provide a data transfer of up to 12 Megabits per second (Mbps). Allowing data packets to be either streamed in real-time or be sent over in larger buffered packets without creating data output lag.

Another solution would have been to store the complete data set in local memory but to still have a reduced data stream out over UART. An SD card linked to the electronic hardware could provide enough storage space to guarantee data log integrity without concern for filling to capacity during long-term study monitoring. It would give rise to the ability to retain system data whilst the Interface is decoupled from a host PC and the potential for offline system settings updates via files pre-loaded onto the SD card.

With the introduction of the Interface Support hardware, the opportunity for hardware implementation of these two alternate data retention solutions arose. Thus, the version 1.0.0 of the Interface Support hardware supports the mounting of a microSD card and a hardware connection to the microcontrollers USB peripheral. However, time limitations within the project meant that the software aspect of these systems was not developed. Future progression of this system would require these to be fully implemented to provide a clinically capable system.

5.6.4 Firmware Commands & Value Configuration

Being able to modify Interface Support firmware or hardware behaviour without having to recompile and re-flash the microcontroller every time is an import function to have during experiments. As the host PC has the UART connection to the Interface Support PCB, the means for two-way communication is already supported. The only requirement is a structure to handle command verification and sorting. This formed into the USART input processing function collection.

A peripheral independent software implementation, the command ingest function provides the means to change the system states in a user-friendly way through a set of UTF-8 character commands. The commands were standardised to fit a set pattern for the command ingest function to sort through. With this command pattern are two sub-sets: the value command, and the toggle command. Value command consisted of a two-letter identifier, a colon delimiter, and a string of number characters that defines a value. This is terminated by the carriage return character '\n'. For example, to set a differential gain to 38, one would send:

kd:38\n

These types of commands are for configuring response behaviours related to the focal cooling Modality such as the PID Controller gain values or piezoelectric air pump power. A data deposition function handles the saving of these values. Each command has its value check against a set upper and lower limit in place to restrict out of bounds behaviour. If they fall out of its limits, the data deposition function sets the value to the closest limit value and sends out an 'data invalid' message to warn the user. If the value falls within bounds, the value gets saved in the relevant variable and a confirmation echo message was sent - though the echo replaces the colon with a '\s' character.

The toggle command follows near the same send format as the value command with a two-letter identifier at the beginning. But that was all that was required – other than the terminating '\n' character. As these commands were only needing to toggling a bit value from its current state. For example, if you wish to toggle the piezoelectric pump to be turned on, the command that would be sent is:

ft\n

Table 5.3 Commands available for configuration of the Interface Support firmware.
Red commands indicate partial or non-function at this point in time.

Command Name	Identifier	Value Range	Command Description
DUTY_CYCLE	dc	0 to 255	Manually control the TEC Driver's duty cycle input
PROPORTIONAL_GAIN	kp	0 to 100	Set the PID controller's proportional gain value
INTEGRAL_GAIN	ki	-6 to 6	Set the PID controller's integral gain value
DERIVATIVE_GAIN	kd	-100 to 100	Set the PID controller's derivative gain value
TEMPERATURE_REFERENCE	tr	10 to 37	Set the PID controller's set point value
SPM_041_POWER	fp	0 to 1400	Set the piezoelectric pump actuation power
CONTROL_TOGGLE	ct	1/0	Toggle the Interface's Focal Cooling modality
HEAT_DISS_TOGGLE	ft	1/0	Toggle the Microfluidic Coolant Pump state
FLOW_METER_TOGGLE	fm	1/0	Toggle the SLF3S-1300B data sampling
DATA_OUT_TOGGLE	do	1/0	Toggle system data stream output to host PC
INTAN_RESET	ir	1/0	Reset the amplifiers on the RHD2216
SIGNAL_SYNC_PULSE	ss	1/0	Send sync pulse signal to Neuronexus hardware
VALVE_STARTUP	vs	1/0	Active the valve startup finction
VALVE_TOGGLE	vt	1/0	Toggle the valve aire flow direction state
INTAN_IMPEDANCE	ii	1/0	In situ RHD2216 electrode impedence measurement
REPORT	rp	1/0	Print a system configurable values report

Toggle commands have an active effect on hardware function enabling the user to switch hardware on or off or have the firmware run through pre-defined functions. These commands don’t require any input value they switch a binary state. Upon successful implementation of the commanded toggle, an echo of the toggle characters with a toggle state value was sent to the host PC. For the piezoelectric air pump example, the echo would be either:

ft 1 ***(if the pump was turned on)***

ft 0 ***(if the pump was turned off)***

A list of all available commands is provided in Table 5.3. To ensure proper command reception and related command function call was achieved, every valid input command is hashed – using the djb2 hashing method. Hashing converts the UTF-8 characters into unique 16bit numbers. These numbers provide for an easier method for writing a switch statement to match a command to the correct function to call. Removing the need to perform character string matching whilst also enabling a simple means to add in a new command. New commands were added by selecting two arbitrary characters (ensuring they haven’t been used before), feeding through the hash function in isolation, and then add the hashed number output to the table in the command ingest fuction header file.

5.7 Interface Support LabVIEW UI

A suite of LabVIEW VIs was written to allow the online visualisation of the streamed Interface experimental data and to handle data storage formatting. The LabVIEW VIs consist of two key elements – the front panel and the block diagram. The block diagram is the VIs source code window which contains the programme written in G. The front panel is the VIs user interface window contains the numeric and symbolic interface objects for system control and data visualisation.

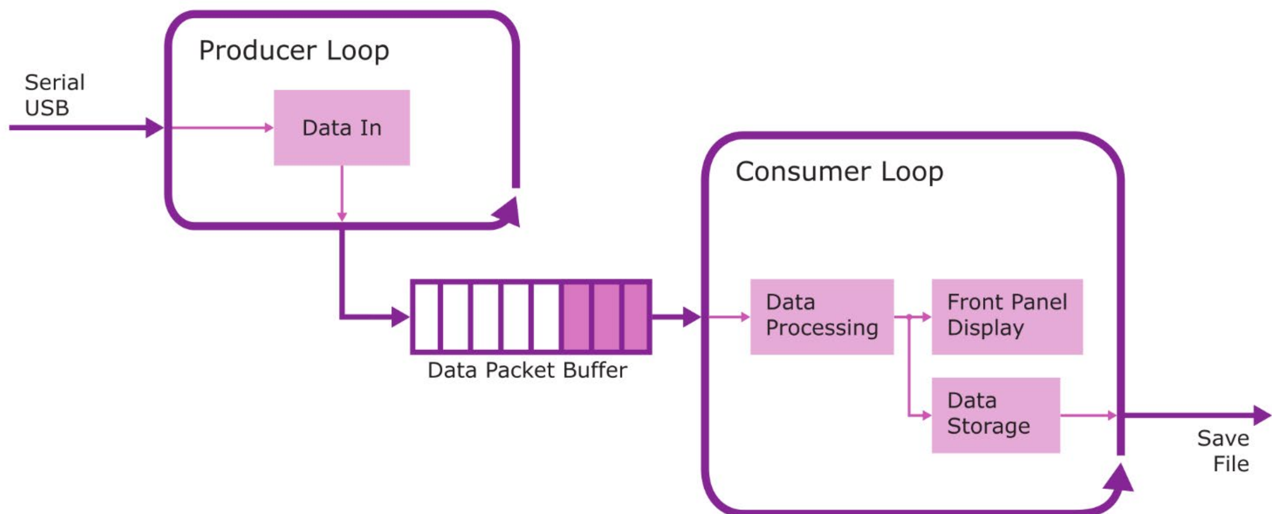


Figure 5.9 LabVIEW programme producer and consumer loop architecture.
Used in all VIs written during this project, this structure separates data collection timings from its display.

Over the course of this project, VIs were first developed to test each of the Interface's function as individual systems, such as for the thermal modality and neural recording modality. These VIs were then integrated together to enable total control over the Interface during *In Vitro* and *In Vivo* experimentation. With a constant flow of data out of the Interface Support hardware, these VIs were constructed using a producer-consumer architecture. This architecture consists of two while loops running in parallel (Figure 5.9).

The producer loop's sole purpose was to read the incoming data stream and load it into a FIFO data buffer. The producer loop iterates as fast as the data send rate of the connected hardware. On the other hand, the consumer loop handled all of the data processing, hardware command sending, data display, and storage during programme run-time. The consumer's refresh rate was normally equal to or slower than the producer loop rate. Having the producer and the consumer processes separate ensures that the potential heavier computational load of the consumer processes does not affect the timings of the data capture. If the data capture were to be delayed beyond the hardware data send rate, then those data packets would potentially lost. Instead, a slow consumer loop results in the producer just increasing the amount of data stored in the buffer for processing.

5.7.1 Interface *In Vivo* VI

For an example of a VI deployed during experiments, the *In Vivo* VI will be explored. The purpose of this VI was to provide continuous monitoring of the thermal and neural recording modalities. It did so whilst simultaneously allowing command of cooling runs to take place and the ability to alter TEC controller properties.

Front Panel

The front panel serves as the primary user interface to the view and control the hardware whilst performing experiments. It is designed to display all modality information streamed out of the Interface Support hardware during run-time (Figure 5.10). Before running the VI, a data file name was inputted, and hardware communication (COM) ports were selected – (1). Once the VI was started, streamed data was ingested and displayed on the various graphs (also called waveform charts) across the panel – (3, 4, 5). These graphs are set to display a 60s data period that was continuously updated. Control of the Interface cooling runs was achieved through a set of run-time editable controls at (2). These controls are split into groups that allow the adjustment of TEC controller gains, set the cooling run timings, and indicate the current cooling run state and time. These controls make use of the firmware command system to enable online and repeatable Interface control.

1 Hardware and File Input 2 Cooling Run Control 3 TEC Temperature Graph
4 Intan ChA and ChB Graph 5 TEC Controller Graphs

Figure 5.10 Front Panel of the In Vivo Experimental VI.
The live graphs provide display all Interface data streamed out. Virtual buttons allow for control over Interface cooling runs. Notable elements of the VI are numbered and with the key under the image.

Block Diagram Processes

Split into three sequential sections, the block diagram for the *In Vivo* begins by running through a single instance of programme initialisation. Here the hardware COM port connection is opened, and the connection settings configured using the VISA serial functions. The VI resets the TEC PID controller gains and temperature setpoint back to the default values. This sets the Interface hardware ready to begin a cooling run process. In parallel to the hardware setup, the folder and experimental save files are created, named, and have column titles added to. The VI then begin the main process loop.

The main loop consists of the producer-consumer architecture, as previously described. In the producer loop there is the VISA read function to capture the data output stream from the Interface hardware, and the enqueue element function which adds the captured data to a queue. This queue is a FIFO buffer that stores data in order of its reception. It is this buffer functionality that allows the producer and consumer loops to share data whilst running independently in parallel. The producer loop is free to iterate at the ≥256Hz rate required whilst the consumer loop iterates at a rate equal to or less than the producer.

The consumer loop contains code to process the data packets. As described in Section 5.6.3, the neural recording data and the thermal data was sent out in two separate data packets that each start with a unique character marker. The markers were used to construct a state-machine to stored modality specific data into the correct processing stream.

With the two data packet type being sent out of the Interface hardware at different rates, the state-machine prevents the packet processing from causing display timings issues. A third state was added for handling the confirmation echo response to commands being acknowledged by the hardware. This command state performs a parity check between the expected command echo and received echo. If parity is false then the state resends the original command, else it accepts the confirmation and allows for a new command to be sent.

During experiments, repeated Interface cooling runs needed to take place. A cooling run specific state-machine was built to enable this functionality. This cooling run state-machine would control the behavioural order of the Interface hardware based on programmed time frames by the user. The frames would dictate the length of the pre-cooling delay, cooling length, and pump off delay. The state-machine would sequentially step through each period as cooling run progresses, altering the hardware state as it did so. The default state was set state 0. In this state all thermal modality hardware was deactivated and, if any active hardware is detected upon entering this state, then it would be toggle to its off state. Activation of a cooling run was achieved through the 'Cooling?' button on the VI's front panel.

Table 5.4 Dataset output format for the Thermal Modulation data stream.

Thermal Modulation Dataset	
Column No.	Data
1	Time (s)
2	TEC Cold-side (°C)
3	TEC Hot-side (°C)
4	TEC Current (A)
5	Controller Error (°C)
6	Proportional Magnitude
7	Integral Magnitude
8	Differential Magnitude
9	PID Summation (%)
10	PWM Duty Cycle
11	Cooling State
12	Null Data
13	Temperature Set Point (°C)

Stepping to state 1, the inputted cooling run periods are used to calculate each states timings and when each subsequent state should activate. The timing data is stored, and the next state was entered. State 3 was the pre-cooling delay state where the state-machine waits in idling from 0s to the pre-cooling delay period end. Once this time is reached, all thermal modality hardware is commanded to activate and State 7 was entered. This state ensures that the cooling stays remains active until the (pre-cooling delay + cooling length) period had elapsed. At this point, the Interface hardware was commanded to disable the TEC and the µFluidic hardware remains active. Retaining a post-cooling coolant flow over the TEC hot-side removes any remaining heat from the system and prevents it from being dumped back into the neural tissue.

State 9 was entered post-cooling and waits for the pump off delay period to elapse – (pre-cooling delay + cooling length + pump off delay). At the end of the period, the µFluidic hardware would be commanded to deactivate and the final state in the sequence is entered – State 17. This state resets the stored time values to zero and rests the 'Cooling?' front panel button - informing the user that the cooling run had ended. If issues of instability in the cooling run occur, or the user wishes to end it early, then the user only needs to manually reset the 'Cooling?' button to cause the deactivation of the cooling hardware.

Experimental Data Saving

Whilst the VI is ingesting and displaying the hardware data stream, it is also simultaneously buffering and saving it. The VI was designed to automatically save the VI's buffered data every 4s. The data is appended to a .txt file created during the initialisation of the VI. Hard-coded folder paths are used to provide a standard filing system for logging experimental data depending on experiment type undertaken (*In Vivo* vs *In Vitro*) and the experiments purpose (debugging or experiment).

Table 5.5 Dataset output format for the neural recording data stream.

Neural Recording Dataset	
Column No.	Data
1	Time (s)
2	Channel A (mV)
3	Channel B (mV)
4	Cooling State

Each time the VI is ran, three saved data files are produced. One contains the neural recording data of the two electrode channels and the seizure detection states (when enabled). The second contains the TEC systems data which includes the TEC temperature data and the TEC controller information. Lastly, a VI system and state file was produced that contains timing and consumer loop data to help with identifying run-time issues in the VI. These can be hard to debug when only viewing a single time point of the VI's values.

All three of these files are date and time stamped to when the set is created. The data array that each save file contains was standardised to a set column arrangement. Detailed in Table 5.4 are the thermal columns 1 to 13 data order, and Table 5.5 details the neural recording columns 1 to 4 data order. Both files generally contain the sample time point, the streamed Interface hardware data, and then the cooling runs status. Other data columns are added to the save file depending on the individual requirements of the experiments. Having at least a partially standardise data array layout provides scope for the writing of reusable post-experiment data processing scripts.

5.8 Microfluidic Loop Monitoring

Implementation of the microfluidic system hardware, that uses the piezoelectric air pump, required the development of specialist functions to enable operation during run-time. The sew-saw flow of the piezoelectric pump setup created two new and unique system conditions to handle:

1. The unknown coolant levels of the reservoirs at startup.
2. Reversing the coolant flow direction when the draining reservoir is empty.

The aim was to develop handlers for these conditions utilising only the existing hardware sensing solutions of the microfluidic system. Actuation within this system is attained by the air flow output of the SPM-041 module and the two 3-way air valves. System state can be monitored through the air pressure sensor on the SPM-041 module or the in-line coolant flow sensor. Using this setup, two programme function sets were developed that provide the means to monitor these conditions during active use and automate the handling of them.

5.8.1 Initial Reservoir Levels Detection

On device start-up, the coolant levels in each reservoir was an unknown. This needed to be determined before any cooling actuation takes place. If not, there would be a high risk of dry running the TEC coolant system during a seizure suppression event. Due to the static flow conditions of the system on start-up, sensing for the reservoir coolant level difference would have to be achieve through the monitoring of reservoir pressure levels.

To understand if using air pressure sensing was a viable solution, the microfluidic system was constructed on the benchtop to mirror a full system experimental setup. The microfluidic system was primed with de-ionised water for the coolant fluid. The two reservoirs were asymmetrically filled such that the 'Full' reservoir contained 15ml of fluid and the 'Empty' reservoir contained 3ml of flid. This representative the microfluidic system state at the start of all experiments.

The reservoir pressurisation behaviour was profiled by air flow pulses from the piezoelectric air pump at incrementing power levels. These pulses lasted 2s each. The first pulse would be applied to the 'Full' reservoir and then the next pulse was applied to the 'Empty' reservoir. A 4s reset period was placed between all pulses to equalise the pressure of the two reservoirs using the valves. Pump power was incremented 10% after both reservoirs experienced a pulse.

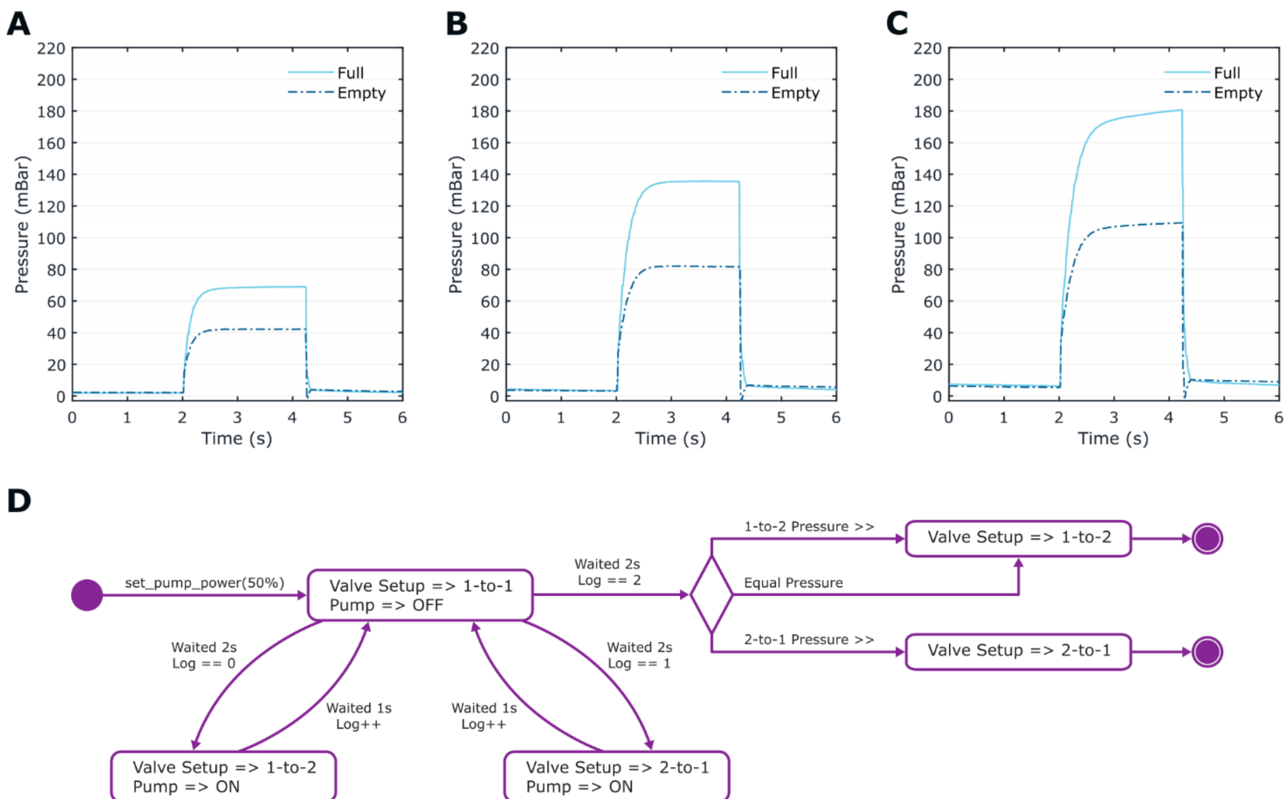


Figure 5.11 Implementation of the reservoir level detection on firmware start-up.
Reservoir pressure level comparison having 20% (**A.**), 50% (**B.**) and 80% (**C.**) pump power applied to two 20ml coolant filled syringes with one at 15ml and the other at 3ml. **D.** The Initial Reservoir Level Detection state machine flow for testing each reservoir and selecting to appropriate valve orientation.

Upon completion of the reservoir testing, the reservoirs pressure data was split into pump power level pairs in MATLAB. The 'Full' and 'Empty' reservoir pressure profiles were aligned and plotted. When the pump was set to 20% power, the aligned pressure profiles of the two asymmetrically filled reservoirs indicate that there is a discernible reservoir pressure difference between the two fill states (Figure 5.11A). This pressure profile difference was replicated when the pump was at higher power levels (Figure 5.11B-C). The relative pressure difference between the two reservoir states at the end of the air pulse is also observed to increase as the pump power is incremented upwards.

The recorded pressure profiles provided evidence of a repeatable reservoir pressurisation behaviour that was dependant on the fill state of each reservoir and was present at a range of power levels. Higher reservoir pressure reading at the end of an air pulse indicated a higher fluid fill state. Conversely, lower reservoir pressure readings indicated a lower fluid fill state. It can also be derived that, with a constant fluid volume in the microfluidic system, the reservoir's measured pressure magnitude is coupled to the fraction of system fluid volume that currently in it.

From these observed pressurisation behaviours, a function was devised to run on firmware start-up (Figure 5.11D). This built upon the code devised to run the reservoir pressure profiling. It first performs a pulse-equalise-pulse pressure application sequence to both reservoirs. It starts by allowing the reservoirs pressure to equalise over to 2s. The software stores the equalised pressure reading from the reservoir before a pressurisation pulse is applied. The pulses are 1s in length with the pump is set to 50% power. A pressure reading is then taken at the end of the pulse period. The difference between the 1st pressure reading and the 2nd pressure reading are compared. The valves are set to apply positive pressure to the reservoir with the highest recorded pressure difference. In the event of an equal pressure result, the valve is set to apply positive pressure to the 1st reservoir sampled.

Empty Reservoir Detection & Switching

Having a non-circulatory coolant flow necessitates the ability to both monitor fluid reservoir levels during active flow and switch flow direction when the draining reservoir becomes empty. From the data gathered on reservoir level detection, it was be determined that the reservoir pressure is coupled to the reservoir fluid level when constant pump power is applied. This behaviour can potential be used to determine when the microfluidic fluid flow direction needs to be reversed.

To verify this hypothesis, the microfluidic system setup up to mirror a full experimental built. The reservoirs were filled with de-ionised water such that one contained 3ml ('Empty') and the other contained 15ml ('Full'). The valves were orientated to have the 'Full' reservoir drain into the 'Empty' reservoir. This would produce a complete pressure profile of the reservoir from the 'Full' state to 'Empty' state. Pump power was set to be constant for an individual run and would be incremented 20% between them. Pressure profiles from the three power levels recorded during the experimental runs are mapped (Figure 5.12A).

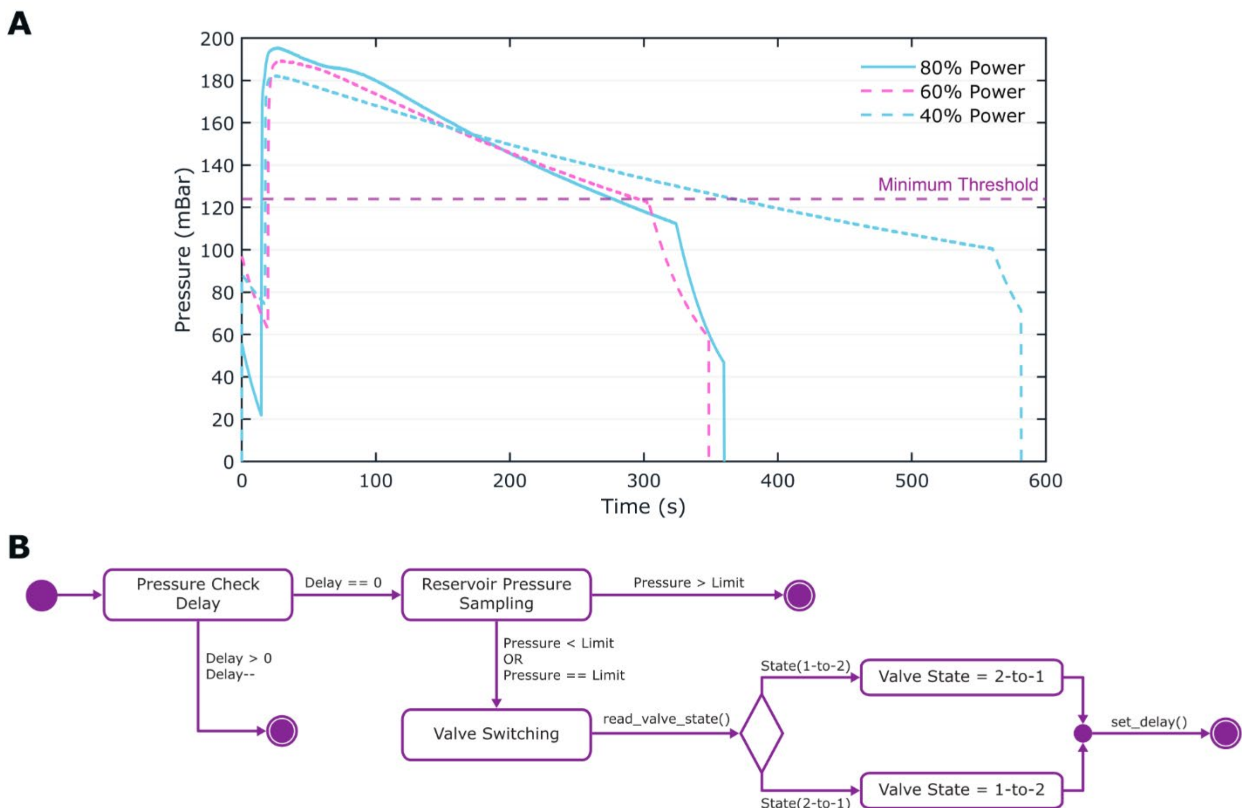


Figure 5.12 Empty reservoir detection for automated reservoir switching.
A. Reservoir pressure recorded during the transition from the reservoir "Full" state to the reservoir "Empty" state at different pump power values. 125mBar is indicated as the minimum threshold switching pressure. **B.** State-machine flow of the empty reservoir detection function activation condition and flow during normal firmware operation.

Variation in the pump power levels is seen to affect the how fast the ‘Full’ reservoir drains through the microfluidic system into the ‘Empty’ reservoir. However, the starting pressure of the ‘Full’ reservoir rises to a similar magnitude across all pump power levels. The transition of a reservoir to being fully drained was marked by a steep, negative change in reservoir pressure. Changing flow direction would need to happen before this steep pressure change occurs. Using the highest pressure reading from the profiles at the empty pressure drop point, the minimum threshold for switching was determined to be 125mBar.

Using this threshold as a basis for detecting the point to switch flow direction, software was developed to implement the functionality (Figure 5.12B). It comprised of two parts. The first is a pressure check delay that samples the pressure measurement from the reservoir but prevents the comparison to the threshold pressure from occurring. This is to account for the initial pressurisation delay period in system when a positive pressure first is applied a reservoir. If a pressure sample is taken before the reservoir pressure reached an ‘operational level’, the comparison may assume that the newly switched to reservoir is empty and try to switch back to the true empty one. The pressure check delay is activated whenever the pump is activated, the flow direction is switched by the software, or the valves are manually switched by the user. The delay is set to wait a length of 1s before pressure comparison can take place.

When the delay reaches 0s, the comparison can freely occur. Valve switching is activated if the measured pressure is equal to or below the threshold. It then goes on to read the current valve state and switches to the opposite configuration. After which the pressure check delay is activated as described beforehand.

5.9 Seizure Detection Algorithm Integration

After system stability had been achieved with the firmware port to the STM32U585, attention shifted to integration of the seizure detection algorithm into the main programme flow. This section will describe the preliminary works undertaken to perform this integration and the indications of successful implementation on the hardware.

Developed by another member of research group[6], the seizure detection algorithm is trained using the recorded neural data from the *In Vivo* experiments. This tailors the detection weightings to the seizure model being employed. This allows for it to be deployed in *future In Vivo* studies and for the detection outputs to be compared against like labelled data.

The end goal for this algorithm is to have it fully integrated into the decision-making process for activation of the Interface's seizure suppression modalities. The algorithm would function independently from external influence and analyse the neural recording in an 'online' capacity. Having the online detection would then close the loop in terms of system control and provide the means to tailor the system response to a patient's epilepsy.

5.9.1 Detection Integration

The implementation of the detection algorithm dictates that it is required to receive a 2 second period of neural recordings – every 2 seconds – to produce an ongoing prediction value of seizure occurrence. To allow this, two pairs of 16-bit int arrays with 512 positions were added as storage buffers. These would store the 2 seconds of neural data needed for detection processing. The buffer pairs, named buffer set 1 & buffer set 2, will flip-flop between filled and processed. A flip-flop regime such as this ensures that no neural data is lost during whilst the algorithm is processing the neural data.

Fill state of each buffer pair is monitored within the main programme flow to check wherever the current active buffer has been filled (Figure 5.13). When it is detected full, the seizure detection function is called and the full buffer's pointer is passed into it. Within this function call, the active buffer state is switched off for the buffer being processed and the previously inactive buffer gets switched in to begin filling. This buffering system functions under the assumption that the seizure detection function is able to complete the processing of a single buffer set within the 2 seconds before the other is filled.

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[6] Dr S. Chen, Unpublished work

In practice, the detection function actually has less than 2 seconds to calculate the seizure confidence value. This down to the placement of the seizure detection function being in the main programme flow rather than contained within an interrupt. It was expected that the large number of calculations would be required to process the 2s buffer set through the algorithm. Placing this process within an interrupt would have a knock effect on the firmware sample times and other update functions. Thus, it must be placed within the main function loop to be called when a buffer full flag is set. Then the sampling interrupt will still be able to maintain its strict timing requirements without issue. All of this results in the seizure detection function allocated runtime being 2s - $T_{Neural_Recording_sampling}$ – $T_{TEC_sampling}$.

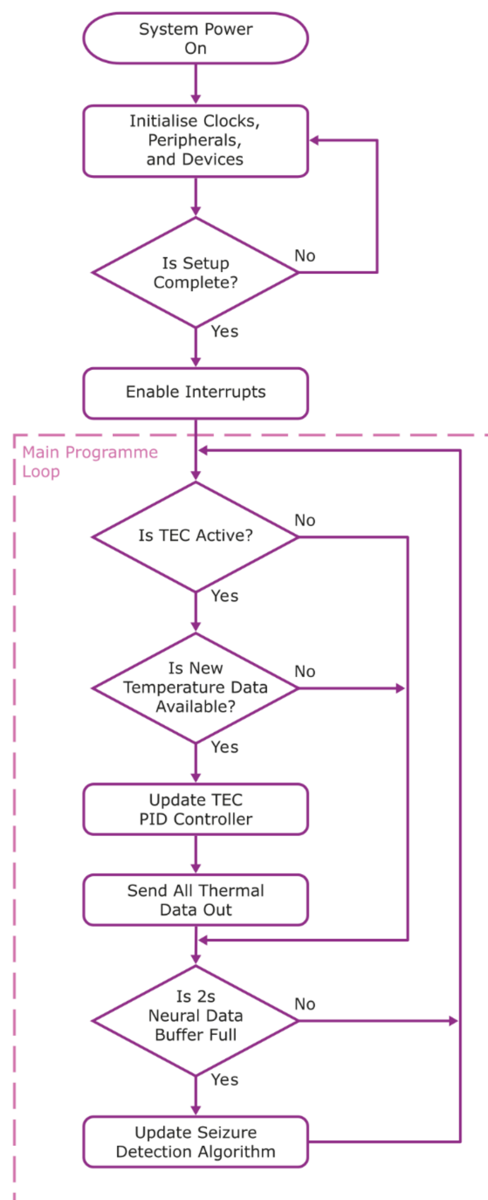

Figure 5.13 Main programme flow with the seizure detection algorithm.
The algorithm state is check at the end of each main loop cycle. It updates its prediction every 2s from the neural recordings of 2s earlier.

To understand if the seizure detection function is capable of being called and produce an output in the allocated runtime, the code was inserted into the firmware for time profiling. Profiling was conducted with the system in its full experimental setup. An Interface v5 was attached to the Interface Support hardware and submerged a vial of Phosphate-buffered solution (PBS). Within this vial was electrode attached to a function generator (MFG-2230M, GW Instek) that is setup to feed *In Vivo* recordings to the Interface. Upon confirmation of setup function, the Interface Support hardware was left to monitor the feed signal whilst the hardware outputted a data stream to the host PC. This stream contained recordings from both electrode channels, markers indicating when the detection function was entered and exited, and the confidence output to confirm function operation.

The markers used to indicate function show the regular calling of the seizure detection algorithm every 2s without any discernible skew in call interval timings (Figure 5.14A). Regular flip-flopping between the two neural recording buffer pairs is observed without any issues. Using these markers, the total time for the detection function to process each buffer pair input was calculated (Figure 5.14B). The detection function runtimes remain stable during the observed period with an average time of 0.0234s (±0.0011s SD) taken to complete the processing of one 2s buffer. This performs well within the computation time slot that it has. It is evident that the seizure detection algorithm is able to be hosted on this system to close the automated seizure suppression loop.

Future progress in this area would be for the full integration of the seizure detection code into the firmware. This would require the implementation of cooling run state machine in the firmware rather than being hosted externally within the LabVIEW VI. Once that requirement is fulfilled then it would be possible to perform real-time seizure detection testing during *In Vivo* studies and profile its seizure detection capability during live seizure event.

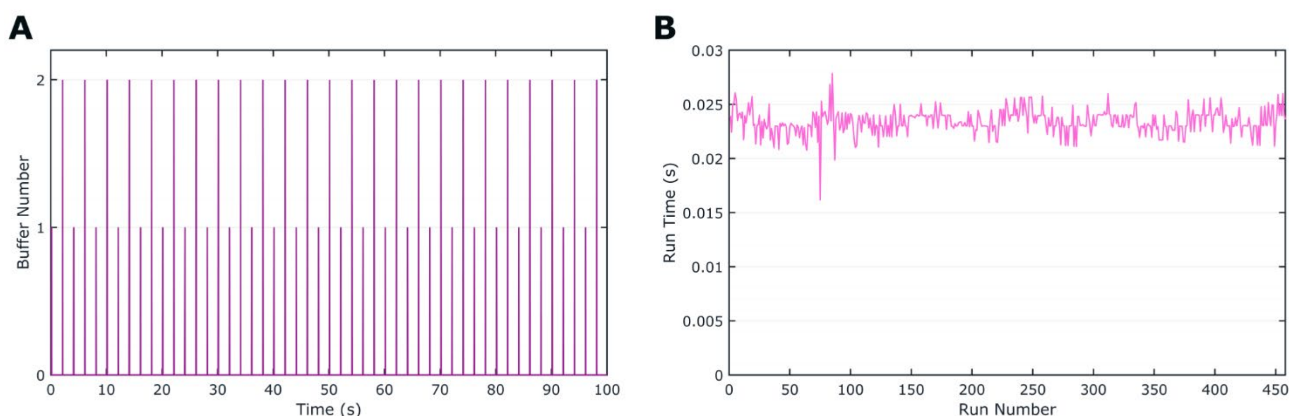

Figure 5.14 Seizure detection algorithm function and timing data.
A. First 100 seconds of the detection function being called – indicated by the spikes. The spiking indicates the entry and exit from the detection function with its magnitude giving the filled buffer number. **B.** Runtimes of the detection function over the course of >450 function calls.

5.10 Summary

The Interface Support hardware's function required a robust firmware to be able to safely control and monitor its systems. Firmware for this project was developed with this statement in mind. Using C99 as the systems programming language, modules for the TEC control, temperature monitoring, neural recording, and microfluidic system control were all incrementally facilitated by the firmware.

Data sampling was controlled through an internal timer-controlled interrupt. This interrupt would be triggered at a 256Hz rate to support the required neural signal acquisition for the seizure detection algorithm. Sampling of the µFluidic system and the TEC thermocouples are sampled during the same interrupt at a 32Hz and 8Hz respectively. Variable rate sampling on one interrupt is enabled by local counts. A combine interrupt design prevented the clashing of multiple sample interrupt requests to maintain accurate sampling periods.

Access to the sampled data was managed through the UART-to-USB bridge between the Interface Support hardware and host PC. A standardised data packet format was devised to efficiently stream the required study data off of the hardware for storage. A command and settings modification protocol was developed for live system control during experimental setups. TEC controller gains could be tuned, individual systems toggle on/off, and cooling runs managed from remote input.

A suite of LabVIEW VIs was written for processing the hardware data stream and acting as a user control interface to affect the Interface Support hardware state. Waveform charts gave live views of system data during studies. Cooling run options could be modified and activated through the interactive GUI the VIs presented.

Automated system actions were introduced with the piezoelectric air pump based microfluidic system. Initial reservoir states could be detected and acted upon by the firmware to optimise the system state after initialisation. Experimental operations could then begin immediately. Continuous reservoirs fluid level monitoring during operation prevented the occurrence of dry running the microfluidic loop. This was achieved through automated reservoir switching when reservoir fluid levels reached too low.

With a mature firmware in place, a study was undertaken to identify if a seizure detection algorithm could be placed in-the-loop. Microcontroller hardware had been selected to provide necessary computational power overhead to, in theory, allow this. After the necessary firmware adaption to support algorithm function, a run time study provided evidence that the seizure detection algorithm could be deployed with the firmware without impeding other firmware operations.

Chapter 6

In Vivo Seizure Suppression

Validation of the Interface systems, specifically the focal cooling and neural recording modality, presented the opportunity for system studies to progress into *In Vivo* epilepsy models. Having both these Interface modalities in place allowed scope to record and suppress epilepsy models activity. The primary aims of conducted *In* Vivo studies was to: verify that the neural recording modality was able to produce clean neural activity data for training and deployment of a seizure detection algorithm; and to demonstrate the focal cooling modalities active modulation of the incited seizure model.

This chapter describes the preliminary work conducted within an *In Vivo* rat model to achieve these research aims. Description of the complete epilepsy model and the *In* Vivo experimental method will be provided. The neural recordings sampled by the Interface Support hardware, via the G-PDMS printed electrodes, will be compared against a commercially available electrode array to authenticate signal content. Recorded neural data from the Interface shall undergo post-processing to determine if the cooling actuation - performed by the Interface - was able to produce a suppressing effect on the seizure models activity. This seizure activity state comparison will be conducted through averaging recorded data across a sets of cooling runs from multiple rat model studies.

All animal work conducted within this chapter was done so under the ethical approval of the University of Sheffield and adhered to the regulations governed by the UK Home Office. Surgeries were performed by two licenced members of the University in accordance with the Animal (Scientific Procedures) Act 1986. This work was made possible through collaboration with Dr J. Berwick's group from the Department of Psychology, University of Sheffield.

6.1 *In Vivo* Epilepsy Model

Before undertaking the *In Vivo* experiments, careful consideration must be taken as to which epilepsy model would be appropriate for what we wish to achieve. For this work, the two models required selection: the seizure model, and the animal model. Study length, hardware size, and the experimental experience of the collaborating scientist all were taken into account when making model selection.

Animal Model

A rat model was chosen as the primary animal model used for the *In Vivo* study into the Interface's seizure suppression capability. This model was chosen predominantly based on the Interface's dimensions. The Interface's structure was sized to potential human implantation due to the complexities of scaling its thermal design – to large sizes and to smaller ones. Its total cooling face covered an area of 9.5 x 9.5mm. With the requirement for an additional commercial neural recording device to be present, exposing the necessary minimum cortex area for device positioning was not achievable with a smaller animal model – such as a mouse. Sizing of an average rat's brain would allow for Interface positioning over the right somatomotor/somatosensory cortex whilst having space to insert a commercial electrode array.

Live rat models and rat brain slices have been used extensively across literature in the understanding of focal brain cooling as a neural modulation technique and in the testing of prototype cooling devices [86, 106, 117]. By performing our *In Vivo* study within a similar model, performance comparisons in recording and suppressing seizure activity will be made easier.

The Seizure Model

4-AP is a proconvulsant that is a well-established model for producing acute epileptiform activity within both *In Vitro* and *In Vivo* models. It has been used as a method to study epileptiform activity evolution, and in the discovery of new anti-epilepsy drugs [153, 154]. Its established use ensures that any suppressing effect achieved can be compared back to the literature.

The 4-AP seizure model is primarily characterised by the inciting of intense and sustained seizure activity when applied to neural tissue [155, 156]. The induced activity can continue for over 1 hour depending on dose concentration and volume applied. Resultant epileptiform activity caused by 4-AP is commonly characterised by spiking and neural signa power increase within the 5-20Hz range [22, 155].

The model's ability to cause sustained seizure activity will allow for sets of cooling runs to be conducted on the same seizure state. The documented characteristics of the 4-AP incited epileptiform activity narrows the window of concern for the neural recording post-processing. The main target frequency bands where the seizure suppressing effects of applied cooling will be most discernible are in the theta (4-7Hz) and alpha bands (8-12Hz).

6.2 Experimental Method

The data presented in this chapter is of the initial investigation into the focal cooling and neural recording modality of the Interface. Seizure suppression studies were performed on three male Hooded Lister rats weighing between 400 and 482g. The rats were housed in a controlled environment (20-22°C) with a 12-hour day/night cycle and had access to food and water ad libitum.

When undertaking the acute *In Vivo* studies, the animal was anaesthetised with urethane at 1.25g/kg i.p – additional 0.25ml doses were applied as required. A homeothermic heating blanket, with rectal temperature monitoring (Harvard Apparatus, UK), maintained the animal's core temperature at ~37°C throughout the surgery and study. All animals were held within a stereotatic frame (Kopf Instruments, USA) for the length of the study. Surgery on the animal exposed the skull over the lateral somatosensory cortex. A dental drill was used to remove an approximate 9 x 10mm section of the rat's skull. Sterile saline was applied as a coolant to the skull bone and exposed cortical surface to prevent thermal damage during drilling. Upon completion of the surgical procedure, the animal and stereotatic frame was moved into a faraday cage for Interface placement, recording system setup, and undertaking of the main study.

Model and Systems Setup

Injection of the 4-AP at the required location the within the somatomotor/somatosensory cortex was enabled by the use of a drug delivery probe (D16, Neuronexus Technologies, USA) that is mounted to a stereotaxic frame arm. The probe's tip is positioned within the cortical tissue near parallel to the cortex surface (Figure 6.1A). Sixteen 177μm^2 microelectrodes are positioned in a line at 100μm intervals from the probes tip. Neural signals from the probe are routed into a Medusa Preamplifier (Tucker-Davis Technologies, USA). Here the signals are pre-amplified and sampled. This preamplifier has an internal battery power source and streams the neural data via optical means to electrically isolation the probe system from mains power.

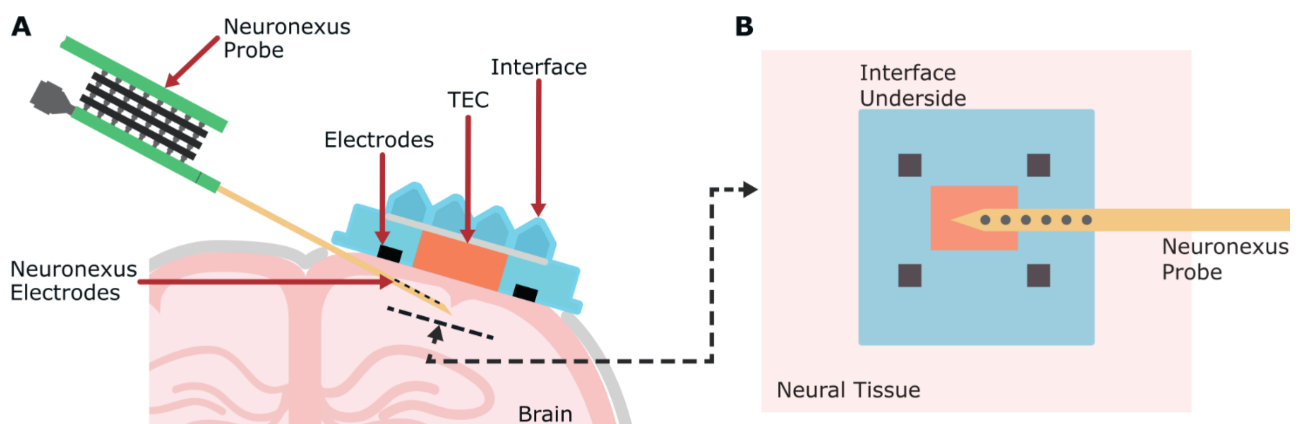

Figure 6.1 Ideal positioning of the Interface and Neuronexus probes.
A. Generalised positioning of the Neuronexus probe array positioning in relation to the Interface TEC and electrodes. Diagram in not to scale. **B.** A bottom-up view of the Neuronexus probe tip placement in relation to the Interface's TEC cold-side – ideal in its centre.

A fibre optic connection is used to link the Medusa Preamplifier to a RZ5 data acquisition (DAQ) system (Tucker-Davis Technologies, USA). This data acquisition system provides support for recording from up to two preamplifiers and formats the incoming optical signals for transfer to a PC. System neural signal acquisition is done so with a 16-bit resolution per channel and at a maximum sampling rate of 24.4kHz.

4-AP injection at the probe tip is controlled via a 4-AP loaded Hamilton syringe mount in a volumetric syringe pump. Before inserting the Neuronexus probe into the rat model's cortex, the drug delivery tube is primed with 4-AP. All air is removed from the probe tube and the small-bore silicone feed lines. Priming ensures the programmed drug volume is correctly dispensed and also prevents air pockets from blocking drug flow or forming in the neural tissue. Once the Neuronexus probe is inserted, the Interface is then positioned on the surface of the exposed cortical site. Neural signal acquisition for the Interface is verified through comparison to Neuronexus probe signals. If signal quality from the Interface electrodes is deemed poor, the Interface is repositioned so that at least one electrode pair displays robust neural signal recordings. Seizure activity is incited within the rat model using a 100μL 4-AP injection. The Neuronexus probe channels are monitored during 4-AP administration for the development of epileptiform activity consistent with the known model activity. If no constant epileptiform activity is achieved after a 5-minute interval post-delivery of the initial does, then a subsequent dose is applied.

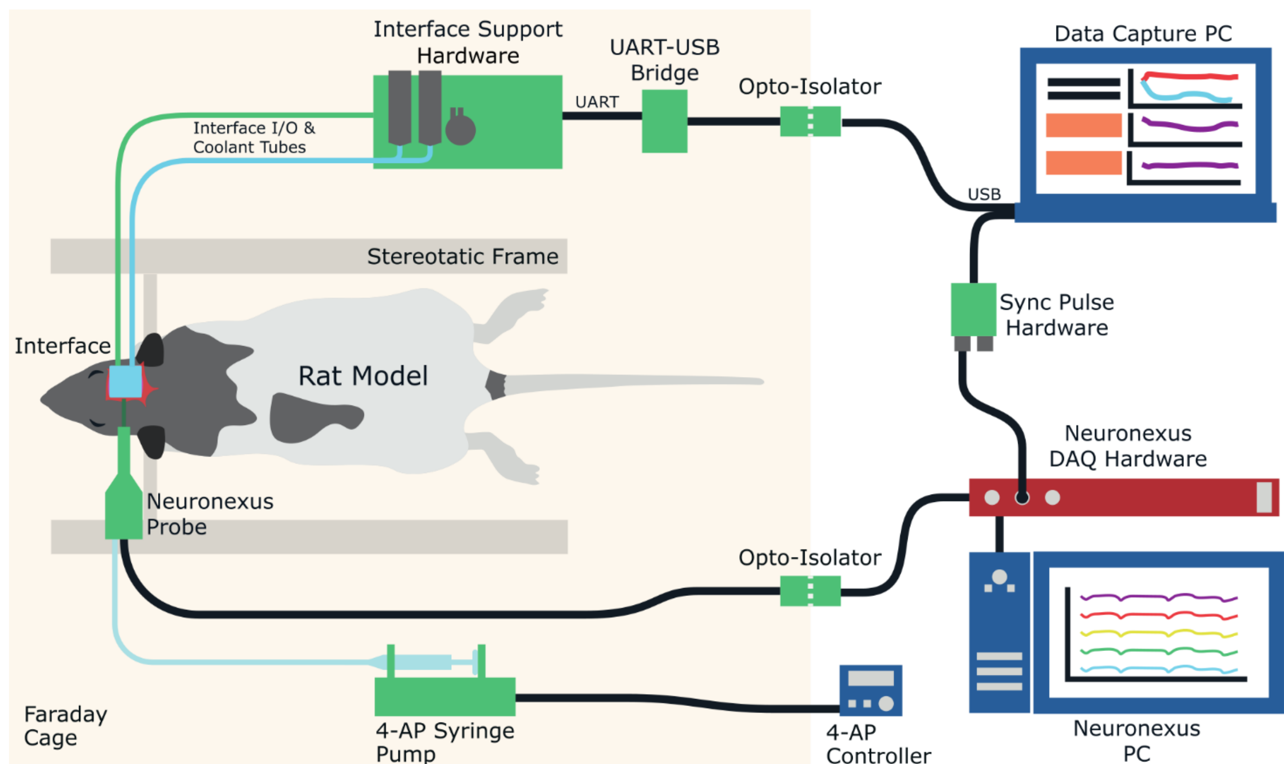

Figure 6.2 Simplified Electronics systems layout for In Vivo studies.
The top flow is the Interface Support hardware setup to control Interface function and allow data streaming to host PC. Neuronexus probe information is routed through an opto-isolated pre-amplifier before being sampled. An Arduino Micro unit drives the neural recording sync pulse to the Neuronexus DAQ for data timing alignment.

The Interface is positioned on the exposed cortical surface so that the centre point of the TEC's cold-side face is aligned to the Neuronexus probe tip (Figure 6.1B). This alignment is managed through an Interface Base Section printed reference layer being positioned on the cortex surface first. TEC and Interface electrode cut outs on the reference layer provide a guide to calculate the stereotactic arm movements required for Neuronexus probe positioning. All four Interface electrodes are intended to be in contact with the cortex surface. Variation between the rat models skull size and shape resulted in some *In Vivo* studies only achieving robust cortical contact with one electrode pair. In these cases, the study proceeds but the data recorded from the unconnected electrode pair is labelled invalid for post-study analysis.

The Interface is secured in place using a custom holding hat which is mounted onto a second stereotactic frame arm for accurate positioning. A pair of small-bore silicone tubes and the Interface-electronics interconnect cable link the Interface to the Interface Support hardware. Power is supplied to the Interface Support hardware using a 7.4V, 2s2p Li-ion battery. The battery pack was selected so that its maximum continuous current draw specification is rated at least 20% above the maximum estimated demand of Interface system for safety. The USART data stream output from the Interface Support hardware is routed into a UART-USB converter. The converter output is connected to a host PC, located external to the faraday cage, via an optically isolated USB cable. De-ionised water is used as the coolant within the Microfluidic system during cooling runs and is maintained at room temperature (Figure 6.2).

Neural Recording Data Sync

During *In Vivo* studies, Neuronexus recordings and Interface data are captured by two independent PCs. Issues in aligning the neural recording data during post-study processing would then be expected. The software for Neuronexus data capture had the functionality to apply stimulation markers to the data set that allowed discreate time points to be recorded. Initial data alignment solution involved manually adding these markers at the start and end of a cooling run. One person counted down to these events whilst another person pressed the button to add the data mark on cue. Manually applying these markers to the data led to human response induced inaccuracies. Thus, the sync pulse hardware was created to remove the human error.

The Neuronexus DAQ hardware had the external facing digital I/O channel from which a programmed response could occur if a trigger pulse is detected. One of these channels had already been programmed to apply a time marker to the Neuronexus data set when triggered by a ≥2.5V pulse. So, to make use of this digital input, an Arduino Micro microcontroller board (Arduino, Italy) was sourced and programmed to supply a 3.3V pulse when sent a command over a serial link.

This Arduino board was connected via USB to the data capture PC for the Interface system. Within the LabVIEW VI - used for the Interfaces *In Vivo* study - it was implemented that a sync pulse command would be sent to the Arduino board by either manually selecting a VI button or automatically during a cooling run event. Automated cooling run sync pulses would be sent whenever a cooling run was initiated; the cooling hardware activated; the TEC was turned off; or when the microfluidic system was turned off. Simultaneous sync pulse marketing of the Interface and Neuronexus data sets provided for greater data alignment accuracy and prevented any sync pulse events from not being recorded.

6.2.1 Cooling Methodology

As state earlier, an aim of the *In Vivo* studies was to provide evidence of the Interface's focal cooling modality successfully suppressing epileptiform activity during a run. Accounting for and reducing the effect of experimental variables model is important so that accurate conclusions can be derived from the recorded data. Controlling experimental variables within biological systems is a difficult endeavour. How the animal model reacts to the 4-AP injection, the neural signal strength of the incited epileptiform activity, and an animal's response to cooling are just some of the model variables that are difficult to account for. In response to this, a robust experimental regime was constructed for the *In Vivo* data collection and processing. Averaging of the Interface's seizure suppressing effect over multiple runs and across multiple rat models will provide control for the variance between models.

The experimental method was built around cooling to a consistent set of four temperature references - 25°C, 20°C, 18°C, and 15°C. Temperature selection was based on the achieved temperature differences within the *In Vitro* studies. 25°C was chosen as the highest temperature based on it being the proposed threshold for when cooling begins to present suppressing effects.

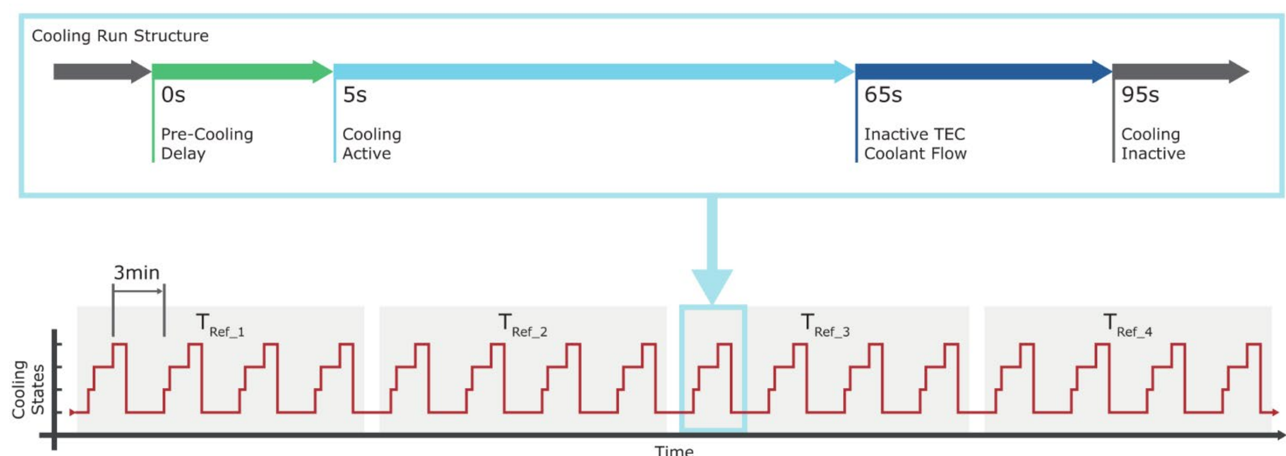

Figure 6.3 In Vivo study cooling run structure.
Cooling run format is standardised through set timings. Four run sets for each temperature are placed in a randomised temperature reference order.

At the start of an *In Vivo* experiment, a random number generator would be used to select the order these temperature reference would be used for cooling. It is noted in literature that focal cooling modulation of seizure activity can induce a neuroprotective effect which could reduce the frequency subsequent seizure events, and/or reduce the seizure intensity (Section 2.1). Temperature order is then randomised to control the neuroprotective effect that the previous cooling temperature depth may have on the next. The randomisation also prevents cooling runs with the same temperature reference being performed at a set point in the induced seizure 'life-cycle'. This removes bias accrued from how the 4-AP model's seizure-like activity can vary over time as the 4-AP concentration in the cortex lessens.

Every cooling run follows a standardise cooling pattern within a set time frame (Figure 6.3). They mirror the cooling run structure used during the *In Vitro* thermal studies. A run comprises of a 5s pre-cooling delay to confirm data integrity; a 60s cooling period where the TEC and microfluidic system are active; and a 30s post-cooling period where the TEC is deactivated but the microfluidic system still has active flow. At the end of this 95s period, all remaining focal cooling systems are deactivated. For each temperature reference, four cooling runs were undertaken. The four cooling runs were performed sequentially. Cooling runs were spaced apart by a 3-minute inter-cooling period in which most Interface systems are in idle except for those related to the neural recording modality. Timing of this inter-cooling period is counted from the end of the active TEC cooling period until the activation of the next cooling run. The equispacing of each run reduces the influence of random transient power variances that could occur within the neural recordings and that runs weren't performed to positively influence the suppressing effect of the focal cooling on seizure activity.

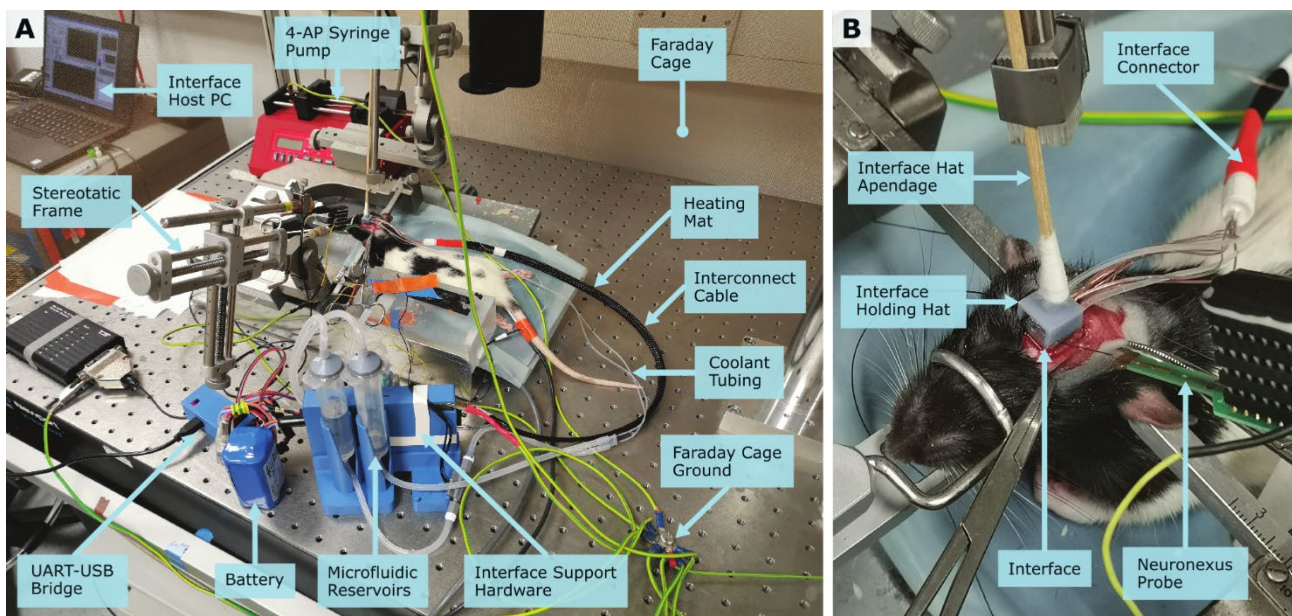

Figure 6.4 In Vivo experimental setup of the Interface Support hardware.
A. The complete experimental setup using the Interface Support hardware alongside the Neuronexus probe. The setup is contained within a faraday cage. The rat model is supported by a stereotaxic frame and heated pad during studies. **B.** Close up of the Interface mounted on the exposed rat model's sensorimotor cortex with the Neuronexus probe implanted underneath.

From this cooling run structure, 16 cooling runs is considered to form a complete set of study data. Accounting the inter-cooling idle periods and a cooling run's length, each study set takes approximately 70 minutes to complete. The *In Vivo* LabVIEW VI provides live monitoring of all Interface systems during a study. It provides the input to activate a cooling run event and to halt it in the event system errors. Two data files are produced from the *In Vivo* VI – the focal cooling data set, and the neural recording data set – due to the sampling rate differences of these systems in the Interface Support firmware. To reduce data loss in the event of a software crash, streamed Interface data is buffered and appended the relevant data set save file every 4s.

6.3 *In Vivo* Performance

The characterisation of the Interface's *In Vivo* function is split to cover three areas. First, simultaneous neural signal recordings from the printed G-PDMS electrodes and the Neuronexus probe will be compared to verify the neural recording modality. Second, the Interface's *In Vivo* focal cooling performance will be presented. Third, averaged neural signal data will be compared to discover if the Interface was able to elicit the suppression of seizure activity through focal cooling modulation.

The *In Vivo* results to be presented were recorded in controlled environmental conditions through performing the studies in the same location and with identical hardware (Figure 6.4A-B). All experiments were conducted in a faraday cage where the hardware layout was replicated to maintain consistent neural signal recording noise conditions across studies. The faraday cage remained closed during the cooling run actuation and was only open during pre-study setup and post-study cleaning. Hardware data link cables were routed through a built-in slot in the faraday cage structure. The Interface Support hardware command system enabled the control of Interface operation without having to enter cage.

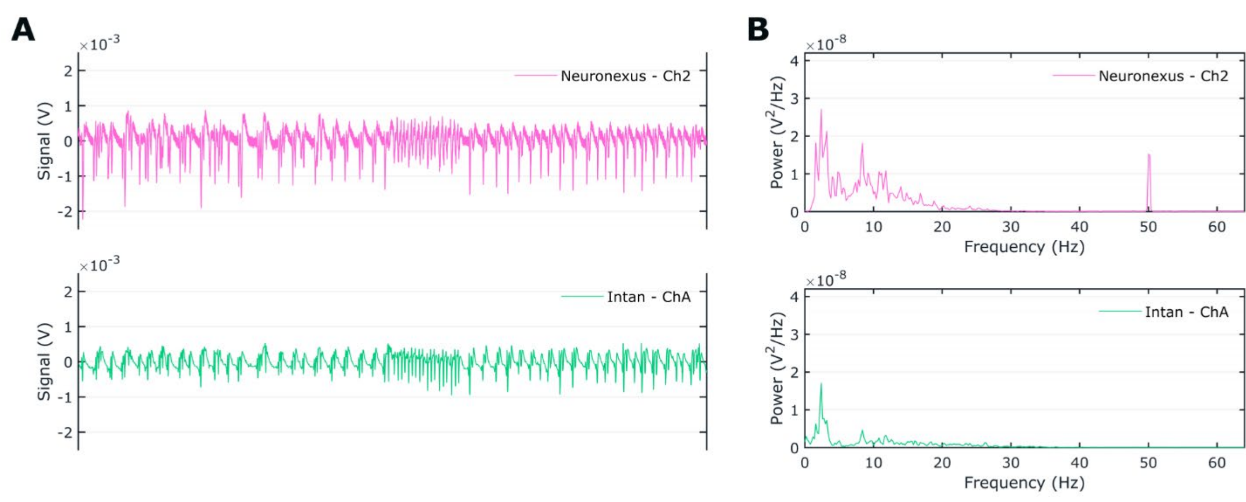

Figure 6.5 Neural recording electrode comparison.
A. Aligned time domain neural signals recorded simultaneously through the G-PDMS electrodes of the Interface and a single electrode of the Neuronexus probe array (Neuronexus, USA). **B.** Power spectral density of each electrode's neural recordings.

6.3.1 Electrode Recording

To verify the neural signal modality of the Interface, the neural signal recordings generated through the printed G-PDMS electrodes were compared to the Neuronexus neural signal recording. The time domain features present and the frequency content of both signals were used to perform it. Sync pulse markers were used to align the neural signal recordings to ensure time parity across all recorded signal features.

A 20 second segment of the aligned Interface and Neuronexus probe recordings provide a snap shoot comparison example (Figure 6.5A). Visual inspection of these two recordings in the time domain demonstrates that the both systems were able to similar neural activity. General seizure spiking is observed with each device independently recording the period of rapid spiking in the neural activity simultaneously. Mirroring of these time domain features within the Neuronexus recordings by the Interface neural recording modality provides strong indication that the Interface system is sensing neural activity and that the content of this sensed activity is independently verified.

With the differing locations of each system's electrodes – Interface electrodes on the cortex surface vs the Neuronexus probe's intra-cortical array – does result in differences between the two recorded signals. The Interface's G-PDMS electrode recordings suffer from greater attenuation when compared to the Neuronexus signal strength. This observation is validated through calculating the Power Spectral Density (PSD) of the presented recording slices (Figure 6.5B). PSD normalise a signals amplitude by the frequency resolution it was sampled at. This means that a broadband signal that was recorded by two systems at different sampling rates can be compared together. It was an applicable method here as the Interface recordings were sampled at a 256Hz rate and the Neuronexus probe recordings were sampled at a 1.526kHz rate. The Interface recordings total normalised signal power between 0 and 30Hz present an ~65% attenuation when compared to that of the Neuronexus probe. This attenuation can be attributed to the location from which the two neural recording systems detecting these electrophysiological signals. The Interface electrode array design fits within the electrocorticography device class. As such, the Interface electrodes are located epidural and means that local field potentials (LFP) must travel through the CSF and the dura it is detected by the electrodes [157]. This epidural, rather than subdural, placement has been reported to produce significate attenuation in neural signal amplitude [158]. On the other hand, the Neuronexus probe electrodes are performing intracortical recording. Its electrode sites are then in direct connect with the neural tissue providing a shorter path signal path to the LFPs.

However, this comparative attenuation of the recorded signals does not detract from fact that near identical signal dynamics are present in both systems recordings. As such, the G-PDMS electrodes are determined to be viable for recording the neural data and monitoring seizure suppression events going forward.

6.3.2 Focal Cooling Ability

Placed epidurally on the animal models cortex, the Interface cooling face has direct and constant contact with the neural tissue during the *In Vivo* studies. As such, the cooling runs were able to be performed with confidence that a thermal mass was loading the cold-side. It had been observed that the nominal cortex surface temperature was ~33.5°C once the Interface had reached thermal equilibrium cortex placement. This was found across all rat models used. Once the Interface had thermal equilibrium the cooling actuation of the neural tissue was approved to commence. Described before, four temperature set points were chosen to cool to – 25°C, 20°C, 18°C, 15°C.

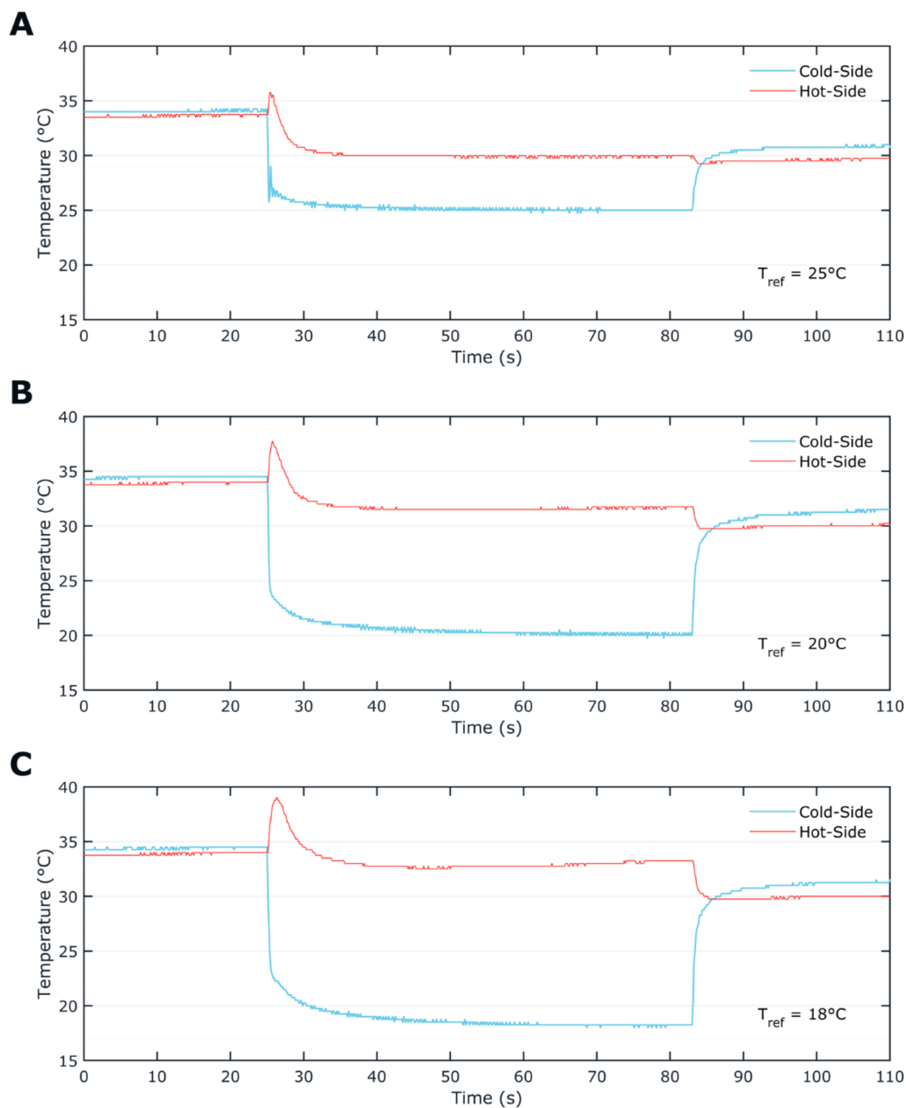

Figure 6.6 Interface cooling profiles recorded during the In Vivo studies.
Single representative cooling profiles of the 25C° temperature set point (**A.**), 20°C temperature set point (**B.**), and 18°C temperature set point (**C.**).

During the cooling runs, the Interface would be able to perform cooling to 25°C, 20°, and 18°C with ease (Figure 6.6A-C). Temperature profiles of the TEC hot-side and cold-side display consistent cooling profiles across the vary cooling depths. Rapid focal cooling achieved down to the 18°C run. The TEC hot-side is observed not breach 40°C during the TEC start-up temperature spike and commonly had its temperature reduced to below nominal cortex surface temperature within the steady-state cooling period.

However, during cooling runs it was found that a commanded 15°C temperature reference was not consistently achievable by the Interface system. It was likely due to a combination of contributing reasons. The hypothesised main culprit was that the heat dissipation system was unable to effectively handle the initial hot-side temperature spike the 15°C cooling runs produced which directly led to system instability. The other potential cause was suggested to be the coolant fluid temperature. In all previous experiments the coolant was kept at a room temperature of ~20°C. Whereas, the *In Vivo* study room temperature would sit between ~25 to 27°C resulting in a warmer coolant fluid over time. This heating of the coolant over time correlates with the Interface's ability of achieving the 15°C target reducing as the *In Vivo* experiments progressed.

Two solutions to allow more consistent 15°C runs are: changing the coolant from de-ionised water one that presents a great thermal conductivity, or to have the microfluidic system pump pressurise the reservoirs and initiate coolant flow just prior to TEC activation. Currently the microfluidic system actives simultaneously with the activation of the TEC. Whilst the TEC begins to instantly pump heat from its cold-side, there is a startup lag with the microfluidic flow in the order of 500-1000ms. The static water is unable to store the large amount of pumped heat that is generated at the start of cooling and thus the instability occurs. These inconsistent performances have meant that there was not enough 15°C cooling runs to be able to average over. As such, the 15°C data is omitted from data presented.

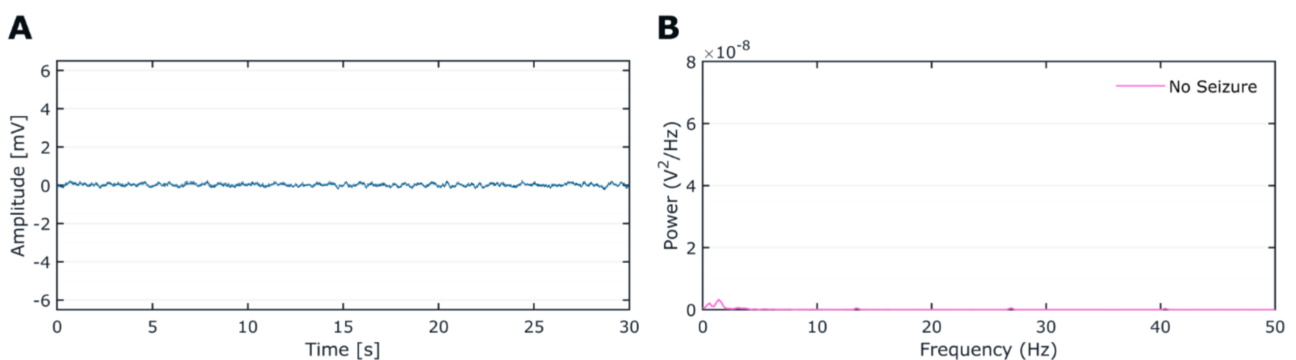

Figure 6.7 Baseline neural activity in the rat model during no seizure.
A. Representative neural activity of the rat model prior to the injection of 4AP. Recorded through the Interface electrode channel A over a 30s period. **B.** PSD of the representative neural activity being the baseline 'healthy' neural activity level for comparison.

6.4 Suppression of Seizure Activity

In order to determine wherever the focal cooling performed had a modulating effect on the incited seizure activity, the neural data first had to be processed before conclusions could be drawn. First, each experiments neural recordings were checked for signal quality. If the signal information the contained in recordings from Channel A or Channel B did not line up with that from the Neuronexus probe, then that Channels data was discounted. From the three animals, each one had its Channel B recording omitted due to low/no signal being recorded on it. All neural data then is derived from electrode Channel A of the Interface.

Twelve cooling runs per temperature reference was deemed to contain valid neural data for processing. Each of these cooling runs had the first 30 seconds before focal cooling was active, and the last 30 seconds of the focal cooling period sliced into isolated recordings.

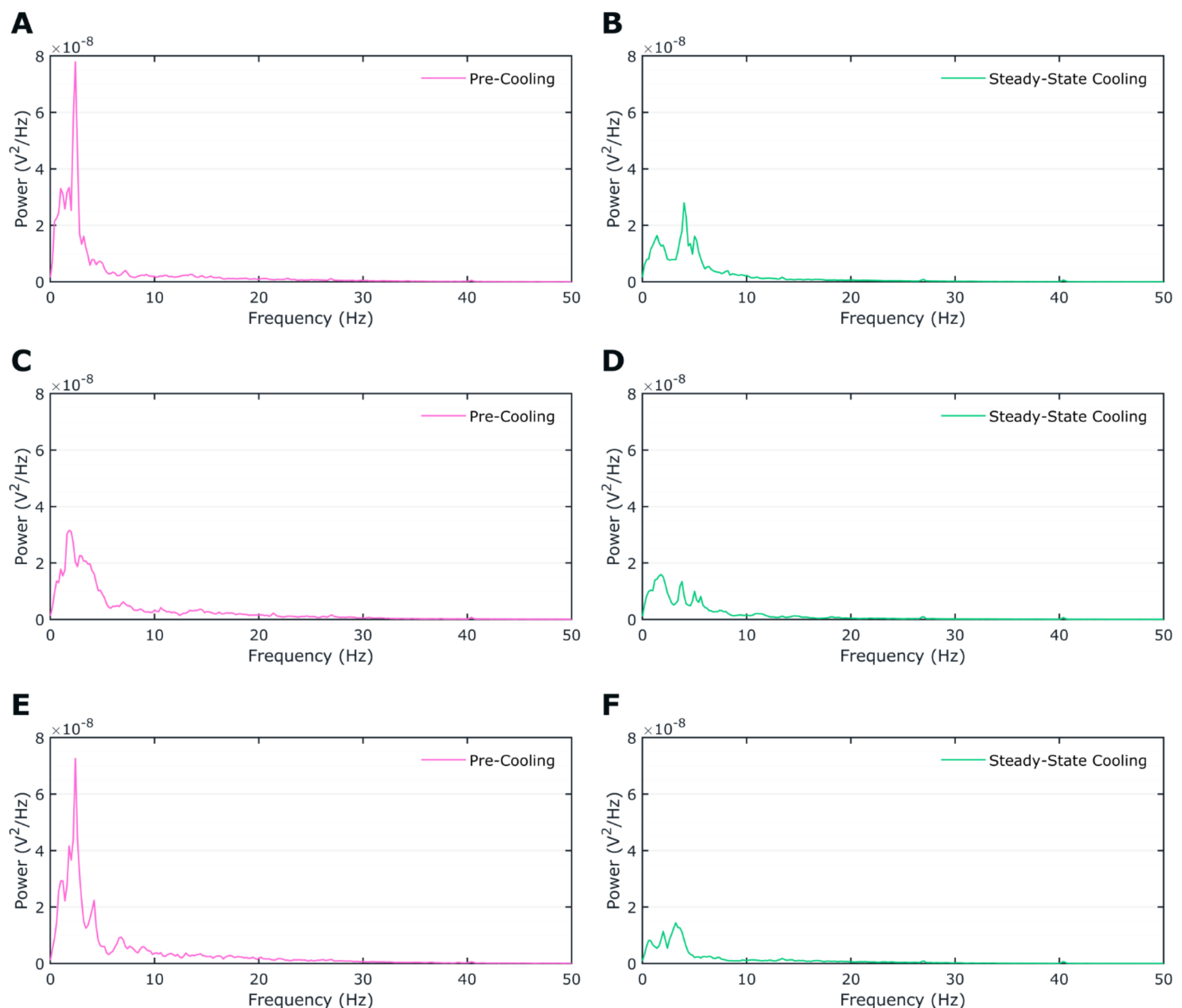

Figure 6.8 Averaged PSD comparisons for focal cooling induced seizure suppression.
On top is the observed signal content during the 30s period before cooling begin and on the bottom is observed neural signal during the latter 30s of the cooling runs when the Interface TEC is seen to be in steady state before turning off.

Every 30 second recording slice was passed through the welch PSD function in MATLAB (MathWorks, USA) to transform the time domain signal into it normalised power spectrum. The following inputs were used for the welch function – window size = 5s, window overlap = 50%, and sampling frequency = 256Hz. The transformed neural data was then grouped into the cooling run temperature reference it was captured during and then further group into wherever it was the pre-cooling neural data or whilst cooling neural data. The PSDs of each cooling temperatures sub-groups were then averaged that would result in each temperature reference having an average pre-cooling PSD and an average cooling PSD. Comparison between the spectral power present in the averaged periods allows for the inference on wherever the focal cooling has produced a suppressive effect when cooling to that temperature refence.

In addition to the cooling run neural data being processed, another 30s slice recording slice was produced from a period recorded before the 4-AP was injected (Figure 6.7A). This is presented as a representative signal to provide a baseline of neural activity within the rat model. The time domain and PSD of it is the activity present when the rat model is only under the influence of the urethane (Figure 6.7B).

Starting with the 25°C cooling runs. The averaged pre-cooling PSD (Figure 6.8A) compared to the average cooling PSD (Figure 6.8B) demonstrates a clear visual difference in seizure activity power between the pre and during the application of focal cooling. This is quantified as a ~35% reduction in the averaged normalised broadband power between 0 – 30Hz. This is heavily indicative of seizure activity being suppressed during the cooling period. Modulation is observed to primarily affect the delta band and theta band.

Modulation through the focal cooling is also observed in the 20°C cooling runs when comparing the average pre-cooling PSD (Figure 6.8C) and the cooling PSD (Figure 6.8D). The pre-cooling power level in the 20°C Cooling runs is noted to be without the large power spike around 3Hz that exists in the 25°C and 18°C pre-cooling PSD. None the less, cooling to 20°C produces an ~46% reduction in the averaged normalised broadband power between 0 – 30Hz. Thus, in steady-state focal cooling to 20°C, the seizure suppression is still occurring.

Comparing the pre-cooling (Figure 6.8E) and steady-state cooling (Figure 6.8F) averaged PSDs of the 18°C cooling runs present the largest observable reduction in seizure power achieved. Seizure suppression due to cooling modulation is shown across the expected 0 to 30Hz band and is quantified as a ~67% reduction in the averaged normalised broadband power between 0 – 30Hz. The effectiveness of cooling to 18°C is in line with what has been reported in literature which has extensively detailed the correlation between cooling to lower temperatures and the increased suppressive modulation it imparts.

6.5 In Vivo Summary

The maturation of the Interface and the Interface Support system allowed for the progression onto *In Vivo* studies. The aim of the studies was to verify the neural recording modality is able to robustly sense neural signals, and to demonstrate the focal cooling modality suppressing seizure activity. A suitable epilepsy model was chosen to with collaborators to fit the Interface's testing aims. A rat model was selected coupled with using the convulsant, 4-AP, to induce epileptiform-type activity for the seizure model.

Inciting of the seizure model was added by a commercial drug delivery system, a Neuronexus D16 probe. An electrode array on this system would provide parallel electrophysiological recording capabilities to compare the Interface electrode data to. Time syncing hardware was fabricated to push simultaneous timing markers to the Interface experimental data and the Neuronexus hardware for data alignment during post processing.

The *In Vivo* studies were designed with cooling runs to four different temperature references - 25°C, 20°C, 18°C, and 15°C. Four cooling runs would be performed at each temperature reference in a row with each run spaced 3 minutes apart. Temperatures were randomised at the start of each experiment to reduce the effect of biologically dependant variables. Three experiments were conducted to record a complete set of cooling runs within three individual animal models.

Analysis of the G-PDMS Interface electrodes ECoG recordings and the parallel Neuronexus probe intracortical recordings verified the functionality of the Interface's neural recording modality. Signal features were shown to be present in both device recordings. The Interface signals were found to have an attenuated amplitude. This, however, is attributed to the Interface electrode's distance from the LFPs origin. Cooling down to 18°C was demonstrated by the Interface's focal cooling modality in a rapid and accurate manner. Thermal instability caused the Interface to struggle to achieve consistent 15°C cooling runs.

Neural data from the cooling runs pre-cooling period and steady-state cooling period sliced into 30s chunks, transformed into PSDs, and then averaged for comparison. Reduction in seizure activity during the 25°C, 20°C, and 18°C cooling runs validates the neural modulating effect of the Interface's focal cooling modality. Averaged normalised power reductions of ~35%, ~46%, and ~67% were calculated respectively.

Next stage of the *In Vivo* work involves the continued collection of cooling run data to provide statistical robustness to the purported seizure suppression ability of this system. With the verified neural recording modality, attention can be turned to attempting the deployment of a seizure detection algorithm *In Vivo* to close the loop in seizure and suppression through focal cooling.

Chapter 7

Conclusion

Presented within this thesis was the work conducted towards the development of a soft, multimodal neural Interface that is designed to monitor and suppress epileptiform activity. Manufacture of the Interface was enabled through the utilisation of direct ink writing – a 3D printing technique leveraged for printing silicones and silicone composites. The regenHU 3D Discovery bioprinter provided the functionality to achieve this. Ease of design alterations within the Interface was used to rapidly iterate system solutions to issues encountered during this research.

SE1700 was used to print the Interface's structural matrix. In this matrix is an embedded micro thermoelectric cooler (2.5 x 3.2 x 0.6mm) to enable actuation of the focal cooling modality. Additional silicone composites were implemented to fulfil specialist system needs. An electrically conductive Graphite-PDMS composite was used to print the Interface's ECoG electrodes. This composite maintains the soft boundary between the neural tissue and the Interface to reduce mechanical damage and glial scar build up at the implant site. A thermally conductive silicone composite was developed for printing the Heat Sink on the TEC hot-side. Composed of SE1700, PDMS, and Alumina, these were mixed in a 3.5:1.5:5 ratio respectively to produce a composite that was rheologically suitable for 3D printing. Mechanical testing verified that the composite retained its mechanical softness. However, the composite's thermal properties restricted the cooling performance of the TEC deeming it unsuitable to be used as the Heat Sink. A mixture of both *In Silico* studies and *In Vitro* experiments were performed to determine a suitable replacement option. As a result, a stainless-steel plate, 6.2 x 6.2mm, was implemented as the Heat Sink.

Removal of the pumped heat from the TEC hot-side required a robust heat dissipation system via liquid cooling. Guidance of the coolant fluid over the hot-side's Heat Sink required the support of a meandering structure – the Microfluidic Loop. The design of a support-free 3D printed tunnel structures was adapted from literature to produce a Loop that could be printed directly onto the Interface's Heat Sink. A python script was written to make automatic alterations to the inter-layer movements within the Microfluidic Loops G-code. This enable continuous printing between print layers that was demonstrated to increases the print reliability. These continuous printing techniques were later adapted during the printed electrodes integration into the Interface Base Section. Through applying continuous printing to the electrode printing resulted factor of 10 reduction in average electrode resistance to 2.83kΩ (±1.69kΩ). Marked increase in electrode print quality and consistence was also noted. The final Interface Version 5 structure measured just 9.5 x 9.5 x 2.3mm.

Functional support of the focal cooling, microfluidic loop, and ECoG recording was provided through the Interface Support hardware system. Power by a 7.4V li-ion battery, the Interface Support hardware was designed enable the primary modalities within a highly integrated setup. A STM32U585 microcontroller is the means by which all system control and monitoring is achieved. The neural recording modality is enabled by an Intan RHD2216 ASIC. The Microfluidic system was actuated via a piezoelectric air pump. Coupled with a pair of air valves, a 'see-saw' flow profile was used to maintain a constant flow regime over the TEC hot-side. The Microfluidic system was able to produce a maximum flow rate of ~71ml/min and supported controllable pump pressure output.

The Interface Support hardware also provided implementations for future Interface modality integration – specifically for the local drug delivery system. The complete Interface Support system was is capable of fitting within a 75 x 130 x 50 mm volume and had a mass ~450g. This size represents the hardware still in it prototyping phase. Part size reduction and the potential of custom ASIC package means that higher levels of integration and a much-reduced system size would be possible in future hardware iterations.

To compliment the Interface Support hardware and enable its operational use, firmware was written in C99 for deployment on the hardware's microcontroller. A PID controller was programmed for the closed loop control of the TEC cold-side temperature. Data sampling was structured within a timer trigger interrupt to provide a pseudo hard-time flow where consistent sampling periods were maintained. Within this sampling interrupt, the neural recording modality was sampled at a 256Hz rate; the Microfluidic system was sampled at a 32Hz rate; and the focal cooling modality sensors were sampled at an 8Hz rate. Hardware control was enabled through a custom command interface. System states could be altered and new PID gains inputted from a remote host PC during experiments. The messaging protocol also provided the means for streaming experimental data from the Interface Support hardware to be gathered and saved on the host PC.

Upon achieving a stable firmware version, a seizure detection algorithm was implemented within the main loop flow to test its stability within the software and if the microcontroller hardware was powerful enough to support it. The algorithm would be called to process a 2s buffer of neural data every 2s. At a maximum, the algorithm had 1.5s to complete its operations. Run time testing of the algorithm whilst recording its function call times resulted in a mean run time of 0.0234s (±0.0011s SD) performing well within its computational time limits.

For monitoring the live data stream and saving it for later processing, a suite of Interface control and data acquisition VIs were written in LabVIEW. These VIs had GUIs that were designed to graph out systems data and provide the control/command options to actuation the Interface systems state. A base set of Interface system LabVIEW blocks were constructed to allow for rapid custom-built VIs for any experimental need. All VIs were designed to save the experimental data continuous whilst running at 2s intervals so minimal data was lost in the cash of a software crash.

At idle, the Interface Support hardware was recorded as consuming 0.592W. Whenever the focal cooling systems would start-up, peaks in power draw would be observed. The maximum these peaks reached was 7.85W. However, once the steady-state cooling temperature is achieved, overall Interface system power consumption during cooling reduced to ~2.75W.

To perform systems verification, an *In Vitro* thermal model was built to emulate the thermal environment an Interface would experience when implanted on neural tissue. Water-agar gel was used as a thermal proxy for neural tissue. It was calculated that a 1%wt water-agar gel had a close thermal conductivity to neural tissue. An Interface sample was encased within this water-agar gel and set within an incubator so that the entire system could be heated to and maintained at ~37.5°C.

From the Interface Version 4 design, temperature differences of >-12°C were recorded on the TEC’s cold-side and fulfils the minimum temperature difference requirement that was derived from literature. From these cooling runs, it was also calculated that the Interface was capable of inducing a ~3°Cs^{-1} cooling rate on the deepest cooling run. This confirmed that the Interface design exceeds both focal cooling modality requirements to be able to theoretically suppress seizure activity. A temperature probe monitoring 3mm away from the TEC’s cooling face confirmed the Interfaces ability to affect temperature change away from the TEC’s cold-side face. Deeper cooling was found to produce the greatest temperature changes at 3mm by the end of a cooling run.

The *In Vitro* verification of the Interface systems and demonstrating that it was able to surpass the minimum requirements for seizure suppression led to the decision to progress onto *In Vivo* studies. Here the aims were to validate the neural recording modality can record electrophysiological signals, and to determine if the focal cooling modality was able to modulate seizure-like activity. In order to fulfil these aims, an epilepsy model was designed with a rat model and the convulsant 4-AP to elicit epileptiform-like activity in the rats somatomotor/somatosensory cortex. To deliver the 4-AP into the cortex, a Neuronexus D16 probe was used. A linear array of electrodes at the tip of this probe would provide the neural recording data to compare the Interface neural recordings against. Collaboration with Dr. J. Berwick's group in the Department of Psychology, University of Sheffield enabled these *In Vivo* studies to progress. All animal work was conducted with the rat model and experimental hardware contained within a faraday cage to reduce external noise.

Four cooling temperature references were used - 25°C, 20°C, 18°C, and 15°C. At the start of each experiment, after the animal surgery and hardware setup was complete, the cooling temperature reference order was randomised. Seizure activity was initiated through the perfusion of 4-AP through the Neuronexus probe. Once seizure-like activity had been established, cooling runs were commenced such that four runs of each temperature refence were conducted sequentially before changing to the next temperature reference. A 3-minute idle period between runs prevented any cooling effect from overlapping with the next run. Syncing hardware was used to inject marker points into both the Interface data and Neuronexus data to allow data alignment in post processing.

Aligning the Neuronexus recordings with the Interface electrode recording first provided validation that the Interface was recording electrophysiological activity. Identically time-domain features were present and aligned in both signals. Comparison of the PSDs of both signals did reveal the attenuation in the signal recorded by the Interface. However, this could be accounted for due to the Interfaces recording electrode being placed epidurally and further away from the neural activity than the Neuronexus probe was.

From the cooling run data recorded from 3 animals, a 30s pre-cooling period and latter 30s steady-state cooling period was first sliced out. Each slice of data was transformed into their PSDs and before being grouped by temperature refence and slice origin. All PSDs with each group was averaged and plotted. The pre-cooling and steady-state cooling PSDs were compared to determine if the Interface's focal cooling had had a suppressing effect or not. Through this comparison it was determined that the Interface focal cooling was shown to have reduced the seizure power whilst cooling was ongoing. Suppressing effects were seen at each temperature reference with the 25°C, 20°C, and 18°C producing averaged normalised broadband power reduction between 0 – 30Hz of ~35%, ~46%, and ~67% respectfully. These results from the *In Vivo* study validates both the neural recording modality and the focal recording modality of the Interface and demonstrates its viability as a device for seizure suppression.

In summation, this research project has manged to fulfil its aims laid out within the introductory chapter. The regenHU 3D Discovery printer was used to leverage 3D printing technologies for manufacturing the Interface structure out of soft silicone inks. This structure was demonstrated to successfully host the focal cooling modality and the neural recording modality. Manufacturing changing to add in the local drug delivery was also explored near the end of the Interface development. Other than the TEC element, the Interface presented a soft external structure.

The focal cooling modality was successfully implemented on with in the Interface. It was the primary driver for most of the structural and material alterations as the research progressed. *In Silico* studies and *In Vitro* experiments were iteratively used to validate and guide these changes. By the final Interface Version 5 design, rates of cooling (~3°Cs^{-1}) were able to be produced the TEC and steady-state temperature maintained (±0.25°C). These specifications position the Interface as being at the top end in terms of achievable cooling rates and time to target temperature.

System firmware was composed and structured to enable hosting of a seizure detection algorithm. Bare-metal programming provided scope to optimise the execution of code pertaining to Interface modality function. It was done in hopes of retaining enough spare computational time for an algorithm to execute within the 2 second recording window. Integration of the Dr S. Chen's seizure detection algorithm and runtime testing demonstrated deployment viability and potential for its online use in-the-loop.

Finally, the Interface, Support hardware, and firmware was fully integrated together for *In Vivo* study. An experiment to test the seizure suppression effectiveness of the Interface was design to minimise the influence of uncontrollable variables with biological systems. Cooling runs were conducted on a 4-AP incited seizure model and its effect on neural signals were recorded through the Interface's printed electrodes. Comparison of nominal seizure activity to seizure activity during a cooling event demonstrated a suppressing effect caused by the Interface's focal cooling modality. This does provide evidence this system does warrant consideration for further development towards becoming a clinically viable implantable device in for the treatment of epilepsy.

7.1 Future Research Directions

The IntegraBrain research project was aimed at presenting a multimodal, implantable device that would present an evolution towards tighter systems integrate. This was with the target of progressing this class of system closer to being deployed within the clinical environment. Because of the multidisciplinary nature of this research project, there are plenty of research threads that can be pursued coming out of this research project.

Hardware Miniaturisation

The current state of the Interface Support hardware is still very much within the realm of prototype. Whilst, the main board PCB is about the size of a mid-range smartphone there is still scope to condense the system further. Smaller component packages, optimised track routing, and component placement would present some immediate results. Beyond layout-based changes, there is also the tighter coupling of the Microfluidic system hardware into the main system hardware. Integration of the pneumatic hardware, i.e. air valves and mounting blocks, will present a challenge. As the neuromodulation electronics design eventual reaches a static, tested state, these systems could be incorporated onto a single ASIC package. to enable system suitable for subcutaneous implantation.

Cooling Deep Cortical Structures

The main restricting element in the viability of the current Interface design in being a treatment option for the broadest set of epilepsy type, is that it is only able to perform cooling at the cortex surface. Whilst the Interface has demonstrated producing a cooling effect 3mm below the TEC cold-side face, this is not deep enough to influence epileptic foci located deeper within a patient's brain structure. A proposed solution to this would the development of a soft, flexible heat pipe [159]. One end of the pipe would be attached to an Interface-like unit on the cortical surface. This unit would contain the required TEC cooling systems to drive the heat pipe heat transfer. Whereas, the other end of the heat pipe would be placed at the epilepsy foci point where it would present a heat exchanger as the site of cooling.

Manufacturing a heat pipe to be soft and to be flexible would result in a significate research project in of itself. Bioinspired heat pipe designs have been reported in literature [160, 161] with some focusing on miniaturisation of heat pipe systems [162]. However, research into biocompatible and implantable designs is still in its infancy. The technical challenges to make such a device viable for human implantation presents a wide scope for future research and discovery.

In-Loop Seizure Detection

Upon validation of the seizure detection algorithm being able to run on the Interface Support hardware without timing issue means the next logical step is to trial the algorithm prediction accuracy during live neural recordings. The algorithm itself was trained using labelled neural signal recordings collected by the Interface during the *In Vivo* studies. The detection algorithms immutable design allows for the detection results captured over the study to be compared with the original MATLAB detection algorithm output after being provided the same recordings. When such testing has built confidence in the accuracy of the detection outputs, the seizure detection algorithm could then be placed in-the-loop with the cooling run activation controls. In order for that to occur Dr. S Chen advised that the algorithm would require more sets of neural recording data for further model training. Thus, pursuing this thread will require undertaking more *In Vivo* studies to produce the number of neural recordings required to train and test the algorithm.

Thermal System Design

Whilst the focal cooling modality was able to perform beyond expectations within the Interface system, there is still scope to experiment further with its design. Performing cooling runs to the edge of the required cooling range (~15°C) still produces frequent thermal instability. Improving cooling performance around this temperature would be the immediate aim. This could be split into two areas of focus. The first is the hardware. Revisiting the study performed with the Heat Sink could present the opportunity to, again, explore powder bed fusion 3D printing and fabricate an Interface unit with a finned heat sink implementation. Coolant fluid experimentation is another section to investigate since the fluid used during experiments was kept a constant throughout for data consistency (de-ionised water).

The second area is the TEC controller. As discussed in Section 5.5.3, a PID controller is not a suitable control system for the TEC due to it being a highly non-linear system and a PID controller being only for linear systems. To reduce development time, the PID controller was used. Because a linear PID controller is not able to adequately model the non-linearity of the TEC behaviour, the region of stable operating behaviour was extremely narrow. The controller was very sensitive to noise and external perturbations. So, to increase that stable operating window, experimenting with controller architectures designed for non-linear systems would be required for improved cooling operation.

A Wireless Future?

Current experimental and clinical designs for focal cooling devices rely on hardwired connections and often bulky support hardware. Whilst this research project was able to produce a relatively compact system size, the hardware was still too large for clinical deployment. In an attempt to find a solution to this issue, two research groups have proposed designs for wireless system focal cooling system.

Both focal cooling devices implement a TEC as core system actuator and utilises RF-DC for wireless power transfer. Hou et al's design embeds the detection and actuation systems onto one remote module to be implanted at the required site. A Bluetooth module is used for two way systems communication and control between the module and a base PC [163]. Improvements were made by Fernandes et al to miniaturise the wireless system further. As a result, a highly integrated device was realised which measured approximately 2 x 2mm and had a thickness of approximately 1.5-2mm [164]. This size allowed for device deployment within almost all required spaces *In Vivo*.

Both of these systems presented a practical means of implementing wireless technologies for a focal cooling device. Future work could be undertaken to incorporate elements for these systems into the future evolution of the IntegraBrain system. Small, solid-state battery technology would be needed to mature for enabling power storage for cooling during periods when wireless power isn't available. Safety is also a concern for the wireless connectivity, especially for Fernandes et al's design. Malicious actors interfering with device function could lead to permanent neural tissue damage.

Chronic Studies

Validation of the Interface system within the acute *In Vivo* epilepsy model laid the ground work for potential undertaking of chronic *In Vivo* studies in the future. Chronic studies would be able to provide data on the stability of the printed electrodes over long term recordings and wherever the softer electrode material reduces chronic immune response from mechanical mismatch. The models immune response can also be monitored at the boundary between the neural tissue and the stiffer TEC cold-side surface to check if this modulates cooling performance.

Chronic studies also provide the opportunity to be able to test the stability and robustness of an in-the-loop seizure detection algorithm. An incited chronic epilepsy model, which displays random occurrences of ictal activity, presents the ability to collect data on the seizure detection algorithms performances and also test the purported neuroprotective effects of cooling on subsequent seizure activity.

Any of these research threads are a potential path to follow. If only there was more time to tread them all!

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Appendix A
Material and Fabrication Methods

All material processing and use should be done in full PPE. This includes gloves, goggles, and a lab coat to prevent unintended injury.

A.1 Material Preparation

Here is the details on the methods used to prepare the materials implemented over the course of this project. Preparation instructions are provided for both the sourced commercial materials and the composite materials developed for, or adapted, to the Interface design.

A.1.1 PDMS

PDMS (SYLGARD 184 Silicone, Dow) is a two-part, heat cured Polydimethylsiloxane elastomer. Its low viscosity allows for mixing with desired additives to produce material composites the have the desired viscosity suitable for direct ink writing 3D printing. Part A and Part B is mixed in a 10:1 ratio respectively.

For the preparation of 4.4g of PDMS. Using the balance (SE-422, VWR), measure 4g of Part A and 0.4g of Part B into a 35ml container. Mount the container in the mixer's adapter (250AD-NAN-U, Intertronics). Measure the mass of the material, container and appropriate mixer adapter. Alter the counterbalance on the mixer (ARM-310CE, Thinky Corporation) to the same mass value as measured and mount the material container unit in the mixer. Set the mixer RPM to 2000 and the timer to 3 minutes. Start the mixer to complete a full cycle. Once the mixer has stopped, remove the container from the setup. Dispense as required.

A.1.2 SE1700

SE1700 (DOWSIL SE 1700, Dow) is a two-part, heat cured polydimethylsiloxane adhesive. This material provides an approximate 8 hour working time with the required shear thinning properties that allow for direct use with 3D printing technologies. Part A and Part B is mixed in a 10:1 ratio respectively.

For the preparation of 4.4g of SE 1700. Using the balance (SE-422, VWR) measure 4g of Part A and 0.4g of Part B into a 35ml container. Mount the container in the mixer's adapter (250AD-NAN-U, Intertronics). Measure the mass of the material, container, and mixer adapter. Alter the counterbalance on the mixer (ARM-310CE, Thinky Corporation) to the same mass value as measured and mount the material container unit in the mixer. Set the mixer RPM to 2000 and the timer to 3 minutes. Start the mixer and complete a full cycle. Once the mixer has stopped, remove the container from the setup. Dispense as required.

A.1.3 Thermal Epoxy

Primarily used in the adhesion of Interface components within the thermal path of the embedded TEC. The Thermal Epoxy (MED-T7110, Epoxy Technology) comes in two parts – Part A and Part B. Both Part A and B are mixed at a ratio of 10:1.

For the production of 2.2g of the Thermal Epoxy. Using a balance (SE-422, VWR) measure 2g of Part A and 0.2g of Part B into a 13ml container. Mount the container in the mixer's adapter (250AD-NAN-U, Intertronics). Measure the mass of the material, container and mixer adapter. Alter the counterbalance on the mixer (ARM-310CE, Thinky Corporation) to the same mass value as measured and mount the material container setup in the mixer. Set the mixer RPM to 2000 and the timer value to 2 minutes. Start the mixer to complete one full cycle. Ensure the mixture is fully combine before use.

A.1.4 Thermal Silicone Composite

The Thermally Silicone Composite is comprised of Al_2O_3 powder (AL606010/23, Goodfellow), PDMS and SE 1700. This material is intended to act as a thermally conductive and electrically non-conductive substrate that can be used with DIW 3D printing technologies. 3D printing ability of this material is achieved by tuning its viscosity via the SE 1700/PDMS ratio. For this system the appropriate Alumina, SE 1700, and PDMS ratio is 10:7:3 respectively with respect to mass.

For the preparation of 5g of the Thermal Silicone Composite. Using the balance (SE-422, VWR) measure out 2.5g of Alumina powder, 1.5g of prepared SE 1700, and 1g of prepared PDMS into a 35ml container. Mount the container in the mixer's adapter (250AD-NAN-U, Intertronics). Measure the mass of the material, container and mixer adapter. Alter the counterbalance on the mixer (ARM-310CE, Thinky Corporation) to the same mass value as measured and mount the material container unit in the mixer. Set the mixer's RPM to 2000 and the timer value to 3 minutes. Start the mixer to complete one full cycle. Remove the contain, open and stir the mixture with a spatula. Replace the lid and remount the container unit in the mixer. Start the mixer to complete another 3-minute cycle. Remove the container from the setup. With a spatula, hand mix the material to combine any separated material. Repeat Steps 6. to 12. twice more. Once finished, the material is ready for use.

A.1.5 Electrically Conductive Silicone

An electrically conductive material that can be 3D printed is produced by mixing graphite flakes (282863-25G, Aldrich) and PDMS. The conductivity and viscosity of the material can be tuned through adjusting the mixture ratio. As the Interface electrodes have a greater requirement for electrical conductivity, the components were being mixed in 50% Graphite/50% PDMS ratio with respect to mass.

For the preparation of 4g of the Graphite Silicone composite. Using the Balance (SE-422, VWR) measure out 2g of Graphite Powder, and 2g of pre-prepared PDMS into a 35ml container. Mount the container in the mixer's adapter (250AD-NAN-U, Intertronics). Measure the mass of the material, container and mixer adapter. Alter the counterbalance on the mixer (ARM-310CE, Thinky Corporation) to the same mass value as measured and mount the material container unit in the mixer. Set the Mixer's RPM to 2000 and the timer value to 3 minutes. Start the Mixer to complete one full cycle. Remove the container from the mixer. Open it and hand mix the contents with a spatula for 20 seconds. Seal the container and then place it back in the mixer. Repeat the Mixer and hand stirring process twice more before the conductive silicone is ready to be used.

A.1.6 Silicone Adhesive

A two-part Silicone-Based Adhesive (MED3-4013, NuSil), this is used primarily in the bonding of non-silicone materials to the bulk Interface material. This adhesive comes is mixed in a 1:1 ratio of Part A to Part B respectively. The following reparation instructions are for the adhesive that is provided the double-barrelled cartridges.

For the preparation of the MED3-4013 Adhesive, remove the front and back caps from the material cartridge. Load the material cartridge into a dispensing gun. Into a 13ml container, dispense the required amount of material. The combination of the packaging and dispensing gun ensures a 1:1 ratio is maintained during measuring. Once the required amount is achieved unmount the material container from the gun. Replace its back cover. With tissue, wipe away any excess of both parts from the nozzle. This will ensure that it doesn't get blocked during storage due to cross-contaminated material curing.

Mount the filled container in the mixer's adapter (250AD-NAN-U, Intertronics). Measure the mass of the material, container and mixer adapter. Alter the counterbalance on the mixer (ARM-310CE, Thinky Corporation) to the same mass value as measured and mount the material container setup in the mixer. Set the mixer RPM to 2000 and the timer value to 3 minutes. Start the Mixer to complete one full cycle. Ensure the mixture is fully combine before use.

A.1.7 Adhesive Surface Primer

A surface primer (MED6-161, NuSil) that is applied to surfaces that normally don't allow sufficient bonding when the silicone adhesive is applied to the raw surface. This is primarily used on the ceramics, and stainless steel in the TEC Assembly when the attaching it to the Base Section. This primer dries by reacting with the moisture in the air so keep container opening to the minimum required time to dispense it.

To use this Primer, the following instructions are to be completed within a fume hood. Clean the required surfaces of the item to be primed with an appropriate solvent. Remove the surface primer from storage. Ensure the primer homogenous by shaking it for 30 seconds. Dispense the required use amount into a sample boat via a pipette. Immediately seal the primer container and place it back in storage. Using a fine-grade brush or microfibre cloth, spread an even layer over the surfaces so that it is visibly wetted but the primer is not pooling. Wait for the primer to dry. Once dry, the item can be handled and removed from the fume hood as bonded with the silicone adhesive as needed.

A.1.8 Silicone Conformal Coating

This surface modification primer (Conformal-Coating 422B, MG Chemicals) is primarily used as a coating to aid in the releasing of printed silicone objects from glass slide. It can also be used to cover 3D printed resin moulds to prevent the cross-linking retarding effect seen with silicones cured within resin prints.

Ensure that all instructions for using this primer take place in a fume hood. To apply the conformal coating, first clean the surface to be primed with a solvent or relevant cleaning product. Remove the primer spray canister from storage. Shake the canister for at least 30 second to thoroughly mix the canister materials. Whilst holding the can nozzle 20cm away from the surface to be primed, apply an even layer of primer across it to the thickness desired. Place the primer canister back into storage. Wait until the surface has fully dried before removing from the fume hood or applying another layer of primer.

A.1.9 Water-Agar Gel

Agar Gel is used in the creation of pseudo-neural tissue for In Vitro thermal tests of the Interface. The water-agar gel is produced with a 1% Agar concentration. This concentration produced a gel with the approximation thermal conductivity of 0.4672 W/m·K at 37°C. Agar powder, 05040-100G, sourced from Sigma Aldrich is used for all In Vitro models produced during this work.

Within a fume hood set up a hot plate stirrer (MS-H_Pro+). Use a balance to measure 0.5g of agar powder into a sample boat. Measure 50ml of distilled water into a 100ml beaker. Place a 15mm magnetic stirrer probe into the beaker and position the beaker on the hot plate platform's centre. Set the hot plate to 200°C and activate the heating element. Using a temperature probe, monitor the water the rising water temperature. Once 100°C has been reached, set the magnetic stirring RPM to 600 and activate stirring. Wait until the stirring probe has reached a constant rotational speed.

After a constant speed is seen, tap the agar sample boat to add a small amount of agar powder the water surface. When that agar powder is fully incorporated into the water, add another amount. Continue this process until there is no more agar powder in the sample boat. Reduce the stirrer speed to 200 RPM and keep heated for 5 minutes.

If the Interface v3 or v4 In Vitro Setup is used:

Turn off the Hot Plate's heating element and stirrer function after the time has elapsed. Place a 150mm petri dish next to the Hot Plate. Use a pair insulated tongs to pick up the beaker and pour the heated water-agar solution into the petri dish ensuring the magnetic stirrer probe is filtered out of the solution. Clean the beaker of agar solution remnants. Leave the water-agar solution to cool down to room temperature (~20°C), setting the agar gel.

If the Interface v5 In Vitro Setup is used:

Turn off the Hot Plate's heating element and stirrer function after the time has elapsed. Using a temperature probe, monitor the water-agar solution until it reaches 55°C. Use a pair of insulated tongs to pick up the beaker and slowly pour it into the 50ml beaker that contains the In Vitro Interface Mount structure. Ensure the magnetic stirrer is filtered out of the solution whilst pouring. Clean the beaker of water-agar solution remnants. Leave the water-agar solution in the In Vitro model beaker to cool down to room temperature (~20°C), setting the agar gel.

A.2 Interface Manufacturing

The following is the complete method to fabricate the Interface v5 design from the initial vector drawing to soldering the Interface connector. The sections are ordered to be followed sequentially with the recommended Interface fabrication order provided in Figure A.1. This process assume access to a 3D Discovery Bioprinter from regenHU and access to their proprietary software for the G-code generation and printing capabilities.

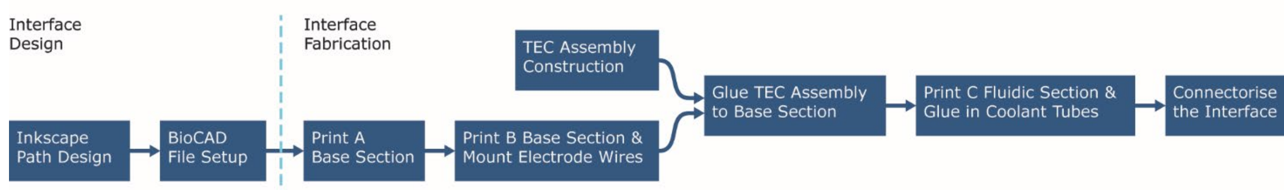


Figure A.1 Interface design and fabrication construction flow.

A.2.1 Interface 3D Printer Path Processing

A custom device workflow is used for Interface print file preparation to circumvent software and print issues experienced with utilising the regenHU software workflow in isolation. This workflow description will discuss the software options and order of operation. The settings presented are the finalised process for Interface Version 5 manufacture. Path drawing details will not be included. A folder containing Inkscape 1.1 SVG files of the Interface Version 5 paths can be provided on request.

Software packages required for this process include Inkscape 1.1, Python 3.9.6, BioCAD 1.1 and a plain text processor. In this instance, Notepad++ is used to fulfil the plain text processor role for manual alteration of the G-code.

Inkscape

To begin with, open a new instance of Inkscape and create a new document. Open the Document Properties. In the Page tab, set the Display Units to 'mm' and have the Page Size set to 'A4' in Landscape. Select the Grids tab. Use the Creation section to make a new 'Rectangular grid'. Ensure that the 'Enabled' and 'Snap to visible grid lines only' are ticked. In grid options have the Grid Units as 'mm' then type 0.228 into Spacing X and Spacing Y value fields. Then close the Document Properties tab.

Zoom into the bottom left of the A4 document by ~1500% or until the grid lines don't subdivide any further. Place two y-axis guides and two x-axis guides 9.350mm or 40 grid lines apart. This is the outer path boundary for the Interface. Lock the guides in place by going to Edit->Lock All Guides. Select the View Layers option on the top icon bar. Create six layers. From the lowest to highest layer, name them: A Base Level 1; A Base Level 2; B Base Level 2; B Base Level 3; B Base Level 4; B Base Level 5.

Interface path drawing can now be undertaken. Select the 'Draw Bezier curves and straight lines' tool for drawing the paths. On A Base Level 1 is the opening for the electrode faces and TEC cold side. On A Base Level 2 is the electrode printed wire channels and where the TEC wire channel begins. On B Base Level 2 is the electrode printing paths using the G-PDMS composite. On B Base Level 3 is a solid layer that covers the electrode channels leaving only the TEC areas open to create a U shape. On B Base Level 4 is a similar path to Level 3 except the U ends are shortened by 0.228mm. On B Base Level 5 is a path that encloses the perimeter of the TEC Assemblies Metal Heat Sink creating a recess to guide its placement. Have an alternating end nodes directly overlap between B Base Level's 3 and 4 and the B Base Level's 4 and 5.

Each path node is to be placed on a grid intersection point. The document has already been setup for nodes to automatically snap to them to make this process easier. For the interface design, all paths are kept straight. If any Bezier curves are inserted, select the offending node(s) with the 'Edit paths by nodes' tool then select the 'Make selected nodes corner' option. Path width should be modified to 0.230 in the Fill and Stroke->Stroke style tab. This helps indicate where any gaps are between paths. Set the path colours to an alternating scheme using Fill and Stroke->Stroke paint tab settings to provide better layer differentiation.

Next the Microfluidic Loop paths are to be drawn. Continuing in the same file, re-open the Document properties. Un-tick the 'Enabled' option in the current 0.228mm grids settings and then create a new rectangular grid. Set this up using the same settings as before other than the spacing values. In the Spacing X and Spacing Y value fields type 0.16264 and then close Document Properties.

The Microfluidic Loop it a highly constrained structure that requires a pre-defined path layout. Guides are used to form a Loop path node placement scaffold. To the right side of the Base Section layers will be the Loop pathing site. On the x-axis place 8 Guides interspaced sequentially left-to-right by 9-1-9-1-9-1-9 grid lines from the first Guideline. On the y-axis place 5 Guides interspaced sequentially top-to-bottom by 9-30-9-5 from the first Guideline. Each Guide intersection point in the scaffold indicates the location of a Microfluidic Loop path corner. Check that the 'Lock All Guides' option is selected under the Edit dropdown menu.

Return to the Show Layers tab window. Create 7 new layers that are placed above the Base Level layers. Name these layers from the one closest to the Base Section layer to the layer list top the following: C Liquid Level 6 [90]; C Liquid Level 7 [90], C Liquid Level 8 [90]; C Liquid Level 9 [45]; C Liquid Level 10 [45]; C Liquid Level 11 [45]; C Liquid Level 12 [45].

Setup is now complete for drawing the Microfluidic Loop paths. Select C Liquid Level 6 [90] as the active layer and select the 'Draw Bezier curves and straight lines' tool. Find the bottom left corner of the Loop Guide scaffold. From this point count 4 grid lines moving right along the x-axis. Place the first path node at this grid point. Continue the drawing the path by following the

Guide intersection points in a clockwise sweep. At each point place a path node. Every point must form a 90° corner between the previous path and current path. The last node should be placed atop the starting node ensuring that they don't connect together and create a closed path. It must be an open path with a defined start and end point. An 'M' shaped channel will have been formed by the drawn path.

A copy of the C Liquid Level 6 path is placed on the C Liquid Level 7 and 8 layers. These copies are placed in exact alignment atop the first drawn path. On C Liquid Level 9 a path is drawn starting from the same start node as the previous paths. It is drawn one grid line offset from the path below into the channel space. This offset is not applied to two of the loop paths sections. Both sections are located on the x-axis Guide on which the start/end node placed. These path sections will become the Microfluidic Loop Inlet and Outlet. On C Liquid Level 10, C Liquid Level 11 and C Liquid Level 12 follow the pattern of drawing a path 1 grid line offset from the previous layer bar the stated path section exceptions. Drawing the C Liquid Level 12 path will close the channel top. Pathing of the Microfluidic Loop is now complete.

The last operation to conduct in Inkscape is to stack the Microfluidic Loop paths a top the Base Section Paths. Select all of the Microfluidic Loop paths using the 'Select and transform Object' tool. Drag the selected layers till they are over the top of the Base Section. The Microfluidic Loops is aligned centrally on the Base Section ensuring that Heat Sink recess formed by the B Base Level 5 path is completely covered in the process.

The Interface path is required to in the DXF R12 format for successful import into BioCAD. Open the File drop down menu and select 'Save As'. Name the Interface Paths 'v5_interface_paths' and in the 'Save as type' drop down menu select 'Desktop Cutting Plotter (AutoCAD DXF R12) (*.dxf)' before saving the file.

BioCAD

Open a new instance of BioCAD. Using the File->Import action, go to the v5_interface_paths.dxf file location and select it for importing. Once imported the layers will be seen in the top window of the print order section. Click the scale tool found in the vertical tool bar. Holding left click down in the pathing workspace, drag the cursor to select all of the imported paths. Release the left mouse button to finalise selection. Perform a single left click within the workspace window. In the Scale command window popup type 3.546 into both scale value inputs and accept the transformation. Isolate the view to the A Base Level 1 layer via the top toolbar option. Use the Measuring Tool on the vertical tool bar to compare the external path dimensions to the Inkscape design to check it scaled correctly.

In the pathing workspace centre are arrows that dictate the XY axis (0,0) origin point of the 3D Discovery printable area. Click the Layer icon located on the top tool bar to create a new layer and name it 'Glass Slide'. Select this layer to make it the active layer. Using the Rectangle shape tool on the vertical toolbar, draw a 75mm by 26mm rectangle than is centred on origin point. This provides reference to the glass slide position that the Interface will be printed on. Use the move tool to select all of the Interface related paths and position them in the centre of the slide. Use the move tool once more the increase the distance between the lower glass slide edge and the Interface edge containing the internal channel exit by 4mm.

Again, isolate the A Base Level 1 layer. Turn on the nozzle travel direction indicators and path print order numbers using the top toolbar. Small markers should now appear on each path that describe how each line will be printed. A Base Level 1 should start from very left-hand path and print continuously until the nozzle reaches the end at the bottom left corner of the TEC insert space. If this is not the case, select the change path direction tool on the vertical toolbar. Then click on that very left-hand line until the arrow away from the line end (or upwards when viewing the screen). This check needs to be undertaken for every layer to ensure correct printing.

For the rest of the layers: A Base Level 2 needs to start printing from the lower left-hand corner with the nozzle then moving right. Printing ends halfway up the right-hand side of the layer paths. B Base Level 2 contains all the Electrode paths and should start printing from the Electrode sites and moves toward the TEC wire channel. Electrodes should print in the order E2, E4, E3, E4. Each Electrode will have a 'no extrude' nozzle travel path near its end but separate. This need to take place after each respective Electrode it is a part of. If their print orders are incorrect, select the switch print order tool on the vertical toolbar. The tool reorders the print paths by the user selecting the print paths in order of printing from the first to the last. Using this reorder the Electrode print paths to conform with the Electrode print order stated before.

B Base Level 3 print start point is located on the bottom left corner and the nozzle should zig-zag inwards towards the centre. The end point is located adject to the TEC wire channel on its left side. B Base Level 4 print start should be located above the Level 3 path end point and should zig-zag its way outwards. B Base Level 5 print start point is located directly above the end point of Level 4. The nozzle should then worm its way inwards and end in the lower left corner of where the Heat Sink will be mounted.

For the C Fluid layers, they all have the same start and end point that is located in the centre of the left inlet/outlet channel horizontal wall. The nozzle should move in a clockwise direction around these closed paths. Evey layer must be verified before continuing.

Material Application

The path materials now need to be assigned to each layer. Go to Tools->Materials to input the extrusion profiles for the print materials. The Interface paths require the material profiles: SE1700 Base v5, SE1700 [90°], SE1700 [45°], and Graphite Silicone [50%]. These profiles are found in Appendix B. Once the profiles are inputted and saved return to BioCAD's main window and select A Base Level 1. To the bottom left of workspace window is the window that displays

the Layer properties. Within this select the empty materials option box and a menu of the saved material profiles is shown. By clicking on the material profile assigns it to the layers path. Material profiles allocations to each layer is described in **Table *A.1***.

Next, create three layer groups by selecting the Group icon on the top tool bar. Name these three groups 'A Base', 'B Base', and 'C Liquid'. Starting with the C Fluid paths, drag and drop the layers one at a time into the group starting with Level 6 until Level 12. Repeat this process for B Base paths start with Level 2 an A Base starting from Level 1.

Table A.1 Material profile allocations for the Interface print path layers.

Interface Section	Layer Name	BioCAD Material Profile
A	Base Level 1	SE1700 Base
	Base Level 2	SE1700 Base
B	Base Level 2	Graphite Silicone [50%]
	Base Level 3	SE1700 Base
	Base Level 4	SE1700 Base
	Base Level 5	SE1700 Base
C	Liquid Level 6 [90]	SE1700 [90°]
	Liquid Level 7 [90]	SE1700 [90°]
	Liquid Level 8 [90]	SE1700 [90°]
	Liquid Level 9 [45]	SE1700 [45°]
	Liquid Level 10 [45]	SE1700 [45°]
	Liquid Level 11 [45]	SE1700 [45°]
	Liquid Level 12 [45]	SE1700 [45°]

Now create a new object by selecting its icon on the top toolbar. It will appear as 'Object 01' in the object window to the left of the workspace. Click and drag the A Base group over to the object and release the left mouse click. This should have placed the group within the object. Select the object. In the properties window below set the initial height to 4.9mm for the glass slide offset from the print bed. Selecting the A Base within the object make sure its build count is set to 1 in the properties window. A Base is ready to be exported from BioCAD. Press the green arrow on the top toolbar to perform the export action. It will be placed within the same folder as the saved BioCAD file. Go to the folder and rename the exported file `v5.2_a_base.iso`.

Return to BioCAD. Remove A Base from the object by selecting it and pressing delete. This will only remove its instance from the object but not from the layer window. Now click B Base and place it into the object. For this print instance, set the object initial height property to 5.51mm to account for A Base being printed. Verify that the B Base build count is 1 and then export it as before. Name this file `v5.2_b_base.iso`.

Finally, this process needs to be repeated for the C Fluid group. The object initial height is set to 6.17mm and the build count must be verified to be 1 in the object's C Fluid properties. Export this print instance and name the file `v5.2_c_fluidic.iso`.

A.2.2 Continuous Print Processing

Before performing this method of processing on G-code with the Continuous Printing script, Python must be installed onto the User machine. Select the 'Add Python.exe to PATH' option when installation is done. Python version 3.9.6 or above should be used to ensure the correct function of the Python Script.

Open file v5.2_b_base in a text editor (Notepad++, Don Ho). First the electrode printing section needs to be masked off from processing. Place a '$' symbol on the line immediately after the '`(Program-Start)`' comment on Line 10 and another symbol after the first 'G1' movement command on Line 104 that makers the beginning of the B Base Level 3 print path. Save this file alteration.

Move the `v5.2_a_base.iso`, `v5.2_b_base.iso` and `v5.2_c_fluidic.iso` files to the same folder that the continuous_printing.py script is located. For this it is recommended to have it in a folder on Desktop to provide a short folder path name – for this example it will be called con_print.

Open the Windows Command Prompt. Providing Command Prompt is pointing to C:\Users\UserName, alter the directory to the con_print folder using the command:

```
cd Desktop\con_print
```

Then run both G-code files through the continuous_printing.py script using the following two commands:

```
py continuous_printing.py v5.2_b_base.iso v5.2_b_base_processed.iso

py continuous_printing.py v5.2_c_fluidic.iso v5.2_c_fluidic_processed.iso
```

Check the amount of command replacements is correct by comparing the number of printed command line statements printed to the number of expected print statements. For `v5.2_b_base.iso` there should be 2 print statements. For `v5.2_c_fluidic.iso` there should be 6 print statements. These files can then be moved back to the required folder ready for printing.

A.2.3 G-code Modification for Continuous Electrode Printing

The last G-code modifications that need to be made before printing can commence is for the continuous printing of the Interface Electrodes. This is performed manually. The general format for the long electrodes (E1 & E3) and short electrodes (E2 & E4) will be describe. It is noted that the electrodes X-axis and Y-axis locations will differ depending on Interface location in BioCAD. The Graphite PDMS Composite purge path G-code will also be given and can be directly copied.

Open `v5.2_b_base.iso` in a text editor like Notepad++. Locate the G-code section for B Base Level 2. Within this block there are 8 discrete printing blocks marked by the M96 G-code command at the end of each one. These blocks are in the pair format: electrode G-PDMS line, electrode non-extrude line. Each pair are to be combined.

Code transformations for the short electrode type and long electrode print paths are given below. The left block represents the code found in the raw G-code output from BioCAD. The right is the continuous electrode code format. Strikethrough is used to denote redundant code to be removed. Colours are used to dictate changes made to the kept code. Orange for modifications to the lines command values. Green for new code added to the block.

For the E1 & E3 Continuous Electrode G-code:

G0 Z5.39
G0 X3.924 Y4.241
G0 Z5.29
M97
M30 P3.6
G1 X4.038 Y3.67
X4.038 Y1.617
X5.178 Y1.617
X5.178 Y-2.547
X3.581 Y-2.547
M96

~~G0 Z5.39~~
~~G0 X3.57 Y-2.55~~
~~G0 Z5.29~~
~~M97~~
~~M30 P3.6~~
~~G1~~ X1.471 Y-2.547
~~M96~~
~~G0 Z5.39~~

→

(Electrode 1 Print Start)
G0 Z5.4
G0 X3.924 Y4.241
G0 Z4.8
M97
M30 P24.4
F0.15 G1 Z5.1
F4.2 G1 X4.038 Y3.67
X4.038 Y1.617
X5.178 Y1.617
X5.178 Y-2.547
X3.581 Y-2.547
M96
X1.471 Y-2.547
(Electrode 1 Print End)

For the E2 & E4 Continuous Electrode G-code:

G0 Z5.39
G0 X3.924 Y-0.095
G0 Z5.29
M97
M30 P3.6
G1 X3.809 Y-0.665
X3.809 Y-1.692
X3.581 Y-1.692
M96

~~G0 Z5.39~~
~~G0 X3.57 Y-1.69~~
~~G0 Z5.29~~
~~M97~~
~~M30 P3.6~~
~~G1~~ X1.471 Y-1.692
~~M96~~
~~G0 Z5.39~~

→

(Electrode 2 Print Start)
G0 Z5.4
G0 X3.924 Y-0.095
G0 Z4.8
M97
M30 P24.4
F0.15 G1 Z5.1
F4.2 G1 X3.809 Y-0.665
X3.809 Y-1.692
X3.32 Y-1.692
M96
X1.471 Y-1.692
(Electrode 2 Print End)

Bracketed comments are placed either side of each Electrode Code block for reading ease when printing this section. The order of Electrode print should be maintained to as it was in the raw G-code output.

The last item to add is a purge line for the mechanical extruder printhead before the Electrode printing beings allowing for G-PDMS flow verification. This code block replaces all G-code between Line 13 and E4 Printing start of the B Base Section. If the purge line ends within 5mm of the Interface edge, shift the X-axis coordinates until it is. The purge G-code is as follows:

```
(Purge Line Start)
G76 Z0
M90 P3 D3
M95 P9
G0 X-23.5 Y1
G0 Z4.9
M97
M30 P10
F2.5 G1 X-13.5 Y1
M96
(Purge Line End)
```

A.2.4 Interface V5.2 Construction

The fabrication method of the Interface v5 Design will be presented in two sections – TEC Assembly fabrication, and Interface printing. Both sections can be performed in parallel up until B Base has been cured. At this point the two separate parts are bonded. It is advised that the TEC Assembly fabrication takes place first to enable one continuous flow for the Interface printing as the time frame for select steps are short.

TEC Assembly Fabrication

On a glass slide, tape down a single 1TC17-16178-1617.H (TECmicrosystems GmbH, DE) TEC unit using polyimide tape so that the solder pads are facing up and uncovered. Cut two 10cm lengths of CZ1105 wire (Cooner Wire, USA). Remove 2mm sheath section from one end on each length of wire. Line up the exposed wire ends with each TEC solder pad so that the wire sheath sits flush with the hot side. Trim the exposed wire down if it extends beyond the pad inner boundary. Once corrected, use the polyimide tape to hold the exposed wire ends in place on the solder pads. Mount a small chisel tip (4ETHL-1, Weller) onto a soldering iron (WE1010, Weller) and set the system to heat to 340°C. Melt a small bead of solder onto the tip of the soldering iron and then apply the bead directly to the exposed wire on one of the TEC pads. Hold it in place so as to deform the wire end flat but staying in the pad bounds. Wait until the solder flows off the soldering iron tip onto the wire and pad before quick removing the heat source off the connection. Repeat the same process for the other pad. Remove the TEC from the polyimide tape.

Mix 3g of the Silicone Adhesive and load into a 2ml syringe. Mount on a 27-gauge dispensing tip. Placing the needle end flush against the TEC side, inject the silicone adhesive into the TEC with the aim to fill all voids that exist within it. Once the inner spaces are filled, wipe away the excess Silicone adhesive so that the edge sits flush to the hot-side and cold-side edges. Place in the oven for 1 hour at 100°C to cure the Adhesive.

Using the same glass slide from soldering, cover a 25mm section with double sided tape. Remove the TEC from the oven and place it – hot-side down – in the centre of the taped piece. Clean the cold-side face of any residue with isopropyl alcohol. Select a 40AWG T-type thermocouple. On one end is the junction for sensing and the other end is left open for electrical connection. Trim the thermocouple length down to 150mm whilst keeping the junction end intact. The exposed junction now needs to be aligned centrally on the cold-side face with all exposed thermocouple wire located within the face boundaries. The thermocouple sheathed section should then trail off the face between the two TEC power wires. It should be bent to conform with the TEC side profile so that the wire sits on the same plane as the TEC power wires. Once aligned, dab a small layer of super glue on the thermocouple junction metal wire where it erupts from the sheathing and tack down the exposed junction onto the TEC cold-side face. Wait for the glue to dry and ensure that the thermocouple is siting flush to the cold-side face.

Place the cold-side Epoxy Silicone mould over the TEC. Check that the side fit flush to the TEC's perimeter. This prevents the Thermal Epoxy from leaking out of the mould. Mix 3g of the Thermal Epoxy. Load into a 2ml syringe with a 22-gauge dispensing tip attached. Slowly add the thermal epoxy to the Cold-side mould to prevent the formation of trapped air. Fill until the surface is level with the mould's top face. Place the working slide into a vacuum chamber. Keep the working slide under a sustained vacuum for 15 minutes to remove any trapped air in the epoxy layer then remove. Replenish the mould epoxy if required after air removal and then place the working slide in the oven to cure the thermal epoxy for 4 hours at 60°C.

Collect together a pair of tin snips, a scribe, and a steel rule. With the rule and scribe, etch a 6.3mm by 6.3mm square onto the surface of a 0.2mm Type 304 Stainless Steel foil (Fisher Scientific, UK) sheet. Cut the stainless-steel square out with the tip snips whilst using electronic callipers to constantly check dimensions and ensure edges remain parallel. After the correct dimensions have been achieved, add a ~0.5mm chamfer to the corners of the stainless-steel heat sink plate.

Mix 1g of the conductive silver epoxy. Cut a 100mm length of 36AWG wire. Strip a 2mm section from one end and bend into a small loop. Tape the heat sink plate down to a glass slide using the polyimide tape. Line up the wire hook so that it will sit in the bottom left corner of the heat sink plate and flush to the plate's surface. On the heat sink plate, cover the area where the wire will be placed with a thin layer of silver epoxy. Cover the wire loop in the silver epoxy and then tape it in place on the heat sink plate – do not cover the bonding area with tape. Add a small amount more of the silver paste to the wire area and smooth down so that it is only the thickness of the wire. Place the setup in the oven and cure for 1 hour at 150°C.

After the heat sink plate and the cold-side thermal epoxy have finished curing, remove both from their respective setups. With the glass slide coated with the doubled-sided tape, place the heat sink plate bare face down in the centre of the tape. On top of the plate, align and place the Heat Sink Jig Frame. Add a small drop of the thermal epoxy to the centre of the heat sink plate. Insert the TEC element in the Heat Sink Jig Frame's centre with the TEC hot-side facing down. Whilst pushing it into place, take the Heat Sink Jig Block and slot it into the Frame. Mount a clamp over the Block and tighten to apply enough pressure to hold it securely in place. Load the setup into the oven and cure for 4 hours at 60°C.

Remove from the oven, loosen the clamp, and demount the Heat Sink Jig elements. Select another 40AWG T-Type thermocouple and trim to 100mm. Align the thermocouple junction so that it sits to the right of the TEC hot side on the heat sink plate. Make sure that it is flush to the face and that the thermocouple wire snakes around to leave the plate where the TEC power wires, and cold-side thermocouple does. Lift the thermocouple off the plate. In the area the thermocouple is to be mounted, add a thin layer of thermal epoxy. Replace the thermocouple back to its selected location and cover in more thermal epoxy so that it insulates all exposed thermocouple wire. Hold the thermocouple in its location using tape. Place in the oven for 4 hours at 60°C to cure the thermal epoxy. The TEC Assembly build process is now complete.

Interface Printing

Before starting the Interface printing process, two items will need to be produced. Two glass slides will need to be coated with the Silicone Conformal Coating and the Printer Slide Mount will need to be printed using an FDM 3D printer. The mount used during this projects Interface production runs was printed out of a white PLA. Other PLA type materials are suitable to be used as substitute.

Mix a 4g batch of SE1700. Load the SE1700 into 33cc syringe until half full. Insert a green 33cc smooth flow piston after filling and compact the SE1700 down toward the extrusion end. Screw on a 0.234mm preci-tip nozzle to the syringe. Mount onto air pressure driven printhead on PH2 using the 33cc syringe adapter ring. Twist fit on the sealed air tube connector and lock the syringe in place using the neck screw.

Close printer front cover. Select PH2 on the printer's HMI. Run the Nozzle Length Measure process for the PH2 printhead ensuring that not material is being extruded from the dispensing tip before initiating. Wait for the process to complete. Using the keyboard's up arrow key, move the printing plate so that PH2's nozzle is not over the nozzle measuring sensor location and above the build area. On the HMI, enable the printhead pressure. Set PH2's pressure to zero on its display using its valve dial to the left of the printer's build area. Place a sheet of tissue below the PH2 nozzle's position. Activate continuous extrusion for PH2. Turning PH2's valve dial clockwise, set the pressure to 0.360MPa on its display. Leave the nozzle to extrude continuously for 20s to verify the correct flow is achieved. Deactivate the continuous extrude on PH2 and disable printhead pressure. Remove the tissue covered in extruded SE1700.

Load a coated slide into the Printer Slide Mount (PSM) with the coated side facing up. If excess slide movement is observed whilst in the mount, use a small section of tape on the slide edge to stabilise it. Mount the PSM in the Printer's build plate recess with the PSM slide insert direct facing away from the user. Close the Printer extraction window. Load the `v5.2_a_base.iso` file into the HMI. Verify the correct file is loaded. Click the HMI's print button. Observe the print process throughout. If the nozzle is to impact the slide, stop the printing process by pressing any keyboard key. Interface v5 A Base section should take 2min 10s to print. Remove the slide from the PSM. Place it in the oven. Cure the A Base section at 100°C for 40min. Remove the SE1700 syringe and place in a freezer to slow its curing.

At T-15mins till A Base section curing complete – begin the process of mixing 3g of the 50% Graphite PDMS Composite (Section A.1.5).

At T-5mins till A Base section curing complete – remove the SE1700-loaded syringe from the freezer to warm up.

Load 1ml of the composite into a 2.5ml glass Hamilton syringe. Insert a syringe plunger that contains the screw mount point for the mechanical extruder. Attach on a 0.335mm preci-tip nozzle. Mount the syringe into the mechanical extruder printhead on the PH3 position. Close the printer hood window. Select PH3 on the Printer HMI. Perform the Nozzle Length Measuring process. After, use the up-arrow key to move the print plate back. Open the printer hood window. Using the arrows on the HMI for PH3, move the mechanical extrusion plate down until it touches the Hamilton plunger. Turn the plate screw clockwise to join the two items. Continue to incrementally move the mechanical extrusion plate down until composite is seen extruding from the nozzle.

Remount the SE1700 syringe onto PH2 following the set-up procedure for it as described earlier. Remove the Interface print slide from the oven and place in the PSM ensuring it fits flush to the mount guides. The slide should be orientated so that the TEC wire channel is facing outwards from the printer towards the Printer hood window. Load the `v5.2_b_base.iso` file in the HMI.

Verify it is the correct version of the G-code modified for continuous printing. Click the HMI's print button and observe the print throughout. Pay particular attention in the Electrode printing process to the purge line print. If a constant flow rate is not reached by the mechanical extruder, stop the print, wipe away any printed composite on the slide, and restart the printing process. The Interface v5 B Base section should take 2min 30sec to print. Upon printing complete, remove the Interface slide from the PSM and place in the oven to cure for 1 hour at 100°C.

Remove both syringes from the printer. Place the SE1700 filled syringe into the freezer again to slow the curing process. If no more B Base sections are required to be printed, then purge the Hamilton syringe of any remaining graphite silicone composite and clean the syringe. The nozzle can be reused by placing it in the oven to cure the material and then, using a needle and small spatula, breaking apart the cured material within.

Whilst the Interface base is curing, cut four 10cm sections of ~36AWG wire (pl/ir or copper core used). On two lengths, strip 2.5mm of the sheath on one end. Bend this exposed end 90° where the edge of the sheath now is. On the other two lengths, strip 1.5mm of the sheath on one end. Bend these wires 90° 0.5mm into the sheathed section from where it was stripped to. This helps the wires lay next to each other in the Interface rather than overlap.

T-5mins before the Interface Base is cured, mix 2g of the Silicone Adhesive. Load this into a 2ml syringe. Attach a 0.406mmID dispensing nozzle to the syringe.

Once the curing is finished, remove the Interface Base slide from the oven. Along the slide edge which the TEC wire channel on the Interface faces, place a 30mm x 6mm section of double-sided tape. Collect up the wires previously stripped and bent. Using a pair of tweezers, insert the wires into the printed electrode wires. The 2.5mm stripped wires are paired with Electrode 1 and Electrode 3. The 1.5mm stripped wires are paired with Electrode 2 and Electrode 4. The wires must be inserted into the electrode wires through the walls along the TEC wire channel. Correct insertion is achieved when all exposed wire is inserted and none of the wire can be seen through the SE1700 layers (i.e. all of the exposed wire is encapsulated by the silicone composite to ensure maximum contact area exposure).

Stick the trailing electrode wires to the double-sided tape to hold them in place. Over the top taped wires, place a 15mm x 3mm section of electrical tape flush to the slide edge. Using the silicone adhesive, encapsulate wire length within the Interface bounds. Fill the space under the electrode wires and have it seal the insertion sites along the channel walls. The adhesive should form a film over the electrode wires – do not fill beyond that. Place the slide in the oven to cure for 1hr at 100°C. Place the silicone adhesive in the freezer.

Whilst the Interface is curing in the oven, take the TEC Assembly unit and move to a space with a fume hood. Apply the adhesive surface primer to surfaces of the TEC Assembly that will contact the Base Section. These include all sides of the TEC except the cold-side and the underside of the Heat Sink. Leave to dry in the fume hood. To prepare for bonding the TEC Assembly to the Base Section, coat a glass slide with the conformal coating and select a clamp.

Once the Interface has completed its curing cycle, remove it from the oven. Remove the silicone adhesive from the freeze and leave it to rewarm over 2 minutes. After, take the adhesive and apply it to the surfaces of the TEC Assembly that had been covered in the primer. Maintain at least a 0.5mm layer on these surfaces to fill any potential voids in the print. Take the TEC Assembly and the Interface print and place in the TEC Assembly such that the cold-side face is touching the printed sections glass slide and the TEC wires are routed through the channel. Take the other prepared slide and place the conformal face against the top of the printed part/Heat Sink. Using the clamp, apply pressure to the directly above the centre of the Interface print ensuring that an even force is applied. With the remaining silicone adhesive, guide its syringe nozzle into the TEC wire channel and fill until the adhesive is level with the Interfaces outer wall. The aim is to completely fill that channel. Once done, place the clamped unit into the oven for 1hr at 100°C. Place the remaining silicone adhesive back into the freezer.

Take the Interface unit out of the oven and remove the clamp Carefully remove the clamping slide from the Interface – it may be useful to use a spatula to help release it. There may be some silicone adhesive that seeped out to cover areas of the Heat Sink. Using a scalpel, carefully slice the excess adhesive off of the Heat Sink surface. Ensure that all excess is removed from the Heat Sink surface. Use the blades edge to scrape any excess away that has manifest as a thin film. Wipe the surface of the Heat Sink clean of any scraped remnants.

Take the SE1700-loaded syringe out of the freezer and let it rewarm to room temperature. Place the Interface print slide back into the PSM ensuring that the interconnect wires are all pointing towards the printer’s hood window. When the SE1700 has rewarmed, mount the syringe into PH2 and follow the previously detailed setup to account for any system changes. Load the `v5.2_c_fluidic.iso file` into the HMI. Verify it is the continuous printing processed file before continuing. Click the HMI’s print button and observe the printing throughout. The main issue to watch for is printing misalignment. The first layer of the Microfluidic Loop should cover the entire Heat Sink. If it doesn’t, the sequence needs to be halted, printed silicone wiped away, realignment performed, and print restarted. After printing is complete, remove the slide from the printer and place in the oven for 1hr at 100°C. Remove the SE1700 syringe. From the printing nozzle from it and store in the freezer for reuse and dispose of the rest of the syringe.

Silicone Tube Attachment

Remove the Interface from the oven. Gather a length of 0.4mmID/1.1mmOD silicone tubing. Cut two 100mm lengths of this silicone tubing using a scalpel and pack away the excess tubing for other use. Remove the silicone adhesive from the freezer and place on the side to rewarm. As it does, place the Interface on a flat surface. The inlet and outlet of the Microfluidic Loop are printed closed. They are required to be opened up for tube attachment. Each closed Loop port can be seen to protrude from the Loop structure towards the edge of the Interface where the interconnect wires exit its body. On each of these ports have an external wall that is needed to be sliced off. Using a scalpel, carefully slice these walls off by first cutting downwards from the top of the Loop ensuring that the blade cuts just behind each port's wall. Cut until the where the first print layer of the Loop. Then, to remove the wall, first grab a pair of tweezers and use them to grip the top of the port wall. With the scalpel in another hand, slowly cut along perpendicular to the Loop port wall at its base. Whilst cutting, slowly pull upwards on the wall with the tweezers until the wall is removed. Be very careful when performing this cut to remove the wall so as not to cut into the Loop any further than required.

Once the walls are removed, the silicone tubes need to be mounted in to the ports. Using the tweezers, practice inserting the tubing dry into the port openings if not performed before. It was found that sliding in the tube laterally is the easiest method. The tubes opening is placed against one of the port's left or right wall. As the hand holding the tube also applies some slight pressure on the tube to hold it against the base of the Loop channel, use the tweezers to grip and bend in the tubing from the side so that it slides into the port opening. Once confident with this, apply a ring of the silicone adhesive around the end of the tubing to insert ~0.5mm back from the tubes face. The adhesive is placed back from its face edge to reduce the likelihood of blocking the tubing when the insertion process is performed.

With the silicone adhesive now applied, perform the practiced action to insert the tube into the port. Once the tubing is within the Loop port opening, push it in so that the tube end is 1-1.5mm into the Loop. Repeat this insertion processes with the other tube. The Loops channel profile is designed such that it will exert enough of a hold on the tubing that it will remain in place once inserted, though careful handling is still required. Using the remaining silicone adhesive, deposit it around the edge where the Loops port meets the silicone tubing. Smear it into this edge using a spatula, not forgetting the underside of the tubing where it contacts the top of the Base Section. Once this external adhesive has been applied, place the Interface in the oven for 1hr at 100°C.

Remove the Interface from the oven. Now the Microfluidic Loop requires testing for any leaks. Fill a 10ml syringe with de-ionised water and attach a 22-gauge tip. Feed the tip pinto one of the silicone tubes and – with the other tube over a sink or container – perfuse the water through the Loop. Vary pressure applied to mechanically stress the Loop to ensure no leaks will form during variable flow rate use. If leaks appear or develop during testing, apply silicone adhesive to those areas, smooth them down with a spatula, and cure in the oven as before. Then repeat the Loop leak test to ensure they have been fixed. The silicone adhesive can now be disposed of and its nozzle cleaned for later reuse this.

After the tube testing is complete, the Interface's primary construction process is complete. Remove any tape that is holding down the Interface interconnect wires to the print slide. Then carefully remove the Interface from the print slide. It will be easier and safer to perform this with the flat end of a spatula. The conformal coating means that the silicone elements are easy to delaminate from the slide but the excessive bending of the Base Section could also delaminate the SE1700 from the TEC Assembly. It is best to wedge the spatula underneath the Interface and then slowly release small sections of it form the slide to completely remove it. The last action on the Interface main body is to agitate the electrode faces. A thin layer of the PDMS component in the composite is seen to form a thin skin on the outer print surfaces of the cured material. Thus, it is necessary to agitate this skin to break it apart and expose the graphite flakes to lower the electrodes impedance. To do this, pick up a scalpel and move the blade across the surface of an electrode with a scraping motion such that the blade is pointing 45° away from the direction of travel. Only perform this action until the electrodes look noticeably duller then when they were freshly printed. Wipe away any debris formed. Now the Interface body build process and preparation is complete. All that is left to perform is soldering the Omnetics connector onto the Interface's interconnect wires.

A.2.5 Interface Connectorisation

Each Interface connector is attached by hand using 0.5mm Lead-Free Solder (T0051388499, Weller), flux (REL0 No-Clean, ChipQuik) and soldering iron (WE1010, Weller) mounted with a small chisel tip (4ETHL-1, Weller). For the Interface connector, an Omnetics MCP-SS-12 is used and for the Interface-to-Board wire, an Omnetics MCS-SS-12 is used.

Refer to the Interface interconnect layout guide for description on pin locations. To prevent damage to the thinner wires solder them in this order: TEC Wires; Electrode Wires; Thermocouple Wires. After soldering the connected is potted to provide mechanical stability at the solder joint. The PDMS Connector Potting Mould will be required for this. This mould is fabricated by taking a negative cast of the Omnetics micro360 12pin plug connector using PDMS.

The following steps are how the solder-cup variants of the Omnetics connectors were attached. Trim the Interface interconnect wires all to the length of the shortest wire. By scraping a scalpel along the wire at 45° from the direction of travel, remove a 1.5mm length of sheath off each wire. Form the TEC Power, Electrode 1/4, and Electrode 2/3 wires into twisted pairs. Turn on the soldering iron and set to 340°C. Inject flux into each solder cup – following the pin layout provided in the main text – until they are half full. Mount the connector and Interface in a set of helping hands. To aid mounting the interface, wrap electrical tape around the interconnect bundle to create a lip for mounting with.

Take a wire and insert it into the solder cup ensuring it remains there without being manually held in place. Apply a small bead of solder to the tip of the soldering iron. Place and hold the soldering iron tip on the solder cup. Allow time for the cup to heat up and the solder flow from the iron into the cup until it is filled. Prevent bridging between cups by ensuring the iron tip only touches one cup at a time. Repeat this soldering process for all wires until they have all been soldered into their respective positions. Handle with extra care once the electrode and thermocouple wires have been attached.

Prepare 3g of the thermal epoxy. Mount the connector into the Connector Potting Mould so that the connector back is at least 6mm from the mould opening. Pour the thermal epoxy into the mould filling it until the epoxy is level with the opening. Place the interface and mould into a vacuum chamber for 30 minutes to remove trapped air caused by the pouring. Remove from the vacuum chamber and cure in an oven for 4 hours at 60°C. De-mould the connector and deburr the cured epoxy edges.

A.2.6 Electrode Plasma Treatment

Plasma activation of the Interfaces Graphite-PDMS electrodes is performed 1 hour before the Interface is used *In Vivo* and mounted on the rat model. To perform this, a cold-plasma producing device, PiezoBrush PZ3-i (Relyon Plasma, Germany) is mounted on printhead 5 in the 3D Discovery printer. This printhead does not have its own air supply on the used printer. Instead, the air supply for printhead 4 was diverted to the plasma rig. Air pressure activation control was enabled through selecting printhead 4 on the HMI software, enabling air flow, and then deselecting printhead 4. Plasma strength control is achieved using the analogue signal input on the plasma rig controller - a box with a potentiometer and switch that allow the user to activate and tune the plasma strength whilst the printer is in motion.

To treat the electrodes, first select the Interface required to be surface activated. On a glass slide, attach a piece of double-sided tape - no smaller than the Interface - in a central position that is ⅔ along the length of the slide. Place the slide in the Printing Slide Mount with the taped side facing up. Adhere the Interface to the tape such that the electrodes are also facing up and then mount the PSM in the Printer.

Check the plasma rig controller is correctly hooked up to the plasma rig. Take the plasma controller out of the printer hood for access during movement. On the HMI select PH4 and activate the printhead pressure. Tune the PH4 pressure – using the dial on the right of the printer – until the PH4 display reads 0.100MPa. Without halting the printhead pressure, deselect PH4 as the active printhead by clicking the 'X' to the right of the printhead selection row on the HMI. Close the printer fume hood.

Use the keyboard arrows to line the plasma rig up with the centre of electrode 1. Use the 'Page Down' key to lower the Rig until it is 2mm above electrode's surface. Set the potentiometer on the plasma rig Controller to 80% power and then switch the plasma on. With continuous movement selected on the HMI, have the plasma rig move over the Interface electrodes in a 'circular' motion of the order E1-E3-E4-E2. Either have the 0.1mm/s button selected or press the required directional key twice to have the plasma rig in constant motion. Repeat this motion thrice or until each Interface electrode has experienced plasma discharge for >20s.

Turn the plasma rig off once this motion complete. Move the printheads vertically so that they are 10cm from the print bed. Select PH4 on the HMI and turn off the printhead pressure flow. Wait 1 minute for the printer's extractor to remove any cold plasma-generated ozone. Open the printer's fume hood. Unmount the PSM from the print bed. Unstick the Interface from its glass slide being careful not to interact with the - now activated - electrodes surfaces and store for later experimental use.

Appendix B
BioCAD Printing Profiles

Material	Interface Version	BioCAD				3D Discovery Printer & HMI				
		Feed Rate	Thickness (mm)	Extrusion Type	Delay (1/16s)	Nozzle Size (mm)	Air Pressure (MPa)	Syringe Volume	Volume Flow Rate (µL/s)	Plunger Velocity (mm/s)
SE1700 Base	v1	7.0	0.380	Pneumatic	400	0.457	0.320	33cc	null	null
SE1700 Liquid Cooling	v1	11.0	0.370	Pneumatic	400	0.457	0.320	33cc	null	null
Thermal Silicone [50%]	v1	6.0	0.400	Pneumatic	300	0.859	0.340	33cc	null	null
Thermal Silicone [50%]	v2	4.0	0.200	Pneumatic	150	0.859	0.380	33cc	null	null
SE1700 Base	v2, v3, v4, v5	5.0	0.210	Pneumatic	300	0.234	0.340	33cc	null	null
SE1700 [90°]	v2, v3, v4, v5	5.5	0.228	Pneumatic	300	0.234	0.340	33cc	null	null
SE1700 [45°]	v2, v3, v4, v5	5.5	0.162	Pneumatic	300	0.234	0.340	33cc	null	null
Graphite Silicone [50%]	v4, v5	4.0	0.220	Mechnical	200	0.335	null	2.5ml	1.09956	0.014

Appendix C
COMSOL Material Profiles

Material	Density (kg/m^3)	Thermal Conductivity (W/m.K)	Heat Capacity (J/kg.K)	Electrical Conductivity (S/m)	Ratio of Specific Heats	Dynamic Viscosity (Pa.s)	Relative Permittivity	Youngs Modulus (Pa)	Coefficient of Thermal Expansion @ 20°C (10-6/K)
RS Pro Thermal Grease	3000	2.9	1500	1.00E-14	n/a	45	n/a	n/a	n/a
Thermal Epoxy - T7110	2010	1.3	960	1.00E-14	n/a	n/a	n/a	n/a	n/a
PDMS	970	0.15	n/a	2.5E-14	n/a	n/a	n/a	15000	907
Stainless Steel 316L	8000	14.5	500	13514	n/a	n/a	n/a	1.93E+11	16.5
Cerebrospinal Fluid	1007	0.57	4096	2	1	0.000784	10.9	n/a	n/a
Brain (Average)	1046	0.51	3630	n/a	n/a	n/a	n/a	n/a	n/a
Aluminium Nitride	3260	180	740	1E-14	n/a	n/a	n/a	3.30E+11	4.5
Water-Agar Gel	1005	0.5316	4200	n/a	n/a	n/a	n/a	n/a	n/a

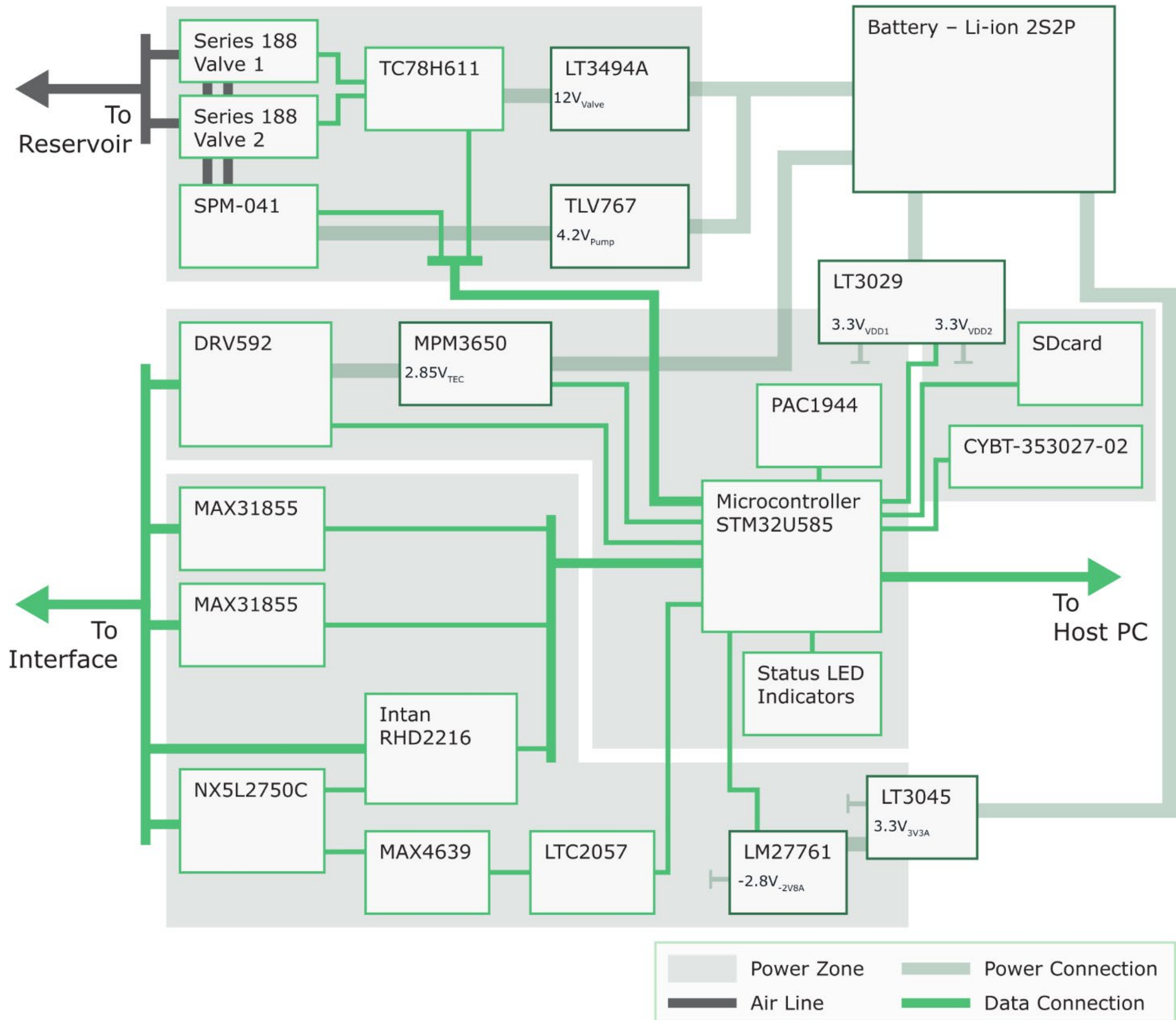
Appendix D
Interface v5 Printing Clips

Interface v5 A Base Section Printing

Interface v5 B Base Section Printing

Interface v5 C Fluidic Section Printing

Appendix E
Expanded Electronic Block Diagram



Appendix F
Low-Pass Filter Transfer Function

A passive low pass filter is placed on the output of the TEC driver to smooth the driving signal so that it is DC and to supress the formation of ripple currents within this DC signal.

$$H(j\omega) = \frac{Z_1}{Z_1 + Z_2} \tag{E.1}$$

Where

$$Z_1 = R + j\omega L \tag{E.2}$$

$$Z_2 = \frac{1}{j\omega C} \tag{E.3}$$

Expanding (E.1) gives

$$H(j\omega) = \frac{\frac{1}{j\omega C}}{R + j\omega L + \frac{1}{j\omega C}} \tag{E.4}$$

Multiple (E.4) through by $j\omega C$

$$H(j\omega) = \frac{1}{(j\omega)^2 LC + j\omega RC + 1} \tag{E.5}$$

Divide (E.5) through by LC

$$H(j\omega) = \frac{\frac{1}{LC}}{(j\omega)^2 + j\omega \frac{R}{L} + \frac{1}{LC}} \tag{E.6}$$

For a RLC circuit, the Quality Factor can be represented by

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{\omega_O L}{R} = \frac{1}{\omega_O RC} \qquad \text{E.7}$$

Substitute (E.7) into transfer function such that

$$H(j\omega) = \frac{\omega_O^2}{(j\omega)^2 + j\omega\frac{\omega_O}{Q} + \omega_O^2} \qquad \text{E.8}$$

Divide through (E.8) by ω_O

$$H(j\omega) = \frac{1}{\left(\frac{j\omega}{\omega_O}\right)^2 + \frac{1}{Q}\frac{j\omega}{\omega_O} + 1} \qquad \text{E.9}$$

Perform a rearrangement on the squared term in the denominator

$$H(j\omega) = \frac{1}{-\left(\frac{\omega}{\omega_O}\right)^2 + \frac{1}{Q}\frac{j\omega}{\omega_O} + 1} \qquad \text{E.10}$$