Optimal Control of Multilevel Flying-Capacitor Converters

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Abstract

This thesis is concerned with the flying-capacitor multilevel power converter topology. This converter is one of several different static power converter circuits which can produce three or more distinct voltage levels at the output terminals. All multilevel converters are constructed from semiconductor power switches which have a lower voltage rating than the maximum terminal voltages, and so are generally used in high power, medium voltage applications. Flying-capacitor converters have internal floating capacitors which provide voltage clamping of the power switches. To ensure correct operation, the internal capacitor voltages have to be at specific balanced levels and this poses a major challenge in the control of the flying-capacitor converter.

The main objective of this work was to investigate the control of a three-phase flying-capacitor inverter, and identify optimal modulation strategies which would improve the output power quality by minimising the harmonic content of the output waveforms. As part of this investigation, suitable capacitor voltage balancing strategies for incorporation within the modulation control system had to be identified. It was also the intention of the work to quantify the effect on performance of different capacitor ratings, in order to provide a definitive guide to selecting components for a practical inverter.

Simulations of various forms of multilevel sinusoidal modulation are presented in the thesis. The modulation schemes covered are selective harmonic elimination (SHE), sine-triangle PWM and space vector PWM. In the flying-capacitor inverter, there are a variety of different implementations possible for each scheme due to the increased number of synthesisable output voltage levels. The relative merits of the different modulators are assessed based on output power quality, and this is done in respect to the novel capacitor voltage balancing strategies developed for each scheme. To aid this investigation, a detailed simulator program has been developed which incorporates realistic models of the inverter system and digital controller.

The investigations into SHE control have revealed that a switching state rotation pattern can be optimally selected to balance the capacitor voltages and actually reduce the harmonic content of the output in the case of practically sized capacitors. System characteristics are presented which can enable the selection of the capacitors based on the load characteristic in order to optimise the performance of the practical inverter.

An in-depth investigation into the various sine-triangle PWM carrier placement options, reference sampling methods and hardware implementation issues known in the literature has been carried out. The results show the effect of the various implementations on output power quality and a comparative assessment is presented in the context of practical sized capacitors. A novel digital hardware-based capacitor

voltage balancing control scheme is proposed and shown to work well without the need of voltage sensors on the capacitors.

Space vector PWM is investigated and a very simple approach to computation of the duty cycles using a carrier-based implementation to generate the space vector firing pattern is presented. It is shown to give the same results as more complex algorithms adopted in the past, aimed at the selection of the synthesising vectors from the large number of switching state vectors in the multilevel inverter. The novel PWM balancing strategy ensures that the inverter operates correctly in a balanced state.

An experimental three-phase, five-level inverter has been constructed and used to confirm the validity of the simulation work. Results presented show that the inverter operates correctly, with balanced capacitor voltages, under all forms of sinusoidal modulation control.

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List of Principle Symbols

Symbol	Meaning	Units
N	number of inverter cells	
V_{dc}	dc link voltage	Volt
V_{level}	inverter level voltage	Volt
V_1	fundamental voltage	Volt
f_1	fundamental frequency	Hertz
ω_1	angular fundamental frequency	radian/s
ϕ	angular displacement between voltage and current fundamentals	radian
$cos\phi$	displacement power factor	
α	control firing angle	radian
m_a	amplitude modulation index	
m_f	frequency modulation index	
D	PWM duty cycle	
T_s	PWM switching period	second
$\mathbf{V}$	voltage space vector	Volt
m	voltage level	
LEV	number of states	
SEQ	number of switching sequences	
P	number of patterns	
B	number of balancing cycles	
$\mathbf{V_C}$	cell-capacitor voltage vector	Volt
$\mathbf{J}$	Jordan switching state control matrix	
$\mathbf{S}$	switching state vector	
$\mathbf{C}$	capacitor matrix	$Farad^{-1}$
E_c	energy stored in a unit cell-capacitor	Joule
ξ	energy factor	s^{-1}

All others symbols have their usually accepted meaning.

List of Abbreviations

AFE	active front-end
APOD	alternative phase opposition disposition
ASIC	application specific integrated circuit
CAD	computer-aided design
CLK	clock
CSI	current source inverter
DF1	distortion factor 1
DF2	distortion factor 2
DPF	displacement power factor
DPS	disposed phase shift
DSP	digital signal processor
EMC	electromagnetic compatibility
FACTS	flexible alternating current transmission system
FFT	fast Fourier transform
FPGA	field programmable gate array
GTO	gate-turn-off thyristor
GUI	graphical user interface
HPS	hybrid phase shift
HVDC	high-voltage direct current
IGBT	insulated gate bipolar transistor
IGCT	insulated gate-commutated thyristor
SCR	silicon controlled rectifier
MOSFET	metal oxide semiconductor field effect transistor
MUX	multiplexer
NPC	neutral point clamped
OOP	object oriented programming
PCB	printed circuit board
PD	phase disposition
PF	power factor
PFC	power factor correction
PI	proportional integral
PIN	positive-intrinsic-negative
PLL	phase locked loop
POD	phase opposition disposition
PS	phase shift
PWM	pulse width modulation
RFI	radio frequency interference

ROM	read-only memory
STATCOM	static compensator
SHE	selective harmonic elimination
SHE-4H2	SHE four cell two harmonics
SHE-4H4	SHE four cell four harmonics
SMPS	switched-mode power supply
SPD	shifted phase disposition
SPOD	shifted phase opposition disposition
SPWM	sinusoidal pulse width modulation
SVPWM	space vector pulse width modulation
THD	total harmonic distortion
TPF	true power factor
UPFC	unified power flow controller
UPLC	universal power line conditioner
UPS	uninterruptible power system
VAr	volt-ampere reactive
VCOX	voltage controlled oscillator crystal
VHDL	VHSIC hardware description language
VHSIC	very high speed integrated circuit
VSI	voltage source inverter
WTHD	weighted total harmonic distortion
ZCT	zero current transition
ZVT	zero voltage transition

Chapter 1 INTRODUCTION

1.1 Electronic Power Conversion

Electronic power converter technology has progressively become a key component in energy generation, transmission, distribution and point of load utilisation. Commercialisation has been driven by advances in first valve electronic and more recently semiconductor technology, opening up opportunities for processing energy far more efficiently by using switching control techniques.

Power can be transmitted by either direct current or alternating current and so there are four basic forms of power conversion required to control and convert it from one form into another [1.1]. These forms of conversion are:

- ac voltage to dc voltage (rectification)
- dc voltage to ac voltage (inverted rectification or inversion)
- dc voltage to dc voltage (dc conversion)
- ac voltage to ac voltage (ac conversion)

System performance as measured by efficiency, reliability and cost is dependent on the optimum selection of operating voltage. It has been accepted since the early days of power distribution that the higher the power, the higher the voltage. This philosophy is true also for electronic power conversion. Therefore as the system power is increased, it is desirable to operate at as high a voltage as possible. The main practical limitation is then set by the available power semiconductor switch technology. Presently, gate-turn-off thyristors (GTO) and diodes are commercially available with blocking voltage ratings of up to 10 kV [1.2]. These older generation devices have limited switching speed capabilities, but newer technology such as insulated gate bipolar transistor (IGBT) and insulated gate-commutated thyristor (IGCT) are becoming available with 6.5 kV voltage ratings. Intense research is on-going to improve both speed and blocking voltage capability, and wide band-gap silicon carbide devices offer promise in the future [1.3]. At present, the device options for medium voltage and high voltage applications are limited and so methods of utilising lower voltage devices in high voltage applications are needed to optimise the system performance.

Series connection of power devices has enabled practical systems to be developed with high maximum operating voltages. However, there are practical problems in

achieving proper voltage sharing under all conditions [1.4]. A better approach is to limit each switch voltage by clamping to a dc voltage source. Over the last 30 years, several converter topologies have been developed which make use of intermediate voltage levels within the power converter, and offer advantages over the single combined switch approach. These multilevel converter approaches have the additional advantage of offering improved waveform quality through increased voltage levels at the output. This flexibility offers component size reductions for filtering the output and allows lower operating switching frequencies in each power device. The added complexity, though, presents major practical design challenges in both component selection and optimal control.

Multilevel converters [1.5, 1.6] represent the latest developments in power electronic converter circuitry, and have opened up hitherto impractical high power applications. Electronic control of very high-power, variable speed drive systems and power conditioning systems for enhancing the quality of the existing high-voltage power distribution networks are the two main application areas where multilevel converters will play a significant role in the future. The integration of alternative renewable energy sources within the power distribution infrastructure will also be aided by these newer forms of power converter.

The work described in this thesis contributes to the understanding and resolution of some of the issues regarding higher power conversion techniques, with specific emphasis on one form of multilevel inverter, namely the flying-capacitor inverter. This chapter provides an overview of multilevel technology and identifies the key issues faced when developing an inverter for a specific application.

1.2 Multilevel Converter Topologies

Multilevel converters are a relatively new class of power switch topologies aimed at high power applications such as motor drives and static power conditioning systems. Conventional two-level inverters, such as the full-bridge inverter, operate by applying either full positive or full negative dc link voltage to the load terminal. Control of the applied voltage pulse width can then be used to modulation the mean amplitude of the output voltage with respect to time.

Multilevel converters have an increased number of power switches, configured so that an increased number of voltage levels can be applied to the load. The extra degrees of freedom in modulation strategy can be used to improve upon the performance offered by a standard inverter. In the case of a dc voltage-fed, voltage source inverter (VSI), it can then be controlled in a simple manner to synthesise an approximated sinusoid

from the available voltage level states. The quality of the sinusoidal load current and voltage can be further improved by the use of PWM techniques during each voltage level switching state, making filtering far more cost effective.

Achieving multilevel voltage operation in practice requires the arrangement of power switches and passive storage elements in a basic bridge configuration. There are three main types of multilevel inverter topology [1.7, 1.8], which can achieve this:

- Diode-clamped
- Flying-capacitor
- Cascaded-cell

1.2.1 Diode-Clamped Converter

The extension of a bridge inverter circuit to multiple voltage levels with diodes used to constrain the maximum voltage across the power switches to safe operating levels was first proposed independently by Baker [1.9, 1.10] and Nabae et al [1.11]. This three-level inverter circuit is commonly known as the neutral point clamped (NPC) inverter, while the general class of these multilevel inverters are referred to as diode-clamped or multipoint-clamped inverters [1.12 – 1.15].

Figure 1.2.1 shows the three-level diode-clamped converter topology in a full-bridge arrangement, offering five separate output voltage levels across the load. Fundamental to the circuit's operation are the two capacitors which provide a mid-point voltage in the dc link, and the four diodes, D_{a1}, D_{a2}, D_{b1} and D_{b2}, which clamp the voltage nodes between series connected switches to the dc link mid-point. The nine allowable switching states for the bridge inverter are listed in Table 1.2.1 together with the resultant voltage level across the load. A '1' indicates that the switch is on and '0' indicates off. The power switches in each inverter phase limb can be grouped into two complementary pairs, (S_{a1}, S_{a3}) and (S_{a2}, S_{a4}), so that when one switch is on the other must be in the off state. The state when S_{a1} and S_{a4} are on is not allowed since this leads to an over-voltage condition across the other two switches.

The diode-clamped inverter can be easily extended to more levels, and Figure 1.2.2 shows the four-level and five-level versions of one phase limb. An additional complementary switch pair for each extra voltage level is added to the inverter limb. Extra capacitors in the dc link are also required to increase the number of voltage points for clamping purposes. Additional diodes are then used to clamp the extra inter-switch voltage nodes. The maximum reverse blocking voltage of each clamping diode depends on its position in the circuit, and therefore the figures illustrate the use of diodes with the same voltage rating as the switches. As the number of capacitors in the

link increases with higher numbers of voltage levels, it is more of a problem to ensure that the capacitor voltages are balanced, and the cost of the large number of clamping diodes is a drawback.

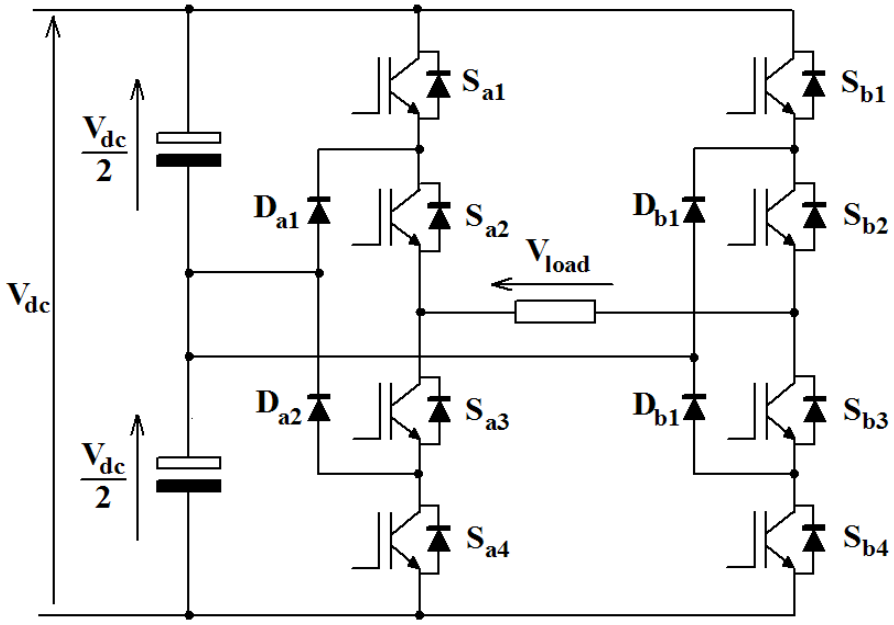
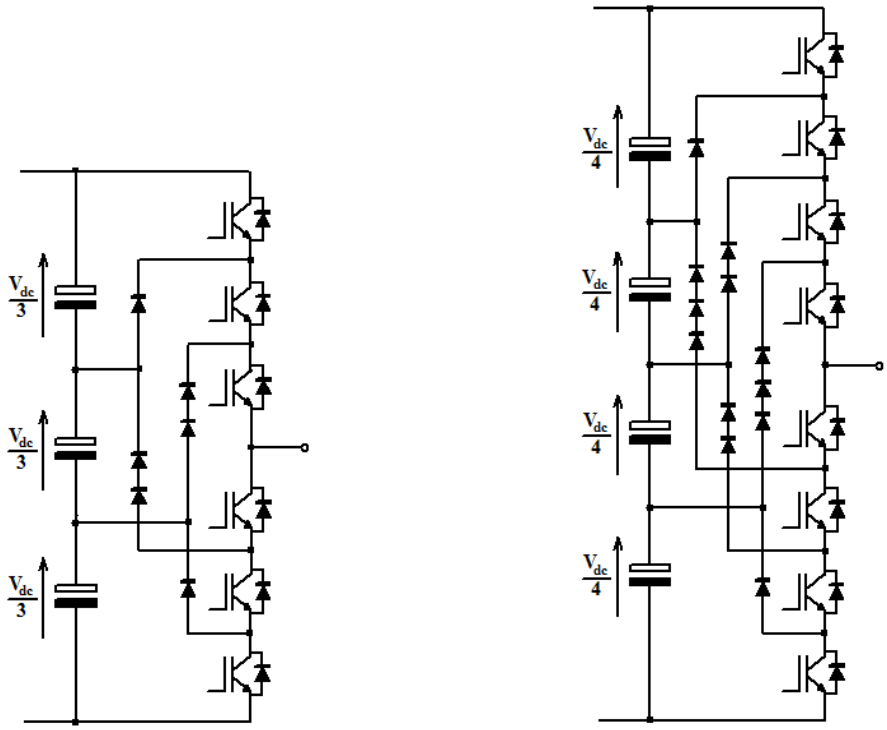


Figure 1.2.1: Five-level diode-clamped bridge inverter

Phase A Switches				**Phase B Switches**				V_{load}
S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{b1}	S_{b2}	S_{b3}	S_{b4}	
1	1	0	0	0	0	1	1	$+V_{dc}$
1	1	0	0	0	1	1	0	$+V_{dc}/2$
0	1	1	0	0	0	1	1	$+V_{dc}/2$
1	1	0	0	1	1	0	0	0
0	1	1	0	0	1	1	0	0
0	0	1	1	0	0	1	1	0
0	1	1	0	1	1	0	0	$-V_{dc}/2$
0	0	1	1	0	1	1	0	$-V_{dc}/2$
0	0	1	1	1	1	0	0	$-V_{dc}$

Table 1.2.1: Five-level diode-clamped bridge inverter switching states



a) Four-level **b) Five-level**

Figure 1.2.2: Diode-clamped multilevel inverter limbs

1.2.2 Flying-Capacitor Converter

The capacitor-clamped multilevel converter is an alternative topology where the clamping diodes are removed and floating capacitors are used instead to clamp the node voltages in the series connected power switches. The floating-capacitor concept can be traced back to circuits developed in the 1960s. The single flying capacitor converter was first proposed by Simon and Bronner [1.16] and IBM researchers [1.17], and the two-level chopper using the capacitor energy transfer mechanism was disclosed by Singer et al. [1.18] in the 1970s. These charge pump circuits are still used today for low power dc voltage conversion.

Present interest in the circuit as a multilevel converter stems from the work of Meynard and Foch [1.19, 1.20] who applied the basic switched capacitor bridge principle to enable voltage clamping in multiple level power converters. The converter has been variously referred to as the imbricated-cell or multicell topology, but it is now more popularly known as the flying-capacitor multilevel converter.

Figure 1.2.3 shows the three-level flying-capacitor converter topology in a full-bridge arrangement, offering five separate output voltage levels across the load. The capacitor voltage is half the dc link voltage and therefore all the power switches block only half the dc link voltage. Table 1.2.2 lists all the switching state modes and

resultant synthesised load voltage for the bridge inverter circuit. There are more allowable switching states than the diode-clamped inverter, and again the switches are grouped into two complementary pairs, (S_{a1}, S_{a4}) and (S_{a2}, S_{a3}), so that when one switch is on the other must be in the off state. This is essential for avoiding a shoot-through condition in the inverter.

The topology is scaled for higher numbers of voltage levels by adding additional cells consisting of a complementary switch pair and capacitor. Figure 1.2.4 shows the four-level and five-level versions of a single phase inverter limb. The circuits illustrated use identically rated capacitors throughout, so therefore the capacitor numbers increase significantly as the number of voltage levels goes up. This is potentially a major drawback in this form of multilevel inverter, since the capacitors are likely to be bulky and costly.

Maintaining the correct voltage across the floating- or cell-capacitor is the main challenge in ensuring proper operation of the inverter. When any intermediary voltage is being synthesised, there is a current path through one or more of the cell-capacitors, which will cause charging or discharging depending on the overall state of the switches and the load current polarity. Therefore the inverter control must ensure that the cell-capacitor voltages are balanced through the proper selection of the switching state combinations.

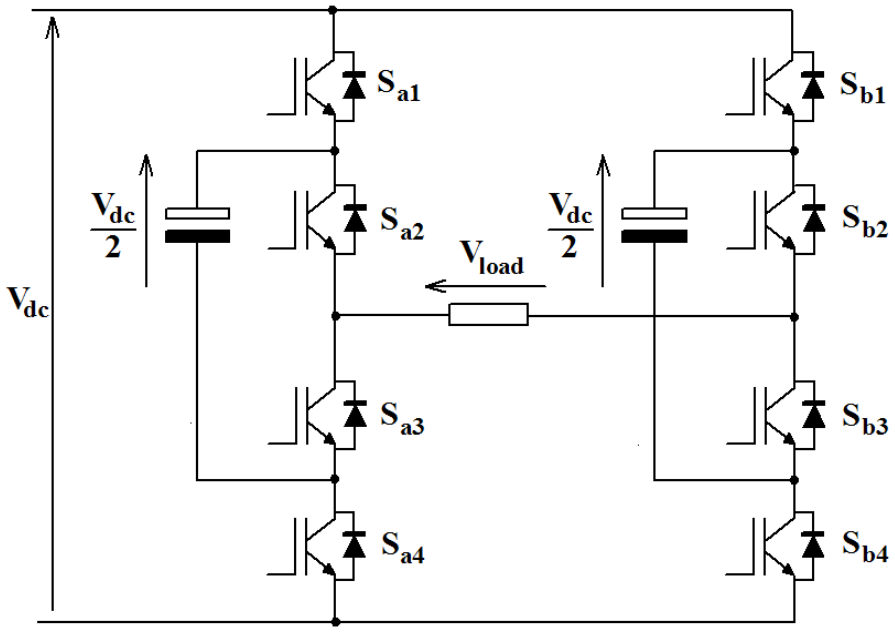
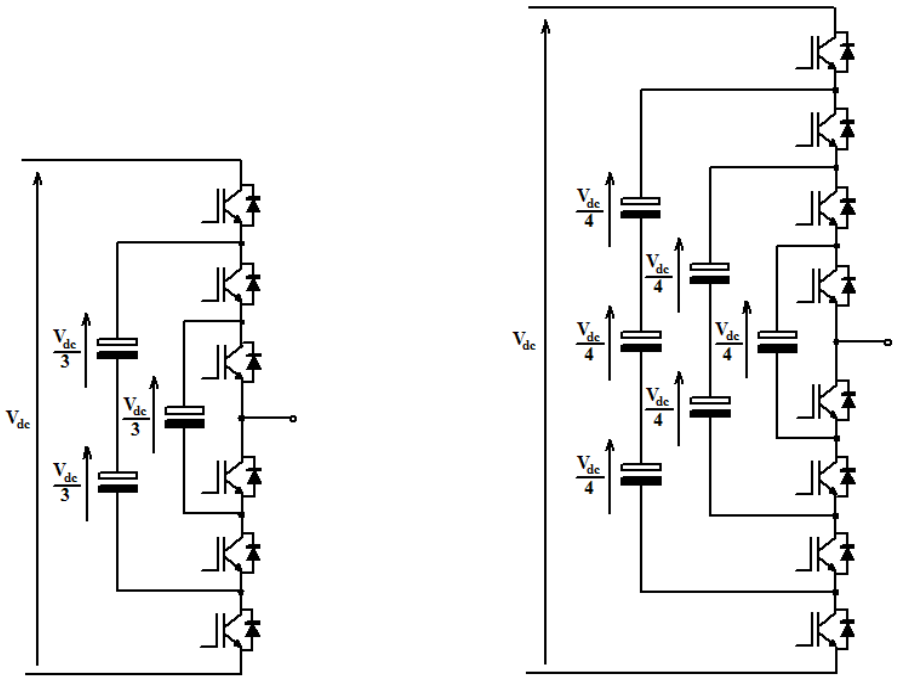


Figure 1.2.3: Five-level flying-capacitor bridge inverter

Phase A Switches				Phase B Switches				V_{load}
S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{b1}	S_{b2}	S_{b3}	S_{b4}	
1	1	0	0	0	0	1	1	$+V_{dc}$
1	1	0	0	1	0	1	0	$+V_{dc}/2$
1	1	0	0	0	1	0	1	$+V_{dc}/2$
1	0	1	0	0	0	1	1	$+V_{dc}/2$
0	1	0	1	0	0	1	1	$+V_{dc}/2$
1	1	0	0	1	1	0	0	0
1	0	1	0	1	0	1	0	0
1	0	1	0	0	1	0	1	0
0	1	0	1	1	0	1	0	0
0	1	0	1	0	1	0	1	0
0	0	1	1	0	0	1	1	0
1	0	1	0	1	1	0	0	$-V_{dc}/2$
0	1	0	1	1	1	0	0	$-V_{dc}/2$
0	0	1	1	1	0	1	0	$-V_{dc}/2$
0	0	1	1	0	1	0	1	$-V_{dc}/2$
0	0	1	1	1	1	0	0	$-V_{dc}$

Table 1.2.2: Five-level flying-capacitor bridge inverter switching states



a) Four-level **b) Five-level**

Figure 1.2.4: Flying-capacitor multilevel inverter limbs

1.2.3 Cascaded-Cell Converter

The cascaded multilevel topology uses several individual full-bridge inverter elements connected in series. One the earliest proposed circuits using the series connection of inverter bridges can be found in a late 1980s paper by Marchesoni et al. [1.21]. In the mid 1990s this circuit using multiple low-voltage inverter cells connected in series was commercialised by Rubicon, notably by their engineer Hammond [1.22, 1.23], for use in high power ac drives.

The basic five-level cascaded-cell inverter is shown in Figure 1.2.5. This circuit features two conventional full-bridges serially connected together with their power rails connected to separate isolated dc voltage supplies. Each full-bridge inverter cell can apply three voltage levels to the load terminals and the complete set of operating states for this circuit are listed in Table 1.2.3, together with the resultant synthesised load voltage. The switch complementary pairs are (S_{a1}, S_{a2}) and (S_{a3}, S_{a4}) in this case to avoid a shoot-through condition.

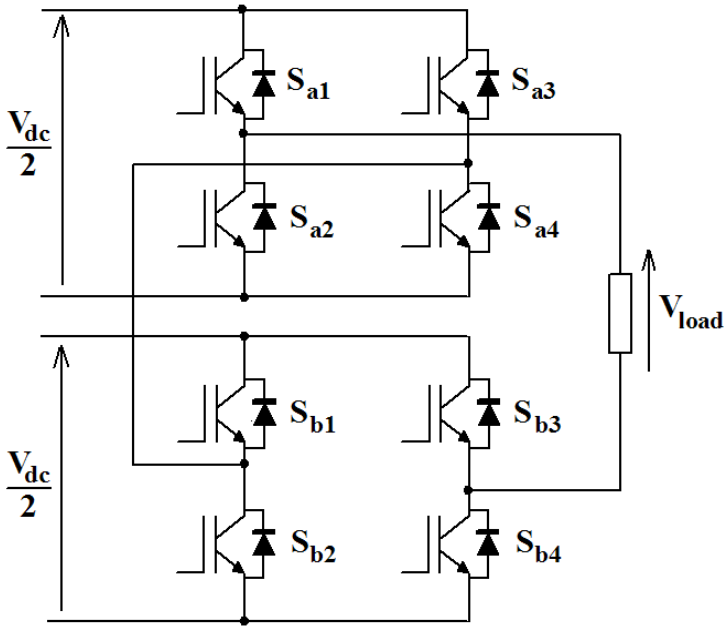


Figure 1.2.5: Five-level cascaded-cell bridge inverter

Phase A Switches				**Phase B Switches**				V_{load}
S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{b1}	S_{b2}	S_{b3}	S_{b4}	
1	0	0	1	1	0	0	1	$+V_{dc}$
1	0	0	1	1	0	1	0	$+V_{dc}/2$
1	0	0	1	0	1	0	1	$+V_{dc}/2$
1	0	1	0	1	0	0	1	$+V_{dc}/2$
0	1	0	1	1	0	0	1	$+V_{dc}/2$
1	0	0	1	0	1	1	0	0
1	0	1	0	1	0	1	0	0
1	0	1	0	0	1	0	1	0
0	1	0	1	1	0	1	0	0
0	1	0	1	0	1	0	1	0
0	1	1	0	1	0	0	1	0
0	1	1	0	1	0	1	0	$-V_{dc}/2$
0	1	1	0	0	1	0	1	$-V_{dc}/2$
1	0	1	0	0	1	1	0	$-V_{dc}/2$
0	1	0	1	0	1	1	0	$-V_{dc}/2$
0	1	1	0	0	1	1	0	$-V_{dc}$

Table 1.2.3: Five-level cascaded-cell bridge inverter switching states

The circuit shown also represents one phase limb of an inverter where each lower inverter-cell load connection is connected together in a three-phase inverter, resulting in a nine-level line-to-line voltage waveform. The voltage level of the inverter can be increased in multiples of two by adding additional bridge inverter cells to each phase limb. Therefore, there is no direct equivalent to the four-level diode-clamped and flying-capacitor inverters.

The cascaded inverter uses the least number of power components, but requires separate isolated power sources for each inverter cell. This would normally entail using a large isolation transformer. However, the topology does look attractive for power conditioning applications where the separate dc supplies can be self-powered in the converter.

1.2.4 Alternative Multilevel Inverters

Some additional work has also been done on combining the different voltage clamping techniques to form more complex hybrid topologies. The diode- and capacitor-

clamped topologies can be used as the basic inverter elements in a cascaded cell topology. For example, Kumar and Kim have described the use of three-level, NPC inverters combined in a cascaded-cell arrangement [1.24]. Peng [1.25] reports a generalised multilevel inverter structure which can be fashioned with both diode clamps and flying-capacitors from which a variety of different topologies can be derived. Figure 1.2.6 illustrates a four-level generalised multilevel inverter structure.

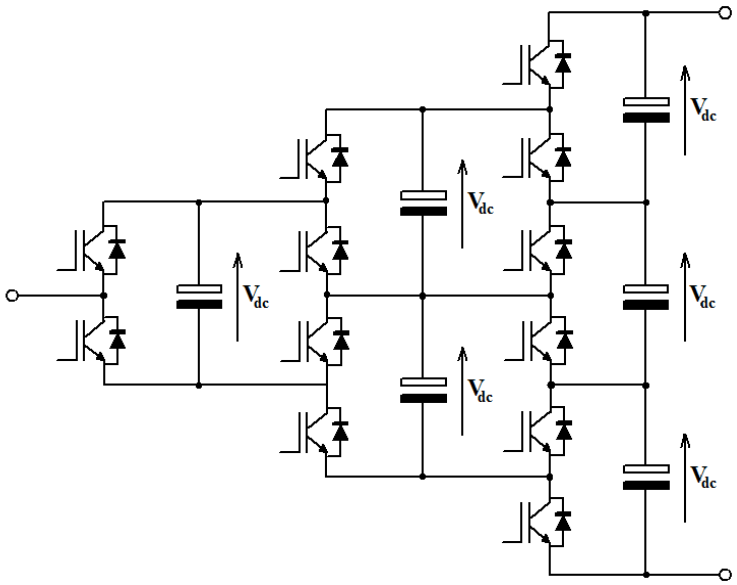


Figure 1.2.6: Generalised four-level converter structure

An early form of multilevel inverter, suggested by Bhagwat and Stefanovic [1.26], was the use of a chain of capacitors and then selectively switching the different voltage points to the load. The main disadvantage of this circuit is the need for high blocking voltage switches connecting the load terminal to the outer capacitors.

Lipo et al. [1.27, 1.28] have reported the benefits of asymmetric voltage level circuits where the individual cell voltages in a cascaded topology are different. This adds extra flexibility in synthesising sine wave output voltages with a lower voltage level contribution made at a much higher switching frequency. The topology has the potential to make better use of low and high voltage switches such as IGBTs and GTOs together in the same inverter.

Drive systems with more than two load voltage levels were developed in the 1960s using transformer coupling of separate inverters [1.29]. A similar approach has more recently been reported by Cengelci et al. [1.30] who use standard commercial inverters with phase-shifted control and transformer coupling of the output to give

multilevel voltage performance. This circuit is a form of cascaded topology but the additional transformer is a disadvantage.

Sustainable Energy (formally International Power Systems) own a patent [1.31] for a multilevel inverter formed by series connection of separate transformer isolated inverters. The five-level inverter is shown in Figure 1.2.7. This circuit has also been investigated more recently by Kang et al. [1.32] who preferably control only one inverter using high-frequency PWM with the other inverters operating with a single voltage pulse per cycle.

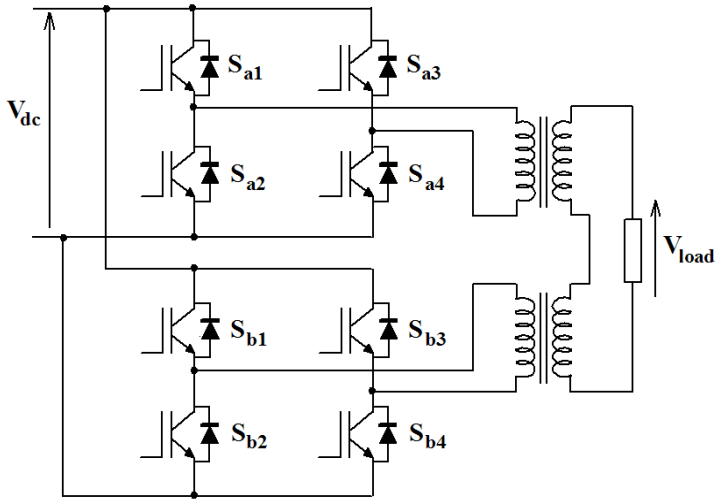


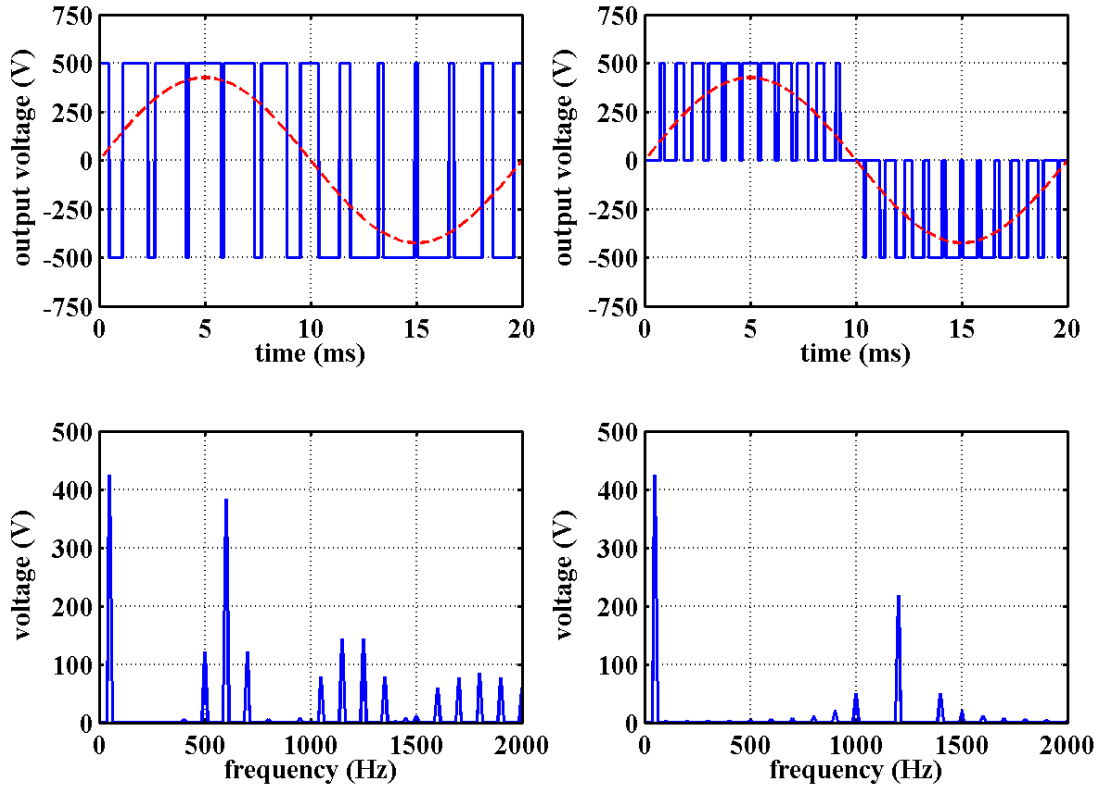
Figure 1.2.7: Cascaded transformer multilevel inverter

1.2.5 Benefits of Increased Voltage Levels

Multilevel inverters have several advantages over the standard full-bridge inverter [1.33]. These circuits allow existing power switches to be used where the system voltages are higher than the individual switch rating. The switching losses in the power electronics can be reduced because of the increased flexibility for voltage waveform synthesis offered by the increased number of voltage levels. In motor drives, the voltage stress across the winding is reduced due to the lower voltage steps applied, and common-mode capacitive coupled noise in the earth connection is less of a problem.

Figure 1.2.8 compares the difference in the output voltage waveform and frequency spectra between a standard two-level inverter and a three-level inverter when the number of switching transitions is the same for each power switch. The three-level affectively doubles the switching frequency and reduces the harmonic content in the output voltage as seen in the spectra. In a motor drive system, this will reduce the

harmonic content in the winding current and lessen the torque ripple at the shaft. The size of any additional filtering required between the load and the inverter will also be reduced.



a) Two-level inverter **b) Three-level inverter**

Figure 1.2.8: Time and frequency domain comparison between two- and three-level inverter-limb voltage waveforms

1.3 Multilevel Converter Control Methods

The simplest control strategy for all forms of multilevel converter involves operation of the individual allowable switch state modes in order to synthesis the desired ac supply voltage from the available output voltage levels. The higher number of switches will give a greater number of voltage levels, and improve the quality of the synthesised waveform in terms of reduced total harmonic distortion (THD). More sophisticated control schemes make use of PWM control of the individual switches so that the average output voltage is more tightly regulated to follow the reference voltage. Modern hardware implementations of multilevel converter modulation systems are almost exclusively done using microelectronics such as embedded microcontrollers, digital signal processors (DSP) and field programmable gate arrays

(FPGA). Software/firmware designs can take various forms and will depend on the required quality of the output waveforms.

The vast majority of applications require ac voltage synthesis, and so the modulation control scheme uses some form of fundamental amplitude and frequency demand reference. The main control schemes for an ac inverter can be divided into three distinct forms. The following section provides an overview of these different schemes, with emphasis to their extension to multilevel inverters.

1.3.1 Selective Harmonic Elimination

In the majority of multilevel inverter applications such as ac drives or static power inverters, the output voltage required is a sinusoid. The selective harmonic elimination (SHE) was one of the earliest forms of control technique applied to thyristor inverters in order to control the amplitude of the fundamental component and remove some of the unwanted harmonic components in two-level inverters. The method controls the inverter phase energisation at pre-computed electrical angles to achieve the desired harmonic amplitude control. Turnbull of GE published one of earliest papers on the subject [1.34], and it was researched in depth by Patel and Hoft [1.35, 1.36]. More recently, the issue has been investigated by Chiasson et al. [1.37] who have used the mathematical theory of resultants to find more complex angle solutions.

The flexibility of the multiple voltage levels allows the synthesis of a sinusoid to be achieved by simple staircase control, whereby each voltage level is applied across the load at the optimal electrical angle in the cycle. The transition timings can be pre-computed and a sequence stored in a look-up table. Nabae et al [1.11] described in detail this approach in their seminal paper on the NPC inverter. This technique can be extended further by additional switching sequences within each voltage level, and Sirisukprasert et al. [1.38] presented a detailed paper on this approach. Chiasson et al. [1.39] have extended their theory of resultants to SHE angle computation for cascaded-cell inverters, and have also investigated the case when the dc source voltages are not the same [1.40]. Vassallo et al. [1.41] have also investigated SHE control of the cascaded-cell multilevel inverter, adopting a cell power equalizing approach in the control implementation.

To ensure the desired spectral quality and output amplitude, the angles at which each voltage level is applied need to be selected. In order to compute these angles a set of simultaneous equations can be derived and solved. The Fourier series of the waveform is first found algebraically so that the individual harmonic expressions are obtained. With an N level inverter, there are $(N-1)/2$ positive voltage levels in the inverter output waveform, and so the amplitudes of $(N-1)/2$ harmonics terms can be solved. For example, in a three-level inverter there is only one positive voltage level, so only the

fundamental can be controlled. The waveform is referenced to the zero-crossing and it is an odd function and so only the odd harmonic, b_n, terms are finite. The amplitude of the n^{th} harmonic has the following relationship,

$$b_n = \frac{4V_{level}}{n\pi} \sum_{i=1}^{(N-1)/2} \cos n\alpha_i \quad \ldots \ (1.3.1)$$

where

α_i are the control angles referenced to the fundamental sinusoid zero crossing

V_{level} is the voltage of each level

An additional pair of harmonics can be controlled by introducing a small pulse of one voltage level amplitude within the waveform. Therefore, the amplitude b_n of the n^{th} harmonic due to this extra pulse is given by,

$$b_n = \frac{4V_{level}}{n\pi} \sum_{i=1}^{S} \left(\cos n\alpha_{2i-1} - \cos n\alpha_{2i} \right) \quad \ldots \ (1.3.2)$$

where

S is the number of extra pulses

For example, the SHE control method can be applied to a three-level inverter, to regulate the fundamental and eliminate two unwanted harmonics; the 5^{th} and 7^{th}. Figure 1.3.1 illustrates the normalised output voltage waveform and Figure 1.3.2 the output harmonic spectrum. To compute the angles, (1.3.1) and (1.3.2) are used to get a set of three simultaneous equations,

$$b_1 = \cos(\alpha_1) - \cos(\alpha_2) + \cos(\alpha_3) = \frac{\pi V_1}{4V_{level}} \quad \ldots (1.3.3)$$

$$b_5 = \cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) = 0 \quad \ldots (1.3.4)$$

$$b_7 = \cos(7\alpha_1) - \cos(7\alpha_2) + \cos(7\alpha_3) = 0 \quad \ldots (1.3.5)$$

The required firing angles can then be computed using the Newton-Raphson method for nonlinear systems of equations [1.42]. The method uses the first two terms of the Taylor series expansion of a function *f(x)*, and an iterative process used to approach the root of the function, using the formula,

$$x_{n+1} = x_n - \frac{f(x)}{f'(x)} \quad \ldots (1.3.6)$$

The method then requires the partial derivative of (1.3.1) for each angle to be solved and has the form,

$$\frac{\partial b_n}{\partial \alpha_m} = -\frac{4V_{dc}}{N\pi} \sin n\alpha_m \quad \ldots \ (1.3.7)$$

The harmonic quality of the output voltage is an important criterion in selecting the optimum control angles, and elimination of as many low-order harmonics is the optimum approach. A three-phase bridge multilevel inverter will feature triplen harmonic cancellation in the line voltages and phase current, so harmonic reduction of the 5^{th} and 7^{th} will mean that the first significant harmonic is the 11^{th}.

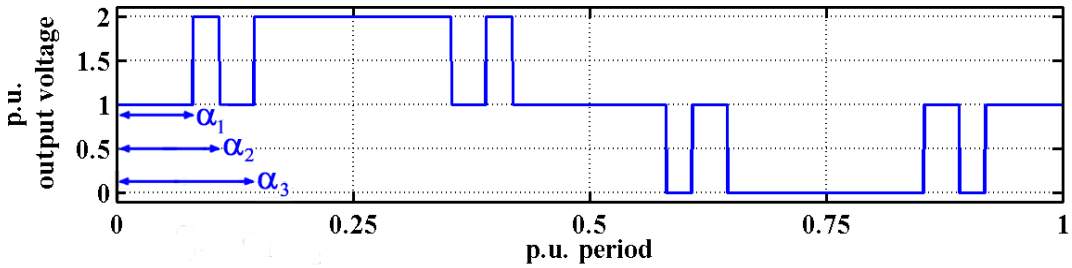


Figure 1.3.1: Three-level inverter output voltage with 5^{th} and 7^{th} harmonics elimination

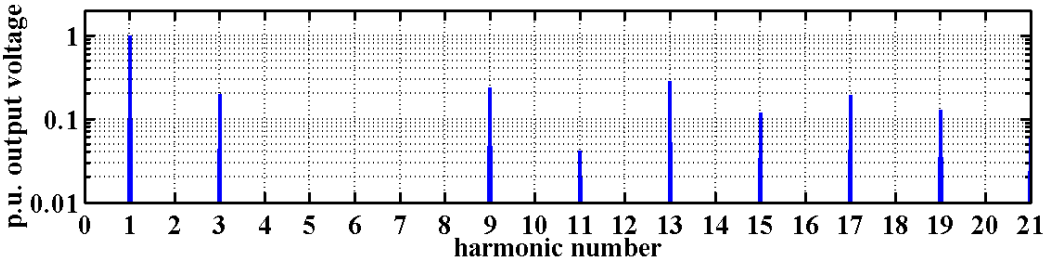


Figure 1.3.2: Spectrum of three-level inverter output voltage with 5^{th} and 7^{th} harmonics elimination

1.3.2 Sine-Triangle PWM

Conventional two-level inverters can be controlled to approximate a sinusoid output voltage using a PWM scheme known as sinusoidal or sine-triangle PWM (SPWM). There has been a great deal of work reported on the subjected, most notably by Bowes [1.43, 1.44], and recently covered in depth in a text book by Holmes and Lipo [1.45]. The output firing signals are generated by the comparison of a sampled sinusoidal reference with a triangular carrier. When the reference is greater than the triangular carrier level, the dc link is connected to the output via the top-side switch, otherwise the bottom-side switch is conducting and the output is at the negative dc link potential. The switching frequency is fixed by the carrier frequency, while the output amplitude is controlled through the reference sinusoid amplitude. The two important control parameters associated with SPWM are listed as follows:

m_a – amplitude modulation index (ratio of reference peak-to-peak to dc link voltage)

m_f – frequency modulation index (ratio of carrier frequency to reference frequency)

In a multilevel inverter, the basic building block of an SPWM controller can be applied to produce a number of different multilevel PWM control strategies, each offering slightly different performance characteristics when applied to a multilevel inverter topology. All the control schemes use one reference sinusoid and a separate carrier for each pair of power switches associated with a voltage level. In a digital implementation carrier redundancy can be exploited to reduce the amount hardware resources required.

Multilevel SPWM schemes can be split into two groups, either using carrier disposition whereby the carriers occupy distinct voltage levels or phase shifting where the carriers are simply phase-shifted from one another. The commonest carrier disposition scheme, Phase Disposition (PD), has a set of carriers all in-phase with each other but with different dc offset voltage levels as shown in Figure 1.3.3 for the single three-level inverter phase limb. The Phase Shifted (PS) scheme, shown in Figure 1.3.4, uses an equal amplitude carrier per level and phase-shifted from one another. It should be noted that the resultant output frequency is doubled in PS for the same m_f as PD. There are a number of SPWM variant schemes known in the literature [1.46 - 1.49], which all make use of different phase and level shifts in the carrier waveforms. The number of permutations of these carrier placements increases with the number of voltage levels available.

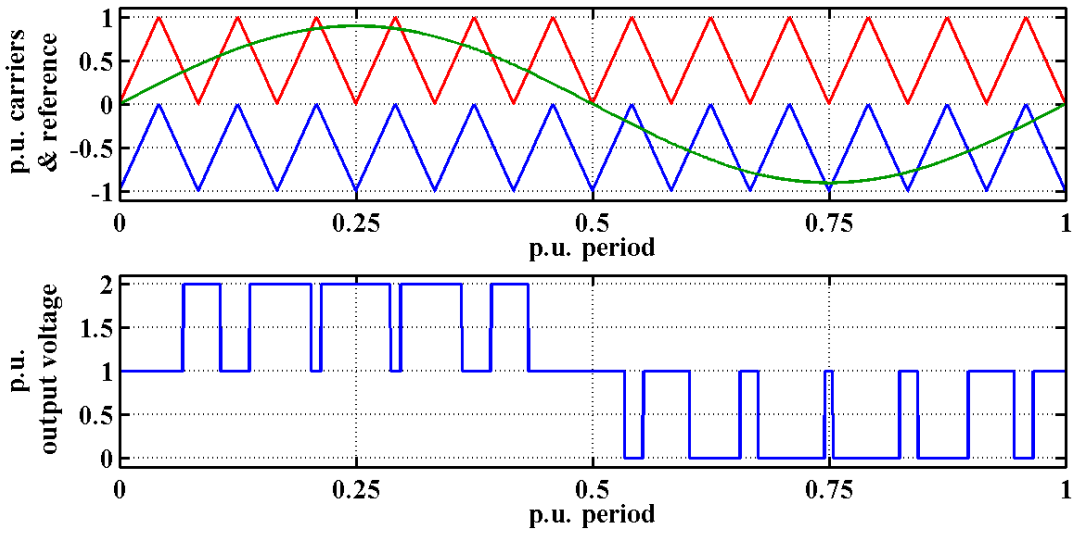


Figure 1.3.3: Two-cell phase disposition SPWM waveforms (m_a = 0.9, m_f = 12)

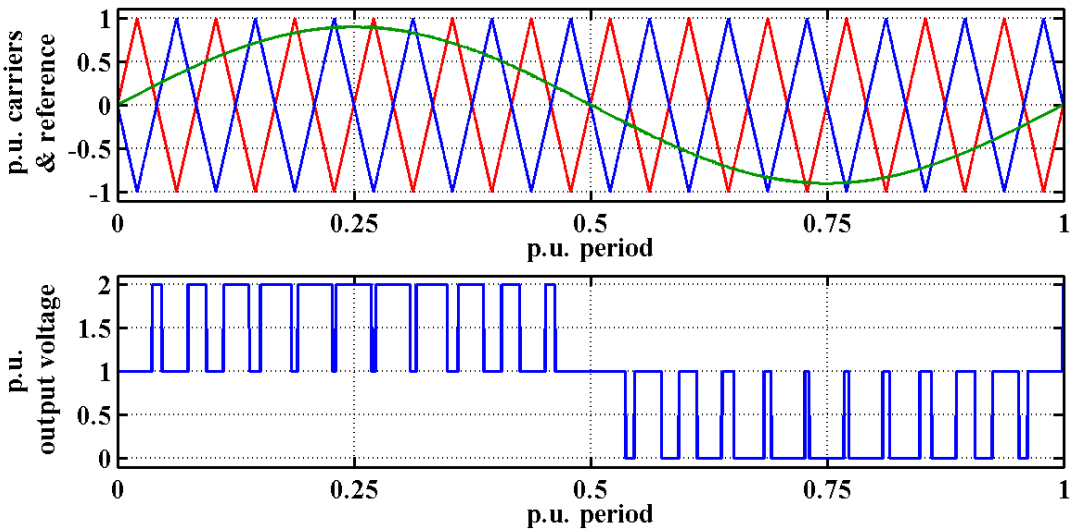


Figure 1.3.4: Two-cell phase shifted SPWM waveforms (m_a = 0.9, m_f = 12)

Modern digital implementations of SPWM entail sampling of the modulation scheme waveforms. Macro sampling can be applied to the reference where the value only changes at the start of carrier triangle (symmetric sampling) or at both peak and trough (asymmetric sampling). Micro sampling effects are present due to the digital controller's clock frequency and possible lower internal sampling rates caused by interrupt servicing, computational latency, etc. These sampling effects, together with the dead-times introduced in the firing signals to avoid shoot-through failures, all influence the performance of the inverter.

1.3.3 Space Vector PWM

The space vector PWM (SVPWM) technique is an important alternative means of generating the switching pattern for a three-phase voltage-source inverter. Mapping of the three-phase stationary reference frame voltage states in the inverter to an orthogonal reference frame using the Clarke transform, allows the duty cycles for each phase to be computed relatively simply. The SVPWM method was first described for controlling NPC inverters in the 1980s [1.50, 1.51].

The Clarke transform is applied to an arbitrary set of balanced three-phase voltages to obtain the so called space vector representation in the complex α-β plane. The time-dependent vector, **V**, is derived from the individual phase-to-neutral voltages according to the relationship.

$$\mathbf{V} = \frac{2}{3}\left(v_{an} + v_{bn} e^{j\frac{2\pi}{3}} + v_{cn} e^{j\frac{4\pi}{3}} \right) \qquad \ldots (1.3.8)$$

where v_{an}, v_{bn} and v_{cn} are the stationary node voltages with respect to the centre-point neutral of a balanced three-phase load, and the following relationship holds:

$$v_{an} + v_{bn} + v_{cn} = 0 \qquad \ldots (1.3.9)$$

The space vector diagram of the eight voltage states in a three-phase inverter is shown in Figure 1.3.5. The triangular sector in which the target reference vector lies is first identified and then the duty cycles for the boundary vectors are computed, giving the upper switch on-time for each phase. The two zero sequence vectors [000] and [111] are conventionally used in equal measure to complete the total switching period, and the resultant switching pattern is arranged symmetrically as shown in Figure 1.3.6. The popularity of the space vector scheme is due to its relatively low harmonic distortion and inherent increased modulation depths ($m_a > 1$). Nowadays, commercial microcontrollers and DSPs aimed at power electronics and motion control applications have dedicated hardware implementations which simplify the use of SVPWM in conventional two-level inverter applications.

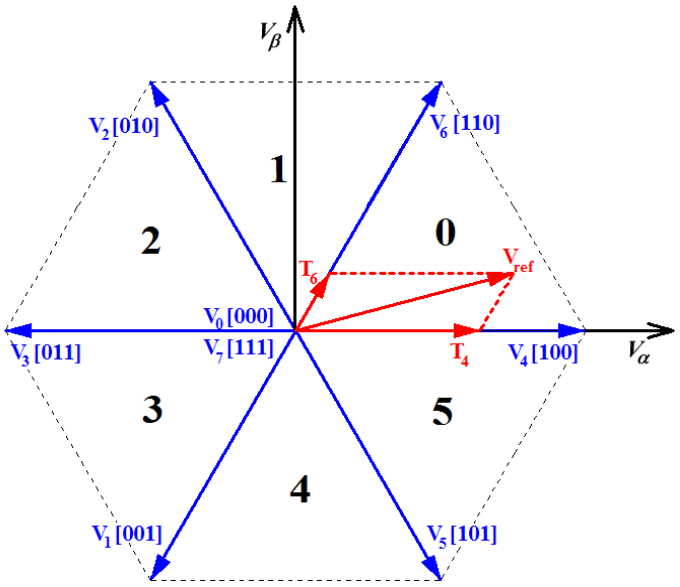


Figure 1.3.5: Space vector diagram for a conventional two-level inverter

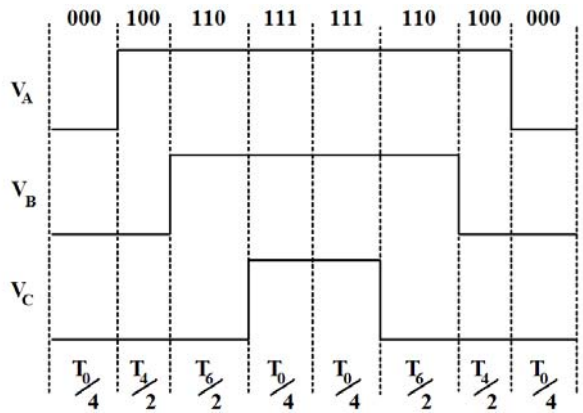


Figure 1.3.6: Symmetric firing pattern of the SVPWM scheme

When the space vector concept is extended to multilevel inverters there are an increased number of space vectors in the orthogonal reference plane. Figure 1.3.7 illustrates the space vector diagram for a three-phase, five-level inverter. The vector number indicates the output voltage level for each phase. This means that there is an increase in the vector options available for synthesising the reference, and this increases the complexity of the computational algorithm required to exploit the performance of the SVPWM control scheme. The problem of optimum selection of the switching state space vectors has intrigued researchers and there have been various optimum solutions reported on the issue, notably Lee et al. [1.52] and Wei at al. [1.53]. The optimum vector selection can also improve other performance criteria such as the common voltage ripple as reported by Zhang et al. [1.54].

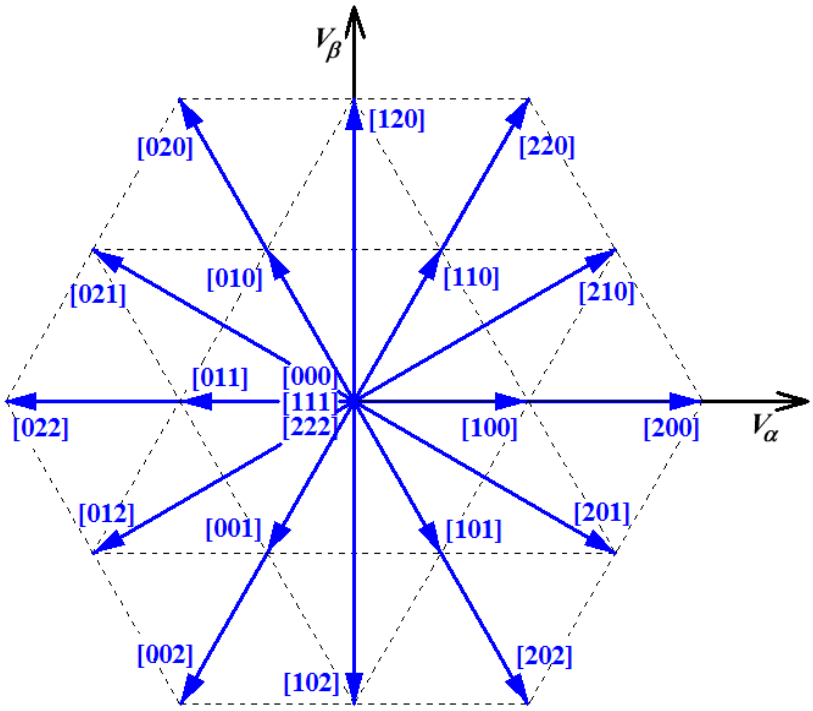


Figure 1.3.7: Space vector diagram for two-cell, three-level inverter

1.3.4 Hysteretic Current Control

Current-regulated control can also be employed in order to maintain the output current within a small hysteresis band. The control can employ multiple hysteresis bands for identifying the required output voltage level such as the method described by Marchesoni [1.55] and Corzine [1.56]. Alternative schemes have also been proposed such as a voltage level selection based on the derivative current error by Bode et al. [1.57].

Hysteretic current control is suitable in motor drive systems where a high bandwidth is required, but can only be used when the rate of change of phase current for a given applied voltage allows a realistic range of inverter switching frequencies. The main disadvantage is the variable switching frequency that results and in so hysteretic current control is not generally favoured in most mainstream applications.

1.4 Multilevel Converter Applications

1.4.1 Forms of Power Conversion

The multilevel converter circuits can be applied to all four canonical power converter forms. Their applications can be briefly categorised as follows:

- **Rectification:** The diode-clamped and flying-capacitor bridge topologies are suitable for use as an active front-end (AFE) for interfacing between an ac source and a system dc link. Rectification can be performed simply by control of the switches and additional benefits of low harmonic current distortion and power factor improvements can be realised. Additional regulation of the dc link can be done and a multilevel AFE will allow regenerative power in a drive system to be supplied back to the ac source. It is also possible to use a cascaded-cell inverter coupled via a transformer to an ac source as a rectifier.
- **Inversion**: This is the primary application for a multilevel converter circuit, where the source voltage is dc and the load is ac. All multilevel circuits can operate as inverters, but in the case of the cascaded-cell circuit, there are multiple voltage sources.
- **DC/DC Conversion**: The diode-clamped and flying-capacitor means of protecting the peak voltages across the power switches can be applied in a chopper circuit configuration. The flying-capacitor circuit was originally conceived for use as a multilevel chopper. In dc power supplies, boosting or bucking modes of control can be used.
- **AC/AC Conversion:** Unlike the matrix converter there is no direct ac to ac conversion mode available inherently in the multilevel configurations, since they use internal dc sources to protect the individual power switches. However, by combining a multilevel AFE and a multilevel inverter in an intertie configuration, connections between different ac systems can be achieved with bidirectional power flow.

1.4.2 Medium Voltage Drive Systems

Traditionally, medium voltage drive systems have used thyristor-based current source inverters because of the lack of available high power forced commutated electronic switches. The advent of the GTO has now shifted the balance towards voltage source inverters and large drive systems are now benefiting from improvements in performance gained from variable speed [1.58]. Multilevel inverter technology has provided even more scope for operating large drives in variable speed, since the main benefit is the improved harmonic quality and reduced switching loss [1.59]. A multilevel inverter has the benefit of operating at higher voltages with fast switching frequencies, so that the output voltage quality is sufficiently good to avoid large additional filtering. This is important with relation to cost and overall drive size.

The original NPC (three-level diode clamped inverter) was originally envisaged for drive applications and indeed it is now used extensively in higher power, medium voltage drive systems [1.60]. The cascaded-cell inverter has also found application in very high power drive systems such as gas pipeline compressors [1.61]. The flying-capacitor inverter has also been commercialised by Alstom for drive system applications [1.62].

To improve system performance further, a second multilevel inverter stage can be added, combining with the machine-side inverter to form an intertie, and used as an active front-end filter to provide power factor correction (PFC). The original work on multilevel PFC focused on large traction drives using three-level GTO NPC converters [1.63]. This combination, shown in Figure 1.4.1, is also suitable for re-generative systems, and is an appropriate solution for interfacing between the utility grid and emerging high power renewable energy generation systems.

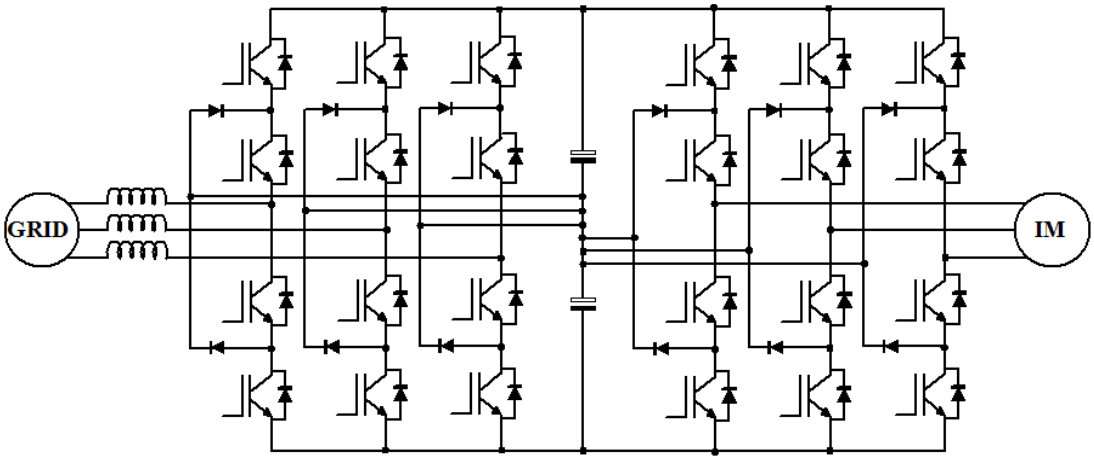


Figure 1.4.1: Three-level diode-clamped multilevel intertie bi-directional converter

1.4.3 Power Conditioning

The concept of a flexible ac transmission system (FACTS) provides opportunities for a number of different applications of multilevel converter circuits to be connected within a power distribution system [1.64], and through control help to improve the overall power quality and system performance.

Decoupled voltage source inverter circuits are used as static VAr compensators (STATCOM), and the benefits of the multilevel inverter make them attractive in higher voltage systems [1.65 - 1.68]. Figure 1.4.2 shows a shunt-connected three-phase inverter in an ac transmission system. The inverter is rated to supply only reactive power at the point of load, thus through optimum control compensate for poor load power factors. This reduces the level of current being supplied by the utility grid and maximises the overall system power delivery capacity.

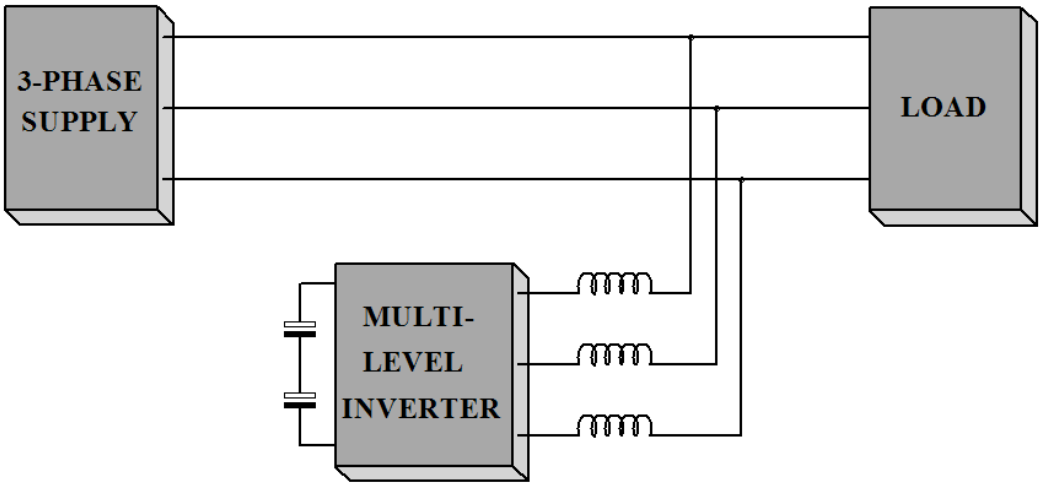


Figure 1.4.2: Shunt-connected multilevel inverter arrangement

Active filtering is also possible with this shunt arrangement where more advanced control of the multilevel inverter can also remove unwanted harmonics from flowing in the transmission system, reducing the requirement for large passive filtering. This is done by controlling the injection of anti-phase current harmonic components which cancel those present in the load current.

Active filtering can also be achieved by series connecting the multilevel inverter via transformers as shown in Figure 1.4.3. This arrangement can de-couple the unwanted load harmonics from the transmission side, and additionally be used for maintaining the load voltage during short lived supply voltage disturbances.

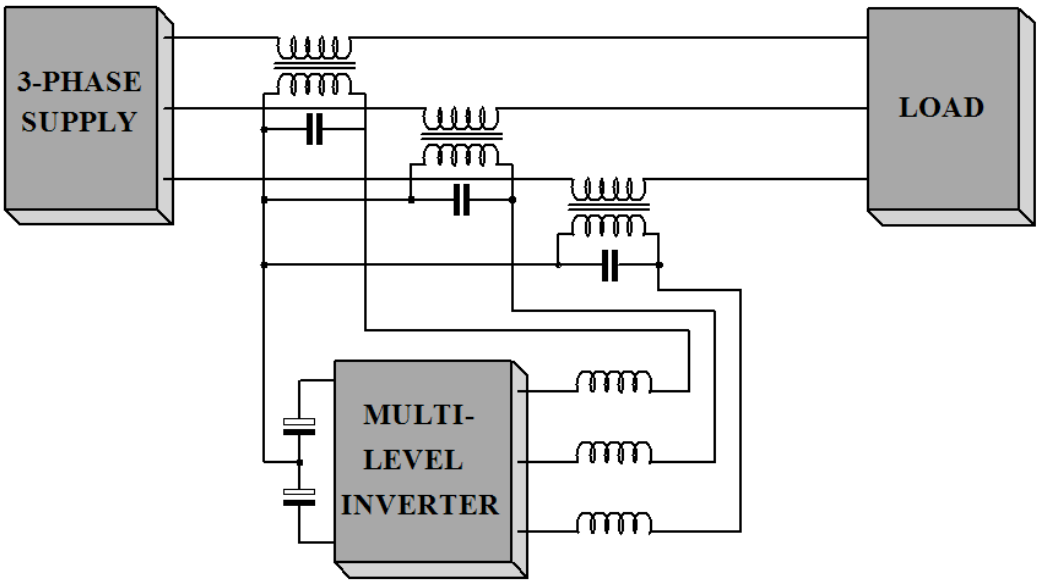


Figure 1.4.3: Series-connected multilevel inverter arrangement

The shunt and series connected multilevel inverters can be combined in the form of an intertie to provide a power quality solution known variously as unified power flow controller (UPFC) or universal power line conditioner (UPLC) [1.69]. The series circuit compensates for source-side harmonics and voltage disturbances, while the shunt circuit deals with load dependent power quality issues.

These system concepts will become increasingly important as more distributed generation networks evolve using combinations of different localised power generation. By replacing the dc link capacitors in a shunt-connected multilevel inverter with a source of dc power such as fuel cells, batteries or other energy storage system the circuit acts as an uninterruptible power supply, providing load power for longer periods of power outage. Extending the concept further, using renewable sources of energy such as photovoltaic and wind turbines, the multilevel inverter system becomes an integral part of a supply generator in a distributed supply network.

1.5 Challenges and Practical Issues

The first challenge faced in developing a multilevel inverter solution for a specific application is selecting from wide variety of circuit topologies, numbers of voltage levels and different modulation control schemes available. There is no definitive answer as to what topology is best for an application. The different circuit topologies contain different numbers of the core constituent components. A comparison can be

drawn by comparing the major component requirements for a nine-level, three-phase inverter when used as a grid-connected shunt active filter. Table 1.5.1 lists the number of different components required in each case. It is assumed that all components are of equal voltage rating so the numbers of clamping capacitors and diodes reflects this.

	Diode-Clamped	**Flying-Capacitor**	**Cascaded-Cell**
Transistors	24	24	24
Diodes	60	24	24
Capacitors	4	18	12

Table 1.5.1: Comparison of the number of main power components

Not surprisingly, the diode-clamped has the largest silicon content with the lowest number of capacitors whilst the flying-capacitor inverter has the most capacitors. The cascaded-cell inverter uses the least number of components but requires smoothing capacitors for each cell which see a significant twice line frequency ripple current. The final decision has to be made by assessing the actual application requirements in terms of power rating and performance, in light of the available rated components to achieve the end goal.

The selection of level number again can only be decided commercially, because of the increasing circuit complexity versus better performance offered as the number of levels increases. The judgement, however, will be dictated by the available power switch technology. Advances in semiconductors are pushing the upper limits of operating breakdown voltage and reducing the switching energy loss characteristic thus increasing the potential operating frequencies of the inverter. Wide band-gap semiconductors may also play a defining role in future developments if the potential promise of these devices is realisable commercially.

Once the best topology has been identified, then the optimum control of the inverter is a major challenge faced by the system designer. Voltage modulation of the fundamental frequency component in ac systems is relatively straightforward and can be achieved easily with modern microelectronics. However, the specific topological requirements for maintaining balanced system operation in terms of equal power loss distribution in all the power electronic switches and ensuring that capacitor voltages are at the required levels is a major issue. Selecting the type of control scheme and operating frequency needs careful thought, since it has a bearing on the size of the energy storage devices and losses in the inverter system.

Of most significance in all multilevel inverter applications is the minimisation of the unwanted harmonic components in the output voltage and/or current. Certain control schemes may offer improved harmonic distortion over other methods, and these issues need to be appraised thoroughly in light of the application and any legislative requirements. Increasing the available output voltage levels can play an important role in reducing the harmonic distortion and operating frequency and will have a bearing on the extra cost and size of passive filtering components. In drive systems, where the load is inductive, the phase current waveforms will be well filtered, but the control scheme must avoid introducing harmonic components which lead to significant torque perturbations at the motor shaft.

Individual drive systems may require different levels of acceptable harmonic distortion. In the case of grid-connection there are a number of international standards setting-out acceptable levels of total harmonic distortion, and allowable levels for individual harmonics of the fundamental. The most notable are IEC EN61000-3-2 [1.70] and IEEE 519-1992 [1.71]. Table 1.5.2 lists the maximum recommended amplitude of the odd current harmonics as a percentage of the supplied fundamental current in distribution systems up to 69 kV as recommended in IEEE519. The total harmonic distortion is recommended to be less than 5%. The even harmonics area limited to 25% of the odd harmonics in the specified range. These levels are for systems where the maximum load current is greater than a 20^{th} of the maximum inverter rating.

Harmonic	**n < 11**	**11 ≤ n < 17**	**17 ≤ n < 23**	**23 ≤ n < 35**	**35 ≤ n**	**THD**
Limit	4%	2%	1.5%	0.6%	0.3%	5%

Table 1.5.2: Maximum harmonic current as percentage of fundamental current

The maximum amplitudes specified in the table have also been incorporated into new IEEE 1547 standards regarding the interconnection of distributed power sources [1.72]. This standard is applicable to inverters for renewable energy sources such as wind, solar panels and fuel-cells.

1.6 Motivation and Objectives

The diode-clamped and cascaded-cell inverters are far more mature technologies commercially. This is partly due to intellectual property rights issues, but can also be understood when comparing the number of capacitor storage elements required, compared to the flying-capacitor circuit. There has been much academic interest in

multilevel control schemes which can be applied to all forms of multilevel inverter. Most work has focussed on specific control techniques and generally assumed the inverter has ideal behaviour with perfect voltage level synthesis. When investigations on system balancing have been undertaken, the effects on output power quality have largely been ignored.

The challenge in getting the flying-capacitor inverter accepted as a suitable alternative for most high power applications is to minimise the total cost of the capacitor storage elements, while maintaining high reliability and excellent power quality performance. Therefore, the focus of this investigation is to identify optimal control techniques in conjunction with system voltage balancing algorithms, and quantify the capacitor sizing against the desired operating parameters.

The main analysis tool for the investigation is a specially developed computer simulation program which incorporates the key characteristics of the overall system's components, so that accurate predictions of behaviour of a real inverter can be assessed. Control optimisation is assessed through experimental work on a four-cell, five-level inverter, and measurements used to verify the validity of the conclusions reached through simulation.

The thesis is divided into the following major chapters:

Chapter 1:

Introduction chapter on multilevel topologies in general, their basic characteristics and major applications with reference to the present state of the art as published in the literature. The practical problems associated with implementation so setting out the motivation and objectives of the research conducted specifically on the flying-capacitor inverter topology.

Chapter 2:

This chapter focuses specifically on the flying-capacitor inverter's characteristics, especially the issue of internal inverter balancing. The existing literature on the topology is reviewed thoroughly and major issues in its implementation highlighted. The complexity of the inverter operating modes is analysed in detail and the requirements for cell-capacitor voltage balancing are identified. Basic circuit models are introduced and a more detailed simulator, developed specifically for the work, is described.

Chapter 3:

Selective harmonic elimination (SHE) control as applied to a flying-capacitor inverter is covered in this chapter. The important issue of system balancing, introduced in Chapter 2, is addressed in the context of the simplest form of SHE,

staircase output voltage operation. An important contribution is made through a systematic method of selecting optimum balancing patterns and it is shown that reductions in harmonic distortion can be achieved when applied to inverters with practical sized cell-capacitors. Simulation is used throughout the chapter to support the analysis.

Chapter 4:

Sine-triangle PWM is dealt with in detail in this chapter, using simulation to analyse the system operation under different carrier placement PWM implementations. The performance of the different PWM schemes is compared, including the influence of practical sized inverter components, and digital controller implementation aspects. A novel digital hardware design of a cell-capacitor voltage balancing approach is presented which is applicable to all forms of PWM control.

Chapter 5:

This chapter repeats the analysis of the inverter when controlled using space vector PWM, and introduces a simplified implementation approach for multilevel inverters. Comparisons are drawn between space vector PWM and sinusoidal PWM, specifically third-harmonic injection.

Chapter 6:

A practical multilevel inverter designed and built for laboratory experimentation is described in this chapter. Results of operation under a variety of different control schemes are used to support the validity of the previous chapters' simulation analysis.

Chapter 7:

The concluding chapter with a review of the major achievements of the work and recommendations on future research work.

1.7 References

[1.1] Mohan, N., Undeland, T.M. and Robbins, W.P., "Power electronics. Converters, applications, and design", John Wiley & Sons, Inc., New York, USA, 3rd Edition, 2003.

[1.2] Akagi, H., "Trends in power electronics and motor drives", Proceedings of PEDS 2003, the 5th International Conference on Power Electronics and Drive Systems, 17 - 20 November, 2003, Vol. 1, pp. 1 - 7.

[1.3] Lorenz, L., "New power semiconductor components for future innovative high frequency power converters", Proceedings of ICIT 2003, IEEE International Conference on Industrial Technology, 10 - 12 December, 2003, Vol. 2, pp. 1173 - 1177.

[1.4] Chittat, V., Hongt, S. and Torrey, D.A., "Series Connection of IGBTs with Active Voltage Balancing", Conference Record of IAS '97, 32nd Industry Applications Society Annual Meeting, 5 - 9 October, 1997, Vol. 2, pp. 961 - 967.

[1.5] Special Section on Multilevel Inverters – I, IEEE Transactions on Industrial Electronics, Vol. 49, No. 4, August 2002, pp. 722 – 888.

[1.6] Special Section on Multilevel Inverters – II, IEEE Transactions on Industrial Electronics, Vol. 49, No. 5, October 2002, pp. 946 – 1100.

[1.7] Lai, J.-S. and Peng, F.Z., "Multilevel converters - a new breed of power converters", Conference Record of IAS '95, the IEEE Industry Applications Society 30th Annual Meeting, 8 - 12 October, 1995, Vol. 3, pp. 2348 – 2356.

[1.8] Teodorescu, R., Blaabjerg, F., Pedersen, J.K., Cengelci, E.,. Sulistijo, S.U, Woo, B.W. and Enjeti, P., "Multilevel converters - a survey", Proceedings of EPE '99, 8th European Conference on Power Electronics and Applications, 7 - 9 September 1999, CD-ROM paper.

[1.9] Baker, R.H., "High-voltage converter circuit", US Patent No. US4203151, Filed 21st September, 1978, Granted 13th May, 1980.

[1.10] Baker, R.H., "Bridge converter circuit", US Patent No. US4270163, Priority Filed 12th September 1978, Granted 26th May, 1981.

[1.11] Nabae, A., Takahashi, J. and Akagi, H., "A new neutral-point-clamped PWM inverter", Proceedings of IAS '80, the IEEE Industry Applications Society Annual Meeting, 29 November – 3 October 1980, pp 761 - 766.

[1.12] Andrejak, J.M. and Lescure, M., "High voltage converters promising technological developments", Proceedings of EPE '87, 2nd European Conference on Power Electronics and Applications, 22 - 24 September, 1987, pp. 1.159 – 1.162.

[1.13] Choi, N.S., Cho, J.G. and Cho, G.H., "A general circuit topology of multilevel inverter", PESC '91 Record. 22nd Annual IEEE Power Electronics Specialists Conference, 24 - 27 June, 1991, pp 96 – 103.

[1.14] Carpita, M. and Tenconi, S., “A novel multilevel structure for voltage source inverter”, Proceedings of EPE '91, 4th European Conference on Power Electronics and Applications, 3 - 6 September 1991, pp. 1.90 – 1.94.

[1.15] Peng, F.Z., Lai, J.S. and McKeever, J., “A multilevel voltage-source converter system with balanced dc voltages”, PESC '95 Record. 26th Annual IEEE Power Electronics Specialists Conference, 18 - 22 June, 1995, pp. 1144 – 1150.

[1.16] Simon, E.D. and Bonner, G., "An inductive energy storage system using Ignitron switching", IEEE Transactions on Nuclear Science, Vol. NS-14, No. 5, 1967.

[1.17] Dickerson, J.A. and Ottaway, G.H., “Transformerless power supply with line to load isolation”, US Patent No. 3596369, Filed 22 December 1969.

[1.18] Singer, Z., Emanuel, A. and Erlicki, M.S., "Power regulation by means of a switched capacitor", Proceedings of the IEE, Vol. 119, No. 2, February 1972, pp. 149 - 152.

[1.19] Meynard, T.A. and Foch, H., "Dipositif électronique de conversion d'énergie électrique", French Patent No. 2679715B1, Filed 25th July 1991, Issued 29th January 1993.

[1.20] Meynard, T.A. and Foch, H., “Multi-level choppers for high voltage applications”, EPE Journal, Vol. 2, No. 1, March 1992, pp. 45 – 50.

[1.21] Marchesoni, M., Mazzucchelli, M. and Tenconi, S., “A non conventional power converter for plasma stabilization”, PESC '88 Record, 19th Annual IEEE Power Electronics Specialists Conference, 11 - 14 April 1988, Vol. 1, pp. 122 – 129.

[1.22] Hammond, P.W., “Medium voltage PWM drive and method”, US Patent No. 5625545, Filed 1st March 1994, Issued 29th April 1997.

[1.23] Hammond, P.W., “A new approach to enhance power quality for medium voltage drives”, Record of the IEEE Industry Applications Society 42nd Annual Petroleum and Chemical Industry Conference, 11 - 13 September 1995, pp. 231 – 235.

[1.24] Kumar, M.R.P. and Kim, J.M.S., “Current control of a hybrid multilevel switching converter”, Proceedings of PEDES '96, the 1st IEEE International Conference on Power Electronics, Drives and Energy Systems for Industrial Growth, 8 - 11 January, 1996, Vol. 1, pp. 346 - 352.

[1.25] Peng, F.Z., "A generalized multilevel inverter topology with self voltage balancing", Conference Record of IAS 2000, the 2000 IEEE Industry Applications Society 35th Annual Meeting, 8 - 12 October, 2000, Vol. 3, pp. 2024 – 2031.

[1.26] Bhagwat, P.M. and Stefanovic, V.R., "Generalized structure of a multilevel PWM inverter", IEEE Transactions on Industry Applications, Vol. IA-19, No. 6, November/December 1983, pp. 1057 – 1069.

[1.27] Manjrekar, M.D., Steimer, P.K. and Lipo, T.A., "A hybrid multilevel inverter topology for drive applications", Proceedings of APEC '98, IEEE 13th Annual Applied Power Electronics Conference and Exposition, 16 - 19 February, 1998, Vol. 2, pp. 523 - 529.

[1.28] McGrath, B.P., Holmes, D.G., Manjrekar, M. and Lipo, T.A., "An improved modulation strategy for a hybrid multilevel inverter", Conference Record of IAS 2000, the 2000 IEEE Industry Applications Society 35th Annual Meeting, 8 - 12 October, 2000, Vol. 4, pp. 2086 – 2093.

[1.29] Flairty, C.W., "A 50 kVA adjustable-frequency 23-phase controlled rectifier inverter", AIEE Industrial Electronics Symposium, 20 -21 September, 1961.

[1.30] Cengelci, E., Woo, B.W., Enjeti, P., Teodorescu, R. and Blaabjerg, F., "A new medium voltage PWM inverter topology for adjustable speed drives", IEEE Transactions on Industry Applications, Vol. 35, No. 3 May/June 1999, pp. 628-637.

[1.31] Schienbein, L.A., Droppo, G.W., Donnelly, M.K. and Harris, B.E., "Step wave power converter", US Patent No. US6198178B1, Filed 21st December 1999, Granted 6th March 2001.

[1.32] Kang, F.-S., Park, S.-J. and Kim, C.-U., "Multilevel inverter employing cascaded transformers", Proceedings of IECON '03, 29th Annual Conference of the IEEE Industrial Electronics Society, 2 – 6 November, 2003, Vol. 3, pp. 2169 – 2174.

[1.33] Shakweh, Y., "MV inverter stack topologies", IEE Power Engineering Journal, June 2001, pp. 139 – 149.

[1.34] Turnbull, F.G., "Selected harmonic reduction in static d-c – a-c inverters", IEEE Transactions on Communications and Electronics, Vol. 83, July 1964, pp. 374 – 378.

[1.35] Patel, H.S. and Hoft, R.G. "Generalized harmonic elimination and voltage control in thyristor inverters – Part I – Harmonic elimination", IEEE

Transactions on Industry Applications, Vol. IE-9, May/June 1973, pp. 310 – 317.

[1.36] Patel, H.S. and Hoft, R.G. "Generalized harmonic elimination and voltage control in thyristor inverters – Part II – Voltage control technique", IEEE Transactions on Industry Applications, Vol. IE-10, September/October 1974, pp. 666 - 673.

[1.37] Chiasson, J.N., Tolbert, L.M., McKenzie, K.J. and Du, Z., "A complete solution to the harmonic elimination problem", IEEE Transactions on Power Electronics, Vol. 19, No. 2, March 2004, pp. 491 – 499.

[1.38] Sirisukprasert, S., Lai, J.-S. and Liu, T.-H., "Optimum harmonic reduction with a wide range of modulation indexes for multilevel converters", Conference Record of IAS 2000, the IEEE Industry Applications Society 35th Annual Meeting, 8 - 12 October, 2000, Vol. 3, pp 2094 – 2099.

[1.39] Chiasson, J.N., Tolbert, L.M., McKenzie, K.J. and Du, Z., "A unified approach to solving the harmonic elimination equations in multilevel converters", IEEE Transactions on Power Electronics, Vol. 19, No. 2, March 2004, pp. 478 – 490.

[1.40] Tolbert, L.M., Chaisson, J.N., McKenzie, K.J. and Du, Z., "Elimination of harmonics in a multilevel converter with non equal DC sources", Proceedings of APEC '03, the 18th Annual IEEE Applied Power Electronics Conference and Exposition, 9 – 13 February, 2003, Vol. 1, pp. 589 – 595.

[1.41] Vassallo, J., Clare, J.C. and Wheeler, P.W., "A power-equalized harmonic-elimination scheme for utility-connected cascaded H-bridge multilevel converters", Proceedings of IECON '03, 29th Annual Conference of the IEEE Industrial Electronics Society, 2 – 6 November, 2003, Vol. 2, pp. 1185 – 1190.

[1.42] Press, W.H., Flannery, B.P., Teukolsky, S.A. and Vetterling, W.T., "Numerical recipes in C. The art of scientific computing", Cambridge University Press, 1988, ISBN 0-521-35465-X, Chapter 9, pp. 270 – 275.

[1.43] Bowes, S.R., "New sinusoidal pulsewidth-modulated inverter", IEE Proceedings, Vol. 122, No. 11, November, 1975, pp. 1279 - 1285.

[1.44] Bowes, S.R. and Mount, M.J., "Microprocessor control of PWM inverters", IEE Proceedings, Vol. 128, Part B, No. 6, November 1981, pp. 293 – 305.

[1.45] Holmes, D.G. and Lipo, T.A., "Pulse width modulation for power converters. Principles and practice", Wiley-IEEE Press Series on Power Engineering, 2003, ISBN 0-471-20814-0.

[1.46] Tolbert, L.M. and Habetler, T.G., “Novel multilevel inverter carrier-based PWM methods”, Conference Record of IAS '98, the 1998 IEEE Industry Applications Society 33rd Annual Meeting, 12 - 15 October, 1998, Vol. 2, pp. 1424 – 1431.

[1.47] Agelidis, V.G. and Calais, M., "Application specific harmonic performance evaluation of multicarrier PWM techniques", PESC '98 Record, 29th Annual IEEE Power Electronics Specialists Conference, 17 - 22 May, 1998, Vol. 1, pp 172 - 178.

[1.48] McGrath, B.P. and Holmes, D.G., “A comparison of multicarrier PWM strategies for cascaded and neutral point clamped multilevel inverters”, Proceedings of PESC 2000, 31st Annual IEEE Power Electronics Specialists Conference, 18 - 23 June, 2000, Vol. 2, pp. 674 – 679.

[1.49] Massoud, A.M., Finney, S.J. and Williams, B.W., “Control techniques for multilevel voltage source inverters”, Proceedings of PESC '03, 34th IEEE Power Electronics Specialists Conference, 15 - 19 June, 2003, Vol. 1, pp. 171 – 176.

[1.50] Steinke, J.K., "Control strategy for a three phase AC traction drive with three-level GTO PWM inverter", Proceedings of PESC '88, 19th Annual IEEE Power Electronics Specialists Conference, 11-14 April 1988, Vol. 1, pp. 431 - 438.

[1.51] Bauer, F. and Heining, H.-D., “Quick response space vector control for a high power three-level inverter drive system”, Proceedings of EPE ’89, the 3rd European Conference on Power Electronics and Applications, 9 – 12 October, 1989, Vol. 1, pp. 417 – 421.

[1.52] Lee, Y.-H., Kim, R.-Y. and Hyun, D.-S., “A novel SVPWM strategy considering DC-link balancing for a multi-level voltage source inverter”, Proceedings of APEC '99, the 14th IEEE Applied Power Electronics Conference and Exposition, 14 - 18 March, 1999, Vol. 1, pp. 509 – 514.

[1.53] Wei, S.-M., Wu, B., Li, F.-H. and Liu, C.-W., "A general space vector PWM control algorithm for multilevel inverters", Proceedings of APEC '03, the 18th IEEE Applied Power Electronics Conference and Exposition, 9 - 13 February, 2003, Vol. 1, pp. 562 - 568.

[1.54] Zhang. H.-R., von Jouanne, A. and Wallace, A. "Multilevel inverter modulation schemes to eliminate common-mode voltages", Conference Record of IAS '98, the 33rd IEEE Industry Applications Annual Meeting, 12 - 15 October, 1998, Vol. 1, pp. 752-758.

[1.55] Marchesoni, M., "High performance current control techniques for applications to multilevel high power voltage source inverters", Proceedings of PESC '89, the 20th IEEE Power Electronics Specialists Conference, 26 - 29 June, 1989, Vol. 2, pp. 672 - 682.

[1.56] Corzine, K.A., "A hysteresis current-regulated control for multi-level drives", IEEE Transactions on Energy Conversion, Vol. 15, No. 2, June 2000, pp. 169 – 175.

[1.57] Bode, G.H., Zmood, D.N., Loh, P.C. and Holmes, D.G., "A novel hysteresis current controller for multilevel single phase voltage source inverters", Proceedings of PESC 2000, 31st Annual IEEE Power Electronics Specialists Conference, 18 - 23 June, 2000, Vol. 4, pp. 1845 – 1850.

[1.58] Marchesoni, M. and Mazzucchelli, M., "Multilevel converters for high power AC drives: a review", Proceedings of ISIE '93, IEEE International Symposium on Industrial Electronics, 1 - 3 June, 1993, pp. 38 - 43.

[1.59] Newton, C. and Summer, M., "Multi-level convertors a real solution to medium/high-voltage drives?", IEE Power Engineering Journal, Vol. 12, No. 1, February 1998, pp. 21 – 26.

[1.60] Tamai, S., Koyama, M., Fujii, T., Mizoguchi, S. and Kawabata, T., "3 level GTO converter-inverter pair system for large capacity induction motor drive", Proceedings of EPE '93, 5th European Conference on Power Electronics and Applications, IEE Conference Publication No. 377, 13 - 16 September, 1993, Vol. 5, pp. 45 – 50.

[1.61] Hammond, P.W., "Enhancing the reliability of modular medium-voltage drives", IEEE Transactions on Industrial Electronics, Vol. 49, No. 5, October 2002, pp. 948 – 954.

[1.62] Beinhold, G., Jakob, R. and Nahrstaedt, M., "A new range of medium voltage multilevel inverter drives with floating capacitor technology", Proceedings of EPE '01, 9th European Conference on Power Electronics and Applications, 27 - 29 August, 2001, CDROM Paper No. PP00426.

[1.63] Ghiara, T., Marchesoni, M. and Sciutto, G., "High power factor control system in multilevel converters for AC heavy traction drives", Proceedings of APEC '90, the 5th IEEE Applied Power Electronics Conference and Exposition, 11-16 March 1990, pp. 672 - 680.

[1.64] Gyugyi, L., "Application characteristics of converter-based FACTS controllers", Proceedings of PowerCon 2000, the International Conference on Power System Technology, 4 - 7 December, 2000, Vol. 1, pp. 391 - 396.

[1.65] Choi, N.S., Cho, G.C. and Cho, G.H., "Modeling and analysis of a static VAR compensator using multilevel voltage source inverter", Conference Record of IAS '93, the 1993 IEEE Industry Applications Society 28th Annual Meeting, 2 - 8 October, 1993, Vol. 2, pp. 901 - 908.

[1.66] Peng, P.Z. and Lai, J.S., "A static VAr generator using a staircase waveform multilevel voltage source converter", Proceedings of PCIM/PQ '94, the Power Quality Conference, 17 - 22 September, 1994, pp. 58 – 66.

[1.67] Liang, Y. and Nwankpa, C.O., "New type of STATCOM based on cascading voltage source inverters with phase-shifted unipolar SPWM", Conference Record of IAS '98, the 1998 IEEE Industry Applications Society 33rd Annual Meeting, 12 - 15 October, 1998, Vol. 2, pp. 1447 – 1453.

[1.68] Min, W., Min, J. and Choi. J., "Control of STATCOM using cascade multilevel inverter for high power application", Proceedings of PEDS '99, 3rd International Conference on Power Electronics and Drive Systems, 27 - 29 July, 1999, Vol. 2, pp 871 – 876.

[1.69] Tolbert, L.M.; Peng, F.Z.; Habetler, T.G., "A multilevel converter-based universal power conditioner", Proceedings of PESC '99, 30th IEEE Power Electronics Specialists Conference, 27 June-1 July 1999, Vol. 1, pp. 393 - 399.

[1.70] IEC Standard EN61000-3-2, "Electromagnetic compatibility (EMC) part 3: Limits – section 2: Limits for harmonic current emissions (equipment input current <= 16A per phase)", 15th March, 2001.

[1.71] IEEE Std. 519-1992, "IEEE recommended practices and requirements for harmonic control in electrical power systems". IEEE Inc., USA, 12 April 1993.

[1.72] IEEE Std. 1547-2003, "IEEE standard for interconnecting distributed resources with electric power systems", IEEE Inc., USA, 26th July, 2003.

Chapter 2 CONVERTER MODELLING AND ANALYSIS

2.1 Introduction

The flying-capacitor multilevel converter, the subject of this thesis, was first proposed by Meynard and Foch in 1991 [2.1]. In this chapter the existing knowledge on the circuit and its' applications are reviewed through the published literature. Later sections then explain the circuit operation and address the necessity to balance the cell-capacitor voltages. A simple matrix model is developed to provide a means for basic circuit modelling and as a tool for further circuit analysis. Options for more advanced simulation of the circuit, especially for investigating the effect of the capacitor voltage variations on performance, are explored in later sections. Finally, the inverter simulator program specifically developed for this research work is described. The generic load model and power quality definitions used throughout the simulation and experimental work for comparative appraisal of different modulation and system balancing control strategies are also introduced. A new parameter is also proposed for assessing the performance of an inverter design based on the rating of the cell-capacitors and the amount of energy stored in the inverter.

2.2 Review of State-of-the-Art

In comparison with other multilevel converter circuits, the flying-capacitor topology has received less attention since its first disclosure in the early 1990s. In total, 153 papers have been identified as being specifically related to the flying-capacitor converter topology and published up until 2004. Of these, around 40% are linked directly to the work of Meynard et al. at the Institut National Polytechnique de Toulouse, France. Figure 2.2.1 shows the number of papers published globally in journals and conferences since 1992. The total number of papers includes 46 English and 16 non-English language journal papers. As can be seen, interest in the topology from other researchers has only happened relatively recently, but the level of publications is still quite low. In comparison there have been at least 206 papers published on other multilevel inverters in 2004 alone.

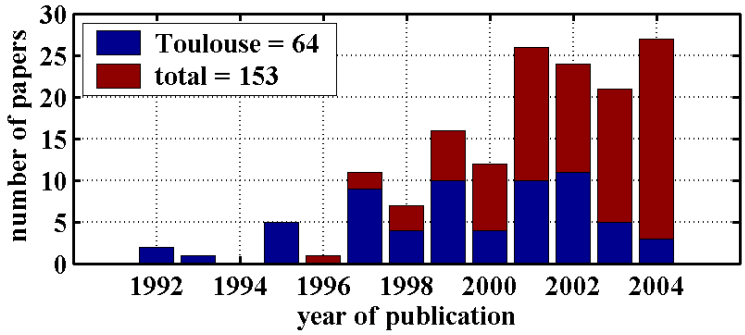


Figure 2.2.1: Annual flying-capacitor paper publication rate

The Toulouse group's progress in developing the flying-capacitor circuit in both chopper and inverter can also charted through the patents filed over the intervening period since their first disclosure [2.1]. There have been 11 individual patent filings and their main industrial collaborators, the Alstom group of companies, are the principal beneficiaries of the intellectual property rights. The implications of this are that other companies seeking to commercialise the flying-capacitor converter will probably need to obtain licensing rights before 2010 at the very least. This is the most likely reason why the amount research on the flying-capacitor converter topology around the globe has been low.

The significant amount of academic literature published by the Toulouse group has covered various aspects of the flying-capacitor topology. Their work initially focussed on the circuit's basic operation, especially as a chopper [2.2, 2.3], and led to the development of the 3 kV to 1.5 kV three-cell GTO chopper for the Alstom T13 locomotive, 80 of which now operate on European railways [2.4]. The extension of the capacitor-clamping concept to inverters was also reported at an early stage [2.5, 2.6], and work has been reported on inverter limbs with eight levels [2.7].

The inherent self-balancing capability of the circuit was understood from an early stage [2.8], although a fuzzy logic controller to improve closed-loop capacitor voltage balanced was later developed [2.9]. Significant work, initially on modelling the capacitor voltages variations [2.10], has led to the development of voltage observers for use in active cell-capacitor voltage regulation [2.11]. A phase-shifted carrier PWM control strategy has been favoured by the group for modulating the output voltage of the flying-capacitor inverter in most papers [2.12], and no work has been reported on alternative modulator control strategies.

The more recent work has led to the extension of the cell concept to a wide variety of derived multi-cell topologies. The so-called stacked multicell converter [2.13] combine two standard inverter limbs together, sharing one set of series connected switches, with cell-capacitors arranged in between the switches. Figure 2.2.2 shows an

example of the stacked multicell. Note that the current is blocked from flowing when both switches are off in the common centre limb. These topologies give increased numbers of voltage levels, and reduce the size of the capacitors, as an alternative to simply increasing the number of cells in the standard flying-capacitor inverter. Other derived topologies investigated include various quasi-resonant, soft-switching converters [2.14]. Another important issue regarding the power converter stage investigated by the group has been failure modes of different parts of the circuit and remedial control techniques for fault-tolerance [2.15, 2.16].

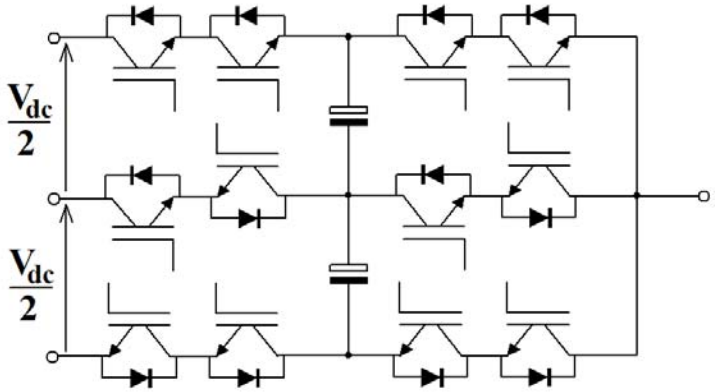


Figure 2.2.2: Stacked multicell converter circuit

In terms of applications areas, the Toulouse group have investigated a direct torque controlled (DTC) induction motor drive [2.17] and active harmonics filtering [2.18]. Meynard has also collaborated with researchers in Canada on an uninterruptible power supply (UPS) [2.19]. He also collaborated with researchers at Stellenbosch who have been investigating the flying-capacitor inverter for a number of years [2.20, 2.21].

There has been some significant work reported by researchers from other institutions. Of significance is the work at Grenoble on a sliding mode capacitor voltage control (CVC) algorithm, which has been shown to improve the dynamic performance of the inverter in an induction motor application [2.22, 2.23]. Researchers at Eindhoven, have investigated capacitor voltage balancing using system modelling [2.24] and have developed detailed analytical models for calculating the losses in the cell-capacitors to aid practical inverter design [2.25].

In respect to control strategies, specific research on the flying-capacitor inverter is sparse. However, other multilevel inverter modulation schemes described in the literature can also be applied to the flying-capacitor inverter in conjunction with a relevant capacitor voltage balancing strategy. Researchers at Hanyang University have investigated carrier rotation for multi-carrier PWM schemes and reported the

balancing properties when applied to the flying-capacitor inverter [2.26, 2.27]. Researchers at Zhejiang University have developed a carrier scheme which varies the triangular carrier amplitude in order to balance through firing rotation [2.28]. They have also investigated the relationships between PWM control and switching loss [2.29].

Agelidis et al., at the University of Glasgow have investigated the flying-capacitor inverter under phase shifted PWM control. They have simulated a novel balancing scheme which uses an injected small square wave in the reference [2.30]. The target application of this work is for high voltage ac power conditioning systems such as a unified power flow controller [2.31].

Researchers at Tsinghua University have recently published their work on a simplified PWM algorithm which incorporates rule based firing rotation for balancing and claims to give similar performance to a space vector algorithm [2.32]. Space vector modulation itself has been investigated for the flying-capacitor inverter by Mendes et al. [2.33]. They have developed a space vector algorithm for multilevel inverters in general, and achieve capacitor voltage balancing independently of the modulator by separately sensing the capacitor voltages and currents, and adjusting the inverter firing accordingly.

Researchers at Queensland University [2.34] have developed a hysteresis current controller which they implemented in an FPGA and used to control a flying-capacitor inverter. Like Mendes, they have used voltage and current sensing with a rule-based controller to achieved balancing.

Some work has been undertaken at the Swiss Federal Institute of Technology on a soft-switching three-level inverter, which uses additional circuitry for forming a resonant circuitry to ensure zero-voltage switching in the main power devices [2.35]. By controlling the four addition power switches, the clamping capacitor voltage is balanced. They have also done some detailed analytical work on the self-balancing mechanism [2.36]. Song researching at Virginia Tech. has also performed a detailed investigation on soft-switching flying-capacitor topologies targeted at active power filtering applications, and has developed rule based capacitor voltage balancing strategies for these systems [2.37].

Workers at Wisconsin University have investigated fault tolerance in the flying-capacitor inverter, and analysed the behaviour under different switch failures and the resultant effect on output voltage level and distortion [2.38]. There work assumes that the system voltages are all balanced.

Other work reported on capacitor voltage balancing include SUPERLEC team's investigation on capacitor voltage balancing using voltage sensing and a hysteresis

band controller [2.39]. Researchers at Lille have also investigated voltage balancing but focussed more on modelling the behaviour of the circuit. [2.40].

National Yunlin University investigators have been researching active front-end rectifiers and power factor correction, and have published a significant number of papers on this subject over the last four years [2.41, 2.42].

Commercially, very little has been reported on real application development although, workers at Alstom (USA) have investigated a power line conditioner application [2.43]. Developers at Alstom (Germany) described the SYMPHONY drive family which are designed for induction motors up to power ratings of 3000 HP [2.44]. They also presented possible application areas for the drive system including large off-shore wind turbine generators. Another paper from Alstom (Germany) reported on control techniques which adjusts the control for balancing purposes depending on the difference in voltage between two adjacent cell-capacitors [2.45]. The Alstom group have the rights to the original patents on the flying-capacitor converter, and have filed a group of patents with respect to the chopper circuit for the T13 locomotive [2.46].

ABB (Sweden) have also been investigating the commercial application of the inverter in power conditioning systems, and they have filed a number of patents on the balancing control of the inverter [2.47].

In a departure from the conventional applications of the flying-capacitor converter topology, researchers at Xi'an Jiaotong University have proposed a multilevel matrix converter [2.48], which uses a two-cell converter arrangement in place of a single bi-directional switch, and with the flying capacitors operating with ac voltage rather than dc.

Overall, there has been no work published specifically on flying-capacitor inverter control optimisation for sinusoidal voltage generation using staircase (selective harmonic elimination). Although various PWM control strategies have been adopted by different research groups, there has been no in depth comparative analysis of the various multi-carrier PWM techniques. The effects of cell-capacitor voltage variation on performance and the trade-offs between control strategies and capacitor size is another area where no significant work can be found in the public domain. These issues are of practical importance in future flying-capacitor inverter commercial development, and it is these areas where the work reported in this thesis is primarily focussed.

2.3 Fundamental Circuit Operation

2.3.1 Flying-Capacitor Converter Topologies

The basic building block of any power converter circuit is the chopper module, where a source dc voltage supply is sequentially connected on and off to an output circuit, and together with additional circuitry forms a power converter. There are two forms of power circuit module for the three-level flying-capacitor chopper topology. These chopper circuits operate with only unidirectional current flow and can be configured as dc-dc converter circuits with the addition of inductors and capacitors in the same way as conventional single-switch, switch-mode regulators. Figure 2.3.1 shows the high-side module in a step-down, buck regulator circuit, and Figure 2.3.2 shows the low-side module in a step-up, boost regulator circuit. Other potential applications include single-quadrant adjustable speed dc motor drives and regenerative energy dumps in other motor drive systems.

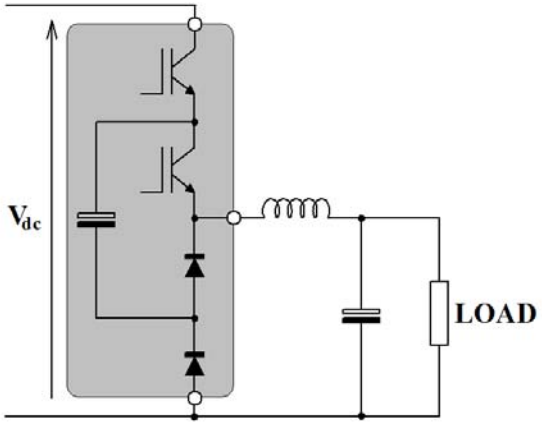


Figure 2.3.1: Buck regulator using high-side chopper module

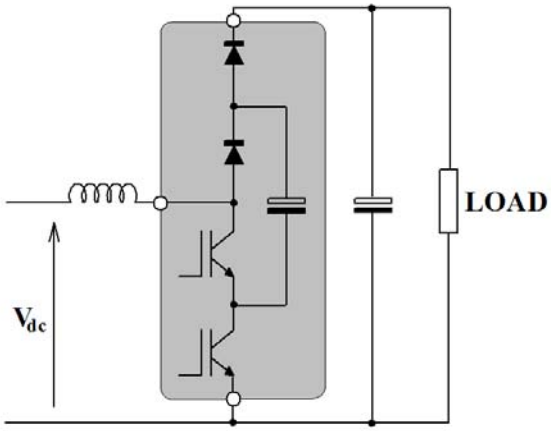


Figure 2.3.2: Boost regulator using low-side chopper module

By combining the two chopper module circuits, bridge circuits can be realised. Three basic forms of bridge circuit can be realised using the three-level chopper modules. Figure 2.3.3 shows the asymmetric bridge consisting of a single high- and low-side chopper. The load current is unidirectional, and so this topology is only suitable for forward converter switched-mode power supplies and switched reluctance machine drives [2.49]. Bidirectional load current flow is achieved by paralleling a high- and low-side chopper, to form a bridge inverter limb. Figure 2.3.4 illustrates the half-bridge topology while Figure 2.3.5 illustrates the full-bridge topology. The inverter bridge can be further extended to multi-phase circuits; most significantly for the majority of application requirements, the three-phase bridge.

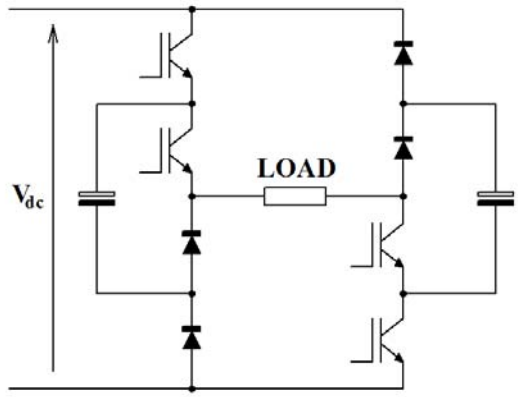


Figure 2.3.3: Asymmetric bridge circuit

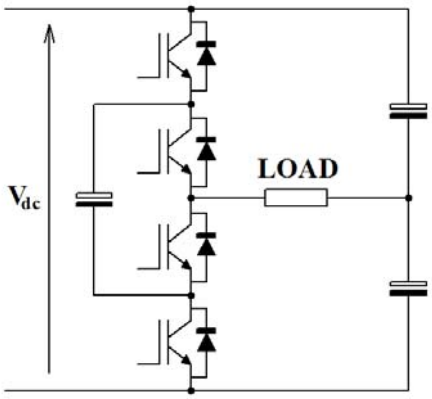


Figure 2.3.4: Half-bridge circuit

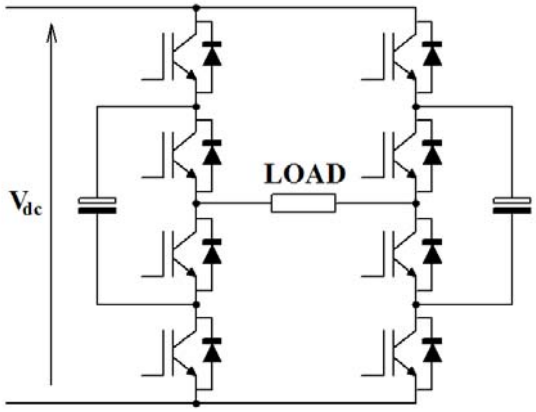


Figure 2.3.5: Full-bridge circuit

The flying-capacitor topology can be easily extended to more voltage levels by adding additional switch pairs and a capacitor. An inverter limb is in the form of a series of connected cells nested inwardly toward the load from the dc link. Figure 2.3.6 illustrates the three-cell configuration. Each cell, as shown in the figure, is composed of a capacitor and two power switches, with the outer cell being the dc link capacitor, not shown. These switches require bidirectional current paths, of which one path is controlled, for example using an IGBT with an anti-parallel diode. Each of the two cell power transistors are operated in a complementary manner. By convention, the cell-capacitors are shown as multiples of a single unit cell-capacitance, indicating the increasing voltage across each capacitor for cells nearer the high-voltage, dc link.

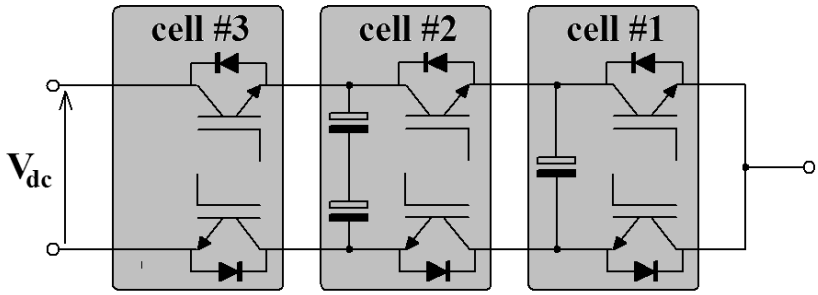


Figure 2.3.6: Four-level inverter limb

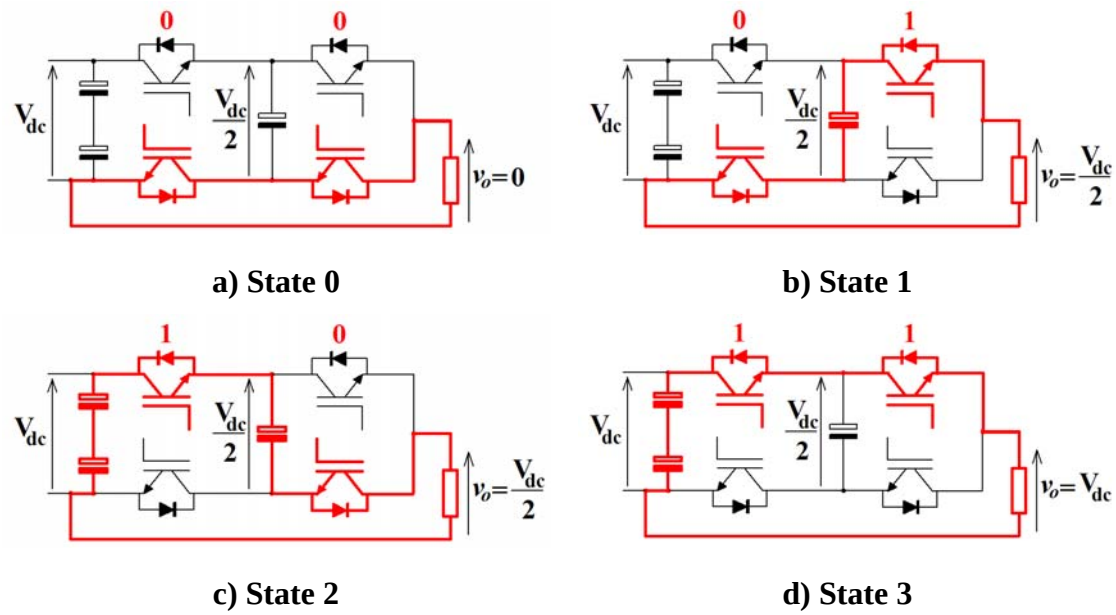
The number of voltage levels in the flying-capacitor inverter is a function of the number of complementary switch pair cells. An *N*-cell inverter limb has *2N* switches and can provide *N+1* distinct dc voltage levels from zero to V_{dc} at the load terminal with respect to the negative dc link voltage. When two limbs are configured as an inverter bridge, then there can be *2N+1* distinct voltage levels across the load

terminals. In a balanced inverter, the floating cell-capacitor average voltages are ideally kept at multiples of V_{dc}/N. Therefore, the cell-capacitor voltages will range between V_{dc}/N and $(N-1)V_{dc}/N$, with the lowest voltage across the capacitor associated with the complementary switch pair nearest the load terminal.

2.3.2 Inverter Operating States

The flying-capacitor inverter limb is controlled by operating all the complementary switch pairs so that either a high- or low-side transistor is commutated in each cell. If both switches are turned-on then this will lead to failure since it constitutes a shoot-though in the load connected cell or an unconstrained current path between a higher voltage capacitor and a lower voltage capacitor in the other cells. When both switches in a cell are not driven on, which is the case when dead-times are introduced to avoid shoot-through between cell state changes, then the polarity of load current flowing at the lower capacitor terminals will dictate which path the current will take via one of the anti-parallel diodes.

In the case of the basic two-cell inverter limb, there are four possible switching states (cell conduction states). Figure 2.3.7 shows the four current conduction paths for a load connected to the negative dc link terminal. As can be seen, there are two ways in which the half-voltage level can be applied to the output terminal. The highest and lowest voltage level states are characterised by either all high- or low-side switches conducting respectively. The figure highlights the transistor and diode in a conducting switch. In reality the current will flow through only one of the constituent solid-state devices. For instance, if the inverter is controlled in state 1 and the load current polarity is positive, then the IGBT is in conduction in the high-side switch of the load connected cell, and the diode is conducting in the low-side switch of the dc link connected cell.



a) State 0 **b) State 1**

c) State 2 **d) State 3**

Figure 2.3.7: Two-cell inverter limb operating states

The voltage level contribution of an *N*-cell inverter limb will depend on the number of high-side switches in conduction. Therefore, with *N* switches in conduction, the N^{th} voltage level is applied at the load terminal with respect to zero. This voltage can be expressed by

$$v_o = \frac{V_{dc}}{N}\sum_{n=1}^{N} S_n \qquad \ldots (2.3.1)$$

where the switch states are assigned S_0, S_1 … S_{N-1}, and logic '1' represents the high-side switch in conduction and the low-side switch in its inert state.

The total number of switching states in an *N*-cell inverter is given by 2^N. The number of states for the m^{th} voltage level, LEV_m, is the number of possible combinations of *m* logic '1's occurring in switching state *S*. These values lie in Pascal's (or Yanghui) triangle and can be calculated using the following formula

$$LEV_m = \frac{(N-1)!}{(N-1-m)!(m)!} \qquad \ldots (2.3.2)$$

The complexity of the inverter and the control task greatly increases with the number of cells. Table 2.3.1 shows the number of components and states in a flying-capacitor inverter as the number of cells is increased. The capacitor number is based on the assumption that the inverter is constructed using a unit capacitor size, and the dc link has *N* capacitors for an *N* cell inverter irrespective of phase number. In reality, the capacitor sizing will be based on the maximum link voltage, output load requirements and the practical implications of the semiconductor switch ratings and operating control scheme. Therefore, the table is purely an indication of inverter complexity

rather than a comparative reference. The row of data for a single cell inverter represents a conventional two-level case.

Cells	Single Phase Limb			Three-Phase Bridge		
	Load Voltage Levels	Switches	Capacitors	Load Voltage Levels	Switches	Capacitors
1	2	2	1	3	6	1
2	3	4	3	5	12	5
3	4	6	6	7	18	12
4	5	8	10	9	24	22
5	6	10	15	11	30	35
6	7	12	21	13	36	51

Table 2.3.1: Flying-capacitor inverter complexity

2.3.3 System Balancing Requirement

It has already been shown that there is more than one switching state capable of providing an intermediary level voltage at the load terminal of the inverter. If the cell-capacitors were ideal with infinite capacitance, then the control task would be relatively simple. However, in a real system the different switching states at a given voltage level lead to different current paths within the flying-capacitor inverter circuit. The current flowing through the cell-capacitors will cause the voltages to vary proportionally with the amplitude, duration and polarity of the current.

Increasing or decreasing capacitor voltage is related to the switch states in adjacent cells to the capacitor. If these switch states are not equal then current will flow in the capacitor. Figure 2.3.8 illustrates the two cases for current flow in a capacitor. As can be seen, if the upper switch state is ‘1’ and the lower ‘0’, then current will flow positively into the capacitor when the load current is positive and the capacitor voltage is increased. For the inverted switch state case, the voltage will decrease with a positive load current. The opposite is true for a negative load current. If the adjacent states are equal then the capacitor is bypassed and there is no effect on its voltage.

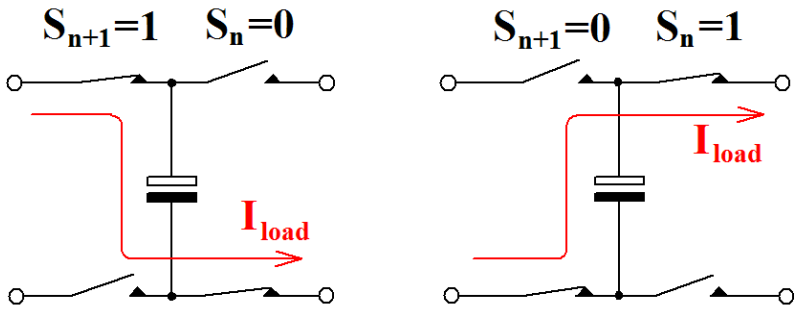


Figure 2.3.8: Current flow paths in a cell capacitor

In the case when there is a constant dc load current, then the inverter control will have to ensure that the time spent in each switching state is equal to achieve balanced capacitor operation. This will also ensure that the inverter is thermally balanced with the losses in the upper set of semiconductor switches are the same. The losses in the lower set of switches will also be the same, but not necessarily equal to the upper switches since the current direction is reversed, and so the diodes will conduct rather than the transistors. The amplitude of the voltage ripple in the cell-capacitor voltage will depend on the switching frequency chosen for control in respect to the capacitance and load current amplitude.

For an N-cell inverter when $m = 1$ or $m = N\text{-}1$, and the output voltage levels are V_{dc}/N or $(N\text{-}1)V_{dc}/N$ respectively, there are N different switching state possibilities (2.3.2). To affect the desired balanced operation, then the control must cycle through all N states when applying these two voltage levels. For inverters with $N > 3$, there are additional middle-range voltage levels with more than N different switching states. In the case when $N = 4$, there are 6 different switching states which give an output voltage of $V_{dc}/2$ with respect to the negative dc link. These are listed in Table 2.3.2. These states can be grouped into three complementary pairs: 3 & 12, 5 & 10 and 6 & 9. To accomplish the capacitor voltage and thermal balancing, it is only necessary to cycle through one of the switching state pairs. This is also the case for the half-voltage level in higher even cell number inverters.

State Number	Switching State S
3	0011
5	0101
6	0110
9	1001
10	1010
12	1100

Table 2.3.2: Switching states for 4-cell inverter, *m* = 2

When the cell number, *N*, is greater than 4 and is odd, then complementary pairing of states cannot be exploited for complete system balancing. Taking the 5 cell case as an example, there are 10 switching states for the mid-voltage levels listed in Table 2.3.3. In this case all 10 states must be cycled through to achieve balanced operation.

State Number	Switching State S
3	00011
5	00101
6	00110
9	01001
10	01010
12	01100
17	10001
18	10010
20	10100
24	11000

Table 2.3.3: Switching states for 5-cell inverter, *m* = 2

When the cell number is even, then the states between the half- and boundary voltage levels can be grouped through symmetry. For instance, the 6-cell inverter, at level m = 2 there are 15 different states, and 15 groups of three states can be identified which if cycled through will give balanced operation. The balancing sets for S in binary notation are listed as follows:

$$\left\{\begin{matrix}000011\\001100\\110000\end{matrix}\right\},\left\{\begin{matrix}000011\\010100\\101000\end{matrix}\right\},\left\{\begin{matrix}000011\\011000\\100100\end{matrix}\right\},\left\{\begin{matrix}000101\\001010\\110000\end{matrix}\right\},\left\{\begin{matrix}000101\\010010\\101000\end{matrix}\right\},$$

$$\left\{\begin{matrix}000101\\011000\\100010\end{matrix}\right\},\left\{\begin{matrix}000110\\001001\\110000\end{matrix}\right\},\left\{\begin{matrix}000110\\010001\\101000\end{matrix}\right\},\left\{\begin{matrix}000110\\011000\\100001\end{matrix}\right\},\left\{\begin{matrix}001001\\010010\\100100\end{matrix}\right\},$$

$$\left\{\begin{matrix}001001\\010100\\100010\end{matrix}\right\},\left\{\begin{matrix}001010\\010001\\100100\end{matrix}\right\},\left\{\begin{matrix}001010\\010100\\100001\end{matrix}\right\},\left\{\begin{matrix}001100\\010001\\100010\end{matrix}\right\},\left\{\begin{matrix}001100\\010010\\100001\end{matrix}\right\}$$

The numbers of states that constitute a balancing group at different voltage levels for a range of cell number inverters are listed in Table 2.3.4. These represent the minimum number of states which have to be cycled through in order to achieve balanced system control. The numbers in brackets are the total number of unique states at the given levels. Balancing of the inverter for low cell number inverters is relatively straightforward and can be accomplished by cycling through the small set of balancing states. These can be stored digitally in the control hardware keeping the complexity down to a minimum. Once the number of cells exceeds 6, then the large number of states which have to be incorporated within the control algorithm is excessive and so places huge demands on the control system.

Cell Number *N*	**Level Number *m***						
	1	**2**	**3**	**4**	**5**	**6**	**7**
2	2 (2)						
3	3 (3)	3 (3)					
4	4 (4)	2 (6)	4 (4)				
5	5 (5)	10 (10)	10 (10)	5 (5)			
6	6 (6)	3 (15)	2 (20)	2 (15)	6 (6)		
7	7 (7)	21 (21)	35 (35)	35 (35)	21 (21)	7 (7)	
8	8 (8)	4 (28)	56 (56)	2 (70)	56 (56)	4 (28)	8 (8)

Table 2.3.4: Minimum number of states for balancing

In the majority of multilevel inverter applications, the output voltage is a periodic waveform which approximates as closely as possible to a pure sinusoid. Therefore, the control can rotate through each member of the balancing set at a given voltage level

cycle by cycle. The premise being that in the steady-state, the current is equal at the same point in the cycle. Therefore, for low even cell number inverters, the number of cycles before a sequence of switching states is repeated is equal to the number of cells. In the case of a 5-cell inverter, this is twice the number of cells, because the half-voltage level requires all 10 states to be used. Figure 2.3.9 shows an example of this control method applied to a 3-cell inverter where the required sinusoidal output voltage is approximated by a staircase waveform. As can be seen, the switching states are different in each cycle at the same point in the output voltage waveform, and the cycling repeats after 3 cycles.

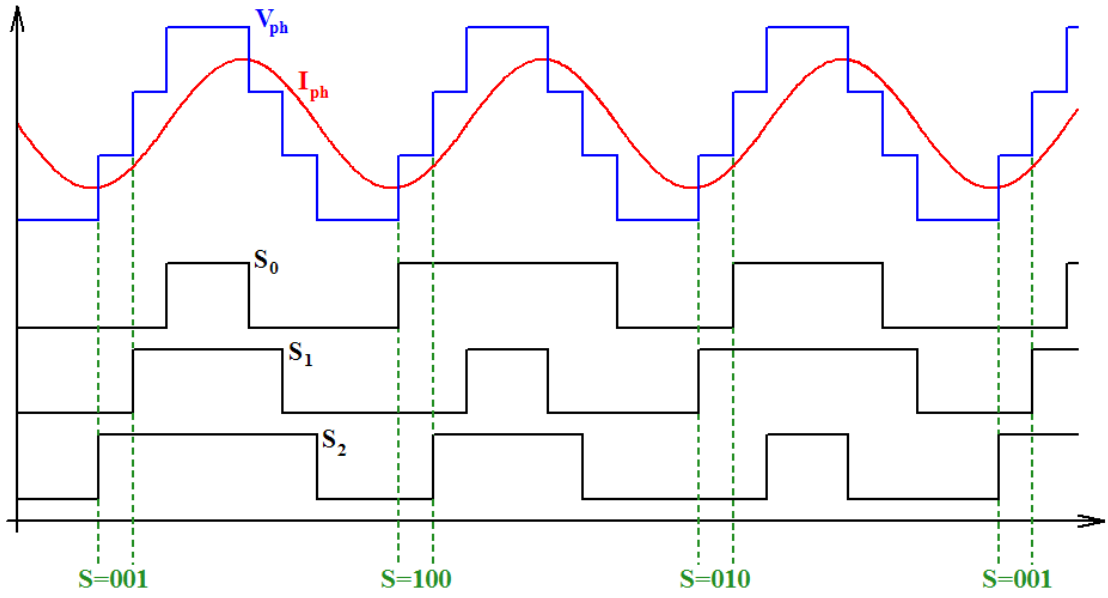


Figure 2.3.9: Firing waveforms for simple state rotation balancing in a three-cell inverter limb

In a real system, with finite voltage ripple on the cell-capacitors, this form of balancing will inevitably lead to sub- and inter-harmonic components being present in the output. With a repeating balancing pattern made up of a set of sequences of states every B cycles, then the lowest frequency component will be at f_1/B Hz where is f_1 is the target output fundamental frequency. These low frequency components are difficult to filter and can pose problems in a real load. Therefore, care must be taken in inverter capacitor selection in conjunction with control optimisation to minimise these effects.

There are a number of different sequence permutations, which will achieve the desired system balancing, and these increase with the number of inverter cells. The number of possible sequences, *SEQ*, is the product of the number of different states at each level.

In a cycle by cycle sequence rotation approach, then the number of possible patterns, P, is calculated by (2.3.4). These permutation numbers for a single phase limb are listed in Table 2.3.5.

$$P = \left(\frac{SEQ}{B} \right)^{x} \quad \ldots (2.3.4)$$

where

$$x = \sum_{n=1}^{B} n \quad \ldots (2.3.5)$$

Cell Number, *N*	**Number of Cycle Sequences, *SEQ***	**Minimum Cycle Number, *B***	**Number of Patterns, *P***
2	2	2	1
3	9	3	162
4	96	4	7962624
5	2500	10	3.460693×10^{30}
6	162000	6	2.789428×10^{29}
7	26471025	35	5.872562×10^{245}
8	1376829440	56	$3.504436 \times 10^{11795}$

Table 2.3.5: Number of balancing permutations

The excessive number of patterns for cell numbers greater than 4 makes pattern optimisation very difficult. By introducing rules to exclude certain sequences and combinations of sequences, then it may be possible to apply a pattern generation algorithm to the balancing control problem. For instance, switching frequency losses will be minimised by reducing the number commutation transitions within a sequence. Using only the sequences involving one switch state change per level transition will reduce the number of permutations. Alternatively, using cell-capacitor voltage feedback, the control itself can select the state or sequence within a cycle to maintain the capacitor voltages within the desired bands. The potential for ‘chaotic’ behaviour and the generation of unwanted very low frequency harmonics is clear especially in higher cell number inverters. These are the challenges faced in balancing the flying-capacitor inverter.

2.4 Modelling of Flying-Capacitor Inverter

2.4.1 Laplace Circuit Analysis of Capacitor Voltages

The two-cell flying-capacitor chopper circuit, shown in Figure 2.4.1, is the simplest form of the inverter topology family. There is only one capacitor and each power switch pair operate in a complementary manner so that there are four operating switching states.

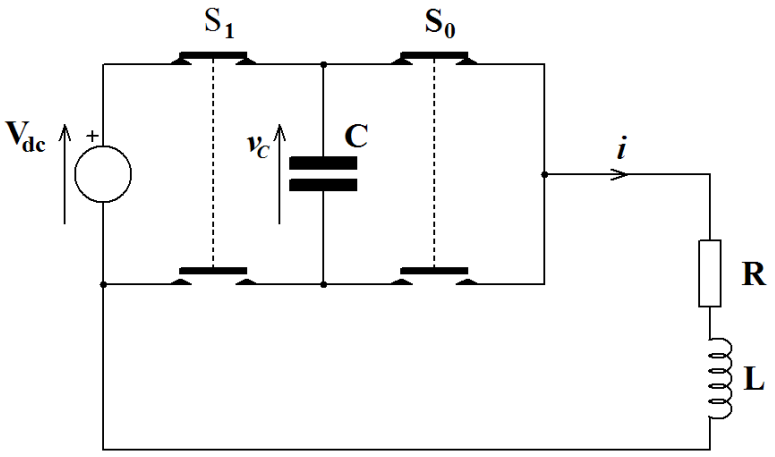


Figure 2.4.1: Two-cell inverter limb

The subject of this analysis, the capacitor voltage, is only connected in the circuit conduction path when the half voltage levels are applied across the load. The Laplace equivalent circuit for these two states [2.50], including the initial capacitor voltage v_{c0} and initial inductor current i_{L0}, are shown in Figures 2.4.2 and 2.4.3.

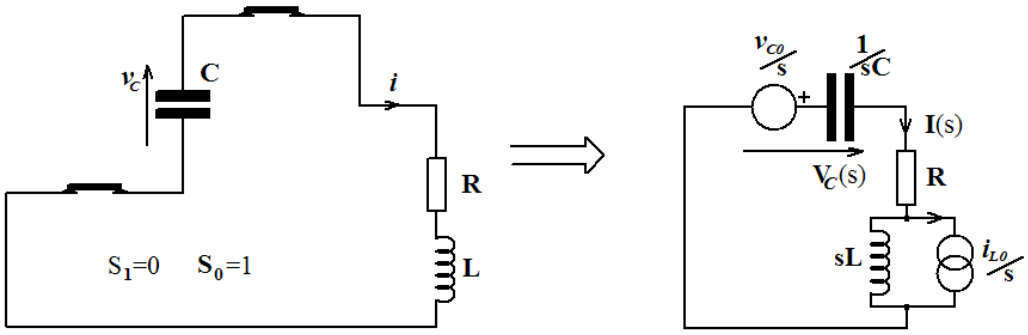


Figure 2.4.2: Laplace equivalent circuit for switch state 1

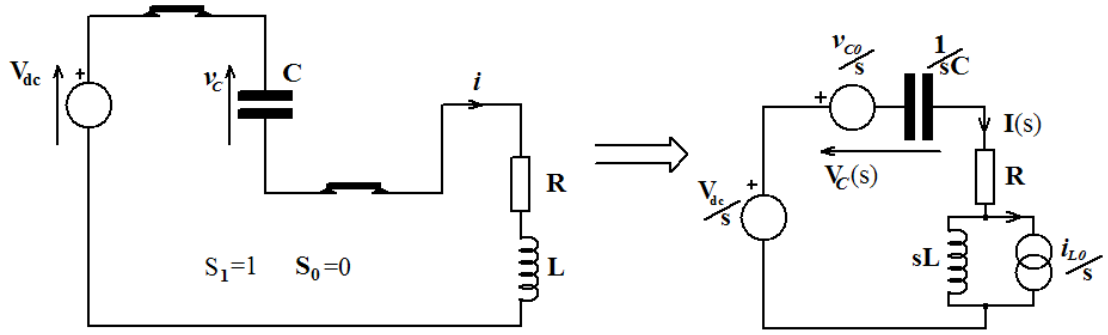


Figure 2.4.3: Laplace equivalent circuit for switch state 2

The Laplace transforms for state 1 are given by

$$V_C(s) = I(s)R + \left(sI(s)L - i_{L0}L\right) \quad \ldots (2.4.1)$$

$$I(s) = -C\left(sV_C(s) - v_{C0}\right) \quad \ldots (2.4.2)$$

By rearranging the equations (2.4.1 and 2.4.2), the state 1 Laplace transform for the capacitor voltage is given by

$$V_C(s) = \frac{v_{C0}CR + sv_{C0}CL}{\left(1 + sCR + s^2CL\right)} - \frac{i_{L0}L}{\left(1 + sCR + s^2CL\right)} \quad \ldots (2.4.3)$$

The Laplace transforms for state 2 are given by

$$V_C(s) = \frac{V_{DC}}{s} - I(s)R - \left(sI(s)L - i_{L0}L\right) \quad \ldots (2.4.4)$$

$$I(s) = C\left(sV_C(s) - v_{C0}\right) \quad \ldots (2.4.5)$$

By rearranging the equations (2.4.4 and 2.4.5), the state 2 Laplace transform for the capacitor voltage is given by

$$V_C(s) = \frac{V_{DC}}{s\left(1 + sCR + s^2CL\right)} + \frac{v_{C0}CR + sv_{C0}CL}{\left(1 + sCR + s^2CL\right)} + \frac{i_{L0}L}{\left(1 + sCR + s^2CL\right)} \quad \ldots (2.4.6)$$

In a high voltage system, the following relationship is true

$$v_{C0}CR >> i_{L0}L \quad \ldots (2.4.7)$$

In other words, the energy stored in the cell-capacitor is much larger than the energy stored in the load inductor. This means that the initial inductor current can be ignored. Therefore, the two switching state circuits can be combined into an equivalent circuit as shown in Figure 2.4.4. It has already been seen that for balanced operation, the time, T, in each state must be equal. Therefore, the input supply voltage is shown as a square-wave voltage with amplitude V_{dc}.

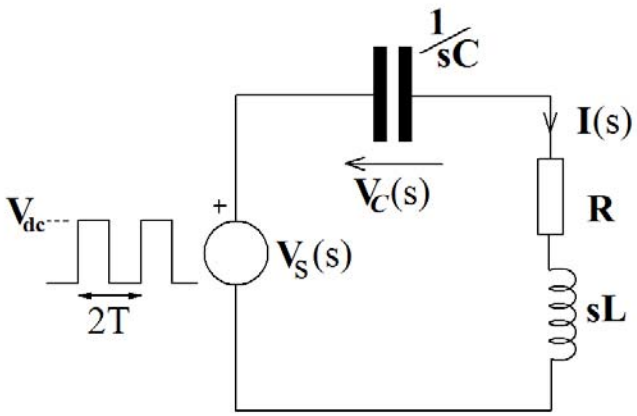


Figure 2.4.4: Two-cell inverter combined equivalent circuit

The Laplace transform of the capacitor voltage function is given by:

$$V_C(s) = \frac{1/sC}{\left(R + 1/sC + sL\right)} V_s(s) \quad \ldots (2.4.8)$$

where

$$V_s(s) = \frac{V_{dc}}{s\left(1 + e^{-Ts}\right)} \quad \ldots (2.4.9)$$

The final value of v_C can be found using the Final Value Theorem:

$$\lim_{t\to\infty} v_C(t) = \lim_{s\to 0} sV_C(s) \quad \ldots (2.4.10)$$

$$v_C(t \to \infty) = \frac{V_{dc}}{2} \quad \ldots (2.4.11)$$

Therefore, the two-cell flying-capacitor inverter will naturally balance with the average capacitor voltage at half the dc link, as long as the switching time for each of the two half-voltage states is equal. The capacitor is not in-circuit for the other two inverter states, and so the voltage will still reach the equilibrium voltage of half the dc link. It is also clear from the above analysis that if the times for the two half voltage states are not equal, then the mean capacitor voltage is a function of the ratio of state 1 period to the combined period of states 1 and 2. Therefore, the control must ensure averaged equal times for each state otherwise asymmetry will result in the output voltage. Any variation in the switching times will also be reflected in a similar variation in capacitor mean voltage, and potentially result in unwanted harmonics in the output.

The equivalent Laplace transform for the inverter can be used to find the time-domain equation for the system, and give some insight into capacitor voltage ripple and

charging transients. Equation (2.4.8) can be rewritten to incorporate a natural resonant frequency and damping factor for the 2nd order denominator term. This gives the following Laplace transform.

$$V_C(s) = \frac{\omega_n^2}{\left(s^2 + 2\zeta\omega_n s + \omega_n^2\right)} \frac{V_{dc}}{s\left(1 + e^{-Ts}\right)} \quad \ldots (2.4.12)$$

where

$$\omega_n = \sqrt{\frac{1}{CL}} \quad \ldots (2.4.13)$$

$$\zeta = \frac{R}{2}\sqrt{\frac{C}{L}} \quad \ldots (2.4.14)$$

and the roots s_1 and s_2 are

$$s_1, s_2 = \zeta\omega_n \pm \omega_n\sqrt{\left(\zeta^2 - 1\right)} \quad \ldots (2.4.15)$$

$$\omega_n^2 = s_1 s_2 \quad \ldots (2.4.16)$$

To obtain the time-domain equation for the capacitor voltage, equation (2.4.12) is first factorised before performing the inverse Laplace transform [2.51].

$$V_C(s) = \frac{\omega_n^2}{(s + s_1)(s + s_2)} \frac{V_{dc}}{s\left(1 + e^{-Ts}\right)} \quad \ldots (2.4.17)$$

$$V_C(s) = \frac{A_1}{(s + s_1)\left(1 + e^{-Ts}\right)} + \frac{A_2}{(s + s_2)\left(1 + e^{-Ts}\right)} + \frac{A_3}{s\left(1 + e^{-Ts}\right)} \quad \ldots (2.4.18)$$

$$V_C(s) = \omega_n^2 V_{dc}\left[\begin{array}{l} \dfrac{1/s_1(s_1 - s_2)}{(s + s_1)\left(1 + e^{-Ts}\right)} + \dfrac{1/s_2(s_2 - s_1)}{(s + s_2)\left(1 + e^{-Ts}\right)} \\ + \dfrac{1/s_1 s_2}{s\left(1 + e^{-Ts}\right)} \end{array}\right] \quad \ldots (2.4.19)$$

The inverse Laplace transform of (2.4.19) will have the form shown below:

$$v_c(t) = \omega_n^2 V_{dc}\left(f_1(t) + f_2(t) + f_3(t)\right) \quad \ldots (2.4.20)$$

where

$$f_1(t) = \frac{1}{s_1(s_1 - s_2)} e^{-s_1 t}\left[\sum_{n=0}^{\infty} e^{nTs_1}(-1)^n u(t - nT)\right] \quad \ldots (2.4.21)$$

$$f_2(t) = \frac{1}{s_2(s_2 - s_1)} e^{-s_2 t}\left[\sum_{n=0}^{\infty} e^{nTs_2}(-1)^n u(t - nT)\right] \quad \ldots (2.4.22)$$

$$f_3(t) = \frac{1}{s_2 s_1}\left[\sum_{n=0}^{\infty}(-1)^n u(t-nT)\right] \quad \ldots (2.4.23)$$

Therefore, the time domain equation for the capacitor voltage is given by the following relationships, where *u(t)* is the unit step function,

$$v_c(t) = V_{dc}\sum_{n=0}^{\infty}\frac{\omega_n^2}{s_1 s_2}(-1)^n u(t-nT)\times \left(1+\frac{s_2}{(s_1-s_2)}e^{-s_1(t-nT)}+\frac{s_1}{(s_2-s_1)}e^{-s_2(t-nT)}\right) \quad \ldots (2.4.24)$$

$$v_c(t) = V_{dc}\sum_{n=0}^{\infty}\frac{\omega_n^2}{s_1 s_2}(-1)^n u(t-nT)\times \left(1+\frac{\left(s_2 e^{-s_1(t-nT)}-s_1 e^{-s_2(t-nT)}\right)}{(s_1-s_2)}\right) \quad \ldots (2.4.25)$$

$$v_c(t) = V_{dc}\sum_{n=0}^{\infty}(-1)^n u(t-nT)\times \left(1+\frac{e^{-\zeta\omega_n(t-nT)}}{2\omega_n\sqrt{\zeta^2-1}}\left(\begin{array}{l}\left(-\zeta\omega_n-\omega_n\sqrt{\zeta^2-1}\right)e^{\omega_n\sqrt{\zeta^2-1}(t-nT)}-\\ \left(-\zeta\omega_n+\omega_n\sqrt{\zeta^2-1}\right)e^{-\omega_n\sqrt{\zeta^2-1}(t-nT)}\end{array}\right)\right) \quad \ldots (2.4.26)$$

$$v_c(t) = V_{dc}\sum_{n=0}^{\infty}(-1)^n u(t-nT)\times \left(1-\frac{e^{-\zeta\omega_n(t-nT)}}{\omega_n\sqrt{\zeta^2-1}}\left(\begin{array}{l}\zeta\omega_n\sinh\left(\omega_n\sqrt{\zeta^2-1}(t-nT)\right)+\\ \left(\omega_n\sqrt{\zeta^2-1}\right)\cosh\left(\omega_n\sqrt{\zeta^2-1}(t-nT)\right)\end{array}\right)\right) \quad \ldots (2.4.27)$$

The capacitor voltage waveform when the inverter is operated from a quiescent start has the form shown in Figure 2.4.5. This was plotted from equation (2.4.27) using MATLAB, with the circuit parameters C = 4.7 mF, R = 30 Ω, L = 100 mH, T = 50 ms and V_{dc} = 400 V. It can be seen that the mean capacitor voltage trajectory heads towards 200 V, the balanced target condition. The ripple voltage component of course can be reduced by switching at a higher frequency or increasing the capacitance.

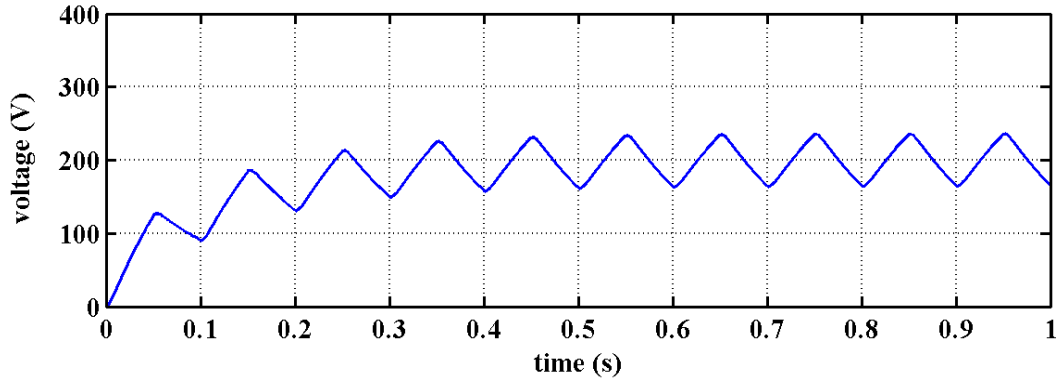


Figure 2.4.5: Transient build-up of the capacitor voltage

2.4.2 Laplace Analysis of Multi-Cell Circuit

The three-cell topology has two individual cell-capacitors and can operate with an additional intermediary voltage level. The number of switch modes is eight and each capacitor has four modes associated with its operation. Using the same analysis technique as in the two-cell case, the Laplace transform for each cell capacitor voltage can be derived. As before in the analysis, the cases when a capacitor is not in circuit with the load are ignored.

Taking the case of the three states, with only one upper switch on in each cell, and giving the lowest intermediary output voltage. This results in two simultaneous equations for each capacitor.

$$V_{C_0}(s) = \frac{\omega_n^2}{(s+s_1)(s+s_2)} \frac{V_{C_1}(s)}{s\left(1+e^{-Ts}\right)} \quad \ldots (2.4.28)$$

$$V_{C_1}(s) = \frac{\omega_n^2}{(s+s_1)(s+s_2)} \left(\frac{V_{dc}}{s\left(1+e^{-Ts}\right)} - \frac{e^{-Ts} V_{C_0}(s)}{s\left(1+e^{-Ts}\right)} \right) \quad \ldots (2.4.29)$$

Using Final Value Theorem (2.4.9):

$$sV_{C_0}(s)|_{s=0} = \frac{sV_{C_1}(s)|_{s=0}}{2} \quad \ldots (2.4.30)$$

$$sV_{C_1}(s)|_{s=0} = \frac{V_{dc} - sV_{C_0}(s)|_{s=0}}{2} \quad \ldots (2.4.31)$$

$$v_{C_0}(t \to \infty) = \frac{V_{dc}}{3} \quad \ldots (2.4.32)$$

$$v_{C_1}(t \to \infty) = \frac{2V_{dc}}{3} \quad \ldots (2.4.33)$$

The same analysis method used for the second level voltage modes, when two switches are on, also reveals the same result. This analysis in part has proven the natural voltage balancing of the flying-capacitor inverter circuit when all modes with equal voltage levels are used with equal time duration. The analysis can be further extended to higher cell numbers, resulting in the following set of simultaneous equations.

$$V_{C_0}(s) = \frac{\omega_n^2 V_{C_1}(s)}{s(s+s_1)(s+s_2)(1+e^{-Ts})} \quad \ldots (2.4.34)$$

$$V_{C_1}(s) = \frac{\omega_n^2 \left(V_{C_1}(s) - e^{-Ts} V_{C_0}(s)\right)}{s(s+s_1)(s+s_2)(1+e^{-Ts})} \quad \ldots (2.4.35)$$

$$V_{C_{N-1}}(s) = \frac{\omega_n^2 \left(V_{dc} - e^{-Ts} V_{C_{N-2}}(s)\right)}{s(s+s_1)(s+s_2)(1+e^{-Ts})} \quad \ldots (2.4.36)$$

Once the levels increase above 2-cells it is very difficult to derive a usable standard time-domain equation for the cell-capacitor voltages since it is dependent on the sequence of switching states and any pattern thereof. Therefore, for higher cell numbers an approach other than Laplace circuit analysis is required for modelling in order to simulate the different waveforms in the system.

2.4.3 Simple Circuit Model of Converter

The fundamental operation and characteristics of the flying-capacitor converter has been shown to offer a great deal of flexibility in terms of operating modes compared to conventional two-level bridges. Complexity increases dramatically as the number of levels increases and this makes it difficult to analyse operation without resorting to computer-aided circuit simulation. Therefore, a simple mathematical model is developed which can be used in MATLAB to simulate the ideal system waveforms under different control schemes.

The state-space equations for the inverter are used to construct a set of matrix equations linking the cell-capacitor voltages and the output load voltage and current. It is preferable that the equations are in a generalised form applicable to any N-cell inverter and that the power switch states vector is included separately. The following set of matrix equations was derived for the generalised N-cell inverter limb shown in Figure 2.4.6.

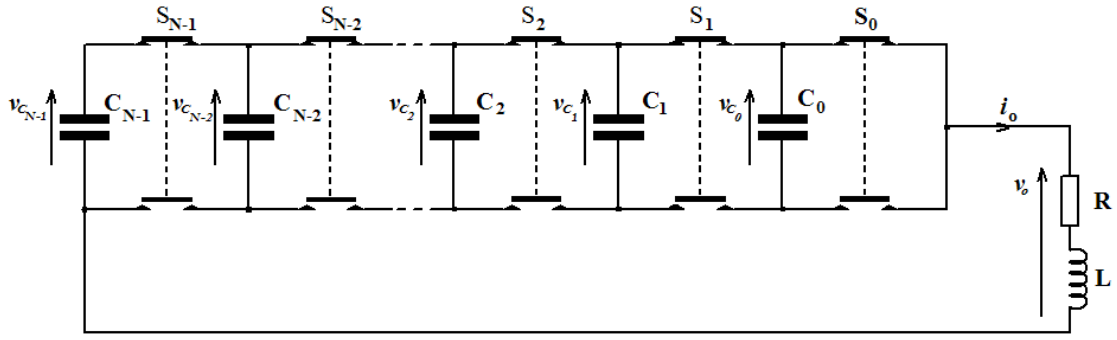


Figure 2.4.6: N-level flying-capacitor inverter limb

The three matrix based equations governing the system on a simple RL load are

$$\frac{\mathbf{dV_C}}{\mathbf{dt}} = -\mathbf{C}\mathbf{J}^{\mathbf{T}}\mathbf{S}i_o \qquad \ldots (2.4.37)$$

$$v_o = \left(\mathbf{S}^{\mathbf{T}}\mathbf{J}\right)\mathbf{V_C} \qquad \ldots (2.4.38)$$

$$\frac{di_o}{dt} = \frac{1}{L}\left(v_o - R.i_o\right) \qquad \ldots (2.4.39)$$

where

$$\mathbf{V_C} = \begin{bmatrix} v_{C_{N-1}} \\ v_{C_{N-2}} \\ \ldots \\ v_{C_2} \\ v_{C_1} \\ v_{C_0} \end{bmatrix}, \ \mathbf{S} = \begin{bmatrix} S_{N-1} \\ S_{N-2} \\ \ldots \\ S_2 \\ S_1 \\ S_0 \end{bmatrix}, \ \mathbf{J} = \begin{bmatrix} 1 & -1 & 0 & 0 & 0 & \ldots \\ 0 & 1 & -1 & 0 & \ldots & 0 \\ \ldots. & \ldots & \ldots. & \ldots & \ldots & \ldots \\ 0 & 0 & \ldots & 1 & -1 & 0 \\ 0 & \ldots & 0 & 0 & 1 & -1 \\ \ldots & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

$$\mathbf{C} = \begin{bmatrix} 1/C_{N-1} & 0 & 0 & 0 & 0 & \ldots \\ 0 & 1/C_{N-2} & 0 & 0 & \ldots & 0 \\ \ldots & \ldots & \ldots & \ldots & \ldots & \ldots \\ 0 & 0 & \ldots & 1/C_2 & 0 & 0 \\ 0 & \ldots & 0 & 0 & 1/C_1 & 0 \\ \ldots & 0 & 0 & 0 & 0 & 1/C_0 \end{bmatrix}$$

By convention $v_{C_{N-1}} = V_{dc}$ in the is the cell-capacitor voltage vector, $\mathbf{V_C}$.

The relationships contain a form of Jordan matrix, **J**, which links the switching states and the cell capacitor voltages to the phase output voltage. These matrix relationships governing the flying-capacitor inverter circuit can be incorporated within a simple

fixed time-stepping procedure to obtain the load voltage v_o and current i_o variation with a particular switch state operated over a time period. By combining different switch states operated over different time-periods any switching sequence pattern can be simulated rapidly.

For example, a MATLAB script was run to simulate one two-cell inverter limb operating in a half-bridge configuration, where one end of the load is tied to $V_{dc}/2$. Figure 2.4.7 shows the resultant load voltage and current waveforms in the steady-state condition when the inverter is operated with a simple 50 Hz staircase control scheme. The circuit parameters for this simulation were V_{dc} = 400 V, R = 10 Ω, L = 30 mH and C = 1 mF. It can be seen from the load voltage waveform that the capacitor voltage variation affects the zero voltage level, and interestingly may 'improve' the shape of the waveform, and reduce some of the unwanted harmonic components if the control and capacitance are optimised correctly. This feature has been explored in the full-bridge configuration using this matrix-based modelling as a tool and the results presented at the EPE conference, 2001 [2.52].

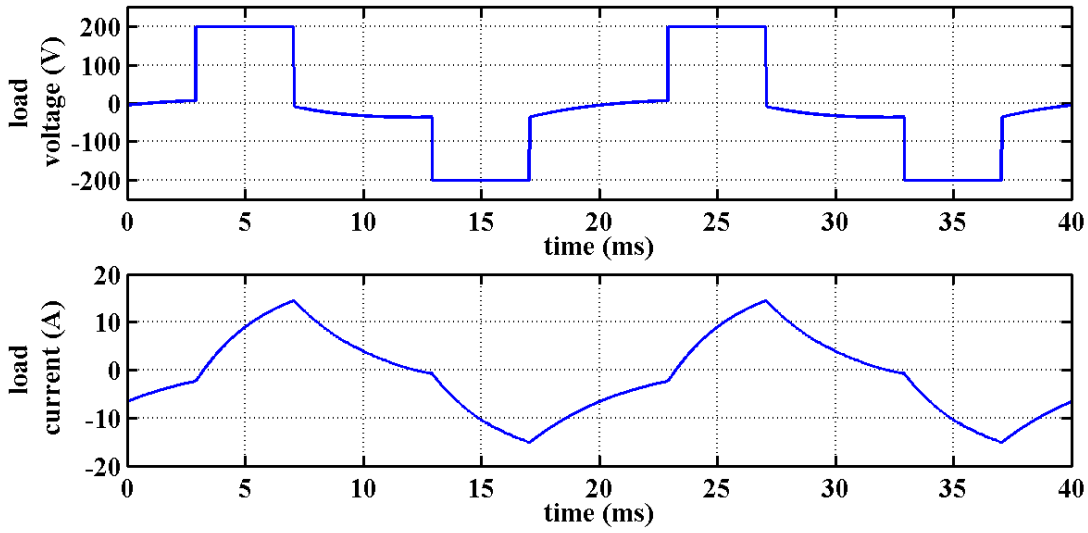


Figure 2.4.7: Two-cycles of steady-state load waveforms

The trajectory of the capacitor voltage increase from a quiescent start can be seen in Figure 2.4.8. It shows that the capacitor voltage will self-balance to $V_{dc}/2$ as expected with the half-voltage states swapping control between each cycle.

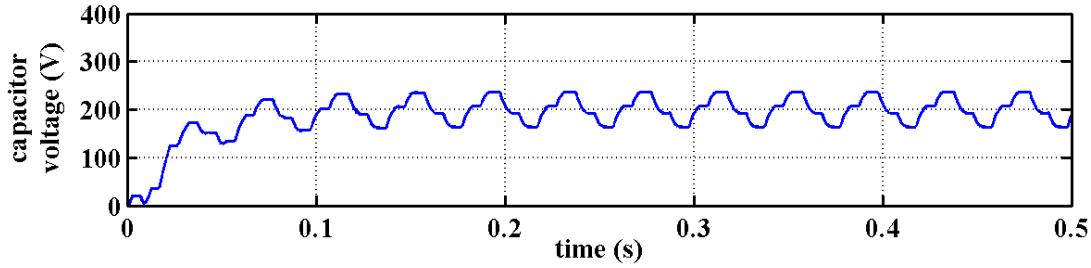


Figure 2.4.8: Capacitor voltage build-up from inert state

2.5 Development of an Inverter Simulator

2.5.1 Simulator Software Design

There are various software tools and simulation packages available for investigating power electronic converters and drives. In the past, computer aided design (CAD) packages have been developed by researchers investigating PWM connected power electronic systems. Bowes et al. at Bristol developed their own CAD package, BTRAP, to aid their PWM research [2.53]. Gateau et al. at Toulouse, however, adopted commercial packages, using a combination of SABER for power electronics and ModelSim for control logic VHDL for simulating the flying-capacitor inverter system [2.54].

Only one such simulation package was available during the project, SIMULINK, a graphical simulation addition to MATLAB. Some investigations were undertaken using the Power System Block Set, a SIMULINK toolbox containing power device and other circuit block models relevant to power electronics systems. However, it was found that the simulation time for one sinusoidal cycle was around 5 minutes on a reasonably fast computer which make very detailed simulation over a sufficient period very time consuming. Since the block set is a proprietary product, full analysis of operating parameters such as switching loss is difficult. Therefore, it was felt that a bespoke solution was needed for this project, allowing full control over the inherent sub-system modelling and offering significantly increased simulation speeds.

The development platform chosen for this work is Microsoft Visual C++, making use of the graphical user interface capabilities in Windows and the power of the C++ programming language [2.55]. A set of library classes implement various circuit elements, using object oriented programming (OOP) techniques to allow fast development of more complex system models [2.56].

In the real world any object can be thought of as having characteristics, or states, and behaviour. OOP uses this principle to instantiate (create) objects within the software,

whereby each object has variables (states) and functions or methods (behaviour). In C++, the class is the blueprint for an object and contains the necessary code to define the required object. This approach helps with modularity in terms of maintaining software, and any modifications can take place at the class level. Different objects which share common traits can be instantiated through the use of derived subclasses. This is achieved by defining an abstract class with generic states and behaviour and then through inheritance defining subclasses which have modifications for the actual objects required. This allows efficient software reuse and behaviour enhancements to be done at the abstract class level.

Applying these OOP techniques to the problem in hand, the base class for circuit simulation is an abstract class which models a two-terminal electrical component with associated behaviour common to all electrical components, i.e. a voltage appears at its terminals when a current flows through it. Derived classes can then include the standard linear components: resistor, capacitor and inductor. A specific method for obtaining the voltage or current at a specific instance in time is used in each case. This uses the basic piecewise linear circuit equations for the component for a small fixed time-step. Using these classes, more complex circuits can be modelled by instantiating each component in the code. Some degree of knowledge has to be adopted, since stable simulations are more likely to be achieved if the integral circuit equations are used for obtaining nodal voltages or currents for passive energy storage devices. Figure 2.5.1 illustrates the simplified class hierarchy of the modelling C++ library.

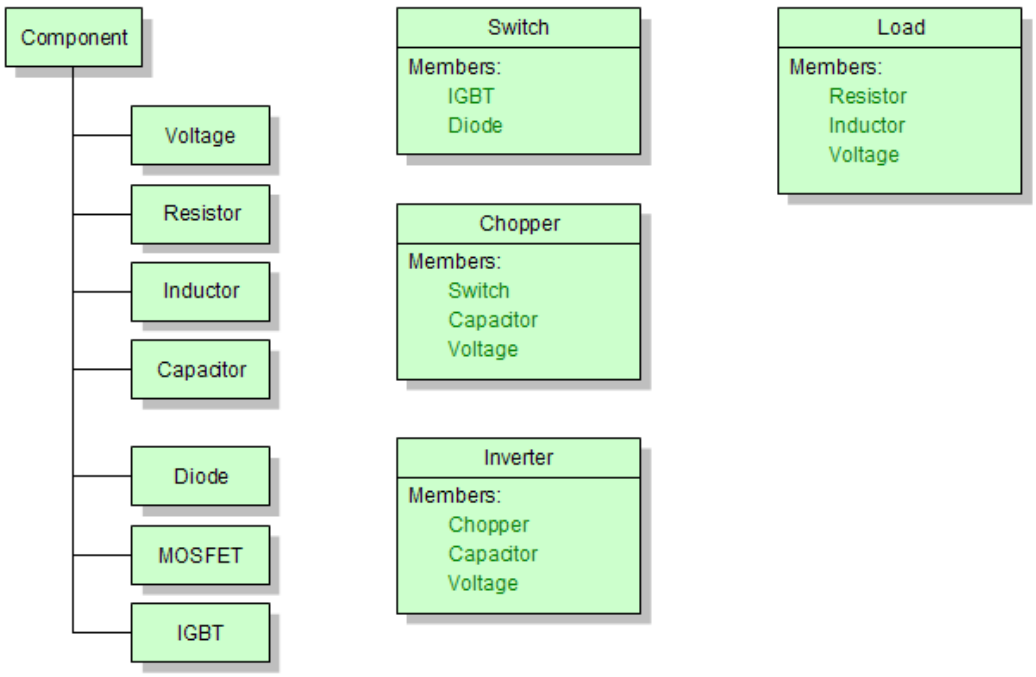


Figure 2.5.1: Class hierarchy and derived simulation classes

Taking these modelling concepts a stage further, nonlinear devices can be added by creating additional classes. In the case of electronic devices, and specifically power switching devices, the voltage characteristic when the device is conducting typically exhibits a nonlinear characteristic. For a simple class model, the device class could incorporate resistor and voltage classes as member variables. Alternatively, the V-I characteristic can be modelled using a look-up table of manufacturers published characteristics. This is the preferred method used in the simulator, and allows for the nonlinear behaviour with temperature to be included. Additionally, electronic device classes include methods for storing the energy absorbed in the device during a switching transition, and this can be done by either using tables of the manufacturer's published data where available or computing the curves using standard formulas for the turn-on or turn-off energy characteristics [2.57].

The complete power converter circuit is modelled as a combination of passive components and nonlinear solid-state switches. Each limb of the flying-capacitor inverter is instantiated using a Chopper class which contains the required number of inverter cells. The complete inverter class is then made up of three Chopper classes. The switching behaviour is controlled via time-stepping code which mimics the digital controller functionality. The different control modulator implementations have been modelled as C++ classes to mimic as closely as possible the likely implementation in a field programmable gate array (FPGA). Gate drive signals control the behaviour of the electronic switch models which in turn control the application of voltage to the load model. When the simulation is run, vectors of computed data are stored for visual display and post-processing.

A graphical user interface (GUI) has been developed using Microsoft Visual C++ development environment, which provides various controls and input data fields in order to improve the usability of the underlying simulator. A screen shot of the complete simulator is shown in Figure 2.5.2. As can be seen, the user interface dialog screen has various controls and edit boxes for selecting and setting the operating control parameters, inverter components and load characteristics. There is an oscilloscope style display for the load operating waveforms, a spectrum analyser display and a text box for displaying the key simulated operating conditions. The spectral components for the load voltage and current waveforms are found using a fast Fourier transform (FFT) written in C++ for the simulator.

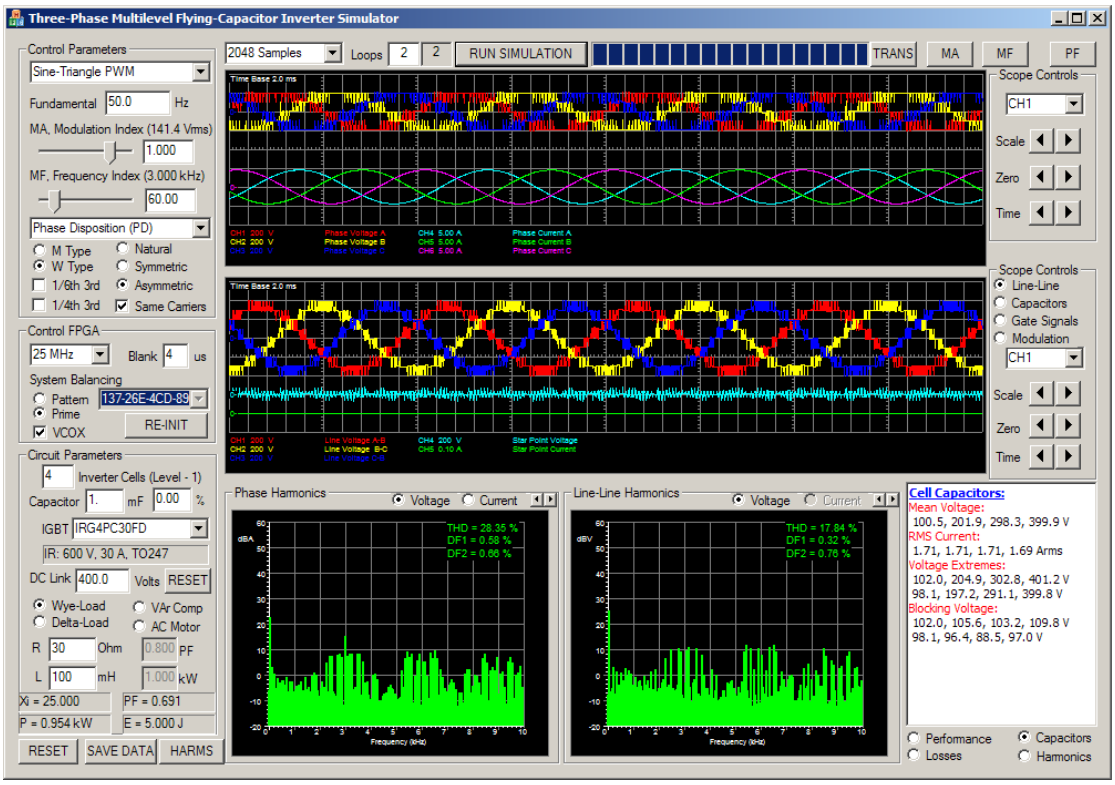


Figure 2.5.2: Simulator graphical user interface

2.5.2 Computation of Harmonic Distortion

The standard figure of merit regarding harmonic content in a waveform is the total harmonic distortion (THD) which expresses as a ratio the amount of unwanted harmonic content to the fundamental, V_1 [2.58]. The standard formula is

$$THD = \frac{100}{V_1}\sqrt{\sum_{n\neq 1} V_n^2} \quad \% \qquad \ldots (2.5.1)$$

A further two terms have been adopted in the literature specifically for quantifying PWM inverter output power quality [2.59, 2.60]. They are distortion factor 1 (DF1) and distortion factor 2 (DF2) and are computed from the following equations,

$$DF1 = \frac{100}{V_1}\sqrt{\sum_{n\neq 1}\left(\frac{V_n}{n}\right)^2} \quad \% \qquad \ldots (2.5.2)$$

$$DF2 = \frac{100}{V_1}\sqrt{\sum_{n\neq 1}\left(\frac{V_n}{n^2}\right)^2} \quad \% \qquad \ldots (2.5.3)$$

DF1 is applicable to ac motor drives which exhibit first order attenuation and it has also been referred to as the weighted THD (WTHD) [2.61]. The DF2 term is applicable to ac systems which have a second order L-C filter between the output of the inverter and the load.

The comparative assessment of sinusoidal modulation schemes is normally based on these THD and DF1 figures of merit and computed by the fast Fourier transform algorithm (FFT) from the voltage and current waveforms. Ideally the flying-capacitor inverter is operated with balanced cell-capacitor voltages at the ideal voltage levels with equal-spacing between the levels. In reality, without infinite capacitance, this will not be the case. There will be errors in the mean voltages and the voltages themselves will have ripple. This will inevitably lead to further harmonic distortion in inverter voltages.

It has been shown that the balancing of a multilevel inverter can lead to the generation of significant sub- and inter-harmonic frequency components at multiples of the fundamental divided by the number inverter cells per phase. It is already a known phenomenon in standard inverters and some researchers take this into account [2.62]. To ensure that these components are not ignored, the THD and DF1 equations need to be modified to take into account the number of levels in a multilevel inverter. The assumption is that any FFT algorithm is applied to data captured in a time window encompassing *m* multiples of the fundamental period, where *m* is the number of cells in the flying-capacitor inverter. The following equations are the modified forms of the classic distortion factors used in the literature.

$$THD = \frac{100}{V_1}\sqrt{\sum_{i=1}^{n} V_{i/m}^2 - V_1^2} \ \% \qquad \ldots (2.5.4)$$

$$DF1 = \frac{100}{V_1}\sqrt{\sum_{i=1}^{n} \frac{m^2 V_{i/m}^2}{i^2} - V_1^2} \ \% \qquad \ldots (2.5.5)$$

These issues are important in understanding harmonic distortion, especially in the case of multilevel inverters. The literature is full of comparisons based on these analytical expressions, and there is a danger that the true nature of harmonic distortion is overlooked. The real definition of THD is shown in equation (2.5.6), where it is a true measure of the unwanted harmonic component in the output power.

$$THD = \frac{100}{\tilde{V}_1}\sqrt{\tilde{V}_T^2 - \tilde{V}_1^2} \ \% \qquad \ldots (2.5.6)$$

where

$\tilde{V}_1$ is the fundamental rms voltage

$\tilde{V}_T$ is the total rms voltage

The simulator also computes the THD of the output voltage and current using the rms value and the fundamental amplitude from (2.5.6). The figures obtained, if computed from simulated data over a long time-frame, will include any multi-cycle repeating

very low frequency harmonic components which may be present due to the control scheme used.

2.5.3 Cell-Capacitor Requirement Indicator

The value and rating of the required cell-capacitors in the flying-capacitor inverter has the most important bearing on overall system size and cost. Firstly, the capacitors must be rated to handle the rms ripple current seen during normal operation. Secondly, the capacitance must be sufficiently high to ensure that the cell-voltages do not deviate too greatly from their balanced values, causing over-voltage conditions on the semiconductor switches.

The simulator provides current data for each capacitor which can be used for capacitor selection. Capacitor manufacturers provide lifetime figures for different ambient temperatures, operating frequencies and ripple currents, so that the inverter can be designed to meet the minimum required lifetime expectancy.

The minimum capacitance required is dependent on the cell-capacitor current amplitude as a function of time. The voltage variation is a function of the integral of current during a switching state and the net contribution due to the balancing control method used. Therefore, for a given synthesised fundamental frequency, higher capacitance is needed for lower inverter switching frequencies, with staircase SHE control being the worst case, To aid in characterising the inverter's performance at a specific synthesising frequency for different balancing and control schemes and load characteristics, it is helpful to use a system parameter which relates the unit cell-capacitor stored energy to the total load power of the three-phase inverter. It is especially instructive when analysing the characteristics of the inverter when operating under staircase SHE control.

The system parameter used throughout the analysis is termed the energy factor, ξ, and can be used for comparative analysis of different control schemes and operating parameters. The energy factor mathematical derivation is as follows:

The basic load real power is given by

$$P = \tilde{I}_a^2 R_a + \tilde{I}_b^2 R_b + \tilde{I}_c^2 R_c \qquad \ldots (2.5.7)$$

and assuming the load is balanced

$$P = 3\tilde{I}_{ph}^2 R \qquad \ldots (2.5.8)$$

The phase current rms $\tilde{I}_{ph}$ can be replaced with the phase voltage rms. $\tilde{V}_{ph}$. and power factor of the fundamental $\cos\phi$ to give

$$P = \frac{3\left(\tilde{V}_{ph}\cos\phi\right)^2}{R} \quad \ldots (2.5.9)$$

Now the phase voltage rms is a function of the dc link voltage, V_{dc} and amplitude modulation index, m_a, so (2.5.9) can be rearranged to give

$$P = \frac{3}{R}\left(\frac{m_a V_{dc}}{2\sqrt{2}}\cos\phi\right)^2 \quad \ldots (2.5.10)$$

In an N-cell inverter, the unit cell-capacitor voltage is

$$V_c = \frac{V_{dc}}{N} \quad \ldots (2.5.11)$$

so rearranging (2.5.10) gives

$$P = \frac{3}{R}\left(\frac{m_a N V_c}{2\sqrt{2}}\cos\phi\right)^2 \quad \ldots (2.5.12)$$

Equation (2.5.12) can be rearranged to separate the unit cell-capacitor energy to give

$$P = 3\left(\frac{\left(m_a N\cos\phi\right)^2}{4RC}\right)\left(\frac{1}{2}CV_c^2\right) \quad \ldots (2.5.13)$$

and where the unit cell-capacitor stored energy, E_c, is given by

$$E_c = \frac{1}{2}CV_c^2 \quad \ldots (2.5.14)$$

Simplifying results in the following relationship

$$P = \xi N^2 m_a^2 \cos^2\phi E_c \quad \ldots (2.5.15)$$

where

$$\xi = \frac{3}{4RC}\ \text{s}^{-1} \quad \ldots (2.5.16)$$

In a practical system, the designer would aim to minimise the capacitor size which can lead to increased voltage ripple on the capacitors. So the parameter, ξ, needs to be as large as realistically possible, while maintaining safe operation of the inverter by minimising the peak switch blocking voltages and peak capacitor voltages. The ripple voltage will also be dependent on the amount of current flowing when the capacitors are in the load current path. Therefore, the current lag angle, ϕ, is also an instructive parameter when quantifying the inverter performance with the system design parameters. It is simply related to the load parameters thus,

$$\phi = \tan^{-1}\left(\frac{\omega L}{R}\right) \quad \ldots (2.5.17)$$

The term, $cos\phi$, is the power factor for an ideal sinusoidal system. It is usually referred to as displacement factor (DPF) to differentiate it from the true power factor (TPF), which is defined as the ratio of real power to apparent power. The displacement power factor of the load is the preferred parameter for analysis of the system and is used throughout the simulations to allow inverter performance comparisons, independent of the power rating and input voltage of the system.

2.5.4 Generic Load Model

The cell-capacitor voltage variation depends on the amplitude and polarity of the load current at intermediary output voltage levels when the capacitor is in circuit. Therefore, the position of the peak of the ideal sinusoidal current with respect to these intermediary voltage levels will affect performance. The angle, ϕ, between the phase current with the phase voltage is dependent on the load characteristics. Therefore, the displacement power factor term, $cos\phi$, is important in quantifying the load characteristic and for comparing the performance of different modulation strategies in the flying-capacitor circuit.

In the case of inductive loads, where the current lags the voltage, the inductance and resistance also dictate the effective filtering of the voltage harmonics seen in the phase current. Rather than limiting load modelling as a simple RL, a more generic approach is adopted by the addition of an idealised e.m.f. sinusoidal voltage term. This gives a good approximation to a load applicable to most ac systems, and has been adopted by other researchers in the past [2.63]. More complex load models could have been adopted, but since of the investigation is focussed specifically on the inverter and the cell-capacitor voltages, and the current distortion is relatively low, then this generic load model is appropriate. Figure 2.5.3 shows the circuit of a star-connected generic load used in the simulator.

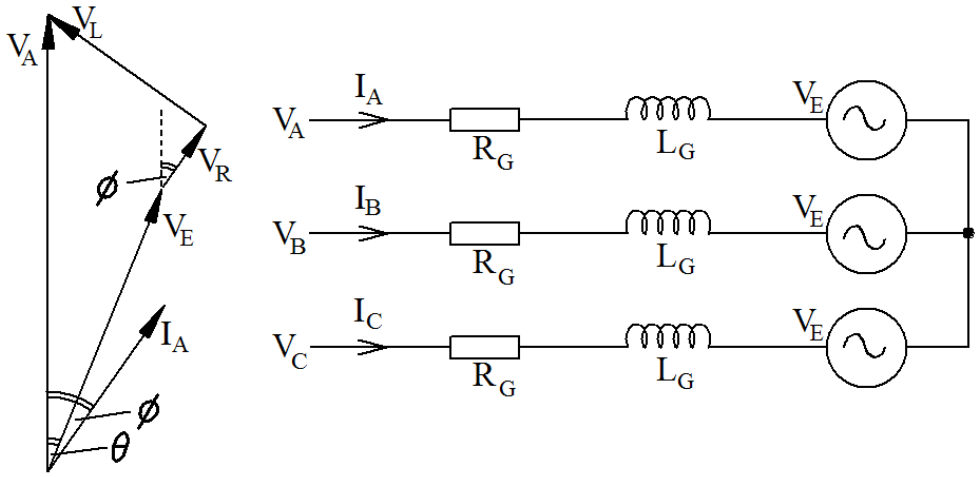


Figure 2.5.3: Generic load model circuit and voltage phasor diagram

The voltage relationships between the load and the phase voltage are given by

$$V_E \sin\theta = V_L \cos\phi - V_R \sin\phi \qquad \ldots (2.5.18)$$

$$V_E \cos\theta = V_A - V_L \sin\phi - V_R \cos\phi \qquad \ldots (2.5.19)$$

where

V_L and V_R are the voltages across R_G and L_G respectively.

There is only one unique solution of R_G and L_G value at the given fundamental frequency for the case when the e.m.f. term is zero and these are R and L in the RL load case. When the back e.m.f. is finite, then there is a range of values of R_G, L_G, V_E and θ which can be used to match the lag angle in the current and output load power. Therefore, when modelling the load system, the resistance, inductance, real power P and displacement power factor $\cos\phi$ are specified. For instance, if the load aims to model an induction motor, then the R_G parameter is the stator winding resistance and the L_G parameter is the leakage inductance. The simulator then computes the required e.m.f. term amplitude V_E and phase shift θ in the following manner.

$$I_{ph} = \frac{P}{3V_{ph}\cos\phi} \qquad \ldots (2.5.20)$$

$$V_R = I_{ph} R_G \qquad \ldots (2.5.21)$$

$$V_L = 2\pi f L_G I_{ph} \qquad \ldots (2.5.22)$$

$$\theta = \tan^{-1}\left(\frac{V_L \cos\phi - V_R \sin\phi}{V_A - V_L \sin\phi - V_R \cos\phi}\right) \qquad \ldots (2.5.23)$$

$$V_E = \frac{V_L \cos\phi - V_R \sin\phi}{\sin\theta} \qquad \ldots (2.5.24)$$

It has already been seen that significant voltage ripple on the flying-capacitor inverter capacitors will lead to significant low order harmonic content in the output phase voltage. Therefore, the resultant current THD will be more representative when using a non-zero e.m.f. parameter in the load model, compared with the basic RL case.

Finally, the equivalent energy factor, ξ, cannot be calculated directly using (2.5.16) as in the simple RL load case. For generic load simulation where the desired output power, P, and the DPF, $cos\phi$, are set, then ξ can be calculated using the following derivation

$$P = \frac{3\left(\tilde{V}_{ph}\cos\phi\right)^2}{R} \qquad \ldots (2.5.25)$$

where

R is the equivalent resistance for an RL load

The phase voltage rms in terms of the dc link voltage and amplitude modulation index is given by

$$\tilde{V}_{ph} = \frac{m_a V_{dc}}{2\sqrt{2}} \qquad \ldots (2.5.26)$$

so rearranging (2.5.25) to obtain a relationship for R gives

$$R = \frac{3\left(m_a V_{dc}\cos\phi\right)^2}{8P} \qquad \ldots (2.5.27)$$

This can now be used in conjunction with the original energy factor equation (2.5.16) to give a modified equation for computing ξ in the simulator,

$$\xi = \frac{2P}{CV_{dc}^2 m_a^2 \cos^2\phi} \qquad \ldots (2.5.28)$$

2.6 Conclusions

The flying-capacitor inverter is an interesting member of the multilevel inverter family, but it has been the least popular for development in new application, and has had fewer research studies dedicated to its operation. This is primarily due to the number of required cell-capacitors which are crucial to its operation and impact significantly on the inverter's size, cost and performance. It is clear, therefore, that optimising the control must focus on reducing capacitor rating while achieving the lowest possible harmonic distortion in the load waveform without compromising safe-operation and the life-time of the power electronic switches.

It has been shown that the increasing level of complexity in terms of the number of operating states, especially as more inverter cells are added, provides a great challenge on the analysis and design of the control system. Nevertheless, as has been shown, the system balancing requirements can be met by correct switching state rotation.

There are many multilevel control schemes which can be applied to a three-phase flying-capacitor inverter, and they all offer different merits in terms of output harmonic signature and operating switching frequencies in the ideal case. When practical sized capacitors are used in the system, then the influence of voltage ripple needs a more detailed examination when operating with the different control schemes.

It has been shown that some operating information can be obtained using basic circuit analysis and modelling techniques. However, the need for rapid and more detailed modelling of the inverter system justified the development of a bespoke simulator package, which will aid the investigation of control approaches, and the effect of capacitor voltage ripple on performance.

2.7 References

[2.1] Meynard, T.A. and Foch, H., "Dipositif électronique de conversion d'énergie électrique", French Patent No. 2679715B1, Filed 25th July 1991, Issued 29th January 1993. (WO93/02501A1, “Electronic device for converting electrical energy”).

[2.2] Meynard, T.A. and Foch, H., “Multi-level choppers for high voltage applications”, EPE Journal, Vol. 2, No. 1, March 1992, pp. 45 – 50.

[2.3] Hamma, F., Meynard, T.A., Tourkhani, F. and Viarouge, P., “Characteristics and design of multilevel choppers”, PESC '95 Record, the 26th Annual IEEE Power Electronics Specialists Conference, 18 - 22 June, 1995, Vol. 2, pp. 1208 – 1214.

[2.4] Meynard, T.A., Foch, H., Thomas, P., Courault, J., Jakob, R. and Nahrstaedt, “Multicell converters: basic concepts and industry applications”, IEEE Transactions on Industrial Electronics, Vol. 49, No. 5, October 2002, pp. 955 – 964.

[2.5] Meynard, T.A. and Foch, H., “Multi-level conversion: high voltage choppers and voltage-source inverters”, PESC '92 Record, 23rd Annual IEEE Power Electronics Specialists Conference, 29 June - 3 July, 1992, Vol. 1, pp. 397 – 403.

[2.6] Meynard, T.A. and Foch, H., “Imbricated cells multi-level voltage-source inverters for high voltage applications”, EPE Journal, Vol. 3, No. 2, June, 1993, pp. 99 – 106.

[2.7] Carrère, P., Meynard, T.A. and Lavieville, J.P., “4000V-300A eight-level IGBT inverter leg”, Proceedings of EPE '95, the 6th European Conference on Power Electronics and Applications, 19 – 21 September, 1995, Vol. 1, pp. 106 - 111.

[2.8] Hamma, F., Meynard, T.A., Tourkhani, F. and Viarouge, P., “Characteristics and design of multilevel choppers”, PESC '95 Record. 26th Annual IEEE Power Electronics Specialists Conference, 18 - 22 June, 1995, Vol. 2, pp. 1208 – 1214.

[2.9] Gateau, G., Maussion, P. and Meynard, T.A.,“Fuzzy phase control of series multicell converters”, Proceedings of the 6th IEEE International Conference on Fuzzy Systems, 1 - 5 July, 1997, Vol. 3, pp. 1627 – 1633.

[2.10] Meynard, T.A. , Fadel, M. and Aouda, N., “Modeling of multilevel converters”, IEEE Transactions on Industrial Electronics, Vol. 44, No. 3, June, 1997, pp. 356 – 364.

[2.11] Gateau, G., Fadel, M., Maussion, P., Bensaid, R. and Meynard, T.A., “Multicell converters: active control and observation of flying-capacitor voltages”, IEEE Transactions on Industrial Electronics, Vol. 49, No. 5, October 2002, pp. 998 – 1008.

[2.12] Pinon, D., Fadel, M. and Meynard, T.A., “Sliding mode controls for a two-cell chopper”, Proceedings of EPE '99, 8th European Conference on Power Electronics and Applications, 7 - 9 September, 1999, CDROM Paper No. 653.

[2.13] Gateau, G., Meynard, T.A. and Foch, H., “Stacked multicell converter (SMC): topology and control”, Proceedings of EPE '01, 9th European Conference on Power Electronics and Applications, 27 - 29 August, 2001, CDROM Paper No. PP00233.

[2.14] Turpin, C., Deprez, L., Forest, F., Richardeau, F. and Meynard, T.A., “A new ZVS imbricated cell multilevel inverter with auxiliary resonant commutated poles”, Proceedings of PESC 2001, the 32nd Annual IEEE Power Electronics Specialists Conference, 2001, Vol. 2, pp. 1159 – 1164.

[2.15] Richardeau, F., Baudesson, Ph. and Meynard, T.A., “Failures-tolerance and remedial strategies of a PWM multicell inverter”, Proceedings of PESC

2000, IEEE 31st Annual Power Electronics Specialists Conference, 18 - 23 June, 2000, Vol. 2, pp. 649 - 654.

[2.16] Turpin, C., Baudesson, P., Richardeau, F., Forest, F. and Meynard, T.A., "Fault management of multicell converters", IEEE Transactions on Industrial Electronics, Vol. 49, No. 5, October 2002, pp. 988– 997.

[2.17] Martins, C.A., Roboam, X., Meynard, T.A. and Carvalho, A.S., "Multi-level direct torque control with imposed switching frequency and reduced ripple", Proceedings of PESC '00, IEEE 31st Annual Power Electronics Specialists Conference, 18 - 23 June, 2000, Vol. 1, pp. 435 - 441.

[2.18] Loudot, S., Pouliquen, H., Meynard, T. and Chéron, Y., "Active current filter for MV/HV networks", Proceedings of EPE '95, the 6th European Conference on Power Electronics and Applications, 19 – 21 September, 1995, Vol. 1, pp. 129 – 134**.**

[2.19] Tourkhani, F., Viarouge, P. and Meynard, T.A., "Optimal design and experimental results of a multilevel inverter for an UPS application", Proceedings of PEDS '97, 2nd International Conference on Power Electronics and Drive Systems, 26 - 29 May, 1997, Vol. 1, pp. 340 – 343.

[2.20] Wilkinson, R.H., Mouton, H. du T. and Meynard, T.A., "Natural balance of multicell converters", Proceedings of PESC 2003, 31st IEEE Power Electronics Specialists Conference, Acapulco, Mexico, 15 – 19 June, 2003, Vol. 2, pp. 1307 – 1312.

[2.21] Wilkinson, R.H., Horn, A. and Enslin, J.H.R., "Control options for a bi-directional multilevel traction chopper", PESC '96 Record. 27th Annual IEEE Power Electronics Specialists Conference, 23 - 27 June, 1996, pp. 1395 – 1400.

[2.22] Donzel, A., and Bornard, G., "New control law for capacitor voltage balance in multilevel inverter with switching rate control (CVC)", Conference Record of IAS 2000, the 2000 IEEE Industry Applications Society 35th Annual Meeting, October 2000, Vol. 3, pp. 2037 – 2044.

[2.23] Thomas, J.-L., Poullain, S., Donzel, A. and Bornard, G., "Advanced torque control of induction motors fed by a floating capacitor multilevel VSI actuator", IEE Seminar, 'Advances in Induction Motor Control', 23 May, 2000, pp. 5/1 - 5/5.

[2.24] Duarte, J.L., Jullicher, P.J.M., Offringa, L.J.J. and van Groningen, W.D.H, "Stability analysis of multilevel converters with imbricated cells",

Proceedings of EPE '97, 7th European Conference on Power Electronics and Applications, 8 - 10 September, 1997, Vol. 4, pp. 168 – 174.

[2.25] Dijhuizen, F.R. and Duarte, J.L., "Proper choice of flying capacitors based on distinct power dissipation models", Conference Record of IAS '98, the 1998 IEEE Industry Applications Society 33rd Annual Meeting, 12 - 15 October, 1998, Vol. 2, pp. 1174 – 1180.

[2.26] Lee, S.-G, Kang, D.-W., Lee, Y.-H. and Hyun, D.-S., "The carrier-based PWM method for voltage balance of flying capacitor multilevel inverter", Proceedings of EPE '01, 9th European Conference on Power Electronics and Applications, 27 - 29 August, 2001, CDROM Paper No. PP00583.

[2.27] Kang, D.-W., Lee, W.-K. and Hyun, D.-S., Carrier-rotation strategy for voltage balancing in flying capacitor multilevel inverter, IEE Proceedings - Electric Power Applications, Vol. 151, No. 2, March, 2004, pp. 239 - 248.

[2.28] Wang, H.-Y., Deng, Y. and He, X.-N., "Novel carrier-based PWM method with voltage balance for flying capacitor multilevel inverters", Proceedings of PESC '04, 35th Annual Power Electronics Specialists Conference, 20 - 25 June, 2004, Vol. 6, pp. 4423 – 4427.

[2.29] Lu, M., Deng, Y., Zhao, R.-X. and He, X.-N., "Relationship between flying capacitor multilevel inverter PWM methods and switching loss minimized PWM method for flying capacitor multilevel inverter", Proceedings of PESC '04, 35th Annual Power Electronics Specialists Conference, 20 - 25 June, 2004, Vol. 6, pp. 4418 – 4422.

[2.30] Xu, L. and Agelidis, V.G., "Active capacitor voltage control of flying capacitor multilevel converters", IEE Proceedings-Electric Power Applications, Vol. 151, No. 3, May, 2004, pp. 313 – 320.

[2.31] Xu, L. and Agelidis, V.G., "A flying capacitor multilevel PWM converter based UPFC", Proceedings of PESC 2001, IEEE 32nd Annual Power Electronics Specialists Conference, 17 - 21 June, 2001, Vol. 5, pp. 1905 – 1910.

[2.32] Liu, W.-H., Yan, G.-G., Chen, Y.-H., Zhang, X.-C. and Han, Y.-D., "A generic PWM control method for flying capacitor inverter", Proceedings of APEC '04, 19th Annual IEEE Applied Power Electronics Conference and Exposition, 22 - 26 February, 2004, Vol. 3, pp. 1686 – 1690.

[2.33] Mendes, M.A.S., Peixoto, Z.M.A., Seixas, P.F. and Donoso-Garcia, P., "A space vector PWM method for three-level flying-capacitor inverters",

Proceedings of PESC 2001, IEEE 32nd Annual Power Electronics Specialists Conference, 17 - 21 June, 2001, Vol. 1, pp. 182 – 187.

[2.34] Zare, F. and Ledwich, G.,"A hysteresis current control for single-phase multilevel voltage source inverters: PLD implementation", IEEE Transactions on Power Electronics, Vol. 17, No. 5, September, 2002, pp. 731 – 738.

[2.35] Yuan, X. and Barbi, I., "Zero-voltage switching for three level capacitor clamping inverter", IEEE Transactions on Power Electronics, Vol. 14, No. 4, July 1999, pp. 771 – 781.

[2.36] Yuan, X., Stemmler, H. and Barbi, I., "Self-balancing of the clamping-capacitor-voltages in the multilevel capacitor-clamping-inverter under sub-harmonic PWM modulation", IEEE Transactions on Power Electronics, Vol. 16, No. 2, March 2001, pp. 256 – 263.

[2.37] Song, B.-M., "Voltage balancing technique for flying capacitors used in soft switching multilevel active power filter" PhD Thesis, Virginia Polytechnic Institute and State University, Blacksburg, VI, USA, July 2001.

[2.38] Kou, X.-M., Corzine, K.A. and Familiant, Y.L., "A unique fault-tolerant design for flying capacitor multilevel inverter", IEEE Transactions on Power Electronics, Vol. 19, No. 4, July, 2004, pp. 979 – 987.

[2.39] Escalante, M.F. and Vannier, J.-C., "Direct approach for balancing the capacitor voltages of a 5-level flying capacitor converter", Proceedings of EPE '99, 8th European Conference on Power Electronics and Applications, 7 - 9 September, 1999, CDROM Paper No. 776.

[2.40] Saudemont, C., Cambronne, J.P. and Rombaut, C., "Capacitor voltages in the imbricated cell topology: generalisation of the variation rules", Proceedings of EPE '99, 8th European Conference on Power Electronics and Applications, 7 - 9 September, 1999, CDROM Paper No. 270.

[2.41] Lin, B.-R. and Hou, Y.-L., "High-power-factor single-phase capacitor clamped rectifier", IEE Proceedings-Electric Power Applications, Vol. 148, No. 2, March, 2001, pp. 214 – 224.

[2.42] Lin, B.-R., Hung, T.-L. and Huang, C.-H., "Bi-directional single-phase half-bridge rectifier for power quality compensation", IEE Proceedings-Electric Power Applications, Vol. 150, No. 4, July, 2003, pp. 397 – 406.

[2.43] Liang, Y. and Nwankpa, C.O., "A power line conditioner based on flying capacitor multilevel voltage source converter with phase shift SPWM",

Conference Record of IAS '99, the 1999 IEEE Industry Applications Society 34th Annual Meeting, 3 - 7 October, 1999, Vol. 4, pp. 2337 – 2343.

[2.44] Beinhold, G., Jakob, R. and Nahrstaedt, M., "A new range of medium voltage multilevel inverter drives with floating capacitor technology", Proceedings of EPE '01, 9th European Conference on Power Electronics and Applications, 27 - 29 August, 2001, CDROM Paper No. PP00426.

[2.45] Keller, C., Jakob, R. and Salama, S., "Topology and balance control of medium voltage multilevel drives", Proceedings of EPE '01, 9th European Conference on Power Electronics and Applications, 27 - 29 August, 2001, CDROM Paper No. PP00430.

[2.46] Lavieville, J.-P., Bethoux, O., Carrere, P. and Meynard, T., "Electronic device for electric energy conversion", Patent No. EP0720281B1, Priority French Filing 29th December, 1994, Granted 17th June, 1998.

[2.47] Lindberg, J., Svensson, K., Bijlenga, B., Jonsson, T. and Stergiopoulos, F., "A converter device and a method for the control thereof", PCT Patent No. WO01/89071A1, Filed 16th May, 2000, Published 22nd November, 2001.

[2.48] Shi, Y., Yang, X., He, Q. and Wang, Z.-A., "Research on a novel multilevel matrix converter", Proceedings of PESC '04, 35th Annual Power Electronics Specialists Conference, 20 - 25 June, 2004, Vol. 3, pp. 2413 – 2419.

[2.49] Watkins, S.J., Čorda, J. and Zhang, L., "Multilevel asymmetric power converters for switched reluctance machines", Proceedings of PEMD '02, the 1st International Conference on Power Electronics Machines and Drives, IEE Conference Publication No. 487, 16 - 18 April, 2002, pp 195 - 200.

[2.50] Thorborg, K., "Power electronics", S.T. Teknik, Göteborg, Sweden, 2nd Edtion, 1985, Appendix B.

[2.51] Seeley, S., "Laplace Transform", Chapter 5, The Transforms and Applications Handbook - Second Edition , CRC Press, 2002.

[2.52] Watkins, S.J. and Zhang, L., "Modelling and control of flying-capacitor inverters", EPE 2001, the 9th European Power Electronics and Applications Conference, Graz, Austria, 27 –29 August, 2001, CDROM Paper No. PP00439.

[2.53] Bowes, S.R. and Clare, J.C., "Computer-aided design of PWM power-electronic variable-speed drives", IEE Proceedings, Vol. 135, Part B, No. 5, September 1988, pp. 240 – 260.

[2.54] Gateau, G., Ruelland, R. and Aime, M., "A co-simulation environment for the test and the validation of digital control strategy on a mixed DSP/FPGA architecture", Proceedings of EPE-PEMC 2004, 11th International Power Electronics and Motion Control Conference, 2 - 4 September, 2004, CDROM Paper No. A32616.

[2.55] Stroupstrop, B., "The C++ programming language", Addison Wesley, ISBN: 0201539926, 1986.

[2.56] Wolf, W.H., "How to build a hardware description and measurement system on an object-oriented programming language", IEEE Transactions on Computer-Aided Design, Vol. 8, No. 3, March 1989, pp. 288 – 301.

[2.57] Erickson, R.W., "Fundamentals of power electronics", Chapman and Hall, New York, USA, May 1997, ISBN 0-412-08541-0. Section 4.3, "Switching loss".

[2.58] IEEE 519-1992, "IEEE recommended practices and requirements for harmonic control in electrical power systems". IEEE Inc., USA, 12 April 1993.

[2.59] Fukuda, S. and Suzuki, K, "Using harmonic determination factor for harmonic evaluation of carrier-based PWM methods", Conference Record of IAS '97, IEEE Industry Applications Society 32nd Annual Meeting, 5 - 9 October, 1997, pp. 1541 – 1541.

[2.60] Agelidis, V.G. and Calais, M., "Application specific harmonic performance evaluation of multicarrier PWM techniques", PESC '98 Record, 29th Annual IEEE Power Electronics Specialists Conference, 17 - 22 May, 1998, Vol. 1, pp. 172 – 178.

[2.61] Holmes, D.G. and Lipo, T.A., "Pulse width modulation for power converters. Principles and practice", Wiley-IEEE Press Series on Power Engineering, 2003, ISBN 0-471-20814-0.

[2.62] Schultz, D., Kompa, T., Hanitsch, R. and Saniter, C., "Investigations of power quality of 1.5 MW wind energy generators", Proceedings of ISES 2001, Solar Wind Congress, 25 November – 2 December, 2001.

[2.63] Preston, T.W., Reece, A.B.J. and Sangha, P.S., "Induction motor analysis by time-stepping techniques", IEEE Transactions on Magnetics, Vol. 24, No. 1, January, 1988, pp. 471 – 474.

Chapter 3 SELECTIVE HARMONIC ELIMINATION

3.1 Introduction

The selective harmonic elimination (SHE) control technique was one of the earliest forms of control applied to optimise voltage-source inverter performance. The control scheme offers low harmonic distortion whilst regulating the amplitude of the desired fundamental frequency component. The switching frequency can be very low and so the older thyristor-based inverters' performance was not limited by the power device switching speed [3.1 - 3.3]. SHE control is now less popular because of advances in power semiconductor technology making higher frequency PWM more attractive, but for very high power systems the control scheme still offers advantages.

In the case of multilevel inverters, the extra voltage levels available offer additional degrees of freedom in minimising total harmonic distortion by pre-computation of the timing of the switching pattern. The earliest proposed multilevel neutral point clamped inverter [3.4] was controlled using the SHE technique. In its basic form, it achieves the lowest number of switching transitions in the inverter giving a staircase-shaped output phase voltage.

This chapter presents the results of an investigation by simulation on a SHE-controlled flying-capacitor inverter. The focus is on the effect of cell-capacitor voltage ripple on overall performance and the voltage balancing approach which minimises harmonic distortion and capacitor size. This form of control, however, is not suitable for low cycle frequency operation, since the required inverter capacitors would be impractically large. Therefore, the analysis has focussed on a fixed operating frequency. This is 50 Hz in the case of a European grid-connected inverter.

The simulator developed specifically for this research study will be used to illustrate the behaviour of the flying-capacitor inverter under steady–state and transient conditions. The simulator's ability to model the behaviour of a real digital logic implementation will also aid the development of laboratory hardware for experimental verification of the theoretical analysis. Simulator output includes time- and frequency-domain data files which are post-processed using MATLAB, mainly for graphical representation, to highlight the main conclusions of this work.

The inverter circuit to be investigated by simulation (and later experimentally) is a four-cell inverter. The circuit diagram of the main power components is shown in Figure 3.1.1. The inverter can synthesise five voltage levels at each phase terminal

with respect to the dc link neutral point, so providing a load line to line voltage with up to nine distinct voltage levels. The inverter model is based around a single unit cell-capacitor rating, and so four capacitors are in parallel across the dc link. The dc link capacitors are fed by an ideal voltage source which prevents the capacitor voltage dropping when current flows from the supply, but their voltages are allowed to increase when any energy is returned as indicated by the blocking diode. The emphasis of the work is on the control of the inverter itself, in particular optimisation of the inverter parameters to improve the output power quality, as measured by the THD of the line voltage and phase current. The simulations were performed on a simple RL load, with a zero back e.m.f.

The simulation work progresses logically by analysing control and parameter effects individually so that a clear picture as to an optimum control strategy can be assessed. The control scheme is first benchmarked under ideal conditions. The interaction between the cell-capacitance and the load parameters is analysed in detail, and an attempt is made at quantifying the behaviour in a normalised fashion. Here the concept of an open-loop sensorless pattern-based balancing strategy to maintain all voltages in the inverter within safe operating bands is introduced. This analysis is used to aid the design of a practical inverter based on real power switches and practical sized capacitors. The performance is then assessed over the whole operating range and the contribution of power switch loss to operation quantified. Finally, the inverter's behaviour is investigated under a number of different transient conditions; namely dc link extreme events, stepped load variation and stepped output voltage demand.

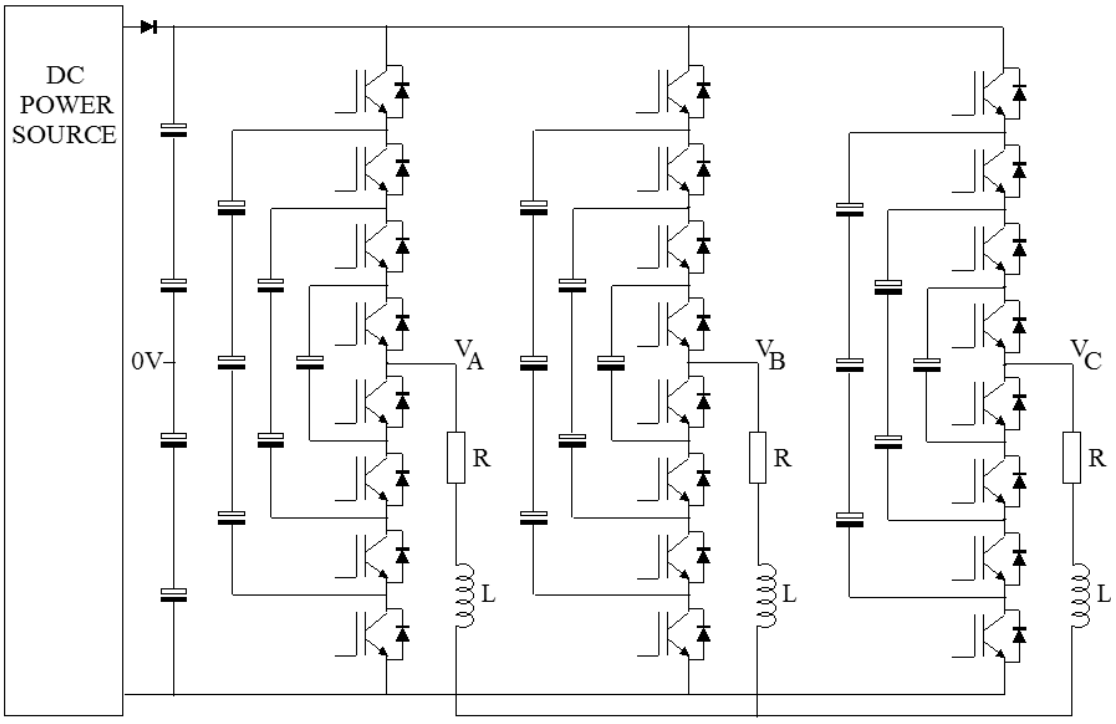


Figure 3.1.1: Five-level flying-capacitor inverter circuit used for simulation

3.2 Optimal SHE Control

The selective harmonic elimination angle commutation (SHE) control is used to eliminate one or more harmonics and regulating the fundamental amplitude. The angles are pre-computed using the Newton-Raphson method to solve the roots of the set of non-linear equations for the odd harmonics components. The number of angles is equal to the number of controlled frequency components. Typically in a real system the angles would also be pre-stored in memory look-up table rather than computed real-time every cycle as this provides the most efficient implementation.

In its simplest form, where the resultant waveform has the shape of a staircase shown in Figure 3.2.1, the number of controlled components is equal to half the number of cells in the inverter due to the requirement for symmetry around the mean level. With basic SHE control, the four-cell, five-level inverter under investigation can only be controlled with the fundamental regulated and one harmonic eliminated. The following equations must be solved using the Newton-Raphson method to obtain the required control angles

$$\cos(\alpha_1) + \cos(\alpha_2) = \frac{\pi m_a}{2} \qquad \ldots (3.2.1)$$

$$\cos(5\alpha_1) + \cos(5\alpha_2) = 0 \qquad \ldots (3.2.2)$$

where

α_1 and α_2 are the angles at which a level transition occurs.

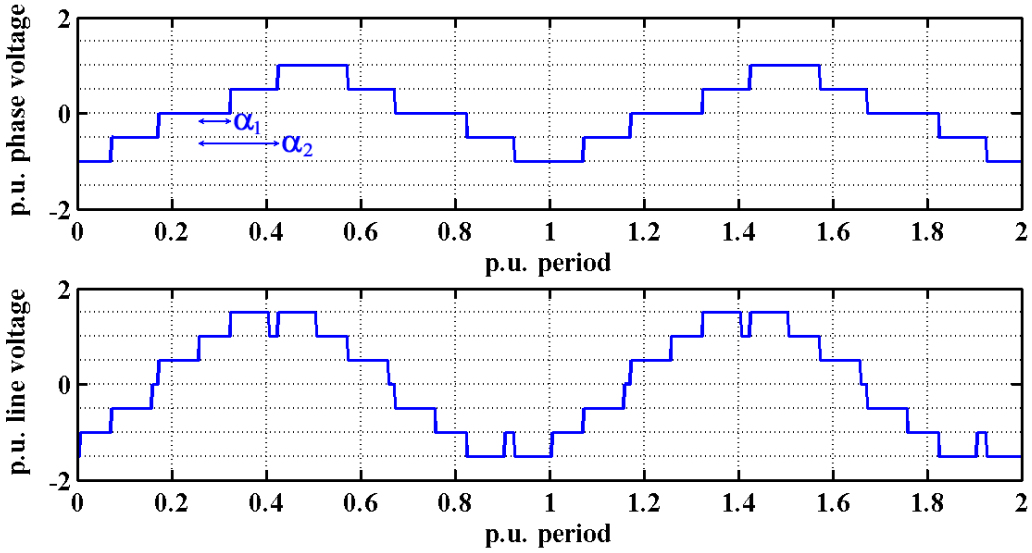


Figure 3.2.1: Two angle SHE control ideal inverter voltages, m_a = 0.85

The SHE method can be extended in multilevel inverters [3.5] by introducing two symmetric step-down pulses within the staircase waveforms and eliminating two additional harmonics, as shown in Figure 3.2.2. The optimum angles, α_1 through α_4, are again computed using the Newton-Raphson method but where the α_3 cosine terms are negative. The MATLAB script for finding these four angles can be found in Appendix A. The four simultaneous equations that have to be solved are

$$\cos(\alpha_1)+\cos(\alpha_2)-\cos(\alpha_3)+\cos(\alpha_4)=\frac{\pi m_a}{2} \quad \ldots (3.2.3)$$

$$\cos(5\alpha_1)+\cos(5\alpha_2)-\cos(5\alpha_3)+\cos(5\alpha_4)=0 \quad \ldots (3.2.4)$$

$$\cos(7\alpha_1)+\cos(7\alpha_2)-\cos(7\alpha_3)+\cos(7\alpha_4)=0 \quad \ldots (3.2.5)$$

$$\cos(11\alpha_1)+\cos(11\alpha_2)-\cos(11\alpha_3)+\cos(11\alpha_4)=0 \quad \ldots (3.2.6)$$

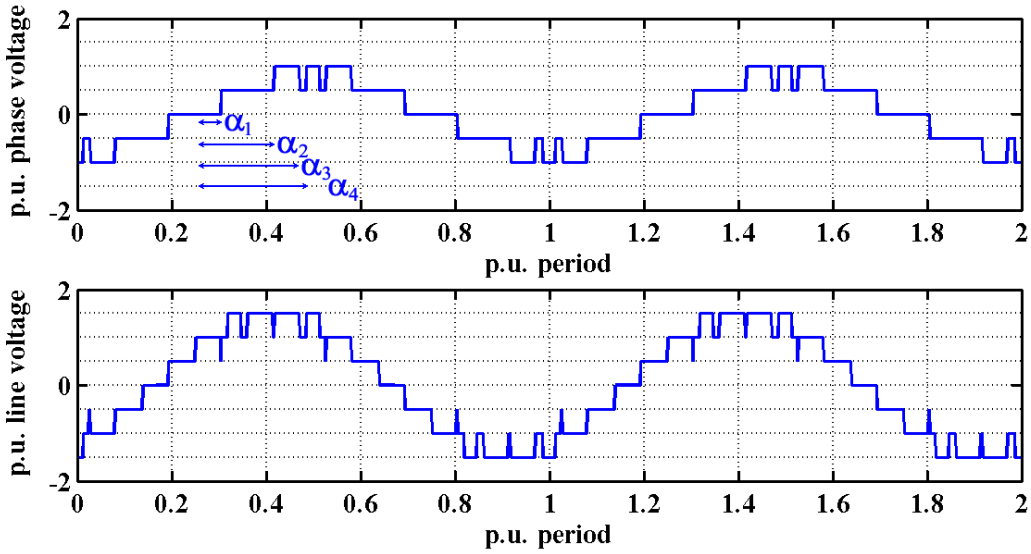


Figure 3.2.2: Four angle SHE control ideal inverter voltages, m_a = 0.85

This method can be extended to higher orders of harmonic elimination, but obtaining a solution can be extremely difficult and other approaches have been suggested. Enjeti and Lindsay [3.6] used linear approximations to the angle solutions to improve algorithm convergence, while the Chiasson, Tolbert et al. [3.7] have applied the theory of resultants to find solutions from an equivalent set of polynomial equations representing the original simultaneous equations. Most recently, Agelidis et al. [3.8] applied a minimisation technique in combination with a randomised search in order to reduce the computation time.

The amount of pre-computational effort and increased memory storage requirements for a higher order SHE scheme are disadvantages and only offer slight improvement

over a PWM implementation in a real-time control scheme. Therefore, only two SHE schemes will be used in the simulation and analysis of the flying-capacitor inverter.

The simulator is used to confirm the validity of the pre-computed angles for the two SHE methods; hereon referred to as SHE-4H2 and SHE-4H4 to indicate inverter cell number and number of frequency components controlled. In each case, the lowest possible harmonic is limited, excluding the triplen harmonics which will be cancelled in the three-phase load. Therefore SHE-4H2 eliminates the 5^{th}, and SHE-4H4 eliminates the 5^{th}, 7^{th} and 11^{th}. This should give the lowest harmonic distortion in the current waveform due to the first-order filtering characteristic of an inductive load.

To validate and compare simulation and computation of SHE angles, the normalised voltage harmonic spectra for the two control schemes are shown in Figure 3.2.3 and Figure 3.2.4. These are the spectral signatures of the voltage waveforms shown in the previous figures, with a m_a = 0.85, and computed using an inbuilt FFT algorithm to obtain the frequency harmonics. They illustrate the desired elimination of low order harmonics.

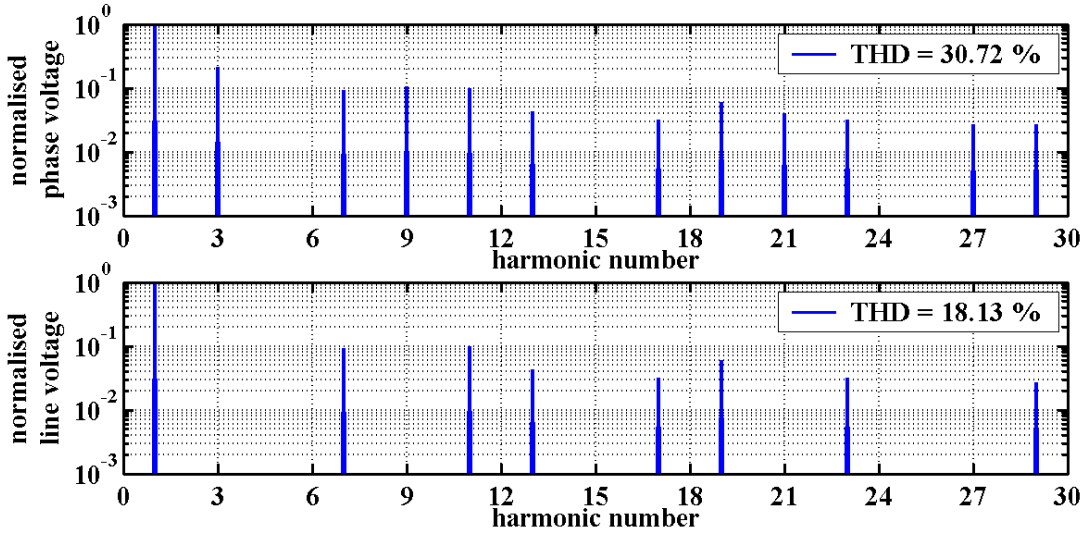


Figure 3.2.3: Ideal voltage spectra for SHE-4H2, and m_a = 0.85

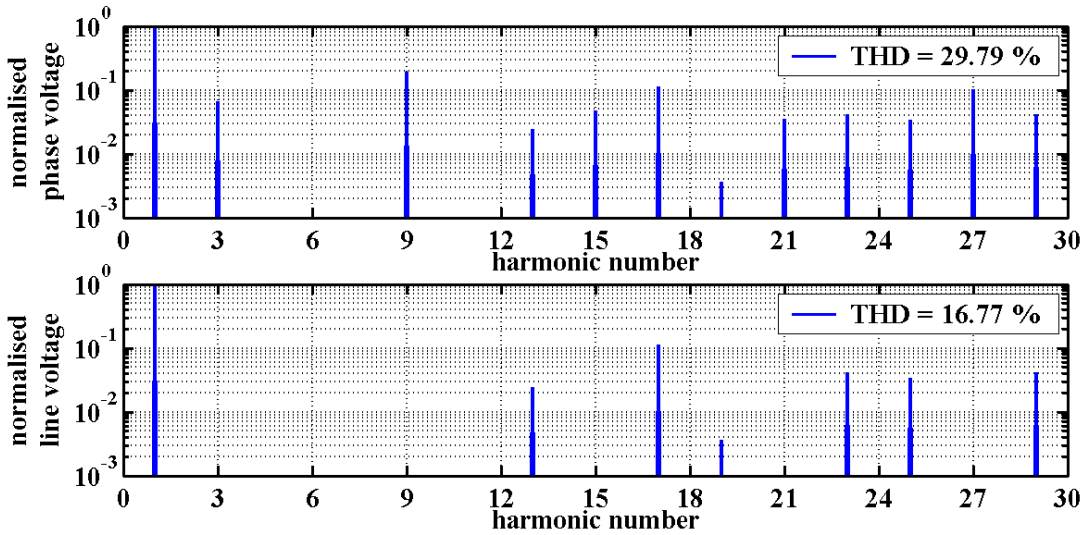


Figure 3.2.4: Ideal voltage spectra for SHE-4H4, and m_a = 0.85

Figure 3.2.5 and Figure 3.2.6 show the variations in THD and DF1 for SHE-4H2 and SHE-4H4 control. For amplitude modulation indexes below 0.4, it is impossible to make use of harmonic elimination without compromising the fundamental amplitude, when using SHE-4H2 staircase approach. SHE-4H4 can eliminate the 5th and 7th harmonics below m_a = 0.4, and it is able to eliminate the three low order harmonics up to m_a = 0.9, apart from a region around m_a = 0.65, where no unique solutions can be found.

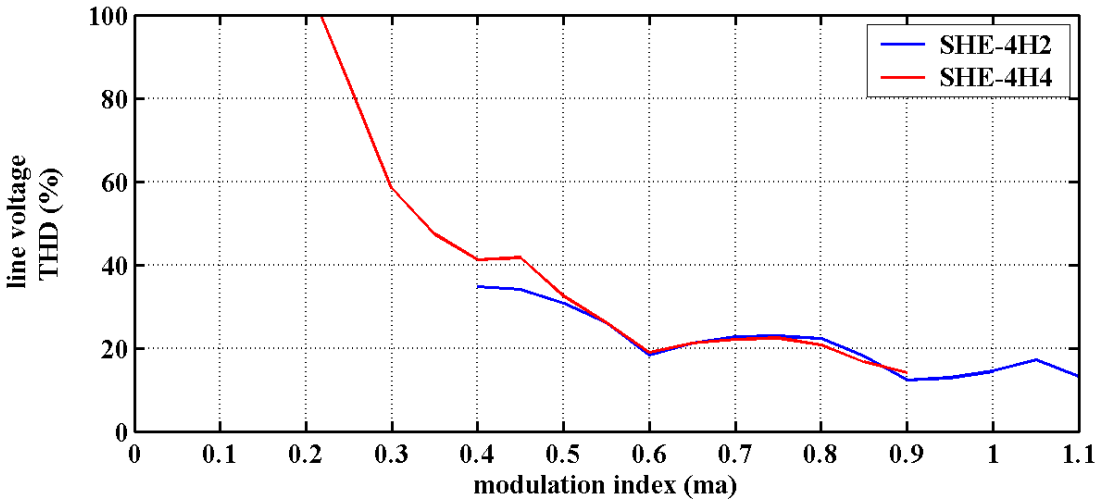


Figure 3.2.5: Line voltage THD variation with modulation index

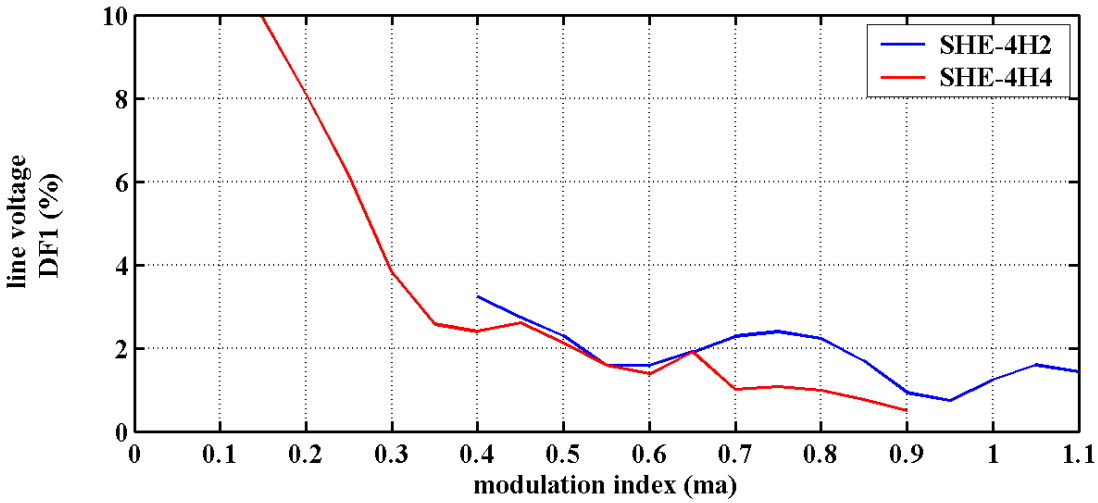


Figure 3.2.6: Line voltage DF1 variation with modulation level index

The figures illustrate that a line voltage THD level in the region of 20% is achievable using all schemes above m_a = 0.6 with very little difference between them. This low harmonic capability at low switching frequency is one of the many benefits of multilevel inverters. The DF1 performance, which is an indicator of an inductive load current harmonic distortion content, does however show a benefit in using more than two angles where the first significant harmonic is the 13th. Increasing the number of commutation angles to eliminate higher harmonics has practical limitations. It is difficult to obtain solutions over all m_a values, and it would increase the complexity of the control implementation. The practical implementation for angle control will use counter-comparators for each reference angle. SHE-4H4 can be implemented using four such digital logic blocks and is consistent with a reusable approach envisaged in a universal digital controller for implementing other PWM schemes. Selective harmonic elimination control scheme can be likened to a PWM scheme with a low carrier frequency, and is often referred to in the literature as SHE-PWM. This term generically defines all pre-computed angle control schemes which do not result in staircase waveforms.

It would be possible to increase the number of switching events and harmonics eliminated, but the digital control implementation is limited to only four counters and comparators. Therefore, the optimum control scheme to be used for the investigation will employ SHE-4H4 for m_a less than 0.9, and SHE-4H2 above that level up to the maximum achievable m_a = 1.15. A waterfall plot, Figure 3.2.7, best illustrates the amplitudes of the spectral components below 1000 Hz for a 50 Hz fundamental. It graphically illustrates the marked reduction in low order harmonics achievable in an ideal system. The lack of solutions for harmonic elimination around m_a = 0.65 is clear from the peaks at the 5th and 7th present in the spectra. The triplen harmonic

elimination in the line voltage across the balanced three-phase is also clear in the waterfall plot.

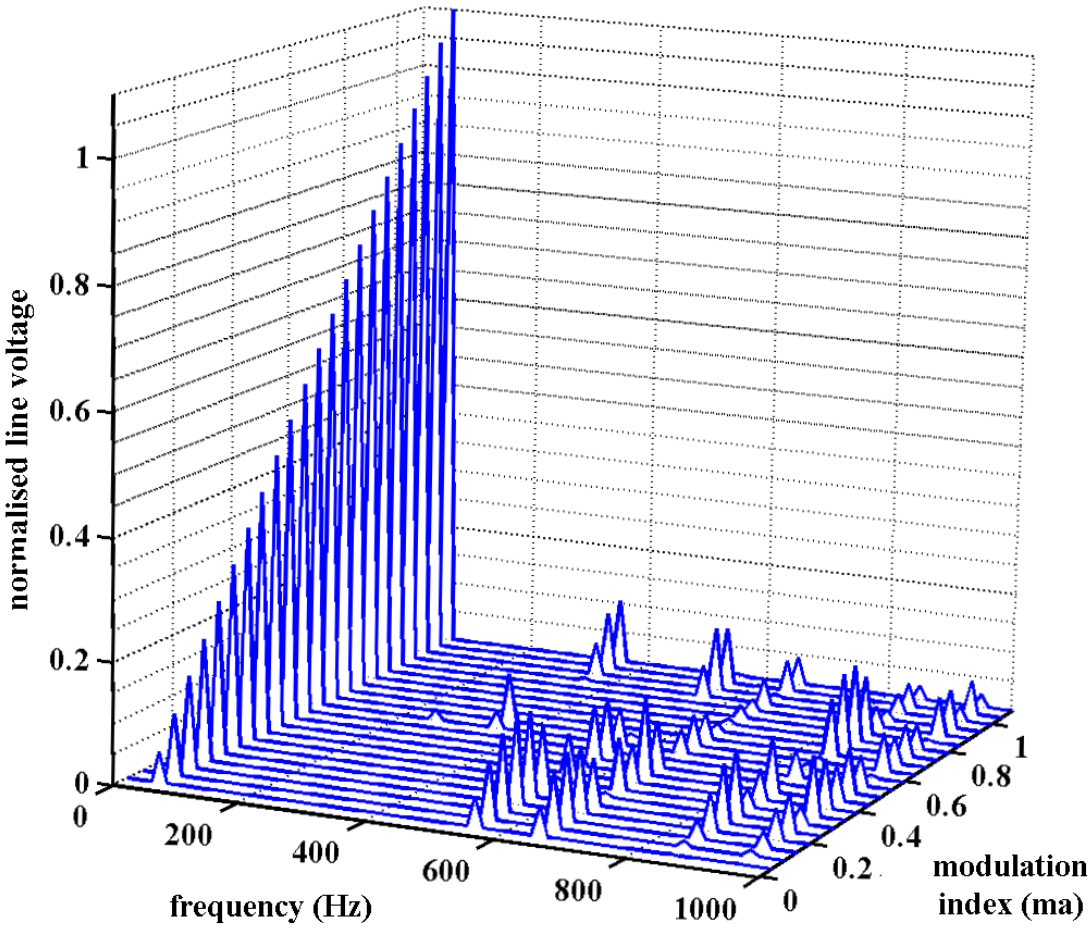


Figure 3.2.7: Ideal line voltage spectrum versus m_a, for optimised SHE scheme

3.3 Pattern Balancing Control Strategy

The four-cell, five-level flying-capacitor inverter can be controlled in a balanced manner under steady-state conditions by cycling through a set of switching patterns. This is an open-loop mode of control with no capacitor voltage measurement, and relies on the natural self-balancing behaviour of the flying-capacitor inverter. To achieve self-balancing, the overall pattern is repeated once every four cycles (number of cells), with different switch states used at the same voltage level of each cycle. This ensures that all four possible switch states are used, and ideally the mean current flowing in all capacitors is zero under steady-state conditions. This approach is illustrated in Figure 3.3.1.

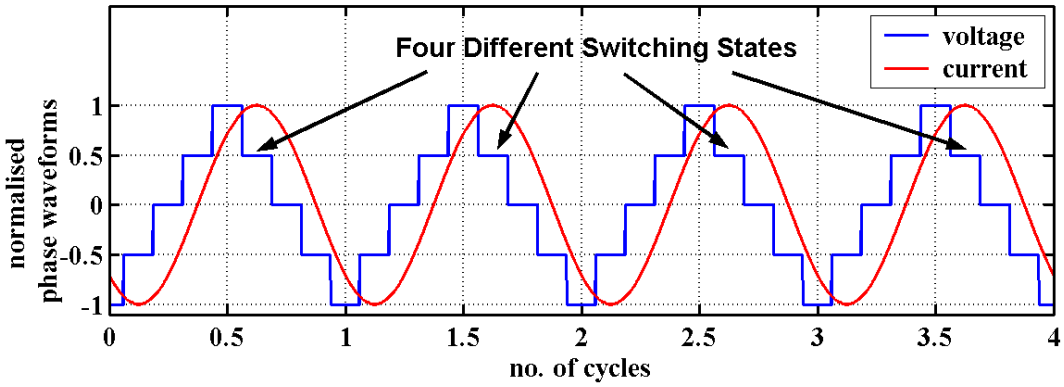


Figure 3.3.1: Ideal phase waveforms with 45^{o} lagging current

This section describes the optimum pattern selection for balancing the inverter's cell capacitors. A sensed voltage balancing scheme is also proposed and compared with the open-loop pattern balancing approach. The following terms are used throughout the discussion:

state: refers to the inverter switch condition

sequence: refers to a set of inverter states from level -1 to +1

pattern: refers to a set of sequences for balancing over four cycles

3.3.1 Switching States in a Four-Cell Inverter

In the four-cell chopper circuit shown in Figure 3.3.2 which forms one phase limb of the three-phase inverter, there are 16 distinct switching states. Operation in each switching state causes a different change in voltage across the three cell-capacitors. The switching states and the net change for a positive load current in each cell capacitor voltage are listed in Table 3.3.1. As can be seen in the table, the four level 0.5 and -0.5 states all lead to different charging effects in the three cell-capacitors, and this is the reason why cycling is required in order to balance the inverter.

In the case of the level 0 switching states, these can be grouped in three pairs with complementary charging characteristics. The complementary pairs are states 3 & C, states 5 & A and states 6 & 9.

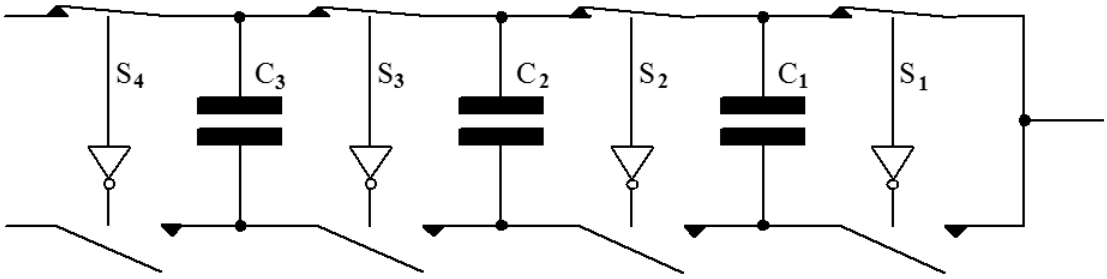


Figure 3.3.2: Four-cell inverter phase-limb circuit

Switching State $S_4S_3S_2S_1$	Output Voltage Level	Voltage Change C_3	Voltage Change C_2	Voltage Change C_1
0000 (0)	-1.0			
0001 (1)	-0.5			-VE
0010 (2)	-0.5		-VE	+VE
0100 (4)	-0.5	-VE	+VE	
1000 (8)	-0.5	+VE		
0011 (3)	0		-VE	
0101 (5)	0	-VE	+VE	-VE
0110 (6)	0	-VE		+VE
1001 (9)	0	+VE		-VE
1010 (A)	0	+VE	-VE	+VE
1100 (C)	0		+VE	
0111 (7)	+0.5	-VE		
1011 (B)	+0.5	+VE	-VE	
1101 (D)	+0.5		-VE	+VE
1110 (E)	+0.5			-VE
1111 (F)	+1.0			

Table 3.3.1: Capacitor voltage net change for each inverter limb switching state

Despite the large number of possible switching sequences in SHE staircase control, the number effectively is limited to those with only one switch state transition per level change, in order to ensure that switching losses are minimised. The number of allowable transitions between switching states in the four-cell inverter is illustrated in Figure 3.3.3. The switching state of the inverter is represented as a binary number with the most significant bit controlling the outer complementary switch pair nearest

the dc link (S_4). '1' indicates that the upper switch is in conduction and contributes to a net voltage level to the inverter output. The figure shows that there are:

4 possible paths between level -1 and a level -0.5;

3 possible paths between any level -0.5 and a level 0;

2 possible paths between any levels 0 and a level +0.5;

1 possible path between any level +0.5 and level +1;

Therefore, 24 different sequences of switching states can be used when stepping-up in voltage level between -1 and +1.

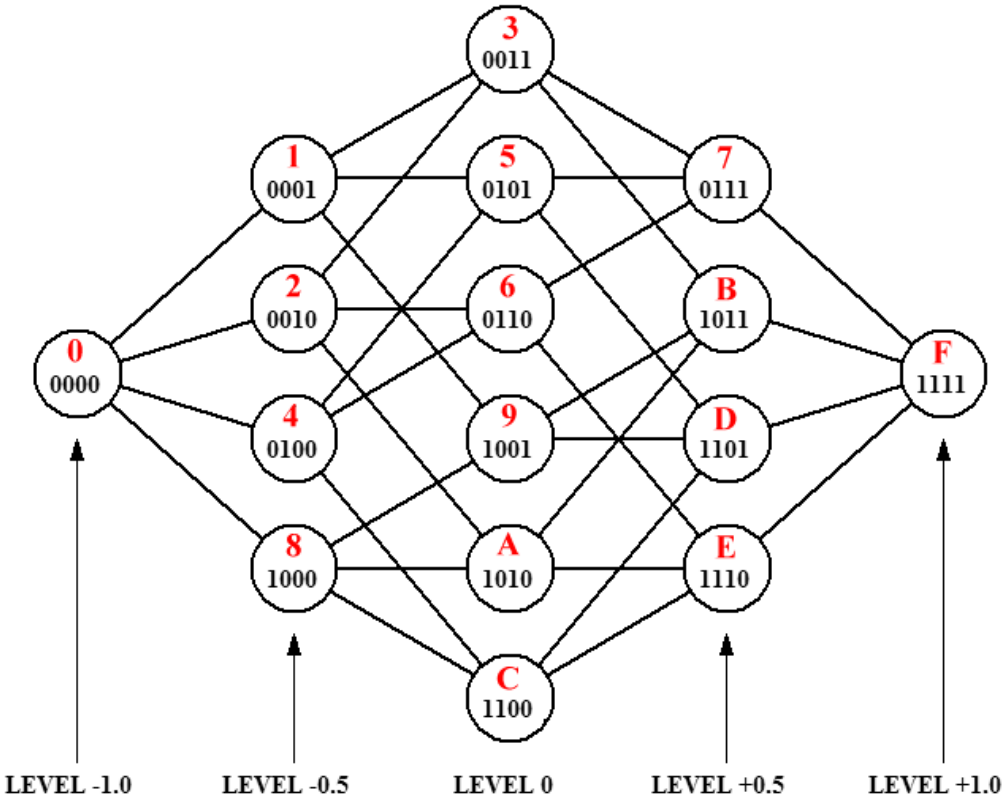


Figure 3.3.3: Allowable transitions between level states

3.3.2 Switching Pattern Selection

To analyse pattern selection, it is first assumed that the load filters all harmonics of the fundamental, and so that the load current waveform is a perfect sinusoid. In the majority of applications, the load is inductive and the phase current lags the phase voltage fundamental component. Figure 3.3.4 shows that relationship between the phase voltage and current under staircase SHE control. The figure also shows the component of load current which can flow through the cell-capacitors for two intermediary voltage levels. As can be seen from level 0 operation, the current is of

equal amplitude but of opposite polarity in the two halves of the staircase voltage cycle. This means that under ideal conditions, the same switching state could be used throughout for level 0 synthesis, since the mean current is zero. This can only be done for one of the cycles because of the requirement for cycling through all four levels - 0.5 and +0.5 switching states, with minimum switching transitions. There is no symmetry to exploit in the level +0.5 case but four cycle rotating of switching states can only be used to maintain next zero charging. Also there is no symmetry in the load current to exploit for balancing purposes when operating at level +0.5, so all four switching states have to be cycled through.

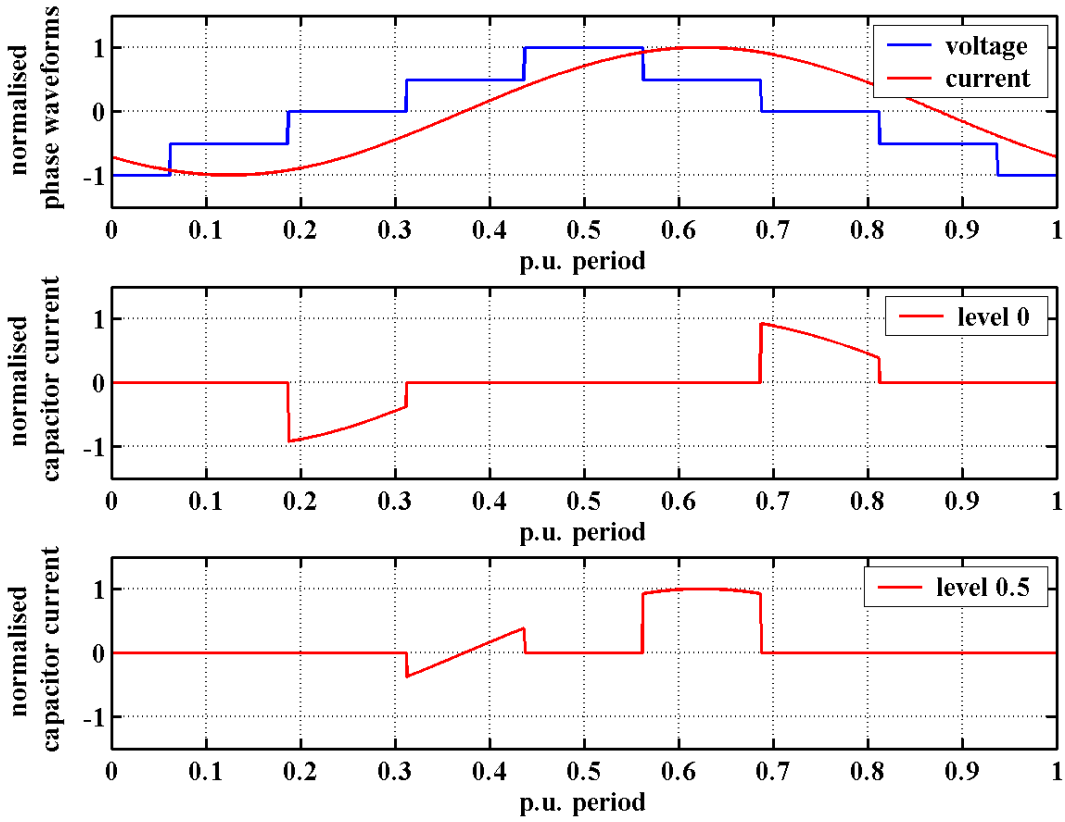


Figure 3.3.4: Idealised phase waveforms with 45^{o} lagging current

A good starting point in identifying valid balancing switching patterns is to keep the individual level switching states the same over one complete cycle, thus forming a sequence. The following labelling is used for each cycle sequence,

$$\overset{U}{\underset{L}{M}}$$

where

L is level -0.5 switching state, using hexadecimal notation

M is level 0 switching state, using hexadecimal notation

U is level +0.5 switching state, using hexadecimal notation

For instance, if the switching states to be used in one cycle are [0000], [0001], [1001], [1101] and [1111], then the switching sequence is $\overset{D}{9}_{1}$. Using the above sequence labelling, the 24 possible switching sequences are as follows:

$$\overset{7}{3}_{1},\ \overset{B}{3}_{1},\ \overset{7}{5}_{1},\ \overset{D}{5}_{1},\ \overset{B}{9}_{1},\ \overset{D}{9}_{1},\ \overset{7}{3}_{2},\ \overset{B}{3}_{2},\ \overset{7}{6}_{2},\ \overset{E}{6}_{2},\ \overset{B}{A}_{2},\ \overset{E}{A}_{2},\ \overset{7}{5}_{4},\ \overset{D}{5}_{4},\ \overset{7}{6}_{4},\ \overset{E}{6}_{4},\ \overset{D}{C}_{4},\ \overset{E}{C}_{4},\ \overset{B}{9}_{8},\ \overset{D}{9}_{8},\ \overset{B}{A}_{8},\ \overset{E}{A}_{8},\ \overset{D}{C}_{8},\ \overset{E}{C}_{8}$$

From inspection of the switching pattern permutations, it is clear that there are groups of 6 pattern permutations made up of just 4 individual sequences, where the sequence order is varied. The basic requirement is that all four -0.5 and +0.5 level states are used, but the level 0 states can be taken from either one complementary pair set or two sets. There are in fact 24 different groups of switching sequences that meet the minimum switching transition criteria. These groups of sequences are listed in Table 3.3.2, with the level 0 contributing states shown as reference.

Level 0	**Switching Sequence Groups**			
3+C and 6+9	$\overset{7\ E\ D\ B}{3_1, 6_2, C_4, 9_8}$	$\overset{B\ 7\ E\ D}{3_1, 6_2, C_4, 9_8}$	$\overset{B\ 7\ E\ D}{9_1, 3_2, 6_4, C_8}$	$\overset{D\ B\ 7\ E}{9_1, 3_2, 6_4, C_8}$
3+C and 5+A	$\overset{7\ B\ D\ E}{3_1, A_2, 5_4, C_8}$	$\overset{B\ E\ 7\ D}{3_1, A_2, 5_4, C_8}$	$\overset{7\ B\ D\ E}{5_1, 3_2, C_4, A_8}$	$\overset{D\ 7\ E\ B}{5_1, 3_2, C_4, A_8}$
6+9 and 5+A	$\overset{7\ B\ E\ D}{5_1, A_2, 6_4, 9_8}$	$\overset{D\ E\ 7\ B}{5_1, A_2, 6_4, 9_8}$	$\overset{B\ 7\ D\ E}{9_1, 6_2, 5_4, A_8}$	$\overset{D\ E\ 7\ B}{9_1, 6_2, 5_4, A_8}$
3+C	$\overset{7\ B\ D\ E}{3_1, 3_2, C_4, C_8}$	$\overset{7\ B\ E\ D}{3_1, 3_2, C_4, C_8}$	$\overset{B\ 7\ D\ E}{3_1, 3_2, C_4, C_8}$	$\overset{B\ 7\ E\ D}{3_1, 3_2, C_4, C_8}$
5+A	$\overset{7\ B\ D\ E}{5_1, A_2, 5_4, A_8}$	$\overset{7\ E\ D\ B}{5_1, A_2, 5_4, A_8}$	$\overset{D\ B\ 7\ E}{5_1, A_2, 5_4, A_8}$	$\overset{D\ E\ 7\ B}{5_1, A_2, 5_4, A_8}$
6+9	$\overset{B\ 7\ E\ D}{9_1, 6_2, 6_4, 9_8}$	$\overset{B\ E\ 7\ D}{9_1, 6_2, 6_4, 9_8}$	$\overset{D\ 7\ E\ B}{9_1, 6_2, 6_4, 9_8}$	$\overset{D\ E\ 7\ B}{9_1, 6_2, 6_4, 9_8}$

Table 3.3.2: 24 groups of switching sequences

Taking the upper left group in the table as an example, the 6 pattern permutations in this group are as follows:

$$\overset{7\,E\,D\,B}{36C9_{1\,2\,4\,8}},\ \overset{7\,E\,B\,D}{369C_{1\,2\,8\,4}},\ \overset{7\,D\,E\,B}{3C69_{1\,4\,2\,8}},\ \overset{7\,D\,B\,E}{3C96_{1\,4\,8\,2}},\ \overset{7\,B\,E\,D}{396C_{1\,8\,2\,4}},\ \overset{7\,B\,D\,E}{39C6_{1\,8\,4\,2}}$$

Therefore, there are 144 valid balancing patterns that meet the minimum switch transition criterion. With such a large number of possible balancing patterns it would be beneficial to identify rules with in the pattern itself which will lead to improved performance. It would make sense that large variations in the capacitor voltages would

lead to poorer output power quality with larger harmonic distortion, and potentially lead to over-voltage stress in the power semiconductors.

With reference to Figure 3.3.5, showing levels -0.5 and +0.5 highlighted when the phase current amplitude is maximum, a pattern rule can be deduced which should reduce overall capacitor voltage ripple. These regions will have the largest levels of capacitor voltage variation. In the pattern, the sequence is changed after level -1, so if the switching state at level +0.5 in the previous sequence gives the same polarity voltage change as the next sequence's switching state at level -0.5, then this is to be avoided. Therefore preferred patterns should not include the next level -0.5 state being the 1's complement of the previous level +0.5 state. For instance, state 8 [1000] should not follow state 7 [0111] and visa versa. This means that the first rule states that the following consecutive sequences pairs are not preferred:

$$\overset{7}{X}\overset{X}{X}_{X\,8},\ \overset{E}{X}\overset{X}{X}_{X\,1},\ \overset{D}{X}\overset{X}{X}_{X\,2} \text{ and } \overset{B}{X}\overset{X}{X}_{X\,4}$$

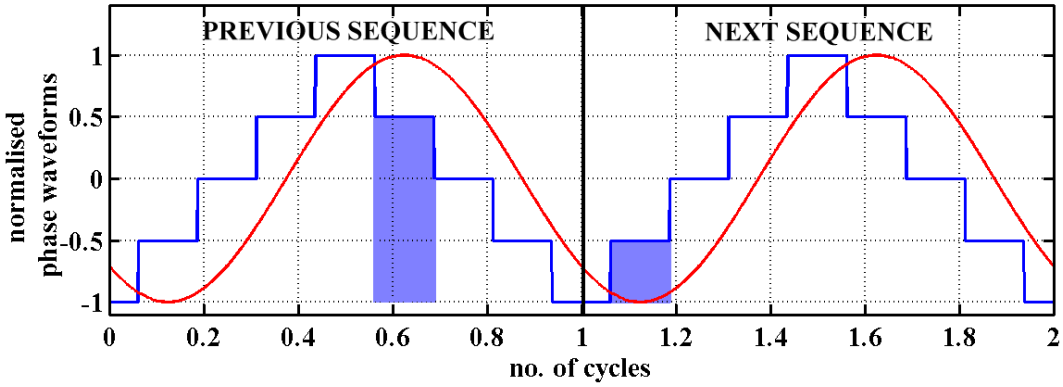


Figure 3.3.5: Idealised phase waveforms with 45^{o} lagging current

The second rule regards the charging/discharging of capacitors within a cycle sequence. When adjacent cells are in a different conduction state, then the capacitor between the cells lies in the current path, and so its voltage will change. Again, with regard to the peak and trough of the current occurring around level +0.5 and level -0.5 respectively, it is preferable that as many as possible cells are in the same state at both levels. Priority for this rule can be assigned to the higher voltage capacitor, C_3, which will see the largest voltage change, and in this case S_4S_3 should be the same. Therefore, level -0.5 state is 4 [0100], then state 7 [0111] is preferred for level +0.5. This also means that 8 [1000] and B [1011] are preferred within a sequence. Another condition applied to state transitions within a sequence is only to switch one cell transistor pair at a time. This means that only four sequences would be preferred for

minimising the voltage variation on C_3 over one sequence cycle, and in each case the C_3 is in the same current path throughout the cycle. These are

$$\overset{7}{5}_{4},\overset{7}{6}_{4},\overset{B}{9}_{8} \text{ and } \overset{B}{A}_{8}$$

Taking the first sequence as an example, Figure 3.3.6 shows the resultant current flowing through C_3. As can be seen, there is symmetry in the cell-capacitor current and so the mean value is zero leading to no net change in cell-capacitor voltage

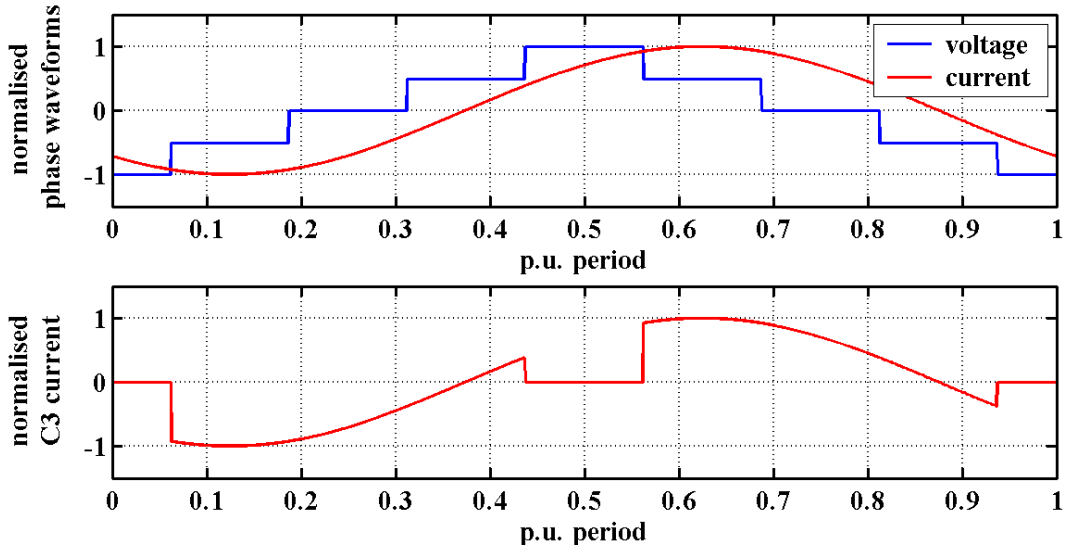


Figure 3.3.6: Idealised phase waveforms and C_3 current

This second rule can be applied also C_2, and to C_1, so there are a further four preferred sequences for inclusion in a pattern, namely

$$\overset{D}{5}_{4}, \overset{D}{C}_{4}, \overset{E}{6}_{2} \text{ and } \overset{E}{A}_{2}$$

It is now possible to make a judgement as to which pattern will give a better performance with lowest cell-capacitor voltage ripple. By first eliminating patterns that break the first rule governing consecutive sequences, and then examining the remaining balancing patterns, the following pattern is predicted to offer the best performance:

$$\overset{7\,E\,D\,B}{3\,6\,C\,9}_{1\,2\,4\,8} \qquad \ldots \textbf{PATTERN \#1}$$

This pattern does not have any consecutive sequences which break the first rule governing the level +0.5 followed by level -0.5. This pattern also contains 2 sequences from the second rule which have preferred state combinations for levels -0.5 and +0.5.

The various balancing patterns can also be screened for ones which are likely to cause poor overall performance. One such pattern which breaks the first rule and only has one good sequence from the second rule for C_1 is

$$\overset{7\ B\ E\ D}{3\ A\ C\ 5}_{2\ 8\ 4\ 1} \quad \ldots \textbf{PATTERN \#2}$$

The above analysis is based on the assumption that the load is inductive with a lagging phase current. The same rule-based analysis can be done for other load characteristics. In the case of a leading phase current angle, the second rule governing a sequence still applies, but the first rule's reasoning is the same but applied this time to a sequence level -0.5 state followed by the next sequence level +0.5 state.

3.3.3 Comparison of Balanced Switching Patterns

To confirm that the rules governing better performing patterns is valid, detailed simulations were run on the two switching patterns identified previously. The simulation results are presented in Table 3.3.3, together with results for the ideal case when the inverter is perfectly balanced and there is no capacitor voltage variation. The dc link voltage was set to 400 V and the SHE-4H2 5th harmonic elimination control settings were m_a = 1 and a fundamental frequency of 50 Hz. The phase voltage fundamental is therefore 141.4 Vrms and the line voltage fundamental is 244.9 rms. A basic R = 2.5 Ω, L = 7.958 mH load model was used (displacement power factor = 0.707) and the individual cell-capacitance is 10 mF. The energy factor, ξ, is 30 s^{-1} and the nominal output power for an equivalent ideal sinusoidal system is 12 kW.

The results indicate good correlation with the predicted performance based on the analysis of the balancing patterns and the rules governing the behaviour of the capacitor voltage ripple. As predicted PATTERN #1, $\overset{7\ E\ D\ B}{3\ 6\ C\ 9}_{1\ 2\ 4\ 8}$, has lower output waveform harmonic distortion compared to PATTERN #2, $\overset{7\ B\ E\ D}{3\ A\ C\ 5}_{2\ 8\ 4\ 1}$. The table also shows that by optimum pattern selection the phase and line voltage THD can be lower than the ideal case, with fixed capacitor voltages. However, because of the additional sub- and inter harmonics at the low frequency, phase current THD is higher. The DF1 term indicates good correlation in predicting the THD of the phase current for this particular simple inductive load. In reality, the phase current THD is the lowest achievable, and for an induction motor the distortion will be greater due to a lesser filtering effect of the smaller phase resistance and leakage inductance.

Parameter	Ideal	PATTERN#1	PATTERN#2
Actual modulation depth, m_a	1.000	1.029	1.030
True power factor	0.694	0.697	0.686
Phase voltage THD (%)	19.25	16.92	23.81
Line voltage THD (%)	14.53	13.07	19.88
Line voltage DF1 (%)	1.25	3.56	9.38
Phase current THD (%)	1.76	3.49	9.41
Capacitor mean voltages (% p.u. cell)	100.0	98.0	75.7
	200.0	198.4	197.5
	300.0	312.1	333.2
	400.0	400.0	401.9
Capacitor peak voltages (% p.u. cell)	100.0	112.4	105.1
	200.0	212.1	239.0
	300.0	332.3	369.3
	400.0	418.2	431.0
Switch peak blocking voltages (% p.u. cell)	100.0	112.4	105.1
	100.0	128.6	170.1
	100.0	167.8	205.9
	100.0	137.2	140.3

Table 3.3.3: Results breakdown comparison for example patterns and ideal case

The simulated output power and voltage regulation do not show any marked difference due to the different patterns adopted. There is a 3% error in the actual modulation depth as expressed as the ratio of the peak of the fundamental frequency component to half the dc link, and is due to the capacitor ripple voltages. A correlation can be seen between load true power factor and THD, as would be expected, since the distortion is an unwanted component contributing only to circulating energy.

Figures 3.3.7 and 3.3.8 show the output waveforms for the two balancing schemes and clearly show the effect the variations in capacitor voltage have on the voltage waveforms. The current waveforms in both cases are essentially sinusoidal since the load is an ideal resistor plus inductor and the harmonic distortion is low. The phase waveforms do not give a clear indication of the harmonic content differences between the patterns. However, the line voltage for the PATTERN #2 does show marked distortion compared to PATTERN #1.

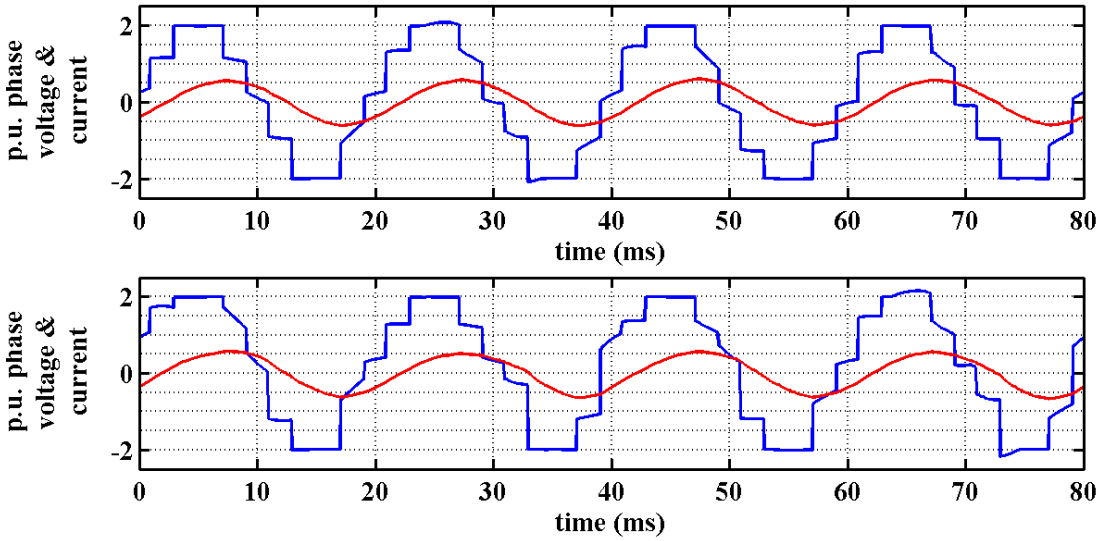


Figure 3.3.7: Phase waveforms, PATTERN #1 (top), PATTERN #2 (bottom)

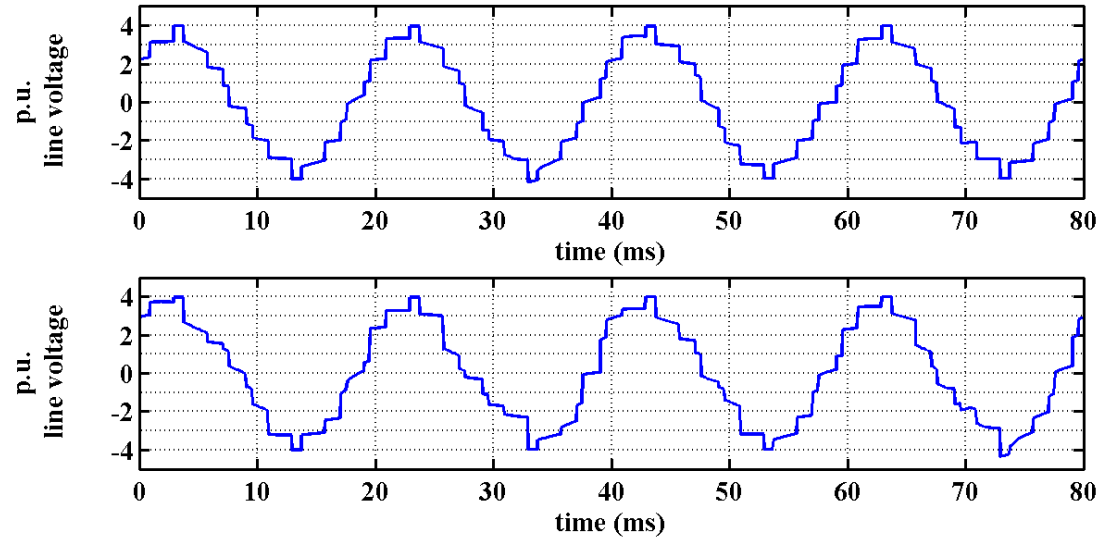


Figure 3.3.8: Line voltages, PATTERN #1 (top), PATTERN #2 (bottom)

The difference in THD between the two balancing pattern control schemes is reflected in the respective frequency spectra. Figure 3.3.9 shows the line voltage spectrum for the two cases, with the frequency components normalised with respect to the fundamental. There are now sub- and inter-harmonics present in the spectra due to the capacitor voltage variations compared with the ideal case. This ought to cause an increase in the THD, but this is not the case for the better pattern. The variations in the capacitor voltages cause the 7^{th} order harmonic to reduce but not at the expense of greater harmonic distortion and additional sub- and inter-harmonic components. The phase current spectra compared in Figure 3.3.10 also show the increased harmonics at

lower frequency, with the 100 Hz and 125 Hz components especially prominent in the PATTERN #2 case.

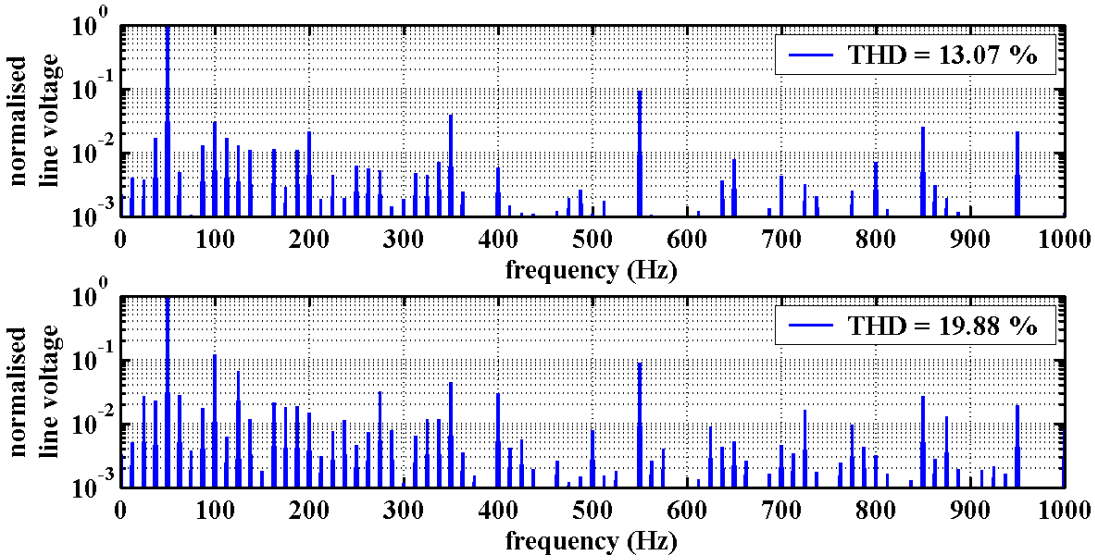


Figure 3.3.9: Line voltage spectrum, PATTERN #1 (top), PATTERN #2 (bottom)

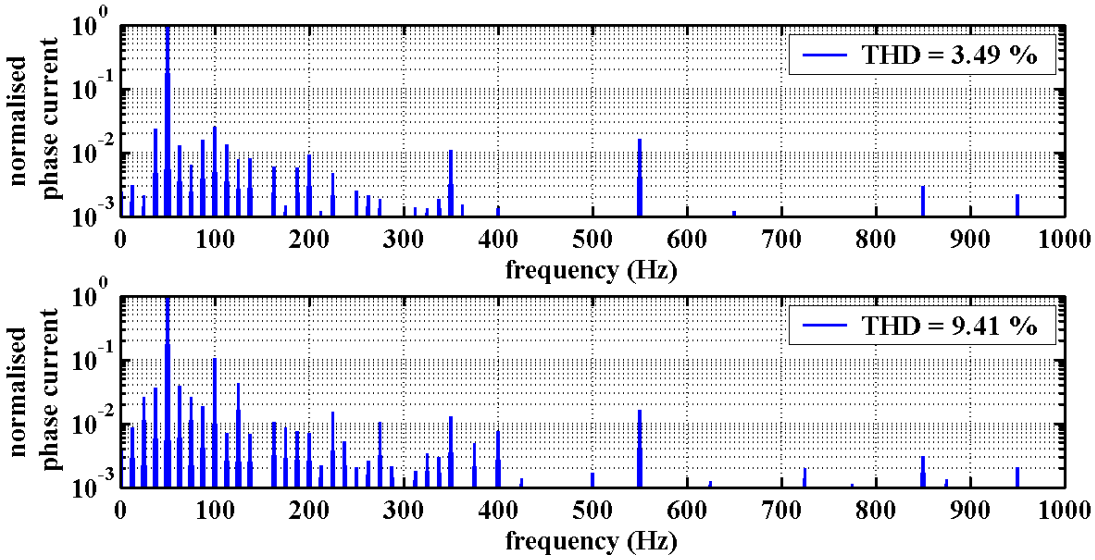


Figure 3.3.10: Phase current spectrum, PATTERN #1 (top), PATTERN #2 (bottom)

The difference in the spectrum between the two schemes can be explained by a noticeable increase in the lower sub- and inter-harmonics, especially the even harmonics, such as the 100 Hz component, which would not be present in an ideal system. These even harmonics can only be generated by asymmetry in the phase voltage. Given that the dc component is effectively zero, the interspersion of varying capacitor voltages on the resultant phase voltage must introduce asymmetry.

The even harmonics present in both patterns points due to a 12.5 Hz fundamental frequency component being present within the system, and its amplification by poor selection of switching pattern. This fundamental component is due to the balancing pattern control strategy and caused by patterns only repeating every four cycles, i.e. 12.5 Hz.

The capacitor voltage waveforms are the most revealing when viewed in the time-domain. Figure 3.3.11 shows the individual cell-capacitor voltages, plotted on the same zero axis for reference, of the inverter controlled by the two balancing pattern schemes. With PATTERN #1, voltage ripple is reasonably low with blocking voltage variations peaking at ±50 % of the nominal values. There can be seen an 80 ms repetition rate in the waveforms and this is most obvious in the capacitor voltages in the poorer performing pattern: a clear indication that this is the primary mechanism for harmonic distortion or even selective harmonic attenuation for the better pattern.

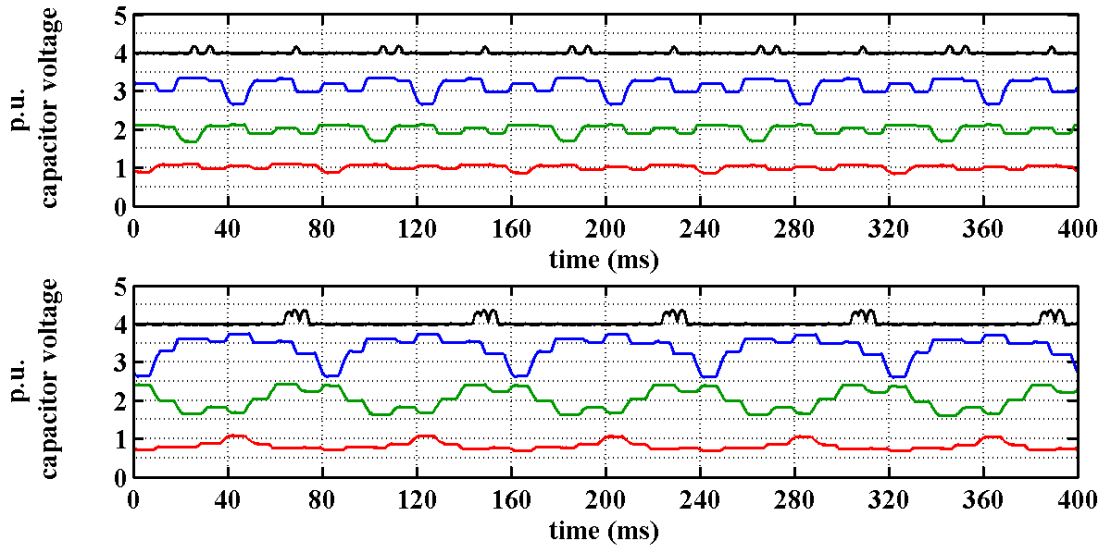


Figure 3.3.11: Capacitor voltages, PATTERN #1 (top), PATTERN #2 (bottom)

3.3.4 Comparison of Balanced Patterns with Different Energy Factors

A revealing comparison of the performance under the different balancing patterns can be made by varying the energy factor, ξ, so that the voltage ripple level varies. Figure 3.3.12 shows the variation in line voltage THD when controlling with the two different patterns. Note that the larger the value of ξ, the smaller the individual cell-capacitance, and so system size and cost can be thought of as decreasing to the left. As can be seen, the performance deviates away from the ideal achievable level, in a beneficial fashion for the best pattern, and detrimentally for the poorer performing

pattern. The phase current THD characteristics, shown in Figure 3.3.13, also show marked improvement when PATTERN #1 is used for balancing.

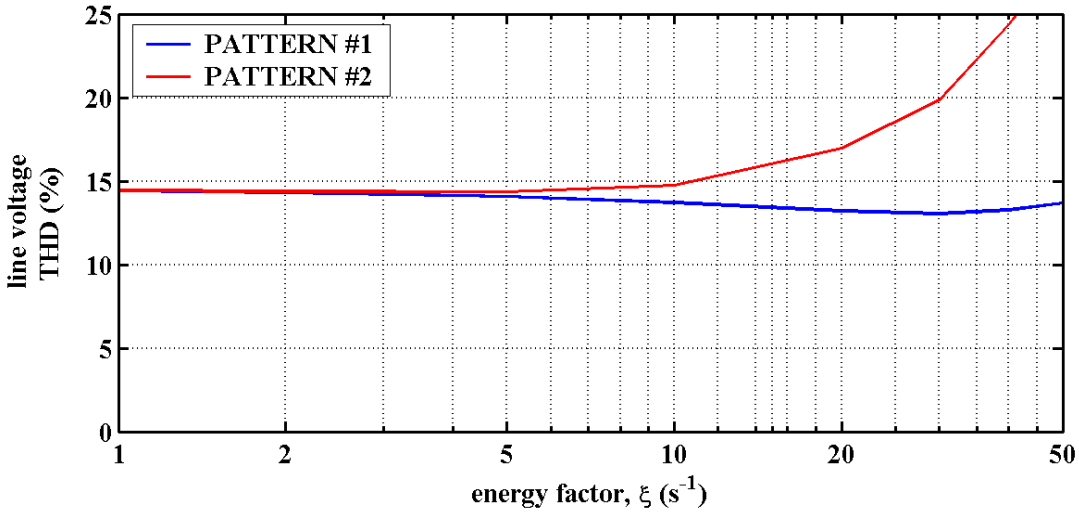


Figure 3.3.12: Variation of line voltage THD with energy factor, ξ

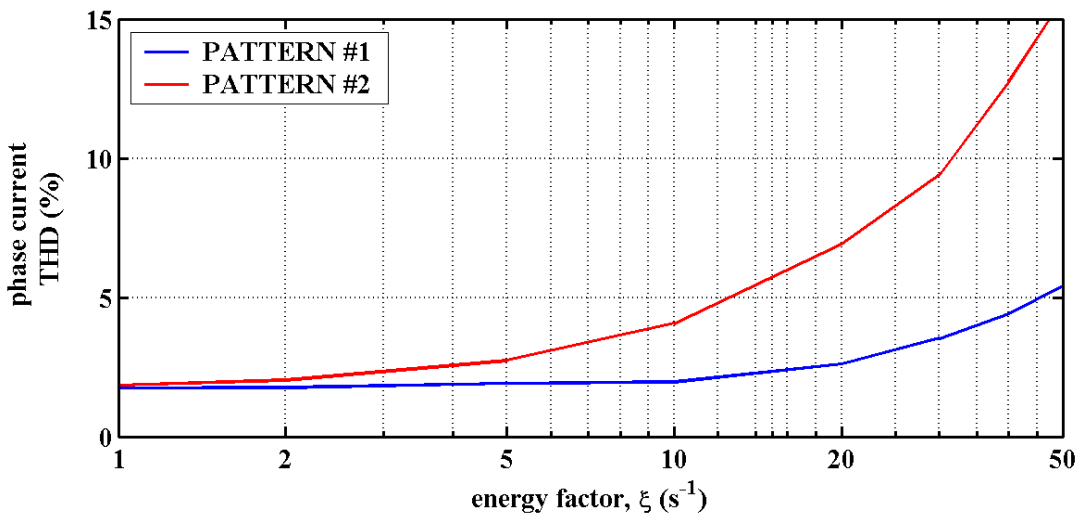


Figure 3.3.13: Variation of phase current THD with energy factor, ξ

3.3.5 Effect of Optimum Balancing Pattern on Different SHE Schemes

The aim of section is to ascertain the effect on output harmonic distortion over the whole range of modulation indexes. The balancing pattern selection was based on the simplest staircase SHE-4H2 control, and so it is important to see the influence it has on SHE-4H4 performance.

Figures 3.3.14 and 3.3.15 show the variations in the THD for the line voltage and phase current as a function of m_a when the best switching pattern is applied to balance

the cell-capacitor voltages. The line voltage THD is similar to the ideal case with no capacitor voltage ripple for forms of SHE control. However, the phase current THD for SHE-4H4 is actually worse than the simpler SHE-4H2 scheme, indicating that the variation in cell-capacitor voltages for the optimum pattern has detrimental effect on harmonic generation. This result suggests that the positive benefits of an optimally selected balancing pattern are only applicable to a staircase output waveform. The reduction in harmonic distortion achievable in higher switching frequency forms of SHE control under ideal cell-capacitor voltage conditions will be negated by the sub- and inter-harmonic generation due to the pattern-based balancing strategy. Therefore, only the staircase form, SHE-4H2, will be considering in the remaining part of this chapter.

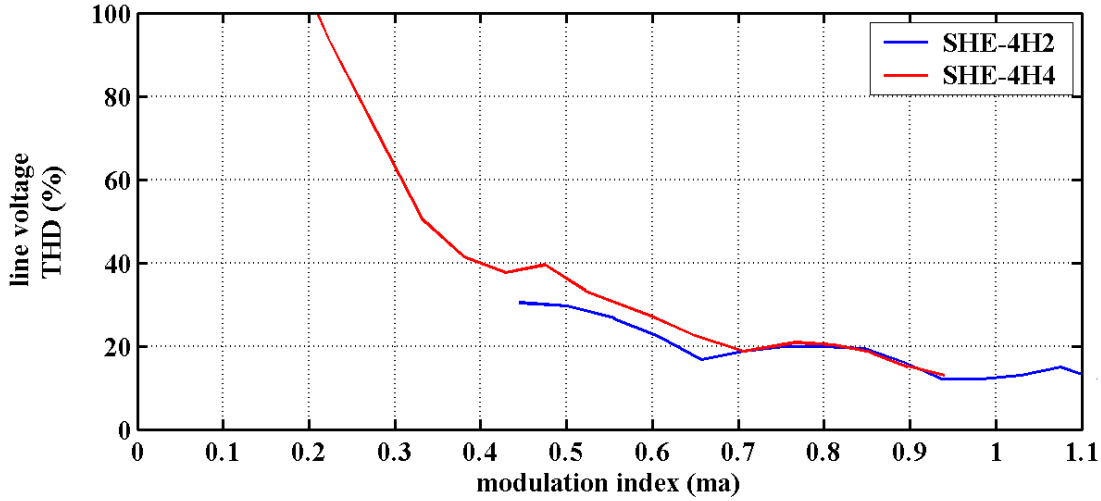


Figure 3.3.14: Line voltage THD variation with achieved modulation index

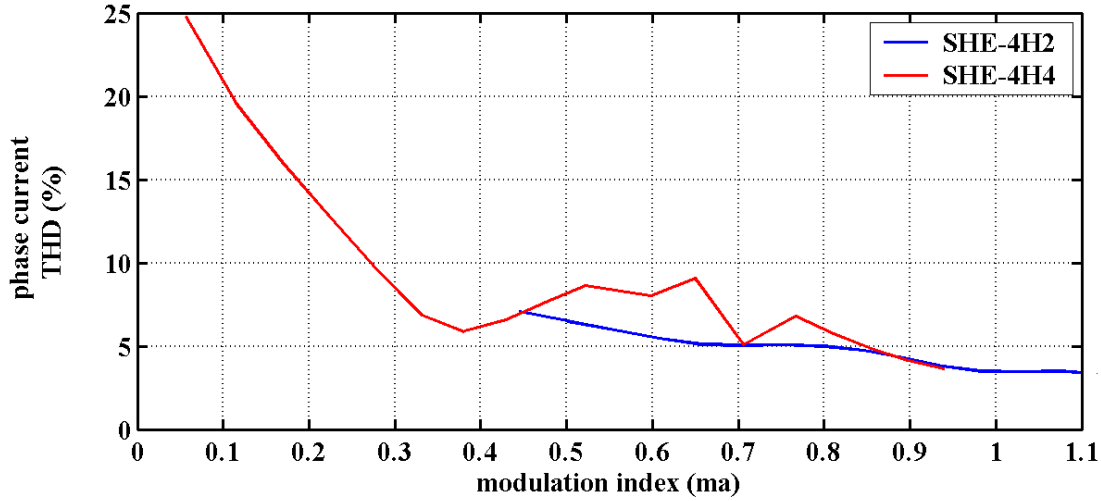


Figure 3.3.15: Phase current THD variation with achieved modulation index

3.3.6 Closed-Loop Capacitor Voltage Balancing

Although the flying-capacitor inverter has a natural self-balancing characteristic, it is recognised that pattern control without voltage sensors will not cope well when the load parameters vary considerably within a cycle [3.9]. There have been a number of proposed schemes for maintaining balanced regulation of the cell-capacitor voltages specifically under PWM control [3.10, 3.11]. No work has been reported for balancing when using staircase SHE control and so an algorithm which will accomplish balanced operation is proposed in this section.

It has already been demonstrated that there is a relationship between the level of harmonic distortion in the output waveforms and the cell-capacitor voltage ripple amplitude. By sensing the capacitor voltages and using optimised switching state selection, the large variations in capacitor voltages seen especially for PATTERN #2 should be reduced.

The proposed method employs comparators for an upper and lower voltage level band for each capacitor. Their output states are combined so that the signals for each capacitor are shown in Table 3.3.4. This uses the relationship between the switch state of those mutually connected to a capacitor and charging/discharging behaviour dependency on current direction. For instance, an adjacent two cells' state of '10' with a positive phase current flowing will boost the voltage across the capacitor connected between the cells.

Capacitor	**Over-voltage Condition**		**Under-voltage Condition**	
	Positive Current	**Negative Current**	**Positive Current**	**Negative Current**
C_3	0100	1000	1000	0100
C_2	0010	0100	0100	0010
C_1	0001	0010	0010	0001

Table 3.3.4: Truth table for capacitor voltage comparators

Using these comparator signals, a simple algorithm for a four-cell inverter can be implemented to decide the optimum switching state to apply to the inverter at a given level. A flow diagram of the algorithm is shown in Figure 3.3.16. The algorithm input signals are the three comparator outputs C1 - 3 and the required output voltage level L. The state of the highest voltage capacitor is checked first. If it is within bands [0000], then the state of the middle capacitor is checked, otherwise the output firing switching state S is assigned to C3. If C2 is outside the regulation bands then S is

assigned to C2. The comparator signal C1 for the lowest voltage capacitor is added to S only if the state of C2 is [0000]. This gives a potential switching state for the inverter control. If all three capacitor voltages are within the regulation bands, S = [0000], then the optimum pattern for the given voltage level demand is found using a look-up table. Otherwise, S is checked to ensure that it will operate the inverter at the required voltage level. If this is not the case, S is either incremented of decremented until the switching state gives the appropriate voltage level.

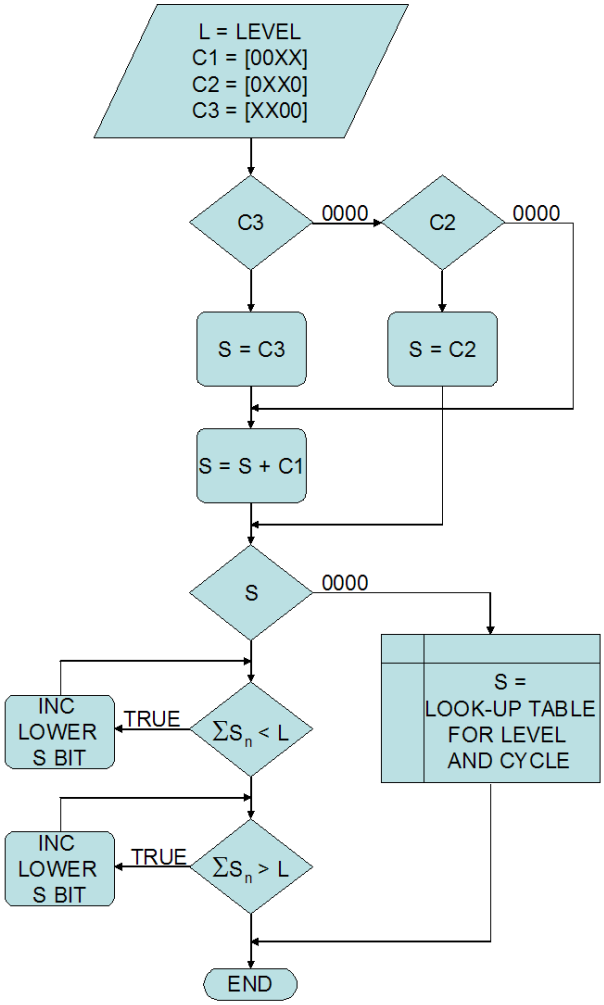


Figure 3.3.16: Flow-chart for closed-loop capacitor voltage balancing

Simulations were conducted under the same conditions as before and the resultant capacitor voltages are shown in Figure 3.3.17, and compared with the optimum PATTERN #1 result. This shows that the voltage ripple has been reduced by applying feedback, but this appears to lead to a pseudo-random behaviour rather than a nicely repeating waveform as before. The tolerance band was set at ±5%, and it was found that tighter tolerances caused instability in the simulation. The mean capacitor

voltages were all kept within 3% of the target values, and the peak voltages were reduced compared with PATTERN #1. For instance, peak voltage on C_3 as a percentage of the unit cell-voltage was 318.2% compared to 332.3%. This shows that the algorithm is achieving balanced voltage control with reduced ripple even compared with the optimum selected pattern. The maximum blocking voltage as a percentage of unit cell-voltage across any switch was also reduced to 156.4%, compared to 167.8% for PATTERN #1. This shows that some improvement can be gained in protecting against over-voltage conditions across the power switch, or it may be possible to increase output power for a given cell-capacitance.

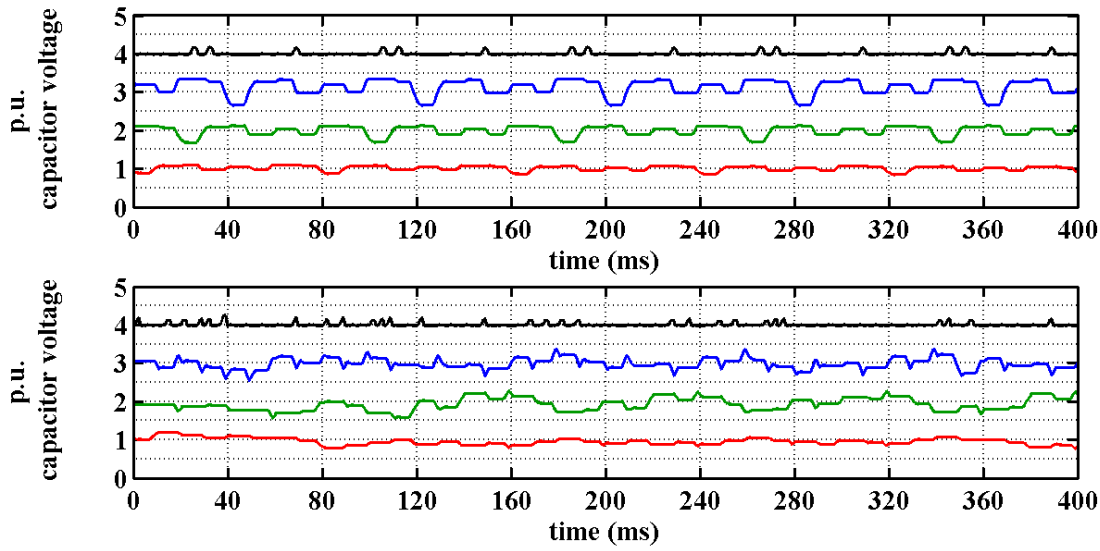


Figure 3.3.17: Capacitor voltage ripple, PATTERN #1 (top) and regulated capacitor voltage (bottom)

The effect of the change in capacitor voltage on output power quality is shown in the plots of line voltage and phase current spectra. For comparison, the PATTERN #1 spectra are also shown in Figures 3.3.18 and 3.3.19. The most interesting feature in the harmonics is a general increase in the sub- and inter-harmonics, but the 100 Hz component is noticeably reduced. This is due to the more random nature of the capacitor ripple waveform effectively spreading the spectral components. This is reflected in increased line voltage and phase current THD, but the values are still lower than a poorly selected open-loop balancing pattern, PATTERN #2. These results indicate that under steady-state conditions, the pre-selected balancing pattern is preferred due its lower harmonic distortion characteristic, but in a real system the closed-loop cell-capacitor voltage control would ensure better transient operation.

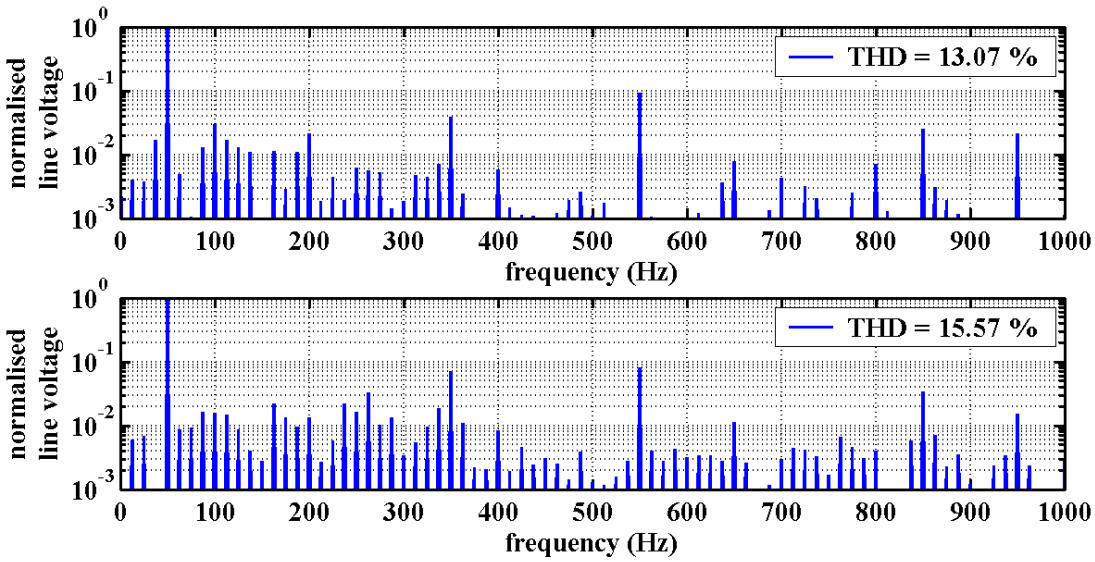


Figure 3.3.18: Line voltage spectrum comparison, PATTERN #1 (top) and regulated capacitor voltage (bottom)

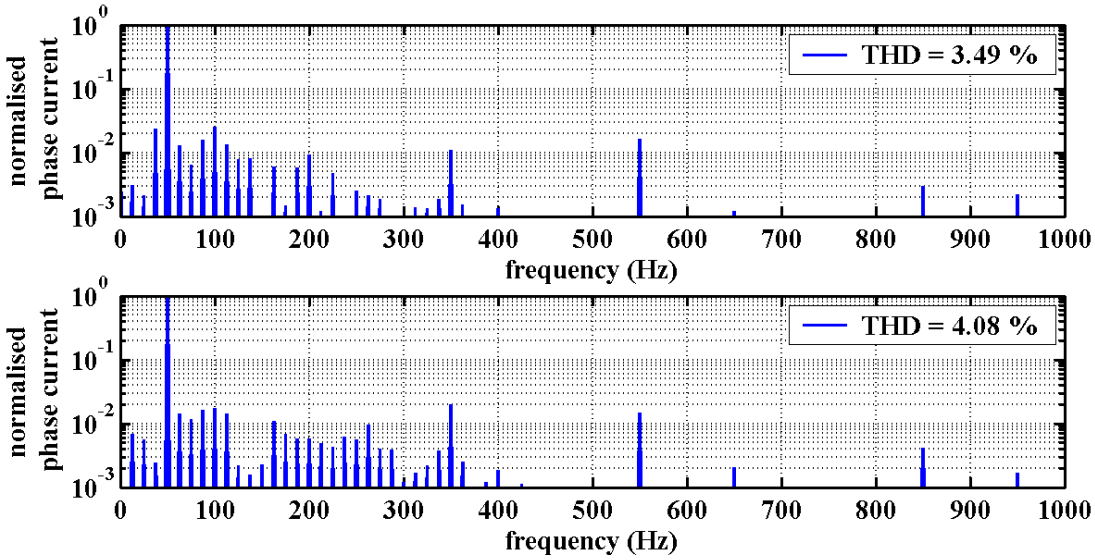


Figure 3.3.19: Phase current spectrum comparison, PATTERN #1 (top) and regulated capacitor voltage (bottom)

3.4 Optimum Cell-Capacitor Selection

Simulation results so far have demonstrated that by optimum balancing pattern selection, and certain load conditions, the line voltage THD will actually be below the theoretical level achievable under the optimum SHE control mode. However, the improvements in performance are at the expense of increased ripple on the cell-capacitor voltages, and higher voltage peaks across the power semiconductor switches. In a real system, a compromise has to be found between safe-operation of

the power switches in terms of maximum voltage blocking capability, reduced capacitor sizing and cost, and the power quality of the load waveforms.

Potential applications of the flying-capacitor inverter cover a wide range of power factor loads. Therefore, it is important to have a standardised capacitor selection methodology. This can be achieved graphically by using the energy factor, ζ, which combines the load characteristic and the cell-capacitance.

3.4.1 Inverter Characteristics

Simulations were run over a matrix of load displacement power factors and system energy factors to obtain the THD and peak blocking voltages for each case. The aim is to provide a set of design characteristics for inverter operation using optimised balancing pattern, staircase SHE4H2 control. These characteristics represent the behaviour for a 50 Hz output fundamental frequency, and therefore are normalised to this frequency. For example, if the output frequency is halved then the energy factor scale has to be halved. The graphs enable the minimum required unit cell-capacitor stored energy to be identified for a target load characteristic.

Figures 3.4.1 and Figure 3.4.2 show the contours of THD expected for varying load DPF and system energy factors. These contours show the predicted harmonic distortion and are specific to operation at a unity m_a demand. The contours for other control modulation depths also show the same trends. It can be seen that the proportion of unwanted harmonics power in the total output power increases as the energy factor is increased. This is especially true in the current harmonic distortion for the linear inductive load. This reflects a decreasing size of capacitor in terms of volume/cost in a real system. This should be expected, but it is important that the behaviour is quantified, so that the inverter design achieves optimal cost versus performance. It can also be seen that the lower harmonic distortion region lies where load displacement power factors are around 0.6 to 0.8. This result is pleasing from the perspective of an inductive type load with lagging current phase angles in the region of 45^o. Symmetry in this performance follows for leading power factors, assuming that the switching pattern is reversed, since the positive benefits of voltage variation by charging/discharging sequence on harmonic reduction do occur during the intermediary voltage synthesis levels.

Figure 3.4.3 shows the variation in phase voltage and current THD as a function of energy factor for three typical displacement power factors. Also plotted is the maximum blocking voltage across any of the power switches in the multilevel inverter under the same conditions. This voltage is the maximum instantaneous difference in voltage of the two adjacent cell capacitors and shows a greater variation than that seen

in the individual capacitor voltages. This is because the capacitor voltages can not be controlled to vary in total sympathy in this type of inverter. Safe-operation under all conditions calls for higher blocking voltage capability in the power devices. The actual selection of power device would be based on other factors as well as blocking voltage. Thermally managed peak operating junction temperatures due to power loss while commutating the target load currents, and margins on the operating points for design system life-times will all play their part in the ultimate device selection.

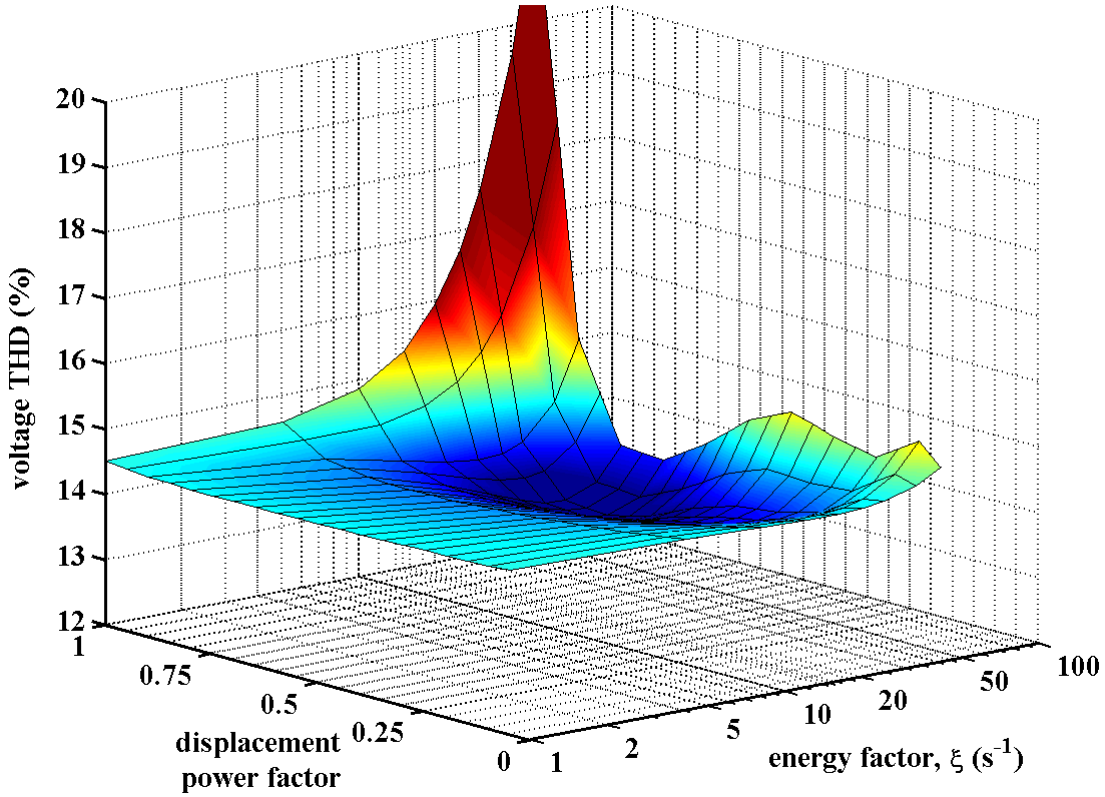


Figure 3.4.1: Contour variation in line voltage THD for different DPF and ξ

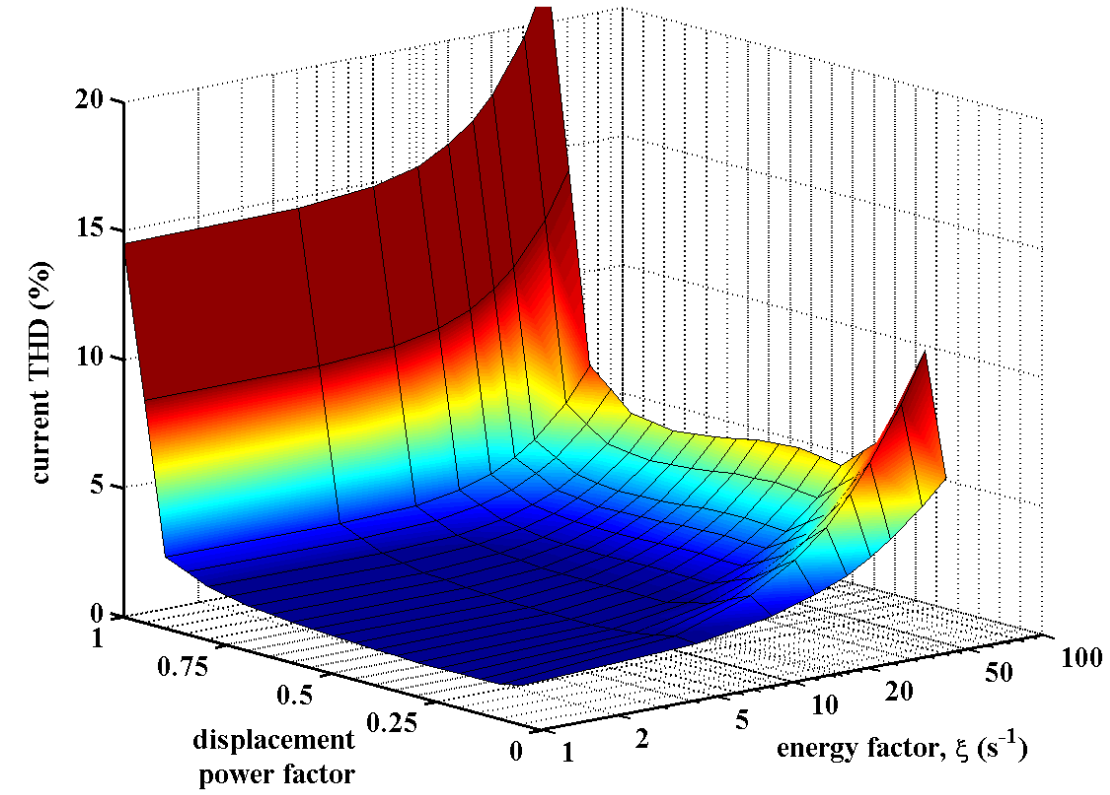


Figure 3.4.2: Contour variation in phase current THD for different DPF and ξ

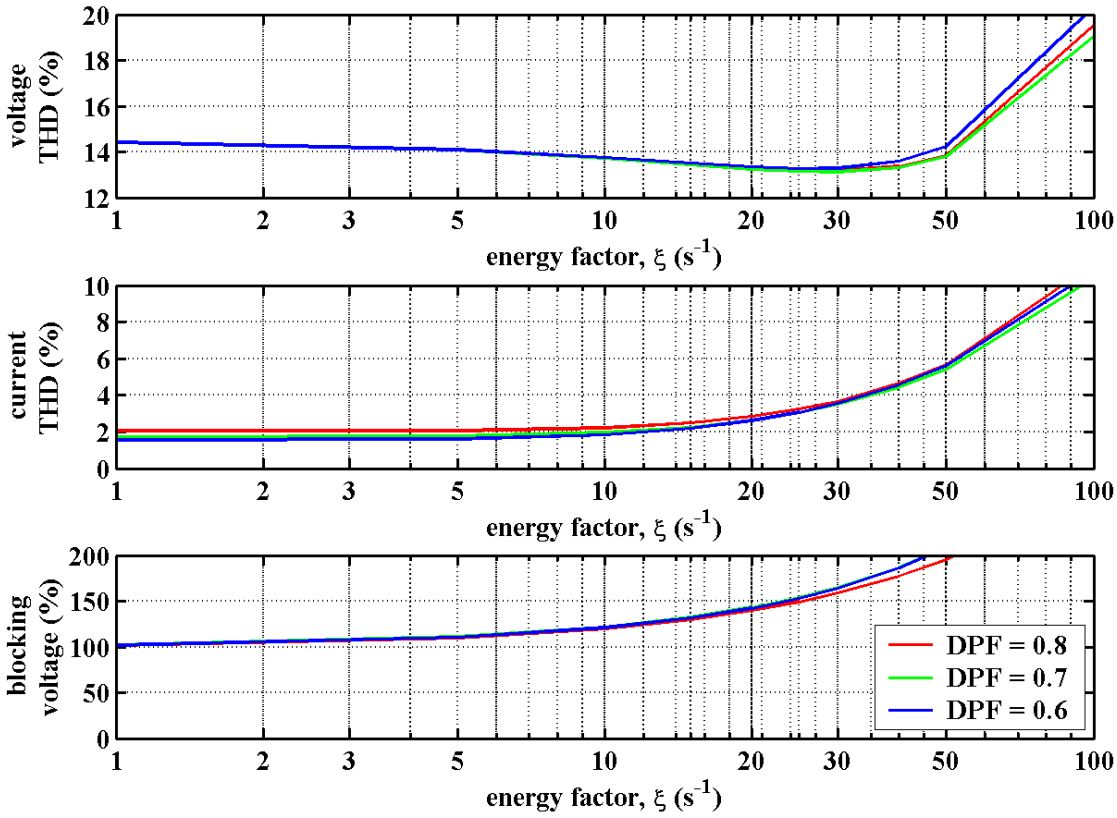


Figure 3.4.3: Variation in voltage & current THD and normalised blocking voltage with respect to the energy factor, ξ

3.4.2 Inverter Design Example

By way of example, the design of a small inverter will be presented in terms of component selection and maximum capability. The inverter is realisable as a working model for a real system and therefore will constitute the experimental tool for verification of the analysis presented in this thesis.

The characteristic contours, Figures 3.4.1, 3.4.2 and 3.4.3, presented in the previous section, can be used to identify the optimum energy factor, ξ, for the inverter for the known load conditions. The energy factor formula (3.4.1), relating the output power as a function of the unit capacitor stored energy, can then be used to select the unit cell-capacitor ratings for the inverter.

$$P = \xi m^2 \cos^2 \phi E_c \qquad \ldots (3.4.1)$$

It is desirable that the inverter is demonstrated on a load exhibiting a lagging power factor in the region of 0.7, typical of a low power induction motor, so an energy factor, ξ, in the range 10 s^{-1} to 50 s^{-1}will offer low output voltage harmonic distortion. With reference to Figure 3.4.3, the maximum allowable peak blocking voltage is to be set at 150% of the unit cell-capacitor voltage. Therefore, ξ should not be greater then 25 s^{-1}.

The operating output frequency is 50 Hz, so there is no need to scale the energy factor. The maximum load power of at about 1.0 kW, so by rearranging the energy relationship (3.4.1), the required energy storage for the four cell inverter (m = 4) can be calculated as follows:

$$E_c > \frac{P}{\xi m^2 \cos^2 \phi} \qquad \ldots (3.4.2)$$

$$E_c > 5.1 \text{ J} \qquad \ldots (3.4.3)$$

On a 400 V dc link, where the unit cell-voltage is 100 V, the required capacitance has to be greater than 1.02 mF in order to avoid excessive voltages across the switches. For the practical inverter, standard rated 1 mF, 200 V capacitors, are readily available and will be used. The power switches will need to cope with a peak voltage of 150 V, but for experimental purposes standard 600 V devices would be desirable since the ripple voltages will be allowed to increase above the design limits used earlier. The IRFGPC30KD, a 600 V, 30 A, IGBT manufactured by International Rectifier, and which incorporates an anti-parallel diode of equivalent rating, is appropriate.

3.5 Steady-State Performance of Simulated Inverter

This section explores, by simulation, the expected performance of the four-cell flying-capacitor inverter design for a requirement to supply a typical 1.0 kW three-phase lagging phase current load. The aim is incorporate the actual system components to be found in the experimental laboratory set-up.

The practical inverter design has four cells per phase and will use 1 mF unit cell-capacitors. An optimised value for ξ of 25 s^{-1} is required for expected load displacement power factors of 0.7 and above in normal operating conditions. This will limit the peak blocking voltage to around 150 % of the nominal cell-capacitor voltage and give good output harmonic quality performance when controlled using optimised SHE and the optimised balancing PATTERN #1.

Therefore, the load parameters for simulation are R = 30 Ω, L = 97.4 mH, which sets the ideal load displacement power factor to 0.7 and gives the optimum ξ. The individual capacitor mean voltages are 100 V with a 400 V dc link. This will result in a maximum theoretical load power of 980 W. The simulator has a library of different power switch models including the IRFGPC30KD IBGT/diode combination selected for the experimental inverter design.

The simulator's iteration time-step is set to 40 ns since the simulated digital control system is clocked at 25 MHz. The four-cell inverter limb requires four 50 Hz cycles before repeating the firing balancing pattern, so the performance results are processed from 32768 data samples taken over an 80 ms period.

3.5.1 Overall Inverter Performance

The simulated steady-state operating electrical performance of the system when the control demand is a 50 Hz, 141.42 V_{rms} per phase leg (m_a = 1 at 400 V dc link) is summarised in Table 3.5.1. The fundamental voltage is slightly higher than the ideal demand, but lower than the ideal lossless system case. This shows that voltage drops in the semiconductors off-set modulation errors caused by capacitor voltage ripple. This is an important point to note when designing a voltage control loop for the system. The voltage and current waveforms for the inverter are shown in Figure 3.5.1. These illustrate well-balanced behaviour over a four-cycle period (80 ms), and it is of interest that there is a noticeable 12.5 Hz component present in the star-point voltage of the load with respect to the 0 V neutral voltage of the overall system.

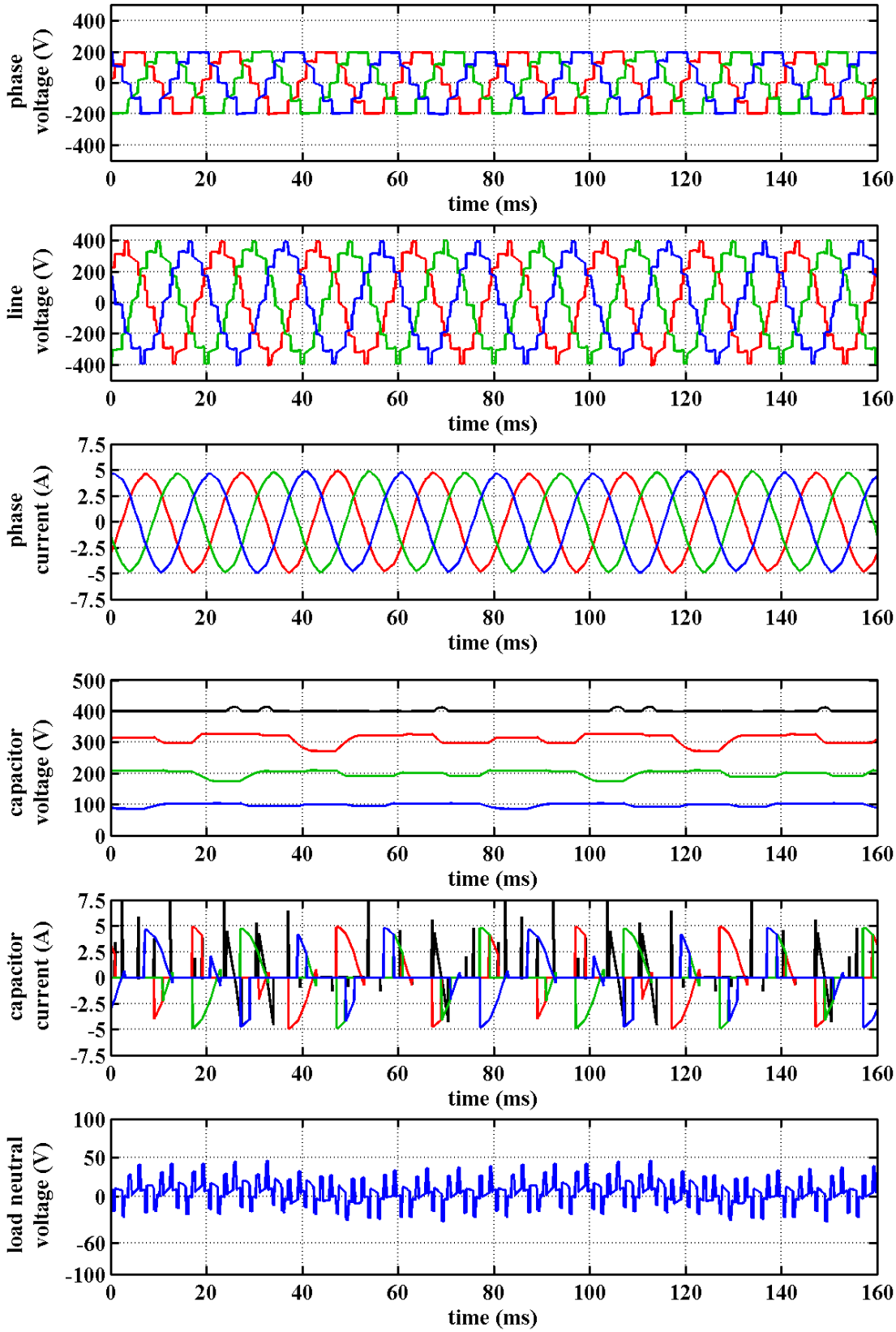


Figure 3.5.1: Operating waveforms for simulated inverter, load DPF = 0.7

Electrical Parameter	Computed Result
Phase voltage	144.55 V_{rms}
Phase current	3.32 A_{rms}
Line voltage	248.61 V_{rms}
Input power	1032 W
Output power	993 W
Total electronics loss	39 W
Efficiency	96.2 %
True power factor	0.690
Fundamental	142.15

Table 3.5.1: Simulated electrical performance of system

The internal operating data for the inverter is also simulated so that device ratings can be assessed. Table 3.5.2 lists the key voltage parameters of the inverter cell capacitors. The peak voltage for an individual capacitor in each cell assumes that voltage sharing is perfect. In a real system, the capacitor reliability would have a significant influence on the life-time of the whole inverter, and life-time expectancy is related to the peak operating voltage and operational current. The third plot from the top in Figure 3.5.1 shows the variation in capacitor voltages for all capacitors normalised to the same common voltage.

	C1	C2	C3
Mean voltage (V)	95.0	196.3	307.9
Individual capacitor peak voltage (V)	100.2	103.6	108.1
Ripple current (Arms)	1.74	1.76	1.77

Table 3.5.2: Capacitor operating conditions

The electronic losses are 1.26 W and 0.35 W for the individual IGBTs and anti-parallel diodes respectively. There are no significant switching losses, (< 10 mW) calculated by energy summation at switching transitions under these operating conditions of a 400 V dc link and at 50 Hz fundamental. The maximum voltages seen by each switch when in the blocking state are 100.2 V, 124.2 V, 152.6 V and 130.5 V, in order of the complimentary switch pair nearest the load. The maximum peak is around the target maximum (150 V), and predicted for the operating load power factor and ξ values.

3.5.2 Output Waveform Harmonic Distortion

The THD of the line voltage is 13.22 %, compared to 14.52 % for the theoretical ideal staircase voltage waveform and is a result of the optimal of balancing pattern selected for control. The current THD is above the theoretical ideally achieved value, but at 2.98 %, below internationally defined limits. A significant 8.12 V peak at 100 Hz harmonic is present in the line voltage in addition to the first major peak of 13.89 V at the fundamental's 7th harmonic frequency. Figure 3.5.2 and 3.5.3 show the harmonic spectra of the line voltage and phase currents produced by the simulation. As can be seen, the filtering effect of the load on the current reduces high-order harmonics, masking the 100 Hz the most significant frequency component after the 50 Hz fundamental.

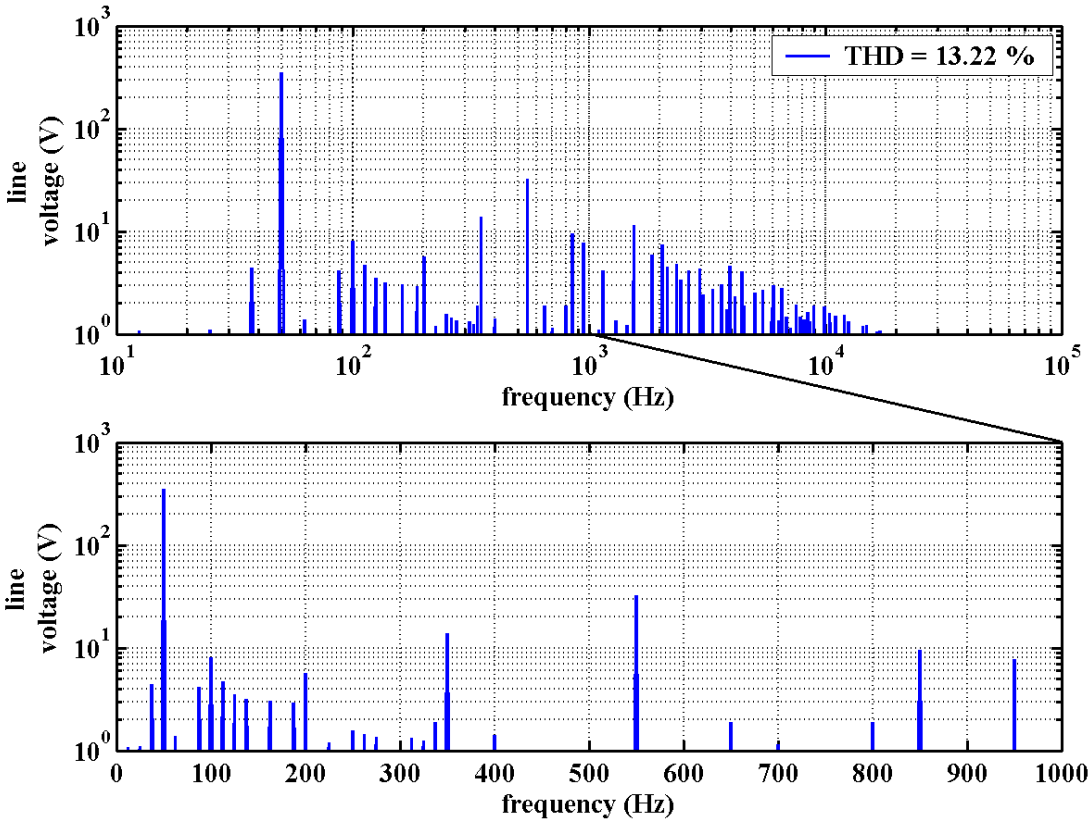


Figure 3.5.2: Line-voltage spectrum, 50 Hz fundamental, m_a = 1.0

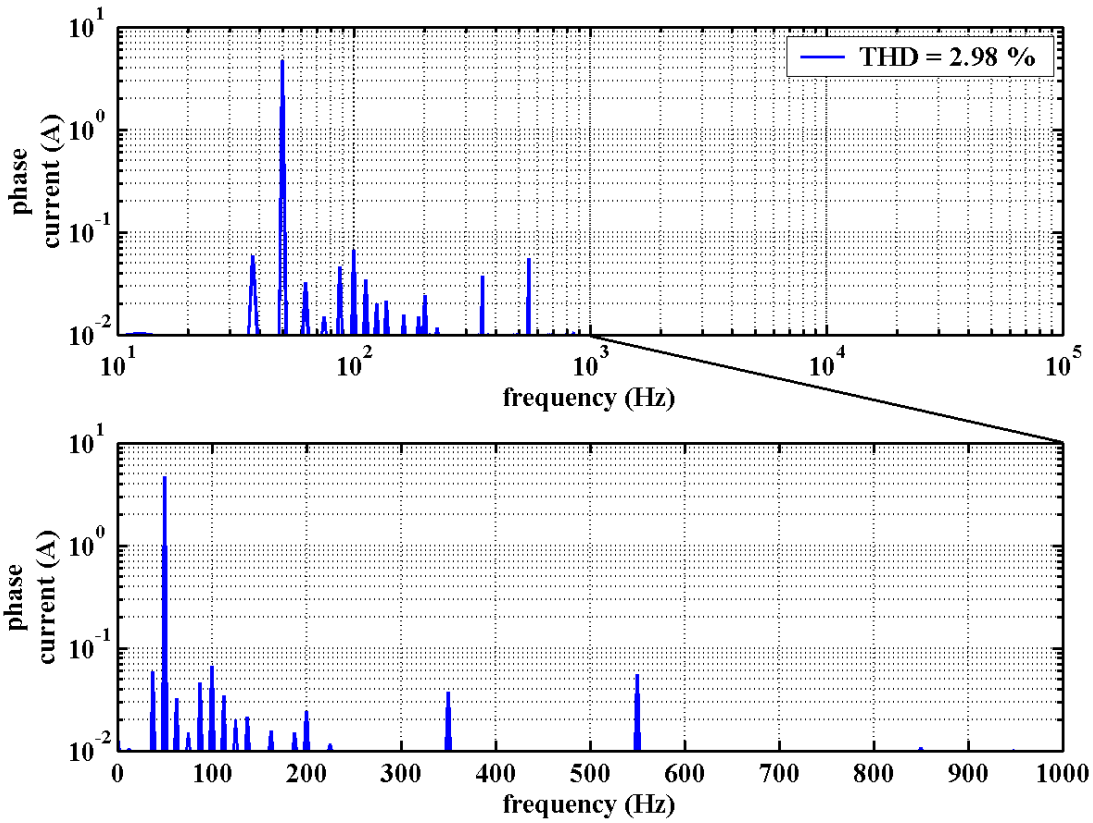


Figure 3.5.3: Phase-current spectrum, 50 Hz fundamental, m_a = 1.0

There is a slight difference in the computed line voltage THD, 17.71 % compared to 17.31 %, when the IGBTs are included in the simulation. This is attributable to the difference in conduction voltage characteristics of diodes and IGBTs. If they were both equal, then the effect would be a small percentage reduction in the amplitude of the phase voltage, but no change in relative harmonic content. The voltage difference in the conduction paths when positive and negative load currents flow, leads to a small voltage in-phase with the current being present in the phase voltage. When the current is positive, the output voltage is lower than the ideal case and higher when the current is negative.

This ac voltage contribution can be seen more clearly if the simulation waveform with device models included is subtracted from a lossless switch modelled waveform under the same conditions, as shown in Figure 3.5.4. At any instant, there only four devices in conduction and could be any combination of diodes or IGBTs depending on the current path through the inverter cells. The inherent square wave adds odd harmonics to the overall line-voltage frequency spectrum, and a net unwanted contribution in the rms of 0.4% of the fundamental. When the relative difference between the semiconductor switch's conduction voltage drop and dc link voltage increases, then this effect will diminish.

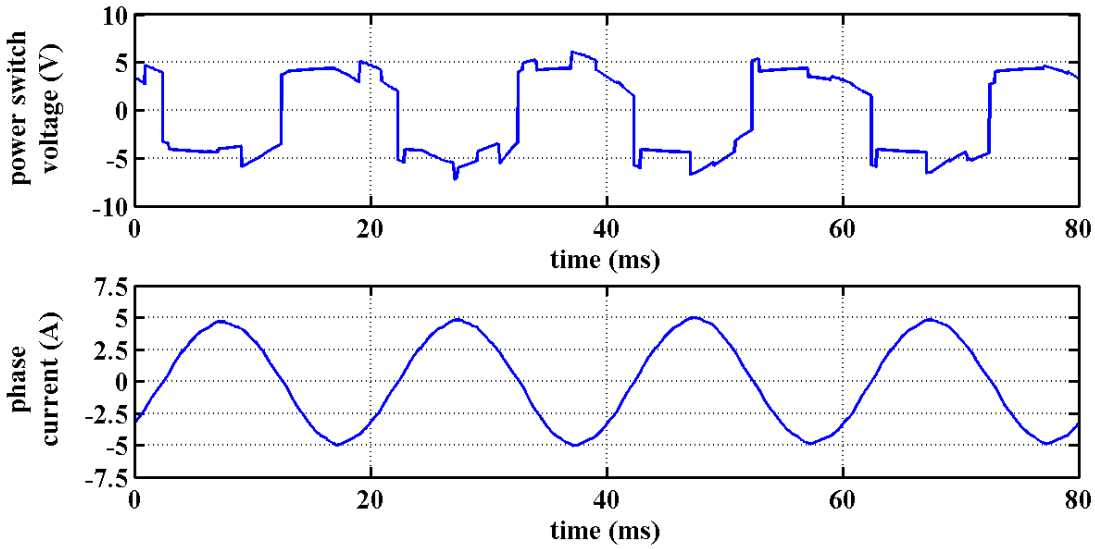


Figure 3.5.4: Electronics voltage drop and phase current

3.5.3 Performance Over Whole Modulation Range

Finally, the performance over the range of output voltage demand is investigated. At lower modulation index levels, the safe operation of the inverters capacitors and semiconductors is not an issue, but good regulation of output voltage and power quality is still expected. Figures 3.5.5 and 3.5.6 show the variation in THD for the output waveforms as a function of demanded voltage level. As can be seen the distortion increases with lower m_a, as expected. Reasonable levels of phase current harmonic distortion are demonstrated for a four-cell inverter with optimised balancing pattern SHE-4H2 control is possible for $m_a > 0.4$.

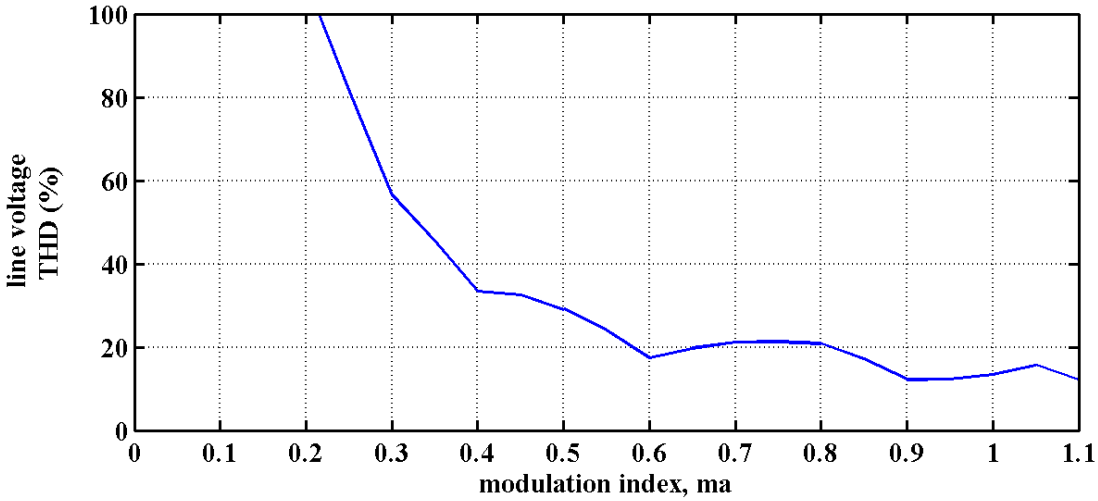


Figure 3.5.5: Line voltage THD variation over modulation demand

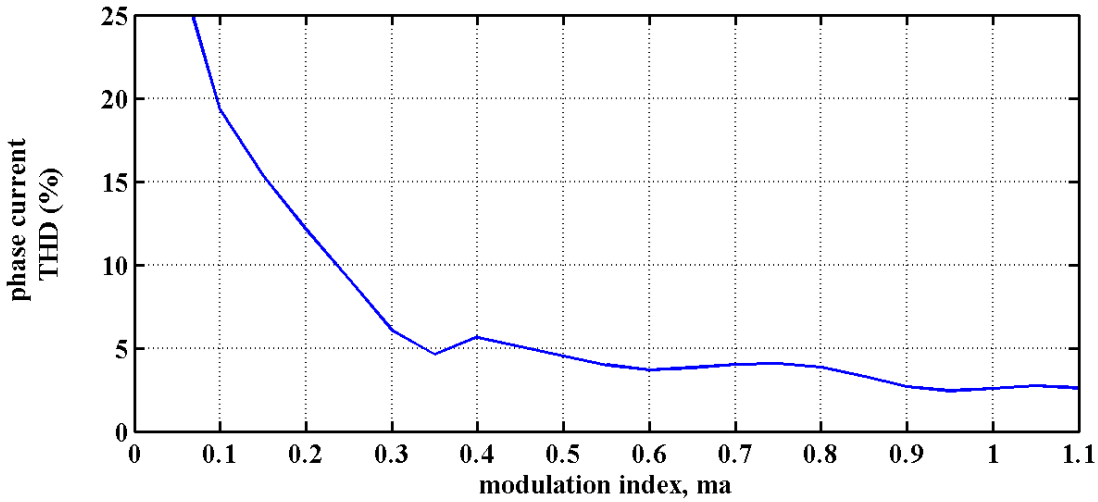


Figure 3.5.6: Phase current THD variation over modulation demand

Under open-loop conditions, the demanded voltage versus actual output voltage characteristic will inevitably exhibit non-linear characteristics. The deviation away from an ideal straight line has to have a low gradient in order to make a control loop design simple, such as the classic PI controller. To ascertain any problems, the error in actual fundamental amplitude against m_a demand is shown in Figure 3.5.7. This shows that the variation is continuously differentiable with no sudden changes in gain above sensible output levels, and the actual error is dominated by the voltage drop introduced by the semiconductor switches.

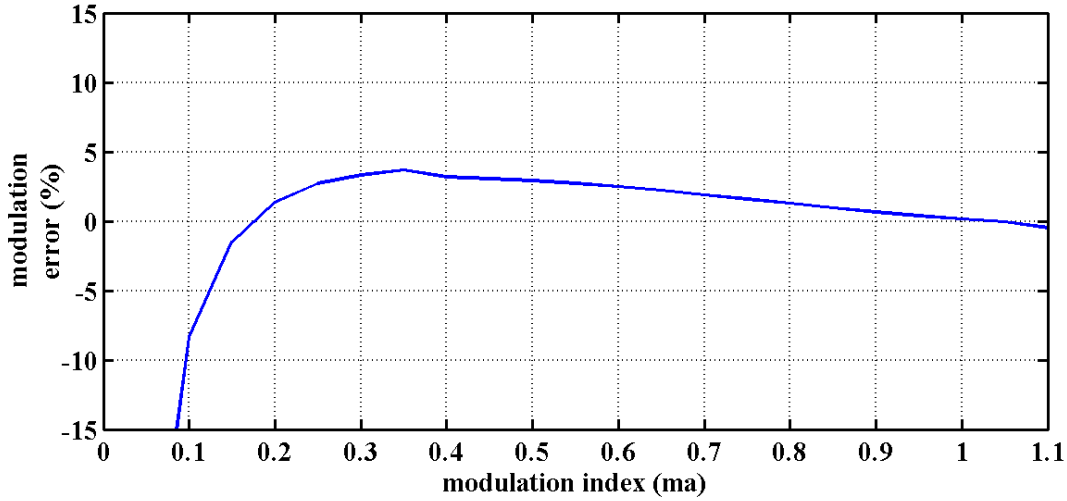


Figure 3.5.7: Error in fundamental amplitude

3.6 Transient Performance of Inverter

Various transient conditions are possible in a real system. The main changes in operating conditions which could have a bearing on operation and especially cell-capacitor voltage balancing are transients which cause the load current to change. Variations in the input voltage, variations in load and changes to the demanded output operating voltage will all lead to transients in the inverter. This section aims to explore any possible issues arising from these transient conditions.

3.6.1 Effect of DC Link Voltage Changes

The worst case transient conditions for the inverter are rapid changes in dc link voltage. To test behaviour under these conditions, the simulated voltage source is turned on and off. This produces a sudden rise in dc link voltage for a step-up condition, but allows energy transfer stabilisation to occur when the voltage is removed. In reality, a step-up transient on the dc link would be far more benign than simulated, due to natural or forced limitation on the dc link charging current. A step-down transient is akin to a power failure, and so is a valid indication of behaviour.

3.6.1.1 Balancing Pattern Control Behaviour

The effect of a dc link voltage transient on the inverter's cell-capacitor voltages is shown in Figures 3.6.1 and 3.6.2. These show that the 'open-loop' balancing pattern control method cannot cope with significant input voltage deviations in a controlled and fault-free manner. The behaviour under transient application of dc link voltage is safely controlled, but the system time-constant is significant. When the dc link source is removed, the upper capacitors collapse inwards to the lower capacitor voltages. The cell-capacitor/load time-constant dictates the rate at which the energy in the capacitors is transferred to the load. Potentially, failures can occur since there can be a short-circuit path through the bottom transistor and top diode when the outer cell-capacitor's voltage is much lower than the inner at the point of cell-commutation. This type of failure has been investigated by researchers at Toulouse [3.12].

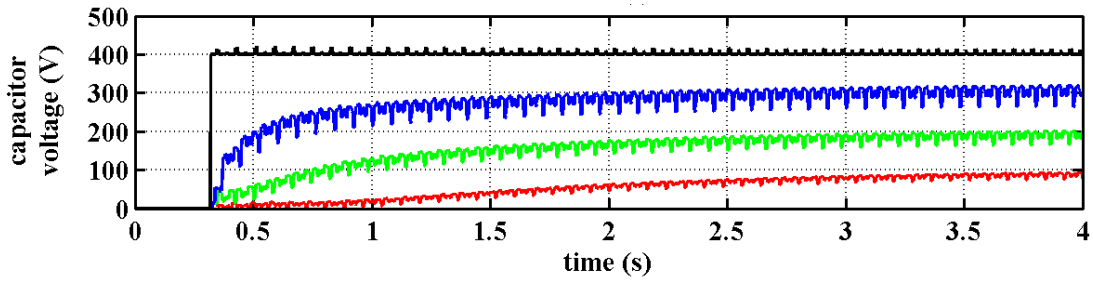


Figure 3.6.1: Step-up dc link transient, 50 Hz fundamental, m_a = 1.0

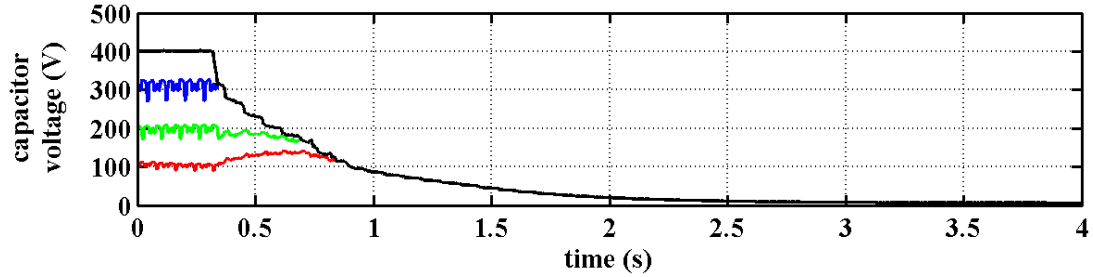


Figure 3.6.2: Failure of dc link transient, 50 Hz fundamental, m_a = 1.0

3.6.1.2 Improved Control of Cell-Capacitor Voltage Balancing

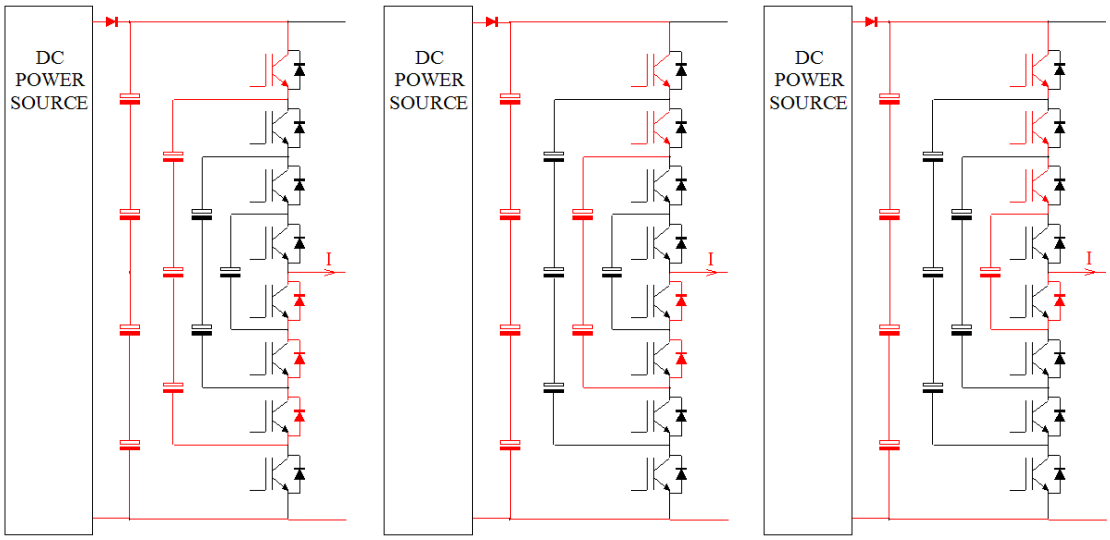
To improve performance, a certain degree of *a priori* knowledge is required in the control, and most importantly feedback signals indicating the capacitor voltage states. Clearly, under transient dc link voltage conditions, the requirement should be for the inverter's internal electronic switch maximum voltages not to exceed a clearly defined maximum. Therefore, the optimum outcome of an input voltage transient is to have the capacitor voltages track the direction change in dc link voltage, and keep a 'balanced' separation. This will ensure that peak voltages across the switches in the off state are minimised.

To enforce controlled behaviour under transient dc link conditions, voltage comparator feedback of each cell-capacitor voltage is required. Then the approach adopted must control the inverter switches in a sequential manner which transfers energy from each cell capacitor bank in harmony with each applied voltage level. This will lead to the required bucking/boosting of the adjacent capacitor towards the stable state. By analysis of the inverter's switching states, the required control switching states are listed in Table 3.6.1 for all conditions.

Voltage Level	Undervoltage Condition		Overvoltage Condition	
	I < 0	I >= 0	I < 0	I >= 0
25 %	0001	1000	1000	0001
50 %	0011	1100	1100	0011
75 %	0111	1110	1110	0111

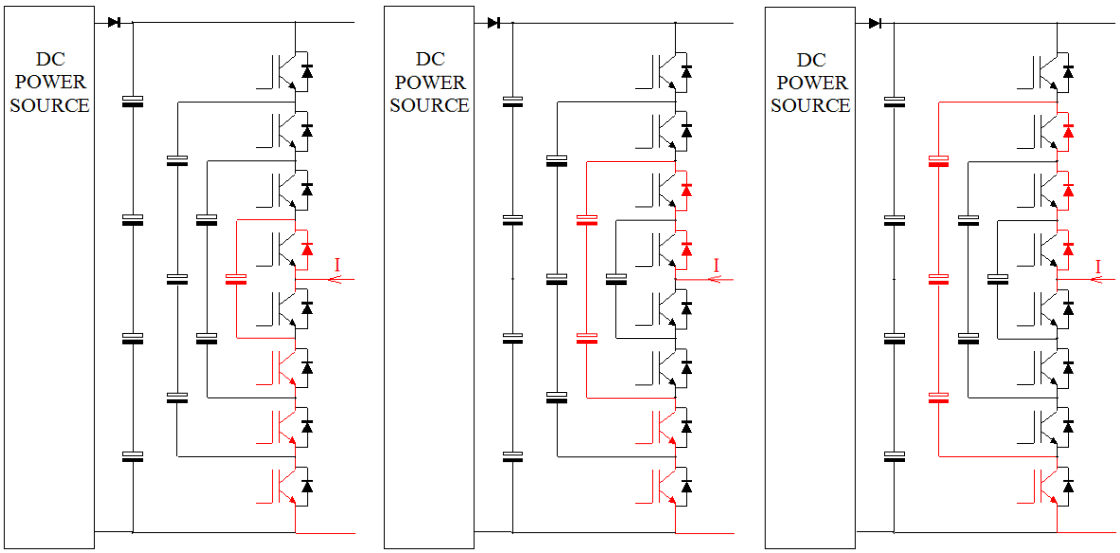
Table 3.6.1: Switching states for optimum capacitor bucking/boosting

Figures 3.6.3 and 3.6.4 illustrate that the current flow when the capacitor voltages need to be boosted. The system control will override normal operation and apply these rules, thus forcing the capacitor voltages towards their equilibrium states. Once the voltage returns to within a specified hysteresis band, set to be outside the steady-sate peaks and troughs in the capacitor voltage, the sequence reverts to the optimum balancing pattern, PATTERN #1.



a) 25 % Voltage (1000) **b) 50 % Voltage (1100)** **c) 75 % Voltage (1110)**

Figure 3.6.3: Capacitor voltage boosting states when phase current is positive



a) 25 % Voltage (0001) **b) 50 % Voltage (0011)** **c) 75 % Voltage (0111)**

Figure 3.6.4: Capacitor voltage boosting states when phase current is negative

In the flying-capacitor inverter, the combination of the actual capacitor voltages on the synthesised output voltage in intermediary level modes has an effect on the phase current, which in turn affects the charging of an individual capacitor if it is in the current path. Also the timing when controlled with the SHE angles is different at each level. This means that the capacitors will charge at different rates. Therefore, the best approach is to monitor only one of the capacitor voltages and to use the voltage condition for deciding when to change operation to this transient mode.

Prior to a source voltage failure, the capacitors will be properly balanced. Once the input source is removed, if nothing is done, then outer-cell voltages will decay quite quickly, leading to potentially a large voltage differential across the cell semiconductors. Therefore, the obvious way to control the inverter in this situation is to use the voltage level information from the outer cell capacitor and then force bucking of all capacitors, so that the voltages, including the dc link through re-charging, will decay in a far more controlled manner. The same thinking can be applied to when a sudden step-down change in dc link voltage occurs, but in this case the inner capacitor should be used to dictate the boosting mode. In reality, it is unlikely that the dc link voltage will suddenly change like that, since it implies an infinite input current source.

When this control scheme is simulated, the resultant transient waveforms are shown in Figures 3.6.5 and 3.6.6. It should be noted that under these conditions, no attempt is made at modifying the voltage control, and the inverter uses the pre-computed angles for m_a = 1. When the dc link voltage is stepped-up, the capacitor voltages reach their

steady-state values in roughly a third less time than in the uncontrolled case, thus limiting the duration of the transient affect on the load. The time taken for the capacitor voltages to decay is also far quicker, whilst maintaining a positive differential between the outer and inner cell-capacitor voltages in each case.

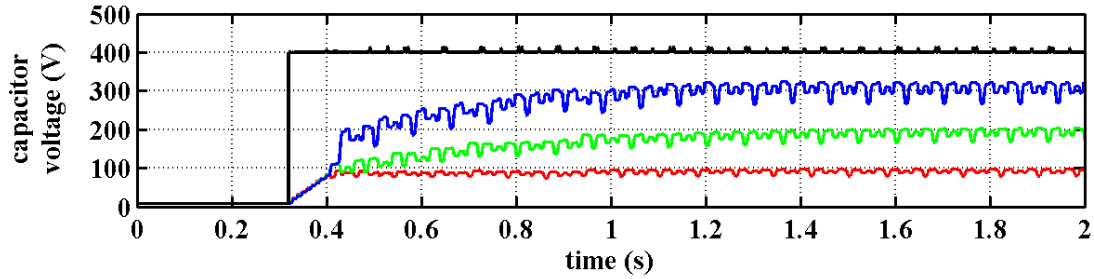


Figure 3.6.5: Step-up dc link transient, 50 Hz fundamental, m_a = 1.0

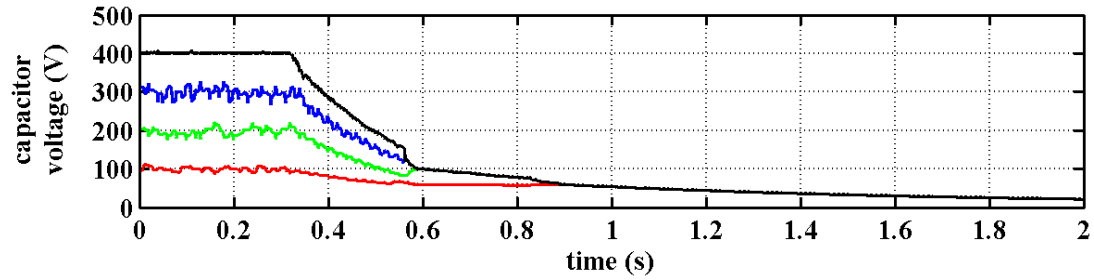


Figure 3.6.6: Failure of dc link transient, 50 Hz fundamental, m_a = 1.0

3.6.2 Load Transient Behaviour

To investigate any possible operating problems for the inverter when the load characteristics transiently change, simulations were performed on a stepped load. The load power was changed from 10 % to 100 % of the maximum rated power and back again. The full power load parameters were set to 38.4 Ω and 91.7 mH giving a 1 kW with DPF = 0.8. The low power load was set by changing the resistance to 600 Ω while keeping the inductance the same. The control settings were kept constant at m_a = 1 and f_1 = 50 Hz.

Figure 3.6.7 shows the resultant inverter system waveforms when there is a transient in the load electrical characteristics. It can be clearly seen from the simulations that there is no requirement for any further control to optimise performance, since there is very little disturbance in the cell-capacitor and dc link voltages. This is because the value of cell-capacitance required to ensure safe operation and low voltage ripple is specified for the maximum charging/discharging current at full load. If the load

characteristic were to lead to excessive current, such as a shorted load, then additional measures would be required to protect the inverter.

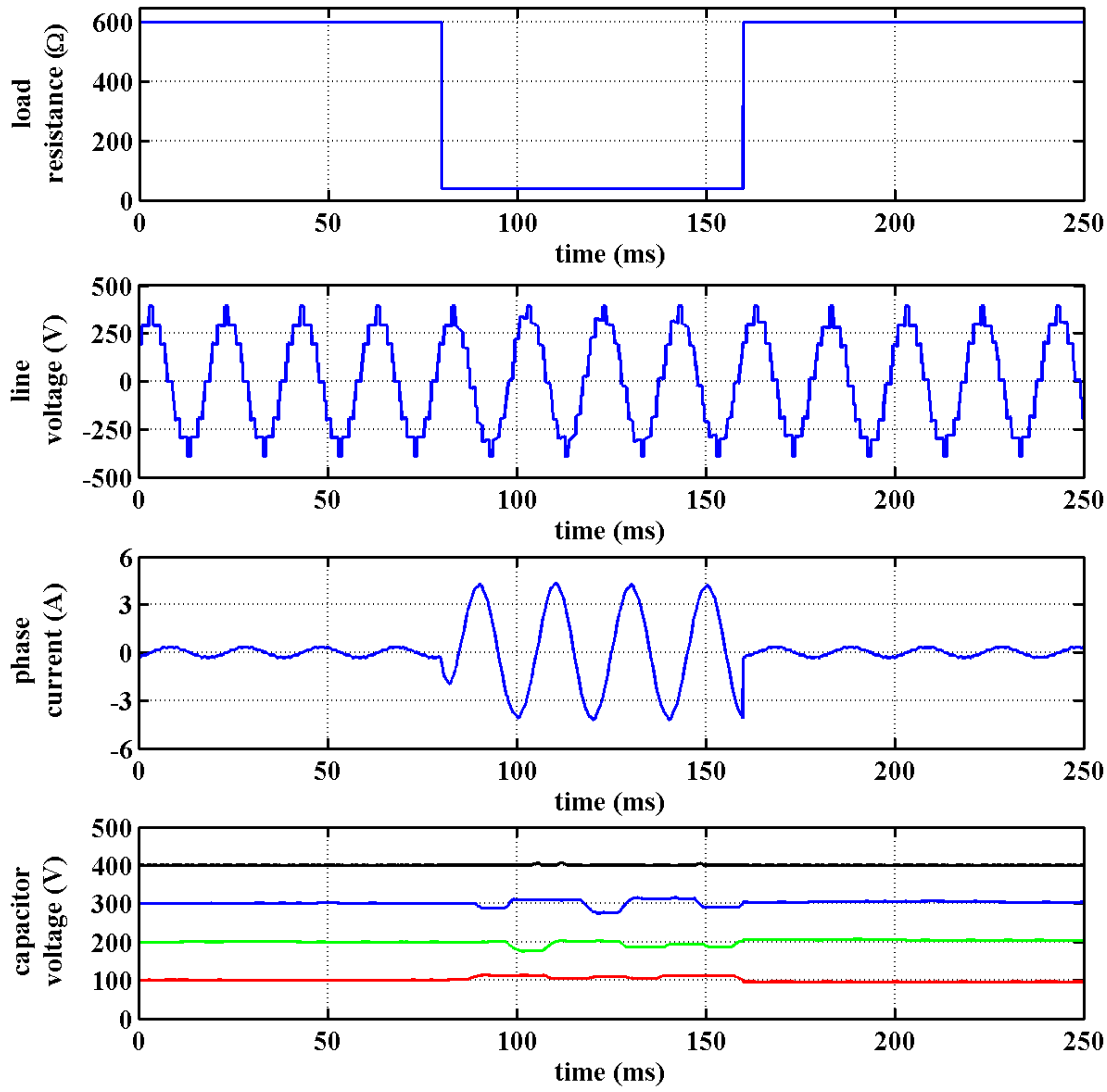


Figure 3.6.7: Output waveforms and capacitor voltages for load transient

3.6.3 Control Voltage Demand Variations

Simulation of a transient step in demanded output voltage will reveal any possible inverter issues which will have to be taken into account when designing a voltage feedback control-loop for the whole system of inverter and load. For these simulations, the modulation index, m_a, is stepped from 0.1 to 1.0 and back again. In practice, this would not be seen as a sudden step but would be more gradual, reflecting the dynamics of the voltage loop in a closed loop system. It is useful, however, in identifying any issues within the safe operation of the inverter when controlled by an

external control system. The load in this case is fixed to 1 kW and a lagging 0.8 power factor.

Figures 3.6.8 shows the effect of this stepped demand on the output voltage and current waveforms of the inverter. The cell-capacitors are also shown, and reveal that there is no noticeable deviation away from the nominal balanced levels. In the case of the step-down demand transient, the capacitor voltages remain at the levels they were at the moment at which the demand was reduced, and will remain so for a considerable period, or until a larger load current flows because of an increased voltage demand or load change. In the case of the step-up voltage demand transient, there is a slight transient change in the mean voltages but it is masked by the ripple voltage component.

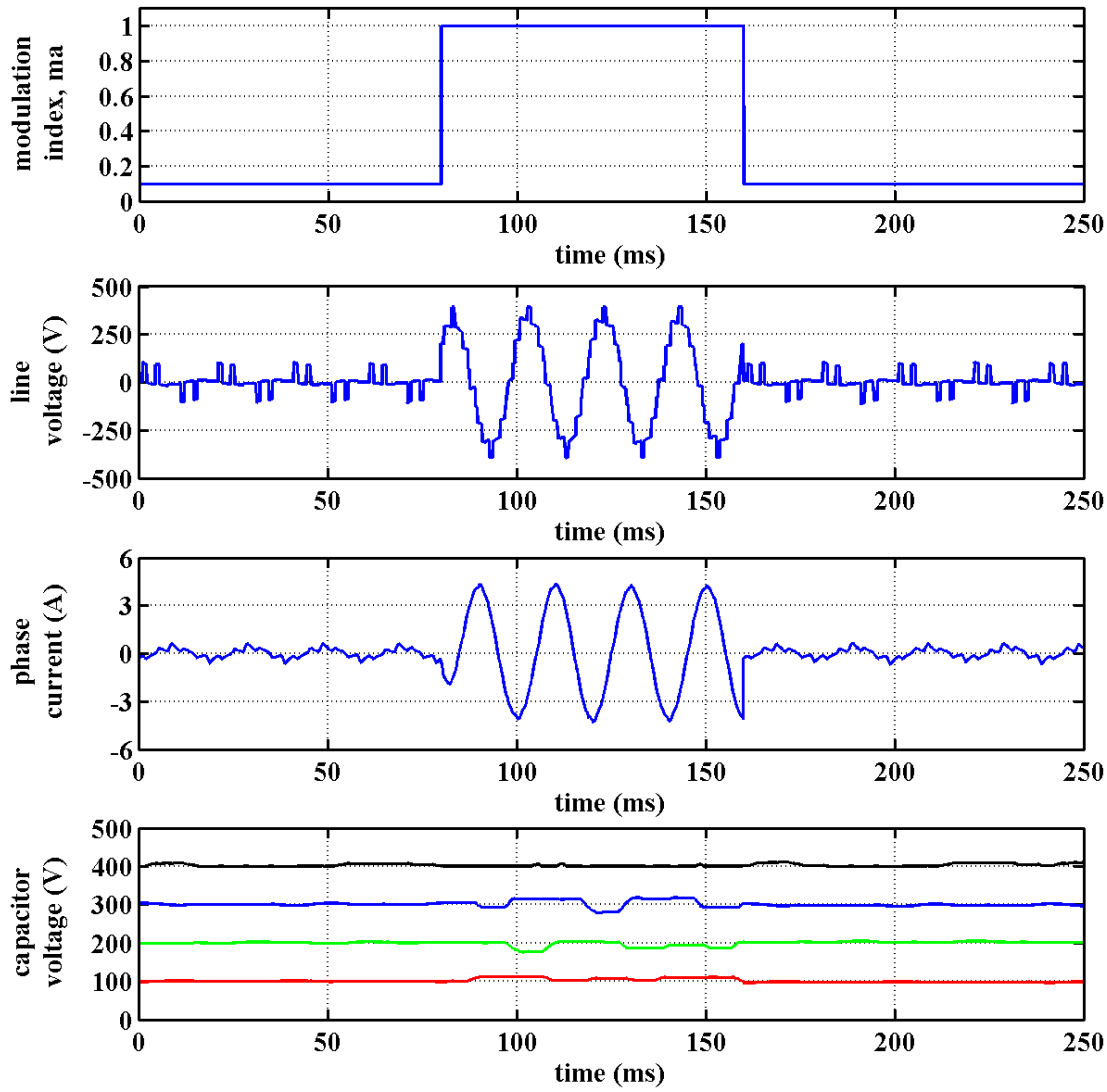


Figure 3.6.8: Output waveforms and capacitor voltages for transient demand voltage

These results suggestion that even with an open-loop voltage balancing strategy for staircase SHE control, there is no complex requirement made on any external voltage control loop.

3.7 Conclusions

This chapter has presented the results of the investigation, using the simulator as a tool, into the behaviour and optimal control of a four-cell, three-phase flying-capacitor inverter when operated with low commutation frequency selective harmonic elimination modulation. To aid comparison and for system optimisation, the energy factor term, ξ, has been used which normalises the system power equation in terms of cell-capacitor stored energy and load DPF. This is a very useful parameter which can be applied to different level number flying-capacitor inverters and other control strategies. It is also possible to compare other multilevel inverters using this term, since it sets the maximum limit of performance for a given size of capacitor.

The concept of an open-loop pattern based balancing strategy has been introduced, and shown to work well under steady-state operating conditions. It has also been shown that pattern selection is very important in optimising output power quality and maximising the power range for a given set of inverter components. Simple rules have been identified to optimise the pattern, and they are shown to hold true for every possible balancing patterns. The methodology for selecting switching states for the inverter when voltage monitoring is available is shown to offer some improvements in terms of increased output power and harmonic distortion in the load current.

The analysis of optimal balancing pattern has led to the identification of sets of normalised design surface plots to aid design of real inverters. This allows a design to be produced based around a unit cell capacitor, and its maximum performance identified. Analysis by simulation of the performance of the optimal inverter design using a realistic power switch model, confirms that design meets the intended specification.

Further simulation has been conducted on various transient scenarios and the effect on performance and safe operation analysed. This has shown that behaviour is fairly well controlled using the sensorless voltage balancing strategy in most cases. However, it has been shown that to improve behaviour of the capacitor voltage transition to a balanced state under severe dc link transient conditions, observation of the capacitor voltages is required, and the control switching patterns adjusted accordingly.

Overall, a SHE scheme offers the possibility to achieve low output current distortion, and if applied to an active bridge rectifier, levels of distortion below the required international standards, without very large capacitors. This mode of control is best

suited to very large, medium to high voltage systems or very high speed machine applications, where switching losses in the electronics are significant. This is because the capacitor sizes are significant for the required levels of storing energy in the system to maintain proper operation. This is due to SHE control being primarily a low frequency operating scheme with each switching state occurring for a significant proportion of the overall synthesising period. Another possible application of a flying-capacitor inverter operating under SHE modulation control would be for a very high frequency power amplifier using many levels.

3.8 References

[3.1] Turnbull, F.G., "Selected harmonic reduction in static d-c – a-c inverters", IEEE Transactions on Communications and Electronics, Vol. 83, July 1964, pp. 374 – 378.

[3.2] Patel, H.S. and Hoft, R.G., "Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part I – Harmonic elimination", IEEE Transactions on Industry Applications, Vol. IA-9, No. 3, May/June, 1973, pp. 310 – 317.

[3.3] Patel, H.S. and Hoft, R.G., "Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part II – Voltage control technique", IEEE Transactions on Industry Applications, Vol. IA-10, No. 5, September/October, 1974, pp. 666 – 673.

[3.4] Nabae, A., Takahashi, I. and Akagi, H., "A new neutral-point-clamped PWM inverter", IEEE Transactions on Industry Applications, Vol. IA-17, No. 5, September/October, 1981, pp. 519 – 523.

[3.5] Sirisukprasert, S., Lai J.-S. and Liu, T.-H., "Optimum harmonic reduction with a wide range of modulation indexes for multilevel converters", Conference Record of IAS 2000, the IEEE Industry Applications Society 35th Annual Meeting, October, 2000, Vol. 3, pp 2094 – 2099.

[3.6] Enjeti, P. and Lindsay, J.F., "Solving nonlinear equations of harmonic elimination PWM in power control", IEE Electronic Letters, Vol. 23, No. 12, June 1987, pp. 656 – 657.

[3.7] Chiasson, J.N., Tolbert, L.M., McKenzie, K.J. and Du, Z., "A unified approach to solving the harmonic elimination equations in multilevel converters", IEEE Transactions on Power Electronics, Vol. 19, No. 2, March 2004, pp. 478 – 490.

[3.8] Agelidis, V.G., Balouktis, A. and Balouktis, I., "On applying a minimization technique to the harmonic elimination PWM control: the bipolar waveform", IEEE Power Electronics Letters, Vol. 2, No. 2, June 2004, pp. 41 – 44.

[3.9] Wilkinson, R.H., Meynard, T.A., Richardeau, F. and Enslin, J.H.R., "Dynamic control and voltage balance of multilevel converters: large signal one-cycle response", Proceedings of EPE '99, 8th European Conference on Power Electronics and Applications, Lausanne, France, 7 - 9 September, 1999,

[3.10] Escalante, M.F. and Vannier, J.-C., "Direct approach for balancing the capacitor voltages of a 5-level flying capacitor converter", Proceedings of EPE '99, 8th European Conference on Power Electronics and Applications, Lausanne, France, 7 - 9 September, 1999,

[3.11] Hamma, F., Meynard, T.A., Tourkhani, F. and Viarouge, P., "Characteristics and design of multilevel choppers", PESC '95 Record, 26th Annual IEEE Power Electronics Specialists Conference, 18 - 22 June, 1995, Vol. 2, pp. 1208 – 1214.

[3.12] Richardeau, F., Baudesson, Ph and Meynard, T.A., "Failures-tolerance and remedial strategies of a PWM multicell inverter", Proceedings of PESC 2000, IEEE 31st Annual Power Electronics Specialists Conference, 18 - 23 June, 2000, Vol. 2, pp. 649 - 654.

Chapter 4 SINE-TRIANGLE PWM

4.1 Introduction

Pulse width modulation control is the most widely used method of controlling the modulation depth of inverters, including the multilevel family. A significant amount of research has been published on the various ways of implementing PWM control [4.1 - 4.3]. The focus here is on carrier-based sinusoidal PWM schemes for controlling a flying-capacitor multilevel three-phase inverter.

The main aim of this investigation is to ascertain which of the large number of possible implementations of multilevel sine-triangle PWM is the optimum for a flying-capacitor inverter, using models of a practical implementation to help simulate as accurately as possible the complete system's performance. The aim is also to develop a balancing control scheme applicable to all forms of PWM control. The four-cell, three-phase inverter adopted for the investigation by simulation is used to compare the different forms of carrier placement strategy, and allows a direct comparison with the SHE control scheme discussed in Chapter 3.

Another major aim is to identify the maximum energy factor for a PWM controlled flying-capacitor inverter. In this case, the issue of peak capacitor voltage will be related to switching frequency and so a modified form is proposed.

The first section explores the different forms of multilevel sine-triangle PWM and bench-marks their performance under ideal system conditions. The balancing of the cell-capacitor voltages is then addressed and a practical implementation developed. The key performance indicators are investigated for different load parameters and system energy factor, in order to establish a practical design guide for the selection of the unit cell-capacitance. Also from a practical implementation perspective, the effect of switching frequency, digital control timing and shoot-through avoidance dead-time are the main issues addressed. The behaviour of the inverter with real switch models is addressed in the final stages of this chapter with a view to comparison with measurements on an experimental inverter. The different forms of carrier placement implementations are then compared by simulation.

4.2 Multilevel Carrier PWM Schemes

There is a wide variety of subtly different ways of implementing PWM. Massoud et al. have published a comprehensive review of the various known techniques [4.4]. In

general, the majority of control schemes involve a triangular carrier signal which is compared to a reference, normally a sinusoid, and the resultant digital signal used to drive the switches accordingly. Schemes involving saw-tooth (asymmetric) carriers are not normally employed in ac systems, but are the norm in switched mode power supplies and other forms of chopper.

Fourier series analysis of the periodic voltage spectrum produced by a carrier based PWM scheme reveals that it has the general form

$$\begin{aligned} v(t) = & \frac{a_{00}}{2} \\ & + \sum_{n=1}^{\infty} \left[a_{0n} \cos\left(n\omega_1 t\right) + b_{0n} \sin\left(n\omega_1 t\right) \right] \\ & + \sum_{m=1}^{\infty} \left[a_{m0} \cos\left(m\left(\omega_c t + \theta_c\right)\right) + b_{m0} \sin\left(m\left(\omega_c t + \theta_c\right)\right) \right] \\ & + \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \left[\begin{array}{l} a_{mn} \cos\left(m\left(\omega_c t + \theta_c\right) + n\omega_1 t\right) \\ + b_{mn} \sin\left(m\left(\omega_c t + \theta_c\right) + n\omega_1 t\right) \end{array} \right] \end{aligned} \quad \ldots (4.1.1)$$

The first term is the dc offset. The second term is the reference fundamental component and its harmonics, index n, and normally referred to as base-band harmonics. The third term is the carrier harmonics, index m, and includes the phase shift θ_c with respect to the fundamental. The fourth term is the sideband harmonics produced by the modulation which will be concentrated around the carrier frequency component and its harmonics. For completeness, the fundamental angle term would also include a phase shift component, and this is required when using this equation for analysis of a three-phase system.

In modern lower power inverters, the switching frequency is usually fixed and the carriers are not synchronised to the reference sinusoid zero crossing. This avoids gear changing in variable speed drives where the switching frequency is changed as the inverter output sinusoid frequency varies. Multilevel inverters are aimed at higher power applications and the semiconductor switch technology has inherent operating speed limitations due to higher switching losses. Therefore, the inverter switching frequencies must be relatively low, so that it is preferable to synchronise the triangular carrier to the reference sinusoid to optimise performance. The following analysis focuses predominantly on synchronous mode operation.

In two-level inverters, there is only one triangular carrier, and there is a set of generally accepted guidelines for the selection of the frequency modulation index, m_f, which dictates the switching frequency of the inverter [4.5]. Firstly, m_f must be an integer otherwise sub-harmonics below the fundamental frequency will be present in the output voltage which is undesirable, especially if at very low frequency in ac

machines. Secondly, if m_f is less than 21, then it should be an odd integer otherwise the output waveform is asymmetric with even harmonics present. Thirdly, for three-phase inverters, m_f should be a multiple of 3 so that its fundamental is at a triplen harmonic frequency of the fundamental and is cancelled out in the load. For larger m_f values, selecting an odd number is less of an issue and does not necessarily need to be an integer.

In Chapter 1, it was shown that in multilevel inverters, the implementation options available are increased, and the additional degrees of carrier positioning both spatial and in time have led to a wide variety of different schemes. This means that the existing rules are not necessarily applicable to all forms of multilevel carrier scheme. Presently, there is no definitive answer as to what is the best scheme. Individual applications may require different approaches, or more likely there are only small differences between implementation.

There has been much work published on analytical approaches based on Fourier series analysis for investigating different carrier-based PWM schemes, most notably Holmes and Lipo [4.6]. It is not the intention of this investigation to confirm previous work, but to use detailed simulation as a tool to investigate the characteristics and behaviour of a flying-capacitor multilevel inverter when controlled by different forms of carrier-based PWM.

This section lays out the terminology used when discussing PWM implementations and provides an initial appraisal of the different carrier placement schemes under ideal inverter conditions.

4.2.1 Carrier Placement Strategies

Original three-level inverter PWM control used a unipolar modulation technique where a single carrier was compared with a rectified sine wave reference to obtain the positive and negative cycle firing signals. An alternative strategy was proposed by Velaerts et al., which used a single carrier and distinct sinusoidal references [4.7]. The sine-triangle PWM extension to more than two levels involves dividing the sine wave reference into distinct bands where the number of bands equals the number of complementary switch pairs in the inverter. The sinusoidal reference is then compared with each triangular carrier and the sum of the comparator signals form the voltage level command for the inverter. This carrier placement strategy is commonly referred to as phase disposition (PD) since all the carriers are in phase, but disposed in contiguous bands. Phase disposition was originally discussed by Carrara et al. [4.8], and extended to include other disposed carrier placements.

Alternatively, the carriers can encompass the whole reference range but are all out of phase from each other. This scheme is commonly referred to as phase shift (PS) multilevel PWM. This form of multilevel PWM has been preferred by the Toulouse group to control the flying-capacitor inverter [4.9].

The simulation work concentrates solely on multilevel sine-triangle PWM schemes where all the carriers are at the same frequency. However, Tolbert and Habetler have proposed a PD scheme with non-equal m_f carriers [4.10], and if applied to all other forms of multilevel PWM would dramatically increase the implementation options available.

4.2.1.1 Phase Disposed PWM

Figure 4.2.1 illustrates the carrier positioning with respect to the sine wave reference and the resultant output voltage level for phase disposition (PD) PWM. Natural sampling refers to the fact that the reference is a pure sine wave without any distortion due to digital sampling. As can be seen, there is symmetry between the positive and negative half cycles because the m_f value is even. This means the phase spectrum contains only odd harmonics of the fundamental spread around the carrier frequency component. The carrier position in the case shown in the figure is sometimes referred to as W-type carriers [4.11], because the carrier at the quarter period has a peak like the middle of the letter W. Alternatively, carriers phase shifted by 180° are deemed M-type for obvious reasons. The influence of this placement is only significant at lower switching frequencies, but is worthy of consideration when designing a practical inverter.

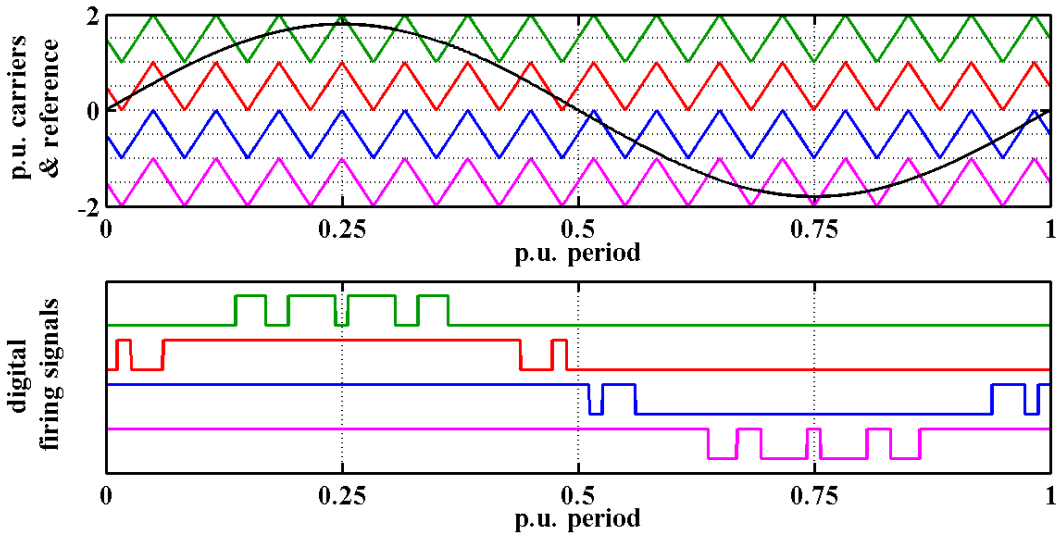


Figure 4.2.1: Modulation waveforms for PD PWM, natural sampling, m_a = 0.9, m_f = 15

Figure 4.2.2 shows the phase and line voltage spectra for PD PWM scheme under the above conditions. As can be there are no even harmonics present and all the triplen harmonics are removed in the line voltage spectrum. The PD scheme results in a significant harmonic at the carrier frequency in the phase voltage, which is cancelled in the line-to-line voltage.

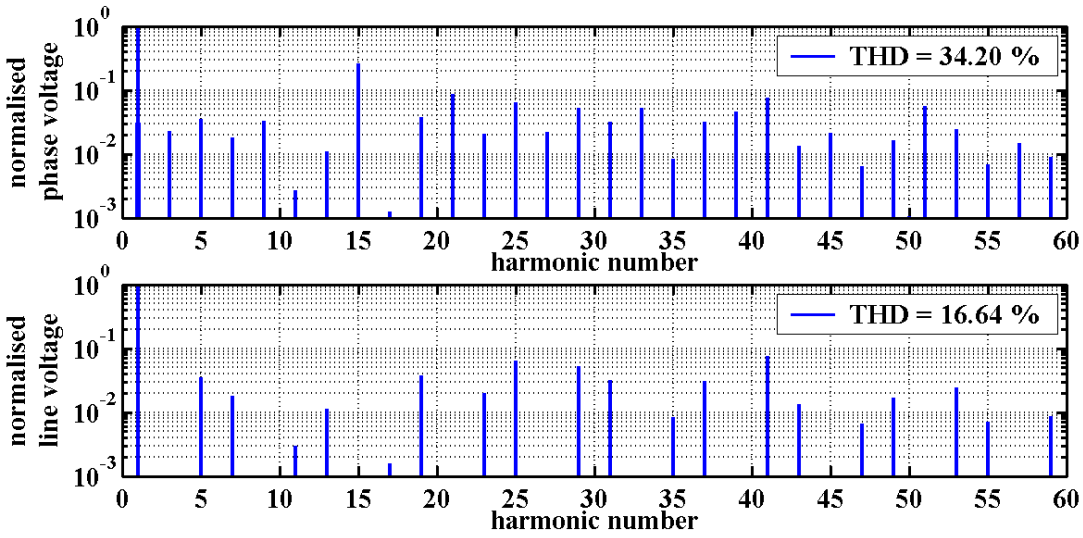


Figure 4.2.2: Voltage spectra for PD PWM, natural sampling, $m_a = 0.9$, $m_f = 15$

When the value of m_f is even, then there is asymmetry in the phase voltage and so the voltage spectra contain both odd and even harmonics as shown in Figure 4.2.3. The triplen harmonics are cancelled in the line voltage, but the harmonic at the carrier frequency is not cancelled. If the same carriers are used in all phases, rather than being synchronised to each phase reference, then the harmonic at the carrier frequency is cancelled in the line voltage, but the triplen harmonics are not, as seen in Figure 4.2.4.

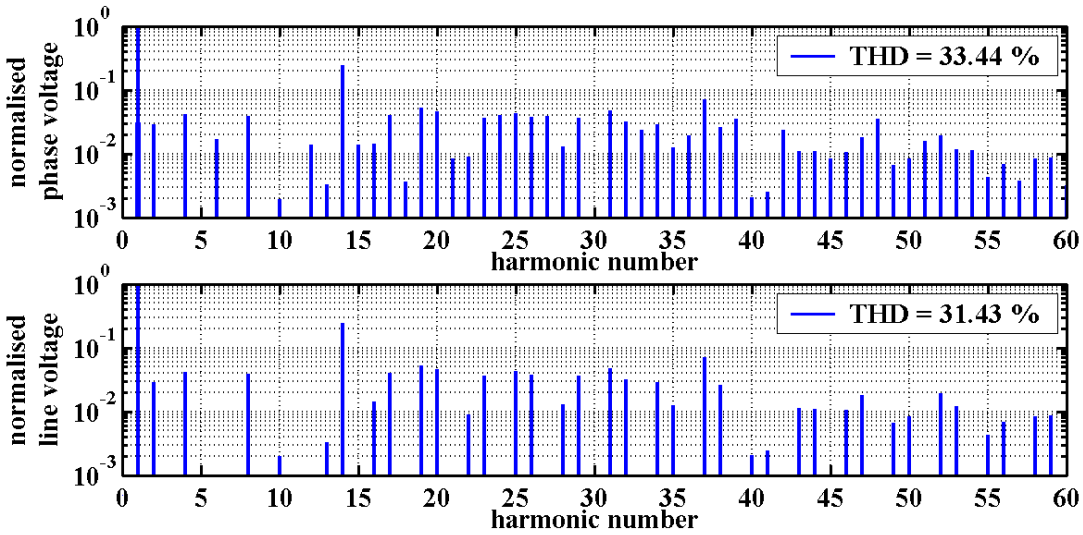


Figure 4.2.3: Voltage spectra for PD PWM, natural sampling, $m_a = 0.9$, $m_f = 14$

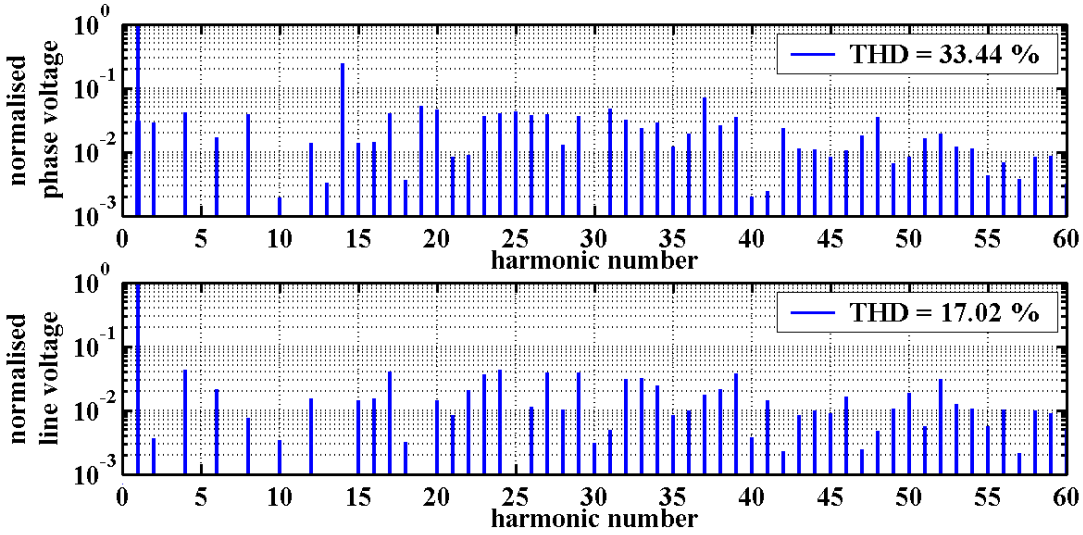


Figure 4.2.4: Voltage spectra for PD PWM, natural sampling with synchronous carriers, $m_a = 0.9$, $m_f = 14$

Therefore at low frequency modulation indexes, it is better to select a value which is an odd integer and multiple of 3. Figure 4.2.5 shows a waterfall plot of the low order harmonic for m_f values ranging up to 30. As can be seen, the carrier frequency component is cancelled, and the benefits of selecting m_f with odd multiples of 3 are not clear cut especially as the index increases.

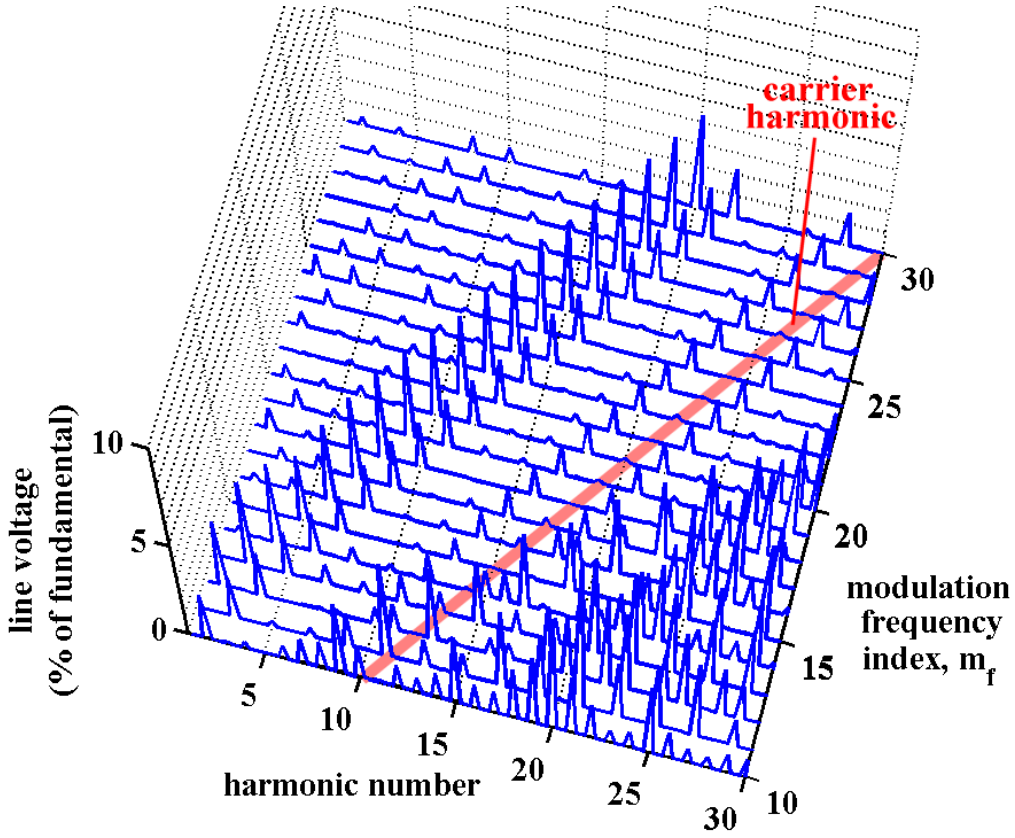


Figure 4.2.5: Low order harmonics versus frequency modulation index, m_f

At higher switching frequencies, the PD scheme results in the spectral signature shown in Figure 4.2.6, with the highest peak in the phase voltage occurring at the carrier frequency, which is cancelled in the line voltage. All the triplen harmonics are cancelled throughout the spectrum. The significant sidebands around the carrier are odd harmonics of the fundamental as expected from the symmetric phase voltage waveform. The sidebands around the twice the carrier frequency, and consequent carrier multiples, are also odd harmonics of the fundamental.

Another important feature of the PD modulation phase voltage spectrum is the wide spread of sidebands around the carrier frequency harmonic. This means that any filtering between the inverter and the load will need to have a much lower cut-off frequency that the inverter switching frequency.

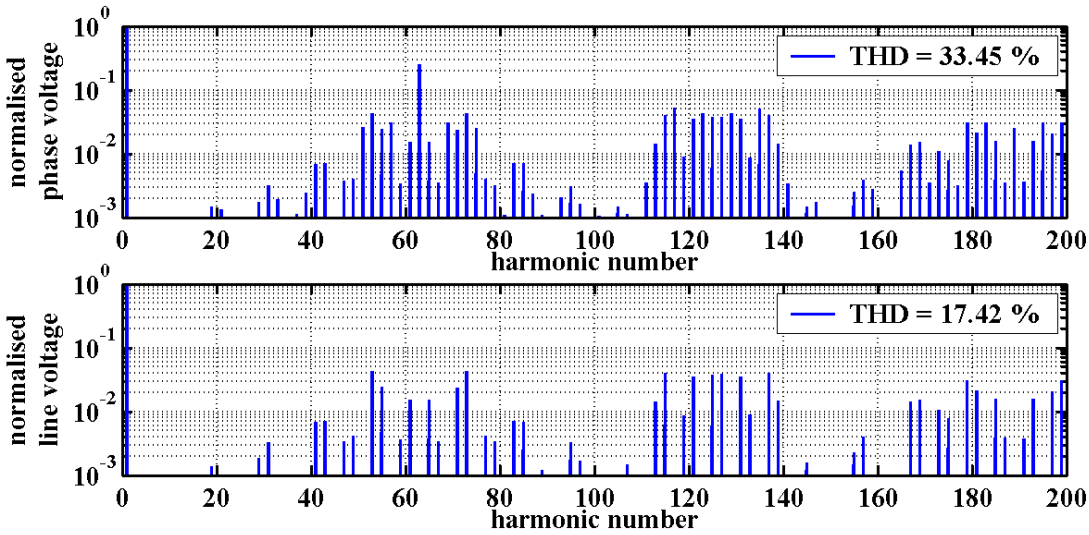


Figure 4.2.6: Voltage spectra for PD PWM, natural sampling, $m_a = 0.9$, $m_f = 63$

With large m_f values, the requirement for an odd integer at a multiple of 3 is not important. Figure 4.2.7 shows the voltage spectral for the case when $m_f = 62$. As can be seen the triplen harmonics, together with the harmonic at the carrier frequency, are all cancelled in the line voltage spectrum. In this case, the sideband harmonics around the carrier frequency are even harmonics, but at the even multiples of the carrier frequency, such as around the 124th harmonic they are odd harmonics. The value of m_f does not need to be an integer either and almost identical performance is seen, since the significant harmonics are concentrated around the carrier frequency and multiples of that frequency.

These results show that the PD PWM obeys the same rules governing m_f selection which applies to the conventional sine-triangle PWM scheme.

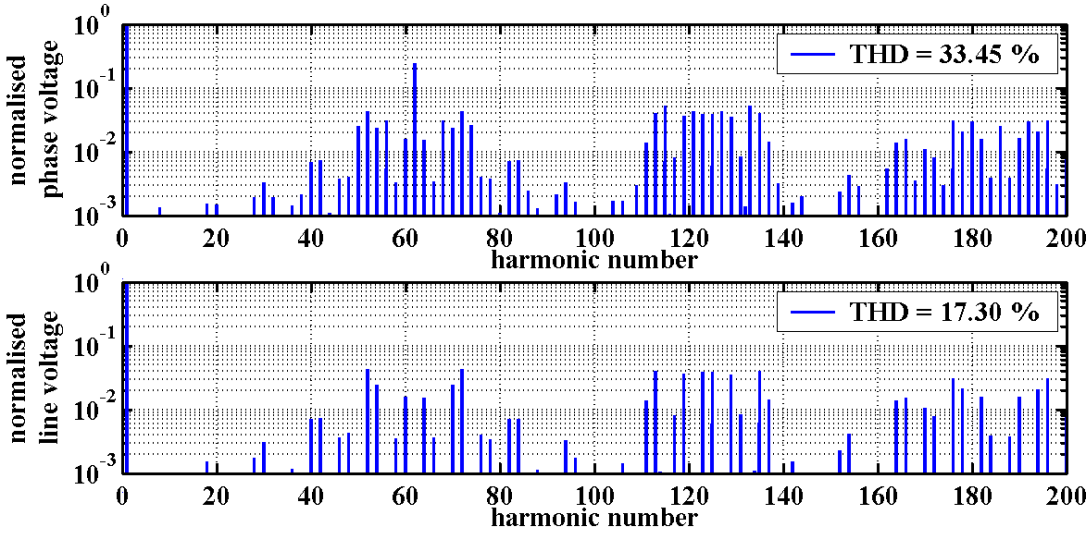


Figure 4.2.7: Voltage spectra for PD PWM, natural sampling, $m_a = 0.9$, $m_f = 62$

4.2.1.2 Opposition Disposition PWM Schemes

There are alternative schemes proposed in the literature [4.7, 4.12, and 4.13] which involve inversion or phase-shifting by 180° of some of the banded carriers in the PD scheme. Phase opposition disposition (POD) inverts the carriers below the zero reference line. Alternative phase opposition disposition (APOD) alternates the carrier phase-shift. Figures 4.2.8 and 4.2.9 illustrate the carrier positioning with respect to the sine wave reference and the resultant output firing commands for the two schemes. In this case, where m_f is odd, both schemes have asymmetry between the positive and negative half cycles and the spectrum only contains odd and even harmonics of the fundamental frequency.

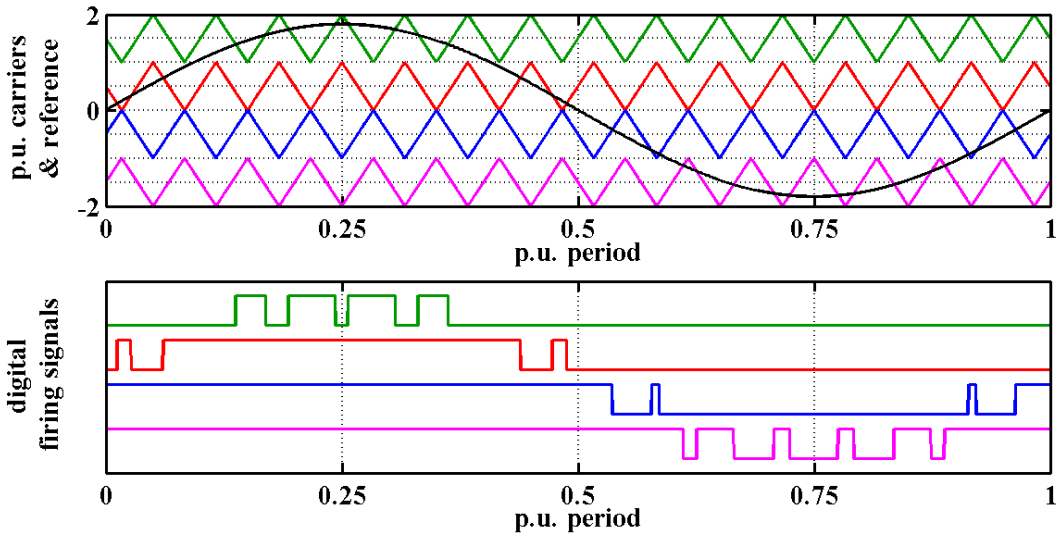


Figure 4.2.8: Modulation waveforms for POD PWM, natural sampling, m_a = 0.9, m_f = 15

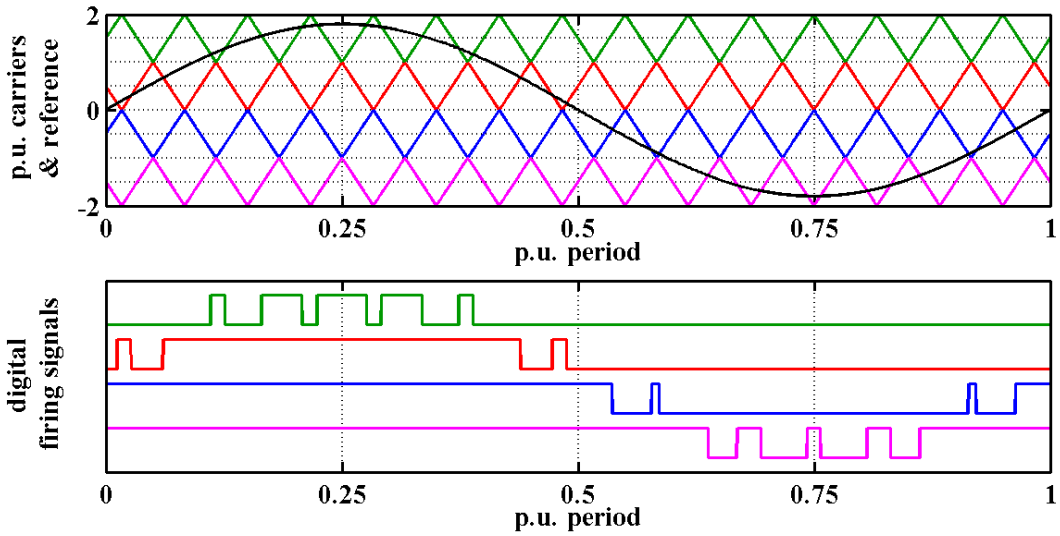


Figure 4.2.9: Modulation waveforms for APOD PWM, natural sampling, m_a = 0.9, m_f = 15

To ensure that the phase voltage spectrum has only odd harmonics, then m_f must be an even integer for these two schemes. Figure 4.2.10 shows the modulation waveforms for the POD scheme when m_f = 12. This is because the phase voltage waveform is composed of individual pulses which are symmetric over a whole cycle, even though there is asymmetry in the positive and negative halves of the whole waveform. To achieve true symmetry, the carriers need to be all phase shifted by 90° as shown in Figure 4.2.11. This results in a W-type carrier when m_f is even. An M-type carrier also gives good results at low even values m_f.

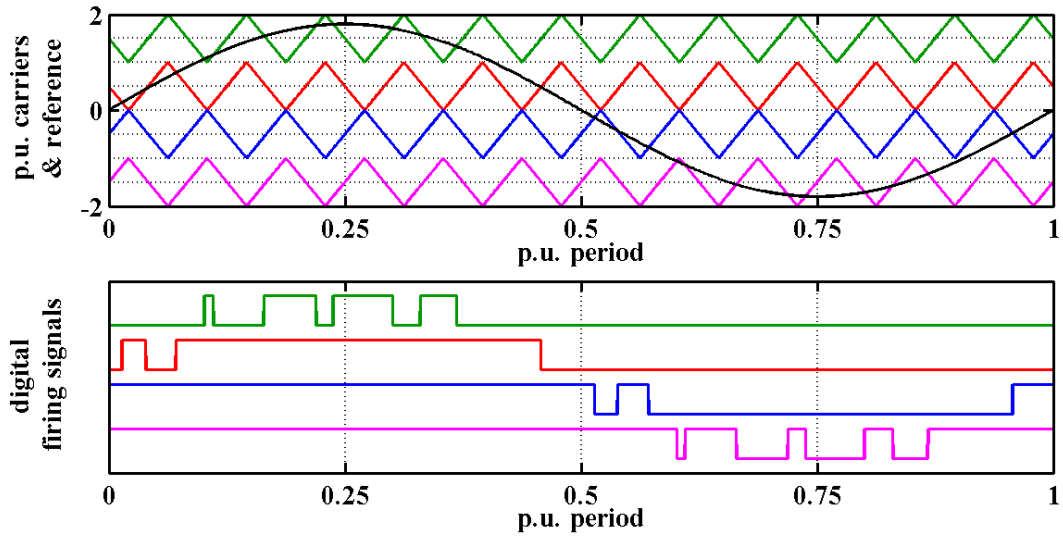


Figure 4.2.10: Modulation waveforms for POD, natural sampling, m_a = 0.9, m_f = 12

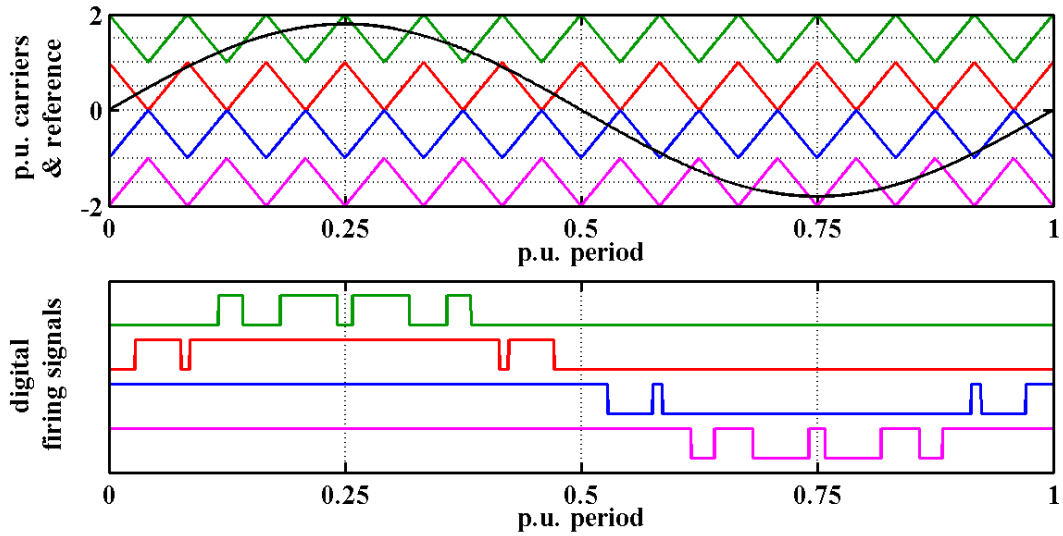


Figure 4.2.11: True symmetry POD, natural sampling, m_a = 0.9, m_f = 12

Therefore at low m_f values, the rules for POD and APOD are that m_f needs to an even integer and a multiple of 3 for a three-phase system. For different numbers of inverter levels, the APOD and POD schemes are directly scalable in terms of carrier placement. However, when the POD scheme is applied to an odd cell number inverter, the centre carrier phase can be either in phase with the upper or lower carrier. Therefore, in the three-cell case, APOD and POD implementations are identical.

At higher frequencies the m_f value and placement are less important. Figure 4.2.12 shows the voltage spectra for the natural sampling POD scheme with $m_f = 60$. It shows a similar envelope of harmonics to the PD scheme. The important differences is that there is no significant harmonic at the carrier frequency, but there are two main odd harmonic sidebands instead. This means that POD PWM has an inherently higher line voltage THD than PD PWM, since these carrier sidebands are no cancelled in the line voltage. From the line voltage THD perspective and the fact that the lower sidebands are spread widely below the carrier, it would appear that POD PWM does not offer any benefits over PD PWM.

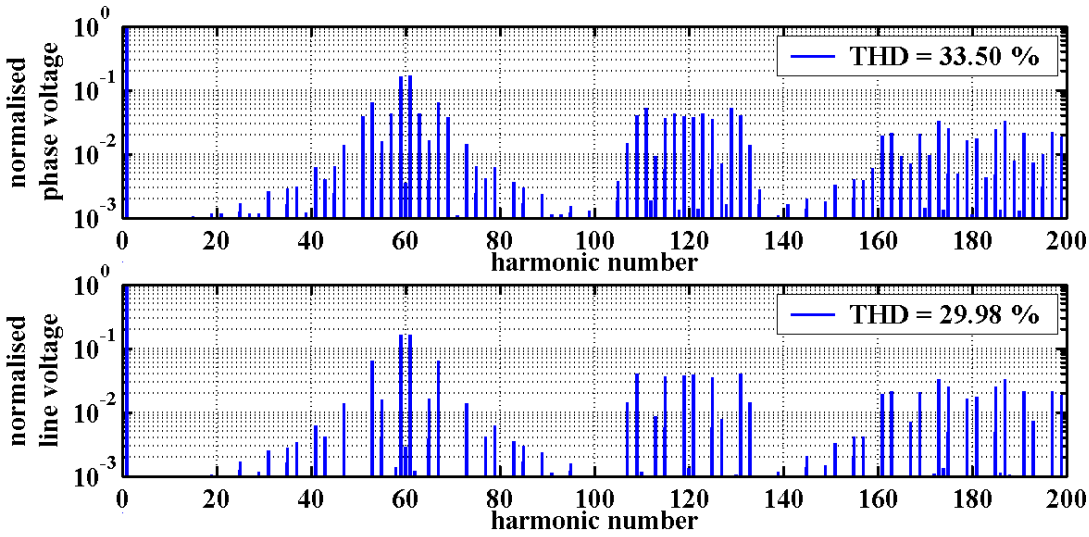


Figure 4.2.12: Voltage spectra for POD PWM, natural sampling, $m_a = 0.9$, $m_f = 60$

Figure 4.2.13 shows the harmonic spectra of the phase and line voltages for natural sampling APOD PWM with the same modulation indexes as before. Here the spectral envelope shows a marked difference compared to PD and POD, with the sidebands grouped more tightly around the carrier and each multiple of the carrier frequency. The significant sidebands are all odd harmonics of the fundamental and triplen harmonic cancellation is plain to see in the line voltage spectrum. APOD PWM also has an inherently inferior line voltage THD due to the lack of carrier component in

phase voltage. The reduced spreading of the lower sideband components at low frequency does however offer the potential of improved performance over PD PWM in systems with output filtering.

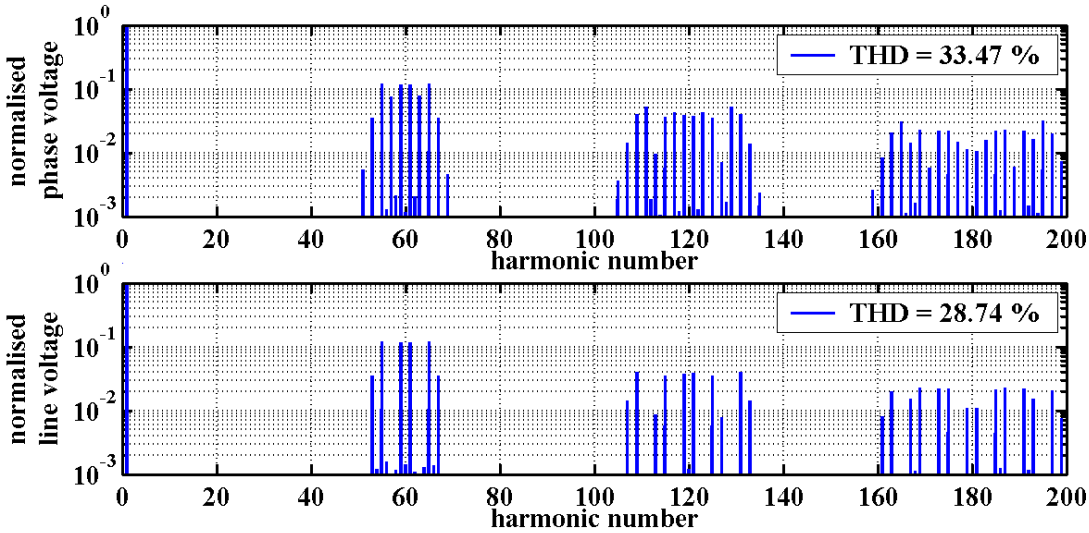


Figure 4.2.13: Voltage spectra for APOD PWM, natural sampling, m_a = 0.9, m_f = 60

4.2.1.3 Phase Shifting PWM Schemes

Another multi-carrier PWM scheme does not involve disposed carriers, but phase-shifting of full modulation amplitude carriers. Each carrier is phase-shifted by an angle equal to 360° divided by the number of inverter cells. Figure 4.2.14 illustrates the carrier and reference relative positions and output firing commands for the phase shift (PS) scheme. The modulation frequency index has to be m_f divided by the number of inverter cells to operate at the same switching frequency as an equivalent disposed scheme. Therefore, the example modulation waveforms are equivalent to PD with m_f = 12. The equivalent value of m_f for PS PWM has to be an even integer to avoid even harmonics being present in the output voltage.

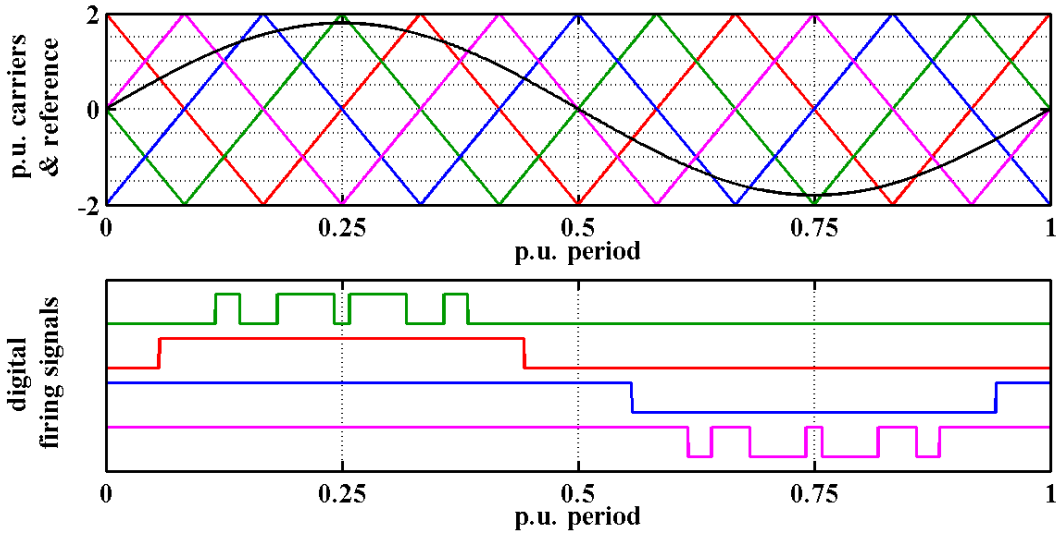


Figure 4.2.14: Modulation waveforms for PS PWM, natural sampling, $m_a = 0.9$, $m_f = 3$

An alternative form of PS has also been described by Agelidis and Calais [4.12], where half the carriers are disposed to each side of the reference. In order to compare equivalent switching frequencies, each carrier m_f is twice the index used for PS. Figure 4.2.15 illustrates the carrier and reference relative positions and output firing commands for this hybrid phase shift (HPS) scheme. As can be seen, HPS also requires even equivalent m_f values so that only odd harmonics are present in the output. It is worth noting that if all the carriers were shifted by 90^o, then the resultant modulation waveforms would be identical to the PS scheme, and at high switching frequencies the two schemes give identical results. Therefore the only benefit of HPS is in implementation, where a digital logic controller can use the same carrier during the positive and negative half cycles, thus halving the number of counters compared to a PS scheme.

The output voltage harmonic spectra for the PS scheme is shown in Figure 4.2.16 for the case when the equivalent $m_f = 60$. The spectral components are grouped tightly around the carrier and each multiple of the carrier frequency and the signature is very similar to the APOD scheme and so the line voltage THD is inherently higher than PD

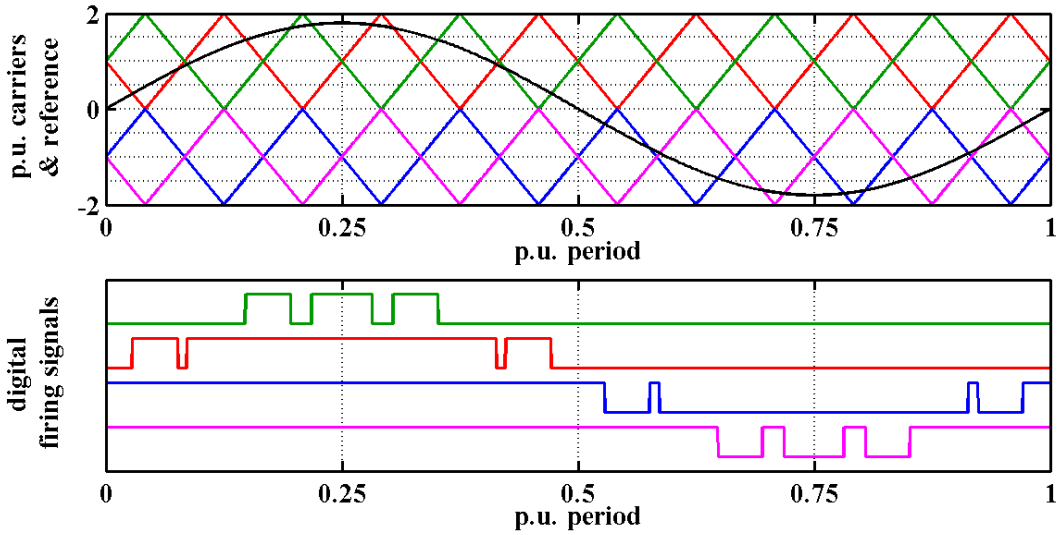


Figure 4.2.15: Modulation waveforms for HPS PWM, natural sampling, $m_a = 0.9$, $m_f = 6$

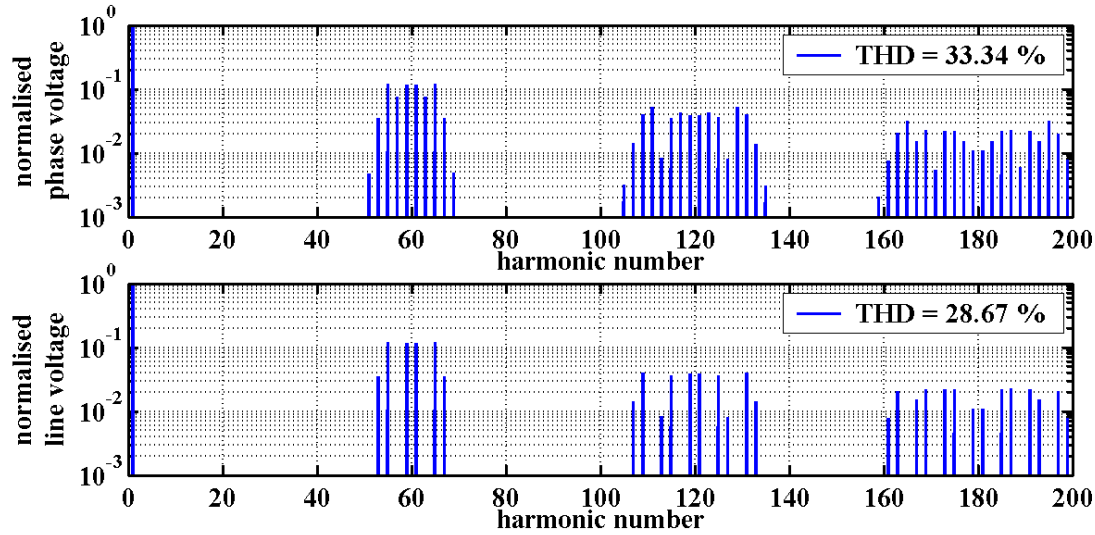


Figure 4.2.16: Voltage spectra for PS PWM, natural sampling, $m_a = 0.9$, $m_f = 15$

4.2.1.4 Alternative Carrier Placement PWM Schemes

The disposed schemes described in the previous sections use 180° phase shifting in the carriers, whilst the PS scheme in the particular case shifts by 90° which is set by the number of inverter cells. An alternative set of carrier schemes are possible by applying a 90° phase shift to the inner band carriers. Figure 4.2.17 illustrates the modulation waveforms when this phase shift is applied to the PD case (SPD). In this case m_f must be odd to ensure that there are no even harmonic components present in the output voltage.

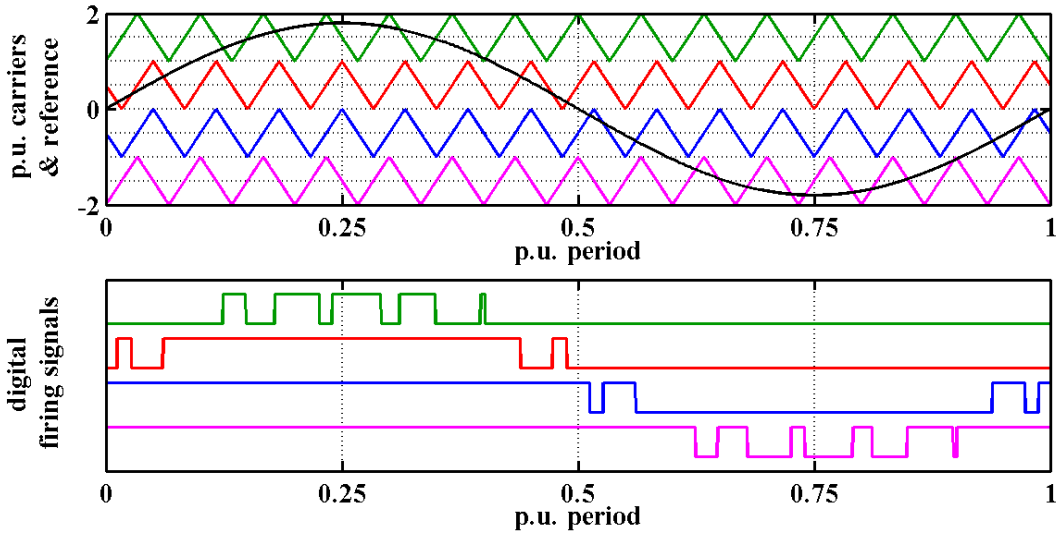


Figure 4.2.17: Modulation waveforms for SPD PWM, natural Sampling, m_a = 0.9, m_f = 15

Figure 4.2.18 shows the output voltage spectra of the SPD PWM scheme. The characteristic is very similar to PD PWM, with a significant harmonic at the carrier frequency being present in the phase voltage spectrum but cancelled in the line voltage spectrum. This carrier frequency cancellation leads to a reasonable low line voltage THD, although it is not as good as standard PD PWM.

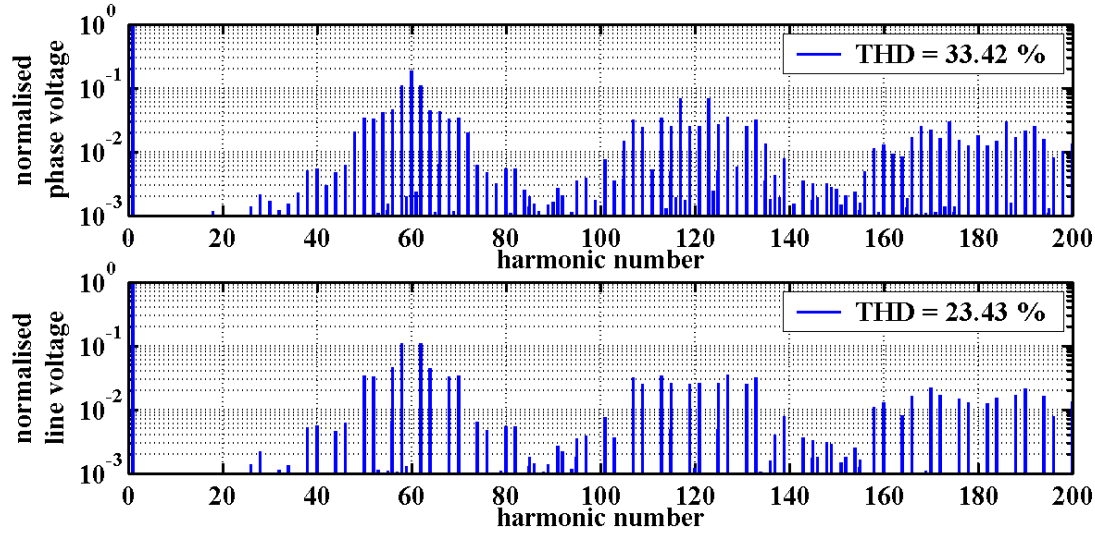


Figure 4.2.18: Voltage spectra for SPD PWM, natural sampling, m_a = 0.9, m_f = 60

Figure 4.2.19 illustrates the result of the phase-shifting of the inner carriers in the POD scheme (SPOD) in the modulation waveforms. In this case m_f must be even to ensure that there are no even harmonics present in the output voltages.

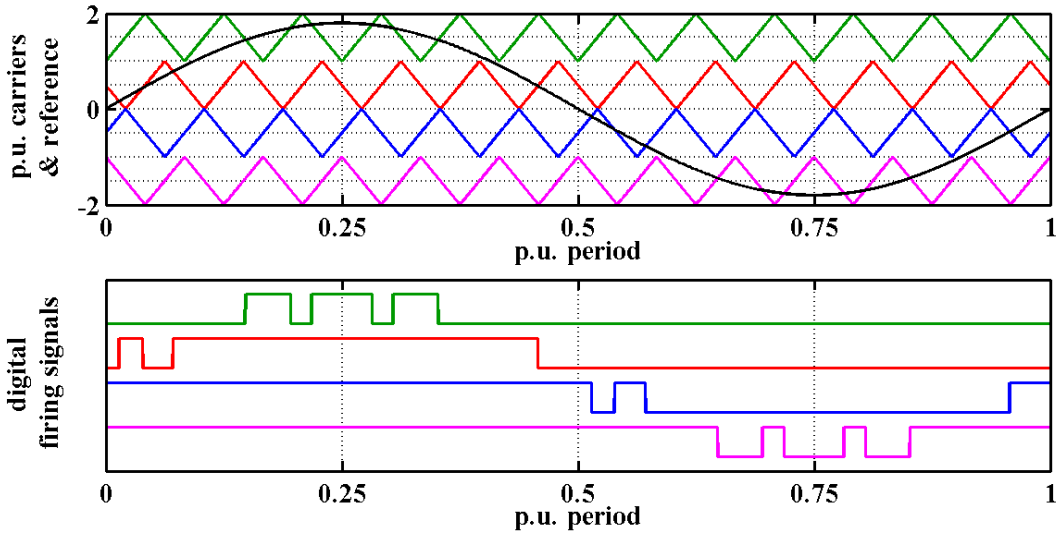


Figure 4.2.19: Modulation waveforms for SPOD PWM, natural Sampling, m_a = 0.9, m_f = 12

Figure 4.2.20 shows the resultant output voltage spectra of this carrier scheme. The spectral signature is very similar to POD with the two sidebands around the carrier frequency which are still present in the line voltage spectrum.

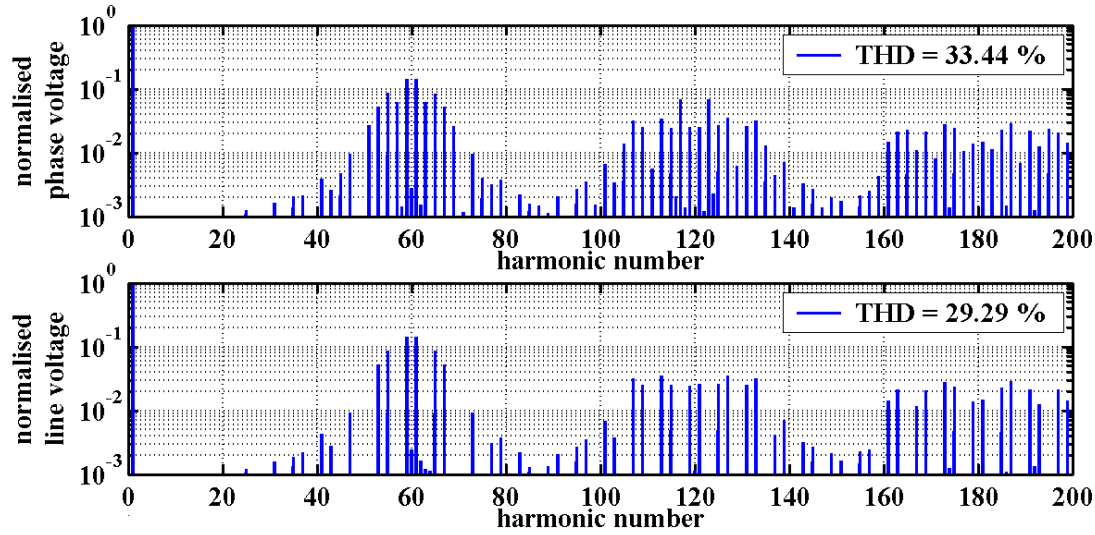


Figure 4.2.20: Voltage spectra for SPOD PWM, natural sampling, m_a = 0.9, m_f = 60

Finally, all the carriers can be phase-shifted from each other like the PS scheme, but disposed into separate bands. Figure 4.2.21 shows the modulation waveforms for this disposed PS scheme (DPS). For this particular carrier placement strategy, there are always odd and even harmonics present in the output voltage spectra regardless of whether m_f is odd or even.

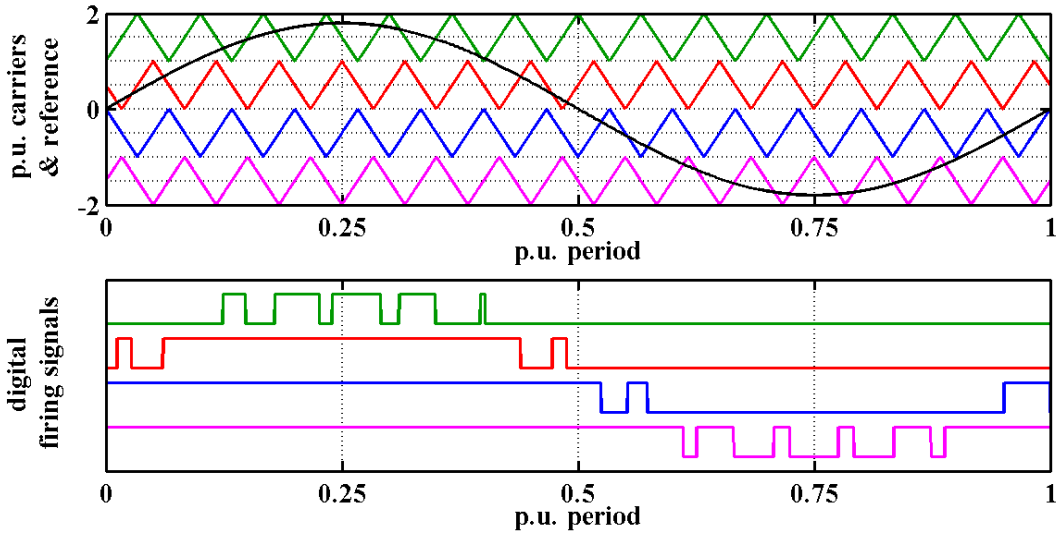


Figure 4.2.21: Modulation waveforms for DPS PWM, natural Sampling, $m_a = 0.9$, $m_f = 15$

The output voltage spectra for DPS PWM, Figure 4.2.22, show clearly the odd and even harmonics in the sidebands around the carrier frequency. Note that the sidebands around even multiples of the carrier frequency contain only even harmonics since m_f is even in this case. The harmonic distortion in the line voltage is the highest of all the possible carrier replacement schemes reviewed.

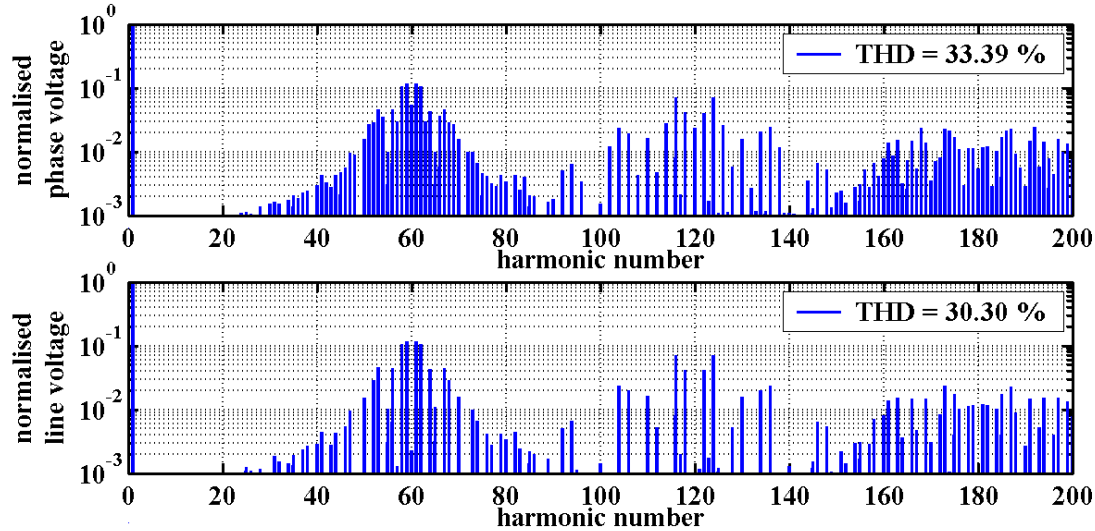


Figure 4.2.22: Voltage spectra for DPS PWM, natural sampling, $m_a = 0.9$, $m_f = 60$

4.2.2 Extending the Modulation Depth

In sine-triangle PWM, the maximum modulation depth is unity when the peak of the reference is equal to the peak of the carrier, or in the case of the disposed methods, the upper carrier. Overmodulation techniques to increase the output voltage have been

investigated in depth by Hava et al. [4.14, 4.15]. Low distortion voltage output modulation with $m_a > 1$ can be achieved, however, by using third harmonic injection in the reference waveform for sine-triangle PWM [4.16, 4.17]. The choice of injected frequency means that it is a common mode signal and cancels like a triplen harmonic in the line voltage, and so not affecting performance. The technique in standard 3-level, three-phase inverters normally uses an injected signal with the $1/6^{th}$ of the amplitude of the reference which can be shown to increase the theoretical range of the modulation depth to 1.155. Alternative amplitudes of $1/4^{th}$ of the reference can also be shown to operate affectively.

This modulation strategy is illustrated for PD PWM in Figure 4.2.23. The third harmonic injection method can of course be applied to all forms of carrier PWM to increase m_a above unity. The effect on the total harmonic distortion is only noticeable in the phase voltage where the third harmonic appears. The spectra for $m_f = 60$ is shown in Figure 4.2.24 for comparison with the previously presented ideal spectra. The third harmonic component is clearly visible in the phase voltage spectrum. There are several significant harmonic components present at lower frequencies compared to PD PWM, but the overall harmonic distortion level is on a par with PD PWM.

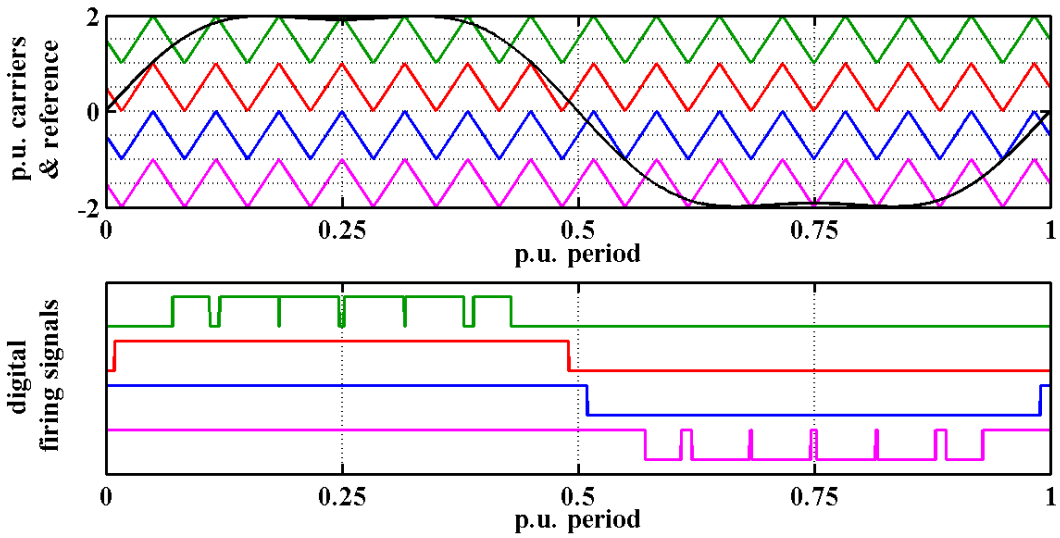


Figure 4.2.23: $1/6^{th}$ Third harmonic injection PD PWM, natural sampling, m_a = 1.155, m_f = 15

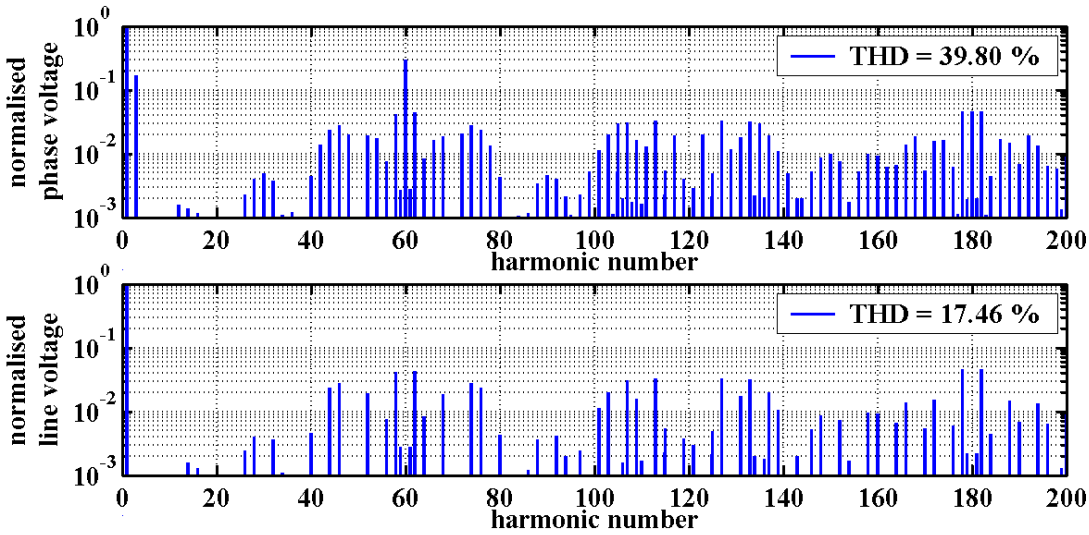


Figure 4.2.24: Voltage spectra of PD + 3rd PWM ,natural sampling, m_a = 0.9, m_f = 60

4.2.3 Reference Sampling Methods

The previous analysis of the carrier placement options assumed that the reference was naturally sampled and continuously varying when compared to the carriers. In reality a digital implementation is unlikely to update the reference on every clock edge and so the reference will be sampled at a slower rate. Bowes described the commonest methods which ensure that the reference is updated at the triangular carrier corners [4.18]. Symmetrical sampling is the term applied to reference update at trough of the carrier, and asymmetric sampling is used to describe reference update at both peaks and troughs in the carrier waveform. It is easy to envisage implementation in a digital system using carrier up-down counters with terminal count signals to enable clocking of the reference. The carrier period between samples thus supplies sufficient time to either compute the reference directly or access the value from a look-up table.

These two modes of sampling, and the resultant output signals, are shown in Figures 4.2.25 and 4.2.26. In the symmetric case there are both odd and even harmonics in the output voltage regardless of the fact that m_f is odd. In the asymmetric case only odd harmonics are present when m_f is odd.

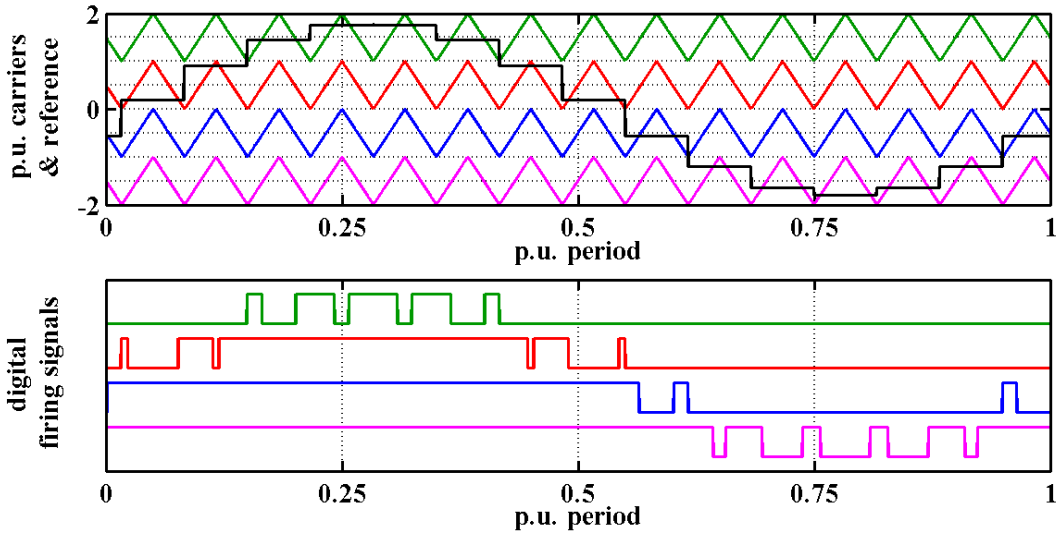


Figure 4.2.25: PD PWM symmetric sampling waveforms, $m_a = 0.9$, $m_f = 15$

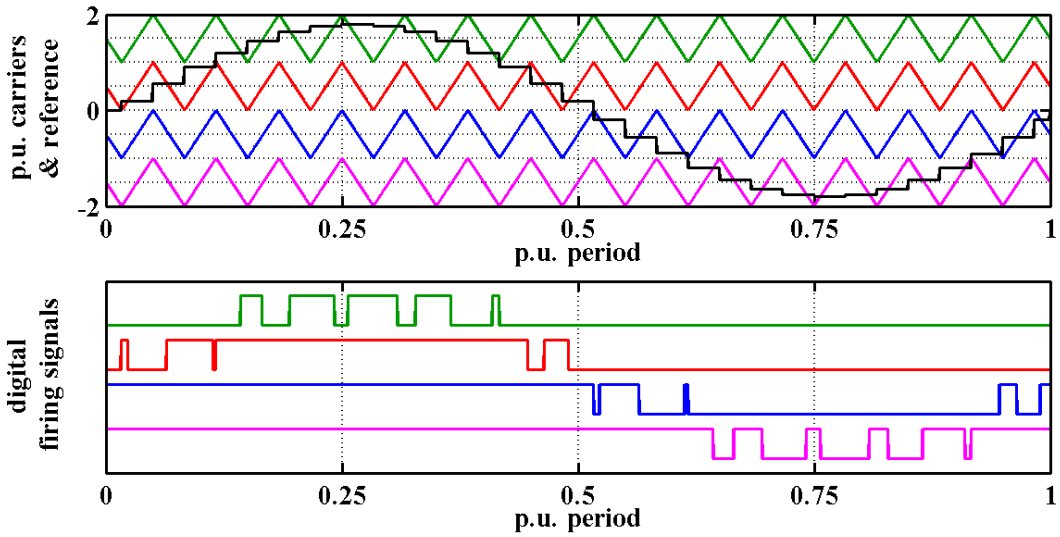


Figure 4.2.26: PD PWM asymmetric sampling waveforms, $m_a = 0.9$, $m_f = 15$

Figure 4.2.27 compares the line spectra for natural, symmetric and asymmetric sampling in the PD PWM scheme case with a high m_f value. The sampled reference does not affect the cancellation of the carrier component in the three-phase line voltage. These are more pronounced additional even harmonics in the symmetric case, especially noticeable in the sidebands of the carrier frequency. The asymmetric sampling line voltage spectrum and THD are very similar to the natural sampling case, and this is the preferred implementation in digital systems.

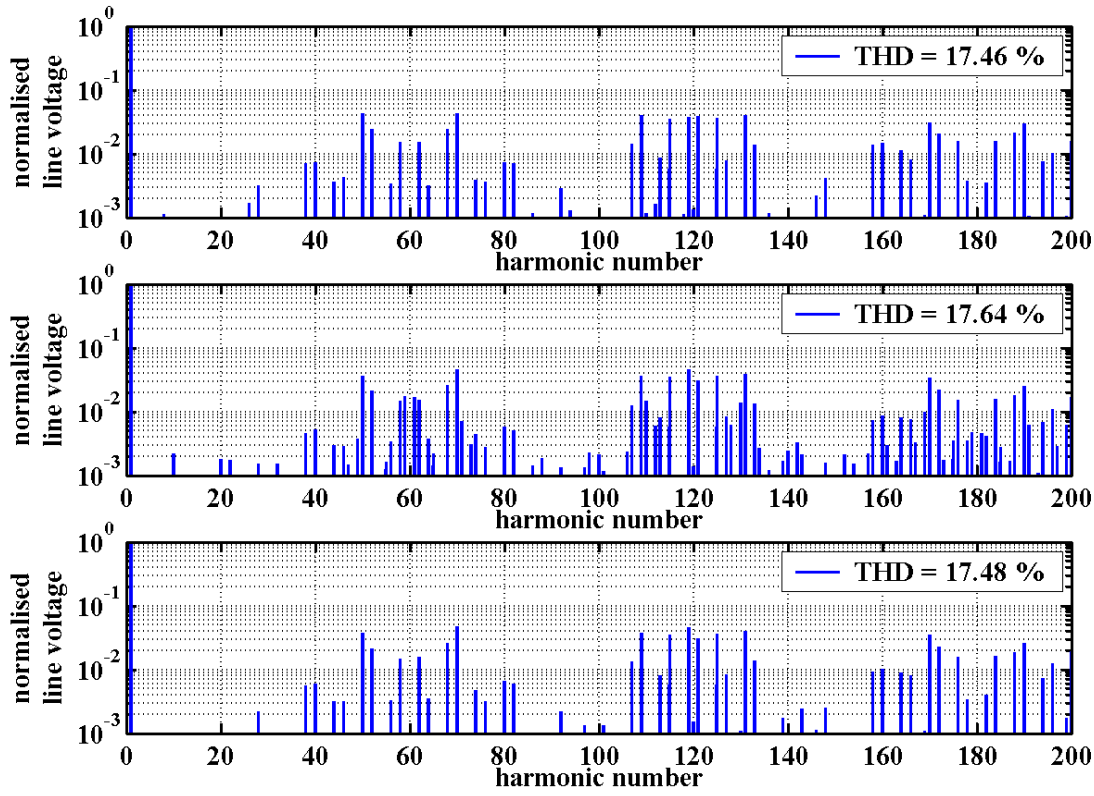


Figure 4.2.27: PD PWM line voltage spectra, natural sampling (top), symmetric sampling (middle), asymmetric sampling (bottom), $m_a = 0.9$, $m_f = 60$

4.2.4 Comparison of Multilevel PWM Schemes

The performance of all the carrier placement schemes outlined in this section can be judged by comparing the harmonic distortion of output voltages. Table 4.2.1 summarises output voltage quality using the standard distortion factors for the case of asymmetric sampling, m_a = 1 and m_f = 60. From these results, the PD scheme produces an output voltage with the lowest harmonic distortion and is therefore likely to be the best PWM scheme for ac motor applications. The line voltage DF1 value is also much lower indicating that the phase current will have lower harmonic distortion. Where second order LC filtering is present on the output of the inverter in power systems, then the PS and DPS schemes appear to offer advantages because of the much lower DF2 value. This is distortion factor weights the harmonic components by a square of the harmonic number and so gives an indication of the harmonic distortion of the filtered output voltage. It is also of interest to note that the APOD, PS and HPS schemes result in very similar line voltage THD levels, since the arrangement of the carriers in these schemes result in almost identical output voltage spectral signatures.

Scheme	Phase Voltage			Line Voltage		
	THD (%)	DF1 (%)	DF2 (%)	THD (%)	DF1 (%)	DF2 (%)
PD	26.95	0.36	0.10	17.07	0.17	0.09
POD	26.90	0.36	0.08	21.54	0.28	0.08
APOD	26.92	0.36	0.10	25.53	0.36	0.11
PS	27.54	0.40	0.08	26.66	0.40	0.04
HPS	27.09	0.37	0.12	25.75	0.37	0.13
SPD	26.95	0.36	0.08	20.77	0.27	0.07
SPOD	26.92	0.37	0.15	23.03	0.32	0.12
DPS	26.93	0.36	0.05	21.89	0.31	0.03

Table 4.2.1: Voltage harmonic distortion for different carrier schemes, m_a = 1.0, m_f = 60

To complete the comparative assessment of the different carrier schemes, the harmonic distortion variation with modulation index is analysed. The schemes PD, SPD and APOD are chosen for comparison. Figure 4.2.28 shows the variation in THD over the whole modulation range of the three schemes, and Figure 4.2.29 the variation in DF1 for the same variation in modulation index. It is clear that the PD scheme is superior over the whole modulation depth range. It is also worth noting that the SPD scheme has identical carrier placement to PD in the inner band and so performance is identical below m_a = 0.5. This is inline with findings from other researchers in the field. The later sections of this chapter dealing with individual control issues and inverter component sizing will only use the PD by way of analysis. The issue of optimum carrier scheme will be assessed again in conjunction with simulation of a complete realistic inverter system model towards the end of the chapter.

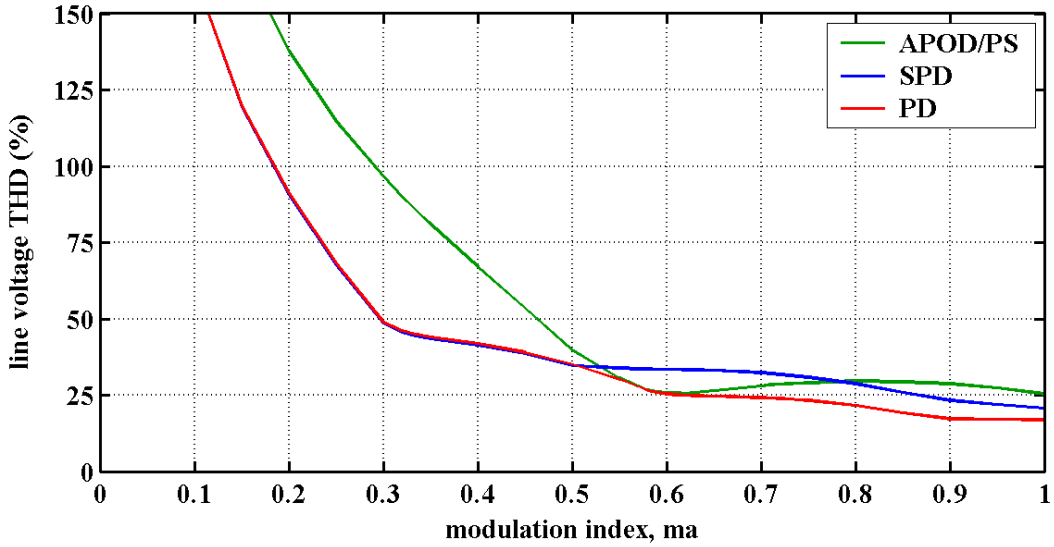


Figure 4.2.28: THD versus modulation index, m_a for different carrier schemes

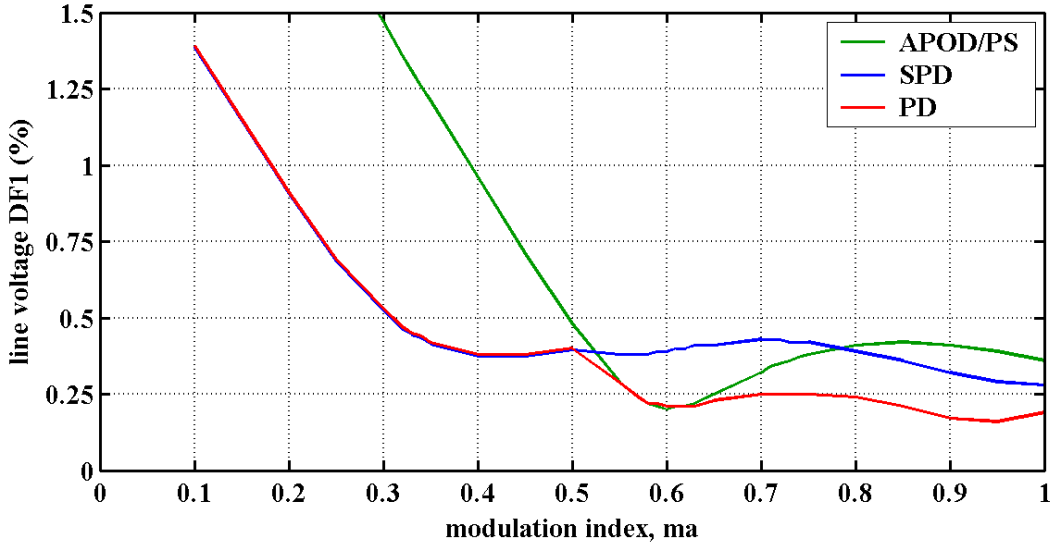


Figure 4.2.29: DF1 versus modulation index, m_a for different carrier schemes

4.3 Cell-Capacitor Balancing Scheme

In previous chapters, it has been shown that the flying-capacitor inverter cell-capacitor voltages can be regulated to balanced levels by ensuring that each capacitor sees zero average current over time. This section firstly explores cell-capacitor voltage balancing using a cyclic sequence of switching state patterns. A novel balancing digital logic block is then presented which can be used in conjunction with any form of fixed frequency PWM control.

4.3.1 Optimum Pattern Balancing Control

System balancing can be performed open-loop by cycling between all switching states in consecutive fundamental periods. This assumes that the current is the same at particular instant in every cycle. This strategy was successful in the low switching frequency SHE mode of operation, aided by the fact that there is a natural balancing mechanism inherent to the inverter. In SHE control, a stored switching sequence is used to cycle between states on consecutive, repeating N cycles where N is the number of inverter cells. This approach can be used together with a carrier based PWM control.

The inverter was simulated with the optimum balancing switching pattern, PATTERN #1, and with PD PWM control. The load parameters were R = 30 Ω and L = 97.4 mH, with no zero e.m.f. The unit cell capacitance was 1 mF and the dc link voltage 400 V, which gives a 1 kW load with a displacement power factor of 0.7 and energy factor, ξ = 25 s^{-1}. The desired fundamental is 50 Hz and the PWM switching frequency 3 kHz (m_f = 60).

Figure 4.3.1 shows the system waveforms produced by simulation. As can be seen, the system is balanced with the mean voltages at 98.9%, 98.9% and 103.1%, but there is noticeable ripple on the cell-capacitor voltages, with the maximum breakdown voltage being 153.7% of the unit cell voltage.

The output waveform spectra, Figure 4.3.2, show that there is a high concentration of components at low frequency made up of sub- and inter-harmonics, as well as harmonics of the fundamental. There are also additional sidebands generated around the carrier frequency component by the interaction of the harmonics components in the capacitor voltages. The relatively poor harmonic quality of the output power is reflected in the relatively high THD of the current waveform. It is interesting, however, to note that the phase and line voltage THD values are lower than the ideal case showing that the balancing pattern and resultant capacitor voltage waveform have a beneficial effect on reducing overall harmonic content.

Improvements can clearly be made by storing a more detailed switching pattern optimised for best performance as before. This approach is not a practical option in the case of higher frequency PWM, and so an alternative strategy must be developed.

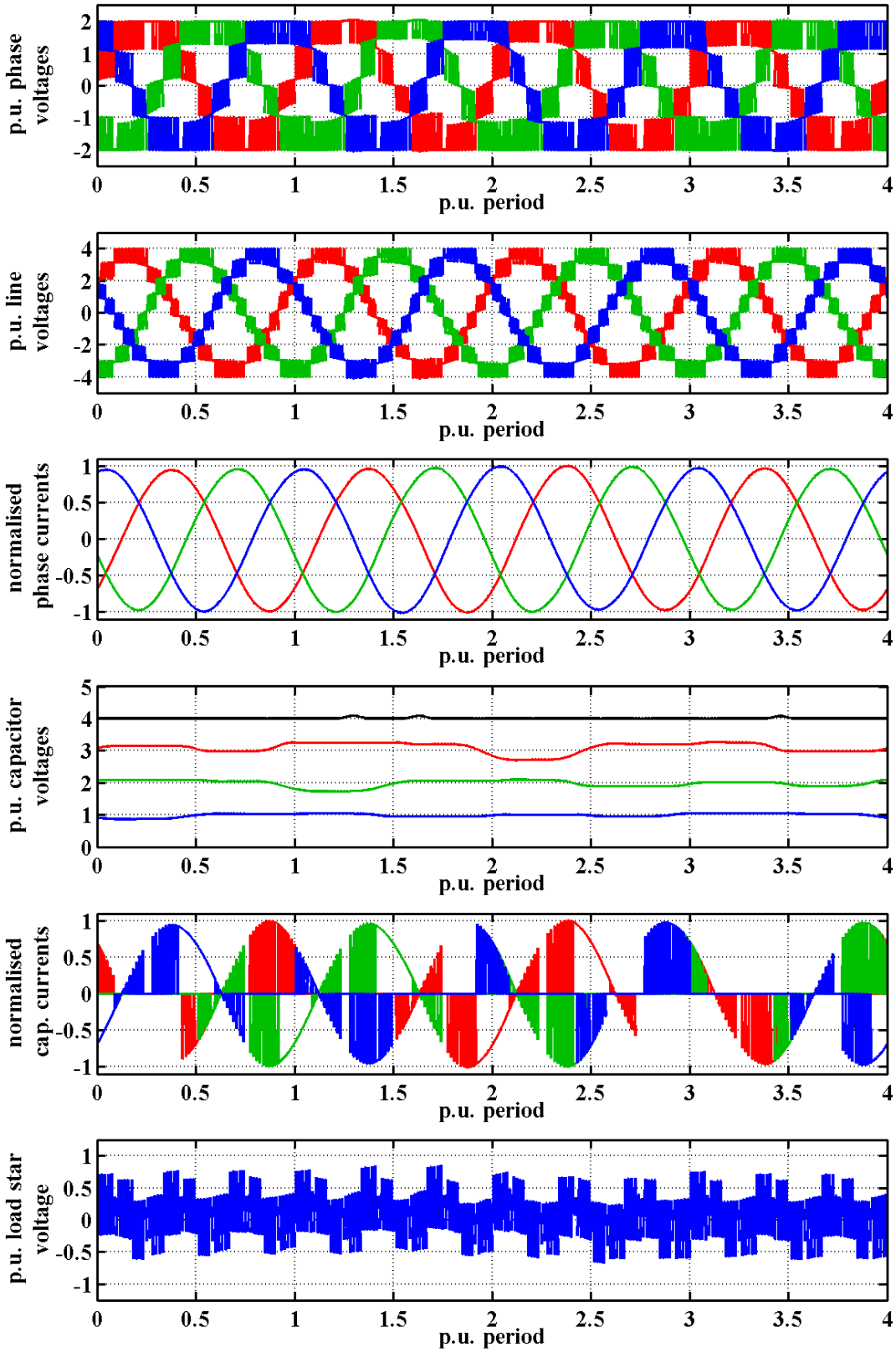


Figure 4.3.1: System waveforms for pattern balancing PD PWM, $m_a = 1$, $m_f = 60$

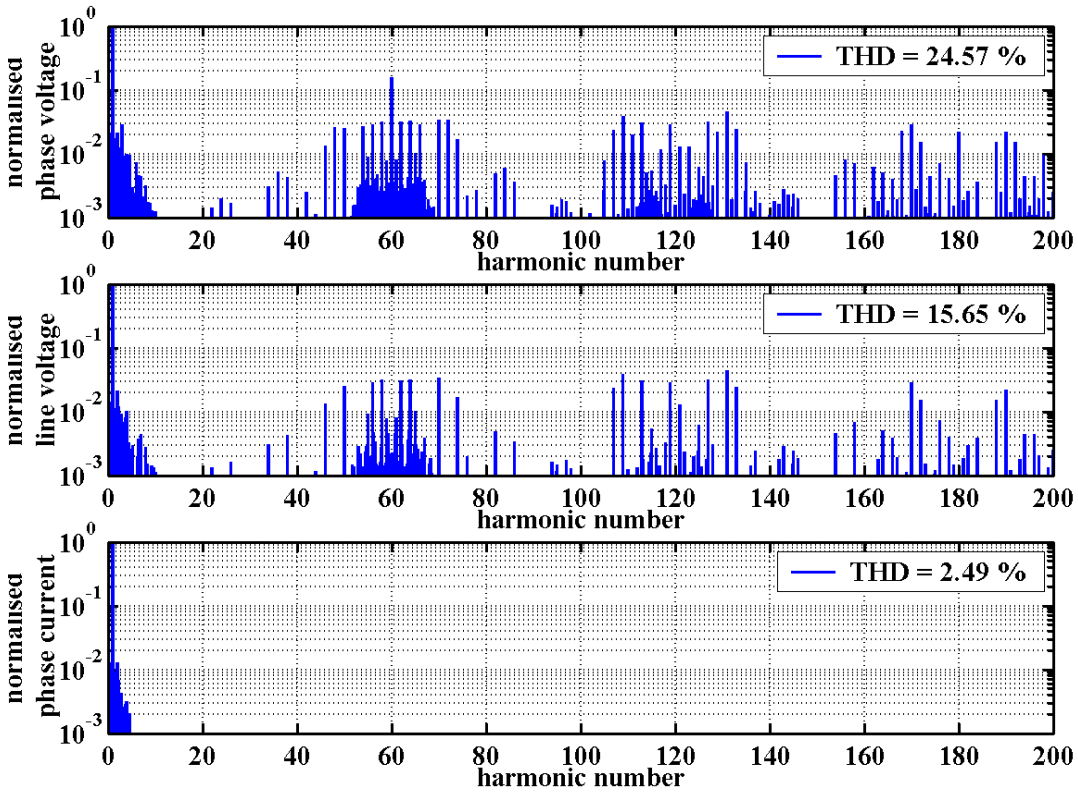


Figure 4.3.2: System spectra for pattern balancing PD PWM, $m_a = 1$, $m_f = 60$

4.3.2 Sub-Carrier Balancing Control

To obtain self-balancing of the cell-capacitor voltages, the complete set of level switching states must occur at the same point in time over different cycles. In the case of the four-cell inverter, the switching states for a given level can be rotated through over four cycles. The obvious way to do this is to multiplex all four comparator firing signals to each cell gate drive, where the selection signal pattern is different in each consecutive cycle, but repeats every four cycles.

These periodic signals must be at a lower frequency to the carrier, i.e. a sub-carrier. It would be preferable if the both balancing frequency and carrier frequency are as close as possible, and so an effective balancing frequency index, m_b, can be equal to $m_f - 1$. It is also necessary that balancing repetition period is not less than the full balancing timeframe dictated by the number of cells in the multilevel inverter. This means that m_b must always be odd, and so when m_f is an odd number, $m_b = m_f - 2$, and when m_f is even, $m_b = m_f - 1$.

The block diagram of the digital implementation of the sub-carrier balancing control is shown in Figure 4.3.3. BCLK1 and BCLK2 are the balancing clocks and their value changes state m_b times a cycle. They are latched to the multiplexers only on a

transition in the PWM firing command signals. This ensures that the balancing algorithm does not introduce increased inverter switching.

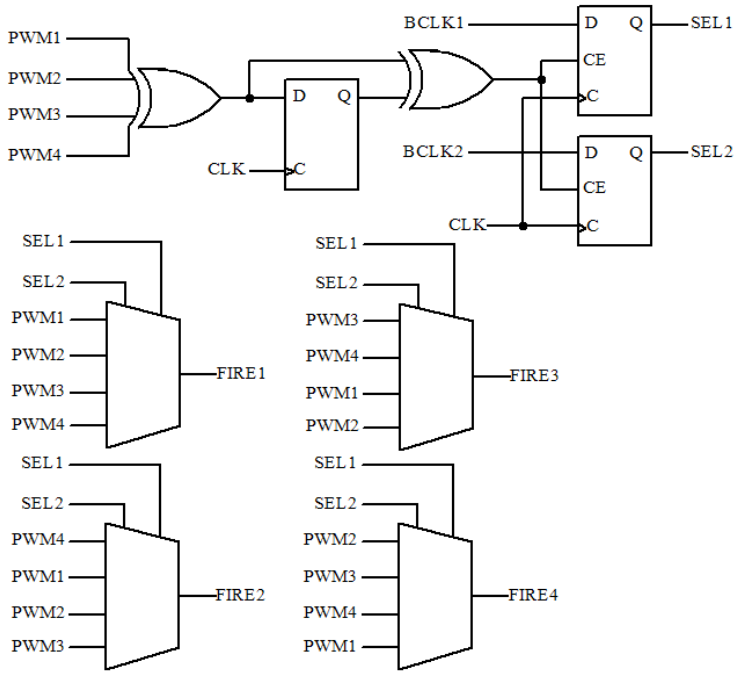


Figure 4.3.3: Sub-carrier PWM balance scheme digital logic block diagram

The timing diagram for this logic approach is shown in Figure 4.3.4. Focusing on the small pulse in line with the peak of the reference, circled, it can be seen that this is distributed in all four firing signals after being processed by the balancing logic block. The resultant sequence of switching states for this particular voltage level is

$$[1011] \rightarrow [0111] \rightarrow [1110] \rightarrow [1101]$$

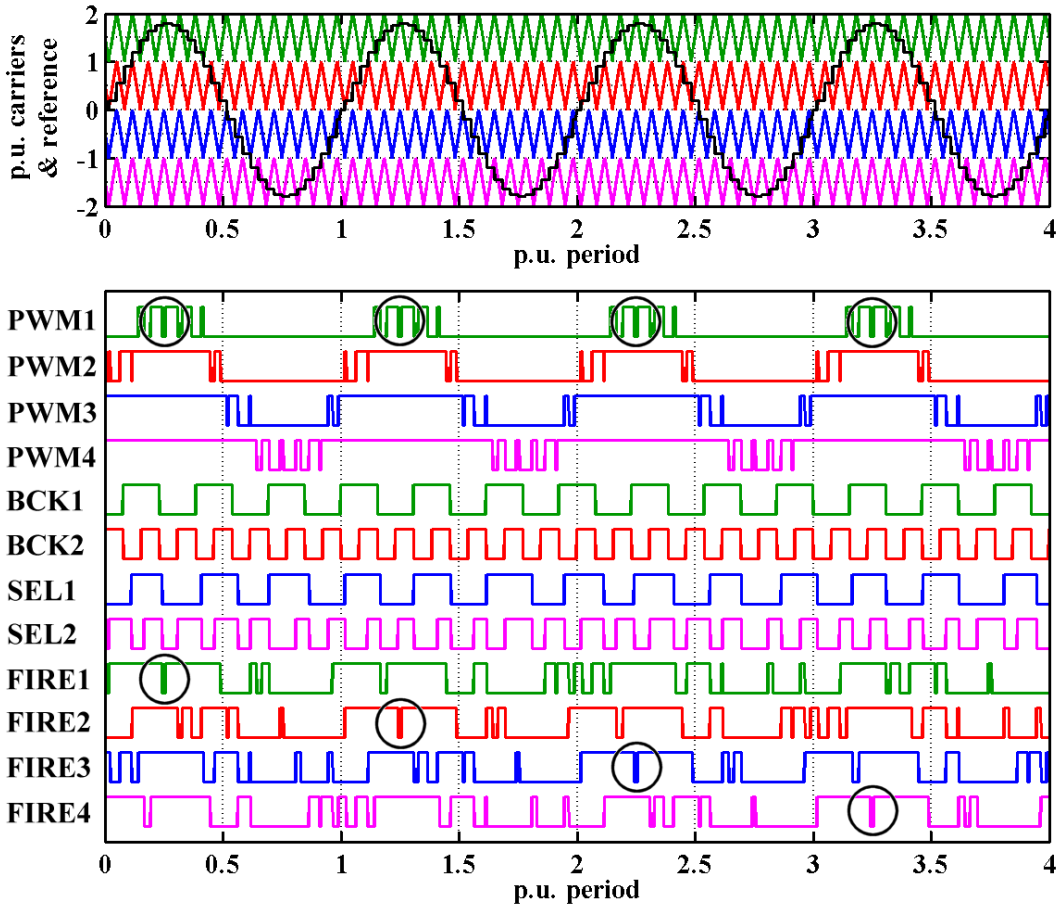


Figure 4.3.4: Balance scheme timing diagram (m_f = 15, m_a = 0.9)

Simulations reveal that this balancing strategy does achieve the desired effect. Figure 4.3.5 illustrates the inverter waveforms when operated under logic balancing control. The amount of voltage ripple is greatly reduced and the phase voltages and currents assume more ideal wave shapes. In this case the mean capacitor voltages are all within 2% of their target values, and the maximum blocking is now reduced to 110.9% of the unit cell voltage.

The frequency spectra for the new balancing scheme are shown in Figure 4.3.6. As can be seen, the phase current THD is greatly reduced in accordance with the reduction in the low frequency components. The voltage spectra reveal that there is an extra concentration of harmonics around the 15^{th} and 30^{th} harmonic of the fundamental. This is a result of the smaller higher frequency ripple component in the inverter capacitors resulting from the balancing algorithm.

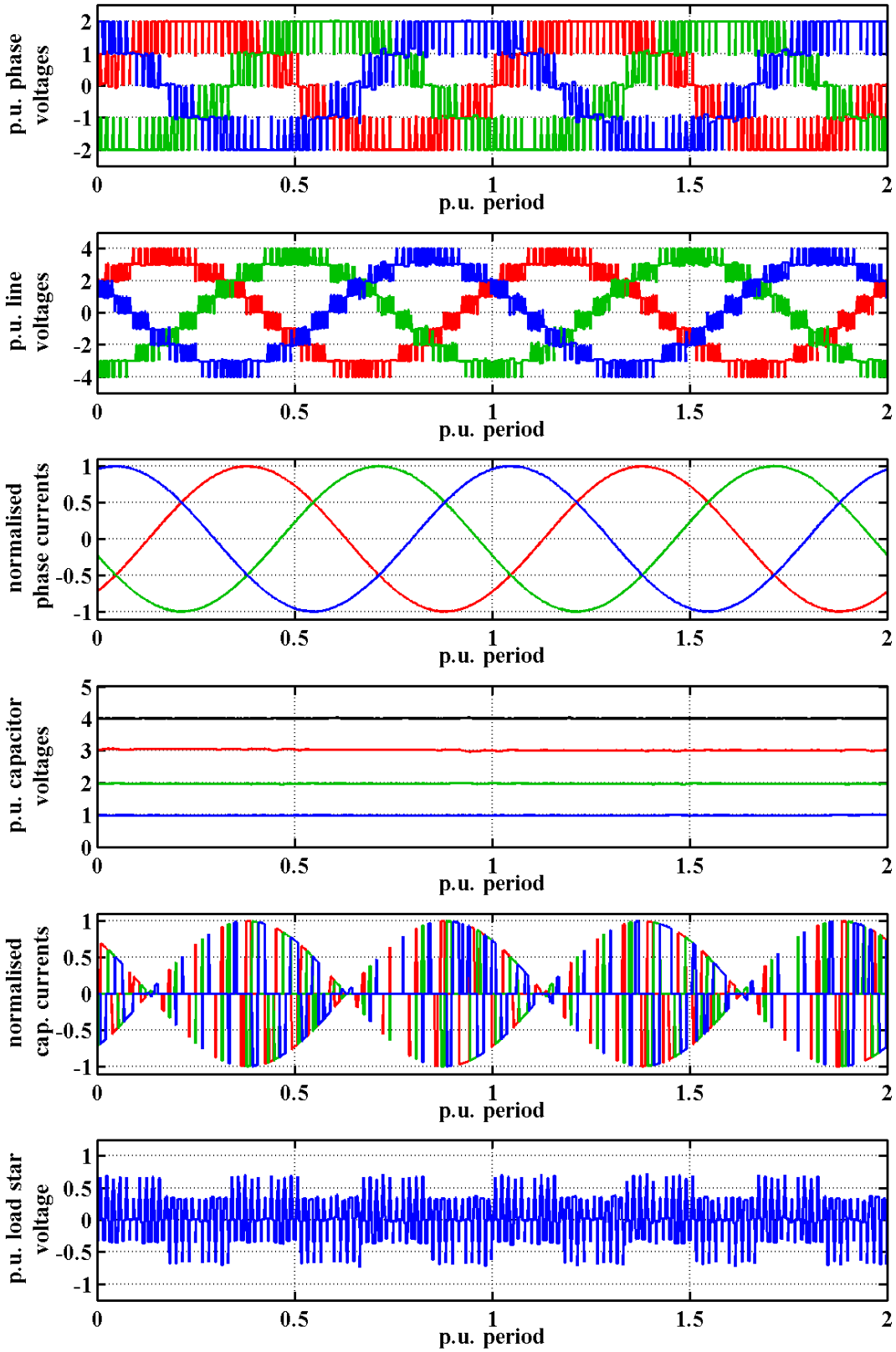


Figure 4.3.5: System waveforms for logic balancing PD PWM, $m_a = 1$, $m_f = 60$

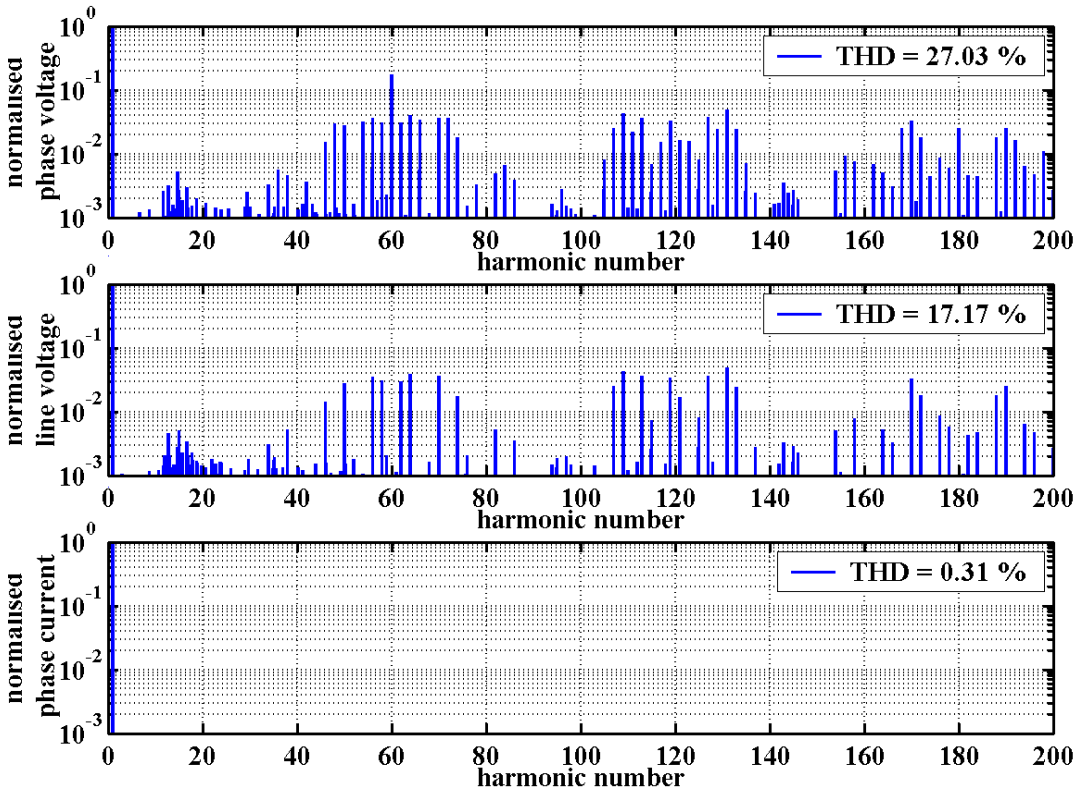


Figure 4.3.6: System spectra for logic balancing PD PWM, $m_a = 1$, $m_f = 60$

4.4 Practical Design and Performance Issues

4.4.1 Inverter Characteristics

In the chapter concerning SHE control, the effect of the balanced control scheme on the inverter operating characteristics were mapped out to assess the relationship between load rating, cell capacitor sizing, maximum switch blocking voltage and output power quality. This analysis is repeated on the inverter synthesising a 50 Hz sinusoid under PD PWM with the optimised logic block balancing scheme.

Simulations were run over a range of load power factors and energy factors, with fixed $m_a = 1$ and $m_f = 60$. The resultant line voltage THD contour is shown in Figure 4.4.1 and the phase current THD contour is shown in Figure 4.4.2. Note that the line voltage and phase current THD values are the same in the unity power factor case (ideal resistive load). Unlike the SHE control voltage THD characteristic where the THD was lower than the ideal case for power factors around 0.7, the THD value shows a peak at around 0.9 for PWM control. Unlike pattern balancing, the beneficial effect of significant low frequency ripple on the cell-capacitors in reducing voltage THD is not present in this form of control, since the cell-capacitor voltages are closer

to the ideal dc levels. Therefore, the angular position of the phase current peak has a dominant effect on performance. The voltage deviation on the cell-capacitor voltages is dependent on current level, and so with displacement power factors in the region of 0.7 (45° lagging angle), higher currents are circulating through the cell capacitors in this intermediary voltage level region. The phase current THD characteristic only shows a gradual increase as the cell capacitor size is reduced, reflecting the large filtering effect of the idealised inductive load model used in the simulation.

Figure 4.4.3 illustrates the variation in maximum blocking voltage together with output THD figures for different energy factors and fixed load power factors. These show very similar characteristics to SHE control, but the deterioration in performance and safe-operation occurs at a higher ξ value reflecting smaller voltage deviations achieved by operating at much higher switching frequencies. The graphs show that ξ is around 110 for maximum allowed blocking voltage for a safely operating inverter with margin on a 0.7 DPF load.

In the case of SHE control, where the inherent switching frequency is lower, the same study revealed a maximum ξ of around 25 for a 50 Hz operating output fundamental frequency. For the four-cell inverter, PWM control with m_f = 2 has an equivalent switching frequency to SHE control, so one would expect that a much higher ξ can be achieved while keeping within safe-operating blocking voltage limits, if there was a linear relationship with increasing m_f. This is not the case with this particular PWM control and balancing scheme. The relationship can be approximated by normalising ξ by a factor of $\sqrt{m_f/2}$ to obtain a direct comparison between the two forms of control. This relationship reflects that the cell-capacitors and load form a circuit which is essentially an under-damped second-order LC with the initial rate of change of voltage governed by the natural frequency.

Figure 4.4.4 shows the variation in maximum blocking voltage for DPF = 0.8 when the PWM curve is normalised to remove the modulation frequency depth effect. These curves now show good correlation and so scaling ξ for different m_f values can be used as design guide approximation when selecting the cell capacitance for a given load. It is important to note that this characteristic is for the particular case of 50 Hz output operation, and so ξ needs to be scaled by fundamental frequency in Hertz divided by 50 for other operating cases.

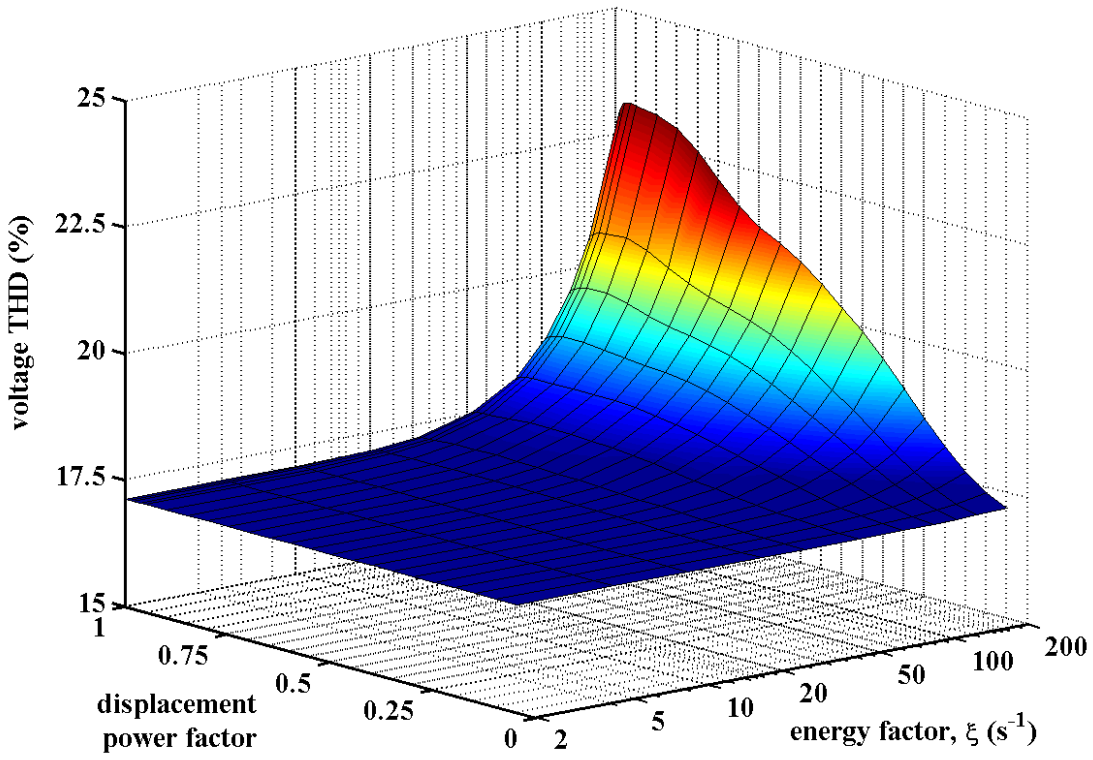


Figure 4.4.1: Contour of line voltage THD, m_a = 1.0, m_f = 60

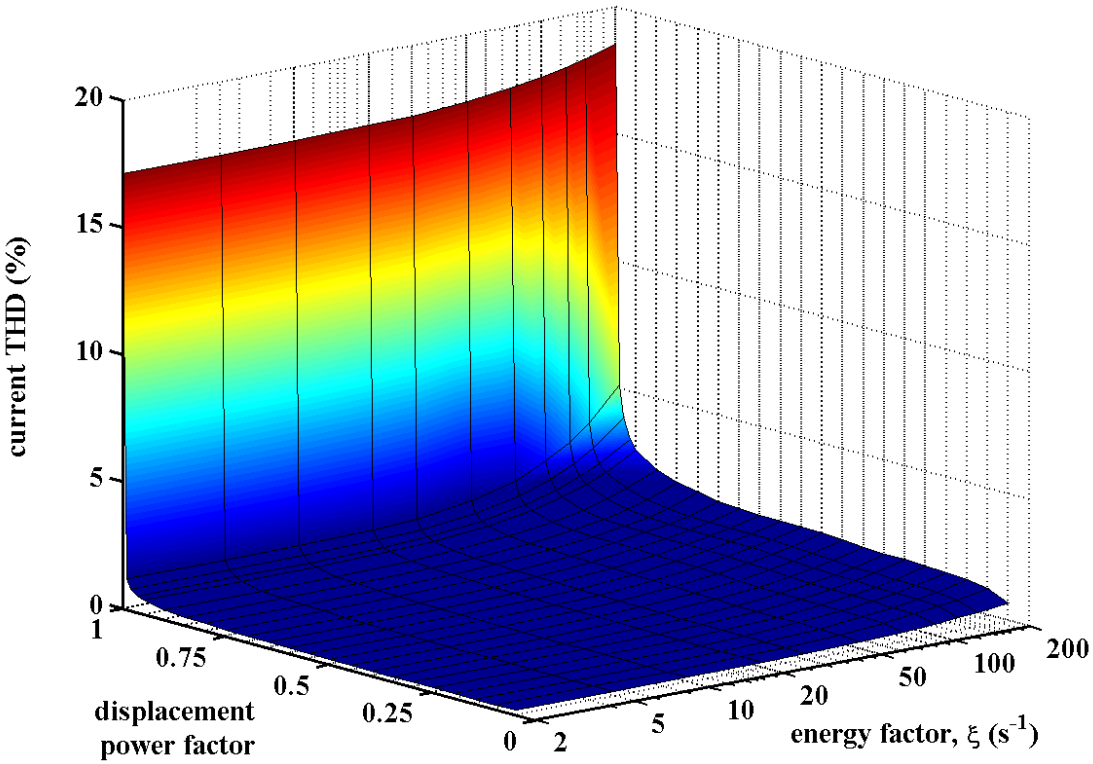


Figure 4.4.2: Contour of phase current THD, m_a = 1.0, m_f = 60

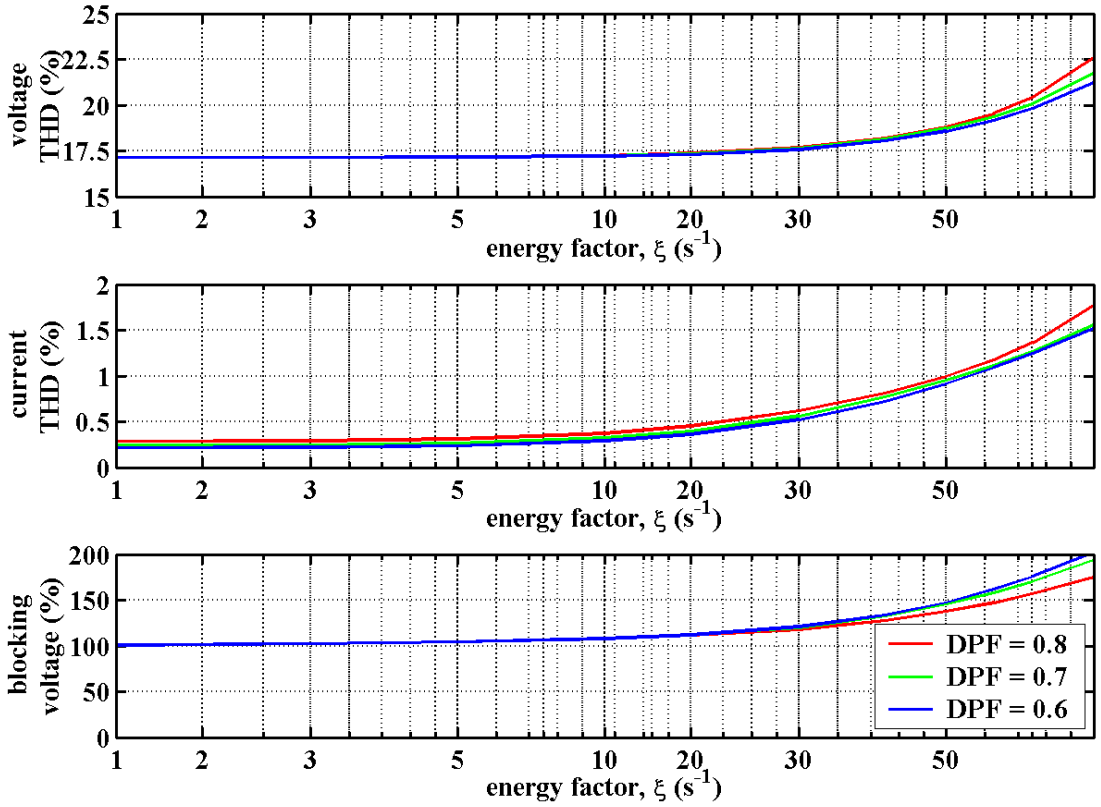


Figure 4.4.3: THD and blocking voltage variations with load, m_a = 1.0, m_f = 60

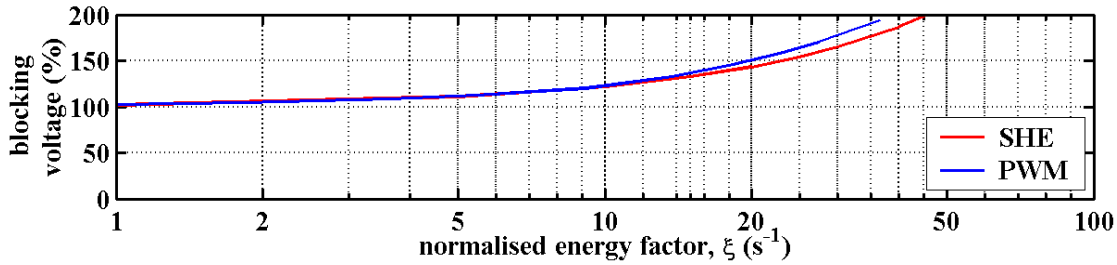


Figure 4.4.4: Blocking voltage variations comparison of SHE and PWM, displacement power factor = 0.8

4.4.2 Realistic Load Modelling

It is clear from the previous simulation using an ideal inductive load, that the filtering effect reduces the phase current THD to an unrealistic level compared to a practical system. To obtain a more realistic comparison of the different PWM carrier schemes, the generic ac machine model is used in the simulation instead of the RL load used in characterising the inverter's behaviour above.

To compare the difference this load model makes on simulated performance with the results presented in section 4.3, a load was used with 2 Ω for winding resistance and 6

mH for the leakage inductance. These values are consistent with a 1 kW induction motor model and machine parameter examples can be found in a book by Hindmarsh and Renfrew [4.19].

Non-linear effects such as saturation are ignored since the intention is to simulate the effect of the lower frequency behaviour on THD of the voltage and current waveforms. The computed phase angle θ has to be adjusted to take into account the phase delay in the phase voltage which the PWM reference sampling introduces. It is one half of the carrier period when the reference is symmetrically sampled and one quarter of the carrier period for asymmetric sampling i.e. 1.5° for the case of m_f= 60.

A simulation was run using asymmetric sampled PD PWM, with an ac motor load of 1 kW and a displacement power factor of 0.7. Figure 4.4.5 shows the predicted system waveforms which result from the simulation. As can be seen, there is no significant difference between the waveforms obtained early on the RL load and those using the generic ac load model, apart from the additional high frequency ripple now present on the phase current waveforms. The balancing of the cell capacitor voltages is working correctly and their mean voltages are within 1% of the target balanced voltage levels. The absolute maximum switch blocking voltage is 110.6% of the unit cell voltage.

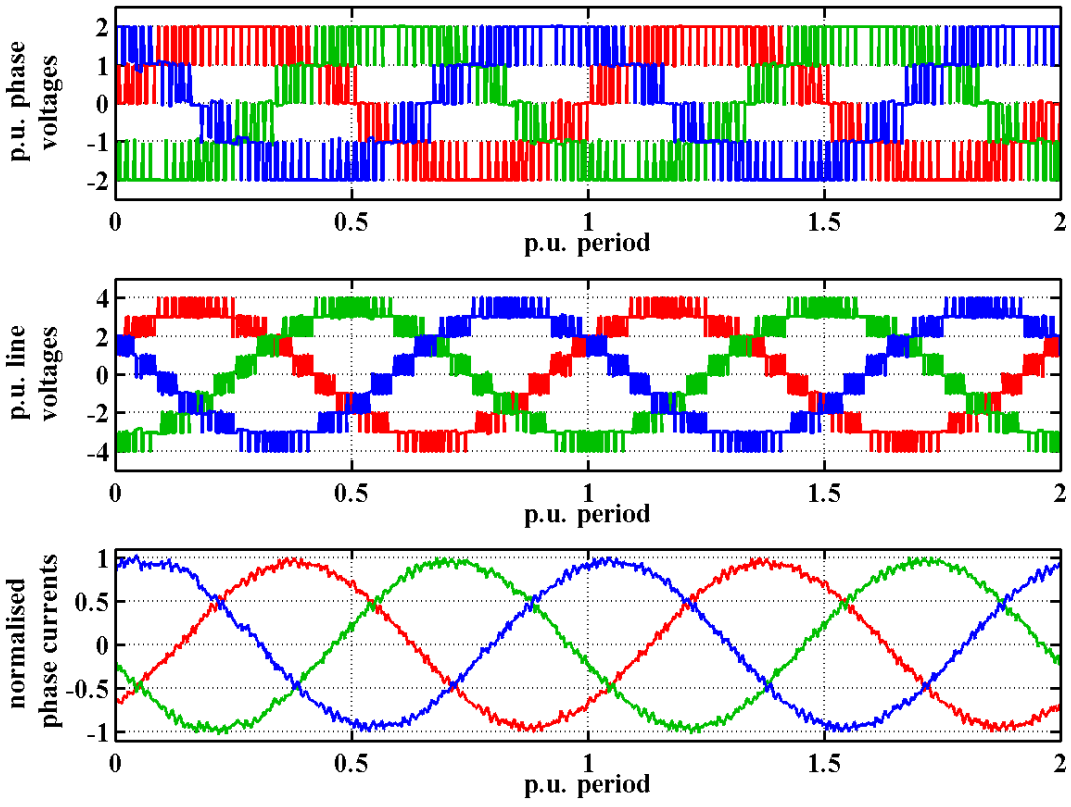


Figure 4.4.5: System waveforms for 1 kW, DPF = 0.7 ac load with asymmetric sampled PD PWM, m_a = 1, m_f = 60

The output spectra for the ac motor simulation are shown in Figure 4.4.6. These again show that are noticeable peaks at 15th and 30th harmonic of the fundamental, but more importantly, the filtering effect of the load is far more realistic to a real system. There are also some higher amplitude harmonics near the fundamental, which are sub- and inter-harmonics related to the overall balancing period of 4 cycles of the fundamental in this 4-cell inverter case. This is especially noticeable in the normalised phase current spectrum where some of the low frequency components are nearly 1% of the fundamental frequency component. This may cause problems in drive systems where the low frequency current harmonics can produce undesirable pulsating torques.

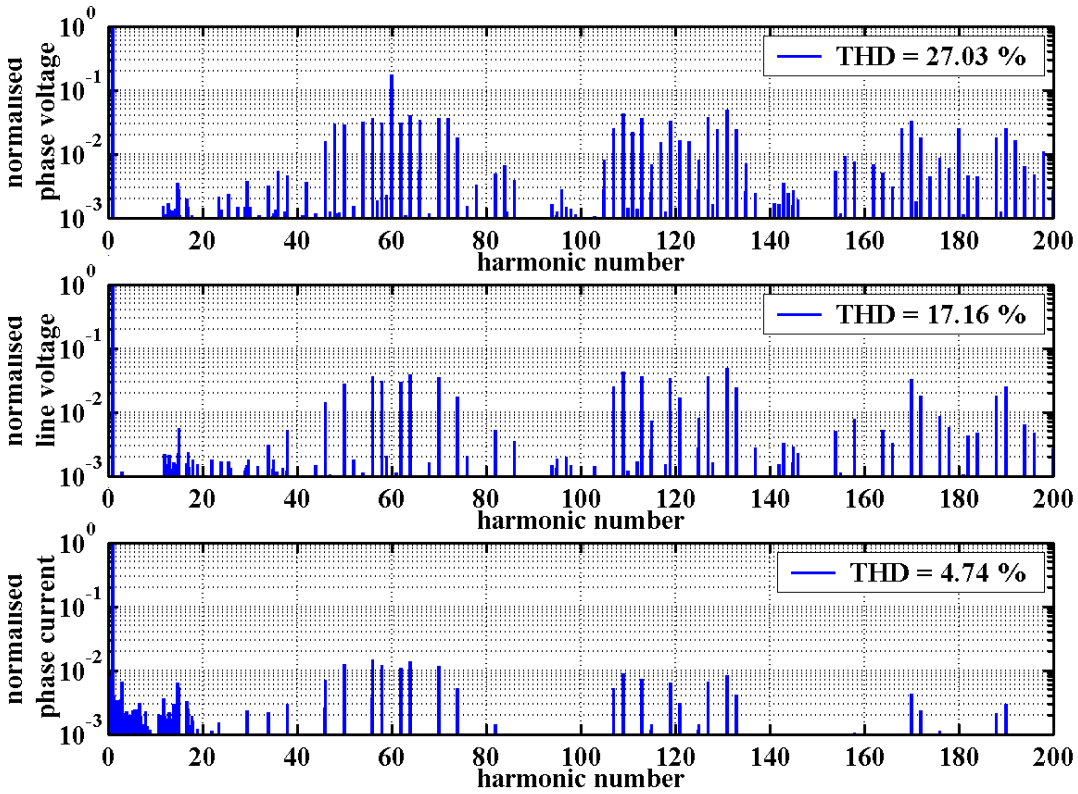


Figure 4.4.6: System spectra for 1 kW, DPF = 0.7 ac motor load with asymmetric sampled PD PWM, $m_a = 1$, $m_f = 60$

4.4.3 Influence of Different PWM Frequencies

A functional system balancing method has been developed and shown to work under simulated conditions with PWM control at one particular switching frequency (m_f = 60). The timing is critical for the balancing scheme to operate correctly and so the influence of different PWM frequencies needs to be assessed.

The ac load is selected for operation at the inverter maximum rating, defined by peak switch blocking voltage for $m_f = 60$. From the energy factor curves, the maximum $\xi = 100\ s^{-1}$ for a 0.7 power factor load. With unit cell voltage of 100 V, the maximum load power is 3.9 kW with the 1 mF unit cell capacitance to be used in prototype four-cell inverter. This means that a 5 hp induction motor load will not cause the inverter to operate outside operating limits imposed for the power switches. Typical values for a 5 hp induction motor are 0.5 Ω for winding resistance and 4 mH for the leakage inductance, and an equivalent displacement power factor is 0.8.

Simulations were performed with an FPGA clock frequency of 25 MHz with the m_f value stepped in increments of 3 from 30 to 498. This gives a switching frequency range of 1.5 kHz to 24.9 kHz with a fundamental of 50 Hz. Figure 4.4.7 shows the variation in output THD and maximum blocking voltage obtained from the simulations.

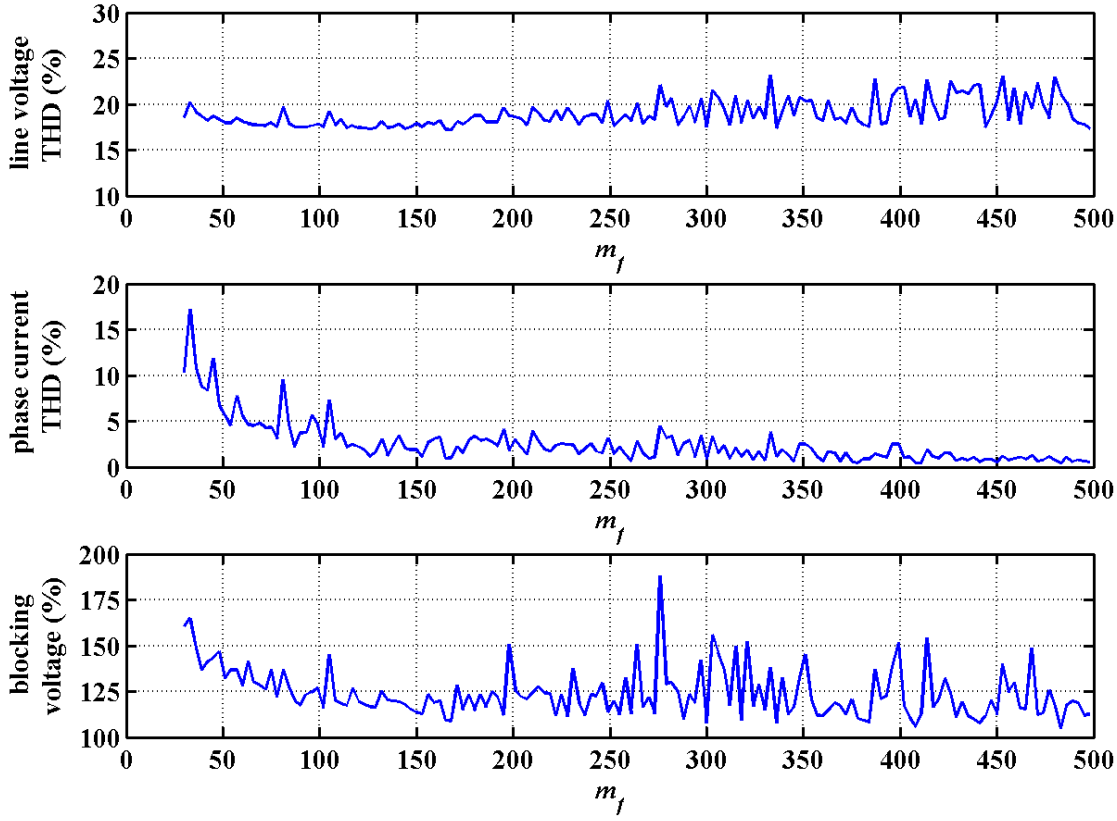


Figure 4.4.7: Variations in THD and blocking voltage over range of PWM frequencies

The general trend is inline with expectations, where phase current THD reduces with increasing frequency. However, these characteristic are not smooth but show perturbations, significant in the blocking voltage case, over the whole m_f range. The reason for this is the errors in the average duty cycles for each switch introduced by

the digital control implementation. Both the PWM carrier counters and the balancing clock counters will experience under-run because the maximum count values used are not always exact integer of the number of clock edges in one cycle.

To remove all bit errors in the implementation, the PWM logic clock should have a frequency which is a common multiple of both m_f and m_b. The alternative would be to adjust the fundamental period so that it meets the same criteria. This is not an attractive option especially if the inverter is grid-connected and the fundamental frequency fixed externally.

One solution is to use a technique employed in consumer audio-visual circuits. In digital set-top boxes the broadcaster sends period information regarding the transmit encoder 27 MHz clock. Each receiver transport processor uses this information to adjust its own voltage controlled oscillator crystal (VCOX) clock. This provides synchronism to digital transport stream audio and video components and ensures sound synchronisation with the displayed picture. Figure 4.4.8 shows an example of a possible VCOX clock circuit which can be used in a master DSP control plus FPGA implementation of a PWM/balancing controller.

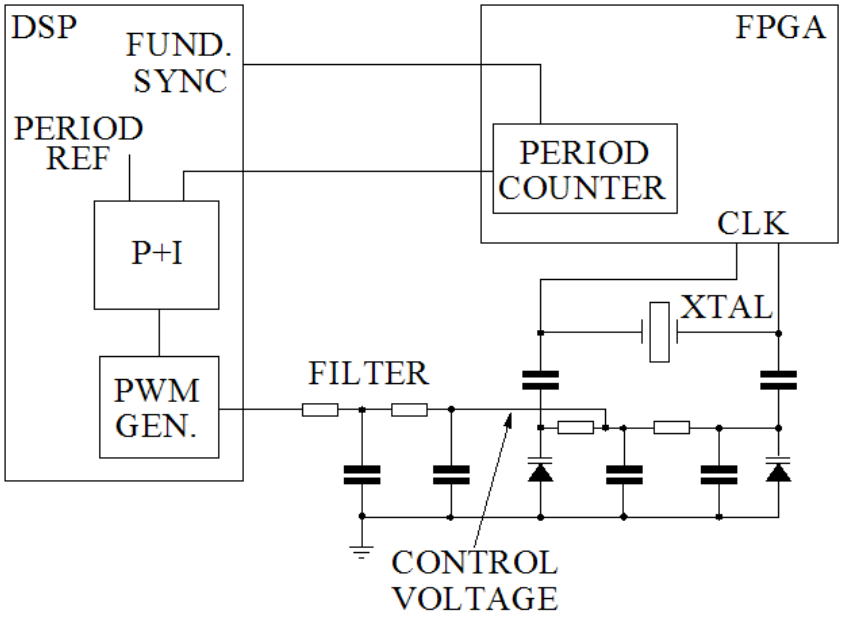


Figure 4.4.8: PWM controlled FPGA clock circuit

The DSP sends a fundamental period pulse steam to the FPGA which is used to set the start of each reference cycle. These pulses are used to enable a counter which clocks on every edge of the FPGA clock. At the end of a period this information is passed back to the DSP and used as an input to an error amplifier with the desired clock

period used as reference. A proportional plus integral controller can then be used to adjust the duty of a PWM output, which in turn is filtered externally and used as the controlling voltage to variable capacitance PIN diodes. The closed-loop control should then adjust the clock to the desired value. The circuit can be designed to offer clock frequency ranges with up to 50 % variation [4.20], which is more than adequate for the practical PWM switching frequencies required. This VCOX approached was simulated over the whole range of m_f values. The results appear impressive as can be seen in Figure 4.4.9.

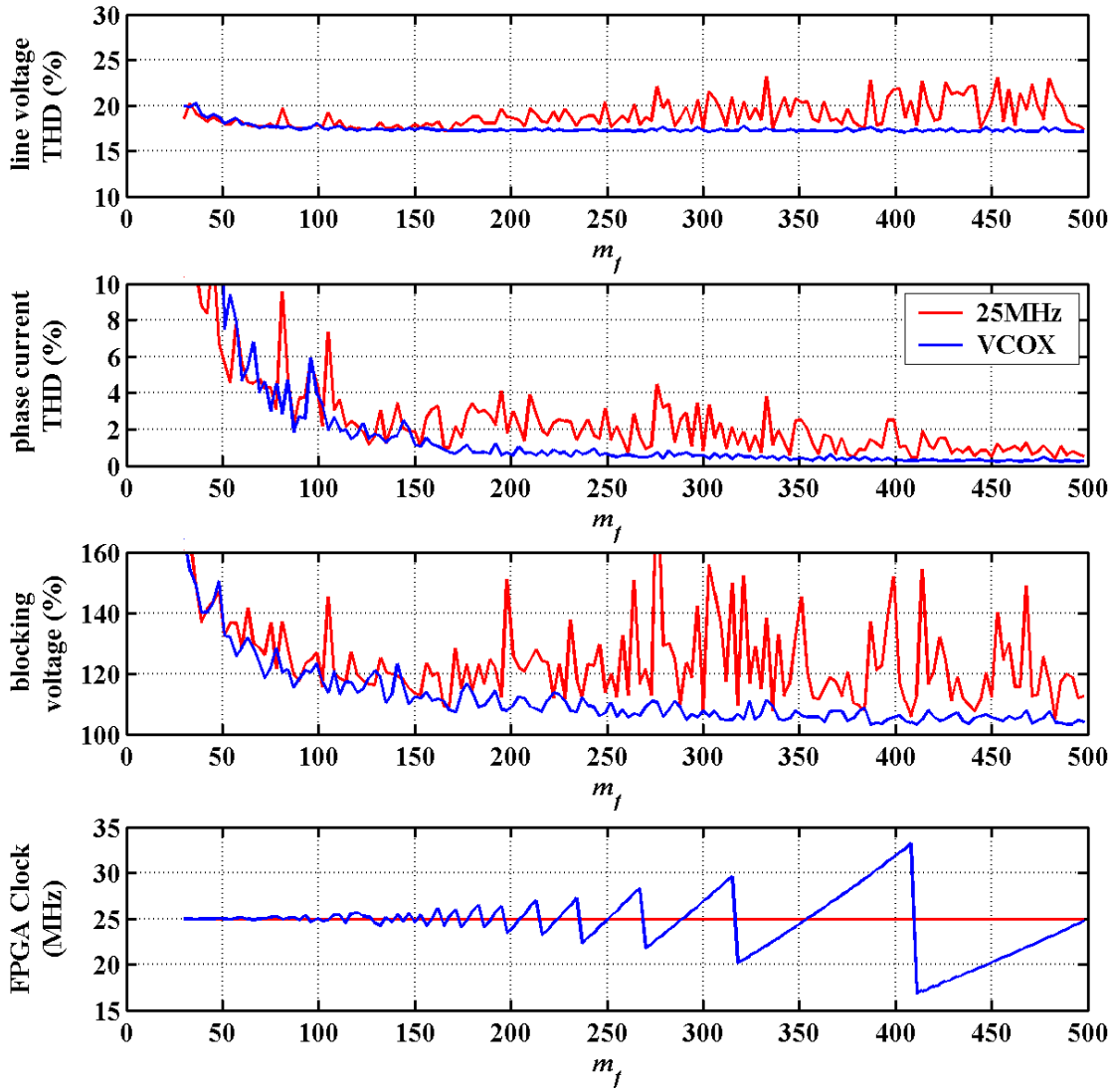


Figure 4.4.9: Variations in THD and blocking voltage over range of PWM frequencies with VCOX clock

The characteristics are far smoother with only slight variations, apart from at low switching frequency. The characteristics do show that by increasing the switching frequency above 10 kHz (m_f = 200 for a 50 Hz fundamental) only small incremental

gains are achieved in output power quality under these particular load and inverter capacitor sizing. However, in some systems high frequency switching is preferred because of acoustic noise issues, although this may lead to problems in containing both conducted and radiated radio frequency interference (RFI).

The reason for the slight variations in blocking voltage and the resultant perturbations in the phase current THD are due the introduction of low frequency components in the cell capacitor voltages. This is due to small duty cycle errors in each cycle even though over the complete balancing four cycle period the errors are averaged out.

4.4.4 Influence of FPGA Clock

Practical performance limitations due to a digital implementation of PWM are known issues and been investigated in the past for standard sine-triangle PWM [4.21, 4.22]. This section investigates the impact of lower digital clock frequencies, especially in respect to the instability issues highlighted in the last section.

The proposed implementation of the multicarrier PWM schemes has a fixed clock for the triangle carrier counter, which means that the maximum count varies if either the frequency modulation index, m_f, or the fundamental frequency is changed. To minimise errors and potential instability in the balanced control system, the master FPGA clock is frequency is locked to ensure the counters for both the triangular carriers and the balancing scheme are zero at the completion of one balanced cycle.

This approach can be applied to the control design with nominal clock frequencies other than the 25 MHz referred to in the above section. Lower frequency clocks will reduce the bit resolution of the sine-triangle comparison and can lead to a reduction in inverter performance. Using the example of an inverter control with an output fundamental of 50 Hz and a switching frequency of 9 kHz (m_f = 180), a VCOX clock can be used in incremental steps of 3.222 MHz. The formula for computing this frequency increment is given by

$$CLK_{\min} = 2m_f \left(m_f - 1\right) f_o \qquad \ldots (4.4.3)$$

The resultant variation in performance is illustrated in Figure 4.4.10. The load is set to 3.75 kW as before with m_a = 1. Even at the lowest clock frequency for this particular control modulation set-up, the performance of the inverter is not reduced significantly. There is only a small percentage reduction in the actual amplitude of the fundamental voltage component and the THD of the line voltage is almost constant over different clock frequencies. However, the simulated phase current THD does reduce slightly with increased digital logic clock frequencies.

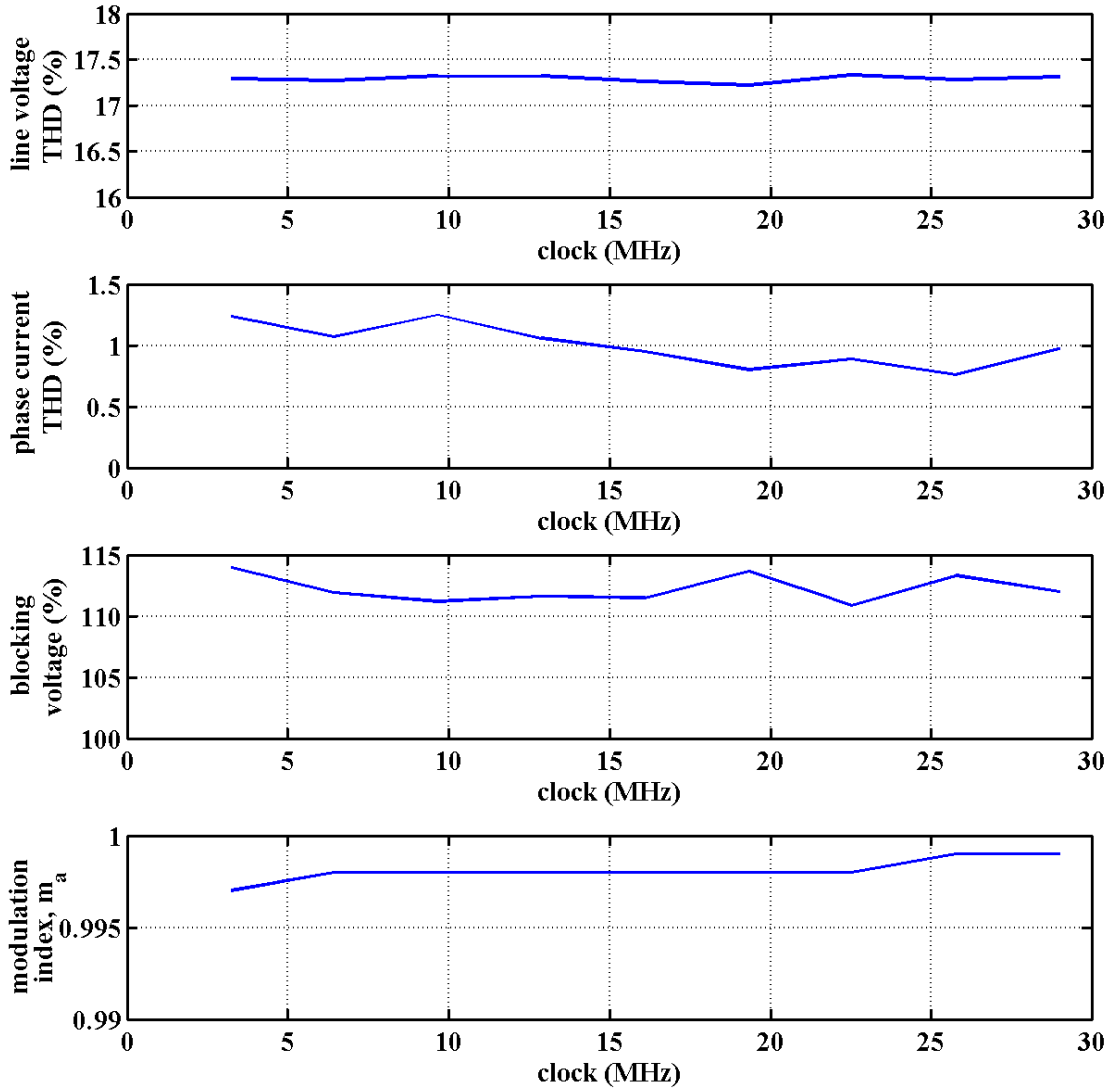


Figure 4.4.10: Variation in inverter performance for different FPGA clocks

4.4.5 Influence of Inverter Dead-Time

Dead-time is defined as the period when the inverter's cell switches are in the inert state and is sometimes referred to as the blanking-time. The timing diagram for the modulation system is shown in Figure 4.4.11. It is necessary in a real inverter to avoid shoot-through in the switch pair adjacent to the load and to stop shorting together of two adjacent cell capacitors in the upper voltage level cells. The dead-time is usually fixed by the control logic, but there is also a delay term introduced by the switching speed of the power switches and if optically isolated, the speed of the optocoupler. This analysis will focus on fixed dead-times introduction by the control logic since any gate driver delays are likely to be much smaller in practice.

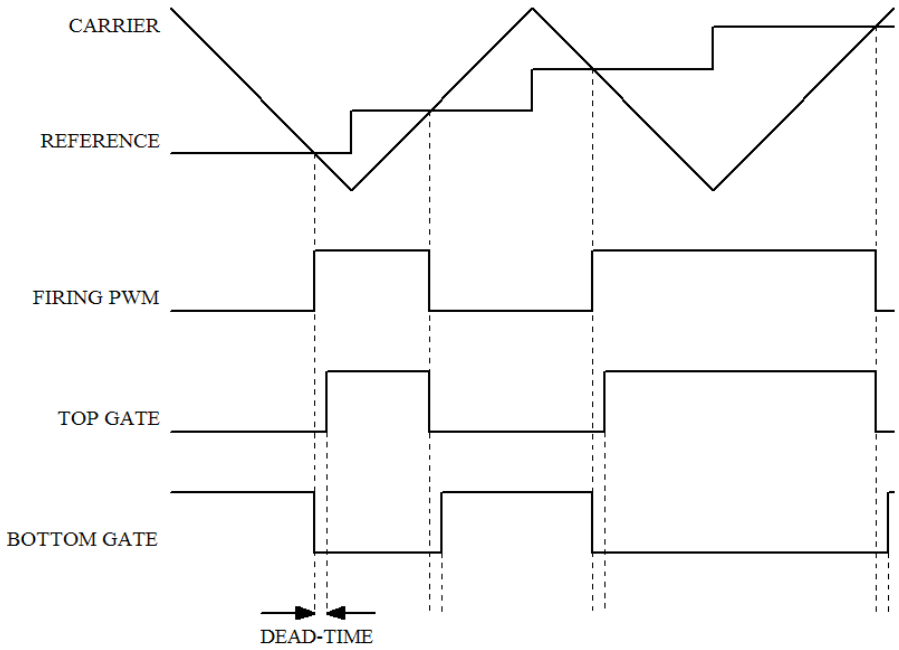


Figure 4.4.11: Modulation timing diagram including dead-time blanking

The path taken by any load current flowing through the inverter is dependent on its polarity when the inverter cell IGBTs are both turned off. If immediately before the top IGBT is turned off, the current flowing in the IGBT/diode switch pair is negative polarity then this current will keep on flowing through the top diode during the dead-time until the bottom IGBT of the inverter cell is turned-on. The net result is an extension of the period of voltage level contribution to the output voltage. If the current is positive polarity, then the output voltage drops one level immediately. The result is that it will modify the output voltage amplitude and phase. This is of particular concern in ac motor drives since the dead-time distortion is more pronounced at low modulation depths, which is a control requirement when operating at low speed (low fundamental frequency). There has been significant work done on compensating for this effect in standard inverters [4.23, 4.24]. The dead-time also introduces distortion in the phase current around the zero-crossing and this too has been investigated in the past [4.25].

An added complication in the case of the balancing swapping of modes in the flying-capacitor inverter, the output voltage can actually drop and increase by one level where two cells are put into the inert state. The voltage level change occurs when there is a switching transition and more than two-cells are changing state due to the balancing algorithm with both cells briefly put into an inert state during the dead-time. If the current is positive then the bottom diode in the inert cell will conduct reducing the level, otherwise the top diode will conduct when the current is negative. Figure 4.4.12 shows a comparison of the phase voltage and current waveforms for no dead-

time and fixed dead-time, to highlight this level jumping. The bottom current waveform also shows the distortion introduced by the dead-time control. The simulated waveforms were produced for a low m_f and large dead-time to exaggerate the effect.

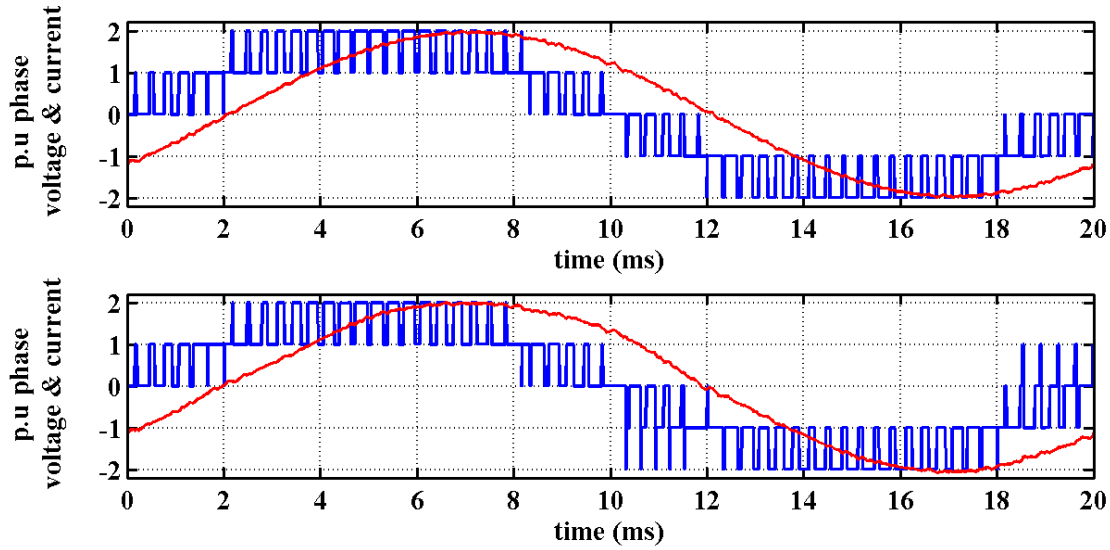


Figure 4.4.12: Comparison of effect on phase voltage and current of no dead-time (top) and with a 20 µs dead-time (bottom)

To quantify the effect of the dead-time value on inverter output performance, simulations are conducted under realistic load conditions. With the cell-capacitance fixed at 1 mF and using a 400 V dc link, the generic 3.75 kW, DPF = 0.8 inductive load is used for further comparison of the control and system issues. It has been seen that performance improvements at higher operating frequencies are only slight, and the sensible approach would be to keep the PWM frequency as low as possible to limit the switching losses in the power converter switches and reduce any possible EMC problems. Therefore, a PWM switching frequency of 9 kHz is used which equates to an m_f = 180 when synthesising a 50 Hz fundamental.

Figure 4.4.13 illustrates the variation in system performance as dead-time is increased. There is a deterioration in the phase current THD due to the distortion in the phase current waveform seen above, which introduces increased low frequency harmonics. The curves also show the effect on modulation depth which will need to be compensated for in practical closed-loop system. This can be achieved by the closed-loop voltage controller adjusting the reference amplitude demand.

The output spectra shown in Figure 4.4.14 illustrates clearly the increased levels in the base-band frequency components caused by the introduction of the dead-time in the inverter firing commands.

Therefore the dead-time should be selected to be as short as possible, and will depend on the switching characteristics of the power electronic devices.

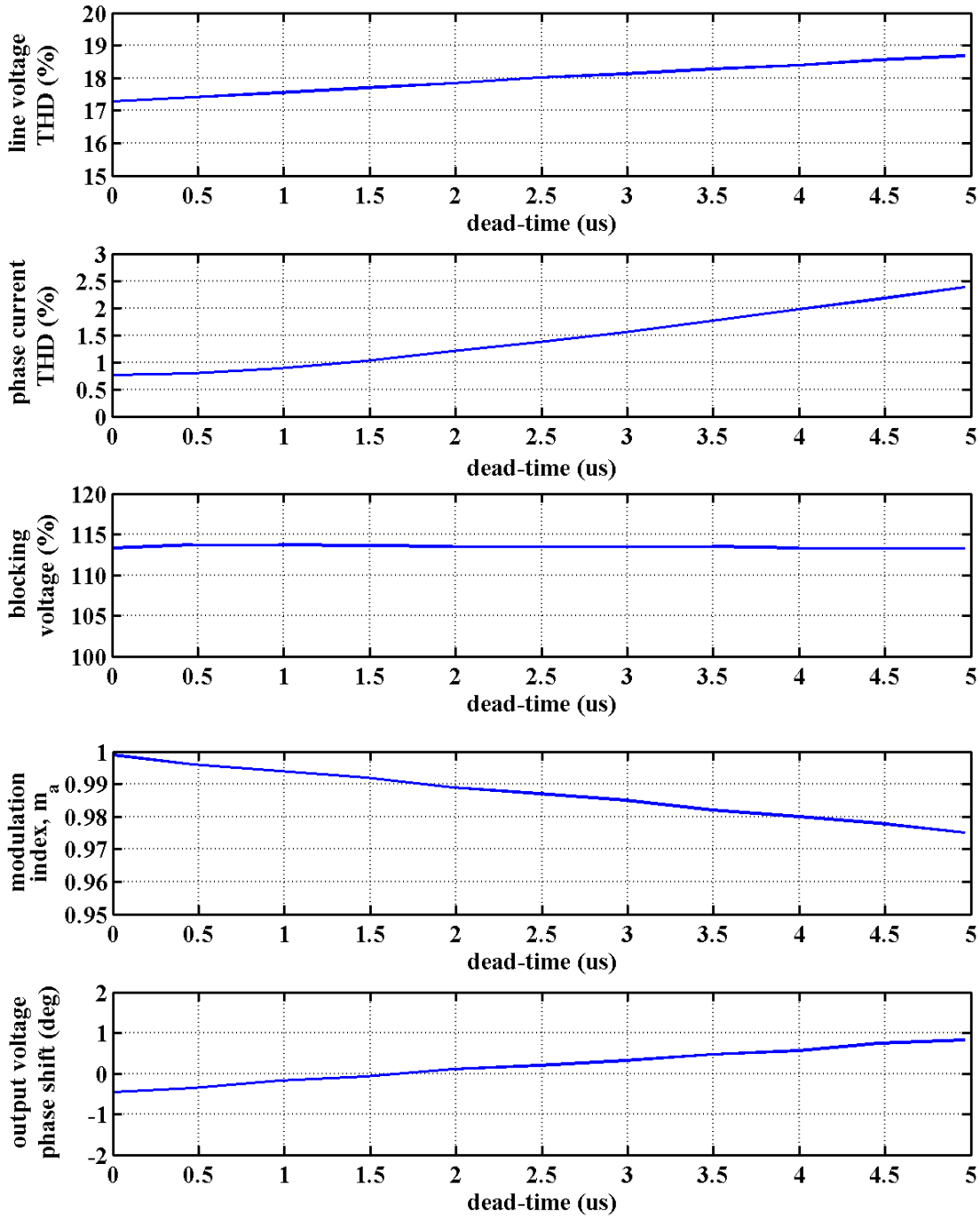


Figure 4.4.13: THD, blocking voltage and modulation parameter variations with dead-time

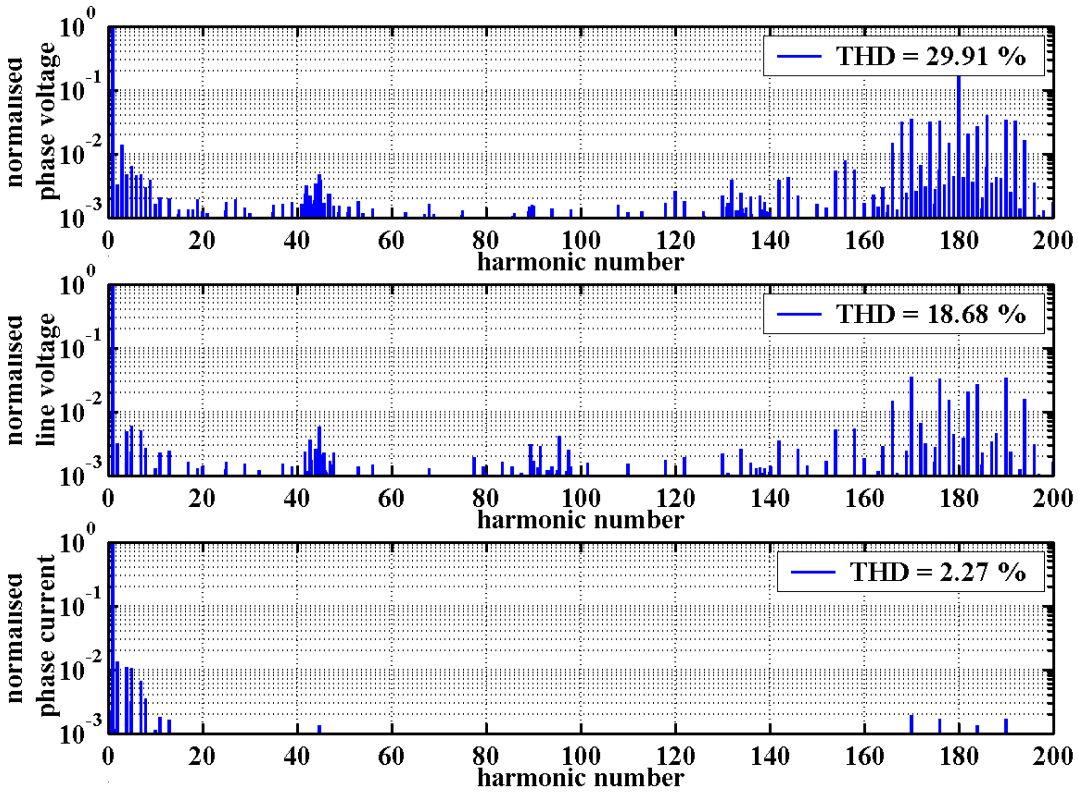


Figure 4.4.14: Voltage and current spectra for m_f = 180, m_a = 1 and 5 µs dead-time

4.5 Practical System Performance Comparison

The simulations so far have focussed on the individual issues of loading, control and inverter component selection, and the effect on system balancing, output power quality and inverter reliability. Earlier in this chapter the wide variety of different carrier placement strategies for multilevel sine-triangle PWM were discussed and their relative merits compared by reference to the ideal output voltage case. A more detailed comparison can now be performed by using a simulation of a practical inverter with real switches.

The inverter components and control settings for comparing the different PWM carrier schemes are listed in Table 4.5.1. A higher operating switching frequency allows a greater output power to be supplied compared to SHE control. The simulated three-phase load requires a total active power of 3.75 kW and has a fundamental frequency DPF of 0.8. Given that there is a trade-off between higher switching frequency and power dissipation in the semiconductor switches, a switching frequency of 3 kHz is selected for synthesising a 50 Hz fundamental output sinusoidal voltage. VCOX FPGA clock control is assumed at a value of 25.134 MHz.

Parameter	Value
DC Link Voltage	400 Vdc
IGBT/Diode	IRG4PC30KD (30 A/600 V)
Unit Cell-Capacitance	1 mF
Load Inductance	4 mH
Load Resistance	0.5 Ω
Load Active Power	3.75 kW
Displacement Power Factor	0.8
Fundamental Frequency	50 Hz
Switching Frequency	3 kHz (m_f = 60)
Dead-Time	3 μs

Table 4.5.1: Simulator settings for PWM scheme comparison

Simulations were run on all forms of PWM carrier scheme including the third harmonic injection approach used for achieving higher modulation depths. Table 4.5.2 lists the different control schemes and the resultant operating parameters of the system. Even though the simulation target m_a value is unity, the actual m_a = 0.97 in all cases. This reduction is due to the combined effect of the 3 μs dead-time and the voltage drop across each power switch. The individual PWM carrier schemes do not affect the output voltage amplitude of the fundamental. Note that the true power factor is less than the ideal 0.8 in each case because of the harmonic content in each phase voltage and current. The third harmonic injection methods results in a reduced overall power factor because of the additional 3rd harmonic term in the phase voltage. The predicted electronic losses are broadly the same for all schemes, showing that the different carrier placements do not influence the losses.

Scheme	m_a	Phase Voltage (Vrms)	Phase Current (Arms)	Line Voltage (Vrms)	TPF	Output Power (kW)	Power Loss (W)
PD	0.97	142.7	11.5	241.8	0.78	3.83	189
POD	0.97	142.8	11.5	244.1	0.77	3.80	189
APOD	0.97	142.8	11.3	246.6	0.77	3.74	187
PS/HPS	0.97	142.8	11.4	246.4	0.77	3.75	187
SPD	0.97	142.7	11.5	243.4	0.78	3.83	188
SPOD	0.97	143.0	11.3	245.2	0.77	3.71	185
DPS	0.97	143.2	115	244.7	0.76	3.71	188
PD + 1/6th	0.97	146.7	11.3	241.9	0.74	3.70	186
PD + 1/4th	0.97	149.3	11.3	242.4	0.73	3.69	185

Table 4.5.2: Output performance comparison of different schemes (m_f = 60)

The output harmonic performance for each scheme is compared in Table 4.5.3. The simulation data shows that the PD scheme results in the lowest line voltage THD, whilst the APOD results in the highest, although the phase current THD figures are broadly similar and will be more dependent on switching frequency and the load filtering characteristic. The increased harmonic content of the phase voltage shown in the 3rd harmonic injected schemes does not adversely affect the line voltage and phase current harmonic content since the extra triplen harmonic is cancelled in the three-phase load.

Scheme	Phase Voltage THD (%)	Line Voltage THD (%)	Phase Current THD (%)
PD	28.91	18.83	5.38
POD	28.72	23.22	6.60
APOD	28.82	27.06	4.76
PS/HPS	28.60	27.01	4.94
SPD	29.02	22.28	6.49
SPOD	29.19	24.34	5.30
DPS	29.08	23.12	7.79
PD + 1/6th	37.33	18.63	4.43
PD + 1/4th	42.26	18.73	4.76

Table 4.5.3: Output distortion comparison of different carrier schemes (m_f = 60)

Table 4.5.4 presents the simulated parameters associated with the capacitors and electronic switches. These values illustrate how well the system is balanced for each carrier scheme. Interestingly, the poorer harmonic performance of the APOD is not related to higher capacitor ripple since the maximum blocking voltage in this case is the lowest of all the schemes. A higher blocking voltage and a larger maximum power loss in one of the switches indicate a poorer balanced operation in the POD and DPS cases.

Scheme	**Cell Voltages (V)**			**Max. Switch (V)**	**Cap. Current (Arms)**	**Peak Power Loss**		
						IGBT (W)	**Diode (W)**	**Trans. (W)**
PD	102.1	200.5	302.1	126.9	5.57	6.57	1.41	0.15
POD	99.9	201.6	301.0	139.9	5.59	6.72	1.45	0.15
APOD	100.2	199.7	299.8	114.5	5.50	6.18	1.36	0.15
PS/HPS	98.7	197.4	299.7	122.5	5.54	6.36	1.36	0.15
SPD	99.5	200.3	301.2	131.1	5.52	6.48	1.36	0.16
SPOD	99.9	201.5	300.3	130.8	5.45	6.44	1.34	0.15
DPS	97.1	202.1	294.7	132.3	5.58	7.13	1.64	0.17
PD + 1/6th	102.1	200.5	301.4	130.9	5.57	6.42	1.36	0.16
PD + 1/4th	99.5	199.1	298.6	128.6	5.52	6.48	1.40	0.16

Table 4.5.4: Phase balancing performance comparison of different carrier schemes

Finally, the variation in predicted power losses and harmonic distortion at different switching frequencies was assessed by simulating the inverter operating with PD PWM at a much higher link voltage and load power. The dc link voltage was set to 1600 V and a 30 kW, 0.8 DPF load model used. This increases the switching loss component of the total electronics losses. As can be seen from Table 4.5.5, the switching losses show a linear increase as a function of the switching frequency. The harmonic distortion also shows an improvement as the switching frequency is increased. The peak blocking voltage also reduces slightly at higher switching frequencies.

Switch Freq. (kHz)	Harmonic Distortion			Max. Block Voltage (V)	Power Losses			
	Phase Voltage THD (%)	Line Voltage THD (%)	Phase Current THD (%)		Max. IGBT Loss (W)	Max. Diode Loss (W)	Max. Switch Loss (W)	Total System Losses (W)
5	27.15	17.26	2.70	442.3	12.51	3.43	0.80	391
10	27.03	17.01	1.44	429.5	12.29	3.30	1.61	410
15	26.86	16.85	0.98	411.5	12.23	3.30	2.38	428
20	26.72	16.72	0.86	415.1	12.24	3.31	3.23	446
25	26.63	16.66	0.80	410.0	12.22	3.30	4.02	464

Table 4.5.5: Effect of switching frequency on performance

4.6 Conclusions

This chapter has shown that there are a wide variety of different sine-triangle PWM implementations, which all result in generally good overall performance. A detailed analysis of the different schemes has been presented, including specific practical issues such as dead-time effects and digital-logic clock frequency limitations. A detailed comparison of the different multicarrier PWM approaches has been performed by simulation on a realistic inverter model, so that the influence of the inverter and load parameters, and more importantly the cell-capacitors could be assessed.

The simulations have revealed that the phase disposed (PD) carrier placement scheme potentially offers the best performance even with realistically sized cell-capacitors. However, when there is significant capacitor voltage variation, then the resultant lower frequency components dominate the unwanted harmonic content of the phase current, and therefore there is less to choose between schemes.

A novel digital hardware balancing control scheme for the flying-capacitor inverter has been proposed that will operate correctly regardless of which PWM control scheme is being used. Simulations have revealed, however, that the performance is very susceptible to timing errors in the system, and a method has been verified which can be implemented and used to reduce these effects. The VCOX control of the FPGA clock is easy to implement. This type of circuit is already an integral part of many home entertainment appliances, but it is a novel approach to control timing accuracy in a power converter system.

The flying-capacitor inverter performance characteristics have been normalised in terms of the energy factor and load displacement power factor. This information can then be used in the design of a real inverter, and is of specific value in optimising the

inverter for the target load and ensuring that the size and cost of the cell-capacitors is minimised.

4.7 References

[4.1] Bowes, S.R., "Pulse-width modulated inverter systems", DSc Collection of Papers, University of Leeds, UK, 1985.

[4.2] Zubek, J., Abbondanti, A. and Norby, C.J., "Pulsewidth modulated inverter motor driven with improved modulation", IEEE Transactions on Industry Applications, Vol. IA-11, No. 6, November/December 1975, pp. 695 – 703.

[4.3] Boost, M.A. and Ziogas, P.D., "State-of-the-art carrier PWM techniques: a critical evaluation", IEEE Transactions on Industry Applications, Vol. 24, No. 2, March/April 1988, pp. 271 – 280.

[4.4] Massoud, A.M., Finney, S.J. and Williams, B.W., "Control techniques for multilevel voltage source inverters", Proceedings of PESC '03, 34th IEEE Power Electronics Specialists Conference, 15 - 19 June, 2003, Vol. 1, pp. 171 – 176.

[4.5] Mohan, N., Undeland, T.M. and Robbins, W.P., "Power electronics. Converters, applications, and design", John Wiley & Sons, Inc., New York, USA, 3rd Edition, 2003, ISBN 0-471-22693-9.

[4.6] H Holmes, D.G. and Lipo, T.A., "Pulse width modulation for power converters. Principles and practice", Wiley-IEEE Press Series on Power Engineering, 2003, ISBN 0-471-20814-0.

[4.7] Velaerts, B., Mathys, P., Tatakis, E. and Bingen, G., "A novel approach to the generation and optimization of three-level PWM wave forms for induction motor inverters", PESC '88 Record, 19th Annual IEEE Power Electronics Specialists Conference, 11 - 14 April, 1988, Vol. 2, pp. 1255 – 1262.

[4.8] Carrara, G., Gardella, S., Marchesoni, M, Salutari, R. and Sciutto, G., "A new multilevel PWM method: a theoretical analysis", PESC '90 Record, 21st Annual IEEE Power Electronics Specialists Conference, 11 - 14 June, 1990, pp. 363 – 371.

[4.9] Meynard, T.A., Foch, H., Thomas, P., Courault, J., Jakob, R., Nahrstaedt, M., "Multicell converters: basic concepts and industry applications", IEEE

Transactions on Industrial Electronics, Vol. 49, No. 5, October, 2002, pp. 955 – 964.

[4.10] Tolbert, L.M. and Habetler, T.G., “Novel multilevel inverter carrier-based PWM methods”, Conference Record of IAS '98, the 1998 IEEE Industry Applications Society 33rd Annual Meeting, 12 - 15 October, 1998, Vol. 2, pp. 1424 – 1431.

[4.11] Menzies, R.W. and Zhuang, Y.-P., “Advanced static compensation using a multilevel GTO thyristor inverter”, IEEE Transactions on Power Delivery, Vol. 10, No. 2, April, 1995, pp. 732 – 738.

[4.12] Agelidis, V.G. and Calais, M., "Application specific harmonic performance evaluation of multicarrier PWM techniques", PESC '98 Record, 29th Annual IEEE Power Electronics Specialists Conference, 17 - 22 May, 1998, Vol. 1, pp 172 - 178.

[4.13] McGrath, B.P. and Holmes, D.G., “A comparison of multicarrier PWM strategies for cascaded and neutral point clamped multilevel inverters”, Proceedings of PESC 2000, 31st Annual IEEE Power Electronics Specialists Conference, 18 - 23 June, 2000, Vol. 2, pp. 674 – 679.

[4.14] Hava, A.M., “Carrier based PWM-VSI drives in the overmodulation region”, PhD Thesis, University of Wisconsin-Madison, Madison, WI, USA, December 1998.

[4.15] Hava, A.M., Kerkham, R.J. and Lipo, T.A., “Carrier-based PWM-VSI overmodulation strategies: analysis, comparison and design”, IEEE Transactions on Power Electronics, Vol. 13, No. 4, July 1998, pp. 674 – 689.

[4.16] Houldsworth, J.A. and Grant, D.A., “The use of harmonic distortion to increase the output of a three-phase PWM inverter”, IEEE Transactions on Industry Applications, Vol. IA-20, No. 5, September/October 1984, pp. 1224 – 1228.

[4.17] Bonert, R. and Wu, R.S., “Improved three phase pulse width modulator for over modulation”, Conference Record of IAS '84, the 1984 IEEE Industry Applications Society 19th Annual Meeting, 30 September - 4 October, 1984, pp. 784 – 786.

[4.18] Bowes, S.R. and Mount, M.J., “Microprocessor control of PWM inverters”, IEE Proceedings, Vol. 128, Part B, No. 6, November 1981, pp. 293 – 305.

[4.19] Hindmarsh, J. and Renfrew, A., “Electrical machines and drive systems”, Butterworth-Heinemann, Oxford, UK, 3rd Edition, 1996, ISBN 0 7506 2724 7.

[4.20] Ware, K.M., Lee, H.-S. and Sodini, C.G, "A 200-MHz CMOS phase-locked loop with dual phase detectors", IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, Dec. 1989, pp. 1560 - 1568.

[4.21] Grant, D.A., Stevens, M. and Houldsworth, J.A., “The effect of word length on the harmonic content of microprocessor-based PWM waveform generators”, IEEE Transactions on Industry Applications, Vol. IA-21, No. 1, January/February 1985, pp. 218 – 225.

[4.22] Zmood, D. and Holmes, D.G., “Practical performance limitations for PWM strategies”, Conference Record of IAS '98, the 1998 IEEE Industry Applications Society 33rd Annual Meeting, 12 - 15 October, 1998, Vol. 2, pp. 1245 – 1252.

[4.23] Jeong, S.G. and Park, M.-H., “The analysis and compensation of dead-time effects in PWM inverters”, IEEE Transactions on Industrial Electronics, Vol. 38, No. 2, April 1991, pp. 108 – 114.

[4.24] Pedersen, J.K. and Blaabjerg, F., “Blanking-time and on-state compensation in a PWM-VSI inverter with one current sensor only”, Proceedings of SPEEDAM ’94, Symposium on Power Electronics, Electrical Drives, Advanced Electrical Motors, 8 - 10 June, 1994, Vol. 1, pp. 267 – 272.

[4.25] Summers, T. and Betz, R.E., “Dead-time issues in predictive current control”, Conference Record of IAS ’02, the 37th IEEE Industry Applications Annual Meeting, Pittsburgh, USA, 13 – 18 October, 2002, Vol. 3, pp. 2086 – 2093.

Chapter 5 SPACE VECTOR PWM

5.1 Introduction

The space vector PWM (SVPWM) [5.1] is an alternative method used to control three-phase inverters, where the PWM duty cycles are computed rather than derived through hardware comparison like sine-triangle PWM reviewed in detail in Chapter 4. In SVPWM, the three-phase stationary reference frame voltages for each inverter switching state are mapped to the complex two-phase orthogonal α-β plane. The reference voltage is represented as a vector in this plane and duty-cycles are computed for the selected switching state vectors in proximity to the reference. In multilevel inverters, the number of switching state vectors increases and this additional complexity has prompted many attempts at optimizing the performance of the SVPWM method for multilevel inverters.

This chapter focuses specifically on one simple multilevel SVPWM scheme which is relatively easy to implement in hardware. The aim is do a direct comparison with the other forms of control when applied to the flying-capacitor inverter.

5.2 Space-Vector Representation

Space vector modulation was developed from the concept that a set of three-phase waveforms can be represented by a single rotating vector. One of the earliest proposed modulation strategies to use this concept was by Murai et al. [5.2]. Space vector PWM developed fully in the late 1980s through the work of various researchers, notably Van der Broeck [5.3]. It was also applied to three-level inverters at that time through the work of Steinke [5.4] and Bauer and Heining [5.5].

The application of SVPWM to multilevel inverters developed throughout the 1990s with various schemes proposed in the literature. The larger number of switching states in a multilevel inverter proved challenging in developing optimum algorithms for the computation of duty cycles and selection of switching states at the different voltage levels. Lee et al. from Hanyang University [5.6] proposed a method of duty cycle computation which was based on the individual triangular regions between the multilevel switching states. A similar approach is been adopted for a generalised SVPWM algorithm developed by Wei, et al. from Ryerson University [5.7] which is aimed at the control of cascaded-cell multilevel inverters. An alternative computation

algorithm for computing the duty cycles has been proposed by Peng et al. from Virginia Polytechnic and State University [5.8].

Zhang et al. from Oregon State University [5.9] investigated switching state selection in order to eliminate common-mode voltages. Li et al. from two New York State universities [5.10] developed a multilevel SVPWM scheme by creating two phase shifted vectors to represent the actual reference vector. They developed this algorithm specifically for the cascaded-cell multilevel inverter where the requirements for cell-capacitor voltage balancing are not present. Also of interest is the work of Filho et al. [5.11], who have applied artificial neural networks (ANN) to the problem of sector identification and duty cycle computation.

It has been appreciated since the beginning of SVPWM development that there is a correlation between the carrier-based PWM scheme and SVPWM [5.12]. Boys and Handley [5.13] analysed the equivalent SVPWM reference showing it has the form of a sinusoid injected with a triangular signal. Wu et al. [5.14] have investigated this relationship concerning a multilevel implementation.

Meynard's group at Toulouse [5.15] have used SVPWM in the control of a flying-capacitor inverter used in an induction motor drive. Voltage balancing is achieved through voltage sensors which change the switching state depending on the voltage level demand from the SVPWM algorithm. Brazilian researchers Mendes et al. [5.16] have been investigating multilevel SVPWM and have demonstrated its application to a two-cell flying-capacitor inverter. The cell-capacitor voltage balancing is achieved by monitoring the cell-capacitor voltages and phase current, and then using a simple on/off controller.

5.2.1 Three-Phase Clarke Transformation

A three-phase system of stationary reference frame voltages can be mapped to a two-phase orthogonal α-β plane. The relationship is shown in Figure 5.2.1. This is a convenient technique especially in rotating three-phase machines, since the rotating system vector in d-q axis plane is found by applying an angular phase shift. The mathematical transform for converting the stationary three-phase parameters to the orthogonal plane is known as the Clarke or Park transform.

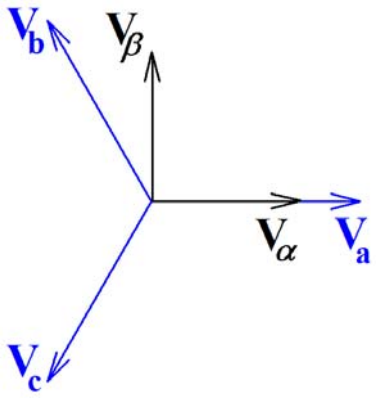


Figure 5.2.1: Relationship between stationary reference frame and complex space vector frame

The Clarke transform acts on an arbitrary set of balanced three-phase voltages to obtain the so called space vector representation in the complex α-β plane. The time-dependent vector, **V**, is derived from the individual phase voltages according to

$$\mathbf{V} = \frac{2}{3}\left(v_{an} + v_{bn} e^{j\frac{2\pi}{3}} + v_{cn} e^{j\frac{4\pi}{3}} \right) \quad \ldots (5.2.1)$$

where v_{an}, v_{bn} and v_{cn} are the stationary node voltages with respect to the centre-point neutral of a balanced three-phase load, and

$$v_{an} + v_{bn} + v_{cn} = 0 \quad \ldots (5.2.2)$$

The orthogonal reference frame components are found using

$$\mathbf{V} = v_\alpha + j v_\beta \quad \ldots (5.2.3)$$

$$v_\alpha = \frac{2}{3}\left(v_{an} + v_{bn} \cos\left(\frac{2\pi}{3}\right) + v_{cn} \cos\left(\frac{4\pi}{3}\right) \right) \quad \ldots (5.2.4)$$

$$v_\beta = \frac{2}{3}\left(v_{bn} \sin\left(\frac{2\pi}{3}\right) + v_{cn} \sin\left(\frac{4\pi}{3}\right) \right) \quad \ldots (5.2.5)$$

These simplify to

$$v_\alpha = \frac{2}{3} v_{an} - \frac{1}{3}\left(v_{bn} + v_{cn} \right) \quad \ldots (5.2.6)$$

$$v_\beta = \frac{1}{\sqrt{3}}\left(v_{bn} - v_{cn} \right) \quad \ldots (5.2.7)$$

The space vector, **V**, is also normally represented in the complex plane using

$$\mathbf{V} = V e^{j\theta} \quad \ldots (5.2.8)$$

where

$$V = \sqrt{\left(v_\alpha^2 + v_\beta^2\right)} \quad \ldots (5.2.9)$$

and

$$\theta = \tan^{-1}\left(\frac{v_\beta}{v_\alpha}\right) \quad \ldots (5.2.10)$$

5.2.2 Space Vector Duty Cycle Computation

In the three-phase system, each phase voltage node can apply a voltage between $+V_{dc}/2$ and $-V_{dc}/2$. If the inverter limb circuit is a basic two-level topology, then only the minimum and maximum voltages are applied. In this case, the inverter has eight possible switching state vectors, and these form a hexagonal constellation pattern in the complex plane as shown in Figure 5.2.2. The vector identification uses a 0 to represent the negative phase voltage level and 1 to represent the positive phase voltage level.

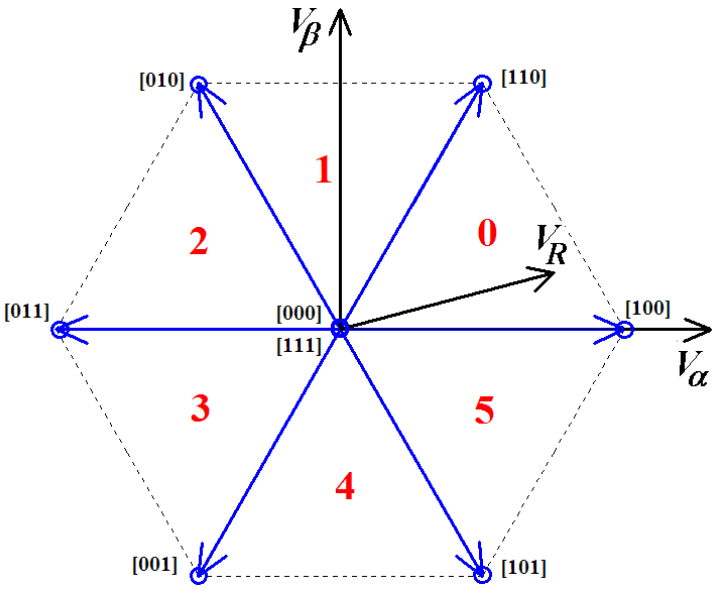


Figure 5.2.2: Inverter state space vector diagram

The duty cycle computation is done for each triangular sector formed by two state vectors. Figure 5.2.3 illustrates the vector composition required for a reference in the sector bounded by the switching state vectors [100] and [110]. The magnitude of each switching state vector is $2V_{dc}/3$. The magnitude of a vector to the mid-point of the line between each switching state vector vertex is $V_{dc}/\sqrt{3}$. The amplitude modulation index, m_a, is defined as the ratio of the peak output voltage sinusoid to maximum positive

available voltage $V_{dc}/2$. Therefore, the maximum possible modulation depth for SVPWM is 1.155 and so SVPWM can operate with modulation depths above unity, in the same way as sine-triangle PWM with 3rd order harmonic injection.

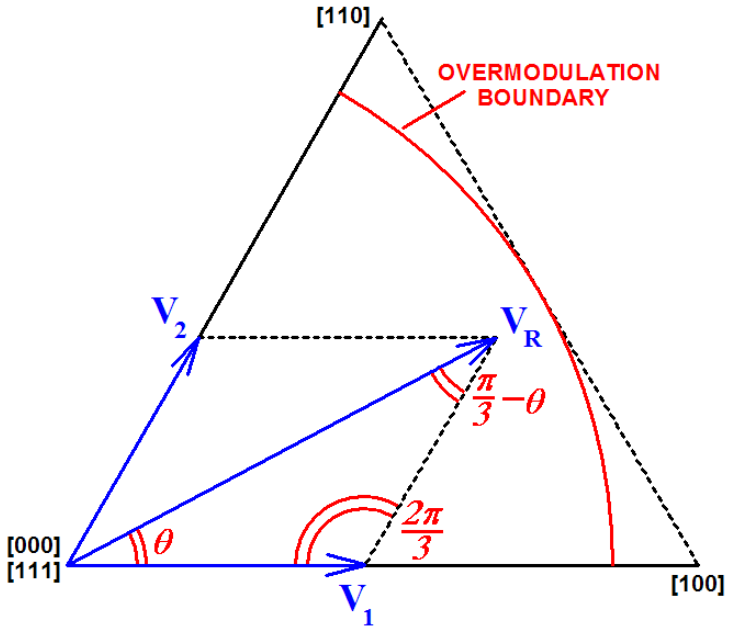


Figure 5.2.3: Sector 0 diagrammatic depiction of vector duty computation

In terms of the modulation depth, the reference vector magnitude, V_R, is given by

$$V_R = \frac{m_a V_{dc}}{2} \quad \ldots (5.2.11)$$

Therefore, the equation for the space vector computation is given by

$$\frac{V_1}{\sin\left(\frac{\pi}{3}-\theta\right)} = \frac{V_2}{\sin\theta} = \frac{m_a V_{dc}}{2\sin\left(\frac{2\pi}{3}\right)} \quad \ldots (5.2.12)$$

where

$$V_1 = D_1\left(\frac{2V_{dc}}{3}\right) \quad \ldots (5.2.13)$$

$$V_2 = D_2\left(\frac{2V_{dc}}{3}\right) \quad \ldots (5.2.14)$$

and

D_1 and D_2 are the duty cycles in one PWM switching period

So (5.2.13) can be re-written in terms of the duty cycles as

$$\frac{2D_1}{3\sin\left(\frac{\pi}{3}-\theta\right)}=\frac{2D_2}{3\sin\theta}=\frac{m_a}{2\sin\left(\frac{2\pi}{3}\right)} \quad \ldots (5.2.15)$$

Now

$$\sin\left(\frac{2\pi}{3}\right)=\frac{\sqrt{3}}{2} \quad \ldots (5.2.16)$$

Therefore, the individual duty cycles for each sector boundary state vector and the zero state vector, [000] or [111], are given by

$$D_1=\frac{\sqrt{3}}{2}m_a\sin\left(\frac{\pi}{3}-\theta\right) \quad \ldots (5.2.17)$$

$$D_2=\frac{\sqrt{3}}{2}m_a\sin\theta \quad \ldots (5.2.18)$$

$$D_0=1-D_1-D_2 \quad \ldots (5.2.19)$$

where

$$D_0=\frac{T_0}{T_s},\ D_1=\frac{T_1}{T_s}\ \text{and}\ D_2=\frac{T_2}{T_s}$$

These give switching times T_0, T_1 and T_2 for each inverter state for a total switching period of T_s. The timing diagram for SVPWM is shown in Figure 5.2.4 for the sector 0. By convention in SVPWM, the switching times are arranged as shown in the figure, so that the switching pattern is symmetric around the centre of the switching period. To do this the zero vector [111] is placed at the centre of the switching period, and the zero vector [000] at the start and end, and total period for a zero vector is divided equally amongst the two zero-vectors.

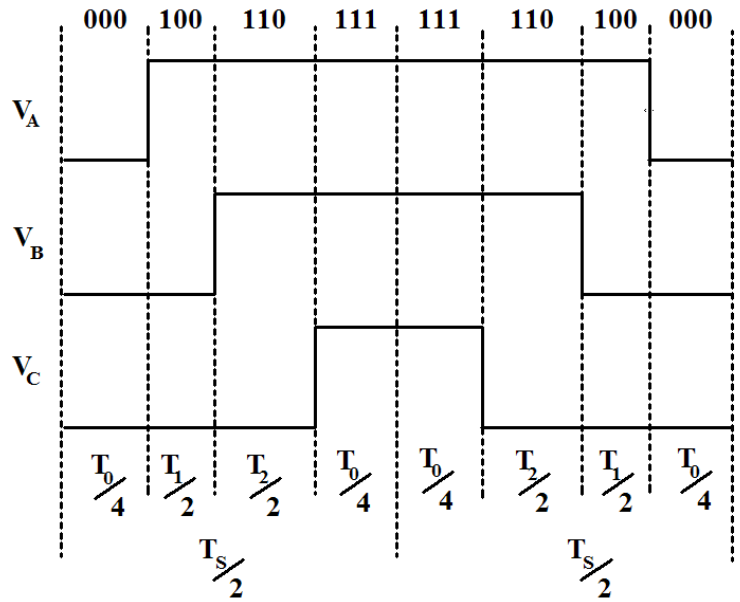


Figure 5.2.4: Space Vector Modulation Timing Diagram

In the other five sectors, the same computational process is applied. Equations (5.2.18 - 5.2.20) still apply, but the reference angle θ is offset by $-n3/\pi$, where n is the sector number, in order to reference θ to the base V_1 vector in each case. Another convention in SVPWM is to ensure there is only one switching transition within half a switching period, so the contributions of the switching state vectors are normally grouped to ensure this.

5.3 Multilevel Space Vector PWM

In multilevel inverters, the additional phase output voltage levels means that the number of state vectors is increased. In the 4-cell, 5-level inverter there are 61 distinct switching state vectors forming the constellation shown in Figure 5.3.1. The overall vector boundary still has a hexagonal form, with vertexes being the full voltage modes in each phase.

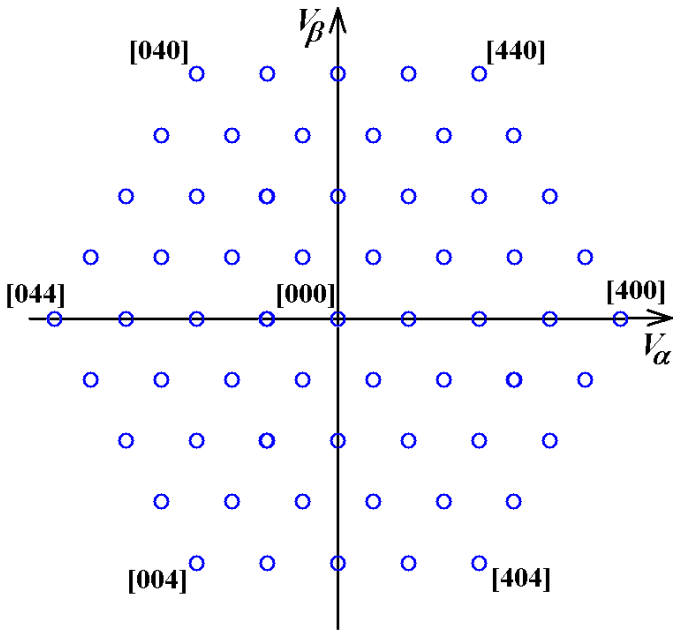


Figure 5.3.1 Four-cell inverter normalised space vector constellation diagram

The large number of possible space vectors which can be used to form a reference vector poses a computational problem. However, this complexity can be reduced to a form where the computational complexity is identical to the standard SVPWM method, and the multilevel issue of balancing can be addressed by the separate block implementation described in Chapter 4.

Figure 5.3.2 shows a reference vector together with the switching state vector points for sector 0 in the case of the four-cell inverter which has five individual phase

voltage levels. The voltage level contribution from each phase is shown in the bracketed indicator for each state vector. The reference vector is positioned within a triangle formed by state vectors [310], [300] and [410]. State vectors within the bounds of the space vector constellation hexagon can be realised with more than one switching mode. For instance, vector [310] is equivalent to [421], and the number of permutations increases towards the centre where there are 5 zero space vectors.

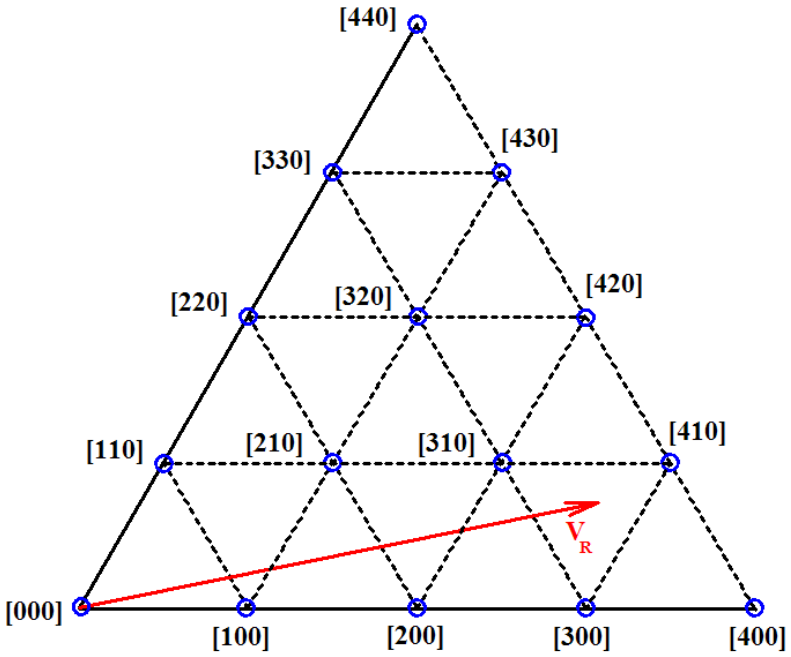


Figure 5.3.2 Voltage Reference Vector in Sector 0

The reference vector can be realised using the combination of switching state vectors shown in Figure 5.3.3. The base vector [310] represents the state of the three phases throughout the duration of the switching period. The PWM duty cycles for the additional voltage contribution can then be calculated using the triangular geometry from two vectors –[010] and [100]. The negative sign indicates that the duty cycle pulse for phase B will be subtracted from the base rather than being added.

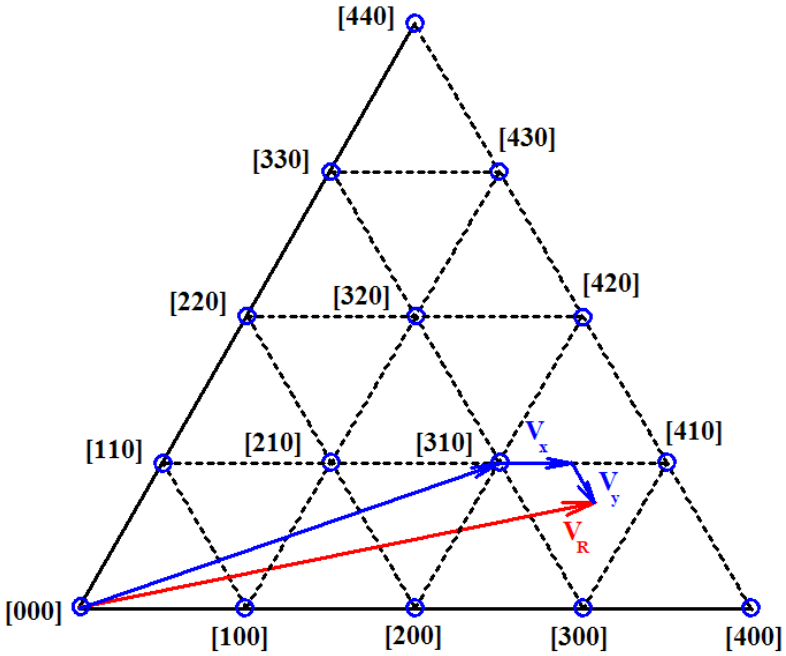


Figure 5.3.3 Vector Summation for Reference

The vector computation making up the total duty cycles for all three phases can be expressed as

$$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = \begin{bmatrix} 3 \\ 1 \\ 0 \end{bmatrix} + D_x \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} - D_y \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} \quad \ldots (5.3.1)$$

The terms D_A, D_B, D_C represent the ratio of average applied voltage to maximum possible voltage (4 levels) in each phase. It is clear that the example base vector [310] can be formed using two separate vectors along the edges of the sector 0 triangle as given by

$$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = \begin{bmatrix} 2 \\ 0 \\ 0 \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ 0 \end{bmatrix} + D_x \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} - D_y \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} \quad \ldots (5.3.2)$$

These vectors can be further expressed as duty cycle percentages of the main hexagon vertex vectors by

$$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = 0.5 \begin{bmatrix} 4 \\ 0 \\ 0 \end{bmatrix} + 0.25 \begin{bmatrix} 4 \\ 4 \\ 0 \end{bmatrix} + D_x \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} - D_y \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} \quad \ldots (5.3.3)$$

Now, the relationship can be further re-arranged by introducing additional duty cycle terms for the two vertex vectors as given by

$$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = 0.5 \begin{bmatrix} 4 \\ 0 \\ 0 \end{bmatrix} + 0.25 \begin{bmatrix} 4 \\ 4 \\ 0 \end{bmatrix} + D_{1'} \begin{bmatrix} 4 \\ 0 \\ 0 \end{bmatrix} + D_{2'} \begin{bmatrix} 4 \\ 4 \\ 0 \end{bmatrix} \quad \ldots (5.3.4)$$

where

$$D_{1'} = \frac{D_x + D_y}{4} \quad \ldots (5.3.5)$$

$$D_{2'} = -\frac{D_y}{4} \quad \ldots (5.3.6)$$

This means that, mathematically, the SVPWM computation problem in a multilevel inverter can be minimised to the following form

$$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = D_1 \begin{bmatrix} 4 \\ 0 \\ 0 \end{bmatrix} + D_2 \begin{bmatrix} 4 \\ 4 \\ 0 \end{bmatrix} \quad \ldots (5.3.7)$$

where

$$D_1 = \frac{2 + D_y + D_x}{4} \quad \ldots (5.3.8)$$

$$D_2 = \frac{1 - D_x}{4} \quad \ldots (5.3.9)$$

Figure 5.3.4 illustrates graphically the vector solutions required to obtain the reference vector in the five-level inverter.

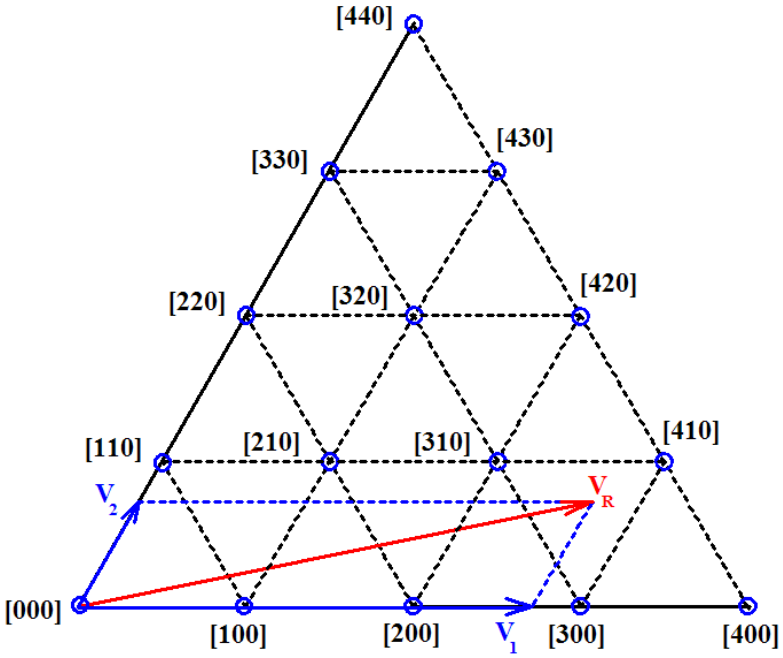


Figure 5.3.4 Space vector decomposition in sector 0

This means that the standard two-level duty cycle equations, (5.2.18 and 5.2.19) can be applied to multilevel inverters to obtain the timing information required to implement SVPWM. In the four-cell inverter, the phase duty cycle terms are first computed using the relevant sector equation, and these are listed in Table 5.3.1.

Sector, n	Phase Angle, θ	Sector Duty Equation
0	$0 \le \theta < \pi/3$	$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = D_1 \begin{bmatrix} 4 \\ 0 \\ 0 \end{bmatrix} + D_2 \begin{bmatrix} 4 \\ 4 \\ 0 \end{bmatrix}$
1	$\pi/3 \le \theta < 2\pi/3$	$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = D_1 \begin{bmatrix} 4 \\ 4 \\ 0 \end{bmatrix} + D_2 \begin{bmatrix} 0 \\ 4 \\ 0 \end{bmatrix}$
2	$2\pi/3 \le \theta < \pi$	$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = D_1 \begin{bmatrix} 0 \\ 4 \\ 0 \end{bmatrix} + D_2 \begin{bmatrix} 0 \\ 4 \\ 4 \end{bmatrix}$
3	$\pi \le \theta < 4\pi/3$	$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = D_1 \begin{bmatrix} 0 \\ 4 \\ 4 \end{bmatrix} + D_2 \begin{bmatrix} 0 \\ 0 \\ 4 \end{bmatrix}$
4	$4\pi/3 \le \theta < 5\pi/3$	$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = D_1 \begin{bmatrix} 0 \\ 0 \\ 4 \end{bmatrix} + D_2 \begin{bmatrix} 4 \\ 0 \\ 4 \end{bmatrix}$
5	$5\pi/3 \le \theta < 2\pi$	$\begin{bmatrix} D_A \\ D_B \\ D_c \end{bmatrix} = D_1 \begin{bmatrix} 4 \\ 0 \\ 4 \end{bmatrix} + D_2 \begin{bmatrix} 4 \\ 0 \\ 0 \end{bmatrix}$

Table 5.3.1: Sector duty equations

Now, these can result in phase duty cycle values greater than 1, so the results are further processed by splitting the duty cycle terms into the fractional and integer parts, to obtain the timing parameters for multilevel SVPWM control. The integer part of each phase duty cycle is the applied base voltage level over the whole switching period. The fractional part is then the ratio of the applied time for the extra voltage level added on the output to the total PWM switching period.

The base voltage level, m, for phase A in a switching cycle is the integer part of D_A. Mathematically, it is found using the floor function and is expressed as

$$m = \lfloor D_A \rfloor \qquad \ldots (5.3.10)$$

The time when level $m+1$ is applied in the centre of the switching cycle can be found from the fractional part of D_A, and is given by

$$T_{m+1} = T_s \left(D_A - \lfloor D_A \rfloor \right) \quad \ldots (5.3.11)$$

This SVPWM can be implemented in hardware using a carrier-based approach to produce the gate firing signals. The modulation timing diagrams for one phase are shown in Figure 5.3.5.

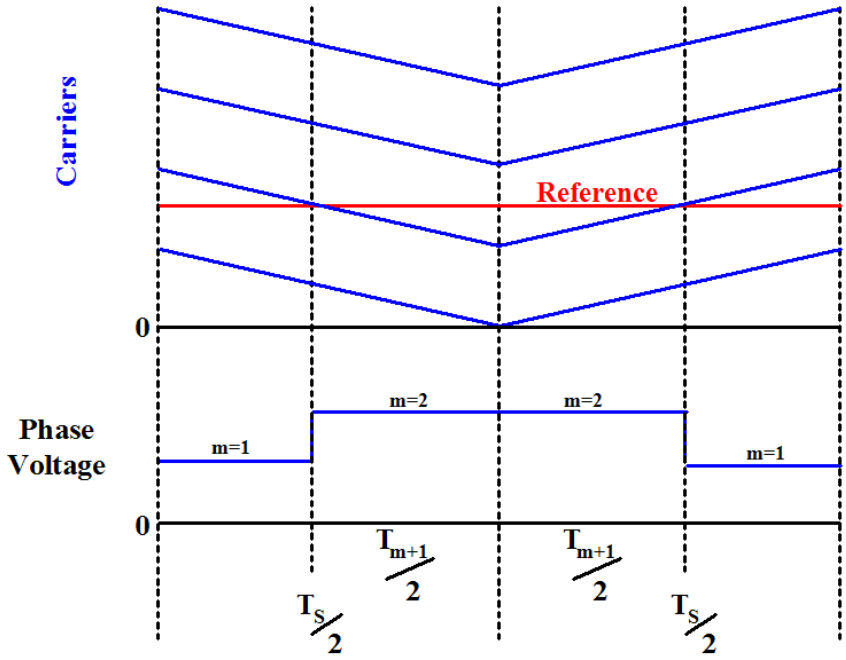


Figure 5.3.5 Space vector carrier-based implementation timing diagram

In the case of the four-cell inverter where the per unit reference span is 2, the phase reference for the comparators can be computed using the duty cycle equations,

$$D_1 = \sqrt{3} m_a \sin\left(\frac{(1-n)\pi}{3} - \theta \right) \quad \ldots (5.3.12)$$

$$D_2 = \sqrt{3} m_a \sin\left(\theta - \frac{n\pi}{3} \right) \quad \ldots (5.3.13)$$

Table 5.3.2 lists the summations required for each sector. In this case, the reference is symmetric around zero and so there is no requirement to include zero voltage vector contributions.

Sector	Phase Angle	Space Vector Phase Reference Voltages		
n	θ	V_a	V_b	V_c
0	$0 \le \theta < \pi/3$	D_1+D_2	$-D_1+D_2$	$-D_1-D_2$
1	$\pi/3 \le \theta < 2\pi/3$	D_1-D_2	D_1+D_2	$-D_1-D_2$
2	$2\pi/3 \le \theta < \pi$	$-D_1-D_2$	D_1+D_2	$-D_1+D_2$
3	$\pi \le \theta < 4\pi/3$	$-D_1-D_2$	D_1-D_2	D_1+D_2
4	$4\pi/3 \le \theta < 5\pi/3$	$-D_1+D_2$	$-D_1-D_2$	D_1+D_2
5	$5\pi/3 \le \theta < 2\pi$	D_1+D_2	$-D_1-D_2$	D_1-D_2

Table 5.3.2: Phase reference equations

The references are then applied to triangular carriers with minima at the centre of each switching period. This means that the reference must be computed and sampled at the maxima of each carrier. This is a form of symmetric regular sampling, but at the opposite points in the carrier cycle to standard carrier-based PWM schemes. The computation of the duty cycle assumes that at the minimum value all inverter cell upper switches are in the off state, so the phase disposition (PD) carrier scheme is used.

When the computed SVPWM reference is analysed, it is clear that this control method is akin to a third harmonic injection scheme. Figure 5.3.6 shows the resultant reference waveform, and its decomposition into a fundamental sinusoid plus third order triangular-shaped injected signal. Boys and Handley [5.13] analysed this triangular third harmonic component in the frequency domain, but the time domain equation can also be found.

The equivalent triangle injected waveform function, $E(\theta)$, can be found by first obtaining the peak of the decomposed pseudo-triangle injected signal at $\theta = \pi/3$. The injected waveform function for the sector where $n = 1$, is given by,

$$E(\theta) = (D_1 - D_2) - 2m_a \cos(\theta) \quad \ldots (5.3.14)$$

Expanding with the duty cycle terms gives,

$$E(\theta) = \sqrt{3}m_a\left(\sin(-\theta) - \sin\left(\theta - \frac{\pi}{3}\right)\right) - 2m_a \cos(\theta) \quad \ldots (5.3.15)$$

Now the value of E can be found for $\theta = \pi/3$ as follows,

$$E(\theta)\Big|_{\theta=\frac{\pi}{3}} = \sqrt{3}m_a\left(-\frac{\sqrt{3}}{2}\right) - 2m_a\frac{1}{2} \quad \ldots (5.3.16)$$

$$E(\theta)\Big|_{\theta=\frac{\pi}{3}} = \frac{m_a}{2} \quad \ldots (5.3.17)$$

Therefore the waveform function, *E(θ)* can be approximated to,

$$E(\theta)=\frac{m_a}{2}\left(\left(\left(\frac{6\theta}{\pi}+3\right)-2\left\lfloor\frac{3\theta}{\pi}+2\right\rfloor\right)\right)(-1)^{\left\lfloor\frac{3\theta}{\pi}+2\right\rfloor} \qquad \ldots (5.3.18)$$

There is a slight error between this triangular approximation and the actual SVPWM equivalent injected signal. Figure 5.3.7 shows the variation in the error over a whole cycle. As can be seen, the maximum error is only 0.2% and so it is possible to implement a SVPWM control using carriers and a reference composed of the summation of a sine wave and a triangular signal. This simple approach lends itself well to a digital implementation.

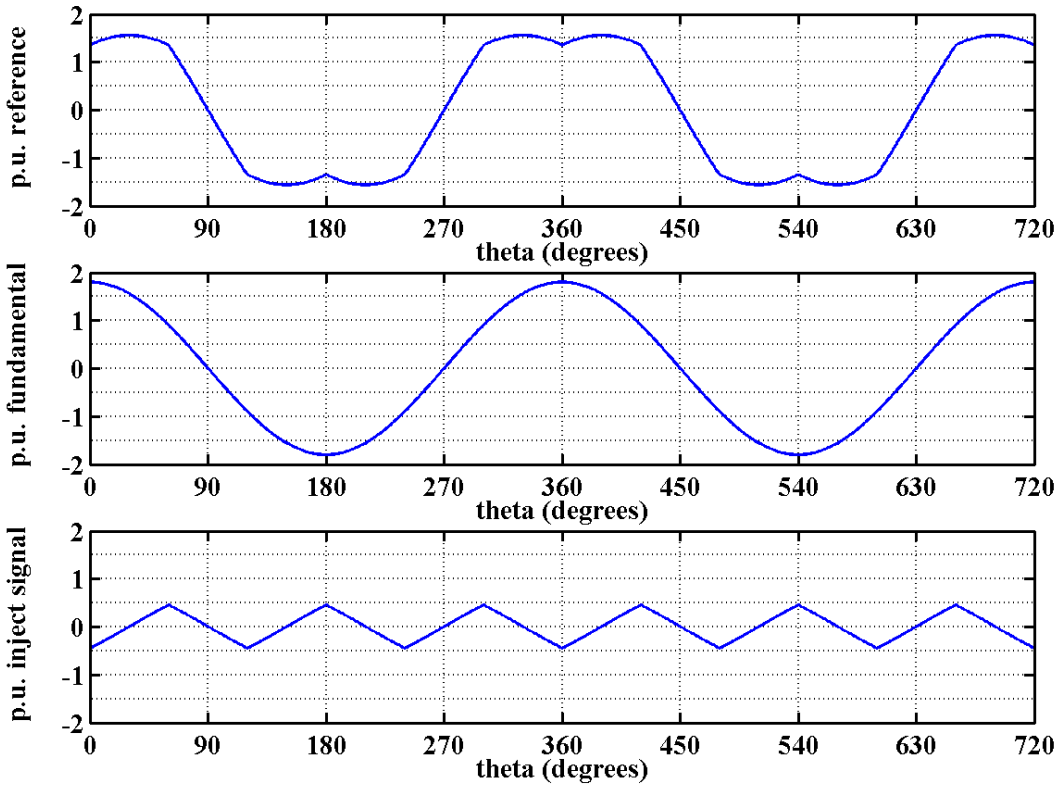


Figure 5.3.6: SVPWM equivalent reference, fundamental and injected 3rd order signal, m_a = 0.9

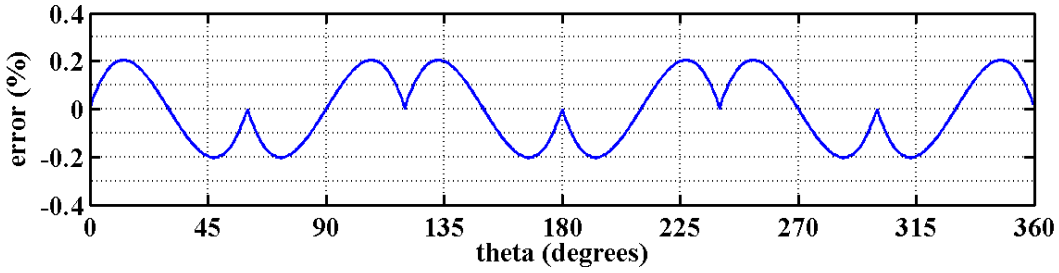


Figure 5.3.7: Error between equivalent SVPWM injected signal and approximated triangle

5.4 Ideal SVPWM Multilevel Firing Signals

This section explains some of the subtle variations in performance due to slight changes in the carrier-based implementation of the multilevel SVPWM scheme. The duty cycles are computed at the peak in the carrier waveform, and then translated into a reference signal, and this has an impact on the symmetry over a cycle of the firing signals applied to the inverter. Figure 5.4.1 shows the modulation waveforms and resultant level firing signals (no balancing algorithm) with a low modulation frequency. As can be seen, the reference is not symmetric and there will be asymmetry in the output voltage which will result in the production of odd and even order harmonics within the spectrum. This is also the case in PD PWM with symmetric sampling.

These even harmonics can be seen in the output voltage spectra shown in Figure 5.4.2. It can also be seen that the SVPWM implementation has a large harmonic at the switching frequency in the phase voltage which is cancelled in the line voltage. This spectral signature was also seen in the waveforms of sine-triangle PD PWM. The phase voltage spectrum also contains significant third and ninth harmonic components due to the injected triangular signal in the reference, which are cancelled in the three-phase load.

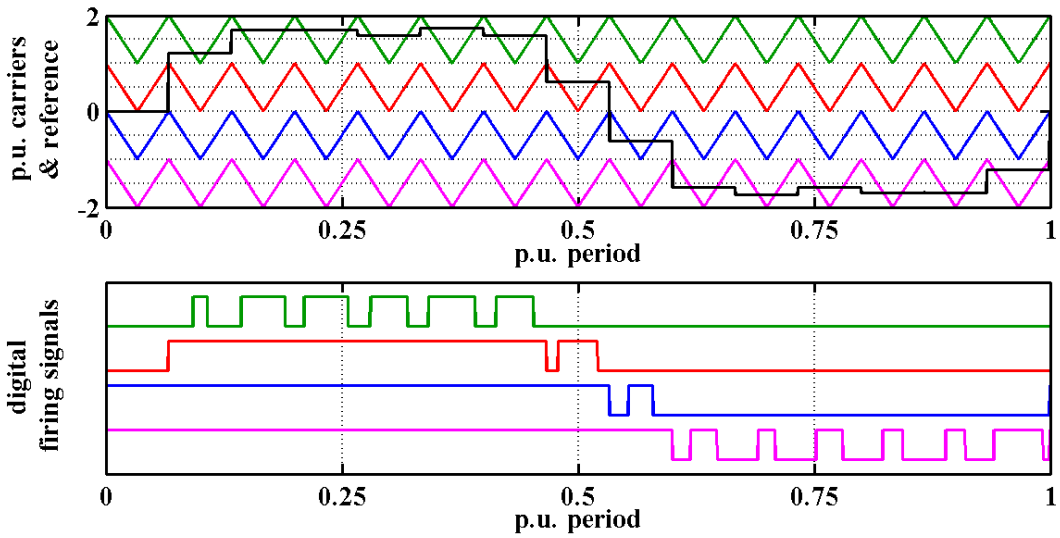


Figure 5.4.1: SVPWM waveforms, m_a = 1.0, m_f = 15

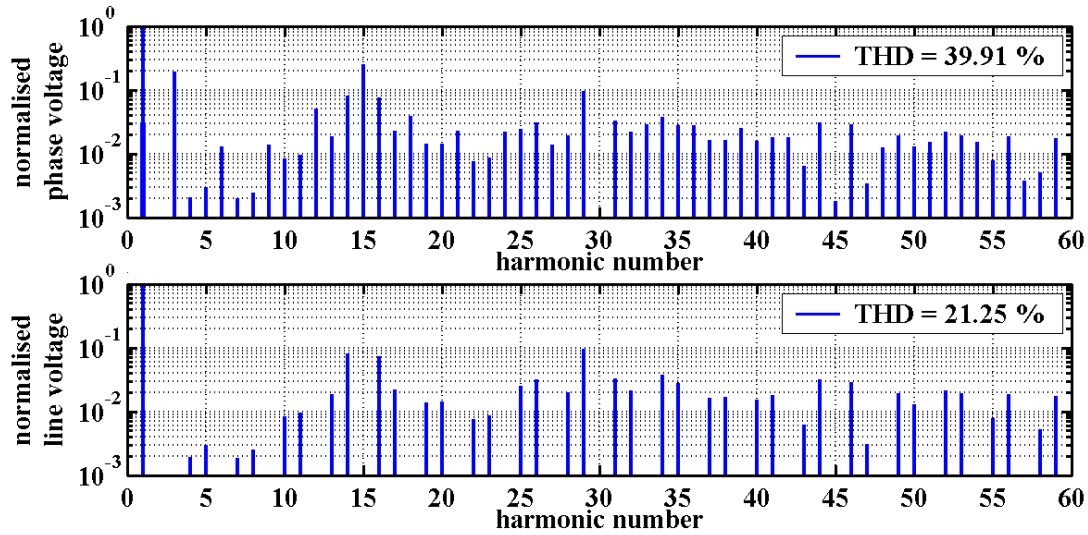


Figure 5.4.2: Voltage spectra of SVPWM, m_a = 1.0, m_f = 15

If m_f is an even number instead, then the reference will have symmetry, as shown in Figure 5.4.3. However, like the multilevel PD PWM scheme, the selection of an even m_f results in asymmetry in the output voltage. The resultant spectra, Figure 5.4.4, again include even order harmonics of the fundamental, but the overall result is very similar to the odd m_f example above.

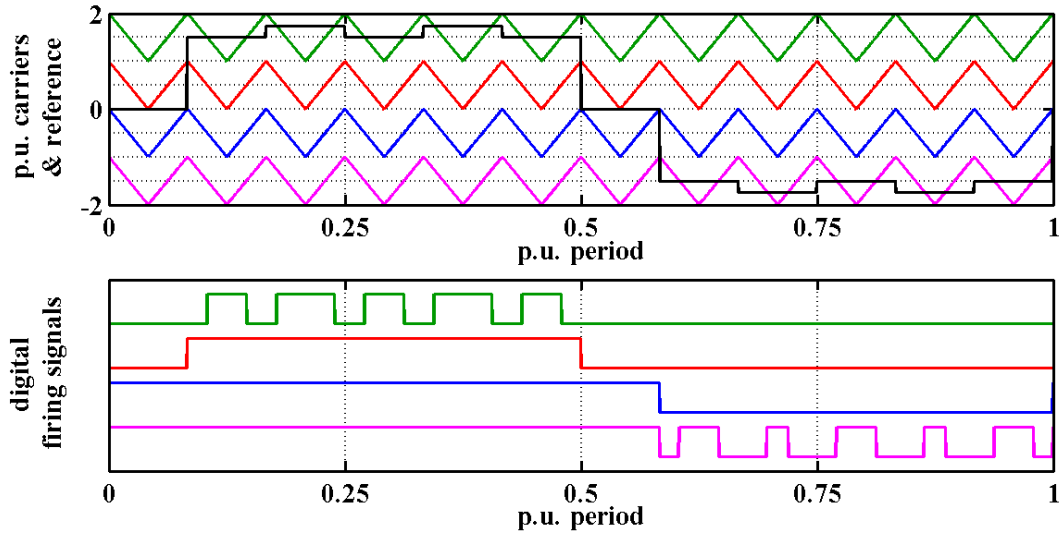


Figure 5.4.3: SVPWM waveforms, m_a = 1.0, m_f = 12

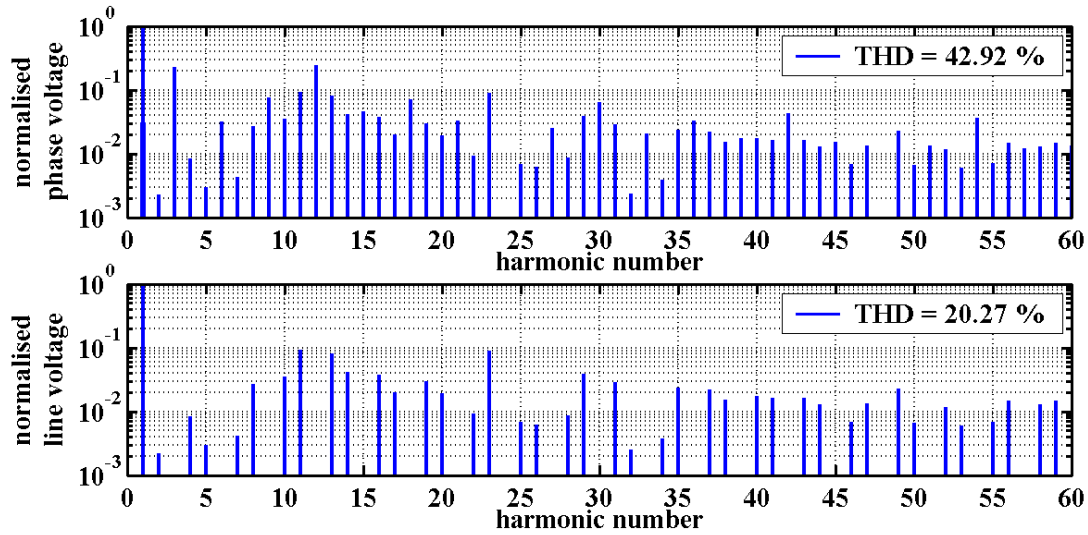


Figure 5.4.4: Voltage spectra of SVPWM, m_a = 1.0, m_f = 12

In the above example, the computation of the reference is done at each peak of the carrier, and results in a phase shift of $180/m_f$ degrees. This can be compensated for in the reference computation by adding $180/m_f$ degrees to the reference demand angle before computing the reference level. The resultant modulation waveforms are shown in Figure 5.4.5. There is still asymmetry in the output voltage as before and this leads to odd and even harmonics being present in the output voltage, as can be seen in Figure 5.4.6. Note that the THD is slightly higher than before, but this is due to the low m_f value selected.

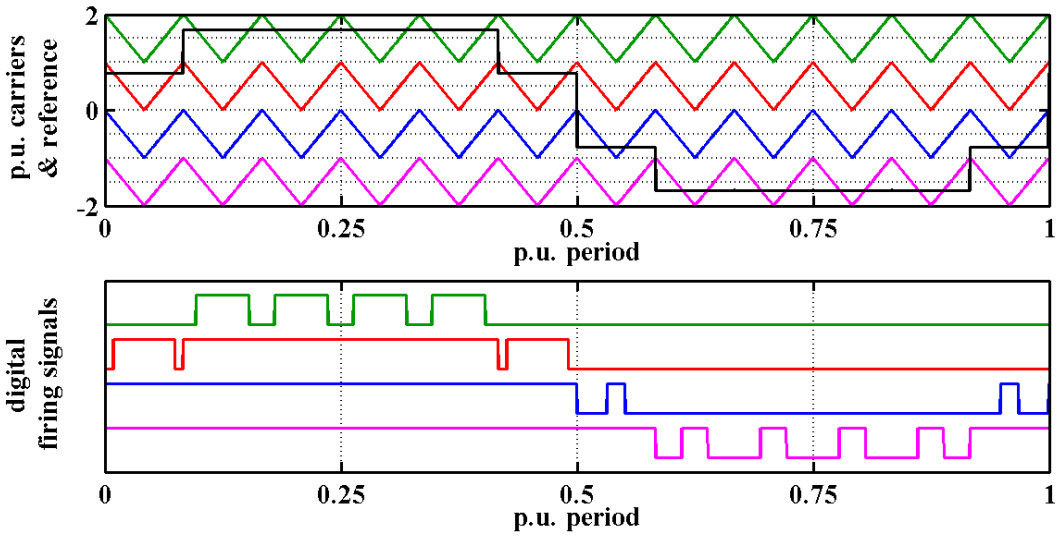


Figure 5.4.5: Phase adjusted SVPWM waveforms, m_a = 1.0, m_f = 12

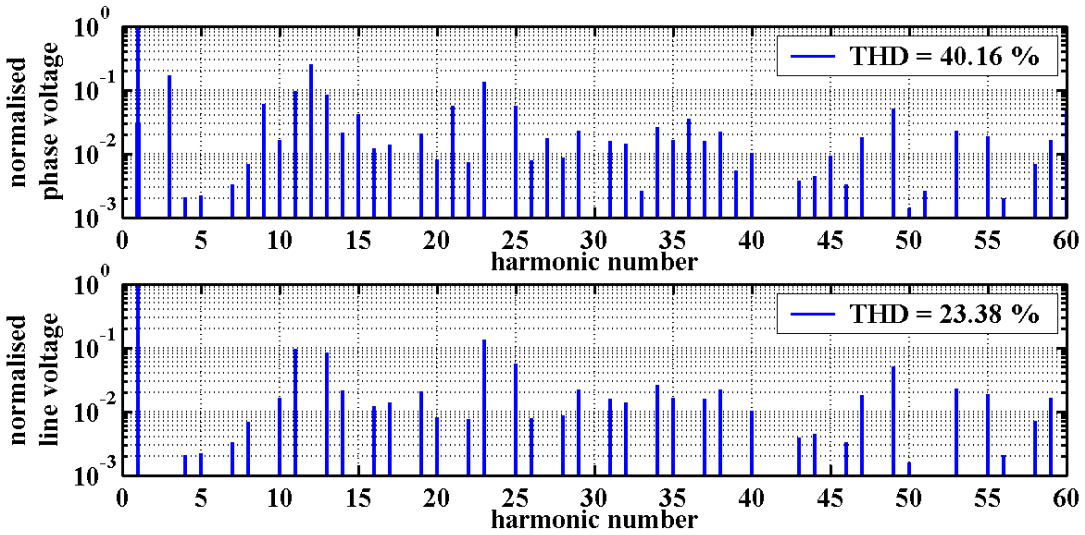


Figure 5.4.6: Voltage spectra of phase adjusted SVPWM, m_a = 1.0, m_f = 12

For higher switching frequencies, the choice of odd or even values m_f is not critical, as long as all three-phase carriers are synchronised in phase. This is because the harmonic component at the carrier frequency will only cancel in the line voltage when the carriers are in phase. This has already been shown in PD PWM. An example of the typical voltage spectra at a high m_f is shown in Figure 5.4.7. The overall performance of this SVPWM implementation under the ideal conditions of no cell-capacitor voltage variation is very good as can be seen by the relatively low line voltage THD. The output quality performance is very similar to that seen for PD PWM.

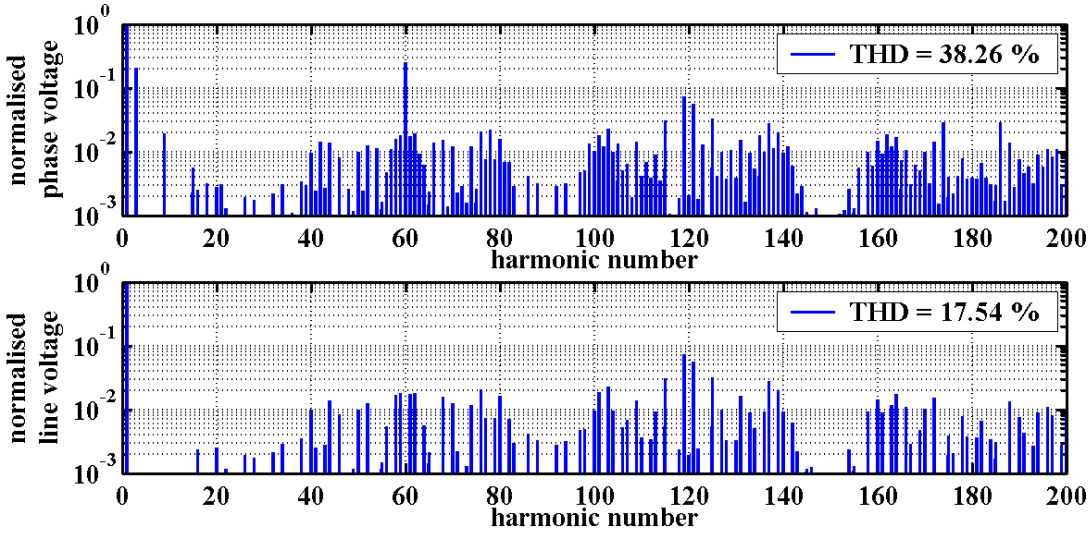


Figure 5.4.7: Voltage spectra of SVPWM with angle adjust, m_a = 0.9, m_f = 60

The phase-shifting of the reference computation to take into account the sampling delay of the carriers is the preferred implementation of the SVPWM scheme which

will be used throughout the analysis of the flying-capacitor simulated inverter. Figure 5.4.8 shows the variation in THD as a function of modulation depth for a perfectly balanced system with m_f = 60. Figure 5.4.9 shows the variation in computed DF1 under the same conditions. These curve show that low harmonic distortion achievable over a wide output voltage amplitude operating range, and are very similar to the ideal characteristics of the sine-triangle PD PWM scheme presented in the previous chapter.

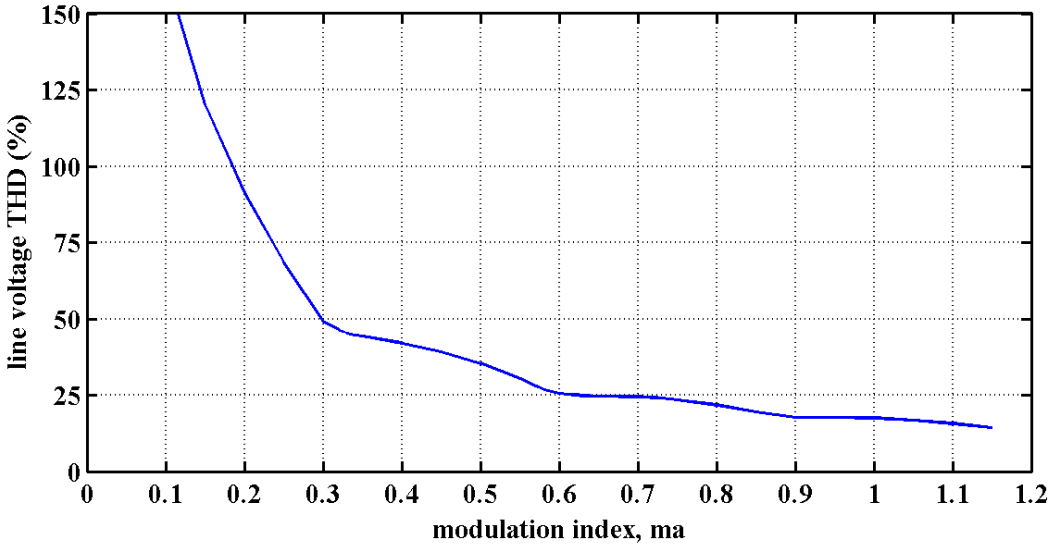


Figure 5.4.8: THD versus modulation index, m_a for SVPWM with m_f = 60

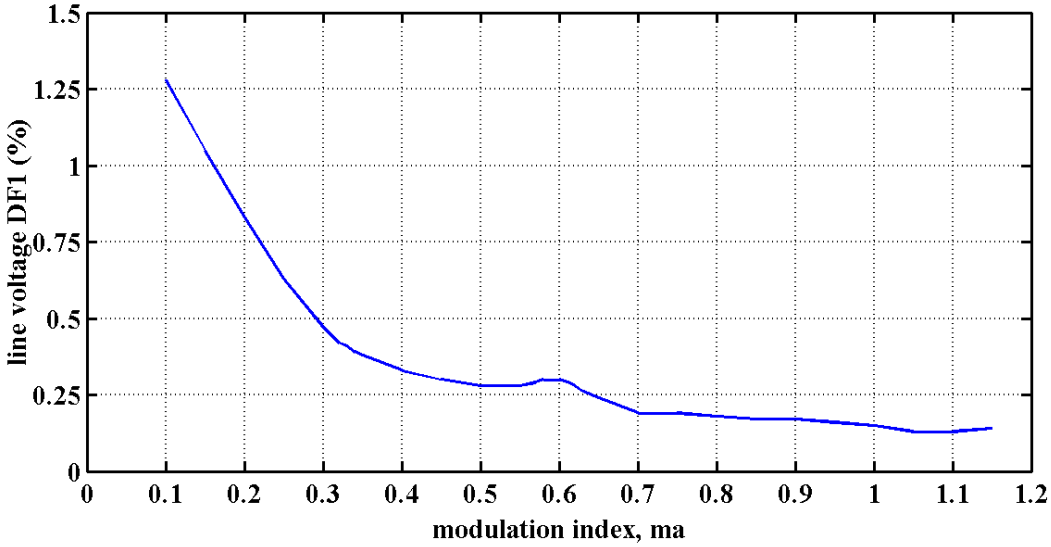


Figure 5.4.9: DF1 versus modulation index, m_a for SVPWM with m_f = 60

5.5 Performance of Balanced Inverter

The implementation of the SVPWM scheme is eminently suitable for applying the sub-carrier balancing scheme developed for sine-triangle PWM and presented in Chapter 4. For a direct comparison between the two types of PWM generation, the flying-capacitor inverter simulation uses the same modulation settings and load model used in Chapter 4. The inverter operates from a 400 V dc link and the unit cell-capacitance is 1 mF. The three-phase generic load model parameters are R_G = 0.5 Ω, L_G = 4 mH, P = 3.75 kW with DPF = 0.8. The control settings are 3 kHz switching frequency (m_f = 60), unity modulation depth (m_a = 1) and 3 μs dead-time.

Figure 5.5.1 shows the operating waveforms for the inverter controlled using the SVPWM scheme. The capacitor voltages are well balanced with only a small voltage ripple, and the phase currents exhibit low harmonic distortion. The load star point voltage waveform contains a dominant triangular shaped ripple component which is due to the effective injected signal in the equivalent reference of the SVPWM scheme.

Figure 5.5.2 shows the spectra of the inverter output waveforms. Both the switching frequency component and the third order harmonic are clearly visible in the phase voltage spectrum, but are cancelled in the three-phase load as can be seen in the line voltage spectrum. The spectral hump below 1 kHz seen in both the line voltage and phase current spectra is due to the voltage ripple in the cell-capacitors, and contributes in an increased THD above the ideal level.

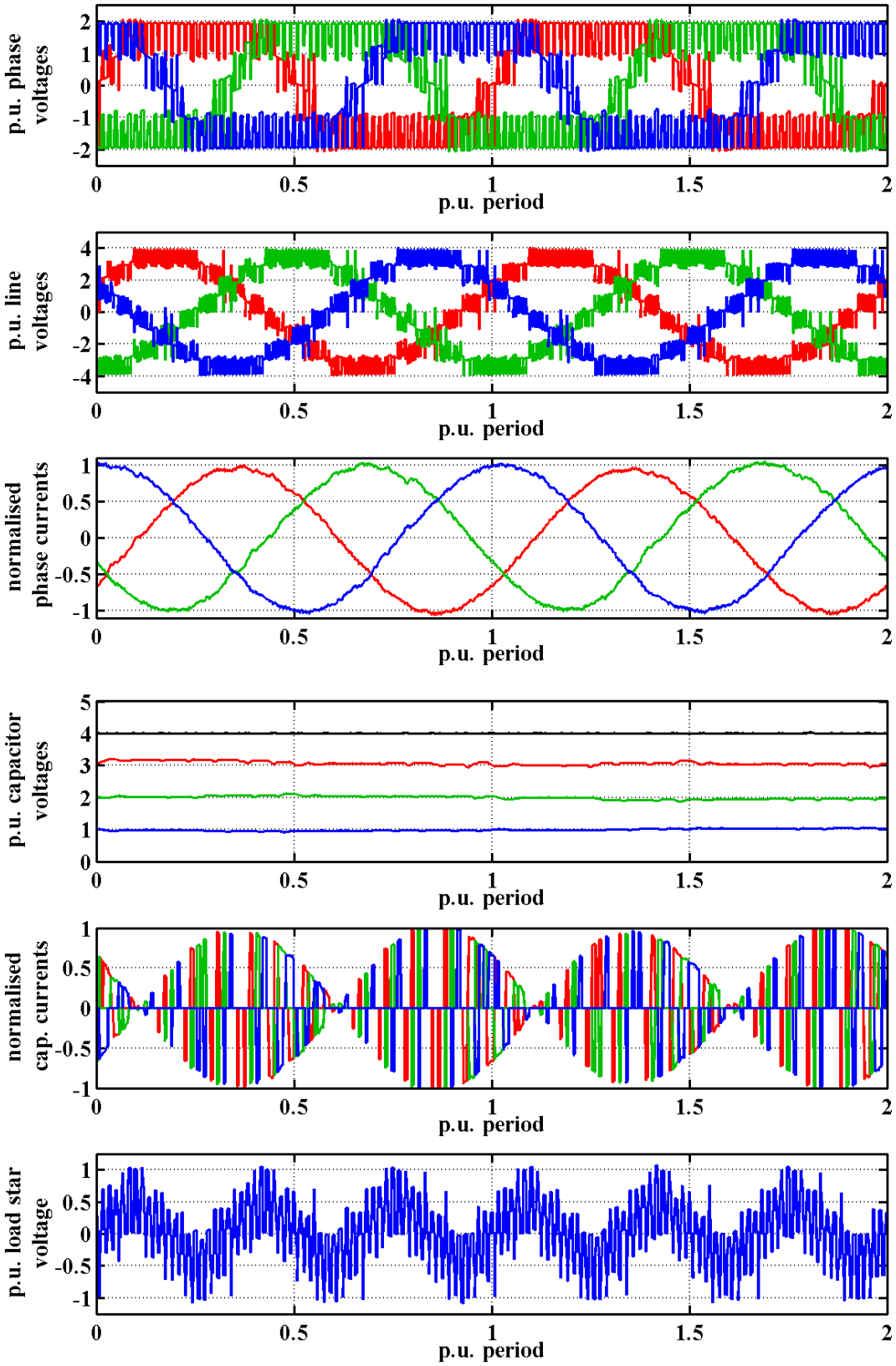


Figure 5.5.1: SVPWM waveforms, m_f = 60, m_a = 1.0

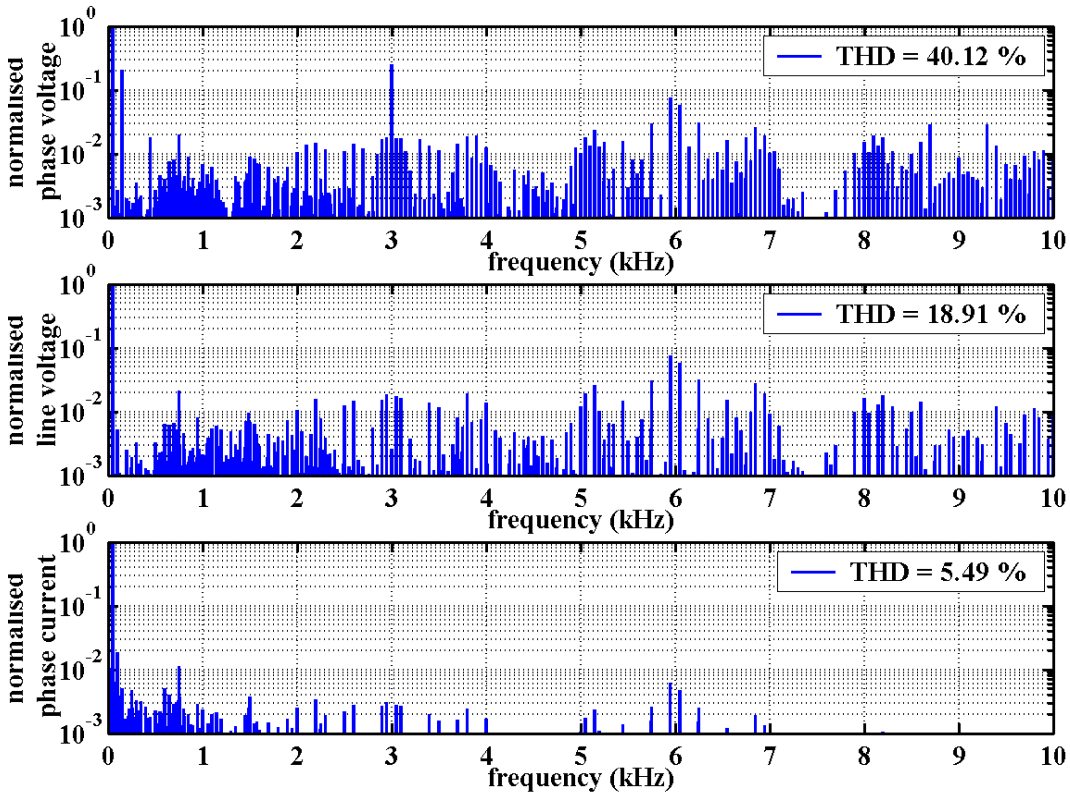


Figure 5.5.2: SVPWM spectra, m_f = 60, m_a = 1.0

The results can be compared with third-harmonic injected sine-triangle scheme, which also allows for increased modulation depth above unity. Table 5.5.1 lists the simulation results for the two schemes operating at two different modulation depths. As can be seen, there is very little to choose between these two control methods.

Scheme	m_a	Phase Voltage (Vrms)	Phase Current (Arms)	Line Voltage (Vrms)	TPF	Power (kW)	Loss (W)
SVPWM (m_a = 1.0)	0.97	147.7	11.5	242.0	0.76	3.84	188
PD + 1/6th (m_a = 1.0)	0.97	146.7	11.3	241.9	0.74	3.70	186
SVPWM (m_a = 1.1)	1.07	160.1	10.3	266.3	0.76	3.76	166
PD + 1/6th (m_a = 1.1)	1.07	158.9	10.2	266.6	0.76	3.68	163

Table 5.5.1: Output performance comparison of different schemes

Table 5.5.2 lists the total harmonic distortion factors for the two control modes. Here there is a slight improvement in phase current quality for the sine-triangle case. This is because the additional harmonics introduced by the effective reference of the SVPWM method, introduces additional inter-modulation harmonic products due to the cell-capacitor voltage frequency components.

Scheme	Phase Voltage THD (%)	Line Voltage THD (%)	Phase Current THD (%)
SVPWM (m_a = 1.0)	40.12	18.91	5.49
PD + 1/6th (m_a = 1.0)	37.33	18.63	4.43
SVPWM (m_a = 1.1)	34.15	16.67	4.42
PD + 1/6th (m_a = 1.1)	30.89	16.68	4.11

Table 5.5.2: Output distortion comparison of different carrier schemes

Table 5.5.3 compares the capacitor and power switch operating parameters and shows that both systems are well balanced although there is a slight increase in capacitor ripple voltage for the sine-triangle case. This means that the power devices must withstand around a 5 % higher blocking voltage in the third harmonic injected sine-triangle PWM case. However, this reduced capacitor voltage ripple amplitude in the SVPWM case does not translate into lower THD for the phase current waveform.

Overall, the performance of the two schemes is very similar, and the choice between which control strategy suites the application best will be based on the hardware implementation. The SVPWM requires greater computational effort in order to generate the duty-cycle reference and so a DSP implementation may be needed. However, it is possible to pre-compute a reference, and adjust the amplitude in real-time based on the amplitude modulation index. This means that both schemes can be implemented in almost identical digital hardware.

Scheme	Cell-Capacitor Voltages (V)			Max. Switch (V)	Cap. Current (Arms)	Peak Power Loss		
						IGBT (W)	Diode (W)	Trans. (W)
SVPWM (m_a = 1.0)	99.2	198.0	301.8	124.8	5.59	6.60	1.42	0.16
PD + 1/6th (m_a = 1.0)	102.1	200.5	301.4	130.9	5.57	6.42	1.36	0.16
SVPWM (m_a = 1.1)	99.9	199.9	300.0	120.4	4.26	6.07	1.02	0.15
PD+ 1/6th (m_a = 1.1)	101.5	200.3	300.3	124.7	4.27	5.87	0.99	0.14

Table 5.5.3: Phase balancing performance comparison of different carrier schemes

5.6 Conclusions

It has been shown that the space vector PWM scheme can be implemented in a very simple manner even for complex systems like the multilevel flying-capacitor inverter. The relationship that exists between the standard SVPWM and sine-triangle, carrier-based PWM was exploited to simplify the multilevel SVPWM duty-cycle computation rather than using a more complex algorithm based on the sub-sector triangles reported by other researchers.

The sub-carrier balancing implementation developed for cell-capacitor voltage ripple minimisation when controlled using sine-triangle PWM also functions correctly when used in SVPWM control. This means that the flying-capacitor SVPWM algorithm is simplified since it does not need to consider the actual switching states, and only operates on the voltage level vectors.

The simulated performance is on a par with optimised sine-triangle schemes, and results have been presented of SVPWM operation including a greater than unity modulation depth. SVPWM performance has been compared to third harmonic injection sine-triangle PWM and the results show the similarity between the two schemes.

5.7 References

[5.1] Handley, P.G. and Boys, J.T., “Space vector modulation: an engineering review”, Proceedings of PEVD '90, the 4th International Conference on Power Electronics and Variable-Speed Drives, IEE Conference Publication No. 324, 17 - 19 July, 1990, pp. 87 – 91.

[5.2] Murai, Y., Ohashi, K. and Hosono, I., “New PWM method for fully digitized inverters”, Conference Record of IAS '85, the 1985 IEEE Industry Applications Society 20th Annual Meeting, 6 - 11 October, 1985, pp. 448 – 453.

[5.3] Van der Broeck, H.W., Skudelny, H.-C. and Stanke, G.V., “Analysis and realization of a pulsewidth modulator based on voltage space vectors”, IEEE Transactions on Industry Applications, Vol. 24, No. 1, January/February 1988, pp. 142 –150.

[5.4] Steinke, J.K., "Control strategy for a three phase AC traction drive with three-level GTO PWM inverter", Proceedings of PESC '88, 19th Annual IEEE Power Electronics Specialists Conference, 11-14 April 1988, Vol. 1, pp. 431 - 438.

[5.5] Bauer, F. and Heining, H.-D., “Quick response space vector control for a high power three-level inverter drive system”, Proceedings of EPE ’89, the 3rd European Conference on Power Electronics and Applications, 9 – 12 October, 1989, Vol. 1, pp. 417 – 421.

[5.6] Lee, Y.-H., Suk, B.-S. and Hyun, D.-S., "A novel PWM scheme for a three-level voltage source inverter with GTO thyristors", IEEE Transactions on Industry Applications, Vol. 32, No. 2, March/April 1996, pp. 260 - 268.

[5.7] Wei, S.-M., Wu, B., Li, F.-H. and Liu, C.-W., "A general space vector PWM control algorithm for multilevel inverters", Proceedings of APEC '03, the 18th IEEE Applied Power Electronics Conference and Exposition, 9 - 13 February, 2003, Vol. 1, pp. 562 - 568.

[5.8] Peng, D., Lee, F.C. and Boroyevich, D., "A novel SVM algorithm for multilevel three-phase converters", Proceedings of PESC 2002, 33rd Power Electronics Specialists Conference, 23 - 27 June, 2002, Vol. 2, pp. 509 - 513.

[5.9] Zhang., H.-R., von Jouanne, A. and Wallace, A. "Multilevel inverter modulation schemes to eliminate common-mode voltages", Conference Record of IAS '98, the 33rd IEEE Industry Applications Annual Meeting, 12 - 15 October, 1998, Vol. 1, pp. 752-758.

[5.10] Li, L., Czarkowski, D., Liu, Y. and Pillay, P. “Multilevel space vector PWM technique based on phase-shift harmonic suppression”, Proceedings of APEC 2000, IEEE 15th Annual Applied Power Electronics Conference and Exposition, 6 - 10 February, 2000, Vol. 1, pp. 535 – 541.

[5.11] Filho, N.P. Pinto, J.O.P. and Bose, B.K., “A neural-network-based space vector PWM of a five-level voltage-fed inverter”, Proceedings of IAS ‘04, the IEEE Industry Applications Society 39th Annual Meeting, 3 - 7 October, 2004, Vol. 4, pp. 2181 – 2187.

[5.12] Blaabjerg, F. and Chen, L.-C., “Comparison of two modulation strategies in a simple 5 kVA PWM-VSI-inverter” Proceedings of COBEP '91, 1st Congresso Brasileiro de Eletrônica de Potência, 2 - 5 December, 1991, pp. 216 – 222.

[5.13] Boys, J.T. and Handley, P.G., “Harmonic analysis of space vector modulated PWM waveforms”, IEE Proceedings, Vol. 137, Part B, No. 4, July 1996, pp. 197 – 204.

[5.14] Wu, H-Y., Deng, Y., Liu, Y.; He, X.-N. “A new clew for research on PWM methods of multilevel inverters: principle and applications”, Proceedings of PCC-Osaka 2002, IEEJ/IEEE Joint IAS Power Conversion Conference, 2 - 5 April, 2002, Vol. 3, pp. 1251 – 1256.

[5.15] Martins, C.A., Roboam X., Meynard, T.A. and Carmlho, AS., "Multi-level direct torque control with imposed switching frequency and reduced ripple", Proceedings of PESC 2000, 31st Annual IEEE Power Electronics Specialists Conference, 18 - 23 June, 2000, June, 2000, Vol. 1, pp. 435 - 441.

[5.16] Mendes, M.A.S., Peixoto, Z.M.A., Seixas, P.F. and Donoso-Garcia, P., “A space vector PWM method for three-level flying-capacitor inverters”, Proceedings of PESC 2001, 32nd Power Electronics Specialists Conference, 17 - 22 June, 2001, Vol. 1, pp. 182 – 187.

Chapter 6 EXPERIMENTAL RESULTS

6.1 Introduction

This chapter presents the results of measurements made on an experimental three-phase flying-capacitor multilevel inverter. The inverter is intended to be used for confirming the simulation results for the various forms of sinusoid synthesis control.

6.2 Laboratory Prototype Inverter Design and Test

The experimental inverter, used for confirming the performance of the various control schemes and the cell-capacitor voltage balancing strategies, is a four-cell, three-phase topology. This circuit can synthesis line to line voltage waveforms with up to 9 distinct voltage levels. The testing is focussed on confirming the validity of the simulation results of the inverter when controlled using staircase SHE-4H2, different carrier placement sine-triangle PWM and space vector PWM.

6.2.1 Power Electronics

The three-phase flying-capacitor inverter topology selected for the experimental work is a four-cell design with 24 individual IGBT power switches. The power processing stage of the inverter is constructed using International Rectifier IRG4PC30KD, 30 A, 600 V, IGBTs and Rubycon 1 mF, 200V electrolytic capacitors. A block diagram of one inverter phase limb is shown in Figure 6.2.1. The IGBT contains an anti-parallel diode of equal rating and so operates with bi-directional current. The TO-247 packaged IGBTs are mounted on individual 10 ^{o}C/W heatsinks and therefore the inverter can handle individual device power dissipation of up to 8.6 W. This is computed using the IGBT's published junction-sink thermal resistance (0.44 ^{o}C/W) and assuming a maximum junction temperature of 115 ^{o}C in a 25 ^{o}C ambient. The individual capacitor maximum rms ripple current rating is 2.7 A at 1 kHz and 105 ^{o}C, and this will limit the practical maximum power conversion capability of the inverter. Simulations reveal that the capacitor current rating is the limiting factor on maximum power throughput and that the experimental inverter can safely handle a 2.5 kVA load when operating in PWM control at 3 kHz with a 400 V dc link.

The maximum operating dc link voltage is limited by the cell-capacitor voltage ratings which would mean an absolute maximum of 800 V, even though the IGBTs could theoretically cope with a 2.4 kV dc link. All tests however will be limited to operation

at 400 V dc maximum to ensure that the maximum voltage ratings of all the power components are not exceeded under any conditions.

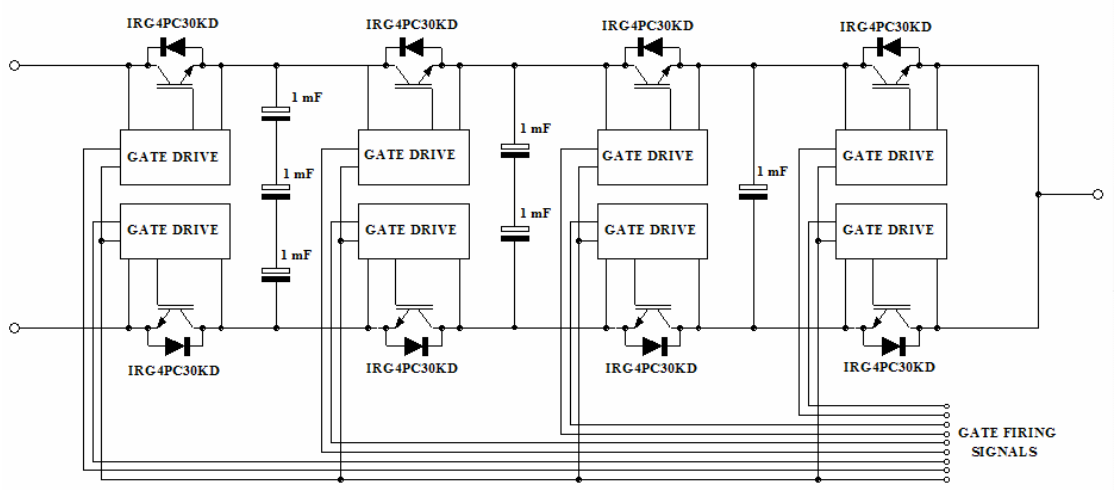


Figure 6.2.1: Inverter phase limb schematic diagram

Each IGBT has its own isolated gate driver shown in the circuit diagram, Figure 6.2.2. Each isolated gate drive circuit operates independently, and includes spurious gate-firing protection [6.1]. The gate-drive is supplied from an isolated switched mode power supply. An optocoupler provides isolation between the gate driver and power device and the small-signal digital logic control circuitry. Minimum on-time and minimum off-time latches ensure that the IGBT is not operated at too high a frequency and that the gate driver is less susceptible to noise. A MOSFET driver stage interfaces directly with the IGBT gate via current limiting resistors. The value of the resistor ensures sufficient gate current to rapidly turn-on the IGBT on and off. This gate-drive design can be scaled to much larger IGBT by increasing the gate drive current capability through reducing the gate resistor values and increasing the rating of the drive MOSFETs.

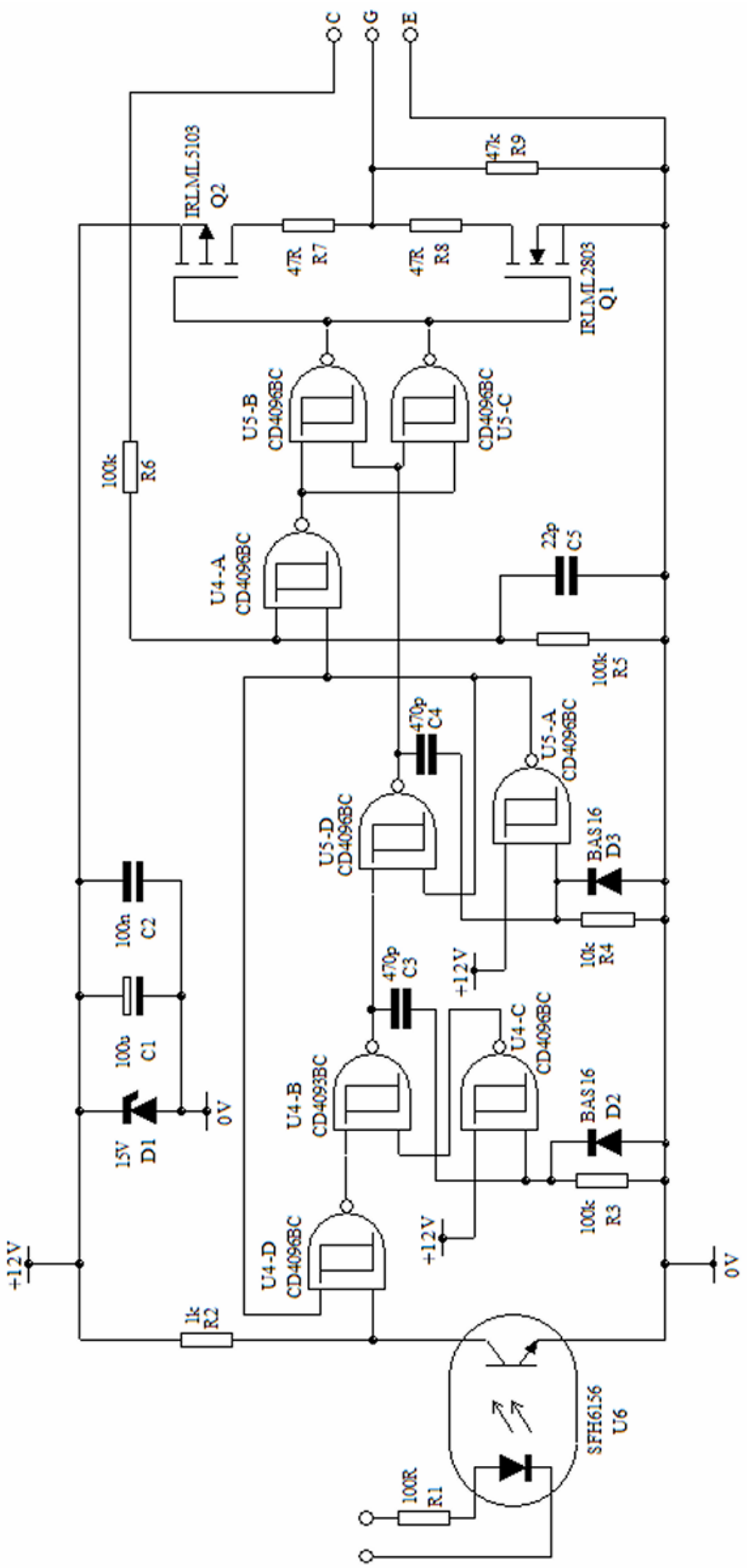


Figure 6.2.2: Gate drive circuit diagram

Two IGBTs plus their gate drive circuits are physically laid out on a single PCB and use mainly surface mount components to minimise board area. The PCB also includes a dual 12V output power supply with galvanic isolation between the input source 24 V supply and the each output rail. The power supply is a specially designed switched-mode power supply (SMPS) which offers high-efficiency and small PCB footprint. The SMPS topology is a forward converter and uses an integrated MOSFET plus PWM control IC (DPASwitch manufactured by Power Integration Inc). Regulation of the 12 V rails, which supply the two gate drivers, is achieved by using error voltage feedback from one of the output voltage rails via an optocoupler. The other 12 V rail is semi-regulated and so an additional 15 V Zener diode, D1, is placed across its rails to protect against any over-voltage conditions. Figure 6.2.3 shows a photograph of a populated dual-IGBT stage PCB, and highlights the major components. The circuit also includes a Motorola 68HC908, 8-bit microcontroller used only for commissioning purposes and disabled when the boards are operating in the inverter.

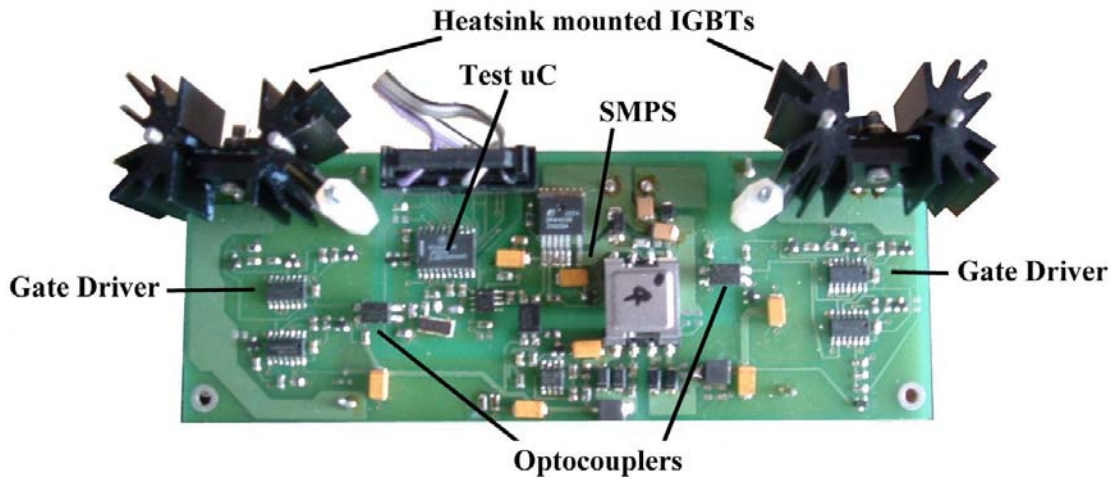


Figure 6.2.3: Dual-IGBT PCB

A single inverter phase limb is constructed from four dual-IGBT stage PCBs, so making a total of 12 PCBs used in the experimental inverter. A photograph of the assembled inverter is shown in Figure 6.2.4. The cell-capacitors can be seen below each set of inverter PCBs. There is also a single 1 mF, 450 V, electrolytic capacitor across the dc link connections for voltage smoothing purposes, seen on the left of the inverter. The small box in the foreground of the picture contains voltage level shifting buffer circuitry between the digital control logic and the gate drivers.

Figure 6.2.4: Flying-capacitor inverter assembly

6.2.2 Control System

The digital gate firing pulse generation and the different forms of control scheme are implemented on a Memec Spartan-II™ LC development board [6.2]. This is a low-cost evaluation platform containing one 100k gate Xilinx Spartan-II Field Programmable Gate Array (FPGA). An FPGA was selected for experimenting on the different control schemes because of the large number of PWM channels required in the multilevel inverter [6.3, 6.4]. Alternative commercially available microcontroller or DSP solutions have insufficient PWM hardware peripheral resources to enable sophisticated control of the experimental inverter.

The internal architecture of the FPGA is dynamically configured to route signals to the internal logic gate resources to match the desired digital circuit design. The development board has an in-circuit programmable ROM where the FPGA configuration file resides. This is programmed via a PC and configures the FPGA once power is cycled on the development board. Xilinx provide a complete Windows-based software development environment which is used to design and simulate a digital design. The software will synthesis a digital logic design and generates the ROM program file. Designs can be developed using a schematic editor, timing

diagram or a hardware description language. Simulation tools can be used to check designs before deployment.

The FPGA design for the experimental inverter has been written in VHDL. There are three separate designs for each form of modulation strategy, although there is a lot of commonality between the designs, using some of the same digital design blocks in each case. It would be possible to implement a single integrated FPGA design solution within the existing Xilinx FPGA, with external modulation scheme selection.

Figure 6.2.5 shows a block diagram of the sine-triangle PWM control implementation for one of the three phases. This block is repeated for the other two phases except for the carrier block since the carriers are common to all three phases. The different forms of carrier placement are controlled by the SCHEME TYPE variable and the switching frequency (m_f) is set by the CARRIER PERIOD. The basic reference signal is obtained from a half-sine ROM look-up table, and it is scaled to give a peak value of twice the maximum carrier value. It is then scaled by the AMPLITUDE demand (m_a) which represents 0 to 100%. If the basic reference is below the maximum carrier value then the upper reference signal is zero and the lower reference signal equals the basic reference. If the basic reference is above the maximum carrier value then the upper reference signal equals the basic reference minus the maximum carrier value, and the lower reference signal equals the maximum carrier value. For third order harmonic injection, the reference table values are changed to include the additional harmonic component. Reference sampling by using latches on the input to the comparator can be set either at the carrier trough (symmetric) or at both peak and trough (asymmetric).

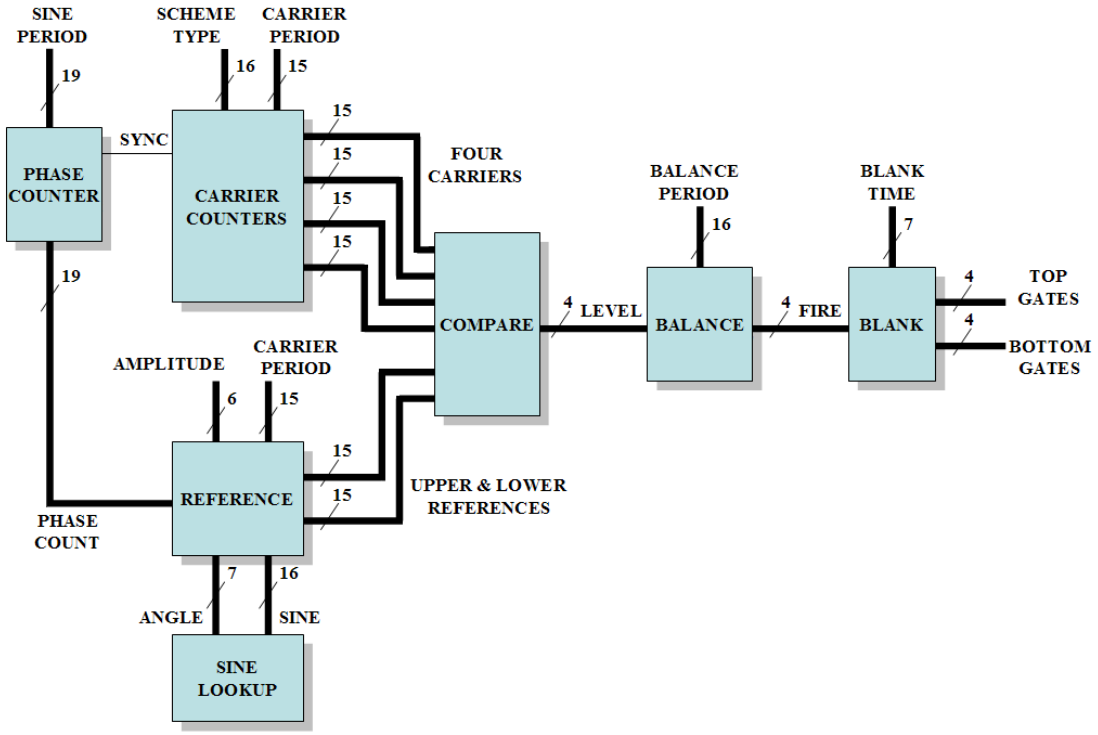


Figure 6.2.5: Block diagram of sine-triangle PWM digital design for one phase

The two band reference signals are then compared with the four carriers to generate the LEVEL signal which indicates the number of top switches in conduction. The balance block is a digital implementation of the balancing scheme described in Chapter 4, and it generates the four cell firing signals. These firing signals are then processed by the blank block which introduces the dead-time between the top and bottom gate-firing signals.

The various control signals which set the operating fundamental frequency, switching frequency, modulation depth and carrier placement scheme can be set externally using a 1 MHz serial communications link. This allows the modulation control system to be controlled by a microcontroller or DSP, and so be incorporated into a complete inverter system.

FPGA implementations of the space vector algorithm have been reported in the literature which performs the duty cycle computation directly using sine and cosine look-up tables, and then rearranging the firing pattern according to convention [6.3]. For this experimental inverter, the equivalent reference, described in Chapter 5, is stored in a look-up table. Therefore, the space vector PWM implementation is almost identical to sine-triangle PWM apart from the ROM data in the reference block. The carriers are fixed to the phase disposed (PD) form and reference sampling is done at the peak of the carriers.

The selective harmonic elimination digital implementation uses a very similar block arrangement except that the carrier spans half the total phase period and the references are the angular firing positions, which are pre-computed and stored in a look-up table. The balancing block contains a look-up table of the required balancing pattern, which is repeated every four cycles.

6.2.3 Test and Measurement System

The laboratory test set-up is shown in block diagram form in Figure 6.2.6, while Figure 6.2.7 shows a photograph of the laboratory set-up and highlights the flying-capacitor inverter and main test hardware. The inverter dc link voltage can be varied up to a maximum of 400 V using a bench power supply. The three-phase test loads are fixed inductors and variable resistors rated up to 10 A. The output voltages are monitored using isolated voltage probes and the phase currents are monitored using a Tektronix, 15 A, Hall-effect current probe. These output waveforms can be displayed on a Yokogawa oscilloscope, not shown, or displayed on a PC using a Picoscope virtual oscilloscope.

The Picoscope allows the waveforms to be captured as a data file on the PC, which is then post-processed using MATLAB to obtain the spectrum and compute the harmonic distortion factors. The sampling rate is 20 kSamples/s, so the measurement bandwidth is 10 kHz, which is sufficient to obtain reasonable results for the inverter switching frequencies used.

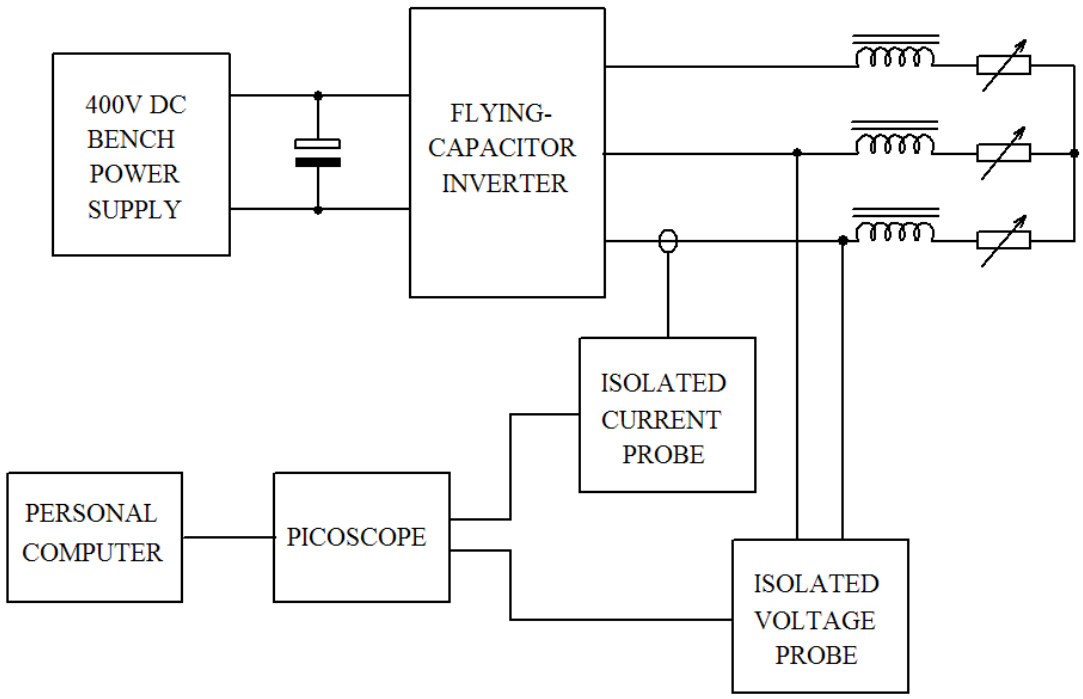


Figure 6.2.6: Block diagram of test and measurement system

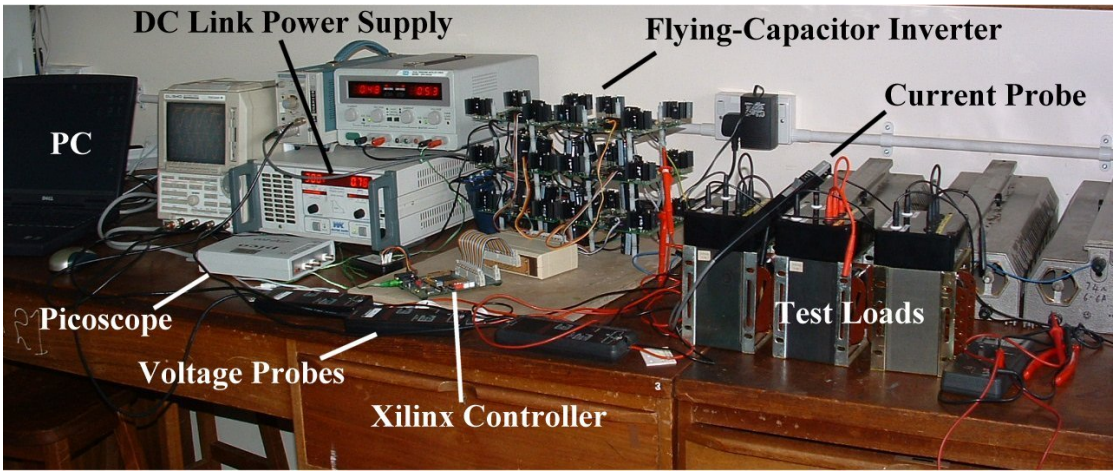


Figure 6.2.7: Test and measurement laboratory setup

6.3 SHE Control Experimental Results

6.3.1 Performance and Balancing

The first sets of results are used to confirm the pre-computed angles for the SHE-4H2 scheme and the cell-capacitor voltage balancing. The measurements were conducted using a 200 V dc power source and high impedance, low current Wye-connected load of 500 Ω and 1 mH. The balancing pattern used is $\overset{7\ E\ D\ B}{3\,6\,C\,9}_{1\ 2\ 4\ 8}$ (PATTERN #1), which was identified during simulation analysis as the optimum balancing pattern.

Figure 6.3.1 shows an oscillogram of the three-phase voltages with respect to the negative dc link and one of the resultant line to line voltages with a unity modulation index for a 50 Hz fundamental. This clearly shows that the cell-capacitor voltages are at the required levels and the inverter has self-balanced. The mean voltages on the phase A limb capacitors are all measured to be less than 1 % of the target values.

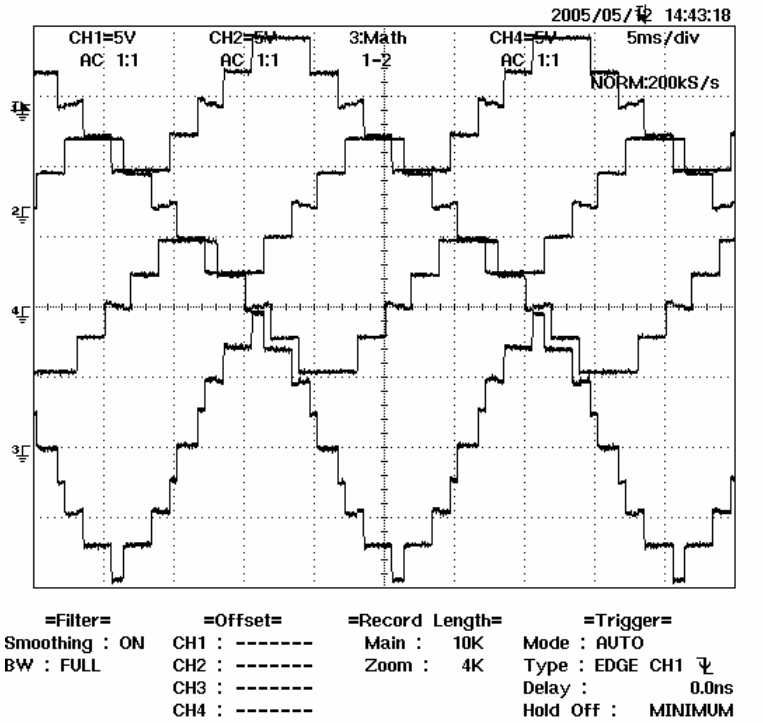


Figure 6.3.1: Oscillogram of the three phase voltages (upper) and a line voltage (bottom) (50 V/div)

A phase voltage and a line voltage waveform were data captured over an 80 ms period (four cycles) using the Picoscope virtual oscilloscope and the data post-processed using an FFT algorithm in the MATLAB environment. Figure 6.3.2 shows the resultant frequency spectra of the voltage waveforms normalised to the 50 Hz fundamental component. As can be seen there is no 5^{th} harmonic (250 Hz) component present in the phase voltage spectrum, indicating that the SHE control is operating correctly. The triplen harmonics present in the phase voltage spectrum are not present in the line voltage spectrum, indicating balanced three-phase output voltage conditions.

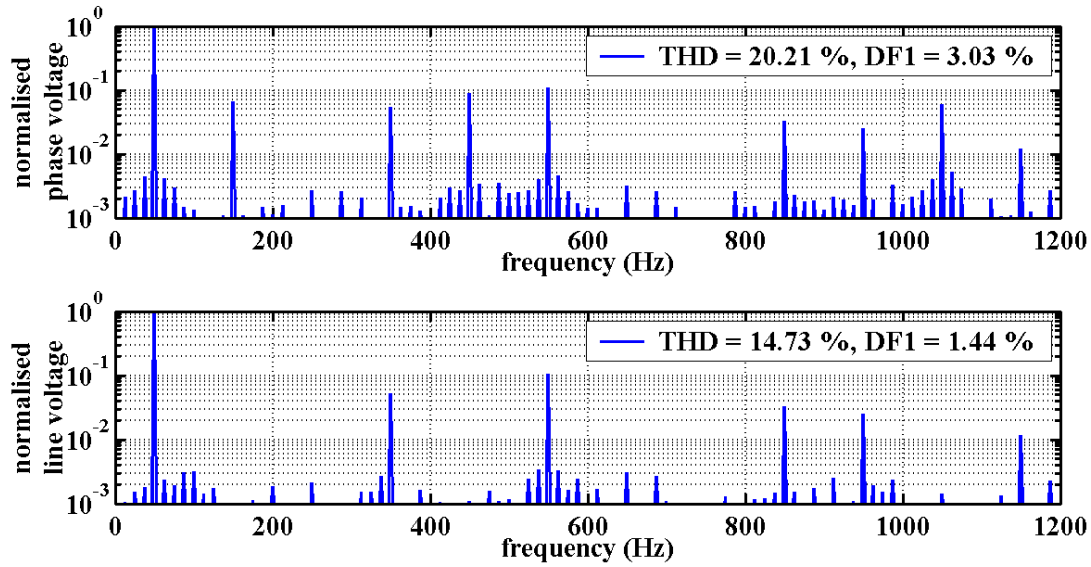


Figure 6.3.2: Phase and line voltage spectra for SHE-4H2 scheme with m_a = 1.0

Further tests were conducted over the whole range of modulation indexes. The measured line voltage THD and DF1 are shown in Figures 6.3.3 and 6.3.4 respectively, together with the simulated characteristics. The overall results show good correlation with the predicted case and indicate that the control is operating correctly over the whole modulation range.

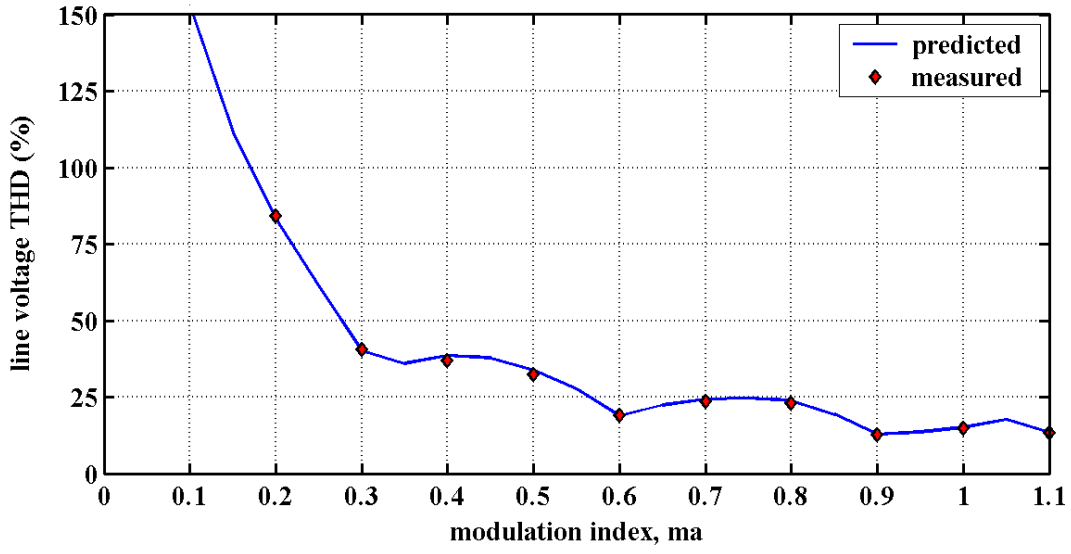


Figure 6.3.3: Variation of line voltage THD against modulation index, m_a

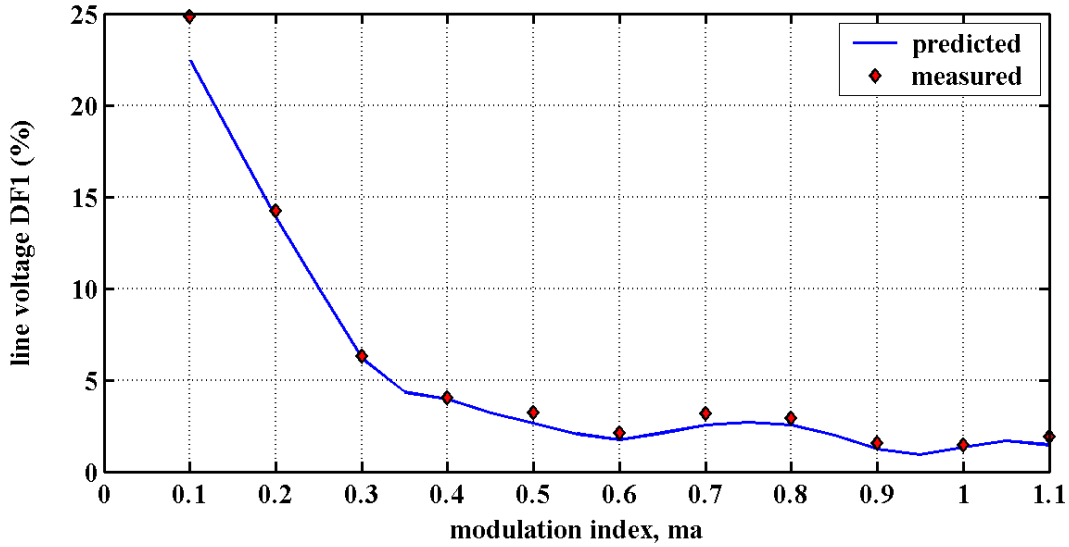


Figure 6.3.4: Variation of line voltage DF1 against modulation index, m_a

The amplitude variation of fundamental and low order harmonics versus modulation depth is shown in Figure 6.3.5. The 5th harmonic is not present above m_a = 0.4 since it is eliminated by the choice of staircase angles. The other low-order harmonics are reasonably low, with peak to peak amplitudes no more than 10 % of dc link voltage, and the fundamental amplitude is shown to be correctly controlled, although there is a slight discernable error at lower modulation indexes due mainly to the voltage drops across the power semiconductors.

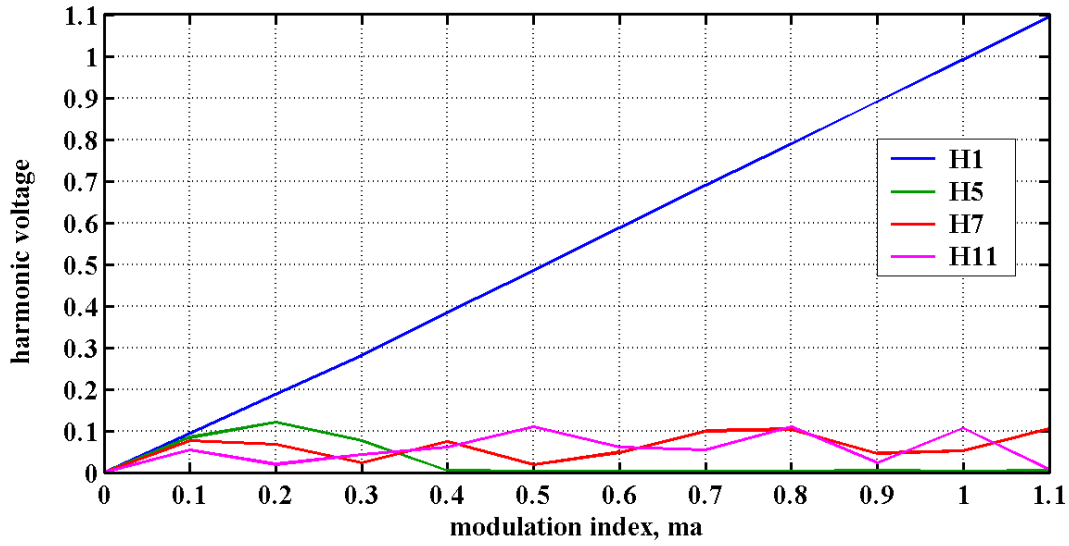
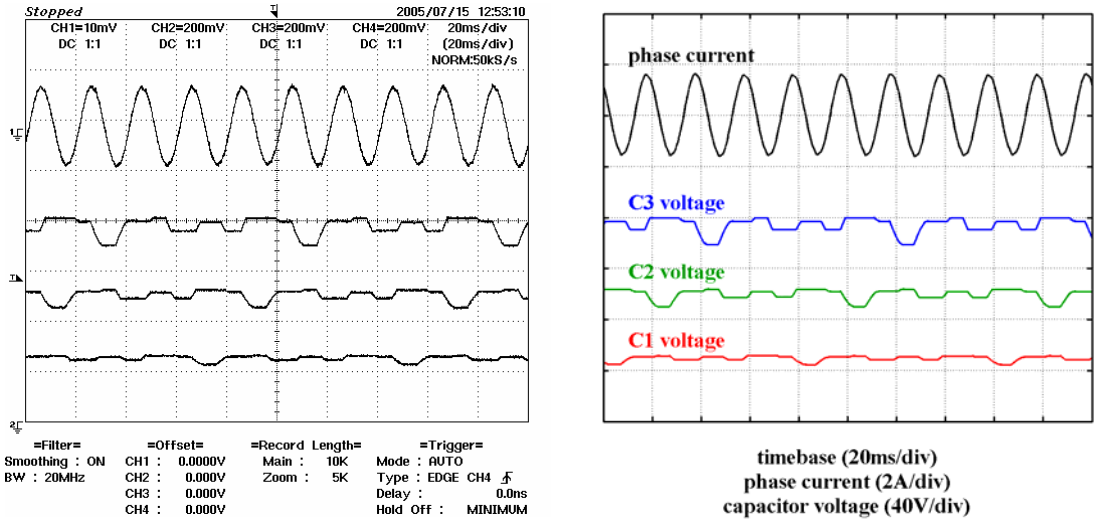


Figure 6.3.5: Amplitude of low order frequency components versus modulation index, m_a

6.3.2 Balancing Pattern Comparison

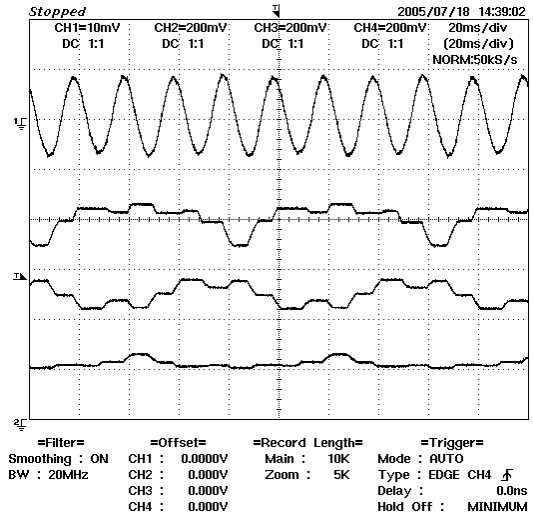
To confirm the predictions of optimum and poor balancing pattern selection for SHE-4H2 control, the load was set to give a system energy factor of 20 and a DPF of 0.6 by setting the load resistances to 37.5 Ω with 160 mH inductors. Various inverter performance parameters were measured when operated with two different balancing patterns; $\overset{7\ E\ D\ B}{3\ 6\ C\ 9}_{1\ 2\ 4\ 8}$ (PATTERN #1) and $\overset{7\ B\ E\ D}{3\ A\ C\ 5}_{2\ 8\ 4\ 1}$ (PATTERN #2).

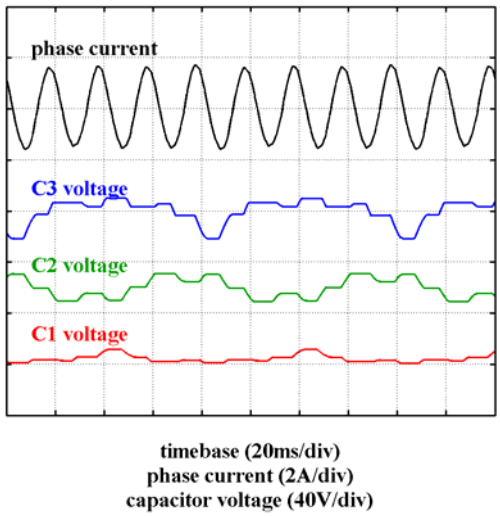
Figures 6.3.6 and 6.3.7 illustrate the effect that the two different balancing patterns have on the cell-capacitor voltage waveforms, with the phase current shown for reference. The repetition frequency of the cell-capacitor voltages is 12.5 Hz in both cases due to the balancing patterns. PATTERN #1 control exhibits a lower peak to peak voltage ripple than the PATTERN #2 case, and the wave shapes agree well with simulation. The resultant three-phase line voltage waveforms are compared in the oscillograms of Figures 6.3.8 and 6.3.9 for the two balancing patterns. It can be seen that the larger capacitor voltage variation of PATTERN #2 leads to an increase in line voltage asymmetry.



a) Experimental waveforms **b) Simulated waveforms**

Figure 6.3.6: PATTERN #1 phase current (top) and cell-capacitor voltages

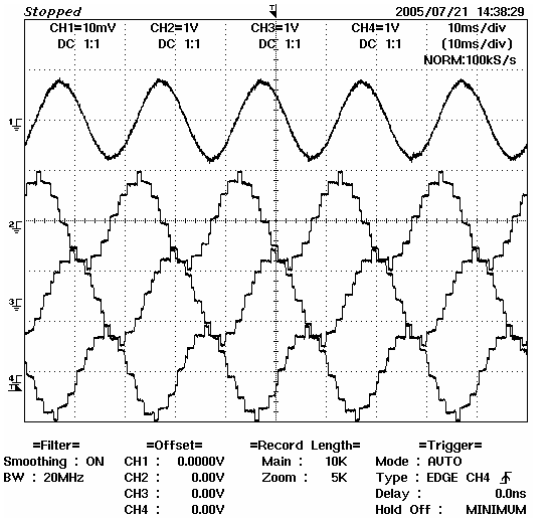


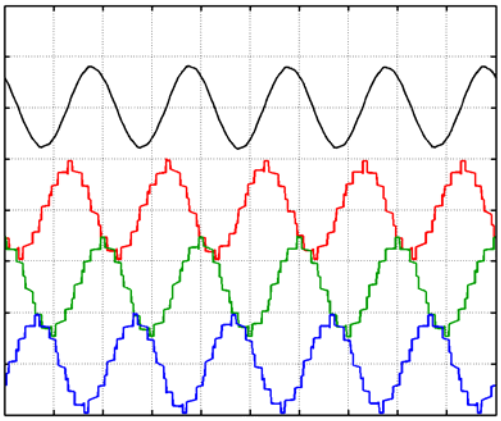


timebase (20ms/div)
phase current (2A/div)
capacitor voltage (40V/div)

a) Experimental waveforms **b) Simulated waveforms**

Figure 6.3.7: PATTERN #2 phase current (top) and cell-capacitor voltages

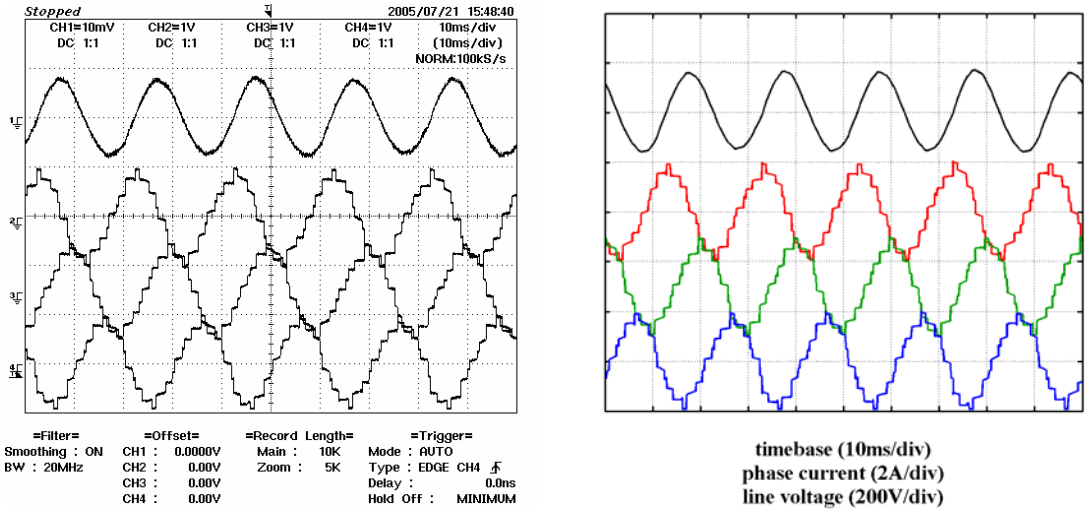




timebase (10ms/div)
phase current (2A/div)
line voltage (200V/div)

a) Experimental waveforms **b) Simulated waveforms**

Figure 6.3.8: PATTERN #1 phase current (top) and line voltages



a) Experimental waveforms **b) Simulated waveforms**

Figure 6.3.9: PATTERN #2 phase current (top) and line voltages

The measured electrical parameters of the inverter show good correlation with the predicted values, as can be seen in Table 6.3.1. The power electronics losses are close to those predicted and validate the IGBT/diode models used in the simulation.

	PATTERN #1		PATTERN #2	
	Predicted	**Measured**	**Predicted**	**Measured**
Input Voltage (V)	200	200	200	200
Input Current (A)	0.75	0.76	0.77	0.77
Input Power (W)	150	152	153	153
Output Power (W)	138	134	141	141
Phase Current (Arms)	1.11	1.09	1.12	1.12
Line Voltage (Vrms)	121.9	120.9	121.6	121.5

Table 6.3.1: Operating performance of different balancing patterns

There is a marked difference in the harmonic content of the line voltage between the two operating patterns as can be seen in the spectra plots of Figures 6.3.10 and 6.3.11. These show that balancing PATTERN #1 offers improved performance with lower unwanted harmonics, especially at 100 and 125 Hz. The computed THD and spectral signature of the measured voltages show good agreement with that predicted by simulation in both cases.

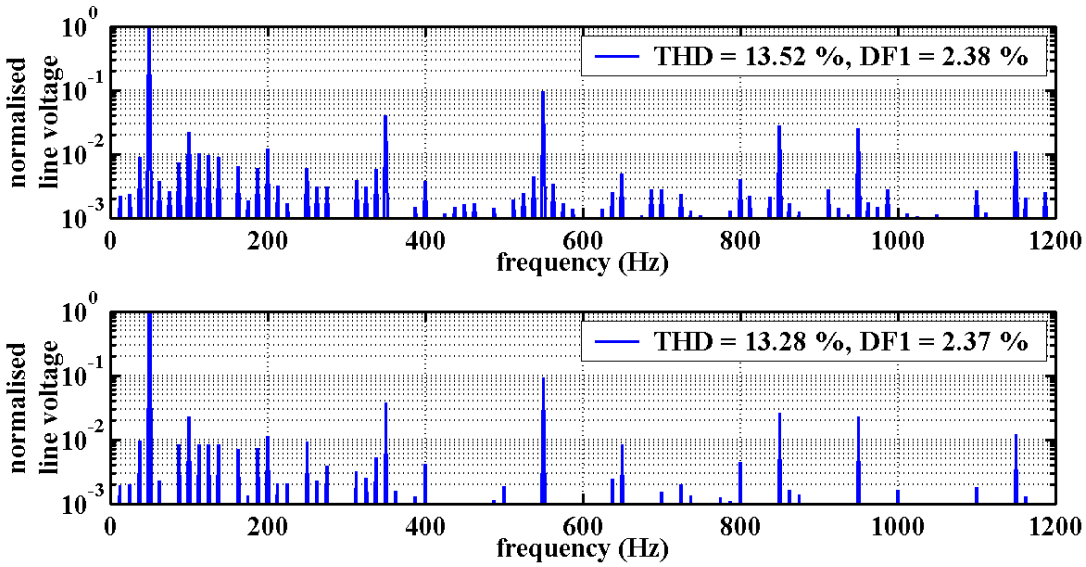


Figure 6.3.10: Line voltages spectra for PATTERN #1, experimental (top) and simulated (bottom)

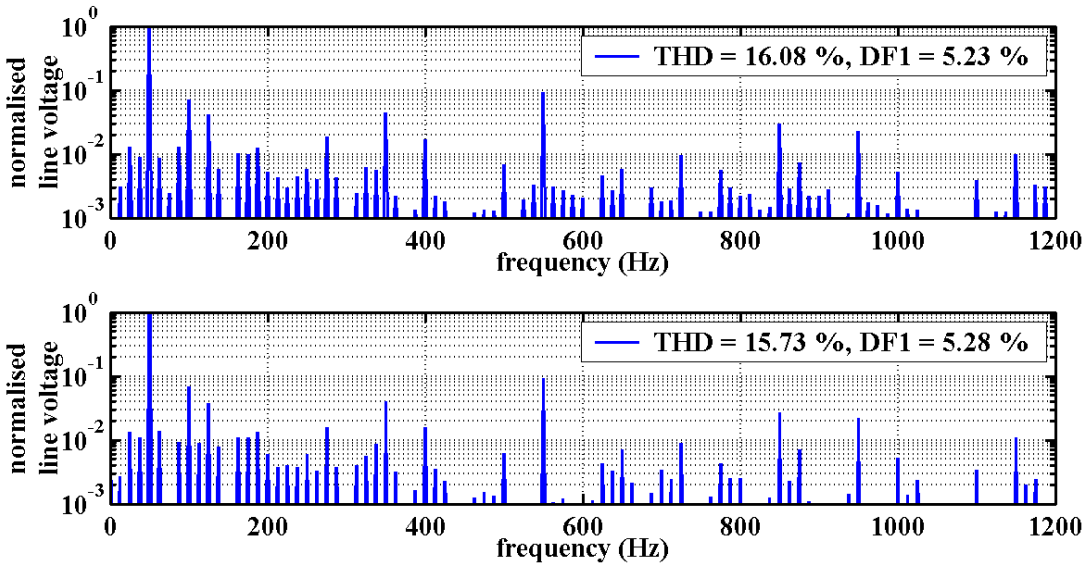


Figure 6.3.11: Line voltages spectra for PATTERN #2, experimental (top) and simulated (bottom)

6.3.3 Variable Load Performance

Further tests were conducted to confirm the THD contour characteristic for different system energy factors and load displacement power factor. The optimum balancing PATTERN #1 with SHE-4H2 control was used with a unity modulation index. Two different load inductors (160 mH and 40 mH) were used with variable resistors ranging from 15 to 70 Ω. Figure 6.3.12 shows the measured line voltage THD and DF1, and phase current THD curves for the 160 mH inductance case. As can be seen

there is good correlation between the predicted and measured characteristics in the case of the line voltage. The line voltage THD curve clearly shows the reduction in harmonics from the ideal level in the $\xi = 25$ region. The measured phase current THD follows the general trend of the predicted values with reasonable accuracy given the very low amplitudes of the harmonics being measured.

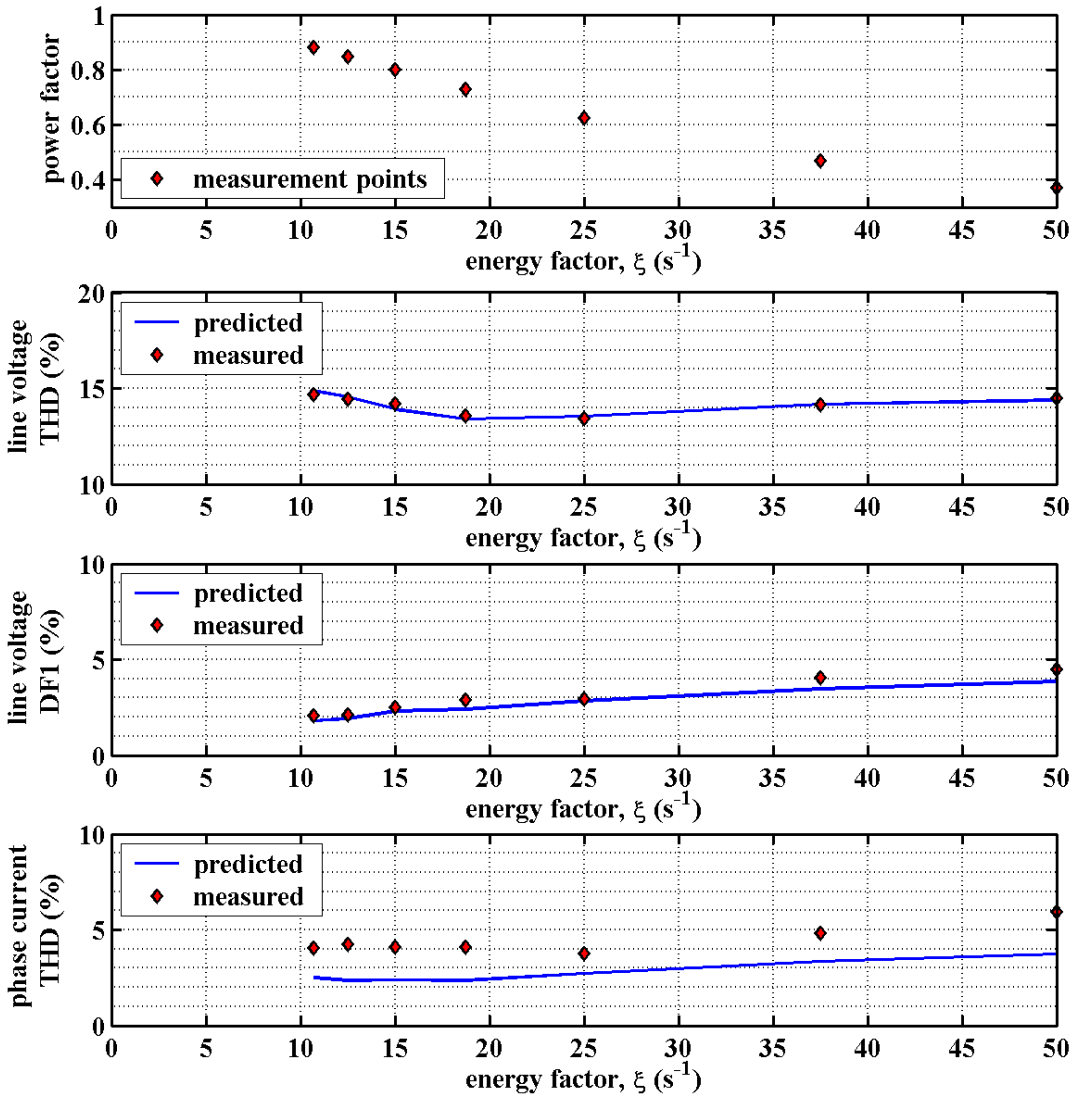


Figure 6.3.12: Variation of power quality indicators for a 160 mH inductive load

Figure 6.3.13 shows the same set of curves for the 40 mH inductance case. Here too good agreement with predicted and measured distortion factors is established, especially at lower energy factors.

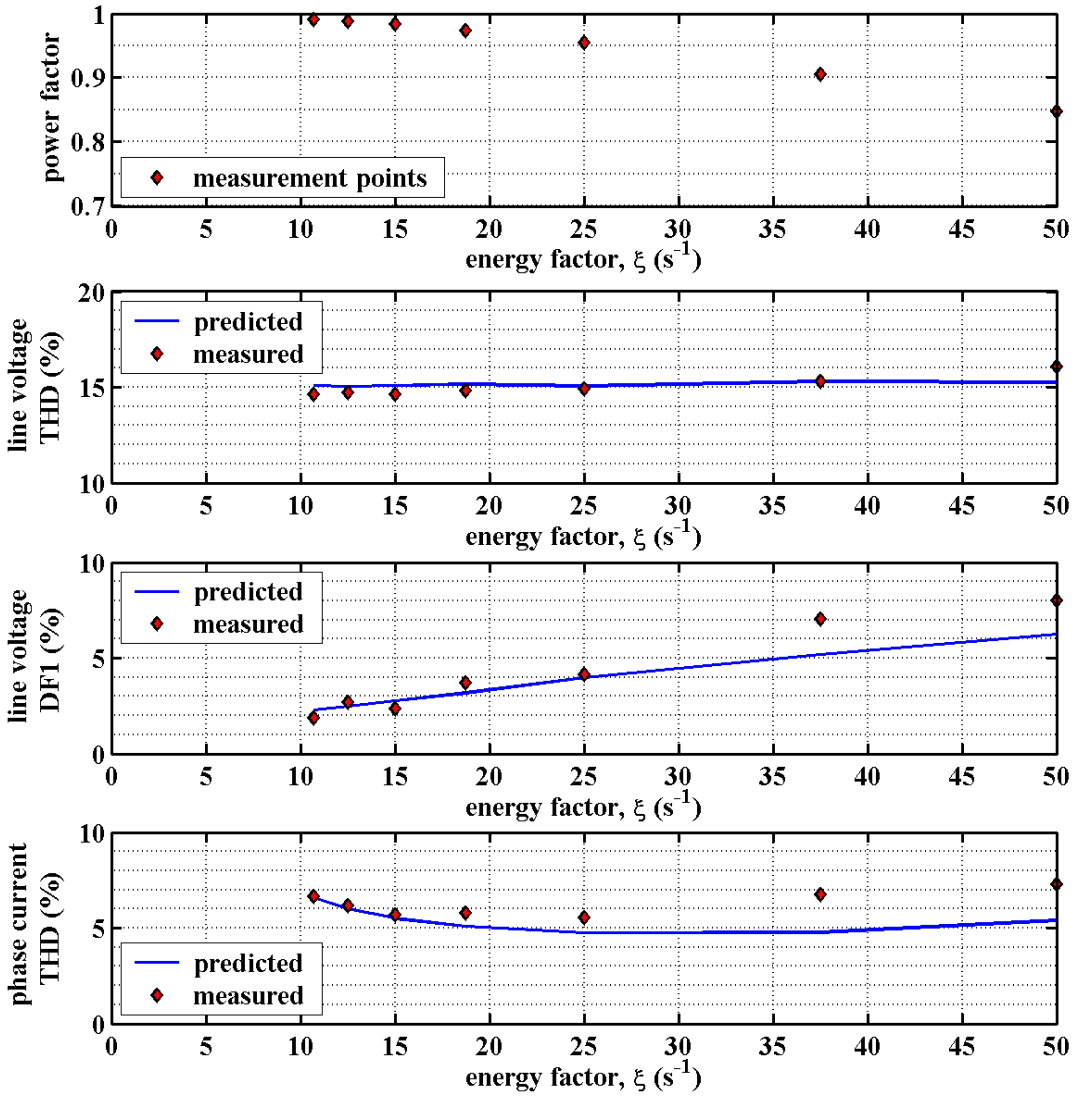
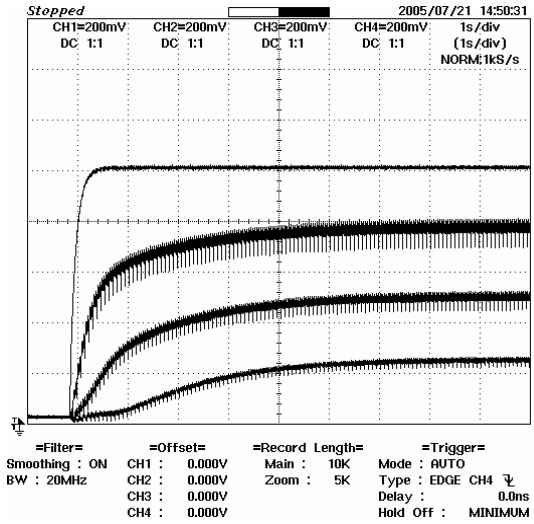


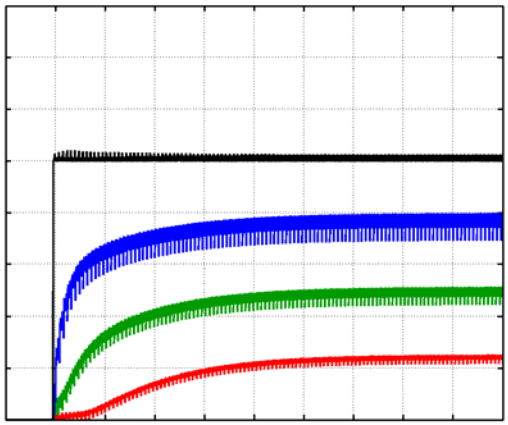
Figure 6.3.13: Variation of power quality indicators for a 40 mH inductive load

6.3.4 Input Voltage Transient Behaviour

The effect of sudden changes to the input voltage supply was investigated on a 37.5 Ω plus 160 mH load. The 1 mF capacitor remained in circuit for this test and the bench dc power source was turn-on and –off. Figure 6.3.14 shows the transient behaviour of the cell-capacitor voltages as they build-up once a step input voltage of 200 V was applied. The measured waveforms compare well with the simulated behaviour

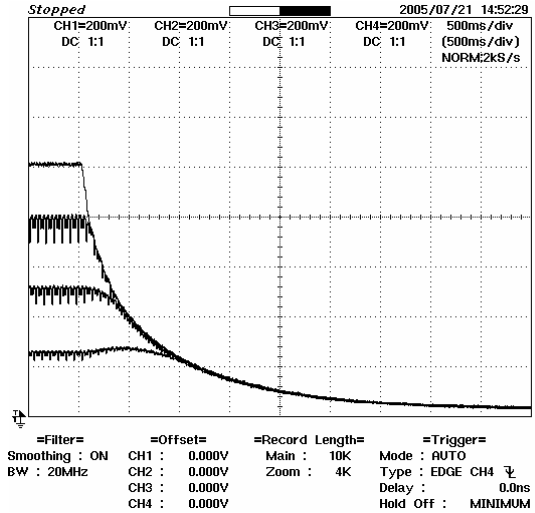
Figure 6.3.15 shows the decay behaviour of the cell-capacitor voltages as the input voltage supply was removed. There is fairly good correlation between the measured and simulated waveforms, although in this case the inverter model does show some imperfections in how it treats current flow between adjacent capacitors when they are at the same potential.

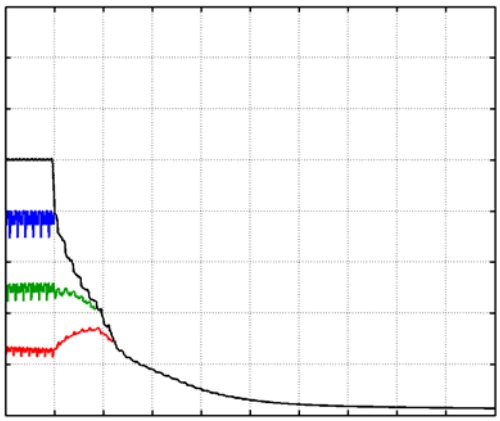




a) Experimental waveforms **b) Simulated waveforms**

Figure 6.3.14: Turn-on transient input voltage, capacitor voltage variation





a) Experimental waveforms **b) Simulated waveforms**

Figure 6.3.15: Turn-off transient input voltage, capacitor voltage variation

6.4 PWM Experimental Results

The detailed simulation of both sine-triangle and space vector PWM control with an open-loop balancing approach based on a sub-carrier swapping logic block revealed that minimising duty cycle errors plays an important role for stable operation. A suggested approach involved using a VCOX where the FPGA clock is dynamically adjusted to ensure that bit errors are minimised while achieving an accurate fundamental frequency in the output waveforms. The present hardware

implementation uses a proprietary Xilinx development PCB, and so does not possess the necessary circuitry to implement a VCOX. To achieve minimal bit errors, the fundamental frequency must therefore be adjusted so that the following relationship holds,

$$8N_c m_f = 4N_b\left(m_f - 1\right) = 4M \quad \ldots (6.4.1)$$

where

M is the number of FPGA clock cycles in one period (SINE PERIOD)

N_c is the maximum carrier count (CARRIER PERIOD)

N_b is the maximum balancing counter count (BALANCE PERIOD)

To adjust M to minimise bit errors, first calculate the number of FPGA clock pulses in one target fundamental period using,

$$M = \frac{f_{FPGA}}{f_1} \quad \ldots (6.4.2)$$

At the desired switching frequency an adjustment constant k_e is then calculated using,

$$k_e = ROUND\left(\frac{M}{2m_f\left(m_f - 1\right)}\right) \quad \ldots (6.4.3)$$

Finally, the modified M is computed using the relationship,

$$M = 2k_e m_f\left(m_f - 1\right) \quad \ldots (6.4.4)$$

The new values of N_c and N_b are then computed using (6.4.1).

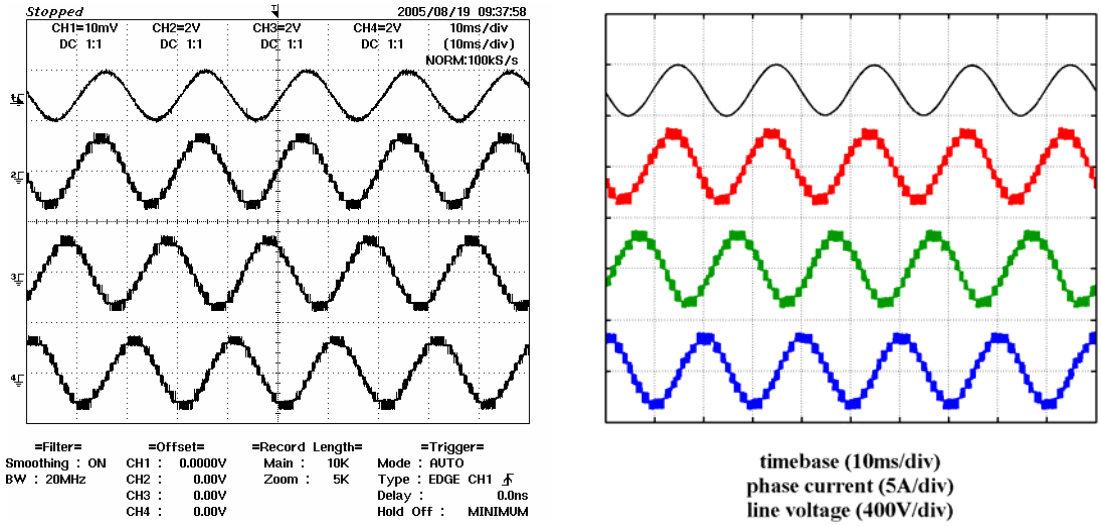
Table 6.4.1 shows a range of M, N_b and N_c values for different m_f values when the target fundamental frequency is 50 Hz, with an FPGA clock of 25 MHz.

m_f	Switching frequency (kHz)	SINE PERIOD, M	Fundamental, f_1 (Hz)	CARRIER PERIOD, N_c	BALANCE PERIOD, N_b
30	1.5	499380	50.062	8323	17220
40	2.0	499200	50.080	6240	12800
60	3.0	502680	49.733	4189	8520
120	6.0	514080	48.631	2142	4320
180	12.0	515520	48.495	1432	2880

Table 6.4.1: Modulation control variables to reduce bit errors for PWM

6.4.1 Sine-Triangle PWM Pattern-Based System Balancing

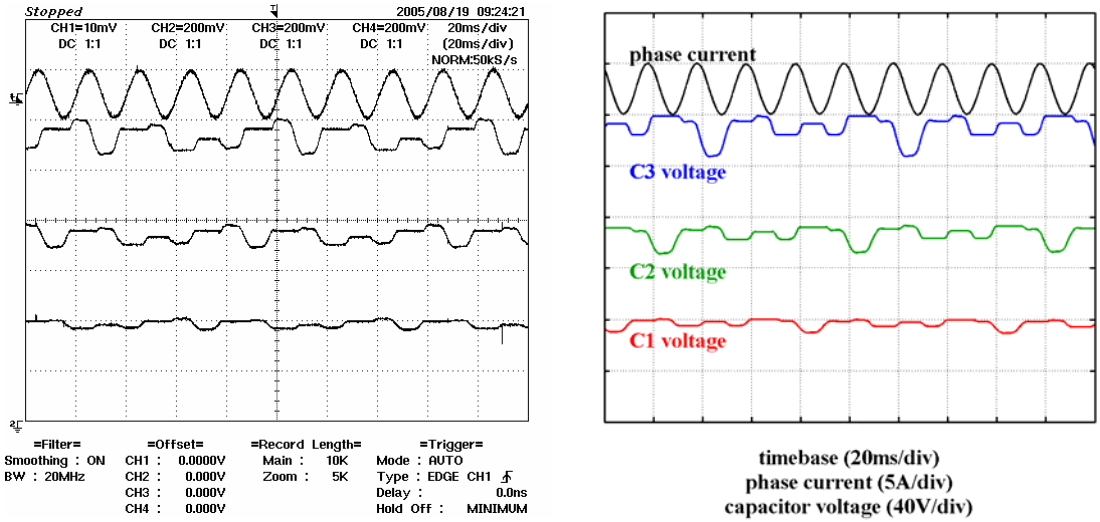
The balancing scheme applied to control the inverter when operating with SHE sinusoidal synthesis can also be used when operating with sine-triangle PWM. Figure 6.4.1 shows the experimental line voltage waveforms for the inverter switching at 3 kHz (m_f = 60) with asymmetric sampled reference, PD carrier placement and balancing using the optimum PATTERN#1. The three-phase load is 37.5 Ω and 160 mH, and the dc link voltage is 300 V. As can be seen, the voltages are well balanced indicating that the inverter is operating with the correct cell-capacitor voltages. The nine voltage levels at 75 V steps can be clearly seen.



a) Experimental waveforms **b) Simulated waveforms**

Figure 6.4.1: Phase current (top) and line voltages with pattern balancing

The actual voltage ripple on the cell-capacitors for phase A, are shown in Figure 6.4.2. As would be expected, the waveforms are almost identical to those seen when operating with SHE control. Although correct operation of the inverter is achieved with this form of balancing control, the large voltage ripple leads to significant variation in the blocking voltage across the switches, and will limit the maximum operating power range of the inverter.



a) Experimental waveforms **b) Simulated waveforms**

Figure 6.4.2: Phase current (top) and cell-capacitor voltages for pattern balancing

The effect of the voltage ripple on the harmonic spectra of the load waveforms is shown in Figure 6.4.3. The PD scheme is characterised by a significant harmonic peak at the switching frequency (3 kHz) in the phase voltage spectrum, which is cancelled out in the line voltage spectrum. The effect of the cell-capacitor voltage ripple is to introduce additional low frequency harmonics associated with its 12.5 Hz fundamental. This leads to the significant low frequency harmonics seen in the current spectra.

The measured harmonic spectra can be compared with the predicted levels under the same operating conditions. Figure 6.4.4 shows the spectra for the phase voltage, line voltage and phase current. The more significant harmonic peaks in the measured spectra are in line with those predicted by simulation. The higher background noise spectral components in the measured spectra are due to the 8-bit ADC sampling resolution of the Picoscope instrument. In the case of the current, the maximum range was set to ±10 A and so the bit resolution was 78 mA, and this adversely affects the phase current spectrum and THD calculation.

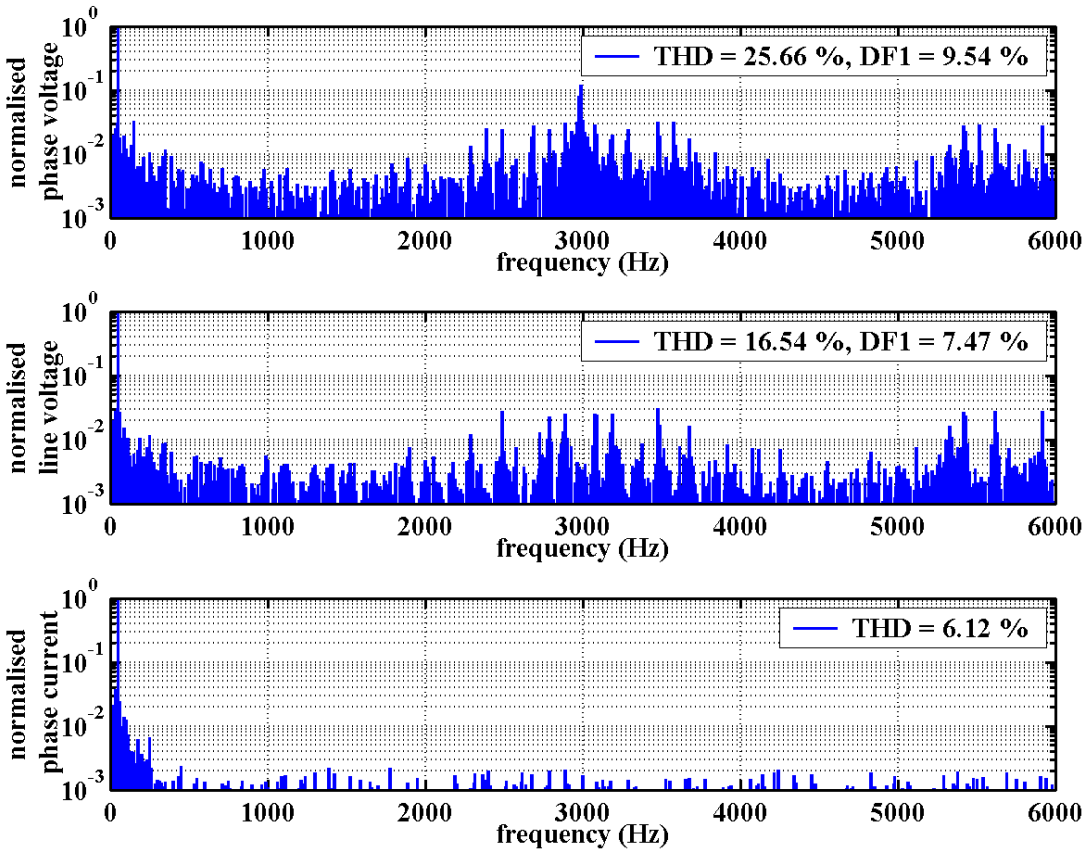


Figure 6.4.3: Experimental PWM load waveform spectra

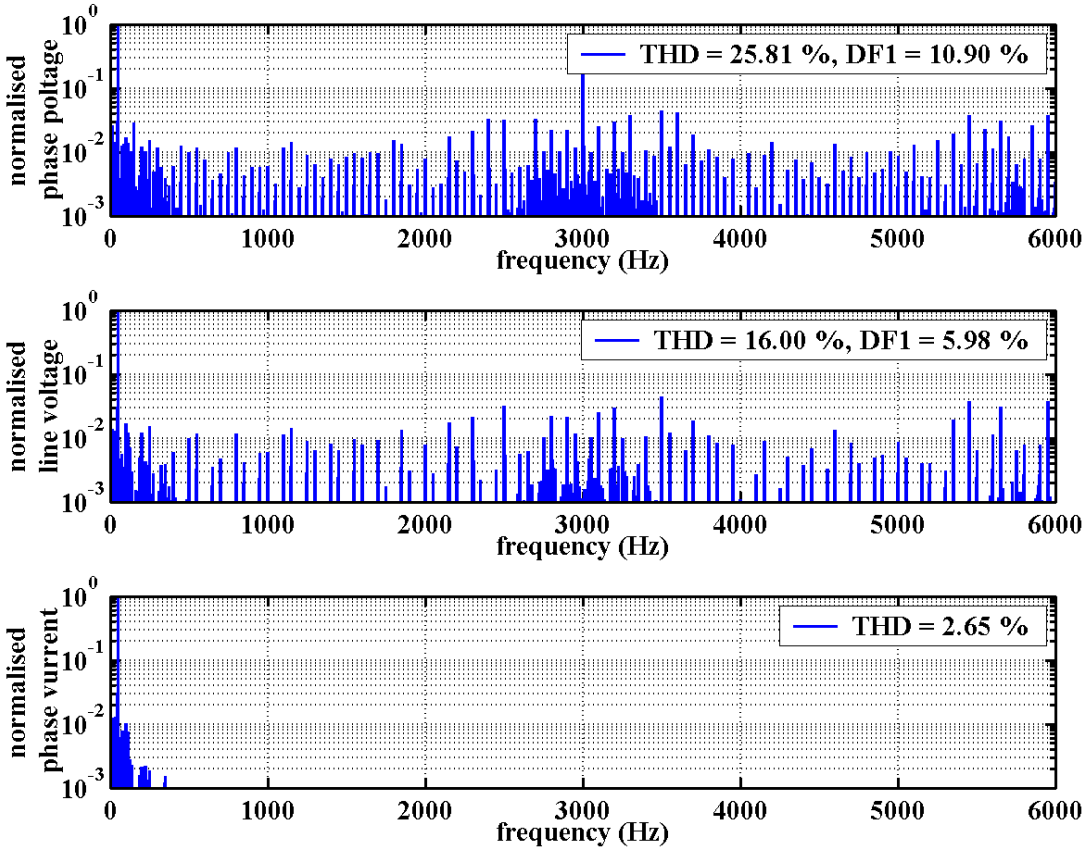


Figure 6.4.4: Simulated PWM load waveform spectra

6.4.2 Sine-Triangle PWM Sub-Carrier Rotation Balancing

The sub-carrier balancing scheme developed using the aid of the simulator in Chapter 4, is aimed at reducing the voltage ripple on the cell-capacitors. It was shown that the performance of this method relies on very accurate timing in the digital control implementation. In the experimental inverter, there are unequal delays in the interface and isolation circuitry between the Xilinx controller and the power electronics gate drivers. This places an operating frequency limitation on the existing inverter design, since the delays cause a mismatch between the average duty cycles for the different cell blocks. Figure 6.4.5 shows the variation in line voltage and phase current THD versus switching frequency. As can be seen, the quality of the output voltage deteriorates as the switching frequency increases. This would not be acceptable in a practical system, and further work is required to improve the design of the isolation interface circuitry between the Xilinx controller and the IGBT gate drivers. However, acceptable operation is demonstrated in the prototype inverter when using a 1.5 kHz (m_f = 30) switching frequency.

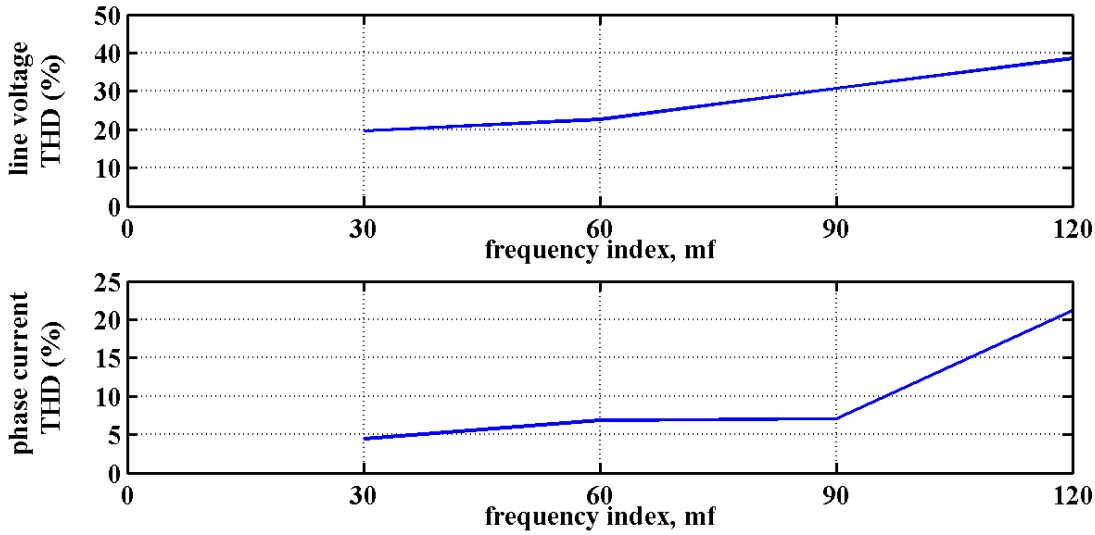
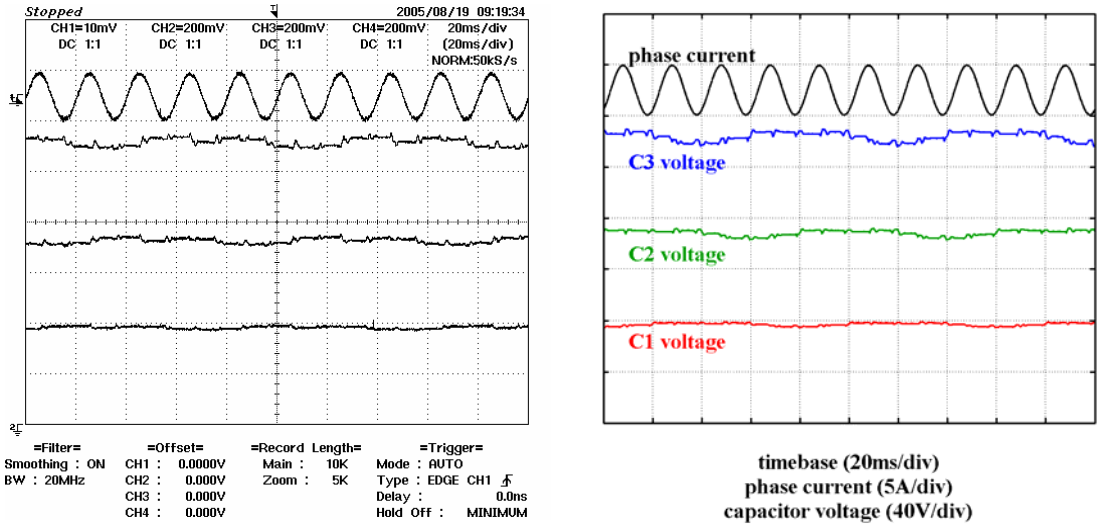


Figure 6.4.5: Performance of prototype inverter for different switching frequencies

Figure 6.4.6 shows the resultant cell-capacitor voltages when the sub-carrier balancing system is operating with a PD PWM scheme. As can be seen, the ripple voltage is significantly reduced compared with previous pattern-based balancing scheme. The implication of this is that the inverter can now supply at much higher power levels without compromising the safe-operation of the IGBTs and diodes. The measured mean voltages across each capacitor are 78.6 V, 142.5 V and 218.8 V, and these values compare favourably with the predicted 77.1 V, 148.1 V and 223.9 V.



a) Experimental waveforms **b) Simulated waveforms**

Figure 6.4.6: Phase current (top) and cell-capacitor voltages

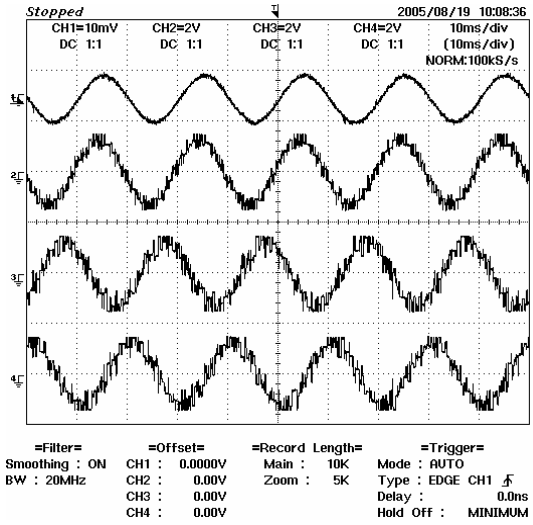
The system performance breakdown is listed in Table 6.4.2 which compares the measured and predicted system quantities. There is general agreement with the measured and predicted results, although the measured output power is 5 % higher than predicted, which is due to the non-linear characteristic and increased losses of the inductor not being taken into account in the model. There are also some additional losses since the simulator does not include parasitic effects and losses associated with other components in the power electronics stage.

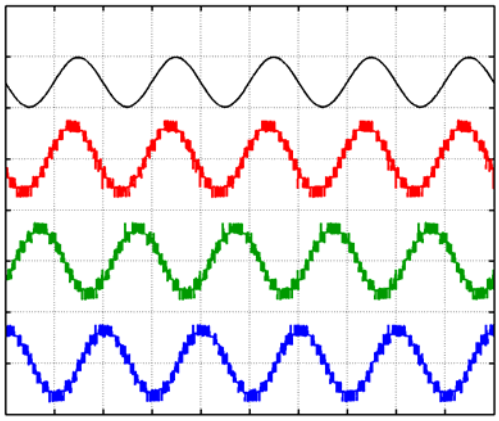
	Predicted	**Measured**
Input Voltage (V)	300	300
Input Current (A)	1.08	1.33
Input Power (W)	351	399
Output Power (W)	333	352
Phase Current (Arms)	1.72	1.77
Phase Voltage (Vrms)	107.4	105.1
Line Voltage (Vrms)	181.9	181.8

Table 6.4.2: Operating performance of different balancing patterns

The three-phase load line voltages are shown in Figure 6.4.7. This shows that the system is operating in a balanced fashion. There is, however, an increase in ripple on Phase C due to an increase in asymmetry in the timing of the eight gate-drive signals.

The effect of this is a noticeable increase in distortion in the bottom two line voltage waveforms.

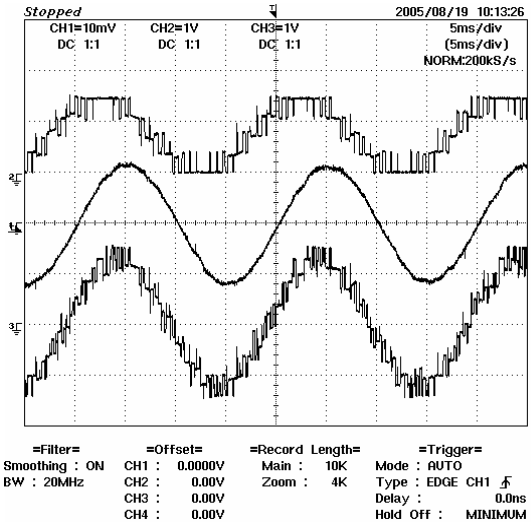


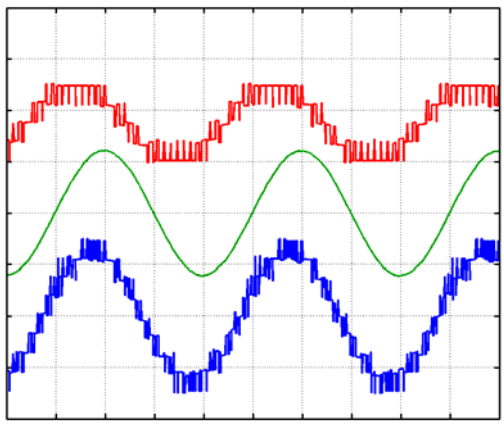


a) Experimental waveforms **b) Simulated waveforms**

Figure 6.4.7: Phase current (top) and line voltages

Figure 6.4.8 shows an expanded view of a phase voltage, phase current and line voltage. The measured waveforms are very similar to those predicted by simulation.





a) Experimental waveforms **b) Simulated waveforms**

Figure 6.4.8: Phase voltage (top), phase current (middle) and line voltage (bottom)

The spectra for the load waveforms are shown in Figure 6.4.9. The PD characteristic switching frequency peak in the phase voltage spectrum at 1.5 KHz is clearly present, but cancelled in the line to line voltage. There are less low frequency harmonics because of the reduced cell-capacitor voltage ripple, although these are not completely eliminated. The measured results can be compared with the predicted spectra shown in Figure 6.4.10. This shows the simulated load waveform spectra under the same operating conditions. There is good correlation between the measured and predicted spectra, especially in the more significant harmonic peaks.

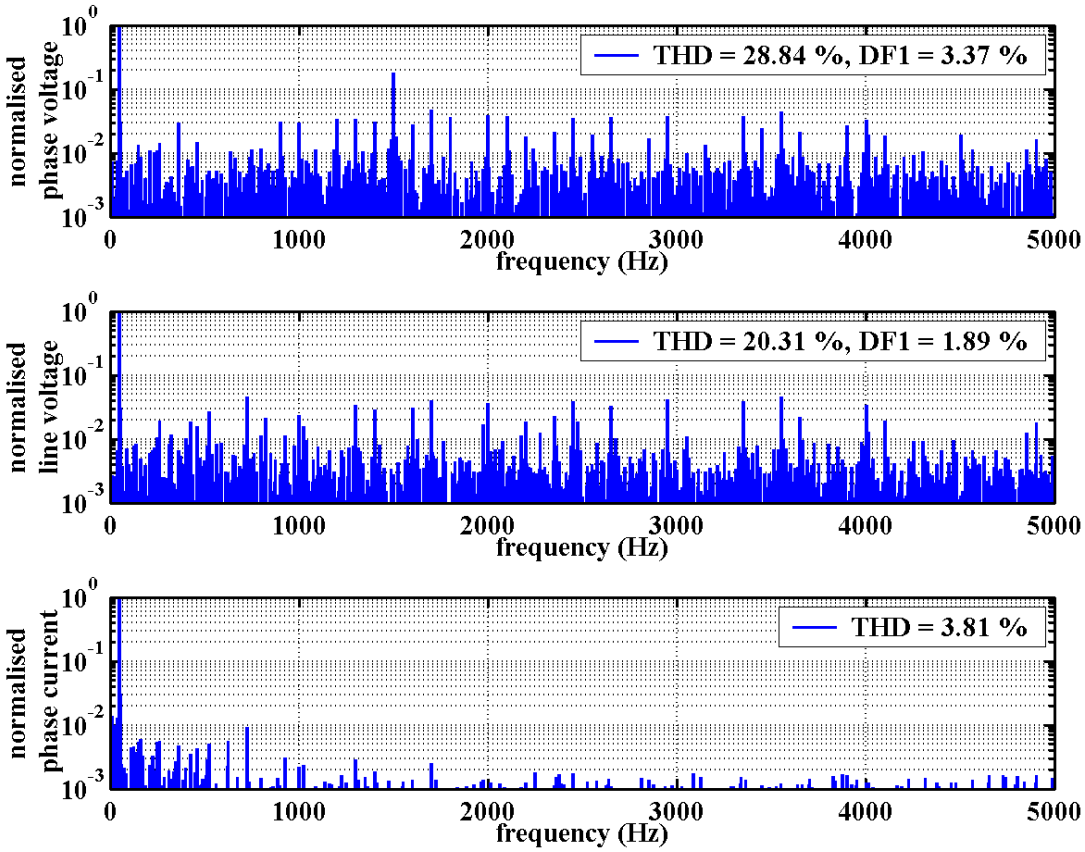


Figure 6.4.9: Measured PD PWM load waveform spectra

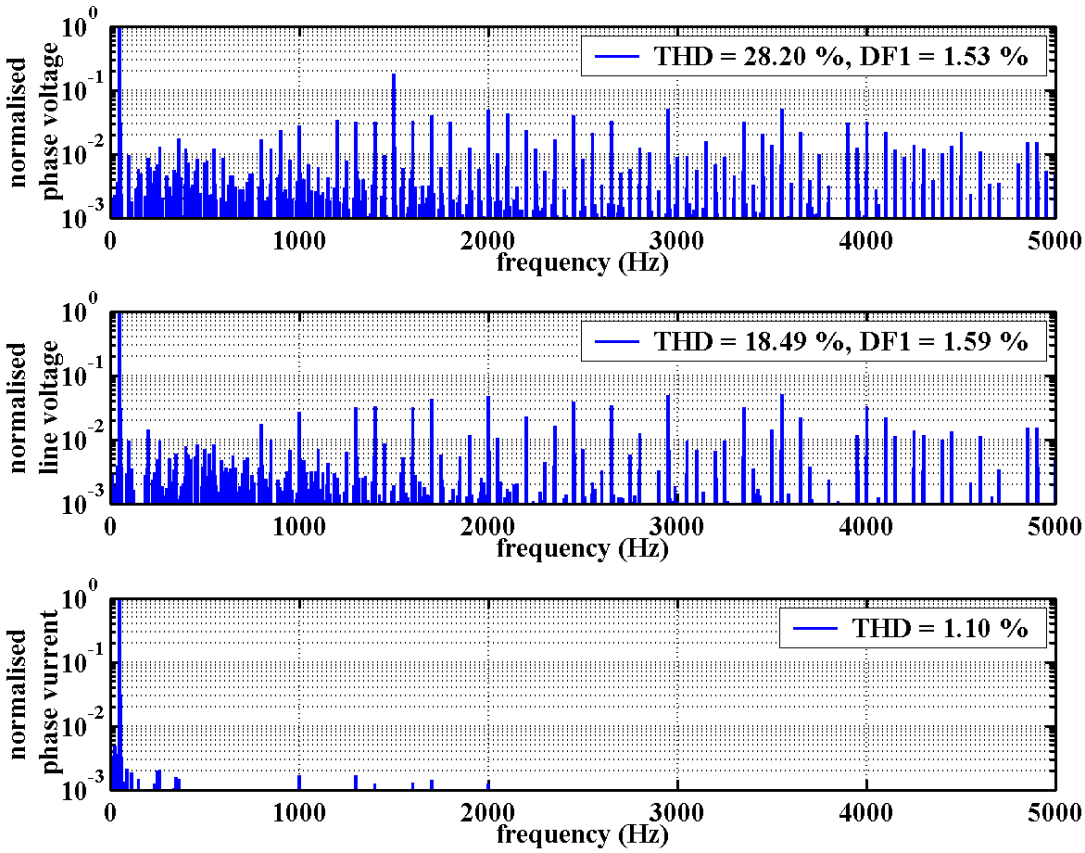


Figure 6.4.10: Simulated PD PWM load waveform spectra

6.4.3 Modulation Depth Variation

The inverter's performance under different modulation depths was measured and the results are presented in Figure 6.4.11. These graphs were produced by post-processing the sampled line voltage waveform at the different operating points. This shows that the harmonic distortion increases as the output amplitude is reduced by the controller. There is good correlation between the measured and predicted line voltage THD. The measured phase current THD is higher in all cases but the trend agrees with the predicted curve. The bottom graph of demand verses actual fundamental amplitude illustrates the excellent operation of the modulation control scheme with no closed-loop voltage feedback control.

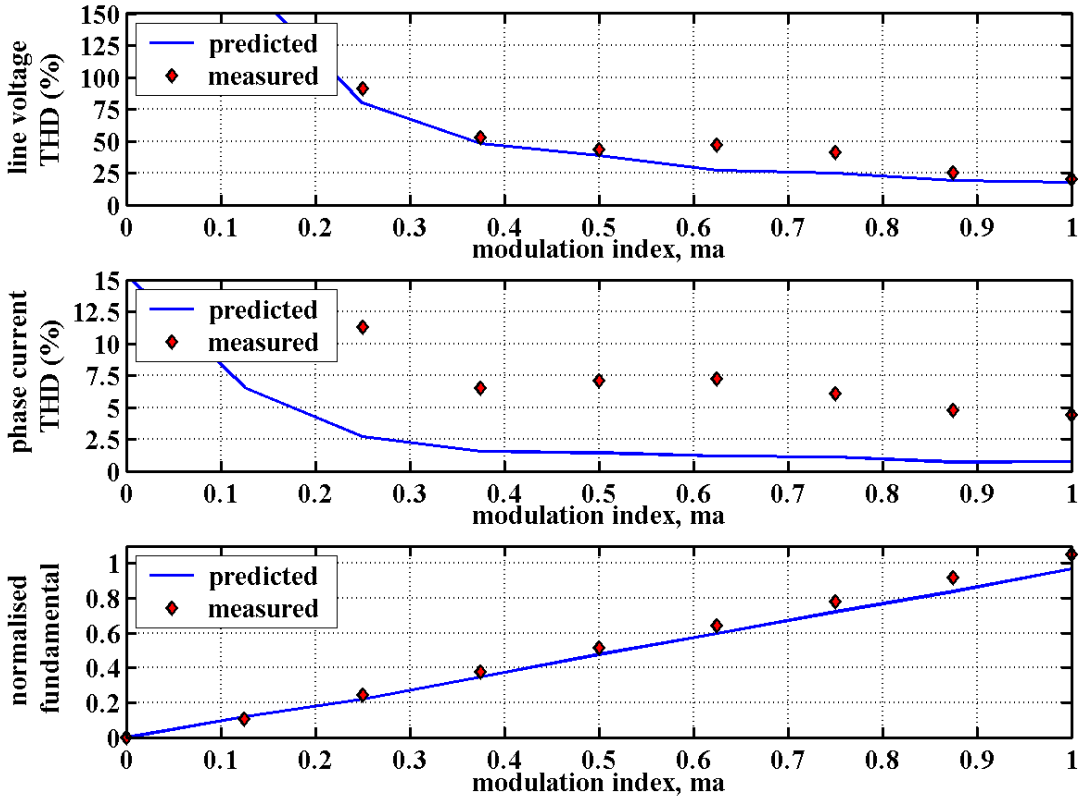


Figure 6.4.11: Performance variations at different modulation depths

6.4.4 Sine-Triangle PWM Carrier Schemes

It has already been seen in Chapter 4 that there are a variety of different multilevel sine-triangle PWM implementations possible, using different carrier positions with respect to each other. Figures 6.4.12 and 6.4.13 show the measured phase voltage and line voltage spectra for the three main disposed carrier implementations with asymmetric reference sampling at a switching frequency of 1.5 kHz (m_f = 30) and unity modulation depth (m_a = 1). As can be seen, the PD scheme offers the lowest line voltage harmonic distortion, whilst APOD gives the worst performance. This agrees with the simulated performance where the line voltage THD values are predicted to be 18.49% (PD), 22.77% (POD) and 26.55% (APOD).

Figure 6.4.14 shows the measured phase current spectra for the three different carrier schemes. In this case PD and APOD schemes lead to similar low harmonic distortion in the current waveform, and the POD scheme causes more distortion although the differences are not significant.

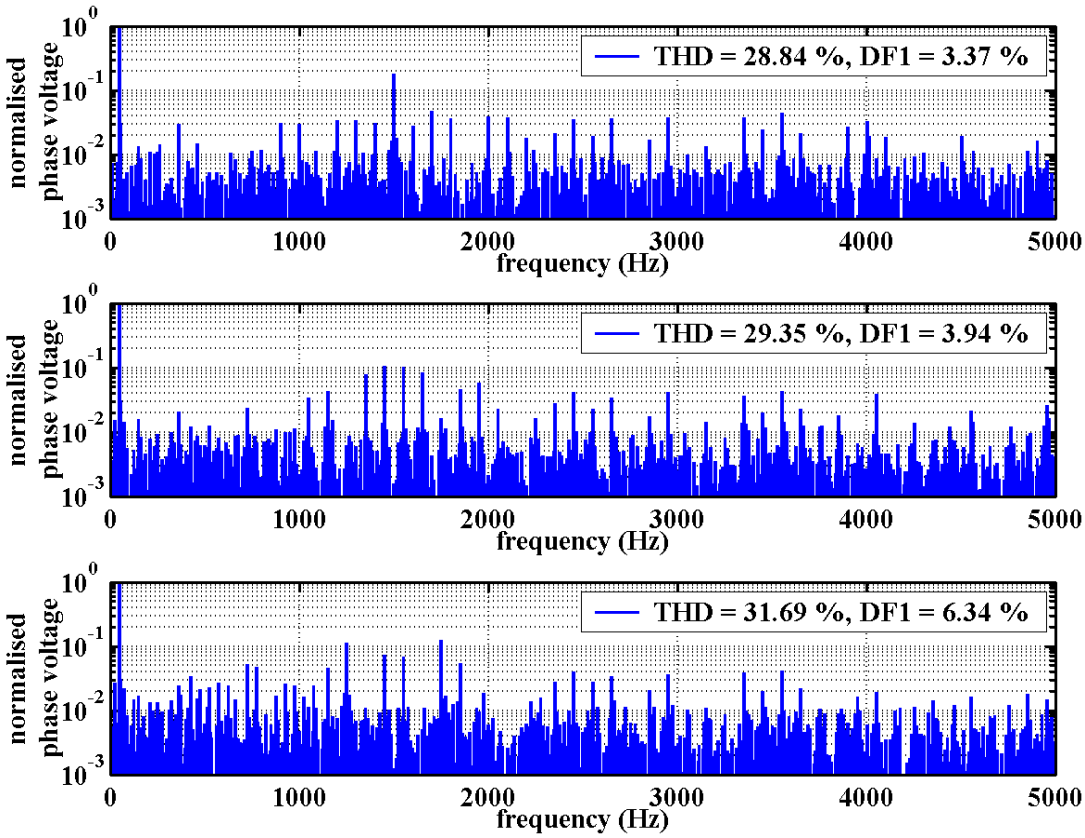


Figure 6.4.12: Phase voltage spectra. PD (top), POD (middle) and APOD (bottom)

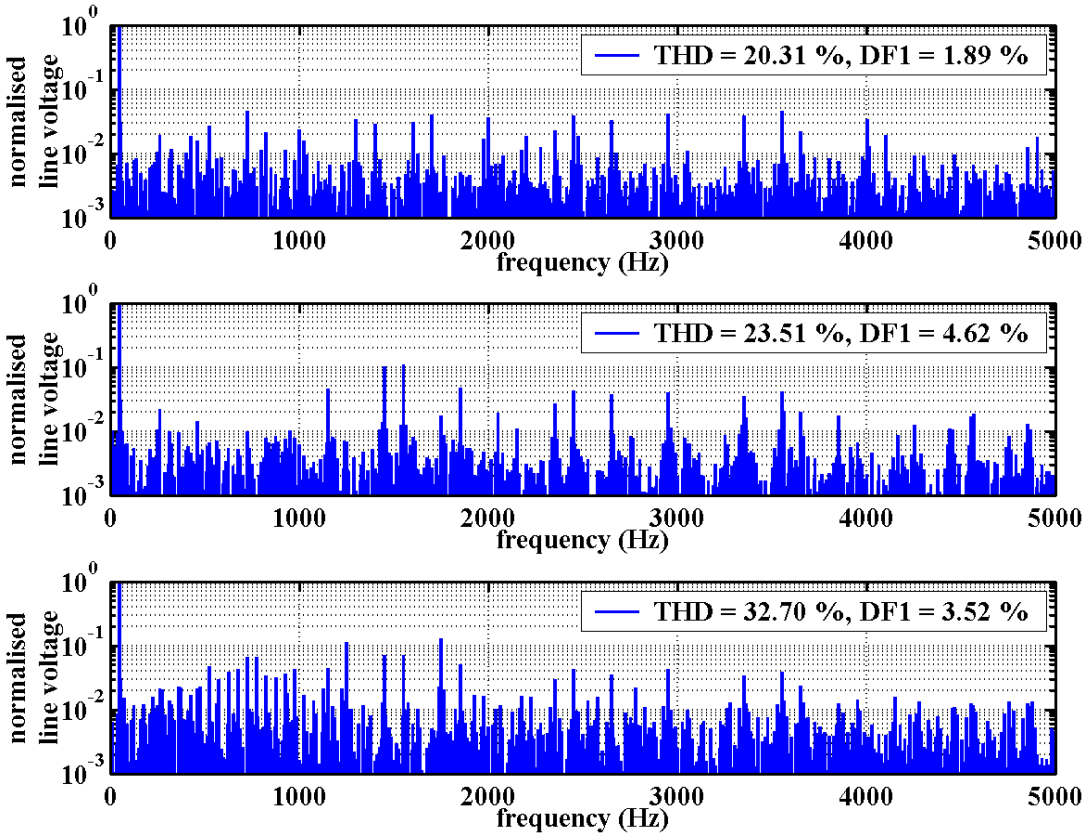


Figure 6.4.13: Line voltage spectra. PD (top), POD (middle) and APOD (bottom)

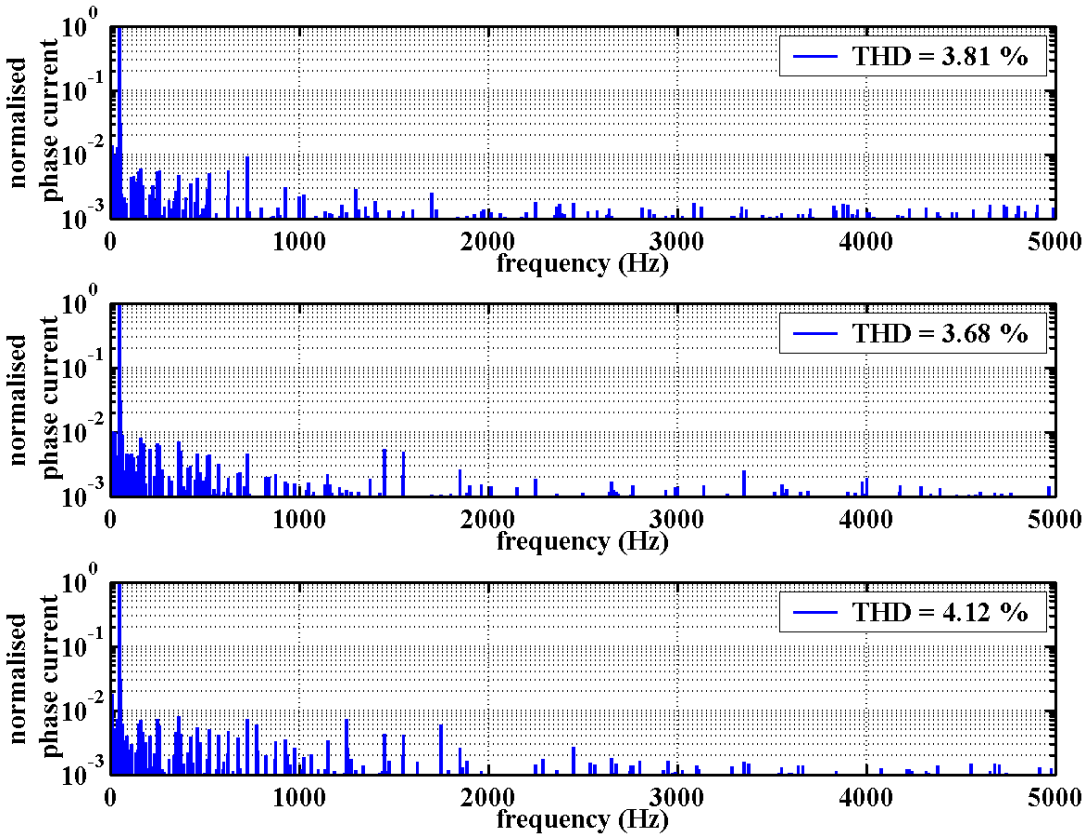


Figure 6.4.14: Current spectra. PD (top), POD (middle) and APOD (bottom)

6.4.5 Third Harmonic Injection Sine-Triangle PWM

The introduction of a third harmonic to the reference is beneficial in increasing the range of the modulation depth above unity. Simulations also suggest that when using PD carriers, the modified reference does not lead to poorer performance. Figure 6.4.15 shows the experimental inverter waveforms with this form of control at a unity modulation depth with a 300 V dc link. The switching frequency is 1.5 kHz and the injected third harmonic sinusoid amplitude is a sixth of the fundamental sinusoid. The effect on output quality performance can be seen in the line voltage and phase current spectra shown in Figure 6.4.16. When compared with the PD scheme in the figures above, it can be seen that performance is broadly similar.

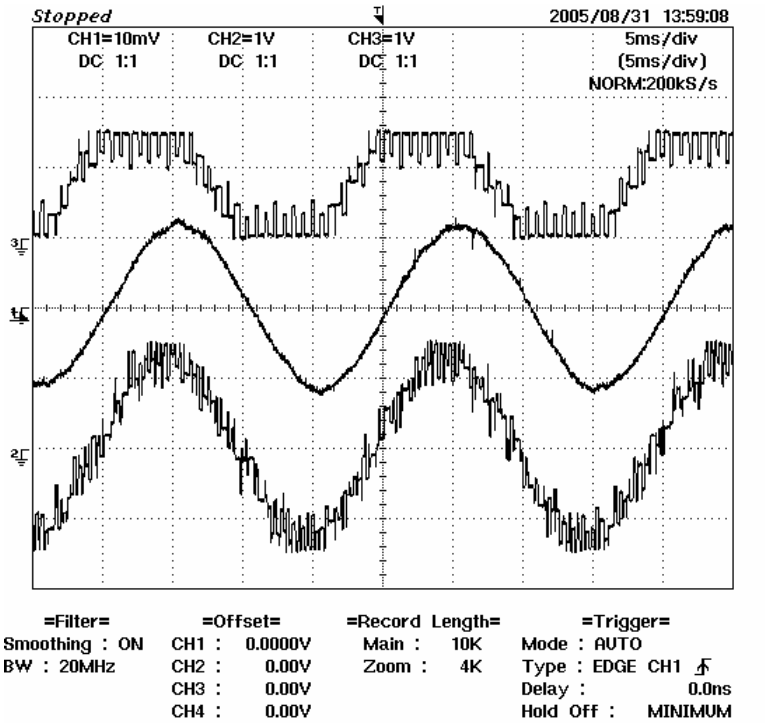


Figure 6.4.15: PD PWM with third harmonic injection waveforms

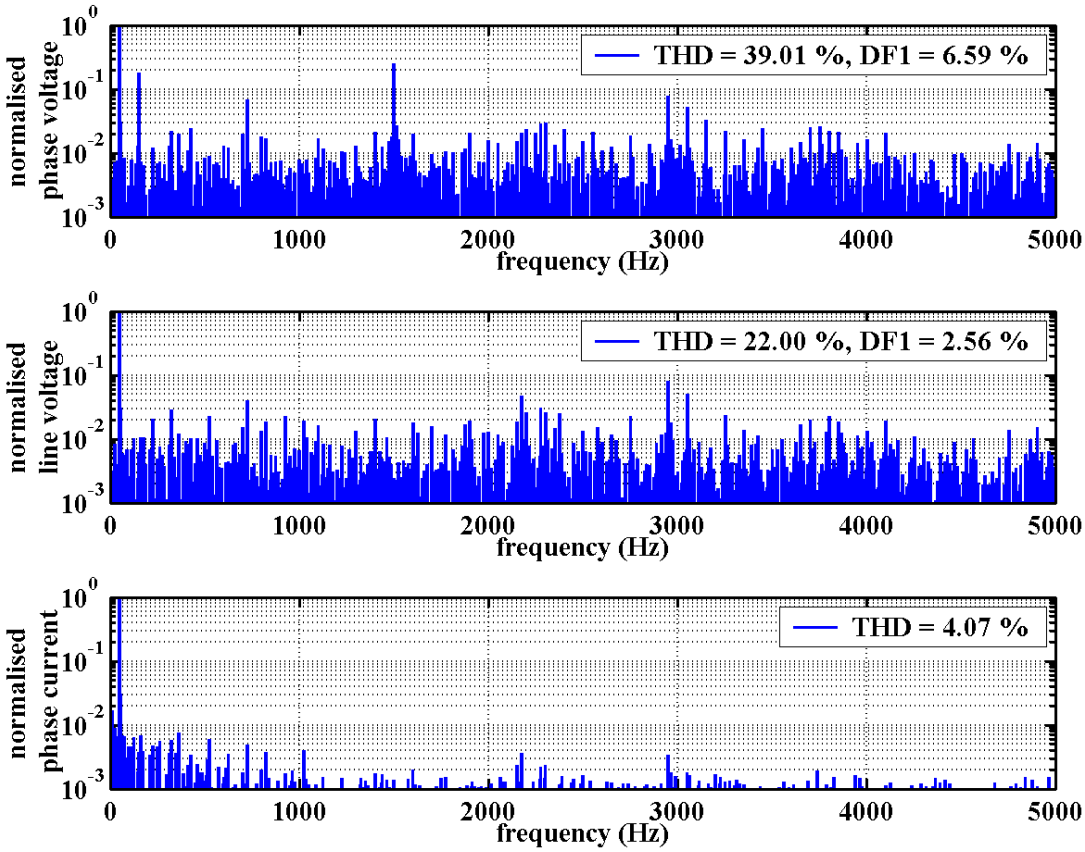


Figure 6.4.16: PD with 1/6th third harmonic injection spectra

6.4.6 Space Vector PWM

The SVPWM, the alternatively method for generating the firing signals in the inverter gives a similar performance to third harmonic injected PD PWM. The experimental inverter waveforms are shown in the Figure 6.4.17 oscillogram. The harmonic spectra for these waveforms are shown in Figure 6.4.18. As can be seen, the waveforms and spectral signatures are very similar to the third harmonic injected case above. The space vector commutation method firing signal generation is akin to a PD PWM scheme, although with different sampling and reference signals. This is the reason why there is a significant peak at the switching frequency in the phase voltage spectrum which is cancelled in the three-phase line voltage spectrum. Therefore, the line voltage THD is comparable to the PD PWM case.

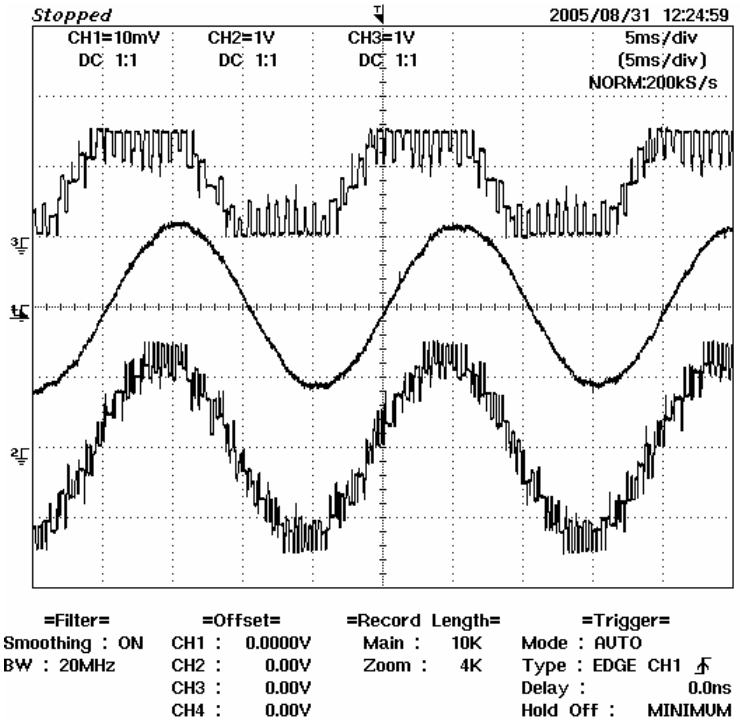


Figure 6.4.17: Space vector PWM waveforms

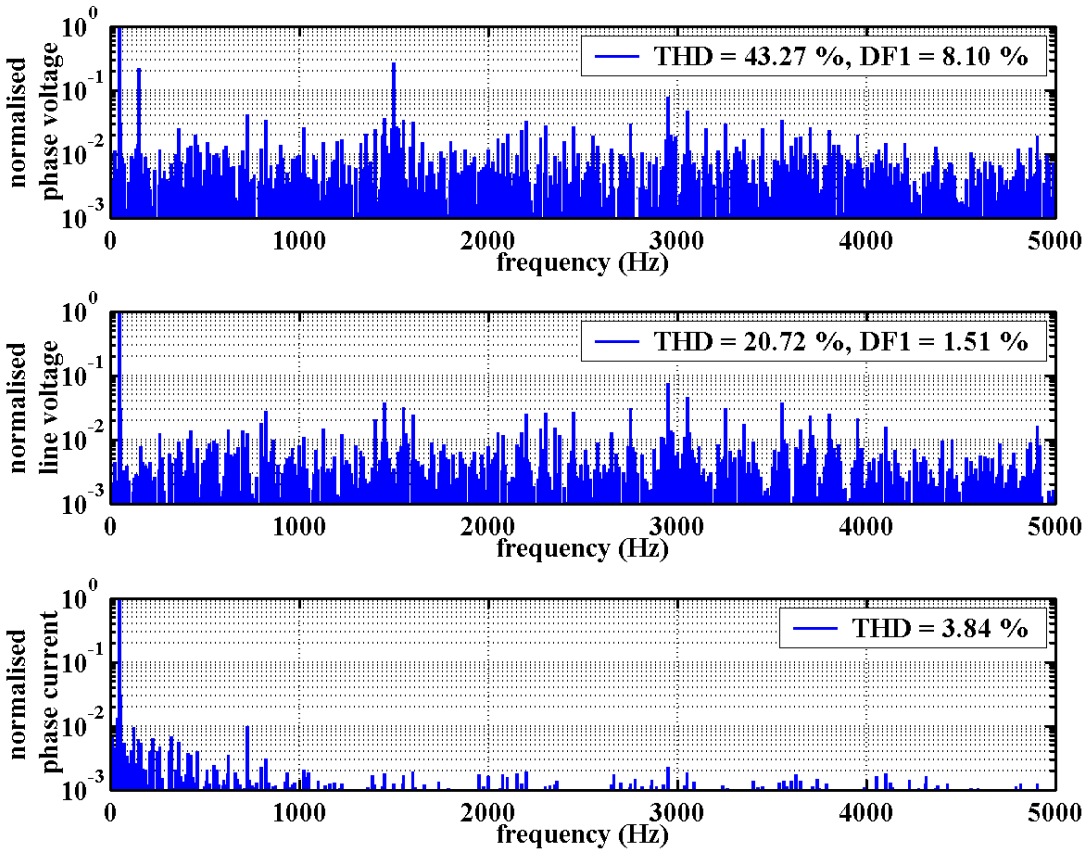


Figure 6.4.18: Space vector PWM spectra

6.4.7 Performance Comparison of Different PWM Schemes

Besides the PD, POD and APOD carrier placement schemes, there are other alternatives which can be used to control the four-cell flying-capacitor inverter. Table 6.4.3 lists the measured harmonic distortion levels for all the different carrier placement schemes investigated. In terms of measured harmonic distortion in the phase current, there is very little difference between the schemes, apart from the DPS implementation. This shows increased harmonic distortion especially at lower frequencies because of the influence of cell-capacitor voltage ripple. Overall the results are in line with predicted distortion levels for the different carrier placement PWM and space vector PWM implementations.

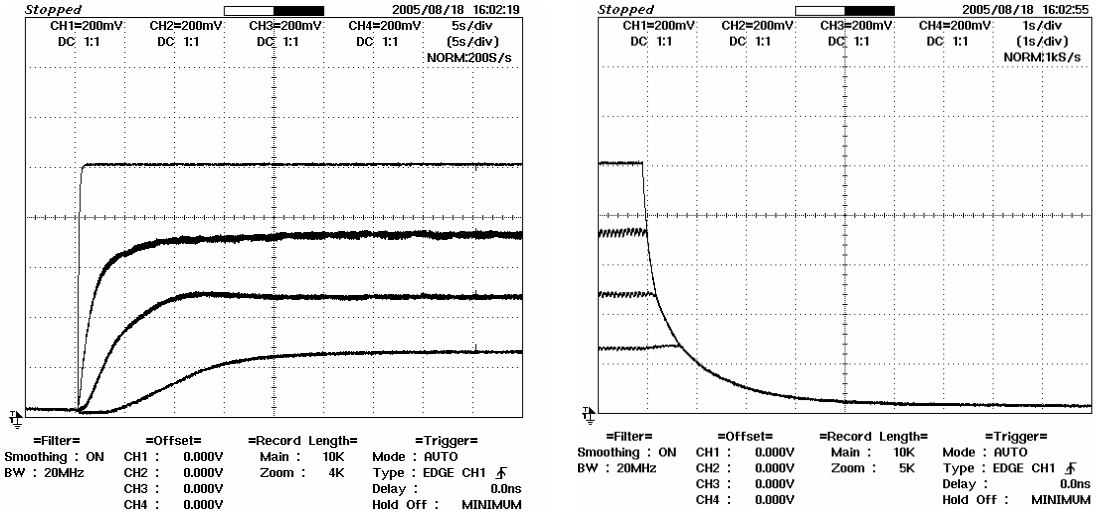
Carrier Scheme	Phase Voltage THD (%)	Line Voltage THD (%)	Line Voltage DF1 (%)	Phase Current THD (%)
PD	28.84	20.31	1.89	3.81
PD + 3rd	39.01	22.00	2.56	4.07
POD	29.35	23.51	4.62	3.68
APOD	31.69	32.70	3.52	4.12
HPS/PS	33.54	31.71	4.15	5.23
SPD	31.24	28.51	3.77	4.77
SPOD	30.80	28.73	3.27	4.22
DPS	33.21	28.89	8.17	5.09
SVPWM	43.27	20.72	1.51	3.84

Table 6.4.3: Measured harmonic distortion factors for various carrier schemes

6.4.8 Input Voltage Transient Behaviour

Figures 6.4.19 show the transient charging and discharging behaviour of the cell-capacitors when a 200 V dc voltage supply is applied and removed. In waveform shape terms, the behaviour is very similar to the case of balanced SHE control presented earlier. However, the transient occurs over a much longer timeframe since it is inversely dependent on the PWM switching frequency.

These plots aim to illustrate the effective long time-constants associated with the cell-capacitors in the system. This means that load transients will not severally affect the system performance and will not lead to significant transient capacitor voltage imbalance. In a practical system, the component selection will be based on cost and safe-operation under steady-state conditions, with the maximum cell-voltage difference taken into account. Therefore, the power switches will not be rated to withstand the full dc link, and so another mechanism for attaining there required voltage levels is needed at start-up in a real system.



a) **voltage charging (5s/div)** b) **voltage decay (1s/div)**

Figure 6.4.19: Cell-capacitor transient characteristic

6.5 Conclusions

A practical four-cell, three-phase flying-capacitor inverter has been built, and tested under laboratory conditions. Overall the measurement results show good correlation with the predicted performance under a variety of different operating control schemes.

It has been demonstrated that optimising the balancing switching pattern when using low frequency SHE control can improve the performance of the inverter in terms of a reduction in some of the low frequency harmonic components. This method has potential where specific harmonics cause problems in the load system, such as resonance due to torque ripple in a motor drive. It is also a way of utilising smaller, lower cost capacitors without compromising performance. The results also highlight the issue of sub- and inter-harmonic generation due to cell-capacitor ripple voltage when operating with the pattern-based balancing strategy. In a practical system, there is a compromise between capacitor size and output power quality and so care would need to be taken in assessing the risk of very low frequency harmonics on load performance.

Well balanced operation of inverter has been achieved with a sub-carrier firing rotation hardware block implemented successfully in the Xilinx FPGA. This works for all forms of high frequency PWM control. The practical results do however highlight short comings in the prototype design, and confirm the predicted sensitivity of the gate-drive signal timings in achieving a well balanced system.

The output power quality of the load waveforms is dependent on the form of carrier placement used for a sine-triangle PWM implementation. It has been shown that the phase disposed (PD) carrier method results in lower line voltage harmonic distortion compared to other proposed schemes. This result shows that the effect of the capacitor voltage ripple does not cause a significant deterioration in the performance of the PD PWM scheme compared to the ideal case. It has also been shown that the addition of a third harmonic component in the reference waveform does not adversely affect the performance of the inverter.

Space vector PWM control also gives good performance and the line voltage THD is as low as the sine-triangle PD PWM scheme. The results also show that space vector PWM is related to the injected third-order harmonic sine-triangle PWM schemes.

6.6 References

[6.1] Lovatt, H.C., McClelland, M.L. and Turner, M.J., "Design of a 3-phase, MOSFET inverter and associated gate-drive circuit", Proceedings of EPE '89, 3rd European Conference on Power Electronics and Applications, 9 - 12 October, 1989, Vol. 1, pp. 165 – 169.

[6.2] Ashenden, P.J., "The designer's guide to VHDL", Morgan Kaufmann Publishers, USA, 2nd Edition, 2002, ISBN 1-55860-674-2.

[6.3] Berto, S., Paccagnella, A., Ceschia, M., Bolognani S. and Zigliotto, M., "Potentials and pitfalls of FPGA application in inverter drives – a case study", Proceedings of ICIT 2003, IEEE International Conference on Industrial Technology, 10 -13 December, 2003, pp. 500 – 505.

[6.4] Tzou, Y.-Y. and Hsu, H.-J., "FPGA realization of space-vector PWM control IC for three-phase PWM inverters", IEEE Transactions on Power Electronics, Vol. 12, No. 6, November 1997, pp. 953 – 963.

Chapter 7 CONCLUSIONS

7.1 Achievements

This thesis has reported a comprehensive investigation into the various forms of modulation control applicable to the flying-capacitor multilevel converter, specifically in relation to the synthesis of sinusoidal output voltages with low harmonic distortion when the topology is employed as an inverter. In this context, the issues of system balancing and the effect of the circuit parameters on performance have been addressed. The major achievements and contributions of this work are summarised as follows:

- A detailed understanding of the cell-capacitor voltage balancing requirements has been demonstrated. It has been shown by using basic circuit analysis that a self-balancing mechanism is inherent to the topology when the averaged duty cycles of each cell switch pair are the same for a given output voltage level.
- A comprehensive simulator program has been developed which includes accurate models of the different components and of the digital control implementation. This has allowed a thorough investigation of sinusoidal modulation and aided the design of an experimental inverter.
- Selective harmonic elimination control has been investigated, specifically in the staircase voltage case. A switching pattern balancing scheme has been developed which ensures that the mean cell-capacitor voltages are at the correct operating levels. The scheme works well in the steady-state and it has been shown that load transient events do not upset the balancing.
- The issue of sub- and inter-harmonic generation has been addressed for the first time in a flying-capacitor inverter with practical sized cell-capacitors. It has been shown that there is a relationship between the capacitor ripple voltage and cycle by cycle balancing strategy and harmonic distortion. It has also been demonstrated that selecting the optimal balancing pattern can improve performance by reducing the harmonics.
- The relationship between the stored energy in the cell-capacitors and the load characteristic has been investigated and a set of normalised curves produced which identify the effect of the cell-capacitance on maximum semiconductor switch blocking voltage and output voltage THD under staircase control.

- The different forms of sine-triangle PWM implementation have been investigated and their relative merits assessed. Practical implementation issues such as reference sampling, digital logic clock frequency and dead-time have all been covered in the analysis.
- A novel balancing scheme has been developed based on a sub-carrier gate-firing rotation which is applicable to all forms of fixed frequency PWM, and which is simple to implement in digital hardware. It has been shown that the digital logic timings are critical for balanced operation and a novel method for ensuring that the timing errors are minimised has been proposed.
- The normalised inverter system operating characteristics have been mapped as functions of the energy stored per unit cell capacitor and the load power factor. It is has been shown that the characteristic energy factor curve has the same form as SHE control and the relationship between switching frequency and maximum safe-operating output power quantified.
- Space vector PWM has been investigated in the context of a multilevel inverter and a simple algorithm has been developed to minimise the computational requirements. It has been shown that the output voltage harmonic distortion level is on a par with the third harmonic injected sine-triangle PWM scheme, and that these two modulation methods are in essence the same.
- An experimental four-cell, three-phase inverter has been constructed and the measured harmonic performance has been assessed. All forms of modulation control have been implemented and there is excellent correlation between the measured system operating parameters and the simulated performance.

7.2 Recommendations for Future Work

There are areas where the practical design of the flying-capacitor inverter can be improved. Firstly, the VCOX approach to optimising the timing of the digital control implementation needs to be validated in practice. Secondly, reductions in the timing delays associated with the interface circuitry between the digital controller and the gate-drivers are required to improve performance especially at higher switching frequency. Finally, it is envisaged that an improved gate drive circuit can be developed which includes a drain-source voltage monitor for detecting over-voltage conditions, and which can be part of a sensed cell-capacitor voltage balancing system.

Although the work presented has addressed all forms of sinusoidal voltage synthesis, and demonstrated practical implementations, there remains one area where a more

thorough understanding is required. The large number of switching states and the necessity for rotating these switching states to achieve cell-capacitor voltage balancing has the potential to introduce unstable or chaotic behaviour. This is an important area of interest especially concerning inverter operation with a stable closed-loop voltage controller.

The flying-capacitor multilevel inverter system can be used in a variety of different high power applications which are only recently becoming practical with modern electronic components. Motor drives are an important application for the inverter, and one specific area where a contribution could be made is in the effect on machine operating performance of harmonics present in the output voltage when operating under staircase control with the pattern-based balancing strategy employed.

Another possible area of research, where a significant contribution can be made, is in the use of the asymmetric bridge form of the flying-capacitor multilevel topology as the power converter stage in a switched reluctance motor drive. The availability of more than one voltage level has the potential to improve the operating performance of these machines over a much wider speed range than is possible using existing two-level power converters. Torque ripple could be reduced by exploiting the extra voltage control modes in profiling the chopped phase current at reduced switching frequency and therefore higher efficiency. Alternatively, the higher efficiency single-pulse voltage control mode can be extended down to lower speeds by reducing the phase operating voltage. The two most likely applications to benefit from this approach are traction where smoother torque is preferred and renewable energy systems, such as wind turbines, where generation would be possible at lower wind speeds than at present. This has the potential for reducing the size of the gearbox or even eliminating it.

The most exciting possibilities for future research on flying-capacitor inverter applications are in the area of power conditioning systems, such as reactive power controllers, active harmonic filters and unified power flow controllers. The necessity for a large number of capacitors in this type of multilevel inverter may well be less of an impediment, especially if the system control is optimised to make use of the available the stored energy. There is also potential in adjusting the internal cell-capacitor voltage variations in a favourable manner in terms of the resultant harmonic generation for cancelling unwanted harmonics in the utility supply system.

The simulator developed for analysing the performance of the flying-capacitor inverter and investigating the influence of the control strategy on performance is a useful tool which can aid further research on the inverter. The experimental inverter also provides an excellent laboratory facility for investigating further the practical performance of systems based on the flying-capacitor inverter.

Finally, some elements of this work have already been disseminated to the international community through the publication of six papers at various conferences. The paper bibliographies are listed in Appendix B. It is expected that an additional two journal papers will be published on the material contained in this thesis, and further conference papers may follow.

Appendix A SHE STAIRCASE ANGLE COMPUTATION

A MATLAB script is used to compute the angles, $\alpha_1 - \alpha_4$, required for SHE-4H4 control. The iterative Newton-Raphson method is used to solve the following set of simultaneous equations

$$\cos(\alpha_1)+\cos(\alpha_2)-\cos(\alpha_3)+\cos(\alpha_4)=\frac{\pi m_a}{2} \quad \ldots (3.2.3)$$

$$\cos(5\alpha_1)+\cos(5\alpha_2)-\cos(5\alpha_3)+\cos(5\alpha_4)=0 \quad \ldots (3.2.4)$$

$$\cos(7\alpha_1)+\cos(7\alpha_2)-\cos(7\alpha_3)+\cos(7\alpha_4)=0 \quad \ldots (3.2.5)$$

$$\cos(11\alpha_1)+\cos(11\alpha_2)-\cos(11\alpha_3)+\cos(11\alpha_4)=0 \quad \ldots (3.2.6)$$

The complete listing of the m-file function is as follows:

```
% she.m
% Newton-Raphson solver for four angle SHE control
% ma is the modulation amplitude
% xn is the number of inverter cells
% bn is b coefficient index vector
% bvalue is b coefficient value array
% function returns first 21 b coefficients
% 4 angle search

function vector=she(ma)
xn=4;
bn=[1 5 7 11];
bvalue=[1 0 0 0];
n=10;               % first 20 coefficients
nTrial=20;          % number of trials

for i=1:xn
    bnvalue(i)=2*ma*bvalue(i);     % scale bn target values
end

% initial seed values to aid convergence
alpha=[0.35 1.1 1.5 1.35];

for T=1:nTrial
```

```
    for i=1:n
        index=2*i-1;
        % set even number b coefficient to zero
        b(index+1)=0.0;
        % sum components
        b(index)=cos(index*alpha(1))
        b(index)=b(index)+cos(index*alpha(2));
        b(index)=b(index)+cos(index*alpha(3));
        b(index)=b(index)-cos(index*alpha(4));
        % scale
        b(index) = b(index)*4/(index*pi);
    end

    % matrix of partial derivatives A(alpha) and negative of
    % function B(alpha)
    for j=1:xn
        B(j)=-b(bn(j)) + bnvalue(j);
        A(j,1)=-4/pi*(sin(bn(j)*alpha(1)));
        A(j,2)=-4/pi*(sin(bn(j)*alpha(2)));
        A(j,3)=-4/pi*(sin(bn(j)*alpha(3)));
        A(j,4)=4/pi*(sin(bn(j)*alpha(3)));
    end

    deltaAlpha=A\B';           % uses LU decomposition
    for j=1:xn
    alpha(j) =alpha(j)+deltaAlpha(j);
    end
end

vector=alpha; % return complete set of firing angles
```

Appendix B PUBLISHED PAPER BIBLIOGRAPHY

[B.1] **Title:** Modelling and control of a flying-capacitor inverter

Authors: Watkins, S.J., and Zhang, L.

Source: Proceedings of EPE '01, 9th European Conference on Power Electronics and Applications, Graz, Austria, 27 - 29 August, 2001, CDROM Paper No. PP00439.

Abstract: This paper presents the results of an investigation into the variation in the output voltage quality of a flying-capacitor inverter under staircase angle control. The trade-offs between capacitor size, power device voltage rating and output voltage quality are assessed through simulation. A general mathematical model for an N-level inverter is used for circuit operation analysis and its results are compared with those from a Simulink® circuit simulation. The computer model allows a thorough investigation of all possible switching pattern permutations that produce the desired sinusoidal output and maintain steady state capacitor voltage balancing. Results show that the total harmonic distortion in a sinusoidal synthesised output can be minimised by the correct selection of the switching mode sequence.

[B.2] **Title:** Influence of multilevel sinusoidal PWM schemes on the performance of a flying-capacitor inverter

Authors: Watkins, S.J. and Zhang, L.

Source: Proceedings of PEMD '02, the 1st International Conference on Power Electronics Machines and Drives (IEE Conference Publication No. 487), Bath, UK, 16 - 18 April, 2002, pp 92 - 97.

Abstract: Multilevel inverters, including the flying-capacitor topology require more complex control due to the additional flexibility offered by the multiple output voltage levels. One such control method is based on the conventional sinusoidal pulse width modulation (SPWM) scheme and uses multiple triangular carriers. There are a number of SPWM variants that achieve the desired inverter control. This paper presents the results of an investigation into these different schemes and their influence on the power quality and efficiency of a flying-capacitor inverter.

[B.3] **Title:** Multilevel asymmetric power converters for switched reluctance machines

Authors: Watkins, S.J., Čorda, J. and Zhang, L.

Source: Proceedings of PEMD '02, the 1st International Conference on Power Electronics Machines and Drives (IEE Conference Publication No. 487), Bath, UK, 16 - 18 April, 2002, pp 195 - 200.

Abstract: This paper presents a new family of multilevel asymmetric power converters which are suitable for unipolar current loads such as a switched reluctance motor drive. The fundamental operation of each topology is reviewed and some simulation results are presented showing the potential system performance improvements that can be realised by operating with intermediary voltages rather than the full dc-link.

[B.4] **Title:** Analysis and control of a multi-level flying capacitor inverter

Authors: Zhang, L., Watkins, S.J. and Shepherd, W.

Source: Proceedings of CIEP '02, 8th IEEE International Power Electronics Congress, Guadalajara, Mexico, 20 – 24 October, 2002, pp. 66 – 71.

Abstract: The paper presents the results of a study into the optimal switch mode sequence for a multi-level flying capacitor inverter to synthesis a sinewave voltage under staircase angle control. It is shown that a properly selected sequence will yield the voltage and loss balances in capacitor voltages and switching devices respectively and minimize the load voltage THD values. A general mathematical model for an N-level inverter is presented which can be conveniently applied for computer simulation of any operating mode.

[B.5] **Title:** An SR drive for a multi-megawatt high-speed application

Authors: Watkins, S.J. and Čorda, J.

Source: Proceedings of EPE '03, 10th European Conference on Power Electronics and Applications, Toulouse, France, 2 - 4 September, 2003, CD-ROM Paper No. 0071.

Abstract: The paper gives an insight into the main features of an SR drive system from the perspective of a multi-megawatt drive

application where the rated speed is typically above ten thousand rev/min and the operating voltage is in the range of several kV. The power electronic converter is based on a topology, which allows the application of multiple voltage levels to the machine's phase windings, while utilising lower voltage, fast switching IGBTs. The system's performance is illustrated by means of computer simulation which includes modelling of the electronics conduction and switching losses together with the copper and iron-loss in the machine.

[B.6] **Title:** Multilevel space vector PWM control schemes for a flying-capacitor inverter

Authors: Watkins, S.J., and Zhang, L.

Source: Proceedings of PEMD '04, the 2nd International Conference on Power Electronics, Machines and Drives (IEE Conference Publication No. 498), Edinburgh, UK, 31 March - 2 April, 2004, Vol. 1, pp. 12 – 17.

Abstract: The paper presents three different computational schemes for achieving space vector pulse width modulation, in the control of a multilevel flying capacitor inverter. Each scheme uses the same method of achieving cell-capacitor voltage balancing. Results of realistic simulations are used to compare and contrast these approaches. The timing control of the inverter switches and output performance of each method are presented and the most suitable one is highlighted.