Study Of Silicon Carbide (SiC) Power Devices Using TCAD Simulation And Experimental Techniques

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Abstract

This thesis presents a comprehensive study of Silicon Carbide (SiC) power electronics, detailing its development and various polytypes, including 4H, 6H, and 3C. It explores the superior physical properties of SiC, such as a wide bandgap, high thermal conductivity, and strong electric field strength, which enable devices to operate at higher temperatures, voltages, and frequencies compared to silicon. Challenges like leakage current and threshold voltage drift are discussed in relation to the reliability and efficiency of SiC devices. The study also highlights applications in electric vehicles, renewable energy systems, and industrial power supplies.

A major focus is SiC MOSFETs, including their operational principles and equivalent circuits. The thesis examines device breakdown mechanisms such as avalanche breakdown and classifies MOSFET types based on structure, operation, and application-specific advantages.

The role of Technology Computer-Aided Design (TCAD) simulations in semiconductor modelling is emphasized. Foundational semiconductor equations, such as Poisson's and Continuity equations, are introduced, along with the Sentaurus TCAD tool. The study discusses meshing techniques essential for accurate simulations and presents detailed flowcharts for modelling SiC JFET devices. Key simulation results are analysed, identifying performance metrics and potential improvements.

The fabrication of SiC MOS devices involves SiC wafer selection, cleaning, and cutting, followed by deposition techniques like Atomic Layer Deposition (ALD) and Magnetron Sputtering. The research proposes a novel dual dielectric stack approach, integrating materials such as BN and TiO_2 to enhance gate dielectric performance. The effects of deposition methods and annealing parameters on dielectric quality are evaluated to improve reliability and efficiency.

MOS capacitor characterization techniques, including SEM, TEM, XRD, and Raman Spectroscopy for surface analysis, as well as CV and IV measurements for electrical properties, are explored. The study identifies optimal dielectric stack configurations for minimizing leakage current, maximizing breakdown voltage, and stabilizing capacitance, providing valuable insights into advanced MOS device development.

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Declaration

I hereby declare that the research presented in this thesis is entirely my own work, except where otherwise indicated. This work has not been previously submitted for any degree or qualification at this or any other university. All sources of information have been duly acknowledged.

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Acronyms and Symbols

Acronyms

AC Alternating Current

BJT Bipolar Junction Transistor

BPD Basal Plane Dislocation

CVD Chemical Vapour Deposition

DC Direct Current

DIMOSFET Double Implanted MOSFET

DMOS Double Diffused Metal Oxide Semiconductor

EV Electric Vehicle

HTCVD High-Temperature CVD

IC Integrated Circuit

IGBT Insulated Gate Bipolar Transistor

I-V Current-Voltage

JFET Junction Field-Effect Transistor

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

DUT Device Under Test

EMI Electromagnetic Interference

EV Electric Vehicle

GaN Gallium Nitride

IGBT Insulated Gate Bipolar Transistor

SiC Silicon Carbide

Si Silicon

WBG Wide Bandgap

CAGR Compound Annual Growth Rate

Symbols

C_{DS} drain-source capacitance

C_{GD} gate-drain capacitance

C_{GS} gate-source capacitance

C_{iss} input capacitance

C_{oss} output capacitance

C_{rss} reverse transfer capacitance

di/dt current rate-of-change

dv/dt voltage rate-of-change

E_{off} the turn-off loss of SiC MOSFET

E_{on} the turn-on loss of SiC MOSFET

I_G	gate current
I_L	load current
I_{DS}	drain-source current
K_p	transconductance coefficient of datasheet-based model
Λ	coefficient of short-channel effect of the datasheet-based model
R_G	gate resistor
R_{CH}	channel resistance
R_{DRIFT}	the resistance of the drift region
R_{JFET}	the resistance of the JFET region
R_{on}	On resistance
R_{SUB}	the resistance of the substrate
T_j	junction temperature
T_{off}	the turn-off time of SiC MOSFET
t_{on}	the turn-on time of SiC MOSFET
V_{DG}	drain-gate voltage
V_{DS}	drain-source voltage
V_{GP}	gate plateau voltage
V_{th}	threshold voltage
V_{GS}	drain-source voltage

1. Introduction and Motivation

1.1. Background to Silicon Carbide (SiC) power Electronics

As silicon power semiconductor devices approach their performance limits, the power electronics industry is focusing on improving towards more efficient (lower losses), higher-temperature and high-performance devices in general. For high-temperature and high-power devices, Silicon Carbide (SiC) stands out as the leading contender among wide bandgap semiconductors for several compelling reasons: High quality (low defect) **large substrate availability**: High quality SiC wafers up to 6 inches in diameter are commercially available, facilitating the production of cost-effective devices and 8-inch wafers becoming available in the near future. **Homoepitaxial growth**: SiC can be homoepitaxially grown, which means it can be grown on a SiC wafer. This avoids issues related to lattice mismatch that can occur with heteroepitaxial growth, leading to higher quality and more reliable devices. **Versatile Doping**: SiC can be doped during crystal growth or through ion implantation to achieve both n-type and p-type conductivity. This versatility allows for the creation of a wide range of electronic devices silicon [1]. **Oxide Film Growth**: Oxide films can be thermally grown both on the silicon (Si) and carbon (C) faces of SiC This capability of growing insulating layers is crucial for creating gate channels, in electronic devices [2].

Moreover, SiC is unique among compound semiconductors because it shares its native oxide, silicon dioxide (SiO_2), with silicon (Si). As mentioned, this characteristic allows SiC to be used in the fabrication of standard MOS (Metal-Oxide-Semiconductor) device structures, leveraging the extensive knowledge and experience accumulated by the silicon industry over many decades [3]. This compatibility not only simplifies the manufacturing process but also enhances the performance and reliability of SiC-based devices in high-temperature and high-power applications, despite some outstanding challenges [4, 5] .

The above radar chart compares the properties of materials used in electronics, such as Silicon (Si), Gallium Nitride (GaN), and Silicon Carbide (SiC). One of the key advantages of Silicon Carbide (SiC) is its higher thermal conductivity, which makes it easier to cool components, such as those used in engine control systems. This is crucial for maintaining performance and reliability in high-power applications. Furthermore, the higher system voltage capability of SiC reduces the resistance loss in wiring. This is particularly beneficial for SiC, where industrial components are now available for voltages up to 3.3 kV. Research is ongoing to further expand these voltage capabilities, which could lead to even more efficient power systems.

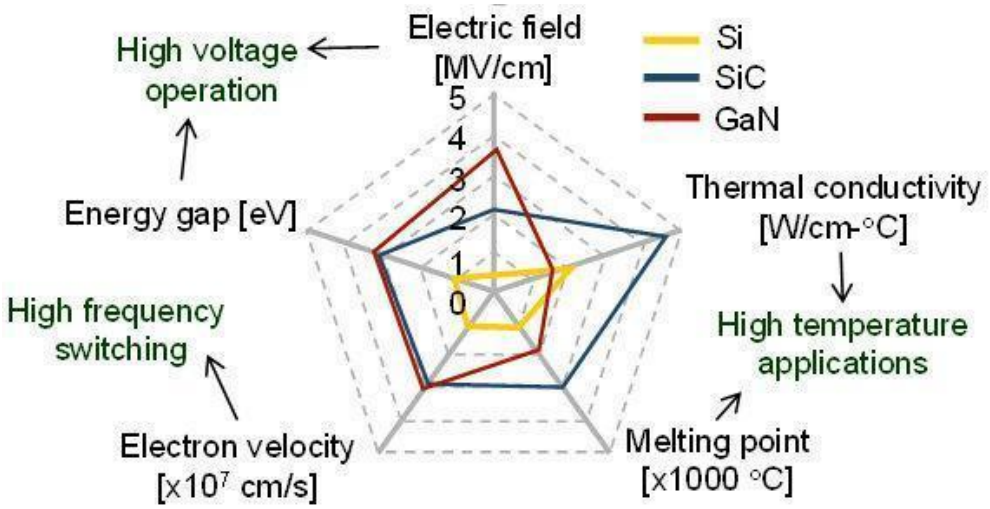


Figure 1.1 Matching the material properties of Si, SiC, and GaN [5]

SiC also demonstrates superior reliability at high temperatures. For example, SiC components have been proven to operate at temperatures as high as +200°C[6–8]. This makes them ideal for applications that require stable performance under extreme conditions. In terms of electrical performance, SiC exhibits low conduction and switching losses. The higher bandgap of SiC results in a smaller drift region for a given rated voltage, which improves conduction losses. Furthermore, the lower parasitic capacitance of SiC reduces switching losses and allows for faster switching rates. This is particularly advantageous in high-frequency applications. The lower parasitic capacitance of SiC also increases the operating frequency. For instance, a 1-5 kV SiC MOSFET can switch at frequencies of hundreds of kHz, compared to tens of kHz for silicon in the same topology. This higher switching frequency can significantly reduce the size of magnetic components, leading to more compact and efficient designs.

The landscape of power electronics has been undergoing a significant transformation driven by the search for higher energy efficiency (lower losses), improved power density, whilst maintaining or improving the system reliability. During this evolution, Silicon Carbide Power Metal-Oxide-Semiconductor Field-Effect Transistors (SiC Power MOSFETs) have emerged as a groundbreaking technology to improve power electronic systems [[1, 9]. With unique material properties and outstanding device performance characteristics, SiC MOSFETs stand as a key enabler in the journey towards a more energy-efficient and sustainable future [10, 11].

Conventional power electronics devices, primarily based on silicon technology, have played a crucial role in power electronics across numerous applications for decades. However, the inherent limitations of silicon devices, such as relatively higher on-resistance, limited

switching speed, and susceptibility to elevated temperatures, have compelled researchers and engineers to investigate alternative solutions. This research for innovation has led to the development of wide-bandgap materials, with silicon carbide at the forefront. SiC's outstanding characteristics, including its wide bandgap, high critical electric field, high thermal conductivity and high saturation electron velocity position it as a superior material to silicon for the development of next generation power electronic systems [3, 12, 13]. Subsequently SiC MOSFETs, as a part of SiC-based devices, exhibit unparalleled improvements over their silicon power device counterparts. These improvements include ultra-fast switching speeds, reduced switching losses, enhanced thermal performance, and improved breakdown voltage capabilities [14]. SiC MOSFETs have rapidly gained popularity in a variety of applications requiring high-frequency operation, high power densities, and stringent thermal management requirements[15].

SiC MOSFETs have the potential to have a significant impact on a variety of sectors, including aerospace, industrial automation, renewable energy systems, electric cars, and plenty more [16]. The ability to efficiently convert and control electrical energy with minimum losses not only translates to improved operational efficiency but also contributes to reduced carbon emissions and enhanced sustainability. In this comprehensive review, we delve into the advances and challenges associated with SiC MOSFET technology [16–18]. By examining the historical context, fundamental principles, recent advancements, and ongoing obstacles, we aim to provide a holistic understanding of the transformative potential of SiC MOSFETs in modern power electronics. This review also contemplates the implications of SiC MOSFETs on emerging applications, envisions future trends, and underscores the importance of addressing the existing challenges to fully unlock the revolutionary promise of this technology [19].

1.2.Polytypes associated with SiC

In 1905, Ferdinand Frederick Henri Moissan, a renowned French chemist, discovered naturally occurring silicon carbide in the Canyon Diablo meteorite from the Barringer meteorite crater in the Arizona desert. Moissan dissolved a 56 kg piece of the meteorite in strong acids, extracting a few tiny crystals identified as silicon carbide. Since then, this mineral has been found in numerous other meteorite samples and impact craters. It was initially believed that the heat generated by the friction between the meteorite and Earth’s atmosphere provided the necessary temperature to form silicon carbide from the raw materials within the meteorite. Some also suggested that the silica (quartz) could come from the material displaced during the

meteorite's impact with Earth's crust. However, there was some debate, as the silicon carbide could have been contaminated from carborundum tools, which were already widely used at the time.

Today, the extraterrestrial origin of this silicon carbide is confirmed by its carbon isotopic composition. The ratio of the 12C isotope to the 13C isotope is about 64, significantly lower than the 12C/13C ratio in terrestrial materials. The prevailing theory now is that interstellar silicon carbide was synthesised in the expanding atmospheres of pre-solar carbon stars [20].

In silicon carbide (SiC), both silicon (Si) and carbon (C) atoms have their four valence electron orbitals sp^3 hybridised, forming very strong Si-C bonds with a dissociation energy of 3.1 eV. These bonds are primarily covalent, as the binding electrons are shared between the two atoms. However, due to carbon's higher electronegativity (2.55 eV for C compared to 1.9 eV for Si), the electron density is greater around the carbon atoms, giving the Si-C bonds a partially ionic character. For a detailed definition and quantitative description of the ionicity of Si-C bonds, refer to specialised literature. Silicon carbide is a compound material that exhibits polymorphism, meaning it can exist in different structures called polytypes. More than 250 polytypes of SiC have been identified, with some of them having a lattice constant as long as 301.5 nm, about one thousand times the usual SiC lattice spacing.

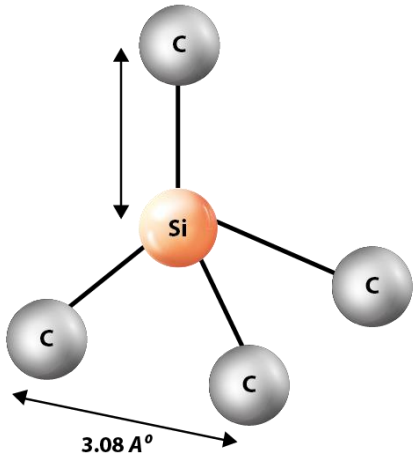


Figure 1.2 The tetrahedron building block of SiC Crystal

Silicon carbide shows a two-dimensional polymorphism called polytypes, which is one of its most significant features. Each polytype has different material properties, such as bandgap, electron mobility, and thermal conductivity, that affect its performance in power devices [16, 18, 21]. Fig 1.2 shows a tetrahedron of four carbon atoms attached to the central silicon atom

representing the basic building block of SiC crystal. Fig 1.3 describes the layer structure of SiC, the tetrahedrally bonded silicon atoms with three carbon atoms within the bilayer and having a single bond to the carbon atom above. The hexagonal frame of Si-C bilayer is the basic building block of formation of polytypes.

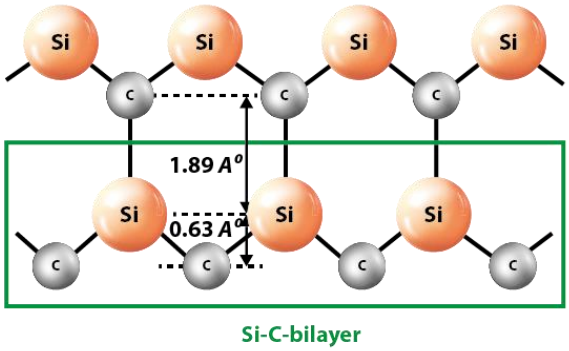


Figure 1.3 Si-C-bilayer

The Ramsdell notation is the most used nomenclature of the SiC In this nomenclature the polytypes name consists of the number followed by a letter. The number indicates the period of the stacking sequence, and the letter indicates the crystal structure which the polytype forms. For a difference sequence the crystal structure may be Cubic, Hexagonal or Rhombohedral which is denoted by C, H and R. The most common polytypes are 3C-SiC, 4H-SiC, 6H-SiC, 15R-SiC, and 2H-SiC. Each polytype has different material properties, such as bandgap, electron mobility, and thermal conductivity, that affect its performance in power devices[22, 23]. Among these polytypes, 4H-SiC is the most widely used in high-power and high-temperature applications, such as SiC MOSFETs. The choice of polytype depends on the specific needs of the application and the quality of the crystals available. 4H-SiC, it is widely used for power devices because of its high breakdown voltage, high thermal conductivity, and high saturation velocity [24, 25].

1.3. Physical Properties of SiC

Silicon carbide (SiC) has a tough crystal structure with strong chemical bonds, giving it excellent mechanical, thermal, chemical, and electrical properties. It is an indirect band gap semiconductor, like silicon and diamond, but with different bond dissociation energies. SiC is very hard, ranking third on the Mohs scale after diamond and boron nitride. It remains solid up to ~2500°C and has a high Debye temperature (~850°C), indicating its high thermal stability.

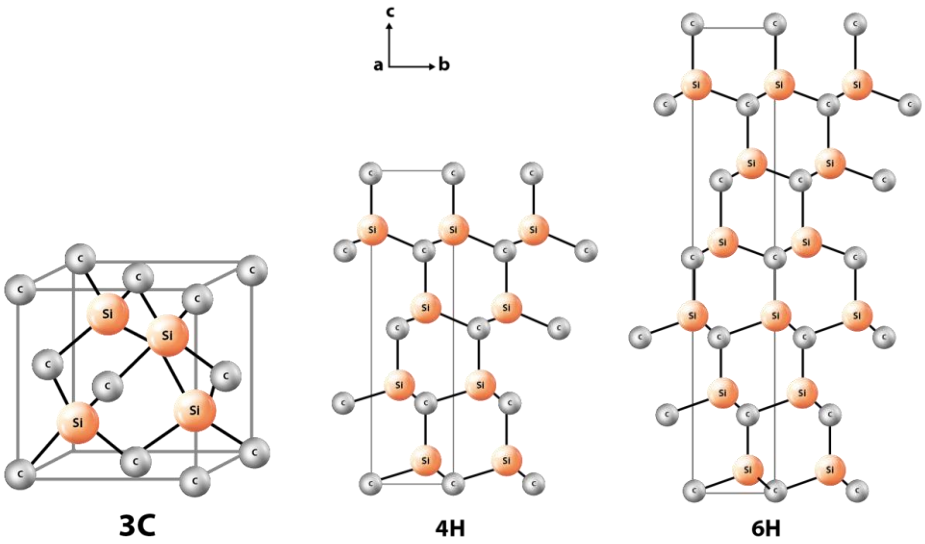


Figure 1.4 Crystal structures of the polytypes of SiC considered in this work

SiC has excellent thermal conductivity, comparable to copper, and is resistant to radiation damage. It is chemically inert at room temperature and can only be etched in molten alkalis above 450°C. Oxidation starts above 900°C, with a slow etching rate in dry oxygen at 1200°C. Despite its low oxidation rate, SiO_2 films can be grown on SiC, which is advantageous over other wide band semiconductors like diamond and III-V nitrides that lack a native oxide.

The table 1.1 provides a comparative overview of key material parameters for Silicon (Si), Silicon Carbide (SiC), and Carbon (C). It reveals a systematic trend in several properties. Bond strength increases from Si to SiC to C, evidenced by higher bond dissociation energies and shorter bond lengths. This trend is mirrored in mechanical properties, with hardness increasing significantly from Si to SiC and reaching a maximum in C (diamond). Thermally, SiC and C exhibit superior properties, with higher thermal conductivity and temperatures. SiC and C also demonstrate higher melting or decomposition temperatures compared to Si. Electrically, the materials exhibit distinct characteristics. Si, with a lower bandgap, is a widely used semiconductor. SiC and C, with their wider bandgaps, are classified as wide-bandgap semiconductors. This wider bandgap leads to lower intrinsic carrier densities in SiC and C, impacting their electrical conductivity. Si generally exhibits higher electron mobility compared to SiC, while C (diamond) is known for its exceptionally high electron mobility. The table also includes information on shallow donor and acceptor activation energies, which are crucial for understanding the behaviour of impurities in these materials.

These material parameters have significant implications for their applications. Si's relatively low bandgap and well-developed processing technology make it the cornerstone of modern

electronics. SiC's high thermal conductivity, wide bandgap, and high breakdown field make it suitable for high-power electronics, high-temperature applications, and harsh environments. C (diamond), with its exceptional hardness, high thermal conductivity, and wide bandgap, holds promise for applications in cutting tools, heat sinks, and high-power electronics, although its high cost and processing challenges currently limit its widespread use.

Table 1.1 physical properties of silicon carbide, silicon and diamond[26]

Material parameter	**Unit**	**Si**	**SiC**	**C**
Bond dissociation energy	eV	2.3	3.1	3.6
Bond length	Nm	0.235	0.185	0.1545
Mohs Hardness		7	9.1 ÷ 9.4	10
Density	g/cm^3	2.33	3.21	3.52
Thermal conductivity at 300 K	W/cm/K	1.3	3.7 ÷ 4.9	20 ÷ 25
Debye temperature	°C	370	850	1600
Melting (decomposition) temperature	°C	1412	~2500 (sublimes)	~3600 (sublimes)
Relative dielectric constant		11.9	10.03	5.7
Band gap energy at 300 K	eV	1.12	3.23	5.47
Intrinsic carrier density at 300 K	cm^{-3}	$8.8 \cdot 10^9$	$1.7 \cdot 10^{-8}$	$\sim 10^{-27}$
Breakdown field at 300 K	V/cm	$(2 \div 4) \cdot 10^5$	$(1.6 \div 3) \cdot 10^6$	$10^6 \div 10^7$
Electron mobility at 300 K	cm^2	1400	900*	>2000
Shallow donor activation energy	meV	43 (Sb)	52 (N)	600 (P)
Shallow acceptor activation energy	meV	45 (B)	190 (Al)	370 (B)
Maximum diameter of native single crystal substrate	Mm	450	200	10
Availability of native oxide		Yes	yes	no

However, 4H-SiC MOSFETs face some challenges, such as high on-resistance, low channel mobility, high interface trap density, and poor oxide quality, that limit their performance and reliability [27, 28]. To overcome these challenges, researchers have developed various techniques to improve the structure and fabrication which will be discussed in this thesis. Other than 4H-SiC MOSFETs, a range of devices have been developed with the aim of reducing the on-resistance and increasing the current density and breakdown voltage of 4H-SiC MOSFETs . These devices include the trench MOSFET, Superjunction MOSFET, double-reSURF MOSFET, and local floating Superjunction MOSFET amongst others.

The table 1.2 compares the properties of three silicon carbide (SiC) polytypes: 3C-SiC, 4H-SiC, and 6H-SiC. These properties include hexagonality, band gap energy, electron affinity, intrinsic carrier density, shallow donor and acceptor activation energies, maximum electron and hole mobilities, and maximum breakdown field, all measured at 300 K. 3C-SiC has no hexagonality, a band gap of 2.36 eV, and an electron affinity of 4.0 eV. It also has a high intrinsic carrier density and moderate activation energies for donors and acceptors. Its electron and hole mobilities are 900 $cm^2/(V \cdot s)$ and 40 $cm^2/(V \cdot s)$, respectively, with a breakdown field of $\sim 1 \cdot 10^6$ V/cm. In contrast, 4H-SiC and 6H-SiC have higher hexagonality, larger band gaps (3.23 eV and 3.08 eV), and lower electron affinities (3.17 eV and 3.45 eV). They exhibit significantly lower intrinsic carrier densities, with 4H-SiC having the lowest. Both have higher electron and hole mobilities compared to 3C-SiC, with 4H-SiC showing the highest values. Their breakdown fields are also higher, at $\sim 3 \cdot 10^6$ V/cm. These differences highlight the suitability of each polytype for specific high-power and high-frequency applications[29, 30].

Table 1.2 important Electrical parameters of different SiC polytypes[31, 32]

Parameter	**Unit**	**3C-SiC**	**4H-SiC**	**6H-SiC**
Hexagonality		0	0.5	0.33
Band gap energy at 300 K	eV	2.36	3.23	3.08
Electron affinity	eV	4.0	3.17	3.45
Intrinsic carrier density at 300 K	cm^{-3}	$1.4 \cdot 10^{-1}$	1.7·10-8	1.8·10-7
Shallow donor (N) activation energy	meV	60-100	52	85-125
Shallow acceptor (Al) activation energy	meV	260	190	239

Maximum electron mobility at 300 K	cm^2 /(V·s)	900	900	360
Maximum hole mobility at 300 K	cm2 /(V·s)	40	120	90
Maximum breakdown field at 300 K	V/cm	~1·106	~3·106	~3·106

1.4. Challenges associated with SiC Power electronics

Despite the benefits of Silicon carbide (SiC) MOSFETs, these devices still face several challenges in the power electronics domain, particularly leakage current, threshold voltage drift, interface defects, issues primarily related to the gate. SiC devices often experience higher leakage currents in the SiC MOS region compared to silicon devices due to the larger band gap of SiC, which enhances tunnelling currents through the gate oxide, and the higher electric fields in blocking states. The stability of the threshold voltage V_{th} in SiC MOSFETs is also a significant concern, as Bias Temperature Instability (BTI) can cause a gradual drift in V_{th}, impacting performance over time. This drift is influenced by the quality of the gate oxide and the presence of interface traps[33, 34]

Electrically active defects at and near the interface between SiC and the gate dielectric significantly affect performance and reliability, as these defects can trap charge carriers, reducing channel-carrier mobility and causing variations in the threshold voltage. The gate oxide in SiC devices must withstand higher electric fields and temperatures compared to silicon devices, with Time-Dependent Dielectric Breakdown (TDDB) being a critical reliability issue. Prolonged exposure to high electric fields can lead to fatal device failure, making the quality of the gate oxide and its interface with SiC crucial for long-term reliability.

This research project focuses on overcoming challenges in silicon carbide (SiC) metal-oxide-semiconductor (MOS) channels by investigating a range of dielectric materials and deposition techniques[35–37].

Fabrication:

- Fabricate SiC MOS channels with three different polytypes (4H, 3C, and 6H) using various dielectric materials (SiO2, AlOx, TiO2, and BN).
- Investigate the performance of MOS channels with stacked dielectric layers (e.g., BN and AlOx, AlOx and SiO2).

- Employ both ALD (Atomic Layer Deposition) and sputtering deposition techniques for fabricating the MOS channels.

Characterization:

- Utilize surface characterization techniques such as Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM), X-ray Diffraction (XRD), Raman Spectroscopy, and Atomic Force Microscopy (AFM) to analyse the physical and chemical properties of the fabricated MOS capacitor surfaces.
- Employ electrical characterization techniques, including Capacitance-Voltage (CV), Current-Voltage (IV), and other relevant measurements, to assess the electrical performance of the fabricated devices.

Simulation:

- Simulate SiC JFETs using Sentaurus TCAD to understand their device characteristics.

Analysis:

- Analyse existing SiC MOSFET devices (Time constraints limited full analysis, but the setup for analysis was completed).

1.4.1. Near Interface trap

The electrical performance of metal oxide semiconductor (MOS) devices is significantly impacted by the physical and electrical properties of the gate dielectric layer and the semiconductor-oxide interface. When the semiconductor substrate undergoes oxidation, it leads to the formation of electrically active defects due to the irregularities in the crystal lattice at the semiconductor's surface. These defects are primarily located at or near the semiconductor-oxide interface [38–40].

Given their proximity to the free carriers in the semiconductor, these defects can trap and release mobile holes and electrons. Defects that trap and release carriers through thermal emission are known as interface traps, while those that do so via tunnelling are referred to as near-interface traps. A high density of these traps can negatively affect the operation of MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors). This includes inefficient modulation of the inversion channel due to interface trapped charge and a reduction in effective field-effect mobility in the inversion channel due to the trapping of mobile charge carriers [41–43].

Therefore, methods to quantify the interface trap density and the energy position of these electrically active defects are crucial for developing high-quality semiconductor-oxide interfaces, which are essential for practical applications of MOS structures. Existing MOS-based characterization techniques, originally developed for Si-SiO_2 interfaces, are primarily used for this purpose. In silicon devices, the most significant traps are interface traps located energetically in the band gap, below the conduction band edge[44].

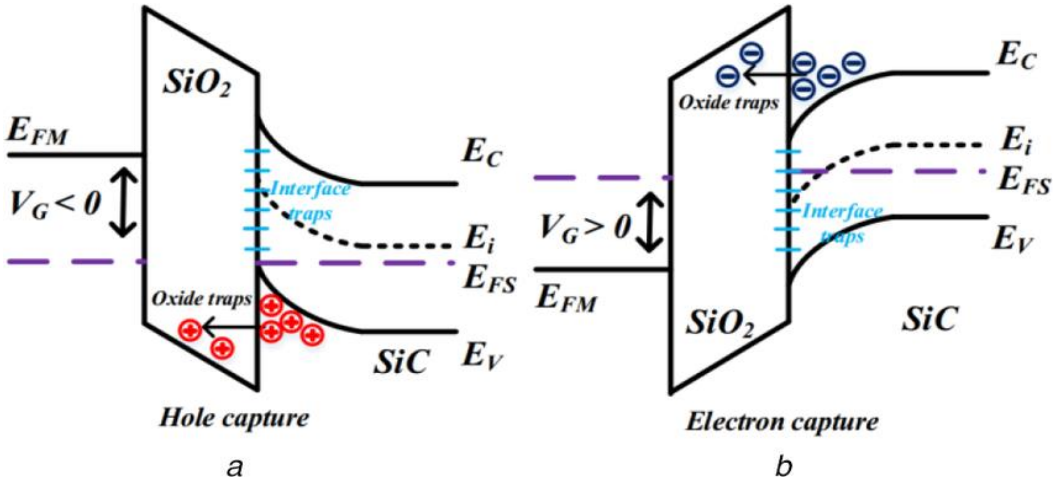


Figure 1.5 band diagram of SiC/SiO_2 structure (a) Holes trapping under negative gate bias stress, (b) Electrons trapping under positive gate bias stress[44].

The figure 1.5 illustrates the energy band structures of a semiconductor device with an oxide layer, highlighting the mechanisms of charge trapping. In the first part (a), with a negative gate voltage ($V_g < 0$), holes (depicted as red circles with "+") are trapped at the interface and in oxide traps below the Fermi level (E_F). In the second part (b), with a positive gate voltage ($V_g > 0$), electrons (shown as blue circles with "-") are trapped at the interface and in oxide traps above the Fermi level. Both diagrams feature key energy levels: the conduction band edge (E_C), valence band edge (E_V), intrinsic Fermi level (E_i), and the Fermi level in SiC (E_{FS}). These charge trapping phenomena are crucial for understanding the electrical characteristics and reliability of MOS devices[3, 45].

Conventional characterization techniques for Si MOSFETs, such as capacitance-voltage and conductance-voltage measurements, are employed to identify electrically active defects with energy levels corresponding to gate biases in the depletion region of operation. Researchers have adapted these techniques for the SiC-SiO_2 interface. However, it is crucial to accurately evaluate the SiC-SiO_2 interface in terms of the electrically active defects that influence the field-effect mobility in SiC MOSFETs. This evaluation is necessary for further developing passivation processes to enhance the electrical characteristics of these devices. [46, 47] In SiC

devices, the energy levels of these defects do not align with the factors that degrade field-effect mobility in SiC MOSFETs.

1.4.2. Gate leakage current

Leakage current in SiC MOSFETs presents a critical concern, as it signifies the undesired flow of current when the device should be in the off state. This issue not only results in power dissipation but also impacts device performance and overall reliability of the power devices [48]. Addressing leakage current involves a multi-faceted approach and requires the consideration of different factors that contribute to its occurrence. Reverse bias-pn junction leakage current, appearing at the drain/source and substrate junctions when reverse biased, can be mitigated by modifying the doping concentration and reducing the junction area [49, 50]. Subthreshold leakage current, flowing through the channel when the gate voltage is below the threshold voltage but above zero, can be alleviated by adjusting the threshold voltage and channel length. Drain-induced barrier lowering (DIBL), which reduces the potential barrier at the source due to the drain's electric field, can be controlled by altering the drain voltage and channel length. Drain-induced barrier lowering (DIBL), which reduces the potential barrier at the source due to the drain's electric field, can be controlled by altering the drain voltage and channel length. The second roll-off, related to threshold voltage reduction with increasing drain voltage, can be regulated using lightly doped drain (LDD) structures and halo implants [51]. Furthermore, the impact of operating temperature on leakage current can be effectively mitigated through the implementation of advanced cooling systems and precise temperature sensors. These measures help maintain optimal operating conditions, thereby reducing the risk of increased leakage currents due to elevated temperatures. Quantum mechanical tunnelling, which contributes to gate oxide leakage current, can be minimised by employing high-quality gate oxide materials and reducing the oxide thickness. This approach ensures a robust barrier against tunnelling effects, enhancing the overall reliability of the device. Leakage currents resulting from hot carrier injection from the substrate to the gate oxide and gate-induced drain lowering (GIDL) can be significantly curtailed through several strategies. Utilising low-resistance substrates helps in reducing the energy of carriers, thereby minimising hot carrier injection. Additionally, avoiding high drain voltages and implementing high-k gate dielectrics while limiting high gate voltages are crucial steps. These measures collectively contribute to reducing GIDL and enhancing device performance[52, 53]

Analysing gate leakage currents based on gate current is a challenging task. The charging and discharging transients of the gate capacitance are the primary factors controlling the gate current. Parasitic inductance complicates this estimation by introducing second-order ringing. Attempts to detect ageing based on peak gate current may result in false-positive monitoring signals. The measured gate current during one switching period, for instance, is depicted in Fig. 1.4 and demonstrates this complexity. During the on-state, gate leakage current in a healthy SiC device is on the order of a few µA; in an aged device, this current ranges between 10 and 25 mA[54]. On the other hand, during switching, the measured gate current is only a few amps. Because gate leakage current estimation can only be performed after the gate current has reached steady state, this difference in magnitude makes the process challenging. Power converters typically run at 100 kHz or higher, and complex digital circuitry is needed for the steady-state measurement to sample and extract the pertinent waveform segments [55].

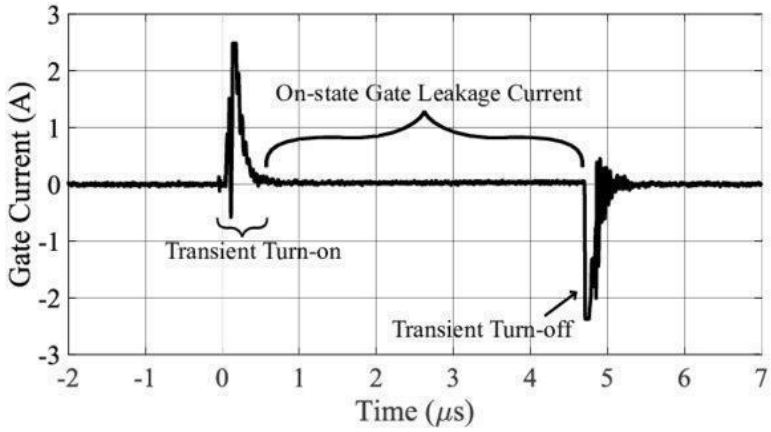


Figure 1.6 Gate current of a SiC MOSFET in the presence of a 20 mA on-state gate leakage current during one switching period using a differential probe across the external gate resistor[56]

Managing in SiC MOSFETs is imperative for achieving peak device performance and reliability. Employing suitable device design and fabrication techniques offers the potential to reduce or eliminate several types of leakage current in SiC MOSFETs, thereby enhancing their advantages compared to traditional devices. For example, techniques have been developed to estimate gate leakage current in SiC MOSFETs[57, 58] , it is crucial to acknowledge that there are inherent limitations and trade-offs to be addressed, necessitating further research and development efforts to explore novel materials, structures, and processes aimed at further enhancing SiC MOSFETs for diverse applications [59].

1.4.3. Threshold Voltage Instability

Threshold voltage instability in SiC MOSFETs is a significant reliability concern, particularly under high-temperature and high-gate-bias conditions. this instability is primarily caused by the coupling of electrical and thermal stresses, leading to the capture and release of charge carriers at the SiC/SiO_2 interface. The resulting threshold voltage (VTH) shift can degrade device performance and reliability, posing challenges for high-power and high-temperature applications. Research efforts to mitigate threshold voltage instability have focused on improving gate oxide quality and developing advanced models to predict and manage V_{TH} shifts. Techniques such as optimising the gate oxide thickness, using high-k dielectrics, and implementing passivation layers have shown promise in reducing instability. Additionally, compact models that account for temperature-dependent trap densities and phonon-assisted tunnelling mechanisms are being developed to enhance the accuracy of simulations and improve device reliability.

There have been several experimental studies on SiC threshold hysteresis, While these experi ments have revealed some fundamental properties of threshold hysteresis, they were not inten ded to provide quantitative data on the submillisecond dynamic behaviour of ΔV_{TH}. For insta nce, they could not measure the evolution of ΔV_{TH} under a negative gate bias or the speed of recovery when switching to a positive bias, considering the magnitudes of these biases and te mperature variations.

1.4.4. Gate Dielectric

SiC MOSFETs hold great potential for use in high-performance power electronics applications such as electric vehicles. In SiC MOSFETs, the gate dielectric is a necessary feature. The transistor is controlled by the gate dielectric, which enables the electron flow between the source and drain regions. Hence the choice of gate dielectric material has a significant impact on SiC MOSFET performance and reliability, and in particular specific channel resistance. The specific channel resistance is inversely proportional to the dielectric capacitance. Therefore, there is a drive to higher dielectric constant materials for the gate to enable lower specific channel resistance. Conventional gate dielectrics used in SiC MOSFETs, like silicon dioxide, are constrained by their large leakage currents and low breakdown voltages under the severe operating conditions of SiC devices. Recent studies have shown that alternative gate dielectric materials can offer lower leakage currents and higher breakdown voltages to get around these limitations [60–62]. To resolve these challenges, a variety of alternative gate dielectrics, including high-k materials, such as hafnium oxide (HfO_2) and nitrides such as silicon nitride

(Si_3N_4 and oxynitrides such as aluminium oxynitride (AlON), have been investigated for use in SiC MOSFETs. Resulting in greater dielectric constants than SiO_2, these materials can enhance device performance by lowering the electric field in the gate dielectric [11, 51, 63]. However, each new dielectric may bring with them new challenges to address such as, defect passivation, thermal stability, interface engineering, and compatibility with SiC substrates. However, the optimal thickness and composition of the stack needs to be carefully optimised to avoid adverse effects on the device characteristics. Also, the band alignments need to be carefully considered as there should be sufficient offset to prevent any leakage current (see figure 1.6). As can be seen in the figure 1.7 SiO_2 has an of 2.7eV from the SiC conduction band and 3.05eV from the SiC valence band which is more than adequate. However, it is not a high k dielectric and has interfacial defects due to carbon being present during the thermal oxidation. Hence the drive towards other dielectrics, which are deposited by other techniques and exhibit high k and high breakdown fields (MV/cm) which are summarised in the figure. AlOx has recently been investigated as a very good candidate dielectric to replace SiO_2.

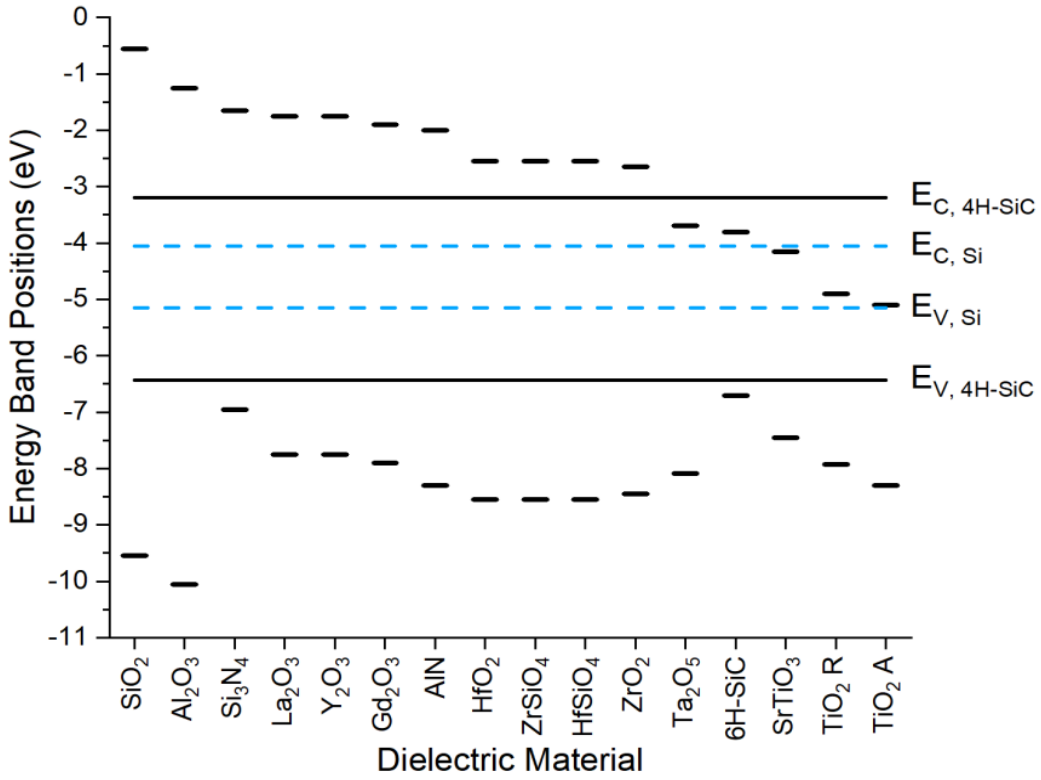


Figure 1.7 Different high-k dielectrics, their breakdown field, band offsets, bandgap in relation to 4H-SiC [51, 64, 65]

1.5. SiC applications

In power electronics, SiC is highly valued due to its superior electrical properties, including high thermal conductivity, high electric field breakdown strength, and low intrinsic carrier

concentration. These attributes enable the production of more efficient and compact power devices. SiC-based power inverters are extensively used in electric vehicles (EVs) and renewable energy systems like solar inverters. This is due to the fact that SiC switching devices such as SiC MOSFETs and the SiC Schottky diodes benefit from lower losses (higher efficiency) and faster switching speeds compared to their silicon counterparts. This results in reduced energy losses and improves overall system performance, making SiC an essential component in modern power electronics solutions. SiC power devices can operate at high frequencies and at power as can be seen in fig. 1.6. It shows the typical application range as 1kW- 500kW, with switching frequency range from 10kHz-10MHz [9, 39, 66, 67].

The automotive sector leverages SiC to enhance the performance and efficiency of various components. In electric vehicles, SiC devices are integrated into the powertrain and charging systems to improve energy efficiency and reduce heat generation, leading to longer battery life and increased driving range. Furthermore, SiC components in ignition systems withstand higher temperatures and voltages, providing better performance and reliability [39, 68–71]. This not only enhances the efficiency of conventional internal combustion engines but also supports the growing shift towards electric mobility by enabling faster charging and better energy management. SiC's high thermal stability, mechanical strength, and resistance to radiation make it a prime candidate for aerospace and defence applications. In high-temperature environments such as turbine engines, SiC components maintain structural integrity and performance. SiC is also used in the construction of randoms?? due to its transparency to radar frequencies and resistance to harsh environments. This ensures reliable protection for radar antennas, crucial for both military and civilian aircraft. The material's resilience under extreme conditions makes it indispensable in the development of next-generation aerospace technologies [72].

In the renewable energy sector, SiC significantly improves efficiency, durability and due to high frequency operation creates smaller systems. SiC-based solar inverters and solar power optimizers are integral to photovoltaic systems, enhancing the efficiency of solar power generation. Also in wind power applications, SiC devices used in turbine converters reduce energy losses and improve overall system performance. Furthermore, SiC is being explored for use in smart grid technologies, where its ability to handle high voltages and currents can improve the reliability and efficiency of power distribution networks. This contributes to the advancement of sustainable energy solutions, crucial for reducing the global carbon footprint [73–76].

SiC substrates are crucial in the manufacturing of high-brightness light-emitting diodes (LEDs). These substrates enable the production of brighter and more efficient LEDs, which are widely used in various lighting applications, including residential, commercial, and industrial settings. The improved thermal management and electrical efficiency of SiC-based LEDs contribute to longer lifespan and reduced energy consumption. This makes them an environmentally friendly alternative to traditional lighting solutions, supporting the global shift towards energy-efficient technologies [77, 78].

In telecommunications, SiC is used for its ability to operate at higher frequencies and power levels. SiC-based radio frequency (RF) devices are employed in high-power and high-frequency applications such as base stations and satellite communications. The material's high thermal conductivity and robustness ensure reliable performance in demanding conditions, facilitating the development of advanced communication networks [79]. As the demand for faster and more reliable communication continues to grow, SiC's role in enabling next-generation wireless technologies becomes increasingly important.

SiC's hardness and chemical stability make it ideal for various industrial applications. As a ceramic abrasive material, SiC is widely used in grinding, cutting, and polishing due to its exceptional hardness. It also serves as a key component in refractory materials, where its high thermal conductivity and resistance to thermal shock make it suitable for use in kiln furniture and other high-temperature environments. The material's durability and resistance to wear extend the lifespan of industrial equipment, reducing maintenance costs and improving operational efficiency. In the semiconductor industry, SiC is used to create components capable of operating under extreme conditions. High-temperature electronics benefit from SiC's ability to function at temperatures much higher than those possible with silicon (SiC; ~400 ^{0}C if the packaging allows, compared to Si which typically operates to 125 ^{0}C), making them ideal for use in harsh environments such as deep-well drilling and aerospace. High-voltage devices, including diodes and transistors, also utilise SiC to improve performance in power distribution systems. This enables the development of more efficient and reliable electronic systems, supporting advancements in a wide range of technologies [10, 80, 81].

SiC's biocompatibility and durability open possibilities in medical technology. It is being explored for use in various medical implants due to its compatibility with human tissue and resistance to wear and corrosion. Potential applications include orthopaedic implants, dental restorations, and cardiovascular devices. The material's inert nature ensures minimal

interaction with body tissues, reducing the risk of inflammation and rejection. This makes SiC an attractive option for long-term medical implants, contributing to improved patient outcomes and quality of life[82, 83].

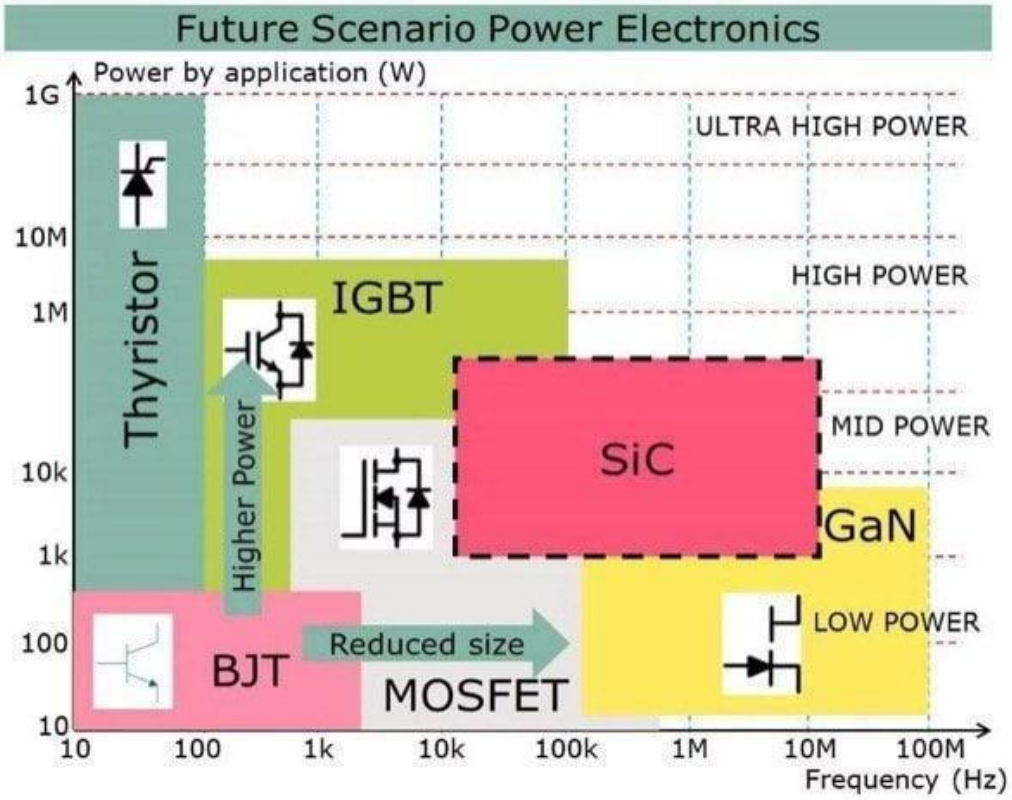


Figure 1.8 SiC switch market 1kW- 500kW @ 10kHz-MHz

SiC is also used in environmental protection and safety applications. SiC membranes are employed for water and gas filtration due to their chemical inertness and mechanical strength. These membranes provide effective filtration in harsh chemical environments, ensuring the removal of contaminants and improving water quality. In safety applications, SiC ceramics are used in personal and vehicle Armor for their lightweight and high hardness, providing effective protection against ballistic threats. This enhances the safety of military personnel and law enforcement officers, highlighting SiC's critical role in protective technologies [55, 83, 84].

Owing to their exceptional properties, the SiC semiconductor market is anticipated to expand rapidly in the coming years. As illustrated in Fig. 1.8, the market is projected to grow at a compound annual growth rate (CAGR) of 30%, increasing from $225 million in 2019 to $2.5 billion by 2025, according to a report by Yole Development. The adoption of SiC semiconductors spans a diverse array of industrial applications, including electric vehicles (EVs), photovoltaics, energy storage systems, power supplies, and motor drivers [85–87].

Among SiC semiconductors, SiC MOSFETs are the most advanced active switches available. With a breakdown field that is ten times higher than that of silicon, SiC MOSFETs with ultra-high-voltage ratings (>10 kV) are practically feasible. Currently, SiC MOSFETs with ratings of 1.2 kV, 1.7 kV, and 3.3 kV are commercially available, capable of replacing silicon insulated gate bipolar transistors (IGBTs) at equivalent voltage ratings. Wolfspeed has introduced 10 kV SiC MOSFETs, surpassing the maximum voltage rating of 6.5 kV IGBTs, with ongoing laboratory research. The high breakdown voltage of SiC MOSFETs is appealing for reducing complexity and enhancing the reliability of power electronics in high-voltage applications.

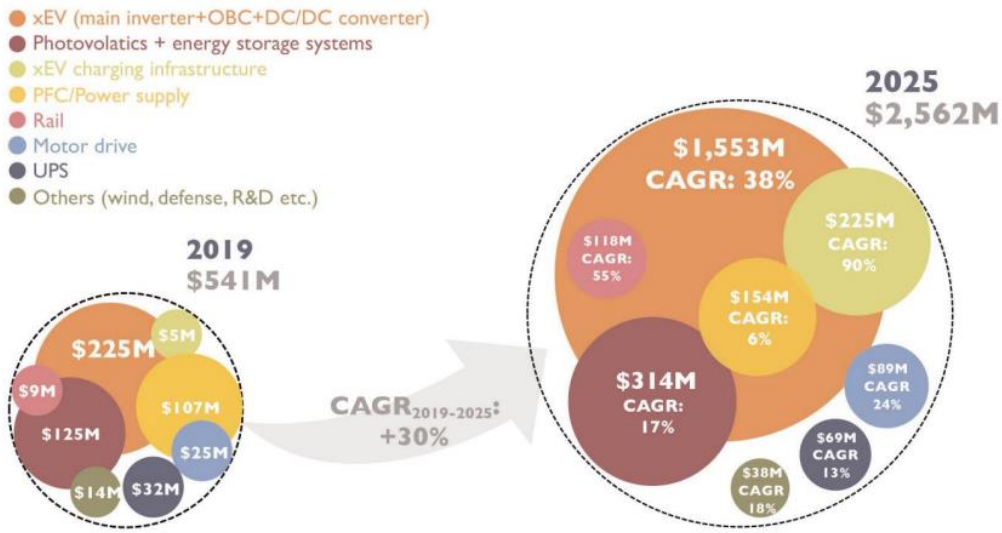


Figure 1.9 2019-2025 market forecast of SiC power semiconductor split by application [85]

This chapter has provided a foundational understanding of SiC power electronics. It explored the background and advantages of SiC over traditional silicon, delving into the various polytypes of SiC and their unique physical properties. The chapter also identified the key challenges associated with SiC power electronics, including near interface traps, gate leakage current, threshold voltage instability, and the crucial role of the gate dielectric. Finally, it discussed the diverse applications of SiC in power electronics, highlighting its potential to revolutionize various industries. Building upon this foundation, Chapter 2 will delve into the intricacies of SiC Power MOSFETs. It will explore the fundamental principles of MOSFET operation, analyse their equivalent circuit models, and investigate the mechanisms of device breakdown. Furthermore, it will classify power MOSFETs into different categories, such as vertical power MOSFETs, D-MOSFETs, and U-MOSFETs, and discuss their unique characteristics and performance advantages.

2. SiC Power MOSFETs

2.1. Introduction

A semiconductor device is classified as a power device when it functions as a rectifier or switch within power electronics. These power devices are integral to the operation of power electronics systems. The inception of power devices dates to 1950. Since then, a variety of silicon (Si) power devices have been developed, including bipolar power transistors (BPT or BIT), insulated gate bipolar transistors (IGBT), gate turn-off thyristors (GTO), static induction transistors (SIT), and power MOSFETs. Despite significant advancements, Si power devices have encountered performance limitations. The progress in power devices has been driven by the introduction of wide bandgap (WBG) materials, which offer superior material properties. These WBG-based power devices, particularly those made from silicon carbide (SiC), have enabled substantial improvements in performance. Most SiC-based power rectifiers and switches for high-voltage applications are designed as vertical devices, utilising semiconducting substrates. This vertical structure allows for efficient handling of high voltages and currents. On the other hand, certain high-power radio frequency (RF) devices, such as metal-semiconductor field-effect transistors (MESFETs), are designed with a horizontal structure and typically use semi-insulating substrates. This horizontal design is advantageous for RF applications due to its ability to manage high frequencies effectively. The introduction of SiC-based devices has opened new possibilities in power electronics, offering higher efficiency, greater thermal conductivity, and the ability to operate at higher temperatures compared to traditional Si devices. These attributes make SiC power devices particularly attractive for applications in electric vehicles, renewable energy systems, and industrial power supplies, where performance and reliability are critical [70, 88].

Silicon carbide (SiC) power devices offer several notable advantages over their silicon (Si) counterparts. Firstly, SiC Schottky Barrier Diodes (SBDs) can achieve a breakdown voltage of approximately 1700 V, significantly higher than the 200 V breakdown voltage of Si-based SBDs. SiC diodes can reach breakdown voltages around 20 kV, comparable to high-pressure Si stacks, while SiC MOSFETs boast a breakdown voltage of about 10 kV, in contrast to the 1 kV breakdown voltage of Si MOSFETs. This enhanced voltage capability allows for more robust performance in high-voltage applications. Additionally, SiC devices can be designed with significantly fewer parallel and series components than Si devices, reducing their complexity and size by up to 90%, which enhances their reliability and efficiency. SiC devices also exhibit superior switching performance, with a negligible reverse recovery rate at

equivalent voltage levels, making them ideal for high-frequency operations in the range of tens of MHz Furthermore, SiC devices generally have a positive temperature coefficient compared to Si devices, allowing them to achieve larger currents using parallel chips, which simplifies the design of high-voltage, high-current devices [89–91].

Among power devices, the power MOSFET stands out as one of the most widely used due to its rapid switching speed, low gate drive power, and ability to handle both high current and voltage applications without destructive failure. When comparing SiC-based power MOSFETs to their Si-based counterparts, SiC power MOSFETs achieve a significantly lower on-resistance ($R_{on,sp}$), resulting in reduced parasitic capacitance and faster switching speeds. Consequently, SiC-based power devices experience lower conduction and switching losses across a wide range of blocking voltages. Additionally, a key advantage of SiC MOSFETs over Si MOSFETs is their thermal performance: as the temperature increases from 25 to 135 °C, the on-resistance of SiC MOSFETs rises by only 20%, compared to a 250% increase for Si MOSFETs[92].

Table 2.1 Specifications of Various Semiconductor Devices from Different Manufacturers [75, 93]

Manufacturer	Model	Voltage Rating	Current Rating	Year
Texas Instruments	TIDA-01605	1200V	40A	2020
Microchip Technology	APT40SM120B	1200V	40A	2021
Toshiba	MG800FXF2YMS3	1700V	800A	2022
ROHM	SCT3030AL	900V	118A	2019
Wolfspeed	C3M0065100K	1000V	32A	2021
STMicroelectronics	SCTW100N65G2V	650V	100A	2020
Infineon	IMW120R045M1H	1200V	45A	2022

Since the introduction of the first silicon carbide (SiC) power MOSFET in 2001, these devices have seen remarkable advancements. The commercialization of SiC power devices has evolved significantly, as illustrated in various industry reports. Today, the leading suppliers of SiC power devices include Cree/Wolfspeed, Microsemi, Infineon, GeneSiC, STMicroelectronics, Mitsubishi, and ROHM. According to market research by Yole, these companies collectively

hold 80% of the SiC power semiconductor market. The most commonly available SiC power devices on the market today are SiC Schottky diodes, SiC JFETs, SiC BJTs, and SiC MOSFETs.

Some of the highest-rated SiC devices in terms of voltage and current include SiC Schottky diodes with ratings of 1.7 kV/25 A, discrete SiC MOSFETs rated at 1.7 kV/72 A, SiC MOSFET modules from Cree/Wolfspeed rated at 1.7 kV/225 A, and SiC BJT modules from GeneSiC rated at 1.7 kV/160 A. Additionally, GeneSiC offers SiC BJTs designed for high-temperature applications, capable of operating at 210 °C with a voltage/current rating of 600 V/20 A. These advancements highlight the significant progress and growing importance of SiC technology in the power semiconductor industry [78, 79]. A typical MOSFET is a field-effect transistor (FET) featuring a metal gate electrode placed atop a silicon dioxide (SiO_2) or dielectric layer, which itself rests on a semiconductor substrate. MOSFETs can be fabricated in two configurations: n-channel MOSFETs and p-channel MOSFETs [94, 95]

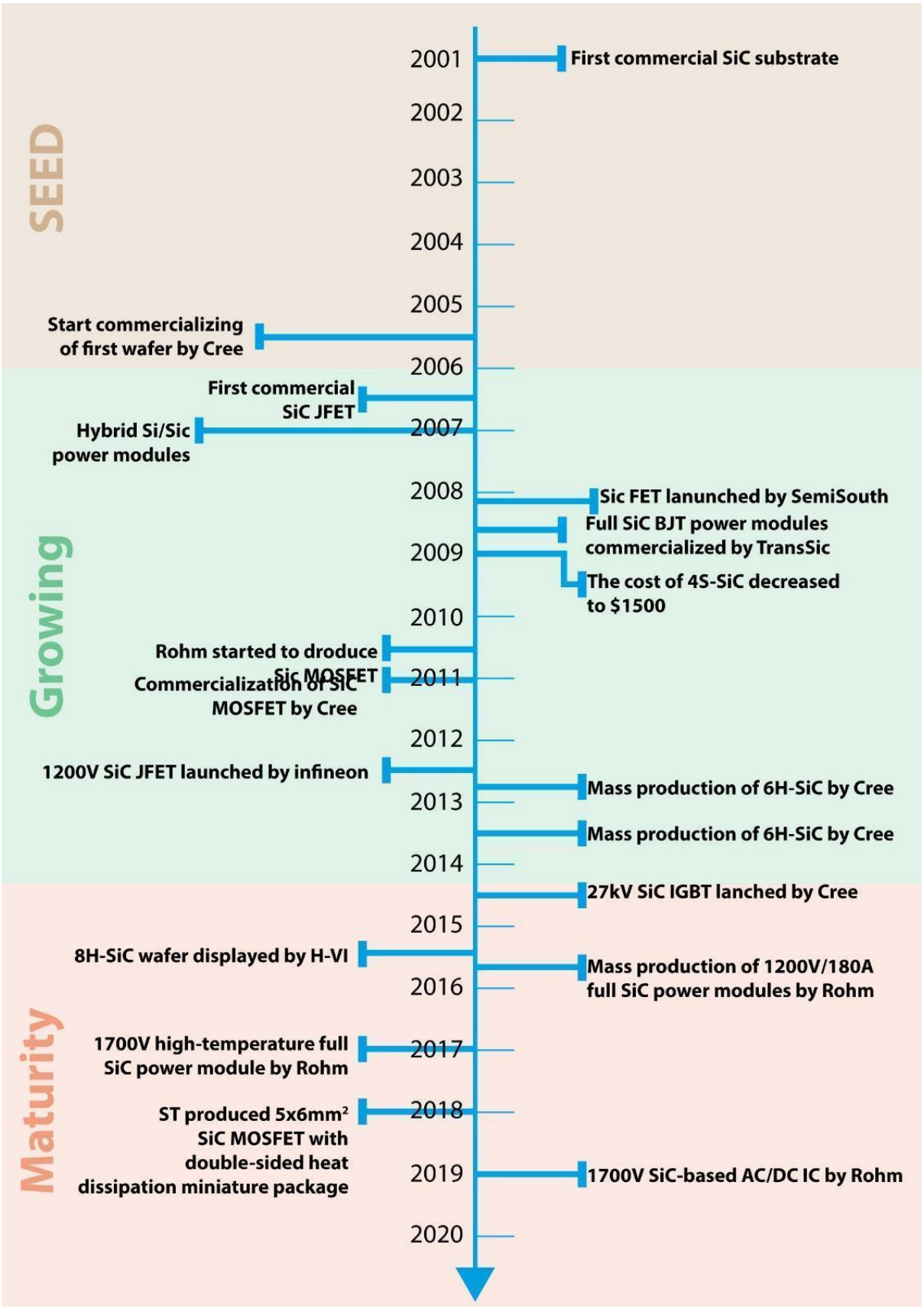


Figure 2.1 Timeline of the developed of SiC Power Semiconductor device [1]

2.2.Principles of MOSFET

The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) originates from a MOS capacitor, where the gate voltage (V_g) regulates the state of the semiconductor surface beneath it by creating either an accumulation or inversion layer. The structure depicted in Figure 2.1 illustrates an n-channel MOSFET, characterised by a gate length (Lg) and width (W). This device comprises a p-type with n-type contacts on upper and lower surface: a low potential region known as the source (n+) and a high potential region referred to as the drain (n+). The n+ layers indicate heavily doped regions. A thin layer of silicon dioxide (SiO_2) is deposited on the top surface, followed by a polysilicon gate material placed on top of the SiO_2 layer.

When a positive V_g is applied, it inverts the semiconductor surface under the gate from p-type to n-type, creating an electron-rich path known as a channel. In an n-channel MOSFET, a positive V_g greater than the threshold voltage (V_{th}) is necessary to form an inversion layer of electrons in the channel. Conversely, in a p-channel MOSFET, a negative V_g exceeding the threshold voltage is required to induce an inversion layer of holes, forming the channel.

For a p-channel MOSFET, a negative gate voltage (V_g) exceeding the threshold voltage (V_{th}) is required to induce an inversion layer of holes, thereby forming a conductive channel. The threshold voltage in a MOSFET is defined as the minimum gate voltage necessary to strongly invert the surface of the substrate beneath the gate electrode. For power MOSFETs, this threshold voltage is typically measured at a drain-source current of 250 µA. Ensuring safety in circuit design is more straightforward when a power MOSFET is off at zero gate voltage (normally off device) [96, 97].

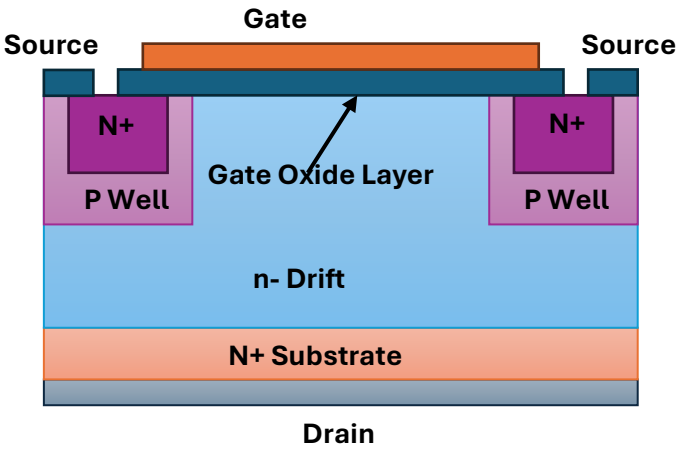


Figure 2.2 cross sectional view of n channel MOSFET

The threshold voltage (V_{TH}) can be expressed as:

$$V_{TH} = \Delta V_{OX} + \Delta \emptyset_s = V_{OX} + \emptyset_s + \emptyset_{ms} \text{----------(2.1)}$$

where $\emptyset_s$ is the surface potential, $\emptyset_{ms}$ is the metal-semiconductor work function difference, andV_{OX} is the potential drop across the oxide. At a threshold voltage, the surface potential $\emptyset_s$ = 2φf p. This expression can be substituted into Equation (2.1) as

$$V_{TH} = V_{oxT} + \emptyset_{ms} + 2\emptyset_{fp} \text{----------(2.2)}$$

where V_{oxT} is the voltage across the oxide at the threshold inversion point and $\emptyset_{fp}$is the potential difference between EF i and EF (in V) given by:

$$\emptyset_{fp} = \frac{kT}{q} ln\ ln\ \frac{N_a}{n_i} \text{----------(2.3)}$$

Here, (k) represents Boltzmann's constant, (T) denotes the absolute temperature, (q) is the electronic charge, N_a is the acceptor doping concentration of the substrate, and n_i stands for the intrinsic carrier concentration of silicon.

The voltage across the oxide at the threshold inversion point can be expressed as:

$$V_{oxT} = \frac{Q_{mT}'}{C_{ox}} \text{----------(2.4)}$$

where $Q_{mT}'$is the charge density on the metal gate at threshold andC_{ox} is the gate oxide capacitance.

$$Q'_{mT} = |Q'_{SD}(max)| - Q'_{ss} \text{----------(2.5)}$$

Where Q'_{mT} represents the charge density on the metal gate at the threshold, $Q'_{SD}(max)$ denotes the conservation of charge density between the metal and the oxide-semiconductor interface, and Q'_{ss} signifies the charge density next to the oxide-semiconductor interface.

The gate oxide capacitance can be described as:

$$C_{0x} = \frac{\varepsilon_{ox}}{t_{ox}} \text{----------(2.6)}$$

The dielectric constant of the oxide is denoted as ε_{ox} and t_{ox} represents the thickness of the oxide layer in the gate dielectric. By substituting Equations (2.5) and (2.6) into Equation (2.2), the equation can be reformulated as:

$$V_{TH} = \frac{|Q'_{SD}(max)|}{C_{ox}} - \frac{Q'_{ss}}{C_{ox}} + \emptyset_{ms} + 2\emptyset_{fp}\text{----------(2.7)}$$

By utilising Equation (2.7) and assuming a flat-band voltage V_{FB}, V_{TH} can be represented as:

$$V_{TH} = \frac{|Q'_{SD}(max)|}{C_{ox}} + V_{FB} + 2\emptyset_{fp}\text{----------(2.8)}$$

$$V_{FB} = \emptyset_{ms} - \frac{Q'_{ss}}{C_{ox}}\text{----------(2.9)}$$

$$|Q'_{SD}(max)| = \sqrt{4q\varepsilon_{si}\emptyset_{fp}N_a}\text{----------(2.10)}$$

In the linear operating region of a MOSFET, the channel resistance (R_{ch}) can be described as

$$R_{Ch} = \frac{L_{ch}t_{ox}}{W\mu_n\varepsilon_{ox}(V_{GS}-V_{TH})}\text{----------(2.11)}$$

where L_{ch} represents the channel length, t_{ox} denotes the gate oxide thickness, V_{GS} is the gate voltage, V_{TH} stands for the threshold voltage, ε_{ox} is the dielectric constant of the oxide, μ_n signifies the average electron mobility in the channel, and (W) indicate

s the channel width.

2.3.Equivalent Circuit of an n-channel MOSFET

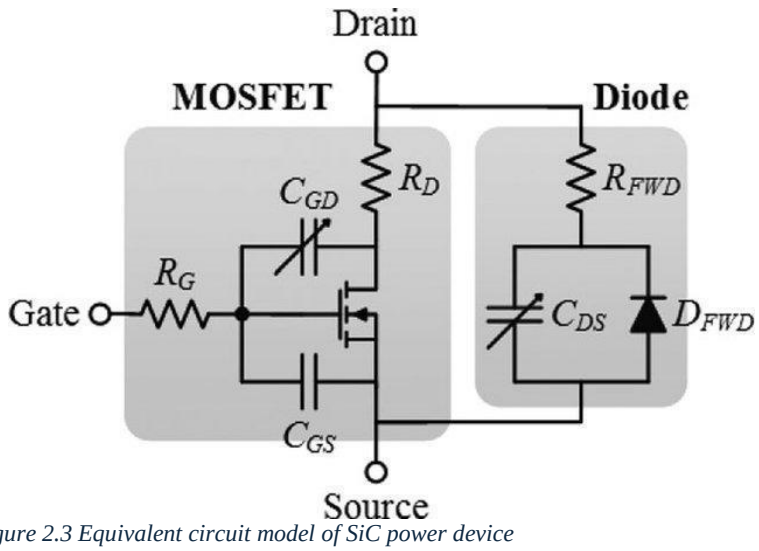


Figure 2.3 Equivalent circuit model of SiC power device

A typical Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is essentially an enhanced version of a MOS capacitor structure. In this configuration, the drain and source terminals are electrically insulated from the gate terminal, as depicted in Figure 2.2. The capacitance between the gate and source (C_{gs}) and the gate and drain (C_{gd}) is primarily determined by the thickness of the gate oxide layer. On the other hand, the capacitance between the drain and source (C_{ds}) is a junction capacitance associated with the parasitic diode.

These intrinsic capacitances are redefined into three key parameters that describe the parasitic capacitances of a MOSFET: input capacitance (C_{iss}), output capacitance (C_{oss}), and reverse transfer capacitance (C_{rss}). The input capacitance, C_{iss}, represents the total capacitance seen at the gate and is the sum of Cgs and C_{gd}, i.e., ($C_{iss} = C_{gs} + C_{gd}$. This capacitance is charged by the gate charge (Q_g) to activate the MOSFET.

The output capacitance, C_{oss}, is the sum of C_{ds} and C_{gd}, i.e., ($C_{oss} = C_{ds} + C_{gd}$. This capacitance represents the total capacitance on the output side of the MOSFET. A smaller C_{oss} is preferred for faster turn-off times of the device, as it allows for more efficient switching. The reverse transfer capacitance, C_{rss}, is approximately equal to C_{gd} and is also known as Miller capacitance. This capacitance is crucial as it allows the dynamic input capacitance to exceed the sum of the static capacitances, creating a feedback loop between the output and input of the device. Furthermore, the internal gate resistance (R_g) is a critical parameter that affects the switching performance, thermal management, and power conversion efficiency of the MOSFET. A higher R_g results in slower switching and increased gate drive losses, leading to higher device temperatures. The non-linearity of C_{gd} and its dependence on the drain bias make it less suitable as a parameter for defining power in MOSFETs. Therefore, the standard practice for describing a power MOSFET involves extracting the gate charge (Qg) at a constant current source [48, 50, 98].

2.4. Theory of Device Breakdown

Enhancements in the performance of power devices aim to achieve negligible current flow during the off state, at high voltage. The ability of a power device to withstand a maximum voltage without a significant increase in current is constrained by the phenomenon known as avalanche breakdown. This breakdown is heavily influenced by the distribution of the electric field within the device. During the off-state of a power device, electron-hole pairs are injected into the depletion region. These pairs gain sufficient kinetic energy from the longitudinal electric field to generate additional electron-hole pairs through collisions with lattice atoms within the space charge region. This process, known as impact ionisation, results in the creation of more electron-hole pairs as carriers acquire high kinetic energy. Impact ionisation is a self-sustaining, multiplicative process. As more electron-hole pairs are generated, the current increases uncontrollably, preventing the device from maintaining an elevated voltage. This leads to avalanche breakdown, which ultimately limits the maximum operating voltage of the device. In addition to avalanche breakdown, power devices can also experience punch-through breakdown. This occurs when the depletion region extends through the entire device, causing

a direct path for current flow and resulting in device failure. Both avalanche and punch-through breakdowns are critical considerations in the design and operation of power devices [49, 99, 100].

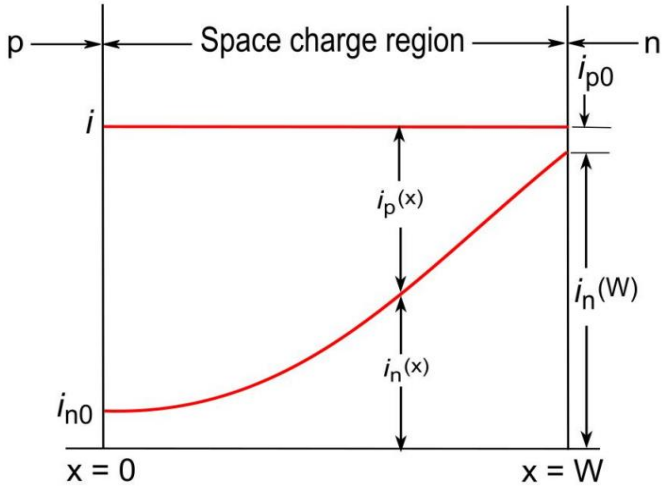


Figure 2.4 Current and hole components through the space charge region

Let us suppose that a reverse-biased current in 0 enters the depletion region at x = 0 as shown in Figure 2.4, the current in will rise with the distance through the depletion region due to the avalanche procedure. The current at the point where x = W can be written as.

$$i_n(W) = M_n i_{n0} \text{----------(2.11)}$$

where Mn is a multiplication factor. The hole i_p will rise through the depletion region from the n-type to the p-type section and reach a maximum value at x = 0. Thus, the entire charge through the pn junction is constant in steady state.

The elementary increment of the current at some point x can be expressed as

$$di_n(x) = i_n(x)\alpha_n dx + i_p(x)\alpha_p dx \text{----------(2.12)}$$

$\alpha_n$and α_p are the electron and the hole ionisation rates, respectively.

rewritten of equation 2.12

$$\frac{di_n(x)}{dx} = i_n(x)\alpha_n + i_p(x)\alpha_p \text{----------(2.13)}$$

The overall current (i) can be expressed as

$$i = i_n(x) + i_p(x) \text{----------(2.14)}$$

By solving for $i_p(x$ in Equation (2.14) and then substituting the result into Equation (2.13), we obtain:

$$\frac{di_n(x)}{dx} + (\alpha_p - \alpha_n) i_n(x) = i\alpha_p \text{----------(2.15)}$$

Assume that $\alpha_p = \alpha_n$

$$i_n(W) - i_n(0) = \int_0^W \alpha \ dx \text{----------(2.16)}$$

Using Equation (2.11), Equation (2.16)

$$\frac{M_n i_{n0} - i_n(0)}{i} = \int_0^W \alpha \, dx \text{----------(2.17)}$$

Since $M_n i_{n0} \approx$ i, and $i_n(0) = i_{n0}$, Equation (2.17) can be express as

$$1 = \frac{1}{M_n} = \int_0^W \alpha \ dx \text{----------(2.18)}$$

The avalanche breakdown voltage is defined as the voltage at which M_n becomes infinite. Consequently, the condition for avalanche breakdown is described by,

$$\int_0^W \alpha \ dx = 1 \text{----------(2.19)}$$

2.5.Classification of Power MOSFETs

Power semiconductor devices, as illustrated in Figure 2.5, are components with either two or three terminals. These devices can regulate the flow of energy within electronic systems. They operate in two primary states: the off-state, where a negligible current flows through the device while the supply voltage is maintained, and the on-state, where a significant current passes through the device. Power MOSFETs are designed with cells that can be arranged in a parallel configuration. This design compensates for the low current capacity of individual transistors and helps achieve a low on-resistance. As majority carrier devices, power MOSFETs offer several advantages, including low gate drive power, fast switching speeds, and an efficient parallel architecture. These features make them highly suitable for various power applications, such as DC-DC converters, low voltage motor control, linear power supplies, and switching power supplies [34, 101].

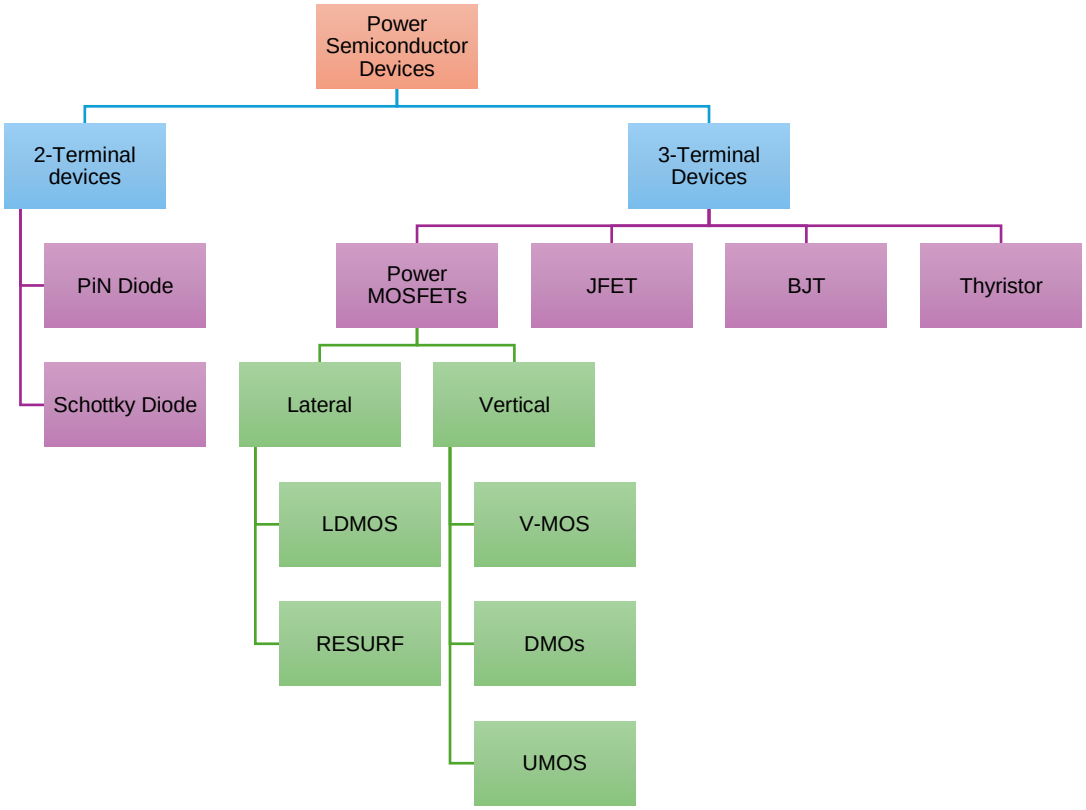


Figure 2.5 Classification of Power Semiconductor Devices: This flowchart categorises power semiconductor devices into 2-terminal and 3-terminal types, detailing various subcategories like PIN Diode, Schottky Diode, Power MOSFETs, JFET, BJT, and Thyristor

Transistors are commonly used in power switches for low voltage applications, typically those operating at less than 200 V. This is because the on-state resistance R_{on} The transistor increases rapidly with an increase in the breakdown voltage (BV). This increase in R_{on} leads to significant conduction losses, which in turn degrade the overall performance of the system. To achieve a low resistive channel in a MOSFET, it is necessary to have a shorter channel length $L_{ch}$and a corresponding reduction in the gate oxide thickness, t_{ox} These two parameters are crucial because they are directly related to the breakdown voltage. However, variations in these parameters limit the use of power MOSFETs in medium and high voltage applications. Single way to overcome this limitation is through the force design of power MOSFETs. This design involves connecting multiple transistors to operate in a multi-level hybrid configuration, which helps manage higher voltages more effectively. Power MOSFETs can be classified into two main types based on their design techniques: lateral and vertical devices. The structure and basic operating principles of both lateral and vertical power MOSFETs will be briefly discussed in the subsequent sections.

2.5.1. Vertical Power MOSFETs

A V-groove MOSFET (V-MOSFET) is a type of metal-oxide-semiconductor field-effect transistor (MOSFET) characterised by its non-planar structure. This device features a V-groove gate design, where the source and drain regions are separated by a p-body substrate. This configuration results in the formation of two p-n junctions, commonly referred to as JA and JB. The gate electrode of the V-MOSFET penetrates a trench that is etched into the device body. This trench is created through a process known as anisotropic etching, which is highly dependent on the crystallographic orientation of the silicon substrate. After the trench is etched, the gate oxide is formed through a thermally oxidation step, and the gate electrode is then deposited[102–104].

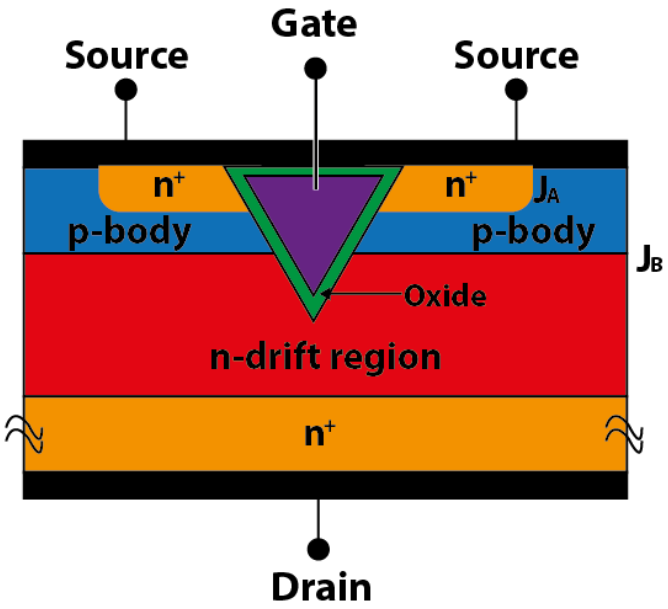


Figure 2.6 Cross sectional representation of V-grove MOSFETs structure

Historically, the V-MOSFET was the first power MOSFET structure to be fabricated and commercialised. However, the stringent conditions required for anisotropic etching, which must align precisely with the silicon crystal orientation, limit the design flexibility of this architecture. This complexity in manufacturing led to the V-MOSFET being less favoured over time. One significant drawback of the V-MOSFET is the degradation of the breakdown voltage. This occurs due to the high electric field crowding at the tip of the V-groove, which can lead to premature breakdown of the device. As a result, the V-MOSFET was eventually replaced by the double-diffusion MOSFET (D-MOSFET), which features a planar architecture that is easier to manufacture and offers better performance characteristics.

2.5.2. D-MOSFETs

The Double-Diffused MOSFET (D-MOSFET) is a type of MOSFET with a planar structure that employs a double diffusion process. In this process, both the p-body region and the source (n+) contact are diffused through a common opening, which is defined by the edge of the gate. This method allows for precise control over the formation of the device's active regions.

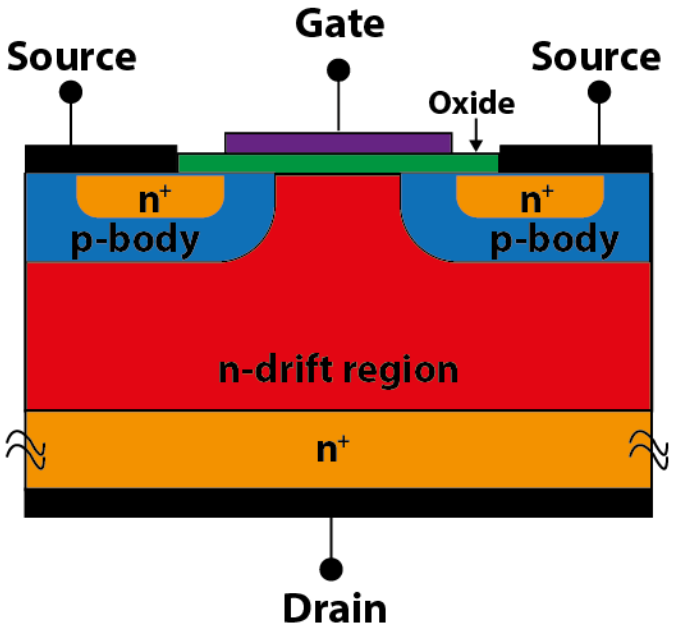


Figure 2.7 Cross sectional representation of Double-Diffused MOSFETs structure

The channel length in a [98] determined by the difference between the lateral diffusion distances of the p-body region and the source (n+). This is illustrated in Figure 2.7. Essentially, the channel length is the distance between the p-body and the source regions after diffusion, which is crucial for the device's electrical characteristics.

In operation, electrons flow laterally through an inversion layer that forms at the interface between the p-body and the gate oxide. These electrons then move into the thick, lightly doped n-drift region. From there, they travel vertically to the drain, establishing a conventional current flow from the drain to the source. However, the D-MOSFET structure has some drawbacks. One significant issue is the non-uniform distribution of current in the drift region. This non-uniformity leads to a higher internal resistance, which is greater than the ideal specific on-resistance of the drift region. This increased resistance can affect the overall efficiency and performance of the device.

2.5.3. U-MOSFET

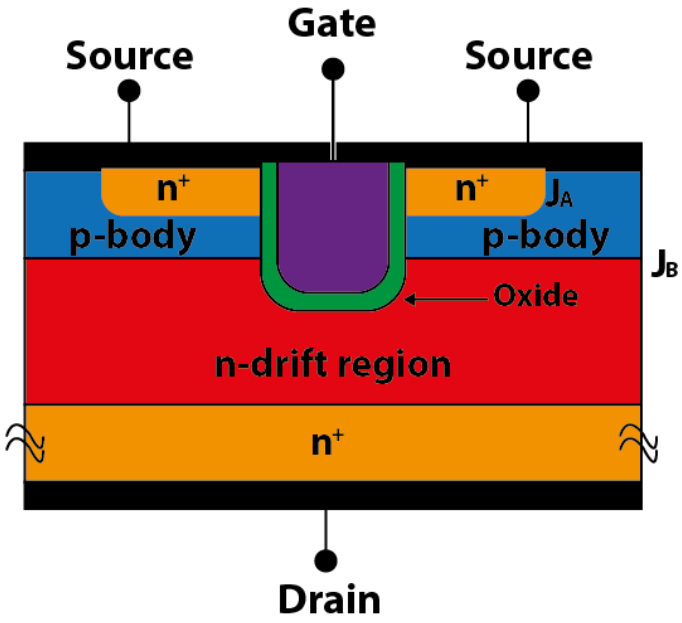


Figure 2.8 Cross sectional representation of Double-Diffused MOSFETs structure

A U-MOSFET (U-shaped Metal-Oxide-Semiconductor Field-Effect Transistor) is a type of MOSFET that features a non-planar structure, like the V-MOSFET. However, instead of a V-shaped groove, it has a U-shaped groove or trench at the gate region, as illustrated in Figure 2.8 [15]. This trench gate is implanted and extends from the top surface of the device, passing through the p-body and the source (n+) regions, and into the n-drift region. This is current state of art device design employed in SiC MOSFETs.

One of the key advantages of the U-MOSFET over the D-MOSFET (Double-diffused MOSFET) is its lower input impedance, which helps in reducing the on-resistance of the device [1]. This is crucial for improving the efficiency and performance of the MOSFET in various applications. The bottom of the trench gate is rounded through a process called isotropic etching. This rounding is essential as it protects the gate oxide and helps in redistributing the electron current, which tends to crowd at the edges of the gate [16]. Additionally, the U-MOSFET benefits from a deeper and more heavily doped p-body. This design ensures that the avalanche breakdown occurs at the junction between the p-body and the n-drift region, enhancing the device's robustness and reliability. Compared to the D-MOSFET, the U-MOSFET offers higher transconductance due to its larger channel density, which allows for better current handling capabilities and overall performance [105, 106].

Chapter 2 delves into the principles, operation, and classifications of Silicon Carbide (SiC) Power MOSFETs. It begins with an Introduction, highlighting the advantages and significance

of SiC technology in power electronics. The fundamental Principles of MOSFETs are explored, explaining their structure and operation. An Equivalent Circuit for n-channel MOSFETs is presented, providing insights into their behaviour and modelling techniques. The Theory of Device Breakdown discusses the mechanisms leading to MOSFET failure, emphasizing factors like voltage stress and thermal limits. The chapter also classifies power MOSFETs, distinguishing between Vertical Power MOSFETs, D-MOSFETs, and U-MOSFETs. Each category is described with its unique structure and applications, showcasing the diversity within power MOSFET designs.

Chapter 3 explores SiC Power Devices, focusing on the SiC IGBT and SiC JFET, which are essential for high-power applications. It begins with an overview of SiC IGBTs, examining their characteristics, gate driver requirements, and modelling techniques. Key fabrication challenges, including defect control and interface properties, are also discussed. The chapter concludes with an introduction to SiC JFETs, highlighting their potential in power electronics. This chapter provides a concise overview of advanced SiC devices, emphasizing their capabilities and the challenges in their development.

3. SiC Power Devices

3.1. SiC IGBT

Silicon-based bipolar devices, such as IGBTs and thyristors, are commonly used in high-power conversion applications, including HVDC transmission systems and circuit breakers. However, the advent of silicon carbide (SiC) devices, which can operate at much higher voltages, has enabled simpler converter designs by reducing the number of levels in multilevel topologies. This advancement enhances efficiency and supports the electrification of more applications, contributing to decarbonization efforts.

The silicon carbide MOSFET is the most extensively studied SiC device structure and is currently available from various vendors with breakdown voltages up to 3.3 kV. Additionally, engineering samples rated up to 15 kV have been produced, demonstrating the suitability of SiC devices for medium and high voltage applications. However, the on-state resistance of unipolar devices increases significantly for voltages above 10 kV due to the thick epitaxial drift layer. Consequently, SiC bipolar devices are more suitable for high-voltage and high-current applications and have garnered significant interest in recent years. Silicon carbide IGBTs combine the ease of voltage control of MOS devices with the low on-state loss of bipolar devices, achieved through conductivity modulation of the drift region. Devices with breakdown voltages up to 27 kV have been shown to achieve improved on-state performance [107–109].

The improvement in on-state performance comes at the cost of higher switching losses due to the time required for minority carriers to be injected and removed during the turn-on and turn-off transients. This trade-off relationship has been extensively studied in silicon bipolar devices, and various methods have been proposed for SiC IGBTs to achieve the optimum trade-off for specific applications. However, efficiency is not the only characteristic that needs optimization. The reliability and ruggedness of SiC devices and SiC-based converters must also be equivalent to, or even better than, the currently available silicon-based converters and devices. Despite the increasing attention SiC devices have attracted, their operation, particularly those achieving blocking voltages above 10kV, presents certain challenges that have not been fully addressed or understood. Specifically, the high dV/dt produced during switching transients can cause EMI issues, voltage spikes, and difficulties in the design of gate drivers. Additionally, achieving equivalent short-circuit robustness to silicon devices is challenging due to the high current density and smaller heat capacity, which lead to rapid temperature rise and eventual device destruction [110].

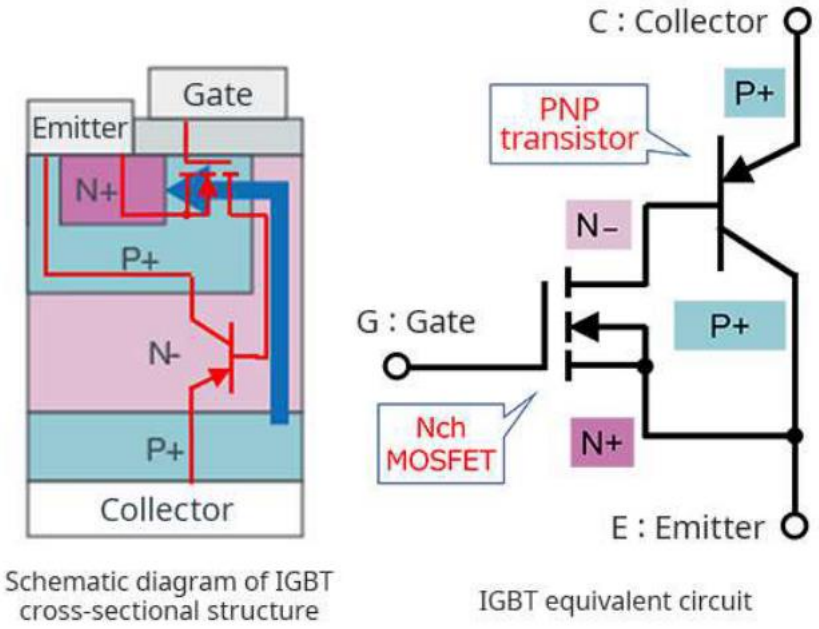


Figure 3.1 structure of IGBT and equivalent circuit

3.2. SiC IGBT Characteristics and Gate Driver

The performance of Silicon Carbide (SiC) IGBTs differ from those of traditional Silicon (Si) IGBTs. This difference arises primarily due to the wide bandgap material properties of SiC and its capability to operate at higher voltages. SiC IGBTs exhibit unique static and dynamic characteristics. These characteristics are influenced by several factors, including the device structure, circuit parameters, and operating temperature [88, 111].

3.2.1. Static Characteristics

The forward characteristics are vital components of the static characteristics of Silicon Carbide Insulated Gate Bipolar Transistors (SiC IGBTs). Figure 3.1 compares the performance of SiC IGBT devices with various blocking voltages as compared to SiC MOSFETs. Generally, the state of SiC IGBTs is lower than that of silicon IGBTs and MOSFETs. This advantage primarily stems from the shorter drift region thickness and the effect of conductivity

modulation in SiC IGBTs. The shorter drift region reduces the resistance path for current flow, while conductivity modulation increases the carrier concentration in the drift region, further lowering the resistance. Despite variations in device parameters causing some dispersion in $R_{on,sp,diff}$ values, the lowest available $R_{on,sp,diff}$ for SiC IGBTs is significantly lower than the theoretical limit for SiC MOSFETs. This makes SiC IGBTs highly efficient for high-power applications, where minimising conduction losses is critical.

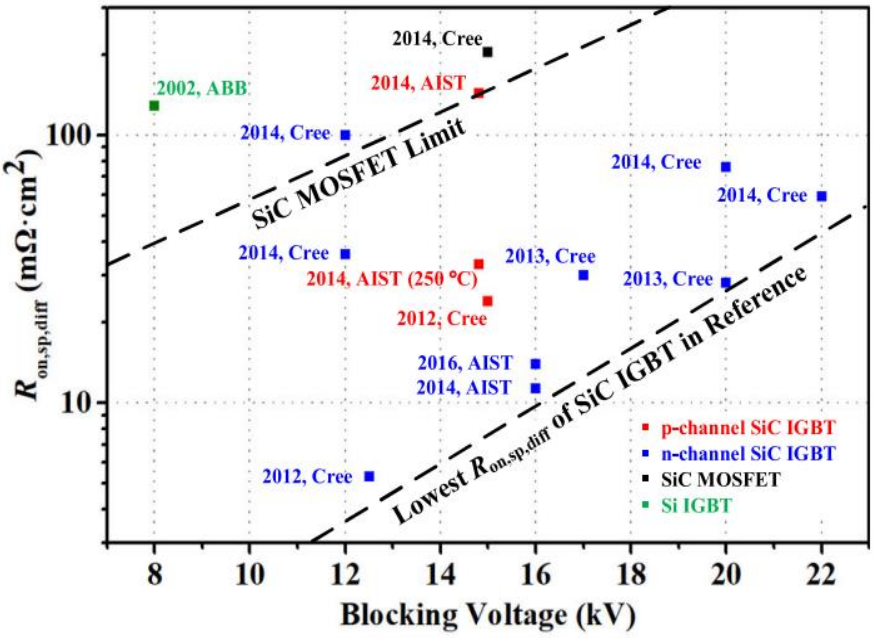


Figure 3.2 A Comparison of Specific On-Resistance vs. Blocking Voltage for Silicon Carbide and Silicon Devices[112, 113]

Furthermore, p-channel devices generally exhibit inferior forward characteristics compared to their n-channel counterparts. This discrepancy arises from the intrinsic material properties and differences in carrier mobility between p-type and n-type Silicon Carbide (SiC). Consequently, n-channel SiC Insulated Gate Bipolar Transistors (IGBTs) are deemed more promising for high-power applications. They provide superior performance, characterised by lower on-resistance and enhanced current handling capabilities. These attributes make n-channel SiC IGBTs particularly suitable for applications such as electric vehicles, renewable energy systems, and industrial power supplies. The blocking capability of these devices, which is influenced by termination technologies, is another critical aspect. These characteristics are essential to ensure that the device can withstand high voltages without breaking down, which is crucial for reliable operation in high-power circuits [88, 114].

Table 3.1 Summary of Specific On-Resistance and Blocking Voltage for Various SiC Devices from Different Manufacturers Over the Years[115, 116]

Year	**Manufacturer**	**Device Type**	**Specific On-Resistance ($R_{on,sp,diff}$)**	**Blocking Voltage (kV)**
2014	Cree	SiC MOSFET	14.2 mΩ·cm²	3.85
2013	Cree	SiC MOSFET	-	2
2012	Cree	SiC MOSFET	-	1.2
2014	AIST	SiC MOSFET	0.63 mΩ·cm²	1.17
2016	AIST	SiC MOSFET	-	1.2
2014	AIST (250 ℃)	SiC MOSFET	-	-
2024	Nexperia	SiC Diode	0.63 mΩ·cm²	1.17
2024	Sumitomo	SiC MOSFET	-	3.3
2022	PGC Consultancy	SiC MOSFET	-	1.25
2024	J-STAGE	SiC Unipolar	-	5

The table 3.1 highlights significant advancements in Silicon Carbide (SiC) technology over the years, particularly in terms of specific on-resistance R_{on,sp_diff} and blocking voltage capabilities. SiC devices, known for their superior performance in high voltage and high temperature applications, have shown a trend towards lower specific on-resistance, indicating improved efficiency with minimal power loss [117–119]. These advancements make SiC devices increasingly attractive for power electronics applications, where efficiency and high voltage handling are critical. The references provided offer detailed insights into these technological improvements, showcasing the continuous research and development efforts in the field of SiC power devices.

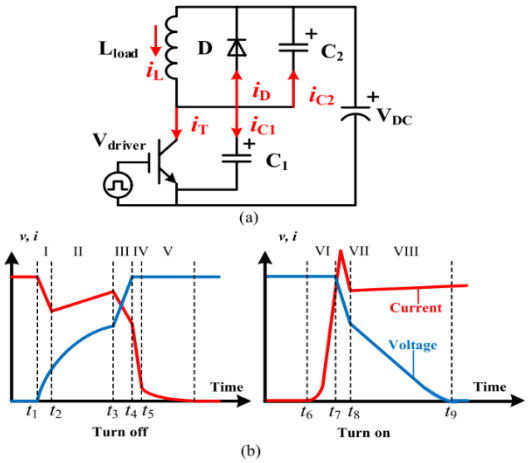


Figure 3.3 Circuit Diagram and Corresponding Waveforms for a Switching Device During Turn-Off and Turn-On Phases

3.2.2. Dynamic Characteristics

Silicon Carbide (SiC) Insulated Gate Bipolar Transistors (IGBTs) are predominantly utilised to drive inductive loads, such as motors and transformers, owing to their high efficiency and rapid switching capabilities. To thoroughly assess the switching characteristics of these power devices, the Double Pulse Test (DPT) is frequently employed. This test is instrumental in providing valuable insights into the dynamic performance of the device under realistic operating conditions. The DPT circuit and the associated switching waveforms of a SiC IGBT are depicted in Figure 3.3. In this configuration, components C_1 and C_2 represent the parasitic capacitances inherent in the circuit [120, 121]. These parasitic elements can significantly influence the switching behaviour and must be accounted for during the analysis.

The turn-off process of the SiC IGBT, as observed in the current waveform, can be segmented into five distinct phases. Initially, the current begins to decrease as the gate voltage is reduced, initiating the turn-off process. This is followed by an increase in the collector-emitter voltage as the current continues to fall. A tail current then persists due to the stored charge in the drift region, which gradually dissipates. Subsequently, the voltage across the device stabilises at its off-state value, and finally, the current reaches zero, indicating that the device is fully turned off. Similarly, the turn-on process can be divided into three phases. The gate voltage is increased, causing the collector-emitter voltage to drop as the device begins to conduct. The current through the device then increases rapidly as the voltage continues to fall. Finally, the voltage stabilises at its on-state value, and the current reaches its steady-state level. These phases are critical for understanding the switching dynamics of SiC IGBTs. A detailed analysis of these phases aids in optimising the gate drive circuits and enhancing the overall performance of the power electronic system [47, 122].

3.3. SiC IGBT model research

Silicon Carbide (SiC) Insulated Gate Bipolar Transistor (IGBT) devices are currently in the developmental stage and are not yet ready for large-scale commercialization. The application of these high-voltage and high-temperature devices faces several challenges, including immature packaging technologies (such as cooling and insulation), driver issues (like Electromagnetic Interference, EMI), and protection mechanisms against overvoltage, overcurrent (OC), and overheating (OT). For device manufacturers and circuit designers, having an appropriate SiC IGBT model is crucial. Such models help in understanding the working principles of these devices, optimising their structure, and predicting their performance under various conditions. In this context, all the SiC IGBT models developed for circuit simulators, as discussed in this article, are mathematical models. One of the most classical mathematical models is the Hefner IGBT model, which is based on semiconductor physics. This model primarily includes equivalent circuits of MOSFETs and employs ambipolar diffusion theory to explain the behaviour of bipolar transistors. Additionally, it incorporates the non-quasi-static effect and nonlinear capacitance effect to accurately analyse the transient processes [122, 123].

Table 3.2 provides a comprehensive overview of all SiC IGBT models developed since 2012. Over time, n-channel SiC IGBTs have increasingly replaced p-channel variants, leading to a shift in simulation models from p-channel to n-channel configurations. The first physical model of the non-punch-through (NPT) SiC IGBT was introduced in [57, 124]. This model's static and dynamic behaviours for p-channel SiC IGBTs, as well as the static behaviours for n-channel SiC IGBTs, were validated using Saber and PSpice simulations.

The developed model, which lacks a buffer layer and is fundamentally a Hefner model, cannot simulate SiC IGBT devices with buffer layers, which are now commonly used. Despite this limitation, the simple NPT structure allows for accurate simulation of static and turn-off behaviours. Another p-channel SiC IGBT model was also developed in [108, 109] and validated through numerical simulations. Unlike Hefner's base carrier distribution model, which relies on the ambipolar diffusion equation, this model employs a piecewise function to simulate the base carrier distribution, as illustrated in Fig. 3.7 (a). This abrupt carrier distribution enables the model to run simulations in SPICE3F5 400 times faster than numerical simulations [18], although it results in a three-slope voltage transition with moderate accuracy in the 2013 version [46, 106].

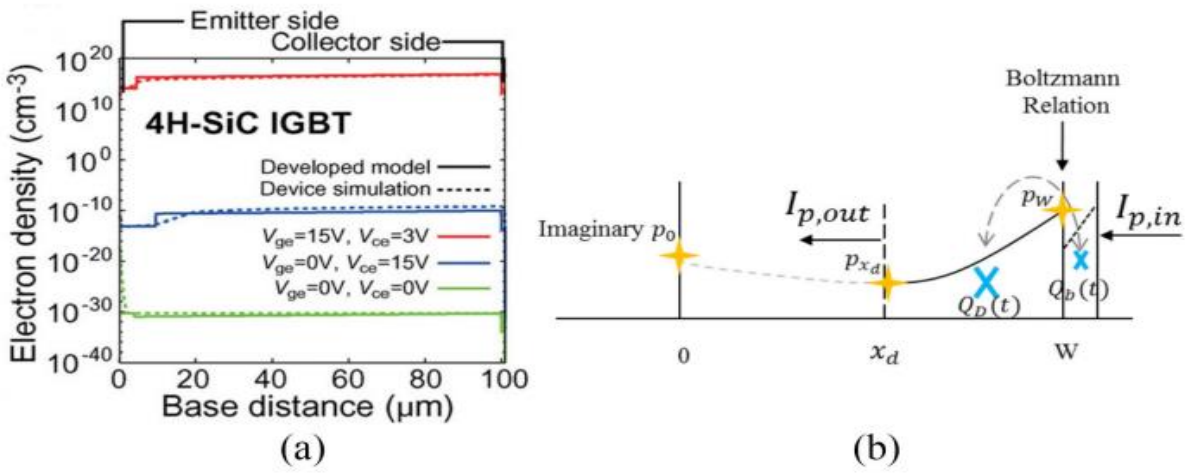


Figure 3.4 The carrier distributions in the base region are represented using (a) a piecewise function [17] and (b) an exponential function

In 2019, the model was further refined and validated under various temperature conditions. Enhancements included the incorporation of an interface traps model and temperature dependence models for intrinsic carrier density and carrier lifetime[122]. These improvements significantly boosted the model's accuracy and reliability.

The study presented in [20] significantly simplifies the Hefner IGBT model by utilising the drain current of the MOSFET (ID) and the current gain of the BJT (β) to calculate the collector current of the IGBT (IC). This simplification is expressed in equation (1). The primary contribution of this work is the development of an electrothermal model for SiC IGBTs, which combines a simplified electrical model with a three-dimensional finite-element-based thermal model. However, this electrothermal model does not account for the heavy injection effect and voltage drop, limiting its capability to simulate only the static characteristics of the device.

$$I_{c(\beta+1)}I_D \text{----------(3.3)}$$

In contrast, the research detailed in [21] extends the Hefner Si IGBT model, incorporating a buffer layer to adapt it for field-stop (FS) SiC IGBTs. By employing a parameter extraction software tool, the study extracts 20 physical and structural parameters from both static and dynamic waveforms [113]. This enhanced model can simulate the static characteristics of 12 kV, and 20 kV SiC IGBTs across various temperatures, as well as the turn-off process under different temperatures, voltages, and currents. It is important to note that there are noticeable discrepancies between the simulated and measured static curves, which may be attributed to inaccuracies in the fitting of static parameters. Additionally, the model's accuracy diminishes

when the SiC IGBT enters the punch-through state, particularly at low current levels. Therefore, to improve the accuracy of SiC IGBT models, it is essential to incorporate the unique punch-through effect when adapting Si models to SiC models. This model employs an exponential expression to represent carrier density distribution and uses linearization to describe temperature-dependent parameters. Consequently, parameters such as current, diffusion capacitance, threshold voltage, and the variation of transconductance with temperature are approximations, making the model's accuracy reliant on the fitting results. Despite these approximations, this model is notable for being the first to verify static, turn-on, and turn-off behaviours under varying temperatures and gate resistances [110].

In [23], a unified IGBT model for both Si/SiC and p/n-channel configurations is developed, building on the foundations laid by and the Hefner model. The validity of this unified model is confirmed through simulations of Si n-channel IGBTs and both n-channel and p-channel SiC IGBTs. Compared to the model in, this unified model offers more accurate simulations of static and turn-off processes, even with certain simplifications. For instance, in dc–dc–ac circuit simulations, a run of several hundred milliseconds in Saber is completed in just 0.0156 seconds, demonstrating the model's suitability for system-level simulations [125].

These physics-based mathematical models, which verify the characteristics of SiC IGBTs to some extent, have become valuable tools for circuit designers. However, models with high-accuracy static, turn-on, and turn-off characteristics are still lacking. The complex parameter extraction process poses a significant challenge for implementing these models in circuit simulators, especially under different temperature conditions. Additionally, improving compatibility with commercial simulators remains a crucial area for development. Therefore, modelling SiC IGBTs requires a balance between simulation accuracy and speed. The current trend is towards developing efficient SiC IGBT models, such as simplified physics-based models or high-accuracy behavioural models, to better predict the electrothermal behaviours of circuits [120, 126].

Table 3.2 Comparison of SiC IGBT Models: Achievements and Limitations (2012-2021)[127, 128]

Year	Device Type	Simulator	Achievement	Limitation
2012	15kV NPT p-channel	Saber & Pspice	First unified physical model	Limited to NPT structure
2013-2019	13kV FS p and n-channel	SPICE3F5	400 times faster than 2D numerical simulation	Neglect of transient experimental results under punch-through behaviour's

2013	1.2kV n-channel	Simulink	Integrated electro-thermal coupling model of different temperature, voltage and current	Low accuracy at low current levels
2014	12KV & 20kV FS n-channel	Saber	Fully prediction of static, turn-on and turn-off behaviours	Partial expression fitted by functions taken to simplify the model
2015	15kV FS n-channel	Simulink	Unified physical model of FS type Si, SiC, n, P IGBT	Approximation of experimental results under punch-through behaviours
2018	>12kV FS n and p-channel	Saber, HSpice, Spectre	Fully prediction of static, turn-on and turn-off behaviours	Approximation of experimental results under punch-through behaviours
2016	1200V, 300A all-SiC modules	Saber & Pspice	Improved performance at higher output currents	Immature fabrication technology and intrinsic defects
2021	Hybrid IGBTs with built-in 650V SiC Schottky barrier diodes	SPICE3F5	Ideal for automotive and industrial applications	
2021	SiC MOSFETs replacing Si IGBTs in EV inverters	Simulink	Up to 70% reduction in switching losses	

3.4. Challenges of SiC IGBT fabrication

Silicon Carbide Insulated Gate Bipolar Transistors (SiC IGBTs) are poised to revolutionise high voltage applications due to their superior theoretical advantages over traditional high voltage devices. Despite their potential, the commercialization of SiC IGBTs faces significant hurdles. These challenges include the fabrication of high-quality SiC n-IGBTs, insufficient operational lifetime, poor SiC/SiO_2 interface properties, and the lack of advanced high voltage, high temperature packaging solutions. Addressing these issues is crucial for unlocking the full potential of SiC IGBTs[47]. This section delves into the primary obstacles hindering SiC IGBT commercialization and explores the ongoing efforts to enhance their performance through optimised growth processes, innovative bulk structure designs, and advanced fabrication techniques.

3.4.1. Fabrication of n-Channel SiC IGBT

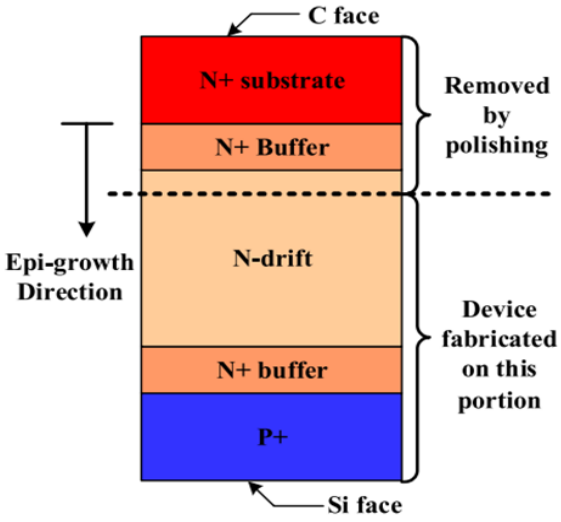


Figure 3.5 Inverted-growth process of free-standing technology

As mentioned above, n-channel SiC IGBT has greater advantages as a high voltage switch and becomes the main research focus. Unfortunately, n-channel SiC IGBT needs a high doping p-type collector as a hole-injection layer. However, in commercial p-type substrate, quality is poor, and resistivity is high (~2.5 Ω cm). The advantages of n-channel SiC IGBT are reduced. Therefore, free-standing technology was proposed by Wang and Cooper for the first time, as shown in Figure 3.5 [8]. The n- and p+ epilayers growing on n-type substrate serves as the drift region and supporting substrate/collector of n-channel SiC IGBT. After that, there are several research works of n-channel SiC IGBT based on free-standing, and the test results of these devices vary. Similar to Cooper's results, n-channel SiC IGBT fabricated by Chowdhury shows poor conductance modulation [129]. It may be attributed to the low injection efficiency due to the very thin and low doping concentration of the p-type collector. Compared with the p-type collector formed by epitaxy, that formed by ion implantation has a native disadvantage in injection efficiency. Although Yonezawa et al. obtained n-channel SiC IGBT with low $R_{on,sp,diff}$, their results showed that with the increase of device size, the $R_{on,sp,diff}$ showed a degradation trend . This phenomenon may be caused by the variation of carrier lifetime distribution. The p-type epilayer, used as supporting substrate, needs to be thick enough and high enough in doping concentration to ensure mechanical strength and low series parasitic resistance. However, in thick p-type epilayer, the doping concentration is limited by the formation of thin ohmic contacts, growth rate, surface roughness, and in-grown defects. In addition, it is very difficult to remove the n-type substrate due to the hardness and chemical

inertness of SiC. Complete separation of substrate, the carrier lifetime reduction and wafer bow, caused by removing substrate process, should be improved further as well. [130]

3.4.2. Defects and Lifetime Enhancement

The quality of silicon carbide (SiC) wafers is a critical factor that directly influences the performance, reliability, stability, and yield of SiC Insulated Gate Bipolar Transistor (IGBT) devices. This, in turn, indirectly impacts the overall cost of fabrication. Defects in SiC wafers can be broadly categorised into intrinsic material defects and structural defects. Intrinsic defects include electronic traps such as Z 1/2 and EH 6/7, while structural defects, often resulting from epitaxial growth processes, encompass issues like micropipes, threading dislocations, basal plane dislocations, 3C inclusions, and stacking faults (SF).

Micropipe density is a key metric used to grade the quality of SiC wafers. Currently, advancements in manufacturing have reduced the micropipe density to less than 3 cm^{-2}, with some wafers achieving densities as low as 0.1 cm^{-2}, effectively realising “zero micropipe” conditions. Additionally, other defects have been minimised to acceptable levels through optimised growth processes and post-growth treatments. These improvements have facilitated the commercialization of low-voltage 4H-SiC Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) devices [87, 131, 132]. However, for SiC IGBT devices, the presence of these defects, particularly as recombination centres, significantly reduces the carrier lifetime in the thick drift region. High-voltage SiC bipolar devices require a long carrier lifetime to minimise the forward voltage drop (V_f). The carrier lifetime is a crucial parameter that balances the trade-off between V_f and switching speed. Therefore, achieving a much longer carrier lifetime is essential for effective lifetime control in bipolar devices. The primary defects that reduce carrier lifetime, known as lifetime-killers, are Z 1/2 and EH 6/7, which are associated with carbon vacancies. Techniques such as carbon ion (C+) implantation followed by annealing, thermal oxidation and annealing, or optimization of growth conditions can significantly reduce the concentrations of these defects to very low levels, as low as 10^11 cm^{-3}. This reduction can result in carrier lifetimes exceeding 10 microseconds (μs), which is sufficient for high-voltage devices operating at several kilovolts (kV). However, for SiC IGBT devices with voltages exceeding 10 kV, the carrier lifetime achieved through these methods is still insufficient due to the extremely thick drift region required. In epitaxial layers with low Z1/2 concentrations, further advancements are necessary to meet the stringent requirements of these high-voltage applications.

3.4.3. SiC/SiO_2 Interface Properties

Silicon carbide (SiC) Insulated Gate Bipolar Transistors (IGBTs) exhibit superior performance compared to their silicon (Si) counterparts. However, the conventional use of silicon dioxide (SiO_2) as the gate dielectric introduces new challenges at the SiC/SiO_2 interface. While the native silicon dioxide layer on SiC can be readily formed in an oxidising environment at high temperatures, similar to the process for Si IGBTs, the oxidation process in SiC also generates additional carbon (C) clusters along with near-interface traps.

The trap density at the SiC/SiO_2 interface is significantly higher by one or two orders of magnitude than that at the Si/SiO_2 interface due to these extra carbon clusters. This high interface trap density, approximately $10^{13}\ cm^{-2}$, leads to a substantial reduction in the channel mobility of SiC Metal-Oxide-Semiconductor (MOS) structures. In contrast, the channel mobility in Si MOS structures is only reduced by a factor of two from its bulk mobility. The high density of interface traps (Dit) also causes several issues, including threshold voltage shifts, degradation of static and dynamic current amplitudes, increased turn-off current tails, and higher leakage currents in the blocking state. Introducing nitrogen during post-oxidation annealing (POA) is the most effective method to reduce Dit. After POA, the channel mobility can reach around 50 $cm^2/V{\cdot}s$. However, this process also introduces defects in the oxides, leading to reliability problems. To achieve a high-quality interface comparable to Si/SiO_2, it is essential to completely remove the remaining carbon atoms and near-interface traps [133].

Another significant issue is the high electric field in the oxide layer. According to Gauss's law, in 4H-SiC IGBTs, the electric field in SiO_2 is 2.5 times higher than in SiC. This is due to the higher critical electric field in SiC IGBTs compared to Si IGBTs, which results in a higher electric field in the SiO_2 layer. Many research efforts have focused on using dielectrics with high dielectric constants (high k) to replace SiO_2, aiming to reduce the electric field ratio between the gate dielectric and SiC. However, these new dielectrics often have poor interfaces with high densities of interface defects and larger leakage currents due to the lower band offset at the new dielectric/SiC interface. Although a stack structure combining SiO_2 and high-k dielectrics can reduce leakage currents and improve channel mobility to some extent, there are still challenges related to compatibility with existing mass manufacturing processes and ensuring long-term robustness under high-voltage operation.

3.4.4. Termination Technologies

Designing reliable and robust edge terminations is crucial for sustaining the high voltage requirements of silicon carbide (SiC) Insulated Gate Bipolar Transistor (IGBT) devices. These terminations are essential as they enable the device to support more than 90% of the bulk breakdown voltage. To date, the primary termination technologies applied to SiC IGBTs are Junction Termination Extension (JTE) and Field Limiting Rings (FLRs)[134].

JTE and FLR technologies play a vital role in managing the electric field at the edges of the device, which is critical for preventing premature breakdown. The terminations used in available SiC IGBT devices are summarised in various studies and figures[135–137]. To mitigate the crowded edge electric field effect, the termination length in SiC IGBTs is significantly longer than that in their silicon counterparts. Consequently, the termination area can account for more than 50% of the chip area, leading to an enlarged chip size and a suboptimal cost-to-area ratio[138]. Accurate control of implantation doses and significant area consumption are necessary for JTE technology to achieve a uniform electric field distribution. As a result, JTE technology is predominantly used in lower voltage devices. On the other hand, FLR technology is targeted at high voltage devices, although it also consumes a large area [139, 140].

To address the area consumption issue, advanced FLR technologies have been developed. These include linearly or regionally optimised distances between FLRs and the combination of JTE and FLR technologies. The former approach reduces the termination length by 30% and increases the breakdown voltage by 23%. The latter approach, which combines JTE and FLR technologies, reduces the termination area by 20% to 30% while achieving the same breakdown voltage. These advancements in termination technologies are crucial for enhancing the performance and efficiency of SiC IGBT devices, ensuring they can meet the stringent requirements of high voltage applications while maintaining a manageable cost-to-area ratio[141, 142].

3.5. SiC JFET

With the successful commercialization of SiC Schottky and JBS diodes, it became clear that SiC switching devices were also necessary to fully harness the potential of silicon carbide for high-power electronics. The wider bandgap of SiC compared to silicon results in a higher built-in voltage and a broader space charge region (SCR) in SiC p±n junctions than in silicon. This allows for the fabrication of normally-off SiC JFETs with a sufficiently thin channel that can

be fully depleted by the SCR at zero gate bias. Since the channel is located within the semiconductor, JFETs avoid issues related to oxide reliability and dielectric strength. Additionally, electrons in a JFET's channel should ideally exhibit low-field mobility close to that in a bulk crystal, as there is no surface or SiC/SiO_2 interface carrier scattering in these device[143–145].

The first 4H-SiC JFETs were introduced by P. Ivanov et al. in 1993[146]. These were normally-on devices featuring a buried p± gate and an n-channel layer (1.2 μm thick; 1.8×10^17 cm^{-3}) grown via sublimation epitaxy on 4H-SiC substrates, which were cut from a single crystal boule using the LETI method. The substrate surface was oriented parallel to the c-axis. The channel height was defined by reactive ion etching of the top n-layer. Devices with a gate length of 9 μm and a channel width of 0.7 mm operated at temperatures up to 400 °C and were characterised at currents up to 80 mA and voltages up to 60 V. The electron low-field mobility of 340 $cm^2/(V·s)$ was extracted from device characteristics at room temperature. In 2005, P. Sannuti et al. reported the electron mobility in JFETs with epitaxial channels oriented parallel to the basal plane[147]. They measured a channel mobility of 398 cm^2 (V·s) in lateral JFETs with a channel doping of $1×10^{17}$ cm^{-3}. Both mobility values (along and perpendicular to the c-axis) are comparable to the bulk electron mobility in 4H-SiC at this doping level (~400 $cm^2/(V·s)$).

The first power 4H-SiC JFETs were developed by H. Mitlehner et al. in 1999[148]. These vertical JFETs (VJFETs) featured a planar channel and were fabricated using selective aluminum implantation into a thick 4H-SiC drift layer to form a buried p+ gate, followed by a second epitaxy to grow a 2.5 μm high channel. These devices operated at currents up to 5 A and could block 1800 V at a gate-source voltage (VGS) of -20 V, with a specific on-resistance (RON-SP) of less than 15 mΩ·cm².In 2001, H. Onose et al. reported the first 4H-SiC power VJFETs with a vertical channel, which required VGS = -50 V to block 2000 V but had a higher RON-SP (~70 mΩ·cm²) due to defects from high-energy implantation. In 2003, J. Zhao et al. introduced 4H-SiC trenched and implanted VJFETs (TI-VJFETs) with gate p+ regions formed by ion implantation in the sidewalls of deep trenches. These devices demonstrated normally off operation with an RON-SP of 3.6 mΩ·cm² and a maximum blocking voltage (VBL) of 1726 V at VGS = 0 V[149]. The electron channel mobility was 561 cm²/(V·s), which is high for SiC JFETs but lower than the bulk electron mobility in 4H-SiC at the same doping level [78, 150].

TI-VJFETs saw significant development, and in 2008, Y. Li et al. reported normally-on devices with a blocking voltage (VBL) of 1650 V and a record low specific on-resistance (RON-SP) of 1.88 mΩ·cm². Around the same time, Semi South Laboratories, Inc. introduced both normally-on and normally-off SiC TI-VJFETs to the market. The normally off TI-VJFETs, designed for 800 V applications, demonstrated very low on-resistance. However, their commercialization faced challenges due to the unconventional and complex fabrication process, which is not compatible with the Double Diffused Metal Oxide Semiconductor (DMOS) processing used in silicon electronics [151, 152].

The performance of SiC JFETs is highly sensitive to the channel doping level, which must be precisely controlled. Each epi-wafer requires individual tuning during device processing based on its doping. Additionally, SiC JFETs need specially designed gate driving circuits, as the blocking voltage depends on the gate-source bias. Despite these challenges, normally-on SiC TI-VJFETs with ratings up to 1700 V/8 A/400 mΩ and 1200 V/120 A/9 mΩ are currently available from United Silicon Carbide, Inc.

Chapter 3 delves deeply into the world of SiC Power MOSFETs. It begins with an introductory overview, explaining the importance and relevance of these components in modern electronic applications. The chapter then outlines the principles of MOSFETs, elaborating on their function and mechanics. Next, it examines the equivalent circuit of an n-channel MOSFET, providing a clear understanding of its internal structure and behavior. The chapter also explores the theory of device breakdown, explaining the conditions and mechanisms that can lead to MOSFET failure. The classification of Power MOSFETs is discussed in detail, highlighting the different types and their specific characteristics. This includes an in-depth look at vertical power MOSFETs, D-MOSFETs, and U-MOSFETs, along with their unique advantages and applications.

The Next chapter focuses on Technology Computer-Aided Design (TCAD), highlighting its role in simulating and optimizing semiconductor devices. It introduces Sentaurus TCAD, explains the importance of meshing for accurate simulations, and presents SiC JFET simulations along with their results, showcasing TCAD's value in device development

4. Technology Computer-Aided Design (TCAD)

4.1. Introduction

The device simulation has played a crucial role in the development of semiconductor technology in terms of design, optimisation, characterisation and, most importantly, providing an insight into the carrier transport mechanisms by studying phenomena that cannot be directly analysed on real devices. The simulation process involves the implementation of numerical procedures in solving equations related to the physical model chosen to describe the transport process in a device. The complexity of the selected physical model and the related time taken to solve the model are two-fold issues to be seriously considered when selecting this simulation approach. However, with the continuous improvement of fast and powerful computational resources these limitations are greatly reduced resulting in more accurate, reliable and high-speed techniques.

Sentaurus developed by Synopsys Inc is a commercial physically based simulator that allows analysis and modelling of 1-D, 2-D, and 3-D semiconductor devices based on approximation models of carrier transport derived from Schrodinger or Boltzmann equation, and self-consistently coupled to Poisson's equation [1]. The Synopsys simulation tool is integrated with Virtual Wafer Fab (VWF) interactive tools for effective interactive run-time environment and scientific visualisation capabilities. This chapter provides an overview into a SiC JFET [154].

4.2. Sentaurus Technology Computer Aided Design

Technology Computer-Aided Design (TCAD) is a crucial tool in semiconductor technology, enabling the modelling of power semiconductor devices and integrated circuits (ICs), including their fabrication and device operation. The TCAD simulation process typically involves three main stages: process simulation, device simulation, and circuit simulation. In process simulation, the Sentaurus Process tool is used to model the physical effects of the fabrication process steps, such as oxidation, ion implantation, and diffusion, to generate the realistic device structure. Device simulation is performed using Sentaurus Device, which involves importing the device structure, defining relevant physical models, setting up boundary conditions, and executing the simulation to analyse the electrical characteristics. Finally, circuit simulation is conducted with Sentaurus Mixed Mode which combines device models and compact models to form a circuit and subsequently executes a simulation to obtain the behaviour of the device in a circuit configuration. Visualisation and analysis of the simulation results are carried out using the Sentaurus Visual tool, where data is imported, visualised, and analysed to evaluate

device and circuit performance. By following these steps, Sentaurus TCAD effectively simulates semiconductor devices and circuits, leveraging the advantages of computer-aided simulations to complement experimental investigations and optimise device designs [130].

The software suite also includes various interactive tools such as Sentaurus Workbench, and Sentaurus Structure Editor, which enhance its capability as a device simulation package. These tools facilitate the creation and editing of device structures. By integrating these functionalities, Sentaurus TCAD provides a robust platform for simulating and optimising power semiconductor devices and circuits [155–157].

4.3. Meshing for TCAD Simulations

TCAD is a finite element method and hence in order to simulate a power semiconductor device a mesh is required. For an accurate description of the device geometry the mesh definition plays a crucial role in specifying nodes in a device structure for numerical simulations. The computational time required to derive a solution of a linear system resulting from the discretization of partial differential equations on a mesh with (N) nodes is proportional to (N^{β}), where (β) ranges from 2 to 3. A mesh size should be smaller than the Debye length to resolve charge variations in space accurately. A poor mesh can lead to convergence errors/failure, inaccurate simulation results, and increased computational time. Therefore, a refined mesh should be specified at the channel junctions, electrodes, and any region containing high electric fields, abrupt doping, or concentration profiles. Hence the mesh configuration should be fully optimised for numerical efficiency [158, 159].

Sentaurus TCAD employs the finite element method by subdividing the simulation domain into smaller regions, usually of triangular or tetrahedral shape, and estimates the dependent variable in the subregion using polynomial approximation. Sentaurus allows mesh specification for 2-D and 3-D device geometries. The software includes tools like Sentaurus Structure Editor for creating and editing mesh structures. In 2-D rectangular geometry, the mesh is defined using X and Y spacings, while in cylindrical 2-D geometry, the radial and angular mesh spacings are specified. These capabilities ensure that Sentaurus TCAD can effectively handle complex device structures with optimised mesh configurations [19, 81, 160].

4.4. SiC JFET Simulations

Silicon Carbide (SiC) Junction Field-Effect Transistors (JFETs) have been of interest due to the fact that they completely avoid the reliability issues associated with the SiC MOS channel. These types are typically co-packaged with silicon devices with robust MOS channel, enabling robust devices which made from these two key parts. The SiC JFET devices offer significant advantages over traditional silicon-based power devices, including higher breakdown voltage, lower on-resistance, and improved thermal stability[161]. To optimise the design and performance of SiC JFETs, accurate simulations are essential[162, 163].

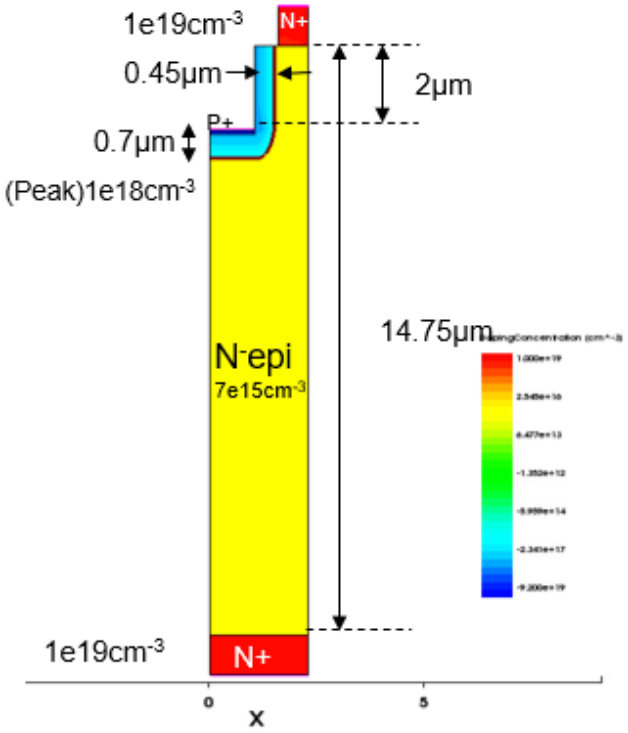


Figure 4.1 SiC JFET diagram for use in the TCAD Simulation

The figure 4.1: showcases a cross-sectional view of a SiC JFET, a type of semiconductor device renowned for its exceptional performance in demanding applications. Key components include the N-epi channel, N+ source and drain regions, and the P+ gate region. The design parameters, such as channel length (2 µm), doping concentrations in the N-epi layer (7e15 cm^{-3}), N+ regions (1e19 cm^{-3}), and P+ gate region (1e19 cm^{-3}), and gate geometry (gate length, gate-source, and gate-drain distances) play a critical role in determining the device's electrical and thermal performance.

The channel length of 2 µm represents a balance between speed and breakdown. Shorter channels generally lead to faster switching speeds but can increase the risk of breakdown. A

channel length of 2 µm likely provides an optimized value that achieves a good combination of speed and breakdown voltage.

The N-epi layer thickness of 14.75 µm is chosen to ensure sufficient thickness for breakdown voltage while minimizing parasitic resistance. A thicker layer provides a larger depletion region, which helps prevent breakdown, but excessive thickness can increase the parasitic resistance of the device. High doping concentrations in the N+ source and drain regions (1e19 cm^{-3}) are essential for low contact resistance and high current carrying capacity. In contrast, the lower doping concentration in the N-epi layer (7e15 cm^{-3}) is crucial for controlling channel current and minimizing leakage current. The P+ gate region also has a high doping concentration (1e19 cm-3) to ensure strong gate control and low gate resistance. The gate geometry, including gate length, gate-source, and gate-drain distances, significantly influences the device's transconductance, switching speed, and noise performance. The specific values for these parameters are chosen depending on the literature to optimize these characteristic[164, 165].

4.4.1. SiC JFET Simulation Results

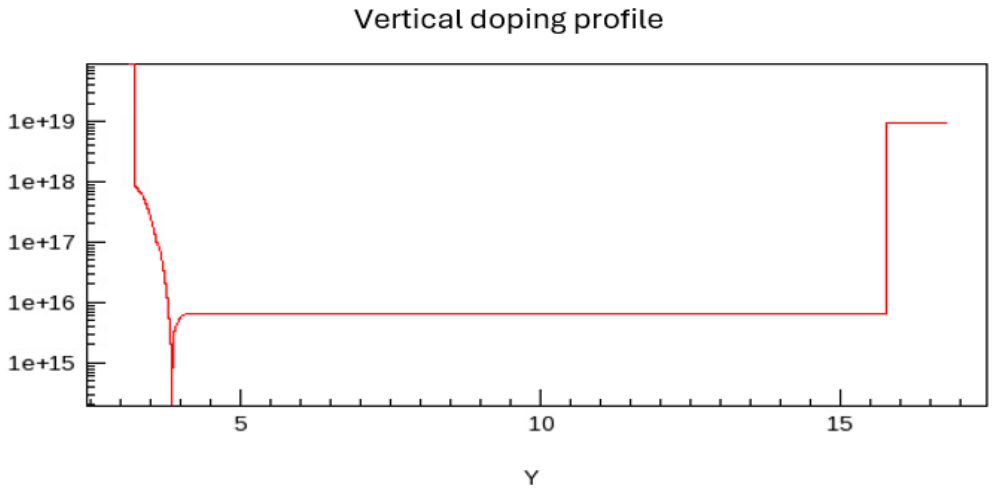


Figure 4.2 The vertical doping profile of the SiC JFET

The target was a high voltage SiC JFET attaining at least 1.2kV. The basic structure with key dimensions is shown in figure 4.1. The basic structure was developed from basic calculations and papers[166–168]. The structure shows an N-epi layer of 14.75µm. The vertical doping profile of the SiC JFET device, as shown in figure 4.1. shows the distinct regions of the device, each playing a vital role. The heavily doped source and drain regions, with a concentration of about 1e19 cm^{-3}, correspond to the N+ source and drain contacts, ensuring low-resistance connections. The channel, represented by the N-epi layer, shows a lighter doping concentration

around 7e15 cm^{-3}, facilitating controlled current flow. The P gate region, is moderately doped with around 1e18 cm^{-3}, effectively controls the current flow between the source and drain.

The abrupt junctions between these regions are notable, as they are crucial for efficient device operation. However, the sharp peaks observed in the doping profile, likely at the interfaces between the N+ source/drain regions and the N-epi channel, could indicate potential non-dualities. These peaks might introduce localised electric fields or defects, potentially degrading device performance.

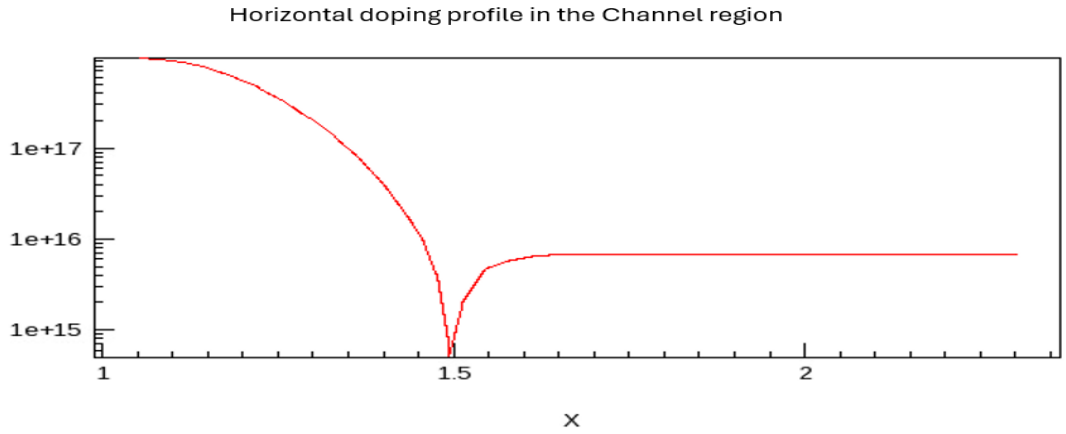


Figure 4.3 The horizontal doping profile in the channel region of the SiC JFET

The provided figure 4.3 illustrates a horizontal doping profile within the SiC JFET channel region. The profile exhibits a non-uniform doping distribution, with a high concentration near the P-gate side (approximately 1e18 cm^{-3}) that gradually decreases towards the N-drift region, stabilizing at around 7e15 cm^{-3}. This carefully engineered doping gradient serves several critical purposes. The high doping near the P-gate facilitates the formation of a depletion region under reverse bias, enabling effective control over current flow. The gradual decrease in doping ensures a smooth transition in the electric field, minimizing the risk of localized high-field regions that could lead to premature breakdown. Furthermore, the controlled doping profile influences the device's on-resistance and transconductance, critical parameters for performance optimization. .

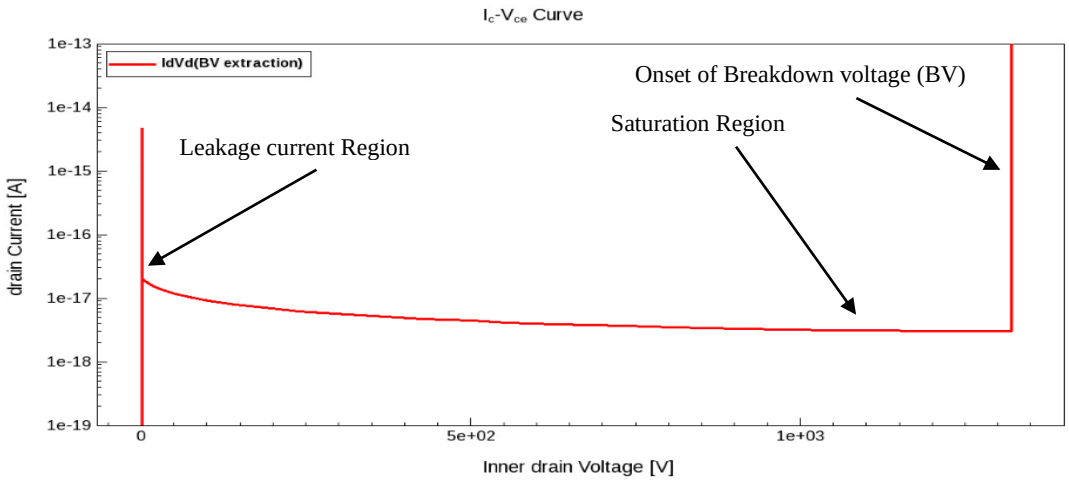


Figure 4.4 Breakdown voltage characteristics of the SiC JFET device

The figure 4.4 illustrates the breakdown voltage characteristics, by showing the relationship between the drain current and the drain voltage of the SiC JFET. It shows a sharp increase in drain current at the breakdown voltage of ~1.3 kV, which is slightly greater than the target voltage of 1.2 kV. Before reaching the breakdown voltage, the drain current remains low and relatively constant, representing the leakage current of the device. Beyond the breakdown voltage, the significant rise in drain current indicates the catastrophic failure of the device. The breakdown voltage is a crucial parameter for power devices like SiC JFETs. As Well as the breakdown voltage, the leakage current is also an important parameter, as it reflects the current flowing through the device when it is not actively conducting, hence a lower leakage current is preferred, as it reduces power dissipation.

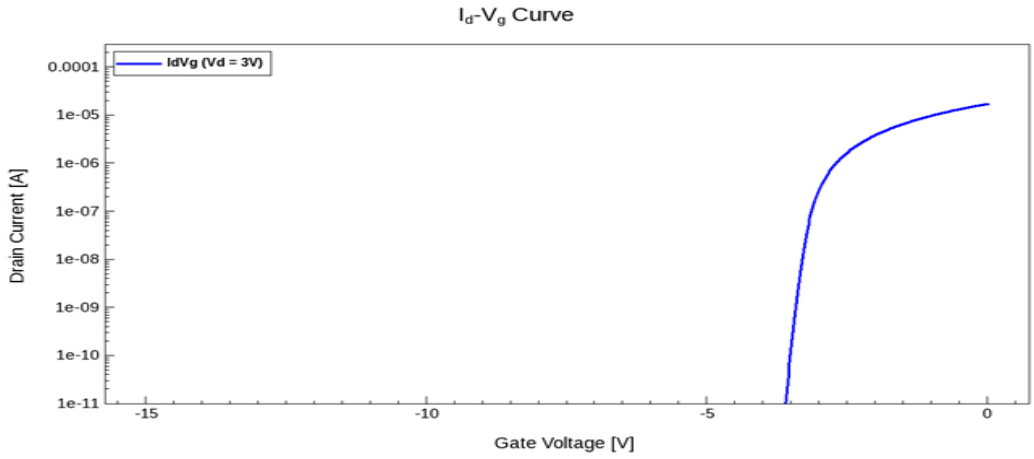


Figure 4.5 The transfer characteristics of the SiC JFET

The figure 4.5 represents the transfer characteristics of the SiC JFET, showing the relationship between the drain current (Id) and the gate voltage (Vg) of the device at a constant drain voltage (V_d = 3V). The transfer characteristics show that this device is normally on (depletion mode) device, because at a gate voltage of 0V there is reasonable drain current. The figure 4.5 shows

a sharp increase in drain current at a ~-3.5Ve, which is the threshold voltage (V_{th}). Below the threshold voltage, the drain current is negligible. The threshold voltage, where the drain current is zero, is known as the gate-to-source cutoff voltage. Above the threshold voltage the drain current gradually increases with rising gate voltage. The drain current rises rapidly and then stabilise at a constant value. The threshold voltage is crucial for JFETs as it determines the gate voltage required to turn the device on and control the drain current.

These output characteristics reveal how the drain current varies with the drain voltage for different gate voltages. At lower drain voltages, the curves appear almost linear, indicating the linear region where the JFET functions as a voltage-controlled resistor. As the drain voltage rises, the drain current reaches a plateau, marking the saturation region where the JFET acts as a current source. The point where the drain current starts to plateau is known as the pinch-off point, occurring when the depletion region extends across the entire channel, effectively pinching off the current flow.

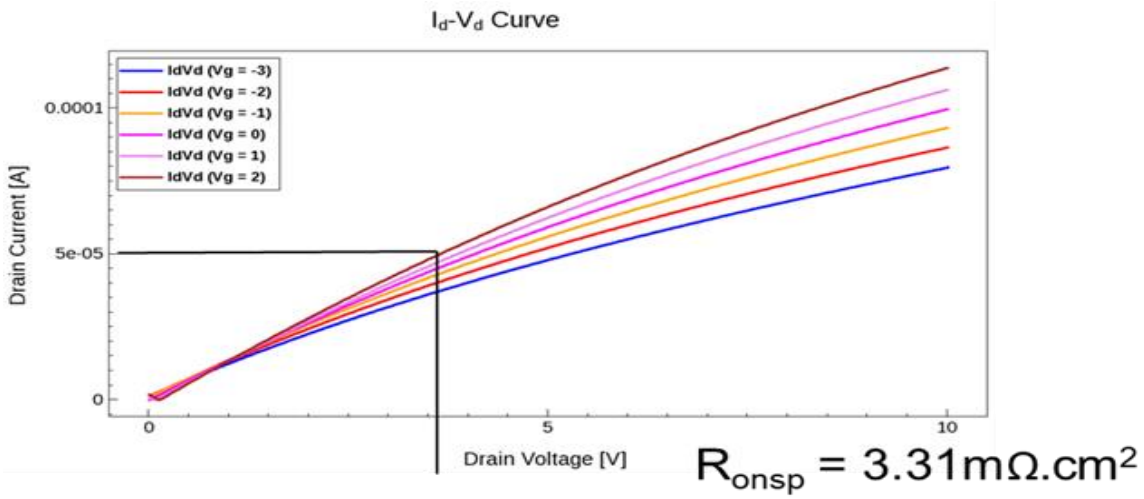


Figure 4.6 The plot illustrates the relationship between the drain current (I_d) and the drain voltage (V_d) of the SiC JFET device at various gate voltages (Vg).

The above figure 4.6 demonstrate the gate voltage effect, where more negative gate voltages shift the pinch-off point to lower drain voltages, resulting in reduced drain currents. This shows the gate's control over the channel conductivity. The designed SiC JFET device achieved a value of 3.31 $m\Omega.cm^2$ which is comparable to state-of-the-art devices. For example, a 1kV device [143]achieved a $1.3m\Omega \cdot cm^2$. This device had a lower breakdown voltage (350V less) and had shorter drift region length as well as a tapered design. A lower R_{onsp} is critical for lower conduction losses and hence efficient power electronics applications. The output characteristics provide valuable insights into the JFET's performance.

4.5. Summary

In this section of the thesis, we demonstrated the simulation of a high voltage silicon carbide JFET device. The device was designed for 1.2kV and achieved a breakdown voltage of 1.35kV with an excellent on state resistance of 3.31 $m\Omega.cm^2$. As shown in this section TCAD simulations were used to optimise the doping profiles for the device design. As well as this the breakdown characteristics, transfer characteristics and the on-state state characteristics.

Chapter 4 explores the application of Technology Computer-Aided Design (TCAD) in simulating and optimizing SiC power devices, with a particular focus on SiC JFETs. It discusses the utility of TCAD tools like Sentaurus TCAD in providing detailed insights into device behaviour and performance. The chapter examines the structural and doping profiles of SiC JFETs, highlighting their impact on device operation. The analysis includes an evaluation of key performance metrics such as breakdown voltage, transfer characteristics, and the relationship between drain current and drain voltage at various gate voltages. These simulations provide a comprehensive understanding of the internal dynamics and operational parameters of SiC JFETs.

Chapter 5 examines an existing SiC MOSFET power device, focusing on SEM and EDX spectrum analysis to assess surface properties and material composition. It also investigates MOS channel degradation through power cycling tests, providing insights into device reliability and performance.

4.6. Appendix 1

Appendix 1 provides a synopsis of the JFET model utilized for simulations with the Sentaurus TCAD tool

5. Analysis of an existing SiC MOSFET Power device

5.1. Introduction

As part of this study, it was decided to explore existing commercially available SiC Power MOSFETs. The objective was to understand construction of these devices and try to gain insights into MOS channel construction and study how they degrade overtime. Due to some unforeseen circumstances not also aspects of this work could be achieved however some progress was made to access commercially available SiC semiconductor MOSFET die and undertake certain analysis.

The device chosen for this work was a 900V device manufactured by the leading supplier of silicon carbide wafers and devices; Wolfspeed. The device was the C3M0065090J [118, 163] (see figure 5.1a) which is a Silicon Carbide MOSFET developed by Wolfspeed for high-efficiency power applications. This device is part of Wolfspeed's C3M family, known for their high efficiency and robust performance in demanding applications. SiC MOSFETs, such as the C3M0065090J, offer superior properties compared to traditional silicon-based devices, including higher breakdown voltage, lower on-resistance, and faster switching speeds. The C3M0065090J is rated for a maximum drain-source voltage of 900 V and a continuous drain current of 36 A at 25°C, with a low on-resistance of 65 mΩ, which helps reduce conduction losses and improve overall efficiency [123, 169, 170]. It comes in a TO-263-7 package, designed for efficient thermal management and ease of integration into power circuits.

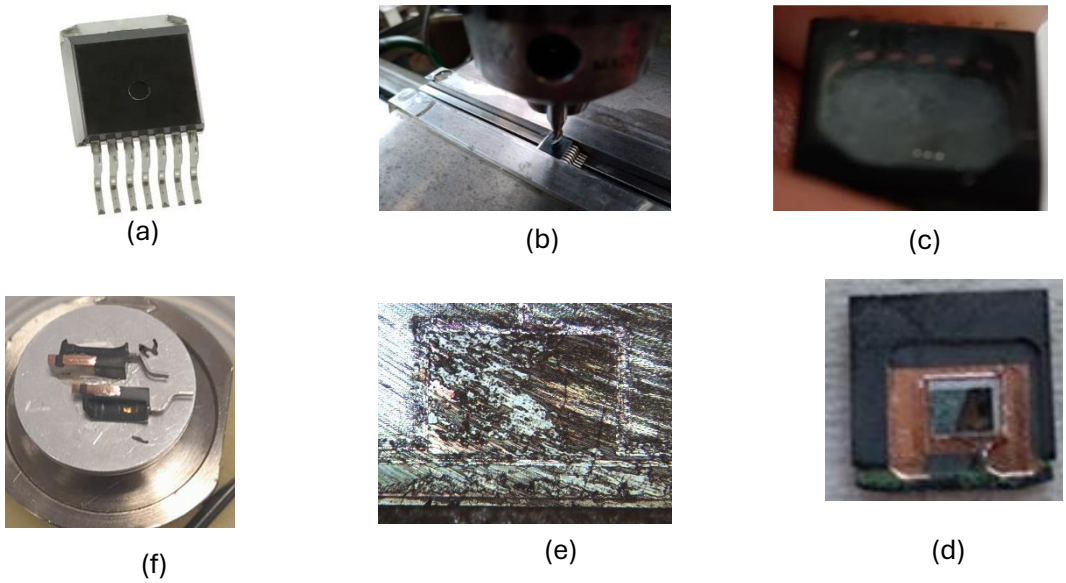


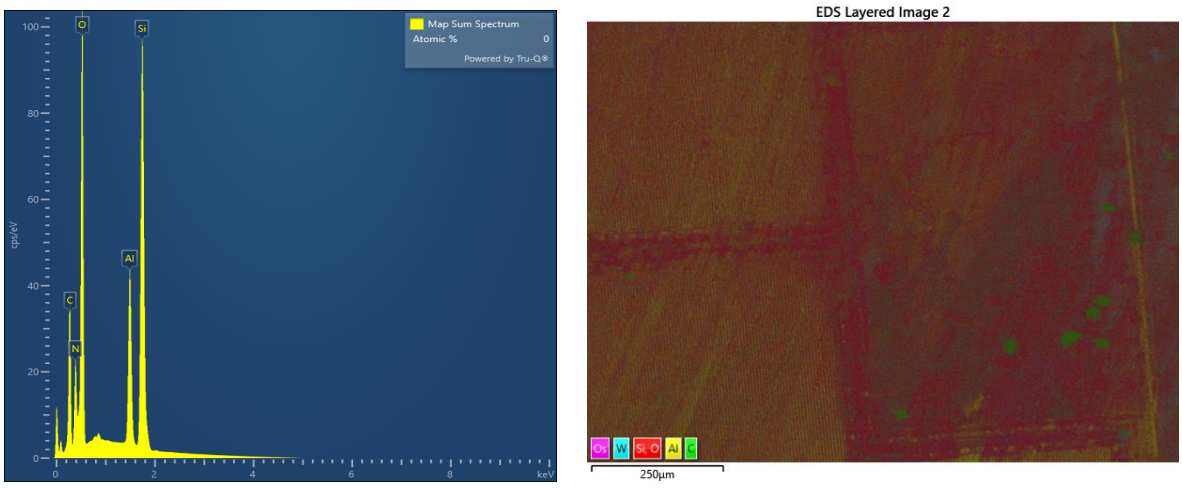
Figure 5.1 (a) C3M0065090J Silicon Carbide (SiC) MOSFET (b)Mechanically drilling the MOSFET to reach the gate (c)overview after drilling (d)Chemically cleaned MOSFET (e)Optical image of Surface (f) diced SiC Sample prepared for cross sectional SEM analysis

The MOSFET includes a fast intrinsic diode with low reverse recovery charge (Qrr), minimising switching losses and enhancing efficiency in high-frequency applications. With a low output capacitance (C_{oss}) of 60 pF, it supports fast switching capabilities. The device is also halogen-free and RoHS compliant, making it environmentally friendly. Key features include high blocking voltage, low on-resistance, fast switching, effective thermal management, and a wide creepage distance of approximately 7 mm between drain and source, enhancing safety and reliability. The C3M0065090J is ideal for use in power supplies, motor drives, solar inverters, electric vehicle (EV) chargers, and industrial power converters [88].

To begin my investigation into the internal structure of the C3M0065090J Silicon Carbide (SiC) MOSFET, I first approached the task by carefully examining the exterior of the device. Recognizing the need to access the internal components, the outer plastic packaging was mechanically milled through carefully. This step required precision to avoid damaging the internal semiconductor device. Once the plastic casing was successfully removed, it was cleaned using appropriate chemical solvents. This cleaning process was essential to eliminate any residual debris or contaminants that could interfere with subsequent analysis.

With the internal components now accessible and clean, a Scanning Electron Microscopy (SEM) was used to conduct a detailed examination of the surface features. SEM was chosen for its ability to provide high-resolution images, allowing for an in-depth analysis of the SiC material and the MOSFET's features [171]. It was initially planned to try to get a cross-sectional view through using focussed ion beam (FIB) milling, however the equipment at the University of York was not functional and not accessible from other sites either. So, the main focus was to use SEM. Through this method, I was able to observe the intricate details of the device, identify any potential defects, and gain valuable insights into the overall quality and performance of the SiC MOSFET.

5.1.1. Energy Dispersive X-ray (EDX) spectrum of the surface



(a) (b)

Figure 5.2 (a) EDX Spectrum of the Surface(b) EDX Layered image of the surface

This figure 5.2 displays the energy dispersive X-ray (EDX) spectrum, which provides information about the elemental composition of the sample. The vertical axis represents the intensity of the X-ray signal, while the horizontal axis represents the energy of the X-rays. Each peak in the spectrum corresponds to a specific element present in the sample. The EDX spectrum for the examined area of figure 5.2b is shown in 5.2a. The key observations from the spectrum include prominent peaks for aluminium (Al) and silicon (Si), indicating these are the major elements present, while smaller peaks for oxygen (O) and carbon (C) suggest some degree of surface oxidation and contamination due the sample being exposed after the milling process. Aluminium is normally found in the metallization layers in the device and in this case could be from the source regions next to the gate. The strong Si signal could also be emanating from the gate polysilicon layer as the gate contact region was being explored. Both C and Si are expected from the SiC itself also.

Additionally, the EDX layered image is a colour-coded map (figure 5.2b) visualising the distribution of different elements across the sample surface, with red representing oxygen (O), green representing carbon (C), and yellow representing aluminium (Al). The image shows the distribution of these elements, with yellow regions indicating higher concentrations of aluminium, and red and green regions indicating higher concentrations of oxygen and carbon, respectively. The variations in colour across the image suggest some degree of heterogeneity in the surface composition, which could be due to factors like surface roughness,

contamination, but principally due to the structure of the SiC MOSFET and the different regions covered by different materials.

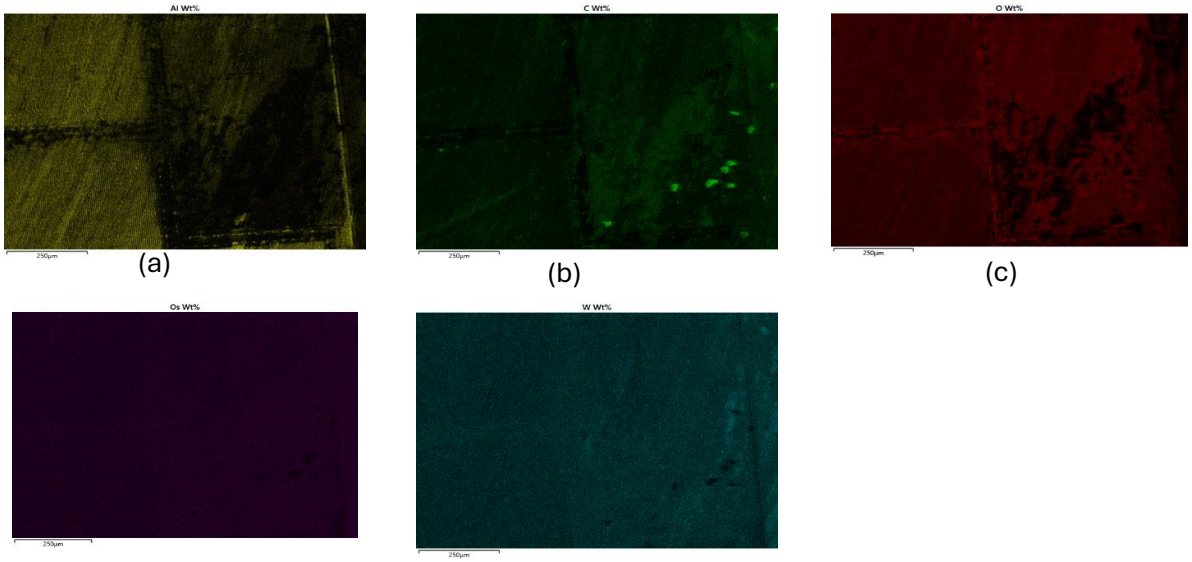


Figure 5.3 EDX images of EDX images (a) Al (b) C (c) O (d) Os (e)W

According to the Figure 5.3 : the EDX images offer a detailed view of the elemental composition of the C3M0065090J SiC MOSFET surface, with colour-coded maps illustrating the distribution of various elements. In (a) it shows the Al clearly as the source metal. The detection of carbon (C) in (b) clearly shows surface contamination possibly from after the milling or during handling, or after environmental exposure. From the oxygen view (shown in c), it is clear that those regions where the carbon was dense shows lower levels of O. So, the carbon could be covering certain regions of the oxidised surface of the gate areas. Notably, tungsten (W) is present, often used in high-temperature applications for its thermal stability, possibly as a protective coating or a manufacturing remnant. However, in this case it maybe that the drill bit used during the milling itself caused this very uniform covering across its entire surface[172].

In summary the EDX spectrum provides quantitative data on the relative abundance of each element, useful for assessing contamination levels or coating effectiveness. The layered image combines individual elemental maps for a comprehensive surface composition overview, aiding in identifying areas of interest and anomalies. Overall, the EDX images indicate that the MOSFET surface is mainly composed of silicon carbide, with some contamination and a potential tungsten from the milling process [97, [173]

Chapter 5 provides a comprehensive analysis of an existing SiC MOSFET power device, focusing on its structural, material, and operational characteristics. The chapter begins with SEM (Scanning Electron Microscopy) analysis, offering detailed insights into the surface morphology of the device. Complementing this, the Energy Dispersive X-ray (EDX) spectrum analysis reveals the elemental composition of the surface, helping to understand the material properties critical to device performance.

Chapter 6 delves into the processes involved in the fabrication of SiC MOS devices, providing a detailed exploration of materials, techniques, and methodologies. It begins with an overview of different types of SiC wafers, including 4H-SiC with epitaxial layers and 3C-SiC wafers, followed by key preparatory steps like wafer dicing and cleaning processes.

The chapter also covers the fabrication of MOS capacitors (MOSCAPs), focusing on techniques such as Atomic Layer Deposition (ALD) for gate oxide formation and Magnetron Sputtering for material deposition. Additionally, the annealing process is discussed as a critical step in enhancing device properties. This chapter provides an in-depth understanding of the intricate processes required to fabricate high-performance SiC MOS devices.

6. SiC MOS device Fabrication

6.1. SiC Wafer

Selecting the right Silicon Carbide (SiC) wafer for power electronic devices involves several key considerations. Firstly, the type and polytype of the wafer are crucial. The 4H-SiC polytype is often preferred for power electronics due to its superior electron mobility and wider bandgap, which translate to higher efficiency and performance[174]. In contrast, the 6H-SiC polytype, with its higher hole mobility and slightly narrower bandgap, is used in high-temperature and high-frequency devices. The wafer diameter is another important factor, with common sizes being 100 mm, 150 mm, and 200 mm. Larger diameters are preferred for higher yield and cost efficiency. Additionally, the doping and resistivity of the wafer play a significant role. N-type wafers, typically doped with nitrogen, offer low resistivity and high conductivity, while P-type wafers are used in specific applications requiring different electrical characteristics. Low defect density is essential for high-performance devices, with parameters like micropipe density and dislocation density needing to be minimised[175–178]. Thermal properties, such as high thermal conductivity and low thermal expansion, are vital for efficient heat dissipation and thermal stability. Lastly, surface quality, including surface roughness and flatness, impacts device performance, with high-quality wafers having minimal surface defects and high homogeneity [140]. SiC wafers possess several advantageous properties that make them suitable for power electronics. They have high thermal conductivity, which enables efficient heat dissipation, crucial for high-power applications. Their wide bandgap allows for operation at higher voltages and temperatures, improving efficiency and performance. SiC wafers also have a high breakdown voltage, supporting high-voltage applications without breakdown. Additionally, they exhibit excellent mechanical strength, ensuring durability and reliability, and are resistant to chemical corrosion, making them suitable for harsh environments [179].

The development of SiC wafers has seen significant advancements over time. In the early 1990s, the first commercial single-crystal SiC wafers were introduced. By the 2000s, wafer diameters increased from 100 mm to 150 mm, improving yield and reducing costs [180]. In recent years, the development of 200 mm wafers has further enhanced production efficiency and device performance. Recent updates include the mass production of 200 mm SiC wafers by companies like SICC (China), enhancing their availability for automotive applications.

6.2.4H-SiC With Epi Layer wafer

The wafer is of the 4H-SiC polytype, known for its superior electron mobility and wider bandgap, making it ideal for high-power and high-frequency applications. The wafer is 4 degrees off-axis, which helps in reducing defects during epitaxial growth and improving the quality of the epitaxial layers. It has a resistivity range of 0.015 to 0.028 ohm cm, ensuring good conductivity essential for power electronic devices. The wafer has Ultra-Low Micropipe density as well as double-side polished by chemical mechanical polishing, ensuring a smooth and defect-free surface on both sides of the wafer. The wafer also features two epitaxial layers: the first layer is N-type buffer layer with a doping concentration of 1.0 x 10^{1} cm^{-3} and a thickness of 1.0 µm, providing a thin, highly conductive layer; the second layer is also N-type with a doping concentration of 7.0 x 10^{15} cm^{-3} (± 20%) and a thickness of 16 µm (± 10%). This wafer specification was very similar to the characteristics used for the TCAD simulation of the SiC JFET device in the earlier chapter. This combination of specifications makes this wafer well-suited for high-performance power electronic applications, as well as providing a foundation for creating advanced MOS channels with different dielectrics.

6.3.3C-SiC wafer

3C-SiC is another important SiC polytype. The SiC epitaxial film was grown using PECVD, features a 3C structure with a thickness of 1.0 µm (±10%) and is oriented along the 3C-SiC (111) plane. The surface is chemically mechanically polished (CMP) to achieve a roughness (Ra) of less than 10 Angstroms. This N-type film exhibits a surface defect density of ≤3E3 cm^{2}, as determined by microscopic inspection of crystallites and other macro-defects. The total thickness variation (TTV) ranges from 5 to 29 µm, and the bow is between 9 and 3 µm. The underlying silicon substrate measures 10 x 10 x 1.0 mm is oriented along the (111) plane and is N-type with P doping. It has a resistivity of 1-10 Ω.cm and is optically polished on both sides.

6.3.1. Wafer Dicing

The wafer dicing process involves using a highly precise machine known as an automated dicing saw, specifically the **Disco DAD3221**. This machine operates similarly to a high-end chop saw, but with much greater precision. The blades used in this process are resin-impregnated with 450 nm diamond particles. As the blade cuts through the wafer, the resin wears away, continuously exposing fresh abrasive diamond particles, ensuring a consistent and effective cutting action.

To begin, the entire wafer is mounted onto a circular frame using dicing tape. This tape is specially designed with a precise thickness and adhesive level to securely hold the wafer and the resulting chips during the dicing process, while also allowing for easy removal of the chips afterward without leaving any residue. Once the wafer is mounted on the frame, the frame is loaded onto the dicer's stage. Using the machine's software, the size and thickness of the wafer, as well as the size and location of the chips, are defined. The dicer then follows these instructions to accurately cut the wafer into the desired chip sizes.

6.4. Wafer cleaning Process

Cleaning Silicon Carbide wafers is a crucial step in the fabrication of high-quality Metal-Oxide-Semiconductor (MOS) devices. The presence of contaminants such as organic residues, metallic particles, and native oxides can significantly impact the performance and reliability of these devices. Therefore, a thorough and systematic cleaning process is essential to prepare the wafer surface for subsequent fabrication steps. The cleaning process involves multiple stages, each designed to address specific types of contaminants and surface conditions. From degreasing to remove organic contaminants, to deoxidizing for eliminating native oxides, and advanced techniques like RCA and ultrasonic cleaning, each step plays a vital role in ensuring the wafer surface is pristine.

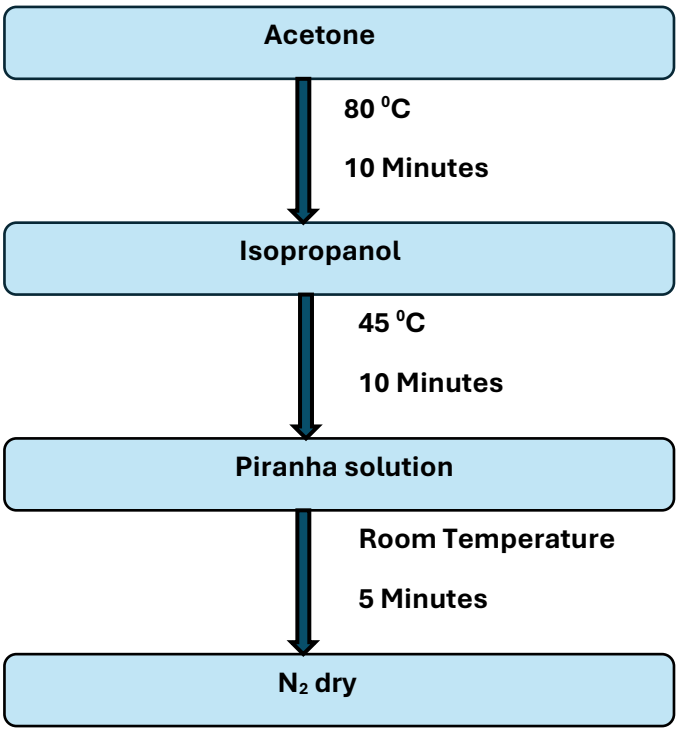


Figure 6.1 SiC wafer Cleaning Process[181]

This provides an overview of the various cleaning methods employed to achieve the high level of cleanliness required for optimal MOS device performance. By understanding and implementing these cleaning processes, researchers and engineers can enhance the quality and efficiency of their SiC-based power electronic devices [145]. Degreasing is the initial step in cleaning SiC wafers, aimed at removing organic contaminants such as oils, greases, and residues from the wafer surface. This process typically involves immersing the wafers in organic solvents like acetone or isopropanol. Ultrasonic agitation is often employed to enhance the removal of these contaminants. The ultrasonic waves create cavitation bubbles in the solvent, which implode and generate localised high-energy jets that dislodge and remove the organic residues from the wafer surface [182]. This step is crucial as it ensures that subsequent cleaning processes are more effective by eliminating the bulk of organic contaminants early on. Deoxidizing is a critical step that involves the removal of native oxides from the SiC wafer surface. Native oxides can form naturally when the wafer is exposed to air, and their presence can interfere with the performance of the MOS device. The wafers are typically treated with hydrofluoric acid (HF) to etch away the oxide layer. This process creates a hydrophobic surface, which is more conducive to the removal of other contaminants in subsequent cleaning steps. The deoxidizing step is essential for preparing the wafer surface for high-quality epitaxial growth and ensuring the integrity of the MOS device. Rinsing is performed to remove any residual chemicals from the wafer surface after the deoxidizing step. High-purity deionized water is used to rinse the wafers thoroughly. This step is crucial to ensure that no chemical residues remain on the wafer surface, which could potentially cause defects or interfere with the performance of the MOS device. The use of deionized water is important as it prevents the introduction of additional contaminants during the rinsing process. Drying is an important step to prevent water spots and contamination from drying residues on the wafer surface. After rinsing, the wafers are dried using methods such as nitrogen blow drying or spin drying. Nitrogen blow drying involves directing a stream of nitrogen gas over the wafer surface to remove water droplets, while spin drying uses centrifugal force to fling water off the wafer surface. Proper drying ensures that the wafer surface remains clean and free of contaminants, which is essential for high-quality device fabrication.

The RCA cleaning process is a widely used method for removing organic residues, metallic contaminants, and particles from the wafer surface. It consists of two main steps: SC-1 clean and SC-2 clean. The SC-1 clean involves immersing the wafers in a mixture of deionized water, hydrogen peroxide (H_2O_2), and ammonium hydroxide (NH_4OH) at elevated temperatures

(75°C to 85°C) for 5 to 15 minutes. This step effectively removes organic residues and particles. The SC-2 clean involves a mixture of deionized water, hydrogen peroxide, and hydrochloric acid (HCl) at similar temperatures, which removes metallic contaminants. The RCA cleaning process is essential for achieving a high level of cleanliness on the wafer surface, which is critical for the performance and reliability of the MOS device [145, 146]. Ultrasonic cleaning is used to remove particles and molecular contaminants from the wafer surface. In this process, the wafers are placed in an ultrasonic bath containing a solution of water, ultrasonic cleansers, and surfactants. Ultrasonic waves generate cavitation bubbles in the solution, which implode and create high-energy jets that dislodge particles from the wafer surface. This method is highly effective in removing fine particles and ensuring a clean surface for device fabrication. Ultrasonic cleaning is particularly useful for removing contaminants that are difficult to eliminate through other cleaning methods. Proper cleaning of SiC wafers is essential to achieve high-quality MOS devices. Contaminants such as organic residues, metallic particles, and native oxides can introduce defects and degrade the electrical properties of the devices. By following a thorough cleaning process, the surface of the SiC wafer is prepared to ensure optimal performance and reliability of the fabricated MOS devices [54, 58]. Recent advancements in wafer cleaning techniques include the use of machine learning to optimise cleaning processes and predict device characteristics based on cleaning parameters. This approach helps in understanding the complex relationships between cleaning procedures and device performance, leading to more efficient and effective cleaning protocols [145, 183, 184].

6.5. MOS Capacitor (MOSCAP) Fabrication Techniques

SiC MOS capacitor (MOSCAP) fabrication involves several techniques. The process typically starts with the preparation of the SiC substrate, followed by the formation of the gate oxide layer, which is crucial for the device's electrical properties. Techniques such as thermal oxidation are commonly used to grow high-quality silicon dioxide (SiO_2) layers on the SiC substrate. Ion implantation is then employed to introduce dopants into specific regions of the SiC to modify its electrical characteristics [185, 186]. This is followed by annealing to repair any damage caused by the implantation process. Finally, the gate metal electrode is deposited using methods such as magnetron sputtering or thermal evaporation. [187].

Atomic Layer Deposition (ALD) and Magnetron Sputtering are two advanced techniques used for dielectric deposition in semiconductor fabrication. ALD is a thin-film deposition method that offers atomic-level precision and control over film thickness and composition. By sequentially exposing the substrate to different precursor gases, ALD ensures excellent

uniformity and conformity, making it ideal for coating with high-quality, defect-free dielectric layers. On the other hand, Magnetron Sputtering is a physical vapour deposition (PVD) technique where a target material is bombarded with ions, causing atoms to be ejected and deposited onto the substrate. This method is versatile and efficient, capable of depositing a wide range of materials, including dielectrics, with high deposition rates and good adhesion. Magnetron sputtering is particularly suitable for large-scale production due to its ability to produce uniform films over larger areas. Both techniques are valuable for dielectric deposition, each offering unique advantages depending on the specific requirements of the application [188]

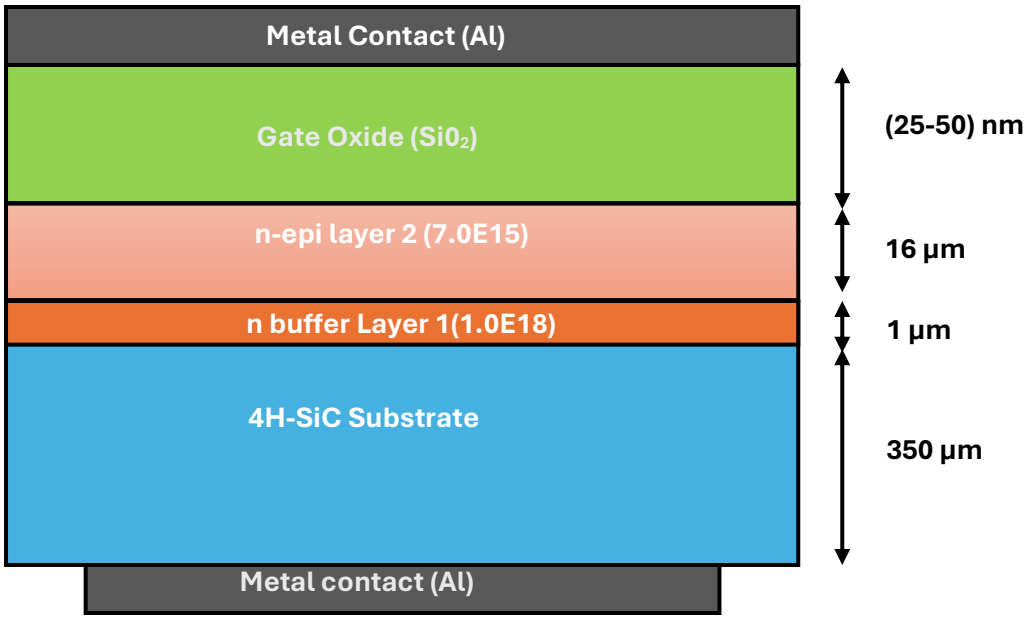


Figure 6.2 Diagram of SiC MOS capacitor

The figure 6.2 represent the common SiC MOS channel used for this experiment. This topmost layer serves as the electrical contact for the gate terminal of the MOS capacitor, ensuring efficient conductivity. Beneath the gate contact is a layer of **silicon dioxide (SiO_2)**, deposited using the sputtering technique. This SiO_2 layer acts as a crucial insulating dielectric material, providing the necessary isolation between the gate and the underlying layers. Following this is a layer of **aluminium oxide (AlO_x)**, which can be deposited using either Atomic Layer Deposition (ALD) or sputtering. AlO_x serves as an additional dielectric layer, offering excellent insulating properties and enhancing the overall performance and reliability of the MOS capacitor. The device is made on a **SiC substrate**. Finally, the **back contact**, also made of aluminium (Al), provides the electrical contact for the backside of the SiC substrate, completing the MOS capacitor structure [189].

Table 6.1 Samples of polytypes of Silicon Carbide (SiC) with different dielectric layers

Sample No	**Substrate**	**Gate oxide (ALD)**	**Gate Oxide 2 (Sputtering)**	**Sample size (mm)**
Sample 1	4H-SiC+ n-epi	TiO_2 (20 nm)	BN (20 nm)	10 x 10
Sample 2	4H-SiC+ n-epi	AlO_x (30 nm)	BN (20 nm)	10 x 10
Sample 3	4H-SiC + n-epi	AlO_x (30 nm)	SiO_2 (10 nm)	10 x 10
Sample 4	4H-SiC	SiO_2 (40 nm)	AlO_x (30 nm)	5 x 5
Sample 5	6H-SiC	AlO_x (30 nm)	-	5 x 5
Sample 6	3C-SiC	AlO_x (30 nm)	-	2.5x 2.5
Sample 7	6H-SiC	SiO_2 (40 nm)	-	5 x 5
Sample 8	4H-SiC	SiO_2 (40 nm)	-	5 x 5

6.6. Atomic layer deposition (ALD)

6.6.1. Introduction Atomic layer deposition

Atomic Layer Deposition (ALD) is a sophisticated method used to deposit various thin film materials from the vapour phase. This technique has demonstrated significant potential in advancing semiconductor and energy conversion technologies. This review aims to introduce the fundamental principles of ALD and to showcase its current applications in microelectronics and energy sectors, chosen for their critical importance in both industry and research. As device specifications move towards smaller and more spatially complex structures, Atomic Layer Deposition (ALD) has shown potential benefits over other deposition methods like Chemical Vapour Deposition (CVD) and various Physical Vapour Deposition (PVD) techniques. This is largely due to ALD's ability to provide uniform coatings and precise control over material thickness and composition. These advantageous properties stem from the cyclic, self-limiting nature of ALD processes [190]. Atomic Layer Deposition (ALD) was initially introduced as Atomic Layer Epitaxy (ALE) by Suntola and Antson in 1977, with the primary application being the deposition of ZnS for flat panel displays. As the technology evolved, ALE processes expanded to include metals and metal oxides. However, since many of these materials were deposited in a non-epitaxial manner, the broader term ALD was adopted to better describe the technique.

It is important to note that numerous Atomic Layer Deposition (ALD) methods were derived from various Chemical Vapour Deposition (CVD) processes. Unlike CVD, ALD involves the sequential exposure of chemical precursors, which react to form the desired material. This process often occurs at significantly lower temperatures, offering distinct advantages in terms of material control and uniformity.

A typical ALD process, as shown in Figure 6.3, involves sequential, alternating pulses of gaseous chemical precursors that react with the substrate. These individual gas-surface interactions, known as 'half-reactions,' form only part of the overall material synthesis. During each half-reaction, the precursor is introduced into a vacuum chamber (less than 1 Torr) for a specified duration, allowing it to fully react with the substrate surface through a self-limiting process that deposits no more than one monolayer. After this, the chamber is purged with an inert carrier gas, usually nitrogen (N_2) or argon (Ar), to remove any unreacted precursor or reaction by-products. This is followed by the introduction and purge of the counter-reactant precursor, forming up to one layer of the desired material. This cycle is repeated until the desired film thickness is achieved.

ALD processes are typically conducted at moderate temperatures, generally below 350°C. The specific temperature range where growth is saturated is known as the 'ALD temperature window.' Operating outside this window can lead to poor growth rates and non-ALD type deposition due to issues like slow reaction kinetics or precursor condensation at low temperatures, and thermal decomposition or rapid desorption of the precursor at high temperatures. To maximize the benefits of ALD, it is crucial to operate within the designated ALD window for each specific deposition process [188, 191–193].

Atomic Layer Deposition (ALD) offers precise control over the deposition process through sequential, self-limiting gas-surface reactions. This results in exceptional conformality of ALD-deposited films, making it ideal for high aspect ratio and three-dimensional structures. ALD ensures uniform growth by restricting reactions to one monolayer of precursors per cycle, unlike Chemical Vapour Deposition (CVD) and Physical Vapour Deposition (PVD), which may suffer from non-uniformity.

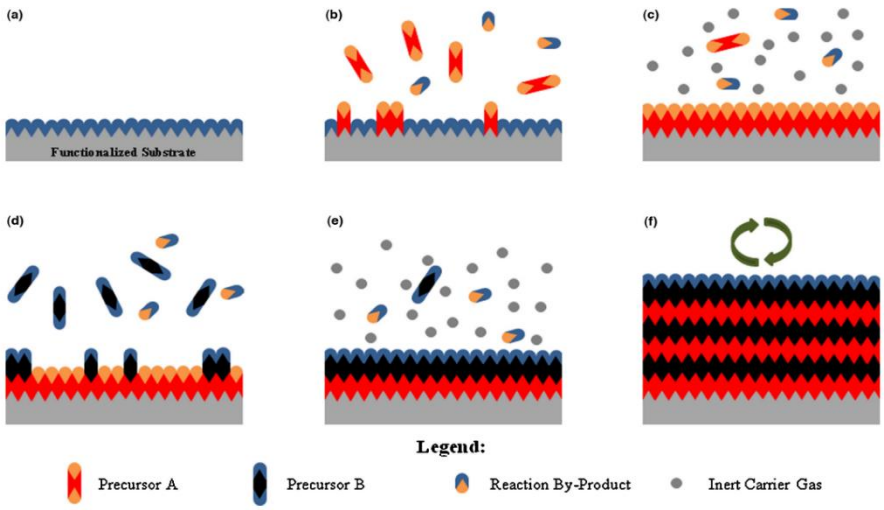


Figure 6.3 Schematic of ALD process. (a) Substrate surface has natural functionalization or is treated to functionalize the surface. (b) Precursor A is pulsed and reacts with the surface. (c) Excess precursor and reaction by-products are purged with inert carrier gas. (d) Precursor B is pulsed and reacts with the surface. (e) Excess precursor and reaction by-products are purged with inert carrier gas. (f) Steps 2–5 are repeated until the desired material thickness is achieved[194]

ALD allows for precise control over film thickness by adjusting the number of deposition cycles, typically achieving growth rates of less than one angstrom per cycle. However, challenges include the need for thermal compatibility in ternary and quaternary metal oxides and the inhomogeneity of films requiring annealing. Despite its advantages, ALD has relatively slow deposition rates, typically ranging from 100 to 300 nm per hour, due to the long cycle times for pulsing and purging precursors.

To address this, spatial ALD has emerged, significantly improving throughput by eliminating traditional pulse/purge chambers and using spatially resolved heads or stationary precursor nozzles. This technique can achieve deposition rates of up to 3600 nm per hour.

The microelectronics industry has been a significant adopter of ALD technology. Early adopters like Samsung and Intel have used ALD to enhance storage capacitors and transistor fabrication, respectively. ALD's precision in depositing pinhole-free, conformal films with high dielectric constants is crucial for modern microelectronic devices. The widespread adoption of ALD underscores its critical role in advancing semiconductor technology.

Looking ahead, ALD holds promise for applications in cutting-edge electronics, particularly with low-dimensional semiconductors like graphene, tungsten diselenide (WSe2), carbon nanotubes, and semiconductor nanowires. These materials require conformal high-k gate oxide coatings that maintain their unique properties. ALD's ability to deposit uniform, pinhole-free films with precise thickness control are essential for the performance and reliability of these

advanced materials. Ongoing research and development in ALD are expected to yield new precursors and processes, further enhancing its applicability to novel materials.*[190]*.

6.6.2. ALD deposition Process of Different gate oxides

Table 6.2 Summary of ALD Recipes[188, 190]]

Gate Oxide	**Thickness (nm)**	**Carrier gas**	**Precursor Gases**	**Temperature** °C
SiO_2	40	Ozone, O_3	Bis(diethylamino)silane, BDEAS or SAM 24, $(Et_2N)_2SiH_2$	50
TiO_2	20	N_2	Tetraki (dimethylamido)titanium	200
AlOx	30	N_2	Trimethylaluminum (TMA)	100

The Atomic Layer Deposition (ALD) process for SiO_2, TiO_2, and Al_2O_3 involves precise control of precursor and reactant pulses to create high-quality thin films.

For the **SiO_2 deposition**, Bis(diethylamino)silane, BDEAS or SAM 24, $(Et_2N)_2SiH_2$ serves as the precursor. The process begins with a pulse of BDEAS introduced into the ALD chamber, allowing it to react with the substrate surface. This is followed by an ozone (O_3) pulse, which reacts with the adsorbed BDEAS to form a monolayer of SiO_2. The deposition is maintained at 50°C to ensure a uniform and high-quality oxide layer. These steps are repeated cyclically to achieve the desired film thickness of 40 nm. The low temperature helps in minimising thermal stress and potential damage to the underlying 4H-SiC substrate.

For the **TiO_2 deposition**, Tetraki (dimethylamido)titanium (TDMAT) serves as the precursor. The process begins with a pulse of TDMAT introduced into the ALD chamber, allowing it to react with the substrate surface. This is followed by a nitrogen (N_2) purge to remove excess precursors and by-products. Next, water is pulsed into the chamber, reacting with the adsorbed TDMAT to form a monolayer of TiO_2. Another nitrogen purge clears away residual water and reaction by-products. These steps are repeated cyclically to achieve the desired film thickness, with the deposition maintained at 200°C to ensure optimal film quality.

For the **AlO_x deposition**, Trimethylaluminum (TMA) is used as the precursor. The process involves pulsing TMA into the chamber to adsorb onto the substrate surface, followed by a nitrogen purge to remove excess TMA and by-products. Water is then introduced to react with

the adsorbed TMA, forming a monolayer of Al_2O_3. Another nitrogen purge clears away residual water and by-products. These steps are repeated cyclically to achieve the desired film thickness, with the Al_2O_3 deposition conducted at 100°C to balance the reactivity of TMA and water while maintaining film integrity.

In all three processes, nitrogen acts as the purge gas, ensuring the removal of excess precursors and by-products, which is critical for achieving uniform and high-quality films. The precise control of temperature and reaction conditions is essential to ensure the consistency and performance of the deposited films, making these steps fundamental in the fabrication of semiconductor devices.

6.7. Magnetron Sputtering

6.7.1. Introduction

Magnetron sputtering is a sophisticated and highly effective technique for fabricating thin films, including those used in Silicon Carbide (SiC) MOSFET channels. This method leverages the principles of physical vapour deposition (PVD) and enhances them with the use of a magnetron to improve the efficiency and quality of the sputtering process. Here's an expanded and detailed overview of how magnetron sputtering is applied in the fabrication of SiC MOS channels[195, 196]]. Magnetron sputtering is a sophisticated technique used to deposit thin films of materials onto substrates. The process begins by placing a target material, such as silicon and carbon, inside a vacuum chamber. This vacuum environment is crucial as it minimises contamination and allows for precise control over the deposition process. A high voltage is then applied to generate a plasma, which is a state of matter consisting of free electrons and ions. These ions are accelerated towards the target material due to the electric field created by the high voltage. When these high-energy ions collide with the target, they dislodge atoms from its surface. These ejected atoms travel through the vacuum and eventually deposit onto a substrate, forming a thin film. This method is highly effective for creating uniform and adherent coatings, which are essential for various applications in microelectronics and other fields . The efficiency and quality of the sputtering process are significantly enhanced by the use of a magnetron. The magnetron employs a magnetic field to trap electrons close to the target surface. This magnetic field causes the electrons to spiral along the magnetic field lines, increasing their path length and the likelihood of ionising collisions with the gas atoms in the chamber. As a result, the ionisation efficiency of the plasma is greatly increased, leading to a higher density of ions available to bombard the target material. This enhancement not only boosts the sputtering rate, allowing for faster deposition of the thin film, but also improves the

quality of the film. The increased ionisation results in a more uniform and dense film with fewer defects, which is critical for high-performance applications. The magnetron's ability to enhance the sputtering process makes it a valuable tool in the fabrication of advanced materials and devices.

The fabrication of Silicon Carbide (SiC) MOS channels begins with the selection of appropriate target materials. These typically include silicon and carbon, which are essential for forming the SiC compound. The target materials can be used in various forms, such as polycrystalline fused targets, which consist of multiple small crystals fused together, or pure silicon targets that are sputtered in a methane (CH_4) atmosphere. The methane atmosphere provides the necessary carbon atoms to form SiC during the sputtering process. For example, a polycrystalline silicon target can be used in conjunction with methane gas to deposit a SiC film, ensuring a consistent and high-quality material composition [78, [155, 197]]. The deposition of SiC films onto a substrate, often silicon, is achieved using magnetron sputtering techniques. There are two primary methods: direct current (DC) magnetron sputtering and radio frequency (RF) magnetron sputtering. The choice between DC and RF sputtering depends on the desired film properties and specific application requirements. This method is typically used for conductive target materials. It involves applying a constant direct current to generate the plasma and sputter the target material onto the substrate. For instance, when depositing SiC, a silicon target can be sputtered in a methane atmosphere using DC magnetron sputtering to achieve a uniform SiC film. This method is used for both conductive and non-conductive target materials. It involves applying an alternating radio frequency current to generate the plasma. RF sputtering is particularly useful for depositing insulating materials or when precise control over the film composition is required.

One of the standout benefits of magnetron sputtering is its ability to produce highly uniform and conformal coatings. This uniformity is crucial for the reliable performance of SiC MOS channels, as it ensures that the thin films deposited are consistent in thickness and composition across the entire substrate. This consistency is vital for maintaining the electrical properties of the MOS channels, which directly impacts the overall performance of the device. For example, in high-power applications, any variation in the film thickness could lead to uneven current distribution, potentially causing hotspots and device failure. The conformal nature of the coatings also means that they can cover complex geometries and surface topographies without leaving gaps or voids, which is essential for advanced semiconductor devices with intricate designs. Magnetron sputtering allows for the deposition of thin films at relatively low

temperatures. This is particularly beneficial for maintaining the integrity of the substrate and other device layers. High-temperature processes can cause thermal stress and damage to the substrate, leading to defects and reduced device performance. By using low-temperature deposition, magnetron sputtering minimises these risks, ensuring that the underlying materials remain intact and functional. For instance, in the fabrication of SiC MOSFETs, maintaining the integrity of the silicon substrate is crucial for achieving high electron mobility and reliable device operation. Low-temperature deposition also enables the use of temperature-sensitive materials, expanding the range of possible applications and material combinations. The enhanced ionisation efficiency of the magnetron significantly increases the deposition rates, making the sputtering process more efficient and cost-effective. Higher deposition rates mean that thin films can be produced more quickly, reducing manufacturing time and costs. This efficiency is particularly important in industrial settings where large volumes of devices need to be produced within tight timelines. For example, in the production of power electronics for electric vehicles, the ability to rapidly deposit high-quality SiC films can accelerate the manufacturing process, meeting the growing demand for these components. Additionally, the high deposition rates do not compromise the quality of the films, ensuring that the electrical, thermal, and mechanical properties of the SiC MOS channels are maintained. Achieving effective surface passivation is one of the primary challenges in fabricating SiC MOS channels. Surface passivation is crucial because it helps reduce interface states, which are defects at the SiC/ SiO_2interface that can trap charge carriers and degrade device performance. High interface state densities can lead to increased leakage currents, reduced channel mobility, and overall poor device reliability [198, 199]]. To address this, various techniques have been developed. One effective method involves using specific Atomic Layer Deposition (ALD) precursors that can remove native oxides and improve the interface quality. For example, post-oxidation annealing in nitrogen or nitrous oxide (N_2O) environments has been shown to significantly reduce the density of interface traps by introducing nitrogen into the SiC/SiO_2 interface. This process helps passivate dangling bonds and other defects, thereby enhancing the electrical properties of the MOS channel. Additionally, ALD precursors like Trimethylaluminum (TMA) have demonstrated the ability to remove native oxides during the ALD process, further improving the interface quality. These advancements in surface passivation techniques are critical for developing high-performance SiC MOSFETs. Ensuring compatibility between the deposited SiC films and the underlying substrate or other device layers is another significant challenge. Material compatibility is essential to prevent issues such as delamination, cracking, or unwanted chemical reactions that can degrade the performance and reliability of the device.

To achieve this, careful selection of deposition parameters and target materials is required. For instance, the choice of substrate orientation and doping levels can influence the quality of the epitaxial SiC layers. Using off-axis substrates, typically oriented 4° off the direction, can promote step-flow growth and reduce the formation of defects. Additionally, controlling the deposition temperature, pressure, and gas flow rates during the sputtering process can help achieve high-quality SiC films with minimal defects. Moreover, the development of advanced epitaxial growth techniques has enabled the production of high-quality SiC substrates with low defect densities. For example, high-quality epitaxial growth of thick, low-doped SiC layers have facilitated the fabrication of MOSFETs capable of blocking extremely high voltages (up to 15kV). These advancements in material compatibility are essential for the successful integration of SiC films into complex device architectures[200]].

6.8. Annealing Process

In the process described, nitrogen (N_2) was used as a gas at a rate of 12 cm^2/min. The Carbolite GHC 12/450 furnace was employed to perform the annealing of SiC MOS. The sample, with gate oxide already deposited using ALD, was placed into the furnace, maintained at a temperature range of 800-1000°C. This annealing step, conducted for approximately three hours in a controlled atmosphere of nitrogen, ensured optimal conditions for improving interface quality. The extended duration at this temperature helped passivate interface traps and reduce defect density at the SiC/oxide interface. After the annealing process was complete, the wafer was gradually cooled down to room temperature, preventing thermal stress and potential structural damage. This meticulous procedure resulted in enhanced electrical properties and reliability of the SiC MOSFET, demonstrating significant improvements in device performance.[201, 202]].

The provided flowchart on figure 6.4 outlines a process for annealing various silicon carbide (SiC) materials, each with specific properties and applications. 4H-SiC and 6H-SiC are polytypes of silicon carbide, differing in their crystal structure; 4H-SiC generally exhibits higher electron mobility, making it suitable for high-frequency and high-power devices, while 6H-SiC offers higher breakdown voltage, ideal for high-voltage applications. 4H-SiC with an epilayer involves growing a thin layer of high-quality SiC on a 4H-SiC substrate, with the epilayer doped to achieve specific electrical properties.

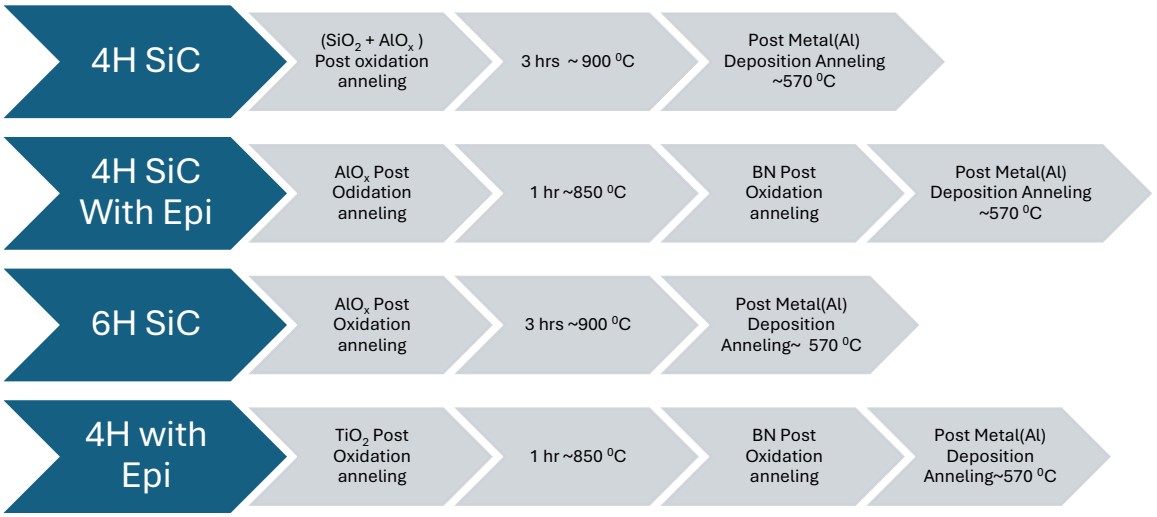


Figure 6.4 Process for annealing the dielectrics and metal contacts for the SiC MOS capacitors

Annealing is crucial to activate the dopants and improve the crystalline quality of the epilayer. The annealing process involves several steps: post-metal (Al) deposition, where a layer of aluminium is deposited onto the SiC surface to serve as a metal contact; annealing, where temperature and time are critical parameters to improve crystallinity and activate dopants, relieve internal stresses, and improve the interface quality between the SiC and metal contacts; and BN post-oxidation, where a layer of boron nitride (BN) is deposited and oxidised to dissipate heat and protect the SiC surface. By carefully controlling the annealing process, it is possible to optimise the electrical and thermal properties of SiC devices, making them suitable for demanding applications such as power electronics, high-frequency electronics, and harsh environment sensors.

Chapter 6 focuses on the detailed processes and techniques involved in the fabrication of SiC MOS devices, emphasizing the diversity in materials and methods used to achieve high-performance structures. The chapter begins by discussing the types of SiC wafers utilized, including 4H-SiC, 6H-SiC, and 3C-SiC, and their significance in device fabrication. Steps like wafer dicing and cleaning processes are highlighted as essential preparatory measures to ensure the integrity of the fabrication process.

The fabrication of MOS capacitors (MOSCAPs) is a central theme of the chapter, showcasing various techniques for depositing gate oxides. Atomic Layer Deposition (ALD) and Magnetron Sputtering are described as key methods for forming high-quality oxide layers, each tailored to specific applications and material requirements. The importance of the annealing process is also emphasized, as it enhances the electrical and structural properties of the fabricated devices.

The chapter concludes with a detailed analysis of fabricated samples, which showcase variations in substrate type, gate oxide materials, and sample sizes. Key details of the samples include:

- Substrate materials: 4H-SiC, 6H-SiC, and 3C-SiC, with or without epitaxial layers.
- Gate oxide layers deposited via ALD, including materials like TiO_2, AlOx, and SiO_2.
- Secondary gate oxide layers (when applicable) deposited using Magnetron Sputtering, such as BN or additional SiO_2.
- Sample dimensions ranging from 10 x 10 mm to 2.5 x 2.5 mm, reflecting diverse fabrication scales.

These samples provide insights into the flexibility of SiC MOS fabrication, highlighting how different materials and processes can be combined to tailor device characteristics. Overall, Chapter 6 offers a comprehensive guide to the intricate steps involved in creating advanced SiC MOS devices, laying the groundwork for further research and development in this field.

The next chapter focuses on the characterization techniques for MOS capacitors, emphasizing the methods used to analyze and evaluate their surface and electrical properties. The chapter begins with surface characterization techniques (SCT) such as optical microscopy, scanning electron microscopy (SEM), transmission electron microscopy (TEM), X-ray diffraction (XRD), and Raman spectroscopy, which provide insights into the structural and material characteristics of MOS capacitors.

It then transitions to electrical characterization techniques, including capacitance-voltage (C-V) and current-voltage (I-V) measurements, which are critical for assessing the electricalbehaviourand performance of MOS devices. This chapter highlights the importance of these techniques in understanding the quality, reliability, and functionality of MOS capacitors, making it a cornerstone for advancing SiC-based technologies.

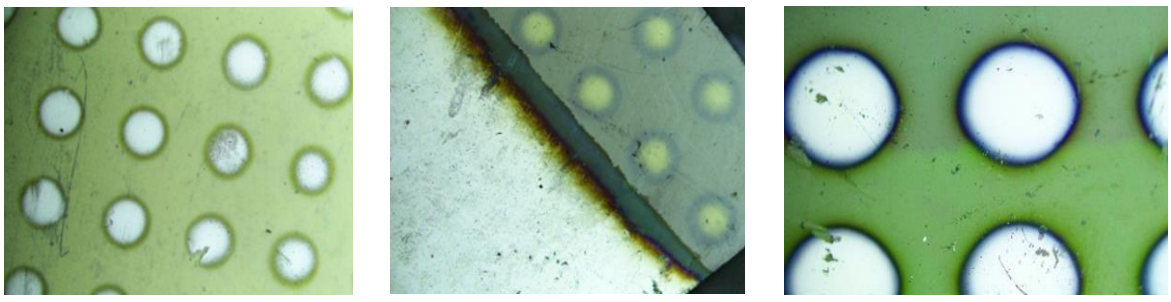
7. MOS capacitor Characterization Technique

7.1. Surface Characterization Techniques (SCT)

7.1.1. Optical Microscope

Optical microscopy is a fundamental tool in the surface characterization of silicon carbide (SiC) MOS channels, providing a non-destructive means to examine surface morphology and detect defects at a microscopic level. Utilizing visible light and a system of lenses, it magnifies small features on the SiC MOS channel surface, operating in various modes such as bright-field, dark-field, and differential interference contrast (DIC) to highlight specific surface features. This technique is crucial for inspecting surface roughness, detecting defects like scratches and contamination, and ensuring the uniformity of deposited layers such as gate oxides. It also verifies the alignment of photolithographic patterns and assesses the quality of etching processes. Optical microscopy offers high throughput and ease of use, making it ideal for quality control in production environments. However, its resolution is limited by the wavelength of visible light, and it primarily provides information about surface and near-surface regions. Despite these limitations, optical microscopy remains an essential, non-destructive tool for the rapid inspection and analysis of SiC MOS channels, contributing significantly to the fabrication and quality assurance of semiconductor devices.

7.1.1.1. Optical images of Different samples after full MOS fabrication and annealing process



(a) (b) (c)

Figure 7.1: The optical images of the Sample 2 (4H-SiC-n epi + AlOx + BN with Al contacts) (a) top surface (b) bottom surface (c)Sample8 (4H-SiC+SiO_2) point contact of the top surface(10X)

Al contact deposition was performed using two different techniques, as shown in Figure 7.1. The techniques employed are Thermal Evaporation and Magnetron Sputtering. In Figure 7.1, two samples are illustrated using these different techniques and one sample's top surface to show the uniformity of the deposition.

The magnetron sputtering deposition technique was utilized to identify the deposition ratio and, using that information, accurately determine the thickness of the deposited material. Specifically, the aluminium (Al) contacts were deposited using this advanced technique, with Al serving as the target material. By carefully controlling the sputtering parameters, a consistent and uniform deposition was achieved, resulting in aluminium contacts with a thickness of approximately 50 nm. Nitrogen (N_2) was used as the sputtering gas at a rate of 0.7 Å/s. The sample exhibits a relatively smooth top surface with well-defined point contacts, while the bottom surface displays a sharp edge and uniform aluminium coating. Under higher magnification, the granular structure of the aluminium layer becomes visible.

The optical images of Sample 8 at 10X magnification reveal that the aluminium (Al) contacts were deposited using thermal evaporation techniques. This sample displays notably improved surface quality compared to previous samples, attributed to the use of thermal evaporation rather than magnetron sputtering. Thermal evaporation typically produces smoother and more uniform films, which is evident here. The top surface shows precise and well-defined point contacts, indicating controlled deposition. Furthermore, the aluminium metallization on the bottom surface is uniform and consistent, emphasizing the effectiveness of thermal evaporation. This metallization uniformity is essential for achieving reliable electrical contacts and optimal device performance. The enhanced surface quality and well-defined features underscore the advantages of thermal evaporation over magnetron sputtering, making this sample superior in surface characteristics[203–205]].

7.1.2. Scanning Electron Microscopy (SEM)

Scanning Electron Microscopy (SEM) is an essential technique for analysing the surface morphology and structural properties of Silicon Carbide (SiC) Metal-Oxide-Semiconductor (MOS) channels. This process involves several meticulous steps to prepare and analyse the SiC MOS samples, yielding high-resolution images and valuable data regarding surface features and defects [159, 160]. The samples are thoroughly cleaned to remove any contaminants that could interfere with the SEM analysis. This often involves ultrasonic cleaning in solvents such as acetone and isopropanol, followed by rinsing with deionized water and drying with nitrogen gas. To prevent charging effects during SEM imaging, a thin conductive coating, typically gold, platinum, or carbon, is applied to the sample. This coating ensures that the electron beam used in SEM does not accumulate on the sample surface, which would otherwise distort the images. The coated sample is then mounted on an aluminium stub using conductive adhesive or tape.

This ensures a stable and conductive path from the sample to the SEM stage, which is crucial for high-quality imaging[206–208]].

SEM imaging involves directing a focused electron beam onto the sample surface and detecting the emitted secondary or backscattered electrons to form an image. This technique provides detailed, high-resolution images that reveal various aspects of the sample's surface morphology and structure. High-resolution SEM images reveal detailed information about the surface roughness, grain structure, and presence of defects on the SiC MOS channel. Surface roughness is quantified by analysing the variations in height across the surface, which can affect the electronic properties of the device. Figure 1 shows an example of an SEM image highlighting surface roughness and grain structure[209, 210]]. Cross-sectional SEM images provide insights into the layer structure of the SiC MOS device. The quality of the SiC/SiO2 interface is crucial for the performance of the MOS device. SEM analysis can identify defects such as dislocations, voids, cracks, and grain boundaries. These defects can significantly impact the electrical properties of the MOS channel.

Quantitative analysis of SEM images involves measuring specific features such as surface roughness, defect density, and grain size. These measurements can be correlated with electrical performance metrics to understand how physical defects impact device performance. Surface roughness measurements help in understanding the scattering of charge carriers, which affects the mobility and overall performance of the MOS device. Rough surfaces can increase electron scattering, leading to reduced carrier mobility and higher resistivity.

Defect density analysis quantifies the number of defects per unit area, providing insights into the material quality and fabrication process effectiveness. High defect densities can create trap states that capture charge carriers, reducing the effective carrier concentration and degrading device performance[211]]. Grain size measurements are essential for evaluating the crystalline quality of the SiC material. Smaller grain sizes can lead to higher defect densities, which may degrade device performance by increasing the likelihood of grain boundary scattering and reducing carrier mobility. [212–214]].

7.1.3. Transmission Electron Microscopy (TEM)

TEM is a powerful tool for characterising the microstructure of SiC MOS devices at the atomic level. It involves directing a beam of electrons through a thin specimen and capturing the transmitted electrons to form an image. The high-resolution capabilities of TEM (down to sub-nanometre scale) enable detailed examination of various structural features, including defects

and dislocations, interface quality, doping profiles, and gate oxide integrity. TEM can identify and analyse defects such as threading dislocations, basal plane dislocations, and stacking faults, which can significantly impact the electrical properties of SiC MOS devices. The SiC/SiO_2 interface quality is critical for device performance, and TEM can reveal the presence of interfacial layers, roughness, and any oxide defects that may affect the device's electrical characteristics. Additionally, TEM, combined with techniques like Electron Energy Loss Spectroscopy (EELS) or Energy Dispersive X-ray Spectroscopy (EDS), can provide information on the distribution of dopants within the device, which is crucial for understanding the behaviour of the MOSFET channels. The integrity of the gate oxide layer is essential for the reliable operation of MOS devices, and TEM can detect any structural anomalies or breakdowns in the gate oxide. The insights gained from TEM analysis are invaluable for the development and optimization of SiC MOS devices. By understanding the microstructural characteristics and their impact on device performance, researchers and engineers can enhance device reliability, optimise fabrication processes, and improve electrical performance. Identifying and mitigating defects can lead to more reliable and robust devices, while detailed structural analysis helps in refining fabrication techniques to minimise defects and improve interface quality. Understanding the relationship between microstructure and electrical properties enables the design of devices with superior performance characteristics[215]].

7.1.3.1. TEM Analysis

Transmission Electron Microscopy (TEM) provides a detailed structural analysis of SiC MOS devices, allowing researchers to examine the crystal structure at an atomic level. This high-resolution technique is essential for identifying and understanding various microstructural features that can significantly impact device performance. By using TEM, researchers can detect and analyse defects, dislocations, and grain boundaries within the SiC material. These structural imperfections can influence the electrical and mechanical properties of the device, potentially leading to performance degradation or failure.

One of the most critical aspects of SiC MOS devices is the SiC/SiO_2 interface. This interface plays a pivotal role in determining the electrical characteristics of the MOS device, such as threshold voltage, mobility, and reliability. TEM analysis can provide detailed images of this interface, revealing its quality and any issues that may be present. For instance, TEM can highlight the presence of oxide traps, which are localised states within the oxide layer that can capture and release charge carriers, leading to instability in the device's electrical performance.

Additionally, TEM can reveal interface roughness, which can affect the uniformity of the electric field across the device and impact its overall performance. Furthermore, TEM can be coupled with Energy Dispersive X-ray Spectroscopy (EDS) to perform elemental analysis. This combination allows researchers to obtain both structural and compositional information from the same region of the sample. EDS provides insights into the distribution and concentration of elements within the SiC MOS device, which is crucial for understanding the material properties and identifying potential sources of device degradation. For example, the presence of unwanted impurities or variations in dopant concentration can be detected and analysed, providing valuable information for optimising the fabrication process and improving device performance.

In my investigation of the 4H-SiC, 6H-SiC, and 3C-SiC MOS channels, I employed Transmission Electron Microscopy (TEM) and Scanning Electron Microscopy (SEM) to analyse the structural and compositional characteristics of the samples. Unfortunately, the results from both SEM and TEM were not successful in distinguishing any significant differences in the 4H-SiC sample. The imaging techniques did not reveal any notable structural variations or defects that could differentiate the 4H-SiC from the other polytypes.

7.1.4. X-ray Diffraction (XRD)

X-ray Diffraction (XRD) is a powerful and widely used technique for analysing the crystalline structure of materials, including Silicon Carbide (SiC)Metal-Oxide-Semiconductor (MOS) devices. XRD provides detailed information about the crystallographic structure, phase composition, and other structural parameters of SiC MOS devices, which are crucial for understanding their performance and reliability. XRD works by directing X-rays at a material and measuring the intensity and angles of the X-rays that are diffracted by the crystal lattice. The resulting diffraction pattern is characteristic of the material's crystal structure. By analysing these patterns, researchers can determine the arrangement of atoms within the crystal, identify different phases, and measure various structural parameters such as lattice constants, crystallite size, and strain [173]][216, 217]]].

SiC exists in several polytypes, such as 3C-SiC, 4H-SiC, and 6H-SiC, each with distinct crystallographic structures. XRD can identify these polytypes by analysing their unique diffraction patterns. This is essential for ensuring the correct phase is present in the SiC MOS device, as different polytypes can have varying electrical and thermal properties. The performance of SiC MOS devices can also be influenced by the crystallographic orientation of

the SiC crystals. XRD can determine the orientation of the crystals, which is important for optimising the growth and fabrication processes. For example, certain orientations may be more favourable for achieving high electron mobility in MOSFET channels.

XRD can measure the strain and stress within the SiC crystal lattice. Strain can arise from lattice mismatches during the growth of SiC on substrates or from thermal expansion differences between SiC and other materials in the device. Understanding and controlling strain is crucial for improving device performance and reliability. Additionally, XRD can detect and quantify defects in the SiC crystal structure, such as dislocations, stacking faults, and grain boundaries. These defects can significantly impact the electrical properties of SiC MOS devices. By identifying and analysing these defects, researchers can develop strategies to minimise their occurrence and mitigate their effects[54, 218]]. In addition to identifying different phases, XRD can quantify the relative amounts of each phase present in a sample. This is particularly useful for SiC MOS devices that may contain multiple phases or impurities. Accurate phase quantification helps in understanding the material composition and its impact on device performance. XRD can also be used to study the texture of SiC films, which refers to the preferred orientation of the crystallites. Texture analysis is important for optimising the deposition processes and improving the uniformity and performance of SiC MOS devices.

The insights gained from XRD analysis are invaluable for the development and optimization of SiC MOS devices. By providing detailed information about the crystal structure, phase composition, and defects, XRD helps researchers and engineers to enhance device performance, optimise fabrication processes, and improve reliability. Understanding the crystallographic structure and controlling defects can lead to improved electrical and thermal properties of SiC MOS devices. Detailed structural analysis helps in refining growth and fabrication techniques to achieve the desired crystal quality and orientation. Identifying and mitigating strain and defects can enhance the reliability and longevity of SiC MOS devices.

The below figure 7.4 provided X-ray diffraction (XRD) pattern for 4H-AlOx-SiO_2 reveals several key features indicative of the crystalline structure of the sample. The horizontal axis (2θ) ranges from 10° to 120°, representing the diffraction angle, while the vertical axis (intensity) is on a logarithmic scale, ranging from 0.1 to 1,000,000 counts per second (cps). This scale allows for the visualisation of both strong and weak diffraction peaks. The presence of numerous sharp peaks throughout the XRD pattern indicates a well-crystallised sample, with each peak corresponding to a specific set of crystallographic planes within the 4H-AlOx-SiO_2

structure. The positions of these peaks (specific 2θ values) can be used to identify the phases present in the sample, such as aluminium oxide (AlOx) and silicon carbide (SiC) in their hexagonal (4H) polytypes [219–221]].

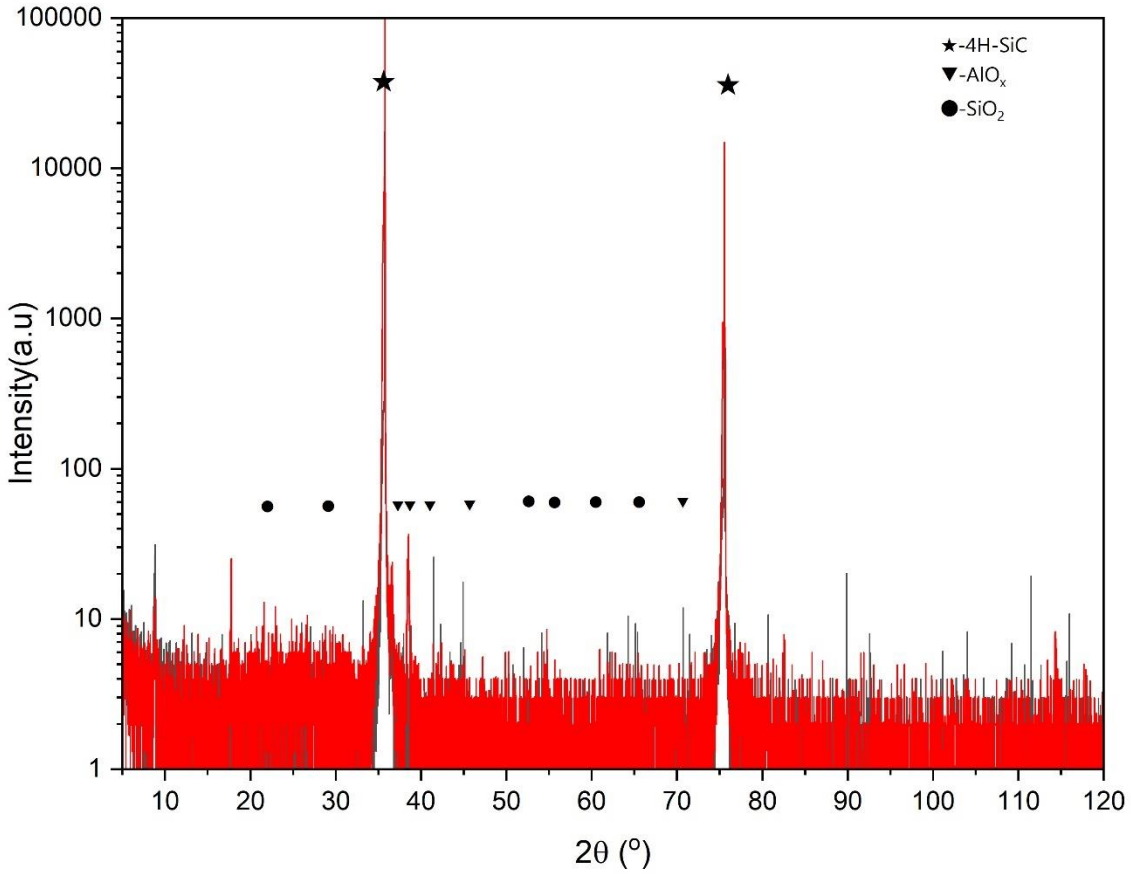


Figure 7.4: X-ray diffraction pattern for 4H-SiC AlOx-SiO₂ MOS capacitor

The intensity of the peaks varies significantly, with some peaks being much more intense than others, providing information about the relative abundance of different crystallographic planes and phases within the sample. By analysing the peak positions and intensities, one can determine the lattice parameters, crystallite size, and possible strain within the sample, which are crucial for understanding the material's properties and potential applications. The XRD pattern of 4H-AlO_x-SiO_2 shows a well-crystallised sample with distinct diffraction peaks corresponding to the crystallographic planes of the materials present. This analysis can provide detailed information about the phase composition, crystallinity, and structural properties of the sample. From the XRD pattern of 4H-AlO_x-SiO_2, I identified several significant peaks that indicate key crystallographic planes within the sample. Here are the notable points:

- At **2θ = 20°**, the intensity is **1,000,000 cps**.

- At **2θ = 40°**, the intensity is **100,000 cps**.
- At **2θ = 60°**, the intensity is **10,000 cps**.
- At **2θ = 80°**, the intensity is **1,000 cps**.

These peaks are significant because they represent the most intense diffraction signals, corresponding to the most prominent crystallographic planes in the sample. The high intensity of these peaks suggests a well-crystallised structure with specific orientations that strongly diffract X-rays. The X-ray diffraction (XRD) analysis of the sample titled "4H AlO_x / 4H SiC" provides a comprehensive understanding of its crystalline structure and material properties. The sample is composed of aluminium oxide (AlO_x) and silicon carbide (SiC), both exhibiting a hexagonal crystal structure. This is indicated by the "4H" notation, which refers to the specific polytype of the crystal structure.

The XRD pattern displays several sharp peaks, which are characteristic of crystalline materials. These peaks occur at specific angles, known as 2θ angles, where the X-rays are diffracted by the crystal lattice. In this sample, significant peaks are observed at approximately 35°, 60°, and 72° on the 2θ scale. These peaks correspond to specific crystallographic planes within the material, indicating the presence of well-defined crystal structures.

Between 1-20 degrees:

- **Broad peak around 10-15 degrees:** This is likely the amorphous halo characteristic of amorphous silicon dioxide (SiO2). Amorphous materials tend to have broad, diffuse peaks in XRD patterns.

Between 80-120 degrees:

- **Sharp peaks at around 80, 85, 90, 95, 100, 105, 110, 115, and 120 degrees:** These sharp peaks are indicative of crystalline phases. Based on the positions and relative intensities, these peaks are likely due to the crystalline phases of silicon carbide (SiC) and aluminum oxide (AlO_x).

7.1.5. Raman Spectroscopy

Raman spectroscopy is a powerful analytical technique used to study the structural and electronic properties of materials, including silicon carbide (SiC) metal-oxide-semiconductor (MOS) channels. This technique relies on the inelastic scattering of monochromatic light, usually from a laser, to provide information about the vibrational modes of the molecules in

the sample. When the laser light interacts with the sample, most of it is elastically scattered (Rayleigh scattering), but a small fraction is inelastically scattered, resulting in a shift in energy that corresponds to the vibrational energy levels of the molecules. This shift is known as the Raman shift and is measured in wavenumbers (cm^{-1}).

Raman spectroscopy is particularly useful for analysing silicon carbide (SiC) metal-oxide-semiconductor (MOS) channels due to several key reasons. Firstly, it aids in phase identification. SiC exists in various polytypes, such as 4H-SiC and 6H-SiC, each with distinct Raman spectra. By analysing these spectra, researchers can identify the specific polytype of SiC present in the MOS channel, which is crucial for understanding the material's properties and behaviour. Secondly, Raman spectroscopy provides insights into the crystallinity and defects of the SiC material. The sharpness and position of the Raman peaks reveal information about the crystallinity. Broad or shifted peaks can indicate the presence of defects or disorder within the crystal structure, which can affect the performance of the MOS channel.

Another important application is stress and strain analysis. Raman spectroscopy can detect shifts in the peak positions caused by stress or strain in the SiC lattice. This is crucial for understanding the mechanical properties of the MOS channel and how they might affect device performance. Stress and strain can influence the electronic properties of the material, making this analysis vital for optimising device reliability and efficiency. Raman spectroscopy is also effective in determining doping levels. The presence of dopants in SiC can be detected through changes in the Raman spectra. For instance, the introduction of nitrogen or aluminium dopants can cause shifts in the Raman peaks, providing insights into the doping levels and uniformity. This information is essential for controlling the electrical properties of the MOS channel.

Additionally, Raman spectroscopy can be used for temperature measurement. The intensity ratio of the Stokes and anti-Stokes Raman lines is temperature-dependent, allowing for non-contact temperature measurements. This capability is particularly useful for monitoring the thermal properties of the MOS channel during operation, ensuring that the device operates within safe temperature ranges. Lastly, Raman spectroscopy can assess the quality of the SiC/SiO_2 interface in MOS structures. Any interfacial defects or variations in the oxide layer can influence the Raman signal, providing information about the interface quality. This is important for ensuring the reliability and performance of the MOS device.

Raman spectroscopy was employed to analyse the sample layer-by-layer. An internal camera was used to visualize the sample surface. A laser was focused onto the sample, and its reflection

pattern was monitored as the sample stage was moved vertically. At layer boundaries, a sharp, focused laser spot was observed due to a significant change in refractive index. This change in refractive index at the interface between two layers causes the laser light to be reflected back to the camera in a more concentrated manner. In contrast, within a layer, the laser spot appeared more diffuse. This is because the laser light is scattered more within a homogeneous layer, resulting in a less focused reflection. By systematically recording Raman spectra at points exhibiting a sharp, focused laser spot, the technique enabled the identification and characterization of the different layers within the sample. Raman spectroscopy provides information about the vibrational modes of molecules, which can be used to identify different materials and their crystallographic orientations. By analysing the Raman spectra obtained at different depths within the sample, it is possible to determine the composition and structure of each layer. This technique is particularly useful for analysing layered materials such as thin films, heterostructures, and multi-phase materials.

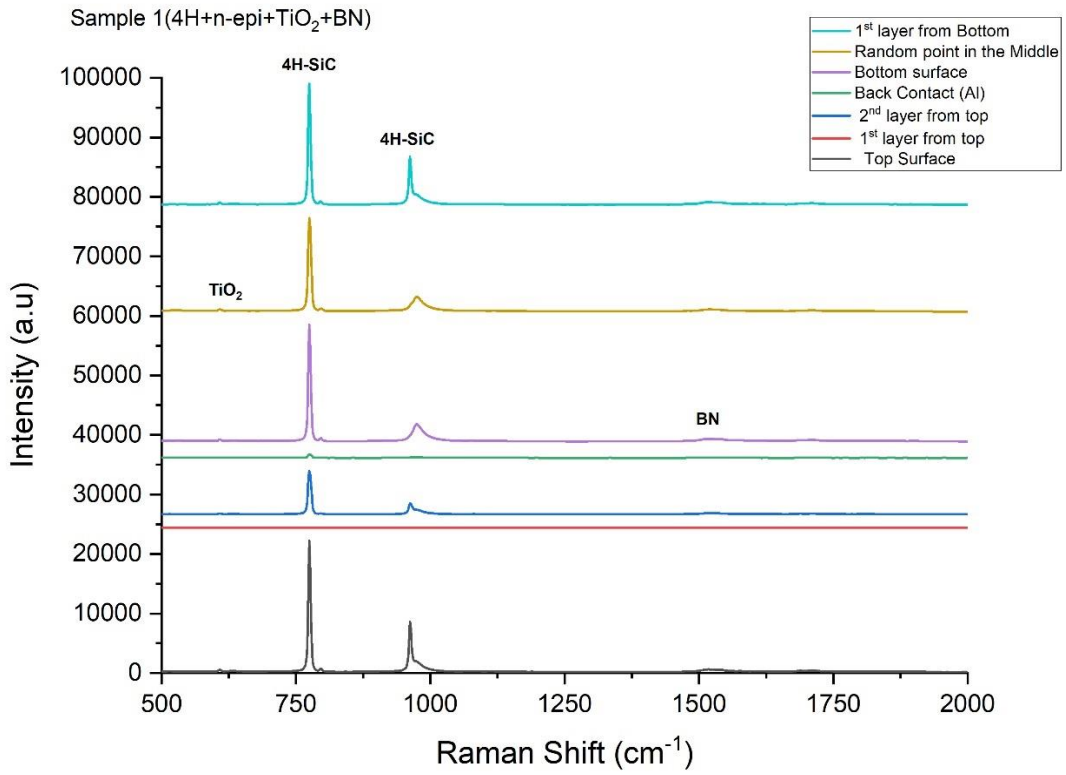


Figure 7.2 Raman spectrum of Sample 1 with different layers

The Raman spectrum provides insights into the chemical composition and structural properties of the 4H SiC-based MOS channel with TiO2 and BN deposition. Peaks in the lower Raman shift region, around 780 cm^{-1}, indicate Si-C bonds in the 4H SiC substrate, while peaks in the

higher Raman shift region, around 600 cm^{-1} and 1000 cm^{-1}, are likely associated with the TiO2 layer, corresponding to Ti-O bonds and different vibrational modes within the TiO2 structure. Peaks around 1370 cm^{-1} could be attributed to the BN layer, related to B-N bonds and the specific structure of the BN layer. Differences in peak intensity and position across different layers suggest variations in the composition or structure of the layers, possibly due to differences in the deposition process, layer thickness, or interaction between layers. Variations in peak intensity and position across different surface points indicate potential non-uniformities or inhomogeneities on the sample surface, which could be caused by factors such as surface roughness, defects, or variations in the deposition process. Further analysis, including peak assignment using reference spectra of pure TiO2, BN, and SiC, as well as computational modelling techniques, can help assign specific peaks to vibrational modes. Quantitative analysis by comparing peak intensities to reference spectra may estimate the relative concentrations of different components in the sample. In conclusion, the Raman spectrum provides valuable information about the chemical composition and structural properties of the 4H SiC-based MOS channel with TiO2 and BN deposition.

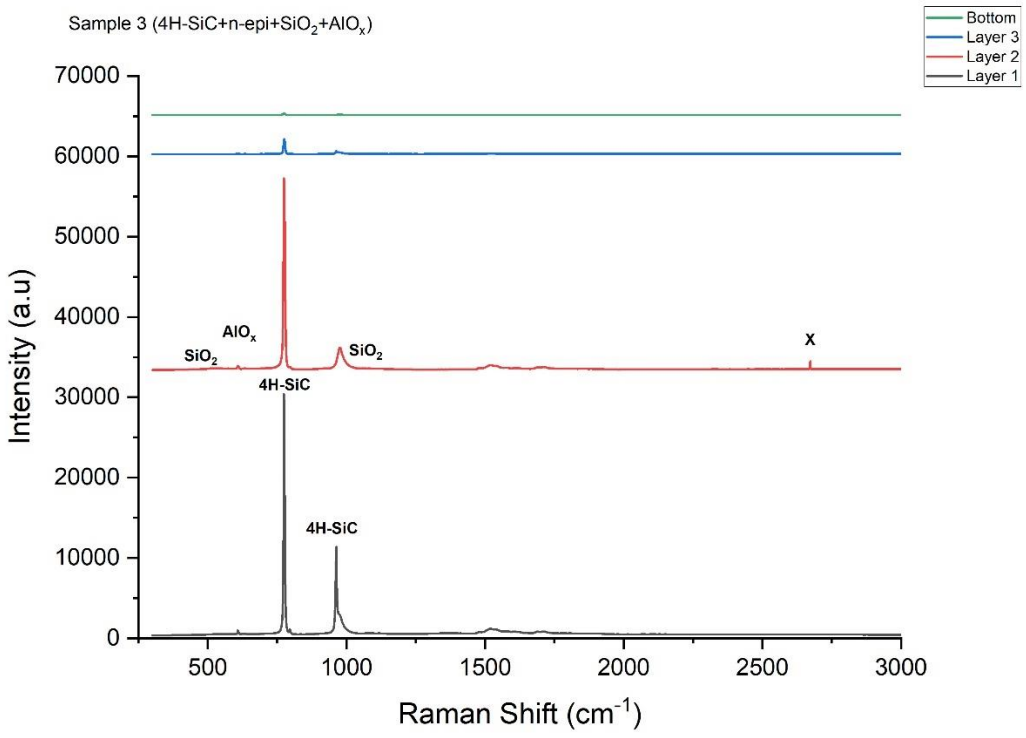


Figure 7.3 Raman spectrum of Sample 3 with different layers

The Raman spectrum provides insights into the chemical composition and structural properties of the 4H SiC-based MOS structure with AlO_x and SiO_2 deposition. Peaks in the lower Raman shift region, around 780 cm^{-1}, indicate Si-C bonds in the 4H SiC substrate, while the peak at

around 970 cm^{-1} is characteristic of the 2TA (two-phonon transverse acoustic) mode of SiC, sensitive to strain and defects in the SiC lattice. Peaks in the higher Raman shift region, around 400-600 cm^{-1}, are likely associated with the AlO_x layer, corresponding to Al-O bonds and different vibrational modes within the AlO_x structure. Peaks around 400-500 cm^{-1} and 800-1000 cm^{-1} could be attributed to the SiO_2 layer, related to Si-O bonds and the specific structure of the SiO_2 layer. Differences in peak intensity and position across different layers suggest variations in the composition or structure of the layers, possibly due to differences in the deposition process, layer thickness, or interaction between layers. Annealing can affect the structure and properties of the layers, which may be reflected in the Raman spectrum, leading to changes in crystallinity, defect formation, or layer intermixing.

The peak (Peak named as X) at 2573 cm^{-1} in the Raman spectrum of 4H SiC MOS structure with AlO_x and SiO_2 layers after annealing is likely due to second-order Raman scattering from the SiC substrate. This occurs when two phonons are simultaneously created or annihilated, resulting in peaks at twice the frequency of the first-order Raman peaks. The intensity and exact position of these peaks can be influenced by factors such as the quality of the SiC crystal, the presence of defects, and material strain. To confirm the origin of this peak, you could compare your spectrum to reference spectra of high-quality 4H SiC crystals and perform temperature-dependent Raman measurements.

The Raman spectrum reveals two prominent peaks: one in the low-frequency region around 700 cm^{-1} and another in the high-frequency region around 970 cm^{-1}. These peaks correspond to the vibrational modes of the material being analysed, with their intensity indicating the relative abundance of the corresponding molecular vibrations. The low-frequency peak at 700 cm^{-1} is likely associated with the transverse optical (TO) phonon mode of the 4H-SiC substrate, involving the vibration of silicon and carbon atoms in opposite directions within the Si-C bonds. This peak's position and intensity can provide information about the crystal quality and strain in the SiC substrate. The high-frequency peak at 970 cm^{-1} is likely associated with the longitudinal optical (LO) phonon mode of the Si-O bonds in the SiO_2 layer, involving the vibration of silicon and oxygen atoms along the Si-O bond direction. This peak's position and intensity can provide information about the quality and thickness of the SiO_2 layer.

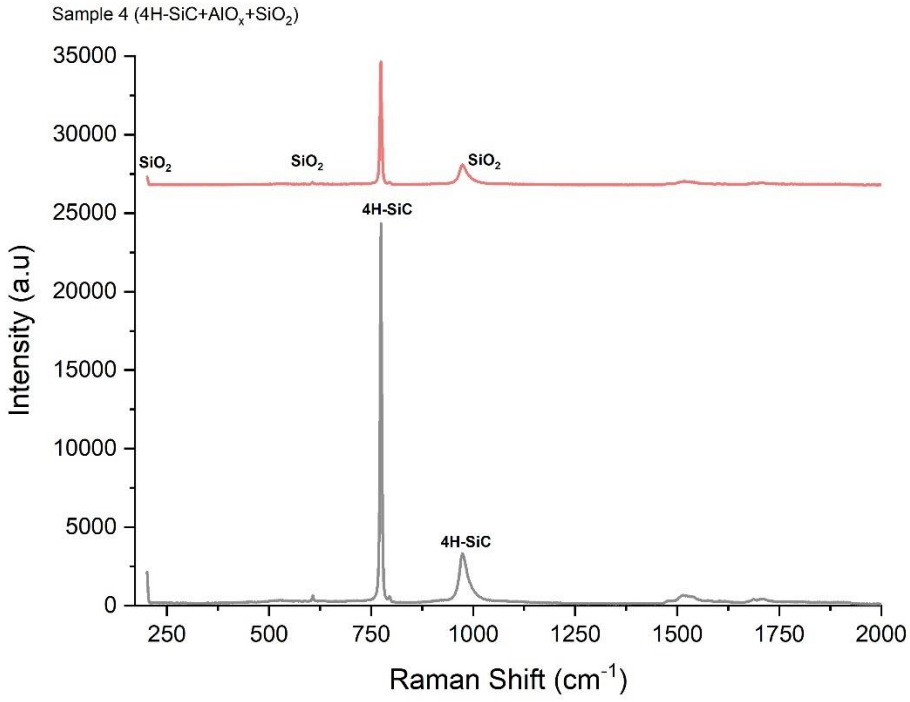


Figure 7.4 Raman spectrum of Sample 4 with different layers

The presence of these two distinct peaks indicates that the Raman spectrum is capturing the vibrational modes of both the 4H-SiC substrate and the SiO_2 layer, with the relative intensities of the peaks providing insights into the relative contributions of these two components to the overall Raman signal. Additionally, the quality of the Raman spectrum can be influenced by factors such as sample preparation, laser power, and exposure time. Comparing the spectrum to reference spectra of pure 4H-SiC and SiO_2 can help confirm the assignments of the observed peaks, and fitting the peaks with appropriate functions can provide quantitative information about the peak positions, widths, and intensities. The Raman peaks identified at 200 cm^{-1}, 760 cm^{-1}, 970 cm^{-1}, 1500 cm^{-1}, and 2700 cm^{-1} are characteristic of 4H-SiC (Silicon Carbide). The peak at 200 cm^{-1} is associated with the transverse acoustic (TA) phonon mode, indicating the fundamental vibrational properties of the SiC lattice. The 760 cm^{-1} peak corresponds to the transverse optical (TO) phonon mode, which signifies the Si-C bond vibrations within the crystal lattice. The 970 cm^{-1} peak relates to the longitudinal optical (LO) phonon mode, crucial for understanding the electronic properties of SiC. The peak around 1500 cm^{-1} can be attributed to second-order Raman scattering processes, providing insights into the anharmonic interactions within the crystal lattice. Lastly, the peak near 2700 cm^{-1} is often associated with overtones or combinations of fundamental phonon modes, offering information about the higher-energy vibrational states and complex interactions within the SiC crystal. Collectively,

these peaks help in characterizing the 4H-SiC material, providing valuable information about its vibrational, optical, and electronic properties[54, 222, 223]].

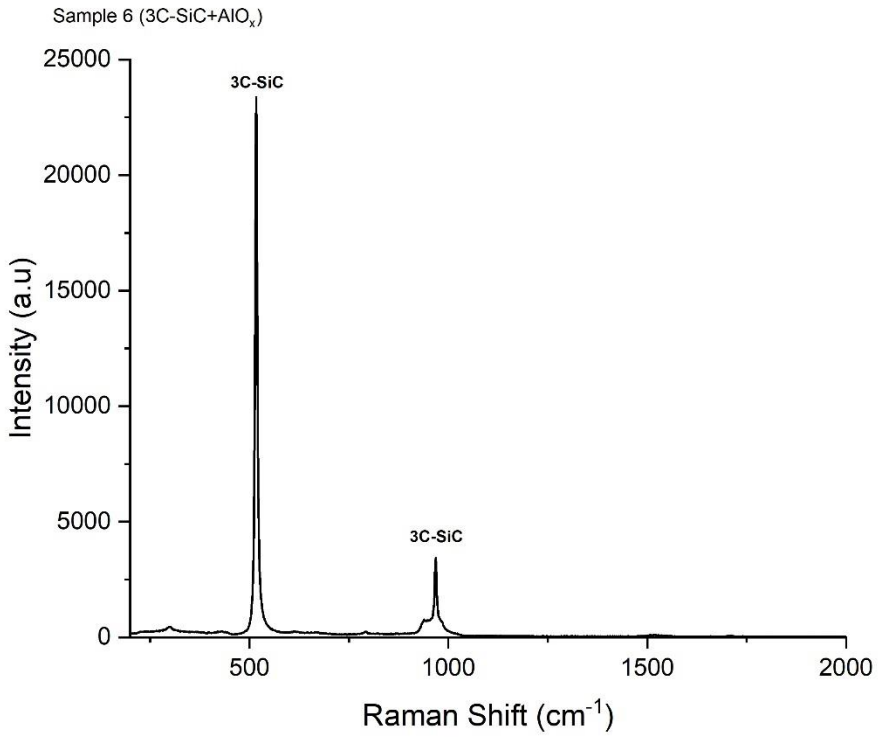


Figure 7.5 Raman spectrum of Sample 6

Based on the Raman spectroscopy graph, the prominent peak at 500 cm^{-1} is indicative of the transverse optical (TO) phonon mode, which is characteristic of 3C-SiC (Cubic Silicon Carbide). This peak is not typically prominent in 4H-SiC (Hexagonal Silicon Carbide), which usually shows significant peaks around 776 cm^{-1} (TO mode) and 796 cm^{-1} (LO mode). The presence of the 500 cm^{-1} peak, along with any additional peaks around 796 cm^{-1}, strongly suggests that the sample is 3C-SiC. These specific Raman peaks help in distinguishing between the 3C-SiC and 4H-SiC polytypes of Silicon Carbide, providing valuable insights into the material's vibrational and structural properties. Analysing the Raman spectrum of a 3C-SiC with Al_2O_3 deposited MOS channel provides valuable insights into the vibrational properties of the 3C-SiC substrate and the deposited Al_2O_3 layer. By examining the peak positions and intensities, we can gather information about the crystal quality, stress, and potential defects within the sample. The spectrum reveals key observations, such as the prominent SiC peaks at ~790 cm^{-1}, corresponding to the transverse optical (TO) phonon mode of 3C-SiC, and ~970 cm^{-1}, associated with the longitudinal optical (LO) phonon mode of 3C-SiC. The TO mode peak provides information about the crystal quality and strain in the SiC substrate, while the

LO mode peak, often weaker, can be sensitive to surface effects and interface quality. Additionally, the Al_2O_3 peaks, particularly the broad band in the 400-600 cm^{-1} range, are characteristic of amorphous Al_2O_3, arising from the vibrational modes of the Al-O bonds in the disordered structure. The exact position and shape of this band can vary depending on the specific composition and structure of the Al_2O_3 layer. The presence of sharp and well-defined peaks in the SiC region indicates a high-quality crystalline structure, while any broadening or shifting of these peaks could suggest defects or strain. The broad band in the Al_2O_3 region confirms the presence of amorphous Al_2O_3, with its intensity and shape providing information about the thickness, density, and potential crystallization of the Al_2O_3 layer. Additional considerations include the influence of the laser excitation wavelength on Raman scattering efficiency and observed peak intensities, as well as the impact of sample preparation, such as surface polishing and cleaning, on the quality of the Raman spectrum. Comparing the spectrum to reference spectra of pure 3C-SiC and Al_2O_3 can help confirm peak assignments and identify any potential impurities or defects.

7.2. Electrical Characterization Techniques

7.2.1. Capacitance-Voltage (CV) Measurements

Capacitance-Voltage (CV) analysis is a crucial technique for characterising the electrical properties of Metal-Oxide-Semiconductor (MOS) channels. This method provides valuable insights into the behaviour of the MOS structure, particularly the SiC/SiO_2 interface, which is critical for device performance. CV analysis involves measuring the capacitance of a MOS structure as a function of the applied voltage. By sweeping the voltage across the MOS capacitor and recording the corresponding capacitance, a CV curve is obtained. This curve reflects the changes in the charge distribution within the MOS structure, providing information about the interface states, doping concentration, and oxide quality. One of the primary uses of CV analysis in SiC MOS channels is to identify and quantify interface states and traps, which are localised energy states at the SiC/SiO_2 interface that can capture and release charge carriers, affecting the device's electrical characteristics. The presence of these states can be inferred from anomalies in the CV curve, such as shifts or peaks, which indicate the trapping and detraining of charges. Additionally, CV analysis can be used to determine the doping concentration and profile of the SiC MOS channel by analysing the capacitance in the depletion region. This information is crucial for understanding the channel's behaviour and optimising the doping process to achieve desired electrical properties. The quality of the gate oxide layer

in SiC MOS devices is critical for their performance and reliability, and CV analysis can reveal information about the oxide thickness, uniformity, and the presence of defects or impurities. For instance, a high density of oxide traps can lead to hysteresis in the CV curve, indicating instability in the device's threshold voltage. The threshold voltage of a MOSFET, which is the voltage required to invert the surface of the semiconductor and form a conductive channel, can also be determined from the CV curve [210, 224–227]]. This parameter is essential for the operation of MOS devices and can be influenced by factors such as doping concentration and interface quality. Furthermore, CV analysis can be used to study the effects of temperature on the electrical properties of SiC MOS channels, as temperature variations can impact the behaviour of interface states and traps, as well as the mobility of charge carriers. By performing CV measurements at different temperatures, researchers can gain insights into the thermal stability and performance of the device under various operating conditions. The insights gained from CV analysis are invaluable for the development and optimization of SiC MOS devices. By providing detailed information about the interface states, doping profile, oxide quality, and threshold voltage, CV analysis helps researchers and engineers to enhance device performance, optimise fabrication processes, and improve reliability. Understanding and mitigating interface states and traps can lead to improved electrical performance and stability, while detailed analysis of the doping profile and oxide quality helps in refining fabrication techniques to achieve better control over the device characteristics [180–182]. Identifying and addressing issues related to oxide traps and interface states can enhance the reliability and longevity of SiC MOS devices. In summary, CV analysis is a powerful tool for characterising the electrical properties of SiC MOS channels, providing comprehensive insights into the interface quality, doping profile, and overall performance of the device, which are crucial for advancing the development of high-performance, reliable SiC MOS devices for various high-power and high-temperature applications [54, 228]].

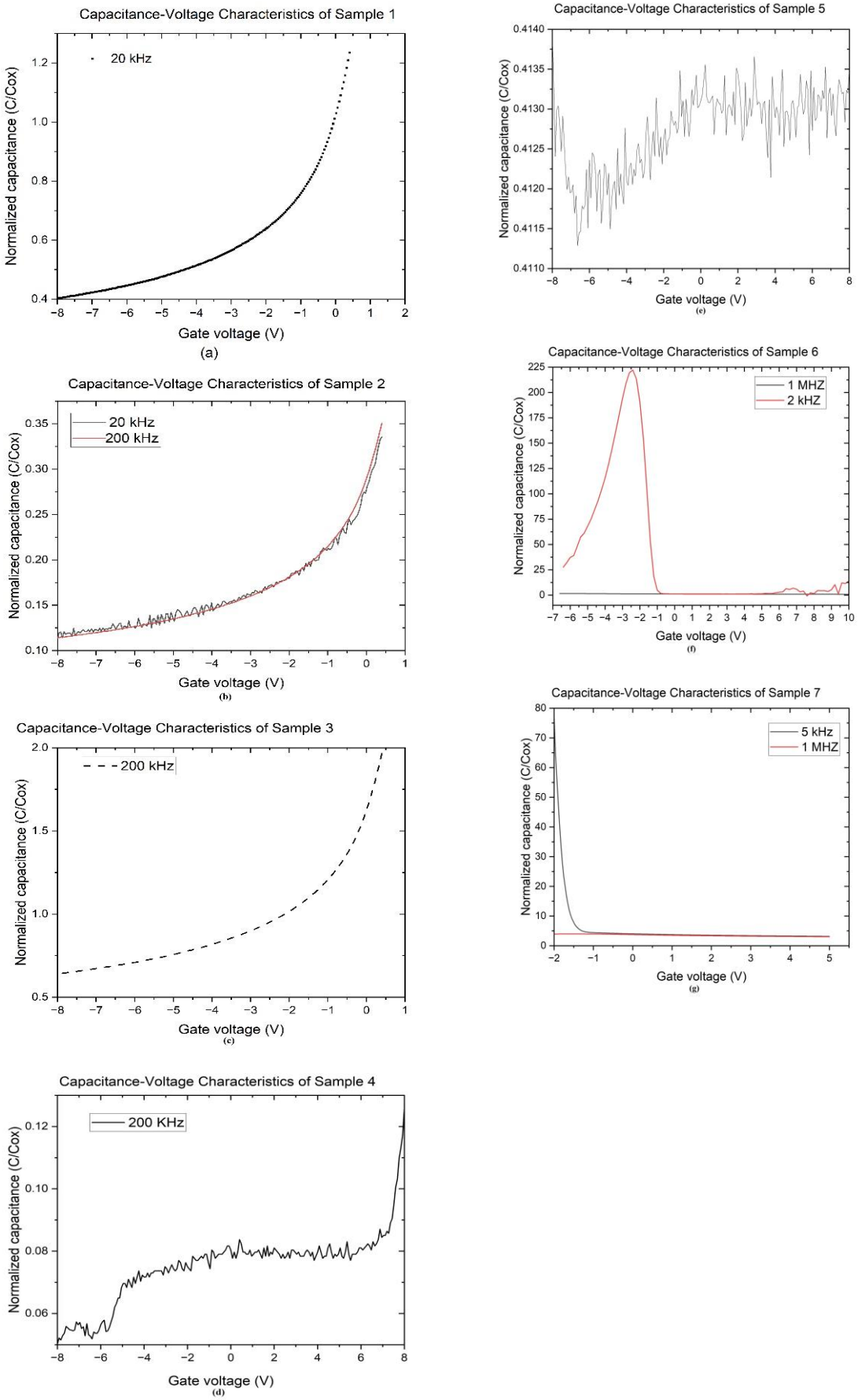


Figure 7.6 Capacitance (C) and gate voltage (Vg) of the (a) Sample 1 (b)Sample 2 (c) Sample 3 (d) Sample 4 (e) Sample 5 (f) Sample 6 (g) Sample 7

The Figure 7.6(a)shows the Capacitance-Voltage (C-V) characteristics of Sample 1, The curve exhibits a gradual, almost exponential rise as the gate voltage becomes less negative, reflecting a transition from the depletion region to the accumulation region. Measured at 20 kHz, the smooth nature of the curve suggests minimal frequency dispersion, indicative of a relatively clean SiC/dielectric interface with limited interface traps. At positive gate voltages, the capacitance approaches C_{ox}, signifying the formation of an accumulation layer in the n-epi channel. For negative gate voltages, the capacitance decreases smoothly, corresponding to the widening of the depletion region in the SiC substrate. The absence of a strong inversion region, characteristic of wide-bandgap materials like 4H-SiC, is due to the high activation energy of donor states in SiC, which limits the formation of an inversion layer under typical operating conditions. The TiO_2 layer, with its high dielectric constant, contributes to the high capacitance, while BN potentially influences the interface quality and smoothness of the curve.

Figure 7.6(b)illustrates the Capacitance-Voltage (C-V) characteristics of Sample 2. The curve shows smooth behaviour across the entire gate voltage range, with two frequency measurements (20 kHz and 200 kHz) nearly overlapping, indicating minimal frequency dispersion and suggesting good interface quality with limited charge trapping effects.

For negative gate voltages, the capacitance gradually increases, corresponding to a reduction in the depletion width of the SiC substrate. The absence of sharp transitions indicates stable charge distribution and effective control of the depletion region by the gate voltage. As the gate voltage becomes more positive, the capacitance continues to rise, reflecting the accumulation of charge carriers at the SiC/dielectric interface, characteristic of the accumulation region in MOS structures. The lack of inversion behaviour, as observed in other wide-bandgap materials like 4H-SiC, is due to the high activation energy of donor states, which prevents the formation of a strong inversion layer under normal operating conditions.

The dual dielectric stack of AlOx and BN influences the C-V characteristics. AlOx, with its moderate dielectric constant, provides reasonable capacitance values and good insulating properties, while BN, known for its layered structure, may introduce some interface effects or trapping mechanisms, though these appear minimal based on the smoothness of the curve. Compared to Sample 1, which uses TiO_2 as the primary dielectric, Sample 2 shows lower capacitance values but improved interface stability, as reflected by the lack of frequency dependence.

The Capacitance-Voltage (C-V) characteristics of Sample 3 represented by the figure7.6 (c), which consists of a 4H-SiC + n-epi substrate with a dual dielectric stack of AlOx and SiO_2 demonstrate a smooth and steady increase in normalized capacitance from approximately 0.5 at 8V to around 2.0 at +1V.

As the gate voltage transitions from negative to positive, the capacitance increases progressively, indicating a transition from the depletion region to the accumulation region. The smooth progression of the curve suggests stable dielectric properties and a high-quality interface between the SiC substrate and the dielectric layers. At positive gate voltages, the capacitance significantly exceeds Cox, reflecting the accumulation of charge carriers at the SiC/dielectric interface. This strong capacitive response is driven by the high dielectric constant of AlOx, which dominates the performance in the accumulation region. Conversely, at negative gate voltages, the capacitance decreases smoothly, indicating the widening of the depletion region in the n-epi layer. This behaviour is consistent with a well-functioning MOS structure, where the gate voltage effectively controls the depletion layer. As with other wide-bandgap materials like 4H-SiC, the C-V curve for Sample 3 does not display strong inversion behaviour at highly negative gate voltages due to the high activation energy of donor states in SiC, which limits the formation of an inversion layer.

The dual dielectric stack of AlOx and SiO_2 significantly enhances the dielectric performance of the sample. The high dielectric constant of AlOx increases the overall capacitance, particularly in the accumulation region, while SiO_2 contributes to improved interface quality and stability. This combination ensures minimal charge trapping and reduces frequency dispersion effects, as evidenced by the smoothness of the curve. Compared to Sample 1 (with TiO_2 and BN), Sample 3 exhibits higher capacitance and better dielectric properties due to the superior performance of AlOx and SiO_2.

The Figure 7.6 (d) shows the Capacitance-Voltage (C-V) characteristics of Sample 4, which consists of a 4H-SiC substrate with a dual dielectric stack of SiO_2 and AlOx, exhibit a gradual increase in normalized capacitance (C/Cox) as the gate voltage increases from −8 V to +8 V. Measured at 200 kHz, the C-V curve reveals a steady rise in capacitance alongside noticeable fluctuations, particularly in the mid-voltage range (−4 V to +4 V). These fluctuations are likely caused by interface-related phenomena such as charge trapping or trap-assisted tunnelling, which may arise from imperfections in the SiO_2/SiC interface or the AlOx layer.

At higher positive gate voltages (>6 V), the capacitance increases sharply, indicating the onset of charge carrier accumulation at the SiC/dielectric interface. This response highlights the role of the AlOx layer, whose high dielectric constant enhances the overall capacitive behaviour in the accumulation region. Conversely, at negative gate voltages (−8 V to 0 V), the capacitance increases gradually as the depletion region narrows, consistent with typical MOS behaviour. The steady rise in capacitance across the voltage range reflects the effectiveness of the dual-layer dielectric stack, although the fluctuations suggest room for improvement in interface quality.

The SiO_2 (40 nm) layer provides a high-quality insulating interface that stabilizes capacitance at lower voltages, while the AlOx (30 nm) layer enhances the capacitive response at higher voltages. Together, these materials offer a balance between good interface quality and increased capacitance, making the stack effective for high-power applications. Compared to Sample 3, which features a thinner SiO_2 layer, Sample 4 demonstrates a more gradual increase in capacitance and more noticeable fluctuations, likely due to the thicker SiO_2 layer's influence on the interface properties.

The Capacitance-Voltage (C-V) characteristics of Sample 5 denoted by figure 7.6 (e), composed of a 6H-SiC substrate with a single dielectric layer of AlOx (30 nm), exhibit a relatively flat capacitance response across the gate voltage range of −8 V to +8 V. The normalized capacitance remains within a narrow range of approximately 0.411 to 0.413, with no significant increase or decrease observed, indicating weak gate control over the charge carrier distribution in the depletion or accumulation regions. Small fluctuations in capacitance are evident throughout the voltage range, likely caused by interface traps, material defects, or inhomogeneities in the AlOx layer or at the AlOx/SiC interface. These fluctuations suggest the presence of localized charge trapping or trap-assisted tunnelling, which may affect the stability of the dielectric performance. The lack of pronounced accumulation or depletion behaviour highlights the limitations of the single-layer AlOx structure in effectively modulating the SiC surface charge. Unlike other samples with dual dielectric layers, such as SiO_2 + AlOx, Sample 5 does not demonstrate the characteristic capacitive modulation typically observed in well-designed MOS structures. While the wide bandgap and thermal conductivity of 6H-SiC provide inherent advantages, the absence of a secondary dielectric layer like SiO_2 limits the interface quality and capacitive response.

The Figure 7.6 (f) describe the Capacitance-Voltage (C-V) characteristics of Sample 6, composed of a 3C-SiC substrate with a single dielectric layer of AlOx (30 nm), display distinct and highly frequency-dependent behaviour across the gate voltage range of −7 V to +10 V. At 2 kHz, the capacitance shows a dramatic peak at −3V, with a normalized capacitance reaching approximately 225. This peak suggests strong charge accumulation or polarization effects at this specific gate voltage. However, at 1 MHz, the capacitance remains flat and near zero across the entire voltage range, indicating that the capacitive response is dominated by interface traps or slow-moving charge carriers. These carriers respond to low-frequency signals but fail to follow rapid voltage changes at higher frequencies.

Beyond the peak at −3 V, the capacitance decreases sharply to near-zero values as the gate voltage becomes more positive, reflecting a widening depletion region and the suppression of charge accumulation at the AlOx/3C-SiC interface. The absence of significant accumulation at higher positive voltages highlights the limitations of the single-layer AlOx dielectric and the challenges associated with the 3C-SiC substrate, including a lower bandgap and potential interface defects. The strong frequency dependence and the erratic nature of the capacitance curve suggest the presence of significant interface traps or defects that dominate the electrical behaviour, leading to charge trapping and release at low frequencies but reduced performance at high frequencies.

The Figure 7.6(g) shows the Capacitance-Voltage (C-V) characteristics of Sample 7, consisting of a 6H-SiC substrate with a single dielectric layer of SiO_2, demonstrate stable and well-behaved behaviour across the gate voltage range of −2 V to +5 V. The normalized capacitance (C/C ox) exhibits a sharp decrease near −2 V before stabilizing at low values across the remainder of the voltage range, indicating effective control of the depletion region in the 6H-SiC substrate. The nearly identical capacitance response at 5 kHz and 1 MHz reflects minimal frequency dependence, highlighting the high quality of the SiO_2 dielectric and the stable interface it forms with the 6H-SiC substrate. The lack of significant variation in capacitance at higher gate voltages further emphasizes the stability of the dielectric layer and its ability to maintain consistent charge modulation. Unlike conventional semiconductors, the C-V curve does not exhibit strong accumulation or inversion behaviours, consistent with the properties of wide-bandgap materials like 6H-SiC, where the high activation energy of donor states suppresses inversion formation. Compared to other samples, such as Sample 5 (which uses AlOx with 6H-SiC), Sample 7 shows far superior stability and minimal frequency dispersion, underscoring the advantages of SiO_2 as a dielectric layer. The flat capacitance response and

robust depletion characteristics make Sample 7 highly suitable for high-power and high-voltage applications, particularly in MOS structures requiring stable dielectric performance under varying electrical conditions.

The **Capacitance-Voltage (C-V) characteristics** of Samples 1 to 7 highlight a broad range of electrical behaviours driven by substrate material, dielectric composition, and interface quality. **Sample 1** (4H-SiC with TiO_2/BN) shows a gradual capacitance increase, reflecting moderate depletion and accumulation behaviour, but its performance is limited by interface challenges. **Sample 2** (4H-SiC with AlOx/BN) displays similar behaviour but benefits from improved stability due to AlOx. **Sample 3** (4H-SiC with AlOx/SiO_2) demonstrates strong and consistent capacitance with minimal frequency dispersion, highlighting the effectiveness of the dual dielectric stack, making it well-suited for high-power applications. **Sample 4** (4H-SiC with SiO_2/AlOx) exhibits a steady rise in capacitance but with fluctuations indicative of interface traps, showing potential for improvement. **Sample 5** (6H-SiC with AlOx) shows flat and constant capacitance with small fluctuations, indicating limited charge modulation due to the single-layer dielectric. **Sample 6** (3C-SiC with AlOx) presents a dramatic capacitance peak at low frequency, followed by a sharp drop and significant frequency dependence, suggesting severe interface challenges. In contrast, **Sample 7** (6H-SiC with SiO_2) exhibits stable and frequency-independent capacitance with excellent depletion characteristics, making it highly suitable for high-power and high-frequency applications. Overall, dual-layer dielectrics (e.g., AlOx/SiO_2) outperform single-layer ones (e.g., AlOx), and substrates like 6H-SiC and 4H-SiC provide superior stability compared to 3C-SiC. Samples 3 and 7 emerge as the most promising for high-performance applications, while Samples 5 and 6 require interface optimization to enhance their reliability.

7.2.2. Current density (J) and Electric field (E) and Current-Voltage (I-V) Measurements

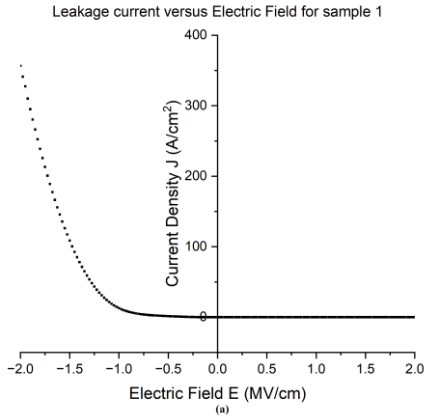
The Electric Field (E) vs Current Density (J) and Current-Voltage (I-V) measurements are fundamental techniques for characterizing the electrical properties of Silicon Carbide (SiC) Metal-Oxide-Semiconductor (MOS) channels. While I-V measurements involve applying a voltage across the device and analysing the resulting current to derive key electrical parameters, E-J measurements provide insights into the behaviour of the MOS structure under varying electric field strengths, particularly the leakage current characteristics.

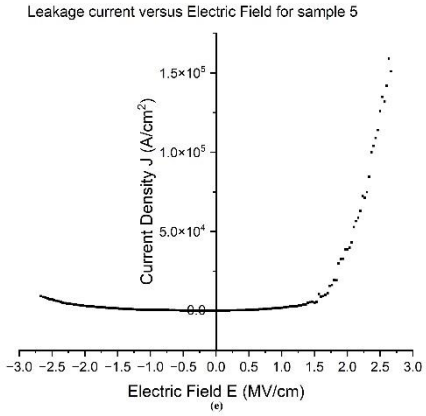
In E-J measurements, the relationship between the applied electric field and the leakage current density is examined. This is crucial for understanding the dielectric properties of the gate oxides and interface behaviour in SiC MOS devices. The E-J curve highlights important features such as the suppression of leakage current at specific field regions and the potential onset of conduction mechanisms, including tunnelling or charge injection. For SiC MOS channels, these measurements are particularly significant because of the high electric fields that SiC devices can endure, attributed to the material's wide bandgap and robust dielectric properties. E-J analysis also helps assess the quality of gate dielectrics, such as SiO_2, Al_2O_3, or multi-layered oxides, by quantifying leakage currents and identifying regions of breakdown or instability.

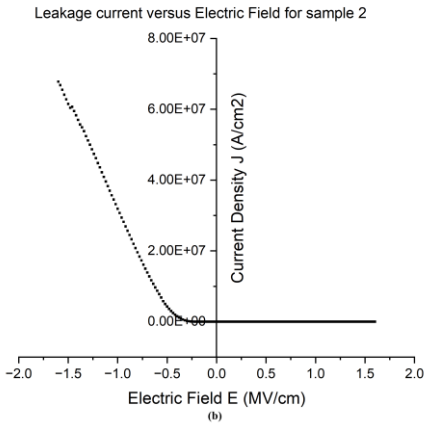
In parallel, I-V measurements remain critical for evaluating parameters like threshold voltage, on-resistance, and channel mobility. The I-V curve defines the linear (ohmic) and saturation regions of device operation. In the linear region, current increases proportionally with voltage, indicating the channel is fully open and the device behaves like a resistor. In the saturation region, current plateaus, showing that the channel is pinched off and the device operates as a current source. For SiC MOS devices, the threshold voltage the voltage required to form a conductive channel is influenced by doping, interface quality, and temperature. On-resistance, another key parameter, reflects the efficiency of the channel when fully open, directly impacting power losses and device performance[229]1..

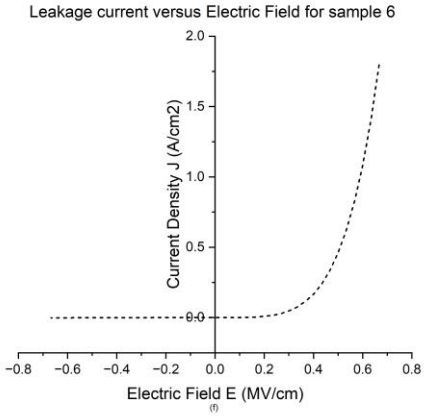
The Figure7.7 (a) graph illustrates the relationship between leakage current density (J) and electric field (E) for a 4H-SiC-based Metal-Oxide-Semiconductor featuring a 20 nm TiO2 gate dielectric and a 20 nm BN interfacial layer. The curve reveals a significant decrease in leakage current density as the electric field increases from -2.0 MV/cm toward 0 MV/cm. Initially, at negative electric fields, the current density is high, indicating substantial leakage, likely due to field-enhanced leakage mechanisms such as tunnelling or defect-related processes. As the electric field approaches zero, there is a sharp decline in current density, suggesting a reduction in leakage current, possibly due to the onset of a breakdown or a threshold electric field.

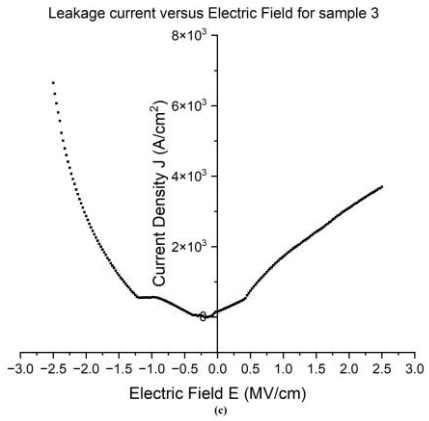
In the positive electric field region, the current density stabilizes at a relatively low level, indicating effective control over leakage currents. This behaviour suggests strong insulating properties of the MOS channel, likely attributed to the high dielectric constant of TiO2 and the additional insulating properties of BN.

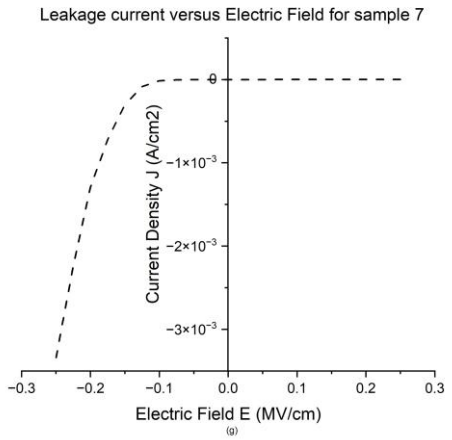












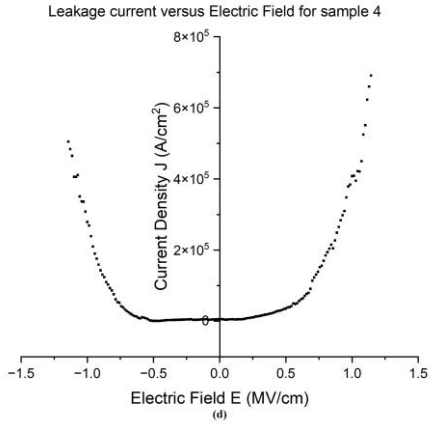


Figure 7.7 The gate current (Ig) and the gate voltage (Vg) of the Samp(a) Sample 1 (b)Sample 2 (c) Sample 3 (d) Sample 4 (e) Sample 5 (f) Sample 6 (g) Sample 7

The sharp reduction in leakage current near zero electric field highlights the effectiveness of the gate control in the MOS structure, while the low leakage in the positive field region reflects good dielectric integrity and minimal defect contribution. Conversely, the high leakage observed at negative fields may point to potential issues with material or interface quality that warrant further investigation. Overall, the graph underscores the effective leakage suppression capabilities of the layered structure in the SiC MOS channel.

The Figure 7.7 (b) depicts the leakage current density (J) as a function of the electric field (E) for Sample 2. The curve reveals a steep decrease in leakage current density as the electric field transitions from -2.0 MV/cm toward 0 MV/cm. Initially, at negative electric fields, the current density is extremely high, indicating significant leakage, possibly due to mechanisms such as tunnelling or defects in the material contributing to field-enhanced leakage. As the electric field approaches zero, the current density drops sharply, suggesting the presence of a threshold electric field where leakage current is significantly suppressed.

In the positive electric field region, the current density remains consistently low, indicating effective suppression of leakage current. This stabilization in the positive field region reflects the strong insulating properties of the MOS structure, likely due to the high dielectric constant of AlOx and the additional insulating layer of BN. The dramatic reduction in leakage current near 0 MV/cm suggests robust gate control and effective dielectric performance in this region.

The Figure7.7(c) shows the leakage current density (J) versus electric field (E) for Sample 3, consisting of a 4H-SiC substrate with an n-type epitaxial layer (n-epi), a 30 nm AlOx (Aluminium Oxide) layer, and a 10 nm SiO2 (Silicon Dioxide) layer.

The curve illustrates a distinct trend in leakage current density. At negative electric fields, the current density is initially high but decreases as the electric field moves toward 0 MV/cm. This decrease suggests that leakage mechanisms such as tunnelling or defect-related conduction dominate in the negative field region. The current density reaches a minimum near -0.5 MV/cm, indicating a point where leakage is at its lowest.

As the electric field becomes positive, the current density starts increasing again, displaying a distinct upward trend beyond 0 MV/cm. This increase suggests the onset of a different conduction mechanism in the positive field region, possibly due to field-induced charge injection or other dielectric breakdown phenomena.

The presence of both AlOx and SiO2 layers likely contributes to the observed leakage characteristics. AlOx, with its high dielectric constant, provides strong insulation, while the SiO2 layer offers additional dielectric stability. However, the rise in leakage current in the positive field suggests potential challenges in dielectric integrity or interface effects between the layers. Sample 3 exhibits a complex leakage behaviour, with a clear minimum in leakage current at moderate negative fields and a subsequent increase in leakage with rising positive electric fields. This behaviour indicates effective leakage suppression at moderate fields but suggests possible issues with dielectric performance or charge injection at higher positive fields.

Figure7.7(d) shows the relationship between leakage current density (J) and electric field (E) for a 4H-SiC-based Metal-Oxide-Semiconductor of sample 4, the material stack comprises 4H-SiC as the substrate, along with dielectric layers of 40 nm SiO_2 and 30 nm AlOx (aluminum oxide). The symmetry of the curve suggests balanced electrical behaviour under both polarities of the applied electric field, implying that the conduction mechanisms are not influenced by asymmetry in the material or interfaces. The rise in current density at higher fields, both positive and negative, points to a sharp increase in leakage, possibly due to dielectric breakdown or tunnelling mechanisms.

Compared to the earlier graph, Figure7.7(c) for Sample 3, this plot demonstrates a different leakage behaviour. While Sample 3 exhibited asymmetry between positive and negative fields, Sample 4 shows a more uniform response, indicating potentially better fabrication uniformity or fewer interface-related defects. The current density in Sample 4 also appears to remain lower across the range of electric fields, suggesting improved insulating properties of the dielectric stack. The results for Sample 4 highlight the importance of the SiO_2 and AlOx layers in controlling leakage current. The material's performance in symmetric fields and its resistance to leakage at moderate fields suggest its suitability for high-voltage applications in electronic devices.

The leakage current behaviour of Sample 5 represented by the figure7.7 (e), composed of 6H-SiC with a 30 nm AlOx dielectric layer, exhibits notable asymmetry. In the positive electric field region, the current density increases sharply at higher fields, indicating the onset of significant leakage and potential dielectric breakdown. In contrast, the negative field region shows minimal current density variation, reflecting an asymmetric conduction mechanism likely influenced by charge trapping, carrier injection differences, or interface effects. This

behaviour contrasts with the more symmetric response observed in Sample 4, where 4H-SiC and a dual dielectric stack were used. The use of 6H-SiC, which has a slightly lower bandgap than 4H-SiC, contributes to this behaviour by facilitating higher carrier injection at the interface with AlOx under a positive electric field, leading to an enhanced electric field.

Furthermore, the absence of a SiO_2 layer in Sample 5 removes additional charge trapping mechanisms that might have suppressed leakage in the negative field region. This results in a steeper rise in leakage current density under positive fields and a lower overall breakdown threshold. The material choice of 6H-SiC, while advantageous for high-power and high-frequency applications due to its thermal stability and high breakdown field strength.

The Figure7.7(f) illustrates the relationship between leakage current density and electric field for a sample 6 consisting of 3C-SiC as the substrate with a 30 nm AlOx dielectric layer and a sample size of 2.5 mm x 2.5 mm. The behaviour of the leakage current is highly asymmetric, with negligible current density in the negative electric field region and a sharp, exponential increase in current density in the positive field region beyond approximately 0.4 MV/cm. This asymmetry indicates a strong insulation capability under negative fields but a rapid onset of significant conduction under positive bias, likely due to dielectric breakdown or tunnelling mechanisms through the AlOx layer.

The use of 3C-SiC, which has a lower bandgap compared to 4H-SiC and 6H-SiC, plays a critical role in this behaviour by facilitating greater charge injection under positive electric fields. This material property, combined with the absence of a dual dielectric stack (as seen in previous samples), makes AlOx the sole insulating layer, which may lead to earlier leakage onset under positive bias. The interface between 3C-SiC and AlOx likely introduces defect states or band alignment issues that exacerbate the asymmetry in conduction, favouring higher leakage in the positive field region.

The smaller sample size (2.5×2.5 mm) reduces the absolute leakage current, but this does not diminish the exponential rise in current density observed at higher positive fields. The strong asymmetry in leakage behaviour suggests that the conduction mechanism is highly dependent on field polarity, likely influenced by interface properties and material characteristics. While Sample 6 exhibits excellent insulating properties for negative electric fields, its steep leakage current increase under positive fields limits its utility in applications requiring high positive bias tolerance.

The figure7.7(g) illustrates the relationship between leakage current density (J) and electric field (E) for a sample 7 consisting of **6H-SiC** as the substrate with a 40 nm SiO_2 dielectric layer. The leakage current behaviour exhibits significant asymmetry between positive and negative electric fields. In the negative electric field region, the current density increases in magnitude sharply and reaches a saturation point near -3×10^{-3} A/cm^2. This behaviour suggests that charge conduction stabilizes under higher negative fields. In contrast, under positive electric fields, the current density remains almost constant and very close to zero, reflecting excellent insulating properties. The SiO_2 layer effectively blocks charge conduction under positive bias, maintaining extremely low leakage levels.

The material properties of 6H-SiC, such as its wide bandgap and high breakdown field strength, contribute to the sample's strong insulation capabilities. The 40 nm SiO_2 dielectric layer further enhances this performance by providing a robust insulating barrier, particularly under positive electric fields. However, the pronounced asymmetry in leakage behaviour between positive and negative fields may result from differences in the charge injection mechanisms or interface trap-mediated conduction at the SiC/SiO_2 interface under opposite field polarities. This behaviour highlights the role of interface engineering in optimizing device performance.

Table 7.1performance summery of the samples

Sample	Dielectric Stack	Leakage Current Behaviour	Breakdown Voltage (V)	Capacitance-Voltage Observations
1	TiO_2 (20 nm) + BN (20 nm)	High leakage under negative fields; asymmetric behaviour with TiO_2 contributing to higher conduction.	~6 V	Gradual increase in capacitance with increasing gate voltage; lacks strong suppression of leakage effects.
2	AlOx (30 nm) + BN (20 nm)	Moderate leakage; higher than SiO_2-based stacks due to BN's contribution.	~5V	Similar to Sample 1 but with slightly better capacitance-voltage behaviour due to AlOx; capacitance varies with frequency.
3	AlOx (30 nm) + SiO_2 (10 nm)	Balanced leakage; moderate suppression due to the addition of SiO_2.	~10 V	Capacitance increases steadily with gate voltage; shows moderate insulation performance compared to pure AlOx samples.
4	SiO_2 (40 nm) + AlOx (30 nm)	Strong insulation; symmetrical and low leakage under high fields.	~8.4 V	Excellent capacitance behaviour; remains stable with increasing gate voltage; significant improvement due to SiO_2.
5	AlOx (30 nm)	Steep leakage rise under positive fields; limited by single-layer AlOx.	~7.5V	Capacitance increases rapidly at higher gate voltages, reflecting early onset of leakage.
6	AlOx (30 nm)	High leakage; early onset of breakdown due to 3C-SiC and single-layer AlOx limitations.	~1.8 V	Capacitance peaks sharply at lower voltages but rapidly degrades, indicating poor insulation at higher gate voltages.

7	SiO_2 (40 nm)	Excellent insulation; negligible leakage under positive fields.	~1V	Very stable capacitance; minimal variation with gate voltage across frequencies, showing strong dielectric performance.

The Table 7.1 represents the analysis of the dielectric stacks and their electrical performance across the samples provides critical insights into the trade-offs between leakage current behaviour, breakdown voltage (BV), and capacitance-voltage (C-V) characteristics.

1. **Leakage Current Behaviour**:
    - Samples with **SiO_2** as a dielectric layer (e.g., Samples 4 and 7) demonstrated superior insulation with significantly reduced leakage current, even under high electric fields. In contrast, stacks containing **BN** (e.g., Samples 1 and 2) or single-layer **AlOx** (Samples 5 and 6) exhibited higher leakage, particularly under negative or high fields. The inclusion of SiO_2 in the stack (Samples 3 and 4) effectively suppressed leakage, highlighting its role as a reliable insulator.
2. **Breakdown Voltage (BV)**:
    - The highest breakdown voltage was observed in **Sample 3** (10 V) due to the balanced combination of **AlOx** and **SiO_2**, showcasing the benefit of dual-dielectric stacks. However, single-layer dielectrics like **AlOx** (Samples 5 and 6) had lower breakdown voltages (7.5 V and 1.8 V, respectively), with Sample 6 further limited by the **3C-SiC substrate**. **Sample 7**, with **SiO_2**, exhibited excellent insulation but a lower breakdown voltage (1 V), likely due to its thinner stack.
3. **Capacitance-Voltage (C-V) Observations**:
    - **Samples 4 and 7**, with **SiO_2**, exhibited stable capacitance with minimal frequency dependence, making them ideal for applications requiring consistent dielectric behaviour. Samples containing **BN** (Samples 1 and 2) displayed less stable capacitance with notable variations, while single-layer **AlOx** (Samples 5 and 6) showed poor insulation and sharp capacitance peaks or early degradation.
4. **Performance Trends**:

- **Dual-dielectric stacks** (Samples 3 and 4) outperformed single-layer stacks by combining the high permittivity of **AlOx** with the strong insulating properties of **SiO_2**. This combination provided balanced leakage suppression and breakdown strength, as seen in Sample 4 with a BV of 8.4 V and excellent C-V stability.

  Single-layer AlOx (Samples 5 and 6) was limited by poor leakage suppression and early breakdown, emphasizing the need for additional layers or improved interface engineering.

BN-containing stacks (Samples 1 and 2) showed higher leakage due to BN's relatively weaker insulating properties, although **Sample 2** benefited from the addition of AlOx. [39, 121, 208]

8. Summary

8.1. Conclusion

In this thesis we studied various aspects of SiC power devices. A thorough literature review of Silicon Carbide materials, devices and applications was provided in the opening chapters. This was followed by a TCAD simulation of a high voltage SiC JFET devices which achieved a breakdown voltage of 1.35kV with very low on resistance of 3.3 $m\Omega.cm^2$. In this project existing commercially available SiC MOSFETs were also examined in order to understand their design to feed this into my own MOS capacitor designs. In the final chapter I presented work on several different MOS capacitor designs. These included different SiC polytypes, including 4H-SiC, 6H-SiC and 3C-SiC. The investigation also included a variety of different dielectrics to try to resolve some of the issues experienced by thermally grown silicon dioxide. The dielectrics were deposited either by atomic layer deposition or magnetron sputtering. The dielectrics explored were silicon dioxide (SiO_2), aluminium oxide (AlO_x), boron nitride (BN), titania (TiO_2). These samples were then investigated through a variety of electrical and other characterisation techniques. The electrical techniques used were I-V and C-V measurements. The other characterisation techniques included Raman and XRD which was able to verify the constituent materials used in fabricating the MOS capacitors. This work provides insights into alternative dielectrics and alternative deposition techniques to thermally grown silicon oxide for SiC MOSFET devices. Through these alternatives it is conceivable that performance benefits could be gained. Also in future work, the investigations into existing SiC MOSFETs could be continued through power cycling experiments followed by detailed investigation to understand any physical impact to the devices. The TCAD work could also be continued through simulating the different dielectrics and trying to match experimental results with the simulated results, to create robust predictive models.

The analysis of dielectric stacks reveals critical trade-offs between leakage current behavior, breakdown voltage (BV), and capacitance-voltage (C-V) characteristics. **SiO_2-based stacks** (e.g., Samples 4 and 7) demonstrated superior insulation with significantly reduced leakage current, even under high electric fields, making them highly reliable insulators. In contrast, stacks containing **BN** (Samples 1 and 2) or single-layer **AlOx** (Samples 5 and 6) exhibited higher leakage, particularly under negative or high fields, highlighting their limitations.

The highest **Breakdown Voltage (BV)** was observed in **Sample 3** (10 V), attributed to the balanced combination of **AlOx and SiO_2**, emphasizing the advantage of dual-dielectric stacks.

Single-layer dielectrics like AlOx (Samples 5 and 6) had lower breakdown voltages (7.5 V and 1.8 V, respectively), with Sample 6 further limited by the 3C-SiC substrate. While **Sample 7**, with SiO_2, exhibited excellent insulation, its breakdown voltage (1 V) was lower due to the thinner dielectric stack.

In terms of **C-V behavior**, Samples 4 and 7, with SiO_2, demonstrated stable capacitance and minimal frequency dependence, making them ideal for consistent dielectric performance. BN-containing stacks (Samples 1 and 2) showed less stable capacitance with notable variations, while single-layer AlOx (Samples 5 and 6) exhibited sharp capacitance peaks or early degradation, indicating poor insulation.

Overall, **dual-dielectric stacks** (e.g., AlOx + SiO_2 in Samples 3 and 4) outperformed single-layer dielectrics by providing balanced leakage suppression, higher breakdown strength, and stable capacitance. Single-layer AlOx and BN-based stacks displayed higher leakage and limited reliability, underscoring the importance of combining dielectrics for enhanced performance.

8.2. Recommendations

- Based on my findings, I recommend photolithography for determining the surface area of the point contact and thermal evaporation as a more precise method for contact deposition compared to magnetron sputtering.
- To prevent Al evaporation during the sintering process at 670°C, consider reducing the sintering temperature, using a protective capping layer, shortening the sintering time, or exploring alternative metallization materials with higher melting points. These strategies can help ensure optimal sintering results while minimizing Al evaporation and maintaining the integrity of the MOS capacitor.
- I suggest performing XRD or SEM analysis after each deposition step during the fabrication process to assess the quality and abundance of the deposited materials. This approach can provide valuable insights into the effectiveness of the deposition techniques and help identify any potential issues early on.
- In this study, the fabrication of the MOS capacitor was carried out using Atomic Layer Deposition (ALD), Magnetron Sputtering, and Thermal Evaporation processes to form the gate oxide, metal contacts, and other layers. However, the fabrication process did not include photolithography for defining the gate mask, resulting in manually

controlled gate dimensions. While the deposition techniques employed were effective for creating high-quality thin films, the absence of photolithography limited the precision and uniformity of the gate structure, which are critical for ensuring consistent and predictable device performance. For future studies, it is strongly recommended to incorporate photolithography into the fabrication process. Photolithography offers enhanced precision by enabling accurate definition of gate dimensions and alignment with other device features, as well as improved uniformity and reproducibility by ensuring consistent gate structures across multiple devices. Furthermore, it is highly compatible with advanced deposition techniques like ALD, Magnetron Sputtering, and Thermal Evaporation, facilitating the fabrication of more sophisticated MOS structures with precise control over layer geometry. By integrating photolithography with these deposition techniques, future work can achieve greater precision, reproducibility, and scalability in MOS device fabrication. This would enable a more comprehensive investigation into the relationship between gate dimensions and the electrical performance of MOS capacitors, particularly on SiC substrates.

8.3. Future Works

Once the necessary risk assessments and approvals are obtained, the designed circuit will be employed to conduct power cycling tests on the C3M0065090J SiC MOSFET. During these tests, critical parameters like gate-source voltage, drain-source voltage, drain current, and junction temperature will be closely monitored. Post-test, a thorough analysis of the device's performance, including changes in on-resistance, gate charge, and switching losses, will be performed. This analysis will help identify any degradation mechanisms, such as thermal cycling fatigue or electromigration. Insights gained from these tests will be instrumental in optimizing the design and operation of SiC power devices, ultimately improving their reliability and longevity. By undertaking these future studies, a deeper understanding of the long-term reliability and degradation mechanisms of SiC power devices can be achieved, accelerating the advancement and application of SiC technology in various power electronics systems.

Future research should focus on further optimizing dual-dielectric stacks, particularly combinations of **AlOx and SiO_2**, to achieve even better leakage suppression and breakdown voltage. Increasing the thickness of SiO_2 in such stacks could enhance the overall dielectric performance without compromising capacitance stability.

To address limitations observed in single-layer dielectrics, especially **AlOx** (Samples 5 and 6), advanced interface engineering techniques should be employed. Techniques like plasma treatments, surface passivation, or adding interfacial layers can help minimize trap states and reduce leakage current.

New dielectric materials with high permittivity and strong insulating properties, such as **HfO_2**, could be investigated to replace or complement existing materials like AlOx and BN. These materials may provide better trade-offs between leakage current, breakdown voltage, and capacitance stability.

Beyond dual-layer stacks, multi-layer configurations combining materials like **SiO_2, AlOx, and high-k dielectrics** could be studied to explore the synergy of multiple materials. These configurations might achieve superior insulation and greater stability under high electric fields.

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Appendix 1

These are the synopsis use to Simulate the 4H- SiC JFET

```
SDE
(define depth @depth@)
(define EpiDoping @EpiDoping@)
(sdegeo:create-rectangle (position 1.6 0 0)  (position 2.3 1 0) "SiliconCarbide" "region_N+source")
(sdegeo:create-polygon (list  (position 1.05 1 0)  (position 2.3 1 0)  (position 2.3 depth 0)  (position 0 depth 0)  (position 0 3.1 0)  (position 1.05 3.1 0)  (position 1.05 1 0) ) "SiliconCarbide" "region_ndrift")
(sdegeo:create-rectangle (position 0 3.1 0)  (position 1.05 3.2 0) "SiliconCarbide" "region_P++gate")
(sdegeo:create-rectangle (position 0 15.75 0)  (position 2.3 16.75 0) "SiliconCarbide" "region_Nsub")
(sdegeo:define-contact-set "source" 4  (color:rgb 1 0 0 ) "##")
(sdegeo:define-contact-set "drain" 4  (color:rgb 1 0 0 ) "##")
(sdegeo:define-contact-set "gate" 4  (color:rgb 1 0 0 ) "##"
(sdegeo:set-current-contact-set "source")
(sdegeo:set-contact-edges (list (car (find-edge-id (position 1.7 0 0)))) "source")
(sdegeo:set-current-contact-set "drain")
(sdegeo:set-contact-edges (list (car (find-edge-id (position 0.95 16.75 0)))) "drain")
(sdegeo:set-current-contact-set "gate")
(sdegeo:set-contact-edges (list (car (find-edge-id (position 0.505 3.1 0)))) "gate")
## (sdeio:save-tdr-bnd (get-body-list) "SiCJFET_1_2kV_version1.tdr")
(sdedr:define-constant-profile "ConstantProfileDefinition_Nsub" "PhosphorusActiveConcentration" 1e19)
(sdedr:define-constant-profile-region "ConstantProfilePlacement_Nsub" "ConstantProfileDefinition_Nsub" "region_Nsub")
(sdedr:define-constant-profile "ConstantProfileDefinition_ndrift" "PhosphorusActiveConcentration" EpiDoping)
(sdedr:define-constant-profile-region "ConstantProfilePlacement_ndrift" "ConstantProfileDefinition_ndrift" "region_ndrift")
(sdedr:define-constant-profile "ConstantProfileDefinition_N+source" "PhosphorusActiveConcentration" 1e19)
(sdedr:define-constant-profile-region "ConstantProfilePlacement_N+source" "ConstantProfileDefinition_N+source" "region_N+source")
 (sdedr:define-constant-profile "ConstantProfileDefinition_P++gate" "AluminumActiveConcentration" 9e19)
(sdedr:define-constant-profile-region "ConstantProfilePlacement_P++source" "ConstantProfileDefinition_P++gate" "region_P++gate")
(sdedr:define-refeval-window "RefEvalWin_horizP+" "Line"  (position 0 3.1 0) (position 1.05 3.1 0))
(sdedr:define-analytical-profile-placement  "AnalyticalProfilePlacement_P+_horizontalgate1"  "AnalyticalProfileDefinition_1"  "RefEvalWin_horizP+"  "Both"  "NoReplace"  "Eval")
(sdedr:define-gaussian-profile "AnalyticalProfileDefinition_1" "AluminumActiveConcentration" "PeakPos" 0  "PeakVal" 1e18 "ValueAtDepth" 1.8e16 "Depth" 0.65 "Gauss"  "Factor" 0.6)
(sdedr:define-refeval-window "RefEvalWin_vertP+" "Line" (position 1.05 1 0) (position 1.05 3.1 0))
(sdedr:define-analytical-profile-placement  "AnalyticalProfilePlacement_P+_verticalgate1"  "AnalyticalProfileDefinition_2"  "RefEvalWin_vertP+"  "Both"  "NoReplace"  "Eval")
(sdedr:define-gaussian-profile "AnalyticalProfileDefinition_2" "AluminumActiveConcentration" "PeakPos" 0  "PeakVal" 1e18 "ValueAtDepth" 1.8e16 "Depth" 0.4 "Gauss"  "Factor" 0.2)
(sdedr:define-refeval-window "RefEvalWin_global" "Polygon" (position 1.05 1 0)  (position 2.3 1 0)  (position 2.3 15.75 0)  (position 0 15.75 0)  (position 0 3.1 0)  (position 1.05 3.1 0)  (position 1.05 1 0))
(sdedr:define-refinement-size "RefinementDefinition_global" 0.3 0.3 0.2 0.2)
(sdedr:define-refinement-placement "RefinementPlacement_ndrift" "RefinementDefinition_ndrift" (list "window" "RefEvalWin_global"))
(sdedr:define-refinement-size "RefinementDefinition_ndriftregion" 0.05 0.05 0.01 0.01)
(sdedr:define-refinement-placement "RefinementPlacement_1" "RefinementDefinition_ndriftregion" (list "region" "region_ndrift" ))
(sdedr:define-refinement-function "RefinementDefinition_ndriftregion" "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-function "RefinementDefinition_ndriftregion" "MaxLenInt" "SiliconCarbide" "SiliconCarbide" 1e-4 1.4 "DoubleSide")
(sde:build-mesh "snmesh" "-a -c boxmethod" "basic_struc1_8.tdr")
# ;reflect the device
```

```
# (system:command "tdx -mtt -X n1_msh.tdr n1_msh_mirr.tdr")


>(sdegeo:set-auto-region-naming OFF)
>(sdegeo:create-rectangle (position 0.525926 -3.153572 0)  (position 0.455803 -0.594354 0) "Aluminum" "Back_Contact_Al")
>(sdegeo:create-rectangle (position 1 0 0)  (position 5 0.0001 0) "Aluminum" "Back_Contact_Al")
>(sdegeo:create-rectangle (position 0 0.0001 0)  (position 6 0.3501 0) "4HSiC" "4H_SiC_")
 >(sdegeo:create-rectangle (position 0 0.3501 0)  (position 6 0.3511 0) "SiC_4H" "4H_SiC_Buffer")
>(sdegeo:create-rectangle (position 0 0.3511 0)  (position 6 0.3611 0) "SiC_4H" "4H_SiC_Epi_Layer")
>(sdegeo:create-rectangle (position 0 0.3611 0)  (position 6 0.36115 0) "SiO2" "SiO2_dielectric_layer")
>(sdegeo:create-rectangle (position 0 0.36115 0)  (position 6 0.36118 0) "Oxide" "AlOx_Layer")
>(sdegeo:create-rectangle (position 1 0.36118 0)  (position 5 0.38618 0) "Aluminum" "frant_Contact_Al")


Sdevice 1
File {
        Grid=          "basic_struc1_8_msh.tdr"
        Parameter= "pp4_des.par"
        Plot=          "@tdrdat@"
        Current=   "@plot@"
        Output=      "@log@"
}
Electrode {
        { Name = "gate" Voltage= (0.0 at 0, -20 at 1) WorkFunction= 5.01} ## Increased to -20V - this is what is used in the UnitedSiC devices
        ## { Name = "gate_mirrored" Voltage= (0.0 at 0, -4 at 1) WorkFunction= 5.01}
        { Name = "source" Voltage= 0.0}
        { Name = "drain" Voltage= (0.0 at 1, 2000 at 10000) Resist= 1E8}
}



Physics {

        Recombination (
                SRH(DopingDep TempDep)
                Auger
                Avalanche(OkutoCrowell )
                ConstantCarrierGeneration (value = @CarrierBG@)
                )

        Aniso       (
                eMobilityFactor (Total) = 0.83
                hMobilityFactor (Total) = 1.00
                )

        Mobility (
                DopingDependence
                HighFieldSaturation
                Enormal
        )

        ## IncompleteIonization
        EffectiveIntrinsicDensity ( oldSlotboom NoFermi)
}
##
Math {
        ExtendedPrecision(@precision@)
        Iterations= 15
        Notdamped= 1000
        eDrForceRefDens= 1
        hDrForceRefDens= 1
        Digits= 5
        ErrRef(electron) = 1
        ErrRef(hole) = 1
        Extrapolate
        Transient= BE
        TensorGridAniso

        RHSmin= 1e-30
        RHSmax= 1e30
        RHSFactor= 1e30
        CDensityMin= 1e-30

        ParallelToInterfaceInBoundaryLayer(FullLayer -ExternalBoundary)
    eMobilityAveraging= ElementEdge
    hMobility veraging= ElementEdge
        ElementAvalancheMinAngle=
        number_of_threads= 8
        Method= ILS(set= 5)
        ILSrc= "
                set (5) {
                iterative(gmres(100), tolrel=1e-10, tolunprec=1e-4, tolabs=0, maxit=200);
                preconditioning(ilut(1.5e-6,-1), right);
                ordering(symmetric=nd, nonsymmetric=mpsilst);
                options(compact=yes, linscale=0, refineresidual=60, verbose=0);
                };
```

```
                        "
                BreakCriteria{Current (Contact="drain" absval= 1e-7)}
                ExitOnFailure
}
Plot {
  TotalCurrentDensity/vector
  eDensity hDensity
  eCurrent hCurrent
  ElectricField/vector
  eQuasiFermi hQuasiFermi
  egradQuasiFermi hgradQuasiFermi
  Potential Doping SpaceCharge
  SRH Auger
  AvalancheGeneration
  eAvalanche hAvalanche
  eMobility hMobility
  DonorConcentration AcceptorConcentration
  Doping
  eVelocity hVelocity
  BarrierTunneling
  ConductionBandEnergy ValenceBandEnergy BandGap
  eQuasiFermi hQuasiFermi
  NonLocal
}
Solve {
                Coupled(Iterations= 10000 LineSearchDamping= 1e-4){ Poisson }
                Coupled(Iterations= 10000 LineSearchDamping= 1e-4){ Poisson Electron Hole}
                Transient (
                        InitialTime= 0 InitialStep= 1e-8 Minstep = 1e-10 Increment= 1.4 Decrement= 2
                        Maxstep= 1000 FinalTime= 10000
                        ){ Coupled { Poisson Electron Hole } }
}
######################################################################
Sdevice 2
## Id Vgs for SiC JFET
Electrode {
                { Name="source" Voltage= 0.0 }
                { Name="gate"  Voltage= (0 at 0, -15 at 3, 0 at 13)}
                { Name="drain" Voltage= (0 at 0, 5 at 3, 5 at 13)}
                }
File            {
                Grid="basic_struc1_8_msh.tdr"
                Parameter="pp4_des.par"
                Plot="@tdrdat@"
                Current="@plot@"
                Output="@log@"
                }
Physics {
                Recombination               (
                        SRH(DopingDep TempDep)
                        Auger
                        ConstantCarrierGeneration (value = 1e8)
                        )
                Aniso                       (
                        eMobilityFactor (Total) = 0.83
                        hMobilityFactor (Total) = 1.00
                        )
                Mobility (
                        DopingDependence
                        HighFieldSaturation
                        Enormal
                        )
                EffectiveIntrinsicDensity (oldSlotboom NoFermi)
                }

Plot            {
                TotalCurrentDensity/vector
                eDensity hDensity
                eCurrent hCurrent
                ElectricField/vector
                eQuasiFermi hQuasiFermi
                egradQuasiFermi hgradQuasiFermi
                Potential Doping SpaceCharge
                SRH Auger
                AvalancheGeneration
                eAvalanche hAvalanche
                eMobility hMobility
                DonorConcentration AcceptorConcentration
                Doping
                eVelocity hVelocity
                BarrierTunneling
                ConductionBandEnergy ValenceBandEnergy BandGap
                eQuasiFermi hQuasiFermi
                NonLocal
                }
```

```
Math        {
            ExtendedPrecision(80)
            Iterations= 15
            Notdamped= 1000
            eDrForceRefDens= 1
            hDrForceRefDens= 1
            Digits= 5
            ErrRef(electron) = 1
            ErrRef(hole) = 1
            Extrapolate
            Transient= BE
            TensorGridAniso
            RHSmin= 1e-30
            RHSmax= 1e30
            RHSFactor= 1e30
            CDensityMin= 1e-30
            ParallelToInterfaceInBoundaryLayer(FullLayer -ExternalBoundary)
      eMobilityAveraging= ElementEdge
      hMobilityAveraging= ElementEdge
            ElementAvalancheMinAngle= 0
            number_of_threads= 8
            Method= ILS(set= 5)
            ILSrc= "
                        set (5) {
                        iterative(gmres(100), tolrel=1e-10, tolunprec=1e-4, tolabs=0, maxit=200);
                        preconditioning(ilut(1.5e-6,-1), right);
                        ordering(symmetric=nd, nonsymmetric=mpsilst);
                        options(compact=yes, linscale=0, refineresidual=60, verbose=0);
                        };
                        "
            BreakCriteria{Current (Contact="drain" absval= 10)}
            ExitOnFailure
            }
Solve       {
            Coupled(Iterations= 1000 LineSearchDamping= 1e-4){ Poisson }
                        NewCurrentPrefix= "Init"
            * -- Ramp Vd from 0 to 5V in 3 sec.--
            Transient (
                        InitialTime= 0 InitialStep= .001 Increment= 1.4 Decrement= 2.0
                        Maxstep= 0.01 FinalTime= 3
                          ) { coupled {Poisson Electron Hole}}
            NewCurrentPrefix= ""
            * -- Ramp Vg from -4 to 10 V in 10 sec (from 3 to 13).--
            Transient (
                        InitialTime= 3 InitialStep= .01 Increment= 1.4 Decrement= 2.0
            Maxstep= 0.01 FinalTime= 13
                        )  {coupled{Poisson Electron Hole}}
            }
#############################################################################

SDevice 3
Electrode {
   { Name="gate"        Voltage= (0 at 0, @Vg@ at 2, @Vg@ at 12)}
   { Name="source"      Voltage= 0.0}
   { Name="drain"       Voltage= (0 at 0, 0 at 2, 10 at 12) }

}

File {
   Grid= "basic_struc1_8_msh.tdr"
   Plot= "@tdrdat@"
   Current= "@plot@"
   Output= "@log@"
   Parameter= "pp4_des.par"
}

Physics {
                        Recombination (
                        SRH(DopingDep TempDep)
                        Auger
                        )

                        Aniso (
                        eMobilityFactor (Total) = 0.83
                        hMobilityFactor (Total) = 1.00
                                    )


                        Mobility (
                        DopingDep
                        HighFieldSaturation
                        Enormal
                        )

                        ## IncompleteIonization
                        EffectiveIntrinsicDensity ( oldSlotboom NoFermi )
```

```
}

Math {

        ExtendedPrecision(@precision@)
        Iterations= 15
        Notdamped= 1000
        eDrForceRefDens= 1
        hDrForceRefDens= 1
        Digits= 5
        ErrRef(electron) = 1
        ErrRef(hole) = 1
        Extrapolate
        Transient= BE
        TensorGridAniso


        RHSmin= 1e-30
        RHSmax= 1e30
        RHSFactor= 1e30
        CDensityMin= 1e-30

        ParallelToInterfaceInBoundaryLayer(FullLayer -ExternalBoundary)
        eMobilityAveraging= ElementEdge
        hMobilityAveraging= ElementEdge
        ElementAvalancheMinAngle=0

        number_of_threads= 8

        Method= ILS(set= 5)
        ILSrc= "
                set (5) {
                iterative(gmres(100), tolrel=1e-10, tolunprec=1e-4, tolabs=0, maxit=200);
                preconditioning(ilut(1.5e-6,-1), right);
                ordering(symmetric=nd, nonsymmetric=mpsilst);
                options(compact=yes, linscale=0, refineresidual=60, verbose=0);
                };
                "
        ## BreakCriteria{Current (Contact="drain" absval=1e-7)}
        ExitOnFailure
}

Plot {
  TotalCurrentDensity/vector
  eDensity hDensity
  eCurrent hCurrent
  ElectricField/vector
  eQuasiFermi hQuasiFermi
  egradQuasiFermi hgradQuasiFermi
  Potential Doping SpaceCharge
  SRH Auger
  AvalancheGeneration
  eAvalanche hAvalanche
  eMobility hMobility
  DonorConcentration AcceptorConcentration
  Doping
  eVelocity hVelocity
  ConductionBandEnergy ValenceBandEnergy BandGap
  eQuasiFermi hQuasiFermi
}


Solve {
        Coupled(Iterations= 10000 LineSearchDamping= 1e-4){ Poisson }
        Coupled(Iterations= 10000 LineSearchDamping= 1e-4){ Poisson Electron Hole}


        NewCurrentPrefix= "Init"
        ## * -- Ramp Vg from 0 to 10 V in 2 sec (from 0 to 2).--
        Transient (
                InitialTime= 0 InitialStep= 1e-8 Minstep = 1e-10 Increment= 1.4 Decrement= 2
                Maxstep= 0.2 FinalTime= 2
                ## *--TurningPoints((Condition(Time(0.0))Value=1e-8))
                ){ coupled { Poisson Electron Hole } }

        NewCurrentPrefix= "v1"
        ## * -- Ramp Vd from 0 to 10 V in 10 sec (from 2 to 12).--
        Transient (
                InitialTime= 2 InitialStep= 1e-8 Minstep = 1e-10 Increment= 1.4 Decrement= 2
        Maxstep= 0.01 FinalTime= 12
                                ) {coupled{Poisson Electron Hole}}

        }
SVisual 1
#-------------------------------------------------------------------------#
```

```
load_library extract
lib::SetInfoDef 1
#-------------------------------------------------------------------------#

set N           @node@
set i           @node:index@


#- Automatic alternating color assignment tied to node index
#-------------------------------------------------------------------------#
set COLORS  [list green blue red orange magenta violet brown]
set NCOLORS [llength $COLORS]
set color   [lindex  $COLORS [expr $i%$NCOLORS]]

#-------------------------------------------------------------------------#


echo "##############################"
echo "plotting Id-Vd(BV) curves"
echo "##############################"

load_file @plot@ -name PLT($N)

if {[lsearch [list_plots] Plot_BV] == -1} {
                create_plot -1d -name Plot_BV
 }

select_plots Plot_BV

set Vd [get_variable_data "drain InnerVoltage" -dataset PLT($N)]
set Id [get_variable_data "drain TotalCurrent" -dataset PLT($N)]
ext::AbsList -out absId -x $Id ;# Compute absolute value of collector currents
create_variable -name absId -dataset PLT($N) -values $absId


create_curve -name BV($N) -dataset PLT($N) \
                -axisX "drain OuterVoltage" -axisY "absId"

set_curve_prop BV($N) -label "IdVd(BV extraction)" \
                -color red -line_style solid -line_width 3

set_plot_prop -title "I<sub>c</sub>-V<sub>ce</sub> Curve" -title_font_size 16 -show_legend
set_axis_prop -axis x -title { Inner drain Voltage [V]} \
                -title_font_size 16 -scale_font_size 14 -type linear
set_axis_prop -axis y -title {drain Current [A]} \
-title_font_size 16 -scale_font_size 14 -type log -range {1e-19 1e-13}
set_legend_prop -font_size 12 -location top_left -font_att bold

#-- Extraction

ext::ExtractBVv -out BV -name BV -v $Vd -i $absId -sign +1


Svisual 2
#-------------------------------------------------------------------------#
load_library extract
lib::SetInfoDef 1
#-------------------------------------------------------------------------#
set N           @node@
set i           @node:index@
set Vd          3V


#- Automatic alternating color assignment tied to node index
#-------------------------------------------------------------------------#
set COLORS  [list green blue red orange magenta violet brown]
set NCOLORS [llength $COLORS]
set color   [lindex  $COLORS [expr $i%$NCOLORS]]

#- Plotting IdVg
#-------------------------------------------------------------------------#
echo "##########################################"
echo "Plotting Id-Vg curve"
echo "##########################################"
load_file @plot@ -name PLT($N)

if {[lsearch [list_plots] Plot_IcVg] == -1} {
                create_plot -1d -name Plot_IdVg
}

select_plots Plot_IdVg

set Vds [get_variable_data "gate OuterVoltage" -dataset PLT($N)]
set Ids [get_variable_data "drain TotalCurrent" -dataset PLT($N)]
ext::AbsList -out absIce -x $Ids ;# Compute absolute value of collector currents
create_variable -name absId -dataset PLT($N) -values $absIce
```

```
create_curve -name IdVg($N) -dataset PLT($N) \
        -axisX "gate OuterVoltage" -axisY "absId"

set_curve_prop IdVg($N) -label "IdVg (Vd = $Vd)" \
        -color $color -line_style solid -line_width 3

set_plot_prop -title "I<sub>d</sub>-V<sub>g</sub> Curve" -title_font_size 20
set_axis_prop -axis x -title {Gate Voltage [V]} \
        -title_font_size 16 -scale_font_size 14 -type linear
set_axis_prop -axis y -title {Drain Current [A]} \
-title_font_size 16 -scale_font_size 14 -type log -range {1e-11 3e-4}
set_legend_prop -font_size 12 -location top_left -font_att bold

## ext::ExtractBVv -out BV -name BV -v $Vd -i $absId -sign +1, need to be able to extract Vt



Svisualv 3
#-------------------------------------------------------------------------#
load_library extract
lib::SetInfoDef 1
#-------------------------------------------------------------------------#
set N           @node@
set i           @node:index@
set Vg           @Vg@


#- Automatic alternating color assignment tied to node index
#-------------------------------------------------------------------------#
set COLORS  [list green blue red orange magenta violet brown]
set NCOLORS [llength $COLORS]
set color   [lindex  $COLORS [expr $i%$NCOLORS]]

#- Plotting IdVd
#-------------------------------------------------------------------------#
echo "########################################"
echo "Plotting Id-Vd curve"
echo "########################################"
load_file @plot@ -name PLT($N)

if {[lsearch [list_plots] Plot_IdVd] == -1} {
        create_plot -1d -name Plot_IdVd
}

select_plots Plot_IdVd

set Vds [get_variable_data "drain InnerVoltage" -dataset PLT($N)]
set Ids [get_variable_data "drain TotalCurrent" -dataset PLT($N)]
ext::AbsList -out absIds -x $Ids ;# Compute absolute value of collector currents
create_variable -name absIds -dataset PLT($N) -values $absIds

create_curve -name IdVd($N) -dataset PLT($N) \
        -axisX "drain InnerVoltage" -axisY "absIds"

set_curve_prop IdVd($N) -label "IdVd (Vg = $Vg)" \
        -color $color -line_style solid -line_width 3

set_plot_prop -title "I<sub>d</sub>-V<sub>d</sub> Curve" -title_font_size 20
set_axis_prop -axis x -title {Drain Voltage [V]} \
        -title_font_size 16 -scale_font_size 14 -type linear
set_axis_prop -axis y -title {Drain Current [A]} \
        -title_font_size 16 -scale_font_size 14 -type linear
set_legend_prop -font_size 12 -location top_left -font_att bold
```

Appendix 2

Appendix 2, provides the all the steps involve preparing the Sample for TEM analysis

The provided SEM image of the Silicon Carbide (SiC) MOSFET interior T-junction reveals several important details about the device's microstructure. The varying textures and contrasts in the image indicate different materials or structural regions within the MOSFET, with bright linear features against a darker background likely representing conductive pathways or areas

where specific materials have been deposited. The image shows regions with both smooth and rough textures; the smoother areas might correspond to well-processed regions, while the

rougher areas could indicate regions that have undergone different processing steps or have different material properties. Any irregularities or anomalies in the image, such as unexpected

roughness or discontinuities in the linear features, could point to potential defects or areas of concern that could affect the performance and reliability of the MOSFET.

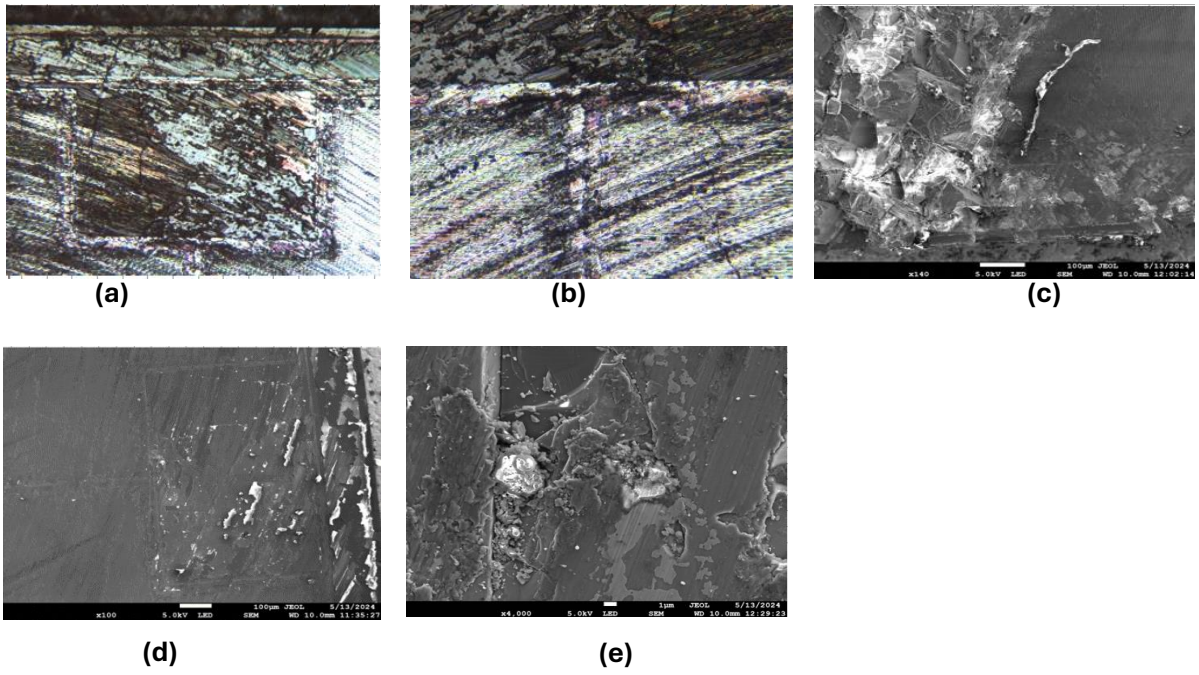

Figure 9.1 Figure 9.2 (a) Optical image of Central channel of MOSFET surface (b) Optical Microscopic image of T-Junction of the MOSFET surface (c)SEM image of the broken Edge of the Surface (d)SEM image of Central channel including T-Junction (e)SEM image of T-Junction

The uniformity and consistency of the features observed in the SEM image can provide insights into the manufacturing quality, with consistent and well-defined features suggesting high-quality fabrication processes, while inconsistencies might indicate areas for improvement. The microstructural details observed can also give clues about the thermal and electrical performance of the MOSFET; for example, well-defined conductive pathways are crucial for efficient electrical performance, while the quality of material interfaces can impact thermal conductivity. These observations are crucial for understanding the internal structure and potential failure points of the SiC MOSFET, guiding improvements in design and fabrication processes to enhance the device's performance and reliability. The second SEM image, taken at a magnification of x20,000, provides a highly detailed view of the crystalline structures within the Silicon Carbide (SiC) MOSFET. Compared to the first image, which was magnified at x700, this image reveals much finer details of the material's surface. The bright areas in the

second image likely indicate regions of different composition or topography, providing insights into the microstructural properties at a much smaller scale. In contrast, the first image, with its lower magnification, offers a broader view of the MOSFET's interior T-junction, highlighting larger structural features and conductive pathways. The second image's higher magnification allows for a closer examination of the crystalline structures, which can be crucial for identifying minute defects or irregularities that might not be visible at lower magnifications. The central feature is a groove or channel with irregular edges, which is crucial for the device's operation as it is where the current flows when the MOSFET is active. The surrounding area displays various textures and shapes, indicating different materials or topographical features at a microscopic level. The channel's edges appear uneven, which might suggest variations in the material deposition or etching processes used during fabrication. These irregularities could impact the electrical performance and reliability of the MOSFET, as they might affect the uniformity of the electric field and current flow within the device. The textures around the channel could represent different layers or regions within the MOSFET, each with distinct properties that contribute to the overall functionality of the device. The highly magnified image of the broken edge of the Silicon Carbide (SiC) MOSFET reveals intricate fracture patterns and microstructural details that are crucial for understanding the material's failure mechanisms. The fracture surface exhibits a variety of textures, indicating different stress points and potential areas of weakness within the SiC material. These features suggest that the failure could be due to mechanical stress or thermal cycling, which are common in high-power electronic devices. Additionally, the presence of any irregularities or defects in the material, visible at this magnification, can point to manufacturing issues that need to be addressed to improve the reliability of future devices.

Preparing SiC MOS samples for TEM analysis involves meticulous techniques to ensure the integrity of the sample. One of the most used methods is Focused Ion Beam (FIB) milling, which is essential for creating thin lamellae suitable for TEM. This process involves using a focused beam of ions, typically gallium ions, to precisely cut and lift out a thin section of the device. The FIB milling process is highly controlled, allowing for the extraction of specific regions of interest within the SiC MOS device. However, the inherent hardness and brittleness of SiC present significant challenges during sample preparation. The high hardness of SiC, which is around 9.2 on the Mohs scale, makes it resistant to mechanical deformation but also prone to cracking and chipping under stress. This brittleness can lead to the introduction of defects or artefacts during the FIB milling process, which can compromise the quality of the

TEM analysis. To mitigate these issues, careful handling and optimization of the milling parameters are crucial. This includes adjusting the ion beam current and voltage to minimise damage, as well as employing low-energy ion polishing to reduce surface roughness and remove any amorphous layers induced by the high-energy ion beam. Additionally, cryo-FIB techniques can be employed to further reduce damage by cooling the sample during milling, which helps to maintain the structural integrity of the SiC. Another important aspect of sample preparation is the use of protective coatings. A thin layer of platinum or carbon is often deposited on the surface of the SiC MOS device before FIB milling. This protective layer helps to prevent ion beam-induced damage and provides a reference for the milling process. Furthermore, the use of lift-out techniques, where the thin lamella is carefully extracted and mounted onto a TEM grid, ensures that the sample remains intact and free from contamination. Begin by carefully cutting the crystals to the desired size and shape using a diamond saw. This step is crucial as it ensures that the sample fits properly into the TEM holder and that the area of interest is accessible for analysis. The precision of the cut will affect the quality of the TEM images, so take your time to make clean, accurate cuts.

Before cut the sample, it is important to sharpen the blade as shown in figure 7.1. A sharp blade will provide cleaner cuts and reduce the risk of damaging the sample. Use a suitable sharpening tool and follow the manufacturer's instructions to ensure the blade is properly sharpened. Regularly check the blade's sharpness and re-sharpen as needed to maintain optimal cutting performance.

The next step is to glue the sample face down. This is done to secure the sample and prevent any movement during subsequent preparation steps. Use an appropriate adhesive that will hold the sample firmly in place without introducing contaminants or damaging the sample. Allow sufficient time for the glue to set and ensure that the sample is firmly attached before proceeding. When mounting the blade, it is essential to ensure the correct orientation of the blade mounting disks. The protruding rims of the disks should face inward. This orientation is critical for maintaining the stability and alignment of the blade during cutting. Incorrect mounting can lead to uneven cuts or damage to the sample. Double-check the orientation before starting the cutting process to avoid any issues and further ensure the blade is touching a water bath to clean and lubricate the cutting blade. After securing the sample and ensuring the blade is properly sharpened and mounted, the next step is to cut individual cross-sections. Begin by carefully positioning the sample on the cutting platform, making sure that the area of interest is aligned with the cutting path of the diamond saw. Proper alignment is crucial to obtain cross-

sections that accurately represent the internal structure of the sample. Next, adjust the cutting parameters on the diamond saw, including the cutting speed and feed rate. These parameters should be optimised based on the material properties of the sample to achieve clean and precise cuts. Consult the saw's manual or rely on previous experience with similar materials to determine the best settings. Once the parameters are set, begin cutting the sample into individual cross-sections. Use a steady hand and apply consistent pressure to avoid any sudden movements that could damage the sample. Each cut should be made slowly and carefully to ensure the integrity of the cross-sections. After making the cuts, carefully collect the individual cross-sections using tweezers or a similar tool. Handle the sections gently, as they can be very delicate, and place them on a clean, flat surface or in a suitable container for further processing. Finally, inspect the cross-sections under a microscope to ensure they are of the desired thickness and quality. If any sections are not suitable, they may need to be re-cut or discarded. Proper inspection at this stage can save time and effort in later steps.

To remove the crystal bond from your TEM samples, follow this three-stage solvent cleaning process using acetone, ethanol, and isopropanol. This method ensures thorough cleaning while minimising the risk of contamination.

Stage 1: Acetone Cleaning: Start by placing the sample in a glass dish containing acetone. Ensure the dish is lined with filter paper to support the sample. Leave the sample in the acetone for approximately 2 minutes. Acetone is highly effective at dissolving organic materials, making it ideal for removing the crystal bond. However, be cautious as acetone can eat through plastics and is easily absorbed through the skin. Keep it away from phones, computers, and your hands. Most importantly, do not allow acetone to encounter the plastic parts or O-rings of the PIPS (Precision Ion Polishing System) or microscopes, as it can cause significant damage. Additionally, acetone can damage LaB6 filaments, so it should be kept away from microscopes.

Stage 2: Ethanol Cleaning: After the acetone bath, transfer the sample to a second glass dish containing ethanol, again lined with filter paper. Leave the sample in the ethanol for about 2 minutes. Ethanol helps to remove any residual acetone and further cleans the sample. Ethanol is less aggressive than acetone but still effective at cleaning the sample surface.

Stage 3: Isopropanol Cleaning: Finally, move the sample to a third glass dish filled with isopropanol, with filter paper lining the dish. Allow the sample to sit in the isopropanol for approximately 2 minutes. Isopropanol serves as a final rinse, removing any remaining residues from the previous solvents and ensuring the sample is clean and ready for TEM analysis.

After the isopropanol bath, carefully remove the sample and place it on a clean filter paper to dry. Ensure the drying environment is clean to prevent any new contaminants from settling on the sample. Begin by cleaning the shiny side of the silicon surfaces that will be glued. Use cotton buds and isopropanol for this task. Dip one end of the cotton bud in isopropanol and use it to wet the silicon surface. Then, use the dry end of the cotton bud to dry the surface. This two-step process helps to lift grease and other contaminants from the surface. It's important to note that solvents alone do not remove grease; they merely lift it from the surface. The mechanical action of the cotton bud is necessary to drag the grease away effectively. Next, prepare the epoxy resin (ER) for glueing. Take a small amount of epoxy resin on a cocktail stick. To avoid applying too much resin, turn the cocktail stick around on a piece of filter paper to remove any excess. This step ensures that you have a thin, even layer of resin for glueing. Lay a thin layer of epoxy resin onto the first silicon surface. Ensure that the layer is even and covers the entire area that will be in contact with the cross-section. Carefully position the cross-section onto the silicon surface with the epoxy resin. Press gently to ensure good contact and adhesion between the silicon and the cross-section. After glueing the first silicon piece to the cross-section, the next step is to prepare the final silicon piece. Spread a thin layer of epoxy resin (ER) onto the shiny side of the final silicon piece. Ensure the layer is even and covers the entire area that will encounter the cross-section.

Carefully drop the final silicon piece onto the opposite side of the cross-section from the first silicon piece. This will create a sandwich structure with the cross-section in the middle and silicon pieces on either side. Using large round-ended tweezers, gently squeeze the entire sandwich structure together. This step ensures that the epoxy resin spreads evenly and that the silicon pieces adhere properly to the cross-section. To achieve flush, square edges, press the pieces into position against a flat surface, such as a table. This alignment is crucial for maintaining the integrity and stability of the sample during TEM analysis. Transfer the assembled sandwich to a hotplate set at 135°C. Maintain pressure on the glue lines using the tweezers for 45-60 seconds. This step helps to ensure that the epoxy resin cures properly and forms a strong bond between the silicon pieces and the cross-section. After maintaining pressure, leave the epoxy resin to set completely. Follow the manufacturer's instructions for the full curing time to ensure the bond is secure. After assembling the sandwich structure and curing the epoxy resin, allow sufficient time for the silicon pieces to bond securely to the substrates. This ensures a strong and stable attachment, which is crucial for the integrity of the TEM sample. Next, prepare a lump of Crystal Bond on a glass slide and heat it until it becomes

hot and fluid. This step is essential as the fluid Crystal Bond will act as an adhesive to mount the specimen onto the glass surface. Once the Crystal Bond is fluid, carefully lay the specimen onto the glass surface, ensuring that the sample is mounted squarely by pressing it into place with large tweezers. Proper alignment is important to maintain the orientation and stability of the sample during TEM analysis. After mounting the specimen, place it on a metal block to cool. The metal block helps to dissipate heat quickly, allowing the Crystal Bond to solidify and secure the sample in place as figure 7.1. Ensure that the sample remains square and properly aligned as it cools. The next step in preparing your TEM sample is to polish the backside. This process is crucial for achieving a smooth, even surface that is essential for high-quality TEM analysis. Follow these steps to ensure effective polishing: To keep the polishing discs clean and free from debris, it is important to maintain a continuous flow of water during the polishing process. The flowing water helps to wash away any particles that are removed from the sample, preventing them from scratching the surface or contaminating the disks. The water supply for the polishing table is controlled using taps located at the side of the table. These taps allow you to adjust the flow rate of the water to suit your polishing needs. However, it is important to note that these taps are weak and should not be relied upon to prevent leaks overnight. Always turn off the water supply at the main valve located at the rear of the table when you are finished polishing for the day. This ensures that the water supply is securely shut off and helps to prevent any potential leaks.

Begin polishing the backside of the TEM sample by placing it on the polishing disk. Apply gentle, consistent pressure to ensure an even polish across the entire surface. The goal is achieving a smooth, flat surface that is free from scratches and other imperfections. Regularly check the progress of the polishing to ensure that the desired surface quality is being achieved.

Figure 9.3 Sample preparation of the TEM analysis (a)sharpening the blade (b) Glueing the sample in tig lase plate on the hot plate (c) Ensure blade is touching water bath to clean and lubricate the cutting blade(d) polishing pads (e) Polish the sample in the direction of the glue line, not across the glue line. (f) Zero the micrometre on the glass slide before measuring sample thickness and measure the thickness of the sample(g) catted Samples (h) Squeeze the whole 4-piece sandwich together with the large round ended tweezers, ensure flush square edges by pressing pieces into position against flat surface (i) Allow Si time to bond securely to the Substrates with Epoxy resin

The next step in preparing your TEM sample involves polishing the backside to achieve a smooth, even surface essential for high-quality TEM analysis. Begin by adhering the polishing pad to a smooth glass polishing surface using water surface tension, ensuring a good grip. Use a car window wiper to smooth out the pad and remove any air bubbles. Place the sample on the polishing pad and use both hands to control it during polishing. If you are right-handed, place the middle finger of your left hand on top of the sample to provide constant and gentle downward pressure, while holding the other end of the glass slide with your index and middle

fingers of your right hand. If you are left-handed, reverse the hand positions. Push the sample back and forth across the polishing pad, ensuring you polish in the direction of the glue line, not across it, to maintain the integrity of the glue line and prevent damage. To square off the sample, start with 15 µm polishing pads. Once the sample is squared off, switch to finer polishing pads (6 µm, 3 µm, and 1 µm) to achieve a high-quality polished surface and a glue line free from asperities. This step should not be time-consuming once the sample is squared off. Ideally, cover each polishing pad with silicon streaking for about 2-3 minutes per pad. Maintain a continuous flow of water during the polishing process to keep the polishing discs clean and free from debris, which helps wash away particles removed from the sample. Control the water supply using the taps located at the side of the table, adjusting the flow rate as needed. However, always turn off the water supply at the main valve located at the rear of the table when finished polishing for the day to prevent leaks. Once polishing is complete, thoroughly rinse the sample with clean water to remove any remaining polishing debris, dry it carefully to prevent water spots or residues, and inspect the polished surface under a microscope to ensure it meets the required standards for TEM analysis. Next, proceed to thinning and polishing the front side of the sample. Start with a 15 µm polish to remove any roughness and achieve a smooth surface. Before measuring the sample thickness, zero the micrometre on the glass slide to ensure accurate measurements. This step is crucial for achieving the desired thickness and quality of the TEM sample. After polishing the backside of the sample, the next step is too thin and polish the front side to achieve the desired thickness for TEM analysis. Begin by using 15 µm polishing paper to reduce the sample thickness to approximately 0.200 mm. This initial step removes the bulk of the material and prepares the sample for finer polishing. Once the sample thickness is down to 0.200 mm, switch to 6 µm polishing paper and continue polishing until the thickness is reduced to approximately 0.135 mm. This step further refines the surface and ensures a more precise thickness. Finally, use 3 µm polishing paper to achieve the final desired thickness of approximately 0.100 mm. This final polishing step ensures a high-quality surface that is suitable for TEM analysis, free from scratches and other imperfections. Throughout the polishing process, regularly check the sample thickness using a micrometre to ensure accuracy, zeroing the micrometre on the glass slide before measuring to obtain precise readings. This careful, step-by-step thinning and polishing process is crucial for preparing a high-quality TEM sample.

As we continue thinning and polishing the front side of the sample, we may notice a reddening of the silicon in thin areas, indicating that the sample is well-thinned and ready to be removed

from the glass slide. Note that not all samples will exhibit this bright reddening. To remove the polished sample from the glass slide, start by submerging the mechanic Post alley thinned sample in acetone to remove any excess Crystal Bond. This step helps to clean the sample and prepare it for further handling. Next, carefully circle the copper (Cu) grid with a diamond file to remove excess silicon and substrate with careful pressure, and to remove the circle of crystal Bond remaining around the sample. This step requires precision to avoid damaging the sample.

Return the sample to the hot plate set at 135°C to soften any remaining Crystal Bond, making it easier to remove the sample from the glass slide. Once the glass slide and sample reach the desired temperature and the crystal Bond becomes highly fluid, begin to slide the sample away using crossover tweezers. This technique reduces the volume of residual glue transported away with the sample. Often, the sample will lift and adhere to the tweezers. If this happens, simply lift the sample into acetone at this point. If the sample does not lift easily, gently lift it from the edge of the glass slide. Then again, I need to proceed with the three steps cleaning as mentioned earlier. To mount the sample for Precision Ion Polishing System (PIPS) processing, begin by using the Duo-post holder, which is designed with two clamping posts located to the left and right of the sample. To release these clamps, exert pressure on the copper (Cu) base ring of the Duo-post. This action is actuated using the black dials on either side of the Duo-post mounting stage. With the Duo-post clamps opened, slide the sample into position using a metal arm. Carefully roll the black dials one notch to secure the sample, and a second notch to raise the sample one increment. At this point, it is crucial to retract the sample positioning arm. Removing the arm now is important because if you try to snap this mechanism out at the last minute when the sample is fully raised, it is liable to ping across the room, potentially causing damage or loss of the sample. Ensure the sample is raised and secured with full clearance from the sample positioning arm, confirming that it is properly positioned and stable for the PIPS process. Proceed with PIPS processing by setting the guns to approximately 3.5 keV with angles at +/- 6° until a small hole is visible in the glue line. As the sample is bowled out around the glue line, light microscope images may become difficult to interpret. Moving through focus with the microscope should help distinguish between defocus effects and real imaging effects, which are also seen in the TEM. The PIPS guns should achieve around 20 µA at 3.5 keV, with a higher value being desirable. Once a hole is seen in the glue line, finish PIPSing at 1.0 keV for 3 minutes with guns at +/- 8°, followed by Piping at 0.3 keV for 10 minutes with guns at +/- 8°. PIPS should be run in double mode for cross-sections. Note that this is not an extensive PIPS manual, and the machine requires regular cleaning and servicing.