Ultra Low Phase Noise Microwave Oscillators

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Doctor of Philosophy

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March, 2024

Abstract

This thesis presents the findings of research into low phase noise oscillators. Four design approaches have been developed with the common aim of achieving ultra low phase noise performance. The main body is split into four chapters which detail each design starting with a 1.5 GHz dielectric resonator oscillator, a 16 GHz distributed Bragg resonator oscillator with parallel amplifiers used in the feedback loop, the development of the feedforward technique for use in a low noise oscillator before finishing with the latest measurements of a 5 MHz crystal oscillator.

The development of a 1.5 GHz dielectric resonator oscillator is presented in Chapter 3 which details the design process of each part and the assembly of the complete oscillator in a metal enclosure. The design of the coupling probes, resonator enclosure and the phase shifting circuits are presented. This chapter ends with the presentation and discussion of ultra low oscillator phase noise measurements.

In the fourth chapter the design of the feedback circuit to be used with a 16 GHz distributed Bragg resonator cavity is presented as well as research into the coupling mechanisms used with this resonator. Initial oscillator phase noise measurements are presented.

A new technique is introduced in Chapter 5 using a feedforward amplifier in an oscillator to suppress the flicker noise introduced by the sustaining amplifier. A derivation of design equations are presented as well as measurements of a 100 MHz oscillator showing that a variable gain feedforward amplifier can be used in the feedback loop without the need for external power limiting circuits.

The sixth and final technical chapter presents state of the art measurements of a 5MHz crystal oscillator. This chapter includes the design of an electronic phase shifter as well as measurements of the individual parts of the oscillator.

Acknowledgements

I thank my supervisors, Professor Jeremy Everard and Dr Simon Bale for their knowledge, experience, encouragement and support throughout this research. Their constant feedback and critical analysis of my work has been invaluable in the completion of this project.

Thank you to all the staff within the school of PET who have helped me with technical work and advice in manufacturing all the parts and PCBs I have used in my measurements.

My friends and fellow PhD students within this research group, Luke Dummott and Stuart Kenny for their support, encouragement and stimulating conversations throughout. A further thank you to Luke for teaching me how to play chess - a welcomed distraction during our many lunch breaks both during lockdown and afterwards! I thank Prof. Andy Marvin for his insight into research practices, support and sharing his valuable experience with me whilst we have been sharing the office.

I wish to express a very special thanks to my parents, Nick and Debi, for without whom I would not have begun this research let alone get to a point in which I could have written this thesis. Thank you for pushing me through this period of my life and encouraging me to persevere with my research.

Finally, a very special thank you my love, Molly. I cannot write in enough detail how much your support, love and encouragement has helped me throughout this work. Without you, I would have never completed this research.

St.John Gilbert, York, March 2024.

Declaration

I declare that this thesis is a presentation of original work and I am the sole author. This work has not previously been presented for a degree or other qualification at this University or elsewhere. All sources are acknowledged as references.

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Chapter 1

Introduction

An oscillator is an electronic device that produces a periodic oscillating output signal without an external input. They are essential timing elements in almost all modern electronic systems including communication, measurement and instrumentation systems providing a reference signal that is used to propagate, synchronise and process signals. The oscillator therefore sets the ultimate noise performance of such systems as large phase noise generated by an oscillator can mask the required signal leading to the introduction of errors into the system. A key characteristic of an oscillator is its frequency stability, which, can be divided into long term and short term stability. Long term stability is the frequency drift of the device as a result of device ageing, poor buffering and thermal effects. Short term stability is the close to carrier frequency stability of an oscillator as a result of phase and amplitude modulation.

Phase noise is defined as the ratio of the phase noise power at a given offset in a 1Hz bandwidth to the total carrier power in a single sideband. It is expressed in dBc/Hz. Phase fluctuations are introduced to the oscillator output spectrum by the transposition of flicker (1/f) noise from the oscillator circuit elements as well as transposed thermal noise.

1.1 Research aims

The aim of the research presented in this thesis is to improve on the phase noise performance of four different oscillators using different design approaches. The four oscillators developed in this research

operate at 1.5 GHz, 16 GHz, 100 MHz and 5 MHz with each presenting their own challenges specific to their configurations. The contribution to the phase noise from all oscillator components is investigated and analysed.

The oscillators developed are feedback oscillators containing amplifiers, phase shifters and output couplers which are all designed to minimise oscillator phase noise. Furthermore, the oscillators use different types of resonator, at 1.5 GHz a dielectric resonator is used, at 16 GHz a distributed Bragg resonator is used, at 100 MHz both and LC and crystal oscillator is used and at 5 MHz a crystal is used. In each case the unloaded Q, Q_0, is kept as high as possible to minimise oscillator phase noise.

Throughout the design phase, low noise design procedures have been followed in order to reduce the noise introduced into the oscillator loop by the individual oscillator elements. In the 1.5 GHz and 16 GHz oscillators, parallel combinations of amplifiers are investigated so that the power available to the resonator is high and to reduce the flicker noise introduced by the devices. In the 100 MHz oscillator a variable gain feedforward amplifier is used to ensure the flicker noise suppression that can be achieved by this amplifier configuration is not degraded by external power limiting components that are used to keep the feedforward amplifier operating correctly.

1.2 Thesis Structure

The thesis is organised into seven chapters. Chapter 2 is a general introduction to oscillator theory and low phase noise design. This includes a review of the literature containing material on the background and operation principles of ultra low phase noise oscillators. The various types of noise including thermal noise, flicker noise and shot noise that contribute to the overall phase noise are introduced before a model for an ultra low phase noise oscillator, developed by Everard [1] is discussed. A full derivation of the equation for oscillator phase noise from this model is also presented that demonstrates how the various oscillator parameters affect the oscillator phase noise. Each subsequent chapter contains a review of the literature specific to the type of oscillator design presented in each chapter.

The third chapter describes the design and manufacture of a 1.5 GHz Dielectric Resonator Oscillator (DRO). Field solver simulations of the resonator are obtained using CST Studio Suite, a software package for 3D electromagnetic analysis. The simulation results are presented as well as an in depth

description and analysis of the circuit designs for all of the oscillator elements. The measurements of the individual oscillator components and state of the art oscillator phase noise measurements are presented.

Chapter 4 contains the design process, implementation and measurements of a 16 GHz Distributed Bragg Resonator (DBR) oscillator. A maximum Q_0 of 160,000 at 16 GHz has been measured. There is also an investigation into the coupling to the resonator for optimum oscillator phase noise that considers loop probes, external impedance transformation networks and aperture coupling, with the aim of achieving 6dB insertion loss at resonance whilst exhibiting the highest possible Q_0. The amplifier design process includes the design of a parallel amplifier used to reduce the flicker noise introduced and to increase the output power when compared to using a single amplifier device. There is also a description of the design of a 10dB output coupler and an electronically tunable phase shifter. This chapter concludes with measurements of the 16 GHz oscillator phase noise performance.

In Chapter 5, research into the suitability of a variable gain feedforward amplifier for use in an ultra low phase noise oscillator is presented. It has previously been shown that the feedforward amplifier can suppress flicker noise introduced by the main amplifier by approximately 20dB [2]. However, incorporating this amplifier configuration into an oscillator reduces the level of flicker noise suppression because in an oscillator, the main amplifier enters saturation, causing its gain to reduce. There is a gain and phase imbalance between the two amplifiers (main and error correction amplifiers) in the feedforward design, that, result in a decrease in the flicker noise suppression.

Using PIN diode limiters to reduce the level of saturation in the main amplifier has been shown to decrease the flicker noise in an oscillator at 7.6 GHz [2]. However the level of flicker noise suppression is reduced to 13dB as the PIN diode contributes flicker noise to the oscillator phase noise spectrum that is not suppressed by the feedforward amplifier. The approach presented in this chapter is to allow the main amplifier to saturate to the level required to ensure the gain of the amplifier is equal to the loop losses in the oscillator. Then, the gain of the error correction amplifier, the attenuation between the amplifier loops and the phase shift between the loops can be adjusted accordingly to remove the need for additional components that will introduce additional flicker noise. The derivation of a complete set of design equations that can be used to design a feedforward amplifier of a specified gain is presented. Measurements of the feedforward amplifier using a variable gain, error correction

amplifier are presented as well as oscillator phase noise measurements of a 100 MHz oscillator using the feedforward amplifier to suppress flicker noise.

The sixth chapter introduces the design and measurement of a 5 MHz crystal oscillator building on the work presented in [3] and [4]. A state of the art phase noise measurement of -132dBc/Hz at 1 Hz offset from the carrier is presented. The design includes an electronically tunable phase shifter that is used to introduce a phase shift into the loop in order to sustain oscillation but also provides a range of phase shifts for tuning the oscillator as the crystal ages causing the resonant frequency to drift.

Finally, conclusions, observations and suggestions for further work are given in the seventh chapter including a brief analysis of the outcomes of this research.

1.3 Related Publications

St.John Gilbert, Simon Bale and Jeremy Everard. Ultra Low Phase Noise 16GHz Oscillator using a Distributed Bragg Resonator *European Frequency and Time Forum (EFTF)*, Neuchatel, 2024. This conference paper was submitted after the submission of this thesis and includes additional measurements of oscillator phase noise the improve on those presented here. The author won the student poster competition for the Oscillators and Noise category.

The work presented in Chapter 6 was previously presented at the joint FCS-ISAF 2020 Virtual Conference (held virtually due to COVID-19 impacting travel).

Chapter 2

Phase noise theory and literature

2.1 Feedback Oscillator

An electronic oscillator is a device that can provide a stable and periodic oscillating signal without the need for an external input signal. Such devices are used in almost all electronic circuits that require a reference or a clocking signal. There are two main types of oscillator design: positive feedback and negative resistance oscillators. The work presented in this thesis will focus on the positive feedback topology. A feedback oscillator can be constructed by applying positive feedback to a resonant element. This is achieved by connecting an amplifier to the output of a resonator and then feeding the output of the amplifier into the resonator input, the filtered signal will continue to build up in the loop until the amplifier saturates and the gain reduces until it becomes equal to the loop losses. Figure 2.1 shows the block diagram of a positive feedback oscillator, where V_i is white Gaussian noise that represents the noise present in the oscillator before startup. The loop voltage equations can be derived from the block diagram as :

$$V_d = V_i + V_b \tag{2.1}$$

$$V_o = A(j\omega).V_d \tag{2.2}$$

$$V_b = B(j\omega).V_o \tag{2.3}$$

The closed loop voltage gain is given by V_o/V_i, therefore substituting (2.2) and (2.3) into (2.1) and rearranging for V_o/V_i, the following equation can be derived demonstrating the closed loop gain as a

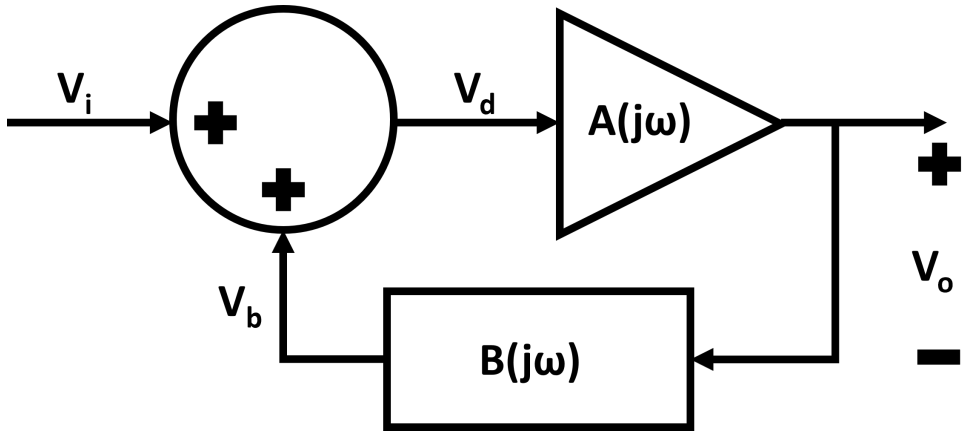


Figure 2.1: Positive feedback applied to a two port device block diagram. An oscillator can be modelled as a two port device where the input is white Gaussian noise.

function of the amplifier and loop transfer functions:

$$A_{vc(j\omega)} = \frac{V_o}{V_i} = \frac{A(j\omega)}{1 - B(j\omega)A(j\omega)} \tag{2.4}$$

In a stable oscillator, there must be a measured output voltage in the absence of an input voltage, i.e. $V_i = 0$. It is at this point that $B(j\omega)A(j\omega) = 1$. The complex terms in (2.4) give rise to the Barkhasuen stability criterion that states that in order to sustain stable oscillation, the open loop gain is at unity and the open loop phase shift is an integer multiple of 2π:

$$|A(j\omega)||B(j\omega)| = 1 \tag{2.5}$$

$$\angle A(j\omega) + \angle B(j\omega) = 2\pi N \quad \text{where} \quad N = 0, 1, 2, 3... \tag{2.6}$$

The gain condition is stated in (2.5) and the phase condition in (2.6). An oscillator requires some signal in the loop to 'start up' and this signal is present as thermal noise in the feedback path. In this period V_i is greater than 0 but is much smaller than V_o. The thermal noise is amplified and filtered by the oscillator loop until the amplifier enters saturation causing the gain of the amplifier to reduce until it is equal to the loop losses. At this point, the gain criterion is met. The closed loop phase shifter must be adjusted such that the phase criterion is satisfied as both criterion are necessary for oscillation to occur.

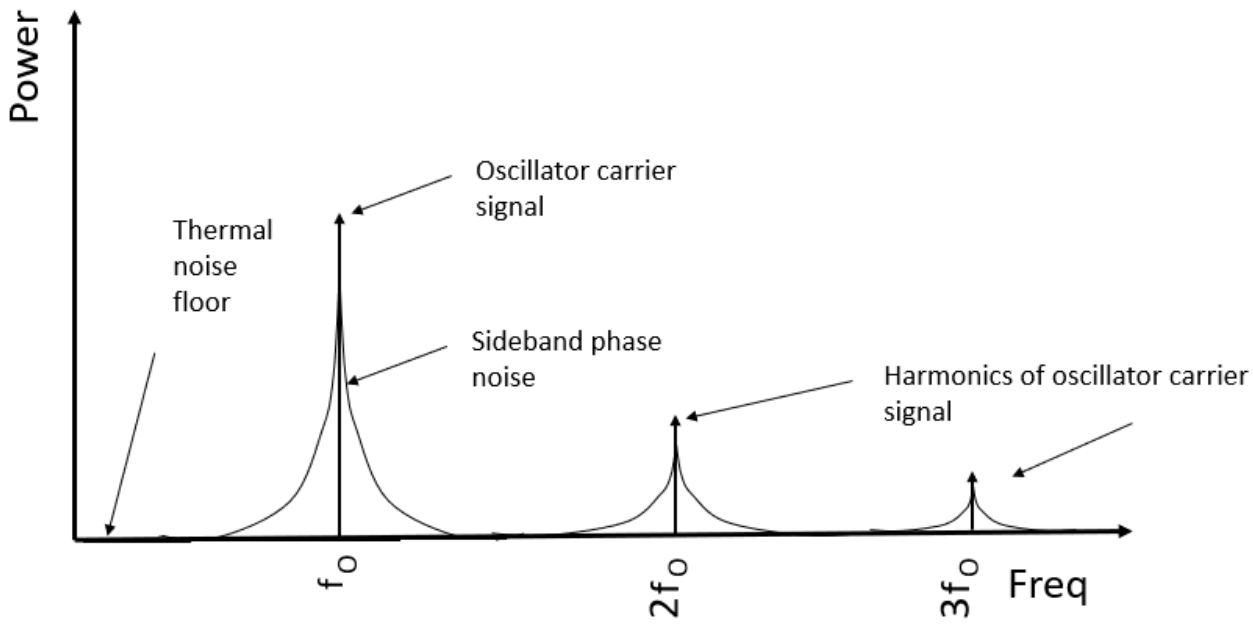


Figure 2.2: Spectrum of real oscillator output.

2.2 Oscillator Phase Noise

2.2.1 Ideal and real oscillators

Phase noise is defined as the ratio of the power density in a single phase noise modulation side-band, per Hz, at an offset frequency to the carrier and the total signal power expressed in dBc/Hz. In the ideal oscillator, the output of the device is a single tone with an infinitely small bandwidth. In this case all of the power would be in the output signal alone and there would be no sidebands in the spectrum.

In reality, such an oscillator is impossible as phase noise modulates the carrier signal from the components within the oscillator loop. The active devices are operating in the non-linear regime that causes harmonics of the carrier to be present in the output spectrum. The real oscillator output spectrum is shown in Figure 2.2 The output power of the real oscillator is distributed over a finite bandwidth and amongst its harmonics. This power distribution is the combination of random amplitude modulation (AM) and phase modulations (PM) resulting from amplitude and phase noise modulating

the carrier signal. Amplitude modulation noise is suppressed by the amplifier limiting process in an oscillator and makes the upper and lower sidebands coherent, [5]. Therefore, only modulation noise as a result of phase fluctuations is considered in this research. Random phase fluctuations are caused by residual phase noise, Shot noise and flicker noise introduced by the oscillator components.

The output signal of a real oscillator modulated by the noisy signals $\alpha(t)$ and $\vartheta(t)$ can be expressed in volts as:

$$V(t) = A_o(1 + \alpha(t)) \cdot \cos[2\pi f_o t + \vartheta(t)] \tag{2.7}$$

where $\alpha(t)$ represents the amplitude modulation, $\vartheta(t)$ is the phase modulation signal and f_0 is the oscillator centre frequency. The AM noise is suppressed and the AM component $\alpha(t)$ reduces to 0, (2.7) can be simplified:

$$V(t) = A_o \cdot \cos[2\pi f_o t + \vartheta(t)] \tag{2.8}$$

If it is assumed that $\vartheta(t) << 1$, then, the modulation index, φ_p, is small. The phase term of (2.8) can be expressed as a frequency modulated signal:

$$\vartheta(t) = \varphi_p(t)\sin(2\pi f_m t) \tag{2.9}$$

Substituting (2.9) into (2.8) yields :

$$V(t) = A_o \cdot \cos[2\pi f_o t + \varphi_p(t)\sin(2\pi f_m t)] \tag{2.10}$$

Using the identity *cos(a+b)=cos(a)cos(b)-sin(a)sin(b)*, we can expand (2.10) to

$$V(t) = A_o \cdot [(\cos(2\pi f_o t) \cdot \cos(\varphi_p(t)\sin(2\pi f_m t)) - (\sin(2\pi f_o t) \cdot \sin(\varphi_p(t)\sin(2\pi f_m t))] \tag{2.11}$$

As the modulation index is small, the small angle approximation can be used, *sin(x)* $\approx x$ and *cos(x)* $\approx$ *1.* Therefore, (2.11) becomes :

$$V(t) = A_o \cdot [(\cos(2\pi f_o t) - \varphi_p(t) \cdot (\sin(2\pi f_o t) \cdot \sin(2\pi f_m t)] \tag{2.12}$$

Finally, using the identity $\sin A \sin B = \frac{1}{2}[\cos(A - B) - \cos(A + B)]$, we can write :

$$V(t) = A_o \cdot [(\cos(2\pi f_o t) - \frac{\varphi_p(t)}{2}((\cos(2\pi(f_0 + f_m)t) - \cos(2\pi(f_0 - f_m)t))] \tag{2.13}$$

This equation describes the output oscillator signal with small phase or frequency changes causing sidebands at frequencies ($f_0 \pm f_m$). These sidebands are the phase noise spectrum expressed as:

$$L(f) = \frac{P_n}{P_c} = \frac{\frac{1}{2}(\frac{A_0\varphi_0}{2})^2}{\frac{1}{2}A_0^2} = \frac{\varphi_p^2}{4} = \frac{\varphi_{rms}^2}{2} = P_\varphi(f_m) \tag{2.14}$$

where φ_{rms} is the RMS noise power and is equal to $\frac{\varphi_p}{\sqrt{2}}$, where φ_p is the peak noise power. The power spectral density is equally distributed about the carrier then the double sideband noise power is equal to :

$$S_\varphi(f_m) = 2P_\varphi(f_m) = \frac{\varphi_p^2(f_m)}{2} \tag{2.15}$$

Therefore, the single side-band phase noise can be written as:

$$L(f_m) = \frac{1}{2}S_\varphi(f_m) \tag{2.16}$$

2.2.2 Thermal Noise

Thermal noise is the noise generated by the random motion of charge carriers in a conductor as a result of thermal excitation [6] and is given by the following equation demonstrated by Nyquist [7]:

$$e_n = \sqrt{4kTRB} \tag{2.17}$$

where e_n is the RMS value of the thermal noise voltage, k is Boltzmann's constant 1.38×10^{-23}, T is the absolute temperature in K, R is the resistance presented by the conductor in Ω and B is the bandwidth in which the noise is measured, in Hz. The noise spectral density of the noise in V^2/Hz is:

$$S_n(f) = e_n^2/B = 4kTR \tag{2.18}$$

Therefore, the noise spectral density is independent of frequency and thermal noise can be regarded as white noise with a constant power spectral density. The amplitude of the noise voltage generated by thermal agitation is random but it has Gaussian distribution [8].

2.2.3 Shot Noise

Shot noise is the noise generated by DC biasing in devices with a potential barrier built in. Fluctuations of the current are caused as DC is not a smooth flow of charge, rather the flow of discrete electrical charges. The spectral density of Shot noise is given as:

$$S_i(f) = 2eI_{DC} \tag{2.19}$$

where e is the electron charge, 1.6×10^{-19} coulomb and I_{DC} is the average DC current. Like thermal noise, Shot noise is independent of frequency and Gaussian, it is therefore also considered as white noise [8].

2.2.4 Flicker Noise

Further noise in excess of thermal and Shot noise components is often referred to as flicker noise. Its spectral density exhibits an approximately $\frac{1}{f}$ characteristic at frequency offsets from the carrier. Rhodin et al. [9] show experimentally that high Q resonators and low noise devices in the feedback path contribute to low phase noise oscillator designs. In passive components such as a resistor, the noise is determined by the construction of the device. The number of contacts, the dielectric material used as well as the quality of the contacts within the device contribute to the $\frac{1}{f}$ noise. The sources of $\frac{1}{f}$ noise in active devices such as semiconductors is investigated in [10–12]. In FETs, the gate-source capacitance (C_{GS}) has been shown through analysis by Siweris et al. to be the non linear element that converts low frequency noise to phase noise [10] and shown experimentally in [11, 12] that the gate noise voltage is modulated onto (C_{GS}). The cause of the noise voltages in semiconductor devices is due to charge carriers randomly moving to and from the traps in conducting channel and oxide [13]. Baseband current modulation and collector-base voltage modulation in BJTs has been shown in [14] to be the mechanism for $\frac{1}{f}$ noise up conversion.

Based on measurements by Hooge [14], the power spectral density of $\frac{1}{f}$ noise can be modelled as:

$$S_f(f) = \frac{K_f}{f^{\alpha}} \tag{2.20}$$

where the constant K_f is equal to the spectral density at 1 Hz and is dependent on the device parameters

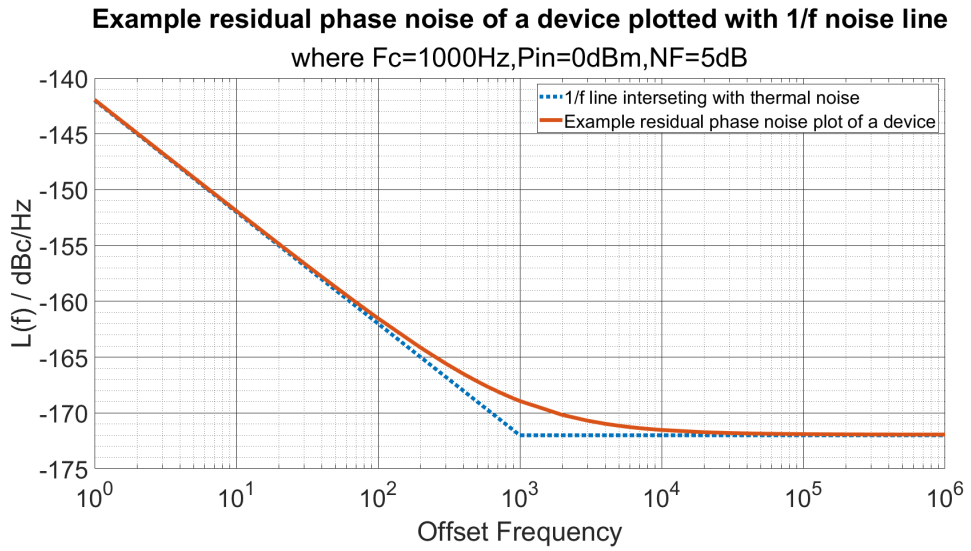


Figure 2.3: Example $\frac{1}{f}$ noise intersecting with the thermal noise to give the flicker noise corner.

such as the material and DC current in the device. Further, the index α is typically in the range 0.8-1.4, though is typically approximated to 1. At higher frequency offsets from the carrier, the $\frac{1}{f}$ noise becomes lower than the thermal noise and the frequency this occurs is called the flicker noise corner. The spectrum in Figure 2.3 shows a 10dB/decade slope representing flicker noise intersection the thermal noise. The flicker noise corner, f_c, is the frequency where the two lines meet.

The spectral density of amplifier flicker noise can be extended to cover a broader range of offset frequencies:

$$S_a(f) = \frac{kTF}{P_i}\left(1 + \frac{f_c}{\Delta f}\right) \tag{2.21}$$

where kTF is the thermal noise of the device with a noise factor, F at input power, P_i, f_c is the flicker noise corner and Δf is the offset frequency from the carrier.

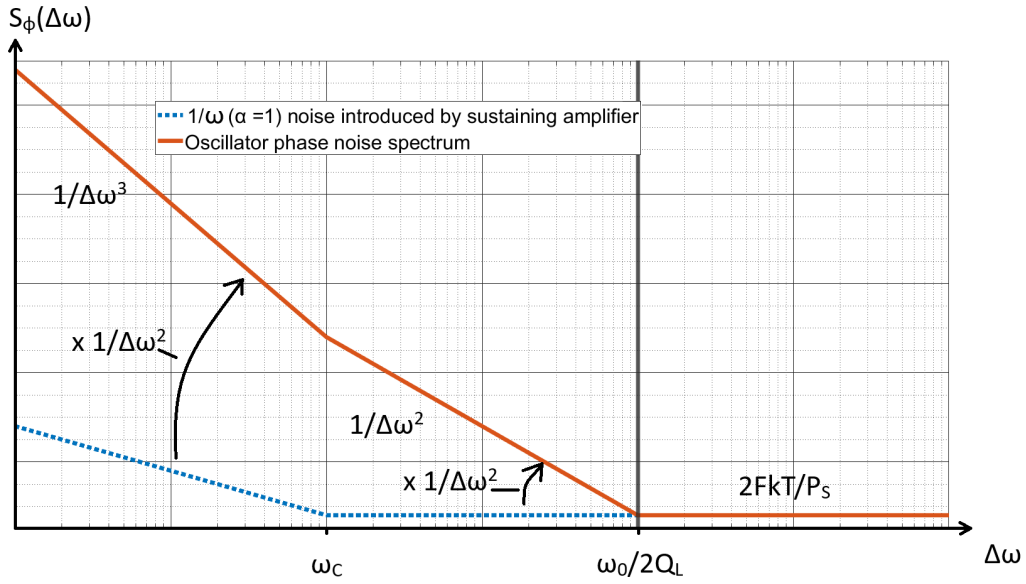


Figure 2.4: Oscillator noise power spectral density plotted variation with frequency from the oscillator frequency. The $1/\Omega$ noise from the amplifier is multiplied by the $1/\Omega^2$ noise introduced by the resonator above and below ω_C.

2.3 Oscillator Phase Noise Models

2.3.1 Leeson's model and Parker's extension

Leeson [15] derived an equation of the expected oscillator output spectrum and presented experimental findings that confirm the validity of the derived equation. However no model was used to prove the equation in this paper. The equation developed by Leeson is :

$$S_\varphi(\Delta\omega) = S_{\Delta\vartheta}\left[1 + \left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right] [15] \tag{2.22}$$

Where $S_\varphi(\Delta\omega)$ is the noise power spectral density of the phase variations, ω_0 is the carrier frequency, Q_L is the loaded quality factor and $\Delta\omega$ is offset frequency from the carrier. $S_{\Delta\vartheta}$ is the noise power spectral density of the additive noise which is equal to $\frac{\alpha}{\Delta\omega} + \frac{2FkT}{P_S}$ where α is a constant determined by the level of $1/\Delta\omega$ variations (typically in the range 0.8-1.2, assumed to be 1 in this section), F is the noise factor of the sustaining amplifier, k is the Boltzmann constant, T is the temperature is kelvin and P_S is the power at the input to the amplifier input. The equation assumes that the flicker noise corner, ω_C, of the amplifier in the oscillator is within the resonator 3dB bandwidth.

The equation shows that the noise power spectral density, noise PSD, decreases at a rate of 9dB per octave (30dB/decade) with increasing frequency up to the frequency that flicker noise effects are no longer dominating. This is due to the $1/\Delta\omega^3$ term that is a result of the product of the $1/\Delta\omega$ noise PSD generated by the amplifier and the $1/\Delta\omega^2$ noise PSD generated by the resonator. After this frequency the spectral density decreases at a rate of 6dB/ octave (20dB/decade) up the frequency where the additive noise becomes white noise and the spectral density is flat with respect to frequency. This is due to the noise PSD of the resonator dominating the spectrum. Figure 2.4 is a plot of equation 2.22 demonstrating the 9dB/octave and 6dB/octave decrease in oscillator noise spectral density.

Equation 2.22 shows that the noise power spectral density of the phase variations, $S_\varphi(\Delta\omega)$, is inversely proportional to Q_L^2, therefore, increasing Q_L will decrease the oscillator phase noise. Furthermore, 2.22 $S_\varphi(\Delta\omega)$ is proportional to the noise figure of the amplifier.

Parker extended this model [16], where it is shown that the optimum insertion loss of the resonator should is for minimum phase noise.

2.3.2 Everard's Model

In order to define a set of equations that accurately predict oscillator phase noise, a simple model for the feedback oscillator was created by Everard [17] that models the oscillator as an LCR network and a two input amplifier representing the feedback loop. The two inputs to the amplifier are of equal impedance and are also equal to the output impedance of the amplifier. One input is used to model the noise in the oscillator and the other is used to model the feedback path. These are modelled separately but the two inputs are summed and amplified to produce a single output signal. The resonance is modelled as an LCR circuit that can incorporate impedance transformations to model any resonant frequency and Q_0. Figure 2.5 shows the model developed by Everard.

A voltage transfer function for the oscillator can be derived from this model. White noise is injected into the noise input V_{IN1}, and $\mathbf{V}_{IN2}$ is the feedback input signal. V_{OUT} can be written as:

$$V_{OUT} = G(V_{IN1} + V_{IN2}) = G(\beta V_{OUT} + V_{IN2}) \tag{2.23}$$

where G is the gain of the amplifier between nodes (1) and (2), and β is the voltage feedback coefficient between nodes (1) and (2). Rearranging for $\frac{V_{OUT}}{V_{IN2}}$, the voltage transfer function between

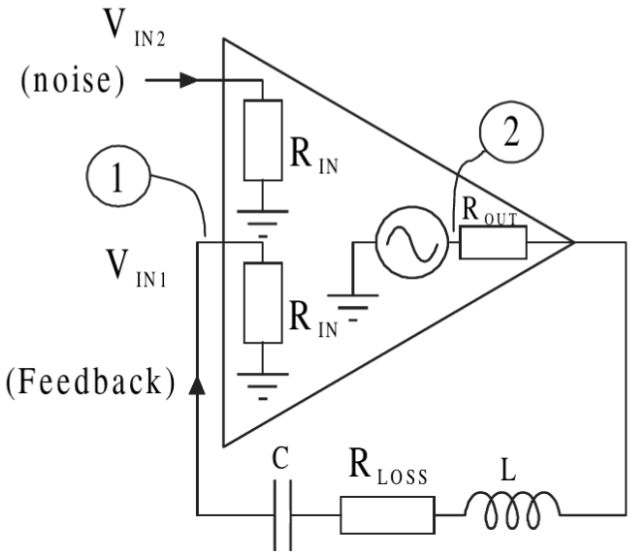


Figure 2.5: Oscillator equivalent circuit model developed by Everard [17].

input ports 1 and 2:

$$\frac{V_{OUT}}{V_{IN1}} = \frac{G}{1-(\beta G)} \tag{2.24}$$

The feedback coefficient can be derived from the potential divider formed by the resonant feedback element between R_{IN1} and R_{OUT}. It can be shown that:

$$\beta = \frac{R_{IN}}{R_{LOSS} + R_{IN} + R_{OUT} + j(\omega L - 1/\omega C)} \tag{2.25}$$

The offset frequency from the carrier, $\Delta\omega$, can be written as $\Delta\omega = \omega \pm \omega_0$, where ω_0 is the carrier frequency. Assuming that $\Delta\omega << \omega_0$, the imaginary part of the denominator in (2.25) can be written as:

$$(\omega L - 1/\omega C) = \pm 2\Delta\omega L \tag{2.26}$$

Q_L of the resonator is:

$$Q_L = \frac{\omega_0 L}{(R_{OUT} + R_{LOSS} + R_{IN})} \tag{2.27}$$

which can be rearranged for L:

$$L = \frac{Q_L(R_{OUT} + R_{LOSS} + R_{IN})}{\omega_0} \tag{2.28}$$

Substituting (2.28) into (2.26) yields:

$$(\omega L - 1/\omega C) = \pm 2Q_L(R_{OUT} + R_{LOSS} + R_{IN})\frac{\Delta\omega}{\omega_0} \tag{2.29}$$

Substituting (2.29) into (2.25) yields:

$$\beta = \frac{R_{IN}}{(R_{OUT} + R_{LOSS} + R_{IN})(1 \pm 2jQ_L\frac{\Delta\omega}{\omega_0})} \tag{2.30}$$

As the Q_0 is :

$$Q_0 = \frac{\omega_0 L}{R_{LOSS}} \tag{2.31}$$

The ratio of Q_L to Q_0 is given by:

$$\frac{Q_L}{Q_0} = \frac{R_{LOSS}}{(R_{OUT} + R_{LOSS} + R_{IN})} \tag{2.32}$$

Therefore:

$$\left(1 - \frac{Q_L}{Q_0}\right) = \frac{R_{OUT} + R_{IN}}{(R_{OUT} + R_{LOSS} + R_{IN})} \tag{2.33}$$

At resonance the feedback coefficient of the resonator is :

$$\beta_0 = \frac{R_{IN}}{(R_{OUT} + R_{LOSS} + R_{IN})} = \left(1 - \frac{Q_L}{Q_0}\right)\left(\frac{R_{IN}}{R_{OUT} + R_{IN}}\right) \tag{2.34}$$

By substituting (2.34) into (2.30), the resonator response becomes:

$$\beta = \left(\frac{R_{IN}}{R_{IN} + R_{OUT}}\right)\left(1 - \frac{Q_L}{Q_0}\right)\left(\frac{1}{1 \pm 2jQ_L\frac{\Delta\omega}{\omega_0}}\right) \tag{2.35}$$

When $R_{IN} = R_{OUT}$, $S_{21} = 2 \times \beta$:

$$S_{21} = \left(1 - \frac{Q_L}{Q_0}\right)\frac{1}{(1 \pm 2jQ_L\frac{\Delta f}{f_0})} \tag{2.36}$$

where Δf is the offset from resonant frequency, now given in Hz and f_0 is centre frequency. This equation describes the variation of insertion loss of resonator circuits, it also defines the closed loop gain of the feedback amplifier. At resonance the second term becomes zero as Δf is zero and the equation simplifies to :

$$S_{21} = \left(1 - \frac{Q_L}{Q_0}\right) \tag{2.37}$$

By substituting (2.35) into (2.24), the voltage transfer function becomes :

$$\frac{V_{OUT}}{V_{IN2}} = \frac{G}{1 - \frac{G(1-\frac{Q_L}{Q_0})(\frac{R_{IN}}{R_{IN}+R_{OUT}})}{(1 \pm 2jQ_L\frac{\Delta f}{f_0})}} \tag{2.38}$$

At resonance $\Delta f = 0$, therefore, $2jQ_L\frac{\Delta f}{f_0}$ becomes 0 and can be ignored. 2.38 now becomes:

$$\frac{V_{OUT}}{V_{IN2}} = \frac{G}{1 - G(1-\frac{Q_L}{Q_0})(\frac{R_{IN}}{R_{IN}+R_{OUT}})} \tag{2.39}$$

Furthermore, at resonance, the ratio V_{OUT} / V_{IN2} is very large and the denominator of 2.39 is approximately 0. Therefore the gain becomes:

$$G = \frac{1}{(1-\frac{Q_L}{Q_0})\left(\frac{R_{IN}}{R_{IN}+R_{OUT}}\right)} \tag{2.40}$$

as $G(1-\frac{Q_L}{Q_0})(\frac{R_{IN}}{R_{IN}+R_{OUT}}) = G\beta_0 = 1$. This equation states that at resonance the amplifier in the oscillator has a gain equal to that of the insertion loss of the resonator. The voltage transfer, equation (2.38) function becomes:

$$\frac{V_{OUT}}{V_{IN2}} = \frac{G}{1 - \frac{1}{\left(1 \pm 2jQ_L\frac{\Delta f}{f_0}\right)}} \tag{2.41}$$

Substituting (2.40) into (2.41) the voltage transfer function becomes:

$$\frac{V_{OUT}}{V_{IN2}} = \frac{1}{(1-\frac{Q_L}{Q_0})\left(\frac{R_{IN}}{R_{IN}+R_{OUT}}\right)\left(1 - \frac{1}{\left(1 \pm 2jQ_L\frac{\Delta f}{f_0}\right)}\right)} \tag{2.42}$$

As we are concerned with the noise at frequency offsets close to the carrier, $\Delta f << f_0$. Then:

$$\frac{Q_L \Delta f}{f_0} << 1 \tag{2.43}$$

The voltage transfer can be further simplified to :

$$\frac{V_{OUT}}{V_{IN2}} = \frac{1}{\left(1-\frac{Q_L}{Q_0}\right)\left(\frac{R_{IN}}{R_{IN}+R_{OUT}}\right)\left(\pm 2jQ_L\frac{\Delta f}{f_0}\right)} \tag{2.44}$$

Oscillator phase noise is typically defined as the ratio of noise power in a 1 Hz side band at a frequency

offset from the carrier, to the total oscillator carrier power. Therefore, the voltage transfer function must be converted to a characteristic that is proportional to power. This can be achieved by producing the square of the output voltage at an offset frequency and the square of the total output voltage.

The input noise power is kTF in a 1 Hz bandwidth where kt is the noise power that would have been available to the noise input if the source impedance had been equal to the the input power impedance, R_{IN}. T is the noise temperature, k is Bolztmann's constant 1.38×10^{-23} and F is the noise factor of the amplifier. The square of the input voltage, V_{IN} is therefore $FkTR_{\mathrm{IN}}$. The Q multiplication process causes the oscillator noise power to fall to the thermal noise floor within the 3dB bandwidth of the oscillator and the square of the output voltage in a 1 Hz bandwidth at an offset to the carrier, Δf, is:

$$\mathrm{V}_{\mathrm{OUT}}^2(\Delta\mathrm{f}) = \frac{\mathrm{FkTR_{IN}}}{4\mathrm{Q}_{\mathrm{L}}^2 \left(\frac{\mathrm{R_{IN}}}{\mathrm{R_{IN}+R_{OUT}}}\right)^2 \left(1 - \frac{\mathrm{Q_L}}{\mathrm{Q}_0}\right)^2} \left(\frac{\mathrm{f}_0}{\Delta\mathrm{f}}\right)^2 \tag{2.45}$$

Writing in terms of $\frac{\mathrm{Q_L}}{\mathrm{Q}_0}$:

$$\mathrm{V}_{\mathrm{OUT}}^2(\Delta\mathrm{f}) = \frac{\mathrm{FkTR_{IN}}}{4\mathrm{Q}_0^2 \left(\frac{\mathrm{Q_L}}{\mathrm{Q}_0}\right)^2 \left(\frac{\mathrm{R_{IN}}}{\mathrm{R_{IN}+R_{OUT}}}\right)^2 \left(1 - \frac{\mathrm{Q_L}}{\mathrm{Q}_0}\right)^2} \left(\frac{\mathrm{f}_0}{\Delta\mathrm{f}}\right)^2 \tag{2.46}$$

Phase modulation can be thought of as linear modulation for small phase deviations much less than 0.1 radian. As the theory is linear, the sideband noise is amplified narrow band noise. The amplifier in the oscillator operates in saturation and it is assumed that the limiting as a result of saturation does not cause any extra components due to mixing. Under hard limiting amplitude noise is suppressed and the input noise is effectively halved. Therefore, the square of the output voltage is halved:

$$\mathrm{V}_{\mathrm{OUT}}^2(\Delta\mathrm{f}) = \frac{\mathrm{FkTR_{IN}}}{8\mathrm{Q}_0^2 \left(\frac{\mathrm{Q_L}}{\mathrm{Q}_0}\right)^2 \left(\frac{\mathrm{R_{IN}}}{\mathrm{R_{IN}+R_{OUT}}}\right)^2 \left(1 - \frac{\mathrm{Q_L}}{\mathrm{Q}_0}\right)^2} \left(\frac{\mathrm{f}_0}{\Delta\mathrm{f}}\right)^2 \tag{2.47}$$

The total output voltage is defined as $\mathrm{V}_{\mathrm{OUTMAXRMS}}^2$ and the phase noise is the ratio of sideband

noise in a 1 Hz bandwidth to the total output power then the phase noise is given as:

$$\begin{aligned} L_f &= \frac{V^2_{OUT}(\Delta f)}{V^2_{OUTMAXRMS}} \\ &= \frac{FkTR_{IN}}{8Q_0^2\left(\frac{Q_L}{Q_0}\right)^2\left(\frac{R_{IN}}{R_{IN}+R_{OUT}}\right)^2\left(1-\frac{Q_L}{Q_0}\right)^2 V^2_{OUTMAXRMS}}\left(\frac{f_0}{\Delta f}\right)^2 \end{aligned} \tag{2.48}$$

We can define the total RF feedback power as the power in the oscillator system, excluding the losses in the amplifier, as P_{RF} or as the power available at the input to the resonator, P_{avo}. Firstly, considering the power defined as the total RF feedback power. It is limited by the maximum voltage swing at the amplifier output and the total impedance in the feedback path:

$$P_{RF} = \frac{(V_{OUTMAXRMS})^2}{R_{OUT} + R_{LOSS} + R_{IN}} \tag{2.49}$$

(2.48) becomes:

$$L_f = \frac{FkT\,(R_{OUT} + R_{IN})^2}{8Q_0^2\left(\frac{Q_L}{Q_0}\right)^2 R_{IN}\left(1-\frac{Q_L}{Q_0}\right)^2 P_{RF}(R_{OUT} + R_{LOSS} + R_{IN})}\left(\frac{f_0}{\Delta f}\right)^2 \tag{2.50}$$

Substituting (2.33) into (2.50), the phase noise is:

$$L_f = \frac{FkT}{8Q_0^2\left(\frac{Q_L}{Q_0}\right)^2\left(1-\frac{Q_L}{Q_0}\right)P_{RF}}\left(\frac{R_{OUT} + R_{IN}}{R_{IN}}\right)\left(\frac{f_0}{\Delta f}\right)^2 \tag{2.51}$$

In the case of a high efficiency oscillator where $R_{OUT} \to 0$, (2.51) simplifies to:

$$L_f = \frac{FkT}{8Q_0^2\left(\frac{Q_L}{Q_0}\right)^2\left(1-\frac{Q_L}{Q_0}\right)P_{RF}}\left(\frac{f_0}{\Delta f}\right)^2 \tag{2.52}$$

In the case where $R_{IN} = R_{OUT}$, then (2.51) simplifies to:

$$L_f = \frac{FkT}{4Q_0^2\left(\frac{Q_L}{Q_0}\right)^2\left(1-\frac{Q_L}{Q_0}\right)P_{RF}}\left(\frac{f_0}{\Delta f}\right)^2 \tag{2.53}$$

If the oscillator power is defined as the power available to the output of the amplifier, P_{AVO}:

$$P_{AVO} = \frac{(V_{OUTRMSMAX})^2}{4R_{OUT}} \tag{2.54}$$

Substituting (2.54) and rearranging, (2.51) becomes:

$$L_f = \frac{FkT}{32Q_0^2\left(\frac{Q_L}{Q_0}\right)^2\left(1-\frac{Q_L}{Q_0}\right)^2 P_{AVO}}\left(\frac{(R_{OUT}+R_{IN})^2}{(R_{IN}.R_{OUT})}\right)\left(\frac{f_0}{\Delta f}\right)^2 \tag{2.55}$$

The phase noise is therefore minimum when $R_{OUT} = R_{IN}$ and the equation becomes:

$$L_f = \frac{FkT}{8Q_0^2\left(\frac{Q_L}{Q_0}\right)^2\left(1-\frac{Q_L}{Q_0}\right)^2 P_{AVO}}\left(\frac{f_0}{\Delta f}\right)^2 \tag{2.56}$$

As the fraction:

$$\frac{(R_{IN}+R_{OUT})^2}{(R_{IN}.R_{OUT})} = 4 \tag{2.57}$$

when $R_{OUT} = R_{IN}$. A general equation that describes all three cases is shown below:

$$L_f = A.\frac{FkT}{8Q_0^2\left(\frac{Q_L}{Q_0}\right)^2\left(1-\frac{Q_L}{Q_0}\right)^N P}\left(\frac{f_0}{\Delta f}\right)^2 \tag{2.58}$$

where:

1. N=1 and A=1 if $P = P_{RF}$ and R_{OUT} =0
2. N=1 and A=2 if $P = P_{RF}$ and R_{OUT} =R_{IN}
3. N=2 and A=1 if $P = P_{AVO}$ and R_{OUT} =R_{IN}

This equation describes the noise performance of an oscillator within the 3dB bandwidth of the resonator, it can be further extended to include the flicker noise corner of the amplifier and the noise outside the resonator 3dB bandwidth. The extended equation is given in 2.59. Section C of this equation gives the phase noise outside of the resonator 3dB bandwidth.

Flicker noise is presented both within and outside the resonator 3dB bandwidth. The flicker noise spectral density, $1 + \frac{f_c}{\Delta f}$, is multiplied by both the noise inside, D, and outside, C, of the resonator 3dB bandwidth. The equation can be further extended to include the noise from any buffer amplifiers at the oscillator output before the measurement device. Assuming the buffer amplifier is phase noise limited, i.e. there is no AM component introduced by the buffer amplifier, the noise is given by $\frac{F_2kT}{C_02P}$ where F_2 is the noise factor of the buffer amplifier, P is the oscillator output power and C_0 is the

output coupler ratio. The complete equation for oscillator phase noise is therefore where F_1 is the cascaded noise factor of the feedback components:

$$L(f) = 10\text{Nlog}\left(\underset{A}{\frac{F_2 kT}{C_0 2P}} + \underset{B}{\left(1+\frac{f_C}{\Delta f}\right)}\left(\frac{F_1 kT}{2P}\underset{C}{\left(\frac{1}{\left[1-\frac{Q_L}{Q_0}\right]^2}\right)}\ldots + \underset{D}{\frac{F_1 kT}{8(Q_0)^2\left(\frac{Q_L}{Q_0}\right)^2\left(1-\frac{Q_L}{Q_0}\right)^2 P}\left(\frac{f_0}{\Delta f}\right)^2}\right)\right) \tag{2.59}$$

where N is the number of oscillators used to make the measurement. It is possible mix the output of two oscillators with similar output frequencies and output power, and measure the phase noise of the down converted signal. In this measurement configuration, $N = 2$ and it is assumed that the two oscillators have identical phase noise spectra, therefore the phase contribution from each oscillator is equal and the actual oscillator phase noise of one oscillator is half the measured phase noise.

2.3.3 Optimisation for Minimum Phase Noise

It is necessary to differentiate (2.58) with respect to the ratio $\frac{Q_L}{Q_0}$ to find optimum conditions for oscillator phase noise. Defining the oscillator power and the input and output impedances is very important as this affects the values of the parameters required for optimum phase noise. Defining the power as P_{RF} and $R_{OUT} = 0$ and assuming that all other terms are constant and defining $Y = \frac{Q_L}{Q_0}$, differentiating (2.58) with respect to Y yields:

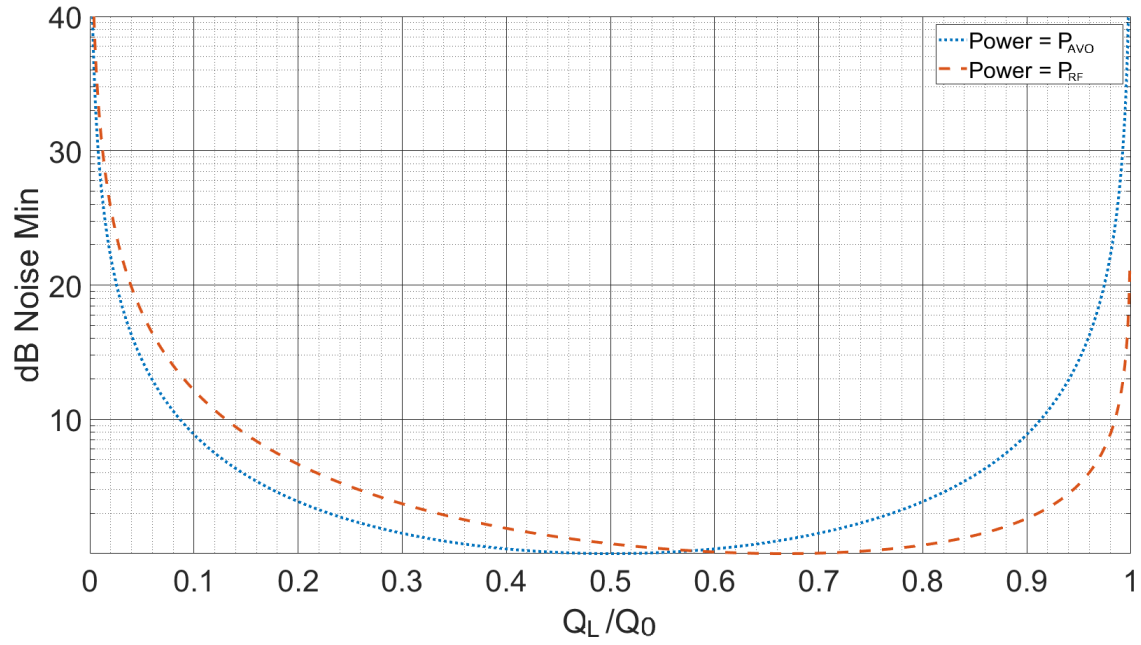
$$\frac{dL(f)}{dY} = \frac{-C(2Y - 3Y^2)}{(Y^2 - Y^3)^2} \tag{2.60}$$

The minimum occurs when this is equal to 0. Solving for Y, the minimum noise occurs when $\frac{Q_L}{Q_0} = \frac{2}{3}$.

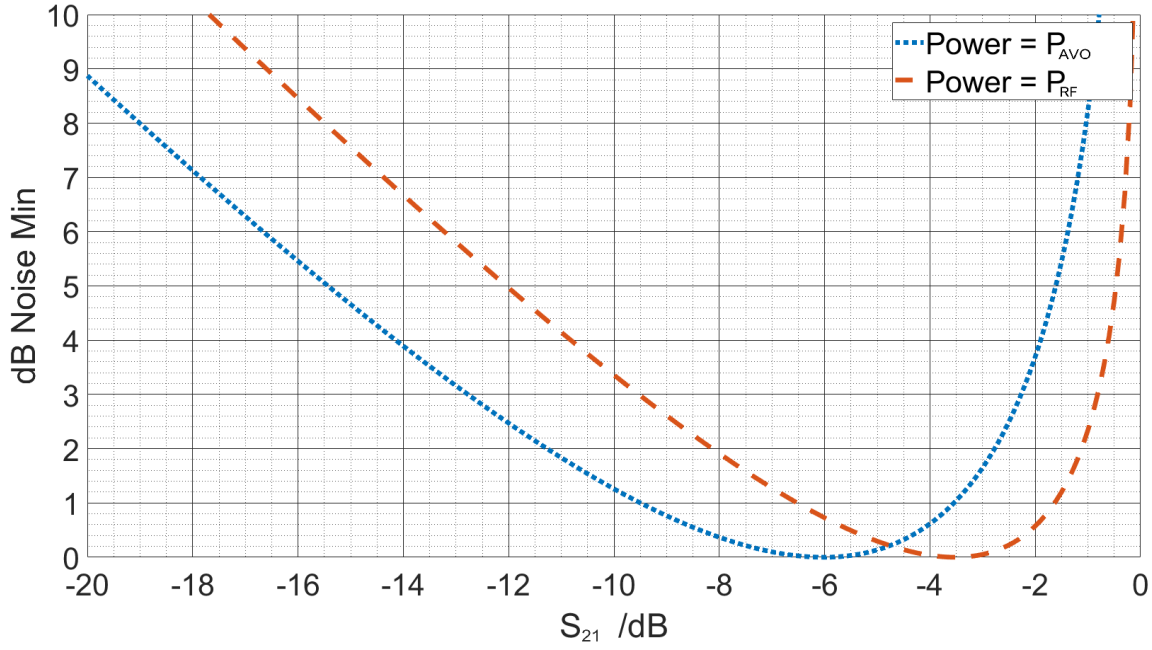
By defining the oscillator power as the power available at the input to the resonator, P_{AVO}, the differential now becomes:

$$\frac{dL(f)}{dY} = \frac{-C(4Y^3 - 6Y^2 + 2Y)}{(Y^4 - 2Y^3 + Y^2)} \tag{2.61}$$

assuming once again all other terms except the ratio $\frac{Q_L}{Q_0}$ are constant and substituting Y for $\frac{Q_L}{Q_0}$. This



(a) Phase noise degradation with varying $\frac{Q_L}{Q_0}$ variation for two different power definitions [18].



(b) Phase noise degradation with varying S_{21} variation for two different power definitions.

Figure 2.6: Oscillator phase noise degradation as a result of varying $\frac{Q_L}{Q_0}$ and S_{21} for two different power definitions.

differential is equal to 0 when the ratio $\frac{Q_L}{Q_0} = \frac{1}{2}$, therefore, for minimum phase noise half of the power is dissipated in the resonator [19].

A comparison plot showing the phase noise variation against the ratio $\frac{Q_L}{Q_0}$ for the two different power definitions is shown in Figure 2.6a. This plot is a plot of (2.60) and (2.61) where Y=$\frac{Q_L}{Q_0}$.

These plots demonstrate the degradation of phase noise with varying $\frac{Q_L}{Q_0}$ and S_{21}. Figure 2.6b demonstrates that the optimum resonator insertion loss for minimum phase noise is 6dB when the oscillator power is defined at the input to the resonator, P_{AVO}. Its important to note that the phase noise degradation is small, less than 1dB from the optimum, if the insertion loss of the resonator is in the range 3.5dB to 9.5dB. Likewise for when the oscillator power defined as the total power in the oscillator system, excluding the losses in the amplifier, P_{RF}, the minimum occurs when the resonator insertion loss is 3.6dB and there is less than 1dB degradation from the minimum if the resonator insertion loss is in the range, 1.5 to 6.5dB. In this thesis, the oscillator power will be defined as the power available to the resonator input.

In order to sustain oscillation, the phase around the feedback loop must be equal to 0 or an integer multiple of 360°. If this condition is not met then the effective Q of the resonator is greatly reduced as the oscillator frequency is no longer at the resonant frequency of the resonator. The effective Q is reduced in proportion to the phase slope of the resonator, $\frac{\Delta\varphi}{\Delta\omega}$. This also causes the insertion loss of the resonator to increase which is compensated for by the amplifier as its gain must now increase. It has been shown experimentally by Cheng and Everard in [20], that the noise performance is degraded in the thermal and flicker noise regions by a factor of $\cos^4\vartheta$ where ϑ is the open loop phase error. Therefore, a 20° phase error will cause approximately 1dB degradation to the oscillator phase noise but 45° error causes 6dB degradation.

2.3.4 Oscillator Phase Noise Spectrum

The spectrum of the phase noise in a real oscillator can be broken down into four sections with different characteristics as shown in Figure 2.7. In the decade from 1 to 10 Hz, the up converted flicker noise from the amplifier is dominant and rolls off at a 30dB/decade rate. The next decade shows the up converted thermal noise due to the Leeson effect, dominates the spectrum rolling off at 20dB / decade. Moving further away from the carrier we can see that the flicker noise from the amplifier, as well as

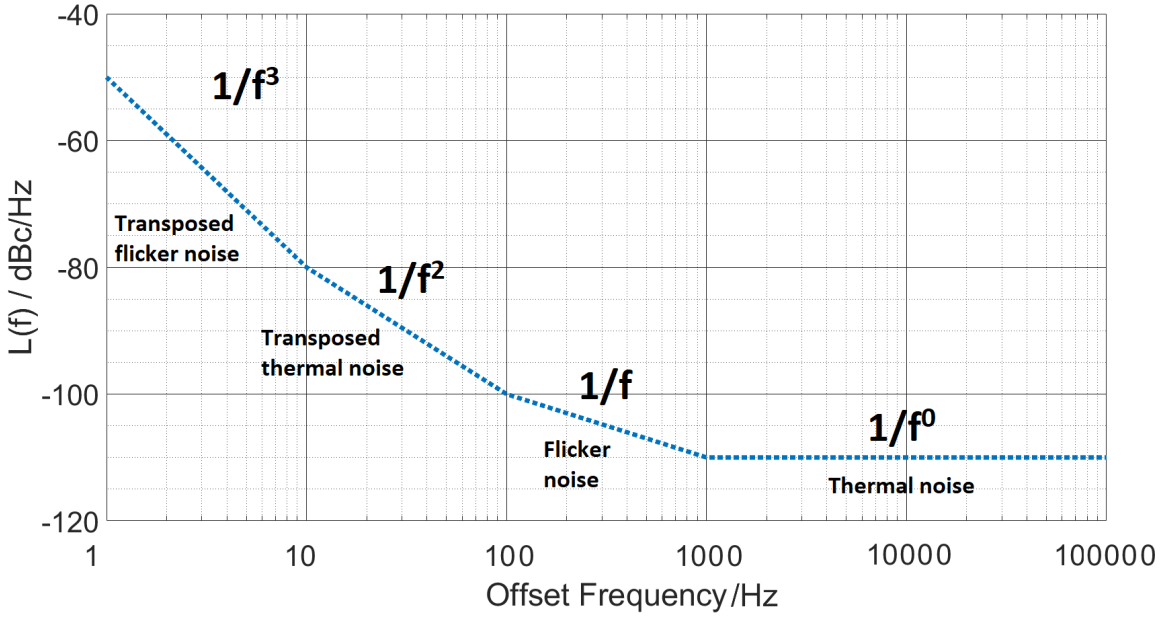


Figure 2.7: Typical oscillator phase noise spectrum with transposed flicker and thermal noise to the carrier frequency.

any other components in the feedback loop, dominates before the flicker noise corner is reached as the spectrum becomes flat where the thermal noise is dominant. The far from carrier thermal noise of a device can be calculated from the following equation [5]:

$$L(f) = -177 + NF + G - P_{IN} \tag{2.62}$$

given in dBc/Hz, where -177dBm is the phase noise contribution to the Johnson-Nyquist noise in a 1 Hz bandwidth (assuming AM and PM contributions are equal), NF is the noise figure of the device under test, DUT, G is the gain of the DUT and P_{IN} is the power at the input of the measurement system.

Not all oscillator phase noise spectra resemble this exactly, in the case where a low Q resonator is used, the flicker noise corner could within the 3dB bandwidth of the resonator. The spectrum may then not include much if any noise resembling $\frac{1}{f}$ characteristic as the transposed flicker and thermal noise are much higher.

Conversely, a high Q resonator oscillator phase noise spectrum may not include much transposed thermal noise. This is due to the thermal noise power being lower than the transposed flicker noise

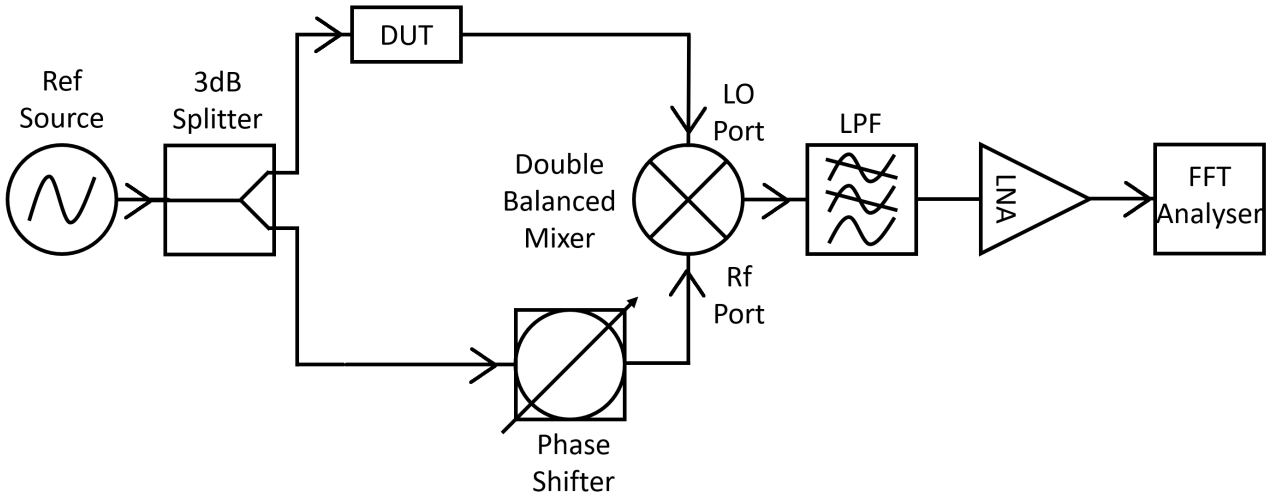


Figure 2.8: Single channel residual phase noise measurement system where two identical devices are being measured.

that dominates up to a frequency where the flicker noise spectrum is most prominent.

2.4 Cross correlation residual phase noise measurement system

It is important to obtain accurate measurements of the noise introduced into any RF and microwave system in order to ascertain the ultimate limit of a device's phase noise performance. Residual noise, is the noise introduced by any two port device into a system and can limit the accuracy of residual phase noise measurements of components such as mixers, amplifiers and phase shifters commonly used in high frequency circuits. The residual phase noise of a 2 port device can be measured using the single channel measurement channel system shown in figure 2.8. A reference signal is equally split and fed into the input of the device under test, DUT. In one arm of the system, a 90° phase shift is applied to the propagating signal in order to ensure the signals at the LO and RF ports of a double-balanced mixer are in quadrature. It is possible to measure two devices, one in each arm after the 3dB splitter, assuming they are identical, however the residual phase noise spectrum will be 3dB higher than a single device measurement. A measurement of the residual phase noise introduced by the system can be made by removing the DUT.

When the signals at the RF and LO ports are in quadrature, the mixer is most sensitive to phase

fluctuations and least sensitive to amplitude noise [21], and used as a phase detector in this setup. The output of the phase detector is then low pass filtered to remove unwanted RF components and passed to a fast Fourier transform, FFT, analyser to plot the noise spectral density of the phase noise introduced by the DUT. It is assumed that the phase noise from the reference signal is correlated and therefore cancels.

This measurement system introduces noise from the mixer, splitters and internal amplifiers and filters within the fast Fourier transform, FFT, analyser that increases the noise floor of the measurement system. It is possible to reduce the noise floor of the system by using two channels and calculating the cross correlation function of the two single channel FFT outputs. Any noise introduced in each channel from the mixers, splitters and filters will be uncorrelated and can therefore be suppressed. A diagram of the cross correlation measurement system is shown in Figure 2.9

The noise at the output of each mixer is presented by Rubiola [22] and can be modelled as two noisy signals:

$$\mathrm{x(t) = a(t) + c(t) \leftarrow FFT \rightarrow X(f) = A(f) + C(f)} \tag{2.63}$$

$$\mathrm{y(t) = b(t) + c(t) \leftarrow FFT \rightarrow Y(f) = B(f) + C(f)} \tag{2.64}$$

where *a(t)* and *b(t)* are the uncorrelated noise signals from either channel and *c(t)* is the DUT noise. The correlated DUT noise is present in both channels and by taking the cross spectrum of the two signals with N number of averages, then:

$$\overline{\mathrm{S_{XY}}} = \frac{1}{\mathrm{N}} \sum_{\mathrm{n=1}}^{\mathrm{n=N}} [(\mathrm{A_n + C_n}).(\mathrm{B_n + C_n})\star] \tag{2.65}$$

The $\star$ denotes complex conjugate. Expanding the brackets yields:

$$\overline{\mathrm{S_{XY}}} = \frac{1}{\mathrm{N}} \sum_{\mathrm{n=1}}^{\mathrm{n=N}} [(\mathrm{A_n B_n}\star) + (\mathrm{A_n C_n}\star) + (\mathrm{C_n B_n}\star) + (\mathrm{C_n C_n}\star)] \tag{2.66}$$

Assuming there is no correlation between *a(t)* and *b(t)*, then increasing the number of cross correlations, N, will cause the uncorrelated to reduce proportional to the number cross correlations. The final CC term that represents the power spectral density of the DUT is left.

Walls [23] demonstrated a cross correlation system that improved on the single channel noise

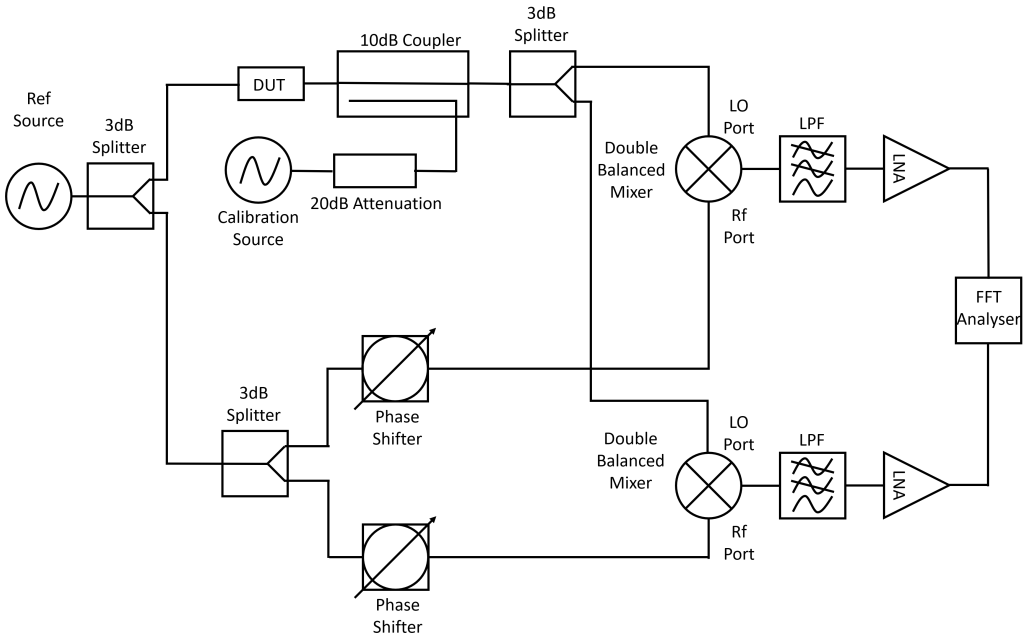


Figure 2.9: Cross correlation residual phase noise measurement system.

floor by approximately 18dB achieving a noise floor of -197dBc/Hz. Bale [24] has shown that the improvement of the system noise floor by approximately 5dB per every factor of 10 increase to the number of correlations using two HP11848 phase noise interfaces. Therefore, the cross correlation method can suppress the uncorrelated noise in each channel by a factor of $\sqrt{\mathrm{N}}$ where N is the number of cross correlations carried out. In this thesis, the same system as used by Bale [24], is often used for residual phase noise measurements.

To calibrate the cross correlation system, a tone of known frequency and amplitude offset from the carrier is injected via the directional coupler in the top channel in figure 2.9. The data is windowed to reduced spectral leakage that occurs as result of the FFT. A Hann window is used to find the offset voltage from the carrier because it has low side lobe levels of -32dB, making it suitable for measuring signals with large amplitude such as the calibration tone. This information is then used in the software to calibrate the measurement and the reference tone can be removed. When using this measurement system, the measurement has always been made using the Flat-top window as this type of data windowing has superior frequency accuracy when compared to the Hann window and increased noise bandwidth.

Chapter 3

1.5 GHz dielectric resonator oscillator

3.1 Introduction to Dielectric Resonator Oscillators

In this chapter the design, manufacture, and measurements of the phase noise of a dielectric resonator oscillator (DRO) at 1.5 GHz is presented. It extends the work presented by this group as part of an ultra-low phase noise atomic clock [25], and is a modified version of a 1.2 GHz DRO developed by this group [26]. The new 1.5 GHz DRO is more compact, fully electronically tunable and offers improved phase noise performance at offsets greater than 1 kHz compared to the previous version. State-of-the-art phase noise measurements of oscillator phase noise of -164.15dBc/Hz at 10 kHz offset with far from carrier noise of <-178dBc/Hz at a carrier frequency of 1.486 GHz are presented.

Dielectric resonators are often used as the frequency selective element in a ultra low phase noise oscillators at frequencies greater than 1 GHz and up to 40 GHz. A dielectric resonator is capable of handling greater power levels than a crystal resonator whilst having high Q_0. Furthermore, they are typically smaller than traditional microwave cavities where the material enclosed is usually air. This is because the resonant frequency of a cylindrical microwave cavity of the TE_{nmp} mode is inversely proportional to the dimensions of the cavity and the square root of the product of the relative permittivity and permeability of the material filling the cavity as demonstrated in 3.1.

$$f_r(TE_{mnp}) = \frac{c}{2\pi\sqrt{\mu_r\varepsilon_r}}\sqrt{\left(\frac{\chi'_{nm}}{a}\right)^2 + \left(\frac{p\pi}{d}\right)^2} \tag{3.1}$$

Where χ'_{mn} is the n^{th} zero of the derivative of the Bessel function of the first kind of order m. The puck radius is given by a, d cavity height, c is the speed of light μ_r is the relative permeability and ε_r is the relative permittivity of the dielectric material filling the cavity.

Air is typically used to fill microwave cavities. The resonant frequency of the dielectric resonator (DR) is dependent on the dimensions and permittivity of the dielectric material, which are typically higher than that of air resulting in a smaller resonator at the same resonant frequency. Furthermore, Q_0 is inversely proportional to the surface resistivity of the material used to manufacture there cavity and therefore changes to the material or variation in the material purity causes variation in the unloaded Q.

A dielectric resonator is constructed from a piece of dielectric material surrounded by an enclosure. The piece of dielectric is commonly referred to as a puck and is made of a material with a high relative permittivity, typically in the range 20-80 [27]. The range of resonant frequencies is from a few GHz up to a few tens of GHz, though this depends on the size of the puck and ability to manufacture small dielectric material. Example dielectric resonators available from EXXELIA TEMEX resonate at frequencies up to 37 GHz [28].

The puck is surrounded by a material of much lower permittivity, typically air. The large difference in permittivity between the dielectric material and the medium surrounding it causes the majority of the microwave field to be confined within the dielectric material resulting in the formation of standing waves. There is however a small proportion of the field that escapes the dielectric material into the air that can be coupled to external probes.

The metal enclosure is placed over the dielectric and coupling probes to stop radiation losses. The enclosure must be designed in such a way that the metal walls are far enough away from the resonator to not perturb the magnetic field around the puck and therefore degrade the Q. If designed correctly, the resonator quality factor is almost independent of the loss tangent of the enclosure walls and dependent only on the loss tangent of the dielectric material. The product $Q \times f$ is approximately constant with quality factors in the order of 10s of thousands are achievable in the high Q TE_{011} mode. The Q_0 of an ideal DRO is calculated using (3.2) [29].

$$Q_0 = \left(\frac{1}{Q_c} + \frac{1}{Q_d} \right)^{-1} \tag{3.2}$$

where Q_c is the Q of the cavity with lossy conducting walls but lossless dielectric and Q_d is the Q of the cavity with a lossy dielectric filling but perfectly conducting walls. If we assume that the power dissipated by the dielectric and lost in radiation is small then the first term becomes very large and $Q_0 \approx Q_d$. Therefore, $Q_0 \approx 1/\tan\delta$ [29].

The size of the dielectric puck at microwave frequencies is small compared to an air filled cavity resonating at the same frequency as the dimensions are determined by the dielectric permittivity. (3.3) can be used to calculate the dimensions from permittivity and resonant frequency or resonant frequency from given dimensions and permittivity as described by Kajfez and Guillon in [30].

$$f_r(TE_{mnp}) = \frac{1}{2\pi\sqrt{\mu_r\varepsilon_r}}\sqrt{\left(\frac{\chi'_{mn}}{a}\right)^2 + \left(\frac{p\pi}{L}\right)^2} \tag{3.3}$$

Where χ'_{mn} is the n^{th} zero of the derivative of the Bessel function of the first kind of order m. The puck radius is given by a, L is the puck height, μ_r is the relative permeability and ε_r is the relative permittivity of the dielectric material. In a cavity resonator the third subscript p would always be an integer number as this denotes the number of half wavelengths variations of the field. In a dielectric resonator, the field variation within the resonator height L is less than one half wavelength which is a result of the end effects of the resonator at points z = 0 and z = L. The resonance condition for all resonant conditions is shown in [30] to be

$$\beta L = \frac{\varphi_1}{2} + \frac{\varphi_1}{2} + l\pi, \quad l = 0, 1, 2, 3... \tag{3.4}$$

where the phase angle in one region, φ_n is:

$$\frac{\varphi_n}{2} = \arctan\left(\left(\frac{\alpha_n}{\beta}\right)\coth(\alpha_n L_n)\right) \tag{3.5}$$

The separation constants in (3.5), α_n and β are given by:

$$\alpha_n = \sqrt{\left(\frac{x_{01}}{a}\right)^2 - k_0^2\varepsilon_{rn}} \tag{3.6}$$

$$\beta = \sqrt{k_0^2\varepsilon_r - \left(\frac{x_{01}}{a}\right)^2} \tag{3.7}$$

where k_0 is the propagation constant of the mode in the regions outside of the puck. This constant is

unknown as the mode frequency is unknown, however it must be greater than or equal to a constant in order for the eigenvalues of a dielectric to be real [31]. For all modes except TE_{11}, this value is χ^2_{mn}, from [31]:

$$k_0 \geq \frac{\chi_{mn}}{\sqrt{\varepsilon_r - 1}} \frac{1}{a} \tag{3.8}$$

In the case of $l = 0$, the mode is TE_{01p} and p can be found using the following equation:

$$p = \frac{1}{\pi}\left(\frac{\varphi_1}{2} + \frac{\varphi_2}{2}\right) \tag{3.9}$$

Assuming that the distances between the resonator ends and the metal enclosure, L_1 and L_2, are infinite and therefore the resonator is isolated in free space ($\varepsilon_{r1} = \varepsilon_{r2} = 1$), the resonance condition simplifies to

$$\beta_z L = 2 \arctan\left(\frac{\alpha}{\beta}\right) \tag{3.10}$$

from which p can be calculated and an estimate of the resonant frequency can be obtained.

Whilst crystal oscillators offer high Q_0 in the order of $10^5 - 10^6$, they cannot handle as high powers as a dielectric resonator which is capable of handling powers from a few milliwatts to a few watts. Further, their range of frequencies are limited by their size and would have to be made very small in order to operate at microwave frequencies. This type of oscillator is attractive for small circuits at low frequencies. A 10 MHz stress compensated (SC) cut, oven controlled crystal oscillator has been developed by this research group [3], with low flicker noise corners of 150 Hz and phase noise of -123dBc/Hz at 1 Hz offset. A 5 MHz crystal oscillator demonstrating -132dBc/Hz phase noise at 1 Hz offset is presented in this thesis in Chapter 6.

3.2 Current state-of-the-art

There are many papers demonstrating low phase noise at high frequencies in DROs [25, 26, 32–35], however, few provide details of the full design process and cannot produce ultra-low phase noise performance at large frequency offsets from the carrier.

The complete design of a 10 GHz tunable ceramic dielectric resonator oscillator has been developed by this research group [32] demonstrating -135dBc/Hz at 10 kHz offset. The coupling probes were asymmetric to move the resonant frequency of an unwanted resonance at 9.21 GHz to 7.68 GHz and

to achieve an insertion loss of 5.5dB at resonance. Q_l was measured as 8,200, using 4.17, $Q_0 = 17,400$. This oscillator uses SiGe devices that produce an output power approximately 15dBm. The power available to the resonator is approximately 12dBm as there is a 3dB output coupler placed between the amplifier output and resonator input, this was implemented to couple the oscillator output. The oscillator frequency can be tuned by applying a bias voltage to the electronically tunable phase shifter that operates from 0-10V bias. The tuning range of the oscillator is from 9.8466 GHz to 9.8472 GHz.

This work was extended by Everard and Theodoropoulos, [26] where the measured phase noise at 10 kHz offset from a 1.25 GHz carrier was -170dBc/Hz. The far from carrier noise was measured to be -180dBc/Hz. The amplifiers used were designed to operate in 'push-pull' configuration of transistors to increase the output power. This DRO was modified by a former PhD student from this research group, Tsvetan Burtichelov, to operate at 1.5 GHz. A measurement of the oscillator operating at 1.5 GHz is presented in [25] demonstrating -163dBc/Hz at 10 kHz offset. The modified 1.5 GHz puck had a measured insertion loss of -7.34dB at 1.488 GHz and a Q_l of 27,000 [36]. The Q_0 was calculated to be 47,330.

A 3.8 GHz DRO developed by this research group [33] demonstrates ultra low phase noise of –150dBc/Hz at 10 kHz offset. The compact oscillator is housed in an aluminium enclosure and offers a tuning range of 200 kHz. The resonator has a dielectric constant of 30 and an Q_0 of the 30,000. The insertion loss of 6dB is achieved by 'trimming' printed microstrip probes. A push-pull configuration of amplifiers, similar to that used in the 1.25 GHz DRO, was used. Rat race couplers are used to divide the input power equally between the amplifiers and recombine the power from the output of each amplifier to increase the total output power.

Yazdani et al. [34] have achieved -90dBc/Hz at 10 kHz offset from 9.44 GHz carrier with an output power of 11.4dBm. The design presented in this paper uses a unique DR design that is optimised for the dominant mode and is shown to be very compact (less than 20 mm diameter). This design does however exhibit low output power and the phase noise plot also shows a high flicker noise corner as the noise floor has not been reached at 1 MHz offset frequency from the carrier. There is no further detail concerning the resonator design nor the Q_0 which could be a factor that has limited the phase noise response. This design focuses more on the overall size of the DRO and hence the oscillator phase noise response is degraded.

Wibisono et al. [35] have demonstrated phase noise performance of -144dBc/Hz at 10 kHz offset from a 2.3 GHz carrier. Their proposed design uses a $\lambda/4$ stub matching network to increase the coupling to the dielectric resonator. As a result, the oscillator output power increases from 10.8dBm to 13.0dBm resulting in a 9dB improvement in the oscillator phase noise at 10 kHz offset from carrier. The Q is relatively low however at approx. 7300 and the noise floor (>100 kHz) of the oscillator is not presented. Their design differs from the feedback oscillator configuration that is presented in this chapter as a common base transistor amplifier is used. This configuration is used as a low input impedance is presented by the common base amplifier however, when compared with common emitter transistor amplifiers, the current gain and power gain is significantly smaller which limits the oscillator power and has the potential to degrade the oscillator phase noise.

Boroditsky et al. [37] have achieved -150dBc/Hz at 10 kHz and -156dBc/Hz and >1 MHz offsets using an 111.111 MHz Oscillator Controlled Crystal Oscillator (OCXO) multiplied to 1 GHz. As discussed, a crystal oscillator typically has higher far from carrier phase noise when compared to DROs as well as being unable to handle high output powers. The phase noise plot in this paper is interesting as the phase noise appears to be constant from 50-110 Hz offsets before rolling off at around 30dB/decade thereafter until the noise floor is reached. The oven controlled oscillator is temperature stable and uses the 3rd overtone frequency in order to reduce close to carrier phase noise. At higher offsets however the phase noise of the voltage controlled oscillator in the feedback loop begins to dominate hence the flat portion of the phase noise plot and subsequent degraded phase noise.

Commercially available DROs operating at similar carrier frequencies such as the Ingenieurbüro Gronefeld GDRO2856 [38] operating at 2.856 GHz offers output power of 17dBm, which is comparable to the DRO presented in this chapter, but at 10 kHz offset from the carrier the measured phase noise performance is -155dBc/Hz. The Raditek RDRO-2-3-13d-12V-S12 is a frequency tunable DRO operating at 2-3 GHz though it offers -95dBc/Hz at 10 kHz offset when measured at 6 GHz carrier frequency, there are unfortunately no measurements for this DRO in the 2-3 GHz range in the datasheet [39].

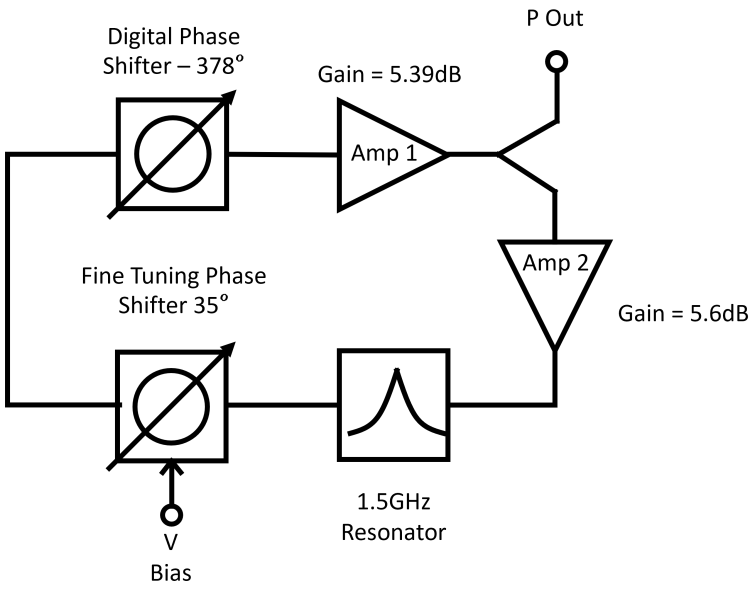


Figure 3.1: Block diagram of the 1.5GHz DRO developed in this chapter.

3.3 1.5 GHz DRO design and measurements

In this section the design, manufacture and measurements of each individual module within the DRO are presented. The final DRO assembly is presented at the end with phase noise measurements of the two DROs that have been built. A block diagram of the DRO is shown in Figure 3.1. The complete oscillator consists of the high Q dielectric resonator followed by a spurious resonance filter, two phase shifters, the first is a fine tuning voltage controlled phase shifter and the second a coarse tuning digital phase shifter giving a tuning range greater than 360°. Following the phase shifters there is an amplifier immediately before the output coupler. At the second output arm of the coupler is the second gain stage, this is necessary to ensure sufficient loop gain and to ensure there is maximum power available at the resonator input.

The coupler is used to provide some attenuation from the first gain stage to the second to reduce the saturation of the second amplifier, therefore, decrease the flicker noise contribution to the oscillator phase noise. All of these conditions are necessary for optimum oscillator phase noise.

3.3.1 Resonator

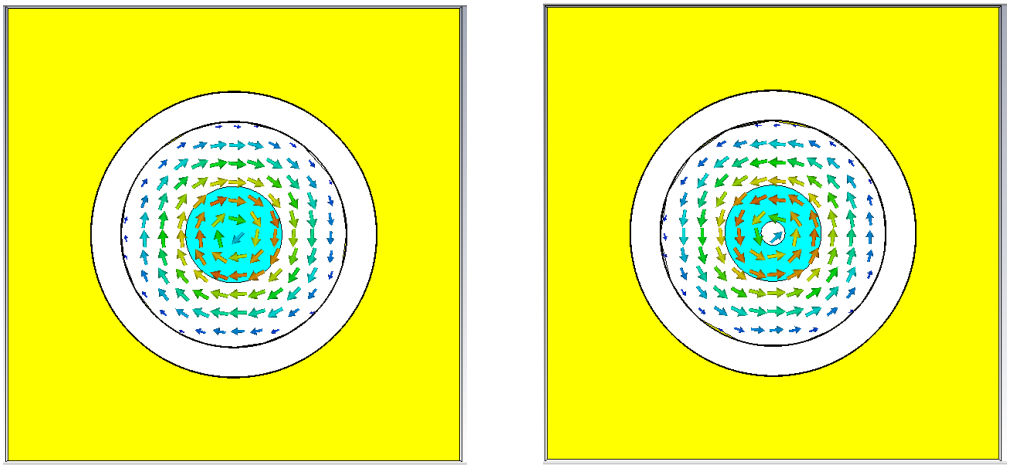
Scaling 3.8 GHz DRO

A 3.8 GHz dielectric resonator oscillator has previously been developed by this research group achieving phase noise performance of -125.6dBc/Hz at 1 kHz offset and -153dBc/Hz at 10 kHz offset. This oscillator was built up in modules before final assembly, the same approach presented in this chapter. The dielectric puck in the 3.8 GHz DRO is made from Barium Titanate, with tan(δ) of approximately 1.34×10^{-5} and ε_r= 29. As most of the field within a Dielectric Resonator (DR) is confined to within the puck, the Q_0 of an ideal resonator in free space is dependent only on the loss tangent of the puck material. The loss tangent is a calculated value based on measured Q_0 and resonant frequency of the 3.8 GHz pucks. We assume that $Q_0 \times f_0$ is constant for a dielectric material, this product has been calculated to be 112,000 at 3.8 GHz from measurements of unbonded pucks in free space.

At 1.5 GHz the calculated Q_0 of the puck in free space is 74,700, however the real value is expected to be much less than this due to the support and the metal enclosure of the puck in the real oscillator dissipating some of the energy in the resonator. The 3.8 GHz puck in free space has an Q_0 of approximately 30,000 however the resonator used in the 3.8 GHz oscillator [33] has Q_0 of 19,700. The Q is degraded because the resonator puck is not in free space, rather the puck is mostly surrounded by air and is supported by an alumina tube used to move the dielectric material way from the metal enclosure base which would degrade the Q. However, the support dissipates some energy resulting in the unloaded Q decreasing.

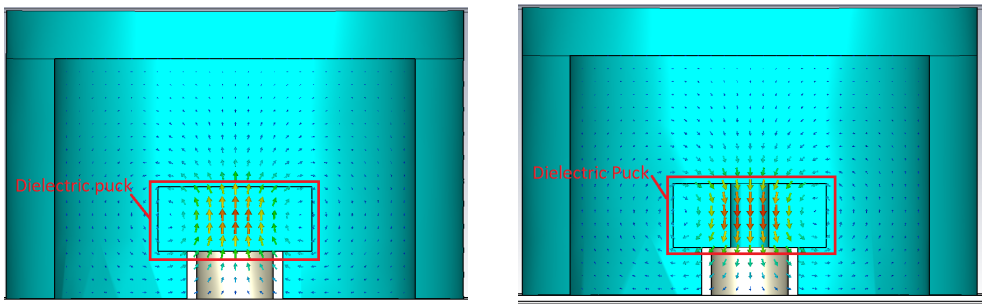
The original 3.8 GHz puck had the centre portion of the puck removed as the electric field is 0 at the centre of the puck but is maximum at approximately $\frac{3}{4}$r. The magnetic field is maximum in the centre of the puck and therefore removing some material in the middle will not disrupt the field but can increase the Q_0 and slightly increase the resonant frequency. The 3.8 GHz puck dimensions were obtained and used to model the resonator in 3D EM modelling software, CST studio suite. The model was then simulated using the Eigenmode solver, without external excitation to obtain resonant modes.

Figures figs. 3.2 and 3.3 are the simulated E and H fields in the dominant TE_{011} mode of the 3.8 GHz resonator. The field patterns are plotted on a plane cutting through the middle of the pucks



(a) With middle section. (b) Middle section removed.

Figure 3.2: Bird's Eye view of model of the pucks used in Eigenmode simulation showing E-Field maximum.



(a) With middle section. (b) Middle section removed.

Figure 3.3: Cross section view of the Eigenmode simulation of the 3.8 GHz pucks, showing the positions of the maximum H-Field.

both vertically and horizontally. It can be seen that both the magnitude of the E and H field increase with the removal of the centre section of the resonator puck, as demonstrated by the darker arrows in both fields. Using the post processing step in CST, Q_0 is calculated to increase from 38,000 to 39,000 (+2.63%). Furthermore, the frequency increased from 3.838 GHz to 3.856 GHz (+0.469%) with the centre portion removed. As the product of Q_0 and f is constant, the dimensions of the original 3.8 GHz puck were scaled in size by the same ratio as frequency, 3.8GHz/1.5GHz = 2.53, and simulated using the eigenmode solver in CST. This solver is useful at this stage because the results from this simulation are used to determine the resonant modes in a shorter time than either the frequency domain or time domain solver. This solver does not use ports to excite the structure like the time

Puck	3.8 GHz	Scaled to 1.5 GHz
Outer Radius /mm	8.01	20.7
Inner Radius /mm	2	5.06
Height /mm	6.68	16.9
Support Outer Radius/mm	5	12.65
Support Inner Radius/mm	4	10.12
Support Height /mm	5	12.65

Table 3.1: Original and scaled 3.8 GHz puck dimensions.

Puck No.	Measured	Scaled
Outer Radius /mm	21.4	20.7
Inner Radius /mm	11.1	5.06
Height /mm	15.77	16.9
Support Outer Radius/mm	16	12.65
Support Inner Radius/mm	9.19	10.12
Support Height /mm	27.42	12.65

Table 3.2: Real 1.5 GHz Puck Dimensions.

domain and frequency domain solvers so insertion loss at the resonant frequency is not calculated. The dimensions of the 3.8 GHz dielectric puck and the scaled dimensions are shown in table 3.1.

The dominant mode was simulated to be 1.500 GHz with a Q_0 of 37,000 calculated using the CST post processing Q-factor calculation tool. This is approximately half of the expected value of the Q_0 of a puck this size in free space.

Modelling the real puck

The DROs developed in this research ultimately made use of a readily available pucks that had been previously used by Dr Tsvetan Burtichelov in his research into the development of an atomic clock within thin research group [25]. These pucks are modified version of the ones used in the 1.2 GHz DROs developed by this group by Dr Konstantinos Theodoropolous [26]. To change the operating frequency from 1.2 GHz to 1.5 GHz for use in the atomic clock, the height and diameter of the pucks were reduced. These pucks are used in the DROs developed here, with their dimensions given in table 3.2.

Equations (3.3)-(3.10) can be used to calculate the resonant frequency of the TE_{01p} mode. As ε_r

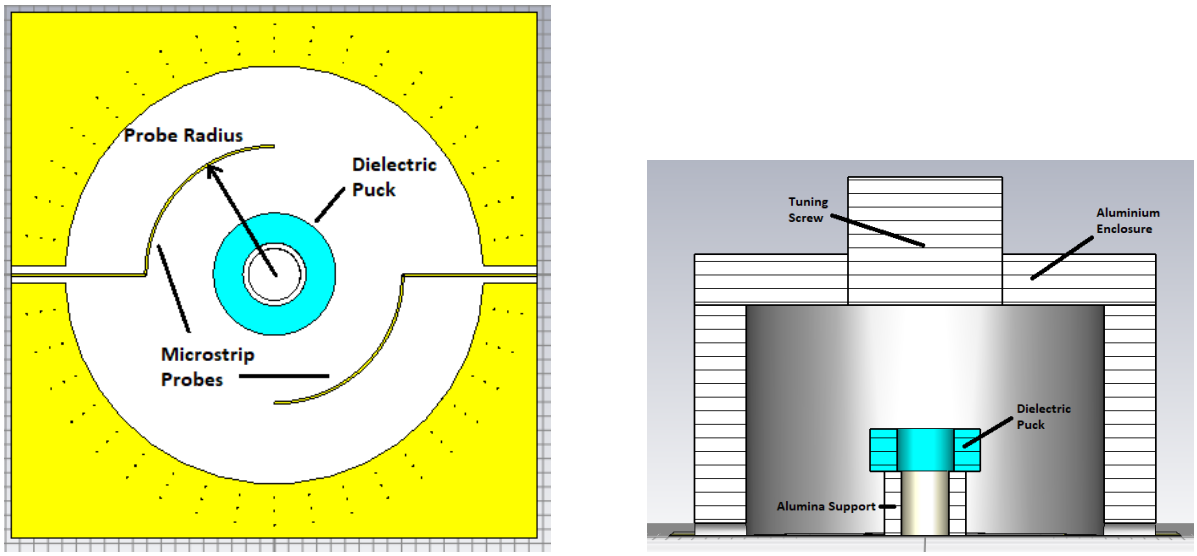
= 29 and a = 21.4 mm, $k_0 \geq 0.0212$. As $k_0 << (\chi_{mn}/a)^2$, we can simplify (3.9) as $\alpha = \beta$. Therefore p is approximately 0.5 and an estimate of the resonant frequency in the TE_{01p} mode is 1.334 GHz. The resonant frequency measured previously by Dr Tsvetan Burtichelov in [36] was 1.488 GHz and there is approximately 10% difference between the calculated and measured value that is caused firstly by the assumption that the resonator is in free space in the calculation and secondly the fact that the real resonator has an inner hole. Both the assumption and the differing puck shape cause the frequency to increase as in reality the enclosure walls are not infinitely far away and perturb the field around the puck.

The support is made from low loss alumina and its purpose is to increase the distance between the PCB on which the probes will be printed and the metal base plate. This reduces reduces the resonator losses in the walls and base, keeping the resonator Q_0 high and dependent only on the loss tangent of the dielectric puck. The loss tangent of alumina is 4×10^{-4}, which is greater than the less tangent of Barium Titanate and the dielectric permittivity is approximately 9.6, which smaller than the dielectric permittivity of Barium Titanate. This will degrade Q_0, though much less than would be the case if the puck was sat directly on top of the PCB or the metal base.

Enclosure design

The outer enclosure that surrounds the dielectric puck must be carefully designed so not to cause unwanted losses in the resonator and therefore degrade the Q_0. Yet, it is necessary as it removes reduces radiation losses. In the past this research group has generally made the enclosure 3 times bigger than the resonator itself to achieve this.

The resonator was modelled in CST and simulated using the Eigenmode solver to find optimum enclosure dimensions and their affect Q_0 and f_0. The PCB substrate, 0.5 mm I-Tera MT40 [40] substrate with $\varepsilon_r = 3.45$ and a loss tangent of 0.0031, was modelled in CST and is the substrate that is to be used for all manufactured PCBs in this chapter. Firstly, the enclosure height was varied whilst keeping the radius constant. A radius of 100 mm was chosen to reduce the effect of the side walls on Q_0 and f_0, as it is greater than 3 times the DR outer radius. The radius of the enclosure has been typically set to 3 times the DR radius in previous resonators developed to reduce the effect of the metal walls on Q_0 and f_0 whilst keeping the enclosure size as small as possible to reduce its weight



(a) Bird's Eye view of the DR model in CST. (b) Cross Section of DR model in CST.

Figure 3.4: CST frequency domain simulation used for probe and enclosure design.

and material cost. In simulations these considerations are not so important for this set of simulations. Table 3.3 shows how increasing the enclosure height causes an increase in Q_0 and a decrease in f_0.

The Q_0 increases until it tends to a maximum value of 37300. The calculated Q_0 of the dielectric resonator is approximately double the simulated value here and that is due to metal enclosure and alumina support. From these simulations it is clear that the height of the enclosure should be large in order to keep the Q_0 high. However, there is a maximum value that can be obtained and that occurs when $H_{enclosure} \approx 2.78 \times (H_{puck} + H_{support})$. Furthermore, the degradation to Q_0 when the enclosure is less than 3% when $H_{enclosure} \approx 1.85 \times (H_{puck} + H_{support})$. This could be beneficial in keeping costs and weight down in the manufacturing process as well as reducing the overall size of the resonator for small changes in Q_0.

A similar set of simulations were run in order to investigate the effect of variation of the enclosure radius on Q_0 and f_0. The enclosure height was kept at a constant 90 mm as at this height the Q_0 was degraded by only 600 (1.6%) and the resonant frequency of 1.499 GHz was closest to 1.5 GHz out of all the simulations run varying the height of the enclosure. Table 3.4 shows the results of these simulations.

A similar pattern emerges with increasing the enclosure radius as the Q_0 increases up to a maximum

Enclosure height/mm	Q_0	f_0 / GHz
50	20300	1.616
60	30700	1.537
70	34600	1.514
80	36100	1.504
90	36700	1.499
100	37100	1.496
110	37300	1.494
120	37300	1.493

Table 3.3: Eigenmode solver simulated Q_0 and f_0 with varying enclosure height.

Enclosure radius /mm	Q_0	f_0 / GHz
40	29700	1.57
50	33900	1.54
60	35600	1.52
70	36300	1.51
80	36600	1.50

Table 3.4: Eigenmode solver simulated Q_0 and f_0 with varying enclosure radius.

value whilst the resonant frequency reduces. This occurs when $R_{enclosure} \approx 3.74 \times R_{puck}$ however there is less than 3% reduction in Q_0 when $R_{enclosure} \approx 2.8 \times R_{puck}$. These simulations have shown that increasing both the enclosure height and radius increases Q_0 of the resonator whilst decreasing f_0 but there is also a maximum achievable Q_0. It is also possible to achieve a high Q_0 whilst not using the maximum radius or height for the enclosure if a small degradation of 3% is permissible.

Probe design

The resonator probes are microstrip lines based on those used in the 3.8GHz DRO developed at by this research group [33]. This allows the length of the probes to be varied to modify the coupling ratio to the 6dB optimum. Figure 3.4 shows the CST model used in the design process, including a tuning screw in the lid of the enclosure that can be used for fine tuning the resonant frequency. This figure shows the modified resonator with probes and gaps in the wall used in later frequency domain simulations

The probes are microstrip line that enter the enclosure at the bottom of the cylindrical walls

through an aperture and curve around $\frac{1}{4}$ of the dielectric puck as demonstrated in Figure 3.4 and have characteristic impedance of 50Ω.

The width of 50Ω microstrip when using the i-Tera substrate [40] is 1.18 mm, this track width is used on all subsequent 50Ω microstrip lines. The height of the enclosure was 90 mm and the radius was 70 mm. The dimensions for the puck did not change. The frequency domain solver is preferred at this stage because the model in the simulation includes the two ports, ensuring the correct mode is coupling to the ports and therefore coupling to the resonator via the probes as well as considering the losses due to the probes and enclosure. It is better suited to simulating models with high Qs than the time domain solver as simulation time is reduced.

The distance between the probes and the centre of the puck was optimised for 5dB insertion loss. This is so that manufacturing tolerances and inaccuracies in the materials used in the CST model can be mitigated and the insertion loss does not exceed 6dB. The simulated insertion loss decreases as the probe radius increases and the probes will be oversized. The ends can, therefore, be trimmed to increase the insertion loss to the desired optimum of 6dB.

A series of simulations varying the radius of the arced microstrip lines were performed to increase the distance the probes are from the centre of the puck where the magnetic field is strongest. Table 3.5 shows the simulated values for resonant frequency, insertion loss, Q_L and calculated Q_0.

From these simulations the general trend is that with increasing probe radius, insertion loss and Q_l increase. There is a slight increase in Q_0 to 34,000 as result of the increasing probe radius from 20mm to 35mm. Increasing the probe radius is 40 mm increases the Q_0 to 40,000 however further increasing

Probe radius /mm	f_0 / GHz	S_{21}	Q_L	Q_0
20	1.51	-4.85	13800	32300
25	1.51	-4.33	13000	33000
30	1.51	-5.42	15000	33300
35	1.51	-8.30	20900	34000
40	1.51	-14.5	32513	40000
45	1.51	-27.4	31800	33200

Table 3.5: Resonant frequency and insertion loss, Q_L and Q_0 at the resonant frequency with varying probe radius.

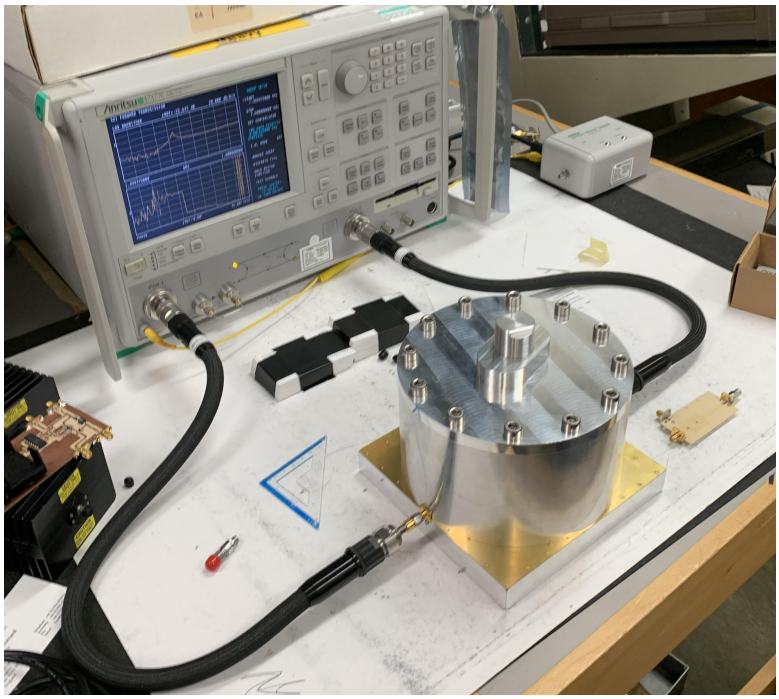


Figure 3.5: Resonator Measurement using Anritsu 37377C Vector Network Analyser.

the probe radius to 45mm causes the Q_0 to reduce to a back to 33,200. The variation in resonant frequency is less than 1% across the range of probe radii in this simulation. In the manufactured PCB for the DR, the probe radius was 27.5 mm as the previous simulations suggest that an insertion loss of 5dB can be achieved by setting the probe radius between 25mm and 30mm, as these radii gave a simulated insertion loss of 4.33dB and 5.42dB respectively .

Manufactured resonator measurements

An enclosure with a radius of 80mm was not manufactured as the simulation showed a small increase Q_0 when compared to the simulation where the enclosure radius was 70mm. It was decided that it was unreasonable to manufacture a larger enclosure, increasing the weight and size of the resonator, for such little improvement in Q. The enclosure with 40 mm radius was also not manufactured as the simulated Q_0 was much lower than the enclosures with a 50mm, 60mm or 70mm radius and the additional cost to manufacture an enclosure with 40mm radius was deemed unnecessary.

The resonator section was measured on a test jig using the Anritsu 37377C Vector Network Anal-

Enclosure radius /mm	f_0 / GHz	S_{21} /dB	Q_L	Q_0
50	1.512	-5.88	19460	39565
60	1.495	-4.424	16380	41685
70	1.487	-3.88	15048	41685
70 (trimmed probes)	1.487	-6.42	24369	46628

Table 3.6: Measured resonant frequency and S_{21}, Q_L and Q_0 at the resonant frequency.

yser to obtain S-Parameters. Figure 3.5 shows a photograph of the measurement setup and table 3.6 shows the measured resonant frequencies, insertion loss at resonance, Q_ls and calculated Q_0s of the three different sized enclosure diameters with the original printed probes as well as the trimmed probes with the largest radius enclosure of 70 mm.

The highest Q_0 is obtained when the enclosure radius is 70 mm, though the resonant frequency is lowest. Using smaller enclosures will increase the resonant frequency at the expense of the Q_0. Furthermore, the insertion loss increases when the radius decreases and the probe length stays the same. The insertion loss of -3.88dB when the enclosure radius = 70 mm is lower than the simulated value which could result in the oscillator output power increasing. The amplifiers would be driven further into saturation leading to increased flicker noise. However, this is still within the -1dB degradation limits of oscillator phase noise as result of varying insertion loss.

The probes were trimmed using a scalpel and achieved an insertion loss of -6.42dB. Q_0 also increases due to a reduction of metal material on the probes near the puck and less of the field is perturbed by the probes. A higher proportion of the power is dissipated by the resonator and the ratio of Q_L to Q_0 is closer to 1/2, therefore, increasing the Q_0 to closer to the theoretical value of 75,000 at 1.5 GHz.

3.3.2 Gain stage

As discussed in Chapter 2, the sustaining amplifier should have low flicker noise and low noise figure in order to ensure the residual phase noise introduced to the oscillator phase noise spectrum by the amplifier is kept to a minimum. Furthermore, the amplifier should produce as high output power as possible, as the power to the input of the resonator is inversely proportional to the oscillator phase noise, and must have sufficient gain to overcome the loop losses and.

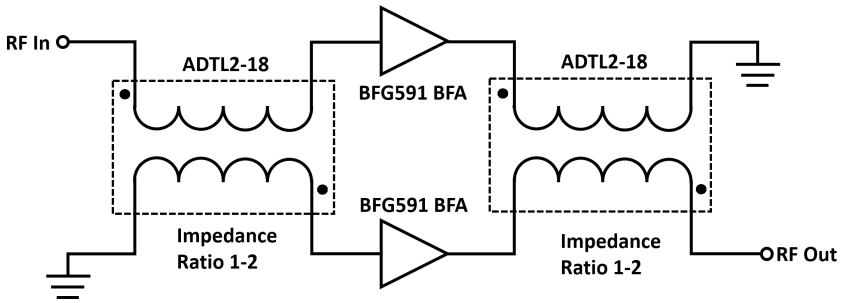


Figure 3.6: Push-pull topology of two parallel amplifiers.

BFG591 push-pull amplifier

Two transistors can be used in push-pull configuration to increase the output power whilst simultaneously reducing the flicker noise by a factor of 10LOG(2N) where N is the number of amplifiers connected in parallel [41]. The power dividing and recombining for the two stages is achieved by using an ADTL2-18+ transformer at the input and output of the amplifier in a push-pull configuration. The topology is shown in Figure 3.6. S-Parameters were obtained for the transformers and simulated using Keysight Advanced Design System, ADS. The simulation showed that each transformer contributes approximately 1dB insertion loss at 1.5 GHz and the power imbalance between the two output ports is -0.18dB.

Two BFG591 transistor amplifiers are to be used in the push-pull amplifier, the schematic of the one amplifier is shown in Figure 3.7. Each amplifier has been designed to give a gain of 8dB up to 1.6 GHz, a table of all component values is shown in table 3.6. A low frequency active bias integrated circuit, IC, the Infineon BCR400W, is used for current stabilisation with R_{ext} setting the collector current to 90mA. The value of R_{ext} is obtained from the IC's datasheet. Dominant pole, low frequency, compensation is applied using C_5 (1µF).

R_F provides negative feedback to set the gain to 8dB using 3.11. A full derivation of 3.11 is presented in [17] where it is also shown that the feedback resistor sets the input and output impedance of the amplifier. Assuming the source and load impedance are equal to an impedance Z_0, then:

$$R_F = Z_0(1 + S_{21}) = 50(1 + 6.3) = 176\Omega \tag{3.11}$$

A resistor value of 180Ω is the closest standard component value that can be used for R_F. The emitter

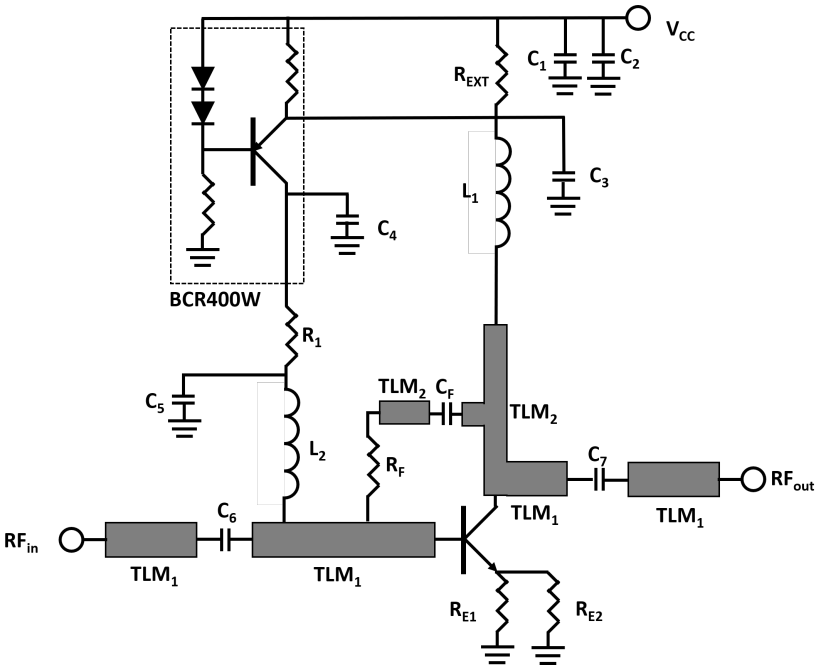


Figure 3.7: Single Stage BFG591 Amplifier schematic.

resistor can be determined from (3.12) where the emitter contact resistance, r_e, is 1.275Ω. This value of r_e is taken from the SPICE model for I_E=90mA.

$$R_E = \frac{Z_0^2}{R_F} - r_e \tag{3.12}$$

For $Z_0 = 50\Omega$, $r_e = 1.275\Omega$ and $R_F = 180\Omega$, R_E is calculated to be 12.6Ω. Two 24 Ω resistors are placed in parallel at the emitter to ground to give a total resistance of 12Ω as there are two emitter pins on the BFG591 package. C_F, C_6 & C_7 are 220pF presenting low broadband impedance and RF isolation is provided by the inductors L_1 and L_2 which are set to 22nH to present an impedance of 207jΩ at 1.5GHz. C_1 and C_4 are 1μF and C_2 is 10μF. The BCR400W datasheet specifies that $C_4 \geqslant 10 \times C_3$ to avoid oscillation. C_3 and C_5 are set to 47pF, R_1 is set to 50Ω and the transmission line, TLM_2, is a distributed inductor of equivalent inductance of approximately 10nH to compensate for the gain roll off. The characteristic impedance of transmission line TLM2 is 70Ω and the length and width of the microstrip line were found simulation using ADS.

S-Parameter simulations were run using Keysight Advanced Design System, ADS, an RF and microwave frequency design package, using the manufacturer's SPICE model for the transistor. The

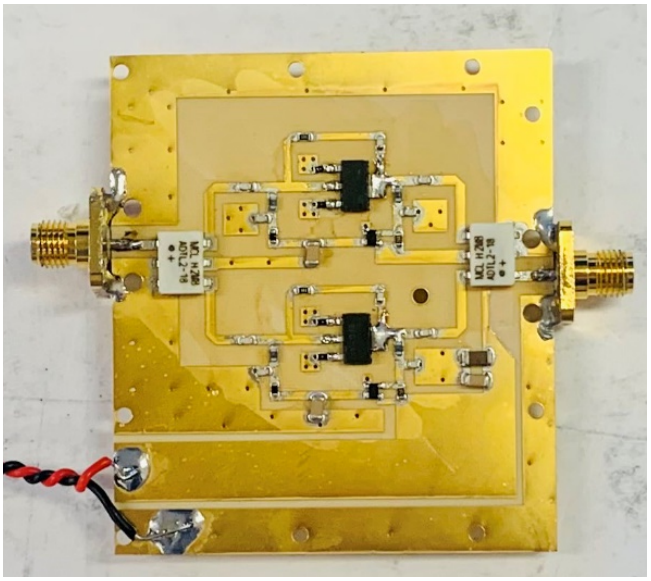


Figure 3.8: Manufactured push-pull amplifier.

simulated gain at 1.5GHz is 6.9dB for two amplifiers in push-pull configuration, each with a collector current of 90 mA and $V_{CE} = 12V$.

Manufactured amplifier measurements

The push-pull amplifier was manufactured and residual phase noise, noise figure, gain and 1dB compression point were all measured. S-Parameters were obtained using the Anritsu Network Analyser. As there will be two amplifiers in the final oscillator, two were manufactured and measured. The manufactured amplifier is shown in Figure 3.8 and Figure 3.9 shows the simulated and measured insertion and return loss of the parallel amplifier. There is good agreement between the simulated and measured gain of of the amplifier up to 0.8 GHz before the simulated gain begins to roll off. The measured gain stays reasonably flat at around 7dB from 0.5 GHz-1.3 GHz with the 3dB point measured at approximately 1.6 GHz. At 1.5 GHz the measured gain is 5.46dB. The plots for measured and simulated return losses are similar from 0 GHz to 1.3 GHz but at 1.5 GHz the measured return loss is around 7dB less than the simulated value. There is also a null in S_{11} at the measured 3dB roll off point which is not observed in simulation. The discrepancies in both gain and return loss are thought to be due to inaccuracies in the SPICE model at higher frequencies out of the device recommended

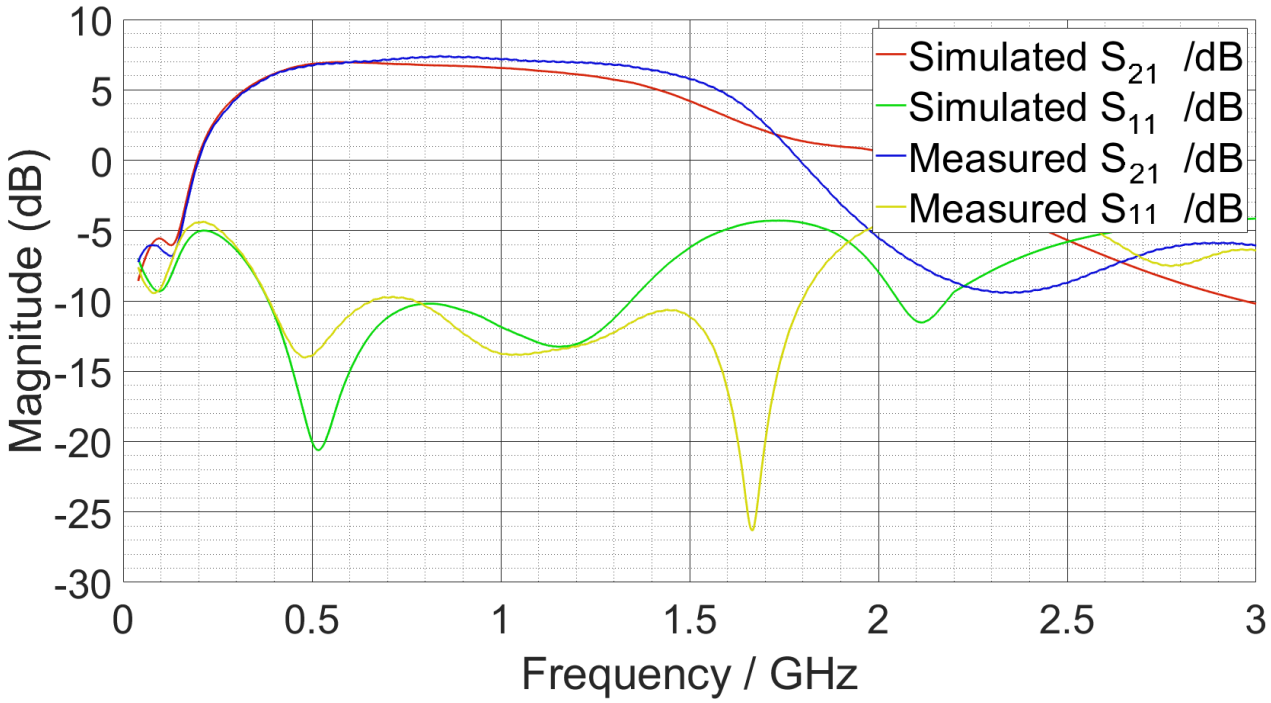
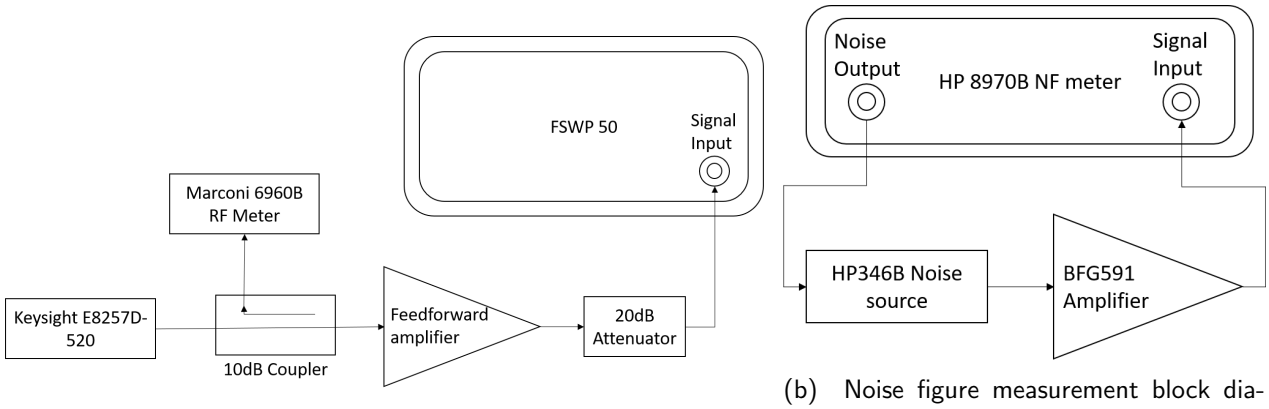


Figure 3.9: Amplifier simulated and measured gain and return loss.

frequency range.

The 1dB compression point of both amplifiers was measured using the Keysight E8257D PSG Signal Generator and the Marconi 6960B RF Power Meter. The input power from the signal generator to the amplifier was increased and the output power was measured via a 20dB attenuator. The output power was measured using the spectrum analyser function on the Rohde & Schwarz FSWP 50. The input power was measured via a 10dB coupler so that the power to the input of the Marconi power meter cannot exceed its maximum input power rating of 20dBm. Figure 3.10a is a block diagram of the measurement setup. The results were plotted against each other and the 1dB compression point was observed when the measured output power differed by 1dB from the linear increase of output power with input power. This was found to be at 25.2 and 25.4dBm output power for the two amplifiers.

The noise figure of the push-pull amplifiers have been measured using the HP 8970B noise figure meter and 3460B noise source. The noise source was connected to the amplifier input and the output of the amplifier was connected to the HP 8970B. This meter can measure noise figure directly at 1.5 GHz without the need for mixing the amplifier output signal down to a frequency within the meter's



(a) P1dB block diagram.

(b) Noise figure measurement block diagram.

Figure 3.10: Block diagrams of the P1dB and noise figure measurement setup.

usable range. A block diagram of the measurement setup is shown in Figure 3.10b and the noise figure obtained from these measurements is 8.24 and 8.37dB for the two amplifiers. This is the noise figure in the linear regime, further measurements are required to measure the noise figure when the amplifier is in saturation, the condition the amplifier would be under in the oscillator. The noise figure can then be determined from the residual phase noise measurement of the device.

Initial residual phase noise measurement of both amplifiers were made using the Rohde & Schwarz FWSP 50 phase noise measurement system, however the maximum input power that can be generated by the system is 13dBm, which is not be high enough to drive the amplifiers into saturation. Furthermore, it was found that the noise floor of the measurement system was higher than the noise floor of the DUT and therefore flicker noise corner and noise figure cannot be calculated. Using the cross correlation method outlined in Chapter 2 a residual phase noise measurement was made with a higher input power that to the amplifier of 20dBm, which is estimated to be the input power to the amplifier in the final oscillator.

From this measurement a more accurate noise figure can be calculated using (3.13)

$$\mathrm{NF} = -177\mathrm{dBm} + \mathrm{P_{MIX}} - \mathrm{PN} + \mathrm{G} \tag{3.13}$$

Where NF is noise figure, -177dBm is the phase noise contribution to thermal noise in dBm, $\mathrm{P_{MIX}}$ is the power at the mixer input and PN is the measured phase noise at 100 kHz offset from the carrier. The estimated noise figure of the amplifier in saturation is 10.7dB. Measurements of both amplifiers is

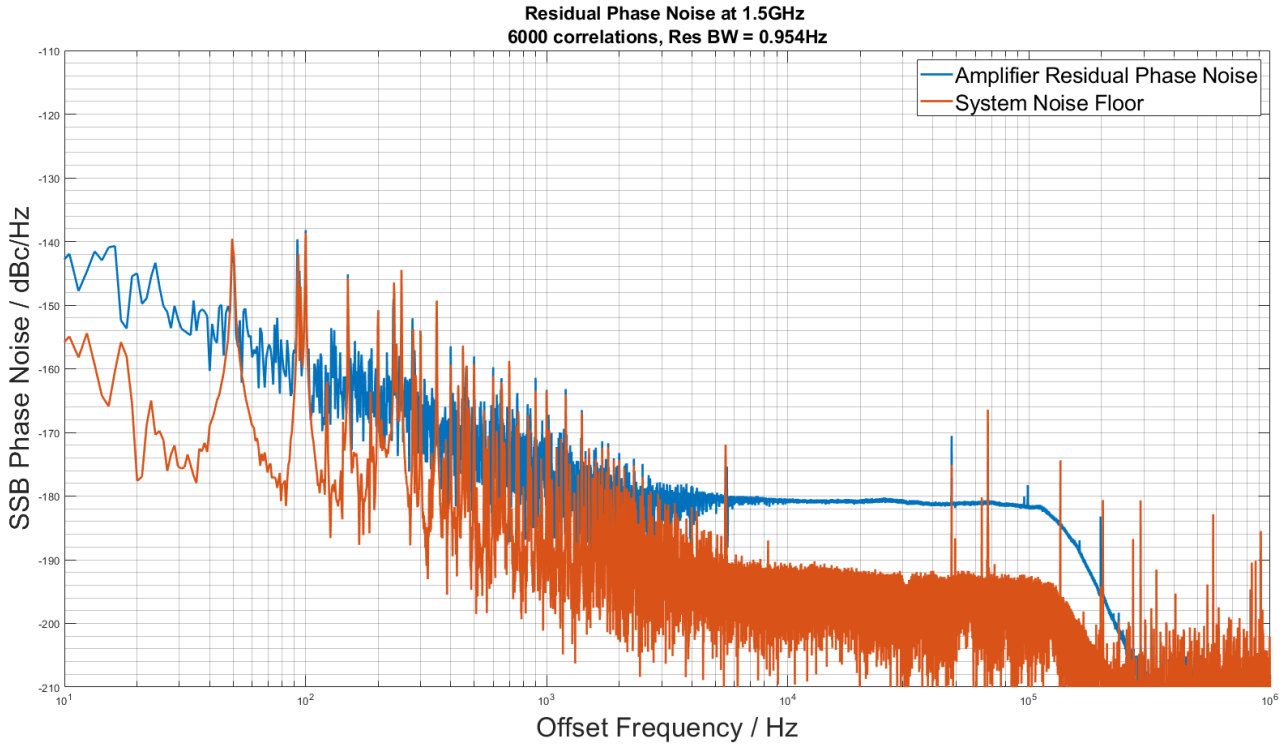


Figure 3.11: Amplifier Residual Phase Noise Measurement, $P_{in} = 20$dBm.

Parameter	Amp 1	Amp 2
Gain /dB	5.39	5.6
Linear Noise Figure /dB	8.24	8.37
Saturated Noise Figure /dB	11.6	11.6
P_{1dB} Compression /dBm	25.4	25.2

Table 3.7: BFG591 gain, noise figure and 1dB compression point measurements.

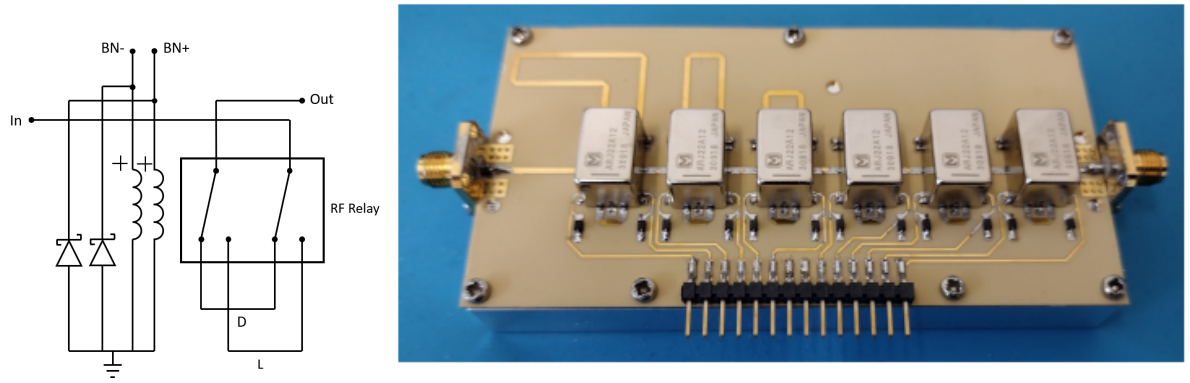
shown in table 3.7. Both amplifiers exhibit almost identical values for the four measured parameters with the largest difference of 0.21dB shown in the gain.

3.3.3 Closed loop phase shift and tuning

As discussed in Chapter 2, the phase of the oscillator loop must be an integer multiple of 360° to sustain oscillation. Furthermore, for optimum oscillator phase noise the loop phase error must be as close to 0 as possible. It is, therefore, necessary to include a phase tuning element to achieve this. By adjusting the phase within the loop the oscillator frequency can be varied. In this section two designs are presented to allow for tuning across the full 360° range. A digital phase shifter with a tuning range of 378° and a resolution of 6° is implemented to achieve coarse phase shift tuning and a voltage controlled phase shifter with a tuning range of 55° that allows for finer phase adjustments to be made due to the analog voltage used to control the phase shift.

Digital phase shifter

A 6 bit phase shifter, that can provide 378° of variable phase shift in 6° increments has been designed by fellow PhD student, Luke Dummott. The circuit uses a dual coil latching relay to change the path of the propagating signal between two microstrip lines, one small line that is a 'bypass' and one equal to the electrical length of the bypass line plus the electrical length of the desired phase shift. The schematic for the 1 bit phase shifter is shown in Figure 3.12a. Six of these sections connected in series with each section able to introduce $5.625°, 11.25°, 22.5°, 45°, 90°$ and 180° of delay, an image of the assembled digital phase shifter is shown in 3.12b. The relay used in this circuit is the Panasonic ARJ22A12 [42] and can be switched by applying 12V to 'BN+' to switch in the longer length of transmission line, or to 'BN-' to switch in the constant length of transmission line. When 12V is



(a) 1 Bit Phase shifter schematic.

(b) 1.5GHz phase shifter testing board, the PCB was bolted to a metal plate.

Figure 3.12: 1 bit digital phase shifter schematic and the assembled 6 bit digital phase shifter.

applied to the 'BN+' pin, the circuit is deemed to be in a '1' state and '0' when 12V is applied to 'BN-'.

The length of the microstrip line at the operating frequency, in mm, for each section was calculated using (3.14). In this equation c is the speed of light in a vacuum, ε_{eff} is the effective dielectric constant of the microstrip lines, N is the total number of bits, n is the number of the current bit and D is the minimum length of microstrip between the relay contacts, constant for all bits. The electrical length can be used to calculate the physical length of the microstrip in mm for a given substrate.

$$L = \left(\frac{c}{\sqrt{\varepsilon_{eff}}} \frac{2^N}{2^n.180} \right) + D \tag{3.14}$$

Due to the non homogeneous nature of microstrip line, the substrate dielectric constant is not used to calculate the length of microstrip required for each section, instead, ε_{eff} is used and is approximated in 3.15 where h is the substrate thickness, w is the width of the microstrip and $\frac{w}{h} \geq 1$.

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} \frac{\varepsilon_r - 1}{2} . \frac{1}{\sqrt{1 + \frac{12h}{w}}} \tag{3.15}$$

The circuit was manufactured and the phase shift and insertion loss were measured for each digital state. The results of these measurements are plotted in Figure 3.13. The delay introduced and therefore the phase shift, by the circuit increases linearly as expected with increasing control state and the range of attainable phase shift is from –37.17° to –415.44°, a total range of 378.27°. The

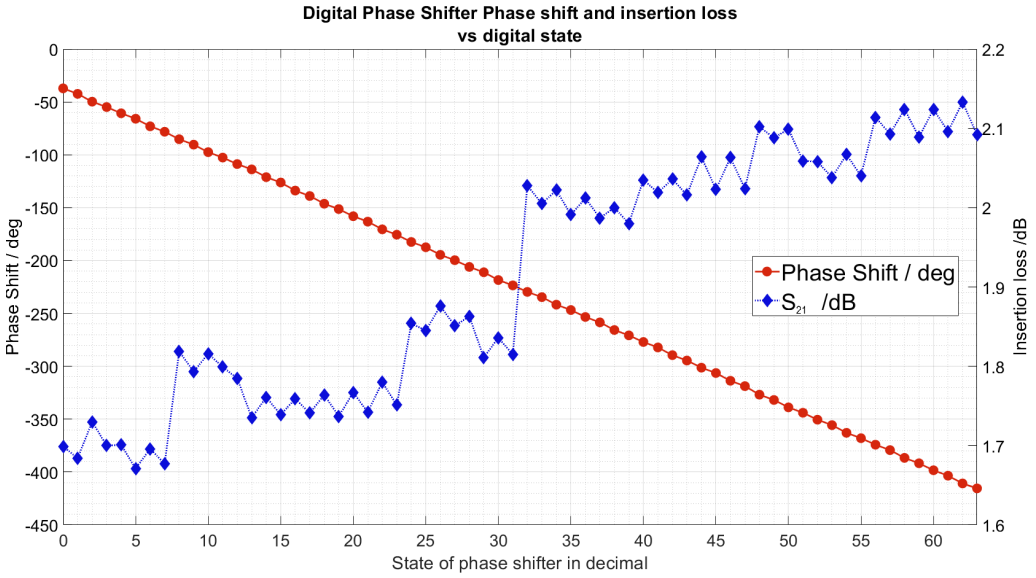


Figure 3.13: Measured phase shift and insertion loss vs decimal state of the digital phase shifter at 1.5GHz.

insertion loss varies from 1.699 to 2.133dB and the general trend shows that increasing the binary control state increases the insertion loss. As the control state is binary, however, there is variation in the insertion loss based on the actual number of relays in the 1 state and the insertion loss of the microstrip line that has been switched in. Between the 0 and 1 state the insertion loss the insertion loss decreases however for all other single bit states there is an increase in insertion loss when compared to the 0 state insertion loss.

Fine tuning electronic phase shifter

One method that has been historically used with success by this group [26, 33] is the modified high pass filter where the series capacitances are replaced with varactor tuning diodes that vary capacitance when a bias voltage is applied.

A modified 5^{th} order Butterworth high pass filter can be used to apply small phase shift to the circuit without serious degradation to the insertion loss. The capacitive elements are replaced by a parallel combination of lower value capacitors and varactor diodes where a bias voltage is applied via shunt inductor L_2 in order to vary the capacitance provided by the varactor diodes. Inductor L_2 is not shunted to ground in this configuration instead it is used as the RF choke on the DC bias line. A

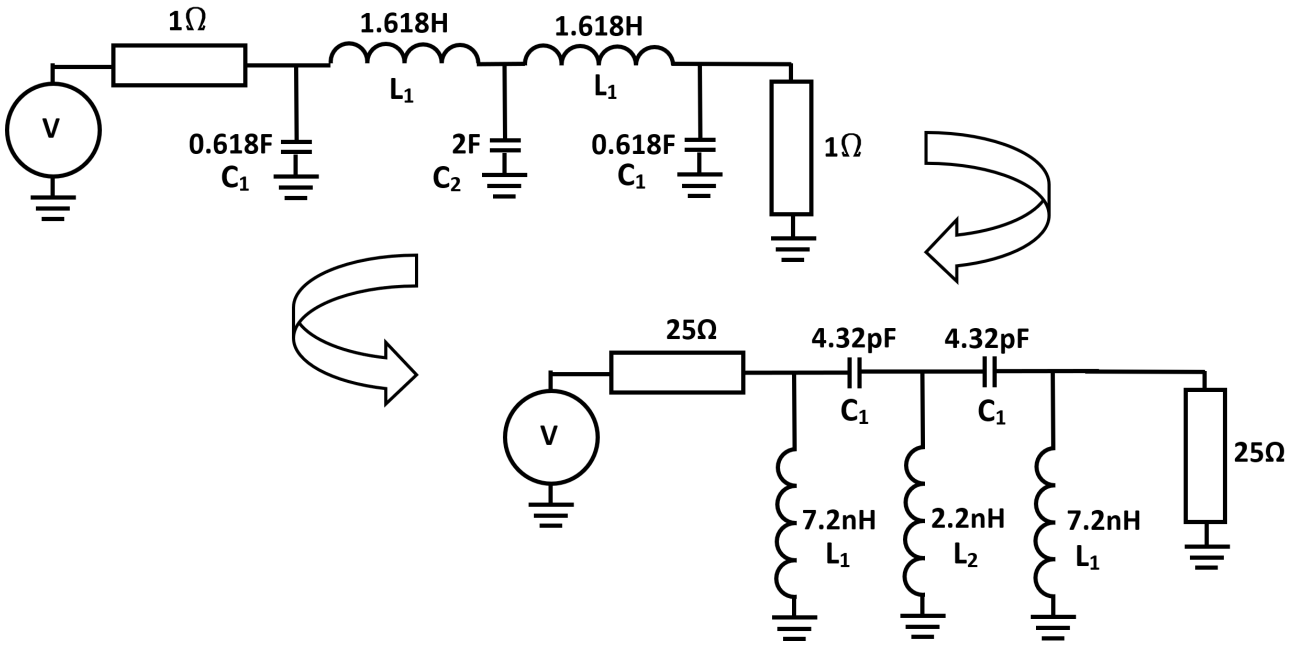
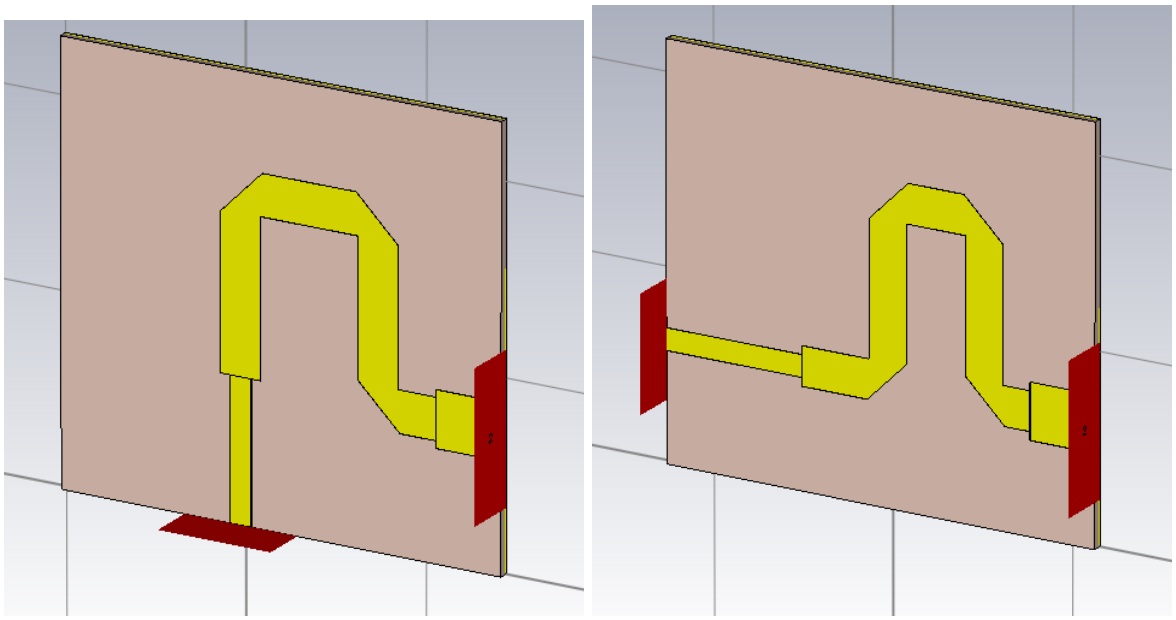


Figure 3.14: 5th Order LPF prototype transformed to a 5^{th} order HPF where f_0=0.9 GHz and $Z_0 = 25\Omega$.

fifth order prototype low pass filter is transformed to a high pass filter were $Z_0 = 25\Omega$ and $f_0 = 0.9$ GHz as shown in Figure 3.14.

The LPF prototype is transformed to a high pass prototype and the parameters were calculated for a cutoff frequency of $0.6 \times f_0$ with a terminating impedance of 25Ω, shown in Figure 3.14. The cutoff frequency is $0.6 \times f_0$ to ensure there is not significant loss in the pass band when the bias voltage for the varactor diode is varied, where f_0 is the oscillator frequency. It is necessary to denormalise to 25Ω as the component values become too small to realise with a terminating impedance of 50 Ω. Further, the impedance transformation reduces the voltage across the varactor diodes thus removing nonlinear effects that have been observed in high power, low phase noise oscillators [26].

For this transformation 2 $\lambda/4$ transformers are used to transform from 50 to 25 Ω (35.36Ω). The dimensions at 1.5 GHz were calculated using the ADS LineCalc to be 29.4 mm in length and 1.88 mm in width. This PCB would eventually be placed in an aluminium enclosure. The circuit had to fit into a corner of the enclosure so the transformers were modified to make them smaller and also to make the entire PCB include a 90° bend. This circuit was to Using the ADS Optimised Bend component the input and output sections were designed.



(a) CST Model of Input λ/4 transformer. (b) CST Model of Output λ/4 transformer.

Figure 3.15: CST models of input and output quarter wave transformer sections with 90° mitre bends.

The design was then created in CST and optimised for minimum S_{11} by varying section lengths and width for lowest insertion loss and return loss. Charge accumulation around the corner points causes an increase in the equivalent capacitance of the bend hence increasing VSWR [43] and, therefore, increasing S_{11}. It is therefore important to design mitred bends to increase the return loss in order to avoid reflections. Reflections cause variations in S_{21} that ultimately degrade the insertion loss of the transformers and would require more gain in the oscillator loop. The sections are not identical as the output section has one more mitre bend, there is slightly greater insertion loss in this section however the return loss is increased by 4dB when compared with the input section. The final CST designs were used in the phase shifter layout. Figure 3.15 shows the input and output section models used in CST.

At 1.5 GHz the simulated insertion loss of the input quarter wave transformer is -0.391dB and the return loss is -18.5dB. The simulated insertion loss of the output transformer is -0.530dB and the return loss is -22.5dB. Figure 3.16 shows the insertion and return loss of both the input and output quarter wave transformer sections across the full simulation range. These circuits are not highly resonant and therefore, the time-domain solver was used for these simulations to decrease simulation

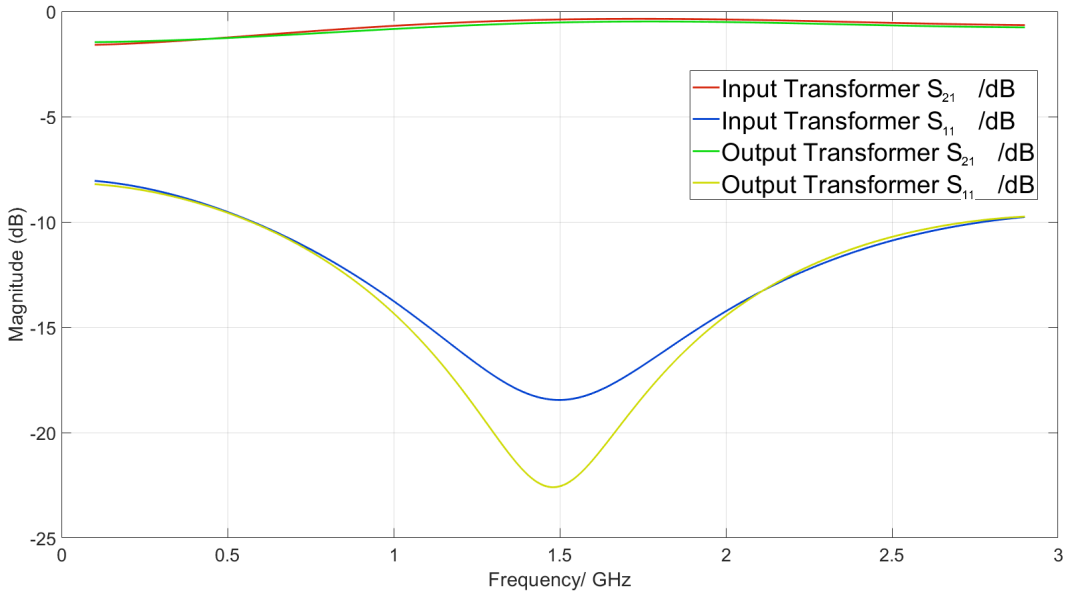
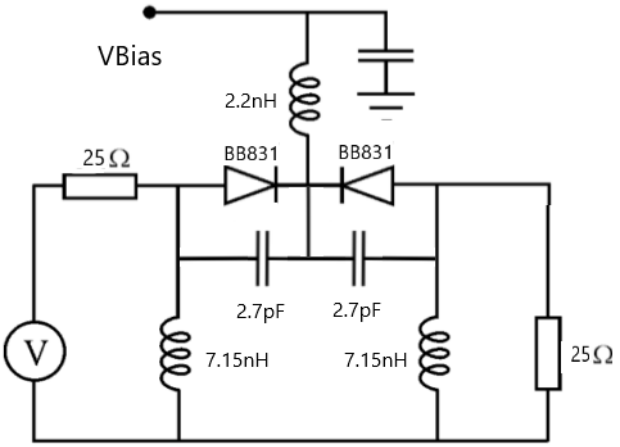


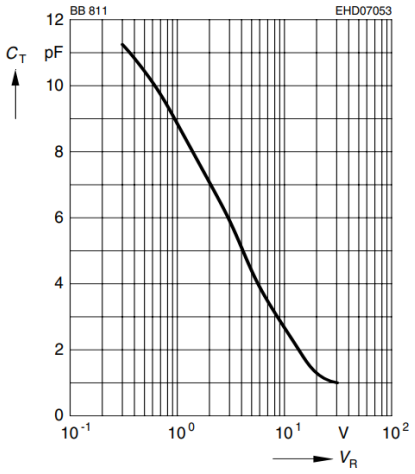
Figure 3.16: Input and output transformer S_{21} and S_{11} simulated in CST.

time when compared to the frequency domain solver.

The schematic for the fine tuning phase shifter is shown in Figure 3.17a, the inductor values have been changed to the nearest standard values available and the capacitors have been replaced by a parallel combination of BB831 varactor diodes and 2.7pF surface mount capacitors. The range of capacitance is shown in Figure 3.17b, as given by the datasheet [44]. The capacitance range is from 11pF to 1 pF with varying bias voltage 0.3V to 20V at 100 MHz, there is not a plot available for this data at 1.5 GHz. The minimum capacitance will therefore be 3.7pF when the bias voltage is 20V. The 2.7pF capacitor was chosen so that a high bias voltage had to be applied to the varactor diodes for the value of capacitance to be close to the calculated value for the HPF. The bias voltage must be kept well above the peak signal voltage to ensure the bias voltage applied to the varactor diodes does not modulate the AC signal. However, this limits the tunable range of this phase shifter. A SPICE model obtained from the manufacturer was used in the ADS simulation for the voltage controlled phase shifter, which included the microstrip equivalent of the input and output transformers. The bias voltage was varied and the simulated insertion loss and phase shift are in Figure 3.18. If an acceptable minimum insertion loss of 1dB then the range of bias voltage for this circuit is from 5-20V.



(a) Tunable Phase Shifter Schematic.



(b) BB831 capacitance vs bias voltage measured at 100 MHz [44].

Figure 3.17: 1.5 GHz tunable phase shifter schematic including BB831 varactor diode and a plot of the CV characteristics of the BB831

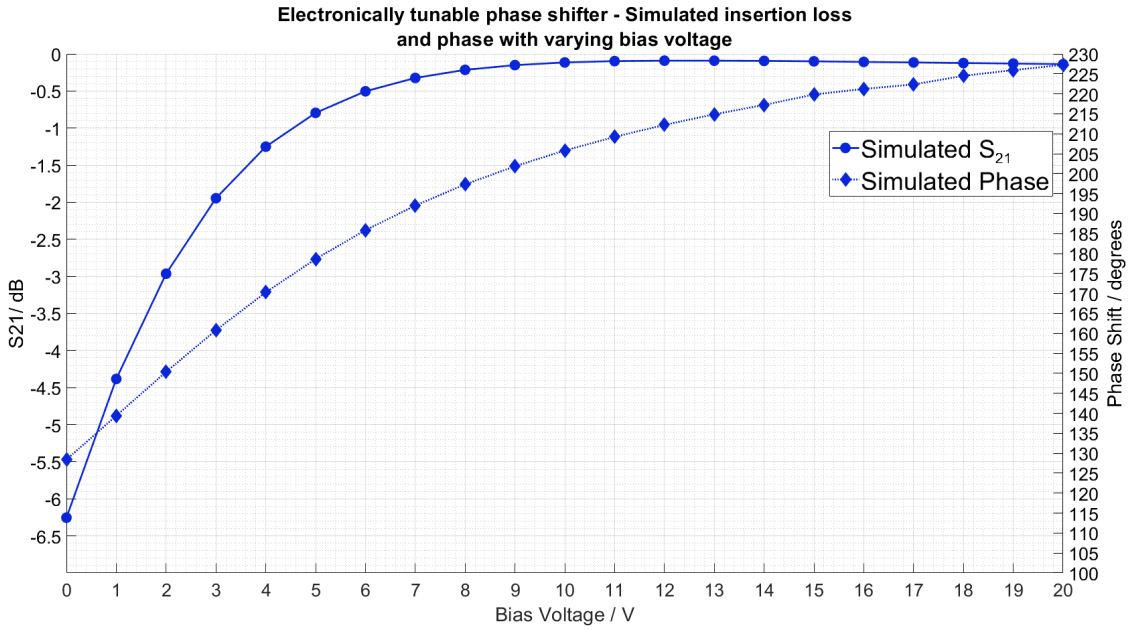


Figure 3.18: Simulated insertion loss /dB and Phase ° vs Bias Voltage /V.

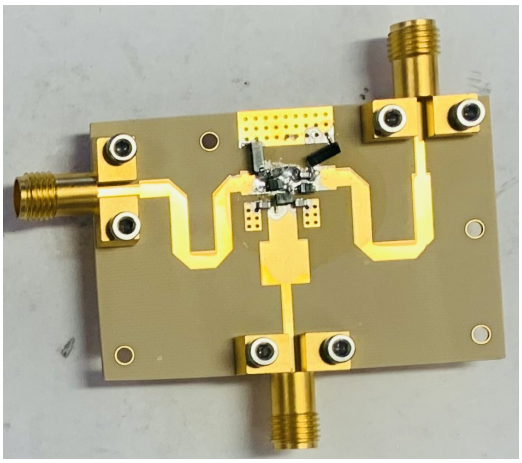


Figure 3.19: Tunable Phase Shifter board with optimised 35.4 Ω and λ/4 transformers and mitred bends.

Therefore the phase shifter would have a tuning range from 178° to 227 ° (49°). The insertion loss is fairly flat between the bias voltages of 9 and 20V where S_{21} is simulated to vary between -0.151 and -0.091dB. The tuning range is 25° between these voltages.

Electronic phase shifter measurements

The manufactured circuit is shown in Figure 3.19 and this circuit's S-Parameters were measured using the Anritsu 37377C Vector Network Analyser with varying bias voltages. Figure 3.20 shows the measured and simulated insertion loss and phase against bias voltage. If we consider an acceptable maximum insertion loss of 1dB then the tuning range is approximately 49° in simulation and 35° measured between bias voltages of 5 and 20V. The simulated model does not include the SMA connectors hence the phase shift in the measured phase shifter is offset from the simulated values. The shape of the phase plots is slightly different in simulation as the gradient of the line is greater than that of the measured value of phase.

Furthermore, the model for the passive components used in the simulation did not include parasitic components, which, unlike the model for the varactor diode, did include parasitic components. The parasitic components for the real components are unknown and is likely the cause of the smaller tuning range. The overall shape of the plot of insertion loss vs bias voltage is similar in simulation and measurement but there is generally more loss in the measured values of S_{21}. This is also thought

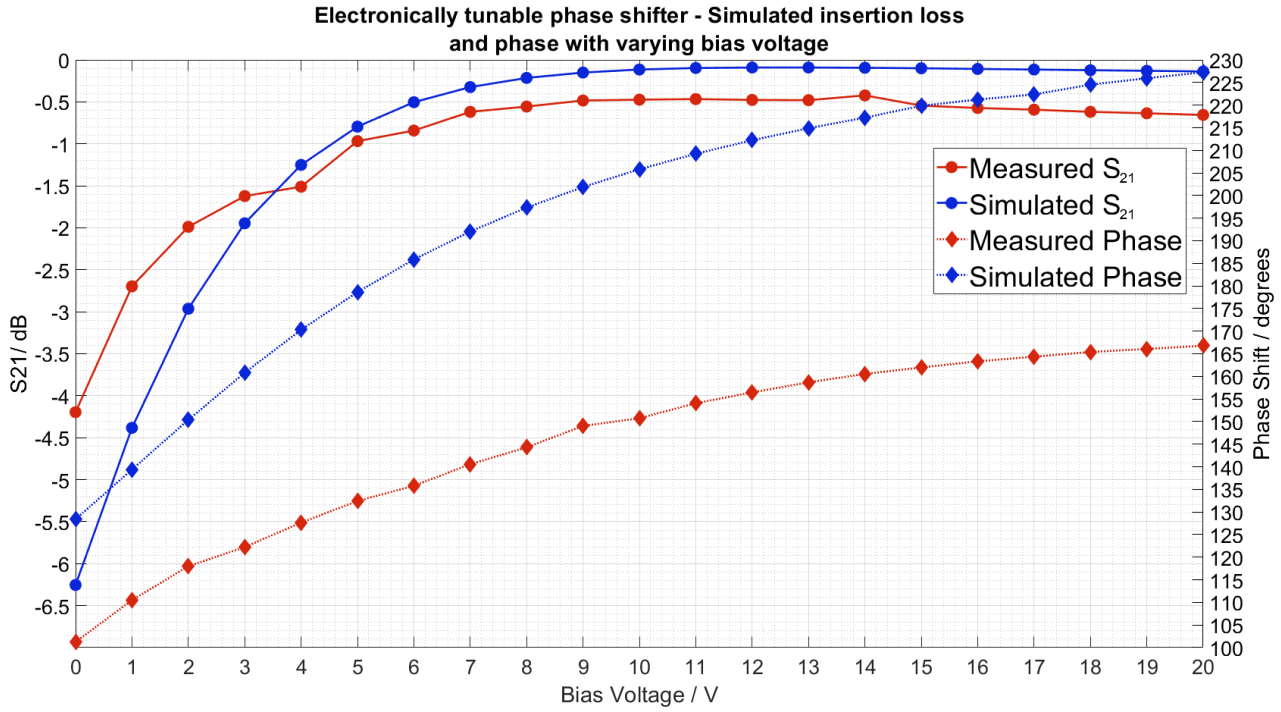


Figure 3.20: Measured insertion loss /dB and Phase ° vs Bias Voltage /V.

to be due to the addition of SMA connectors that were not modelled in ADS. Figure 3.21 is a plot of measurements of residual phase noise for both digital and fine tuning phase shifters measured using the same setup as the amplifiers except the input power to the DUTs was reduced to 18dBm for the digital phase shifter and 16.5dBm for the fine tuning resistor. Further, the signal source was from a complete 1.5 GHz DRO built as part of this research. At this stage a complete oscillator had been built and the input power to the DUTs could be calculated more accurately based on the oscillator output power of 18dBm.

The measurements show that the residual phase noise of both phase shifters is very close to the system noise floor as the traces are overlaid onto each other even after 1000 cross correlations. Increasing the number of correlations to 10,000 might make the traces smoother and reduce the system noise floor by 5dB but would increase the measurement time from 1 hour to 5 hours. Even then the system noise floor may not be below the residual phase noise of the phase shifters so the number of cross correlations was kept at 1000.

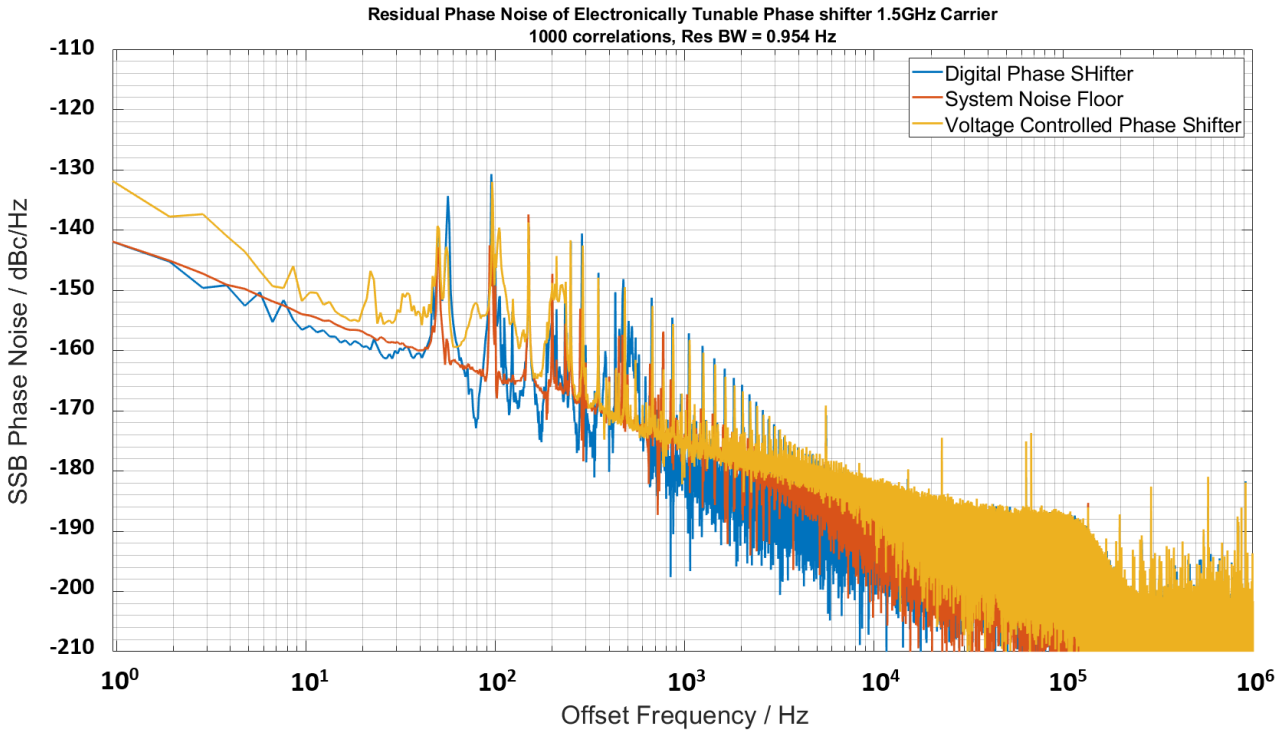


Figure 3.21: Residual phase noise of both phase shifters measured using cross correlation measurement system.

The traces do show however that the residual phase noise of the phase shifters is less than the far from carrier residual phase noise measured in the amplifier and therefore will have less of an effect on the overall oscillator phase noise than the amplifier and that the flicker noise corner of the phase shifters is less than the amplifier flicker noise corner.

3.3.4 Output Coupler

Wideband coupler design

Two amplifiers are required in the 1.5GHz DRO to overcome the loop losses. The gain of the two push-pull amplifiers operating in the linear regime is approximately 11dB. The worst case loop losses (excluding delay line losses as these are unknown at this stage) is the sum of the loss introduced by the phase shifters and the resonator. The smallest insertion loss introduced by the digital phase shifter is approximately 1.66db, the electronic tunable phase shifter introduces a minimum of approximately

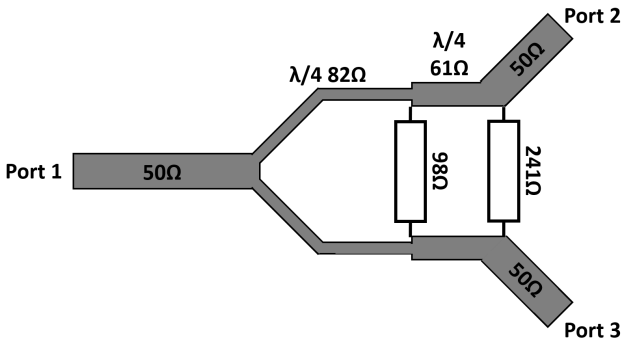


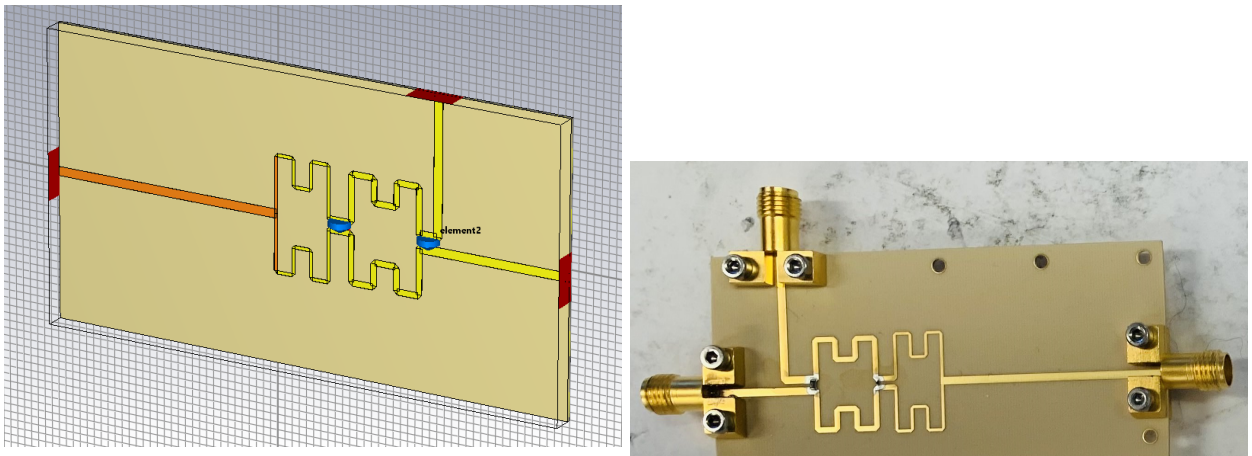
Figure 3.22: Wideband Wilkinson Divider where f_1/f_2=2.

0.42dB loss and the minimum resonator insertion loss is 3.88dB. Therefore the total minimum loop losses that are possible for the DRO are approximately 5.88dB. The excess gain is therefore 5.12dB meaning that the amplifier will enter a maximum of 5.12dB gain compression.

In order to reduce the level of saturation a wideband Wilkinson divider is used to couple the output signal and to attenuate the power at the input of the second amp by 3dB, reducing the level of saturation the amplifier enters and decrease the noise figure and the flicker noise corner of the amplifier. As the actual loop losses are unknown at this stage, there will be approximately 2.88dB excess gain after the introduction of the coupler. This allows for variation in the loop losses when the oscillator is tuned and for using different DR and enclosure of varying size, all of which will changing the level of excess gain in the oscillator loop.

Furthermore the wideband coupler allows for different dielectric pucks to be implemented into the oscillator to change the resonant frequency without increasing the loop losses. The broadband coupler design increases the isolation between both output ports [45] as well as decreasing return loss in the desired band when compared to a single stage Wilkinson divider.

A single stage Wilkinson divider uses two quarter wave transformers of characteristic impedance equal to $\sqrt{2}Z_0$ and a single resistor equal to $2 \times Z_0$ to equally split RF power between two ports where the impedance at each port is Z_0. This design is inherently narrow band as the quarter wave transformers are designed for a specific centre frequency. As the operation frequency moves away from the centre frequency the transformer is no longer $\lambda/4$ resulting in an impedance mismatch between it's input and output ports. Therefore, the input power can be reflected decreasing the return loss



(a) Optimised wideband Wilkinson divider model used in CST.

(b) Manufactured Wideband Wilkinson Divider.

Figure 3.23: CST model and manufactured wideband coupler.

of the circuit. The output port isolation is also decreased as the operating frequency moves from the centre frequency as the power propagating from port two to three through the resistor is no longer in anti phase with the power that propagates from port two to three via the two $\lambda/4$ transmission line sections as they are no longer $\lambda/4$. Therefore, the off centre frequency power that combines at port three that was incident at port two does not cancel.

The design of the broadband Wilkinson divider is presented in [45] where more than one pair of $\lambda/4$ microstrip transformers and resistors are used to increase isolation and return loss in the bandwidth.

The optimum transmission line impedances for a 2 stage, 2 way splitter where bandwidth ratio f_1/f_2 =2 are $1.22 \times Z_0$ for the first stage and $1.64 \times Z_0$ for the second stage [45]. The isolation resistors are given as $4.82 \times Z_0$ for the first isolation resistor and $1.96 \times Z_0$ for the second. Therefore, in a 50Ω system the $\lambda/4$ t_x lines have characteristic impedance of 82 Ω. A resistor of value 98Ω isolates the two transformers. The second stage of microstrip has characteristic impedance of 61Ω and is also $\lambda/4$ at the centre frequency of 1.5 GHz. Isolation is provided by a 241Ω resistor. The bandwidth is 1 GHz centred at 1.5 GHz. The design is shown in Figure 3.22.

A CST time domain solver was used to simulate the design and optimise the track lengths and widths for the required impedances and λ using the time domain solver. Initially ADS LineCalc was used to calculate the lengths and widths of microstrip before CST was used to optimise the dimensions

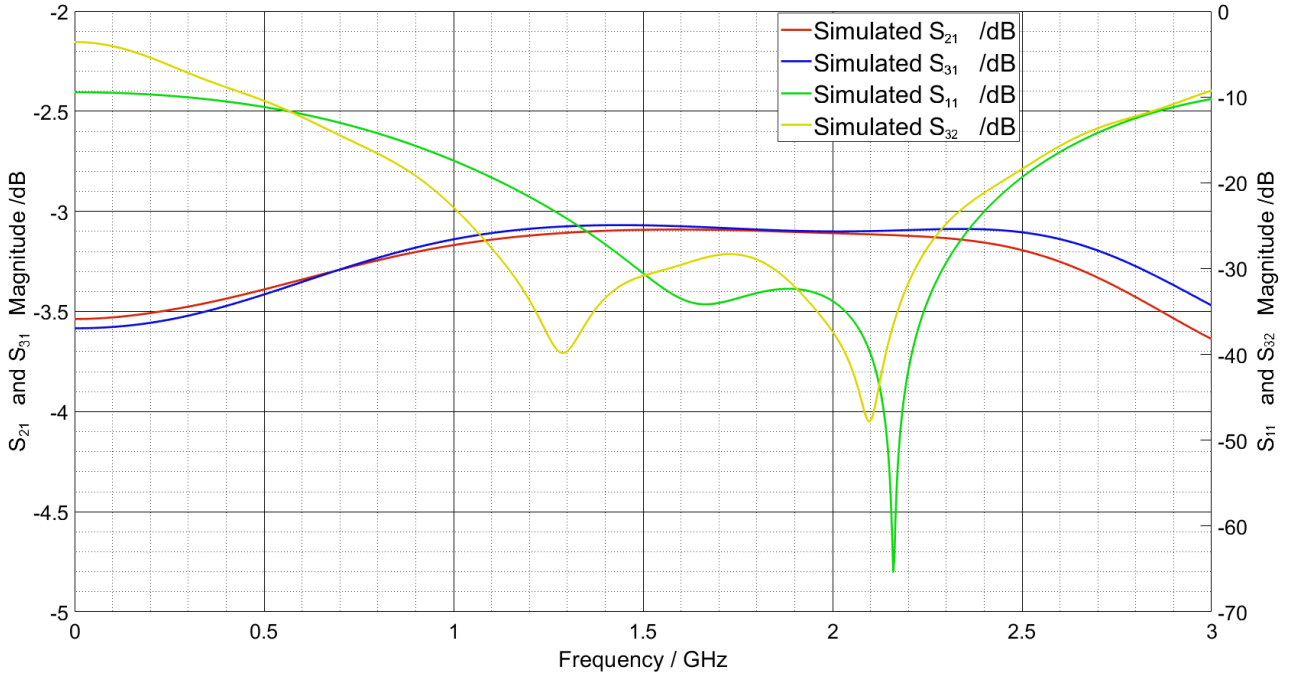


Figure 3.24: Simulated wideband coupler S-Parameters after optimisation.

and the mitre bends. An image of the model used in the CST simulations is shown in Figure 3.23a, the quarter wave microstrip sections are mitred so that the PCB are is reduced and that the lines cannot coupler to themselves. The corners are mitred to prevent charge build up and therefore reduce possible reflections. The optimised length of the 82Ω section is 29.2 mm with a width of 0.445 mm. The length of the 61Ω section after optimisation is 31 mm and the width is 0.809 mm. The simulated S-Parameters after optimisation, are plotted in Figure 3.24.

The top plane of the CST model was exported into ADS layout for manufacture with additional lengths of 50Ω microstrip added at the input and output ports to ensure the circuit will fit within the oscillator enclosure with the adjacent PCBs. The manufactured circuit is pictured in Figure 3.23b. The S Parameters of the power divider were measured using the Anritsu 37377C Vector Network Analyser (VNA), with a 50Ω termination at the other port when either output port was connected to the VNA. Figure 3.25 is a plot of the measuredS_{21} and S_{31}, output port isolation and return loss.

Table 3.8 summarises the S Parameter measurements at 1.5 GHz and the simulated values in CST.

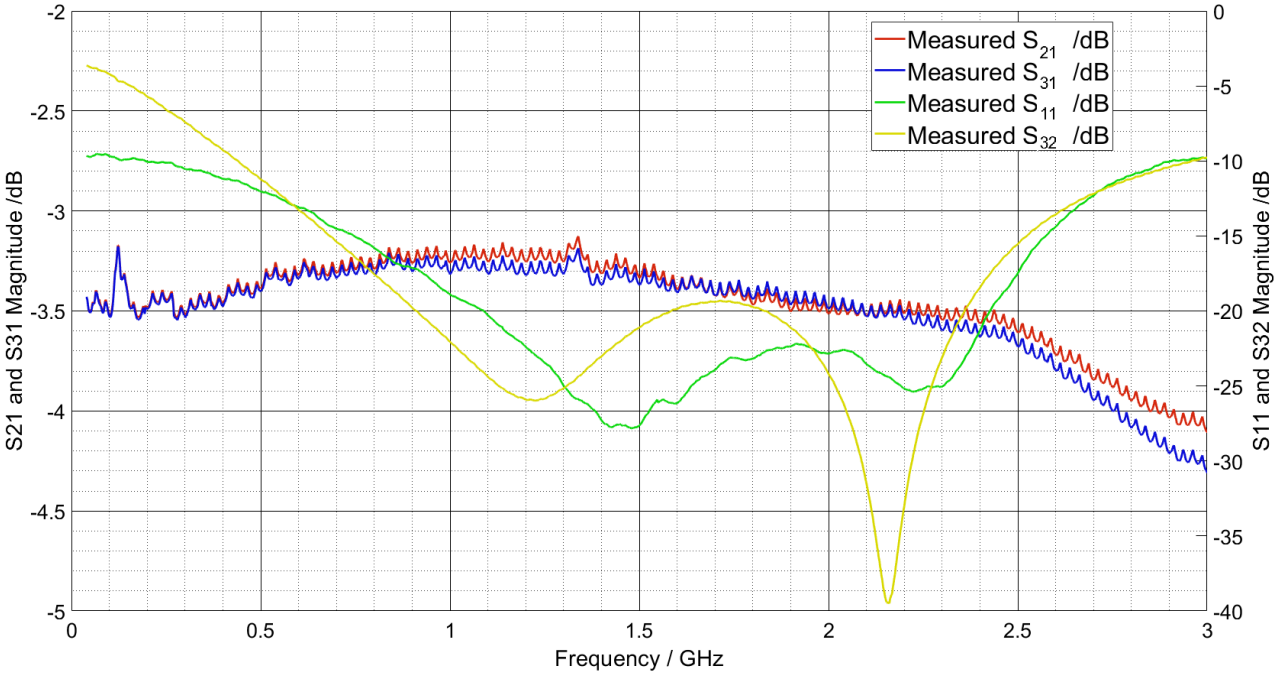


Figure 3.25: Manufactured wideband Wilkinson divider measured S-Parameter.

The port isolation, S_{32} is 7dB better in simulation, the simulation assumes the resistors between the ports are ideal whereas the real resistors are soldered onto the PCB. The resistors will have parasitic effects that could allow some breakthrough between ports hence a degradation in S32.

The insertion losses, S_{21} and S_{31} are very close to the simulated values, the slight discrepancy is thought to be due to the connectors adding in their own loss which hasn't been accounted for in simulation. The output arms introduce equal insertion loss at 1.5GHz and are 0.37dB different from the ideal value of 3dB. This is also likely to have been caused by the SMA connectors that are not accounted for in simulation. There is a small amount of ripple across the measured frequency range of amplitude 0.1dB with a ripple period of approximately 250 MHz. The network analyser calibration was remeasured which confirmed that the calibration does not introduce this ripple.

Ripple in measurements of S_{21} is introduced when there is an impedance mismatch which results in a reflection. A standing wave can form if the electrical length of the transmission line carrying the reflected signal is equal to lambda/2. The wavelength of 250MHz signal propagating on the 50Ω microstrip track is 712 mm, which means $\lambda/2$ is 356 mm. There is length of 50Ω microstrip that is this

Parameter @ 1.5 GHz	Measured /dB	Simulated /dB
S_{11}	-27.6	-38.6
S_{21}	-3.37	-3.09
S_{31}	-3.37	-3.06
S_{32}	-21.1	-28.1

Table 3.8: Summary Table of measured and simulated S-Parameters of Broadband Coupler.

large which suggests that the impedance mismatch occurs elsewhere in the measurement setup. It is thought that there is an impedance mismatch between the 50Ω coaxial cables connecting the network analyser to the PCB and the SMA connectors. Assuming that the coaxial cables do present 50Ω, then the input and output arms of the PCB are not 50 Ω, resulting in a small amount of power reflecting back from where the connectors meet the PCB and forming a standing wave, which, modulates the S_{21} measurement.

3.4 Complete oscillator phase noise measurement

The oscillator is mounted in an aluminium enclosure that provides some shielding to the circuits and reduces radiation losses. The enclosure also allows the individual PCBs to be connected together without the need for additional SMA connectors or coaxial cables. This will, therefore, reduce any potential losses between the separate stages as all microstrip lines have been designed to present 50Ω (with the exception of the electronic phase shifter) and can therefore be soldered together.

The enclosure was designed using Autodesk Inventor, computer aided design software, based on the existing PCB designs. The box is deliberately oversized which allows for additional or modified PCBs to be added. There are two ports, one for the bias voltage to the electronic tunable phase shifter and the other is the output port from the oscillator. There is a hole for a chassis mount Tusonix power line filter [46] that is used to filter low frequency noise present on the power line that could be modulated onto the phase noise spectrum of the oscillator. The lid is screwed to the main body using M5 cap screws that are spaced 20 mm apart (λ/10 in air). This is to reduce field penetration through the gap between the lid and the base parts of the enclosure. An exploded view of the metal enclosure with all parts is shown in Figure 3.26.

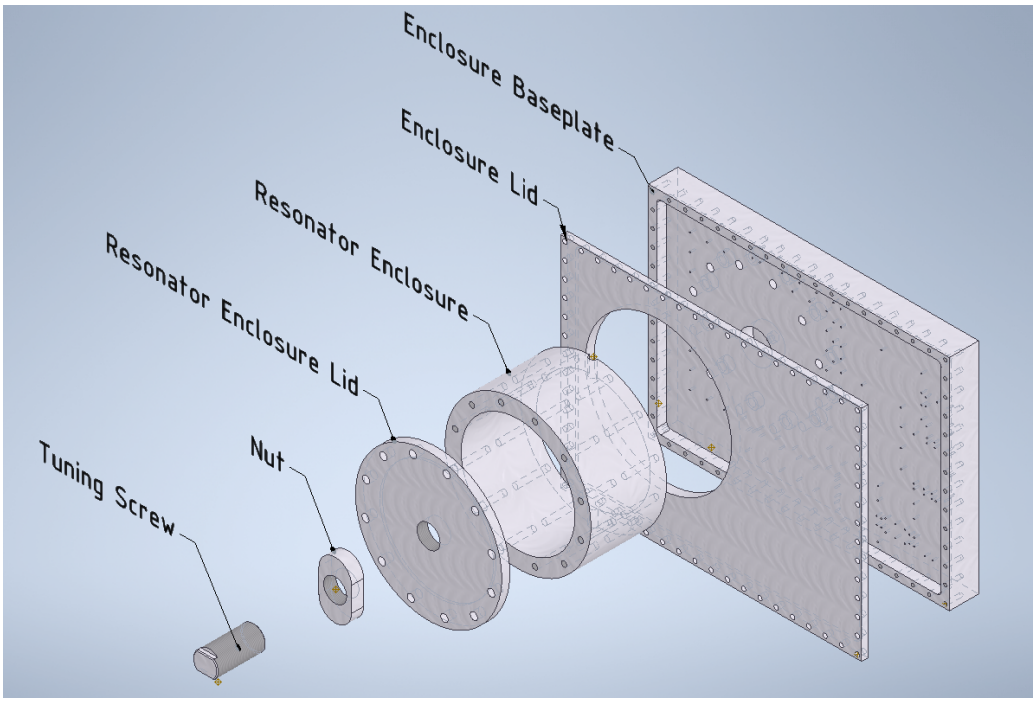


Figure 3.26: Autodesk Inventor drawing of metal enclosure.

3.4.1 Oscillator tuning and power measurements

In order to start the oscillator, it must be tuned so that the oscillator loop phase is a multiple of 360°. A 9 volt battery was used as the bias voltage source rather than a variable power supply as batteries introduce less low frequency noise into the system and as almost no current is drawn by the varactor diodes the bias voltage should not change over time. The actual voltage across the battery was 9.32V and the digital phase shifter state was changed by applying 12V to the relay pins to switch in/out the additional length of microstrip line. The oscillator output was connected to the R & S FSWP 50 spectrum analyser and the state of the digital phase shifter was varied until the maximum output power of 21.25dBm was achieved. The digital phase shifter introduced a phase shift of -163°. Once the maximum output power was achieved, the enclosure lid was secured to the base in preparation for the phase noise measurement to provide ensure good shielding to the PCBs.

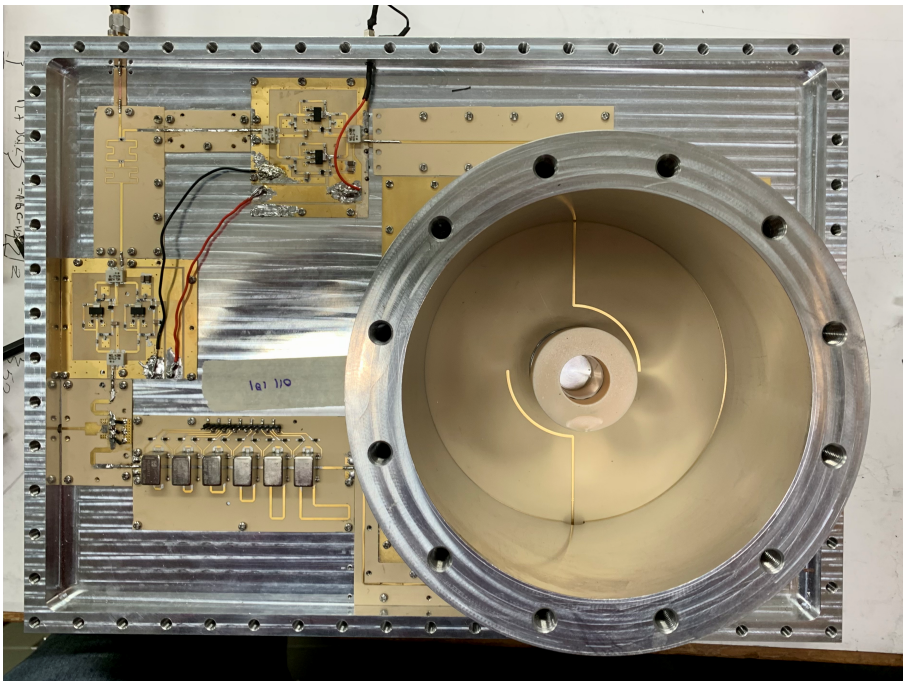


Figure 3.27: Birds Eye view of the complete oscillator with lid removed.

Parameter	Value
Q_0	41685
Q_L	15048
f_0 (operating frequency)	1.487 GHz
f_c (flicker noise corner)	5 kHz
F_1 (noise factor of components in the loop)	36.6
F_2 (noise factor of buffer amplifier)	1 (no buffer amplifier was used)
P (power available to resonator input)	0.224W
C_0 (coupling ratio between P_{AVO} and P_{OUT})	0.224

Table 3.9: Parameters used to calculated the theoretical oscillator phase noise.

Component	Noise Figure /dB	Noise Factor	Gain /dB	Gain (linear)
Digital Phase Shifter	2.00	1.58	-2	0.631
Electronic Phase Shifter	4.00	2.51	-0.800	0.832
Amplifier 1	10.7	11.7	5.8	3.80
Output Coupler	3.37	2.14	-3.37	0.468
Amplifier 2	10.7	11.7	5.25	3.33

Table 3.10: Parameters used to calculated the cascaded noise figure of components in the oscillator loop.

Frequency Offset /Hz	Phase Noise /dBc/Hz
1	-50.06
10	-80.05
100	-109.97
1000	-139.27
10000	-165.11
100000	-179.6
1000000	-180.71

Table 3.11: Theoretical oscillator phase noise at key offset frequencies.

3.4.2 Theoretical oscillator phase noise

The theoretical oscillator phase noise can be calculated using (2.59). The necessary parameters required to calculate the oscillator phase noise are shown in table 3.9. The noise factor of the components within the loop is calculated using Friis' formula for noise as these components are cascaded together. (3.16) demonstrates this formula where the subscript represents the stage number, F is is noise factor of the stage and G is the power gain of the stage. The values used in the cascaded noise factor calculation are shown in table 3.10. The order that the components are placed in the oscillator is the order that they are placed in the calculation for cascaded noise figure.

$$F_{TOTAL} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_1 - 1}{G_1 G_2} + \ldots + \frac{F_n - 1}{G_1 G_2 \ldots G_n} \tag{3.16}$$

Figure 3.28 is generated from (2.59) and the parameters from tables 3.9 and 3.10. From the measurements made of the individual modules, it is predicted that the oscillator phase noise will be

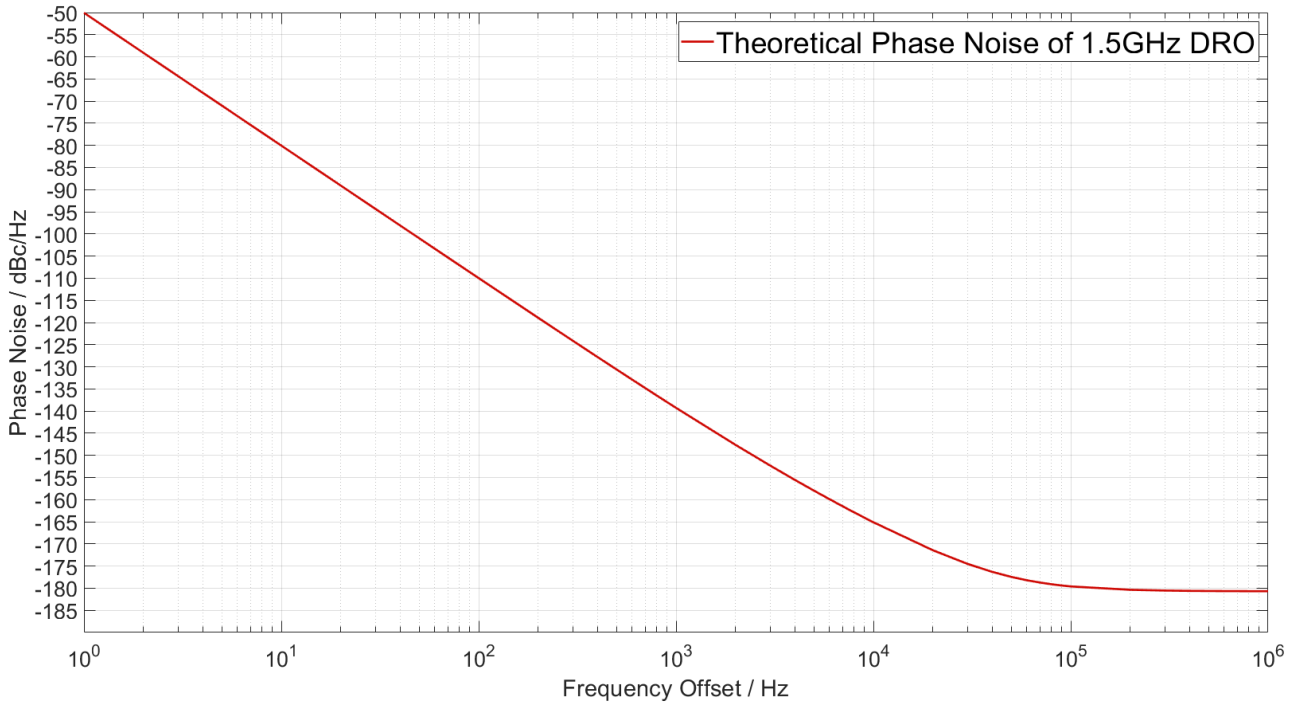


Figure 3.28: Theoretical oscillator phase noise calculated using 2.59 and the parameters from 3.9.

lower than other comparable oscillators within the literature at 10 kHz with phase noise -167dBc/Hz. The far from carrier noise floor will reach -181dBc/Hz which is state-of-the-art performance for a DRO at similar frequencies.

3.4.3 Single oscillator phase noise measurements using Rohde and Schwarz FSWP 50 phase noise measurement system

The phase noise of the first oscillator was measured using the Rohde and Schwarz FSWP 50 phase noise measurement system, R & S FSWP 50, in its phase noise mode. This mode automatically searches for a carrier signal and measures the phase noise of it. The oscillator is powered using a 12V lead acid battery rather than a power supply to reduce the noise introduced. The actual voltage supplied to the oscillator was 12.78V from the fully charged battery.

Both the 9V battery used to bias the electronic phase shifter and the 12V battery used to power the oscillator, and the oscillator (in its aluminium enclosure) were placed in a metal box to reduce interference onto the output signal and to shield the power cables from the battery to the oscillator.

The output of the oscillator was connected to a 3dB attenuator and a double shielded SMA coaxial cable inside the box that was connected to a bulkhead connector on the box wall. The other side of the bulkhead connector was then connected to another double shielded SMA cable before being connected to the FSWP 50. The 3dB attenuator was necessary to ensure the input power to the R & S FSWP 50 did not exceed 20dBm, the maximum input power to the R & S FSWP 50 without internal attenuators switching in. The internal mechanism for switching in attenuators is unclear and therefore the effect on the phase noise measurement is unknown. The 3dB attenuator is assumed to attenuate the carrier and phase noise power by 3dB and its residual phase noise power is smaller than the oscillator phase noise power and will therefore, not affect the measurement. Within the box, the oscillator was sat on partially inflated tyres to reduce the impact of vibrations on the phase noise measurement. Once the lid was secure the phase noise measurement could be made.

A resolution bandwidth (RBW) of 5% per half-decade was used, the R & S FSWP 50 splits each decade into two in order to otpimise the number of correlations per decade depending on selected RBW, 1000 correlations were made in the 1-10 Hz band. The input power measured at the R & S FSWP 50 input was 16.25dBm. Figure 3.29 is a plot containing both theoretical oscillator phase noise and the measured oscillator phase noise of the oscillator. Table 3.12 contains the both the theoretical and measured oscillator phase noise at key offset frequencies from the carrier frequency.

There is a plot of the estimated system noise floor taken from the FSWP 50 specification sheet [47]. The specification sheet does not include data for the system noise floor at 1.5GHz but does include data for the system noise floor at 1 GHz, with an input power greater than 10dBm and 1 correlation. The exact input power is unspecified so is assumed to be 10dBm, the specification also sates that for 1000 cross correlations carried out the noise floor decreases by 15dB, this has been subtracted from the data given on the sheet for the plot of the estimated noise floor. The plot shows that the noise floor at 1GHz, with 10dBm assumed input power and 1000 cross correlations, the noise floor is below the measurement. It is expected that the actual noise floor is approximately 6.25dB lower than this estimated noise floor as the measured input power to the FSWP for the oscillator measurement was 16.25dBm.

The oscillator phase noise is typically above the predicted phase noise at all offset frequencies except for at 1 MHz offset. Here the phase noise is actually 1dB lower than the theory would suggest.

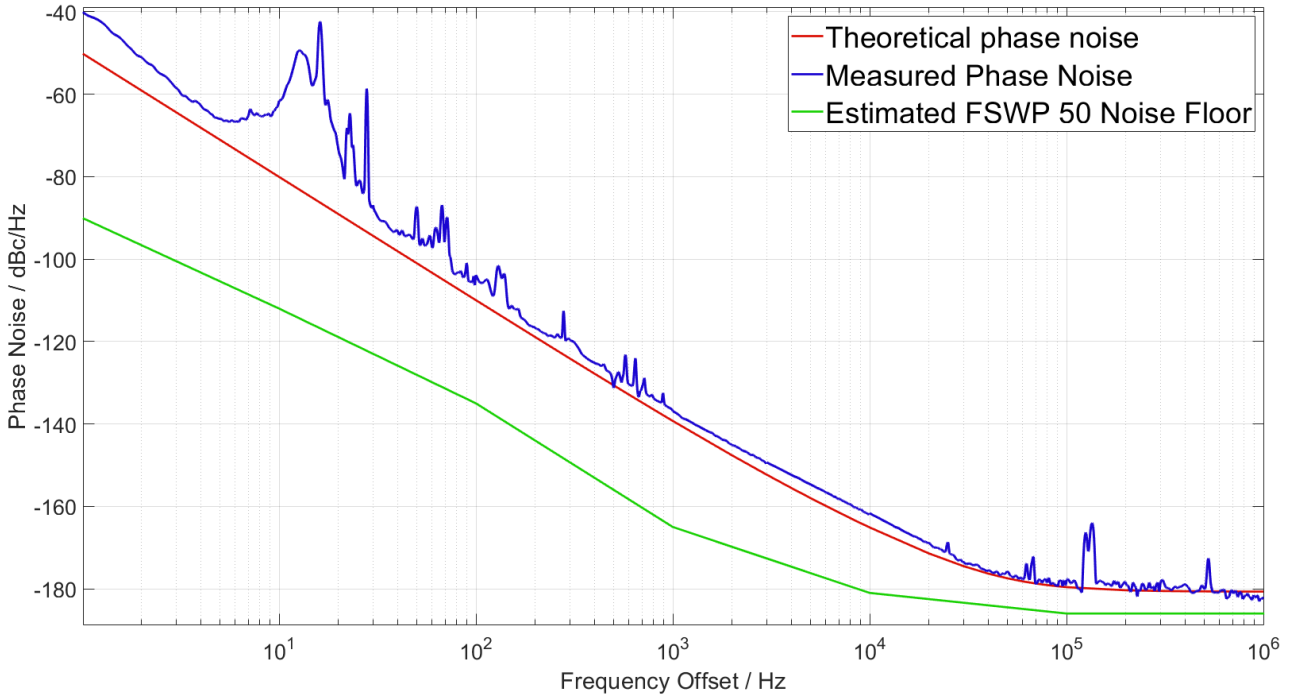


Figure 3.29: Initial Oscillator phase noise measurement with theoretical plot.

Frequency Offset /Hz	Theoretical Phase Noise /dBc/Hz	Measured Phase Noise /dBc/Hz
1	-52.54	-39.91
10	-82.63	-61.63
100	-112.52	-103.88
1000	-140.34	-136.86
10000	-166.59	-161.69
100000	-180.69	-177.87
1000000	-181.71	-182.04

Table 3.12: Theoretical and measured oscillator phase noise at key offsets.

At around 15 Hz offset the measured oscillator phase noise increases over a broad range forming a hump in the plot from 10-30 Hz. Between 1 kHz and 10 kHz offset the the trace is smooth but is still approximately 4dB greater than the theory. It was thought at first that a spurious resonance, introduced by a standing wave forming inside the aluminium enclosure, was causing the hump in the measurement so microwave absorber was affixed to the lid and walls of the enclosure. This was to avoid a standing wave forming within the enclosure, however, with this addition the close to carrier phase noise was still greater than the theoretical oscillator phase noise.

The 9V battery used for biasing the varactor diodes was replaced with three 3V button cells in series that were placed within the aluminium enclosure to remove unwanted modulation on the power line (the oscillator was re-tuned as the bias voltage applied to the varactor diodes was now 9.86V). Further attempts to remove this spurious noise were made were made by removing the voltage controlled phase shifter from the loop and replaced with an equivalent HPF that provided the same phase shift. A second attempt removing the digital phase shifter and replacing it with an empty PCB without the relays that had the various lengths soldered in to achieve the same phase shift as the digital phase shifter was made however the hump could not be removed.

Figure 3.30 shows the best oscillator phase noise measurement to date obtained through the same measurement process as described earlier except the electronic phase shifter was biased with 3 button cells within the aluminium enclosure,the microwave absorbing material was affixed to the inside wall of the enclosure and the tuning screw was adjusted for highest oscillator output power. The output power of the oscillator decreased to 18dBm once the digital phase shifter was tuned to allow oscillation to be sustained, the theoretical oscillator phase noise was recalculated to account for this.

The frequency range of the oscillator was measured by varying the bias voltage applied to the electronically tunable phase shifter, whilst keeping the digital phase shifter in a constant state. The minimum bias voltage applied to the electronically tunable phase shifter in the oscillator, and still produce an output was 5.7V. The maximum was 12.1V. Over this range of bias voltages the frequency range was 47 kHz. The output power variation as frequency variation is plotted against varying bias voltage in Figure 3.31

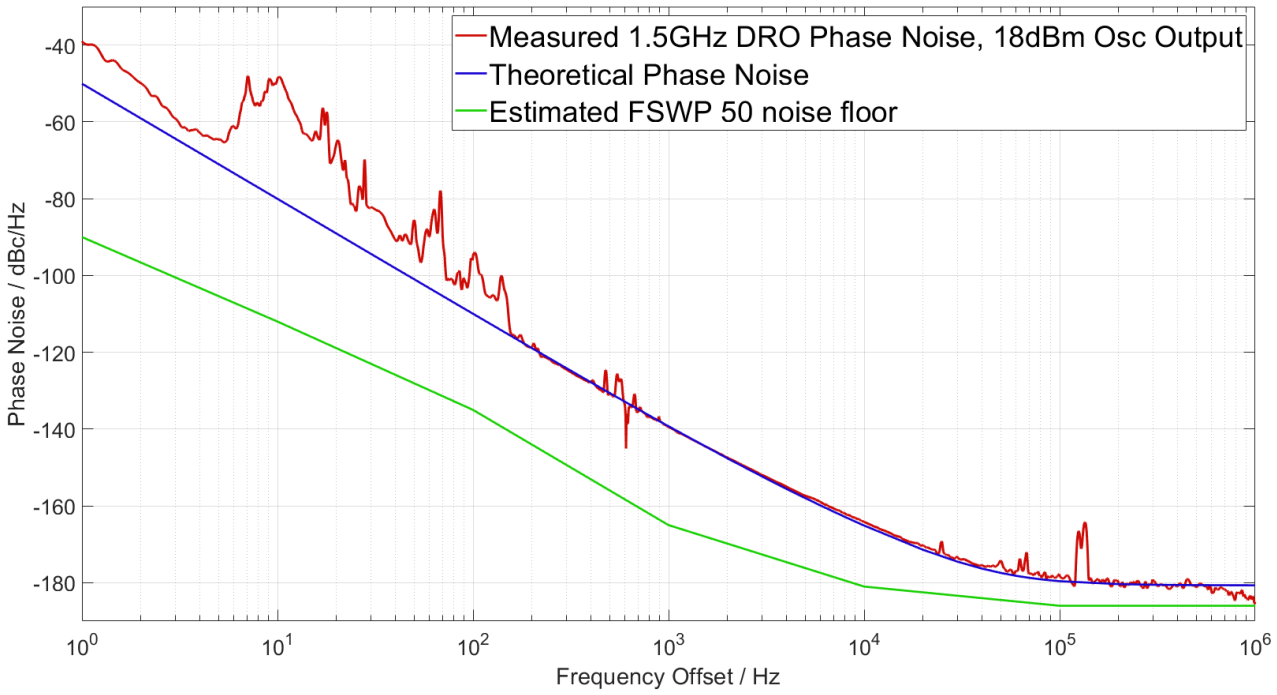


Figure 3.30: Best oscillator phase noise measurement with theoretical plot.

3.4.4 Dual oscillator phase noise measurement using Symmetricom 5120 A (Option 01)

To rule out the possibility of the R & S FSWP 50 introducing the 'hump' in the oscillator phase noise plot a second set of oscillator phase noise measurements were made using the Symmetricom 5120 A (Option 01) phase noise measurement system. This system has a maximum input frequency of 30 MHz so the oscillator frequency must therefore be mixed with another source operating less than 30 MHz away from the oscillator. The two DROs that have been manufactured were used used for this measurement and the frequency was tuned using the tuning screw such that the oscillator frequencies were different by 10 MHz. The two signals can then be mixed and the 10 MHz 'beat' signal measured. As two oscillators are contributing to the noise power the actual phase noise of one oscillator will be half (3dB) that of the measurement.

The block diagram in Figure 3.32 shows the measurement setup. The two DRO outputs are first passed through a 1.2-1.7 GHz isolator [48] to minimise any reflections or power coupled from the other oscillator propagating in the reverse direction into the DRO output. A MiniCircuits ZEM-

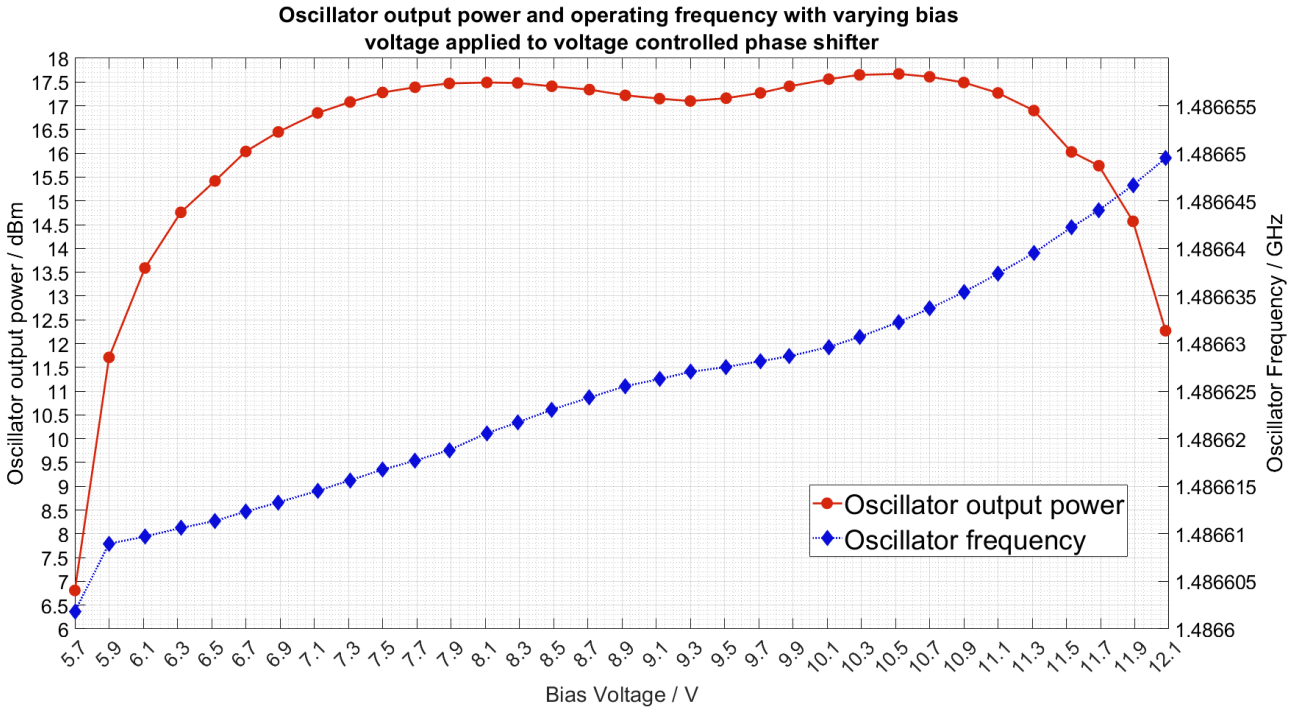


Figure 3.31: Oscillator Frequency (solid diamond) and Output power (solid dot) plotted against bias voltage applied to the electronically tunable phase shifter. No output signal from the oscillator was observed outside the bias range 5.7V-12.1V. The frequency tuning range is 47 kHz.

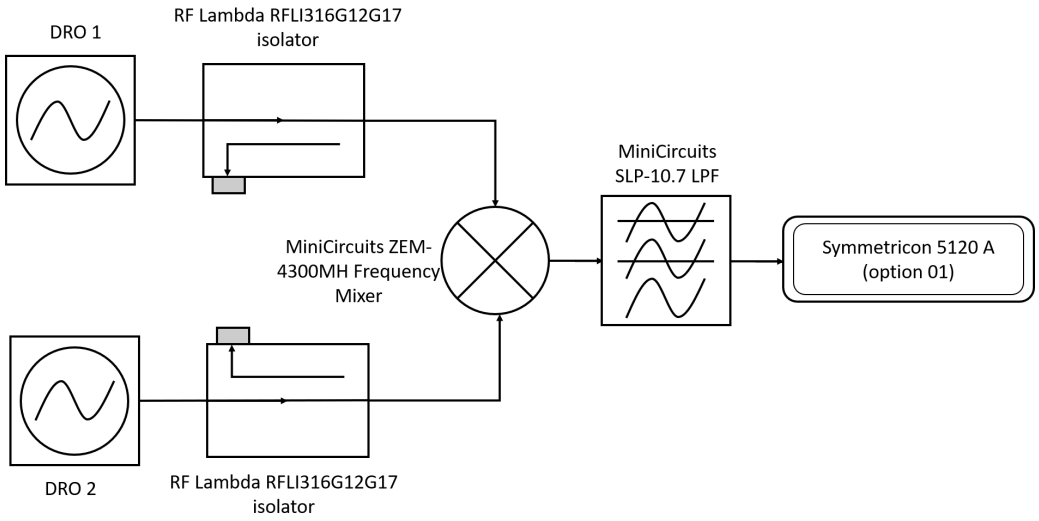


Figure 3.32: Block diagram of the measurement setup using the Symmetricom 5120 A phase noise measurement system. The phase noise of the beat signal is measured in this setup.

4300MH mixer [49] is used to mix the two DRO outputs, the output of the mixer is then passed through a MiniCircuits SLP-10.7 DC-11 MHz low pass filter (LPF) [50], that removes any higher order harmonics or other RF signal that could damage the Symmetricom instrument. The Symmetricom 5210A Option 01 phase noise measurement system is used to measure the 10 MHz signal. Multiple attempts at measurements were made however all finished abruptly with an error stating that the input frequency changed significantly. Figure 3.33 is a plot of the data collected by the Symmetricom until it terminated the measurement. The input frequency was 10 MHz and the input power was 13dBm, the plot is much smoother than previous measurements using the R & S FSWP 50 and the hump at 10 Hz offset appears to have been removed. There is however, still a small hump at 30 Hz in the oscillator phase noise measurement. The far from carrier noise is much higher but this is expected at the Symmetricom has a higher noise floor than the R & S FSWP 50, the internal measurement of the noise floor confirmed that the measurement was reaching the noise floor of the system at frequency offsets greater than approximately 20 kHz. It was concluded that the oscillator output frequency variation was the cause of the hump at around 10 Hz offset in the R & S FSWP 50 measurement as the measurement made using the Symmetricom terminated an error stating that the input frequency changed significantly, and the data captured up until that point does not appear to

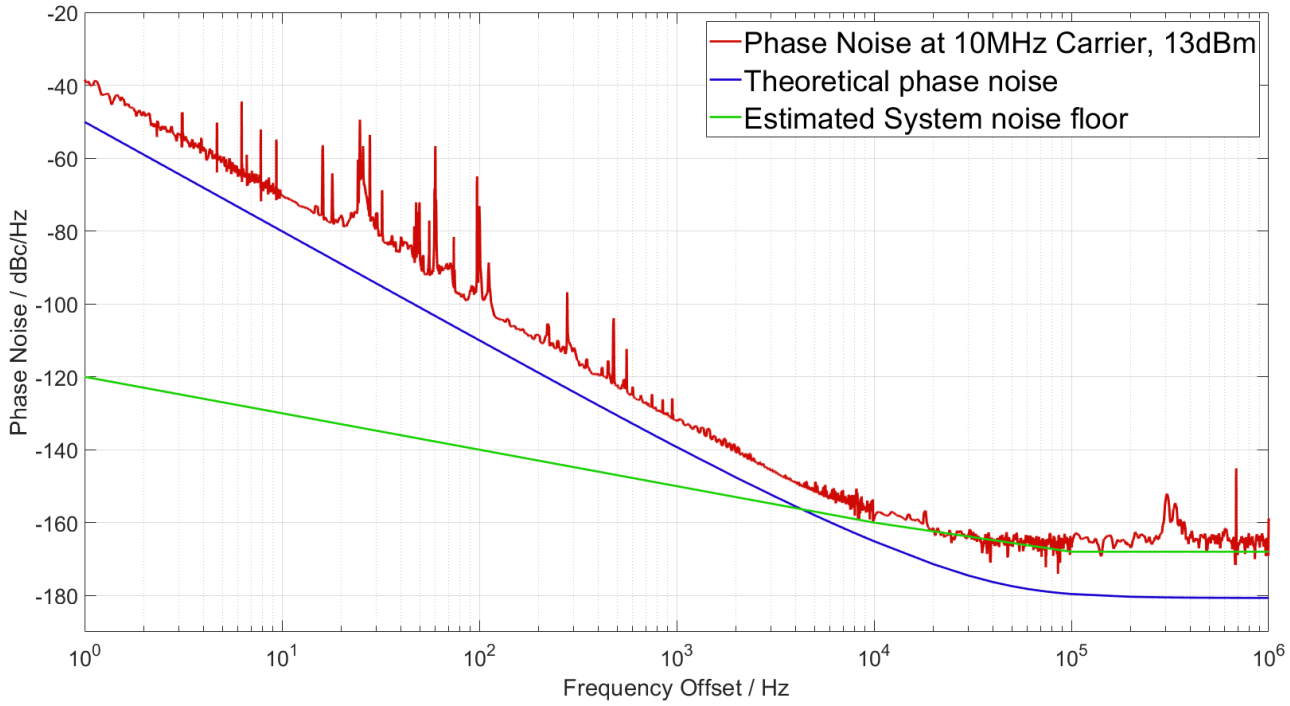


Figure 3.33: Oscillator phase noise measurement of two DROs using the Symmetricom 5210A option 01 phase noise measurement system. The measurement was terminated with an error stating the input frequency had changed significantly.

show sudden increases in phase noise at 10 Hz offset.

The DRO circuits are mounted in large aluminium enclosure, that, can act as heat sinks for the PCBs. The amplifiers generate a lot of heat as they are operating beyond their recommended frequency range and at high current in saturation. This is warming the resonator enclosure causing the resonant frequency to change and as a result, the oscillator frequency to change during the measurement. The phase noise spectrum is measured relative to the power level at the initial oscillator frequency but as the oscillation frequency changes the output power is being measured at the wrong frequency. The carrier power appears now appears at an offset frequency from the original carrier frequency .

The DRO was placed in a temperature controlled chamber and left overnight to reach a constant temperature. An initial measurement has been made at 25°C. For the measurement, the oven was turned off as the control system introduced vibrations that can degrade the phase noise. It was found that for duration of the measurement (approx. 1 hour), the temperature variation was around 0.1°C. Figure 3.34 depicts the oscillator phase noise of the DRO kept at 25°C and includes the previous measurement of the DRO oscillator phase noise at ambient temperature. The phase noise of the oscillator at far from carrier offsets ties in with the theory and the previous measurements made in this chapter, at frequency offsets 10-100 Hz, the trace does seem to be smoother than previously measured and the hump at 10-30 Hz offset has been greatly reduced. The measured oscillator phase noise at 10 Hz is -66.0dBc/Hz, this is an improvement of 5dB compared with the previous measurement. There is a sharp peak at around 8 Hz offset, it is narrower than the hump in the previous measurement and has shifted frequency to closer to the carrier.

This measurement has shown that by keeping the temperature constant, the oscillator output frequency variation has been reduced over the measurement duration. Therefore, there is a reduction in apparent increased phase noise in the measurement at small frequency offsets from the carrier. There is still some variation as the phase noise measurement is still greater than the theoretical phase noise at 10-100 Hz offset, which suggests that an optimum temperature for the oscillator has yet to be found.

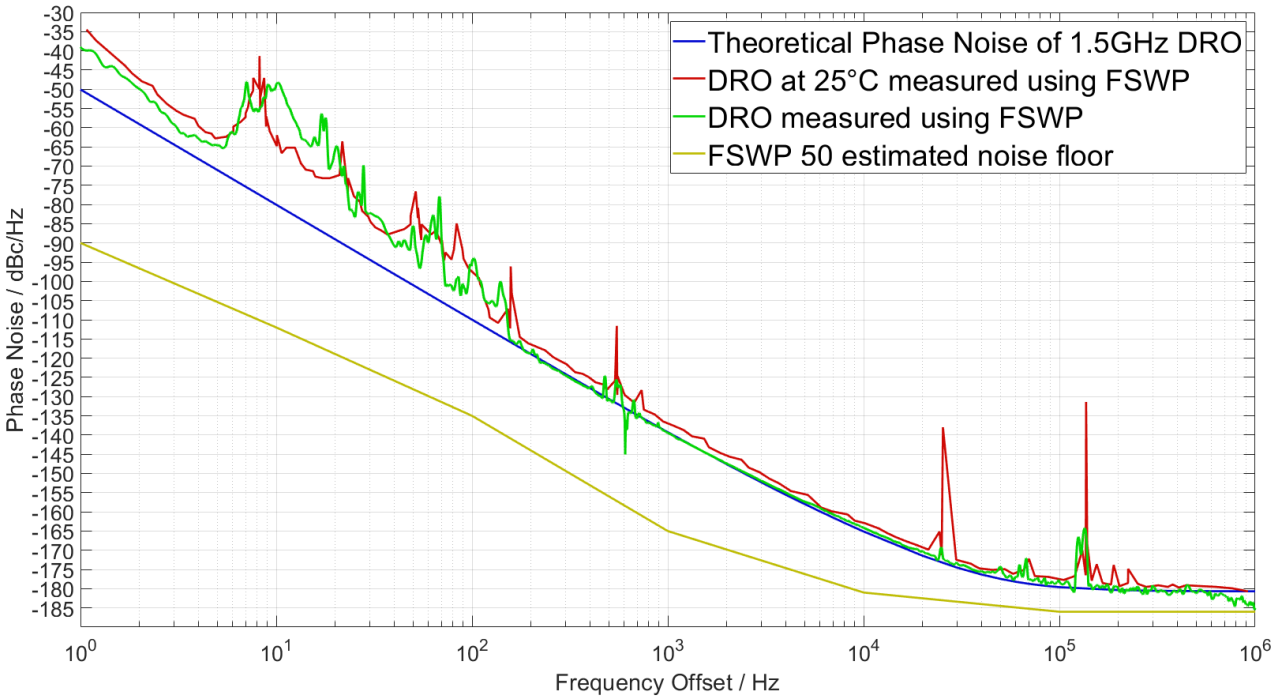


Figure 3.34: Original DRO measurement sat at ambient temperature and oscillator phase noise measurement of the DRO placed inside a temperature controlled chamber and held at 25° measurements plotted together.

3.5 Conclusions

An ultra-low phase noise oscillator operating at 1.487 GHz has been developed with state-of-the-art phase noise performance of -164.15dBc/Hz at 10 kHz offset with far from carrier noise of <-178dBc/Hz and a tuning range of ±47 kHz. The DRO is housed in an aluminium enclosure, unlike the previous version presented in [36] and the 1.25GHz DRO presented by this research group in [26].

The measured oscillator phase noise of the next closest performing oscillator in the literature, the Ingenieurbüro Gronefeld GDRO2856 [38], at 10kHz offset from a 2.856GHz carrier is -155dBc/Hz. As oscillator phase noise is proportional is the square of the carrier frequency 2.59, scaling the frequency down to 1.5GHz would decrease the oscillator phase noise at 10kHz offset to -160.5dB. The measured phase noise at 10kHz offset is 3.65dB lower in the 1.5GHz DRO developed in this chapter even after frequency scaling showing that the DRO presented here offers state of the art phase noise performance of available DROs.

This performance improves on the -163dBc/Hz at 10kHz offset measured in the previous version of the 1.5GHz DRO developed at by this research group [25] by 1.15dB. However, the oscillator phase noise measurement at 10kHz is 5.85dB greater than the measured phase noise in the 1.25GHz oscillator previously presented by this research group [26].

The carrier frequency of the DRO presented here is greater than the 1.25GHz DRO by a factor of 1.2. As the phase noise is proportional to the square of the carrier frequency 2.59, the expected degradation to the measured phase noise is 20log(1.2)dB, approximately 1.6dB due to increasing the carrier frequency.

It is thought that additional the 4.25dB degradation in oscillator phase noise measurement is due to the smaller Q_0 of the 1.5GHz resonator and larger noise figure of the feedback components. The unloaded Q of the resonators used in the 1.25GHz oscillator was 57,600, however the unloaded Q of the 1.5GHz resonator used in the DRO presented here is 41,700.

The resonators in the DRO developed here are the same resonators used in the 1.25GHz DRO but were ground down to change their frequency, which has appeared to cause a decrease in the unloaded Q. As the resonators are manufactured from the same material the expected unloaded Q of a 1.5GHz resonator from the $Q \times f$ ratio is 50,000, which is a factor of 1.2 larger than the actual unloaded Q of

the resonators used. As the oscillator phase noise is inversely proportional to the unloaded Q squared, this has caused a degradation of approximately 1.6dB.

The noise figure of the feedback components is estimated to be 15.3dB in the 1.5 GHz DRO, 4.8dB worse than the estimated noise figure of the feedback components in the 1.25GHz DRO. This would degrade the phase noise performance by 4.8dB as the oscillator phase noise is proportional to the noise figure of the feedback components. However, the power available at to the resonator is 23.5dBm in the 1.5GHz DRO which is 2dB greater than the power available at the resonator input in the 1.25GHz DRO which decreases the oscillator phase noise of the 1.5GHz DRO by 2dB when compared to the 1.25GHz DRO as the oscillator phase noise is inversely proportional to P_{AVO}.

To summarise, the smaller Q_0 has degraded the phase noise performance by approximately 1.6dB, the increased frequency has also degraded the oscillator phase noise by approximately 1.6dB and the increased noise figure has degraded the phase noise by approximately 4.8dB. The increased power at the resonator input when compared to the 1.25 GHz DRO has improved the oscillator phase noise by 2dB, therefore the total degradation is approximately 6dB when compared to the 1.25GHz DRO. This is confirmed in the measured phase noise at 10kHz offset from the carrier of both DROs as the 1.5GHz DRO phase noise is 5.85dB worse at this offset compared to the 1.25 GHz DRO.

Therefore, to improve the oscillator phase noise performance so that it is comparable to the previous 1.25GHz DRO [26] developed by this research group, a resonator designed to operate at 1.5GHz with a high unloaded Q should be used.

Furthermore, it is suggested by the author that higher gain amplifier alternative should be explored to remove the need for two series amplifiers. This would improve the oscillator phase noise performance by firstly reducing the cascaded noise figure of the feedback loop and therefore reduce the oscillator far from carrier phase noise response. In addition this will reduce the saturation as the excess gain will be reduced therefore reducing the flicker noise corner in the oscillator phase noise.

Further measurements of the DRO at different temperatures should be made to find an optimum operating temperature such that the heating effects of the transistors are reduced and the frequency variation is not modulated onto the phase noise. Alternatively, the amplifiers could themselves be mounted in a non conductive enclosure within the metal housing to insulate the PCBs from the large metal heat sink presented by the aluminium enclosure.

Chapter 4

16 GHz Distributed Bragg Resonator Oscillator

4.1 Distributed Bragg Resonator

It is shown in (2.59), that, the phase noise of an oscillator is inversely proportional to Q_0. High Q resonators should be used to achieve ultra low oscillator phase noise. At microwave frequencies Dielectric Resonators, Microwave Cavities and whispering gallery mode resonators are commonly used as they offer high Qs and high power handling capabilities. A distributed Bragg resonator (DBR) uses low loss dielectric plates positioned within a microwave cavity to increase the Q and in this chapter the development of an ultra low phase noise oscillator operating at 16 GHz using a high Q DBR is presented.

Q_0 of a microwave cavity is limited by the surface resistivity of the metal end walls but higher Q_0 can be achieved by incorporating low loss dielectric plates into the cavity [51–56]. The plates confine the majority of the H field of the propagating waves to the centre section and away from the lossy end walls.

For rectangular and circular microwave cavity resonators, Q_0 is given by (4.1) from [57] where Q_c is the Q of the cavity with lossy conducting walls but lossless dielectric and Q_d is the Q of the cavity with perfectly conducting walls but lossy dielectric. The high Q, TE_{011}, mode in a cylindrical cavity

is at its maximum when the ratio of the cavity height and cavity radius is approximately 2 [58].

$$Q = \left(\frac{1}{Q_c} + \frac{1}{Q_d}\right)^{-1} \tag{4.1}$$

The Q of a cavity with lossy conducting walls with lossless dielectric, Q_c, is given by (4.2) where k is the wavenumber ($= \omega\sqrt{\mu\varepsilon}$), a is the cavity radius, d is the cavity height, η is the wave impedance, p'_{nm} is the extrema of Bessel functions of first kind, R_s is the surface resistivity of the wall material, β is the phase constant of the TE_{nm} mode and n is the number of standing wave pattern variations in the radial direction.

$$Q_c = \frac{(ka)^3 \eta da}{4(p'_{nm})^2 R_s} \frac{1 - \left(\frac{n}{p'_{nm}}\right)^2}{\left\{\frac{ad}{2}\left[1 + \left(\frac{\beta an}{(p'_{nm})^2}\right)^2\right] + \left(\frac{\beta a^2}{p'_{nm}}\right)^2 \left(1 - \frac{n^2}{(p'nm)^2}\right)\right\}} \tag{4.2}$$

The Q of a cavity with lossless walls and lossy dielectric is given in (4.3) where tanδ is the loss tangent of the dielectric material.

$$Q_d = \frac{1}{\tan\delta} \tag{4.3}$$

Q_0 of an air filled cavity is equal to Q_d as there are no dielectric losses and it is therefore inversely proportional to the surface resistivity of the wall material. Therefore the enclosure material limits the quality factor of the resonator.

The distributed Bragg resonator reduces this Q dependence on the wall material by placing low loss dielectric plates within the cavity to confine the EM field to the central air sections and away from the cavity walls. There is a sudden change in material permittivity between the air and dielectric sections that results in the partial reflection of the propagating EM wave.

High Q resonators have been developed using rutile (TiO_2) rings placed at the end face of Sapphire cylinders [51, 52] offering Q_0 in the order of 10^6 -10^9 but these sophisticated systems require complex cooling mechanisms to achieve high Q_0 making the resonator difficult to implement into a compact system as well as increasing the cost of manufacture and use.

Q_0s of 650,000 and 450,000 at 9 and 13.2 GHz, respectively, by Flory et al. [53, 54] have been demonstrated using a periodic sapphire resonator consisting of interpenetrating concentric rings and plates. The thickness of the plates and air sections were shown to be a quarter of the wavelength of

the guide wave in periodic arrangement in order to maximise reflections at the air/plate interface.

Breeze et al. [59] state that there is an exponential decay of the electric energy upon the field penetrating the dielectric and therefore in the the first quarter-wave section the majority of the dielectric losses have occurred. It is shown in simulation that, using an aperiodic spherical structure that distributes more electric energy from the electric field energy in the air gaps than in the dielectric plates, increases Q_0 by one order of magnitude higher than the Q observed in a periodic BBR. The structure of the aperiodic arrangement consists of hollow dielectric spheres whose thicknesses asymptotically approach the quarter wave reflectors the closer they are the the walls.

A 10 GHz aperiodic DBR was built at York by Everard et al. [55], demonstrating a Q_0 of 196 797. It was also shown in simulation that the Q_0 of the resonator does not increase any further with increasing number of plates when more than 8 plates were used, though this has not been proved experimentally. A tunable resonator was later developed based on the original 10 GHz oscillator demonstrating that within a 130 MHz tuning range, the insertion loss variance was -2.84 to -12.03dB with Q_0 varying from 43,788 to 122,550 [56]. A simplified diagram of a periodic DBR is shown in Figure 4.1.

4.1.1 ABCD parameter model

The distributed Bragg Resonator that was built as part of this research was designed by Dr Simon Bale and Professor Everard in collaboration with Keysight Technologies. The chamber is a microwave cavity with short circuit ends with an internal aperiodic arrangement of alumina dielectric plates.

Bale and Everard [55] demonstrate that the aperiodic arrangement of the dielectric plates in this resonator can be modelled as a series of waveguides using ABCD parameters. Due to the symmetry of the chamber only one half of the chamber needs to be modelled. Figure 4.2 shows how the resonator can be modelled as a series of waveguides. The ABCD parameter for each waveguide section is generated using (4.4):

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \cosh\left(\frac{\gamma l}{n}\right) & Z_0 \sinh\left(\frac{\gamma l}{n}\right) \\ \frac{1}{Z_0}\sinh\left(\frac{\gamma l}{n}\right) & Z_0 \cosh\left(\frac{\gamma l}{n}\right) \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{4.4}$$

where n is the number of the waveguide section, γ is the complex propagation constant and l is the

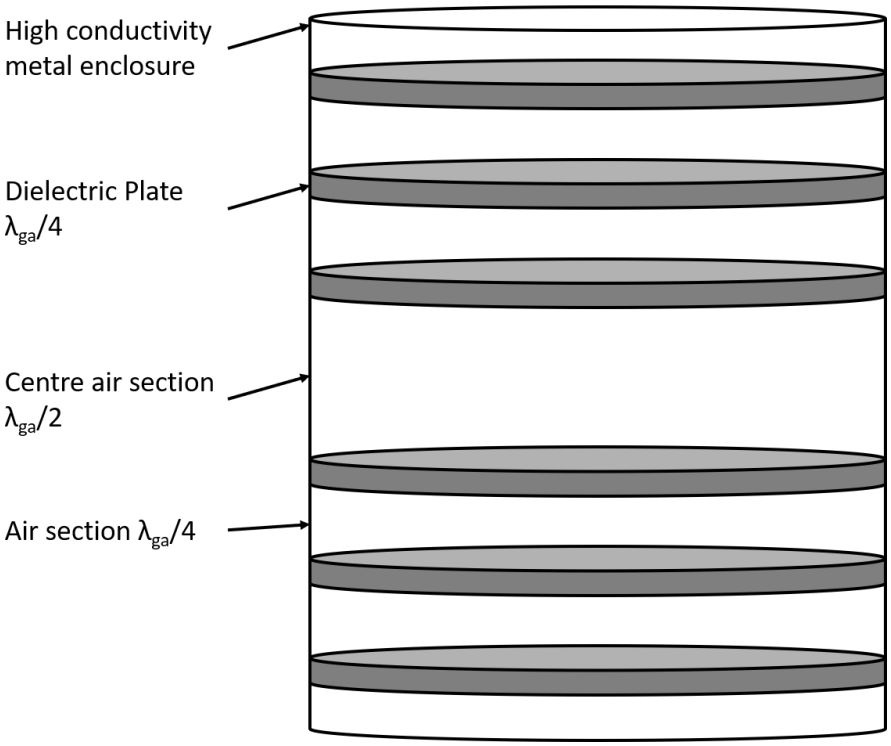


Figure 4.1: Periodic DBR diagram with equal $\lambda/4$ air and dielectric sections. An aperiodic DBR would be optimised such that the size of the sections asymptotically approach $\lambda/4$.

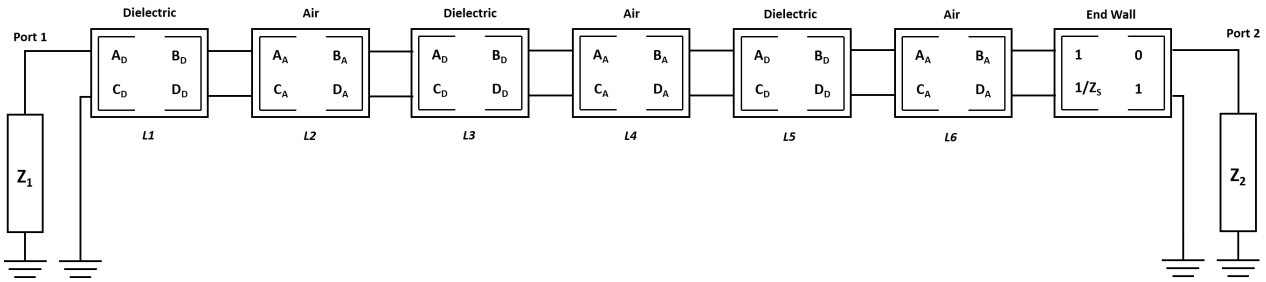


Figure 4.2: Series of waveguide ABCD parameter models used to model half of the 6 plate DBR. The resonator is symmetrical so it is therefore possible to consider half of the sections in the model.

length of a lossy transmission line used to model this chamber. γ is given by:

$$\gamma = \alpha + j\beta \tag{4.5}$$

where β is:

$$\beta = \sqrt{\omega^2\mu\varepsilon - \left(\frac{\chi'_{mn}}{a}\right)^2} \tag{4.6}$$

where ω is the oscillating angular frequency, μ is the relative permeability, ε relative permittivity, χ is the nth zeros of the derivative of the Bessel function of order m, and a is the radius of the chamber.

Attenuation in the air sections

The attenuation coefficient, α, is different for the air gap and dielectric sections as the only losses present in the air sections are from the side walls. The attenuation in Np/m is given by (4.7) for the attenuation coefficient of the air section for a TE_{mn} mode of frequency f [56].

$$(\alpha_c)^{TE_z}_{mn} = \frac{R_s}{a\eta\sqrt{1 - \left(\frac{f_c}{f}\right)^2}}\left[\left(\frac{f_c}{f}\right)^2 + \frac{m^2}{\chi'_{nm} - m^2}\right] \tag{4.7}$$

where η is:

$$\eta = \sqrt{\frac{\mu}{\varepsilon}} \tag{4.8}$$

The surface loss resistance of the guide walls is R_s, the lower cut off frequency is f_c of the waveguide section given in (4.9):

$$f_c = \frac{\chi'_{mn}}{2\pi\alpha\sqrt{\mu\varepsilon}} \tag{4.9}$$

The guide wave impedance, Z_{TE}, is given by (4.10):

$$Z_{TE} = \frac{\eta}{\sqrt{1 - \left(\frac{f_c}{f}\right)^2}} \tag{4.10}$$

For the dielectric plates, the loss of this section is the sum of the loss due to the dielectric material and the losses due to the conducting side walls:

$$\alpha_t = \alpha_c + \alpha_d \tag{4.11}$$

The loss of the conducting side wall, α_c is given in (4.7) and α_d is given in (4.12) [56]:

$$\alpha_d = \frac{\omega^2 \mu\varepsilon \tan\delta}{2\sqrt{\omega^2\mu\varepsilon - \left(\frac{\chi'_{nm}}{a}\right)^2}} \tag{4.12}$$

where tanδ is the loss tangent of the dielectric, given by the manufacturer as 2×10^{-5} for the alumina plates used in this chamber, and epsilon is the relative permittivity of the dielectric, in this case 9.75.

The loss in the metal end walls of the cavity is approximated by considering the complex propagation constant and the intrinsic wave impedance for a good conductor [56]. The surface roughness of the material was not considered in this calculation. The complex propagation constant is given in (4.13):

$$\begin{aligned} \gamma &= j\omega\sqrt{\mu\varepsilon}\sqrt{\frac{\omega\mu\sigma}{2}} \\ &= (1+j)\sqrt{\frac{\omega\mu\sigma}{2}} \end{aligned} \tag{4.13}$$

For a good conductor the intrinsic wave impedance is :

$$\eta = \frac{j\omega\mu}{\gamma} \tag{4.14}$$

Rearranging for γ, substituting into (4.13) and then simplifying gives an equation for the wave impedance in a good conductor, Z_S, in terms of the metal conductivity, σ, angular frequency ω and the metal permeability μ (typically 1) :

$$\eta = Z_S = (1+j)\sqrt{\frac{\omega\mu}{2\sigma}} \tag{4.15}$$

These equations can be used to design each waveguide section in a periodic DBR where the lengths of the air and dielectric sections are a quarter of a wavelength at 16 GHz. A periodic structure was designed first before the design was optimised to maximise the magnitude of the input reflection coefficient (S_{11}), using a genetic algorithm to vary the plate positions. The radius of the cavity is 37.5mm.

The dimensions of the air gaps and each plate for the optimised aperiodic DBR are shown in table 4.1, the value asymptotically approaches $\lambda/4$ the closer the section is to the end walls.

Section Identifier	Material	Thickness/mm
L_C	Air	10.7
L_1	Dielectric	0.97
L_2	Air	8.37
L_3	Dielectric	1.2
L_4	Air	7.62
L_5	Dielectric	1.55
L_6	Air	4.92
L_{END}	Copper	6.85

Table 4.1: Dimensions of air gaps and plates.

4.1.2 CST Eigenmode solver simulation of 16GHz DBR

The distributed Bragg resonator was modelled in CST and simulated without any coupling mechanism using the Eigenmode solver to simulated the resonant frequency and calculate the Q_0. The copper enclosure used the library material for 'annealed' copper with an electric conductivity of 5.8×10^7 S/m, the library model for air for the air sections and the 'lossy' Alumina model with a specified loss tangent of 2×10^{-5} and dielectric conductivity of 9.75. These parameters were obtained from the manufacturer of the plates. Figure 4.3 is a cross section view of the DBR used in the Eigenmode CST simulation. The brown material is the copper, the pale colour represented the dielectric plates and the air sections are hidden.

The high Q TE_{011} mode was observed to resonate at 15.7872 GHz as demonstrated in figures 4.4. In the first figure a cross section of the model of the DBR at the plane Z = 0 shows the magnetic field distribution in all sections. The red areas show where the field is strongest with blue being the weakest field. As expected the field is strongest at the edges of the cavity and in the centre with the field patterns getting weaker the further away from the centre the field is. The arrows indicate the direction of the field which shows that close to the walls the magnetic field acts in the opposite direction to the field at the centre. The second and third images show the DBR model observed at the cross section where Y=0, the vertical middle of the resonator. The second image shows the electric field of the TE_{011} mode that spins around the centre and is weakest where the H field is observed to be strongest. The third image is a plot of the H field across the plane Y=0 confirming the correct field pattern and showing that the field is strongest at the walls and in the centre but also that field acts

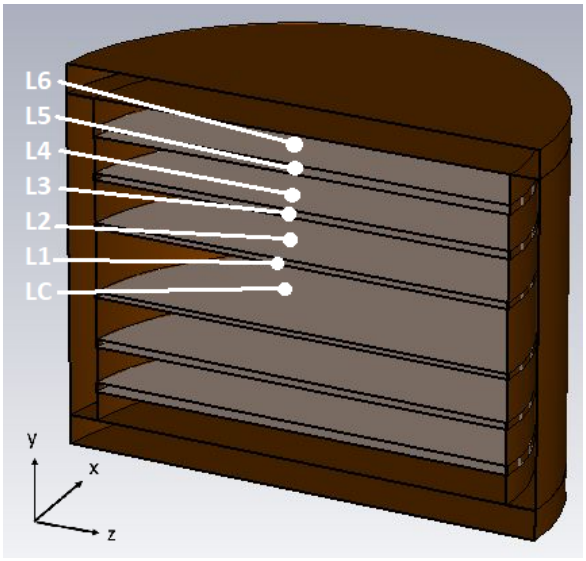


Figure 4.3: Cross section of the model of the 16 GHz DBR used in the eignemode simulations with labelled Air/Dielectric sections that match the labels given in table 4.1.

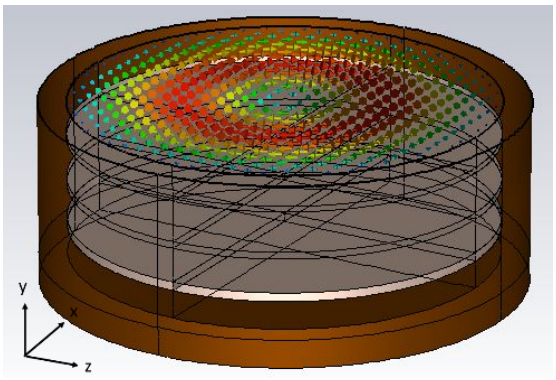
in opposite directions in these positions. The Eigenmode simulation estimates the Q_0 to be 215,000.

4.1.3 Spira Shield

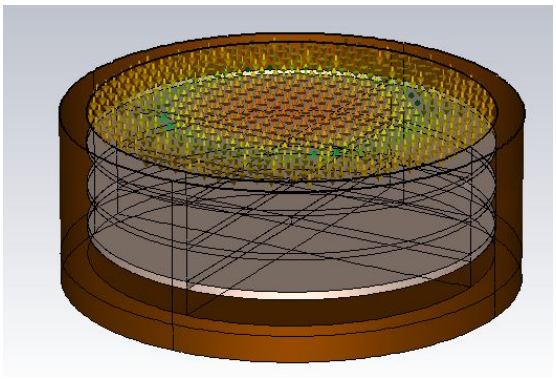
The DBR is built up from 6 copper rings, 6 dielectric plates and 2 end sections. The diameter of the alumina plates is larger than the diameter of the ring and there is a ledge cut into each one side of each ring for the plate to rest on. There is a groove cut onto the other side of the ring to allow a gasket to sit in. The chosen gasket was the 0.86mm $\pm$ 0.51mm Spira-Shield [60] and is held in place by four narrower sections that 'pinch' the gasket.

The gasket presses each alumina plate against the next copper ring to precisely position the plates within the cavity in order to reduce vibrations causing the plates to move and therefore cause the resonant frequency to vary and degrade the Q. Figure 4.5 shows the cross section of the side walls and the alumina plate press up to the next copper section by the gasket. The gasket also forms a seal between the copper rings and reduces EM leakage from within the cavity via the small gaps between the rings.

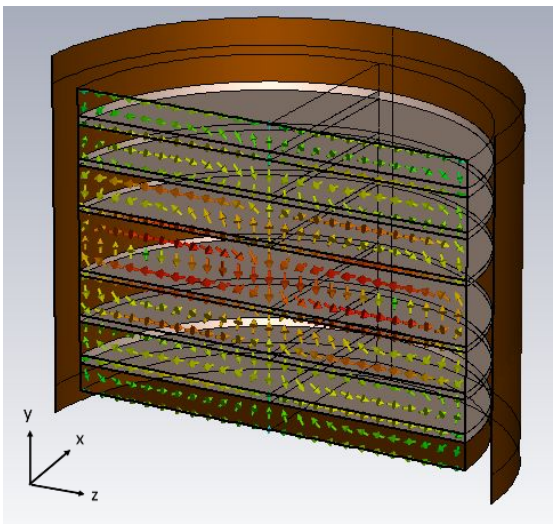
The chamber was assembled in two halves, starting at the middle plate and working towards the cavity end wall. Figure 4.6 shows how the bottom half of the chamber was has been constructed first



(a) Electric field inside the DBR on the plane y = 0.



(b) Magnetic field inside the DBR on the plane y = 0.



(c) Magnetic field inside the DBR on the plane z = 0.

Figure 4.4: EM field patterns on the z = 0 and y = 0 planes demonstrating the correct field patterns or the TE_{011} mode. The resonant frequency is 15.7872 GHz.

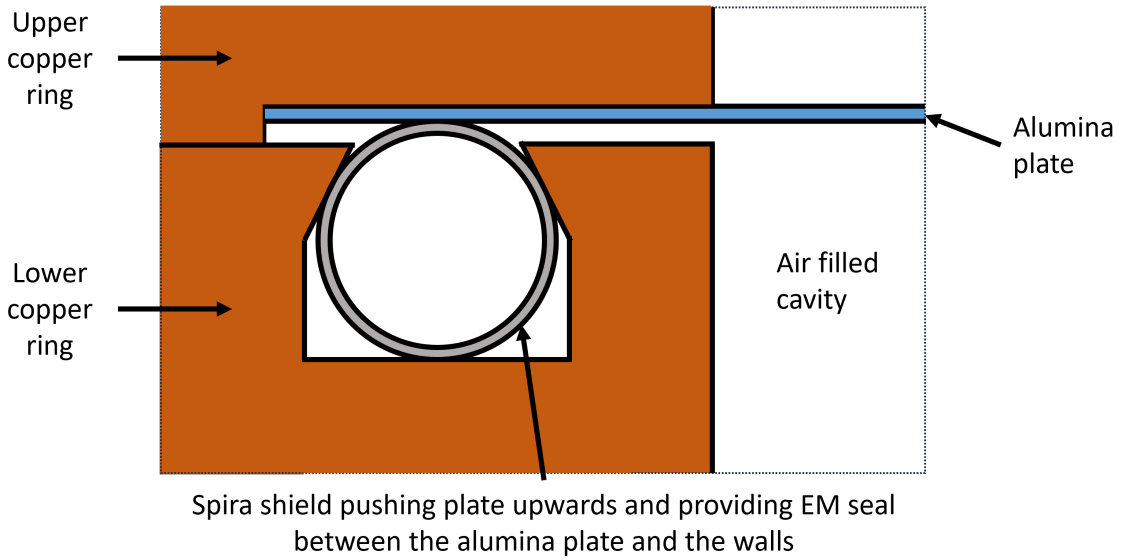


Figure 4.5: Cross section of the DBR side wall showing the Spira shield gasket pressing the alumina plate against the upper copper ring.

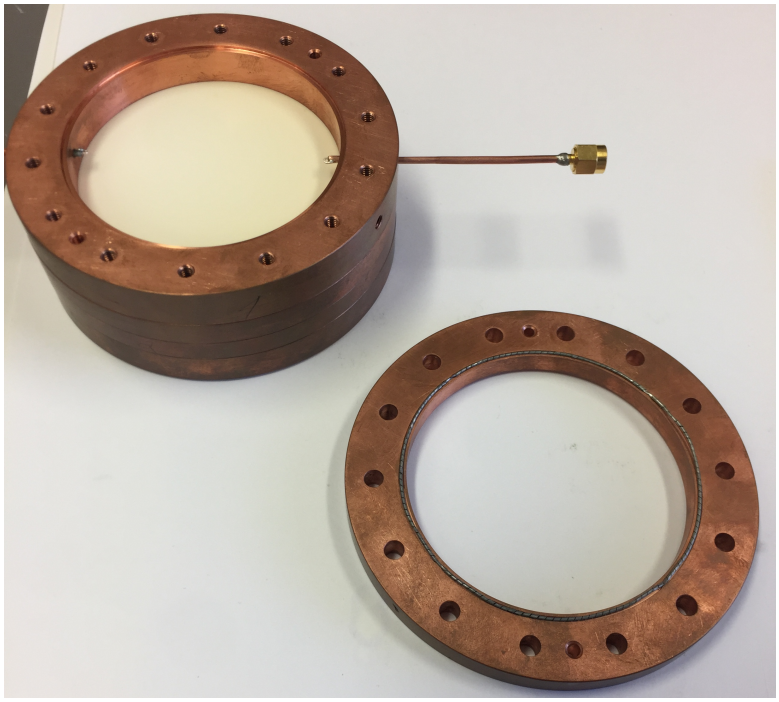


Figure 4.6: Half of the DBR assembly with the Spira Shield.

Component	Material	Diameter/mm
Outer Conductor	Copper	2.2 ± 0.03
Dielectric	PTFE	1.68 ± 0.03
Inner Conductor	Silver plated copper clad steel	0.51 ± 0.013

Table 4.2: Dimensions and material of RG405 coaxial cable used to manufacture the DBR probes.

and screwed in from the bottom. Initially this half was built up from the middle plate, and screwed down from the top but it has now been flipped so that the second half can be built up from the middle. The small silver ring in this figure demonstrates a Spira gasket secured in place.

The narrow sections in the grooves are not sufficient to stop the gasket from falling out of place due to gravity and a small amount of superglue was used in between each of the 'pinched' sections to reinforce them and hold the gasket in place.

4.2 Coupling to resonator

This section presents the findings of the research into coupling to the high Q TE_{011} mode in the resonator with insertion loss as close to 6dB as possible. Coaxial loop probes and aperture coupling have been investigated in both simulation and in practise.

4.2.1 Initial loop probe measurements

It was shown in Chapter 2 that the insertion loss of the resonator should be -6dB to make the ratio Q_L/Q_0 minimum. This is the point at which a quarter of the power is reflected, a quarter of the power is transmitted and the remaining half is dissipated by the resonator and maintains the Q_L/Q_0 and is optimum for low phase noise.

Initial experimentation used hand-made probes made from RG405 coaxial cable with a loop formed by the centre conductor and the outer shield. The loop had an internal diameter of approximately 0.1mm. This diameter is an estimated value based on the dimensions of the RG405 coaxial cable that are listed in table 4.2. The probe position was varied by pushing the probes further into the cavity from a starting point within the cavity walls in 1mm increments. The measured insertion loss and calculated Q_0 from this experiment are shown in Figure 4.7.

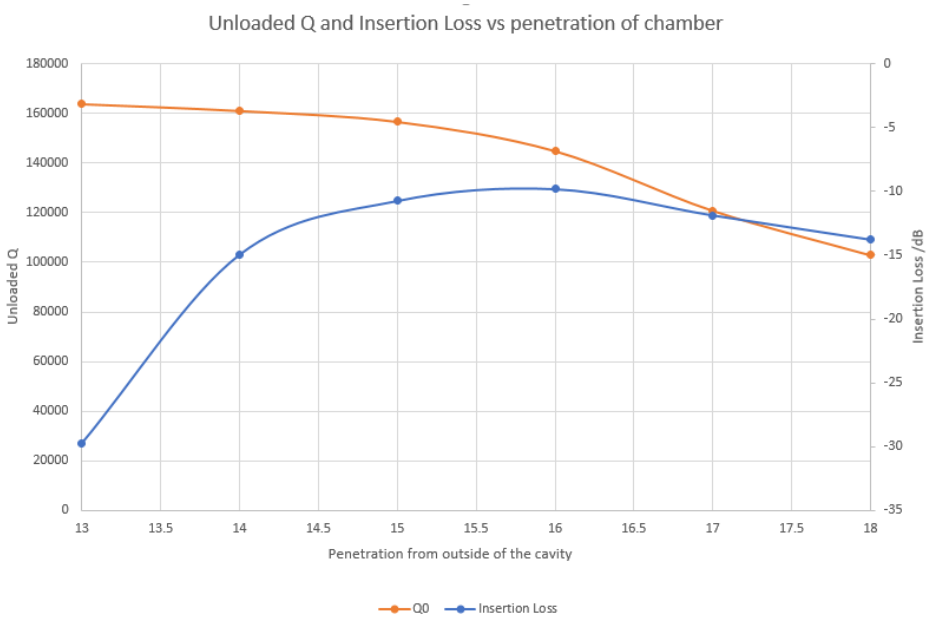


Figure 4.7: Q_0 and Insertion loss variation plotted against the penetration of the loop probes into the cavity.

The Q_l was calculated by measuring the resonant frequency and dividing this value by the measured 3dB bandwidth which was then used to calculate the Q_0 using (4.16).

$$Q_0 = \frac{Q_L}{(1 - |S_{21}(\omega_0)|)} \tag{4.16}$$

The highest Q_0 observed occurred when the penetration of the probe from the outer edge of the wall was 13mm. The cavity wall thickness is 15mm. The probe was within the wall in this position and the insertion loss was -29.7dB. At a penetration of 16mm (approximately 1mm within the cavity), the lowest insertion loss of -10.57dB was observed. Q_0 was calculated to be 145,000 when the probes were placed in that position. (4.16) assumes equal coupling from both probes, which, is not an accurate assumption for the probes used in this measurements. The loops are not identical in size and the length of the coax is different. Furthermore, once inside the cavity there is no way of knowing that the probes are orientated in an identical manner and are positioned perfectly flat to ensure maximum coupling to the H field without dismantling it. It was therefore decided that a simulation approach would be taken as this method ensures that the probes are identical in size and placement.

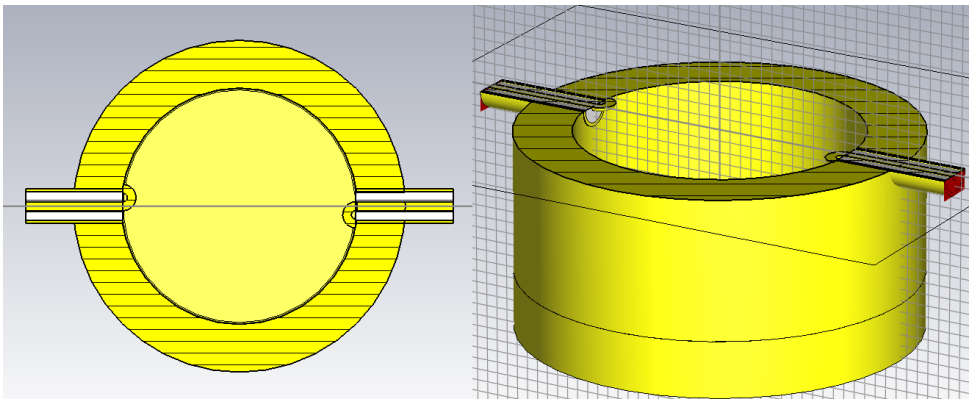


Figure 4.8: CST model of the DBR with variable coaxial probes at 5 GHz. The same model was later modified such that the dimensions were smaller and the TE_{011} mode was resonant at 16 GHz.

4.2.2 Loop probe simulations

A 16 GHz cylindrical cavity was modelled in CST and the Q_0 for these simulations was dropped to 5000 by reducing the conductivity of the copper model from 5.8×10^7 S/m to 8.07×10^5 S/m, to reduce the simulation time. The cavity radius is 12.359mm and the height is double the radius, 24.718 mm, to ensure the highest unloaded Q in the TE_{011} mode. An Eigenmode solver simulation was run first to obtain the field pattern within the cavity to show where the magnetic field in the TE_{011} mode is strongest. The eigenmode solver does not use any ports so this simulation did not include any coupling probes.

Once the correct field pattern for the TE_{011} mode was observed in simulation, the frequency domain solver was used to simulate the resonator with coaxial loop probes as it is suggested by the vendor to be used for highly resonant structures such as cavity resonators. Parametric sweeps were run varying the probe radius and penetration of the probes. The centre conductor of the RG405 model was extended and curved around to the outer conductor of the coaxial cable as demonstrated in figure 4.8.

A series of simulations were run varying the probe radius from 0.05mm to 1.05mm, probe loops were kept as close as possible to the cavity wall as possible. Low insertion loss of between -3 and -6dB was achieved although the Q_0 reduced by half from the designed 5000 to 2000 with the introduction of the probes. Further simulations varying the probe position within the cavity whilst maintaining 0.05mm loop radius have shown that slight increases Q_0 to approximately 2300 can be achieved,

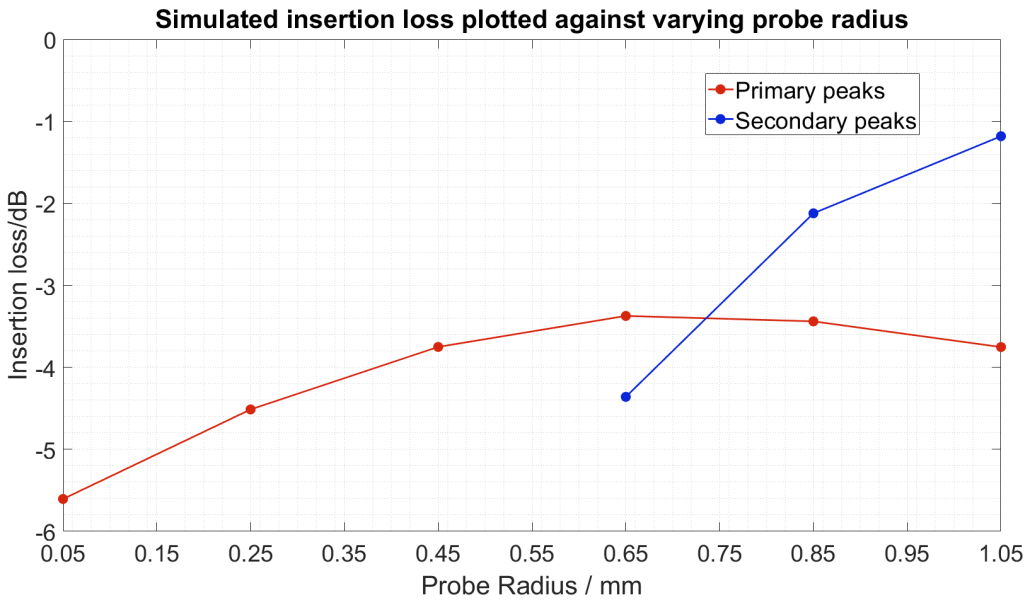


Figure 4.9: Simulated insertion loss plotted against bore depth of the probe with constant radius at 16 GHz.

whilst maintaining -6dB insertion loss. The general trend from reducing the probe radius shows that Insertion loss reduces whilst Q_0 increases.

Figure 4.9 is a plot of probe radius vs Insertion loss and Figure 4.10 is probe radius vs Q_0 at 16 GHz. These simulations suggest that at 16 GHz the RG405 coaxial cable is likely not the best size for designing probes that can achieve both high Q_0 and around 6dB insertion loss as the loop radius needs to be smaller than 0.05mm. Unfortunately the probes must be manufactured using RG405 Coax and the DBR already has the correct holes drilled for RG405 to penetrate into the walls. These simulations have however, provided useful information on where the probes should be best placed within the cavity in order to maximum the coupling to the high Q mode.

The optimum position is close to the cavity walls but not within them and the probe loops should be as small as possible to reduce insertion loss. There does appear to be a trade-off between high Q_0 and low insertion loss but it has been shown that high Qs can be achieved with insertion loss within the -3 to -9dB range.

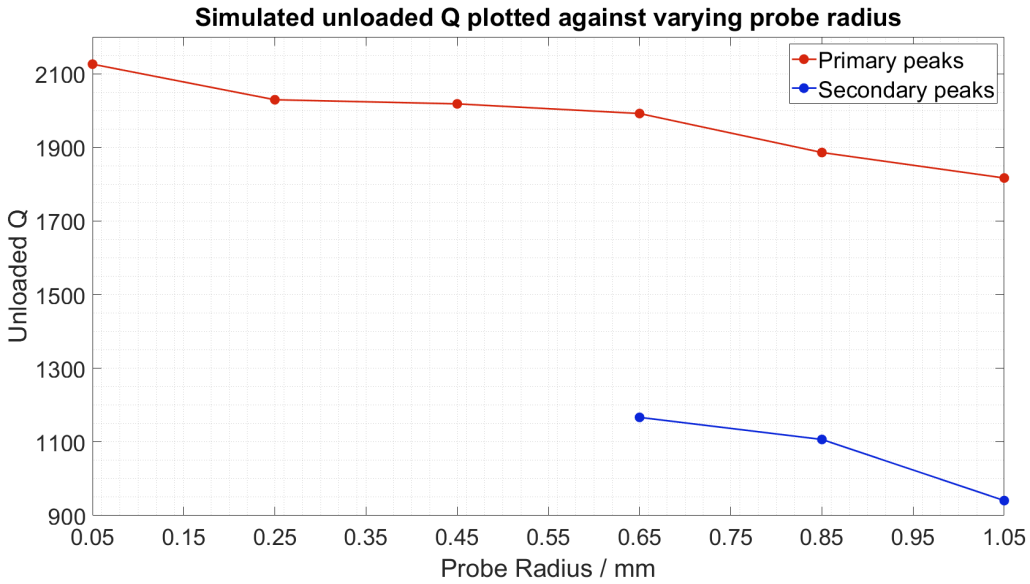


Figure 4.10: Calculated Q_0, using (4.16) and simulated Q_L, plotted against the probe bore depth of the probe with constant radius at 16 GHz.

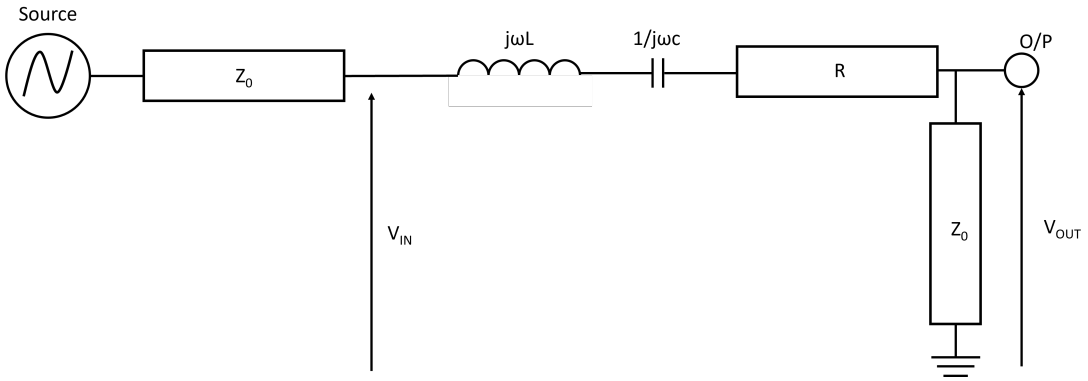
4.2.3 External impedance transformation network

It became difficult to manufacture identical probes by hand and place them exactly to couple to the high Q mode and maintain 6dB insertion loss at resonance and therefore a different approach using external impedance transformers was investigated. The impedance transformation network matches the resonator impedance at resonance to an optimum source and load impedance to achieve a specified insertion loss.

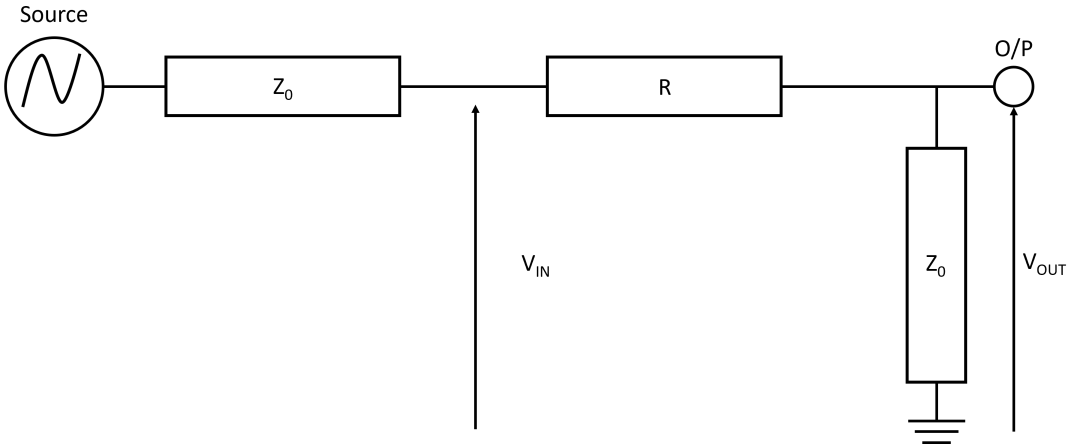
The 16 GHz resonator and the network analyser can be modelled as an LCR network connected to a source and load impedance as demonstrated in figure 4.11a. At the resonant frequency, the imaginary impedances presented by the inductor and capacitor cancel as $j\omega_0 L = \frac{1}{j\omega_0 C}$. The simplified model is shown in figure 4.11b. The insertion loss at resonance can be calculated using the following equation:

$$S_{21} = \frac{V_{out}}{V_{in}} (1 + S_{11}) \tag{4.17}$$

The ratio $\frac{V_{out}}{V_{in}}$ is equal to the ratio $\frac{Z_0}{R+Z_0}$. The return loss at resonance, S_{11}, is given by the reflection



(a) Simplified LCR model of the resonator connected to a network analyser.



(b) Simplified LCR model at resonance connected to a network analyser where the imaginary impedances have cancelled each other.

coefficient:

$$S_{11} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{4.18}$$

where Z_L is the sum of the real impedance of the resonator and load impedance, $R + Z_0$. Substituting (4.18) into (4.17) gives:

$$S_{21} = \frac{Z_0}{R + Z_0}\left(1 + \frac{R}{R + 2Z_0}\right) \tag{4.19}$$

This equation can be simplified and rearranged into quadratic equation that can be solved for R for a given S_{21} and load impedance:

$$0 = 2RZ_0 + 2Z_0^2 - S_{21}(R^2 + 3Z_0R + Z_0^2) \tag{4.20}$$

With the calculated resistance at resonance, it is possible to calculate an optimum source and load impedance for a specified insertion loss at resonance. A quarter wave transformer is used transform the actual source and load impedance to the optimum value so that the resonator sees the optimum source and load impedance presented to it at the resonant frequency and, therefore, the insertion loss is changed to a specific value.

The insertion loss of the DBR were measured using the Anristu 37377C Vector Network Analyser network analyser, to be -10.579dB and the load and source impedance are 50Ω. Using (4.20), the value of the series resistance is calculated to be 245.75 Ω.

At resonance Q_0 is given in terms of resistance, R, and capacitance, C, in 4.21. The resonant frequency is defined in terms of inductance, L, and capacitance in 4.22.

$$Q_0 = \frac{1}{\omega_0 RC} \tag{4.21}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{4.22}$$

4.21 is rearranged in terms of C to give 4.23 and 4.22 is rearranged for L to give 4.21. The reactive component values can now be calculated. The resonant frequency of 16.0302 GHz and Q_0 of 141,502 are substituted into 4.23 & 4.24 to give C = 0.252aF and L = 390.3913μH.

$$C = \frac{1}{\omega_0 R Q_0} \tag{4.23}$$

Microstrip Component	Width/mm	Length/mm	Impedance Ω	Electrical Length °
λ/4 Transformer	0.153	2.93	93.1	90
Phase matching	0.552	0.937	50	30

Table 4.3: Calculated lengths and Widths from LineCalc after optimisation.

$$L = \frac{1}{C\omega_0^2} \tag{4.24}$$

The optimum source and load impedance can now be calculated to give an insertion loss of 6dB in the system by substituting the value for the series resistance into (4.20) and solving for Z_0, once again assuming the losses of the resonator are purely resistive. This calculated load impedance is 123.8 Ω.

It is important to note however, that this LCR equivalent has 0° phase shift at resonance due to the L and C components cancelling each other out. This is not observed in the actual DBR. The phase shift at resonance is in fact 64° and must also be accounted for. An ADS simulation was set up that demonstrates how the change in source and load impedance of the LCR equivalent changes the insertion loss at resonance to the required value of 6dB. Further an S-Parameter block loaded with the S2P file obtained from the VNWA, is simulated with additional lengths of ideal microstrip line of 32° to change the measured phase at resonance to be 0°. From there the source and load impedances were changed to the calculated values achieve the 6dB loss at resonance.

A quarter wave transformer was designed and placed between the phase compensation transmission lines and the source and load to present the 123.8Ω to the resonator whilst presenting 50Ω to the rest of the measurement system. The λ/4 transformer impedance is the geometric mean of the actual source impedance and the calculated load impedance. The impedance of the λ/4 transformer is $\sqrt{50\Omega \times 123.8\Omega} = 93.1\Omega$. Once the correct performance had been verified and the electrical lengths and transformer impedance had been optimised, the values were converted to physical microstrip lines using the LineCalc tool in ADS. The dimensions are given in table 4.3.

A diagram of this simulation is shown in Figure 4.12. The measured S-parameters of the DBR were exported to an S2P file and used in the ADS simulation using the 'S2P' component. Figure 4.13 is plot of the measured S_{21}, the simulated S2P file with matching network, as well as the S2P file simulated with the matching networks set where the dimensions are 20% smaller to account for

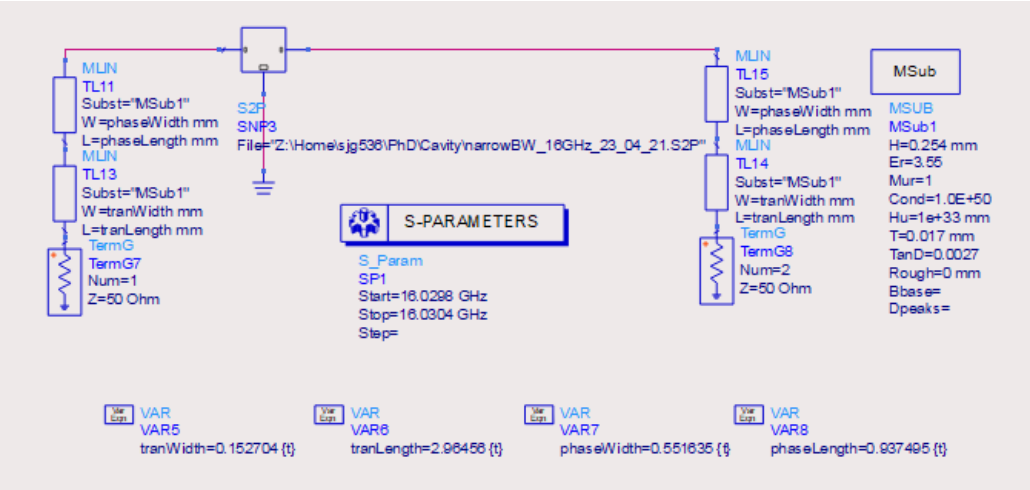


Figure 4.12: ADS Schematic for external impedance transformation networks with optimised microstrip lengths and widths. The S2P file created from the measurement of the 16 GHz DBR is loaded into the 'S2P' ADS component.

the worst case tolerances specified by the manufacturer, EuroCircuits. The impedance transformation network decreases the insertion loss to 6.07dB and the Q_0 is 139800. With the worst case tolerances the insertion loss increases to 8.35dB but the Q_0 increases slightly to 142000. This approach is that is not tuneable and cannot therefore account for the variation in performance due to the manufacturing tolerances. The critical parts are the length of the 50Ω microstrip lines that cause the resonator to have 0° phase at resonance and the length of the quarter wave transformers. A tuning simulation was set up to show the variation of the dimensions of the impedance transformer network affects the final performance.

It is shown in Figure 4.13 that the length of the delay lines affects the insertion loss, in this case increasing it by 2dB. Various tuning methods have been considered such using a weakly coupled length of microstrip line and manually cutting away the coupled line to vary the phase. However, when the coupled section is cut away there is negligible effect of the phase shift.

Another approach was to incorporate wider, lower impedance microstrip line that could be cut to the correct 50Ω width. This has been demonstrated in ADS simulation to vary the phase of the line but the constant variation in impedance results in a non-linearly changing insertion loss and results in the overall network becoming too lossy. After discussions with the EuroCircuits UK representative, it

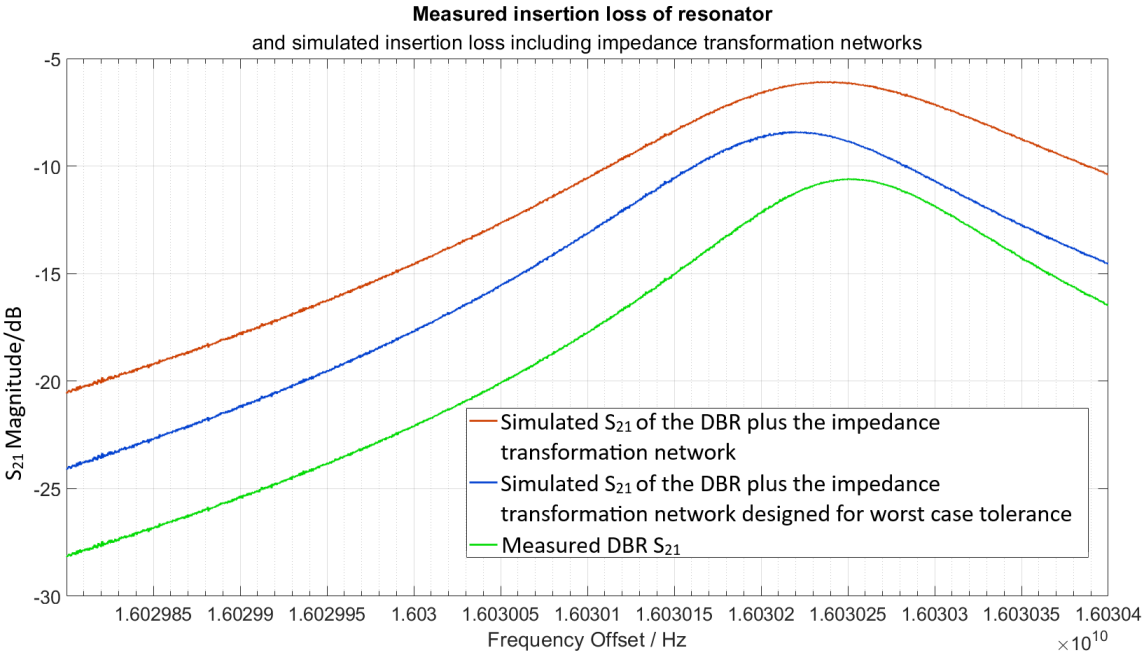


Figure 4.13: Measured S_{21} of the resonator (green trace), the simulated S_{21} of the measured S_{21} with the external matching network designed to reduce the insertion loss to 6dB, (red trace), and simulated resonant peak with 20% shorter length microstrip lines that accounts for the worst case tolerance in the manufacture.

Figure 4.14: Manufactured 'identical' probes. These updated probes were manufactured by hand so they cannot be perfectly identical.

was suggested the variation to the overall length of line would be very small. The simulation varying the widths of the tracks showed the effect of the track width tolerance on the insertion loss to also be very small.

As the probes were not identical, two new probes were manufactured by hand with small loops and with equal lengths of coaxial cable both set to 3λ (≈ 38.7 mm) to remove the need for the critical delay sections in the impedance transformer. Figure 4.14 is an image of the new probes. The new probe loops were manufactured by bending the centre conductor as tightly as possible back on itself and soldering to the outer ground conductor. A resistor leg was used to push the hole through the loop ensuring no PTFE was blocking the hole and to ensure the loops were approximately the same size. The new probes were used to measure the resonator at 16 GHz and a resonant peak at 16.023 GHz was observed with insertion loss of 8.15dB and calculated Q_0 of approx. 147,000. This improvement in insertion loss means that the impedance transformation network can be designed more easily with less intrinsic losses as the quarter wave transformer to 50Ω transition will result in a smaller amount of propagating power reflecting back from the ports. The series resistance at resonance was calculated to be 155.8Ω and the optimum source and load impedance was calculated to be 68.8Ω. A new network was designed using the same process as before and optimised in ADS with the new impedance transforming network

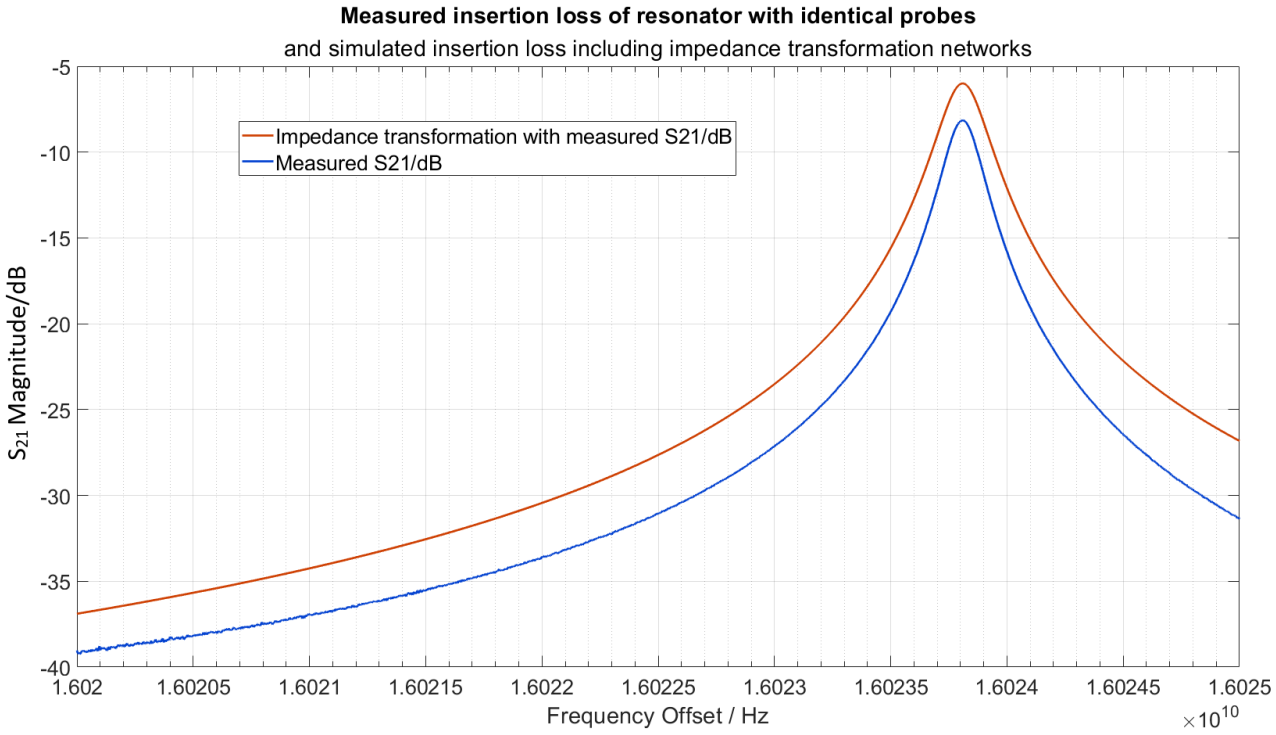


Figure 4.15: Measured magnitude of S_{21} of DBR using the new 'identical' probes and simulated magnitude of S_{21} of the impedance transformation network and the S2P file from the DBR measurement.

Microstrip Component	Width/mm	Length/mm	Impedance Ω	Electrical Length °
λ/4 Transformer	0.325	2.890	67	90
Phase matching	0.552	3.687	50	119

Table 4.4: Calculated lengths and Widths from LineCalc after optimisation.

design parameters shown in table 4.4.

The geometric mean of 50Ω and 68.8Ω is calculated to be 58.6Ω, however in simulation the insertion loss decreased to 7dB and not the 6dB required. With an impedance transformer of 67Ω impedance, the insertion loss dropped to 6.079dB.

Figure 4.15 shows the measured insertion loss and phase at resonance with new probes and the improvement to the insertion loss and phase with the impedance transforming network. The insertion loss decreases from 8.15dB to 6.07dB whilst the Q_0 remained at 147,000.

Manufactured Impedance transformation networks

The design for the impedance transformation network was incorporated into a PCB design with the taper and slots required for the WithWave 2.92 mm connectors that were selected for use in these measurements. 7 further PCBs were manufactured with varying phase matching lengths from -1 mm to +2.5 mm in 0.5 mm increments. The additional PCBs were manufactured to see how the variation in the phase compensation lengths of microstrip affected the measured insertion loss and measured Q_l at resonance. The networks were connected to the resonator and a series of measurements were made starting with the smallest phase compensation length up to the largest. Firstly, consider Figure 4.16 which is a plot of the measured and simulated insertion loss at resonance of the DBR with the impedance transformation networks. The simulated insertion loss of the resonator is highest when the matching network with no phase compensation line variation is used as expected. With increasing length of this line the insertion loss increases fairly linearly up to 2 mm additional length, approximately 65° additional phase for each network. The insertion loss at resonance is never exactly -6dB and the plot of the simulated insertion loss at resonance across the -1 mm to +0.5 mm range is almost a symmetrical around approximately -0.25 mm. This suggests that the length of the phase compensation line could be decreased to -0.25 mm to achieve an insertion loss of -6dB.

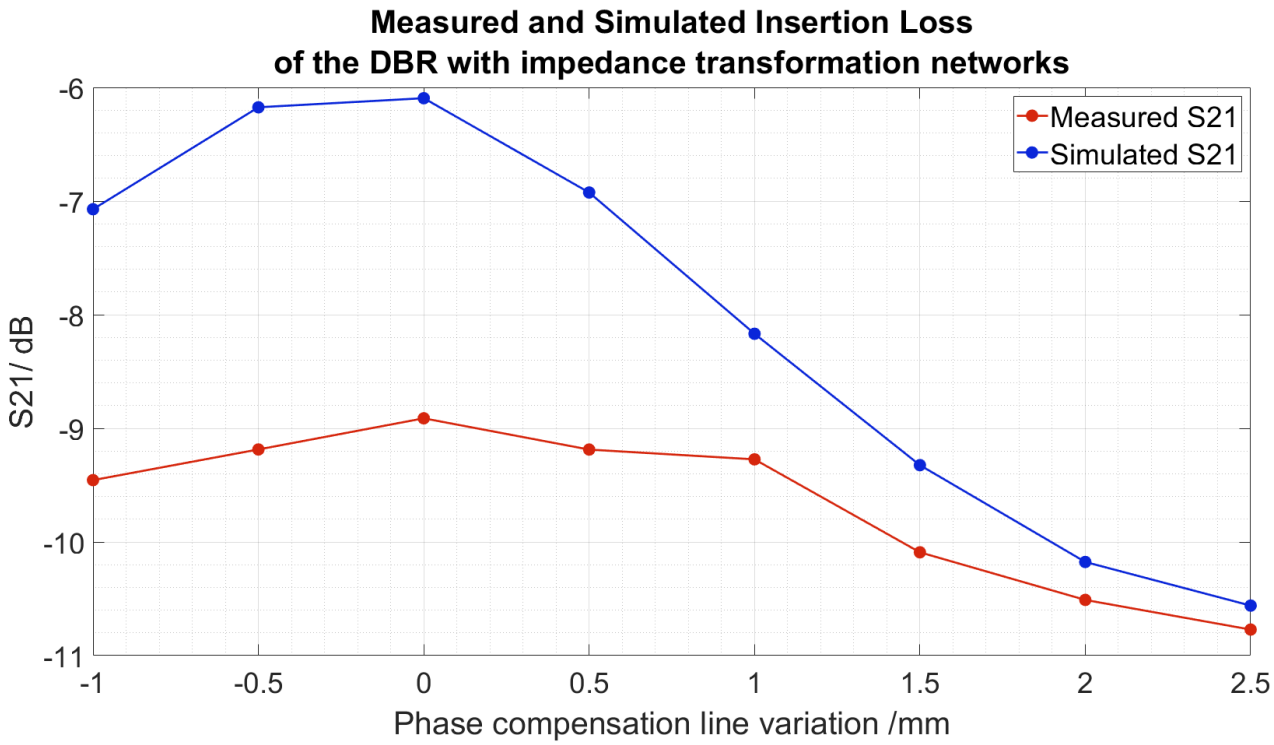


Figure 4.16: Measured and simulated resonator insertion loss at resonance with impedance transformation networks connected plotted against varying phase compensation microstrip line length variation.

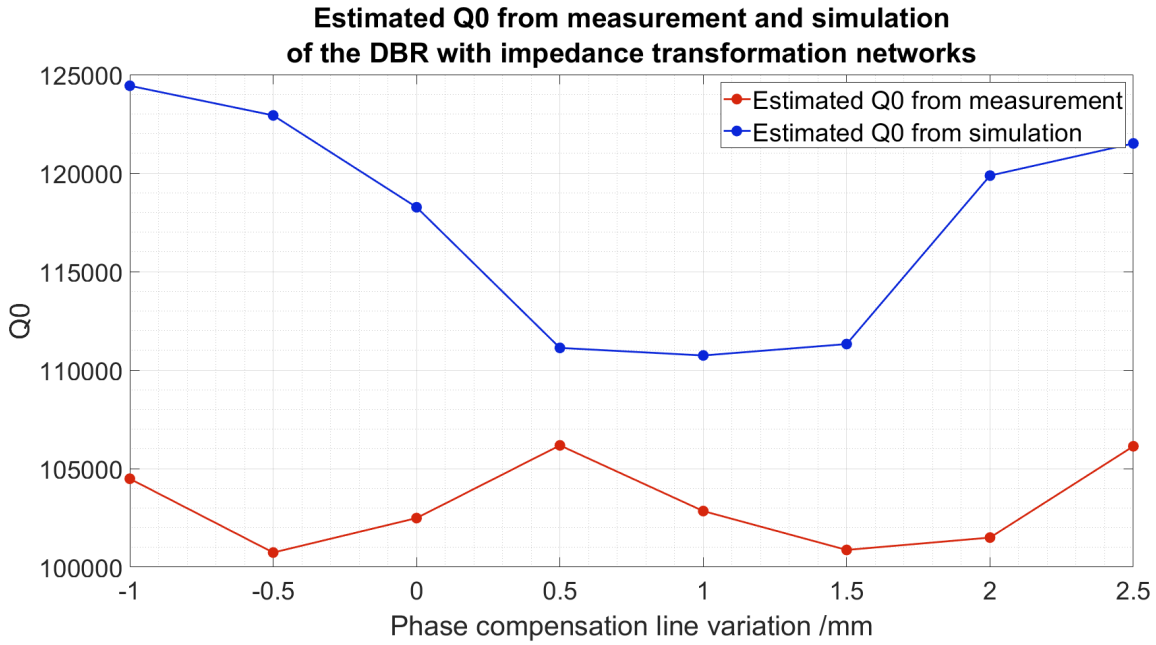


Figure 4.17: Measured and simulated resonator unloaded Q at resonance with impedance transformation networks connected.

The measured insertion loss however is consistently greater than the simulated values with the highest measured insertion loss of 8.912dB being 2.817dB larger than the simulated value. As with the simulated value this was observed with the matching network with 0 mm variation in the phase compensation line. Each of the impedance transformer networks is connected to the resonator and the VNWA with two WithWave 2.92 mm connectors each, which adds additional loss into the circuit that has not been accounted for in the design stage. It is thought that this additional loss is the cause of the difference in the simulated and measured insertion loss at resonance. Furthermore, the networks were designed to provide an impedance transformation from the resonator to a 50Ω system, however the actual source and load impedance is set by these connectors and presents an unknown impedance to both ends of the transformation network. The insertion loss and Q_l are both used to calculate the Q_0 of the resonator in simulation and measurement using (4.16) and it is plotted against varying phase compensation line in Figure 4.17. As with the insertion loss, the calculated Q_0 is consistently smaller in measurement however the maximum variation is smaller, approximately 5,000 in measurement compared with 14,000 in simulation.

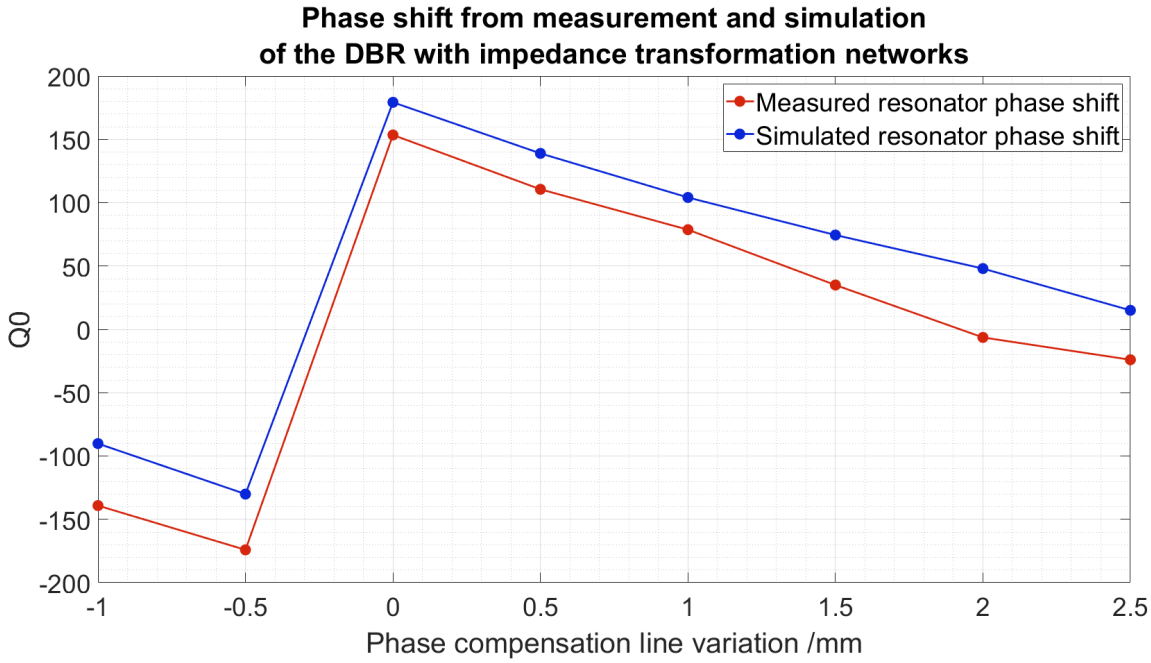


Figure 4.18: Measured and simulated resonator phase shift at resonance with impedance transformation networks connected.

The final plot of data from this set of measurements is shown in Figure 4.18 which is a plot of the measured and simulated phase shift of the entire resonator and impedance transformer network systems. The shape of both plots is similar with the phase shift decreasing at approximately the same rate. There is a constant offset however between the simulated and measured phase that indicates the that the manufactured PCBs introduce a constant phase shift across the range of circuits measured. This is likely to be introduced by the four connectors used on each PCB, which were used across all measurements but were not accounted for in simulation as the exact phase shift introduced by them has not been confirmed through measurement. The average phase variation between measurement and simulation is –38° or +322° suggesting that each with wave connector introduces 80.5° of phase shift each (assuming precisely manufactured PCBs and equal phase shift between the four connectors).

The S-parameters of the DBR without any impedance matching networks were remeasured and it was found that the insertion loss at resonance was no longer -8.15dB as used in the calculation of the resistor model used in the design stage but now -7.756dB. This variation is believed to be a result of temperature fluctuations and small movements in the probe position after the networks were

connected and disconnected from the DBR.

The simulation was modified to include the S-parameter file from the most recent measurement of the DBR with an insertion of -7.756dB at resonance and the impedance transformation networks designed for the DBR with an insertion loss of -8.15dB were added. The simulated insertion loss was -6.09dB, a difference of 0.01dB from the previous simulated insertion loss at resonance with the S-Parameters that gave an insertion loss at resonance at -8.15dB. The only part of the PCB that was not included in the simulation model was the connectors which suggest their influence on the PCB must cause the degradation in insertion loss and Q_0 of the resonator with the impedance transformation networks.

Whilst showing in simulation that an impedance transformation network can decrease the insertion loss of a resonator, the implementation of such a network increases the insertion loss and degrades the Q_0 of the resonator. In order to overcome the losses and phase shift introduced by the connectors, a precise model is required but such a model is unavailable. This method of reducing the resonator insertion loss was therefore not incorporated into the final oscillator design.

4.2.4 Waveguide Coupling

Aperture coupling into cavities from waveguides is presented in [61] and is a coupling mechanism that was considered as part of this research to reduce the insertion loss of the resonator, to ensure identical coupling at the input and output and to reduce vibration sensitivity. As described, it became very difficult to manufacture by hand, small loop probes that were identical in shape and size resulting in unequal coupling.

This can degrade the calculated Q_0 from (4.16) as it is assumed there is equal coupling at both ports for this equation to be accurate. Furthermore, waveguide is rigid and can be bolted to the cavity in a more secure way than the probes making this coupling method less susceptive to vibrations that have been shown to degrade the Q.

The coupling by small aperture theory presented by Bethe [62] demonstrates the relationships between the fields inside two cavities separated by an infinitely thin conductive wall with a small hole in it and is used to calculate the characteristic frequencies and phase relationships of such system or to calculate the field strength and the spatial distribution of emitted radiation from a small hole. The

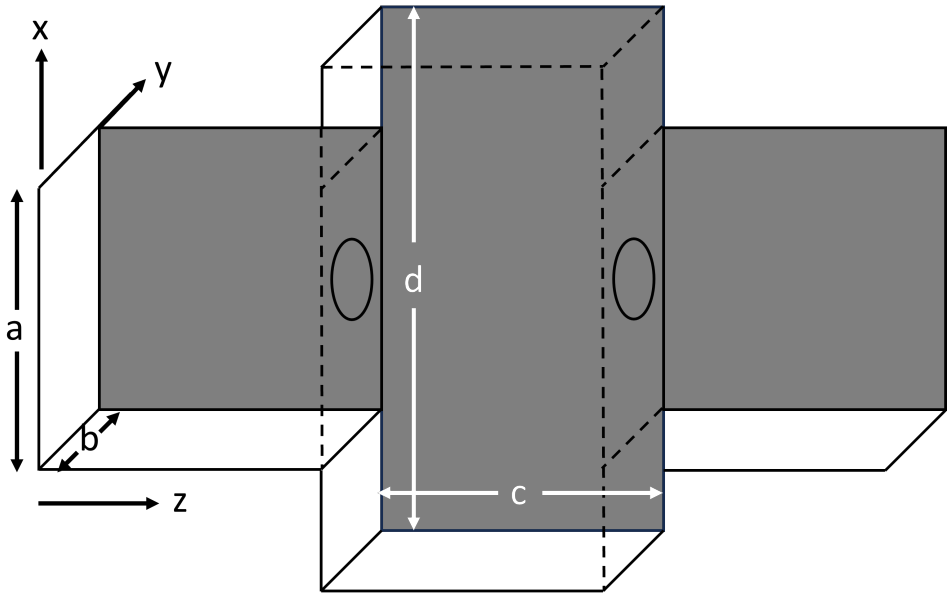
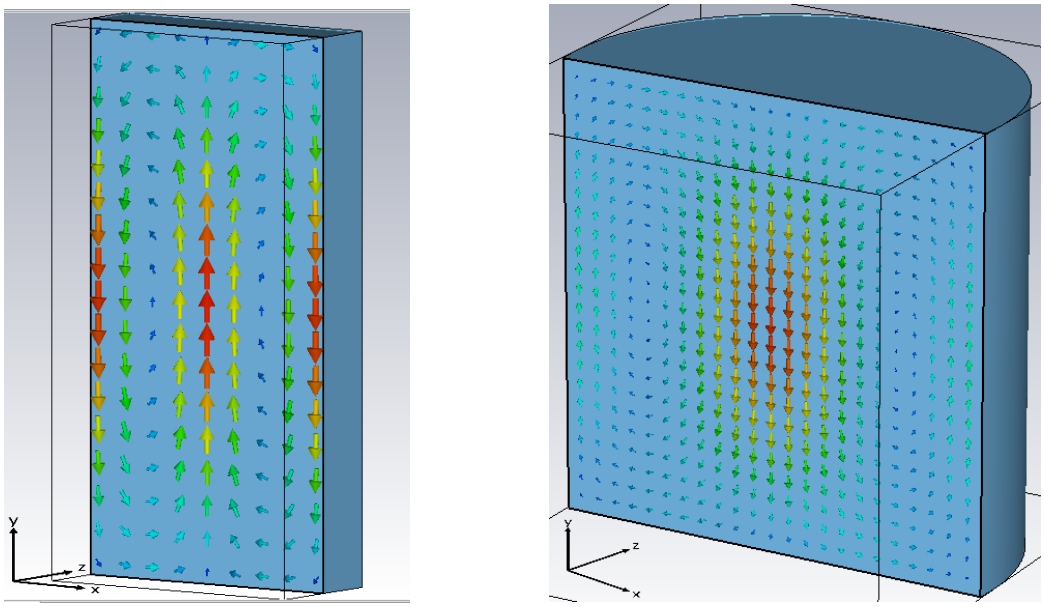


Figure 4.19: Two port cavity system taken from [61] and used as the starting point for the design of the aperture coupling to the DBR.

theory states that the aperture is equivalent to the combination of radiating electric and magnetic dipoles, where the dipole moments are are proportional to the electric field in the normal direction and magnetic field in the in the tangential direction respectively. Collin [61] presents an example of aperture coupling from waveguides to resonant cavities is presented where it is shown that the external Q, Q_e of a two port rectangular cavity resonating in the TE_{101} mode, coupled to rectangular waveguides by small circular apertures is given by (4.25):

$$Q_e = \frac{acdb^2}{8\alpha_m^2\beta_{10}}\left(\frac{k_{101}c}{\pi}\right)^2 \qquad [61] \tag{4.25}$$

where a is the width of the waveguide, b is the height of the waveguide and the cavity, c is the length of the cavity, d is the width of the cavity, β_{10} is propagation constant of the TE_{10} mode in the waveguide, k_{101} is the cutoff wave-number for the TE_{101} mode and α_m is the magnetic polarizability of the aperture. For a round hole $\alpha_m = \frac{4r_0^3}{3}$ [61] (r_0 is the hole radius) and for a rectangular hole $\alpha_m = \frac{\pi l d^2}{16}$ [61] (l is the aperture width and d is the aperture height), assuming that the thickness of the wall is infinitely small. The diagram of the example two port cavity system from [61] is shown in Figure 4.19, the induced magnetic dipole in the aperture is directed in the x direction.



(a) H field of the TE_{101} in a rectangular cavity. (b) H field of the TE_{011} in a cylindrical cavity.

Figure 4.20: Magnetic field patterns plotted on a plane of TE_{101} mode in a rectangular cavity and the TE_{011} showing the similarities between the H fields in both modes.

The H-Field of the TE_{101} mode in a rectangular cavity is shown in Figure 4.20a, the magnetic field is orientated in the vertical, Y, direction in this model and is equivalent to the X direction in the diagram in 4.19.

The field pattern is strongest at the side walls, where the apertures would be positioned, and in the middle of the cavity. This figure shows a cross section of the cavity of the plane at Y = 0, the field pattern is observed in all planes at all values for Y.

The H field across the plane at Y=0 for the TE_{011} mode in a cylindrical cavity is shown in Figure 4.20b where the vertical, Y, axis is equivalent to the X axis in the diagram in 4.19. The field pattern on this plane is identical to that of the field shown in Figure 4.20a on the plane Y=0.

Unlike the rectangular cavity, the field pattern is not observed in all planes at all values for Y, as the cavity is cylindrical. It is assumed that (4.25) can be used to design the input and output aperture for a cylindrical cavity as the magnetic field in the vicinity of the aperture is the same across the width of it if the size of the aperture is very small compared to the diameter.

Design procedure

(4.25) can be rearranged for the magnetic polarizability, α_m of the aperture as follows:

$$\alpha_m = \sqrt{\frac{acdb^2}{8Q_e\beta_{01}}\left(\frac{k_{011}c}{\pi}\right)^2} \tag{4.26}$$

were the parameters have the same meanings as before. The distributed Bragg cavity is built up from different waveguide sections of alternating material with lengths asymptotically approaching $\lambda/4$ as they get closer to the end wall. This introduces an additional constraint on the design of an aperture to be used to couple from an external piece of waveguide. The aperture must not be larger than the height of the central section, 10.71mm, as the aperture would then extend across three of the cavity sections.

Furthermore, the input and output waveguides must be designed such that the magnetic field inside the waveguide is orientated in the same direction as that inside the cavity, the broad wall must be orientated in the vertical direction for the TE_{01} to become dominant. A custom rectangular waveguide was designed such that the TE_{01} is the dominant mode and the cut off frequency was less than 16 GHz. WR42 waveguide was considered for use however the dimensions of the broad wall are 10.668mm, this would increase the difficulty in manufacturing the central section with a thin aperture as the height of the central section in 10.71mm.

A rectangular waveguide with a vertically orientated broad wall of 10.25mm will have a cutoff frequency of 14.624 GHz and the dominant mode is the TE_{01} mode. The short side was set to 4mm to keep the ratio of the waveguide sides similar to the ratio of the dimensions of the WR42 waveguide and the Q_0 and Q_e were set to 200,000 (therefore there should be no losses in the ideal case). The dimensions of the central section of the DBR were used as most of the field is contained within this section. The height is 10.7mm and the radius is 37.5mm. The desired magnetic polarizability of an aperture is calculated to be $3.299 \times 10^{-9}mm^3$ using these values for Q_0, a and b.

From this value the design of the aperture can be made using $\alpha_m = \frac{4r_0^3}{3}$ for a round hole and $\alpha_m = \frac{\pi l d^2}{16}$ for a rectangular hole. The radius of the round hole should be 1.353mm. The equation for the dimensions of the rectangular aperture has two unknown quantities, the height l and the width d.

The height was set to 8mm as this is almost the height of the waveguide and ensures that the

calculated width will be small as d is inversely proportional to $\sqrt{1}$. The calculated width of the aperture is 1.449mm.

Simulation

The distributed Bragg resonator was modelled in CST including all air and dielectric sections. The walls used the lossy copper component included in CST with an electric conductivity of 5.8×10^7. The alumina plates were modelled using the lossy Alumina component in CST where the dielectric constant was specified as 9.75 and the loss tangent set to a constant 2×10^{-5}. The waveguide and aperture were also modelled and waveguide ports were used in the frequency domain solver simulations. The eigenmode solver was also used to simulate the resonant modes of the cavity and aperture however the waveguide sections were closed at the ends to form a short circuit.

The waveguide sections were simulated first to confirm that the TE_{011} was the dominant mode. The correct field pattern and cut off frequency of 14.629 GHz confirm that this waveguide is suitable for use at 16 GHz. The aperture aims to couple the propagating TE_{01} mode in the waveguide to the TE_{011} mode in the cavity, the orientation of the waveguide is such that the magnetic field in the waveguide is orientated vertically, in the same direction as the magnetic field of the TE_{011} mode in the cavity. By using a tall and narrow rectangular aperture, it was thought that other spurious modes near the 16 GHz resonant frequency would not be coupled to if their magnetic fields were not orientated in the same direction.

The simulations of the waveguide and Bragg cavity used the rectangular aperture where the height of the aperture was 8mm and the width was 1.5mm. A series of simulations have been made that initially used a larger loss tangent of 2×10^{-4} and then decreasing to the required 2×10^{-5}. This procedure was followed as it was found that the simulation of the DBR where the loss tangent of the alumina was set to 2×10^{-5} would not complete successfully with adaptive mesh refinement as too many mesh cells were created by the adaptive mesh process and the server used to run the simulation ran out of disk space during simulation.

The eigenmode solver with the adaptive mesh refinement option was used to first determine if the correct mode could be supported in the DBR with the waveguide-aperture transition for alumina loss tangent values of 0.002, 0.001 and 0.00005. In order to ensure the simulation completed successfully

Alumina tanδ	f_0 / GHz	S_{21} /dB	Q_0
0.0002	15.800	-1.38	27275
0.0001	15.800	-0.784	48482
0.00005	15.79231	-0.487	74946
0.00002 (no adaptive mesh)	15.818	-0.266	132287

Table 4.5: Simulated resonant frequency, insertion loss and Q_0 with decreasing Alumina loss tangent.

without running out of disk space during the simulation the loss tangent of the alumina plates was dropped to 2×10^{-4}. The manufacturer specified loss tangent of the alumina plates is 2×10^{-5}, so the effect of increasing the loss tangent by a factor of ten is estimated to decrease the Q_0 by a factor of 10,000 to 20,000. After consultation with the manufacturing technicians about the thickness of the aperture, it was decided that a 0.5mm thick aperture could be manufactured and was therefore used in the CST model.

Once the eignemode solver had successfully shown the correct field pattern for the TE_{011} mode for each simulation, the frequency domain solver was used to simulate the S-Parameters of the resonator with varying Alumina loss tangent. As the resonator is symmetrical, only port 1 was excited in order to reduce simulation time and to use less disk space. The tetrahedral mesh was used, and the adaptive meshing option was selected. The initial maximum mesh cell was set to 10 cells per wavelength. The simulated resonant frequency of the TE_{011} modes of the resonator, insertion loss and the calculated Q_0 , obtained from the simulated S_{21}, are shown in table 4.5. As the simulation run where the alumina loss tangent was set to 2×10^{-5} did not complete successfully with the adaptive mesh option selected, it was run again without the adaptive mesh option with the same initial settings as the previous simulations. These simulated parameters are also shown in table 4.5. As expected the Q_0 increases as the value of the loss tangent was decreased. The largest Q_0 was observed when the loss tangent was equal to 2×10^{-5} as per the manufacturer's specification however value of the Q_0 has dropped from the calculated 215,000 from the initial Eigenmode simulation of the cavity without any coupling mechanism, to 121,000.

A further series of simulations were run where the width of the aperture was varied using the parametric sweep option in CST. The model for alumina used a loss tangent of 2×10^{-5} and the adaptive mesh option was not selected, the minimum number of cells per wavelength was set to 11. The

Aperture width/mm	f_0 / GHz	S_{21} /dB	Q_0
0.5	15.818	-0.806	148981
1	15.818	-0.385	137550
1.5	15.818	-0.266	132287
2	15.815	-0.234	118306
2.5	15.816	-0.200	121391

Table 4.6: Simulated resonant frequency, insertion loss and Q_0 where the Alumina loss tangent is set to 2×10^{-5} and the aperture width is varied. The adaptive mesh option was not selected.

width of the aperture was varied from 0.5mm to 2.5mm whilst keeping a constant height of 8mm, the simulated resonant frequency, insertion loss and Q_0 are given in table 4.6. The simulated parameters show that increasing the aperture width decreases the resonant frequency slightly by around 0.01% but there is a large decrease in Q_0 from 148981 to the minimum value of 118306 (approx 19%). The lowest Q_0 is not with the widest aperture however, rather the second widest. There is a slight increase in Q_0 when the width of the aperture increases from 2mm to 2.5 mm though this is only by about 3000, approximately 2.5%. Furthermore, the insertion loss at resonance decreases asymptotically, the rate at which the loss decreases is greater between the smallest three aperture widths and appears to approach a value close to 0.2dB. Further simulations would be required to determine whether there is a limit to the insertion loss at resonance.

The original dimensions of the aperture were selected for manufacture as this gave a high Q_0 and 0.54dB improvement in insertion loss when compared with the smallest aperture. Lerger apertures degraded the Q_0 for minimal improvement in insertion loss.

Manufactured parts and measurements

The central ring of the original DBR was redesigned in Autodesk Inventor to incorporate a removable internal ring that had the aperture cut into it, allowing for an easier replacement of the aperture coupling mechanism without the need for removing the entire central ring. The design also included the waveguide to aperture transition as well as a face with four screw holes to allow for the waveguide launcher section to be attached.

The waveguide launcher consists of a section of waveguide with a short circuit wall at one end. This face has recessed holes cut into it to allow the launcher to be bolted to the centre ring. The probe

used to excite the TE_{01} mode in the waveguide is a length of RG405 coaxial cable that penetrates the broad side of the waveguide. For ease of manufacture and to reduce manufacturing costs, the redesigned central section was manufactured from Aluminium.

As discussed in previous sections the lossy end walls of a microwave cavity determine the Q_0 of a cavity resonator, however in the DBR the alumina plates cause the majority of the EM field to be contained within the central section and away from the end walls. It was thought that the side walls had a small effect on the Q_0 and that aluminium could be used despite its smaller conductivity which could degrade the Q.

The waveguide launcher was modelled in CST and to find the optimum probe position and dimensions. Ultimately, the lowest insertion loss was found when the centre conducting pin of the coax was placed $\lambda/4$ from the short circuit end wall and the length of the centre conductor was 2mm. This is half the width of the short wall of the waveguide, none of the PTFE or outer conductor should enter the waveguide air section.

The central section was designed in two halves as it was not possible to manufacture it in one solid piece of metal. Furthermore there is a small radius of 0.5mm in the corners of the waveguide and in the aperture corners. This is limited by the manufacturing process and the tools available at the School of Physics, Engineering and Technology workshop.

The CST model was changed to include the 0.5mm radius in the corners of the rectangular aperture. The loss tangent of the Alumina model was 0.00002 and adaptive meshing option was not selected. There were 7.9 million tetrahedrons. The insertion loss of the updated resonator was -0.307dB, 0.041dB larger than the model without the rounded corners but the Q_0 increased to 154000. The exploded view of all parts that were manufactured in shown in Figure 4.21, there are alignment pins included. The parts are listed below:

1. Removable central ring with waveguide to aperture transition
2. Centre ring of the cavity that houses the aperture ring
3. Waveguide section with threaded holes for the screws that hold both waveguide pieces together
4. Waveguide section with clearance holes, hole for coax probe and threaded holes to allow clamps for the coax to be attached

5. Top part of coax clamp with clearance holes to attach to the waveguide, threaded holes to allow for screws to attach the bottom part of the clamp to this part and half of the hole for the coax probe

6. Bottom part of coax clamp with clearance holes to attach to the top part of the clamp and half of the hole for the coax probe

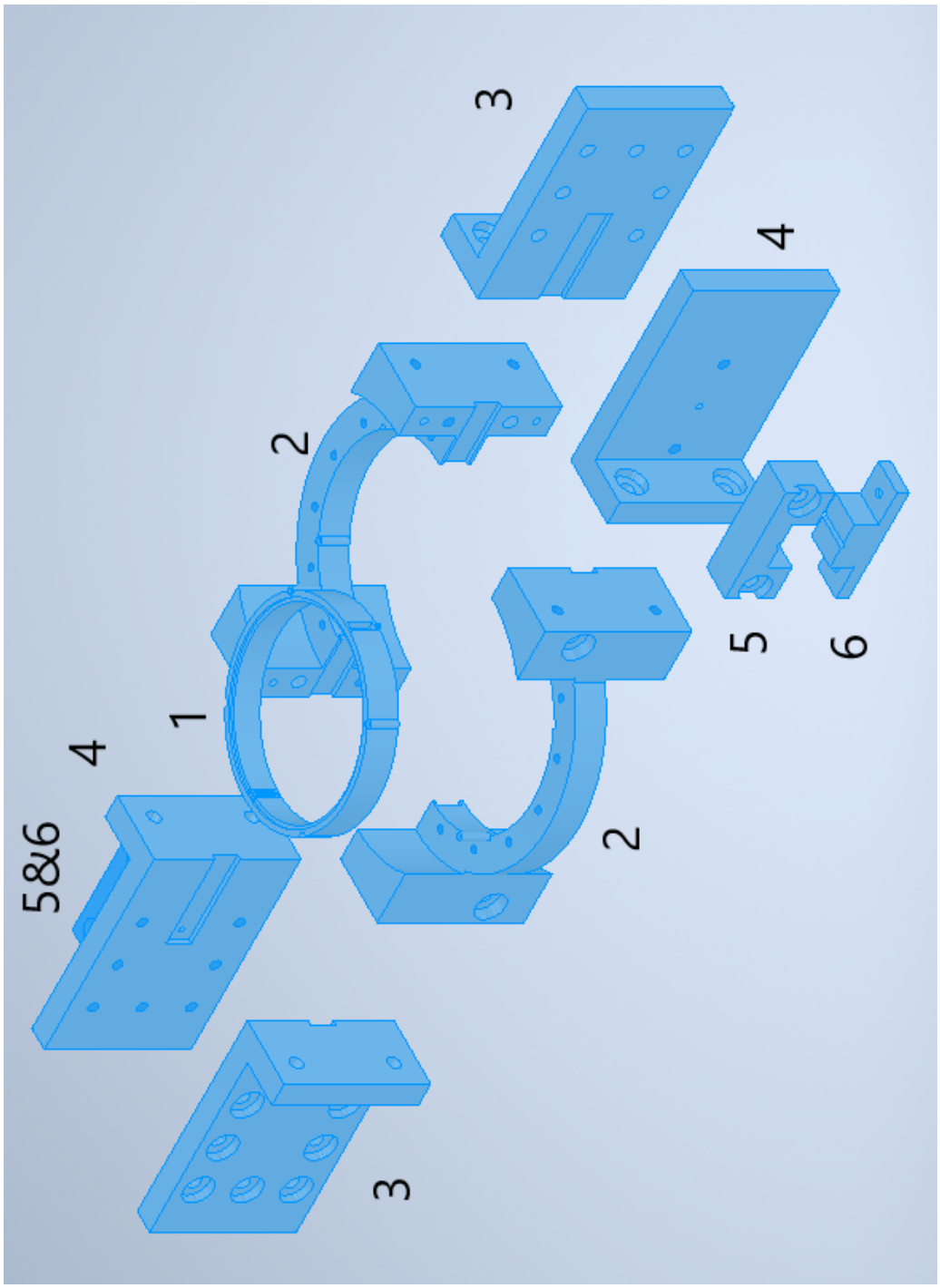


Figure 4.21: Autodesk Inventor assembly file generated from the different parts that were designed to replace the existing central section of the DBR with waveguide to aperture transitions, all parts have been highlighted to emphasise the edges that could be hidden in this view.

Aperture height /mm	Aperture width /mm	Insertion loss at resonance /dB	F_0 /GHz	Q_L	Q_0
8	1.5	11.2	15.918	12860	17790
3	2.367	37.9	15.934	55430	56140
3	2.814	30.6	15.939	87940	90610

Table 4.7: Measured insertion loss at resonance, resonant frequency and Q_l and calculated Q_0 of the DBR with different aperture coupling mechanisms.

Three rings were manufactured, with three different aperture sizes and were measured using the Anritsu network analyser. The measured resonant frequency, insertion loss and Q_l as well as the calculated Q_0 using (4.16) given in table 4.7. The height of the apertures in the first ring is 8mm and the width is 1.5mm, these are the calculated values described previously and used in the simulations. The second set of apertures have heights of 3mm and a width of 2.367mm, calculated using (4.25) where the aperture height is 3mm and the other parameters are kept the same as before. This height was chosen to show how a smaller aperture height affects the measurement of the resonator. There is a limit to how small the aperture height can be before the width becomes larger than the height, in the case for this system, the aperture height will equal the width when it is set to 2.875mm. The third aperture uses the 3mm height as before but the Q_e was set to equal half the Q_0 to try to achieve 6dB insertion loss at resonance.

The measurements made with the first ring shows that the insertion loss is 11.2dB and is significantly higher than the simulated insertion loss at resonant. Furthermore, the measured resonant frequency is 15.918 GHz whereas the simulated resonant frequency is 15.818 GHz. Q_l is 12860, gives an Q_0 of 17790, both of which are significantly smaller than the simulated values and previously measured value for Q_L and subsequent Q_0 calculation using probes to couple to the resonator.

The other two apertures that were measured had a much larger insertion loss at resonance but the measured Q_L and calculated Q_0 were higher in both cases that observed using ring 1. The resonant frequency changes by approximately 5 MHz between the these two measurements are is approximately 20 MHz different from the measured resonant frequency using the first ring.

The highest Q_0 of 90610 was observed with the third aperture design was used. In this case the height was 3mm, and the width was 2.814mm. This width was calculated by setting $Q_e = Q_0$

to achieve 6dB insertion loss. Instead it is observed that the insertion loss at resonance decreases unexpectedly from 37.9dB to 30.6dB.

The loss of the waveguide launchers was measured by placing the two waveguide/coax transition sections back to back and the measured insertion loss is 1.739dB. This contributes to the total insertion loss to the waveguide systems and suggests the actual insertion loss of the resonator itself is 1.739dB lower. If this were the case then the insertion loss of the resonator only is -9.461 when using the first ring. Then, the calculated Q_0 would increase to 19381. As the increase in insertion loss does not contribute to a large enough increase in Q_0 it is thought that it is the aperture design that is the cause of the degradation to Q_0 and the insertion loss at resonance.

4.3 Amplifiers

To sustain oscillation the losses within the feedback loop must be overcome so that the net gain is 1. The output of the oscillator will be over-damped in the case that the loop gain is less than unity or under-damped if the gain is greater than unity. The amplifier in the feedback loop must therefore have sufficient gain to overcome all losses within the loop but not too much to cause the amplifier to be driven hard into saturation which can increase the noise figure of the amplifier and degrade the oscillator phase noise.

SiGe transistors and amplifiers are an ideal choice for use in the feedback loop of ultra-low phase noise oscillators as they have low residual phase noise but, at microwave frequencies such as 16 GHz they offer low output power. (2.59) shows that the phase noise response is inversely proportional to the power available at the input of the resonator and it is therefore necessary to ensure the amplifier can provide high power at the input of the resonator.

GaAs transistors are more suited to high power microwave circuits, but they exhibit flicker noise corners much higher than those of their SiGe counterparts. The low frequency flicker noise is modulated onto the carrier causing high close to carrier high frequency noise observed in GaAs MESFET oscillators. It has been found that the source of low frequency flicker noise is caused by the random carrier-generation-recombination in the gate and source depletion region [9]. It is therefore necessary to try to reduce the $\frac{1}{f}$ noise of a GaAs amplifier using external circuit techniques as the $\frac{1}{f}$ noise is

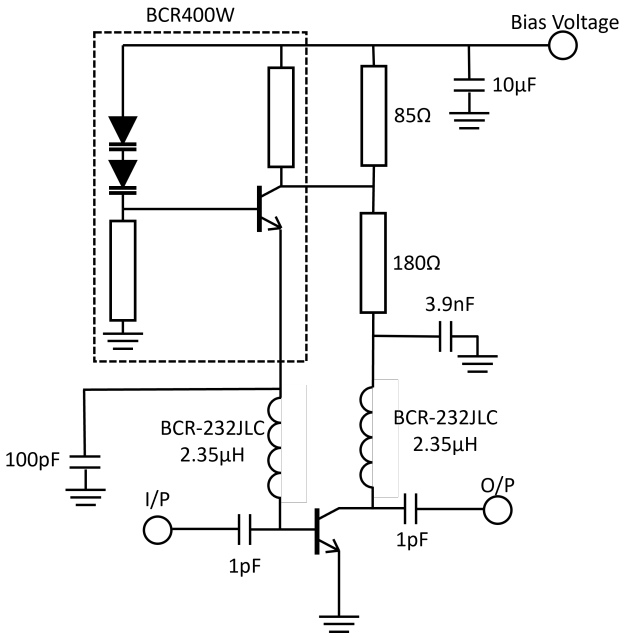


Figure 4.22: BFU730 Transistor amplifier schematic using BCR400W active bias.

intrinsic to the device and degrades oscillator phase noise performance at close to carrier frequencies.

An amplifier with as low noise figure as possible is necessary as the noise figure is the ultimate limit to the oscillator's noise floor. The far from carrier residual phase noise of the amplifier can be calculated using the (2.62), which shows that the noise figure of the amplifier is proportional to the residual phase noise of the amplifier at far from carrier offsets. Three amplifiers have been considered for use in the feedback path of the oscillator, the NXP BFU730F [63], Analog Devices HMC3653 [64] and the Marki APM6849SM [65]. The BFU730 amplifier schematic is depicted in Figure 4.22, the design uses the BCR 400R [66] active bias with 85Ω resistor to provide a collector current of 10mA and a bias voltage of 6V.

The RF isolation was provided by Coilcraft BCR-232JLC conical inductors [67] that provide broadband RF isolation, represented as 2.35µH inductors in the schematic. A 180Ω resistor biases the transistor collector at 3V. The design was assembled on Rogers 4003 0.5mm substrate but the measured gain was 6.227dB, too low for use in this oscillator.

Gerber files for the evaluation boards from the manufacturers for the other two amplifiers were obtained and manufactured in house. The Rogers 4350 [68] substrate with copper thickness of 17µm

Amplifier	Gain /dB	$P_{Out1dBm}$ /dBm	F /dB
Analog Devices HMC3653LP3BE	11.637	13.3	6.14
Marki APM6849SM	9.835	19.6	4.89

Table 4.8: Measured amplifier parameters at 16 GHz from three amplifiers considered suitable for use in a 16 GHz oscillator.

and board thickness of 0.254 mm was used to manufacture the HMC3653 and APM6849SM test boards. The HMC3653 requires a single 5V supply and the Marki APM6849 requires two 6V supplies. The gain, noise figure and 1dB compression point were all measured using the measurement techniques described in Chapter 3 and the results are in table 3.7. The connectors used were Rosenberger SMA connectors with narrow centre conductors [69] as standard SMA centre conductors would be too wide for the 50Ω transmission line at 16 GHz. The gain of the BFU730 is too low for use in the oscillator loop on its own and would have to be cascaded in series with another device to overcome the loop losses. Cascading two of these amplifiers would increase in the noise figure of the feedback elements which degrades the oscillator phase noise measurement. The Marki APM6849SM device offers the highest output power in 1dB gain compression of 19.6dBm as well as a lower noise figure than the HMC3653LP3BE

4.3.1 Parallel Amplifier design

It has been demonstrated by Rubiola and Boudot [41], that a parallel combination of amplifiers not only increases the output power of the whole device but also reduces the flicker noise of the amplifier by a factor m, or $3\log_2(m)$dB, where m is the number of amplifiers in the parallel array (assuming negligible losses and perfect symmetry in the power splitting structure). Rubiola demonstrated this flicker noise reduction in practice using two amplifiers in parallel producing an output with a flicker noise reduction of approx. 2.5dB.

To reduce the flicker noise of the Marki APM6849SM whilst increasing the power available at the output of the amplifier a parallel combination of these devices was investigated starting with the simulation of three different power splitting structures in CST. The aim of these simulations was to estimate the losses of the dividers when the power is split 2, 4, 8 and 16 ways and then combined

using the same structure. These losses will reduce the gain of the amplifier as well as degrade the flicker noise reduction.

The Wilkinson divider and the rat race coupler are power dividers that offer good output port isolation and equally split the input power between two outputs. The main difference is the phase of the outputs, the Wilkinson divider splits the power with 0° phase shift between the output ports but the Rat Race coupler, using the sum and delta ports as outputs, port B as the input and port C terminated in 50Ω, produces outputs 180° out of phase.

The third structure is an integrated planar spatial power divider/combiner [70] that utilises a Klopfenstein taper to transform the impedance of the input line to a scaled value of the input impedance dependant on the number of outputs required. This structure has the advantage of not being restricted to dividing power 2^N ways but great care must be taken to ensure the output arms are designed so that the phase of the signal at the end of each path is the same across all ports. This results in a rather bulky design where the rate of change of phase of the outermost output ports is a factor n times greater than that of the most central port where n is the number of outputs.

Rat race coupler

The 'Rat Race' or 180° hybrid coupler, is comprised of four ports and a central ring. The circumference of the ring is equal to 1.5λ and the four ports are placed on one side of the ring at λ/4 intervals. Figure 4.23 is a schematic of a rat race coupler where the port λ/2 from the input is the isolated port. The remaining ports are the outputs and are in antiphase. The characteristic impedance of the ring is equal to $\sqrt{2} \times Z_0$ whereas the port impedances are all equal to Z_0 for equal power division between the outputs. The LineCalc tool was used in ADS to calculate the widths and lengths for the different sections and a model of a rat race coupler with an ideal 50Ω resistor was created in CST. At 16 GHz and using the Rogers 4350 [68], the width of the 50Ω sections is 0.540mm, $\sqrt{2} \times Z_0 = 70.7\Omega$ sections is 0.284mm. The circumference of the central ring is calculated to be 17.182mm, therefore the radius of the ring is 2.753mm. The time domain solver was used to simulated the model and optimise the dimensions so that the centre of the output pass bands were at 16 GHz and the input power was equally split between the two output ports. After optimisation the radius of the ring was found to be the same, the width of the 50Ω line is 0.553mm and the width of the 70.7Ω section is 0.25mm.

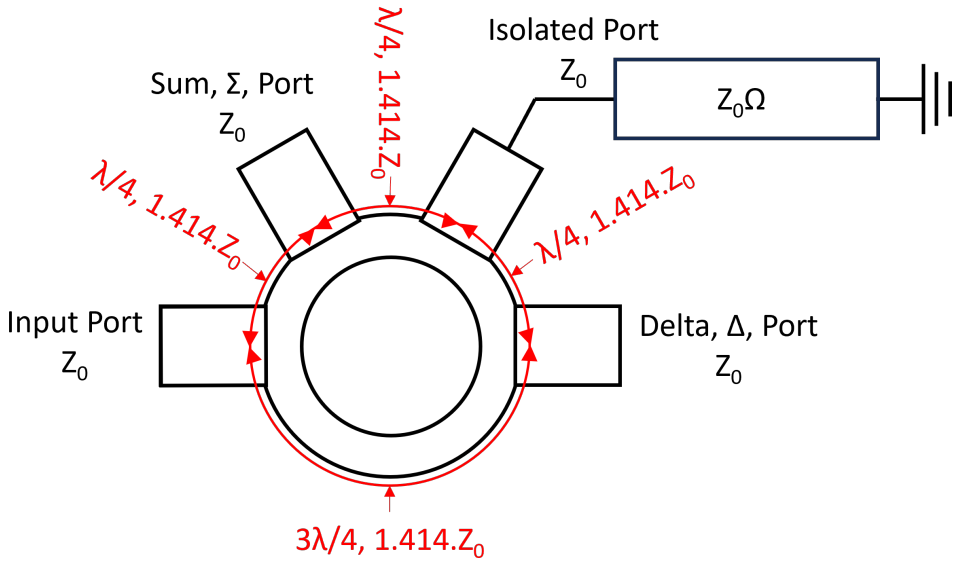


Figure 4.23: 'Rat Race' Coupler schematic for the coupler arranged such that the two output ports provide equal power in antiphase.

Wilkinson divider

A Wilkinson divider uses two quarter wave transformers and a resistor equal to $2 \times Z_0$ to equally split the input power between the two output ports. Unlike the rat race coupler, the phase difference of the output signals is 0°. The quarter wave transformers have an impedance equal to $\sqrt{2} \times Z_0$ and are both connected to the input port at one end. At the other end, a resistor is placed across the transformers to provide the output port isolation and ensure the impedance seen looking into all ports is Z_0. Figure 4.24 is a circuit diagram of the Wilkinson divider. The circuit was modelled and simulated in CST using the time domain solver, the widths of the microstrip used were the same as the rat race coupler model before optimisation. The length of 16 GHz microstrip line for the quarter wave transformers was calculated to be 0.230mm. The gap that the resistor is placed across is equal to the spacing between the pads of a 0402 SMD, a small resistor is necessary at 16 GHz to reduce the parasitic effects introduced by the component. The gap width is 0.5mm.

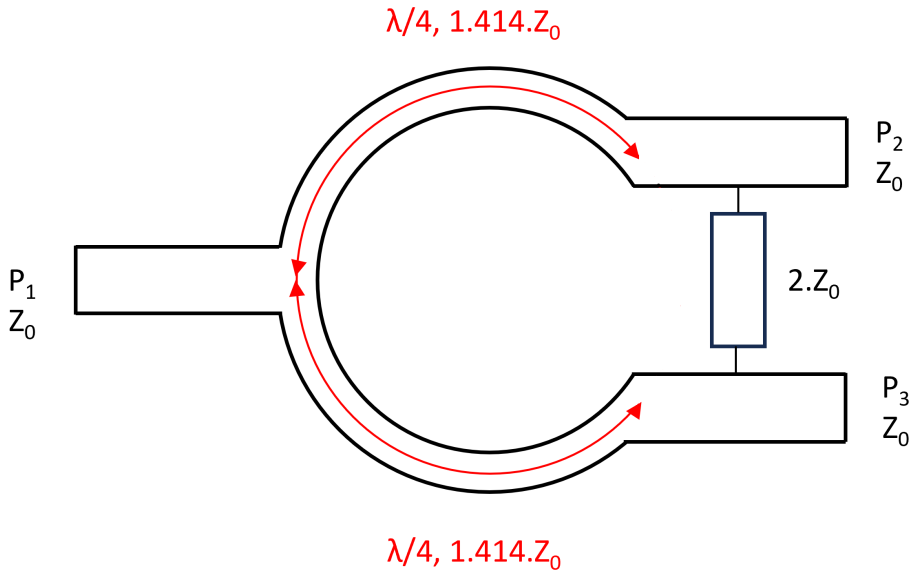


Figure 4.24: Wilkinson divider that equally splits the input power between the two output ports with equal phase of the output signals.

N-Way divider using Klopfenstein taper

The integrated spatial planar power combiner presented in [70], can be used to achieve any number of output ports where the input power is equally split in a much simpler implementation. The design comprises of an input port of impedance Z_0 that is connected to a wide microstrip line via a Dolph-Tchebycheff taper [71]. The impedance of the wide microstrip is equal to $Z_0 \div N$, where N is the number of output ports. The output ports all have characteristic impedance Z_0, and are equally spaced across the wide microstrip line.

The propagating quasi-TEM wave at the input port forms a cylinder wave as the microstrip line begins to widen and the characteristic impedance decreases. The wave is diffracted and according to Huygen's principle, each point now becomes a new source of wavelets. A plane wave can then form due to constructive interference in the oversized section. This design is advantageous as there are no lumped elements that can introduce parasitics into the system.

The taper is a high pass structure and for a specified length of taper, it offers minimum reflection coefficient magnitude in the pass band. The taper is designed using a modified version of the equation developed presented by Klopfenstein [71] that accounts for large impedance transformations between

the input and output sections of the taper, the modified equation is presented in [72] and is shown in (4.27):

$$\ln(Z_0) = \frac{1}{2}\ln(Z_1 Z_2) + \frac{\rho_0}{\cosh(A)}\left\{A^2\varphi(2x/l, A) + U\left(x - \frac{l}{2}\right) + U\left(x + \frac{l}{2}\right) - 1\right\} \tag{4.27}$$

where Z_0 is the impedance in Ω at a point from the centre of the taper, Z_1 is the impedance of the input transmission line, L_2 is the impedance of the output transmission line, ρ_0 is the maximum return loss of the taper, cosh(A) is the ratio of maximum return loss and maximum reflection coefficient, U is the unit step function and $\varphi(2x/l, A)$ is defined as follows:

$$\varphi(2x/l, A) = \int_0^{2x/l} \frac{I_1(A\sqrt{1-y^2})}{A\sqrt{1-y^2}}\,dy \tag{4.28}$$

Where I_n is the first kind of modified Bessel function of first order. The impedance of the taper can be calculated anywhere along the taper for a given length, impedance transformation and maximum reflection coefficient. A convenient calculator is available for download from Microwaves101 [73], this was used in the design of the taper for the power divider to be used at 16 GHz. The design was built up from 21 discrete impedance calculations which were then used to calculate a series of microstrip lines of equal lengths to built up to form the real taper.

A maximum reflection coefficient of -30dB was used to transform from 50Ω to 25Ω (to allow for a power divider of a factor of 2 to be designed) with a minimum operating frequency of 16 GHz. The calculated impedances at 21 discrete points along the taper are plotted in table 4.9. These impedances are then used to calculate the width of the microstrip required for each section of microstrip in the series. ADS LineCalc tool was used to calculate the width of a microstrip built on 0.25mm Rogers 4350 as before. A two way power divider was then designed incorporating the taper and the 50Ω input and output ports. The output ports were equally spaced across the wide microstrip line and the length of the wider, lower impedance microstrip line was optimised for lowest insertion loss. The CST model of the design is shown in Figure 4.25 and the time domain solver was used to simulate its S-Parameters. S_{21} and S_{11} are plotted in Figure 4.26.

The insertion loss from the input to both output ports is 3.452dB, and the return loss is 19.731dB at 16 GHz. The return loss has increased by 10dB from the specified -30dB at 16 GHz in the design stage. The -30dB spec was for the tapered section only, the model used in simulation included two

Position X	X/mm	Impedance	Calculated Microstrip Width /mm
-1	-2.475	25.761	0.565
-0.9	-2.228	26.185	0.580
-0.8	-1.980	26.725	0.600
-0.7	-1.733	27.382	0.624
-0.6	-1.485	28.161	0.652
-0.5	-1.238	29.065	0.685
-0.4	-0.990	30.096	0.723
-0.3	-0.743	31.249	0.765
-0.2	-0.495	32.516	0.812
-0.1	-0.248	33.886	0.862
0	0	35.355	0.917
0.1	0.248	36.888	0.974
0.2	0.495	38.442	1.032
0.3	0.743	40.001	1.091
0.4	0.990	41.534	1.150
0.5	1.238	43.006	1.204
0.6	1.485	44.388	1.257
0.7	1.733	45.651	1.304
0.8	1.980	46.762	1.347
0.9	2.228	47.728	1.384
1	2.475	48.529	1.414

Table 4.9: Calculated Dolph-Tchebycheff impedances at distance X mm from the centre of the taper. The impedances are then converted to a microstrip track width at 16 GHz using 0.25 mm Rogers 4350 substrate.

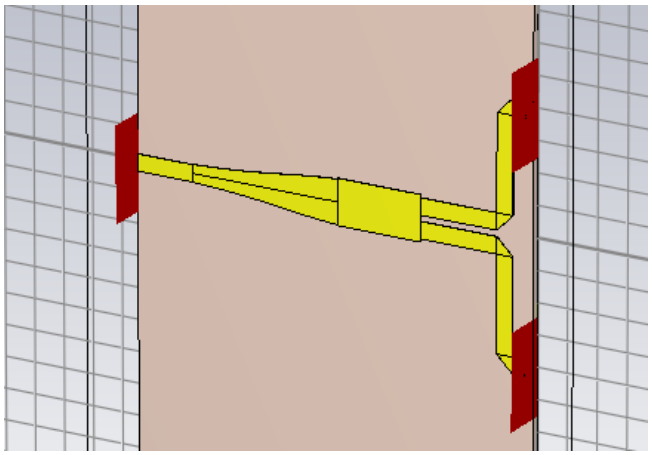


Figure 4.25: CST model of the 2 Way splitter incorporating the Dolph-Tchebycheff taper designed for use above 16 GHz on Rogers 4350 substrate with maximum permissible reflection coefficient of -30dB. All ports present 50Ω impedance.

output arms that present 50Ω impedance to the 25Ω microstrip line. The large transition in impedance appears to have caused some power to be reflected and therefore reducing the return loss at 16 GHz.

4.3.2 Simulated couplers placed back to back

2 Way power splitting and combining

Models of all three couplers were placed back to back to split and then recombine the input power. These simulations assume that the input and output impedances of the amplifiers would be 50Ω and are useful in giving an indication of the loss introduced by the structures that would therefore decrease the amplifier gain. The modelled splitting and combining structures are shown in Figure 4.27 where the input and output ports are modelled as waveguide ports. The time domain solver with a mesh cell density of 30 mesh cells per wavelength was used in the simulations to simulate the S-Parameters. The simulated insertion loss at 16 GHz for all three structures is similar, 0.66dB for the spatial planar combiner structure, 0.58dB for the rat race structure and 0.53dB for the Wilkinson structure. The rat race coupler structure has sharper roll off at frequencies away from 16 GHz however the maximum insertion loss is only 3dB across the simulated bandwidth. The Wilkinson structure and integrated spatial planar structure exhibit less variation in insertion loss and would therefore allow a wider range of resonant frequencies to oscillate. The simulated return loss of the three structures is plotted

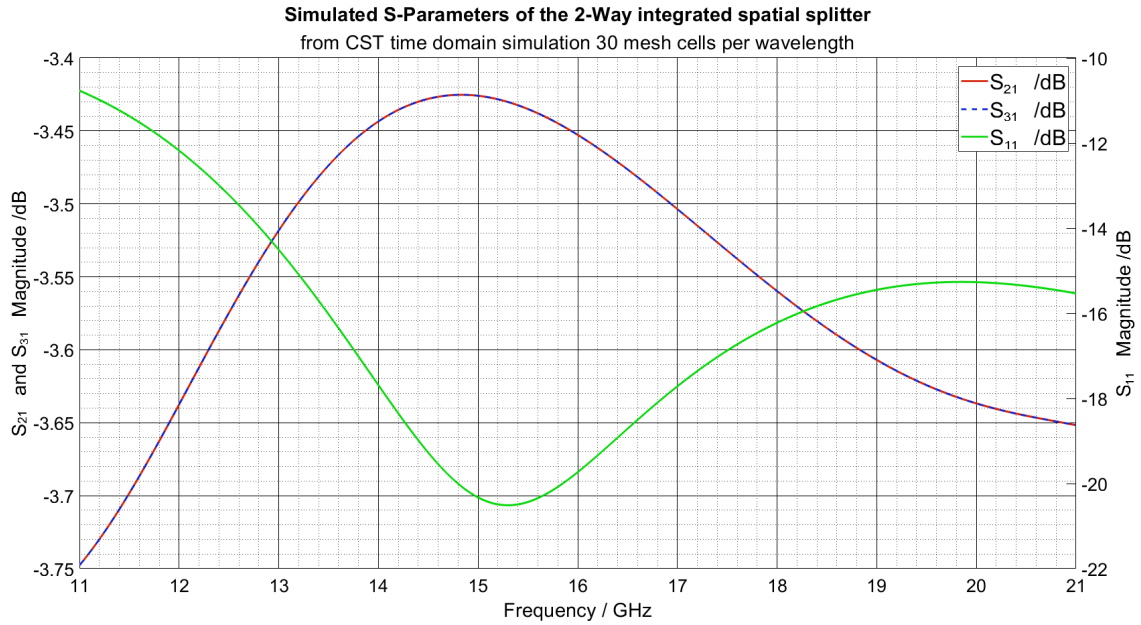
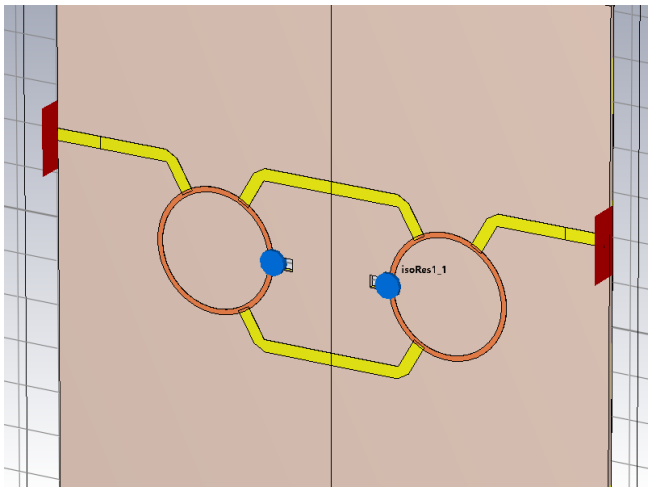
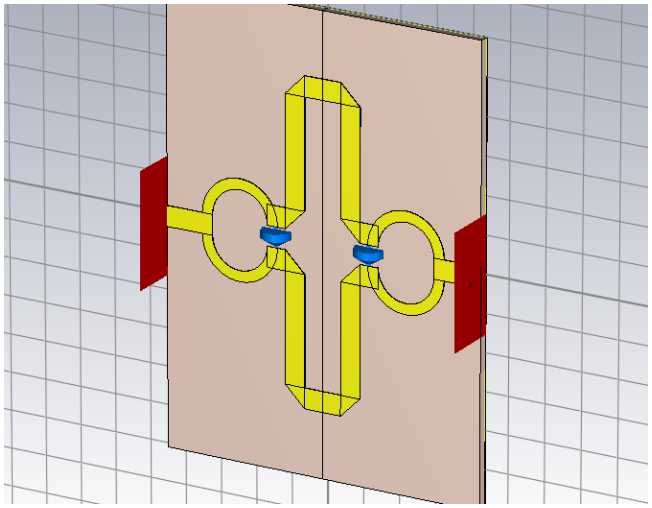


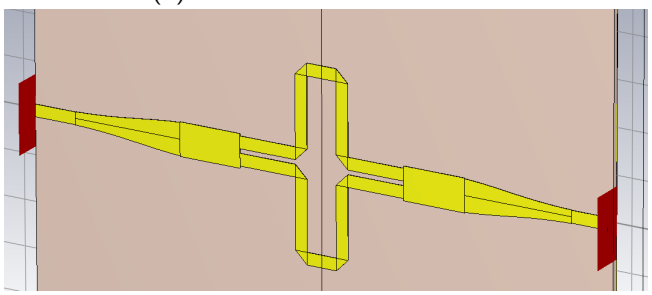
Figure 4.26: Simulated S-Parameters of the modelled circuit. The return loss of the whole structure is 10dB less than the expected return loss of the taper, this can be attributed to the sharp transition from 25Ω microstrip to 2 50Ω microstrip lines. The large impedance change has caused some of the propagating signal to reflect.



(a) Rat race structure.



(b) Wilkinson divider structure.



(c) Integrated spatial combiner structure.

Figure 4.27: 3 back to back models used to simulate the S-Parameters of the power splitting and combining structures.

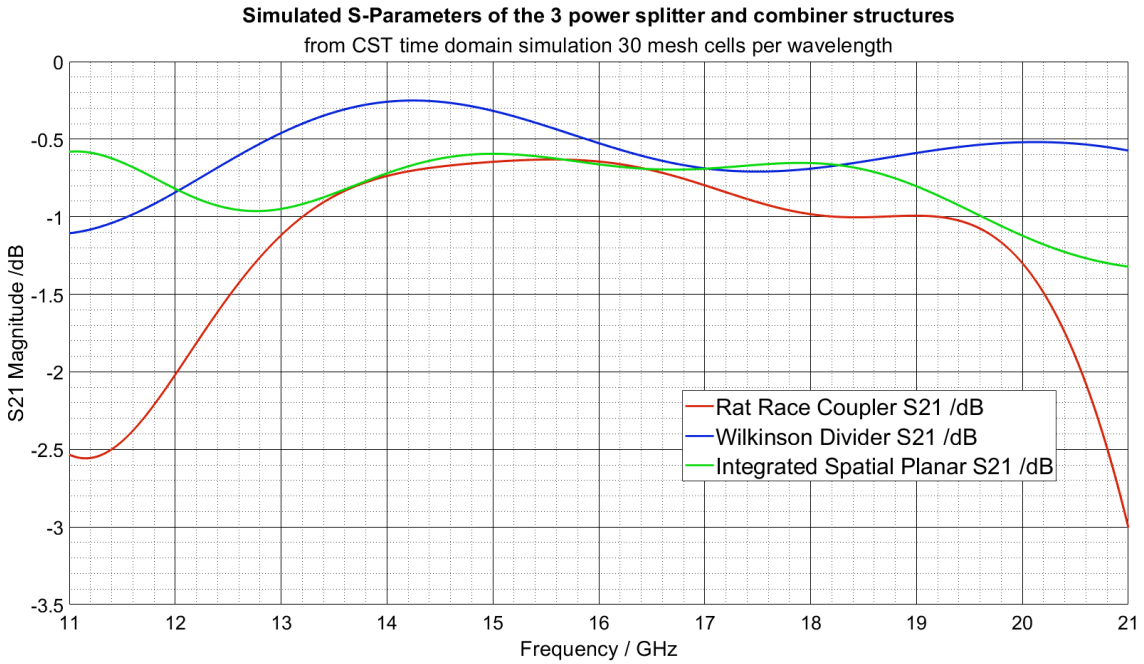


Figure 4.28: Simulated insertion loss of the three 2-way power splitting and combining structures.

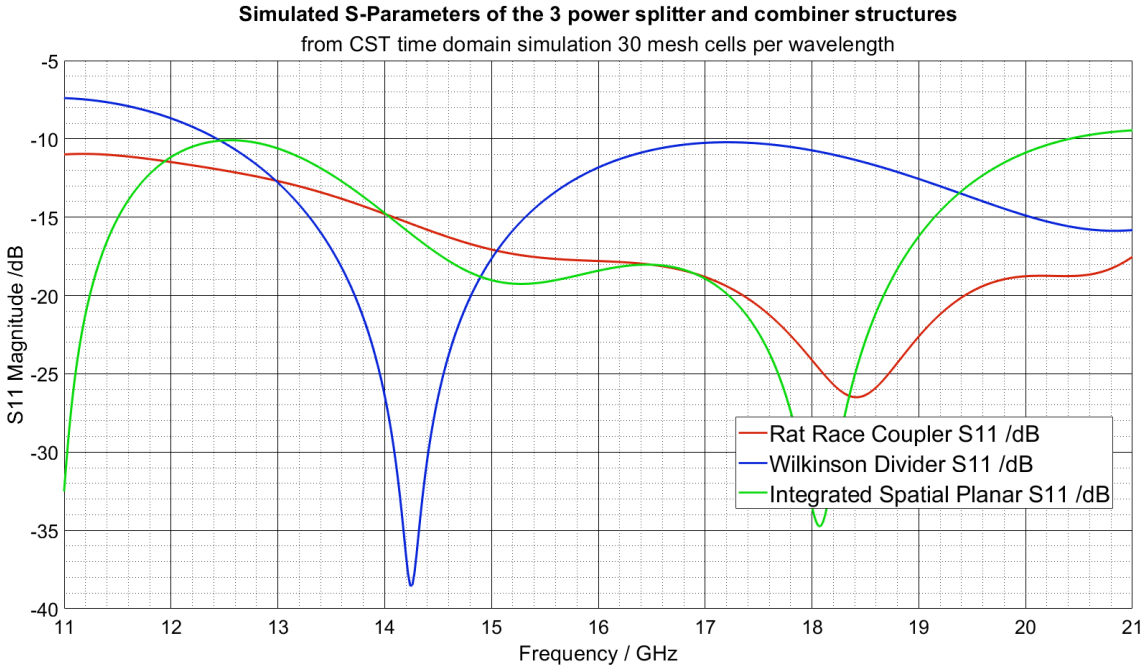


Figure 4.29: Simulated return loss of the three 2-way power splitting and combining structures.

in Figure 4.29. At 16 GHz, the Wilkinson structure demonstrates the smallest return loss and is approximately 5dB lower than the rat race structure. There is a sharp trough at 14.2 GHz however, this suggests further optimisation to the design could be possible to move the frequency where the trough is at its maximum value.

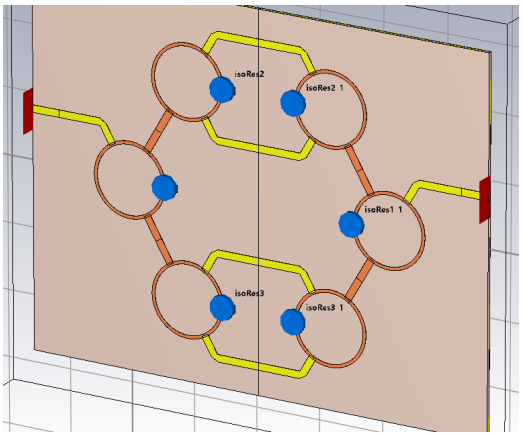
The three structures are inherently narrow band because the designs all use impedance transformations that are centred at 16 GHz. However, the return loss is always greater than 10dB from 12.5 GHz to 20.4 GHz and less than $\frac{1}{10}$th of the input power will be reflected across this frequency range. These simulations do not include the amplifiers and assume that the input and output impedance of the devices is 50Ω.

4, 8 and 16 Way power splitting and combining

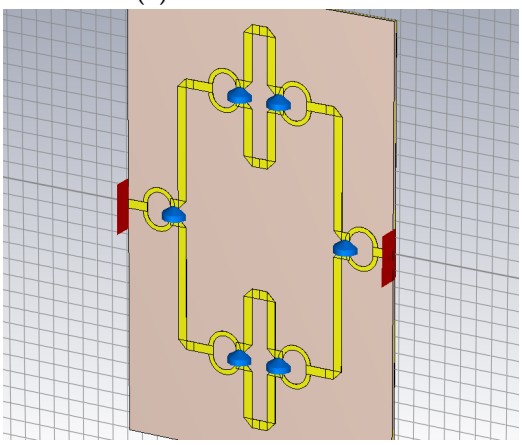
In order to divide the power equally between four, eight and sixteen devices, the corporate structures can be extended by introducing a duplicate stage at the two outputs. The microstrip lines used as the output ports on the 2 way dividers were extended such that two power dividers could be introduced and the input power would be divided between four ports. Furthermore, the length of the microstrip lines was calculated to ensure the device PCB footprint could be housed between the four output ports.

To achieve equal power split between this many amplifiers, the integrated spatial planar divider had to be redesigned, transforming from 50Ω at the input to 12.5Ω, 6.25Ω and 3.125Ω so that the 50Ω output ports could be equally spaced along the wide, lower impedance microstrip line. The design process was the same as described in section 4.3.1 except for the smaller impedances used at the output of the taper. The length of the output arms of the spatial planar combiner had to be varied firstly to ensure the amplifier PCB footprint could fit within the ports and secondly to ensure the phase between the output ports was an integer multiple of 360°. The propagating wave fronts in the combining stage must all reach wide section of microstrip in the combiner in phase and constructively interfere with one another to recombine as much of the incident power as possible, reducing the insertion loss.

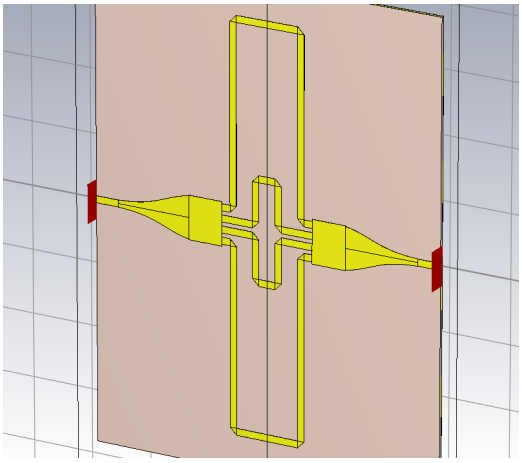
Large lengths of microstrip line were added to the two outside ports to ensure all four ports are in phase. This adds to the complexity of the design and would require greater precision in manufacturing as the phase slope of the longer microstrip lines gets steeper as the length of the line increases. There



(a) Rat race structure.



(b) Wilkinson divider structure.



(c) Integrated spatial combiner structure.

Figure 4.30: The 3 4-Way power splitting and dividing models used to simulate the S-Parameters of the power splitting and combining structures.

is less margin of error at the frequency of interest for all ports signals at the combining stage being in phase.

The structures were once again simulated using the time domain solver in CST. The models used in the CST time domain simulations are depicted in Figure 4.30 and the simulated insertion loss of the three structures are plotted in Figure 4.31. The integrated spatial planar structure is the most narrow band with a sharp roll off in insertion loss at around 14 and 17.2 GHz. This could be potentially useful in the oscillator should unwanted resonant modes near the desired frequency of 16 GHz occur as this structure would act as a band pass filter and therefore increase the oscillator loop loss at frequencies outside of this band.

At 16 GHz the insertion loss of the Wilkinson divider introduces the greatest loss of 1.49dB. The integrated spatial combiner introduces 0.865dB and the rat race structure 0.967dB. Therefore there is a difference of 0.625dB between the three designs. These simulations suggest that the integrated spatial planar structure is best suited to splitting the input power between four amplifiers and then recombining their output power.

The design process for the three power splitting and combining structures was repeated to allow for 8 and 16 amplifiers to be connected in parallel and the insertion loss of these structures was simulated in CST.

4.3.3 Manufactured straight through boards

The models created in CST were used to create the PCB layouts in ADS. The metal layer in CST for each coupler was exported to ADS Layout. The three couplers were manufactured in order to measure the 3 Port device S-Parameters, these PCBs were used to measured the output port isolation, return loss and the insertion loss and phase shift of the input to output ports. Three PCBs with the couplers placed back to back were also manufactured so that the total insertion loss of the combiners could be measured. An image of the three back to back circuit boards used for measurements is shown in Figure 4.32, the Rogers 4350 substrate used for the amplifier modules was used here and is used for all subsequent PCBs.

2 splitter/combiners as well as 2 way splitters were manufactured and measured to make a comparison with the simulated values for insertion loss, return loss, and output port isolation. The measured

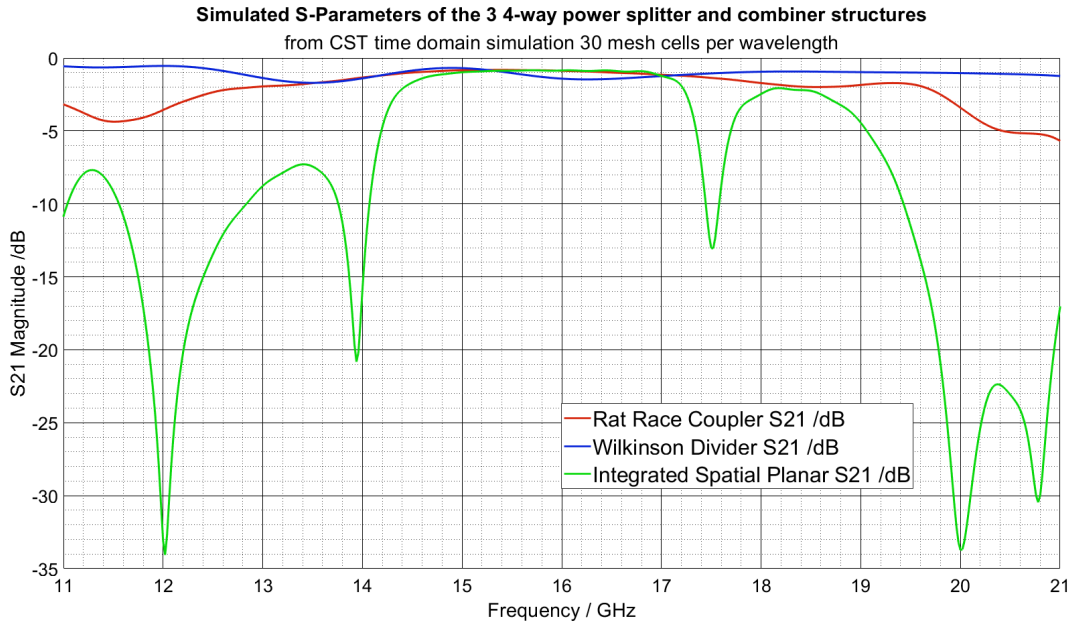


Figure 4.31: Simulated S_{21} for the 3 types of splitter/combiners where the power is divided between four ports before recombining through a mirror of the power dividers. The length of microstrip used at the output ports of the splitting stage are determined by the Marki APM 6849SM PCB footprint for all designs. Additional lengths of microstrip were added to the integrated spatial planar design to ensure the phase of the four output signals from the splitting stage were in phase.

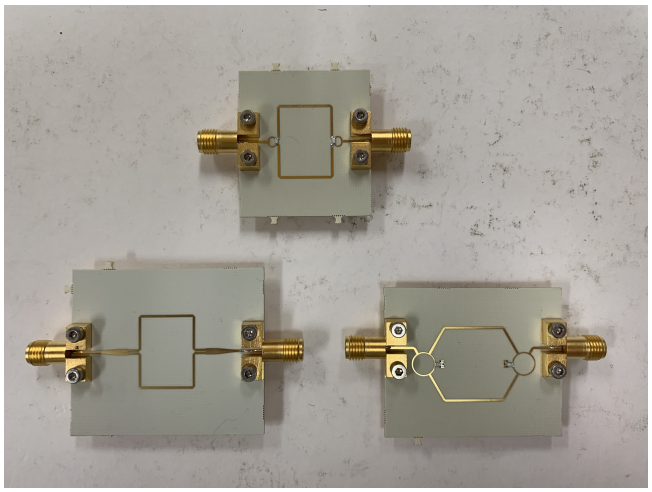


Figure 4.32: Back-to-back (clockwise from top), Wilkinson divider, Rat Race Coupler and Integrated planar spatial power combiner.

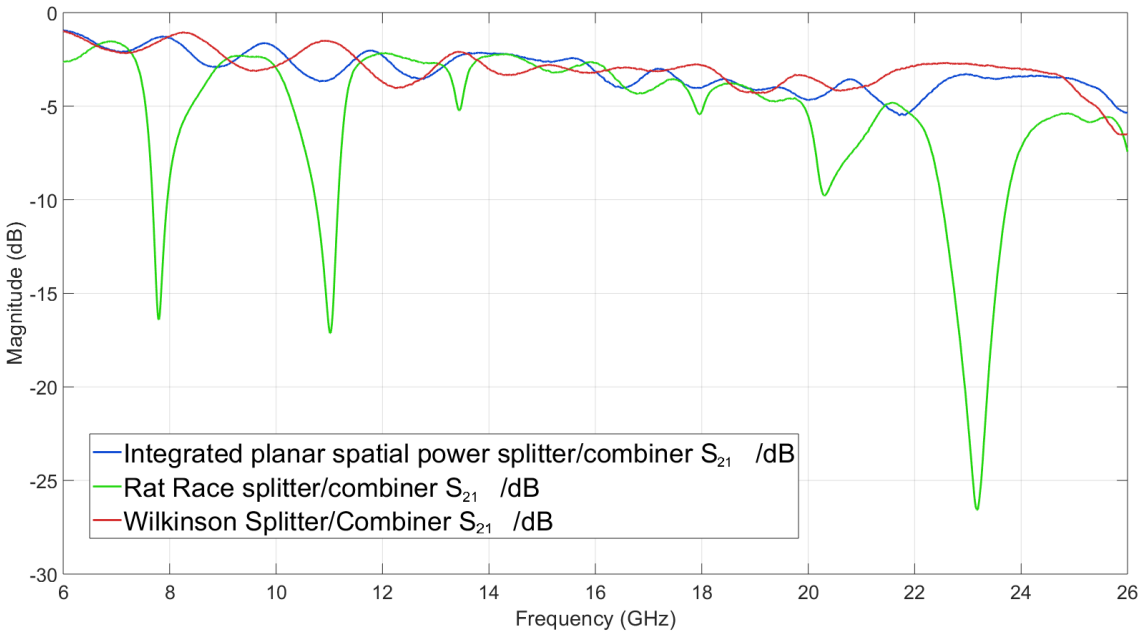


Figure 4.33: Measured insertion loss of three back-to-back power dividing structure.

results were approximately 2dB worse at 16 GHz and there was unwanted ripple in the passband of all structures. This is demonstrated in Figures 4.33 and 4.34 for all two way splitter/combiner structures. The models used in CST did not include a model for the SMA connectors and the resistors in the Rat Race and Wilkinson dividers were modelled as ideal. The ripple was observed in the spatial planar structure however, which did not include any lumped elements. Passband ripple is caused by mismatch in impedance resulting in reflections, the model used in CST to simulate the couplers did not include a model of the connector or the taper that was included in the PCB layout. The only feature common to all PCBs that was not modelled was the SMA connector. It was decided that a model of the SMA connector should be included in the CST simulations.

4.3.4 Ripple in the passband investigation

To simplify this investigation a straight through test board was designed and modelled in CST and then manufactured. The straight through board was made up from a combination of the input and output grounded coplanar waveguide transmission lines that were used on the Marki APM6849SM test board using. The measurements for insertion loss and return loss of the CPWG through board are

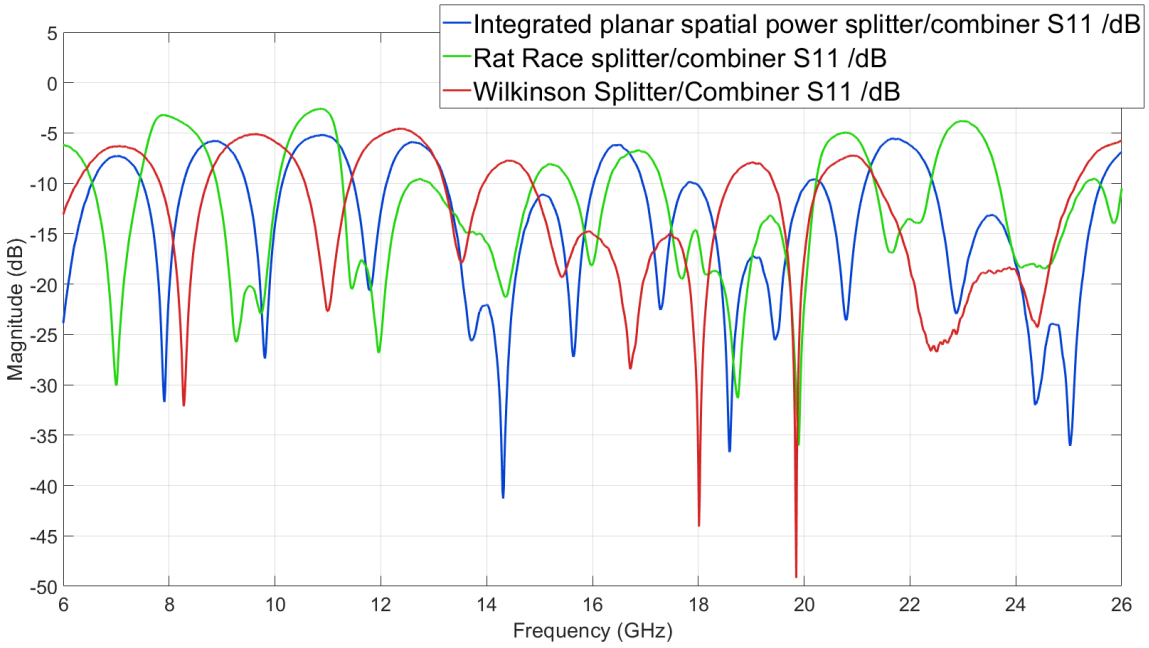


Figure 4.34: Measured return loss of three back-to-back power dividing structure.

presented in Figure 4.35. There is significant discrepancy between the two boards that were designed to be identical except, one board included the taper that was taken directly from the Marki Evaluation board Gerber file. The other extended the CPWG to the edge of the board.

There is a small increase in insertion loss up to 14 GHz on the straight through test board with no taper, after which the loss rapidly increases before decreasing at around 17 GHz. The second appears to show the insertion loss decreasing with increasing frequency with ripple of magnitude 3dB at its worst case. The ripple period is 4GHz.

Assuming the connectors are identical between the two test boards, it was thought that the taper and solder joints were cause of the ripple. The length of the test board is 22.92mm, approximately $\lambda/2$, of the ripple frequency wavelength observed in test board 2. Therefore a standing wave can form between the input and output connectors at a frequency of around 4 GHz which is modulates the trace for S_{21}. At 16 GHz, however, the loss in the version without a taper is still significant which suggests that the connectors are also introducing additional loss.

The connectors were selected because of their low cost and their narrow centre conductors, other

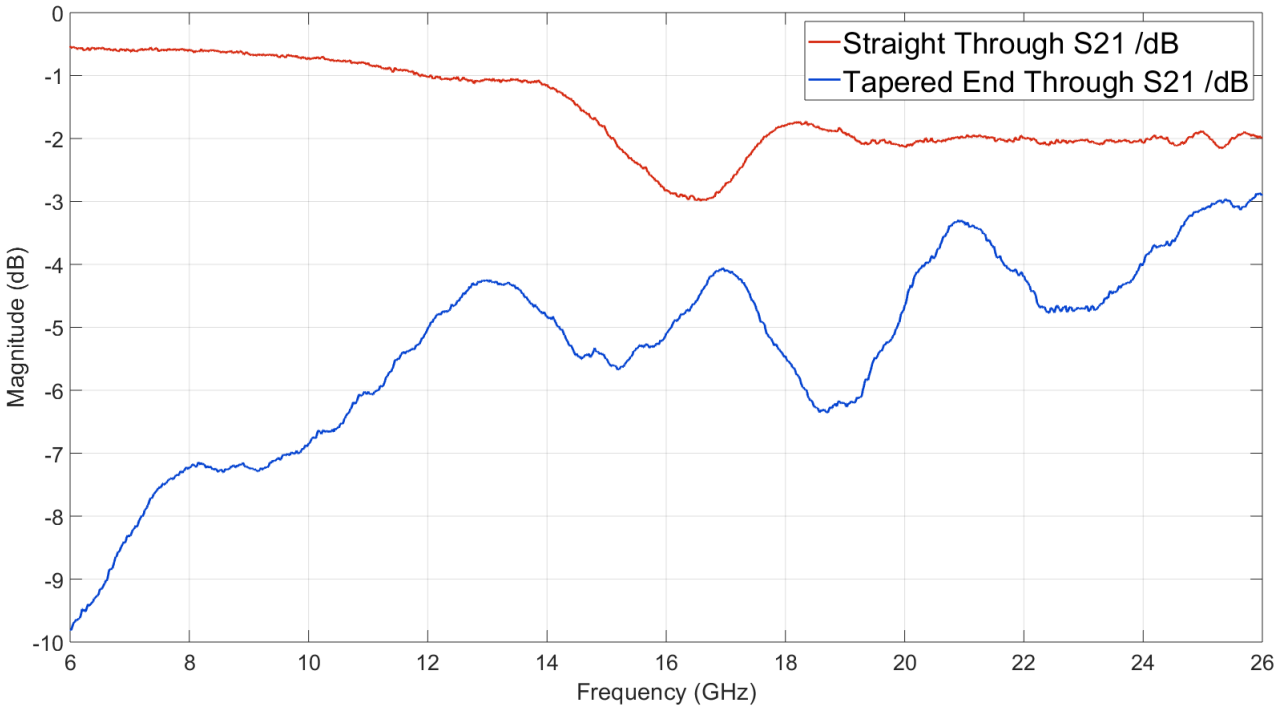


Figure 4.35: CPWG Through test board measurements.

SMAs have centre conductors that would be larger than the track width. They are specified to work up to 18 GHz however from these plots it is clear that the addition of these connectors and how they connect to the CPWG line, affects the performance above 14 GHz.

A CST model of the CPWG through board was created initial simulations showed that without the connector model and measuring just the S-Parameters of the through board, the insertion loss increases with frequency. The simulation was run over a broad frequency range and at the maximum frequency of 26 GHz, the insertion loss is approximately 0.9dB. At 16 GHz the insertion loss is 0.8dB, it is important to note that there is no ripple in the simulated S_{21} when the taper is not present but there is small ripple in the simulation when the taper is present. Plots of S_{21} from this simulation are shown in Figure 4.36 as well as a screenshot of the model used. This suggests that the ripple is caused by the addition of the connectors and the solder joint, an improved model was created using the same CPWG through board but included a model for the Rosenberger Connector. A spare connector was cut in half and the central conductor was measured. The centre pin had a step in the middle so this was accounted for in the model. It was impossible to measure the dimensions of the

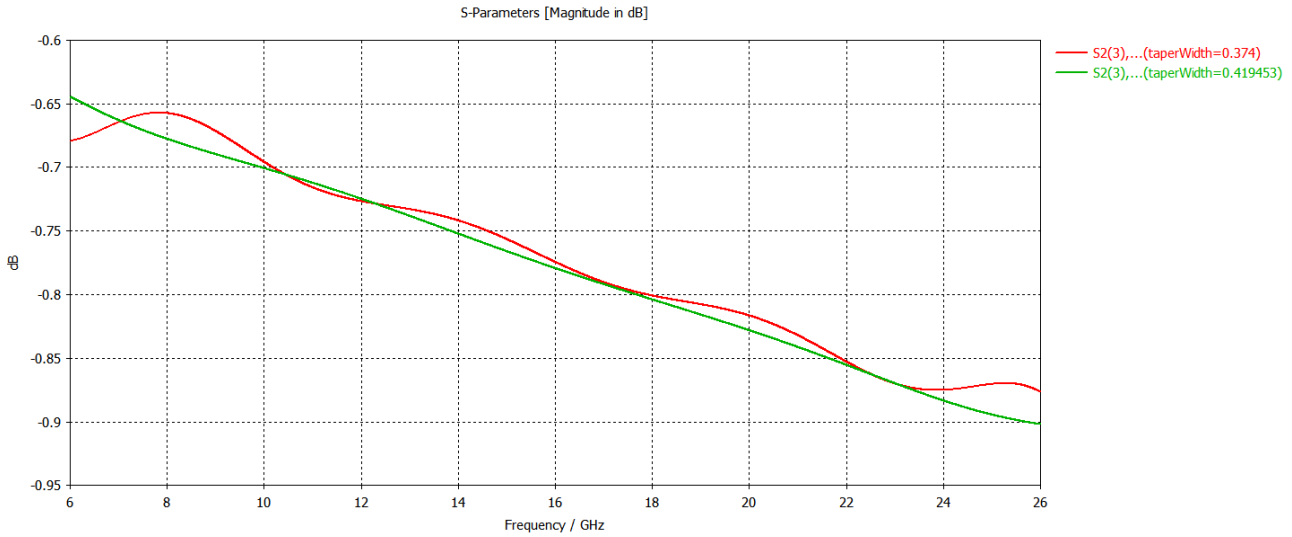


Figure 4.36: CST Simulated S_{21} varying the width of the taper between the designed taper value and taking the CPWG to the end of the board.

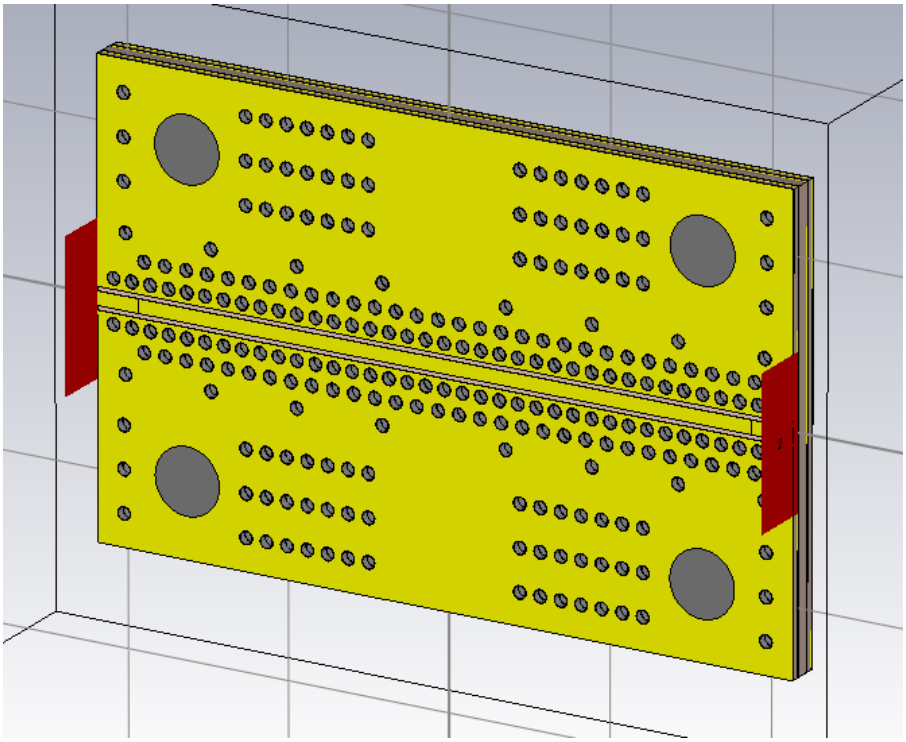


Figure 4.37: CST model of the straight through board with varying taper width.

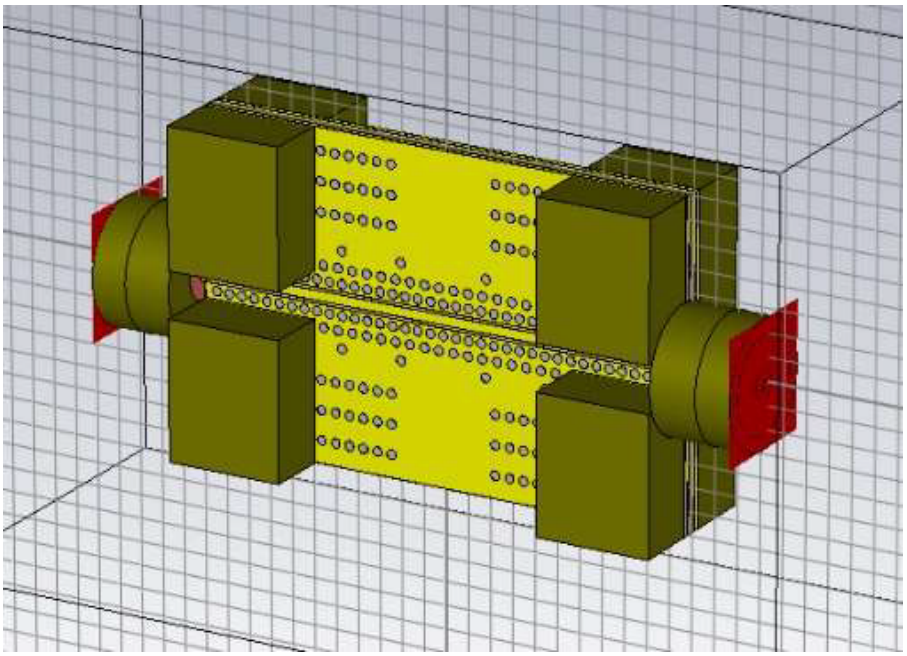


Figure 4.38: CST model of the through board including Rosenberger connector model.

jack end of the connector so this was not included in the model. Figure 4.38 shows the model of the CPWG through board with the Rosenberger Connector Model and Figure 4.39 is the simulated insertion loss of the test through board with the Rosenberger SMA model. It is clear that the Rosenberger connector is too lossy at 16 GHz and the taper used at the end of the board was causing the impedance mismatch between the connector and the board that resulted in the ripple observed across the simulated frequency range. The WithWave end launch 2.92mm connector [74] was selected for use. This connector has an air core rather than PTFE and the datasheet suggests stable operation up to 40 GHz. Simulating this component was more difficult as a spare connector was unavailable to cut in half and measure the diameter of the centre conductor. WithWave do however provide a very detailed layout for mounting the connector to the Rogers 4350 and a demo board is available. In absence of an accurate simulation, the demo board was obtained and S-Parameters were measured. The length of the WithWave Demo boards is 25.46mm, slightly longer than the Rosenberger test board but, there is approximately 1.4dB improvement in insertion loss at 16 GHz when compared with the straight through test board using the Rosenberger connectors. A test board with two microstrip lines of equal length to the WithWave demo board was produced, one to allow for the WithWave 2.92mm

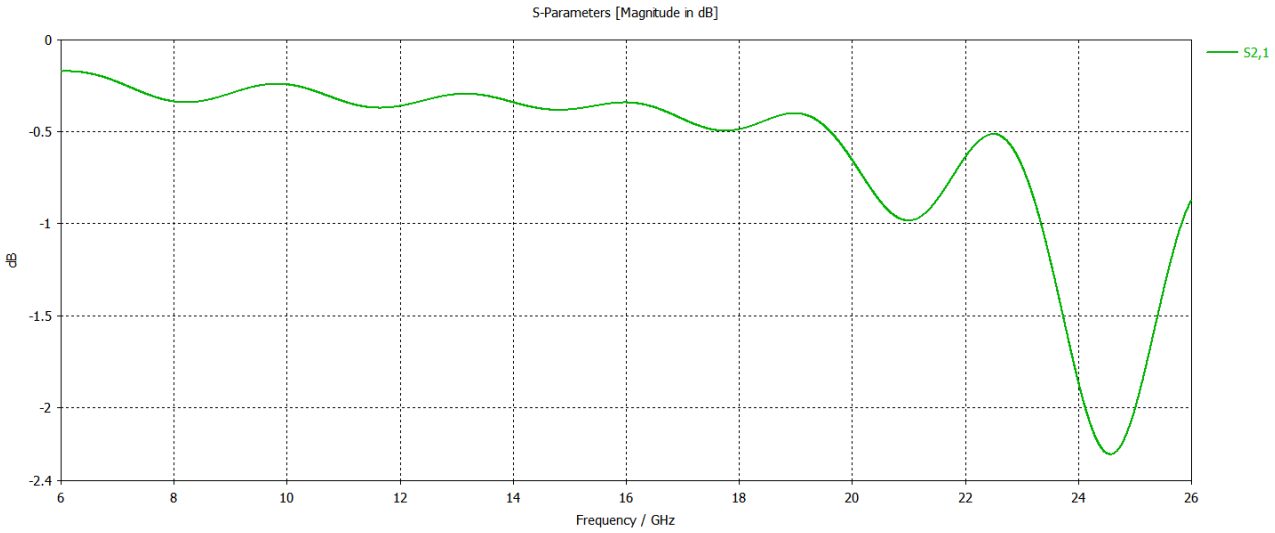


Figure 4.39: Simulated insertion loss of the through board with the Rosenberger SMA connector model.

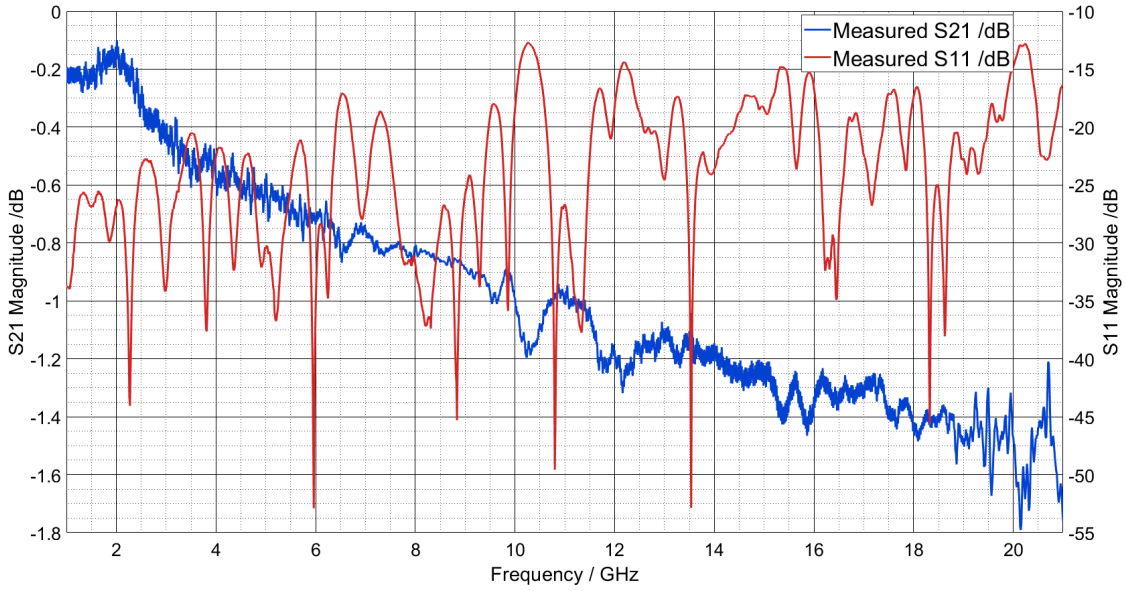


Figure 4.40: Measured insertion and return loss of the demo board obtained from WithWave.

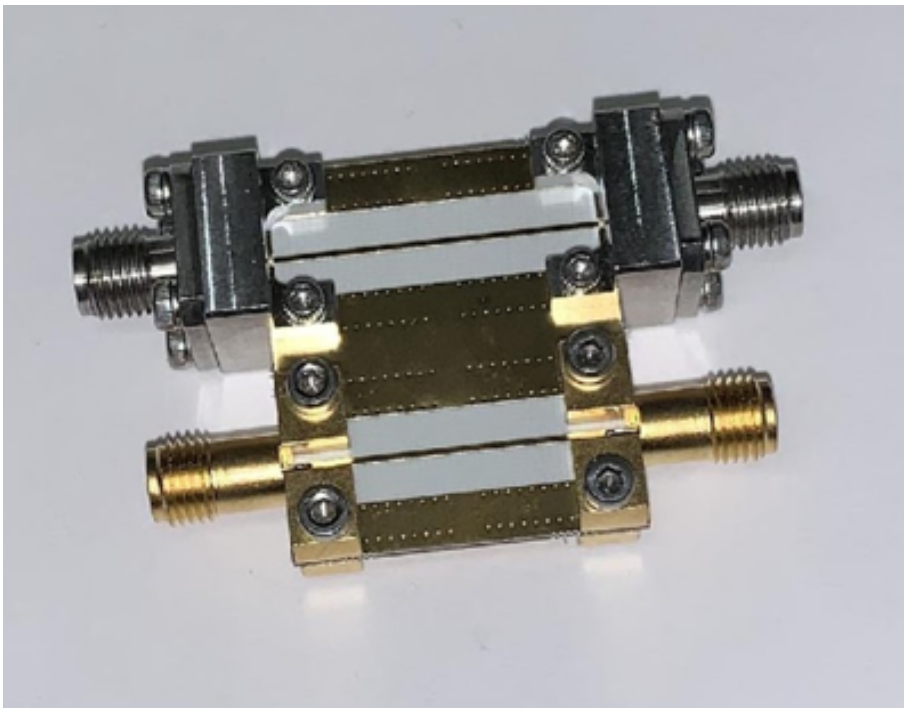


Figure 4.41: Image of the microstrip test boards with both the air core WithWave 2.92mm connector (top) and the PTFE core Rosenberger SMA connector (bottom).

connectors to be mounted and the other designed for mounting the Rosenberger SMA connectors. Both lengths of microstrip have tapers at each end, the line connected to the WithWave connectors used the suggested taper provided by the manufacturer for the Rogers 4350 substrate and the line connected to the Rosenberger SMA connectors used the same taper as the previous straight through test board used with Rosenberger SMA connectors.

The test board with both connectors mounted on the same board is shown in Figure 4.41 and plots of the measured S_{21} and S_{11} for both boards are in Figure 4.42. There is clear improvement across the whole frequency range, the loss overall is reduced and the ripple magnitude is also greatly reduced. At 16 GHz the loss using the WithWave connectors is -1.30dB compared with -2.36dB when using Rosenberger Connectors and the return loss at 16 GHz also improves by around 5dB. These experiments have shown that the Rosenberger connectors are too lossy at 16 GHz and the taper used to connect them causes ripple in the pass band. The WithWave connectors reduce the ripple and are less lossy. It is therefore more suitable to use the WithWave connectors when making measurements

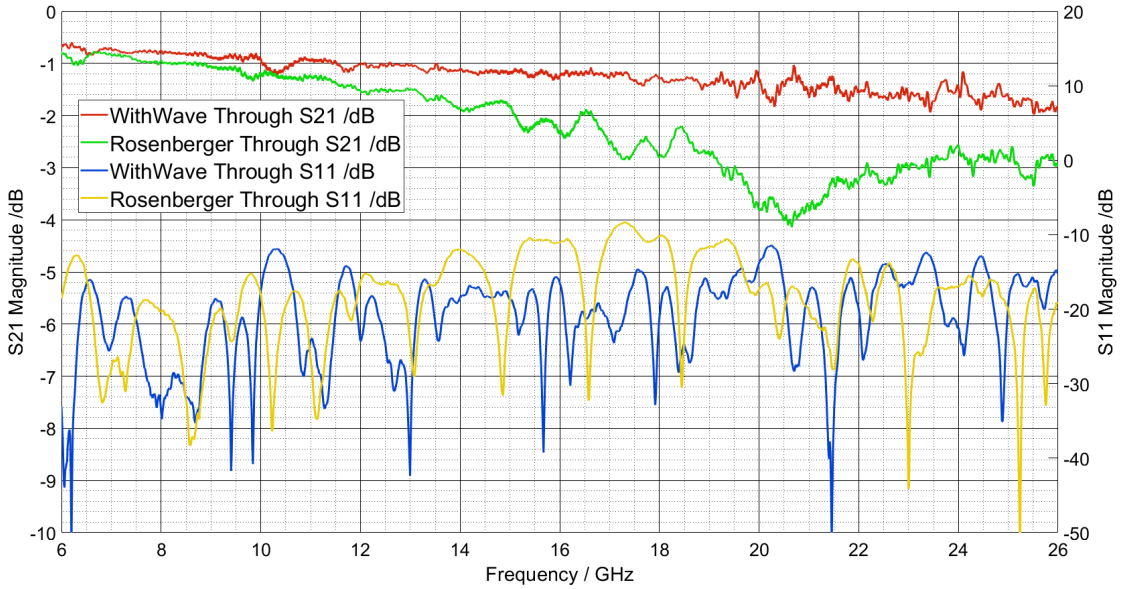


Figure 4.42: Measured insertion loss and return loss of the same straight through piece of microstrip with the two different connectors.

Marki APM6849 Test Board	Gain @ 16 GHz /dB	Noise Figure @ 16 GHz	P1dB @ 16 GHz /dBm
Rosenberger SMA	9.33	4.96	19.4
WithWave 2.92mm	9.58	4.89	19.6

Table 4.10: Gain, NF and P1dB at 16 GHz for the two amplifier modules using the Rosenberger SMA connectors with the narrow centre conductor and the WithWave 2.92mm connectors.

at 16 GHz. Measurements were made with similar board but using CPWG. The loss on the microstrip version was less than that of the CPWG versions and as all other circuits are microstrip, it was decided that microstrip should be used for all future designs. The original power splitter/combiner test boards were redesigned to incorporate the WithWave connectors as well as the Marki Amplifier test board. S-Parameters were measured for all of the boards so that a comparison could be made between them. Figure 4.43 is a plot of S_{21} and S_{11} for the two amplifier test modules with the two different connectors. There is a slight improvement in gain and a slight degradation in return loss at 16 GHz and there is still ripple present though the magnitude of this ripple has been reduced. This suggests there is still an impedance mismatch somewhere on the microstrip line.

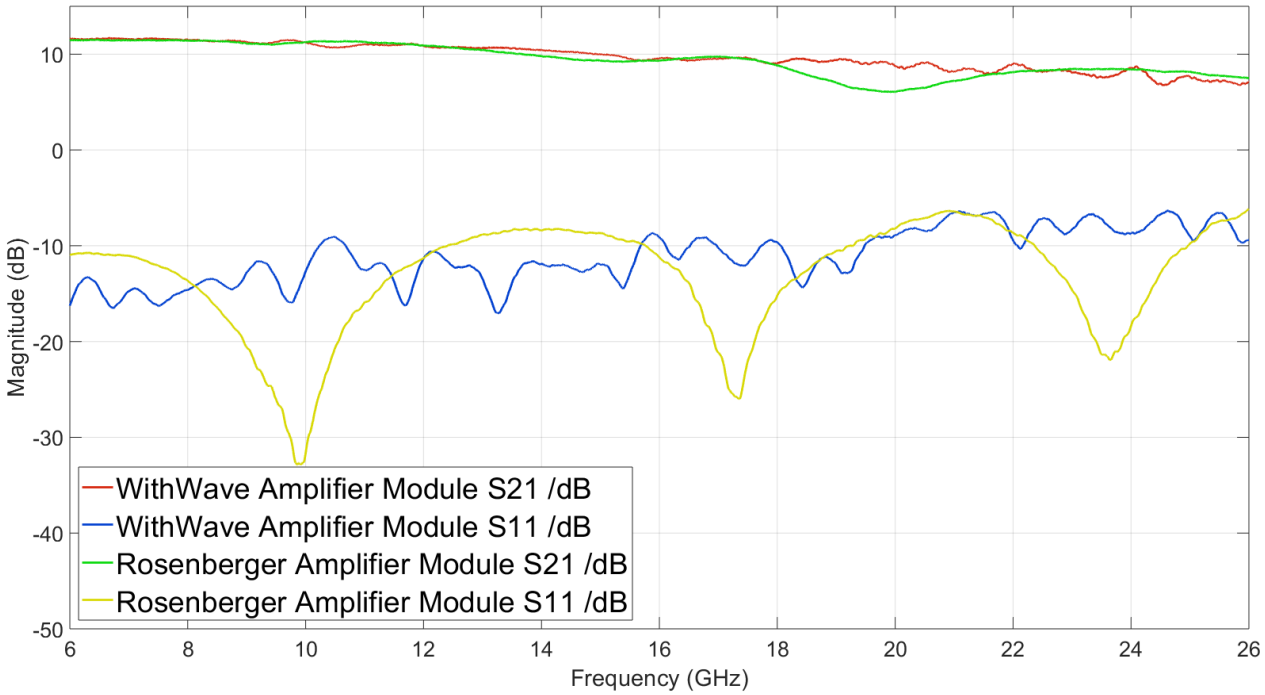


Figure 4.43: Measured S_{21} and S_{11} for both amplifier modules with the two different connectors.

Noise figure and 1dB compression point measurements were also made in the same way as described in Chapter 3, these measurements are shown in table 4.10 with the measurements from the previous microstrip amplifier module.

4.3.5 2 Way Splitting and combining circuits with WithWave connectors

The PCB layouts were updated to include the suggest landing pattern for the WithWave 2.92mm connectors and were manufactured. An image of the three PCBs with the updated landing pattern for the WithWave connectors is shown in Figure 4.44. The insertion loss of the three structures was measured and are plotted in Figure 4.45, to aid with the comparison to the simulated insertion loss using CST, Figure 4.28 is also shown here in Figure 4.46. Firstly, the introduction of the WithWave connectors has reduced the amplitude of ripple found in the previous measurement, Figure 4.33, across all three circuits. The ripple is still present but its maximum amplitude is now less than 1dB from 13-19 GHz whereas the maximum amplitude of the ripple was previously 2dB for all three structures. The general shape of all three plots matches the simulation except there is additional loss at all measured

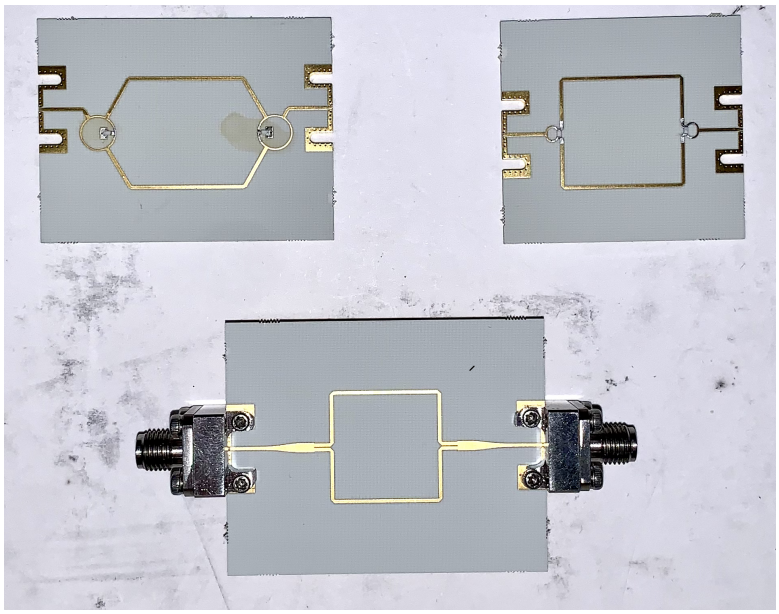


Figure 4.44: Updated PCBs including the landing pattern for the WithWave connectors.

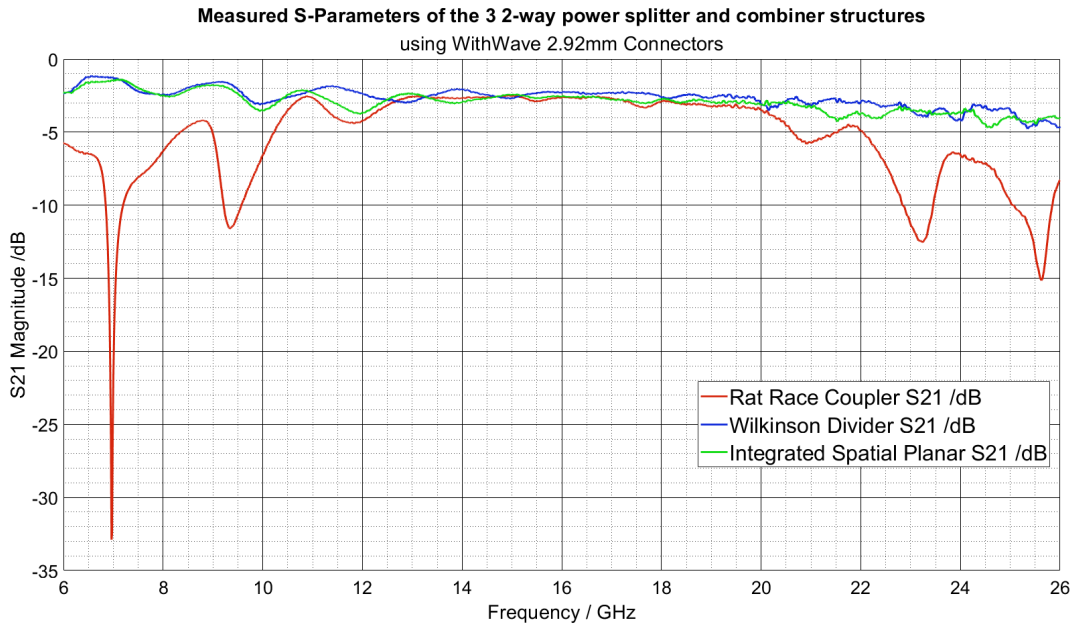


Figure 4.45: Measured insertion loss of the 3 power and splitter combiner structures with the WithWave connectors.

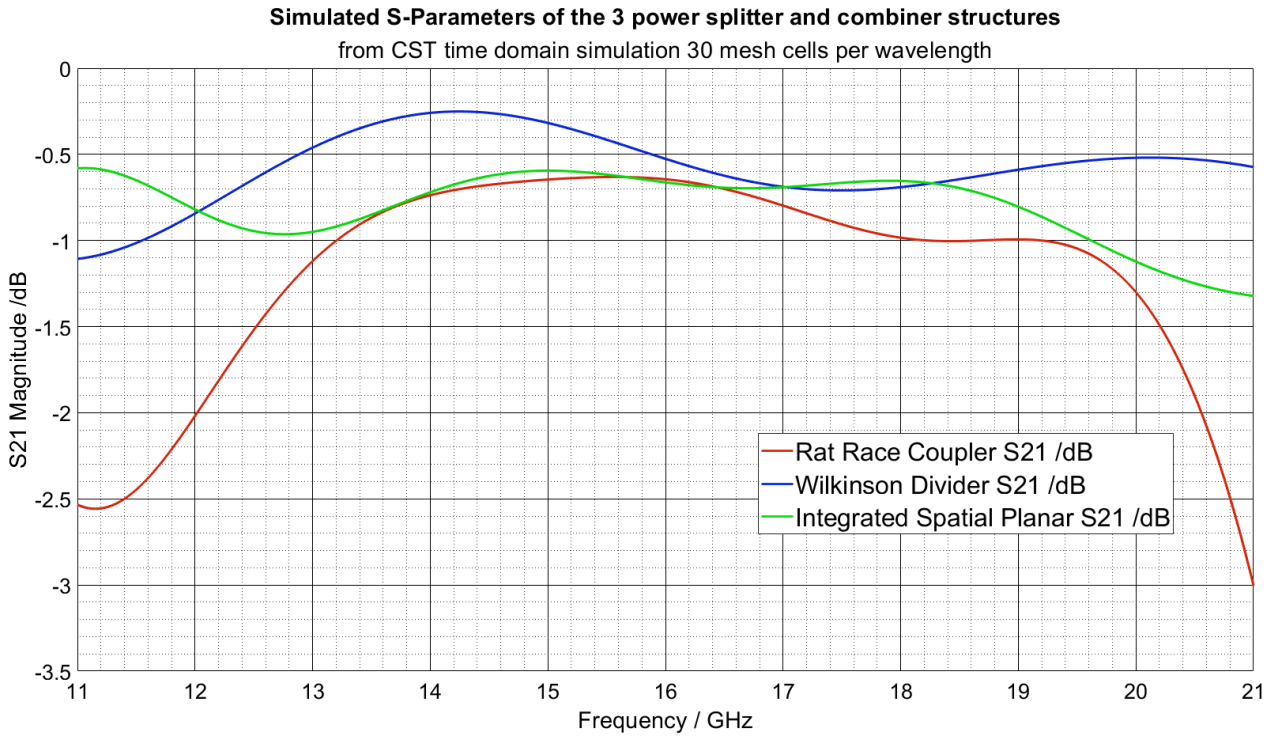


Figure 4.46: Simulated insertion loss of the three 2-way power splitting and combining structures.

frequencies due to the introduction of the connectors. At 16 GHz the measured insertion loss of the rat race structure is 2.59dB, for the Wilkinson structure it is 2.21dB and for the spatial planar structure it is 2.60dB giving a maximum variation in insertion loss of 0.39dB. The rat race structure exhibits a narrower bandwidth centred at 16 GHz than the other two structures, something that is also observed in simulation.

4.3.6 4 Way splitting and combining measurements

Test boards containing the three different power dividers splitting the input power four ways before recombining were manufactured to measure the insertion loss of the structures without the amplifiers present. An image of the three four way splitter combiner structures is shown in Figure 4.47 and Figure 4.48 is a plot of the measured insertion loss of the three manufactured circuits.

The insertion losses measured at 16 GHz are very similar at around 2.6dB. As the WithWave connector losses are estimated to be 0.25dB each, then the gain of the parallel amplifier will be

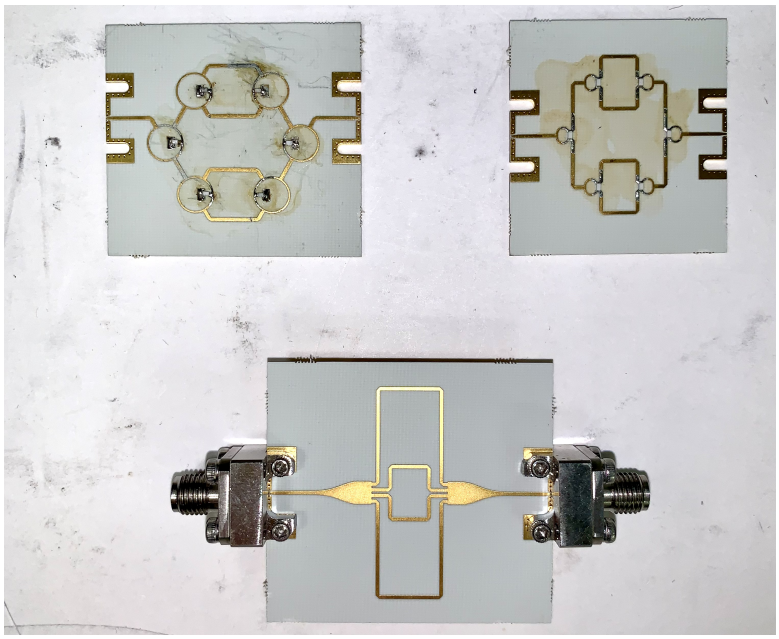


Figure 4.47: 4 Way power splitter and combiner networks with WithWave connectors. Clockwise from the top left is the Rat Race structure, the Wilkinson divider structure and the integrated spatial planar combiner structure.

reduced by around 2dB for this 4 way parallel combination of amplifier. The Rat Race structure offers the broadest passband without significant increases in insertion loss close to 16 GHz, both the planar structure and the Wilkinson Divider structure have increases in loss around 14-15 GHz.

4.3.7 Parallel Amplifier Measurements

The rat race couplers were selected to be used for the parallel combination of amplifiers. For 2 and 4 amplifiers in parallel the variation in insertion loss was very small so any of the three structures could have been used. The Wilkinson structure was not used because it has the broadest passband bandwidth, this is potentially useful should the resonator be required to change resonant frequency. However, a narrower passband is preferred in this instance, as the cavity has many spurious modes that could lead to oscillation at the wrong frequency.

The rat race design is preferred over the integrated spatial planar structure as the design does not include such large impedance transformations nor does it have to add additional lengths of microstrip line at each output arm in the splitting and at the input to the combining stages. The simulated

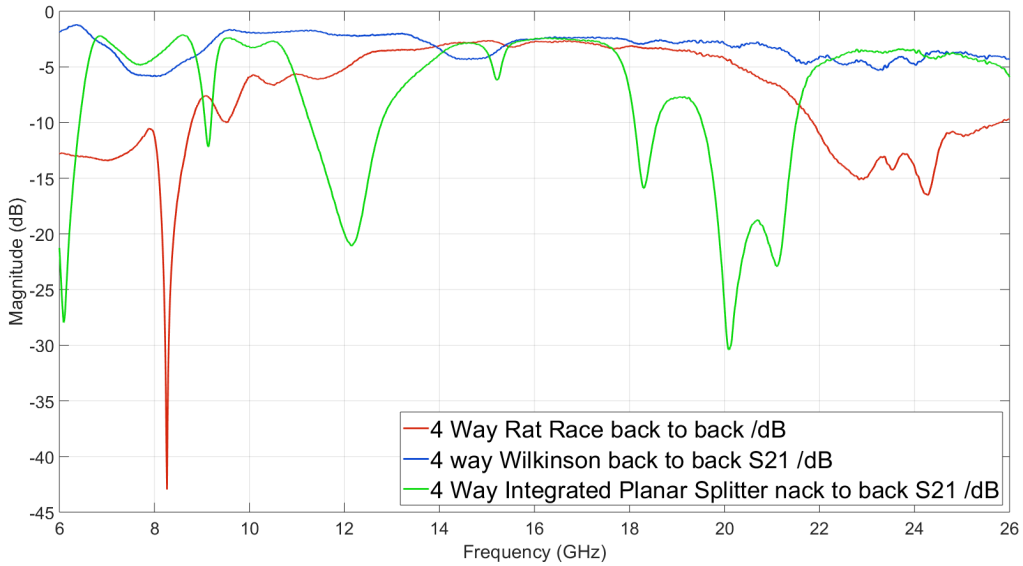


Figure 4.48: Comparison of $S_{21}$for the 3 types of splitter/combiners where the power is divided between four ports before recombining through a mirror of the power dividers.

8 and 16 way spatial planar splitters quickly became very large and the rate of change of phase at the outermost ports was very sharp which could lead to problems in the recombining of the incident power. Any discrepancies between the length of the microstrip at each port would therefore result in an increase in the associated insertion loss of the structure and therefore decrease the overall gain.

It is important to note that the connector type was changed from the WithWave 2.92mm to a different 2.92mm connector manufactured by Johnson-Cinch Connectivity [75] at this stage. The WithWave connectors were never soldered onto any of the PCBs as it is possible to use pressure mount to make the measurements. This suited the early measurement stages when multiple measurements of multiple PCBs were made (including phase shifters and couplers that are described in the next sections and the impedance transformation networks discussed in a previous section). Eventually the connectors began to wear through the repeated installation and removal. The newer connectors are designed to be soldered onto the PCB so were used for the parallel amplifier circuit measurements. All measurements were made with 6V to both the power and bias connections on all amplifiers. An image of the 2 and 4 devices in parallel connected by rat race couplers is shown in Figure 4.49. S-Parameters were measured using the Anritsu network analyser, S_{21} and S_{11} are plotted in figures figs. 4.50 and 4.51 as well as the S-Parameters from the single stage amplifier PCB with the new 2.92mm connectors

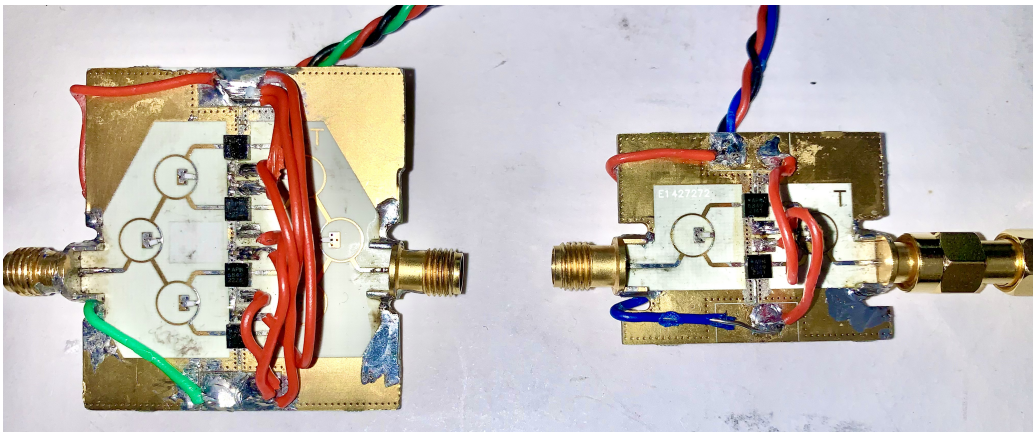


Figure 4.49: Image of the parallel amplifiers with four (left) and two (right) devices and the Johnson-Cinch 2.92mm connectors.

soldered on. As expected from the increasing loss observed by adding more splitting and combining stages in simulation and measurement, the amplifier gain decreases with increasing number of stages. The single stage amplifier gain was measured to be 9.97dB, the measured gain for two in parallel is 8.35dB and 7.41dB for four in parallel. The measured gain of the four amplifiers in parallel agrees with the sum of the gain of the single amplifier and the losses of the power splitting and combining structures as the measured gain is 2.56dB less than that of the single stage amplifier.

The measured gain at 16 GHz of the amplifier with two Marki APM6849SM amplifiers in parallel is 0.84dB less than that of the single stage. The measured insertion loss of the two way rat race structure is without any amplifiers was -2.59dB. It is unclear as to why this difference has arisen however the expected trend of decreasing gain with increasing number of devices is followed which suggests that the measurements made for the two way power splitting and dividing structures without the amplifiers are inaccurate. This could be due to the WithWave connectors being improperly placed onto the PCBs.

The noise figure, NF, and output power in 1dB gain compression, P1dB, was measured for both amplifiers and the results of these measurements are displayed in table 4.11 as well as the gain of both amplifiers. The measurements made for the single amplifier are also included to aid in comparison. The output power in 1dB gain compression increases with increasing number of parallel amplifier, though at a much slower rate than expected. In theory, the the increase in P_{1dBm} is 3dB for every

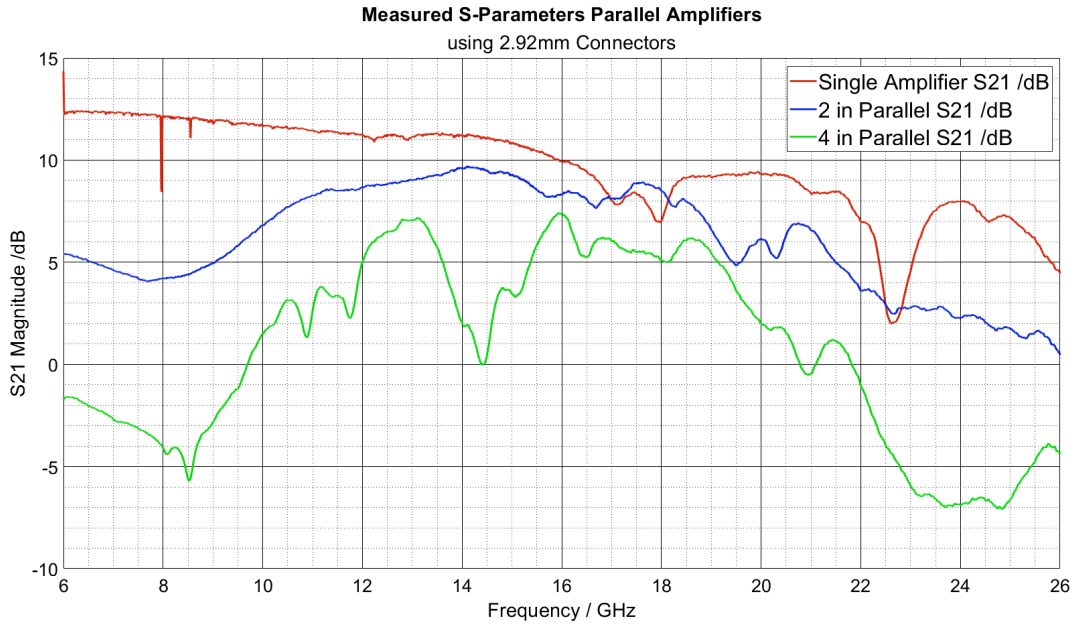


Figure 4.50: Measured Gain of the parallel amplifiers, the single stage amplifier is included for comparison.

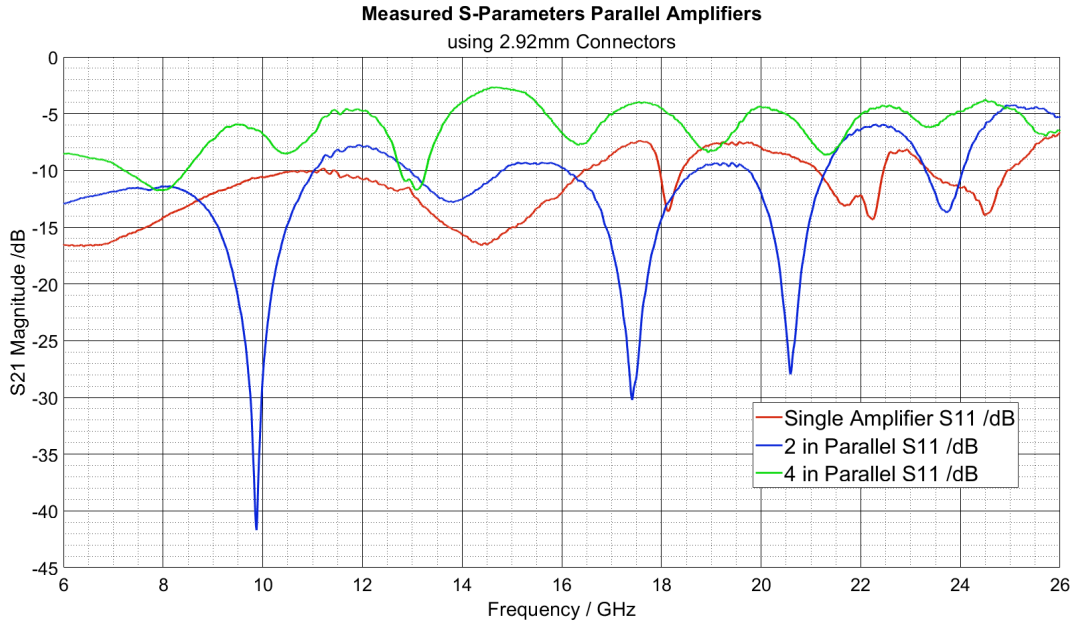


Figure 4.51: Measured return loss of the parallel amplifiers, the single stage amplifier is included for comparison.

Marki APM6849 Configuration	Gain @ 16 GHz /dB	Noise Figure @ 16 GHz	P1dB @ 16 GHz /dBm
Single	9.97	4.96	19.4
2 in parallel	8.35	5.86	21.2
4 in parallel	7.41	6.47	22.5

Table 4.11: Gain, NF and P1dB at 16 GHz for all amplifier configurations.

factor of two increase in the number of parallel amplifiers, the increase measured is between 1.6 and 1.8dB. The additional losses in the power division and combining stages is degrading the maximum output power as well as the gain.

The noise figure of the two amplifiers was measured using the noise figure mode on the R & S FSWP 50 with the HP346B noise source. The noise figure increases with increasing number of parallel amplifiers due to the increased losses of the the additional power dividers. Noise figure is the ratio of signal to noise ratio at the input of a device and the signal to noise ratio at the output of the device expressed in dB. The addition of more power dividing stages introduces losses at the input and output ports increasing the signal to noise ratio at the output of the device.

4.3.8 Residual phase Noise measurements of single and parallel amplifiers

Using (2.62) and the gain and noise figures from table 4.11, the far from carrier noise of the amplifiers can be calculated. For the single, 2 in parallel and 4 in parallel the noise floor is calculated to be -168.89dBc/Hz, -170.29dBc/Hz and -170.62dBc/Hz, respectively. Figure 4.52 is a plot with the measured residual phase noise of the three amplifiers as well as the noise floor, measured using the 11848 cross correlation system developed by Dr Simon Bale [24] and carrying out 10,000 correlations. The plot ignores the data obtained at frequencies less than 100 Hz offset as the resolution band width of the system was 7.6 Hz. The input powers to the mixer for each measurement was kept to 7.5dBm and the input power to the amplifiers was measured via a 10dB coupler. This is included on the plots.

Also on the graph are the calculated far from carrier noises for the amplifiers as well -10dB/decade lines that demonstrate the flicker noise introduced by the amplifiers, these lines are lined up with the parts of the graphs that decrease at the same rate.

The measured flicker noise corner for the single amplifier is 90 kHz, by placing two of the same

devices in parallel the measured flicker noise corner is approximately 40 kHz and for four in parallel it is approximately 20 kHz demonstrating that the parallel combination of amplifiers does suppress the flicker noise introduced by the amplifier as expected. It would be easier to see the by exactly how much the flicker noise has been suppressed each time the number of amplifiers is increased by a factor of two if the residual phase noise of the amplifiers was measured above 100 kHz. This is possible using the 11848 system but causes the measurement time to double. An estimate of the flicker noise suppression can be made using this measurement however as the the calculated noise floors are similar. The -10dB/decade line for the 2 amplifiers in parallel is approximately 4dB lower than that of the single amplifier -10dB/decade line. The noise floor of the single amplifier is 1.1dB higher so the estimated flicker noise suppression is 2.9dB. The noise floor for the two parallel amplifiers is very similar so the estimated flicker noise suppression is 2.6dB as the -10dB/ decade line for the four parallel amplifiers is approximately 2.6dB lower.

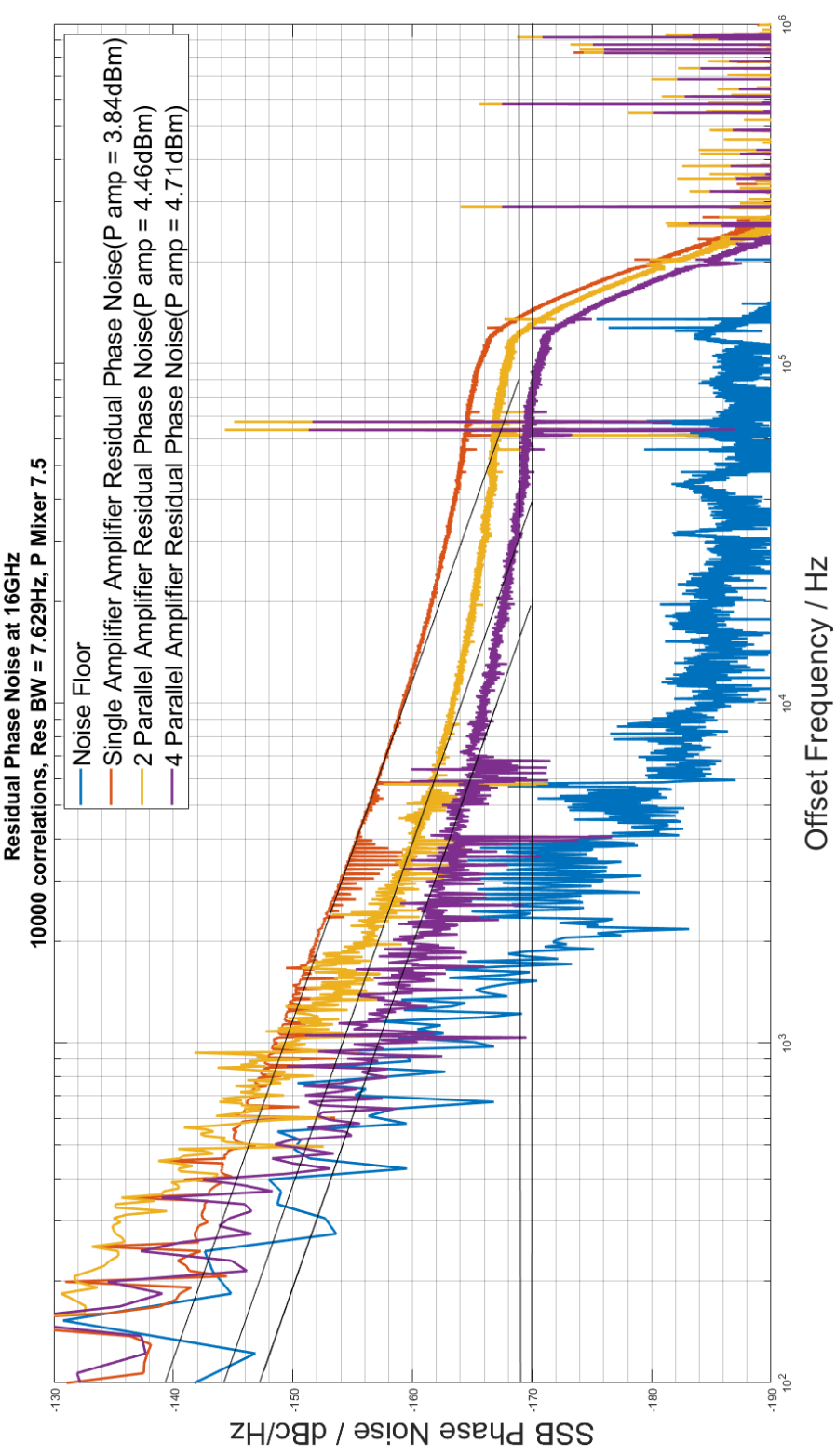


Figure 4.52: Residual phase noise measurements of the 3 amplifiers plotted with the measured system noise floor for a power level of 7.5dBm to the input mixer. 10,000 correlations were made.

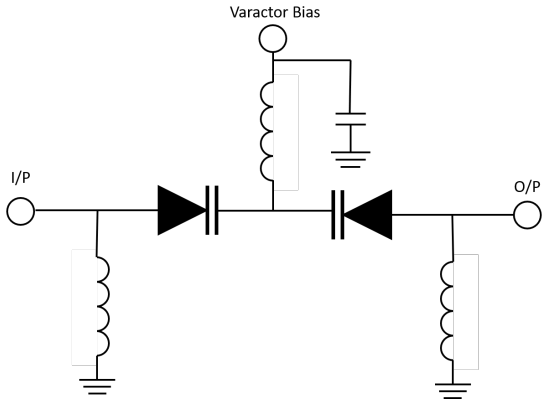


Figure 4.53: Electronically Tunable Phase shifter circuit diagram.

4.4 Phase shifters

The modified high pass filter previously used in Chapter 3 is considered here for use in this oscillator. The circuit diagram is shown in Figure 4.53. The self-resonance and parasitic effects of lumped elements at microwave frequencies cause problems with manufacturing a design and also incorrect operation. At 16 GHz, the values for the inductors and capacitors becomes very small – in the order of nH and fF. Whilst the inductors can be replaced with a short circuit stub the varactor diodes remain a challenge.

Other electronic phase shifters investigated include the modified Schiffman phase shifter that incorporates varactor diodes that vary the capacitance of the transmission line and therefore the phase. Wali et al., have demonstrated a maximum phase variation of 168° over 10.7-12 GHz BW [76] but the measured insertion loss is worse than 2dB over this range. Another design considered was that of Padilla et al. [77], which is a modified hybrid coupler with varactor diodes reflecting the signal at ports 2 and 3 back into the coupler. The tuning range was small at the centre frequency of 12.5 GHz, only 40° but the losses were between 1 and 2dB over the tuning range making it less lossy than the Schiffmann design.

A high pass filter based tunable phase shifter was designed to operate at 16 GHz as other designs were too lossy or didn't provide an adequate tuning range. By increasing the operation frequency to 16 GHz the loss will increase and the tuning range decrease. An ADS model of the MACOM MA46H120 varactor diode was available for use in simulation. An impedance transformation was required to

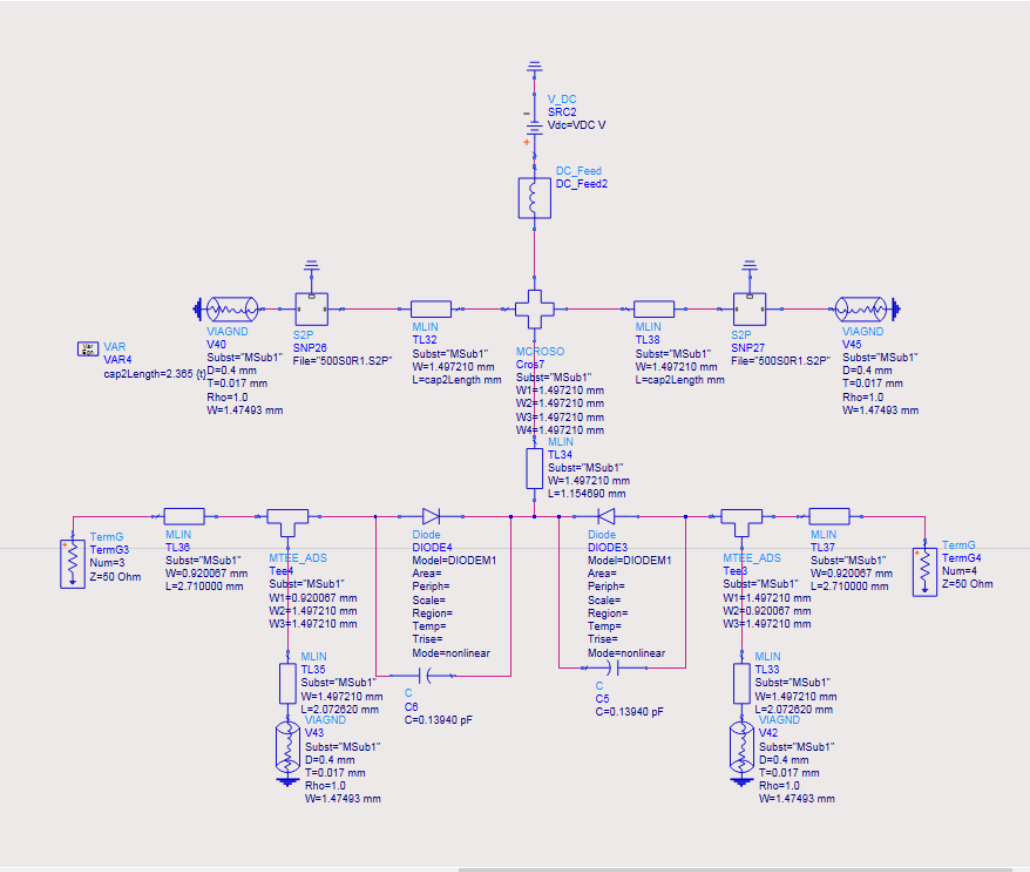


Figure 4.54: Electronically tunable phase shifter model used in ADS to simulated the frequency response of the phase shifter. A SPICE model of the varactor diode was used as well as microstrip line models and the ADS model for a via hole.

change the denormalised impedance from 50 to 25 Ω. This was because the calculated values for the capacitance in a fifth order Butterworth filter denormalised to 50 Ω would be approximately 0.2pF. Unfortunately, the lowest capacitance the MA46H120 varactor diode can exhibit is around 0.15pF. A large bias voltage would be required to achieve capacitance in this case and would give a narrow tuning range.

By transforming the denormalised impedance to 25 Ω, the normalised value of capacitance for C_1 and C_2 is approximately 0.4pf. This is attainable with a much lower bias voltage as this value is roughly in the middle of the tuning range of the varactor diode. This does however reduce the value of the inductor and as this will be implemented using a SC stub, reduces its length. It does however

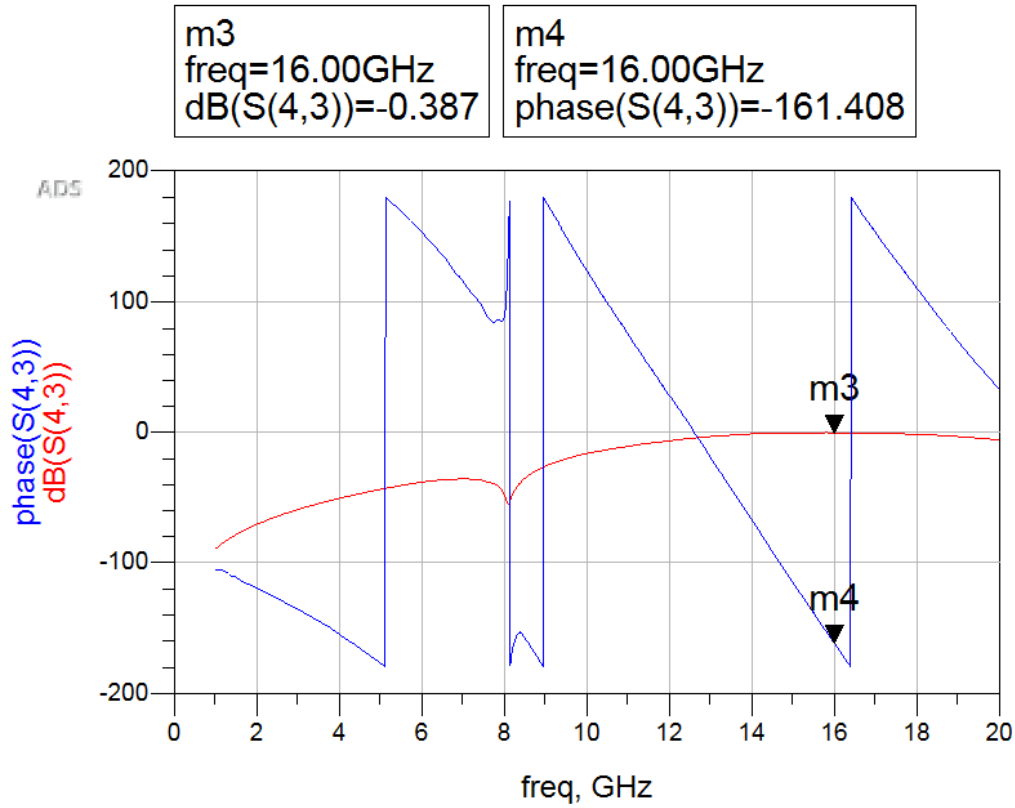


Figure 4.55: Simulated S_{21} phase /° and magnitude /dB when VBias = 7V.

increase its width. The electrical length of the SC stub at a single frequency can be calculated using (4.29):

$$j\Omega L = jZ0\tan(\beta l) \tag{4.29}$$

Where L is the inductance and βl is the electrical length of a stub. The denormalised inductors values are L1=L3= 670pH and L2=207pH. The ADS model is shown in Figure 4.54, the decoupling capacitors have been replaced with S2P files of measured 0.1pF ATC capacitors (SNP26 and SNP27), the capacitors of a fifth order Butterworth high pass filter have been replaced with the varactor diode models and the inductor L2 has been replaced with a length of microstrip of equal inductance calculated using (4.29). It provides the isolation between the DC bias network and the RF signal. The simulated tuning range is 75 degrees and the worst case insertion loss is 0.528dB. A plot of the insertion loss and phase of the phase shifter when VBias = 7V is shown in Figure 4.55 There is a notch

Figure 4.56: Notch at 8 GHz caused by the biasing network of the phase shifter.

at lower frequencies on this plot however and this has been observed to change when the decoupling capacitor values (SNP26 and SNP27) and the length of the line connecting L2 equivalent stub and the capacitor was changed. The bias network, including the inductive stub, decoupling capacitors and lengths of microstrip that the capacitors connect to, forms a notch filter with a resonant frequency of approximately 8 GHz. Figure 4.56 is a plot of the insertion loss of the bias network section with a notch at 8 GHz. At 16 GHz the insertion is simulated to be 0.387dB and the phase shift is –161.4°. The lengths of the microstrip used to connector to the decoupling capacitors and the capacitor values were optimised to ensure that 16 GHz is out of the notch bandwidth. The centre frequency of the notch of the optimised bias network formed by the bias network is 6.46 GHz and the insertion loss at 16 GHz was -44dB.

4.4.1 Prototype PCBs and measurements

The phase shifter schematic in ADS was used to create a PCB layout. Four different PCB layouts were designed as it was found that another varactor diode, the MACOM MAVR-000120-1411, could have

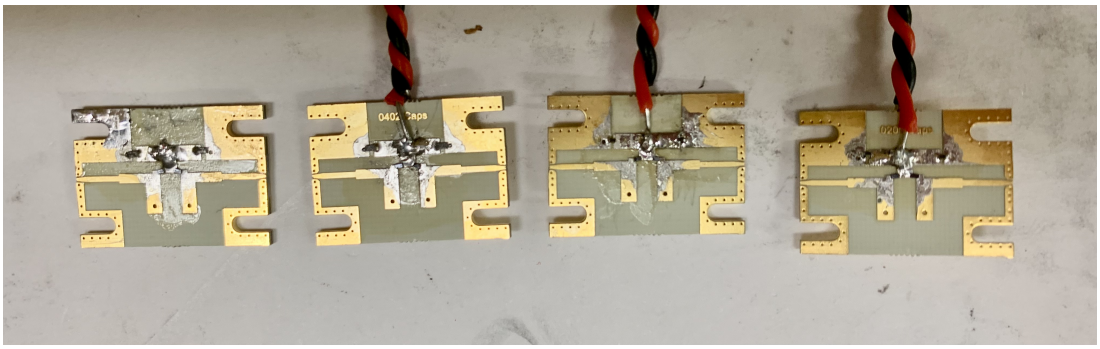


Figure 4.57: L-R Manufactured 16 GHz phase shifters using MACOM MAVR-000120-1411 varactor diodes 0402 size decoupling 0.1pF capacitors, MACOM MA46H120 varactor diodes with 0402 size decoupling capacitors, MACOM MAVR-000120-1411 varactor diodes 0201 size decoupling 0.1pF capacitors and MACOM MA46H120 varactor diodes with 0201 size decoupling capacitors.

the potential to be used and two different sized capacitors were available for the decoupling capacitors, 0201 and 0402. The capacitors used in the manufacture were manufactured by Kyocera AVX and are from the Thin-Film RF/Microwave Capacitor Technology Thin-Film Technology Accu-P Series [78]. Figure 4.57 is a photo of the four 16 GHz phase shifter PCBs. The phase shifters insertion loss and phase at 16 GHz were measured against varying bias voltage using the Anritsu. Plots of the measured insertion loss and phase against varying bias voltage are shown in figures figs. 4.58 to 4.61.

MAVR-000120-1411 with 0201 decoupling capacitor

This implementation of the phase shifter uses the MAVR-000120-1411 varactor diode with 0201 decoupling capacitors on the bias line. The minimum insertion loss of this circuit was achieved with a bias voltage of 11V and was -3.41dB. The phase response against bias voltage is fairly linear and the maximum range of phase shift is 103.17°. However with 0V bias the insertion loss is -7.834dB, too lossy for use in an oscillator as it has the potential to cause the oscillator to stop oscillating. The variation in insertion loss at bias voltages greater than 5V is 1.371dB and phase shift tuning range is 76.61°.

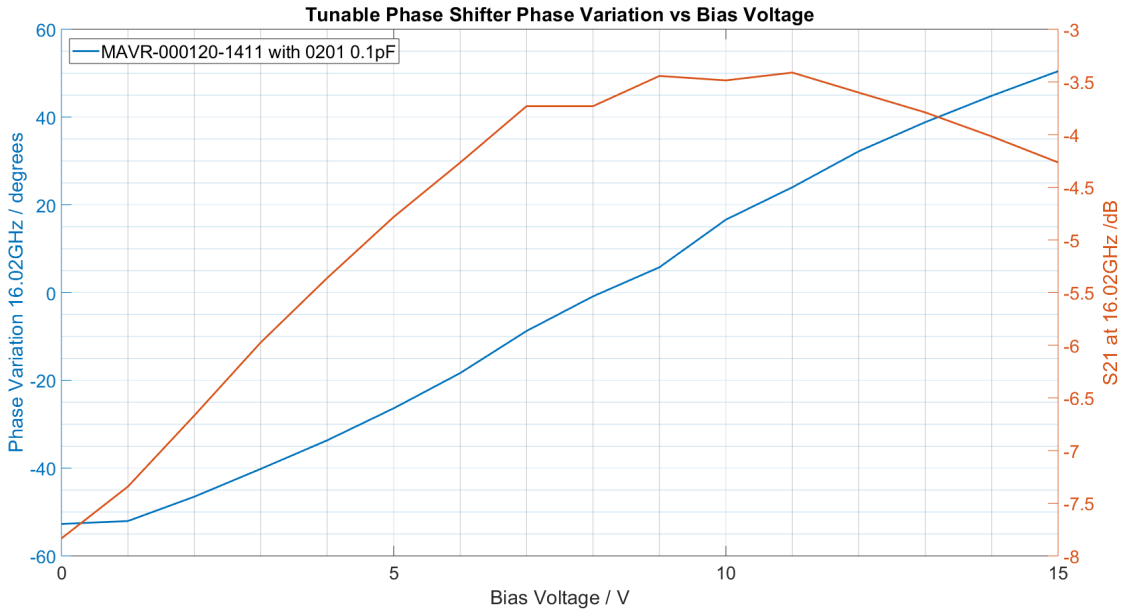


Figure 4.58: Measured insertion loss and phase plotted against varying bias voltage for the 16 GHz phase shifter using MAVR-000120-1411 varactor diodes 0201 size decoupling 0.1pF capacitors.

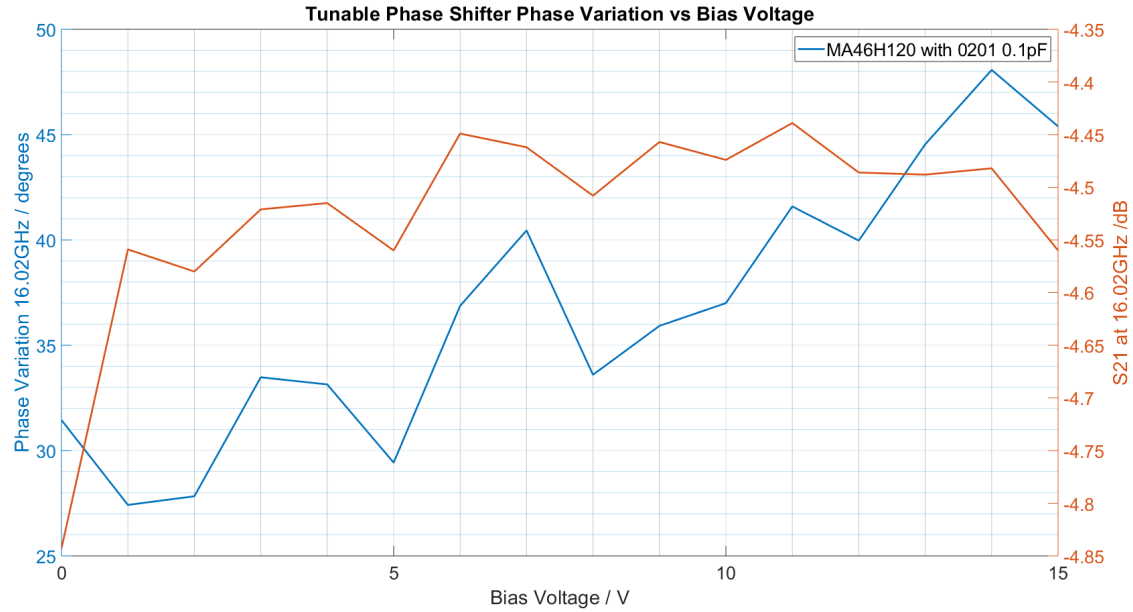


Figure 4.59: Measured insertion loss and phase plotted against varying bias voltage for the 16 GHz phase shifter using MACOM MA46H120 varactor diodes with 0201 size decoupling capacitors.

MA46H120 with 0201 decoupling capacitor

The second circuit used the same 0201 decoupling capacitors but the MA46H120 varactor diode was used instead. Measurements of insertion loss had a maximum variation of 0.404dB however the minimum insertion loss was greater than the previous circuit by 1.03dB at -4.44dB, which is likely to introduce too much loss into a 16 GHz oscillator. The phase response is non linear and there are bias voltages that cause the phase shifter to introduce the same amount of delay as another voltage. The tuning range is smaller than the previous circuit across the range of measurements with the possible range of tuning 20.65° across all bias voltages and 18.64° from 5-15V. A smaller tuning range could be useful in an oscillator as greater precision can be achieved in applying the correct bias voltage to cause the oscillator loop to equal 360°. However this implementation introduces too much loss across the range of bias voltages which, added to the loss of all other components is unlikely to be overcome by a single amplifier. A second gain stage is likely to be needed in that case and will increase the far from carrier noise of the oscillator as the noise figure will increase.

MAVR-000120-1411 with 0402 decoupling capacitor

The minimum insertion loss of the phase shifter using the MAVR-000120-1411 varactor diodes and 0402 decoupling capacitors is -1.979dB which is the lowest insertion loss observed for all four phase shifting circuits. At 0V bias the insertion loss is -6.549dB, the maximum insertion loss introduced by this circuit. From 5-15V the phase shift increases linearly with increasing bias voltage, across this range of bias voltages the phase shift varies from –29.47° to 39.04° providing a maximum phase shift variation of 68.51°. Across this tuning range the insertion loss variation is 1.276dB.

MA46H120 with 0402 decoupling capacitor

The final implementation used the MA46H120 varactor diode with the 0402 size decoupling capacitor. The minimum insertion loss of this circuit is -2.318dB and is 0.339dB more than that of the previous implementation. The maximum insertion loss is -6.965dB at 0V bias. A tuning range from 5V to 15V bias of 68.65° is achieved which is comparable to the previous and first implementations. There is linearly increasing phase shift across the 5-15V bias range. The range of insertion loss across this range of bias voltages is 1.5dB, 0.224dB more than the previous implementation.

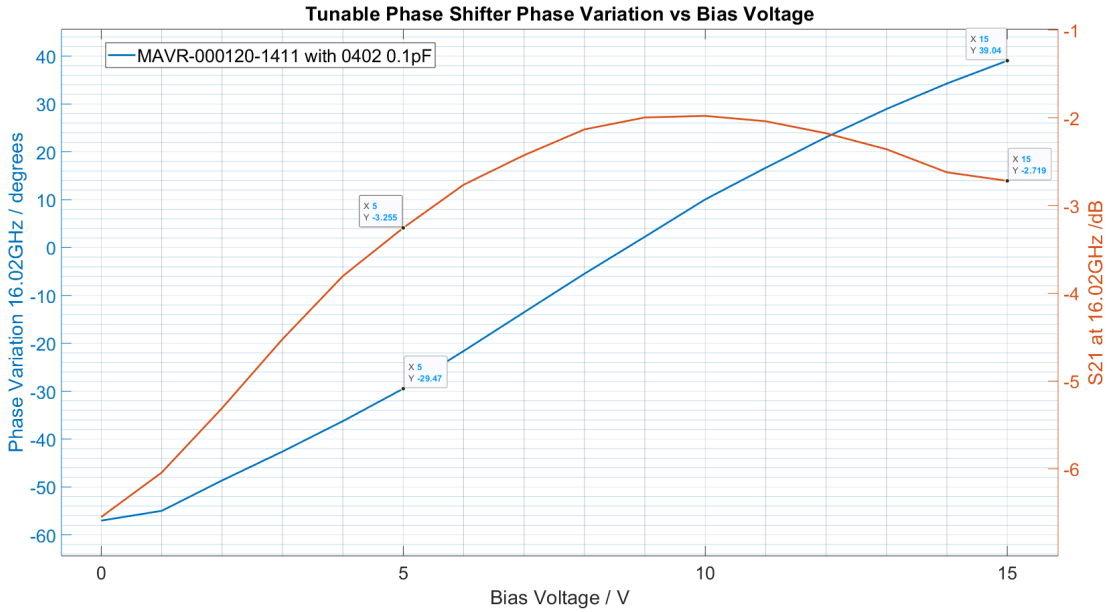


Figure 4.60: Measured insertion loss and phase plotted against varying bias voltage for the 16 GHz phase shifter using MAVR-000120-1411 varactor diodes 0402 size decoupling 0.1pF capacitors.

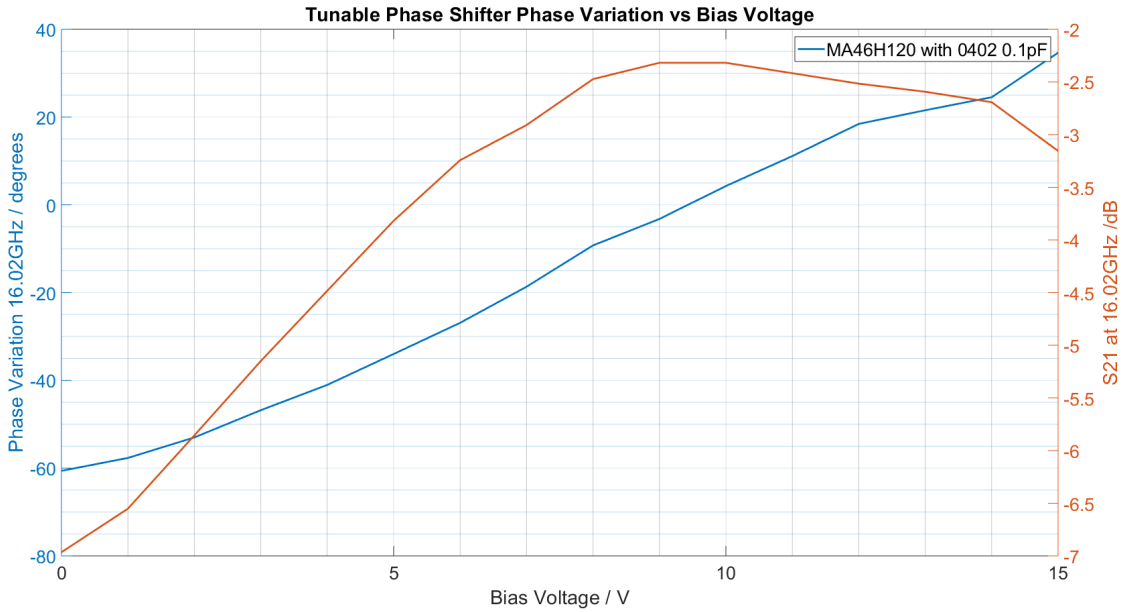


Figure 4.61: Measured insertion loss and phase plotted against varying bias voltage for the 16 GHz phase shifter using MACOM MA46H120 varactor diodes with 0402 size decoupling capacitors.

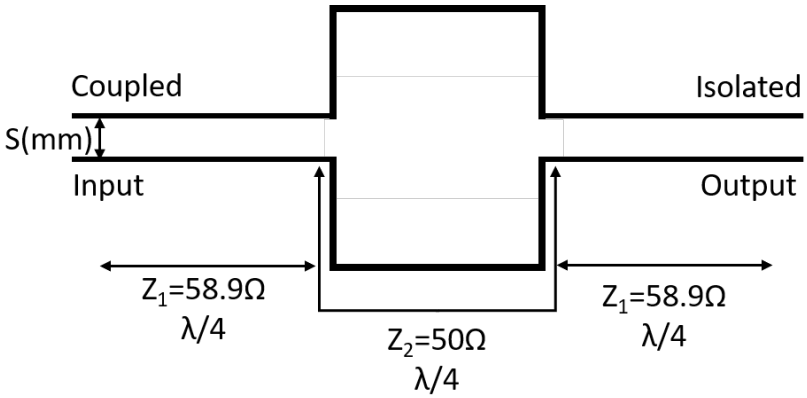


Figure 4.62: Circuit diagram for broadband directional coupler.

These measurements suggest that using the 0201 size decoupling capacitors will increase the insertion loss of the circuit at all bias voltages, it would be preferred then to use the implementations with 0402 capacitors in order to reduce the insertion loss of the phase shifter. The phase shifter should therefore use the 0402 decoupling capacitors and should be operated with a minimum bias voltage of 5V and a maximum of 15V, this would give a maximum range of insertion loss of 1.5dB for the phase shifter if the MA46H120 varactor diode is used. The tuning range would be 68° with either varactor diode. As the range of phase introduced is similar, the MAVR-000120-1411 varactor diode should be used for lowest insertion loss across the tuning range of 5-15V.

4.5 Output coupler

The complete oscillator will form a closed loop and in order to observe a 16 GHz oscillating signal, a method of coupling the signal to an output port is required. This part of the circuit must also be low loss and make a small contribution to the overall phase noise power of the oscillator. A wideband directional coupler can be designed using multiple coupling sections. The coupling ratio sets the best case for insertion loss at the centre frequency but it is not possible to design a single section directional coupler at 16 GHz that achieves -10dB coupling as the separation between the coupling lines to too small to be manufactured.

An ideal 10dB coupler will couple exactly -10dB of the input signal to the coupled output port. The lowest possible insertion loss from the input to the output port is 0.46dB for an ideal 10dB

coupler. The design for the multi section directional coupler must include a central section that is λ/4 in length that doesn't provide any coupling. This is due to the two coupling sections both also being λ/4 in length and therefore two λ/4 sections will not provide any coupling if placed next to each other to form a λ/2 coupling section as the coupled signals from both λ/4 will be out of phase. Figure 4.62 shows the circuit diagram. A full analysis of the circuit is performed in [79], where a derivation for the coupling equations is presented. The coupling ratio is given by the following (4.30):

$$C_1 = \Gamma_{in} = (Z_1^4 - 1)/(Z_1^4 - 1) \tag{4.30}$$

Where C_1 is the coupling ratio at the coupled output, Γ_{in} is the reflection coefficient and Z_1 is the impedance of the coupling section. The central non coupling section should have an impedance equal to Z_0. Rearranging for Z_1 gives:

$$Z_1 = \left(\frac{1+C}{1-C}\right)^{\frac{1}{4}} \tag{4.31}$$

The coupling ratio for the individual λ/4 sections is calculated from the impedance of Z_1 :

$$C_1 = (Z_1^2 - 1)/(Z_1^2 + 1) \tag{4.32}$$

In a 50Ω system and 10dB coupler ratio the impedance of the coupling sections should therefore be 58.9Ω with a coupling ratio of the coupling sections equal to 7.92dB.

Using LineCalc tool in ADS and the design parameters for the Rogers 4350 board to be used, the correct dimensions for the coupled lines were calculated and simulated in CST. Optimisation simulations were performed to reduce the insertion loss at 16 GHz. These included varying the shape of the non-coupling centre section, the separation between the coupled section, the width of the microstrip lines used in the non-coupling section as well as the width of coupled section lines.

It was found that the insertion loss was found to be 0.3dB lower when the central track width was equal to that of the coupled section, the impedance of the microstrip was now 60.8 Ω. This believed to be due to the lack of sudden changes in width between the different transmission lines and less power reflections occurring at the junction. Figure 4.63 shows the CST model used in the simulation. The coupler was manufactured using this CST model with the only difference being the manufactured model included the additional lengths of Tx line used to attach the connectors. The

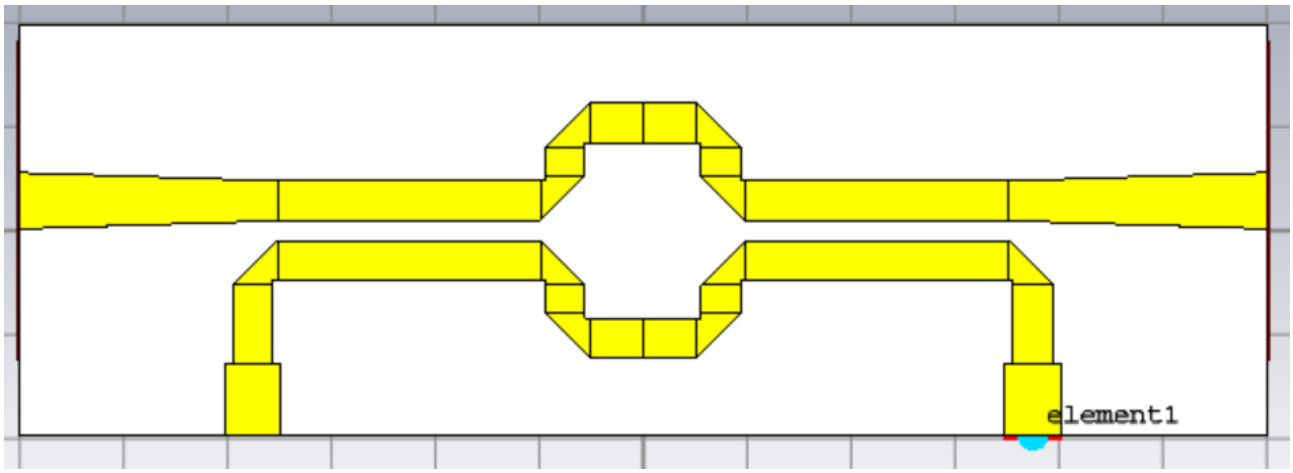


Figure 4.63: CST model for broadband directional coupler used to optimise the separation between the input and output lines and the dimensions of the microstrip lines.

simulated S-Parameters of the optimised wideband 10dB coupler are shown in Figure 4.64. The measured S-Parameters from the manufactured 10dB coupler are plotted in Figure 4.65. At 16 GHz the loss of the through line was measured to be -1.63dB, S_{11} was -17.8dB and S_{31}, the coupled output, was measured to be -11.7dB. The through line loss is about 1dB more lossy than predicted and the coupled output is 1.7dB more lossy than predicted. This is thought to be due the addition of the WithWave connectors and the additional lengths of microstrip line required to connect them as well as inaccuracies in the way CST models losses in the copper and the dielectric in the substrate.

The Knowles FPC06075 [80] coupler was also considered for use. A test board was manufactured using the Gerber file provided by the manufacturer and measured for comparison with the wideband directional coupler design. The loss at 16 GHz was measured to be -2.72dB more than 1dB more than the optimised microstrip design and was therefore considered to be too lossy for use in the 16 GHz oscillator.

4.6 Complete oscillator

Multiple 16 GHz oscillators have been built using different combinations of the amplifiers. It was found that the electronically tunable phase shifter using the MAVR-000120-1411 varactor diodes and 0402 decoupling capacitors would introduce at least 2dB insertion loss into the loop and this value

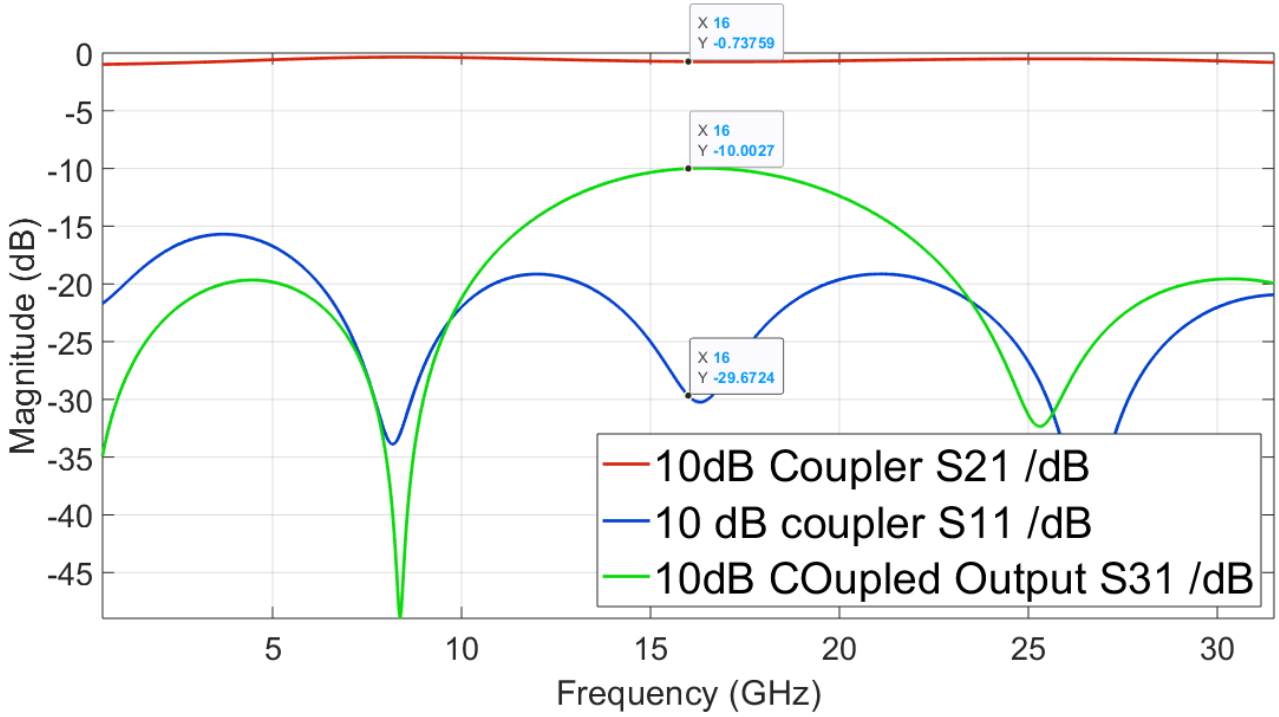


Figure 4.64: Simulated S-Parameters of the CST model for the 10dB directional coupler.

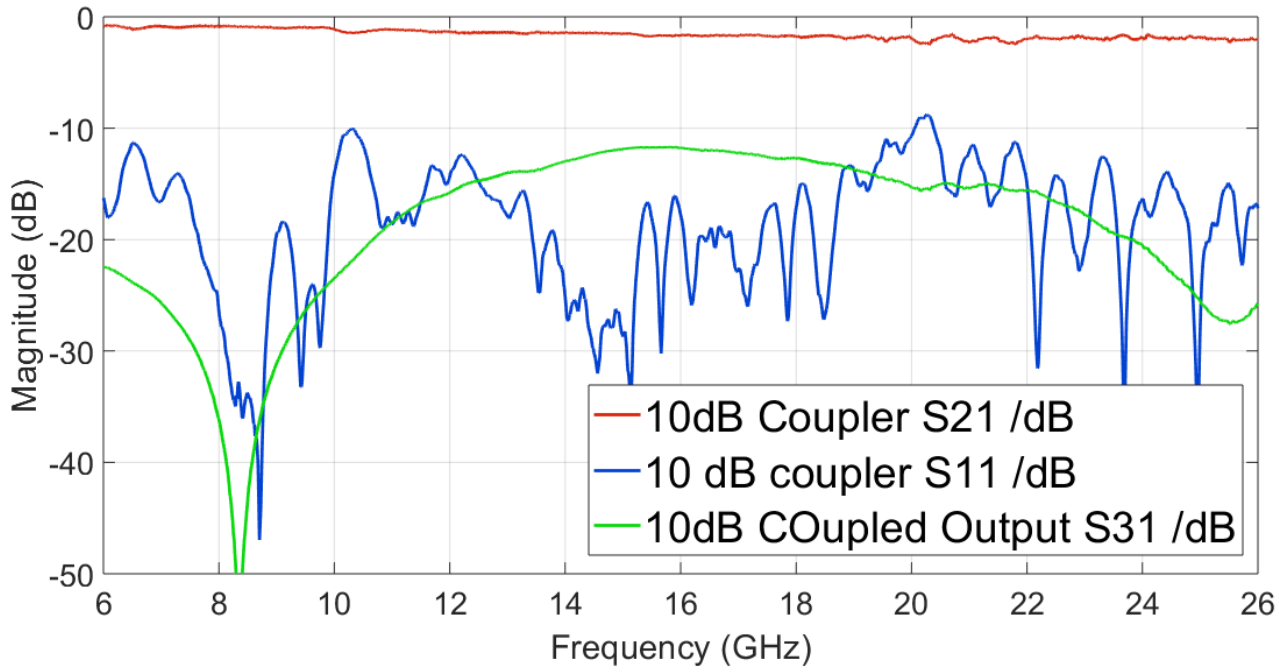


Figure 4.65: Measured S-Parameters of the CST model for the 10dB directional coupler.

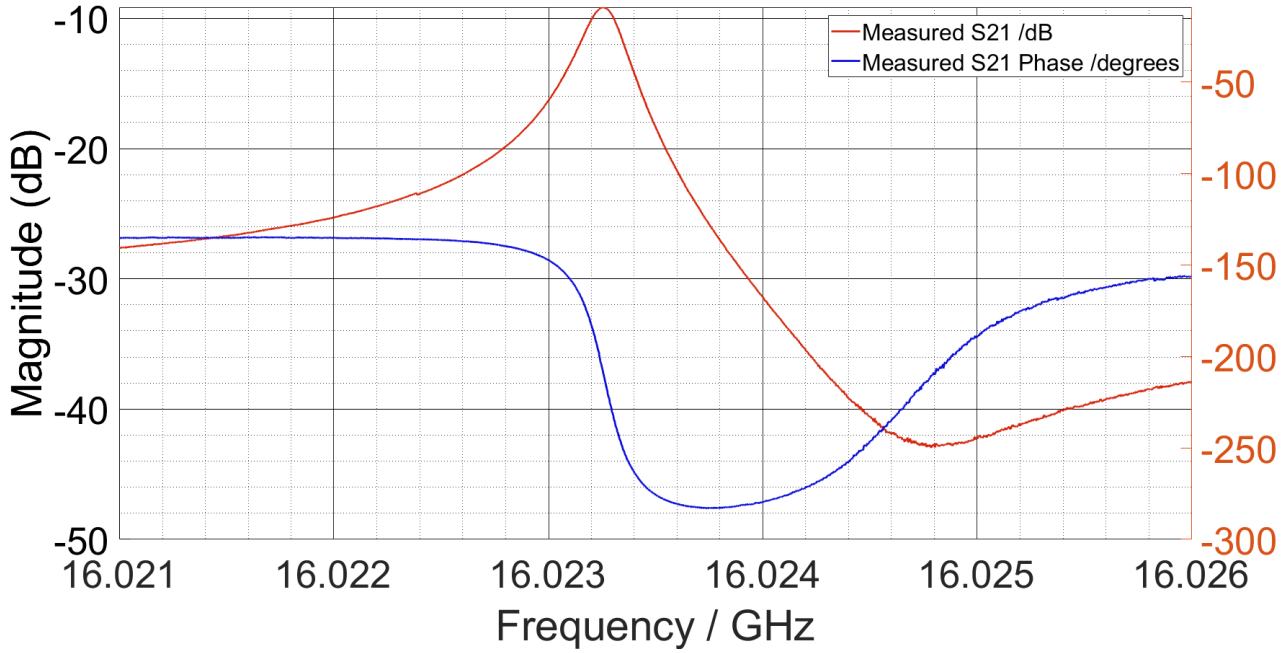


Figure 4.66: Measured insertion loss of the resonant peak at 16.02 GHz.

will increase across the tuning range, varying the power available to the input of the resonator and therefore affect the oscillator phase noise. Furthermore the tuning range was 68.51°. As the losses in the loop are likely to be an issue in this oscillator, a mechanical phase shifter was selected for use. The ATM P1507 [81] was chosen as it offers 90°/GHz phase shifter and is operational from 0-18.6 GHz. The insertion loss at 16 GHz was approximately 1dB across a full 360° tuning range.

The resonator S-Parameters were measured again as the probes had to be replaced, the measured insertion loss showing the resonant peak is depicted in Figure 4.66 where the resonant frequency is 16.023 GHz and the insertion loss is -9.14dB. The measured 3dB bandwidth is 215 kHz giving a Q_l of 74600 and a Q_0 of 115000. The typical oscillator configuration is shown in Figure 4.67, the 'Amp 2' component is varied for the oscillator measurements for the different number of amplifiers place in parallel. Each measured had at least one Marki APM6849SM device in series before the 'Amp 2' in order to increase the loop gain. Open loop measurements showed that the excess gain was less than 0dB when only one amplifier was placed in the oscillator loop as a result of all of the losses in the loop including the interconnecting coaxial cable, that introduces a loss of 2.14dB. The different oscillator

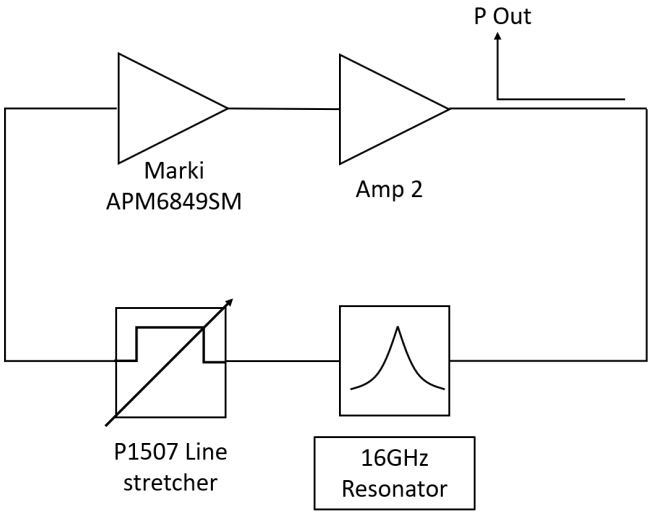


Figure 4.67: Typical oscillator configuration block diagram. Amplifier 2 is changed for each measurement and consists of different number of parallel amplifiers/series attenuators/series amplifiers.

phase noise measurements made used the following amplifier configurations in place of 'Amp 2':

1. Single Marki APM6849SM device
2. 6dB attenuator in series with Single Marki APM6849SM and the PCB with 2 Marki APM6849SM devices in parallel
3. 6dB attenuator in series with Single Marki APM6849SM and the PCB with 4 Marki APM6849SM devices in parallel

The excess gain of the open loop oscillator in the three different configurations was measured to be 3.27dB, 1.85dB and 2.27dB respectively. The final configuration for 'Amp 2' required an additional gain stage to increase the excess gain to be greater than 0dB, a second Marki APM6849SM device was placed in front of the PCB with four devices in parallel to achieve this. A 6dB attenuator was placed in front of the single Marki device to reduce the overall excess gain to around 2dB and to reduce the saturation of the single device. The oscillator was placed in an aluminium shielding box lined with foam to help stabilise the temperature. An image of the oscillator setup is shown in Figure 4.68. The bias voltages for the Marki devices, V_B and V_C, were both set to 5V for these measurements. It was found that with 6V to both pins that the devices could become unstable resulting in oscillations. This

meant that too high a current could be drawn and could damage the devices. The datasheet for the devices states that unconditional stability can be achieved when the bias voltages are set to 5V, the R & S FSWP 50 V_{Supply} and V_{Tune} voltage supply points were used to power the amplifiers.

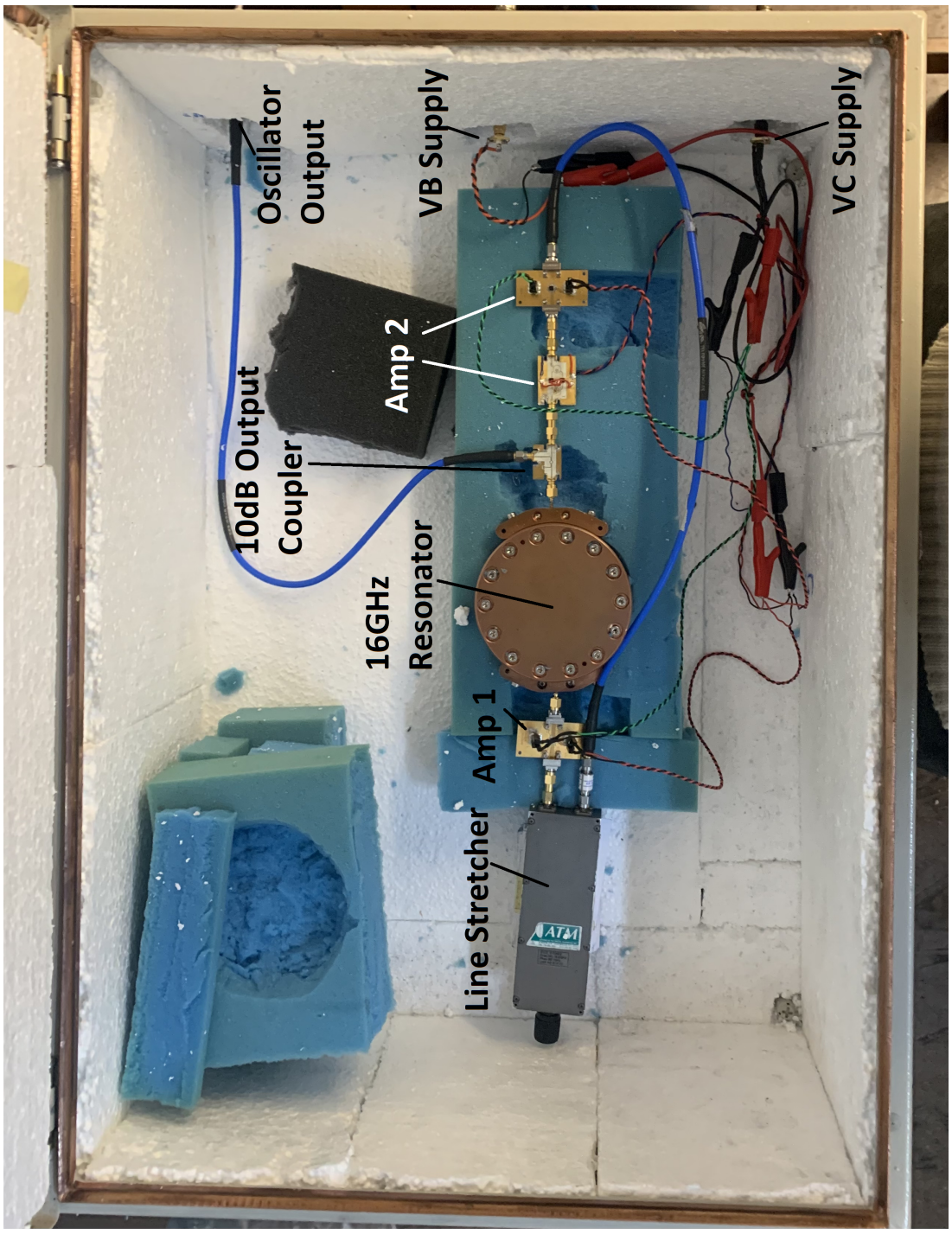


Figure 4.68: 16 GHz oscillator placed in shielding box and surrounded by foam. In this image 'Amp 2' is a series combination of a single APM6849 and the PCB with two APM6849 devices in parallel. A 6dB attenuator is placed before the single amplifier, after the line stretcher to reduce the excess gain in the loop and therefore reduce the saturation of the devices.

4.6.1 Measured oscillator phase noise

Single Marki AP6849SM amplifier configuration

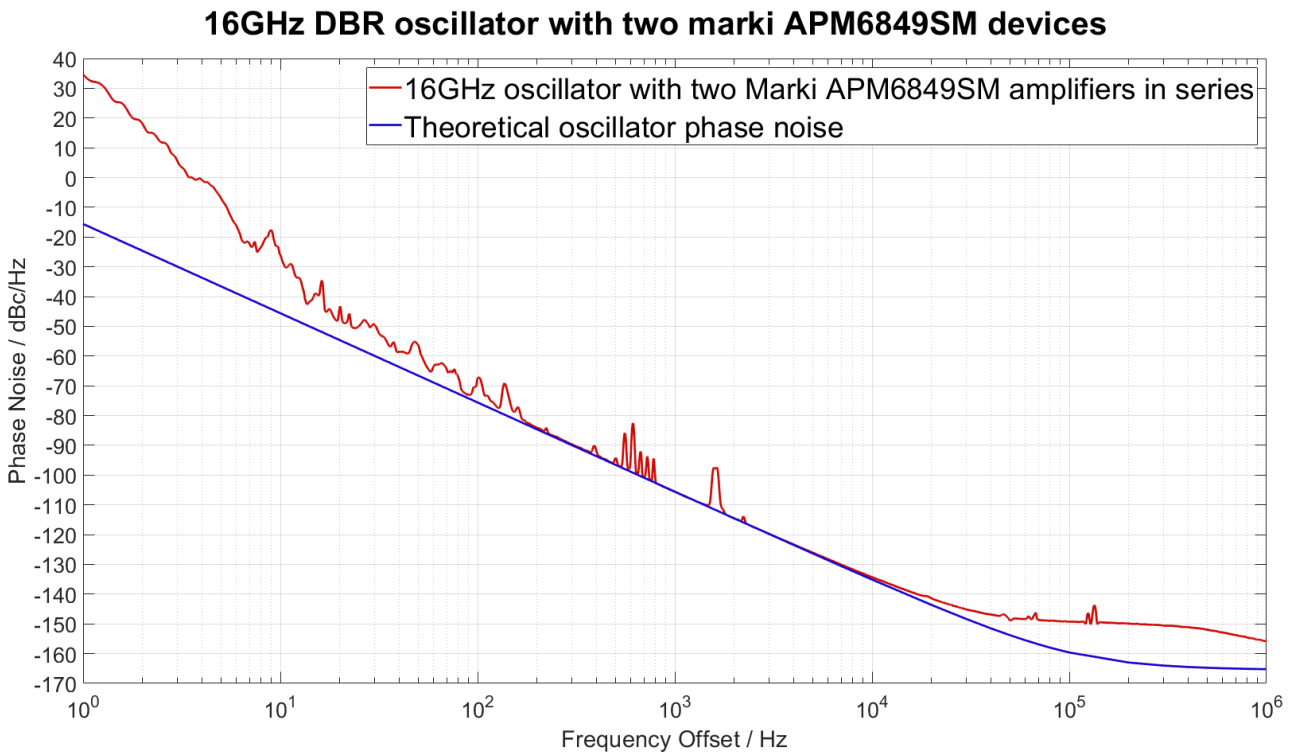


Figure 4.69: Measured 16 GHz DBR oscillator where 'Amp 2' is a single Marki APM6849SM device. This configuration therefore has two of the Marki devices in the feedback loop separated by the line stretcher and the SMA to SMA coaxial cable.

The R & S FSWP 50 phase noise measurement system was used to measure the phase noise of the different oscillators with the oscillator output being taken directly to the RF input via two coaxial cables and a female to female SMA connector attached to the wall of the metal enclosure. The total losses introduced by the two cables and the connector was measured to be 2.145dB.

The first oscillator configuration that was measured used a single Marki APM6849 amplifier placed in the 'Amp 2' position. There are therefore two Marki devices in the feedback loop, one at the resonator output and the other connected in series with it but placed after the line stretcher and SMA coaxial cable. The output couple is connected to the output of the second amplifier and to the input of the resonator. The measured output power at the R & S FSWP 50 input was 4.73dBm, therefore

the actual power at the oscillator output is 6.875dBm. The power available to the resonator can be calculated by subtracting the coupling ratio of the output coupler, -11.7dB and adding the insertion loss of the through line, -1.63dB to the oscillator output power, 6.875dBm, giving 16.945dBm. 1000 correlations in the 1-10 Hz band were made and the resolution bandwidth was 5%.

The measured phase noise is plotted in Figure 4.69, this figure also includes a plot of the theoretical phase noise of the oscillator calculated using the following parameters: flicker noise corner (f_c) =90 kHz, Q_L = 74600, Q_0 = 114618, noise figure (NF_1)= 19dB and power available at the resonator input (P_{AVO}) = 16.945dBm. The measured noise figure of the amplifier is 4.96dB when it is operating in the linear regime, in the oscillator the second amplifier is likely to be driven into saturation. The noise figure is an estimate of the noise figure of all the components in the feedback loop and includes both amplifiers and the line stretcher and coaxial cable.

The measured oscillator phase noise agrees with the theory in the frequency range 100-10,000 Hz but is significantly different outside of this range. Considering the measured oscillator phase noise from 1-100 Hz offsets, the measured oscillator phase noise is higher than the theory but offsets less than 3 Hz the measured oscillator phase noise is positive. This is likely due to the oscillation frequency rifting due to thermal effects causing the resonator frequency to drift. This results in the output power being overlaid onto the phase noise plot and masking the actual noise power. This is also likely to be the cause of the increased noise up to 7 Hz offset when compared to the theory. From 7 Hz -100 Hz there appears to be small peaks indicating that other noise sources are modulating onto the phase noise response, there is a peak at 50 Hz (and subsequent harmonics at 100 and 150 Hz) caused by mains. The measured phase noise is fairly smooth from 100 Hz up to 10 kHz where is agrees with the theory but at frequency offsets greater than 10 kHz, the measured phase noise begins to flatten implying that the far from carrier noise floor is being reached.

This would also suggest that the flicker noise corner of the amplifier has decreased from the calculated value of 90 kHz. This is unlikely as the calculated value is calculated from a measurement of the amplifier operating in the linear regime whereas at least one of the amplifiers in the oscillator are likely to be saturating causing the flicker noise corner to increase. The measured phase noise begins to roll off at frequency offsets of 300 kHz and above suggesting that there is something introducing the measured phase noise from 10 kHz offsets and above.

2 Parallel Marki AP6849SM amplifiers configuration

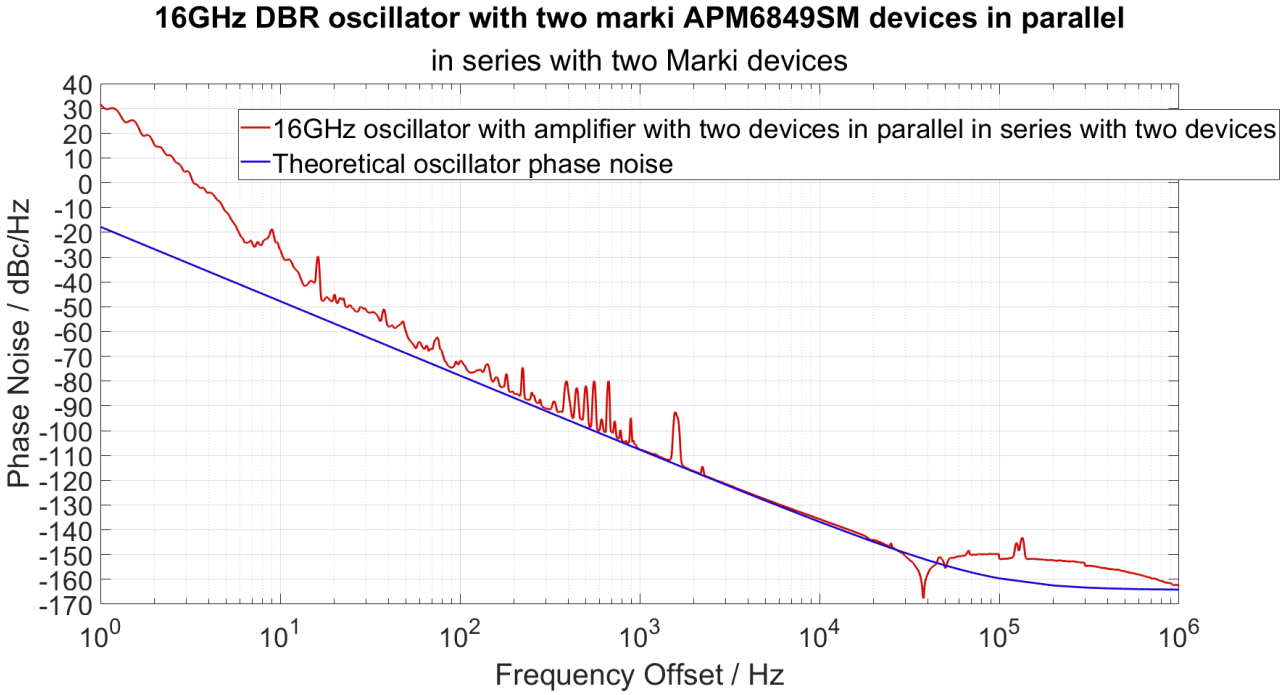


Figure 4.70: Measured 16 GHz DBR oscillator where 'Amp 2' is a series combination of a 6dB attenuator, a single Marki APM6849SM device and the amplifier with two devices placed in parallel.

The second oscillator configuration placed the output of the amplifier with two devices in parallel, at the coupler input. A 6dB attenuator was placed at the input of the second single Marki device and its output was connected to the parallel amplifier input. The oscillator output power measured at the input to the R & S FSWP 50 was 4.86dBm, the power at the oscillator output was calculated to be 6.995dBm and the power available at the resonator input is calculated to be 17.065dBm. The measured oscillator phase noise is plotted in Figure 4.70 and the theoretical phase noise using the same parameters as before for Q_L and Q_0 but the noise figure is estimated to be 21dB, flicker noise corner is 40 kHz and P_{AVO} is 17.065dBm.

The close to carrier phase noise is once again greater than 0dBc/Hz up to 3 Hz offsets and is higher than the calculated theory up to approximately 100 Hz offset. This is thought to once again be the result of frequency variation of the oscillator causing the apparent measured phase noise to increase when in reality the noise is actually the power in the oscillation frequency after it has changed. From

100 Hz to 1 kHz there are lots of 'spurs' in the measurement but the bottom of these 'spurs' agree with the theory. The measured phase noise from 1 kHz - 10 kHz agrees with the theory but after 25 kHz the measured noise forms a sharp trough, reaching a minimum at 35 kHz, before increasing up to -150dBc/Hz at 100 kHz offset.

This trough is thought to be caused by 'cross correlation collapse' where an additional random process is introduced into the cross correlation measurement system but is anti correlated (in anti phase and correlated) between each channel [82]. The cross spectrum will collapse to zero at a frequency where the amplitude of both the carrier signal and the additional signal is equal. The additional noise could be a result of the oscillator AM noise has not been suppressed in the limiting process and is leaking into the measurement system, causing the notch in the phase noise measurement. The measured phase noise then starts to roll off to -160dBc/Hz at 1 MHz offset, the calculated value at this offset frequency.

4 Parallel Marki AP6849SM amplifiers configuration

The final configuration replaces the amplifier with two devices in parallel with the amplifier with four devices in parallel. The 6dB attenuator is still placed between the two single device amplifiers. The input power to the R & S FSWP 50 was measured to be 5.9dBm so the calculated power available at the resonator input is 18.115dBm. The flicker noise corner is 20 kHz and the noise figure is estimated to be 25dB. Q_L and Q_0 are kept at 74,600 and 114,618.

The measurement made in this configuration is in the closest agreement with the theory at offsets greater than 1 kHz but the increase at carrier offsets closer than 100 Hz is still present, though the trace is smoother than previous measurements. From these measurements it is clear the the noise figure is too high and increases with the number of parallel amplifiers used. This results in an increase to measured phase noise of the oscillator. At 10kHz offset the measured oscillator phase noise is -132dBc/Hz and the far from carrier noise is -160dBc/Hz.

Furthermore, the close to carrier noise is far from the theory and is likely caused by variation in the oscillation frequency. The likely cause of this is due to thermal effects on the resonator changing the resonant frequency over the course of the measurement and temperature stabilisation of the cavity must be considered in order to reduce the frequency drift.

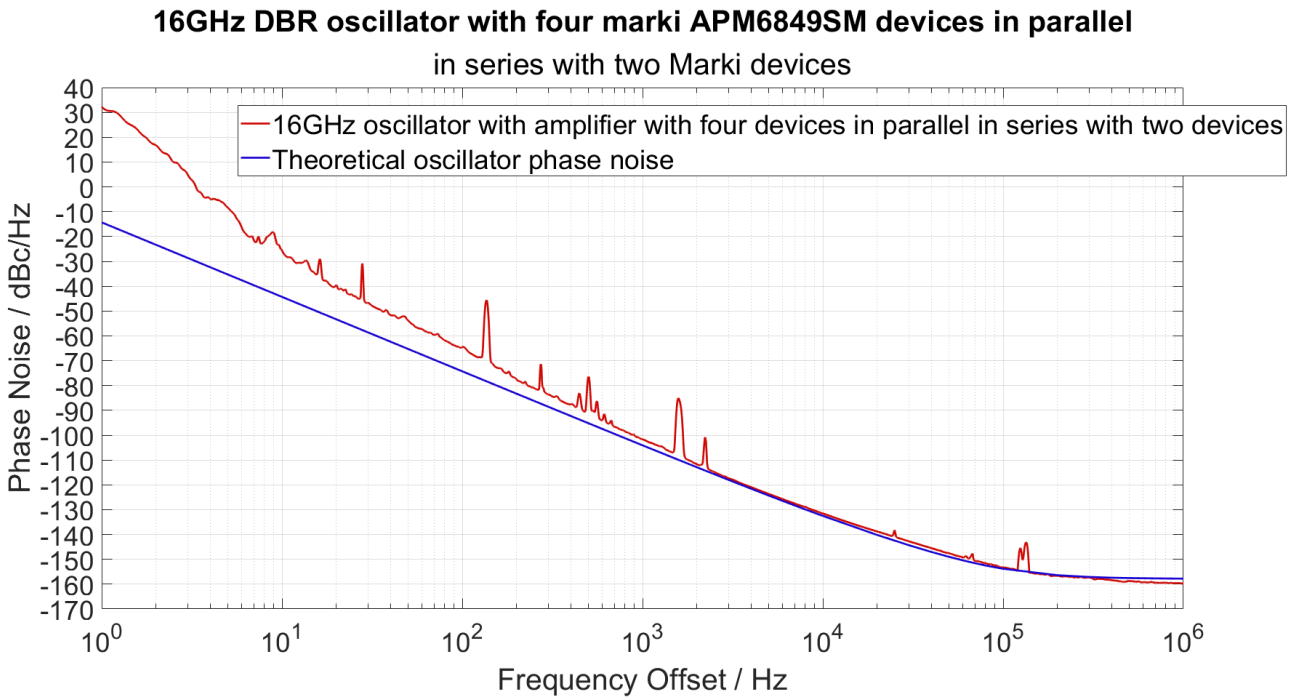


Figure 4.71: Measured 16 GHz DBR oscillator where 'Amp 2' is a series combination of a 6dB attenuator, a single Marki APM6849SM device and the amplifier with four devices placed in parallel.

4.7 Conclusions and further work

The development of a 16 GHz DBR oscillator is presented in this chapter including research into coupling to the resonator, flicker noise reduction of amplifiers by placing devices in parallel and finally initial measurements of the oscillator phase noise. The measurement that most closely matches the theory was obtained by using the amplifier with four devices in parallel however the noise figure is very high and causes an increase in the measured phase noise.

Furthermore, the oscillator frequency appears to vary over the measurement period that is introducing apparent positive phase noise at close to carrier offsets. This is actually the power at the oscillation frequency once as it is changing but is being mistaken as phase noise by the R & S FSWP 50. The causes of the frequency variation include temperature and vibrations.

Further measurements should be made of the resonator to determine its temperature stability and its vibrational sensitivity. The DBR incorporates Spira Gasket to hold the plates firmly in place and does appear to keep the resonant frequency stable if it is being manually tapped. A scientific measurement is necessary however to accurately demonstrate this. It was observed that the resonant frequency does change when the cavity is touched causing a slight heating effect and changing the size of the metal rings. A series of measurements of the resonator's S-parameters should be made whilst varying the temperature of the resonator. Furthermore, the oscillator should stabilised to a specific temperature and further phase noise measurements should be made with the aim of removing the frequency drift and therefore decreasing the close to carrier phase noise.

One of the main issues in this chapter is the losses introduced by the connectors at 16 GHz. The oscillator measurements had to be made with multiple gain stages in order to allow oscillation to be sustained. To reduce these losses, all PCBs should be manufactured on the same board and as small lengths interconnecting coaxial cable should be used. Furthermore the insertion loss must be reduced to closer or below 6dB so that smaller gain from the amplifier is required. This will reduce the noise figure of the feedback amplifier.

An electronically tunable phase shifter should also be included if it can be shown to introduce a smaller insertion loss at 16 GHz. It should be incorporated into a single PCB with the other feedback components to remove unnecessary 2.92mm connectors. The output coupler could be replaced with

a 3dB power divider, similar to the 1.5 GHz DRO design to reduce the input power to second stage amplifiers if it is found that more than one amplifier is required. This would reduce the amount of saturation the second stage, placed at the resonator input, experiences and will reduce the noise figure.

The research into waveguide coupling should be extended to determine why the simulated results do not match the measurement. This approach to coupling to the resonator has the potential to decrease the insertion loss of the resonator and would reduce the required amplifier gain (and therefore the noise figure). It is also more robust than the current probe coupling. Further oscillator phase noise measurements should be made once with the improvements suggested in this section have been made in order to improve upon the current oscillator phase noise measurements.

Chapter 5

Feedforward amplifier Oscillator

5.1 Introduction

A feedforward amplifier is an amplifier design that is commonly used to reduce third order intermodulation distortion in communication systems. The amplifier output is sampled into an 'error correction loop' that compares the amplifier output with the input signal to the amplifier. The two signals are combined out of phase so that the noise introduced by the amplifier is isolated as the carrier signal is suppressed. The noise signal is then amplified and subtracted from main signal therefore suppressing the noise introduced by the original amplifier. A block diagram demonstrating the basic operation of a feedforward amplifier is shown in Figure 5.1

It is possible to apply this technique to ultra low phase noise oscillator design however there are few papers presenting measurements of ultra low phase noise oscillators using feedforward amplifier designs. This chapter presents the findings of research into the feedforward amplifier and its use in a low phase noise oscillator operating at 100 MHz. 100 MHz was chosen as the oscillating frequency for this research as a fellow PhD student is developing a low phase noise 100 MHz crystal oscillator and it is easier to precisely tune the phase difference between the error correction loop and the main path due to the longer wavelength at 100 MHz when compared to the wavelengths of the oscillators presented in Chapters chapters 3 and 4.

State-of-the-art residual phase noise measurements of a heavily saturating amplifier with error correction are presented showing at least 10dB suppression of the noise introduced by the main am-

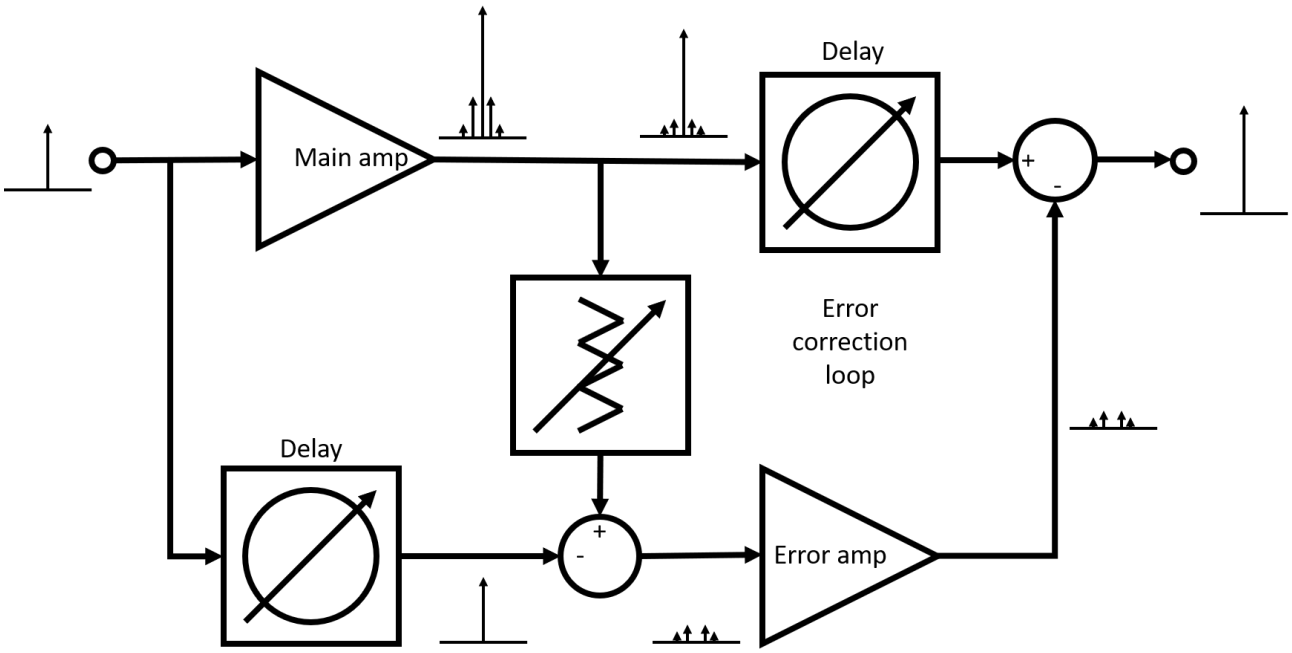


Figure 5.1: Feedforward basic operation principle.

plifier as well as oscillator measurements demonstrating a 20dB suppression of close to carrier noise in an LC oscillator. Furthermore, the design process and equations derived for use in a variable gain feedforward amplifier are presented.

5.2 Current state-of-the-art

The feed forward amplifier was first developed by Black [83] in 1925 as an amplifier linearisation technique and was later used by Seidel [84] in 1971 to reduce distortion in a radio delay system achieving 38dB reduction in third order inter-modulation distortion. The technique has been commonly used since to reduce third order inter-modulation distortion in many modern communication systems but the feedforward amplifier has also been used to reduce flicker noise in GaAs FET amplifiers used in microwave oscillators. GaAs devices offer greater power handling capabilities when compared with Silicon devices and operate at higher frequencies at the expense of increased phase noise at close to carrier frequency offsets.

It has been shown by this research group that the feed forward amplifier can be used in microwave

oscillators to reduce the flicker noise introduced to the circuits by the amplifier. 20dB flicker noise suppression has been achieved in a GaAs based feed forward amplifier with a carrier frequency of 7.6 GHz however, when applied to a high Q oscillator, the flicker noise suppression is reduced by 14dB [2]. It is thought that the cause of this degradation is due to the PIN diode limiters used in the oscillator to prevent the amplifier saturating and therefore increasing gain imbalance in the feed forward amplifier. Gain and phase imbalance between the main and error correcting amplifier reduces the flicker noise suppression of the amplifier and ultimately degrade the oscillator phase noise. PIN diode limiters introduce their own flicker noise to the oscillator that counteracts the suppression produced by the feedforward amplifier. Therefore an amplifier design without the need for PIN diode limiting is required to make use of the maximum flicker noise suppression of the feedforward amplifier.

Third order inter-modulation distortion has been shown to decrease by 31dB by introducing a second error correction loop to the feedforward amplifier by Hornavar et al., [85]. This circuit further linearises the feedforward amplifier for high power design and there is no description of how the introduction of a second error loop affects the system's overall noise figure which is a key parameter to minimise in an ultra low phase noise oscillator.

Automatic alignment of the error correction loop in the feedforward amplifier is possible with the injection of a pilot tone, as demonstrated by Braithwaite [86]. The approach presented in that paper uses a non linear feedback loop that is allowed to oscillate at a frequency outside the carrier bandwidth. The tone is then injected into the feedforward amplifier before the main amplifier and the output tone is measured at the output. From this measurement the tone (and therefore noise) suppression can be determined. The gain and phase of the tone generation feedback loop is determined by the cancellation of the tone. The power of the tone is tracked by the gain of the system and the frequency is tracked by the phase. As the feedforward amplifier works to suppress the injected tone the gain of the tone generator is reduced until oscillation can no longer be sustained and the tone is removed as a result. The removal of the pilot tone once the system has converged is important as residual distortion introduced by the tone is also removed. This system has been shown to reduce out of band power by approximately 30dB at 6.8 MHz offsets from the carrier band. However, this system does not continue to self adjust and allows for variations in the local environment to affect the gain and phase of the error correction loop therefore allowing for possible degradation to the noise

suppression.

An alternative approach to feedforward linearisation is presented by Li et al. in [87], where low pass correlation control is used to control a vector modulator in both the signal and error cancellation loops. Whilst achieving inter-modulation distortion reduction of -68dB, this paper does not present residual phase noise measurements of the system. It is therefore unclear how the close to carrier noise introduced by the main amplifier is reduced. The circuits introduced into the correction loops will likely introduce their own flicker noise components to the feedforward amplifier as well as increase the noise figure. The noise figure of the feedforward amplifier is given by the sum of the losses in the signal and error correction path and the noise figure of the error amplifier (a full derivation is presented in the next section) and it is therefore preferred to include as few components as possible in that path. This keeps the noise figure to a minimum and therefore improves the phase noise performance of an oscillator using the feedforward amplifier.

The feedforward amplifier can operate with some compression in the main amplifier [88] providing the remaining parts of the circuit are well designed however exactly how this is possible is not presented. A 10 GHz dielectric resonator oscillator developed by Hati et al. [89] has shown a 10dB improvement in oscillator phase noise with the feedforward amplifier operating in the saturation region however the design of the amplifier and how much gain compression applied to the amplifier, is not presented.

The aim of this work is to present a technique using variable gain in the feed forward amplifier that can be used in a feed forward oscillator without the need for PIN diode limiters. By allowing the main amplifier to enter saturation, the feedforward technique can then be applied to the oscillator to suppress the introduced AM and PM noise. The error correction loop can then be monitored and adjusted as required to ensure gain and phase imbalances cannot affect the amplifier noise performance and therefore contribute to a degradation in oscillator phase noise.

5.3 Theory of operation

The feedforward amplifier differs from the more common feedback amplifier as two amplifiers are used in the linearisation process. Feedback amplifiers compare the output of a non linear amplifier with the input and amplifies the difference. Feedforward compares a sample of the output of the main amplifier

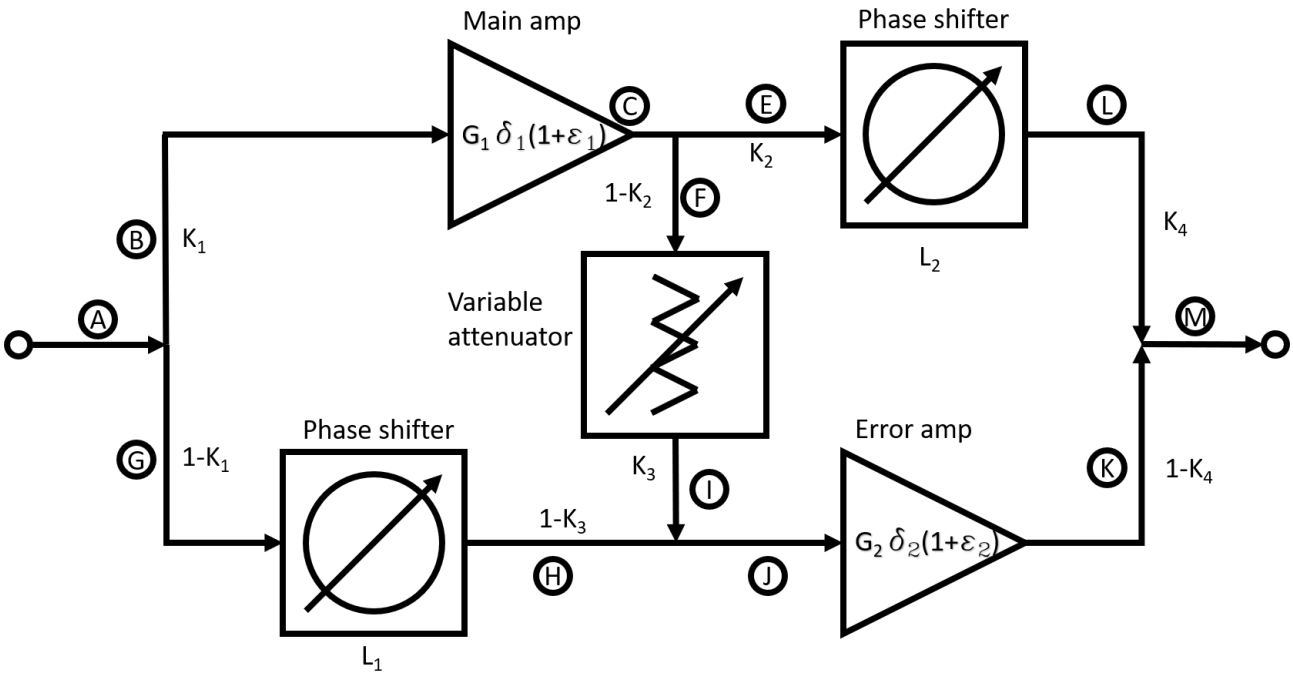


Figure 5.2: Simplified Feedforward Amplifier.

with the input signal and the difference is amplified by a second amplifier. The output of the second amplifier is then compared with the output of the main amplifier and the difference of the two is then produced at the system output. Hence, distortion produced by the main amplifier is removed before the output of the feedforward amplifier.

The signal continuously moves forward through the amplifier allowing this configuration to be unconditionally stable as there is no feedback path. Figure 5.2 shows a simplified feedforward amplifier [17]. In this model, ε_1 is the flicker noise of the main amplifier, ε_2 is the flicker noise of the error amplifier, therefore the modulation of the gain of each amplifier is $(1 + \varepsilon_n)$. δ_1 and δ_2 are the gain and phase balance that ideally is equal to 1. In that case the flicker noise suppression in each loop is given as $10\text{Log}(1 - \delta_n)$ in dB. The coefficients K_n represent the coupling coefficients of the four power dividers/combiners. The coefficients L_1 and L_2 are the losses from the phase shifters.

5.3.1 Phasor analysis and derivation of design equations

For an ideal feedforward amplifier, the gain is defined as follows:

$$G_{FF} = G_1K_1K_2K_4L_2 \tag{5.1}$$

This equation can be used to calculate the gain of the main amplifier and coupler ratios of the couplers in the '(A)(B)(C)(E)(L)(M)' path for a specified gain of the feedforward amplifier or vice versa. In order to achieve maximum flicker noise suppression, the attenuation in path '(F)(I)' and gain of the error correcting amplifier must be determined. The power at point (J), P_J, must contain only the isolated flicker noise introduced from the main amplifier, i.e. the unmodulated input carrier signal must be removed from the 'noisy' signal coming from point (J). Therefore the magnitude of the carrier power at point (H) must equal the magnitude of the carrier power at point (I) and the two signals must be in antiphase. The magnitude of the power P_H is given by:

$$P_H = L_1(1-K_1) \tag{5.2}$$

The power of the carrier signal at point (I) is defined as:

$$P_I = K_1\delta_1(1+\varepsilon_1)G_1(1-K_2)X \tag{5.3}$$

Where X is the attenuation from the variable attenuator. In the ideal amplifier P_I is proportional to P_H:

$$P_I = \frac{1-K_3}{K_3}P_H \tag{5.4}$$

Substituting (5.2) and (5.3) into (5.4):

$$K_1\delta_1G_1(1+\varepsilon_1)(1-K_2)X = \frac{L_1(1-K_1)(1-K_3)}{K_3} \tag{5.5}$$

Rearranging for X and taking the magnitude of the signal at the centre frequency yields:

$$X = \frac{L_1(1-K_1)(1-K_3)}{K_1K_3(1-K_2)G_1} \tag{5.6}$$

We now have an equation for the level of attenuation required to ensure the power at point (I) is equal to the magnitude of the power at point (H). The total power at point (J) can now be calculated:

$$P_J = K_3 P_I - P_H(1 - K_3) \tag{5.7}$$

Substituting (5.5),(5.2) and (5.3) into (5.7), P_J is written as:

$$\begin{aligned} P_J &= L_1(1 - K_1)(1 - K_3)\delta_1(1 + \varepsilon_1) - L_1(1 - K_1)(1 - K_3) \\ &= L_1(1 - K_1)(1 - K_3)\left(\delta_1(1 + \varepsilon_1) - 1\right) \end{aligned} \tag{5.8}$$

The output of the error amplifier is given as:

$$\begin{aligned} P_K &= P_J \delta_2 G_2(1 + \varepsilon_2) \\ &= L_1(1 - K_1)(1 - K_3)\left(\delta_1(1 + \varepsilon_1) - 1\right)\delta_2 G_2(1 + \varepsilon_2) \end{aligned} \tag{5.9}$$

The gain of the error correcting amplifier can be calculated from the magnitude of the total power at point (J), P_L and the magnitude of the amplified noise power ε_1. Signals P_L & P_K must be in antiphase so that the flicker noise introduced by the main amplifier is cancelled.

$$P_K = \frac{K_4}{1 - K_4} P_L \tag{5.10}$$

$$P_L = K_1 K_2 \delta_1 G_1(1 + \varepsilon_1) L_2 \tag{5.11}$$

Substituting (5.11) and (5.9) into (5.10) yields:

$$L_1(1 - K_1)(1 - K_3)\left(\delta_1(1 + \varepsilon_1) - 1\right)\delta_2 G_2 = \frac{K_4}{1 - K_4} K_1 K_2 \delta_1 G_1(1 + \varepsilon_1) L_2 \tag{5.12}$$

The phase noise and balance coefficient are ignored as this equation is to be used to calculate the magnitude of the gain of the error amplifier. Therefore (5.12) can be rearrange for G_2 in terms of the coupler ratios, loop losses and main amplifier gain:

$$G_2 = \frac{K_4 K_2 K_1 G_1 L_2}{(1 - K_4)(1 - K_3)(1 - K_1) L_1} \tag{5.13}$$

(5.13),(5.6) and (5.1) can now be used to design a feedforward amplifier for a specified gain with couplers of any ratio. P_K can now be written as:

$$\begin{aligned} P_K &= \frac{L_1(1-K_1)(1-K_3)(\delta_1(1+\varepsilon_1)-1)\delta_2 K_4 K_2 K_1 G_1 L_2(1+\varepsilon_2)}{(1-K_4)(1-K_3)(1-K_1)L_1} \\ &= \frac{(\delta_1(1+\varepsilon_1)-1)\delta_2 K_4 K_2 K_1 G_1 L_2(1+\varepsilon_2)}{(1-K_4)} \end{aligned} \tag{5.14}$$

The output power of the feedforward amplifier P_M is given as follows:

$$\begin{aligned} P_M &= K_4 P_L - (1-K4)P_K \\ &= K_4 K_2 K_1 G_1 L_2 \delta_1(1+\varepsilon_1) - (\delta_1(1+\varepsilon_1)-1)\delta_2 K_4 K_2 K_1 G_1 L_2(1+\varepsilon_2) \\ &= K_4 K_2 K_1 G_1 L_2(\delta_1(1+\varepsilon_1) - (\delta_1(1+\varepsilon_1)-1)\delta_2(1+\varepsilon_2)) \end{aligned} \tag{5.15}$$

In the ideal case $\delta_1 = \delta_2 = 1$, the amplifier is perfectly balanced. (5.15) simplifies to:

$$\begin{aligned} P_M &= K_4 K_2 K_1 G_1 L_2((1+\varepsilon_1) - \varepsilon_1(1+\varepsilon_2)) \\ &= K_4 K_2 K_1 G_1 L_2(1+\varepsilon_1-\varepsilon_1-\varepsilon_1\varepsilon_2) \\ &= K_4 K_2 K_1 G_1 L_2(1-\varepsilon_1\varepsilon_2) \end{aligned} \tag{5.16}$$

The error amplifier should have a low flicker noise corner as this will reduce the amount of flicker noise modulated onto the output signal. As flicker noise is modulation noise, it is dependent on the signal level it is modulated onto. As the input power to the error correcting amplifier is considerably lower than the input to the main amplifier, the flicker noise introduced by the error correcting amplifier is also small. It is therefore possible to use high power GaAs devices for the error correcting amplifier with minimal degradation to the feedforward amplifier flicker noise suppression. As $\varepsilon_2 \to 0$, 5.16) becomes:

$$P_M = K_4 K_2 K_1 G_1 L_2 \tag{5.17}$$

which is equal to (5.1), the gain of the feedforward amplifier.

5.3.2 Loop cancellation

The loop cancellation can be calculated by considering the carrier signal to have unity amplitude and phase of 0°. The error signal can be modelled with amplitude of $1 + \delta V$ and phase $180° + \varphi$. The

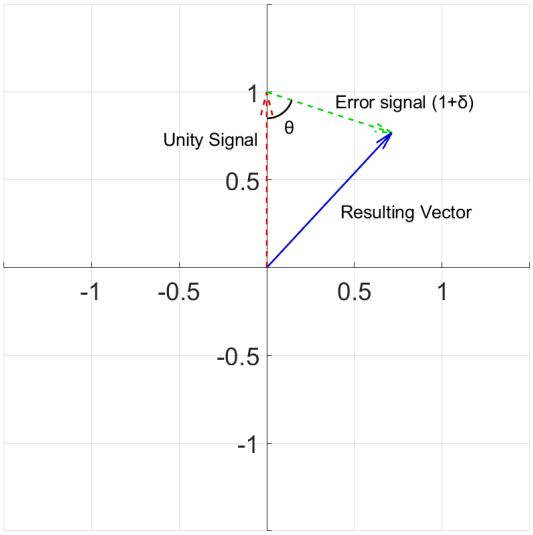


Figure 5.3: Phasor plot of the loop cancellation.

amplitude of the resulting suppressed signal is therefore:

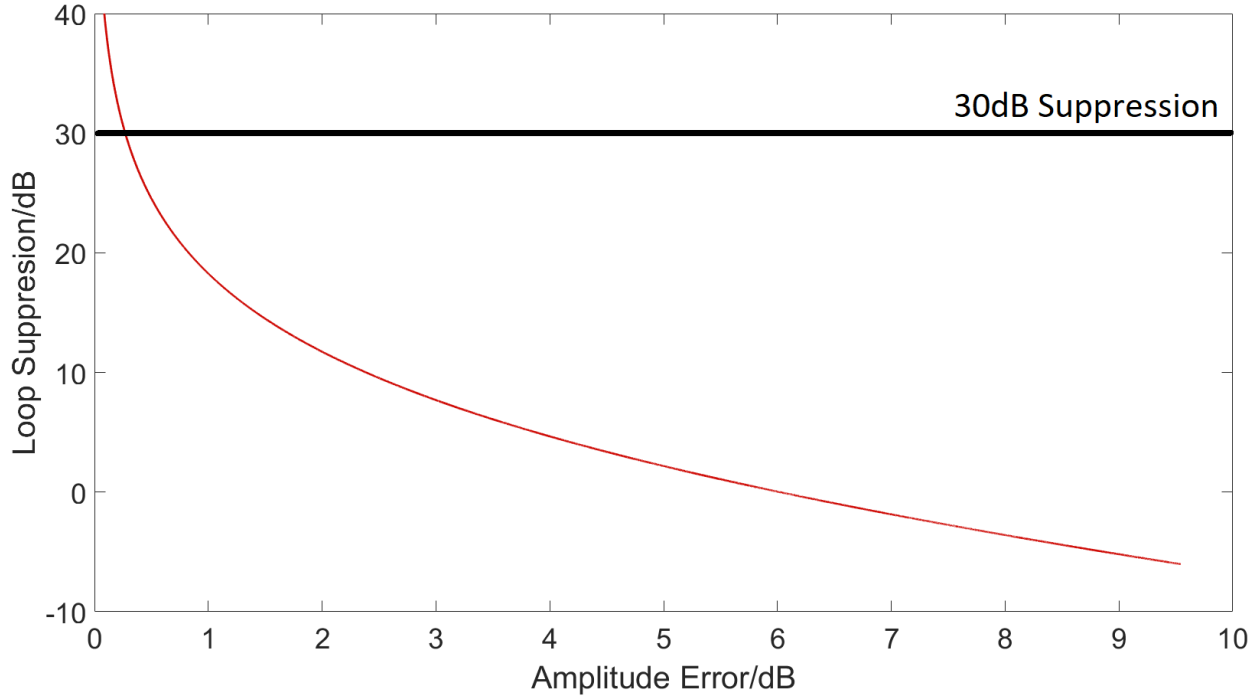
$$A = \sqrt{[1-(1-\delta V)\cos(\vartheta)]^2 + [(1-\delta V)\sin(\vartheta)]^2} \tag{5.18}$$

The cancellation is the inverse of the amplitude:

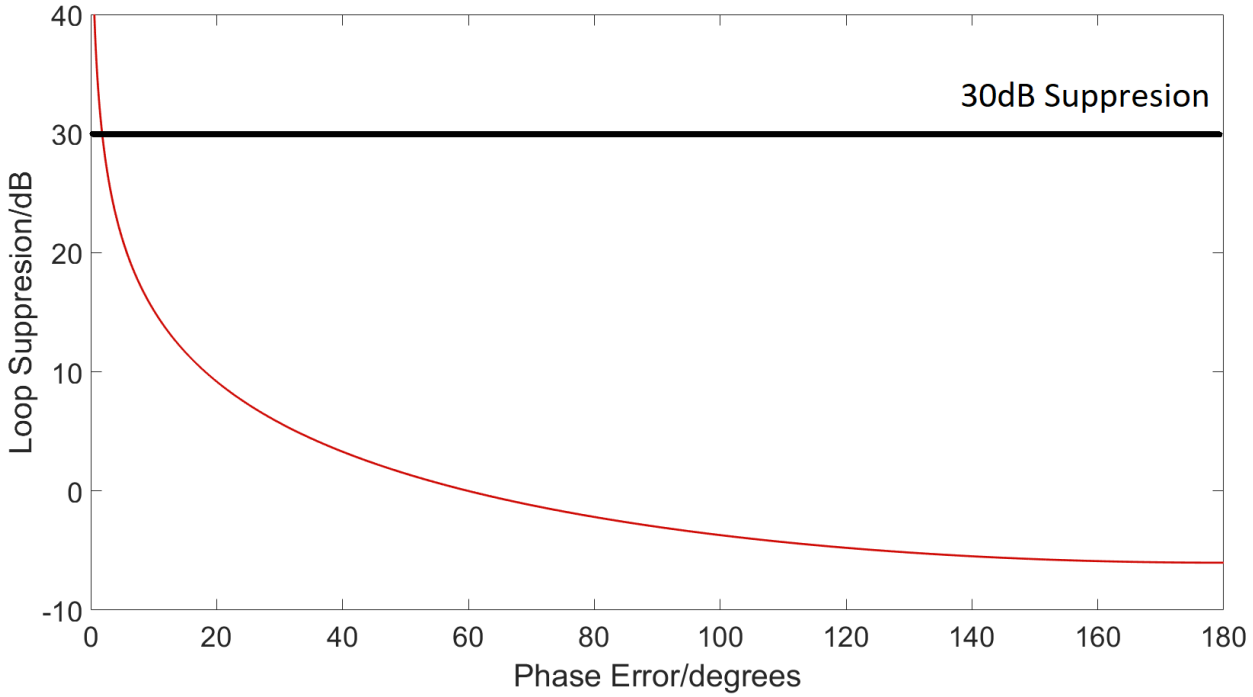
$$C = \frac{1}{\sqrt{[1-(1-\delta V)\cos(\vartheta)]^2 + [(1-\delta V)\sin(\vartheta)]^2}} \tag{5.19}$$

A phasor plot in Figure 5.3 demonstrates how amplitude and phase imbalance affect the error cancellation in the feedforward amplifier. In the ideal case the resulting vector will lie on top of the unity signal on the Y axis as the phase error and amplitude error will both be equal to 0. Figure 5.4 shows the predicted loop cancellation for varying loop phase error and amplitude error from (5.18). These plots were made by plotting this equation for when $\delta = 1$ and $\varphi = 0$ and varying the other parameter.

They demonstrate how precisely the amplitude and phase imbalance must be controlled to achieve high flicker noise suppression. For 30dB suppression, the phase error must be kept below 1.8° plus 0dB amplitude error or the amplitude error must be less than 0.27dB with 0° phase error.



(a) Loop cancellation with phase error =0 and varying amplitude error.



(b) Loop cancellation with amplitude error =0 and varying phase error.

Figure 5.4: Loop cancellation with varying amplitude and phase error.

5.3.3 Noise figure

The signal to noise ratio at the input of the feedforward amplifier is given by (5.20):

$$\mathrm{SNR_{Input}} = \frac{\mathrm{S}}{\mathrm{n_i}} \tag{5.20}$$

Where S is the power of the input signal to the feedforward amplifier and $\mathrm{n_i}$ is the input signal noise power. This is the maximum available noise power for a conjugate match and is defined as the product:

$$\mathrm{n_i} = \mathrm{k} \times \mathrm{T} \times \mathrm{B} \tag{5.21}$$

Where k is Boltzmann's constant, 1.38×10^{-23}, T is the absolute temperature in kelvin and B is the equivalent noise bandwidth in Hertz. The signal to noise ratio of the output signal is given in (5.22):

$$\mathrm{SNR_{Output}} = \frac{\mathrm{G_{FF}S}}{\mathrm{n_e}(1-\mathrm{K_4})} \tag{5.22}$$

Where $\mathrm{G_{FF}}$ is the gain of the feedforward amplifier, $\mathrm{n_e}$ is the noise power produced by the error amplifier and the other terms have the same definition as previously defined. The noise produced by the error amplifier is given as:

$$\mathrm{n_e} = \mathrm{n_i G_2 F_{error}} \tag{5.23}$$

Where $\mathrm{G_2}$ is the gain of the error amplifier, $\mathrm{F_{error}}$ is the noise factor of the error amplifier and $\mathrm{n_i}$ is the input signal noise power as before. The gain of the feedforward amplifier is given in (5.1) this is substituted into (5.22) with (5.23):

$$\mathrm{SNR_{Output}} = \frac{\mathrm{G_1 K_1 K_2 K_4 L_2}}{\mathrm{n_i G_2 F_{error}}(1-\mathrm{K_4})} \tag{5.24}$$

The gain of the error amplifier, $\mathrm{G_2}$ is given in (5.13) which is substituted into (5.24):

$$\begin{aligned} \mathrm{SNR_{Output}} &= \frac{\mathrm{G_1 K_1 K_2 K_4 S L_2}}{\mathrm{n_i F_{error}}(1-\mathrm{K_4})} \frac{(1-\mathrm{K_4})(1-\mathrm{K_3})(1-\mathrm{K_1})\mathrm{L_1}}{\mathrm{G_1 K_4 K_2 K_1 L_2}} \\ &= \frac{(1-\mathrm{K_3})(1-\mathrm{K_1})\mathrm{L_1 S}}{\mathrm{n_i F_{error}}} \end{aligned} \tag{5.25}$$

The noise figure is the ratio of input and output SNRs expressed in dB:

$$\begin{aligned} \mathrm{NF} &= 10\mathrm{Log}\left(\frac{\mathrm{SNR_{Input}}}{\mathrm{SNR_{Output}}}\right) \\ &= 10\mathrm{Log}\left(\frac{\mathrm{S}}{\mathrm{n_i}}\frac{\mathrm{n_i F_{error}}}{(1-\mathrm{K_3})(1-\mathrm{K_1})\mathrm{L_1 S}}\right) \\ &= 10\mathrm{Log}\left(\frac{\mathrm{F_{error}}}{(1-\mathrm{K_1})(1-\mathrm{K_3})\mathrm{L_1}}\right) \end{aligned} \tag{5.26}$$

The noise figure of the ideal feedforward amplifier is given only by the noise produced by the error correcting amplifier and the losses in the bottom path of the system as the noise from the main amplifier is suppressed. Larger values of $\mathrm{K_1}$ and $\mathrm{K_3}$ will keep the noise figure low at the expense of the overall amplifier gain. Therefore, the error amplifier must have a low noise figure to ensure the feed forward system has low noise figure and coupling ratios, $\mathrm{K_1}$ and $\mathrm{K_3}$, must also be kept low.

5.4 Variable gain feedforward amplifier

A PIN diode limiter should not be used to stop the main amplifier in the Feedforward configuration entering saturation. This is due to the additional residual phase noise introduced to the oscillator loop by the PIN diode that can be greater than the residual phase noise introduced by the Feedforward amplifier.

Excess loop gain is required initially but to sustain oscillation the closed loop gain must be one. The amplifier enters saturation if there is no external power limiting and therefore the gain of the amplifier changes. The main amplifier entering saturation causes the gain and phase imbalance between the main and error amplifiers to increase as the error amplifier gain does not also enter saturation. This leads to a reduction in the flicker noise suppression of the feedforward amplifier. The phase shift in the two loops can be adjusted as well as the gain of the error amplifier to account for this and increase flicker noise suppression even when the main amplifier has entered saturation.

The oscillator should be designed in such a way that the gain compression of the main amplifier is known once the oscillator is stable. The gain of the main amplifier in saturation can then be used to calculate required gain of the error correction amplifier and the attenuation from the variable attenuator using (5.5) and (5.13). The loop phase of both the main loop and the error correction

loop must also be modified to account for the different phase shift introduced by the saturating main amplifier. If the oscillator is designed for a known gain suppression in the main amplifier, then the phase shift introduced by the main amplifier in suppression can be measured.

5.5 100 MHz feedforward amplifier

The feedforward amplifier is designed to operate at 100 MHz for use in a 100 MHz crystal oscillator developed at York by this research group. Currently, the 100 MHz crystal oscillator requires an amplifier that can produce 8-10dB of gain with a saturated output power of approximately 0dBm. The feedforward amplifier must therefore produce a gain in this range as well as a low output power to ensure the crystal is not damaged by the saturated amplifier in the oscillator.

5.5.1 Amplifier simulations and Feedforward amplifier simulations

ADS 2020 was used to prove that the equations derived for the gain of the error amplifier, the level of attenuation and the total gain of the feedforward amplifier were correct. Initial simulations used amplifier components from the ADS library and external noise sources to model flicker noise. A simulation was created with an amplifier of 24dB gain with a 1dB compression point of 19dBm and a noise figure of 5dB. The ADS component 'PhaseNoiseMod' was placed at the input of the amplifier to introduce residual phase noise to the amplifier, the flicker noise corner of the noise was set to 50 kHz and the model used for simulation is shown in Figure 5.5, the input power was kept low to ensure linear operation.

The simulated residual phase noise spectrum is plotted in Figure 5.6, simulated flicker noise corner is actually 10 kHz and not 50 kHz. The reason for this decrease is because of the gain and noise figure of the amplifier. The 'PhaseNoiseMod' box has 0dB noise figure however the amplifier component has a noise figure of 5dB. The far from carrier thermal noise is determined from ?(2.62) to be -152dBc/Hz using the amplifier gain of 24dB, noise figure of 5dB and 4dBm power at the amplifier output. The intercept between the $\frac{1}{f}$ noise and the thermal noise therefore appears to decrease because of the increased far from carrier noise.

Using the harmonic balance simulation to sweep the input power, a simulation of the the output

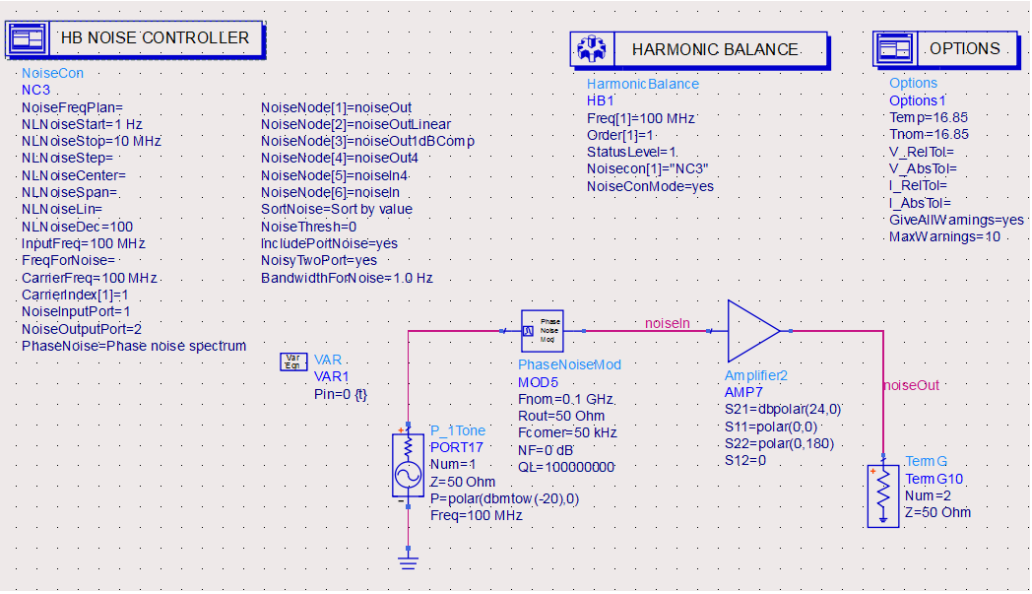


Figure 5.5: ADS harmonic balance simulation of single stage amplifier used to simulate the amplifier residual phase noise.

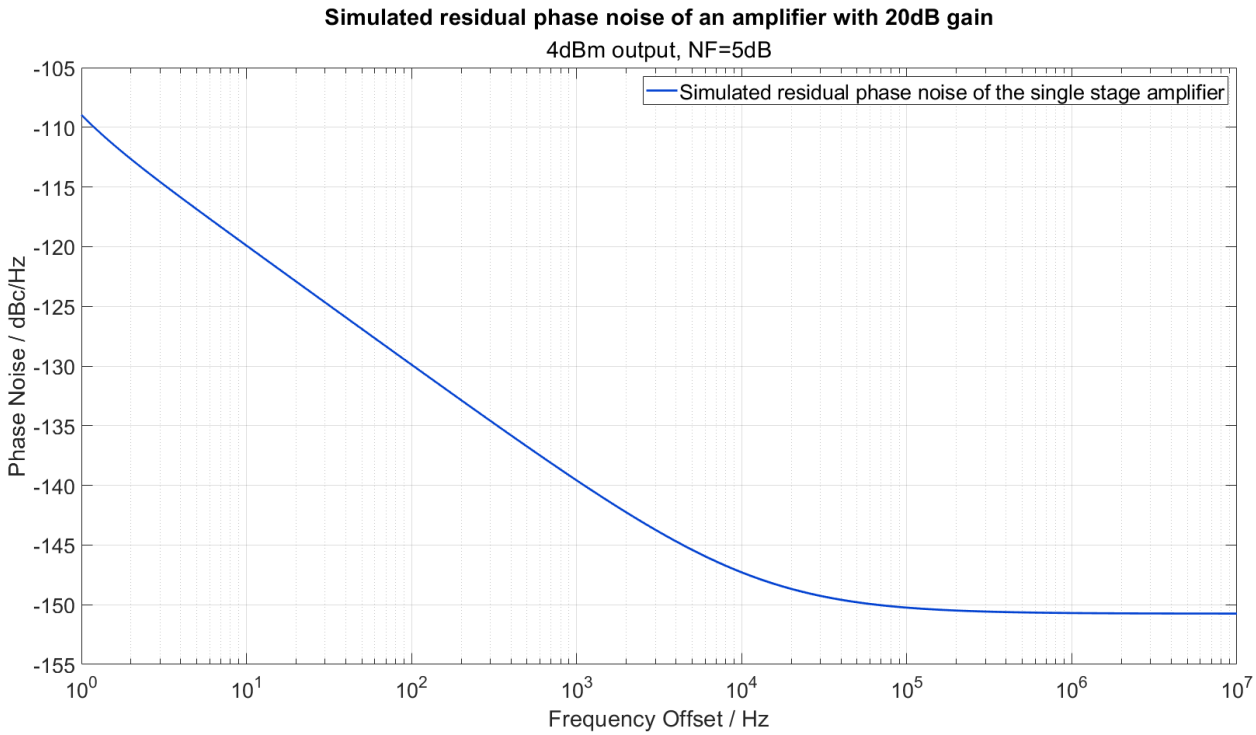


Figure 5.6: Plot of the simulated residual phase noise of the amplifier. The far from carrier noise is -152dBc/Hz which agrees with the theoretical thermal noise floor.

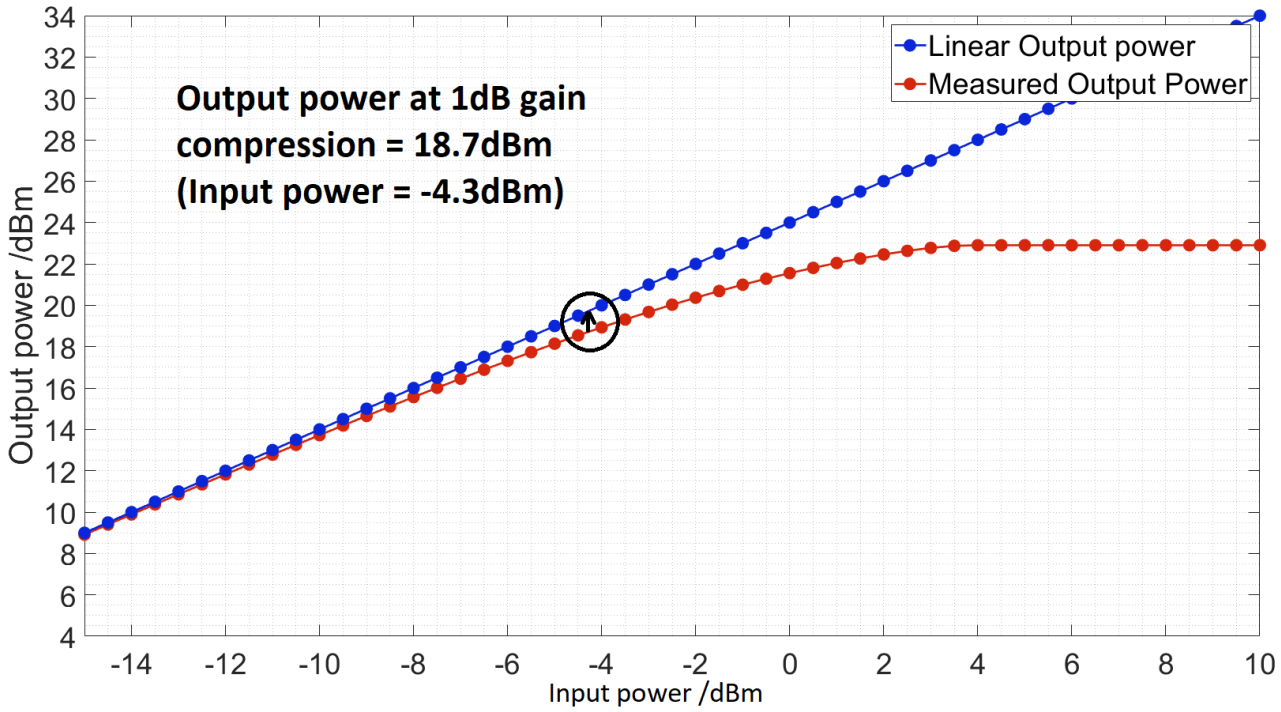


Figure 5.7: The simulated output power with increasing input power of the amplifier and the theoretical linear power increase of the amplifier. The plot shows the output power to be 19dBm in 1dB compression and the saturated power to be 25dBm as expected.

power against input power was made. A plot of simulated input and output power is shown in Figure 5.7 including the theoretical linear power increase with increasing input power. The maximum output power from the amplifier is 25dBm and the output power in 1dB compression is 19dBm which is in agreement with the model settings. A feedforward network was modelled in ADS using the same amplifier and the phase noise mod component. The overall gain is required to be 9dB, therefore the coupler ratios for couplers 1,2 and 4 can be calculated to be 7dB, 1dB and 7dB using (5.13),(5.6) and (5.1). The coupler ratio K_3 is set to 3dB. Using (5.13), and assuming that there are no additional losses in the error loop the gain of the error amplifier must be 13.95dB. The error amplifier has a noise figure of 5dB, therefore the noise figure of the feedforward amplifier can be calculated using (5.26) to be 9dB. The required attenuation is calculated using (5.6) to be 11.1dB.

The feedforward amplifier simulation was set up with the calculated parameters however the error amplifier gain and the attenuation were modified until the residual phase noise plot was flat. If the

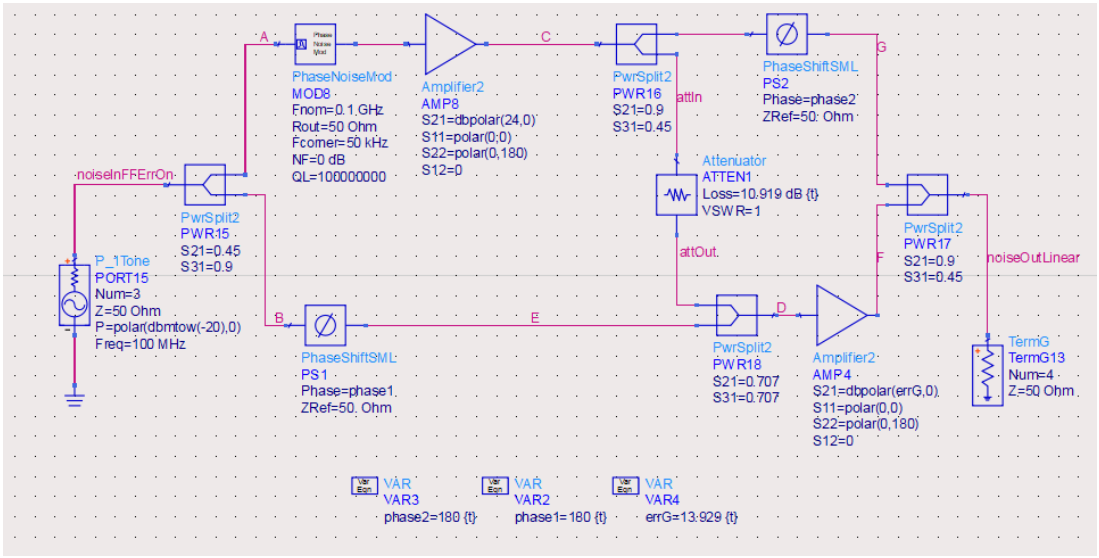


Figure 5.8: Simulation model of the feedforward amplifier. The main amplifier and phase noise modulation block are the same as used in the previous simulation. The error amplifier is the same ADS amplifier model but with a different gain. The noise figure of the error amplifier was kept at 5dB. The coupler ratios are $K_{1,4} = 7\text{dB}$ & $K_2 = 1\text{dB}$ & $K_3 = 3\text{dB}$.

residual phase noise plot is flat then the only noise generated by the feedforward amplifier is thermal noise which is independent of frequency and all noise introduced in the main loop is cancelled. The model used in simulation is shown in Figure 5.8. The amplifiers do not introduce a phase shift which allows for the phase shifters in the main and error loop to both be set to 180° to ensure the correct cancellation of the carrier signal and then the error signal. The tuned values for the attenuator and error amplifier gain are -10.919dB and 13.929dB respectively. A plot of the the simulated residual phase noise is shown in Figure 5.9.

This plot also includes the simulated residual phase noise of the feedforward amplifier with the error amplifier removed from the error correction loop. This was achieved by terminating the error amplifier output in 50Ω and terminating the input to K_4 from the error correction loop with 50Ω. The residual phase noise of the feedforward amplifier with error correction shows a flat response across all frequency offsets. Therefore all noise introduced by the main amplifier has been suppressed and the remaining noise is thermal noise introduced by the error correcting amplifier. The gain of the system is 9dB, the noise figure is 9dB and the output power is -11dBm. The calculated thermal noise from (2.62) is -148dBc/Hz which agrees with the simulation.

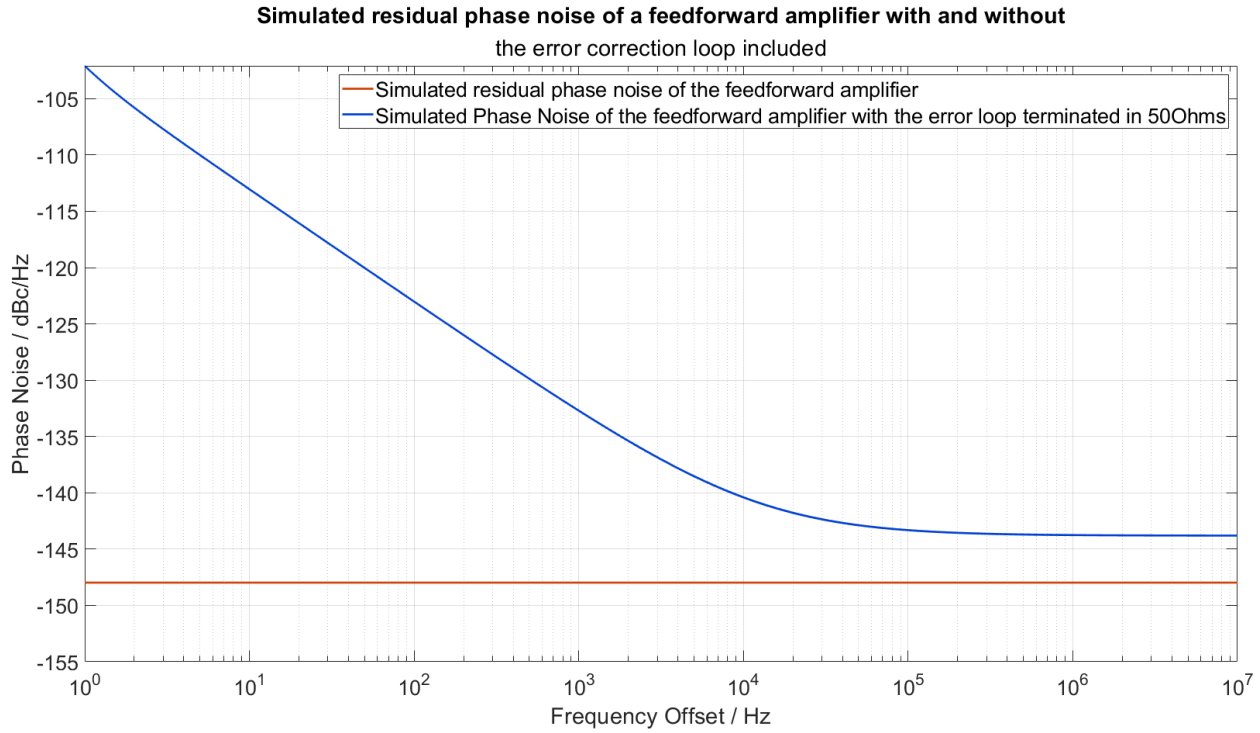


Figure 5.9: Simulated residual phase noise of the feedforward amplifier with the error correction loop correctly designed and a residual phase noise plot of the feedforward amplifier with the error correction amplifier removed. The output of the error amplifier and input to coupler $\mathrm{K_4}$ were terminated in 50Ω to remove the error correction loop.

The other plot shows the residual phase noise plot of the feedforward amplifier without any correction and therefore the residual phase noise introduced by the main amplifier can modulate the output of the amplifier causing the noise side band that is visible in Figure 5.9. The noise figure is no longer dependent of the error amplifier and the couplers in the error path as these components are effectively removed. The noise figure is now dependent on the noise figure of the main amplifier and the coupler ratios in the main path. The signal to noise ratio at the output is now:

$$\mathrm{SNR_{OutputErrorOff}} = \frac{\mathrm{K_2K_4L_2S}}{\mathrm{n_iF_{Main}}} \tag{5.27}$$

where $\mathrm{F_{Main}}$ is the noise figure of the main amplifier. The noise figure of the feedforward amplifier

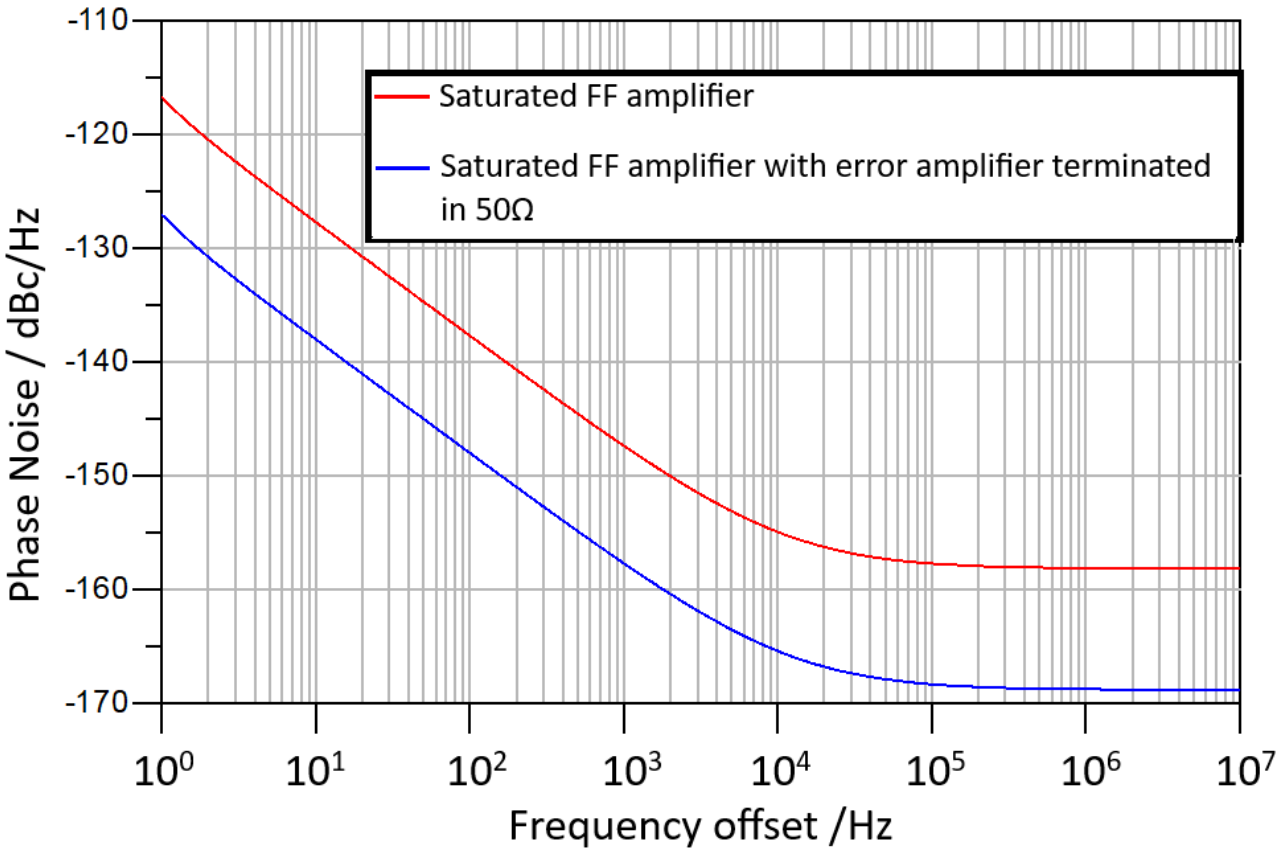


Figure 5.10: Simulated resiual phase noise of the saturating ideal feedforward amplifier. The main amplifier is operating in 3dB gain compression and the overall gain has decreased to 1.942dB.

without the error correcting loop is:

$$\begin{aligned} \mathrm{NF} &= 10\mathrm{Log}\left(\frac{\mathrm{SNR_{Input}}}{\mathrm{SNR_{Output}}}\right) \\ &= 10\mathrm{Log}\left(\frac{\mathrm{S}}{\mathrm{n_i}}\frac{\mathrm{n_i F_{Main}}}{\mathrm{K_2K_4L_2S}}\right) \\ &= 10\mathrm{Log}\left(\frac{\mathrm{F_{Main}}}{\mathrm{K_2K_4L_2}}\right) \end{aligned} \tag{5.28}$$

The noise figure of the FF amplifier without the error correcting amplifier is now 13dB and from (2.62), the calculated far from carrier noise for an amplifier of noise figure 13dB, gain of 9dB and input power -11dBm is -144dBc/Hz which agrees with the simulation. The input power to the feedforward amplifier with error correction was increased such that the input power to the main amplifier caused the device

to saturate and the gain suppression would become 3dB. The input power to the main amplifier must be 1dBm and therefore the input power to the FF amplifier must be 8dBm due to the losses in the input coupler. This input power was calculated from the simulated gain compression measurement used to produce Figure 5.7. A plot of the simulated residual phase noise when the input power is increased to 8dBm is shown in Figure 5.10. This plot also includes the simulated residual phase noise of the feedforward amplifier with 8dBm input power but with the error amplifier terminated in 50Ω.

The plot labelled 'noiseOutLinearErrOff.pnmx' is the simulated residual phase noise of the feedforward system with the error amplifier output terminated in 50Ω with the main amplifier saturating. The other trace, 'noiseOutLinear', is the simulated residual phase noise of the feedforward amplifier with the main amplifier saturating and the error correction loop connected but with the attenuation of 10.919dB and error correction amplifier gain of 13.929dB.

The simulation shows that the feedforward amplifier is no longer cancelling the error signal as the flicker noise corner has increased to 10 kHz which is the flicker noise corner of the main amplifier and the noise modulation source. The simulated feedforward amplifier with the error amplifier removed also shows a 10 kHz flicker noise corner however there is an offset in all of the points of approximately 10.5dB. The far from carrier noise of the feedforward amplifier terminated in 50Ω is -168.766dBc/Hz, the gain is 4.617 and the output power is 14.219dBm. From (2.62), the noise figure of the feedforward amplifier with the error amplifier terminated is 17.836dB. The couplers K_2 & K_4 are 1dB and 7dB. The noise figure of the main amplifier can be calculated by rearranging (5.28) for F_{Main}, which gives a noise figure of 9.836dB.

The far from carrier noise of the feedforward amplifier with the error correction loop connected is simulated to be -158.131dBc/Hz. The simulated gain is 1.942dB and the output power is 9.942dBm, the noise figure of the feedforward amplifier is therefore 26.869dB. The reason for this increase in noise figure when the main amplifier operates in the saturation region is that the error cancelling loop is no longer suppressing the noise introduced by the main amplifier and the noise figure is now dependent on both the noise from the main and error paths. The noise figure is therefore given by the sum of

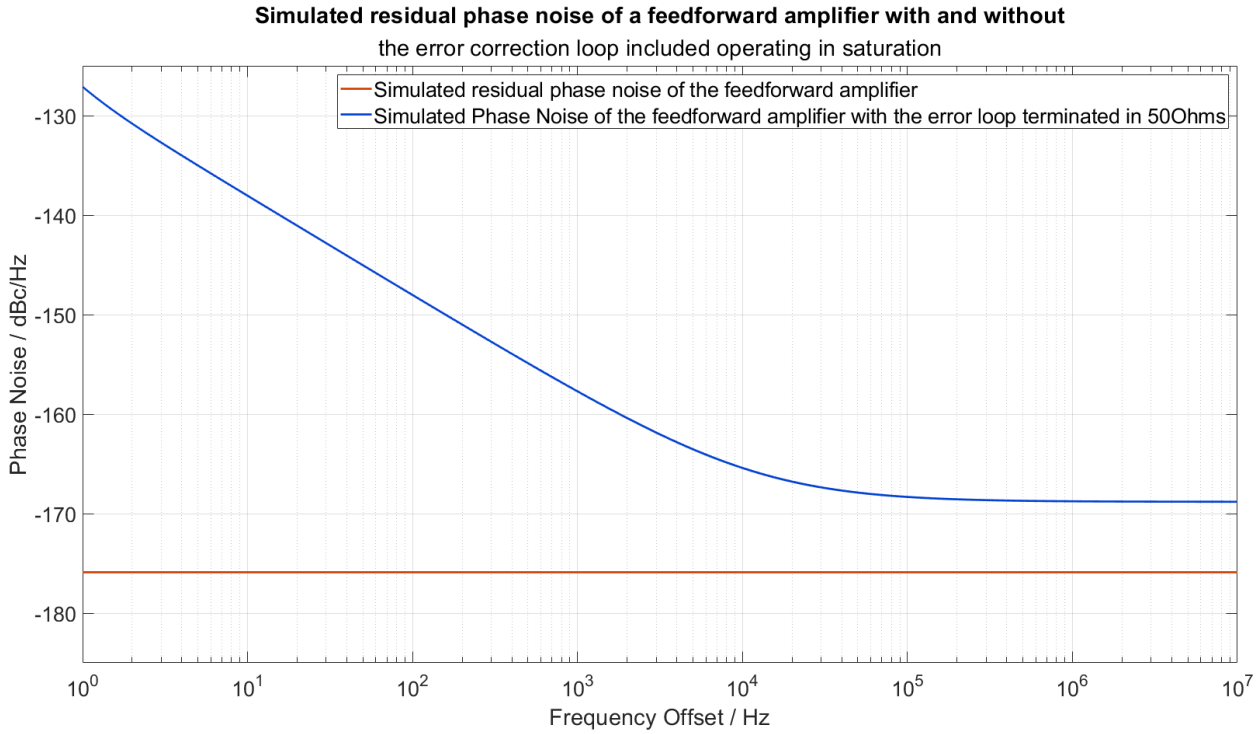


Figure 5.11: The simulated residual phase noise plot of the corrected feedforward amplifier with high input power. The error amplifier cancels the residual phase noise introduced by the saturated main amplifier now that the attenuator and error amplifier gain have been changed.

the noise figures of both :

$$\begin{aligned} \mathrm{NF} &= 10\mathrm{Log}\left(\frac{\mathrm{F_{Main}S}}{\mathrm{n_i K_2 K_4 L_2}}\right) + \\ &\quad 10\mathrm{Log}\left(\frac{\mathrm{F_{Error}S}}{\mathrm{n_i}(1-\mathrm{K_1})(1-\mathrm{K_4})\mathrm{L_1}}\right) \\ &= 10\mathrm{Log}\left(\frac{\mathrm{F_{Main}S}}{\mathrm{n_i K_2 K_4 L_2}} + \frac{\mathrm{F_{Error}S}}{\mathrm{n_i}(1-\mathrm{K_1})(1-\mathrm{K_4})\mathrm{L_1}}\right) \end{aligned} \tag{5.29}$$

which gives a calculated noise figure of 27dB for the saturated feedforward amplifier. In order to cancel the noise introduced by the saturating main amplifier, the gain of the error amplifier should now be recalculated using (5.13).

The coupler ratios have remained the same and the losses L_1 & L_2 are still assumed to be 0 but the gain of the main amplifier has decreased to 21dB. The gain of the error amplifier is therefore 10.95dB. Similarly the attenuation needs to be recalculated, using (5.6) the attenuation must be changed to

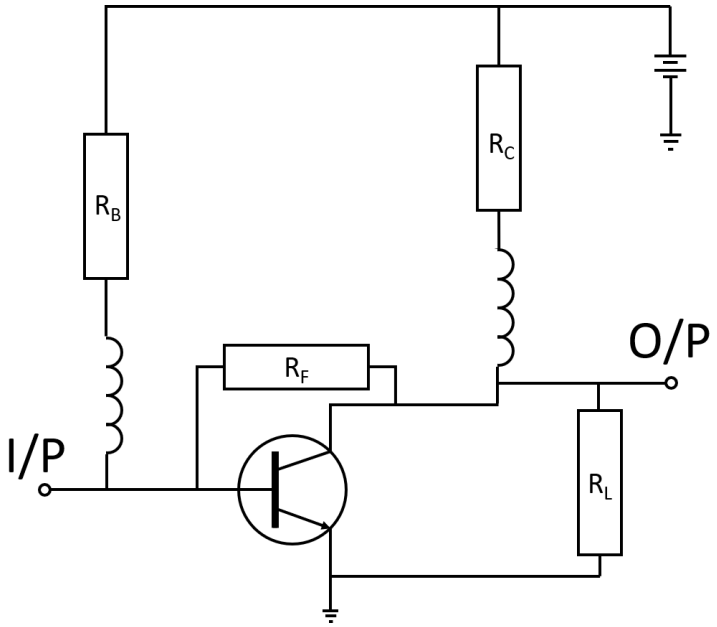


Figure 5.12: Broadband feedback design with biasing resistors and load resistor to ensure the device will remain stable regardless of the connected load. The shunt load resistor can be placed at the input in series though this is generally not preferred as this causes an increase in the noise figure.

8.1dB. The simulation was changed to fit these parameters and the simulated residual phase noise is shown in Figure 5.11.

The feedforward amplifier with correctly defined attenuation, error amplifier gain and phase shift between the loops can suppress the noise introduced by the saturating main amplifier as demonstrated by the flat simulated residual phase noise response of the feedforward system.

These simulations have shown that the error amplifier with variable gain can be used in an oscillator. By setting up the feedforward amplifier gain in the linear region initially, the gain of the error amplifier and the attenuation can be varied as the main amplifier begins to saturate as the closed loop gain of the oscillator approaches one. This simulation has simplified the process by assuming the phase of the amplifiers do not change and has allowed the phase shifters to remain constant, in reality the phase shifters must also be variable so that the carrier signal and the noise are in antiphase at the relevant points in the circuit.

The gain of the error amplifier must be variable in order to ensure the flicker noise suppression of the feedforward amplifier is not degraded by the main amplifier saturation. It must also be able to be

used in a system of characteristic impedance of 50Ω, a broadband feedback design can be implemented to provide a good input and output match by placing feedback resistor from the transistor collector to the base as shown in Figure 5.12.

This diagram includes biasing resistors R_B & R_C, there is no emitter resistor to ground as this has been found to increase the flicker noise in amplifiers. However, a load resistor is placed across the output to ensure the device's input reflection coefficient cannot exceed 1, causing instability regardless of the connected load impedance. Various designs were created and simulated in ADS using SPICE models of suitable transistors, it was found however that the noise figure increases with decreasing gain of the device that ultimately could degrade the residual phase noise of the error amplifier and therefore the feedforward amplifier. It was decided that a simpler approach would be taken with amplifiers available in the laboratory already, by varying the supply voltage.

5.5.2 First FF Iteration

The amplifiers that have been chosen to be used initially are the ZFL-1000VH+ devices from Mini-circuits [90]. This device can offer around 22dB (158x) of gain at 100 MHz with a noise figure of 4.6dB. 4 ZFSC-2-2-S+ [91] 3dB splitters are used in this design. The gain of the error amplifier must therefore equal the gain of the main amplifier in this configuration which can be shown using (5.13) assuming the losses in the phase shifter are negligible:

$$\begin{aligned} G_2 &= \frac{K_4 K_2 K_1 G_1 L_2}{(1-K4)(1-K_3)(1-K_1)L_1} \\ &= \frac{0.5 \times 0.5 \times 0.5 \times G_1}{0.5 \times 0.5 \times 0.5} \\ &= G_1 \end{aligned}$$

In order to allow for dynamic adjustment of the amplifier, the attenuators and phase shifters must be variable. For the phase shifters two ATM P1607 line stretchers [92] with a 90° phase shifter per GHz adjustment were used. At 100 MHz, these can therefore offer a 9 ° tuning range which, despite being narrow, is sufficient for precise tuning of the loop phases.

The attenuator is a Mini-Circuits ZX76-31R75PP-S+ 7 bit digital step attenuator capable of delivering 31.5dB attenuation in 0.25dB increments [93]. The small incremental step size allows for

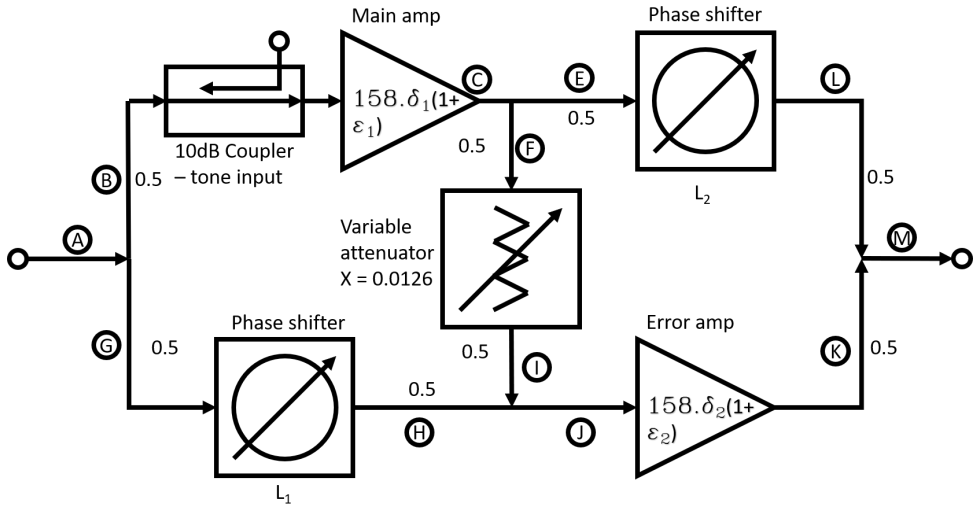


Figure 5.13: Feedforward amplifier design using two ZFL-1000VH+ amplifiers.

precise adjustment of the attenuator to ensure the amplifier gain balance is as close to 1 as possible. It is controlled by an Arduino that uses two buttons, one to count up and one to count down from 0 to 127 and present the binary equivalent of the counter variable to seven output pins. The attenuator is connected to the Arduino via the CBL-5FT-MPD+ control cable recommended by Mini-Circuits. The code for the Arduino used to control this attenuator can be found in appendix A, the user can toggle through the attenuation state using two momentary push buttons and a 4 digit seven segment display will display the value of attenuation the attenuator will introduce, as well as the state of the counter variable.

Using (5.6) and assuming the loss from the first phase shifter is negligible, the required attenuation is 19dB (0.0127x):

$$\begin{aligned} \mathrm{X} &= \frac{\mathrm{L_1}(1-\mathrm{K_1})(1-\mathrm{K_3})}{\mathrm{K_1K_3}(1-\mathrm{K_2})\mathrm{G_1}} \\ &= \frac{0.5 \times 0.5}{0.5 \times 0.5 \times 0.5 \times 158} \\ &= 0.0127 \ (-19\mathrm{dB}) \end{aligned}$$

Initially the actual attenuation of the step attenuator was measured against the programmed state and it was found that there is a constant offset in actual attenuation and the expected attenuation

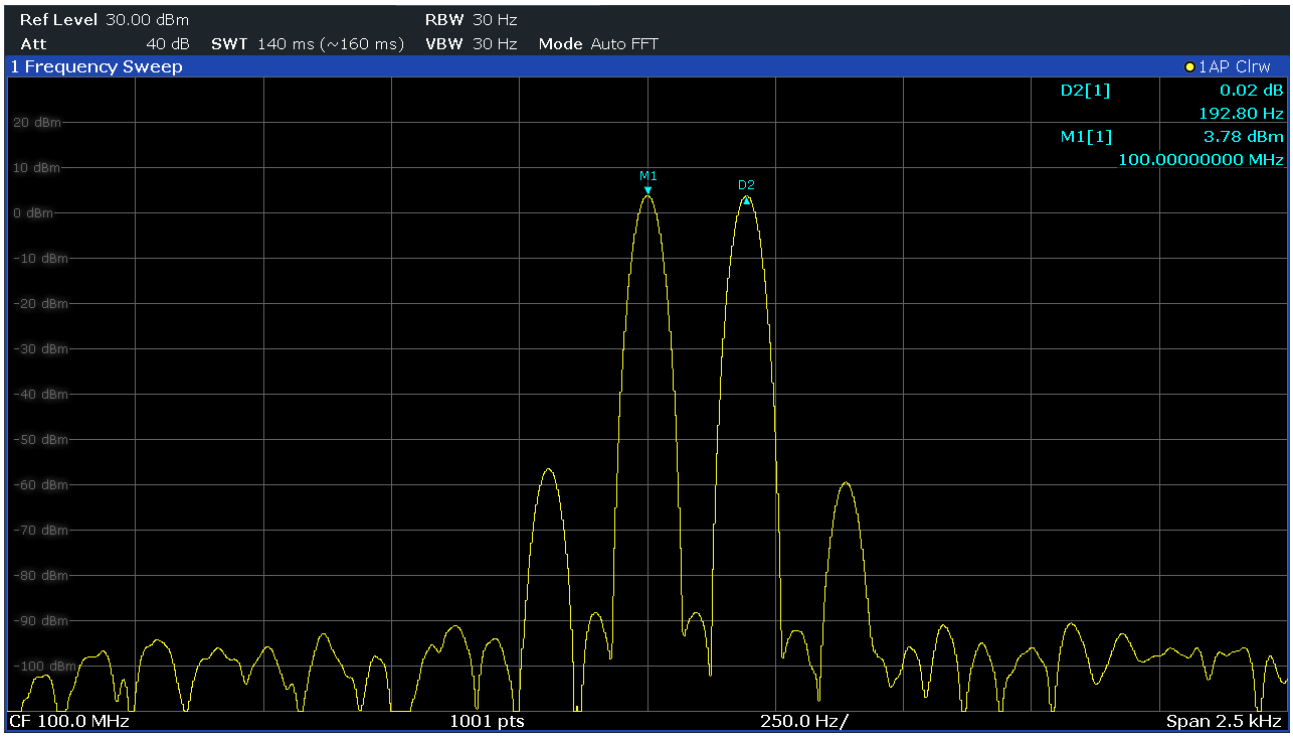


Figure 5.14: Calibration spectrum of the amplifier with the error amplifier output terminated in 50Ω.

for the current state. The value of this offset varies from 1.542 to 1.598dB so a constant offset of 1.57 was programmed into the display code. A block diagram of the first iteration feedforward amplifier is shown in Figure 5.13.

5.5.3 Calibration

The ZFDC-10-5-S+ Directional Coupler [94] from Mini-Circuits is used to apply a calibration tone to the input of the main amplifier. The coupler is inserted backwards before the input of the main amplifier but after the input 3dB splitter so that a signal at a frequency offset from the carrier passes through the main amplifier as well as the attenuating arm. The input splitter must have high output port isolation so that the calibration tone does not propagate into the error path via the first phase shifter. This tone will be suppressed so long as the the inputs to power combiner 3 and 4 are in antiphase and the magnitude of the carrier signal at the inputs to combiner 3 are equal and the magnitude of the noise power at the inputs to coupler 4 are equal.

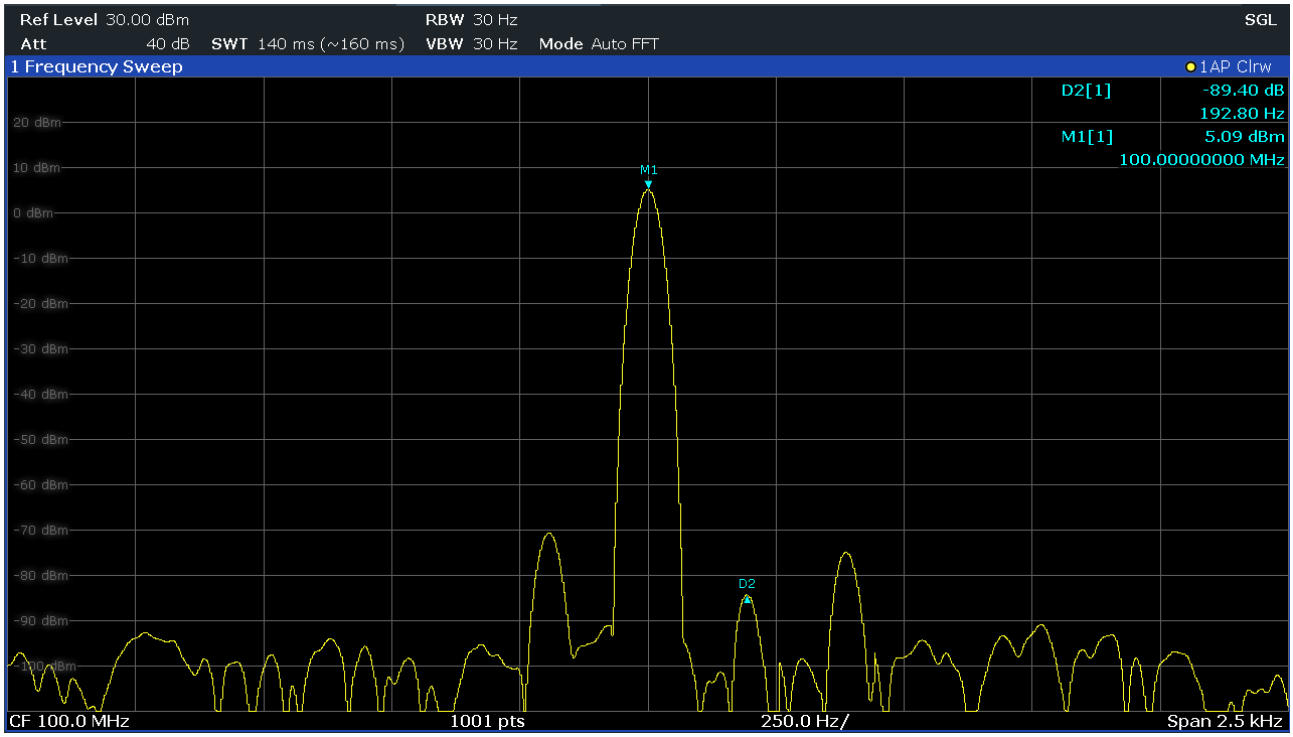


Figure 5.15: Calibration spectrum of the feedforward with error correction.

The magnitude of the tone power should be known and the level of suppression can be calculated from the output spectrum of the system. Using the spectrum analyser mode on the R & S FSWP 50, the level of attenuation and the line stretchers can be adjusted to maximise the suppression of this tone and therefore the close to carrier noise. Figure 5.14 shows the carrier signal at 100 MHz and the calibration tone at 193 Hz offset with the output. The carrier signal amplitude was -7dBm and the calibration tone magnitude was -1dBm as this provided the same power level as the carrier signal at the input of the main amplifier. Therefore the amplitudes of the carrier and calibration tone at the output of the feedforward amplifier are equal.

When operating the feedforward amplifier in the linear regime, it is fine to use a calibration tone of equal magnitude to the carrier. However, when operating the feedforward amplifier in the saturation region the tone power must be much lower than that of the carrier tone as a high power calibration tone can cause the error amplifier to saturate. As the noise power from the main amplifier is very low in amplitude compared with the carrier, the tone power should be kept low.

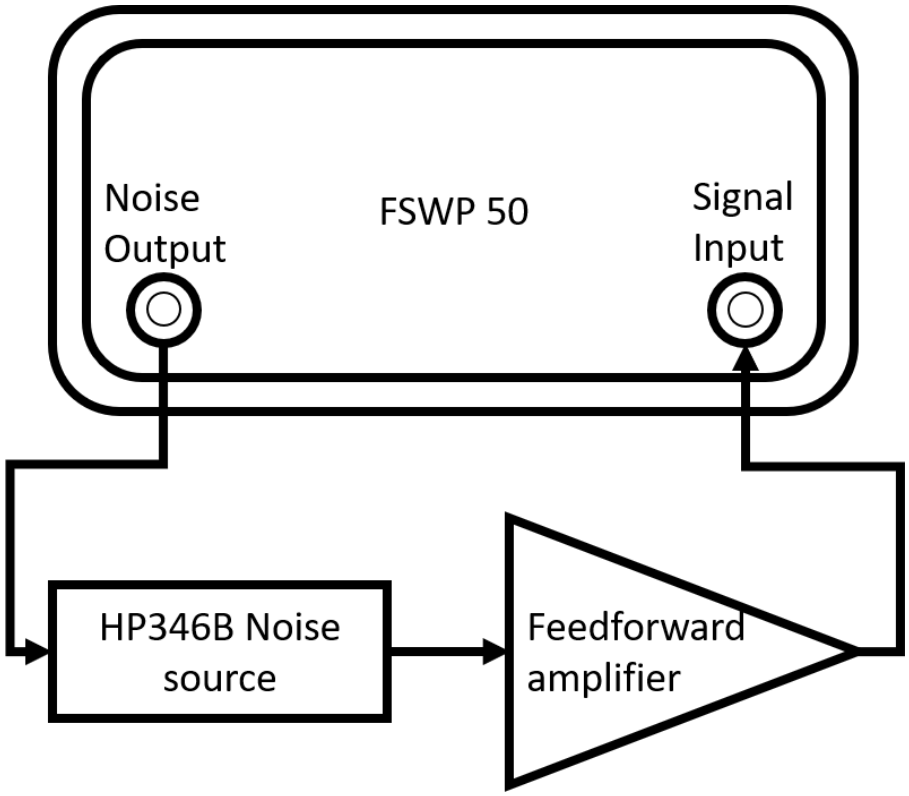


Figure 5.16: Feedforward amplifier noise figure measurement setup using the noise figure measurement mode on the Rohde and Schwarz FSWP 50 phase noise measurement system.

Figure 5.15 is a plot of the output spectrum of the feedforward amplifier with the error amplifier connected into the loop. The calibration tone is suppressed by almost 90dB however as the feedforward amplifier is narrow band the suppression will increase due to thermal variation in the area. It was observed that the suppression decreased to 40dB after a few minutes and settled there.

The gain of the amplifier is 1.2dB lower than expected, when the error amplifier is disconnected from the error loop. This corresponds to the measured loss of the 10dB coupler of 1.281dB. A noise figure measurement of the feedforward amplifier was made using the R & S FSWP 50 in its noise figure measurement mode and the HP346B noise source, the block diagram is shown in Figure 5.16. The measured noise figure is 12.6dB. The theoretical noise figure is 11.3dB and is calculated from using (5.26) where $K_1 = K_3 = 0.478\ L_1$ is assumed to be 0 and the noise factor of the ZFL1000VH is 3.1. The measured value for noise figure is 1.3dB greater than the theoretical value and this is attributed to the additional losses in the error path from the phase shifter and interconnecting coaxial cables. A 1dB

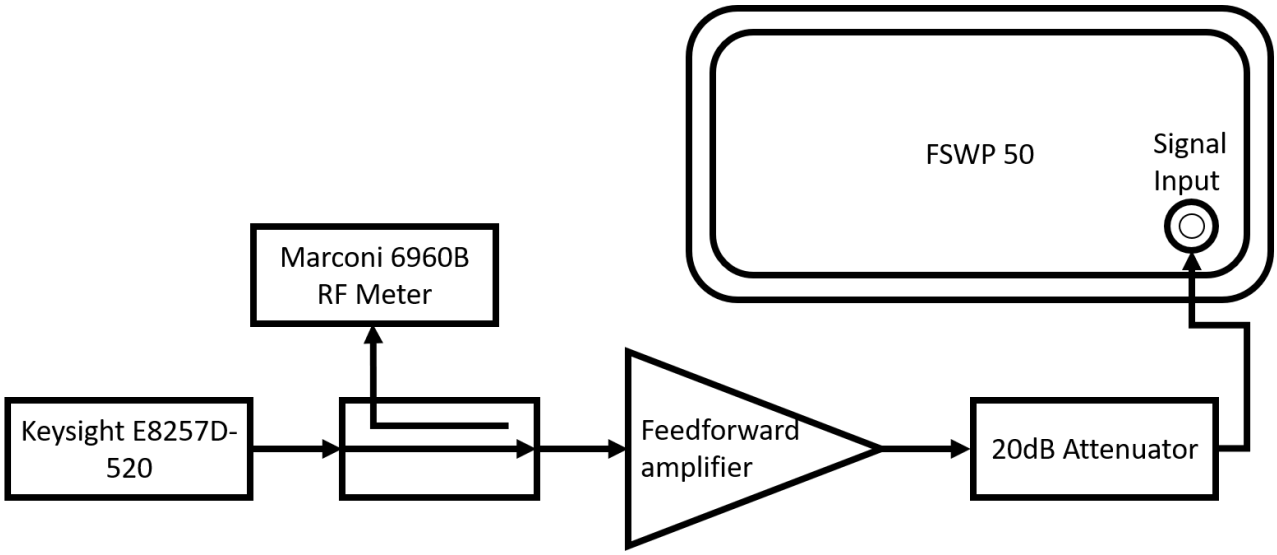


Figure 5.17: Output power at 1dB compression measurement setup.

compression point measurement was made of the feedforward amplifier using the Keysight E8257D signal generator [95], the Marconi 6960B RF power meter [96] and the R & S FSWP spectrum analyser to measure the output power of the amplifier. Figure 5.17 shows the measurement setup where the input signal is sampled via a 10dB coupler to the Marconi power meter and the output power from the feedforward amplifier is measured by the R & S FSWP via a 20dB attenuator. This setup allows for measurement of both input and output power simultaneously. The coupled output from the 10dB directional coupler was measured to be 9.27dB rather than 10dB lower than the input signal and the measured power is 19.77dB lower than the actual power. These offset figures were used in the calculation of the 1dB compression point and all measurements were plotted in Figure 5.18.

From this the output power at 1dB compression is estimated to be 29.4dBm which is too high for use with the crystal resonator as the crystal is rated for a maximum 0dBm input power. Furthermore, this measurement shows that the feedforward amplifier in this configuration can produce output powers of greater than 1W that can damage any of the measurement equipment available. The gain was measured to 12.6dB, whereas the gain of a single VFL1000VH was measured to be 22.8dB. The expected gain of the feedforward amplifier with the coupling ratios used is 13.8dB however the main path introduces an additional 1.2dB due to the loss of the 10dB directional coupler. A residual phase noise measurement was made using the R & S FSWP with an input power to the amplifier of -7dBm,

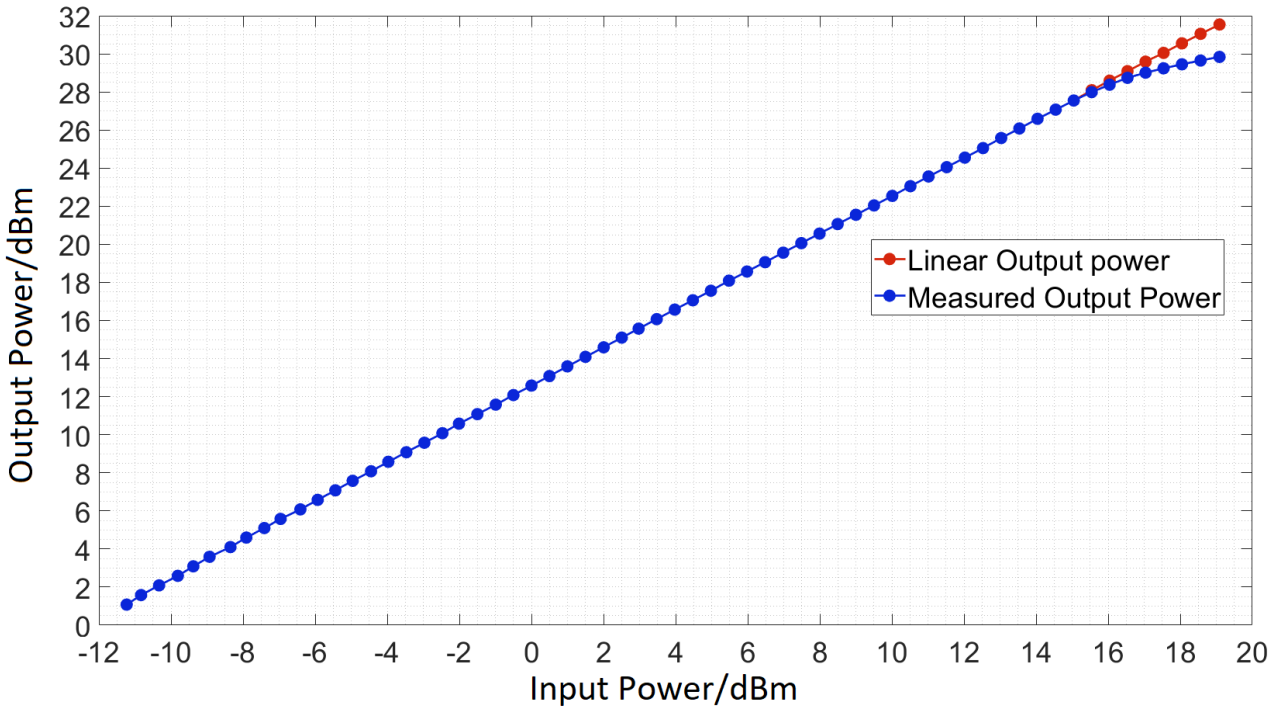


Figure 5.18: Output power at 1dB compression measurement plot.

the input power to the R & S FSWP was 5dBm. Figure 5.19 is a plot of the residual phase noise of the feedforward amplifier and the system noise floor. The input power to the system was 5dBm in both measurements, the resolution bandwidth was 10% and 1000 cross correlations were performed. The amplifier, despite being able to suppress close to carrier noise by 40dB, introduces additional residual phase noise above the noise floor from 20 Hz to 3 kHz. In this band the residual phase noise is almost flat before dropping at a rate of approximately 10dB per decade until the thermal noise dominates the plot noise spectrum. This characteristic is not present in the residual phase noise measurements of the main or error amplifier but was found to be present in a residual phase noise measurement of the digital attenuator.

The digital attenuator residual phase noise was measured in its current state and plotted against the noise floor of the measurement system. The input power to the attenuator was -2dBm as this was measured to be the input power to the device inside the feedforward amplifier. The output power to the R & S FSWP was -5dBm for both measurements and 1000 cross correlations were performed. Figure 5.20 is a plot of the measured residual phase noise of the digital attenuator under these conditions.

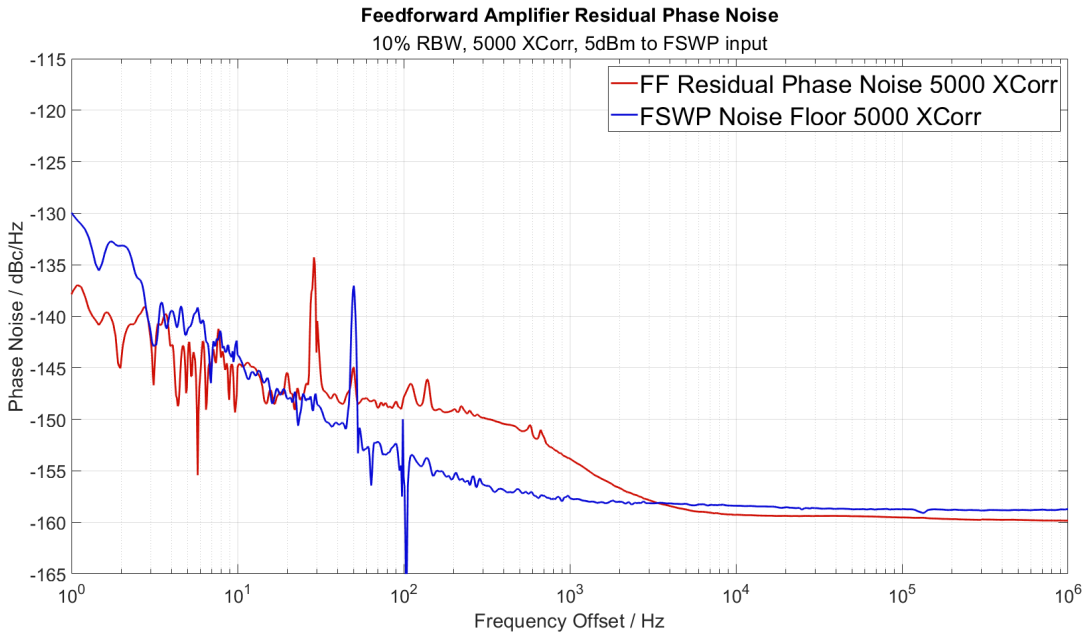


Figure 5.19: Feedforward amplifier residual phase noise.

It is clear that this component introduces the additional noise into the feedforward amplifier but the exact mechanism behind this noise generation remains unknown. Further measurements were made changing the power supply to batteries and decreasing the the supply voltage to the attenuator from 5 to 3.3V, however, the additional noise was still present.

The state of the attenuator was changed so that the smallest attenuation possible was introduced by not switching in any attenuators however the additional noise was still introduced though the noise power was approximately 3dB less in the zero state. Figure 5.20 also has two plots for the 0 state attenuator with differing supply voltages from batteries and shows that the supply voltage and power supply is not the cause of the additional noise and it is in fact inherent in the digital attenuator. The noise figure of the digital attenuator was measured to be 1.24dB in the '0' state with an actual attenuation of 1.2dB, furthermore, in the 10.56dB state the noise figure was measured to be 10.41dB with attenuation of 10.2dB. Using (2.62), the far from carrier noise of the attenuators is -182dBc for both states suggesting that the residual phase noise measurement of the digital attenuator is limited by the far from carrier noise of the measurement system.

As this noise cannot be cancelled in the error correcting amplifier as it is only present in the lower

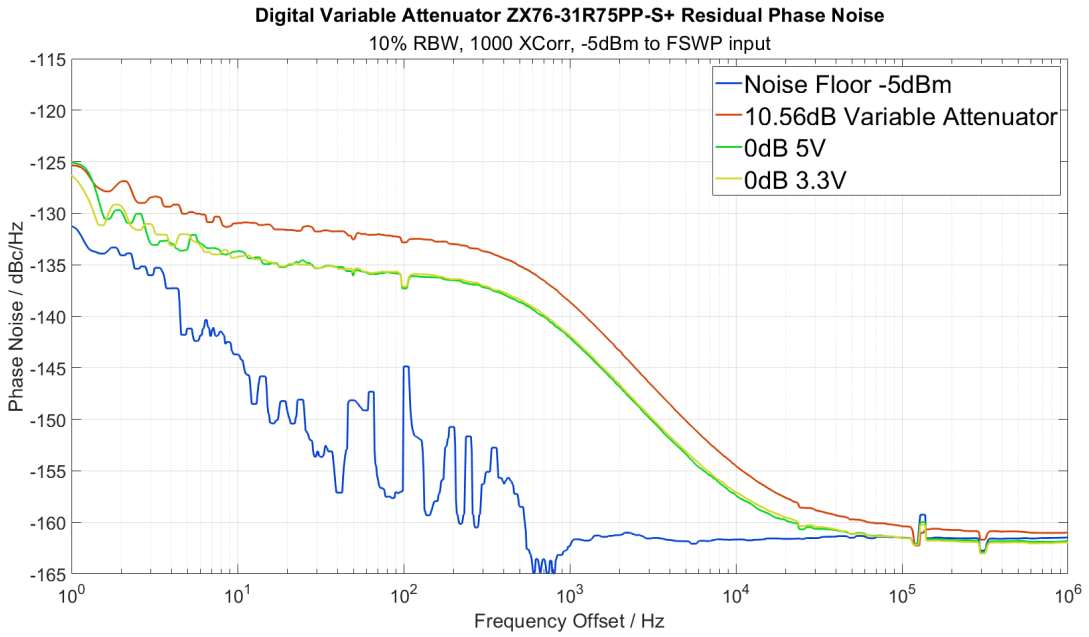


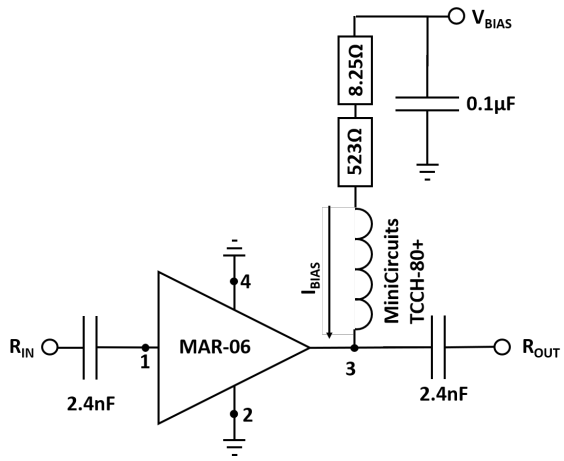
Figure 5.20: Residual phase noise plots of digital attenuator.

error loop path, this noise would be introduced into an oscillator and therefore negate any improvement on residual phase noise achieved through suppression in the feedforward amplifier, therefore an alternative design must be investigated.

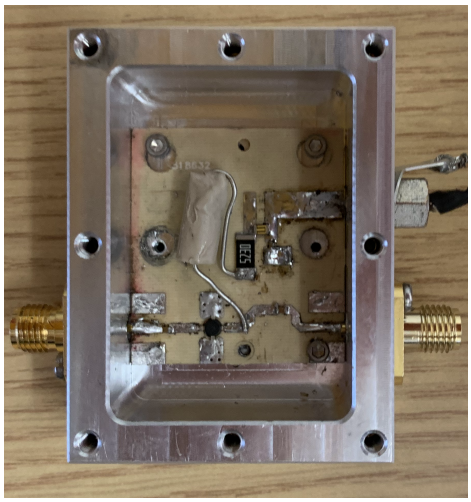
5.5.4 Second Iteration

The two issues with the first iteration of the feedforward amplifier are the excess phase noise introduced by the digital attenuator and the high output power of the ZFL1000VH+ amplifiers. The second iteration includes a switchable attenuator designed by a fellow PhD student, Luke Dummott, that uses resistive π networks for various attenuation levels ranging from 0.1dB to 3.2dB. The six bit design uses relays to switch in the attenuation increments similar to that of the phase shifters used in the 1.5 GHz DRO and within the feedforward amplifier and the theoretical range of attenuation is 0-6.3dB.

It is necessary to replace the main amplifier with a lower output power amplifier whilst also exhibiting a gain of around 20dB. The losses in the feedforward amplifier will decrease the overall gain by 10.2dB and it is therefore necessary to maintain a high gain in the main amplifier to ensure the



(a) MAR06 schematic suggested by the manufacturer.



(b) MAR06 amplifier housed in an aluminium box.

Figure 5.21: MAR-06 schematic as suggested by the manufacturer and the manufactured PCB mounted in an aluminium box. Biasing is via a Filterconn that filters the power lines to remove high frequency interference.

amplifier gain is sufficient for use in an ultra low phase noise oscillator.

MAR-06 amplifier

The MAR-06 from Mini-circuits can provide a gain of 21.8dB at 100 MHz with a low noise figure of 2.3dB, according to the datasheet [97]. The output power in 1dB compression is specified at 500 MHz to be 3.7dBm. The schematic for the amplifiers is shown in Figure 5.21a which is the design suggested by the manufacturer for 'optimum' bias current of 16mA with a 12V supply voltage. PCBs were manufactured using the design available from Mini-Circuits and the amplifier gain, NF and P1dB were measured at 100 MHz using the same methods described in previous sections. The manufactured PCBs were mounted in aluminium enclosures with Tusonix EMI filters [46] on the power line. An image of the MAR-06 amplifier is shown in Figure 5.21b.

The layout and components used were the same as those suggested by the manufacturer except for the Mini-Circuits TCCH-80+ RF chokes, which could never make a reliable connection to the output of the device and hence only provided intermittent biasing current. The suggested choke was replaced with a 2.2µH inductor, the datasheet did not specify the value of inductance that the TCCH-80+

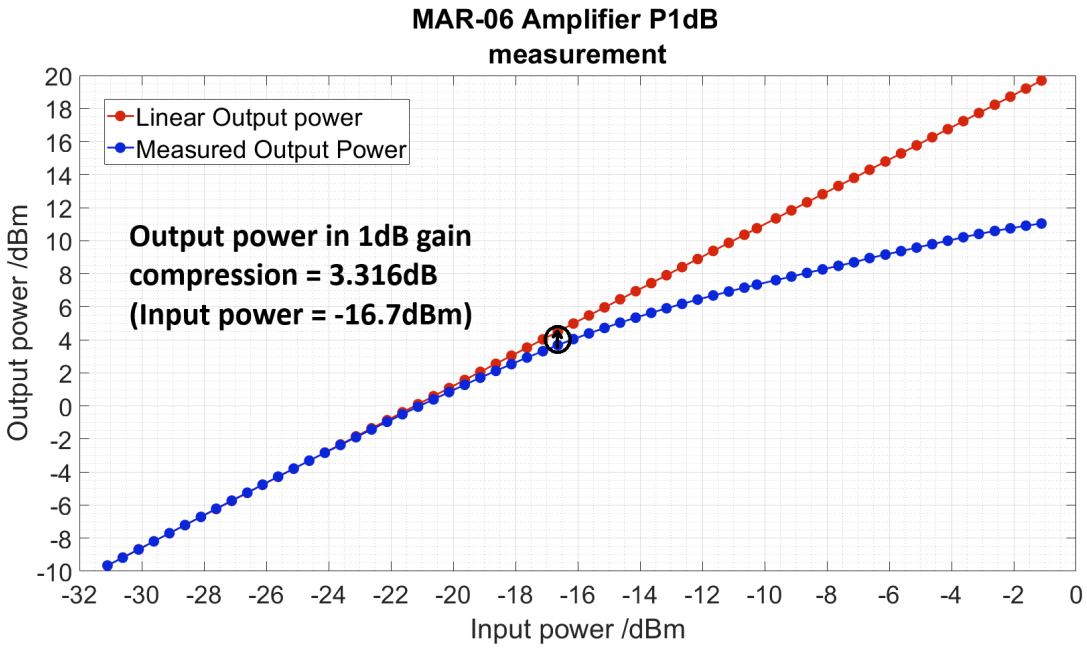


Figure 5.22: MAR06 Output power with increasing input power. The output power at 1dB compression is 3.316dBm.

presents with 16mA current so an estimate based on the data provided was made.

The gain was measured to be 21.44dB, the noise figure was measured to be 2.07 and the power at 1dB output compression was measured to be 3.316dB. Figure 5.22 is a plot of the measured output power with varying input power to the MAR-06 amplifier. There is a plot of the predicted linear gain of the amplifier also in order to calculate the P1dB compression point. The measured 1dB compression point is much lower than that measured using the ZFL1000-VH+ amplifiers which makes the MAR-06 amplifier a better choice for use in the feedforward amplifier as this feedforward amplifier is designed to be used in a 100 MHz crystal oscillator where the input power to the resonator should be in the order of a a few milliwatts.

The error amplifier in the feedforward system must be able to provide variable gain, a measurement of S_{21} at 100 MHz was made using the Anritsu 37377C Vector Network Analyser where the bias voltage to the amplifier was varied. The input power to the amplifier from the network analyser was -20dBm to keep the amplifier in the linear regime. A plot of the gain variation is shown in Figure 5.23, below 6.5V bias the gain became too low to measure. The main amplifier will be biased with 12V at all

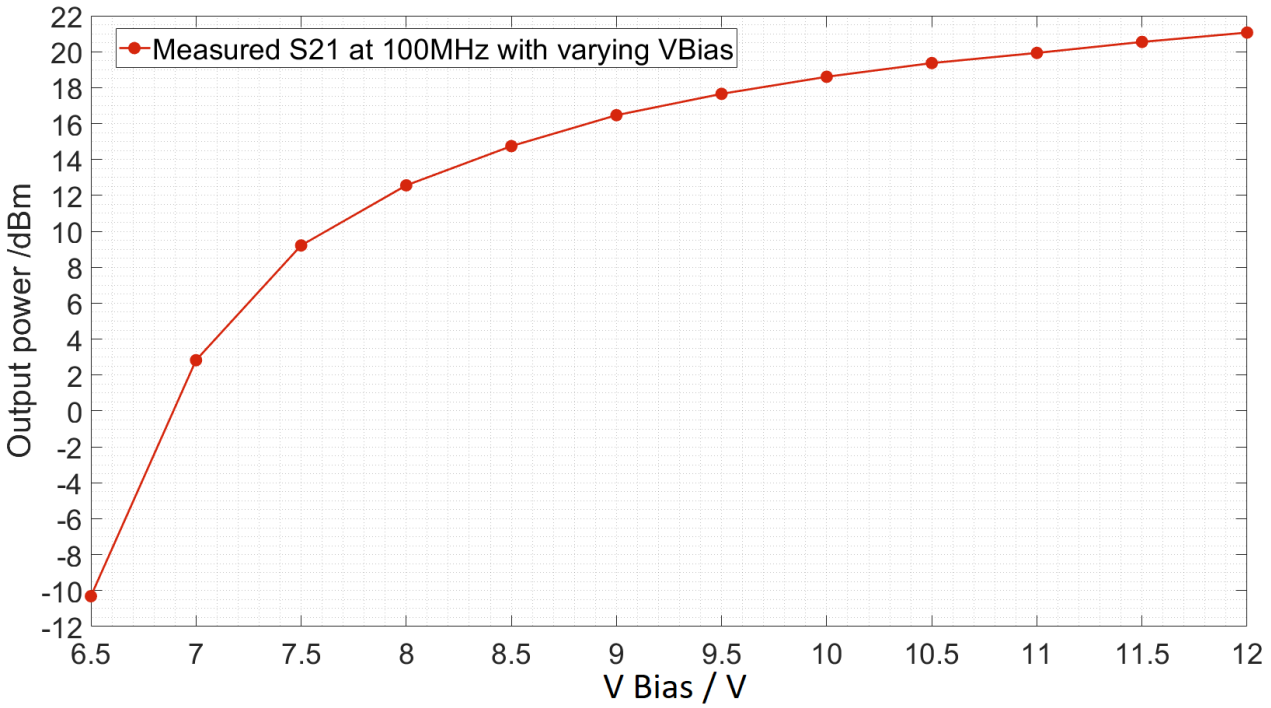


Figure 5.23: MAR06 gain at 100 MHz with varying bias voltage, -20dBm input power.

times, the error amplifier will initially be biased with 12V when the feedforward amplifier is set up for operation in the linear regime. However the bias voltage will be reduced to reduce the gain of the error amplifier once the main amplifier begins to saturate.

This plot shows that the gain of the error amplifier can be reduced to the required level as defined by the level of saturation of the main amplifier and the coupler ratios, by simply reducing the bias voltage. A residual phase noise measurement of the MAR-06 amplifier was made using the R & S FSWP 50 phase noise measurement system in both the linear and saturated regime. An input power to the amplifier of -23.10dBm was used to measure the residual phase noise amplifier of the MAR-06 in the linear regime, a plot of this measurement and the system residual phase noise floor is shown in Figure 5.24. The input power to the R & S FSWP for both measurements was -1.5dBm. From this measurement it is estimated that the flicker noise corner frequency, F_C is approximately 200 Hz. The input power to the DUT was increased to cause it to enter the saturation region and a residual phase noise measurement was also made.

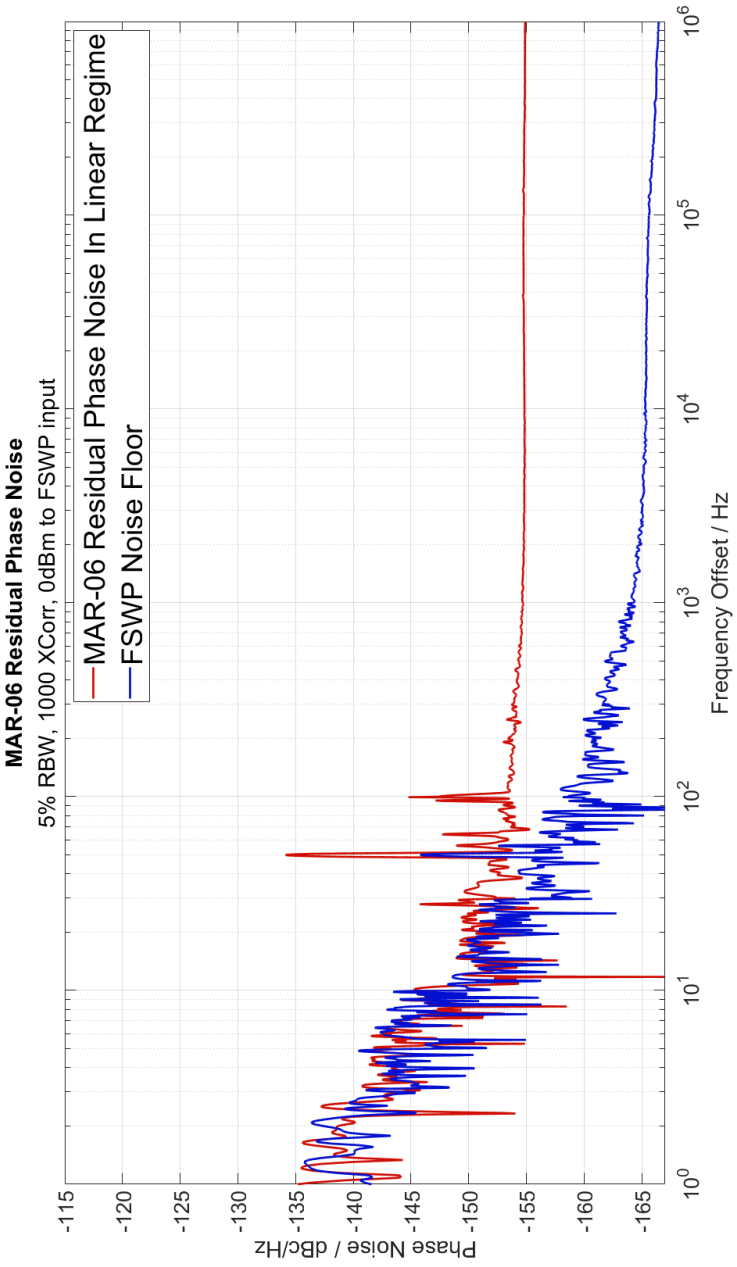


Figure 5.24: MAR06 residual phase noise measurement in linear regime. The input power to the amplifier was -21.4dBm and the power to the input of the R & S FSWP for both measurements was -0dBm. The measurement was run for 1000 cross correlations with a 5% resolution bandwidth.

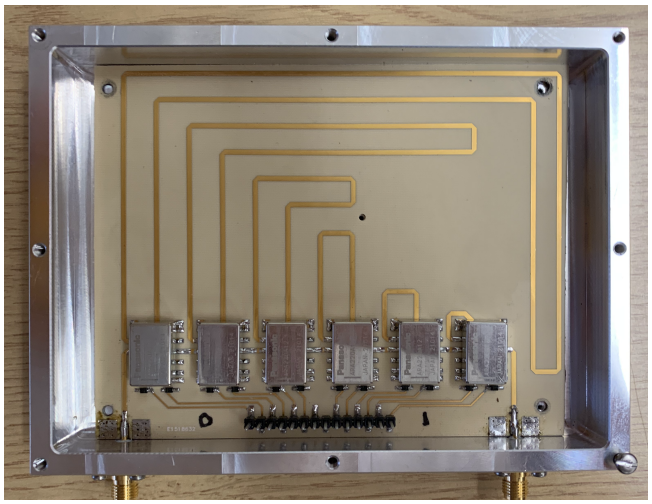


Figure 5.25: Manufactured 100Mhz digital phase shifter housed in an aluminium enclosure. The maximum delay this device can switch in to the circuit is 180°.

Digital Phase Shifter

The phase shifter circuits used in the feedforward amplifier loops are similar the design used in the 1.5 GHz phase shifter from Chapter 3, both the phase shifter discussed here and in Chapter 3 were designed by fellow PhD student Luke Dummott. The design is a six bit variable phase shifter that uses six relays to switch in and out 6 different lengths of the microstrip line to increase or decrease the electrical length of the line the signal passes through, thus adding delay as required by the circuit. At 100 MHz however the electrical length of microstrip lines is much longer than it is at 1.5 GHz for the same delay and therefore the lines required to achieve the same $6°, 12°, 24°, 48°, 96°$ and $192°$ phase shift for the six sections would be 15 times longer. Instead, the 100 MHz phase shifter was designed to be a 6 bit phase shifter as before except providing up to 180° of phase shift in 2.8125° increments. The schematic for the 1 bit phase shifter is the same as the schematic in Figure 3.12a. The 6 bit phase shifter comprises of six of these sections connected in series. The electrical length of the six microstrip lines are $2.8125°, 5.625°, 11.25°, 22.5°, 45°$ and $90°$ calculated (3.14).

Two of these circuits were manufactured and were both housed in an aluminium enclosure, as shown in Figure 5.25. The measured phase shift and insertion loss vs the binary state is plotted in Figure 5.26. The measured phase shift decreases linearly with increasing state number and the insertion loss varies between 0.1 and 0.45dB. The variation in insertion loss is small and generally

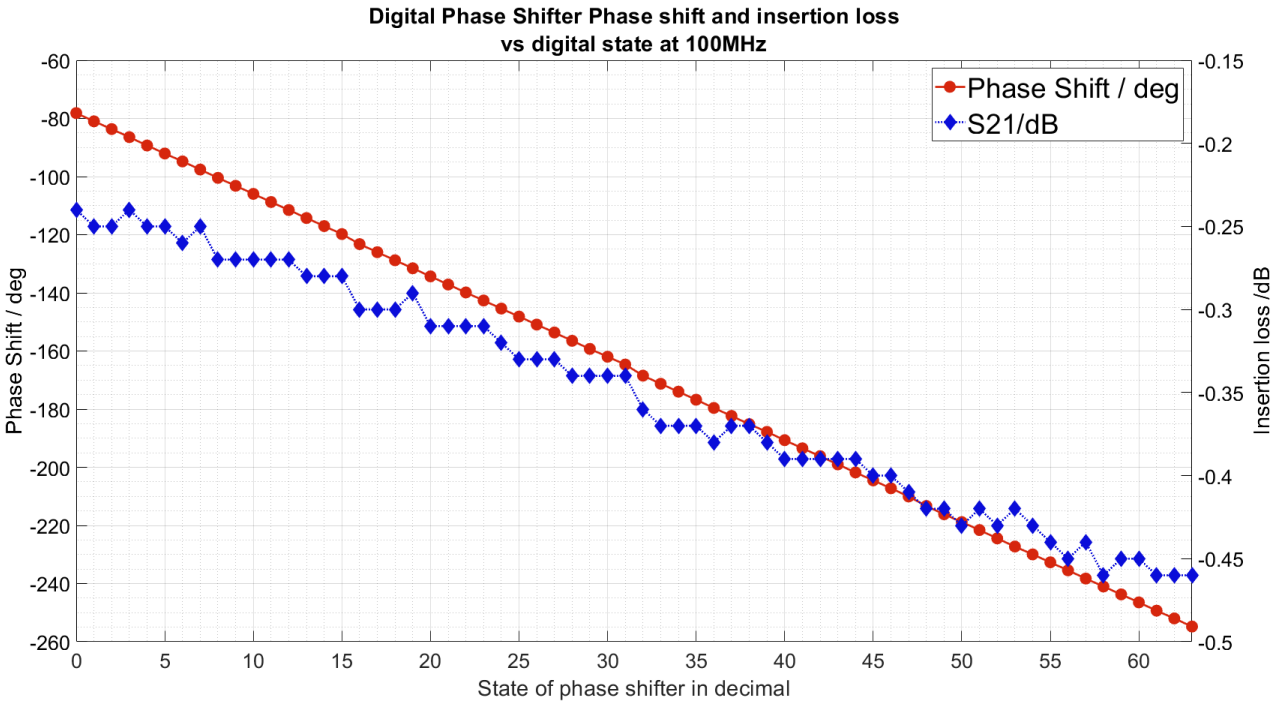


Figure 5.26: 100 MHz phase shifter phase shift and insertion loss plotted against the decimal state of the device.

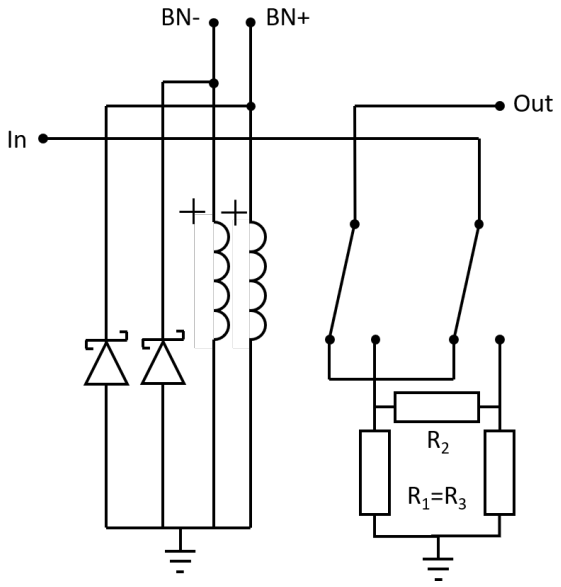


Figure 5.27: 1 Bit digital attenuator design, 6 1 bit sections can be connected in series to increase the attenuation. The resistive π networks provide attenuation from 0.1dB to 3.2dB where the previous section presents half the attenuation of the current one so that the attenuator can be controlled with a binary input, similar to the phase shifter design.

follows a linear increase as the state number increases. As an increased number of microstrip lines (and therefore binary bits set to 1) increases, then the insertion loss also increases. It is possible for the insertion loss to decrease when there are large changes in the number of bits set to 1.

Digital Attenuator

In addition to using the MAR-06 amplifier in place of the ZFL1000VH+ amplifiers, the second iteration of the feedforward amplifier incorporates a digital attenuator in place of the MiniCircuits ZX76-31R75PP-S+ step attenuator. The design of the digital attenuation is a modified digital phase shifter, it uses 6 relays to switch in and out different paths for the propagating wave. However, the lengths of microstrip line used to introduce additional phase are replaced with 6 resistive π networks presenting attenuation of 0.1dB, 0.2dB, 0.4dB, 0.8dB, 1.6dB and 3.2dB. The attenuation is doubled each time so that the attenuator can be controlled with a binary input. The design criterion for the digital attenuator was not to be able to produce a wide range of attenuation but rather to be able to make as small increment as possible to the attenuation presented. The feedforward amplifier components

Bit number	Attenuation/dB	R_1&R_3/ Ω	R_2 / Ω
0	0.1	8660	0.56
1	0.2	4320	1.1
2	0.4	2200	2.2
3	0.8	1100	4.7
4	1.6	549	9.1
5	3.2	274	19.1

Table 5.1: Calculated resistor values for the π Networks used in the digital attenuator. The attenuation of each stage is double that of the previous stage to allow for a binary code to be used to change the attenuation.

have been designed to work in 50Ω system so therefore the π networks must also be designed for this. The π networks should also present 50Ω in both the forward and reverse direction, therefore the two shunt resistors are equal. (5.30) and (5.31) taken from [98] can be used to calculate the values of the resistors in the π network:

$$R_1 = R_3 = \frac{1}{\frac{10(\frac{K2^n}{10})+1}{Z_0(\frac{K2^n}{10}-1)} - \frac{1}{R_2}} \tag{5.30}$$

$$R_2 = \frac{1}{2}(10^{\frac{K2^n}{10}} - 1)\sqrt{\frac{Z_0^2}{10^{\frac{K2^n}{10}}}} \tag{5.31}$$

Where K is the attenuation of the smallest attenuation of the entire series of attenuators in linear form, Z_0 is the characteristic impedance and n is the bit number. The calculated values for the six attenuator sections are contained in table 5.1. These values have been calculated using equations eqs. (5.30) and (5.31) for characteristic impedance of 50Ω. The manufactured attenuator is housed in an aluminium enclosure as shown in Figure 5.28. A series combination of a 10dB attenuator, the digital attenuator and a Texscan 0-10dB rotary attenuator was used in the attenuation arm of the feedforward amplifier as the digital attenuator was designed to attenuate the signal in 0.1dB increments, the maximum attenuation was 6.3dB. Therefore an increased total amount of attenuation was required. The same 3dB couplers are used as before (3 ZFSC-2-2-S+ splitters with S_{21} = –3.2dB) and with the main amplifier gain of 21.44dB from the MAR-06, the value of attenuation required is calculated to be 17.87dB using (5.6). The rotary attenuator was set to present 6dB attenuation and therefore the digital attenuator can be adjusted to provide the remaining attenuation required to within 0.05dB.

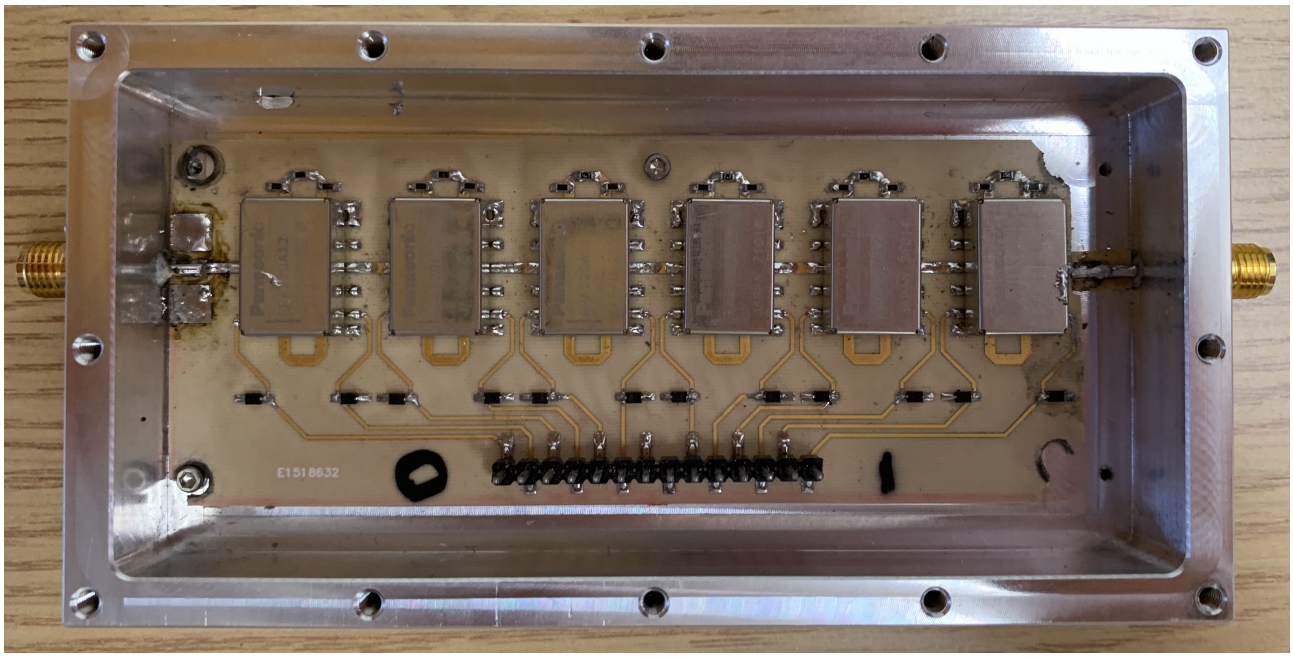


Figure 5.28: Manufactured digital attenuator housed in an aluminium enclosure.

Complete MAR-06 Feedforward Amplifier

The second iteration feedforward amplifier was assembled using the MAR-06 amplifier for both the main and error amplifier, the series combination of the 10dB, rotary and digital attenuator, and the digital phase shifters. As with the first iteration, three ZFSC-2-2-S+ splitters and one ZESC-2-1 were used for couplers K_{1-4}. The ZFDC-10-5-S+ directional coupler placed in the reverse direction after the input power divider was retained but in the second iteration a further ZFDC-10-5-S+ was used in the forward direction to couple the output of coupler K_3. This allows for constant monitoring of the carrier suppression using a spectrum analyser without the need to break the feedforward amplifier loop to measure the suppression. The carrier power can be measured at the input to coupler K_3 in advance and from the measured output, the suppression can be calculated.

The complete feedforward amplifier schematic is shown in Figure 5.29 and Figure 5.30 shows the assembled feedforward oscillator. The individual circuits are mounted in aluminium boxes however in this image the lids have been removed to allow for tuning. The complete network is also placed within a shielded box to remove unwanted interference during the residual phase noise measurements. There are two SMA through ports to allow for the input and output power to pass through the shielded

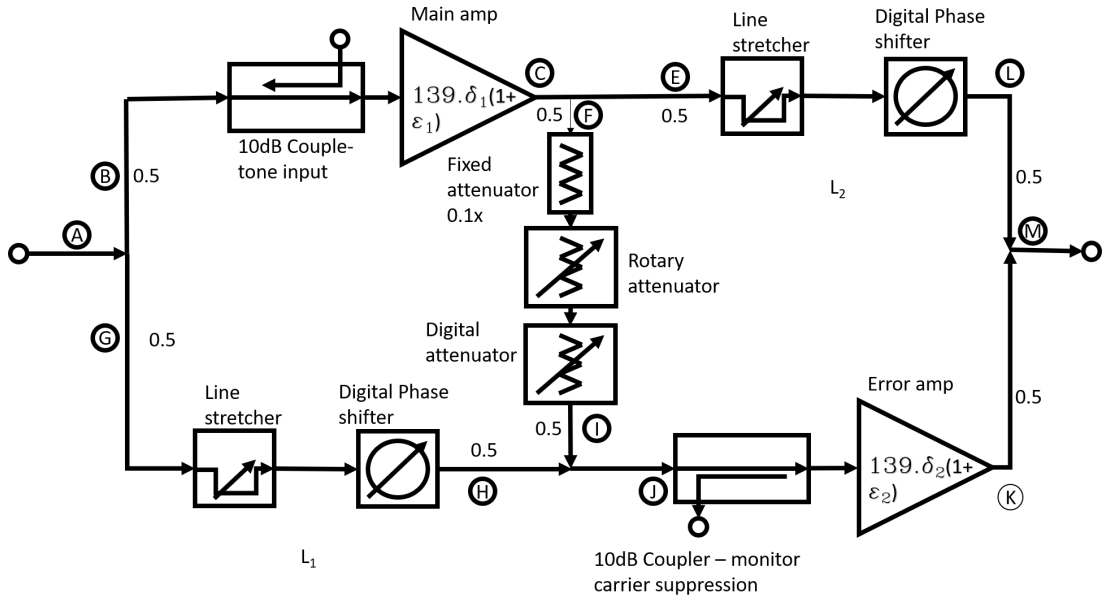


Figure 5.29: Complete feedforward schematic with MAR-06 amplifiers, digital attenuation and digital phase shifting.

walls as well as holes to allow for the bias voltage for the amplifiers to pass through. The amplifiers must be powered by a variable power supply to allow for precise tuning of the feedforward amplifier.

Calibration of the feedforward amplifier in the linear regime

The first set of measurements of the second iteration of the feedforward amplifier were made with a low input power to ensure the main amplifier would not saturate. The input power to the whole system was kept at a constant -20dBm for these measurements, the input power to the amplifier was measured to be -25.9dBm and therefore the expected main amplifier gain is approximately 21.4dB. The power at point (H) was measured before the main amplifier loop was connected, this value was -26.1dBm. Using (5.6), the attenuation between points (F) and (I) was calculated to be 17.8dB, assuming there are no losses in the phase shifting path. In reality there are losses but as the required phase is unknown the exact amount of loss in also unknown. The power at point (I) was reduced to as close to -26.1dBm as possible before the loop was closed and the output of the 10dB direction coupler at point (J) was connected to the Agilent E4404B spectrum analyser [99].

The phase shifter was adjusted until the 100 MHz carrier was at its smallest on the spectrum

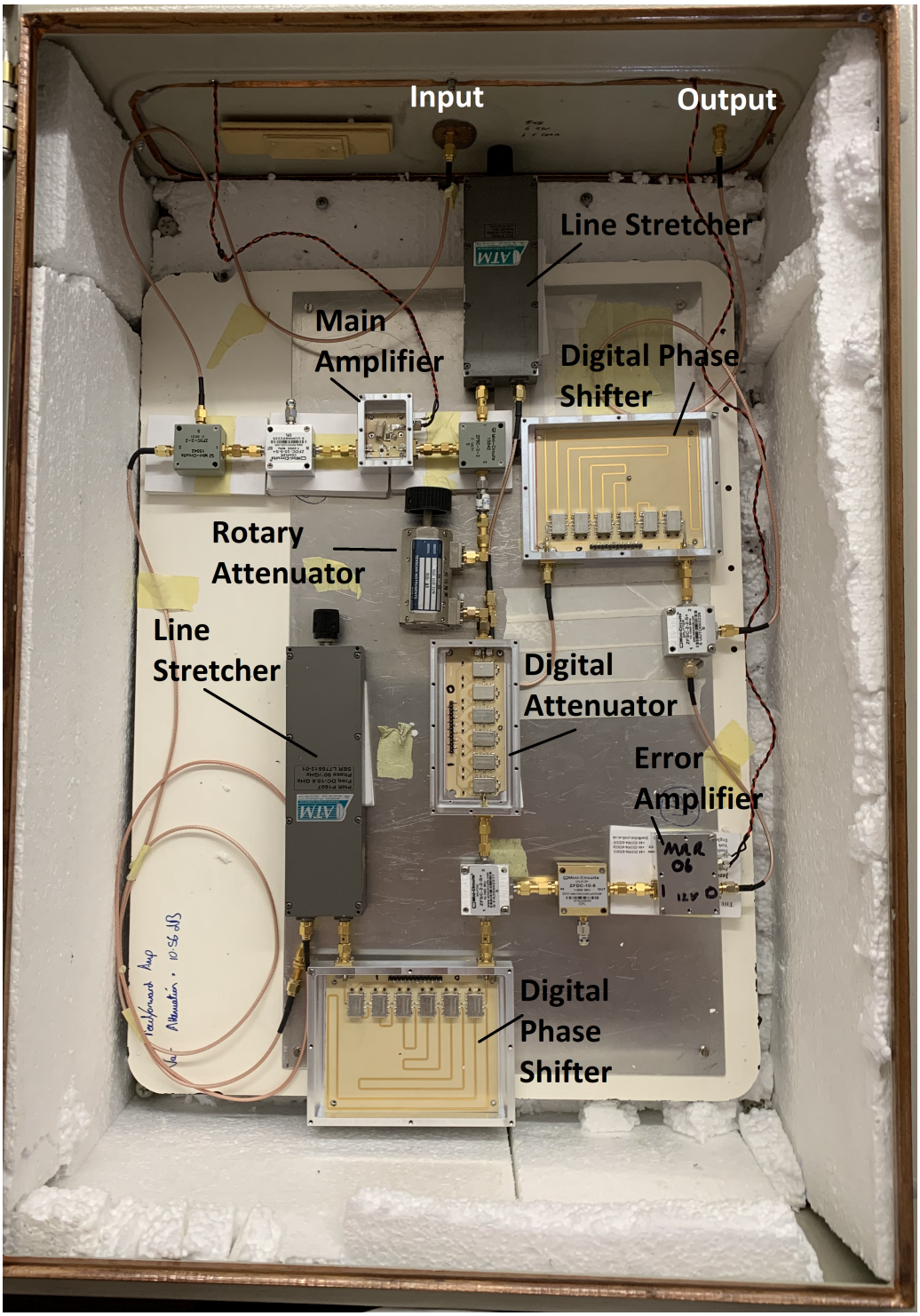


Figure 5.30: Assembled feedforward amplifier housed within a shielded enclosure. Each of the circuits is hosed in an aluminium enclosure, the lids are removed in this image to allow for tuning of the amplifier.

analyser output. Then the variable digital phase shifter was adjusted to further reduce the amplitude of the carrier signal. Finally, the line stretcher was adjusted to find the absolute minimum amplitude of the carrier signal. It was found that the digital phase shifter range was too small to minimise the carrier signal so a length of coaxial cable of approximately 180° was added in to provide a constant phase shift.

The measured carrier amplitude was -78.57dBm on the spectrum analyser output. The coupler introduced -10dB of loss to this signal so the actual carrier power at point (J) was -68.57dBm. The input power to the feedforward amplifier was -21.93dBm, so therefore the carrier suppression was calculated to be 46.64dB.

In order to calibrate the second loop, the R & S FSWP 50 residual phase noise measurement system was used to show how much a tone at offset of 294 Hz was suppressed. As before the tone was applied to the reverse coupled directional coupler at a frequency of 100MHz +294 Hz, with a power level of -40dBm. After the directional coupler the actual power level of the tone at the input of the amplifier was measured to be -50dBm. The phase noise spectrum of the feedforward amplifier was measured continuously from 100 Hz to 1 kHz offset so that the amplitude of the tone could was visible at the feedforward amplifier output.

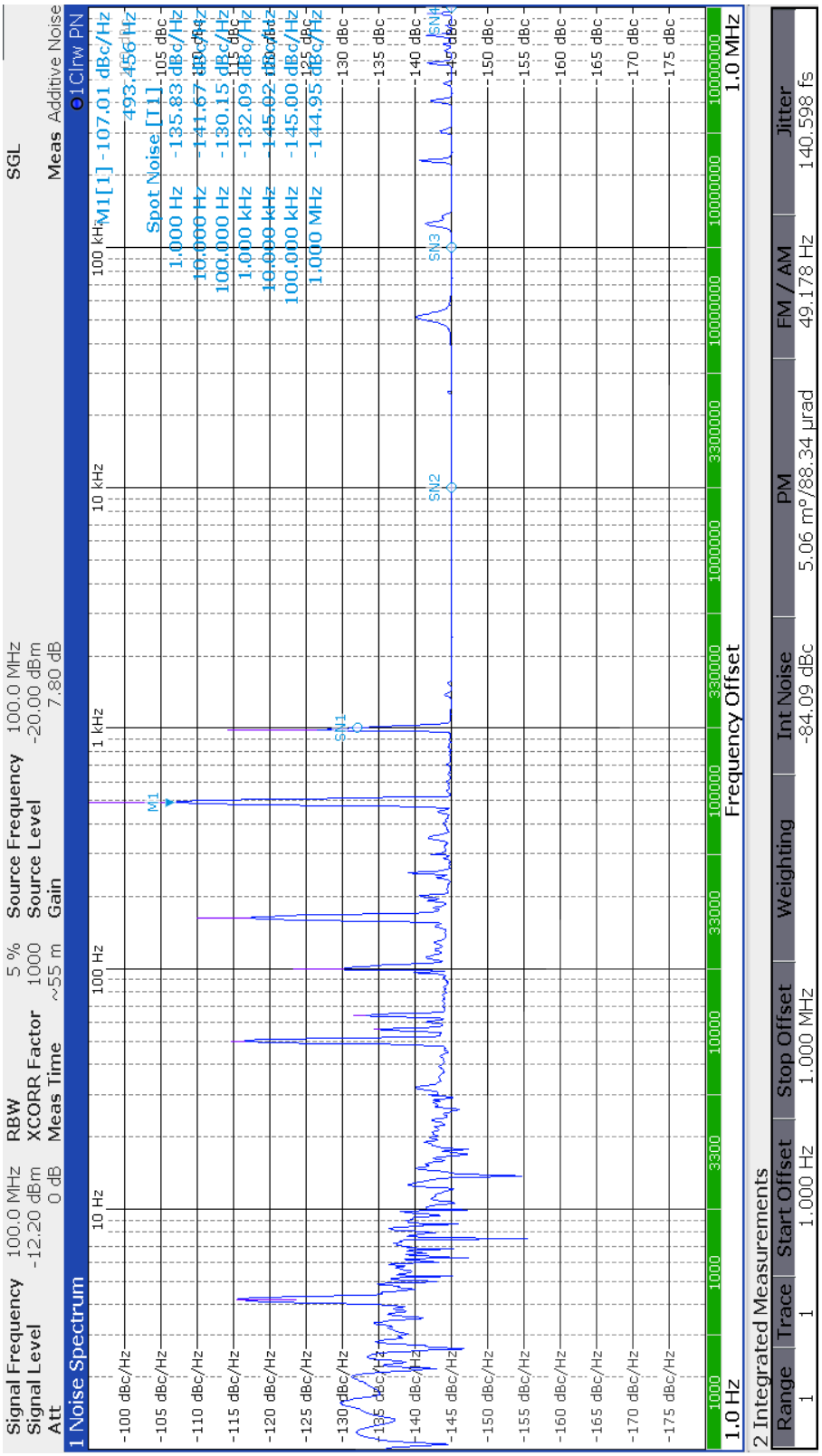


Figure 5.31: Screenshot of residual phase noise measurement with calibration tone applied to the system. The tone is at an offset frequency of 294 Hz from the carrier and the measured power at the output relative to the carrier is -107.01dBc/Hz, shown by marker M1.

The digital phase shifter was then set to apply a delay to the error path in order to minimise the amplitude of the tone. The amplitude of the tone was measured to be -107.01dBc/Hz at its lowest once the phase shifter had been adjusted and the bias voltage to the error amplifier varied as shown in Figure 5.31. As the main amplifier is operating in the linear regime, the error amplifier was expected to be biased with 12V to match the bias voltage of the main amplifier and therefore produce the same gain. It was found that a slight increase in the bias voltage to 12.2V for the error amplifier was required in order to match the main amplifier gain and ensure the tone suppression was at its maximum. This is because the error amplifier gain must be equal to the main amplifier gain plus the loss introduced by the 10dB directional coupler used to monitor the carrier suppression.

The output power from the feedforward amplifier was measured to be -12.20dBm, therefore the actual power of the calibration tone at the output of the FF amplifier is -119.21dBm. The power of the calibration tone at the input of the main amplifier was -50.55dBm, therefore the tone suppression is 68.66dB. Therefore it is expected that the flicker noise is suppressed by 68.66dB. Once calibrated the tone and monitor coax cables were removed and the two 10dB directional coupler ports were terminated with 50Ω loads. Now a residual phase noise measurement can be made of the feedforward amplifier operating in the linear regime. The feedforward amplifier residual phase noise was measured using the R & S FSWP 50 with the FF network enclosed within the shielded box. The gain of the feedforward amplifier was measured to be 8.8dB.

The noise figure is calculated from (5.26) using the measured noise figure of the MAR-06 of 2.07dB and the coupler ratios of couplers K_1 and K_3 of -3.2dB. It was assumed that losses in the error path were 0dB. The calculated noise figure of the feedforward amplifier is 8.47dB, using (2.62) to calculate the theoretical far from carrier phase noise of the feedforward amplifier, the calculated noise is -147.45dBc/Hz.

The calibration tone and sampled signal to the spectrum analyser were removed and these ports were terminated in 50Ω. The measured residual phase noise of the calibrated FF amplifier and the noise floor of the measurement system are plotted in Figure 5.32. The measured residual phase noise of the amplifier at frequency offsets smaller than 400 Hz are overlaid by the measured system noise floor which means that the feedforward amplifier residual phase noise is smaller than the phase noise introduced by the measurement system and is not possible to measure with the R & S FSWP 50.

The measurement of the far from carrier noise at frequencies greater than 1 kHz is in the range -145 to -145.37dBc/Hz, this suggests there are approximately 2.5dB of losses in the error loop that are contributing to a higher than predicted noise figure. This plot suggests that the flicker noise corner is less than 400 Hz and that the error correcting loop is causing the flicker noise introduced by the main amplifier to be suppressed.

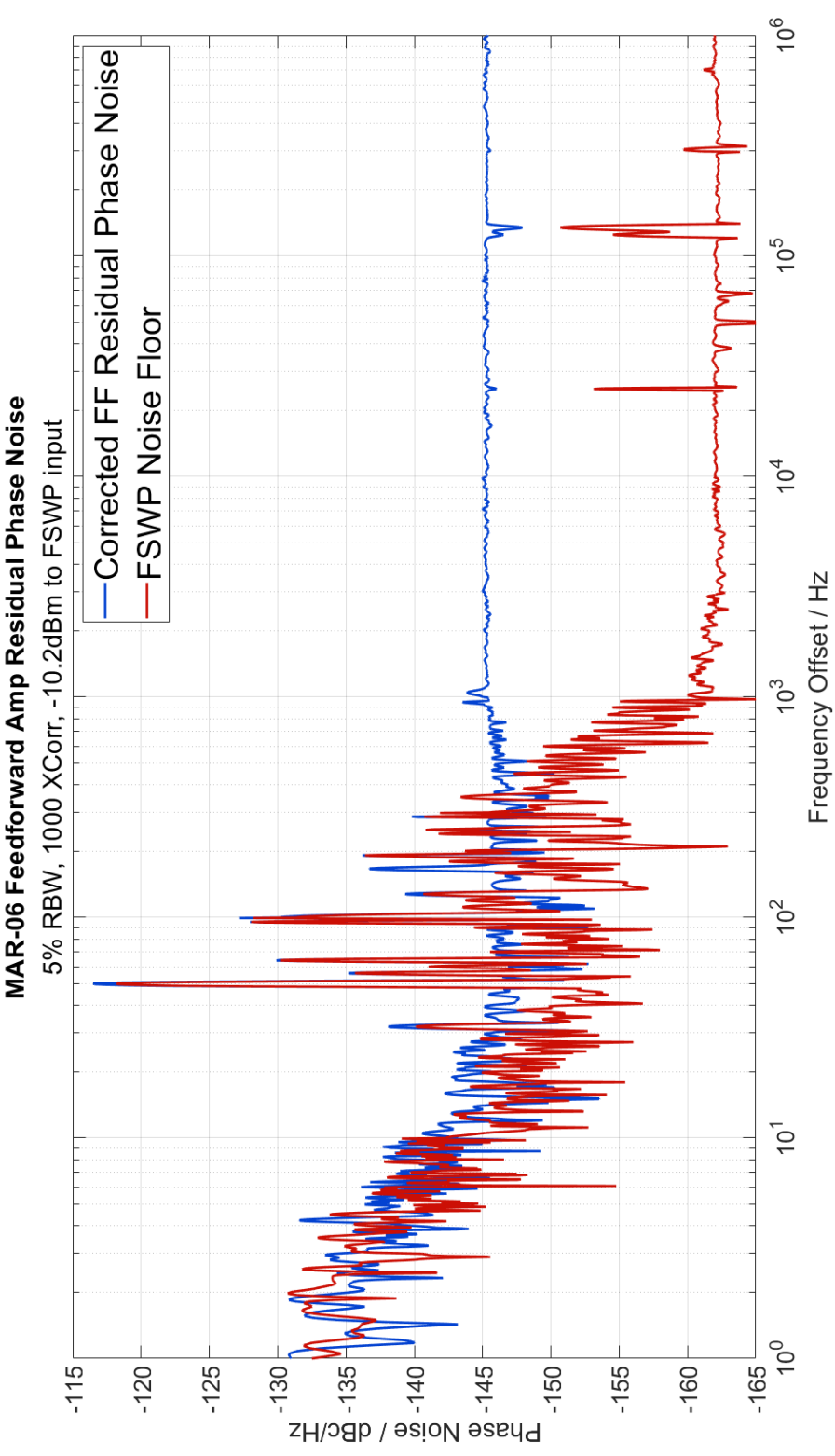


Figure 5.32: Residual phase noise measurement of the calibrated feedforward amplifier with input power -20dBm and the phase noise of the measurement system.

The input power to the FF amplifier can be increased to -5dBm so that the input power to the main amplifier is -8.6dBm which, according to Figure 5.22, would cause the main amplifier gain to drop to approximately 16dB ($\approx$ 4dB compression). As expected, the increase in input power increases the gain and phase imbalance within the feedforward amplifier and causes the flicker noise introduced by the main amplifier to increase, Figure 5.33 is a plot of the residual phase noise of the feedforward amplifier with increased input power as well as the system noise floor at the same input power.

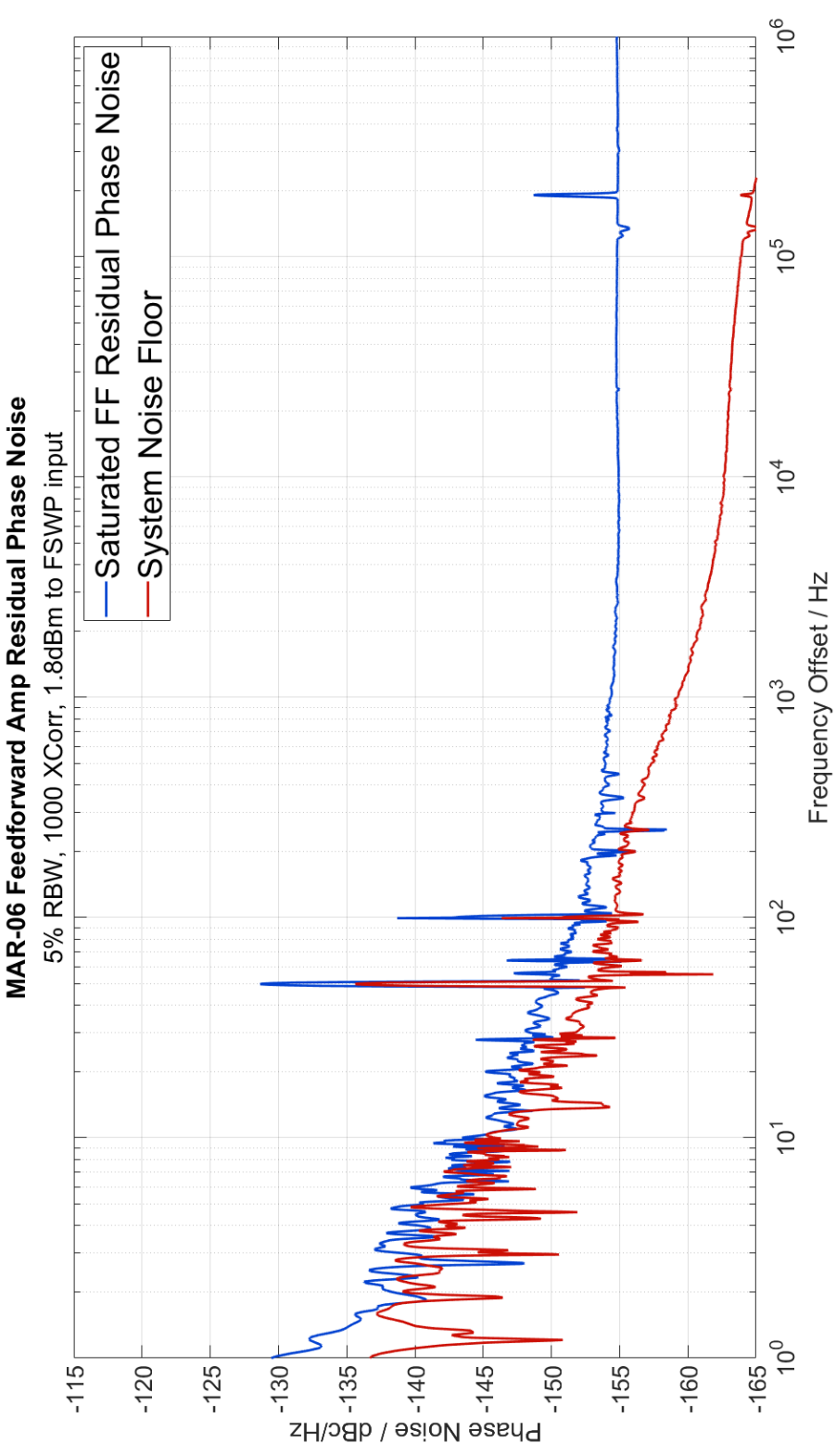


Figure 5.33: Residual phase noise measurement of the feedforward amplifier with input power -5dBm in order to saturate the main amplifier. The correcting loop is calibrated for -20dBm input power but the input power was increased to -5dBm in order to cause the main amp to enter saturation. The expected gain compression is 4.2dB.

The residual phase noise of the amplifier is measured to be above the system residual phase noise at all frequency offsets which allows the flicker noise corner to be estimated to be approximately 100 Hz. The far from carrier noise of the amplifier is approximately -155dBc/Hz, as the input power to the R & S FSWP 50 is 1.8dBm and the gain has reduced to 4.8dB, the noise figure has increased. Using (2.62), the noise figure can be calculated to be 15.187dB. This increase in noise figure is caused by the fact that there is amplitude error between the inputs to coupler K_4. The error correcting loop is no longer suppressing as much of the noise introduced by the main amplifier, including thermal noise, and the noise figure is no longer solely dependent on the error amplifier and couplers K_1&K_3.

Calibration of the feedforward amplifier in the saturation region

The feedforward amplifier was re-calibrated to suppress the flicker introduced by the saturating main amplifier using the same method as described in the previous section. Firstly the carrier suppression at point (I) was measured using the same spectrum analyser. The value of attenuation was varied until the 100 MHz carrier amplitude reached a minimum value. Then the phase shifter was adjusted to further reduce the signal amplitude before finally the attenuation was varied again to reach the absolute minimum amplitude of the carrier. The amplitude of the carrier tone was measured to be -68.91dBm. The input power to the feedforward amplifier was -5dBm and the output coupler at point (I) introduces 10dB attenuation, therefore the suppression of the carrier signal at point (I) is calculated to be -53.91dB.

The same calibration tone used in calibrating the amplifier in the linear regime was used, 294 Hz offset, -40dBm input to the reverse coupled directional coupler. The input power to the amplifier from the tone was therefore -50dBm. The same tone was used so that the error amplifier did not saturate and would cause errors in the flicker noise cancellation.

The R & S FSWP 50 residual phase noise measurement system was once again used to measure the power level in the tone relative to the carrier at the amplifier output and the bias voltage of the error amplifier was varied until the tone reached a minimum power level. Then the phase shifter was varied in order to add delay into the signal in the top path so that the noise power at points (L) and (K) were in antiphase. The final step was to finely adjust the error amplifier bias voltage to ensure the the gain balance between the main and error amplifier was at its lowest and the tone was

suppressed as much as possible. The phase noise spectrum at the output of the FF amplifier showed that the power level of the tone was -110.10dBc/Hz.

The carrier signal power was -1.96dBm, the power of the calibration tone is therefore -112.06dBm. As the amplitude of the tone at the input of the main amplifier was measured to be -50dBm, the suppression of the tone is therefore -62.06dB. The gain of the amplifier was measured to be 4.02dB. A second residual phase noise measurement was made with the error correcting amplifier removed from the circuit. To do this, the error amplifier was disconnected from the input of power combiner K_4 and terminated with a 50Ω load, the input to the power combiner was also terminated with a 50Ω load. A plot of the measured residual phase noise of the saturated amplifier with the error amplifier included and disconnected in shown in Figure 5.34.

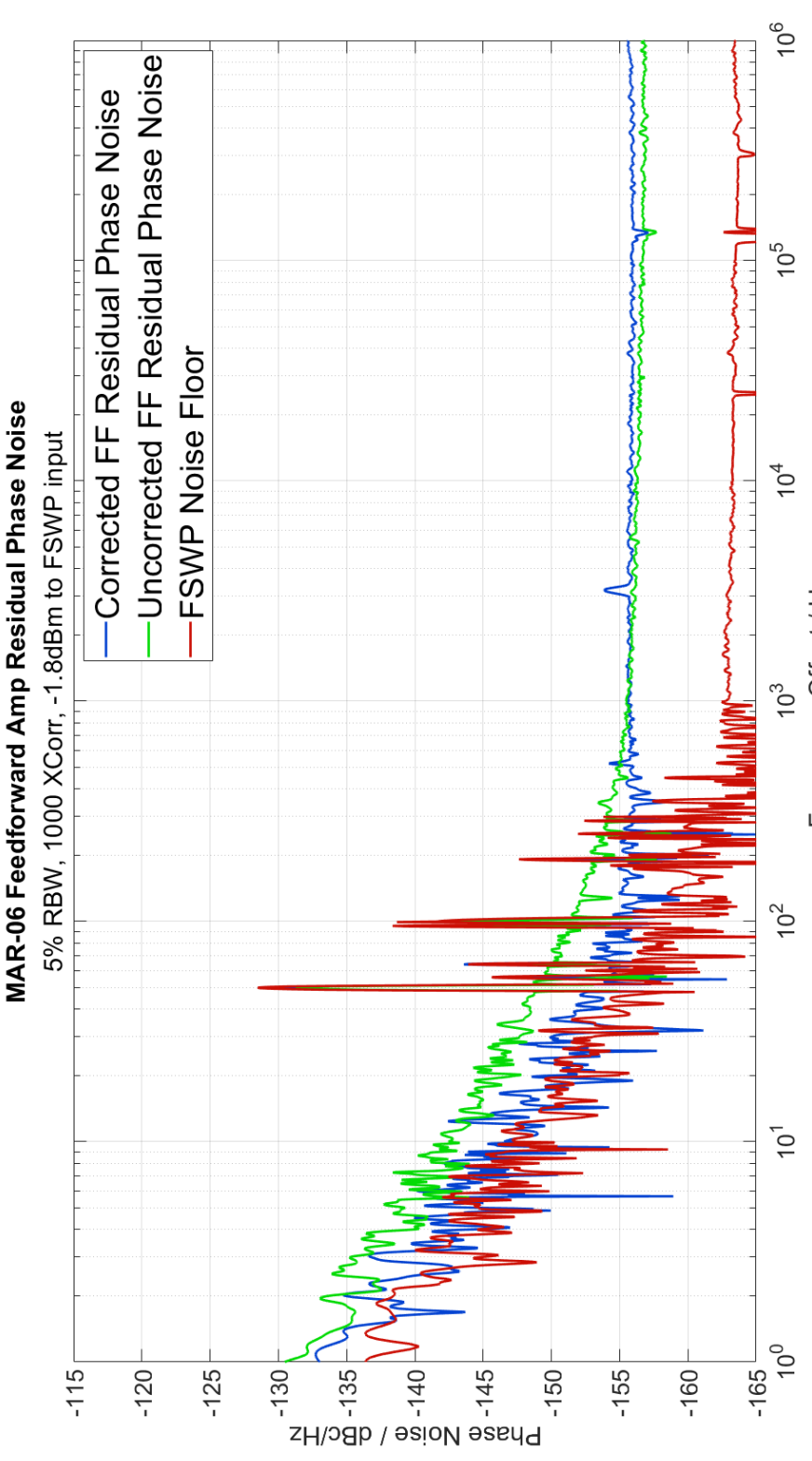


Figure 5.34: Residual phase noise measurement of the calibrated feedforward amplifier with input power -5dBm and a residual phase noise plot of the feedforward amplifier with the error amplifier removed. The plot also includes the measured residual phase noise of the R & S FSWP 50 measurement system.

With the error amplifier connected into the loop, the residual phase noise measurement of the feedforward amplifier is once again overlaid by the measured residual phase noise of the measurement system. It is therefore equal or less than the residual phase noise of the measurement system and cannot be measured using the R & S FSWP 50. This suggests that the error correction loop is suppressing the flicker noise as expected. With the error amplifier disconnected there is an increase in the flicker noise of the feedforward amplifier, the trace for this residual phase noise measurement is above the noise floor measurement with a flicker noise corner of approximately 250 Hz.

It is therefore possible to adjust the gain of the error amplifier, the attenuation between the loops and the delay in each loop accordingly to allow for flicker noise suppression when the main amplifier is saturating to achieve flicker noise suppression in the feedforward amplifier. At 10-100 Hz offsets the improvement in the residual phase noise measurement with the error loop connected is at least 5dB, though the measured residual phase noise of the corrected amplifier with the error loop connected is overlaid by the system noise floor. The actual flicker noise suppression is likely to be greater than this. The noise figure of the feedforward amplifier has increased to approximately 15dB, calculated by (2.62) using a measured far from carrier noise of -156dBc/Hz, gain of 4.02 and input power of -1.8dBm.

Despite the error correction loop suppression, the noise figure increase is caused by the increased noise figure of the saturating main amplifier.

5.6 100 MHz feedforward amplifier oscillator

5.6.1 LC Oscillator

Two 100 MHz oscillators have been assembled using the feedforward amplifier in the feedback loop. The components in the feedback loop are the same with the only difference being the type of resonator used. The first resonator that was used is an LC resonator with an insertion loss of -4.45dB at 100 MHz, Q_L of 48.51 and therefore a Q_0 of approximately 120. Figure 5.35 is the schematic of for the LC resonator used in the first oscillator. The second resonator is a crystal oscillator with a resonant frequency of 100 MHz, insertion loss of -5dB, Q_L of 50,000 and Q_0 of 120,000. The maximum input power to the crystal oscillator is 0dBm, the lumped LC resonator was used to build up the oscillator

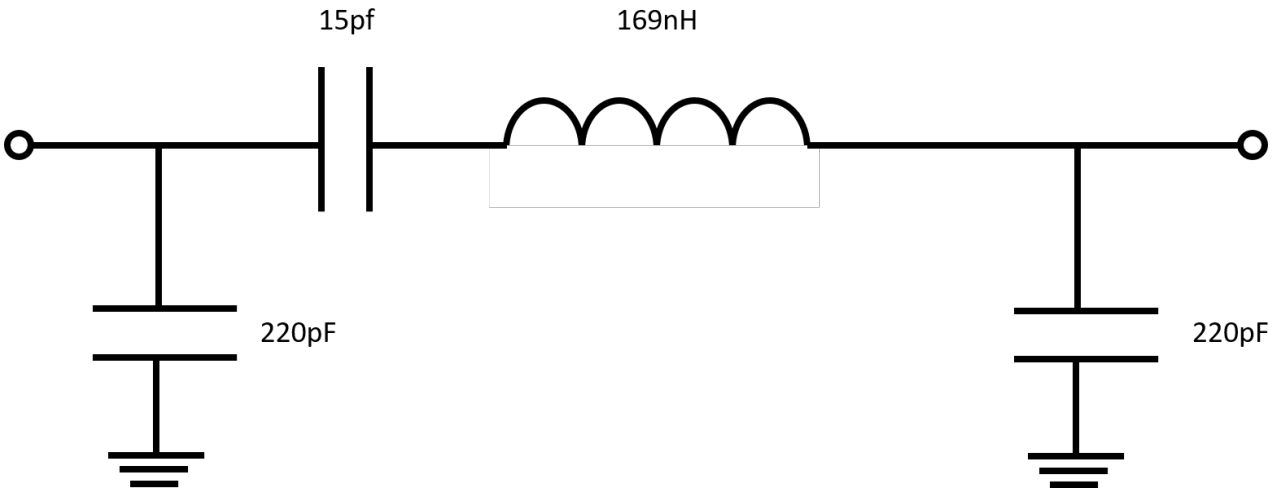


Figure 5.35: LC resonator schematic with $Q_L = 48.51$ and $S_{21} = -4.45$dB at 100 MHz.

first so that the loop power could be measured and therefore ensure the maximum input power to the crystal could not be exceeded.

The oscillation output is coupled from the loop via a ZFDC-10-5-S+ 10.8dB directional coupler from MiniCircuits [94]. The S-Parameters of directional coupler were measured using the Anritsu network analyser with a 50Ω load terminating the port that was not being measured. The coupled output was measured to be -10.714dB and the through loss from input to output port was measured to be -1.136dB.

A duplicate 100 MHz digital phase shifter designed by Luke Dummott was used in the feedback loop in series with a line stretcher to adjust the loop phase. The digital phase shifter can provide a minimum phase shift of 2.813° so the line stretcher was added in series to allow for precision tuning of the loop phase. The line stretcher provides 90°/GHz of phase shift so therefore at 100 MHz, the maximum variation in phase shift is 9°. The oscillator circuit is shown in Figure 5.36. Initially the error amplifier in the feedback loop was removed and all coupler ports that connect the main loop to the error correction loop were terminated with 50Ω loads.

The coupled output was connected to the spectrum analyser input of the R & S FSWP 50 and the digital phase shifter digital input was varied until the the oscillation peak was observed to have maximum power. The measured output power of the oscillator was -17.8dBm.

P_{AVO} was calculated from the measured output power plus the coupling ratio of the output coupler

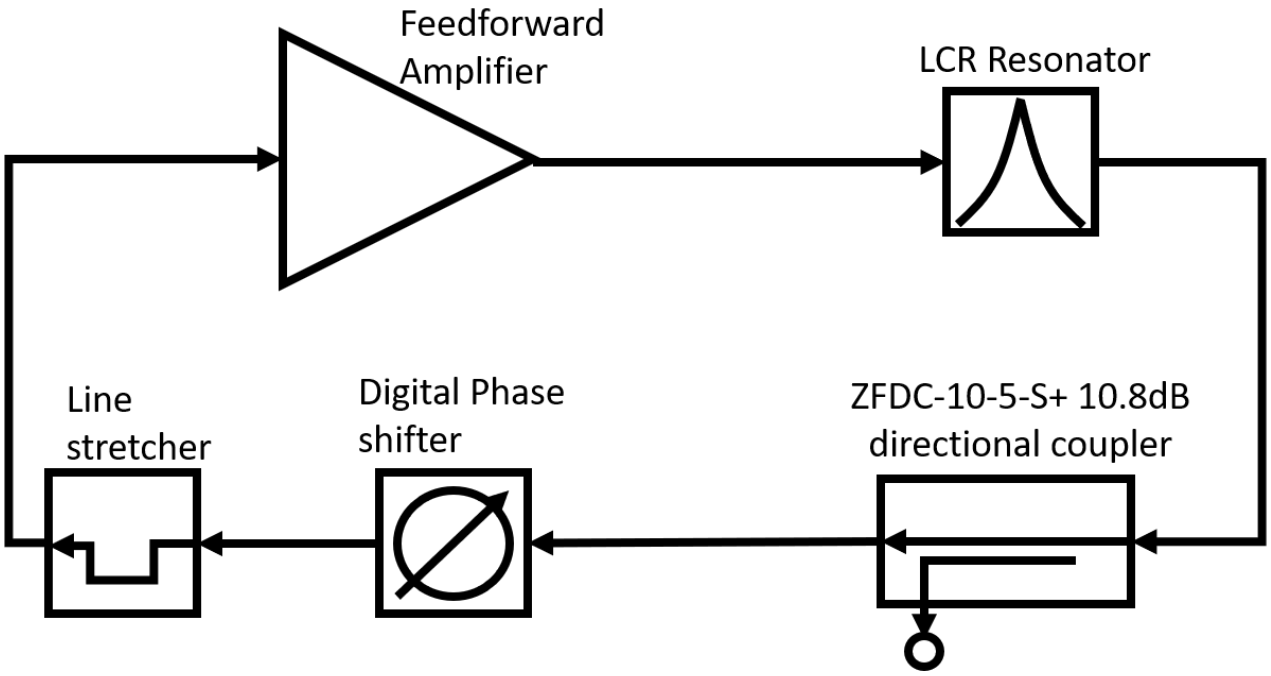


Figure 5.36: LC oscillator block diagram with the feedforward amplifier used in the feedback loop.

(10.714dB) plus the insertion loss of the LC resonator (-4.556dB) to be -2.636dBm. The oscillator phase noise was measured without the error correction loop connected and the main amplifier was allowed to enter saturation. This measurement is plotted in Figure 5.37.

The error correction loop was then reconnected in the feedforward amplifier and the attenuation between the main loop and error correction loop was increased until the power measured at point (J), on figure 5.2, via a ZFDC-10-5-S+ directional coupler, was minimum. Then the digital phase shifter control input was increased until the power at point (J) further reduced to a minimum before the line stretcher was used for fine adjustment of the phase. The 100 MHz carrier signal at point (J) was measured to be be approximately -65dBm, there was variation around this power level because the carrier signal power is so small and is therefore susceptible to small movements affecting the measurement.

A tone was injected to the input of the main amplifier at a frequency offset of 300 Hz from the carrier and the oscillator phase noise was measured from 100 Hz to 1 kHz. The power of this tone was set at -40dBm. The measurement time was less than 0.2 seconds so the gain of the error correction

amplifier and the phase shifter in the main loop can be varied and the tone suppression can be observed in real time.

The gain of the error amplifier was varied by decreasing the power supply voltage until the tone observed in the phase noise spectrum reached a minimum. This occurred when the voltage was dropped from 12V to 9.6V. Then the digital phase shifter control signal was varied until the offset tone power reached a minimum. The tone suppression was measured to be approximately -102dBc/Hz. At the input to the main amplifier the tone power was measured to be -50dBm. The input power to the R & S FSWP was -17.4dBm and the power of the suppressed tone is -119.4dBm. therefore the tone suppression is calculated to be -69.4dBm. P_{AVO} was calculated to be -1.963dBm.

The oscillator phase noise with the error correction amplifier was then measured and the result from this measurement is plotted in Figure 5.37. The theoretical noise is calculated using (3.28) using the parameters in table 5.2. The noise figure is calculated using the Friis equation, (3.16), for a series combination of components. The parameters used to calculate the respective noise figures for the oscillator feedback loops for both oscillator configurations (with and without the error correction amplifier connected) are shown in tables 5.3 and 5.4. Its important to calculate the noise figure with the correct ordering of the feedback components as the calculated noise figure will differ from the actual noise figure contributing to the oscillator phase noise calculation, therefore the order in which the components are listed is the order in which they are placed in the feedback loop.

The calculated noise figure for the series feedback components in the LC oscillator, with no error correcting path in the feedforward amplifier, is 7.92dB. The noise figure calculated for the feedback loop components with the feedforward amplifier including the error correction loop is 10.45dB. In both configurations the measured oscillator phase noise is less than the theoretical phase noise at frequency offsets less than 1 MHz. The lower calculated loop noise figure for the oscillator without the error correction amplifier results in a lower oscillator phase noise in both theory and in measurement, despite the larger flicker noise corner used in the calculation because resonator 3dB bandwidth is approximately 1 MHz, which is greater than the flicker noise corners used in the theoretical calculation of the oscillator phase noise. Furthermore, this is why the measured phase noise at offset frequencies higher than 1 MHz are close to the calculated values.

Osc Config	Q_L	Resonator S_{21} /dB	Q_0	F_1	P_{AVO}	F_C /Hz
Main amp only	46	-4.556	106.9	7.92	-2.363	1000
With error correction	46	-4.556	106.9	10.45	-1.963	100

Table 5.2: Parameters used for the theoretical oscillator phase noise calculation. The noise figure for the loop components is different but all other parameters are the same.

Osc Component	NF/dB	Gain /dB
10dB Coupler	1	-1
Digital Phase Shifter	0.45	-0.45
Line Stretcher	1	-1
3dB Splitter	3.2	-3.2
Main Amplifier	2.06	18
3dB Splitter	3.2	-3.2
Digital Phase Shifter	0.45	-0.45
3dB Splitter	3.2	-3.2

Table 5.3: LC oscillator components in order from resonator output to resonator input, the error correction loop is omitted from the amplifier so the main amplifier is in series with the splitters and phase shifter.

Osc Component	NF /dB	Gain /dB
10dB Coupler	1	-1
Line Stretcher	1	-1
Feedforward Amplifier	8.47	8

Table 5.4: LC oscillator components in order from resonator output to resonator input, the error correction loop is included and amplifier is treated as one component with a noise figure calculated using (5.26).

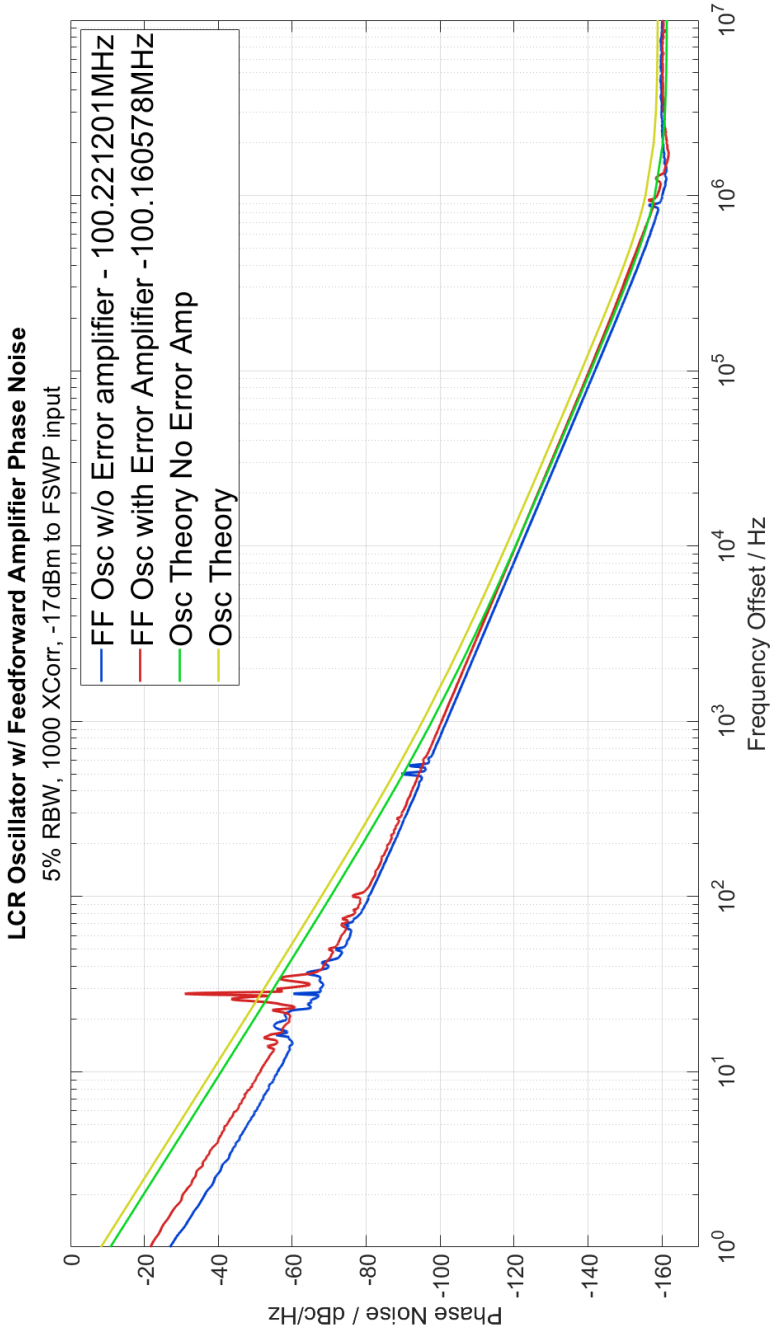


Figure 5.37: Measured LC oscillator phase noise with the feedforward amplifier used in the feedback loop. Two measurements were made, with and without the error correction loop connected. The theoretical oscillator phase noise is calculated based on the measured parameters for both oscillator configurations.

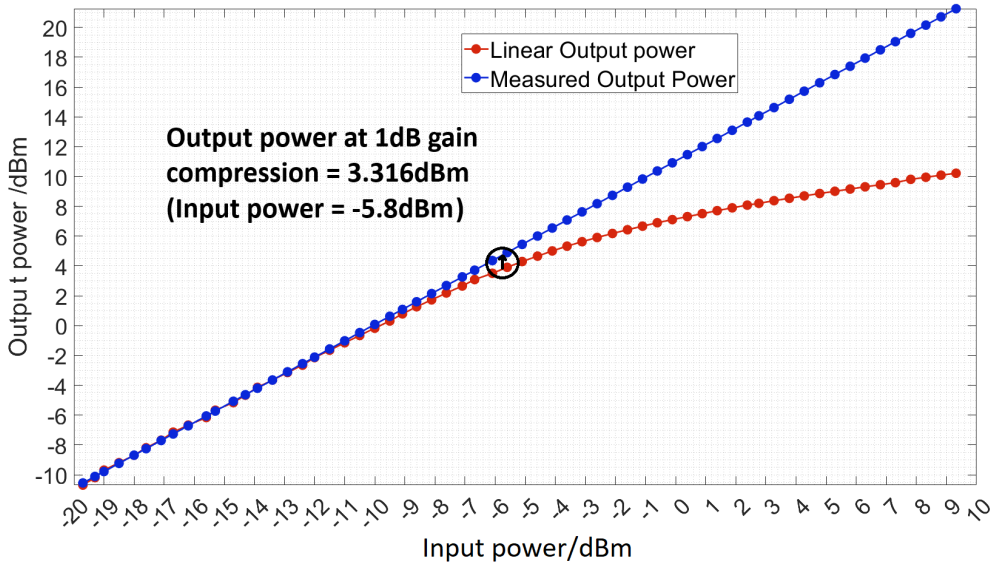


Figure 5.38: The feedforward amplifier with the error correction loop removed output power measured with increasing input power. The output power in 1dB compression is 5.5dBm, for the output power to be -2.363dBm the input power must be approximately -12.2dBm.

The flicker noise corner falling within the resonator 3dB bandwidth does not account for the discrepancies between the measured and theoretical phase noise at frequency offsets less than 1 MHz. At less than 1 kHz offsets the measured phase noise is between 10 and 20dB lower than the calculated value. It is thought that this is caused because the wrong flicker noise corner was used in the calculation, the flicker noise corners used were calculated from the residual phase noise measurements made of the feedforward amplifier with an input power of -5dBm. Firstly considering the oscillator without the error correction loop applied to the amplifier. As the feedforward amplifier output is connected to the input of the resonator, the estimated output power of the oscillator is -2.363dBm, the output of the main amplifier is connected to a 3dB splitter, a digital phase shifter, a line stretcher and then another 3dB splitter before the output is measured. The actual estimated output power of the main amplifier is therefore $-2.363\text{dBm} + 3.2\text{dB} + 1.45\text{dB} + 3.2\text{dB} = 5.214\text{dBm}$. From the P1dB measurement, Figure 5.22, made for the MAR-06 amplifier, the input power to the main amplifier must be approximately -14.2dBm. Therefore the input power in the oscillator loop is the estimated amplifier input, plus the through loss of the 10dB coupler used to apply the calibration tone plus 3dB splitter loss. This is calculated to be $-14.2\text{dBm} + 1\text{dB} + 3.2\text{dB} = 10\text{dBm}$, therefore the amplifier is not being driven as far

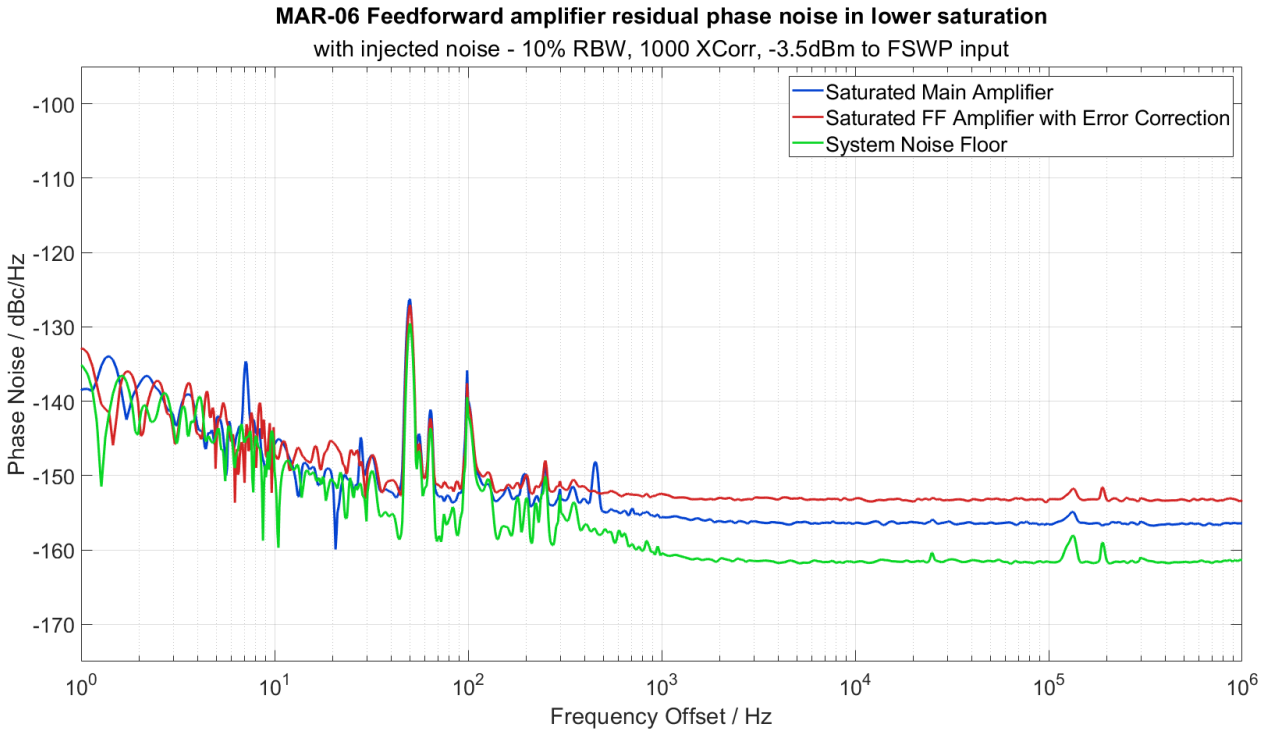


Figure 5.39: The residual phase noise measurements of the feedforward amplifier with and without the error correction loop connected. The main amplifier saturation was reduced to approximately 0.1dB and the output power of the amplifiers was approximately -2.636dBm.

into saturation as anticipated and the flicker noise corner for the saturating amplifier are not accurate for these measurements.

A further P1dB compression measurement was made, this time the feedforward amplifier without the error correcting loop was measured, not just the MAR-06 on its own. A graph of output power plotted against increasing input power is plotted in Figure 5.38. The output power in 1dB compression is 5.5dBm and the input power is estimated from the graph to be approximately -5.8dBm. To achieve the output power of the amplifier in the oscillator loop, the input power must therefore be -12.2dBm. From the plot the gain of the feedforward amplifier would be 9.75dB, 0.11dB less than the maximum value. The level of gain saturation is therefore much lower than expected. The residual phase noise of the feedforward amplifier with and without the error correction loop was remeasured using a lower input power. The input power was varied until the output power of the feedforward amplifier reached as close to -2.363dBm as possible, once that residual phase noise measurement had been made, the

error loop was connected and the same calibration process as before was followed. The residual phase noise measured is plotted in Figure 5.39, the cables connected from the output to the input introduce a loss of approximately 0.9dB, hence the input power to the R & S FSWP is 0.9dB higher than the actual output power of the amplifier. The system noise floor with the same input power to its input is also plotted. It can be seen that the two residual phase noise measurements are limited by the system noise floor before the flicker noise corner of both amplifier configurations can be observed and it is therefore impossible to calculate an accurate flicker noise corner to be used in the oscillator phase noise calculation.

5.6.2 Noise Injection

The lower flicker noise corner produced by the amplifier whilst its in the oscillator loop means that any flicker noise suppression achieved by the feedforward amplifier is not observed in the oscillator phase noise measurement because the amount of flicker noise power that can be suppressed is low. The lower noise figure of the feedforward amplifier without the error correction loop causes the oscillator phase noise to be lower than if the error correction loop was connected. To confirm the feedforward amplifier with the error correction loop connected is operating correctly a white noise source was applied to the coupler used to apply a calibration tone to the amplifier via a series of attenuators that provide 40dB attenuation. The residual phase noise of the feedforward was remeasured with the external noise applied.

Firstly, the error loop was removed from the feedforward amplifier and the residual phase noise was measured. The input power to the amplifier was varied such that the output power was measured to be -3.5dBm as observed previously. Once this measurement was complete, the error correction loop was reconnected and the feedforward amplifier was calibrated using the same calibration process described previously except that a tone was not injected so that it could be measured in the output phase noise spectrum. Instead, the noise source was used to measure the suppression in the output spectrum. The results of the residual phase noise measurements are plotted in Figure 5.40 where is can be observed that the injected noise is suppressed by 27dB. This measurement confirms that the feedforward amplifier can suppress the noise generated by the main amplifier when it is driven into saturation by varying the gain of the error amplifier, the attenuation between the two paths and the

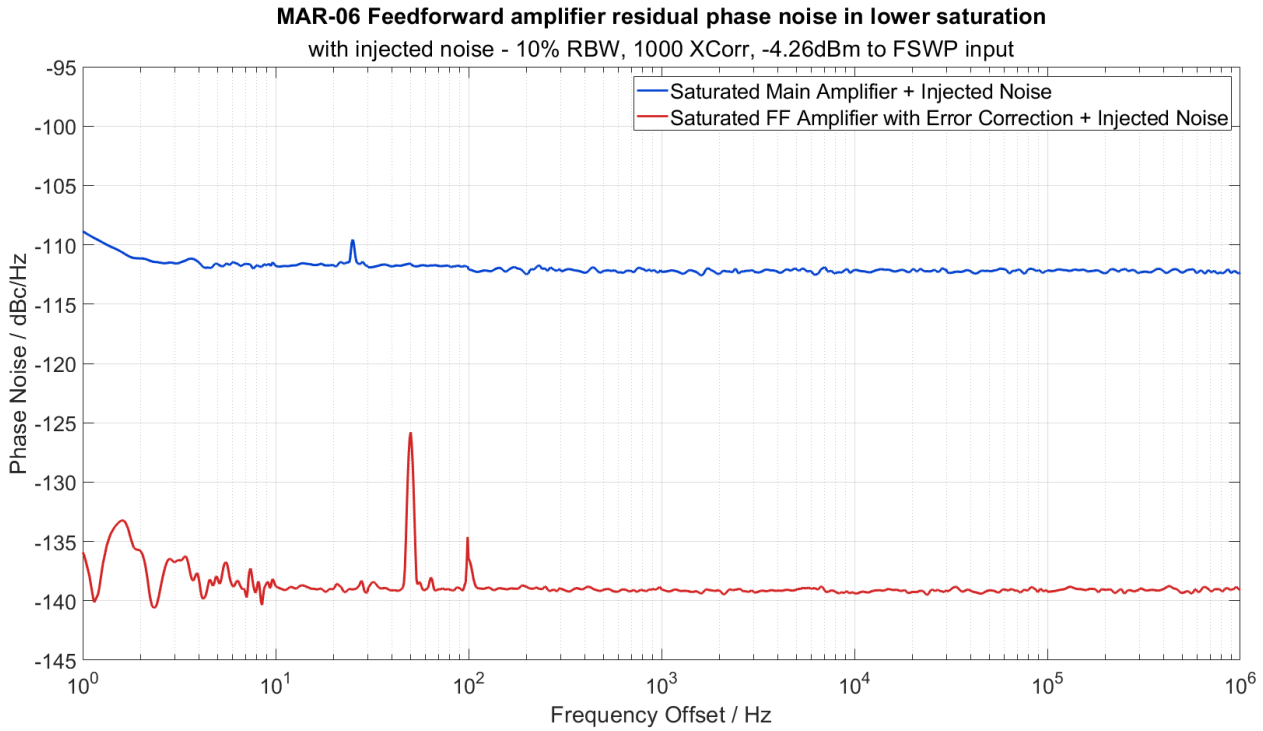


Figure 5.40: The residual phase noise measurements of the feedforward amplifier with and without the error correction loop connected with the white noise source injecting noise into the system. The noise introduced into the system is shown to be suppressed by 27dB.

phase shift between them so that the signals entering the power combiners are in antiphase.

The amplifier was once again connected back into the oscillator loop and the oscillator phase noise was measured with white noise injected and the error loop disconnected and then reconnected. Once again the same calibration process for maximising the noise suppression was used as before except the noise injected to the input of the main amplifier was used in place of a tone at an offset frequency. The oscillator has up converted the thermal noise that is causing the $\frac{1}{f^2}$ decrease in phase noise with frequency. It is observed that there is a 20dB reduction in the $\frac{1}{f^2}$ noise suggesting that all noise introduced by the main amplifier would be suppressed by 20dB. This confirms that the feedforward amplifier can be used in an oscillator where the main amplifier is allowed to saturate. The gain of the error amplifier, the attenuation between the loops and the phase shift of the signals at the inputs of the power combiners can be controlled to linearise the feedforward system. ultimately, this removes the need for PIN diode limiters that have previously been used to reduce the power in the oscillator

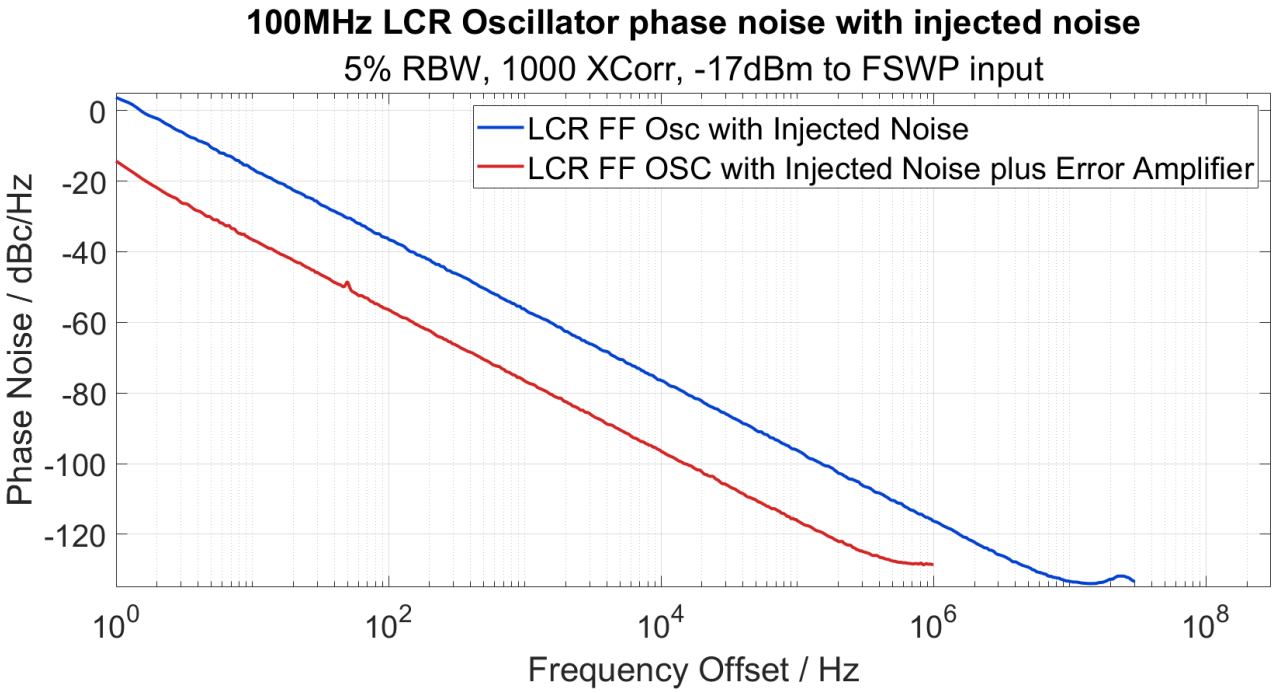


Figure 5.41: Oscillator phase noise measurement with noise injected. The phase noise plot is up converted thermal noise that decreases at a rate equal to $\frac{1}{f^2}$. There is 20dB suppression of noise between the two oscillation configurations.

loop and stops the main amplifier from saturating.

It is important to note that the far from carrier noise has increased and that is because the introduction of the error correction loop increases the noise figure of the feedforward amplifier. This is because the main amplifier noise figure has not increased enough to increase the noise figure of the feedforward amplifier without the error correction loop to be greater than the noise figure of the feedforward amplifier with the error correction loop connected. If it were the case that the main amplifier could enter greater gain compression then the noise figure would likely increase and the far from carrier noise of the feedforward amplifier without error correction would increase to level greater than that currently observed in the feedforward amplifier with the error correction loop. If that were the case, the far from carrier noise of the main amplifier would also be suppressed.

The same measurement was attempted using the crystal resonator instead of the LC resonator in the oscillator. It was found that varying the phase shifters in the feedforward amplifier caused the phase shift of the whole oscillator loop to vary enough to stop the oscillation. It was therefore not

possible to apply the feedforward technique to the crystal oscillator but this research has demonstrated the possibilities of using a variable gain feedforward amplifier in an ultra low phase noise oscillator.

5.7 Conclusions and further work

The increase in flicker noise corner with the error amplifier disconnected shows how the flicker noise of an amplifier used in the saturation regime can be reduced, this means therefore, that an amplifier used in the feedback path of an oscillator can make use of the feedforward error correction technique to reduce the flicker noise it introduces to the oscillator phase noise measurement. The device used here, the MAR-06, is a low noise BJT based device so the flicker noise corner is expected to be low, however the findings from these measurements suggest this technique can be applied to high power GaAs FETs used in higher power oscillators. As this amplifier was designed to be used in a crystal oscillator, a high power GaAs FET is not suitable as the crystal can be easily damaged but in other low noise oscillators such as DROs or cavity resonator oscillators, this technique could be applied.

This amplifier can be calibrated for maximum suppression regardless of the input power to it and can therefore be controlled automatically. The two points of reference, point (I) and point (M) can be sampled and fed into a control system that firstly aims to reduce the amplitude of the carrier signal at point (M). This could be achieved by using a microcontroller to switch the digital attenuator and phase shifter until a minimum value is reached. Secondly, a tone of known frequency offset and amplitude should be applied as before and the output phase noise spectrum measured at a narrow range of frequency offsets. The amplitude and the frequency of the tone offset can be measured and processed by a microcontroller to change the bias voltage and phase shifter, to reduce the power level of the tone to a minimum. This process can be carried out continuously or at regular intervals depending on the application of the oscillator.

The technique is applied to an LC oscillator successfully though the level of saturation observed in the main amplifier is low and therefore a significant increase in flicker noise is not observed and cannot be suppressed. To demonstrate the noise suppression in an oscillator, noise was injected via a noise source and a suppression of 20dB in the oscillator is achieved marking a 6dB improved on the noise suppression achieved by the PIN diode limited oscillator presented in [2]. Measurements were

attempted using a 100 MHz crystal resonator in place of the LC resonator in the oscillator however an additional loss of approximately 0.5dB was introduced. Whilst oscillation could be sustained initially, the level of saturation of the main amplifier was even smaller and adjusting the phase shifters in the feedforward amplifier resulted in the oscillation stopping. A higher gain main amplifier or changes to the coupling ratios $K_{1,2\&4}$ are therefore necessary

It is suggested that further work of this topic should start with changing the amplifier used in the main amplifier to be GaAs as this will typically introduce more flicker noise than a BJT. These devices also operate at higher gain and greater levels of saturation can be achieved in an oscillator loop making the oscillation more stable. These devices operate at higher powers and frequencies and are therefore unlikely to be applicable to a crystal oscillator. An alternative resonator such as a DRO is a more suitable candidate. The calculations derived here and the techniques used in varying the gain and phase accordingly can be transferred to a different oscillator design, providing the couplers used are suitable for use at higher power and frequencies.

Adaptive feedforward control should be implemented to the system to monitor feedforward amplifier's residual phase noise output and adjust the attenuator, error amplifier gain and phase shifters accordingly. These components can all be digitally controlled so the next step would be to sample the power at point (J) to monitor the carrier cancellation and at point (M) to monitor noise suppression. A tone could periodically be injected and removed to minimise its contribution to the phase noise with the adaptive feedforward control carrying out the calibration steps to optimise the phase noise performance.

Chapter 6

5 MHz crystal oscillator

6.1 Introduction

The work presented in this chapter builds on the work presented by Timothy Nankervis for his BEng project [4]. In that work the oscillator was built up using separate modules connected via coaxial cables. A length of coaxial cable was used to adjust the oscillator loop phase and preliminary phase noise measurements were made achieving -118dBc/Hz at 1 Hz offset, -147dBc/Hz at 10 Hz offset and far from carrier noise of -162dBc/Hz.

In this work a tunable phase shifter is designed to replace the length of coaxial cable used to adjust the loop phase shift and contain all components within an aluminium box. It is hoped that the tunable phase shift can adjust the loop phase more precisely and improve on the oscillator phase noise performance. By mounting all PCBs in a metal enclosure it removes the need for SMA connectors and coaxial cables to connect the circuits together. Oscillator phase noise of -132dBc/Hz at 1 Hz offset and -160dBc/Hz at frequency offsets greater than 1 k Hz is measured.

This research group has previously presented the in depth design and ultra low phase noise measurements of an SC Cut 10 MHz crystal oscillator using a double oven to temperature stabilise the resonator [3]. At 1 Hz offset, the phase noise of two oscillators measured against each other was -118.9dBc/Hz. Therefore the estimated phase noise for a signal oscillator is -121.9dBc/Hz. Without the double oven configuration, one of the 10 MHz oscillators demonstrated phase noise of -122.4dBc/Hz at 1 Hz offset.

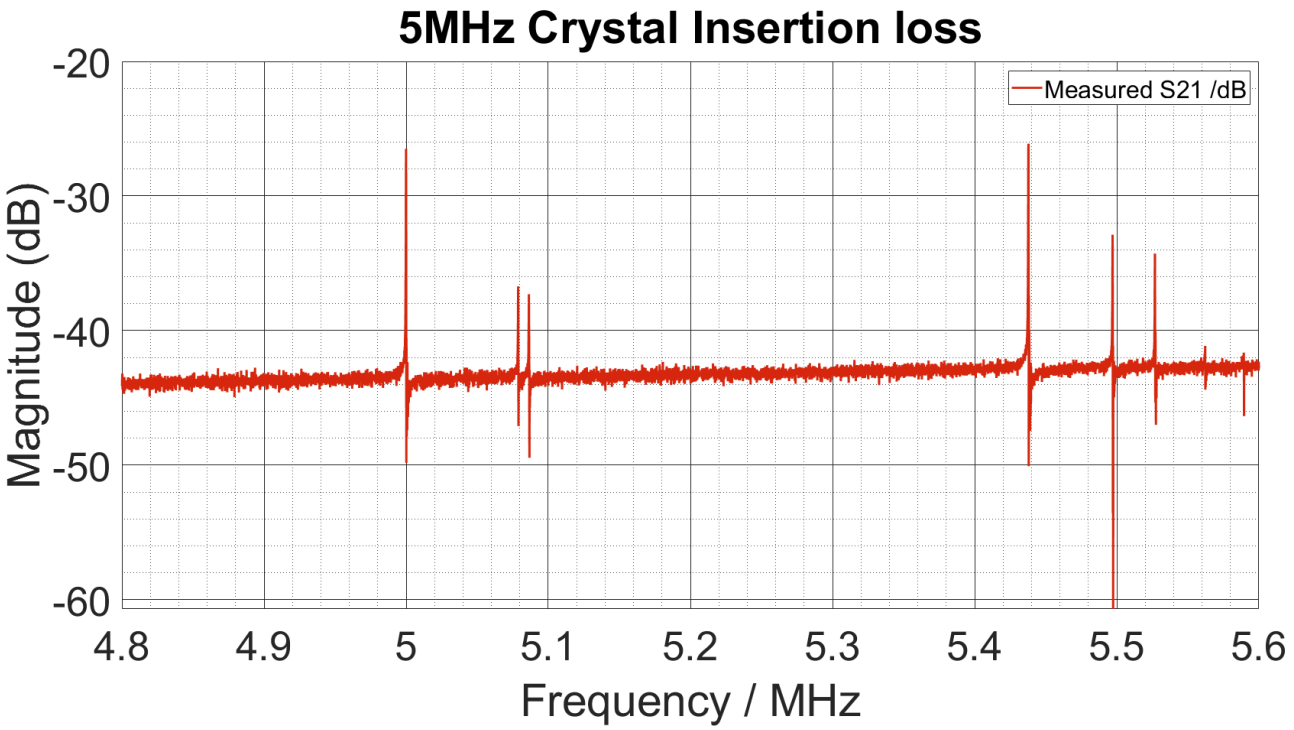


Figure 6.1: Broadband sweep S_{21} using USB DG8SAQ vector network analyser [103]. The resonance at 4.999818MHz is the required peak to use in the oscillator, the resonance at 5.44 MHz is the unwanted.

At 1 Hz offset from a 5 MHz carrier, the minimum oscillator phase noise measured using a bond via array manufactured, BVA, resonator was -136dBc/Hz in [100], however there was 13dB of variation in phase noise measured at 1 Hz offset across the range of four resonators used in these measurements. In [101], the predicted phase noise at 1 Hz offset from a 3.9 MHz carrier of a silicon micro-electromechanical systems, MEMS, oscillator is approximately -130dBc/Hz however this has not yet been shown in measurement. A quartz crystal oscillator presented in [102] demonstrates phase noise of -97dBc/Hz at 1 Hz offset from a 20 MHz carrier, though a detailed oscillator circuit is not presented. By scaling to 5 MHz, the phase noise is estimated to decrease by 12dB to -109dBc/Hz at 1 Hz offset.

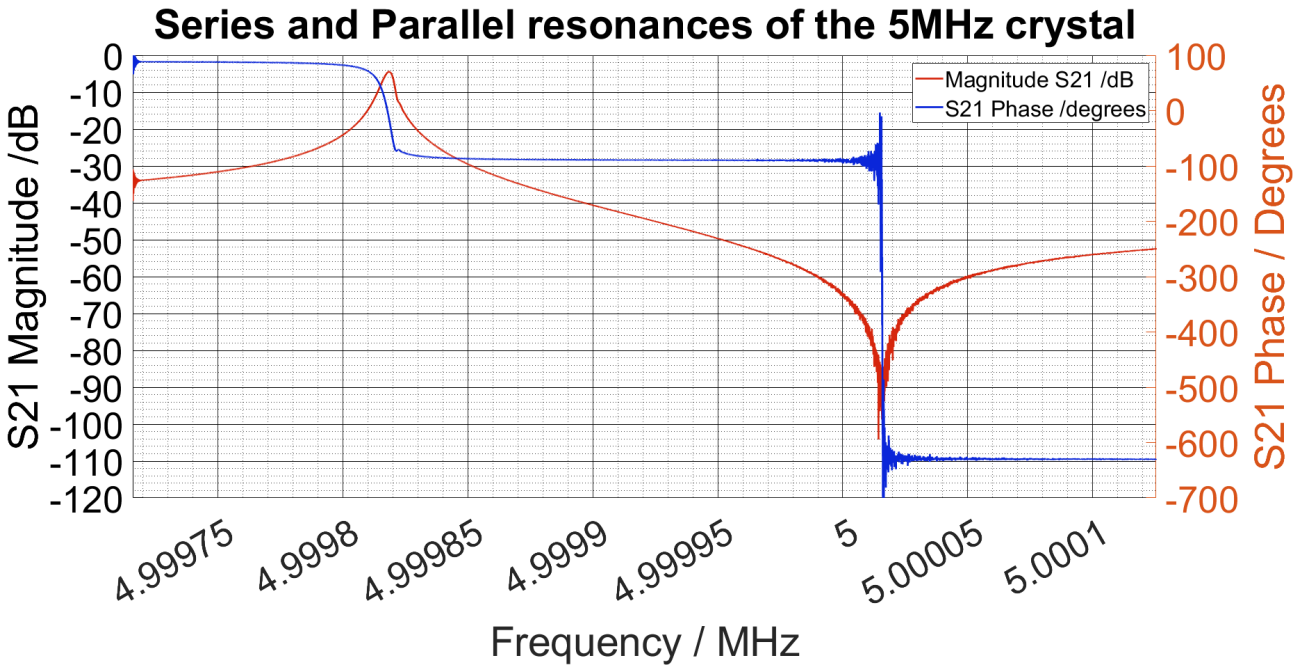


Figure 6.2: S-Parameter sweep of the series resonant peak at 4.999 MHz. The insertion loss at resonance is -4.14dB and the Q_l measurement of 950,541. Q_0 is then calculated to be 2,506,315.

6.2 5 MHz crystal

6.2.1 5MHz crystal measurements

The crystal that was used in this project was manufactured by Nofech Electronics Ltd and is a 5.0 MHz SC-cut crystal. The datasheet for the crystal states that the resonant frequency is 4,999,989 Hz, the series capacitance is stated to be 0.211fF and the series resistance is 61.4Ω. The turn over temperature is 87.6°. The crystal was connected to 50Ω transmission line within an aluminium enclosure and an S-Parameter measurement from 4.8 to 5.6 MHz was made using the SDR-Kits DG8SAQ 3E [103] USB vector network analyser. The S_{21} magnitude is plotted in Figure 6.1 showing resonant peaks at 5 MHz and 5.44 MHz.

To measure the insertion loss of the resonant peak at 5 MHz a narrow band sweep is required to increase the number of data points around the resonant frequency. This is because the Q_0 of the resonator is very high. The broad band sweep serves only to see other resonant frequencies the crystal produces. A narrow band measurement was made from 4.99981 MHz to 4.99988 MHz to accurately

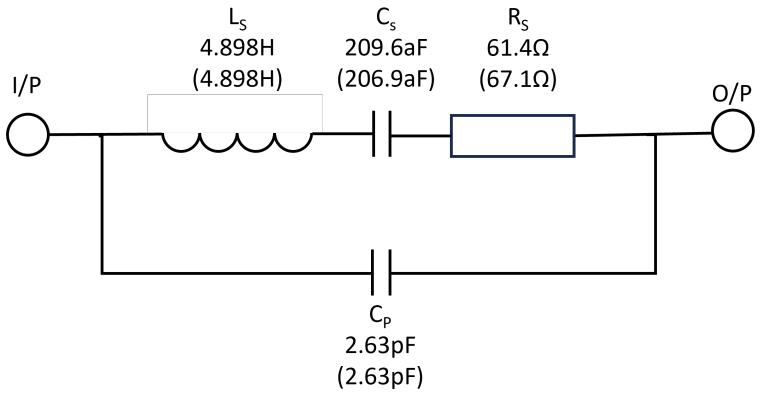


Figure 6.3: Quartz crystal LCR model including calculated components and tuned component values.

measure the resonant frequency, insertion loss and Q_l of the resonator. The insertion loss was measured to be -4.14dB at the resonant frequency of 4,999,818 Hz. The 3dB bandwidth of the resonator was measured to be 5.26 Hz giving a Q_l of 950,541. Using (4.16) the Q_0 can be calculated to be 2,506,315. An LCR model of the crystal resonator can now be calculated, the model for a quartz crystal is shown in Figure 6.3.(6.1) describes the relationship between the Q_0, the resonant frequency, series inductance and series resistance, $61,4\Omega$, which can be rearranged for L_S.

$$Q_0 = \frac{\omega_S L_S}{R_S} \rightarrow L_S = \frac{Q_0 R_S}{\omega_S} = \frac{2.506 \times 10^6 \times 61.4\Omega}{2\pi \times 4.999818 \times 10^6} = 4.898\text{H} \tag{6.1}$$

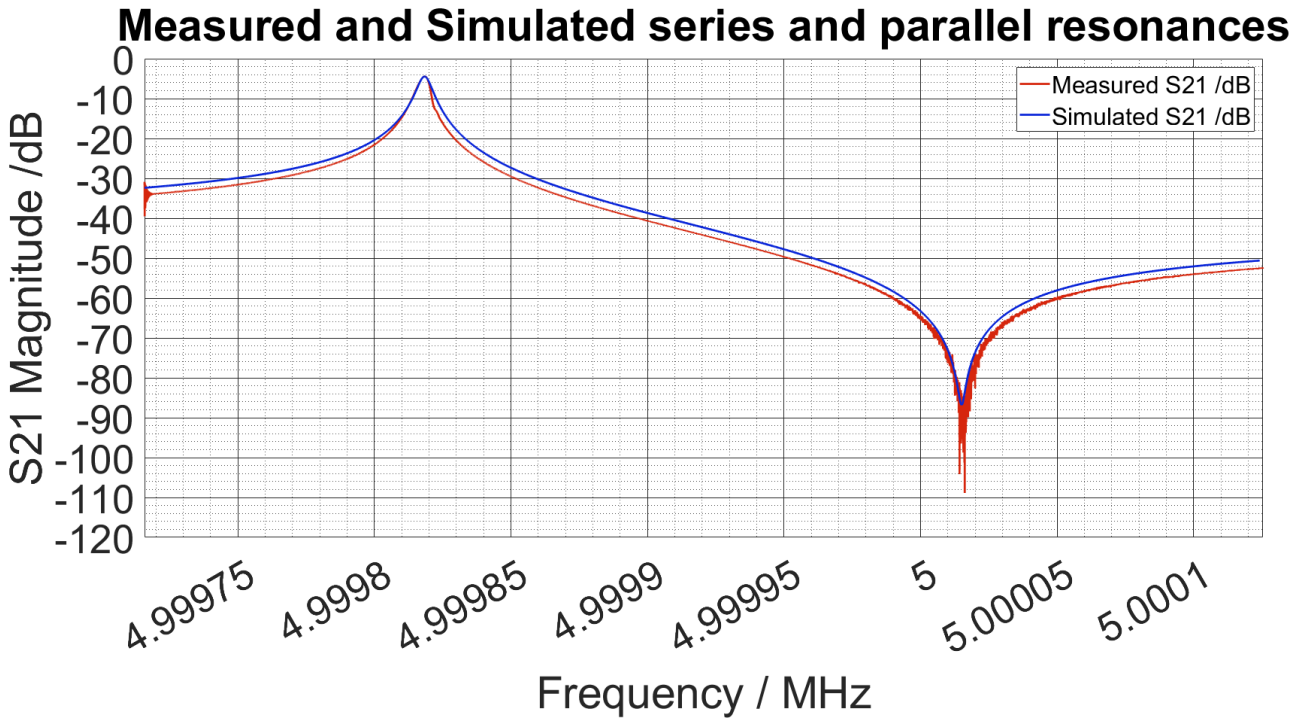
The series resonant frequency is given in (6.2) which can be rearranged for the series capacitance.

$$\omega_s = \frac{1}{\sqrt{L_S C_S}} \rightarrow C_S = \frac{1}{w_0^2 L_S} = \frac{1}{(2\pi \times 4.999818)^2 \times 10^6 \times 4.898} = 206.9\text{aF} \tag{6.2}$$

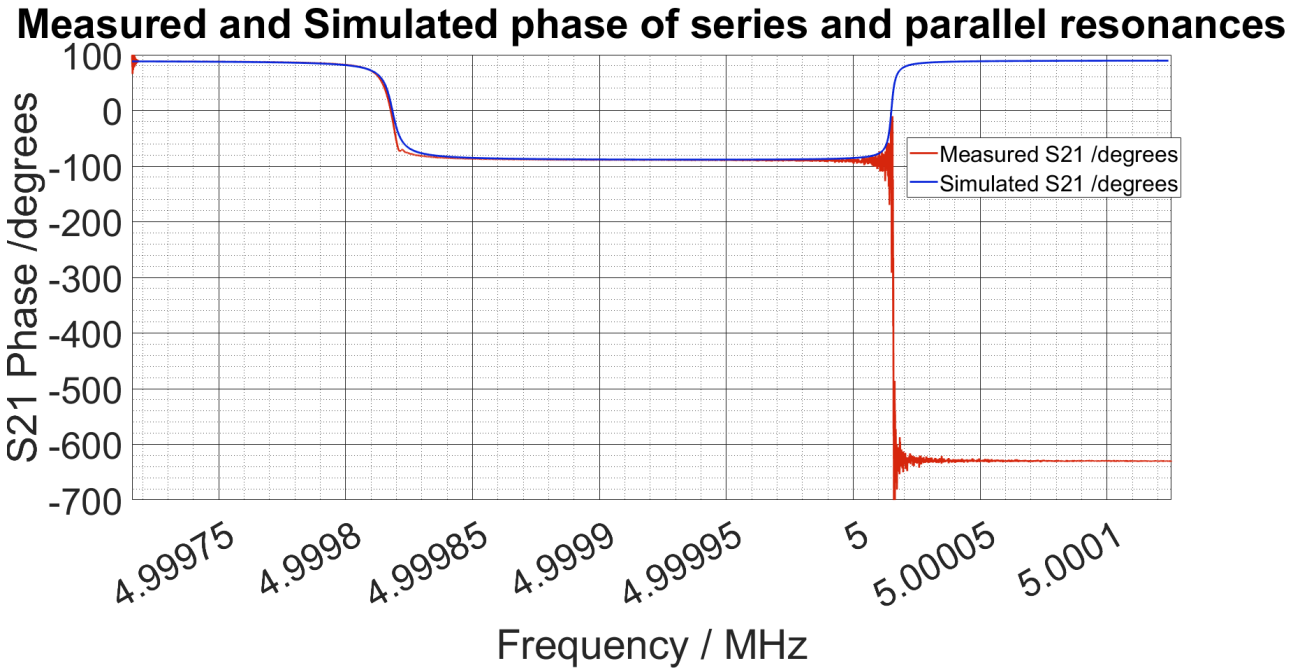
The parallel capacitance is a parasitic effect of the resonator package, at this frequency the reactance of the series LC equals the reactance of the parallel capacitor. (6.3) gives the parallel resonant frequency, it can be rearranged for C_P, the parallel capacitance.

$$\omega_p = \frac{1}{\sqrt{L_S\left(\frac{C_P \times C_S}{C_P + C_S}\right)}} \rightarrow C_P = \frac{C_S}{2\left(\frac{\omega_P}{\omega_S} - 1\right)} = \frac{206.9 \times 10^{-18}}{2\left(\frac{5.000014 \times 10^6}{4.999818 \times 10^6} - 1\right)} = 2.63\text{pF} \tag{6.3}$$

The resonator was modelled in ADS and an S-Parameter simulation was carried out to tune the components values to accurately reflect the measured resonator. Figure 6.3 is the equivalent circuit



(a) Measured and simulated magnitude of S_{21}.



(b) Measured and simulated phase of S_{21}.

Figure 6.4: Measured and simulated S_{21} of the 5 MHz crystal resonator.

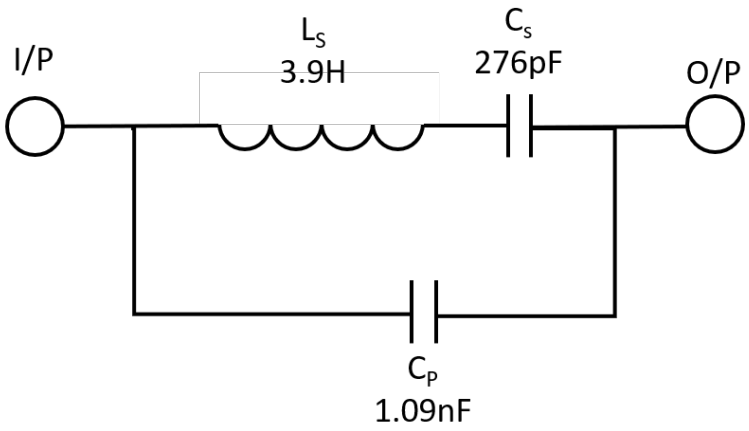


Figure 6.5: Schematic of spurious resonance filter.

model for the resonator with the calculated component values. The tuned values are listed in brackets. Figures 6.4 shows the plots of the measured and simulated magnitude and phase of S_{21}.

Spurious Resonance Filter

As noted in Figure 6.1, there is a spurious resonance at 5.44 MHz that could cause the oscillator to oscillate at the wrong frequency. The insertion loss at the peak of the spurious resonance was measured to be -3.01dB, it must be attenuated by implementing a notch filter. The spurious resonance filter is a modified crystal equivalent circuit with no resistive losses, other than parasitic effect of the components which minimises passband losses and stop band damping. The schematic of this circuits is depicted in Figure 6.5. This design uses the parallel resonance to attenuate stop band frequencies, as is observed in the plot of the resonator insertion loss in Figure 6.2. The series inductor and capacitor component values can be calculated using (6.2) and setting the series resonant frequency to be 5 MHz. The value of capacitance selected for use was 276pF and therefore the inductor value must be 3.9μH. As there are no series resistive components the inductor Q is the only component that defines the notch bandwidth. A high Q is required to ensure sufficient stop band attenuation, a self wound air core inductor was manufactured by hand to achieve this. Air cored inductors typically offer higher Qs than ferrite core components [104]. Manufacturing by hand allowed for fine adjustments of the inductance by adding an additional winding until the precise value of inductance was reached. For inductors

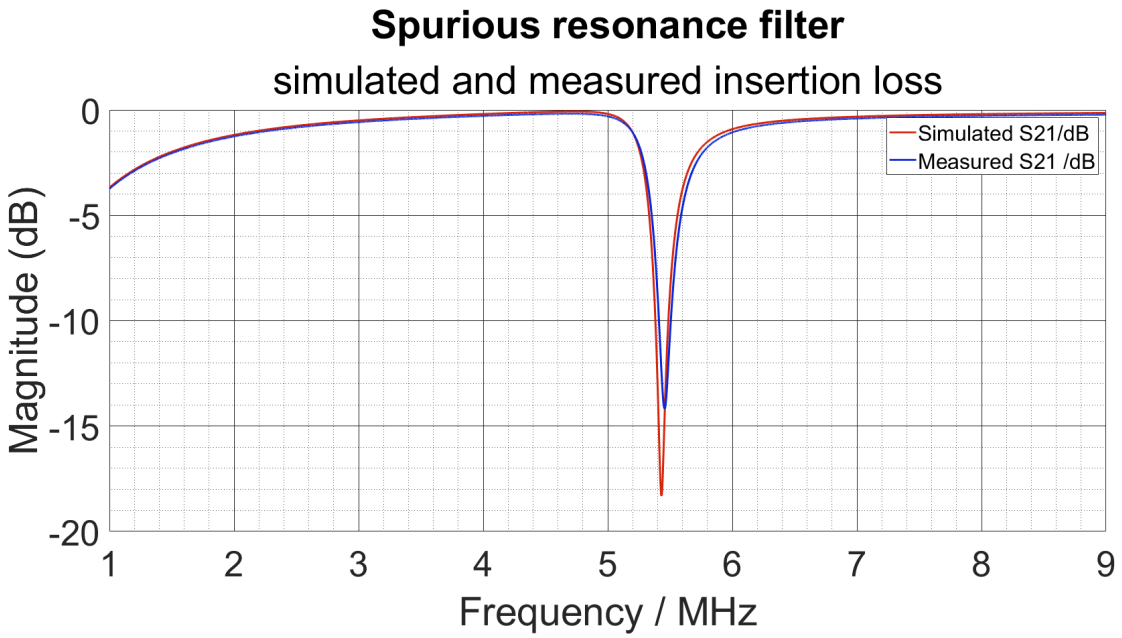


Figure 6.6: Measured and simulated insertion loss of the notch filter.

where the diameter d is much smaller than the length l, the inductance in nH can be approximated by (6.4). A full derivation of this approximation is given in [104].

$$L \approx \frac{N^2 \times d^2}{l} \tag{6.4}$$

The diameter of the core is 6.9mm and the length is approximately 30mm, for 3970nH or 3.97μH, 50 turns are required. The inductance was measured using a Digimess automatic RLC meter [105] to be 3.94μH.

The parallel capacitance is calculated using (6.3) and the parallel resonant frequency of 5.44 MHz given a value of 1.09nF. Both the series and parallel capacitors were parallel combination of polystyrene film capacitors to reduce the resistive parasitics that would increase passband loss and stop band damping. A range of capacitors were measured individually to find capacitors with capacitance closest to the required filter parameters. These components were also measured using the Digimess automatic RLC meter. The S-Parameters of the filter were measured and S_{21} is plotted in Figure 6.6 which also includes a plot of the simulated S-Parameters generated using ADS. There is good agreement between the simulated response and the measured response, at 5.44 MHz the measured insertion loss is -13.4dB

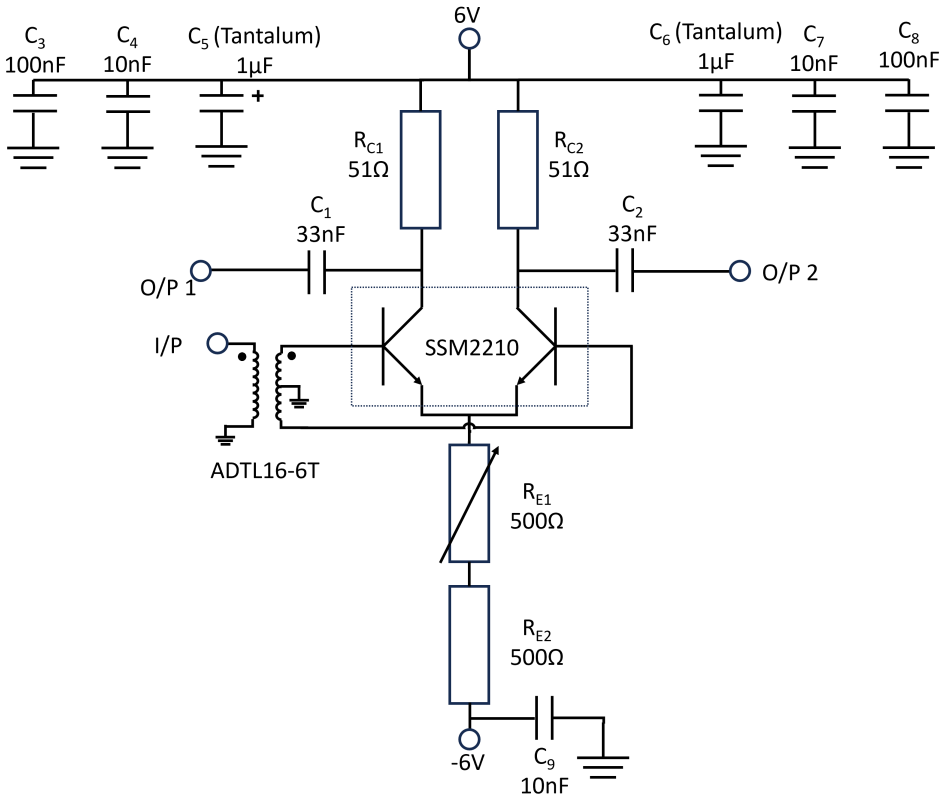


Figure 6.7: Long tailed pair differential amplifier with input impedance transformer and variable emitter resistor.

whereas at 5 MHz the insertion loss is -0.31dB.

6.3 Long-tailed Pair Differential Amplifier

6.3.1 Amplifier Design

The amplifier used in this work is based on the amplifier design presented in [3], the same device, the SSM2210 [106], though the output power had decreased in the design presented here. A long tailed pair with a super matched NPN transistor pair was used in a differential amplifier to limit the output power without saturating the amplifier, avoiding non linear effects and reducing AM noise of the oscillator. The two outputs are useful for providing the same output signal to the feedback loop and the output of the oscillator, though 180° out of phase. The device selected for use was the Analog

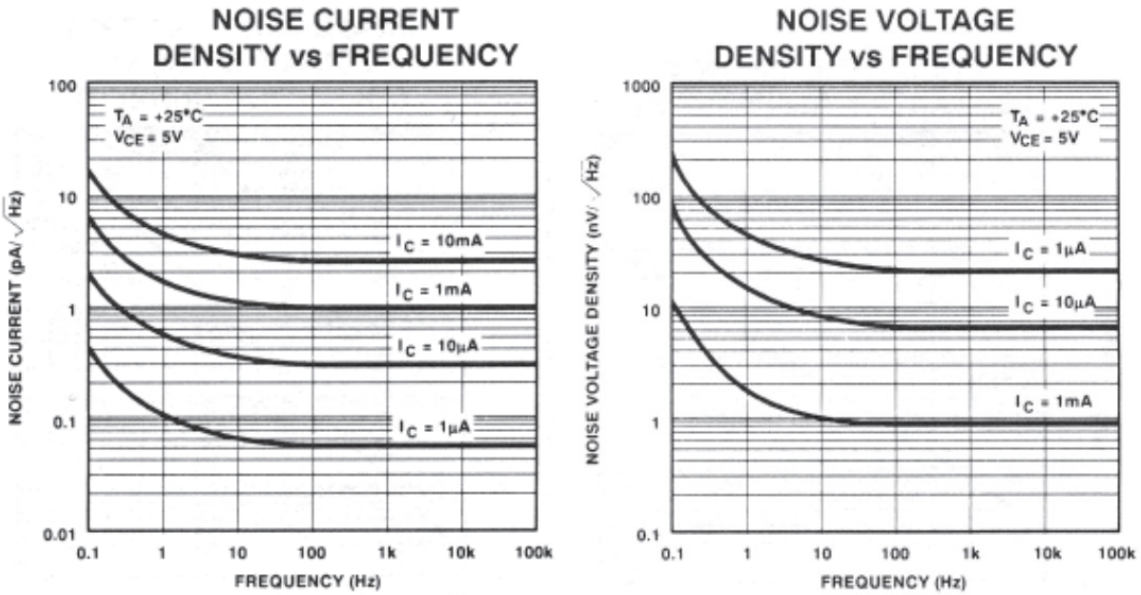


Figure 6.8: Plots of noise voltage and current density plotted against frequency, taken from the SSM2210 datasheet [106].

Devices SSM2212 as they are low noise and offer good symmetry. These devices offer a noise voltage density of less than $0.9\text{nV}/\sqrt{\text{Hz}}$ for collector currents greater than 1mA and frequencies greater than 100k. The noise current density is between 1 and $3\text{pA}/\sqrt{\text{Hz}}$ at frequencies greater than 100 kHz and collector currents between 1 and 10mA [106]. The flicker noise corner is estimated using the noise current density vs frequency plot on the datasheet, to be between 1 and 10 Hz depending on the current (shown in Figure 6.8). The output impedance is required to be 50Ω which can be set by making the collector resistors equal to 50Ω. The amplifier should provide a maximum power to the crystal of 200µW (-6.98dBm). A full derivation of the emitter resistance required to set the collector currents to achieve this range of drive power is shown in the report by Tim Nankervis who started this work for a BEng project [4]. The emitter resistor required to deliver the maximum drive power is 500Ω and the collector current in each transistor is therefore 5.79mA. The minimum drive power was set to be 50µW, the emitter resistance is shown to be 1kΩ and the collector current is 2.89mA.

The bases of the transistor pairs are driven differentially via an ADT16-6T impedance transformer that, transforms the source impedance of 50Ω to 800Ω. There are two secondary winding with a centre tap. Optimum source impedance for low noise is given by equation $\text{R}_{\text{S0}} = \frac{\text{e}_\text{n}}{\text{i}_\text{n}}$, a full derivation of this

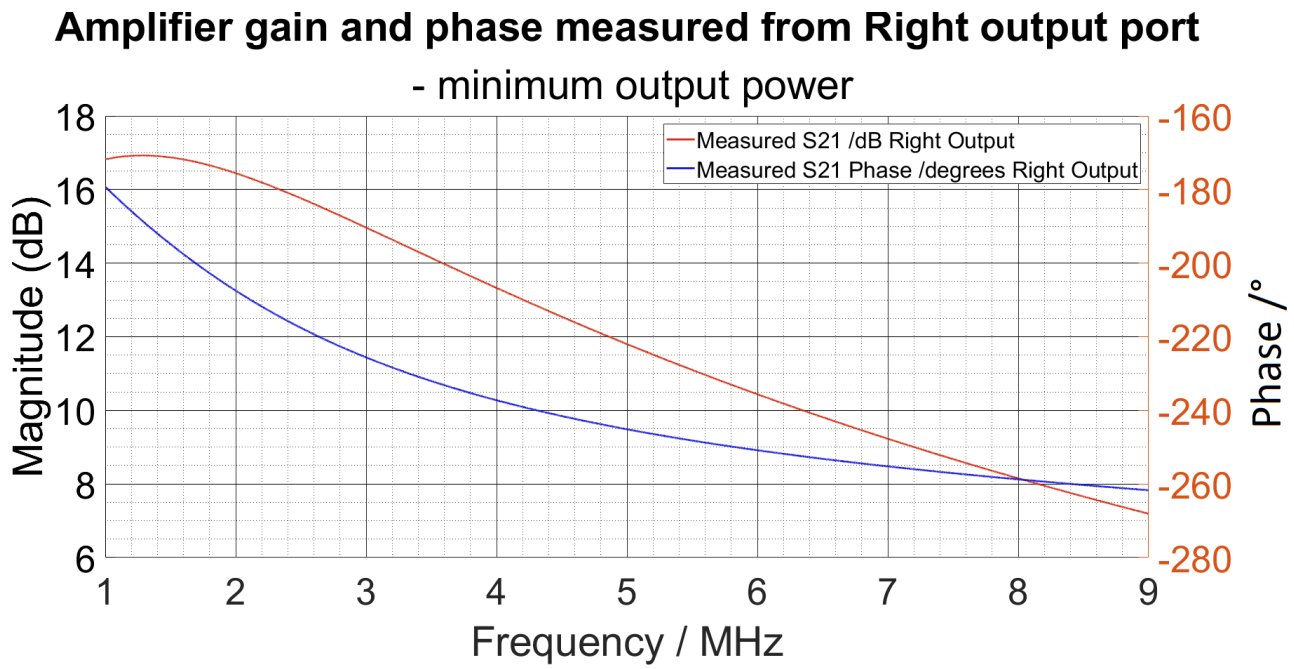
equation is presented in [107]. For a collector current in the range 2.89mA-5.79mA, the noise current density is approximately $2\text{pA}/\sqrt{\text{Hz}}$ and the noise voltage density is approximately $0.8\text{nV}/\sqrt{\text{Hz}}$, the optimum source impedance is 400Ω. The impedance transformer operating differentially presents an impedance of 400Ω to each transistor which is found to be optimum for a collector current of approximately 6mA. The circuit diagram for the amplifier module is shown in Figure 6.7 including ceramic decoupling capacitors on the outputs and near the voltage supplies. A polarised tantalum capacitor was also included near the voltage supplies to filter lower frequencies.

6.3.2 Amplifier Measurements

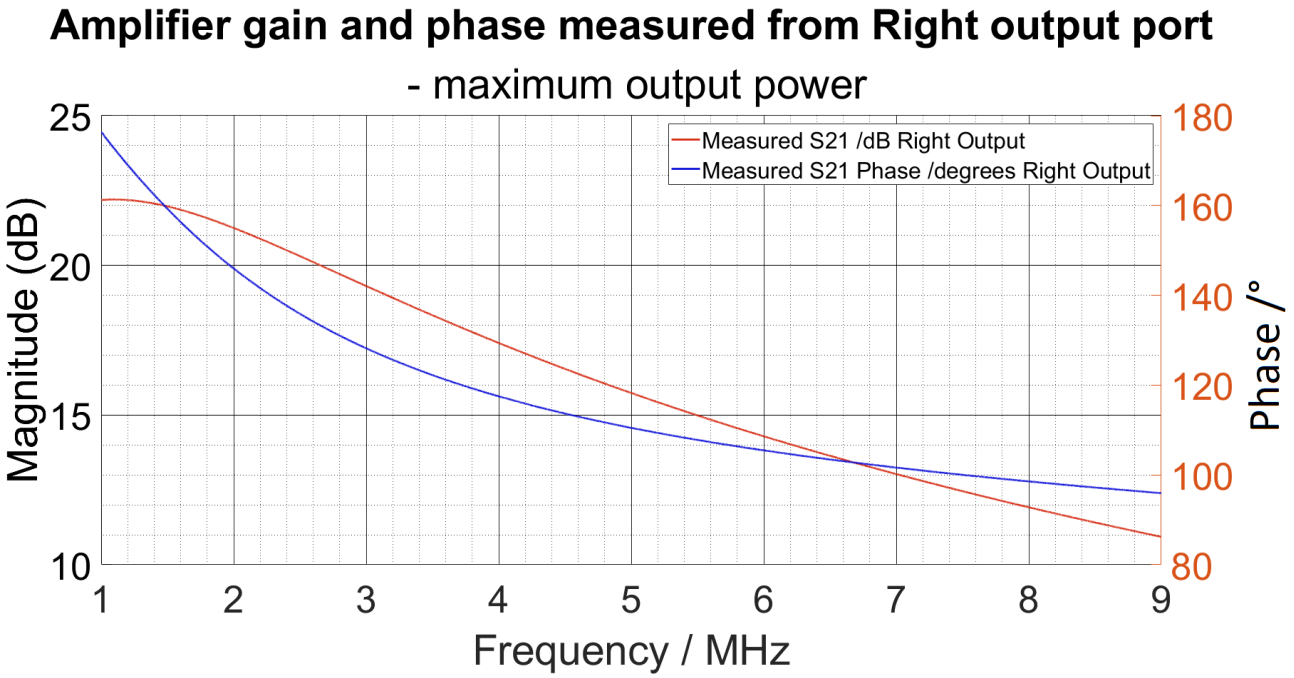
The amplifier design was manufactured using Rogers 4003 [68] low loss substrate using the Gerber file produced for [4]. A Bourns 3224X500 500Ω potentiometer was used for the variable resistor. Figure 6.9 contains the measured gain and phase of the differential amplifier in both minimum and maximum output power configurations. Output 2 was measured as this is used for the oscillator output, output 1 was terminated in 50Ω, the gain at 5 MHz was measured to be 11.8dB and 15.7dB in the minimum and maximum states respectively. The phase at 5 MHz was measured to be –65.1° and –69.5° for minimum and maximum output power respectively. Output 1 was also measured with output 2 terminated in 50Ω and in both power configurations, the gain was measured to be 11.8dB and 15.7dB showing that the supermatched pair are equally balanced. The measured phases were 110.5° and 115.0, 175.6° and 184.5° out of phase with their respective right side output.

6.4 Electronically Tunable Phase Shifter

The phase shifter designed in this section provides a tunable phase shift to the oscillator. The range of phase shift introduced is smaller in this circuit than in phase shifters used in previous chapters as the wavelength of a 5 MHz is much larger that the other frequencies and therefore the phase shift remains reasonable constant regardless of the length of interconnecting cables used to connect the resonator, amplifier and filter circuits together. The phase shifter should introduce an absolute phase shift to ensure the Barkhausen criterion is met but should also be able to vary the phase shift to counteract the ageing effect of the crystal. Over time the crystal resonant frequency and therefore the phase shift



(a) Minimum amplifier gain, potentiometer set to 500Ω.



(b) Maximum amplifier gain, potentiometer set to 0Ω.

Figure 6.9: Minimum and maximum gain and phase measurement for the differential amplifier.

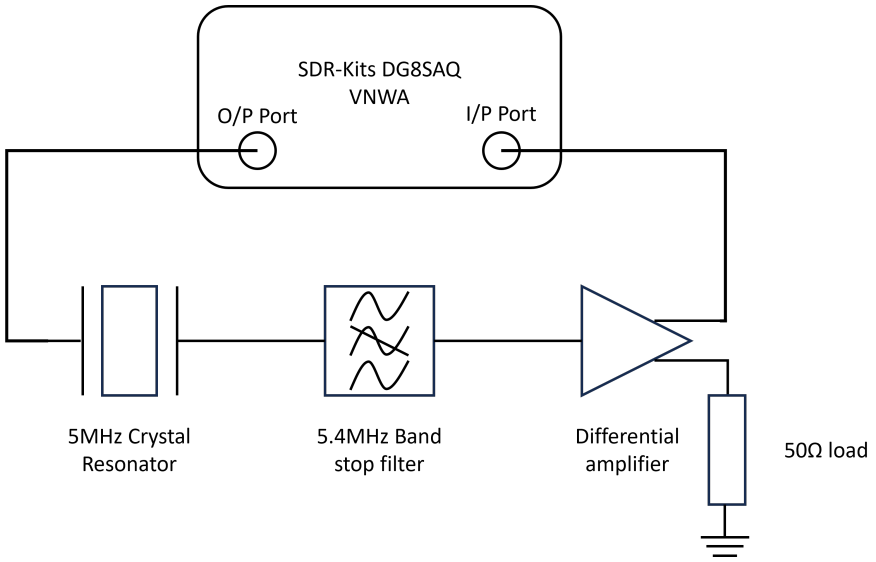
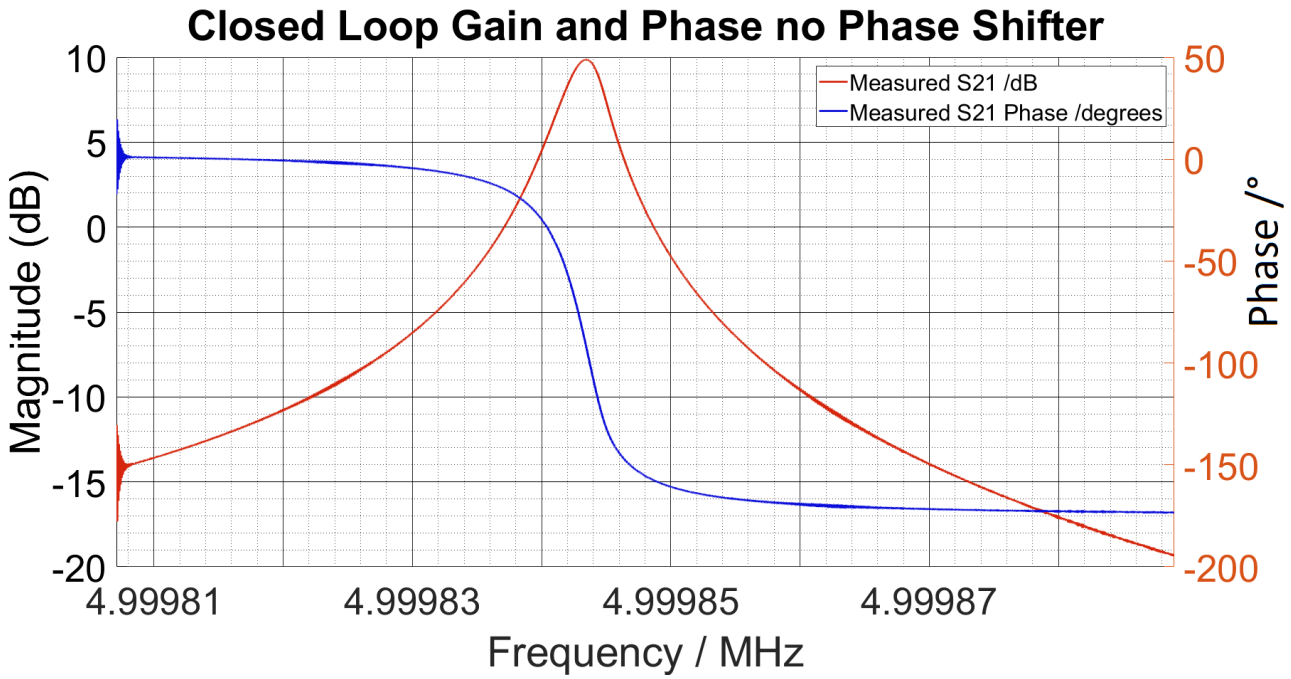


Figure 6.10: 5 MHz oscillator closed loop S-Parameter measurement setup. The oscillator components except for the phase shifter are connected in series to measure the excess gain and phase of the loop at 5 MHz.

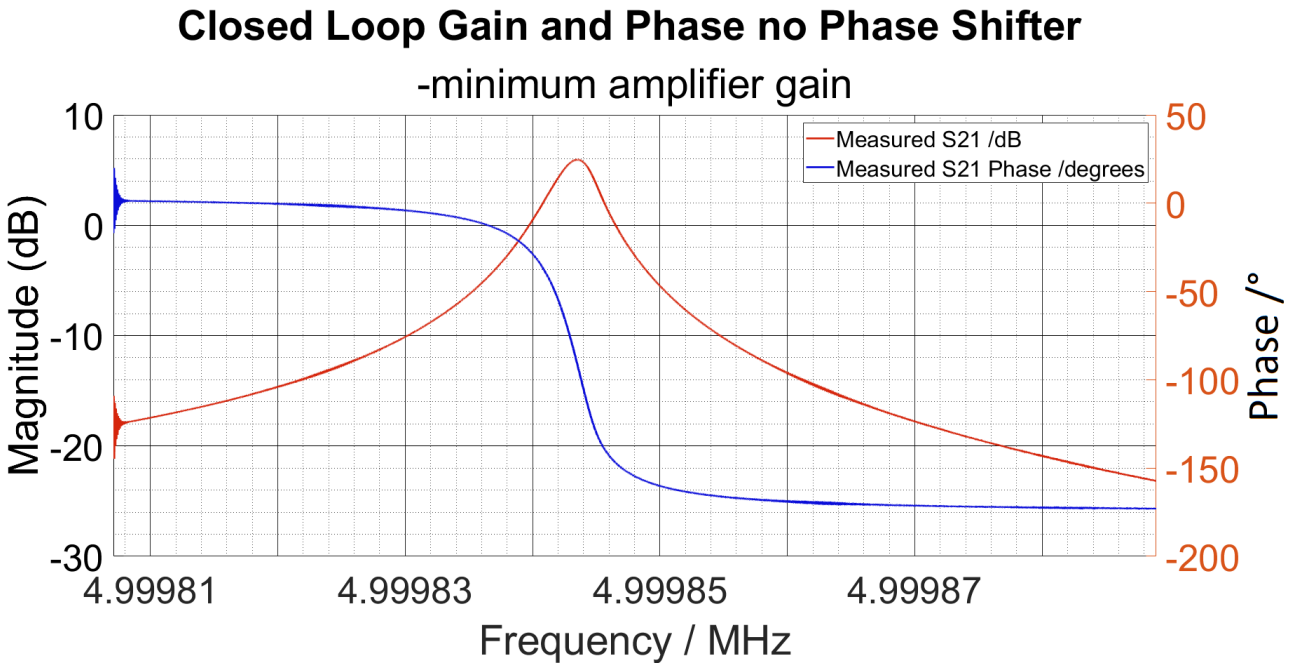
introduced by it will change, a tunable phase shifter allows for the loop phase to be varied to $N \times 360°$ at the resonant peak.

6.4.1 Closed loop Phase Shift

An S-Parameter measurement was made to find the excess gain of the loop and the phase shift of S_{21} at 5 MHz using the SDR Kits DG8SAQ vector network analyser [103] that must be corrected for by the phase shifter. The other oscillator components are connected in series in the order they would be connected in the oscillator loop. The output from the DG8SAQ was connected to the crystal, the spurious resonance filter was then connected to the crystal output and finally the amplifier was connected to the filter's output. The output from the left amplifier output was then connected to the DG8SAQ and the right output was terminated with a 50Ω load. Figure 6.10 is a diagram of the measurement setup. Two measurements were made, one with the maximum amplifier output power and one with the minimum. The insertion loss at resonance, 4.99 MHz was measured to be 9.84dB with the maximum amplifier output power and 5.94dB with the minimum. The loop phase shift was measured to be –91.0° with the maximum amplifier output power and –89.6° with the minimum



(a) 5 MHz oscillator closed loop S-Parameter measurement with maximum amplifier output power. At resonance the insertion loss is 9.84dB and the phase shift is $-91.0°$.



(b) 5 MHz oscillator closed loop S-Parameter measurement with minimum amplifier output power. At resonance the insertion loss is 5.94dB and the phase shift is $-89.6°$.

Figure 6.11: Closed loop S-Parameter measurements with maximum and minimum amplifier output power.

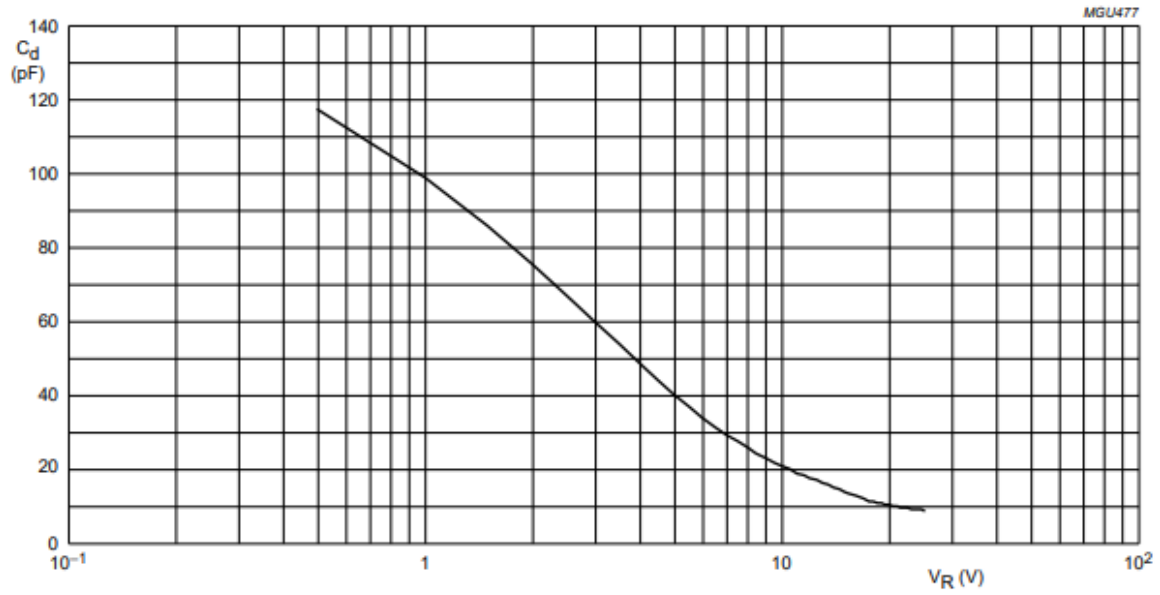


Figure 6.12: CV characteristics of the BB201 varactor diode [108], from 0-12V reverse voltage the range of capacitance is from 118pF - 9pF.

output power. Therefore, the phase shifter must provide a range of possible phase shift that covers the range 89.6 – 91.0° to ensure the oscillator phase shift can be tuned so that the oscillation frequency is the resonant frequency of the crystal with any amplifier drive level. Figure 6.11 shows plots of the insertion loss and phase shift for both measurement configurations.

6.4.2 Modified High Pass Filter Design

The previous iteration of the 5 MHz crystal oscillator used a 10m length of coaxial cable to ensure the loop phase was an integer multiple of 360°. This is bulky and cannot be modified easily to adjust the phase shift for different amplifier output powers or to account for the ageing of th crystal causing the resonant frequency to change. As observed in the previous section, the required range of phase shift is 89.6 – 91.0°.

A tuneable phase shifter was required and the modified high pass structure used in Chapters 3 and 4 was used to achieve this aim. As with the previous phase shifter designs the capacitors were replaced with varactor diodes and the inductor L2 was connected to a bias voltage instead of shunting to ground. The varactor diode used in this phase shifter was the NXP BB201 varactor diode [108].

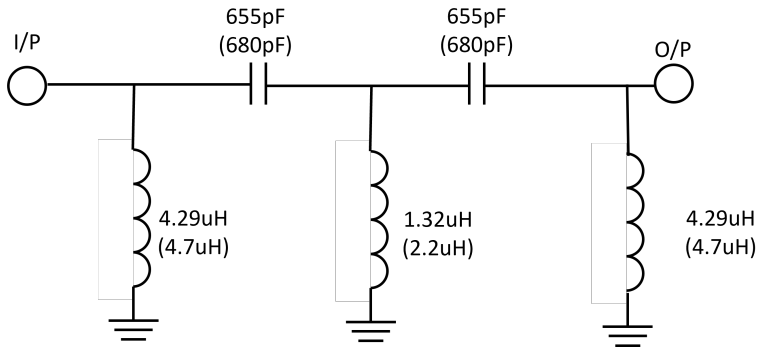


Figure 6.13: 5th order Butterworth high pass filter where $f_0 = 2.4\text{MHz}$ and denormalised to 50Ω.

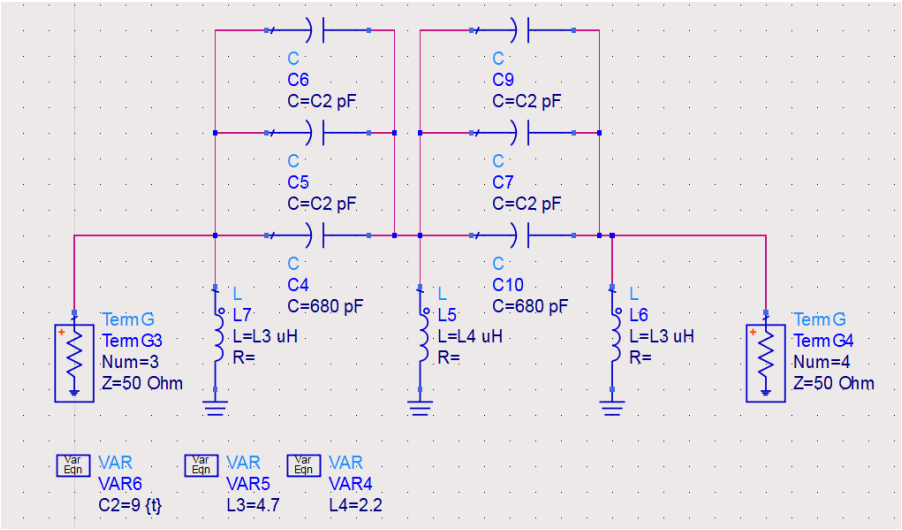


Figure 6.14: Modified 5th order Butterworth high pass filter including parallel tunable capacitors to model the phase shifter tuning range.

The CV characteristics of the varactor diode are shown in Figure 6.12 which shows that the maximum range of capacitance is 9pF - 118pF. Two varactor diodes are placed in parallel with each other and a further capacitor in the actual circuit to increase the capacitance to a value suitable for use in the modified high pass filter

A 5th order Butterworth high pass filter was designed for a cut off frequency of 2.4 MHz and denormalised to 50Ω. This cutoff frequency was chosen so that the phase shift introduced by the circuit was slightly larger than the maximum required 91.0° but also it introduces low insertion loss at 5 MHz. It was shown in ADS simulation that a 5th order high pass Butterworth filter designed for

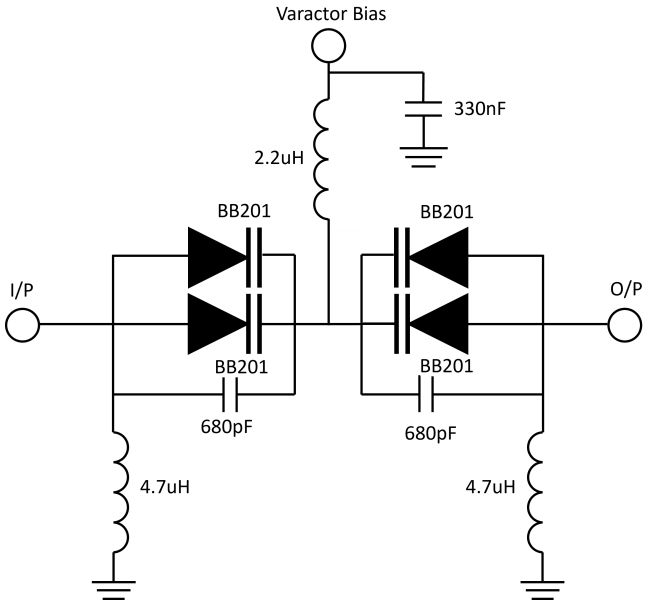


Figure 6.15: 5 MHz phase shifter schematic based on a 5th order butter worth high pass filter. A 330nF capacitor is used for decoupling, the bias voltage is applied via inductor L2 as this is used to isolate the RF line from the DC path.

a cutoff frequency of 3 MHz ($0.6 \times f_0$, see Chapter 3) would have a phase shift of 117.9°, much greater than the required phase shift which cannot be reduced at 5 MHz sufficiently with the introduction of the varactor diodes. With a cutoff frequency of 2.4 MHz the phase shift at 5 MHz is simulated to be 91.9°, Figure 6.13 is the schematic of the high pass filter used as the basis of the phase shifter. Standard E12 component values nearest to the final were selected, these are included in brackets in Figure 6.13.

A spice model for the varactor diode was unavailable so the ADS model made use of the tuning function to simulate the possible range of phase shift at 5 MHz. The two series capacitors are replaced with a parallel combination of a capacitor and two varactor diodes that were modelled as tunable capacitors in simulation. The tuning range of the capacitors was from 9-118pF. Increasing the capacitance in simulation decreased the overall phase that can be achieved by decreasing the bias voltage to the varactor diodes on the real circuit. At 5 MHz the simulated range of phase shift was 81.7 – 94.1° with the insertion loss varying from -0.003dB to -0.066dB. Figure 6.14 is an image of the ADS model used in simulation and the final schematic for the phase shifter circuit is shown in Figure 6.15.

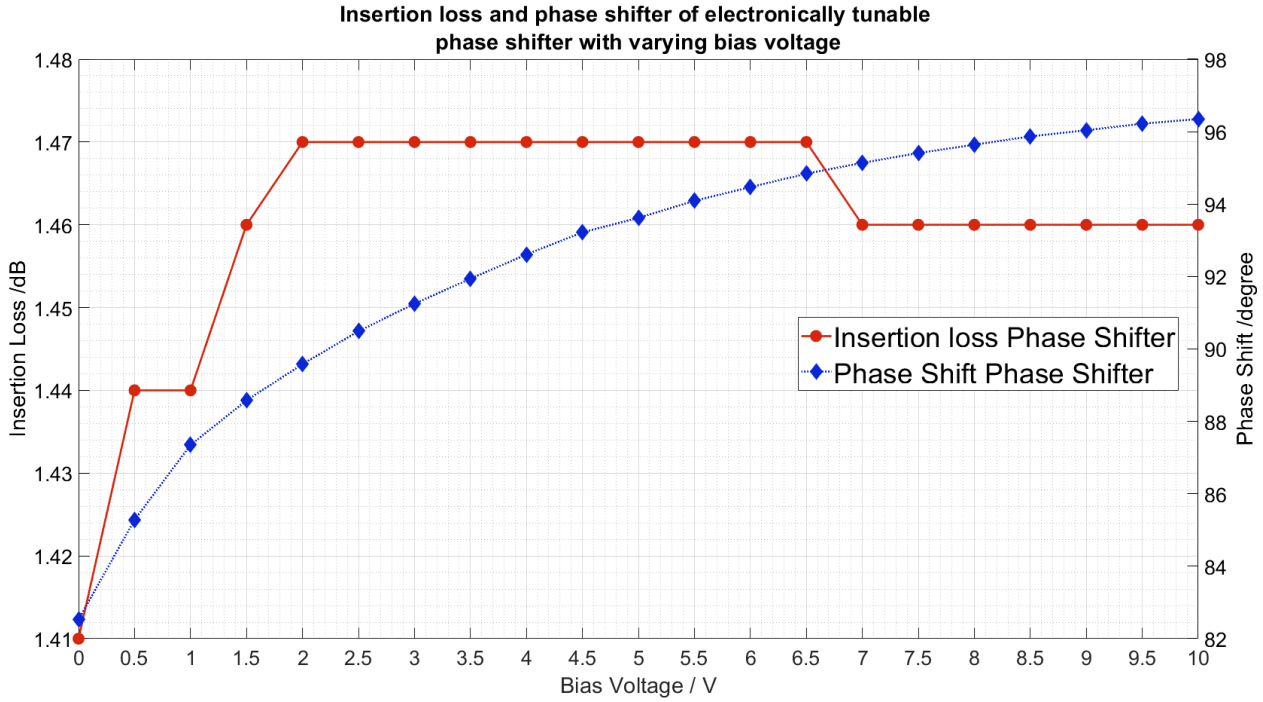


Figure 6.16: Measured insertion loss and phase shift of the voltage controlled phase shifters.

6.4.3 Phase Shift Measurements

A PCB for the 5 MHz phase shifter was designed and manufactured on 0.508mm Rogers 4003 [68] low loss substrate. High quality Coilcraft inductors and polystyrene capacitors were used to keep the noise figure low. The insertion loss and phase shift was measured against bias voltage , these measurements are plotted in Figure 6.16. The phase shifter can introduce a phase shift from 82.53° to 96.35° with 0-10V bias. From these measurements it is predicted that a bias voltage to the phase shifter between 2 and 3V would be sufficient to change the oscillator loop phase to an integer multiple of 360°. The insertion loss at 5 MHz varies from 1.41dB to a maximum 1.45dB across the full tuning range.

6.5 Oscillator Measurements

The crystal oscillator block diagram is shown in Figure 6.17, the assembled oscillator was connected in this order and housed in an aluminium enclosure, with the three PCBs screwed into the base. The crystal pins are soldered to wires connected to the the input of the band stop filter and the

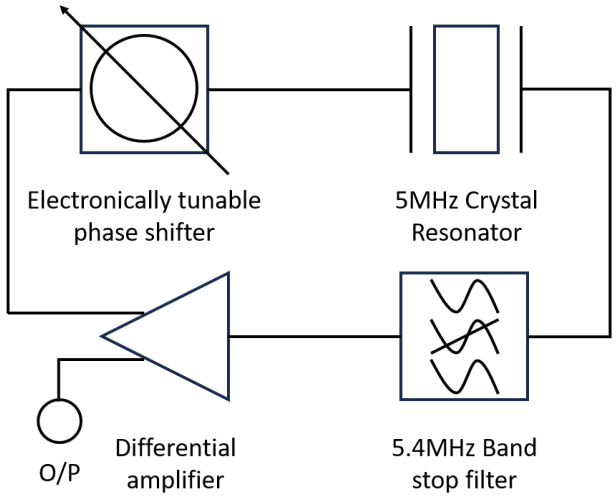


Figure 6.17: Complete 5 MHz crystal oscillator block diagram.

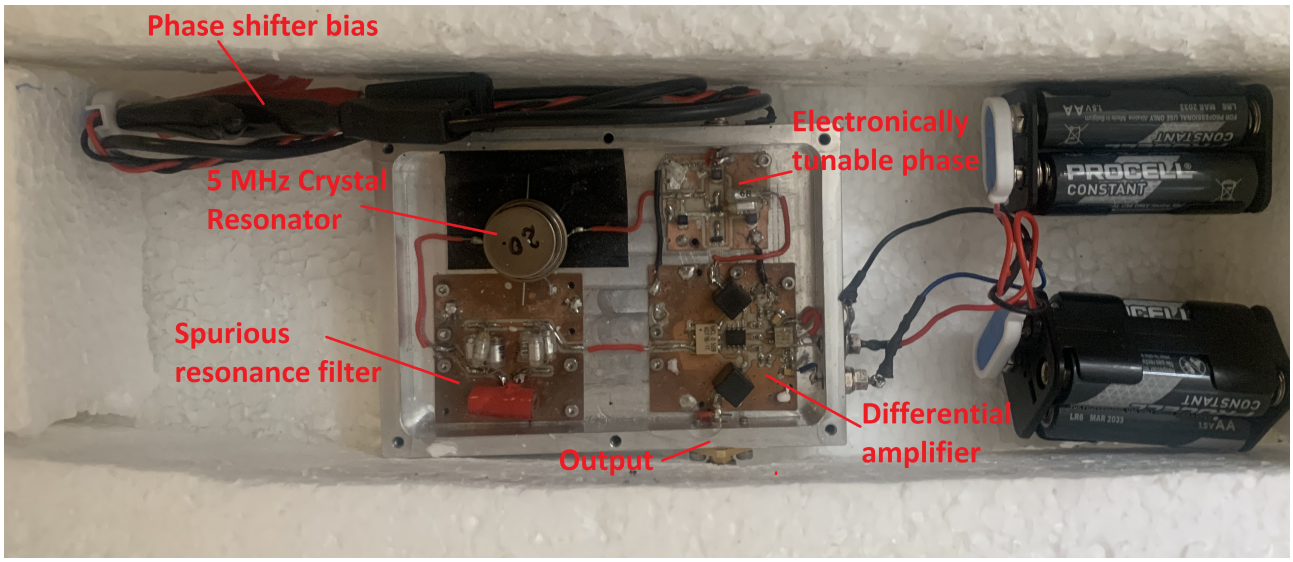


Figure 6.18: 5 MHz Oscillator enclosed in polystyrene and placed within a shielded box.

output of the tunable phase shifter, a third pin is grounded. Figure 6.18 is an image of the oscillator components housed in an aluminium box. The metal box was surrounded by polystyrene to reduce local temperature variations affecting the measurements.

AA batteries were used to reduce any bias line phase noise modulations that could increase the oscillator phase noise. This restricts the possible varactor diode bias voltages to multiples of 1.5V.

Two 6V battery packs were used to power the amplifier, each using four brand new 1.5V AA batteries. The measured voltages supplied from the batteries were were +6.37V and -6.36V. Four oscillator phase noise measurements were made, with varactor bias voltages of 0V and 1.6V. It was found that the oscillation could not be sustained with a varactor bias voltage of 3V. One AA cell was measured and provided 1.6V bias voltage.

Various oscillator phase noise measurements were made using the R & S FSWP 50 phase noise measurement system, varying the amplifier output power and varactor diode bias voltage. It was found that the lowest close to carrier phase noise was achieved with -9.64dBm output power from the amplifier using 0V phase shifter bias. The oscillator phase noise measurement for this configuration is plotted in Figure 6.19. At 1 Hz offset the oscillator phase noise is -132dBc/Hz and the far from carrier noise is -160dBc/Hz. The graph also includes a plot of the theoretical oscillator phase noise calculated using (2.59) where P_{AVO} = –11dBm, F_C = 50Hz, Q_L = 950540, Q_0 = 2506315 and F_1 = 2.3dB. The noise figure was measured at 10 MHz as the HP 346 noise source has a minimum frequency of 10 MHz. The measured oscillator phase noise also suggests that the noise figure of the device at 5 MHz is lower as the theoretical noise at greater than 10 kHz is larger than the measured noise at the same frequency offsets.

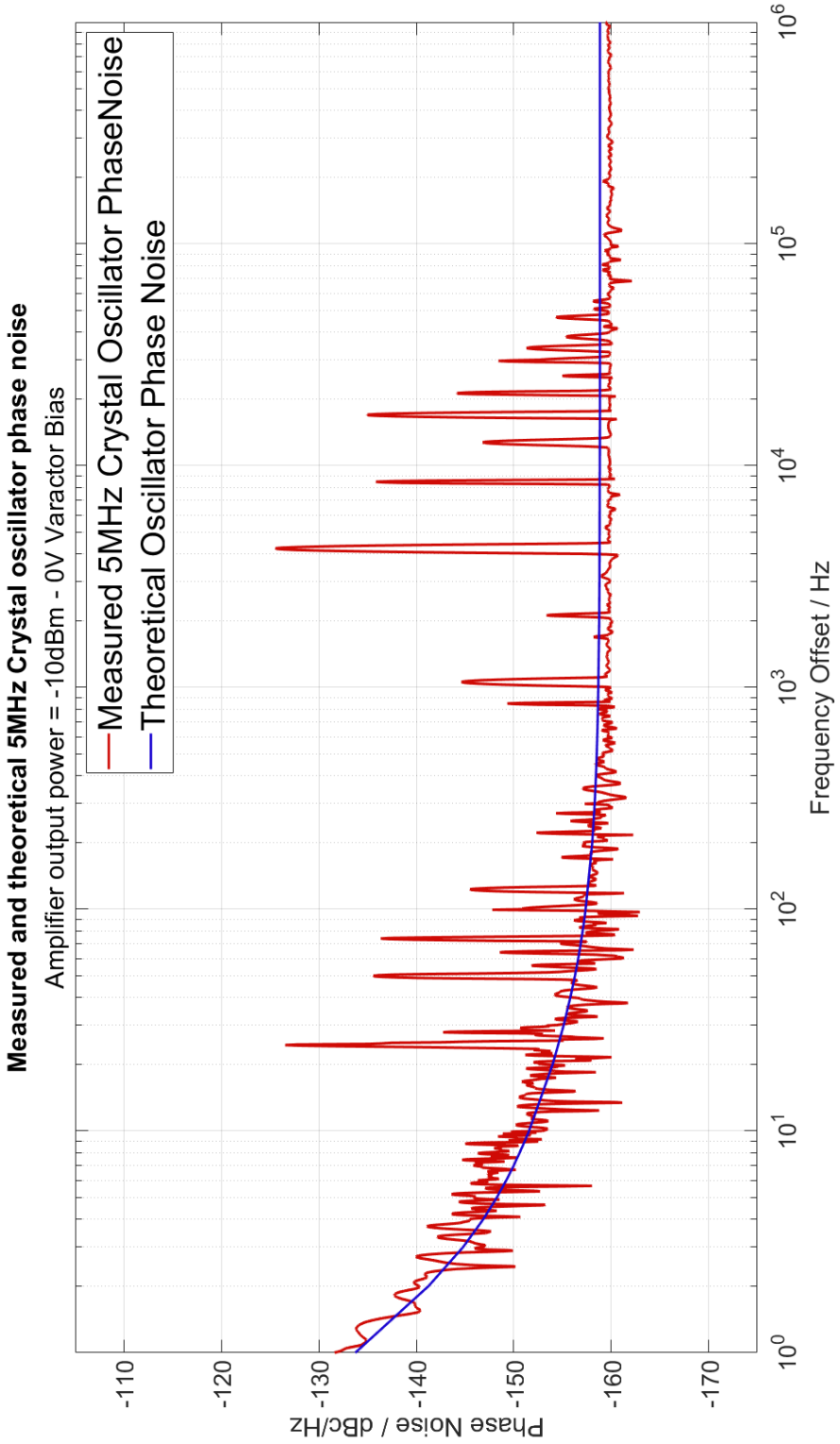


Figure 6.19: 5 MHz oscillator phase noise measurement with theoretical phase noise plotted on the same graph.

6.6 Conclusions and further work

This work has achieved state-of-the-art oscillator phase noise performance exceeding previous measurements made by this group of the 5 MHz crystal oscillator of -118dBc/Hz at 1 Hz offset by 14dB, achieving -132dBc/Hz. Furthermore the previous measurement of -147dBc/Hz at 10 Hz offset has been improved by approximately 6dB presented here where an oscillator phase noise measurement of -153dBc/Hz. The far from carrier noise in the oscillator presented in this chapter is -160dBc/Hz, approximately 2dB higher than the previous measurement of -162dBc/Hz. It is thought that this due to the noise figure of the amplifier increasing as the amplifier output power was varied to find the lowest phase noise at 1Hz offset.

It is also 4dB better at 1 Hz offset than the previously presented 10 MHz oscillator when scaled to 10 MHz (+6dB). The oscillator phase noise at 1Hz offset of the BVA resonator oscillator [100] is measured at -136dBc/Hz where P_{AVO} was -10dBm and the noise figure of the feedback components was 3.5dB. This is 4dB lower than the phase noise of the oscillator measured at 1Hz offset in this chapter.

In the oscillator developed in this chapter the P_{AVO} was -11dBm and the noise figure was estimated to be 2.3dB. The increased P_{AVO} of 1dB in [100], would decrease the oscillator phase noise by 1dB compared to the 5MHz oscillator developed in this chapter. The noise figure of the feedback components in the oscillator developed in this chapter is 1.2dB smaller which would improve the phase noise measurement by 1.2dB compared to the BVA oscillator. Therefore a net improvement of 0.2dB would be expected by the oscillator developed here. The BVA oscillator phase noise is actually measured to be 4dB lower at 1Hz offset suggesting that the BVA resonator alone can improve the oscillator phase noise by approximately 3.8dB.

The 5MHz oscillator measured in this chapter has measured oscillator phase noise at 1Hz offset that is 2dB better than that of phase noise than the 3.9MHz oscillator [101]. If the frequency of the 3.9MHz oscillator was scaled to 5MHz, the phase noise at 1Hz offset would be -128dBc/Hz, approximately 4dB worse than the performance of the 5MHz oscillator presented here.

Furthermore, scaling the oscillator frequency of the 20MHz crystal oscillator down to 5MHz would improve the measured oscillator phase noise of the oscillator presented in [102] from -97dBc/Hz to

-109dBc/Hz. The 5MHz oscillator presented here would still offer an improvement in oscillator phase noise of 23dB.

Further work should look to developing a temperature stabilising oven for the crystal that will decrease frequency drift due to temperature variation. A measurement of the Allan deviation should be carried out to measure the long term stability of the oscillator before and after any potential additions of an oven to the oscillator.

The oscillator uses low flicker noise amplifiers though it may be possible to further improve on the flicker corners of the amplifiers by introducing parallel amplifiers or the feedforward technique. Both of these techniques will present challenges as the parallel combination of amplifiers will increase the output power of the amplifier and the feedforward technique will require very large phase shifters to accurately adjust the phase of the two paths. Furthermore, it was observed at 100 MHz that the high Q_0 crystal resonator oscillator was highly susceptible to phase changes in the tuning of the amplifier loops causing the oscillator loop phase to move significantly away from the required phase. This resulted in the oscillation stopping.

BVA crystal resonators could replace the current resonators in order to improve upon the close to carrier phase noise with the aim of achieving better than the minimum -136dBc/Hz at 1 Hz offset measured in [100].

Chapter 7

Conclusions and future work

The aim of this research was to develop ultra low phase noise oscillators, four different oscillator configurations have been presented. A detailed design process of a dielectric resonator oscillator operating at 1.5 GHz is presented which builds on previous research undertaken by this research group [26, 36] which culminates in state-of-the-art phase noise measurements. A 16 GHz distributed Bragg resonator oscillator has been assembled including parallel amplifiers to suppress flicker noise and increase the power available to the resonator. The development of the feedforward amplifier technique applied to an oscillator to suppress flicker noise is also presented without the need for PIN diode limiters. A 100 MHz oscillator using this amplifier has been built showing noise suppression of at least 20dB. Finally, a 5 MHz crystal oscillator is developed with state-of-the-art phase noise of -132dBc/Hz at 1 Hz offset.

7.1 1.5GHz DRO discussion and suggested further work

The development of a 1.5 GHz dielectric resonator oscillator has been presented where the main achievements were housing all the individual components within a single aluminium enclosure, a fully tunable phase shifting network to allow for the oscillator loop phase to be adjusted across the full 360° range and the tailored resonator coupling and housing. Ultra low phase noise measurements of two oscillators are presented demonstrating -164dBc/Hz at 10kHz offset, an improvement of 1dB when compared to the previous iteration developed by this research group. Reasons for the degradation

of the phase noise performance when compared to the 1.25GHz DRO developed by this group [26] are given with suggestions on how to achieve improved phase noise measurements. These suggestions include replacing the amplifiers with a single stage to reduce the noise figure and replacing the resonator with a resonator designed to operate at 1.5GHz with an unloaded Q closer to the predicted 50,000.

This DRO outperforms the closest comparable DRO in the literature, the Ingenieurbüro Gronefeld GDRO2856 [38], at 10kHz offset by 3.65dB when taking into account the frequency scaling from 2.856GHz, GDRO2856 operating frequency, to 1.5GHz.

Accurate measurements of the far from carrier noise are presented for this oscillator that had not previously been obtained. At 1 MHz offset the measured oscillator phase noise is -182dBc/Hz. In addition to the oscillator phase noise measurements, it has been shown in simulation and practice that the microstrip probes can be designed to couple to the resonator for optimum phase noise performance as well as optimum dimensions for a metal enclosure.

The close to carrier phase noise is observed to 'peak' around 10-100 Hz offset that is thought to be caused by temperature variations in the oscillator causing the oscillation frequency to move and give an incorrect phase noise measurement. Preliminary measurements have shown that temperature stabilisation of the enclosure can improve on the oscillator phase noise response but further measurements should be carried out to determine that temperature variations are the exact cause of this peak in the phase noise. The resonators were unfortunately damaged that could result in small microscopic cracks forming that would also affect the temperature stability of the resonator. Further resonators should be obtained and used in the oscillator to determine if that is the cause of the unexpected increase in close to carrier phase noise. It is hoped that with these suggestions, further work can demonstrate an oscillator phase noise measurement that closely matches the close to carrier phase noise theory with fewer spurious peaks in the spectrum.

Further investigating into the large metal enclosure affecting the phase noise spectrum should be undertaken and it is suggested that the PCBs are electrically isolated from it to improve temperature stability. The enclosure could be acting as a large heat sink causing temperature changes in the oscillator resulting in the resonant frequency changing. A metal enclosure is necessary to prevent outside sources interfering and modulating onto the phase noise spectrum but should be investigated to determine its affect on the oscillator frequency.

7.2 16 GHz DBR oscillator discussion and suggested further work

A high Q_0 distributed Bragg resonator has been built with extensive research into the coupling mechanisms presented. An ultra low phase noise oscillator has been built using this resonator including parallel amplifiers used to increase the power available to the resonator input and to suppress flicker noise introduced.

The major issue with the 16 GHz oscillator is the losses in the oscillator loop that have meant that multiple series amplifiers are required to increase the open loop gain such that the oscillation can be sustained. The 2.92mm and SMA connectors used in the oscillator component have been shown to introduce ripple and loss as well as the smaller than desired resonator coupling. It is suggested that future work on this oscillator combines all PCBs onto 1 large board to reduce the number of separate PCBs and therefore reduce the losses introduced by their connections.

Two amplifiers have been successfully used in the 1.5 GHz DRO and are separated by a 3dB coupler to reduce the amount of saturation the second amplifier exhibits which would also decrease the flicker noise and thermal noise introduced into the oscillator loop. This approach could also be investigated as it appears that the current oscillator phase noise measurements are degraded due to the high level of saturation in the amplifier placed at the resonator input.

The electronic tunable phase shifter should be developed to reduce the insertion loss it introduces at 16 GHz, it is preferable to use and electronic tuning device in the oscillator because the oscillator frequency can be controlled more precisely and done so remotely.

Finally, further investigations into the waveguide coupling to the resonator should be undertaken to determine why the simulated resonator does not tie in with the measurements. If this coupling mechanism proves to be successful then the resonator losses can be reduced. This will also reduce the level of saturation the sustaining amplifier enters and the degradation of the oscillator phase noise.

7.3 100 MHz Feedforward amplifier oscillator

This research has demonstrated how a feedforward amplifier can be incorporated into an ultra low phase noise oscillator without the need of external power limiting circuits that stop the main amplifier entering saturation. It has been shown that the error and main loop phase shifts, the attenuation

between the loops and the gain of the error amplifier can be adjusted to keep the level of flicker noise suppression observed by the non saturating amplifier in the saturation regime and can therefore be used in an oscillator where the amplifier will naturally enter saturation.

It has been demonstrated manually that these components can be adjusted to suppress noise in the oscillator by a least 20dB however, noise was introduced from an external source to demonstrate this. This is an improvement of 6dB compared to the system previously developed by this research group that uses PIN diodes to limit the saturation of the main amplifier [2]. The actual flicker noise suppression was not observed as the amplifiers used in the feedforward amplifier were very low noise devices and had low flicker noise corners inside the 3dB bandwidth of the resonator and therefore did not appear in the oscillator phase noise spectrum.

An amplifier with greater flicker noise corners could be used to demonstrate the effect more clearly. The next stage of this research should focus on automating the tuning of the feedforward amplifier whilst the oscillator is operating. This could be done continuously and would keep suppressing the flicker noise introduced by the main amplifier if the oscillator frequency varies over time. This would require multiple measurement points placed at key points in the loop which would introduce some loss that must be accounted for. The gain of both amplifiers must be measured as well as the power levels and phase shift at the input to the third coupler. The error loop phase shifter control will require a phase noise measurement to be made to adjust its phase shift as the ideal feedforward amplifier cancels the carrier signal in the error loop. Therefore, the carrier signal cannot be used as a reference to measure the phase difference at the input to the fourth coupler.

7.4 5 MHz Feedforward amplifier oscillator

The development of a 5 MHz crystal oscillator has been presented achieving a phase noise measurement of -132dBc/Hz at 1 Hz offset. Furthermore an electronically tunable phase shifter has been introduced allowing greater control over the oscillator than in previous iterations.

This is an improvement of 14dB when compared to the previous iteration which demonstrated a phase noise of -118dBc/Hz at 1Hz offset. The 5MHz crystal oscillator also improves on the close to carrier measurement of the 10MHz oven controlled crystal oscillator [3] developed by this research

group by 4dB after frequency scaling.

Furthermore, the 5MHz presented here offers a 2dB improvement in phase noise at 1Hz offset from the carrier compared to the scaled oscillator phase noise of 3.9MHz crystal oscillator presented in [101] and 23dB improvement at 1Hz offset when compared to the 20MHz crystal oscillator measurement presented in [102] if the carrier frequency is scaled to 5MHz.

It is suggested that BVA crystals should replace the current crystals in the oscillator with the aim of improving on the oscillator phase noise. An Allan deviation measurement of the oscillator should be made to determine the long term frequency stability of the oscillator. In addition, a double oven that encapsulates the resonator should be built to heat the crystal to an optimum temperature for minimum phase noise. This has been achieved in the 10 MHz crystal oscillator developed by this group [3, 36] and has shown an improvement in the Allan deviation of the oscillator when compared to the deviation of the oscillator without a double oven.

Appendices

Appendix A

Arduino source code to control ZX76-31R75PP-S+ digital step attenuator

```
#include <Arduino.h>
#include "HT16K33.h"

HT16K33 seg(0x70);

uint32_t start, stop;


int ledPin[7] = {7,8,9,10,11,12,13};
int buttonPin[2] = {2,3};
volatile int buttonState = LOW;
volatile int buttonStateDown = LOW;
int counter = 0;
double atten = 0.000;
```

```
double minStep = 0.250;
double offset = 1.563;
double val = 0.0;

void setup()
{
  seg.begin();
  seg.displayClear();
  Wire.setClock(100000);
  seg.brightness(5);
  seg.displayOn();
  Serial.begin(9600);
  for (int i =0;i<7;i++)
  {
    pinMode(ledPin[i], OUTPUT);
    }

  for (int j =0;j<2;j++)
  {
    pinMode(buttonPin[j], INPUT);
    }

  attachInterrupt(digitalPinToInterrupt(3), pin_ISR_3, RISING);
  attachInterrupt(digitalPinToInterrupt(2), pin_ISR_2, RISING);

}

void loop()
{
```

```
  displayNum(counter);
}

void pin_ISR_2(){
  static unsigned long up_last_interrupt_time = 0;
  unsigned long up_interrupt_time = millis();
  buttonState = digitalRead(2);
  if(counter<127 && buttonState==HIGH && up_interrupt_time -
                                    up_last_interrupt_time > 500){

      counter++;
  }
}
void pin_ISR_3(){
  static unsigned long down_last_interrupt_time = 0;
  unsigned long down_interrupt_time = millis();
  buttonStateDown = digitalRead(3);
  if(counter>0 && buttonStateDown==HIGH && down_interrupt_time -
                                  down_last_interrupt_time > 500){

      millis();
      counter--;
  }
}


void displayBinary(byte count)
{
  for (int i =0;i<7;i++)
```

```
  {
    if (bitRead(count, i)==1)
    {
      digitalWrite(ledPin[i], HIGH);
    }
    else
    {
      digitalWrite(ledPin[i], LOW);
    }
  }

}
void displayNum(int number){
  displayBinary(number);
  Serial.println(number) ;
  Serial.println(number, BIN) ;
  atten = (offset+(number*minStep));

  Serial.println(atten, 2) ;
  Serial.println() ;



  seg.displayFloat(atten);
  delay(1000);
  seg.displayInt(number);
  delay(1000);
}
```

Appendix B

Ultra low phase noise 16GHz oscillator using a distributed Bragg resonator conference paper and poster

The following documents were presented at the European Frequency and Time Forum (EFTF), Neuchatel, 2024. This conference paper was submitted after the submission of this thesis and includes additional measurements of oscillator phase noise that improve on those presented here. The oscillator was built using two Analog devices HMC3653 amplifiers. The measured phase noise at 10kHz offset from the carrier is improved by approximately 4dB when using the lower power HMC3653 devices when compared to using 2 Marki APM6849SM devices in series with the amplifier consisting of 4 Marki APM6849SM devices in parallel.

The author won the student poster competition for the Oscillators and Noise category.

Ultra Low Phase Noise 16GHz Oscillator Using a Distributed Bragg Resonator

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***Abstract*—This paper presents the design of a 16GHz oscillator using a high Q distributed Bragg resonator (DBR) with an aperiodic arrangement of high purity, low-loss alumina plates (ϵ_r = 9.75, loss tangent of $\approx 1 \times 10^{-5}$ to 2×10^{-5}). The resonator demonstrates an unloaded Q up to 160,000 & the plates are held in place using Spira-Shield O-Ring gaskets to maintain mechanical stability. Preliminary phase noise measurements of -77dBc/Hz at 100Hz offset & -135dBc/Hz at 10kHz offset are presented.**

***Index Terms*—Distributed Bragg resonator, 16GHz, High unloaded Q, Spira-Shield, Ultra low phase noise**

I. Introduction

The oscillator used in time sensitive electronic equipment sets the ultimate phase noise performance of the system. It is therefore essential to develop ultra-low phase noise oscillators to ensure that phase noise, jitter & Allan deviation are minimised. The phase noise is proportional to $1/Q^2$ [1], [2].

Microwave cavities are often used as the resonant element in oscillators as they are capable of handling high powers but the Q is limited by the surface resistivity of the metal walls. Higher unloaded Qs can be achieved by incorporating low loss dielectric plates into the cavity [3]–[9] that confine the majority of the field energy to the centre section and away from the lossy end walls.

A periodic Bragg resonator was presented by Maggiore *et al* stating an unloaded Q of 531×10^3 [3] at 18.99GHz using sapphire plates.

Flory *et al* [4], [5] have demonstrated periodic sapphire resonators exhibiting unloaded Qs of 650,000 and 450,000 at 9 and 13.2 GHz respectively consisting of interpenetrating concentric sapphire rings and plates inside a metal cavity to reduce the losses in the metal walls. For maximum power reflection in the air/dielectric interface, the thickness of the plates and air sections were a quarter of the wavelength of the guide wave.

It was shown in simulation by Breeze *et al* [6] that distributing more of the field energy in the air gaps than in the dielectric plates by using an aperiodic arrangement, increases the Q factor compared to a periodic DBR. A 30GHz sapphire resonator was later developed by that research group [7] demonstrated an unloaded Q of 600,000.

The authors wish to thank Agilent Technologies Inc (Santa Clara, California) and the UK Engineering and Physical Sciences Research Council (EPSRC) for their funding and support

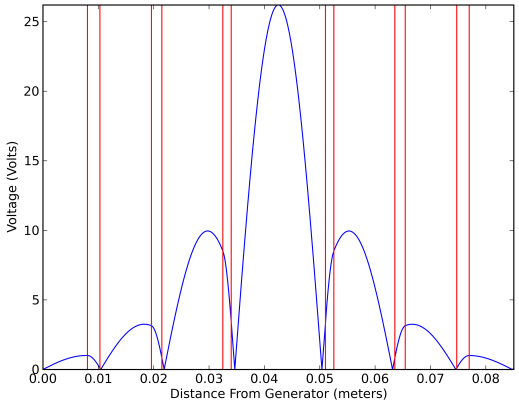

Fig. 1. Simulation voltage standing wave inside a 10GHz DBR developed by this research group [8], the peaks occur in the lower loss air sections, rather than the more lossy dielectric sections. The vertical lines represent the dielectric plates

A 10GHz aperiodic DBR was built at York by Bale and Everard [8], demonstrating a Q_0 of 197,000 where it was also shown in simulation that the unloaded Q of the resonator saturates when 8 plates were used. The simulated voltage standing wave pattern of the aperiodic resonator developed by this research group is shown in figure 1. This shows that the voltage peaks occur in the low loss air sections rather than inside the more lossy dielectric sections (vertical lines), as is the case for a periodic structure.

A tunable 10GHz resonator has also been developed demonstrating insertion loss variance of -2.84 to -12.03dB with unloaded Q varying from 43,800 to 123,000 within a 130MHz tuning range [9] by this research group.

In this paper, the designs and phase noise measurements of a high power and a low power feedback oscillator using a high Q aperiodic DBR operating at 16GHz are presented.

II. Ultra Low Oscillator Phase Noise Theory

It is necessary to develop an equivalent circuit model from which a phase noise equation can be derived. Such a model has been developed by Everard, [1], [2], shown in figure 2, where an equation is derived and expanded to include the flicker

$$L(f) = 10NLog\left(\underbrace{\frac{F_2kT}{C_0 2P_{AVO}}}_{A} + \underbrace{\left(1+\frac{f_C}{\Delta f}\right)}_{B}\left(\frac{F_1kT}{2P_{AVO}}\underbrace{\left(\frac{1}{\left[1-\frac{Q_L}{Q_0}\right]^2}\right)}_{C} + \underbrace{\frac{F_1kT}{8(Q_0)^2\left(\frac{Q_L}{Q_0}\right)^2\left(1-\frac{Q_L}{Q_0}\right)^2 P_{AVO}}}_{D}\left(\frac{f_0}{\Delta f}\right)^2\right)\right) \quad (1)$$

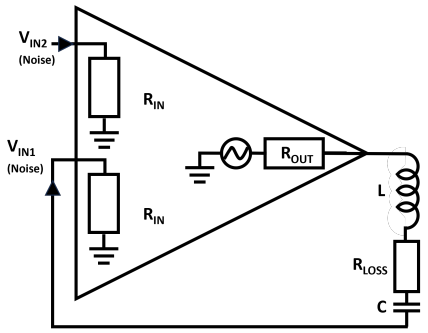

Fig. 2. Equivalent circuit model of the feedback oscillator where the resonant element is modelled as an LCR network and the feedback path is modelled as a two input amplifier [1]

noise corner of the feedback amplifier, the noise outside the resonator 3dB bandwidth and noise from a buffer amplifier. The complete phase noise equation is given in equation 1 [2].

This equation can be split into four sections, where section A is the noise introduced by the buffer amplifier. F_2 is the noise figure of the buffer, C_0 is the coupling ratio between the power available at the resonator input, P_{AVO}, and the power at the input of the buffer. Part B is the flicker noise spectral density of the feedback amplifier where F_C is the flicker noise corner of the device. The noise floor outside the resonator 3dB bandwidth is calculated using part C, caused by the closed loop amplifier gain. Finally, the oscillator phase noise within the 3dB bandwidth is given in part D which is the specific phase noise equation where $R_{OUT} = R_{IN}$ and the power is defined as the power available at the input of the resonator, P_{AVO}.

Part D is minimum when $Q_L/Q_0 = 1/2$, and therefore the insertion loss of the resonator is 6dB. Here the maximum power is dissipated by the resonator [10]. The loop losses must be overcome by the feedback amplifier which should have a low noise figure (F_1) and low flicker noise corner (f_c) such that equation 1 is kept to a minimum. It is also necessary that this amplifier produce high output power and be placed as close to the resonator input as possible so that P_{AVO} is high which also minimises equation 1.

If the open loop phase shift deviates from an integer multiple of 360°, then the oscillator no longer oscillates at the resonant frequency of the resonator. The effective Q of the resonator reduces at a rate proportional to the phase slope of the resonator causing a degradation to the phase noise in the thermal and flicker regions. It is demonstrated experimentally by Cheng and Everard in [11] that the phase error causes a degradation to the phase noise by a factor of $cos^4\theta$, where θ is the open loop phase error.

III. Oscillator Design

A. High Q Distributed Bragg Resonator

The resonant element is a 16GHz Bragg resonator designed to operate in the high Q TE_{011} mode. High purity, low loss alumina plates (ϵ_r = 9.75, loss tangent of $\approx 1 \times 10^{-5}$ to 2×10^{-5}) are distributed within a microwave cavity. The section heights increase towards $\lambda/4$ at the far end of the cavity as demonstrated in figure 1. More energy is reflected away from the lossy end walls resulting in a higher unloaded Q than the classic air filled cavity. The size of each section asymptotically approaches $\lambda_{Guide}/4$ and was designed using the same process adopted in [8], by considering each air/dielectric section as a separate waveguide section. The separate sections were simulated together and optimised using a genetic algorithm to maximise the Q.

Coupling to the resonator is achieved using small coaxial loop probes positioned close to the side wall of the central section orientated in the same direction as the plates. RG405 coax is used for the probes and the diameter of the area enclose by the centre conductor is 0.5mm. A maximum measured unloaded Q of 160,000 was observed although there was large insertion loss of approximately 30dB. The unloaded Q of the resonator used in the final oscillator was 115,000 with an insertion loss of 9.14dB.

B. Amplifiers

Three amplifiers have been used in the oscillators, Analog Devices HMC3653, Marki APM6849SM and an amplifier consisting of 4 APM6849 devices connected in parallel using Rat Race couplers. The parallel amplifier was used to suppress the flicker noise introduced by a single device and to increase the output power. It has been shown by Boudot and Rubiola [12] that a flicker noise reduction of $3log2(m)$ dB is possible by using m number of parallel amplifiers. The measured gain, output power in 1 dB compression, $P_{Out1dBm}$, and noise figure of these amplifiers are shown in table I.

Amplifier	Gain /dB	$P_{Out1dBm}$ /dBm	NF /dB
HMC3653LP3BE	11.637	13.3	6.14
APM6849SM	9.835	19.6	4.89
Parallel APM6849SM	7.41	21.5	6.47

TABLE I
MEASURED AMPLIFIER PARAMETERS AT 16GHZ FROM THREE AMPLIFIERS CONSIDERED SUITABLE FOR USE IN A 16GHZ OSCILLATOR

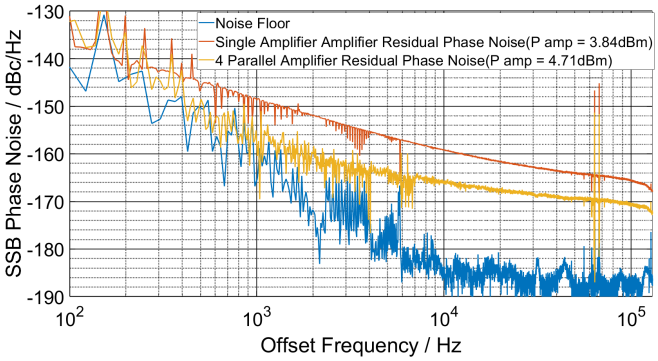

Fig. 3. Measured residual phase noise of the single amplifier, parallel amplifier and noise floor of the measurement system with a resolution bandwidth of 7.63Hz, 7.5dBm input power to the mixer after 10,000 correlations

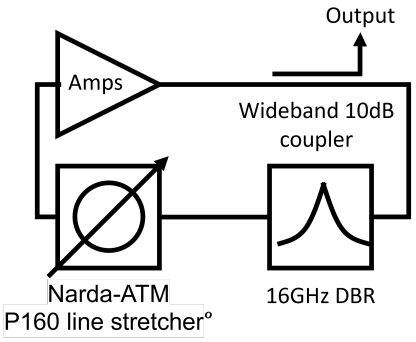

Fig. 4. Generic 16GHz DBR oscillator block diagram, the 'Amps' component represents the different amplifier combinations used in the measurements

The measured gain of the parallel amplifier has decreased by 2.43dB when compared with a single APM6849SM device, and the noise figure has increased by 1.51dB whilst the output power in 1dB compression has only increased by 2dB and not the expected 6dB. It is clear that losses have been introduced by the Rat Race structure in the parallel amplifier.

A residual phase noise measurement of the HMC3653 amplifier was made using an FSWP50 indicating a flicker noise corner of 30kHz. Residual phase noise measurements of the APM6849SM single device and the parallel configuration were made using the cross correlation system developed at York by Bale *et al* [13] to demonstrate the flicker noise suppression. The noise floor of the FSWP was too high to measure the single and parallel APM6849 amplifiers and so Bale's system was used as it has a lower noise floor. 10,000 correlations were carried out and the input power to the mixers, P_{IN}, was kept constant at 7.5dBm.

The measured residual phase noise of both amplifiers is plotted in figure 3 from which the estimated flicker noise corner of the amplifier reduces from 70kHz to 20kHz. The far from carrier noise is estimated to be -166dBc/Hz for the single amplifier and -170dBc/Hz for the parallel amplifiers. This system is only suitable to measure up to 100kHz offsets so an estimate has been made for the amplifier far from carrier noise. Theory predicts a 6dB reduction in flicker noise for four parallel amplifiers. It is estimated from the plotted results and different operating condition that the flicker noise improvement due to the parallel network is between 5-6dB.

IV. Oscillator Phase Noise Measurement, Conclusions and Further Work

At 16GHz the losses introduced by the interconnecting cables, the passive components and the PCB connectors is large and therefore the open loop gain must be increased to overcome this. The high power oscillator consisted of a series combination of two single APM6849 devices followed by the parallel amplifier. A 6dB attenuator was placed between the two single devices to reduce the saturation of the second stage with the aim of reducing any increase in flicker noise and noise figure. However, the cascaded noise figure of the feedback components was calculated to be 25dB which has had a significant affect on increasing the oscillator phase noise.

To reduce the noise figure, a second oscillator was built using two lower power HMC3653 devices. A 6dB attenuator was placed between these devices. The HMC3653 offers increased gain of 11.7dB at 16GHz, therefore fewer devices were required to overcome the loop losses. The noise figure of the feedback path was calculated to be 14dB. In both oscillators, a Narda-ATM P160 line stretcher was used to adjust the loop phase shift and a 10dB wideband coupler designed in house was used to couple the oscillator output.

Phase noise measurements of both oscillators were made using the Rohde and Schwarz FSWP 50 phase noise measurement system and both oscillators were placed in a shielded enclosure for the measurement. 1000 correlations were made in the smallest offset frequency band (1-10Hz) with a 5% resolution bandwidth. The measurement time was approximately 1 hour.

Using equation 1 and the measured parameters of Q_L, Q_0, P_{1dBm}, F_C and calculated cascaded NF, the theoretical oscillator phase noise can be calculated for both the high power and low power configurations. The estimated F_C has been increased to 30kHz in the high power theory plot as 20kHz gave a phase noise calculation that was too small and was therefore inaccurate to what has been measured. This suggests that the saturation of the parallel amplifier has caused an increase to the flicker noise. The measured and theoretical oscillator phase noise plots are shown in figure 5.

The lower power oscillator matches the theory above 100Hz offsets whereas the higher power oscillator measurement is greater than the theory at offsets less than 1kHz. It is thought that the high noise figure and potential excessive saturation of the amplifiers used in the high power oscillator has introduced additional noise components to the phase noise spectrum.

The higher power oscillator is expected to present lower phase noise than the lower power configuration. However, the number of amplifiers required in the high power oscillator and the 6dB attenuator used to limit amplifier suppression has considerably increased the noise figure and therefore increased

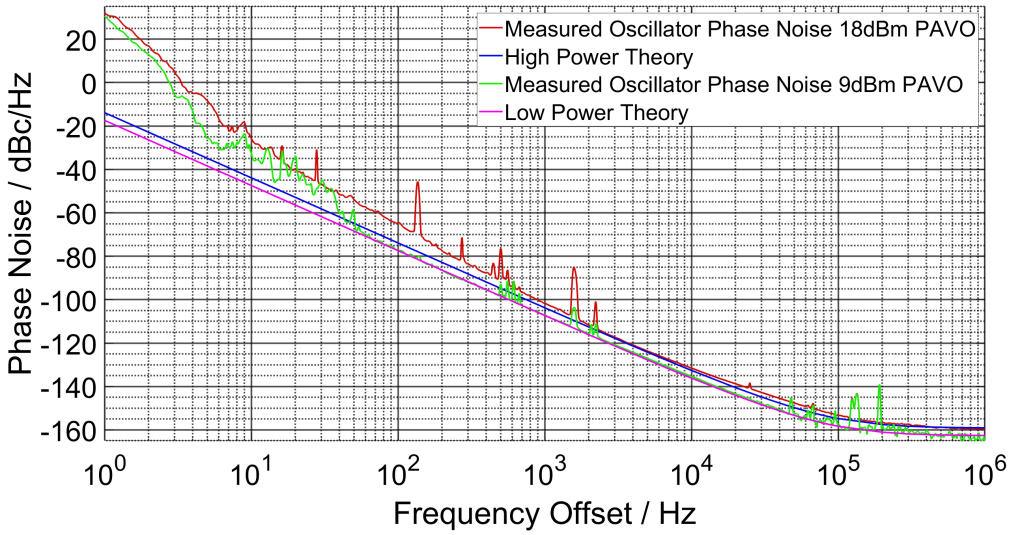

Fig. 5. Theoretical and measured oscillator phase noise plots of the 16GHz DBR oscillator. The theoretical plot is calculated using equation 1 and measured parameters Q_L, Q_0, P_{1dBm}, F_C and NF

the oscillator phase noise such that it is larger than the low power oscillator.

The close to carrier frequency noise increase is possibly due to the oscillation frequency changing during the measurement process as result of thermal effects in the oscillator. The change in oscillator frequency appears as positive phase noise in the measurement at an offset from the initial oscillator frequency. Temperature stabilisation of the resonator should be considered to stop the metal resonator enclosure expanding/contracting and improve the close to carrier phase noise response.

Future iterations of the oscillator should aim to reduce the number of series amplifiers in the feedback loop to reduce the noise figure and saturation of the amplifiers. Further work on resonator coupling to ensure small insertion loss whilst maintaining a high unloaded Q is necessary and alternative methods of coupling should be explored. 20-30dB improvements in phase noise should therefore be possible.

ACKNOWLEDGMENT

The authors wish to thank Agilent Technologies Inc (Santa Clara, California) and the UK Engineering and Physical Sciences Research Council (EPSRC) for their funding and support

REFERENCES

[1] J. Everard, *Fundamentals of RF Circuit Design*, 1st ed. New York, USA: Wiley, 2001.

[2] J. Everard, T. Burtichelov, and K. Ng, "Ultralow Phase Noise 10-MHz Crystal Oscillators," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 66, no. 1, pp. 181–191, Jan 2019.

[3] C. J. Maggiore, A. M. Clogston, G. Spalek, W. C. Sailor, and F. M. Mueller, "Low-loss microwave cavity using layered-dielectric materials," *Applied Physics Letters*, vol. 64, no. 11, pp. 1451–1453, 03 1994.

[4] C. Flory and H. Ko, "Microwave oscillators incorporating high performance distributed bragg reflector microwave resonators," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 45, no. 3, pp. 824–829, 1998.

[5] C. Flory and R. Taber, "High Performance Distributed Bragg Reflector Mircowave Resonator," *IEEE Transactions On Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 44, no. 2, pp. 468–495, 1997.

[6] J. Breeze, J. Krupka, and N. M. Alford, "Enhanced quality factors in aperiodic reflector resonators," *Appl. Phys. Lett*, vol. 91, no. 15, 2007.

[7] J. Breeze, M. Oxborrow, and N. McN Alford, "Better than Bragg: Optimizing the quality factor of resonators with aperiodic dielectric reflectors," *Applied Physics Letters*, vol. 99, no. 11, p. 113515, 09 2011.

[8] S. Bale and J. Everard, "High-Q X-Band Distributed Bragg Resonator Utilizing an Aperiodic Alumina Plate Arrangement," *IEEE Transactions On Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 57, no. 1, pp. 66–73, 2010.

[9] S. J. Bale, P. D. Deshpande, M. Hough, S. J. Porter, and J. K. A. Everard, "High-q tuneable 10-ghz bragg resonator for oscillator applications," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 65, no. 2, pp. 281–291, 2018.

[10] J. Everard, M. Xu, and S. Bale, "Simplified phase noise model for negative-resistance oscillators and a comparison with feedback oscillator models," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 59, no. 3, pp. 382–390, 2012.

[11] K. K. M. Cheng and J. K. A. Everard, "Noise performance degradation in feedback oscillators with nonzero phase error," *Microw. Opt. Technol. Lett.*, vol. 4, no. 2, pp. 64–66, Jan. 1991.

[12] R. Boudot and E. Rubiola, "Phase noise in RF and microwave amplifiers," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 59, no. 12, pp. 2613–2624, Dec. 2012.

[13] S. J. Bale, D. Adamson, B. Wakley, and J. Everard, "Cross correlation residual phase noise measurements using two hp3048a systems and a pc based dual channel fft spectrum analyser," in *EFTF-2010 24th European Frequency and Time Forum*, 2010, pp. 1–8.

Ultra Low Phase Noise 16GHz Oscillator Using a Distributed Bragg Resonator

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Abstract:- This paper presents the design of a 16GHz oscillator using a high Q distributed Bragg resonator with an aperiodic arrangement of high purity alumina plates demonstrating an unloaded Q up to 160,000. Preliminary phase noise measurements demonstrate -75dBc/Hz at 100Hz offset & -134dBc/Hz at 10kHz offset.

Introduction:-

- Phase noise is inversely proportional to Q_0^2 & P_{AVO} [1]
- This work builds on the work published on Distributed Bragg Resonators by this research group[2,3] & by Breeze *et al*[4]
- High resonator power of **>18dBm** is achieved using parallel amplifiers with high Q > 100,000 observed

16 GHz Bragg Cavity:-

- High purity Alumina plates are placed in an **aperiodic** arrangement within a microwave cavity to contain the field **away from the lossy end walls**
- Mechanical stability and reduced EM leakage are achieved using a **Spira Shield** gasket
- Unloaded Qs of **160,000** have been demonstrated with this resonator with an insertion loss of -9.14dB

- Air sections asymptotically approaching λ/4
- Central air section λ/2
- Dielectric sections asymptotically approaching λ/4
- H Field strongest in the middle of the central section

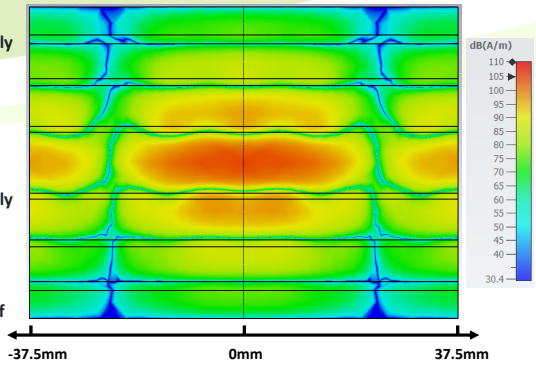


Fig 1. Distributed Bragg Resonator Magnetic Field pattern of TE_{011}, modelled in CST.

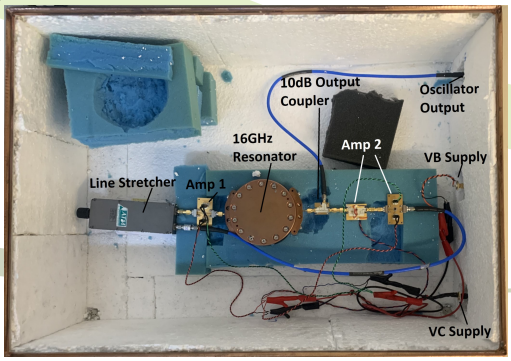


Fig 3. Complete oscillator with two single Marki devices in series with a parallel combination of 4 devices.

Oscillator Design:-

- **Low noise** Marki APM6849SM devices were used for 1st and 2nd gain stage
- 3rd gain stage consisted of **4 Marki APM6849SM** devices connected in **parallel**
- Parallel amplifiers **reduce the flicker noise corner** from 90kHz to 20kHz
- Furthermore, parallel arrangement **increases** the measured **output power** in 1 dB compression from **19.4dBm to 22.5dBm** with 6V bias
- The oscillator is housed in a **shielded enclosure**

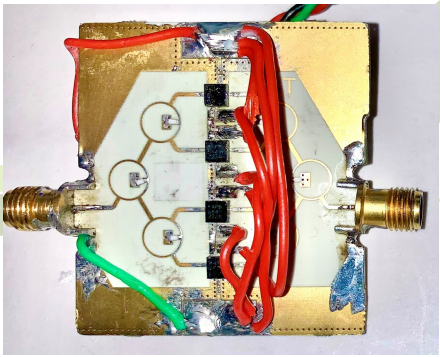
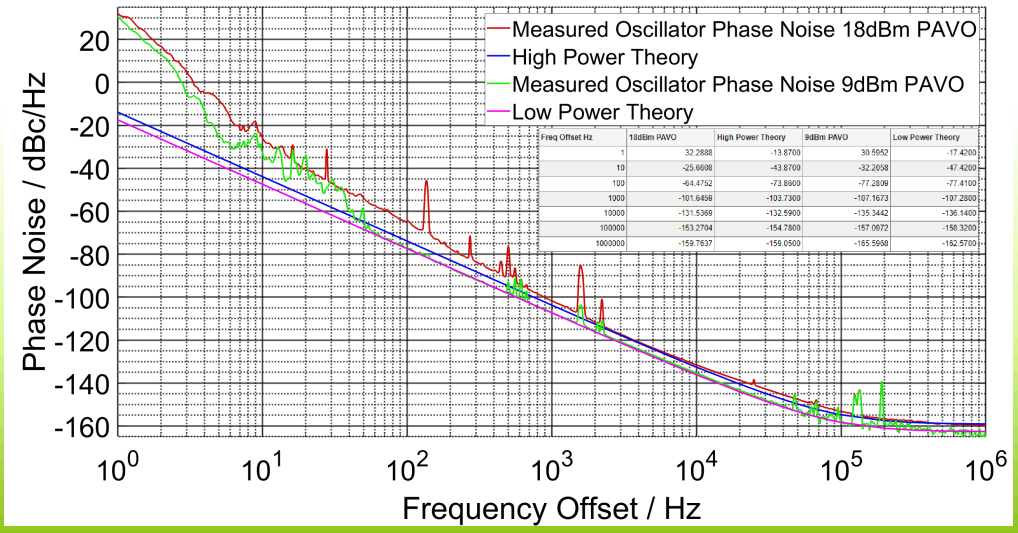


Fig 2. 4 devices in parallel to increase output power and reduce flicker noise

Measurements:-

- R&S **FSWP 50** used for Phase noise measurements for both oscillator configurations
- Theory calculated using P_{AVO} = **18.1 dBm**, F_C = **30kHz**, **NF** = **25dB** for high power oscillator
- Theory calculated using P_{AVO} = **9dBm**, F_C = **30kHz**, **NF** = **14 dB** for low power oscillator
- Q_L and Q_0 are **74600** and **115000** for both
- The high close to carrier noise is likely caused by variation in the oscillation frequency
- Lower power oscillator has lower phase noise due to smaller noise figure
- Flicker noise suppression is not as high due to saturated single devices in series with parallel amplifier



Freq Offset Hz	18dBm PAVO	High Power Theory	9dBm PAVO	Low Power Theory
1	32.2888	-13.8700	30.5652	-17.4200
10	-25.6608	-43.8700	-32.2058	-47.4200
100	-64.4752	-73.8900	-77.2809	-77.4100
1000	-101.6459	-103.7300	-107.1673	-107.2800
10000	-131.5369	-132.5900	-135.3442	-136.1400
100000	-153.2704	-154.7800	-157.0972	-158.3200
1000000	-159.7637	-159.0500	-165.5958	-162.5700

Fig 4. Oscillator phase noise measurement and calculated oscillator phase noise

We wish to thank Agilent Technologies Inc (Santa Clara, California) and the UK Engineering & Physical Sciences Research Council (EPSRC) for their funding and support

References:
1 Everard, Jeremy. *Fundamentals of RF Circuit Design : With Low Noise Oscillators*, John Wiley & Sons, Incorporated, 2001
2 S. Bale & J. Everard, "High-Q X-band distributed Bragg resonator utilizing an aperiodic alumina plate arrangement," *IEEE Transactions on Ultrasonics, Ferroelectrics, & Frequency Control*, vol. 57, no. 1, pp. 66-73, Jan. 2010
3 S. J. Bale, P. D. Deshpande, M. Hough, S. J. Porter & J. K. A. Everard, "High-Q Tuneable 10-GHz Bragg Resonator for Oscillator Applications," *IEEE Transactions on Ultrasonics, Ferroelectrics, & Frequency Control*, vol. 65, no. 2, pp. 281-291, Feb. 2018
4 Jonathan Breeze, Jerzy Krupka, Neil McN Alford; Enhanced quality factors in aperiodic reflector resonators. *Appl. Phys. Lett.* 8 October 2007; 91 (15)

References

[1] J. Everard, *Fundamentals of RF Circuit Design*, 1st ed. New York, USA: Wiley, 2001, p. 163.

[2] J. K. Everard and C. D. Broomfield, "Reduced transposed flicker noise in microwave oscillators using gaas-based feedforward amplifiers," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 54, no. 6, pp. 1108–1117, 2007.

[3] J. Everard, T. Burtichelov, and K. Ng, "Ultralow Phase Noise 10-MHz Crystal Oscillators," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 66, no. 1, pp. 181–191, Jan 2019.

[4] T. Nankervis, "Ultra low noise crystal oscillators," Ph.D. dissertation, Department of Electronic Engineering, University of York, Department of Electronic Engineering, University of York, York, UK, 2017.

[5] A. Hati, D. Howe, F. Walls, and D. Walker, "Noise figure vs. pm noise measurements: a study at microwave frequencies," in *IEEE International Frequency Control Symposium and PDA Exhibition Jointly with the 17th European Frequency and Time Forum, 2003. Proceedings of the 2003*, 2003, pp. 516–520.

[6] F. E. Terman, *Radio Engineers' Handbook*, 1st ed. New York and London: McGraw-Hill Book Company, 1943, p. 476.

[7] H. Nyquist, "Thermal agitation of electric charge in conductors," *Phys. Rev.*, vol. 32, pp. 110–113, Jul 1928. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRev.32.110

[8] P. Horowitz and W. Hill, *The art of electronics*, 1st ed. Cambridge: Cambridge University Press, 1980, pp. 288–289.

[9] H. Rohdin, C.-Y. Su, and C. Stolte, "A study of the relation between device low-frequency noise and oscillator phase noise for gaas mesfets," in *1984 IEEE MTT-S International Microwave Symposium Digest*, 1984, pp. 267–269.

[10] H. Siweris and B. Schiek, "Analysis of noise upconversion in microwave fet oscillators," *IEEE Transactions on Microwave Theory and Techniques*, vol. 33, no. 3, pp. 233–242, 1985.

[11] P. Dallas and J. Everard, "Characterization of flicker noise in gaas mesfet's for oscillator applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 2, pp. 245–257, 2000.

[12] A. Riddle and R. Trew, "A new method of reducing phase noise in gaas fet oscillators," in *1984 IEEE MTT-S International Microwave Symposium Digest*, 1984, pp. 274–276.

[13] A. van der Ziel, "Unified presentation of 1/f noise in electron devices: fundamental 1/f noise sources," *Proceedings of the IEEE*, vol. 76, no. 3, pp. 233–258, 1988.

[14] F. Walls, E. Ferre-Pikal, and S. Jefferts, "Origin of 1/f pm and am noise in bipolar junction transistor amplifiers," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 44, no. 2, pp. 326–334, 1997.

[15] D. Leeson, "A simple model of feedback oscillator noise spectrum," *Proceedings of the IEEE*, vol. 54, no. 2, pp. 329–330, 1966.

[16] T. Parker, "Current developments in saw oscillator stability," in *31st Annual Symposium on Frequency Control*, 1977, pp. 359–364.

[17] J. Everard, *Fundamentals of RF Circuit Design*, 1st ed. New York, USA: Wiley, 2001, p. 181.

[18] ——, *Fundamentals of RF Circuit Design*, 1st ed. New York, USA: Wiley, 2001, p. 163.

[19] J. Everard, M. Xu, and S. Bale, "Simplified phase noise model for negative-resistance oscillators and a comparison with feedback oscillator models," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 59, no. 3, pp. 382–390, 2012.

[20] K. K. M. Cheng and J. K. A. Everard, "Noise performance degradation in feedback oscillators with nonzero phase error," *Microw. Opt. Technol. Lett.*, vol. 4, no. 2, pp. 64–66, Jan. 1991.

[21] G. Cibiel, M. Regis, E. Tournier, and O. Llopis, "Am noise impact on low level phase noise measurements," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 49, no. 6, pp. 784–788, 2002.

[22] E. Rubiola and F. Vernotte, "The cross-spectrum experimental method," *arXiv: Instrumentation and Detectors*, 2010.

[23] W. Walls, "Cross-correlation phase noise measurements," in *Proceedings of the 1992 IEEE Frequency Control Symposium*, 1992, pp. 257–261.

[24] S. J. Bale, "Ultra high q resonators and very low phase noise measurement systems for low noise oscillators," Ph.D. dissertation, Department of Electronic Engineering, University of York, Department of Electronic Engineering, University of York, York, UK, 2012.

[25] T. Burtichelov and J. Everard, "Latest results in the development of an ultra-low phase noise rb cpt vapour cell atomic clock," in *2017 Joint Conference of the European Frequency and Time Forum and IEEE International Frequency Control Symposium (EFTF/IFCS)*, 2017, pp. 837–841.

[26] J. Everard and K. Theodoropoulos, "Ultra-low phase noise ceramic based dielectric resonator oscillators," in *2006 IEEE International Frequency Control Symposium and Exposition*, 2006, pp. 869–874.

[27] *Dielectric Resonator*, Exxelia Temex, 2015, exxelia Temex Dielectric Resonator Datasheet. [Online]. Available: https://exxelia.com/uploads/PDF/e7000-v1.pdf

[28] *DIELECTRIC RESONATORS*, EXXELIA TEMEX, 2015, xXELIA TEMEX reserves the right to modify herein specifications and information at any time when necessary to provide optimum performance and cost. [Online]. Available: https://exxelia.com/uploads/PDF/e7000-v1.pdf

[29] D. M. Pozar, *Microwave Engineering*, 3rd ed. New York, USA: Wiley, 2004, pp. 313–328.

[30] D. Kajfez and P. Guillon, *Dielectric Resonators*, 1st ed. 16 Sussex Street London SW1V 4RW UK: Artech House Inc, 1986, pp. 129–132.

[31] C. A. Balanis, *Advanced Engineering Electromagnetics*, 1st ed. The Atrium Southern Gate, Chichester West Sussex PO19 8SQ England: John Wiley & Sons, Inc., 1989, pp. 506–525.

[32] M. Sallin, L. Zhou, C. Broomfield, and J. Everard, "Broad tuning ultra low noise dros at 10 ghz utilising ceramic based resonators," in *IEEE International Frequency Control Symposium and PDA Exhibition Jointly with the 17th European Frequency and Time Forum, 2003. Proceedings of the 2003*, 2003, pp. 411–416.

[33] P. D. Deshpande and J. Everard, "Compact low phase noise 3.8 ghz oscillator," in *2014 European Frequency and Time Forum (EFTF)*, 2014, pp. 203–207.

[34] M. Yazdani, D. Bates, and L. Murphy, "The design and fabrication of a compact low phase noise dielectric cavity resonator oscillator," in *2014 44th European Microwave Conference*, 2014, pp. 719–722.

[35] G. Wibisono and T. Firmansyah, "Design of dielectric resonators oscillator for mobile wimax at 2.3 ghz with additional coupling $\lambda/4$," in *TENCON 2011 - 2011 IEEE Region 10 Conference*, 2011, pp. 489–493.

[36] T. Burtichelov, "Ultra-low phase noise atomic clock using coherent population trapping (cpt) in rubidium," Ph.D. dissertation, Department of Electronic Engineering, University of York, Department of Electronic Engineering, University of York, York, UK, 2017.

[37] R. Boroditsky and J. Gomez, "Ultra low phase noise 1 ghz ocxo," in *2007 IEEE International Frequency Control Symposium Joint with the 21st European Frequency and Time Forum*, 2007, pp. 250–253.

[38] *Ultra Low Noise 2.856GHz S-Band DRO*, Ingenieurbüro Gronefeldy, May 2017, revised Rept. 2020. [Online]. Available: https://gronefeld.de/wp-content/uploads/2018/03/GDRO2856_Datasheet.pdf

[39] *Dielectric Resonant Oscillator 2-3 GHz, +13dBm. Output Power, 12 Volts*, RADITEK INC, July 2018, rDRO-3-2-13d-12V-s12 datasheet. [Online]. Available: http://raditek.com/IC-OSCILLATORS/DRO/RDRO-2-3-13d-12V-s12.pdf

[40] *Isola I-Tera MT40 Very Low-Loss Laminate and Prepreg*, Isola Group, Jan 2023, isola I-Tera MT40 Datasheet. [Online]. Available: https://www.isola-group.com/wp-content/uploads/data-sheets/i-tera-mt40.pdf?t=433366612

[41] E. Rubiola and R. Boudot, "Phase noise in rf and microwave amplifiers," in *2010 IEEE International Frequency Control Symposium*, 2010, pp. 109–111.

[42] *Microwave Devices RJ RELAYS Product Catalog*, Panasonic, 2022, aSCTB105E 202204. [Online]. Available: https://industry.panasonic.com/global/en/downloads/?file_cd=301612&tab=catalog&series_cd=1217

[43] T. Edwards, *Foundations for Microstrip Engineering*, 2nd ed. Baffins Lane, Chichester West Sussex PO19 1UD England: John Wiley & Sons, Inc., 1992, pp. 138–141.

[44] *Silicon Variable Capacitance Diodes*, Infineon Technologies AG, Nov 2009, edition 2009-11-16. [Online]. Available: https://www.mouser.co.uk/datasheet/2/196/bb831series-89147.pdf

[45] S. Cohn, "A class of broadband three-port tem-mode hybrids," *IEEE Transactions on Microwave Theory and Techniques*, vol. 16, no. 2, pp. 110–116, 1968.

[46] *Bushing Style EMI Filter*, Tusonix, 2015, rev. 0. [Online]. Available: https://www.farnell.com/datasheets/1844945.pdf

[47] Rohde and Schwarz, "Rohde and schwarz ®fswp phase noise analyzer and vco tester specifications," 2024, accessed on 8/10/24. [Online]. Available: https://scdn.rohde-schwarz.com/ur/pws/dl_downloads/pdm/cl_brochures_and_datasheets/specifications/3683_7719_22/FSWP_specs_en_3683-7719-22_v0600.pdf

[48] *Ultra Wide Band Coaxial Isolator 1.2GHz-1.7GHz*, RF Lambda, 2023, rev 3. [Online]. Available: https://www.rflambda.com/pdf/isolator/RFLI316G12G17.pdf

[49] *ZEM-4300MH Frequency Mixer*, MiniCircuits, 2023, rev C. [Online]. Available: https://www.minicircuits.com/pdfs/ZEM-4300+.pdf

[50] *Low Pass Filter SLP-10.7+*, MiniCircuits, 2023, rev C. [Online]. Available: https://www.minicircuits.com/pdfs/SLP-10.7+.pdf

[51] N. R. Nand, J. G. Hartnett, and C. Lu, "State-of-the-art cryocooled sapphire oscillators," in *2012 IEEE International Frequency Control Symposium Proceedings*, 2012, pp. 1–2.

[52] M. Tobar, J. Hartnett, E. Ivanov, D. Cros, P. Blondy, and P. Guillon, "Cryogenically cooled sapphire-rutile dielectric resonators for ultrahigh-frequency stable oscillators for terrestrial and space applications [atomic frequency standards]," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 7, pp. 1265–1269, 2000.

[53] C. Flory and H. Ko, "Microwave oscillators incorporating high performance distributed bragg reflector microwave resonators," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 45, no. 3, pp. 824–829, 1998.

[54] C. Flory and R. Taber, "High Performance Distributed Bragg Reflector Mircowave Resonator," *IEEE Transactions On Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 44, no. 2, pp. 468–495, 1997.

[55] S. Bale and J. Everard, "High-Q X-Band Distributed Bragg Resonator Utilizing an Aperiodic Alumina Plate Arrangement," *IEEE Transactions On Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 57, no. 1, pp. 66–73, 2010.

[56] S. J. Bale, P. D. Deshpande, M. Hough, S. J. Porter, and J. K. A. Everard, "High-q tuneable 10-ghz bragg resonator for oscillator applications," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 65, no. 2, pp. 281–291, 2018.

[57] D. M. Pozar, *Microwave Engineering*, 3rd ed. New York, USA: Wiley, 2004, pp. 316–322.

[58] R. Collin, *Foundations for Microwave Engineering*, ser. IEEE Press Series on Electromagnetic Wave Theory. Wiley, 2001, pp. 507–508. [Online]. Available: https://books.google.co.uk/books?id=2SxoQgAACAAJ

[59] J. Breeze, J. Krupka, and N. M. Alford, "Enhanced quality factors in aperiodic reflector resonators," *Appl. Phys. Lett*, vol. 91, no. 15, 2007.

[60] S. Manufacturing, "Spira-shield," 2024, accessed on 14/03/24. [Online]. Available: https://www.spira-emi.com/product/spira-shield/

[61] R. Collin, *Field Theory of Guided Waves*, ser. IEEE Press Series on Electromagnetic Wave Theory. Wiley, 1991, pp. 499–531. [Online]. Available: https://ieeexplore.ieee.org/book/5265444

[62] H. A. Bethe, "Theory of diffraction by small holes," *Phys. Rev.*, vol. 66, pp. 163–182, Oct 1944. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRev.66.163

[63] *BFU730F NPN wideband silicon germanium RF transistor*, NXP Semiconductors, 4 2011, rev. 1. [Online]. Available: https://www.nxp.com/docs/en/data-sheet/BFU730F.pdf

[64] *HMC3653LP3BE HBT GAIN BLOCK MMIC AMPLIFIER, 7 - 15 GHz*, Analog Devices, 9 2017, v02.0917. [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/hmc3653.pdf

[65] *APM-6849SM 2-30 GHz Surface Mount Low Phase Noise Amplifier*, Marki Microwave, 2019, rev F. [Online]. Available: https://markimicrowave.com/assets/0c4b0f88-5ae7-4301-abc5-b56a5ee3ef5e/APM-6849SM-2-30%20GHz%20Surface%20Mount%20Low%20Phase%20Noise%20Amplifier.pdf

[66] *BCR400W Active Bias Controller*, Infineon, 5 2007. [Online]. Available: https://www.infineon.com/dgdl/Infineon-BCR400W-DataSheet-v01_01-en.pdf?fileId=db3a30431400ef68011407e93d8601a1

[67] *SMT Broadband Conical Inductors*, Coilcraft, 12/10/21, document 334R-2. [Online]. Available: https://www.coilcraft.com/getmedia/471b9e75-1786-4dd2-a17c-052e223a0b59/bcr.pdf

[68] *RO4000® Series High Frequency Circuit Materials*, Rogers Corporation, 2022, rev. 1592 080322. [Online]. Available: https://www.rogerscorp.com/advanced-electronics-solutions/ro4000-series-laminates/ro4350b-laminates

[69] *SMA RIGHT ANGLE JACK PCB*, Rosenberger Hochfrequenztechnik GmbH & Co. KG, 2014, tECHNICAL DATA SHEET. [Online]. Available: https://docs.rs-online.com/301e/0900766b814f70e1.pdf

[70] L. Li and K. Wu, "Integrated planar spatial power combiner," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 4, pp. 1470–1476, 2006.

[71] R. W. Klopfenstein, "A transmission line taper of improved design," *Proceedings of the IRE*, vol. 44, no. 1, pp. 31–35, 1956.

[72] D. Kajfez and J. Prewitt, "Correction to "a transmission line taper of improved design" (letters)," *IEEE Transactions on Microwave Theory and Techniques*, vol. 21, no. 5, pp. 364–364, 1973.

[73] Chip, "Klopfenstein taper," 2013, accessed on 13/04/20. [Online]. Available: https://www.microwaves101.com/encyclopedias/klopfenstein-taper

[74] *End Launch Connectors*, WithWave, Nov 2020, 201101 Ver 1.7. [Online]. Available: https://www.with-wave.com/_files/ugd/39c61f_d2f5cd8cb78640ea9269c976b1a68e7c.pdf

[75] *2.92mm END LAUNCH JACK FOR .042" BOARD*, cinch connectivity solutions, 2019, 2.92mm END LAUNCH JACK FOR .042" BOARD. [Online]. Available: https://www.belfuse.com/resources/drawings/cinchconnectivitysolutions/johnson/dr-ccs-john-145-0701-851.pdf

[76] R. Wali, L. Osman, T. Razban, and Y. Mahé, "Electronically reconfigurable two-stage schiffman phase shifter for ku band beam steering applications," *International Journal of Advanced Computer Science and Applications*, vol. 9, no. 11, 2018. [Online]. Available: http://dx.doi.org/10.14569/IJACSA.2018.091178

[77] P. Padilla, J. F. Valenzuela-Valdés, J. L. Padilla, J. M. Fernández-González, and M. Sierra-Castañer, "Electronically reconfigurable reflective phase shifter for circularly polarized reflectar-

ray systems," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 9, pp. 705–707, 2016.

[78] *Thin-Film RF/Microwave Capacitor Technology Thin-Film Technology Accu-P® Series*, KYOCERA AVX, 2021, accu-P Std. [Online]. Available: https://www.mouser.co.uk/datasheet/2/40/Accu_P-3077555.pdf

[79] E. Fooks and R. Zakarevicius, *Microwave Engineering Using Microstrip Circuits*, 1st ed. Division of Simon and Schuster One Lake Street Upper Saddle River, NJUnited States: Prentice Hall, 1990, pp. 129–132.

[80] *12 to 18 GHz 10dB Directional Coupler*, Dielectric Laboratories, June 2023, 2777 Route 20 East, Cazenovia, NY 13035— Phone: (315)655-8710. [Online]. Available: https://www.knowlescapacitors.com/getattachment/Products/Microwave-Products/Couplers/FPC06075_Datasheet.pdf.aspx?lang=en-US

[81] Narda-ATM, "Phase shifter / line stretcher," 2023, accessed on 22 May 2023. [Online]. Available: https://www.atmmicrowave.com/wp-content/uploads/p150xx.pdf

[82] C. W. Nelson, A. Hati, and D. A. Howe, "A collapse of the cross-spectral function in phase noise metrology," *Rev. Sci. Instrum.*, vol. 85, no. 2, p. 024705, Feb. 2014.

[83] H. Black, "Translating systems," U.S. Patent 1,686,792, Oct. 9, 1928.

[84] H. Seidel, "A microwave feed-forward experiment," *The Bell System Technical Journal*, vol. 50, no. 9, pp. 2879–2916, 1971.

[85] M. A. Honarvar, M. Moghaddasi, and A. R. Eskandari, "Power amplifier linearization using feedforward technique for wide band communication system," in *2009 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, 2009, pp. 72–75.

[86] R. N. Braithwaite, "Positive feedback pilot system for second loop control in a feedforward power amplifier," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 10, pp. 3293–3305, 2008.

[87] W. Li, J. Meng, C.-j. Gou, J. Tang, and F.-m. He, "A new analog adaptive feed-forward power amplifier," in *2016 Asia-Pacific International Symposium on Electromagnetic Compatibility (APEMC)*, vol. 01, 2016, pp. 466–468.

[88] C. McNeilage, E. Ivanov, P. Stockwell, and J. Searls, "Review of feedback and feedforward noise reduction techniques," in *Proceedings of the 1998 IEEE International Frequency Control Symposium (Cat. No.98CH36165)*, 1998, pp. 146–155.

[89] A. Hati, C. W. Nelson, and D. A. Howe, "Low phase noise amplifier and oscillator using feed-forward technique at 10 ghz," in *2006 IEEE International Frequency Control Symposium and Exposition*, 2006, pp. 228–232.

[90] *Coaxial Amplifier ZFL-1000VH+*, Mini-Circuits, May 2023, rev. E. [Online]. Available: https://www.minicircuits.com/pdfs/ZFL-1000VH+.pdf

[91] *ZFSC-2-2+ Power Splitter/Combiner*, Mini-Circuits, May 2023, rev. E. [Online]. Available: https://www.minicircuits.com/pdfs/ZFSC-2-2+.pdf

[92] Narda-ATM, "Phase shifter / line stretcher," 2023, accessed on 22 May 2023. [Online]. Available: https://www.atmmicrowave.com/coaxial/phase-shifter-line-stretcher/

[93] *COAXIAL WIDEBAND Digital Step Attenuator ZX76-31R75PP-S+*, Mini-Circuits, May 2023, rev. F. [Online]. Available: https://www.minicircuits.com/pdfs/ZX76-31R75PP-S+.pdf

[94] *ZFDC-10-5-S+ Directional Coupler*, Mini-Circuits, May 2023, rev. D. [Online]. Available: https://www.minicircuits.com/pdfs/ZFDC-10-5+.pdf

[95] *Kesight E8257D-520 PSG Microwave Analog Signal Generator*, Keysight, June 2023. [Online]. Available: https://www.interlligent.co.uk/wp-content/uploads/2020/10/e8257d-psg-microwave-analog-signal-generator-data-sheet.pdf

[96] *Marconi 6960B RF Power Meter*, Marconi, June 1998, vol 2. [Online]. Available: https://usermanual.wiki/Document/MARCONI6960BOpsManual.1282853555/view

[97] *Drop In Monolithic Amplifier DC-2GHz MAR-06+*, Mini-Circuits, June 2023, rev. D. [Online]. Available: https://www.minicircuits.com/pdfs/MAR-6+.pdf

[98] P. Vizmuller, *RF design guide*, 1st ed. 685 Canton Street Norwood, MA 02062 USA: Artech House., 1995, pp. 64–65.

[99] *Keysight Technologies ESA-E Series Spectrum Analyzer*, Keysight, 2017. [Online]. Available: https://www.keysight.com/zz/en/assets/7018-01953/data-sheets/5989-9815.pdf

[100] J. Chauvin, P. Weber, J.-P. Aubry, F. Lefebvre, F. Sthal, S. Galliou, E. Rubiola, and X. Vacheret, "A new generation of very high stability bva oscillators," in *2007 IEEE International Frequency Control Symposium Joint with the 21st European Frequency and Time Forum*, 2007, pp. 1261–1268.

[101] B. Bourgeteau, R. Levy, D. Janiaud, P. Lavenus, O. Le Traon, S. Grousset, T. Signamarcheix, and L. Benaissa, "Quartz resonator for mems oscillator," in *2014 European Frequency and Time Forum (EFTF)*, 2014, pp. 286–289.

[102] H.-Q. Xie, C.-W. Zeng, X.-L. Jia, Y.-D. Peng, C. Wang, and J.-L. Tang, "Optimization for phase noise in cross-coupled integrated quartz crystal oscillator," in *2016 13th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, 2016, pp. 1378–1380.

[103] SDR-Kits, "Introducing the dg8saq vnwa 3 low cost 1.3 ghz vector network analyzer," 2021, accessed on 27/02/24. [Online]. Available: https://www.sdr-kits.net/DG8SAQ-Vector-Network-Analyzer-3-Series

[104] J. Everard, *Fundamentals of RF Circuit Design*, 1st ed. New York, USA: Wiley, 2001, pp. 58–60.

[105] *Automatic RLC meter RLC 100*, Digimess, 1999. [Online]. Available: http://www.digimessinstruments.co.uk/datasheets/english/drlc100eng.pdf

[106] *Audio Dual Matched NPN Transistor SSM2210*, Analog Devices, 2013, rev. C. [Online]. Available: https://www.analog.com/media/en/technical-documentation/obsolete-data-sheets/ssm2210.pdf

[107] J. Everard, *Fundamentals of RF Circuit Design*, 1st ed. New York, USA: Wiley, 2001, p. 119.

[108] *BB201 Low-voltage variable capacitance double diode*, NXP, Oct 2001, product Specification. [Online]. Available: https://www.nxp.com/docs/en/data-sheet/BB201.pdf