
The Electronic and Electrical Engineering
Electrical Machines and Drives Research Group

# Dead Time Compensation and Phase Lag Compensation in 2-Level and 3-Level Grid Connected H-Bridge Power Inverter

By

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# *Abstract*

Dead Time ($\boldsymbol{T_d}$) is a certain time which is added into power inverter for avoiding short circuit events when power switches are turning on or off. Although dead time is used in H-Bridge to avoid a shoot-through event from occurring, it will inevitably cause distortion and energy loss. Methods such as Dead Time Compensation (DTC) and Dead Time Elimination (DTE) are used for compensating power loss, voltage drop, and high distortion caused by dead time $\boldsymbol{T_d}$. In many literatures, most of DTC or DTE are used in 2-level H-Bridge ***PWM*** system for motor drives and open-loop system. This thesis presents a DTC technology which is used in a single phase 2-level and 3-level Grid Connected H-Bridge Power Inverter. As result, except DTC technology, the technology of Phase Locked Loop (***PLL***) and ***PI*** current control are described and discussed as well. Moreover, MATLAB Simulink simulation results, and electrical circuit design experimental results about the DTC in Grid Connected Power Inverter presented in the thesis is discussed.

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| Name | Symbol |
|---|---|
| $\boldsymbol{DC}$ Power Supply | $\boldsymbol{V_{DC}}$ |
| Output voltage from H-Bridge | $\boldsymbol{V_{AB}}$ |
| Average Voltage | $\boldsymbol{V_{AV}}$ |
| Fundamental Voltage of $\boldsymbol{V_{AB}}$ | $\boldsymbol{V_{inv}}$ |
| Grid Voltage | $\boldsymbol{V_{grid}}$ |
| Peak Grid Voltage | $\boldsymbol{\widehat{V}_{grid}}$ |
| Inverter side Current | $\boldsymbol{I_{AB}}$ |
| Grid side Current | $\boldsymbol{I_{grid}}$ |
| Peak Grid Current | $\boldsymbol{\widehat{I}_{grid}}$ |
| Phase Locked Loop | $\boldsymbol{PLL}$ |
| Proportional-Integral Current Control | $\boldsymbol{PI}$ Current Control |
| $\boldsymbol{d}$-axis Grid Voltage | $\boldsymbol{V_{grid(d)}}$ |
| $\boldsymbol{q}$-axis Grid Voltage | $\boldsymbol{V_{grid(q)}}$ |
| $\boldsymbol{d}$-axis Grid current | $\boldsymbol{I_{grid(d)}}$ |
| $\boldsymbol{q}$-axis Grid current | $\boldsymbol{I_{grid(q)}}$ |
| Proportional parameter of $\boldsymbol{PLL}$ | $\boldsymbol{K_{p(PLL)}}$ |
| Integral parameter of $\boldsymbol{PLL}$ | $\boldsymbol{K_{i(PLL)}}$ |
| Proportional parameter of Current Control | $\boldsymbol{K_{p(PI)}}$ |
| Integral parameter of Current Control | $\boldsymbol{K_{i(PI)}}$ |
| Calculated voltage from $\boldsymbol{PI}$ Current Controller | $\boldsymbol{V_{con}}$ |
| Reference $\boldsymbol{d}$-axis Grid Voltage | $\boldsymbol{V_{d(ref)}}$ |
| Reference $\boldsymbol{q}$-axis Grid Voltage | $\boldsymbol{V_{q(ref)}}$ |
| Reference $\boldsymbol{d}$-axis Grid Current | $\boldsymbol{I_{d(ref)}}$ |
| Reference $\boldsymbol{q}$-axis Grid Current | $\boldsymbol{I_{q(ref)}}$ |
| Reference Modulation Signal | $\boldsymbol{V_{sin}}$ |
| Peak voltage of $\boldsymbol{V_{sin}}$ | $\boldsymbol{\widehat{V}_{sin}}$ |
| Carrier signal | $\boldsymbol{V_{tri}}$ |
| Peak voltage of $\boldsymbol{V_{tri}}$ | $\boldsymbol{\widehat{V}_{tri}}$ |
| Modulation index | $\boldsymbol{m_i}$ |
| Duty Cycle | $\boldsymbol{D}$ |
| Duty Cycle of $\boldsymbol{V_{AB}}$ | $\boldsymbol{D_{AB}}$ |
| Sinusoidal Pulse Width Modulation | $\boldsymbol{SPWM}$ |
| $\boldsymbol{PWM}$ frequency | $\boldsymbol{f_{pwm}}$ |
| Modulation signal frequency | $\boldsymbol{f_{sin}}$ |
| Grid frequency | $\boldsymbol{f_{grid}}$ |
| Dead Time Compensation | DTC |
| Deadtime Compensation | $\boldsymbol{DTC}$ |
| Phase Lag Compensation | $\boldsymbol{PLC}$ |
| Dead Time Elimination | DTE |
| Dead Time | $\boldsymbol{T_d}$ |

| | |
|---|---|
| Dead Time Error | $V_e$ |
| Dead Time Duty Cycle | $D_{T_d}$ |
| Dead Time Voltage Reduction | $V_{DT}$ |
| Dead Time Compensation Voltage | $V_{DTC}$ |
| Phase Lag Compensation Voltage | $V_{PLC}$ |
| Inverter side inductor | $L_{inv}$ |
| Inverter side ESR | $R_{inv}$ |
| Grid side inductor | $L_{grid}$ |
| Grid side ESR | $R_{grid}$ |
| Filter Capacitor | $C_f$ |
| Damping Resistor | $R_d$ |

# *Chapter 1*

# Introduction

## *1.1 Background*

What is the power electronic converter? It is an essential piece of technology for transforming electrical energy using the various types of semiconductor power devices, thereby ensuring electrical products are able to work in the right situation and giving the highest efficiency. There are four main types of power electronic converters, DC to DC (buck, boost), AC to AC (frequency conversion), AC to DC (rectifier) and DC to AC (inverter). Power converter could not only change the waveform of voltage and current, but also change other parameters such as frequency and phase angle etc.

The concept and principle of inverter has already been mentioned by David Prince in 1925 through an article in the GE review titled “The Inverter” [1]. Based on research on rectifier device, David Prince gave the idea about converting DC power to AC power or signal, which encouraged the research not only on the inverter, but also the research on thyristor decade later with the advent of semiconductor devices. The development of inverter was challenging and time consuming due to the limits of power devices. Before 1956, the research about inverter is based on rectifier device such as high-vacuum or gas-discharge tube [2]. As result, output power, AC waveform and efficiency are poor. It was not until research regarding the first thyristor was published, spurring investment from industry in 1956, after which the development of power inverter

started to grow up quickly. After invention of thyristor, the growing process of power inverter could be separated into three stages.

The first stage was from 1956 to 1980. The function of thyristor is similar to a diode, limiting the current flow direction. The difference between thyristor and diode is that thyristor could be turned “on” or “off” through the gate signal and it is because of this controllable characteristic that it is able to be utilised in inverter circuits. Voltage-Regulated SCR (Silicon-Controlled Rectifier) inverter was published first. After that, researchers realize that it was important to improve the output waveform from power inverter by designing better strategy to control gate signal. As result, in 1964, F.G.Turnbull put forward strategy “Selected Harmonic Reduction” method for use in the power inverter [3]. This method reduced troublesome harmonics and gave an output waveform which closer to a sinusoidal waveform. This method led to the basic idea for the future research and design on Pulse-Width Modulation (***PWM***) method. Between 1956 and 1980, most of power devices, thyristor mainly, could only work in low switching frequency. As result, most of inverters could only gave low frequency output around 400Hz. At that time, the size of the power inverter, transformer and filter were large, and also the transfer efficiency of inverter was low.

The second stage was from 1981 to 2000. During this stage, the design of power inverter was based on high switching frequency power devices such as Gate Turn-off Thyristor, MOSFET (Metal-Oxide-Semiconductor field-effect transistor) and IGBT (Insulated-

gate Bipolar Transistor) etc. Many electrical equipment such as transformer and filter inductor are related to the switching frequency which needs to be attenuated to improve output waveform fidelity. With higher switching frequency, the size of transformer and inductor can be smaller, which decreasing cost. Higher switching frequencies also afford a larger separation from output fundamental waveform, thereby, reducing the attenuation burden on the filter. As result, increasing switching frequency in the PWM system for driving power inverter is of great importance during this time.

The third stage starts after 2000. Although increasing switching frequency is desirable, increasing it without limit causes issues such as Skin effect, Electromagnetic interface and switching energy loss on power devices are becoming more significant. An important question arises in how to balance energy loss and frequency to reach the highest efficiency. In order to decrease the power loss on power devices, soft-switching technologies such as zero-voltage and zero-current switch had been developed. In addition, multi-level inverter technologies were becoming more popular, and since has become one of the main areas in development of inverter. The advantage of multi-level inverter is that it makes an output AC waveform with smaller voltage quantization transitions, and this lowers total harmonic distortion and decreases power loss in every single power device in an inverter. After 2000, the technologies on microelectronics, computers, intelligent control, and software keep developing. As result, ***PWM*** control technologies are becoming more intelligent, efficient and complex, which increases the output efficiency of power inverters.

Power inverters are widely used in many areas – motor drive, induction heater and air conditioner etc. Nowadays, power inverters are important in developing renewable energy technologies such as wind power and solar power. The aim of developing these renewable energy technologies is to decrease the use of non-renewable energy such as fossil fuel and coal and decrease greenhouse gas emissions. In addition, with the new goal of government policy in global areas, further boosting development of renewable. Achieving Zero-Carbon in 2050 is one of the most important goals in the UK [4][5]. Zero-Carbon is important not only in the UK, but also in the whole world [6]. From the global forecast summary in [7][8], renewable electricity capacity has increased from 750GW in 2016 to 950GW in 2024. And then the capacity goal in 2030 is at least 11000GW. In renewable energy technologies, Photovoltaic solar (PV) technology is a popular and fast-growing technology. The electric capacity of PV power increased from 90GW in 2016 to 400GW in 2024 [7]. Grid Connected PV power inverter system is a main research area in PV power technology. It transfers DC energy from ***PV*** panels to AC output into Grid. Power inverter is very important since it directly influences the efficiency of energy transfer from PV to Grid. As result, switching speed, control technologies and power inverter structure are important research areas in Grid connected PV power system.

## *1.2 Motivation*

With development of renewable energy technologies, higher efficiency power inverter system is required. In any power inverter, a dead time interval is necessary to guarantee a certain time for both devices in a single leg to be ‘off’ to avoid short circuit event during the commutation of power switches. Although dead time can ensure no short circuit event in $\boldsymbol{PWM}$ control, it will inevitably cause distortion since a diode is needed to conduct inductive load current especially during current zero-crossing. In addition, it will cause more problems such as power loss and output voltage reduction etc. In summary, without modification dead time usually negatively affects the performance of the power inverter since without dead time the devices turn-on and off would crossover giving rise to shoot-through, and this would increase power dissipation; the achieved maximum and/or minimum pulse width is affected, and the bridge voltage is not easily controlled at zero current crossings. As result, some technologies such as Dead Time Elimination (DTE) and Dead Time Compensation (DTC) are used to decrease dead time effect in power inverters.

Most DTC and DTE are used in 2-level power inverter in motor drives since the output current and voltage drop directly influences output power on motor. In addition, the voltage and current fluctuation during zero-crossing also influence motor drives. As result, they are used in the power inverter in motor drives for solving the reduction of voltage and current, and the fluctuation during zero-crossing. Main difference between DTC and DTE is current polarity detect method.

On the other hand, some DTC and DTE are also used in grid-connected power inverter. They focus on eliminating the distortion caused by dead time effect during zero-crossing through regulating the close-loop calculations (***PLL***, ***PI***, ***PID*** control etc).

Around 2005 technology dictated the dead time ($\boldsymbol{T_d}$) is usually to be set larger than $\mathbf{5}\boldsymbol{us}$ because of the switching speed of power switch is slow at that time. With new material and technologies for building power switch, switching speed is much faster now. By using high switching speed (short turn on and off time) power switch, dead time $\boldsymbol{T_d}$ can be set to very short ($\boldsymbol{T_d} < \mathbf{0.5}\boldsymbol{us}$). As result, dead time effect is ignored in research when dead time is very short. On the other hand, very high-speed power switch is expensive which increase the cost in product. Besides, the default dead time in most ***PWM*** driver ***IC*** and microcontroller is $\mathbf{1}\boldsymbol{us}$ or more.

On the other hand, $\mathbf{0.5}\boldsymbol{us}$ dead time is short in the power inverter system with $\mathbf{20}\boldsymbol{kHz}$ switching frequency. What if switching frequency is increased to $\mathbf{60}\boldsymbol{kHz}$ or higher, then $\mathbf{0.5}\boldsymbol{us}$ dead time is long in this much higher switching frequency power inverter system. In the future, the turn-on and turn-off time of power switches will be shorter which decrease the dead time. But with the increase of requirement of higher switching frequency, the dead time effect will be more serious.

In conclusion, the technology for compensating dead time effect is still necessary in power inverter system.

## *1.3 Contribution*

In this thesis, a novel Dead Time Compensation (DTC) used in single phase Grid Connected 2-level and 3-level Power Inverter system will be introduced and described. The DTC is consisted of two parts, a deadtime value Compensation (***DTC***) and a Phase Lag Compensation (***PLC***). All contribution presents in this thesis focuses on proving accurate and stable DTC system in grid-connected H-Bridge power inverter. This section presents the contributions in this thesis mainly in Chapter 2, Chapter 3, Chapter 4 and Chapter 5.

### Chapter 2

- Literature review and summary of DTC and DTE technologies.
- Literature review of various of ***PLL*** system, $\boldsymbol{\alpha\beta}$ signal transfer method in single phase system.
- Literature review of technologies of current controller in grid connected systems.

### Chapter 3

- Deadtime Compensation ( ***DTC*** ) operation in 2-level H-Bridge ***SPWM*** compensating power reduction and distortion caused by dead time.
- Phase Lag Compensation (***PLC***) in 2-level H-Bridge ***SPWM*** compensating every phase lag caused by dead time and every signal transfer time delay between output ***PWM*** signal and power switches.

- Deadtime Compensation (***DTC***) operation in 3-level H-Bridge Level-shift ***SPWM***.
- Phase Lag Compensation (***PLC***) operation in 3-level H-Bridge Level-shift ***SPWM***.

## Chapter 4

- Detail of ***PI*** parameter calculation in ***PLL*** and ***PI*** current controller, and decoupling system in ***PI*** current controller.
- An improved current detector based on ***ACPL_7900*** available for detecting high switching frequency component of output current from H-Bridge inverter.
- An improved current polarity detector flows the current detector for providing accurate current direction information for DTC system.

## Chapter 5

- Providing flowchart detail of how the DTC (***DTC*** & ***PLC***) is operated and cooperated with ***PLL*** and ***PI*** current controller without changing their calculation progress in STM32F407 microcontroller.

## *1.4 Thesis Structure*

### Chapter 2

Providing background information and literature review. Section 2.1 provides a short introduction of whole grid-connected power inverter system. Section 2.2 describes the structure of a H-Bridge inverter and $\boldsymbol{SPWM}$ system of 2-level H-Bridge inverter system. Section 2.3 describes the $\boldsymbol{SPWM}$ system in a 3-level H-Bridge inverter. Section 2.4 provides literature review about DTC and DTE technologies. Section 2.5 provides the background information and basic structure of a low-pass filter $\boldsymbol{LCL}$. Section 2.6 introduces the basic information about Phase-Locked Loop ($\boldsymbol{PLL}$) and $\boldsymbol{PI}$ current controller in a grid connected system. Section 2.7 and 2.8 provides the literature review about challenge and technologies in PV power system.

### Chapter 3

Section 3.1 and 3.2 describes the detail of dead time effect in a 2-level H-Bridge inverter including the effect on output voltage, duty cycle and distortion. Section 3.3 describes DTC system operation in a 2-level H-Bridge inverter. Section 3.4 presents a MATLAB Simulink simulation about DTC operation in an open-loop 2-level H-Bridge inverter. Section 3.5 and 3.6 describes the detail of dead time effect and DTC system in a 3-level H-Bridge inverter system. Then, in section 3.7, a simulation of DTC operation in an open-loop 3-level H-Bridge inverter is shown.

## Chapter 4

This chapter focuses on describing the design of experimental platform for DTC operation in grid connected H-Bridge inverter. Section 4.1 provides detail of every component design in a low-pass filter $\boldsymbol{LCL}$. Section 4.2 provides detail about design of $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current controller, including the calculation of $\boldsymbol{PI}$ (Proportional and Integral) compensator parameters. From section 4.3 to 4.6, the design of power switch drive circuit, detector, current polarity detector and safety modules is described.

## Chapter 5

This chapter introduces microcontroller system design of $\boldsymbol{PWM}$, DTC, $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current controller. And then providing detail about how the $\boldsymbol{SPWM}$, $\boldsymbol{DTC}$, $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current controller cooperates in the microcontroller STM32F407.

## Chapter 6

Section 6.1 presents the experimental results of current and voltage detector operation, and then the results of current polarity detector operation in DTC system. Section 6.2 and 6.3 together present the Simulation and Experiment validation about dead time effect and DTC operation in a grid connected 2-level H-Bridge inverter. Finally, section 6.4 shows only the MATLAB simulation result of dead time effect and DTC operation in a grid connected 3-level H-Bridge power inverter.

# *Chapter 2*

## *Background information and literature review*

The previous chapter set out the goals of the research and described the motivation in this project. This chapter reviews relevant research publications providing further insight into the topic and provides a benchmark for the present state-of-the-art. Prior to reviewing the literature, the basic structure of the power electronic converter system is introduced.

## *2.1 Introduction*

This project focuses on developing a grid connected power inverter system. Fundamentally this system consists of an H-Bridge power inverter, pulse width modulator (***PWM***) system, ***PI*** current controller and a ***PLL*** to synchronize inverter system to grid as shown in **Figure 2-1**

Operation of the system is as follows:

With reference to **Figure 2-1**, DC power is transformed into AC via the single-phase inverter stage which then injects AC currents into the grid. The input signals to system are active and reactive power demands and the output is an AC voltage waveform which is synchronized to the grid and an AC current which is phase-shifted from the AC

voltage to inject the requested reactive power. The inverter itself consists of a H-bridge inverter power stage, ***PWM*** generator, ***PI*** current controllers and a phased-locked loop (***PLL***) for synchronizing the inverter output to grid. The inverter output voltage is filtered by a ***LCL*** filter before connecting to grid.

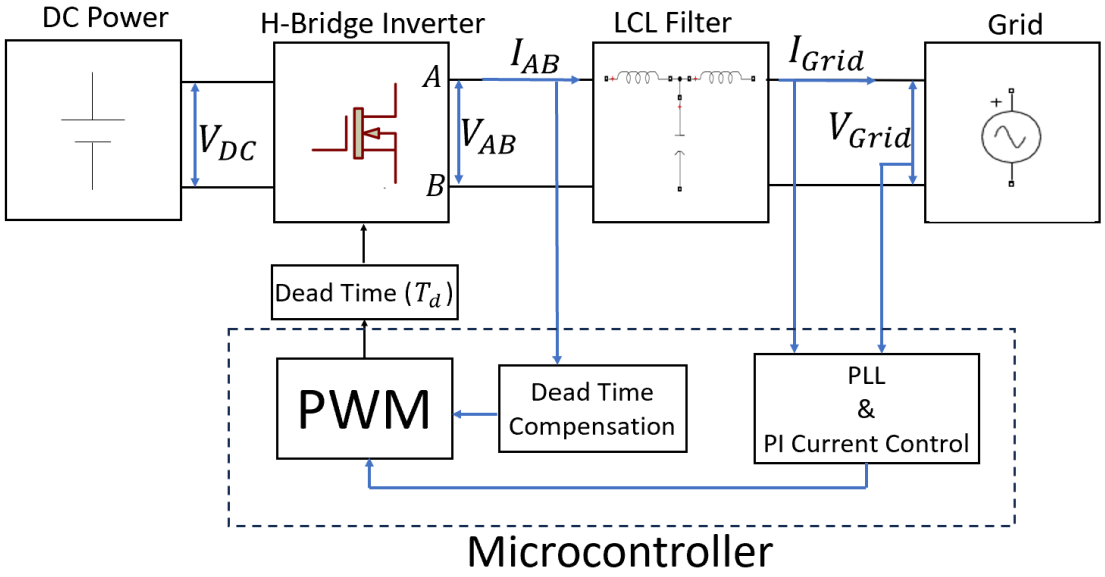


**Figure 2-1: Block Diagram of Grid Connected H-Bridge Power Inverter.**

# 2.2 H-Bridge Power Inverter

## 2.2.1 H-Bridge Inverter

Power inverter is a system which transfers DC power to AC power, and it is widely used in many areas such as motor control, grid power system and renewable energy transfer systems. Of the many types of inverter circuits described in the literature, half-bridge and H (full) bridge are still the most popular due to low-component count and the inherent cost advantage this brings. The work described in this thesis is focused on

H-bridge due to its lower voltage overhead requirements when compared to the half-bridge inverter.

**Figure 2-2** shows a basic structure of H-Bridge inverter which consists of four power switches such as MOSFET and IGBT. In this project, the MOSFET power switch is used in the design of H-Bridge inverter.

H-Bridge inverter contains two power switch legs $\boldsymbol{A}$ and $\boldsymbol{B}$, and each leg contains two power switches with the symbol + denoting the high-side device and – denoting the low-side device. Thus, leg $\boldsymbol{A}$ consists of switches $\boldsymbol{SA+}$ and $\boldsymbol{SA-}$, while the leg $\boldsymbol{B}$ consists of switch $\boldsymbol{SB+}$ and $\boldsymbol{SB-}$. $\boldsymbol{DA+}$ and $\boldsymbol{DA-}$ are the freewheeling diodes of power switches in leg $\boldsymbol{A}$, $\boldsymbol{DB+}$ and $\boldsymbol{DB-}$ are the freewheeling diodes of power switches of leg $\boldsymbol{B}$. In MOSFET power switches, all freewheeling diode functions are achieved by body diodes between drain and source terminals om MOSFET.

The output of leg $\boldsymbol{A}$ is labelled as node $\boldsymbol{A}$, and the output of leg $\boldsymbol{B}$ is labelled node $\boldsymbol{B}$ and the load is connected between these two nodes. The $\boldsymbol{PWM1}$ and $\overline{\boldsymbol{PWM1}}$ are complementary $\boldsymbol{PWM}$ signals used to control the respective switches. The $\boldsymbol{PWM}$ system is described later in this section.

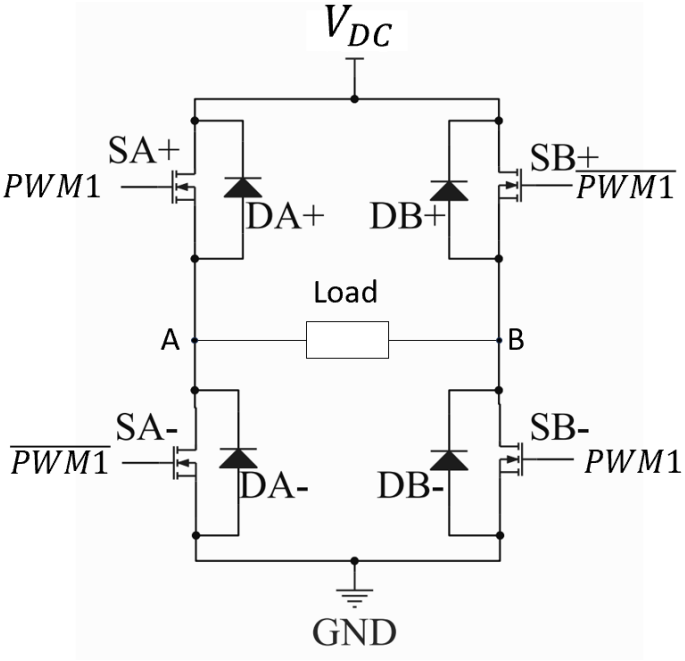


**Figure 2-2 : Basic Structure of H-Bridge Inverter.**

2-level H-bridge produces a bipolar output voltage $\boldsymbol{V_{AB}}$. As shown in **Figure 2-3** (a), when the switches $\boldsymbol{SA+}$ and $\boldsymbol{SB-}$ are turned on, switches $\boldsymbol{SA-}$ and $\boldsymbol{SB+}$ are turned off. Current flows from leg $\boldsymbol{A}$ to leg $\boldsymbol{B}$, with a positive peak current ($\boldsymbol{I_{AB} = +I_{peak}}$), and the load voltage $\boldsymbol{V_{AB} = +V_{DC}}$. When the switches $\boldsymbol{SA+}$ and $\boldsymbol{SB-}$ are turned off, the switches $\boldsymbol{SA-}$ and $\boldsymbol{SB+}$ are turned on, current flows from leg $\boldsymbol{B}$ to leg $\boldsymbol{A}$, as shown in **Figure 2-3** (b). So, the current direction is negative ($\boldsymbol{I_{BA} = -I_{AB}}$) and the load voltage is $\boldsymbol{V_{AB} = -V_{DC}}$. **Figure 2-3** (c) shows the load voltage and current waveforms for a resistive load H-Bridge inverter.

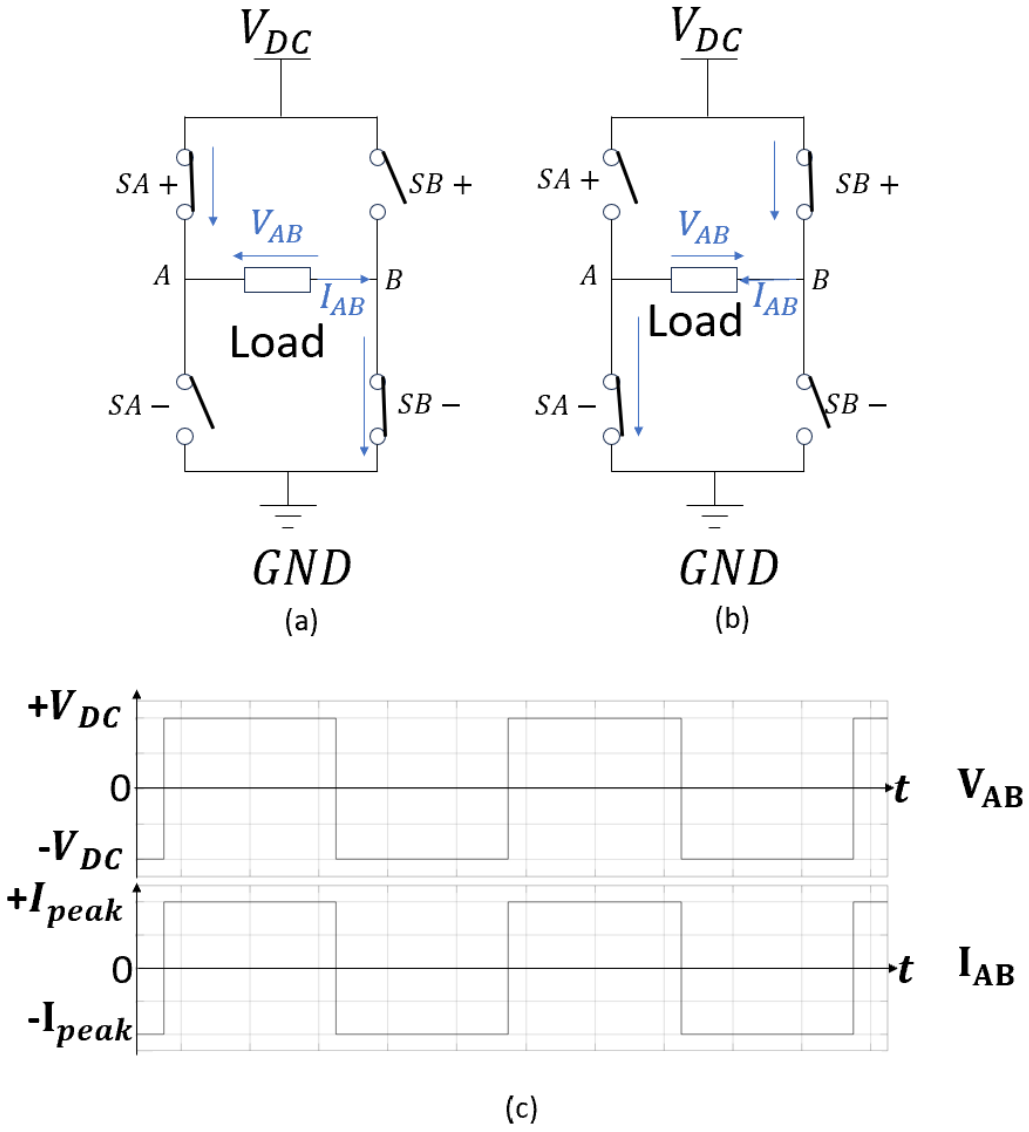


**Figure 2-3 : (a) $V_{AB} = +V_{DC}$, $I_{AB} > 0$. (b) $V_{AB} = -V_{DC}$, $I_{AB} < 0$. (c) Voltage and current waveform with restive load.**

With an inductive load the behavior of H-Bridge is different. The output current with an inductive load cannot change instantaneously. After the inductor flux has been established it will act as current source, and it will continue to maintain current flow (both amplitude and direction) regardless of the status of the switching devices. As result, the freewheeling diodes (body diodes) of switches are used for maintaining the

current path when the power switches are turned off. **Figure 2-4** and **Figure 2-5** shows the direction of output voltage and current between the leg ***A*** and ***B*** of H-Bridge when the load is inductive.

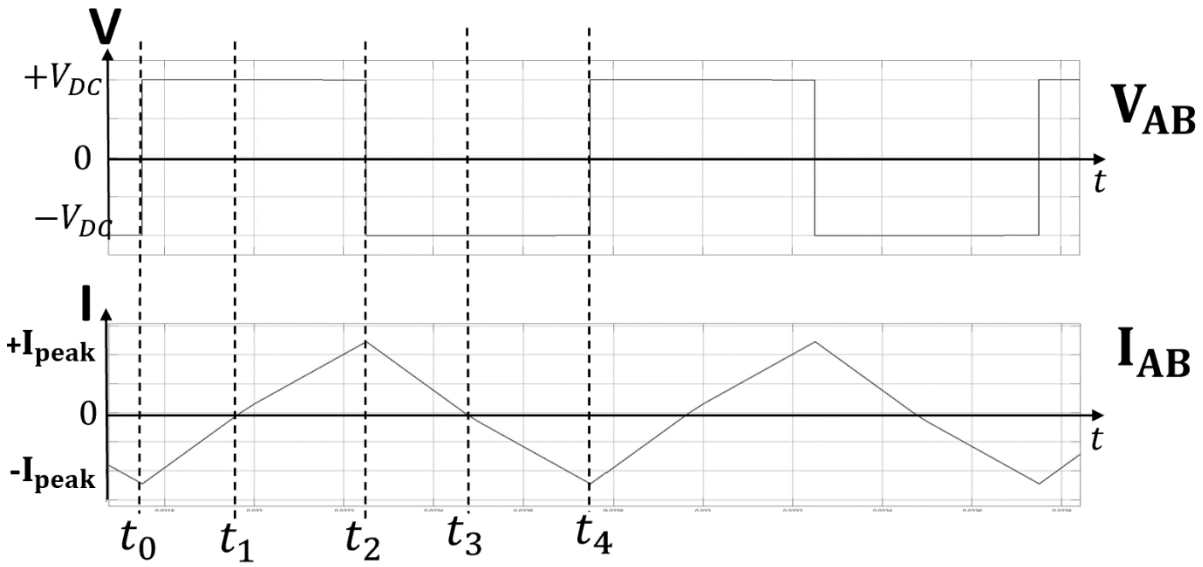


**Figure 2-4 : Output load voltage $V_{AB}$ and current $I_{AB}$ waveform with inductive load.**

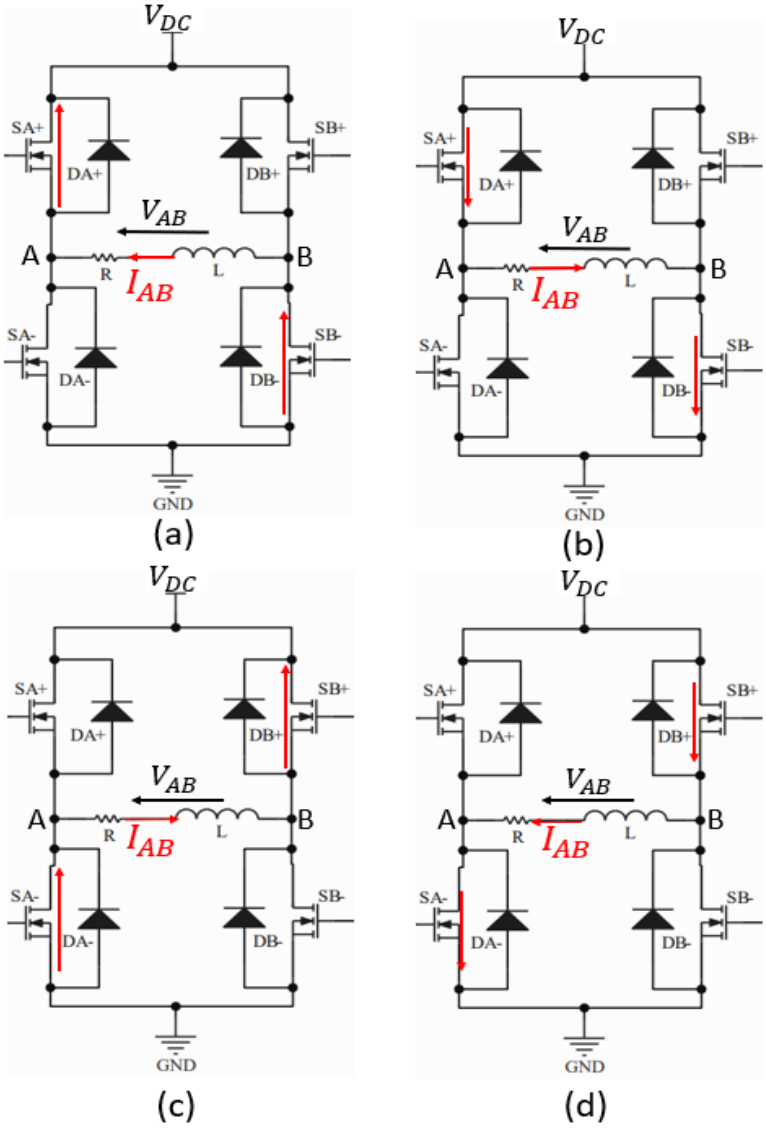


**Figure 2-5 : Voltage and current direction in H-Bridge from when time $t$ from $t_0$ to $t_4$. (a) $t_0$ to $t_1$, (b) $t_1$ to $t_2$, (c) $t_2$ to $t_3$, (d) $t_3$ to $t_4$.**

Before time $\boldsymbol{t_0}$, the switch $\boldsymbol{SA+}$ and $\boldsymbol{SB-}$ are kept off, while $\boldsymbol{SA-}$ and $\boldsymbol{SB+}$ are kept on. The load voltage $\boldsymbol{V_{AB} = -V_{DC}}$ and load current $\boldsymbol{I_{AB} = -I_{peak}}$. At time $\boldsymbol{t_0}$, $\boldsymbol{SA+}$ and $\boldsymbol{SB-}$ turns on, while $\boldsymbol{SA-}$ and $\boldsymbol{SB+}$ turns off, $\boldsymbol{V_{AB} = +V_{DC}}$. From time $\boldsymbol{t_0}$ to $\boldsymbol{t_1}$, the energy stored in inductive load start to release, current keeps flowing from leg $\boldsymbol{B}$ to

leg $\boldsymbol{A}$. Because MOSFET switch is bidirectional after it is conducted, the load current $\boldsymbol{I_{AB}}$ flows from leg $\boldsymbol{B}$ to leg $\boldsymbol{A}$ through the $\boldsymbol{SB-}$ and $\boldsymbol{SA+}$ as shown in **Figure 2-5**(a).

At time $\boldsymbol{t_1}$, the energy stored in load inductance has been fully released, hence the current reaches to $\boldsymbol{0A}$. From $\boldsymbol{t_1}$ to $\boldsymbol{t_2}$, the switches $\boldsymbol{SA+}$ and $\boldsymbol{SB-}$ are still on, while $\boldsymbol{SA-}$ and $\boldsymbol{SB+}$ are still off, $\boldsymbol{V_{AB}}$ is still equal to $\boldsymbol{+V_{DC}}$. The load current $\boldsymbol{I_{AB}}$ flows from leg $\boldsymbol{A}$ to leg $\boldsymbol{B}$ through $\boldsymbol{SA+}$ and $\boldsymbol{SB-}$, which is shown in **Figure 2-5** (b). The inductive load is charged at positive direction and $\boldsymbol{I_{AB}}$ start to increase.

At time $\boldsymbol{t_2}$, the switches $\boldsymbol{SA+}$ and $\boldsymbol{SB-}$ turns off, while $\boldsymbol{SA-}$ and $\boldsymbol{SB+}$ turns on, load voltage $\boldsymbol{V_{AB}}$ changes from $\boldsymbol{+V_{DC}}$ to $\boldsymbol{-V_{DC}}$. The load current $\boldsymbol{I_{AB}}$ reaches to the $\boldsymbol{+I_{peak}}$.

From $\boldsymbol{t_2}$ to $\boldsymbol{t_3}$, the energy stored in the load starts to release and this maintains current flow from leg $\boldsymbol{A}$ to leg $\boldsymbol{B}$ through the $\boldsymbol{SA-}$ and $\boldsymbol{SB+}$ as shown in **Figure 2-5**(c).

At time $\boldsymbol{t_3}$, the energy in inductive load is fully released, hence $\boldsymbol{I_{AB}}$ decrease to 0. From $\boldsymbol{t_3}$ to $\boldsymbol{t_4}$, $\boldsymbol{SA-}$ and $\boldsymbol{SB+}$ are still on, while $\boldsymbol{SA+}$ and $\boldsymbol{SB-}$ are still off, $\boldsymbol{V_{AB}}$ is still equal to $\boldsymbol{-V_{DC}}$. The load current $\boldsymbol{I_{AB}}$ start to flow from leg $\boldsymbol{B}$ to leg $\boldsymbol{A}$ through the $\boldsymbol{SB+}$ and $\boldsymbol{SA-}$ as shown in **Figure 2-5** (d). During this time, the inductive load is charged in negative direction, which increases from 0 to $\boldsymbol{-I_{peak}}$.

The time $\boldsymbol{t_4}$ is equal to $\boldsymbol{t_0 + T_{PWM}}$, where $\boldsymbol{T_{PWM}}$ is the period time of $\boldsymbol{PWM}$ wave. At this time, $\boldsymbol{I_{AB}}$ reaches to $\boldsymbol{-I_{peak}}$ and a new $\boldsymbol{PWM}$ period starts.

From time $\boldsymbol{t_3}$ to $\boldsymbol{t_4}$, switches $\boldsymbol{SA+}$ and $\boldsymbol{SB-}$ turns on ($\boldsymbol{SA-}$ & $\boldsymbol{SB+}$ off), $\boldsymbol{V_{AB} = +V_{DC}}$. Now, the energy stored in the inductor starts to release, current keeps flowing from leg $\boldsymbol{B}$ to leg $\boldsymbol{A}$ through switches $\boldsymbol{SA+}$ and $\boldsymbol{SB-}$. $\boldsymbol{I_{AB}}$ increases from $\boldsymbol{-I_{peak}}$ to 0.

In conclusion, when $\boldsymbol{I_{AB}}$ is positive, the inductor is charged when $\boldsymbol{V_{AB} = V_{DC}}$, while discharged when $\boldsymbol{V_{AB} = -V_{DC}}$. When $\boldsymbol{I_{AB}}$ is negative, the inductor is charged when $\boldsymbol{V_{AB} = -V_{DC}}$, while discharged when $\boldsymbol{V_{AB} = +V_{DC}}$. It is clear to see that the output current is only conducted by the MOSFET power switches in ideal H-Bridge, and the voltage drop on power switches is zero since the resistance of switches is 0 ideally. If the power switches are changed to IGBT, the inductive current from inductive load will be conducted by extra free-wheeling diodes, which may cause voltage drop on diodes. In addition, the effect of diode recovery will affect the system under high frequency.

In the previous discussion, the switches turn on and off at low frequency, and the duty cycle of switches is always 50%. It is clear to see that the energy in the inductor is released and stored completely during the work of the H-Bridge. The inductor in load acts as a filter, which changes the waveform shape of output current and voltage. Comparing the load current waveform in **Figure 2-3** (c) and **Figure 2-4**, $\boldsymbol{I_{AB}}$ is changed from square wave to a triangle wave after inductive filter, but still far from a $\boldsymbol{sin}$ or $\boldsymbol{cos}$ waveform. The output from H-Bridge is related to the filter and circuit design of load. In addition, the control system of H-Bridge is very important. In the next section, the $\boldsymbol{PWM}$ control system is described.

## 2.2.2 *PWM* Control System in 2-level H-Bridge inverter

Before describing ***PWM*** system, two definitions relating to ***PWM*** system needed to be described, which are Duty Cycle and Fundamental signal.

The duty cycle is the ratio of ON time $\boldsymbol{T_{on}}$ of the switch to the ***PWM*** time period $\boldsymbol{T_{PWM}}$. The ***PWM*** time period $\boldsymbol{T_{PWM}}$ is fixed which is equal to the total time of $\boldsymbol{T_{on}}$ and $\boldsymbol{T_{off}}$ time. **Figure 2-6** shows the duty cycle change of a control pulse and equation (1) presents the calculation of duty cycle. The duty cycle of control pulse in ***PWM*** system decides the duty cycle of output voltage $\boldsymbol{V_{AB}(t)}$ from H-Bridge inverter.

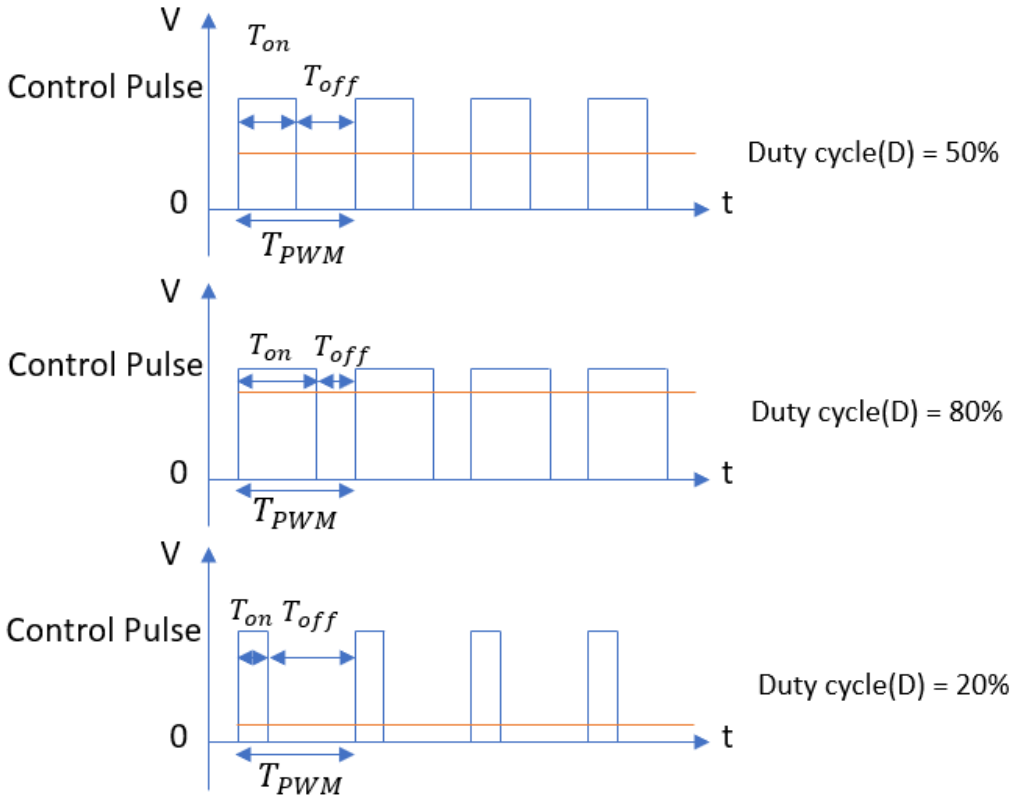


**Figure 2-6 : Control pulse Duty Cycle.**

$$\boldsymbol{Duty\ Cycle = D = \frac{T_{on}}{T_{PWM}}} \qquad (1)$$

Fourier analysis demonstrates that a repeating signal $\boldsymbol{f(t)}$ can be represented by an infinite series of $\boldsymbol{sin/cos}$ waveforms. Typically, a waveform is decomposed into integer multiples of its fundamental frequency $\boldsymbol{\omega_0}$ where the coefficients associated with each $\boldsymbol{sin/cos}$ term represent the contribution of a particular harmonic component. The Fourier series and fundamental signal are important in H-Bridge inverter and $\boldsymbol{PWM}$ system as they are used to determine the total harmonic distortion ($\boldsymbol{THD}$) in the output voltage/current waveforms and help in the design of the output filter. $\boldsymbol{THD}$ is used for checking how much noise or other signals are mixed with the fundamental signal. The definition of the Fourier series is given below where equation (2) shows how a time varying signal $\boldsymbol{f(t)}$ can be decomposed into an infinite sum of sine and cosine terms. Equations (3)-(5) define the coefficients for (2). Equations (6) and (7) define the complex form of the Fourier series.

$$\boldsymbol{f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} [a_n \cos(n\omega_0 t) + b_n \sin(n\omega_0 t)]} \tag{2}$$

$$\boldsymbol{a_0 = \frac{2}{T}\int_0^T f(t)dt = 0(no\ bias)} \tag{3}$$

$$\boldsymbol{a_n = \frac{2}{T}\int_0^T f(t)\cos(n\omega_0 t)\,dt} \tag{4}$$

$$\boldsymbol{b_n = \frac{2}{T}\int_0^T f(t)\sin(n\omega_0 t)\,dt} \tag{5}$$

$$\boldsymbol{f(t) = \sum_{n=-\infty}^{n=\infty} C_n e^{in\omega_0 t}} \tag{6}$$

$$\boldsymbol{C_n = \frac{1}{T}\int_0^T f(t)e^{-in\omega_0 t}dt} \tag{7}$$

Sinusoidal $\boldsymbol{PWM}$ ($\boldsymbol{SPWM}$) is commonly used in controlling power switches in H-Bridge inverters. **Figure 2-7** (a) shows the block diagram of a Sinusoidal Pulse Width Modulation ($\boldsymbol{SPWM}$) system. $\boldsymbol{V_{sin}(t)}$ is the reference sine waveform which is called modulation signal, and it is the amplitude and frequency of this waveform which influences amplitude and frequency of output waveform from inverter. $\boldsymbol{V_{tri}(t)}$ is the triangle wave which is called carrier signal. The signals $\boldsymbol{PWM1}$ and $\overline{\boldsymbol{PWM1}}$ are output $\boldsymbol{PWM}$ signal produced by comparing two signals $\boldsymbol{V_{sin}(t)}$ and $\boldsymbol{V_{tri}(t)}$, they are used for controlling the gate of power switches.

In a 2-level H-Bridge inverter, the switches $\boldsymbol{SA+}$ and $\boldsymbol{SB-}$ are controlled by $\boldsymbol{PWM1}$, while $\boldsymbol{SA-}$ and $\boldsymbol{SB+}$ are controlled by $\overline{\boldsymbol{PWM1}}$. In **Figure 2-7**, the values 0 and 1 correspond to conduction states of the switches with 0 being off (not conducting) and 1 being on (conducting). The signal $\boldsymbol{PWM1}$ and $\overline{\boldsymbol{PWM1}}$ are complementary. When $\boldsymbol{V_{sin}(t) > V_{tri}(t)}$, $\boldsymbol{PWM1 = 1}$ ($\boldsymbol{SA+}$ & $\boldsymbol{SB-}$ **are on**) and $\boldsymbol{\overline{PWM1} = 0}$ ($\boldsymbol{SA-}$ & $\boldsymbol{SB+}$ **are off**), $\boldsymbol{V_{AB}(t) = +V_{DC}}$. This time is on time $\boldsymbol{T_{on}}$. When $\boldsymbol{V_{sin}(t) < V_{tri}(t)}$, $\boldsymbol{PWM1 = 0}$ ($\boldsymbol{SA-}$ & $\boldsymbol{SB+}$ $\boldsymbol{are\ off}$) and $\boldsymbol{\overline{PWM1} = 1}$ ($\boldsymbol{SA-}$ & $\boldsymbol{SB+}$ $\boldsymbol{are\ on}$). $\boldsymbol{V_{AB}(t) = -V_{DC}}$. This time is off time $\boldsymbol{T_{off}}$.

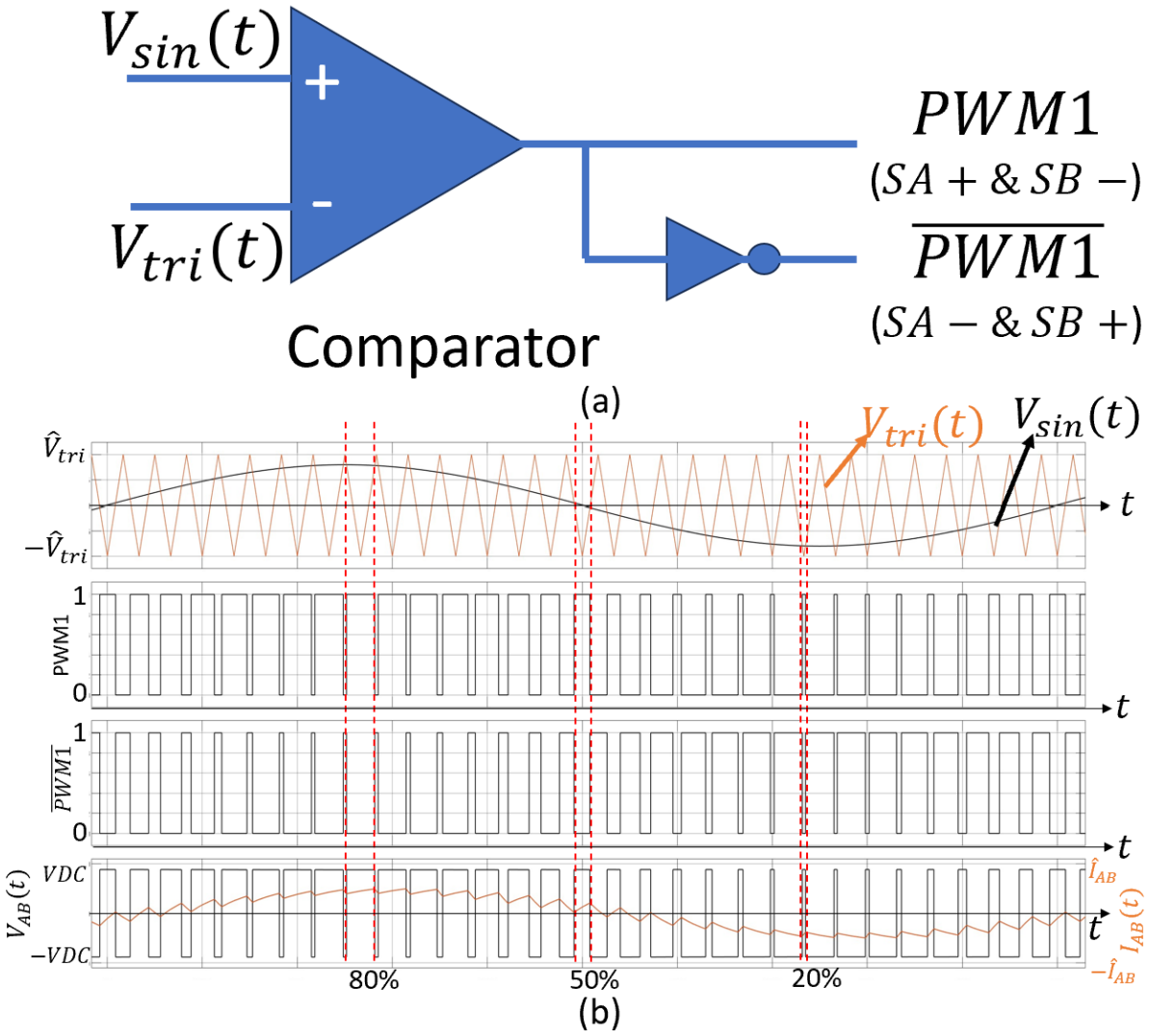


**Figure 2-7 : (a) Block diagram of *PWM* system. (b) waveform of $V_{tri}(t)$, $V_{sin}(t)$, *PWM*1, $\overline{PWM1}$, $V_{AB}(t)$ and $I_{AB}(t)$.**

For the description that follows it has been assumed that the load has been inductively filtered and the corner frequency of the inductive filter is significantly lower than ***PWM*** frequency but higher than the sinusoid frequency such that the current is sinusoidal with a small ripple and has negligible phase shift with respect to the reference. With ***SPWM*** control system, the duty cycle of $V_{AB}(t)$ varies according to the reference signal

$\boldsymbol{V_{sin}(t)}$. The duty cycle also influences the energy charge and release in the inductive load, which influences the increase or decrease of $\boldsymbol{I_{AB}(t)}$.

The reference modulation signal $\boldsymbol{V_{sin}(t)}$ is a per unit value which represents a low frequency $\boldsymbol{sin}$ waveform with equation (8).

$$\boldsymbol{V_{sin}(t) = \widehat{V}_{sin} * \sin(\omega_{sin}\, t) \quad \omega_{sin} = 2\pi f_{sin} \quad f_{sin} = \frac{1}{T_{sin}}} \tag{8}$$

where $\boldsymbol{\widehat{V}_{sin}}$ is the peak value of $\boldsymbol{V_{sin}(t)}$, $\boldsymbol{f_{sin}}$ is the frequency of $\boldsymbol{V_{sin}(t)}$ and it is also the fundamental frequency of output waveform from H-Bridge inverter. $\boldsymbol{V_{tri}(t)}$ is a triangle carrier wave which changes between $\pm\boldsymbol{\widehat{V}_{tri}}$ with high carrier frequency $\boldsymbol{f_{tri}}$. In equation (9), $\boldsymbol{\widehat{V}_{tri}}$ is the peak voltage of $\boldsymbol{V_{tri}(t)}$, the $\boldsymbol{f_{pwm}}$ is the high carrier frequency which is also the $\boldsymbol{PWM}$ frequency. During the first half $\boldsymbol{PWM}$ period from 0 to $\frac{\boldsymbol{T_{pwm}}}{\boldsymbol{2}}$, $\boldsymbol{V_{tri}(t)}$ increases from negative peak value $-\boldsymbol{\widehat{V}_{tri}}$ to positive peak value $\boldsymbol{\widehat{V}_{tri}}$. during half $\boldsymbol{PWM}$ period from $\frac{\boldsymbol{T_{pwm}}}{\boldsymbol{2}}$ to $\boldsymbol{T_{pwm}}$, $\boldsymbol{V_{tri}(t)}$ is decreasing from $+\boldsymbol{\widehat{V}_{tri}}$ to $-\boldsymbol{\widehat{V}_{tri}}$.

$$\boldsymbol{V_{tri}(t) = \begin{cases} \frac{4\widehat{V}_{tri}}{T_{pwm}} * t - \widehat{V}_{tri} & 0 < t < \frac{T_{pwm}}{2} \\ \widehat{V}_{tri} - \frac{4\widehat{V}_{tri}}{T_{pwm}} * t & \frac{T_{pwm}}{2} < t < T_{pwm} \end{cases} \quad T_{pwm} = \frac{1}{f_{pwm}}} \tag{9}$$

**Figure 2-8** shows the zoomed diagram of waveform of signal $\boldsymbol{V_{sin}(t)}$, $\boldsymbol{V_{tri}(t)}$ and $\boldsymbol{V_{AB}(t)}$ in a single $\boldsymbol{PWM}$ period. Because frequency of $\boldsymbol{V_{tri}(t)}$ is much higher than $\boldsymbol{V_{sin}(t)}$, after zooming in one period of $\boldsymbol{V_{tri}(t)}$, the $\boldsymbol{V_{sin}(t)}$ can be seen as a constant value. In $\boldsymbol{PWM}$ system, for avoiding over modulation, the peak value of modulation waveform $\boldsymbol{\widehat{V}_{sin}}$ is lower than $\boldsymbol{\widehat{V}_{tri}}$ ($\boldsymbol{-\widehat{V}_{tri} < V_{sin}(t) < \widehat{V}_{tri}}$).

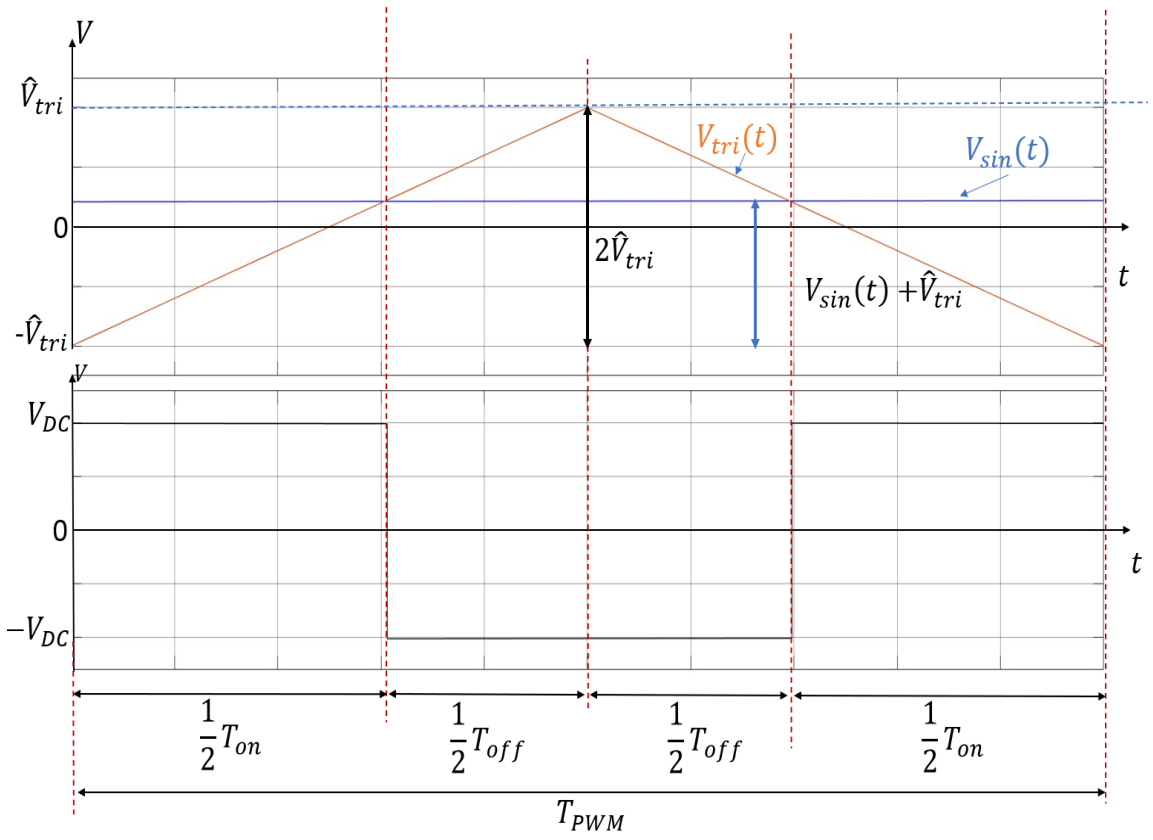


**Figure 2-8 :** Diagram of waveform of signal $\boldsymbol{V_{sin}(t)}$, $\boldsymbol{V_{tri}(t)}$ and output $\boldsymbol{V_{AB}(t)}$ in one $\boldsymbol{T_{pwm}}$

In ***SPWM*** system, the total time of one ***PWM*** period is $\boldsymbol{T_{PWM}}$ which is equal to $\boldsymbol{T_{on} + T_{off}}$. The duty cycle $\boldsymbol{D = \frac{T_{on}}{T_{PWM}}}$ and it is related to the ratio between $\boldsymbol{V_{sin}(t)}$ and $\boldsymbol{V_{tri}(t)}$. Using the similar triangle method the $\boldsymbol{D}$ can be calculated as equation (10) below.

$$\boldsymbol{D = \frac{T_{on}}{T_{pwm}} = \frac{V_{sin}(t) + \hat{V}_{tri}}{2\hat{V}_{tri}} = \frac{1}{2}\left[\frac{V_{sin}(t)}{\hat{V}_{tri}} + 1\right]} \qquad (10)$$

Since the modulation signal $\boldsymbol{V_{sin}(t) = \hat{V}_{sin} * \sin(\omega_{sin} t)}$, equation (10) can be equivalent to equation (11).

$$\boldsymbol{D = \frac{1}{2}\left[\frac{V_{sin}(t)}{\hat{V}_{tri}} + 1\right] = \frac{1}{2}\left[\frac{\hat{V}_{sin}}{\hat{V}_{tri}} * sin(\omega_{sin} t) + 1\right]} \qquad (11)$$

As shown in equation (12), the ratio between $\boldsymbol{V_{sin}(t)}$ and $\boldsymbol{\widehat{V}_{tri}}$ is termed $\boldsymbol{m_i}$ which is called Modulation Index in $\boldsymbol{SPWM}$ system. Then equation (13) shows the $\boldsymbol{D}$ related to the $\boldsymbol{m_i}$.

$$\boldsymbol{m_i = \frac{V_{sin}(t)}{\widehat{V}_{tri}} = \frac{\widehat{V}_{sin}}{\widehat{V}_{tri}} * sin(\omega_{sin} t)} \tag{12}$$

$$\boldsymbol{D = \frac{1}{2}[m_i + 1]} \tag{13}$$

The voltage after low-pass filter of $\boldsymbol{V_{AB}(t)}$ is $\boldsymbol{V_{inv}(t)}$ and its equation is,

$$\boldsymbol{V_{inv}(t) = V_{DC} * m_i} \tag{14}$$

Now, it is clear to see that the $\boldsymbol{D}$ is varies with the modulation signal $\boldsymbol{V_{sin}(t)}$, so as the $\boldsymbol{V_{inv}(t)}$. The voltage $\boldsymbol{V_{inv}(t)}$ is also the fundamental voltage signal of $\boldsymbol{V_{AB}(t)}$.

In conclusion, the parameter of modulation signal $\boldsymbol{V_{sin}(t)}$ decides the frequency, amplitude and phase of output voltage and current from inverter. As shown in **Figure 2-7** (b), the load voltage $\boldsymbol{V_{AB}(t)}$ is a high frequency pulse wave changed between $\pm\boldsymbol{V_{DC}}$, and the load current $\boldsymbol{I_{AB}(t)}$ is a waveform consisted of a low frequency $\boldsymbol{sin}$ wave with fundamental frequency $\boldsymbol{f_{sin}}$ plus a small ripple wave with high $\boldsymbol{f_{pwm}}$ frequency. A suitable low pass filter is required to filter high frequency part from load voltage and current, only leaving the fundamental composition. The design of filter is related to the $\boldsymbol{f_{pwm}}$. Normally, the inductor filter is chosen to have corner frequency lower than $\boldsymbol{f_{pwm}}$. As result, increasing switching frequency to increase $\boldsymbol{f_{pwm}}$ in $\boldsymbol{PWM}$ system is one important research now. The typical technology is the development of $\boldsymbol{GaN}$ material power switches.

## 2.3 3-level H-Bridge inverter and its $PWM$ control

In the previous two sections, the basic operation of a H-Bridge inverter and its $\boldsymbol{SPWM}$ system are described. With a modulation signal $\boldsymbol{V_{sin}(t)}$ and a carrier signal $\boldsymbol{V_{tri}(t)}$, the $\boldsymbol{SPWM}$ signal is produced to drive the power device in a 2-level H-Bridge inverter. In this section, the 3-level H-Bridge inverter and its $\boldsymbol{SPWM}$ system will be introduced.

The 3-level H-Bridge inverter is a kind of multi-level power inverters. The electrical circuit structure of H-Bridge inverter in 2-level and 3-level system are same which shown in **Figure 2-2** in section **2.2.1**, but with different $\boldsymbol{SPWM}$ control system. **Figure 2-9** shows the block diagram of $\boldsymbol{SPWM}$ system of 3-level H-Bridge power inverter.

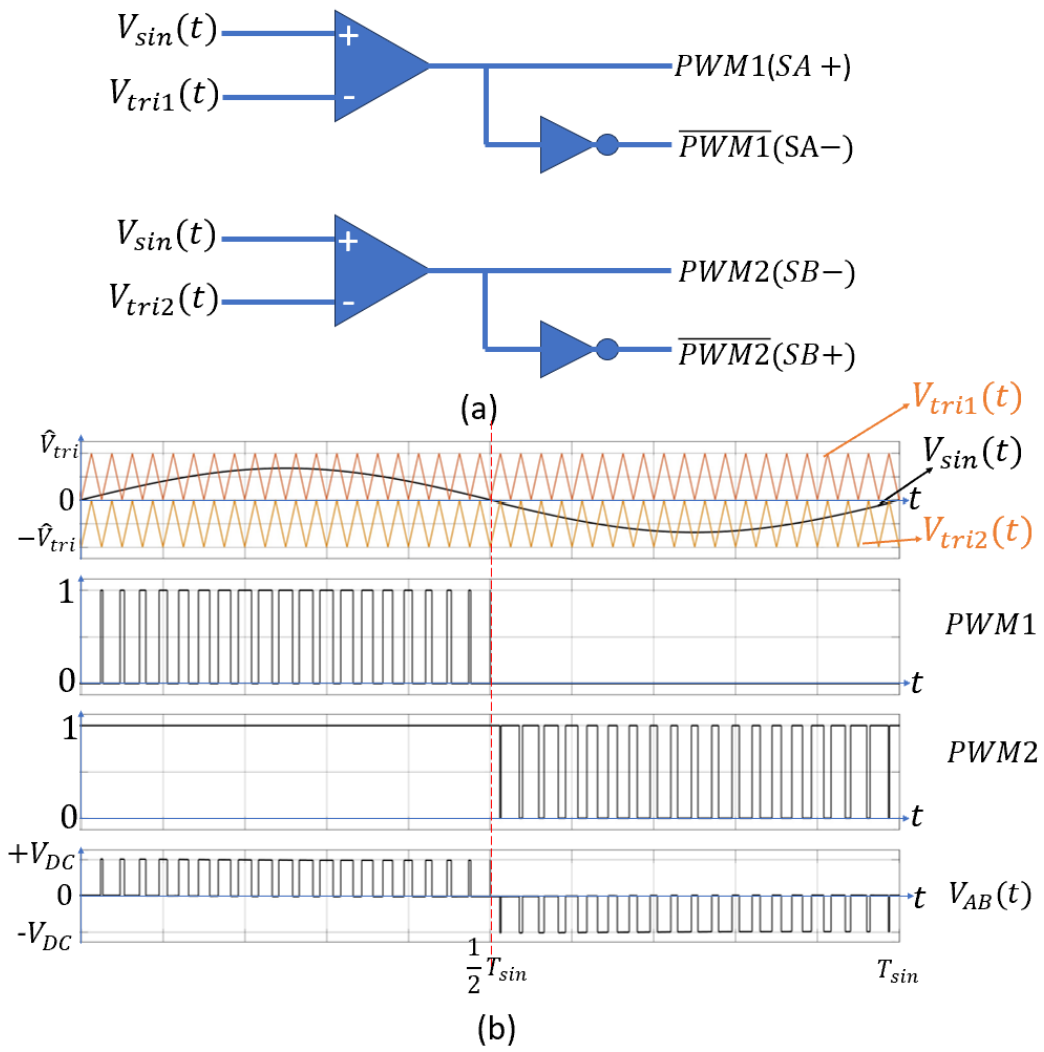


**Figure 2-9: (a) Block diagram of *PWM* system in 3-level H-Bridge inverter. (b) *PWM* input and output signal and output voltage.**

As shown in **Figure 2-9** (b), the output voltage from H-Bridge inverter $\boldsymbol{V_{AB}(t)}$ with 3-level ***SPWM*** system is changed between $+\boldsymbol{V_{DC}}$,$\boldsymbol{0V}$ and $-\boldsymbol{V_{DC}}$.

Referring to **Figure 2-9** (a), ***SA*** side switches and ***SB*** side switches are controlled separately by two ***PWM*** output signals ***PWM1*** and ***PWM2***. As result, in 3-level ***SPWM*** system, two carrier signals are required which are $\boldsymbol{V_{tri1}(t)}$ and $\boldsymbol{V_{tri2}(t)}$. Equation (15) and (16) show equation of $\boldsymbol{V_{tri1}(t)}$ and $\boldsymbol{V_{tri2}(t)}$.

$$V_{tri1}(t) = \begin{cases} \dfrac{2\hat{V}_{tri}}{T_{pwm}} * t & 0 < t < \dfrac{T_{pwm}}{2} \\ \hat{V}_{tri} - \dfrac{2\hat{V}_{tri}}{T_{pwm}} * t & \dfrac{T_{pwm}}{2} < t < T_{pwm} \end{cases} \qquad T_{pwm} = \frac{1}{f_{pwm}} \tag{15}$$

$$V_{tri2}(t) = \begin{cases} \dfrac{2\hat{V}_{tri}}{T_{pwm}} * t - \hat{V}_{tri} & 0 < t < \dfrac{T_{pwm}}{2} \\ -\dfrac{2\hat{V}_{tri}}{T_{pwm}} * t & \dfrac{T_{pwm}}{2} < t < T_{pwm} \end{cases} \qquad T_{pwm} = \frac{1}{f_{pwm}} \tag{16}$$

Referring to **Figure 2-9** (b), signal $V_{tri1}(t)$ is a triangle waveform changes between $0V$ and $+\hat{V}_{tri}$ with $f_{pwm}$. Signal $V_{tri2}(t)$ is a triangle waveform changes between $-\hat{V}_{tri}$ and $0V$ with the same $f_{pwm}$. The frequency and phase of $V_{tri1}(t)$ and $V_{tri2}(t)$ are same with different voltage bias, so, this type of $SPWM$ multi-level control is named as Level-Shift $SPWM$ control.

The output of $PWM$ signals $PWM1$ and $\overline{PWM1}$ are complementary, $PWM2$ and $\overline{PWM2}$ are complementary. The power switch $SA+$ and $SA-$ are controlled by $PWM1$ and $\overline{PWM1}$. The $SB+$ and $SB-$ are controlled by $\overline{PWM2}$ and $PWM2$. As shown in **Figure 2-9** (a), the production of $PWM1$ signal is only related to $V_{sin}(t)$ and $V_{tri1}(t)$. While the $PWM2$ is only related to $V_{sin}(t)$ and $V_{tri2}(t)$.

When $V_{sin}(t) > V_{tri1}(t)$, $PWM1 = 1$ ($SA+$ is on), while $\overline{PWM1} = 0$ ($SA-$ is off). When $V_{sin}(t) < V_{tri1}(t)$, $PWM1 = 0$ ($SA+$ is off), while $\overline{PWM1} = 1$ ($SA-$ is on). On the other hand, when $V_{sin}(t) > V_{tri2}(t)$, $PWM2 = 1$ ($SB-$ is on), while $\overline{PWM2} = 0$ ($SB+$ is off). When $V_{sin}(t) < V_{tri2}(t)$, $PWM2 = 0$ ($SB-$ is off), while $\overline{PWM2} = 1$ ($SB+$ is on).

**Table 1** shows all switching status and the output voltage $\boldsymbol{V_{AB}}$ in an ideal 3-level H-Bridge inverter.

**Table 1: switching status and output voltage $V_{AB}$ relation.**

| Status | $\boldsymbol{PWM1(SA+)}$ | $\boldsymbol{\overline{PWM1}(SA-)}$ | $\boldsymbol{\overline{PWM2}(SB+)}$ | $\boldsymbol{PWM2(SB-)}$ | $\boldsymbol{V_{AB}(V)}$ |
|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 | $\mathbf{0}$ |
| 2 | 1 | 0 | 0 | 1 | $\boldsymbol{+V_{DC}}$ |
| 3 | 0 | 1 | 1 | 0 | $\boldsymbol{-V_{DC}}$ |
| 4 | 0 | 1 | 0 | 1 | $\mathbf{0}$ |

Referring to **Figure 2-9** (b), from time $\boldsymbol{t = 0}$ to $\boldsymbol{\frac{1}{2}T_{sin}}$, $\boldsymbol{V_{sin}(t) > 0}$. $\boldsymbol{V_{sin}(t)}$ at its positive half $\boldsymbol{sin}$ period. Since $\boldsymbol{V_{sin}(t)}$ is always larger than $\boldsymbol{V_{tri2}(t)}$ during this time, $\boldsymbol{PWM2 = 1}$ ($\boldsymbol{SB-}$ is on) and $\boldsymbol{\overline{PWM2} = 0}$ ($\boldsymbol{SB+}$ is off). When $\boldsymbol{V_{sin}(t) > V_{tri1}(t)}$, $\boldsymbol{SA+}$ is on, $\boldsymbol{SA-}$ is off, the voltage between leg $\boldsymbol{A}$ and leg $\boldsymbol{B}$ is $\boldsymbol{V_{AB} = +V_{DC}}$, current flow through the $\boldsymbol{SA+}$ and $\boldsymbol{SB-}$ from leg $\boldsymbol{A}$ to $\boldsymbol{B}$, charging the inductor in output load. The $\boldsymbol{I_{AB}}$ direction is positive ($\boldsymbol{I_{AB} > 0}$). When $\boldsymbol{V_{sin}(t) < V_{tri1}(t)}$, $\boldsymbol{SA+}$ is off, $\boldsymbol{SA-}$ is on. Since both $\boldsymbol{SA-}$ and $\boldsymbol{SB-}$ are conducting, the point $\boldsymbol{A}$ and $\boldsymbol{B}$ are both conducted to the ground, $\boldsymbol{V_{AB} = 0}$. The current from inductor keeps flows in same direction through the $\boldsymbol{SA-}$ and $\boldsymbol{SB-}$. During the positive half period of $\boldsymbol{V_{sin}(t)}$, the $\boldsymbol{T_{on}}$ is the time when $\boldsymbol{V_{sin}(t) > V_{tri1}(t)}$.

From time $\boldsymbol{t = \frac{1}{2}T_{sin}}$ to $\boldsymbol{T_{sin}}$, the $\boldsymbol{V_{sin}(t) < 0}$, $\boldsymbol{V_{sin}(t)}$ at its negative half $\boldsymbol{sin}$ period. During this time, the $\boldsymbol{V_{sin}(t)}$ is always lower than $\boldsymbol{V_{tri1}(t)}$ and so, $\boldsymbol{SA+}$ is off, $\boldsymbol{SA-}$ is on. When $\boldsymbol{V_{sin}(t) < V_{tri2}(t)}$, $\boldsymbol{SB+}$ is on, $\boldsymbol{SB-}$ is off, $\boldsymbol{V_{AB} = -V_{DC}}$, current $\boldsymbol{I_{AB}}$ through the $\boldsymbol{SB+}$ and $\boldsymbol{SA-}$ from leg B to A, charging the inductor in negative direction, $\boldsymbol{I_{AB} < 0}$. $\boldsymbol{V_{sin}(t) > V_{tri2}(t)}$, $\boldsymbol{SB+}$ is off, $\boldsymbol{SB-}$ is on, since $\boldsymbol{SA-}$ and $\boldsymbol{SB-}$ are both conducting, $\boldsymbol{V_{AB} = 0V}$ again. The inductive current keeps flowing in negative direction

through the $SB-$ and $SA-$, $I_{AB} < 0$. During the negative half period of $V_{sin}(t)$, the $T_{on}$ is the time when $V_{sin}(t) > V_{tri2}(t)$.

The main idea of 3-level $SPWM$ is same to the system in the 2-level $PWM$ system, by changing the duty cycle of power switch to control the duty cycle of output voltage $V_{AB}(t)$.

During the positive half period of $V_{sin}(t)$, $V_{AB}(t)$ only changes between $0$ and $+V_{DC}$, and it is related to the $V_{sin}(t)$ and $V_{tri1}(t)$. **Figure 2-10** shows their relationship.

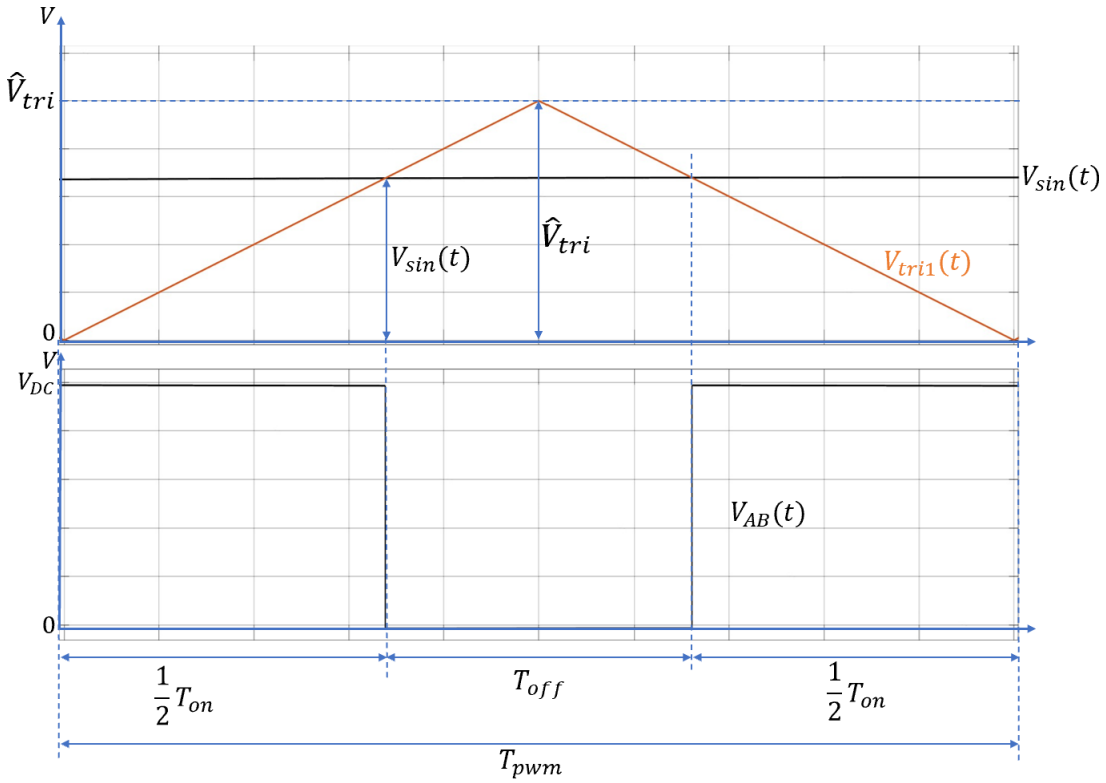


**Figure 2-10: Relation between $V_{sin}(t)$, $V_{tri1}(t)$ and $V_{AB}(t)$ during positive half-cycle.**

Referring to **Figure 2-10**, by using the similar triangle equation, the duty cycle during the positive half period of $V_{sin}(t)$ in 3-level is,

$$D = \frac{T_{on}}{T_{pwm}} = \frac{V_{sin}(t)}{\hat{V}_{tri}} = \frac{\hat{V}_{sin}}{\hat{V}_{tri}} * \sin(\omega_{sin} t) = m_i \qquad (17)$$

In positive half period of $\boldsymbol{V_{sin}(t)}$, $\boldsymbol{1 \geq \sin(\omega_{sin} t) \geq 0}$. The voltage after low-pass filter is,

$$\boldsymbol{V_{inv}(t) = V_{DC} * m_i} \tag{18}$$

During the negative half period of $\boldsymbol{V_{sin}(t)}$, $\boldsymbol{V_{AB}(t)}$ only changes between $\boldsymbol{0}$ and $\boldsymbol{-V_{DC}}$, and it is related to the $\boldsymbol{V_{sin}(t)}$ and $\boldsymbol{V_{tri2}(t)}$. **Figure 2-11** shows their relationship.

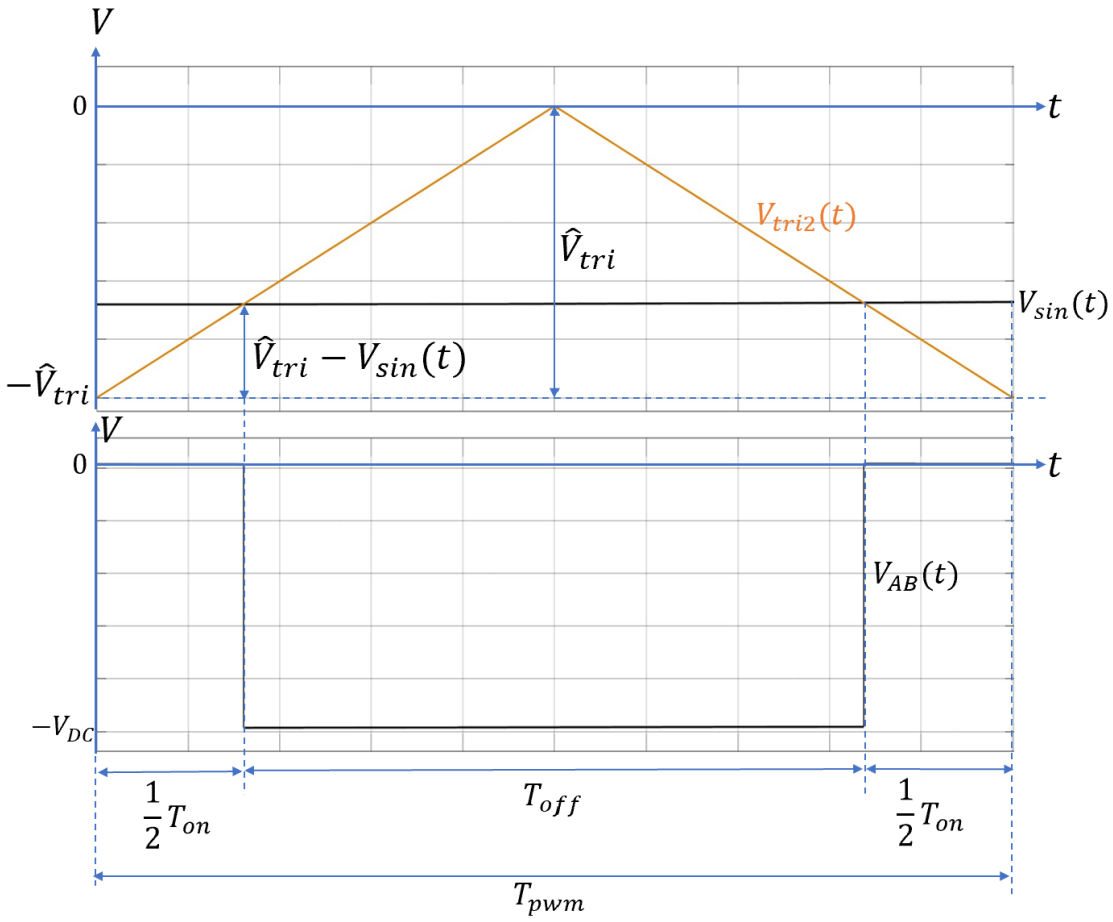


**Figure 2-11: Relation between $\boldsymbol{V_{sin}(t)}$, $\boldsymbol{V_{tri2}(t)}$ and $\boldsymbol{V_{AB}(t)}$ during negative half cycle**

Referring to **Figure 2-11**, the duty cycle $\boldsymbol{D}$ is equal to

$$\boldsymbol{D = \frac{T_{on}}{T_{pwm}} = \frac{V_{sin}(t) - (-\hat{V}_{tri})}{\hat{V}_{tri}} = 1 + m_i} \tag{19}$$

During the negative half period of $\boldsymbol{V_{sin}(t)}$, $\boldsymbol{-1 \leq \sin(\omega_{sin} t) \leq 0}$. The equation of fundamental voltage is

$$\boldsymbol{V_{inv}(t) = V_{DC} * m_i} \quad (20)$$

It is clear to see that, the $\boldsymbol{V_{inv}(t)}$ equation in a whole $\boldsymbol{V_{sin}(t)}$ period is same.

In a 2-level H-Bridge inverter, with only one output $\boldsymbol{SPWM}$ signal $\boldsymbol{PWM1}$, all power switches in leg $\boldsymbol{A}$ and leg $\boldsymbol{B}$ works under high switching frequency in a whole period of $\boldsymbol{V_{sin}(t)}$, which increase power loss on every switches. With 3-level $\boldsymbol{PWM}$ system, the power switches on each side of H-Bridge inverter ($\boldsymbol{SA}$ or $\boldsymbol{SB}$) will only work under high switching frequency in a half period of $\boldsymbol{V_{sin}(t)}$. $\boldsymbol{SA}$ side power switches work in high frequency at positive period of $\boldsymbol{V_{sin}(t)}$ while $\boldsymbol{SB}$ side power switches work in high frequency at negative period. As result, even for the same high switching frequency, comparing to the 2-level H-Bridge inverter, the power loss on each power switch in a H-Bridge inverter during the switching is decreased. On the other hand, with the increase of numbers of carrier signal in $\boldsymbol{PWM}$ system, $\boldsymbol{PWM}$ system will be more complex.

## 2.4 Dead Time Effect and Dead Time Compensation.

The descriptions provided in the previous section assumed the switching devices exhibited ideal switch characteristics and could turn-on and turn-off instantaneously.

Real devices take a finite time to turn-on and turn-off and, therefore, the behavior of the circuit is more complex.

In a two-level or three-level H-Bridge inverter, the two switches on same leg ($\boldsymbol{SA+}$ & $\boldsymbol{SA-}$ or $\boldsymbol{SB+}$ & $\boldsymbol{SB-}$) must not be turned on at same time to avoid short circuit occurring. The high currents that flow during a short circuit may break the power switches with may even lead to the destruction of whole circuit system. In the previous section, all power switches in H-Bridge work under ideal situation, which they can turn on and off instantly. In actual work, any power switch requires a certain time for turning on or off. In order to ensure two switches in same leg are not on at same time, a certain delay time called dead time ($\boldsymbol{T_d}$) is added between the turning off of one device (i.e. $\boldsymbol{SA+}$) and the turning on of the complementary device (i.e. $\boldsymbol{SA-}$).

Although dead time is used in H-Bridge to avoid short-circuit events, it will inevitably cause distortion since the body diode will be needed to conduct the inductive load current. This distortion becomes significant during the zero-crossing points of the reference signal. In addition, it will cause more energy loss in H-Bridge inverter [9]-[14]. In order to decrease the dead time effect, the dead time compensation (DTC) is required.

There are two main methods for decreasing the dead time effect, Dead Time Compensation (DTC) and Dead Time Elimination (DTE). The purpose of DTC [15]-[27] is compensating the output voltage, current reduction and distortion caused by dead time. The dead time still exists, but by producing the right duty cycle of output voltage $\boldsymbol{V_{AB}}$, the voltage and current reduction can be compensated. So as the distortion. Most

DTC techniques rely on knowing the polarity of the inverter current and therefore require accurate current sensor especially for reading high switching frequency component. DTE usually detects the voltage on the freewheeling diode parallel to power switches instead of detecting current polarity [29]-[34]. As result, the accurate current detector is not required in DTE. On the other hand, since every voltage on diode in a power inverter is required to be detected, multiple detectors are required in DTE technologies. Most DTC and DTE calculate the error voltage from output average voltage for compensation, and most of them are used in inverter system in three phase open-loop motor control. But still there are some DTC and DTE technologies are used in close-loop power inverter system [34]-[36], especially in the Neutral-Point-Clamp Converter (NPC) system. In close-loop power inverter system, the DTC and DTE are usually achieved by adding extra calculation into the ***PLL*** or current control calculation for decreasing distortion.

In this research, the DTC will be used for compensating the dead time effects in the single-phase grid connected H-Bridge power inverter without influence the close-loop control calculation progress. The proposed dead-time compensation techniques used in 2-level and 3-level H-Bridge inverter are described in detail in Chapter 3. Many DTC technologies require high accuracy current detectors for taking all current data, but these current detectors are expensive. On the other hand, some current detects technologies take filtered current data and then create simulated inverter current in microcontroller for DTC, but it may cause delay during data transfer and progress and inaccurate current polarity data. In Chapter 4 in this thesis, a cheap and easily design

current detector and current polarity detector designed for DTC system is introduced. It directly produces current polarity information of inverter side current from H-Bridge which can detect high frequency current zero-crossing information, avoiding delay of data transfer as well.

## 2.5 $\boldsymbol{LCL}$ filter

$\boldsymbol{LCL}$ filter is a stable and useful low-pass filter used inside H-bridge inverter system especially for grid-connected H-Bridge power inverter, even in the PV energy system [37]-[39]. In addition, a suitable $\boldsymbol{LCL}$ filter is important in the analysis of dead time effect and DTC. The $\boldsymbol{LCL}$ filter included in inductive load maintains the current flows and voltage output from H-Bridge inverter. During dead time, all power switches are turned off, only the energy stored in the inductive load acting as a current source maintaining output voltage and current flow in H-Bridge inverter. A suitable $\boldsymbol{LCL}$ filter is required not only for filter, but also for supplying enough energy to maintain current flow and voltage during dead time in H-Bridge especially during current zero-crossing time. The DTC technology in this thesis can produce ideal output voltage from inverter, but the $\boldsymbol{T_d}$ still exists. As result, if $\boldsymbol{LCL}$ filter is not suitable, output current from H-Bridge inverter still contains unexpected distortion especially during current zero-crossing even DTC is already operated.

Comparing to L and LC low pass filter, $\boldsymbol{LCL}$ filter is third-order filter, after the cut-off frequency, the slop of dB attenuation can reach to -60dB/dec. As result, it can provide

low current ripple and good harmonic attenuation with smaller size of inductor [40]-[43].

***LCL*** filter in H-Bridge inverter is used to filter high frequency component in ***PWM*** output voltage and current from H-Bridge inverter. **Figure 2-12** shows a typical ***LCL*** filter with damping resistor system.

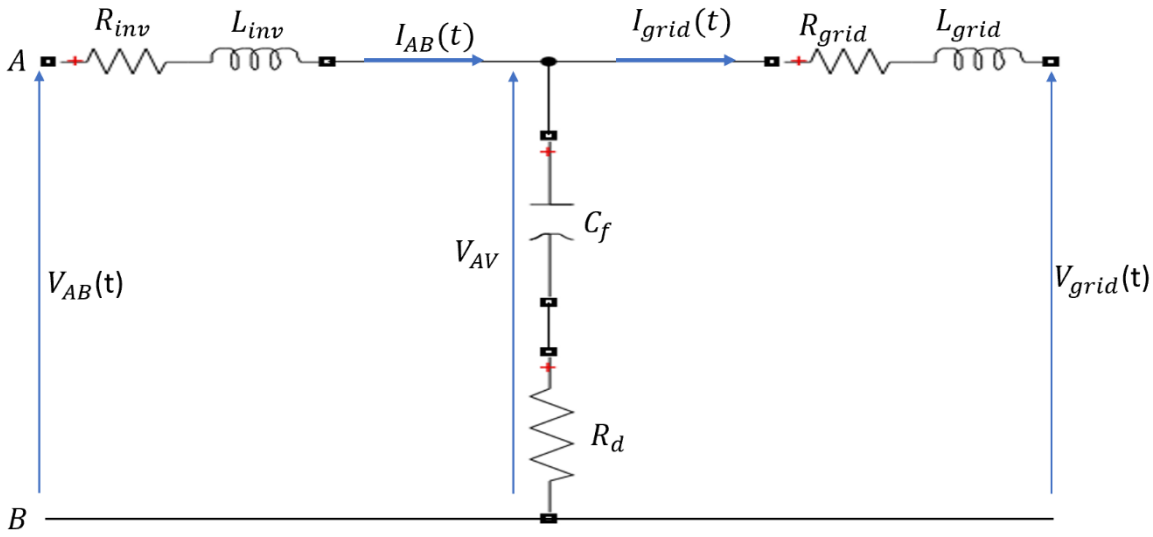


**Figure 2-12 : *LCL* filter with damping resistor**.

As shown in **Figure 2-12**, the input of ***LCL*** filter is $\boldsymbol{V_{AB}(t)}$ from power inverter, while the output from ***LCL*** filter is connected to the grid system which is equal to $\boldsymbol{V_{grid}(t)}$. The design of ***LCL*** filter can be separated into four parts, the design of inverter side inductor $\boldsymbol{L_{inv}}$, capacitor $\boldsymbol{C_f}$, grid side inductor $\boldsymbol{L_{grid}}$ and damping resistor $\boldsymbol{R_d}$. The methods for calculating ***LCL*** parameter are always related to power switching frequency, modulation index, the max ripple of current, maximum output power and maximum voltage drop on two inductors [44]-[49].

The $\boldsymbol{L_{inv}}$ is designed for filtering the highest harmonic component in $\boldsymbol{V_{AB}(t)}$ which occurs at switching frequency $\boldsymbol{f_{tri}}$. After the filtering of $\boldsymbol{L_{inv}}$, the filtered voltage $\boldsymbol{V_{AV}}$

is directly equal to the fundamental voltage $\boldsymbol{V_{inv}(t)}$. In addition, it is mainly used to limit the maximum ripple current in inverter side current $\boldsymbol{I_{AB}(t)}$, which is usually from 5% to 10% [50]. In Chapter 4, equation of calculating $\boldsymbol{L_{inv}}$ according to the ripple current, duty cycle and $\boldsymbol{V_{AB}(t)}$ will be presented.

The design of capacitor $\boldsymbol{C_f}$ is related to the power factor. In order to maintain certain power factor, the $\boldsymbol{C_f}$ is used to absorb the reactive power from total rated power from grid and the reactive power should be lower than $\boldsymbol{10}$% of rated power [48].

In one factor, the second inductor $\boldsymbol{L_{grid}}$ can further attenuate the harmonic after the $\boldsymbol{L_{inv}}$ and $\boldsymbol{C_f}$. The $\boldsymbol{L_{grid}}$ can increase inverter robustness under weak and large variation grid system [51]. In $\boldsymbol{LCL}$ filter, the total inductance $\boldsymbol{L_T} = \boldsymbol{L_{inv}} + \boldsymbol{L_{grid}}$ should be as small as possible for decreasing the voltage drop on the $\boldsymbol{L_T}$. Under low fundamental frequency, the $\boldsymbol{C_f}$ can seem like an open circuit, only $\boldsymbol{L_{inv}}$ and $\boldsymbol{L_{grid}}$ need to be considered. The voltage drops on $\boldsymbol{L_T}$ should be lower than 10% of grid voltage. The $\boldsymbol{L_{inv}}$ has already calculated at first part, after getting the $\boldsymbol{L_T}$, the $\boldsymbol{L_{grid}}$ can be calculated easily.

After $\boldsymbol{L_{inv}}$, $\boldsymbol{L_{grid}}$ and $\boldsymbol{C_f}$ is calculated, the resonance frequency $\boldsymbol{f_{res}}$ of $\boldsymbol{LCL}$ filter can be calculated as well. It is important to ensure that the $\boldsymbol{f_{res}}$ is lower than half of the $\boldsymbol{f_{tri}}$ and high than 10 times of $\boldsymbol{f_{sin}}$ [48][50]. Frequency $\boldsymbol{f_{res}}$ can be used to check whether the design of inductors and capacitor are suitable for the inverter and grid system.

One drawback of $\boldsymbol{LCL}$ filter is its instability caused by the resonance frequency itself [51]. A damping system is used for solving this problem. There are two main types of damping system, passive damping and active damping. In passive damping system, the

passive damping element is added into $\boldsymbol{LCL}$ filter to decrease the resonance peak of the system. In general, passive damping element includes extra resistor or capacitor [49]. The advantage of passive damping is that it does not requires any change on the control strategy. On the contrary, the extra damping element will cause more power loss in filter. Active damping technology focusing on adding extra close-loop system into control strategy to decrease influence from $\boldsymbol{f_{res}}$ [49][53]. The advantage of this method is that it does not require extra damping component, which avoid extra power loss. But the design of control strategy will be complex. In this research, the passive damping technology will be used, and it is presented in section 4.1later.

The detail of calculation of parameter in $\boldsymbol{LCL}$ filter is presented in a later chapter.

# 2.6 Grid connected power inverter system.

## 2.6.1 Phase locked loop ($\boldsymbol{PLL}$)

In a grid connected power inverter system, Phase Locked Loop ($\boldsymbol{PLL}$) and current controller are important for synchronizing inverter output current with grid voltage and injecting active and reactive power.

**Figure 2-13** shows a basic block diagram of Phase Locked Loop which contains Phase Detector (PD), Low Pass Filter (LF) and Voltage Controlled Oscillator (VCO). PD compares VCO output signal, $\boldsymbol{V_{out}}$, to $\boldsymbol{PLL}$ input signal, $\boldsymbol{V_{in}}$, to generate a phase error signal, $\boldsymbol{V_{PD}}$. The error signal is a pulse signal with an average value that corresponds to the phase error and, thus, $\boldsymbol{V_{PD}}$ is low pass filtered to obtain the average phase error

signal, $\boldsymbol{V_{cont}}$. The VCO output frequency $\boldsymbol{\omega_{out}}$ increases or decreases according to the $\boldsymbol{V_{cont}}$. As shown by **Figure 2-13**, $\boldsymbol{V_{cont}}$ is proportional to phase difference and ***PLL*** operates as a feedback loop driving the frequency (and/or phase error) to zero. $\boldsymbol{V_{in}}$ and $\boldsymbol{V_{out}}$ are the time varying signals and $\boldsymbol{\theta_{in}}$ and $\boldsymbol{\theta_{out}}$ are actual phase signals. Simple ***PLL*** implementations use a XOR gate as the phase detector but can only synchronize the frequency. To achieve simultaneous frequency and phase lock a phase frequency detector based on state machine is often used[54]-[57].

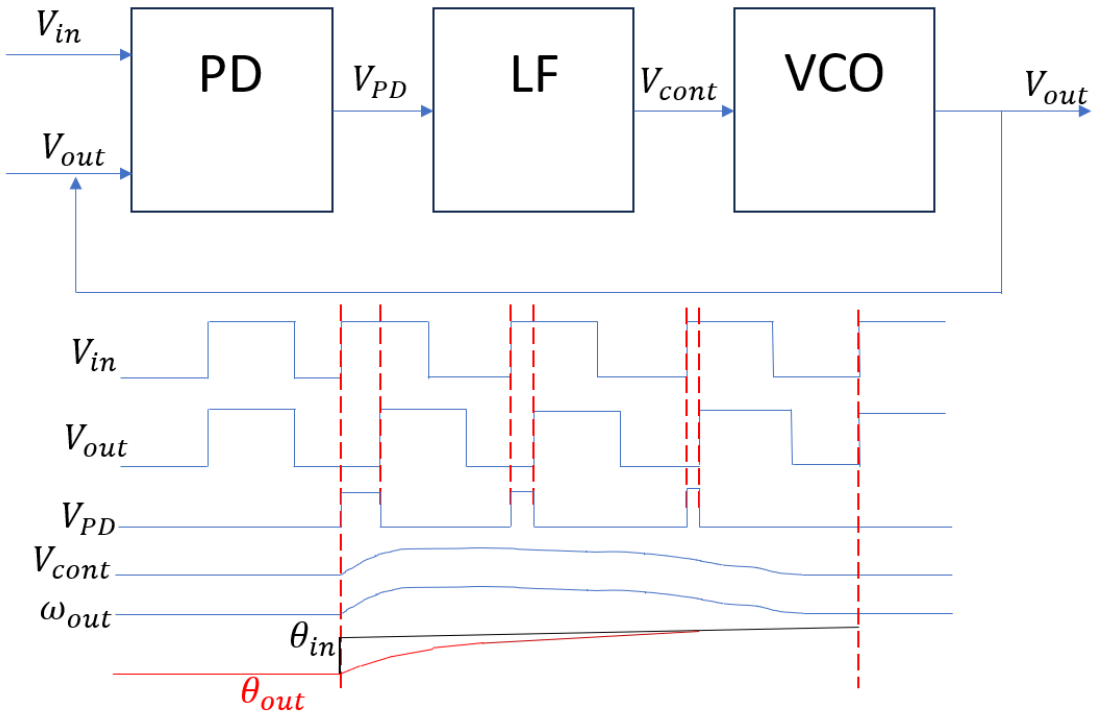


**Figure 2-13 :A basic Phase Locked Loop.**

There are many different types of ***PLL*** used in three-phase grid system. But the presented state-of-art is Synchronous reference frame ***PLL*** (SRF- ***PLL***). SRF- ***PLL*** is achieved by detecting the fundamental frequency ($\boldsymbol{\omega_{grid}t}$) and angle ($\boldsymbol{\theta_{grid}}$) from

power grid. **Figure 2-14** shows the block diagram of an SRF- ***PLL*** system and its relationship with PD, LF and VCO.

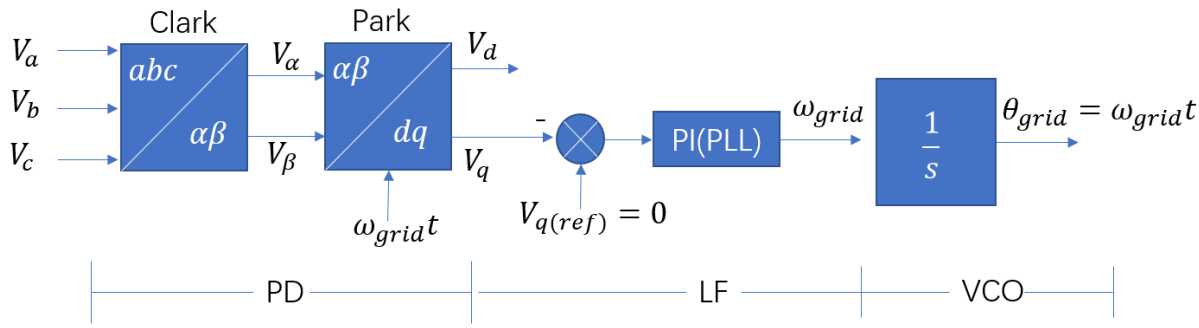


**Figure 2-14 : The block diagram of SRF- *PLL*.**

By using Clark and Park transform, the three-phase reference frame can be transferred to $\boldsymbol{dq}$ rotating reference frame where $\boldsymbol{d}$ and $\boldsymbol{q}$ represent the direct and quadrature components of the signal. In SRF- ***PLL***, $\boldsymbol{d}$ axis is usually the main control axis, is usually aligned with $\boldsymbol{V_a}$ and it represents in-phase (active) contribution of the signal. Since the goal of ***PLL*** is to generate an in-phase locked reference signal, $\boldsymbol{q}$ axis contribution should be zero and therefore an ***PI*** compensator is used to for the $\boldsymbol{q}$ axis signal component $\boldsymbol{V_q}$ to zero.

Clark equation shown in equation (21) connects the phase voltages $\boldsymbol{V_{a,b,c}}$ to $\boldsymbol{dq}$ components $\boldsymbol{V_{d,q}}$ when the $\boldsymbol{d}$ axis is aligned with $\boldsymbol{V_a}$ axis.

$$\begin{pmatrix} \boldsymbol{V_d} \\ \boldsymbol{V_q} \\ \boldsymbol{V_0} \end{pmatrix} = \frac{\boldsymbol{2}}{\boldsymbol{3}} \begin{pmatrix} \boldsymbol{\cos(\theta_{grid})} & \boldsymbol{\cos\left(\theta_{grid} - \frac{2}{3}\pi\right)} & \boldsymbol{\cos\left(\theta_{grid} + \frac{2\pi}{3}\right)} \\ \boldsymbol{-\sin(\theta_{grid})} & \boldsymbol{-\sin\left(\theta_{grid} - \frac{2}{3}\pi\right)} & \boldsymbol{-\sin\left(\theta_{grid} + \frac{2}{3}\pi\right)} \\ \boldsymbol{\frac{1}{2}} & \boldsymbol{\frac{1}{2}} & \boldsymbol{\frac{1}{2}} \end{pmatrix} * \begin{pmatrix} \boldsymbol{V_a} \\ \boldsymbol{V_b} \\ \boldsymbol{V_c} \end{pmatrix} \quad (21)$$

If the voltage of a phase is defined as $\boldsymbol{V_a = V_m * \cos(\theta)}$, and $\boldsymbol{\theta = \theta_{grid}}$, then after the transformation, $\boldsymbol{V_d = V_m}$, and, if the ***PLL*** is locked, $\boldsymbol{V_q}$ and $\boldsymbol{V_0}$ are both zero.

Although SRF- ***PLL*** is the most convenient ***PLL*** system, it is highly dependent on the quality of grid signals. Noise and distortion present three phase grid voltages may influence the accuracy of ***dq*** system. As result, SRF- ***PLL*** need extra filtering to eliminate the noise and high harmonic in the grid such as Moving average filter (MAF- ***PLL***) and complex coefficient filter (CCF- ***PLL***) [58]-[70].

SRF- ***PLL*** system for a single-phase system is similar to that in three-phase system with the exception that only the Park transformation is used to transfer ***αβ*** reference frame to ***dq*** rotating reference frames. Since the single-phase grid system consists of only one signal, the grid is set as the ***α*** signal and the ***β*** signal is generated by delaying the input by a quarter of a cycle $\left(\frac{T}{4}\right)$ from ***α***. This kind of single phase ***PLL*** is called orthogonal-signal-generator-based phase-locked loops (OSG- ***PLL***) since $V_\beta$ lags $V_\alpha$ by **90°**. The block diagram for OSG- ***PLL*** is shown in **Figure 2-15**.

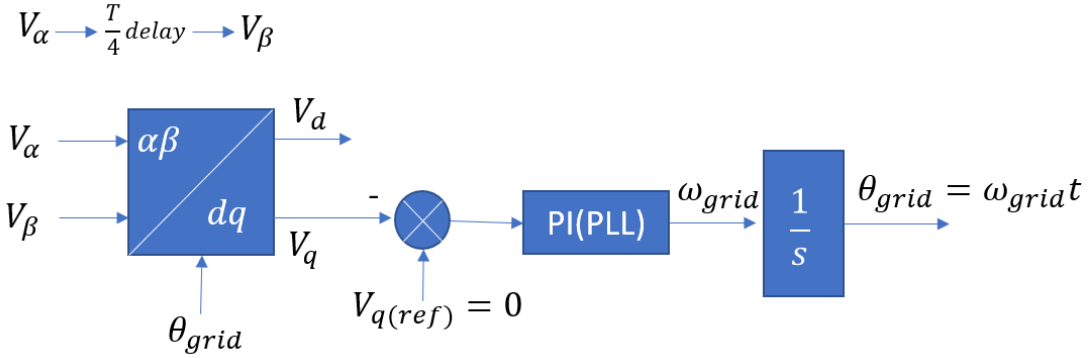


**Figure 2-15 : Basic block diagram of *PLL* in single phase grid system.**

There are two different Park transform equations that can be used depending on alignment of the ***α***-axis to the ***d***-axis or the ***q***-axis.

$$\begin{pmatrix} \boldsymbol{V_d} \\ \boldsymbol{V_q} \end{pmatrix} = \begin{pmatrix} \boldsymbol{\cos(\theta_{grid})} & \boldsymbol{\sin(\theta_{grid})} \\ \boldsymbol{-\sin(\theta_{grid})} & \boldsymbol{cos(\theta_{grid})} \end{pmatrix} \begin{pmatrix} \boldsymbol{V_\alpha} \\ \boldsymbol{V_\beta} \end{pmatrix} \quad (22)$$

$$\begin{pmatrix} \boldsymbol{V_d} \\ \boldsymbol{V_q} \end{pmatrix} = \begin{pmatrix} \boldsymbol{\sin(\theta_{grid})} & \boldsymbol{-\cos(\theta_{grid})} \\ \boldsymbol{\cos(\theta_{grid})} & \boldsymbol{sin(\theta_{grid})} \end{pmatrix} \begin{pmatrix} \boldsymbol{V_\alpha} \\ \boldsymbol{V_\beta} \end{pmatrix} \quad (23)$$

If grid signal is taken as being a cosine waveform, then $\boldsymbol{V_\alpha = V_m \cos(\theta)}$ and $\boldsymbol{V_\beta = V_m \sin(\theta)}$, $\boldsymbol{V_m}$ is the peak voltage of grid**.** The $\boldsymbol{V_{d,q}}$ can be calculated by equation (22). And when the actual $\boldsymbol{\theta}$ is equal to the $\boldsymbol{\theta_{grid}}$, the $\boldsymbol{V_d = V_m}$ while $\boldsymbol{V_q = 0}$. If the grid signal is a sine waveform then $\boldsymbol{V_\alpha = V_m \sin(\theta)}$ and $\boldsymbol{V_\beta = -V_m \cos(\theta)}$, by using equation (23), and when $\boldsymbol{\theta = \theta_{grid}}$, $\boldsymbol{V_d = V_m}$ while $\boldsymbol{V_q = 0}$. In both systems, $\boldsymbol{d}$-axis is the main control axis and $\boldsymbol{V_q}$ is kept at 0 through the ***PI*** system to achieve ***PLL***.

As with the three-phase ***PLL*** system, the accuracy of ***PLL*** is determined by the characteristics of the voltage detector and noise distortion of grid voltages. The performance of the single-phase ***PLL*** is also dependent on the generating an accurate $\boldsymbol{\beta}$ signal. Reference [71] provides a discussion of the methods used to transform $\boldsymbol{\alpha}$ to $\boldsymbol{\beta}$. The most popular way is the Time-Delay (TD)- ***PLL*** which is often achieved digitally but relies on the accurate voltage detector and low distortion of grid. A second method is to use the Hilbert transform to replace the TD in ***PLL***. Hilbert transform is also known as a quadrature filter, which can phase shift signal by $\pm\frac{\boldsymbol{\pi}}{\boldsymbol{2}}$ according to the frequency. Hilbert transform can produce orthogonal signal from input grid signal and used in ***PLL*** control. The ideal Hilbert transform can make phase shift without change on amplitude of input signal. But in actual work, the different signals caused by the Hilbert transform will influence $\boldsymbol{V_d}$ and $\boldsymbol{V_q}$ reference in ***PLL***. The Second Order General Integrator ***PLL*** (SOGI- ***PLL***) produces a pair of orthogonal signals from the

original grid signal while at the same time providing filtering which can suppress the high harmonic and DC component. This method is widely used in single-phase ***PLL*** system now, but the challenge is its complex design. References [71]-[79] contains more information about OSG- ***PLL*** in single phase system. In conclusion, in ***PLL*** system, ***dq*** rotating reference frame is required from grid. To maintain in phase with grid system, the component $V_q$ should be kept zero and the $V_d$ represent peak voltage of grid. The challenge of ***PLL*** system is how to get accurate signal under distorted grid, creating accurate ***dq***-axis signal.

## 2.6.2 Current controller

The current controller is responsible for ensuring the correct amplitude and phase current is injected into the grid. The proportional-integral (***PI***) current control [84]-[91] is the most popular method used in three-phase and single-phase grid-connected power system. **Figure 2-16** shows the ***PI*** current controller used in single phase grid connected power inverter for providing reference signals in ***PWM*** modulator.

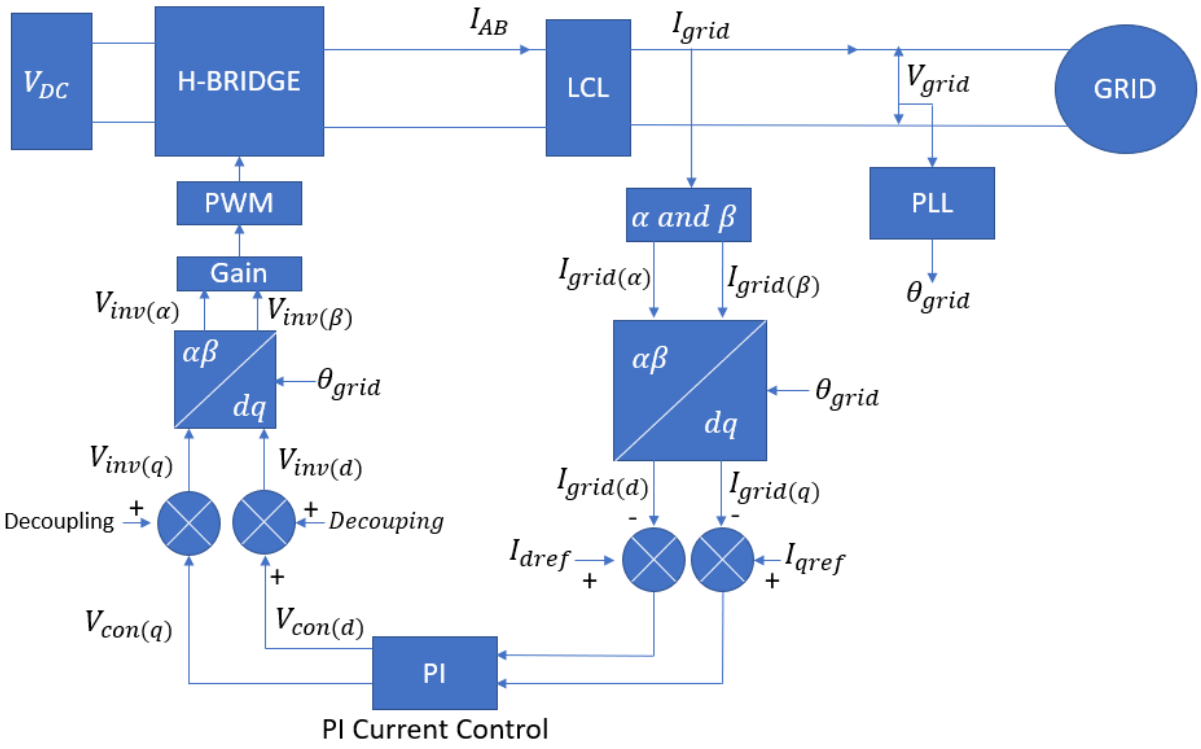


**Figure 2-16 : *PI* current control in single phase grid connected power inverter.**

Similar to ***PLL*** system, current controller is performed in ***dq*** reference frame and, therefore, it is necessary to transform the measured signal from their single-phase values by using ***α*** to ***β*** and Park transformation. The goal of current controller is to ensure the current injected into the grid, $\boldsymbol{I_{grid}}$, has the correct amplitude and phase to meet the active (***P***) and reactive (***Q***) power demand. Referring to **Figure 2-16**, the grid current and voltage, $\boldsymbol{I_{grid}}$ & $\boldsymbol{V_{grid}}$, can be measured and used to determine the actual ***P*** and ***Q*** delivered to the grid. $\boldsymbol{I_{grid}}$ is transformed into ***dq*** components, $\boldsymbol{I_{grid(d)}}$ and $\boldsymbol{I_{grid(q)}}$, to facilitate the power measurements and to provide feedback measurements for the inner current loops. The measured ***dq*** grid currents are compared to reference current values $\boldsymbol{I_{dref}}$ and $\boldsymbol{I_{qref}}$ that are obtained from the higher-level ***PQ*** power controller. Normally, the $\boldsymbol{I_{grid(d)}}$ represents the active power component in the grid

current which should directly equal to the peak current value of grid current if unity power factor is required while the $\boldsymbol{I_{grid(q)}}$ should be kept at zero to suppress the reactive power. The $\boldsymbol{dq}$ current error signals are then fed into a $\boldsymbol{PI}$ compensator which is tuned to drive the current error signal to zero within a reasonable time. In order to decrease the effects of the grid distortion though from inductor in $\boldsymbol{LCL}$ filter a decoupling system is used after $\boldsymbol{PI}$ compensators [96]-[98] providing the inverter output voltages $\boldsymbol{V_{inv(d,q)}}$. Inverse Park transformations provide the $\boldsymbol{V_{inv(\alpha,\beta)}}$ which represents the fundamental $\boldsymbol{sin}$ or $\boldsymbol{cos}$ signal of $\boldsymbol{V_{AB}(t)}$. According to equation (14) from section 2.2.1, $\boldsymbol{V_{inv(\alpha)}(t) = V_{DC} * \frac{\hat{V}_{sin} * \sin(\omega_{sin} t)}{\hat{V}_{tri}}}$, where $\boldsymbol{\hat{V}_{sin} * \sin(\omega_{sin} t)}$ is the reference signal in $\boldsymbol{SPWM}$ system and it is equal to $\boldsymbol{V_{inv(\alpha)}(t) * \frac{\hat{V}_{tri}}{V_{DC}}}$. The $\boldsymbol{\frac{\hat{V}_{tri}}{V_{DC}}}$ is the **Gain** in the current control system shown in **Figure 2-16**

The $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current controller operate together simultaneously. Once locked, the $\boldsymbol{PLL}$ supplies the frequency $\boldsymbol{\omega_{grid}}$ and angle $\boldsymbol{\theta_{grid}}$ into system, while $\boldsymbol{PI}$ current controller produces modulation signal into $\boldsymbol{PWM}$ system according to the $\boldsymbol{\omega_{grid}}$, $\boldsymbol{\theta_{grid}}$ and demanded grid current values. $\boldsymbol{PI}$ current controller is suitable for SPWM, SVPWM and multi-level PWM systems [89][92]-[95]. One of drawbacks of $\boldsymbol{PI}$ current controller is its zero-steady-state error. Even $\boldsymbol{PI}$ compensator works under the steady-state situation, there is still small fluctuation remain in the actual output around the reference value. Proportional-Resonant (PR) current control focus on producing infinite gain at fundamental frequency to eliminate the fluctuation during the steady-state situation in $\boldsymbol{PI}$ current control [99]-[106]. Comparing to $\boldsymbol{PI}$ current control, $\boldsymbol{PR}$ current controller is a stationary frame control ($\boldsymbol{\alpha\beta}$ axis control), the Park transfer is not

required in ***PR* current** controller. In addition, the ***PQ*** outer control loop and voltage outer loop are the system which taking the output power and voltage from ***DC*** link as the reference to produce the reference current value $\boldsymbol{I_{dref}}$ and $\boldsymbol{I_{qref}}$ [91][103].

# 2.7 PV power system

Solar Photovoltaic (PV) is one of the most important and popular renewable energy sources in recent years. The power inverter is widely used in PV power system for transferring the DC energy from solar PV panels to AC energy. In grid connected power system, the grid will be fed by the energy from solar PV array. One challenge in PV grid connected power system is the voltage and power control system of DC link from PV panel. Unlike regular DC input source, the power from solar PV varies according to weather, angle and the load. As result, the variable DC voltage may influence the energy which can be transferred into grid. In order to maximise energy transfer, Maximum Power Point Tracker (MPPT) system is widely used in PV grid connected power inverter system [107]-[112]. MPPT form an outer control loop which varies the inverter's DC link voltage, typically using a boost converter, to ensure the maximum power can be extracted from the PV system.

One challenge with PV grid connected inverter system is leakage current caused by high frequency switching interacting with the PV panel capacitance. It is directly related to the structure of power inverter, ***PWM*** system and output filter and stray capacitance, $\boldsymbol{C_{PV}}$, of PV panel which is usually connected to earth for safety reasons.

As result, common-mode and differential-mode voltage caused by inverter creates leakage current. It is mandated that electrical circuits should be protected from earth leakage currents above a certain level. Therefore, excessive leakage currents can lead to nuisance tripping and in some circumstances prove hazardous. Further analysis of leakage current is explained in the next section.

Transformers are widely used to mitigate PV leakage current by providing isolation between output from power inverter and grid. However, transformers are large and expensive. In recent years, transformerless topologies have received research attention. Instead of using a transformer, a combination of filters and/or modified circuit topologies and/or modified control/modulation is used to reduce leakage current. With all these methods, the goal is often maintaining a constant common-mode voltage across $\boldsymbol{C_{PV}}$ to suppress leakage current [113]-[117].

Adding a Common-mode filter and differential mode filter are other methods for suppressing leakage current [118]-[123]. The purpose of this method is to decrease the common-mode voltage caused in power inverters. With the decrease of common-mode voltage, the voltage deviation on $\boldsymbol{C_{PV}}$ is minimized to a suitable value.

Another method is changing structure of inverter and its $\boldsymbol{PWM}$ control system such as H5, H6, HERIC [124]-[126] structure of power inverter. They are widely used in multi-level power inverters. Creating an extra current path inside the inverter to maintain constant common-mode voltage for decreasing leakage current. More methods for suppressing leakage current in multi-level inverter are shown in reference [127]-[131].

## 2.8 Analysis leakage current in PV grid connected power inverter.

In this section, the analysis of leakage current from H-Bridge inverter will be described. **Figure 2-17** shows a PV grid connected power inverter with basic EMI filter. As mentioned earlier, leakage current is related to common-mode and differential-mode voltage in inverter, output filter and $\boldsymbol{C_{PV}}$.

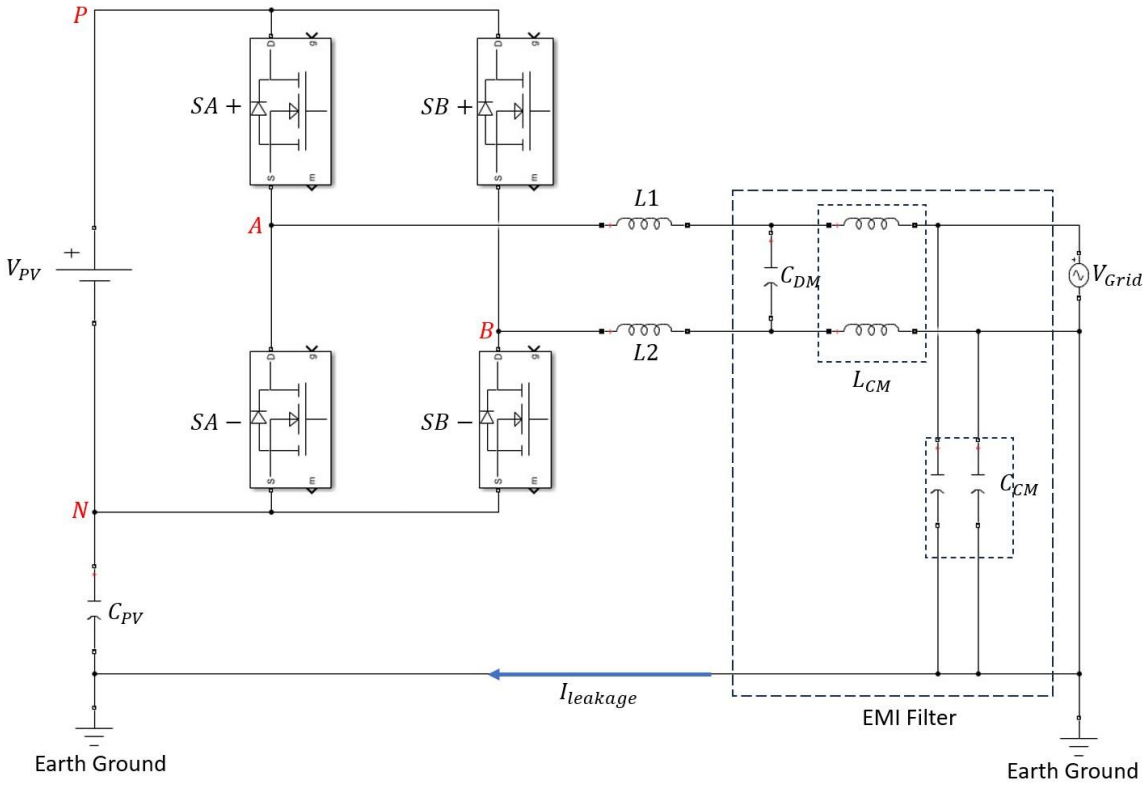


**Figure 2-17 : PV grid connected power inverter with EMI filter.**

In order to understand the relationship between the leakage current, common-mode voltage and differential-mode voltage, the circuit in **Figure 2-17** is transformed into an equivalent circuit which combines common-mode and differential-mode voltage. Firstly, the power inverter electrical circuit can be equivalent to the circuit consisting of two voltage sources $\boldsymbol{V_{AN}}$ and $\boldsymbol{V_{BN}}$ as shown in **Figure 2-18**. They are the output

voltage between two midpoints of inverter and DC voltage negative point N. As shown in **Figure 2-18**, there are three voltage sources in the circuit, $\boldsymbol{V_{AN}}$, $\boldsymbol{V_{BN}}$ and $\boldsymbol{V_{grid}}$. However, the frequency of grid voltage source is very low (50-60Hz) compared to frequency spectrum of $\boldsymbol{V_{AN}}$ and $\boldsymbol{V_{BN}}$ (10k-30MHz). During this calculation, the voltage across stray capacitor caused by grid is ignored.

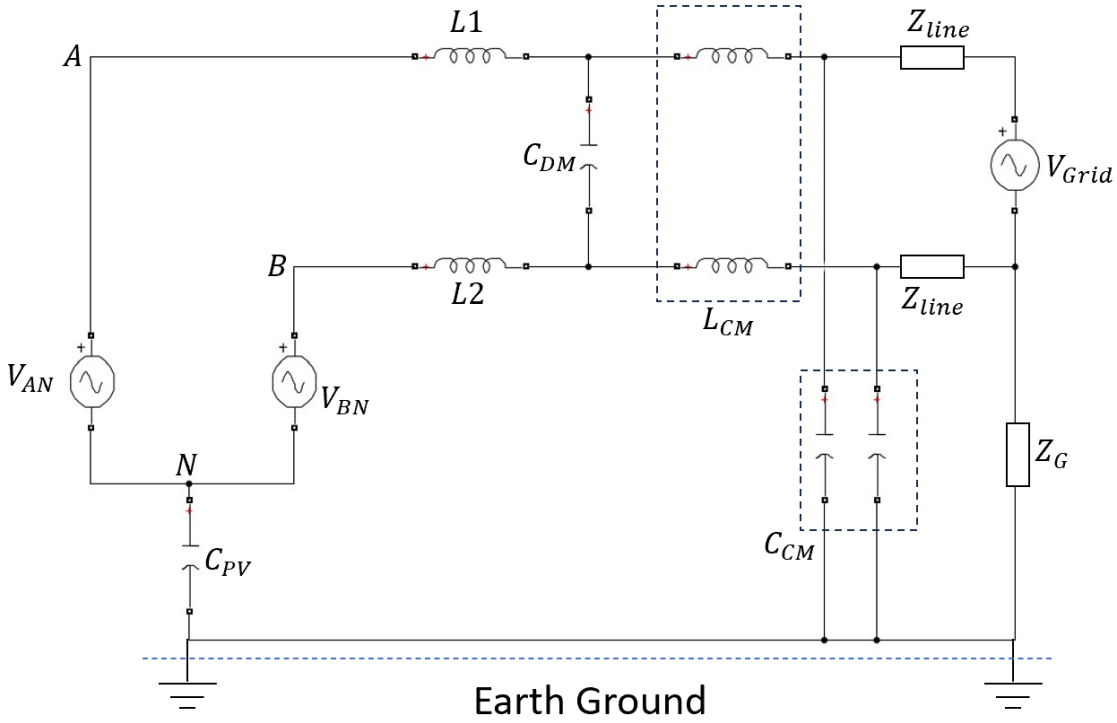


**Figure 2-18 : Equivalent circuit for $\boldsymbol{V_{AN}}$ and $\boldsymbol{V_{BN}}$.**

The equations below show the relationship between output $\boldsymbol{V_{AN}}$, $\boldsymbol{V_{BN}}$, common-mode voltage $\boldsymbol{V_{CM}}$ and differential-mode voltage $\boldsymbol{V_{DM}}$.

$$\boldsymbol{V_{CM}} = \frac{\boldsymbol{V_{AN}} + \boldsymbol{V_{BN}}}{\boldsymbol{2}} \tag{24}$$

$$\boldsymbol{V_{DM}} = \boldsymbol{V_{AN}} - \boldsymbol{V_{BN}} \tag{25}$$

$$\boldsymbol{V_{AN}} = \frac{\boldsymbol{V_{DM}}}{\boldsymbol{2}} + \boldsymbol{V_{CM}} \tag{26}$$

$$\boldsymbol{V_{BN}} = -\frac{\boldsymbol{V_{DM}}}{\boldsymbol{2}} + \boldsymbol{V_{CM}} \tag{27}$$

According to the equation above, the equivalent circuit in **Figure 2-18** can be further simplified which related to the $\boldsymbol{V_{CM}}$ and $\boldsymbol{V_{DM}}$, which is shown in **Figure 2-19**. $\boldsymbol{Z_{line}}$ and $\boldsymbol{Z_G}$ are the impedance in circuit line and impedance from grid to earth ground.

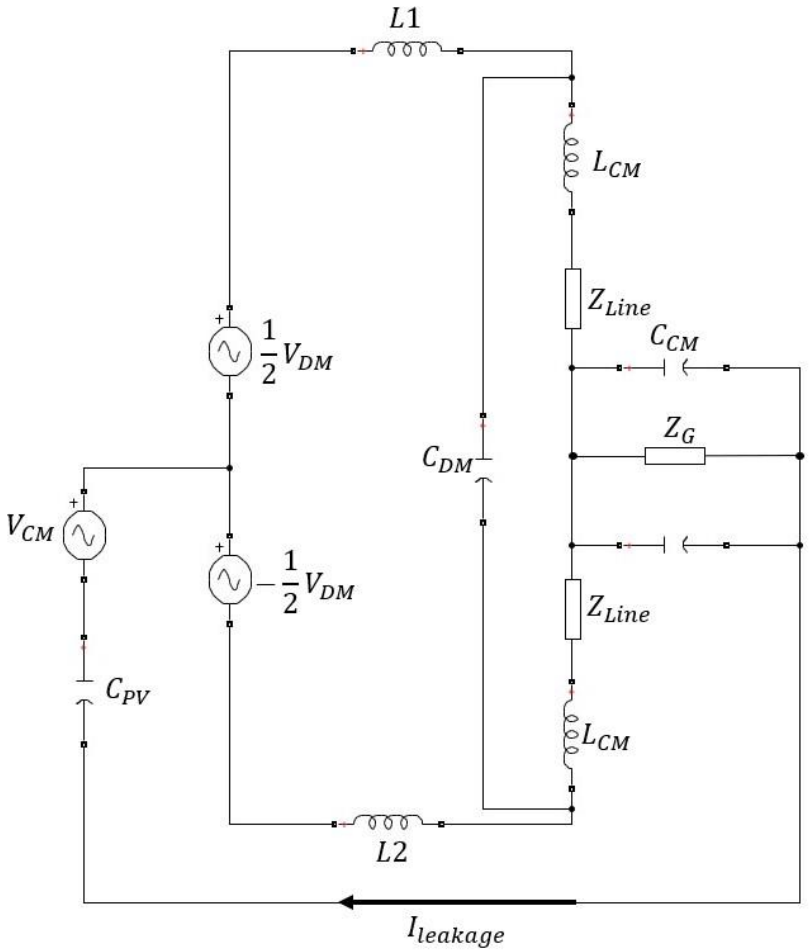


**Figure 2-19 : Equivalent circuit of PV power inverter in $\boldsymbol{V_{CM}}$ and $\boldsymbol{V_{DM}}$ mode.**

Now, only common-mode voltage and differential-mode voltage can be seen as the voltage source in inverter system. Using superposition and Norton's theorem, the circuit for $\boldsymbol{V_{CM}}$, $\boldsymbol{V_{DM}}$ and leakage current can be further equivalent which is shown in **Figure 2-20**.

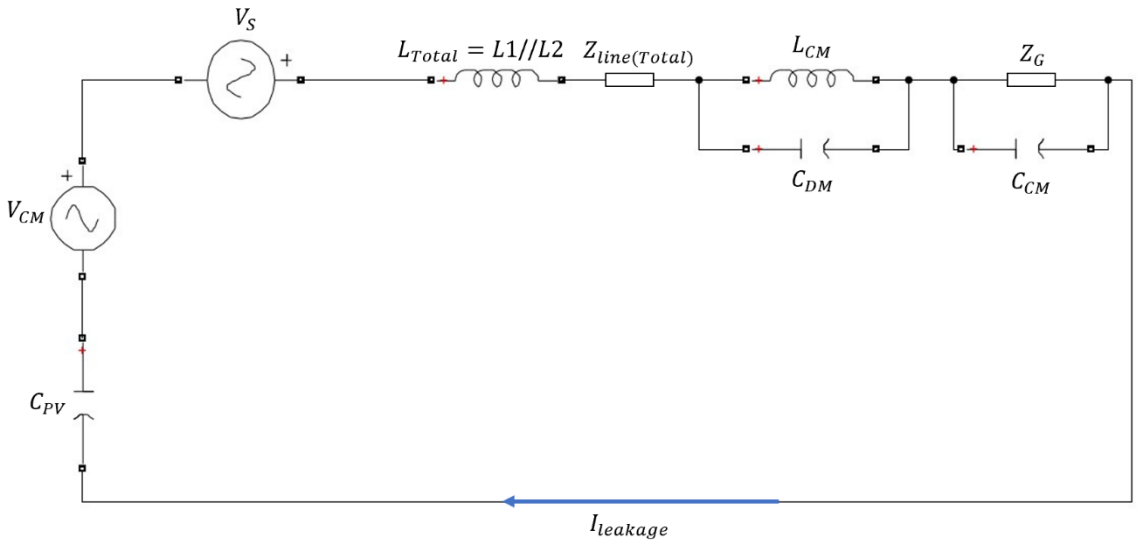


**Figure 2-20 : Final equivalent circuit for PV power inverter system.**

In the circuit shown in **Figure 2-20**, the $\boldsymbol{V_S}$ is the total equivalent voltage from differential-mode voltage and line inductor $\boldsymbol{L1}$ and $\boldsymbol{L2}$, it is shown in equation (28).

$$\mathbf{V_S} = \frac{\mathbf{V_{DM}}}{\mathbf{2}} * \frac{\mathbf{Z_{L2}} - \mathbf{Z_{L1}}}{\boldsymbol{Z_{L2}} + \mathbf{Z_{L1}}} \tag{28}$$

The $\boldsymbol{L_{Total}}$ and $\boldsymbol{Z_{line(Total)}}$ are the total inductance of $\boldsymbol{L1}$ and $\boldsymbol{L2}$ in parallel circuit, and total line impedance.

According to equation (28), the equivalent voltage $\boldsymbol{V_S}$ is related to the line inductor $\boldsymbol{L1}$,$\boldsymbol{L2}$ and $\boldsymbol{V_{DM}}$. There are two systems according to the line inductor, which are Symmetric system and Asymmetric system. **Table 2** below shows the relationship between switches sequence and common-mode voltage and differential-mode voltage.

**Table 2 : Output voltage of 2-level H-bridge inverter and switches sequence.**

| Switch Sequence | SA+ | SA- | $V_{AN}$ | $V_{BN}$ | $V_{DM}$ | $V_{CM}$ |
|---|---|---|---|---|---|---|
| ① | 0 | 0 | 0 | 0 | 0 | 0 |
| ② | 1 | 0 | $V_{PV}$ | 0 | $V_{PV}$ | $\frac{V_{PV}}{2}$ |
| ③ | 0 | 1 | 0 | $V_{PV}$ | $-V_{PV}$ | $\frac{V_{PV}}{2}$ |

**Table 3 : Total output voltage in Asymmetric system which $L1$=L and $L2$=0.**

| Switch Sequence | | SA+ | SA- | $V_{CM}$ | $V_S$ | $V_{total} = V_{CM} + V_S$ |
|---|---|---|---|---|---|---|
| ① | | 0 | 0 | 0 | 0 | 0 |
| ② | | 1 | 0 | $\frac{V_{PV}}{2}$ | $\approx -\frac{V_{PV}}{2}$ | $\approx 0$ |
| ③ | | 0 | 1 | $\frac{V_{PV}}{2}$ | $\approx \frac{V_{PV}}{2}$ | $\approx V_{PV}$ |

**Table 4 : Total output voltage in Symmetric system which $L1$=$L2$=$\frac{L}{2}$.**

| Switch Sequence | | SA+ | SA- | $V_{CM}$ | $V_S$ | $V_{total} = V_{CM} + V_S$ |
|---|---|---|---|---|---|---|
| ① | | 0 | 0 | 0 | 0 | 0 |
| ② | | 1 | 0 | $\frac{V_{PV}}{2}$ | 0 | $\frac{V_{PV}}{2}$ |
| ③ | | 0 | 1 | $\frac{V_{PV}}{2}$ | 0 | $\frac{V_{PV}}{2}$ |

**Table 3** shows the relationship between switch sequence and total voltage of $\boldsymbol{V_{CM}}$ and $\boldsymbol{V_{DM}}$ in Asymmetric system. In this system, only the $\boldsymbol{L1}$ is the line inductor. In this case, the $\boldsymbol{V_S}$ is equal to $\frac{V_{DM}}{2}$. In a 2-level H-Bridge inverter, the switch sequence only changes between sequence ② and ③. According to **Table 3**, the total voltage of $\boldsymbol{V_S}$ and $\boldsymbol{V_{CM}}$ are changed between 0 and $\boldsymbol{V_{PV}}$. If the voltage on stray capacitor $\boldsymbol{C_{PV}}$ is fluctuating, leakage current must flow. As result, in Asymmetric system, leakage current is high because of fluctuations of $\boldsymbol{V_S}$ and $\boldsymbol{V_{CM}}$.

$$\boldsymbol{I_{leakage} = C_{PV} * \frac{dV_{total}}{dt}} \tag{29}$$

In a Symmetric system, the line inductor is separated into two same value inductors $\boldsymbol{L1}$ and $\boldsymbol{L2}$. As shown in **Table 4**, because $\boldsymbol{L1 = L2}$, the $\boldsymbol{V_S}$ can be 0. Since the $\boldsymbol{V_{CM}}$ is kept

constant, there is no voltage fluctuation on the $\boldsymbol{C_{PV}}$, hence the leakage current should be 0.

On the other hand, if the system is 3-level H-Bridge inverter, in the Symmetric system, the switch sequence changes between ①, ② and ③. As result, the leakage current is caused by fluctuation of total voltage.

# 2.9 Chapter Conclusion

This chapter provides background information and literature review about H-Bridge inverter, $\boldsymbol{SPWM}$, Dead Time Compensation, $\boldsymbol{LCL}$ filter and close-loop control system. The analysis and calculation in H-Bridge and $\boldsymbol{SPWM}$ system is related to the analysis of dead time effect, the operation of DTC which will be presented in next chapter. In addition, it is also related to $\boldsymbol{LCL}$ filter and close-loop system design which is presented in Chapter 4.

# *Chapter 3*

## *Dead time and Dead time compensation*

This chapter describes the effect that dead time has on the inverter output waveform the distortion that causes in the voltage and current waveforms. Subsequently the chapter proposes a compensation scheme to mitigate the effects of dead time by modifying the pulse width modulator.

## 3.1 Dead time effect in 2-level H-Bridge inverter

The ideal operation of H-Bridge inverter with a resistive and inductive load was described in the previous chapter where it was assumed that the power electronic switching device (MOSFET or IGBT) changes its conduction state instantaneously and therefore the low-side device in a leg can be turned-on at the same time as the high-side device is turned off. In reality, it takes a finite time for the switching devices to change their conduction states and, therefore, it is necessary to turn off the conducting device before turning on the non-conducting device in the same leg. The resulting time delay between the device switching control signals (gate-source voltages) is known as the dead time ($\boldsymbol{T_d}$). The dead time is achieved by inserting a delay between the turn-off edge of $\boldsymbol{PWM1}$ (high-side) and the turn-on edge of $\overline{\boldsymbol{PWM1}}$. Considering leg $\boldsymbol{A}$, since during the dead time interval $\boldsymbol{SA+}$ nor $\boldsymbol{SA-}$ are in their off-state, then diode $\boldsymbol{DA+}$ or $\boldsymbol{DA-}$ must be conducted to maintain a path for the inductive inverter current. Which of the

diodes $DA+$ or $DA-$ is conducting depends on the direction of the inverter current $I_{AB}$ and this can cause the leg output voltage to change leading to distortion.

**Figure 3-1** shows inverter waveforms for $I_{AB} > 0$ for the duration of a $PWM$ cycle where the sinusoidal input voltage $V_{sin}(t)$ appears to be constant. $PWM1$ and $\overline{PWM1}$ are gate signal produced by comparing signal $V_{sin}(t)$ and $V_{tri}(t)$. The signal $SA \pm$ and $SB \pm$ are the actual gate signal of switches, which is the signal after adding turn on delay (dead time $T_d$). The $T_{pwm}$ is period time of one period of $V_{tri}(t)$. $\widehat{V}_{tri}$ is the peak voltage of signal $V_{tri}(t)$. The $e(t)$ is the difference voltage between $V_{sin}(t)$ and $V_{tri}(t)$, which can be calculated using,

$$e(t) = V_{sin}(t) - V_{tri}(t) \tag{30}$$

In the description which follows $t = t_0$ is the start of a $PWM$ period and this is denoted by the condition $V_{tri}(t_0) = -\widehat{V}_{tri}$ where $V_{tri}(t)$ is at its negative peak voltage. The voltage drop of the free-wheeling diode is equal to $V_{diode}$. The lowest two waveforms show the inverter output voltage $V_{AB}$ ($T_d = 0$) is the output voltage without dead time (ideal case) and $V_{AB}$ ($T_d > 0$) shows the output waveform with dead time. Since $I_{AB} > 0$, current flows from leg $A$ to leg $B$. During $t_0$ to $t_1$, $V_{sin}(t) > V_{tri}(t)$, $e(t) > 0$, and therefore switches $SA+$ and $SB-$ are on, $SA-$ and $SB+$ are off such that $V_{AB} = +V_{DC}$. At time $t_1$, $V_{sin}(t_1) < V_{tri}(t_1)$ and so switches $SA+$ and $SB-$ turns off and $SA-$ and $SB+$ remains off due to dead time $T_d = t_2 - t_1$. Since all switches are off, inductive action causes $DA-$ and $DB+$ to turn on to maintain a path for $I_{AB}$ to flow. With $DA-$ is conducting, $V_A = 0 - V_{diode}$ and with $DB+$ conducting $V_B = V_{DC} +$

$\boldsymbol{V_{diode}}$ and so $\boldsymbol{V_{AB} = -V_{DC} - 2 * V_{diode}}$. At the end of the dead time interval, $\boldsymbol{SA-}$ and $\boldsymbol{SB+}$ turn on, and the $\boldsymbol{I_{AB}}$ flows through two switches instead of two diodes, without voltage drop on diode, $\boldsymbol{V_{AB} = -V_{DC}}$. At time $\boldsymbol{t_3}$, $\boldsymbol{V_{sin}(t_3) > V_{tri}(t_3)}$, switches $\boldsymbol{SA-}$ and $\boldsymbol{SB+}$ turn off, while $\boldsymbol{SA+}$ and $\boldsymbol{SB-}$ remain off because of the dead time. The diodes $\boldsymbol{DA-}$ and $\boldsymbol{DB+}$ turn on again and $\boldsymbol{V_{AB} = -V_{DC} - 2 * V_{diode}}$. At time $\boldsymbol{t_4}$ the second dead time interval has elapsed and so $\boldsymbol{SA+}$ and $\boldsymbol{SB-}$ turn on, $\boldsymbol{V_{AB} = +V_{DC}}$, current $\boldsymbol{I_{AB}}$ is conducted by $\boldsymbol{SA+}$ and $\boldsymbol{SB-}$. After $\boldsymbol{t = t_0 + T_{pwm}}$, a new cycle starts again. As can be seen, the dead time has had the effect of lengthening the -$\boldsymbol{V_{DC}}$ duration time of $\boldsymbol{V_{AB}}$.

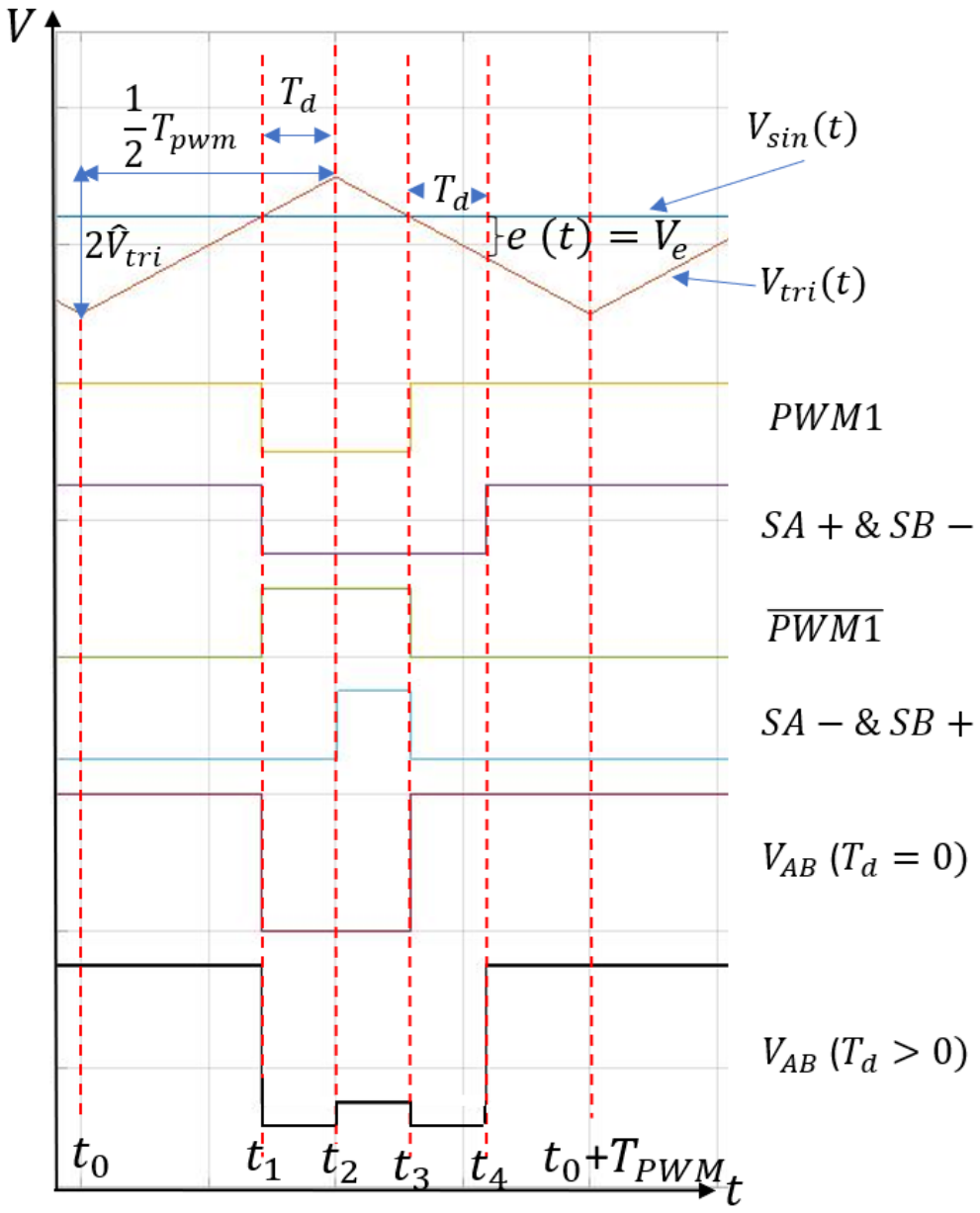


**Figure 3-1 : *PWM* signal, Gate Signal, Switch Signal and output $V_{AB}$ when $I_{AB} > 0$.**

**Figure 3-2** shows the inverter signals when the current direction is negative $\boldsymbol{I_{AB} < 0}$, i.e. current flow from leg $\boldsymbol{B}$ to leg $\boldsymbol{A}$. From $\boldsymbol{t_0}$ to $\boldsymbol{t_1}$, $\boldsymbol{V_{sin}(t) > V_{tri}(t)}$, $\boldsymbol{SA+}$ and $\boldsymbol{SB-}$ are on conducting $\boldsymbol{I_{AB}}$ and $\boldsymbol{V_{AB} = +V_{DC}}$. From $\boldsymbol{t_1}$ to $\boldsymbol{t_2 = t_1 + T_d}$, $\boldsymbol{SA+}$ and

$\boldsymbol{SB-}$ are off and $\boldsymbol{SA-}$ and $\boldsymbol{SB+}$ remain off due to the dead time. Inductive action turns on the diodes $\boldsymbol{DA+}$ and $\boldsymbol{DB-}$ to maintain a path for current to flow and so $\boldsymbol{V_{AB} = +V_{DC} + 2 * V_{diode}}$. From $\boldsymbol{t_2}$ to $\boldsymbol{t_3}$, $\boldsymbol{V_{sin}(t) < V_{tri}(t)}$, $\boldsymbol{SA-}$ and $\boldsymbol{SB+}$ are on, $\boldsymbol{V_{AB} = -VDC}$. Current $\boldsymbol{I_{AB}}$ is conducted by switches $\boldsymbol{SA-}$ and $\boldsymbol{SB+}$. From $\boldsymbol{t_3}$ to $\boldsymbol{t_4}$, $\boldsymbol{SA-}$ and $\boldsymbol{SB+}$ are off, while $\boldsymbol{SA+}$ and $\boldsymbol{SB-}$ remain off because of the dead time. $\boldsymbol{DA+}$ and $\boldsymbol{DB-}$ again conduct, and $\boldsymbol{V_{AB} = +V_{DC} + 2 * V_{diode}}$. At time $\boldsymbol{t_4}$, $\boldsymbol{SA+}$ and $\boldsymbol{SB-}$ turn on $\mathbf{V_{AB}} = \boldsymbol{+V_{DC}}$. The cycle completes at $\boldsymbol{t = t_0 + T_{pwm}}$. Dead time now has had the effect of lengthening $\boldsymbol{+V_{DC}}$ interval of the waveform.

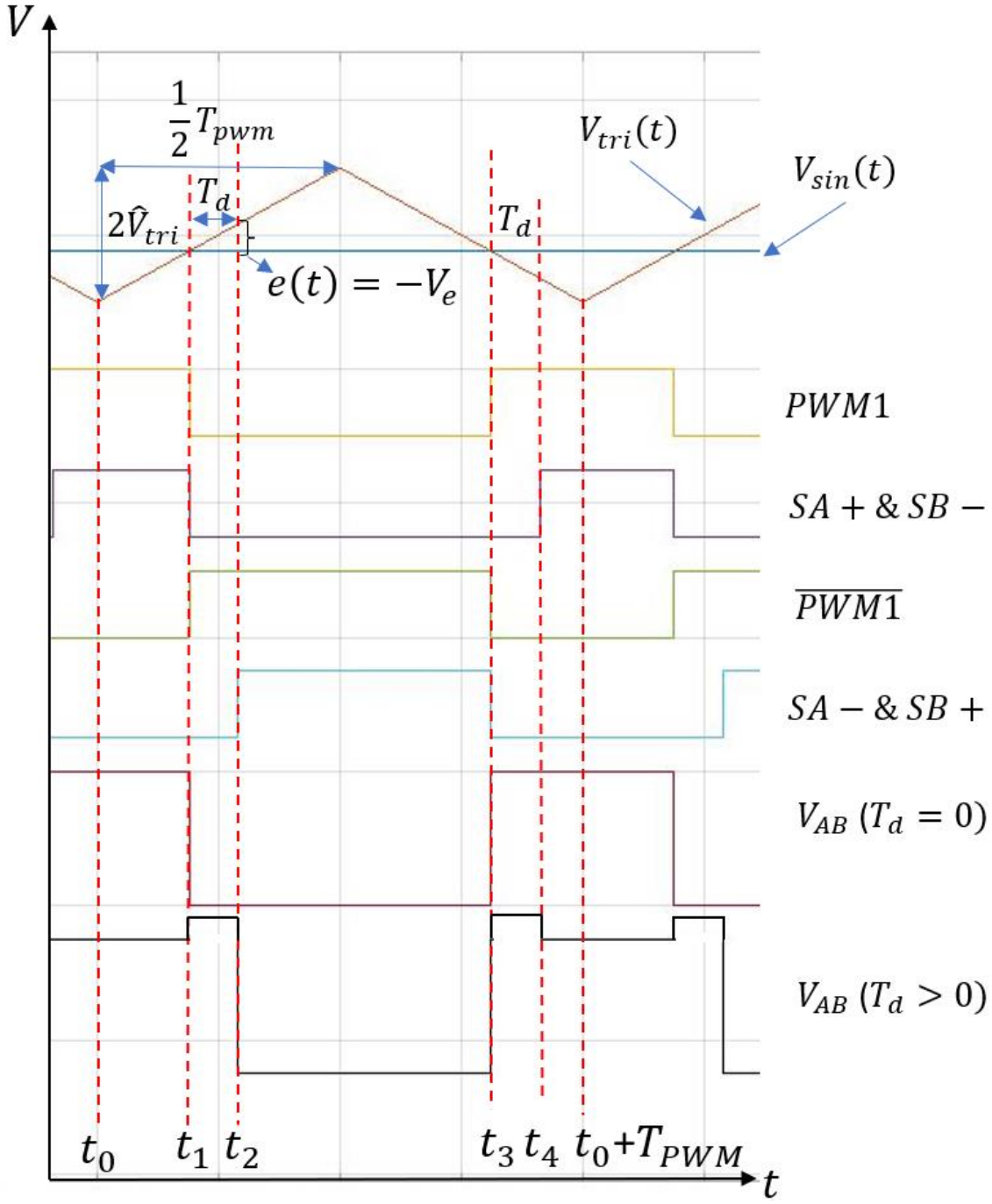


**Figure 3-2 : *PWM* signal, Gate Signal, Switch Signal and output $V_{AB}$ when $I_{AB} <$ 0.**

As shown in **Figure 3-1** and **Figure 3-2**, dead time affects the apparent duty ratio of the inverter output waveform dependent on the direction of the output current. The

effect on the duty ratio will be most apparent when the inverter current undergoes a zero crossing, and this leads to the current waveform being distorted.

## 3.2 Modelling and analysis of the deadtime process

This section develops a mathematical model for the deadtime effect. **Figure 3-3** (a) shows the model for zero dead time where $\boldsymbol{e(t) = V_{sin}(t) - V_{tri}(t)}$ is the PWM error signal which is quantified by the block labelled $\boldsymbol{V_{AB}}$ which represents the H-bridge. **Figure 3-3**(b) shows the with dead time model where the H-bridge is modelled using a hysteresis characteristic. With $\boldsymbol{I_{AB} > 0}$, the $\boldsymbol{V_{AB}}$ changes from $\boldsymbol{-V_{DC}}$ to $\boldsymbol{+V_{DC}}$ when $\boldsymbol{e(t) = V_e}$, and then changes from $\boldsymbol{V_{DC}}$ to $\boldsymbol{-V_{DC}}$ at $\boldsymbol{e(t) = 0}$. In **Figure 3-3** (c), during $\boldsymbol{I_{AB} < 0}$, $\boldsymbol{V_{AB}}$ changes from $\boldsymbol{-V_{DC}}$ to $\boldsymbol{+V_{DC}}$ when $\boldsymbol{e(t) = 0}$, and then changes from $\boldsymbol{V_{DC}}$ to $\boldsymbol{-V_{DC}}$ at $\boldsymbol{e(t) = -V_e}$. Voltage $\boldsymbol{V_e}$ is labelled on **Figure 3-1** and **Figure 3-2** is equivalent to the change in $\boldsymbol{V_{tri}(t)}$ over the dead time interval. Using the principles of similar triangles the ratio (gradient) of the triangle wave is $\frac{2\hat{V}_{tri}}{\frac{T_{pwm}}{2}} = \frac{V_e}{T_d}$.

$$\frac{\boldsymbol{V_e}}{\boldsymbol{T_d}} = \frac{\boldsymbol{2\hat{V}_{tri}}}{\frac{\boldsymbol{T_{pwm}}}{\boldsymbol{2}}} \Rightarrow \boldsymbol{V_e = 4f_{tri} * T_d * \hat{V}_{tri}} \tag{31}$$

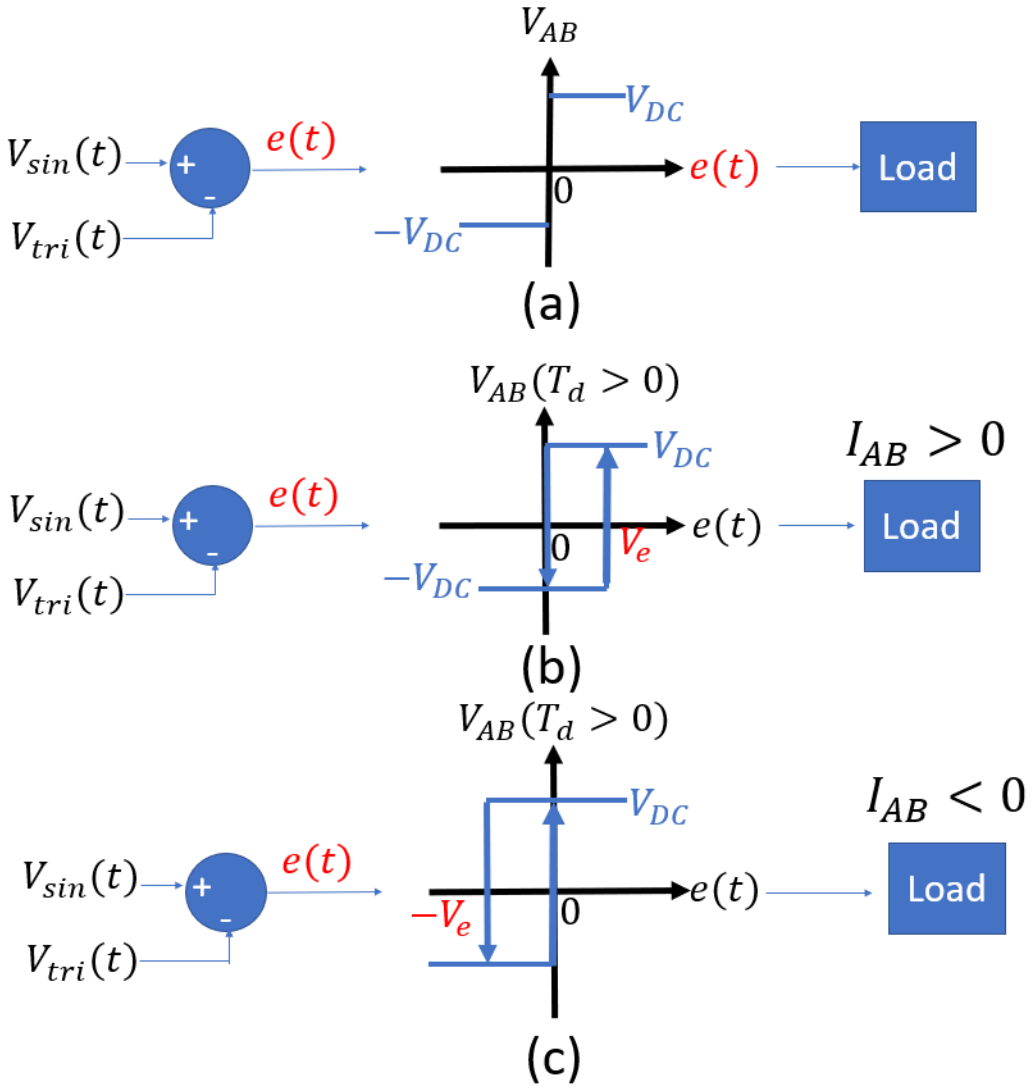


**Figure 3-3 : Relation between signal difference $e(t)$ and output voltage $V_{AB}$. (a) $T_d = 0$, (b) $T_d > 0$ and $I_{AB} > 0$, (c) $T_d > 0$ and $I_{AB} < 0$**

As shown in **Figure 3-1** and **Figure 3-2**, and according to equation (31), the proportion of a $PWM$ cycle taken by the dead time can be expressed as the duty ratio $D_{T_d}$ is,

$$D_{T_d} = \frac{T_d}{T_{PWM}} = \frac{V_e}{4\hat{V}_{tri}} \tag{32}$$

When the load current $I_{AB}(t) > 0$, the apparent duty cycle of $V_{AB}$ is reduced by $D_{T_d}$. $D_{AB} = D - D_{T_d}$. When the load current $I_{AB}(t) < 0$, the apparent duty cycle of $V_{AB}$ is

increased by $\boldsymbol{D_{T_d}}$. Therefore, the duty cycle for a $\boldsymbol{SPWM}$ waveform with dead time is given by.

$$\boldsymbol{D_{AB} = \frac{1}{2}[m_i + 1 - 2 * D_{Td} * sgn(I_{AB})]} \quad (33)$$

Consequently, the fundamental component of the $\boldsymbol{SPWM}$ waveform is given by,

$$\boldsymbol{V_{inv}(t) = V_{DC} * [m_i - 2 * D_{Td} * sgn(I_{AB})]} \quad (34)$$

The $\boldsymbol{sgn(I_{AB})}$ represents the current direction of $\boldsymbol{I_{AB}}$, $\boldsymbol{sgn(I_{AB}) = 1}$ when $\boldsymbol{I_{AB} > 0}$, while $\boldsymbol{sgn(I_{AB}) = -1}$ when $\boldsymbol{I_{AB} < 0}$.

Therefore, it can be seen that the dead time affects the amplitude of the fundamental and so, distorts the waveform. The effects become more pronounced at the waveform zero-crossing points where the contribution from the $\boldsymbol{D_{T_d}}$term is at its largest.

# 3.3 Dead Time Compensation of 2-level H-Bridge inverter

## 3.3.1 Deadtime Compensation ($\boldsymbol{DTC}$)

In order to reduce the effects of dead time, a correction signal is added to error signal prior to quantization to compensate for the signal delay caused by the dead time.

From the equation (12), the inverter modulation index is $\boldsymbol{m_i = \frac{V_{sin}(t)}{\widehat{V}_{tri}}}$, and substituting this into (34), the fundamental of the H-bridge voltage can be rewritten as,

$$\boldsymbol{V_{inv}(t) = V_{DC} * [\frac{\widehat{V}_{sin} * \sin(\omega_{sin} t) - \frac{1}{2} V_e * sgn(I_{AB})}{\widehat{V}_{tri}}]} \quad (35)$$

The term $\boldsymbol{\widehat{V}_{sin} * \sin(\omega_{sin} t)}$ is the original reference signal $\boldsymbol{V_{sin}(t)}$ and the term $\boldsymbol{-\frac{1}{2} V_e * sgn(I_{AB}) = V_{DT}}$ is due to the dead time. The effect of the dead time can be

reduced by adding a term to nullify $\boldsymbol{V_{DT}}$, $\boldsymbol{0 = V_{DT} + V_{DTC}}$ where $\boldsymbol{V_{DTC}}$ is the deadtime compensation voltage.

$$\boldsymbol{V_{DTC} = \frac{1}{2} V_e * sgn(I_{AB})} \tag{36}$$

**Figure 3-4** compares the output voltage without dead time ($\boldsymbol{T_d = 0}$), with dead time ($\boldsymbol{T_d > 0}$) and with deadtime compensation ($\boldsymbol{DTC}$) when $\boldsymbol{I_{AB}(t) > 0}$. With $\boldsymbol{DTC}$ the reference signal is $\boldsymbol{\frac{1}{2} V_e}$ greater than $\boldsymbol{V_{sin}(t)}$.

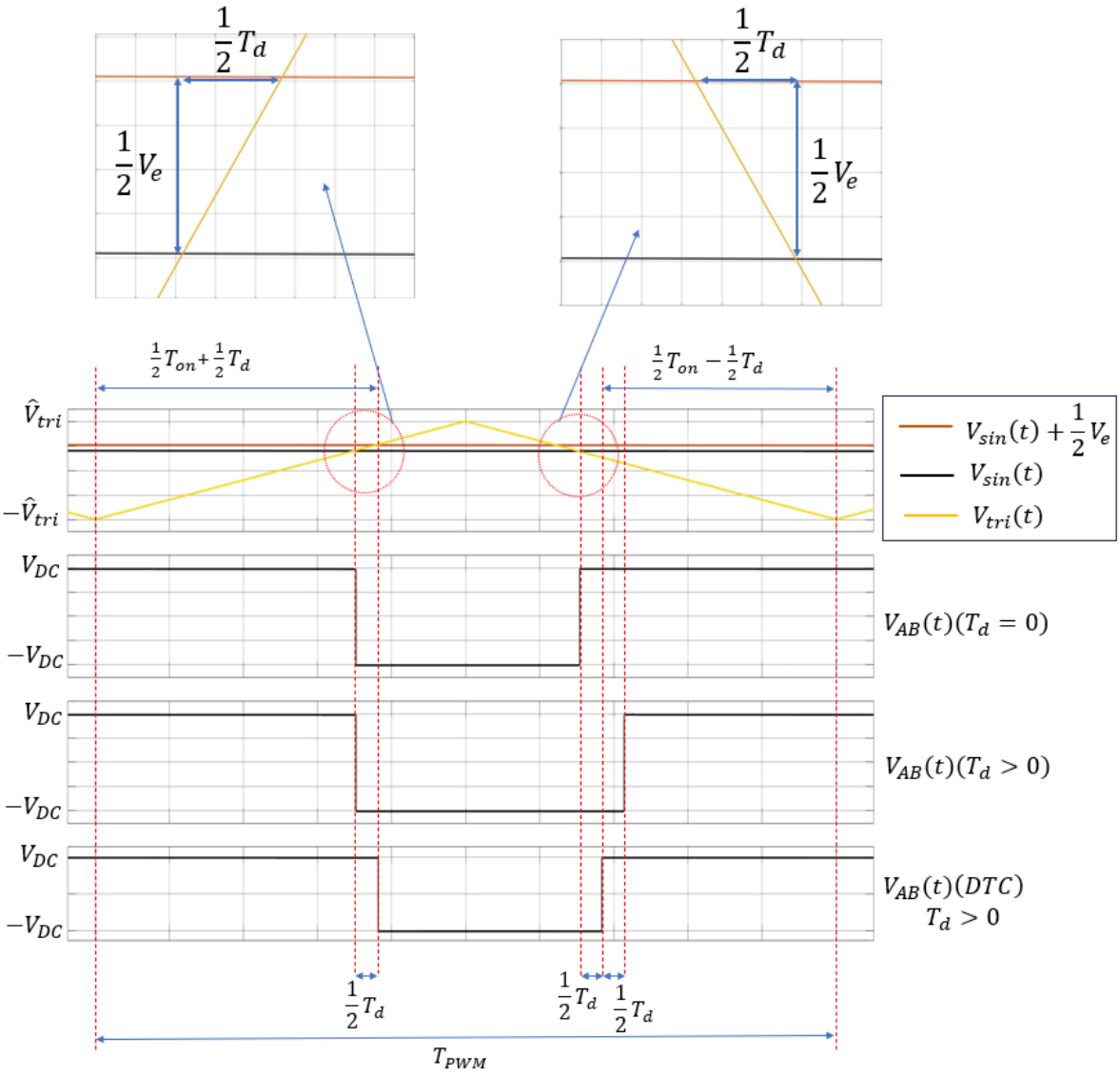


**Figure 3-4 : Deadtime compensation operation when $\boldsymbol{I_{AB} > 0}$.**

As shown in **Figure 3-4**, after adding the $\boldsymbol{V_{DTC}}$, the corrected waveform incurs a delay $\frac{1}{2}\boldsymbol{T_d}$ on its falling edge with respect to $\boldsymbol{T_d = 0}$. The corrected waveform also incurs a delay of $\frac{1}{2}\boldsymbol{T_d}$ on its rising edge. The net result is the deadtime compensation has delayed the waveform by $\frac{\boldsymbol{T_d}}{2}$ but had zero effect on its duty ratio.

When $\boldsymbol{I_{AB} < 0}$, the $\boldsymbol{V_{DT} = +\frac{1}{2}V_e}$, so the $\boldsymbol{V_{DTC}}$ should be $-\frac{1}{2}\boldsymbol{V_e}$. **Figure 3-5** shows the output voltage $\boldsymbol{V_{AB}(t)(DTC)}$ after adding the compensation voltage $\boldsymbol{V_{DTC}}$. Here, the compensated reference signal is $\frac{1}{2}\boldsymbol{V_e}$ below the original reference.

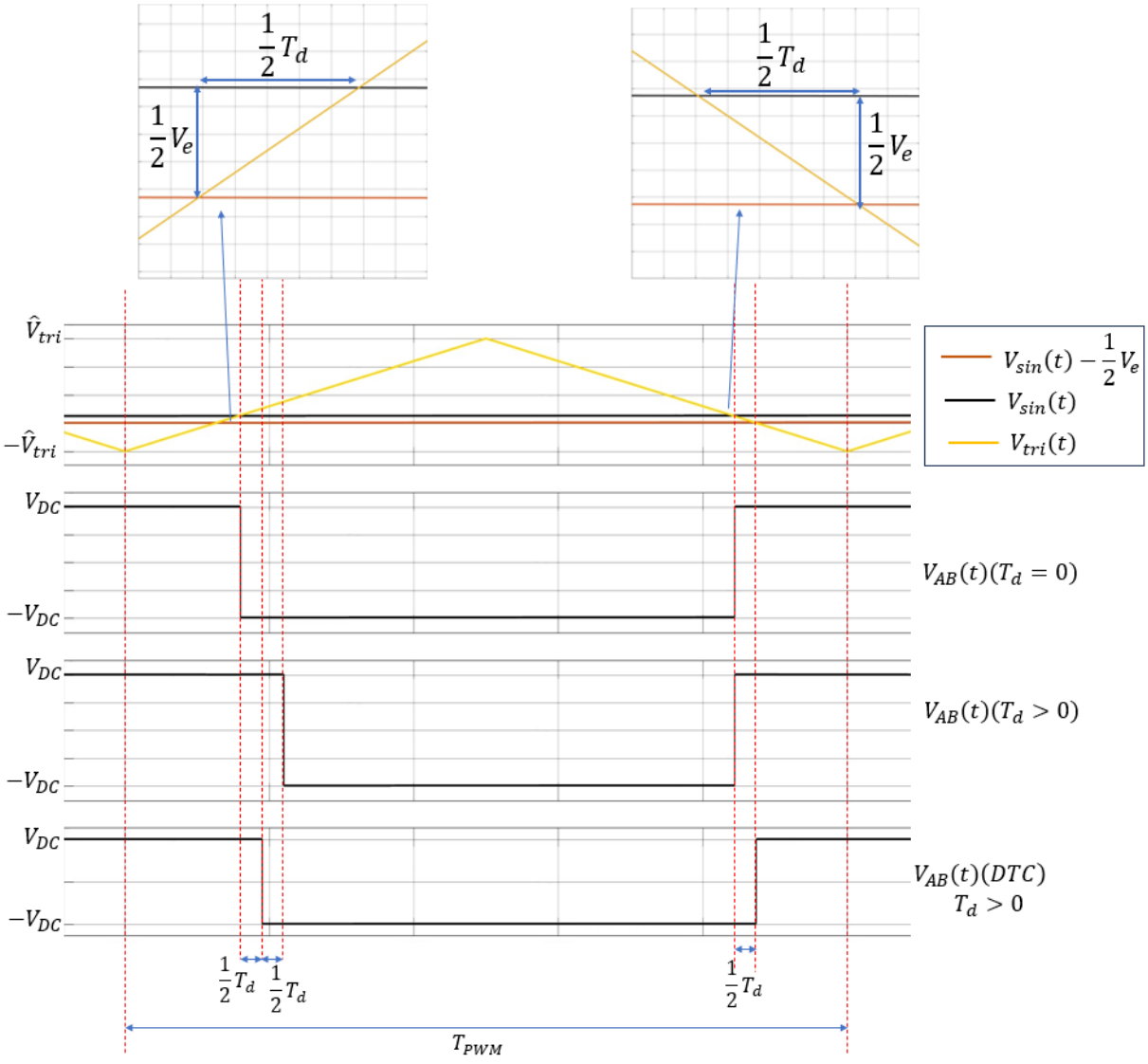


**Figure 3-5 : Deadtime compensation operation when $\boldsymbol{I_{AB} < 0}$.**

Similar to the previous case, the duty cycle is compensated, but the falling edge and rising edges are both delay by $\frac{1}{2}\boldsymbol{T_d}$.

**Figure 3-6** shows a block diagram represents the dead time and deadtime compensation processes.

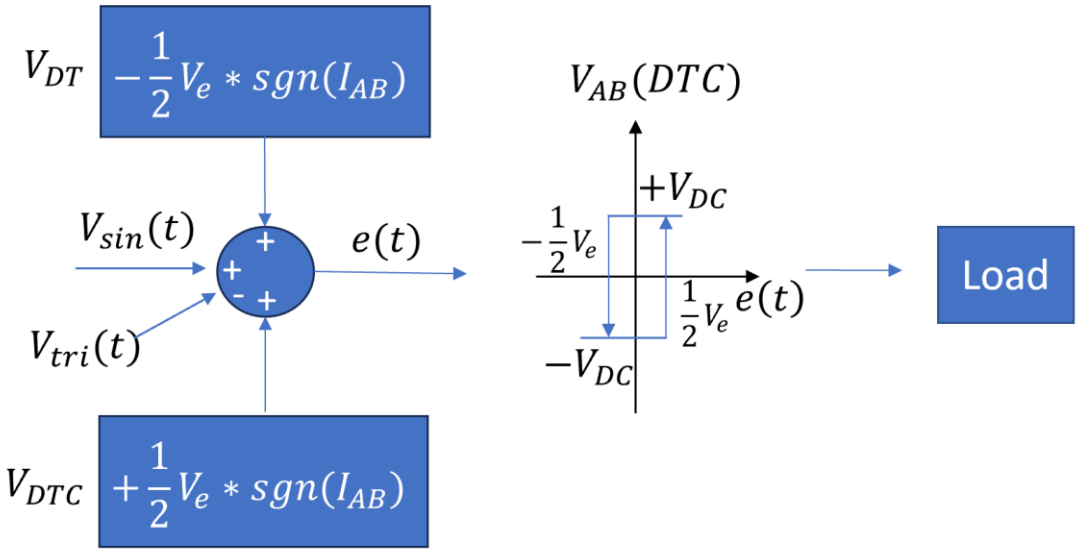


**Figure 3-6 : The block diagram of relationship between $\boldsymbol{e(t)}$ and $\boldsymbol{V_{AB}(DTC)}$ after adding $\boldsymbol{V_{DTC}}$.**

After adding $\boldsymbol{V_{DTC}}$ into ***SPWM*** system, the duty cycle and fundamental voltage in $\boldsymbol{V_{AB}(t)(DTC)}$ is same as that in $\boldsymbol{V_{AB}(t)(T_d = 0)}$, the dead time effect is compensated. But after comparing the relationship between $\boldsymbol{e(t)}$ and $\boldsymbol{V_{AB}(t)(T_d = 0)}$ from **Figure 3-3** (a) with relationship between $\boldsymbol{e(t)}$ and $\boldsymbol{V_{AB}(t)(DTC)}$ in **Figure 3-6**, it is clear to see that the whole waveform of $\boldsymbol{V_{AB}(t)(DTC)}$ is $\frac{1}{2}\boldsymbol{T_d}$ delay to $\boldsymbol{V_{AB}(t)(T_d = 0)}$. In conclusion, the $\boldsymbol{V_{DTC}}$ can solve the distortion of $\boldsymbol{V_{AB}(t)}$, compensate the duty cycle and fundamental voltage change from dead time effect, but a phase lag with $\frac{1}{2}\boldsymbol{T_d}$ will be remained.

## 3.3.2 Phase Lag Compensation ($PLC$)

To compensate the $\boldsymbol{DTC}$ induced phase lag, a phase lag compensation voltage $\boldsymbol{V_{PLC}}$ will be added into $\boldsymbol{SPWM}$ system. In reality, in electrical circuit, many factors will produce extra time delay into the system such as turn on/off delay inside chips, long circuit line etc. The phase lag compensation proposed here can help solve this kind of time delay $\boldsymbol{T_{delay}}$ and $\frac{1}{2}\boldsymbol{T_d}$ time delay together.

The phase lag compensation is related to the slope of $\boldsymbol{V_{tri}(t)}$. When $\frac{\mathbf{dV_{tri}(t)}}{\mathbf{dt}} > \mathbf{0}$ a voltage of $-\boldsymbol{V_{PLC}}$ is added into $\boldsymbol{V_{sin}(t)}$. When $\frac{\mathbf{dV_{tri}(t)}}{\mathbf{dt}} < \mathbf{0}$ a voltage $+\boldsymbol{V_{PLC}}$ is added into $\boldsymbol{V_{sin}(t)}$. **Figure 3-7** shows an example of how the phase lag compensation work.

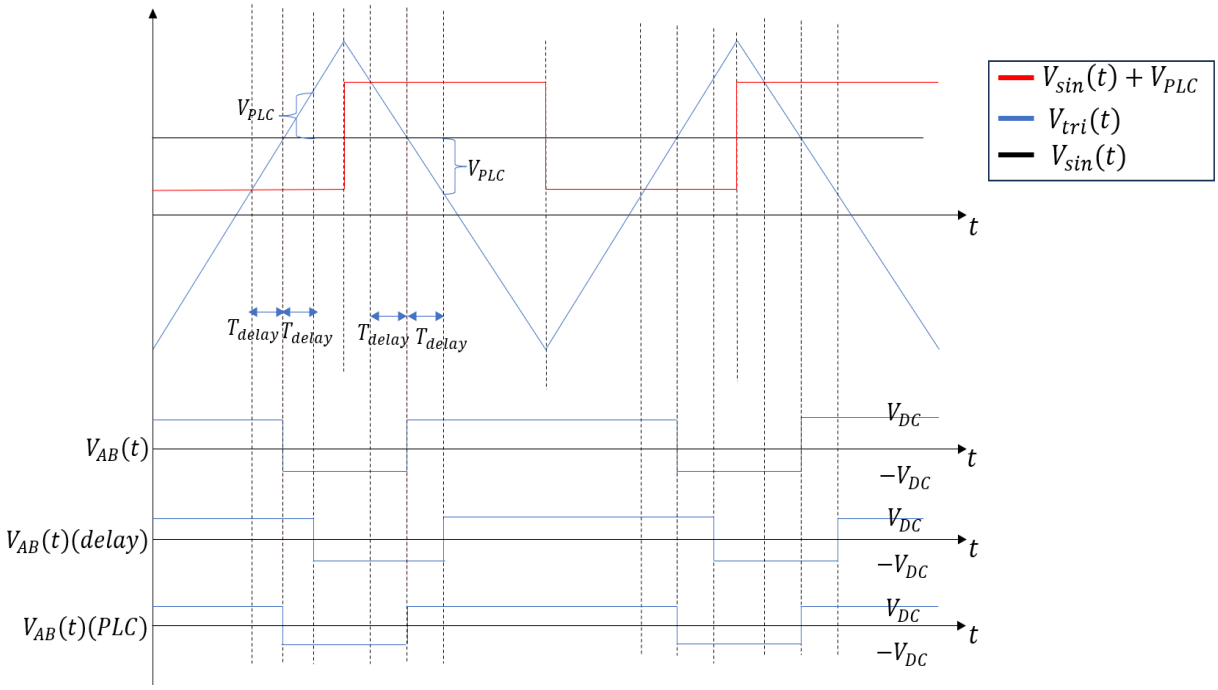


**Figure 3-7 : The example of phase lag compensation operation.**

To simplify the presentation of $\boldsymbol{PLC}$ scheme it has been assumed that dead time is zero. In **Figure 3-7**, it is clear to see that the delayed inverter waveform, $\boldsymbol{V_{AB}(t)(delay)}$, is delay from the reference waveform, $\boldsymbol{V_{AB}(t)}$, by time $\boldsymbol{T_{delay}}$. When $\boldsymbol{V_{tri}(t)}$ is

increasing, the load voltage transition from $+\boldsymbol{V_{DC}}$ to $-\boldsymbol{V_{DC}}$ must occur earlier and so, the $\boldsymbol{V_{sin}(t)}$ should be decreased by $\boldsymbol{V_{PLC}}$. When $\boldsymbol{V_{tri}(t)}$ is decreasing, the load voltage transition from $-\boldsymbol{V_{DC}}$ to $+\boldsymbol{V_{DC}}$ must occur earlier and so $\boldsymbol{V_{sin}(t)}$ should be increased by $\boldsymbol{V_{PLC}}$. **Figure 3-7** shows that after adding the $\boldsymbol{V_{PLC}}$ into $\boldsymbol{V_{sin}(t)}$, the phase lag corrected voltage waveform, $\boldsymbol{V_{AB}(t)(PLC)}$, is same to the ideal output voltage waveform $\boldsymbol{V_{AB}(t)}$. The calculation of value of $\boldsymbol{V_{PLC}}$ is similar to equation (31), the ratio of similar triangles. The equation of $\boldsymbol{V_{PLC}}$ is,

$$\boldsymbol{V_{PLC} = 4 * f_{pwm} * T_{delay} * \widehat{V}_{tri} * sgn(V_{tri})} \quad (37)$$

The $\boldsymbol{sgn(V_{tri})}$ represents the gradient of $\boldsymbol{V_{tri}(t)}$. $\boldsymbol{sgn(V_{tri}) = 1}$ if $\frac{\mathbf{dV_{tri}(t)}}{\mathbf{dt}} < \mathbf{0}$. $\boldsymbol{sgn(V_{tri}) = -1}$ if $\frac{\mathbf{dV_{tri}(t)}}{\mathbf{dt}} > \mathbf{0}$.

After adding the deadtime compensation value $\boldsymbol{V_{DTC}}$, the $\frac{1}{2}\boldsymbol{T_d}$ phase lag remained. So, the $\boldsymbol{T_{delay}} = \frac{1}{2}\boldsymbol{T_d}$, and $\boldsymbol{V_{PLC} = 2 * T_{delay} * \widehat{V}_{tri}} = \frac{1}{2}\boldsymbol{V_e}$. As result, when $\boldsymbol{V_{tri}(t)}$ is increasing, $-\frac{1}{2}\boldsymbol{V_e}$ is added into reference signal while $+\frac{1}{2}\boldsymbol{V_e}$ is added when $\boldsymbol{V_{tri}(t)}$ is decreasing.

**Figure 3-8** shows the output load voltage $\boldsymbol{V_{AB}(t)(DTC\&PLC)}$ after adding the $\boldsymbol{V_{DTC}}$ and $\boldsymbol{V_{PLC}}$ together. It is clear to see that the waveform of $\boldsymbol{V_{AB}(t)(DTC\&PLC)}$ is same as the ideal $\boldsymbol{V_{AB}(t)}$ waveform without $\boldsymbol{T_d}$. So, the $\frac{1}{2}\boldsymbol{T_d}$ phase lag is also solved. Focusing on the $\boldsymbol{e(t)}$ and $\boldsymbol{V_{AB}(t)(DTC\&PLC)}$, after adding deadtime compensation and phase lag compensation, the voltage level of $\boldsymbol{V_{AB}(t)(DTC\&PLC)}$ will be shifted once the $\boldsymbol{V_{sin}(t) > V_{tri}(t)}$ or $\boldsymbol{V_{sin}(t) < V_{tri}(t)}$.

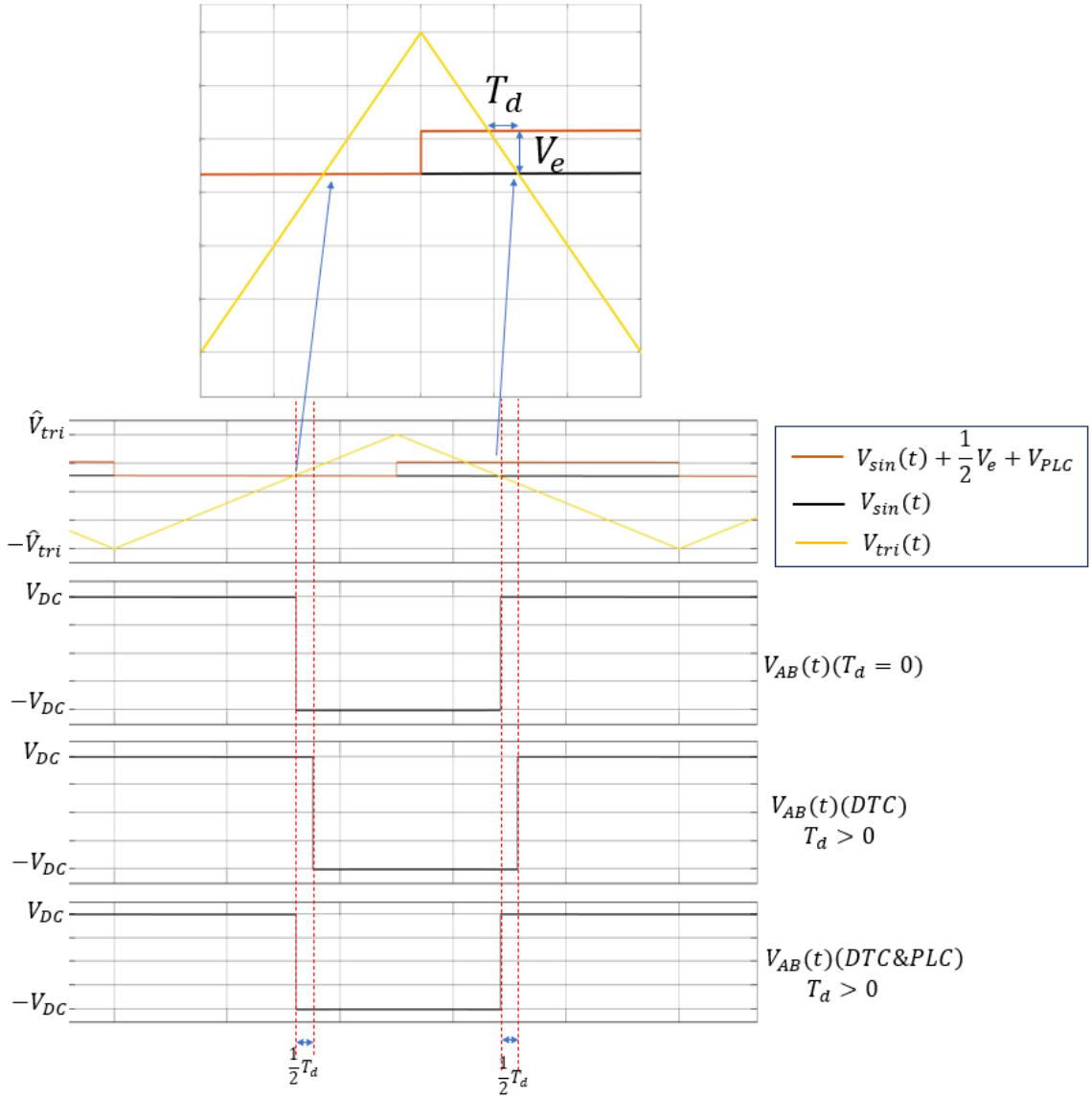


**Figure 3-8 : Deadtime compensation and phase lag compensation operation when $I_{AB}(t) > 0$.**

**Figure 3-9** shows the output load voltage $V_{AB}(t)(DTC\&PLC)$ after adding $V_{DTC}$ and $V_{PLC}$ when $I_{AB}(t) < 0$. Similar to the previous result, the voltage $V_{AB}(t)(DTC\&PLC)$ is same as the ideal $V_{AB}(t)$ when $T_d = 0$ after adding all compensation. Now, the relationship between $e(t)$ and voltage level change of $V_{AB}(t)(DTC\&PLC)$ is shown in **Figure 3-10**.

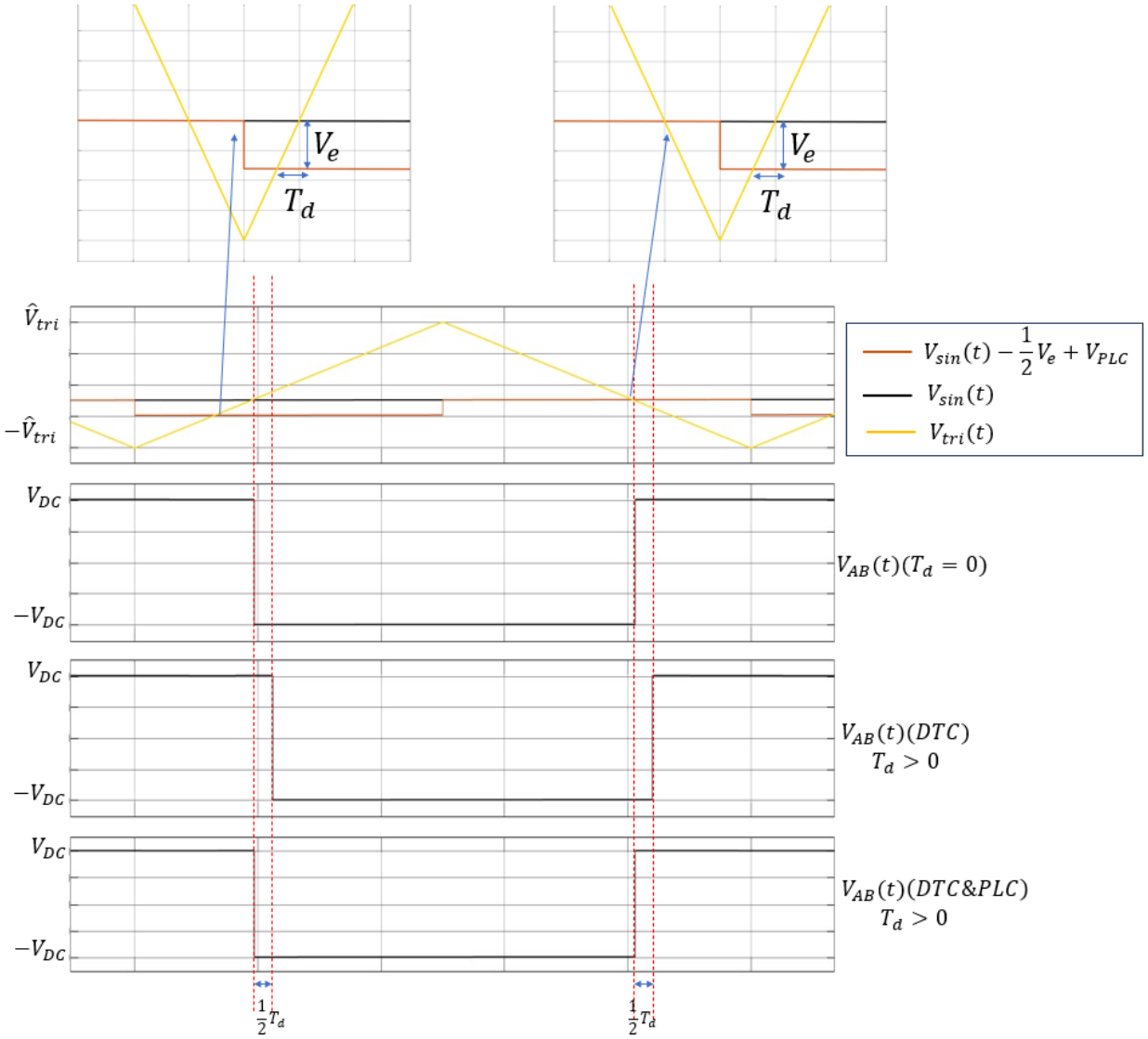


**Figure 3-9 : Deadtime compensation and phase lag compensation when $I_{AB}(t) < 0$.**

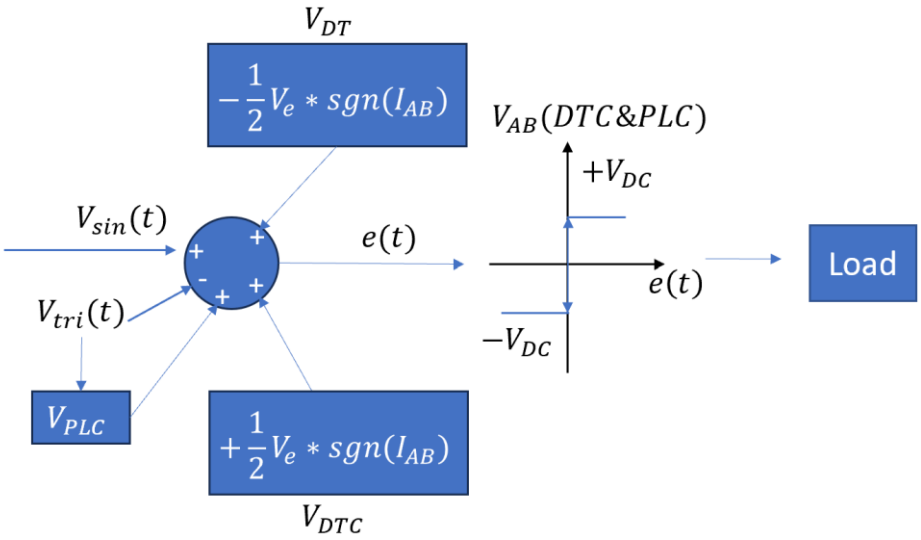


**Figure 3-10 : Relationship between $e(t)$ and $V_{AB}(DTC\&PLC)$** after adding $V_{DTC}$ and $V_{PLC}$.

The combined deadtime compensation and phase lag compensation pulse width modulator is shown in **Figure 3-11**.

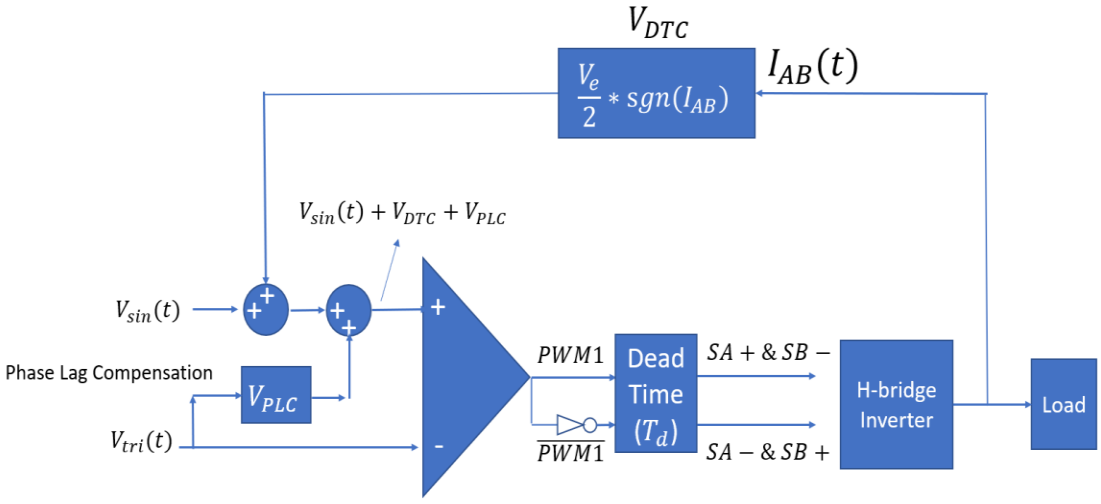


**Figure 3-11 : the block diagram of Dead Time Compensation.**

The new reference signal $V_{sin}(t) + \frac{1}{2} * V_e * sgn(I_{AB}) + V_{PLC}$ will be used to compare with carrier signal $V_{tri}(t)$. It is important to note that the purpose of dead time compensation is to compensate the change in duty cycle, fundamental voltage from load

voltage and phase lag caused by the $T_d$. The dead time $T_d$ remains in the H-Bridge system but its distorting effect has been mitigated to some extent.

## 3.4 MATLAB Simulation of the dead time compensation in 2-level H-Bridge inverter

**Figure 3-12** (a) shows the 2-level H-Bridge inverter and **Figure 3-12** (b) shows its ***SPWM*** control with $T_d$ in MATLAB/Simulink simulation.

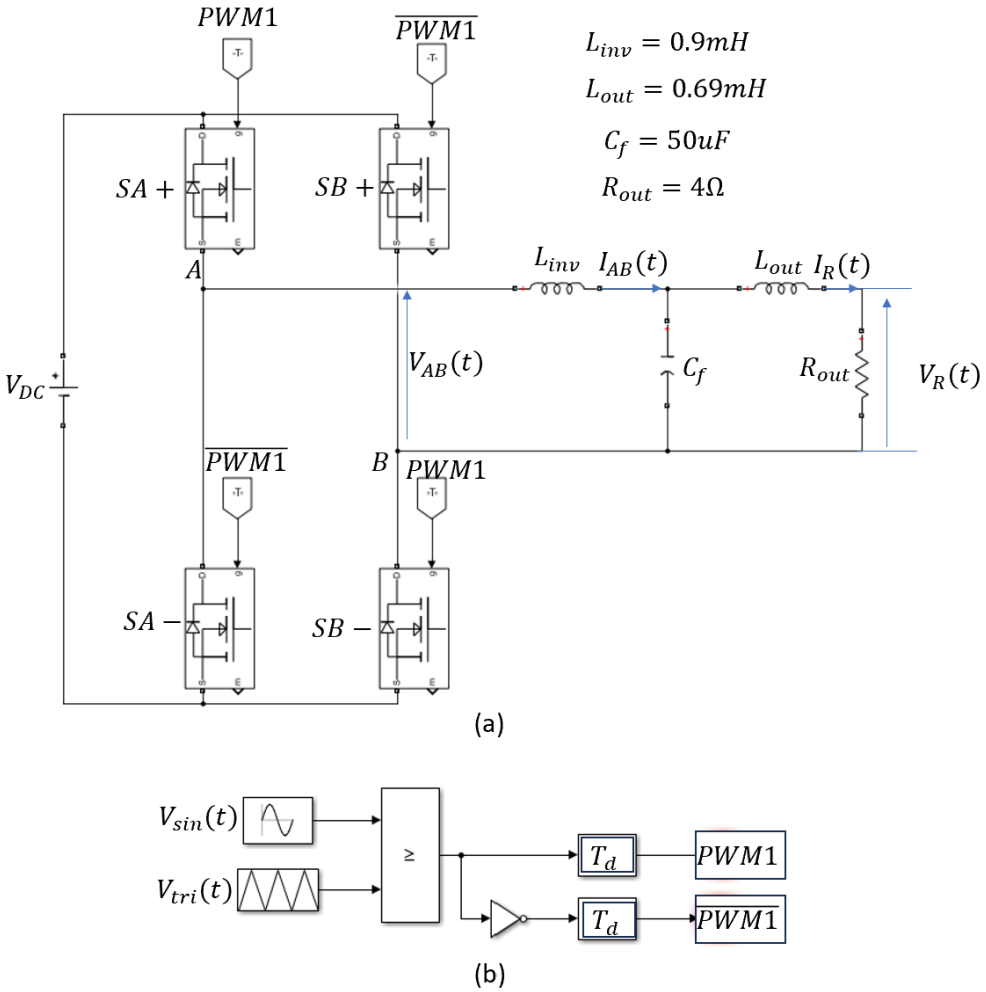


**Figure 3-12 : (a) MATLAB/Simulink 2-level H-Bridge inverter, (b) *SPWM* system.**

In this MATLAB/Simulink simulation, the inverter system drives a resistive load, $\boldsymbol{R_{out}}$. The parameters of all components are also shown in **Figure 3-12** (a). The $\boldsymbol{DC}$ voltage $\boldsymbol{V_{DC} = 100V}$. The sinusoidal reference voltage is $\boldsymbol{V_{sin}(t) = 0.65 * \sin(2\pi * 50 * t)}$ with a peak voltage $\boldsymbol{\hat{V}_{sin} = 0.65V}$ and a frequency $\boldsymbol{f_{sin} = 50\ \text{kHz}}$. The $\boldsymbol{PWM}$ carrier has a peak of $\boldsymbol{\hat{V}_{tri} = 1V}$ and a frequency $\boldsymbol{f_{tri} = 20kHz}$.

**Figure 3-13** shows the $\boldsymbol{DTC}$ and $\boldsymbol{PLC}$ in MATLAB simulation.

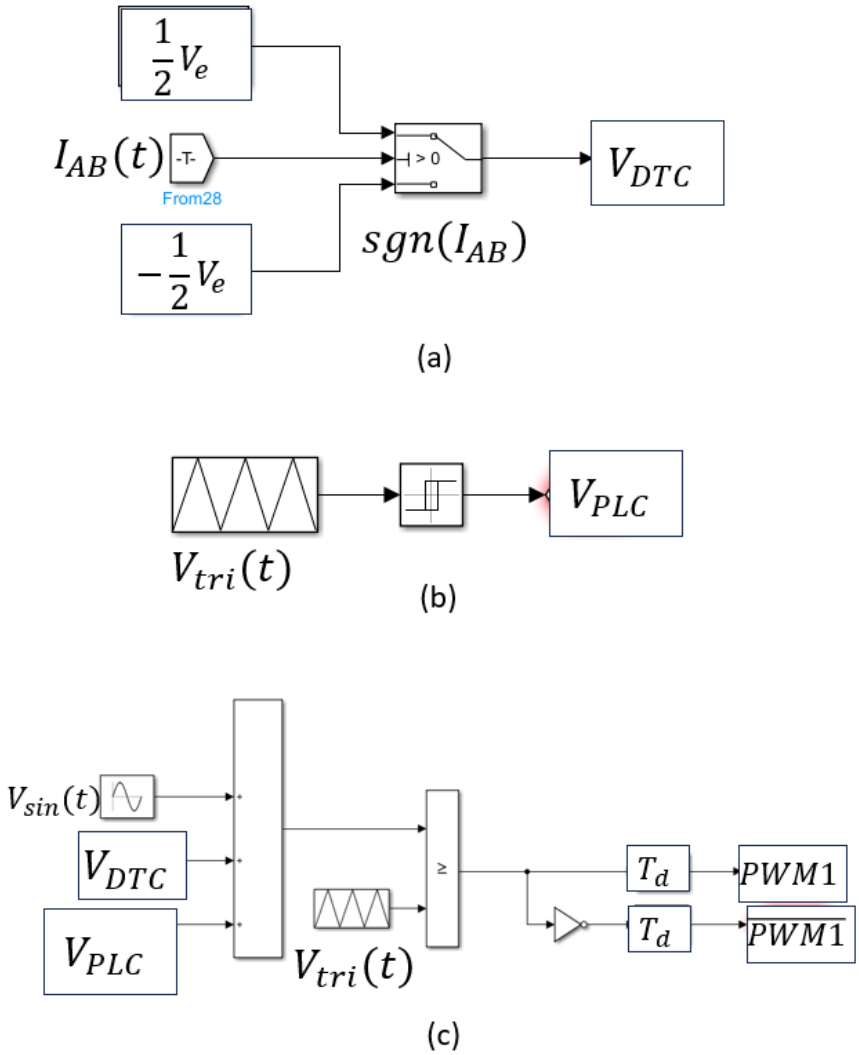


**Figure 3-13 : (a) $\boldsymbol{DTC}$ system, (b) $\boldsymbol{PLC}$, (c) $\boldsymbol{SPWM}$ with $\boldsymbol{DTC}$ and $\boldsymbol{PLC}$**

In **Figure 3-13** (a), the $\boldsymbol{DTC}$ is achieved by using a "Switch" function in MATLAB, if $\boldsymbol{I_{AB} > 0}$, $\boldsymbol{V_{DTC} = \frac{1}{2}V_e}$ while $\boldsymbol{I_{AB} < 0}$, $\boldsymbol{V_{DTC} = -\frac{1}{2}V_e}$. In **Figure 3-13** (b), the $\boldsymbol{PLC}$ is achieved by using a "Relay" function in MATLAB. It reads the gradient of $\boldsymbol{V_{tri}(t)}$. $\boldsymbol{V_{PLC} = -\frac{1}{2}V_e}$ when gradient of $\boldsymbol{V_{tri}(t)}$ is positive. While $\boldsymbol{V_{PLC} = \frac{1}{2}V_e}$ in opposite. **Figure 3-13** (c) shows the final $\boldsymbol{SPWM}$ system after adding $\boldsymbol{DTC}$ and $\boldsymbol{PLC}$ system. **Figure 3-14** shows the new reference signal waveform after adding the $\boldsymbol{V_{DTC}}$ and $\boldsymbol{V_{PLC}}$.

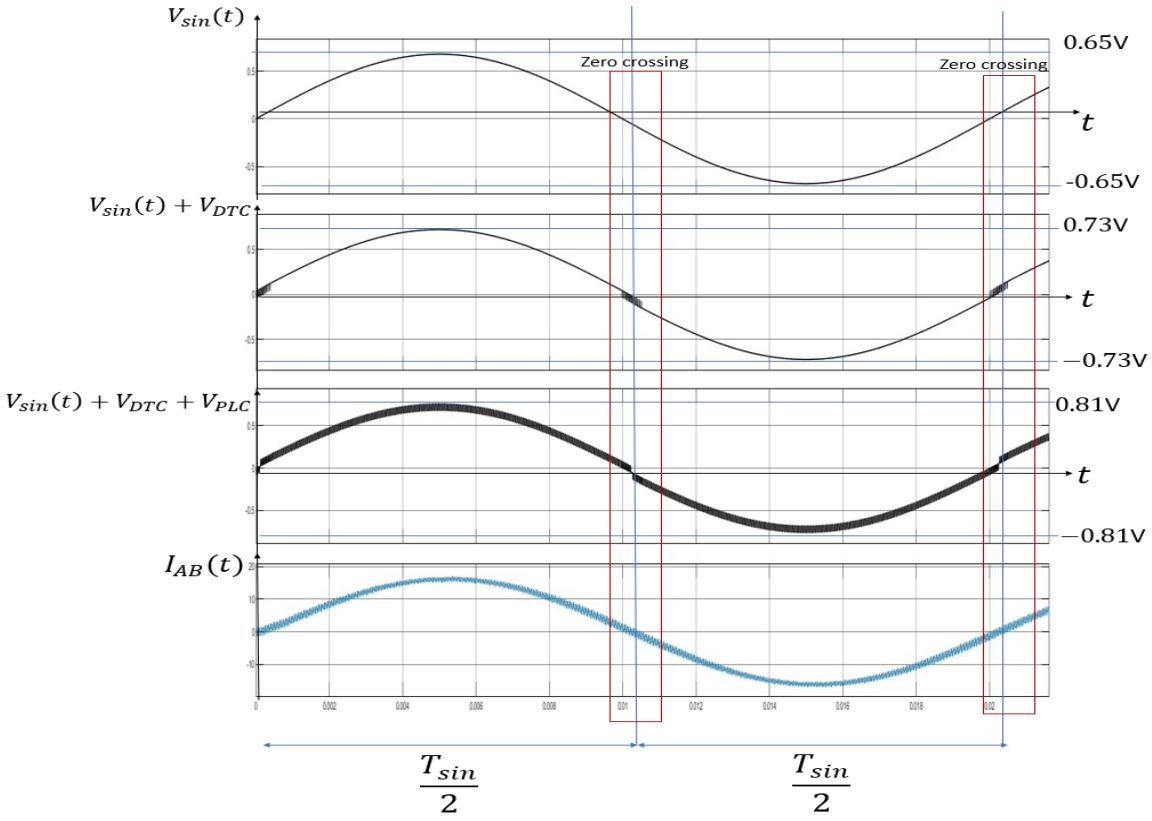


**Figure 3-14 : New modulation reference signal wave with $\boldsymbol{DTC}$ and $\boldsymbol{PLC}$.**

The dead time $\boldsymbol{T_d = 1us}$, hence the $\boldsymbol{V_{DTC} = V_{PLC} = \frac{1}{2}V_e = 0.08V}$. It is clear to see that the $\boldsymbol{V_{sin}(t)}$ is added $\boldsymbol{\frac{1}{2}V_e}$ when $\boldsymbol{I_{AB}(t)}$ at positive half cycle while is added $\boldsymbol{-\frac{1}{2}V_e}$ at negative half cycle of $\boldsymbol{I_{AB}(t)}$. During the zero crossing of $\boldsymbol{I_{AB}(t)}$, because the current fluctuates around zero, the $\boldsymbol{V_{DTC}}$ will changes between $\boldsymbol{\pm\frac{1}{2}V_e}$ in high frequency (switching frequency). The $\boldsymbol{V_{PLC}}$ is a pulse wave with high switching frequency $\boldsymbol{f_{pwm}}$.

Based on the $\boldsymbol{V_{sin}(t) + V_{DTC}}$ waveform, the high frequency $\boldsymbol{V_{PLC}}$ pulse waveform is added together and the final reference signal $\boldsymbol{V_{sin}(t) + V_{DTC} + V_{PLC}}$ is shown in **Figure 3-14**.

**Figure 3-15** shows the output voltage on resistor $\boldsymbol{R_{out}}$ under different dead time situations. As can be seen, the compensation schemes reduce the effects of dead time.

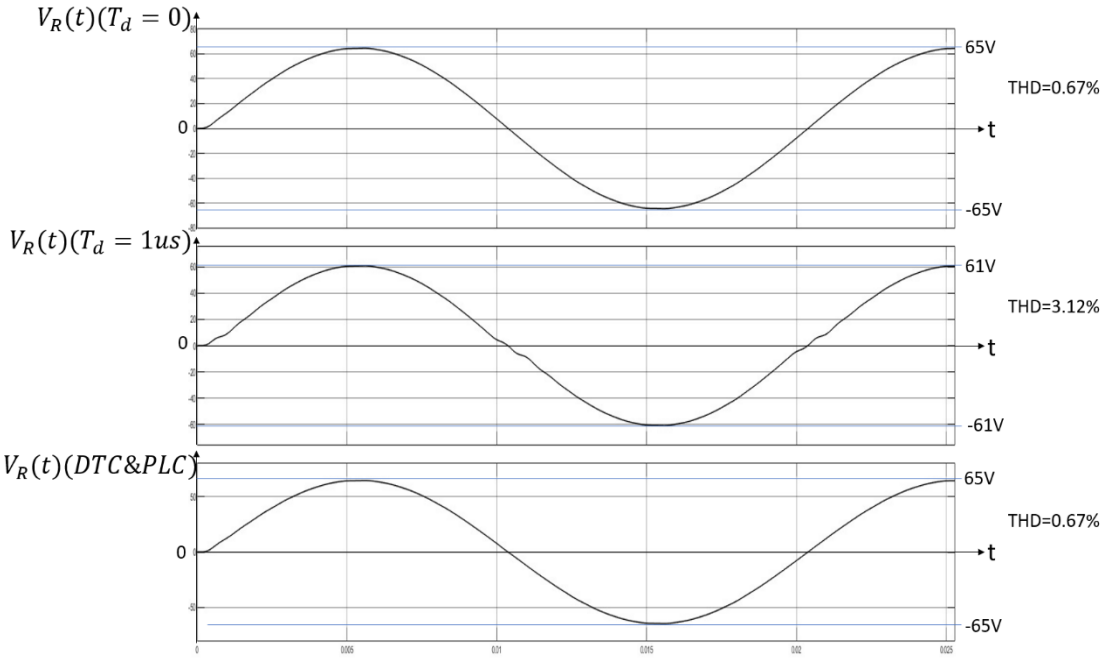


**Figure 3-15 : Output voltage $\boldsymbol{V_R(t)}$ with $\boldsymbol{T_d = 0}$, $\boldsymbol{T_d = 1us}$ and with compensation.**

In equation (34), it has proved that the voltage reduction caused by the dead time effect is equal to $\boldsymbol{V_{DC} * \left[\frac{1}{2} * \frac{V_e}{\hat{V}_{tri}}\right] = 4V}$. As shown in **Figure 3-15**, when $\boldsymbol{\sin(\omega_{sin} t) = 1}$, the $\boldsymbol{V_R(t)}$ reaches to the positive peak voltage which is equal to $\boldsymbol{V_{DC} * m_i = 65V}$ when $\boldsymbol{T_d = 0}$. After adding $\boldsymbol{1us}$ dead time, the voltage decreases $\boldsymbol{4V}$, as result, the positive peak voltage of $\boldsymbol{V_R(t)}$ is decreased from $\boldsymbol{65V}$ to $\boldsymbol{61V}$. In addition, it is clear to see that

there is a serious distortion cause by the dead time during the zero crossing. After the compensation system is added into $\boldsymbol{SPWM}$ system, the voltage reduction is recovered, $\widehat{\boldsymbol{V}}_{\boldsymbol{R}}$ changes back from $\boldsymbol{61V}$ to $\boldsymbol{65V}$. And the distortion during zero crossing is compensated. It is clear to see that from $\boldsymbol{THD}$ value, the $\boldsymbol{THD}$ in $\boldsymbol{V_R(t)}$ is 0.67% when $\boldsymbol{T_d = 0}$, then increases to 3.12% because of $\boldsymbol{T_d}$. However, with the $\boldsymbol{DTC}$ and $\boldsymbol{PLC}$, the distortion is compensated, $\boldsymbol{THD}$ is decreased back to 0.67% which equal to the $\boldsymbol{THD}$ in ideal H-Bridge system.

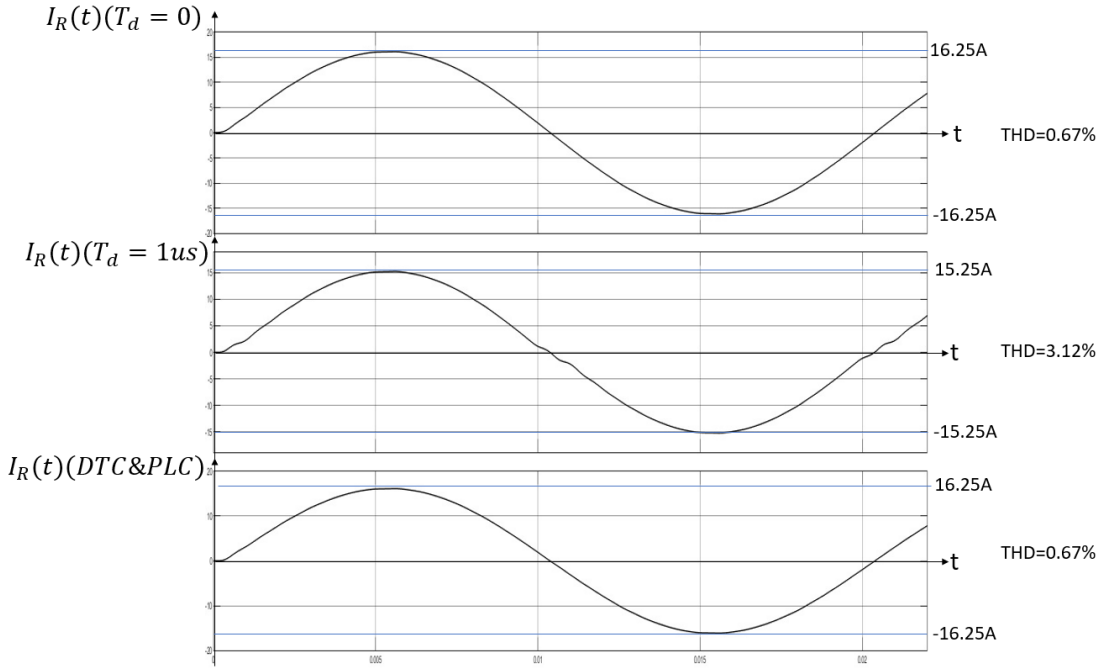


**Figure 3-16 : Output current $\boldsymbol{I_R(t)}$ with $\boldsymbol{T_d = 0}$, $\boldsymbol{T_d = 1us}$ and with compensation.**

**Figure 3-16** shows the output current through $\boldsymbol{R_{out}}$ ($\boldsymbol{I_R(t)}$). $\boldsymbol{I_R(t) = \frac{V_R(t)}{R_{out}}}$, so, the peak current $\widehat{\boldsymbol{I}}_{\boldsymbol{R}}$ is equal to $\boldsymbol{16.25A}$ when $\boldsymbol{\sin(\omega_{sin}t) = 1}$ and $\boldsymbol{T_d = 0}$. With $\boldsymbol{T_d = 1us}$, the $\widehat{\boldsymbol{I}}_{\boldsymbol{R}}$ is decreased to $15.25\boldsymbol{A}$. After adding compensation, the $\widehat{\boldsymbol{I}}_{\boldsymbol{R}}$ changes back to $\boldsymbol{16.25A}$.

It is clear to see that the distortion is solved during zero crossing, and $\boldsymbol{THD}$ is decreased as well.

**Figure 3-17** shows the $\boldsymbol{V_R(t)}$ when $\boldsymbol{T_d = 2us}$ and $\boldsymbol{T_d = 3us}$ and after compensation. It is clear to see that the peak voltage $\boldsymbol{\hat{V}_R}$ is decreased more with the increase of $\boldsymbol{T_d}$. And $\boldsymbol{THD}$ is higher with the increase of $\boldsymbol{T_d}$. However, after adding the dead time compensation, the decrease of $\boldsymbol{\hat{V}_R}$ can be compensated, and $\boldsymbol{THD}$ is decreased to the ideal value in system without $\boldsymbol{T_d}$.

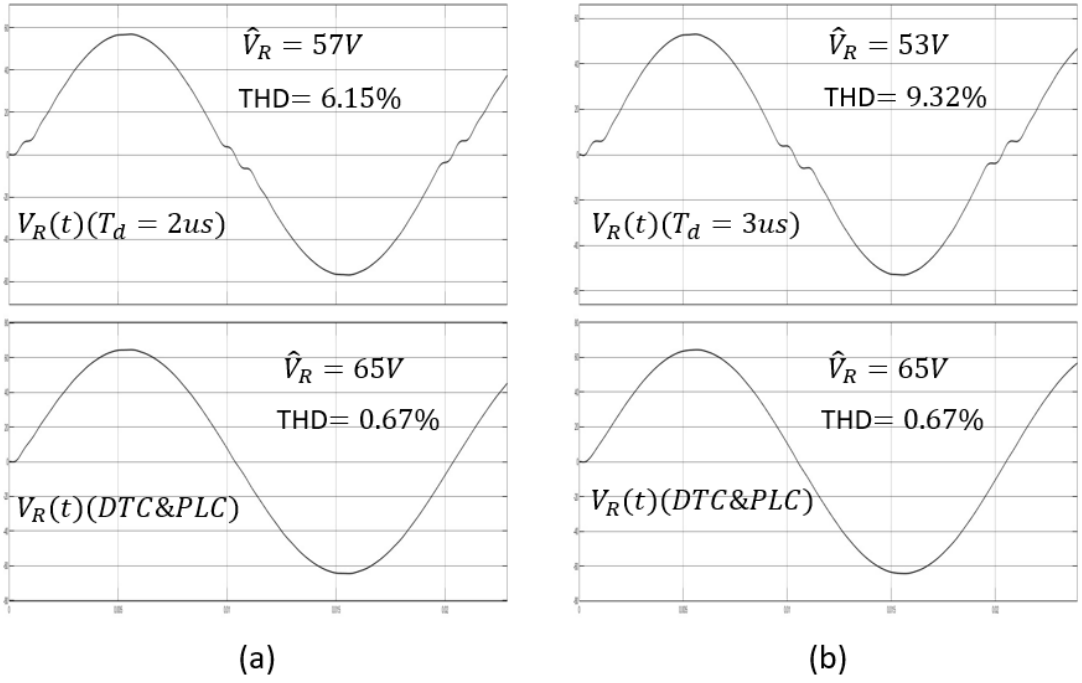


**Figure 3-17 : Output voltage $\boldsymbol{V_R(t)}$. (a) $\boldsymbol{T_d = 2us}$, (b) $\boldsymbol{T_d = 3us}$**

As shown in the MATLAB simulation result, the dead time compensation is suitable for different $\boldsymbol{T_d}$ in $\boldsymbol{SPWM}$ system. The value of $\boldsymbol{V_{DTC}}$ and $\boldsymbol{V_{PLC}}$ are the key points in this compensation method, and they can be calculated easily since they are only related to the $\boldsymbol{f_{pwm}}$, $\boldsymbol{\hat{V}_{tri}}$ and $\boldsymbol{T_d}$ which shown in equation (31) and (37).

## 3.5 Dead Time effect analysis in 3-level H-Bridge inverter

In this section, the Dead Time effect in a 3-level H-Bridge inverter will be described. In previous section 2.3, the structure and $\boldsymbol{SPWM}$ system of a 3-level H-Bridge inverter has been described. The electrical circuit structure of 2-level and 3-level H-Bridge are same. But the power switches in leg $\boldsymbol{A}$ and leg $\boldsymbol{B}$ are controlled separately by two $\boldsymbol{SPWM}$ signals $\boldsymbol{PWM1}$ and $\boldsymbol{PWM2}$. In 3-level H-Bridge inverter, dead time effect is still analysed according to the current direction of $\boldsymbol{I_{AB}(t)}$. As a 3-level H-Bridge inverter, the voltage range of $\boldsymbol{V_{AB}(t)}$ is related to the $\boldsymbol{V_{sin}(t)}$. $\boldsymbol{V_{AB}}$ changes between $\boldsymbol{0V}$ and $+\boldsymbol{V_{DC}}$ during the positive half period of $\boldsymbol{V_{sin}(t)}$. On the other hand, $\boldsymbol{V_{AB}}$ changes between $\boldsymbol{0V}$ and $-\boldsymbol{V_{DC}}$ during negative half period of $\boldsymbol{V_{sin}(t)}$. As result, in this section, the dead time effect on 3-level H-Bridge inverter will be analysed in two parts according to the direction of $\boldsymbol{V_{sin}(t)}$ and $\boldsymbol{I_{AB}(t)}$.

### 3.5.1 Dead Time effect at positive half period of $\boldsymbol{V_{sin}(t)}$

During the positive half period of $\boldsymbol{V_{sin}(t)}$ time, $\boldsymbol{V_{sin}(t)}$ is always larger than $\boldsymbol{V_{tri2}(t)}$, the $\boldsymbol{SB+}$ is always off and $\boldsymbol{SB-}$ is always on. As result, only switch status of $\boldsymbol{SA+}$ and $\boldsymbol{SA-}$ decides the output voltage $\boldsymbol{V_{AB}}$. **Figure 3-18** shows the relation between $\boldsymbol{V_{sin}(t)}$, $\boldsymbol{V_{tri1}(t)}$, switch status of leg A power switches and output voltage $\boldsymbol{V_{AB}}$ during the positive half period of $\boldsymbol{V_{sin}(t)}$.

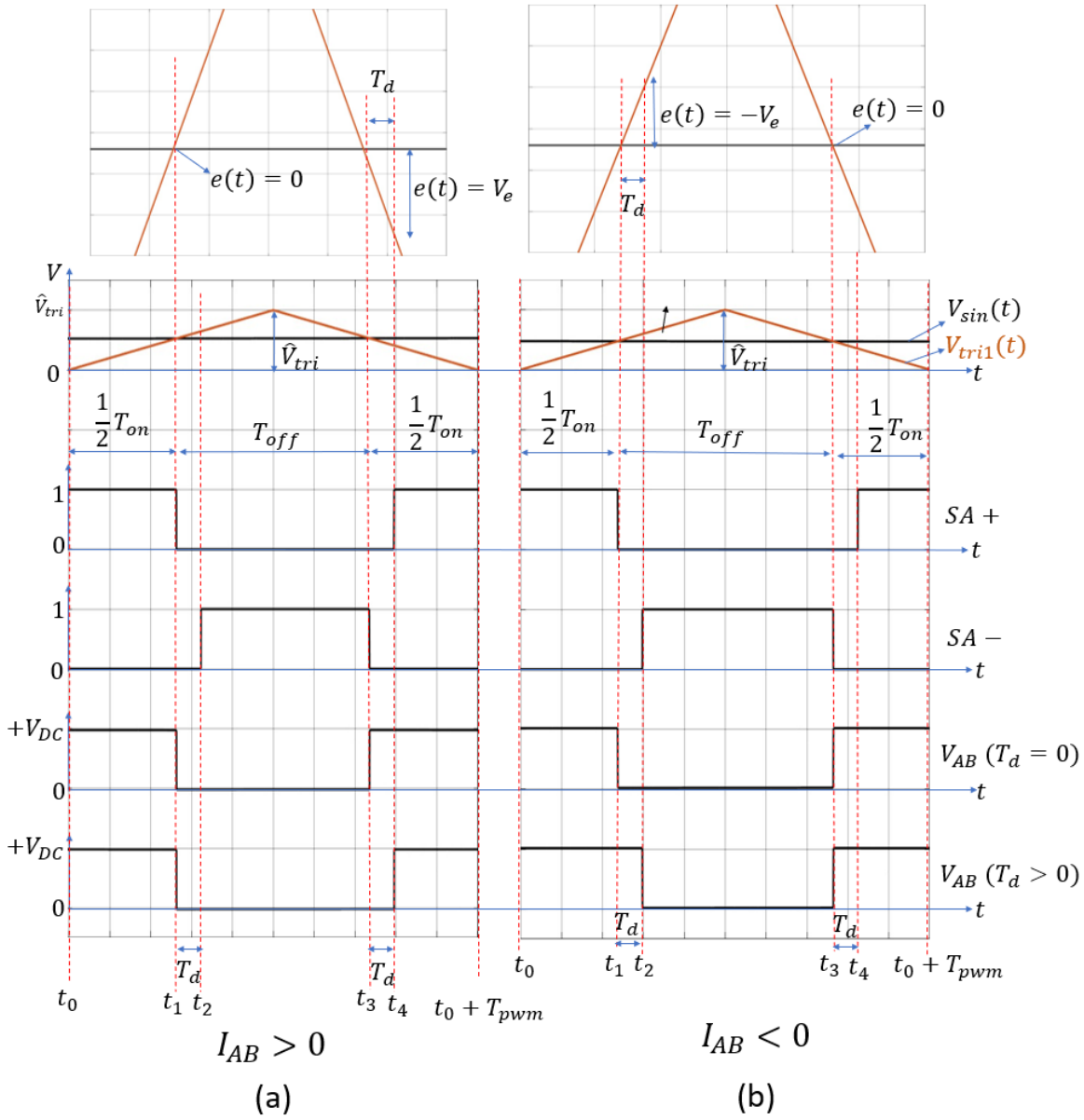


**Figure 3-18: The $T_d$ effect during the positive half period of $V_{sin}(t)$. (a) $I_{AB} > 0$, (b) $I_{AB} < 0$**

Focusing on the time when $I_{AB}(t) > 0$ firstly. A complete period of $T_{pwm}$ is from $t = t_0$ to $t_0 + T_{pwm}$. A new $PWM$ period starts at $t_0$, $V_{tri1}(t)$ starts from its lowest voltage ($0V$). From $t_0$ to $t_1$, $V_{sin}(t) > V_{tri1}(t)$, $SA+$ is on, $SA-$ is off, current $I_{AB}$ through the $SA+$ and $SB-$ from leg $A$ to $B$, the inductive load is charged by $DC$ power, $V_{AB} = +V_{DC}$. At $t = t_1$, $V_{sin}(t_1) < V_{tri1}(t_1)$, $SA+$ turns off, because of the

$T_d$, the $SA-$ is off as well. During dead time $T_d$ ($t_1$ to $t_2$), only $SB-$ is on, the inductive action keeps current flow in the same direction, which through the $SB-$ and the diode $DA-$. The voltage drop on the diode is ignored, so the voltage at point $V_A$ and $V_B$ are same (connected to the ground), the $V_{AB} = 0V$. At $t = t_2$, $SA-$ turns on. From $t_2$ to $t_3$, $SA-$ and $SB-$ are on, inductive current flows through the $SB-$ and $SA-$, $V_{AB} = 0$. At $t = t_3$, $V_{sin}(t_3) > V_{tri1}(t_3)$, $SA-$ turns off, while $SA+$ is still off because of $T_d$. From $t_3$ to $t_4$, the inductive current $I_{AB}$ flows though the $SB-$ and $DA-$ again, $V_{AB}$ is still at $0V$. Until $t = t_4$, $SA+$ turns on, $I_{AB}$ flows through $SA+$ and $SB-$, which charge the inductive load, $V_{AB}$ turns to $+V_{DC}$. From $t_4$ to ($t_0 + T_{pwm}$), $SA+$ and $SB-$ are on, $I_{AB}$ flows through them, $V_{AB}$ is still equal to $+V_{DC}$.

**Figure 3-18** (b) shows the dead time effect when $I_{AB} < 0$. Time $t$ starts at $t_0$ ($V_{tri1}(t_0) = 0V$). From $t_0$ to $t_1$, $V_{sin}(t) > V_{tri1}(t)$, $SA+$ and $SB-$ are on, $V_{AB} = +V_{DC}$, the inductive load release energy, keeping the $I_{AB}$ flows in negative direction through $SA+$ and $SB-$. From $t_1$ to $t_2$, $V_{sin}(t) < V_{tri1}(t)$, $SA+$ is off, $SA-$ is off because of $T_d$, the inductive action turns on the $DA+$, current flows through the $SB-$ and $DA+$, the $V_{AB} = +V_{DC}$. At $t = t_2$, $SA-$ turns on. From $t_2$ to $t_3$, $SA-$ and $SB-$ are both on, the inductive current flows through the $SB-$ and $SA-$ from leg $B$ to leg $A$, $V_{AB}$ turns to $0V$. At $t = t_3$, $V_{sin}(t_3) > V_{tri1}(t_3)$, $SA-$ turns off. From $t_3$ to $t_4$, $V_{sin}(t) > V_{tri1}(t)$, $SA-$ and $SA+$ are both off because of $T_d$, the $DA+$ is on again, current flows through the $SB-$ and $DA+$, $V_{AB} = +V_{DC}$. At $t_4$, $SA+$ turns on. From $t_4$ to $t_0 + T_{pwm}$, inductive current flows through the $SB-$ and $SA+$, $V_{AB} = +V_{DC}$.

In a 3-level H-Bridge inverter, the $\boldsymbol{e(t)}$ is introduced as the different voltage between $\boldsymbol{V_{sin}(t)}$ and $\boldsymbol{V_{tri1}(t)}$ or $\boldsymbol{V_{tri2}(t)}$. During the positive half period of $\boldsymbol{V_{sin}(t)}$, $\boldsymbol{V_{sin}(t)}$ is always larger than $\boldsymbol{V_{tri2}(t)}$, which the switches status in leg B is fixed. As result, only the $\boldsymbol{e(t)}$ value between $\boldsymbol{V_{sin}(t)}$ and $\boldsymbol{V_{tri1}(t)}$ is considered during this time. The equation of $\boldsymbol{e(t)}$ is,

$$\boldsymbol{e(t) = V_{sin}(t) - V_{tri1}(t)} \tag{38}$$

The $\boldsymbol{V_e}$ is equivalent to the change in $\boldsymbol{V_{tri1}(t)}$ over the dead time interval. The meaning of $\boldsymbol{V_e}$ in 3-level H-Bridge is same to that in 2-level system. Referring to **Figure 3-18**, the $\boldsymbol{V_e}$ can be calculated by similar triangle equation. Different to the 2-level system, the peak-to-peak voltage of $\boldsymbol{V_{tri1}(t)}$ is $\boldsymbol{\hat{V}_{tri}}$ instead of $\boldsymbol{2 * \hat{V}_{tri}}$. As result, the equation of $\boldsymbol{V_e}$ in 3-level system is,

$$\frac{\boldsymbol{V_e}}{\boldsymbol{T_d}} = \frac{\boldsymbol{\hat{V}_{tri}}}{\frac{\boldsymbol{T_{pwm}}}{\boldsymbol{2}}} \Rightarrow \boldsymbol{V_e = 2 f_{tri} * T_d * \hat{V}_{tri}} \tag{39}$$

The block diagram of relation between $\boldsymbol{e(t)}$ and $\boldsymbol{V_{AB}}$ with different current direction with $\boldsymbol{T_d}$ is shown in **Figure 3-19**.

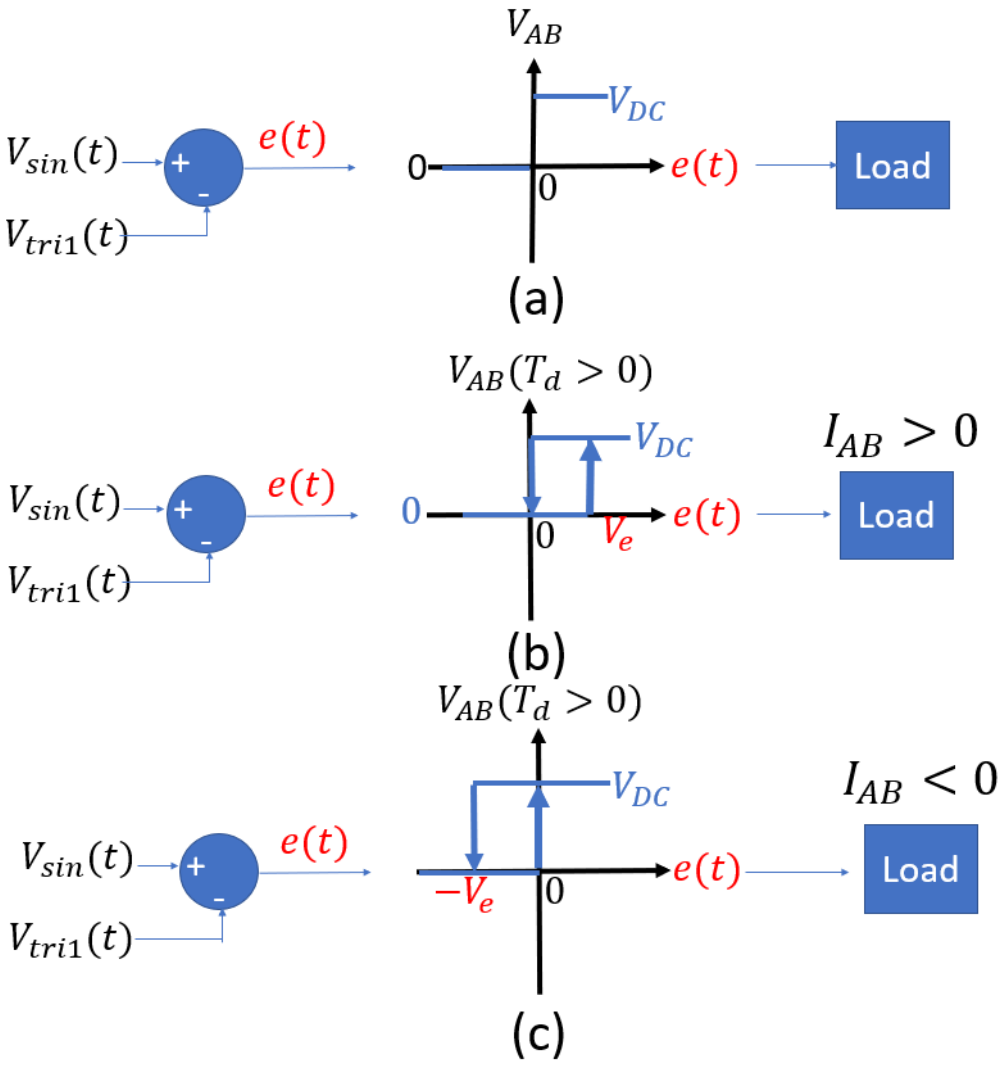


**Figure 3-19: Relation between $e(t)$ and output $V_{AB}$ during negative period. (a) $T_d = 0$, (b)$T_d > 0$ and $I_{AB} > 0$, (c) $T_d > 0$ and $I_{AB} < 0$.**

**Figure 3-19** (a) shows the voltage change of $V_{AB}$ under ideal situation ($T_d = 0$), $V_{AB}$ changes once $e(t) = 0$. With the dead time effect ($T_d > 0$), if $I_{AB} > 0$, $V_{AB}$ turns from $+V_{DC}$ (high-level voltage) to $0V$ (low-level voltage) at $e(t) = 0$, while $V_{AB}$ turns from $0V$ (low-level voltage) to $+V_{DC}$ (high-level voltage) at $e(t) = +V_e$. The time for $V_{AB} = +V_{DC}$ ($T_{on}$) is decreased by $T_d$.

On the other hands, when $I_{AB} < 0$, $V_{AB}$ turns from $+V_{DC}$ (high-level voltage) to $0V$ (low-level voltage) at $e(t) = -V_e$, while $V_{AB}$ turns from $0V$ (low-level voltage) to

$+\boldsymbol{V_{DC}}$ (high-level voltage) at $\boldsymbol{e(t) = 0}$. The time for $\boldsymbol{V_{AB} = +V_{DC}}$ ($\boldsymbol{T_{on}}$) is increased by $\boldsymbol{T_d}$.

Referring to **Figure 3-18**, the duty cycle of $\boldsymbol{T_d}$, $\boldsymbol{D_{T_d}}$ in the 3-level H-Bridge can be calculated as,

$$\boldsymbol{D_{T_d} = \frac{T_d}{T_{pwm}} = \frac{V_e}{2\widehat{V}_{tri}}} \tag{40}$$

With the $\boldsymbol{T_d}$, when $\boldsymbol{I_{AB} > 0}$, the duty cycle $\boldsymbol{D}$ is decreased by $\boldsymbol{D_{T_d}}$, so $\boldsymbol{D_{AB} = D - D_{T_d}}$. when $\boldsymbol{I_{AB} < 0}$, the duty cycle $\boldsymbol{D}$ is increased by $\boldsymbol{D_{T_d}}$, so $\boldsymbol{D_{AB} = D + D_{T_d}}$. As result, the equation of $\boldsymbol{D_{AB}}$ in 3-level H-Bridge inverter (positive period of $\boldsymbol{V_{sin}(t)}$) is,

$$\boldsymbol{D_{AB} = \frac{\widehat{V}_{sin} * \sin(\omega_{sin} t)}{\widehat{V}_{tri}} - sgn(I_{AB}) * D_{T_d} \qquad sin(\omega_{sin} t) > 0} \tag{41}$$

The $\boldsymbol{sgn(I_{AB}) = 1}$ when $\boldsymbol{I_{AB} > 0}$, while $\boldsymbol{sgn(I_{AB}) = -1}$ when $\boldsymbol{I_{AB} < 0}$. The fundamental voltage of $\boldsymbol{V_{AB}}$ with $\boldsymbol{T_d}$ is $\boldsymbol{V_{inv}(t)}$ which is equal to

$$\boldsymbol{V_{inv}(t) = V_{DC} * D_{AB} = V_{DC} * \left[\frac{\widehat{V}_{sin} * \sin(\omega_{sin} t)}{\widehat{V}_{tri}} - sgn(I_{AB}) * D_{T_d}\right]} \tag{42}$$

According to equation (42), after adding the $\boldsymbol{T_d}$ into system, a $\boldsymbol{V_{DC} * sgn(I_{AB}) * D_{T_d}}$ voltage drop is caused.

## 3.5.2 Dead Time effect at negative half period of $\boldsymbol{V_{sin}(t)}$

At the negative half period of $\boldsymbol{V_{sin}(t)}$, since the $\boldsymbol{V_{tri1}(t)}$ is always larger than $\boldsymbol{V_{sin}(t)}$, $\boldsymbol{SA+}$ keeps off, while $\boldsymbol{SA-}$ keeps on. During this time, the $\boldsymbol{SPWM}$ system focuses on

$\boldsymbol{V_{sin}(t)}$ and $\boldsymbol{V_{tri2}(t)}$. **Figure 3-20** shows the dead time effect in 3-level system with different direction of $\boldsymbol{I_{AB}}$.

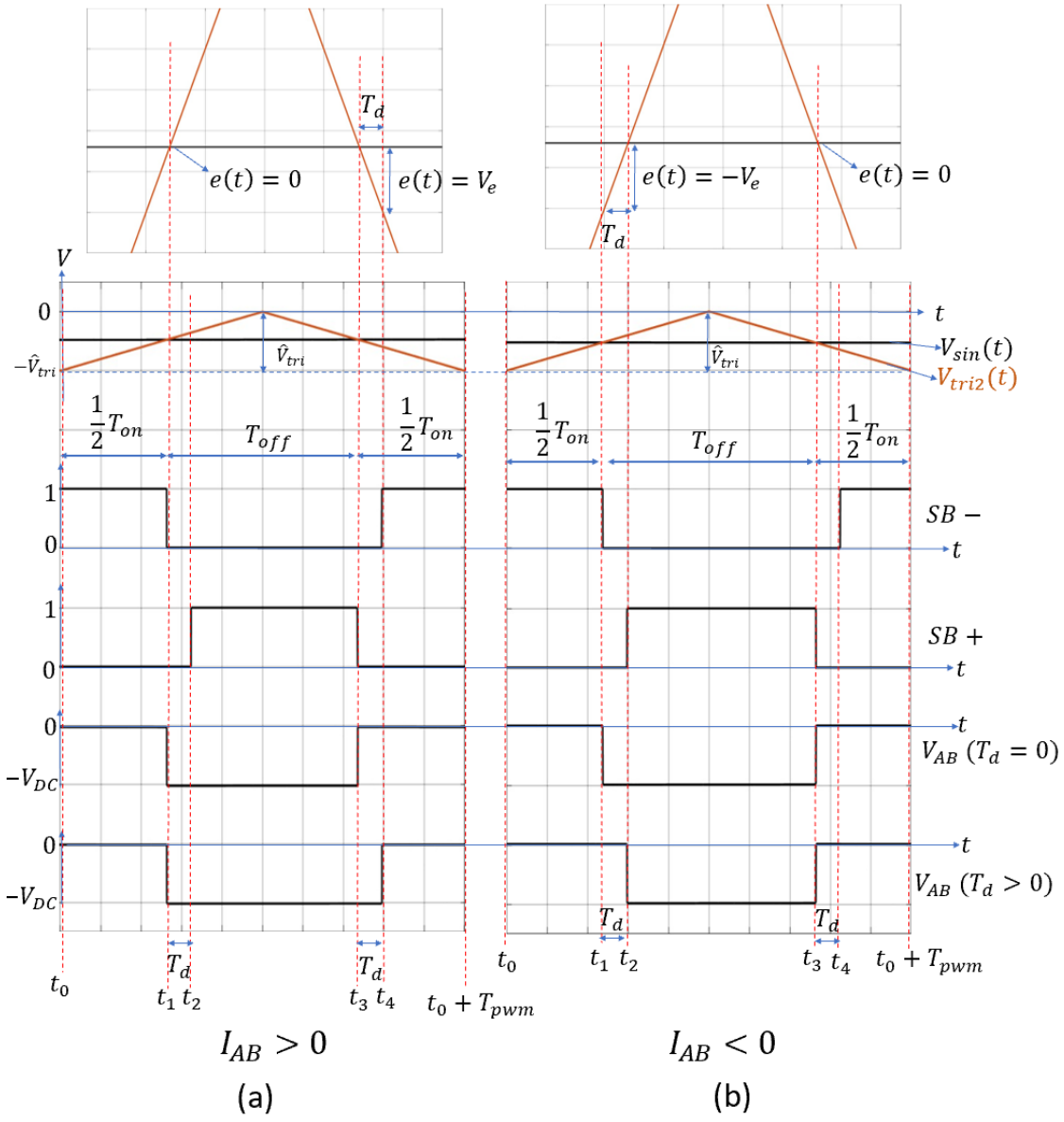


**Figure 3-20: The dead time effect during the negative period of $\boldsymbol{V_{sin}(t)}$.**

Firstly, focusing on the dead time effect when $\boldsymbol{I_{AB} > 0}$. Starting at $\boldsymbol{t = t_0}$, the $\boldsymbol{V_{tri2}(t_0) = -\hat{V}_{tri}}$. From $\boldsymbol{t_0}$ to $\boldsymbol{t_1}$, $\boldsymbol{V_{sin}(t) > V_{tri2}(t)}$, $\boldsymbol{SB+}$ is off, $\boldsymbol{SB-}$ is on, inductive current flows through the $\boldsymbol{SA-}$ and $\boldsymbol{SB-}$ from leg $\boldsymbol{A}$ to leg $\boldsymbol{B}$, $\boldsymbol{V_{AB} = 0}$. At $\boldsymbol{t = t_1}$, $\boldsymbol{V_{sin}(t_1) < V_{tri2}(t_2)}$, $\boldsymbol{SB-}$ turns off, inductive action turns $\boldsymbol{DB+}$ on. From

$t_1$ to $t_2$, current flows through the $SA-$ and $DB+$ from leg $A$ to $B$, $V_{AB} = -V_{DC}$. $SB+$ turns on at $t = t_2$, from $t_2$ to $t_3$, inductive current flows through the $SA-$ and $SB+$, $V_{AB} = -V_{DC}$. At $t = t_3$, $V_{sin}(t_3) > V_{tri2}(t_3)$, $SB+$ turns off, $DB+$ turns on. During $T_d$ $(t_3 \; to \; t_4)$, the inductive current flows through $SA-$ and $DB+$, $V_{AB} = -V_{DC}$. At $t = t_4$, $SB-$ is turned on, current flows through the $SA-$ and $SB-$, $V_{AB}$ turns to $0V$. From $t_4$ to $t_0 + T_{pwm}$, switching status remains, so as the $V_{AB}$ and $I_{AB}$ conditions remain.

Now, focusing on the time when $I_{AB} < 0$. The $PWM$ period starts at $t_0$, $V_{tri}(t_0) = -\widehat{V}_{tri}$. From $t_0$ to $t_1$, $V_{sin}(t) > V_{tri2}(t)$, $SB-$ is on, $SB+$ is off, inductive current flow through the $SA-$ and $SB-$ from leg $B$ to $A$, $V_{AB} = 0V$. At $t = t_1$, $SB-$ turns off. The time from $t_1$ to $t_2$ is dead time, $SB-$ is off, $SB+$ is still off, and so inductive action turns on the $DB-$, current flows through the $SA-$ and $DB-$, $V_{AB}$ is still $0V$. At $t = t_2$, $SB+$ turns on. From $t_2$ to $t_3$, $SA-$ and $SB+$ are on, current flows through the $SB+$ and $SA-$, the inductive load is charged by $DC$ voltage, $V_{AB} = -V_{DC}$. At $t = t_3$, $SB+$ turns off, inductive action turns on the $DB-$ again keeping current flows through the $SA-$ and $DB-$, $V_{AB}$ turns to $0V$. Durning the $T_d$ ($t_3$ to $t_4$), $SB-$ is still off, inductive current still flows through the $SA-$ and $DB-$, $V_{AB} = 0V$. At $t = t_4$, $SB-$ turns on. From $t_4$ to $t_0 + T_{pwm}$, current flows through the $SA-$ and $SB-$ again, $V_{AB} = 0V$.

During the negative half period of $V_{sin}(t)$, the switches status on leg $A$ are fixed. Only the difference value between $V_{sin}(t)$ and $V_{tri2}(t)$ is considered.

$$e(t) = V_{sin}(t) - V_{tri2}(t) \tag{43}$$

**Figure 3-21** shows the relation between $e(t)$ and $V_{AB}$ with dead time effect.

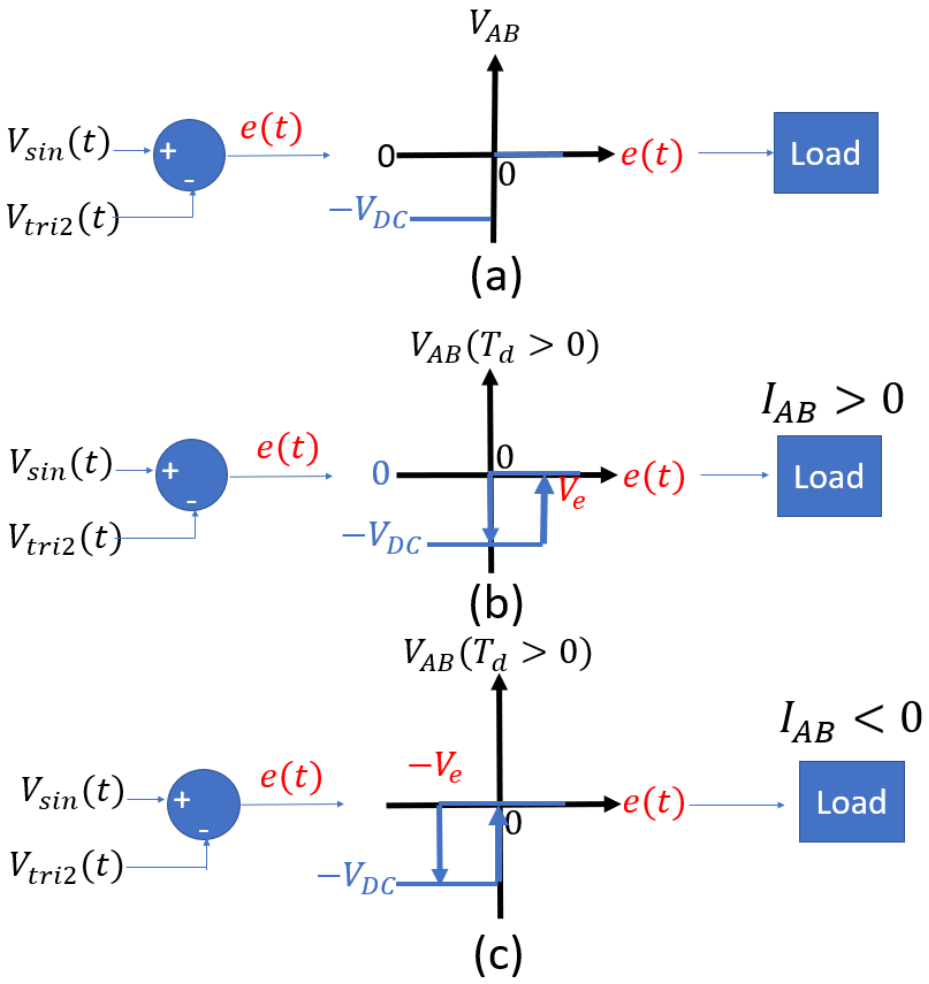


**Figure 3-21: Relation between $e(t)$ and output $V_{AB}$ during negative period. (a) $T_d = 0$, (b)$T_d > 0$ and $I_{AB} > 0$, (c) $T_d > 0$ and $I_{AB} < 0$.**

**Figure 3-21** (a) shows the ideal situation ($T_d = 0$) of $V_{AB}$ changes with $e(t)$. $V_{AB}$ changes between $0$ and $-V_{DC}$ at $e(t) = 0$.

Referring to **Figure 3-21**, if $I_{AB} > 0$, $V_{AB}$ turns from $0V$ (high-level voltage) to $-V_{DC}$ (low-level voltage) at $e(t) = 0$, while $V_{AB}$ turns from $-V_{DC}$ (low-level voltage) to $0V$ (high-level voltage) at $e(t) = +V_e$. The time duration for $V_{AB} = 0V$ ($T_{on}$) is decreased by $T_d$.

On the other hands, when $\boldsymbol{I_{AB} < 0}$, $\boldsymbol{V_{AB}}$ turns from $\boldsymbol{0V}$ (high-level voltage) to $\boldsymbol{-V_{DC}}$ (low-level voltage) at $\boldsymbol{e(t) = -V_e}$, while $\boldsymbol{V_{AB}}$ turns from $\boldsymbol{-V_{DC}}$ (low-level voltage) to $\boldsymbol{0}$ (high-level voltage) at $\boldsymbol{e(t) = 0}$. The time for $\boldsymbol{V_{AB} = 0V}$ ($\boldsymbol{T_{on}}$) is increased by $\boldsymbol{T_d}$. The duty cycle of dead time is $\boldsymbol{D_{T_d} = \frac{V_e}{2 * \hat{V}_{tri}}}$. When $\boldsymbol{I_{AB} > 0}$, $\boldsymbol{D_{AB} = D - D_{T_d}}$. When $\boldsymbol{I_{AB} < 0}$, $\boldsymbol{D_{AB} = D + D_{T_d}}$. Taking the $\boldsymbol{D_{T_d}}$ into the equation (19), equation of $\boldsymbol{D_{AB}}$ is,

$$\boldsymbol{D_{AB} = \frac{\hat{V}_{sin} * \sin(\omega_{sin} t)}{\hat{V}_{tri}} + 1 - sgn(I_{AB}) * D_{Td}} \quad (44)$$

The fundamental voltage equation is,

$$\boldsymbol{V_{inv}(t) = V_{DC} * \left[\frac{\hat{V}_{sin} * \sin(\omega_{sin} t)}{\hat{V}_{tri}} - sgn(I_{AB}) * D_{T_d}\right]} \quad (45)$$

Which is equal to the equation (42) described before in positive period of $\boldsymbol{V_{sin}(t)}$.

As result, whenever the positive or negative period of $\boldsymbol{V_{sin}(t)}$, the fundamental voltage $\boldsymbol{V_{inv}(t)}$ is decreased by $\boldsymbol{sgn(I_{AB}) * D_{T_d}}$, and it is only related to the current direction of $\boldsymbol{I_{AB}}$.

# 3.6 Dead Time Compensation in 3-level H-Bridge inverter

The previous section describes the dead time effect in a 3-level H-Bridge inverter. In this section, the Dead Time Compensation system in 3-level H-Bridge inverter will be introduced and described.

Equation (45) provides the output fundamental voltage $\boldsymbol{V_{inv}(t)}$ under the dead time effect. In equation (45), $\boldsymbol{D_{T_d} = \frac{V_e}{2 * \hat{V}_{tri}}}$, equation (45) is equivalent to

$$V_{inv}(t) = \frac{\widehat{V}_{sin} * \sin(\omega_{sin} t) - \frac{1}{2} V_e * sgn(I_{AB})}{\widehat{V}_{tri}} \quad (46)$$

The term $\widehat{V}_{sin} * \sin(\omega_{sin} t)$ is the original reference signal $V_{sin}(t)$, and the term $-\frac{1}{2} V_e * sgn(I_{AB}) = V_{DT}$ is due to the dead time. The effect of dead time can be reduced by adding a term to nullify $V_{DT}$, $0 = V_{DT} + V_{DTC}$, where $V_{DTC}$ is the deadtime compensation voltage.

$$V_{DTC} = \frac{1}{2} V_e * sgn(I_{AB}) \quad (47)$$

The equation of $V_{DTC}$ in 2-level and 3-level system are same, the difference is the value of $V_e$. In 2-level system, $V_e = 4 * f_{pwm} * T_d * \widehat{V}_{tri}$, while in 3-level system, $V_e = 2 * f_{pwm} * T_d * \widehat{V}_{tri}$.

**Figure 3-22** shows the block diagram of ***DTC*** system in 3-level system.

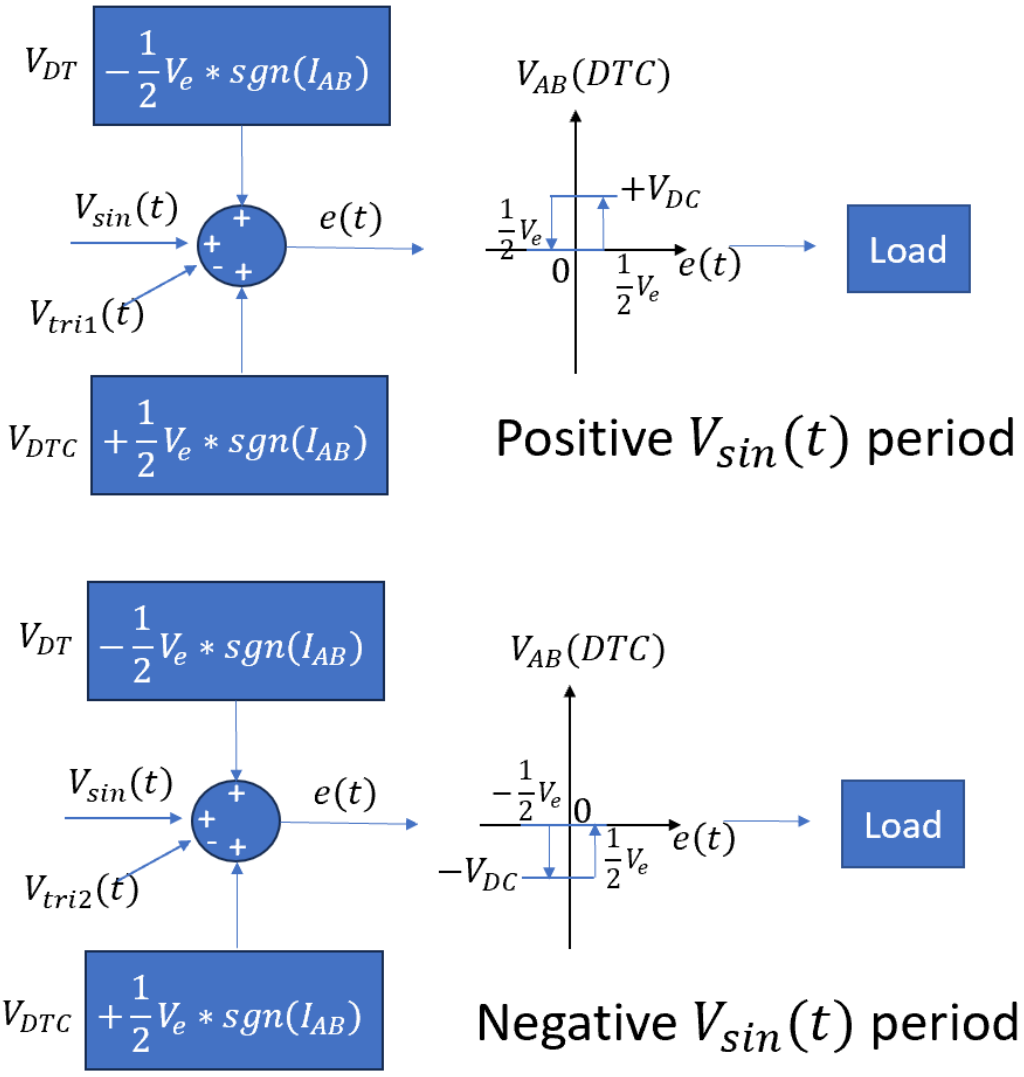


**Figure 3-22: Block diagram of *DTC* in 3-level system.**

Similar to the 2-level ***DTC*** system, after adding $\boldsymbol{V_{DTC}}$, phase lag remained. As result, ***PLC*** system is also required.

As described before in section 3.3, the ***PLC*** system in 2-level and 3-level system are same. But the phase lag compensation value $\boldsymbol{V_{PLC}}$ are different. In the 3-level system, the $\boldsymbol{V_{PLC}}$ is equal to

$$\boldsymbol{V_{PLC} = 2 * T_{delay} * \hat{V}_{tri} * f_{pwm} * sgn(V_{tri})} \quad (48)$$

Since $\boldsymbol{T_{delay} = \frac{1}{2}T_d}$, $\boldsymbol{V_{PLC} = T_d * \hat{V}_{tri} * f_{pwm} * sgn(V_{tri})}$. Because the phase and frequency of $\boldsymbol{V_{tri1}(t)}$ and $\boldsymbol{V_{tri2}(t)}$ are same, either of them can be used as the reference to decide the $\boldsymbol{sgn(V_{tri})}$. If the gradient of $\boldsymbol{V_{tri1}(t)}$ or $\boldsymbol{V_{tri2}(t)}$ is positive, $\boldsymbol{sgn(V_{tri}) = -1}$. If the gradient of $\boldsymbol{V_{tri1}(t)}$ or $\boldsymbol{V_{tri2}(t)}$ is negative, $\boldsymbol{sgn(V_{tri}) = +1}$. The final block diagram of ***DTC*** and ***PLC*** is shown in **Figure 3-23**.

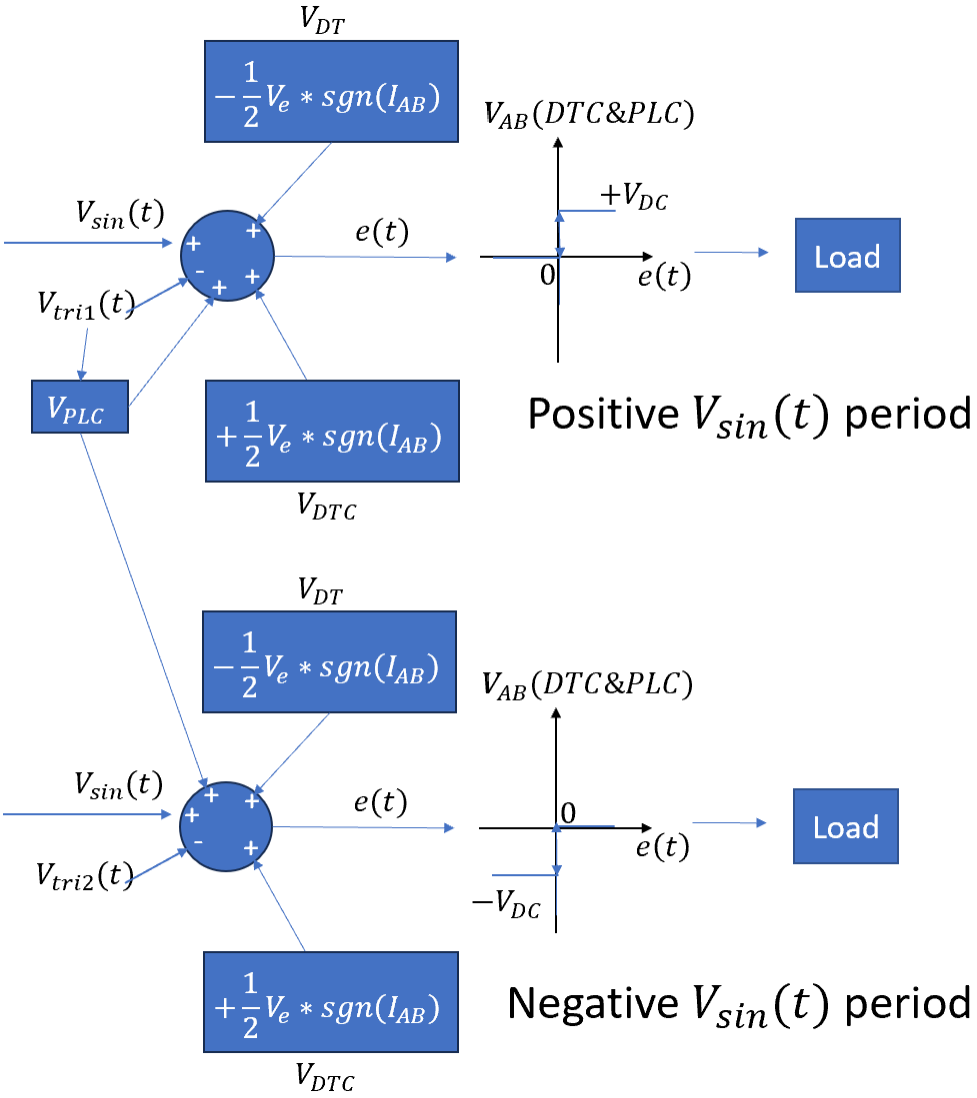


**Figure 3-23: Block diagram of *DTC* and *PLC* system in 3-level system.**

After adding the ***PLC***, the phase lag is compensated.

In conclusion, the new modulation signal after adding ***DTC*** and ***PLC*** is equal to $\boldsymbol{V_{sin}(t) + V_{DTC} + V_{PLC}}$, and this new value will be compared with $\boldsymbol{V_{tri1}(t)}$ and

$\boldsymbol{V_{tri2}(t)}$ to produce new ***SPWM*** output signal. The block diagram of Dead Time Compensation in 3-level H-Bridge inverter is shown in **Figure 3-24**.

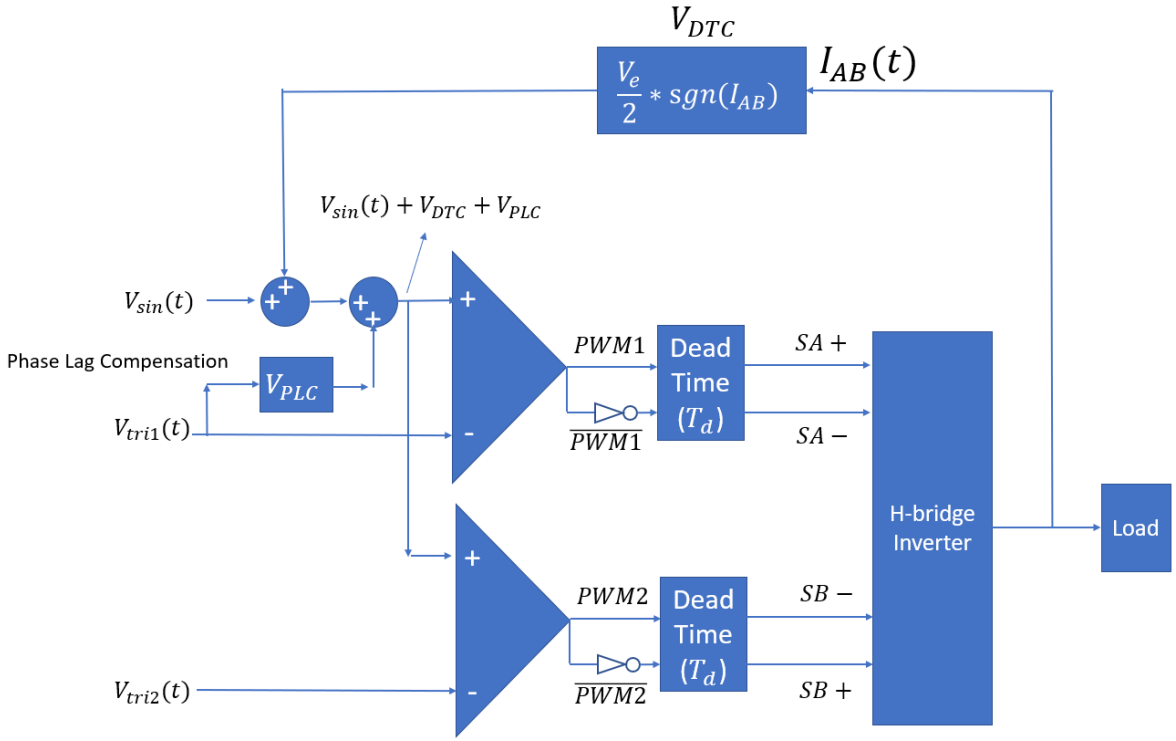


**Figure 3-24: The block diagram of Dead Time Compensation in 3-level H-Bridge inverter.**

The aim of Dead Time Compensation in 3-level system is still to produce ideal output voltage $\boldsymbol{V_{AB}}$ by updating new modulation signal for compensating the energy loss and distortion caused by $\boldsymbol{T_d}$.

# 3.7 MATLAB Simulink simulation of Dead Time Compensation in 3-level H-Bridge inverter

The Dead Time Compensation system in 3-level H-Bridge inverter has been described in previous section. This section will show the Simulink simulation of Dead Time Compensation in 3-level H-Bridge inverter.

**Figure 3-25** (a) shows the structure of 3-level H-Bridge inverter and **Figure 3-25** (b) shows the 3-level $\boldsymbol{SPWM}$ system with dead time in Simulink simulation.

In this simulation, the inverter system drives a resistive load $\boldsymbol{R_{out}}$. The parameter of component in the H-Bridge inverter are shown in **Figure 3-25** (a). The sinusoidal reference voltage $\boldsymbol{V_{sin}(t) = 0.65 * \sin(2\pi * 50 * t)}$ with peak value $\boldsymbol{\widehat{V}_{sin} = 0.65}$ and a frequency $\boldsymbol{f_{sin} = 50Hz}$. For the $\boldsymbol{PWM}$ carrier signal, the peak value $\boldsymbol{\widehat{V}_{tri} = 1}$. $\boldsymbol{V_{tri1}(t)}$ changes between $\boldsymbol{0V}$ and $\boldsymbol{1V}$, $\boldsymbol{V_{tri2}(t)}$ changes between $\boldsymbol{0V}$ and $\boldsymbol{-1V}$. Their frequency $\boldsymbol{f_{pwm} = 20kHz}$.

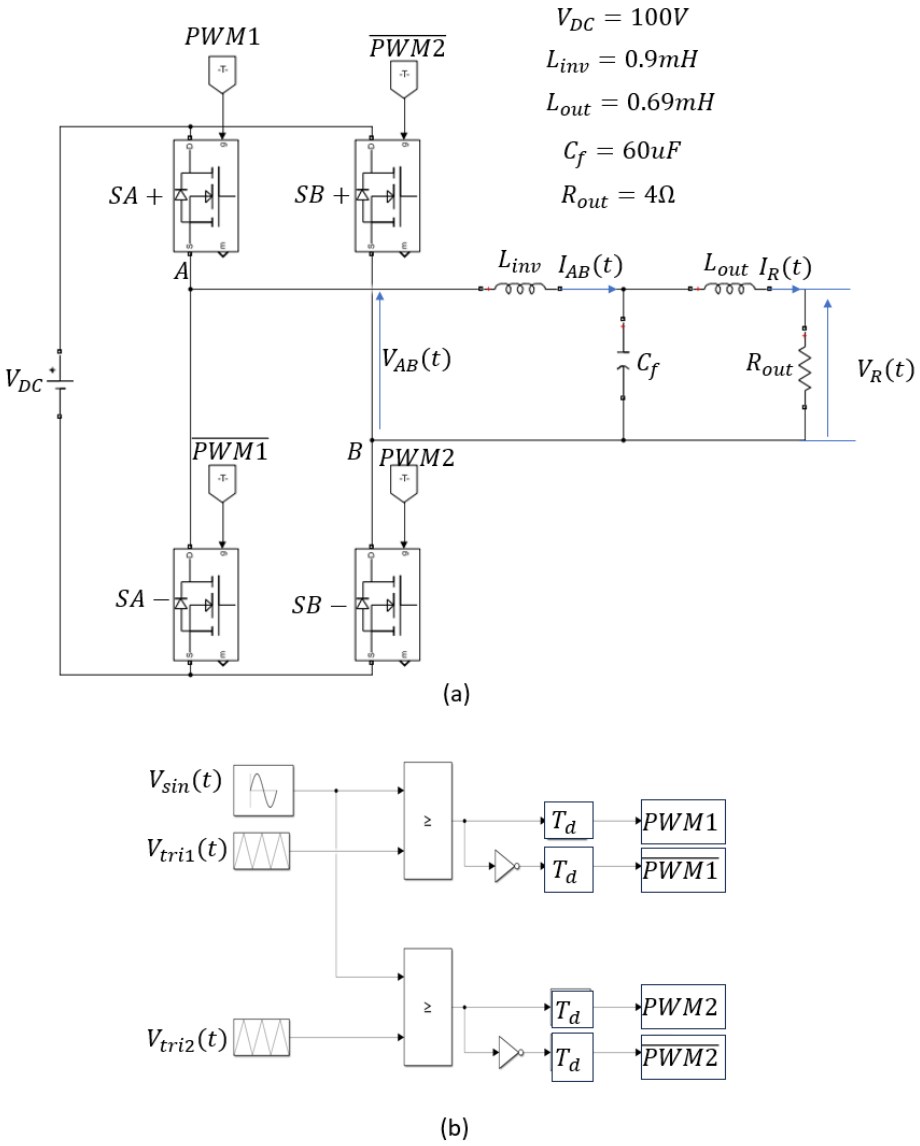


**Figure 3-25: (a) 3-level H-Bridge inverter and its control signal, (b) 3-level *SPMW* system.**

**Figure 3-26** shows the ***DTC*** and ***PLC*** system in simulation. A "SWITCH" function in Simulink is acted as a current direction detector, which decides the value of $\boldsymbol{V_{DTC}}$. The $\boldsymbol{V_{PLC}}$ is achieved by reading the gradient of $\boldsymbol{V_{tri1}(t)}$, if gradient is positive, $\boldsymbol{V_{PLC}}$ is negative, while $\boldsymbol{V_{PLC}}$ is positive when gradient is negative. As shown in **Figure 3-26** (c), the final modulation signal with ***DTC*** and ***PLC*** is equal to $\boldsymbol{V_{sin}(t) + V_{DTC} + V_{PLC}}$.

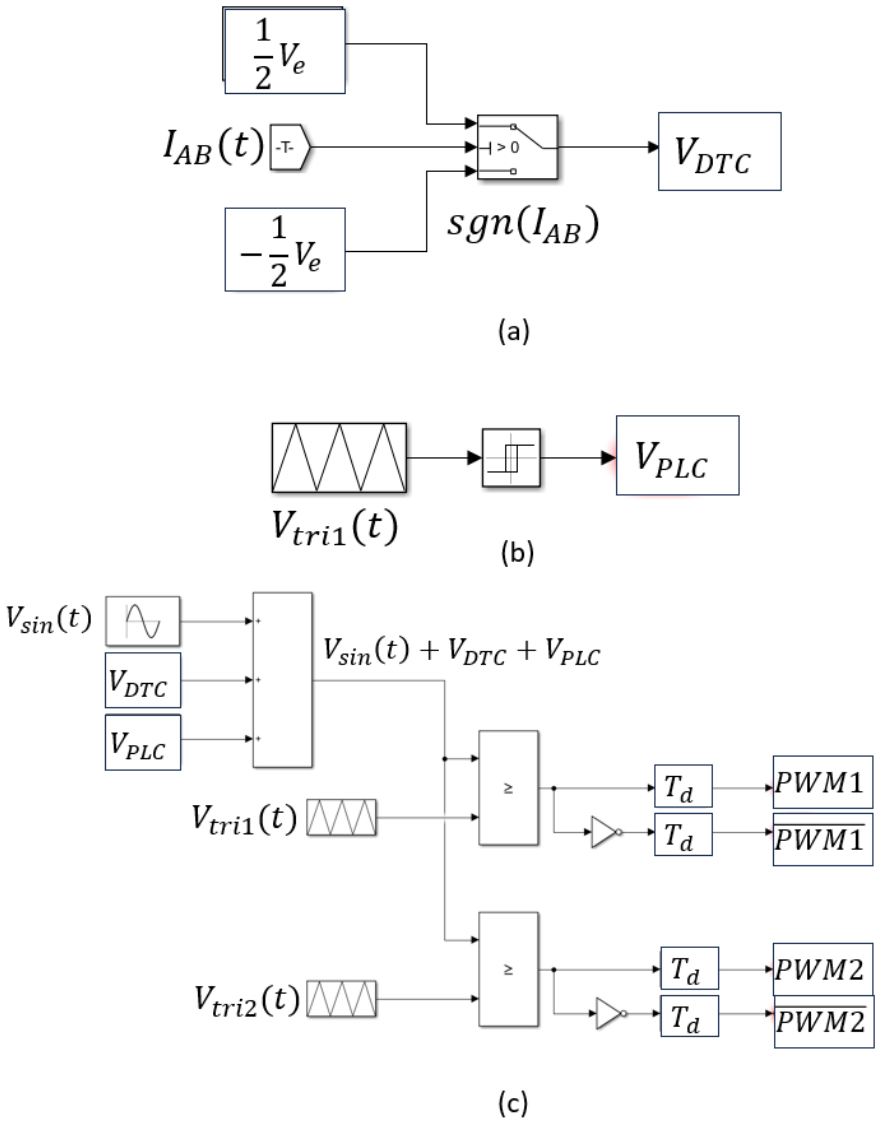


**Figure 3-26: (a) *DTC* system, (b) *PLC* system, (c) 3-level *SPWM* with *DTC* and *PLC*.**

**Figure 3-27** shows the original $\boldsymbol{V_{sin}(t)}$, $\boldsymbol{V_{tri1}(t)}$ and output voltage $\boldsymbol{V_{AB}}$ with and without Dead Time compensation system. **Figure 3-28** shows the original $\boldsymbol{V_{sin}(t)}$, $\boldsymbol{V_{tri2}(t)}$ and output voltage $\boldsymbol{V_{AB}}$ with and without Dead Time compensation system.

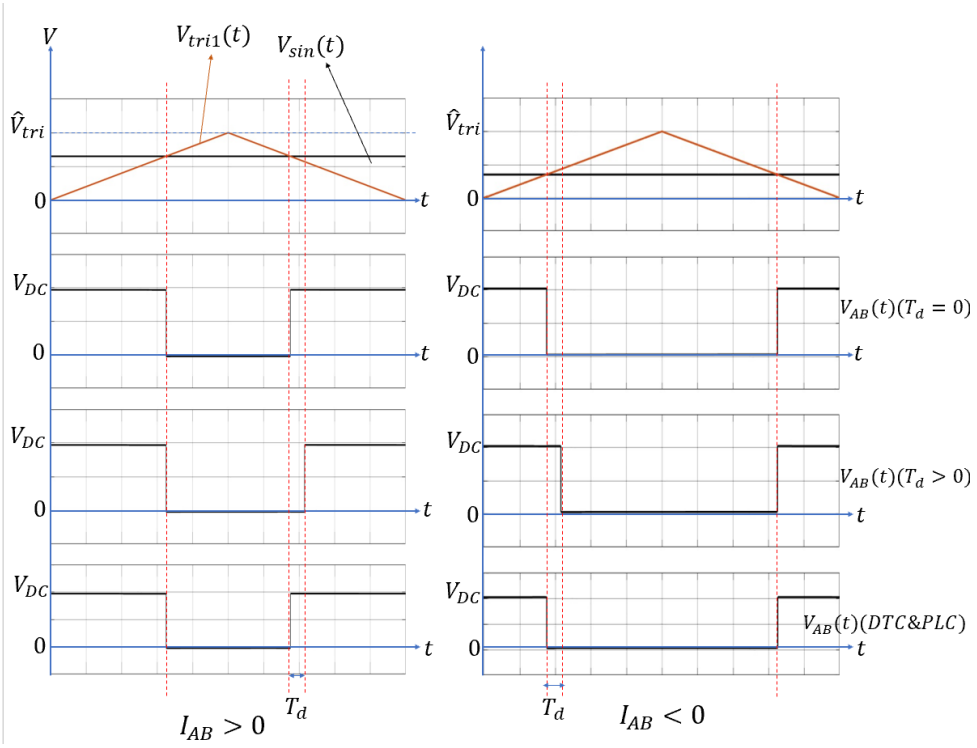


**Figure 3-27: waveform of $V_{sin}(t)$, $V_{tri1}(t)$ and $V_{AB}(t)$.**

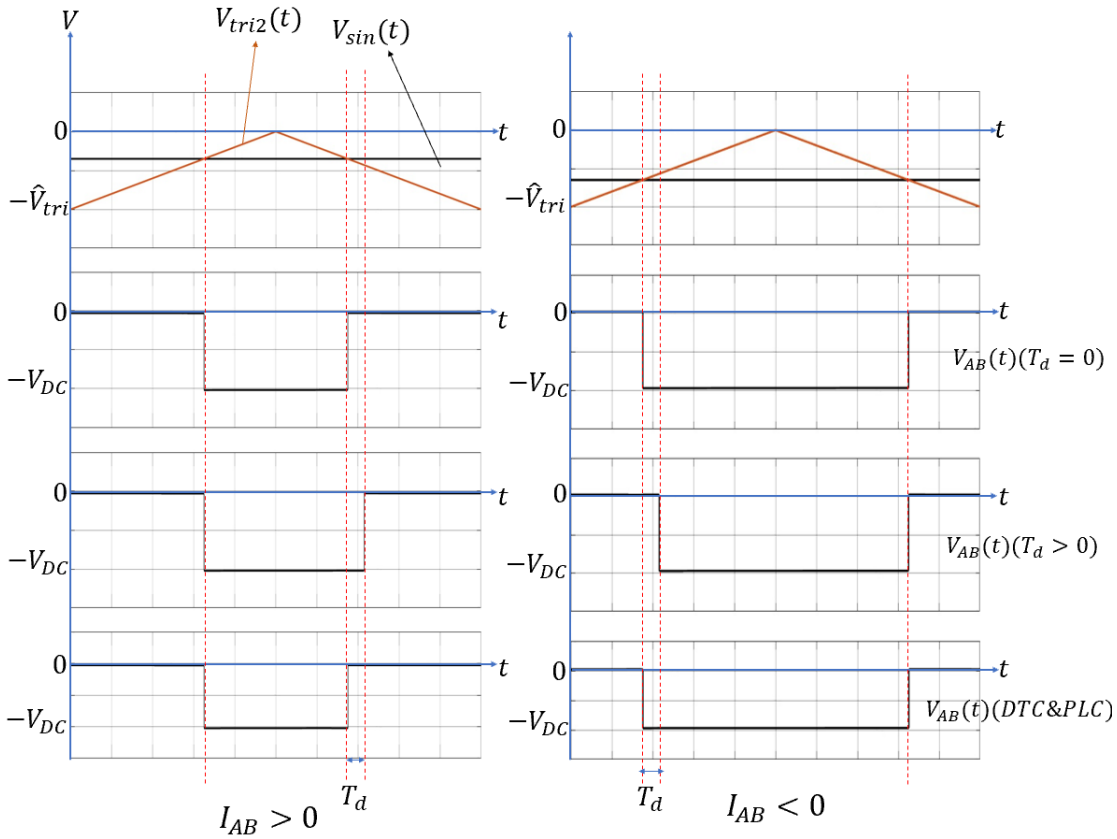


**Figure 3-28: waveform of $V_{sin}(t)$, $V_{tri2}(t)$ and $V_{AB}(t)$.**

$\boldsymbol{V_{AB}(t)(T_d = 0)}$ is the ideal output voltage without dead time, $\boldsymbol{V_{AB}(t)(T_d > 0)}$ is the output voltage with dead time, and $\boldsymbol{V_{AB}(t)(DTC\&PLC)}$ is the output voltage after adding the $\boldsymbol{DTC}$ and $\boldsymbol{PLC}$ system. It is clear to see that after adding the $\boldsymbol{DTC}$ and $\boldsymbol{PLC}$ system, all $\boldsymbol{V_{AB}(t)(DTC\&PLC)}$ under different condition are equal to the ideal output voltage $\boldsymbol{V_{AB}(t)(T_d = 0)}$.

**Figure 3-29** shows the output voltage on the resistor $\boldsymbol{R_{out}}$ under different conditions.

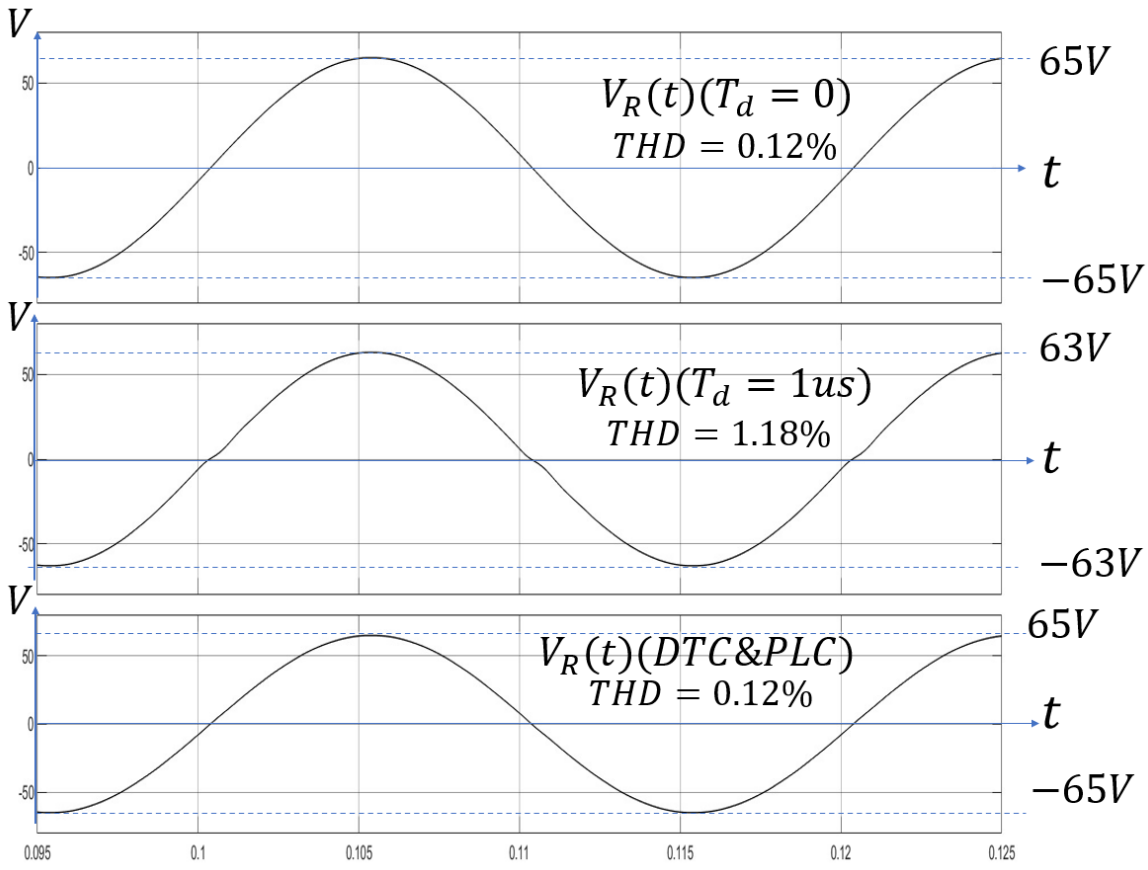


**Figure 3-29: $V_R(t)$ with different conditions.**

$\boldsymbol{V_R(t)(T_d = 0)}$ is the ideal output resistor voltage, $\boldsymbol{V_R(t)(T_d = 1us)}$ means the resistor voltage with $\boldsymbol{1us}$ dead time, the $\boldsymbol{V_R(t)(DTC\&PLC)}$ means the output resistor

voltage when the system with $\boldsymbol{DTC}$ and $\boldsymbol{PLC}$. The peak modulation index is $\mathbf{0.65}$. The $\boldsymbol{T_d = 1us}$, according to equation (45), the voltage reduction caused by the dead time is equal to $\boldsymbol{V_{DC} * \left[\frac{1}{2} * \frac{V_e}{\hat{V}_{tri}}\right] = 2V}$. As shown in **Figure 3-29**, when $\boldsymbol{T_d = 1us}$, the peak voltage of $\boldsymbol{V_R(t)}$ drops from $\boldsymbol{65V}$ to $\boldsymbol{63V}$. After adding the Dead Time Compensation system, the voltage drop is compensated, in addition, the distortion caused by $\boldsymbol{T_d}$ is compensated especially during the zero-crossing time. The $\boldsymbol{THD}$ is decreased to $\mathbf{0.12\%}$ after adding the Dead Time Compensation.

**Figure 3-30** shows the output current through the $\boldsymbol{R_{out}}$ which is $\boldsymbol{I_R(t)}$ under different conditions.

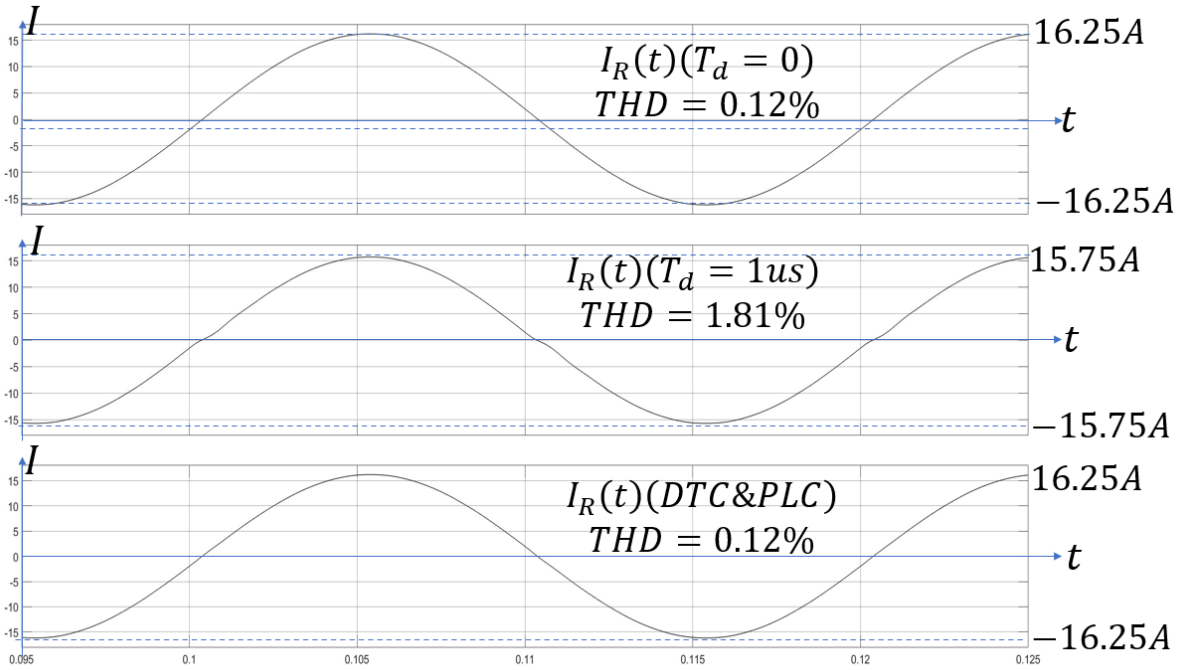


**Figure 3-30: resistor current $\boldsymbol{I_R(t)}$ under different conditions.**

The current $\boldsymbol{I_R(t) = \frac{V_R(t)}{R_{out}}}$, the $\boldsymbol{R_{out} = 4\,\Omega}$, without dead time effect, peak voltage $\boldsymbol{\hat{V}_R = 65V}$, $\boldsymbol{I_R(t) = \hat{I}_R = 16.25A}$. With $\boldsymbol{T_d = 1us}$, the voltage drop is $\boldsymbol{2V}$, which cause the $\boldsymbol{0.5A}$ current reduction as well. As result, the current $\boldsymbol{I_R(t)(T_d = 1us)}$ is

equal to $\mathbf{15.75}\boldsymbol{A}$ referring to **Figure 3-30**. After adding the $\boldsymbol{DTC}$ and $\boldsymbol{PLC}$ system, the current drop is compensated. The distortion caused by $\boldsymbol{T_d}$ is compensated especially during the zero-crossing.

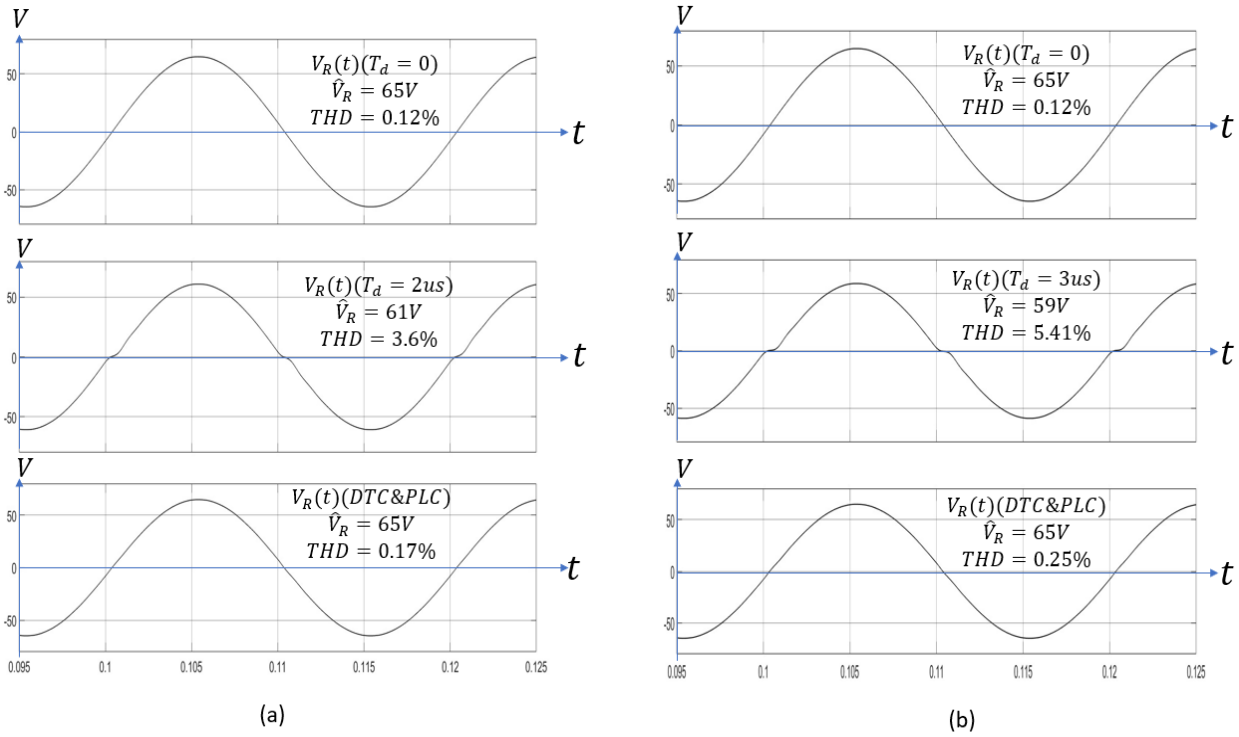


**Figure 3-31: waveform of output voltage $\boldsymbol{V_R(t)}$. (a) $\boldsymbol{T_d = 2us}$, (b) $\boldsymbol{T_d = 3us}$**

As shown in **Figure 3-31**, with the increase of $\boldsymbol{T_d}$, the voltage reduction is larger, and more distortion is caused especially during the zero-crossing. As shown in **Figure 3-31** (a), after adding the $\boldsymbol{DTC}$ and $\boldsymbol{PLC}$ system, the voltage drops and distortion caused by $\boldsymbol{T_d = 2us}$ are both compensated. When $\boldsymbol{T_d = 3us}$, the voltage drops are compensated by the $\boldsymbol{DTC}$ and $\boldsymbol{PLC}$, but the distortion caused by $\boldsymbol{3us\ T_d}$ is not be fully compensated. The $\boldsymbol{THD}$ after adding $\boldsymbol{VDTC}$ and $\boldsymbol{VPLC}$ is $\mathbf{0.25}\%$. As described before in section 3.4, the Dead Time compensation can produce ideal $\boldsymbol{V_{AB}(t)}$, but the $\boldsymbol{T_d}$ still exists. In the 3-

level system, $\boldsymbol{0V}$ is the lowest peak voltage of $\boldsymbol{V_{tri1}(t)}$ and the highest peak voltage of $\boldsymbol{V_{tri2}(t)}$, when the modulation reference signal close to $\boldsymbol{0V}$, the turn on time of $\boldsymbol{PWM1}$ and $\overline{\boldsymbol{PWM2}}$ are very short, which the turn on time of $\boldsymbol{SA+}$ and $\boldsymbol{SB+}$ are very short. Even with the Dead Time Compensation, the long $\boldsymbol{T_d}$ will cover the short turn on time of power switches especially during the zero-crossing time. As result, it is hard to produce the ideal $\boldsymbol{V_{AB}}$ during this time, which the distortion can not be fully compensated.

In conclusion, from section 3.4 to 3.5, the dead time effect and dead time compensation in 3-level H-Bridge inverter are introduced and described. This section shows the MATLAB/Simulink simulation of $\boldsymbol{DTC}$ and $\boldsymbol{PLC}$ system in 3-level H-Bridge inverter. It proves that the $\boldsymbol{DTC}$ can compensate the voltage drop and distortion caused by $\boldsymbol{T_d}$, and $\boldsymbol{PLC}$ can remove the phase lag. But with the increase of $\boldsymbol{T_d}$, the distortion caused by dead time effect is hard to be fully compensated. This is one point required to be improved in the future.

# 3.8 Chapter Conclusion

This chapter has demonstrated how dead time effects the performance of an inverter system. A deadtime compensation ($\boldsymbol{DTC}$) has been proposed that helps to reduce the waveform distortion nearby the zero-crossing points and voltage and current reduction. Since the $\boldsymbol{DTC}$ introduced a delay into bridge output, further compensation system has

been incorporated to remove this phase lag. Finally, the performance of the compensation system has been demonstrated using MATLAB/Simulink simulations.

Comparing the $\boldsymbol{V_{DTC}}$ and $\boldsymbol{V_{PLC}}$ value in the 2-level and 3-level H-Bridge inverter, the two values in the 3-level dead time compensation is lower than that in 2-level dead time compensation because of the peak-to-peak voltage of carrier signal. In 2-level H-Bridge inverter, with the increase of $\boldsymbol{T_d}$, the $\boldsymbol{V_{DTC}}$ and $\boldsymbol{V_{PLC}}$ value will be increased as well for compensate it. As result, the peak voltage of $\boldsymbol{V_{sin}(t) + V_{PLC} + V_{DTC}}$ will easily over the $\boldsymbol{\widehat{V}_{tri}}$ which cause over modulation. But in 3-level H-Bridge inverter dead time compensation, with same $\boldsymbol{T_d}$, the $\boldsymbol{V_{DTC}}$ and $\boldsymbol{V_{PLC}}$ are lower, which the over modulation does not happen easily.

# *Chapter 4*

## Power electronic hardware system design

This chapter describes the design of the power electronic hardware platform that is subsequently used to provide experimental validation of the proposed dead time compensation scheme. The system consists of a H-bridge inverter, ***LCL*** filter connected between the inverter and the load/grid and a microprocessor controller.

**Figure 4-1** shows the block diagram of the whole grid connected power inverter system.

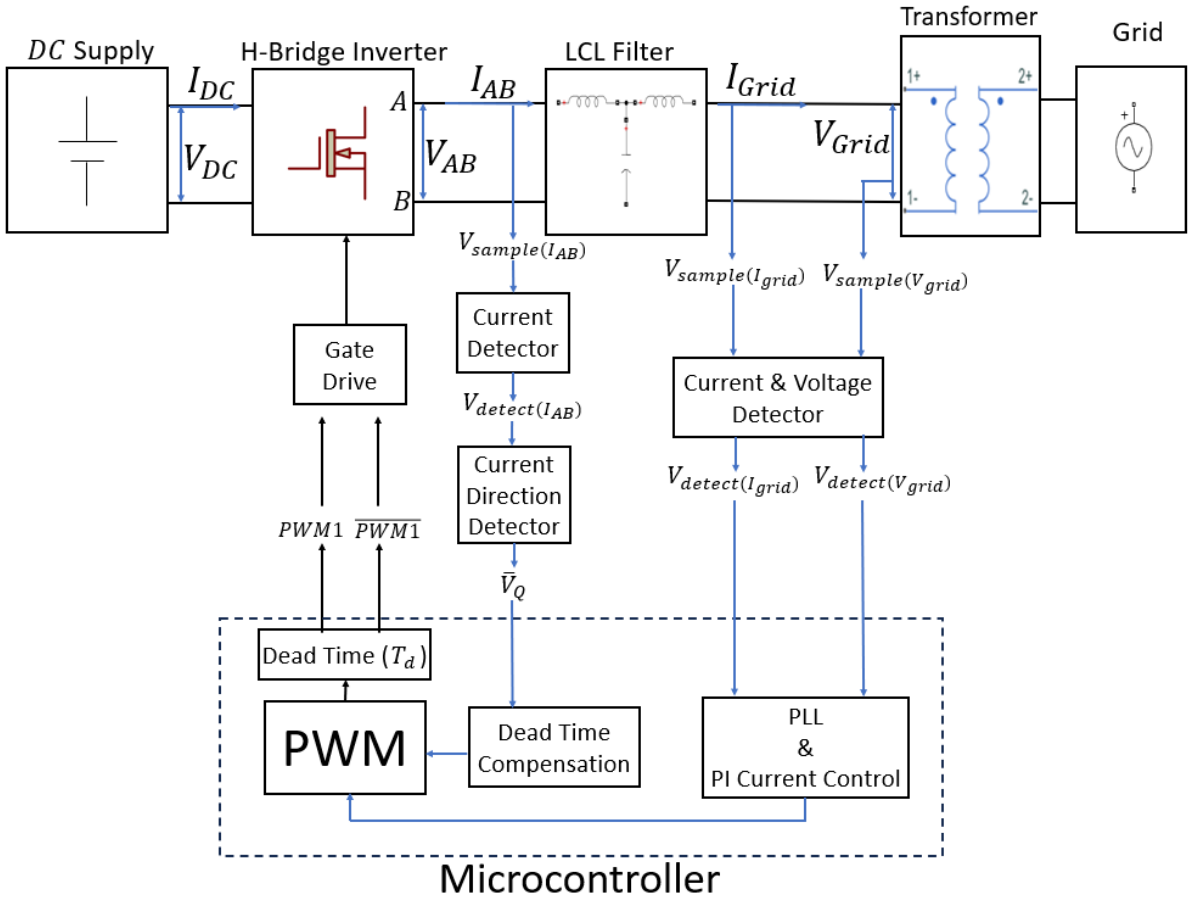


**Figure 4-1: Block Diagram of grid connected power inverter circuit.**

# 4.1 Design of *LCL* filter

The ***LCL*** filter shown in **Figure 4-2** is connected between the inverter output $\boldsymbol{V_{AB}}$ and grid $\boldsymbol{V_{grid}}$ and is used to attenuate the ***PWM*** harmonics to an acceptable level. It is essential that the filter is carefully designed to ensure adequate filtering while not introducing unwanted resonant behavior. The filter provides multiple functions:

i) Converts $\boldsymbol{V_{AB}}$ from SPWM to a sinewave

ii) Attenuates high frequency components of $\boldsymbol{I_{grid}}$ so the grid current is sinusoidal

iii) Limits the rate of the change $\boldsymbol{I_{AB}}$ to provide controllable dynamics for inverter

iv) Provides enough energy for maintaining current flow direction and voltage level during dead time.

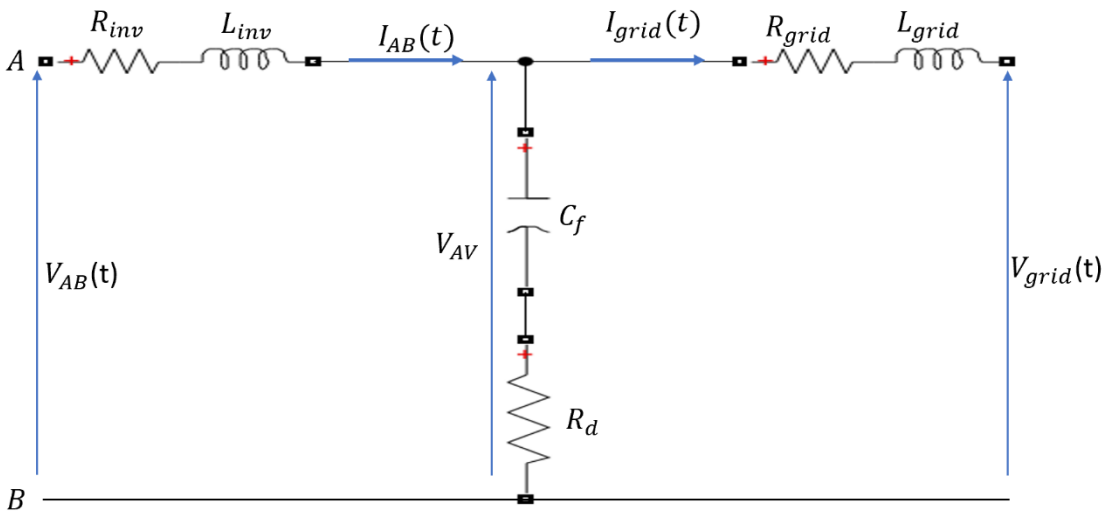


**Figure 4-2 : A basic electrical circle of *LCL* filter.**

Equation (49) and (50) show the inverter voltage to grid current transfer function of ***LCL*** filter with and without damping resistor. Without the damping resistor the filter will exhibit unwanted resonant behavior, and this is not desirable since it can cause excessive energy flow and destabilize the control system. Equation (51) shows how to calculate the resonance frequency of ***LCL*** filter. The resonance frequency should be larger than 10 times of fundamental frequency and lower than half of switching frequency [48][50].

$$\boldsymbol{H_{LCL}(s) = \frac{I_{grid}(s)}{V_{AB}(s)} = \frac{1}{(L_{inv} * L_{grid} * C_f)s^3 + (L_{inv} + L_{grid})s}} \quad (49)$$

$$\boldsymbol{H_{LCL(damping)}(s) = \frac{I_{grid}(s)}{V_{AB}(s)} = \frac{C_f * R_d + 1}{(L_{inv} * L_{grid} * C_f)s^3 + (C_f * (L_{inv} + L_{grid}) * R_d)s^2 + (L_{inv} + L_{grid})s}} \quad (50)$$

$$\boldsymbol{\omega_{res} = \sqrt{\frac{L_{inv} + L_{grid}}{L_{inv} * L_{grid} * C_f}}} \quad (51)$$

**Figure 4-3** shows the block diagram of Grid connected H-Bridge inverter and **Table 5** introduces the parameters in inverter system which will be used for designing the ***LCL*** filter.

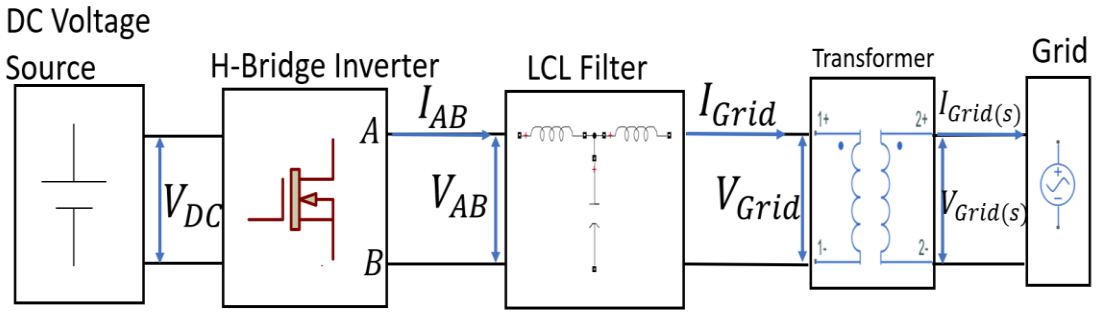


**Figure 4-3 : Block diagram of Grid connected H-Bridge inverter.**

**Table 5 : Parameter in the $LCL$ filter design.**

| Parameter | Symbol | Value |
|---|---|---|
| **Grid Voltage** | $V_{grid}$ | $50(V_{rms})$ |
| **Secondary Grid Voltage** | $V_{grid(s)}$ | $230(V_{rms})$ |
| **Grid Current** | $I_{grid}$ | $10(A_{rms})$ |
| **$DC$ Supply Voltage** | $V_{DC}$ | $100(V)$ |
| **Rated Power** | $S$ | $500(VA)$ |
| **Fundamental frequency** | $f_{sin}$ | $50(Hz)$ |
| **$SPWM$ frequency** | $f_{pwm}$ | $20k(Hz)$ |
| **Max Current Ripple** | | **10%** |

In this research, a transformer is used to transfer the output voltage after $LCL$ filter ($V_{grid}$) into the grid net ($V_{grid(s)}$) system. The design of $LCL$ filter is related to the parameter supplied in **Table 5** and the design of it will be introduced step by step in this section.

# 4.1.1 Inverter side inductor $L_{inv}$ design

Since the switching frequency is much higher than the resonance frequency. The impedance of $C_f$ is ignored and the resistor $R_d$ is ignored. As result, $L_{inv}$ is main inductor to filter the high frequency ripple.

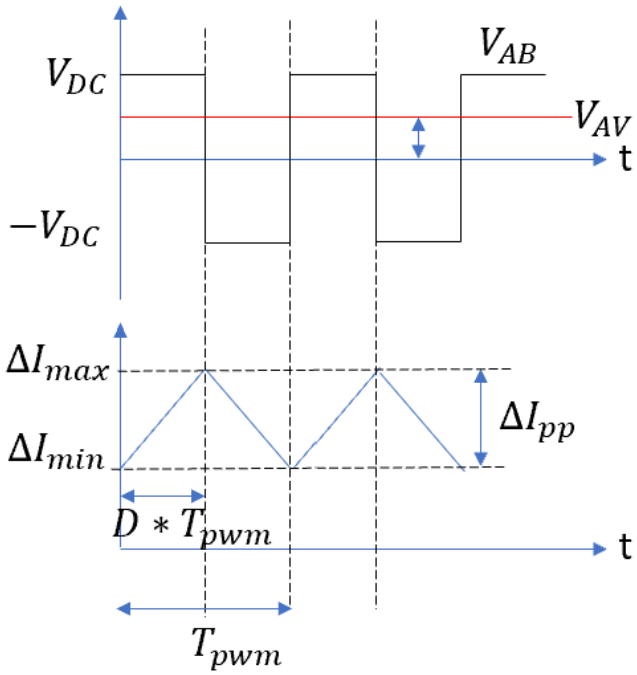


**Figure 4-4 : inverter side inductor voltage and max current ripple.**

Because the switching frequency is much higher than the fundamental frequency, the voltage $\boldsymbol{V_{AV}}$ is the voltage after filter which can be seen as the fundamental voltage $\boldsymbol{V_{inv}}$. The voltage on inverter side inductor $\boldsymbol{L_{inv}}$ is equal to $\boldsymbol{V_{AB} - V_{inv}}$, $\boldsymbol{V_{L_{inv}} = V_{AB} - V_{inv}}$.

By using the equation for the inductor, voltage and ripple current, the ripple current can be calculated as shown in the equation (52) and (53). The $\boldsymbol{D}$ is the duty cycle.

$$\boldsymbol{V_{AB} - V_{AV} = V_{DC} - V_{inv} = L_{inv} * \frac{\Delta I_{pp}}{D * T_{pwm}}} \tag{52}$$

$$\boldsymbol{\Delta I_{pp} = \frac{D * T_{pwm} * (V_{DC} - V_{inv})}{L_{inv}}} \tag{53}$$

**Since,**

$$\boldsymbol{V_{inv} = V_{DC} * D = V_{DC} * m_i = V_{DC} * \frac{\hat{V}_{sin}}{\hat{V}_{tri}} * sin(\omega_{sin} t)}$$

$$\Delta \boldsymbol{I_{pp}} = \frac{\frac{\widehat{\boldsymbol{V}}_{\boldsymbol{sin}}}{\widehat{\boldsymbol{V}}_{\boldsymbol{tri}}} * \boldsymbol{sin}(\boldsymbol{\omega_{sin}t}) * \boldsymbol{T_{pwm}} * \boldsymbol{V_{DC}} * \left(\mathbf{1} - \frac{\widehat{\boldsymbol{V}}_{\boldsymbol{sin}}}{\widehat{\boldsymbol{V}}_{\boldsymbol{tri}}} * \boldsymbol{sin}(\boldsymbol{\omega_{sin}t})\right)}{\boldsymbol{L_{inv}}} \tag{54}$$

The calculation of duty cycle and fundamental voltage has been explained in the previous chapter. The final calculation of ripple current is shown in the equation (54). Differentiating (54) allows the maximum ripple value to be found. Then the $\boldsymbol{I_{pp(\max)}}$ can be found when $\mathbf{sin}(\boldsymbol{\omega_{sin}t}) = \frac{\mathbf{1}}{\mathbf{2}\frac{\widehat{V}_{sin}}{\widehat{V}_{tri}}}$. As result, the equation of maximum ripple current is shown in equation (55), and the inverter side induction can be calculated in equation (56).

$$\Delta \boldsymbol{I_{pp(MAX)}} = \frac{\boldsymbol{T_{pwm}} * \boldsymbol{V_{DC}}}{\mathbf{4} * \boldsymbol{L_{inv}}} \tag{55}$$

$$\boldsymbol{L_{inv}} = \frac{\boldsymbol{V_{DC}}}{\mathbf{4} * \boldsymbol{f_{pwm}} * \Delta \boldsymbol{I_{pp(MAX)}}} \tag{56}$$

According to the reference [50], the current ripple should be kept lower than 5% to 10%. A value of 10% is chosen in this research. Max current ripple of $\boldsymbol{I_{grid}}$ occurs when it reaches to $\hat{\boldsymbol{I}}_{\boldsymbol{grid}}$. As the result, the $\Delta \boldsymbol{I_{pp(MAX)}} = \boldsymbol{I_{grid(rms)}} * \sqrt{\mathbf{2}} * \mathbf{10}\%$. The $\boldsymbol{V_{DC}}$ is $\mathbf{100}\boldsymbol{V}$ and $\boldsymbol{I_{grid(rms)}}$ is $\mathbf{10}\boldsymbol{A}$, $\boldsymbol{f_{pwm}}$ is 20kHz. Then the $\boldsymbol{L_{inv}} = \mathbf{0.9}\boldsymbol{mH}$.

## 4.1.2 Capacitor $C_f$ design

The capacitor $\boldsymbol{C_f}$ is used to suppress the reactive power from total rated power from grid. The reactive power should be limited 5% to 10% of the rated power [48]. Equation

(57) shows the relationship of for the reactive power, $\boldsymbol{Q}$, of $\boldsymbol{C_f}$. Since reactive power $\boldsymbol{Q}$ should be 5% of rated power $\boldsymbol{S}$, the value of $\boldsymbol{C_f}$ can be calculated by equation (58).

$$\boldsymbol{Q} = \frac{(\boldsymbol{V_{grid(rms)}})^2}{\frac{\boldsymbol{1}}{\boldsymbol{2\pi f_{grid} * C_f}}} \tag{57}$$

$$\boldsymbol{C_f} = \frac{\boldsymbol{S} * \boldsymbol{5\%}}{(\boldsymbol{V_{grid(rms)}})^2 * \boldsymbol{2\pi f_{grid}}} \tag{58}$$

The rated power of grid is equal to $\boldsymbol{500VA}$, $\boldsymbol{V_{grid(rms)} = 50V}$ and $\boldsymbol{f_{grid} = 50Hz}$. The $\boldsymbol{C_f = 31.8uF}$.

# 4.1.3 Grid side inductor ($L_{grid}$) design

The total inductance of $\boldsymbol{L_{inv}}$ and $\boldsymbol{L_{grid}}$ should be as small as possible to limit the voltage drop on the inductors. With a low fundamental frequency, the $\boldsymbol{C_f}$ can be treated like an open circuit, only $\boldsymbol{L_{inv}}$ and $\boldsymbol{L_{grid}}$ need to be considered. The voltage drop on the total inductor should be lower than 10% from grid voltage. The impedance of series inductor can be calculated as $\boldsymbol{2\pi * f_{grid} * (L_{inv} + L_{grid})}$. Then the voltage on total inductor can be calculated by equation (59). Since the $\boldsymbol{I_{rated}}$ is equal to $\frac{\boldsymbol{S}}{\boldsymbol{V_{grid(rms)}}}$, the total inductance can be calculated by equation (60).

$$\boldsymbol{V_{drop} = I_{rated(rms)} * 2\pi * f_{grid} * (L_{inv} + L_{grid}) = 10\% * V_{grid(rms)}} \tag{59}$$

$$\boldsymbol{L_{inv} + L_{grid}} = \frac{\boldsymbol{10\% * V_{grid(rms)}}}{\frac{\boldsymbol{S}}{\boldsymbol{V_{grid(rms)}}} * \boldsymbol{2\pi * f_{grid}}} = \frac{\boldsymbol{10\% * V_{grid(rms)}^2}}{\boldsymbol{S * 2\pi * f_{grid}}} \tag{60}$$

According to all parameters known the $\boldsymbol{L_{Total} = 1.59mH}$ and $\boldsymbol{L_{grid} = 0.69mH}$.

Now according to resonant frequency $\boldsymbol{\omega_{res}}$ equation in (51), $\boldsymbol{f_{res} = 1446Hz}$ which is higher than 10 times of $\boldsymbol{f_{grid}}$ and lower than half of $\boldsymbol{f_{pwm}}$ [48][50], and so meets the design requirements.

### 4.1.4 Damping resistor $R_d$ design.

The damping resistor is used for decreasing the influence the resonance caused by $\boldsymbol{LCL}$ filter. The resistor should not be large for avoiding energy loss and filter efficiency of $\boldsymbol{LCL}$. Equation (61) shows the method for calculating the damping resistor.

$$\boldsymbol{R_d = \frac{1}{2\pi f_{pwm} * C_f}} \tag{61}$$

The $\boldsymbol{R_d}$ is equal to 0.25Ω.

According to Equation (49), the bode diagram of $\boldsymbol{LCL}$ without damping resistor is shown in **Figure 4-5**. According to equation (50), the bode diagram of $\boldsymbol{LCL}$ with damping resistor is shown in **Figure 4-6**.

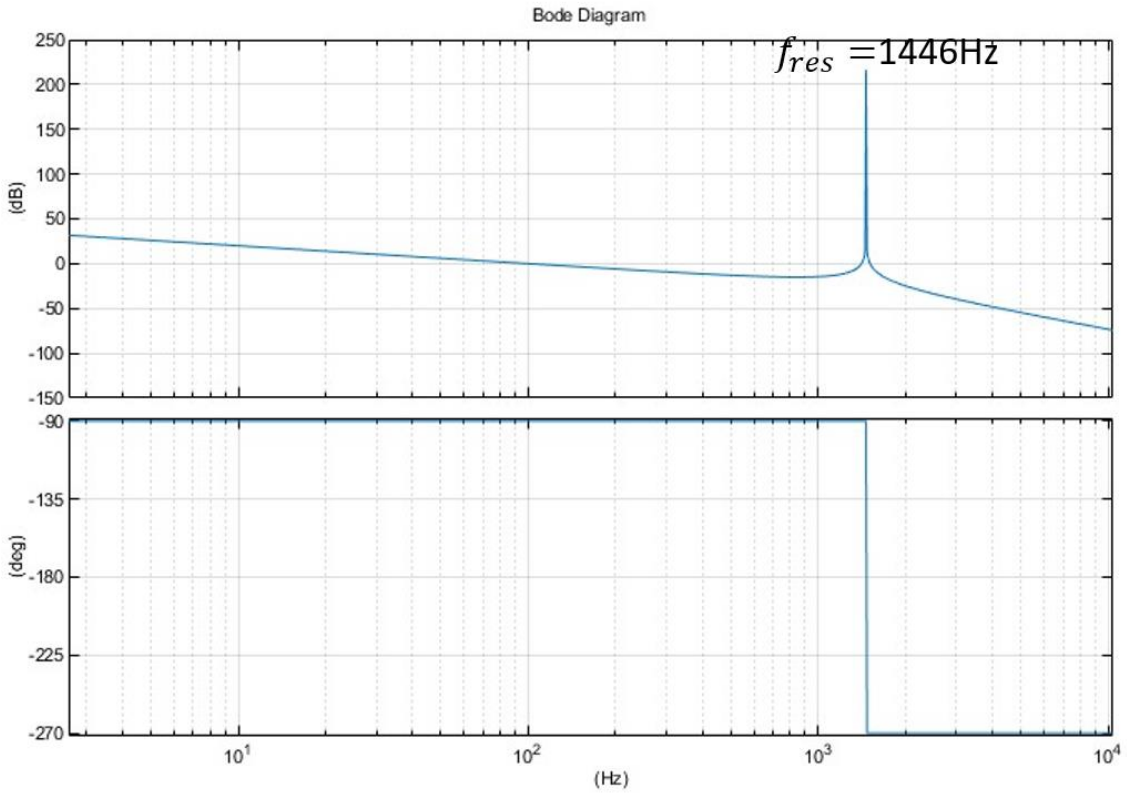


**Figure 4-5 : Bode diagram of $LCL$ without damping resistor.**

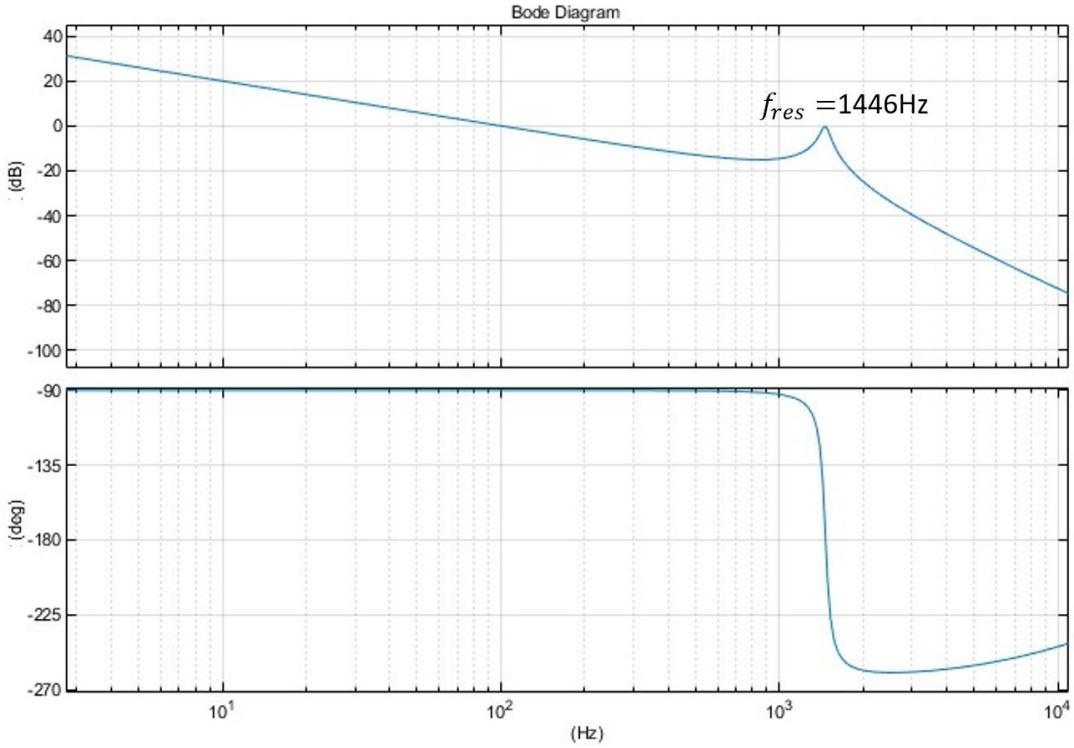


**Figure 4-6 : Bode diagram of $LCL$ with damping resistor.**

The advantage of $\boldsymbol{LCL}$ filter is its high -60dB/dec after the resonance frequency, which provide good low-pass filter for high switching frequency. Comparing the $\boldsymbol{LCL}$ system with and without damping resistor, the high gain at $\boldsymbol{f_{res}}$ is decreased from 200dB to 0dB. As result, the instability system caused by the resonance frequency form $\boldsymbol{LCL}$ will be damped by the $\boldsymbol{R_d}$.

# 4.2 Grid Connected Power Inverter System

## 4.2.1 Phase Locked Loop ($\boldsymbol{PLL}$)

In $\boldsymbol{PLL}$ system, the angle between $\boldsymbol{d}$-axis and $\boldsymbol{\alpha}$-axis represents the grid angle, and the value on $\boldsymbol{q}$-axis is kept at 0. As shown in **Figure 4-7**, the $\boldsymbol{\theta_{grid}}$ and $\boldsymbol{V_{grid}}$ represent the actual grid voltage angle and vector voltage. The $\boldsymbol{\widehat{\theta}_{grid}}$ is the angle between $\boldsymbol{d}$-axis voltage and $\boldsymbol{\alpha}$-axis which is calculated from the $\boldsymbol{PLL}$ system, the $\boldsymbol{\widehat{d}}$ and $\boldsymbol{\widehat{q}}$ are $\boldsymbol{dq}$ axis from $\boldsymbol{PLL}$.

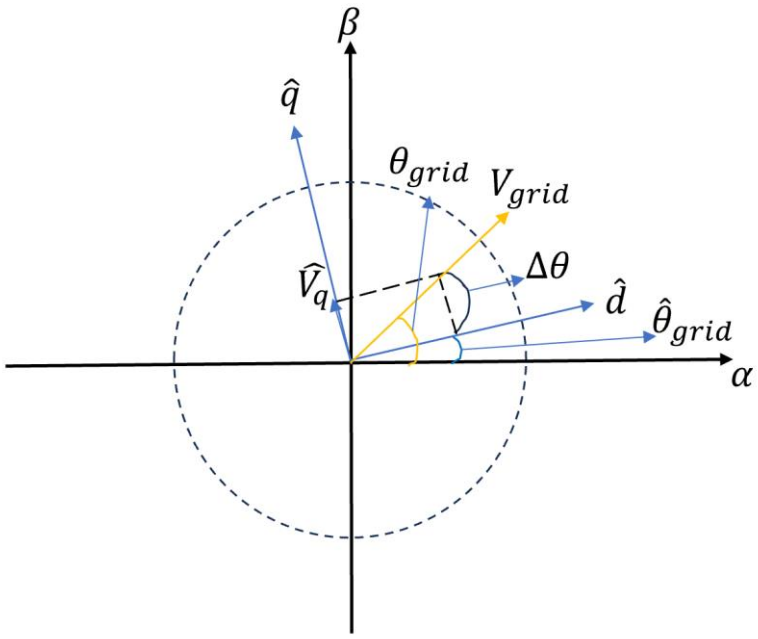


**Figure 4-7 : $dq$ reference frame in $PLL$ system of grid.**

Here $\Delta\boldsymbol{\theta} = \boldsymbol{\theta_{grid}} - \widehat{\boldsymbol{\theta}}_{\boldsymbol{grid}}$ is the error between the actual grid angle and angle estimated by the $\boldsymbol{PLL}$. The $\boldsymbol{q}$ axis voltage $\widehat{\boldsymbol{V}}_{\boldsymbol{q}}$ is given by equation (62)

$$\widehat{\boldsymbol{V}}_{\boldsymbol{q}} = \boldsymbol{V_{grid}} * \boldsymbol{sin}(\Delta\boldsymbol{\theta}) \tag{62}$$

Assuming $\Delta\boldsymbol{\theta}$ is very small, then the $\widehat{\boldsymbol{V}}_{\boldsymbol{q}}$ can be calculated in equation (63)

$$\widehat{\boldsymbol{V}}_{\boldsymbol{q}} = \boldsymbol{V_{grid}} * \Delta\boldsymbol{\theta} \tag{63}$$

Since $\Delta\boldsymbol{\theta} = \boldsymbol{\theta_{grid}} - \widehat{\boldsymbol{\theta}}_{\boldsymbol{grid}}$, the block diagram of $\boldsymbol{PLL}$ closed loop is shown in **Figure 4-8**. As described previously, the $\boldsymbol{PLL}$ produces grid angle achieved by keeping the $\widehat{\boldsymbol{V}}_{\boldsymbol{q}}$ to 0 through $\boldsymbol{PI}$ compensation. The $\widehat{\boldsymbol{V}}_{\boldsymbol{q}}$ should kept same to the reference voltage $\boldsymbol{V_{q(ref)}}$. So, the $-\widehat{\boldsymbol{V}}_{\boldsymbol{q}}$ keep same to the $-\boldsymbol{V_{q(ref)}}$ which is shown in **Figure 4-8** (b). Because the $\boldsymbol{V_{q(ref)}}$ is $\mathbf{0}$, **Figure 4-8** (c) shows the final equivalent block diagram of $\boldsymbol{PLL}$. The input of $\boldsymbol{PI}$ compensator is equal to $+\widehat{\boldsymbol{V}}_{\boldsymbol{q}} - \mathbf{0}$.

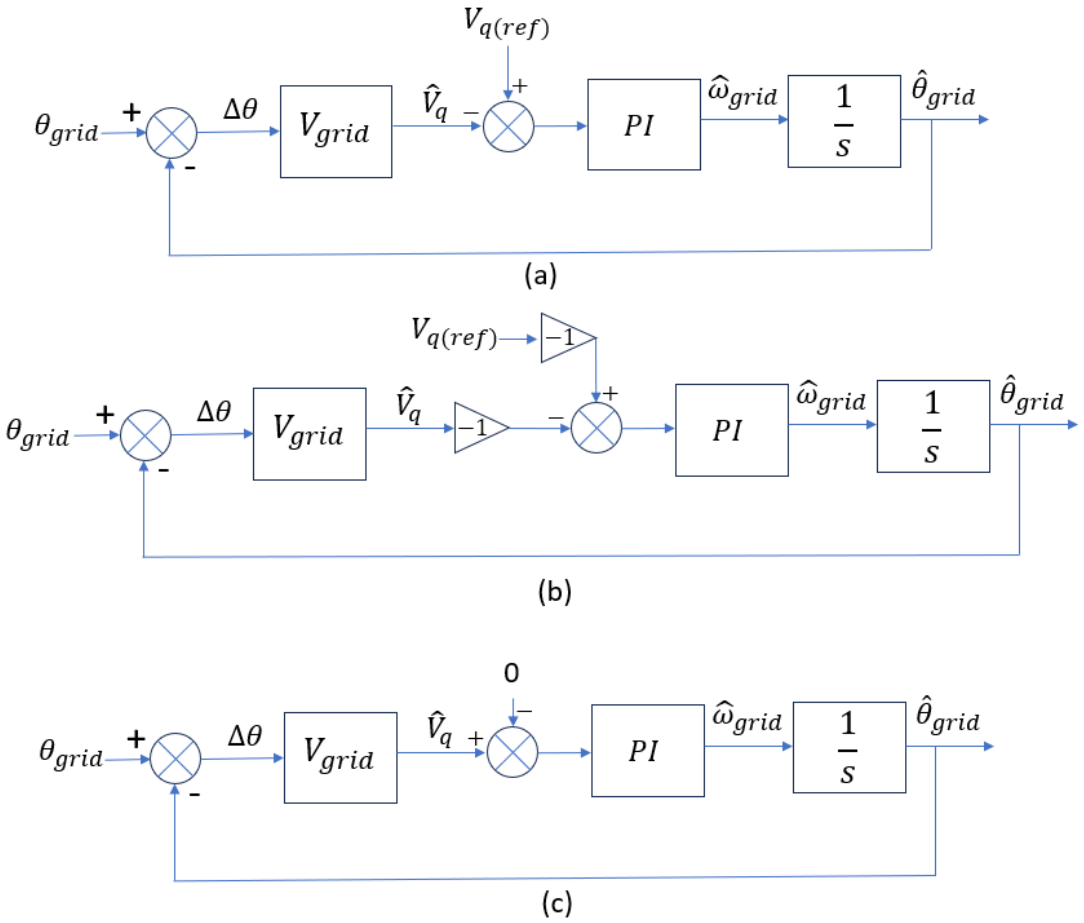


**Figure 4-8 : Block diagram of *PLL* loop.**

The close-loop transfer function of ***PLL*** is shown in equation (64).

$$\boldsymbol{H_{close}(s) = \frac{K_{PI(PLL)}(s) * V_{grid}}{s + K_{PI(PLL)}(s) * V_{grid}}} \tag{64}$$

The gain of ***PI*** $\boldsymbol{K_{PI(PLL)}}$ is shown in equation (65).

$$\boldsymbol{K_{PI(PLL)}(s) = K_{p(PLL)} + \frac{K_{i(PLL)}}{s}} \tag{65}$$

Putting the gain of $\boldsymbol{K_{PI(PLL)}}$ into the close-loop transfer function for the ***PLL*** is,

$$H_{close}(s) = \frac{V_{grid} * K_{p(PLL)} * s + V_{grid} * K_{i(PLL)}}{s^2 + V_{grid} * K_{p(PLL)} * s + V_{grid} * K_{i(PLL)}} \quad (66)$$

Since it is a second-order system, comparing it to a standard second-order system allows coefficients to be chosen:

$$s^2 + V_{grid} * K_{p(PLL)} * s + V_{grid} * K_{i(PLL)} = s^2 + 2 * \zeta * \omega_n * s + {\omega_n}^2 \quad (67)$$

Then, according to equation (68) and (69), the value of $K_{p(PLL)}$ and $K_{i(PLL)}$ in $PI$ system can be calculated.

$$K_{p(PLL)} = \frac{2 * \zeta * \omega_n}{V_{grid}} \quad (68)$$

$$K_{i(PLL)} = \frac{{\omega_n}^2}{V_{grid}} \quad (69)$$

In these two equations, $\zeta$ is damping ratio and $\omega_n$ is natural frequency. The $\omega_n$ is equal to the fundamental frequency $\omega_{sin}$. The damping ration $\zeta$ can be calculated according to overshoot desired in $PI$ calculation [80]-[83]. Normally, damping ratio is set as $0.707$ [82][83]. The value $V_{grid}$ here will taking the peak voltage of grid voltage $\widehat{V}_{grid}$

## 4.2.2 *PI* current control

As described before about the $\boldsymbol{PI}$ current controller in power grid connected system, the whole system consists of the $\boldsymbol{\alpha\beta}$ to $\boldsymbol{dq}$ system, $\boldsymbol{PI}$ calculation and decoupling system.

In single-phase grid system, the grid current is transformed from to $\boldsymbol{I_{grid(\alpha)}}$ to $\boldsymbol{I_{grid(\beta)}}$ by delaying $\boldsymbol{I_{grid(\alpha)}}$ by $\frac{\boldsymbol{\pi}}{\boldsymbol{2}}$. Because the fundamental frequency of grid is low, the impedance of capacitor $\boldsymbol{C_f}$ in $\boldsymbol{LCL}$ filter can be assumed be an open circuit. In the $\boldsymbol{PI}$ current control calculation, only the impedance of filter inductors should be considered. The relationship between the inverter side fundamental voltage, grid current and grid side voltage is,

$$\boldsymbol{V_{inv}} = \boldsymbol{R_T} * \boldsymbol{I_{grid}} + \frac{\boldsymbol{d}}{\boldsymbol{dt}} * \boldsymbol{L_T} * \boldsymbol{I_{grid}} + \boldsymbol{V_{grid}} \tag{70}$$

Here $\boldsymbol{R_T}$ is the total resistance of $\boldsymbol{R_{inv}}$ and $\boldsymbol{R_{grid}}$, while $\boldsymbol{L_T}$ is the total inductance of $\boldsymbol{L_{inv}}$ and $\boldsymbol{L_{grid}}$. In the $\boldsymbol{\alpha\beta}$ reference frame. Then the $\boldsymbol{V_{inv(\alpha\beta)}}$ can be transferred to $\boldsymbol{dq}$ frame by equation (72).

$$\boldsymbol{V_{inv(\alpha,\beta)}} = \boldsymbol{R_T} * \boldsymbol{I_{grid(\alpha,\beta)}} + \frac{\boldsymbol{d}}{\boldsymbol{dt}} * \boldsymbol{L_T} * \boldsymbol{I_{grid(\alpha,\beta)}} + \boldsymbol{V_{grid(\alpha,\beta)}} \tag{71}$$

$$\boldsymbol{V_{inv(dq)}} = [\boldsymbol{T}]\boldsymbol{V_{inv(\alpha,\beta)}} \tag{72}$$

The $[\boldsymbol{T}]$ is the park transformer function. With equation (71) and park transfer function, the progress of $\boldsymbol{dq}$ transfer is shown from equation (73) to equation (79).

$$[\boldsymbol{T}]\left[\boldsymbol{V_{inv(\alpha\beta)}}\right] = [\boldsymbol{T}][\boldsymbol{R}][\boldsymbol{T}][\boldsymbol{T}]^{-1}\left[\boldsymbol{I_{grid(\alpha\beta)}}\right] + [\boldsymbol{T}]\frac{\boldsymbol{d}}{\boldsymbol{dt}}\left\{[\boldsymbol{L}][\boldsymbol{T}][\boldsymbol{T}]^{-1}\left[\boldsymbol{I_{grid(\alpha\beta)}}\right]\right\} + [\boldsymbol{T}]\left[\boldsymbol{V_{grid(\alpha\beta)}}\right] \tag{73}$$

$$\left[\boldsymbol{V_{inv(dq)}}\right] = [\boldsymbol{R}]\left[\boldsymbol{I_{grid(dq)}}\right] + [\boldsymbol{T}][\boldsymbol{L}]\frac{\boldsymbol{d}}{\boldsymbol{dt}}\left\{[\boldsymbol{T}]^{-\mathbf{1}}\left[\boldsymbol{I_{grid(dq)}}\right]\right\} + \left[\boldsymbol{V_{grid(dq)}}\right] \quad (74)$$

$$\left[\boldsymbol{V_{inv(dq)}}\right] = [\boldsymbol{R}]\left[\boldsymbol{I_{grid(dq)}}\right] + [\boldsymbol{T}]\frac{\boldsymbol{d}}{\boldsymbol{dt}}\{[\boldsymbol{T}]^{-\mathbf{1}}\}[\boldsymbol{L}]\left[\boldsymbol{I_{grid(dq)}}\right] + [\boldsymbol{T}][\boldsymbol{L}][\boldsymbol{T}]^{-\mathbf{1}}\frac{\boldsymbol{d}}{\boldsymbol{dt}}\left\{\boldsymbol{I_{grid(dq)}}\right\} + \left[\boldsymbol{V_{grid(dq)}}\right] \quad (75)$$

$$[\boldsymbol{R}] = \begin{bmatrix}\boldsymbol{R_T} & \mathbf{0}\\ \mathbf{0} & \boldsymbol{R_T}\end{bmatrix}, [\boldsymbol{L}] = \begin{bmatrix}\boldsymbol{L_T} & \mathbf{0}\\ \mathbf{0} & \boldsymbol{L_T}\end{bmatrix}, [\boldsymbol{T}]\frac{\boldsymbol{d}}{\boldsymbol{dt}}[\boldsymbol{T}]^{-\mathbf{1}} = \begin{bmatrix}\mathbf{0} & -\boldsymbol{\omega_{grid}}\\ \boldsymbol{\omega_{grid}} & \mathbf{0}\end{bmatrix}, [\boldsymbol{T}][\boldsymbol{T}]^{-\mathbf{1}} = \begin{bmatrix}\mathbf{1} & \mathbf{0}\\ \mathbf{0} & \mathbf{1}\end{bmatrix} \quad (76)$$

$$\begin{bmatrix}\boldsymbol{V_{inv(d)}}\\ \boldsymbol{V_{inv(q)}}\end{bmatrix} = \begin{bmatrix}\boldsymbol{R_T} & -\boldsymbol{\omega L_T}\\ \boldsymbol{\omega L_T} & \boldsymbol{R_T}\end{bmatrix}\begin{bmatrix}\boldsymbol{I_{grid(d)}}\\ \boldsymbol{I_{grid(q)}}\end{bmatrix} + \begin{bmatrix}\boldsymbol{L_T} & \mathbf{0}\\ \mathbf{0} & \boldsymbol{L_T}\end{bmatrix}\frac{\boldsymbol{d}}{\boldsymbol{dt}}\begin{bmatrix}\boldsymbol{I_{grid(d)}}\\ \boldsymbol{I_{grid(q)}}\end{bmatrix} + \begin{bmatrix}\boldsymbol{V_{grid(d)}}\\ \boldsymbol{V_{grid(q)}}\end{bmatrix} \quad (77)$$

$$\boldsymbol{R_T} * \boldsymbol{I_{grid(d)}} + \boldsymbol{L_T} * \frac{\boldsymbol{d}}{\boldsymbol{dt}}\boldsymbol{I_{grid(d)}} = \boldsymbol{V_{inv(d)}} + \boldsymbol{\omega_{grid}}\boldsymbol{L_T} * \boldsymbol{I_{grid(q)}} - \boldsymbol{V_{grid(d)}} \quad (78)$$

$$\boldsymbol{R_T} * \boldsymbol{I_{grid(q)}} + \boldsymbol{L_T} * \frac{\boldsymbol{d}}{\boldsymbol{dt}}\boldsymbol{I_{grid(q)}} = \boldsymbol{V_{inv(q)}} - \boldsymbol{\omega_{grid}}\boldsymbol{L_T} * \boldsymbol{I_{grid(d)}} - \boldsymbol{V_{grid(q)}} \quad (79)$$

According to equation (78) and (79), the system of $\boldsymbol{dq}$ frame is shown in **Figure 4-9**.

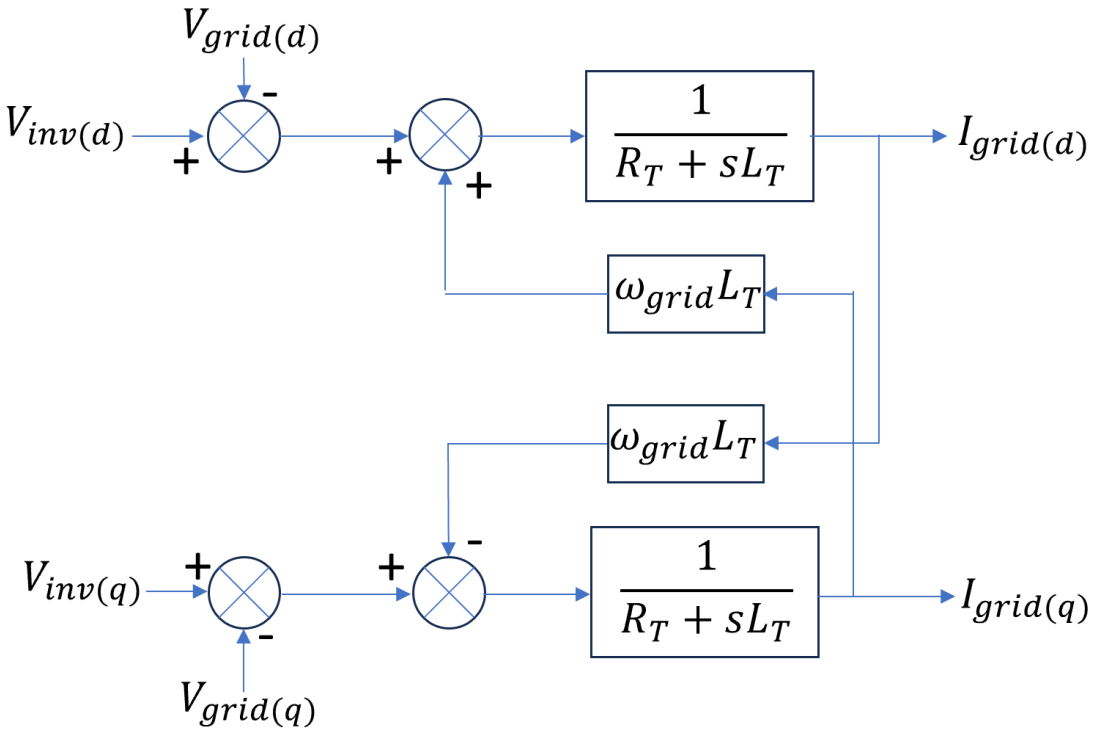


**Figure 4-9 : Block diagram about inverter and grid side voltage and current in $dq$ frame.**

As shown in **Figure 4-9**, there is a cross-coupling between the $\boldsymbol{d}$ & $\boldsymbol{q}$ axis grid currents caused by the $\boldsymbol{\omega_{grid}L_T}$ term. In order to make decoupled close-loop control of current $\boldsymbol{I_{grid(d)}}$ and $\boldsymbol{I_{grid(q)}}$, the inverter side voltage should be controlled as follows,

$$\boldsymbol{V_{inv(d)} = V_{con(d)} - \omega L_T * I_{grid(q)} + V_{grid(d)}} \quad (80)$$

$$\boldsymbol{V_{inv(q)} = V_{con(q)} + \omega L_T * I_{grid(d)} + V_{grid(q)}} \quad (81)$$

The $\boldsymbol{V_{con(d)}}$ and $\boldsymbol{V_{con(q)}}$ are calculated voltages produced from the $\boldsymbol{PI}$ compensator in current control. Adopting equation (80) and (81), the block diagram of decoupling system in current control is shown in **Figure 4-10**.

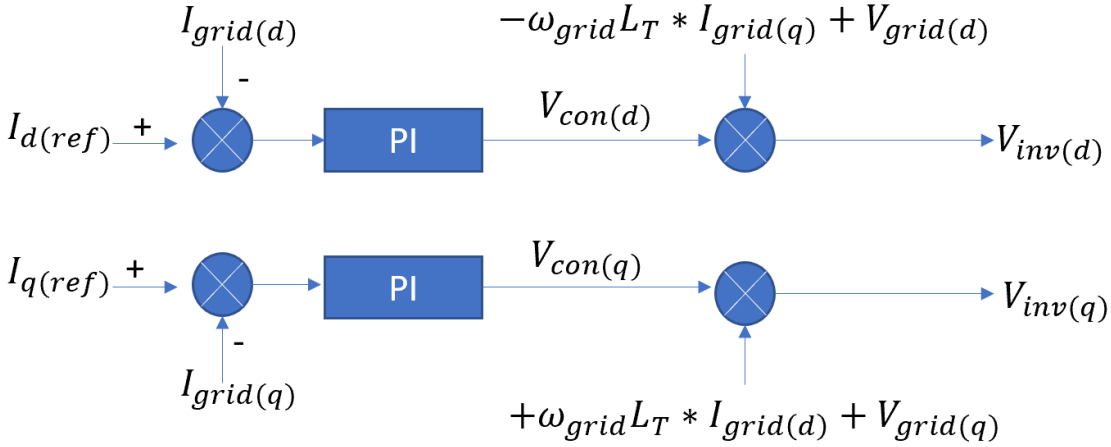


**Figure 4-10 : Block diagram of decoupling system.**

Now, combining the control and hardware platform system from block diagram in **Figure 4-10** and **Figure 4-9**, and after decoupling, only the ***PI*** and impedance $\frac{1}{R_T+sL_T}$ are remaining as shown in **Figure 4-11**.

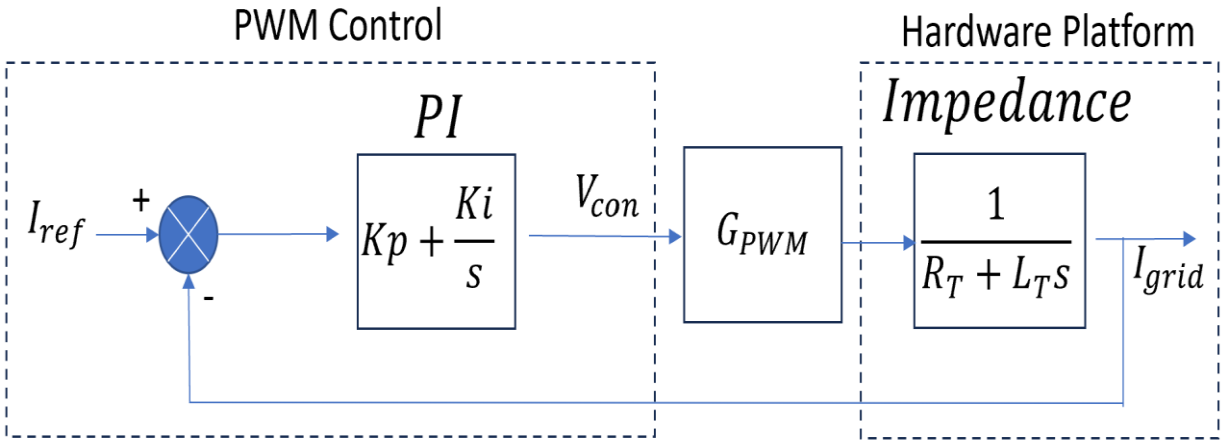


**Figure 4-11 : Close loop of *PI* current Control system.**

In **Figure 4-11**, the $G_{PWM}$ is the gain between the value from the ***PI*** and ***PWM*** control with the actual output from the inverter. It represents the energy loss on the switches in inverter. In this research, the $G_{PWM}$ is assumed to be **1**, which the low energy loss on the switches can be ignored.

The closed loop transfer function of ***PI*** current control is applied as equation.

$$\boldsymbol{H_{PI(close)}(s) = \frac{K_{p(PI)}s + K_{i(PI)}}{L_T s^2 + (R_T + K_{p(PI)})s + K_{i(PI)}}} \tag{82}$$

Now, the $\boldsymbol{s^2 + \frac{R_T + K_{p(PI)}}{L_T}s + \frac{K_{i(PI)}}{L_T}}$ is another standard second-order system which can be related to the second-order prototype $\boldsymbol{s^2 + 2 * \zeta * \omega_n * s + {\omega_n}^2}$. As result, the $\boldsymbol{K_{p(PI)}}$ and $\boldsymbol{K_{i(PI)}}$ can be calculated in the equation (83) and (84).

$$\boldsymbol{K_{p(PI)} = 2 * \zeta * \omega_n * L_T - R_T} \tag{83}$$

$$\boldsymbol{K_{i(PI)} = L_T * {\omega_n}^2} \tag{84}$$

The value chooses of damping ration $\boldsymbol{\zeta}$ and $\boldsymbol{\omega_n}$ is same to the description in previous section 4.2.1.

The whole system of Grid connected power inverter is shown in **Figure 4-12**.

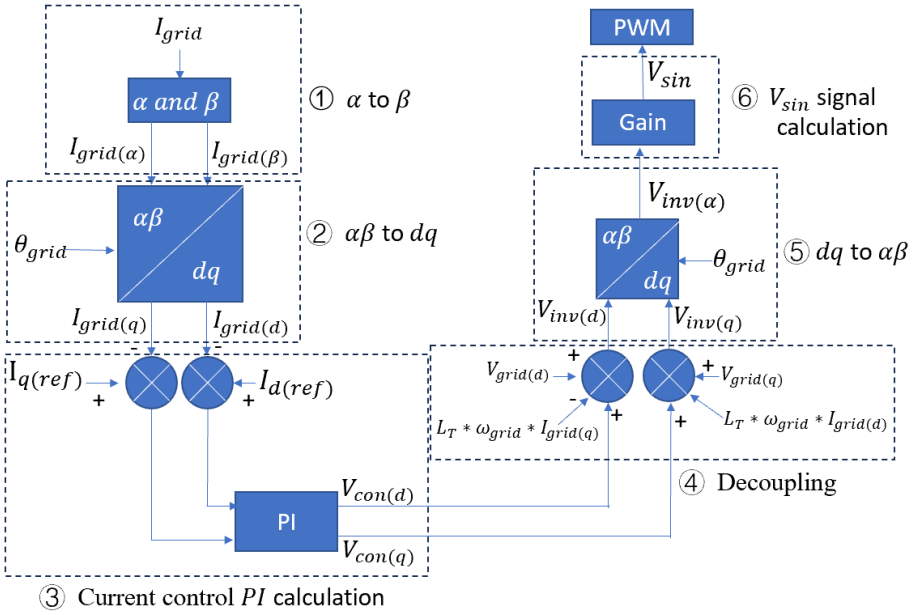


**Figure 4-12 : Block Diagram of whole *PI* current control and *PLL* system.**

# 4.3 Circuit design of H-Bridge inverter

The H-bridge converter consists of two identical bridge legs labelled $\boldsymbol{A}$ & $\boldsymbol{B}$ and their gate drivers and protection circuits.

The H-bridge consists of four IMW65R072M1H MOSFETs, each of which are controlled through their own independent gate driver IC. The 1EDBx275F [132] is a single-channel isolated gate drive IC featuring a bootstrap circuit suitable for driving high-side devices. **Figure 4-13** shows the schematic circuit diagram of gate drive circuit of H-Bridge inverter which is divided into two half-bridge legs $\boldsymbol{A}$ & $\boldsymbol{B}$. It should be noted that the input ($\boldsymbol{PWM1}$) and outputs ($\boldsymbol{A}$&$\boldsymbol{B}$) have isolated grounds, $\boldsymbol{GND1}$ & $\boldsymbol{GND2}$ respectively.

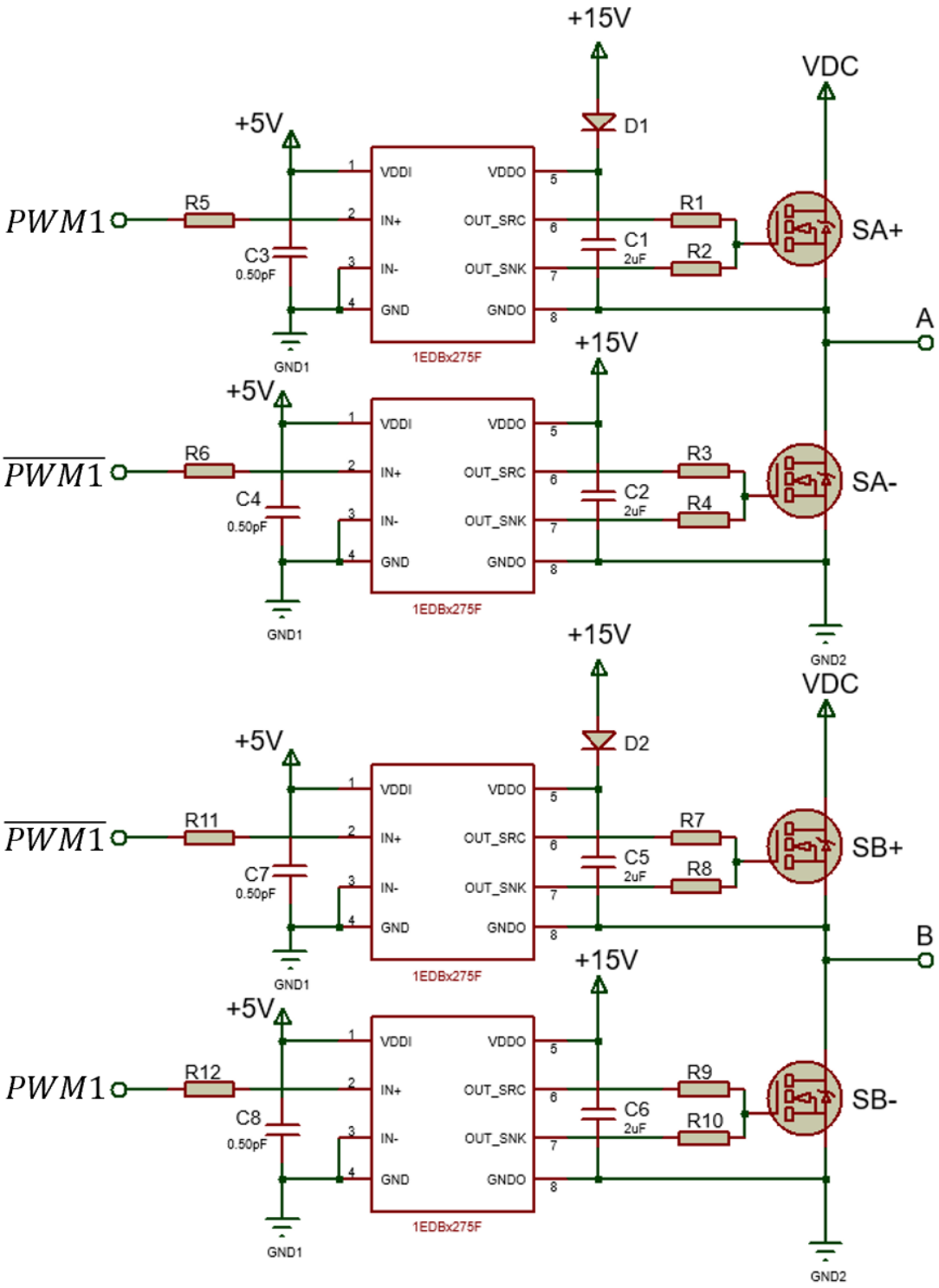


**Figure 4-13 : The schematic circuit diagram of H-Bridge drive circuit**

The 1EDBx275F gate driver IC provides separate source and sink (***OUT_SRC*** and ***OUT_SNK*****)** connections to the MOSFET gate allowing different turn-on and turn-off gate resistor values to be controlled only by the input single on $\boldsymbol{IN+}$ in the chip. The

gate driver input signals $\boldsymbol{PWM1}$ and $\overline{\boldsymbol{PWM1}}$ are produced from the STM32 microcontroller, and they are complementary. The schematic of drive circuit of leg B of H-Bridge is same as that in leg A. The switches $\boldsymbol{SA+}$ and $\boldsymbol{SB-}$ are controlled by $\boldsymbol{PWM1}$, while $\boldsymbol{SA-}$ and $\boldsymbol{SB+}$ are controlled by $\overline{\boldsymbol{PWM1}}$.

As shown in **Figure 4-13**, there are two different grounds which are isolated by the IC. The $\boldsymbol{GND1}$ is the ground for all control system including microcontroller, gate drive IC, detector circuit and protect circuit. The $\boldsymbol{GND2}$ is the ground for main DC power and H-Bridge.

**Figure 4-14** shows the operation of bootstrap circuit in one leg of H-Bridge inverter, the operation on another leg is same.

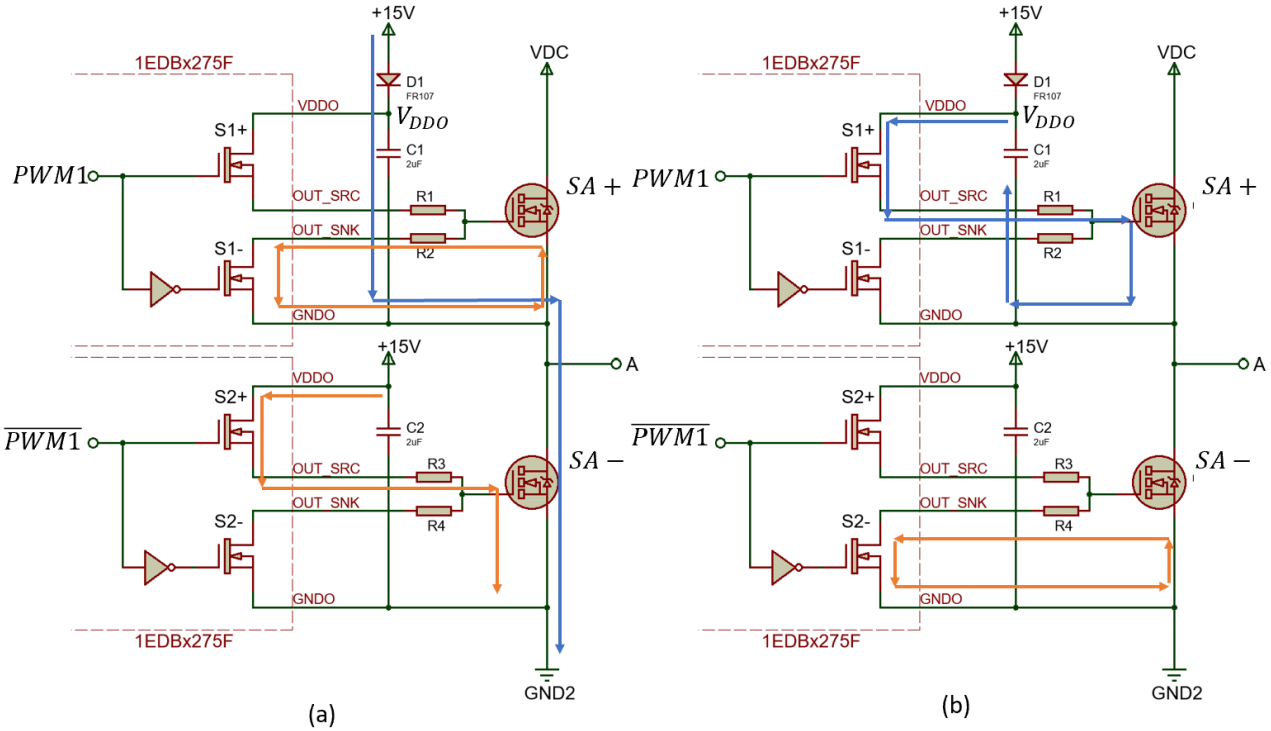


**Figure 4-14 : Current flow in bootstrap circuit (a) When $\boldsymbol{PWM1}$ is low and $\overline{\boldsymbol{PWM1}}$ is high, (b) When $\boldsymbol{PWM1}$ is high and $\overline{\boldsymbol{PWM1}}$ is low.**

The bootstrap circuit is used for driving upper power switches such as $\boldsymbol{SA+}$ and $\boldsymbol{SB+}$. Recalling that a MOSFET switch is turned on when the Gate Source voltage $\boldsymbol{V_{GS}}$ is larger than the MOSFET threshold voltage $\boldsymbol{V_{th(GS)}}$. For the lower side of power switches $\boldsymbol{SA-}$ and $\boldsymbol{SB-}$, their Source pin is connected to the $\boldsymbol{GND2}$ (0V) and as result, it is easy to support enough voltage to turn on the lower side switches. For the upper side switches, for example, if the $\boldsymbol{SA+}$ turns on, the voltage between pin Source and $\boldsymbol{GND2}$ is almost equal to the voltage between $\boldsymbol{A}$ and $\boldsymbol{GND2}$, which should be equal to the $\boldsymbol{VDC}$ if MOSFET SA+ is on. Since $\boldsymbol{V_{GS}}$ should larger than the threshold voltage $\boldsymbol{V_{th(GS)}}$, then voltage between the Gate to $\boldsymbol{GND2}$ should be larger than $\boldsymbol{VDC + V_{th(GS)}}$. To provide sufficient voltage to turn on the upper side switches in H-Bridge inverter, the bootstrap capacitor $\boldsymbol{C1}$ is charged by +15V through the bootstrap diode $\boldsymbol{D1}$ and this voltage is floated on top of the $\boldsymbol{SA+}$ source voltage to drive its gate.

The voltage source $\boldsymbol{+15V}$ is used for driving power switches. As shown in **Figure 4-14**, the inner circuit of 1EDBx275F chips can be seen as an equivalent circuit which is consisted of two power switches with complementary control signal. In **Figure 4-14** (a), the signal $\boldsymbol{PWM1}$ is low and $\boldsymbol{\overline{PWM1}}$ is high, switches $\boldsymbol{S1+}$ and $\boldsymbol{S2-}$ turns off, while $\boldsymbol{S1-}$ and $\boldsymbol{S2+}$ turns on. When $\boldsymbol{S2+}$ turns on, the switch $\boldsymbol{SA-}$ will be turned on by $\boldsymbol{+15V}$ voltage source, while the $\boldsymbol{SA+}$ turns off. At the same time, the voltage at point $\boldsymbol{A}$ is close to 0 because of $\boldsymbol{GND2}$, the bootstrap capacitor $\boldsymbol{C1}$ is charged by the $\boldsymbol{15V}$ voltage source through bootstrap diode $\boldsymbol{D1}$. In **Figure 4-14** (b), the $\boldsymbol{PWM1}$ is high and $\boldsymbol{\overline{PWM1}}$ is low, $\boldsymbol{S1+}$ and $\boldsymbol{S2-}$ are turned on, while $\boldsymbol{S1-}$ and $\boldsymbol{S2+}$ are turned off. The bootstrap capacitor $\boldsymbol{C1}$ has been fully charged. Now, the capacitor $\boldsymbol{C1}$

will be the $+\mathbf{15}\boldsymbol{V}$ voltage source, and the $\boldsymbol{V_{GS}}$ of $\boldsymbol{SA+}$ is same as the voltage on $\boldsymbol{C1}$. Because the $\mathbf{15}\boldsymbol{V}$ is higher than the $\boldsymbol{V_{th(GS)}}$, the switch $\boldsymbol{SA+}$ will be turned on. On the other hand, the voltage $\boldsymbol{V_{DDO}}$ is the voltage on $\boldsymbol{C1}$ to the $\boldsymbol{GND2}$ which is equal to $\boldsymbol{V_{DC}+\mathbf{15}\boldsymbol{V}}$, so the bootstrap diode $\boldsymbol{D1}$ stop the current flow from $\boldsymbol{C1}$ to the $\mathbf{15}\boldsymbol{V}$ voltage source. As result, the DC reverse block voltage for bootstrap diode $\boldsymbol{D1}$ should be at least larger than $\boldsymbol{V_{DC}}$.

The value of bootstrap capacitor $\boldsymbol{C1}$ is the key in the circuit, it is needed to be fully charged during the $\boldsymbol{SA-}$ turns on. During the $\boldsymbol{SA+}$ is turned on, $\boldsymbol{C1}$ should have enough energy to keep $\boldsymbol{V_{GS}}$ is always higher than $\boldsymbol{V_{GS(th)}}$. The value of $\boldsymbol{C1}$ can be calculated by equation (85) [133].

$$\boldsymbol{C1} > \frac{\mathbf{2} * \left[\mathbf{2}\boldsymbol{Q_g} + \frac{\boldsymbol{I_{qbs(max)}}}{\boldsymbol{f}} + \boldsymbol{Q_{ls}} + \frac{\boldsymbol{I_{cbs(leak)}}}{\boldsymbol{f}}\right]}{\boldsymbol{V_{CC}} - \boldsymbol{V_f} - \boldsymbol{V_{LS}} - \boldsymbol{V_{Min}}} \tag{85}$$

$\boldsymbol{Q_g}$= Gate charge of high-side FET (Field-Effect Transistor).

$\boldsymbol{f}$ = switching frequency.

$\boldsymbol{I_{qbs(max)}}$ = Maximum $\boldsymbol{I_{VDDOq}}$ quiescent current which can be found in the 1EDBx275F datasheet.

$\boldsymbol{I_{Cbs(leak)}}$= bootstrap capacitor leakage current.

$\boldsymbol{V_{CC}}$ = Logic supply voltage source.

$\boldsymbol{V_f}$= Forward voltage drops across the bootstrap diode.

$\boldsymbol{V_{LS}}$= Voltage drops across the low-side FET or load.

$\boldsymbol{V_{Min}}$= Minimum voltage between $\boldsymbol{V_G}$ and $\boldsymbol{V_S}$.

$\boldsymbol{Q_{ls}}$= level shift charge required per cycle (Typically $\mathbf{5}\boldsymbol{nC}$ for 500V/600V MGDs (MOS-gate drivers) and $\mathbf{20}\boldsymbol{nC}$ for 1200V MGDs).

In this application, the $\boldsymbol{Q_g}$ is $\mathbf{22}\boldsymbol{nC}$ from the datasheet of MOSFET IMW65R072M1H. Switching frequency is $\mathbf{20}\boldsymbol{kHz}$. The $\boldsymbol{I_{qbs(max)}}$ is $\mathbf{1}\boldsymbol{mA}$ from the datasheet of 1EDBx275F. The $\boldsymbol{Q_{ls}} = \mathbf{5}\boldsymbol{nC}$, $\boldsymbol{V_{CC}} = \mathbf{15}\boldsymbol{V}$ and $\boldsymbol{V_f} = \mathbf{1.3}\boldsymbol{V}$.The value of $\boldsymbol{V_{LS}}$, $\boldsymbol{V_{Min}}$ and $\boldsymbol{I_{Cbs(leak)}}$ are assumed be negligible (zero). According to the equation (85), the value of bootstrap capacitor $\boldsymbol{C1}$ should at least be $\mathbf{14}\boldsymbol{nF}$. In this project, the value of $\boldsymbol{C1}$ is $\mathbf{2}\boldsymbol{uF}$.

# 4.4 Current and voltage detector

In this project, the $\boldsymbol{PLL}$, $\boldsymbol{PI}$ current controller and dead time compensator require current and voltage measurement. This section describes the operation and the design of detection systems.

The first part of detector system is setting the sample resistor for output current and voltage in H-Bridge.

**Figure 4-15** shows the schematic diagram of $\boldsymbol{LCL}$ filter and detection circuit connected between $\boldsymbol{leg\ A}$ and $\boldsymbol{leg\ B}$ of H-Bridge inverter.

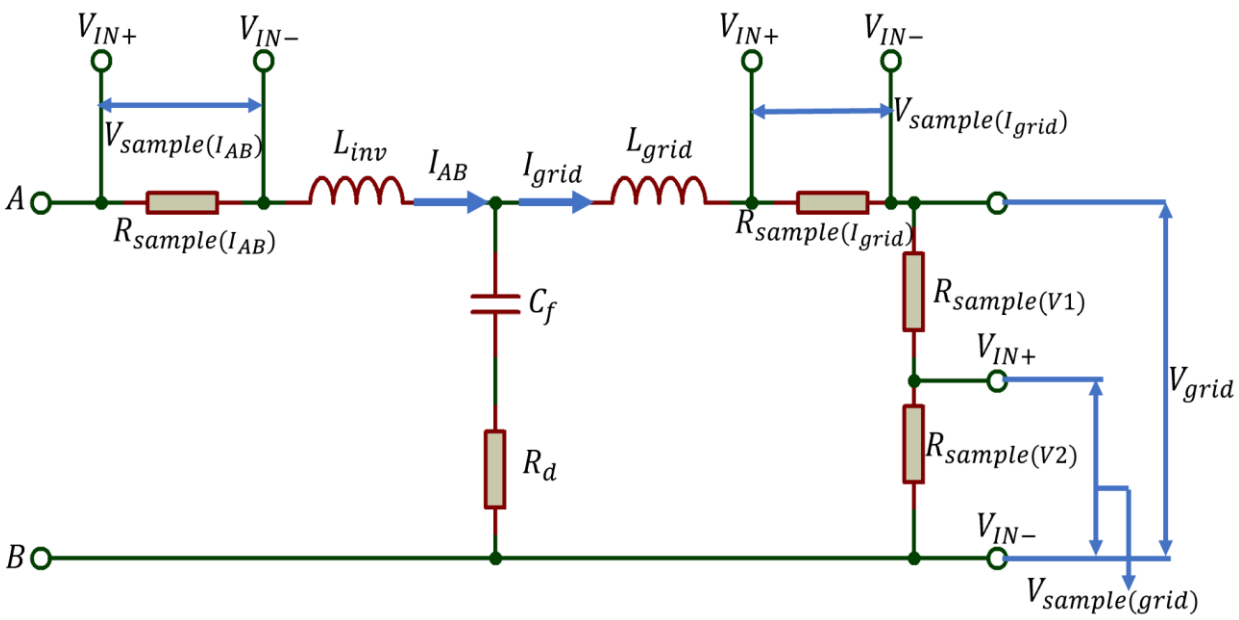


**Figure 4-15 : Schematic circuit diagram of main output circuit with sample resistor.**

The sample resistor $\boldsymbol{R_{sample(I_{AB})}}$ and $\boldsymbol{R_{sample(I_{grid})}}$ are used for detecting the current of $\boldsymbol{I_{AB}}$ and $\boldsymbol{I_{grid}}$. As shown in **Figure 4-15**, the voltage on sample resistor will be detected and this is proportional to the current flowing through the $\boldsymbol{R_{sample(I_{AB})}}$ and $\boldsymbol{R_{sample(I_{grid})}}$ which are $\boldsymbol{I_{AB}}$ and $\boldsymbol{I_{grid}}$. If these two sample resistors are both equal to $\boldsymbol{1\,\Omega}$, the value of $\boldsymbol{V_{sample(I_{AB})}}$ and $\boldsymbol{V_{sample(I_{grid})}}$ are directly equal to $\boldsymbol{I_{AB}}$ and $\boldsymbol{I_{grid}}$. So, the $\boldsymbol{V_{sample(I_{AB})}}$ and $\boldsymbol{V_{sample(I_{grid})}}$ can represent the sample current of $\boldsymbol{I_{AB}}$ and $\boldsymbol{I_{grid}}$. But large resistor will increase power loss, the low resistance sample resistor should be chosen. The $\boldsymbol{R_{sample(I_{AB})}}$ and $\boldsymbol{R_{sample(I_{grid})}}$ are both $\boldsymbol{0.01\Omega}$ in this application, and so $\boldsymbol{V_{sample(I_{AB})} = 0.01 * I_{AB}}$ and $\boldsymbol{V_{sample(I_{grid})} = 0.01 * I_{grid}}$. $\boldsymbol{V_{sample}}$ is scaled by the microcontroller, which is introduced in this section later.

The resistors $\boldsymbol{R_{sample(V1)}}$ and $\boldsymbol{R_{sample(V2)}}$ are used for detecting voltage of $\boldsymbol{V_{grid}}$. The $\boldsymbol{R_{sample(V1)}}$ is large which equal to $\boldsymbol{0.1M\Omega}$, and $\boldsymbol{R_{sample(V2)}}$ is equal to $\boldsymbol{200\Omega}$. Because of large value of $\boldsymbol{R_{sample(V1)}}$, the influence of sample resistors of $\boldsymbol{V_{grid}}$ can be ignored. The sample voltage $\boldsymbol{V_{sample(V_{grid})}}$ is the voltage on sample resistor $\boldsymbol{R_{sample(V2)}}$, which $\boldsymbol{V_{sample(V_{grid})}} = \frac{\boldsymbol{R_{sample(V2)}}}{\boldsymbol{R_{sample(V1)}+R_{sample(V2)}}} * \boldsymbol{V_{grid}}$. The sample voltage $\boldsymbol{V_{sample(V_{grid})}}$ is 0.002 times of real voltage $\boldsymbol{V_{grid}}$, $\boldsymbol{V_{sample(V_{grid})}} = \boldsymbol{0.002} * \boldsymbol{V_{grid}}$.

The detector circuit design is built based on the $\boldsymbol{ACPL\_7900}$ isolation amplifier. It has high frequency bandwidth (100kHz) and short time response. In this application, all detectors have same design. **Figure 4-16** shows the schematic diagram of detector circuit.

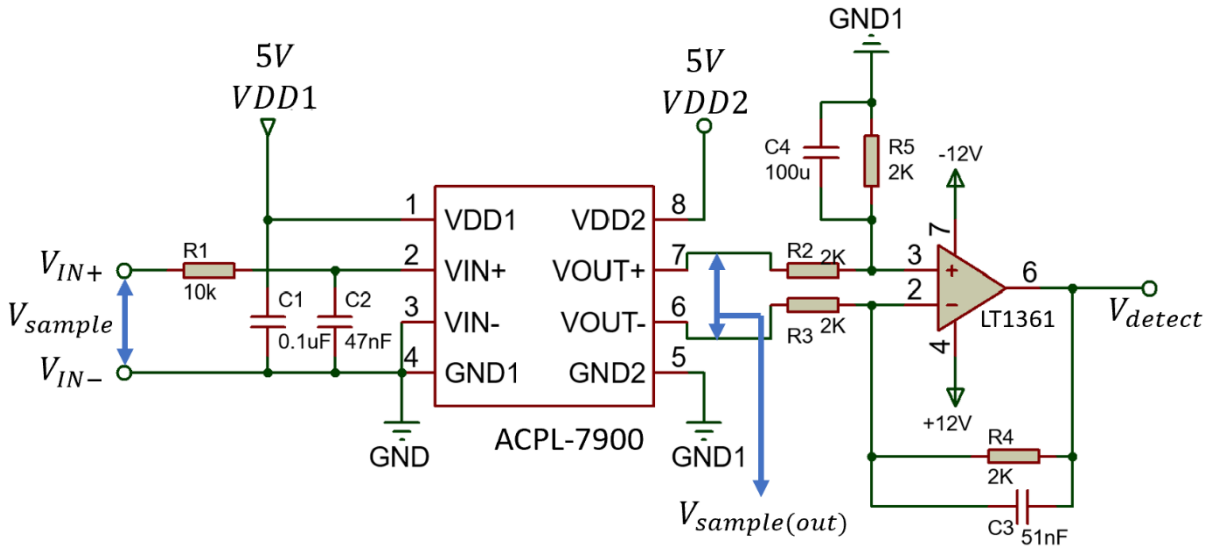


**Figure 4-16 : Schematic diagram of detector circuit.**

$\boldsymbol{V_{sample}}$ represents any sample voltage or current including $\boldsymbol{V_{sample(I_{AB})}}$, $\boldsymbol{V_{sample(I_{grid})}}$ and $\boldsymbol{V_{sample(V_{grid})}}$. The $\boldsymbol{V_{sample(out)}}$ is the output voltage produced by $\boldsymbol{ACPL\_7900}$ amplifier. The $\boldsymbol{V_{detect}}$ is the output from the detector including $\boldsymbol{V_{detect(I_{grid})}}$ ,

$V_{detect(I_{AB})}$ and $V_{detect(V_{grid})}$ for detect current of $I_{grid}$, $I_{AB}$ and detect voltage of $V_{grid}$. The signal produced by the detector will be used for $PI$ current controller, $PLL$ and dead time compensation in microcontroller.

The $ACPL\_7900$ is an isolation amplifier which provides an amplification factor out/in = 8. As result, the $V_{sample(out)}$ of $I_{grid}$ and $I_{AB}$ are $0.08$ times of real $I_{grid}$ and $I_{AB}$ now. While $V_{sample(out)}$ of $V_{grid}$ is $0.016$ times of $V_{grid}$. Another part of detector circuit is differential amplifier based on the $LT1361$ which has high frequency bandwidth and short response time in line with the performance of the $ACPL\_7900$. The detector output $V_{detect}$ can be easily calculated as equation below.

$$V_{detect} = \frac{R4}{R3} * V_{sample(out)} \quad (63)$$

So, the final output $V_{detect}$ can be modified by giving suitable ratio between $R3$ and $R4$ providing a method to compensate for the $0.08$ and $0.016$ scale factors. Another consideration is the acceptable voltage range of microcontroller ADC system. In this application $R4 = R3$. As result, the output signal $V_{detect(I_{grid})}$ and $V_{detect(I_{AB})}$ from detector are equal to $0.08$ time of $I_{grid}$ and $I_{AB}$. The output signal $V_{detect(V_{grid})}$ is equal to $0.016$ times of $V_{grid}$. $V_{detect(I_{grid})} = 0.08 * I_{grid}$, $V_{detect(I_{AB})} = 0.08 * I_{AB}$, and $V_{detect(V_{grid})} = 0.016 * V_{grid}$.

## *Power supplies of Detector Circuit*

As shown in **Figure 4-16**, in a detector circuit, the $ACPL\_7900$ is applied by two separated $5V$, and $LT1361$ is applied by $\pm 12V$ power supply. The voltage source $\pm 12V$ are obtained from the main power system. The two separates $5V$ connected to

$\boldsymbol{VDD1}$ and $\boldsymbol{VDD2}$ of $\boldsymbol{ACPL\_7900}$ are produced from $\boldsymbol{+12V}$ voltage source, which is described in this section later.

As shown in **Figure 4-16**, the ground $\boldsymbol{GND}$ **pin** of input side of $\boldsymbol{ACPL\_7900}$ is connected to the $\boldsymbol{V_{IN-}}$ of sample resistor, the voltage at $\boldsymbol{GND}$ is floating. The datasheet of $\boldsymbol{ACPL\_7900}$ recommends that the power supply for the input side of $\boldsymbol{ACPL\_7900}$ can be built by a bootstrap circuit. However, under high frequency excitation the bootstrap circuit in main output circuit will be influenced especially when testing the inverter side current $\boldsymbol{I_{AB}}$. The high frequency component in current $\boldsymbol{I_{AB}}$ can not be fully captured because of the input power supply of $\boldsymbol{ACPL\_7900.}$ Instead, a DC to DC converter $\boldsymbol{IB1205S}$ is used for input power supply of $\boldsymbol{ACPL\_7900}$.The isolated DC to DC converter $\boldsymbol{IB1205S}$ can transfer $\boldsymbol{+12V}$ to $\boldsymbol{5V(for\ VDD1)}$. The $\boldsymbol{GND1}$ is the ground of microcontroller side and this is also the ground reference of voltage source $\boldsymbol{\pm 12V}$. While the ground reference of $\boldsymbol{VDD1}$ is the floating $\boldsymbol{GND}$. The isolated $\boldsymbol{IB1205S}$ converter can achieve the voltage conversion and isolate the $\boldsymbol{GND1}$ and floating $\boldsymbol{GND}$. Then, supplying stable 5V power supply to $\boldsymbol{VDD1}$ of $\boldsymbol{ACPL\_7900}$.

Another $\boldsymbol{5V}$ voltage supply for the $\boldsymbol{VDD2}$ of $\boldsymbol{ACPL\_7900}$ is produced from $\boldsymbol{+12V}$ voltage source by a $\boldsymbol{TL431}$ voltage regulator and the ground reference to $\boldsymbol{VDD2}$ is $\boldsymbol{GND1}$ which is shown in **Figure 4-17**.

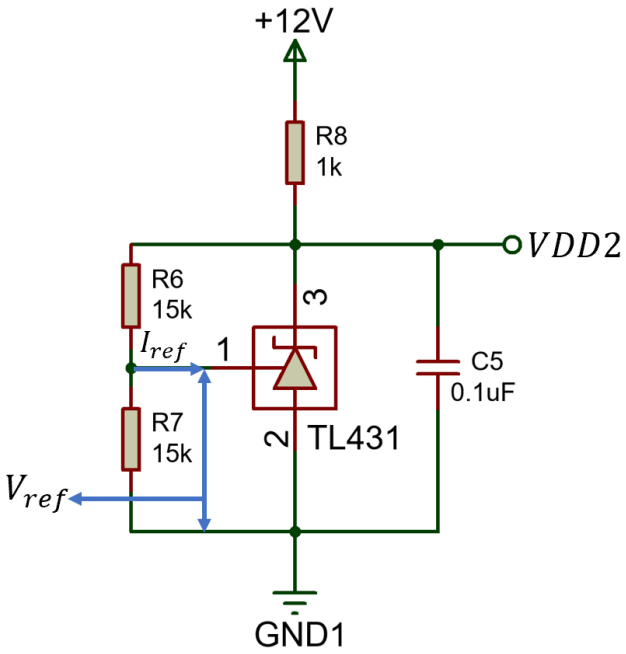


**Figure 4-17 : voltage regulator for converting $+12V$ to $+5V$ supplying $VDD2$.**

This $+5V$ which supplies $VDD2$ voltage source has same $GND1$ with $+12V$ voltage source, and it is the power of output side of $ACPL\_7900$.

The output voltage of $TL431$ voltage regulator is connected to $VDD2$ is equal to $+5V$ which can be calculated by equation (86).

$$VDD2 = V_{ref} * \left(1 + \frac{R6}{R7}\right) + I_{ref} * R6 \quad (86)$$

The $V_{ref}$ and $I_{ref}$ in $TL431$ is $2495mV$ and $2\mu A$, the resistor $R6$ is equal to $R7$ which is $15K\Omega$. As result, the $VDD2$ is equal to $5.02V$.

In conclusion, whole detector circuit board consists of a main detector circuit including the amplifier $ACPL\_7900$ and $LT1361$, and its power supply circuit including $1B1205S$ and $TL431$ voltage regulator. **Figure 4-18** shows the circuit board of the

detector system. The whole detector system is designed to be connected as a solderable single in-line module which can be replaced and maintained easily.

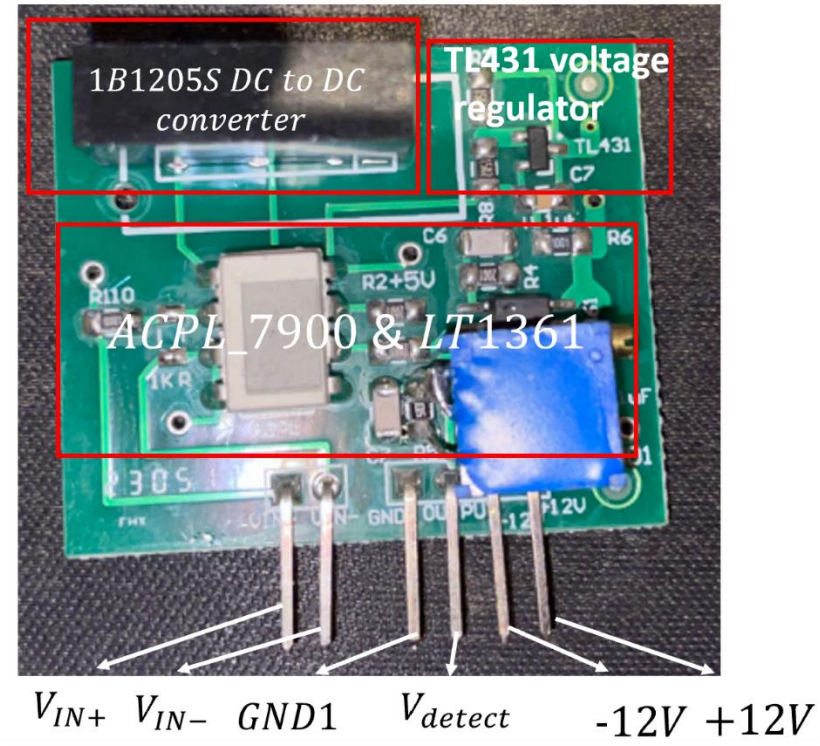


**Figure 4-18 : Detector module**

The final part of this section describes the voltage offset system for transferring the detect signal from detector into the microcontroller. In order to achieve feedback control, the detected signal $\boldsymbol{V_{detect(I_{grid})}}$ and $\boldsymbol{V_{detect(V_{grid})}}$ are needed to be sent into the $\boldsymbol{ADC}$ system in microcontroller. In STM32F407ZGT6 microcontroller, the accepted voltage in $\boldsymbol{ADC}$ system is from $\boldsymbol{0V}$ to $\boldsymbol{3.3V}$. Since the output waveform from detector circuit can go negative, it exceeds the range from $\boldsymbol{0V}$ to $\boldsymbol{3.3V}$. A voltage offset system is used to adding an offset voltage with the detect signal, increasing the voltage level of zero point, ensuring all detect signal from detector are in the range from $\boldsymbol{0V}$ to $\boldsymbol{3.3V}$.

**Figure 4-19** shows the voltage offset circuit for the sample voltage $V_{offset(V_{grid})}$, which is the detect signal of $V_{grid}$.

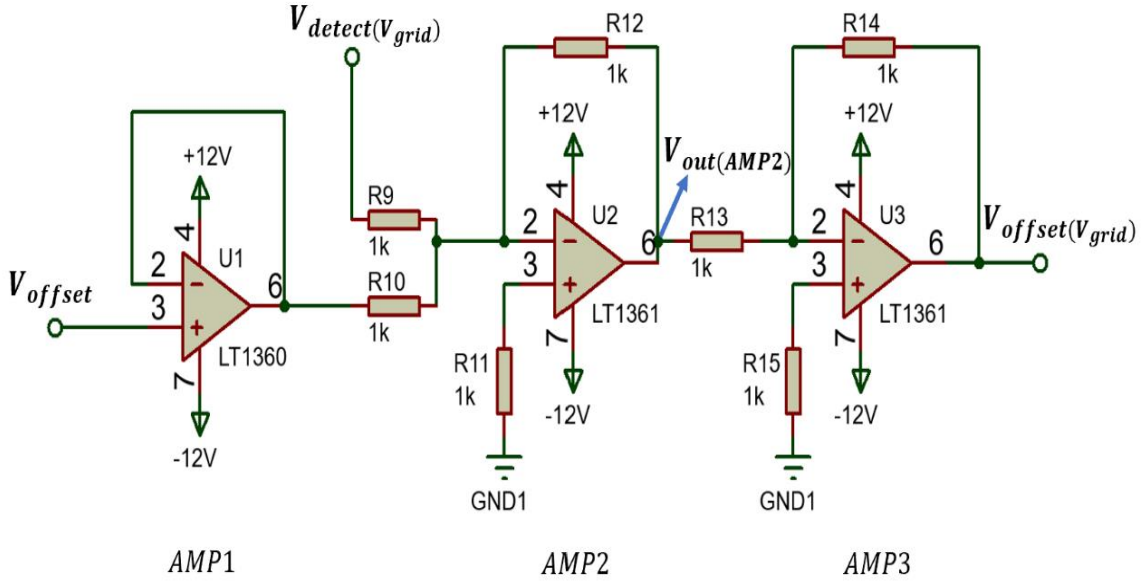


**Figure 4-19 : Schematic diagram of the offset voltage circuit for $V_{detect(V_{grid})}$.**

The $V_{offset}$ is a fixed voltage equal to $\mathbf{1.5}V$ produced from the microcontroller. There are three $LT1361$ amplifier used for building the offset voltage. The $AMP1$ is a voltage flower, the $AMP2$ act as an inverting adder, and $AMP3$ is an inverting amplifier. The output voltage from $AMP2$ and $AMP3$ can be calculated according to the amplifier equation shown below.

$$V_{out(AMP2)} = -\left(\frac{R12}{R9} * V_{detect(V_{grid})} + \frac{R12}{R10} * V_{offset}\right) \quad (65)$$

$$V_{offset(V_{grid})} = V_{out(AMP2)} * \left(-\frac{R14}{R13}\right) \quad (66)$$

Since all resistor from $\boldsymbol{R9}$ to $\boldsymbol{R14}$ are same, the $\boldsymbol{V_{out(AMP2)}}$ is equal to $-(\boldsymbol{V_{detect(V_{grid})}} + \boldsymbol{V_{offset}})$. The peak voltage of $\boldsymbol{V_{grid}}$ is between $\pm\boldsymbol{70V}$, after the detector, the peak voltage of $\boldsymbol{V_{detect(V_{grid})}}$ from detector is between $\pm\boldsymbol{1.12V}$. Finally, the $\boldsymbol{1.5V}$ offset voltage $\boldsymbol{V_{offset}}$ is added with $\boldsymbol{V_{detect(V_{grid})}}$, the final range of $\boldsymbol{V_{offset(V_{grid})}}$ is between $+\boldsymbol{2.62V}$ and $+\boldsymbol{0.38V}$, which is in the range from $\boldsymbol{0V}$ to $\boldsymbol{3.3V}$. For the current $\boldsymbol{I_{grid}}$, the peak current of $\boldsymbol{I_{grid}}$ is $\pm\boldsymbol{14A}$, with the same offset voltage, the range of $\boldsymbol{V_{offset(I_{grid})}}$ is between $\boldsymbol{2.62V}$ and $\boldsymbol{0.38V}$ as well. So, it is also in the range of $\boldsymbol{ADC}$ system of the microcontroller.

In conclusion, the final signal received by microcontroller is equal to $\boldsymbol{V_{detect(V_{grid})}} = \boldsymbol{V_{grid}} * \boldsymbol{0.016} + \boldsymbol{1.5V}$, while $\boldsymbol{V_{detect(I_{grid})}} = \boldsymbol{I_{grid}} * \boldsymbol{0.08} + \boldsymbol{1.5V}$. The scaling factors 0.016 and 0.08, and voltage offset $\boldsymbol{1.5V}$ will be removed during the calculation in the microcontroller.

In summary, this section has described the circuit design of a detector system shown in **Figure 4-18**. The first advantage of this detector is that it contains two own power converters $\boldsymbol{IB1205S}$ and $\boldsymbol{LT431}$. As result, the detector only needs $\pm\boldsymbol{12V}$ power supply to power whole detector module. The second advantage is that the output from detector can be easily modified by changing the ratio between $\boldsymbol{R4}$ and $\boldsymbol{R3}$ of $\boldsymbol{LT431}$ amplifier. As result, this detector circuit can be widely used in different circuit for detecting current or voltage.

# 4.5 $MAX913$ current zero-crossing detector circuit design

In section 4.4, the detector circuit is introduced, and the detect signal of $\boldsymbol{V_{grid}}$ and $\boldsymbol{I_{grid}}$ is transferred into the microcontroller for ***PI*** current controller and ***PLL*** control. The current $\boldsymbol{I_{AB}}$ is required for the dead time compensation. Same as the detector used for $\boldsymbol{I_{grid}}$, the detect signal $\boldsymbol{V_{detect(I_{AB})}}$ is 0.08 times of real current $\boldsymbol{I_{AB}}$. For the dead time compensation, the most important is the information about the direction of current $\boldsymbol{I_{AB}}$. In this section, the circuit design for detecting current direction of $\boldsymbol{I_{AB}}$ is introduced.

The zero-crossing detector is designed based on the fast comparator $\boldsymbol{MAX913}$. **Figure 4-20** shows the schematic diagram of $\boldsymbol{MAX913}$ zero-crossing detector.

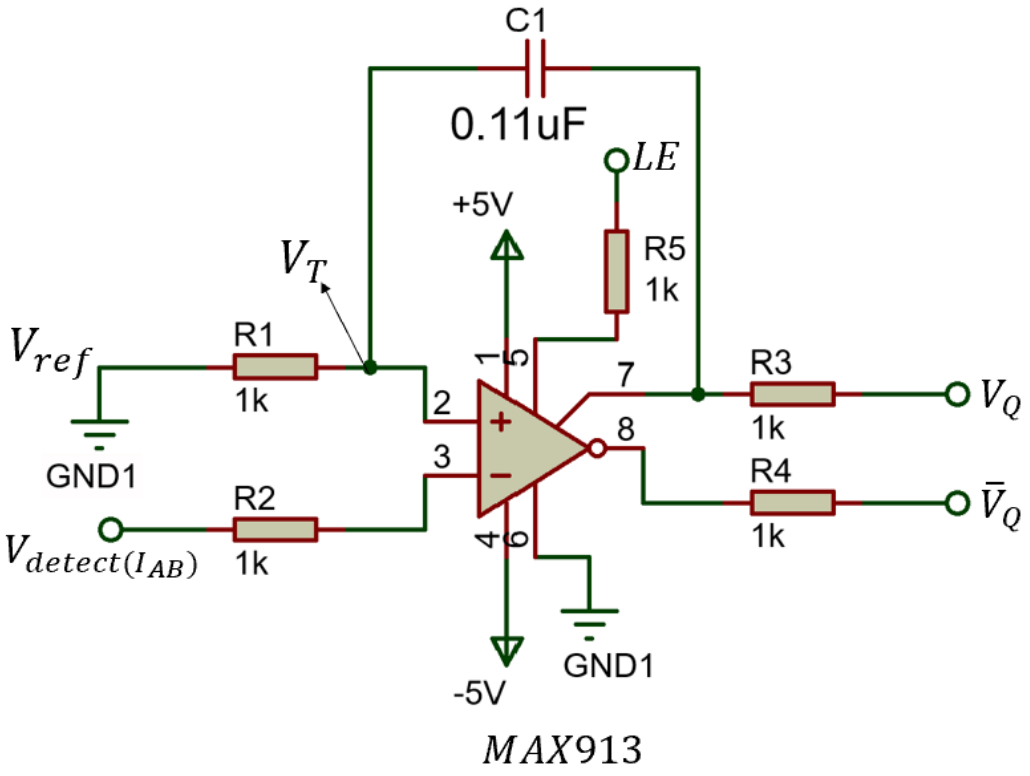


**Figure 4-20 : Schematic diagram of *MAX*913 zero-crossing detect circuit.**

As shown in **Figure 4-20**, the input signal of $\boldsymbol{MAX913}$ is the $\boldsymbol{V_{detect(I_{AB})}}$ which produced from the detector circuit described in section 4.4. The $\boldsymbol{V_{detect(I_{AB})}}$ represents sample current of $\boldsymbol{I_{AB}}$. The reference voltage $\boldsymbol{V_{ref}}$ is equal to $\boldsymbol{0V}$ since it is connected to the $\boldsymbol{GND1}$. The $\boldsymbol{V_{detect(I_{AB})}}$ is compared with reference voltage $\boldsymbol{0V}$ in $\boldsymbol{MAX913}$ comparator to produce the output signal $\boldsymbol{V_Q}$ and $\boldsymbol{\bar{V}_Q}$. Because the $\boldsymbol{V_{detect(I_{AB})}}$ is connected to the inverting input of $\boldsymbol{MAX913}$, when $\boldsymbol{V_{detect(I_{AB})}}$ is larger than $\boldsymbol{0V}$, the output $\boldsymbol{V_Q}$ turns to low voltage ($\boldsymbol{0V}$), while output $\boldsymbol{\bar{V}_Q}$ turns to high voltage (5V) and vice versa. Terminal $\boldsymbol{LE}$ is the latch enable and when $\boldsymbol{LE}$ is at a high voltage, the output of $\boldsymbol{MAX913}$ will be latched. When $\boldsymbol{LE}$ is at low voltage, the $\boldsymbol{MAX913}$ will not be latched.

The signal $\overline{\boldsymbol{V}}_{\boldsymbol{Q}}$ will be used since the high-level voltage represents the positive direction of $\boldsymbol{I}_{\boldsymbol{AB}}$, while low-level voltage represents the negative direction of $\boldsymbol{I}_{\boldsymbol{AB}}$. The current direction signal $\overline{\boldsymbol{V}}_{\boldsymbol{Q}}$ will be sent into the microcontroller for the dead time compensation. As shown in **Figure 4-20**, a capacitor $\boldsymbol{C1}$ is connected between the positive input and output pin of $\boldsymbol{MAX913}$, which is used to decrease the unwanted fluctuation of output $\overline{\boldsymbol{V}}_{\boldsymbol{Q}}$ caused by the noise in the input signal of comparator. Normally, a resistor is connected between the positive input pin and output of the comparator to build a Schmitt trigger. It will create a hysteresis window ($\pm\boldsymbol{V}_{\boldsymbol{T}}$) around the reference voltage to block the noise influence in the range of $\pm\boldsymbol{V}_{\boldsymbol{T}}$. But this method will decrease the resolution of zero-crossing detect and it is suitable for the system with low frequency system. As described before in section 2.2, the output current $\boldsymbol{I}_{\boldsymbol{AB}}$ from H-Bridge inverter contains high frequency harmonic signal. So, the signal $\boldsymbol{V}_{\boldsymbol{detect}(\boldsymbol{I}_{\boldsymbol{AB}})}$ contains high frequency harmonic signal as well. During the zero-crossing time, the voltage changes of $\overline{\boldsymbol{V}}_{\boldsymbol{Q}}$ will turns between high- and low-level voltage at high frequency as well. If the Schmitt trigger is used, the data about zero-crossing loss, hence influence the accurate of dead time compensation. As result, a capacitor is added as shown in **Figure 4-20** instead of using the resistor. **Figure 4-21** shows an example of the input and output signal from comparator after adding a capacitor between the positive input and output.

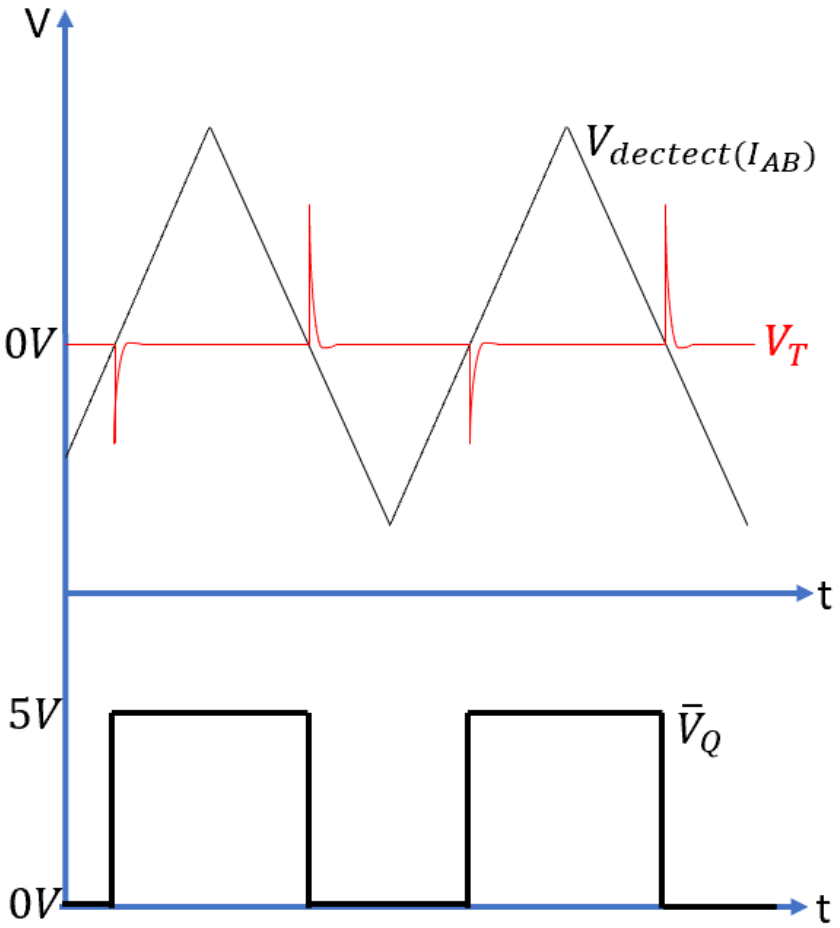


**Figure 4-21 : The input and output signal of *MAX*913 comparator with Schmitt trigger capacitor.**

Because of the capacitor $\boldsymbol{C1}$, it will produce a small impulse on the non-inverting pin $\boldsymbol{V_T}$ of comparator during the voltage turns of $\bar{\boldsymbol{V}}_{\boldsymbol{Q}}$. As shown in **Figure 4-21**, when $\boldsymbol{V_{detect(I_{AB})}}$ crosses the $\boldsymbol{0V}$ from positive to negative, $\bar{\boldsymbol{V}}_{\boldsymbol{Q}}$ turns from high-level to low-level voltage because of zero-crossing, the $\boldsymbol{C1}$ produce a positive impulse voltage on positive input of comparator. At the same time, $\boldsymbol{V_{detect(I_{AB})}}$ keep decreasing, while $\boldsymbol{V_T}$ is increased by the impulse. This produces a large voltage difference between $\boldsymbol{V_{detect(I_{AB})}}$ and $\boldsymbol{V_T}$, hence the small noise voltage from $\boldsymbol{V_{detect(I_{AB})}}$ can not cause the

false trigger and influence the output voltage $\overline{V}_Q$. Because the $C1$ is small, the $V_T$ will returns to the $0V$ from the impulse in very short time, hence it will not influence the next comparation between $V_{detect(I_{AB})}$ and $V_T$.

# 4.6 H-Bridge protection circuit design

This section introduces the protection circuit in H-Bridge inverter. There are two main protection circuits in this project. The first protection is named as $I_{DC}$ **Overcurrent Detector**. It is used to detect if the current which through the whole H-Bridge is over the max current limit. The max limit current is set according to the peak output current from the H-Bridge which will be described in this section. The second protection circuit is named as **Power Switch Protecting Circuit**. It is used to protect every MOSFET power switch in a H-Bridge inverter. The design of this circuit is according to the maximum pulse drain current ($I_{D(pulse)}$) in a MOSFET power switch. The detail will be described later in this section.

## $I_{DC}$ Overcurrent Detector

As shown in **Figure 4-22**, a $0.01\Omega$ sample resistor ($R_{sample(I_{DC})}$) is connected between the $DC$ supply and H-Bridge. Same to the current detector system described in section 5.2, the output from current detector is $V_{detect(I_{DC})}$ which is equal to $0.08 * I_{DC}$. Then a full wave precision rectifier is used to transfer all negative component in $V_{detect(I_{DC})}$ to positive. The output from rectifier is named as $\widehat{V}_{detect(I_{DC})}$.

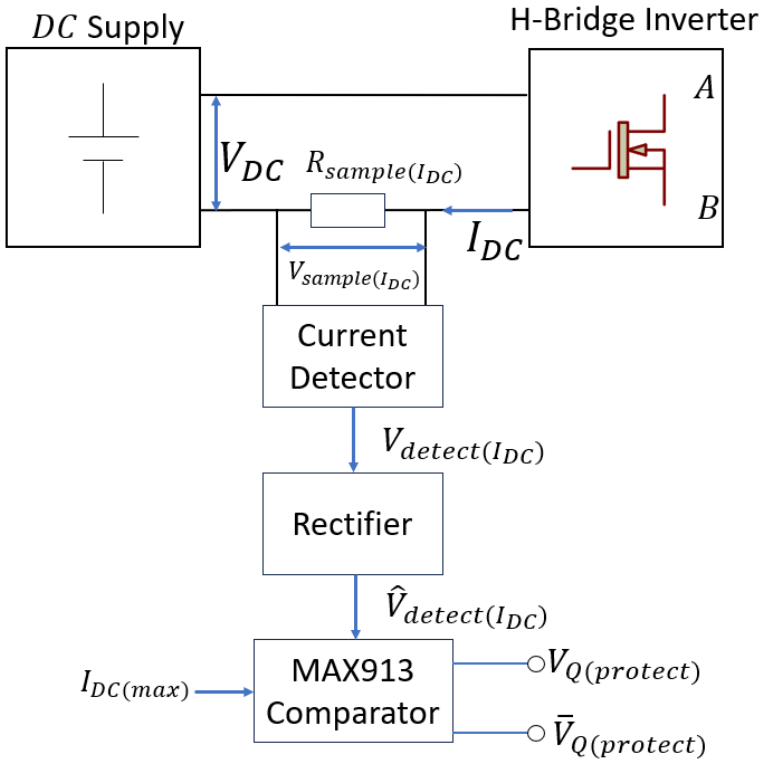


**Figure 4-22: $I_{DC}$ protect circuit block diagram.**

After that, the signal $\widehat{V}_{detect(I_{DC})}$ will be compared with a reference constant voltage transferred from $I_{DC(max)}$ which represent the max limit current set in system.

**Figure 4-23** (a) shows electrical circuit of ***MAX913*** Schmitt trigger comparator.

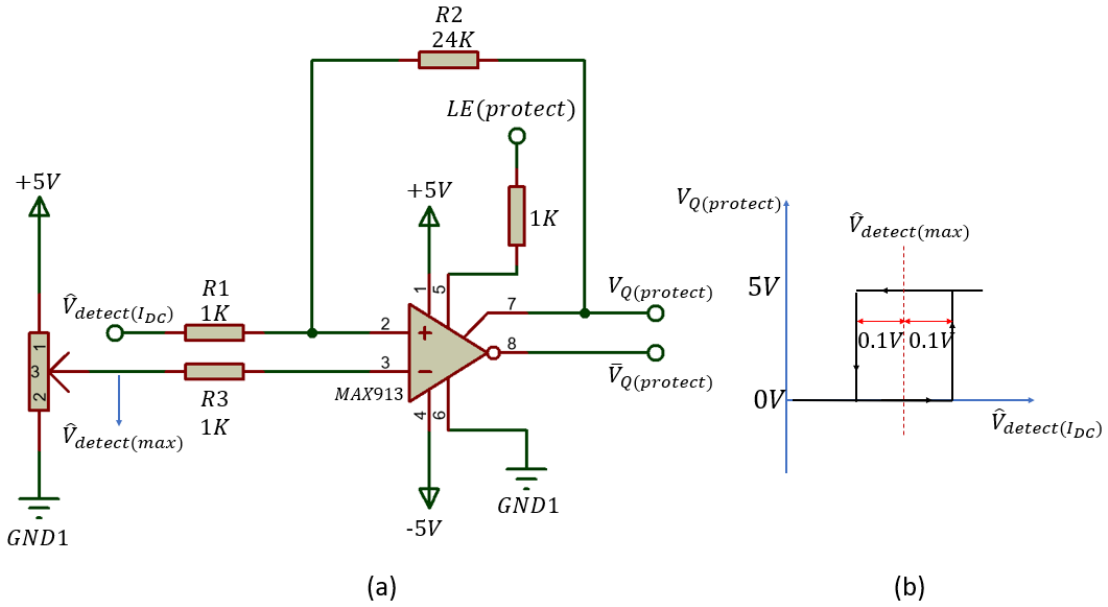


**Figure 4-23: MAX913 Schmitt trigger comparator. (a) Electrical circuit, (b)Hysteresis Curve of Schmitt trigger.**

The reference voltage $\widehat{\boldsymbol{V}}_{\boldsymbol{detect(max)}}$ is transferred from the $\boldsymbol{I_{DC(max)}}$ according to calculation equation in the current detector, so $\widehat{\boldsymbol{V}}_{\boldsymbol{detect(max)}} = \boldsymbol{I_{DC(max)}} * \boldsymbol{0.08}$. The $\widehat{\boldsymbol{V}}_{\boldsymbol{detect(max)}}$ is produced by a voltage regulator from $\boldsymbol{5V}$ power supply. In the comparator, if $\widehat{\boldsymbol{V}}_{\boldsymbol{detect(I_{DC})}} > \widehat{\boldsymbol{V}}_{\boldsymbol{detect(max)}}$, the output from comparator $\boldsymbol{V_{Q(protect)}}$ turns from $\boldsymbol{0V}$ to $\boldsymbol{5V}$. The pin $\boldsymbol{V_{Q(protect)}}$ is connected into the microcontroller. Once the microcontroller reads the voltage change of $\boldsymbol{V_{Q(protect)}}$ from low to high voltage. The microcontroller will shut down the whole system. At the same time, the $\boldsymbol{LE(protect)}$ pin will be given a $\boldsymbol{3.3V}$ voltage from microcontroller to latch off the comparator. So that, after the protection is triggered, the comparator will not be miss triggered again to turn off the protection. The latch off is turned off after the whole H-Bridge is checked and restarted.

As shown in **Figure 4-23**, a resistor $\boldsymbol{R2}$ is connected between positive pin of comparator and output, which creating a Schmitt trigger circuit, and the hysteresis curve is shown in **Figure 4-23** (b). The reason for using Schmitt trigger here is to increase the stability of protection system when the output current $\boldsymbol{I_{DC}}$ is very close to the $\boldsymbol{I_{DC(max)}}$, and the protection will not be miss triggered by small fluctuation in $\boldsymbol{I_{DC}}$. With the Schmitt trigger, the protection is act when $\boldsymbol{\widehat{V}_{detect(I_{DC})} > \widehat{V}_{detect(max)} + 0.1V}$. In this project, the max current limit ($\boldsymbol{I_{DC(max)}}$) is set as $\boldsymbol{28A}$, so $\boldsymbol{\widehat{V}_{detect(max)} = 2.24V}$. As result, when $\boldsymbol{\widehat{V}_{detect(I_{DC})} > 2.24V + 0.1V = 2.34V}$, the protection is act.

## Power Switch Protection Circuit

The aim of this protection system is monitoring the voltage and current between Drain and Source $\boldsymbol{V_{DS}}$ and $\boldsymbol{I_{DS}}$ of MOSFET power switches. To protect the power switches in H-Bridge from over current events the protection circuit is used to limit the maximum current due of short-circuits or broken load. The protection system gives signal to shut down whole system.

**Figure 4-24** shows the protection circuit design of switch $\boldsymbol{SA-}$ in H-Bridge inverter. The protection circuit is consisted of the protection diode $\boldsymbol{D_{protect}}$, Zener diode $\boldsymbol{Z_{protec}}$, resistor $\boldsymbol{R_{protect}}$, transistor $\boldsymbol{T_{protect}}$, capacitor $\boldsymbol{C_{protect}}$ and FODM453 Optocouplers. The design of protection system for other power switches in H-Bridge inverter are all same. Only difference is the $\boldsymbol{+15V}$ voltage source on FODM453 in upper and lower side of power switches, which is explained in this section later.

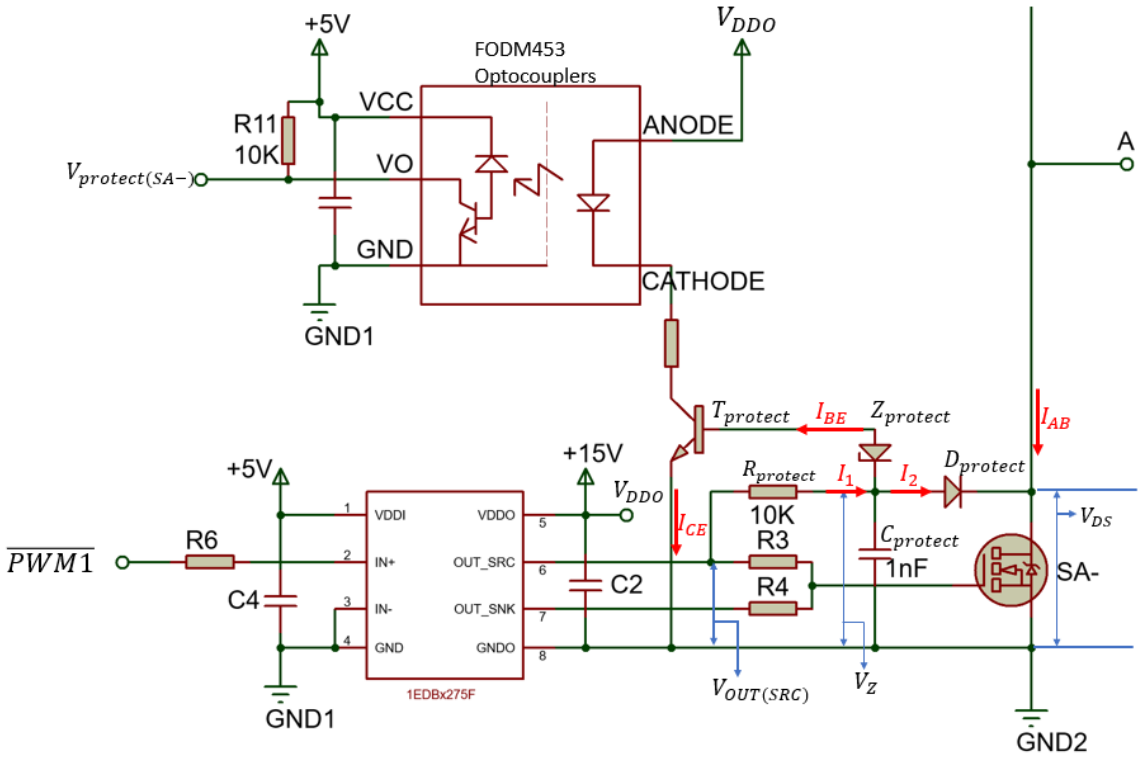


**Figure 4-24 : Protection circuit of switch $SA-$.**

The voltage $\boldsymbol{V_{DS}}$ is Drain to Source voltage of power switch. In the power switch IMW65R072M1H, the turn on resistor $\boldsymbol{R_{DS(on)}}$ between Drain and Source is $\boldsymbol{72m\Omega}$. In this project, the peak current allowed to flow through in H-Bridge $\boldsymbol{\hat{I}_{AB}}$ is 14A. The turn on voltage Zener diode is 5.1V. The choose of turn on voltage of this Zener diode is according to the max pulse drain current ($\boldsymbol{I_{D(pulse)}}$).

At first, the operation of protection system under normal working conditions will be described. When the $\boldsymbol{SA-}$ is turned off, the gate control voltage $\boldsymbol{V_{OUT(SRC)}}$ is 0, hence the voltage $\boldsymbol{V_Z}$ is also 0. The Zener diode $\boldsymbol{Z_{protect}}$ is turned off, no current flows through into the Base of transistor $\boldsymbol{T_{protect}}$, and it is turned off. As result, the FODM453 is turned off, the output signal $\boldsymbol{V_{protect(SA-)}}$ from the FODM453 is equal to $\boldsymbol{5V}$. After the $\boldsymbol{SA-}$ is turned on, the $\boldsymbol{V_{DS}}$ is equal to $\boldsymbol{R_{DS(on)} * \hat{I}_{AB}}$ which is equal to $\boldsymbol{1V}$. On the

other hand, the $\boldsymbol{V_{OUT(SRC)}}$ is equal to $\mathbf{15}\boldsymbol{V}$. Because the $\boldsymbol{V_{OUT(SRC)}}$ is higher than the $\boldsymbol{V_{DS}}$, the diode $\boldsymbol{D_{protect}}$ is turned on, then it clamps the $\boldsymbol{V_Z}$ to $\mathbf{2.3}\boldsymbol{V}$ which is equal to $\boldsymbol{V_{DS}} + \boldsymbol{V_F}$, $\boldsymbol{V_F}$ is $\mathbf{1.3}\boldsymbol{V}$ is the forward voltage drop of $\boldsymbol{D_{protect}}$. Because the $\boldsymbol{V_Z}$ is lower than turn on voltage of $\boldsymbol{Z_{protect}}$, $\boldsymbol{Z_{protect}}$ still turns off, $\boldsymbol{I_{BE}} = \mathbf{0}$, hence the current $\boldsymbol{I_1}$ which through $\boldsymbol{R_{protect}}$ is equal to the current $\boldsymbol{I_2}$ which through the $\boldsymbol{D_{protect}}$, equal to $\frac{\mathbf{15}\boldsymbol{V}-\mathbf{2.3}\boldsymbol{V}}{\mathbf{10}\boldsymbol{K}} = \mathbf{1.27}\boldsymbol{mA}$. This current is too small compared to $\boldsymbol{I_{AB}}$, it can be ignored. Because $\boldsymbol{I_{BE}} = \mathbf{0}$, $\boldsymbol{T_{protect}}$ turns off, hence optocouplers turns off, the output $\boldsymbol{V_{protect(SA-)}}$ is still at $\mathbf{5}\boldsymbol{V}$, it means the H-Bridge is working under normal condition.

The voltage $\boldsymbol{V_Z}$ is related to the $\boldsymbol{V_{DS}}$ of power switches, and the turn on voltage of $\boldsymbol{Z_{protect}}$. Now, assuming the current flows through H-Bridge becomes much higher than the peak limit current in H-Bridge because of wrong operation of $\boldsymbol{PWM}$ or a fault with the load during the time switch when $\boldsymbol{SA-}$ is on. With the increase of current through $\boldsymbol{SA-}$, $\boldsymbol{V_{DS}}$ increase as well, hence $\boldsymbol{V_Z}$ increases with $\boldsymbol{V_{DS}}$ because of clamp diode $\boldsymbol{D_{protect}}$. Consider the Base to Emitter voltage $\mathbf{0.7}\boldsymbol{V}$ of $\boldsymbol{T_{protect}}$, when $\boldsymbol{V_Z}$ is higher than $\mathbf{5.8}\boldsymbol{V}$ $(\mathbf{5.1} + \mathbf{0.7})$, $\boldsymbol{Z_{protect}}$ is turned on. Now, current can flow through the Zener diode to Base of transistor $\boldsymbol{I_{BE}} \neq \mathbf{0}$, since $\boldsymbol{V_Z}$ is clamped at 5.8V which is lower than $\boldsymbol{V_{DS}}$, $\boldsymbol{D_{protect}}$ turns off, hence $\boldsymbol{I_2} = \mathbf{0}$, $\boldsymbol{I_1} = \boldsymbol{I_{BE}} = \frac{\mathbf{15}-\mathbf{5.8}}{\mathbf{10}\boldsymbol{K}} = \mathbf{0.92}\boldsymbol{mA}$. The current gain of transistor is 80, so the Collector and Emitter current $\boldsymbol{I_{CE}}$ is equal to $\mathbf{80} * \mathbf{0.92}\boldsymbol{mA} = \mathbf{73.6}\boldsymbol{mA}$. According to datasheet of FODM453, the turn on current of FODM453 is $\mathbf{16}\boldsymbol{mA}$. So, optocoupler is turned on, the protect signal $\boldsymbol{V_{protect(SA-)}}$ turns to 0, which means the current flows through H-Bridge is over the limit max current, and then whole system is shut down.

In conclusion, when $\boldsymbol{V_Z}$ is higher than $\mathbf{5.8}\boldsymbol{V}$, the protection system starts to work. At this time, $\boldsymbol{V_{DS}}$ is equal to 4.5V, so the max limit current $\boldsymbol{I_{AB(max)}}$ is $\mathbf{62.5}\boldsymbol{A}$. When turn on voltage of $\boldsymbol{Z_{protect}}$ is $\mathbf{5.1}\boldsymbol{V}$, the maximum limited current available through H-Bridge is 62.5$\boldsymbol{A}$. Equation (87) shows the calculation of $\boldsymbol{V_Z}$ according to the maximum current $\boldsymbol{I_{AB(max)}}$.

$$\boldsymbol{V_Z} = \mathbf{1.4} + \boldsymbol{V_{DS(max)}} = \mathbf{1.4} + \boldsymbol{R_{DS(on)}} * \boldsymbol{I_{AB(max)}} \quad (87)$$

By checking datasheet of IMW65R072M1H MOSFET, the maximum pulsed drain current ($\boldsymbol{I_{D(Pulse)}}$) is $\mathbf{69}\boldsymbol{A}$, the set of $\boldsymbol{I_{AB(max)}}$ should be lower than the $\boldsymbol{I_{D(Pulse)}}$.

The set of turn on voltage of $\boldsymbol{Z_{protect}}$ is related to the $\boldsymbol{R_{DS(on)}}$ and $\boldsymbol{I_{D(Pulse)}}$ in a MOSFET power switch. With different model of MOSFET used in H-Bridge, the suitable Zener diode should be chosen.

In addition, the value of resistor $\boldsymbol{R_{protect}}$ relates to the current $\boldsymbol{I_1}$, $\boldsymbol{I_B}$ and $\boldsymbol{I_{CE}}$. In order to ensure the optocoupler can turn on when the current flows through H-Bridge over the limitation, the $\boldsymbol{I_{CE}}$ should be larger than $\mathbf{16}\boldsymbol{mA}$, which $\boldsymbol{I_{CE}} = \mathbf{80} * \frac{\boldsymbol{V_{OUT(SRC)}} - \boldsymbol{V_Z}}{\boldsymbol{R_{protect}}}$. Then the resistor $\boldsymbol{R_{protect}}$ can be calculated.

Capacitor $\boldsymbol{C_{protect}}$ is used to provide filtering to avoid false trigger of protection system during the switch turn on /off transitions. In case of the circuit about $\boldsymbol{SA-}$ in **Figure 4-24**, after $\overline{\boldsymbol{PWM1}}$ turns to high, the voltage $\boldsymbol{V_{OUT(SRC)}}$ turns to 15V for turn on the $\boldsymbol{SA-}$ switches. But in actual circuit, MOSFET switch has a certain turn on time. During this time, $\boldsymbol{SA-}$ still off, hence $\boldsymbol{V_{DS}}$ is equal to $\boldsymbol{V_{DC}}$, while $\boldsymbol{V_{OUT(SRC)}}$ has already changed to $\mathbf{15}\boldsymbol{V}$. If there is no $\boldsymbol{C_{protect}}$, $\boldsymbol{V_Z}$ turns to $\mathbf{15}\boldsymbol{V}$ immediately with voltage change of $\boldsymbol{V_{OUT(SRC)}}$. Because $\boldsymbol{V_Z}$ is lower than $\boldsymbol{V_{DS}}$ since the MOSFET switch is still

off, $\boldsymbol{D_{protect}}$ turns off. Since $\boldsymbol{V_Z}$ is higher than the turn on voltage of $\boldsymbol{Z_{protect}}$, $\boldsymbol{Z_{protect}}$ is turned on so as the FODM453 optocoupler, $\boldsymbol{V_{protect(SA-)}}$ turns to 0V. As result, because of the turn on time of power switches, the protection system is triggered accidentally. In order to avoid the accidental trigger of protection system, $\boldsymbol{C_{protect}}$ is required. $\boldsymbol{C_{protect}}$ & $\boldsymbol{R_{protect}}$ form a RC integral circuit, which slow the voltage change of $\boldsymbol{V_Z}$ during the turn on delay time of power switch. In MOSFET IMW65R072M1H, the turn on delay time is $\boldsymbol{18.2ns}$, it is necessary to ensure that the $\boldsymbol{V_Z}$ does not reach to the turn on voltage of protection system (5.8V) during turn on delay time ($\boldsymbol{18.2ns}$). The charge equation of capacitor $\boldsymbol{C_{protect}}$ is,

$$\boldsymbol{V_Z = V_{OUT(SRC)} * \left(1 - e^{-\frac{t}{R_{protect} * C_{protect}}}\right)} \quad (88)$$

Assuming $\boldsymbol{V_Z}$ reaches to $\boldsymbol{5.8V}$ when $\boldsymbol{t = 18.2ns}$, $\boldsymbol{R_{protect} = 10k\Omega}$. As result, the $\boldsymbol{C_{protect}}$ should larger than $\boldsymbol{3.7pF}$ for ensure the $\boldsymbol{V_Z}$ does not reach to $\boldsymbol{5.8V}$ in $\boldsymbol{18.2ns}$. In this research, $\boldsymbol{C_{protect} = 1nF}$, when $\boldsymbol{t = 18.2ns}$, $\boldsymbol{V_Z}$ reaches to $\boldsymbol{27mV}$ which is lower than the turn on voltage of $\boldsymbol{Z_{protect}}$. After power switch $\boldsymbol{SA-}$ turns on, $\boldsymbol{V_Z}$ is clamped by $\boldsymbol{D_{protect}}$, and then the protection system will work as described in this section.

On the other hand, $\boldsymbol{C_{protect}}$ can avoid the false trigger caused by the junction capacitor of diode $\boldsymbol{D_{protect}}$. The junction capacitor is related to the recovery time of diode, when the voltage on the diode is changed from forward to reverse voltage, diode need a certain time to start to block the reverse current. In case of the $\boldsymbol{D_{protect}}$ shown in **Figure 4-24**, under normal condition, the $\boldsymbol{D_{protect}}$ is turned on to clamp the $\boldsymbol{V_Z}$ when $\boldsymbol{SA-}$

turns on. After the $\boldsymbol{SA-}$ is turned off, $\boldsymbol{V_{OUT(SRC)}}$ is also at $\boldsymbol{0V}$, $\boldsymbol{D_{protect}}$ turns off as well. But the voltage on junction capacitor of $\boldsymbol{D_{protect}}$ can not change immediately, and $\boldsymbol{V_{DS}}$ is equal to $\boldsymbol{V_{DC}}$, hence the voltage $\boldsymbol{V_Z}$ changes to $\boldsymbol{V_{DC}+V_F}$ immediately once the $\boldsymbol{SA-}$ turns off. Although the time for this ripple voltage is very short, it may cause the false trigger of protection system, even the high voltage will damage the H-Bridge driver and protection circuit. The $\boldsymbol{C_{protect}}$ here is used to suppress the voltage change caused by the junction capacitor of $\boldsymbol{D_{protect}}$. The junction capacitance of diode is only $\boldsymbol{15pF}$ which is much lower than the capacitance of $\boldsymbol{C_{protect}}$ ($\boldsymbol{1nF}$). The energy in junction capacitor will be absorb by $\boldsymbol{C_{protect}}$ in very short time. After adding $\boldsymbol{C_{protect}}$, the voltage at $\boldsymbol{V_Z}$ is equal to the voltage on $\boldsymbol{C_{protect}}$. During $\boldsymbol{SA-}$ turns on, the peak $\boldsymbol{V_Z}$ is equal to $\boldsymbol{2.3V}$. At the time $\boldsymbol{SA-}$ turns off, the voltage at $\boldsymbol{V_Z}$ can not change immediately because of $\boldsymbol{C_{protect}}$. As result, the $\boldsymbol{V_Z}$ will not increase to voltage $\boldsymbol{V_{DC}+V_F}$ instantly. Instead, the $\boldsymbol{V_Z}$ will increase slowly from $\boldsymbol{2.3V}$ to $\boldsymbol{V_{DC}+V_F}$. But the recovery time of $\boldsymbol{D_{protect}}$ is very fast ($\boldsymbol{150ns}$), $\boldsymbol{V_Z}$ will only increase a little before $\boldsymbol{D_{protect}}$ start to block. During the $\boldsymbol{SA-}$ is off, the energy stored in the $\boldsymbol{C_{protect}}$ will be released through the resistor $\boldsymbol{R_{protect}}$, $\boldsymbol{R3}$, $\boldsymbol{R4}$ and MOSFET switch $\boldsymbol{S2-}$ in the 1EDBx275F IC, hence $\boldsymbol{V_Z}$ decrease to 0 shortly.

In conclusion, the protection system monitors the voltage $\boldsymbol{V_{DS}}$ of MOSFET power switch in H-Bridge inverter, and then producing protecting signal $\boldsymbol{V_{protect}}$ into microcontroller. The protection system of switch $\boldsymbol{SA-}$ is described in this section as an example. The design of the protection systems for the other three switches are the same. The only difference between protection systems of upper and lower side power switches

is the input side power source of FODM453 optocoupler. As shown in **Figure 4-24**, the Anode pin of FODM453 is connected to $+\mathbf{15}\boldsymbol{V}$ power source. This connection is only for the two lower side power switches. As described before in section 4.1, the reason for using bootstrap circuit in H-Bridge drive circuit is that the power source of upper side power switches is connected to a floating point. Same reason for the input power of FODM453 of protection system of upper side power switches. When FODM453 is turned on, the Cathode pin is connected to the Source of power switch. As result, the Anode pin is connected to the $\boldsymbol{V_{DDO}}$ which is supplied from the bootstrap capacitor which shown in **Figure 4-25**.

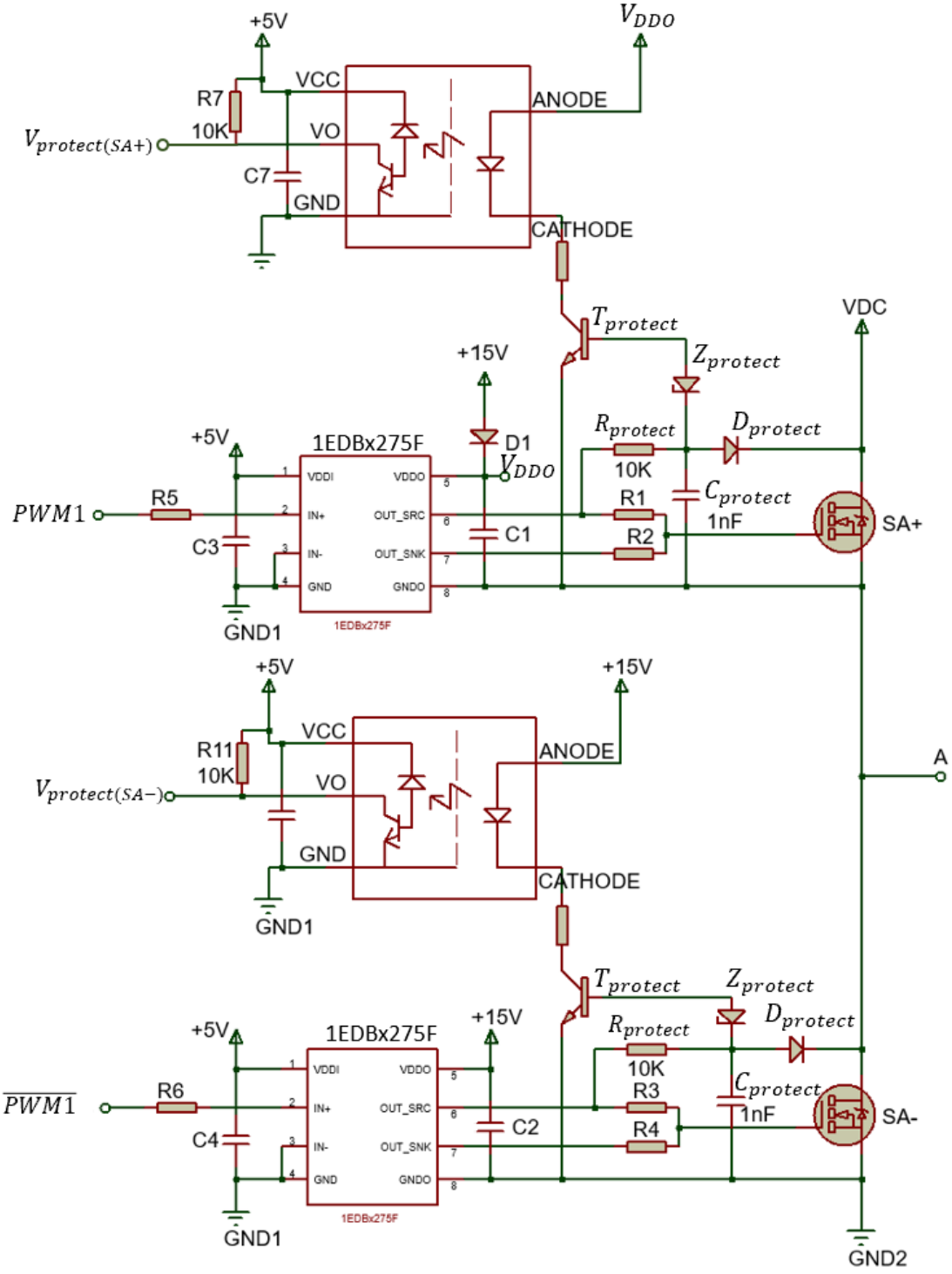


**Figure 4-25 : Protection system for leg *A* power switches in H-Bridge inverter.**

There are four protect signals from protection system which are $\boldsymbol{V_{protect(SA+)}}$, $\boldsymbol{V_{protect(SA-)}}$, $\boldsymbol{V_{protect(SB+)}}$, $\boldsymbol{V_{protect(SB-)}}$. When all signals are at high voltage ($\boldsymbol{5V}$), it means H-Bridge circuit are working under normal condition. When any $\boldsymbol{V_{protect}}$ signal

changes from $\mathbf{5}\boldsymbol{V}$ to $\mathbf{0}\boldsymbol{V}$, it means the current through that power switches have exceded the limit current ($\boldsymbol{I_{AB(max)}}$), protection system is triggered. **Figure 4-26** shows the continue design of protection system about the latch off.

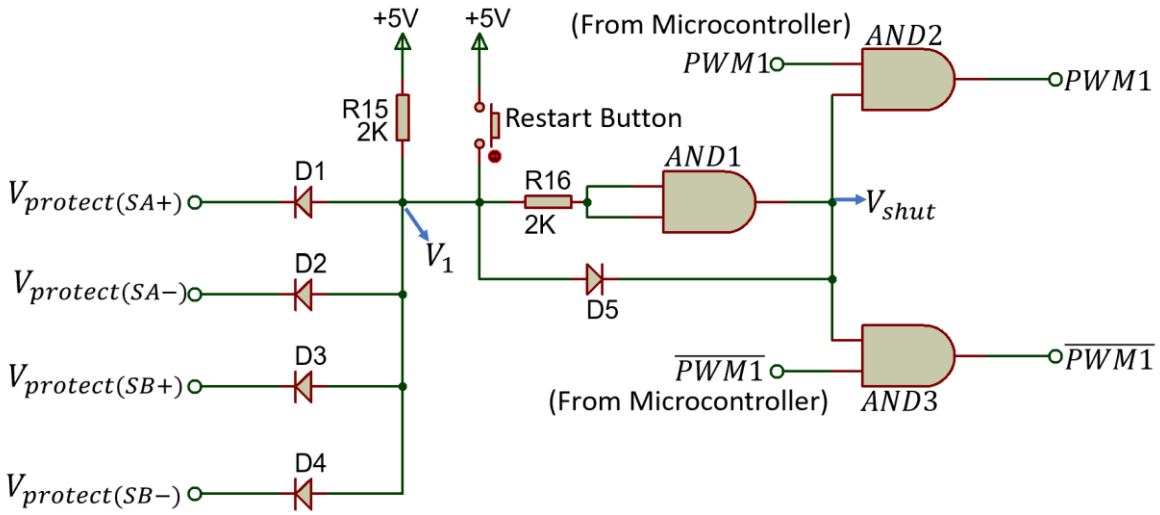


**Figure 4-26 : Latch off circuit in protection system.**

The $\boldsymbol{PWM}$ signal $\boldsymbol{PWM1}$ and $\boldsymbol{\overline{PWM1}}$ from microcontroller is connected to two $\boldsymbol{AND}$ gates as shown in **Figure 4-26**. When $\boldsymbol{V_{shut}} = \mathbf{0}$, the output of $\boldsymbol{AND2}$ and $\boldsymbol{AND3}$ are always equal to $\mathbf{0}\boldsymbol{V}$, which shut down $\boldsymbol{PWM}$ control. When $\boldsymbol{V_{shut}} = \mathbf{5}\boldsymbol{V}$, $\boldsymbol{AND2}$ and $\boldsymbol{AND3}$ are connected, the $\boldsymbol{PWM}$ signal can be sent out.

When system is working under normal condition, all protection signals $\boldsymbol{V_{protect}}$ keep at $\mathbf{5}\boldsymbol{V}$. As shown in **Figure 4-26**, since the point $\boldsymbol{V_1}$ is pulled up to $+\mathbf{5}\boldsymbol{V}$ with resistor $\boldsymbol{R15}$, $\boldsymbol{V_1}$ is also equal to 5V, the diode $\boldsymbol{D1}$ to $\boldsymbol{D4}$ are turned off. Because the voltage $\boldsymbol{V_1}$ is $\mathbf{5}\boldsymbol{V}$, $\boldsymbol{AND1}$ is turned on, $\boldsymbol{V_{shut}}$ is equal to $\mathbf{5}\boldsymbol{V}$, $\boldsymbol{PWM}$ signal is working. When H-Bridge system encounters an overcurrent event and the protection system is activated, one of protection signal changes from $\mathbf{5}\boldsymbol{V}$ to $\mathbf{0}\boldsymbol{V}$. The corresponded diode ($\boldsymbol{D1}$ to $\boldsymbol{D4}$) turns on which clamp the $\boldsymbol{V_1}$ to $\mathbf{0.7}\boldsymbol{V}$. As result, $\boldsymbol{AND1}$ turns off, $\boldsymbol{V_{shut}} = \mathbf{0}\boldsymbol{V}$ and

$\boldsymbol{PWM}$ signal is cut off. Once $\boldsymbol{V_{shut} = 0V}$, $\boldsymbol{V_1}$ is clamped to $\boldsymbol{0.7V}$ by diode $\boldsymbol{D5}$. At this point, even all $\boldsymbol{V_{protect}}$ signal turns back to $\boldsymbol{5V}$, $\boldsymbol{V_{shut}}$ is still equal to $\boldsymbol{0V}$ which cut off $\boldsymbol{PWM}$ signal. The diode $\boldsymbol{D5}$ here act as a latch off.

The latch off act by diode $\boldsymbol{D5}$ here is unlocked by pressing the Restart Button shown in **Figure 4-26**. After pressing the button, $\boldsymbol{V_1}$ turns to $\boldsymbol{5V}$, and then turns on $\boldsymbol{AND1}$ gate, hence $\boldsymbol{V_{shut}}$ is turned to $\boldsymbol{5V}$ again. Finally, the output of $\boldsymbol{PWM}$ signal can be unlocked. In addition, all protection signals $\boldsymbol{V_{protect}}$ and $\boldsymbol{V_{shut}}$ will be monitored by the microcontroller. Four red LEDs represent four $\boldsymbol{V_{protect}}$ signals. Once the protection of power switch is triggered, the representative red LED will light, and microcontroller shut down the $\boldsymbol{PWM}$ and all power system. After restart, the microcontroller monitors the voltage on $\boldsymbol{V_{shut}}$, after $\boldsymbol{V_{shut}}$ is changed from $\boldsymbol{0V}$ to $\boldsymbol{5V}$, the microcontroller can start to produce $\boldsymbol{PWM}$ signal.

In conclusion, two protection systems work together to protect H-Bridge system. In the $\boldsymbol{I_{DC}}$ Overcurrent Detector, if current $\boldsymbol{I_{DC}}$ excess the $\boldsymbol{I_{DC(max)}}$ ($\boldsymbol{28A}$), the protection is acted and then shut H-Bridge system. In the power switch protection system, the protection will be triggered if $\boldsymbol{I_{AB}}$ over the $\boldsymbol{I_{AB(max)}}$ ($\boldsymbol{62.5A}$). If only the $\boldsymbol{I_{DC}}$ Overcurrent Detector protection is activated, it means that the total current $\boldsymbol{I_{DC}}$ exceeds the set max current ($\boldsymbol{I_{DC(max)} = 28A}$), the whole system will be shut down. If the power switch protection is triggered, it means the total current flows through the H-Bridge inverter has over $\boldsymbol{62.5V}$ which may damage MOSFET in H-Bridge inverter. After the

system is shut down, according to the light LED on the board, the represents power switch should be checked if it is damaged.

## 4.7 Chapter Conclusion

This chapter demonstrates all electrical circuit design for experimental platform of grid-connected H-Bridge power inverter. Section 4.1 presents the design of $\boldsymbol{LCL}$ filter. The $\boldsymbol{LCL}$ filter is designed to filter high harmonic component in output voltage and current from H-Bridge inverter. In addition, a suitable design of $\boldsymbol{LCL}$ filter should contain enough energy to maintains current direction and voltage level during dead time. Section 4.2 describes the calculations of $\boldsymbol{PI}$ parameter in $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current controller. Suitable $\boldsymbol{PI}$ parameter can ensure responses speed and stability of close-loop system. Section 4.3 in this chapter presents the gate drive circuit of power switches in H-Bridge inverter. Section 4.4 presents the whole voltage and current sampling system. This section presents an improvement detector circuit design based on $\boldsymbol{ACPL\_7900}$ modules. The improvement includes reconstruction of input power supply of $\boldsymbol{ACPL\_7900}$ for providing accurate and stable reading of high switching current component. The detector module is used for current and voltage detector in system. Instead of using multiple different voltage level power supply described in datasheet of $\boldsymbol{ACPL\_7900}$, the improved detector circuit only requires $\boldsymbol{\pm 12V}$ power supply and it is available to be used in different kind of circuit for detecting current or voltage. Section 4.5 shows the current polarity detector system flowed with the current detector to provide accurate current direction information for DTC operation. Finally, in section

4.6, the protection system of whole H-Bridge platform is described. In addition, with power switches protection system, every power switches in a H-Bridge inverter can be monitored and protected.

This chapter presents the design of hardware platform used in dead time compensation in grid connected H-Bridge inverter experiment. Next chapter presents the microcontroller system design. Describing dead time compensation operation with $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current controller operation in $\boldsymbol{PWM}$ system.

# *Chapter 5*

# Microcontroller System Design

The previous chapter described the development of hardware platform used to validate the proposed dead time compensation system. This chapter describes the software-based control system based on a $\boldsymbol{STM32}$ microcontroller.

ARM and DSP are two main important cores in microcontroller system. ARM core is a powerful control unit which cooperating with different peripherals to achieve various of functions.

ARM based microcontroller is widely used in many areas such as embedded system, server, CPU and mobile device etc.

Digital Signal Processor (DSP) is specialized designed to optimize the operation of digital signal processing. DSP contains high operating frequency (can be higher than 2000MHz) and high calculation speed especially for mathematics and floating-point calculation. As result, DSP is widely used in audio signal processing, telecommunication and digital image processing etc.

Now, most of microcontrollers is designed based on ARM cores because of its powerful control unit. In addition, company such as ***ST*** and ***TI*** starts to build ARM based microcontroller with DSP function, which provides flexible control and high calculation speed at same time. The $\boldsymbol{STM32F407}$ serious microcontroller contains high operation frequency, DSP instruction and various of peripherals (especially are

multiple ***ADC*** peripherals and ***PWM*** system). In addition, ***STM32*** microcontroller software library is abundant, which can make control and calculation easier and faster. The microcontroller ***STM32F407ZGT6*** is used in this project and more detail is introduced later in this section.

In the first section in this chapter, ***PWM*** generator system in microcontroller ***STM32F407ZGT6*** will be described. ***PWM*** system is the basic system in this project, dead time compensation, ***PI*** and ***PLL*** control is all based on ***PWM*** system.

In the second section, the method of achieving dead time compensation in microcontroller will be introduced and described. In section 4.5, the zero-crossing detector circuit has been described, this section describes the process of using output signal from zero-crossing detector to control dead time compensation.

In the third section, the method of achieving ***PLL*** in microcontroller will be introduced. Also including the introduction of ***ADC*** system in microcontroller.

In the fourth section, the ***PI*** current controllers in microcontroller is described.

## The *STM32F407ZGT6* microcontroller

The ***STM32*** series microcontroller is widely used in many areas such as electrical control, signal processing, motor control and medical equipment etc. It contains varies of peripherals such as GPIO, UART, SPI, I2C, DCA and ADC etc. The varieties of peripherals can be easily integrated with different sensors and communication interface, which increase the adaptation rate of ***STM32*** microcontroller used in industrial range. With many years of development on its Arm Cortex CPU, the ***STM32*** microcontroller

and its embedded system are faster and more powerful. In addition, considering its low prices, $\boldsymbol{STM32}$ microcontroller becomes one of the most widely adopted microcontrollers in the world. In addition, the DSP instruction and FPU function can increase calculation speed for $\boldsymbol{PI}$ calculation in complex control systems. In this application, the $\boldsymbol{STM32F407ZGT6}$ microcontroller is chosen because its high operation frequency, which can reach to $\boldsymbol{168MHz}$, provides sufficient data throughput rate for the DTC and grid control system.

## 5.1 The $\boldsymbol{PWM}$ system in microcontroller $\boldsymbol{STM32F407ZGT6}$

This section introduces $\boldsymbol{PWM}$ system in microcontroller $\boldsymbol{STM32F407ZGT6}$.

$\boldsymbol{PWM}$ signal can be produced by using a comparator such as $\boldsymbol{MAX913}$ to compare the signals from two signal generators. Also, there are varies of $\boldsymbol{PWM}$ generator ICs such as $\boldsymbol{SG3525A}$ can be chosen to produce $\boldsymbol{PWM}$ signal. The main idea of producing $\boldsymbol{PWM}$ signal is comparing a fundamental frequency modulation signal with a high switching frequency carrier signal. In hardware design of $\boldsymbol{PWM}$ generator, the sine modulation signal and triangle carrier signal can be produced easily by signal generation. Their voltage normally changes between positive and negative peak value with $\boldsymbol{0V}$ offset voltage. The goal of generating $\boldsymbol{PWM}$ signal in $\boldsymbol{STM32}$ microcontroller is same, but the way for creating the modulation $\boldsymbol{V_{sin}(t)}$ signal, carrier $\boldsymbol{V_{tri}(t)}$, and output $\boldsymbol{PWM}$ signals are different.

In ***STM32*** microcontroller, the Timer peripheral is used by ***PWM*** system. **Figure 5-1** shows how the Timer system is used to achieve the ***PWM*** system in microcontroller. The upper waveform shows timer counter, ***CNT***, which is a staircase counting up and then down and so is equivalent to $\boldsymbol{V_{tri}(t)}$. The lower waveform shows the ***PWM*** output from ***PWM1***.

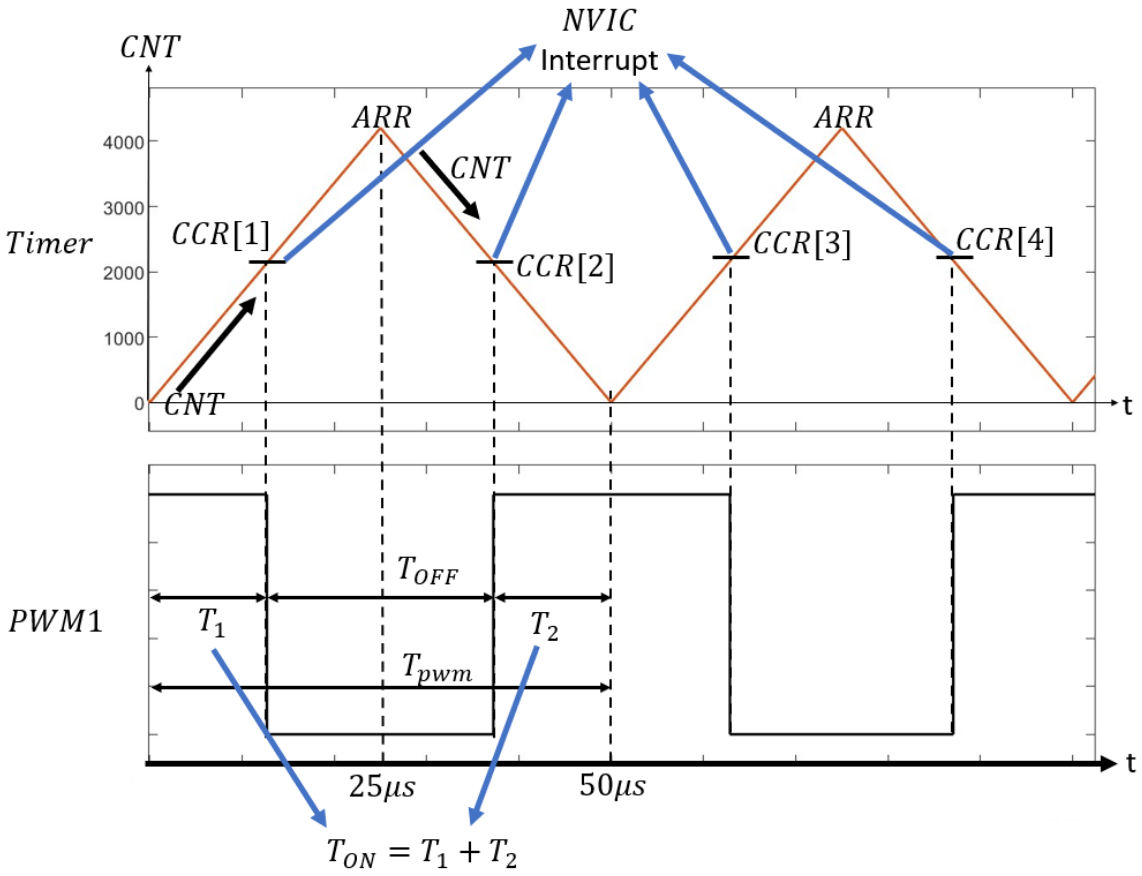


**Figure 5-1 : The Timer system and output *PWM1* signal.**

There are three important factors in the ***PWM*** system of microcontroller which are the value of ***ARR***, ***CNT*** and ***CCR***. The ***CNT*** is the counter number which start to count from 0 to ***ARR***, and then count down from ***ARR*** to 0. The time for each step of ***CNT*** is related to the Timer peripheral in the microcontroller. In the ***STM32F407ZGT6*** microcontroller, the crystal oscillator frequency is ***168MHz***, therefore every Timer

increment corresponds to $\mathbf{5.95}\boldsymbol{ns}$ time step. Hence every count of $\boldsymbol{CNT}$ (0 to 1, 1 to 2, 2 to 3…) takes $\mathbf{5.95}\boldsymbol{ns}$. As shown in **Figure 5-1**, the whole counting progress of $\boldsymbol{CNT}$ creates carrier signal $\boldsymbol{V_{tri}(t)}$ in microcontroller. The value of $\boldsymbol{ARR}$ is decided by $\boldsymbol{PWM}$ switching frequency of $\boldsymbol{V_{tri}(t)}$. In this project, the switching frequency is $\mathbf{20}\boldsymbol{kHz}$, the time for half cycle of $\boldsymbol{V_{tri}(t)}$ is $\mathbf{25}\boldsymbol{\mu s}$, hence the time for $\boldsymbol{CNT}$ reach from 0 to $\boldsymbol{ARR}$ is also $\mathbf{25}\boldsymbol{\mu s}$. So, the $\boldsymbol{ARR}$ is equal to $\frac{\mathbf{25}\boldsymbol{\mu s}}{\mathbf{5.95}\boldsymbol{ns}} = \mathbf{4200}$. In microcontroller, the peak value of $\boldsymbol{V_{tri}(t)}$ is fixed and only dependent on the switching frequency.

The value of $\boldsymbol{CCR}$ decides the duty cycle of output $\boldsymbol{PWM}$ signal. When $\boldsymbol{CNT}$ is higher than $\boldsymbol{CCR}$, $\boldsymbol{PWM1}$ produces a low-level voltage. When $\boldsymbol{CNT}$ is lower than $\boldsymbol{CCR}$, $\boldsymbol{PWM1}$ produces a high-level voltage. If the value of $\boldsymbol{CCR}$ is kept constant, the duty cycle is kept constant as well. The time for updating $\boldsymbol{CCR}$ value is important in $\boldsymbol{PWM}$ system in microcontroller. For example, $\boldsymbol{CNT}$ increases from 0 to $\boldsymbol{ARR}$, and it is just over the $\boldsymbol{CCR}[\mathbf{1}]$ (the value of $\boldsymbol{CCR}[\mathbf{1}]$ is diagrammatically shown in Figure 5-1), $\boldsymbol{PWM1}$ produces low-level voltage. Now, if $\boldsymbol{CCR}$ value is directly changed to a higher value $\boldsymbol{CCR}[\mathbf{2}]$, and it is higher than $\boldsymbol{CNT}$, $\boldsymbol{PWM1}$ turns to high-level voltage instantly. As result, $\boldsymbol{PWM1}$ turns between high-level and low-level voltage multiple times in a half cycle of $\boldsymbol{V_{tri}(t)}$, hence the power switches turn on or off multiple times in a half cycle as well. This kind of situation should be avoided in the control of H-Bridge inverter to avoid spurious switching events. A latch system is used to avoid this situation to ensure that $\boldsymbol{PWM}$ output signal only change once per each half cycle of $\boldsymbol{V_{tri}(t)}$. In the $\boldsymbol{STM32F407}$ microcontroller, this latch function is performed by the shadow register.

The $\boldsymbol{NVIC}$(**Nested Vectored Interrupt Controller**) is an interrupt system that the program jumps out from main program loop temporarily to execute critical functions within the interrupt system, and then return back to the main program loop to continue progress. The interrupt system can be triggered in many ways in microcontroller. In the $\boldsymbol{PWM}$ system, the interrupt is triggered by every time $\boldsymbol{CNT}$ reaches $\boldsymbol{CCR}$ value.

For example, assuming that the first $\boldsymbol{CCR}$ value is $\boldsymbol{CCR}[\mathbf{1}]$, and $\boldsymbol{CNT}$ start from 0. When $\boldsymbol{CNT}$ over the $\boldsymbol{CCR}[\mathbf{1}]$, $\boldsymbol{PWM1}$ produces low-level voltage. Now, an interrupt system is trigger since $\boldsymbol{CNT}$ reached the value of $\boldsymbol{CCR}[\mathbf{1}]$, and then program jumps into the interrupt system. In the interrupt system, the next $\boldsymbol{CCR}$ value $\boldsymbol{CCR}[\mathbf{2}]$ is saved into the shadow register ready for updating while the latest $\boldsymbol{CCR}$ value remains $\boldsymbol{CCR}[\mathbf{1}]$. After $\boldsymbol{CNT}$ reach to the $\boldsymbol{ARR}$, the $\boldsymbol{CCR}$ value is updated to $\boldsymbol{CCR}[\mathbf{2}]$ held in the shadow register automatically. When $\boldsymbol{CNT}$ decreases from $\boldsymbol{ARR}$ and lower than the $\boldsymbol{CCR}[\mathbf{2}]$, $\boldsymbol{PWM1}$ produces high-level voltage. At same time, the next value $\boldsymbol{CCR}[\mathbf{3}]$ is saved into shadow register in the interrupt system, but the latest $\boldsymbol{CCR}$ value is still $\boldsymbol{CCR}[\mathbf{2}]$. Until $\boldsymbol{CNT}$ decreases to 0, the $\boldsymbol{CCR}$ value is updated to $\boldsymbol{CCR}[\mathbf{3}]$ automatically. After that, a new cycle of $\boldsymbol{V_{tri}(t)}$ starts again. Because of shadow register, it can be ensured that value of $\boldsymbol{PWM1}$ only changes once in every half cycle of $\boldsymbol{V_{tri}(t)}$. And the next $\boldsymbol{CCR}$ value will be given when every time $\boldsymbol{CNT}$ is equal to present $\boldsymbol{CCR}$ value. As result, the key for producing a $\boldsymbol{V_{sin}(t)}$ modulation signal in microcontroller is to use appropriate values of $\boldsymbol{CCR}$.

As described in section 2.2.2, the duty cycle in $\boldsymbol{PWM}$ system is $\boldsymbol{D = m_i = \frac{V_{sin}(t)}{\hat{V}_{tri}}}$ where $\boldsymbol{m_i}$ is modulation index and $\boldsymbol{V_{sin}(t)}$ is modulation signal. The on-duration time $\boldsymbol{T_{ON} = T_{pwm} * m_i}$. Because the frequency $\boldsymbol{f_{pwm} = \frac{1}{T_{pwm}}}$ is much higher than the grid sine wave frequency $\boldsymbol{f_{sin}}$, in a $\boldsymbol{PWM}$ cycle of duration of $\boldsymbol{T_{pwm}}$, two $\boldsymbol{CCR}$ values can be treated as same. The relationship between $\boldsymbol{T_{ON}}$ with $\boldsymbol{CCR}$ and $\boldsymbol{ARR}$ is,

$$\boldsymbol{T_{ON} = T_{pwm} * \left(\frac{CCR}{ARR}\right)} \tag{89}$$

The $\boldsymbol{D = \frac{T_{ON}}{T_{pwm}}}$. As result, the transfer equation of $\boldsymbol{CCR}$ is,

$$\boldsymbol{CCR = \frac{1}{2} ARR * \left(1 + \frac{V_{sin}(t)}{\hat{V}_{tri}}\right)} \tag{90}$$

Given that $\boldsymbol{f_{pwm} = 20kHz}$, $\boldsymbol{f_{sin} = f_{grid} = 50Hz}$, then $\boldsymbol{\frac{20kHz}{50Hz} = 400}$. There are 400 $\boldsymbol{T_{pwm}}$ intervals in a $\boldsymbol{V_{sin}}$ period, and the $\boldsymbol{PWM}$ updates on both up and down count, so that there are two $\boldsymbol{CCR}$ values in a $\boldsymbol{V_{tri}}$ period and totally $\boldsymbol{800 = 400 * 2}$ $\boldsymbol{CCR}$ in a $\boldsymbol{V_{sin}}$ period.

Rather than calculate the sinewave values in real-time, a look-up table (LUT) is used to speed the calculations. 800 $\boldsymbol{CCR}$ values were calculated and stored during a program initialisation. It should be notes that many years ago only quarter cycle would have been stored in LUT, but the increase availability of onboard memory does not impose such restrictions today.

As described in this section, the two $\boldsymbol{CCR}$ values in one $\boldsymbol{T_{pwm}}$ is treated as same because the $\boldsymbol{f_{pwm}}$ is much higher than $\boldsymbol{f_{sin}}$. As result, another operation is that 400 $\boldsymbol{CCR}$ values are saved in a LUT, and each $\boldsymbol{CCR}$ is used twice in each $\boldsymbol{T_{pwm}}$.

**Figure 5-2** (a) shows a $V_{sin}$ period and the $CNT$ triangular wave, and **Figure 5-2** (b) shows the first and last three $T_{pwm}$ periods in a single $V_{sin}$ period.

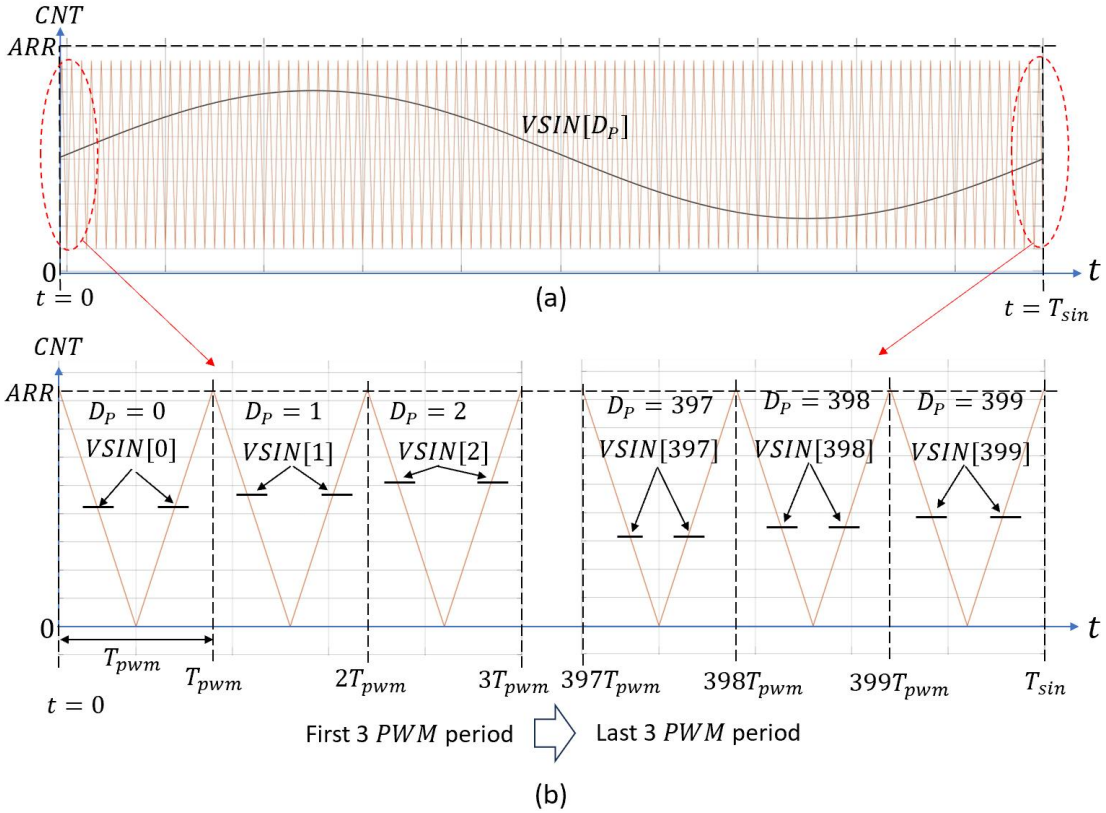


**Figure 5-2: (a) $VSIN[D_P]$ and $CNT$ in a $V_{sin}$ period, (b) The $CCR$ value in the first and last 3 $T_{pwm}$ periods.**

The calculated $\boldsymbol{CCR}$ values during the program initialisation are saved in an array $\boldsymbol{VSIN[D_P]}$, the $\boldsymbol{D_P}$ is the index number of the array. Since a $\boldsymbol{V_{sin}}$ period is divided into $\boldsymbol{400\ T_{PWM}}$, the $\boldsymbol{D_P}$ is the driver point index of array which increases from $\boldsymbol{0}$ to $\boldsymbol{399}$ in every $\boldsymbol{V_{sin}}$ period.

Referring to **Figure 5-2** (b), the first $\boldsymbol{V_{sin}}$ period starts at $\boldsymbol{t = 0}$, because of the $\boldsymbol{400}$ $\boldsymbol{T_{pwm}}$ periods in a $\boldsymbol{V_{sin}}$ period, the $\boldsymbol{V_{sin}}$ period will end at $\boldsymbol{t = 400 * T_{pwm} = T_{sin}}$ (where $\boldsymbol{T_{sin} = \frac{1}{f_{sin}}}$). The second $\boldsymbol{V_{sin}}$ period then starts at $\boldsymbol{t = T_{sin}}$. On the other hand,

the index $\boldsymbol{D_P = 0}$ at the start of the $\boldsymbol{V_{sin}}$ period, and it is increased by 1 every $\boldsymbol{T_{pwm}}$ from $\boldsymbol{0}$ to $\boldsymbol{399}$ in a $\boldsymbol{V_{sin}}$ period. Then $\boldsymbol{D_P}$ is then reset to $\boldsymbol{0}$ at the start of a new $\boldsymbol{V_{sin}}$ period. Referring to **Figure 5-2** (b), the $\boldsymbol{CCR}$ value in $\boldsymbol{VSIN}[\boldsymbol{0}]$ is the modulation value used in either side in this $\boldsymbol{T_{pwm}}$ period, similar to the modulation value in $\boldsymbol{VSIN}[\boldsymbol{1}]$ to $\boldsymbol{VSIN}[\boldsymbol{399}]$.

As described previously in the description of the $\boldsymbol{CCR}$ value updates in interrupt system, the next $\boldsymbol{CCR}$ value will be updated in the present interrupt system. As shown in **Figure 5-2**, new $\boldsymbol{V_{sin}}$ period starts at $\boldsymbol{t = 0}$ **or** $\boldsymbol{T_{sin}}$ and $\boldsymbol{D_P = 0}$, $\boldsymbol{CNT}$ counts down and reaches to the $\boldsymbol{CCR = VSIN}[\boldsymbol{0}]$, interrupt system is triggered and the next $\boldsymbol{CCR}$ value is still $\boldsymbol{VSIN}[\boldsymbol{0}]$, so $\boldsymbol{D_P}$ remains unchanged. After $\boldsymbol{CNT}$ has counted down to 0, then $\boldsymbol{CNT}$ starts to count up, and eventually reaches $\boldsymbol{VSIN}[\boldsymbol{0}]$ again, the interrupt system is triggered again. The next $\boldsymbol{CCR}$ value should be updated to the $\boldsymbol{VSIN}[\boldsymbol{1}]$, so the driver point index $\boldsymbol{D_p}$ is updated ($\boldsymbol{D_P + 1}$) to take right value in $\boldsymbol{VSIN}$ LUT.

**Figure 5-3** shows the flowchart of $\boldsymbol{CCR}$ update in the interrupt system.

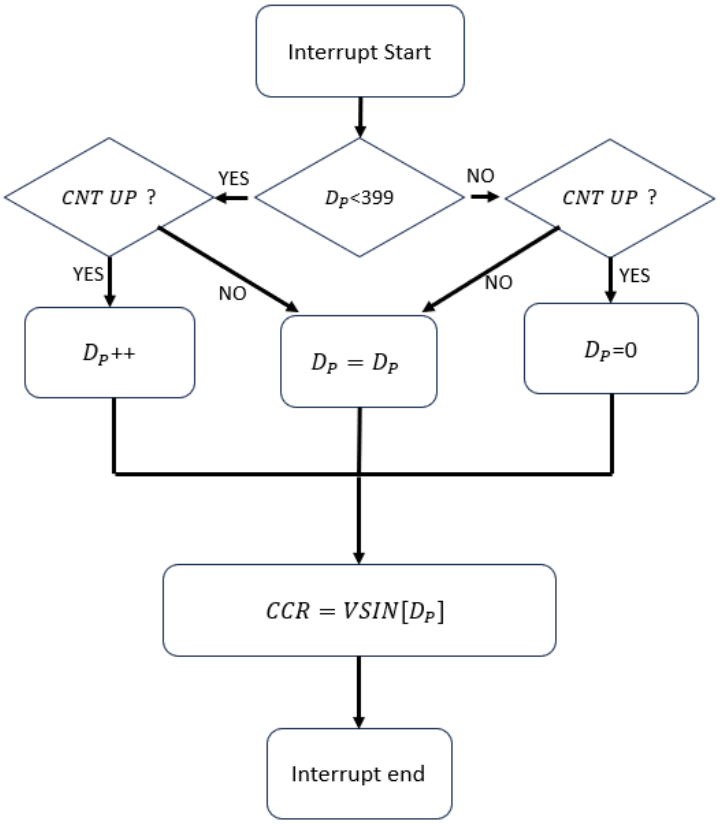


**Figure 5-3: The flowchart of $CCR$ value update.**

## 5.2 Design and implementation of Dead Time Compensation

The proposed deadtime compensation ($\boldsymbol{DTC}$) and phase lag compensation ($\boldsymbol{PLC}$) methods has been described in section 3.3. The concept is to add a deadtime compensation value $\boldsymbol{V_{DTC}}$ and a phase lag compensation value $\boldsymbol{V_{PLC}}$ into the $\boldsymbol{V_{sin}(t)}$ to create a new modulation signal. In this section, the design and implementation of the proposed compensation system responsible for updating the $\boldsymbol{CCR}$ value in microcontroller is described.

Firstly, reviewing the Dead Time Compensation through the block diagram in **Figure 5-4**.

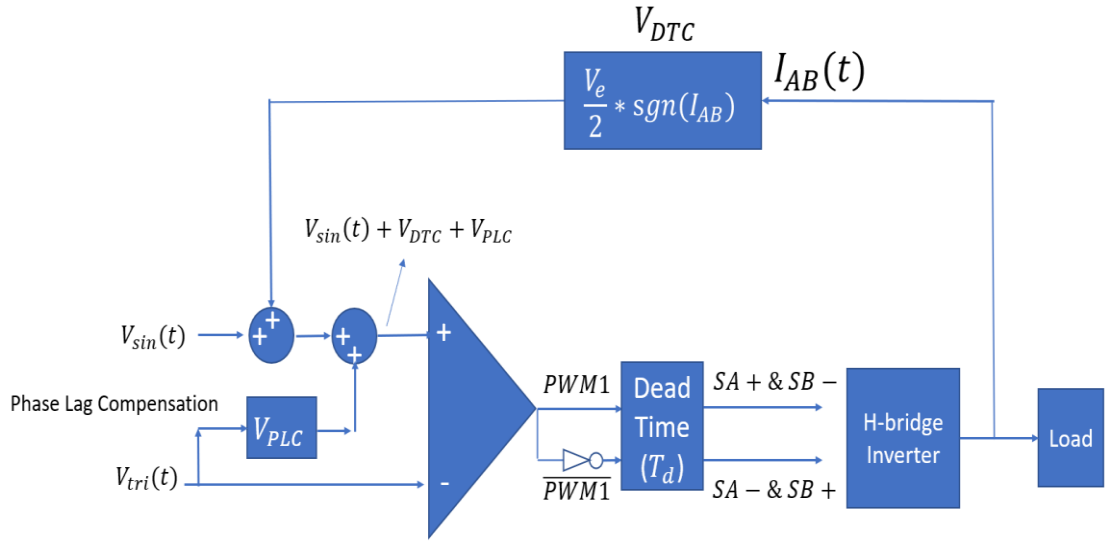


**Figure 5-4: Block diagram of *PWM* system with *DTC* and *PLC***

The final modulation signal is $\boldsymbol{V_{sin}(t) + V_{DTC} + V_{PLC}}$. The transfer of $\boldsymbol{V_{sin}(t)}$ into $\boldsymbol{CCR}$ has been described. The value of $\boldsymbol{V_{DTC}}$ and $\boldsymbol{V_{PLC}}$ used in microcontroller are named $\boldsymbol{V_{DTC(CCR)}}$ and $\boldsymbol{V_{PLC(CCR)}}$ to avoid confusion with the voltage-based signals described previously. The voltage based deadtime compensation voltage signal is $\boldsymbol{V_{DTC}}$ given by equation (36) in section 3.3.1.

$$\boldsymbol{V_{DTC} = \frac{1}{2}V_e * sgn(I_{AB}) = 2 * f_{pwm} * T_d * \hat{V}_{tri} * sgn(I_{AB})} \qquad (36)$$

The signal $\boldsymbol{sgn(I_{AB}) = 1}$ when $\boldsymbol{I_{AB} > 0}$, while $\boldsymbol{sgn(I_{AB}) = -1}$ when $\boldsymbol{I_{AB} < 0}$. Since the value of $\boldsymbol{\hat{V}_{tri}}$ in voltage based signal is $\boldsymbol{1}$, while the $\boldsymbol{\hat{V}_{tri}}$ in microcontroller is equal to $\boldsymbol{\frac{1}{2}ARR = 2100}$ since $\boldsymbol{CNT}$ signal extends from 0 to 4200 and has to represent $\pm\boldsymbol{\hat{V}_{tri}}$. The deadtime compensation value used in $\boldsymbol{CCR}$ mode in microcontroller is $\boldsymbol{V_{DTC(CCR)}}$ which is equal to,

$$V_{DTC(CCR)} = 2100 * V_{DTC} = 2100 * \frac{1}{2} V_e * sgn(I_{AB}) \quad (91)$$

On the other hand, the $V_{PLC}$ is the voltage-based phase lag compensation value can be calculated according to the equation (37) in section 3.3.2.

$$V_{PLC} = 4 * f_{pwm} * T_{delay} * \hat{V}_{tri} \quad (37)$$

Same to the relation between the $V_{DTC}$ and $V_{DTC(CCR)}$, the $CCR$ value of phase lag compensation is $V_{PLC(CCR)}$ which is equal to $2100 * V_{PLC}$. Since the $T_{delay}$ is equal to $\frac{1}{2} T_d$ (half the dead time), $V_{PLC(CCR)}$ is,

$$V_{PLC(CCR)} = 2100 * V_{PLC} = 2100 * \frac{1}{2} V_e \quad (92)$$

Now, focusing on how to add the $V_{DTC(CCR)}$ in microcontroller. According to the current polarity information from the $MAX913$ current zero-crossing detector circuit, $V_{DTC(CCR)}$ is calculated and saved in an array named $VDTC[D_{P(DTC)}]$, the $D_{P(DTC)}$ is the drive point index of $VDTC$ array which increases from $0$ to $799$ in a $V_{sin}$ period. With the $DTC$ system, the voltage-based modulation signal is equal to $V_{sin}(t) + V_{DTC}$, while in the microcontroller, the $CCR$ value with $DTC$ is equal to $VSIN[D_P] + VDTC[D_{P(DTC)}]$. The $LUT$ in $VSIN[D_P]$ is fixed. The $V_{DTC(CCR)}$ value calculated in the present $V_{sin}$ period will be saved in the $VDTC[D_{P(DTC)}]$ and then they will be used at the next $V_{sin}$ period.

**Figure 5-5** shows the new modulation value in the first and last 3 $T_{pwm}$ periods in a $V_{sin}$ period.

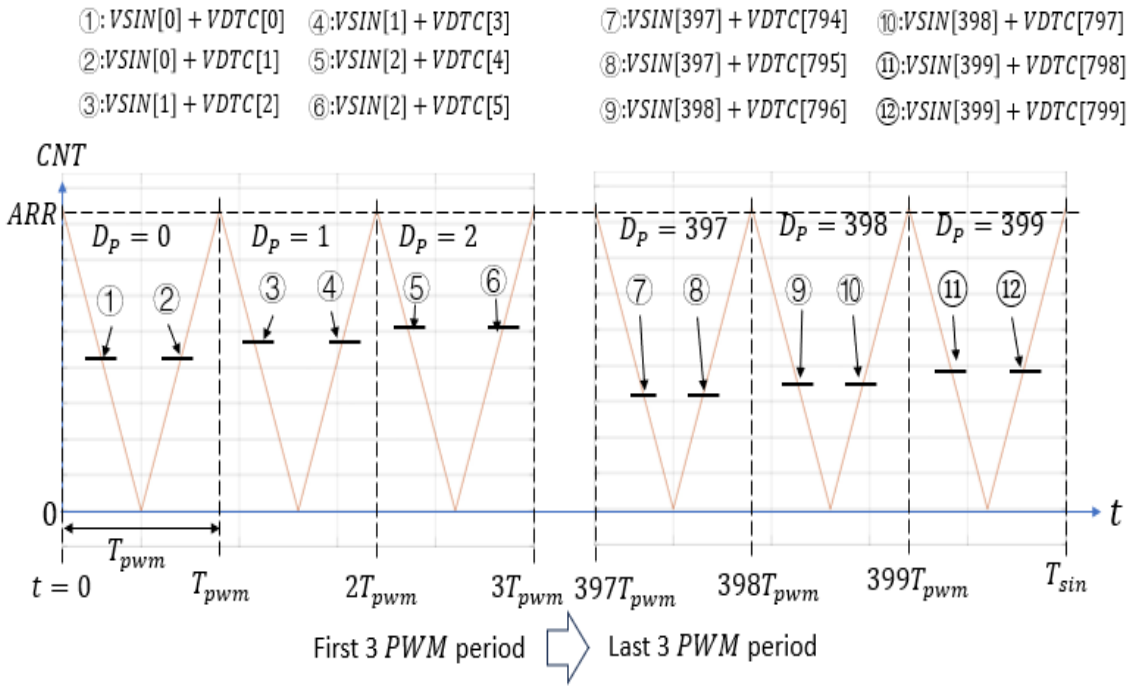


**Figure 5-5: The $CCR$ value with $DTC$ system in the first and last 3 $T_{pwm}$ periods in a $V_{sin}$ period.**

The operation of the $\boldsymbol{VSIN[D_P]}$ $\boldsymbol{LUT}$ has been described previously. Referring to **Figure 5-5**, the index $\boldsymbol{D_P}$ increases every $\boldsymbol{PWM}$ cycle, while the index $\boldsymbol{D_{P(DTC)}}$ increments every half $\boldsymbol{PWM}$ cycle from $\mathbf{0}$ (at $\boldsymbol{t = 0}$) to $\mathbf{799}$ (at $\boldsymbol{t = T_{sin}}$) in a $\boldsymbol{V_{sin}}$ period. The $\boldsymbol{DTC}$ system requires the current signal polarity information to update the $\boldsymbol{V_{DTC(CCR)}}$ value, and during the current zero-crossing, it is possible that current polarity changes in a single $\boldsymbol{T_{pwm}}$ period. In order to take full information of current polarity, two $\boldsymbol{V_{DTC(CCR)}}$ calculations in a single $\boldsymbol{T_{pwm}}$ are required. As result, $\boldsymbol{D_{P(DTC)} + 1}$ in every half $\boldsymbol{T_{pwm}}$.

Referring to **Figure 5-5**, in the first $\boldsymbol{V_{sin}}$ period, all $\boldsymbol{V_{DTC(CCR)}}$ value in $\boldsymbol{VDTC[D_{P(DTC)}]}$ are $\boldsymbol{0}$. The $\boldsymbol{V_{sin}}$ period starts at $\boldsymbol{t = 0}$, $\boldsymbol{CNT}$ counts down to $\boldsymbol{VSIN[0]}$, which trigger the interrupt program. During this interrupt program, the next $\boldsymbol{CCR}$ should be equal to $\boldsymbol{VSIN[0] + VDTC[1]}$ as shown in **Figure 5-5**. Because all $\boldsymbol{V_{DTC(CCR)}}$ in the first $\boldsymbol{V_{sin}}$ period is $\boldsymbol{0}$, the next $\boldsymbol{CCR}$ is equal to $\boldsymbol{VSIN[0]}$. After updating next $\boldsymbol{CCR}$, the $\boldsymbol{V_{DTC(CCR)}}$ will be calculated and saved in the $\boldsymbol{VDTC[0]}$. Then this interrupt program is finished. The next interrupt program is triggered when $\boldsymbol{CNT}$ counts up to the $\boldsymbol{VSIN[0]}$ again. Then $\boldsymbol{D_P + 1}$, and $\boldsymbol{D_{P(DTC)} + 1}$, the next $\boldsymbol{CCR}$ is equal to $\boldsymbol{VSIN[1] + VDTC[2] = VSIN[1] + 0}$. Then, another $\boldsymbol{V_{DTC(CCR)}}$ will be calculated and saved in the $\boldsymbol{VDTC[1]}$. When the $\boldsymbol{D_{P(DTC)}}$ increases to $\boldsymbol{799}$ at the final $\boldsymbol{T_{pwm}}$ of the first $\boldsymbol{V_{sin}}$ period, all $\boldsymbol{V_{DTC(CCR)}}$ values are saved in the $\boldsymbol{VDTC[D_{P(DTC)}]}$ array. The next $\boldsymbol{V_{sin}}$ period starts at $\boldsymbol{t = T_{sin}}$, at this moment, the $\boldsymbol{D_P}$ and $\boldsymbol{D_{P(DTC)}}$ turns back to $\boldsymbol{0}$.The $\boldsymbol{CNT}$ counts down to the $\boldsymbol{VSIN[0] + VDTC[0]}$ and the interrupt program is triggered. In this interrupt program, the next $\boldsymbol{CCR}$ is updated firstly which is equal to $\boldsymbol{VSIN[0] + VDTC[1]}$. Then, the $\boldsymbol{V_{DTC(CCR)}}$ saved from last $\boldsymbol{V_{sin}}$ period in the $\boldsymbol{VDTC[0]}$ is updated to a new $\boldsymbol{V_{DTC(CCR)}}$ value. After $\boldsymbol{CNT}$ counts up and reaches to $\boldsymbol{VSIN[0] + VDTC[1]}$, another interrupt program is triggered. In this interrupt program, the next $\boldsymbol{CCR}$ is updated firstly which is equal to $\boldsymbol{VSIN[1] + VDTC[2]}$. Then, the old $\boldsymbol{V_{DTC(CCR)}}$ in $\boldsymbol{VDTC[1]}$ is updated to a new one calculated from present $\boldsymbol{V_{sin}}$ period. Similar to the rest value in the $\boldsymbol{VDTC[D_{P(DTC)}]}$ in this $\boldsymbol{V_{sin}}$ period. In conclusion of the $\boldsymbol{DTC}$ system in microcontroller, the $\boldsymbol{V_{DTC(CCR)}}$ value is calculated and updated in $\boldsymbol{VDTC}$ array in every $\boldsymbol{V_{sin}}$ period and then they will be used to update $\boldsymbol{CCR}$ at next $\boldsymbol{V_{sin}}$ period.

In the $\boldsymbol{PLC}$ system, the value of $\boldsymbol{V_{PLC}}$ is only related to the carrier signal $\boldsymbol{V_{tri}}$. The $\boldsymbol{V_{PLC}} = +\frac{\mathbf{1}}{\mathbf{2}}\boldsymbol{V_e}$ during the half period of $\boldsymbol{T_{pwm}}$ when $\boldsymbol{V_{tri}}$ is decreasing from $+\widehat{\boldsymbol{V}}_{\boldsymbol{tri}}$ to $-\widehat{\boldsymbol{V}}_{\boldsymbol{tri}}$. On the other hand, the $\boldsymbol{V_{PLC}} = -\frac{\mathbf{1}}{\mathbf{2}}\boldsymbol{V_e}$ during another half period of $\boldsymbol{T_{pwm}}$ when $\boldsymbol{V_{tri}}$ is increasing from $-\widehat{\boldsymbol{V}}_{\boldsymbol{tri}}$ to $+\widehat{\boldsymbol{V}}_{\boldsymbol{tri}}$. In microcontroller system, the count up of $\boldsymbol{CNT}$ represents the time period of $\boldsymbol{V_{tri}}$ changing from $-\widehat{\boldsymbol{V}}_{\boldsymbol{tri}}$ to $+\widehat{\boldsymbol{V}}_{\boldsymbol{tri}}$. While the count down of $\boldsymbol{CNT}$ represtents the time period of $\boldsymbol{V_{tri}}$ changing from $+\widehat{\boldsymbol{V}}_{\boldsymbol{tri}}$ to $-\widehat{\boldsymbol{V}}_{\boldsymbol{tri}}$. According to equation (92) shown in this section, the $\boldsymbol{V_{PLC(CCR)}} = +\mathbf{2100} * \frac{\mathbf{1}}{\mathbf{2}}\boldsymbol{V_e}$ when $\boldsymbol{CNT}$ counts down, while $\boldsymbol{V_{PLC(CCR)}} = -\mathbf{2100} * \frac{\mathbf{1}}{\mathbf{2}}\boldsymbol{V_e}$ when $\boldsymbol{CNT}$ counts up. After adding $\boldsymbol{PLC}$ system into $\boldsymbol{PWM}$ system, the $\boldsymbol{CCR} = \boldsymbol{VSIN}[\boldsymbol{D_P}] + \boldsymbol{VDTC}\left[\boldsymbol{D_{P(DTC)}}\right] + \boldsymbol{V_{PLC(CCR)}}$. If the interrupt program is acted when $\boldsymbol{CNT}$ count down, the next value of $\boldsymbol{V_{PLC(CCR)}}$ should be equal to $-\mathbf{2100} * \frac{\mathbf{1}}{\mathbf{2}}\boldsymbol{V_e}$, so the next $\boldsymbol{CCR}$ is equal to $\boldsymbol{VSIN}[\boldsymbol{D_P}] + \boldsymbol{VDTC}\left[\boldsymbol{D_{P(DTC)}}\right] - \mathbf{2100} * \frac{\mathbf{1}}{\mathbf{2}}\boldsymbol{V_e}$. On the other hand, if the interrupt program is triggered when $\boldsymbol{CNT}$ count up, the next value of $\boldsymbol{V_{PLC(CCR)}}$ should be equal to $+\mathbf{2100} * \frac{\mathbf{1}}{\mathbf{2}}\boldsymbol{V_e}$, and the next $\boldsymbol{CCR}$ is equal to $\boldsymbol{VSIN}[\boldsymbol{D_P}] + \boldsymbol{VDTC}\left[\boldsymbol{D_{P(DTC)}}\right] + \mathbf{2100} * \frac{\mathbf{1}}{\mathbf{2}}\boldsymbol{V_e}$.

**Figure 5-6** shows the flowchart of whole $\boldsymbol{PWM}$ system contains the $\boldsymbol{DTC}$ and $\boldsymbol{PLC}$ system.

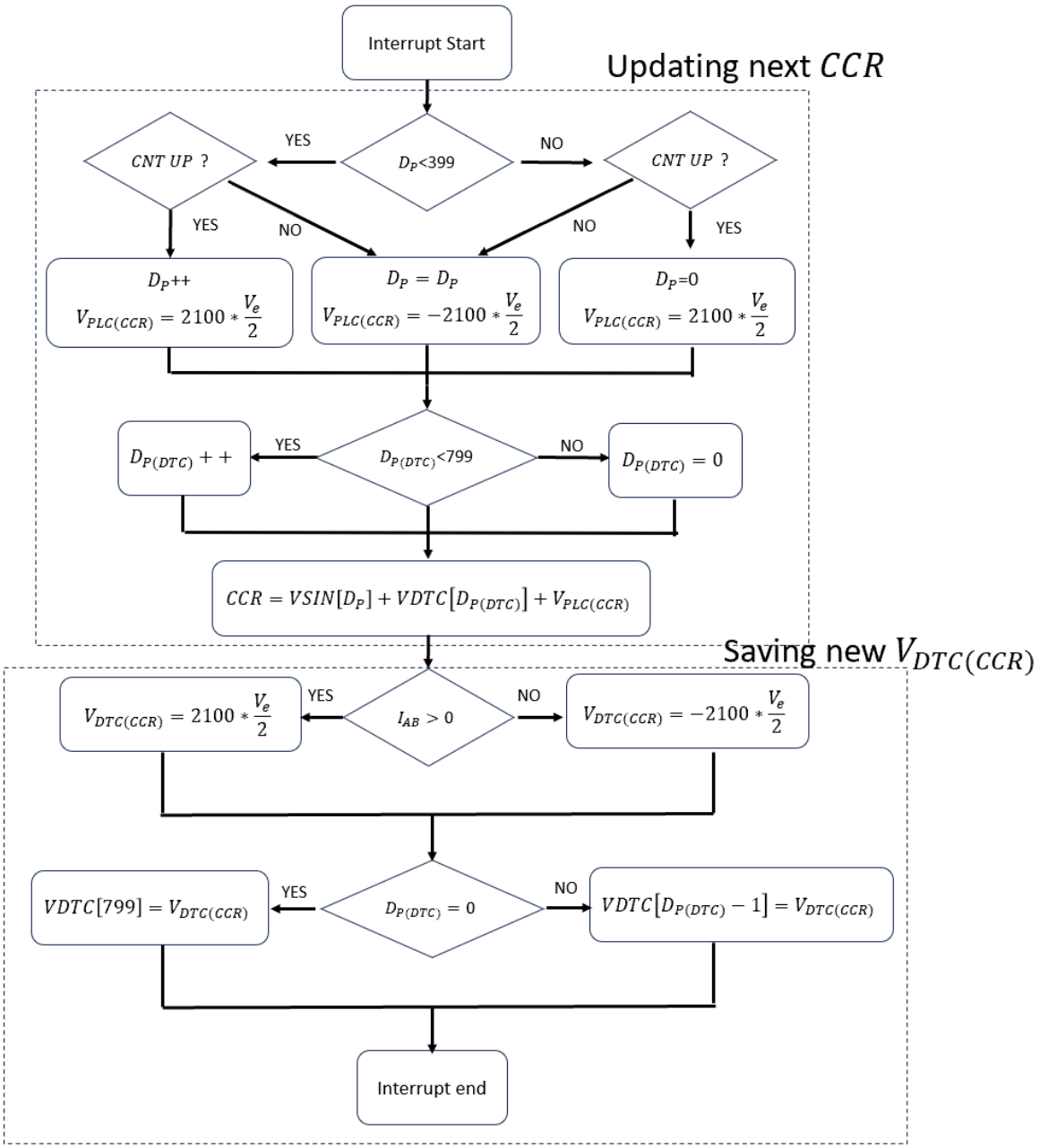


**Figure 5-6 : Flowchart for *PWM* update interrupt featuring Dead Time Compensation**

As shown in **Figure 5-6**, the whole ***PWM*** system in microcontroller is consisted of two parts, the first part is updating next ***CCR*** with ***DTC*** and ***PLC***, the second part is saving the ***DTC*** value for next $V_{sin}$ period. It should be noticed that the new ***DTC*** value is

saved in the point of array $\boldsymbol{VDTC}[\boldsymbol{D_{P(DTC)}} - \mathbf{1}]$. So, when $\boldsymbol{D_{P(DTC)}} = \mathbf{0}$, the $\boldsymbol{DTC}$ value should be saved in the last block in array which is $\boldsymbol{VDTC}[\mathbf{799}]$.

In addition, it is clear to see that the $\boldsymbol{VSIN}$ LUT has no change, $\boldsymbol{DTC}$ and $\boldsymbol{PLC}$ is achieved by the value of $\boldsymbol{V_{DTC(CCR)}}$ in $\boldsymbol{VDTC}$ LUT and $\boldsymbol{V_{PLC(CCR)}}$.

# 5.3 *ADC* Sampling in microcontroller

The built-in $\boldsymbol{ADC}$ of $\boldsymbol{STM32F407}$ microcontroller is used to sample analogue values of the currents and voltages for the $\boldsymbol{PI}$ current controllers and $\boldsymbol{PLL}$. In this section, the transformation of analogue voltage and current signals via the $\boldsymbol{ADC}$ to controller signals will be explained.

In the previous two sections of this chapter, the $\boldsymbol{PWM}$ and dead time compensation system are introduced under the open-loop circuit condition. As result, all $\boldsymbol{CCR}$ values in the $\boldsymbol{VSIN}$ LUT are fixed. After adding $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current controller, the system is changed to close-loop system. After the $\boldsymbol{PWM}$ system is started with the initial $\boldsymbol{VSIN}$ LUT, the $\boldsymbol{CCR}$ value in $\boldsymbol{VSIN}$ LUT will be updated according to the feedback from output grid current $\boldsymbol{I_{grid}}$ and $\boldsymbol{V_{grid}}$. The calculation of $\boldsymbol{PLL}$, $\boldsymbol{PI}$ current controller and new $\boldsymbol{VSIN}$ LUT creation is all achieved in the Main program in the microcontroller.

**Figure 5-7** shows an example of the first and last 3 $\boldsymbol{T_{pwm}}$ period with $\boldsymbol{ADC}$ sample system.

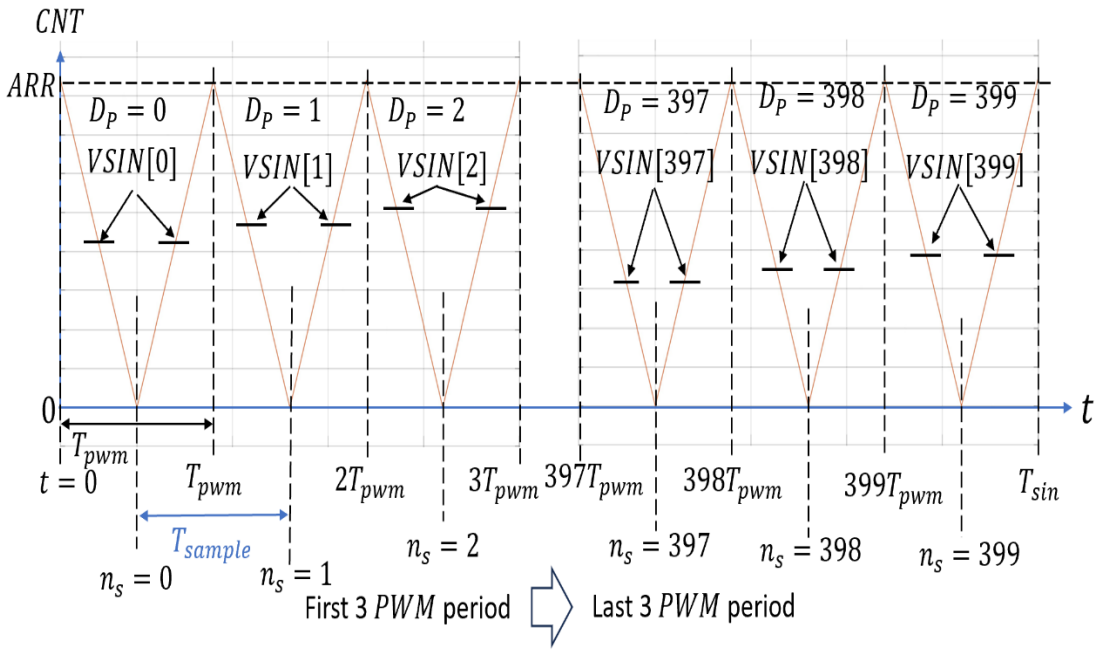


**Figure 5-7: The first and last 3 $T_{pwm}$ in a $V_{sin}$ period with *ADC* sample.**

The microcontroller reads the ***ADC*** sampling every $\boldsymbol{T_{sample} = T_{pwm}}$. ***STM32F407*** microcontroller contains multiple ***ADC*** systems. Two separated ***ADC*** systems are used to take the value of sample current $\boldsymbol{I_{grid}}$ and sample voltage $\boldsymbol{V_{grid}}$.

Two separated ***ADC*** systems are acted at same time to detect the current and voltage simultaneously, and they are triggered every $\boldsymbol{T_{sample}}$ by a fixed timer in the microcontroller.

Then, the sample current of $\boldsymbol{I_{grid}}$ and sample voltage $\boldsymbol{V_{grid}}$ will be saved into array $\boldsymbol{I_{adc}[n_s]}$ and $\boldsymbol{V_{adc}[n_s]}$ separately, the $\boldsymbol{n_s}$ is the index number of array and also represents the number of sample. Referring to **Figure 5-7**, every ***ADC*** sample is captured at the middle point of $\boldsymbol{T_{pwm}}$. Because a single ***CCR*** value saved in the ***VSIN*** LUT is used in a whole $\boldsymbol{T_{pwm}}$, the ***ADC*** sample is set at the middle point of $\boldsymbol{T_{pwm}}$ for calculating a respectively average modulation value in this $\boldsymbol{T_{pwm}}$.

Then the sampling value in $\boldsymbol{I_{adc}[n_s]}$ and $\boldsymbol{V_{adc}[n_s]}$ will be rescaled to represent the true analogue values as described before in section 4.4. The acceptable voltage range of $\boldsymbol{ADC}$ system is between 0 to $\boldsymbol{3.3V}$ and this is converted into a 12-bit value giving the range from 0 to 4095. Consider the 12-bits system of $\boldsymbol{ADC}$ sampling, the equation for current and grid calculation in microcontroller are shown below.

$$\boldsymbol{V_{grid} = (V_{adc}[n_s] - 1861) * \frac{3.3}{4095} * \frac{1}{0.016} = (V_{adc}[n_s] - 1861) * 0.05} \quad (93)$$

$$\boldsymbol{I_{grid} = (I_{adc}[n_s] - 1861) * \frac{3.3}{4095} * \frac{1}{0.08} = (I_{adc}[n_s] - 1861) * 0.01} \quad (94)$$

Then, the calculated voltage and current is saved in the array $\boldsymbol{V_{grid(\alpha)}[n_s]}$ and $\boldsymbol{I_{grid(\alpha)}[n_s]}$ since the $\boldsymbol{\alpha}$ axis value is directly equal to the value from output of H-Bridge inverter.

The arrays are used because they are required in the $\boldsymbol{\alpha}$ to $\boldsymbol{\beta}$ transformation, and then the $\boldsymbol{\alpha\beta}$ to $\boldsymbol{dq}$ transformation. The value in $\boldsymbol{V_{grid(\alpha)}[n_s]}$ and $\boldsymbol{I_{grid(\alpha)}[n_s]}$ is used in $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current controller to produce a dynamically change $\boldsymbol{V_{sin}(t)}$, which is used to create new values in $\boldsymbol{VSIN}$ LUT to replace old values. And this $\boldsymbol{VSIN}$ LUT is kept updated through the $\boldsymbol{PLL}$ and current control calculation. The detail of operation of $\boldsymbol{PLL}$, $\boldsymbol{PI}$ current controller and $\boldsymbol{PWM}$ system in close-loop system is described in later section in this chapter. **Figure 5-8** shows the basic flow chart of the close-loop system.

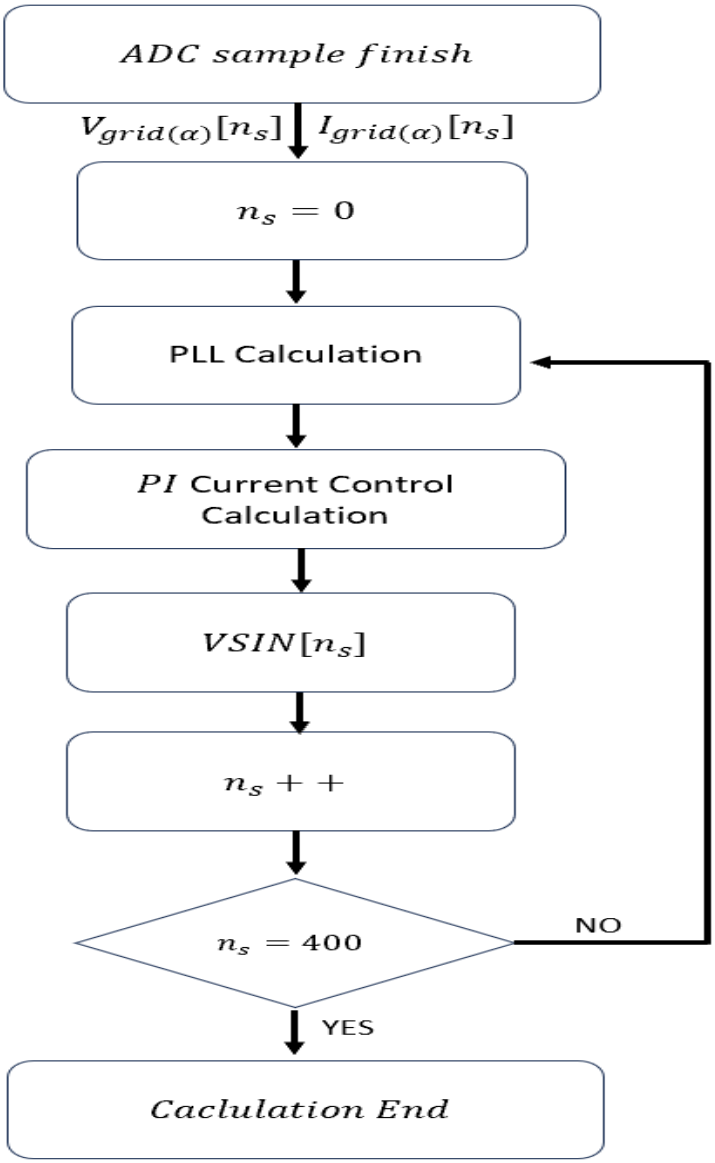


**Figure 5-8: Basic close-loop system for calculating *VSIN LUT*.**

As shown in **Figure 5-8**, in a loop, the index $n_s$ is increased from **0** to **399** for filling the new ***VSIN*** LUT array. The value stored in the new ***VSIN*** **LUT** is calculated through the ***PLL*** and ***PI*** current controller in the main program according to the sample current and voltage value in the $V_{grid(\alpha)}[n_s]$ and $I_{grid(\alpha)}[n_s]$. The detail of how to update old ***VSIN*** LUT to new LUT is described in the next section.

# 5.4 Microcontroller system design of *PLL*

**Figure 5-9** shows the block diagram of ***PLL*** system.

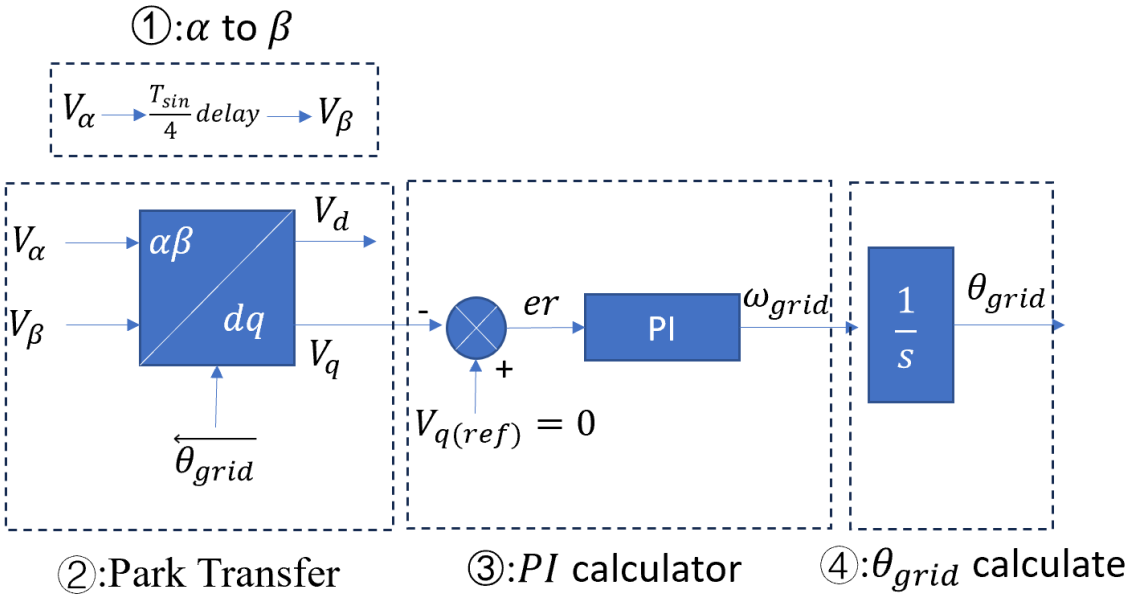


**Figure 5-9: Block diagram of *PLL*.**

As shown in **Figure 5-9**, the first step in the operation of the ***PLL*** is the generation of $\boldsymbol{\beta}$ value from $\boldsymbol{\alpha}$. Because of ***ADC*** sampling, $\boldsymbol{\alpha}$ value of current and voltage has been saved in the $\boldsymbol{I_{grid(\alpha)}[n_s]}$ and $\boldsymbol{V_{grid(\alpha)}[n_s]}$. The first step in ***PLL*** program is to calculate the $\boldsymbol{\alpha}$ to $\boldsymbol{\beta}$ reference frame values. The two arrays $\boldsymbol{I_{grid(\beta)}[n_s]}$ and $\boldsymbol{V_{grid(\beta)}[n_s]}$ are used to save $\boldsymbol{\beta}$ axis value of current and voltage. The next step is to transfer $\boldsymbol{\alpha\beta}$ to $\boldsymbol{dq}$ values. In the third step of ***PLL*** calculation, the frequency of grid voltage $\boldsymbol{\omega_{grid}}$ is calculated through the ***PI*** calculation. There are two main types of ***PI*** calculation, position algorithm and velocity algorithm. In position algorithm ***PI*** calculation, the input is the error value between the reference value and actual input value, while the output is the actual position of control signal. Equation (95) shows a basic ***PI*** equation in position algorithm in continuous time.

$$\boldsymbol{m(t) = K_p * er(t) + K_i * \int er(t)} \quad (95)$$

The $\boldsymbol{m(t)}$ is actual position of control signal and $\boldsymbol{er(t)}$ is error value and $\boldsymbol{er(t) = y_{ref}(t) - y(t)}$, $\boldsymbol{y_{ref}(t)}$ is the reference value and $\boldsymbol{y(t)}$ is the detected value. For the ***PLL*** system, $\boldsymbol{er(t) = V_{ref(q)}(t) - V_{grid(q)}(t)}$, and the output $\boldsymbol{m(t)}$ is the frequency of grid $\boldsymbol{\omega_{grid}(t)}$. Equation (95) shows the ***PI*** calculation in continuous time. In microcontroller, the discrete time ***PI*** is usually used. The discrete time ***PI*** of position algorithm is,

$$\boldsymbol{m(n) = K_p * er(n) + K_i * \sum_{i=0}^{n} er(i) * \Delta t} \quad (96)$$

The time different $\boldsymbol{\Delta t}$ is equal to sample time $\boldsymbol{T_{sample}}$, the $\boldsymbol{\sum_{i=0}^{n} er(i)}$ means sum of errors.

In many applications it may be necessary to change the controller parameters for different operating conditions and/or operation modes. For example, quite often systems have a start-up controller which is used to carefully drive system from zero to nominal operating point. When the nominal operating point is reached, main controller takes over operation. Sometimes the transition between start-up and main control causes a disturbance (bump) in system response due to a mismatch between the values of the state variables and gains of start-up and main controller. Similar effects can be seen when system transition from manual to automatic control and vice versa. As result, many platforms operation requirements usually demand that manual/automatic changeover be made in the so-called "bumpless" manner.

One bumpless method is called velocity algorithm ***PI*** calculation. Instead of producing $\boldsymbol{m(n)}$ directly, velocity algorithm produces the change in the value of the manipulated

variable for each sample. Equation (97) shows the change value of manipulated variable $\Delta \boldsymbol{m}(\boldsymbol{n})$ in discrete time.

$$\Delta \boldsymbol{m}(\boldsymbol{n}) = \boldsymbol{m}(\boldsymbol{n}) - \boldsymbol{m}(\boldsymbol{n-1}) = \boldsymbol{K_p} * [\boldsymbol{er}(\boldsymbol{n}) - \boldsymbol{er}(\boldsymbol{n-1})] + \boldsymbol{K_i} * \boldsymbol{er}(\boldsymbol{n}) * \Delta \boldsymbol{t} \quad (97)$$

Now, present output signal $\boldsymbol{m}(\boldsymbol{n}) = \boldsymbol{m}(\boldsymbol{n-1}) + \Delta \boldsymbol{m}(\boldsymbol{n})$. At the time of changeover of manual/auto, the output value from the manual $\boldsymbol{m}(\boldsymbol{n-1})$ is considered, since the $\Delta \boldsymbol{m}(\boldsymbol{n})$ is very small at this time, the new output signal calculated form velocity algorithm ***PI*** calculator is very close to the output from manual mode. As result, the "bump" is eliminated.

In this research, the velocity algorithm ***PI*** is used in the ***PLL*** and current control. **Figure 5-10** shows an example of working of $\boldsymbol{n_s}$ and the parameter which should be used in calculation.

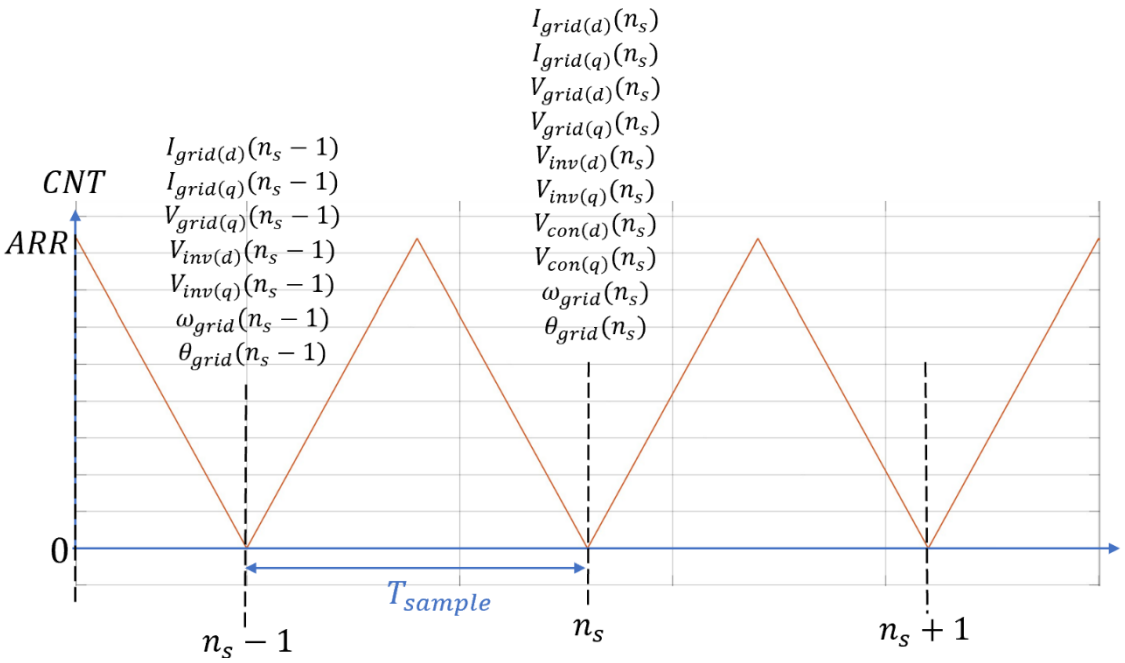


**Figure 5-10:** The example of calculation system with ***ADC*** $\boldsymbol{n_s}$ sample.

Referring to **Figure 5-10**, $\boldsymbol{n_s}$ is sample number, all value with ($\boldsymbol{n_s}$) is taken or calculated at present $\boldsymbol{T_{sample}}$, while all value with ($\boldsymbol{n_s - 1}$) is saved from the last $\boldsymbol{T_{sample}}$.

In the $\boldsymbol{PLL}$ system, $\boldsymbol{er(n_s) = V_{ref(q)}(n_s) - V_{grid(q)}(n_s)}$ , $\boldsymbol{er(n_s - 1) = V_{ref(q)}(n_s - 1) - V_{grid(q)}(n_s - 1)}$ . $\boldsymbol{\Delta t = T_{sample}}$ . The output $\boldsymbol{m(n_s) = \Delta\omega_{grid}(n_s)}$ represents the change in grid frequency. Assuming the reference value is kept constant, $\boldsymbol{V_{ref(q)}(n_s) = V_{ref(q)}(n_s - 1)}$ and so the $\boldsymbol{PI}$ calculation in $\boldsymbol{PLL}$ is,

$$\boldsymbol{\Delta\omega_{grid}(n_s) = K_p * \left[V_{grid(q)}(n_s - 1) - V_{ref(q)}(n_s)\right] + K_i * [er(n_s)] * T_{sample}} \quad (98)$$

The frequency of grid voltage $\boldsymbol{\omega_{grid}(n_s)}$ is,

$$\boldsymbol{\omega_{grid}(n_s) = \omega_{grid}(n_s - 1) + \Delta\omega_{grid}(n_s)} \quad (99)$$

Where $\boldsymbol{\omega_{grid}(n_s - 1)}$ is the frequency data from last sample time.

The next step is the calculation of angle $\boldsymbol{\theta_{grid}}$ of grid voltage, since $\boldsymbol{\theta_{grid}}$ can be calculated by integral of $\boldsymbol{\omega_{grid}}$, the equation of $\boldsymbol{\theta_{grid}}$ is,

$$\boldsymbol{\theta_{grid}(n_s) = \theta_{grid}(n_s - 1) + \omega_{grid}(n_s) * T_{sample}} \quad (100)$$

$\boldsymbol{\theta_{grid}(n_s - 1)}$ is the angle calculated from last sample time.

When $\boldsymbol{PLL}$ is stable, the actual $\boldsymbol{V_{grid(q)}}$ is equal to $\boldsymbol{V_{ref(q)}}$, the $\boldsymbol{\omega_{grid}}$ keeps constant and represents the frequency of grid voltage. So, the $\boldsymbol{\theta_{grid}}$ increases in the range from 0 to $\boldsymbol{2\pi}$ with a per sample increment step of $\boldsymbol{\omega_{grid} * T_{sample}}$.

**Figure 5-11** shows the flowchart of $\boldsymbol{PLL}$.

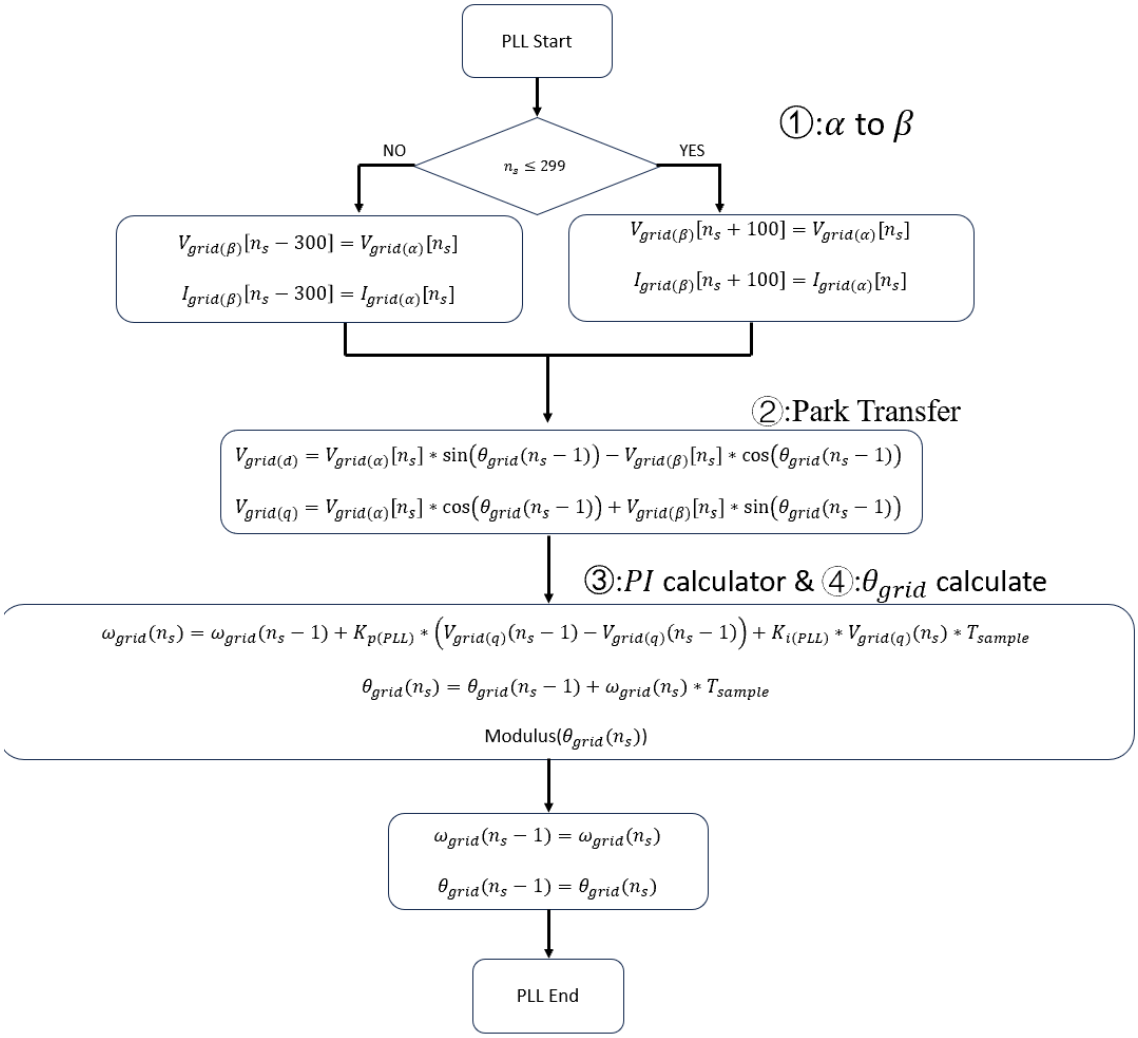


**Figure 5-11: The program flowchart of *PLL* system.**

# 5.5 Microcontroller system design of *PI* current controller

With the grid voltage obtained from the ***PLL***, voltage and current signals are sampled, the grid current is able to be calculated. **Figure 5-12** shows the block diagram of ***PI*** current controller.

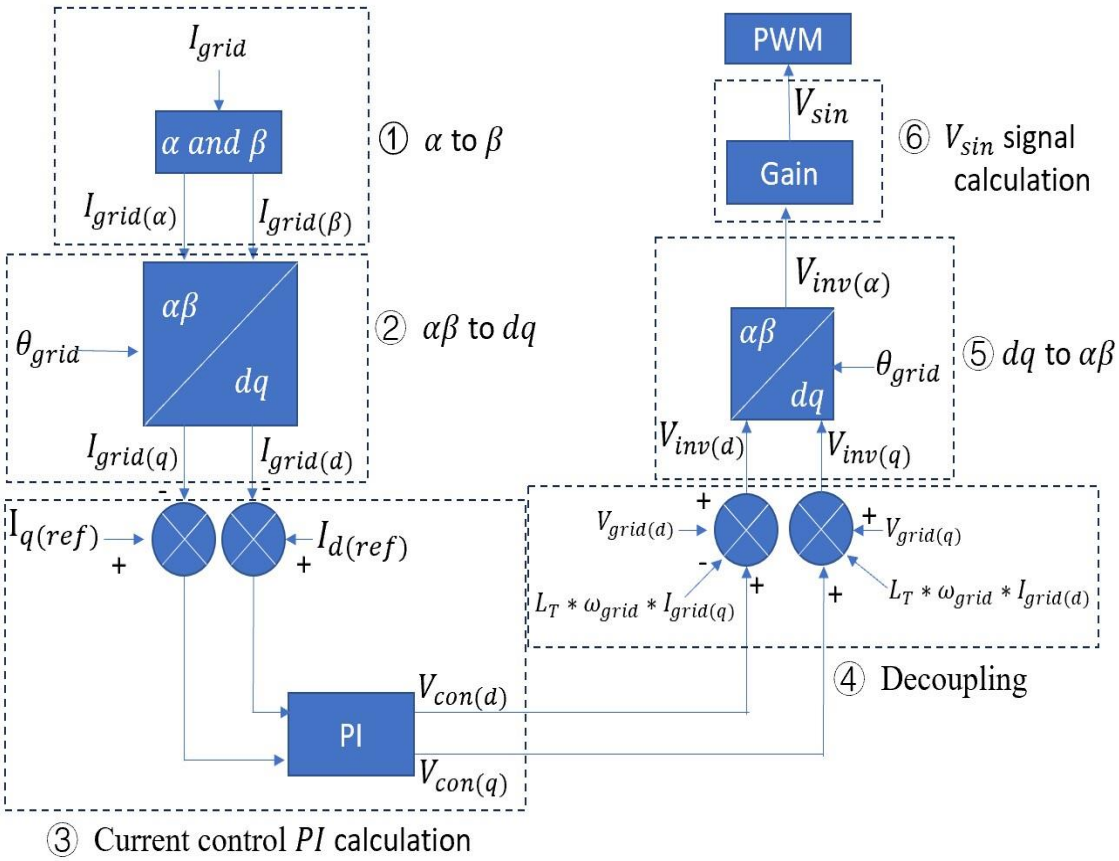


**Figure 5-12: Block diagram of *PI* current controller.**

The first step in current controller is creating $\boldsymbol{I_{grid(\beta)}}$ signal from $\boldsymbol{I_{grid(\alpha)}}$. This has been done at the beginning of the ***PLL*** system. So, the $\boldsymbol{\alpha\beta}$ current value are saved in the $\boldsymbol{I_{grid(\alpha)}[n_s]}$ and $\boldsymbol{I_{grid(\beta)}[n_s]}$**.** In step ②, the $\boldsymbol{\alpha\beta}$ values of current are transformed into $\boldsymbol{dq}$ values. Step ③ calculates the $\boldsymbol{dq}$ values of inverter voltage, $\boldsymbol{V_{con(d)}}$ and $\boldsymbol{V_{con(q)}}$, from the ***PI*** compensator. The velocity algorithm ***PI*** calculation is also used

in this calculation where the current error signal is calculated using $\boldsymbol{er(n_s) = I_{(ref)}(n_s) - I_{grid}(n_s)}$, while output is the control voltage $\boldsymbol{V_{con}}$. Equation (101) and (102) shows the $\boldsymbol{PI}$ calculation in current control in $\boldsymbol{dq}$ axis.

$$\boldsymbol{V_{con(d)}(n_s) = V_{con(d)}(n_s - 1) + K_{p(PI)} * [I_{grid(d)}(n_s - 1) - I_{grid(d)}(n_s)] + K_{i(PI)} * (I_{ref(d)}(n_s) - I_{grid(d)}(n_s)) * T_{sample}} \quad (101)$$

$$\boldsymbol{V_{con(q)}(n_s) = V_{con(q)}(n_s - 1) + K_{p(PI)} * [I_{grid(q)}(n_s - 1) - I_{grid(q)}(n_s)] + K_{i(PI)} * \left(I_{ref(q)}(n_s) - I_{grid(q)}(n_s)\right) * T_{sample}} \quad (102)$$

Step ④ is the decoupling system which removes the cross-coupled terms from the calculation giving the $\boldsymbol{dq}$ inverter voltages.

$$\boldsymbol{V_{inv(d)}(n_s) = V_{con(d)}(n_s) - \omega_{grid} L_T * I_{grid(q)}(n_s) + V_{grid(d)}(n_s)} \quad (103)$$

$$\boldsymbol{V_{inv(q)}(n_s) = V_{con(q)}(n_s) + \omega_{grid} L_T * I_{grid(d)}(n_s) + V_{grid(q)}(n_s)} \quad (104)$$

In step ⑤, the $\boldsymbol{V_{inv(\alpha)}}$ is calculated by $\boldsymbol{dq}$ to $\boldsymbol{\alpha\beta}$ transfer.

The penultimate step is to transform the $\boldsymbol{dq}$ inverter voltage to the $\boldsymbol{\alpha\beta}$ reference frame from which the time domain inverter signal can be obtained,

$$\boldsymbol{V_{inv} = V_{inv(\alpha)}(n_s) = V_{inv(d)}(n_s) * sin\left(\theta_{grid}(n_s)\right) + V_{inv(q)}(n_s) * cos\left(\theta_{grid}(n_s)\right)} \quad (105)$$

The final step is calculating modulation signal $\boldsymbol{V_{sin}}$ in microcontroller. According to equation about $\boldsymbol{V_{inv}}$ and $\boldsymbol{V_{sin}}$ in (14), $\boldsymbol{V_{sin}}$ is equal to,

$$\boldsymbol{V_{sin} = V_{inv} * \frac{\widehat{V}_{tri}}{V_{DC}}} \quad (106)$$

And according to equation (90) about the transfer between $\boldsymbol{V_{sin}}$ and $\boldsymbol{CCR}$. The final equation between $\boldsymbol{CCR}$ and $\boldsymbol{V_{inv}}$ is,

$$\boldsymbol{CCR} = \frac{\boldsymbol{ARR}}{\mathbf{2}} + \frac{\mathbf{1}}{\mathbf{2}} * \frac{\boldsymbol{ARR}}{\boldsymbol{V_{DC}}} * \boldsymbol{V_{inv}} \quad (107)$$

Since $\boldsymbol{ARR = 2100}$ and $\boldsymbol{V_{DC} = 100V}$, the $\boldsymbol{CCR = 2100 + 21 * V_{inv}}$. This $\boldsymbol{CCR}$ value is saved in the array $\boldsymbol{VSIN_{00}[n_s]}$ **or** $\boldsymbol{VSIN_{01}[n_s]}$. When one of the arrays is used to save the modulation signal value, another array is used for generating $\boldsymbol{PWM}$ signal. In the main program, $\boldsymbol{N_{array}}$ is used as flag to represent which $\boldsymbol{VSIN}$ array is currently being used. When $\boldsymbol{N_{array} = 0}$, the new modulation $\boldsymbol{CCR}$ value is saved in the $\boldsymbol{VSIN_{00}}$ array, while $\boldsymbol{VSIN_{01}}$ array is used as LUT for driving $\boldsymbol{PWM}$ signal. When $\boldsymbol{N_{array} = 1}$, the $\boldsymbol{VSIN_{01}}$ array is used to save new $\boldsymbol{CCR}$ value, while $\boldsymbol{VSIN_{00}}$ is used for driving $\boldsymbol{PWM}$ signal.

**Figure 5-13** shows the flowchart of $\boldsymbol{PI}$ current controller.

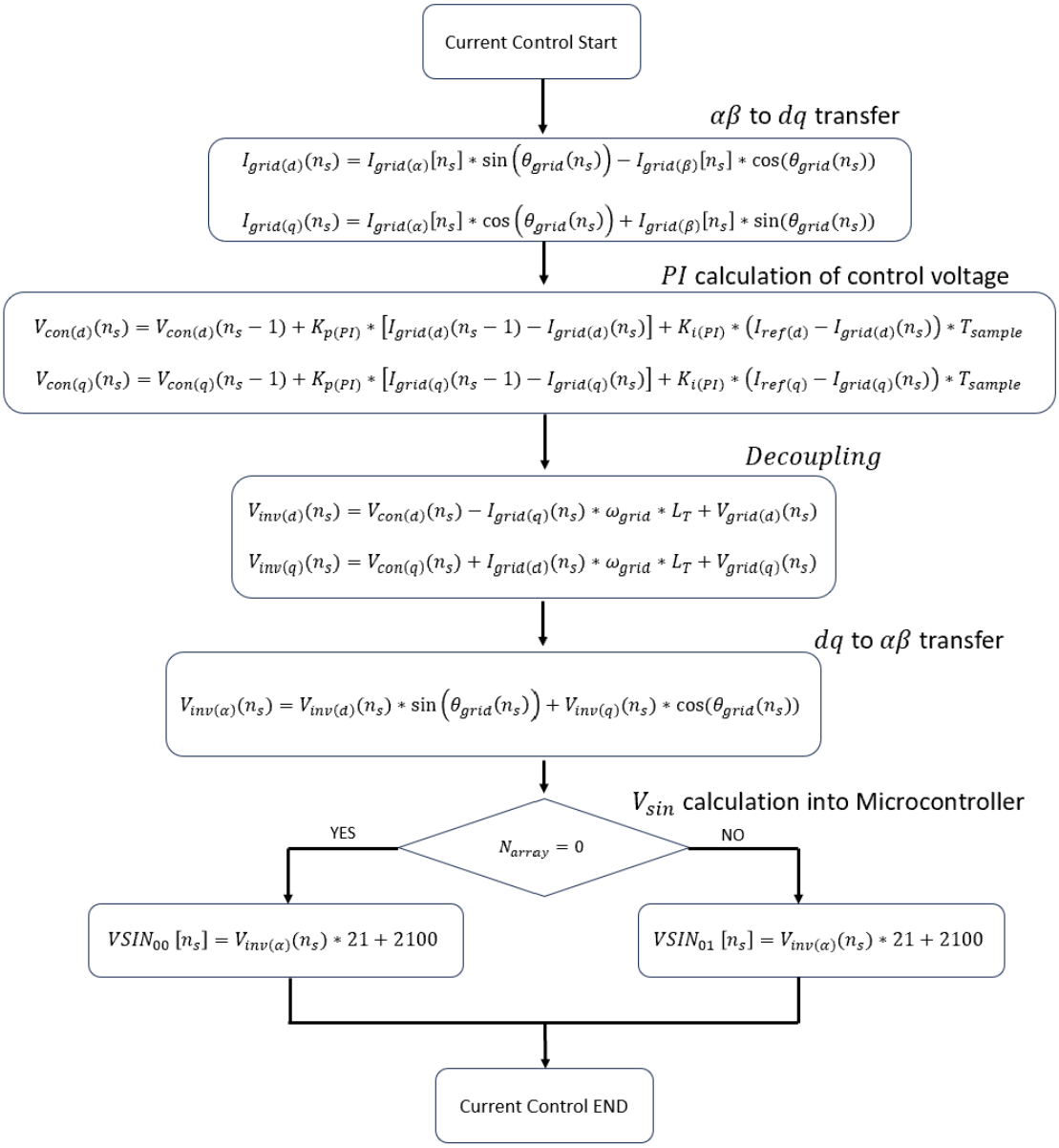


**Figure 5-13: The flowchart of *PI* current controller in microcontroller.**

# 5.6 A summary of the whole *PWM* timing and control system

The design and implementation of ***PWM*** system, dead time compensation, ***PLL*** and ***PI*** current controller sub-systems have been introduced separately in this chapter. In this final section, a description of cooperating of all sub-systems is provided.

After $\boldsymbol{ADC}$ sampling, microcontroller has obtained new values for the voltage and current signals and, therefore, $\boldsymbol{PWM}$ pulse width is updated. In order to do this a new value for $\boldsymbol{CCR}$ is determined and it is placed into $\boldsymbol{VSIN}$ LUT ($\boldsymbol{VSIN_{00}}$ or $\boldsymbol{VSIN_{01}}$) array. In a $\boldsymbol{V_{sin}}$ cycle, $\boldsymbol{VSIN}$ LUT is filled and will be used at next $\boldsymbol{V_{sin}}$ cycle. Therefore, it is essential that the time taken to perform every controller, $\boldsymbol{PLL}$ calculation and $\boldsymbol{PI}$ current calculation should be short than a sample ($\boldsymbol{PWM}$) period. During a sample period, not only the calculations time should be considered, but also the time for data transfer in and out from different arrays, $\boldsymbol{ADC}$ data transfer time should be considered. It is hard to ensure that all system can be finished in the time between two samples ($\boldsymbol{50\mu s}$) without influencing $\boldsymbol{PWM}$ update. As result, a system design for adapting the calculation speed of $\boldsymbol{STM32F407}$ microcontroller is described.

**Figure 5-14** shows the flowchart of main calculation program of current controller and $\boldsymbol{PLL}$. Instead of calculating each new $\boldsymbol{CCR}$ value after each $\boldsymbol{ADC}$ sample, the calculation starts after all $\boldsymbol{ADC}$ sampling in a $\boldsymbol{V_{sin}}$ cycle is all finished and saved.

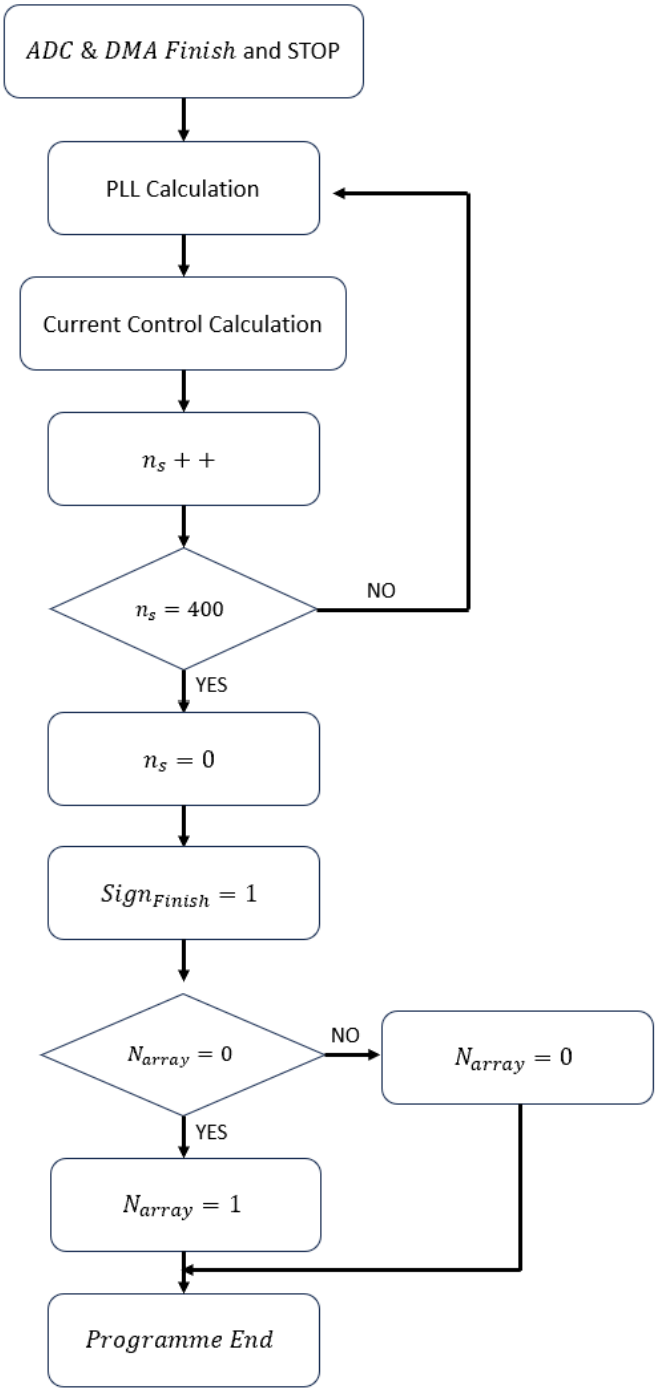


**Figure 5-14: Flowchart of Main calculation program.**

To speed up data transfer, Direct Memory Access (***DMA***) system is used to transfer the data from ***ADC*** register to certain index in an array without requiring an interrupt service routine. After the first $\boldsymbol{V_{sin}}$ period is finished, 400 ***ADC*** current and voltage

sample values are saved in the $\boldsymbol{I_{adc}[n_s]}$ and $\boldsymbol{V_{adc}[n_s]}$ arrays through $\boldsymbol{DMA}$ system. Then $\boldsymbol{ADC}$ and $\boldsymbol{DMA}$ system stops, and calculation starts according to the data saved in the $\boldsymbol{I_{adc}[n_s]}$ and $\boldsymbol{V_{adc}[n_s]}$. With the increase of $\boldsymbol{n_s}$ in the loop of program from $\mathbf{0}$ to $\mathbf{399}$, all new modulation values is calculated and filled into the LUT. Which $\boldsymbol{VSIN}$ array ($\boldsymbol{VSIN_{00}}$ or $\boldsymbol{VSIN_{01}}$) is used to save calculated modulation value is dependent on the value of $\boldsymbol{N_{array}}$ as described in the previous section. In the program shown in **Figure 5-14**, the flag $\boldsymbol{Sign_{Finish}}$ is introduced to shows the calculation finish condition. If the calculation is not finished, $\boldsymbol{Sign_{Finish}}$ keeps at $\mathbf{0}$. After calculation is finished and new LUT is filled, $\boldsymbol{Sign_{Finish}}$ turns to 1 to signify the $\boldsymbol{VSIN}$ array with new modulation values is ready to be used in the $\boldsymbol{PWM}$ system. And at the beginning of a next $\boldsymbol{V_{sin}}$ period ($\boldsymbol{D_P = 0}$), the updated LUT start to be used. Referring to **Figure 5-14**, after $\boldsymbol{Sign_{Finish} = 1}$, $\boldsymbol{N_{array}}$ turns, so that after next calculation is finished, the new modulation value can be saved in another $\boldsymbol{VSIN}$ array.

At the beginning of a new $\boldsymbol{V_{sin}}$ period, after $\boldsymbol{PWM}$ is driven by new LUT, the $\boldsymbol{ADC}$ system is restarted for taking new sample voltage and current for $\boldsymbol{PI}$ calculation. **Figure 5-15** shows flowchart of $\boldsymbol{PWM}$ interrupt service routine with current control, $\boldsymbol{PLL}$ and dead time compensation.

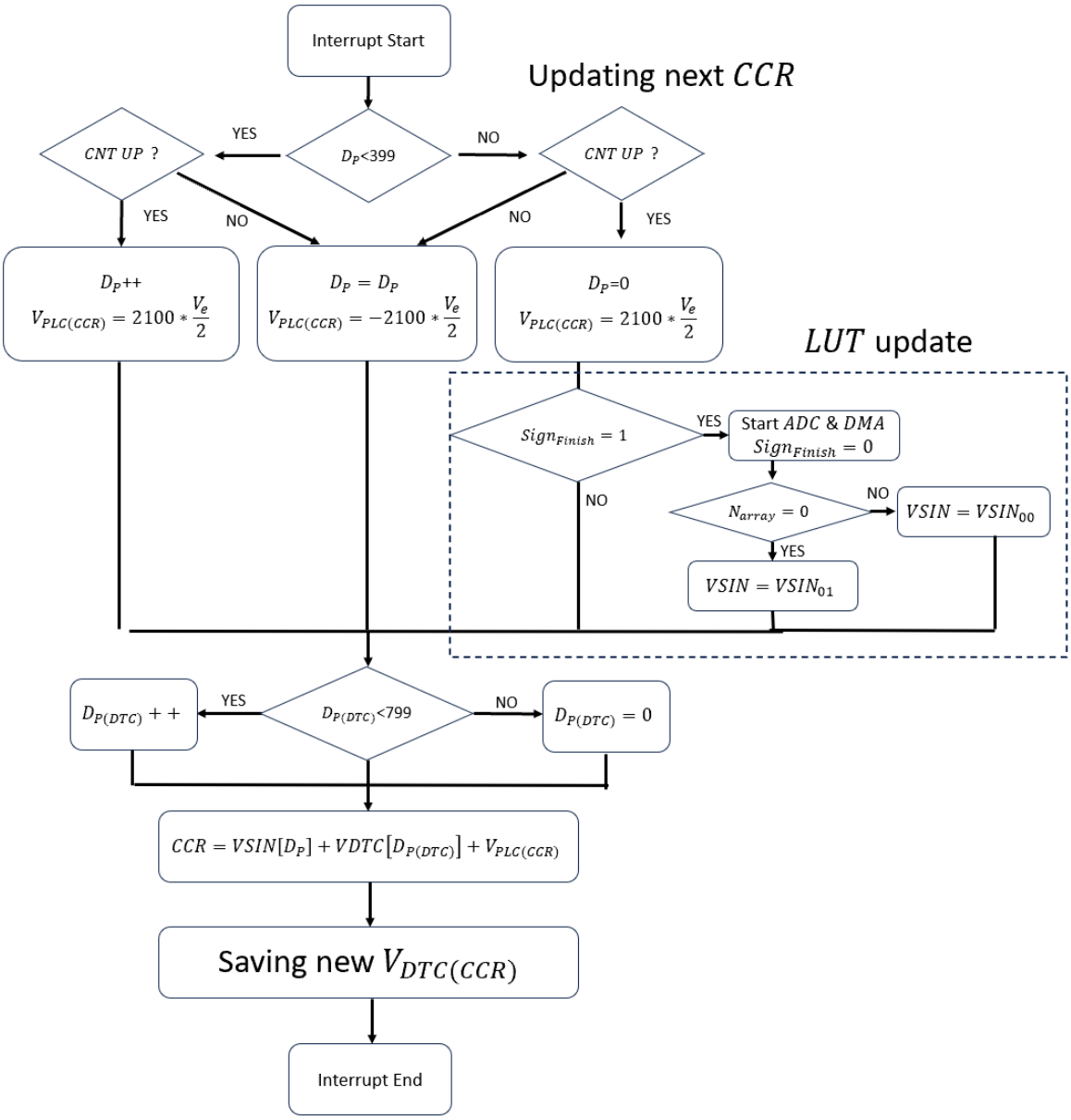


**Figure 5-15 : Flowchart of *PWM* interrupt program with DTC and grid connected system.**

As shown in **Figure 5-15**, $\boldsymbol{VSIN}$ LUT is only updated to $\boldsymbol{VSIN_{00}}$ or $\boldsymbol{VSIN_{01}}$ at the end of cycle according to $\boldsymbol{N_{array}}$ from the main program. After LUT updating, the $\boldsymbol{Sign_{Finish}}$ is set to 0 and the $\boldsymbol{ADC}$ system is restarted.

For example, at the first $\boldsymbol{V_{sin}}$ period, $\boldsymbol{VSIN_{00}}$ array is used as the LUT of $\boldsymbol{PWM}$ system, and the $\boldsymbol{ADC}$ system starts to capture voltage and current signals, in total $\mathbf{400}$ values are transferred by $\boldsymbol{DMA}$ in the first $\boldsymbol{V_{sin}}$ period. At the second $\boldsymbol{V_{sin}}$ period, $\boldsymbol{ADC}$ system is stopped, and calculation is started. During this time, $\boldsymbol{VSIN_{00}}$ LUT is being used to provide the sine wave reference values for $\boldsymbol{PWM}$ system, while new values of $\boldsymbol{CCR}$ are being calculated and saved in $\boldsymbol{VSIN_{01}}$ array. Assuming all calculation can be finished in this $\boldsymbol{V_{sin}}$ period. After all calculations are completed, $\boldsymbol{Sign_{Finish}}$ is set to $\mathbf{1}$, $\boldsymbol{VSIN}$ reference is changed from $\boldsymbol{VSIN_{00}}$ LUT to $\boldsymbol{VSIN_{01}}$ LUT ready for next $\boldsymbol{V_{sin}}$ period. At the third $\boldsymbol{V_{sin}}$ period, $\boldsymbol{ADC}$ system is restarted and $\boldsymbol{Sign_{Finish}}$ is changed to 0. After all, $\boldsymbol{ADC}$ sample is finished, the new $\boldsymbol{CCR}$ value is calculated and saved in $\boldsymbol{VSIN_{00}}$ array at the fourth cycle. In conclusion, $\boldsymbol{VSIN}$ LUT is updated every two $\boldsymbol{V_{sin}}$ period ($\boldsymbol{40ms}$) in this system. This way ensures that there is enough time in microcontroller to finish all calculations and data transfer without influencing the progress of $\boldsymbol{ADC}$ sample and $\boldsymbol{PWM}$ program. As described in this section, $\boldsymbol{ADC}$ sampling system is acted every period of $\boldsymbol{T_{pwm}}$, if $\boldsymbol{PWM}$ frequency is higher, $\boldsymbol{T_{pwm}}$ is shorter, and it is much harder to ensure every calculation can be finished in a short $\boldsymbol{T_{pwm}}$ time. By using the method described in this section, all $\boldsymbol{ADC}$ sample program are finished at the first $\boldsymbol{V_{sin}}$ period, and only once all calculations are finished, $\boldsymbol{Sign_{Finish}}$ changes to 1, the new LUT is updated. In this research, the update of LUT is acted every two $\boldsymbol{V_{sin}}$ periods. The key for $\boldsymbol{PLL}$ and current controller is maintaining their $\boldsymbol{dq}$ axis value to their reference value, and $\boldsymbol{dq}$ axis values are not changed significantly in every

cycle. As result, it is acceptable that $\boldsymbol{PI}$ calculation in $\boldsymbol{PLL}$ and current controller can be acted every 2 $\boldsymbol{V_{sin}}$ periods in this research.

# 5.7 Chapter Conclusion

This chapter describe the operation and program design of $\boldsymbol{SPWM}$, $\boldsymbol{DTC}$, $\boldsymbol{PLC}$, $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current control in microcontroller $\boldsymbol{STM32F407}$. Section 5.1 describes the basic $\boldsymbol{SPWM}$ system in H-Bridge inverter in microcontroller. Section 5.2 describes how the $\boldsymbol{SPWM}$ signal is updated by $\boldsymbol{DTC}$ and $\boldsymbol{PLC}$ system in microcontroller. Section 5.3 presents $\boldsymbol{ADC}$ sampling system for taking voltage and current data in microcontroller. In section 5.4 and 5.5, the progress of $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current controller with $\boldsymbol{ADC}$ sampling system in microcontroller is introduced and described. These two sections present two different $\boldsymbol{PI}$ calculation methods in $\boldsymbol{PLL}$ and current controller -- position algorithm and velocity algorithm. Velocity algorithm $\boldsymbol{PI}$ calculation solves “bumpless” problem in position algorithm $\boldsymbol{PI}$ system. As result, more stable velocity algorithm $\boldsymbol{PI}$ system is used in $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current control calculations. In section 5.6, the summary of combination of DTC, $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current control system is introduced and described. It is mentioned in section 5.6 that in case all system can not be finished in certain time, this chapter provides a program method that extend the calculation time and maintaining the system stability.

# *Chapter 6*

## *Simulation and Experimental Validation*

This chapter provides simulation and experimental validation for the proposed deadtime and phase lag compensation system. In the first section, the open loop behaviour of the system operating with a resistive load but without ***PLL*** and ***PI*** current controller enabled provides characterisation of the dead time compensation in H-Bridge power inverter. In the second and third section, the output of H-Bridge inverter is connected to grid and ***PLL*** and ***PI*** current controllers are in operation allowing the performance of the compensation scheme to be demonstrated in a close-loop system. In the final section, the simulation result of DTC operation in a 3-level H-Bridge inverter connected to grid with ***PLL*** and ***PI*** current controller is presented.

# 6.1 Dead Time compensation in H-Bridge

This section provides experimental result for the Dead Time Compensation (DTC) (including the ***DTC*** and ***PLC***) and operating with a 2-level H-Bridge inverter connected to a resistor load. The output voltage and current from H-Bridge and their THD when the dead time is equal to $\mathbf{1}\boldsymbol{us}$, $\mathbf{2}\boldsymbol{us}$ and $\mathbf{3}\boldsymbol{us}$ will be shown. After that, the output waveform and THD after adding the DTC system will be provided.

**Figure 6-1** shows the block diagram of open-loop H-Bridge inverter and DTC system,

**Table 6** shows the basic parameter in the H-Bridge inverter.

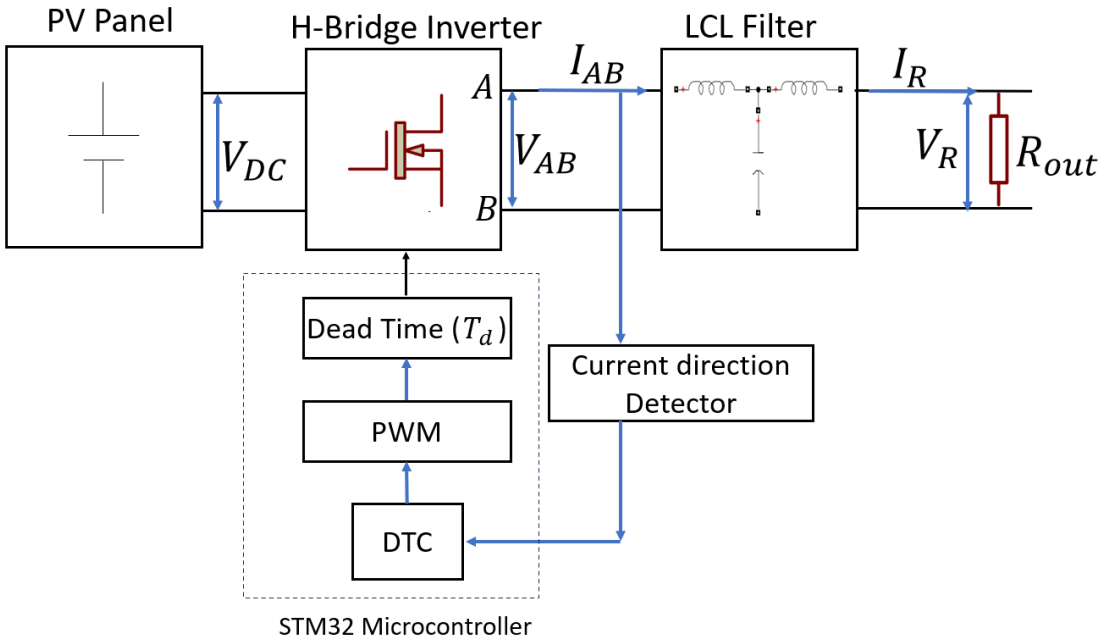


**Figure 6-1: Block diagram of H-Bridge inverter with Dead time compensation in open-circuit.**

**Table 6 : Parameter in H-Bridge inverter circuit and *PWM* system.**

| Parameter | Symbol | Value |
|---|---|---|
| ***DC*** main power supply | $\boldsymbol{V_{DC}}$ | $\boldsymbol{100V}$ |
| Inverter side inductor | $\boldsymbol{L_{inv}}$ | $\boldsymbol{0.9mH}$ |
| Grid side inductor | $\boldsymbol{L_{grid}}$ | $\boldsymbol{0.69mH}$ |
| ***PWM*** frequency | $\boldsymbol{f_{PWM}}$ | $\boldsymbol{20kHz}$ |
| Fundamental frequency | $\boldsymbol{f_{sin}}$ | $\boldsymbol{50Hz}$ |
| Carrier wave peak voltage | $\boldsymbol{\hat{V}_{tri}}$ | $\boldsymbol{1V}$ |
| Modulation wave peak voltage | $\boldsymbol{\hat{V}_{sin}}$ | $\boldsymbol{0.48V}$ |
| Max Modulation index | $\boldsymbol{\hat{m}_i}$ | **0.48** |
| Voltage gain in voltage sensor | $\boldsymbol{G_V}$ | $\boldsymbol{0.016}$ |
| Current gain of current sensor | $\boldsymbol{G_I}$ | $\boldsymbol{0.08}$ |
| Inverter side inductor | $\boldsymbol{L_{inv}}$ | $\boldsymbol{0.9mH}$ |
| Inverter side inductor ESR | $\boldsymbol{R_{inv}}$ | $\boldsymbol{0.15\Omega}$ |
| Grid side inductor | $\boldsymbol{L_{grid}}$ | $\boldsymbol{0.69mH}$ |

| $\boldsymbol{Grid\ side\ inductor\ ESR}$ | $\boldsymbol{R_{grid}}$ | $\boldsymbol{0.15\Omega}$ |
|---|---|---|
| Filter capacitor | $\boldsymbol{C_f}$ | $\boldsymbol{32uF}$ |
| Damping resistor | $\boldsymbol{R_d}$ | $\boldsymbol{0.25\Omega}$ |
| Output resistor | $\boldsymbol{R_{out}}$ | $\boldsymbol{3.75\Omega}$ |
| $\boldsymbol{ARR}$ value | $\boldsymbol{ARR}$ | $\boldsymbol{4200}$ |

The first experiment here is testing the reliability of current and voltage detector, since all calculation regarding $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current controller requires measurements of voltage and current signals.

As described in section 4.4, $\boldsymbol{I_{detect} = 0.08 * I_{actual}}$, and $\boldsymbol{V_{detect} = 0.016 * V_{actual}}$. In this test, the peak modulation index of $\boldsymbol{m_i}$ is equal to $\boldsymbol{0.48}$, $\boldsymbol{PWM}$ frequency $\boldsymbol{f_{pwn} = 20kHz}$, and $\boldsymbol{V_{sin}(t)}$ frequency is $\boldsymbol{f_{sin} = 50Hz}$. **Figure 6-2** shows the voltage on output resistor $\boldsymbol{V_R}$ and the detected voltage from voltage detector $\boldsymbol{V_{detect(R)}}$. The voltage $\boldsymbol{V_R}$ is tested by using an active differential probe, while the $\boldsymbol{V_{detect(R)}}$ is taken by testing the output from voltage detector.

It is clear to see that they have same phase and frequency, but different level of voltage. The peak voltage is shown in **Figure 6-2**, $\boldsymbol{\frac{\hat{V}_{detect(R)}}{\hat{V}_R} = 0.016}$, it proves that the design and operation of voltage detector is correct.

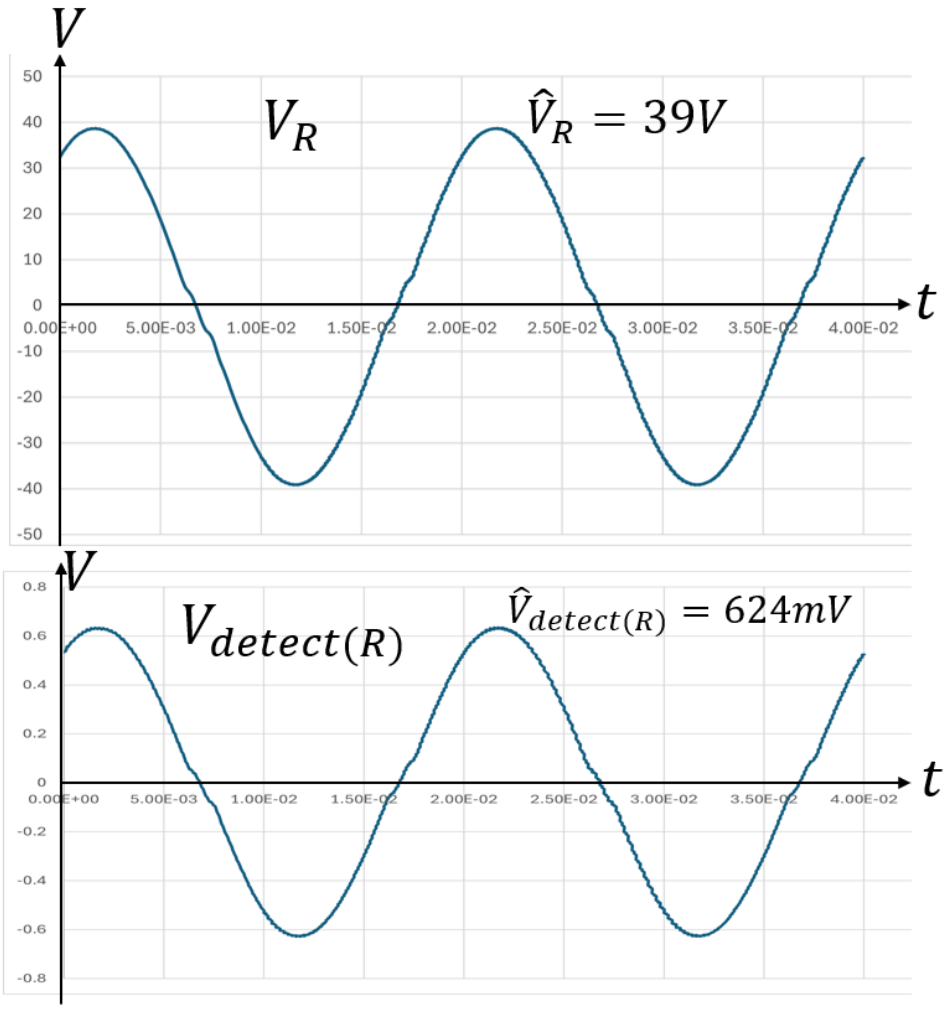


**Figure 6-2: experimental result of $V_R$ and $V_{detect(R)}$.**

**Figure 6-3** shows the output current through the resistor $R_{out}$. The $I_R$ is calculated by a high accuracy current sensor, while $I_{detect(R)}$ is calculated from the current detector circuit described in section 4.4. It is clear to see that their waveform shape, phase and frequency are all same. Comparing the peak current between them, $\frac{\hat{I}_{detect(R)}}{\hat{I}_R} = \mathbf{0.08}$, proving that the design and operation of current sensor is correct.

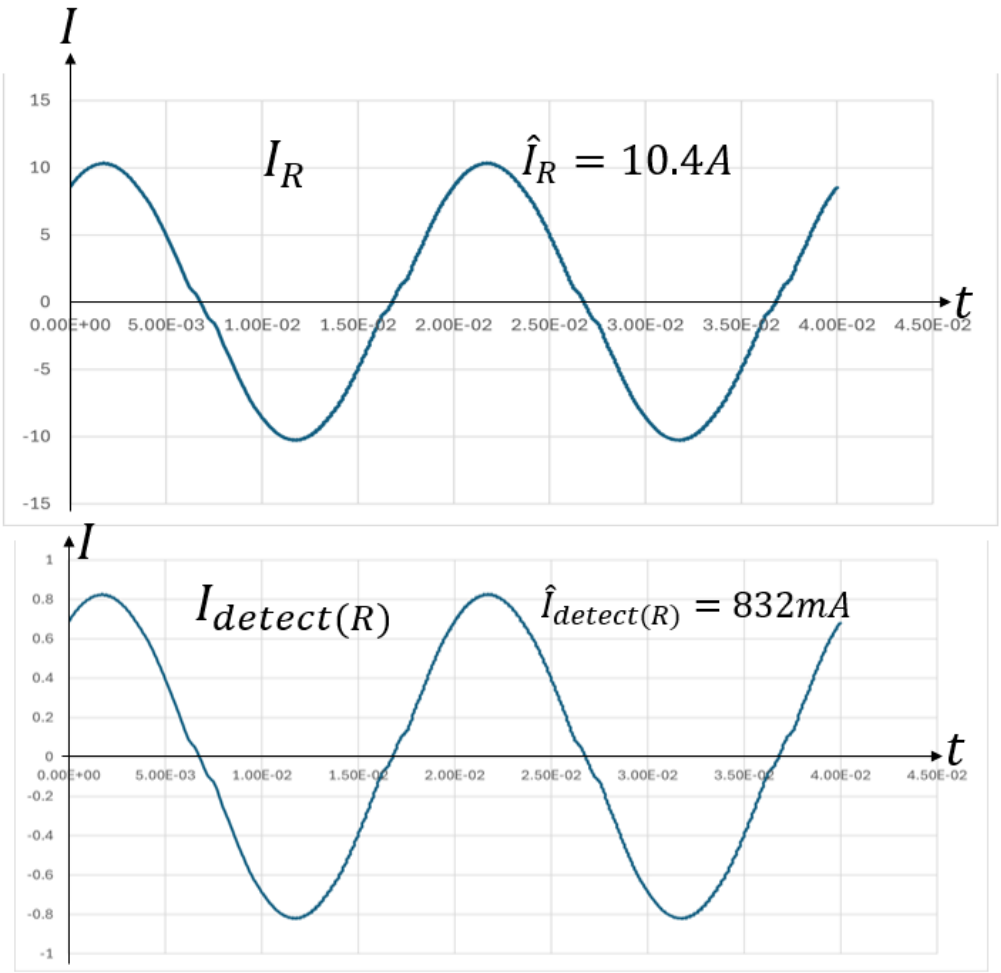


**Figure 6-3: Experiment result of $I_R$ and $I_{detect(R)}$**

In ***DTC*** system, the current polarity of $I_{AB}$ is very important since decides the polarity of deadtime compensation value added into ***PWM*** system. The current polarity detector of $I_{AB}$ is achieved by an MAX913 which is described in section 4.5. The current from detector $I_{detect(AB)}$ represents the detected $I_{AB}$ value, and signal $\overline{V}_Q$ represents the current direction (polarity) of $I_{AB}$.

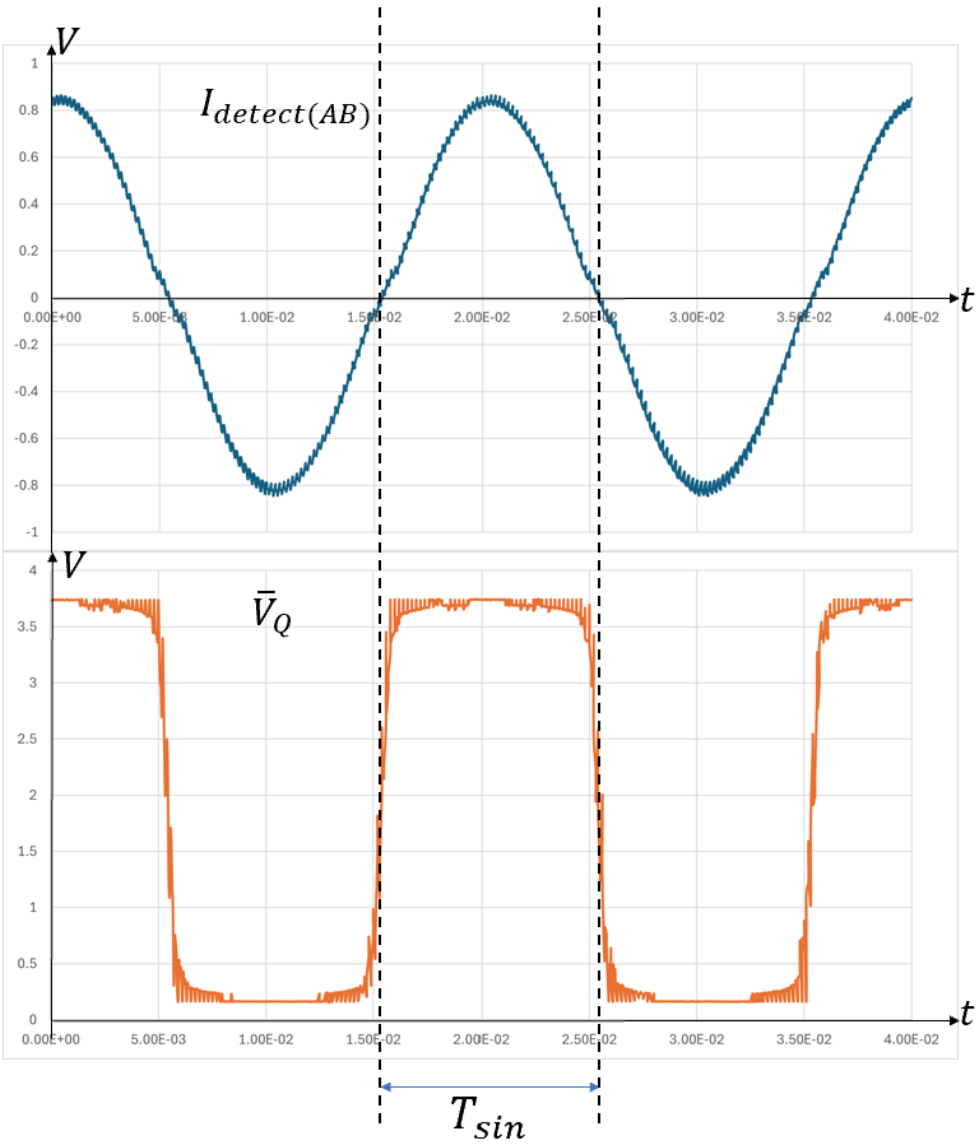


**Figure 6-4: Current waveform $I_{detect(AB)}$ and $\bar{V}_Q$ output from MAX913 in $V_{sin}$ period.**

**Figure 6-4** shows $I_{detect(AB)}$ and $\bar{V}_Q$ during zero-crossing of $I_{detect(AB)}$. As the current approaches a zero, multiple switching events are triggered, and this behaviour is shown in more detail in **Figure 6-5**. After zooming into the zero-crossing time of $I_{detect(AB)}$ and $\bar{V}_Q$, The current ripple is ~0.2 A and as the high-frequency current component crosses zero, multiple switches of $\bar{V}_Q$ occur.

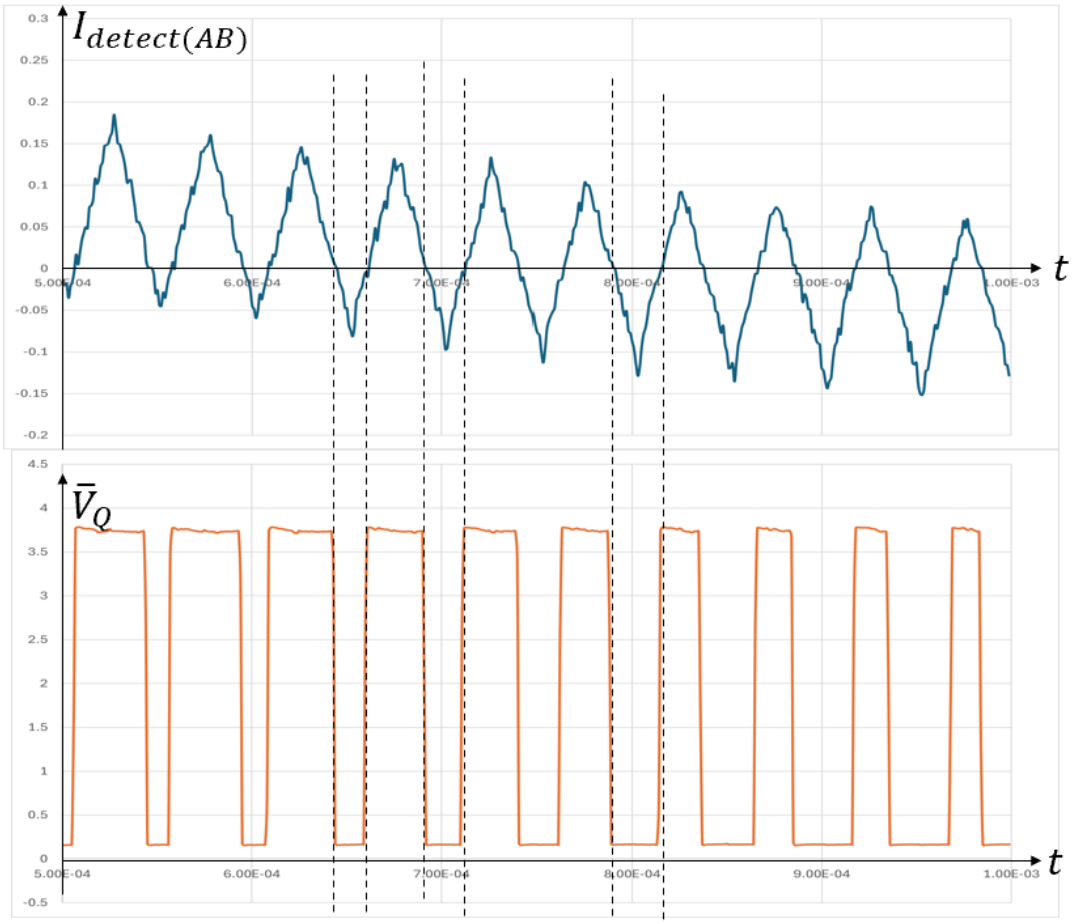


**Figure 6-5: Zoom of $I_{detect(AB)}$ and $\bar{V}_Q$ during zero-crossing.**

As described in section 5.1, the ***PWM*** in microcontroller ***STM32F407*** is achieved dependent on ***CNT***, ***ARR*** and ***CCR*** value, equation (90) shows the transfer equation from $\boldsymbol{V_{sin}(t)}$ to ***CCR*** value in microcontroller.

$$\boldsymbol{CCR = \frac{1}{2} ARR * \left(1 + \frac{V_{sin}(t)}{\hat{V}_{tri}}\right)}$$

According to the parameter in **Table 6**, the modulation signal in the microcontroller is shown in **Figure 6-6**.

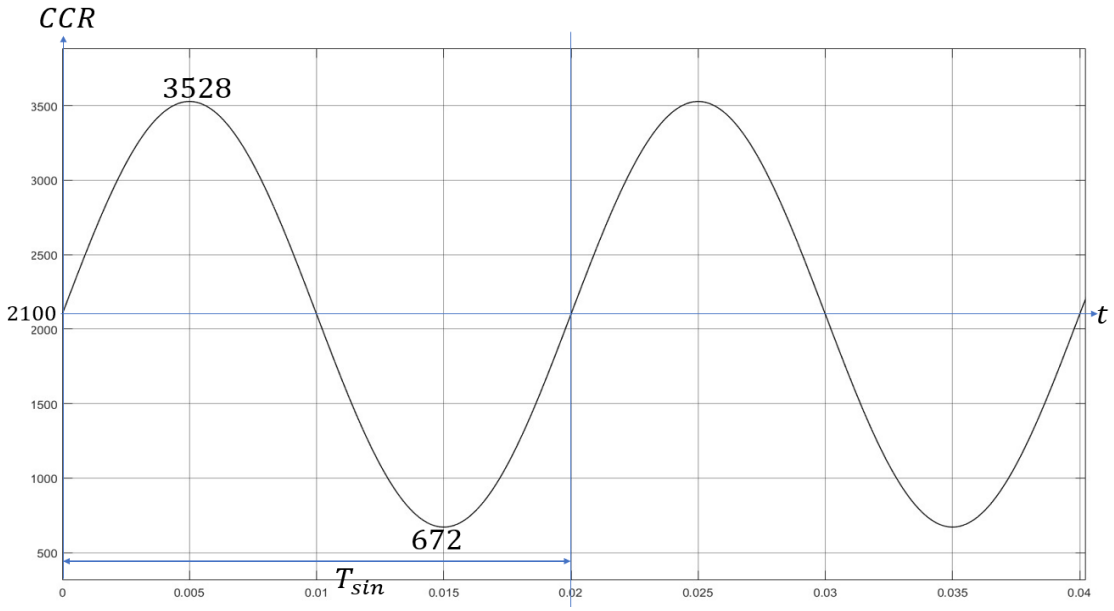


**Figure 6-6: *CCR* value in *VSIN* LUT in *PWM* system in microcontroller.**

The final part of this section shows the response of the system with and without dead time compensation. The load resistor current and voltage with dead time values $\boldsymbol{T_d = 1us, 2us\ and\ 3us}$ is shown.

**Figure 6-7** shows the experimental output voltage on $\boldsymbol{R_{out}}$. When $\boldsymbol{T_d = 1us}$, $\boldsymbol{V_e = 0.08V}$, according to equation (32) and (34), the voltage drop of $\boldsymbol{\widehat{V}_R}$ is equal to $\boldsymbol{V_{DC} * \left[\frac{1}{2} * \frac{V_e}{\widehat{V}_{tri}}\right] = 4V}$. It is clear to see that, after adding the DTC system into ***PWM*** system, the peak voltage $\boldsymbol{\widehat{V}_R}$ is increased by $\boldsymbol{4V}$. In addition, the distortion caused by $\boldsymbol{T_d}$ around zero-crossing is compensated, which decrease the THD from 3.44% to 1.59%.

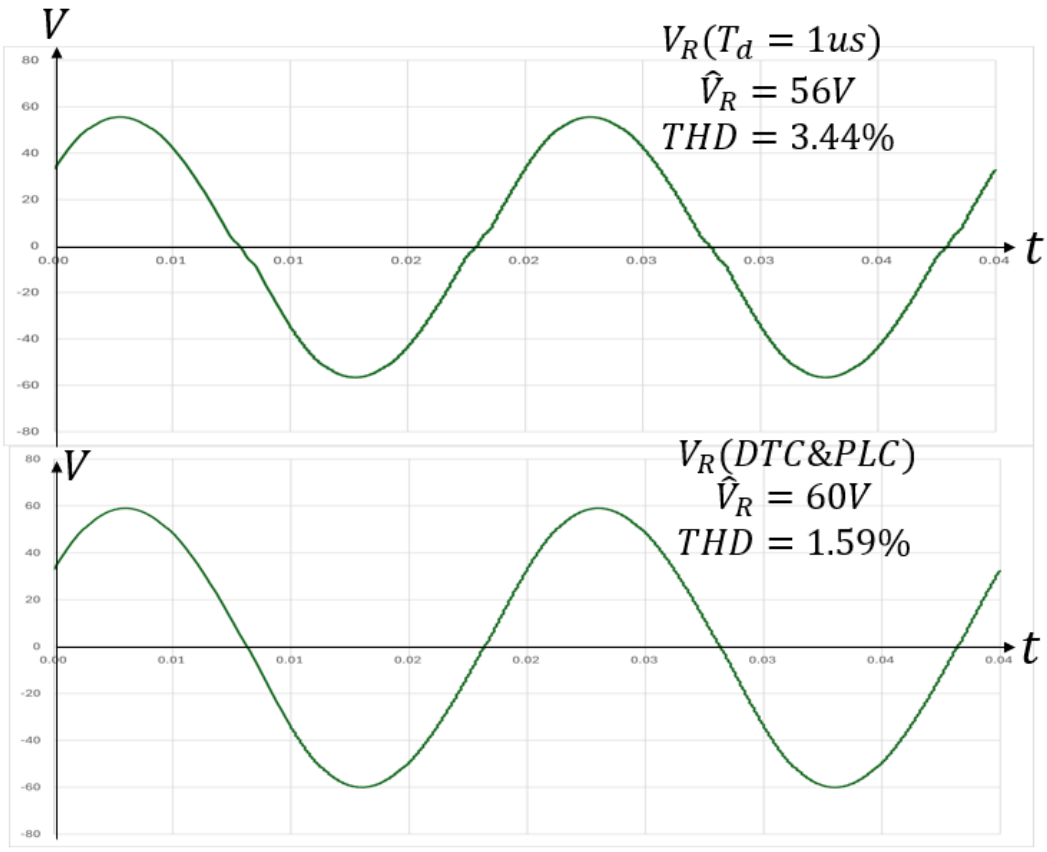


**Figure 6-7: Experiment result of output voltage $V_R$ when $T_d = 1us$ and with $DTC\&PLC$ compensation.**

**Figure 6-8** shows the output current through the $R_{out}$. The current $I_R = \frac{V_R}{R_{out}}$, it is clear to see that with the compensated $4V$ from the dead time effect on $\hat{V}_R$, the peak current $\hat{I}_R$ is increased from $14.9A$ to $16A$. In addition, the distortion caused by $T_d$ around zero-crossing is compensated.

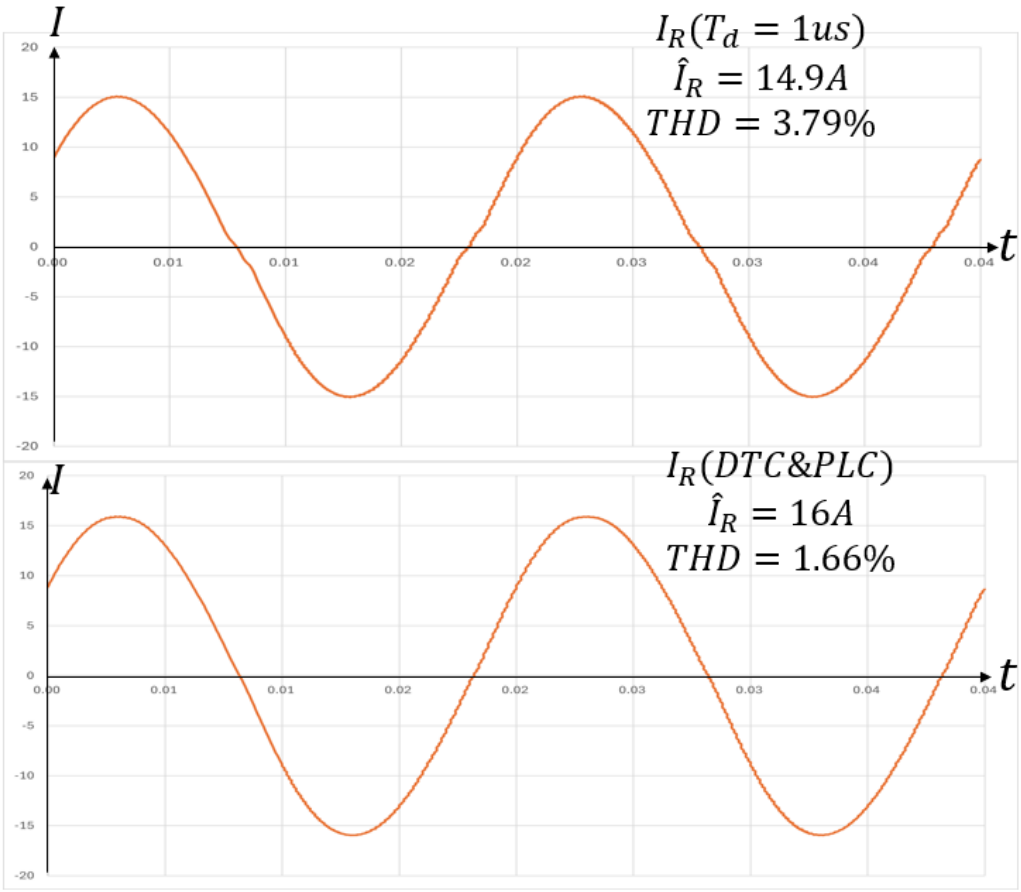


**Figure 6-8: Experiment result of output current $I_R$ when $T_d = 1us$ and with DTC compensation.**

**Figure 6-9** and **Figure 6-10** shows the $I_R$ and $V_R$ when $T_d = 2us$ and $T_d = 3us$, and their condition after adding DTC system.

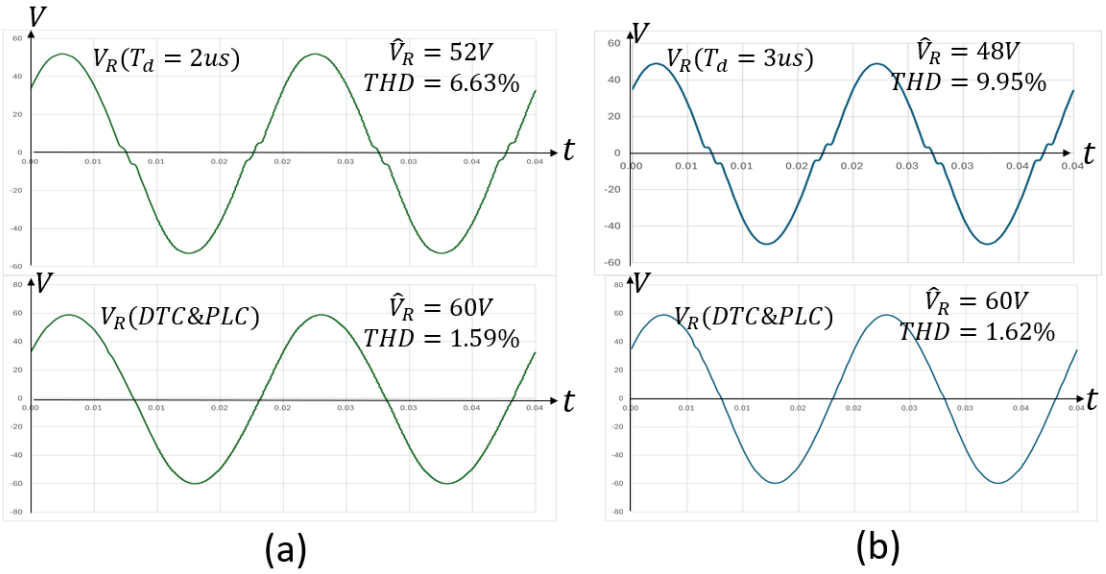


**Figure 6-9 : Experiment result of output voltage $V_R$ (a) $T_d = 2us$, (b) $T_d = 3us$**

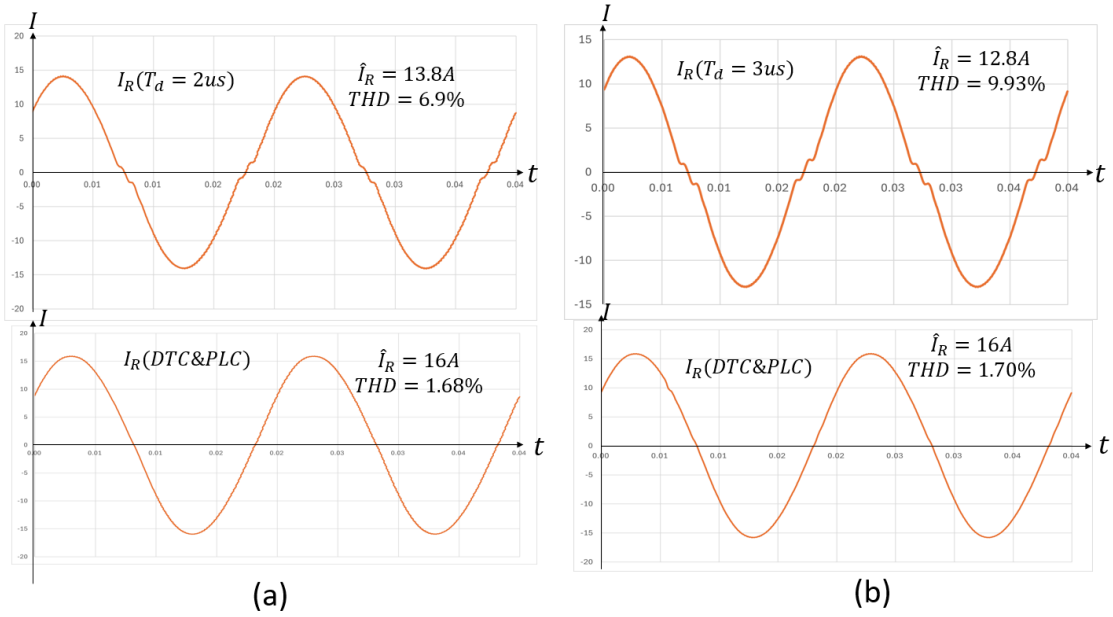


**Figure 6-10: Experiment result of output current $I_R$ (a) $T_d = 2us$, (b) $T_d = 3us$**

It is clear to see that with the increase in $T_d$, voltage drop of peak voltage $\hat{V}_R$ and peak current $\hat{I}_R$ are higher. In addition, the distortion caused by $T_d$ is more pronounced during the zero crossing. After adding ***DTC*** and ***PLC*** system, the voltage and current drop can be compensated when $T_d = 2us$ or $3us$. It should be noticed that the THD in current and voltage is little high after the compensation when $T_d = 3us$. This is

because after adding value $\boldsymbol{V_{DTC}}$ and $\boldsymbol{V_{PLC}}$, when $\boldsymbol{V_{sin}(t)}$ reaches to its peak value $\boldsymbol{\widehat{V}_{sin}}$, the final new modulation signal is equal to $\boldsymbol{\widehat{V}_{sin} + V_{DTC} + V_{PLC}}$. In microcontroller, if the new modulation value is too close to the $\boldsymbol{\widehat{V}_{tri}}$, the calculation and update of $\boldsymbol{CCR}$ value in interrupt system will be short and it may delay the update of $\boldsymbol{CCR}$ value and cause increase of distortion.

In conclusion, this section shows the experimental result of H-Bridge power inverter works under open-loop system. It has shown the effect of dead time effect and the application of compensation to the H-Bridge power inverter. The result shows the output current and voltage on $\boldsymbol{R_{out}}$ under different time of $\boldsymbol{T_d}$. With greater distortion occurring during the zero-crossing. On the other hand, the Dead time Compensation proves that it can compensate the energy loss and distortion caused by $\boldsymbol{T_d}$.

## 6.2 *PLL* and *PI* current close-loop control

In this section, the MATLAB Simulink result is provided for the system operating with $\boldsymbol{PLL}$ and with $\boldsymbol{PI}$ current controller. The output of H-Bridge is connected to Grid which through a transformer which provides both isolation and transformation ratio. The ratio of transformer is 1:5, $\boldsymbol{50V_{rms}}$ to $\boldsymbol{240V_{rms}}$.

**Figure 6-11** shows the block diagram of Grid-connected H-Bridge power inverter system.

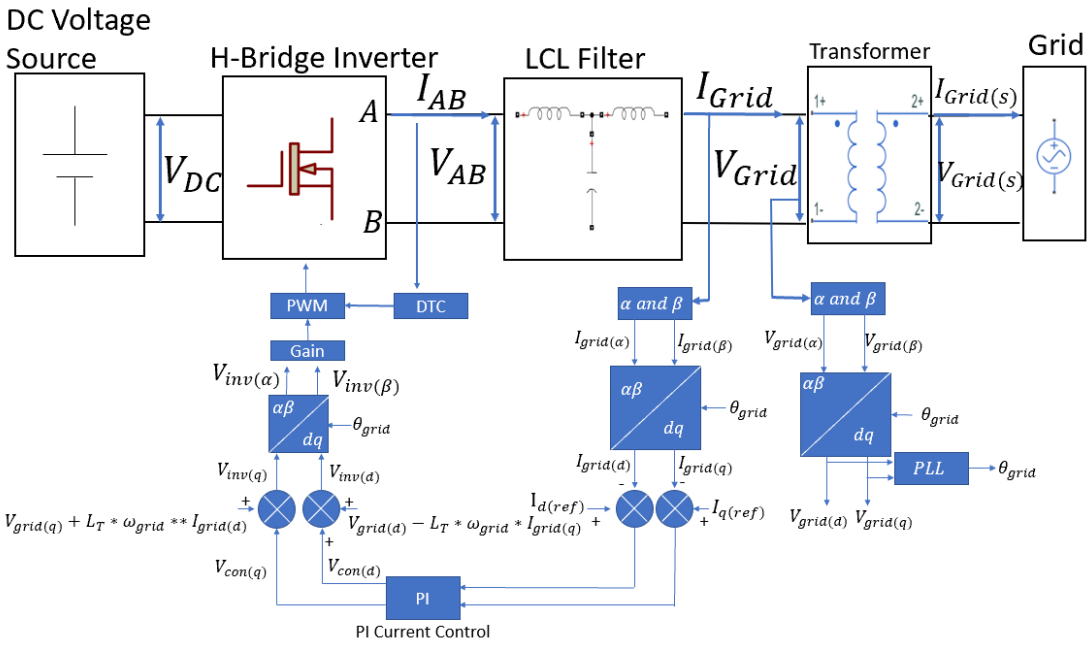


**Figure 6-11: Block diagram of Grid-connected H-Bridge power inverter system.**

**Table 7** gives the parameter used in the grid-connected H-Bridge power inverter system.

**Table 7: parameter in grid-connected H-Bridge power inverter.**

| Parameter | Symbol | Value |
|---|---|---|
| $\boldsymbol{DC}$ Voltage Supply | $\boldsymbol{V_{DC}}$ | $\boldsymbol{100V}$ |
| RMS grid voltage | $\boldsymbol{V_{grid(rms)}}$ | $\boldsymbol{50V_{rms}}$ |
| RMS grid current | $\boldsymbol{I_{grid(rms)}}$ | $\boldsymbol{10A_{rms}}$ |
| Peak grid voltage | $\boldsymbol{\hat{V}_{grid}}$ | $\boldsymbol{70V}$ |
| Peak grid current | $\boldsymbol{\hat{I}_{grid}}$ | $\boldsymbol{14A}$ |
| Sampling time | $\boldsymbol{T_{sample}}$ | $\boldsymbol{50us}$ |
| Reference $\boldsymbol{q}$ axis voltage | $\boldsymbol{V_{q(ref)}}$ | $\boldsymbol{0V}$ |
| Reference $\boldsymbol{d}$ axis current | $\boldsymbol{I_{d(ref)}}$ | $\boldsymbol{14A}$ |
| Reference $\boldsymbol{q}$ axis current | $\boldsymbol{I_{q(ref)}}$ | $\boldsymbol{0A}$ |
| Grid frequency | $\boldsymbol{f_{grid}}$ | $\boldsymbol{50Hz}$ |
| $\boldsymbol{K_P}$ of $\boldsymbol{PLL}$ | $\boldsymbol{K_{P(PLL)}}$ | $\boldsymbol{6.34}$ |
| $\boldsymbol{K_i}$ of $\boldsymbol{PLL}$ | $\boldsymbol{K_{i(PLL)}}$ | $\boldsymbol{1350}$ |
| $\boldsymbol{K_P}$ in current control | $\boldsymbol{K_{P(PI)}}$ | $\boldsymbol{0.406}$ |
| $\boldsymbol{K_i}$ in current control | $\boldsymbol{K_{i(PI)}}$ | $\boldsymbol{130}$ |
| Rated Power | $\boldsymbol{S}$ | $\boldsymbol{500VA}$ |
| Gain | $\boldsymbol{G_{PWM}}$ | 21 |

The value of $K_p$ and $K_i$ in ***PLL*** and ***PI*** current controller can be calculated through equation (68), (69), (83) and (84). During the experiment, it was found that integral controller $K_i$ for both ***PLL*** and ***PI*** current controller had to be reduced to stabilise operation.

The ***PLL*** is used to synchronise the inverter output to grid and in this process, it provides the grid angle and grid frequency. The key for $\theta_{grid}$ calculation in ***PLL*** is keeping $q$-axis grid voltage $V_{grid(q)}$ to 0 using the $q$-axis ***PI*** compensator. **Figure 6-12** shows the $dq$ ***axis*** voltage in $V_{grid}$ in MATLAB simulation.

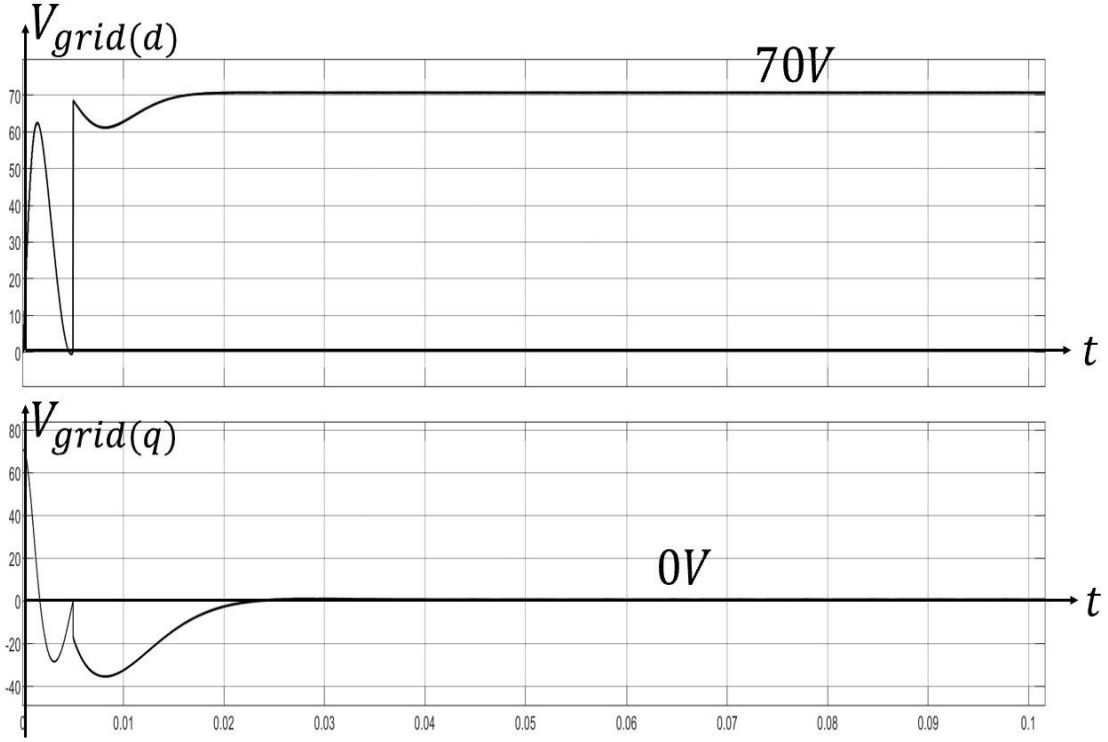


**Figure 6-12: MATLAB simulation result of $V_{grid(d)}$ and $V_{grid(q)}$.**

The ***PLL*** system is fully synchronized with $V_{grid}$ after a full grid period ($t > 0.02s$), after that $V_{grid(q)}$ is kept at $0V$, $V_{grid(d)}$ represents the peak voltage $\widehat{V}_{grid}$ which is

equal to $\mathbf{70}\boldsymbol{V}$. **Figure 6-13** shows the relation between grid voltage $\boldsymbol{V_{grid}}$ and calculated grid angle $\boldsymbol{\theta_{grid}}$.

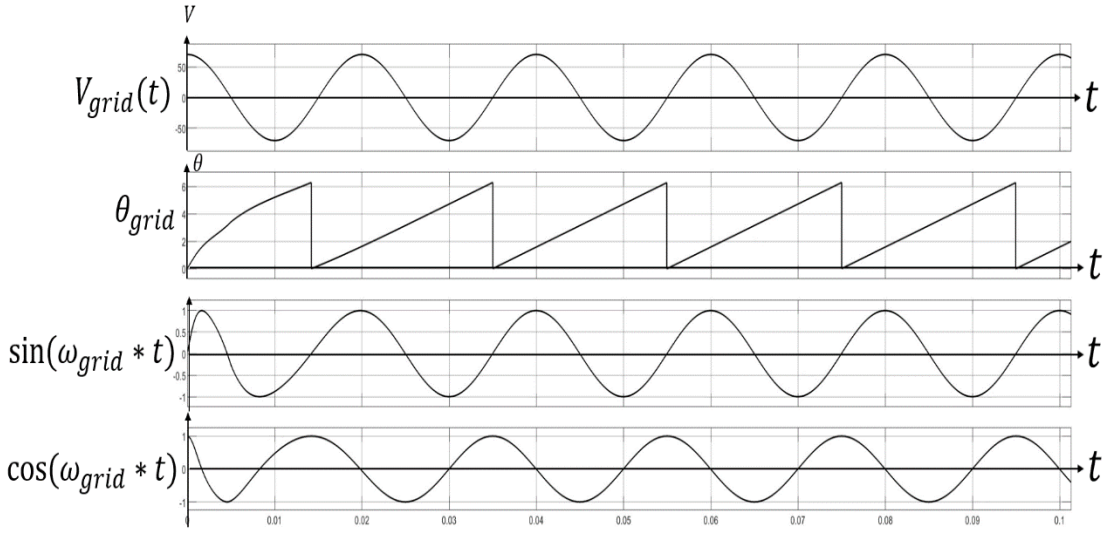


**Figure 6-13: The relation between grid voltage $\boldsymbol{V_{grid}(t)}$ and calculated grid angle $\boldsymbol{\theta_{grid}}$ in MATLAB simulation.**

As shown in **Figure 6-12**, the initial value of $\boldsymbol{V_{grid(q)}}$ is far from the 0, which produce larger $\boldsymbol{\omega}$ in order to chase the angle of $\boldsymbol{V_{grid}(t)}$. Then, as the controller acts to drive $\boldsymbol{V_{grid(q)}}$ towards 0, the calculated frequency $\boldsymbol{\omega}$ is forced towards $\boldsymbol{\omega_{grid}}$ and the $\boldsymbol{\theta_{grid}}$ eventually equals to angle of $\boldsymbol{V_{grid}(t)}$. As shown in **Figure 6-13**, a $\boldsymbol{sin}$ and $\boldsymbol{cos}$ waveform are produced by using the $\boldsymbol{\theta_{grid}}$ from $\boldsymbol{PLL}$, and the $\boldsymbol{sin}$ waveform is in phase with $\boldsymbol{V_{grid}}$. It proves that the $\boldsymbol{PLL}$ is synchronized with a $\boldsymbol{sin}$ waveform $\boldsymbol{V_{grid}(t)}$.

After $\boldsymbol{\theta_{grid}}$ is calculated from the $\boldsymbol{PLL}$, it can be used in the current control, which allows current to be injected at the correct phase and frequency. The key for $\boldsymbol{PI}$ current

control is keeping the $\boldsymbol{dq}$ axis current $\boldsymbol{I_{grid(d)}}$ and $\boldsymbol{I_{grid(q)}}$ at their reference values to provide the desired active power $\boldsymbol{P}$ and reactive power $\boldsymbol{Q}$. The $\boldsymbol{I_{ref(d)}}$ is set as $\boldsymbol{14A}$, while $\boldsymbol{I_{ref(q)}}$ is set as $\boldsymbol{0A}$, which the total rated power is equal to the active power $\boldsymbol{P}$ in system.

Before continuing $\boldsymbol{PI}$ current controller in this section, the initial system of whole H-Bridge system from $\boldsymbol{t = 0}$ should be described. At the beginning, $\boldsymbol{PLL}$ controller is operated firstly. An initial modulation reference signal $\boldsymbol{V_{sin}}$ is created according to the grid angle calculated from $\boldsymbol{PLL}$. With the initial modulation reference signal, the output grid current is synchronized to grid voltage. Then $\boldsymbol{PI}$ current controller is operated with $\boldsymbol{PLL}$, updating $\boldsymbol{V_{sin}}$ every $\boldsymbol{V_{sin}}$ period. Ensuring output grid current $\boldsymbol{I_{grid}}$ is still synchronized with grid voltage $\boldsymbol{V_{grid}}$, and maintaining the peak grid current $\boldsymbol{\hat{I}_{grid}}$ to its reference value.

Referring to **Figure 6-14**, the initial system is described.

The starts time ($\boldsymbol{t = 0}$) acts at the zero-crossing of $\boldsymbol{V_{grid}(t)}$ from negative to positive. At this time, only voltage detector is operated to take grid voltage data for $\boldsymbol{PLL}$ calculation. $\boldsymbol{PLL}$ calculation is finished in this period, and the initial modulation reference signal $\boldsymbol{V_{sin}}$ is created.

At time $\boldsymbol{t = T_{sin}}$, the initial $\boldsymbol{V_{sin}}$ starts to be used to drive $\boldsymbol{PWM}$ signal controlling switches in H-Bridge. As result, output current $\boldsymbol{I_{grid}(t)}$ is produced. At the same time, current detector is operated to get grid current data for preparing $\boldsymbol{PI}$ current control calculation. As shown in **Figure 6-14**, from $\boldsymbol{T_{sin}}$ to $\boldsymbol{2T_{sin}}$with $\boldsymbol{PLL}$ system, the grid

current is synchronized with grid voltage. The initial peak modulation index is set as $\mathbf{0.75}$. Thus, peak current $\hat{\boldsymbol{I}}_{\boldsymbol{peak}} = \mathbf{11}\boldsymbol{A}$.

At $\boldsymbol{t} = \mathbf{3}\boldsymbol{T}_{\boldsymbol{sin}}$, $\boldsymbol{PI}$ current calculation is operated. A new modulation reference signal $\boldsymbol{V}_{\boldsymbol{sin}}$ is created by $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current calculation together from $\mathbf{3}\boldsymbol{T}_{\boldsymbol{sin}}$ to $\mathbf{4}\boldsymbol{T}_{\boldsymbol{sin}}$.

But until $\boldsymbol{t} = \mathbf{4}\boldsymbol{T}_{\boldsymbol{sin}}$, $\boldsymbol{V}_{\boldsymbol{sin}}$ is updated.

After $\mathbf{4}\boldsymbol{T}_{\boldsymbol{sin}}$, $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current controller keeps working together to update modulation signal. $\boldsymbol{I}_{\boldsymbol{grid}}$ keeps synchronizing to $\boldsymbol{V}_{\boldsymbol{grid}}$ and its peak value $\hat{\boldsymbol{I}}_{\boldsymbol{grid}}$ reaches to $\mathbf{14}\boldsymbol{A}$ ($\boldsymbol{I}_{\boldsymbol{ref}}$) after steady-state conditions.

Because all voltage and current data at start time of system ($\boldsymbol{t} = \mathbf{0}$) are $\mathbf{0}$, an extra $\boldsymbol{V}_{\boldsymbol{sin}}$ period is required for both $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current controller to get a basic initial value ($\boldsymbol{V}_{\boldsymbol{grid(d,q)}}$ & $\boldsymbol{I}_{\boldsymbol{grid(d,q)}}$) to do the calculations.

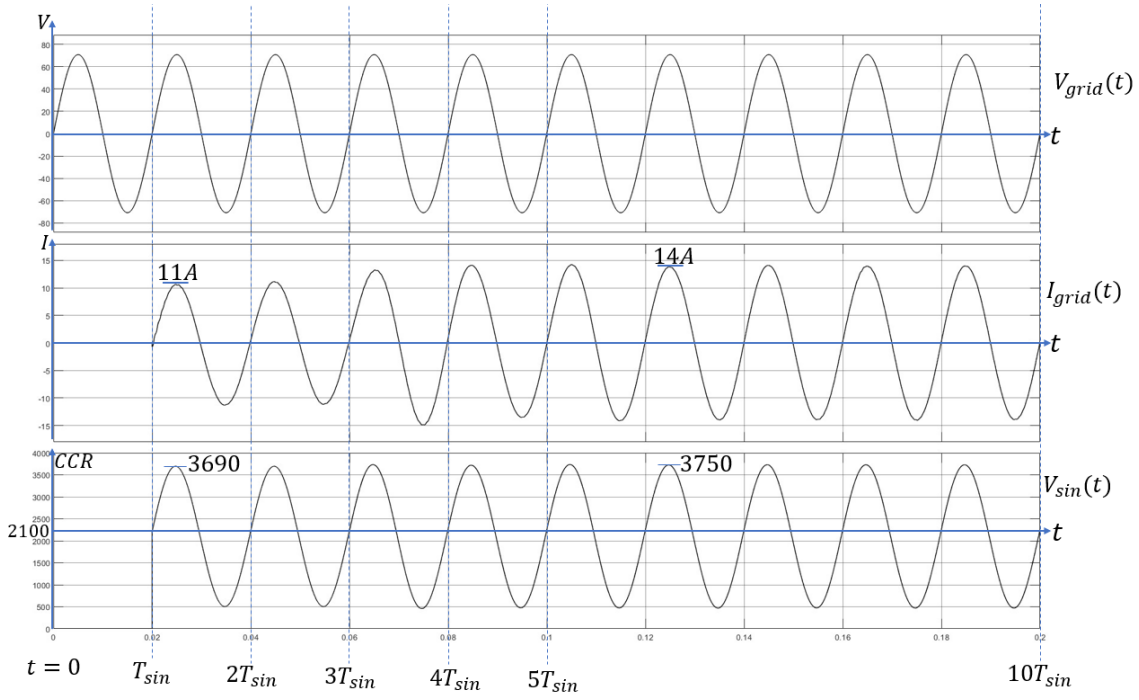


**Figure 6-14: Simulation of $\boldsymbol{V}_{\boldsymbol{grid}}(\boldsymbol{t})$, $\boldsymbol{I}_{\boldsymbol{grid}}(\boldsymbol{t})$ and $\boldsymbol{V}_{\boldsymbol{sin}}(\boldsymbol{t})$ during initial system.**

**Figure 6-15** shows $\boldsymbol{I}_{\boldsymbol{grid(d)}}$ and $\boldsymbol{I}_{\boldsymbol{grid(q)}}$ from grid current $\boldsymbol{I}_{\boldsymbol{grid}}(\boldsymbol{t})$.

Referring to **Figure 6-15**, $\boldsymbol{I_{grid(d)}}$ and $\boldsymbol{I_{grid(q)}}$ are calculated after $\boldsymbol{t = T_{sin}}$, and $\boldsymbol{I_{grid(d)}}$ represents the peak current $\boldsymbol{\hat{I}_{grid}}$ when $\boldsymbol{I_{grid(q)} = 0}$. From $\boldsymbol{T_{sin}}$ to $\boldsymbol{3T_{sin}}$, $\boldsymbol{I_{grid(d)} = 11A}$ and $\boldsymbol{I_{grid(q)} = 0.08A}$. So, the peak current $\boldsymbol{\hat{I}_{grid} = 11A}$ during this time. Therefore, demonstrating the convergence of $\boldsymbol{I_{grid(d)}}$ and $\boldsymbol{I_{grid(q)}}$ controller. After $\boldsymbol{t = 3T_{sin}}$, ***PLL*** and ***PI*** current controller work together, $\boldsymbol{I_{grid(d)}}$ start to chase the $\boldsymbol{I_{d(ref)} = 14A}$, while $\boldsymbol{I_{grid(q)}}$ starts to chase the $\boldsymbol{I_{q(ref)} = 0A}$. After $\boldsymbol{t = 6T_{sin}}$, ***PI*** current controller works under steady-state condition.

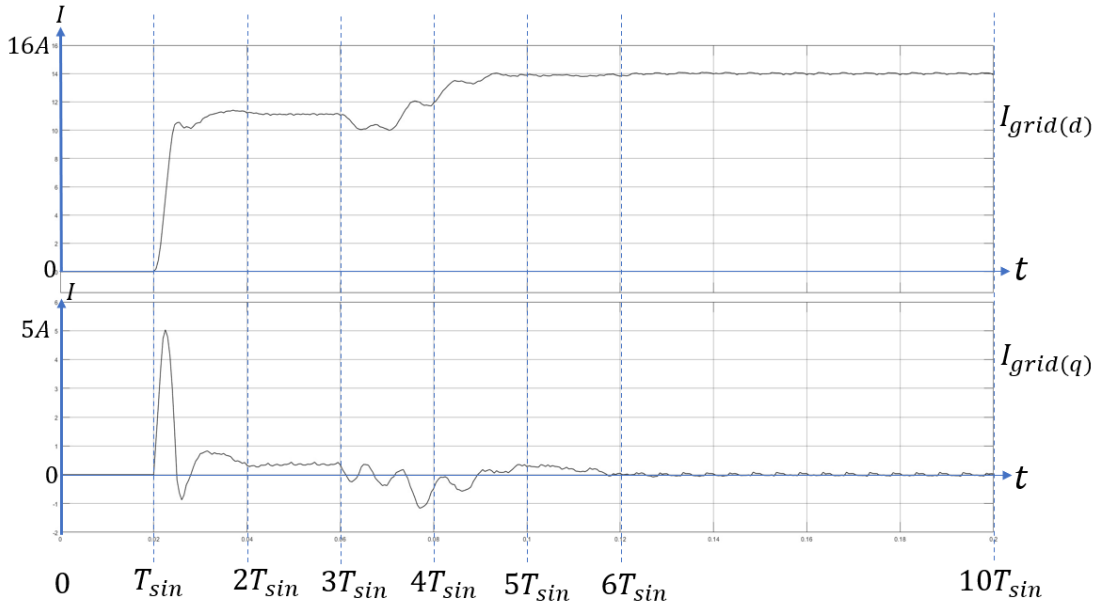


**Figure 6-15: Simulation result of $\boldsymbol{dq}$ axis current of $\boldsymbol{I_{grid}(t)}$, $\boldsymbol{I_{grid(d)}}$ and $\boldsymbol{I_{grid(q)}}$.**

**Figure 6-16** shows $\boldsymbol{V_{inv(d)}}$ and $\boldsymbol{V_{inv(q)}}$ which can be used to represent the $\boldsymbol{dq}$ axis voltage of the fundamental inverter voltage $\boldsymbol{V_{inv}}$ in the output voltage from H-Bridge inverter $\boldsymbol{V_{AB}(t)}$. Because ***PI*** current control calculation is started after $\boldsymbol{2T_{sin}}$, $\boldsymbol{V_{inv(d)}}$ and $\boldsymbol{V_{inv(q)}}$ are calculated after $\boldsymbol{2T_{sin}}$.

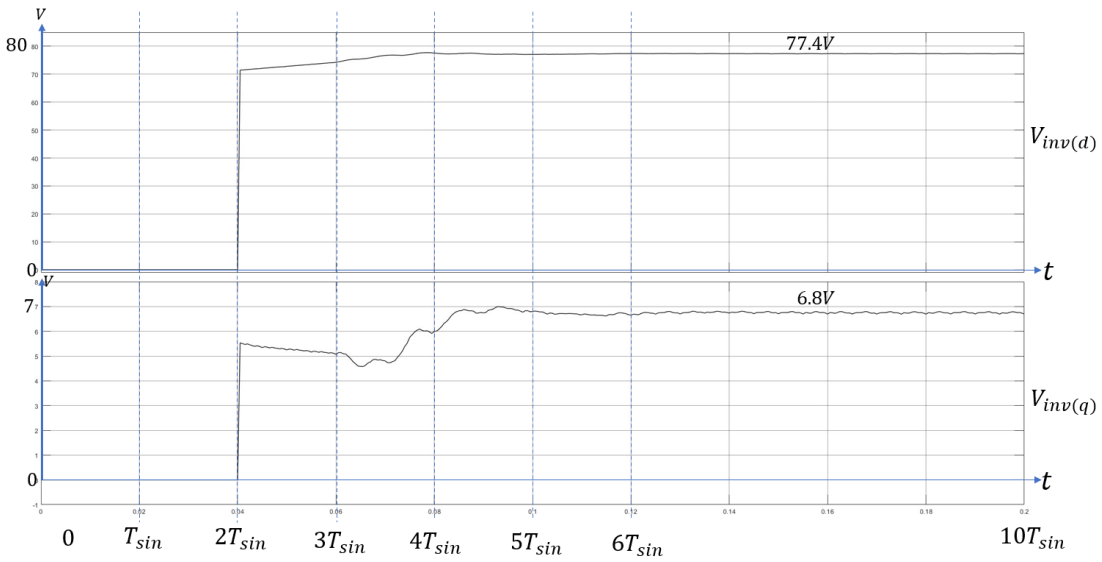


**Figure 6-16 : Simulation result of inverter side fundamental $dq$-axis voltage.**

After calculations, $\boldsymbol{V_{inv(d)}}$ and $\boldsymbol{V_{inv(q)}}$ are transformed to $\boldsymbol{V_{inv(\alpha)}}$ and $\boldsymbol{V_{inv(\beta)}}$. Where $\boldsymbol{V_{inv(\alpha)}}$ is equal to the fundamental signal $\boldsymbol{V_{inv}}$ as shown in **Figure 6-17**.

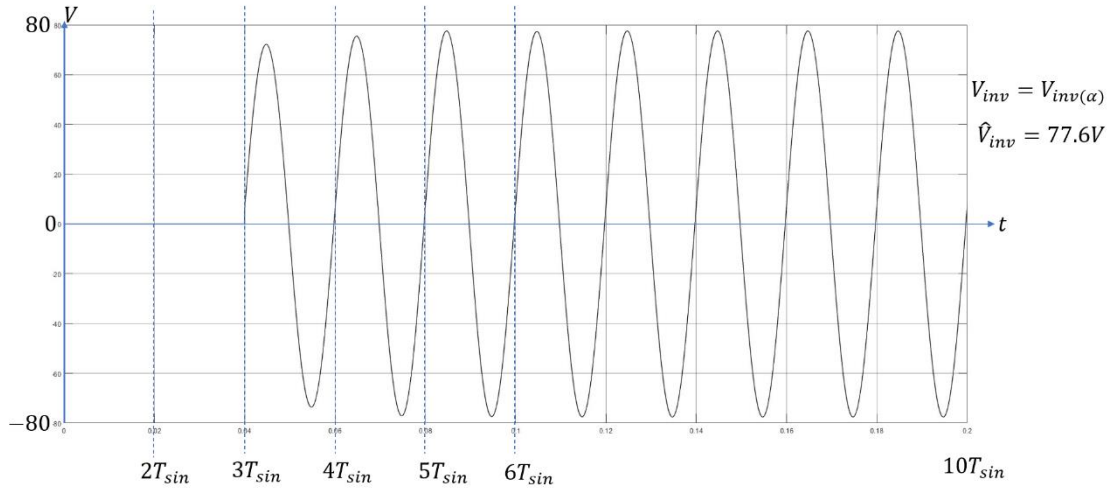


**Figure 6-17: Simulation result of fundamental inverter side voltage $\boldsymbol{V_{inv}(t)}$.**

The final step is producing $\boldsymbol{CCR}$ value into $\boldsymbol{VSIN}$ LUT according to the $\boldsymbol{V_{inv}}$ from $\boldsymbol{PI}$ current calculation. As described before, $\boldsymbol{CCR}$ can be calculated as,

$$\boldsymbol{CCR = \frac{ARR}{2} + \frac{1}{2} * \frac{ARR}{V_{DC}} * V_{inv}}$$

The modulation signal in microcontroller is shown in **Figure 6-18**.

In microcontroller, the midpoint of $\boldsymbol{V_{sin}}$ is equal to $\frac{\boldsymbol{ARR}}{\boldsymbol{2}} = \boldsymbol{2100}$.

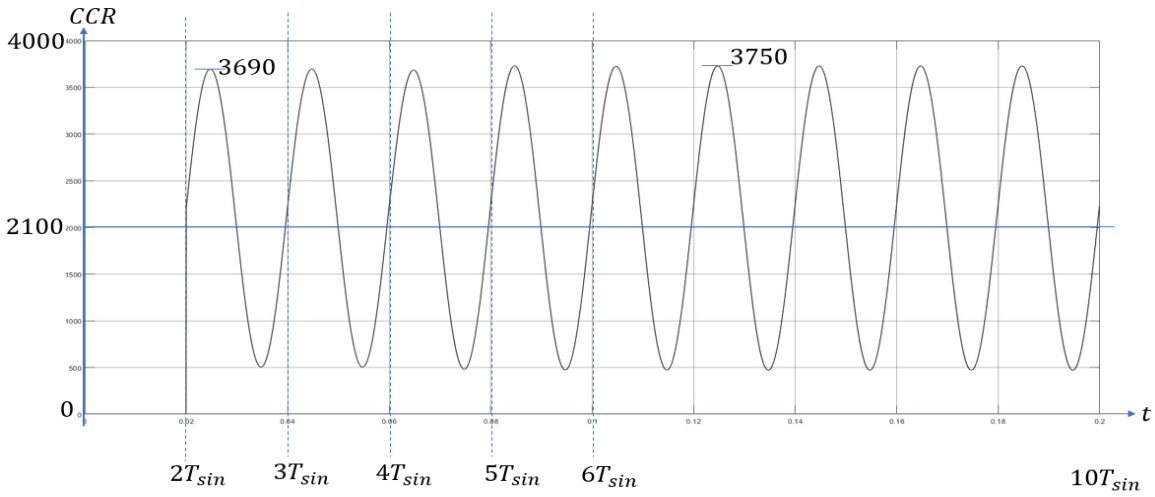


**Figure 6-18: Modulation signal $\boldsymbol{V_{sin}(t)}$ in microcontroller produced from the *PI* current control.**

**Figure 6-19** shows the output waveform of grid current, voltage and fundamental voltage from H-Bridge inverter after ***PLL*** and ***PI*** current controller works under steady-state condition.

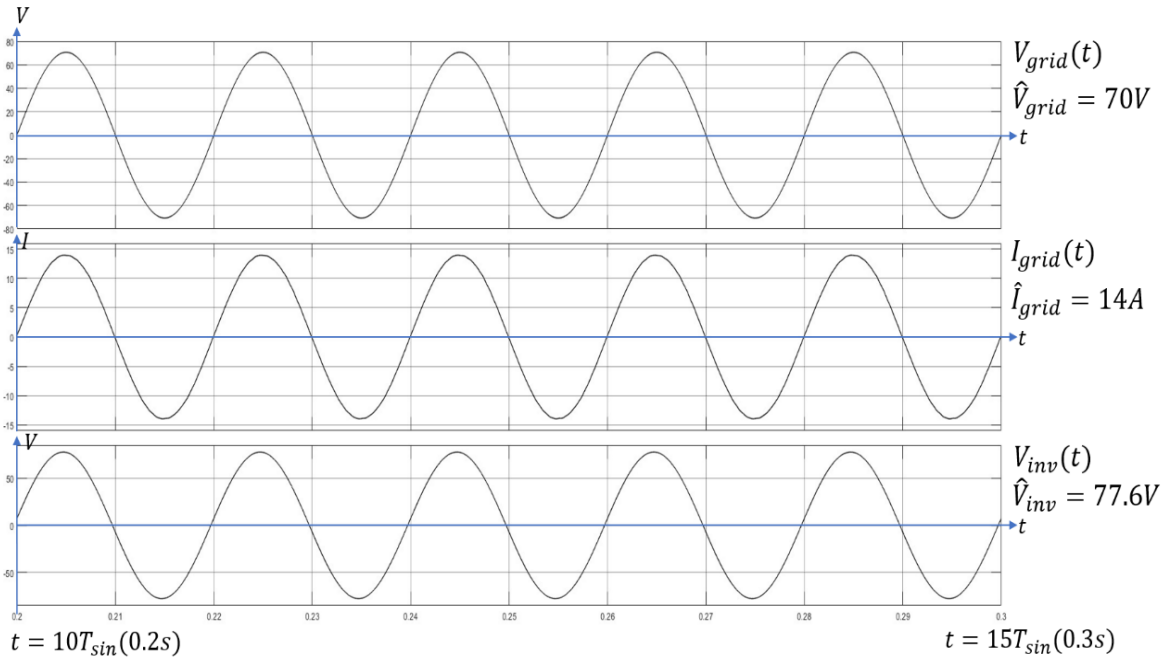


**Figure 6-19: Simulation result of output waveform from grid connected H-Bridge power inverter.**

After $\mathbf{0.2}\boldsymbol{s}$ $(\mathbf{10}\boldsymbol{T_{sin}})$, the system has reached to steady-state condition. It is clear to see that the output voltage and current are at same phase and frequency $(\mathbf{50}\boldsymbol{Hz})$, which proves that $\boldsymbol{PLL}$ system works correctly. In addition, the peak current $\hat{\boldsymbol{I}}_{\boldsymbol{grid}}$ can be kept at $\mathbf{14}\boldsymbol{A}$ which is equal to the reference current $\boldsymbol{I}_{\boldsymbol{ref(d)}}$ set in the current control.

This section has shown the operation of $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current controller in an ideal 2-level H-Bridge inverter $(\boldsymbol{T_d} = \mathbf{0})$ through MATLAB simulation. The current is in same phase and frequency with grid voltage. The peak current is same to the reference peak current set in the current controller.

## 6.3 Dead Time Effect and Dead Time Compensation operation with grid $PLL$ and $PI$ current control.

In this section, through analysing simulation and experiment result, the dead time effect and dead time compensation operation with $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current controller is introduced and discussed.

Firstly, **Figure 6-20** shows the simulation result of $\boldsymbol{V_{grid}(t)}$ and $\boldsymbol{I_{grid}(t)}$ during the initial time with $\boldsymbol{T_d = 1us}$. And **Figure 6-21** shows the simulation of $\boldsymbol{dq}$-axis current from $\boldsymbol{I_{grid}(t)}$ with $\boldsymbol{T_d = 1us}$.

The initial work of H-Bridge system is same as described in the previous section when $\boldsymbol{T_d = 0}$.

From $\boldsymbol{2T_{sin}}$ to $\boldsymbol{4T_{sin}}$, only $\boldsymbol{PLL}$ system works, it is clear to see that the peak current $\boldsymbol{\hat{I}_{grid}}$ during this time is decreased from $\boldsymbol{11A}$ to $\boldsymbol{5A}$ caused by dead time effect. After $\boldsymbol{t = 4T_{sin}}$, $\boldsymbol{PI}$ current controller starts to work, which forces $\boldsymbol{dq}$-axis current to their reference value. As shown in **Figure 6-19** and **Figure 6-24**, at the start of $\boldsymbol{PI}$ current control, since the $\boldsymbol{5A}$ is much lower than the reference current $\boldsymbol{14A}$, if the $\boldsymbol{5A}$ is increased to $\boldsymbol{14A}$ in short time by $\boldsymbol{PI}$ current controller, an overshoot may occur. A high current peak reaches to $\boldsymbol{25A}$ is caused because of dead time effect. In addition, the fluctuation of $\boldsymbol{dq}$-axis current during the steady-state condition is larger. Finally, although the peak current is reduced because of dead time effect, $\boldsymbol{PI}$ current controller can ensure the $\boldsymbol{\hat{I}_{grid}}$ can reach to its reference peak value ($\boldsymbol{14A}$). But the distortion caused by dead time effect during zero-crossing can not be removed.

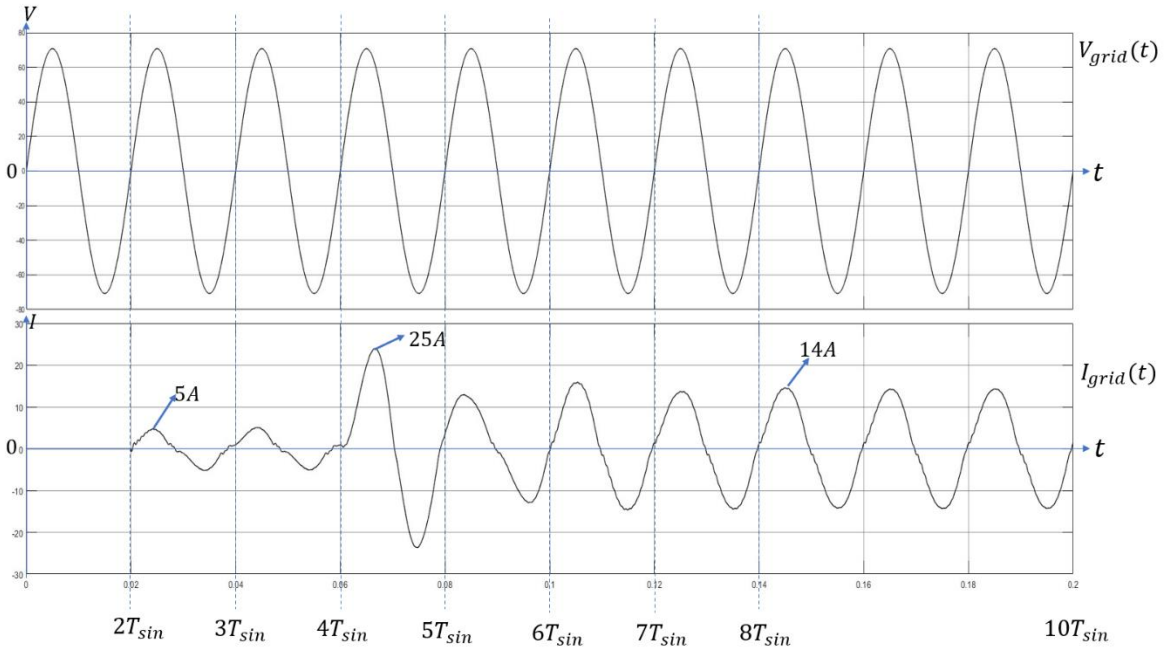


**Figure 6-20: Simulation result of $V_{grid}(t)$ and $I_{grid}(t)$ during initial time with $T_d = 1us$.**

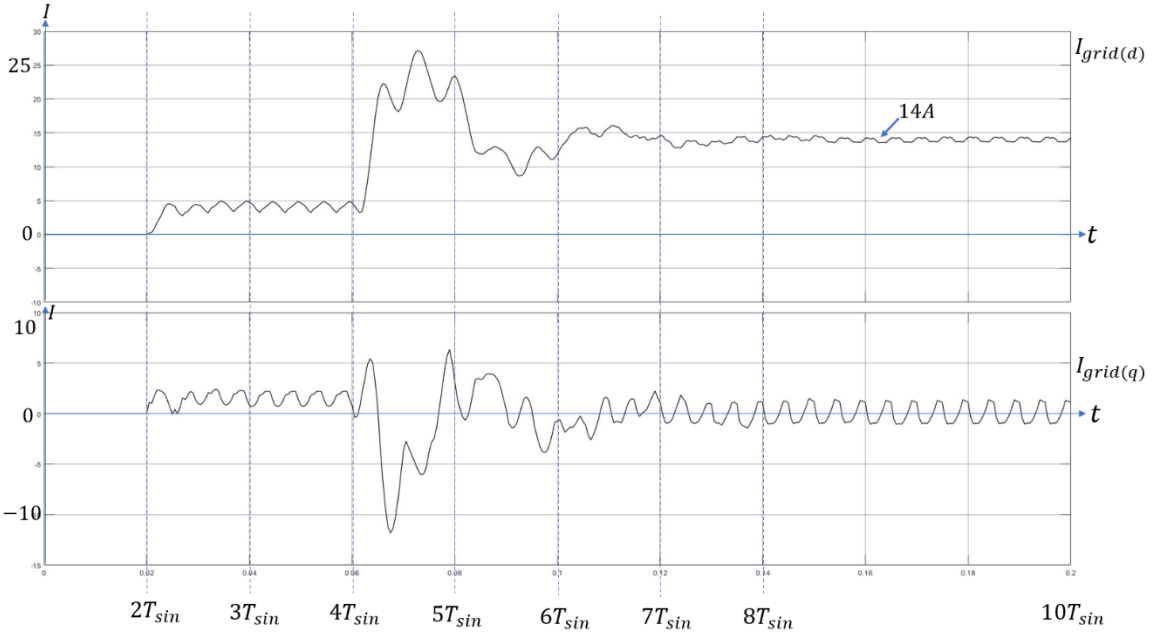


**Figure 6-21: Simulation result of $dq$-axis current with $T_d = 1us$**

**Figure 6-22** shows the $V_{grid}(t)$ and $I_{grid}(t)$ during the initial time after ***DTC*** system is operated. After the start-up transient, the current polarity detector for $I_{AB}$ is turns on

at $\boldsymbol{t = T_{sin}}$ for DTC system calculation. Then DTC is activated at $\boldsymbol{t = 2T_{sin}}$. As shown in **Figure 6-22**, the peak current $\boldsymbol{\hat{I}_{grid}}$ is increased to $\boldsymbol{11A}$ by operation of DTC system. As result, after $\boldsymbol{PI}$ current controller is activated at $\boldsymbol{t = 3T_{sin}}$, the small current error between $\boldsymbol{11A}$ and $\boldsymbol{14A}$ can not cause overshoot. In addition, the distortion caused by dead time during zero-crossing is compensated by DTC system shown in **Figure 6-22**.

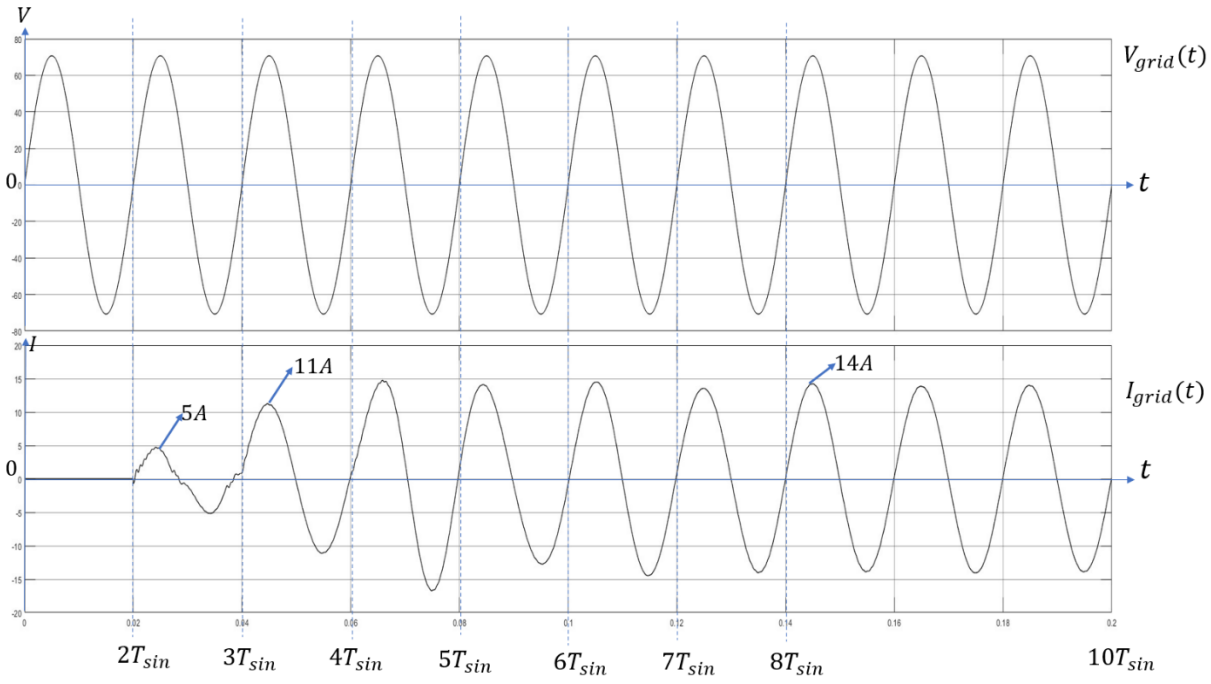


**Figure 6-22: Simulation result of $\boldsymbol{V_{grid}(t)}$ and $\boldsymbol{I_{grid}(t)}$ during the initial time with $\boldsymbol{DTC}$ system.**

Observing $\boldsymbol{dq}$-axis current of $\boldsymbol{I_{grid}}$ with DTC system in **Figure 6-23**, from $\boldsymbol{2T_{sin}}$ to $\boldsymbol{3T_{sin}}$, $\boldsymbol{I_{grid(d)}}$ is increased from $\boldsymbol{5A}$ to $\boldsymbol{11A}$ with the operation of DTC system. After $\boldsymbol{PI}$ current controller works under steady-state condition, the fluctuation of $\boldsymbol{I_{grid(d,q)}}$ is smaller.

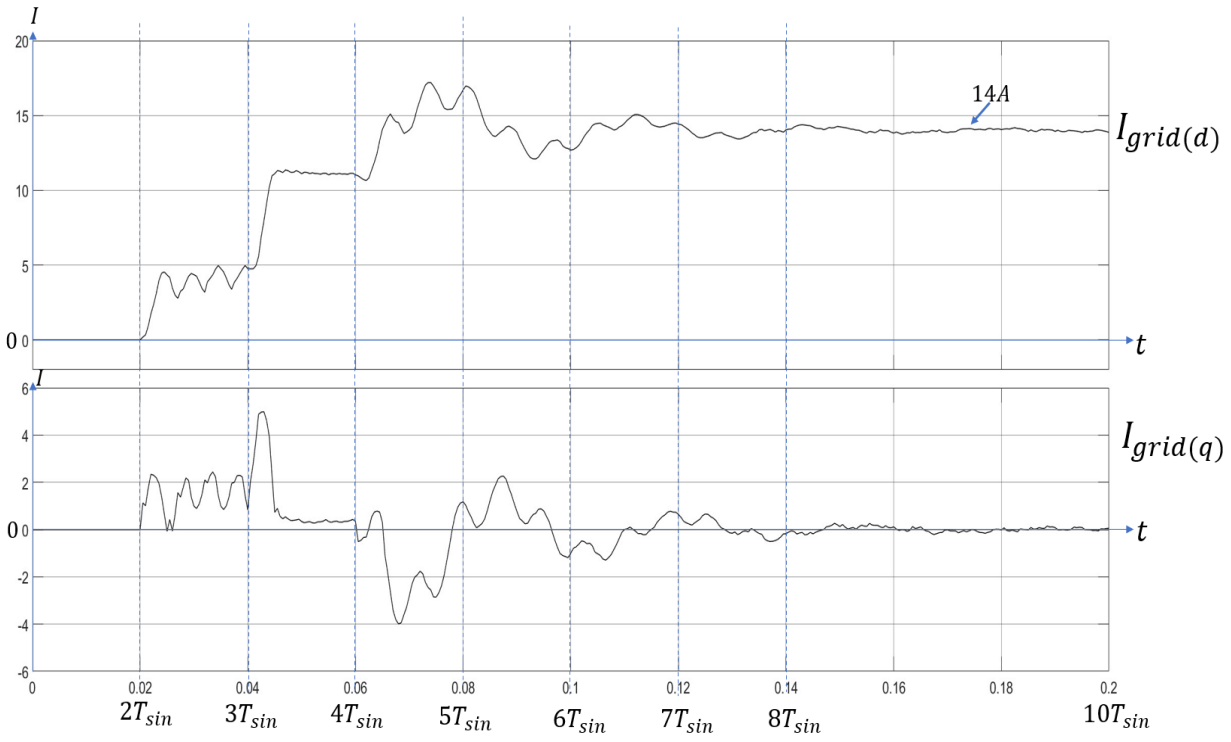


**Figure 6-23: Simulation result of $dq$-axis current of $I_{grid}$ with DTC system**

**Figure 6-24** shows simulation result of the grid voltage, current and inverter side fundamental voltage under different conditions after ***PLL*** and ***PI*** current controller works under steady-state conditions. As shown in **Figure 6-24**, from $\mathbf{0.2}\boldsymbol{s}$ to $\mathbf{0.3}\boldsymbol{s}$, ***PLL*** and current controller has worked under steady-state conditions and $\boldsymbol{T_d} = \mathbf{0}$. After $\boldsymbol{t} = \mathbf{0.3}\boldsymbol{s}$, $\boldsymbol{T_d}$ is changed to $\mathbf{1}\boldsymbol{us}$. It is clear to see that $\hat{\boldsymbol{I}}_{\boldsymbol{grid}}$ is decreased to $\mathbf{10.5}\boldsymbol{A}$ caused by dead time effect, but then $\hat{\boldsymbol{I}}_{\boldsymbol{grid}}$ is changed back to $\mathbf{14}\boldsymbol{A}$ because of current controller keeps $\boldsymbol{I}_{\boldsymbol{grid(d)}}$ to its reference value, and $\boldsymbol{I}_{\boldsymbol{grid(d)}}$ represents the $\hat{\boldsymbol{I}}_{\boldsymbol{grid}}$. In ***SPWM*** system, in order to maintain correct value of $\hat{\boldsymbol{I}}_{\boldsymbol{grid}}$, the $\hat{\boldsymbol{V}}_{\boldsymbol{sin}}$ of $\boldsymbol{V_{sin}(t)}$ in ***SPWM*** system is increased accordingly to maintain enough power into the grid to keep the current of $\boldsymbol{I}_{\boldsymbol{grid}}$.

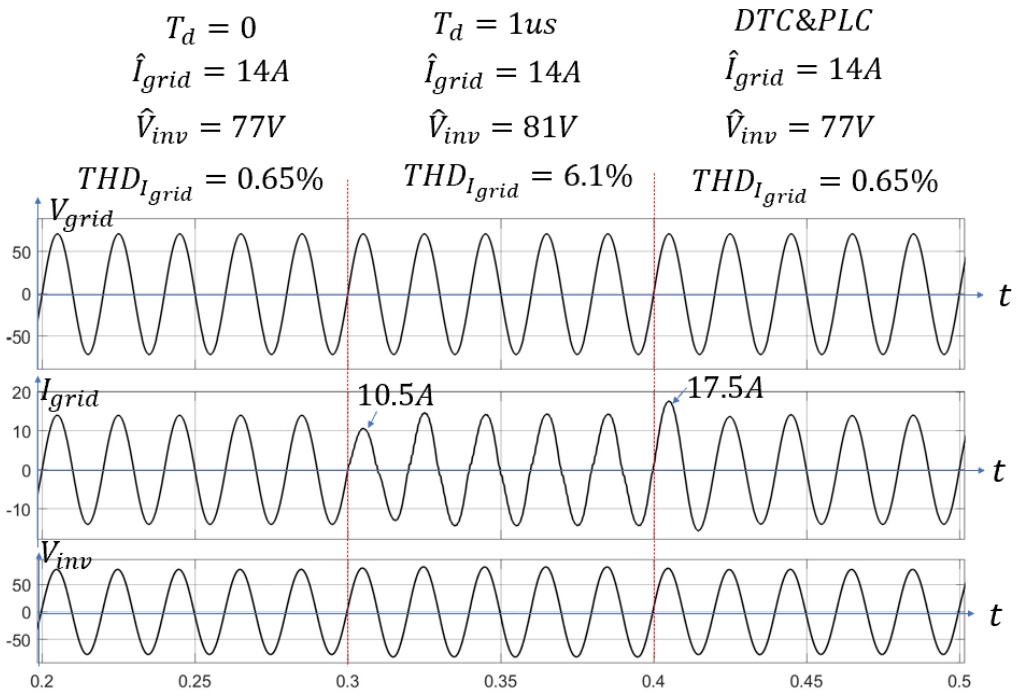


**Figure 6-24 : Simulation result of $V_{grid}$, $I_{grid}$ and $V_{inv}$ waveform under dead time effect and dead time compensation effect.**

After introducing dead time, although $\boldsymbol{PI}$ current controller can maintain the peak current value of $\boldsymbol{I_{grid}}$, the distortion caused by $\boldsymbol{T_d}$ cannot be compensated according to the $\boldsymbol{THD}$ value in $\boldsymbol{I_{grid}}$ shown in **Figure 6-24**. After $\boldsymbol{t = 0.4s}$, DTC system is enabled. $\boldsymbol{\hat{I}_{grid}}$ is increased because dead time compensation adds compensation value onto $\boldsymbol{V_{sin}(t)}$, then it is maintained to $\boldsymbol{14A}$ by current controller. After compensation, $\boldsymbol{\hat{V}_{inv}}$ changes from $\boldsymbol{81V}$ to $\boldsymbol{77V}$, which means $\boldsymbol{\hat{V}_{sin}}$ is decreased back to the value which is same to the $\boldsymbol{\hat{V}_{sin}}$ when $\boldsymbol{T_d = 0}$. The current reduction caused by $\boldsymbol{T_d}$ now is compensated by DTC instead of current control itself. In addition, it is clear to see that the distortion caused by $\boldsymbol{T_d}$ is compensated especially during current zero-crossing, and, therefore, $\boldsymbol{THD}$ is decreased.

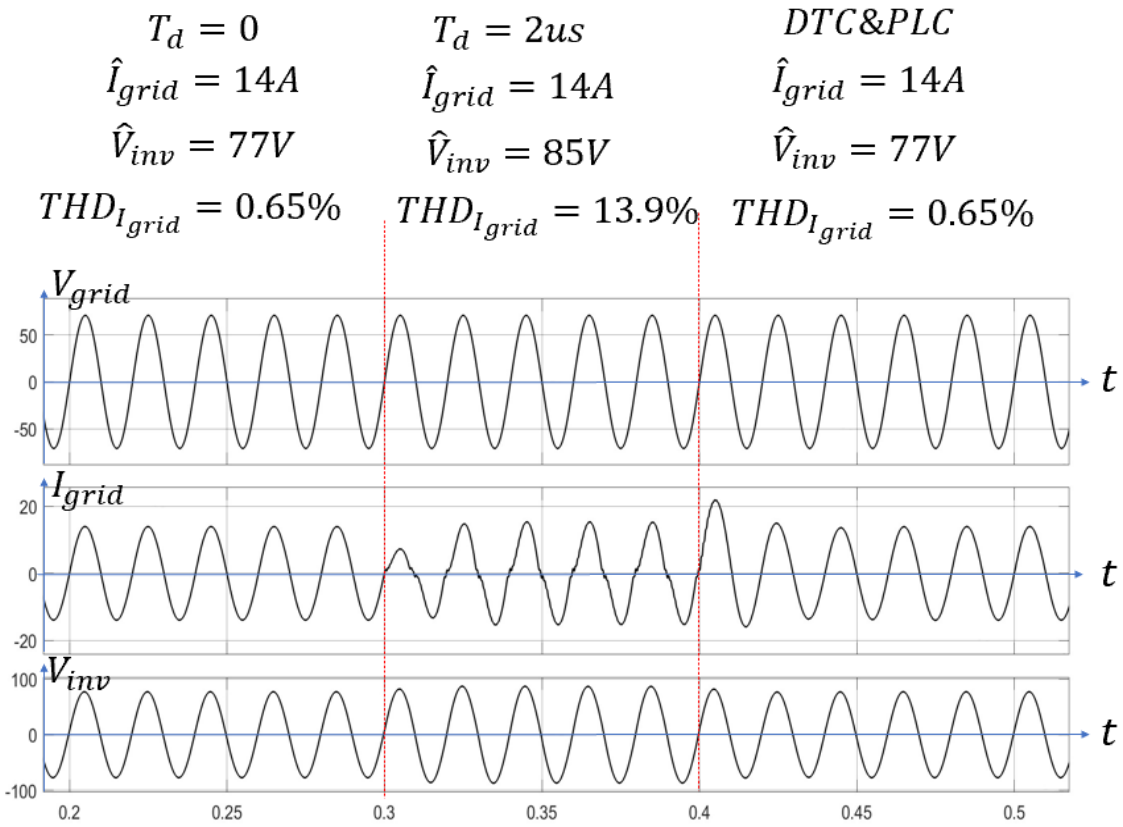


**Figure 6-25: Simulation result of $V_{grid}$, $I_{grid}$ and $V_{inv}$ waveform under dead time effect and dead time compensation effect.**

**Figure 6-25** shows the $V_{grid}$, $I_{grid}$ and $V_{inv}$ when $T_d = 2us$. The system exhibits similar behaviour with the addition of dead time introducing distortion near the zero crossing points and affecting the grid current. Compensation combined with feedback mitigates the effect of dead time and corrects for instantaneous errors.

The final part of this section shows the experiment result of $V_{grid}$ and $I_{grid}$ from the H-Bridge circuit when $T_d = 1us$ and $T_d = 2us$ and the output after adding dead time compensation.

**Figure 6-26** and **Figure 6-28** shows the $V_{grid}$ and $I_{grid}$ when $T_d = 1us$ and $T_d = 2us$, while **Figure 6-27** and **Figure 6-29** shows the output after system is added DTC into with $1us\ T_d$ and $2us\ T_d$.

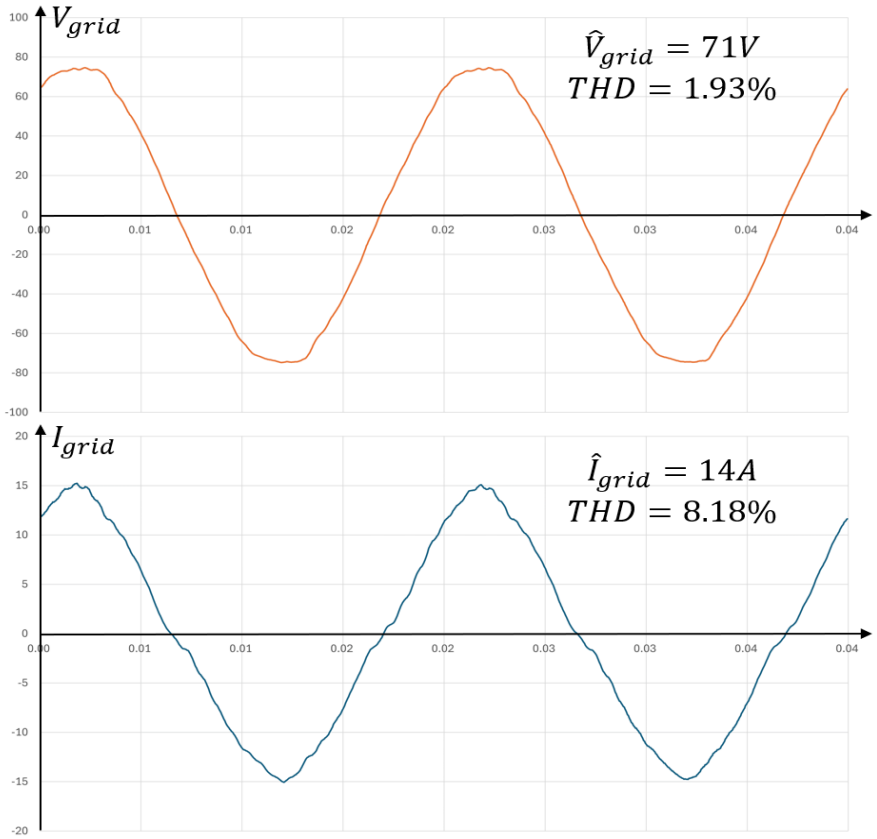


**Figure 6-26: Experimental result of grid voltage $V_{grid}$ and output current $I_{grid}$ when $T_d = 1us$.**

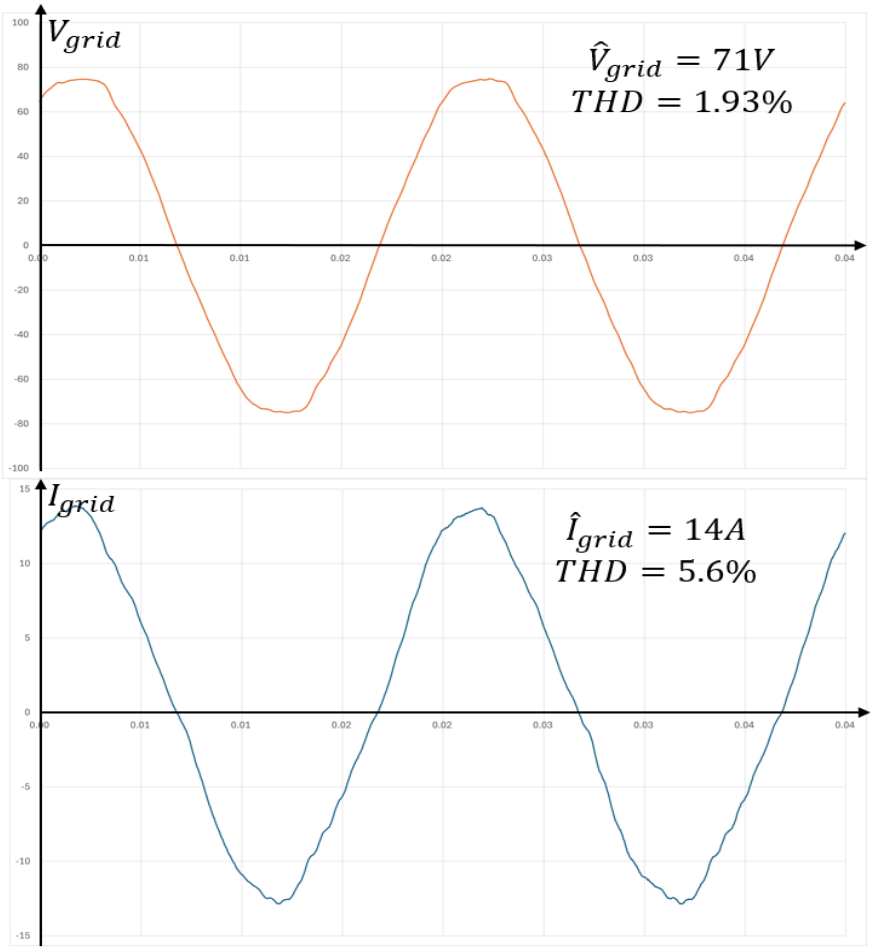


**Figure 6-27: Experimental result of grid voltage $V_{grid}$ and output current $I_{grid}$ when $T_d = 1us$ and adding Dead time Compensation.**

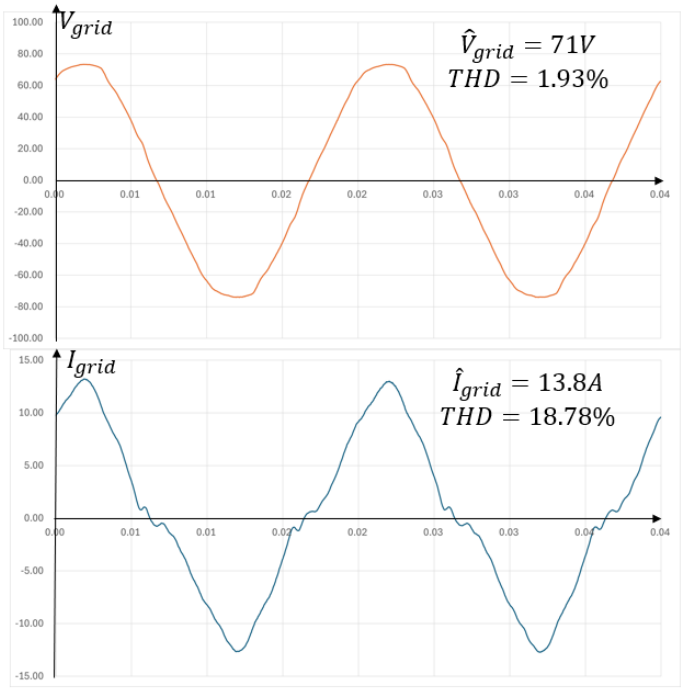


**Figure 6-28: Experimental result of grid voltage $V_{grid}$ and output current $I_{grid}$ when $T_d = 2us$.**

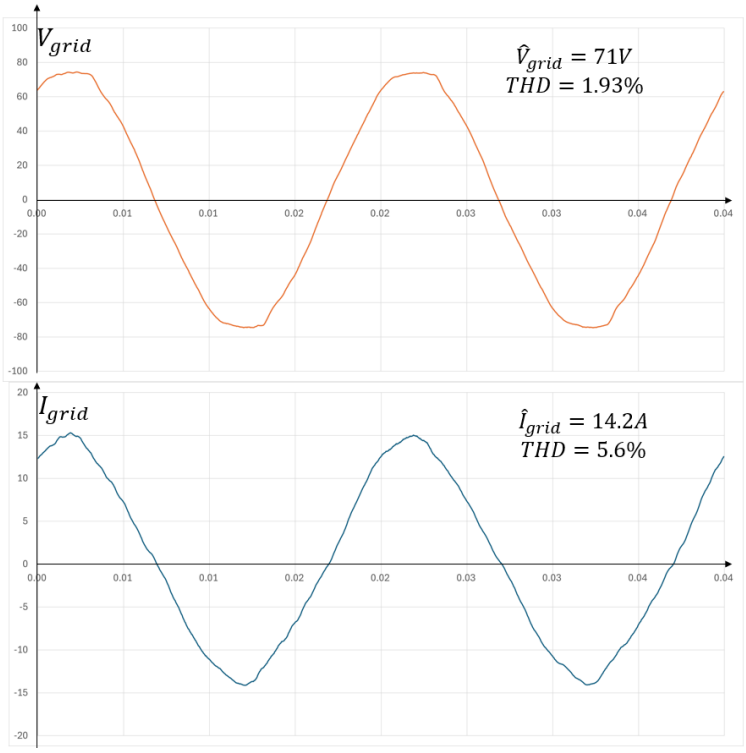


**Figure 6-29: Experimental result of grid voltage $V_{grid}$ and output current $I_{grid}$ when $T_d = 2us$ and with Dead time compensation.**

It is clear to see that more distortion is caused due to increase of $\boldsymbol{T_d}$, from $\mathbf{8.18\%}$ to $\mathbf{18.78\%}$ with significant distortion occurring near the zero-crossing of current. With $\boldsymbol{PI}$ current controller, the current can still maintain at reference set value. After adding DTC compensation, the distortion caused by $\boldsymbol{T_d}$ is compensated as shown in **Figure 6-27** and **Figure 6-29**. The $\boldsymbol{THD}$ after the compensation is $\mathbf{5.6\%}$. It should be noted that actual grid voltage is trapezoidal in shape rather than the pure sinewave used in the MATLAB simulations and this will also influence the distortion in output current $\boldsymbol{I_{grid}}$. But according to the $\boldsymbol{THD}$ measurement after Dead time compensation, the compensation system provides a significant amount of correction about the zero crossing-point, and this is further improved by the current controller.

In conclusion, this section provides the simulation and experimental results about dead time effect and dead time compensation operation in a 2-level grid connected H-Bridge power inverter. For the initial time of H-Bridge inverter, dead time effect causes current reduction when only $\boldsymbol{PLL}$ system is operating. With increase of $\boldsymbol{T_d}$, this current reduction is higher. And with increase of $\boldsymbol{T_d}$, more distortion is caused during the current zero-crossing.

With $\boldsymbol{DTC}$ system, the current reduction during the initial time is compensated, which solve the current overshoot problem after $\boldsymbol{PI}$ current controller is enabled as well. During steady-state conditions, the fluctuation of $\boldsymbol{dq}$-axis current is decreased by DTC system, which making $\boldsymbol{PI}$ current controller more stable. The distortion caused by dead time effect is compensated by DTC system in grid-connected H-Bridge system.

## 6.4 MATLAB Simulation validation of dead time effect and DTC operation in a Grid Connected 3-level H-Bridge Power inverter

In this section, the MATLAB simulation of DTC operation in 3-level H-Bridge inverter operation in close-loop system is shown.

**Figure 6-30** shows MATLAB Simulation structure of close-loop 3-level H-Bridge inverter with Dead Time Compensation system. The operation of ***PLL*** and ***PI*** current controller in 3-level H-Bridge inverter is similar to the system in 2-level H-Bridge inverter. Every component parameter in the H-Bridge is same which has been shown in section 6.1.

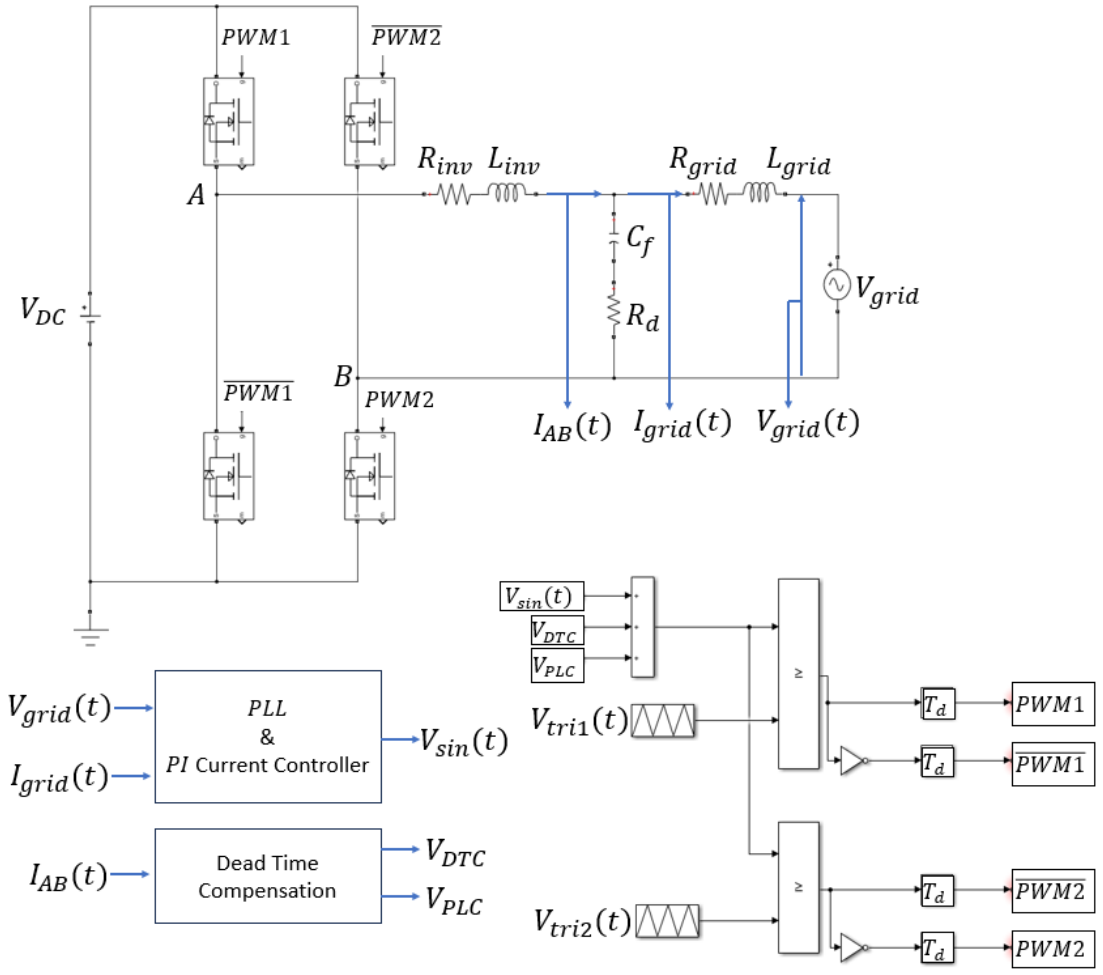


**Figure 6-30: Grid Connected 3-level H-Bridge power inverter MATLAB Simulation.**

The initial system of close-loop 3-level H-Bridge inverter is same to the system in 2-level which described in section 6.2. **Figure 6-31** shows the simulation result of grid voltage $\boldsymbol{V_{grid}(t)}$ and the comparation of output current $\boldsymbol{I_{grid}(t)}$ when system is working with $\boldsymbol{T_d = 0}$, $\boldsymbol{T_d = 1us}$ and with DTC operation.

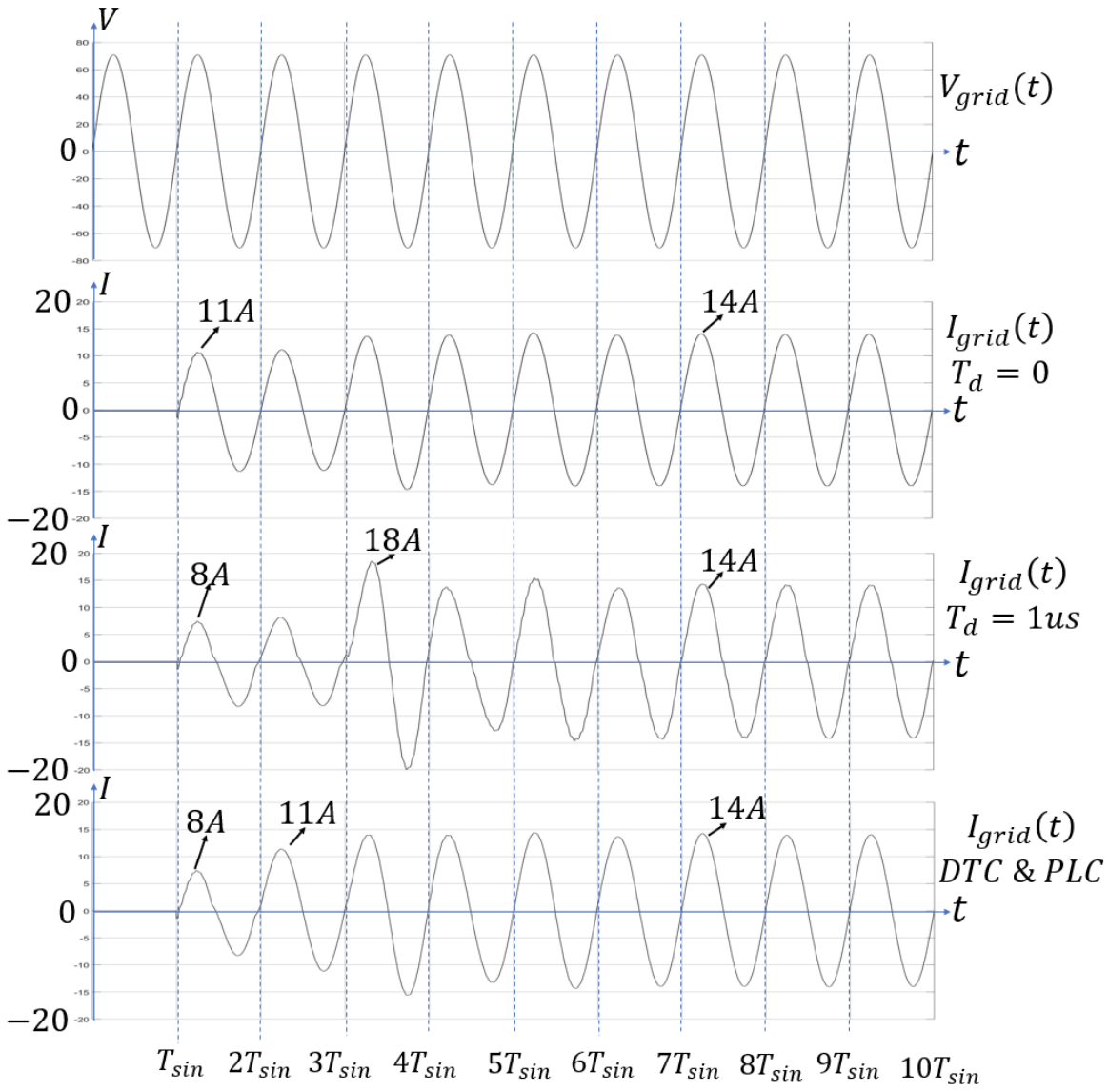


**Figure 6-31: Simulation result of $V_{grid}(t)$ and comparation of $I_{grid}(t)$ under different conditions during initial time.**

From $t = T_{sin}$ to $2T_{sin}$, only ***PLL*** controller is operating, output grid current is synchronized with grid voltage. Because of the initial peak modulation index is $0.75$, the $I_{grid}(t) = 11A$ if $T_d = 0$. As shown in **Figure 6-31**, $I_{grid}(t)$ is decreased to $8A$ because of $1us$ $T_d$ from $T_{sin}$ to $2T_{sin}$. According to equation (45) in section 3.5 about fundamental output voltage reduction, the reduction is half comparing to the voltage

reduction in 2-level system. Thus, the reduction in output current is only $\boldsymbol{3A}$. Since the $\boldsymbol{8A}$ is closer to the reference current $\boldsymbol{14A}$, the current over-shoot after $\boldsymbol{PI}$ current controller is operated after $\boldsymbol{t = 3T_{sin}}$ is lower which only reach to $\boldsymbol{18A}$. Although the peak current $\boldsymbol{\hat{I}_{grid}}$ when $\boldsymbol{T_d = 1us}$ reaches to $\boldsymbol{14A}$ after steady-state of $\boldsymbol{PI}$ current controller, more distortion is caused during the zero-crossing of $\boldsymbol{I_{grid}(t)}$.

As shown in **Figure 6-31**, after $\boldsymbol{t = 2T_{sin}}$, dead time compensation is activated, the current reduction is compensated. Most importantly, the distortion caused by dead time effect during zero-crossing is compensated by DTC system.

**Figure 6-32** shows the $\boldsymbol{dq}$-axis current from $\boldsymbol{I_{grid}(t)}$ when $\boldsymbol{T_d = 1us}$ and **Figure 6-33** shows the $\boldsymbol{dq}$-axis current from $\boldsymbol{I_{grid}(t)}$ when dead time compensation is operated. It is clear to see that the fluctuations of $\boldsymbol{dq}$-axis current after steady-state situation is larger with dead time effect. After DTC system is operated, the current fluctuation is decreased.

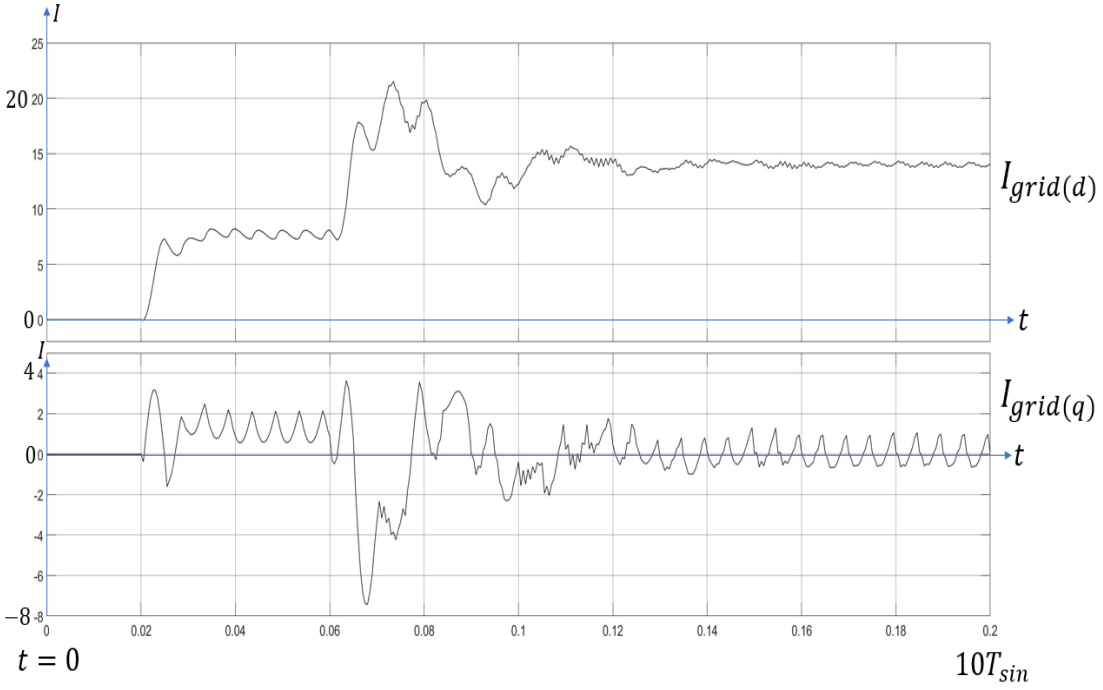


**Figure 6-32: Simulation result of $I_{grid(d)}$ and $I_{grid(q)}$ with $T_d = 1us$**

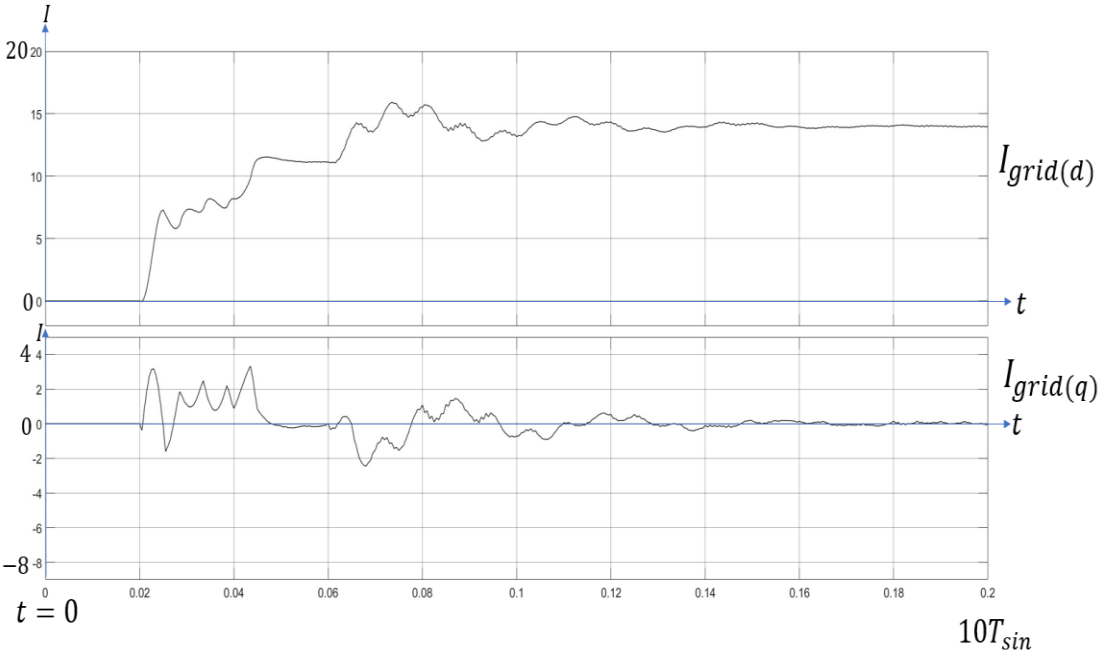


**Figure 6-33: Simulation result of $I_{grid(d)}$ and $I_{grid(q)}$ with DTC operation.**

**Figure 6-34** shows the comparation of $I_{grid}(t)$ when $T_d = 0$, $T_d = 1us$ and with Dead Time Compensation operation after steady-state of **PI** current controller. With

***PLL*** and ***PI*** current controller, the grid current can be synchronized with grid voltage. The $\hat{I}_{peak}$ can be kept at its reference peak value. The ***THD*** of $I_{grid}(t)$ is increased from $0.26\%$ to $4.04\%$ by the dead time. With the Dead Time Compensation operation, the distortion is compensated, ***THD*** is decreased back to $0.26\%$ referring to **Figure 6-34**.

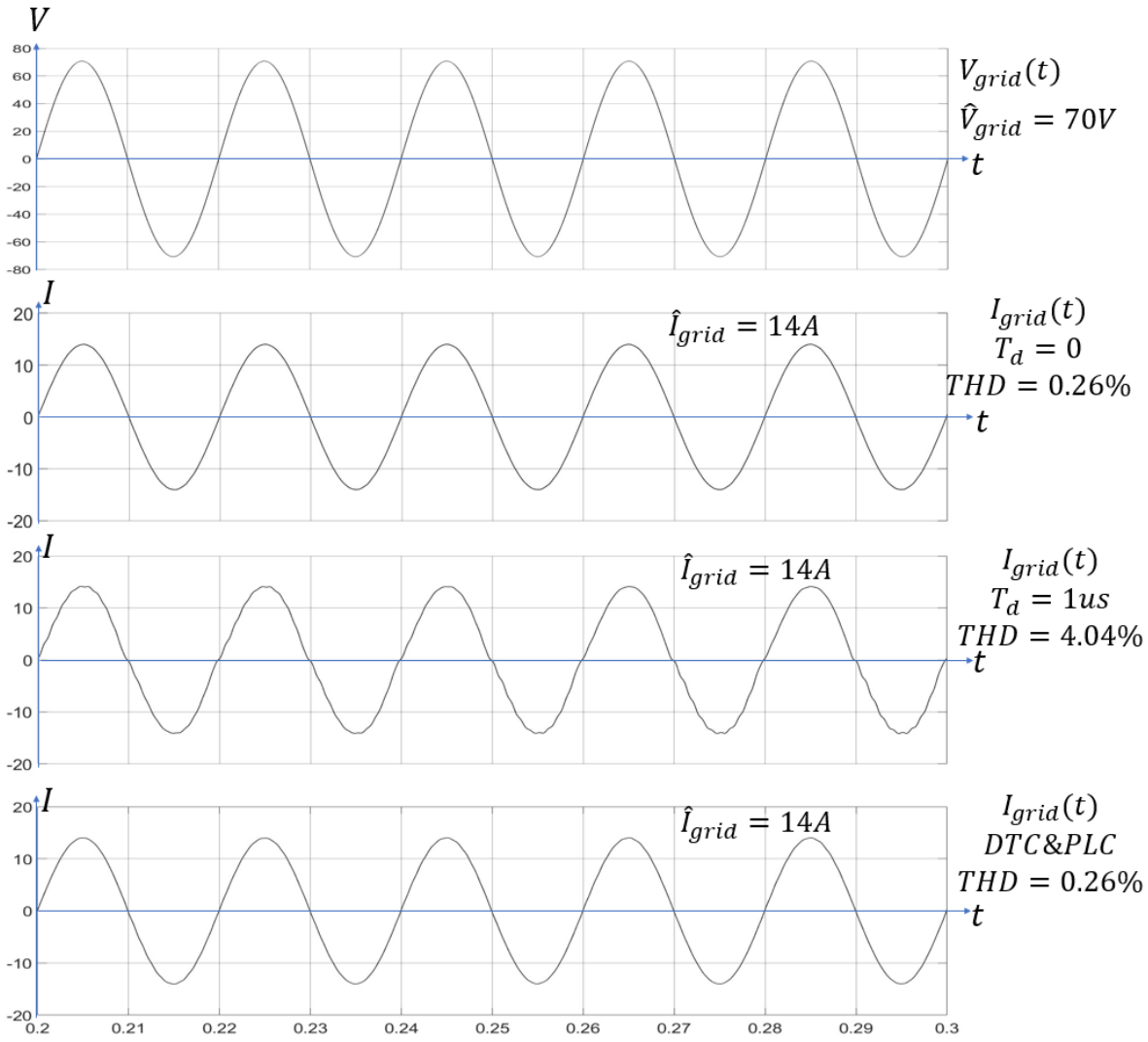


**Figure 6-34: Simulation result of $V_{grid}(t)$, and comparation of $I_{grid}(t)$ under different conditions after steady-state of *PI* current controller.**

**Figure 6-35** shows $\boldsymbol{I_{grid}(t)}$ comparison with $\boldsymbol{T_d = 2us}$. The $\boldsymbol{THD}$ is much higher reaching to $\mathbf{7.64\%}$ with $\boldsymbol{2us\ T_d}$, the distortion at zero-crossing is more serious. After Dead Time Compensation is activated. The distortion caused by dead time effect is compensated and $\boldsymbol{THD}$ is decreased to $\mathbf{0.31\%}$.

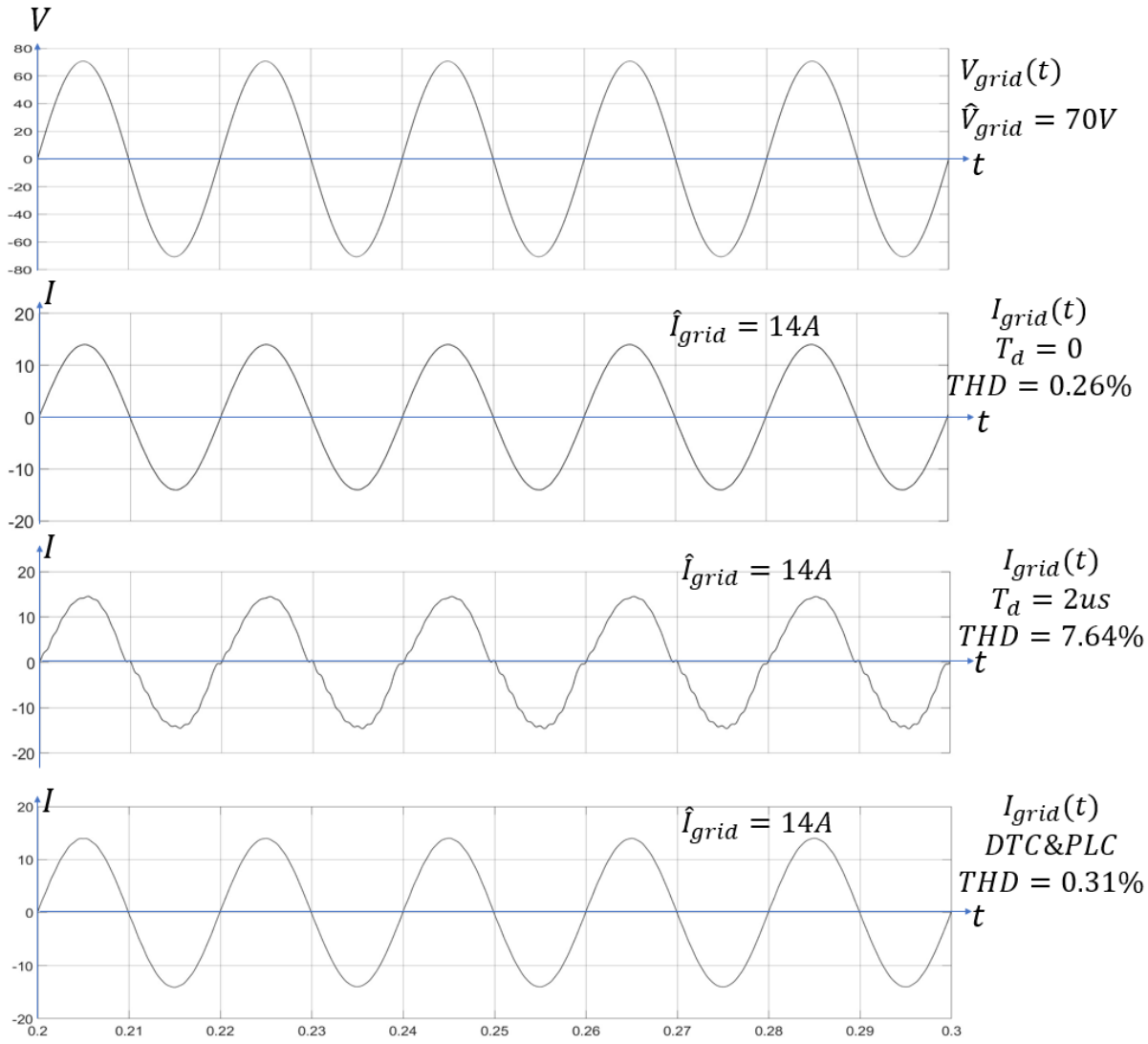


**Figure 6-35: Simulation result of $\boldsymbol{V_{grid}(t)}$, and comparation of $\boldsymbol{I_{grid}(t)}$ under different conditions after steady-state of $\boldsymbol{PI}$ current controller with $\boldsymbol{T_d = 2us}$.**

In conclusion, this section presents MATLAB Simulink simulation results of Dead Time Compensation in close-loop 3-level H-Bridge power inverter system. With longer

dead time, more distortion is caused especially during the zero-crossing time. After DTC system is operated, the distortion caused by dead time effect can be compensated which decreases the $\boldsymbol{THD}$. In addition, the current reduction caused by dead time effect during the initial $\boldsymbol{PLL}$ working can be compensated by DTC system as well. Which decrease the current over-shoot once the $\boldsymbol{PI}$ current controller is operated, making $\boldsymbol{PI}$ current controller more stable.

## 6.5 Chapter Conclusion

This chapter presents the simulation and experiment results of $\boldsymbol{DTC}$ and $\boldsymbol{PLC}$ system operation in a grid connected 2-level H-Bridge inverter firstly. It demonstrates the dead time effect during the initialization and steady-state operation of a close-loop 2-level H-Bridge inverter. The results shows that $\boldsymbol{DTC}$ and $\boldsymbol{PLC}$ system can compensate the current reduction during the initialization, and compensate the distortion caused by dead time during zero-crossing. Besides, the simulation results of DTC system operation in a grid connected 3-level H-Bridge inverter are shown in this section. The simulation validation shows that $\boldsymbol{DTC}$ and $\boldsymbol{PLC}$ system can compensate the current reduction when only $\boldsymbol{PLL}$ is operating. In addition, the most serious problem—the distortion cause by dead time during zero-crossing, can be compensated by $\boldsymbol{DTC}$ and $\boldsymbol{PLC}$ system in close-loop 3-level H-Bridge inverter system.

# *Chapter 7*

## *Conclusion and Future Plan*

This chapter summaries the works presented in this thesis. Then, some future work about the expansion of the research in this thesis will be demonstrated.

## 7.1 Thesis Conclusion

In Chapter 1, the background of development of power inverter technologies is introduced. The Grid-connected power inverter technology is popular and widely used in renewable energy system. For any power inverter system, dead time is necessary for avoiding short circuit events. But it causes voltage, current reduction and distortion during operation of power inverter. This provides a motivation to supply a Dead Time Compensation system used in grid-connected power inverter system for compensating current reduction and distortion caused by dead time.

In Chapter 2, the background and literature review related to grid-connected power inverter system is introduced. Including the basic structure of H-Bridge power inverter and 2-level, 3-level $\boldsymbol{SPWM}$ system. And the different technologies DTC and DTE for reducing dead time effect. Then, the function of each component in a $\boldsymbol{LCL}$ low-pass filter is described. In order to synchronize the output grid current from H-Bridge to the grid voltage and maintaining the output power from H-Bridge inverter, $\boldsymbol{PLL}$ and $\boldsymbol{PI}$

current controller is required. The literature review of different kinds of $\boldsymbol{PLL}$ and current controller are introduced in this chapter.

In Chapter 3, the novel Dead Time Compensation technologies for 2-level and 3-level grid connected H-Bridge power inverter is introduced. The Dead Time Compensation (DTC) includes two parts, a deadtime value compensation ($\boldsymbol{DTC}$) and phase lag compensation ($\boldsymbol{PLC}$). With the $\boldsymbol{DTC}$ and $\boldsymbol{PLC}$ operation, H-Bridge inverter can produce output voltage $\boldsymbol{V_{AB}}$ which is equal to the $\boldsymbol{V_{AB}}$ from ideal H-Bridge inverter ($\boldsymbol{T_d = 0}$).

In Chapter 4, the detail of every parameter calculation in $\boldsymbol{LCL}$ low-pass filter is described. Then, the detail of calculations of Proportion-Integral ($\boldsymbol{PI}$) component in $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current controller is described. Besides, in $\boldsymbol{PI}$ current controller section, the equation shows how the current coupling is caused and then the method of decoupling system is introduced. After that, the electrical circuit design of experimental platform is introduced, including H-Bridge inverter and its power switch driver circuit, detector and protection modules. Then the current and voltage sampling system is described. And then this chapter presents detail of Detector Modules design based on $\boldsymbol{ACPL\_7900}$ for providing accurate voltage and current data used in $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current controller. The detector designed in this thesis compensate the inaccurate reading of high frequency component of output current which is caused by unstable floating voltage supply at input of $\boldsymbol{ACPL\_7900}$. Then, a current polarity detector based

on $\boldsymbol{MAX913}$ comparator is introduced for providing high frequency and accurate current polarity data especially during zero-crossing to $\boldsymbol{DTC}$ system. Finally, the protection modules provide the methods for monitoring current through every power switch and limiting the max current through whole H-Bridge inverter.

In Chapter 5, the software design in microcontroller $\boldsymbol{STM32F407}$ is described, including the program of $\boldsymbol{SPWM}$ operation, $\boldsymbol{DTC}$, $\boldsymbol{PLC}$, $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current controller. Then, this chapter introduce the microcontroller system design of combining DTC system with grid connected system. In addition, it provides a system design method which solve the problem if processing speed of microcontroller is not enough.

In Chapter 6, the simulation and experiment validation of DTC system operation in grid-connected power inverter system is demonstrated. The first section in this chapter shows the operation of current and voltage detector. And the operation of current polarity detector is demonstrated. During the zero-crossing of output current $\boldsymbol{I_{AB}}$, the high switching frequency component in $\boldsymbol{I_{AB}}$ occurs multiple zero-crossing events, the current polarity turns in high frequency during this time. The result of current polarity detector demonstrates that it can produce accurate current direction information under high switching frequency conditions.

From section 2 to section 3 in this chapter, the simulation and experiment validation demonstrates the $\boldsymbol{DTC}$and $\boldsymbol{PLC}$system operation in grid-connected 2-level H-Bridge inverter. The results shows that the DTC can compensate voltage and current reduction,

compensate distortion caused by dead time especially during zero-crossing. In addition, the DTC system compensates the dead time effect without changing or disturbing the $\boldsymbol{PLL}$ and $\boldsymbol{PI}$ current control progress.

In section 4 in this chapter, the simulation result demonstrates the DTC system operation in grid-connected 3-level H-Bridge inverter. The results shows that DTC system can compensate current reduction during the initial time when only $\boldsymbol{PLL}$ is operating. In addition, the distortion caused by dead time is compensated by DTC system in close-loop 3-level H-Bridge inverter.

In conclusion, this thesis provides a novel Dead Time Compensation (DTC) method containing deadtime value compensation ($\boldsymbol{DTC}$) and phase lag compensation ($\boldsymbol{PLC}$) for grid-connected H-Bridge power inverter (2-level & 3-level).

In the DTC system in this thesis, the calculation of $\boldsymbol{V_{DTC}}$ and $\boldsymbol{V_{PLC}}$ are related to the $\boldsymbol{PWM}$ frequency, peak-to-peak voltage of carrier signal and $\boldsymbol{T_d}$. The new modulation reference signal is equal to $\boldsymbol{V_{sin}(t) + V_{DTC} + V_{PLC}}$. With the increase of $\boldsymbol{T_d}$, the peak voltage of new modulation signal ($\boldsymbol{V_{sin}(t)}$) may extend above the peak voltage of carrier signal which causes over-modulation. But in 3-level power inverter system, the $\boldsymbol{V_{DTC}}$ and $\boldsymbol{V_{PLC}}$ are both equal to half of the value in 2-level system. As result, the DTC system can compensate longer $\boldsymbol{T_d}$ without over-modulation in 3-level H-bridge system.

## 7.2 Future work

In 3-level H-Bridge inverter, the $\boldsymbol{SPWM}$ system is called Level-Shift $\boldsymbol{PWM}$ which is also a popular $\boldsymbol{SPWM}$ technologies used in other multi-level H-Bridge inverter such as 5-levels H-Bridge inverter. The analysis of dead time effect and dead time compensation in 3-level H-Bridge inverter is also suitable for higher level multi-level H-Bridge inverter with Level-Shift $\boldsymbol{PWM}$ system. With the increase of levels in multi-level H-Bridge inverter, the deadtime compensation value $\boldsymbol{V_{DTC}}$ and phase lag compensation value $\boldsymbol{V_{PLC}}$ is smaller according to the description in section 3.6 and 6.4. As result, over modulation caused by dead time compensation can be avoided easier in higher levels multi-level H-Bridge inverter. Multi-level H-Bridge inverter is usually built based on high switching speed power switches for operating in high frequency conditions. With the requirement of higher operating frequency inverter system, same dead time ($\boldsymbol{T_d}$) effect becomes more serious. Dead time effect can not be ignored, and dead time compensation is required. This thesis has started the dead time compensation research in grid connected 3-level H-Bridge inverter. It has potential to keep researching dead time compensation described in this thesis, which can be used in higher levels grid connected multilevel H-Bridge inverter.

The system presented here was limited in voltage (for health and safety reasons) and required the use of a step-up transformer. Often $\boldsymbol{PV}$ inverters contain isolation transformers for the purpose of mitigating leakage currents. Nowadays, $\boldsymbol{PV}$ Grid Connected Power Inverter technologies are arising where a boost power converter to increase the voltage level of $\boldsymbol{DC}$ supply, then transfer through the power inverter into

the grid without transformer (Transformerless Grid Connected Power Inverter). These technologies can decrease the size of whole system and decrease the price on building transformer. A further research opportunity exists to study the effect of dead time and dead time compensation systems on grid-connected transformerless PV inverter.

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