1550 nm Wavelength Single Photon Avalanche Diodes

(Design rules of double Zn diffusion and floating guard rings for premature edge breakdown suppression in planar InGaAs/InP SPADs)

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Contents

Abstract

An increasing number of diverse applications rely on single photon detectors to detect weak optical pulses. Among various single photon detectors, planar InGaAs/InP SPADs are the most practical for NIR detection. Since SPADs are operated beyond their avalanche breakdown voltage, it is vital to suppress premature edge breakdown. To evaluate existing design rules for edge breakdown suppression, two rounds of planar InGaAs/InP SPAD wafers (referred to as Round 1 and Round 2) were designed, fabricated and characterised for 1550 nm wavelength single photon detection. This thesis investigated the design rules of double Zn diffusion and FGRs for edge breakdown suppression through the measurements of avalanche gain, DCR and SPDE as well as electric field simulation.

The Round 1 wafers were found to be unsuitable for SPAD operation due to the non-optimal electric field profiles caused by wafer growth uncertainties. Hence, measurements and data analyses (2-D electric field simulations) were limited to linear-mode operation. Utilised actual Zn diffusion profiles, simulation data confirm the optimum difference to be $d_1 \geq 1.5$ μm and $(d_2 - d_1) \geq 0.5$ μm. Both experimental and simulation data suggested that the FGRs are only effective when their spacing is ≤ 4 μm. Increasing the Zn extension margin (beyond 4 μm) is also advisable to gain further PEB suppression.

Using improved wafer and device fabrication for Round 2, planar InGaAs/InP SPADs exhibit SPDE of up to 50 % with DCR of 1 Mcps at 225 K. Devices exhibit similar DCRs regardless of various Zn diffusion extensions, FGR spacing, number of FGRs or the absence of FGRs. The 2-D electric field simulation results indicate that FGR spacing needs to be ≤ 4 μm. They also highlight how the deviation of Zn diffusion profiles could reduce the effectiveness of stepped Zn diffusion, such that edge breakdown is present regardless of FGR designs. Despite the poor performance, round 2 illustrates that achieving the desired stepped Zn diffusion profiles (within the tolerance afforded by Zn diffusion technology) is crucial in suppressing premature edge breakdown.

Finally, a new wafer structure for planar InGaAs/InP APDs/SPADs to minimise the impact of Zn diffusion depths' deviation was proposed. In the proposed structure, although Zn diffusions are needed, the active region's electric field are not affected by the deviation in Zn diffusion depths. This is attributed to adding a p-charge sheet layer. 2-D electric field simulations suggest that the proposed structure does not suffer from PEB and so FGRs are redundant. Further simulations investigated how the proposed structure copes with ± 20 % variation in both p- and n- charge sheet doping densities. Overall, the simulation study demonstrated that the proposed wafer structure is promising in obtaining the desired electric field profiles regardless of the inaccuracies in Zn diffusion depths.

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Publications

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Abbreviations

APD	Avalanche photodiode
AR	Anti-Reflection
BBT	Band-to-band tunnelling
CW	Continuous Wave
PPLN	Periodically Poled Lithium Niobate
cps	Count per second
DIAL	Differential Absorption LiDAR
DCR	Dark Count Rate
DUT	Device under test
DGR	Double Guard Ring
EDFA	Erbium-Doped Fibre Amplifier
EVOA	Electrical Variable Optical Attenuator
EHP	Electron-Hole pair
FGR	Floating Guard Ring
FWHM	Full-Width at Half-Maximum
HMPT	Hybrid PMT
Hz	Hertz
HMDS	Hexamethyldisilazane
IR	Infra-red
ICP	Inductively Coupled Plasma
KTP	Potassium Titanyl Phosphate
LiDAR	Light Detection and Ranging
LIA	Lock-in amplifier
NIR	Near infra-red
NbN	Niobium Nitride
NIM	Nuclear Instrumentation Module
NGR	No Guard Ring
MIR	Mid Infra-red
MOCVD	Metal Organic Chemical Vapour Deposition
PMT	Photomultiplier Tube
PDF	Probability density function
PEB	Premature Edge Breakdown
PDE	Photon Detection Efficiency
PPLN	Periodically Poled Lithium Niobate

PMGI	Polymethylglutarimide
PECVD	Plasma Enhanced Chemical Vapour Deposition
QKD	Quantum Key Distribution
QE	Quantum Efficiency
RPL	Random Path Length
RIE	Reactive Ion Etching
SRH	Shockley-Read-Hall
SNSPD	Superconducting Nanowires Single Photon Detector
SPAD	Single Photon Avalanche Diode
SAM	Separate Absorption and Multiplication
SPDE	Single Photon Detection Efficiency
SAG	Selective Area Growth
SMU	Source Measure Unit
SIMS	Secondary Ion Mass Spectroscopy
SiO_2	Silicon oxide
SiN	Silicon nitride
SGR	Single Guard Ring
TDLiDAR	Tunable Diode LiDAR
TAT	Trap-assisted tunnelling
TTS	Transit Time Spread
TLM	Transmission Line Measurement
UV	Ultra-violet

Symbols

c	Speed of light
Δ_t	Time elapsed between the outgoing signal and returning signal
E_g	Bandgap of semiconductor
λ_c	Cutoff wavelength
h	Planck's constant
$\hbar$	Reduced Plank's constant
V_{bd}	Breakdown voltage
ζ	Ionisation path length
α	Ionisation coefficient of electron
β	Ionisation coefficient of hole
$h_e(\zeta)$	Probability density function of electron
$h_h(\zeta)$	Probability density function of hole
q	Electronic charge
E	Electric field
E_{th}	Threshold energy
α^*	Enabled ionisation coefficient of electron
β^*	Enabled ionisation coefficient of hole
d_e	Dead space for electron
d_h	Dead space for hole
w	Avalanche width
x	Position
M_e	Pure electron gain
M_h	Pure hole gain
M	Avalanche gain
F	Excess noise
k	Ratio of the ionisation coefficient
F_e	Excess noise from pure electron injection
F_h	Excess noise from pure hole injection
n_i	Intrinsic carrier concentration
A	Area
τ_{eff}	Effective carrier lifetime
m^*	Electron effective mass
α_T	Constant on the order of unity
E_a	Activation energy

I_{diff}	Diffusion current
I_{GR}	Generation and recombination current
I_{tunn}	Tunnelling current
W_{poten}	Width of the potential barrier
η	External quantum efficiency
P_a	Probability of photon absorption
P_b	Breakdown probability
V_{over}	Overbias ratio
t_{on}	On-time
V_{Bias}	Bias voltage
V_{DC}	DC bias
C	SPAD's capacitance
C_{bd}	Temperature coefficient of breakdown voltage
I_0	Forward current at 0 V
V	Total bias
n	Ideality factor
k_b	Boltzmann's constant
$W_0()$	Zeroth solution to the Lambert W function
$w(V)$	Voltage dependant depletion width
ε	Relative permittivity of the dielectric
V_p	Punchthrough volatge
N_{dop}	Doping concentration
V_{ph}	Potovoltage
R_{sense}	Sensing resister
I_{ph}	Photocurrent
I_{pri}	Primary current
$R_{measured}$	Measured responsivity
R_{ideal}	Ideal responsivity
P_d	Dark count probability
N_d	Number of measured dark counts per second
f	Repetition rate
$\mu_{variable}$	Attenuation in EVOA
$\mu_{coupling}$	Attenuation in Janis probe station
μ_{device}	Coupling efficiency
P_{in}	Measured optical power
R	Responsivity

I_p	Measured photocurrent
E_{pulse}	Measured pulse energy
E_{photon}	Photon energy for a given wavelength
$\bar{n}$	Average number of photons per pulse
N_t	Number of measured total counts per second
P_t	Probability of the measured events during the measurement
$P_{s(e)}$	Survival probability of electron
$P_{s(h)}$	Survival probability of hole
r	Random number
L	Random path length
v_e	Drift velocity of electron
v_h	Drift velocity of hole
n_e	Number of electron
n_h	Number of hole
$<t_b>$	Breakdown time
σ	Timing jitter
I_{L0}	Initial intensity of the light
α_{abs}	Absorption coefficient
J_{tun}	Tunnelling current density
P	Zn diffusion extension
S	Floating guard ring spacing
D	Diameter
E_{bd}	Breakdown electric field
T	Temperature
V_{ex}	Excess bias
P_{be}	Breakdown probability from pure electron injection
P_{bh}	Breakdown probability from pure hole injection
ΔV_{bd}	Breakdown voltage difference

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Chapter 1: Introduction

1.1 Applications

An increasing number of diverse applications rely on single photon detectors to detect weak optical pulses. Notable examples include Quantum Key Distribution (QKD), Light Detection and Ranging (LiDAR) and remote gas sensing, which are discussed in detail below. For some applications, their principle of operation relies on single photon detectors, whereas others could operate with less sensitive optical detectors but gain substantial performance improvement with single photon detectors.

1.1.1 Quantum Key Distribution (QKD)

QKD is a communication system for secured distribution of the secret encryption key [1], [2]. In a QKD system, the secret encryption key is shared between the sender and recipient using single photons for each signal 'bit' and transmitted through low-loss optical fibre links. The polarisation state of each photon represents a single bit (either '1' or '0') of the encryption. If an eavesdropper wants to steal the secret key, they must seize the photons of the bits. However, the non-cloning principle indicates that the photon's quantum state is impossible to replicate [2], [3]. Therefore, if the security of optical fibre link has been compromised by the presence of an eavesdropper, the authorised users will be alerted through excessive errors in the received encryption key. To implement the most secured QKD systems, truly single photon source and single photon detector are essential [4].

Implementation of QKD has progressed in recent years [5]–[7]. Initial attempts had limited usable link distance because the optical signal could not be amplified and loss in optical fibres, causing the data rate to decreases exponentially with the link distance [8]. This limitation was overcome by adopting twin-field QKD protocol, which utilises two phase-coherent signals from Alice and Bob [9], [10]. Based on this protocol and using ultra-low-loss fibre, [11] achieved a secret link with a key rate of 300 - 0.2 kb/s over 500 - 800 km without quantum repeaters. With shorter link distances, the key rates for fibre-based QKD systems are much higher, e.g. 115 Mb/s over a 10 km standard fibre [12]. QKD systems have also been demonstrated in free space, e.g. a satellite-based system with a secret key rate of 47.8 kb/s over 2000 km [13].

1.1.2 Light Detection and Ranging (LiDAR)

Using electromagnetic waves with shorter wavelengths than radio waves for range detection, LiDAR systems achieve longer ranges [14], [15]. It is widely used in environment monitoring [16]–[19], archaeology [20], [21] and autonomous driving [22]–[24]. It typically comprises a transmitter, a receiver, and an information processing system. Optical signals sent out by a laser in the transmitter

system are (partially) reflected by the target. The returning optical signals are detected by an optical detector employed in the receiver system. The distance between the LiDAR system and the target is given by $\frac{\Delta_t c}{2}$, where c is the speed of light and Δ_t is the time elapsed between the outgoing signal and returning signal.

The LiDAR system generally requires an optical detector with high gain because the returning optical signal can be heavily attenuated, or even down to a single photon level [22], [24]. Therefore, although the LiDAR system does not necessary require a single photon detector, it still can benefit from single photon detectors to achieve the longest range [25]–[27], especially when combining the technique of Time Correlated Single Photon Counting (TCSPC) [28], [29]. McCarthy *et al.* [30] employed an Single Photon Avalanche Diode (SPAD) in the LiDAR system that can measure range up to 4.5 km at 1550 nm wavelength. Later Pawlikowska *et al.* [31] obtained target's depth and intensity distribution map up to 10 km by using a highly sensitive SPAD. In addition, Zhu *et al.* [32] demonstrated their LiDAR can detect the sea fog within diameter of 180 km by using Superconducting Nanowire Single Photon Detectors (SNSPD).

1.1.3 Remote gas sensing

With the increasing pace of climate change, monitoring of greenhouse gases becomes particularly important. Optical gas sensing techniques, utilising the difference in gas absorption spectra, are a popular candidate in the gas sensing field due to their ability to be operated remotely [33]–[35]. Many industrially and environmentally essential gases have 'absorption signatures' in the infrared (IR) region while others absorb at ultra-violet (UV) wavelength. In particular, three significant greenhouse gases (CO_2, CH_4 and N_2O) exhibit clearly defined absorption peaks at NIR wavelengths between 1650 and 1750 nm [36]. This wavelength range is also where water vapour is weakly absorbing. Therefore, near-infrared (NIR) optical detection systems are suitable for environmental study and industrial monitoring. Unlike QKD demanding true single photon detection, gas sensing systems only require the detection of a weak signal which contains a few photons [37].

Despite the high cost and complicated design, Differential Absorption LiDAR (DIAL) is the most promising optical gas detection technique [17], [33], [36]. An example is shown in Fig. 1.1. The DIAL system utilises two (or more [17]) optical signal emitters with close but different wavelengths. The main emitter will send out optical pulses with the 'on wavelength' to coincide with an absorption peak of the gas of interest. The reference emitter also emits optical pulses but at the 'off wavelength' chosen to be just outside the absorption peak of the gas of interest. By comparing the intensity of the returning main signal and the reference signal, the DIAL system can obtain accurate gas concentration.

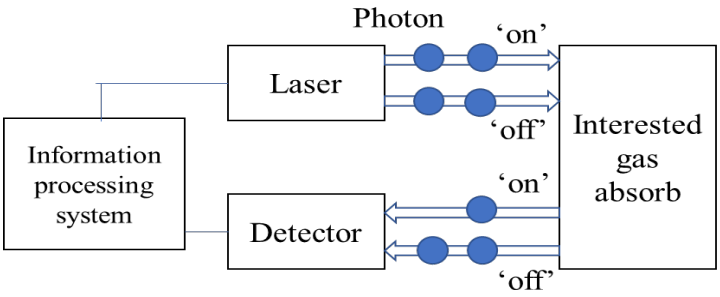

Fig. 1.1: Schematic illustration of Differential Absorption LiDAR (DIAL).

Another variant is Tunable Diode LiDAR (TDLiDAR) [37]–[39]. In [38], [39], the laser emission wavelength is tuned across a narrow band around 1650.9 nm wavelength, where methane exhibits a strong absorption peak. The laser emission is also modulated in time. Ref [37] added DIAL and utilised a SPAD in their TDLiDAR gas sensing system, achieving continuous methane monitoring capable of detecting leak as low as 0.012 g/s over a distance of 90 m [37].

1.2 Wavelength requirement and semiconductor material choice

There is a high demand for photon detection for NIR wavelength range from 800 to 1700 nm such as fibre optic telecommunication, QKD and LiDAR. Fibre-based communications require a detector highly sensitive to the 850, 1310 and 1550 nm wavelength, where the transmission loss in silica fibre is relatively low. Among those three wavelengths, 1550 nm becomes the mainstream wavelength because of its lowest optical power loss (0.2 dBm/km). In addition, optical communication systems typically require amplifying the optical signal by using an Erbium-Doped fibre amplifier, which has the second most prominent peak gain at 1550 nm (the first peak gain is at 1530 nm) [40].

Current LiDAR systems in self-driving vehicles mainly requires wavelength detection on 905 or 1550 nm for different considerations. The detector technology for 905 nm is based on Si so is far more mature than those at 1550 nm. The wavelength at 905 nm has a higher penetration ability in humid weather than at 1550 nm due to the strong water absorption at 1550 nm. However, the wavelength of 1550 nm has better eye safety than 905 nm, allowing higher output power for longer distance detection. Furthermore, the solar background at 1550 nm is lower than at 905 nm, leading to lower noise and less need for filtering techniques [27].

The photoelectric effect explains the photon-induced electrical current inside the semiconductor: an electron can gain energy by absorbing the incident photon such that it can be promoted from the valance band to the conduction band [41]. Therefore, the absorbed photon's minimum energy should be the same as the bandgap of the semiconductor material, E_g. The relationship between the cutoff wavelength, λ_c, and the semiconductor bandgap is given by

$$\lambda_c = \frac{hc}{E_g}, \tag{1.1}$$

where h is the Planck's constant.

Materials with different bandgaps thus have different λ_c, resulting in different detection wavelength ranges. SPADs utilising Si (λ_c = 1100 nm), Ge (λ_c = 1800 nm) or $In_{0.53}Ga_{0.47}As$ (λ_c = 1700 nm, referred to InGaAs hereafter) for photon absorption are suitable for the detection of photons with the wavelength in the range of 300 - 1100 nm, 800 - 1800 nm, or 700 - 1700 nm, respectively [42]–[44].

Si based SPADs are a popular choice for the most APD detection and dominate the market because of their huge manufacturing base. However, it cannot detect the photons with wavelength between 1300 - 1550 nm, which are crucial for optical fibre communications and remote gas sensing. Ge has a cutoff wavelength of 1800 nm, but its indirect bandgap reduces photon absorption efficient ~ 1550 nm wavelength. With a cutoff wavelength of 1700 nm, a direct bandgap and being lattice-matched to InP substrate, InGaAs become the most common choice for 1550 nm wavelength detection [45]. An alternative optical detection material is $GaAs_{0.52}Sb_{0.48}$ (refer to GaAsSb hereafter), which has a similar bandgap and to InGaAs and is also lattice matched to InP substrates [46], [47]. Wafer growth and device fabrication technologies for GaAsSb are however considerably less matured than those for InGaAs. Therefore, InGaAs-based SPADs were chosen for NIR wavelength detection. Specifically, this thesis focuses on the design rules for planar InGaAs/InP SPADs.

1.3 Thesis organisation

Chapter 2 gives the background theory for impact ionisation which yields avalanche multiplication and excess noise in APDs, followed by the key parameters for SPADs, such as DCR, SPDE, afterpulsing and timing jitter. Additionally, quenching circuity for SPAD operation were also included. Furthermore, different type of SPADs for NIR wavelength detection were reviewed, along with other technologies for single photon detection.

Chapter 3 introduced the methodology for devices fabrication and characterisation. Simulation models for devices design and data analysis were also introduced.

Chapter 4 – planar InGaAs/InP SPADs were design, grown and fabricated using different combinations of Zn diffusion profiles and FGRs spacing. Devices do not work as proper SPADs because the actual electric field profiles are different from the intended design, which confirmed by experimental C-V data and 1-D electric field simulations. The effectiveness of various Zn diffusion profiles and FGRs design on edge breakdown suppression for planar InGaAs/InP APDs were investigated using the2-D electric field simulations.

Chapter 5 presents experimental and simulation results of InGaAs/InP SPADs produced in Round 2, using improved wafer and devices fabrication compare to those in Chap. 4. Planar InGaAs/InP SPADs with double Zn diffusion exhibits SPDE of up to 50 % with DCR of 1 Mcps at 225 K. The effect of Zn diffusion extension and FGRs design on DCR and SPDE were evaluated and discussed.

Chapter 6 investigated the design criteria for optimising the Zn diffusion depths for planar InGaAs/InP SPADs with double Zn diffusion. The desired electric profile is sensitive to the variation of charge sheet doping and the deviation in Zn diffusion depths during the wafer growth. A new structure was proposed to relax the tolerance of Zn diffusion process, followed by the investigation of FGRs, Zn diffusion extension and charge sheet sensitivity for the proposed structure design.

Chapter 7 concludes the thesis and provides suggestion for future research work of existing and proposed structure for planar InGaAs/InP SPADs.

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Chapter 2: Background Theory and Literature Review

2.1 Avalanche photodiodes (APDs)

In its simplest possible form, an APD is essentially a reverse biased PN diode. When a large reverse bias is applied to a PN junction, the current will rapidly increase, identified as breakdown. The corresponding voltage is named breakdown voltage V_{bd}. If the breakdown is caused by the avalanche, the breakdown is named avalanche breakdown. Otherwise, it is tunnelling breakdown, which is also known as Zener breakdown.

2.1.1 Impact ionisation

Impact ionisation is fundamental to the operation of APDs and SPADs. In an electron-initiated impact ionisation event, when an electron gains sufficient energy from a strong reverse electric field, it can promote a bound electron from the valance band to the conduction band, by giving up all or some of its energy. There are now two free electrons and a free hole, as illustrated in Fig. 2.1(a). In a hole-initiated impact ionisation event, the hole gives up some or all of its energy to produce a pair of free electron and hole. The daughter electron and hole can also gain energy from the reverse electric field and eventually have sufficiently high energy to initiate further impact ionisation events. Successive impact ionisation events will lead to a significant multiplication of primary carriers, hence current amplification or internal gain.

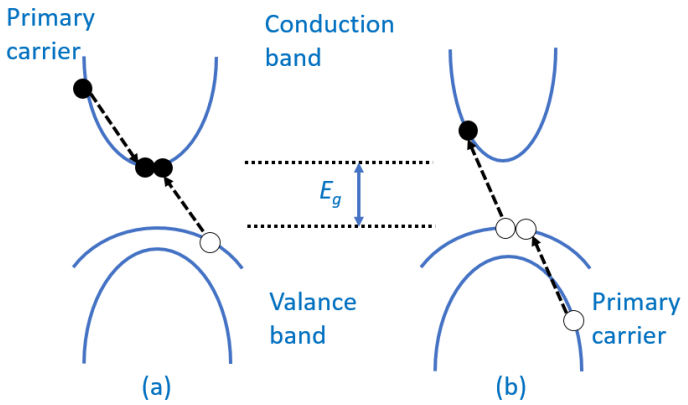

Fig. 2.1: Illustrations of (a) an electron-initiated and (b) a hole-initiated impact ionisation event.

The impact ionisation process is a random process. There is a distribution of the carrier's path length between two consecutive ionisation events, termed ionisation path length, ζ. The reciprocal of the average ionisation path length is termed impact ionisation coefficient, α (for electron) and β (for hole),

respectively. These are material properties representing a carrier's ability to initiate impact ionisation per unit distance. They are also strongly dependent on the electric field and temperature (because phonon scattering is sensitive to the temperature).

In several important APD/SPAD simulation models, the probability density function (PDF) of ζ, $h_e(\zeta)$ for electron and $h_h(\zeta)$ for hole, are the main material- and field-specific inputs to the models. An example of $h_e(\zeta)$ is shown in Fig. 2.2 (dashed line). $h_e(\zeta)$ has non-zero values for all positive ζ values, meaning the electron can initiate impact ionisation process regardless of its ionisation path length since its injection or its last ionisation event.

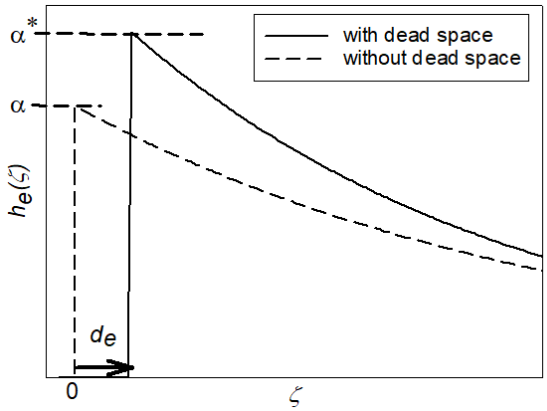

Fig. 2.2: Examples of $h_e(\zeta)$ with and without dead space.

However, the carrier's history can affect the distribution of ζ. A carrier must travel a certain distance under the electric field to gain sufficient energy in order to initiate impact ionisation. The minimum distance required is called carrier's dead space, which can become significant in narrow avalanche regions (< 500 nm approximately) [1], [2]. The relationship between the dead space and threshold energy is expressed as

$$d = \frac{E_{th}}{qE}, \tag{2.1}$$

where q is the electronic charge, E is the electric field, and E_{th} is the threshold energy (usually greater than the bandgap).

Many realistic yet computationally efficient APD/SPAD simulation models use a 'hard' dead space approximation for $h_e(\zeta)$ and $h_h(\zeta)$ to account for the carriers' history. In this approximation, $h_e(x_e)$ is given by [1]

$$h_e(\zeta_e) = \begin{cases} 0 & , \quad \zeta_e < d_e \\ \alpha^* \exp[-\alpha^*(\zeta_e - d_e)] & , \quad \zeta_e \geq d_e \end{cases}, \tag{2.2}$$

where α^* and d_e are the electron's enabled ionisation coefficient and the dead space, respectively. The relationship between α and α^* is given by

$$\alpha^* = (\frac{1}{\alpha} - d_e)^{-1}. \tag{2.3}$$

Similar expressions for holes are obtained by replacing d_e and α^* with d_h and β^* in Eqn. (2.2) and (2.3). An example of $h_e(\zeta)$ using 'hard' dead space approximation is shown in Fig. 2.2. Suppose a carrier has travelled a distance ζ less than dead space, it cannot initiate any impact ionisation and $h_e(\zeta)$ is zero. When ζ reaches or exceeds dead space, $h_e(\zeta)$ becomes non-zero.

2.1.2 Avalanche gain and noise

In 1966, McIntyre [3] developed analytical equations for avalanche gain as functions of ionisation coefficients and carrier injection position. One of the assumptions used was that the ionisation coefficient depends only on the uniform electric field instead of the carriers' history. This was later termed by other APD researchers as the local model. Although the local model can lead to inaccurate results when dead space becomes significant (as in the case of later APD designs), its simplicity and accessibility has ensured its continued use. In the local model, the gain of an APD due to the injected carrier at position x is given by:

$$M(x) = \frac{\exp[-\int_x^w (\alpha - \beta)dx']}{1 - \int_0^w \alpha \exp[-\int_{x'}^w (\alpha - \beta dx'')]dx'}, \tag{2.4}$$

where w is the avalanche width.

The injection profile of the carrier clearly affects the value of M for a given APD. If $x = 0$ or w, then the resultant gain is termed as pure electron gain, M_e, or pure hole gain, M_h, respectively. Assuming a constant electric field profile (i.e. α and β remain constant within the avalanche region), Eqn. (2.4) can be simplified into

$$M_e = \frac{1}{1 - \frac{\alpha}{\beta - \alpha}(\exp[(\beta - \alpha)w] - 1)} \tag{2.5}$$

and

$$M_h = \frac{1}{1 - \frac{\beta}{\alpha - \beta}(\exp[(\alpha - \beta)w] - 1)}. \tag{2.6}$$

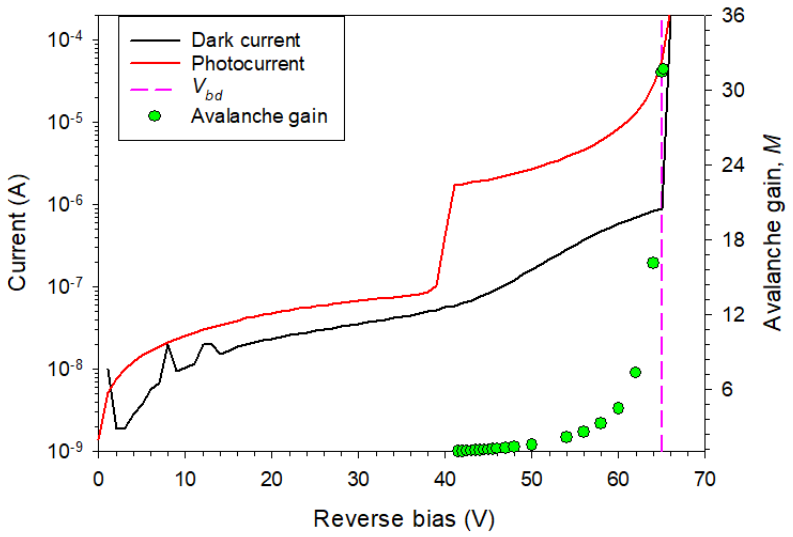

Fig. 2.3: Example of experimental results of reverse current-voltage data of an APD with and without light.

Avalanche breakdown occurs when the gain becomes infinite, resulting in a self-sustaining avalanche current. Fig. 2.3 shows an example of avalanche breakdown at -65 V, where the current rapidly increases. The breakdown voltage estimated from the current increase should agree with the measured avalanche gain. Otherwise, it might come from another mechanism, such as premature edge breakdown (PEB). Using the local model, the breakdown voltage of an ideal p-i-n APD can be obtained from the horizontal axis offset from 1/*M* versus reverse bias plots, as presented in Fig. 2.4. In principle, avalanche breakdown requires a positive feedback loop from the electrons and holes. If the ionisation process is initiated only by a single type of carrier (i.e. electrons in InAs), the gain will exponentially increase but cannot produce a self-sustaining current.

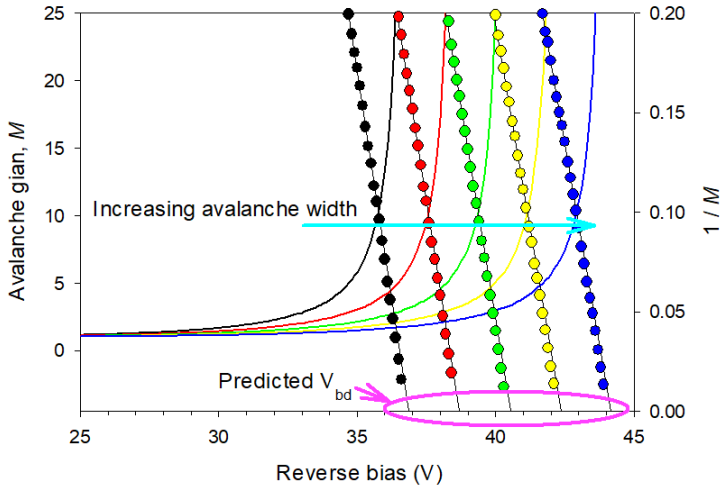

Fig. 2.4: Estimating from 1/M versus V characterisation, the results were plotted from calculation.

There is a fluctuation in the gain due to the randomness of impact ionisation. The associated noise in an APD is characterised by excess noise factor, F, defined as

$$F = \frac{< M^2 >}{< M >^2}. \tag{2.7}$$

McIntyre's local model predicted that the F can be expressed as a function of gain and the ratio of the ionisation coefficient k ($k = \beta/\alpha$) [3]. The pure electron and pure hole initiated multiplication noise, F_e and F_h, can be calculated from

$$F_e(M_e) = kM_e + (2 - \frac{1}{M_e})(1 - k) \tag{2.8}$$

and

$$F_h(M_h) = \frac{1}{k}M_h + \left(2 - \frac{1}{M_h}\right)\left(1 - \frac{1}{k}\right). \tag{2.9}$$

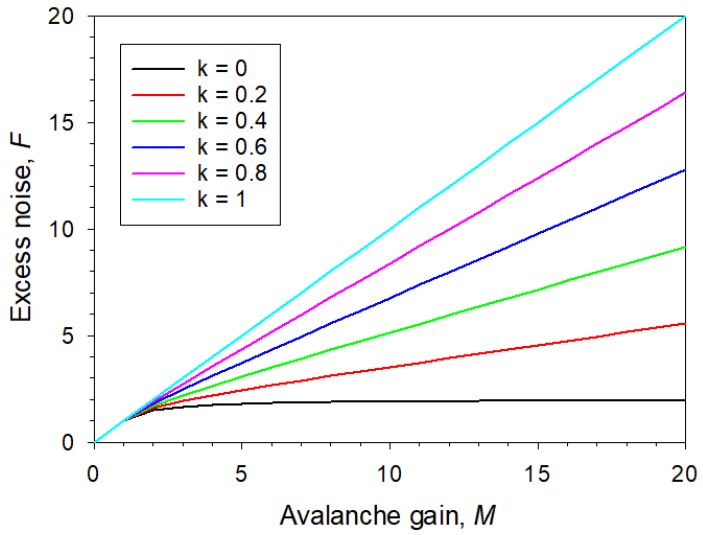

Fig. 2.5: Predicted excess noise for k = 0 to 1 in the step of 0.2 using the local model (Eqn. (2.8)).

Fixing the M term in Eqn. (2.8), the excess noise for material with different k is compared in Fig. 2.5. APD with low excess noise can be obtained by utilising a material with dissimilar α and β. Choosing an appropriate carrier injection profile for a given material can also achieve low excess noise. Take InP as an example; its β is greater than α for a given electric field, so the gain from pure hole injection is higher than that from pure electron injection, as demonstrated in Fig. 2.6. Moreover, the noise is lower from pure hole injection than from pure electron injection.

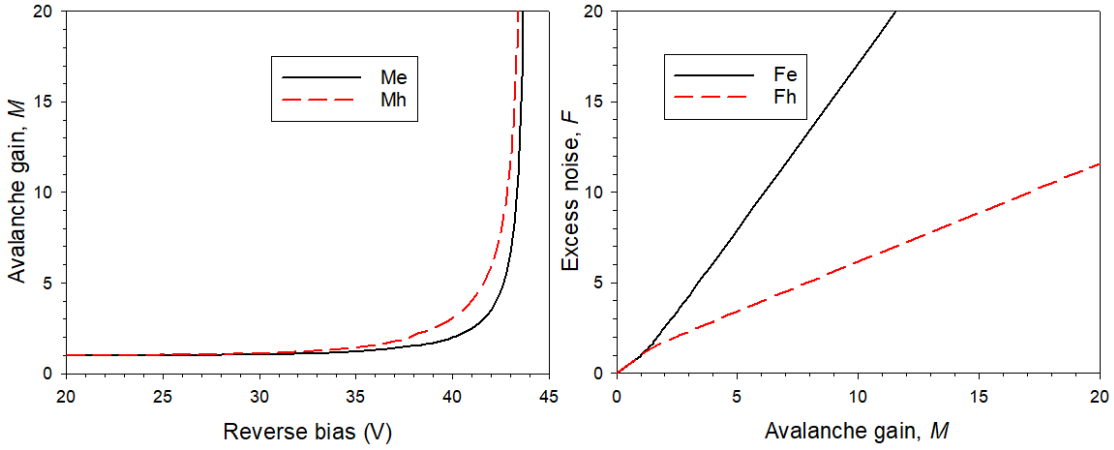

Fig. 2.6: Calculated (left) M_e (V) and M_h (V) and (right) F_e (V) and F_h (V) of InP using the local model and reported ionisation coefficient [4].

2.1.3 APD dark current

The dark current is devices dependent, while the photocurrent is the product of the primary current multiplied by the avalanche gain. High dark current will limits the achievable gain and so the sensitivity of the APD. Hence, APD's dark current should be as low as possible. The dark current is mainly dominated by two mechanisms: bulk dark current and surface leakage current (more details in section 3.1.2). It is preferring the dark current is dominated by the bulk current since it can be reduced by dropping the operating temperature, while the surface leakage current is less sensitive to the temperature.

The bulk dark current consists of the diffusion current I_{diff}, generation and recombination current I_{GR} and band-to-band tunnelling current I_{tun}, given by the following equation:

$$I_{diff} = I_0\left[\exp\left(\frac{qV}{k_bT}\right) - 1\right], \tag{2.10}$$

$$I_{GR} = \frac{qn_iAW}{\tau_{eff}}, \tag{2.11}$$

and

$$I_{tunn} = \frac{(2m^*)^{1/2}q^3EVA}{4\pi^2\hbar^2{E_g}^{1/2}}\exp\left(-\frac{\alpha_T(2m^*)^{\frac{1}{2}}E_g^{\frac{3}{2}}}{qE\hbar}\right), \tag{2.12}$$

where n_i is the intrinsic carrier concentration, A is the device's area, τ_{eff} is the effective carrier lifetime, m^* is the electron effective mass, $\hbar$ is the reduced Plank's constant, and α_T is a constant on the order of unity and dependent on the shape of the potential barrier.

At the low field, bulk dark current is mainly dominated by I_{diff} and $I_{GR,}$ while either I_{tunn} or avalanche dominates the current at the high field region. Both I_{diff} and I_{GR} is highly sensitive to the operating temperature, each of them can be distinguished by extracting the activation energy E_a from Arrhenius

plot. If the E_a is closed to bandgap, the current is dominated by I_{diff}, while the I_{GR} is dominating when E_a is close to half of the bandgap.

On the other hand, if the avalanche dominates the high field and results in a breakdown, the current will increase sharply at V_{bd}. In contrast, the sharpness of the current increase will reduce when the tunnelling become significant, increasing the dark current. Furthermore, the tunnelling current is not sensitive to the temperature, making it less controllable cf. avalanche.

2.2 SPAD

Depending on the applied reverse bias, there are two operation modes of APD: linear mode and Geiger mode. The linear mode APDs are operated below V_{bd} whereas the Geiger mode APDs are operated above V_{bd}. Above breakdown voltage, the reverse electric field is large enough to allow a single photo-generated carrier to produce a measurable electrical signal. Hence, the Geiger mode APD is also known as the SPAD. It is highly sensitive and quickly responds to the detection of the weak light signal down to a single photon level. For SPAD, the performance is no longer determined by the gain and excess noise since the gain is infinite after the avalanche breakdown. Instead, SPAD's performance is characterised by the dark count rate (DCR), photon detection efficiency (PDE), jitter and afterpulsing effect.

2.2.1 Dark count rate

SPADs have the same dark current characterisation as APDs. Under such a high electric field in SPAD, a dark carrier can trigger an avalanche breakdown event without an incident photon. The undesirable triggering events are taken as the noise of the SPAD, and the rate of these events triggered by dark carriers per second is described as the dark count rate. The unit of DCR is taken as Hz or count per second (cps). Three main mechanisms will contribute to DCR: thermal generation, band-to-band tunnelling (BBT) and trap-assisted tunnelling (TAT).

Thermal generation contains I_{diff} and I_{GR} and it is one of the main mechanisms contributing to the dark count rate, where the carriers gain enough thermal energy to promote themselves from the valance band to the conduction band [5]. In practice, the generation and recombination is more likely to happened in the absorption region of the SPAD. This can be described by the Shockley-Read-Hall (SRH) process and can be estimated through the extracted activated energy E_a, which is approximately half of the bandgap.

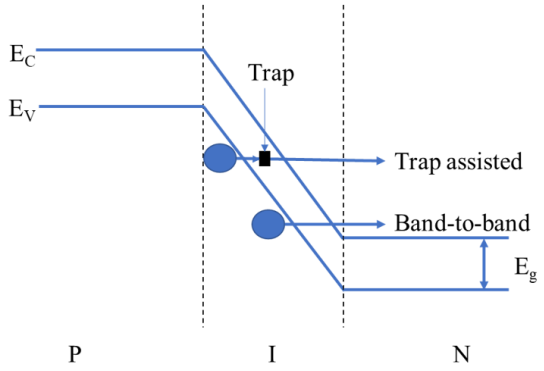

Fig. 2.7: Schematic of tunnelling process.

In BBT, the bounded electrons in the valence band could overcome the potential barrier by quantum-tunnelling into the conduction band. A schematic of two tunnelling mechanism is illustrated in Fig. 2.7 using an ideal p-i-n diode. As the electric field increases, the potential barrier width, W_{poten} becomes thinner, allowing the electron to tunnel through more easily [6],

$$W_{poten} = \frac{E_g}{qE}. \tag{2.13}$$

Where E_g is the material bandgap, E is the electric field, and W_{poten} is the width of the potential barrier. TAT is a complex tunnelling process since it involves the existence of traps, which are typically formed by the semiconductor defect. In this case, the potential barrier could be split into two separate small barriers by the deep-level defects of the semiconductor. Thus, trapped carriers can tunnel more easily, increasing the DCR.

2.2.2 Single photon detection efficiency

The sensitivity of the SPAD is characterised by Photon Detection Efficiency (PDE), which is the product of external quantum efficiency, η, and breakdown probability P_b, expressed as

$$PDE = \eta \times P_b\,. \tag{2.14}$$

Sometimes, the PDE is expressed as single photon detection efficiency (SPDE) or single photon quantum efficiency [7]–[9]. The external quantum efficiency itself is the product of the probability of photon absorption (P_a) and the probability of photo-generated carriers transit from photon absorption region into multiplication region (P_t). P_t is less than unity in SPAD with heterostructure within the active region.

The breakdown probability is the probability of a single carrier to initial the avalanche breakdown. It is an essential indicator of how quickly the avalanche current grows, leading to breakdown. Two simulation models are used for P_b are the analytical recurrence equation [10] and the Random Path Length (RPL) model [11], [12]. The RPL model is a Monte Carlo technique developed for avalanche

gain and excess noise simulation [11]. It was later extended by Tan *et al.* [12] for SPAD simulation (more details in section 3.5). Increasing applied bias will increase P_b, thus increasing the PDE. However, increasing P_b also increases DCR, making a trade-off between PDE and DCR. In addition, the abruptness of P_b is influenced by the carrier injection profile, the ionisation coefficients ratio and the avalanche width [10], [13]–[15]. Fig. 2.8 shows an example of P_b of Si and InP as a function of the overbias ratio, defined as $V_{over} = (V - V_{bd}) / V_{bd}$. For the same thickness, P_b of Si increases faster than P_b of InP because k is smaller in Si than in InP [10], [12], [16]. Moreover, despite the dead space effect, P_b increases faster with avalanche width [14], [17]. Therefore, a thicker avalanche width can achieve higher P_b for a given overbias voltage.

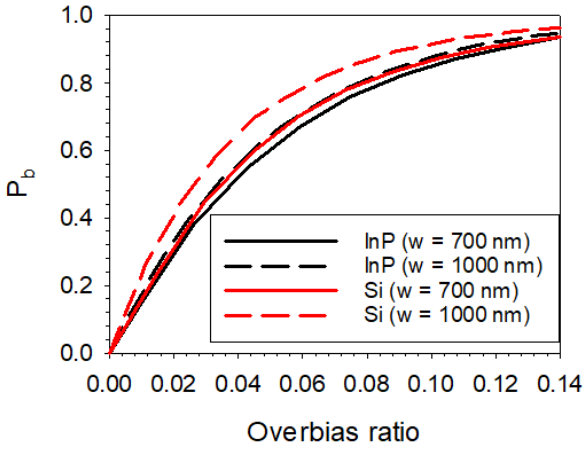

Fig. 2.8: Calculated P_b versus overbias ratio for an ideal p-i-n structure with avalanche width of 700 and 1000 nm by using reported ionisation coefficients (InP [18] and Si [19]), and RPL model [12].

2.2.3 Jitter

For a given SPAD and operating condition (i.e. external circuit), timing jitter is the uncertainty between photon arrival time and the avalanche signal produced time. It described how accurately the SPAD can determine the arrival time of a photon. The time needed to build up a measurable avalanche current fluctuates instead of being stable. Apart from the system, the jitter of the SPAD is mainly attributed to the variation in avalanche current build-up time. Simulation shows the jitter decreases with increasing overbias voltage because the spread of PDF of the breakdown time is decreases [12]. In this case, the material with a similar k tends to have a smaller jitter for a fixed P_b [12]. This is because larger k values provide more feedback carriers (electrons for pure electron injection and holes for pure hole injection) to build up the avalanche current, reducing the time it takes to breakdown.

Jitter can also be influenced by the position of photon absorption and the uniformity of the electric profile across a given SPAD [20]. For instance, if the carriers are absorbed at the edge where the electric field is different from the centre, the build-up time in avalanche current will be affected, increasing the uncertainty in time to breakdown. Ideally, the electric field within the avalanche and absorption regions

is uniform to achieve the smallest jitter. Moreover, it is possible to minimise the jitter by introducing a metal ring to cover the edge of devices to avoid injecting photon near device's edge [20].

2.2.4 Afterpulsing

During an avalanche event, millions of carriers flow through the SPAD, and some of them might be trapped by the deep-level traps linked to the defects within the semiconductor material [21]. When the SPAD is overbiased to detect the next photon, these trapped carriers could be released from the traps and trigger an avalanche breakdown in the absence of photons, causing an addition dark count. This phenomenon is called afterpulsing.

Another simple method to prevent the afterpulsing effect is to set a sufficient hold-off time before the SPAD is ready to detect the next photon [22]. During the hold-off time, the SPAD is inactive to allow the trapped carriers to recombine without causing an event. Hence, the hold-off time also known as dead time, and it limits the maximum operating frequency of the SPAD. It can vary from nanoseconds to microseconds and depend on the material quality. Increasing the operating temperature could decrease the de-trapping lifetime and reduce the afterpulsing effects. However, increasing temperature will also increase the primary DCR from thermal generation.

2.2.5 Quenching circuitry

Once an avalanche event is triggered by a dark or photo-generated carrier, the avalanche current must be quenched; otherwise, significant self-heating will damage the devices. Therefore, a SPAD must be operated with a quenching circuit.

Passive quenching

Passive quenching is the simplest circuit because it only requires a ballast resistor value in series with the SPAD, as illustrated in Fig. 2.9 (a). The ballast resistor typically has a value of 100's kΩ, and the sensing resistor has a 50 Ω for the impedance match. When the avalanche current flows through the ballast resistor, a voltage is induced across the ballast resistor, reducing the voltage across the SPAD around or below V_{bd}. Thus, the avalanche current is quenched. However, the highly resistive resistor will increase the time needed for SPAD to return to operating mode, limiting the switching speed and, hence, the detection speed. Example data from SPADs during recharging can be found in ref [23].

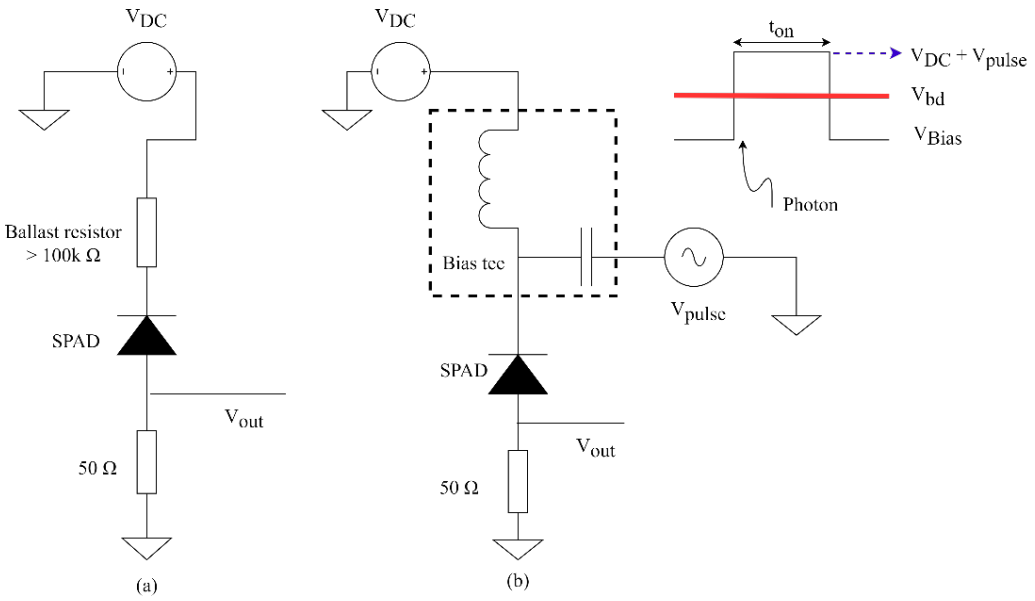

Fig. 2.9: Schematics of (a) a passive quenching circuit and (b) a gated quenching circuit.

Gated quenching

Gated quenching is commonly employed to supress a SPAD's DCR, but it is only suitable when the photon's arrival time is known. An example of the gated quenching method is illustrated in Fig. 2.9 (b). The SPAD is biased at V_{Bias} which is below V_{bd} by a constant V_{DC} until a pulse ('gate') is applied with the synchronisation of a photon. In this case, the pulse brings the voltage of SPAD above V_{bd}, allowing photon detection. After t_{on}, the pulse is withdrawn such that SPAD is operated below breakdown, thus avalanche current is quenched. The gated quenching can be used in combination with a ballast resistor to perform passive gated quenching for long AC pulses. Unfortunately, the use of the ballast still causes slow recharge. In addition, passive gated quenching requires a bias-tee whose capacitor will distort the pulse shape [23].

Since the distribution of dark count followed the Poisson distribution within the pulse, shortening the pulse width reduces the DCR [24], [25]. However, at the rising edge and falling edge of the gate signal, the charge and discharge of the SPAD's capacitance will generate transient current signal, given by

$$i = C\frac{dV}{dt}, \tag{2.15}$$

where C is the SPAD's capacitance and dV / dt is the rate of change of the gate. The transient can be several mV over 50 Ω resistor, overwhelming the weak avalanche signal. As a result, both measured DCR and SPDE may be underestimated, especially when a high repetition rate is used in the gate pulses. Common methods to extract the weak avalanche signal are discussed below.

In self-differencing technique [26], the weak avalanche is extracted by numerically subtracting the two output signals, which have identical responses, but one is shifted by a clock period. The InGaAs/InP

SPAD gating frequency based on self-differential technique can reach 1.25 GHz. Gigahertz clock of detection was also demonstrated (InGaAs/InP SPAD) with sine wave gating technique [27], [28]. The gate are sinusoidal waves instead of the rectangular pulses. Since the transient signal has the same frequency as the gate signal, the weak avalanche signal can be extracted using an appropriate bandpass filter. In addition, sine wave gating allows the pulse width to be very short, potentially reducing the afterpulsing [29].

Another method to cancel the transient is by introducing a dummy capacitor. The capacitor can in the form of an extra device (with the same resistance and capacitance as the device under test (DUT)) or a variable capacitor generate the same transients [23], [30]–[32]. The signal from a comparator or a differential amplifier then substrates the transient from the DUT's signal, leaving only the avalanche pulses.

Active quenching

The active quenching circuit will detect the growing avalanche current and directly bring the operating voltage of SPAD below V_{bd}. This method is more complicated than the other methods since extra feedback loops and delay circuits are needed [33]. When the feedback loops detect the avalanche current, it generates a signal to the controller logic, reducing the voltage below the breakdown. Unlike the rechanging process in passive quenching, a specific delay circuit is required to bring the SPAD back to active mode. In this case, the SPAD cannot be fully quenched unless the delay time exceeds the quenching time.

Moreover, the signal delay between the quenching circuit and devices must be optimised, as suggested by [22], [34]. In practice, if the standby time of the SPAD is long, its lifetime will be reduced because the SPAD is kept biasing above breakdown. Meanwhile, the DCR might be increased as thermal excitation, or tunnelling mechanisms are more likely to happen.

2.3 Review of SPADs

2.3.1 General design considerations

The different performance parameters between APDs and SPADs lead to different design considerations in terms of material and avalanche width. For example, a high-speed APD requires thin avalanche and absorption regions (< 1.0 μm) to reduce transit time whilst achieving acceptable avalanche gain and responsivity [35]–[37]. Avalanche materials with dissimilar α and β are preferred in APD designs for low excess noise [3]. In contrast, thick avalanche and absorption regions (> 1.0 μm) are needed in SPAD to maximise the SPDE and minimise tunnelling current to manage DCR. Although materials with dissimilar α and β are predicted to have higher P_b for a given bias, they also require more

time to build up the avalanche current and produce larger timing jitter [12], [15], compared to materials with similar α and β. Therefore, SPADs do not necessarily utilise avalanche materials with dissimilar α and β.

Despite the differences mentioned above, APDs and SPADs do have some common design considerations regarding wafer and device designs as described below.

Wafer structures

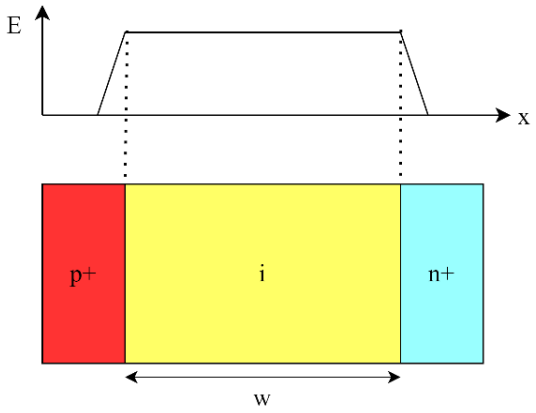

Fig. 2.10: Example of a p-i-n device and its electric field profile.

A p-i-n or n-i-p structure is the simplest possible wafer structure of APDs and SPADs, as illustrated in Fig. 2.10. The avalanche multiplication process mainly takes place in the intrinsic region known as the avalanche region, where high reverse electric field exists. This structure typically utilised a single homogenous material where the photon absorption and impact ionisation happened at the same place. Since the carrier's injection profiles (pure electron/hole) affect the performance, as discussed in section 2.1.2, choosing p-i-n or n-i-p depends on the ionisation coefficient with the same illumination side. Since $\beta > \alpha$ in InP, hole injection into the avalanche region is preferred over electron injection to produce the best possible $F(M)$ characteristics for a given InP avalanche width. Hence InP APD designs should ensure the incoming photons are absorbed primarily in the n-layer, if a simple p-i-n or n-i-p structure is used.

As discussed in section 1.3, InGaAs is promising for optical detection at 1550 nm wavelength. However, since the bandgap of InGaAs is relatively small (E_g = 0.75 eV), undesirable tunnelling current will dominate an InGaAs APD dark current when a large reverse electric field is applied, limiting the usable avalanche gain. Hence, an APD/SPAD made with InGaAs avalanche region is unlikely to offer good performance.

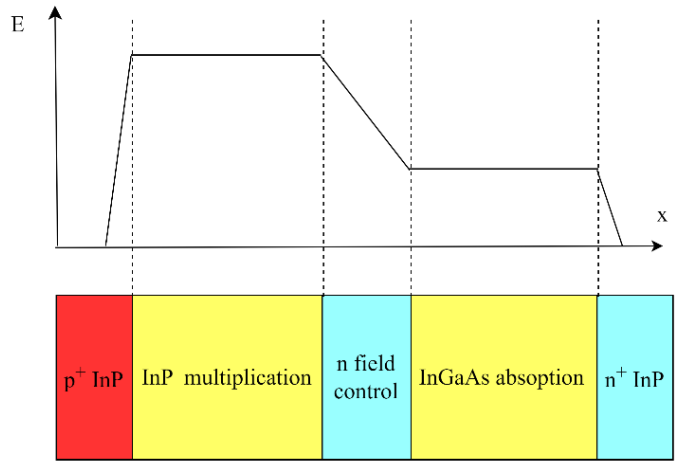

Fig. 2.11: Example of a InGaAs/InP SAM device and its electric field profile.

Separate Absorption and Multiplication (SAM) structure, first applied to near infrared APDs in 1979 [38], is commonly used to overcome this issue. An example of InGaAs/InP SAM APD is illustrated in Fig. 2.11. The narrow bandgap InGaAs absorber is subjected to low electric field, preventing high tunnelling current. The wide bandgap InP avalanche region is subjected to high electric field to produce avalanche gain without significant tunnelling current. The large difference in electric fields in the absorption and multiplication region is achieved by a charge sheet with a carefully chosen doping density and thickness. There is also one or more InGaAsP grading layers between the InGaAs absorption and InP charge sheet layers (introduced in [39]). Its purpose is to minimise holes pileup at the InGaAs/InP heterointerface, reducing loss of photo-generated carriers for both APDs and SPADs, as shown in Fig. 2.12. For SPADs, it can also reduce charge persistence effect and hence timing jitter [20], [40], [41].

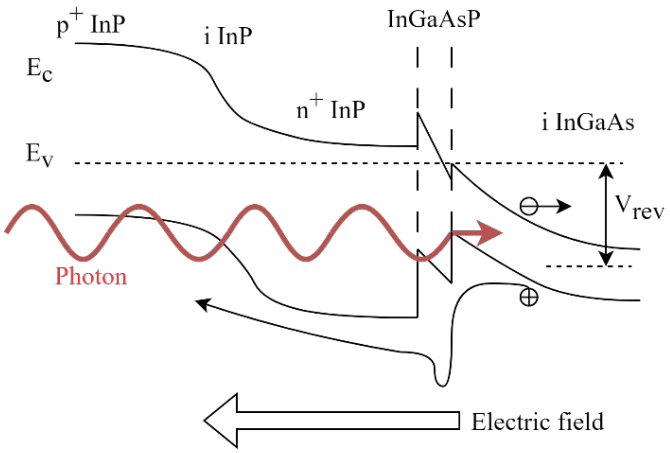

Fig. 2.12: Energy band diagram of typical InGaAs/InP SAM APD under reverse bias condition.

Device structures

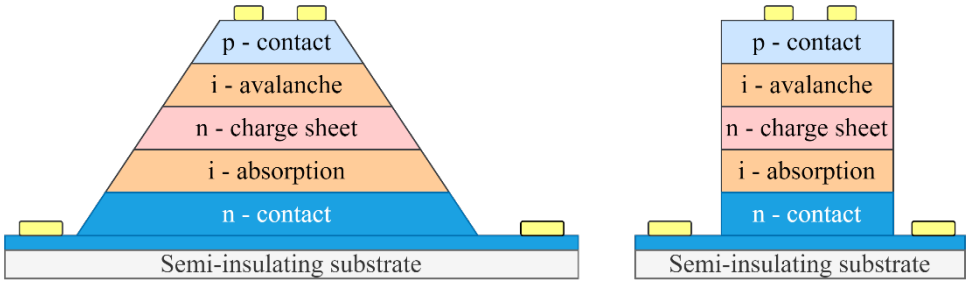

Fig. 2.13: Example of a mesa p-i-n-i-p SAM structure via (left) wet and (right) dry etching process.

There are two device structures of APDs and SPADs, namely mesa and planar. An example of mesa APD is illustrated in Fig. 2.13. To produce a mesa APD/SPAD, the full wafer structure is completed using wafer growth, before using dry or wet etching to remove unwanted semiconductor materials, leaving behind the isolated mesa device. Dry etching is an anisotropic process, while wet etching is an isotropic process which will lead to a reduction of the devices' radii. Depending on the etching selectivity, more complicated material structures might require multiple etching steps. The wafer growth allows fine control of each layer's doping density and thickness, simplifying the fabrication process. There is also more flexibility for devices' geometry design in mesa devices.

However, exposed mesa sidewalls can cause local high electric field (hotspots), increasing the surface leakage current and the chance of PEB [42]. Furthermore, the locally enhanced photocurrent results from the local high field yielded a non-uniform gain, which increases the excess noise of APDs [31] or the jitter of SPAD [43]. Passivation is required to prevent the device's surface from being contaminated or damaged during the fabrication or operation, which degrades the device's reliability [44].

Multiple mesa structures were developed to minimise the issues mentioned. The early attempt was developed for Si APDs [45] but not used in current commercial or research Si APDs. It has been adopted for SiC APDs [46]. More recently, an InGaAs/InAlAs APD in triple mesa structure was developed to suppress leakage current and PEB [47]. The smallest mesa contains a contact layer. The second larger mesa contains an edge-field buffer layer and a field control layer. The largest mesa contains the remaining layers (e.g. avalanche and absorption layer). The high electric field was confined within the central region (the smallest mesa), thus reducing the surface leakage current and preventing the PEB.

Unlike a simple mesa device, a planar device cannot easily be modified because it is defined by dopant implantation (e.g. Si SPADs) or diffusion (InP SPADs), leading to a more complicated process than a mesa. The passivation on the surface further protects the devices, increasing their reliability and lifetime [48]. The planar structure offers more tolerance to surface leakage current for SPAD than APD

[24], because the high field in the avalanche region is kept away from the surface, minimising risk of contaminations.

On the other hand, the planar device might suffer from PEB due to the curvature effect after dopant implantation or diffusion process (more details in later section). To reduce cross-talk between planar SPADs devices, especially in closely-packed SPADs in an array, etching is often used to better isolate the devices [44], [49]. Although there are more fabrication steps in planar APDs than in mesa APDs, commercial Si and InGaAs/InP APDs are manufactured in large quantities. Both are used in a wide range of applications.

2.3.2 InGaAs / InP based

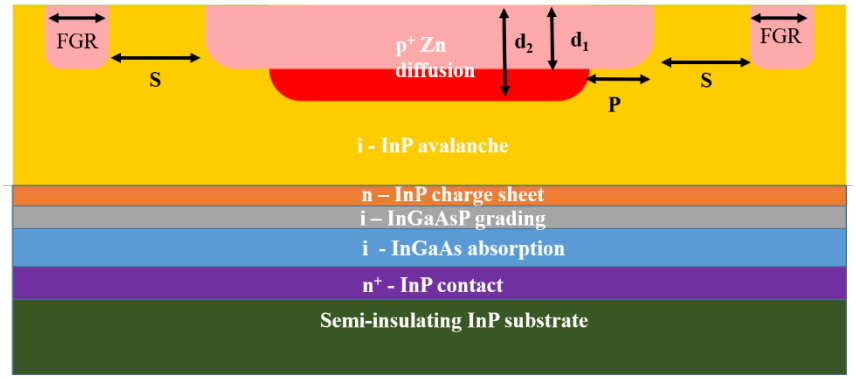

Fig. 2.14: Example of a planar InGaAs/InP SAM APD with double Zn diffusion and FGRs. (In this work) the depth of shallow and deep Zn diffusion are noted as d_1 and d_2, respectively. The spacing between shallow diffusion and floating guard ring is noted as S while the extension between shallow and deep diffusion is noted as P.

InGaAs / InP APDs

InGaAs/InP APDs are currently the dominant optical detector in metro/long-haul optical fibre communication's receiver modules, thanks to their high sensitivity and gain-bandwidth product [50]–[52]. The first report of using InGaAs/InP APDs (mesa devices) for single photon detection at 1300 nm was in 1984 [53]. However, research and commercialisation efforts were concentrated on InGaAs/InP APDs only, with research efforts InGaAs/InP SPADs only restarted in late-1990s.

Commercial InGaAs/InP APDs adopt the planar structure, as shown in Fig. 2.14. The devices' active region is defined by Zn diffusion into an undoped InP layer and hence far away from the semiconductor surface. Due to the curvature effect, the electric field at the active region's periphery tends to be significantly higher than those in the active region, resulting in a PEB [54]. Since PEB is highly detrimental to APD operations [55], other design features were introduced to planar APDs to suppress the electric field at the junction periphery. These are (i) a modified Zn diffusion process to increase the

radius of curvature and (ii) introduced floating guard rings (FGRs) to further reduce the electric field at the active region's periphery.

For (i), this can be implemented using double Zn diffusion [48], a combination of etching and a single Zn diffusion process [56] or more complicated selective area growth (SAG) [57]. Double Zn diffusion is the dominant method and used in commercial APDs. Ref [48] reported design rules for the double Zn diffusion depths (**d_1 > 1.5 μm; d_2 = 2.4 - 2.7 μm; (d_2 – d_1) = 0.5 - 1.5 μm**) and spacing of FGRs (**1.0 to 3.0 μm**). These were extracted from simulated electric field profile of planar APDs with FGRs of various designs, assuming constant Zn profiles within the Zn-diffused regions were extracted from simulations. However, there was no experimental validation in [48] nor in subsequent planar APD studies [58]–[61].

Experimental studies on FGR effectiveness were reported by Cho *et al.* [58] in 2000 and Wei *et al.* [59] in 2002. Ref [58] investigated FGR spacing (from the edge of central junctions) from 3.5 to 5.0 μm. Based on photocurrent scans across the APDs, they concluded that 4.0 μm as their optimal design. However, it is unclear if the optimum FGR spacing is applicable to other planar InGaAs/InP APD designs (e.g. with different Zn diffusion depths). Although Ref [59] presented electric field simulation results for design with varying FGR spacing (1.0 to 3.0 μm), the experimental data only covered designs with FGR spacing of 1.0 μm. Hence no design rules on FGR spacing were available from ref [59].

A series of 2-D electric field simulations for planar InGaAs/InP APDs with FGRs were reported in 2018 [60]. However their APD designs differed greatly from the practical planar APDs, with very small active region (1.0 μm diameter) and FGR spacing (0.3 – 0.8 μm, significantly smaller than the recommended range from ref [48]). Hence, their recommended range of FGR spacing, 0.3 – 0.8 μm, may not apply to typical planar APDs.

Recently, Zhang *et al.* [61] compared experimental breakdown voltages of planar APDs with different FGR spacing. However, the APDs were produced using a single Zn diffusion process and without recess etching, so likely to suffer from edge breakdowns. Indeed, their reported breakdown voltages of 32-35 V are far lower than the expected values (~ 54 V from the experimental value of [62] and ~58.1 V from calculations using ionisation coefficients of InP [18]). Thus, their reported FGR spacing is unlikely to be relevant to typical planar APDs.

Overall, none of these studies [48], [58]–[61] demonstrated their guard ring and Zn diffusion design through both simulation and experimental data. In addition, previous simulation studies assumed either constant doping or error function for the Zn diffused regions instead of actual Zn doping profiles.

InGaAs / InP SPADs

In late-1990s, research on InGaAs/InP SPADs focused on characterisation of commercial InGaAs/InP APDs (e.g. from Epitaxx [63] and Fujitsu [64]) in Geiger mode [65], [66]. The first reports of custom-designed InGaAs/InP SPADs appeared in 2000s [40], [67]–[69]. In 2006, Pellegrini *et al.* [40] reported InGaAs/InP SPADs with 10 % SPDE at 200 K. The SPADs were fabricated using double Zn diffusion and two FGRs to suppress PEB, as implemented in APDs of ref [48], but there was no details of the Zn diffusion depths or FGR design. Their SPAD has a noise equivalent power of 6×10^{-16} $W/\sqrt{Hz}$ at 200 K, which is worse than the performance of Epitaxx [63] but better than Fujitsu [64] linear mode APDs. Later, more comprehensive studies and design criteria for InGaAs/InP SPADs were reported by Princeton Lightwave [24], [68] and Politecnico di Milano (Polimi) group [69].

The SPADs in ref [68] also utilised double Zn diffusion (so that the breakdown voltage of deep diffusion is smaller than that of shallow diffusion) to suppress the PEB, but they did not incorporate FGR(s). Further InGaAs/InP SPADs with double Zn diffusion and no FGR were demonstrated (with a SPDE of up to 30 %) in [43]. However, these SPADs and the commercial SPADs (from [68], also without FGR) exhibited non-uniformity in electric field across the active region, worsening the timing jitter [43].

Subsequent SPADs with lower jitter (below 90 ps at 225 K) and more uniform electric field across the active region were reported in [70] by the same group. The SPADs showed a good SPDE of over 25 % at 1550 nm and DCR of 100 kcps. The changes included addition of FGRs and modified Zn diffusion profile. For the latter, the design ensured (i) a minimum voltage difference of 10 V between deep and shallow diffusion by varying the diffusion depths, and (ii) < 3 % variation in electric field within the active region by varying P [70]. However, from 2014 onwards, Polimi's group reverted to SPADs without FGRs that still exhibit uniform detection efficiency within the SPAD's active area (e.g. [41] and [71]).

It is possible for SPADs without FGRs and double Zn diffusion to exhibit uniform electric fields within their active areas. Using the SAG of InP directly above the active region, an InGaAs/InP SPAD fabricated using single Zn diffusion and without FGR was reported [72]. It exhibited a SPDE of up to 43 % at 225 K and a DCR of 55 kcps. Another example is ref [73], which reported an InGaAs/InP SPAD produced using a combination of recess etching and single Zn diffusion process to create the active region (as used for APD in [56]), though a single FGR was still employed. However, both the SAG process and recess etching introduce considerable complexities and costs to the SPAD fabrication, which is already more demanding than APD fabrication.

However, most SPAD researchers (e.g. [31], [32], [74], [75]) still used the FGR and double Zn diffusion designs from ref [48] and [40] to suppress PEB. Therefore it is unclear if FGRs and double Zn diffusions are essential to suppress PEB and reduce dark count in InGaAs/InP SPADs. In this thesis, **a study to**

evaluate the effectiveness of FGRs and double Zn diffusion profiles on SPAD's SPDE and DCR was carried out. The absence or presence of FGR has implication on the fill-factor of individual SPADs and minimum pitch for SPAD arrays.

Performance of InGaAs / InP SPADs

A record SPDE of 55% at 1550 nm was reported by Comandar *et al.* [76]. The SPAD was gated at 1 GHz at room temperature with an afterpulsing probability of 10.2 % when a dead time was set to 10 ns. Later, Fang *et al.* [75] obtained a PDE up to 60 % at 1550 nm, but they stated that a PDE of 40 % with 3 kcps and a probability of 5.5 % is more appropriate for practical use. In [75], they used double Zn diffusion and an FGR to suppress the PEB, with an additional dielectric metal reflection layer to increase the absorption efficiency. Zhang *et al.* [31] further optimised the reflector by combining the metal layer with a SiO_2/TiO_2 distributed Bragg reflector to increase the absorption efficiency, achieving a high SPDE of 30 % with a low DCR of 665 cps at 233 K. Furthermore, the low DCR also contributed by adding another FGR to suppress further the edge field around periphery region [31]. Although the depth difference of 0.4 µm is smaller than the suggested minimum of 0.5 µm in [48], He *et al.* [32] demonstrated that their single FGR SPAD has a SPDE of 55.4 % with a DCR of 43.8 kcps at 247 K, in the absence of PEB.

2.3.3 InGaAs / $In_{0.52}Al_{0.48}As$ SPAD

$In_{0.52}Al_{0.48}As$ (referred to as InAlAs hereafter) is a ternary alloy with a larger bandgap of 1.45 eV but the same lattice constant as InP [77]. It is becoming popular and is considered to replace InP because of the lower tunnelling effect at higher fields. Moreover, [78]–[80] reported and confirmed that InAlAs has a smaller temperature coefficient of breakdown voltage C_{bd} than InP, which means the breakdown voltage of InAlAs is less sensitive to temperature than InP. This is believed to be because the alloy scattering in InAlAs is temperature-independent, reducing the sensitivity of the ionisation coefficient with temperature [81]. Another advantage to choosing InAlAs for Geiger mode operation is the large dissimilar ionisation coefficient [82], [83]. As discussed in Section 2.2.2, a smaller k of InAlAs is predicted to have a more rapid increase in P_b than InP, allowing InAlAs to achieve higher SPDE before the DCR becomes significant [15]. It is noted that the material with a larger k is predicted to have better timing characteristics because it has more carrier feedback to build up the avalanche current than the material with a smaller k [12], [15].

The first InGaAs/InAlAs SPAD reported by Karve *et al.* [84] exhibited SPDE of 16 % at 130 K. Zhao *et al.* [85] demonstrated a self-quenching and self-recovering InGaAs/InAlAs SPADs with a SPDE of 11.5 % and a DCR of 3.3 Mcps at 160 K without the need of external quenching circuitry. After optimising the structure to reduce the tunnelling effect in [86], Meng *et al.* improved their mesa InGaAs/InAlAs SPAD with a SPDE of 26 % and a DCR of 100 Mcps at 210 K. Their SPAD exhibits a

jitter of 70 ps, comparable to state InP-based SPADs in 2016 [55], [87]. Recently, InGaAs/InAlAs SPAD with a SPDE of 35 % and a DCR of 33 Mcps at 240 K was achieved by implementing a tripper mesa structure to suppress the surface leakage current and premature breakdown [88]. Furthermore, Lee *et al.* [89] reported that their SPDE exceeded 60 % at 1310 nm despite the high DCR. Instead of using mesa structure, Tian *et al.* [90] demonstrated a planar InGaAs/InAlAs SPAD, which exhibits a SPDE of 10.4 % and DCR of 3.1 Mcps at room temperature.

Although the avalanche properties of InAlAs is better than InP, currently reported InAlAs/InGaAs SPADs are not as good as expected compared to InGaAs/InP SPADs. In terms of manufacture, InAlAs is less mature than InP, so the material quality of InAlAs tends to be poor, increasing DCR and afterpulsing probability. In addition, the aluminium composition requires extra protection to prevent oxidisation, which will increase the dark current and degrade the devices.

2.3.4 Ge-on-Si SPAD

Ge has an indirect bandgap of 0.8 eV with a cut-off wavelength of 1550 nm (detection wavelength up to 1600 nm at room temperature). Hence Ge is a suitable absorption material for 1550 nm wavelength SPADs. However, Ge SPADs require cooling to cryogenic temperature (e.g., 100 K) to suppress band-to-band tunnelling current which leads to high DCR [91]. The reduction in temperature reduces the bandgap, reducing the cut-off wavelength of Ge to 1450 nm, severely limiting the detection efficiency of Ge SPAD at 1550 nm wavelength. By adopting the SAM structure, Loudon *et al.* reported the first Ge/Si SPAD with a DCR of 100 kcps at 200 K [92]. However, the large lattice mismatch at the Ge/Si interface led to an extremely low SPDE (0.01 % at 1210 nm). For photon absorption, the wafer used $Si_{0.7}/Ge_{0.3}/Si$ multiple quantum wells rather than bulk Ge, so the overall thickness of Ge was only 300 nm.

With the development of high-quality epitaxial Ge layers on Si substrates, Ge-based SPAD is back in the spotlight, especially when it incorporates the modern silicon foundry fabrication process. It is called Ge-on-Si SPADs with a μm-dimensioned thickness Ge absorber to guarantee the absorption efficiency. Lu *et al.* [28] reported the first mesa Ge-on-Si SPADs with a DCR of more than 100 Mcps at 200 K (comparable to the DCR value from [92]) and an SPDE of 14 % at 1310 nm. Later, Ge-on-Si SPADs adopted different structures (e.g. planar [93], [94] and waveguide-coupled [95]) to mitigate the DCR while maintaining high SPDE, as shown in Fig. 2.15.

Despite their high DCR compared to InGaAs/InP SPADs, Ge-on-Si SPADs were demonstrated to have lower afterpulsing probability and higher maximum count rate under the same operation condition that is promising to be used for high-speed QKD and integration in standard silicon photonics [37], [93], [96], [97]. However, fabrication of Ge-on-Si SPADs remain significantly more complex than other infrared SPADs. Their weak absorption at 1550 nm wavelength fundamentally limit their SPDE values.

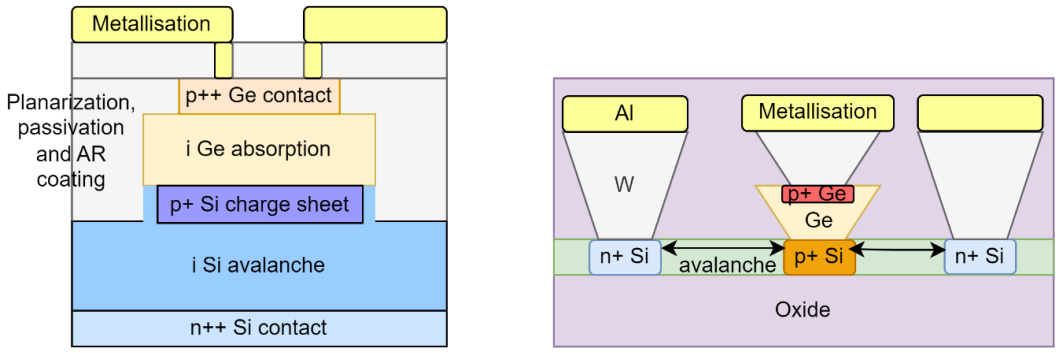

Fig. 2.15: Schematic of the cross-section of (left) planar and (right) waveguide structure Ge-on-Si SPADs reported in [93] and [95], respectively.

2.4 Other technologies for single photon detection

In addition to SPADs, the focus of this work (and literature review), there are other devices for single photon detection. These notable technologies are discussed below.

2.4.1 Photomultiplier tubes (PMTs)

The earliest device that demonstrated light detection at single photon level was PMT. PMT is an electric vacuum device that uses the photoelectric effect to detect a single photon. It is mainly composed of a photocathode, an anode and multiple dynodes. The photocathode coated with photoemissive material will absorb the incident photon and generate an electron due to the photoelectric effect. This photoelectron will be accelerated under a significantly high electric field and collide with the dynodes. A much larger gain (10^6-10^7) can be obtained following further electron generation and collision. However, the high gain of the PMT requires a very large operating voltage, which sometimes exceeds 1 kV. The need for a vacuum environment and glass tubes makes PMTs bulky and very fragile. Moreover, there is a lack of suitable photocathode material absorb IR, severely limiting the quantum efficiency of PMT in the NIR and MIR spectral ranges to < 2.5 % [98], [99].

The slow temporal response of PMT is another disadvantage. The temporal response of PMT is characterised by the Transit Time Spread (TTS), which is the time difference between photon arrival and the production of measurable current at anodes. The Full-Width at Half-Maximum (FWHM) represents the TTS, whose value is in nanosecond scale depending on the structure, dynode shape and number of stages. A structure called hybrid PMT (HMPT) was developed to reduce the jitter by replacing the dynodes with an avalanche diode [100], [101]. In HMPTs, there is still a bombardment region for electrons to provide the largest part of the gain with an additional gain from the avalanche diode. The commercial HMPTs from Hamamatsu have comparable gain (1.2×10^5) to standard PMTs and a significantly low TTS of 20 – 150 ps for visible wavelength detection [101].

2.4.2 Superconducting nanowires single photon detectors (SNSPDs)

The typical structure of the SNSPD is made of ultra-thin, low-temperature superconducting material such as niobium nitride (NbN) [102], [103]. There is a critical temperature and biased current for SNSPD to become 'superconductive'. The operating temperature of the SNSPDs is just below their critical temperature and is biased with a DC, which is slightly lower than its critical current. When there is an incident photon, it will break up the Cooper electron pair, forming a 'hot spot' with weak resistance. The local current density will keep increasing until it exceeds the critical current density if the hot spot is sufficiently large. Finally, a resistive region will inform across the entire nanowire, causing a sudden drop of the bias current, which is then sensed by a readout circuit. The main advantage of SNSPDs is their ultra-fast response and almost negligible dark count. They also offer shorter recovery time (in picosecond scale) and smaller timing jitter than SPADs. However, the critical temperature normally ranges from 0.8 to 5 K, requiring liquid helium cryostats, resulting in significant extra cost, weight and overall dimension.

In 2001, Gol'tsman *et al.* first demonstrated that SNSPD can detect a single photon with a detection efficiency of 20 % at 810 nm wavelength. Since then, many researchers expanded the detection wavelength from mid-infrared (MIR) to UV by using different superconducting films, including WSi [104], [105] and MoSi [106]. In addition, the detection efficiency of SNSPD at 1550 nm wavelength increased from 3 % at the beginning to more than 93 % [107], [108]. A new record of detection efficiency at 1550 nm is 98 %, as reported by Reddy *et al.* in 2020 [109]. Their SNSPD is based on MoSi, and the device's vertical optical stack design was optimised to prevent the theoretical loss of photons through mechanisms such as scattering and dielectric absorption. Furthermore, a high-speed SNSPD based on NBN was demonstrated to achieve sub-picosecond jitter for visible and 1550 nm wavelength [110].

2.4.3 Up-conversion single photon detectors (UCSPDs)

Although the Si SPAD has poor performance at wavelengths longer than 1000 nm, the excellent behaviour at shorter wavelengths and huge manufacturing base make it attractive to be extended the detection beyond the limit, especially for high-speed single photon detection [111], [112]. An up-conversion single photon detector is used for 1550 nm wavelength detection but based on Si SPAD. This is achieved by the use of non-linear optics before the Si SPAD. The non-linear optics medium utilised sum frequency generation can convert photons at 1550 nm to a shorter wavelength (< 1000 nm). Finally, a photon at the telecom band can be detected by a Si SPAD.

The single photon quantum state frequency conversion was first theoretically and experimentally demonstrated by Kumar *et al.* in 1990 and 1992 [113], [114], respectively. They used Potassium titanyl phosphate (KTP) to convert photons from 1064 nm to visible 523 nm. However, the observation was

weak due to the low conversion efficiency of KTP. Later, Albota and Wong found that periodically poled lithium niobate (PPLN) has a higher non-linear property than KTP, which can achieve a conversion efficiency of 90 % [115]. Thus, the PPLN is widely adopted in UCSPD. However, the pump laser will introduce an extra noise into the system. Utilising a long wavelength laser pump and a narrow band filtering based on volume Bragg grating, Shentu *et al.* reported a low noise UCSPD with a detection efficiency of 30 % and a DCR of 100 cps [116]. Furthermore, their group implemented this low-noise UCSPD to overcome the noise from sunlight that a free space QKD system can achieve over 53 km during the day [117].

2.4.4 Comparison

Various single detectors are compared in Table 2.1. PMTs have done an excellent job in specific fields [121]. However, they are beaten by the other detectors for NIR detection. Although the SNSPDs show the best performance among those of comparison, their operation temperature is typically below 4 K, which is unsuitable for most applications. In contrast, the SPADs can operate at temperatures reached by thermoelectric coolers whilst providing acceptable dark count and quantum efficiency.

Despite the good performance of Si SPADs, the UCSPDs technique requires a delicate design to cooperate with the frequency conversion and the detection part. In general, Ge-on-Si and InGaAs/InAlAs SPADs exhibit a higher dark count cf. InGaAs/InP SPADs due to the less mature growth technique. Apart from material growth, they still require a complicated design to mitigate the DCR further while maintaining sufficient high SPDE; examples of the complicated design for Ge-on-Si SPAD are demonstrated in Fig. 2.15. Overall, InGaAs/InP SPADs are the most practical single photon detectors for NIR detection. This thesis focuses on the design and fabrication of InGaAs/InP SPADs, specifically on the effectiveness of FGRs and double Zn diffusion profiles on SPAD's SPDE and DCR.

Table 2.1 Comparison of single photon detectors.

Detector	Ref	Material	Temp. (K)	λ (nm)	SPDE (%)	DCR (cps)	Jitter (ps)
HPMT	[101]	GaAsP	300	520	45	100	90
NIR-PMT	[99]	InGaAs/InP	200	1500	2	0.2 M	1500
SNSPD	[108]	WSi	0.12 - 2	1550	93	1 k	150
	[118]	NbN	0.9		78	158	<50
	[109]	MoSi	0.72 - 0.78		98	N.A.	N.A.
UCSPD	[116]	Si	290	1550	28.6	100	N.A.
	[119]		290		36	90	450
SPAD	[93]	Ge-on-Si	125	1310	38.0	2 M	310
	[94]		165		25.0	< 1 M	204
	[68]	InGaAs/InP	225	1550	> 20.0	< 10 k	N.A.
	[76]		293		50.0	< 416.5 k	N.A.
	[75]		253		40.0	14.5 k	N.A.
	[41]		255		30.0	1.37 k	84
	[120]		293		20.9	5.1 k	NA.
	[88]	InGaAs/InAlAs	240		35.0	33 M	N.A.
	[90]		290		10.4	20.4 M	170

2.4 References

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Chapter 3: Methodology

3.1 Current–Voltage measurements

Current-voltage (I-V) measurements are the first and the most crucial characterisation technique to identify the electric properties of the APDs and SPADs. They were performed using the HP 4140B Picoammeter, which can measure the current level down to the picoamp level or the Keithley 236 Source-Measure Unit (SMU) in a dark environment.

3.1.1 Forward bias I-V measurements

Although both APD and SPAD operated at reverse bias, the forward I-V characteristics are still essential because they provide information on series resistance and the nature of the current. An example is presented in Fig. 3.1.

The current nature can be extracted and described by the ideality factor from fitting Shockley's ideal diode equation:

$$I_F(V) = I_0 \left[\exp\left(\frac{qV}{nk_bT}\right) - 1\right], \tag{3.1}$$

where I_0 is the forward current at 0 V referred to as saturation current, V is the total bias applied to the devices, k_b is Boltzmann's constant and n is the ideality factor that is the typical value between 1 and 2. If n is close to 1, the current is dominated by diffusion current, whereas the generation and recombination current is dominant when n is close to 2.

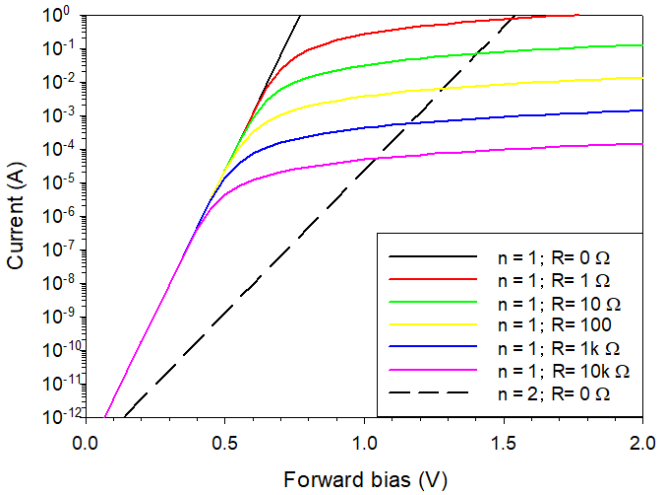

Fig. 3.1: Calculated forward current-voltage characteristics of diodes with a given I_0 and ideality factor of 1 (solid line) for various series resistance and 2 (dash line) for zero resistance.

The increase of forward current will be reduced due to the voltage drop on the series resistance, which can be obtained by fitting measured forward I-V data with the equation given by

$$I_F(V) = I_0\left[\exp\left(\frac{qV - IR}{nk_bT}\right) - 1\right]. \tag{3.2}$$

However, solving the equation can be tricky since both *I* term appear on both sides. There are two methods to solve this equation. One approach is using Eqn. (3.1) to find the ideality factor first, then substitute the *n* and the measured I-V data into Eqn. (3.2), adjusting the *R* until they fit. Another method utilised the Lamber W function, which is the inverse of $f(w) = we^w$ to rearrange the equation Eqn. (3.2):

$$I_F(V) = \frac{nk_bT}{qR}W_0\left[\frac{qI_0R}{nk_bT}\exp\left(\frac{q}{nk_bT}(I_sR + V)\right)\right] - I_0\,, \tag{3.3}$$

where $W_0()$ is the zeroth solution to the Lambert W function.

3.1.2 Reverse bias I-V measurements

Dark current level can be seen clearly in reverse I-V data such that the device's performance is initially identified. Dark current can consist of bulk and surface leakage currents. The bulk current will depend on the device's cross-sectional area, so it will scale with the device's area when it dominates the dark current. If surface leakage current is the dominant, the dark current will scale with the perimeter (especially for mesa structure). Insufficient passivation on the surface can increase the surface leakage current. Moreover, an undesired surface state formed at the etched sidewall in mesa design can result in a high dark current, limiting the device's performance. Hence, it is important to optimise the etching process and implement a proper passivation layer.

The bulk dark current consists of the diffusion current I_{diff}, generation and recombination current I_{GR} and band-to-band tunnelling current I_{tun}, given by the following equation:

$$I_{diff} = I_0\left[\exp\left(\frac{qV}{k_bT}\right) - 1\right], \tag{3.4}$$

$$I_{GR} = \frac{qn_iAW}{\tau_{eff}}, \tag{3.5}$$

and

$$I_{tunn} = \frac{(2m^*)^{1/2}q^3EVA}{4\pi^2\hbar^2{E_g}^{1/2}}\exp\left(-\frac{\alpha_T(2m^*)^{\frac{1}{2}}E_g^{\frac{3}{2}}}{qE\hbar}\right), \tag{3.6}$$

where n_i is the intrinsic carrier concentration, A is the device's area, τ_{eff} is the effective carrier lifetime, m^* is the electron effective mass, $\hbar$ is the reduced Plank's constant, and α_T is a constant on the order of unity and dependent on the shape of the potential barrier. At the low field, dark current is mainly

dominated by I_{diff} and $I_{GR,}$ while either I_{tunn} or avalanche dominates the current at the high field region. Unlike surface leakage current, the bulk dark current can be reduced by dropping the operating temperature. However, if I_{tunn} dominates the current at the high field, the dark current cannot drop as I_{tunn} is not sensitive to temperature. Thus, it should be avoided.

V_{bd} is another indication from reverse I-V measurements. As mentioned in Section 2.1.2, the breakdown is contributed by the avalanche and tunnelling process. If the avalanche process dominates the breakdown, the current will increase sharply at V_{bd}. In contrast, the sharpness of the current increase will reduce when the tunnelling become significant. The dominance of tunnelling is detrimental to APDs, especially for SPADs. Furthermore, devices should have a consistent breakdown voltage regardless of size from the same wafer. A large spread of breakdown voltage indicates devices are suffering from edge breakdown or having a non-uniform electric profiles. Edge breakdown is more likely to happen in mesa devices that are caused by etching process whereas the non-uniform electric profiles tend to because of the poor growth quality.

Fig. 3.2 presents typical reverse I-V data of InAlAs p-i-n APD. The test devices were fabricated by using the research group's mask set which contains 4 different sizes of the circular mesa (25, 50, 100, 200 µm radius devices or 35, 60, 110, and 210 µm radius devices depending on which etching pattern was used). A consistent avalanche breakdown voltage is observed in Fig. 3.2 (a), where the dark current rapidly increase at -44 V. The dark current of the tested devices is dominated by the surface leakage current as indicated in Fig. 3.2 (c).

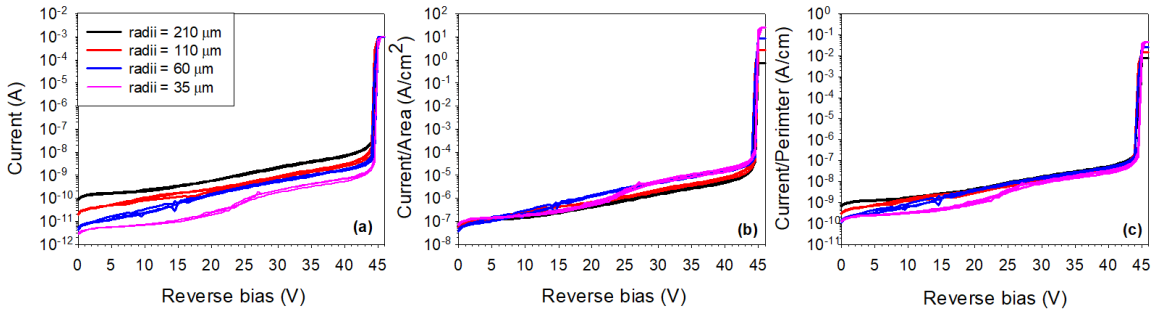

Fig. 3.2: Example of (a) experimental reverse dark I-V (b) normalised dark current with device's area (c) normalised dark current with device's perimeter.

3.2 Capacitance-Voltage measurements

Capacitance-Voltage (C-V) measurements were performed using an HP 4725 LCR meter. The LCR meter will apply a reverse DC bias voltage on the diode with a superimposed sinusoidal AC test signal whose peak-to-peak value is smaller than the DC bias to avoid measurement errors. The instrument has two RC models to extract the measured impendence. The series model should be used if both series and shut resistance are high. The other most commonly used is the parallel model, which is applicable when the series resistance of a diode is much smaller than its parallel shunt resistance. The LCR meter also

provides the phase angle to monitor whether the diode capacitance dominates the impedance. Ideally, this phase angle should be close to 90°. It is acceptable to have a phase angle between 80 and 90, otherwise, the impedance could be dominated by the resistance or inductance, resulting in an inaccurate result.

The relationship between capacitance and depletion width is demonstrated by

$$C(V) = \frac{\varepsilon_0 \varepsilon_r A}{w(V)}, \tag{3.6}$$

where *w(V)* is the voltage dependant depletion width, *A* is the diode's area, ε is the relative permittivity of the dielectric. A typical C-V curve for a SAM InGaAs/InAlAs APD is shown in Fig. 3.3 (left). At ~ -30 V, the capacitance become nearly constant. This voltage is called puchthrough voltage (V_p), when the InGaAs absorber is fully depleted. In Fig. 3.3 (right), the C-V data is normalised with diode's area after the radius correction. This is attributed to the radii of the devices can be reduced by the isotropic (wet) etching process. Hence, the C-V data would not scale with area until the reduction of radii is included.

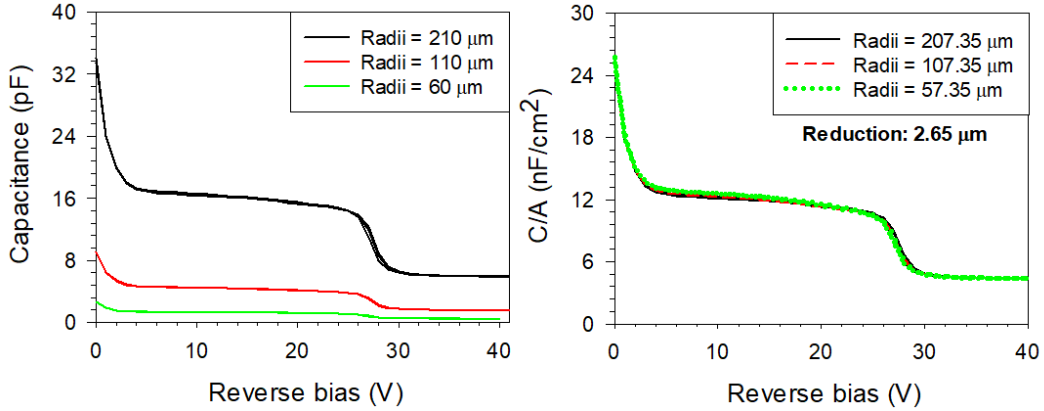

Fig. 3.3: (Left) measured C-V data from devices with different radius. (Right) normalised capacitance with area after radii correction.

The expected device's electric field profile forms the layer thickness and doping concentration are calculated by solving one dimensional Poisson's equation, which is given by

$$\frac{\partial E}{\partial x} = \frac{q N_{dop}}{\varepsilon_0 \varepsilon_r}, \tag{3.7}$$

where *E* is the electric field and N_{dop} is the doping concentration of the region. These data can then be used to simulated the C-V data using Eqn. (3.6). In this model, doping concentration and the depletion width are adjustable parameters that are used to modify the simulated C-V data until it agrees with the experimental data.

Ideally, the depletion width and the doping profile of the devices should be roughly the same as the request for wafer growth. Fitting the experimental and expected C-V data can check those variations.

To minimising the uncertainty from the experimental C-V data, the normalised C/A data should be chosen for the fitting because the normalised capacitance with area only depends on the relatively permittivity of the dielectric and the depletion width. Fig. 3.4 shows an example of the C-V fitting with experimental C-V data in Fig. 3.3 (left).

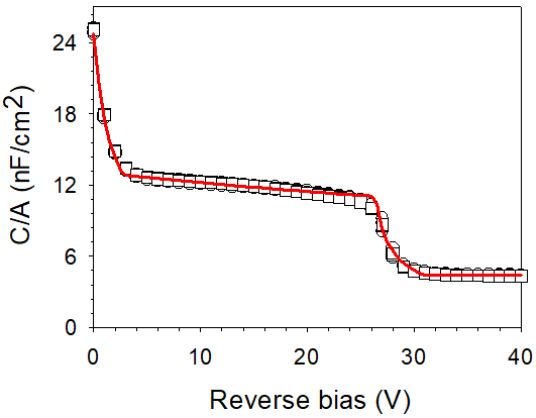

Fig. 3.4: Experimental (symbol) and simulated (line) normalised capacitance with diode's area.

However, there is no criteria for the fitting such that multiple solutions could provide a good fitting. In a worst scenario where the fitted doping concentration and depletion width are far away from the growth sheet, secondary ion mass spectroscopy (SIMS) measurements can offer more accurate information. Unlike the C-V measurement which gives information for electrically active dopants, SIMS measures all the dopants in the sample. It is a destructive technique involving a high energy ion beam to bombard the sample. After the sample is bombarded by the primary ions, the mass ratio and the densities of the secondary ejected ions will be measured and analysed, providing highly accurate doping and the doping element species.

3.3 Avalanche gain measurements

3.3.1 Experimental setup

The avalanche gain can be easily obtained by dividing the photocurrent by dark current. However, this would lead an inaccurate result since DUT can have a significantly high dark current. In this work, the avalanche gain measurement utilised a phase-sensitive-detection method to distinguish the photocurrent from the dark current. The schematic of the gain setup is shown in Fig. 3.5. An SMU was used to apply the bias across the device and sensing resistor. Before light coming from a continuous wave (CW) laser to the DUT, it was optically chopped at a certain frequency (180 Hz) by an optical chopper. Meanwhile, this frequency was fed into the lock-in amplifier (LIA) as a reference signal. In this case, the DUT will generate an AC photocurrent instead of a DC photocurrent that is then across the sensing resistor. Finally, the LIA will take this photovoltage and an accurate photocurrent can be obtained.

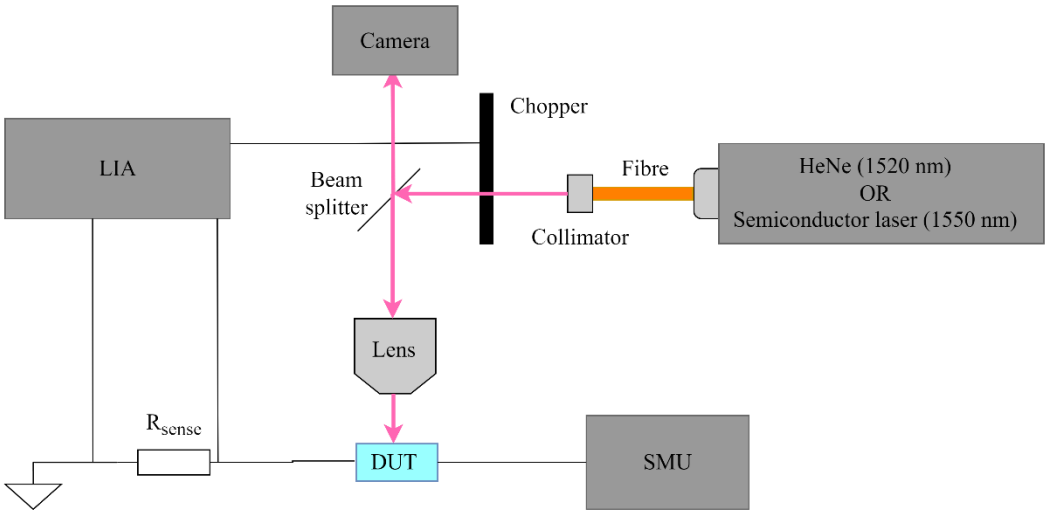

Fig. 3.5: Schematic of avalanche gain setup. The continues wave light is chopped at 180 Hz by an optical chopper controlled by the LIA. The DUT is biased by a SMU and the photovoltage is measured by the LIA through the sense resistor (typically 1000 Ω).

3.3.2 Avalanche gain and responsivity

The photocurrent is converted from the measured photovoltage using

$$I_{ph} = \frac{V_{ph}}{0.45 \times R_{sense}}, \tag{3.8}$$

where V_{ph} is the recorded photovoltage from the LIA and R_{sense} is the resistance values of the sense resistor. The value of 0.45 is the factor for converting the root mean square voltage of a square wave to peak-to-peak.

Avalanche gain $M(V)$ is given by the ratio of photocurrent $I_{ph}(V)$ to primary current I_{pri}, which is defined as unmultiplied photocurrent and also known as the photocurrent at unity gain. For SAM APDs, the unity gain is generally taken when biased at V_p, when the absorber is fully depleted. However, the carriers can diffuse from absorber to the multiplication, resulting in a gain greater than unity at V_p. In this case, the unity gain point needs to be calibrated depends on experimental photocurrent. An example is shown in Fig. 3.6 (left), which shows the experiment photovoltage versus reverse bias in the log scale. The significantly increase before -26 V is because the depletion width is still expanding and hence the collection efficiency. At ~ 27 V, the nearly constant photovoltage indicates the i-absorber is fully depleted. Therefore, -27 V can be taken as the unity gain point and corresponded $M(V)$ is shown in Fig. 3.6 (right).

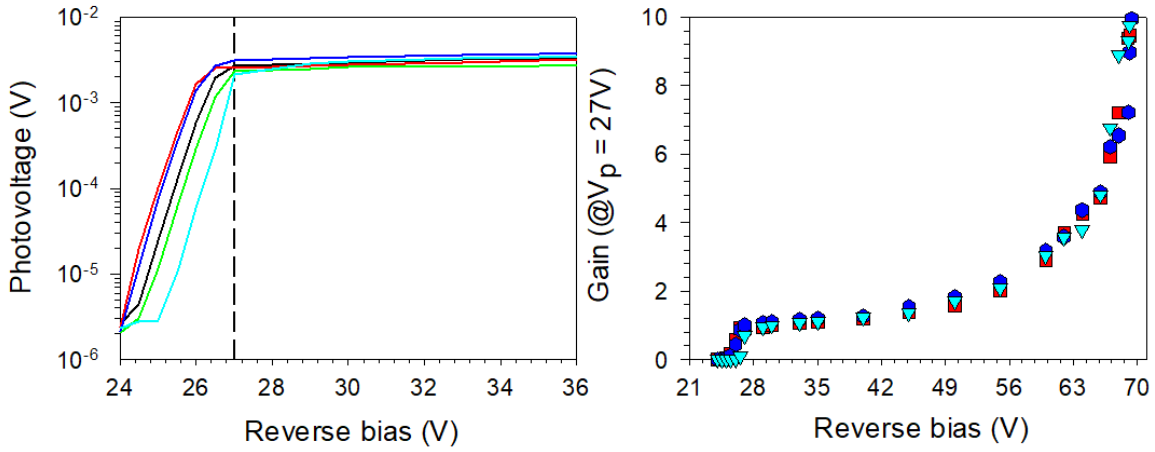

Fig. 3.6: (Left) photovolatge (of 100 Ω sensing resistor) versus reverse bias. (Right) avalanche gain (assume unity gain at -27 V) versus revers bias. Data obtained from InGaAs/InP devices using the avalanche gain setup.

Responsivity is measured using the same experimental setup and procedure as for avalanche gain measurements. It requires the measure of the optical power from the CW laser to the DUT. Power meter with a correspond wavelength is generally used to measure the optical power underneath the lens prior to the gain measurements. The responsivity is taken as the ratio of photocurrent and the input optical power, as calculated below:

$$Responsivity\ \left(^{A}/_{W}\right) = \frac{I_{ph}\ (A)}{optical\ power\ (W)}. \tag{3.9}$$

Since the responsivity increase with gain, it is generally taken at the unity gain point. Knowing the responsivity at unity gain is important because it can work out the external quantum efficiency, which indicates the maximum achievable SPDE for a given SPAD. The external quantum efficiency (QE) is given by

$$QE = \frac{R_{measured}}{R_{ideal}}, \tag{3.10}$$

where

$$R_{ideal} = \frac{\lambda\ (\mu m)}{1.24}, \tag{3.11}$$

and $R_{measured}$ is the measured responsivity and R_{ideal} is the ideal responsivity for a given wavelength λ in micrometres.

3.4 SPAD measurements

3.4.1 Experimental setup for unpacked samples

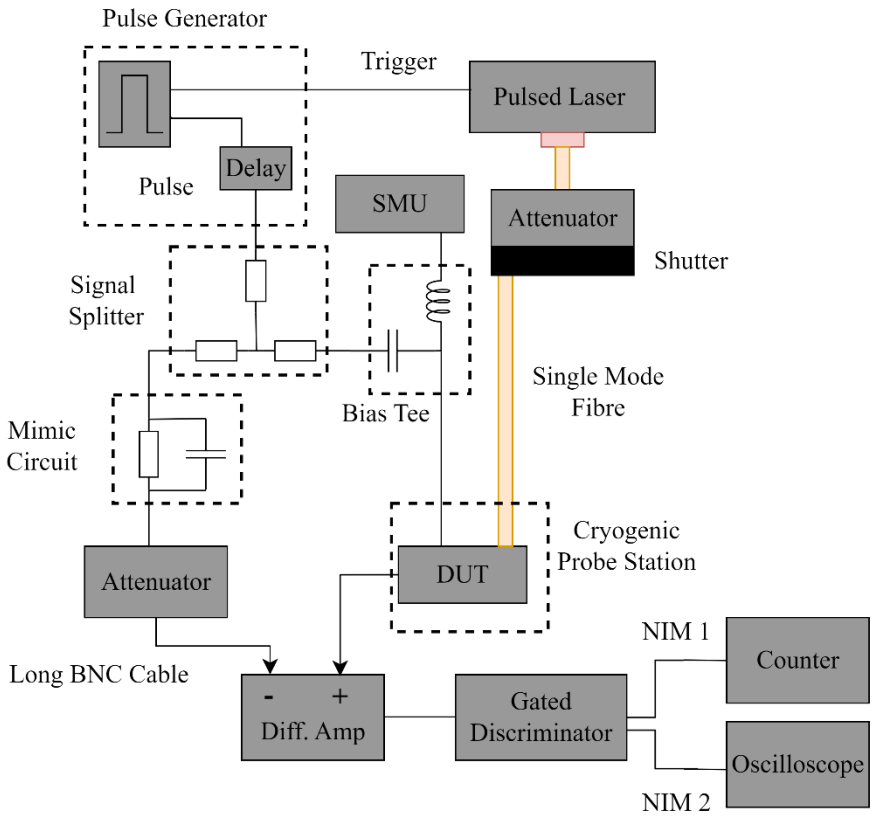

Fig. 3.7: Schematic of experimental setups for dark and photon counting measurements.

The experimental setup for dark and photon count measurements is illustrated in Fig. 3.7. DUT were placed in cryogenic probe station (ST-500 Janis probe station) under vacuum environment and with an external temperature controller. Gated quenching method was choosing for the measurements. The AC bias was superimposed to the DC bias using the commercial bias tee (Picosecond Pulse Labs 5530A). The inductor of the bias tee is used to block the AC from the SMU while the capacitor is used to block the DC from the pulse generator. The DC bias (provided by Keithley 6487 Picoammeter) was set to below breakdown (but after V_p). The AC bias was provided by TTi-TGP3152, which also coupled the same repetition rate to trigger the pulsed laser. The AC signal was split for the SPADs and a dummy circuit. The former will produced a transient signal and the later was used to mimic the shape of transient signal by adjusting the capacitance values. The amplitude of the transient signal from the dummy circuit was modified by the attenuator (HP 335D VHF). Before the transient is successfully cancelled, both signals from the dummy circuit and the SPADs need to arrive to the differentiated amplifier at the same time. This was done by adjusting the coaxial cable length as the speed of electrical signal travel in the coaxial cable is equal to 2/3 speed of light. The output from the diff. amp was converted to a nuclear

instrumentation module (NIM) signal using the customised gated discriminator (designed and constructed by Dr. S. Dimler), and finally recorded by the counter (Canberra Dual Counter/Timer 512). To produce a NIM signal (defined as ~ 16 mA into 50 Ω and for ~ 2 ns), the output of avalanche signal needs to be larger than the threshold values set on the gated discriminator. However, the transient signal can also larger than the threshold voltage, leading to a false triggering. Therefore, the threshold voltage on the discriminator must larger than the transient signal but smaller than the avalanche signal. This was monitored by a Keithley 2700 Digital Multimeter. A second NIM signal was generated in parallel for identifying the source of the produced NIM signal on the oscilloscope. The second NIM signal should occurs with the avalanche signal at the same time, otherwise the NIM signal is triggered by the transient, resulting in an inaccurate result. In addition, the customised gated discriminator can only allow to be triggered once per gate, which helps to check the experiment settings (i.e. the maximum recorded raw count per second is 10^3 and 10^6 for 1 kHz and 1 MHz, respectively).

3.4.2 DCR

DCR measurements were taken using a fixed pulse height AC bias while adjusting the DC bias from below breakdown until an 'event' occurs. This was introduced to minimise the transient effect which affected by the amplitude of the AC bias, especially when it was non-impedance match. This would lead to an uncertainty for excess bias since the determined breakdown voltage affected by the threshold voltage on the discriminator. Due to non-impedance match of the Janis probe station, the actual AC pulse applied to the devices is distorted.

Ideally, the threshold voltage on the discriminator should be set as low as possible such that the small avalanche signal can be detected. Therefore, cancel the transient is important prior to the DCR and SPDE measurements. The procedures of transient cancellation are given by follow:

- Increase the DC bias greater Vp but below V_{bd} by 5 ~ 10 V.
- Monitored the signal from SPAD and dummy circuit on the oscilloscope under the same amplitude ranges.
- Adjust the variable capacitor in the dummy circuit as well as the electrical attenuator to match amplitude of the signal.
- Adjust the BNC cable length to let two signals become identical shown on the oscilloscope.
- Fed two signal into diff. amp in right orders (i.e. signal from SPAD to positive side).
- Monitor the second NIM signal on oscilloscope and adjust the threshold voltage on the discriminator to ensure no NIM signal can be trigged when devices were biased below breakdown. Preferably, the set threshold voltage is just above the values that the NIM signal will triggered by the transient.

To obtain reliable DCRs, data are recorded typically for 1 minute or longer with repeated multiple times. In this work, the DCRs were recorded for 1 second and repeated 60 times. The DCR is calculated by measuring the mean number of dark counts per second and normalising for the duty cycle, which is the product of the repetition rate (frequency) and 'on-time' (width) of the applied AC pulse. Assuming the dark carriers follows Poisson distribution [1], the normalised DCR related to the dark count probability (P_d) are given by

$$P_d = \frac{N_d}{f}, \tag{3.12}$$

and

$$DCR = \frac{-\ln(1 - P_d)}{t_{on}}, \tag{3.13}$$

where N_d is number of measured dark counts per second, t_{on} is applied pulse width and f is the repetition rate.

3.4.3 SPDE

The photon counting measurements were followed by the DCR measurements under the same bias condition. This is because the DCR can shift with time, the back-to-back measurements can obtain more reliable SPDE. A pulsed laser (ALPHLAS, PICOPOWER-LD-1550-20) with 1566.5 nm central wavelength and 23.1 ps (at 100 kHz) pulse width was used for photon pulse generation, along with an electrical variable optical attenuator (EVOA) (EXFO FVA-3100) to yield an averaged 0.1 photon per pulse. The status of the photon source to the devices was controlled by the shutter of the EVOA such that the pulsed laser was kept switching on during the measurements, minimising the variation of optical power and hence the average photon number per pulse.

Apart from the attenuation from the EVOA ($\mu_{variable}$), there is also an optical power loss inside the Janis (at the end of fibre), which taken as $\mu_{coupling}$. Since the devices were not-fibre coupled inside the Janis, the coupling efficiency (μ_{device}) from fibre to devices also need to included. Together, the total attenuation is given by

$$\mu_{total} = \mu_{variable} + \mu_{coupling} + \mu_{device}. \tag{3.14}$$

The optical power loss inside the Janis probe station can be calculated using a commercial InGaAs photodiode with known responsivity, as given by

$$\mu_{coupling}\,(dB) = 10 \times \log_{10}\left(\frac{P_{in} \times R}{I_p}\right), \tag{3.15}$$

where P_{in} the measured optical power before coupled into Janis probe station, R is diode responsivity and I_p is the measured photocurrent.

The coupling efficiency is included because the core of the diameter of single mode fibre can larger than test devices (65 μm cf. 10 – 40 μm). In this case, the coupling efficiency from the fibre to device's optical window is taken as the ratio of photocurrent (under the same optical power) from devices with 200 μm diameter to those with 10/20/40 μm diameter.

Finally, the average number of photons per pulse ($\bar{n}$ = 0.1 in this work) can be obtained by adjusting the variable attenuator in Eq. (3.14). The calculation is given by

$$\bar{n} = \frac{E_{pulse}}{E_{photon} \times 10^{\frac{\mu_{total}}{10}}}, \tag{3.16}$$

where the E_{pulse} is the measured pulse energy which converted by the measured optical power, E_{photon} is the photon energy for a given (1550 nm) wavelength.

There are two equations to deduce the SPDE experimentally [2], and although they both include the existence of the dark count, slightly different definitions of SPDE lead to different results.

$$SPDE = \frac{1}{\bar{n}} \ln\left(\frac{1 - P_d}{1 - P_t}\right), \tag{3.17}$$

$$SPDE = \frac{P_t - P_d}{1 - e^{-\bar{n}}}, \tag{3.18}$$

and

$$P_t = \frac{N_t}{f}, \tag{3.19}$$

where $\bar{n}$ is the average number of photons per pulse, N_t is the number of measured total counts per second. P_d is the dark count probability, and P_t is the probability of the measured events during the measurement.

Eqn. (3.17) assumes that the photon can still be detected if it arrives with a dark event simultaneously, whereas Eqn. (3.18) assumes that only one avalanche event caused by a photon or a dark count can be detected. The former might suitable for sub-Geiger mode APD. In contrast, the latter is more appropriate to apply for the SPAD because only one carrier can initiate an avalanche event. The SPDE of this work was calculated using **Eqn. (3.18)**.

3.4.4 Experimental setups for packaged samples

For the packaged devices, DCR and SPDE measurements can carried out in the SPAD setup using a capacitance quenching circuit (CQC) designed and constructed by Dr S Dimler [3]. Unlike the Janis probe station, this setup has a smaller temperature range of 290 to 300 K. However, the SPAD setup offer simpler operation than the former because the signal splitter, bias tee, attenuator and diff. amp are integrated on the CQC printed circuit board (PCB). In addition, all the component on the CQC PCB are impedance match so that it offers better transient cancellation compared to Janis probe station, despite

the packaged devices might non-impedance match to the CQC board. More details about the CQC PCB can be found in [4].

3.5 SPAD modelling

This section described the two simulation models for breakdown probability calculations. These are the analytical recurrence equation [5], [6], [7] and the RPL model [8], [9]. Both of them assumes the electric field is constant and yield a highly similar P_b for a given p-i-n diode. However, RPL model can simulate the temporal statistics while the recurrence equation is limited to P_b simulation.

3.5.1 Recurrence equation

The recurrence equations for breakdown probability were initiated developed in [5] and were expended in [6], [7]. The history-dependent ionising probabilities are given by

$$p_e(x'|x)\,dx = \alpha(x'|x)\exp\left(-\int_x^{x'}\alpha(x'|x'')dx''\right)dx = \alpha(x'|x)P_{se}(x'|x)dx \tag{3.20}$$

and

$$p_h(x'|x)\,dx = \beta(x'|x)\exp\left(-\int_x^{x'}\beta(x'|x'')dx''\right)dx = \alpha(x'|x)P_{sh}(x'|x)dx\,, \tag{3.21}$$

for electron and hole, respectively. The $P_{s(e,h)}$ is the survival probability that a carrier travelling from x' to x will not initiate impact ionisation. These equation can coupled with hard dead space model, so the $P_{s(e,h)}$ can be taken as (1 - $h_e(\zeta)$) and (1- $h_h(\zeta)$) for electron and hole, respectively.

Using the history-dependent ionisation probabilities, the history-dependent breakdown probabilities for any p-i-n diodes (regardless of avalanche width and electric field) are given by

$$\big(1-P_e(x')\big) = P_{se}(x'|0) + \int_0^{x'} p_e(x'|x)\big(1-P_e(x)\big)^2(1-P_h(x))\,dx \tag{3.22}$$

and

$$\big(1-P_h(x')\big) = P_{sh}(x'|w) + \int_{x'}^{w} p_h(x'|x)\big(1-P_h(x)\big)^2(1-P_e(x))\,dx\,. \tag{3.23}$$

3.5.2 Random Path Length (RPL)

RPL model exploited the Monte Carlo simulation technique to sample the entire probability density function of ionisation path length in order to simulate avalanche gain statistics [8]. It is well suited to study the statistical process of impact ionisation because it could record all the temporal information of each trial in many trials (typically 100,000). Therefore, the spatial and temporal information of the impact ionisation not only could be used to predict the gain and noise but also could be used to study the avalanche breakdown statistics [9].

RPL requires the input of $h_e(x_e)$ and $h_h(x_h)$ whose details in Section 2.1.1. It would randomly select a number, r, which is evenly distributed between 0 and 1 to represent the ionisation probability of the carriers. Substituting this random number r to the ionisation probability of an electron, $P_e(x_e) = \int_0^{x_e} h_e(x_e)$, gives the ionisation path length of $L_e = d_e - \frac{\ln(1-r)}{\alpha^*}$.

To implement the RPL model, a sequential approach is used to track the impact ionisation process. Fig. 3.8 shows the electron and hole tracking process, respectively. After an electron is injected at position 0, the model will start to generate its random path length, L. If the random path length is shorter than avalanche width, the model will allow the electron to impact ionisation and so generate a new EHP. At the same time, the position and the time of the ionisation event happened would be recorded. The random path length will be continuously generated and compared with the depletion width until the first electron leaves the device. Then, the model will keep repeating this process until all the electron leaves the devices (no more impact ionisation event happens). Next, the recorded ionisation position and time from each electron will be used to track the impact ionisation of the corresponding hole in a similar manner. Each time an impact ionisation event happens, the RPL model will record the position and time and then give them to the related tracking process.

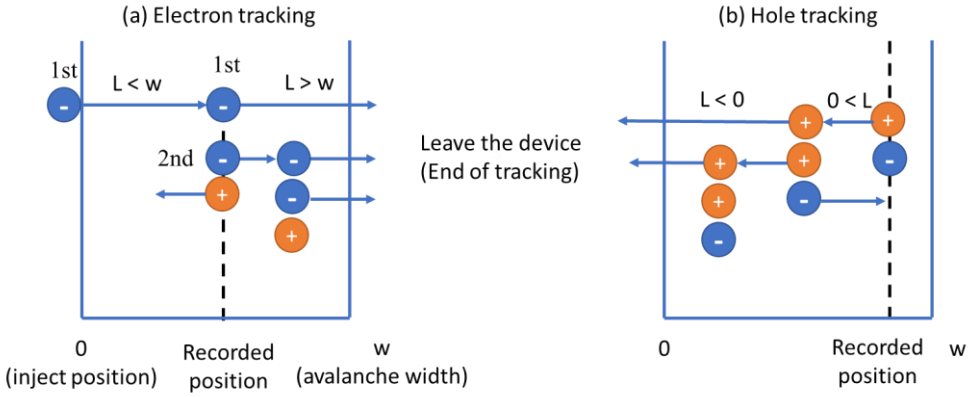

Fig. 3.8: Electron (a) and hole (b) tracking process in RPL simulations.

The ratio of either local and enabled ionisation coefficient of the offspring carrier and the parent carrier is used to represent the variable k, where $\beta(*)/\alpha(*)$ for pure electron injection and $\beta(*)/\alpha(*)$ for pure hole injection. The RPL will assume the electric field is uniform, and the carriers will have a constant saturated drift velocity (i.e. $v_e = v_h = 1 \times 10^5 m/s$). The avalanche current is calculated by Ramo's theorem

$$I = \left(\frac{q}{w}\right)(n_e v_e + n_h v_h)\,, \tag{3.24}$$

where w is the avalanche width, n_e and n_h is the number of electron and hole, respectively.

The avalanche process in the simulation that for above breakdown will never stop as the gain is infinite. Therefore, similar to the quenching circuit, it needed to be 'quenched' in SPAD modelling by setting a

threshold current. A threshold current values is set to 10 μA and once the avalanche current larger than the threshold, the simulation will be stopped. The breakdown probability P_b is calculated by dividing the number of trial reach to breakdown by the total number of trails. The average time it takes to breakdown is defined as breakdown time $<t_b>$ and its standard deviation referred to as timing jitter σ.

3.6 Devices fabrication

Devices fabrication procedure and photolithography process for mesa devices and planar InGaAs/InP SPADs will be discussed in this section. Both mesa and planar devices fabrication utilised standard photolithography process but planar InGaAs/InP SPADs required extra fabrication for the double Zn diffusion.

3.6.1 Standard mesa fabrication procedure

After cleaving the whole growth wafer into a small piece of sample, the sample will be immersed into three different solvents in order: warmed n-butyl acetate (to remove any dirt or grease), acetone (to remove any chemical solvent) and isopropanol (to further clean and dilute acetone). This is called three stage cleaning process, followed by the standard photolithography process.

The sample is firstly dehydrated on the 100 °C hot plate for several minutes and then be evenly coated by photoresist in the spinner. It is important to choose the correct type of photoresist according to the mask design. The positive photoresist is soluble after exposed with UV light whilst the negative photoresist is insoluble after being exposed. The thickness of spanned photoresist can be modified depend on the spinning speed and time. Afterward, the sample will be soft baked on the hot plate to finalise and secure the photoresist. The photoresist later is exposed to UV light in the mask aligner for a given set time, which determined the thickness of the photoresist and the wavelength of the UV light. Finally, the desired pattern now is transfer from the mask to the photoresist after the developing process.

Metallisation was done by either thermal evaporation (for Ti/Au and Au/Zn/Au) or sputter coating (for Ti/Au only) in this work. Since the metal have deposited all over the sample, the unwanted metal needs to be removed by simply place the sample into acetone. The acetone will remove the photoresist as well as the metal on the top, which is known as lift off process.

The next step is etching the sample to form multiplied individual mesa devices, which can be done by either wet (acid) or dry (plasma) etching. For samples with the semi-insulating substrate, the etching process also helps to reach the bottom contact layer. In this case, the sample needs to be pattered by the bottom contact mask and followed by the metal deposition and lift-off process, which is the final step of the fabrication. In contrast, the final step for sample with conducted substrate is metal deposition on the back without patterning and lift-off process.

A fabricated example with the semi-insulating substrate is shown in Fig. 3.9. This work chooses wet etching instead of dry etching since wet etching caused less damage to the mesa wall, which can introduce a hotspot or increase the dark current. Material-selective etchants are used to reach the bottom contact layer. These were HCl:DIW (2:1) for InP as well as H_2SO_4:H_2O_2:DIW for InAlAs, InGaAsP and InGaAs.

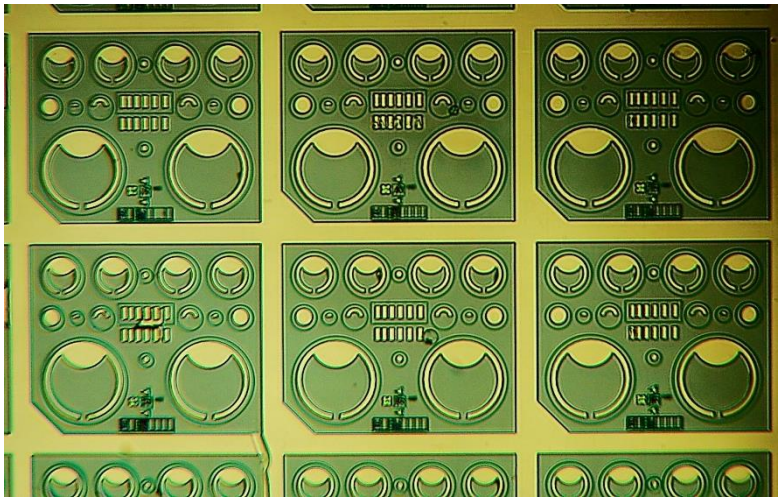

Fig. 3.9: Sample with semi-insulating substrate after etching, metallisation and lift-off process for bottom contact layer. The top contact of each mesa devices are visible and the unit cells were defined by etching down to bottom contact layer.

3.6.2 Photolithography and etching

Two positive photoresist (SPR 220 and SPR 350) were used in this work. The condition for this work used in photolithography process are summaries in Table 3.1. Apart from the photoresist, polymethylglutarimide (PMGI) was coated prior to photoresist for metallisation. This was introduced to create undercut below the thick photoresist after the developing, allowing the acetone more effectively remove the photoresist and hence the lift-off process. Further reduce of lift-off time can be achieved by using EKC 830 prior to acetone, which is a much stronger positive resist stripper. The use of PMGI was similar to photoresist except need for a longer soft bake time (5 to 6 minutes) at a higher temperature (180 ℃).

Table 3.1: Conditions for photolithography process with two photoresists.

Step	**Equipment / Solvents**	**Conditions**	
		SPR 350	SPR 220
Dehydration bake	Hot plate	100 ℃, 1 - 2 min	100 ℃, 1 - 2 min
Soft bake		100 ℃, 1 min	100 ℃, 3 min
Exposure	UV 400	4 - 5 sec	18 - 19 sec
	UV 300	12 - 13 sec	39 - 40 sec
Developing	MF26A:H_2O (0.7:1)	1 min	1.5 min

If the samples have a dielectric layer (i.e. silicon oxide (SiO_2) or silicon nitride (SiN)), adhesion promoter of hexamethyldisilazane (HMDS) is required to apply before photoresist. The HMDS is used to improve the adhesion between the photoresist and dielectric layers, ensuring the photoresist will not

peel off in the later process. Unlike the PMGI, the HMDS used in this work did not involve soft bake. Instead, samples were soaked with HMDS for 30 seconds inside the spinner, followed by the same spinning process as the other resists. The photoresist or PMGI later was directly deposited on top without taking out the samples.

Dielectric layer is commonly employed as a passivation layer or anti-reflection (AR) coating. This work mainly deposited SiN as passivation layer using the plasma enhanced chemical vapour deposition (PECVD). Since SiN will deposit on the entire samples, it is necessary to clear the SiN from the optical window and metal contact. Depend on the purpose, SiN was etched either by the HF acid or plasma etching.

In this work, only the 40 % HF was used to completely remove the SiN (more details in Appendix C), which was done by Dr T Blain under the Help and Safety rules of the University of Sheffield. Compared to HF, plasma etching is more controllable and safer. There were two plasma etching method used: (i) reactive ion etching (RIE) and (ii) inductively coupled plasma (ICP) etching. The ICP provided more uniformed etching than RIE but its higher power caused more damage with the photoresist, which making the photoresist become hard to remove afterwards. In addition, due to the equipment usage restrictions, only the samples without metal can be used in ICP. Therefore, RIE is more flexible and was mainly used to clear the area for optical window and metal contact in this work (discussed in Appendix C).

3.6.3 Planar InGaAs/InP SPADs fabrication

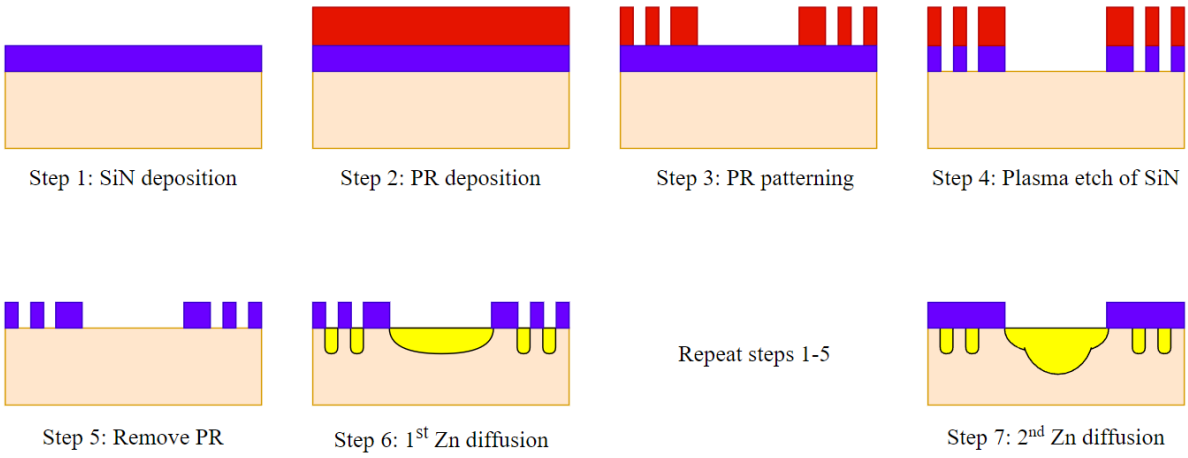

Fig. 3.10: Schematic of fabrication process for double Zn diffusion.

Unlike the mesa devices, planar InGaAs/InP SPADs in this work requires double Zn diffusion to define the active region. A schematic of fabrication for double Zn diffusion is show in Fig. 3.10. The Zn diffusion was done by the external company after the wafer growth. The Zn diffusion profiles are mainly controlled by the diffusion temperature, pressure and time. Optimising the those parameters can lead to

a well-controlled Zn diffusion profiles, but they are depend on the type of reactor as well as the diffusion technique [10]. The Fig. 3.11 (left) shows the received images from the contactor after the double Zn diffusion while the Fig. 3.11 (right) shows the actual devices after the fabrication.

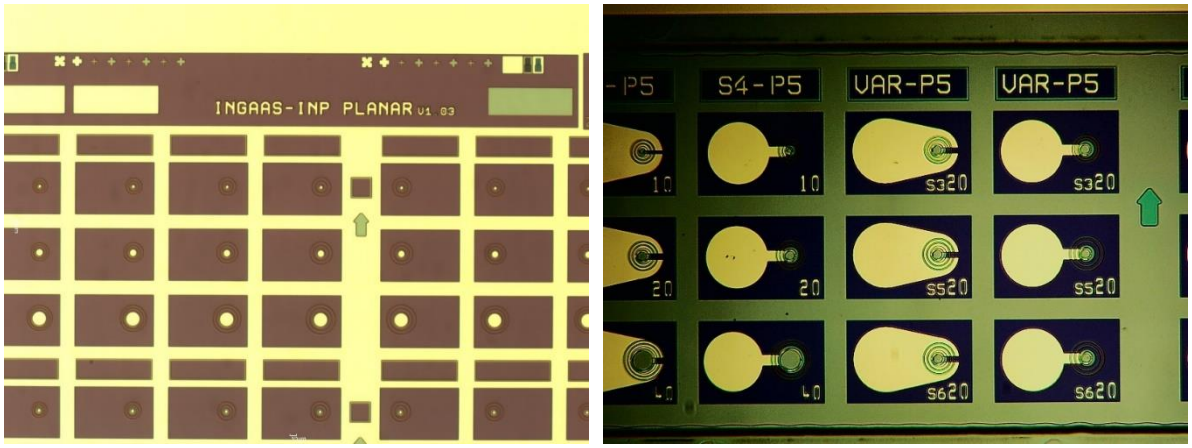

Fig. 3.11: Image of planar InGaAs/InP SPADs after double Zn diffusion process (left) and after fabrication (right).

3.7 References

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Chapter 4: InGaAs/InP Single Photon Avalanche Diode (Round 1)

This chapter presents the experimental and simulation results for planar InGaAs/InP SPADs from two wafers with identical epi-wafer structures but different Zn diffusion depth combinations. SPAD variants include varying active region diameter, Zn diffusion extension, and FGRs (number of FGRs and their spacing from the active region). The target application was remote methane detection at 1.65 µm wavelength. The desired operation temperature of the InGaAs/InP SPAD is 275 K (for portability), with an upper limit of 20 Mcps for dark counts.

The Round 1 wafer and original photolithography mask were designed by Dr Dimler. He also developed the Round 1 device structure script in the TCAD simulation. The first sample in Round 1 (referred to sample B1) was fabricated by Dr Petticrew.

4.1 Wafer design

4.1.1 InGaAs absorber width and absorption efficiency

Absorption efficiency of InGaAs at 1.65 µm wavelengths at 77 to 300 K was calculated using

$$I\,(x) = I_{L0}\exp(-\alpha_{abs}x)\,, \tag{4.1}$$

where I_{L0} is the initial intensity of the light, and α_{abs} is the optical absorption coefficient. Due to a lack of published absorption coefficients of InGaAs at 77 K for wavelength beyond 1.61 µm, it was necessary to first extrapolate the data of [1] to 1.65 µm and then interpolate between the 77 and 300 K data [1]. The calculations assumed (i) negligible optical reflection loss at the air-semiconductor interface and (ii) negligible reflection from the metal contact on the substrate-side.

The calculated efficiency versus absorber width as functions of wavelengths and temperature are shown in Fig. 4.1. Using the value of absorption efficiency at 1.55 µm wavelength as a reference, the 300 K absorption efficiency decreases by 10 and 30 % at 1.60 and 1.65 µm, respectively. The reductions worsen as temperature decreases. At the target temperature of 275 K, an absorber width of 1.50 µm provides only ~ 40 % efficiency at 1.65 µm wavelength. Hence an absorber of 1.60 µm was chosen as a compromise.

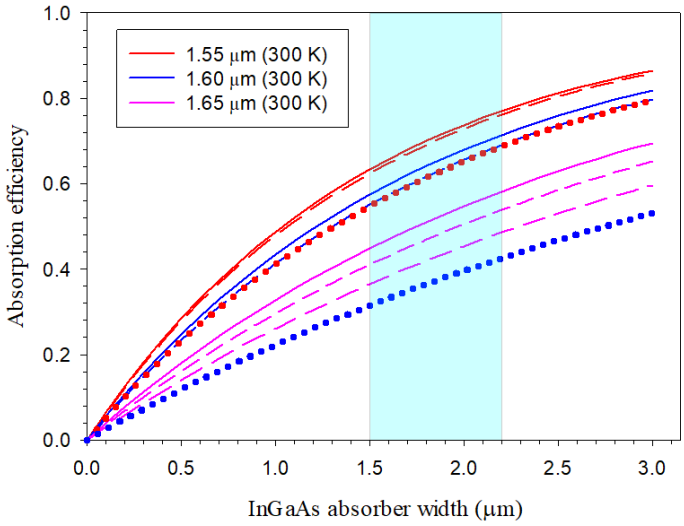

Fig. 4.1: Absorption efficiency versus InGaAs absorber width at wavelengths of 1.55, 1.60 and 1.65 µm and temperature of 300 (solid lines), 275 (dashed line) and 77 K (dotted line). Highlighted region represented the typical InGaAs absorber width of InGaAs/InP SPADs in the literature.

4.1.2 Tunnelling current and DCR

SPAD dark currents originate from a combination of bulk and surface leakage mechanisms, whose dominance depends on the specific wafer, device design and operation temperature. Those from bulk leakage mechanisms, namely diffusion current, generation-recombination current, and tunnelling current, will lead to dark counts. Of these, only tunnelling current is strongly dependent on the electric field. Hence, the upper dark count limit was used to establish the maximum electric field across the InGaAs absorber and the InP avalanche region.

Assuming a unity breakdown probability (worst case scenario), the SPAD having zero dead time, and excluding afterpulsing, the upper dark count limit of 20 Mcps leads to a maximum acceptable bulk dark current of 3.2 pA for a SPAD during Geiger mode operation. For an active region radius of 15 µm, the SPAD active area is 7.07×10^{-6} cm^2, so the maximum acceptable bulk dark current density is 450 $nAcm^{-2}$. Allowing for the other bulk dark current mechanisms and additional dark counts caused by afterpulsing, an **upper limit of 45 $nAcm^{-2}$ for band-to-band tunnelling current density** is used instead for the wafer design of this work.

Using Eqn. (2.12) and material-specific parameters [2], [3], band-to-band tunnelling current densities at 300 K for InGaAs and InP were calculated as functions of electric field and width. The corresponding results are shown in Fig. 4.2 (left) and (right). Two reference lines at 450 and 45 $nAcm^{-2}$ (the upper limit) are included. Observing Fig. 4.2, for the widths considered, the electric field across the InGaAs absorber and the InP avalanche region should be < **165** and **480 kV/cm**, respectively during Geiger mode operation.

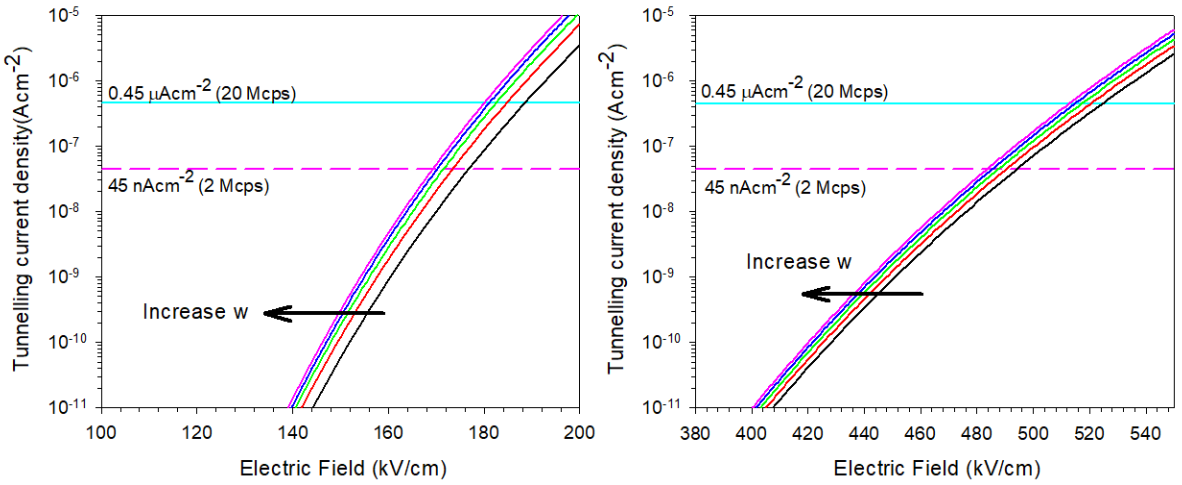

Fig. 4.2: Calculated band-to-band tunnelling current density versus electric field in the InGaAs absorber (left) and InP avalanche region (right) for 0.5, 1.0, 1.5, 2.0 and 2.5 μm.

4.1.3 Breakdown probability and DCR

SPADs rely on avalanche breakdowns to produce large avalanche currents, so the minimum electric field in the InP avalanche region for non-zero breakdown probability (i.e. the breakdown field) must be considered. Using recurrence equations [4] and ionisation coefficient for InP [1], P_b for pure hole injection was calculated as functions of electric field and avalanche widths. The results are compared in Fig. 4.3. For a given avalanche width, P_b is zero until the electric field exceeds the breakdown field, after which P_b increases with the electric field and eventually approaches unity. As the avalanche width increases, the breakdown field (defined as the electric field where $P_b > 0.01$) decreases.

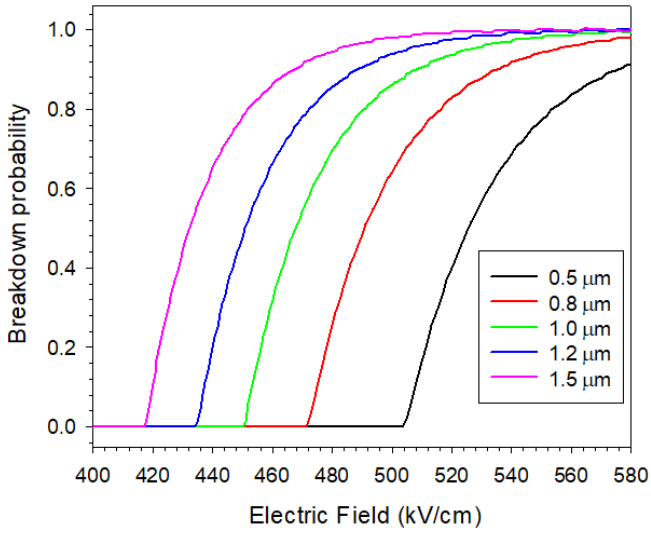

Fig. 4.3: InP avalanche breakdown probability from pure hole injection versus electric field for avalanche widths ranging from 0.5 to 1.5 μm.

Values of breakdown field and electric field limit due to tunnelling current are compared in Table 4.1, for InP avalanche width ranging from 0.6 to 1.5 μm. To achieve non-zero P_b while avoiding excessive

tunnelling current, the InP avalanche width should exceed 0.8 µm. Increasing the avalanche width increases the working electric field range (e.g. from 48 to 93 kV/cm for 0.8 to 1.5 µm).

Table 4.1: Calculated electric field limits for various InP avalanche width.

InP avalanche width (µm)	Maximum E (kV/cm) for J_{tun} < 0.45 µA/cm^2	Minimum E (kV/cm) for P_b > 0
0.6	523.0	505.0
0.8	520.0	472.0
1.0	517.0	451.0
1.2	514.0	435.0
1.5	511.0	418.0

Using the chosen absorber width (1.6 µm) and a range of avalanche widths (0.8 – 1.2 µm), the overall characteristics of DCR versus electric field in the InP avalanche region were simulated. The simulations considered only the dark carriers originated from InP band-to-band tunnelling and that these dark carriers experienced the appropriate P_b value from the InP avalanche region. The SPAD active regions were assumed to have 15 µm radius. The P_b results and overall DCR are plotted against electric field in the InP avalanche region in Fig. 4.4 (top) and (bottom), respectively. At P_b = 0.8, for avalanche width of 0.8, 1.0 and 1.2 µm, the simulated DCR values are ~ 11.0, 2.0 and 0.5 Mcps respectively. Wider avalanche regions exhibit lower DCR, but they require larger operating voltages and are more demanding on wafer growth, compared to narrower avalanche regions. Hence, **an avalanche width of 1.0 µm** was chosen for this work.

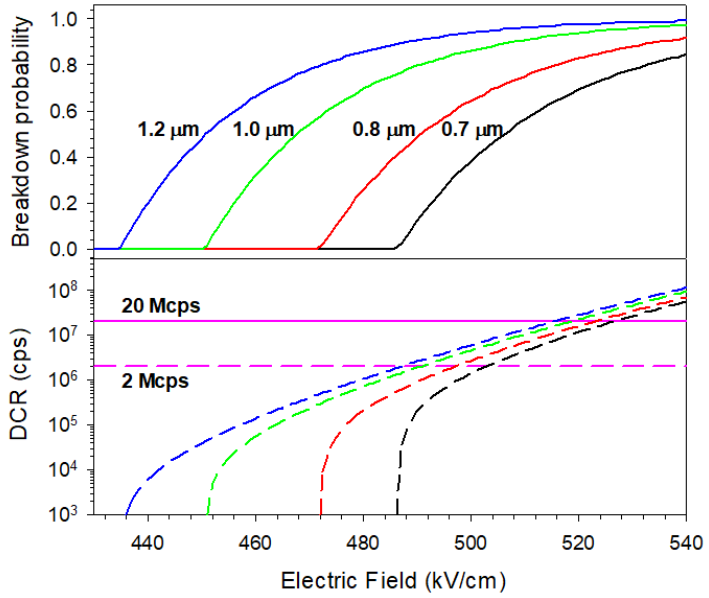

Fig. 4.4: Simulation of (top) avalanche breakdown probability for pure hole injection and (bottom) dark count rate (free running mode) versus electric field.

4.1.4 InGaAs/InP SPAD wafer

Overall, the InP avalanche and InGaAs width was chosen to be 1.0 and 1.6 µm, respectively. The large difference between electric fields in the two regions is maintained by the charge sheet. The charge sheet thickness was 0.3 µm to allow for sufficient control of charge sheet doping profile during the wafer growth.

Doping density of the charge sheet should be sufficiently high to maintain the large electric field difference, but not so high as to result in an un-depleted absorber at the breakdown condition. To find the appropriate range of charge sheet's doping density, the punch through voltage, V_p, was plotted as function of charge sheet's doping density, as shown in Fig. 4.5 (top). Breakdown voltage ($P_b > 0.01$) and voltage to achieve $P_b = 0.8$ are also included. The upper limit for charge sheet's doping density is where V_p exceeds the breakdown voltage, resulting in 9e16 cm^{-3} in this case.

The lower limit of the charge sheet's doping density is determined by the peak field in the InGaAs absorber, shown in Fig. 4.5 (bottom). To avoid significant band-to-band tunnelling current in the InGaAs absorber, the peak field should be **< 165 kV/cm**, resulting in a lower limit of 6.9×10^{16} cm^{-3}. Hence the appropriate range of charge sheet's doping density is from 6.9×10^{16} cm^{-3} to 9.0×10^{16} cm^{-3}.

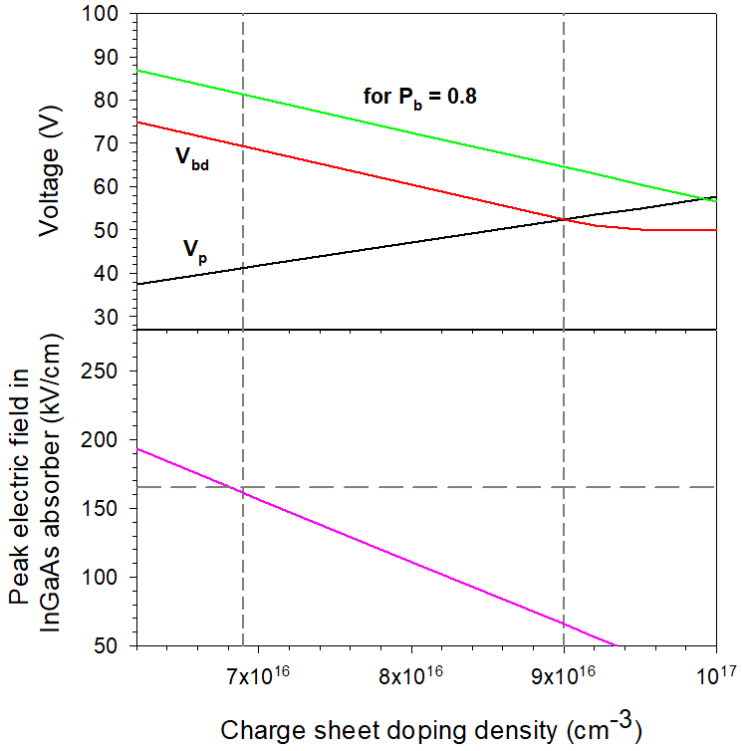

Fig. 4.5: Predicted punch through voltage and breakdown voltage (top) and (bottom) peak electric field in InGaAs when $P_b = 0.8$ for InGaAs/InP SPAD with 1.6 µm InGaAs, 1.0 µm InP and 0.3 µm charge sheet for various charge sheet doping.

4.2 Wafers and samples

Two wafers, wafer A (ZDCAPD-179) and wafer B (ZDCPD-178), were grown using metal organic chemical vapour deposition (MOCVD) by LandMark Optoelectronics Corporation. Their as-grown wafer structures were identical, as summarised in Table 4.2.

Table 4.2: As-grown structures of wafer A and wafer B.

Function	**Material**	**Doping (cm^{-3})** (± 20 %)	**Thickness (nm)** (± 10 %)
Avalanche	InP	Undoped	3000
Charge Sheet	InP	N (Si) 7.2×10^{16}	300
Grading	InGaAsP (1.03 µm)	Undoped	30
Grading	InGaAsP (1.17 µm)	Undoped	30
Grading	InGaAsP (1.35 µm)	Undoped	30
Absorber	$In_{0.53}Ga_{0.47}As$	Undoped	1600
Buffer	InP	N (Si) 1.0×10^{18}	1000
Substrate	InP (semi-insulating, Fe-doped)		

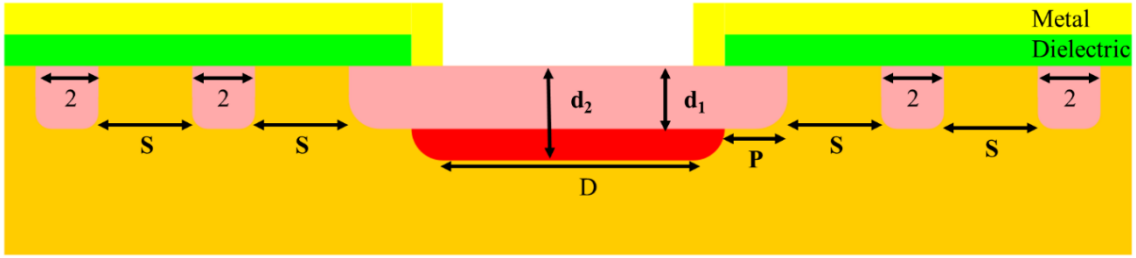

Fig. 4.6: Cross-sectional schematic diagram of the devices, in which their double Zn diffusion is offset by a distance of P and a guard ring placed at a distance of S.

Following wafer growths, LMOC carried out double Zn diffusion on both wafers using the photolithography masks produced according to the designs of this work. The affordable tolerance provided by LMOC for total Zn diffusion depths and photolithography is ± 0.1 and 1.0 µm, respectively. Moreover, the afforded variation in the charge sheet doping is ± 20 %. Original photolithography masks were designed by Dr S Dimler, University of Sheffield. The two wafers had different post-growth double Zn diffusion depths (wafer A: 1.5 and 2.0 µm; wafer B: 1.7 and 2.0 µm) to achieve the same avalanche width of 1.0 µm in the undoped InP layer.

The remaining fabrication (using methodology described in section 3.6) with tolerance of ± 2.0 µm was carried out at University of Sheffield. Cross-sectional view of the final devices is depicted schematically in Fig. 4.6. For each device, the shallow Zn diffusion extends over the deep Zn diffusion by a distance of *P*, and the guard rings are placed away from the edge of the first (shallow) Zn diffusion by a distance of *S*. Each guard ring has a width of 2.0 µm.

The variants contained in the mask are summarised in Table 4.3 (details in Appendix A). A total of three device fabrication rounds were completed on the two wafers, as summarised in Table 4.4 (along with metal contacts used). The first fabrication attempt on wafer B (sample B1) was carried out by Dr Petticrew. I-V characteristics of sample B1 (presented later) revealed need for modifications in the photolithography mask designs and p-metal contacts. These were implemented for sample B2 and A2, which had Au/Zn/Au p-contacts using thermal evaporator followed by rapid thermal annealing for 3 sec at 360 °C.

Table 4.3: Device variants for photolithography mask.

Device variants	Value or range
Device diameter (*D*)	10, 20 and 40 µm
Zn diffusion extension (*P*)	3 - 5 µm, in steps of 1 µm
Guard ring spacing (*S*)	4 - 8 µm, in steps of 1 µm

Table 4.4: Device fabrication rounds completed using the two wafers.

Wafer	Sample	Metal Contacts	Contribution
Wafer B (internal ref: 178)	B1	p^+ and n^+: Ti/Au No bondpad	Dr Petticrew
	B2	p^+: Au/Zn/Au n^+: Ti/Au Bondpad: Ti/Au	This work
Wafer A (internal ref: 179)	A2		

4.3 APD characterisation

APD characterisation (including I-V, C-V and avalanche gain measurements) provides initial performance indicators for the SPAD samples. Full APD characterisation data of samples B2 and A2 are presented. A lack of bondpads on devices from sample B1 prevented reliable avalanche gain measurements, so only the I-V and C-V experimental data were obtained.

4.3.1 I-V measurements

Room temperature forward dark I-V data of sample B1, B2 and A2 are compared in Fig. 4.7. The data shown are for devices with 20 µm diameter, P = 3 µm and a range for S values. Samples B2 and A2 exhibit lower series resistance, attributed to their p-metal contact being Au/Zn/Au instead of Ti/Au.

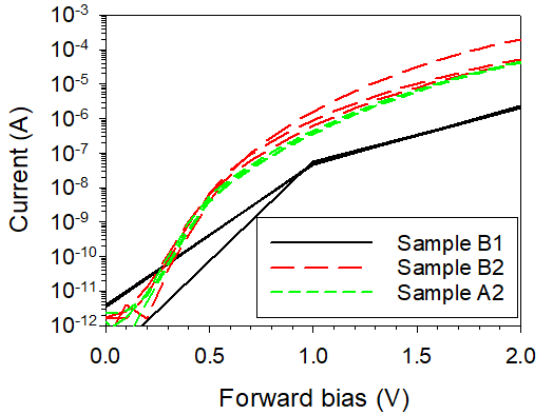

Fig. 4.7: Forward dark I-V data of the three samples. Devices have 20 μm diameter, P = 3 μm and varying S (4, 6 and 8 μm).

Room temperature reverse dark I-V data of sample B2 and A2 are shown in Fig. 4.8(left) and (right), respectively. Data presented were obtained from design variants of P = 3 and 5 μm in combination with S = 4 and 8 μm. Similar to the observations from Fig. 4.8, devices from a given sample exhibit similar dark current before breakdown, regardless of design variants but certain design variants introduce small variations in V_{bd} (up to ~ 3 V). For a given P, devices with S = 4 μm have larger V_{bd} than those with S = 8 μm (by 2 V). For a given S, V_{bd} values of devices with varying P (3, 4 and 5 μm) are indistinguishable.

Observing Fig. 4.8, reverse dark I-V data from both samples are indistinguishable prior to breakdown. There is however small variations in the V_{bd}, despite samples B2 and A2 have identical wafer structure and intended InP avalanche width. The small variations in the V_{bd} are attributed to small variations in avalanche widths in the fabricated devices (details in 4.3.2 and 4.3.3).

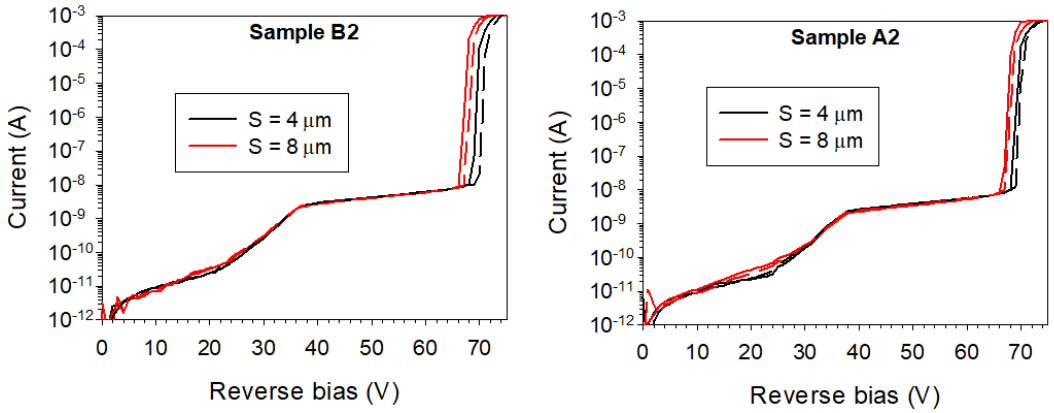

Fig. 4.8: Reverse I-V data of devices from samples B2 (left) and A2 (right) for the same S with different P (dashed line for 3 μm and solid line for 5 μm).

The additional dark currents observed in sample B2 are attributed to surface leakage mechanism(s), based on analyses of dark current data from different-sized devices. Dark current, dark current density (dark current divided by device's area) and dark current divided by perimeter from different-sized devices are plotted in Fig. 4.9. The results from different-sized devices are in closer agreement in Fig.

4.9 (right) than in Fig. 4.9 (middle). Hence, prior to breakdown, the dark currents are dominated by surface leakage current. As discussed in section 2.3.1, although the dark current has increased due to surface leakage, this should not affect the SPAD performance because the active region is far from the surface.

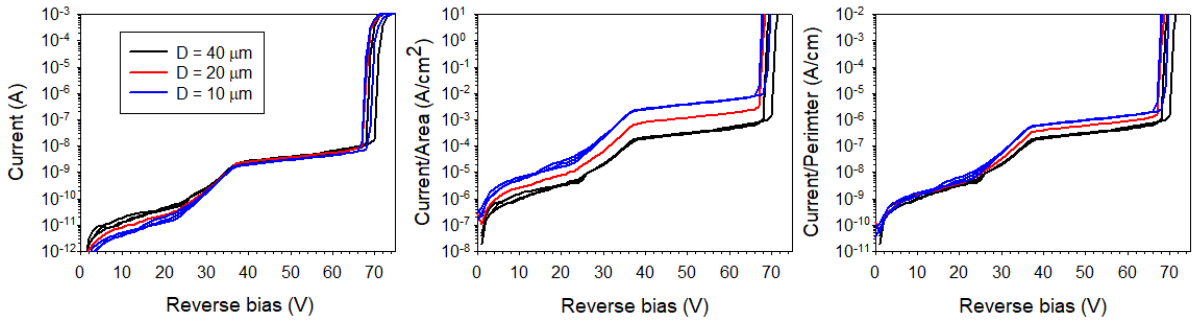

Fig. 4.9: (Left) dark current comparison between different sizes of device. (Middle) dark current density. (Right) normalised dark current with perimeter. Devices have the same S = 4 μm with various P (3 and 5 μm). For clarity, only data from sample A2 was presented.

4.3.2 SIMS

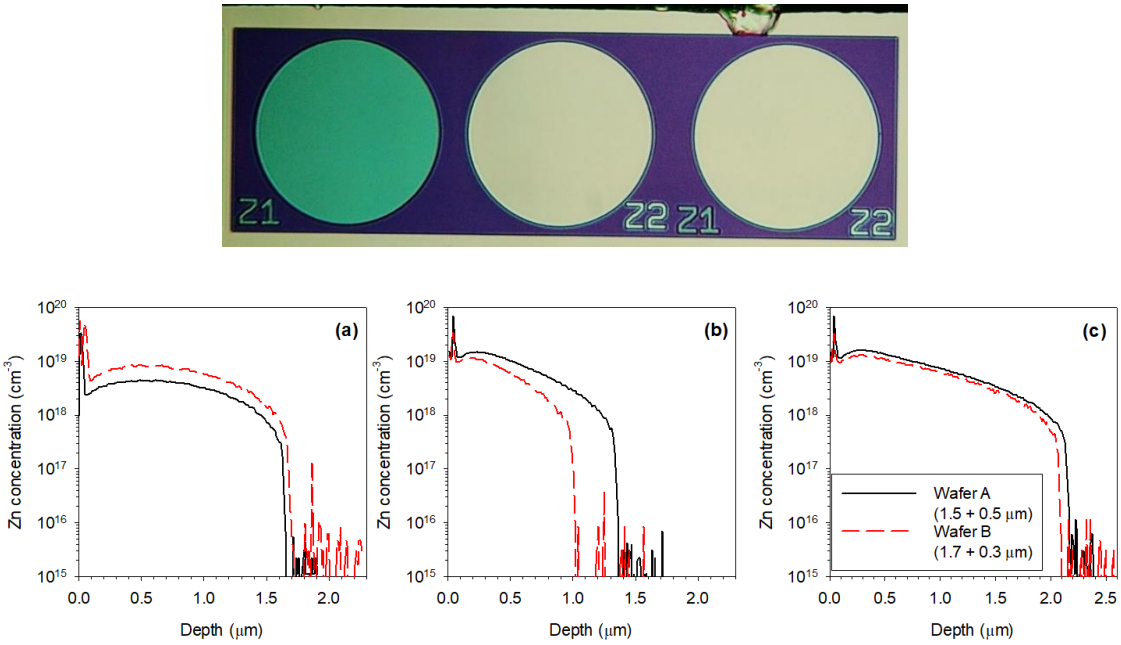

Fig. 4.10: (Top) Photos of three Zn diffusion apertures for SIMS. (Bottom) Zn profiles obtained from SIMS performed on wafer A and B for (a) Z1, (b) Z2 and (c) Z1+Z2.

Doping profiles of both wafers were extracted using SIMS by Loughborough Surface Analysis. SIMS was performed on designated Zn diffusion apertures with 200 μm diameter on the samples. These are apertures for first Zn diffusion only ('Z1'), second Zn diffusion only ('Z2'), and double Zn diffusion ('Z1+Z2'), as shown in Fig. 4.10 (top). Note that the photo showed the Z1 aperture covered in a thin SiN layer, which was excluded from SIMS data analyses.

Zn profiles of wafer A and wafer B are compared in Fig. 4.10. The double Zn diffusion depths achieved (using 1×10^{17} cm^{-3} as the threshold value) in wafers A and B are 2.15 and 2.08 μm, respectively, as shown in Fig. 4.10 (c). These are slightly deeper than the 2.00 μm intended. The actual InP avalanche regions in wafer A and wafer B are, therefore, slightly narrower than the intended value (0.85 μm and 0.92 μm cf. 1.0 μm). These led to slightly different V_{bd} in wafer A and wafer B observed in Fig. 4.8.

Detailed Si profiles of the n-charge sheets for both wafers are shown in Fig. 4.11. Although the Si concentration is higher than the 7.2×10^{16} cm^{-3} intended, it is worth noting that not all the Si atoms detected in SIMS are electrically active dopants (activated). Based on SIMS alone, the n-charge sheet doping is close to the intended design, albeit with some dopant diffusion.

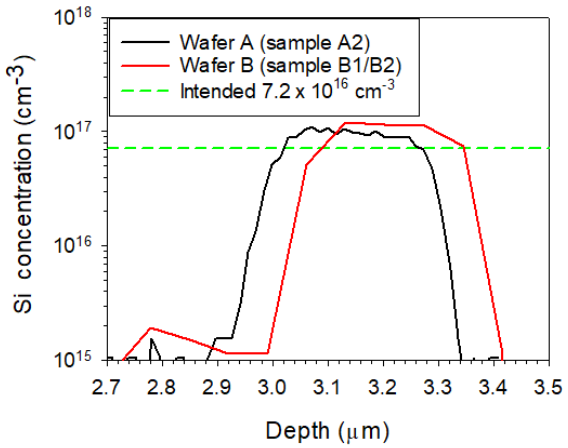

Fig. 4.11: Si profiles of n-charge sheets of wafer A and B obtained from SIMS.

4.3.3 C-V

To obtain more accurate experimental C-V data, the photolithography mask was modified to re-purposed the 'Z2' (deep diffusion only) and 'Z1+Z2' Zn diffusion apertures (200 μm diameter) meant for SIMS into large devices without FGR or Zn diffusion extension. Au/Zn/Au was deposited on the apertures as p- metal contacts. These were carried out on sample A2. C-V data from these large devices (without shallow Zn diffusion region and FGR) are shown in Fig. 4.12. With the increased junction area, the capacitance values are above the setup limit for the entire reverse bias range, improving the data quality considerably. For 'Z1+Z2', a sudden decrease in capacitance ~ -30 V was observed, which is consistent with the data from SPAD devices. The minimum voltage to fully deplete the InGaAs absorber (V_p) for wafer A and B are therefore -30 V. The C-V data from Z2 exhibited a larger V_p, as expected from its shallower Zn diffusion depth and hence wider InP avalanche region.

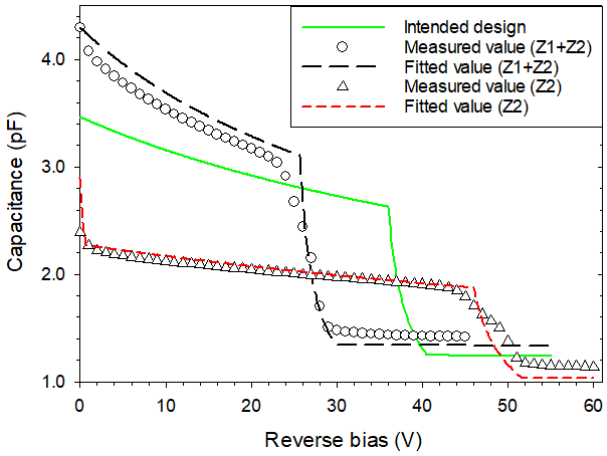

Fig. 4.12: (Symbol) experimental C-V of large devices with 200 μm diameter (re-purposed from 'Z1+Z2' and 'Z2') and (line) fittings for sample A2.

Fittings and the experimental results are in good agreement, suggesting an avalanche width of 0.8 μm and charge sheet doping density of 6.3×10^{16} cm^{-3} for devices with 200 μm diameter. The extracted avalanche width is close to the SIMS value (0.85 μm), as expected because the C-V data came from the same feature used in SIMS measurements. In addition, the fitted charge sheet doping density of sample A2 shows an agreement with those from sample B1, in line with SIMS data shown in Fig. 4.11. The extracted avalanche width values from these and earlier C-V fittings are summarised in Table 4.5. More C-V fitting data can be found in Appendix D.

Table 4.5: Comparison of avalanche width between SIMS and C-V fitting for three samples. C-V fitting used charge sheet layer thickness of 300 nm with 6.3 × 10^{16} cm^{-3} doping density.

Sample (wafer)	**Avalanche width from 200 μm devices**		**Avalanche width from 40 μm devices**
	SIMS (μm)	C-V fitting (μm)	C-V fitting (μm)
B1 (wafer B)	----	----	0.80 **(a)**
B2 (wafer B)	0.92	----	0.77 **(b)**
A2 (wafer A)	0.85	0.80 **(c)**	0.70 **(d)**

The electric field profiles for wafer A and wafer B were calculated using key wafer structure parameters in Table 4.5 at the corresponding V_{bd}. They are compared in Fig. 4.13, which also include the intended field profiles. For each wafer structure, the corresponding V_{bd} was the voltage at which peak electric field in the InP avalanche region reaches the associated breakdown electric field. The latter was calculated using a RPL model [5] and validated InP ionisation coefficients [6]. Since the experimental charge sheet doping is lower than intended, the peak electric field in InGaAs absorber at V_{bd} reaches upper design limit (165 kV/cm) for all wafer structures. Hence, band-to-band tunnelling from InGaAs is expected when reverse bias exceeds V_{bd}.

Overall, C-V and electric field analyses indicate that the electric field profiles deviate significantly from the intended design. The high field in the absorber will result in a significantly high DCR during SPAD

operation, so the APD is unlikely to function as a competitive SPAD, despite of the relatively low dark current prior to breakdown.

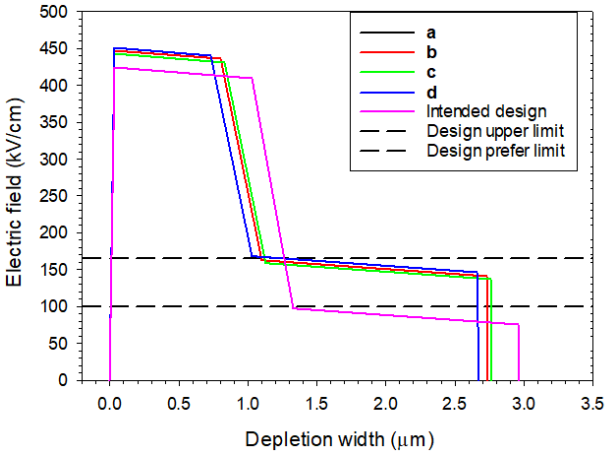

Fig. 4.13: Simulated electric field profiles of different wafer structures (from Table 4.5) for wafers A and B at associated breakdown voltage. Charge sheet thickness and doping density were 300 nm and 6.3 × 10^{16} cm^{-3}, respectively.

4.3.3 Avalanche gain measurements

Measurements of photocurrent data utilised the phase sensitive detection (section 3.3) and a 1.55 μm wavelength diode laser. Avalanche gain versus bias, $M(V)$, data were obtained by normalising the photocurrent data to the photocurrent value at APD's punch through voltage, V_p. Devices are labelled according to the guard ring spacing, S, and Zn diffusion extensions, P values. For example, a diameter of 20 μm APD with S = 4 μm and P = 4 μm is named D20_S4P4. For clarity, only experimental data of devices with 20 μm (D20) are shown below. For given S and P values, different-sized devices have similar I-V and V_{bd}.

To assess if the device suffer from PEB, the avalanche gain data are presented along with the dark current and photocurrent data in Fig. 4.14. The avalanche gain rises rapidly at the same voltage as the dark current and photocurrent data, indicating an absence of PEB for all S and P values.

Observing Fig. 4.14, for given P values, devices with S = 6 μm and S = 8 μm have a higher gain than devices with S = 4 μm at a given voltage. Moreover, $M(V)$ data of S = 4 μm devices are noticeably more abrupt than those of S = 6 μm and S = 8 μm devices. Abrupt $M(V)$ can sometime be caused by undesirable impact ionisation in the InGaAs absorber. However, additional simulations using the RPL model suggest that much higher electric field (> 300 kV/cm) in the InGaAs absorber is needed. Therefore, the abrupt $M(V)$ does not originate from the InGaAs absorber. In sample A2, the photocurrent

data of S = 4 μm devices also decrease with voltage at voltage between -50 and -60 V. The different trend of S = 4 μm devices are discussed in details later (Fig. 4.24).

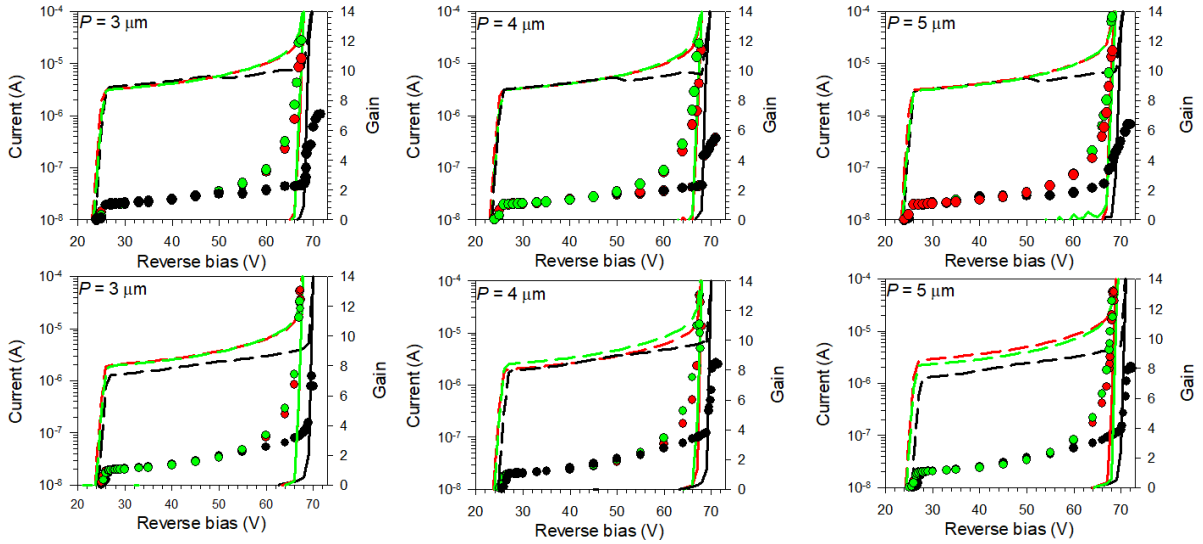

Fig. 4.14: Data of D20 devices in (top) sample A2 and (bottom) sample B2 for various S (black for 4 μm, red for 6 μm) and green for 8 μm) for a given P. The solid line shows the dark current and the dashed line shows the photocurrent with a 1550 nm laser illumination.

4.4 SPAD characterisation

Fig. 4.15 (left) shows the reverse dark I-V data at 200K, obtained from sample B2 using Janis ST-500 probe station (section 3.4). DUTs were biased below breakdown with a fixed peak-to-peak pulse height of 10 V, pulse duration of 20 ns, and a repetition frequency of 100 kHz. Fig. 4.15 (right) compares the dark count rate from several devices (all without optical window), which all exhibit high DCR values which gradually increase with overbias between 0.2 – 1.7 V, before rising again for overbias beyond 1.7 V.

The experimental values for overbias between 0.2 – 1.7 V are in broad agreement with DCR values predicted from solely InGaAs band-to-band tunnelling current, which are also shown in Fig. 4.15 (right). The predicated utilised the 1-D electric field estimated from C-V fittings and assumed either P_b of 0.1 or 1.0. The agreement confirms that both wafer A and B have undesirably high electric field in the InGaAs absorbers (165 kV/cm at breakdown) leading to undesirably high DCR values. The later increase of DCR with overbias (beyond 1.7 V) was attributed to afterpulsing.

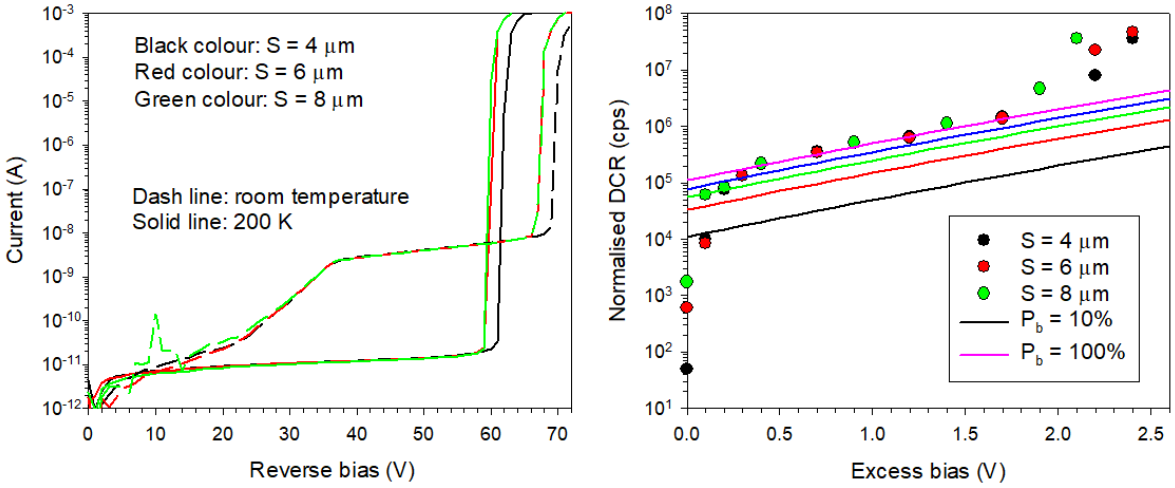

Fig. 4.15: (Left)dark current comparison between room temperature and 200K; (right) experimental DCR at 200 K from sample B2 (symbol) and simulated DCR from InGaAs BBT with various P_b assumption of 10, 30, 50, 70 and 100 %.

4.5 Simulation and analysis

Although samples A2 and B2 are unlikely to function as a competitive SPAD, the design of Zn diffusion profiles and FGR can applied to other planar InGaAs/InP APDs. Hence, further simulations and analyses focusing on the linear mode (not exceeding breakdown) are presented below.

2-D electric field simulations were carried out using commercial TCAD software Synopsis, based on a device structure simulation script originally developed by Dr S Dimler. The Zn diffusion profiles in the diffused p-region utilised experimental SIMS data (Fig. 4.10). The lateral Zn diffusion was assumed to be the same as the vertical diffusion. The charge sheet doping was assumed to be constant as 6.3×10^{16} cm^{-3} (from C-V fitting) and constant doping profiles were assumed for all other layers.

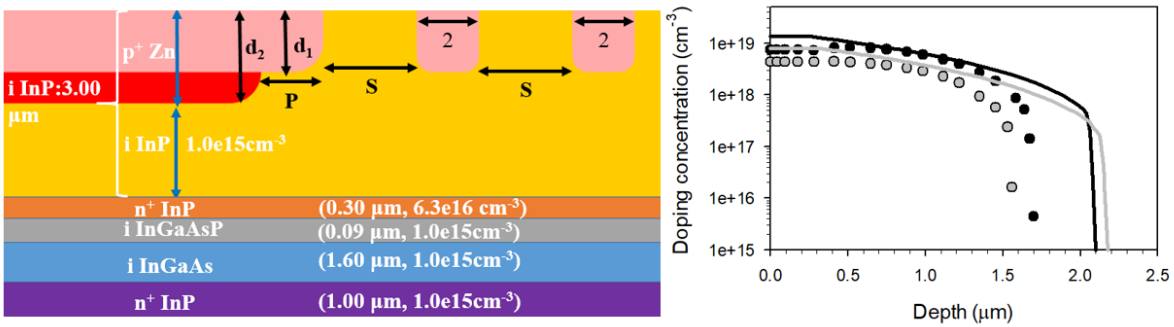

Fig. 4.16: (Left) wafer structure of active regions used in the simulation. (Right) Zn doping profiles from SIMS data were used in the simulations of waferA's shallow (grey symbols) and deep Zn-diffused regions (grey line). Zn doping profiles for wafer B (black symbol and black line) are also shown.

The simulation variables covered are summarised in Table 4.6. The two wafers have an identical structure within their active regions, hence identical bulk breakdown voltage. The breakdown electric field (E_{bd}) for a 0.8-1.0 μm thick InP avalanche region is 424 - 432 kV/cm, as calculated using InP

ionisation coefficients [6] and a RPL model ([5]). A breakdown field of 424 kV/cm (occurring at -70 V for both wafers) was used when comparing electric profiles from these TCAD simulations.

Table 4.6:Simulation variables for a given wafer structure.

Simulation variable	Value or range
Number of floating guard rings	0, 1 or 2
Zn diffusion depth, d_1 and d_2	1.7 and 2.0 µm (wafer A)
	1.5 and 2.0 µm (wafer B)
Guard ring spacing, S	1 - 8 µm, in step of 1 µm
Zn extension margin, P	2 – 5 µm, in step of 1 µm

Simulations of 2-D electric field profiles were carried out for each design at -70 V. From each 2-D plot, the electric field profiles along 3 points of interest, C1 to C3, were extracted, as illustrated in Fig. 4.17. C1 is within the active region and is representative of electric field profiles of the active region. C2 is at the edge of shallow diffusion (where the curvature effect tends to be prominent), whereas C3 is at the outer edge of FGR (for APDs with FGRs).

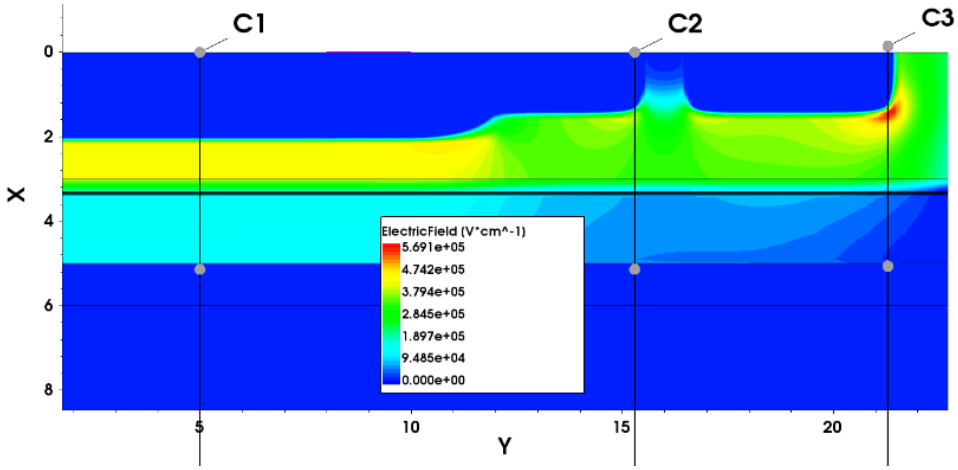

Fig. 4.17: Simulated electric field profiles of APD with a single guard ring (S = 4 µm, P = 4 µm) from wafer B. Points of interests are C1 (active region), C2 (edge of shallow diffusion), and C3 (outer edge of FGR).

Effects of FGRs

To observe the effects of FGRs, simulated electric field profiles along C1, C2 and C3 for APDs without and with two FGRs from wafers A P = 4 µm and S = 4 µm are compared in Fig. 4.18 (left) and (right), respectively. Observing C1 field profiles in Fig. 4.18, adding FGRs does not alter the C1 field profiles, because C1 is far from the edge of the active region. However, C2 field profiles are noticeably lower in the APD with FGRs than in those without FGRs. Also, C2 field profiles in APDs without FGRs are identical to C3 field profiles of APDs with FGRs, because electric field hotspots are pushed away from the active region when FGRs are present. The same observations apply to the wafer B field profiles shown in Fig. 4.19. Comparing Fig. 4.18, the simulated C2 profile in wafer A is lower than in wafer B. Therefore, the Zn diffusion depth combination (d_2/d_1) of wafer A (1.5/2.0 µm) is more effective in PEB

suppression than that of wafer B (1.7/2.0 µm), in line with design criteria of $d_1 \geq 1.5$ µm and $(d_2\text{-}d_1) \geq 0.5$ µm for planar InGaAs/InP APDs from [7].

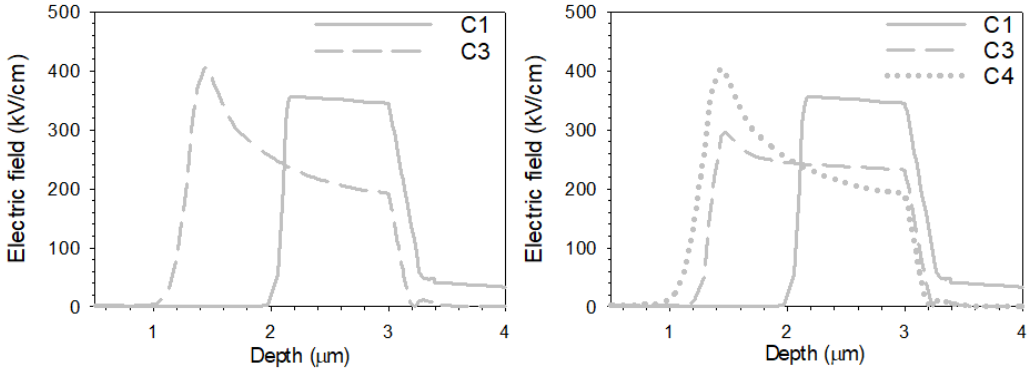

Fig. 4.18: Simulated electric field along C1, C2 and C3 for APDs (left) without and (right) with guard rings for wafer A at -70 V. S = 4 µm and P = 4 µm were used.

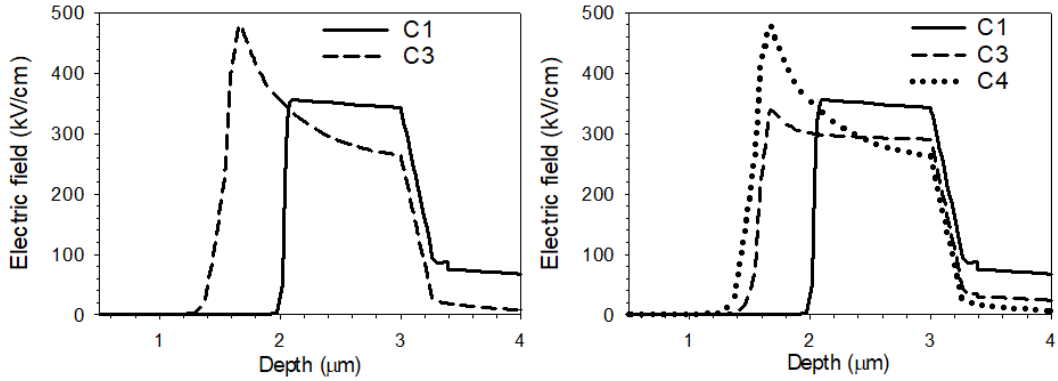

Fig. 4.19: Simulated electric field along C1, C2 and C3 for APDs (left) without and (right) with guard rings for wafer B at -70 V. S = 4 µm and P = 4 µm were used.

Effects of FGR spacing

Fig. 4.20 compares the C2 field profiles with S = 2 to 8 µm, using wafer A simulations with P = 2 and 5 µm. Electric field profiles along C1 are included for reference. The highly similar electric field profiles for the two P values suggests that varying P does not affect edge breakdown suppression.

In APDs with S < 5 µm, electric field profiles are lower along C2 than C1, so the APDs would avoid edge breakdown. As S exceeds 5 µm, the C2 field profile grows and eventually exceeds the C1 field profile, potentially causing edge breakdown. Similar electric field profile comparisons were made for wafer B and have yielded the same observations, as shown in Fig. 4.21. Base on the simulation, edge breakdown can be suppressed by FGRs, and the ring-to-junction should be smaller than 5 µm.

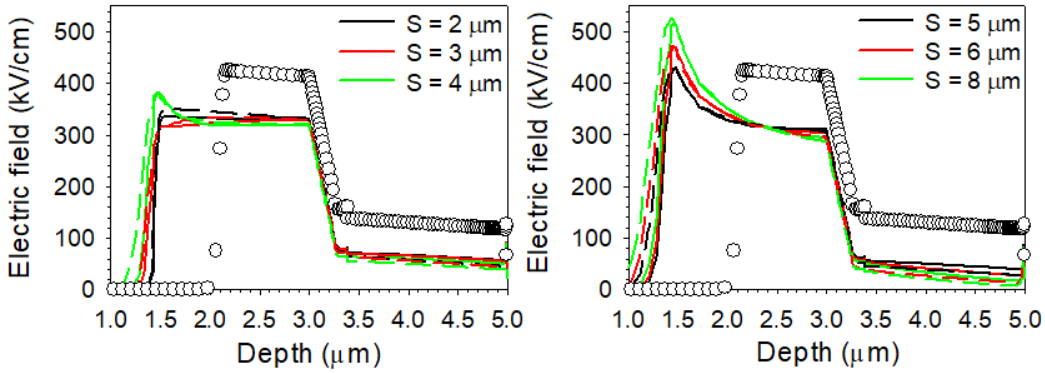

Fig. 4.20: Simulated electric field profiles along C1 (symbol) and C3 (solid line for P = 2 μm and dashed line for P = 5 μm) of different guard ring spacing (different colour) for wafer A at -70 V.

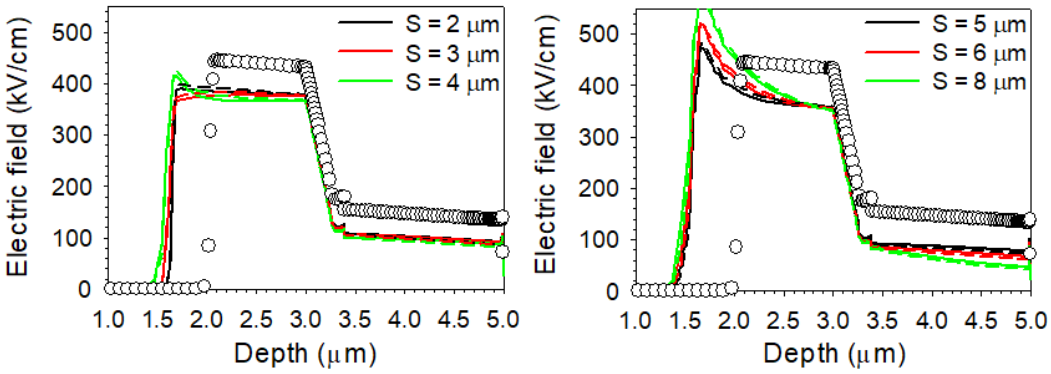

Fig. 4.21: Simulated electric field profiles along C1 (symbol) and C2 (solid line for P = 2 μm and dashed line for P = 5 μm) of different guard ring spacing (different colour) for wafer B at -70 V.

Fig. 4.22 compares the experimental $M(V)$ results for APDs with S = 4, 5, 6 and 8 μm from wafer A (left) and wafer B (right). Data for APDs with P = 5 μm are shown here. Simulated $M(V)$ results, which were obtained using a validated InP APD simulation model [6] for various avalanche widths (constant electric field across the avalanche regions was assumed) are also included. The experimental results are in agreement with simulated results for 1.1 μm avalanche width. The maximum gains that could be measured reliably were limited by the APD's current (dark current and photocurrent), which could become so large as to cause significant voltage drop across the series resistance used in the $M(V)$ measurement setup, reducing the actual reverse bias across the APD. Experimental gain values of APDs with $S \geq 5$ μm in both wafers increases abruptly at ~-67 or -68 V, whereas those of APDs with S = 4 μm continue to increase until measurements were limited by the voltage drop mentioned above. This indicates edge breakdown in the $S \geq 5$ μm APDs, consistent with the simulation results in Fig. 4.20 and Fig. 4.21.

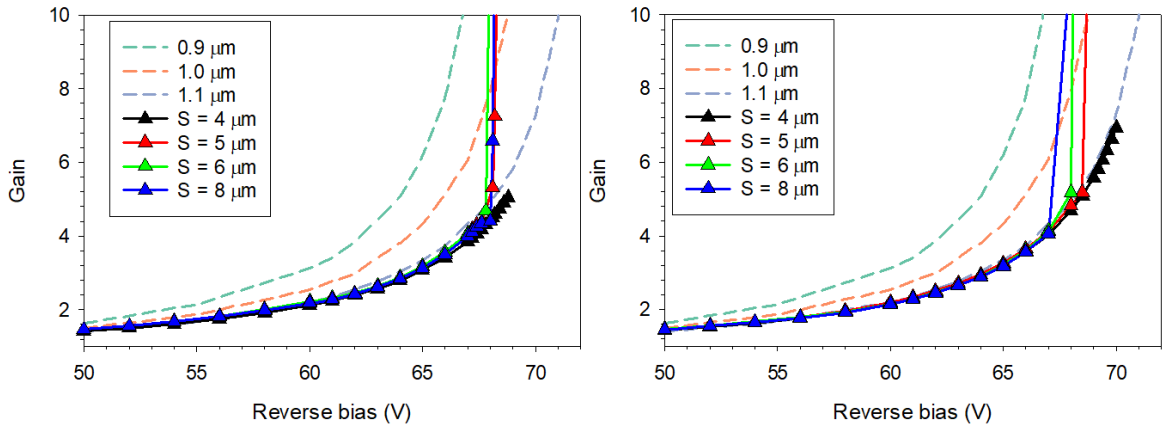

Fig. 4.22: Simulated (dash line) and experimental avalanche gain (symbol and line) of APDs with different S and P = 5 µm from wafer A (left) and wafer B (right).

The combination of simulation and experimental results confirms that FGRs do achieve edge breakdown suppression when appropriate spacing is used. The maximum working *S* values from experimental and simulation results are summarized in Table 4.7. Both wafers A and B show agreement despite the uncertainty/tolerance of the Zn diffusion depths and lateral accuracies.

Table 4.7: Comparison of maximum working FGR spacing from simulation and experiment data.

Wafer	**Maximum working FGR spacing (µm)**	
	Simulation	Experiment
A	$S < 5$	$S < 5$
B	$S < 5$	$S < 5$

Effects of Zn diffusion extension, P

Experimental V_{bd} versus guard ring spacing for a given *P* from two wafers are compared in Fig. 4.24 (left) and (right), respectively. The experimental V_{bd} was approximated by the voltage when the dark current reached 100 µA. For both wafers, there is a decrease of V_{bd} when S exceeds 4 or 5 µm for a given *P*, agreeing with observation in previous section. Regardless of FGR spacing, APDs with $P = 5$ µm exhibit slightly higher V_{bd} values for both wafers, suggesting that edge breakdown suppression is more effective with $P = 5$ µm. This differs from the observation from the simulated electric field profiles that $P = 2$ and 5 µm are highly similar field profiles (Fig. 4.20 and Fig. 4.21). The discrepancy between simulations and experimental results may be due to the simulation observation was limited to electric field profiles (as opposed to full I-V simulations). The favourable effect of increasing *P* is consistent with [8] where *P* was increase from 4 to 10 µm in planar SPADs. Considering both the experimental and simulation results, it is advisable to use $P > 4$ µm to ensure sufficient PEB suppression.

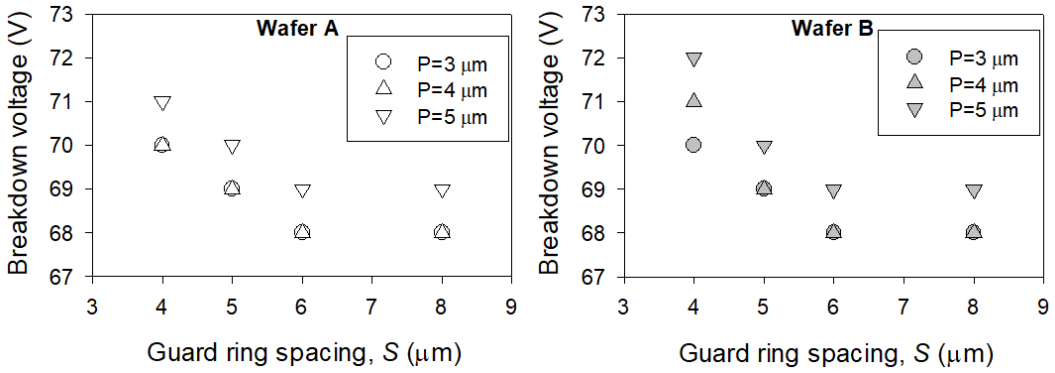

Fig. 4.23: Experimental breakdown voltage (from I-V results of 20 μm diameter APDs) versus guard ring spacing in wafer A (left) and B (right) as function of P.

FGRs and charge persistence

Although the APD's edge is covered by the metal to avoid side injection, a larger light spot can result in side injection due to the carrier's diffusion in the InGaAs. The APDs used were from wafer A with $P = 5$ μm and various S values. Avalanche gain decreases with reverse bias at ~ -63 V (before breakdown) in APDs with all S values (albeit M is small in some of the APDs). These are similar to decrease in photocurrent reported in [9], whose APDs were measured with a large white light illumination spot and the results were attributed to insufficient suppression of PEB. This was also observed in planar SPADs with FGRs [10], [11], though the data were not explained in detail.

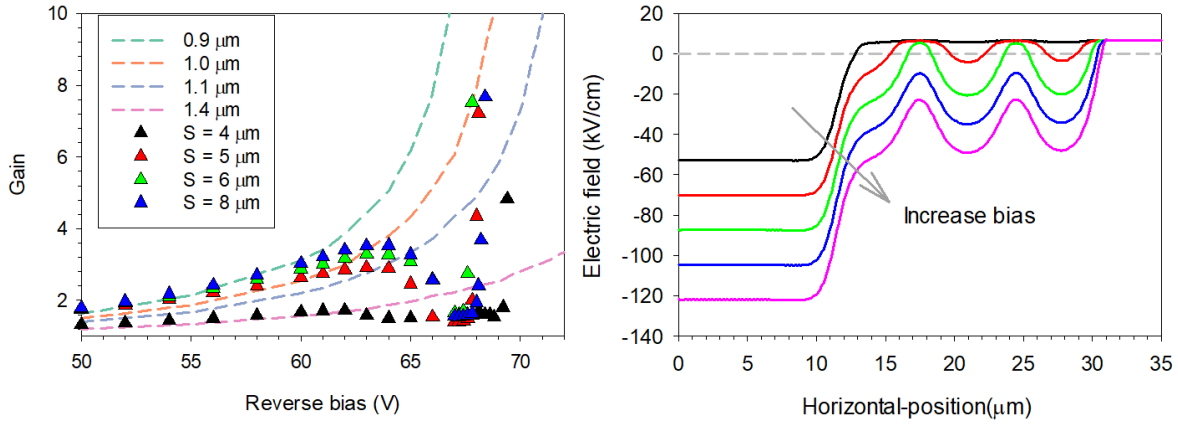

Fig. 4.24: (Left) experimental avalanche gain from side injection of APDs with different S and P = 5 μm in wafer A. (Right) simulated vertical electric field components at the InGaAs/InP heterointerface for wafer A with reverse bias ranges from -40 to -60 V, in a step of 5 V. APD has 20 μm diameter with S = 5 μm and P = 5 μm.

The avalanche gain measured with illumination far from the active region in Fig. 4.24 (left) are also much lower than those shown in Fig. 4.22. The difference can be explained using the charge persistence model from planar SPAD [25]. When reverse bias increases above certain values, presence of FGRs leads to non-zero values for vertical electric field component outside the active region, as shown in Fig. 4.24 (right). This increases the proportion of photogenerated holes in the thick InGaAs layer outside the active region overcoming the InGaAs/InP heterojuction barrier and enter the InP avalanche layer (still

outside the active region). The InP layer underneath the shallow Zn diffusion will produce a relatively small gain (< 2), much smaller than that produced by the active region.

4.6 Conclusion

Unfortunately, devices exhibit high DCRs due to lower charge sheet doping than the intended design. Hence, they do not function as competitive SPADs. The design rules of double Zn diffusion and FGR spacing on PEB suppression for planar APD were extracted in this work.

The optimum difference between Zn diffusion depths was confirmed to be $d_1 \geq 1.5$ μm and $(d_2 - d_1) \geq 0.5$ μm. To ensure FGRs can suppress PEB, their spacing was recommended to be ≤ 4 μm for 1.5 μm ≤ d_1 ≤ 1.7 μm. This work also advises increasing the Zn extension margin (i.e. beyond 4 μm) to gain further PEB suppression. Given the similarity between planar InGaAs/InP APDs and InGaAs/InP SPADs, the design rules identified above are likely to apply to the latter too.

4.7 References

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Chapter 5: InGaAs/InP Single Photon Avalanche Diode (Round 2)

5.1 Wafers and devices (wafers C, D, E and F)

5.1.1 Wafer design (wafers C, D, E and F)

Structure details of the Round 2 SPAD wafers C, D, E and F are presented in Table 5.1. They are similar to those of the Round 1 wafers (Table 4.2), except for the charge sheet layer and an additional 50 nm InGaAs contact layer on the top. The Round 2 wafers were designed to have double Zn diffusion depths of 1.5/2.0 µm in the undoped InGaAs and InP layer to achieve an avalanche width of 1.0 µm. Hence they are nominally more similar to wafer A than to wafer B of Round 1.

Table 5.1: As-grown structures of Round 2 wafers C, D, E and F.

Function	**Material**	**Doping (cm^{-3})** (± 20 %)	**Thickness (nm)** (± 10 %)
Contact	InGaAs	Undoped	50
Avalanche	InP		2995
Charge Sheet	InP	N (Si) 8.0×10^{16}	300
Grading	InGaAsP (1.03 µm)	Undoped	30
Grading	InGaAsP (1.17 µm)	Undoped	30
Grading	InGaAsP (1.35 µm)	Undoped	30
Absorber	$In_{0.53}Ga_{0.47}As$	Undoped	1600
Buffer	InP	N (Si) 1.0×10^{18}	1000
Substrate	InP (semi-insulating, Fe-doped)		

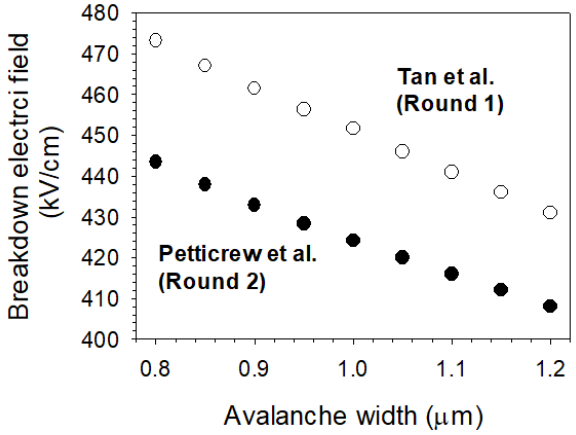

Fig. 5.1: Comparison of E_{bd} versus avalanche width characteristics simulated using the RPL model and InP ionisation coefficients from Petticrew et al. [1] for Round 2 and Tan et al. [2] for Round 1.

In the Round 2 wafers, the thickness of the charge sheet remains at 0.3 µm, but an increased doping density was requested for the wafer growth, following revised simulations of E_{bd} as a function of avalanche width using more recent and accurate InP ionisation coefficients from Petticrew *et al.* [1] instead of those of Tan *et al.* [2], as shown in Fig. 5.1. Updating the ionisation coefficients produced a slightly higher breakdown electric field for a given avalanche width, necessitating higher charge sheet doping density.

The updated P_b results and overall simulated DCR due to band-to-band tunnelling against the electric field in the InP avalanche region, as shown in Fig. 5.2 (a) and (b), respectively. **An avalanche width of 1.0 µm** still meets the DCR specification so it is retained the same in the Round 2 wafer design. In addition, the electric field limit for the InGaAs absorber in SPADs was rounded down to **150 kV/cm**, similar to the field limit for the InGaAs absorber in APDs. 1-D electric field simulations were carried out for the wafer structure of Table 5.1, yielding punchthrough voltage, breakdown voltage and electric field versus charge sheet doping, shown in Fig. 5.2 (c) and (d). Further 2-D electric field simulations using TCAD produced similar results, which are also plotted in Fig. 5.2 (right). The 1-D and 2-D electric field simulations indicate that the appropriate range of charge sheet's doping density is 6.75 - 8.95 × 10^{16} cm^{-3} and 6.55 - 9.25 × 10^{16} cm^{-3}, respectively. Therefore, the mid-point value of **8.00 × 10^{16} cm^{-3}** was chosen for the Round 2 wafer design. With these values, 1-D and 2-D simulations indicated V_p of -45 V. The expected V_{bd} from the 1-D simulation is -57 V, whereas the more spread out electric field profiles in the 2-D simulation yield slightly larger values of -60 V.

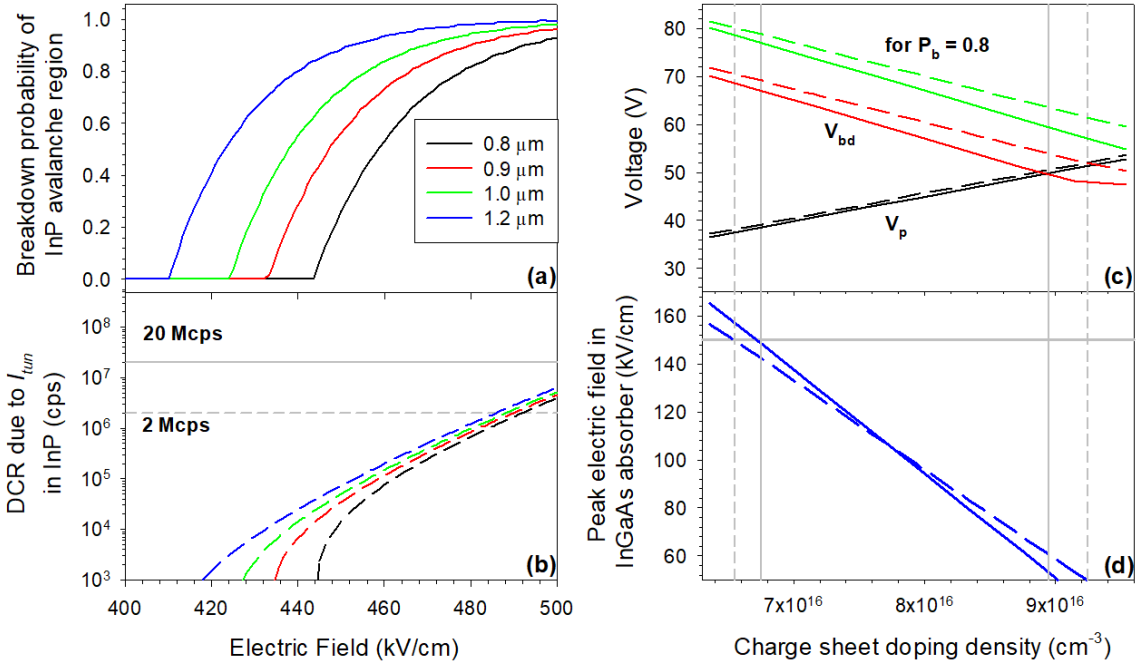

*Fig. 5.2: Simulated **(a)** avalanche breakdown probability for pure hole injection and **(b)** dark count rate (free running mode) versus electric field. Simulated **(c)** key voltages (V_p, V_{bd} and voltage to achieve P_b = 0.8) and **(d)** peak electric field in InGaAs absorber at P_b = 0.8 versus charge sheet doping density. The simulations were carried out using 1-D (solid lines) and 2-D electric field models (dashed lines) for wafer structure of Table 5.1.*

5.1.2 Wafers and samples

The four wafers (ZDCAPD- 54, 55, 58 and 59) were grown using MOCVD by LandMark Optoelectronics Corporation in a single growth run. Hence their nominal wafer structures were identical (Table 5.1). The design variants included in Round 2 photolithography masks are summarised in Table 5.2 (further details in Appendix B). In each unit cell of the new photolithography mask designs, two large D = 200 µm Zn diffusion apertures (shallow diffusion only named 'Z1' and double Zn diffusion named 'Z1+Z2') were retained to facilitate SIMS measurements. A series of four large, planar devices was added to facilitate accurate C-V measurements. Their diameters were 80, 100, 150 and 200 µm, designed with S = 4 µm and P = 5 µm. A further planar device without FGR and P = 4 µm was included as a reference device ('NGR').

Table 5.2: Device variables for photolithography mask.

Device variants	**Value or range**
Device diameter (D)	10, 20 and 40 µm
Zn diffusion extension (P)	4 and 5 µm
Guard ring spacing (S)	3 - 6 µm, in step of 1 µm
Number of FGR	1 and 2

A total of four samples (referred to as C1, D1, E1 and F1 hereafter) were fabricated from pieces of the four wafers. The fabrication process was the same as that used in Chap. 4, except for an additional etching step to remove the top InGaAs layer from the device's optical window (following the top (p^+) metal deposition). This was introduced to avoid unwanted photon absorption in the top InGaAs. Only the part of InGaAs layer within the optical window was etched. For devices with no optical window at all, their top InGaAs layers remained. Furthermore, Ti/Au was deposited for all the contacts. With p-InGaAs contact layer, using Ti/Au as the metal contacts would still yield acceptable ohmic contacts for the Round 2 samples (unlike Ti/Au on p-InP layer in Round 1).

5.2 APD characterisation (wafer C, D, E and F)

5.2.1 Uniformity of APD wafers

The dark I-V data at room temperature of the largest (D = 200 µm) and typical devices (D = 20 µm) without FGR from the four samples are compared in Fig. 5.3. For a given device diameter/variant, the data of different samples are indistinguishable. Prior to breakdown, the D = 20 µm devices exhibited higher leakage currents than D = 200 µm devices, suggesting that the dark currents of the former are dominated by surface leakage currents. Similar observations were made from the Round 1 devices. The D = 20 µm devices exhibited slightly lower breakdown voltages than D = 200 µm devices (by ~ 2 V),

suggesting that the larger devices have shallower diffusion depths (and hence wider avalanche width and larger V_{bd}), compared to the smaller devices. This too is consistent with observations in Round 1.

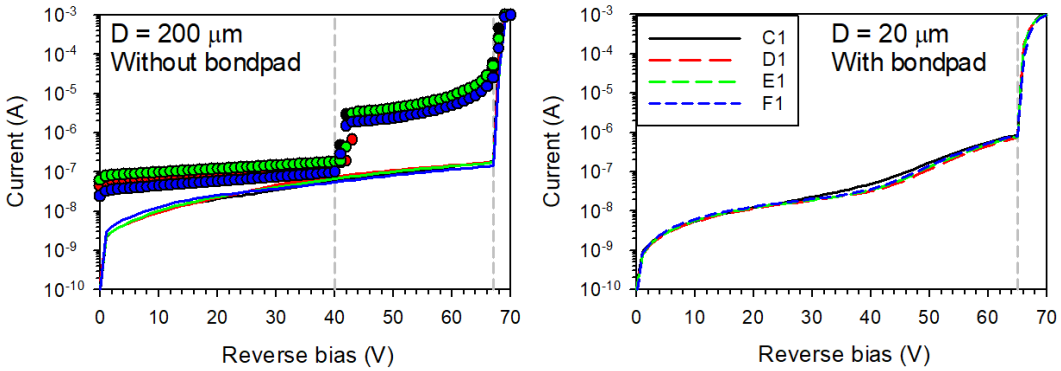

Fig. 5.3: Reverse I-V data of (left) 200 µm diameter devices with double FGRs and (right) 20 µm diameter devices without FGR from samples C1, D1, E1 and F1. Photocurrents of 200 µm diameter devices from white light illumination are also included (symbol).

Room temperature experimental C-V results of 200 µm diameter devices from the four samples are highly similar, as shown in Fig. 5.4. The experimental results are similar to the C-V characteristics expected from the wafer design, which is also plotted in Fig. 5.4. SIMS data of Zn diffusion and Si profiles from wafer C are shown in Fig. 5.5. The Si profile confirms the n-charge sheet doping is close to the intended value, as shown in Fig. 5.5 (right). Depths of the shallow ('Z1') and deep Zn diffusion ('Z1+Z2') however deviate from the desired values (1.5 and 2.0 µm). Hence, devices have a wider avalanche width than the intended 1.0 µm. This results in different values V_{bd} between the design (-57 V) and the experimental reverse I-V data (-65 V to -67 V), despite the similar V_p values.

Observing Fig. 5.3 and Fig. 5.4, the four samples show consistent dark current, V_{bd}, and capacitance for a given diameter, guard ring spacing, and Zn diffusion extension. Due to the excellent uniformity between the four wafers (from a single growth run), only the data from sample C1 are presented below for clarity, although measurements were also carried out on other samples.

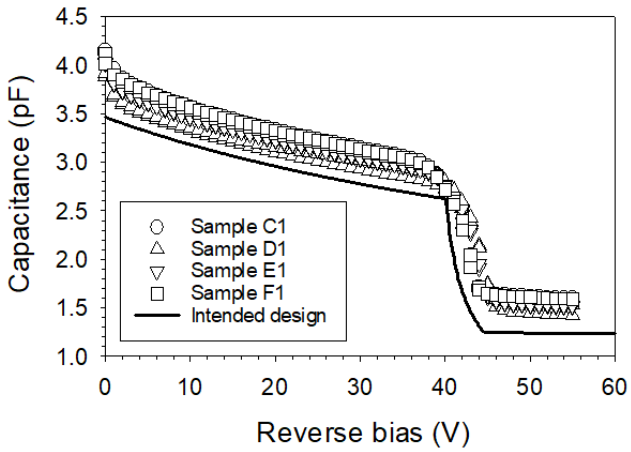

Fig. 5.4: Experimental (symbol) and expected (line) C-V data of 200 µm diameter devices from samples C1, D1, E1 and F1 are compared to the C-V characteristics from the design (structure in Table 5.1).

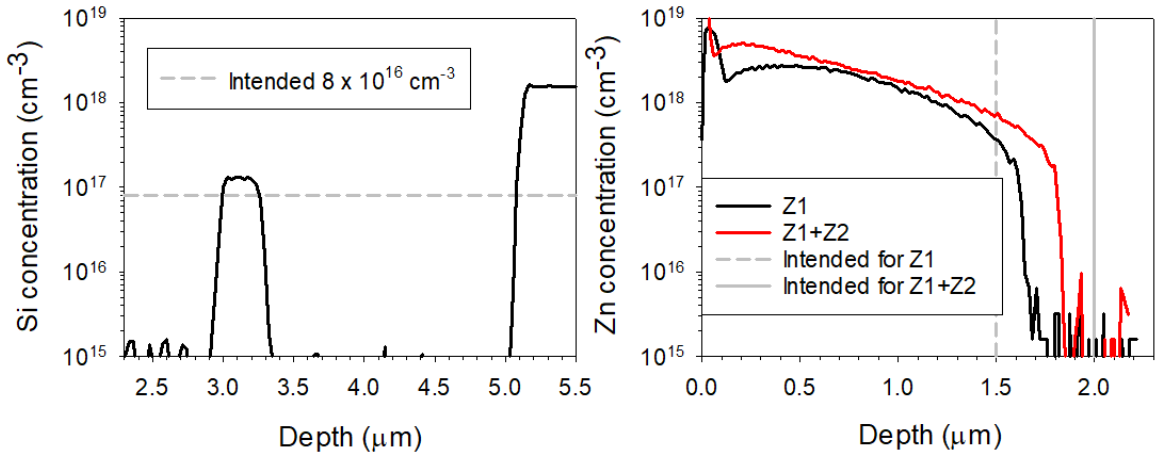

Fig. 5.5: SIMS data of (left) Zn and (right) Si doping profiles from wafer C.

5.2.2 Room temperature I-V data and C-V fittings

Room temperature forward I-V data obtained from sample C1 are compared to data from Round 1 (sample A1) in Fig. 5.6 (left). The additional InGaAs contact layer significantly improves the forward I-V characteristics by reducing the series resistance. However, sample C1 exhibited ~ 100 times higher reverse dark current before breakdown compared to sample A1, as shown in Fig. 5.6 (right).

Using an avalanche width of 1.15 μm (SIMS data in Fig. 5.5), a charge sheet doping of 7.1×10^{16} cm^{-3} and a charge sheet thickness of 300 nm, a good fit to C-V data of devices with 200 μm diameter can be achieved, as shown in Fig. 5.7 (left). The corresponding simulated electric field profiles, shown in Fig. 5.7 (right), indicate that the field in the InGaAs absorber will be < 150 kV/cm, when the devices are biased 10 V above breakdown (-65 V) to achieve a breakdown probability (0.8). Hence the desired doping profile has been achieved in Round 2, an improvement compared to Round 1.

However, based on the observations in Chap. 4 and prior works [3], the D = 20 μm devices have deeper Zn diffusion depth and hence smaller avalanche width. The experimental V_p from the photocurrent data (not shown here) for D = 20 μm devices is ~ -40 V. Electric field and capacitance calculations were repeated as functions of reverse bias. These utilised the charge sheet layer details from the C-V fitting of Fig. 5.7 (left) (300 nm and 7.1×10^{16} cm^{-3}) with the avalanche region width as the only adjustable parameter. Using an avalanche region width of 1.0 μm, the simulated V_p and V_{bd} values are similar to those of D = 20 μm devices (-40.1 and -63.8 V cf. -40 and -65 V). The deduced device structure is summarised in Table 5.3. Calculated C-V characteristics and electric field profiles are shown in Fig. 5.8 (left) and (right), respectively. The electric field in the InGaAs absorber will still be < 150 kV/cm at the voltage needed to achieve P_b = 0.8.

Table 5.3: Deduced devices structure for D = 20 μm devices.

Layer	Doping density (cm^{-3})	Thickness and depth (μm)
Zn diffusion	-	Assuming same as SIMS (d_1/d_2 = 1.7/1.85)
InP avalanche	-	1.0
n-charge sheet	7.1×10^{16} (from C-V fitting)	0.3
InGaAs absorber	-	1.6

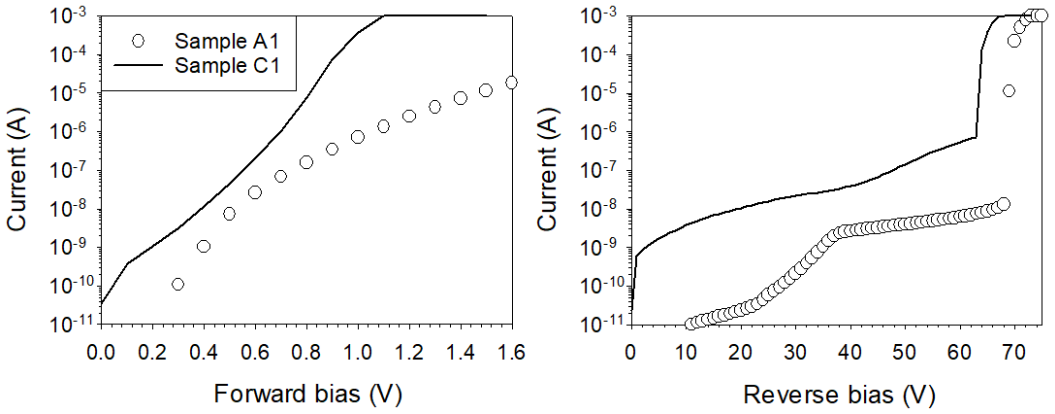

Fig. 5.6: I-V data of device with D = 20 μm, S = 4 μm and P = 4 μm from samples (line) C1 and (symbol) A1.

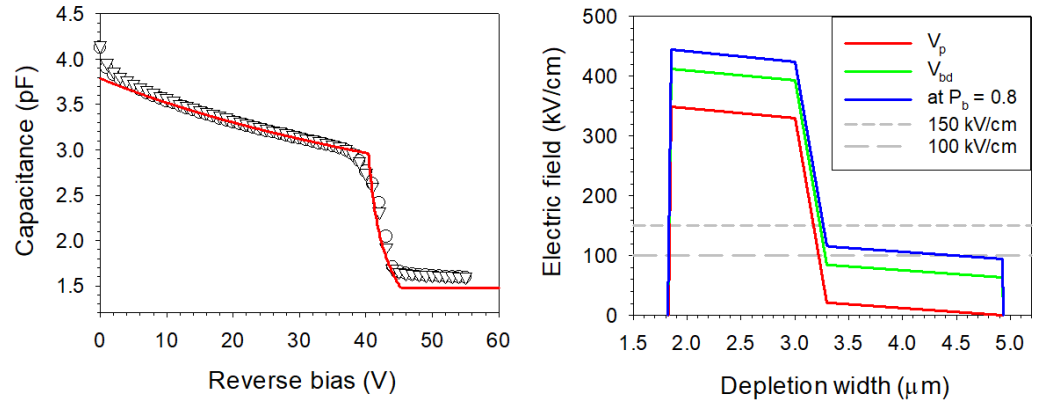

Fig. 5.7: (Right) experimental C-V data of sample C1 (symbol) and fitting (line) using 1.15 μm avalanche width, a 300 nm charge sheet layer doped with 7.1×10^{16} cm^{-3} for D = 200 μm devices. (Left) simulated electric field profiles based on C-V fitting for D = 200 μm devices.

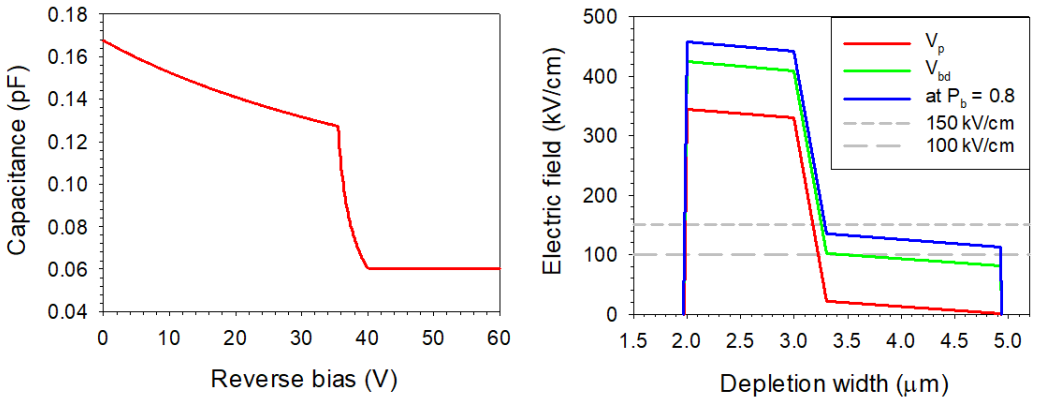

Fig. 5.8: (Right) simulated C-V data using 1.0 μm avalanche width, a 300 nm charge sheet layer doped with 7.1×10^{16} cm^{-3} for D = 20 μm devices. (Left) simulated electric field profiles based on the 1.0 μm avalanche width estimation for D = 20 μm devices.

5.2.3 Effects of FGR spacing and Zn diffusion extension

Reverse dark current data of 20 μm diameter devices with various S and P values in sample C1 at room temperature are compared in Fig. 5.9. Devices have similar V_{bd} and dark current regardless of S and P values. However, the V_{bd} of devices with S = 4 μm is smaller than or similar to those with S = 6 μm for a given P, opposite to the Round 1 observation (Fig. 4.28). Similar to Round 1, for a given S, the experimental V_{bd} of P = 5 μm devices is 1 V larger than those of P = 4 μm devices.

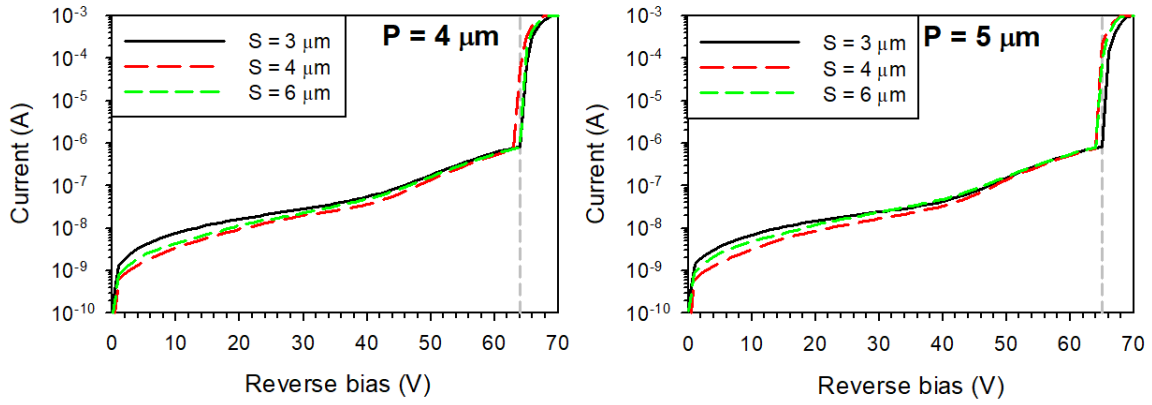

Fig. 5.9: I-V data of 20 μm diameter devices with double FGRs and different S and P = (right) 4 μm and (left) 5 μm from sample C1. Devices have no optical window.

Avalanche gain data obtained using a 1550 nm wavelength laser and phase-sensitive-detection method are shown in Fig. 5.10, along with their dark current data. For each device, breakdown voltages observed from $M(V)$ and I-V data are consistent, including those without FGR. This suggests a lack of edge breakdown in these devices, including those without FGR. A decrease in photocurrent was observed in devices with S = 3 μm, suggesting the FGR loses effectiveness when S > 3 μm in Round 2 [4]. For a given P, devices tend to have a higher gain with the increased S values, similar to the observation in Round 1. The 200 μm diameter devices exhibit a lower gain than 20 μm diameter devices for a given reverse bias since the former has a wider avalanche region.

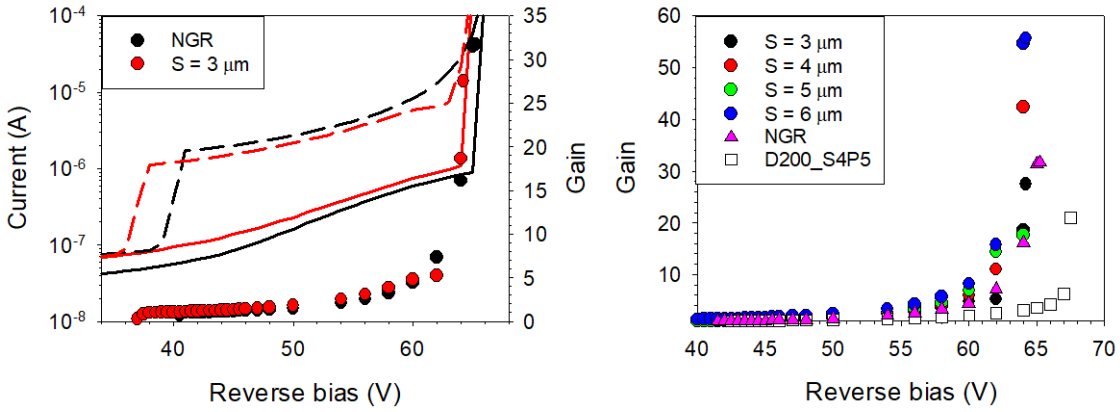

Fig. 5.10: Data from 20 μm diameter devices on sample C1. (Left) dark current (solid line), photocurrent (dashed line) and gain (symbol) versus reverse bias of devices without FGR and with double FGRs. (Right) gain data of devices P = 4 μm and various S values as well as 200 μm diameter devices.

5.5.4 2-D electric field simulations

2-D electric field simulations were carried out using commercial TCAD software Synopsis. The Zn doping profiles used are the parameterised forms of SIMS data from 200 µm diameter devices, as shown in Fig. 5.11. The Si doping density used was 7.1×10^{16} cm^{-3} from the C-V fitting. The shallow diffusion depth is deeper than intended (1.70 µm cf. 1.50 µm), whereas the deep diffusion depth is shallower than intended (1.85 µm cf. 2.15 µm).

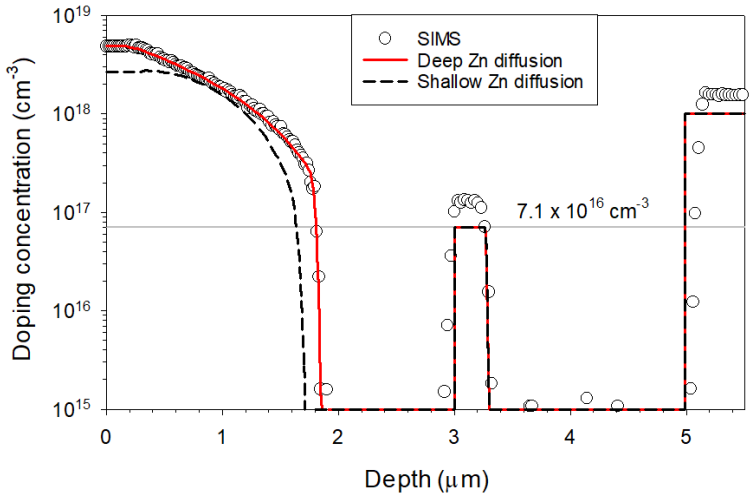

Fig. 5.11: Doping profiles of shallow (dashed line) and deep (solid line) Zn diffusion used in TCAD simulation were obtained by parametrising the SIMS data (symbol).

Fig. 5.12 compares the simulated electric field with S = 1 to 8 µm and P = 5 µm at -71 V, the voltage at which peak electric field in InP avalanche region reaches E_{bd} of 412 kV/cm for 1.15 µm InP at 290 K). When S > 4 µm, the field at the edge of shallow diffusion becomes larger than those in the active region, indicating ineffective FGR. The suggested maximum useful FGR spacing is $S \leq 4$ µm, similar to the observations from simulations for wafer A (Round 1).

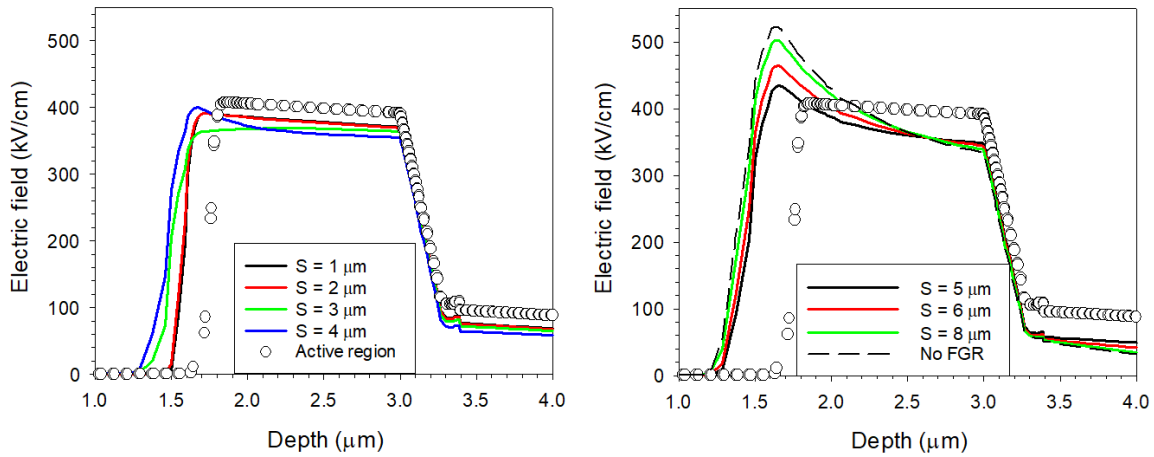

Fig. 5.12: Simulated electric field at active region (symbol) and at the edge of shallow diffusion (solid line) for different guard ring spacing (different colour) at -71 V.

Peak electric field values under and at the edge of shallow Zn diffusion from simulations using S = 1 to 8 µm and P = 5 µm are compared in Fig. 5.13. The electric field in the active region at breakdown voltage is also included as a reference. The electric field under shallow diffusion reaches E_{bd} with S > 4 µm at breakdown voltage. Also, S = 4 µm devices have similar electric fields under, at the edge of shallow diffusion and within the active region. Thus, S = 4 µm devices are effectively without the double-stepped diffusion junction and likely suffer from PEB.

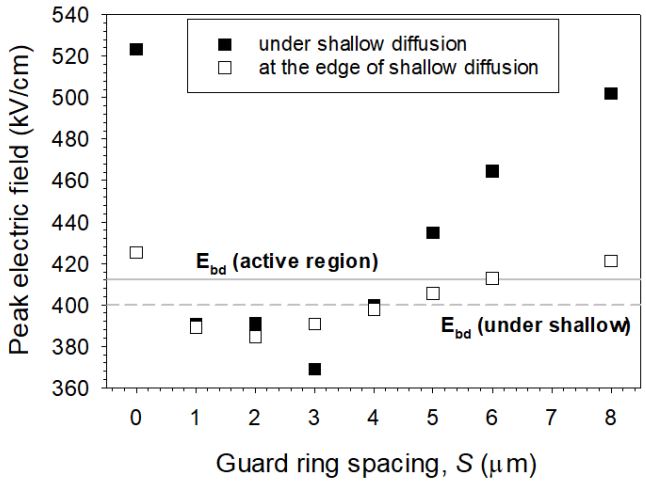

Fig. 5.13: Simulated electric field as a function of guard ring spacing under (black) and at the edge (white) of shallow diffusion for P = 5 µm at -71 V.

5.3 SPAD characterisation (sample C1)

To perform SPAD characterisation at different temperatures, it is necessary to know the temperature dependence of V_{bd}. Hence, dark I-V measurements for sample C1 were carried out at room temperature, 250 K and 200 K. The data are shown in Fig. 5.14. Dark currents decreased rapidly with decreasing temperature, suggesting that the measured dark currents are not dominated by tunnelling current, whose temperature dependence is very weak. For a given temperature, there is only 1 V variation in V_{bd} for different S and P. The V_{bd} decreases from ~ -67 to ~ -57 V as temperature decreases from 300 to 200K. The extracted C_{bd} was 0.10 V/K, similar to the reported values for APDs/SPADs with ~ 1.0 µm InP avalanche width (0.17 V/K [5] and 0.12 V/K [6]).

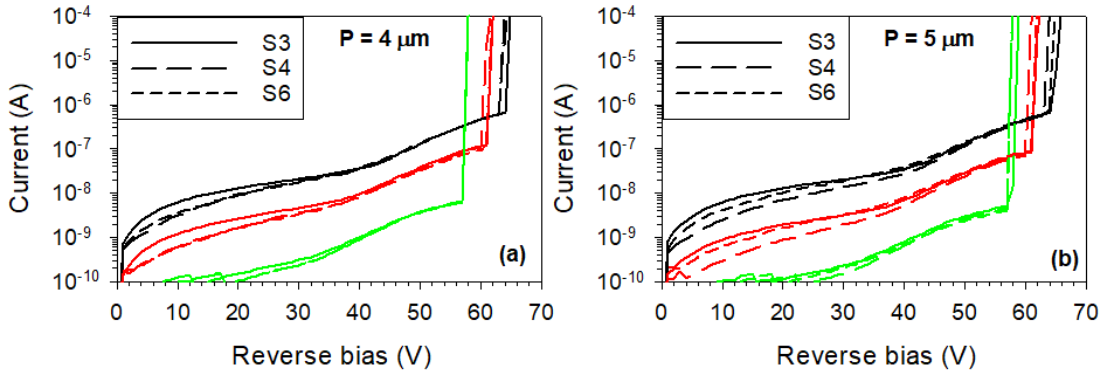

Fig. 5.14: Temperature dependent reverse I-V (black for room temperature, red for 250 K and green for 200 K) of 20 μm diameter devices without optical window and with S = 3, 4 and 6 μm. The devices have (a) P = 4 μm and (b) P = 5 μm.

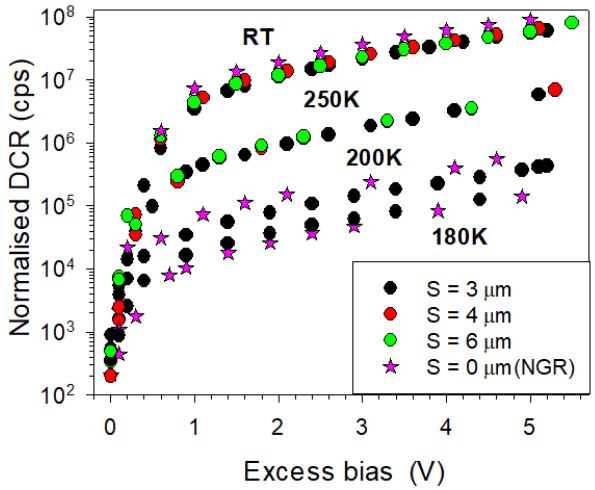

Fig. 5.15: Normalised DCR versus excess bias voltage at 180 K to room temperature. Data from devices with 20 μm diameter, P = 4 μm, double FGRs and various S.

Dark count measurements were performed on sample C1 using the Janis ST-500 probe station and the same measurement condition as Chap. 4 (section 4.4). The photon count data was obtained using heavily attenuated laser pulse with an average of 0.1 photon per pulse. Fig. 5.15 compares the DCR versus excess bias data from various devices as a function of temperature. For a given *T*, the DCR data of devices with different *S* values or even without FGR are indistinguishable. The DCR decreases as temperature decreases. Similar DCR versus excess bias characteristics were obtained from $P = 5$ μm devices (data were not shown for clarity). Fig. 5.16 (left) and (right) compare devices' raw dark and photon count with double FGR and single FGR at 200 K, respectively. The DCRs are unaffected by the number of FGRs (1 or 2), their spacing or the absence of FGRs. The photon counts rise above the dark count when $V_{ex} > 2$ V in all devices at 200 K, indicating the SPDE is also unaffected by the FGRs' designs.

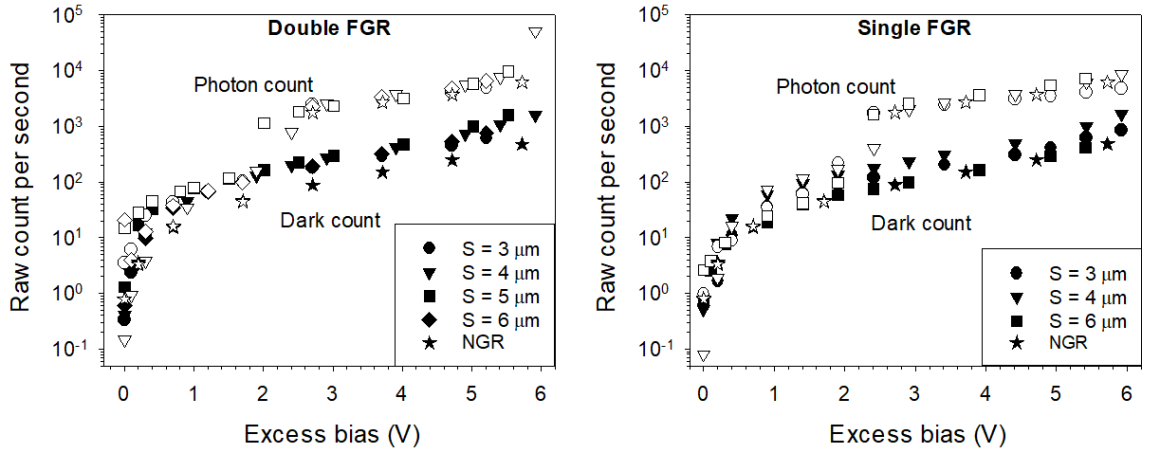

Fig. 5.16: Raw dark count and photon count (0.1 photon per pulse on average) for devices with (left) double FGR and (right) single FGR at 200 K. The devices have 20 µm diameter, P = 4 µm and different S. Devices without FGR are also shown for references.

DCR versus SPDE characteristics at 200 K of this work and reported values for planar InGaAs/InP SPADs are compared in Fig. 5.17. Although devices with different FGR's design (including those without FGRs) exhibit indistinguishable DCR, their SPDE versus excess bias characteristics vary, resulting in variation of their DCR versus SPDE characteristics. The DCR of this work obtained at 200 K is more than 100 times higher than the reported values obtained at slightly higher temperatures (225 to 243 K). Note that there was no AR coating on the devices, so the SPDE values of this work can potentially increase by up to 30 %.

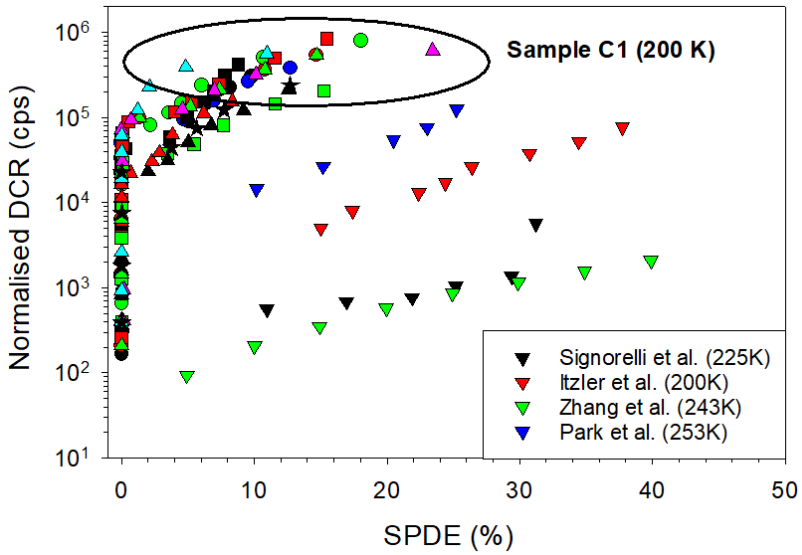

Fig. 5.17: Comparison of normalised DCR versus SPDE from sample C1 and other reports (Signorelli et al. [7], Itzler et al. [8], Zhang et al. [9] and Park et al. [10]).

5.4 Improved SPAD performance (wafer C)

5.5.1 Device design

To reduce the device's dark current, another fabrication round was carried out to remove the top i-InGaAs layer from more areas of the samples, such that only the area for p-metal contact retains the Zn-diffused InGaAs, as illustrated in Fig. 5.18. This was excepted to reduce diffusion-related dark current from the top InGaAs layer. The modified mask design and fabrication details are discussed in Appendix C. This yields C2 (test piece for fabrication) and C3 (main sample for characterisation).

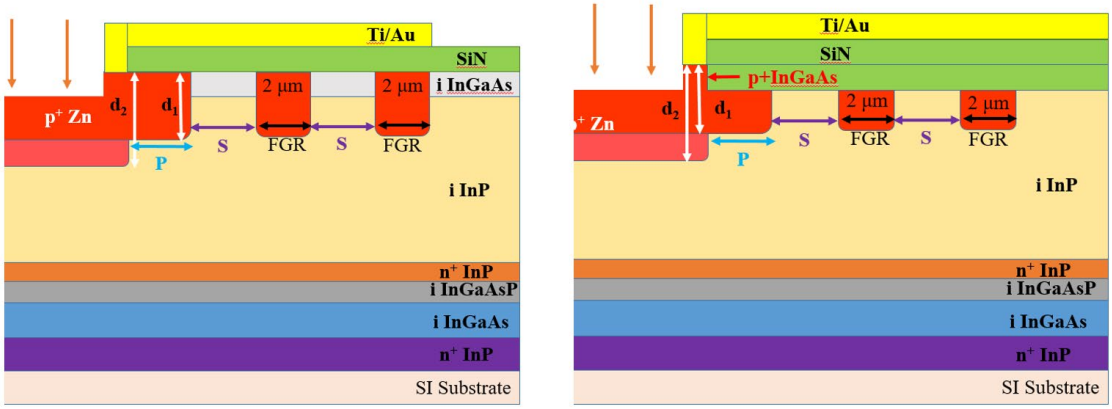

Fig. 5.18: Cross-sectional illustration of (left) sample C1 and (right) samples C2 and C3.

5.5.2 Experimental results (sample C3)

I-V measurements

Room temperature forward I-V data obtained from sample C3 are compared to data from sample C1 in Fig. 5.19 (left). Sample C3 exhibits currents that increase exponentially with forward bias without significant series resistance. Thus, it still benefits from the top Zn-diffused InGaAs. The reverse dark current of sample C3 is reduced from µA to nA levels, as shown in Fig. 5.19 (right).

Fig. 5.20 shows the reverse dark I-V data from 13 devices without FGR from different unit cells of sample C3. These devices have inconsistent dark currents, ranging from 5 nA to 1 µA, inconsistent with the uniform data in Fig. 5.19 (right). This is attributed to these devices without FGR suffering from the photolithography misalignment (~ 1 µm) during the fabrication process, which led to some unwanted i-InGaAs remaining on the top (followed by the top metal deposition), as illustrated in Fig. 5.21.

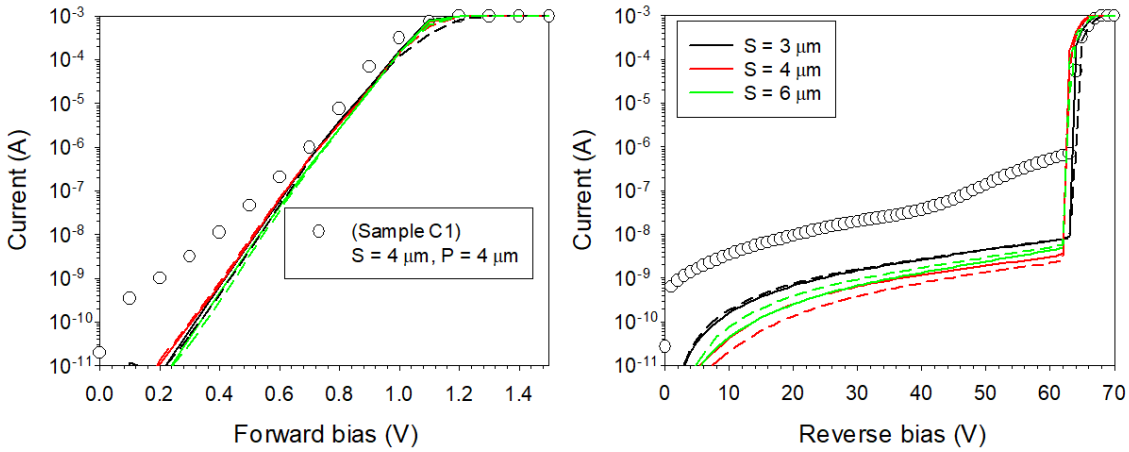

Fig. 5.19: (Left) forward and (right) reverse I-V of devices with various S and P (solid line for 4 μm and dashed line for 5 μm) values from sample C3. Devices have 20 μm diameter and without optical window. The data obtained from sample C1 was shown in symbol.

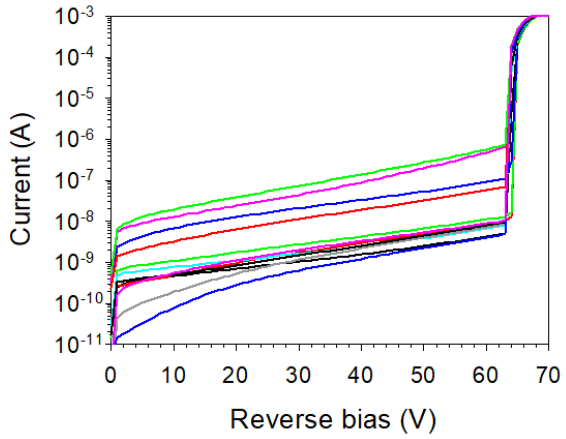

Fig. 5.20: I-V data of 13 devices without FGR from sample C3.

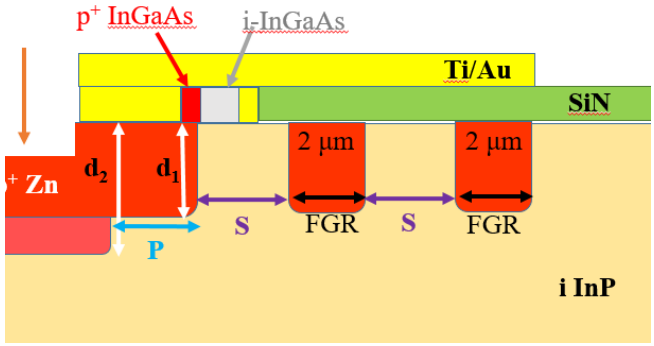

Fig. 5.21: Cross-section of fabricated devices in sample C3 with misalignment of InGaAs removal.

DCR measurements

For a given excess bias, DCR of sample C3 at 225 K is lower than DCR of sample C1 at 200 K, as shown in Fig. 5.22. This trend follows the reduction in reverse dark currents from sample C1 to sample C3. Therefore, the bulk dark current from the top InGaAs layer contributes significantly to the DCR values of sample C1.

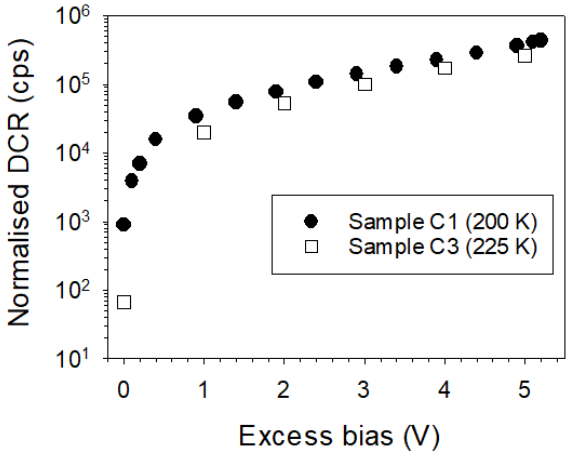

Fig. 5.22: Normalised DCR of devices with S = 3 μm, P = 4 μm and without optical windows from samples C1 at 200 K and C3 at 225 K.

The temperature dependence of DCR of sample C3 as a function of excess bias is shown in Fig. 5.23. Fitting the data yields DCR activation energy of 0.35 and 0.13 eV for 275 - 225 K and 200 - 150 K, respectively. The extracted E_a values are plotted against excess bias in Fig. 5.23 (right), along with extracted values from 275 – 150 K for references. For T = 225 to 275 K, the E_a of 0.35 eV is close to half of the InGaAs bandgap (0.75 eV), indicating that the primary DCR source is generation-recombination current in InGaAs. At lower temperatures (200 - 150 K), the much smaller E_a values suggest contributions from InGaAs tunnelling current (band-to-band, trap-assisted, or a combination of both) [8].

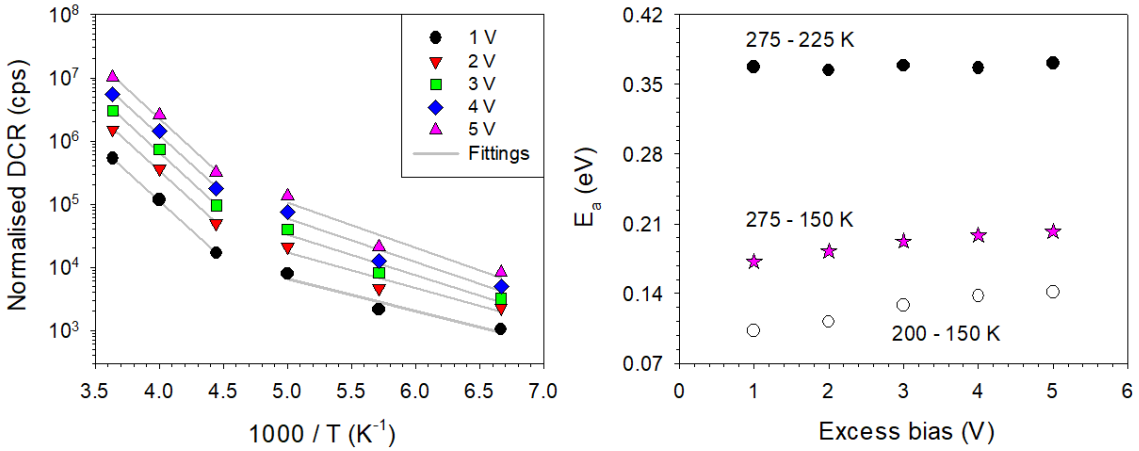

Fig. 5.23: (Left) DCR versus 1000/T (150 to 275 K), measured at 1 to 5 V excess biases for device S6P5D. (Right) extracted E_a for different excess bias at 150 – 275 K.

Fig. 5.24 shows the DCR versus repetition rate (from 10 kHz to 1 MHz) with an overbias pulse of 20 ns and 3 V magnitude. For < 200 kHz, the DCR remains constant with repetition rate, indicating that the DCR is not dominated by dark counts of the carriers trapped during previous avalanche events. Above 200 kHz, DCR increases sharply with repetition rate, suggesting that the afterpulsing effect becomes significant, especially at low temperatures. When using the repetition rate of 100 kHz (with 20 ns pulse width), the DCR is not affected by the afterpulsing effect.

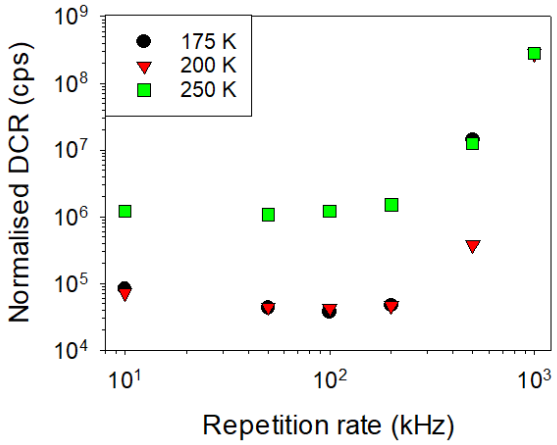

Fig. 5.24: DCR versus repetition rate for device S6P5D at different temperatures obtained using overbias pulse with 20 ns duration width and 3 V magnitude. Devices have no optical window.

The comparison of DCR data as a function of temperature for various S and P = 4 µm are presented in Fig. 5.25 (left). Data was obtained from devices without optical window. For a given temperature, DCR is indistinguishable (also for P = 5 µm, data not shown here). However, the DCR of devices with optical window is almost 10 times higher and exhibit more variation than those without optical window, as can be observed from T = 225 K data in Fig. 5.25 (right). The large variation is attributed to devices with optical window and P = 4 µm having unwanted InGaAs on the sample due to the photolithography misalignment (i.e. 1 µm), increasing the DCR. For devices with P = 5 µm and FGRs (as well as devices with P = 4 µm and without FGR), their DCR is similar to those without optical window, regardless of S values (data not shown here). Data of devices with a single FGR (not shown here) are also similar, suggesting no reduction in DCR is gained from the introduced FGR and the second FGR. These observations are consistent with those for sample C1 (Fig. 5.16). The same trend was observed in devices with optical window and single FGR for P = 4 and 5 µm (data not shown).

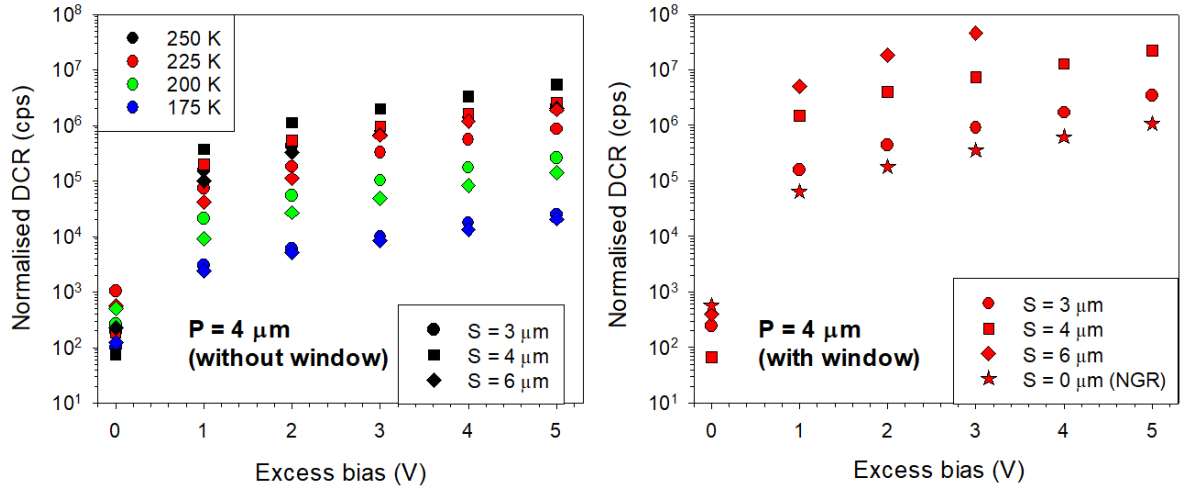

Fig. 5.25: DCR of devices without optical window at 175 to 250 K and (left) with optical window at 225 K (right). Devices have P = 4 µm and various S as well as devices without FGR.

SPDE measurements with averaged 0.1 photon per pulse

At 225 K, averaged SPDEs data obtained from two devices with double and single FGR for different S and P = 5 µm are shown in Fig. 5.26 (left) and (right), respectively. Devices with P = 5 µm and devices with P = 4 µm without FGR were chosen because their DCRs are less affected by the photolithography misalignment compared to P = 4 µm. The average SPDE data of devices without FGR were also included. For devices with double FGRs and without FGR, the SPDE increases with excess bias regardless of S. This is attributed to the increase of excess bias, yielding a higher P_b.

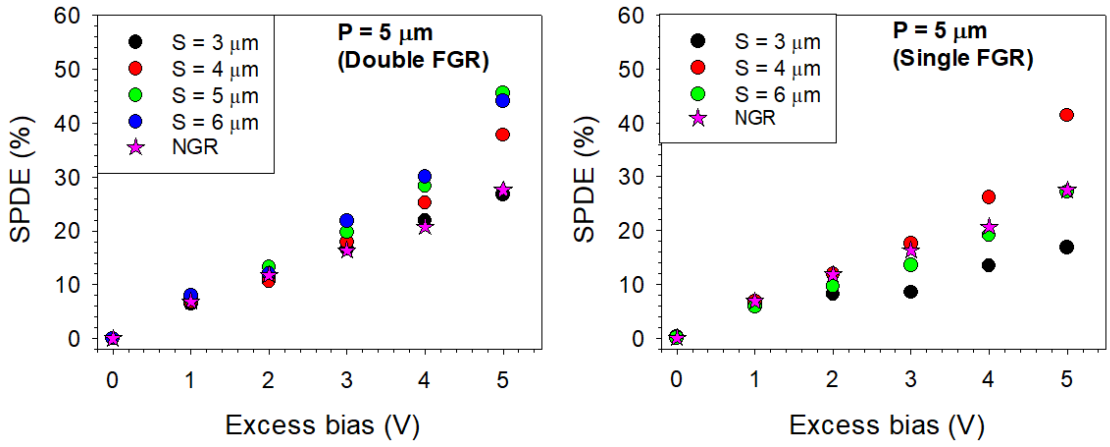

Fig. 5.26: Averaged SPDE from two devices with P = 5 µm, different S, double FGRs (left) and single FGR (right) at 225 K. Devices with P = 4 µm and without FGR were also included for references.

The DCR and SPDE of devices for different diameters and optically sensitive areas are compared in Fig. 5.27 (left) and (right), respectively. The devices used have S = 4 µm, P = 5 µm and double FGRs. Devices with different diameters show similar DCR, suggesting that the dominant mechanism(s) is not related to bulk dark current. Comparing same sized devices with different optical-sensitive areas, their DCRs are similar but their SPDE values differ. Devices with larger optical-sensitive area exhibit higher SPDEs than those with the smaller optically sensitive area (i.e. 30 % cf. 9 % at V_{ex} = 5 V), even after different coupling efficiency was accounted for. These SPDE observations are consistent with those from sample C1. The highest SPDE recorded was 45 %, with a DCR of 1 Mcps at 225 K. The experimental responsivity at unity gain is 0.76 A/W, which yields a quantum efficiency of 61 %, close to the 66 % expected for a 1.6 µm InGaAs (assuming no reflection loss). Therefore, devices will have a maximum theoretical SPDE of 61 %, higher than the experimental SPDE values.

The DCR density versus SPDE obtained from sample C3 are compared with other work in Fig. 5.28. DCRs of sample C3 are an order of magnitude higher than other planar InGaAs/InP SPADs at 225 K, but lower than those of InGaAs/InAlAs SPADs.

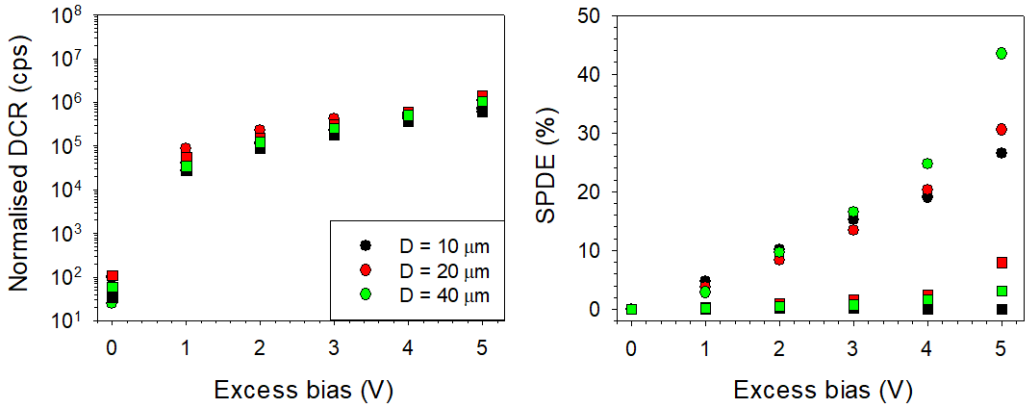

Fig. 5.27: DCR (left) and SPDE (right) versus excess bias characteristics of SPADs with different diameters (colour) and different bondpad design (circle for larger and square for smaller optical sensitive area).

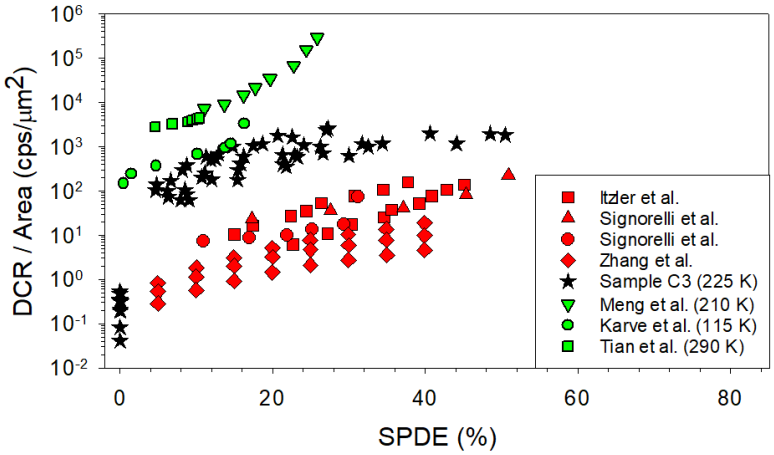

Fig. 5.28: DCR normalised to device's area versus SPDE from sample C3, other InGaAs/InP SPADs (red symbol) (Itzler et al. [8], Signorelli et al. [7], Zhang et al. [9] and Signorelli et al. [11]) at 225 K and InGaAs/InAlAs SPADs (green symbol) (Meng et al. [12], Karve et al. [13] and Tian et al. [14]).

5.5 1-D electric field simulation and analysis (wafer C, sample C3)

The calculated dark carrier rate versus electric field solely caused band-to-band tunnelling current in p-i-n diode with 20 µm diameter and a 1.0 µm InP avalanche width is shown in Fig. 5.29 (left), along with that for 1.6 µm InGaAs p-i-n diode. Combining 1-D electric field profiles from C-V fitting with the P_{be} obtained using recurrence equation and InP ionisation coefficient for 250 K [1], P_{be} versus excess bias characteristics as calculated for a SAM APD (deduce devices structure in Table 5.3). The product of dark carrier rate and P_{be} yield predicted DCR due to the InP avalanche region, as shown in Fig. 5.29 (right). The predicted DCR from the InGaAs absorber is omitted because the values < 10 for the excess bias range considered.

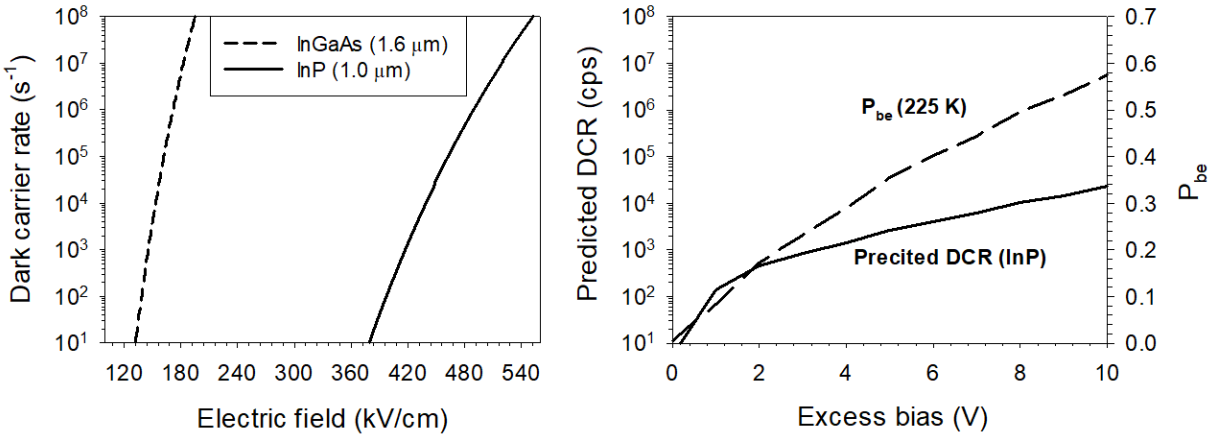

Fig. 5.29: (Left) Calculated dark carrier rate versus electric field from band-to-band tunnelling current of a 1.0 μm InP and a 1.6 μm p-i-n InGaAs. (Right) predicted DCR (solid line) using the simulated P_{be} (dash line) versus excess bias for InGaAs/InP SPADs at 250 K.

Fig. 5.30 (left) shows the simulated SPDE (with absorption efficiency of 0.61) versus excess bias characteristics at 250 K, which was calculated by converting the P_{bh} from an ideal p-i-n electric field into a SAM electric field. Assuming the electric field under the shallow Zn diffusion is uniform (of a 1.3 μm InP avalanche width), the rest of the layers are similar to those of the deduce devices structure (Table 5.3). The simulated SPDE versus excess bias data under shallow Zn diffusion was also included in Fig. 5.30 (left). The simulation suggested that the SPDE of under shallow Zn diffusion is insignificant when $V_{ex} < 5$ V, which is the range used in measurements. The simulated SPDE of active region and experimental SPDE versus excess bias are found to be in agreement, as shown in Fig. 5.30 (right).

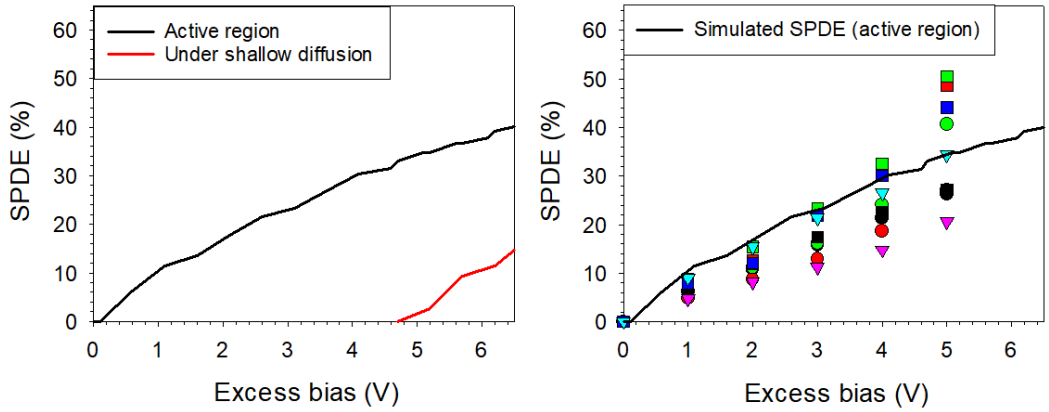

Fig. 5.30: (Left) simulated SPDE versus excess bias for SAM structure (Table 5.3) with 1.0 μm (active region) and 1.3 μm (under shallow Zn diffusion) avalanche width. (Right) experimental (symbol) and simulated (line) SPDE verse excess bias.

The simulated DCRs and SPDEs data at 250 K from Fig. 5.29 and Fig. 5.30 are summarised and compared in Fig. 5.31, along with experimental DCRs and SPDEs at 225 K from devices without FGR and with various FGR's design. Since the actual depletion region will increase by the shallow Zn diffusion and FGRs, simulated DCRs due to band-to-band tunnelling current in InP avalanche region with different diameters were introduced in Fig. 5.31 (left), ranging from diameters of 20 μm (for the

active region) to 62 μm (for devices with double FGRs, $S = 6$ and $P = 5$ μm). The experimental DCR versus excess bias characteristics are ~ 100 times higher than those of simulated DCR under the same trend, confirming that the experimental DCR is not dominated by BBT in InP. Therefore, the design of the wafer structure is valid.

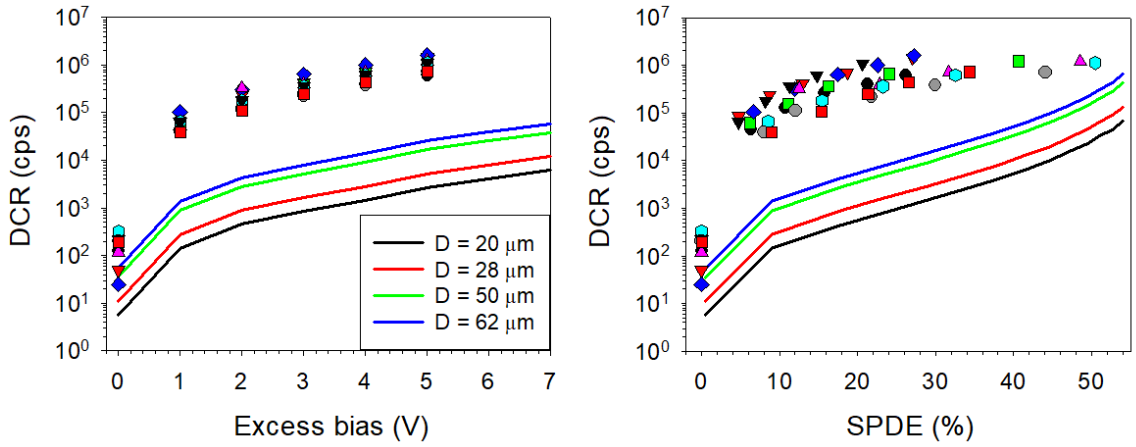

Fig. 5.31: Experimental (symbol) and simulated (line) DCR versus excess bias (left) and DCR versus SPDE (right). Experimental data was obtained at 225 K while simulation data was obtained using InP ionisation coefficient for 250 K.

Overall, both 1-D and 2-D electric field (shown in Fig. 5.13) simulations revealed that the excessive DCRs likely result from the edge breakdown. These explain the experimental observation in Fig. 5.27, which suggests the DCR is not dominated by the bulk dark current. The deviation of Zn diffusion depths can make the FGRs lose effectiveness, leading to PEB around the peripheral region. In this case, carriers can experience higher P_b, yielding higher DCR than expected. Although ref [7] suggested the breakdown of shallow Zn diffusion (electric field hotspot) will lead to a sudden increase of DCRs, this was not observed in this work within the measurement ranges.

To implement effective FGRs, it is vital to minimise the deviation of Zn diffusion depths, especially for the shallow Zn diffusion which formed the FGRs. Possible solutions could be: (i) implement the deep Zn diffusion first and then the shallow Zn diffusion to reduce the variation in shallow diffusion depth; (ii) increase the thickness of the top i-InP cap layer (from 3.0 to 3.5 μm) to allow more tolerance design for optimising Zn diffusion depth difference.

5.6 Conclusion

Planar InGaAs/InP SPADs from this work exhibit a higher DCR than the reported planar InGaAs/InP SPADs. Nevertheless, devices exhibit SPDE of up to 50% (without AR coating) with DCR of 1 Mcps at 225 K, better than reported state-of-art InGaAs/InAlAs SPADs.

Using experimental and simulation data of DCR and SPDE, this work supports the design rules of Zn diffusion profiles and FGRs extracted in Chap. 4 on PEB suppression for planar InGaAs/InP SPADs.

Although the simulation indicates that a single FGR is enough to effectively suppress PEB when their spacing ≤ 4 μm for d_1 = 1.5 μm, the experimental DCR results suggest otherwise. The DCRs are highly similar regardless of *P*, *S* and number of FGRs or the absence of FGRs. Further 1-D and 2-D electric field simulations revealed that the disagreement was caused by manufacturing tolerance in the shallow Zn diffusion depth. It resulted in insufficient difference in Zn diffusion depths with (d_2 - d_1) < 0.3 μm, instead of the 0.5 μm intended, leading to edge breakdowns for all devices regardless of FGRs. The poor performance of these devices illustrates the importance of appropriate stepped Zn diffusion profiles for PEB suppression.

5.7 References

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Chapter 6: Simulation of Novel InGaAs/InP SPAD Design

6.1 Improvements for planar InGaAs/InP SPADs structure

Unlike mesa InGaAs/InP SPADs, whose electric fields are mainly determined by their charge sheet layer's thickness and doping density, the electric field profiles of a planar InGaAs/InP SPAD are affected by the Zn diffusion depths. Therefore, variations of Zn diffusion depths result in uncertainties in the electric field profile, increasing the non-recurring engineering cost.

Ref [1] and [2] provide the design criteria for double Zn diffusion profiles in the planar InGaAs/InP SPADs to optimise the uniform electric field profiles without using the FGRs. They suggest the V_{bd} of shallow diffusion should be at least 10 V larger than the V_{bd} of deep diffusion, otherwise avalanche breakdown of shallow Zn diffusion will contribute to DCR. Recently, it was suggested that a wider and deeper shallow diffusion can mitigate the charge persistence effect and, hence, reduce the DCR [3].

A series of 1-D electric field simulations were carried out based on the design criteria from [2] for optimising the Zn diffusion profiles for double Zn diffusion planar InGaAs/InP SPADs without FGRs. Table 6.1 summarises the layer thickness and doping density used in the simulations. The charge sheet layer's thickness and doping densities were identical to Round 2 (Table 5.1). Typically, planar InGaAs/InP SPADs have a 3.0 or 3.5 µm InP cap. The value of 3.5 µm was chosen to allow a reasonably larger range of shallow Zn diffusion depths whilst having a 1.0 µm avalanche width (obtained by a deep Zn diffusion depth of 2.5 µm).

Table 6.1: Input for 1-D electric field simulation.

Function	Material	Doping density (cm^{-3})	Thickness (µm)
Deep Zn diffusion (d_2)	InP (p^+)	1.0×10^{18}	2.5
Avalanche	InP (i)	1.0×10^{15}	0.7 – 2.0 (under deep Zn diffusion) 0.7 – 3.0 (under shallow Zn diffusion)
Grading	InGaAsP (i)	1.0×10^{15}	0.03
Charge sheet	InP (n)	$(8.0 \pm 1) \times 10^{16}$	0.3
Absorber	InGaAs (i)	1.0×10^{15}	1.6
Cladding	InP (n^+)	1.0×10^{18}	---

The E_{bd} was calculated for various avalanche widths using the RPL model with InP ionisation coefficients at 290 K [4]. Both simulation models assumed the electric field is uniform. Coupled with 1-D electric field profiles, the V_{bd} was calculated for a given avalanche width and charge sheet layer's

doping density. Hence, the breakdown voltage difference (ΔV_{bd}) between shallow and deep Zn diffusion as functions of avalanche width was obtained.

The results are shown in Fig. 6.1 for the charge sheet's doping densities of $7 - 9 \times 10^{16}$ cm^{-3}. The red zones in the figure represent combinations of avalanche width and d_1 that achieve $V_{bd} \geq 10$ V. Using $V_{bd} \geq 10$ V, the range of viable d_1 increases with charge sheet doping densities for a given avalanche width. Increasing the doping densities in the charge sheet increases the red zone area, widening the viable range of d_1.

However, there are uncertainties around the charge sheet's doping density in practical wafer growth. Their effects on the viable d_1 range are illustrated using the Zn diffusion depths of Round 2 wafers, which are also included in Table 6.2. Although the Round 2 wafers have a 3.0 µm i-InP cap layer instead of the 3.5 µm used in the simulation, it is evident that the maximum viable d1 decreased by 70 %, which is significantly greater than the deviation between the design and actual values of d_1 (~ 16%). Therefore, although the deviation in the charge sheet's doping density is within the wafer growth tolerance of ± 20 % specified by the wafer foundry, the deviation might result in significant variation in the viable d_1 range.

There are also uncertainties around the Zn diffusion depths (specification of d_2 had a ± 0.1 µm tolerance). Based on simulation data of Fig. 6.1, wafer with 3.5 µm i-cap InP can ended up with a ΔV_{bd} ~ 2.2 V, reduced from 12.8 V due to deviation of d_2. Furthermore, the shallow Zn diffusion depths may increase during the second diffusion process needed to achieve a stepped diffusion profile, further increasing uncertainties in the actual Zn diffusion profiles.

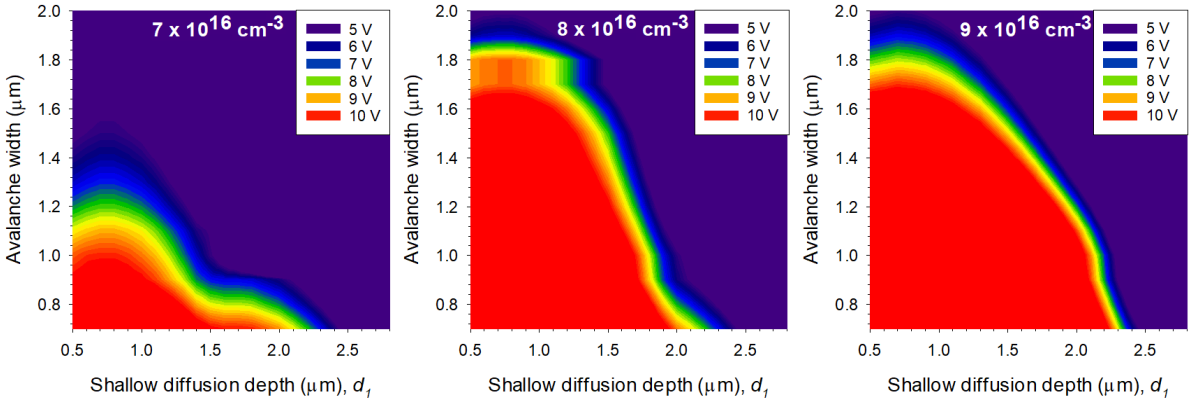

Fig. 6.1: V_{bd} difference as a function of avalanche width (0.7 – 2.0 µm, in step of 0.1) and shallow Zn diffusion depths (0.7 – 3.0 µm, in step of 0.1) for an InGaAs/InP SPAD with 3.5 µm i-InP cap layer, 0.3 µm charge sheet layer thickness and various charge sheet doping ($7 - 9 \times 10^{16}$ cm^{-3})

Table 6.2: Summary from Fig 6.1 with a 0.3 µm charge sheet layer and 3.5 µm InP cap layer for $\Delta V_{bd} > 10$ V.

Doping density (cm^{-3})	**Viable d_1**	**d_1**
7.0×10^{16}	0.5 – 1.0	1.75 (actual)
8.0×10^{16}	0.5 – 1.7	1.50 (design)
9.0×10^{16}	0.5 – 2.1	---

Assuming no PEB occurs by optimising the Zn diffusion depth difference based on the design criteria in [1] and [2], the actual electric field profiles can still vary from the intended design. This is attributed to the sensitivity of the electric field to the charge sheet doping despite the activated charge sheet doping being close to the intended design (maximum of ± 13 %). Since the diffusion depth will vary depending on mask opening for the same diffusion process [5], the active region's electric field between large and small diameter devices will differ, which was confirmed in Chap. 5. In addition, active region's electric field become even less predictable due to the tolerance (± 0.1 µm) afforded by the Zn diffusion technology, increasing the non-recurring engineering cost. Hence, apart from optimising the doping densities in n-charge sheet layer, it is important to minimise the effect of deviation in Zn diffusion depths on desired electric field in active region.

6.2 Proposed structure for InGaAs/InP SPADs

To relax the tolerance of Zn diffusion depths and obtain a uniform electric field close to the design, a new structure for planar InGaAs/InP SPADs is proposed. The proposed structure is inspired by the multiple mesas [6] and planar structures [7], [8] for InGaAs/InAlAs APDs/SPADs. An example of planar InGaAs/InAlAs SPADs is illustrated in Fig. 6.2.

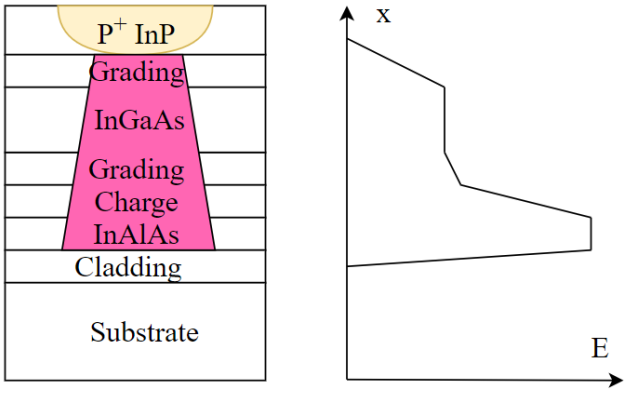

Fig. 6.2: Schematic of the cross-section of planar InGaAs/InAlAs SPADs [8].

6.2.1 Wafer structure

The proposed structure is illustrated in Fig. 6.3 and it shares some common features with the standard planar InGaAs/InP SPADs. In the proposed structure, the Zn diffusion depths no longer determine the avalanche width. Instead, an additional undoped InP layer is introduced as the actual avalanche layer, therefore uncertainties in Zn diffusion depths will not affect avalanche width. As a result, different-sized devices should have the same avalanche width. However, the Zn diffusion is still required to confine active region in the avalanche layer. Hence, the FGRs are included to further suppress the local field caused by the curvature effect after the Zn diffusion, minimising the impact ionisation process in the buffer layer. The field separation between the i-InP buffer layer and the avalanche layer is achieved by introducing another charge sheet layer with a different type (p^+) of doping.

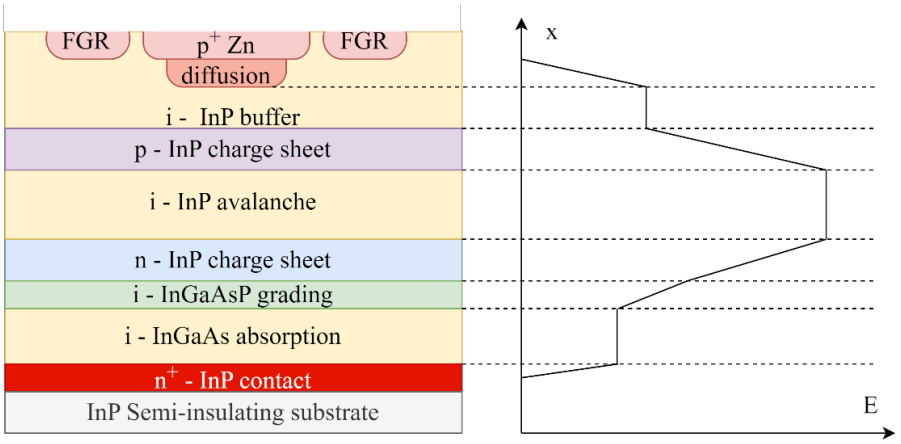

Fig. 6.3: Device diagram for the proposed structure and each layer's corresponding electric field.

6.2.2 2-D electric field simulation

2-D electric field simulations were carried out using commercial TCAD software Synopsis, modifying the device structure simulation script based on those for Round 2 (Chap. 5). The simulated wafer structure is summarised in Table 6.3. The undoped InP avalanche has a thickness of 1.0 µm, and the p-charge sheet layer has the same thickness as the n-charge sheet layer, which is 300 nm. Using 8.1×10^{16} cm^{-3} for n-charge sheet doping densities and 9.1×10^{16} cm^{-3} for p-charge sheet doping. The 1-D simulation of electric field profiles confirmed that the electric field would be < 100 kV/cm at the voltage for achieving $P_b = 0.8$.

Since the avalanche gain of a 1.0 µm thick InP p-i-n diode rises beyond unity for $E > 370$ kV/cm, the electric field in the InP buffer should not exceed 370 kV/cm to avoid unintended avalanche multiplication. The simulations used 1.0 µm for the buffer layer by modifying the deep diffusion from 1.85 µm to 2.0 µm, whereas simulated shallow Zn diffusion depth was retained at 1.7 µm from Round 2 SIMS data. They are compared in Fig. 6.4, whereas the overall doping profiles of the proposed structure are shown in Fig. 6.5. The lateral diffusion was assumed to be the same as the vertical diffusion.

The E_{bd} for a 1.0 µm thick InP avalanche and buffer layer is 424 kV/cm at room temperature (from Fig. 5.1). Hence, simulations of 2-D electric field profiles were carried out for each design at -78 V when the peak electric field in the InP avalanche layer reaches 424 kV/cm.

Table 6.3: Simulated (intended) wafer structure for 2-D electric fields simulation.

Purpose	Material	Doping density (cm^{-3})	Thickness (µm)
Zn diffusion	InP	Based on SIMS	(d_1) 1.7 / (d_2) 2.0
Buffer	InP	1.0×10^{15}	1.0
p-charge	InP	$- 9.1 \times 10^{16}$	0.3
Avalanche	InP	1.0×10^{15}	1.0
n-charge	InP	8.1×10^{16}	0.3
Grading	InGaAsP	1.0×10^{15}	0.09
Absorber	InGaAs	1.0×10^{15}	1.6
N+ contact	InP	1.0×10^{18}	---

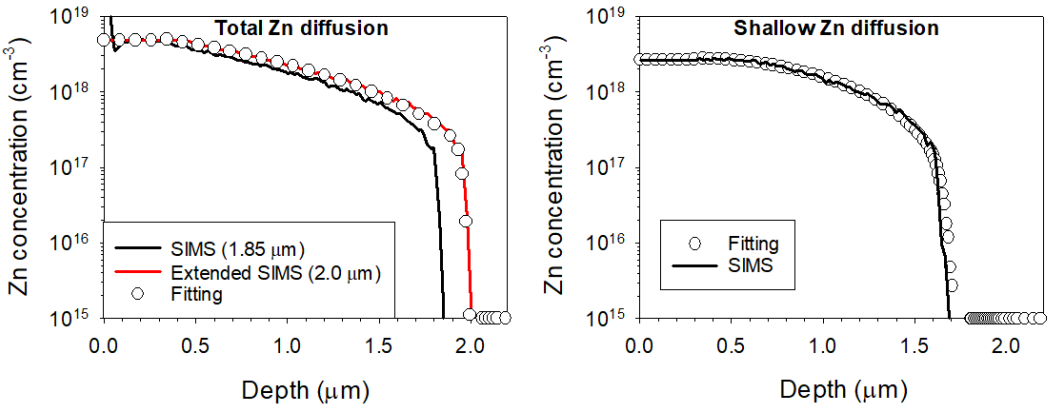

Fig. 6.4: Zn doping profiles of double Zn diffusion (right) and shallow Zn diffusion (left). The fitting doping profiles for 2-D electric field simulation were included as symbols.

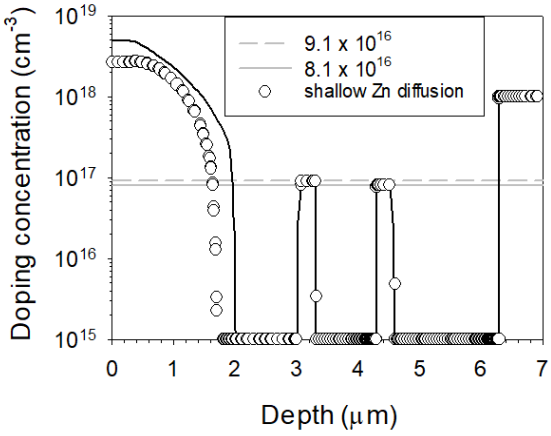

Fig. 6.5: Simulated doping profiles under deep (line) and shallow Zn diffusion (symbol) of proposed planar structure (Table 6.3).

The simulation variables covered are summarised in Table 6.4. From each 2-D plot, the electric field profiles along 6 points of interest, C1 to C6, were extracted, as illustrated in Fig. 6.6. C1 and C2 are

within and at the edge of deep Zn diffusion, respectively. C3 is at the edge of shallow diffusion (where the curvature effect tends to be prominent), whereas C4 is at the outer edge of FGR (for devices with FGRs). These are the same as in section 4.5. Interest points C5 and C6 are the mid-point within Zn-diffused InP buffer and i-InP avalanche layer, respectively. The active region (deep Zn diffusion) in the simulation has an intended 15 µm radius.

Table 6.4: Simulation variables for a given structure.

Simulation variable	Value or range
Number of FGRs	0, 1 or 2
Guard ring spacing, ***S***	2 – 8 µm, in step of 2 µm
Zn extension, ***P***	4 – 8 µm, in step of 2 µm
Doping densities of p-charge sheet	9.1×10^{16} cm^{-3} (± 20 %)
Doping densities of n-charge sheet	8.1×10^{16} cm^{-3} (± 20 %)

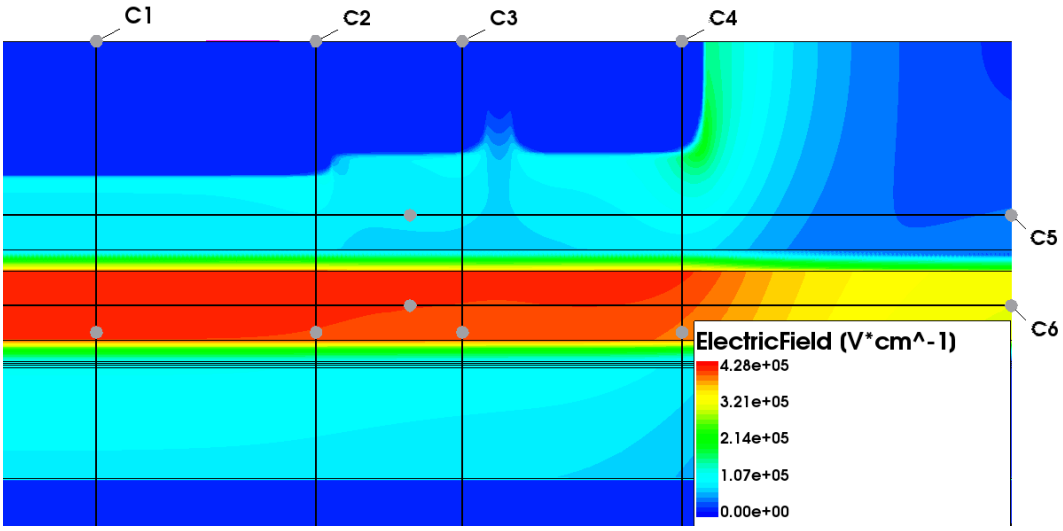

Fig. 6.6: Simulated electric field profiles of devices with a single FGR (S = 4 µm, P = 4 µm) at – 78V from the proposed structure. Points of interest are C1 (under deep diffusion), C2 (edge of deep diffusion), C3 (edge of shallow diffusion), C4 (outer edge of FGR), C5 (mid-point of InP buffer layer) and C6 (mid-point of InP avalanche layer).

Effects of FGRs (and their spacing)

To observe the effects of FGRs, simulated electric field profiles along C1, C3 and C4 for the proposed structure without and with two FGRs are compared in Fig. 6.7(left) and (right), respectively. The data shown are from devices with $P = 4$ µm and $S = 4$ µm. C2 field profiles are omitted due to their similarity to C1 profiles. Comparing the two plots in Fig. 6.7, the C1 and C3 electric field profiles are unaffected by the presence of FGRs. Adding FGRs only pushed the hotspot away from the deep Zn diffusion, leading to identical C3 and C4 field profiles in Fig. 6.7(right). This observation is consistent with earlier observations of the original planar structure (Fig. 4.23).

Fig. 6.8 compares the C3 field profiles with P = 4 µm and P = 8 µm for S = 4 to 8 µm. Electric fields along C1 are included for reference. The two P values have highly similar electric field profiles, suggesting that varying P does not influence the edge breakdown suppression, which is consistent with the observation for the original planar structure. When S > 4 µm, the C3 field profiles start to exceed the C1 field profiles (for depth < 3 µm), which is highly undesirable. However, Fig. 6.7 and Fig. 6.8 show that the C3 field profiles are significantly lower than C1 field profiles regardless of the FGRs and their spacing, differing from those for the original planar structure. This is attributed to the high field in the avalanche layer controlled by a p-type charge sheet layer. The low electric field profiles of the buffer layer (depth < 3 µm) along C3 suggest that FGRs are unnecessary for the proposed structure to suppress the edge breakdown caused by the curvature effect after the Zn diffusion.

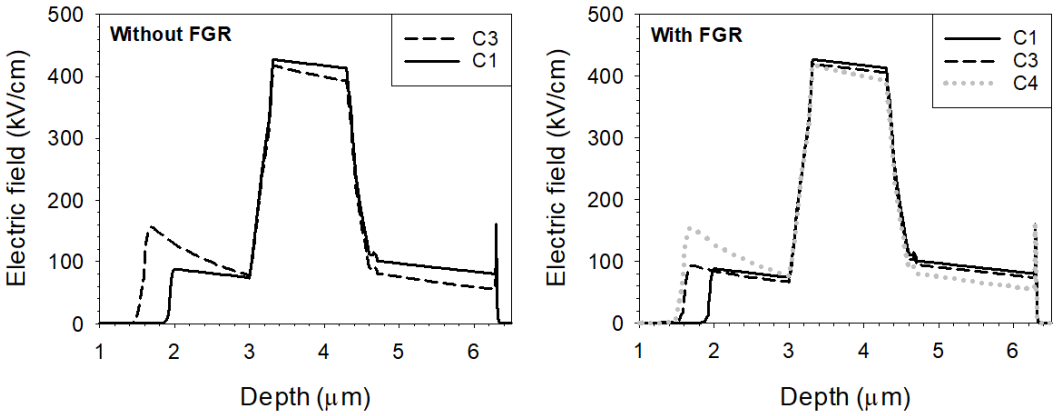

Fig. 6.7: Simulated electric field along C1, C3 and C4 for devices without (left) and with (right) FGR for the proposed structure at -78 V. S = 4 µm and P = 4 µm were used.

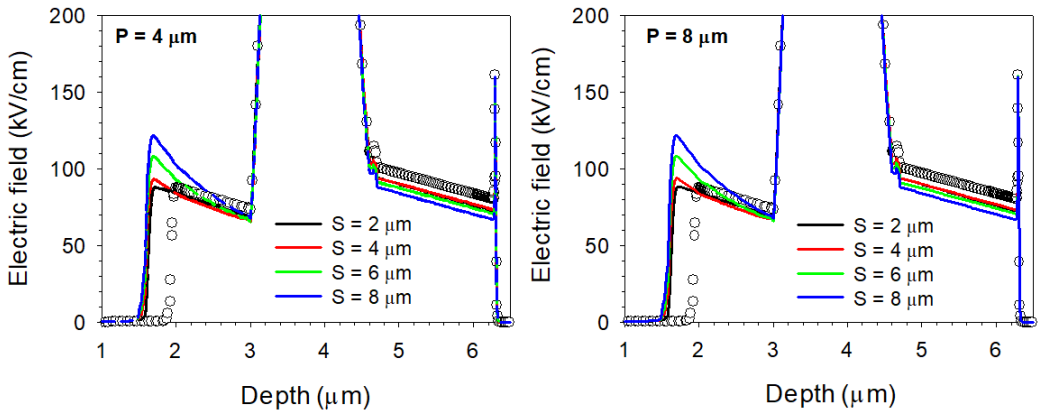

Fig. 6.8: Simulated electric field profiles along C1 (symbol) and C3 (solid line) of devices at -78 V. Design variants include P = 4 µm and 8 µm for a range of S values.

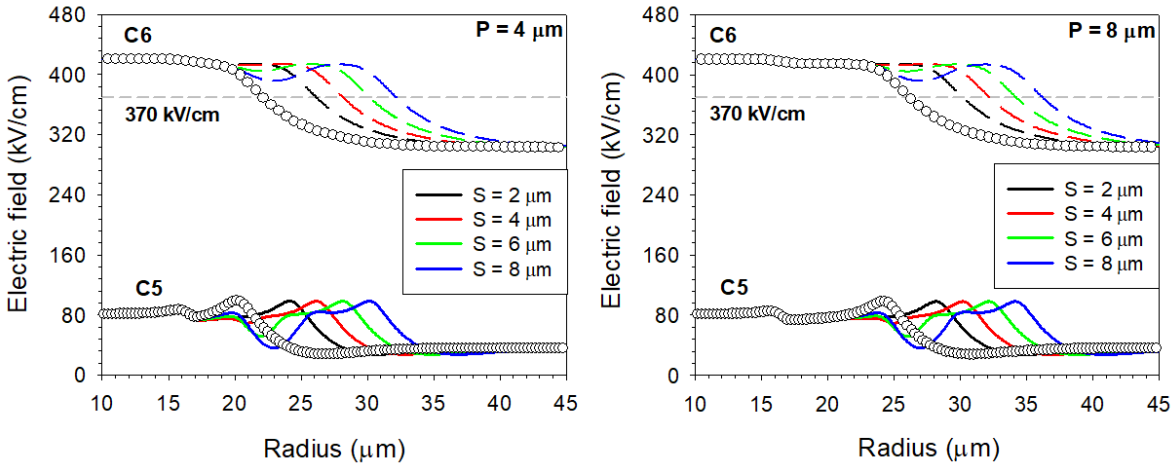

Fig. 6.9: Simulated electric field profiles along C6 (dashed lines) and C5 (solid lines) for P = 4 μm (left) and P = 8 μm (right) of different S values at -78 V. Results of devices without FGRs (with the same P) were included as symbols.

Indeed, introducing unnecessary FGRs might lead to undesirable effects for the proposed structure. Using P = 4 μm, simulated electric fields along C5 and C6 for S = 4 to 8 μm are compared in Fig. 6.9 (left). Corresponding electric fields from devices without FGRs are also included. A similar set of electric field profiles for P = 8 μm devices are shown in Fig. 6.9 (right). The non-zero electric field along C5 and C6 outside the active region (~ 40 kV/cm and ~ 300 kV/cm, respectively) is attributed to p-InP charge sheet layer in the proposed structure. The neighbouring devices are therefore electrically connected so electrical crosstalk is likely to be an issue. To isolate the devices electrically in the proposed structure, an additional etching process is required. Any mesa sidewall resulting from etching should be kept far from the active region. Comparing devices with and without FGR, the electric fields along C5 or C6 and outside the region defined by the deep Zn diffusion aperture remain high for greater distances. Hence FGRs are detrimental to achieving well-confined electric field profiles in the proposed structure.

Sensitivity of charge sheet doping densities

Although the simulation suggests the proposed structure is not sensitive to the Zn diffusion profiles, the additional p-charge sheet layer might introduce another variation for the electric field profiles. Therefore, a series of 2-D electric field simulations were carried out to evaluate the effect(s) of doping density variation (± 20 %) of the p- and n- charge sheet from the intended values (9.1×10^{16} and 8.1×10^{16} cm^{-3}) on the electric field profiles. The simulations were carried out at -78 V (the breakdown condition).

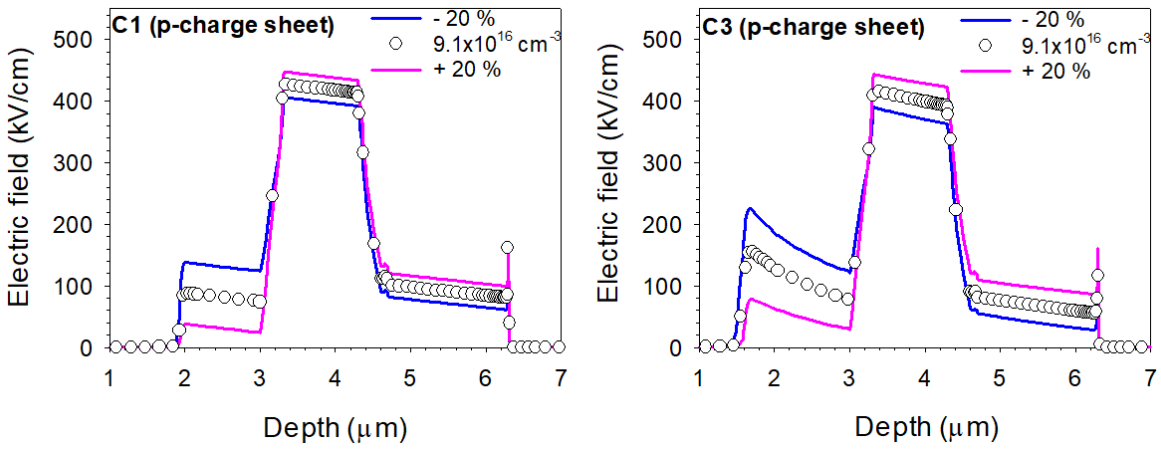

Fig. 6.10: Simulated electric field along C1 (left) and C3 (right) for p-InP charge sheet doped to 9.1 × 10^{16} cm^{-3} (symbol) ± 20% (solid line) at -78 V.

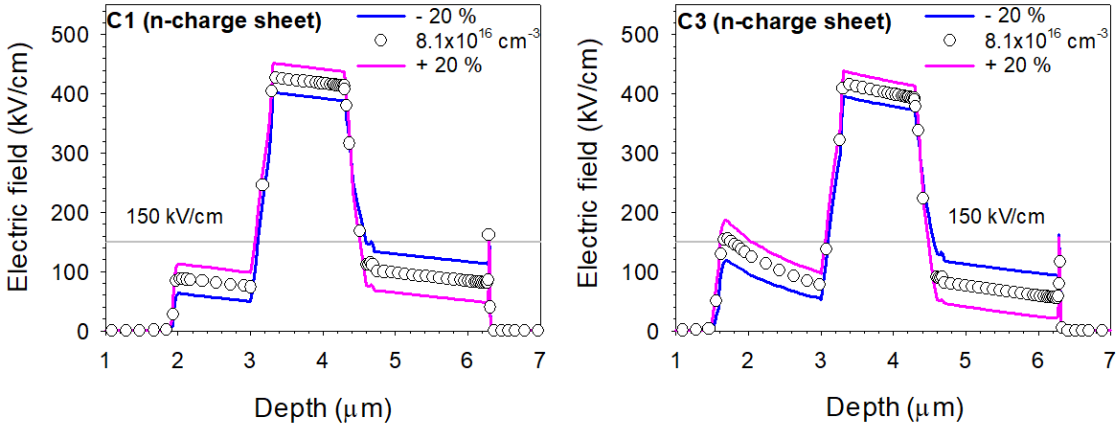

Fig. 6.11: Simulated electric field along C1 (left) and C3 (right) for n-InP charge sheet doped to 8.1 × 10^{16} cm^{-3} (symbol) ± 20% (solid line) at -78 V.

Their electric field profiles along C1 and C3 for p-InP charge sheet doped to 9.1 × 10^{16} cm^{-3} ± 20 % are shown in Fig. 6.10 (left) and (right), respectively. Variation of the p-charge sheet's doping densities has only a minor effect on the C1 electric field but a more noticeable difference on the C3 field profiles. However, the hotspot caused by the Zn diffusion (for depth < 3 μm) is still lower than the limit, suggesting the proposed wafer structure is not affected by the deviation in p-charge sheet densities alone.

The corresponding electric field profiles for the n-InP charge sheets doped to 8.1 × 10^{16} cm^{-3} ± 20 % are shown in Fig. 6.11(left) and (right), respectively. When the n-charge sheet's doping density increases, the electric fields in the InGaAs absorber along C1 and C3 increase. This is expected since the main function of the n-charge sheet layer is to control the difference in electric fields between the InP avalanche layer and the InGaAs absorber layer.

Assuming both p- and n- charge sheet doping densities have ± 20 % variation, the resultant C1 and C3 field profiles are compared in Fig. 6.12. When both values reduce by 20 %, the electric field in the

InGaAs absorber is similar to those of the intended values, with a slightly increased electric field in the buffer layer (but still < 370 kV/cm). When both values increased by 20 %, the electric field of the buffer layer (for depth < 3 μm) along C1 becomes negligible, as well as those in C3 field profiles. Indeed, both C1 and C3 show highly similar electric field profiles, suggesting that the p-charge sheet layer lost effectiveness in separating the electric field between the buffer and avalanche layer. This is confirmed by the C5 and C6 field profiles, as shown in Fig. 6.13. The electric field along C6 was maintained at ~ 500 kV/cm both within and outside the active region, while C5 field profiles were maintained at ~ 36 kV/cm outside the active region. Hence, the worst scenario is that the doping density values of p- and n- charge sheet layers increase by 20 % from the intended wafer structure.

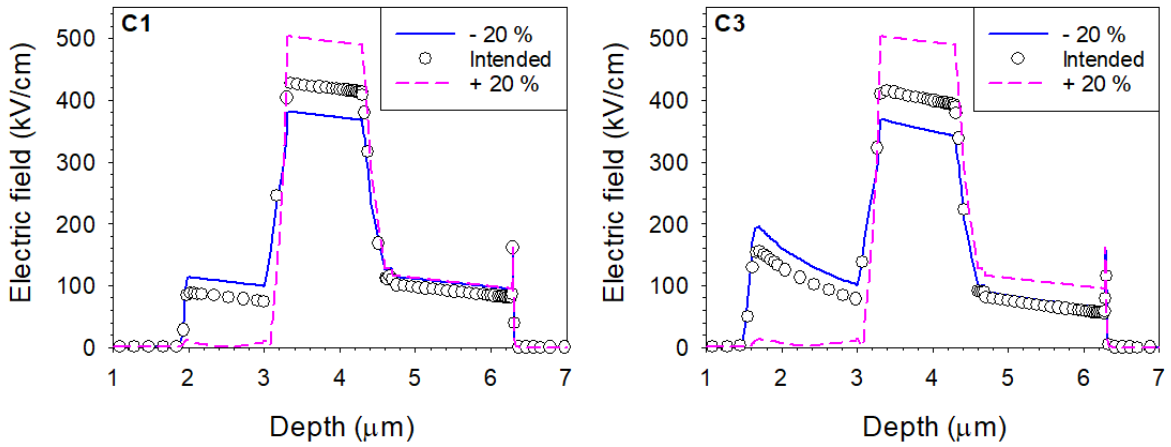

Fig. 6.12: Simulated electric field along C1 (left) and C3 (right) for both p-charge sheet (9.1 × 10^{16} cm^{-3}) and n-charge sheet (8.1 × 10^{16} cm^{-3}) doped to -20 % (solid line) and +20 % (dashed line) at -78 V. The electric field of the intended values was also included.

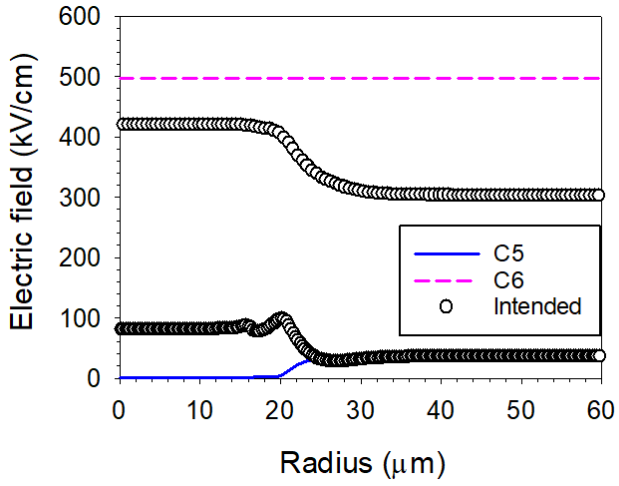

Fig. 6.13 : Simulated electric field along C5 (solid line) and C6 (dashed line) for both p-charge sheet (9.1 × 10^{16} cm^{-3}) and n-charge sheet (8.1 × 10^{16} cm^{-3}) doped to +20 % at -78 V. The electric field of the intended values was also included.

6.3 Conclusion

A new wafer structure with an additional p-charge sheet was proposed to minimise dependence on accurate Zn diffusion depths for planar InGaAs/InP APDs/SPADs. The 2-D electric field profiles from TCAD simulation suggested the FGRs are unnecessary for the proposed wafer structure because the hot spot after Zn diffusion is prevented by the p-charge sheet layer. In the proposed structure, FGRs are redundant and increase the active region unnecessarily. Also the p-charge sheet layer outside the intended devices' active regions should be removed, to avoid electrical cross-talks between neighbouring devices.

The effect(s) of varying doping density of the p-charge sheets on the electric field in the device's active region were also investigated. It was found that within ± 20 % variations in the p-charge sheet doping densities have minor effects on the active region's electric field. Hence, the proposed wafer structure offers potential for achieving the desired electric field without being subjected to inaccuracies in double Zn diffusion depths.

6.4 References

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Chapter 7: Conclusion & Future Work

7.1 Conclusion

Two planar InGaAs/InP SPAD wafers (Round 1) were designed, grown and fabricated using different combinations of Zn diffusion profiles and FGR spacing. Unfortunately, the devices exhibited high DCRs hence they do not function as competitive SPADs. These were due to actual electric fields in the InGaAs absorbers being much higher than intended design (caused by lower than intended charge sheet doping). Using these devices, experimental data were obtained from their linear mode operation. Coupled with TCAD simulations of 2-D electric fields (utilising actual Zn diffusion profiles in the APD wafers), the effectiveness of stepped Zn diffusions and FGRs on breakdown suppression in planar InGaAs/InP APDs was investigated. Both simulation and experimental results suggest that FGRs are only effective when their spacing to shallow Zn diffusion is ≤ 4 μm. Experimental data confirmed that the stepped Zn diffusions do suppress PEB, but the dependence on *P* value was small within the range considered. Finally, the optimum difference between Zn diffusion depth appears to be consistent with the design criteria of $d_1 \geq 1.5$ μm and $(d_2 - d_1) \geq 0.5$ μm for planar InGaAs/InP APDs from [1]. Although those suggestions are from the linear-mode operation, it is believed that effective FGRs can reduce the DCR from edge breakdown suppression. This informs future FGRs design for planar InGaAs/InP SPADs with double Zn diffusion.

Using improved wafer and device fabrication, competitive planar InGaAs/InP SPADs were produced in Round 2. Devices exhibit a higher DCR than the reported planar InGaAs/InP SPADs. Nevertheless, devices exhibit SPDE of up to 50 % with DCR of 1 Mcps at 225 K, better than reported state-of-art InGaAs/InAlAs SPADs. Experimental data confirms SPADs require a top InGaAs layer to avoid excess series resistance, but only the Zn-diffused InGaAs for metal contact should be retained. Otherwise the diffusion-related bulk dark current would contribute to the DCRs. This does create a trade-off between better performance and a more complex fabrication process.

Devices exhibit similar DCRs regardless of various *P*, *S*, number of FGRs or the absence of FGRs, despite the contribution from top InGaAs being minimised. Both 1-D electric field simulation and experimental DCRs at 225 K suggested the DCRs are not dominated by the bulk dark current and the contribution from band-to-band tunnelling current is insignificant. Therefore, excessive DCRs might attributed to the poor wafer quality or the edge breakdown. The 2-D electric field simulation provides the same suggestion as those in Round 1 for FGR spacing (≤ 4 μm). Unlike those in Round 1, the simulation shows the deviation of Zn diffusion profiles in Round 2 yields an ineffective stepped diffusion junction, causing PEB regardless of the different FGRs design (similar to experimental data).

Therefore, achieving the correct stepped Zn diffusion profiles for implementing the optimum FGR design for PEB suppression is crucial.

To optimise the Zn diffusion profiles (electric field profiles) [2], [3], 1-D electric field simulations were carried out using the wafer structure of Round 2 design. It confirms that the optimised Zn diffusion depths for a given structure are sensitive to charge sheet doping densities. The simulation also suggests the deviation of shallow and deep Zn diffusion depths further increases the electric field profile uncertainty. Hence, it is necessary to minimise the variation in n-charge sheet doping and the deviation of Zn diffusion depths to achieve the desired electric field profiles.

A new structure with wafer details was proposed to relax the tolerance of Zn diffusion depths to obtain the desired electric field for planar InGaAs/InP SPADs. The 2-D electric fields simulation suggests that FGRs are unnecessary since the hot spot caused by the curvature effect after Zn diffusion is significantly lower than 370 kV/cm to yield avalanche gain. Indeed, the FGRs would increase the active region beyond the deep Zn diffusion aperture (active region) thus they are undesirable for the proposed structure. The simulations also suggested that the p-charge sheet layer will contribute to electrical coupling between individual devices and, hence, electrical cross-talks. Therefore, an additional (but can be simplified) etching process is required to isolate the individual devices electrically.

Further investigations were carried out by adjusting the doping density variation (± 20 %) of the p- and n- charge sheet from the intended values. It was found that independent variation in the p-charge sheet doping densities has a minor effect on the electric fields, whereas the n-charge sheet layer has a strong impact on the electric field for the avalanche and absorber layer (as expected). The simulation suggested that p-charge sheet layer becomes ineffective when both doping density variation of p- and n- charge sheet is increased by 20 %. Overall, those studies provide guidance for implementing the proposed structure, which is promising to obtain a uniform electric field close to design using the proposed structure, achieving better performance and lower cost for the planar InGaAs/InP SPADs design.

7.2 Future Work

Chapter 4 demonstrated the negative effects of the high electric field in the InGaAs absorber due to the low activated charges sheet doping for SPAD operation. For the APD operation, experimental data did not show that insufficient edge breakdown suppression can lead to poor performance. Instead, devices with inefficient FGRs tend to have higher gains than those with efficient FGRs while having a similar V_{bd}. Therefore, optical probe scanning can be used to verify the optimised FGRs or Zn diffusion profiles for edge breakdown suppression. In addition, excess noise measurements can help to analyse the detrimental effect of insufficient edge breakdown suppression, which could lead to non-uniform electric field profiles. Hence, non-uniform gain could occur, and it would depend on the effectiveness of the

different FGR and Zn diffusion profile designs. Those non-uniform gain profiles can lead to different excess noise factors, as suggested by [4] based on the experimental comparison in mesa InGaAs/InP APDs.

Unfortunately, the Zn diffusion profiles and the device's geometry cannot be modified due to the nature of planar InGaAs/InP SPADs. However, the SPDE of planar InGaAs/InP SPADs shown in Chap. 5 can be increased by up to 30 % (at 1550 nm wavelength) through a 200 ~ 250 nm SiN AR coating layer. In addition, the photolithography alignment tolerance for the devices with P = 4 μm needs to be increased to yield consistent experimental results. The optical probe scanning method can be used to reveal the nature of edge breakdown suppression for SPAD operation, despite a lack of edge breakdown in APD operation. This would help to identify whether the source of excessive DCRs is dominated by the electric field hotspot at the peripheral region due to the inefficient FGRs or deviation of the Zn diffusion profiles.

On the other hand, the measurements for planar InGaAs/InP SPADs were only carried out for DCR and SPDE due to setup limitations. Devices need to be packed properly to enable future measurements for timing jitter and reduce the measurement uncertainty. This allows devices to be tested in the SPAD setup using the CQC PCB (described in section 3.4.4). Ideally, packed devices are impedance matched such that the actual AC pulse applied to the devices will not be distorted, reducing the measurement uncertainties. In addition, devices need to be packaged with a thermal electric cooler to be operated at lower temperatures than those of black box setups. The variation of the SPDE can be minimised by packaging the devices in pigtails, ensuring the photon will incident into the device's optical window. Using the CQC PCB, the devices can be quenched further properly instead of only relying on the gated quenching.

The simulation for the proposed structure in Chap. 6 only investigated the charge sheet sensitivity for a given double Zn diffusion InGaAs/InP SPADs. Hence, the simulation can be extended for InGaAs/InP SPADs with single Zn diffusion, simplifying the fabrication process. This can be achieved by modifying the simulated Zn diffusion profiles from actual SIMS data with a reasonable assumption. Since the proposed structure requires additional etching to isolate devices electrically, simulating the double mesa geometry to access the edge breakdown characteristics close to the mesa wall is necessary. This allows the photolithography alignment tolerance to be optimised for the etching process. By doing that, the ineffective FGR spacing (for either single or double FGR) in the previous simulation (Chap. 6) can be taken as the starting point. However, there might be a trade-off depending on the requirement after coupling with the diameter of the Zn diffusion, which is used to confine the electric field within the buried avalanche layer. Finally, the InGaAs/InP SPADs can be grown, fabricated and characterised based on the proposed structure. With the proposed structure, devices are expected to have the same avalanche width and hence the breakdown voltage regardless of diameter. Nevertheless, edge

breakdown due to the addition etching process can lead to an inconsistent breakdown voltage, suggesting the photolithography alignment tolerance has not been optimised. The optical probe scanning method can verify the edge breakdown or presence of the non-uniform electric field.

7.3 References

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Appendix A

Mask design for Round 1

The photolithography masks used for Round 1 (Chap. 4) are summarised in Table A. 1. The 5 photolithography masks (v1.05) were designed and then be modified (v1.08). The modification included (i) additional alignment mark in mask 3 to 5, (ii) transmission line measurement (TLM) features in mask 3 and 4, and (iii) optional mask layers to make electrical contacts to the charge sheet.

Table A. 1: Summary of photolithography masks and organisations that carried out the associated device fabrication steps. The mask number are identical in v1.05 and v1.08, except for absence of mask 6 in v1.05.

Mask number and order of use	**Purpose**
1	First Zn diffusion (shallow)
2	Second Zn diffusion (deep)
3	Top contact
4	Bondpads
5	Etch to n-InP buffer to create cleave channels and facilitate n-contacts
6	n-contacts

Table A. 2 summaries the variants contains on the mask, which shown in Fig. A. 1. The whole unit cell is divided into left and right parts depending on the metal covering. Devices on the left side have an optical window, while the metal fully covers the devices' window on the right side. Devices without optical window on the right side were intended for dark count measurement. The metal covered device edge to prevent side injection of the optical signal. As a result, the actual optical window of the device is smaller than the active region. Moreover, three Zn diffusion (shallow only, deep only and total) opening with 200 µm diameter was included for potential SIMS measurements.

Table A. 2: Repeated from Table 4.3.

Device variants	**Value or range**
Device diameter (*D*)	10, 20 and 40 µm
Zn diffusion extension (*P*)	3 - 5 µm, in steps of 1 µm
Guard ring spacing (*S*)	4 - 8 µm, in steps of 1 µm

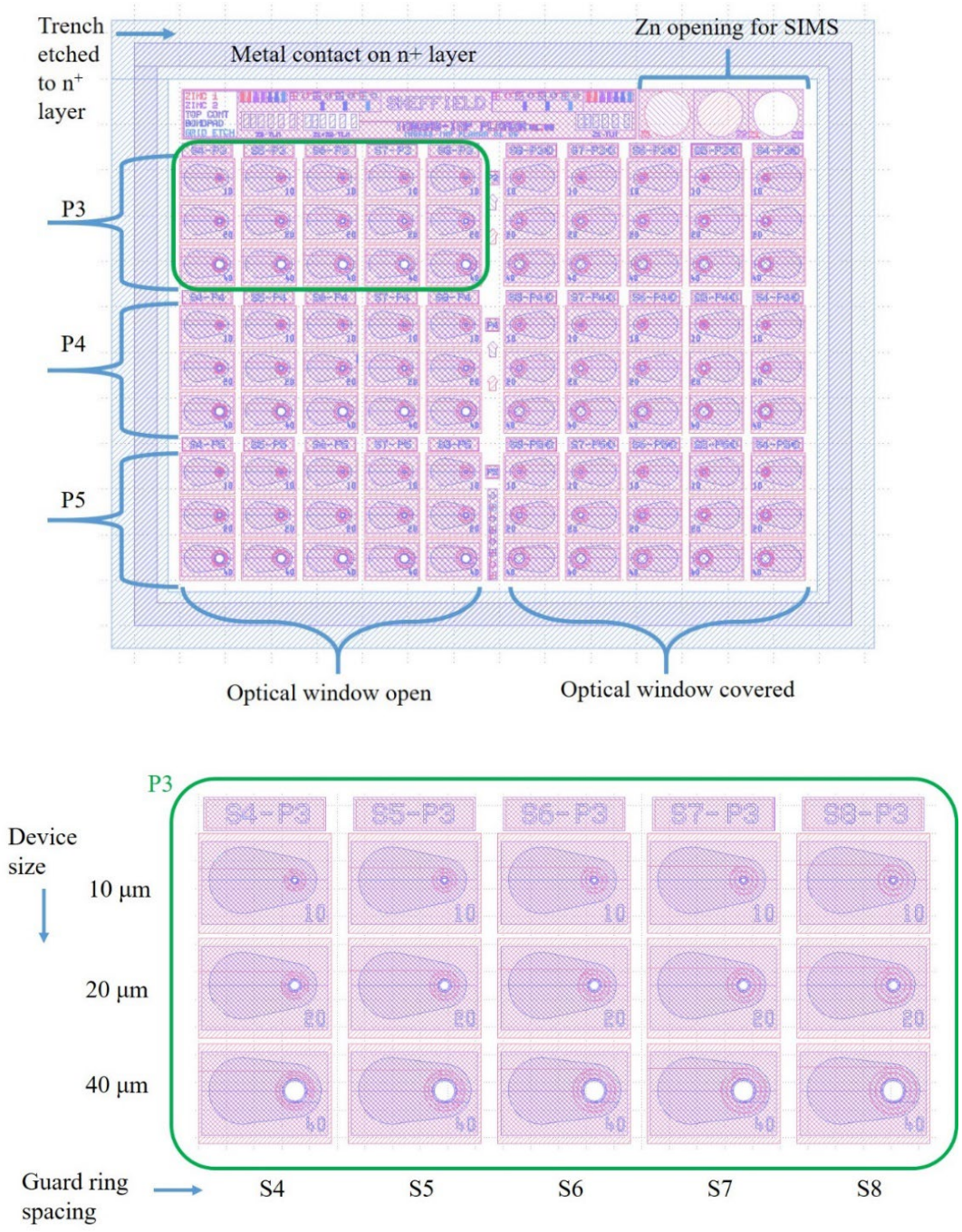

Fig. A. 1: Unit cell (top) and devices variants for a given P values(bottom) of the Round 1 mask design (v1.05).

Appendix B

Mask design for round 2

Fig. B. 1 shows the devices with various design on the photolithography mask for Round 2 (Chap. 5). The unit cell was split into two sub cell for different Zn diffusion extension (P = 4 and 5 µm). Each sub cell contains different guard ring spacing (S) of 3, 4, 5 and 6 µm. Among them, only the device with S = 4 µm has a diameter of 10, 20 and 40 µm, while the device with other spacing only has a diameter of 20 µm.

Take sub cell of P = 4 µm (shown in Fig. B. 1 (bottom)) as an example; there are 6 columns with different design purposes. Devices with S = 4 µm are in columns 1 and 2 with a diameter of 10, 20 and 40 µm. Although they are identical, the FGR features of the devices are covered by the bondpad in column 1. Similarly, devices in column 3 are the same as in column 4 except for the bondpad design. Devices with a guard ring spacing of 3, 5 and 6 µm are included in columns 3 and 4 with a diameter of 20 µm. To assess the dark count rate for the SPAD, non-optical activated devices with S = 3, 4 and 6 µm with a diameter of 20 µm are placed in column 6. As mentioned earlier, devices all have double FGR, while the SGR devices with guard ring spacing of 3, 4 and 6 µm are included in column 5 with the absence of a different bond pad design.

Apart from the various designs, 4 large diameters (80, 100, 150 and 200 µm) devices with S = 4 µm and P = 5 µm are used for accurate C-V measurements. A device with S = 4 µm, P = 4 µm and no FGR was also included as a reference sample. In addition, two large Zn diffusion apertures (shallow diffusion only and double Zn diffusion only) were included for potential SIMS measurements.

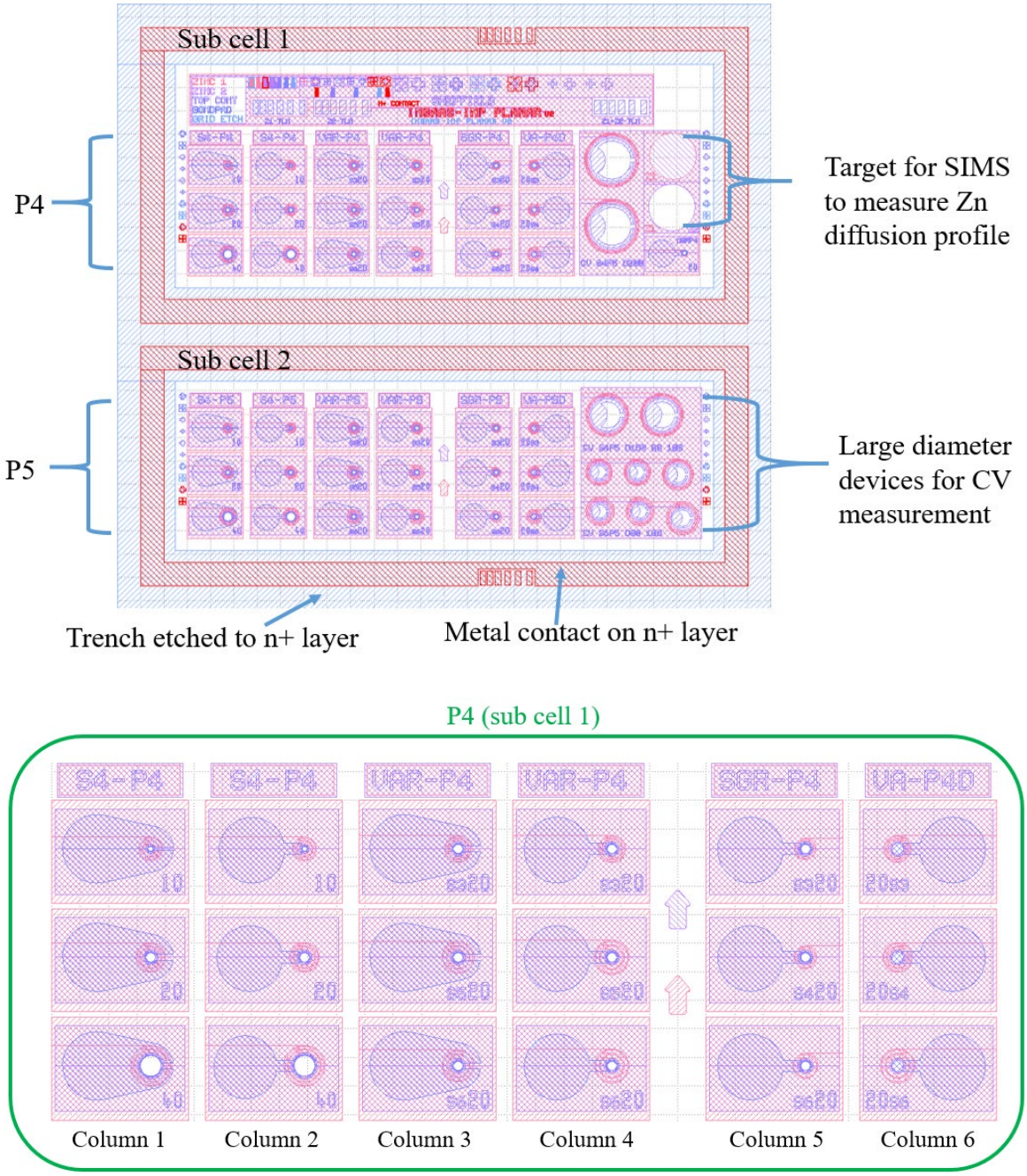

Fig. B. 1: Unit cell (top) and devices variants for a given P (sub cell) (bottom) of the Round 2 mask design.

Appendix C

Modified mask and fabrication for top InGaAs removal

C.1 Modified mask for InGaAs removal

Additional masks are required to remove the excessive top InGaAs in Round 2 planar InGaAs/InP SPADs, as summarised in Table C.1. To remove the top InGaAs, the SiN layer needs to be removed. However, the initial alignment was created on the SiN layer by the double Zn diffusion process. Hence, it is necessary to re-create the alignment marks on the semiconductor surface (layer 7). Layer 8 is used to protect the area of Zn-diffused InGaAs from etching so it can be retained for top metal contact. The modified top contact in layer 9 is designed to cover the etched InGaAs fully. After the SiN deposition, layer 10 can be used to etch down the SiN for optical window and bondpad deposition.

Table C. 1: Summary of additional mask sets for top InGaAs removal.

Mask Layer number	Title	Function	Data polarity
7	Alignment mark	To re-create alignment marks	Clear
8	InGaAs open	Keep the area of InGaAs for metal contact	Dark
9	Top contact	Modified top contact for metal deposition	Clear
10	SiN open	Open SiN for optical window bondpad deposition	Clear

The InGaAs open is located between shallow (Z1) and deep (Z1+Z2) diffusion which are highly doped, as shown in Fig. C. 1. Whereas the Fig. C. 2 (left) shows the design of the modified top contact ('TC'). The size of the top contact is slightly larger than the InGaAs open to ensure retained InGaAs will not exposed in the later fabrication process, preventing surface roughness as well as the surface leakage current. In addition, a larger pattern increases the undercut tolerance of the InGaAs if the wet etching method is chosen. However, the misalignment of the top contact will also make the metal connect to the Zn-diffused InP layer. Since top contact determined the device's area (as shown in Fig. C. 2 (right)), the SiN open pattern was designed to be smaller than those of top contact. Furthermore, Fig. C. 3 shows design of SiN open that cooperated with different bondpad design to avoid unnecessary etching of InGaAs or InP from the dry etching process.

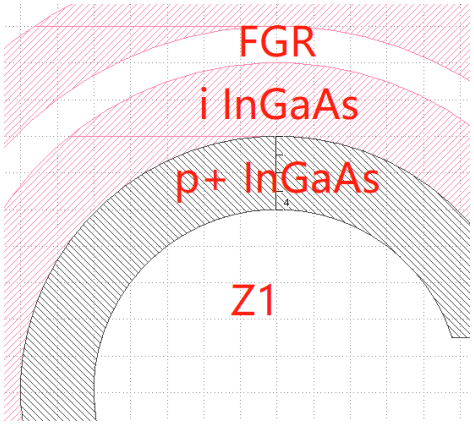

Fig. C. 1: Design of InGaAs open.

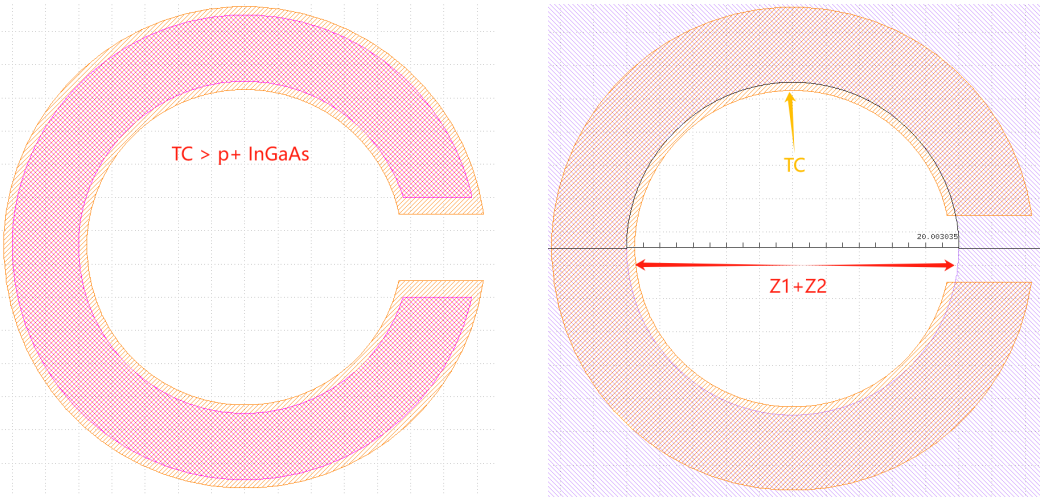

Fig. C. 2: Design of top contact.

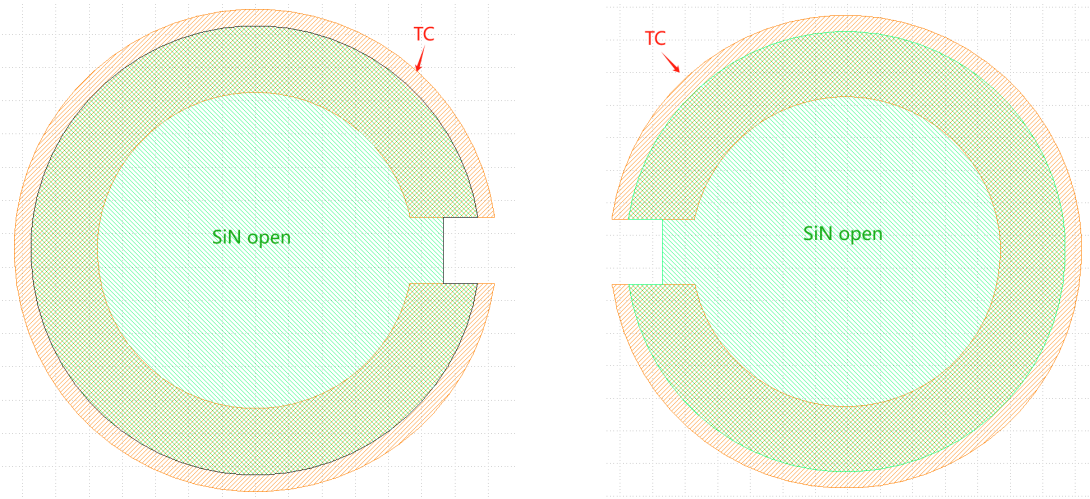

Fig. C. 3: Design of SiN open for different bondpad designs (left for Fig. 5.17(right) and right for Fig. 5.17(left)).

C.2 Fabrication for top InGaAs removal

The first trial of fabrication was done on sample C2 (Round 2), followed by optimisation for sample C3. The two samples have similar fabrication except for the method to re-create the alignment marks. Test sample C2 used the dry etching method (ICP) to etch down the InGaAs and InP to create alignment marks (as shown in Fig. C. 4 (left)), whereas the main sample C3 relied on metal deposition to form alignment marks (as shown in Fig. C. 4 (right)). It is evident that the alignment created by the dry etching is harder to see compared with those by metal deposition. This is because InGaAs and InP have different rates for a given ICP recipe. Moreover, the dry etching yields a rough surface on InP, leading to difficulty in aligning the alignment mark under the microscope. Therefore, it is more reliable to use the metal deposition to create the alignment despite the fact that the metal might peel off during the later wet etching process. The whole fabrication processes are summarised in Fig. C. 3, along with the used mask order.

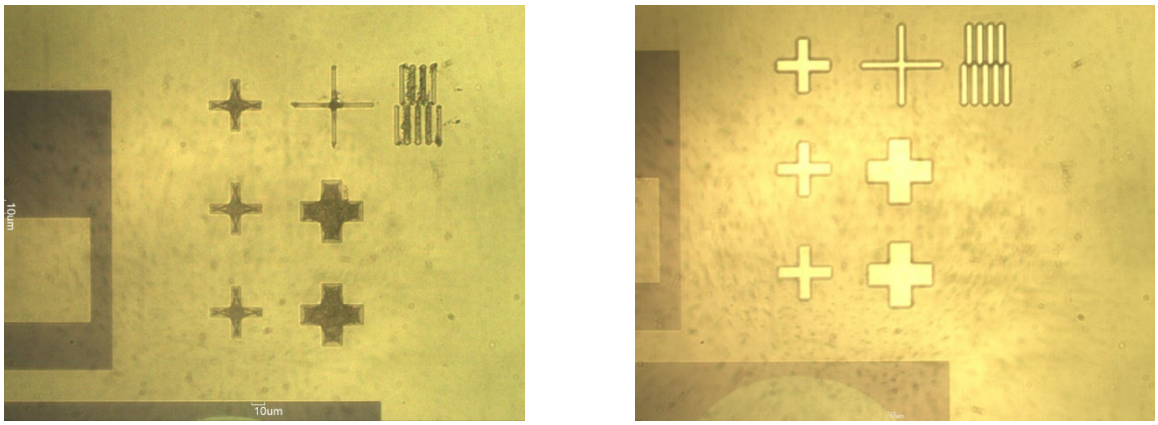

Fig. C. 4: Alignment mark created by ICP dry etching (left) and metal deposition (right).

Table C. 2: Summary of fabrication process for samples C2 and C3 in Round 2.

Mask order	Mask purpose	Step
7	Alignment mark	(Sample C2) Standard photolithography, followed by ICP dry etching to create alignment mark.
		(Sample C3) Standard photolithography, followed by metal deposition to create alignment marks.
		Used 40 % HF to remove SiN, this was done by Dr. Blain.
8	InGaAs open	Standard photolithography, followed by wet etching using H_2SO_4: H_2O_2: DI.
9	Top contact	Standard photolithography, followed by sputter deposition (Ti/Au).
		~ 260 nm SiN deposition using PECVD.
10	SiN open	Standard photolithography, followed by RIE dry etching.
4	Bondpad	Standard photolithography, followed by thermal evaporation (Ti/Au).

5	Bottom contact etch	Standard photolithography, followed by selected wet etching using H_2SO_4:H_2O_2:DIW (1:1:10) for InGaAsP and InGaAs; whereas HCl:DIW (2:1) for InP.
6	Bottom contact deposition	Standard photolithography, followed by thermal evaporation (Ti/Au).

Appendix D

Supplementary data from Round 1

Room temperature reverse dark I-V data from sample B1 are shown in Fig. D.1. Devices exhibit low dark current (~ 1 nA) before breakdown, regardless of design variants. Design variants do however introduce small variations in V_{bd} (up to ~ 3 V). For a given P, devices with S = 4 µm have the largest V_{bd}, with S = 6 and 8 µm having slightly lower V_{bd} (by 2 V). For a given S, devices with P = 5 µm have the largest V_{bd}, with P = 3 and 4 µm having slightly lower V_{bd} (by 1 V).

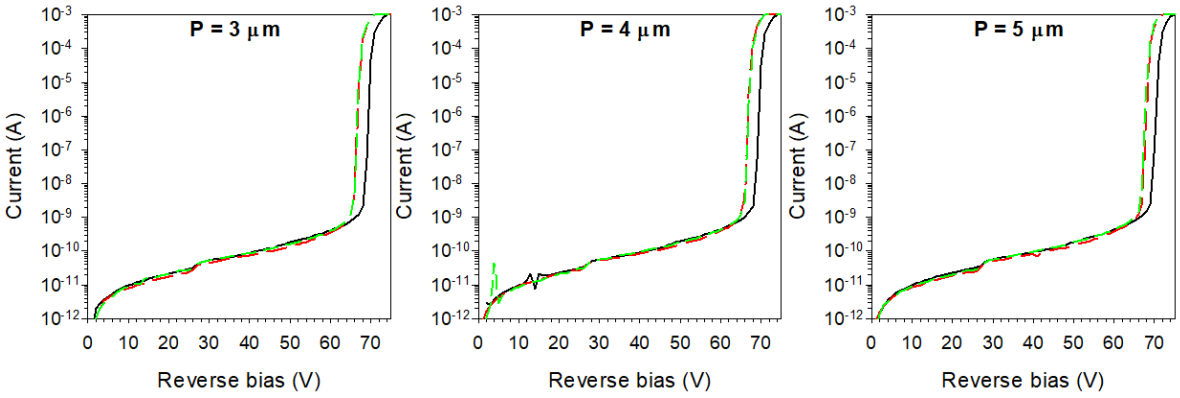

Fig. D.1: Reverse I-V data of devices from sample B1 for a given P (3, 4 and 5 µm) with various S (black for 4 µm; red for 6 µm; green for 8 µm). Devices have diameter of 20 µm.

In Fig. D.2 , I-V data of sample B1 and B2 are compared. They have similar range of V_{bd}. The dark currents are similar prior to punch through, but they differ by ~ 1 order of magnitude prior to breakdown, despite originating from the same wafer and Zn diffusions.

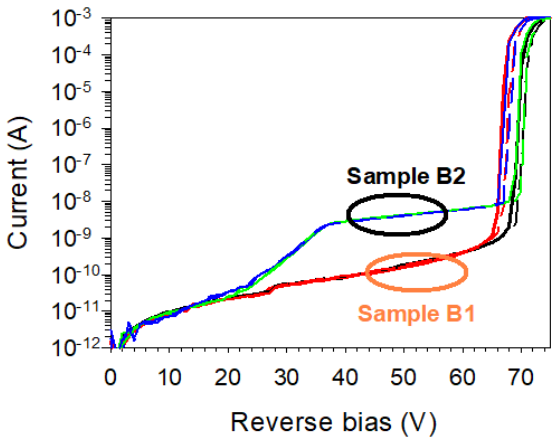

Fig. D. 2: Dark current comparison between sample B1 and B2 for the same S and P values.

C-V data of sample B1 for devices with $P = 5$ µm and $S = 4$ µm are shown in Fig. D.3 (left) and (right), respectively. Device's diameter was 40 µm. The capacitance values are close to the lower limit of the LCR meter used, so data around the 0.1 pF should be treated with caution. All devices exhibited a sudden decrease of capacitance between -27 and -30 V, regardless of S and P values. This is smaller than $V_p \sim 40$ V from the wafer design. For a given P value, the capacitance increases very slightly with S, suggesting that presence of FGR affects capacitance. For a given S value, the capacitance increases with P, suggesting that the shallow Zn diffusion too affects capacitance.

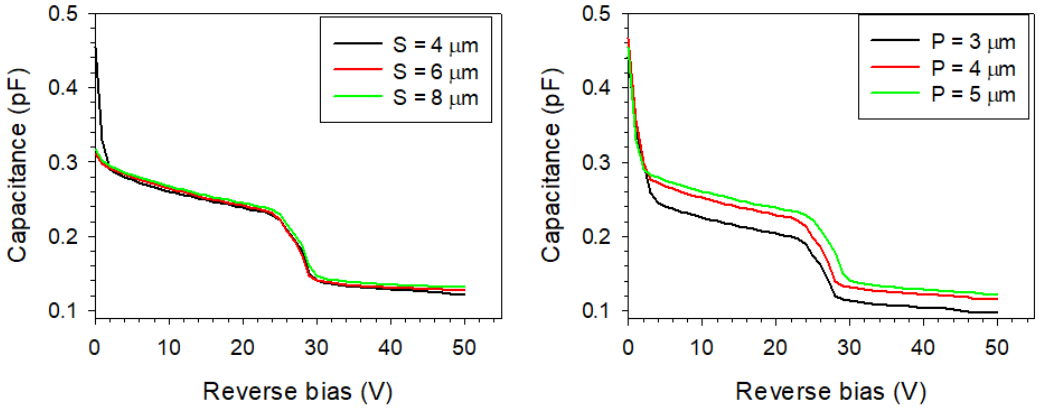

Fig. D. 3:C-V data of device with 40 µm diameter for (left) various guard ring spacing and P = 5 µm and (right) various Zn diffusion extension and S = 4 µm. Data was obtained from sample B1.

Table D. 1: Input for C-V fitting using 1-D electric field solver.

Material	Dielectric constant	Doping (cm^{-3})	Thickness (µm)
InP (p^+)	12.5	1.0×10^{18}	---
InP (avalanche)	12.5	-1.0×10^{15}	0.80 ~ 0.95
InP (n)	12.5	6.3×10^{16}	0.30
InGaAsP (i)	11.8	-1.0×10^{15}	0.09
InGaAs (absorber)	13.9	-1.0×10^{15}	1.60
InP (n^+)	12.5	-1.0×10^{18}	---

Mean values were obtained from the experimental C-V results of sample B1 with 40 µm diameter, $S = 8$ µm and $P = 3$ µm to serve as reference data in C-V fittings, which involved 1-D electric field simulations (abrupt doping profiles) for a range of reverse bias (0 to -50V). Table D.1 summarises the layer thickness and doping density used in the fittings. The C-V fittings using active region diameter of 40 and 54 µm are compared to the mean experimental results (diameter = 40 µm) and those expected from the SPAD design in Fig. D.4. The experimental V_p is ~ 10 V lower than the expected V_p, so the fittings required a lower doping density in the charge sheet compared to the SPAD design. Also, the fitting using 40 µm diameter is significantly lower than the experimental results. Increasing the diameter to 54 µm (which include the shallow Zn diffusion and the FGR) improve the agreement between the fitting and the experimental results prior to punch through. The poorer data quality for capacitance values around 0.1 pF prevented useful observations for C-V fittings at reverse bias beyond -30 V.

Nevertheless, the C-V fittings for sample B1 (40 µm diameter) indicated that avalanche width and charge sheet doping are 0.8 µm and 6.3 × 10^{16} cm^{-3}, respectively. The avalanche width extracted from C-V fitting is slightly less than that from SIMS (0.8 µm cf. 0.92 µm), which are due to (i) uncertainty associated with the non-abrrupt doping profile at the p^+-InP layer and the n-InP avalanche region, and (ii) dependence of Zn diffusion depth on the diffusion aperture. Compared to the small diffusion apertures used in actual SPADs (40 µm), the large diffusion apertures (200 µm diameter) in SIMS features are likely to produce shallower Zn diffusion depths, resulting in slightly wider InP avalanche regions. The C-V fittings also confirmed that, at least for some design variants, the shallow Zn diffusion region and the FGR do contribute to the device capacitance, complicating the efforts of estimating electric field profile from experience C-V data.

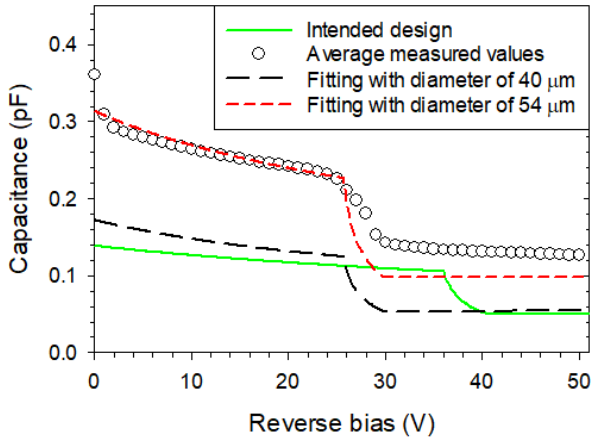

Fig. D. 4: C-V fittings and mean experimental C-V results from devices with 40 µm diameter on sample B1.

The C-V data of SPADs with 40 µm diameter from B2 and A2 are presented in Fig. D.5 (right) and (left), respectively. Due to parasitic capacitance from device bondpads in sample B2, much higher capacitance data were recorded, compared to data of sample B1 (Fig. 4.14). Hence these data are unsuited for detailed C-V fittings. The data however are still useful and facilitated additional observations as follows.

Both samples exhibited two sudden capacitance decreases. The first decrease at ~ -26 V is attributed to full depletion of the InGaAs absorber within the active region (i.e. those defined by the deep diffusion). For sample A2, V_p ~ -26 V indicated an avalanche width of 0.7 µm, less than the 0.8 µm obtained from the large 'Z1+Z2' C-V results (Fig. 4.16). The later, second decrease at ~ -37 V is attributed to depletion into the InGaAs absorber under the shallow diffusion.

Based on SIMS data (Fig. 4.12), the Z1 diffusion depth is ~ 1.7 µm, giving ~ 1.3 µm of InP avalanche width under the shallow Zn diffusion region. Using 1.15 µm InP avalanche width, charge sheet doping density of 6.3 × 10^{16} cm^{-3} and charge sheet thickness of 300 nm, a punch-through voltage of -40 V was predicted, in agreement with the experimental C-V data of Fig. D.5. This suggests that InP avalanche region under the shallow Zn diffusion region do become depleted (at ~ -40 V in this case). This supports

the earlier observation that the shallow Zn diffusion region and the FGR do contribute to the device capacitance (Fig. D.4).

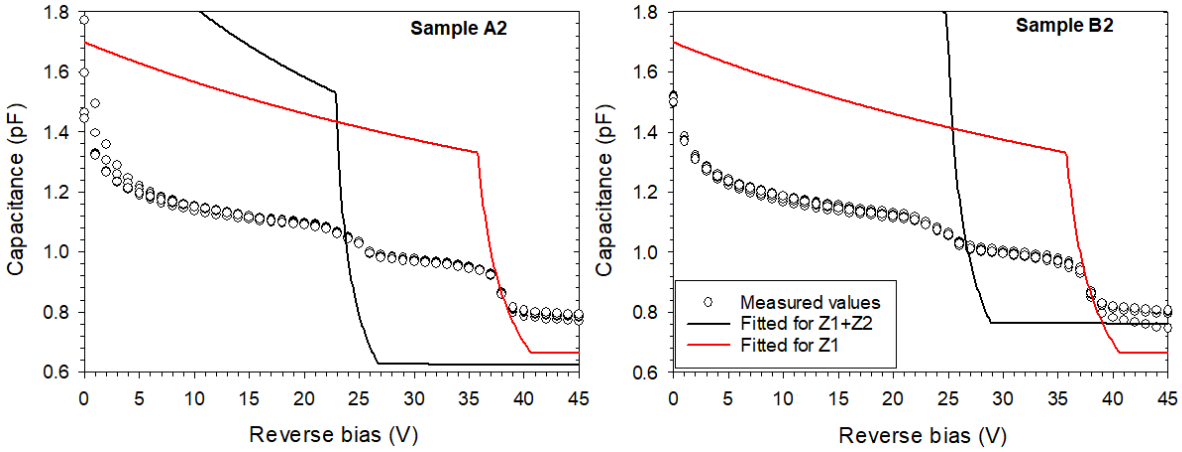

Fig. D. 5: Experimental (symbol) and calculated (line) C-V of devices with 40 µm diameter from sample A2 (left) and sample B2 (right).

Appendix E

Supplementary data from Round 2

Photos of devices with different bondpad designs are presented in Fig. E.1. In Fig. E.1 (left), the area (FGRs and shallow Zn diffusion) outside the active region is not covered, so it can absorb incident photons with energy < 0.75 eV. In Fig. E.1 (right), the device's optical-sensitive area is much more limited. Therefore, the photosensitive area of a device is influenced by the bondpad design.

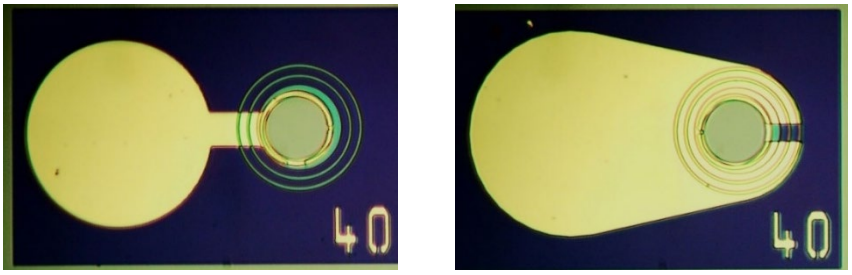

Fig. E. 1: Top views of devices with a larger (left) and smaller (right) optically sensitive area.

The raw dark counts and photon counts from SPADs with larger and smaller optical-sensitive areas are shown in Fig. E.2 (left) and (right), respectively. As expected, the DCR decreases as the diameter decreases. The small difference in raw dark count data between the two figures is attributed to experimental uncertainty. SPADs with larger optical-sensitive areas exhibit a higher photon count than those with smaller optical-sensitive areas, despite the same optical power used in the measurements. This might be because, in devices with large optical-sensitive area, carriers originally created through photon absorption outside the active region, experience different P_b compared to those created within the active region. The variation of P_b can lead to a variation of photon count data.

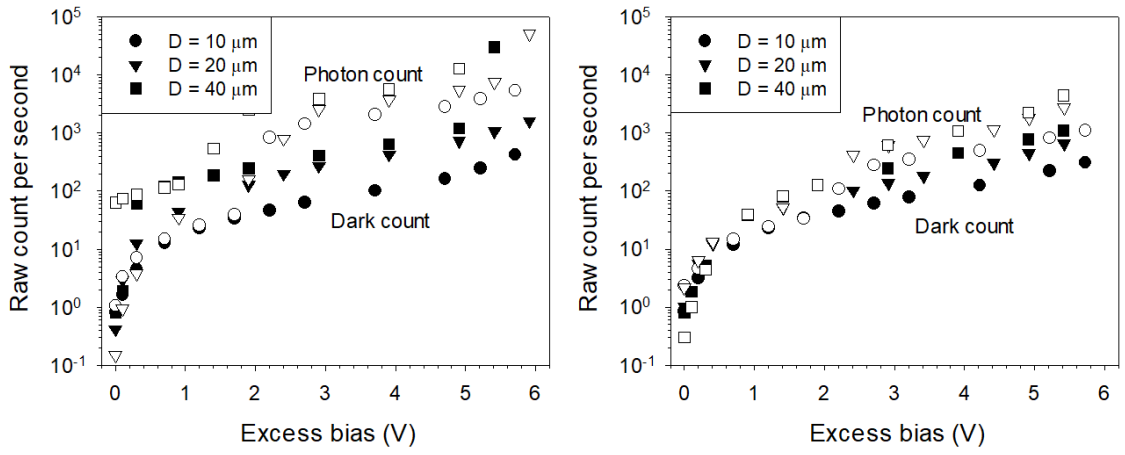

Fig. E. 2:Raw dark count (black) and photon count (0.1 photon per pulse on average) (white) from devices with a larger (right), and smaller (left) optical-sensitive area and different diameters at 200 K. Devices have double FGRs, S = 4 μm and P = 4 μm.