University of Sheffield

Design, Optimisation, and Analysis of Multi-Level SiC Converters

By

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A thesis submitted in fulfilment of the requirements for the degree of

Doctor of Philosophy

Department of Electronic and Electrical Engineering

Faulty of Engineering

The University of Sheffield

November 2023

Abstract

Silicon Carbide (SiC) devices, known for their thermal stability, high efficiency, and excellent high-temperature performance, have become vital in power electronics after decades of development. These devices offer significant potential for higher switching speeds, lower energy losses, and enhanced system performance. Multi-level converters (MLCs) are especially valued for their capability to increase output voltage levels, minimise power losses, reduce harmonic distortion, and decrease voltage stress on switching devices. This thesis explores the design, application, modelling, and analysis of MLC based on SiC power devices.

This thesis firstly focuses on analysing the performance of three-level topologies (NPC, ANPC, T-type) under varying conditions using precise device parameter models. Key factors like voltage stress and power losses are evaluated, with particular attention to the suitability of SiC MOSFETs in high-voltage aviation applications, providing recommendations for topology selection for different applications. It also highlights a fully integrated three-level NPC module optimised for specific applications, focusing on electrical, electromagnetic, and thermal performance. Unlike combined several two-level modules, it minimises parasitic inductance and uses a novel baseplate for better efficiency and thermal management in aerospace. Using an equivalent heat transfer coefficient instead of CFD simulations quickly estimates power device temperatures, reducing computational time and cost. A linear estimation method determines output power under varying airflow rates and assesses scalability. For the three-level NPC topology, a two-port small-signal model is established. S-parameters are measured using a VNA and converted to Z-parameters for parasitic inductance extraction, with validation showing an error of less than 10%. The extracted parameters are applied to DPT simulation and platform testing, confirming their accuracy.

Acknowledgement

Throughout my PhD research journey, I have been fortunate to receive support and guidance from many outstanding people whose help has been crucial to my academic growth and personal development. I would like to express my deepest gratitude.

First and foremost, I would like to thank my supervisor, Prof. Antonio Griffo, for his invaluable guidance and support during my studies. His wisdom, patience and motivation have been my driving force. I am very grateful to him for his guidance in writing my thesis. I am honoured to be his PhD student. I would like to thank my second supervisor, Prof. Jiabin Wang, for providing me with knowledge and advice. I would also like to express my sincere gratitude to Dr Shangjian Dai for his help in my experiments, and the challenges and successes we shared together will be my precious memories forever.

I would like to thank my parents, especially for their support and encouragement in completing my studies. Their love, encouragement and sacrifices have been a strong shield for me to pursue my academic dreams.

I would also like to thank all the staff of the Department of Electrical and Electronic Engineering at the University of Sheffield for their support and dedication. Special thanks go to my colleagues and my friends for their help and support.

I would like to express my sincere gratitude to all those who have supported me. This thesis is the result of our joint efforts.

Table of Acronyms and Symbols

Acronyms

Acronym	Description
AC	Alternating current
ANPC	Active neutral point clamped
BJT	Bipolar transistor
CFD	Computational fluid dynamics
CHB	Cascaded H-bridge
CSC	Current source converter
CTE	Coefficient of thermal expansion
DC	Direct current
DCB	Direct copper bonded
DPT	Double pulse test
DUT	Device under test
EMI	Electromagnetic interference
EV	Electric vehicle
FC	flying capacitor
FEM	Finite element method
FET	Field effect transistor
FRD	Fast recovery diode
GaN	Gallium Nitride
HEV	Hybrid electric vehicle
IGBT	Insulated gate bipolar transistor

MLC	Multi-level converter
MOR	Model order reduction
MOSFET	Metal-oxide-semiconductor filed-effect transistor
NPC	Neutral point clamped
NTC	Negative temperature coefficient
PCB	Printed circuit board
PCM	Phase change material
PEEC	Partial element equivalent circuit
PM	Power module
PMSM	Permanent magnet synchronous machine
PWM	Pulse width modulation
RMS	Root-mean-square
RF	Radio frequency
SBD	Schottky barrier diode
Si	Silicon
SiC	Silicon carbide
SVPWM	Space vector pulse width modulation
TDR	Time-domain reflectometry
TIM	Thermal interface material
TNPC	T-type neutral point clamped
THD	Total harmonic distortion
UPS	Uninterruptible power supply
VNA	Vector network analyzer
VSC	Voltage source converter
WBG	Wide bandgap

Symbols

Symbol	Description
C_{ds}	Drain-source capacitance
C_{gd}	Gate-drain capacitance
C_{gs}	Gate-source capacitance
C_{iss}	Input capacitance
C_{oss}	Output capacitance
E_B	Breakdown field
E_g	Bandgap energy
E_{off}	Turn-off energy
E_{on}	Turn-on energy
E_{sw}	Switching energy
f_{load}	Load frequency
f_{res}	Resonant frequency
f_{sw}	Switching frequency
i_{ds}	Drain-source current
L_{loop}	Loop inductace
m	Modulation index
M	Switch angle number in the first quarter cycle
P_{cond}	Conduction loss
P_{off}	Turn-off power
P_{on}	Turn-on power

P_{sw}	Switching loss
R_g	Gate resistance
$R_{ds(on)}$	drain-source on resistance
R_{thjc}	Thermal resistance from junction to case
T_j	Junction temperature
V_{BR}	Breakdown voltage
V_{ds}	Drain-source voltage
$V_{ds(on)}$	On-state voltage
V_{gs}	Grain-source voltage
V_{th}	Threshold voltage
v_{sat}	Saturation drift velocity
V_{dc}	DC-link voltage
μ_n	Electron mobility
μ_p	Hole mobility
λ	Thermal conductivity
ε_r	Relative permittivity
*	Reference quantity

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CHAPTER 1
General Introduction

1.1 Background and Motivation

After a hundred years of development, power electronic technology has been widely used in various electrical conversion systems. The history of power electronics can be traced back to the early 20th century, with a primary focus on power conversion and control, Fig.1-1 shows the development milestone of power electronics technology. Long-term advances in power semiconductor devices have enabled power electronic systems with higher switching speeds, wider temperature ranges, higher achievable power, higher efficiency, and reliability. In the future, the technology should be developed towards high efficiency, low cost, and low consumption.

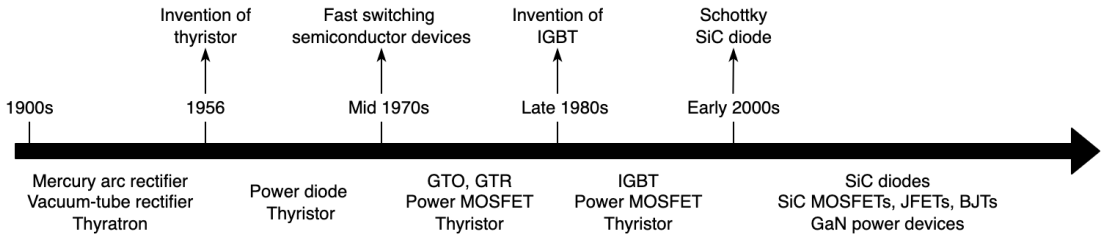


Fig.1-1 Development milestone of Power Electronics technology [1]

Early power electronics relied heavily on discrete devices that were large and limited in efficiency and power density. As these devices evolved, particularly with the advent of bipolar transistors (BJTs) and field effect transistors (FETs), they allowed for more efficient and controllable AC to DC, DC to AC, and DC to DC conversions. In order to integrate these power devices more efficiently while ensuring reliability and efficiency, manufacturers have integrated these devices with diodes, passive components and driver circuits into a single module, and this integration has led to the creation of the power module.

In addition, at the end of the last century, advances in substrate materials and packaging technology, as well as the excellent properties of SiC and Gallium Nitride (GaN), have made the power module an even more desirable solution in the field of power electronic conversion. In 1975, SEMIKRON introduced the first power module to the market.

Overall, the history of power electronics has been a progression from single power device to integrated solutions, and power modules have played a key role in this process, helping designers more easily meet changing requirements.

Fig.1-2 shows the path from a semiconductor wafer to a converter that can drive a load. Completing this transition involves multiple steps and levels of technology. The following is a general process for moving from a power device to a full-featured converter:

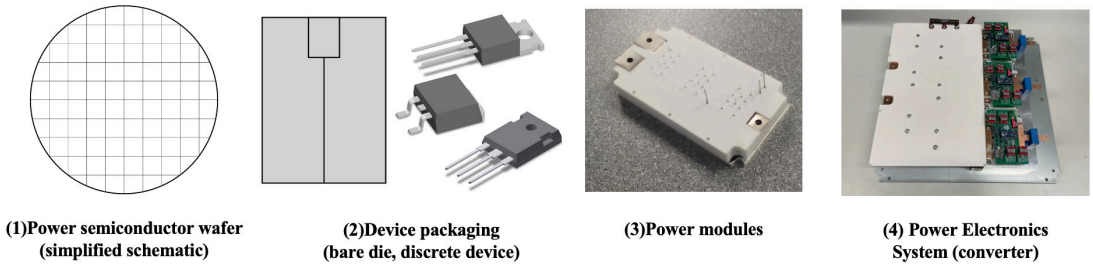


Fig.1-2 From power semiconductors to converter

1. Power semiconductor devices: Wafers are processed through several steps including doping, ion implantation and etching to form the required basic power semiconductor devices.
2. Device packaging: To facilitate practical use, semiconductor devices need to be properly packaged after fabrication. They are usually placed in a protective enclosure, which provides physical support, electrical connections, and thermal management. In addition to this, unpackaged semiconductor bare dies without any leads or enclosures can also be integrated directly into power modules, which saves a lot of space and allows for efficient heat dissipation due to direct contact with the substrate. However, it requires more complex circuit connection and special manufacturing techniques which may result in defects and device failures. Fig.1-3 shows an example of a failed weld.

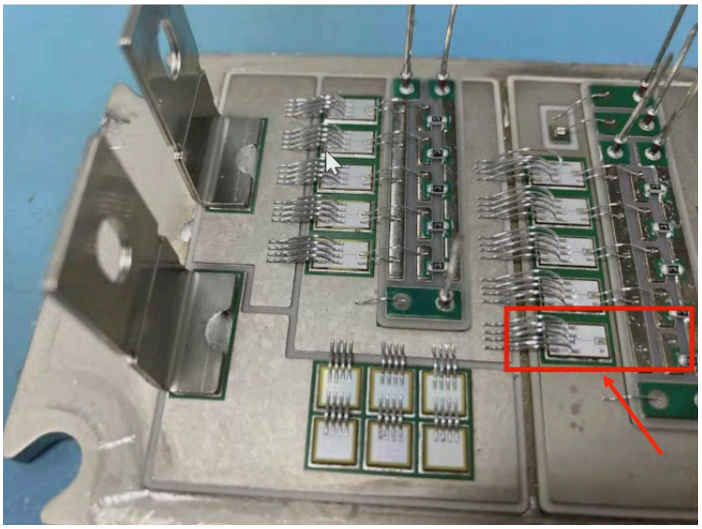


Fig.1-3 Gate failure in one MOSFET

3. Power module integration: Multiple power devices are often combined into power modules for higher power applications. These modules may incorporate cooling, gate drive circuitry and protection. Assembly and packaging are critical here as they affect the thermal performance, reliability, and overall efficiency of the module.
4. Converter design and assembly: To form a converter, power modules need to be integrated into the system. This includes: designing the circuit topology (e.g., half-bridge, full-bridge, or multi-level). Designing control circuits to control the switching action of the power module. Integrating the DC input power supply, DC-link capacitors, busbars, and protection circuits. Selecting the appropriate heat sink and housing for the converter to achieve higher power levels and provide physical protection.

Finally, converters can be integrated into larger systems. For example, power supplies for electronic devices, motor drives, inverters for solar panels, or any other application. This process demonstrates the multidisciplinary character of power electronics, incorporating materials science, semiconductor processing, electrical engineering, and thermal management.

Current research heavily focuses on Si IGBT modules and SiC MOSFET modules for two-level and three-level topologies. This thesis fucuses on the development of three-level power modules and converters. To achieve three-level topologies, many industrial applications use multiple two-level modules connected electrically. The advantage of this approach is that there is no need to consider the special internal

structure of the modules, and the system capacity can be increased by connecting multiple modules in parallel. However, it is not possible to reduce the parasitic parameters by changing the internal structure of the modules, and the converter size may be larger, with an increase in system losses and a higher cost due to the need for multiple modules.

Another way to implement a three-level topology is to use a three-level module directly, which, as a comparison, is usually able to optimise the output waveform using a simpler control strategy, and generally has better efficiency and lower losses, but increasing the system capacity may increase the cost.

In conclusion, power modules are more than simple integration of components, they also involve thermal management, electromagnetic compatibility, as well as driving and protection techniques. This thesis will analyse these aspects in a detailed study. The advent of power modules provides a simplified approach to enable efficient power conversion and control in a system more easily.

Recently, as an alternative to the use of power modules in power converters, printed circuit boards (PCB) embedded packaging technology has also been proposed to integrate power devices. The biggest advantage is to facilitate system integration. With the gradual maturity of the PCB process, the devices embedded in the printed circuit board, the system volume can be further reduced, and reliability can be further improved compared to traditional PCB.

Whichever of the above technologies, it is vital that they are investigated not only for technological and industrial progress, but also for meeting social and economic needs, achieving sustainable development, and protecting the environment.

To meet these trends, the general active research areas in power electronic systems are:

1. Use of new semiconductor materials (e.g. SiC/GaN)
2. New chip technologies: smaller structures, higher operating temperatures and current densities, higher stability.
3. Novel packaging technologies: optimised internal electrical connections, improved heat dissipation and reduced material costs.

4. Integration and modularity, which helps to reduce size and weight as well as improve system reliability and stability. Integration and modularity also help to simplify system design and reduce costs, for example by adding in a single package control, protection, and monitoring functions.
5. High frequency and high-power density packaging requiring low resistance and low parasitic inductance design.

1.2 Power Electronics System

Power electronic systems are a fundamental part of modern technology. They play an indispensable role in the efficient and flexible conversion and control of electricity. While the end of the previous section provided a variety of future directions for power electronics, they also provided a variety of potential challenges. This section describes the basic components and technical challenges of power electronic systems.

1.2.1 WBG Power Semiconductors

Previous studies have shown that the performance of Si power switching devices has reached its theoretical limits, which is determined by the fundamental material parameters [2] (e.g., the critical field for avalanche breakdown). Therefore, extensive research on new materials has been conducted in the past few decades, and the development focus on wide-bandgap (WBG) semiconductors, including SiC and GaN. They are attractive for advanced power devices due to their superior physical properties, these wide-bandgap materials can provide better performance [3]-[7]. SiC has many homogeneous polytypes with similar crystal structures, such as 3C-SiC, 6H-SiC, and 4H-SiC. In the field of power electronics, 4H-SiC is usually chosen to manufacture power devices. Table 1-1 summarises the comparison of the physical properties of semiconductor materials [8].

Table 1-1 Comparison of characteristics of different semiconductor materials

Properties	Si	4H-SiC	GaN
Bandgap Energy: E_g (eV)	1.12	3.26	3.39
Electron Mobility: μ_n (cm^2/Vs)	1400	950	1500
Hole Mobility: μ_p (cm^2/Vs)	600	100	200
Saturation Drift Velocity: v_{sat} (cm/s) $\times 10^7$	1	2.7	2.5
Breakdown Field: E_{br} (MV/cm)	0.23	2.2	3.3
Thermal Conductivity: λ (W/cmK)	1.5	3.8	1.3
Relative Permittivity ε	11.8	9.7	9.0

As can be seen from Table 1-1, SiC has ten times the dielectric breakdown field strength compared with Si, this means that SiC can withstand higher breakdown voltage, at the same breakdown voltage, SiC devices can be made to have much thinner drift layer with higher doping concentration. The resistance of high-voltage semiconductor devices is mainly determined by the width of the drift layer [9]. Under the same breakdown voltage, compared with the Si device, the SiC device can reduce the specific on-resistance in the drift region by 300 times [10]. The currently used Si MOSFETs support a maximum breakdown voltage of around 900V, while SiC MOSFETs can support a breakdown voltage of up to 1700V.

Fig.1-4 shows a comparison of three semiconductor materials, the bandgap determines the temperature limit for device operation, the breakdown field determines the stability and reliability of semiconductor devices at high voltages, a high breakdown electric field means higher voltage withstand capability [11]. High voltage operation means the possibility of less required devices. Thermal conductivity determines heat dissipation characteristic of semiconductor device, high thermal conductivity helps to reduce the operating temperature of the device and prolongs the life of the device, means less cooling is required. Saturation velocity affects the device's carrier transported switching speed, WBG semiconductor materials have higher saturation drift velocity and are therefore more suitable for high frequency and high-power applications. In conclusion, SiC MOSFETs offer several advantages over Si IGBTs: fast switching speed, high operating temperature, high breakdown voltage and linear current-voltage (I-V) characteristics [12]-[19].

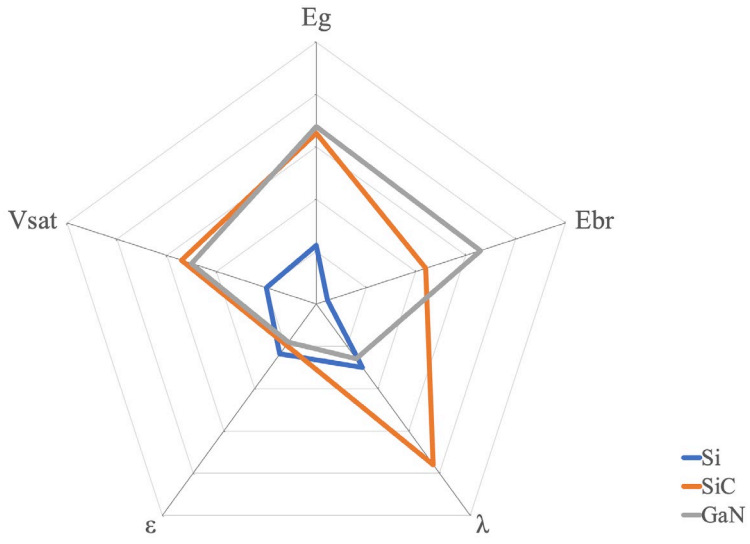


Fig.1-4 Physical parameters of different semiconductor materials

Overall, SiC can withstand higher voltages and temperatures, can operate at higher frequencies, switching faster, resulting in lower power losses and improved overall energy efficiency. Despite the above device advantages, SiC MOSFETs are not perfect and there are still some challenges that prevent SiC MOSFETs from entering mass market applications, and the disadvantages of SiC devices are listed below:

1. High manufacturing cost: The fabrication process for SiC devices is more complex compared to Si devices, which results in higher manufacturing costs for SiC-based products. At the device level, SiC MOSFETs still face challenges of gate oxide reliability and threshold voltage (V_{th}) instability [20]-[22]. However, costs are expected to decrease as the technology matures.

2. Material quality and defects: Some defective problems are still bothering SiC substrates and epitaxy [23], which can further affect device performance and production. Achieving high-quality, defect-free SiC substrates is challenging and increases production costs.

1. Limited market supply: Due to the relatively short time to commercialisation and low production yields, the market share of SiC devices has not yet reached the level of Si devices. This may result in a limited supply of higher priced SiC devices [24].
2. Relatively low current handling: Despite their advantages in voltage handling and thermal performance, SiC devices typically have lower current handling compared to Si devices, However, the current capacity of a single SiC device may be lower than that of a corresponding Si device due to the higher material and fabrication costs of SiC, resulting in SiC device designs that may favour high voltage over high current applications under the same cost and size constraints. This can limit their use in some high-current applications. While higher current handling can be achieved by paralleling multiple devices, current imbalance between parallel SiC MOSFETs is also a real problem in high-current applications, where unbalanced current distribution can lead to thermal imbalance and reduced reliability [25].

3. Complex gate drive circuits: SiC devices require dedicated gate drive circuits due to their unique electrical characteristics. The faster switching speeds of

SiC devices result in a high sensitivity to circuit parasitics [26]-[27], and therefore require precise gate control and the design of more appropriate power loop circuit layouts, which can be more complex to design and implement than Si devices.

Despite these limitations, the strengths of SiC described previously make it a semiconductor material with great potential for the future. Current research and development efforts are focused on addressing these weaknesses and further optimising SiC technology to release its full potential.

SiC MOSFETs combine the advantages of SiC materials and MOSFETs devices, they can withstand high breakdown voltage, have lower on-resistance, and fast switching. When turned on, since SiC MOSFETs have linear I-V characteristics [28], they have low conduction losses over a wide current range. MOSFETs do not exhibit the tail current that IGBTs do during turn-off, which requires additional time for the current to decay in IGBTs. This feature allows for sharper and quicker turn-off in MOSFETs, reducing energy loss during switching. Based on these reasons, SiC MOSFETs are more and more widely used in high-efficiency converters and industrial power supplies. Fig.1-5 shows a comparison of the working range of different power devices made of different materials [29].

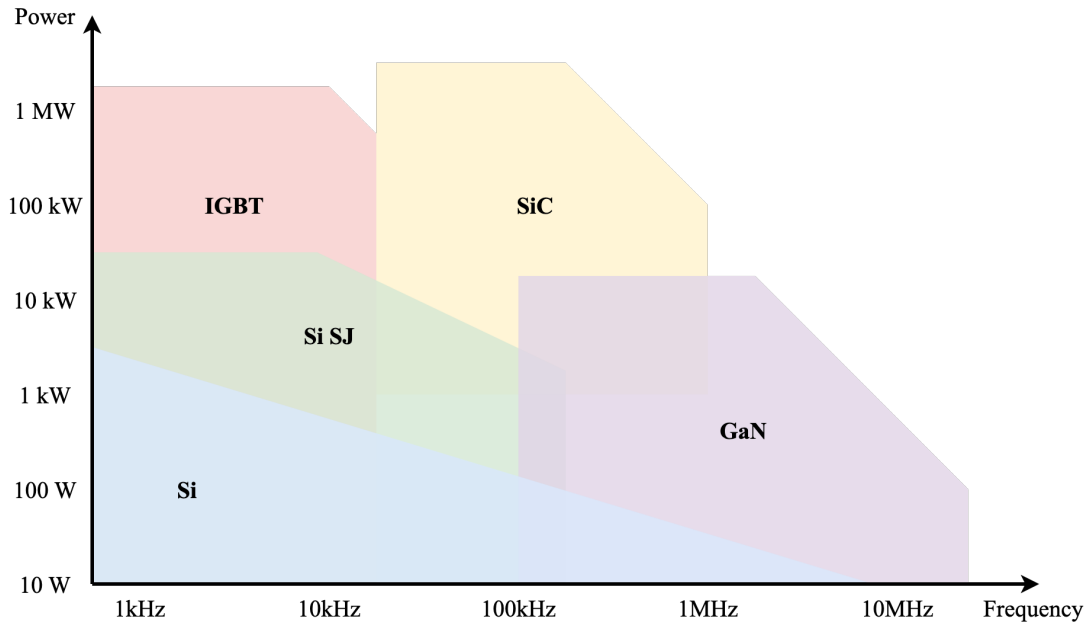


Fig.1-5 Power semiconductor device applications based on power and frequency levels

Efficient power conversion is heavily dependent on the power semiconductor devices used in the power conversion system. High-power applications are becoming more efficient and smaller in size because of improvements in power device technology. Such devices include IGBTs and SiC MOSFETs, which are a good fit in high-power applications due to their high voltage ratings, high current ratings, and low conduction and switching losses.

Specifically, applications with bus voltages >400V require device voltage ratings >650V to leave sufficient margin for safe operation. Applications including industrial motor drives, electric vehicles/ hybrid electric vehicles (EVs/HEVs), traction inverters and solar inverters for renewable energy are at the power level of a few kilowatts (kW) to a megawatt (MW) and beyond. Applications for SiC MOSFETs and IGBTs are at similar power levels, but split as the frequency increases, as shown in Fig.1-5.

SiC MOSFETs are becoming common in power factor correction power supplies, solar inverters, DC/DC for EVs/HEVs, traction inverters for EVs, motor drives and railway, while IGBTs are common in motor drives (AC machines), uninterruptible power supplies (UPSs), solar central- and string-type power inverters <3kW, and traction inverters EVs/HEVs.

1.2.2 Power Converters Using WBG Devices

The converter converts DC input to AC output, essential for power electronics, EVs, airplanes, and renewable energy. It is categorized into voltage type and current type converters based on the DC power supply. In the mid-20th century, medium and high-power converters used thyristor switching devices, however, the thyristors could not switch themselves off once they were turned on, and additional forced commutation circuits were required. Forced commutation circuits increase the weight, size, and cost of the converter, limit the switching frequency, and reduce system reliability. Based on technological advances, the vast majority of today's converters utilize fully controlled power semiconductor switching devices, and in this thesis, only converters consisting of fully controlled devices are discussed.

In order to meet the needs of high-power applications with higher withstand voltages and higher currents, one solution is to connect the devices directly in parallel

to increase the current rating, and to connect the devices directly in series to increase the withstand voltage rating. However, it is difficult to ensure that the current distribution during the operation of each switching device, especially during turn-on and turn-off, is identical [30]. Moreover, directly connecting devices in series or parallel usually requires lowering the operating frequency, so this is not the most effective measure to expand the output capacity of the converter. Other common ways to increase converter capacity are multi-level techniques. The primary reason for using MLCs is their unique voltage stacking capability, which effectively allows for an increase in voltage levels. This capability enables the combination of multiple lower voltage sources to produce a high voltage output, rather than relying on a single high voltage source. MLCs can generate output waveforms that are closer to a sine wave as they can switch between multiple different voltage levels. Such waveforms have lower Total harmonic distortion (THD), providing smoother voltage output, which is particularly important for applications requiring high power quality. This innovation started in the 1970s with the cascaded H-bridge (CHB) converter [31]. The circuit topologies of MLCs are varied and relatively complex, and several common topologies are described below, while a detailed numerical comparison of various MLCs will be analysed in Chapter 2.

In the last few decades, three-level converters have gradually gained interest as an alternative solution to the standard VSC. Among the many topologies that have been developed, these include neutral point clamped (NPC), T-type NPC (TNPC), Active NPC (ANPC), flying capacitor (FC), CHB, and other structures. Several studies have highlighted the advantages offered by three-level converters [32]-[37]. In these topologies, NPC and T-type are considered to be competitive solutions and have received the most research attention [38]-[40].

The three-level NPC converter proposed in [41] is widely used in the power electronics system. The converter's output terminal potential clamps to the neutral point potential. Compared with the conventional VSC, the NPC converter output contains less harmonic content. This three-level NPC converter is used to drive a three-phase induction motor, experimental results show that the output current contains very small low-order harmonics. A further advantage of the three-level converter circuit is that each main switching device is switched off at only half the

voltage of the DC side. Therefore, this circuit is particularly suitable for high-voltage, high-capacity applications.

[42]-[43] paid more attention to the research of three-level T-type converters, and developed an average loss model, in this model, losses are affected by different factors (e.g. modulation index, power factor). In addition to the low output harmonics mentioned above, three-level T-type converters also use devices with lower rated voltages and only use half of the DC bus voltage, resulting in lower switching losses compared to two level VSC. In these papers, experiments show that compared with two-level converter and three-level NPC converter, three-level T-type has a higher efficiency in the range of 10-30kHz. [42] also focus on the three-level T-type converter, the purpose is to prove the feasibility and advantages of using three-level T-type converter instead of two-level converter in low-voltage applications. By using a three-level T-type prototype for experimental measurement, the three converters were compared under different power factor angles and different switching frequencies. Within 10-30kHz, the efficiency of three-level T-type converter is significantly higher than that of two-level converter, while there is little difference within 10kHz, therefore, the trade-off between cost and efficiency can be considered in this range. In the frequency range above 30kHz, three-level NPC converter slightly exceeds three-level T-type in efficiency. However, it is worth noting that, unlike conventional NPC topology, the T-type cannot benefit from voltage stress splitting, which limits its use in high-voltage applications [44].

ANPC converter is an improved mid-point clamped MLC, which adds some active components to the conventional NPC converter to solve the problems of voltage balance and switching losses that exist in the conventional NPC converter [45]-[46]. ANPC converters can better balance the voltage of the DC side capacitor by adding additional active switches. By optimising the switching sequence, ANPC converters can reduce the switching losses and thus improve the efficiency of the converter. ANPC converters have gained significant interest in low- and medium-voltage power electronics applications [47]-[48]. However, due to the high cost of SiC switches, the use of six SiC MOSFETs per phase leg leads to a significant increase in the cost of the converter system [49]-[50], while the ANPC converter may have a higher structural and control complexity than a conventional NPC converter. To reduce the cost, some research [51]-[53] replace active switches from SiC MOSFETs

to Si IGBTs, the proposed topology utilises SiC MOSFETs to reduce the switching losses and achieves zero-current switching of Si IGBTs.

FC converters arose in the 1990s to achieve multi-level outputs by using flying capacitors to create intermediate voltage [54]. There is no DC link balancing problem due to the absence of neutral point. In this topology, the flying capacitor is used to replace the DC source while generating the voltage level. In general, FC converters have a modular design that allows higher voltage levels to be achieved by adding more capacitors and switches than the NPC converter, which provides flexibility in system design. However, the voltage control of the flying capacitor, the pre-charging of the capacitors during start-up and the large number of capacitors employed are the main challenges faced by such topologies [55]-[56]. FC topologies are not competitive in low to medium switching frequency applications due to the high cost of flying capacitors at low to medium switching frequencies [57].

Compared to conventional converters, MLCs typically use more semiconductor chips, resulting in larger volumes and requiring additional gate drive circuits. However, the increased number of output voltage levels and the step reduction in voltage amplitude allow MLCs to significantly improve the quality of output voltage and current. This improvement reduces the need for Electromagnetic Interference (EMI) filters and improves load efficiency. According to the above content, Fig.1-6 summarises the classification of mainstream MLCs topologies. This classification highlights the different approaches to achieving multi-level conversion, either through a single DC source with various clamping methods or through multiple DC sources with cascaded H-bridges.

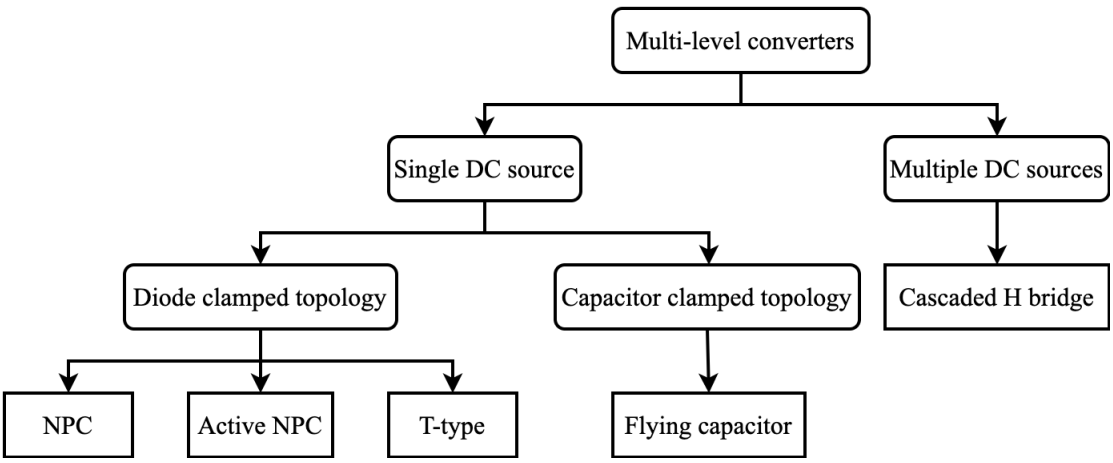


Fig.1-6 Multi-level converter classification

1.2.3 Power Electronics Packaging and Power Module

This section examines the fundamentals of power electronics packaging and power modules, emphasizing their role in modern power systems. Power electronics packaging involves encasing electronic components and circuits in protective casings to enhance system reliability, performance, and efficiency under diverse environmental conditions. The process covers encapsulating electronic components and integrated circuits in a suitable case or package to protect them and provide the necessary connections, which increases the durability of the equipment and reduces the failure rate while also improving the overall performance and efficiency of the system.

A MOSFET die represents an unpackaged semiconductor chip from the manufacturing process, used directly in product integration without leads or casing. Power modules, typically integrating multiple semiconductor devices like IGBTs, MOSFETs, and diodes, come in compact, user-friendly packages. They include necessary circuitry and thermal management, offering electrical and mechanical support. These modules address specific power and voltage needs, ensuring efficient power conversion and control, crucial for high-power applications.

Currently on the commercial market, the power modules used in high voltage and high current applications are mainly occupied by IGBT modules [58] that combine Si IGBTs and Si FRDs (fast recovery diodes). According to the above introduction, the power modules made by SiC can reduce the switching loss caused by the tail current and the diode recovery current and can work in the high frequency range. Therefore, it has very good development prospects, and the following literature specifically analyses the advantages of SiC power modules.

In order to verify the fast-switching capability of the SiC power module, [59] firstly evaluated the static current-voltage characteristics and capacitance-voltage characteristics, and then evaluated the performance of using SiC devices and Si devices in a DC-DC boost converter through experiments, indicating that due to the small input capacitance and lower Miller effect, SiC module has fast switching capability. However, the experimental results show that compared to the Si IGBT power module, a larger voltage oscillation will produce in the SiC MOSFET power module when the switch is turned off. Through the double pulse experiment, [60]

verified that the sic module can reduce the conduction loss and the diode reverse recovery loss, and the performance is tested in the three-phase permanent magnet motor platform. Through observation and comparison, the reverse recovery current of the Si diode is much higher than that of the SiC diode under the same forward current, thus the reverse recovery loss of the diode is reduced due to the smaller reverse recovery current in the module. When comparing different modules with the same three-phase permanent magnet motor load, obtained in a very wide range of speed, the efficiency of the SiC module is higher than that of the Si module. This paper uses a hybrid SiC power module and does not use a full SiC power module. Although the performance improvement is not as great as that use of a full SiC module, it also verifies the advantages of SiC materials. In [61], the developed full SiC power module is applied to the traction inverter. Compared with the Si IGBT module, under the output power of 220kW, the weight and volume of the SiC module are smaller, and the achieved power density is more than 50% higher than that of Si IGBT modules. In a wide output power range, the efficiency of the full SiC MOSFET module is higher than that of Si IGBT module.

At present, in some special applications, the power module needs to work at a higher temperature (> 200°C). In order to meet this demand, special power module packaging technology is needed. [62]-[63] improve the heat dissipation design, use air cooling, and use a new bonding technology for interconnection. Performance tests are carried out through experiments, and the results show that these modules can run above 200°C, which is higher than the 150°C operating temperature of traditional Si IGBT power modules. At the same time, a comparison of switching losses has been carried out, and it is found that the switching loss of SiC MOSFET modules is one third of that of Si IGBT modules. As packaging technology is still developing rapidly, reliable packaging and optimisation at high temperatures still have much room for improvement.

Fig.1-7 shows a typical SiC power module package, typically, power modules consist of a multi-layer structure with heterogeneous materials including semiconductor devices, substrate, baseplates, and solders, etc. The heat generated by the power devices is transmitted vertically through the substrate and baseplate to the heatsink, and the electrical connection between the devices is mainly achieved through aluminium bonding wires. This type of package generates a high current

density at the bonding wires, which results in relatively high temperatures. High interconnect reliability can be achieved by low-temperature silver sintering of power devices, increasing reliability by a factor of about 10 [64].

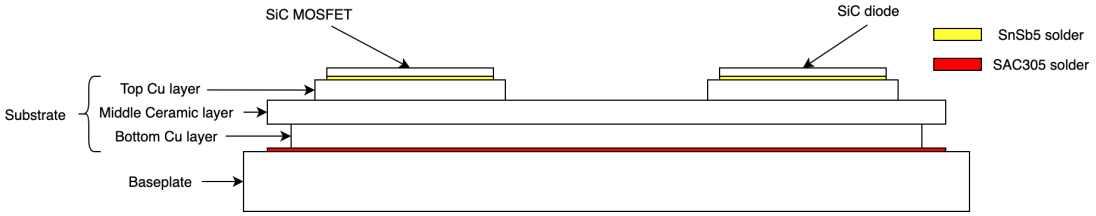


Fig.1-7 Cross sectional diagram of a typical SiC power module

The packaging of power modules requires suitable material selection, packaging materials and technologies must be adapted to the stringent thermal and electrical constraints [65]-[67]. Table 1-2, Table 1-3 lists the physical properties of some common materials used in power modules. Materials with closer coefficient of thermal expansion (CTE) will enhance the lifetime of the module and can reduce the stresses in the interface materials and internal materials, the higher the thermal conductivity, the lower the Junction-case thermal resistance will be and the lower the junction temperature difference in operation.

Another important characteristic is the material density, especially the substrate, for example, using the copper substrate as a reference, the density of AlSiC material is 1/3, while CuW has twice the density, so AlSiC will provide considerable weight reduction and improve reliability. With the reduction in material cost, Si_3N_4 is highly recommended for power module packaging. Si_3N_4 has a similar CTE as Si, resulting in lower thermo-mechanical stresses during temperature changes. As a result, power modules packaged in Si_3N_4 have improved reliability in high power and high temperature SiC packages.

Table 1-2 Relationship between the combination of coefficient of thermal expansion and thermal conductivity of different materials and thermal resistance

	CTE (ppm/K)	Thermal conductivity (W/mK)	Rthjc (K/W)
Silicon die	4	136	
Cu/Al_2O_3	17/7	390/25	0.35
$AlSiC/ Al_2O_3$	7/7	170/25	0.38
Cu/AlN	17/5	390/170	0.28
AlSiC/AlN	7/5	170/170	0.31
$AlSiC/Si_3N_4$	7/3	170/60	0.31

Table 1-3 Typical properties of different materials for substrates and substrates

	Material	CTE (ppm/K)	Thermal conductivity (W/mK)	Density (g/cm^3)
Baseplate	CuW	6.5	190	17
	AlSiC	7	170	2.9
	Cu	17	390	8.9
Substrate	Al_2O_3	7	25	
	AlN	5	170	
	Si_3N_4	3	60	
Die	Si	4	136	
	SiC	2.6	270	

The objective of SiC module packaging is to realize its application at high temperatures and high frequencies, so a series of new considerations for packaging must be made. The development trend of SiC power semiconductor packages is mainly reflected in three aspects: module structure, materials, and technology.

In conclusion, SiC power module has the advantages of high efficiency, lower losses, high temperature resistance and high-power density. Therefore, it is widely used in automotive, aerospace, PV, and other industrial fields. For example, in EVs, SiC power modules can improve charging efficiency and shorten charging time [68]; in aircraft power system, it can reduce the weight and heat generation of the whole system and improve efficiency [69]-[71]; it reduces the effect of common mode voltage for PV inverters [72].

1.3 Overview of Non-ideal Effects of Power Electronics

In the rapidly evolving field of power electronics, the performance of a system depends not only on the ideal behaviour of the components but is also significantly affected by a range of non-ideal effects. These effects are often due to physical and practical limitations of components and materials, and they present challenges that require complex engineering solutions. A more comprehensive overview of these non-ideal effects is provided below, focusing on their impact on system design and operation.

1. Loss Mechanisms: The loss mechanisms of power devices include conduction losses, switching losses, and reverse recovery losses. Conduction losses occur during device conduction due to the resistance of the conduction path, depending on the conduction resistance and current. Switching losses happen during the transition between “on” and “off” states, influenced by switching

frequency, device characteristics, voltage and current during the transition, and switching times. Reverse recovery losses occur in power diodes when stored charge is removed during the switch from on to blocking state, causing brief reverse current flow. To reduce these losses and enhance system efficiency, selecting devices with low on-resistance, low reverse recovery time, and low gate charge, along with optimising circuit design, is essential. Understanding and managing these loss mechanisms is critical for improving the efficiency and reliability of power electronic systems.

2. Parasitic Effects: In electronic circuits, components inherently have parasitic components such as parasitic capacitance, inductance and resistance. These components, although unintended and may be present in the component itself or in the layout of the circuit board, can cause energy loss, oscillations, voltage overshoots, and other undesirable effects. Parasitic inductors and capacitors, in particular, can cause ringing and oscillation in circuits, which not only interferes with the normal performance of the device, but can also cause additional losses.
3. Thermal Management Challenges: Power devices generate heat due to internal losses during operation, which not only affects their performance and efficiency, but may also shorten the service life of the equipment. Without effective thermal management measures, excessive heat accumulation can lead to performance degradation or even equipment failure. Especially when the heat is excessive, it may lead to thermal runaway, causing the device temperature to rise to the point of self-destruction. Therefore, it is critical to develop efficient thermal management solutions that help ensure that heat is dissipated efficiently and that device temperatures are maintained within safe operating ranges, thus avoiding early failures due to overheating.
4. Electromagnetic Compatibility: The nonlinear components and switching actions of power electronic devices can generate harmonics and EMI that can affect the performance and reliability of other electronic devices and systems. Noise generated by power electronic circuits can interfere with other equipment by conduction or radiation. EMI is particularly influential on the performance of sensitive equipment and must be carefully considered and controlled at the design stage, for example using shielding, optimised layouts and the addition of filters.

In summary, these non-ideal effects must be fully considered and addressed in the design and application of power electronic converters. By optimising device losses, improving thermal management, reducing parasitic effects and controlling EMI, the performance and reliability of the system can be significantly enhanced, extending the lifespan of the equipment. These efforts not only help to enhance the overall efficiency of the power electronics system, but also ensure its stable and reliable operation in various application environments.

1.3.1 Power Losses in Converters

Power losses in power electronics systems have a significant impact on their performance, reliability, and efficiency. These systems are integral to a variety of applications ranging from power supplies, renewable energy systems, to EVs. Their primary function is to convert and control electrical power, however, this process is not entirely efficient, and some energy is inevitably lost in the form of heat. Power losses in power electronics are primarily divided into three categories: conduction losses, switching losses, and reverse recovery losses. These power losses lead to an increase in the temperature of the device, and if not properly managed, can cause device failure. Therefore, it is essential to design power electronic systems that minimise these losses and effectively dissipate the heat generated [73]-[74].

1. Conduction losses: Conduction losses refer to the power dissipated due to the resistance of the conduction path when a semiconductor device is in the “on” state. As the current flowing through the device increases or the on-resistance increases, these losses also rise. When current flows through a semiconductor device, the internal resistance causes energy to be dissipated as heat. Conduction loss is generally proportional to the square of the current flowing through the device and depends on the device’s on-resistance. This type of loss is typically the most significant among all types of losses.
2. Switching losses: The switching devices of a power electronic converter incur switching losses each time they are switched on or off. During the state transition, both the voltage across the device and the current flowing through it are non-zero, causing energy to be dissipated as heat, thereby resulting in power losses. The switching frequency and device characteristics, such as the

gate charge of the MOSFET, have a significant effect on the extent of these losses.

3. Reverse recovery losses: In rectifier diodes and some types of MOSFETs, the charge stored in the diode needs to be removed when the diode switches from the on state to the off state. Losses are incurred in this process, which are called reverse recovery losses. In MOSFETs, the body diode is a built-in component with reverse recovery time and reverse recovery losses. This body diode acts during reverse conduction of the MOSFET. For SiC MOSFETs, the reverse recovery losses of the body diode are typically much smaller than that of Si MOSFETs due to the characteristics of the SiC material. Furthermore, many high-performance SiC MOSFET power module designs use an additional Schottky diode to further minimise reverse recovery losses. This is because Schottky diodes have no carrier storage and therefore no reverse recovery loss. Since this thesis focuses on the performance of SiC-based power electronic systems, it will not be overly concerned with reverse recovery losses.

On this basis, it is crucial to understand the specific mechanisms of these losses in different converter topologies. It is especially critical to develop more accurate models to predict and reduce power losses by studying the behaviour of power devices and semiconductor devices such as diodes. The literature extensively examines losses in two-level and three-level converters, focusing on semiconductor losses. While approximations of IGBT and diode I–V switching characteristics, some earlier studies [75]-[77] have been used to estimate switching losses, an alternative, more straightforward method employs the switching energy–current (Esw–I) characteristics. This approach indicates that the switching losses of an IGBT–diode pair approximately correlate with the switching voltage and current, as detailed in [78]. Research on switching losses, utilizing a second-order approximation of the IGBT and diode Esw–I characteristics, is presented in [79] for a three-level NPC converter, along with analytical formulas specific to switching losses in two-level converters. It is noted that for two-level converters, all continuous pulse width modulation (PWM) techniques yield identical switching losses, irrespective of the load phase angle [80].

Regarding conduction losses in two-level converters, detailed formulas are provided in [76] and [81]. These calculations hinge on the linear I–V characteristics of IGBT–diode modules. Differing from switching losses, the conduction losses in two-level converters are influenced by the choice of PWM strategy and the load power factor. For NPC converters, expressions accounting for various modulation strategies are documented in [82]. Regarding the calculation of different losses, several methods have been proposed. [83] proposes a fast calculation method based on the datasheet. The MOSFET is modelled, the amount of stored charge is related to the energy in the parasitic capacitance to calculate the voltage drop and rise time. The theoretical model was verified through experiments, and finally it was proved through comparative data that the model can allow the estimation of losses within the error range of up to 10%. It is worth noting that the module assumed and used in this paper has a low stray inductance, so the voltage oscillation is relatively small, when the stray inductance is large, the model may no longer be valid, or the charge calculation needs to be corrected.

1.3.2 Parasitic Parameters and Reduction

Parasitic inductance has a significant effect on the turn-on and turn-off processes of power switching devices. This is mainly due to the voltage response of parasitic inductance in the face of current variations. This effect is particularly noticeable in high-frequency, high-speed switching applications. The following are the main effects of parasitic inductance of power switching devices [84]-[86]:

1. Overvoltage: When a power device is switched off, the current flowing through the switching device attempts to fall rapidly to zero. However, due to the presence of parasitic inductance, a voltage surge is produced across it that is proportional to the rate of change of current. This can cause a rapid rise in switching voltage that may exceed the device's rating and damage the device. The overshoot voltage dV is equal to the parasitic inductance multiplied by the rate of change of current di/dt. Fig.1-8 describes the voltage overshoot caused by the inductance.

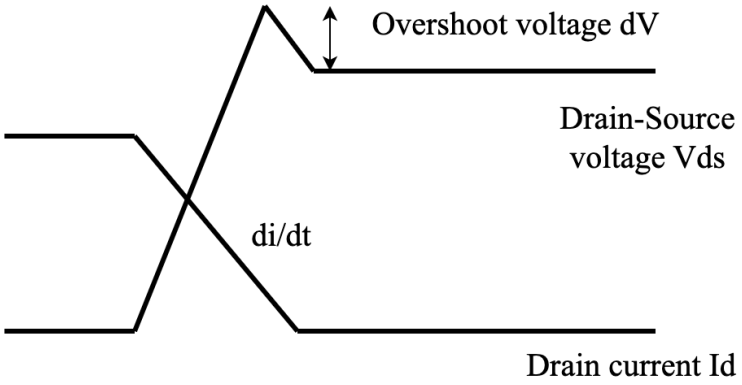


Fig.1-8 Voltage overshooting caused by parasitic inductance

2. Delayed turn-off: The turn-off time of a switching device may be slightly delayed due to the inductance limiting the rapid change in current.
3. Increased switching losses: During turn-on and turn-off, the transitions in current and voltage due to parasitic inductance are not instantaneous, meaning that during these transitions the device is between on and off states, resulting in additional switching losses.
4. Oscillations: Parasitic inductors and other capacitors (e.g., MOSFET output capacitance C_{oss}, or other parasitic capacitors) may form an LC oscillating circuit, causing oscillations in the voltage and current on the device. This not only increases switching losses but may also interfere with the normal operation of other parts.

As mentioned in the previous subsection, The SiC MOSFET and with no reverse recovery SiC schottky barrier diode (SBD) can reduce the reverse recovery current and thus further reduce the switching losses [91]. However, they also aggravate oscillations during switching [88]-[89], making SiC MOSFET and SiC SBD more suitable for high-frequency converters. These effects may be more noticeable in power modules due to their more complex interconnections, higher currents, and more stored electromagnetic energy. To simulate and mitigate these negative effects, the parasitic inductance of these high-speed power modules needs to be improved.

The fast-switching capability of a power device is affected by the parasitics introduced due to the semiconductor die itself and the package of the module itself, as the latter produces a fraction of the overall parasitic inductance. More detailed parasitic parameter models can be obtained by considering the parasitic inductance of the module package, i.e., copper busbars, terminal pins, and bonding wires. Fig.1-9

shows the parasitic parameter model for one phase leg of a two-level module. The model describes the power module during switching transients. This model includes the gate capacitance (C_{gs}, C_{gd}), output capacitance (C_{ds}), gate inductance (L_g), drain and source inductances (L_d, L_s) introduced by the MOSFET die itself.

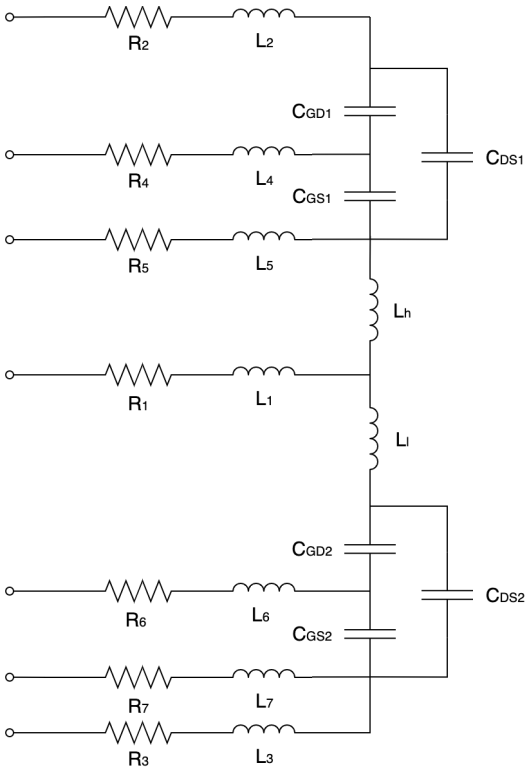


Fig.1-9 Parasitics of the SiC MOSFET die and parasitics added by the packaging

It is widely recognised that commutation inductance causes significant voltage overshoot and ringing at turn-off [90]-[94], Therefore, minimising these parasitics in the design of power modules is an important challenge for high-performance converter systems.

Due to the difficulty of reducing the parasitic parameters of the MOSFET die itself, the question of how to minimise the parasitic parameters of the package has become a recurring theme in the literature on WBG power modules and their applications over the last few years [95]-[99]. New module designs with much lower parasitic inductances inside the module than their predecessors have been introduced for high power modules. [100] measured the parasitic inductance of SiC power module and found that the inductance between the terminals of the module is as low as about 15nH, compared with the IGBT module with the same structure has 40nH stray inductance. The module arranges internal bonding wires to make the drain

current and source current as close as possible to reduce stray inductance. The power module used in [101] removes the bond wires, using a new planar packaging technology to achieve low-inductance design, and apply a RC-C snubber between the two DC terminals DC+ DC- to reduce the loop inductance. [102] proposes a SiC half-bridge power module. The low inductance design of the module comes from minimising the length of the power loop and choosing to increase the width of the power terminals to distribute the current evenly among each device. [103] shows a sandwich SiC power module structure without bonding wires. In order to minimise the parasitic inductance caused by the wiring between the positive and negative terminals (DC+/DC-), the design connects the source of the upper semiconductor and the drain of the lower semiconductor to the same substrate, compared with the traditional bonding wire connection, this can shorten the wiring length between the upper and lower semiconductors. Integrating the DC bus capacitor and gate driver in the power module can reduce the parasitic inductance in the commutation loop and gate loop of the half-bridge power module [104]. Through simulation comparison, it is found that the power module with integrated DC bus capacitor can reduce the voltage overshoot by three times, the stray inductance reduced by three times to 7.2nH. Other power modules use multi-layer substrates, including three layers of copper and two layers of ceramics, to achieve 1.15nH stray inductance. Such a substrate design can compensate for the thermal effect of ceramics because heat is diffused in the copper layer [105]. [106] provides another way to reduce stray inductance by using laminated busbar and snubber capacitors. Since the inductance of the laminated busbar is proportional to the distance and length, and inversely proportional to the width, the relationship between the length and width of the busbar needs to be considered in the design, and finally the optimal aspect ratio is obtained through modelling and analysis. The buffer capacitor can compensate the inductance between the main capacitor and should be placed as close as possible to the power module. However, too many capacitors will cause the bus circuit to be longer, which will increase the stray inductance. Therefore, it is necessary to conduct multiple simulations and experiments to determine the best solution.

To design and optimise the internal circuit layout of the power module, simulation modelling is required when designing the power module. The goal of packaging is to obtain a low-inductance power module that can work at high power. In any case, the

result is that many key components are very close to each other, and the multiphysics coupling effect becomes more prominent. Finite element method (FEM) is very effective for solving the partial differential equations involved in the mathematical expressions of many physical phenomena (electromagnetic, mechanical, thermal).

Minimisation of module parasitics is most easily achieved by using modelling tools to assess the impact of system constraints and design approaches on performance. Due to time and cost constraints, it is often not feasible to evaluate intermediate design solutions through hardware prototyping. Instead, computationally based methods such as FEA and partial element equivalent circuit (PEEC) can often be used for this purpose. The package of the SiC power module needs to reduce the parasitic impedance. To achieve this goal, most packages are as compact as possible. However, this will cause difficulties in the measurement of electrical parameters, so in order to obtain these parameters, need to rely more on simulation. Electromagnetic modelling relies on numerical techniques used to solve Maxwell's equations in terms of unknown electric and magnetic field distributions and/or current and charge distributions in space. To simulate the module's inductances, a quasi-static EM solver, in this case ANSYS Q3D Extractor, was used, the workflow of Q3D is shown in Fig.1-10. The software allows for visualising the current distribution at high frequencies and extracting self and mutual inductances of current paths. Q3D has been used to evaluate parasitic inductance in SiC MOSFET power modules [107]-[111], and Si IGBT power modules [112]-[113].

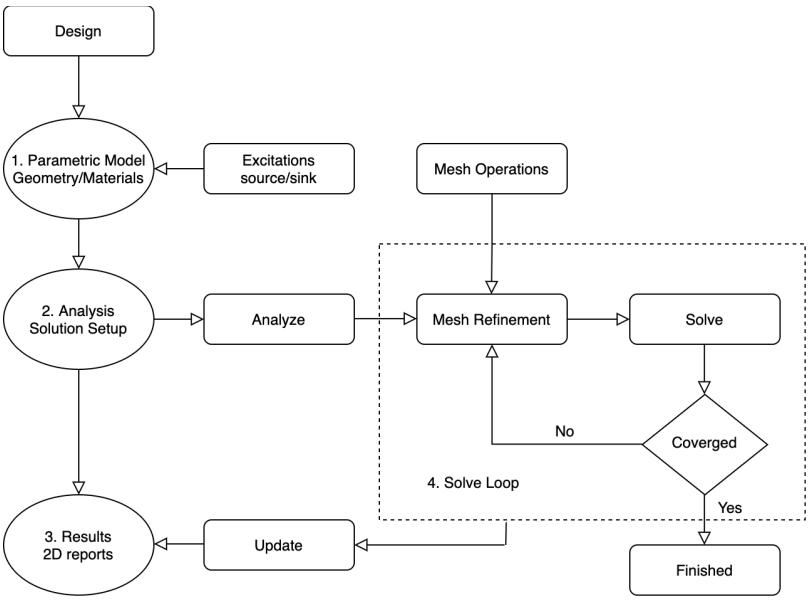


Fig.1-10 Q3D solve procedure

Two electromagnetic modelling methods are introduced in [114] to extract the parasitic parameters of the power module package. The first is to use the ANSYS Q3D Extractor solver, and the second is to use the PEEC solver. The second solution method has good prospects and can solve some of the limitations of Q3D electromagnetic modelling. This paper takes TO-247 package and sic half-bridge power module as examples to verify these two modelling methods respectively, analyse the advantages and disadvantages of the two methods, and prove that the PECC method can more accurately predict the parasitic parameters of the package, However, further improvements are needed to increase the calculation speed. [115] provides design ideas for power modules, Fig.1-11 shows the flow chart of designing a power module, this paper focuses on the role of different software in the design process and the sequence of use.

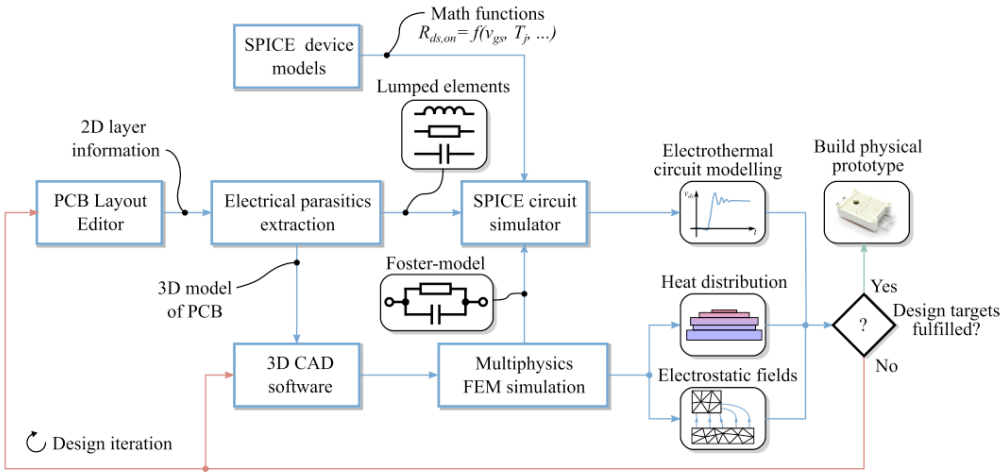


Fig.1-11 A design example of power modules [115]

The method presented in the previous subsection can be effective in quickly obtaining the parasitic parameters, however, very large and complex models may require a significant amount of computational time and may not easily converge, and detailed structural information about the internal structure of most commercial power modules is not available to obtain the partial parasitic inductance through software modelling. Measurement-based methods can be further divided into two subcategories: time-domain reflectometry (TDR) and frequency-domain impedance measurements. TDR is a technique used to measure and locate faults in a cable or transmission line. TDR works by sending a pulse or high-speed stepping signal to the cable and then measuring the signal that is reflected back. Based on the timing and amplitude of the

reflected signal, the location and nature of the fault can be determined [116]-[117]. TDR methods require complex experimental setups, special hardware (TDR/sampling header) and software, as well as an iterative multistep process, and are thus practical applications are limited. Frequency-domain impedance measurements are a technique for measuring resistance, capacitance, inductance, or other complex impedance values at different frequencies. Such measurements are usually done using a network analyzer or frequency response analyzer. The purpose of the measurement is to understand and analyse how the electrical impedance of a particular circuit changes as the frequency changes. The impedance measurement method has gained wide acceptance as a simple and easy-to-use technique with higher accuracy and ease of use for circuit designers [118]-[121]. This method basically involves making frequency domain impedance (Z-parameter) measurements between two terminals of a power device by means of an impedance analyzer or a vector network analyzer (VNA). However, this impedance measurement is currently limited to a single-port configuration between two device terminals, with the third terminal floating during the measurement. As we will demonstrate in later sections, the unconnected floating terminal introduces significant measurement errors due to parasitic coupling to ground. For microwave field effect transistors such as GaAs MESFETs, a characterization technique based on VNA-based S-parameter measurements was developed to extract small-signal equivalent circuits and intrinsic components [122]-[124]. This S-parameter measurement method has also been applied to Si power MOSFETs [125], but it requires a cumbersome de-embedding procedure prior to S-parameter measurements and iteratively obtaining the inductance values by converting and matching the Y parameters with the reference Y parameters, which inevitably increases the complexity of the measurements and reduces the measurement accuracy. A simple two-port measurement technique and applied it to some discrete power MOSFETs is proposed [126] and Si IGBT power modules with satisfactory results [127].

1.3.3 Thermal Management

Thermal management of power modules has become an important area of research due to the increasing demand for high performance electronic systems. Efficient thermal management of these modules is essential to ensure their reliability and longevity, as high temperatures can cause permanent damage and shorten the life of

electronic components. A number of approaches have been proposed for thermal management of power modules, including the use of heat sinks, forced air cooling, liquid cooling, and phase change materials (PCM) [128]-[130].

1. Heat sinks are common thermal management tools that increase the surface area for heat dissipation. Typically made of highly conductive materials like aluminium or copper, heat sinks are designed to maximise heat transfer from the power module to the surrounding environment.
2. Forced air cooling uses a fan to circulate air over the power module, increasing the heat transfer rate to the environment. Due to its low cost and ease of operation, it is widely used in high-power systems such as data centres and power electronics. However, fans can present noise and reliability issues and are limited by ambient temperature.
3. Liquid cooling has proven to be an effective thermal management method because it has a higher thermal conductivity compared to air cooling. The use of liquid cooling also allows for a compact cooling system, which is beneficial for space-constrained applications. However, liquid cooling requires a closed-loop system, which increases the cost and complexity of the thermal management solution.
4. PCM has been proposed as a thermal management method because these materials undergo a phase change at a specific temperature, providing greater heat storage capacity. PCM can be used alongside other thermal management strategies to enhance overall performance. PCM has proven effective in reducing temperature spikes in high-power systems.

The choice of thermal management strategy depends on the system's specific requirements and may include heat sinks, forced air cooling, liquid cooling, or PCM. Effective thermal management is critical to ensuring the reliability and longevity of power modules, as high temperatures can cause permanent damage to electronic components. Using SiC power modules, which have lower conduction and switching losses, can help simplify thermal management, much research has been conducted on thermal management of power modules.

In addition to the low-induction design of the power module [101] also provides a real-time temperature monitoring technology. The principle of this method is that the

threshold voltage V_{th} and the on-state voltage $V_{ds(on)}$ of the power MOSFET change linearly with temperature within a certain working range. Through the measured threshold voltage and/or on-state voltage, find $T_j(V_{th})$ and/or $T_j(V_{ds(on)})$ on look-up table to estimate the temperature.

The thermal response and high-temperature operating capability of the SiC power module was evaluated through experiments and numerical values [131], and the temperature dependence of the module's thermal dynamics was modelled for thermal analysis. The electro-thermal model is analysed by combining the electrical characteristics of the SiC device and the equivalent thermal circuit. Numerical analysis results show that SiC devices in power modules can operate at high temperature and reduce heat dissipation through simplified cooling systems. The numerical results of electrical response and thermal response are consistent with the experimental results from ambient temperature to extremely high temperature. However, this method will waste a lot of time when analysing a complex structure and a large number of modules, it is not suitable for all applications. This aspect requires subsequent research and improvement.

[132] studies the static and dynamic modelling and loss prediction methods of SiC power modules. The static model uses the expression of the channel current to describe the transfer and output characteristics at different temperatures. The dynamic characteristic model includes the junction capacitance, dynamic transconductance and stray parameters of the package. On the basis of these two models alone with the thermal network, a method for predicting loss and junction temperature is proposed. This method integrates the voltage and current obtained through the model to calculate the losses. If the power losses are applied to the RC network, it can be equivalent to the current from the junction temperature terminal to the case temperature terminal to calculate the junction temperature.

A simplified analytical thermal model of the power module was developed in [133]. This model considers the thermal interaction between different module chips based on the analysis method. The thermal interaction between components depends on the boundary conditions, the value of the power dissipation in the different components and the number of working chips. Modelling this effect as simply calculated energy and thermal resistance allows a reasonably low measurement of the

module. A method is proposed to use RC network to evaluate thermal resistance and thermal capacity, then estimate the transient thermal resistance of semiconductor devices.

[134] using the simulation software COMSOL Multiphysics to conduct thermal simulation and fluid dynamics simulation, to obtain the change of thermal resistance under different coolant temperature and fluid velocity. The results show that the thermal performance of the half-bridge power module using epoxy resin lead frame module is improved by about 40%, and the parasitic inductance of this module is 12nH, which is about 40% less than the DCB-based module. In addition, the double pulse test shows that the overcharge voltage can be reduced when the DC link capacitor is integrated inside the module.

Most power modules use a heatsink-fan cooling system, but the geometry of the heatsink and fan operating point will affect the thermal performance. [135] proposed a model to predict the performance of the fan and verified the results through numerical simulations and experiments. The results show that using this model with a given thermal resistance can reduce weight to the greatest extent.

[136] used software to simulate the thermal model of the power module and constructed a compact RC network consisting of 115 R and C, then used the model to predict the temperature of the SiC MOSFET. It is further integrated into the LTspice model, and the losses and junction temperature of the MOSFET under different frequency ranges are predicted through electromagnetic thermal simulation, which proves that the module has good electro-thermal performance. This paper shows that power modules can be effectively designed by using simulation software that already exists in the market. The tools used in this article include Abaqus for thermal modelling, Maxwell for electromagnetic modelling, and LTspice for electrical and electro-thermal simulation. The accuracy of simulation can be improved through experimental evaluation.

In the thermal management of power modules, the FEM and CFD are two important tools that help to optimise the heat distribution of electronic devices and the design of the cooling system to ensure that the device operates stably within a safe temperature range [137]-[140].

1. FEM: FEM is used for thermal analysis to evaluate and optimise the temperature distribution and thermal management of components. The process involves discretizing structures into small elements, applying control equations to each element, numerically solving these equations, and post-processing the results. FEM helps identify hot spots, optimise heat sink designs, and select appropriate thermal materials. For example, FEM can analyse and optimise the thermal behaviour of inductors and power switches in a power converter.
2. CFD: CFD simulates fluid flow and heat transfer around components to optimise cooling system designs. This process includes meshing the problem domain, defining initial and boundary conditions, solving the Navier-Stokes equations, and visualizing the results. CFD is used to optimise the position and speed of fans or the layout of liquid cooling systems, ensuring stable operation and extended lifespan of electronic devices.

Combining FEM with CFD enables multi-physics coupled simulations that simultaneously model electrical, thermal, and fluid phenomena, accurately predicting the thermal behaviour of power modules. Accurate simulation thermal models can quickly evaluate and improve design schemes, reducing the cost and time of physical experiments. By combining simulation technology and sensor data, real-time monitoring and dynamic adjustment of the power module are realised to ensure that the system is always in the best operating condition, thus significantly improving its thermal management efficiency and reliability.

1.4 Scope and Overview of Research

1.4.1 Aim and Objectives

The aim of this thesis is to conduct a comprehensive analysis and exploration of various SiC converter technologies, with a particular focus on the design, optimisation, and performance analysis of three-level NPC topology power modules and converters. The research seeks to bridge the gap between theoretical studies and practical applications in the field of power electronics, especially in converter technology. The study primarily targets applications with a DC bus voltage of 540V/1080V and a single-phase output power of around 100kW, such as aircraft starter-generator systems, EV motor drives, renewable energy systems, and industrial motor drives.

This research reviews existing converter topologies and their applications across different fields, analysing and comparing the design principles and performance characteristics of two-level and three-level converters. It identifies the advantages and limitations of both in various applications, with a detailed comparative analysis of MLCs that highlights their benefits over traditional two-level converters, aiming to enhance the operational efficiency of power electronic systems, reduce harmonic distortion, and improve power levels. Additionally, in response to the growing demands of More Electric Aircraft (MEA), there is a need to develop a highly efficient, high-power-density three-level SiC power module. This includes the design and optimisation of power modules capable of operating at higher DC bus voltages and under the worst-case scenario environmental conditions, meeting the stringent electrical and thermal management requirements inherent in aerospace environments. The core objective of the research is to develop a three-phase three-level power converter based on the designed power module, using new methods to measure the parasitic inductance of MLCs and verifying their accuracy through double-pulse tests (DPTs) to evaluate the electrical performance of the converter.

1. Conduct a comprehensive review of existing converter topologies used in various applications, such as renewable energy integration, EV propulsion, industrial motor drives, and aerospace systems. Identify the key features, advantages, and potential drawbacks of two-level and three-level converter topologies, with a focus on the benefits of three-level converters, including increased efficiency, reduced harmonic distortion, and enhanced power capability.
2. Evaluate the performance characteristics of different switching devices used in converter topologies by analysing datasheet parameters. Establish PLECS models to simulate and analyse the impact of these devices on the overall converter performance.
3. Develop and simulate various three-level converter models, comparing their electrical characteristics, such as switching losses, conduction losses, and THD, with those of two-level converters using PLECS. Conduct a numerical comparison and analysis of the electrical performance of these models.
4. Assess the suitability of different converter topologies for use in aircraft starter-generator systems. Provide recommendations for the optimal topology

based on the specific requirements of aerospace applications. Analyse and study the performance indicators critical to different applications.

5. Develop a three-level NPC power module capable of operating at 540V/1080V DC bus voltage, ensuring that each phase of the module can deliver 100 kW of output power. Evaluate and select power semiconductor devices, such as SiC MOSFETs and diodes, based on performance indicators like on-resistance, maximum current, and thermal characteristics to enhance performance and reliability.
6. Perform detailed electrical simulations of the three-level NPC converter under worst-case operating conditions, focusing on evaluating converter performance, including power losses and efficiency of different devices.
7. Model and analyse parasitic inductance in the power module, optimising the layout to minimise parasitic inductance, reduce voltage overshoot, and improve switching performance.
8. Execute detailed thermal simulations to analyse both steady-state and transient thermal behaviour. Ensure that the switching devices operate within a safe range under worst-case conditions by analysing steady-state thermal behaviour. Evaluate the impact of different baseplate materials on thermal behaviour, and compare the thermal resistance obtained from transient thermal behaviour analysis with experimental results to enable quick temperature estimation of the module.
9. Study the cooling performance of heat sinks using CFD technology, particularly focusing on the thermal behaviour of devices at different air speeds. Address the challenge of CFD's long computation time by proposing a new method for rapidly estimating device temperature and use this method to estimate the maximum achievable power of the power module.
10. Develop an integrated design for the three-level NPC SiC power converter, minimising parasitic inductance by optimising the busbar design. Implement a laminated busbar design by stacking copper layers with insulating materials to ensure even current distribution and solid physical support. Select appropriate DC capacitors and heat sinks to maintain optimal thermal performance and stability.
11. Construct a three-phase three-level converter using the optimised design, including assembling the power modules, DC capacitors, and cooling system.

Integrate gate driver boards, voltage sensor boards, and current sensors to precisely control and monitor the converter's performance.

12. Accurately extract parasitic inductance for more complex MLCs using S-parameter measurements and two-port network theory. Establish a small-signal model of the converter to facilitate the measurement and extraction of parasitic parameters and validate the extracted parasitic inductance values against simulation results.
13. Establish a testing platform for the converter and conduct DPTs to evaluate switching characteristics and overvoltage situations. Compare experimental results with simulation models to validate theoretical analysis and ensure converter performance under real-world conditions.

The aim of this thesis is to provide a useful resource in the field of power electronics, providing insight into the latest advances and practical challenges in MLCs technology. Through this comprehensive study, the thesis aims to contribute to the development of more efficient, reliable, and high-performance converter systems.

1.4.2 Main Contributions

All the objectives outlined in Section 1.4.1 have been achieved and are detailed in the thesis. The main contributions of this PhD thesis are summarised below:

1. Previous research has extensively compared two-level converters with various three-level converters, highlighting their respective advantages and disadvantages. These studies have also deeply analysed the topologies of different two-level and three-level converters, explaining their design principles and operating mechanisms. However, many of these studies were based on simulation models that only allowed for the modification of certain device parameters. In contrast, the present work establishes precise device parameter models, particularly focusing on the performance of devices under varying junction temperatures and different gate resistances. This allows for a more accurate description of the electrical performance of different converters. The work also develops PLECS models for different three-level converter topologies, including NPC, ANPC, and T-type converters. It thoroughly analyses the factors affecting the performance of three-level converters, such as voltage stress, switching losses, conduction losses, and

THD, under varying voltage, power, switching frequency, and the number of parallel power semiconductor devices. Additionally, many studies have focused on the application of IGBT or Si MOSFET in two-level converters, especially in areas like renewable energy generation, UPS, and EV drive systems. However, there has been relatively less research on the use of third-generation semiconductor SiC MOSFETs in three-level inverters, particularly in emerging high-voltage applications like aircraft starter-generator systems. This work evaluates the performance of SiC power semiconductor chips of the same voltage rating produced by different manufacturers, highlights the differences and selection criteria for various devices, and assesses the suitability of different converter topologies for aircraft starter-generator systems. Recommendations for topology selection based on aviation application requirements are provided.

2. Many of the three-level power modules currently available in the market are assembled by externally connecting two or even more two-level modules. While this approach allows for the direct use of existing modules, it introduces unnecessary parasitic inductance due to the additional connections. This thesis presents a power module based on a three-level NPC topology designed for 540V/1080V DC bus voltages. By analysing the power switch losses and thermal performance of the power module, suitable parallel configurations of MOSFETs were selected to ensure efficient operation under the worst-case conditions while keeping the maximum temperature within a safe range. The module adopts an optimised layout design that balances and reduces the parasitic inductance in the commutation loop while effectively eliminating the mutual inductance from the control loop to the commutation loop, thereby minimising the risk of damage to power semiconductor devices caused by high voltage overshoots during switching. Additionally, a novel baseplate material was chosen based on electrothermal modelling, making the module more suitable for aerospace applications.
3. For power converters, using CFD simulations can determine the performance of heat sinks. When the airflow speed is insufficient, the heat sink cannot provide effective cooling to power semiconductors, leading to excessive device temperatures and potential damage. However, considering the limitations of CFD, such as the significant computational load required for

solving multi-physics coupling problems involving complex geometries, achieving results often takes a long time due to the need for high-resolution meshes and intricate physical models. This thesis proposes using an equivalent heat transfer coefficient to replace the cooling system, allowing for a quick estimation of power device temperatures, reducing unnecessary time and computational costs. Based on this, a linear estimation is used to derive the possible maximum output power of the module under different airflow speeds, which is then employed to evaluate the scalability of the module.

4. The measurement of specific partial parasitic inductance values within a given power module has been a challenging issue, especially without damaging its external structure. Current literatures primarily focus on extracting partial parasitic inductance in discrete components or two-level modules. However, compared to two-level topologies, multi-level topologies are more complex due to the increased number of switching devices and the additional interconnections and wiring within the packaging, leading to more intricate equivalent circuit models. This thesis targets the three-level NPC topology converter, where a two-port network MLC small-signal model is established. Using a VNA, the S-parameters are measured and then converted to Z-parameters for detailed analysis. The parasitic inductance extraction method is validated, showing an error of less than 10% compared to the values obtained from 3D electromagnetic simulation. Subsequently, the extracted parasitic parameters are applied to the developed accurate DPT simulation model, and a three-level converter platform is constructed and tested to evaluate switching characteristics, overvoltage conditions, and overall electrical performance. The experimental results are compared with the simulation model, confirming the accuracy and applicability of the theoretical analysis.

1.4.3 Organization of Thesis

This thesis consists of five chapters and two appendixes, the content of each is summarised as follows:

Chapter 1 introduces an overview of power electronics system and non-ideal effects of power electronics, the literature review begins with an introduction to

power electronic systems, including the advantages of WBG devices, different types of converter topologies, and different package types of power electronic systems especially power modules. The non-ideal effects in power electronic systems are highlighted, including power losses, parasitic parameters, and the impact of the thermal effects on the system. Extensive analytical literatures are presented on how to accurately analyse and mitigate these non-ideal effects.

Chapter 2 introduces and evaluates the characteristics of several common converter topologies, and suitable application scenarios are presented according to the advantages and disadvantages of specific topology. Power semiconductor devices from different manufacturers have been modelled to simulate their electrical characteristics. The best performing device was chosen, and two-level, NPC, T-type, and ANPC converters were built using this device. Electrical performance analyses were carried out under different conditions and the simulation results were summarised and analysed, and it is proposed that the decision on which topology to use should be made according to the conditions of the specific application.

Chapter 3 presents a 540V/1080V power module for aerospace applications. The NPC topology was chosen for the design based on its operating environment; a more detailed electrical & electromagnetic analysis of the NPC topology was carried out. The parasitic inductance of the loop is optimised by optimising the layout of the SiC power module and the manufacturing process of the module is described. In addition, a steady state and transient thermal model based on the power module is simulated and analysed, a suitable heat sink with fan is identified using the CFD methodology and the maximum power that may be achieved by the module with better heat dissipation is estimated.

Chapter 4 describes the process of building an entire three phase SiC converter from the power module introduced in Chapter 3, which details the design process of the laminated DC busbar and its loop inductance. For the parasitic inductance, which is crucial in affecting the performance of the converter, a small-signal model is modelled for the three-phase converter constructed, and the parasitic inductance is further obtained by measuring the S-parameters by considering the small signal model as a network of 16 different two-port networks, which implies that the effects of

capacitance and resistance can be neglected at high frequency. Finally, the feasibility of this method was verified by building an experimental platform for DPT.

Chapter 5 concludes the doctoral work of the thesis as well as potential suggestions for future work are provided.

Appendix A describes the converter technology which is different from the power module-based converter technology which integrates the converter in PCB, it is low cost, light weight, small size and is an emerging converter solution in recent years. Two different PCB-based embedded converter designs are proposed based on their technical characteristics and thermal modelling is carried out for each of them, the results show that it is a very competitive solution even in the worst-case scenario when suitable thermal vias are used.

Appendix B is a continuation of the power losses of the three-level NPC converter at different junction temperatures in Chapter 3, Section 3.2.

1.5 List of Publications

1. Z. Li *et al.*, “Modular design of a three-level SiC MOSFET power module for more-electric aircraft applications,” in *11th International Conference on Power Electronics, Machines and Drives (PEMD 2022)*, 2022, pp. 58–63.

CHAPTER 2
Comparative Analysis of Three-Level Converter for an Aircraft Starter-Generator

2.1 Introduction

In the domain of power electronics, converters play a crucial role in a wide range of applications, including renewable energy integration, EV propulsion, industrial motor drives, and domestic energy systems. The primary function of an inverter is the conversion of DC to AC, and its operational efficiency and effectiveness critically influence the overall performance of the encompassing system. Due to the diverse application scenarios, a variety of converter topologies exist, each with its own characteristics, advantages, and potential drawbacks.

This chapter provides a comprehensive comparative analysis of three-level converters used in aircraft starter-generator systems, highlighting their significant advantages over traditional two-level converters, such as increased efficiency, reduced harmonic distortion, and improved power level. It begins by describing the most common converter topologies, clarifying their operating principles, unique features, and their respective advantages and disadvantages. The chapter then compares various switching devices from different semiconductor manufacturers, evaluating their parameters based on datasheets and building PLECS models. Subsequently, different three-level converter models, including NPC, ANPC, and T-type converters, are built and their electrical performances are numerically compared, analysed, and evaluated. Key factors such as voltage stress, switching losses, conduction losses, and THD are thoroughly investigated, providing a clear understanding of how three-level converters can enhance the overall efficiency and functionality of aircraft starter-generators.

Furthermore, by synthesising and comparison the results of different three-level converter topologies, this chapter aims to provide insights and guidelines for selecting the most suitable converter topology to enhance the performance, reliability and efficiency of aircraft starter generator systems. The analysis aims to offer valuable

insights for the development of more robust and efficient power conversion systems in modern aviation technology.

2.2 Advantages, Disadvantages, and Characteristics of MLCs

In conventional two-level VSCs, power devices are limited by the DC bus voltage, making them unsuitable for high-voltage applications. To meet higher voltage requirements, multiple power switches are connected in series, which can cause issues with dynamic voltage distribution. Additionally, high voltage stress and switching losses limit the use of two-level converters in medium- and high-voltage applications [141].

MLCs, introduced in the mid-1970s [142], address these issues by using more voltage levels, which reduce voltage stress on power devices and are suitable for higher voltage applications [143]. The increased number of levels leads to smoother switching, resulting in an output waveform closer to a sinusoidal shape. This reduces THD, improves power quality, and enhances system reliability and stability. Additionally, MLCs offer higher efficiency and lower device voltage stress [144]-[148]. Despite their advantages, MLCs are more complex, requiring additional power devices and passive components, as well as more intricate control strategies for proper operation. This complexity leads to higher costs, larger size, and challenges in maintenance and fault diagnosis.

After decades of technological development, MLCs have replaced conventional two-level converters in some medium and high-voltage applications. such as power traction & drives, renewable energy conversion, flexible alternating current transmission systems (FACTS), EVs, electric airplanes, high voltage DC (HVDC) transmission [149]-[153]. Apart from this, MLCs are also advantageous in some low-voltage applications that need to operate at high switching frequencies [154].

To compare with MLCs, the basic two-level VSC is introduced. This simplest form of VSC uses two output voltage states (+Vdc, -Vdc) and is commonly used in variable speed drives and renewable energy systems. Its simplicity, low cost, and robustness make it widely used in the industry. However, two-level VSCs can

produce high dv/dt and harmonic distortion in the output waveform. Fig.2-1 shows the typical topology of a two-level VSC.

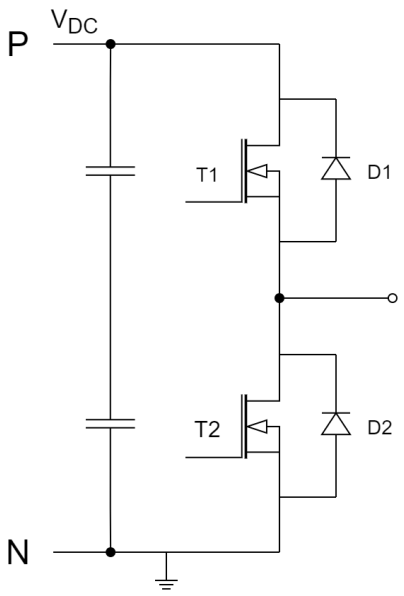


Fig.2-1 Typical two-level converter topology

The NPC converter is a widely used MLC topology, especially in industrial, automotive, and drive applications due to its high performance and simplicity. The basic three-level NPC structure, as shown in Fig.2-2, includes an additional output voltage state, zero voltage, compared to two-level VSCs. This addition helps in reducing harmonic distortion and voltage stress on the power devices, leading to better waveform quality. However, NPC converters are more complex, requiring careful DC link voltage balancing. It was the first MLC topology developed, with a phase leg comprising four power switches (T1-T4) connected via clamping diodes (D5 & D6) to the midpoint.

The three-level ANPC converter is an advancement over the three-level NPC converter. The topology is shown in Fig.2-3, it uses active switches instead of diodes to clamp the neutral point to control the current flow in the zero state, which provides better control over the output voltage and current. This leads to lower losses, better efficiency, and more flexibility in control strategies. However, the ANPC converter has increased complexity due to additional switches and the need for more sophisticated control methods.

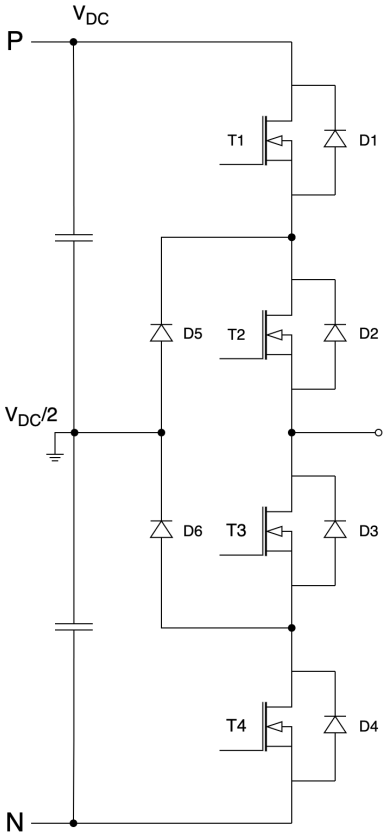


Fig.2-2 Typical three-level NPC converter topology

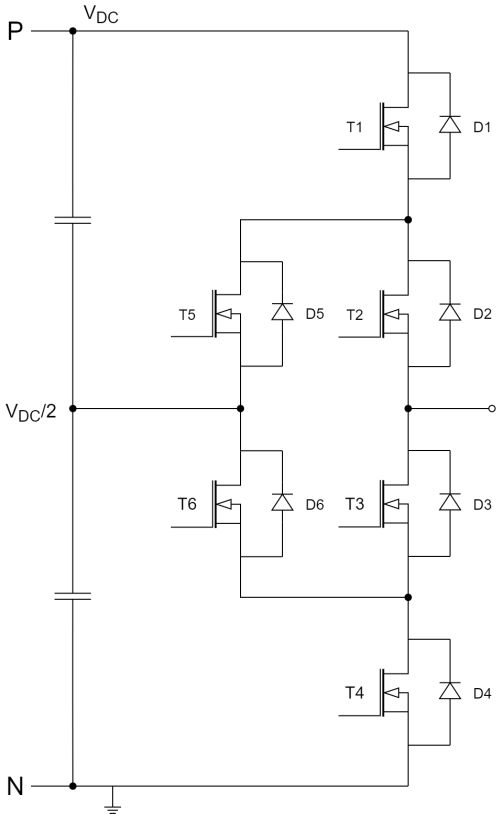


Fig.2-3 Typical three-level ANPC converter topology

The three-level T-type, or T-NPC converter, combines the benefits of two-level VSCs and three-level NPC converters. It uses two clamping devices at the voltage midpoint and two switches in the DC link, achieving three voltage levels: +Vdc, 0, -Vdc. This structure reduces the number of clamping diodes and gate drivers, offers high voltage output quality, and mitigates unbalanced loss distribution seen in NPC converters [155]. However, the devices must withstand the entire DC bus voltage, limiting its application in high-voltage scenarios [156]. Fig.2-4 shows its typical topology. The T-type topology can also be combined with other structures, like NPC and FC, to create hybrid converters [157]-[158].

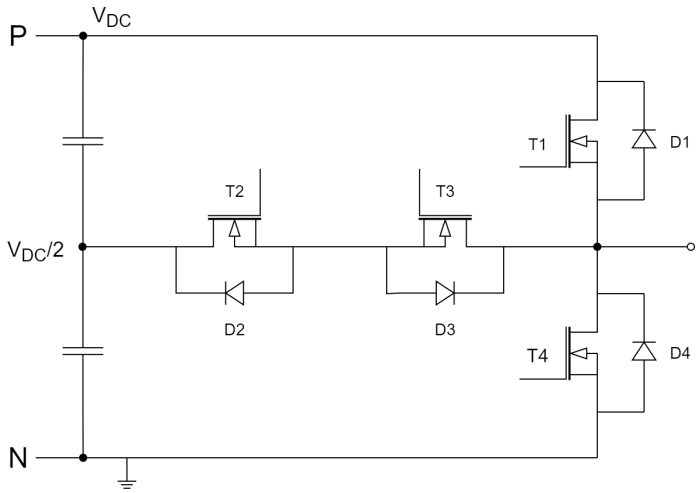


Fig.2-4 Typical three-level T-type converter topology

A FC converter uses capacitors and switches to convert DC input into AC output. This topology creates voltage levels using flying capacitors in each converter leg, with each capacitor typically holding a constant voltage equal to half the DC bus voltage. Introduced in the 1990s [159]-[160], the FC converter's main advantage is that it requires only one DC power supply and can reduce the harmonic content in the output waveform. However, it requires many large clamping capacitors and switches, increasing system cost and complexity. Additionally, maintaining voltage balance across capacitors is challenging and requires a complex pre-charge circuit. Despite these challenges, FC converters can produce high voltage levels due to their modular design [161], Fig.2-5 shows the typical FC converter topology.

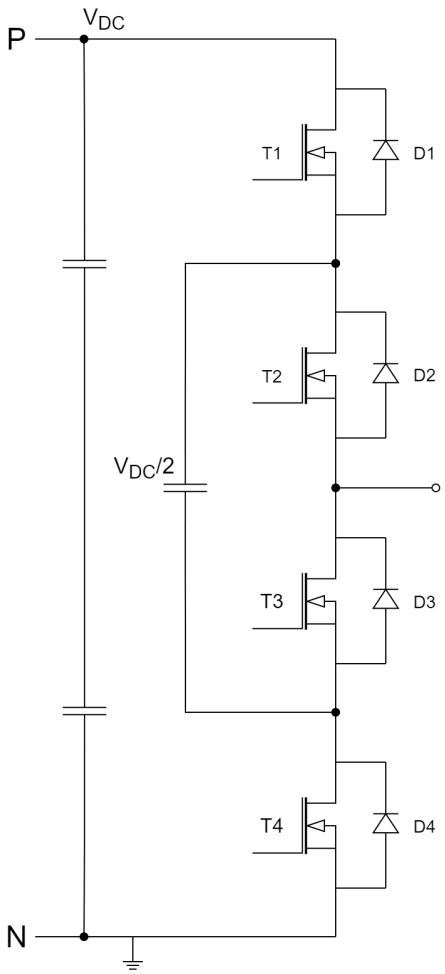


Fig.2-5 Typical three-level FC converter topology

The CHB converter is a MLC that uses multiple H-bridge cells in series to convert DC to AC power. Each H-bridge has its own DC source, allowing the output phase voltage to achieve several levels. This results in excellent output waveform quality with reduced harmonics, electromagnetic interference EMI, and lower voltage stress on switching devices. However, the need for separate DC sources for each unit increases complexity and can lead to imbalance issues, limiting the CHB converter's applicability. The five-level CHB topology, shown in Fig.2-6, uses two series-connected H-bridges to provide five output voltage levels: 0, $\pm V_{dc}/2$, and $\pm V_{dc}$. For a CHB converter with n cells, the output can reach 2n+1 levels between + V_{dc} and - V_{dc}.

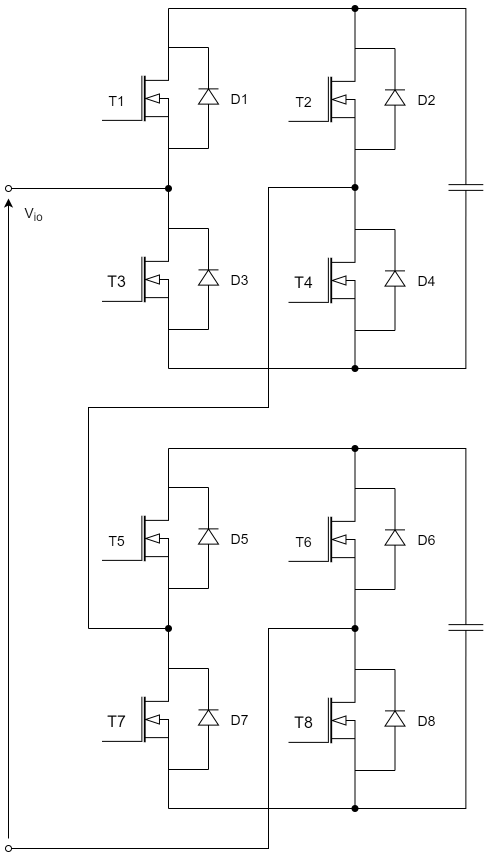


Fig.2-6 A two cell five level cascaded converter topology

Based on the characteristics of the various converters mentioned above, a stage-by-stage summary can be made, and Table 2-1 summarises the number of switching devices, the number of clamping diodes, the number of flying capacitors, the number of DC sources and the maximum withstand voltages of the devices required for these converters. To summarise, the advantages and disadvantages of each of these topologies are:

1. NPC converter: Advantages: No floating capacitors, good dynamic response, simple design, low cost and compact in three-level structure. Disadvantages: Increased cost and reduced reliability as number of levels increase due to dramatical increase in number of diodes, unequal loss in switches
2. ANPC converter: Advantages: No floating capacitors, good dynamic response, simple design, equal loss in switches, low cost and compact in three-level structure. Disadvantages: Increased number of floating capacitors as level increase, more complex control than NPC, different voltage rating of power switches at higher levels

3. T-type converter: Advantages: No floating capacitors, no diodes, simple control. Disadvantages: Higher voltage stress on switches, low efficiency at high frequency operation due to high switching losses, not suitable for high voltage, high power traction drives.
4. FC converter: Advantages: Cost efficient in higher level structures, modular structure. Disadvantages: High number of floating capacitors, complex control, high stored energy in capacitors, high voltage ripples at low frequencies, voluminous and heavy, requires plenty of voltage sensors, low reliability
5. CHB converter: Advantages: No floating capacitors, high reliability, modular, simple control. Disadvantages: Isolated DC sources are needed which is not provided in grid-connected traction applications, more power switches.

Table 2-1 Comparison of different converter characteristics

Topology	Number of power switches	Number of diodes	Number of flying capacitors	Number of DC-link capacitors	Maximum blocking voltage
2L VSC	2	0	0	2	V_{dc}
3L NPC	4	2	0	2	$V_{dc}/2$
3L ANPC	6	0	0	2	$V_{dc}/2$
3L T-type	4	0	0	2	V_{dc}
3L FC	4	0	2	2	$V_{dc}/2$
3L CHB	4	0	0	1	$V_{dc}/2$

The industry currently favours MLCs for medium to high power ratings in three-phase topologies, particularly those with a common DC bus, as they are practical for high-power applications like pumps, conveyors, fans, and traction systems. This preference arises because topologies with multiple isolated DC sources are impractical. MLCs with a common DC bus help develop three-phase configurations, reduce phase current, and increase power ratings, such as in EV superchargers for faster charging. However, the complexity of design, due to the need for more switches, auxiliary capacitors, gate drivers, and complex voltage balancing techniques, presents a significant barrier to widespread adoption. Additionally, the increase in active/passive components affects the size and cost of power converters and impacts reliability and lifespan, as capacitors can be points of failure. Thus, market players must find a balance between cost, voltage balance, size, reliability, and manufacturing to optimise performance and reliability.

2.3 Three-Level Converter Performance Analysis

Based on the detailed analysis of the advantages and disadvantages of several common converters and application scenarios in the previous section, the practical application scenarios involved in this thesis include high power converters on more electric aircraft and medium power converters that can be used for EVs as well as motor drives (approximately 100kW per phase). Of the many topologies that have been developed, NPC and T-type are the most competitive solutions [38]-[39], [42]. Therefore, three main converter types, NPC, ANPC, and T-type, are considered and compared with the two-level VSC.

2.3.1 Device Selection in Three-level Converters for Aircraft Starter-Generator

The selection of devices in three-level converters is critical for optimising the performance, efficiency, and reliability of aircraft starter-generators. This section explores the key considerations and criteria for selecting appropriate semiconductor switches to ensure optimal operation under the demanding conditions of aviation applications. There are currently SiC MOSFETs manufactured by several manufacturers in the commercial market. MOSFETs manufactured by different companies may have different designs and manufacturing processes resulting in different parameters such as threshold voltage, on-state resistance, maximum current, and voltage, etc., which can affect the performance of the converter. It is therefore crucial to analyse the performance and behaviour of SiC MOSFETs manufactured by different companies, which will help us to understand the advantages and limitations of these devices in converter applications.

The price and accessibility of SiC MOSFETs from different manufacturers may vary and by analysing their performance in converters, it can help to assess the cost effectiveness of the device. This section will analyse four possible candidates, they are CPM3-1200-0013A from Cree, NTC020N120SC1 from ON Semiconductor, G3R12MT12-CAL from Gene SiC and S4103 from Rohm, they are all bare die devices rather than discrete devices. Evaluating the performance of different manufacturers' SiC MOSFETs in converters can help to select the most suitable device for a particular application.

To achieve this evaluation effectively, advanced simulation tools are essential. PLECS, a simulation software for the design and analysis of power electronic systems and control strategies, offers the capabilities needed for such detailed analysis. It has efficient solvers and specialized power electronics component models to enable rapid simulation of large and complex power electronics systems. PLECS allows simulations to be performed in several physical areas such as electrical, thermal, and mechanical, which is useful for considering heat dissipation, mechanical stresses, and other non-electrical effects in system design. It can help to design and optimise converters to improve the performance and efficiency.

Unlike using ideal power device models, in order to analyse the performance of converters using different devices, it is necessary to characterize them separately and accurately, and for these non-ideal models, their physical parameters need to be included, which can usually be obtained from data sheets. The use of non-ideal switching models can provide more accurate simulation results, especially when system efficiency and power losses are of concern. However, using a non-ideal switching model will usually slow down the simulation, so there is a trade-off between simulation accuracy and speed.

By importing data sheet graph information, the turn-on/turn-off energy characteristics of the device can be obtained by linearly fitting the plot of switching loss versus device currents (I_{ds}) at different voltage levels and temperatures in PLECS. Fig.2-7 shows the import process of switching losses, the data in the left-side figures are extracted from the datasheet and provide detailed curves showing the relationship between switching energy (turn-on/-off energy) and drain-source current under different gate resistances. The right-side figures offer a three-dimensional visualization to better understand the switching energy characteristics under various conditions, and it can be extended to different gate resistance situations through linear fitting. By analysing this figure, it is possible to better understand the energy loss under different gate resistance and drain-source current conditions, predict switching losses under various operating conditions, and thus improve overall circuit efficiency.

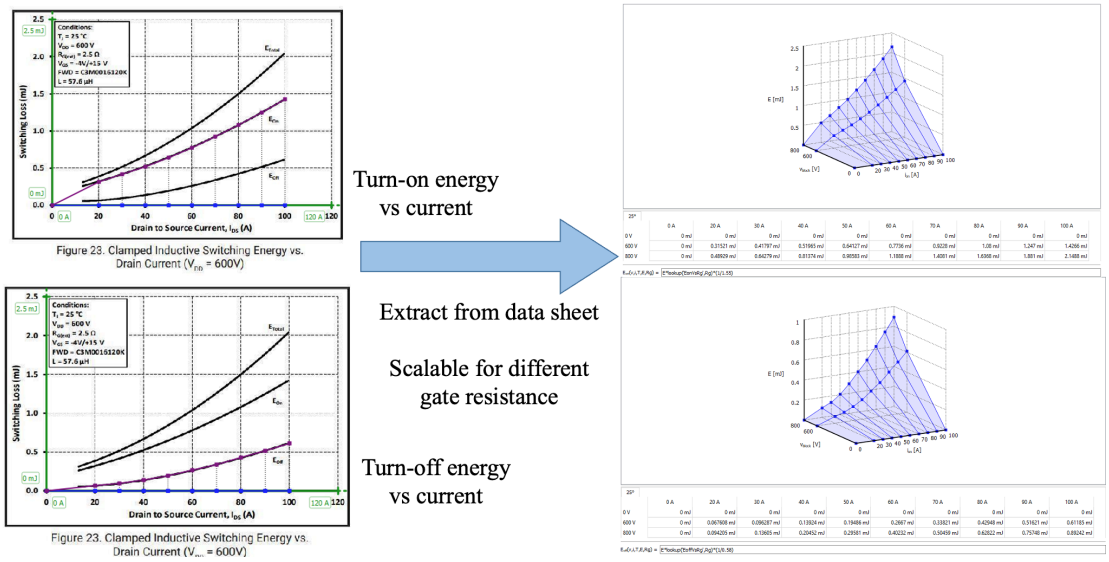


Fig.2-7 Procedure of importing switching losses

Similarly, the conduction losses of the device can be obtained by linearly fitting the first and third quadrant output characteristics of the device at different gate-source voltage (V_{gs}) and temperatures in PLECS, Fig.2-8 shows the import process of conduction losses, the left-side figure provides curves showing the relationship between drain-source voltage and drain-source current under different gate voltages and temperatures. The right-side chart offers a three-dimensional visualization, more intuitively demonstrating the impact of temperature on the relationship between drain-source voltage and current. As the temperature increases, the drain-source voltage increases for the same drain-source current, affecting the device's switching characteristics and efficiency.

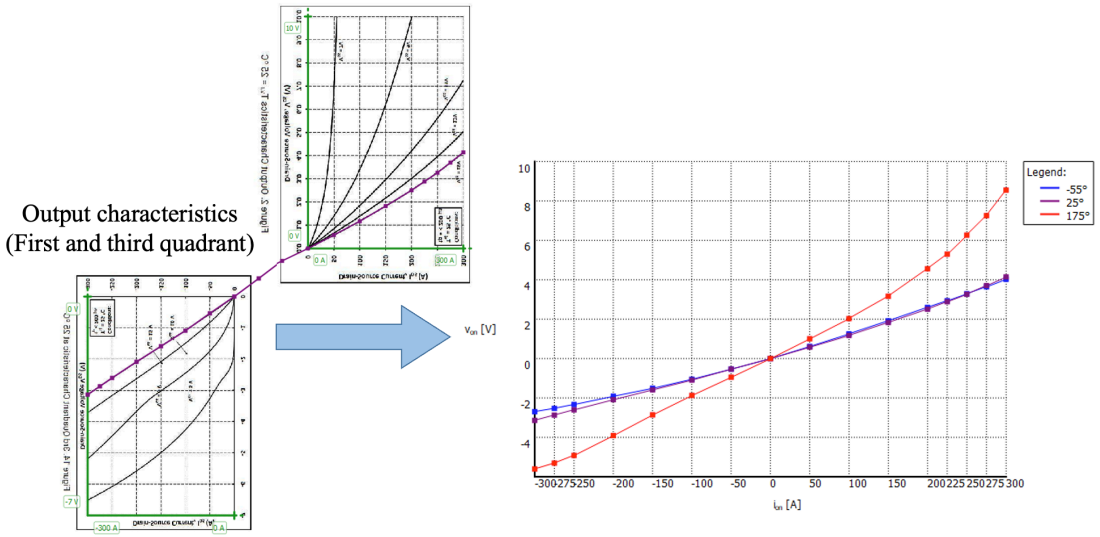


Fig.2-8 Procedure of importing conduction losses

Using PLECS can also describe the device's physical structure in terms of thermal impedance from the junction to case by fitting the single pulse thermal transient. Fig.2-9 shows the import process of thermal model, the figure on the left shows the transient thermal impedance curve of a semiconductor device demonstrating the pattern of change of thermal resistance with time, and the figure on the right shows a model of the corresponding thermal resistance network describing the thermal transition process from junction to case. By analysing and applying this thermal impedance data, the thermal behaviour of the device can be better understood and managed to improve overall system performance and reliability.

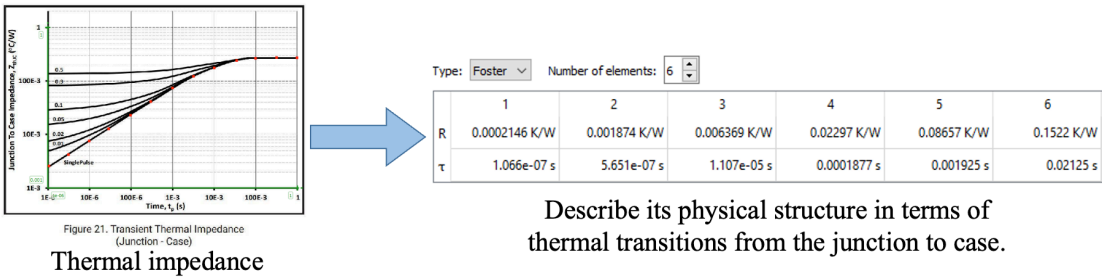


Fig.2-9 Procedure of importing conduction losses

Although the switch energy and output characteristics provided in the datasheets by different device manufacturers are obtained under different test conditions (such as different junction temperature and Vgs), by performing linear fitting on the switch device models established in PLECS, it is possible to compare the performance of different devices under the same test conditions within the same converter model.

To compare the performance of different devices, they were all tested under the same condition, the converter selected here should be capable of supplying 100kW of power to the DC distribution grid at a stabilised voltage of 540VDC which is suitable for an aircraft starter-generator. The AC-DC converter needs to transmit power in both directions to enable the motor to provide initial start-up. Here it is assumed that the motor may be represented by an alternating voltage source varying between 0V/0Hz to 200V_{RMS} at 1700Hz at full speed. And in start mode it is assumed that the motor starts from standstill to half speed operation at which the generator is producing a voltage of 100V_{RMS} at 850Hz.

By simulating the aircraft starter-generator power electronics system, the interactions within the complete system can be understood. This helps identify

potential issues arising from integration, such as harmonics, losses, and control. Simulation can provide a detailed analysis of the motor's performance under different operating conditions, including evaluating motor efficiency, torque, speed control, and dynamic response. Additionally, it offers a platform for testing and validating control strategies, facilitating the accurate calculation of power device losses within the converter.

Fig.2-10 shows in detail the components of the aircraft starter-generator power electronics system and their functions, including current control, two-level converter, loss calculation, motor mode selection, and monitoring of key system parameters such as I_{dq}, V_{dq}, torque, and speed. The converter output current can be calculated as (2.1):

$$P = 3V_{rms}I_{rms}cos\varphi$$

$$I = \frac{P}{3Vcos\varphi} = \frac{100000}{3 \times 200 \times 1} = 166.7Arms \tag{2.1}$$

$$I_{pk} = 166\sqrt{2} = 236A$$

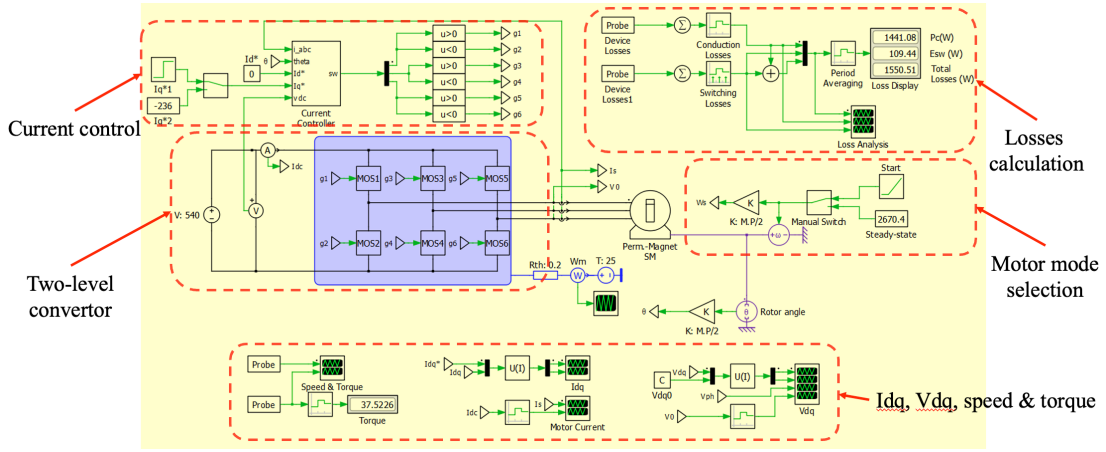


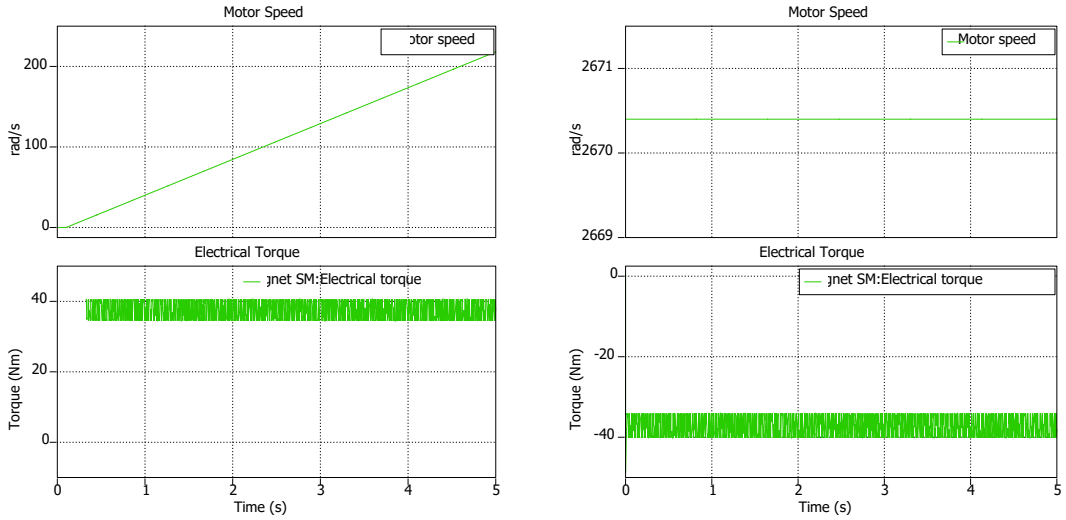
Fig.2-10 Aircraft starter-generator model in PLECS

Fig.2-11 shows the motor speed and electric torque of the PM machine in the starting mode and in the generating mode. In starting mode, the motor provides positive torque, overcoming inertia and load to accelerate the system's rotation. In generating mode, the motor provides negative torque, absorbing mechanical energy and converting it into electrical output. The torque can be calculated using (2.2):

$$\varphi_m = \frac{V_{peak}}{\omega} = \frac{100\sqrt{2}}{2\pi \times 850}(starting) = \frac{200\sqrt{2}}{2\pi \times 1700}(starting)$$

$$= 0.0265Vs \tag{2.2}$$

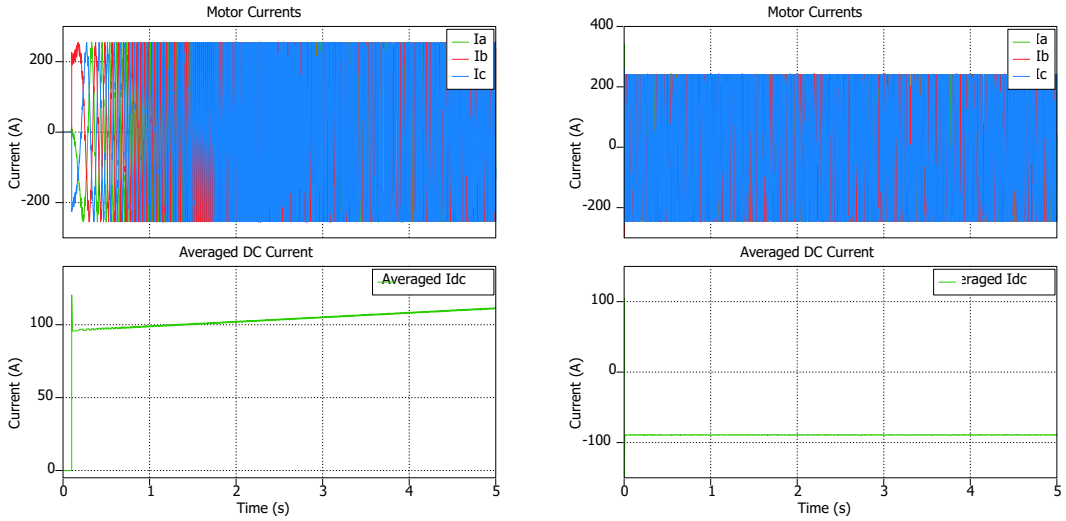
$$T = \frac{3}{2}\frac{P}{2}\varphi_m I_q = \frac{3}{2} \times 4 \times 0.0265 \times 236 = 37.5Nm$$



(a) (b)

Fig.2-11 Motor speed and electrical torque for (a) starting mode (b) generating mode

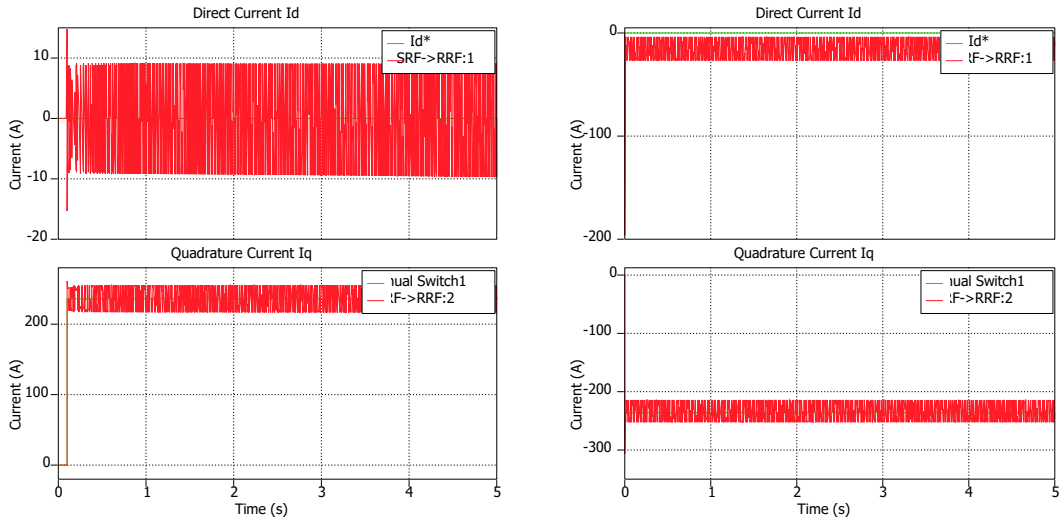
Fig.2-12 shows the variation of phase currents and DC currents of the motor in the starting mode and in the generating mode.



(a) (b)

Fig.2-12 Motor phase current and DC current for (a) starting mode (b) generating mode

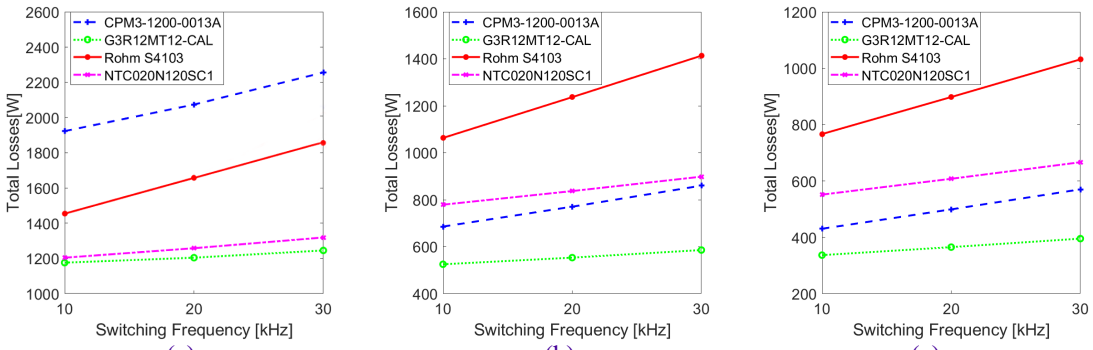
Fig.2-13 shows the variation of direct current I_d and quadrature current I_q of the motor in starting mode and generating mode. In starting mode, the motor needs to provide torque for acceleration, so the quadrature current I_q is large, while the direct current I_d remains at a low level to reduce current losses. In generating mode, the motor converts mechanical energy into electrical energy, and the quadrature current I_q is negative, indicating that the motor is absorbing mechanical energy and generating electricity. The direct current I_d remains at a low level, indicating the stability of the current during the generation process.



(a) (b)

Fig.2-13 Direct current Id and quadrature current Iq for (a) starting mode (b) generating mode (green: reference value, red: actual value)

Fig.2-14 shows a comparison of the total losses of different MOSFET devices in starting mode for different switching frequencies and different numbers of paralleled MOSFET dies. Similarly, Fig.2-15 shows a comparison of losses in the generation mode.



(a) (b) (c)

Fig.2-14 Starting mode loss comparison of different devices at different switching frequencies (a) 2 MOSFETs in parallel (b) 3 MOSFETs in parallel (c) 4 MOSFETs in parallel

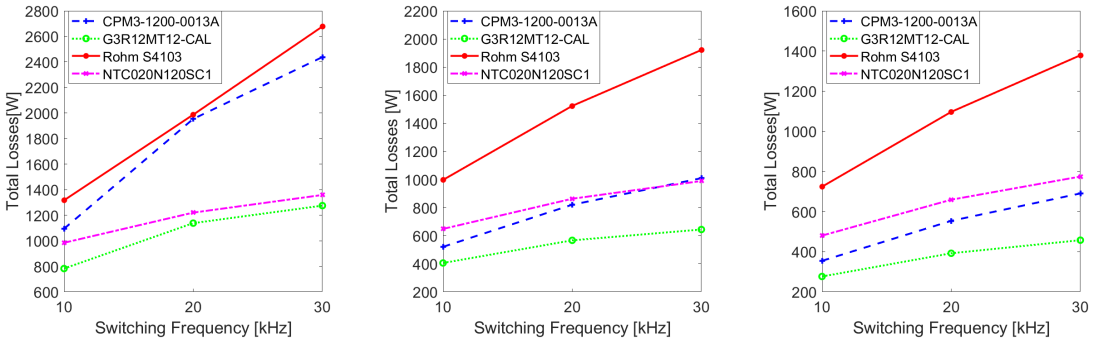


Fig.2-15 Generating mode loss comparison of different devices at different switching frequencies (a) 2 MOSFETs in parallel (b) 3 MOSFETs in parallel (c) 4 MOSFETs in parallel

By comparing and summarising the performance of different devices under different test conditions, several conclusions can be obtained:

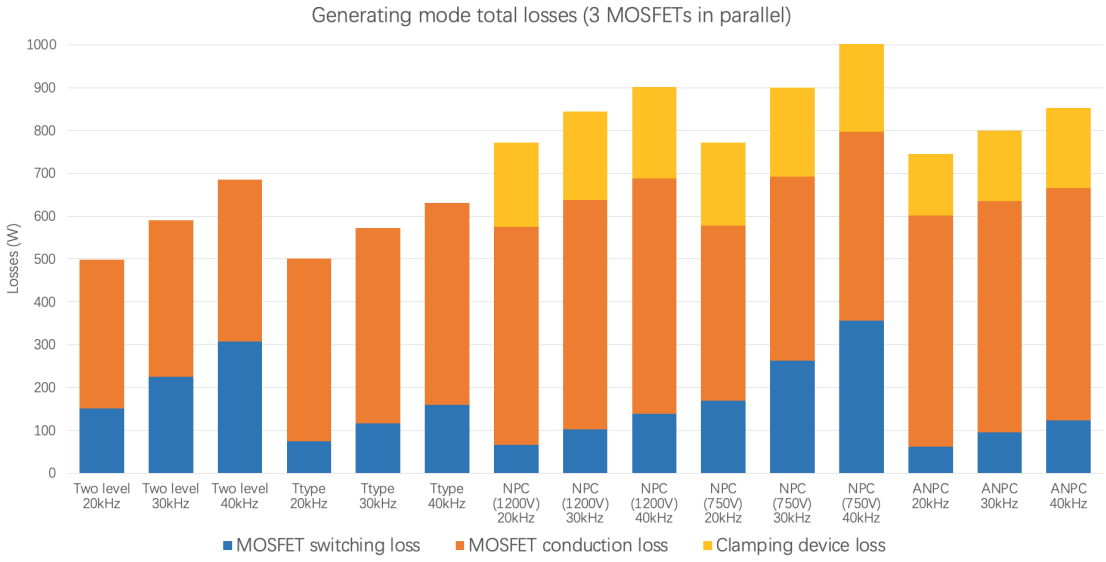
1. The more MOSFETs in parallel, the lower the total losses. This is because parallel MOSFETs can share the current, reducing the power loss in each MOSFET. In all the cases, as the number of parallel MOSFETs increases from 2 to 4 or even more, the total losses decrease, especially at high switching frequencies.
2. Increasing the switching frequency leads to higher total losses, primarily due to the rise in switching losses at higher frequencies, and this trend is observed in both starting mode and generating mode as the switching frequency increases from 10kHz to 30kHz.
3. From datasheets, G3R12MT12-CAL from GeneSiC has the smallest on-state resistance of 10mΩ, followed by CPM3-1200-0013A from Cree which has an on-state resistance of 13mΩ. The other two devices have an on-state resistance of 20mΩ and above.
4. The G3R12MT12-CAL shows a very competitive performance in all operation modes and at all frequencies.
5. When paralleling three or more MOSFETs in one switch, the CPM3-1200-0013A's performance is much improved and better than the NTC020N120SC1.
6. The S4103 has the highest losses in most cases, may not be suitable for efficient applications.
7. Converter design allow scalability for different applications and power levels using the same method.

2.3.2 Performance Comparison of Converters with Different Topologies

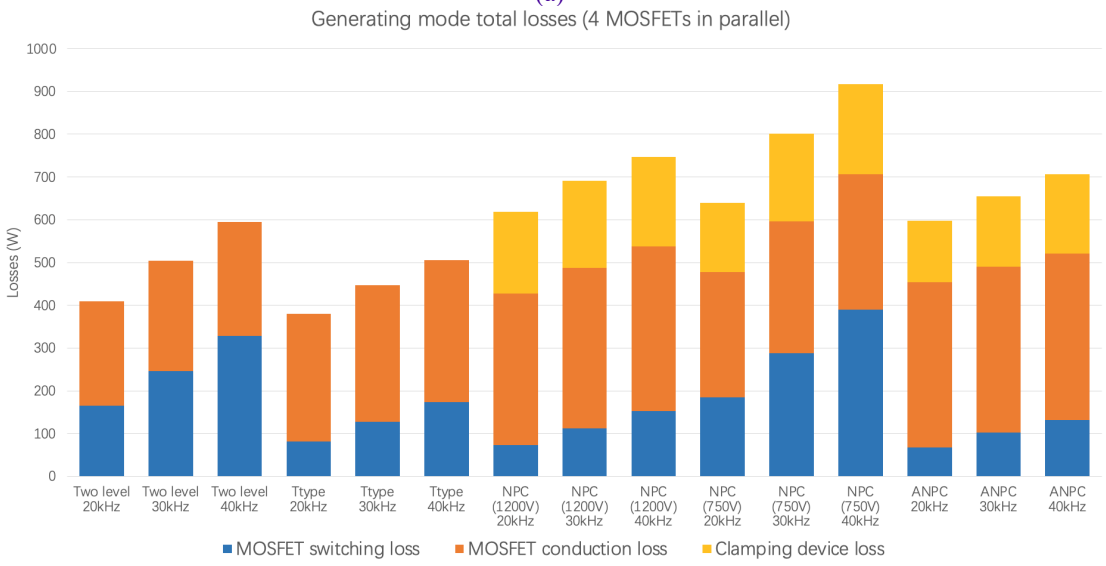
This section will compare several common converters of different topologies using device G3R12MT12-CAL. The converter loss simulations were all performed based on PLECS software, and the THD was also measured. With the increase in aviation electrical equipment, 540V and even 1080V DC bus is becoming an acceptable option, it is also expected that the output power is expected to further increase to hundreds of kWs. Therefore, simulations were carried out in two cases, the first one with DC-bus voltage is 540V, I_{rms} is167A. The second is with DC-bus voltage is 1080V and I_{rms} is 282A. Each represents two possible applications: the first case models an application where the converter should be able to deliver 100kW to the DC network at a stabilized voltage of 540V DC and the second case represents a converter capable of delivering 300kW to the DC network at a stabilized voltage of 1080V DC. For the first 540V case, in addition to using a 1200V device G3R12MT12-CAL, also consider a lower voltage class 750V device G3R10MT07-CAL for comparison. For the second high voltage 1080V case, in addition to using 1200V devices, higher voltage class 1700V device G3R20MT17-CAL is also considered for comparison. Products from the same company have been chosen here to minimise possible effects due to differences in production processes.

Fig.2-16 shows a comparison of the losses generated by different types of converters when the DC voltage is 540V and I_{rms} is 167A, Fig.2-17 shows a comparison of the losses when the DC voltage is 1080V and I_{rms} is 282A. For the same topology, increasing the switching frequency results in higher total losses due to the increased switching loss of the MOSFETs. Three-level converters reduce switching losses by introducing a midpoint potential that halves the voltage stress on the switching devices. As a result, three-level converters generally outperform two-level converters in terms of losses in power switching devices, particularly in high-power applications where they effectively reduce total losses. However, for NPC and ANPC converters, the additional clamping devices contribute to increased overall losses. In all scenarios, connecting more MOSFETs in parallel reduces both switching and conduction losses, while the losses of the clamping devices remain unchanged due to the consistent number of these devices. Nevertheless, it is necessary to consider

reasonable space utilization and cost issues when choosing the appropriate number of parallel devices.



(a)



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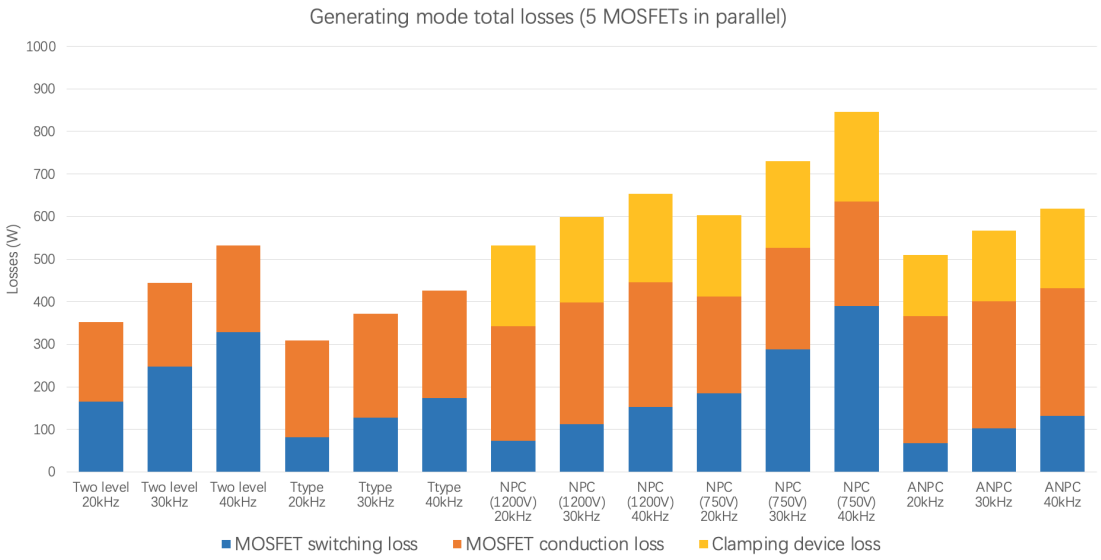
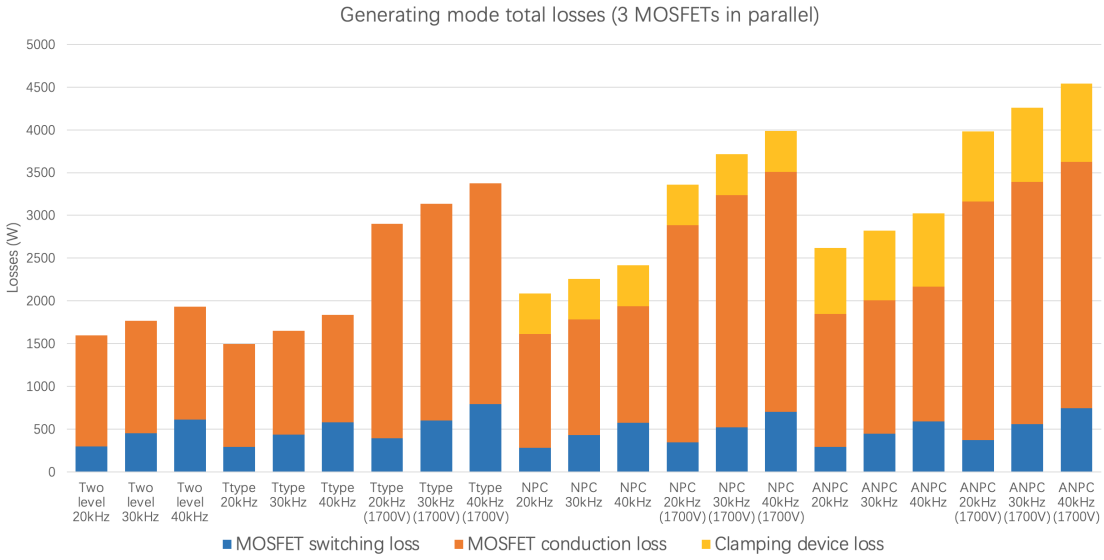
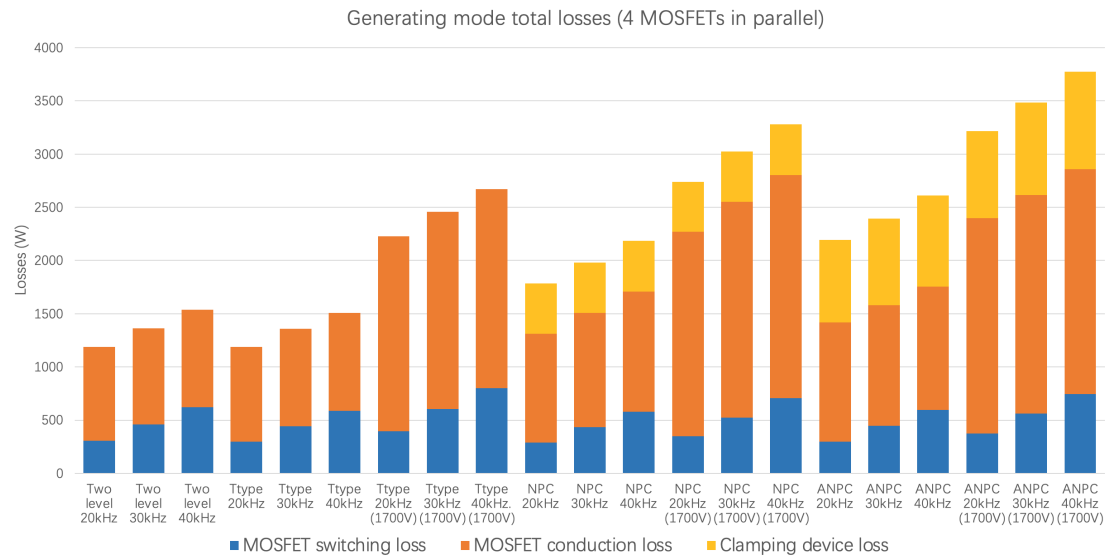


(c)

Fig.2-16 Detailed loss comparison of converters with different topologies at different switching frequencies (540V V_{DC} 167A I_{RMS}) (a) 3 MOSFETs in parallel (b) 4 MOSFETs in parallel (c) 5 MOSFETs in parallel



(a)



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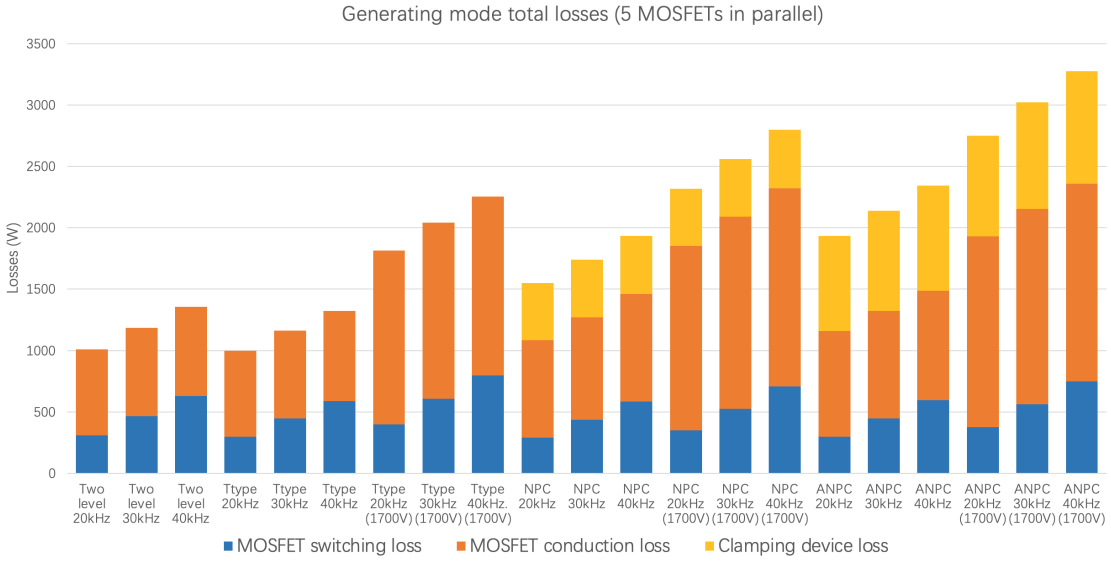
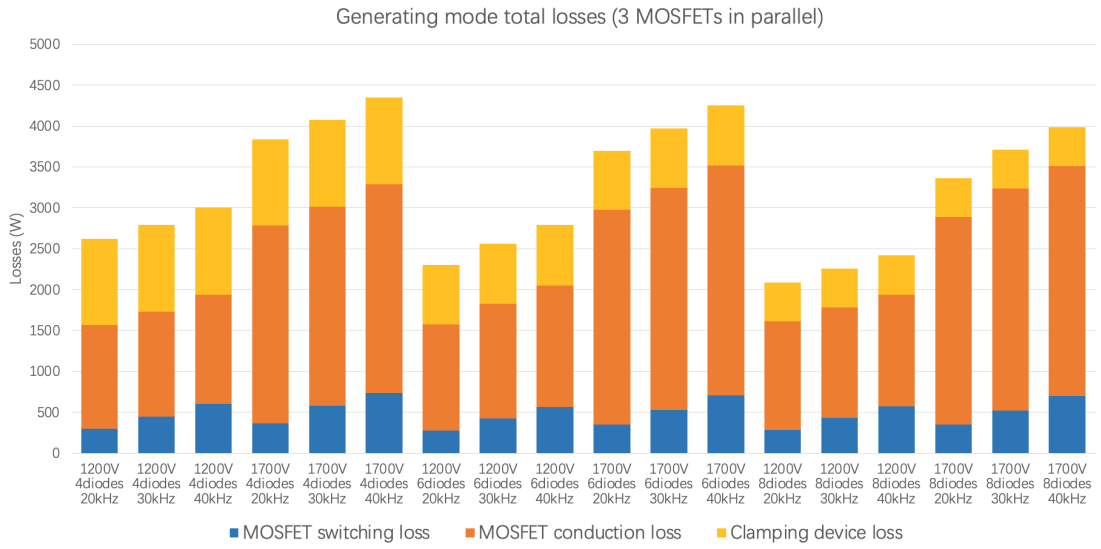


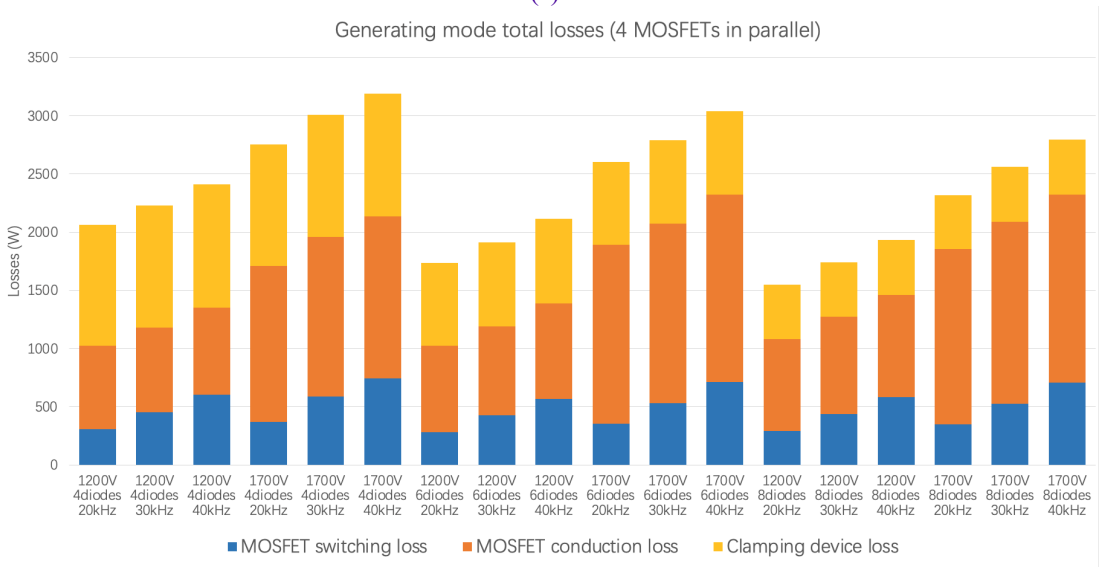
(c)

Fig.2-17 Detailed loss comparison of converters with different topologies at different switching frequencies (1080V V_{DC} 282A I_{RMS}) (a) 3 MOSFETs in parallel (b) 4 MOSFETs in parallel (c) 5 MOSFETs in parallel

Fig.2-18 compares the effect on NPC converter losses when different numbers of diodes are connected in parallel. Increasing the switching frequency usually leads to an increase in total losses, this is evident in all combinations of voltage class devices (1200V and 1700V) and diode numbers. Although 1700V devices can withstand higher voltage stresses, due to their own relatively high $R_{ds(on)}$, topologies using 1700V devices generally exhibit higher total losses than those using 1200V devices, and it is important to select the appropriate voltage rating device for the specific application. Due to current sharing, the loss of clamping devices decreases as the number of clamping diodes in parallel increases, and similar to the previous conclusion, a trade-off between losses and number of devices is required.



(a)



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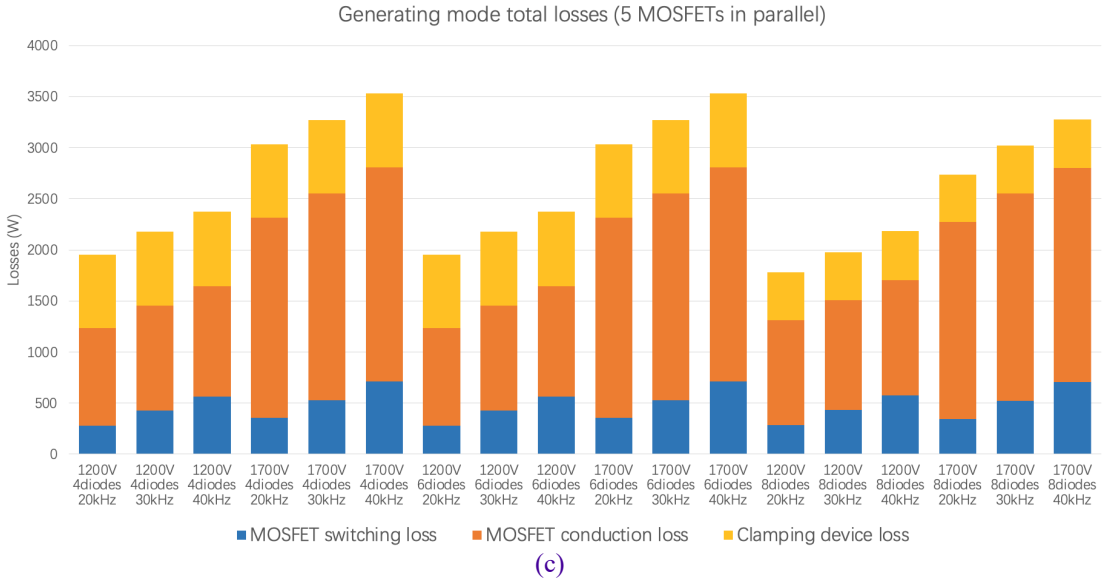
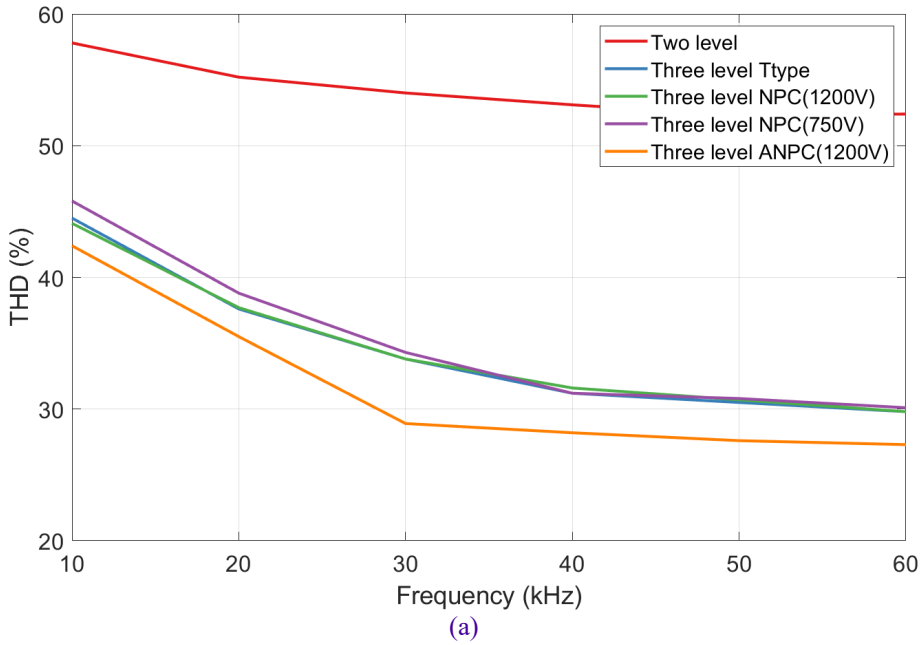


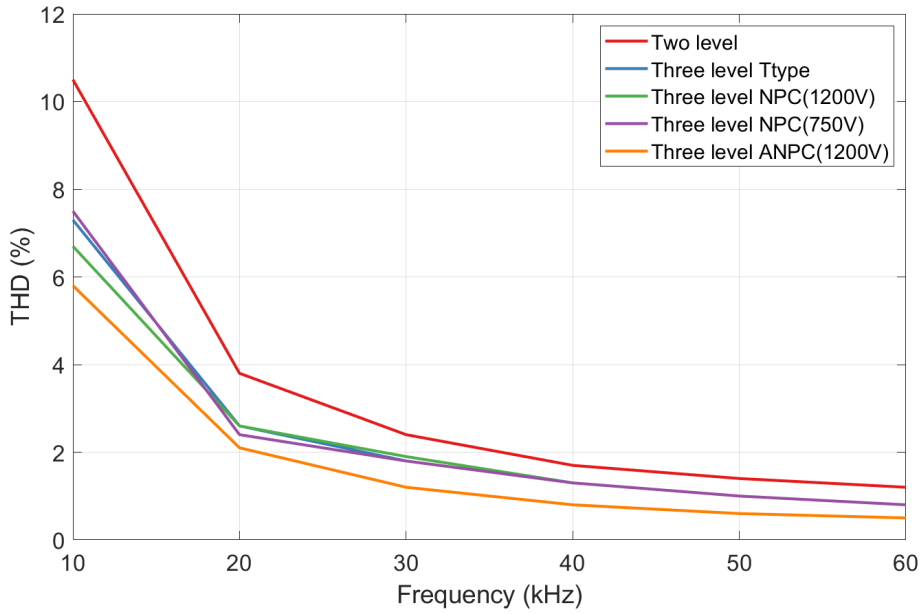
(c)

Fig.2-18 The effect of connecting different number of clamping diodes in parallel on the converter losses. (a) 3 MOSFETs in parallel (b) 4 MOSFETs in parallel (c) 5 MOSFETs in parallel

Fig.2-19(a) shows the variation of voltage THD with increasing switching frequency for different converters and Fig.2-19(b) shows the variation of current THD. As the switching frequency increases, the THD of all topologies shows a decreasing trend, indicating that higher switching frequencies help reduce harmonic distortion and improve output signal quality. The two-level topology maintains a relatively high THD, which decreases slowly as the frequency increases, remaining higher than other topologies across the entire frequency range. The three-level topologies, including Ttype and NPC, exhibit a significant decrease in THD with increasing frequency, converging at frequencies above 40 kHz. The three-level ANPC topology achieves the lowest THD, with the most substantial reduction as the frequency rises. Unlike the NPC topology which has only one zero-state, the ANPC topology has four different zero-states. The switching frequency of each power switch in this PWM modulation strategy is Fs, resulting in a doubling of the frequency of the output voltage to 2 Fs. Consequently, ANPC achieves the lowest THD across all frequency ranges among the topologies. Better harmonic distortion with the same switching frequency also allows further benefits such as the reduction in size and cost of passive filtering components.



(a)



(b)

Fig.2-19 Comparison of (a)THDv (b)THDi of different converters at different switching frequencies

In general, the three-level NPC converter includes more semiconductor devices, resulting in higher conduction losses compared to a two-level VSC. The additional clamping diodes further increase diode conduction losses. However, the voltage stress on each switch is reduced to half of the DC-link voltage, which can lower switching losses, especially in high voltage applications. The three-level T-Type converter, similar to the two-level VSC, has comparable conduction losses due to its use of multiple semiconductor devices. However, it is limited in high voltage applications as the device must withstand the full DC bus voltage. The ANPC converter can further improve THD without increasing the switching frequency. These three-level converters all exhibit better voltage and current THD, achieving the same performance as two-level converters but at lower switching frequencies.

Other research also highlights multifaceted benefits of three-level converters [32]-[34]. Efficiency comparisons of VSC, NPC and T-type converters were carried out over a wide range of switching frequencies. The results show that the efficiency of the VSC is higher only at low frequencies but decreases significantly above 10 kHz. On the other hand, the T-type is more efficient at moderate frequencies from 10 kHz to 30 kHz, while the NPC is slightly more efficient above 30 kHz. Three-level converters provide output voltages with lower harmonic distortion than VSC, which reduces the requirement for EMI filters and improves the efficiency of the motor. In addition,

both topologies suffer from high cost and increased control complexity due to the high number of parts.

2.4 Conclusions

This chapter investigates into the performance characteristics of various three-level converters in high-power applications, particularly focusing on their applications in aircraft starter-generator systems. It highlights the advantages of three-level converters over conventional two-level converters, such as improved efficiency, reduced harmonic distortion, and better suitability for high- voltage applications. Nevertheless, MLCs are inherently more complex, necessitating additional components and advanced control strategies, which raise costs and complexity.

It assesses the performance of different switching devices from multiple manufacturers, with a particular focus on SiC MOSFETs, using detailed simulations in PLECS models. PLECS is also used to simulate the converters, providing insights into device selection based on efficiency and loss characteristics. The chapter compares the losses and THD of different converter topologies across various switching frequencies and power levels. The analysis reveals that three-level converters outperform two-level converters in minimising losses and THD, particularly in high-power applications, concluding that they significantly enhance efficiency and power quality.

The chapter concludes the choice of semiconductor devices and converter topology is crucial for optimising performance and reliability. When selecting switching devices from different manufacturers or with different voltage ratings, it is important to evaluate them based on the specific application. Performing preliminary simulations to quickly identify the optimal devices can help avoid unnecessary time and cost losses. Different topologies of converters are suitable for different application scenarios, and it is necessary to make a compromise in choosing the appropriate topology for a specific need.

CHAPTER 3
Three Level NPC SiC Power Module Design and Considerations

3.1 Introduction

SiC power modules are preferred in power electronics for their high-temperature operation, power density, thermal conductivity, and low on-state resistance, making them ideal for high-frequency, high-power applications like EVs, aerospace and renewable energy systems. However, their integration requires a thorough understanding of electrical and thermal behaviour. Analysing the electrical and electromagnetic properties of SiC power modules helps improve operation, stability, efficiency, and optimisation. This includes studying conduction and switching characteristics, parasitic elements, loss mechanisms, and thermal effects. Effective thermal analysis is crucial as it impacts performance and longevity by managing heat generation and dissipation [162]-[164].

Driven by the urgent need to reduce carbon emissions and improve energy efficiency, the global aviation industry is transitioning to electrification. Advanced electrical systems are replacing traditional mechanical, pneumatic, and hydraulic systems to meet higher power demands and operational efficiency. Innovative electrical designs and enhanced thermal management of power modules are crucial to meet these needs. This chapter builds on the power loss analysis of various topologies discussed in Chapter 2, with a particular focus on the electrical simulation of the NPC converter. The primary focus in MATLAB/Simulink simulations is to determine the required number of MOSFETs and diodes, establish their characteristic models, and analyse power losses under various operating conditions. By examining different operating conditions and configurations, the goal is to identify the optimal setup to minimise power losses and enhance the overall efficiency of the power module.

Secondly, due to the additional current commutation loops introduced by multi-level structures, the importance of studying the inductance of NPC topology loops is highlighted. This is crucial for the subsequent selection of power module layouts. The parasitic inductance is modelled within the power module loops and its impact on

voltage overshoot and oscillations is discussed. Next, the criteria for selecting suitable power devices in the power module are discussed. These criteria ensure the module maintains high efficiency and stability under different operating conditions. Through optimised layout, component placement, and the use of advanced materials and technologies, the chapter presents design solutions for effectively reducing module inductance and describes the assembly process of the power module.

Finally, the thermal design of the three-level NPC module is discussed. Effective thermal management is crucial for the reliability and efficiency of power modules. This section provides a detailed thermal analysis of the power module, considering both steady-state and transient conditions. It evaluates different materials and designs to optimise heat dissipation and ensure the module operates within a safe temperature range. Additionally, the heat dissipating system is discussed, introducing a novel method for quickly estimating device temperature and maximum achievable power based on the thermal conductivity coefficient.

3.2 Evaluation and Impact of Power Losses in Power Modules

With an increasing global commitment to carbon neutrality by mid-21st century, the aviation industry sees electrification as crucial for enhancing efficiency and reducing its environmental footprint. The transition towards MEA has been marked by significant advancements in electrical systems replacing older mechanical, pneumatic, and hydraulic technologies. Traditionally, aircraft have utilized 270V DC power supplies, with power electronics converters generally handling tens of kWs. However, these are now deemed insufficient as the increasing demand for on-board electric power, and future aircraft will likely need power supplies of ±540/1080V DC to handle power levels scaling up to several MWs [165]. This shift requires innovative electrical designs and enhanced thermal management of power modules to meet the increased power demands and ensure reliability in the face of aviation's significant role in CO_2 emissions, estimated at 12% of the transport sector's total.

To accommodate the development needs of MEA, it is necessary to design and manufacture a power module that can operate at 540V/1080V DC bus voltage, with each phase capable of delivering 100 kW of output power. According to the power

loss analysis of different type of topologies in Chapter 2, although T-type topology have good competitiveness in terms of power loss, one of the advantages of the NPC topology is the introduction of intermediate voltage levels, which reduces the voltage stress on the individual power switches and improves the system reliability. When the module is required to operate at a DC bus voltage of 1080V, the T-type converters may subject the device to excessive voltage stresses affecting the electrical performance. The ANPC topology has better THD performance at the same switching frequency, but the use of switching devices instead of diodes as clamping devices increases the cost, size, and weight of the power module.

For aerospace applications, a high-efficiency, high-power density three-level power converter has been developed and demonstrated. Detailed electrical simulations have been performed in MATLAB/Simulink to evaluate the converter's performance and support the module's design, e.g., identify the number of dies for the MOSFETs and diodes to parallel. Each MOSFET and diode is modelled using an accurate electrical model based on three-dimensional look-up tables representing the output characteristic drain-source current I_{DS} (V_{DS}, V_{GS}, T) as a function of drain-source V_{DS} and gate-source V_{GS} voltages and temperature T, see Fig.3-1. The electrical specifications of the proposed NPC module are as follows:

- The DC voltage bus (V_{DC}) = 1080 V (±540 V with reference to midpoint)
- Power factor (cosφ) = 0-1
- Gate to source voltage (V_{GS}) = 0-15 V
- Load frequency (f_{Load}) = 2 kHz
- Switching frequency(f_{sw}) = >16 kHz
- Load current ($I_{Loadrms}$)=250A (steady state), 400A (peak of AC current)

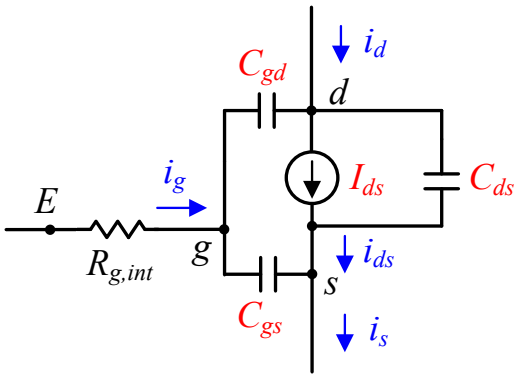


Fig.3-1 Circuit model of MOSFETs

The discussion of the power losses of different types of converters under different conditions is presented in Chapter 2. In this Chapter, electrical simulations are presented to evaluate converter losses and efficiency. The simulations are based on specific devices datasheets characteristics, using look up tables for the three phase three level NPC topology. To achieve the required load current, devices must be connected in parallel, this arrangement facilitates the analysis of power losses trends as the number of paralleled MOSFETs changes from 3 to 8 per switch. Different operating conditions are also considered to evaluate different loading operation e.g. with power factor 0 or 1, as well as different operating temperatures.

From the Simulink results, the output phase-phase (line-to-line) voltage V_{ab}, phase-neutral voltage V_{az} and output voltage V_{ao} are shown in Fig.3-2 as follows:

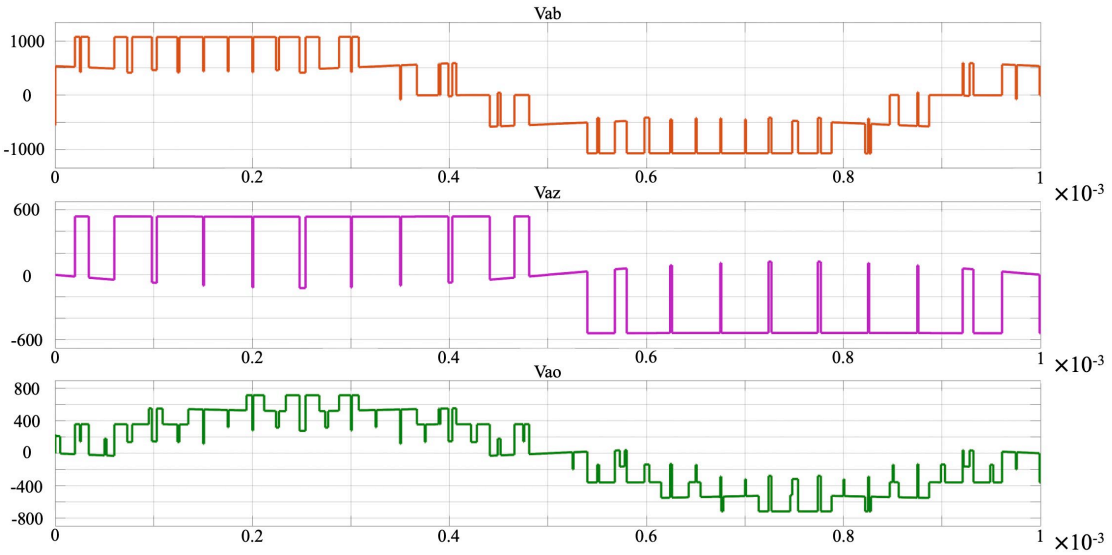
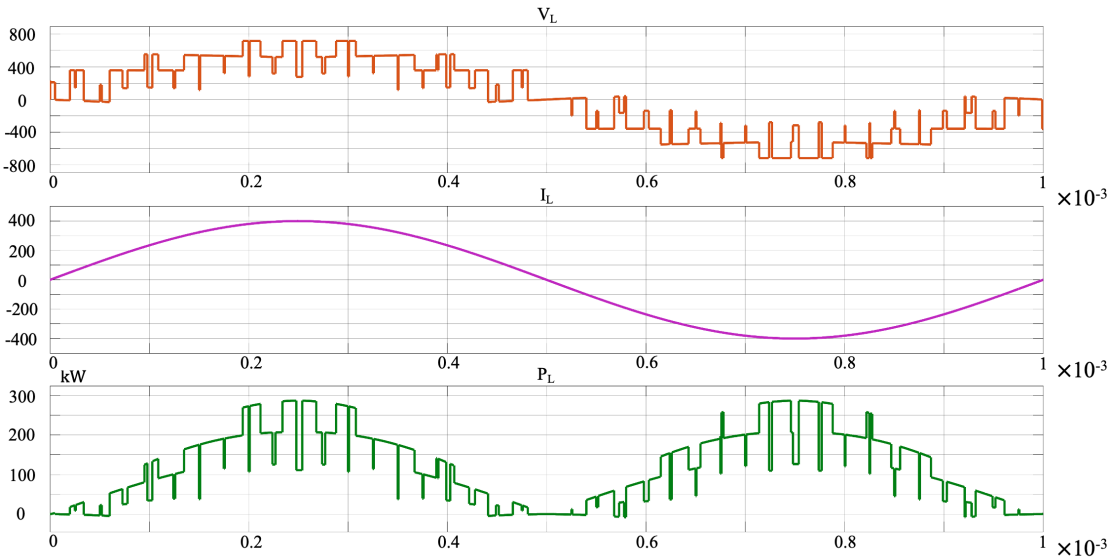
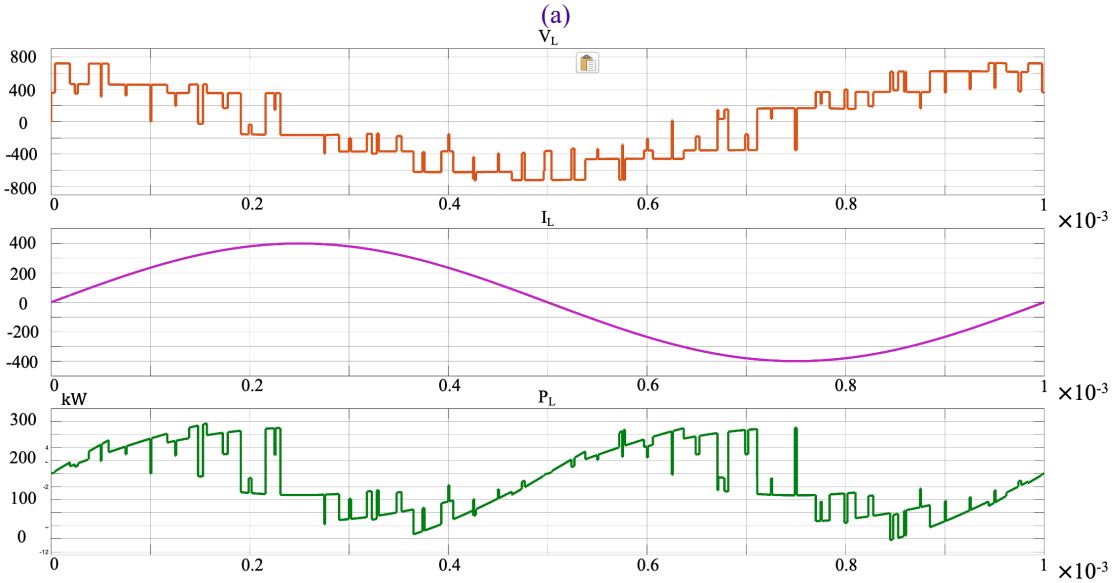


Fig.3-2 Phase-phase voltage, phase-neutral voltage, and load voltage waveforms

Fig.3-3 shows the output (load) characteristics of NPC converter when PF=1 (φ=0) and 0 (φ=90), respectively. Fig.3-3(a) reflects the power output when the voltage and current change synchronously, since the power factor is 0, the phase difference between the current and voltage in Fig.3-3(b) is 180°. the RMS value of load voltage is 400 V, the RMS value of load current is 282 A, and the output power is 112.8 kW per phase, which matches the design specifications for each phase output power target.



(a)



(b)

Fig.3-3 Load voltage, load current, and load power waveforms, (a) PF=1 (b) PF=0

Switching losses mainly occur as devices switch between on and off states. This is because during these transitions, the switching devices must pass through a state where both voltage and current are present, which results in significant energy losses. These losses can be estimated from the MOSFET and diode switching characteristics [166]. However, the more convenient way for calculating the switching losses is to utilize the switching energy-current (E-I) characteristic for on and off times. The switching losses can be calculated by (3.1) for the turn-on and turn-off energy in MOSFEET and diodes as [167].

$$P_{sw} = P_{on+off} = \frac{1}{\pi} \cdot f_{sw} \cdot [E_{on}(i) + E_{off}(i)] \tag{3.1}$$

Conduction losses occur when the switching device is in the on-state (i.e. turned on) state, due to the current needing to pass through the internal resistance of the switching device (known as the on-state or conduction resistance). Therefore, the power loss during conduction is computed by multiplying the voltage and the current in on-state. Integration of the instantaneous power losses over the switching cycle gives an average value of the MOSFET conduction losses:

$$P_{cond} = \frac{1}{T_{sw}} \int_0^{T_{sw}} p_{cond}(t)dt = \frac{1}{T_{sw}} \int_0^{T_{sw}} u_{ds}(t) \cdot i_{ds}(t)dt$$
$$= \frac{1}{T_{sw}} \int_0^{T_{sw}} R_{DSon}(i) \cdot i_{ds}^2(t)\, dt = R_{DSon} \cdot I_{Drms}^2 \quad (3.2)$$

The magnitude of the conduction loss is usually proportional to the square of the current, reducing either the current or the on-state resistance can reduce the conduction loss.

Fig.3-4 shows waveforms of V_{ds}, I_{ds}, and V_{gs} respectively of a MOSFET in one cycle. These waveforms are commonly used to analyse and optimise the switching behaviour, power loss and efficiency of transistors. The power losses discussed in this section are derived from this analysis. In the V_{gs} waveform, each transition from low to high or high to low represents a switching event. The switching energy can be estimated as $\Delta t \times V_{ds} \times I_{d,}$ where Δt is the duration of the switching. In Fig.3-4, the values of V_{ds} and I_{ds} during switching should be read at the same time points. The MOSFET conducts when V_{gs} is 15V. By reading the rms value of I_{ds} for each conduction period from Simulink, the conduction losses can be calculated. Total loss is the sum of switching loss and conduction loss. In this simulation, data from multiple cycles is required to make a more accurate average estimate.

Based on the methods described above, by analysing the simulation results of the established converter model, the conduction losses of the power MOSFET under different conditions can be determined. For the conduction loss comparisons in different power factors, the conduction loss is compared at the same modulation index (M=1) and power factor=1 (unity) and =0 (lagging). Table 3-1 and Table 3-2 show the conduction losses incurred when different numbers of MOSFETs are connected in parallel at power factor 0 and 1, respectively. According to simulation results, although the conduction losses produced by individual MOSFET are not significantly

different in both scenarios, a low power factor, which indicates a phase difference between current and voltage, leads to increased reactive power and potentially larger currents, thereby increasing conduction losses. In power electronic systems, increasing the power factor can reduce reactive currents, thus lowering conduction losses. Another conclusion is clear: regardless of the power factor, paralleling more devices in one switch means that less current flows through each device, resulting in lower conduction losses.

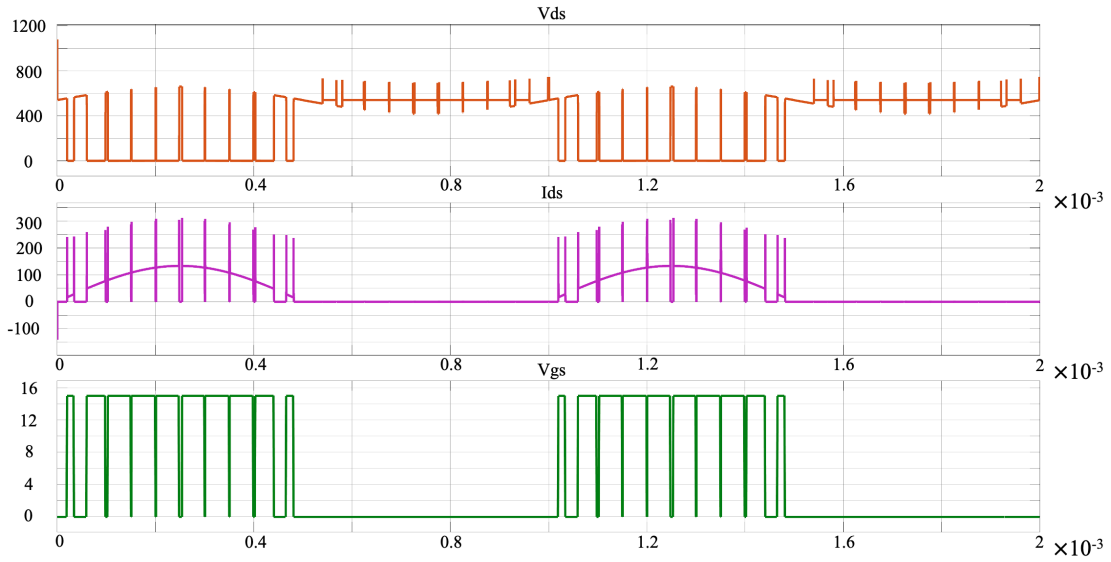


Fig.3-4 Characteristics of one MOSFET

Table 3-1 Conduction losses for different number of MOSFETs in parallel (PF=0)

Conduction losses (W)	Top/Bottom MOSFETs	Middle MOSFETs	Total losses/one leg
3 MOSFETs per Switch	56.22	79.80	816.12
4 MOSFETs per Switch	33.35	44.28	621.04
5 MOSFETs per Switch	20.24	28.13	483.70
6 MOSFETs per Switch	14.07	19.39	401.52
7 MOSFETs per Switch	10.34	14.18	343.28
8 MOSFETs per Switch	8.22	11.21	310.88

Table 3-2 Conduction losses for different number of MOSFETs in parallel (PF=1)

Conduction losses (W)	Top/Bottom MOSFETs	Middle MOSFETs	Total losses/one leg
3 MOSFETs per Switch	52.30	73.38	754.08
4 MOSFETs per Switch	29.72	42.39	576.88
5 MOSFETs per Switch	18.93	25.79	447.20
6 MOSFETs per Switch	13.45	18.02	377.64
7 MOSFETs per Switch	9.64	13.42	322.84
8 MOSFETs per Switch	7.60	10.57	290.72

Switching loss is independent of the modulation index M and the load PF [168] but increase linearly with switching frequency. Table 3-3 shows the switching losses per phase leg for different number of parallel MOSFETs, as the switching frequency remains the same, the switching losses of the device remain almost unchanged.

Table 3-3 Switching Losses for different number of MOSFETs in parallel

Switching losses per leg (W)	Temp.=25℃, F_{sw} = 20 kHz, I_{rms} = 282.2 A
3 MOSFETs per Switch	105.3
4 MOSFETs per Switch	97.8
5 MOSFETs per Switch	93.4
6 MOSFETs per Switch	98.8
7 MOSFETs per Switch	104.7
8 MOSFETs per Switch	102.4

The total losses of MOSFETs are expressed as the sum of conduction and switching losses, thus the total losses for each leg can be expressed as the sum of MOSFET losses and Diode losses, follows:

$$P_{total} = P_{cond} + P_{sw} + P_{clamping\ diode} \tag{3.3}$$

From losses given in Table 3-4 (I_{rms} = 282.2 A, f_{sw} = 20 kHz, PF=0), and Table 3-5 (I_{rms} = 282.2 A, f_{sw} = 20 kHz, PF=1), it is implying that conduction losses are dominant over switching losses. To achieve the efficiency target of 99% of 100kW output power, the power losses per leg should be less than 1000W. Based on this, the power density of the device can be obtained by the ratio of the total power loss to the surface area of the power device. The specific number of paralleled power devices will be determined by several factors, including converter efficiency, thermal effects of the module, internal layout constraints, and cost considerations.

The losses in the above tables are based on the characteristics of the device at a junction temperature of 25 ℃. From the device's datasheet, electrical characteristics at temperatures of 125℃ and 175 ℃ are provided in addition to those at 25 ℃. The same simulations have also been applied at these two temperatures. Due to space limitations, the specific values of device losses obtained are available in Appendix B for reference.

Table 3-4 Losses for different number of MOSFETs in parallel (PF=0)

Losses per leg (W)	Conduction losses	Switching losses	Diode losses	Total losses	Efficiency
3 MOSFETs per Switch	816.12	105.3	216.0	1137.42	98.99%
4 MOSFETs per Switch	621.04	97.8	211.8	930.64	99.17%
5 MOSFETs per Switch	483.70	93.4	232.2	809.30	99.28%
6 MOSFETs per Switch	401.52	98.8	223.8	724.12	99.36%
7 MOSFETs per Switch	343.28	104.7	221.4	669.38	99.41%
8 MOSFETs per Switch	310.88	102.4	214.8	628.08	99.44%

Table 3-5 Losses for different number of MOSFETs in parallel (PF=1)

Losses per leg (W)	Conduction losses	Switching losses	Diode losses	Total losses	Efficiency
3 MOSFETs per Switch	754.08	105.3	229.8	1089.18	99.03%
4 MOSFETs per Switch	576.88	97.8	228.6	903.28	99.19%
5 MOSFETs per Switch	447.20	93.4	232.2	772.80	99.31%
6 MOSFETs per Switch	377.64	98.8	225.6	702.04	99.38%
7 MOSFETs per Switch	322.84	104.7	225.6	653.14	99.42%
8 MOSFETs per Switch	290.72	102.4	229.2	622.32	99.45%

3.3 Loop Parasitic Inductance Effects and Impact of NPC Topology

This section reports the loop parasitic inductance model of the power module. Parasitic inductance is an inductance that is not intentionally designed but is added to or created by a specific object. Parasitic inductance in power modules is generally in the nH range. In short, parasitic inductance is created wherever there is an electric connection, but the inductance carried by different sizes or shapes of conduction paths varies. For example, the parasitic inductance of bonding wires inside power modules is generally in the range of nH, while the laminated busbars commonly used in power electronics are in the range of 10s of nH or even hundreds of nH. Inductors store energy by magnetic fields, as well as parasitic inductors.

The fast-switching transients of SiC devices results in high current gradients di/dt, significantly higher than those in traditional Si devices, leading to over-voltages $L\times di/dt$ ue to parasitic inductances intrinsic to interconnections, especially evident in multi-chip high power modules [169]. The power module is internally connected electrically between devices and terminals by using bond wires and copper substrate. Connections between devices inevitably introduce parasitic inductance, which causes voltage overshoot during commutations. Therefore, it is important to model the

different current loops inside the module and optimise the design to achieve a smaller parasitic inductance. Taking Cree's 1200V 300A SiC MOSFET module as an example, the switching loss of the module is about 6mJ at a low resistance of 2.5Ω and an RMS load current of 282A. The same current will store 4.0mJ of energy in a 100nH busbar, so the energy stored in the busbar is comparable to the switching loss of the device.

For the NPC three-level converter, the positive level cannot switch directly to the negative level, it must pass through neutral level in between. Moreover, for a bridge arm, only one device is allowed to turn on at a time, which means that there will not be a state where two devices switch at the same time. The available switching status and the commutation process is summarised in Table 3-6, four of the eight commutations are due to device turn-off and the other four are due to device turn-on. In this table, state 1 means the device is turned-on and state 0 means the device is turned-off. In addition, Fig.3-5 shows these four current commutation loops in NPC three-level converter.

Table 3-6 Commutation process of NPC topology

Switching state		Positive current		Negative current	
P-O	(1100)-(0100)	Loop A	T1 turn-off		
	(0100)-(0110)			Loop C	D1 reverse recovery
O-N	(0110)-(0010)	Loop B	T2 turn-off		
	(0010)-(0011)			Loop D	D6 reverse recovery
N-O	(0011)-(0010)			Loop D	T4 turn-off
	(0010)-(0110)	Loop B	D4 reverse recovery		
O-P	(0110)-(0100)			Loop C	T3 turn-off
	(0100)-(1100)	Loop A	D5 reverse recovery		

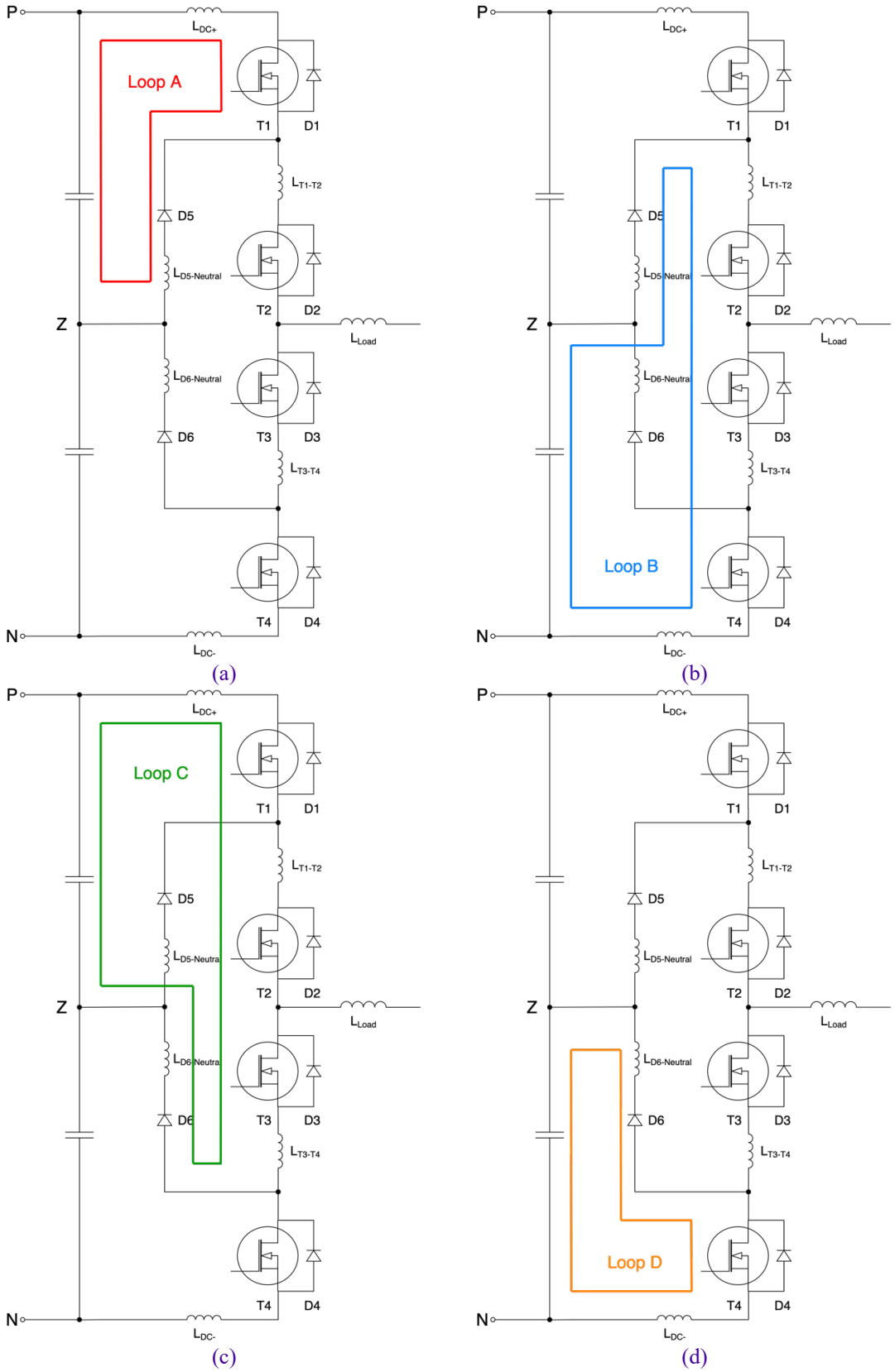


Fig.3-5 Current commutation in NPC converter

The NPC three-level converter half-bridge has a total of four commutation loops denoted in the following with letters A, B, C, D. Two loops A and D, are considered large as they involve both the top and bottom switches in a half-bridge leg,

corresponding to the large vectors of the standard space vector 3-level PWM. Two loops B and C are considered small as they involve one of the outer switches and the clamping diodes, corresponding to the medium or small vectors in the space vector PWM. The top and bottom switches T1 and T4 are turned off in the small commutation loop, while T2 and T3 are turned off in the large commutation loop. Reverse recovery occurs in D5 and D6 in the small commutation loop; in D1 and D4 in the large commutation loop, and no reverse recovery occurs in D2 and D3. In order to have similar over-voltages and therefore stress on the devices, it is desirable for the loop A and loop D to have similar parasitic inductance values, and similarly for loops B and C.

In reference to Fig.3-5, the inductance of the different commutation loops can be expressed as:

$$\begin{aligned} L_{loop\,A} &= L_{DC+} + L_{D5-neutral} \\ L_{loop\,B} &= L_{DC-} + L_{D5-neutral} + L_{T1-T2} + L_{T3-T4} \\ L_{loop\,C} &= L_{DC+} + L_{D6-neutral} + L_{T1-T2} + L_{T3-T4} \\ L_{loop\,D} &= L_{DC-} + L_{D6-neutral} \end{aligned} \tag{3.4}$$

Large parasitic inductances can lead to severe voltage overshoots and oscillations at high di/dt switching, therefore the next step is to simulate the DPT to obtain the voltage overshoots and oscillations. The device under test (DUT) is driven with two short on-pulses. Pulse one is used to ramp-up the current through the load inductor. The length of pulse one along with the inductor value and bus voltage sets the load current, I_L. At the end of pulse one the DUT is driven off and current commutates to and circulates through the clamping diode (D5 and D6). Given the forward voltage drop of the clamping diode is small compared with the bus voltage, any decay of the inductor current will be negligible so long as the off period is kept short, Fig.3-6 shows the basic double pulse test waveforms.

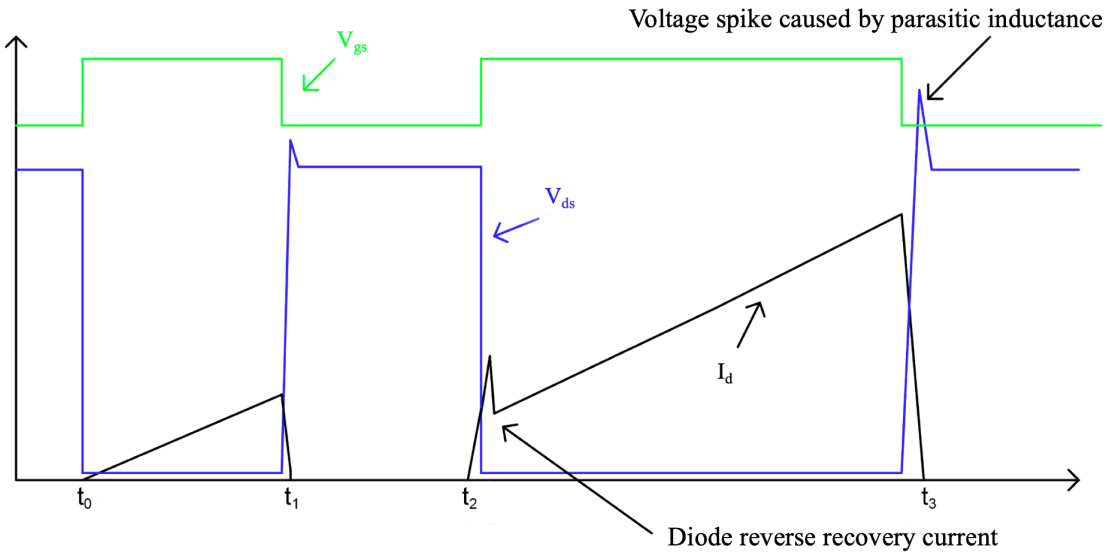


Fig.3-6 Basic experimental waveforms of DPT

At t_0, the first pulse is applied to the gate, the MOSFET under test is saturated and conductive, the electric potential U is added to the load L, the current of the inductor rises linearly. When both U and L are determined, the current value is determined by t_1, and the longer the time, the higher the current. Therefore, the value of the current can be set autonomously.

At t_1, the DUT is turned off and the current of the load L is renewed by the clamping diode, which decays slowly. At t_2, the second pulse is applied to the gate, the MOSFET under test conducts again, the freewheeling diode enters reverse recovery, and the reverse recovery current passes through the DUT as shown in the figure. At t_3, the MOSFET under test turns off again, and the current is higher at this time, because of the parasitic inductance, a voltage spike will be generated because of the parasitic inductance, expressed as:

$$\Delta V_{ds} = L_\sigma \times \frac{di_d}{dt} \tag{3.5}$$

Fig.3-7 shows the state of each switch and current path when testing the switching characteristics of the different devices, picture (a) shows test for device T1 and D5, picture (b) shows test for device T2 and D4, picture (c) shows test for device T3 and D1, picture (d) shows test for device T4 and D6. The current conduction paths are shown in blue and the current freewheeling paths are shown in green.

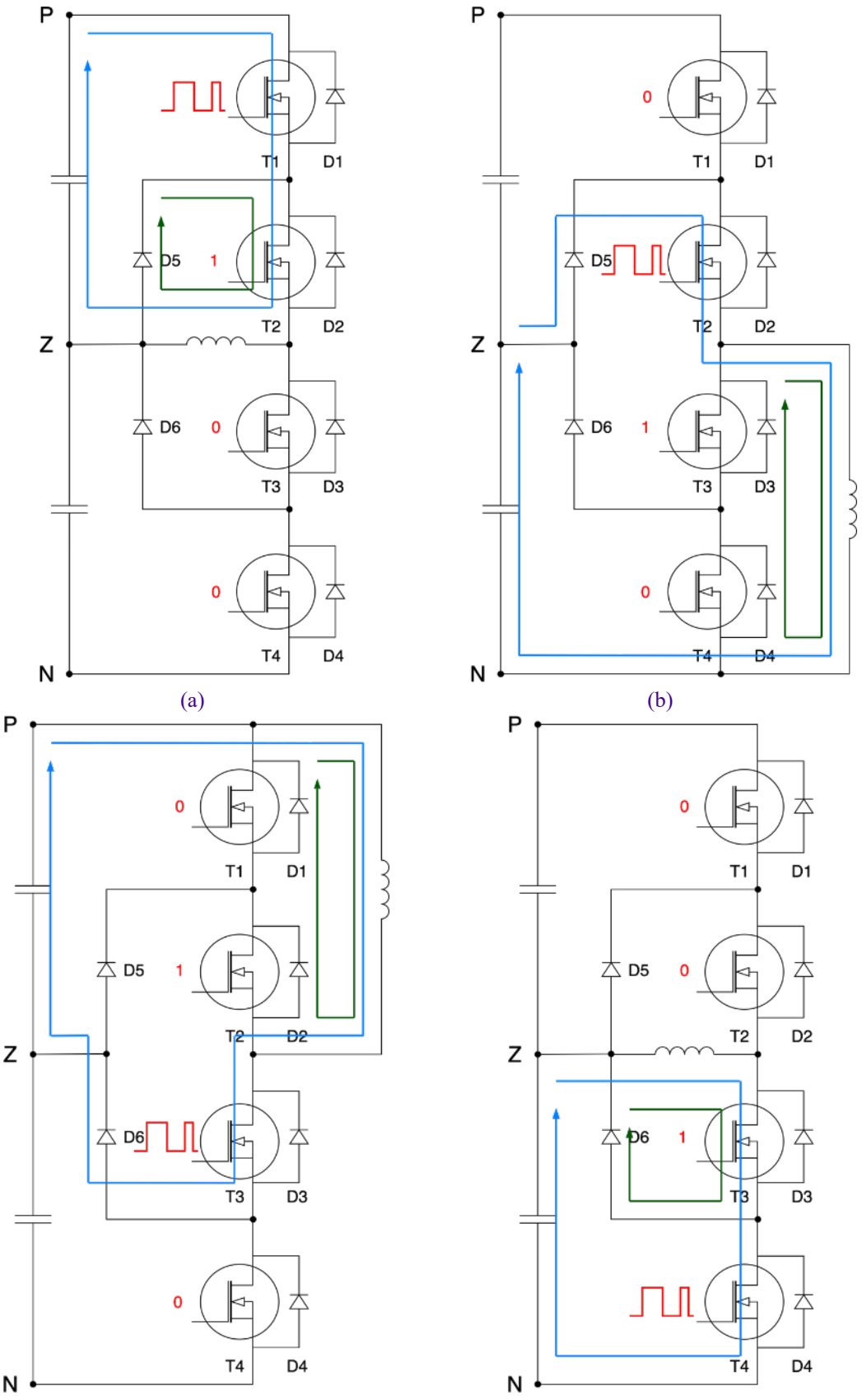


Fig.3-7 Double pulse test for different devices (Blue: current conduction path, Green: current freewheeling path, Red: gate drive signal)

3.4 Power Module Design and Layout Optimisation

Power module packaging integrates multiple discrete power electronic devices to meet the specific needs of various power and voltage applications. These modules provide electrical connections, structural integrity, and thermal management for power semiconductor devices. Most of the current research uses a combination of multiple two-level power modules to build a three-level NPC topology converter, this method requires additional electrical connections may introduce additional parasitic inductance, which in turn affects the switching characteristics of the power device. In this chapter, the proposed three level NPC power module will deliver a multi-level full SiC module suitable for 540V/1080V DC applications, which are typical voltage levels being considered for MEA applications. The main novelty is that the thesis offers a multi-level power module analysis (from both electrical, electromagnetic, and thermal aspects) for aerospace applications using third-generation semiconductors as critical components. Fig.3-8 shows the power module physical diagram, the electrical connection diagram, the compact converter, and the use of converter in the overall drive system.

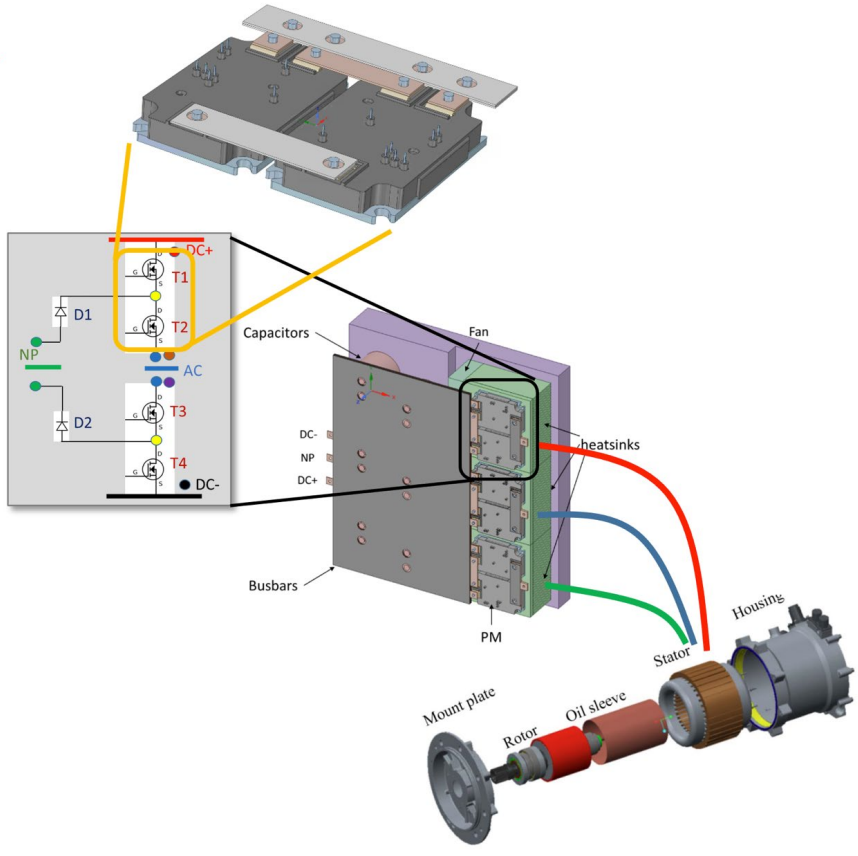


Fig.3-8 Compact drive system

3.4.1 Selection of Power Semiconductor Devices

As discussed in Chapter 2, the optimal power device will be selected among those available commercially considering performances (e.g., on-state resistance $R_{ds(on)}$, maximal current and other relevant electrical and thermal characteristics), availability, lead time and compatibility of the metallization with the sintering process employed by the manufacturing project partner Dynex Semiconductors. Based on the specification, 1200V SiC devices were considered for the application. On this basis the suppliers considered were Rohm, STMicroelectronics and Wolfspeed.

Depending on the application scenario of the power module, the requirements and criteria used for the choice of MOSFETs are:

- High drain current (I_d)
- Low Drain-Source resistance ($R_{ds(on)}$)
- Device rated breakdown voltage (V_{BR}) 1200V
- Availability on relatively short lead time (weeks, not years)
- Suitability of source and gate terminals on top of die for wire bonding
- Availability of surface metallisation
- Availability of a companion diode of a suitable current and voltage rating to pair with the MOSFET

The highest current rated device shown on Rohm catalogue is the S4103 1200V N-channel SiC power MOSFET bare die, at 95A@25°C, $R_{ds(on)}$ of 22mΩ. Rohm also has SiC diodes, but only as discrete packaged devices, not bare die which are required. STMicroelectronics has 1200V MOSFETs available, but due to very high demand and low capacity, their typical lead time was 2 years, which is not practical. Apart from the lead time ST MOSFETs are an attractive option because of the competitive cost, high I_d, small device size and low $R_{ds(on)}$. The SCT110N120G3D2AG MOSFET for example has V_{BR} 1200V, I_D 100A@25°C, 79A@100°C, and 15mΩ $R_{ds(on)}$. ST diodes max current rating is 40A at 1200V V_{BR}, and 173nC capacitive charge. Despite the good performances of these devices, the long lead time make the STMicroelectronics dies not practical. Wolfspeed has readily available as bare die CPM3-1200-0013A, which are 1200V MOSFETs with current rating of 149A@25°C, and 102A@100°C, with very low $R_{ds(on)}$ at 13mΩ. These are available on relatively short lead time (weeks) from distributors available. Wolfspeed also has a 1200V, 50A, 250nC SBD

diode CPW5-1200-Z050B, to pair with these MOSFETs. The device has terminals which are suitable for manufacturing with Dynex processes and have metallisation options suitable for wire bonding. ON Semiconductor has 1200V MOSFETs available on market, the NTBG020N120SC1 has similar parameters compared to Rohm's S4103, its I_D is 98A@25°C, and 20mΩ $R_{ds(on)}$. The lower I_d and higher $R_{ds(on)}$ make these two devices not very competitive in this application. Especially according to the simulation results from Chapter 2, when paralleling three or more MOSFETs in one switch, the CPM3-1200-0013A's performance is much improved and better than the NTC020N120SC1.

Based on the criteria and available options, Wolfspeed CPM3-1200-0013A SiC MOSFETs and Wolfspeed CPW5-1200-Z050B SiC diodes were chosen as the preferred devices type due to commercial availability, ease of manufacturing and suitable power ratings.

3.4.2 Power Module Layout Optimisation

The power module layout requires the smallest possible loop inductances. Commutation loop parasitic inductances have been calculated using ANSYS Q3D software. The four commutation loops are illustrated in Fig.3-9, for two potential layouts considered during the design process. The half-bridge NPC leg is realized in both cases with two sub-modules, one for devices T1-T2-D5 and one for T3-T4-D6. This approach is adopted to maximise yield and minimise manufacturing complexity and cost of very large substrates. Two external connections through busbars will be needed to connect the output and the NPC point, respectively, of the two sub-modules. Although this results in additional length of the current paths and consequently additional parasitics, the cost and yield benefits still justify the approach.

As shown in Fig.3-9, two module layouts were considered corresponding to a symmetric and asymmetric design, respectively. The advantage of the asymmetric design is that both sub-modules use the same DCB substrates, which can save costs, reduce part numbers and manufacturing steps. However, in the asymmetrical design, the neutral point connection terminals on the two sub-modules are on opposite sides (left for the top sub-module and right for the bottom) and, therefore, long external busbars will be needed for connecting the two terminals. On the other end, in the symmetrical design both the neutral point terminals are on the same side (right of the

module) in common with the positive and negative DC-bus terminals. This approach reduces the physical size of the external busbar, which reduces the resulting parasitic inductance. In the symmetric design the corresponding commutation loops A/D and B/C have similar lengths. Therefore, it is expected that the relative parasitic inductances LA/LD and LB/LC will be similar resulting in similar voltage transients. This is not the case for the asymmetrical design, where the conduction paths A/D and B/C are different. This asymmetry and the corresponding difference in inductances will result in different commutation transient voltages when the module commutates between the DC+ and midpoint, and DC- and midpoint. The final design adopts the symmetrical layout. For the symmetrical design, the substrates of the two sub-modules are different and need to be fabricated separately.

(a) (b)

Fig.3-9 Commutation loops for the three-level leg for: (a) Asymmetrical design (b) Symmetrical design

The commutation loop inductances have been evaluated for the two designs using ANSYS Q3D. A 3D CAD model of the SiC module is drafted in ANSYS Spaceclaim and simulated in Q3D as shown in the example of Fig.3-10 for loop B. This figure shows the results of a 3D electro-magnetic field simulation, specifically for the current density distribution in the power module. The changes in colour represent different levels of current density. Such distribution maps can reveal areas of concentrated current and potential hotspots, which are crucial for optimising circuit design and enhancing efficiency. The zoomed-in view in the figure shows the detailed current density distribution at wire bonds, where the highest current density occurs in

this example. In that specific area, the current density reaches 130A/mm², measured under a current excitation of 400A.

The complete commutation loops are constituted by the connection of several branches each with its partial parasitic impedance. The inductance values and their series resistances were evaluated at 1 MHz. Each of these partial impedances is extracted numerically in Q3D and the total inductance are reported in Table 3-7, this table shows that the difference in parasitic inductance between loop A and D in the asymmetric design is more than double, and there is also a 8nH difference between loop B and C. The parasitic inductance between loops A and D in the symmetric design, as well as the parasitic inductance between loops B and C, are very close to each other, confirming the expectations for balanced inductances for the symmetrical loops.

Table 3-7 Loop parasitic inductances

Design	Loop A	Loop B	Loop C	Loop D
Asymmetrical	22.2nH	68.5nH	76.9nH	9.3nH
Symmetrical	11.1nH	75.3nH	74.6nH	9.9nH

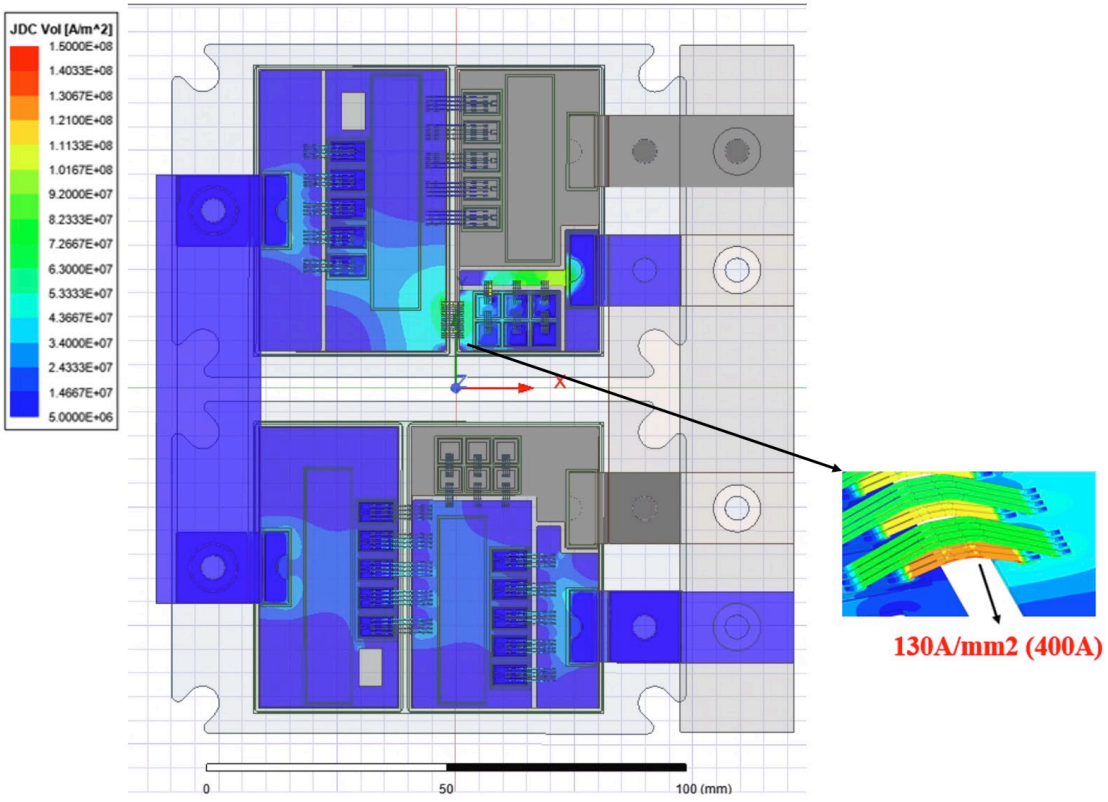


Fig.3-10 Q3D simulation plot of loop B current density distribution

Potential coupling between the control loops associated with the gate drive signals and the power loops associated with the commutation current signals need to be minimised or even avoided. This can be achieved by arranging the control loops and current loops to be perpendicular. The final design features perpendicular loops as shown in Fig.3-11, C1-C4 are control loops for T1-T4 MOSFETs respectively.

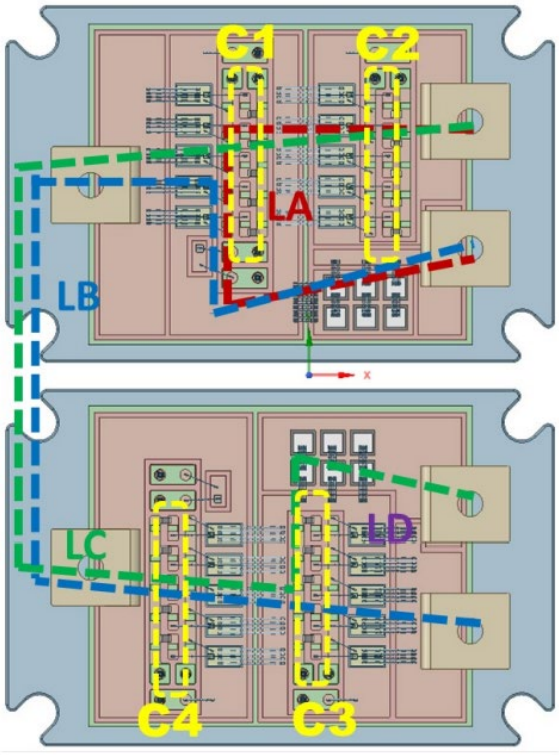


Fig.3-11 Interaction between the power and control loops

Table 3-8 shows the self-inductances of the control loops C1-C4 and the mutual inductances between the control loops and power loops obtained by using ANSYS Q3D. It is clear that the mutual coupling is relatively small, implies that the influence of the control loop on the commutation loop in this layout is negligible.

Table 3-8 Control loop inductances

Control Loops	Self-inductance	Mutual inductance	
C1	17.09nH	LA	0.16
		LC	0.93
C2	16.95nH	LA	0.48
		LC	0.97
C3	17.15nH	LA	0.03
		LC	0.70
C4	17.06nH	LA	0.03
		LC	0.78

Once extracted, detailed parasitics can be used for detailed electrical circuit simulations in numerical software e.g. Spice or MATLAB/Simscape to evaluate the converter's performance under switching conditions and support the optimisation of the module's design, this part will be covered in detail in Chapter 4.

Fig.3-12 shows a comparison of different loop inductances in the power modules used in other studies compared to the 100kW 3L-NPC power module developed. Due to the topology characteristics, in 3L-TNPC, the different commutation loops do not differ significantly in terms of distance, therefore there is no significant difference between the parasitic inductance values of the two commutation loops. According to the simulation results, compared to the published literature [170], the parasitic inductance of small loop in the proposed power module is much smaller compared to the 100kVA and 150kVA TNPC modules with similar power levels, while the parasitic inductance of large loop is relatively larger due to the disadvantage of topology. When compared with the 10kW TNPC module, the parasitic inductance of the large loop is about 20nH larger, and the higher power makes it more competitive. The parasitic inductance of small loop and large loop is smaller when comparing with other NPC modules, but due to the different power ratings of these three modules, the results here are for reference only.

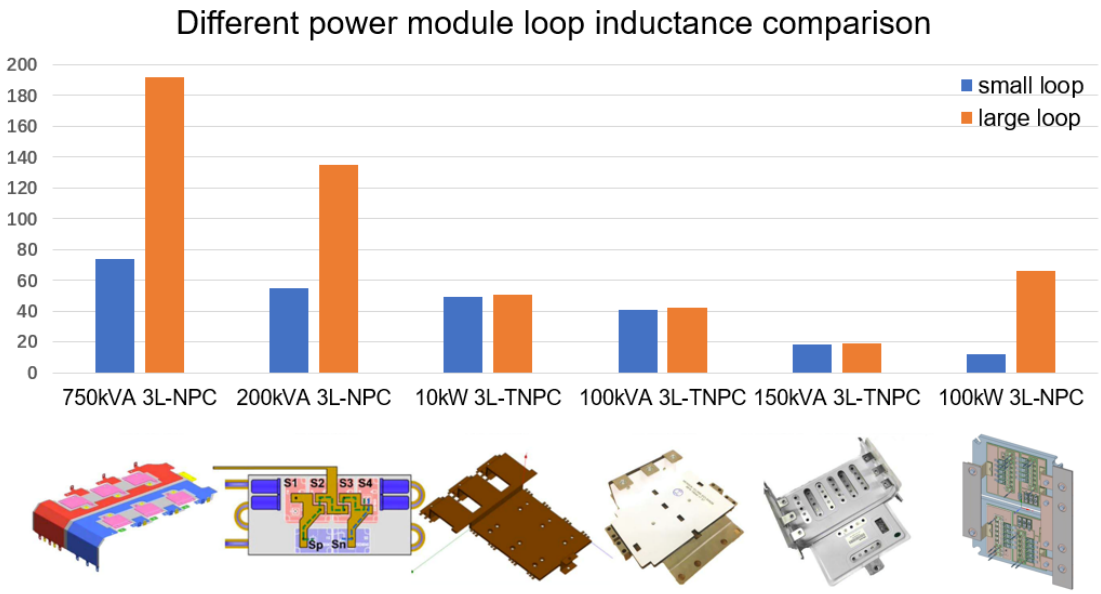


Fig.3-12 Loop parasitic inductance comparison [169]

3.4.3 Power Module Construction

The module embeds a high reliability Si3N4 substrate soldered to an AlSiC baseplate for air cooling. The employment of these materials helps to reduce the thermal expansion mismatch while allows sufficiently low thermal resistance of the junction to case resistance. The use of AlN auxiliary substrates can provide low parasitic resistance for the main power loops, low mutual inductance between the power loop and the control loop, and also works as good scalability on the main substrate. For die attachment (NTC & auxiliary substrate), a high temperature solder alloy of Sb5Sn was employed while SAC was used for the rest joints. Ultrasonic Al wire bonding is employed for the interconnect to avoid excessive use of long busbar, and thus reduce the parasitic resistance. The overall process is honoured to follow the following steps:

1. Die, temperature sensor, auxiliary substrate attachment: The module prototype starts with the attach of dies, negative temperature coefficient (NTC) and auxiliary substrate, by solder reflowing of high temperature Sn5Sb solder alloy.
2. Initial wire bonding: Al wires were applied for the gate to the auxiliary substrate connect, the source to auxiliary substrate connects, the connection for the temperature terminals, and the source to drain connect on individual substrates. A total of eight Al wires were employed to bond each MOSFETs and four Al wires were used for bond each diode, see Fig.3-13.

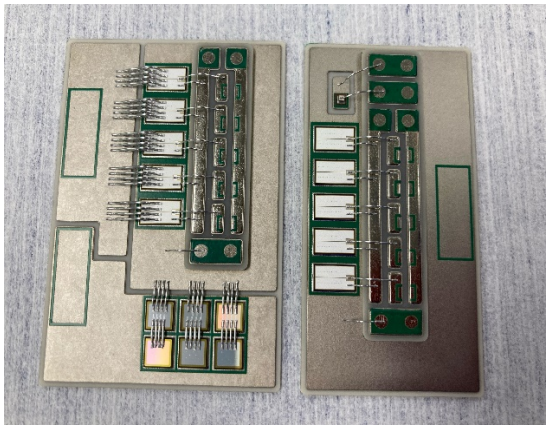


Fig.3-13 Substrate samples after initial wire bonding

3. Substrate attach: SnAg3.5Cu was employed for attaching the power substrate to the AlSiC baseplate. Fig.3-14 shows the power substrate after bonding.

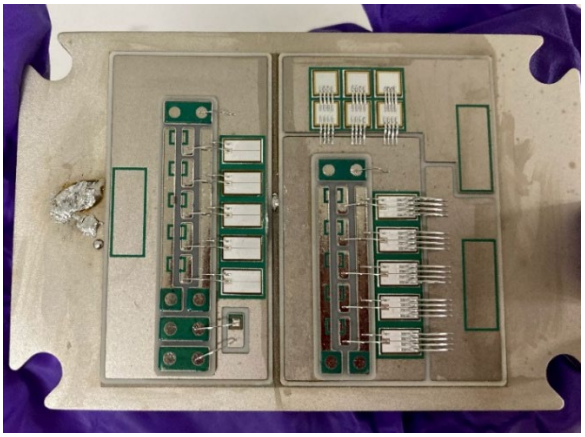


Fig.3-14 Baseplate sample after substrate attachment

4. Final wire bonding: Final wire bonding process is carried out when substrate have been attached to the baseplate, this is to connect the two switches from two substrates in series.
5. Terminals and gate resistor bonding: The bonding for terminal, pins and gate resistors were carried out together after all the wire bonding process has completed. Fig.3-15 shows the picture of baseplate sample with terminals.

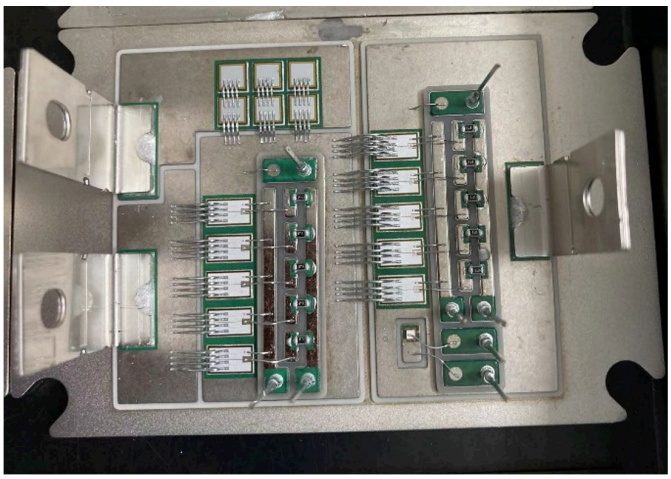


Fig.3-15 Photo of baseplate sample before frame bonding

6. Frame bonding: Power module cases were bonded onto the AlSiC baseplate using an industry-used gel, 3D printed cased were used.

3.5 Thermal Considerations

The electrical and thermal behaviour as well as the electro-thermal interactions within the package design have been simulated using a suite of modelling tools. These include high-frequency modelling (e.g. using Ansoft Q3D), ANSYS Mechanical and

ICEPAK. The extensive electro-thermal simulations of the power module have been performed with the aim of verification of the performance within the required MLC application to comply with the performance specifications.

3.5.1 Steady State Thermal Analysis

A vertical cross-section of the proposed module is shown in Fig.3-16. The heat-flow paths from the dies passes through eight physical layers in the model: SiC MOSFETs/diodes, $SnSb_5$ solder layer (act as a heat spreader to dissipate heat from the MOSFETs/diodes), top Cu substrate layer, Si_3N_4 Ceramic substrate layer, bottom Cu substrate layer, substrate to baseplate SnAgCu305 solder attach, Cu101 baseplate, and TIM. It is assumed that the bottom surface of the TIM is in contact with a fixed temperature heatsink.

Fig.3-16 Vertical cross-section of power module

Table 3-9 shows the thickness and thermal conductivity of these materials used in the proposed power module, the thickness of the material was determined by the partner company, DYNEX Semiconductor, based on previous product experience, to ensure that it met the requirements of safety standards.

Table 3-9 Thickness and thermal conductivity of different layers

Material/Layer	Thickness (mm)	Thermal Conductivity (W/mK)
SiC MOSFET	0.18	99.5
SiC diode	0.38	99.5
SnSb5 solder layer	0.05	57
Top Cu substrate layer	0.30	400
Middle ceramic substrate layer	0.30	33
Bottom Cu substrate layer	0.30	400
SnAgCu305 solder layer	0.20	58
Copper baseplate	3.00	400
Thermal pad	0.25	6.5

Power loss densities of the top and bottom sub modules are applied as inputs to the thermal model established in ANSYS package. It is expected that the losses and

efficiency calculation remain approximately the same in the final design as they are only marginally affected by the dies location on the substrate.

Simulations were conducted with losses calculated assuming devices characteristics at T_j=25°C, 125°C and 175°C. An ideal heatsink surface temperature at 80°C is assumed to provide a boundary condition on the bottom TIM surface. Results for five MOSFETs and six diodes are reported in the following figures. This section only presents the thermal simulation results of the device characteristics at T_j=175°C. This is the case where the device produces the highest power losses and is used to represent the worst-case scenario. Fig.3-17 shows the temperature distribution at T_j=175°C, the highest temperatures are generated at the middle MOSFETs, as this is where the highest power losses are generated.

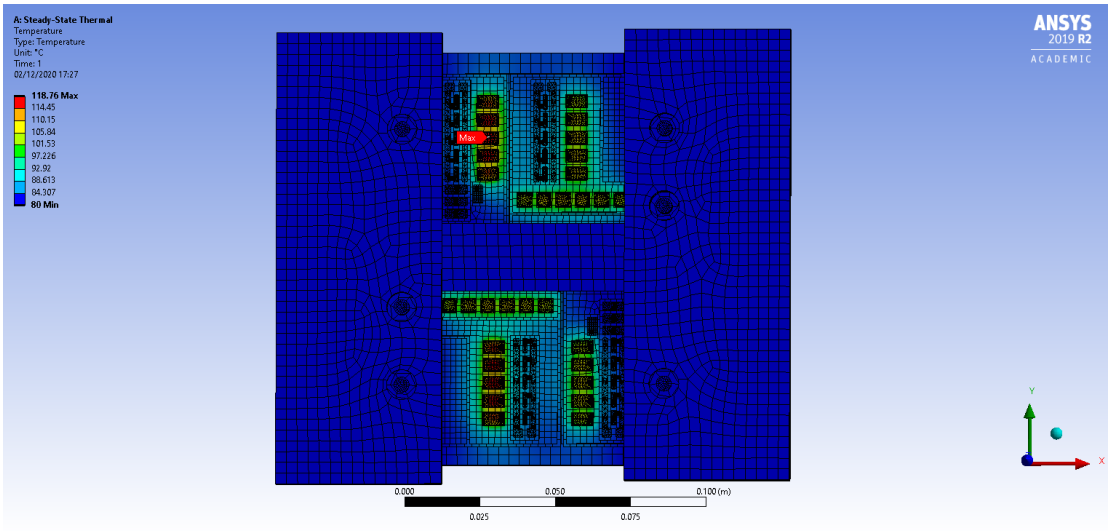
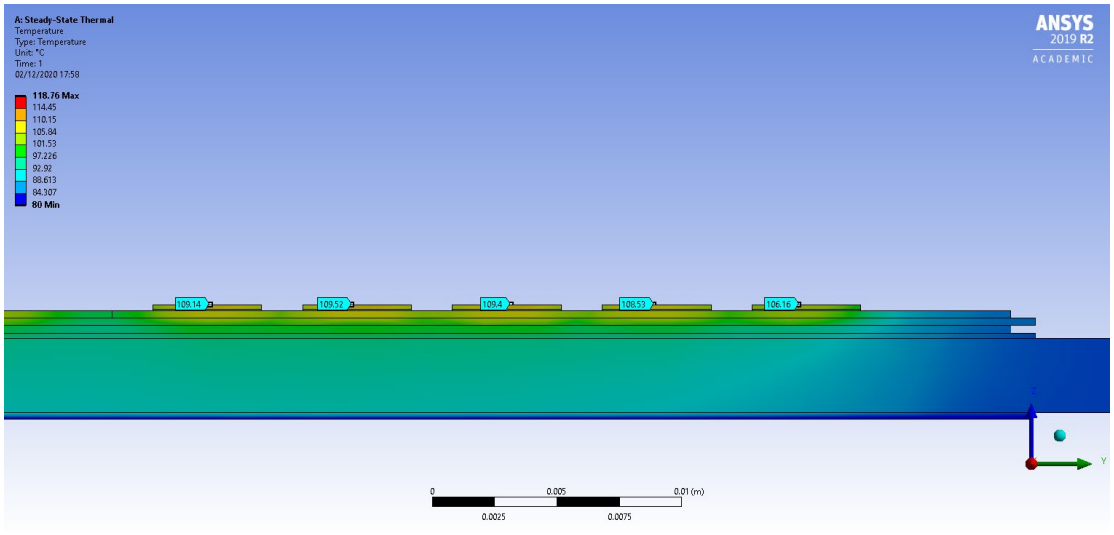
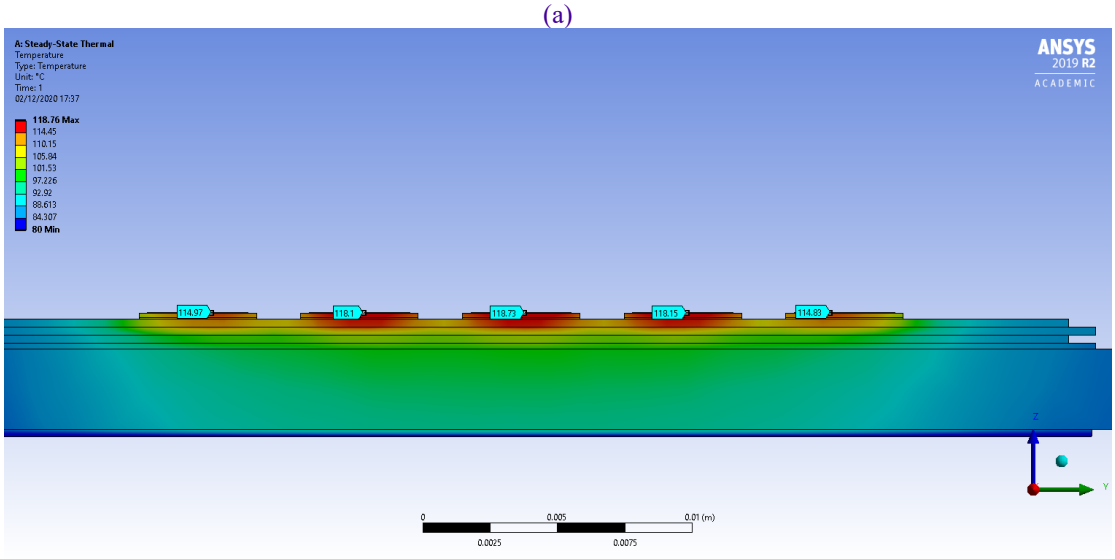


Fig.3-17 Steady-state temperature distribution (losses calculated at 175°C)

Fig.3-18(a), (b), and (c) show the vertical temperature distribution for the top/bottom MOSFETs, middle MOSFETs, and clamping diodes, respectively. When using the losses calculated under the 175°C characteristics for thermal simulation, the maximum temperature is around 109°C on top/bottom MOSFET, 118°C on middle MOSFET, and 109°C on clamping diode.



(a)



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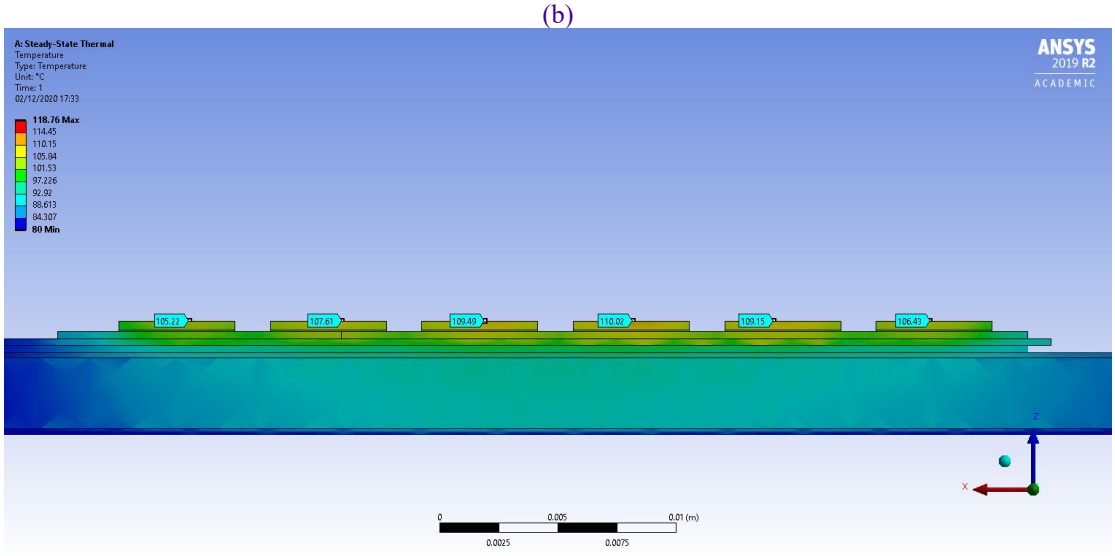


(c)

Fig.3-18 Vertical temperature distribution of (a) top/bottom MOSFETs (b) middle MOSFETs (c) NPC diodes

Due to packaging and reliability issues, according to the datasheet, it would be desirable to restrict the maximum devices temperature to below 175°C. This means that the maximum temperature obtained even in this worst-case scenario satisfies the design requirements.

In aerospace applications, reducing the weight of modules is crucial for enhancing fuel efficiency, and it is also important to maintain consistent performance in high-temperature and harsh environments. In power modules, while the materials for power devices and substrates are usually fixed, there is still room for improvement in the choice of baseplate materials. To evaluate the thermal performance of power modules with different baseplate materials, simulations are conducted in ANSYS Mechanical. The boundary conditions are assumed iso-thermal at 80°C on the heatsink top surface. A TIM Kerafol KERATHERM ROT86/82190X190X0.25 86/82 Thermal Pad 6.5W/mK is assumed between the modules baseplate and the heatsink.

Simulations have been conducted with both copper and AlSiC baseplates. AlSiC has significantly lower density (3.01g/cm^3) than Cu (8.96g/cm^3) resulting in significantly lighter modules and ultimately higher power density of the converter. Additionally, AlSiC has a coefficient of thermal expansion (from 6.5 to 9x10^{-6}) lower than Cu (17 x10^{-6}) and closer to SiC (4 x10^{-6}). The better matched coefficient of thermal expansion of AlSiC and SiC dies results in lower thermo-mechanical stress in transient thermal conditions which ultimately improves the expected reliability of the modules. However, AlSiC has a lower thermal conductivity (180–200W/mK) than Cu (400 W/mK) resulting in higher expected temperatures, in extreme high-power applications, copper baseplate may still be preferred because their excellent thermal conductivity helps dissipate heat more efficiently. This is confirmed by the simulation results shown in Fig.3-19, since the thermal conductivity of AlSiC is lower than that of copper, the modules with AlSiC baseplates exhibit higher temperatures at the hottest points compared to those with copper baseplates. Fig.3-20 shows the corresponding vertical temperature distribution, it displays a temperature gradient from the bottom to the top of the device, with higher temperatures near the areas where the current flows, revealing the effectiveness and path of heat dissipation in the vertical direction.

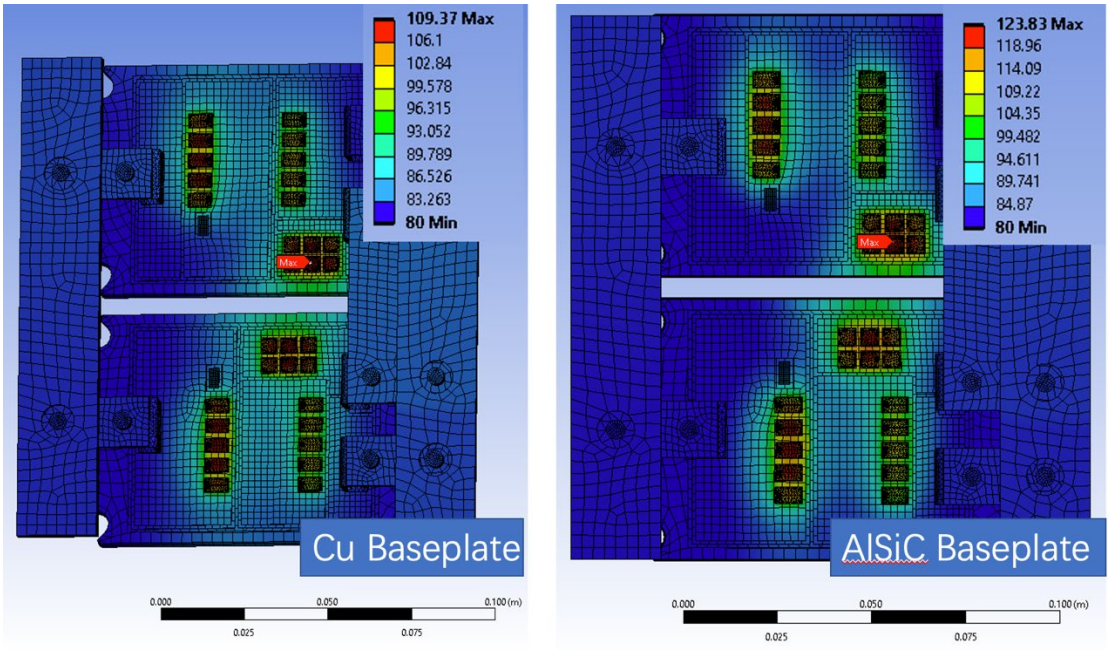


Fig.3-19 Steady-state temperature distribution in the power modules

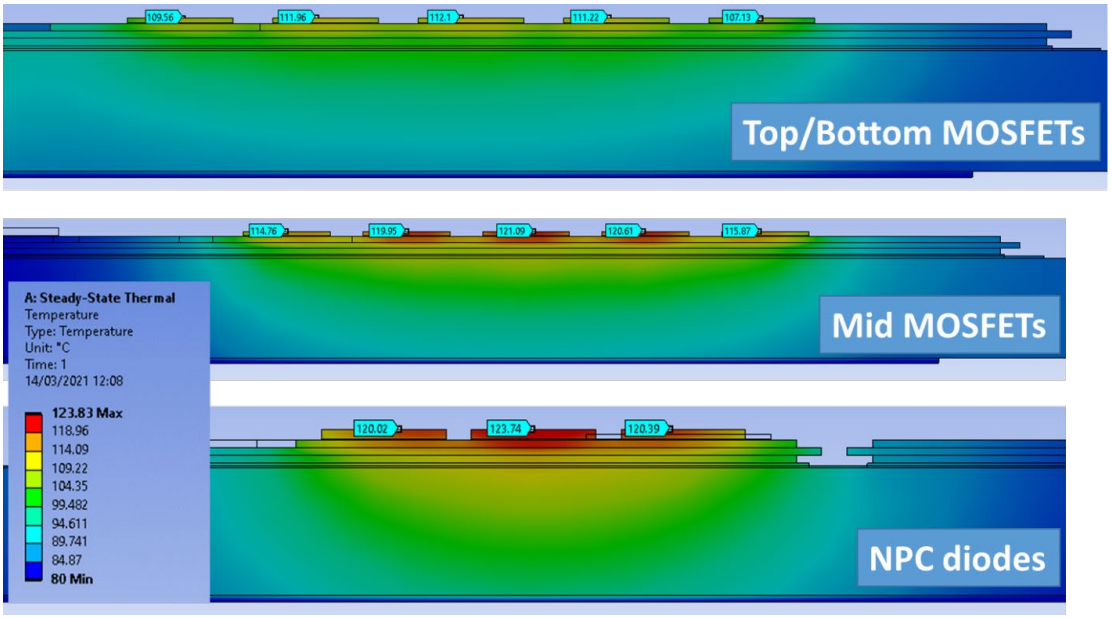


Fig.3-20 Steady-state vertical temperature distribution in the power modules

Table 3-10 summarises the maximum temperatures that can be achieved in different devices when using different materials baseplate. In both cases the maximum temperatures are in the diodes and the peak temperature is expected to be 15°C higher with the AlSiC baseplate. Despite the slightly worse thermal performances, the advantages mentioned above make AlSiC the preferred option in this design.

Table 3-10 Maximum temperature of the different devices

	Cu baseplate	AlSiC Baseplate
Top/Bottom MOSFETs	101.6℃	110.1℃
Middle MOSFETs	107.3℃	118.9℃
NPC Diodes	107.5℃	119.2℃

3.5.2 Transient Thermal Analysis

Transient thermal simulations have been conducted to calculate the thermal impedance in a single-pulse case. In single-pulse tests, by applying a rapid current or voltage pulse and measuring the temperature change after the pulse, thermal impedance can be calculated, this leads to a more comprehensive assessment of the thermal performance of the device. This test reveals the device's instantaneous temperature response, which is crucial for assessing thermal stability and reliability in practical use. The FE method allows the observation of the transient response of the thermal model and thus extracts the parameters of the RC thermal network model for further thermal design, thermal management, life prediction, etc. Transient thermal simulations have been conducted to calculate the thermal impedance in a single-pulse case. Results are shown in Fig.3-21 for the SiC MOSFETs, and in Fig.3-22 for the clamping diodes.

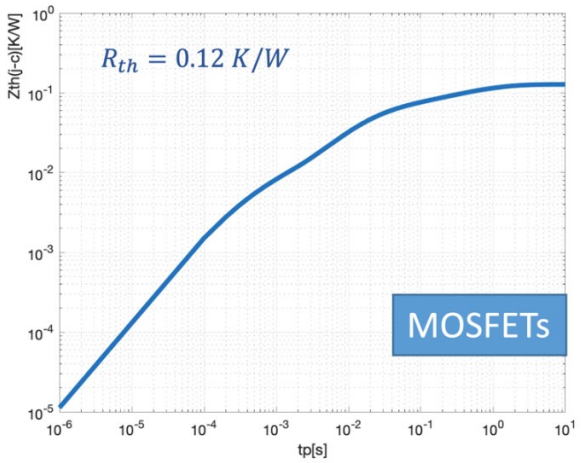


Fig.3-21 MOSFETs transient thermal impedance for single-pulse

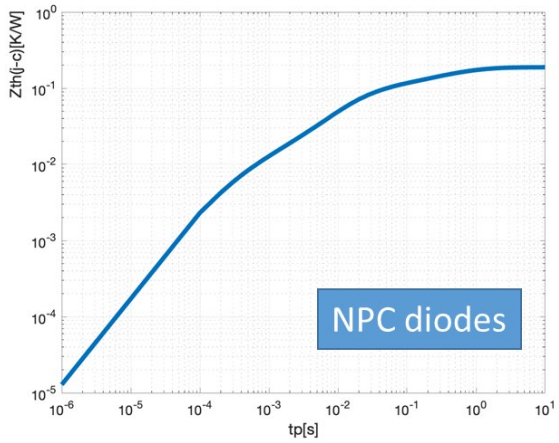


Fig.3-22 Diodes transient thermal impedance for single-pulse

Although the RC parameters of the Foster model does not correspond to each material layer, the RC parameters in the model can be easily extracted by fitting from the transient thermal impedance Z_{th} curve obtained from actual measurements, so the model is often used for practical modelling and simulation to calculate the junction temperature of the power device.

The real-time thermal performance of the module was evaluated through in-situ transient thermal impedance measurement. During the thermal test, the junction temperature T_j of the body diode of SiC MOSFET was monitored by using the forward voltage drop V_f across the body diode. The MOSFET body diode was heated up with a heating current of 50A for 120s to reach thermal equilibrium. Following this, the heating current was discontinued, and the changes of the forward voltage of the body diode was recorded during the cooling stage under a constant bias current of 50 mA, for another 120s. The forward voltage recorded was then converted into the junction temperatures of the body diodes. During the test, the MOSFET was totally switched off by applying a negative gate voltage.

The transient thermal impedance profile of the SiC MOSFET is shown in Fig.3-23 along with a list of fourth-order parameters (in the form of the corresponding combination of thermal resistance R_i and time constant τ_i) for the Foster model, from this figure the thermal resistance is 0.11K/W which is close to the simulated value.

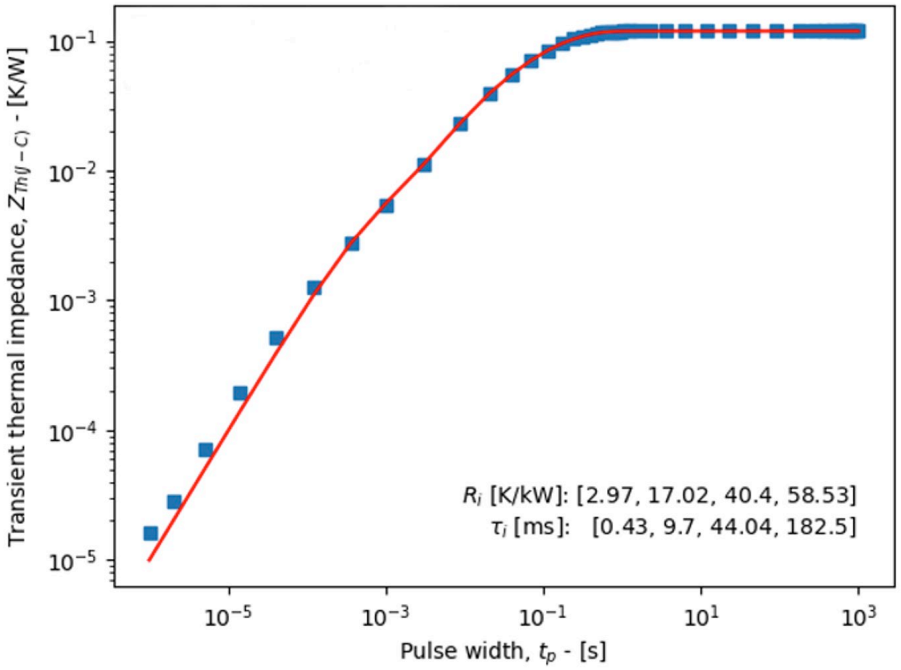


Fig.3-23 SiC MOSFET thermal impedance curve

The dynamic thermal resistance curve can be expressed as (3.6):

$$Z_{thjc}(t) = \sum_{i=1}^{n} r_i \times (1 - e^{-\frac{t}{\tau_i}}) \qquad (3.6)$$

$$\tau_i = r_i \times c_i$$

If the power device loss P(t) is known and the module's base plate temperature is known during the dynamic temperature rise process, the junction temperature of the power device can be obtained from the equation (3.7):

$$T_{vj}(t) = P(t) \times Z_{thjc}(t) + T_{case}(t) \qquad (3.7)$$

3.5.3 CFD Thermal Analysis

The boundary conditions used in the FE simulation presented previously were assuming a power module baseplate temperature of 80℃ to represent the worst-case scenario. Instead of this boundary condition, this subsection uses the complete heat sink with fan to evaluate the module's performance, here, the temperature of the devices at different air speeds will be simulated using ANSYS Icepak. The CFD

capabilities of ANSYS Icepak provide a sophisticated simulation environment for analysing and predicting the temperature distribution and heat transfer within electronic devices under various cooling conditions. Through these simulations, the goal is to determine optimal airflow parameters that maximise cooling efficiency without compromising device performance. In the simulations the fan model is Ebmpapst 8314H and the heatsink is LA 10/150 24V from FISCHER ELEKTRONIK.

According to the fan's air volume-static pressure characteristic diagram shown in Fig.3-24 (P-Q curve), the maximum flow rate will appear when the pressure drop across the fan is zero. This only happens if there are no obstacles in front of or behind the fan, allowing air to flow freely into and out of the fan. Once the fan is partially blocked, such as a heatsink being placed in front of the fan, then there will be some pressure drop across the fan. The air speed at the centre of the heatsink is 3.4m/s, measured by an anemometer when the fan is at rated power. Multiplying the air speed by the effective area of the heatsink gives a mass flow rate of 44.8m^3/h for a single fan, which is the operating point of the cooling system.

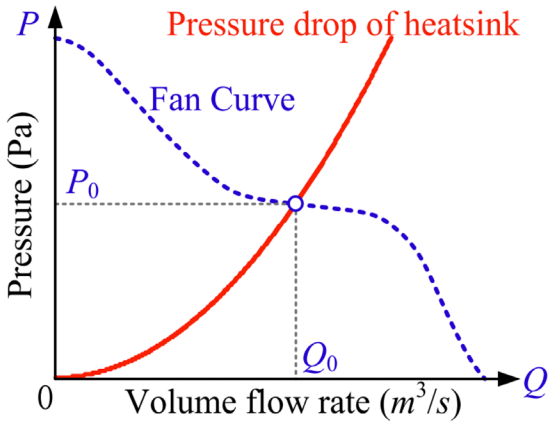


Fig.3-24 Heatsink operating point

Fig.3-25 shows a schematic of this cooling system, where heat is generated in the power module and then transferred to the heatsink via vertical heat transfer, The fan forces the air to flow, which greatly enhances the convection process, thus transferring the temperature from the heatsink to the environment faster.

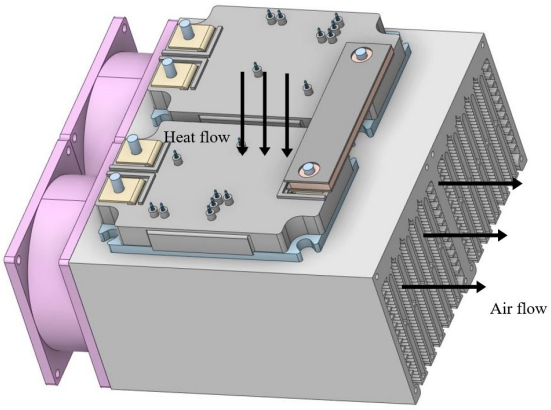


Fig.3-25 3D view of forced Air-cooled system

The subsequent measurements were taken at air speeds of 1, 3, 3.4 and 5m/s, respectively, when the power modules were connected in parallel using 5 MOSFETs, resulting in the temperatures on the different devices shown in Fig.3-26. Table 3-11 summarises the specific average temperature values for different devices at different air speeds. It shows that the temperature generated by the devices does not exceed the maximum device junction temperature (175℃) when the air speed is above 3m/s.

Table 3-11 Average temperature under different air speed

Air speed	Top/bottom MOSFETs	Middle MOSFETs	Diodes	Baseplate
1 m/s	226.1℃	246.3℃	211.3℃	224.2℃
3 m/s	150.1℃	169.9℃	141.1℃	147.8℃
3.4 m/s	144.3℃	161.2℃	134.2℃	142.7℃
5 m/s	129.5℃	149.5℃	114.1℃	127.5℃

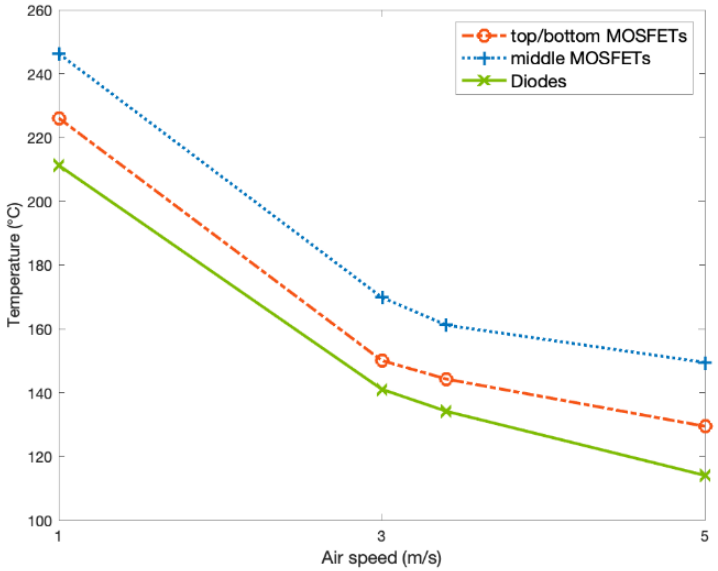


Fig.3-26 Device temperature at different air speeds

Fig.3-27 shows the air flow rates at different locations in the CFD simulation. By examining the flow rate in different areas, it is possible to determine which areas have better cooling effects. Understanding the distribution of flow rates aids in optimising the thermal design, such as adjusting the positions of fans, altering the size, or rearranging the layout of heat sinks. Fig.3-28 shows the heat transfer coefficient at different locations (distance along the x-axis) at different air speeds (Maximum power loss of 950W, inlet air flow ranges from 1m/s to 5m/s). Overall, higher air speeds significantly increase heat transfer efficiency, but heat transfer efficiency decreases with x-axis distance.

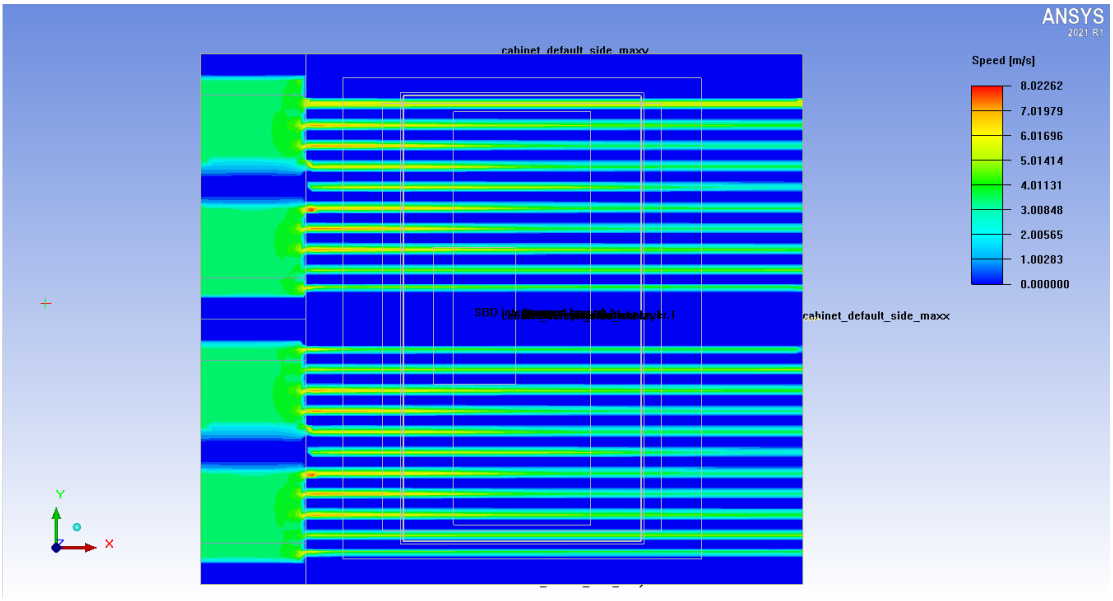


Fig.3-27 Air flow speed on the fans and fins of heatsink

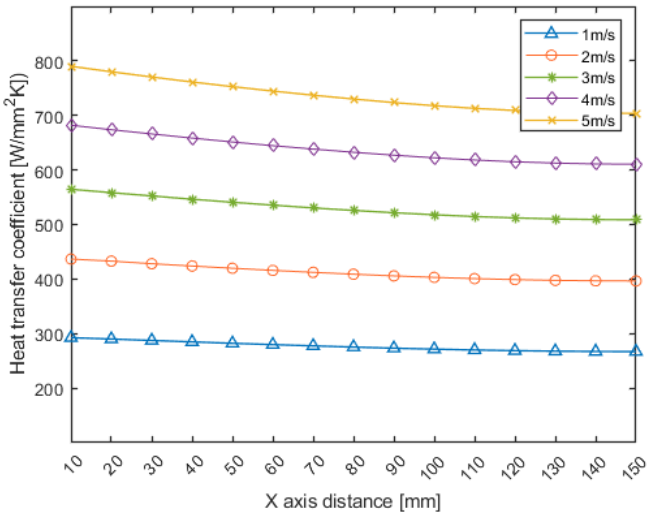


Fig.3-28 Comparison of heat transfer coefficient along the axial direction

3.5.4 Maximum Achievable Power with Forced Air Cooling

While liquid-cooled systems offer efficient heat dissipation, there are many challenges in aerospace applications, including increased system weight, reliability and maintenance complexity. In addition, in some cases, liquid-cooled systems may not comply with avionics standards and safety requirements, and therefore are not widely adopted in aircraft electronics [171]-[172]. Therefore, power density achievable with the air cooling, is evaluated in this section. Since CFD simulations are too slow and computationally demanding, especially when many heat sources are involved. Therefore, faster simulations with equivalent heat transfer coefficients were developed and used to quickly estimate the maximum power that may be achieved by the converter.

Forced air convection in a parallel plate finned heatsink, which is common in power electronics applications, is considered here. Applying the analytical model in [173], it is possible to establish a functional relationship between heat transfer coefficients and the axial distance for the heatsink as a function of the air mass flow rate, which varies from 4g/s to 7g/s. The ANSYS mechanical simulation results are obtained by setting the heat transfer coefficients to the top surface of heatsink as boundary conditions.

Table 3-12 summarise the temperatures of different devices at different air mass flow rate for different numbers of MOSFET paralleled. From this table, when only three MOSFETs are paralleled per switch, some devices reach temperatures exceeding 175°C, making them unsuitable for practical use. With four or five devices paralleled per switch, all power devices operate below 175°C, meeting operational standards. However, when four devices are paralleled, the maximum temperature of the middle MOSFET can reach up to 166°C. Therefore, considering a safety margin, paralleling five devices might be a more practical choice. According to the analysis of the converter power losses in Section 3.2, 99% efficiency can be achieved at the same time when choosing five devices in parallel. Table 3-13 shows the maximum power (one phase/leg) that can be achieved under different conditions at a fixed temperature of 125°C. Fig.3-29 shows that the more devices are connected in parallel and the faster the air flow rate, the higher the power can be achieved.

Table 3-12 Three MOSFETs per switch

Components	Temperature (°C)		
	4g/s	5g/s	7g/s
Top MOSFETs (3 in parallel)	197.4	188.9	177.9
Bottom MOSFETs (3 in parallel)	175.4	166.8	155.5
Middle MOSFETs (3 in parallel)	223.5	213.1	201.3
Top MOSFETs (4 in parallel)	152.7	146.1	136.9
Bottom MOSFETs (4 in parallel)	139.5	132.5	123.6
Middle MOSFETs (4 in parallel)	166.0	158.8	149.5
Top MOSFETs (5 in parallel)	124.4	118.4	110.6
Bottom MOSFETs (5 in parallel)	115.9	110.0	101.9
Middle MOSFETs (5 in parallel)	133.0	126.8	118.9

Table 3-13 Maximum power at different conditions (per phase)

Achievable power (kW)	4g/s	5g/s	7g/s
3 MOSFETs per switch	79.98	84.40	90.05
4 MOSFETs per switch	112.59	118.65	127.51
5 MOSFETs per switch	146.45	155.34	169.07

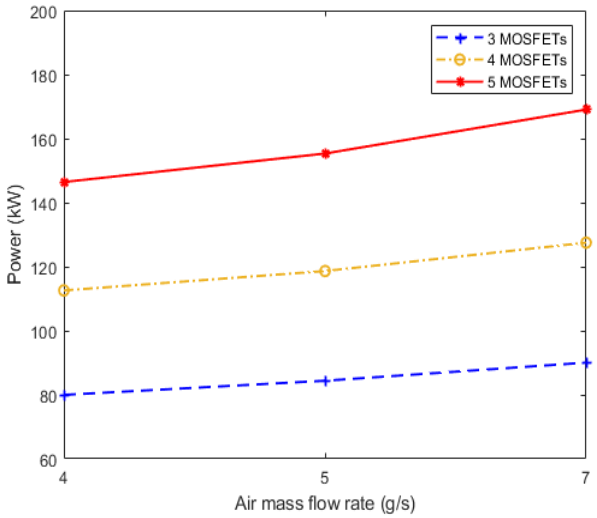


Fig.3-29 Achievable power (per phase) for different air flow rates and different devices in parallel

3.6 Conclusions

This chapter details the electrical analysis, design and construction process, and the thermal evaluation of a modular three-level SiC MOSFET power module. Based on loss simulation analyses under different conditions and coupling with thermal models, a full SiC power module was developed for building three-level NPC converter for aeronautic application. It contains five SiC MOSFETs in parallel per switch, suitable for a maximum DC-link voltage of 540V/1080V and current rating up to 400A. In the designed SiC power module, the DC+ and DC- power terminals are

located on the same side, and the AC power terminal is located on the other side. This design not only facilitates the connection to DC link capacitances, but also make it easy for paralleling and/or three phase converter arrangement. For one power module, there are an upper module and a bottom module, as makes it easy to replace and maintenance if one of them fails. This helps to increase reliability, and meanwhile reduces the cost. The module size is of 145 mm (l) × 108 mm (w) × 15.47 mm (h), and the weight is 448g (224g ×2). Considering a power rating capability of 432kW, the power density of the module is estimated to be 1.78 W/mm^3.

The electrical simulation conducted in this chapter provides a basis for understanding the performance of the three-level NPC converter. The NPC topology effectively reduces voltage stress on individual power switches, this is especially important considering the higher DC bus voltage requirements (540V/1080V) needed to meet the higher power demands of future aircraft. Using a Simulink model based on specific device datasheets, a detailed evaluation of switching and conduction losses was performed. The results found that paralleling more devices in one switch can reduce the losses per device, which is crucial for maintaining efficiency and reliability under high power conditions. The research elaborates on the adverse effects of parasitic inductance on module performance, including voltage overshoot during switching events. The study demonstrates that optimising the design to minimise loop inductance and enhance module layout symmetry can effectively mitigate these effects, thereby improving the reliability of the power module while balancing cost, manufacturability, and performance. The criteria and reasons for selecting power MOSFETs in power modules are introduced. By optimising the layout of the module, such as using a symmetrical design between the two sub-modules and arranging control loops perpendicular to the commutation loops, the parasitic inductance of the power module is minimised. The manufacturing process of the module is also provided.

Thermal analysis indicates that effective thermal management is crucial for maintaining the reliability and efficiency of power modules. In steady-state thermal simulations, when five devices are connected in parallel, all devices can operate within the safe margin even under worst-case conditions (175°C junction temperature, 80°C baseplate temperature). Using materials with better thermal properties, such as AlSiC, can significantly enhance reliability and reduce weight, although there might

be some trade-offs in thermal performance. To further assess the thermal performance of power devices, a single-pulse transient thermal analysis was conducted, revealing that the thermal resistance of the power MOSFET is approximately 0.11K/W. High-power switches typically handle large currents and voltages, generating significant heat. Low thermal resistance helps maintain lower operating temperatures and simplifies and improves the efficiency of thermal design. Moreover, CFD simulations evaluated the performance of the power module with a heatsink. The results show that the heatsink and fan used can only ensure the power devices operate within a safe margin when the air speed is above 3m/s. However, due to the significant computational requirements of CFD simulations, this section introduces a novel method based on the heat transfer coefficient to accurately estimate device temperatures at different air speeds. This method allows for quick estimation of the thermal performance of devices and can be used to predict the maximum achievable power of the module.

In summary, as more aircraft transition to electrification, it is necessary to advance power module technology to handle higher voltages and power levels more efficiently and reliably. By addressing these challenges, this chapter provides insights into developing advanced power modules that meet the strict requirements of the aviation industry, contributing to the goal of carbon neutrality and paving the way for a more sustainable future.

CHAPTER 4
Comprehensive Analysis of Three Phase Converter: Design, Construction, Measurement, and Electrical Performance

4.1 Introduction

This chapter focuses on the design, construction, parasitic measurements, and electrical performance of a three-level SiC power converter. The constructed converter suitable for high voltage and high power consists of the power modules introduced in Chapter 3 rather than semiconductor discrete devices. These converters are crucial in a variety of applications, including industrial motor drives, renewable energy systems, EVs, and aerospace. A key factor affecting the converter is the parasitic impedance during the commutation, which can lead to voltage overshoot, ringing, and increased switching losses. Parasitic inductance is unavoidable in converter circuits, typically originating from wiring, connectors, switching devices, and other components. Therefore, using appropriate parasitic inductance extraction methods is essential for evaluating the performance of the converter.

The construction of an NPC converter involves designing the busbar for connecting its external terminals, selecting appropriate heatsinks, and choosing DC capacitors of suitable size and performance, etc. This chapter first outlines the design of a three-level NPC converter, including the busbar design and the assembly process, from material selection to component integration. It describes the details of converter busbar design aimed at minimising parasitic inductance while ensuring robust physical support and uniform current distribution. Next, based on the converter's small-signal model, S-parameter measurements are conducted through a two-port network, and the method for extracting parasitic inductance is discussed in depth. These inductance values are critical for detailed DPT simulation models, ensuring that overshoot voltages and oscillation frequencies caused by parasitic inductance remain within safe operating limits. Furthermore, an experimental platform is established to verify and analyse the power converter's electrical performance. This practical evaluation combines theoretical design principles with real-world applications, providing a comprehensive understanding of the converter's dynamic characteristics.

In summary, this chapter not only discusses the design and assembly of a three-phase NPC converter but also emphasizes the importance of accurate inductance measurement techniques and performance evaluation. The significance of S-parameters at high frequencies and their role in accurately modelling the converter's dynamic behaviour is highlighted.

4.2 From Power Module to Three Phase Converter

4.2.1 Converter Busbar Design

The main purpose of the converter's busbar design is to minimise the size of the parasitic inductance, to provide reliable physical support and to ensure that the current density is distributed as evenly as possible, while the physical properties of the materials (e.g., breakdown voltage) need to be taken into account to select suitable conduction and insulation materials. The current mainstream designs are laminated busbar, the electrical connection is made by stacking copper layers together with isolation material layers such as PTFE, with suitable cut-outs. Papers [174]-[178] all follow this design methodology, as each kind of PM is designed in a different way so the design of the busbar will be slightly different, the busbar design for this 3L converter is shown below.

The design of the busbar was based on the following principles: the current should be distributed as evenly as possible, the parasitic inductance should be as small as possible, and the local temperature should not be too high. After considering factors such as space occupation, thermal effects, parasitic inductance, and manufacturing feasibility, the design shown in Fig.4-1 was chosen, it shows a side view of this converter with the corresponding electrical connections, the power modules used here are those presented in the previous chapter. Fig.4-2 shows the distribution of each layer of the busbars together with the DC capacitor, Fig.4-3 shows the cross section of busbars and DC capacitor, and Fig.4-4 shows the fabricated busbars.

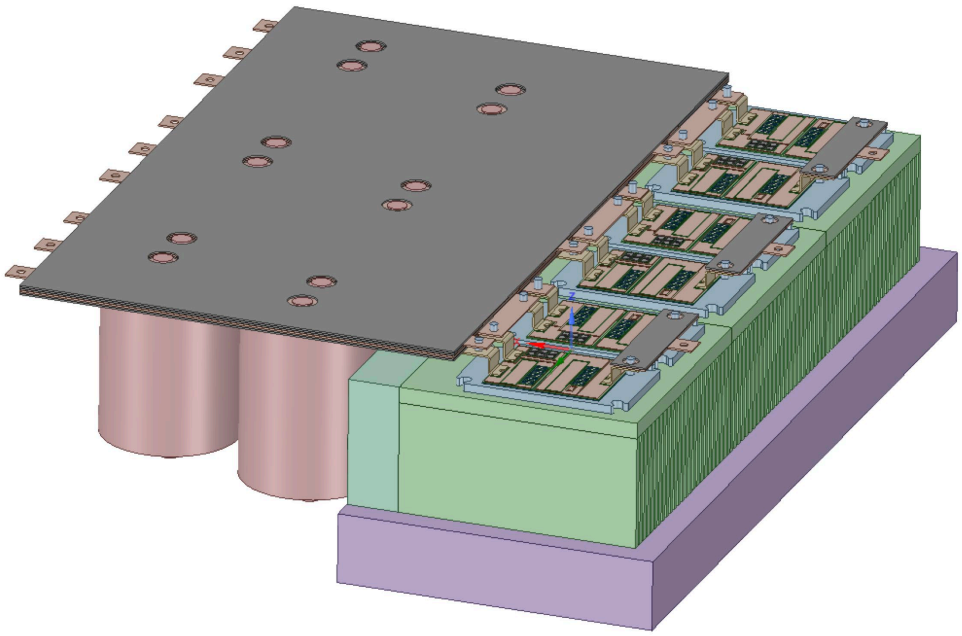


Fig.4-1 Converter busbar design and system integration

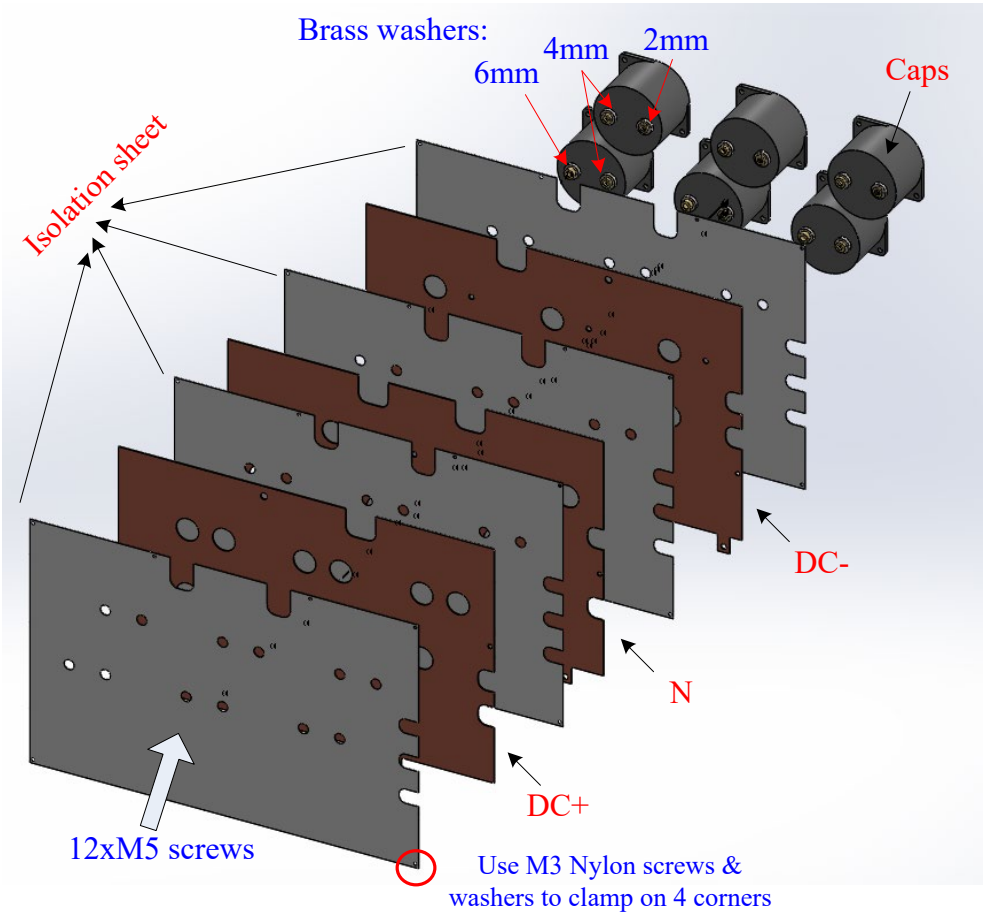


Fig.4-2 Layers of busbars

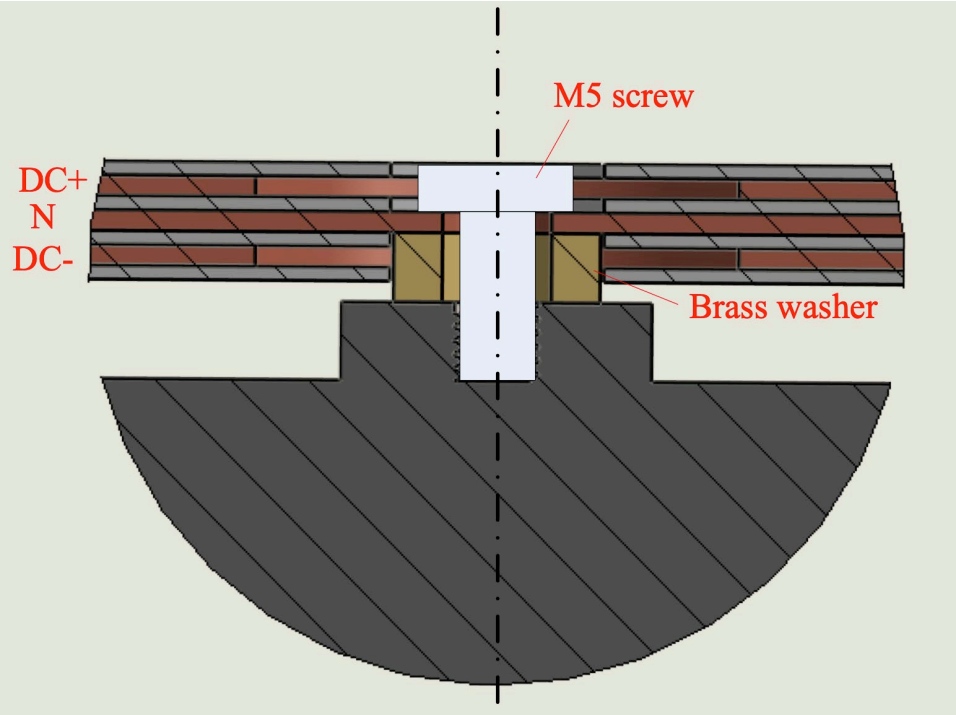


Fig.4-3 Cross section of busbars with securing screw

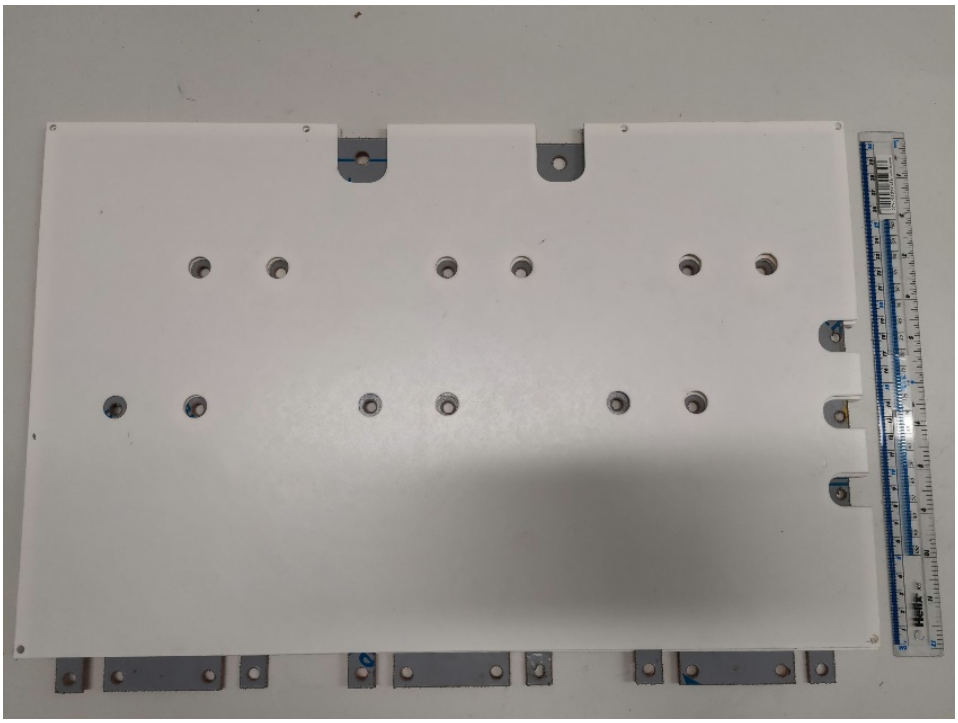


Fig.4-4 Fabricated busbars

Previous study [174] has shown that for rectangular copper plates the parasitic inductance can be calculated by the following analytical equation (4.1), where w, t, l, and d indicate width, thickness, and length of each conductor, and the distance between two conductors, respectively.

$$L_{self} = 0.2l \times \left[ln\left(\frac{2l}{w+t}\right) + 0.5 + 0.2235\left(\frac{w+t}{l}\right)\right] nH \quad (4.1)$$

According to equation (4.2), the primary approach for optimising the total parasitic inductance of a busbar focuses on reducing self-inductance and enhancing the mutual inductance. This optimisation is closely linked to the overlapping area and the spacing between different conductive layers. To enhance mutual inductance, a design with a larger overlap area and a reduced vertical distance between these conductive layers is advantageous. Additionally, such strong coupling between the layers offers enhanced resistance to external magnetic disturbances.

$$L_{total} = L_{self1} + L_{self2} - 2 \times L_{mutual} \quad (4.2)$$

Table 4-1 shows the self-inductance, mutual inductance, and total inductance in different loops, it can be seen that the loop inductance obtained using this busbar is nearly symmetrical. Fig.4-5 shows the current flow in different loops on the busbar, where the current direction of loop A is in red and that of loop B is in blue, the current commutation loops were introduced in Section 3.3. In addition to this, the possible effects of different thicknesses of insulation layer were investigated, Table 4-2 is the total inductance of Loop A and Loop B with different thicknesses of insulation layer, it shows an increase in the thickness of the insulation layer leads to an increase in the total inductance but the magnitude is small and within an acceptable range. Since this converter is intended for high voltage and high-power application, 1mm thickness of insulation layer is used to provide sufficient voltage withstanding capabilities, the use of 1mm thick insulation layer is usually based on a combination of ensuring electrical safety, meeting mechanical and thermal management requirements, and cost effectiveness.

Table 4-1 Loop inductances (self & mutual)

Loops	DC	NP	Mutual	Total
Loop A (Small loop)	34.10nH (DC+)	32.75nH	29.78nH	7.29nH
Loop B (Large loop)	62.18nH (DC-)	67.29nH	54.51nH	20.45nH
Loop C (Large loop)	34.22nH (DC+)	31.44nH	23.58nH	18.50nH
Loop D (Small loop)	62.40nH (DC-)	63.60nH	58.78nH	8.44nH

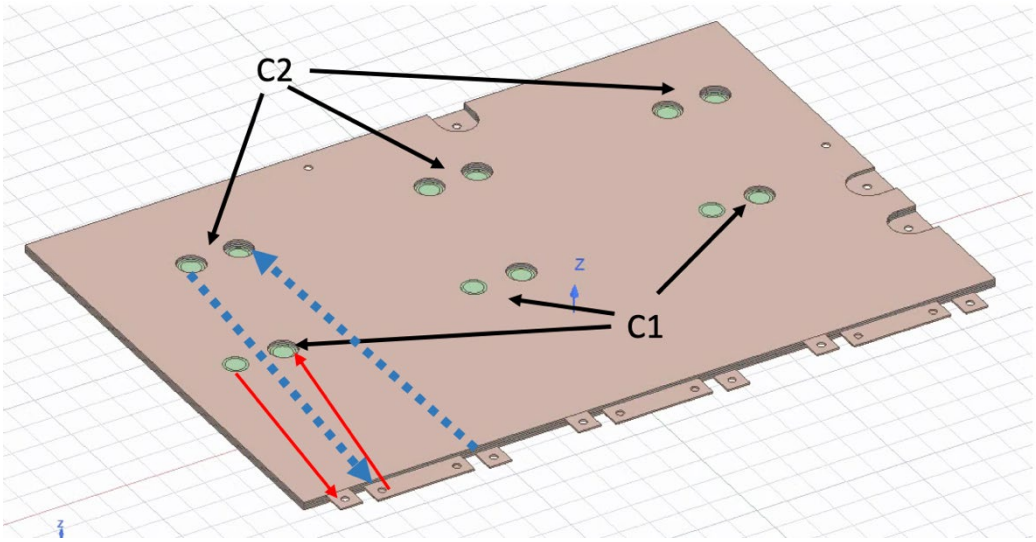


Fig.4-5 Current flow direction in different loops

Table 4-2 Loop inductances with different

Thickness of insulation layer	Total (Loop A)	Total (Loop B)
0.5mm	6.36nH	19.57nH
0.7mm	7.03nH	19.99nH
1.0mm	7.29nH	20.45nH

4.2.2 Three-Level SiC Converter Construction

The overall design of the module with housing is shown in Fig.4-6. It shows that AC terminals are on one side while DC and neutral terminals are on the other side. The plastic surrounding the auxiliary pins on the housings are provided for insulation as well as support for PCB gate drives boards. The six busbar terminals have the same dimension, the pins layout for both modules are also the same. Manufacturability considerations have been taken into account in the design of these substrates. The modules are optimised to be as compact as possible for higher power density and lower parasitic inductance.

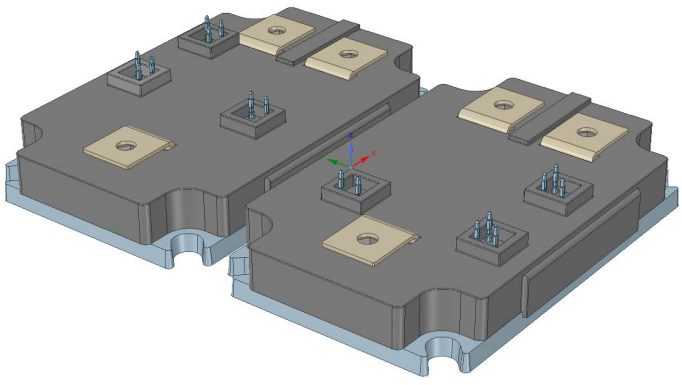


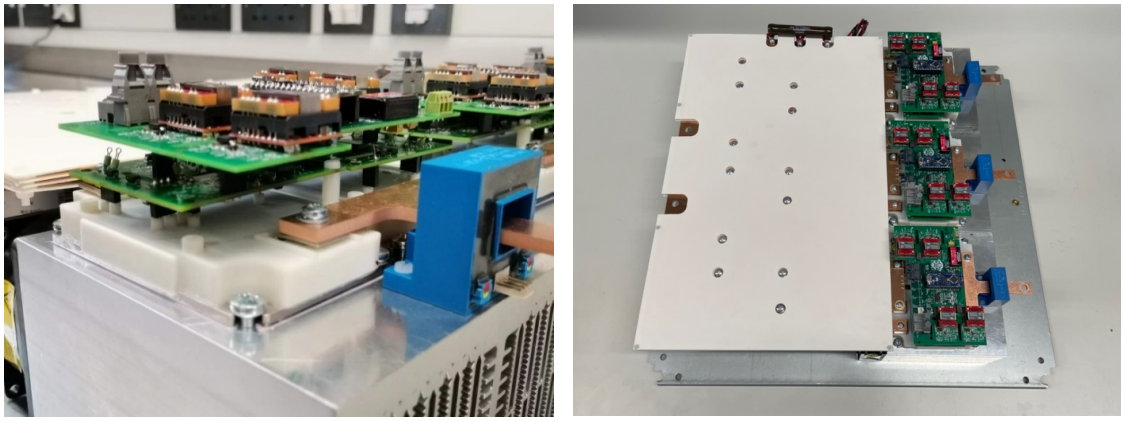
Fig.4-6 Overall module design with housings

The complete assembly of the three-level converter requires the following components: six DC capacitors TDK B25620, these capacitors are used to store and smooth the current and keep the power supply stable. A set of laminated DC busbars used for distributing power to modules. three T-shape AC busbars for three phase output connection. two voltage sensor boards monitor and regulate the voltage level of the system. three current transducers measure and control the current flowing through the converter, while two transducer signal regulating boards process and adjust signals from these sensors. To maintain a safe operational temperature within the converter, two sets of six cooling fans each are utilized for effective heat dissipation. The power module's switching operations are managed by three sets of gate drive boards, consisting of two sub gate drive boards and one master board. The essential components for power conversion are the three sets of power modules, each containing an upper and a bottom power module in a 3L phase leg configuration. Additionally, three heatsinks equipped with fans are placed beneath the power modules to enhance thermal management and prevent overheating damage.

In the process of assembling the converter, as shown in Fig.4-7, the DC capacitors and the spacer underneath then are first fixed in one side of the box, and the three heat sinks are fixed on the other side, Hall current sensors are mounted on the top surface of the heatsink to provide a convenient way to measure the current via the AC output busbars.

Fig.4-7 Capacitors, heatsinks, and sensors mounting

After that the power modules are mounted on the heatsinks, the TIM needs to be fixed between them to ensure secure mounting and good contact with the heat sink for effective heat dissipation. Next, DC capacitors are connected to the busbar to provide DC voltage snubbing and filtering, and then the power modules are screwed to the busbar, ensuring that all electrical connections are correct and secure. Afterwards the gate control boards are mounted on top of the power module to achieve precise control of the converter switching action, Fig.4-8(a) and Fig.4-8(b) show the photograph of one phase leg of the completed converter and the top view of the converter, Fig.4-9 shows the each busbar terminal in correspondence with the circuit topology.



(a) (b)

Fig.4-8 (a) Phase leg building block (b) Three level NPC converter

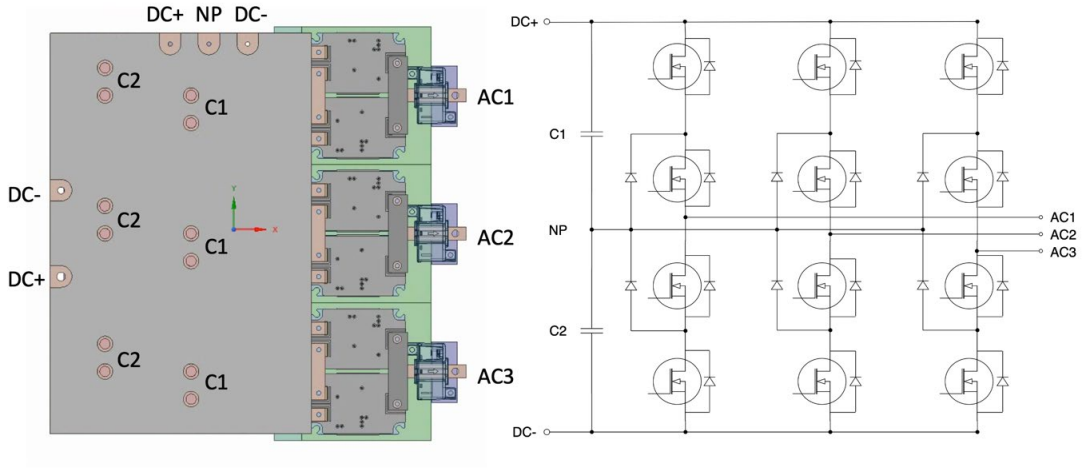


Fig.4-9 Converter top view and electrical connection

4.3 Parasitic Inductance Extraction of Three-Level NPC Power Module

This section delves into the theoretical foundations and practical applications of two-port networks, the emphasis is placed on the significance of S-parameters (Scattering parameters), which are crucial for describing the behaviour of electrical networks, particularly in high-frequency engineering scenarios. Additionally, this section explores a variety of methods and techniques for inductance extraction within the framework of two-port network theory. Previous studies have focused on extracting parasitic inductances of discrete MOSFET devices, as well as two level power modules with simple structures. Here, these methodologies are extended to the more complex three-level power modules, providing a deeper insight into their inductive characteristics and enhancing our understanding of these systems.

Second-order RLC series circuits are often used for parameter extraction and analysis, where the values of the circuit components RLC can be obtained by analysing the impedance curve. The impedance of each component added in series can be expressed by equation (4.3),

$$Z = Z_R + Z_L + Z_C = R + j\omega L_{eq} - \frac{1}{j\omega C_{eq}} \tag{4.3}$$

the resonant frequency defined as (4.4):

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \tag{4.4}$$

At low frequencies, the voltage drop across the capacitor predominates; at high frequencies, it shifts to the inductor; and at the resonant frequency, the voltage drop across the resistor becomes significant. The main contribution to the impedance in the low frequency range is the capacitance, in the high frequency range the impedance is dominated by the inductance, and at self-resonant frequency the voltages across V_L and V_C will be equal in magnitude but opposite in phase the impedance value is determined by the resistance.

This study uses a two-port network for frequency response analysis of the RLC circuit to obtain parasitic inductance values from impedance performance. Simplified

two-port network of MOSFET is shown in Fig.4-10. At low frequencies, the capacitor delta connection is converted to star connection and the contribution of capacitance at a low frequency (1 MHz) to the Z-parameters of the two-port network is specified in equations (4.5)-(4.8).

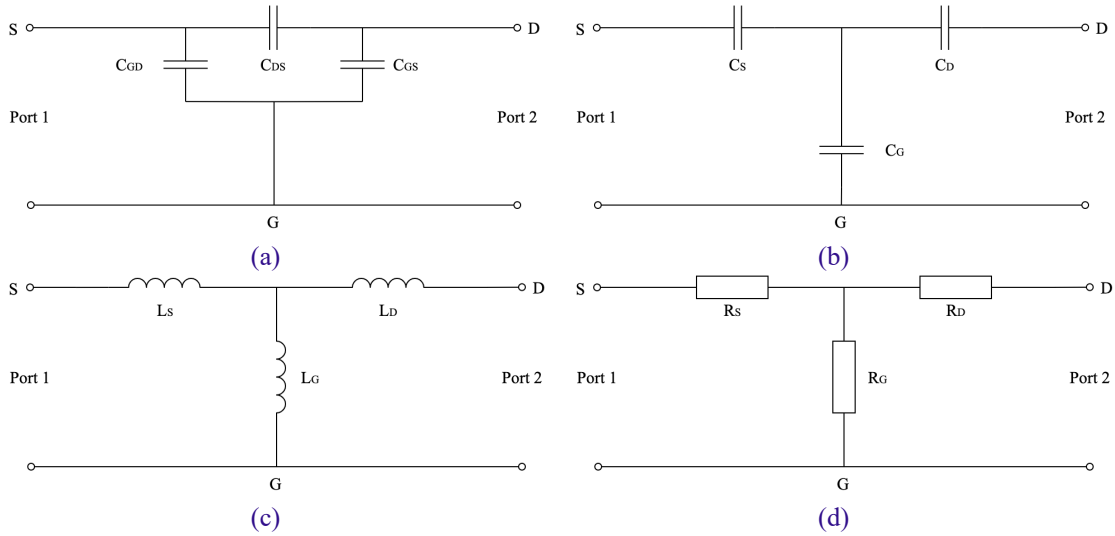


Fig.4-10 Two-port MOSFET network (a) at low freq for delta connection capacitance extraction (b) at low freq for star connection capacitance extraction (c) at high freq for inductance extraction (d) at self-resonant freq for resistance extraction

$$Z_{11(low\ frequency)} = \frac{V_1}{I_1|_{I_2=0}} = X_{C_S} + X_{C_G} = \frac{X_{C_{GS}}(X_{C_{DS}} + X_{C_{GD}})}{X_{C_{GS}} + X_{C_{GD}} + X_{C_{DS}}} \tag{4.5}$$

$$Z_{12(low\ frequency)} = \frac{V_1}{I_2|_{I_1=0}} = X_{C_G} = \frac{X_{C_{GS}} \cdot X_{C_{GD}}}{X_{C_{GS}} + X_{C_{GD}} + X_{C_{DS}}} \tag{4.6}$$

$$Z_{21(low\ frequency)} = \frac{V_2}{I_1|_{I_2=0}} = X_{C_G} = \frac{X_{C_{GS}} \cdot X_{C_{GD}}}{X_{C_{GS}} + X_{C_{GD}} + X_{C_{DS}}} \tag{4.7}$$

$$Z_{22(low\ frequency)} = \frac{V_2}{I_2|_{I_1=0}} = X_{C_D} + X_{C_G} = \frac{X_{C_{GD}}(X_{C_{DS}} + X_{C_{GS}})}{X_{C_{GS}} + X_{C_{GD}} + X_{C_{DS}}} \tag{4.8}$$

Fig.4-10(c) shows that the inductive impedance dominates at high frequencies, when the capacitance and resistance are neglected. For the two-port network, the Z-parameters are defined as (4.9)-(4.12):

$$Z_{11(high\ frequency)} = \frac{V_1}{I_1|_{I_2=0}} = X_{L_S} + X_{L_G} \tag{4.9}$$

$$Z_{12(high\ frequency)} = \frac{V_1}{I_2|_{I_1=0}} = X_{L_G} \tag{4.10}$$

$$Z_{21(high\ frequency)} = \frac{V_2}{I_1|_{I_2=0}} = X_{L_G} \tag{4.11}$$

$$Z_{22(high\ frequency)} = \frac{V_2}{I_2|_{I_1=0}} = X_{L_D} + X_{L_G} \tag{4.12}$$

At the self-resonant frequency, where both capacitance and inductance are negligible. For the two-port network, the Z-parameters can be defined as (4.13)-(4.16):

$$Z_{11(SRF)} = \frac{V_1}{I_1|_{I_2=0}} = X_{R_S} + X_{R_G} \tag{4.13}$$

$$Z_{12(SRF)} = \frac{V_1}{I_2|_{I_1=0}} = X_{R_G} \tag{4.14}$$

$$Z_{21(SRF)} = \frac{V_2}{I_1|_{I_2=0}} = X_{R_G} \tag{4.15}$$

$$Z_{22(SRF)} = \frac{V_2}{I_2|_{I_1=0}} = X_{R_D} + X_{R_G} \tag{4.16}$$

At high frequency (RF and microwave frequencies) direct measurement of Y (conductance), Z (impedance), or H (Hybrid) parameters are difficult for several reasons: unavailability of equipment to measure RF/microwave current and voltage; difficulty of obtaining perfect shorts/opens due to radiation effects; active devices may be unstable under open/short conditions. S-parameters, also known as scattering parameters, are an important set of parameters used to characterise the electrical properties of linear RF and microwave networks [179]-[180]. These parameters are primarily used to explain how these networks scatter or reflect energy. S-parameters are widely used in the field of network analysis and are particularly important when evaluating the performance of high-frequency electronic components such as antennas, filters, and amplifiers. While other parameters such as the Z and Y parameters can be used at lower frequencies, the S-parameters are preferred at microwave and RF frequencies because they are easier to measure under these conditions and are more directly related to measurable quantities such as power and phase shift. At high frequency it may be more practical to measure scattering parameters, a_1, a_2, b_1, b_2 are variables used to describe the transmission and reflection of signals in a two-port

network, these parameters represent the incident and reflected wave amplitude at the network ports, defined as (4.17):

$$b_1 = S_{11}a_1 + S_{12}a_2$$
$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{4.17}$$

This equation describes how the input signals (a_1 and a_2) are converted into output signals (b_1 and b_2) through the network. Here, S_{11}, S_{12}, S_{21}, S_{22} are the scattering parameters that describe the characteristics of the network, it can be obtained that:

$$S_{11} = \frac{b_1}{a_1|_{a_2=0}}$$
$$S_{21} = \frac{b_2}{a_1|_{a_2=0}}$$
$$S_{12} = \frac{b_1}{a_2|_{a_1=0}} \tag{4.18}$$
$$S_{22} = \frac{b_2}{a_2|_{a_1=0}}$$

This work uses VNA to measure the S-parameters for both two ports. The VNA allows the measurement of the S-parameters, so they need to be converted to Z-parameters before numerical analysis. [181] introduces equations and matrix transformations that facilitate the conversion between different types of parameters. It elaborates on the mathematical foundation for converting S parameters to other forms like Z, Y, H, ABCD, and the reverse, and provides detailed algebraic expressions that accommodate complex normalizing impedances. According to [181], for a standard two-port network, the conversion can be performed by (4.19)-(4.22), where Z_0 is the characteristic impedance (50Ω), In RF and microwave systems, especially coaxial cables and transmission lines, 50Ω is often used as the characteristic impedance. This is a compromise between the 30Ω (minimum attenuation) and 77Ω (maximum power handling) impedance standards. 50Ω characteristic impedance ensures high power handling while maintaining relatively low attenuation of the signal, making it suitable for a wide range of applications. In addition, it helps to reduce signal reflections and

ensure efficient signal transmission, which is especially critical in high-frequency applications.

$$Z_{11} = \left[\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}\right]Z_0 \tag{4.19}$$

$$Z_{12} = \left[\frac{2S_{12}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}\right]Z_0 \tag{4.20}$$

$$Z_{21} = \left[\frac{2S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}\right]Z_0 \tag{4.21}$$

$$Z_{22} = \left[\frac{(1+S_{22})(1-S_{11})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}\right]Z_0 \tag{4.22}$$

In conclusion, for the discrete device electrical model, the extraction of its parasitic parameters can be accomplished by the following steps. Firstly, the S-parameters of the device are measured in the frequency range of 100 kHz-40 MHz, and after that the S-parameters are converted to Z-parameters by (4.19)-(4.22). Accordingly, the parasitic parameters of the device can be obtained by calculating (4.5)-(4.16) at different frequencies.

For more complex models, e.g. three-level power modules, a further expansion on the above is required. The total loop inductances as calculated using Q3D in the previous chapter cannot be measured directly in a fully assembled module due to the presence of the MOSFET dies. In order to characterize the parasitics and validate the calculations for the purpose of developing accurate switching simulation models, a novel procedure based on the measurements of a number of equivalent two-port networks is proposed here. A typical two-port network is illustrated in Fig.4-11. In this model, the network is considered as a black box with two ports, each having a voltage and a current associated with it.

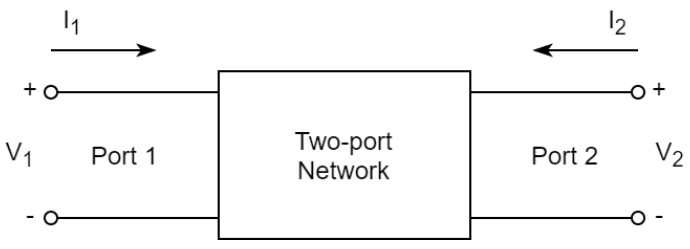


Fig.4-11 A general two-port network with current and voltage defined

Fig.4-12 shows the established small-signal circuit model of the NPC power module, which includes parasitic capacitance, resistance, and inductance. The small-signal model makes it possible to solve complex non-linear problems using simple linear algebra methods, which is particularly important in high-frequency electronic design. The power module can be characterized by the connection of several RLC branches, with capacitances C representing the input/output capacitances of the active devices, and RL representing the parasitic resistances and inductances of the interconnections. Fig.4-13 shows the internal structure of the power module, the connection points 1-18 identify the 18 external terminals of the power modules, they correspond to ports 1-18 in the small-signal model, respectively. DC, D, G, S, AC subscripts stand for parasitics of the DC branch connections, drain, gate, source kelvin terminals and AC output, respectively. Afterwards, this small-signal model needs to be transformed into a two-port network for S-parameters measurement, to fully obtain the parasitic inductances of the three-level power module, 16 different two-port networks need to be established, Table 4-3 shows the required port connections for each port and the extracted parameters under each case. Among these 16 different two-port networks, case 1 and case 16 can extract two desired parasitic inductances at the same time, while all other examples can only extract one desired inductance.

To conduct the parasitic parameter extraction, all S-parameters are first measured from 100 kHz to 40 MHz using VNA, and then converted to Z-parameters using Eqs. (4.19)-(4.22), and finally the desired parasitic inductance values are obtained using (4.9)-(4.12). Fig.4-14 shows the two-port network of simplified equivalent circuit diagram of case 1, in this case, terminals 1 and 2 forming port 1, terminals 3-18 are joined together with terminal 2 to form port 2. It can be seen that in this case, not only LG1 connected to ground can be extracted, but also LDC+ can be extracted because the circuit connected to Port 1 is not a lumped network. However, the components connected to port 2 is a lumped network which is not required. Thus, in this case, two parasitic inductances can be effectively extracted. Similarly, case16 can also extract two parasitic inductances. Besides these two cases, two different lumped networks are produced, making it impossible to accurately determine the specific parasitic parameter values of each part. Therefore, only the parasitic parameters connected to ground can be effectively extracted.

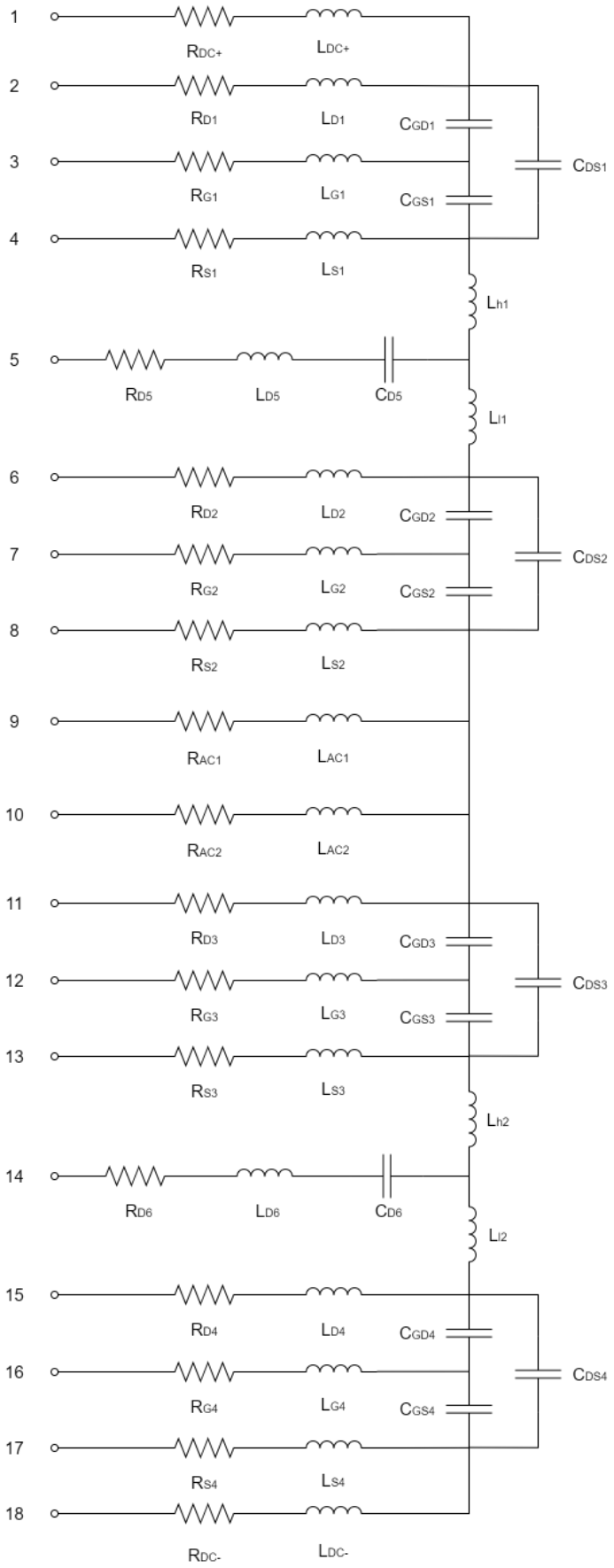


Fig.4-12 Small signal circuit model of NPC power module

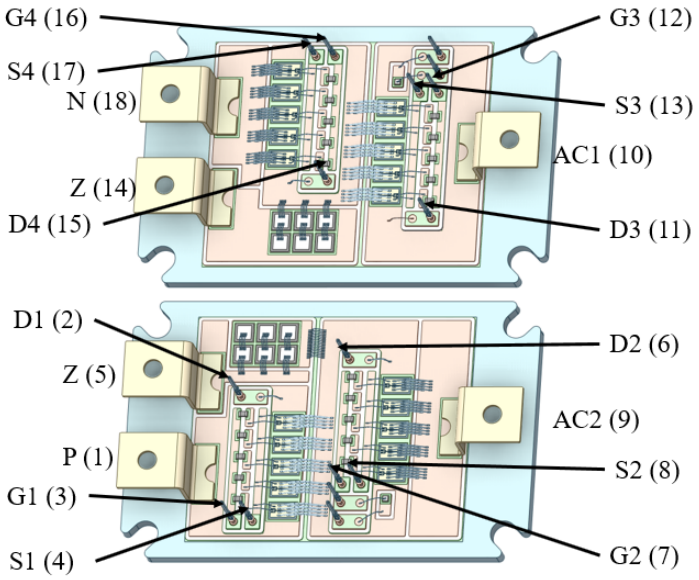


Fig.4-13 Accessible connection pins and terminals

Table 4-3 Different case configuration

	Port 1 (terminal)	Port 2 (terminal)	Ground (terminal)	Extracted inductance
Case 1	1	3-18	2	LDC+,LD1
Case 2	1-2	4-18	3	LG1
Case 3	1-3	5-18	4	LS1
Case 4	1-4	6-18	5	LD5
Case 5	1-5	7-18	6	LD2
Case 6	1-6	8-18	7	LG2
Case 7	1-7	9-18	8	LS2
Case 8	1-8	10-18	9	LAC1
Case 9	1-9	11-18	10	LAC2
Case10	1-10	12-18	11	LD3
Case11	1-11	13-18	12	LG3
Case12	1-12	14-18	13	LS3
Case13	1-13	15-18	14	LD6
Case14	1-14	16-18	15	LD4
Case15	1-15	17-18	16	LG4
Case16	1-16	18	17	LDC-,LS4

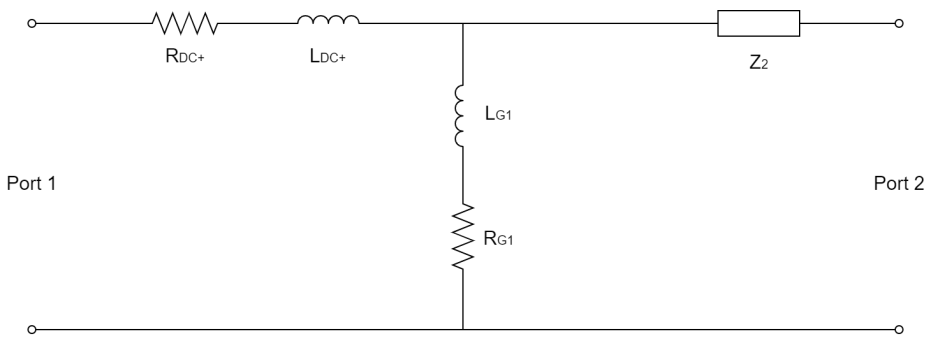


Fig.4-14 Simplified small signal circuit for case 1

All parasitic parameters in the model can theoretically be extracted by this method. In this work more attention is paid to the device's switching characteristics, and only the parasitic inductance is extracted.

4.4 Experiment Verifications

In this section, the practical evaluation of the theoretical models and methods discussed earlier will be explored, with a particular focus on the extraction of parasitic inductance and the evaluation of three-level power modules using double-pulse testing. These experiments are crucial for confirming the accuracy and applicability of theoretical analyses and for ensuring that established models can withstand practical application.

4.4.1 Parasitic inductance extraction

The power module is experimentally characterized with a Siglent SVA1000X VNA over a frequency range of 100 kHz to 40 MHz. Using the VNA allows to see how the component network is working in a certain frequency range. The DUT is connected to the VNA where inject a signal from one port and simultaneously measures the signal reflected back to this port and the signal emerging from the other ports. To ensure the accuracy of the measurement, the phase and amplitude of the obtained signal should not have significant errors. The interconnecting cable that connects the VNA to the DUT can cause phase shifts that lead to errors in the measurement, this work uses a two-port 'Short-Open-Load-Thru' calibration to eliminate the effects caused by the cable. A customized PCB board suitable for the module interface shown in Fig.4-15 was designed to connect the VNA to the power module, a 50 Ω coaxial BNC connector is utilized for impedance matching [182]. To remove the influence of the PCB board, an additional PCB compensation board corresponding to each of the 16

cases is designed. These decoupling PCBs allow for the measurement of the PCB parasitics to decouple the inherent characteristics of the DUT from the interconnection PCB, by data post-processing.

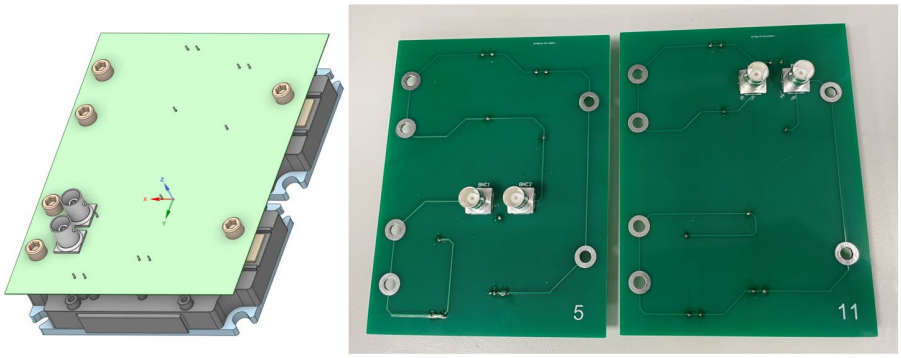


Fig.4-15 Customised PCBs for testing

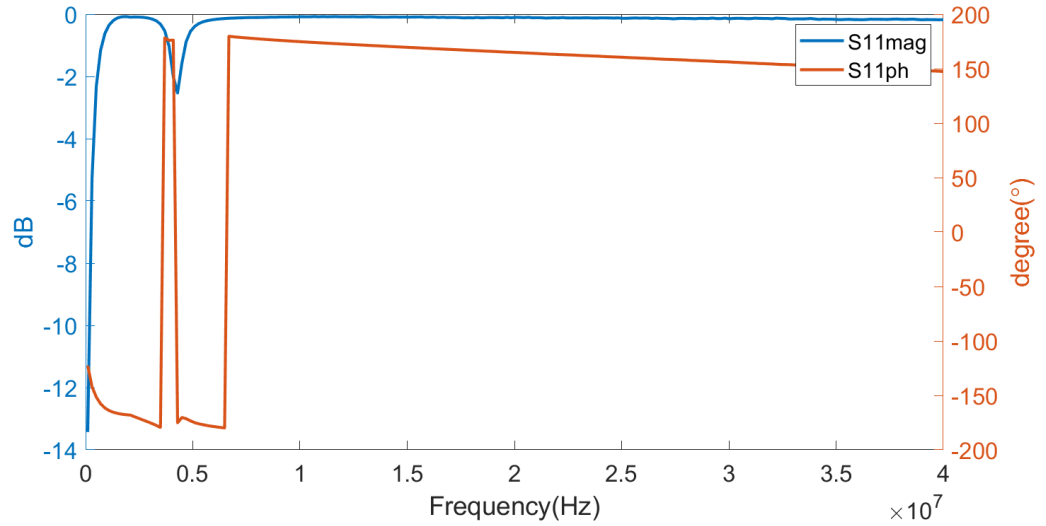
Since the two-port network is a symmetric reciprocal network, S12 and S21 as well as Z12 and Z21 should be equal, and from the results obtained also provide the proof. Fig.4-16 shows the S-parameters obtained from VNA for case 4, the blue curve shows the amplitude of the S-parameter in decibels (dB) and the orange curve is the phase of the S-parameter in degrees (°). Fig.4-17 shows the Z-parameters calculated by S-parameter conversion, in case 4 only one inductance LD5 can be extracted as other parts of two-port network are lumped, so only the inductance value obtained from Z12 and Z21 is valid here. The parasitic capacitance causes a decrease in the impedance magnitude at frequencies below the self-resonant frequency and can be determined from the negative slope. Similarly, the parasitic inductance can be calculated from the positive slope at frequencies above the self-resonant frequency. The slope of the impedance magnitude can be derived from equation (4.3).

$$Z' = L_{eq} - \frac{1}{\omega^2 C_{eq}} \tag{4.22}$$

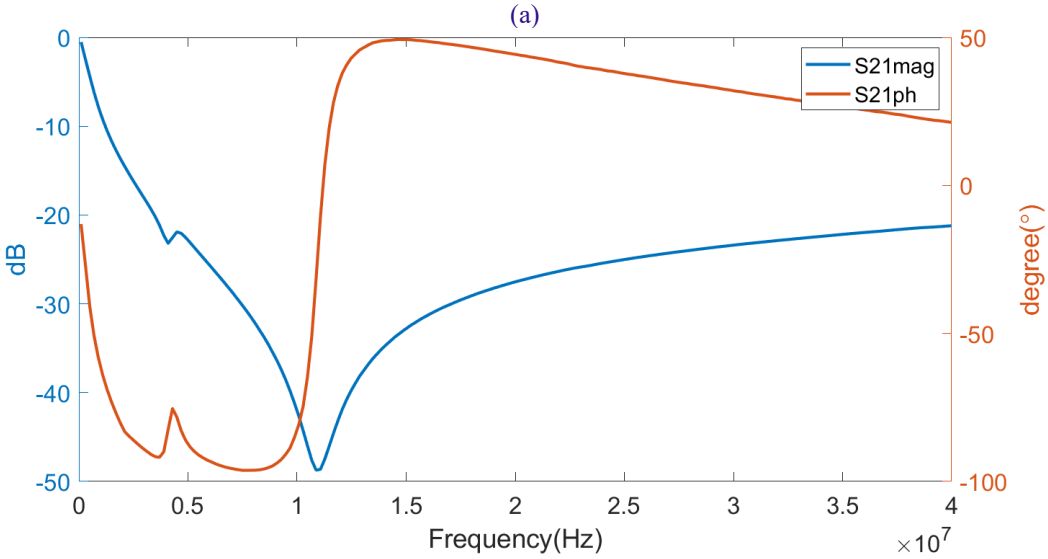
When frequency is much higher than self-resonant frequency, means:

$$Z'_{high\ freq} = L_{eq} - \frac{1}{\omega^2 C_{eq}} \approx L_{eq} \tag{4.23}$$

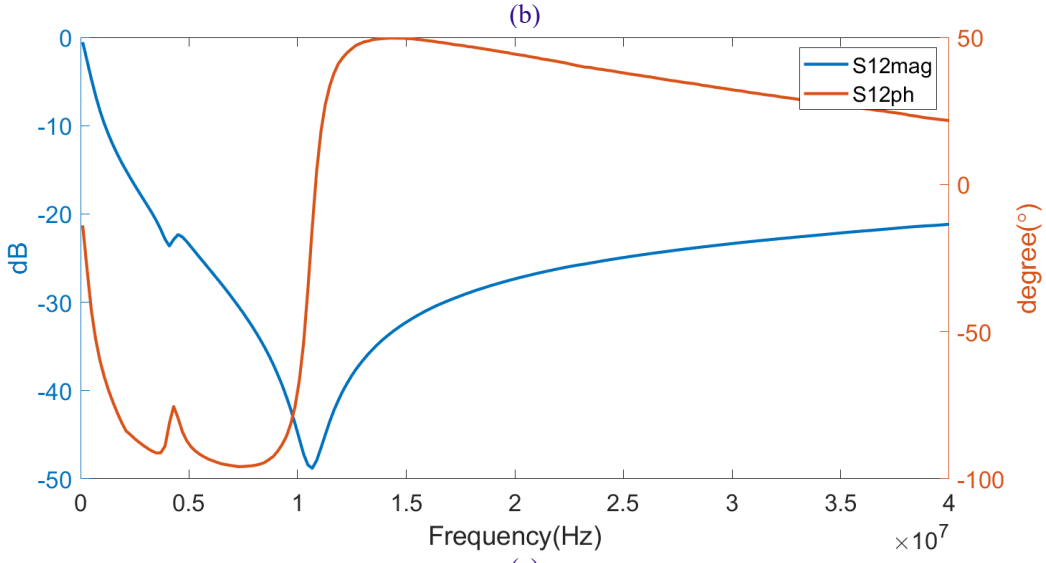
Therefore, the parasitic inductance can be obtained by calculating the slope of the Z-parameters at high frequencies. To save space, the experimental results of only one case are shown here.


S11mag
S11ph
dB
degree(°)
Frequency(Hz)
×10^7

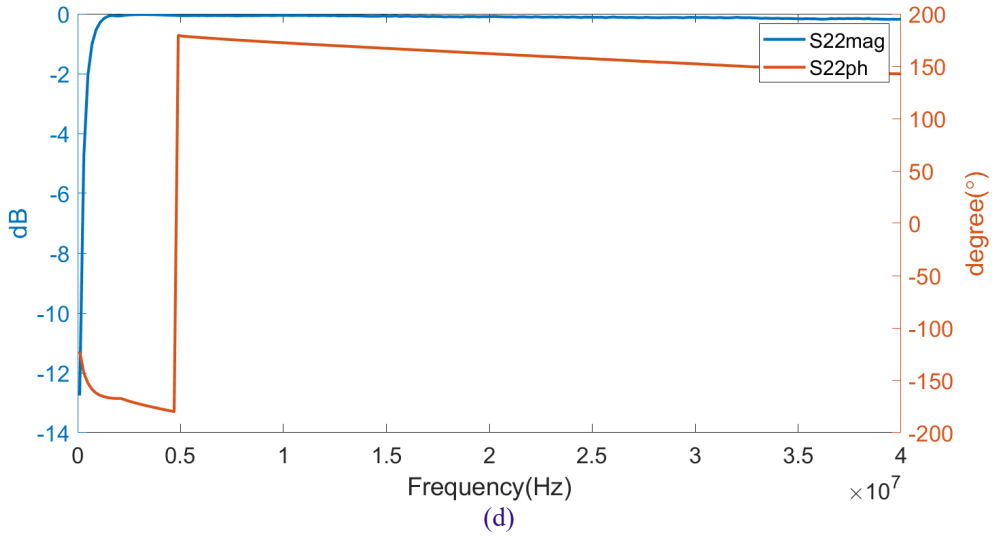
(a)


S21mag
S21ph
dB
degree(°)
Frequency(Hz)
×10^7

(b)

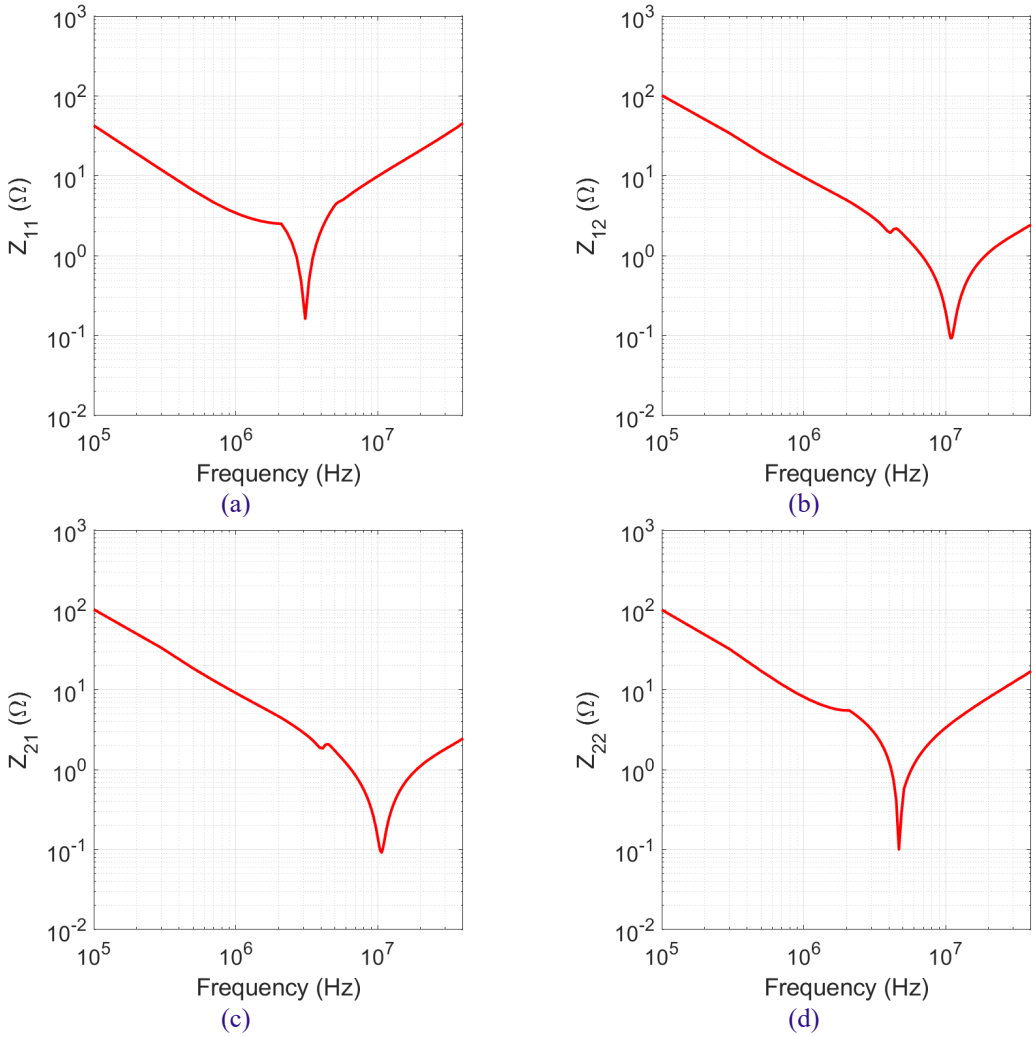

S12mag
S12ph
dB
degree(°)
Frequency(Hz)
×10^7

(c)



(d)

Fig.4-16 Measured S-parameters of case 4 of SiC power module. (a)S11 (b)S21 (c) S12 (d)S22



(a) (b) (c) (d)

Fig.4-17 Z-parameters calculated by S-parameter conversion of case 4 (a) Z11 (b)Z12 (c) Z21 (d)Z22

By measuring each of the 16 cases using VNA and converting the obtained S-parameters to Z-parameters, the value of parasitic inductances in each part of the power module can be obtained. Table 4-4 summarises all the results obtained and

compares these values with those obtained from ANSYS Q3D simulation, indicating a difference of less than 10%.

Table 4-4 Simulated & measured partial inductance

Parasitic inductance (nH)	Simulated(Q3D)	Measured	%difference
D1 (T1 MOSFET)	20.61	22.49	8.7%
G1 (T1 MOSFET)	22.64	20.97	7.6%
S1 (T1 MOSFET)	20.71	20.53	0.9%
D2 (T2 MOSFET)	20.74	20.78	0.2%
G2 (T2 MOSFET)	21.92	19.94	9.5%
S2 (T2 MOSFET)	20.72	21.28	2.7%
D3 (T3 MOSFET)	21.27	23.11	8.3%
G3 (T3 MOSFET)	22.64	23.31	2.9%
S3 (T3 MOSFET)	20.67	20.72	0.2%
D4 (T4 MOSFET)	20.62	21.88	5.9%
G4 (T4 MOSFET)	22.59	22.95	1.6%
S4 (T4 MOSFET)	20.72	21.08	1.7%
DC+	9.58	10.16	5.9%
DC-	7.75	8.25	6.3%
AC1	7.72	8.46	9.1%
AC2	9.11	9.74	6.7%
D5 (Clamping diode)	11.82	10.99	7.3%
D6 (Clamping diode)	11.89	12.87	7.9%

4.4.2 Double-Pulse Test of Three-Level Power Module

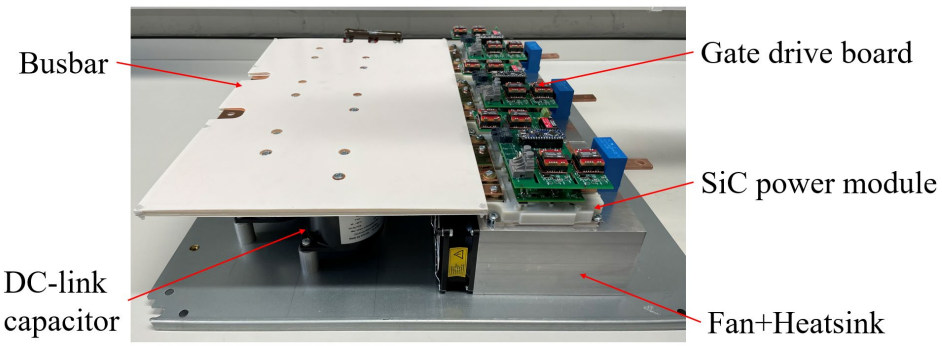
The DPTs are performed separately to validate the switching characteristics under the two types of commutation modes. The Double-Pulse Test is a standard method used to evaluate the dynamic performance of power modules, particularly useful for testing power switches and other components under rapid switching conditions. This section outlines the experimental setup, describes the simulation model and interprets the results to evaluate the performance attributes of the power converter under test.

To characterize the switching behaviour of the SiC converter and measure the over-voltage seen by the devices under the worst-case scenario, DPTs were performed on a 1080V DC-bus using the setup shown in Fig.4-18(a) with the converter platform,

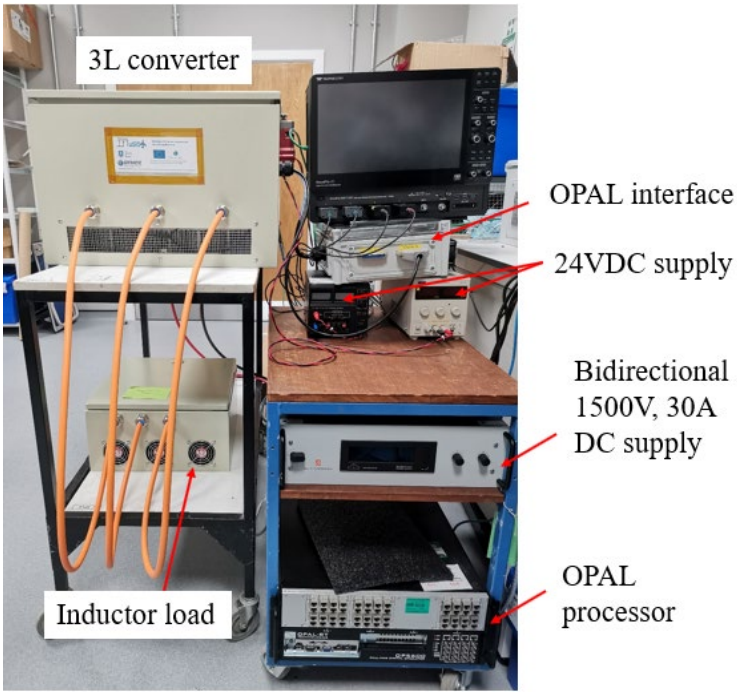
including laminated DC busbars, DC-link capacitors, gate drive board, SiC power modules, and air cooling heatsinks. Costumed gate drives were designed in order to drive the large gate current and provide the required protection functions. Fig.4-18(b) shows the built test platform, where the experimental equipment used is listed in Table 4-5. In this configuration, the OPAL simulator enables the coupling of high-speed FPGA-based models, such as converters and power electronics drivers, with relatively slower power and motor system models on the CPU, resulting in finer-grained real-time simulation. A 24V DC power supply provides power to the drive control circuit of power modules. a Bidirectional 1500V, 30A DC Supply provides the voltage input to the three-level three phase converter. The rig is based on a three-phase converter designed for demonstration purposes. An air-core load inductor was sized to provide up to 440A at turn off and was alternatively connected to each of the three-phase of the converter to characterize each phase separately. For the sake of brevity, only results for one of the switching is reported here.

Table 4-5 Test equipments

Item	Manufacturer	Model
Power module	Dynex	-
SiC MOSFET die	Wolfspeed	CPM3-1200-0013A
SiC Diode die	Wolfspeed	CPW5-1200-Z050B
Load inductor	-	25uH, 47mΩ
Differential probe	TELEDYNE	HVD3220
Digital simulator	OPAL-RT	OP5600
Oscilloscope	TELEDYNE	WavePro 404HD
Power supply	Delta Elektronika	SM1500-CP-30



(a)



(b)

Fig.4-18 (a)Built 3-phase 3-L NPC converter (b)Test platform

The gate driver is a critical component used to control semiconductor switches. Conducting functional tests ensures that the gate driver can correctly respond to control signals, effectively switching on and off the semiconductor switches. Functional testing can help detect any faults in the circuit, such as connection issues, component damage, or design errors. By performing these tests before the DPTs, it is possible to prevent more severe circuit damage that could occur under high-voltage and high-current conditions during testing. The gate drive functional test was carried out first as shown in Fig.4-19, in this test, a built-up model is used to make the gate driver board simulate a MOSFET device through Digital simulator OP5600. A MOSFET with characteristics including a gate-source capacitance (C_{gs}) of 40uF and a gate resistance (R_g) of 2.2Ω was selected to simulate the parameters of a three-level power module, which has a C_{gs} of 37.7uF and an R_g of 2.2Ω. This selection aims to model scenarios involving the fastest switching speeds. Fig.4-20 shows the functional test results, when DUT is T1, T1 receives a double-pulse signal while T2 remains continuously on, and T3 and T4 are kept off. When DUT is T2, T2 receives a double-pulse signal, T3 remains continuously on, and both T1 and T4 are off. For T3 as the DUT, it receives a double-pulse signal, T2 stays continuously on, and T1 and T4 are off. When T4 is the DUT, it receives a double-pulse signal, T3 stays on continuously,

and T1 and T2 are off. The specific current loops for DPT of different devices have been presented in Fig.3-7.

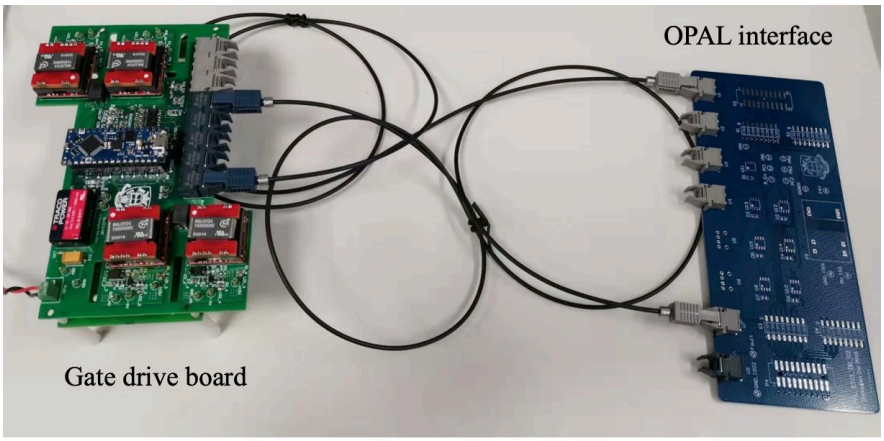


Fig.4-19 Gate drive functional test

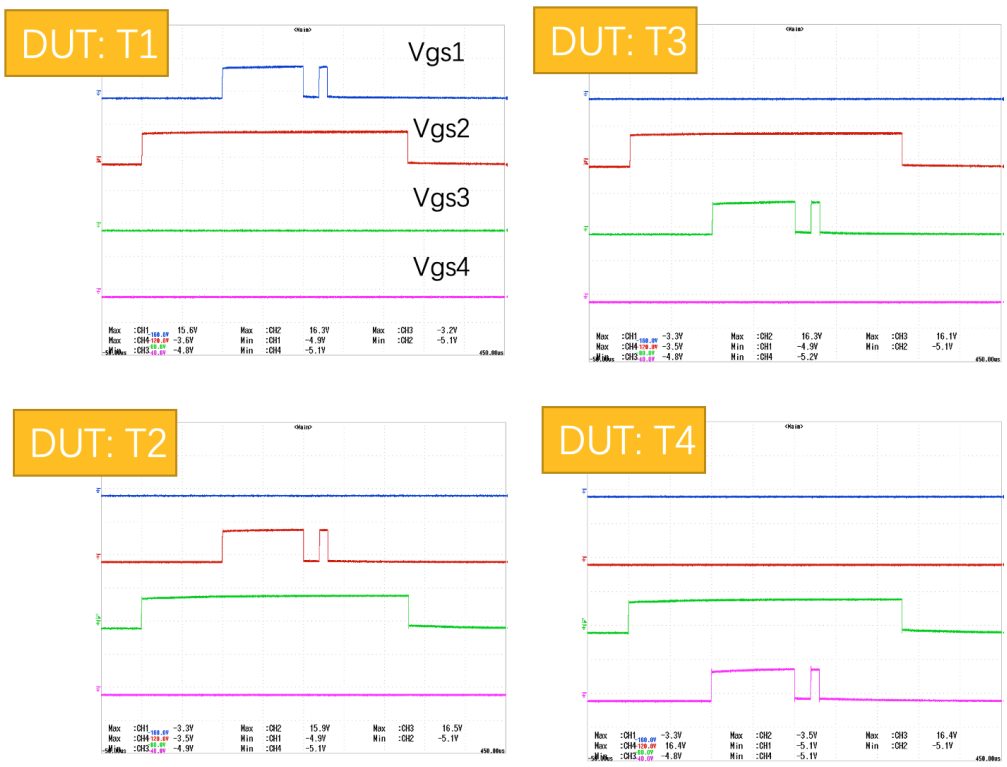


Fig.4-20 DPT test with capacitor load (*time: 50us/div, voltages: 20V/div*)

By establishing simulation models and comparing them with experimental results, the accuracy of theoretical analyses can be verified. This helps to confirm whether the model assumptions and theoretical derivations are effective and whether the theoretical model can accurately predict the behaviour of actual power systems. Simulation models provide a platform to assess the impact of design changes without

the need for actual construction and testing. Different configurations, materials, or components can be tried in the model and the impact of changes can be quickly accessed to optimise the design and reduce cost and time. To compare with experimental results, detailed three-level converter model in Matlab/Simulink is developed for precise circuit simulation, as shown in Fig.4-21. This model includes power switches from T1 to T4 and clamping diodes, which are modelled as Simscape components based on SPICE parameters, enabling accurate simulation of real device performance. Additionally, the model includes a DC power supply and DC capacitors, all extracted parasitic inductances, a double-pulse signal for the T1 device, and measurements of the power module output signal.

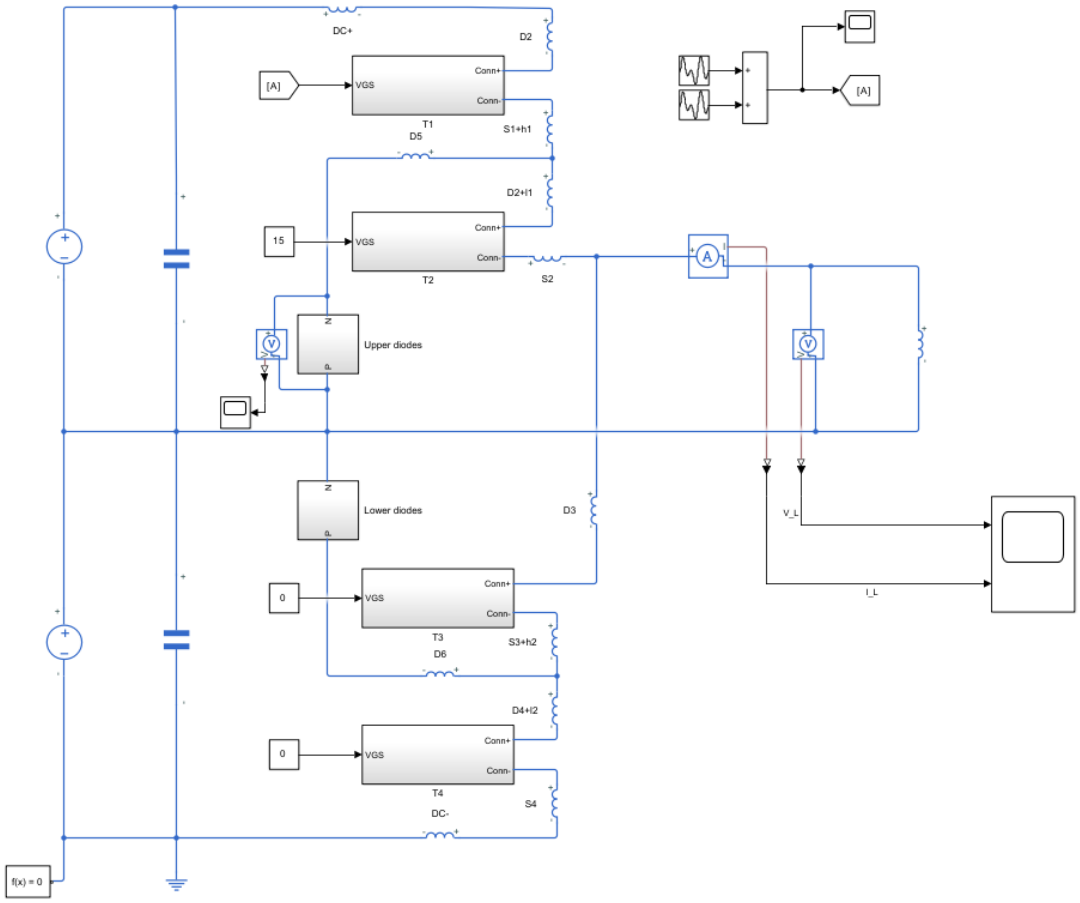
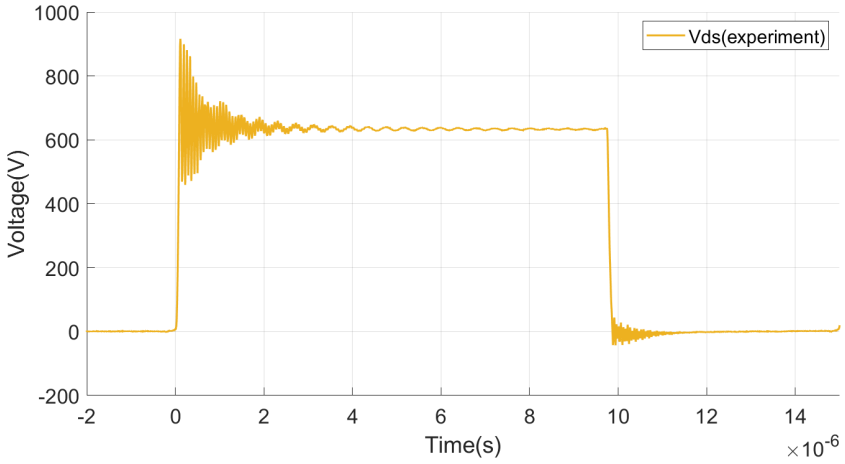


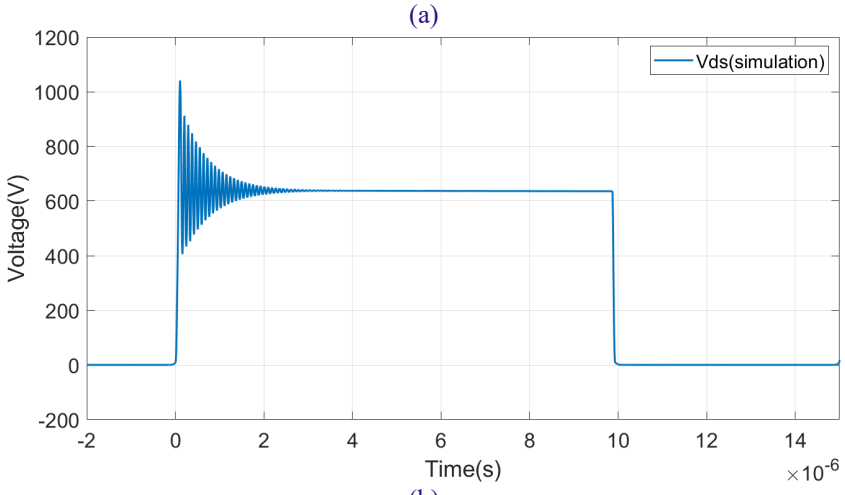
Fig.4-21 DPT Simulink model for power switch T1

Fig.4-22 shows the experimental switching characteristics of the DUT T2 compared with the simulated characteristics when the DC voltage is 1080V and the current is 200A. Fig.4-22(a) and Fig.4-22(b) respectively display the experimental and simulated V_{ds} waveforms. Due to the effects of parasitic inductance and parasitic capacitance within the MOSFET structure, an LC oscillation circuit is formed. After

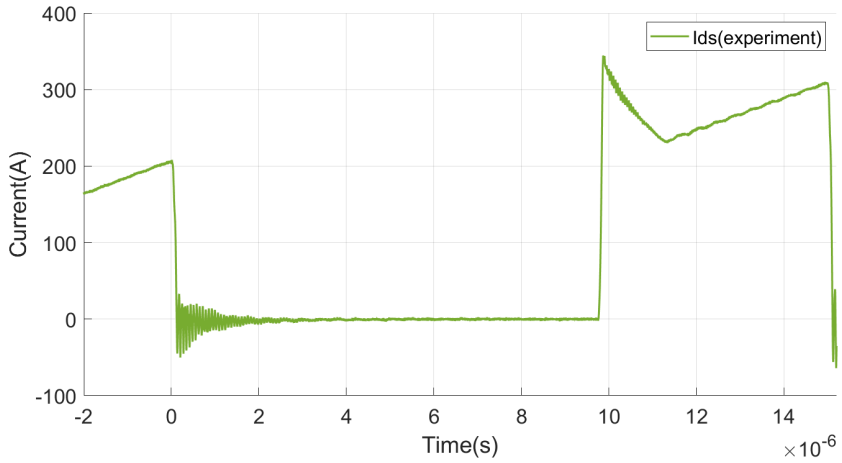
the DUT T2 is switched off, the V_{ds} voltage rapidly rises and produces oscillations until it stabilizes. Fig.4-22(c) and Fig.4-22(d) show the experimental and simulated waveforms, respectively. Oscillations were observed when the I_{ds} dropped to zero after the MOSFET switched off. The high dV/dt and dI/dt during the switching transients of the SiC MOSFET, along with parasitic components in the circuit, are responsible for these oscillations. Due to the reverse recovery of diodes, this reverse recovery current can reach high peak values in a very short time, especially in high-speed switching applications. When the MOSFET turns on, the high peak reverse recovery current combines with the MOSFET's forward current, creating a spike in the current waveform.



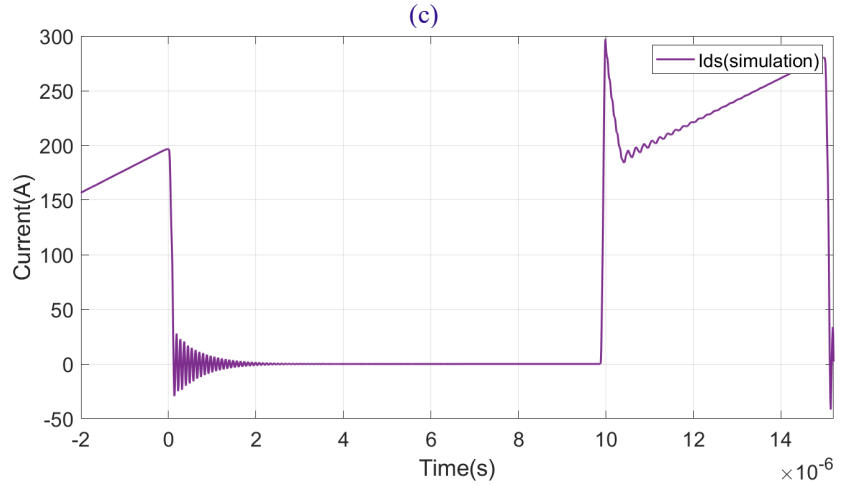
(a)



(b)



(c)



(d)

Fig.4-22 Switching waveforms (a)Measured Vds (b)Simulated Vds (c)Measured Ids (d)Simulated Ids. (1080V DC, 200A DUT: T2)

Table 4-6 summarises the oscillation frequency and maximum voltage obtained in the DPTs for the active devices T1-T4, comparing measured and simulated results. According to this table, for T2 and T3 devices, the maximum voltage obtained from the simulation is higher than that observed in the experiment. The comparison of I_{ds} results from Fig.4-22(c) and Fig.4-22(d) shows that when T2 and T3 devices are switched on, the simulation model yields a higher reverse recovery current and higher di/dt, leading to a greater maximum voltage in the simulation results. The reverse recovery effect is more obvious during the DPTs of T2 and T3, which is why the differences between experimental and simulation results are not significant in the DPTs of T1 and T4. This may be due to the difference between the electrical model of the clamping diodes and the actual diodes. However, even under worst-case scenarios, according to the datasheet, the maximum voltage produced by the power devices T1-T4 remains below the device's maximum safe operating voltage of 1200V.

Table 4-6 Test results

	Oscillation frequency (MHz)	Maximum voltage (V)
T1(experiment)	15.8	807
T1(simulation)	15.6	812
T2(experiment)	12.7	920
T2(simulation)	11.2	1020
T3(experiment)	13.0	960
T3(simulation)	11.5	1063
T4(experiment)	16.4	779
T4(simulation)	17.2	785

Furthermore, the behaviour of the devices was compared for different DC bus voltages and load currents, Fig.4-23 shows the maximum V_{ds} value for T2 from experiment results, and Fig.4-24 shows the corresponding overshoot voltage. The difference between the maximum overshoot voltages at different DC bus voltages is less significant. As the load current increases, the overshoot voltage increases in all cases. In all cases the over-voltage is within the expected safety margin.

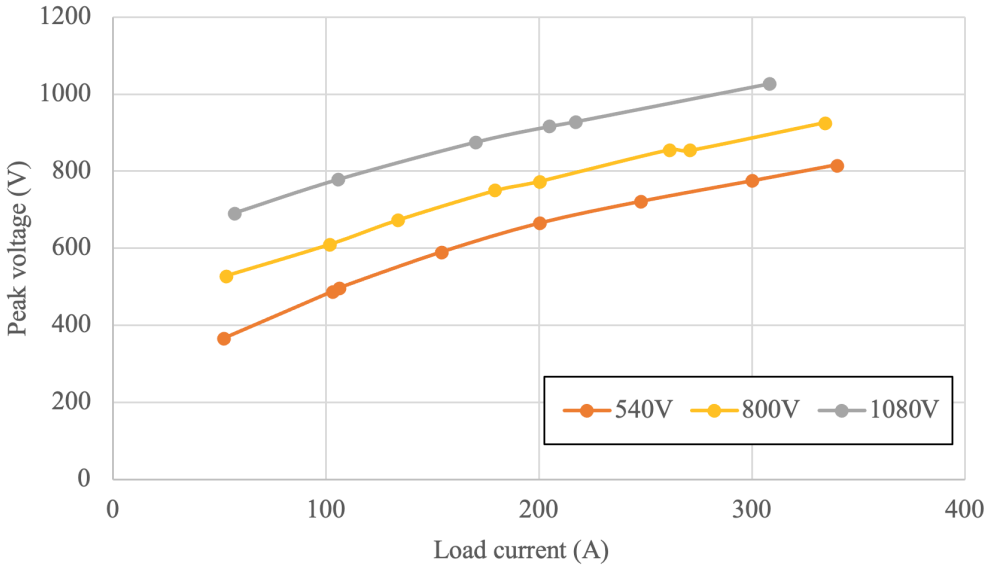


Fig.4-23 Peak voltage of Vds

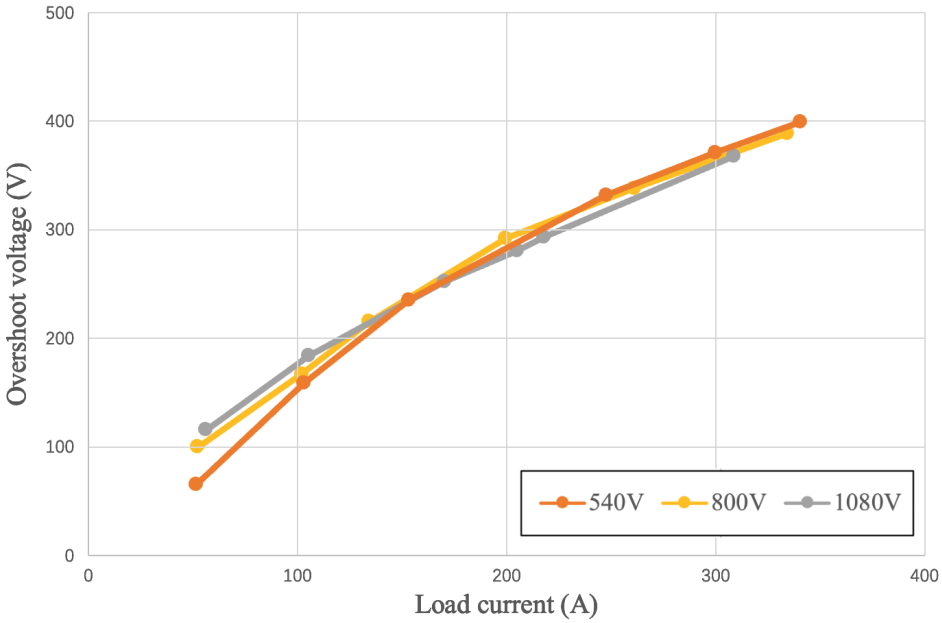
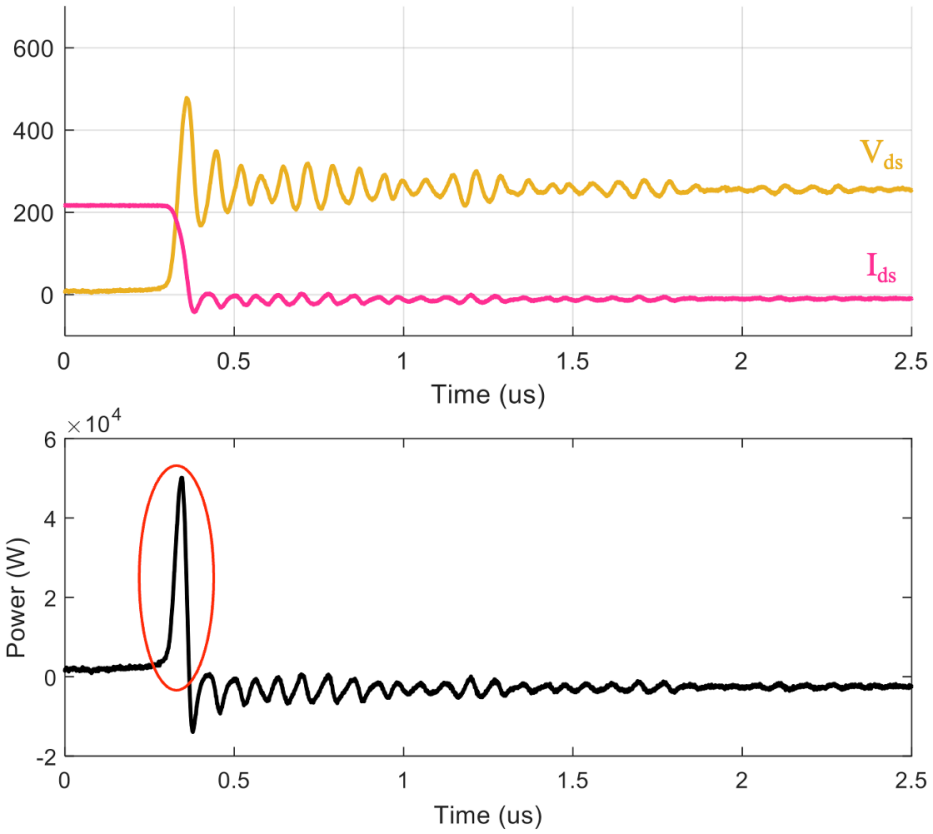


Fig.4-24 Overshoot voltage of Vds

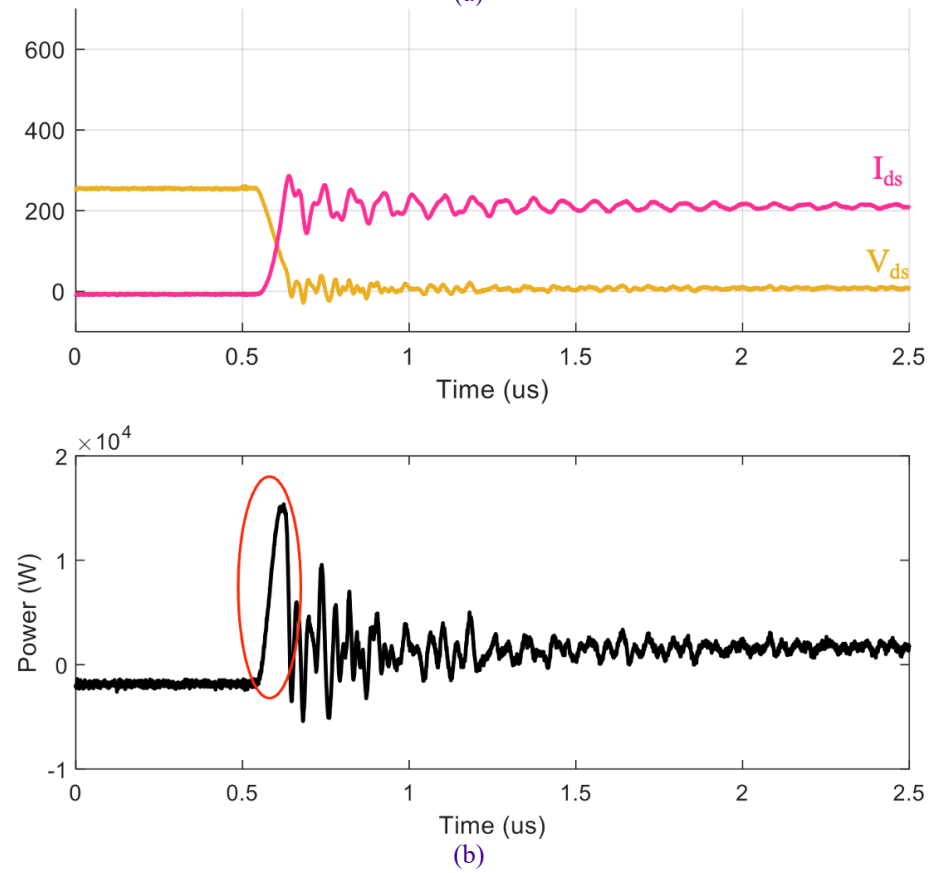
The switching losses of MOSFET power devices can be obtained by integrating the instantaneous power loss during the switching period, and this step is implemented through a MATLAB program. Fig.4-25 shows the V_{ds} (yellow) and I_{ds} (pink) from DPT experiment results, and the resulting power curve (black) for the device turn-off and turn-on transient. Using the same loss calculation method, the Table 4-7 summarises the turn-on and turn-off losses generated by the switching devices when the DC voltage is 800V output current is 300A and the DC voltage is 1080V output current is 200A for two cases.

Table 4-7 Device switching losses

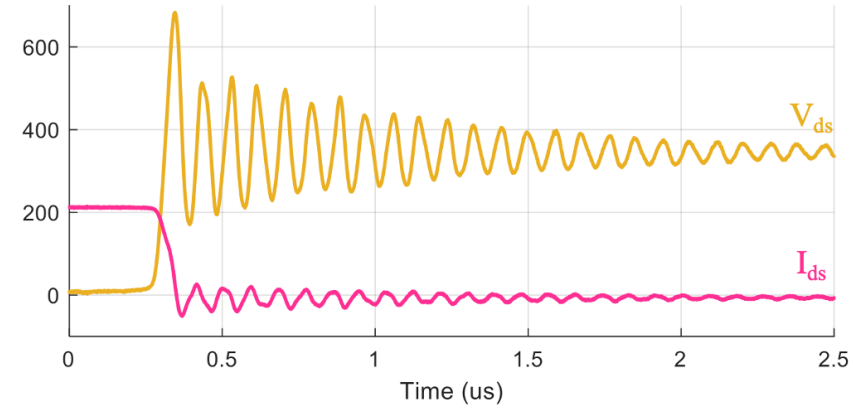
Devices	800V/300A		1080V/200A	
	Turn-on	Turn-off	Turn-on	Turn-off
T1	1.6mJ	4.5mJ	2.6mJ	3.9mJ
T2	1.3mJ	5.3mJ	1.7mJ	4.3mJ
T3	1.4mJ	4.6mJ	1.3mJ	4.0mJ
T4	1.5mJ	3.3mJ	2.9mJ	3.4mJ

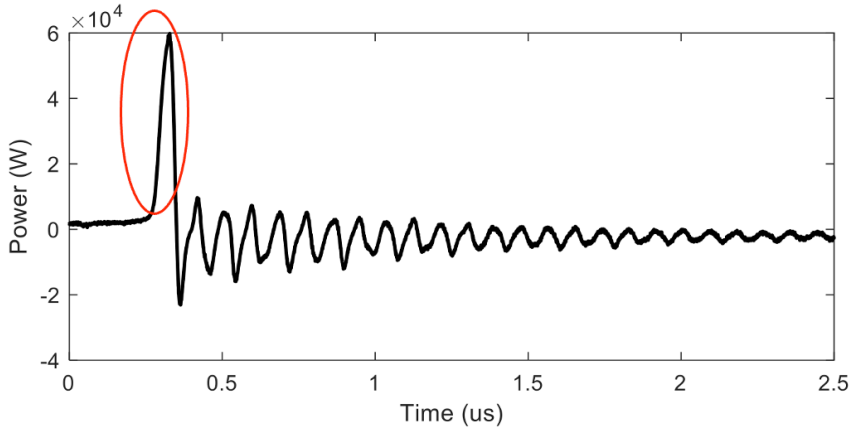

600
400
200
0
V_{ds}
I_{ds}
0
0.5
1
1.5
2
2.5
Time (us)
$\times 10^4$
6
4
2
0
-2
Power (W)
0
0.5
1
1.5
2
2.5
Time (us)

(a)


600
400
200
0
I_{ds}
V_{ds}
0
0.5
1
1.5
2
2.5
Time (us)
$\times 10^4$
2
1
0
-1
Power (W)
0
0.5
1
1.5
2
2.5
Time (us)

(b)





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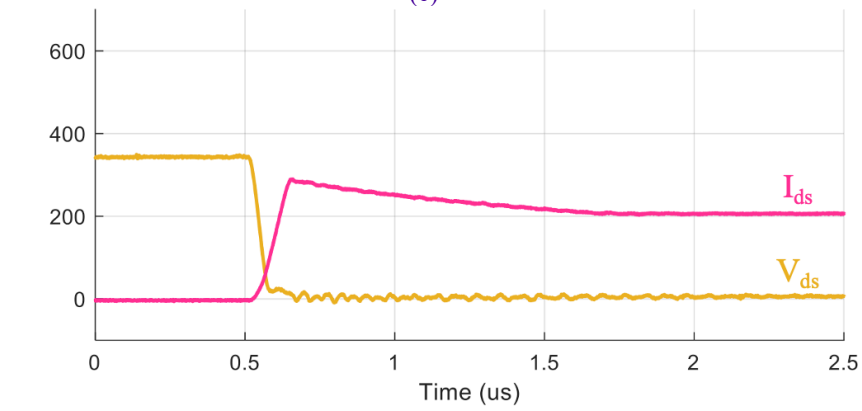
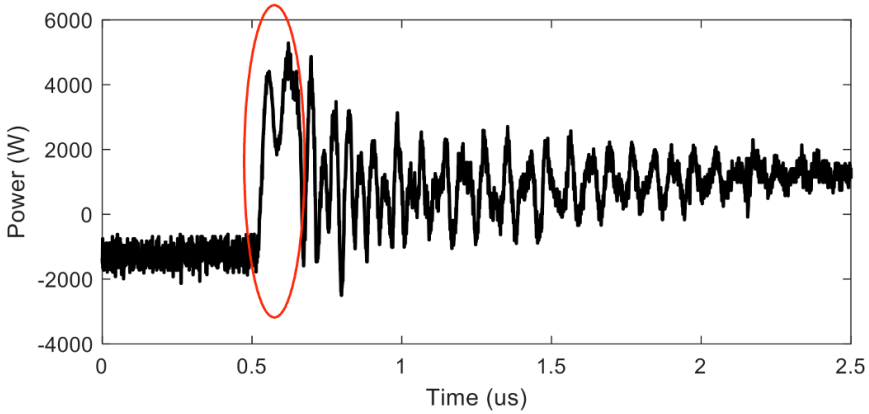




(d)

Fig.4-25 Switching transients for (a)outer switch T4 turn off (b)outer switch T4 turn on (c) inner switch T2 turn off (d) inner switch T2 turn on

4.5 Conclusions

This chapter delves deeply into the intricate design, construction, measurement, and electrical performance evaluation of a three-level SiC power converter. Initially, the converter's laminated DC busbars were designed by stacking copper layers with isolation material layers to optimise performance and reduce inductance. Subsequently, the construction of the three-phase three-level converter was completed using the power modules designed in Chapter 3.

The chapter then introduces a method for extracting parasitic parameters based on S-parameters through a two-port network. By establishing a small-signal model of the converter, 16 two-port networks were created, and the corresponding S-parameters were measured from VNA, and Z-parameters were obtained by converting S-parameters. Experimental validation was conducted using custom-designed PCBs corresponding to each case. The results demonstrated that the parasitic inductance values extracted by the VNA had an error within 10% of the Q3D simulated values, showcasing the method's effectiveness in accurately measuring parasitic inductances in complex multi-port power modules.

Furthermore, a converter testing platform was established, and extensive DPTs were conducted to verify and analyse the electrical performance of the power converter. This chapter synthesizes the results of theoretical analysis and experimental testing of the three-level converter. The close correlation between simulation predictions and experimental results confirms the accuracy of the theoretical models and underscores the importance of proper inductance measurement techniques.

In summary, this chapter completes the design and assembly of the three-phase converter from the power module, highlighting the role of high-frequency S-parameters in extracting parasitic parameters and accurately simulating the converter's dynamic behaviour. This approach ultimately enhances the design and functionality of high-performance power converters.

CHAPTER 5
Conclusions and Future Work

5.1 Conclusion

In this thesis, a scalable compact SiC-based power module and corresponding high-power converter have been developed and optimised. This converter operates at 540V/1080V DC bus voltage with a per-phase output power of 100 kW, focusing on applications such as aircraft starter-generator systems, electric vehicle motor drives, renewable energy systems, and industrial motor drives. During this process, the advantages of multi-level converters and their suitable application scenarios are discussed, along with an analysis of electrical and thermal behaviours, including a method for quickly estimating the temperature of power devices. Furthermore, a partial parasitic inductance extraction method for this complex multi-level module is proposed, supported by extensive experimental results to validate the presented concepts.

This work compares two-level and three-level converters, analysing the design principles of different topologies and their performance under varying junction temperatures and gate resistances. The research developed precise PLECS models for NPC, ANPC, and T-type three-level converters and explored how key factors such as voltage stress, switching losses, conduction losses, and THD impact converter performance. Unlike previous studies focusing on IGBT and Si MOSFETs, this work emphasizes the performance of third-generation semiconductor SiC MOSFETs in high-voltage applications, especially in aircraft starter-generator systems. The experimental results show that three-level converters are more effective in minimising losses and THD, particularly in high-power environments, thereby enhancing efficiency and power quality. T-type converters perform best in terms of power losses, while ANPC excels in THD performance; however, practical applications still require a balanced consideration of device voltage stress, cost, and size. Overall, three-level converters offer higher efficiency and lower harmonics in high-power applications compared to two-level converters, though they introduce additional complexity and cost. Detailed simulations validate the advantages of three-level converters in

reducing losses and improving power quality, and recommendations are provided for selecting appropriate topologies and devices for different application scenarios.

The current three-level power modules on the market typically achieve their design by connecting multiple two-level modules, but this approach introduces additional parasitic inductance that negatively impacts performance. This work proposes a power module based on a three-level NPC topology suitable for 540V/1080V DC bus voltages. By optimising the layout and parallel configuration of MOSFETs, the module achieves efficient operation under extreme conditions while maintaining temperature within safe limits. The design minimises parasitic inductance in the commutation loop, reducing the risk of voltage overshoot and device damage, and incorporates a baseplate material better suited for aerospace applications. To address the high computational load of CFD simulations, an equivalent heat transfer coefficient method is introduced, allowing for rapid temperature estimation and determining maximum output power under varying airflow conditions, thereby assessing the module's output power scalability. In summary, for safety and cost-effectiveness considerations, the NPC topology was selected based on the specific application, effectively reducing voltage stress without the need for additional clamping power devices. The appropriate number of parallel power MOSFETs was chosen to meet application requirements based on the electrical and thermal performance of the power module under worst-case conditions. The internal structure of the module was optimised considering the loop inductance. This work addresses key challenges in developing advanced power modules for more efficient and reliable aircraft electrification, thereby supporting the sustainable development of the aviation industry.

Measuring partial parasitic inductance in power modules without damaging their structure has always been a challenge, especially in multi-level topologies where the increased number of components and complex internal wiring make the equivalent circuit model more complicated. This work focuses on a three-level NPC topology, establishing a two-port network small-signal model. S-parameters were measured using a VNA and converted into Z-parameters for analysis, showing less than 10% error compared to Q3D simulation values. The extracted parasitic parameters were then applied to the DPT simulation model, and a testing platform was used to validate the switching characteristics and overall performance of the three-level converter. The

consistency between simulation and experimental results confirmed the model's accuracy and highlighted the importance of precise inductance measurement.

5.2 Future Work

The thesis introduces a detailed design process for multi-level converters using SiC devices, presenting optimisation strategies, and conducting comprehensive analyses on electrical, electromagnetic, and thermal aspects. Based on the comprehensive research findings and advances outlined in this thesis, to further enhance the performance, scalability, and application scope of SiC based power modules and converters, future research could potentially develop in the following directions:

1. Investigating alternative semiconductor materials: The potential benefits of integrating GaN transistors in multi-level converters should be examined, with an analysis of their impact on efficiency and thermal performance in high-frequency, high-power applications. These materials offer higher switching speeds, enabling more compact and efficient designs when integrated into power modules.
2. Thermal management optimisation: Further research could focus on enhancing the thermal management strategies for multi-level converters using advanced materials and cooling technologies to improve reliability under the extreme conditions typical of aerospace applications. This study evaluated forced air cooling, but more innovative thermal management solutions, such as hybrid air-liquid cooling or the use of PCM, could also be explored to further increase power density while maintaining or even reducing weight. Practical testing of these cooling solutions in high-stress aerospace environments is necessary to verify their effectiveness and durability.
3. Scalability and modularity: Promote the development of converters towards higher integration and modularity to simplify design and reduce costs. Exploring modular and scalable designs can enhance the flexibility of deploying multi-level converters across various power levels and application scenarios, offering more adaptable solutions. Investigating how to extend the methods developed in this work to converters operating at different power levels and in various applications can provide valuable insights for broader

industry use. As electrification expands across many industrial sectors, there is a need for dynamically modular designs that can be manufactured on a large scale at lower costs while maintaining high performance.

4. Detailed performance analysis: This work has conducted thorough DPTs on the constructed NPC converter, but it is crucial to extend this to long-term performance analysis. Such analysis is needed to understand the degradation behaviours of SiC MOSFETs under various operational stresses. These results should be compared with other semiconductor devices to pinpoint areas where SiC technology requires improvement. Additionally, more extensive long-term tests could be conducted under actual aerospace conditions, including extreme temperature operations, vibrations, and high altitudes. This will help to better understand the reliability and durability of the proposed power module designs, especially under sustained stress conditions.
5. Reduce the undesired factors produced by SiC devices: When the MOSFET is turned-on, spikes often observed in I_{ds}, they are commonly associated with the reverse recovery characteristics of the diode. This phenomenon is primarily due to the physical and electrical characteristics of the diode as it transitions from conducting to blocking state. Future work could consider selecting diodes with faster reverse recovery times to minimise the impact of reverse recovery current; designing driving strategies appropriately; and incorporating suitable damping components (such as RC networks) at critical points to help absorb the spike currents. When the MOSFET is turned off, the oscillations observed as I_{ds} drops to zero can be addressed by improving the gate drive strategies, using appropriate gate resistances and drive voltages to ensure a rapid and smooth turn-off; improving circuit layout to shorten high current paths, reduce the effects of parasitic inductance and capacitance; and considering electromagnetic compatibility at the design stage to reduce radio frequency interference and oscillation issues.
6. Enhanced parasitic parameter extraction methods: Although this work has already demonstrated the effectiveness of the two-port network model in extracting parasitic inductance, future research could focus on refining these methods for more complex converter designs. Further optimisation of layout could be explored to minimise parasitic inductance as much as possible.

Additionally, innovative packaging technologies, such as integrated planar busbars or three-dimensional packaging, could be explored to reduce parasitic inductances and enhance overall performance.

7. AI-driven design optimisation: Machine learning and artificial intelligence algorithms can be utilised to automatically optimise the design parameters of power modules, such as device selection, layout configuration, and thermal management strategies. This approach can accelerate the design process and enhance performance outcomes.

These future research directions aim to address remaining challenges and exploit the untapped potential of SiC-based power electronics technology, bringing more innovations and applications to energy conversion, industrial automation, and renewable energy. As the technology advances, further improvements in the performance, efficiency, and reliability of converters can be expected, along with their widespread application in emerging fields.

APPENDIX A
Three Level PCB-Based Embedded Converter Using SiC Bare Die

A.1 Introduction

The trends of integration, miniaturization, and system-level optimisation are increasingly shaping the landscape of modern electronics technology. PCB-embedded converters epitomize this evolution, transitioning from traditional bulky converters to more compact and efficient systems directly integrated into PCBs. As technology progresses, the need to incorporate more functionality into smaller spaces has made embedding power converters into PCBs both practical and necessary. These converters are pivotal across a wide array of applications, ranging from consumer electronics to aerospace.

A PCB-based embedded converter is a type of power converter that is designed and fabricated using PCB technology, a detailed description of the technology can be found at [183]-[184]. These converters are widely used in power electronics applications due to their compact size, low cost, and high efficiency. In [185], the embedding of SiC power chips is presented. Typically, these converters comprise several power semiconductor devices, passive components, and control circuits mounted on a PCB, which serves as the foundation, providing electrical connections and mechanical support.

The advantages of using PCB technology in converter design are numerous. PCB-based converters are more compact and lighter than traditional wire-wound or discrete component designs, making them ideal for applications where space and weight are critical. They are also easier to fabricate and assemble, reducing manufacturing costs and improving production efficiency. The use of surface mount technology (SMT) components can enhance thermal performance through better heat dissipation. Additionally, compared to power modules, PCB-based converters can significantly reduce parasitic inductance due to shorter electrical connections, achieving extremely low loop inductance values (<0.5nH) as highlighted in [186].

Overall, PCB-based converters provide a versatile and cost-effective solution for a broad spectrum of power electronics applications. This chapter outlines the benefits and technical features of PCB-embedded technology, selects a suitable converter topology, and develops a PCB-embedded converter model. Furthermore, it conducts a thermal analysis for different converter model designs, emphasizing the crucial role of thermal vias in heat dissipation.

A.2 PCB-Based Converter Model Development

As discussed in Chapter 2, while new converter topologies may not lead to major advancements [187], integration and packaging are seen as crucial for enhancing converter performance [188]-[189]. PCBs are favoured for their proven technology, standardized manufacturing processes, and cost efficiency. They enable the electrical interconnection of components on the PCB surface, and recent focus has shifted to embedding devices within the multilayer structure of PCBs to achieve higher density connections and more compact, lightweight systems [190]-[191].

Compared to conventional power modules, PCB-embedded converters integrate power devices directly into the PCB, optimising space utilization and system integration. These converters are ideal for low- to medium-power applications, such as portable devices and medium-power motor drives, due to their compactness and flexibility in layout. Power modules, however, are more suited for high-power applications like EVs and industrial controls, as they are designed to handle greater power but often with fixed topologies. PCB-embedded converters benefit from standard PCB manufacturing processes, which lower costs and reduce parasitic inductance through shorter connection lengths and optimised wiring. In contrast, power modules may have higher parasitic inductance due to longer internal connections and the use of thicker conductors. Therefore, PCB-embedded converters are preferred for compact, customized applications, while power modules are better suited for high-power, high-voltage scenarios. This chapter explores the optimal arrangement of semiconductor chips and passive components on PCBs to create scalable high-power AC/DC converters, aiming to achieve high power density with minimal weight and size. In conventional PCB circuits, packaged semiconductors are electrically connected to other components in the circuit through the printed circuit

board. The PCB embedding method embeds the power semiconductor chip in the circuit board, and Fig.A-1 shows the difference between them.

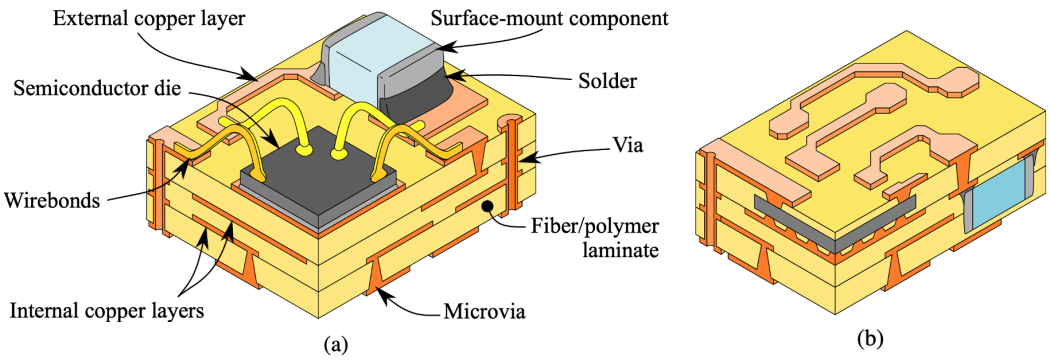


Fig.A-1 (a)Standard PCB with devices mounted on its surface; (b)same devices embedded in the PCB [192]

A comparison of the different converter topologies has been presented in chapter 2, T-type can achieve a THDi similar to that of two-level VSC, with a -33% switching frequency, the T-type topology is the most efficient in all cases, with comparable conduction losses to that of the two-level VSCs, but with lower switching losses. The power modules presented in chapter 3 are applied in high voltage and high-power application scenarios, where the power devices cannot bear excessive voltage stress, leading to the selection of the NPC topology. While in the PCB embedded converter, the required DC bus voltage is 540V, to pursue a higher converter performance, the T-type topology was finally chosen for the PCB embedded converter.

To design high power density AC-DC converters, it is critical to understand high temperature PCB technology, available 1200V/80A SiC semiconductor die, suitable passive components, series-parallel connections and sharing techniques. It is also essential to carefully examine AC-DC converter topologies that can effectively utilise PCB packaging methods. This will help in selecting the right components so that the converter ratings and operating voltages can be adjusted according to future application requirements. A key aspect of this work is the evaluation of the thermal performance of the package-optimised high power density converter. For this purpose, high fidelity models need to be developed to calculate the maximum temperature of the components, including estimation of the heat emitted from the PCB package.

To design the PCB embedded converter for medium power level application, it was considered to make additional electrical connections to form a T-type topology

based on a half-bridge topology, where each switch is connected in parallel using five semiconductor power dies. The original design placed T2, T3 and T4 in the same plane. T2 and T3 share the same copper layer for common source connection, and the bottom of T3 and T4 share the same copper layer to connect them to the AC output. T1 is placed directly below T4 and is connected through several micro vias. All devices are embedded in the whole PCB design. The tracked PCB schematic is shown in Fig.A-2.

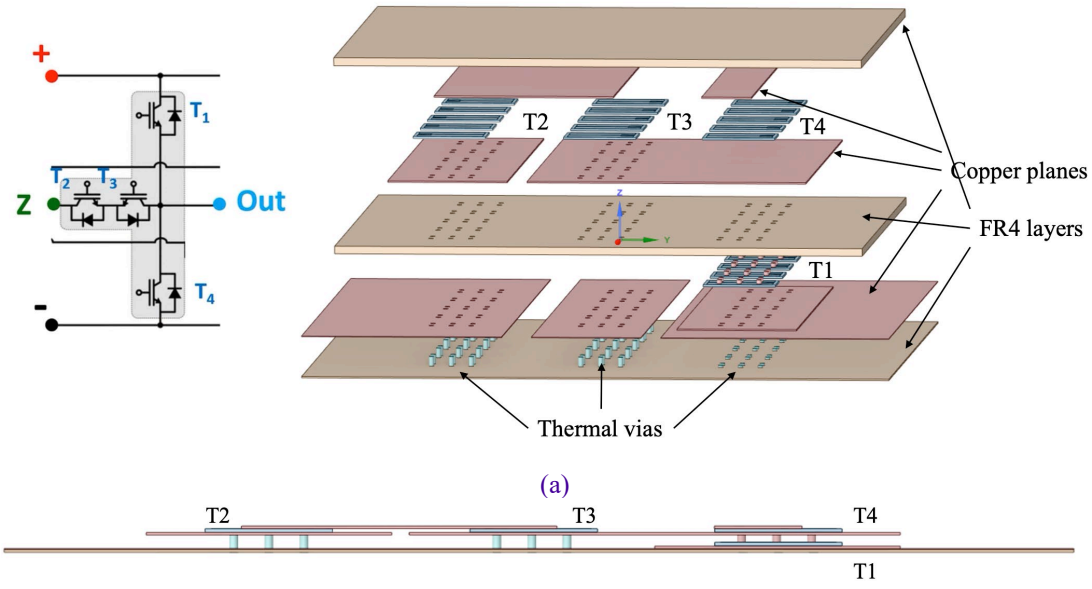
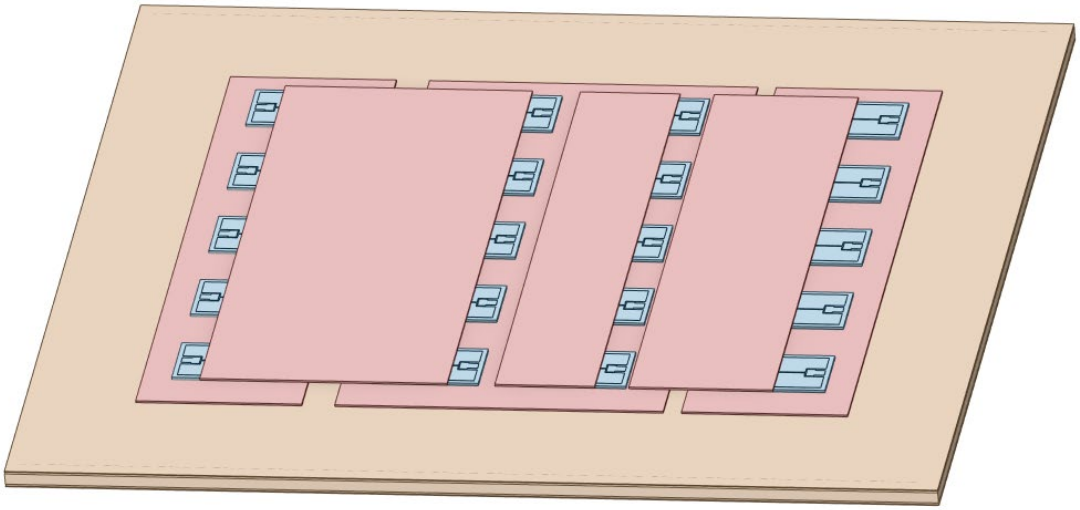
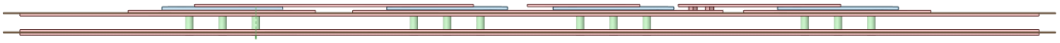


Fig.A-2 (a)Stacked T-type converter layers (b)side view of stacked embedded T-type PCB converter (without FR4 layer)

This stacked structure design is a considered option, but in the actual fabrication process two switches (T1&T4) stacked may cause some difficulties at the technical level, so at the same time a PCB structure that places all the devices in the same plane is also designed. This planar structure moves the T1 switch from underneath T4 to its other side, as shown in Fig.A-3, and connects it to the drain of T4 via a copper trace and micro vias.



(a)



(b)

Fig.A-3 (a)Planar PCB embedded converter (b) Side view of planar embedded T-type PCB converter (without FR4 layer).

Multilayer PCB typically consist of alternating layers of conductive copper and insulating FR4 material. Depending on the specific requirements of the design, the exact thickness and composition of each layer may vary. However, a general description of a multilayer printed circuit board stack, from top to bottom, is as follows:

1. Prepreg Layer: Made of glass fibre cloth with partially cured epoxy resin, it bonds copper and fibre layers in a PCB while providing electrical insulation. During lamination, the prepreg cures to create a strong structure. Thickness ranges from 50 to 200 microns, based on material and design needs.
2. Top Copper Layer: The outer conductive layer, usually copper, includes traces, component pads, and connections for power semiconductor sources and gate control signals. According to equation (5.1), common copper thickness (d) is typically 1 oz/ft² (~35 µm) or 2 oz/ft² (~70 µm). Thicker layers handle higher currents, improve heat dissipation, and increase the current-carrying capacity of the PCB (hundreds of amperes) [193].

$$d = \frac{m}{\rho \times A^2} = \frac{1oz}{8.9kg/dm^3 \times 1sq^2} = 34.29\mu m \tag{5.1}$$

3. Inner Copper Layer: Inner conductive layer, usually made of copper. It connects the drain of the power semiconductor die and connects to the external components via conductive vias. The copper thickness of this layer is usually the same as that of the top layer.
4. FR4 inner core: Main insulating layer made of FR4 material, a glass fibre reinforced epoxy laminate. It provides mechanical strength and electrical insulation between the internal copper layers. FR4 core thicknesses range from 0.8 mm to 1.6 mm or thicker, depending on the overall thickness of the printed circuit board and design requirements.
5. Inner Copper Layer: Second inner conductive layer.
6. Prepreg Layer: Another layer of adhesive prepreg similar to the first layer, which bonds the inner and outer layers together.

This work builds two PCB embedded converter designs based on the above structure, the first stacked structure can further save space but may cause difficulties for the manufacturer, the second planar one places all the switches in the same plane for easy fabrication, which helps in heat dissipation of the device but slightly increases the space.

A.3 PCB-Based Converter Thermal Considerations

The development of PCB-based power converters faces challenges in current capacity and managing hot spots. In this study, PCB track current is limited to 100A continuously and 200A temporarily. Component temperatures are capped at 125°C during normal operation and 140°C under fault conditions, ensuring reliability and efficiency. Copper planes in PCB designs serve both as conductors and heat spreaders, traditionally using heat sinks for cooling. A more efficient solution is incorporating thermal vias to enhance vertical heat dissipation.

Thermal vias are small copper-filled holes in a PCB that transfer heat between layers, enhancing overall thermal performance. They create a strong conduction path for efficient heat dissipation, which is crucial in high-power, high-density designs. By effectively transferring heat from components, thermal vias help prevent overheating, improve reliability, and extend device lifespan. Fig.A-4 shows a cross-sectional view of a PCB embedded converter, comparing designs with and without thermal vias.

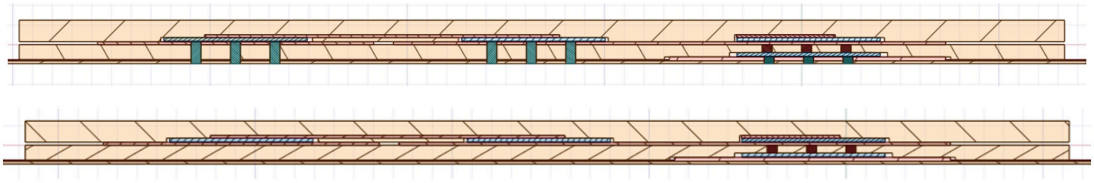


Fig.A-4 PCB cross-section with thermal vias (top), PCB cross-section without thermal vias (bottom)

Larger thermal vias can provide a larger heat transfer area, thus enhancing heat transfer efficiency. However, it may affect the structural integrity of the PCB. And more thermal vias means more heat transfer paths, which helps to improve heat dissipation efficiency. But the size and number of thermal vias need to be balanced to ensure that they do not unduly weaken the mechanical structure and electrical performance of the PCB.

More and denser thermal vias means that more meshes need to be generated during the simulation process, which can result in a long simulation time or even failure to converge leading to task abort. To solve this problem, two different vias models are designed, in the first scenario shown in Fig.A-5, the diameter of the chosen vias model is 0.5mm, and a total number of 6 vias are used, which are connected to the MOSFET model at the top and to the copper layer model at the bottom.

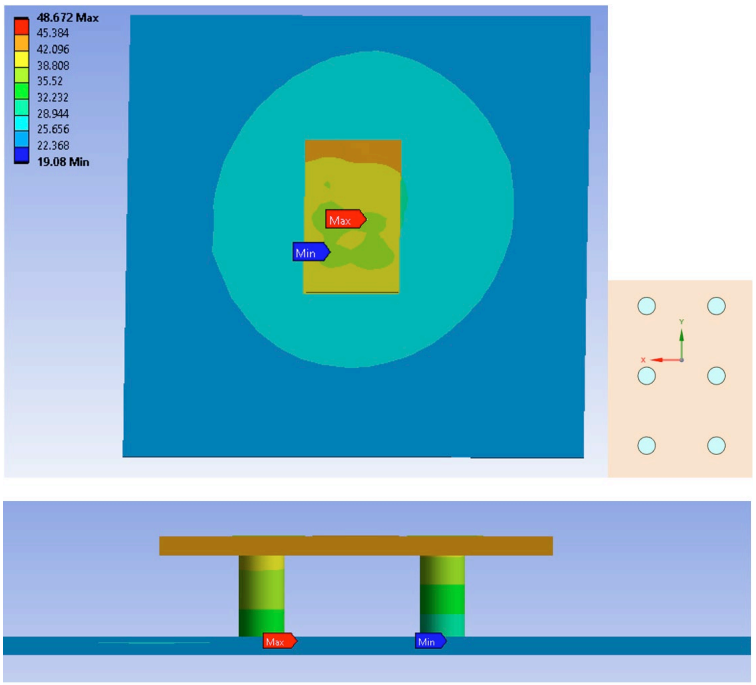


Fig.A-5 Thermal distribution with fewer vias

In the second scenario shown in Fig.A-6, a model diameter of 0.2 mm was chosen and a total number of 35 were used, the first using multiple cylinders with a small individual cross-sectional area and the second using fewer cylinders with a large individual cross-sectional area, the total cross-sectional area of both designs being nearly the same.

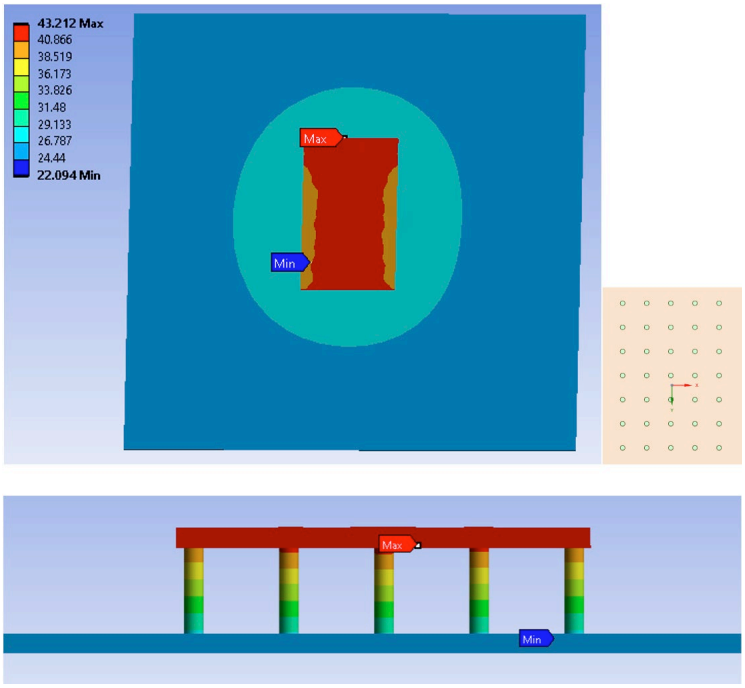


Fig.A-6 Thermal distribution with more vias

From the thermal simulation results, the maximum temperatures generated using the two models were 48.6 °C and 43.2 °C, respectively. Using the first design results in slightly worse heat dissipation, but the error is within acceptable limits, and the first represents a case where poor heat dissipation means better actual performance. Therefore, to simplify the simulation model and save simulation time, this design is applied to the thermal simulation model afterwards.

When simulating the temperature rise of a PCB with thermal vias in ANSYS Mechanical, it's essential to set accurate boundary conditions to reflect the system's physical environment. After setting these conditions, a transient or steady-state thermal analysis can be conducted to assess the temperature rise in the PCB model. Firstly, the temperatures generated under different boundary conditions were analysed in the half leg configuration model. The PCB bottom surface temperature was set to be 25°C in all cases, but the top surface was set to have three different convection conditions. In the first case, a convection coefficient of 400 W/m^2K is used to

simulate forced air convection with heat sinks, in the second case a convection coefficient of 20 W/m^{2}K is used to simulate natural air convection, and in the third there is no convection applied.

Fig.A-7 shows the temperature distribution for the three cases, naturally the case with higher thermal convection coefficient boundary condition has better heat dissipation performance, but even without convection applied, the maximum temperature difference is 106 °C, which does not lead to device damage due to overheating. It is worth noting that no thermal vias are used in the modelling here.

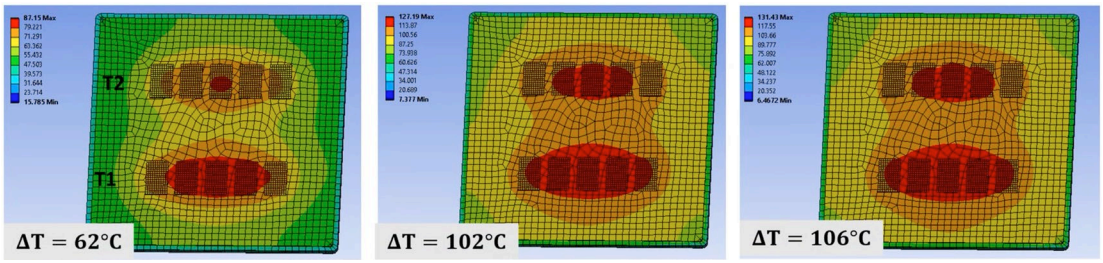
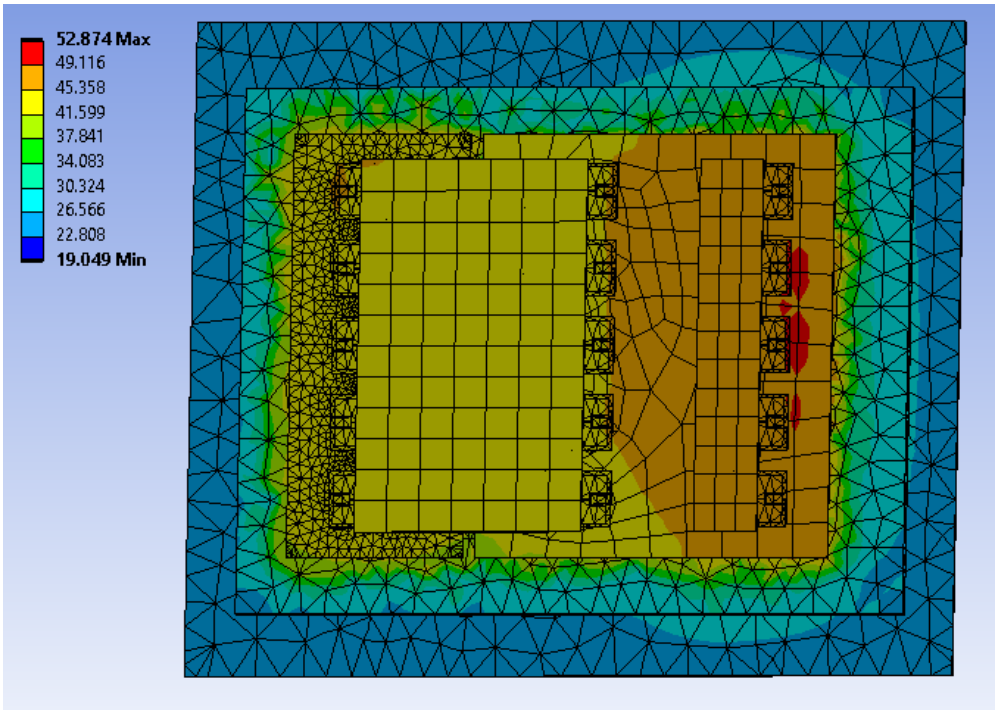


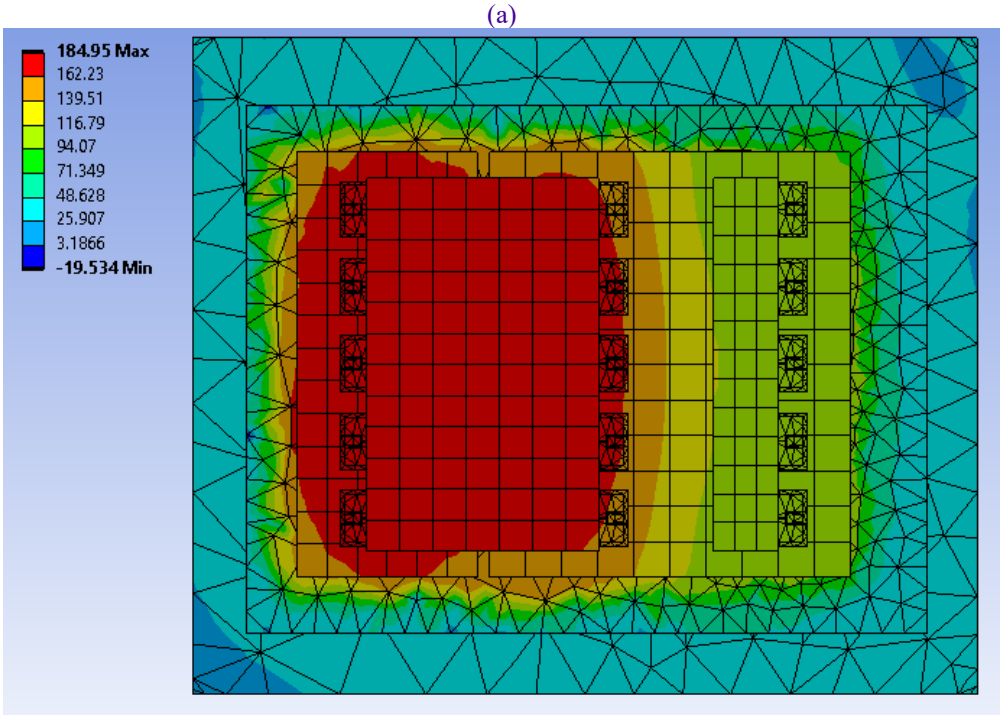
Fig.A-7 Temperature distribution for three cases

After knowing the influence of the above aspects, the thermal simulation of the stacked T-type PCB-based embedded model created in the Section A.3 is performed using the thermal vias model with poor heat dissipation and without setting the thermal convection coefficients on the top surface of the PCB to simulate the worst scenario case.

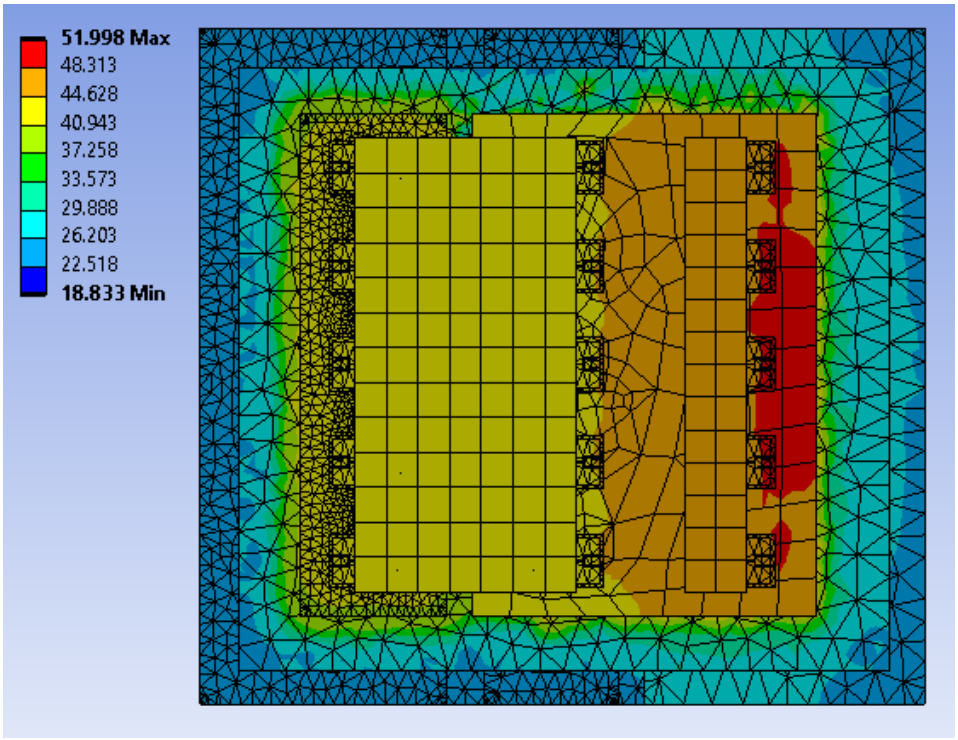
The thermal performance of the different cases was compared, Fig.A-8(a) shows the temperature distribution with thermal vias and the distance between semiconductor dies is 1.6mm, Fig.A-8(b) shows the temperature distribution without thermal vias and the distance between semiconductor dies is 1.6mm, Fig.A-8(c) shows the temperature distribution with thermal vias a and the distance between semiconductor dies is doubled to 3.2 mm, Fig.A-8(d) shows the temperature distribution without thermal vias and the distance between semiconductor dies is 3.2mm. To better show the temperature distribution all results hide the top FR4 layer.


52.874 Max
49.116
45.358
41.599
37.841
34.083
30.324
26.566
22.808
19.049 Min

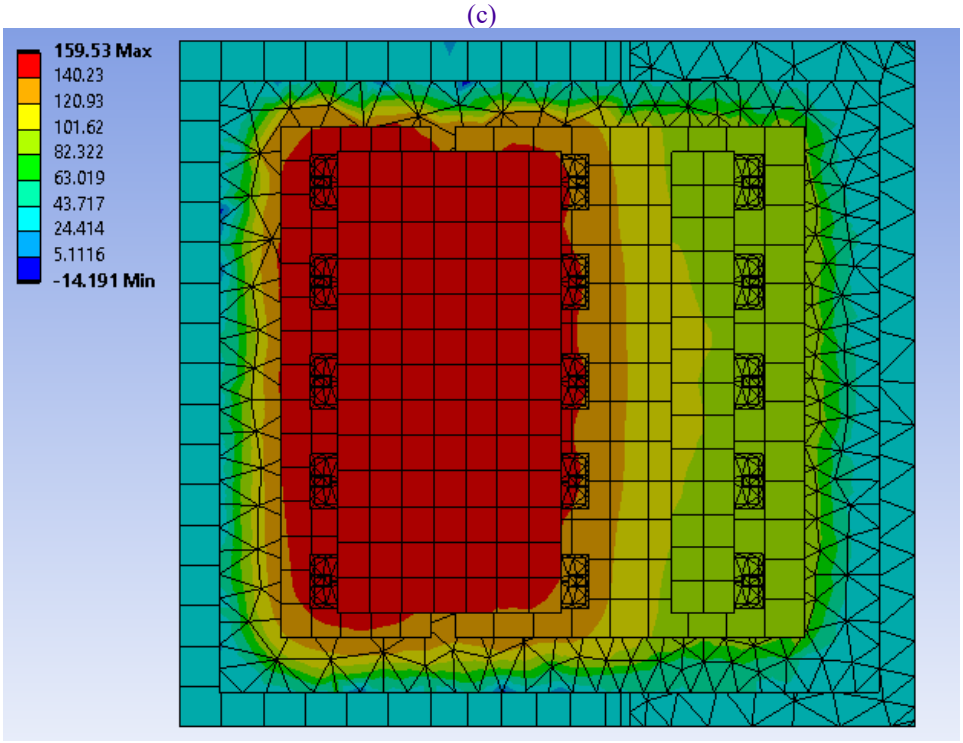
(a)


184.95 Max
162.23
139.51
116.79
94.07
71.349
48.628
25.907
3.1866
-19.534 Min

(b)



(c)



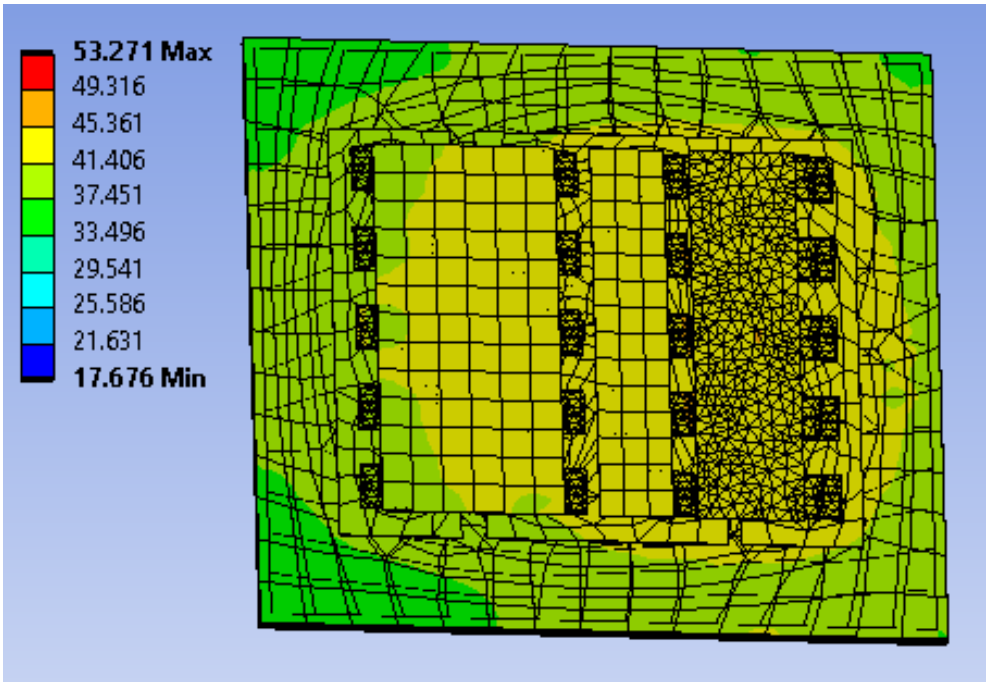
(d)

Fig.A-8 Temperature distribution (a) with thermal vias, 1.6mm distance between dies (b) without thermal vias, 1.6mm distance between dies (c) with thermal vias, 3.2mm distance between dies (d) without thermal vias, 3.2mm distance between dies

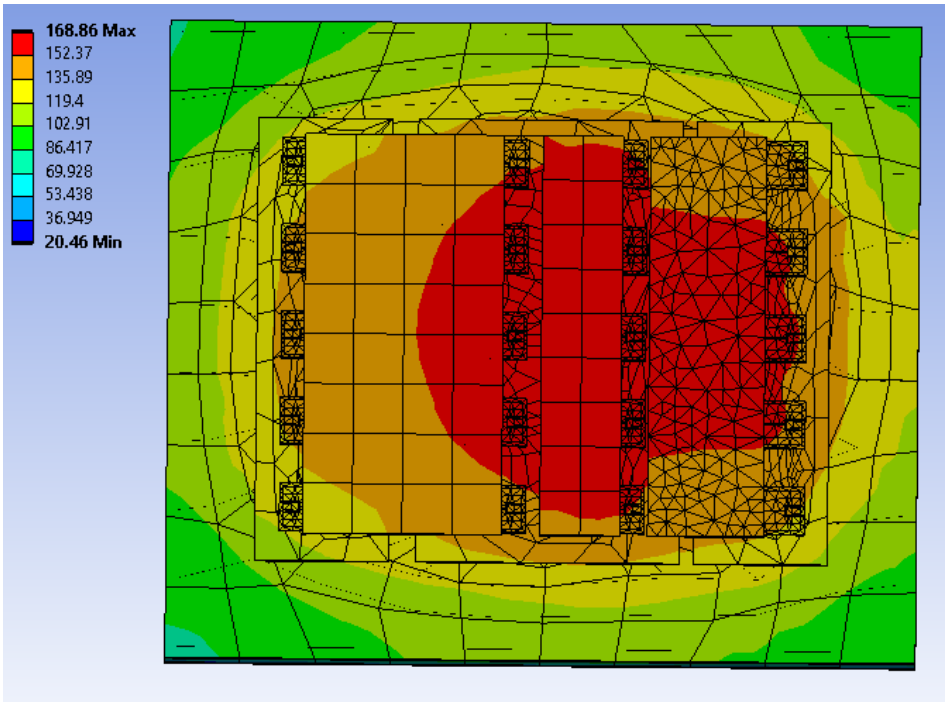
Based on the above simulation results, compared to the case without thermal vias, the PCBs with thermal vias (Figs. (a) and (c)) exhibit significantly lower maximum temperatures under the same conditions, suggesting that the thermal vias effectively aid in the vertical conduction of heat and mitigate localised hot spots. A smaller die

distance (1.6 mm) resulted in higher temperatures (Figures (a) and (b)). In contrast, increasing the die distance to 3.2 mm (Figs. (c) and (d)) helped to reduce the heat build-up between the dies, lowering the maximum temperature. However, if thermal vias are used then the distance between the dies has little effect on the heat, at this point, slightly reducing the spacing between dies has minimal impact on the thermal performance of the converter, but it significantly improves the space utilization of the PCB. When thermal vias are used, the highest temperature occurs at device T4 due to higher losses. When thermal vias are not used, the highest temperature occurs at devices T2, T3 because the temperature cannot be transferred vertically.

In addition, the structure of the planar T-type PCB-based embedded converter is also analysed by thermal simulation for comparison, only the case when the distance between the semiconductor dies is 1.6 mm is considered here. Fig.A-9(a) shows the temperature distribution of this PCB structure with thermal vias, and Fig.A-9(b) shows the temperature distribution without thermal vias.



(a)



(b)

Fig.A-9 Temperature distribution (a)with thermal vias (b) without thermal vias

It can be seen that there is little difference in the thermal behaviour of this planar design with the thermal vias versus the stack design, and when the thermal vias are not used, even though the maximum temperature of the planar design will be lower than that of the stacked design, both are exceeding the maximum temperature that the device can withstand at this point.

However, due to the short period of the project and the difficulty of the manufacturing process. The PCB-based embedded converter designed above has not been physically built yet, so it is not possible to experimentally verify the above simulation results and conduct further testing.

A.4 Summary

This chapter introduces a relatively new PCB-based converter technology, unlike the use of power modules, this approach helps to reduce the cost, size, and weight of the converter, but it cannot be applied to high voltage and high-power scenarios.

Based on this technology, two different PCB embedded converter designs with three level T-type topology are designed, each of them has advantages and disadvantages, but no matter which design can be practically applied eventually, according to the thermal simulation results, as long as a proper heat dissipation

method is used and each device is connected to the thermal vias, both PCB's have a good heat dissipation performance, even in the worst case scenario.

To conclude this chapter provides a design solution for multi-level PCB based converter design, however unfortunately it cannot be verified at this point in time so further research is required.

APPENDIX B
Three-level SiC Converter Power Losses at 125°C and 175°C Junction Temperature

Due to space limitations in the main text, the electrical performance of the three-level SiC converter at junction temperatures of 125°C and 175°C is summarised in Appendix B.

Table B-1 and Table B-2 show the conduction losses and switching losses for varying numbers of parallel-connected MOSFETs at a device junction temperature of 125°C, respectively.

Table B-1 Conduction losses for different number of MOSFETs in parallel (Temp.=125°C)

Conduction losses (W)	Top/Bottom MOSFETs	Middle MOSFETs	Total losses/one leg
3 MOSFETs per Switch	74.77	106.13	1085.40
4 MOSFETs per Switch	44.68	60.22	839.20
5 MOSFETs per Switch	27.52	38.25	557.70
6 MOSFETs per Switch	19.14	25.98	541.44
7 MOSFETs per Switch	14.06	19.57	470.82
8 MOSFETs per Switch	11.34	15.69	432.48

Table B-2 Switching Losses for different number of MOSFETs in parallel (Temp.=125°C)

Switching losses per leg (W)	Temp.=125°C, F_{sw} = 20 kHz, I_{rms} = 282.2 A
3 MOSFETs per Switch	90.5
4 MOSFETs per Switch	82.8
5 MOSFETs per Switch	79.6
6 MOSFETs per Switch	82.6
7 MOSFETs per Switch	89.7
8 MOSFETs per Switch	88.8

Table B-3 shows the total losses in each phase leg as well as the efficiency when the device's junction temperature is 125 °C, Table B-4 shows the power density per chip under this case, the power density is set as one of the boundary conditions of the thermal simulation model.

Table B-3 Losses for different number of MOSFETs in parallel (Temp.=125°C)

Losses per leg (W)	Conduction losses	Switching losses	Diode losses	Total losses	Efficiency
3 MOSFETs per Switch	1085.40	90.5	296.4	1472.30	98.69%
4 MOSFETs per Switch	839.20	82.8	295.2	1217.20	98.92%
5 MOSFETs per Switch	557.70	79.6	311.4	948.70	99.16%
6 MOSFETs per Switch	541.44	82.6	306.6	930.64	99.17%
7 MOSFETs per Switch	470.82	89.7	305.4	865.92	99.23%
8 MOSFETs per Switch	432.48	88.8	298.2	819.48	99.27%

Table B-4 Power density for different device (Temp.=125°C)

Power density per chip (W/m^3)	Top/bottom MOSFETs	Middle MOSFETs	Clamping diodes
3 MOSFETs per Switch	1.445×10^{10}	1.995×10^{10}	2.707×10^{9}
4 MOSFETs per Switch	8.750×10^{9}	1.148×10^{10}	2.696×10^{9}
5 MOSFETs per Switch	5.529×10^{9}	7.412×10^{9}	2.844×10^{9}
6 MOSFETs per Switch	3.963×10^{9}	5.164×10^{9}	2.800×10^{9}
7 MOSFETs per Switch	3.030×10^{9}	3.997×10^{9}	2.789×10^{9}
8 MOSFETs per Switch	2.477×10^{9}	3.241×10^{9}	2.724×10^{9}

A worst case with junction temperature of 175°C is also considered here, Table B-5 and Table B-6 show the conduction losses and switching losses when different numbers of MOSFETs are connected in parallel, respectively.

Table B-5 Conduction losses for different number of MOSFETs in parallel (Temp.=175°C)

Conduction losses (W)	Top/Bottom MOSFETs	Middle MOSFETs	Total losses/one leg
3 MOSFETs per Switch	93.88	134.06	1367.64
4 MOSFETs per Switch	55.03	75.28	1042.48
5 MOSFETs per Switch	34.01	46.71	807.20
6 MOSFETs per Switch	23.92	32.59	678.12
7 MOSFETs per Switch	17.27	23.26	567.42
8 MOSFETs per Switch	13.56	18.83	518.24

Table B-6 Switching Losses for different number of MOSFETs in parallel (Temp.=175°C)

Switching losses per leg (W)	Temp.=175°C, F_{sw} = 20 kHz, I_{rms} = 282.2 A
3 MOSFETs per Switch	85.7
4 MOSFETs per Switch	79.6
5 MOSFETs per Switch	75.4
6 MOSFETs per Switch	78.8
7 MOSFETs per Switch	82.1
8 MOSFETs per Switch	83.6

Table B-7 shows the total losses in each phase leg as well as the efficiency when the device junction temperature is 125℃, Table B-8 shows the power density per chip under this case.

Table B-7 Losses for different number of MOSFETs in parallel (Temp.=175℃)

Losses per leg (W)	Conduction losses	Switching losses	Diode losses	Total losses	Efficiency
3 MOSFETs per Switch	1367.64	85.7	336.0	1789.34	98.41%
4 MOSFETs per Switch	1042.48	79.6	329.4	1451.48	98.71%
5 MOSFETs per Switch	807.20	75.4	355.8	1238.40	98.90%
6 MOSFETs per Switch	678.12	78.8	349.8	1106.72	99.02%
7 MOSFETs per Switch	567.42	82.1	340.2	989.72	99.12%
8 MOSFETs per Switch	518.24	83.6	333.0	934.84	99.17%

Table B-8 Power density for different device (Temp.=175℃)

Power density per chip (W/m^3)	Top/bottom MOSFET	Middle MOSFETs	Clamping diodes
3 MOSFETs per Switch	1.773×10^{10}	2.478×10^{10}	3.069×10^{9}
4 MOSFETs per Switch	1.053×10^{10}	1.409×10^{10}	3.008×10^{9}
5 MOSFETs per Switch	6.631×10^{9}	8.860×10^{9}	3.250×10^{9}
6 MOSFETs per Switch	4.774×10^{9}	6.296×10^{9}	3.195×10^{9}
7 MOSFETs per Switch	3.546×10^{9}	4.597×10^{9}	3.107×10^{9}
8 MOSFETs per Switch	2.838×10^{9}	3.763×10^{9}	3.041×10^{9}

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