Investigation of Gallium Nitride Bidirectional Power Semiconductor Devices with Polarization Super Junction Technology

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By

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Abstract

Due to its superphysical features, Gallium-Nitride, one of the wide band-gap materials, has been a favoured option for the next generation of power devices in recent years. The pervasive applications of GaN in the photoelectric field have accelerated the development of GaN technologies for power electronic applications. GaN-based devices have low on-state resistance, high switching speed and high voltage blocking capability for high-frequency/temperature operation. In particular, the development and commercialization of GaN epitaxial growth technology with large diameter substrates make GaN power devices have a lower cost. As a result, research on GaN power semiconductors is a hot topic in the world.

The aims of work in this thesis focus on investigating new compact monolithic bidirectional switches using Polarization Super Junction concept (Bi PSJ HFETs), one of the most compact bidirectional switches reported to date. Under different bias conditions, Bi PSJ HFETs can be operated as Bidirectional devices, unidirectional HFETs with/without Hybrid Drain-embedded Gate Injection Transistor (HD-GIT) mode and diodes in both directions. Large-area Bi PSJ HFETs with Schottky Gate and Ohmic Gate are fabricated on 6' Sapphire wafer, as well as test structure. Numerical simulations and electrical characterisation prove that Bi PSJ HFETs can realize the function of bidirectional switches. Detailed analysis of the on-state behaviour of the fabricated Bi PSJ HFETs is presented.

Next, temperature-dependent on-state characteristics of PSJ Merged Schottky Barrier Diode (PSJ MSBD) and PSJ HFETs are presented and discussed. The trends of specific on-state resistance with increasing temperature are calculated and shown, which are critical for thermal analytical models of Ron.A and further improvement of on-state performance for PSJ devices.

Finally, Current large-area PSJ devices are mainly based on multi-finger layout designs, strongly dependent on the metallization flatness and the insulator layer quality in designing large-area devices. Finger parasitic impedance e is essential to the manufactured performance of devices. In this work, it introduces five layout schemes, including Multi-finger Drain-Source(D-S) Layout, Multi-finger Drain-Source-Drain(D-S-D) Layout, Multi-finger Source-Drain-Source Layout (S-D-S), Checkerboard layout and Hexagonal-shaped layout. It compares the simulated parasitic impedance of metalization layouts for 1A PSJ HFETs. The area of the active region for each layout is also calculated for a 10A current rating with various

PSJ lengths. The advantages and disadvantages of layouts are discussed based on the simulation results.

Publication

1. X. Tan and E. M. S. Narayanan, “Compact GaN-based Bidirectional Polarization Super Junction HFETs with Schottky Gate on Sapphire,” 2023. doi: 10.14311/isps.2023.022.

Contents

List of Figures

List of Tables

Chapter 1: Introduction

1.1 Overview

The rapidly spreading global COVID-19 pandemic has profoundly impacted the global and national environment, societies and economies since December 2019. The potential new practices and social forms facilitated by the epidemic impact energy demand and consumption. According to the released 'Energy consumption in the UK 2021', except domestic sector, the energy consumption in industry, services and transport shows a decreasing trend. The total energy consumption in the UK decreased by 12.9% of oil equivalent between 2019 and 2020. All fuels saw declines except biofuels and waste; in particular, petroleum fell by 15.9 million barrels (25%)[1].

On the other hand, net CO_2 emissions from energy use fell by 16% with lower consumption [2]. Even while economies are bent under the weight of Covid-19 lockdowns and the dropped energy demand, renewable energy sources alternatives to fossil fuels, such as wind and solar photovoltaics, continue growing rapidly [3]. In UK's energy market in 2020, For the first time, renewables made up more than 40% of the generation mix, and their proportion in the UK's primary energy mix increased to 17%. [2]. This new energy economy is emerging but the transformation still has a long way to go. Despite advances in renewable energy and electric transportation, coal and oil use will rebound sharply in 2021. Largely as a result, its carbon dioxide emissions recorded the second-largest annual increase in history[3].

To cope with the massive growth in energy demand, climate change, cost-effectiveness and achieving a sustainable society in the future, there is an increasing demand for clean and renewable electricity. The growing focus on electrification is fuelling the demand for different forms of electricity. Power electronics is a branch of electrical engineering. Power electronics uses electronic devices to control and convert electrical power, which is used in power generation, transmission, distribution and control. From home electronics to space applications, stable and reliable power electronics system are needed to power the required specifications. The main components of power electronic systems are switching power converters composed of power semiconductor devices.

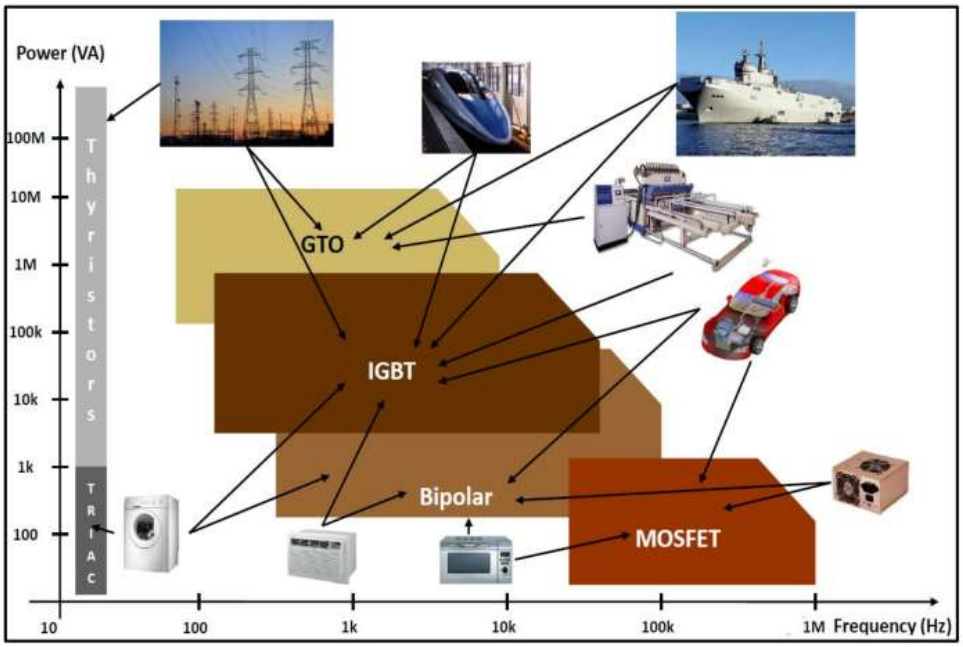


Figure 1.1.1:Power semiconductor devices and applications with respect to operating power and switching frequency.

The main components of power electronic systems are switching power converters composed of power semiconductor devices. Power semiconductor devices are the heart of electrical energy conversion and power/current control in electrical circuits. In essence, it is the function of the power switch and power conversion by utilising the one-way conductivity of the semiconductor. Figure 1.1.1 shows the major power semiconductor devices and their associated applications at different operating powers and switching frequencies. The global power semiconductor market was valued at USD 40.5 billion in 2022 and is projected to be worth USD 55.8 billion by 2027, with an annual growth rate of 6.6% from 2022 to 2027[4]. The demand for power semiconductor devices has exceeded the factory capability, especially as the nationwide lockdown and closure of semiconductor plants caused by COVID-19 have further fuelled the supply shortage trend[5].

Silicon (Si) has dominated the semiconductor industry since the invention of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) in 1959 due to its low cost, mature technologies, reliability, and facility of growing high-quality native oxides on its surface[6]. Nowadays, Silicon-based semiconductors make up about 80% of the power market, including Si MOSFETs, super-junction power MOSFETs and insulated-gate bipolar transistors (IGBTs). Unfortunately, the intrinsic material characteristics of Si fundamentally restrict the performance enhancement of the devices. Si is a narrow band-gap semiconductor (band gap energy (E_G)=1.1eV), which limits its power handling capacity. Si-based devices are reaching a stage of theoretical performance limits. As a result, As an

alternative to silicon, market participants are concentrating on wide-bandgap (WBG) materials to provide more efficient power converters with less power loss. Silicon Carbide (SiC), Gallium nitride (GaN), Diamond, and other novel materials with a wide bandgap are extensively researched.

1.2 Need for wide band-gap semiconductors

There is ongoing research to develop the WBG materials' potential and harness its benefits. As technology progresses, a newer class of power device based on GaN and SiC has come onto the scene and competed against silicon IGBTs and MOSFETs in various segments.[7]. Table 1.1 presents the fundamental intrinsic material properties of Si, 4H-SiC and GaN. Figure 1.2.1 compares detailed vital parameters of WBG materials and Si. The current mainstream GaN power transistors exploit the characteristics of the two-dimensional electron gas (2DEG) at the interface between GaN and AlGaN. Hence, pertinent data regarding 2DEG is presented in Table 1.2.1. It should be emphasized that in the relevant literature or for actual devices we can find the observed electron mobility of 2DEG is different, which depends on the structural quality of the layers. The interface roughness scattering and the alloy disorder scattering are factors affecting low-temperature 2DEG mobility. At room temperature or high temperature, polar optical phonon scattering is the dominant scattering mechanism. It is an effective way to enhance in the electron mobility by adjusting the nucleating layer to reduce the dislocation and scattering.

Table 1.1: Fundamental intrinsic material properties of Si, SiC, GaN and Diamond([8],[9], [10])**.**

Parameters	Symbol	Si	4H-SiC	GaN
Band-gap	E_g (eV)	1.12	3.26	3.39
Critical electrical field	E_C (MV/cm)	0.23	2.2	3.3
Thermal conductivity	λ $(W/m.k)$	150	380	130
Electron mobility	μ $(cm^2/V.s)$	1400	950	800(Bulk) 1700(2DEG)
Saturation Velocity	v_{SAT}	1 (normalised)	2.2	2.5

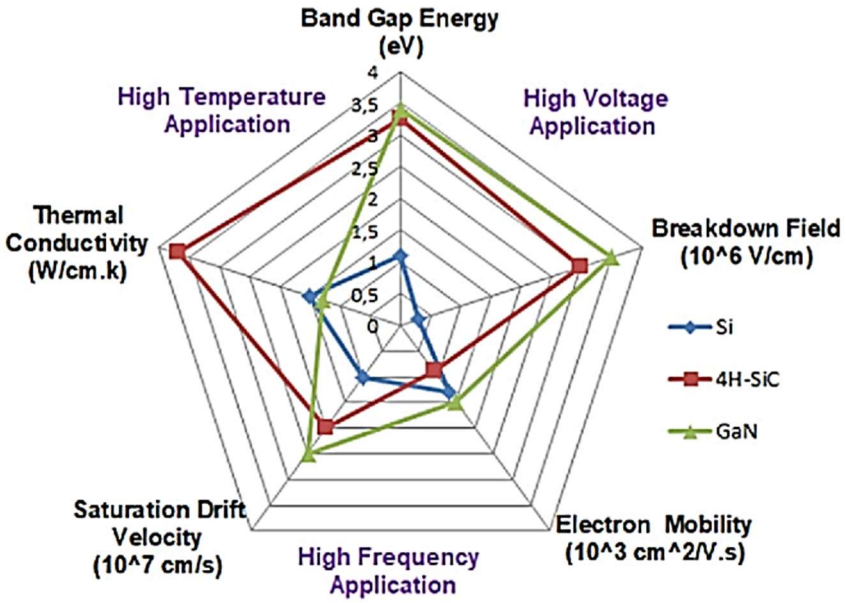


Figure 1.2.1 : Comparison of material properties for Si, 4H-SiC, and GaN [11].

For a power converter, the on-state resistance, blocking capability and switching speed are significant principles to evaluate its performance. The voltage blocking capability is relative to the breakdown voltage of power devices in the off-state. When carriers obtain enough energy to overcome the band-gap to generate Electron-Hole pairs (E-H pair), generated electron-hole pairs are accelerated by the electric field and lead to further generation of electron-hole pairs. The multiplication phenomenon causing a significant current is called impact ionisation. The impact ionisation process, given by a material constant, eventually leads to the avalanche breakdown. Avalanche breakdown is a physical limitation to withstanding voltage for any material. The critical electrical field of materials refers to the maximum electrical field that accompanists the onset avalanche breakdown for an abrupt plane-parallel junction. The relationship between the theoretical breakdown voltage B_V and the critical electrical field E_C can be induced from basic electrostatics, and the Equation is shown below [10]:

$$B_V = E_C \times L \quad \text{--- (1.1)}$$

$$B_V = E_C \times \tau \times v_{SAT} = E_C \times \frac{1}{2\pi fc} \times v_{SAT} \quad \text{---(1.2)}$$

$$B_V \times fc = \frac{E_C \times v_{SAT}}{2\pi} \quad \text{--- (1.3)}$$

Where L is the spacing of the electron path, τ is the transit lift time of the electron in the path, $v_{SAT}$is the saturation velocity of carriers, and fc is the cut-off frequency. From Equation (1.3), it is evident that a high critical electric field E_C and high saturation velocity (v_{SAT}) can enhance the breakdown voltage of devices operating at high-frequency switching applications. Compared with Si-

based devices, WBG semiconductors have a greater voltage-blocking capability because the extreme electrical field Ec is over ten times higher than Si. The higher electron mobility of comprehensive band-gap materials promises lower electrical resistance.

For another, the higher electron mobility of wide band-gap materials promises lower electrical resistance and, thus, low conductor losses [12]. In addition, the saturation velocity over twice faster as that of Si makes carriers inject/remove faster in the depletion region, which improves the switching speed.

Another critical advantage of WBG devices is that they reduce power dissipation at high-frequency operations. The Equation of power loss in a hard-switching chopper circuit is shown below:

$$Loss \propto \frac{\sqrt{f}}{FOM} \quad \text{---(4)}$$

"FOM" is the Figures of Merit, which is calculated from the intrinsic material properties. Table 1.2.2 lists the FOM of wide band-gap materials normalised to Si.

Table 1.2 :FOM of wide band-gap materials normalised to that of Si [13]**.**

Figure of Merit	Si	SiC	GaN
$M_{RonA} = \varepsilon\mu {E_c}^3$	1	560	2414
$M_{Loss} = E_C\sqrt{\mu}$	1	8.2	14

In Table 1.2, M_{RonA} is the inverse of conduction loss per unit area and M_{Loss} is the inverse of total loss, including conduction losses and switching losses. It can be found that wide band-gap semiconductors with larger values can reduce power loss effectively compared to silicon power devices operating at the same frequency.

All the material properties and factors listed above indicate WBG power semiconductors break through limits in traditional silicon devices and increase the electric energy conversion efficiency. SiC devices are gaining in popularity as an alternative to silicon IGBTs in high-voltage/high-current applications such as motor drivers. Switching power supplies and other compressed applications get the potential to utilise GaN-based devices.

1.3 GaN Market and the commercial Gallium Nitride devices

The following are certain areas where GaN devices significantly outperforms Si-Based technologies:

- Lower on-state losses:
- Better voltage-blocking capability
- Higher switching speed
- Higher efficiency at higher frequency

Since the first GaN-based transistors were introduced in the early to middle of the 1990s, GaN devices have become the focus of extensive studies and development for high-voltage, high-frequency, and high-power applications[14]. In 2001, the first GaN HEMTs on 4-inch wafers were produced. Fujitsu developed the world's most efficient power-saving high GaN HEMT power amplifier in 2021 ,which achieved 82.8% power conversion efficiency at 2.45 GHz and reduce power loss by about 25%[14].

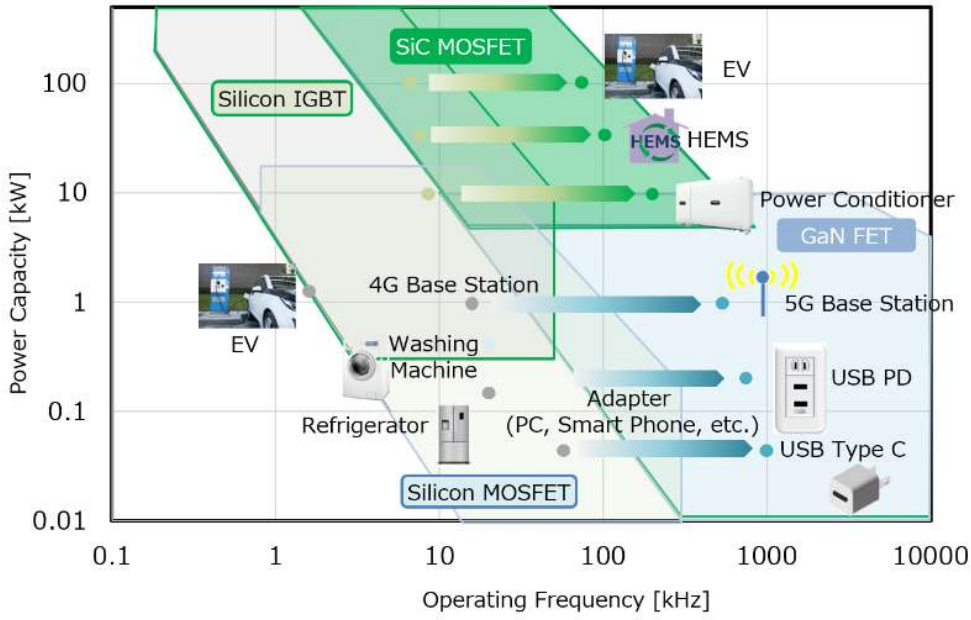


Figure 1.3.1: Application range of Si, SiC, GaN device for each power capacity and operating frequency[15].

By 2021, the market for GaN semiconductor devices would indeed be valued $1.85 billion and be expanding quickly. From 2022 to 2031, it is anticipated to expand at an annualized rate of growth of 27.4%, reaching $19.5 billion by the end of that period[16]. Figure 1.3.1 shows possible applications for Si, SiC and GaN power devices for each power capacity and operating frequency. As shown in Figure 1.3.1, GaN has desired properties in high-power amplification and power systems of 10kW or less[9]. The rise in the adoption of 5G Network Globally and the rise in demand for USB power delivery boosts the demand for GaN Semiconductor Devices.

Currently, 100 V and 650 V GaN devices are majorly serving the current and near-future demands in power systems. Commercial GaN-based power electronic devices are now available from

Efficient Power Conversion Corporation, Inc., Transphorm, Inc., Panasonic, InC., GaN system, Inc., Fujitsu Ltd., NXP Semiconductor, N.V., and Infineon. Considering the trade-off between the device manufacturing costs and the device estimated performance based on its intrinsic material properties, GaN has become an excellent material for fabricating power semiconductor devices over the past years. As depicted in Figure 1.3.2, GaN-based devices can achieve 10 times lower specific on-resistance compared to SiC-based devices at 600V-class.

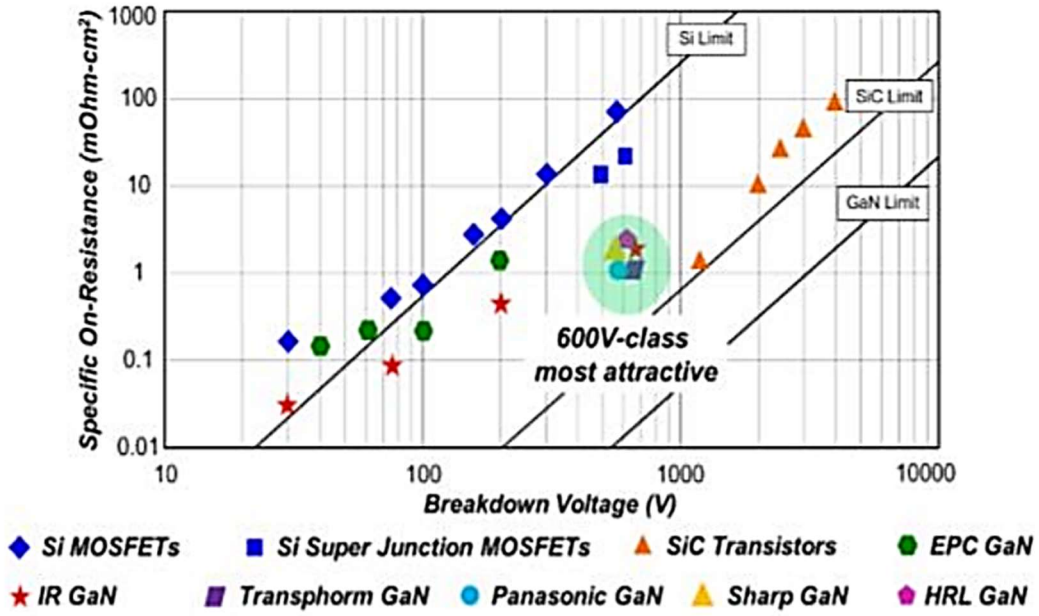


Figure 1.3.2: Theoretical specific on-resistance limits of Si, SiC and GaN devices vs breakdown Voltage[17]**.**

1.4 Bidirectional GaN switches and applications

A bidirectional power switch (BPS), also namely an AC-switch or four-quadrant switch (FQS) in literature, can support bidirectional on-state current and block voltages of both polarities in the off-state[18][19]. Traditional BPS is made with two MOSFETs in series or two quadrants IGBT with didoes. The integration limitations of MOSFETs/IGBTs are mainly caused by their vertical structure, which makes it highly challenging to place two FETs on a single chip and optimise the voltage ratings of devices with cost, on-state resistance and voltage ratings of approximately 30V and above. The lateral structure of GaN HEMTs and the absence of body diodes make it relatively easy to create a monolithic bidirectional GaN switch (Bi-GaN).

In 2007, Panasonic proposed the monolithic dual-gate AlGaN/GaN bidirectional switch using normally-off Gate Injection Transistors (GIT)[20]. In 2022, Innoscience launched the 40V bidirectional GaN device platform and successfully imported the normally-off bi-directional GaN-on-silicon HEMT with a single gate into Oppo and Realme mobile phone motherboards for efficient and more compact over-voltage-protection (OVP) systems. The on-state resistance is only 4.8mΩ with the 2.1mm*2.1mm package size. Compared with back-to-back connected NMOS MOSFETs, Innoscience Bi-GaN HEMTs reduce the size by 64% and the peak power heating by 85%[21]. In the following two years, the family of Innoscience Bi-GaN expanded, and new products had lower on-state resistance, higher breakdown voltage, and smaller package sizes. The low threshold voltage is one limitation of Bidirectional switch configurations based on normally-off GaN HEMT technology.In 2023, Transphorm demonstrated 60mΩ GaN-based integrated BPS assembled in a TO247 package. It consists of a bi-directional normally-on back-to-back GaN die and two low-voltage Si MOSFETs to achieve the normally-off behaviour. The threshold voltage of Transphorm's Bi-GaN switch, depending on MOSFET, is up to 4V to meet the high threshold requirements of some applications. Compared with the state-of-art SiC BPS, it has excellent figures of merit and 60% lower switching loss [22].

The typical IV characteristic of monolithic dual-gate Bi-GaN and IGBT-based bidirectional switches is shown in Figure 1.4.1. The bidirectional switch is enabled by only a single GaN device with dual gates, while a total of four devices by two IGBTs and two Fast Recovery Diodes (FRDs) are required for the conventional one. It is an obvious difference in Figure 1.4.1 that there are offset voltages in on-state current in both directions for IGBT-based bidirectional switches, while monolithic Bi-GaN does not have. The offset voltage is caused by the voltage drop of FRDs, which increases the switching loss.

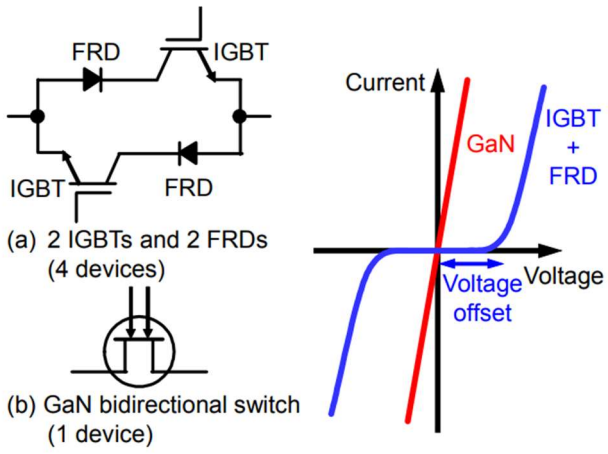


Figure 1.4.1: The typical IV characteristic of (a)monolithic GaN and (b)IGBT-based bidirectional switches[23]

Figure 1.4.2 compares Navitas's Bi-Directional GaNFast Power IC announced in 2024 with IGBT/MOFET-based BPS. Monolithic Bidirectional GaN switches have the smallest size, lowest switching loss, highest switching frequency, and lowest cost.

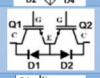
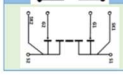
Switch Configuration	Description	Chip area / Size / Complexity	Number of Components	ON-state Voltage Drop	Switching Loss	Switching Frequency	Gate Control Complexity
	Diode bridge + asymmetric IGBT	Very high	5	3.5V [2 diodes + 1 IGBT]	High	16kHz	Low
	Asymmetric IGBT + freewheeling diodes	Very high	4	2.5V [1 diode + 1 IGBT]	High	16kHz	Low
	Back-to-back reverse-blocking IGBTs	High	2	2.0V [1 symmetric IGBT]	Very high	8kHz	Medium
	Si power MOSFETs + JBS diodes	High	4	1.25V [1 diode + 1 MOSFET]	Low	60kHz	Low
	Back-to-back SiC power MOSFETs + antiparallel and series JBS diodes	Very high	6	1.25V [1 diode + 1 MOSFET]	Low	100kHz	Medium
	Four-terminal SiC monolithic BiDFET	Medium	1	0.5V [1 BiDFET]	Low	100kHz+	Medium
	Monolithic bi-directional GaN power IC	Lowest	1	0.5V [1 Bi-directional GaN power IC]	Lowest	500kHz+	Medium

Figure 1.4.2: The comparison of bidirectional switch configurations[24]

BPS can be used in a variety of power conversion applications, such as power inverter, DC-DC/AC-DC/AC-AC converters, matrix converters, solid-state circuit breakers, Current Source Inverter Systems (CSI), Voltage Source Inverter (VSI), charge and discharge of energy storage system[20]. Among them, BPS is mainly used in matrix converters and solid-state circuit breakers as the most critical component. The matrix converter is a utility model relating to a direct conversion type AC-AC power conversion device, which can reduce operating losses in traditional two-stage AC-DC-AC conversion. The 3x3 matrix converters are used to drive three-phase motors. For 3x3 matrix converters, nine bidirectional switches are arranged in three rows and three columns, as shown in Figure 1.4.3.

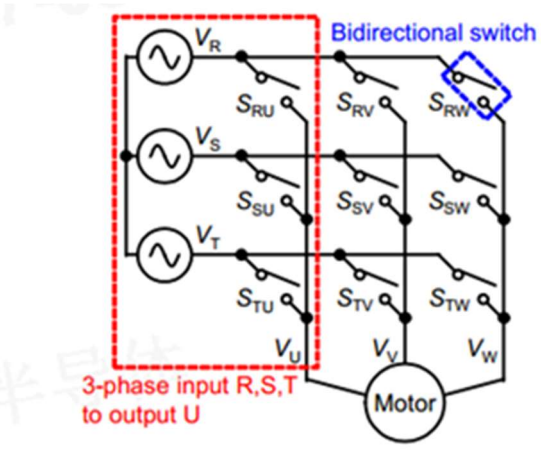


Figure 1.4.3:The 3x3 matrix converter with nine bidirectional switches[25]

Solid state circuit breakers (SSCB) are mainly used in DC power distribution systems in data centres, office buildings, ships and other fields. Compared to mechanical circuit breakers, SSCB using BPS can interrupt fault currents more quickly and protect electrical equipment connected to the power system from short circuit obstacles. The BPS in SSCB is employed to interrupt the current in both directions. Small on-state resistance (Rdson) to reduce on-state loss is an essential indicator for BPS. The schematic diagram of SSCB with a bidirectional switch is shown in Figure 1.4.4.

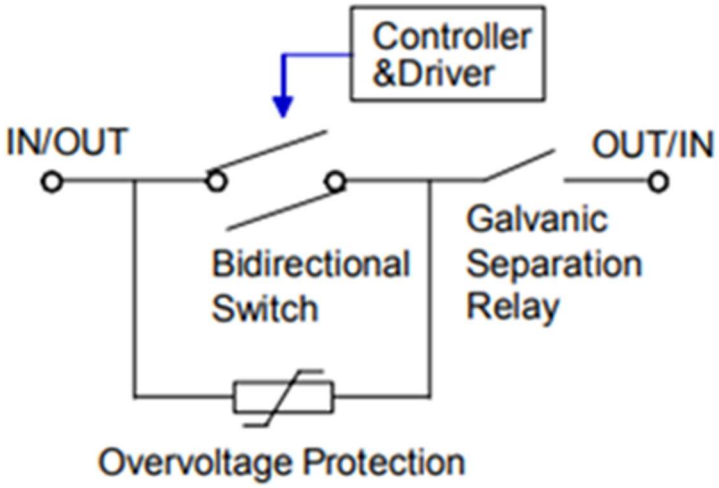


Figure 1.4.4: Schematic diagram of SSCB with a bidirectional switch[26]

1.5 Objectives of this Research Work

In modern power applications, bidirectional power switches are significant components of matrix converters, state circuit breakers, etc. Bidirectional GaN switches (Bi-GaN) have received high attention in recent years and. Due to excellent material properties and lateral device structure without a body diode, it is easier to fabricate monolithic Bi-GaN with a small size, low switching loss, high breakdown voltage, high switching frequency, and low cost. Bi GaN are promising to replace MOSFET/IGBT-based BPS.

For safety reasons, the BPS must be normally off. There are two main routes for GaN. One is using normally-off GaN HEMT. The advantage is that it only use a single die can enable the bidirectional behaviour. By sharing the drift region, the monolithic GaN BPS can achieve ultra-low Rdson in a small size. However, it is limited by immature technology, especially fabrication. In addtion, the threshold voltage of present BPS using normally-off GaN is around 1.5V. It is not high enough when the device is working in a high-power application or cluttered environment.

Another route for BPS is based on the normally-on GaN technology. The typical bidirectional can be seen as two conventional D-mode AlGaN/GaN back to back connected in common drain. By connecting a low-voltage MOSFETs in each source terminal, the normally-off behaviour can be realized. Silimar to Cascode,the threshold voltage of BPS depends on that of MOSFET and can be over the 3V. Similar to convential AlGaN/GaN HEMTs, the bidirectional normally-on GaN HEMTs face many issues, such as current collapse and the lack of high-voltage capability. The Polarisation Super Junction(PSJ) concept proposed in 2006 is a effective electric field management, which can effectively to push the high voltage breakdown and relieve the current collapse by relaxing the crowding electric for high voltage GaN devices.

In this research, the compact monolithic normally-on bidirectional GaN HEMT using PSJ concept(Bi PSJ HFETs) is investigated. Based on two structure such as Bi PSJ HFETs with Schottky gate and with ohmic Gate, it cancels the common drain electron, which is one of the most compact bidirectional switches reported to date. By simulation and measurement, electrical characteristics successfully validates the Bi PSJ HFETS concept and functionality with different gate polarity control. Accurate analytical models of the on-state resistance for Bi PSJ HFETs at room temperature are built to calculate and analyze their components. Analytical models will promote an understanding of the mechanism of Bi PSJ HFETs. In addition,it is noticed that first time to design and fabricate large-area Bi PSJ HFETs in wafer level on the 6’ Sapphire substrate.

In order to construct the thermal analysis model of PSJ devices in the future, the on-state behaviour of Ohmic contact, PSJ Schottky and unidirectional PSJ FETs as the function of temperature is analysed based on a large number of experimental data. These results are critical for further improvement of on-state performance for unidirectional and bidirectional PSJ HFEMTs.

According to the experiment results of test structure and large-area Bi PSJ HFETs, there is a obvious gap. Parasitic impedances (R, L&C) of layouts for large area devices influence on-state resistance, switching speed, propagation and phase delays. It is necessary to reduce and allocate parasitic impedance reasonably for achieving a uniform current and temperature distribution as well as reducing the oscillatory behaviour when switching. In this research , it introduces 5 layout schemes, such as typical multi-finger layout, Multi-finger Drain-Source-Drain(D-S-D) Layout, Multi-finger Source-Drain-Source Layout (S-D-S), Checkerboard layout and Hexagonal-shaped layout. In order to comparison, 3D models for 1A unidirectional PSJ HFETs with 10um PSJ length with 5 layouts are built and simulated by ANSYS 3Q. The induced parasitic parameter of different layouts are extracted and compared with advantages and disadvantages.

1.6 Thesis Organization

The thesis is organised as follows:

Chapter 1: A brief comparison of Si versus WBG materials is provided. GaN devices have attracted the most attention in research among WBG materials because of their outstanding properties, and the GaN market grew rapidly. The present bidirectional GaN devices is introduce and compared with MOSFET/IGBT-based BPS.

Chapter 2: GaN's unique polarisation effect as well as its fundamental properties are presented. The formation of the 2DEG in an AlGaN/GaN heterostructure is thoroughly described, and the AlGaN/GaN High Electron Mobility Transistor (HEMT) technology's operating principles are then presented. The PSJ concept was introduced, which included constructing PSJ structures, forming 2DEG and 2DHG, and advancing PSJ technology to overcome challenges with AlGaN/GaN HEMTs. Traditional bidirectional switch configurations using MOSFET and IGBTs are introduced as their operation principle. It also display different implementations for bidirectional GaN switches as well as benefits and disadvantages. The electrical characteristic of bidirectional PSJ HFETs with the floating drain electrode are shown in this chapter.

Chapter 3: In this chapter it propose the compact monolithic bidirectional PSJ device (Bi PSJ HFETS) without floating electrode in the meddle. The structure and equivalent circuit of compact Bi PSJ HFETS with Schottky Gate and Ohmic Gate are shown. By simulation, electrical characteristics successfully validates the Bi PSJ HFETS can realize the bidirectional behaviour. At the end of the chapter, it displays mask design for fabricated Bi PSJ HFETs and overall process flow.

Chapter 4: The fabricated test structure and large-area Bi PSJ HFETs with Schottky and Ohmic Gate at the wafer level are shown in this chapter, as well as their electrical characteristic. Experiment data validates the Bi PSJ HFETS concept and functionality with different gate polarity control. The on-state resistance of Bi PSJ HFETs as the function of PSJ length and temperature are analysed. Accurate analytical models of the on-state resistance for Bi PSJ HFETs are demonstrated which fits well with the experimental data at room temperature.

Chapter 5: Investigation of on-state resistance as the function of temperature can be helpful to analyze and construct the thermal analytical models of on-state resistance in the future. This chapter evaluates different components of Test Element Group (TEG) FETs as a function of different temperatures. According to the a lot experiment data, the ohmic contact for AlGaN/GaN, the on-state performance of PSJ Schottky diode and on-state resistance of PSJ FETs are discussed with the temperature.

Chapter 6: There is gap of electrical characteristics between test structure and large-are Bi PSJ HFETs due to the parasitic impedance of layouts and its no-uniform distribution. In this chapter, it introduce the influence of parasitic impedance for the large-area devices. There are 5 layout designs are introduced and its 3D model designed for 1A large-area PSJ HFETs are shown in this chapter. The active region, parasitic resistance and inductance for 5 layouts are extracted and compared.

Chapter 7: A fair summation and future research work will be included in this chapter.

Chapter 2: GaN-Base Polarisation Super-Junction Technologies

The physical features of GaN and its polarisation effect will be covered in this chapter. High electron mobility transistor (HEMT) technology based on conventional GaN will be reviewed, along with its critical electrical characteristics and limitations. The concept of polarisation super-junction (PSJ) is discussed in this section, which is used to overcome the electric field management issues of traditional GaN-based HEMTs and improve the trade-off relationship between Ron.A and BV. Finally, previous bidirectional switch implementations and monolithic bidirectional devices are present.

2.1 Fundamentals of Gallium Nitride Technology

2.1.1 Crystal structure of Gallium Nitride

In 1969 Maruska and Tietjen used a hydride vapour phase epitaxy (HVPE) method to synthesize GaN for the first time[27]. In 1991, A high-quality and uniform GaN film on the sapphire substrate was directly grown by Nakamura using a Metalorganic Chemical Vapour Deposition (MOCVD) route([28],[29]).

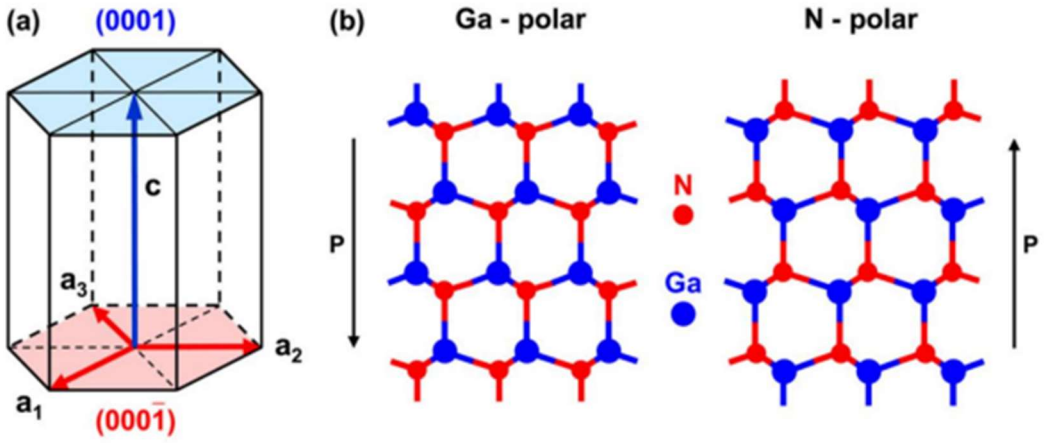


Figure 2.1.1: Schematics of wurtzite Gallium-face GaN and Nitride face GaN crystal structure with a spontaneous polarization (P) [21].

As the III-V nitride materials, GaN has three different crystal structures: wurtzite-type, Zinc blende and Rock salt[30]. Usually wurtzite-type GaN is usually for the fabrication of power semiconductor devices to support the thermodynamically stable structure under standard conditions

([10],[31]). Wurtzite-type GaN has an asymmetrical Hexagonal Closed-Packed (HCP) structure with two distinct cut faces, namely the Gallium (Ga) face (grown along [0001] direction) and Nitride (N) face (grown along [000$\bar{1}$] direction), which is perpendicular to C-axis. Here, the C-axis refers to a specific direction in the GaN crystal structure, that is, the direction indicated by the lattice constant C shown in Figure 2.1.1(a). The C-axis is perpendicular to the basal plane in wurtzite structures[31]. The (0001) cleavage plane of GaN, also known as the C-axis cleavage plane, is the most stable surface of GaN crystal structure. It has the lowest surface energy, so it is easier to form during growth and preparation. Ga-face (grown along [0001]direction) can be obtained by growing over the c-plane sapphire substrate by MOCVD, while N-face can be raised by using Molecular Beam Epitaxy (MBE) under some specific preparation[32]. The different cut face leads to other electrical characteristics.

2.1.2 Polarization effect

In a binary compounded semiconductor, a chemical bond is established between two distinct atoms. The formation of dipoles in the atomic bond is a result of a difference in their electronegativity. Similarly, Ga-atom and N-atoms in wurtzite-type GaN have the opposite polarity. N-atom is more electronegative than Ga-atom. Therefore, a specific polarisation called spontaneous polarization (P_{SP}) is generated along the C-axis in the absence of the external strain([33],[34],[35]). Figure 2.1.1 shows the asymmetrical hexagonal structure of (a) Ga-face GaN and (b) N-face GaN crystal structure with the spontaneous polarization (P_{SP}) [36].

As shown in Figure 2.1.1, the black ball is Ga-atom, while the grey ball stands for N-atom. The σ represents polarization-induced charge density. The plus and minus signs of σ represent the positive and negative charge polarity, respectively. The direction of the spontaneous polarization depends on the crystal growth direction. For Ga-face, the spontaneous polarisation points to the substrate along [0001] direction. On the contrary, the direction of the spontaneous polarization is oriented along [000$\bar{1}$] direction[34]. Figure 2.1.2 shows the spontaneous polarization of GaN, InN and AlN with their lattice constant.

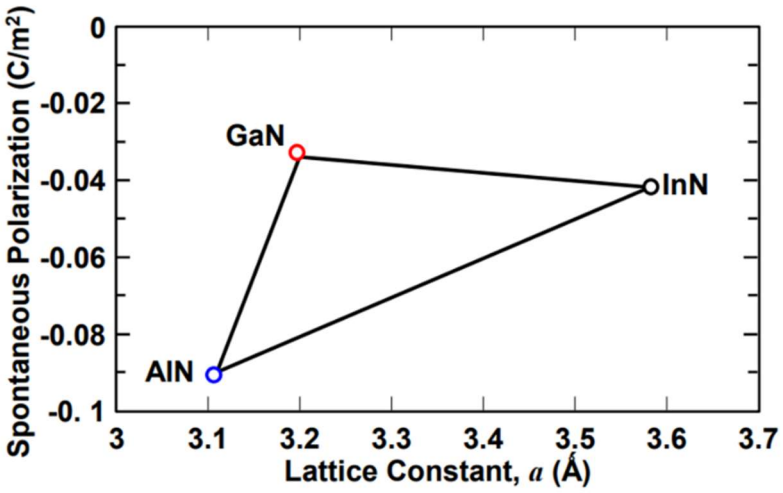


Figure 2.1.2: The spontaneous polarization of GaN, InN and AlN[36].

Due to inside mechanical stress, heterostructures with various lattice constants generate an additional type of polarisation termed piezoelectric polarisation (P_{PE}). Hence, piezoelectric polarisation is related to in-plane strain and reliant on lattice mismatch[31]. Compressive or tensile stresses make the piezoelectric polarization polarity to be positive or negative([37],[38]). Figure 2.1.3 shows the theoretically calculated piezoelectric polarization for AlGaN, InGaN and AlInN over GaN substrate versus molar fraction X by Ambacher et al[33]. The lattice constant of AlGaN, InGaN, and AlInN is dependent on the mole fraction of X. The lattice mismatch between the ternary alloy and the GaN layer varies with varying mole fractions of X, which affects the mechanical strain and magnitude of the piezoelectric polarisation charge density.

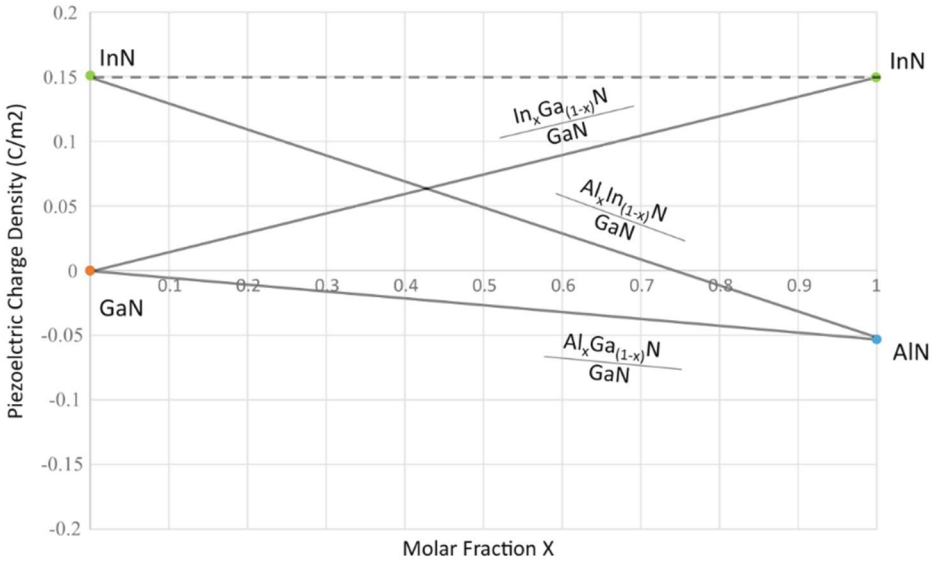


Figure 2.1.3: Theoretically calculated piezoelectric polarization charge density for $Al_xGa_{1-x}N$, $In_xGa_{1-x}N$, and $Al_xIn_{1-x}N$ over GaN substrate, as a function of the mole fraction x[31].

The top and bottom layers of heterogeneous structures have different magnitudes of spontaneous and piezoelectric polarization, which results in a fixed polarization charge called a polarization-induced sheet charge(σ) at the hetero-interface. Thus, polarization-induced sheet charge (σ) can be expressed by Equation(2.1):

$$\sigma = \Delta P \qquad \text{------(2.1)}$$

Where ΔP stands for the polarization gradient in spac.

The density of polarization-induced sheet charge (σ) at an abrupt interface of a heterostructure can be expressed as the following[34]:

$$\sigma = P_{top\ layer} - P_{bottom\ layer} = (P_{SP(top\ layer)} + P_{PE(top\ layer)}) - (P_{SP(bottom\ layer)} + P_{PE(bottom\ layer)}) \qquad \text{------(2.2)}$$

Here, $P_{SP(top\ layer)}$ ($P_{SP(bottom\ layer)}$) and $P_{PE(top\ layer)}$ ($P_{PE(bottom\ layer)}$) are the spontaneous and piezoelectric polarization present in the top (bottom) layer of the heterostructure.

Figure 2.1.4 demonstrates the spontaneous polarization (P_{SP}) and piezoelectric polarisation (P_{PE}) in AlGaN/GaN heterojunctions under different conditions, as well as how polarization-induced sheet charges affect the flow of the flowing electron. As previously mentioned, crystal growth direction decides the direction of spontaneous polarisation. Whereas tensile or compressive strain dictates the polarity of piezoelectric polarization. Spontaneous and piezoelectric polarisation in the AlGaN and GaN layers creates fixed polarisation charges at the AlGaN/GaN heterointerface[23].

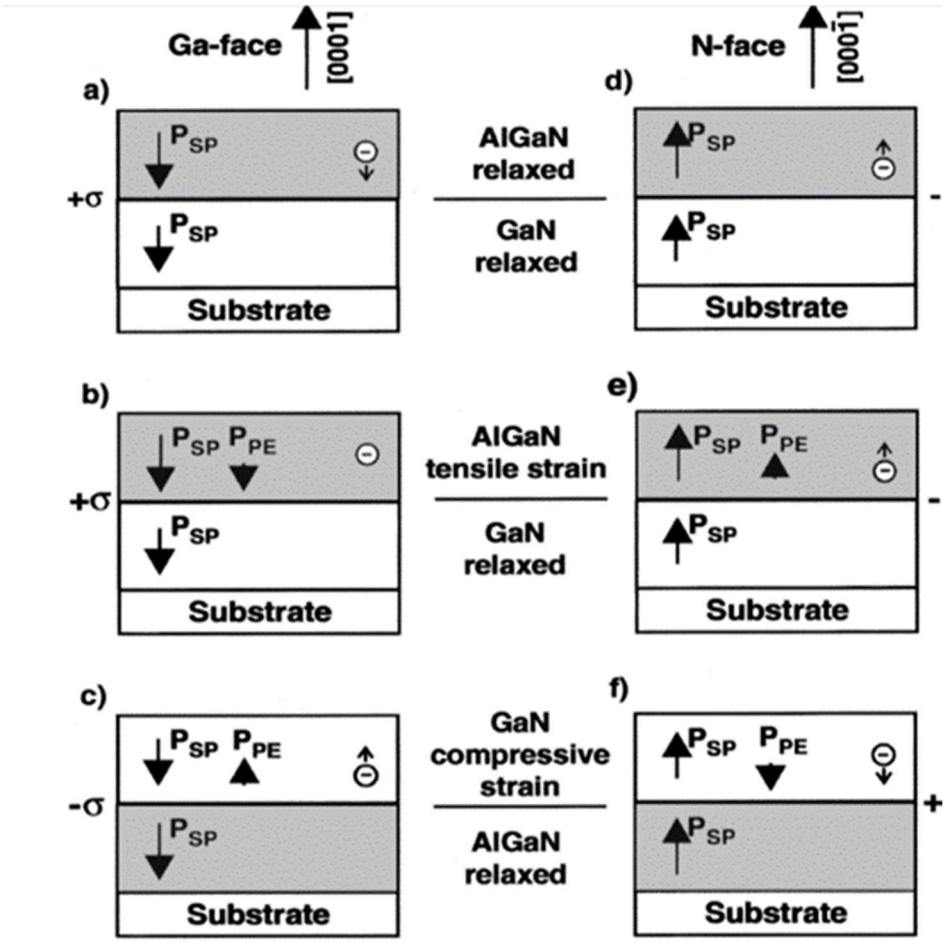


Figure 2.1.4: The spontaneous, piezoelectric polarization and polarization-induced charge density in AlGaN/GaN heterostructures[34]**.**

2.1.3 The formation of 2DEG and 2DHG

As shown in Figure 2.1.4(a),(b) and (f), when the polarization-induced sheet charge density (σ) is positive at the hetero-interface, it attracts and accumulates free electrons for compensation. As a result, at the hetero-interface, two-dimensional electron gas (2DEG) is formed. On the other hand, two-dimension hole gas (2DHG) is developed when the polarisation-induced sheet charge density (σ) is negative because free electrons concentrate and flow away hetero-interface, as shown in Figure 2.1.4 (c),(d) and (e).

For AlGaN/GaN-based devices, the GaN layer can be considered fully relaxed ($i.e\ P_{PE(GaN)} = 0$) because its thickness is several orders of magnitude greater than the AlGaN layer, similar to the example shown in Figure 2.1.4 (b). The polarisation-induced sheet charge density (σ) can be formed by:

$$\boldsymbol{\sigma = P_{AlGaN} - P_{GaN} = (P_{SP(AlGaN)} + P_{PE(AlGaN)}) - P_{SP(GaN)}} \quad \text{------ (2.3)}$$

According to Figure 2.1.3, $P_{SP(AlGaN)}$ is large than $P_{SP(GaN)}$. Therefore, it will be a positive polarization charge at the AlGaN/GaN interface.

2.1.4 2DEG properties in AlGaN /GaN Heterostructures

The existence of 2DEG is a consequence of the polarization effect and the considerable difference in conduction bands between GaN and AlGaN, which is a significant and unique property.

Figure 2.1.5 illustrates the energy band diagram of an undoped AlGaN/GaN heterojunction with the 2DEG channel. On the left is AlGaN layer having a slightly broader band gap, whereas on the right is GaN with a narrower band gap. The difference in conduction band energy induces a conduction band offset, which results in the formation of the quantum well.

Due to the polarization effect, positive polarization charges are induced at the AlGaN/GaN interface, while negative polarization charges are generated on the other side of the AlGaN layer. These differently charged areas form an electric field inside the AlGaN layer. When free electrons are attracted and accumulated to compensate for positive polarization-induced charges, they diffuse from the AlGaN layer to the narrower band-gap GaN layer, then trapped in a quantum well by the potential barrier**[39]**, as shown in Figure 2.1.5. 2DEG reduces impurities and the coulomb scattering. As a result, electrons in 2DEG region have high density and extreme mobility. Based on this unique characteristic, 2DEG is critical in developing GaN-based HEMT architecture as a considerable candidate for carriers.

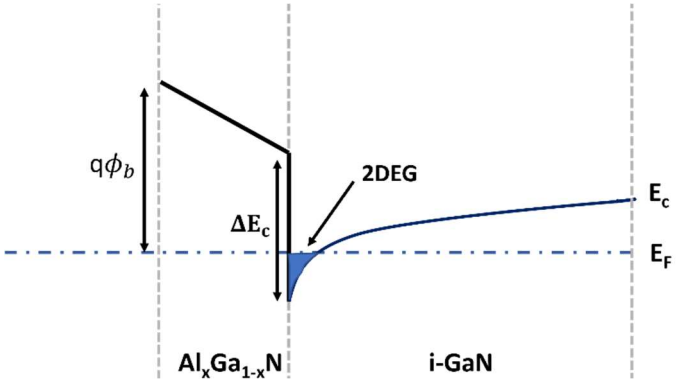


Figure 2.1.5: The energy band of an undoped AlGaN/GaN heterostructure with 2DEG.

In 1992, the presence of a two-dimensional electron gas (2DEG) was first confirmed in the unintentionally doped AlGaN/GaN hetero-interface by M.A. Khan et al. And its steplike features were observed by the quantum Hall effect[40]. In this report[40], the mobility of 2DEG at room temperature was measured to be 834 cm^2/Vs for the $Al_{0.13}Ga_{0.87}N$/GaN heterostructure. After increasing to 2626 cm^2/V at 77K, 2DEG mobility became saturated. The mobility remains mostly constant when the temperature is from 77 to 4.2K. 2DEG density was measured to be 2.6 x $10^{12}cm^{-2}$ at 7K.

In the past three decades, much worthy research has been done on 2DEG transport properties in AlGaN/GaN heterostructure. It has been proven that the low-temperature sheet carrier density (N_s) of 2DEG in AlGaN/GaN depends on the thickness and alloy composition X of the AlGaN layer. Smorchkova et al. reported that 2DEG begins to form in the $Al_{0.27}Ga_{0.73}$ N/GaN only when AlGaN barrier thickness exceeds 3nm at 13K, as shown in Figure 2.1.6[41]. The density of 2DEG grows with increasing AlGaN thickness until it reaches a value near to the polarization-induced charge density. When the AlGaN thickness exceeds a certain threshold, the AlGaN layer relax via cracking under tensile strain, thereby reducing the 2DEG density.

The Al mole fraction determines the band-gap and lattice constant of AlGaN. The piezoelectric polarization and barrier height increase when the Al mole fraction increases. Figure 2.1.7 shows the approximately linear relationship between the sheet density of 2DEG versus Al mole fraction at 13K temperature in 31nm-thick AlGaN layer. The growth rate is about 5.45 x 10^{13} cm^{-2} when the composition x of AlGaN is between 0.09 and 0.31[41]. Nowadays, for high-quality AlGaN/GaN-based HFETs, Al mole fraction X is set for AlGaN layer between 0.15 and 0.4. For high Al composition X, it leads to a significant lattice mismatch, surface defects and a large difference in thermal coefficient, which reduces the 2DEG mobility. The sheet density. When X lower than 0.15, electrons are poorly confined as a result of the conduction band offset being tiny[34]. In[42] it was reported that the sheet density of 2DEG in the material have minimal temperature dependence

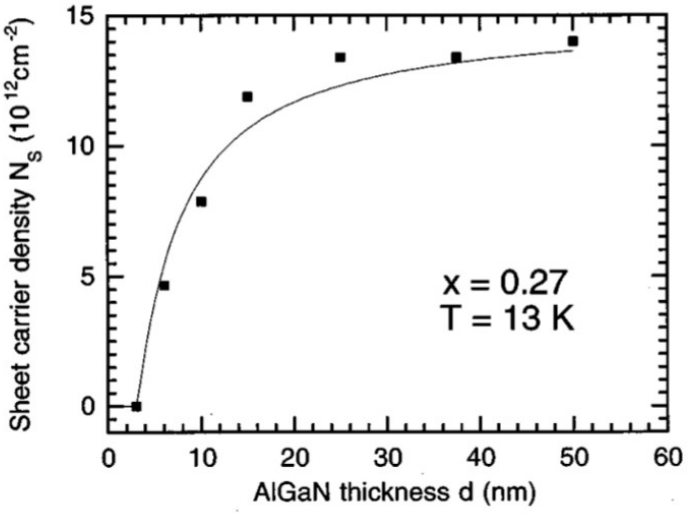


Figure 2.1.6: The sheet carrier density of 2DEG in $Al_{0.27}Ga_{0.73}$ N/GaN versus the AlGaN thickness[41].

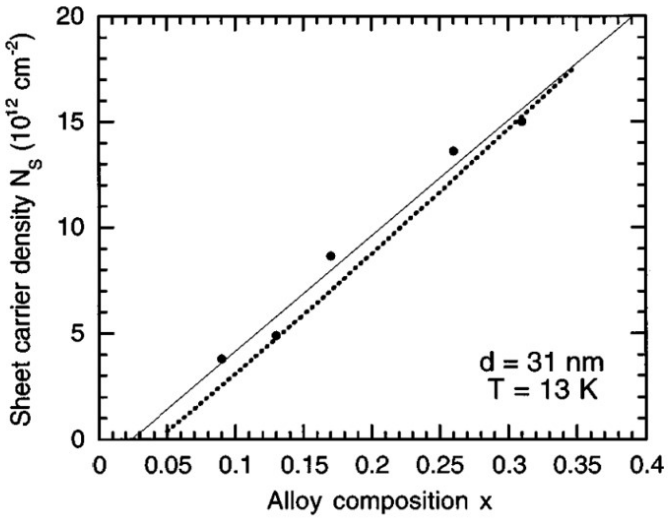


Figure 2.1.7:The sheet carrier density of 2DEG in $Al_xGa_{1-x}N$ as the function of Al mole fraction [41].

The low-temperature electron mobility (μ) of 2DEG in AlGaN/GaN also varied significantly with the AlGaN thickness and Al mole fraction, as shown in Figure 2.1.8 and Figure 2.1.9. The electron mobility (μ) goes down with a thicker AlGaN layer or with higher alloy composition of X, resulting from electrons distributing closer to the heterointerface and becoming more sensitive to the structure imperfections with increasing the electron sheet density. It raises the interface roughness scattering and the alloy disorder scattering, significantly affecting low-temperature electron mobility.

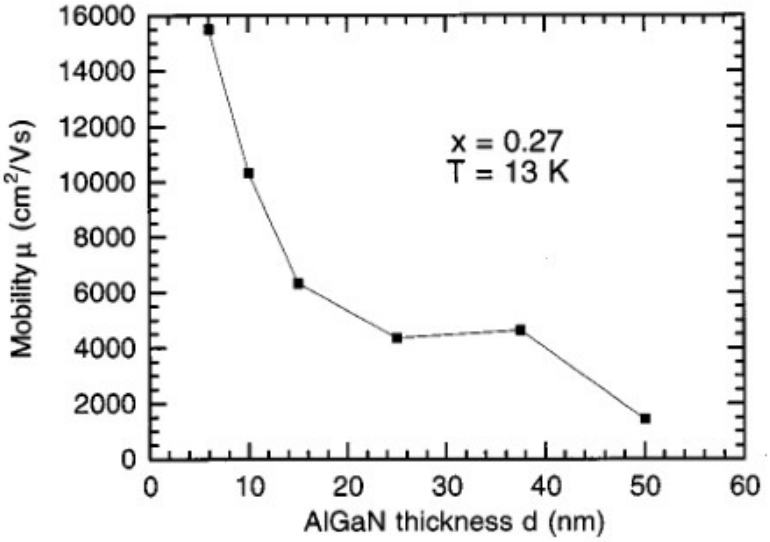


Figure 2.1.8: The low-temperature electron mobility of 2DEG in $Al_{0.27}Ga_{0.73}$ N/GaN versus the AlGaN thickness[41].

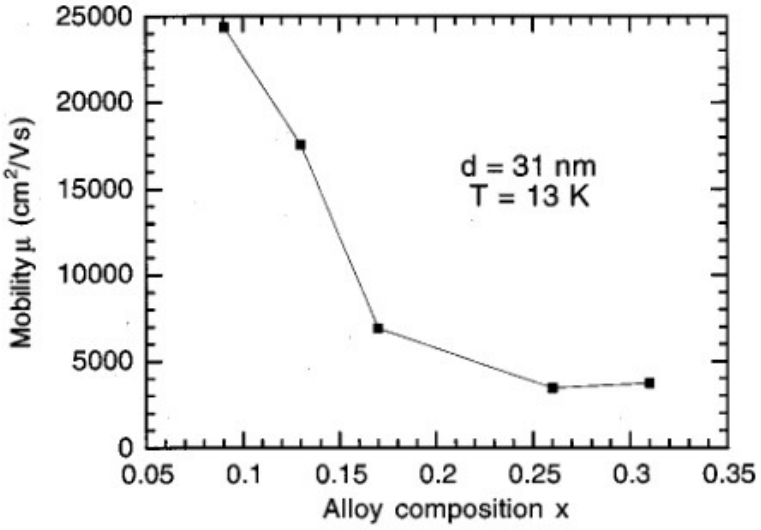


Figure 2.1.9：Low-temperature electron mobility in the 2DEG of $Al_xGa_{1-x}N$/GaN as a function of alloy composition x[41]**.**

At room temperature or higher temperature, three scattering mechanisms, acoustic deformation potential, polar acoustic phonon, and polar optical phonon scatterings, impact the mobility of 2DEG formed at the AlGaN/GaN heterointerface. In [43], it simulates and presents the temperature dependences of the 2DEG mobility limited by each of the three scattering mechanisms and the overall mobility for different carrier concentrations. It can be found in Figure 2.1.10 that polar optical phonon scattering is typically the dominant scattering mechanism at any temperature.

By the Matthiessen's rule, the overall 2DEG mobility limited by the three scattering mechanisms can be calculated by:

$$\frac{1}{\mu} = \frac{1}{\mu_{ADP}} + \frac{1}{\mu_{PE}} + \frac{1}{\mu_{POP}} \qquad \text{------(2.4)}$$

Where μ is overall 2DEG mobility, $\mu_{ADP}$is the mobility limited by the acoustic deformation potential, μ_{PE} is the mobility limited by the polar acoustic phonon, $\mu_{ADP}$is the mobility limited by the polar optical phonon scatterings. In some paper, it only considers the mobility limited by the polar optical phonon and acoustic deformation potential for GaN FETs[44]. The polar acoustic phonon scattering can be negligible since its energy is very low.

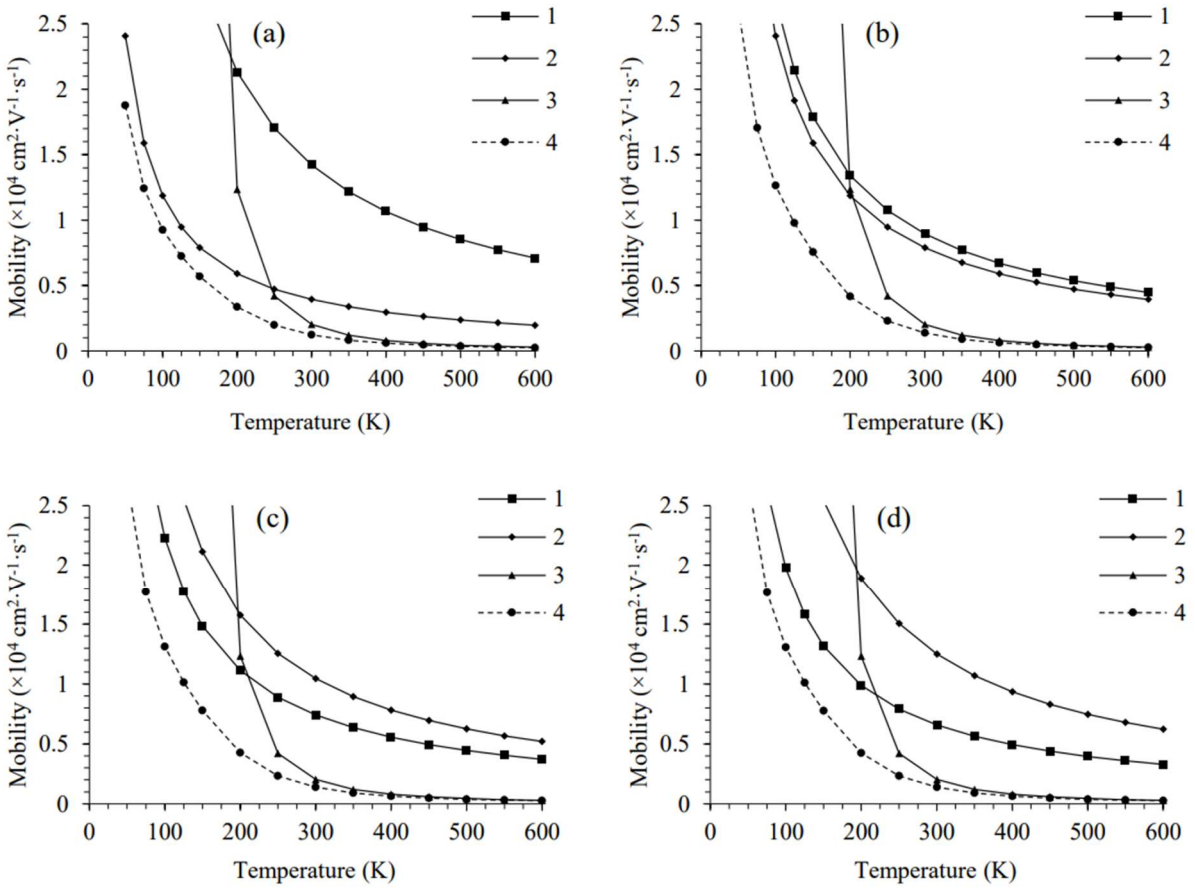


Figure 2.1.10: The mobility of 2DEG with the carrier concentration of (a) 1 x 10^{12} cm^{-2}, (b) 4 x 10^{12} cm^{-2},(c) 7 x 10^{12} cm^{-2} and (d) 1 x 10^{13} cm^{-2} as the function of temperature. (Line 1: acoustic deformation potential scattering; Line 2: polar acoustic phonon scattering; Line 3: polar optical phonon scattering; Line 4: overall mobility)[43]

According to the relationship with the corresponding momentum relaxation time, the mobility limited by one scattering mechanism can be derived by:

$$\mu = \frac{q}{m}\tau \qquad \text{------(2.5)}$$

Where q is the elementary charge, m is the effective mass, and τ is momentum relaxation time.

The momentum relaxation time (τ_{ADP}) due to the acoustic deformation potential scattering is calculated by[45]:

$$\tau_{ADP} = \frac{\hbar^3 v_1^2 \rho b}{m\kappa T \varphi_{AD}^2} \qquad \text{-------(2.6)}$$

where ħ is the reduced Planck constant, v_1 is the velocity of longitudinal acoustic phonon, ρ is the density, b is the effective width of the 2DEG, m is the effective mass, κ is the Boltzmann constant and φ_{AD} is the acoustic deformation potential.

The momentum relaxation time (τ_{POP}) due to the polar optical phonon scattering can be calculated by[46]:

$$\tau_{POP} = \frac{4\hbar^2\pi\varepsilon\left(1-5\frac{V_T}{E_g}\right)\left(\frac{1}{\varepsilon_\infty}-\frac{1}{\varepsilon_0}\right)^{-1}}{qm\left(2q \quad {}_{POP}\left(1+\frac{E_{POP}}{E_g}\right)\right)^{1/2} N_p} \qquad \text{-------(2.7)}$$

where ħ is the reduced Planck constant, ε is the dielectric constant, V_T is the thermal voltage, E_g is the band gap and E_{POP} is the polar optical phonon energy, q is the elementary charge, m is the effective mass. ε_∞ and ε_0 are the relative permittivity at high and low frequency, respectively.

The parameter Np is the phonon Planck function as follows[46]:

$$N_p = \left(exp\left(\frac{E_{POP}}{V_T}\right)\right)^{-1} \qquad \text{------(2.8)}$$

Figure 2.1.11 shows the band diagrams of GaN/AlGaN/GaN heterostructure with a thick GaN cap. When GaN cap layer is thick enough, the 2DHG exists in the CaN /AlGaN interface, as dotted line shown in Figure 2.1.12. With the increasing GaN cap layer thickness, the sheet density of 2DEG goes down from an approximate $1.3 \times 10^{13} cm^{-2}$ to $0.65 \times 10^{13} cm^{-2}$.

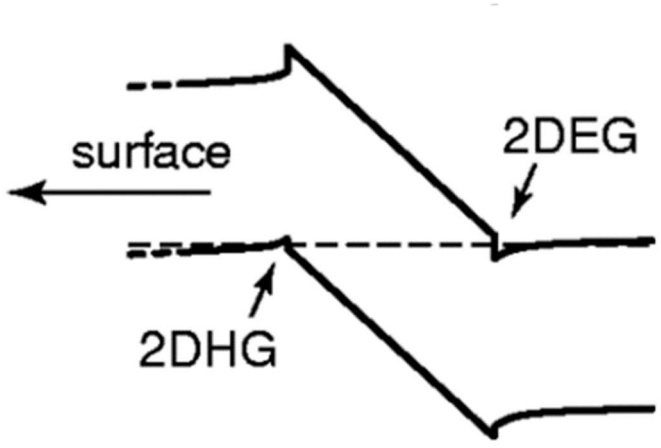


Figure 2.1.11: The Band diagrams of GaN/AlGaN/GaN heterostructure[47]**.**

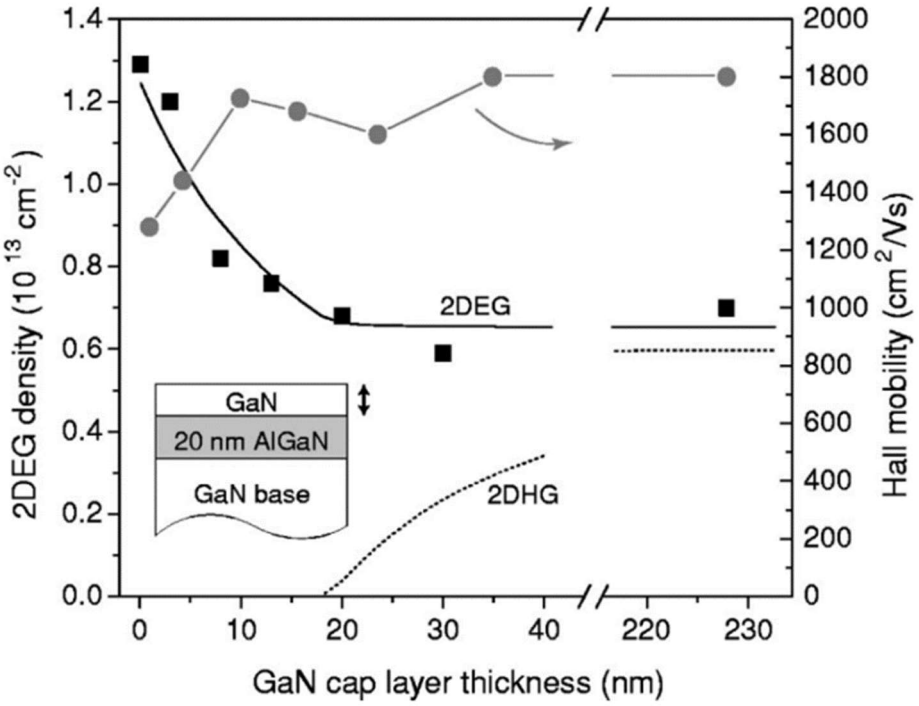


Figure 2.1.12: The influence of GaN cap layer thickness on sheet density and mobility[47].

2.2 AlGaN/GaN-based High Electron Mobility Transistor

In addition to meeting the application requirements, ideal power semiconductors should have three main characteristics. It has minimal on-state resistance, which can conduct a larger current with minimal voltage drop. Second, it has minimal leakage in the off state. Third, it has a fast-switching speed and minimal loss during the transitions. That is what drives people to research and develop new materials, new devices and new technologies.

2.2.1 The structure of conventional AlGaN/GaN-based HEMTs

Based on the superior electron mobility of spontaneously formed 2DEG as well as excellent material properties, AlGaN/GaN-based High Electron Mobility Transistor (HEMT) has been got great attention and developed since the first AlGaN/GaN HEMT was subsequently demonstrated in 1993([48],[14]).

By adopting the high density and high mobility 2DEG as the conduction channel, AlGaN/GaN-based HEMTs are capable of obtaining low resistance, a fast switching speed, and low switching loss. HEMTs based on AlGaN/GaN have a high breakdown voltage because of their outstanding material and electronic characteristics and high off-state breakdown voltage. In most modern power electron

systems, AlGaN/GaN-based HEMTs are exploited for power switching and high-frequency signal amplification.

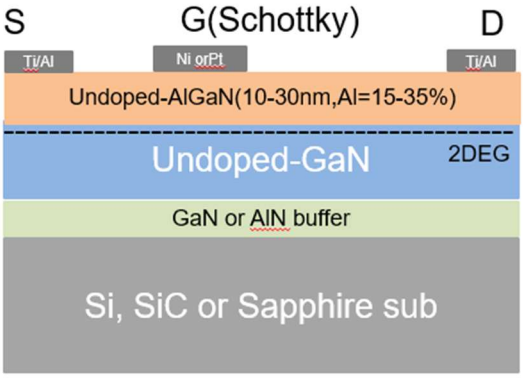


Figure 2.2.1 The cross-section of a general conventional AlGaN/GaN HEMT.

The schematic diagram for normally-on conventional AlGaN/GaN HEMTs is shown in Figure 2.2.1. Typically, $Al_xGa_{1-x}N$/GaN heterostructure consisting of an undoped AlGaN/GaN is grown on a thick non-native substrate like Si, SiC or Sapphire because it is expensive and difficult to obtain native GaN substrates. However, it unavoidably leads to lattice mismatch and stress between GaN and foreign substrate, degrading device performance. It employs the nucleation layer like AlN or GaN to release the strain and improve hetero-epitaxial crystal growth quality. Metal Organic Chemical Vapor Deposition (MOCVD), Hydride Vapor Phase Epitaxy (HVPE) and Molecular Beam Epitaxy (MBE) are technologies used for the epitaxial growth of GaN and $Al_xGa_{1-x}N$ layer. MOCVD is the most widely used technique for GaN-based epi-structures due to its experience and success in developing optoelectronic devices and the high growth rate. MBE is also frequently used to grow III-nitrides. Compared with MOCVD, the whole process of MBE occurs in ultra-high vacuum chambers at low temperatures with a significantly lower growth rate of 1 μm per hour. Consequently, high-purity and quantity films can be grown precisely and flexibly([29], [49], [50]).

During epitaxial growth, 2DEG is spontaneously induced at the interface of $Al_xGa_{1-x}N$ /GaN. $Al_xGa_{1-x}N$ acts as the barrier layer with Al mole fraction X in AlGaN between 15% and 30%, typically. The thickness of $Al_xGa_{1-x}N$ is about 10 ~ 30 nm.

The three electrodes that comprise the three-terminal conventional AlGaN/GaN HEMTs are named the Gate, Source, and Drain electrodes. While the Source and Drain form ohmic contacts to the 2DEG, the Gate electrode forms the Schottky contact to govern the current. Schottky contact with a Schottky barrier height (ϕ_b) forms rectifying junction between metal and semiconductor material. Nickel (Ni) and Gold (Au) is most used to fabricate Schottky contact[51]. The high Schottky barrier

height can reduce leakage. On the other side, the contact resistance of source/drain contact is an important criterion and is always monitored to evaluate ohmic contact and process stability in GaN industry. The ohmic contact should have a much smaller resistance compared with that of the semiconductor device. When the current flows through the device, the voltage drop on the ohmic contact is lower than the voltage drops of the device itself, so it does not affect the IV characteristics of the device. For in ultra-high frequency and high-power GaN devices, ohmic contact is one of the key problems in the design and manufacture. Forming a good ohmic contact depends on the choice of metal material. ohmic contacts, made from Titanium (Ti), Aluminium (Al), Ni and Au, can provide a low-resistance connection between the semiconductor material and the metal drain/source electrode([52],[53]).

2.2.2 Si, SiC and Sapphire substrates for AlGaN/GaN HEMT

Owing to the restrictions of epitaxial techniques, GaN-based devices lack affordable, large-scale, high-quality GaN wafers[57]. Hence, GaN growing on foreign substrates is employed to manufacture GaN power semiconductors. The quality of the GaN epilayer is highly dependent on the substrate's properties and the nucleation layer growth. The substrates for the manufacture of devices are chosen in consideration of the following features:

- lattice mismatch
- Thermal conductivity
- Coefficient of thermal expansion(CTE)
- Cost

Table 2.1 Some of the crucial characteristics of different substrate materials is shown in Table 2.1. The high lattice mismatch and the variation in the thermal expansion coefficients between the epitaxial layer and substrate degrade device performance due to the high density of crystallographic defects, high device leakage current, short minority carrier lifetime, high device leakage current, short minority carrier lifetime and so on[58]. The nucleation layer employing AlN or GaN reduces the lattice mismatch and increases thermal boundary resistance between GaN and foreign substrate. Substrates with higher thermal conductivities speed up heat dissipation during operation, improving the device's performance. GaN-based power devices are typically manufactured on SiC and Sapphire. The majority of efforts have recently been concentrated on silicon substrates([59][60]).

Table 2.1: Intrinsic parameters of substrate materials for AlGaN/GaN-based HEMTs([10],[61]**).**

	Sapphire	SiC	Si	GaN
Lattice mismatch (%)	16	3.1	−17	0
Linear thermal expansion coefficient ($\times 10^{-6}$ K^{-1})	7.5	4.4	2.6	5.6
Thermal conductivity (W cm^{-1} K^{-1})	0.25	4.9	1.6	2.3
Cost	Cheap	Expensive	Cheap	Very expensive
Dislocation density of GaN films grown on substrate (optimized) (cm^{-2})	Low 10^8	Low 10^8	Low 10^8	10^4–10^6

Sapphire (Al_2O_3) has been a common platform for producing GaN-LEDs since the first deposition of GaN grew on Sapphire substrate by HVPE method was successful obtained in 1969 by Maruska and Tietjen[62]. Experience in developing optoelectronic devices, existing infrastructure and mature technologies make the GaN grown on Sapphire substrates much easier. However, it is argued that the lattice mismatch and the difference in thermal expansion coefficient are main causes of stress in the GaN layer at room temperature. During the 2-step growth process for GaN on Sapphire, after the deposition of an approximately 20-nm-thick nucleation layer at 550–700 °C, the water temperature is increased to around 1000 °C for the growth of the main GaN layer[31]. Since the linear thermal expansion coefficient for GaN is $5.6x10^{-6}$/K while for sapphire is 7.5x10-6/K, the wafer is under stress and bowing after cooling down. For a thick GaN film on Sapphire, the stress in Sapphire substrate is always tensile. The stress in GaN film is compressive near the interface while is tensile near the surface, as shown in Figure 2.2.2. The stress causes the wafer to bow or crack. Surface and channelling cracking of sapphire and GaN, sapphire debonding along the interface, and sapphire debonding by spalling are common types of cracks observed when GaN grows on Sapphire[63].

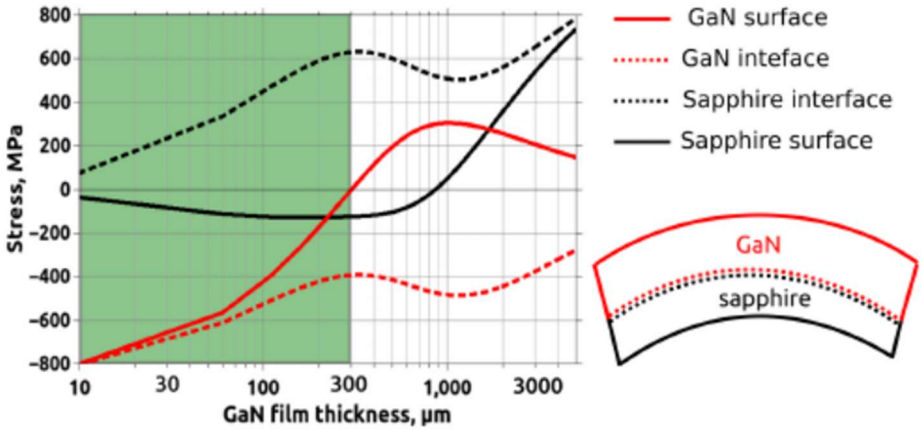


Figure 2.2.2: The stress in a GaN film on a sapphire as a function of the GaN film thickness[63]**.**

Table 2.2 summarises issues of GaN devices based on sapphire substrate and practical solutions. The on

Table 2.2: Challenges and practical solutions of GaN-based derives on Sapphire([2],[55]**)**

Challenge	Issues	Solutions
Lattice mismatch	● Stress near the hetero-interface ● Dislocation ● Reduction in the charge carriers mobility	Use of the nucleation layer
Material defects /dislocation	Deep traps (partly involved in the current collapse mechanism)	Low dislocation density GaN epitaxial growth
A low thermal conductivity	● Self-heating ● A sizeable current reduction due to an increase in the lattice temperature	Flip chip bonding onto a material with high thermal conductivity [2]
The difference of the thermal expansion coefficient	Wafer bowing or cracking due to thermal stress during cooling after growth	The occurrence of cracks and bowing are dependent on GaN film thickness [2]
Sapphire exists in large diameters	The strong wafer bows after cooling	

Silicone carbide has several advantages over other non-native materials as a substrate for GaN epitaxy. SiC is similar to wurtzite-typed GaN with a minor lattice mismatch of 3.1%. With a thin AlN nucleation layer, the lattice mismatch between SiC and GaN can be less than 1 %, easily achieving high-quality GaN-on-SiC epi-structures[64]. On the other hand, SiC has a high thermal conductivity coefficient of about 380W/m.k. It is beneficial in applications where heat dissipation is essential for smaller cooling systems, such as radio frequency equipment for satellite and radar communications. AlGaN/GaN HEMTs were reported to degrade with decreased transconductance and increased on-state resistance because of higher temperatures at high drain voltage operation, even on SiC substrates[65]. In addition, the high cost is one of the limitations.

Silicon is the most widely well- for GaN-based HFETs because of the high quality and the low cost of leveraging readily available large-diameter silicon wafers [66]. Due to its trigonal symmetry, the epitaxial growth of (0001)GaN can grow on the Si substrate. However, the significant thermal mismatch between GaN and Si is one of the issues which leads to cracks and limits the fast process of GaN growth [67]. In addition, the lattice mismatch in Si and GaN is inevitable. When AlN or GaN grows on a Silicon substrate, there are a lot of defects because Si tends to form amorphous SiN[31]. Therefore, the quality of GaN grown on Sillion is significantly lower than that of Sapphire. In the past

year, many studies on the improvement in the quality of GaN on Si substrate have been done, and well-conductin low-cost Si substrate will replace Sapphire and SiC in the future.

2.2.3 Operating principles and characteristics parameters

Figure 2.2.3 shows the conduction band profile of a typical normally-on AlGaN/GaN HEMT under the gate voltage of 0V. The solid line is the conduction band of the AlGaN and GaN layer. The dashed line stands for the Fermi level. As described in Section 2.1.4, a conduction band offset (ΔE_C) due to the difference in the conduction band energies forms and creates a triangular quantum well at the interface of AlGaN and GaN. The triangular quantum well traps the accumulated electrons and forms a 2DEG channel. Without any gate bias voltage (V_g), the device shows the normally-on characteristics, resulting from the spontaneously induced 2DEG providing a conduction channel between Drain and Source. Applying an input signal to the gate can control the on-state current and switch the device.

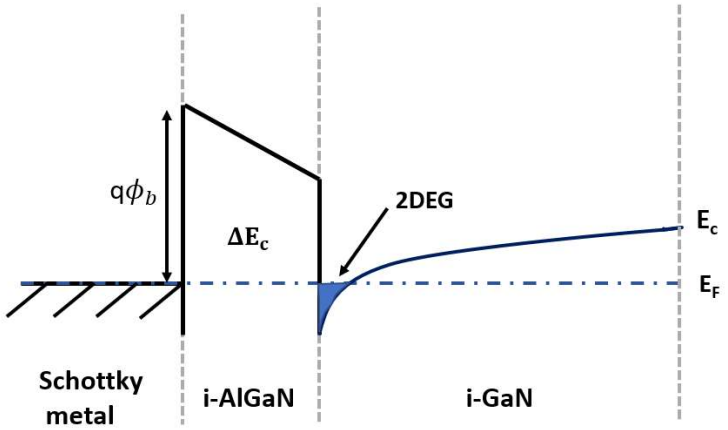


Figure 2.2.3: The conduction band profile of a typical AlGaN/GaN HEMT at Vg=0V.

A normally-on AlGaN/GaN has a negative threshold voltage (V_{th}). V_{th} is defined as the minimum gate voltage value when the device current starts to flow, which can be expressed as the following[10]:

$$V_{th} = \phi_b - \Delta E_C - V_{AlGaN} = \phi_b - \Delta E_C - \frac{qN_s d_{AlGaN}}{\varepsilon_0 \varepsilon_{AlGaN}} \qquad \text{-------(2.9)}$$

Where ϕ_b= Schottky barrier height,

ΔE_C=Conduction band offset between GaN and AlGaN

N_s= The sheet carrier density of 2DEG

ε_{AlGaN}= Relative dielectric constant of AlGaN

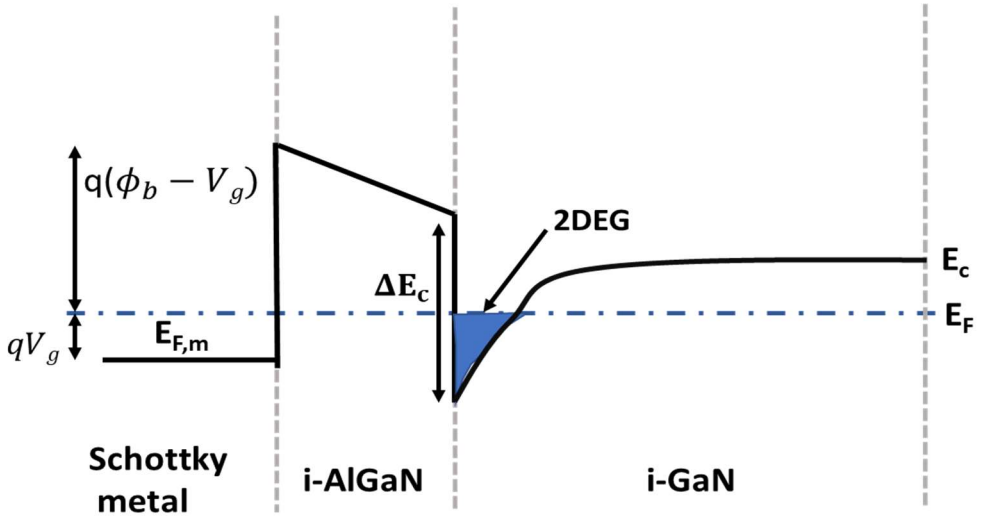
d_{AlGaN}= AlGaN thickness

q= electron charge

From Equation 2.9, the threshold voltage is determined by the Schottky barrier height, thickness and 2DEG sheet density. According to Figure 2.1.6 and Figure 2.1.7, both AlGaN thickness and its alloy composition X affect the sheet carrier density in 2DEG.

When positive gate bias is applied (i.e. V_{gs}>0V), it lowers the Schottky barrier height (ϕ_b) and pull the conduction energy band further down towards the Fermi level (E_F), as shown in Figure 2.2.4(a). The quantum well becomes deeper, so the 2DEG sheet density increases.

When the gate bias voltage is negative (Vth<Vgs<0V), Schottky barrier height (ϕ_b) of Gate metal increases, as well as the conduction energy band goes up forwards the Fermi Level (EF), as shown in Figure 2.2.4(b). Holes from the Gate electrode are injected into 2DEG and recombined with free electrons. The density of 2DEG decreases, as well as the drain current.



(a) Vg>0V

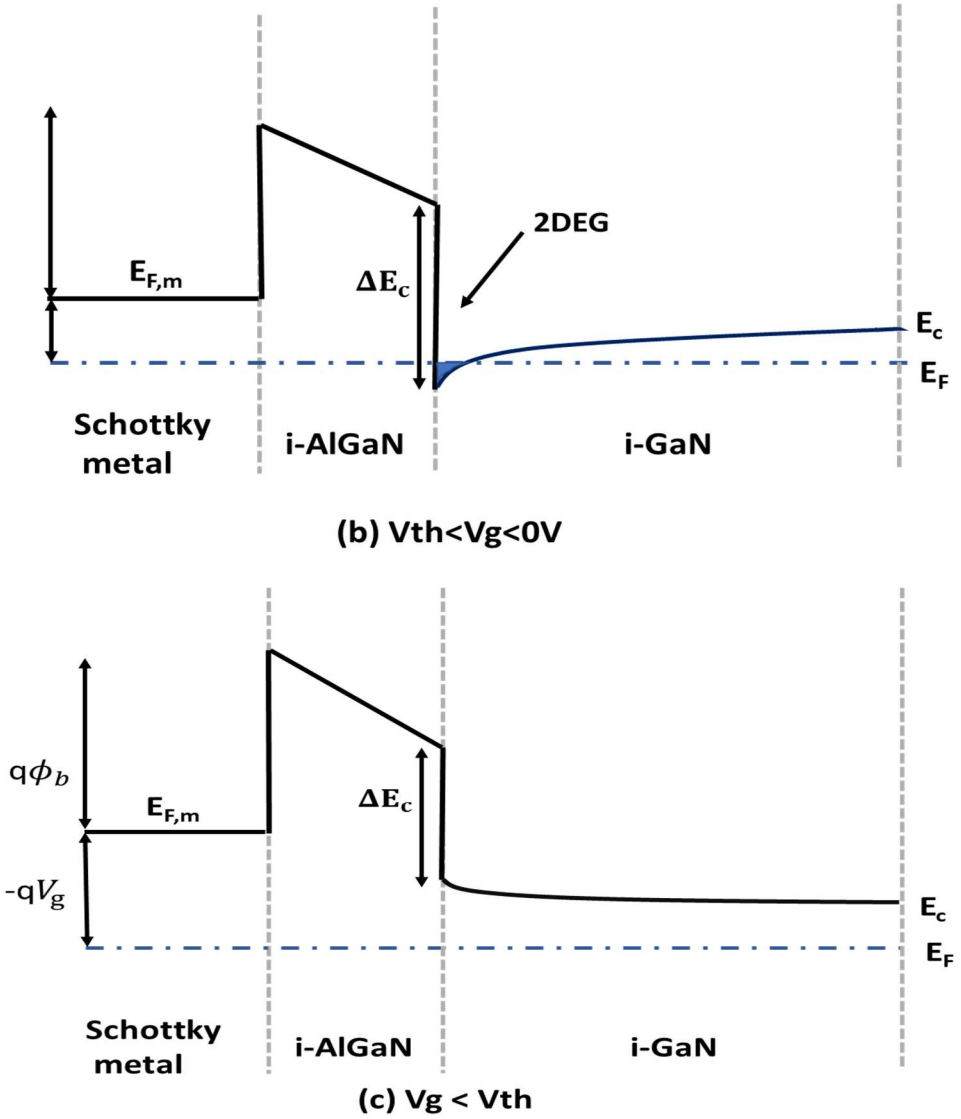


Figure 2.2.4: Conduction energy band diagram of a typical AlGaN/GaN HEMT with varying Gate Voltage (a) $V_g > 0$ (b) $Vth<Vg < 0$ (c) $V_g < V_{th}$

Figure 2.2.4(c) describes the conduction band diagram when the gate voltage falls below the threshold voltage ($V_{gs}<V_{th}$). The 2DEG channel under the gate region is pinched off, which cuts off the current conduction path. Thus the device enters turn-off. The schematic diagrams of a conventional AlGaN/GaN HEMT during off-state are shown in Figure 2.2.5.

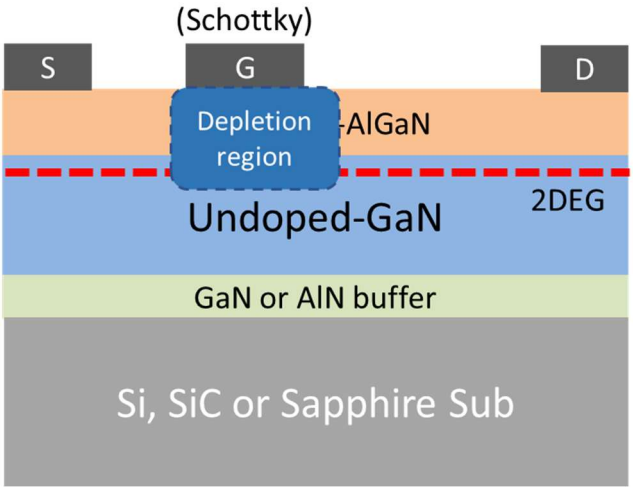


Figure 2.2.5: Schematic Diagrams of a conventional AlGaN/GaN HEMT during off-state.

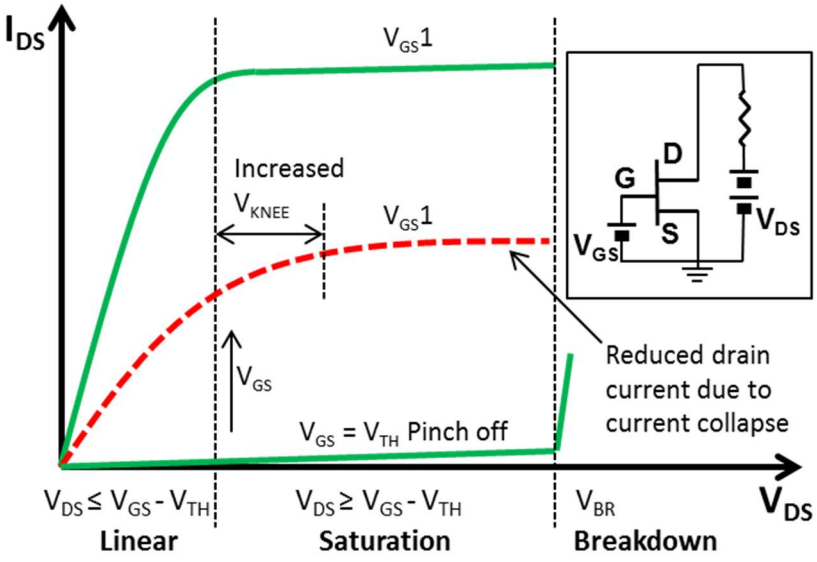


Figure 2.2.6: Schematic electrical characteristics of an AlGaN/GaN HEMT.

Figure 2.2.6 shows schematic output I_{ds}-V_{ds} and off-state characteristics of an AlGaN/GaN HEMT with a common source configuration. As lateral Field Effect Transistors, the IV curves with various Gate Voltage (V_{gs}) values can be divided into linear and saturation regions. According to the model presented by H. Morkoc et al.[54], the electron velocity is directly proportional to the applied electric field with constant mobility in the linear region (i.e. $V_{ds} < V_{gs}$-V_{th}). Hence, the drain current linearly increases in the linear region, which can be expressed as:

$$I_{ds} = \frac{W}{L} \cdot \frac{\varepsilon_{AlGaN}}{d} \left[(V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right] \quad \text{------(2.10)}$$

The on-state resistance (R_{on}) can be extracted during this region. Due to V_{ds} is smaller than $V_{gs} - V_{th}$, the $\frac{V_{ds}^2}{2}$ in Equation 2.10 can be ignored. So Equation of R_{on} can be derived by:

$$R_{on} = \frac{V_{ds}}{I_{ds}} = \frac{V_{ds}}{\frac{W}{L} \cdot \frac{\varepsilon_{AlGaN}}{d} \cdot \mu_{2DEG} \cdot \left[(V_{gs} - V_{th})V_{ds}\right]}$$

$$= \frac{\mathbf{1}}{\frac{W}{L} \cdot \frac{\varepsilon_{AlGaN}}{d} \cdot \mu_{2DEG} \cdot (V_{gs} - V_{th})} \quad \text{------(2.11)}$$

With the increasing drain voltage ($V_{ds} > V_{gs}$-V_{th}), over a certain value of the electric field, carrier velocity is independent of the electric field and becomes saturated. The current I_{ds} can be expressed as in **Error! Reference source not found.**[55]:

$$I_{ds} = \frac{W}{L} \cdot \frac{\varepsilon_{AlGaN}}{d} \cdot v_{sat}\left[\left(V_{gs} - V_{th}\right) - V_{dss}\right] \quad \textbf{------(2.11)}$$

Where v_{sat} stands for the saturation velocity and V_{dss} is the saturation drain voltage.

In addition, the transconductance (g_m) is also a vital parameter in evaluating device performance. Transconductance (g_m) is defined as the drain current change rate in the linear region when Gate voltage changes. The ideal power device has a significant transconductor (g_m) that has a large output current I_d when applying a small V_{gs}. In addition, the switching speed increases with the high transconductance[56]. g_m can be expressed in Equation(2.12)as:

$$g_m = \frac{dI_{ds}}{dV_{gs}}, \text{ at } V_{ds} < V_{dss} \quad \text{-----(2.12)}$$

2.2.4 Electric field management issues

Lateral GaN-based power devices also suffer from challenging topics, such as current collapse, lack of high blocking voltage capability and the lack of avalanche capability.[68].

The major phenomenon of degraded performance in high-voltage GaN HEMTs is current collapse. In the literature, current collapse refers to a phenomenon involving the degradation of drain current and increase in dynamic Ron after applying a high Vds bias. For AlGaN/GaN HEMTs, current collapse is reversible. The reduced drain current can be recoverable by heating or UV light. Figure 2.2.7 shows the Id-Vds characteristics of GaN-based HEMT before (solid lines) and after (dotted lines) current collapse. The mechanism of current collapse is that electrons in 2DEG accumulate in the high electrical field at the drain side of the gate and accelerate to the AlGaN surface, AlGaN barrier and buffer layer. This is then captured by surface/bulk traps, as shown in Figure 2.2.8. The term traps refers to energy

states in the band-gap of a semiconductor. Traps result from several factors, such as crystal defects, dislocations, or impurities.

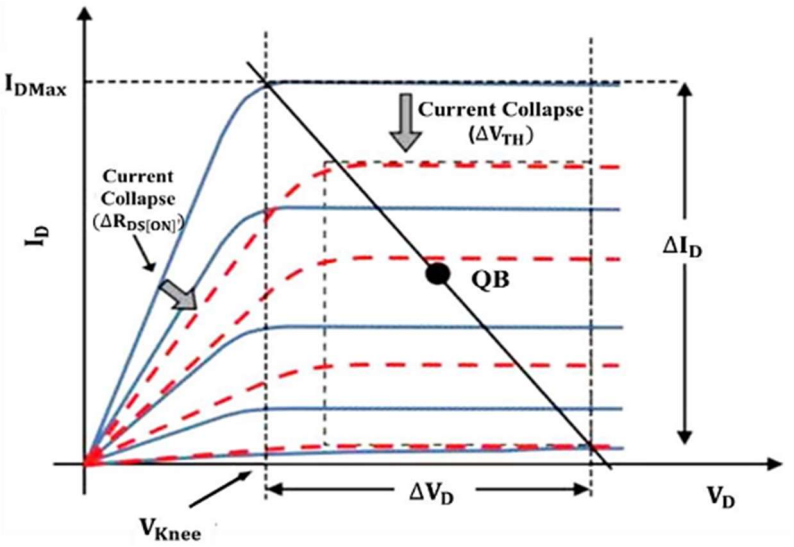


Figure 2.2.7: Current collapse for conventional AlGaN/GaN devices[69].

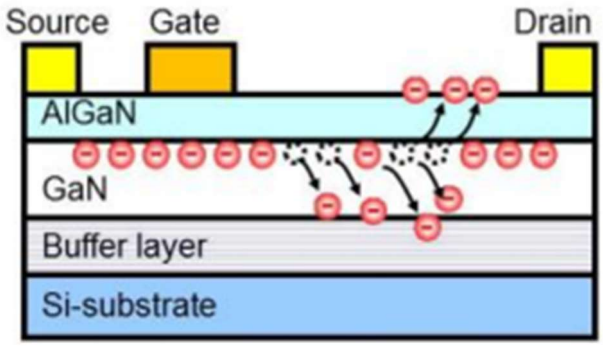


Figure 2.2.8: Schematic illustration of accumulated electrons trapped in the surface/bulk[70]**.**

This gate and drain lag condition of the quiescent bias (QB) are the main parameters used to characterise the current collapse [71]. The corresponding measurement techniques are combined in the pulsed I-V measurements, in which both the gate and drain voltages are pulsed at the same time from a quiescent bias.

In Figure 2.2.7, the drain current lags the drain voltage, which is known as drain lag. This phenomenon is also called 'knee walk-out', in which the knee voltage at which the drain current saturates rises. Drain lag is associated with deep-level defects in the GaN buffer region. Generally, the GaN buffer layer of high-voltage GaN HEMTs requires deep-level defects by doped by acceptors like Carbon (C), which can help suppress the buffer leakage. The GaN buffer defects trap charge generated

due to hot carriers scattering from the channel or due to gate leakage. AlGaN/GaN devices display higher drain lag ratios when the buffer layer conductivities are lower.

At the constant low field drain voltage, to avoid the complications of device heating, the gate lag can be measured by comparing the transient and steady-state drain currents. At large negative gate voltage, hot electrons tunnel into the AlGaN barrier and then fill surface states between the gate and drain. The positive polarization charges at the bare AlGaN surface are reduced by charge conservation. Therefore, the sheet density of 2DEG in the channel decreases, as well as the extended depletion region of 2DEG. The excess negative charges deplete the underlying 2DEG and create a "virtual gate", as shown in Figure 2.2.9. In operation mode with fast pulses, if the emission rate of the surface donors is much slower than the speed of gate voltage change, it leads to current collapse, in which the transient drain current decreases and lags the gate voltage. Passivation can significantly improve the gate lag.

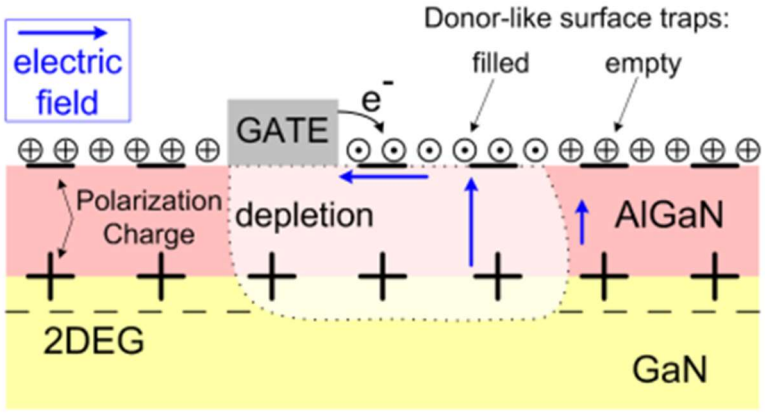


Figure 2.2.9: The virtual grid effect[72]

Much relative research has been done to suppress current collapse using semiconductor process technologies([73],[74]). The solution methods are to mitigate the crowded electric field to accelerate the electron into the trap, to reduce traps, especially the surface trap, and to increase the path resistance of the electron injection trap[31]. Field plate and surface passivation like Si_x, SiO_2, Al_2O_3 are standard solutions for current collapse by releasing electric field and reducing surface traps.

When increasing drain voltage and the negative gate voltage to turn off the device, the positive polarization charges accumulate in the carriers at the gate region. The crowding electrical field at the edge of gate easily overcomes the critical electrical field of GaN (3.3 MV/cm), which easily occurs the avalanche breakdown. As shown in Figure 2.2.10, a peak of the electric field occurs at the drain-side edge of the Gate and makes the breakdown voltage challenging to reach the theoretical value during off-state. In practice, the breakdown voltage is usually defined as when the leakage current exceeds 1mA/mm.

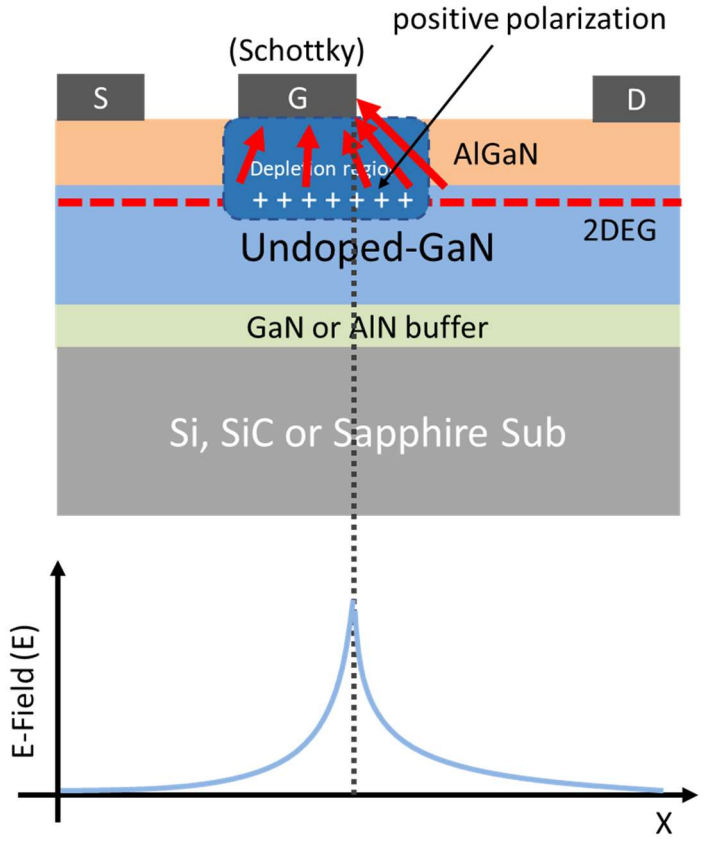


Figure 2.2.10: Schematic of electric field crowding at Gate edge with the field profile.

2.2.5 Field plate technologies

The traditional electric field management solution employed in lateral GaN devices is Field Plate (FP) technologies, which was first demonstrated in 2003[75]. It can reduce the trap reoccupation, suspend the current collapse and enhance the voltage-blocking capacity by designing the electric field profile and suppressing the field crowding at the gate edge ([76],[77],[78],[79]).

Figure 2.2.11 shows the cross-section structure of AlGaN/GaN HEMT with the source field plate and its electric field profile. It can be found that FP technologies can suppress the field crowding at the drain side of the Gate edge but have a new peak at the edge of Drain electrodes. The breakdown voltage of AlGaN/GaN HFET with Source FP increases from 100V to 600V, and ultra-low on-state resistance can be achieved [80]. It has been reported that the breakdown voltage and power density increase when the Field Plate length increases. Meanwhile, the unity current gain frequency (f_T)and the maximum frequency of oscillation (f_m) is degraded [81]. Although FP technologies can reduce the peak value, they can not eliminate it to achieve the ideal fat electric field.

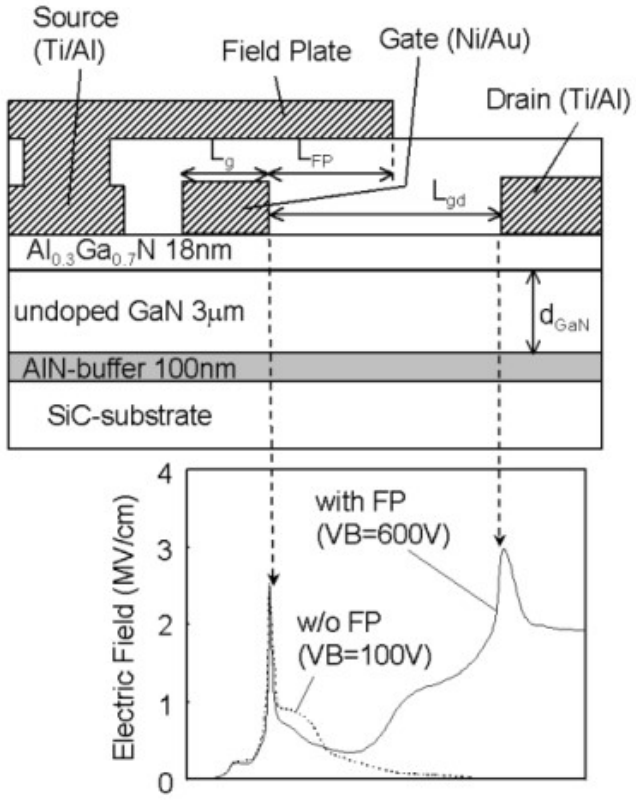


Figure 2.2.11: Cross-section schematics and electric-field profile of AlGaN/GaN HEMT with a source filed plate[80]**.**

2.2.6 Gate Injection Transistor Structure

Gate Injection Transistor (GIT) Structure is an approach to solving the current collapse by injecting holes from the p-GaN to the 2DEG region that reduce charge trapping effects and releases the trapped electrons instantaneously. Figure 2.2.12 shows the Schematic cross-section of conventional GIT. The p-type gate on the P-GaN layer can thicken the AlGaN layer to avoid carrier losses under the P-type region. From the I-V Characteristics in Figure 2.2.13, the drain current of a GIT FET increases obviously owing to the conductivity modulation[82], compared with the normally-on conventional GaN FET. The threshold voltage of GIT also increases over zero, which achieves normally-off behaviour. Here is the typical structure of an E-mode GaN transistor.

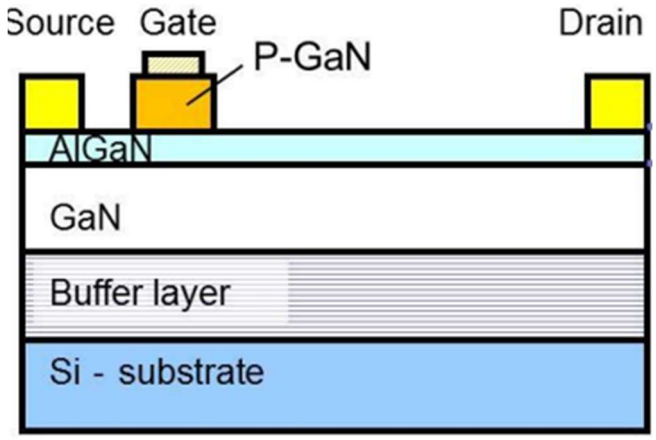


Figure 2.2.12: Schematic cross-section of conventional GIT[70].

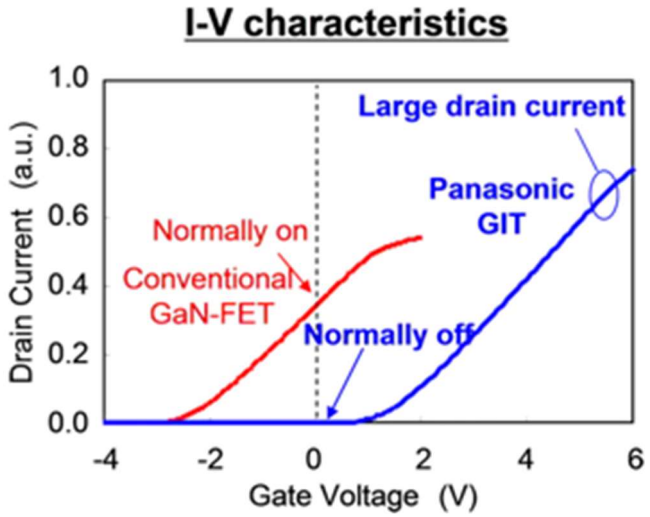


Figure 2.2.13: (a) I-V Characteristics of Normally Off GIT GaN and Conventional Normally On GaN [77].

In 2015 Panasonic proposed the new Hybrid-Drain-embedded GIT (HD-GIT) based on the conventional GIT structure, as shown in Figure 2.2.14 (a). In the HD-GIT structure, additional p-GaN regions under Drain are introduced near the drain and electrically connected to it. In theory, holes can be injected in this P-type region to release trapped electrons during the switching operation instantaneously. Figure 2.2.14 compares the dynamic on-resistance of a conventional GIT and the HD-GIT for inductive-load switching. The R is the on-state resistance of the conventional GIT normalized to its resistance at 500V. While the R0 is the on-state resistance of the new HD-GIT normalized to its resistance at 500V. There is a sharp increase of the on-state resistance for conventional GIT observed when the stress is over 600V for the conventional GIT. New HD-GIT is free from current collapse with a slight rise in R [70]. It is the common method to evaluate the degradation of devices by monitoring dynamic Ron during applying the high-voltage stress. The reliability standard for GaN

devices is that the degradation of Ron should be less than 20% after 1000H Regular/High Temperature Reverse Bias.

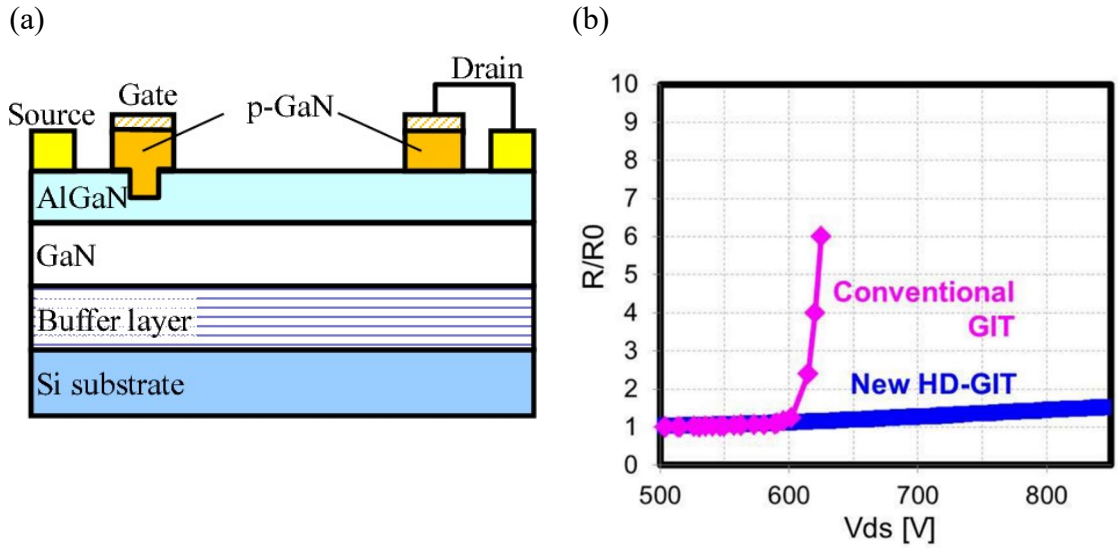


Figure 2.2.14: (a)Schematic cross-section of HD-GIT and (b) Measured dynamic on-resistance of a conventional GIT and the HD-GIT for inductive-load switching, normalized to the dc values (R/R0)[70].

2.3 Polarisation Super junction technologies

The alternative electrical field management, polarisation Super junction (PSJ), was proposed by A. Nakajima et al. in 2006 to push the high voltage breakdown by relaxing the crowding electric field[83]. Without doping any impurities, PSJ technology utilizes the charge compensation effect through positive and negative polarization charges to achieve the charge balance[84].

2.3.1 Induction of the PSJ Concept

PSJ technology is based on an un-doped GaN/AlGaN/GaN double heterostructures throughout the lateral channel. Figure 2.3.1 shows schematics of (a) PSJ structure and (b) its energy band diagram at thermal equilibrium[85]. There is a double-hetero GaN/$Al_{0.23}Ga_{0.77}N$/GaN capping with a p-type GaN layer doping with Magnesium (Mg). GaN(000$\bar{1}$)/AlGaN(0001) and AlGaN (000$\bar{1}$)/GaN(0001) coexist with an equivalent magnitude of positive and negative polarization charge (σ). Attracted and accumulated Electrons(holes) by the positive(negative) polarization charges are confined in the triangle quantum well. Therefore, two-dimension hole gas (2DHG) and 2DEG are spontaneously formed at the GaN/AlGaN and AlGaN/GaN interface, respectively.

In 2010, the density and mobility of 2DHG were first demonstrated over 1.1×10^{13} cm^{-2} and 16 $cm^2V^{-1}S^{-1}$ at the University of Sheffield, United Kingdom and POWDEC K.K, Japan ([86],[87]). It should be noticed that the Mg-doped in P-GaN does not contribute to the charge balance because the charge density from the Mg layer is much lower than 2DHG[88]. The presence of the high-density 2DHG could facilitate the development of p-channel HFETs in GaN.

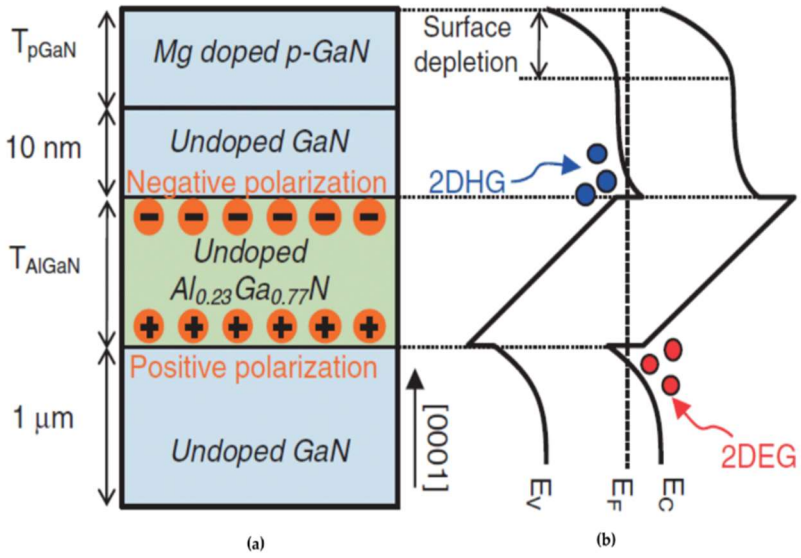
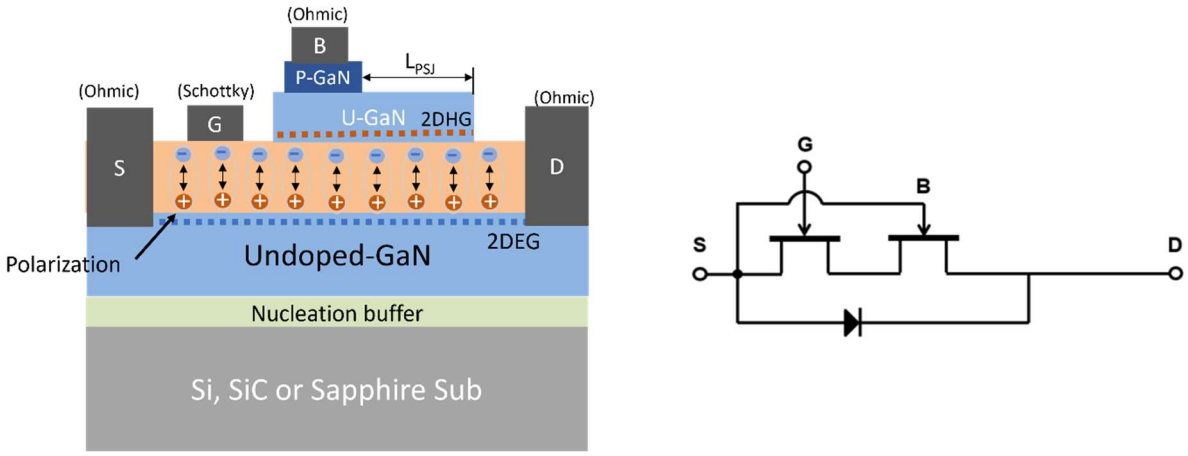


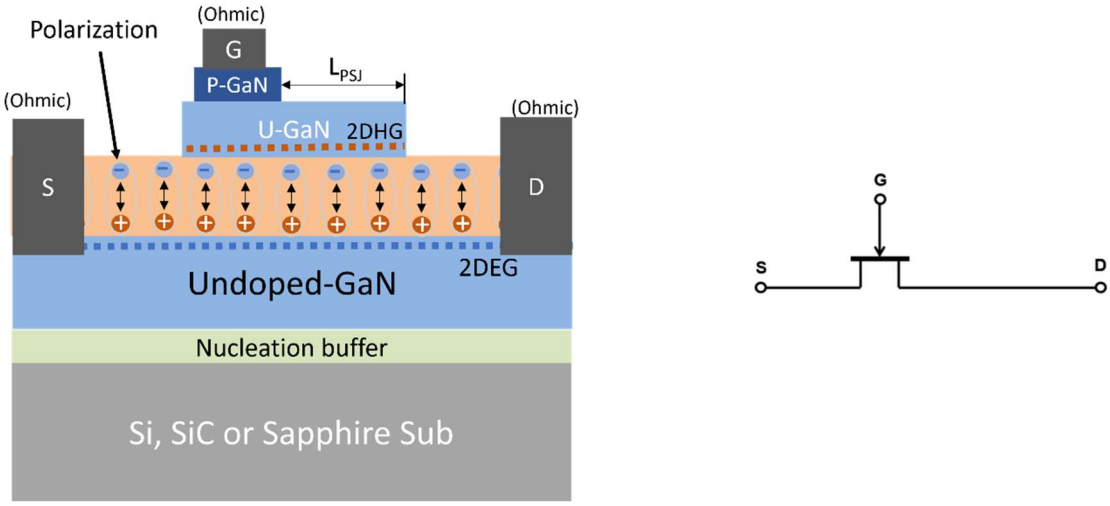
Figure 2.3.1: Schematics of (a) PSJ structure and (b) energy band diagram at thermal equilibrium[85].

2.3.2 PSJ Field Effect Transistors

In 2011, the Sheffield power microelectronic team demonstrated high-voltage GaN PSJ Field Effect Transistors (PSJ HFETs) on the Sapphire substrate [84]. Figure 2.3.2 shows the simplified cross-section schematic of a typical GaN-based PSJ HFET (a) with Schottky Gate and (b) with Ohmic Gate. Both PSJ SG HFETs and PSJ OG HFETs are normally-on devices.



(a) PSJ SG HFET



(b) PSJ OG HFET

Figure 2.3.2: The simplified cross-section of a typical GaN-based HFET and equivalent circuit (a) with Schottky Gate and (b) with Ohmic Gate on Sapphire substrate

The PSJ HFET with Schottky Gate (PSJ SG HFET) has four electrodes: Source (S), Drain (D), Gate (G) and Base (B). Drain and Source electrodes on the AlGaN layer are connected to the 2DEG using ohmic contacts. The gate is formed as a Schottky contact to govern the current and switch the device on/off. The base makes an ohmic contact with the 2DHG through the top p-GaN layer and is electrically connected to the gate or Source. Thus, the device with Schottky Gate can provide an inherent body diode to show reverse conducting characteristics [89]. On the right of Figure 2.3.2(a), it shows the equivalent circuit of PSJ SG HFET with Base connected to Source. When $V_{gs}>V_{th}$, the current flows through the 2DEG channel from Drain to Source, identical to that of conventional AlGaN/GaN HFETs. During off-state, the negative gate voltage (Vth>Vgs) is applied, thus pinching off the 2DEG underneath the gate region. As the drain voltage increases, the base and drain electrodes discharge 2DHG and 2DEG. The charge remains in balance. The PSJ region is depleted and acts as an intrinsic region. [89]. Therefore, a flat field can be achieved in the ideal conditions, as shown in Figure 2.3.3.

For PSJ HFETs with Ohmic Gate (PSJ OG HFET), there are three electrodes: Source, Drain and Gate. The Drain/Source electrode on AlGaN employs ohmic contacts to connect to the 2DEG. The gate electrode forms the Ohmic contact to 2DHG by the p-GaN layer doping with Mg. Here, an equivalent PN diode is formed by 2DHG and 2DEG, which enables reverse conduction from Gate to

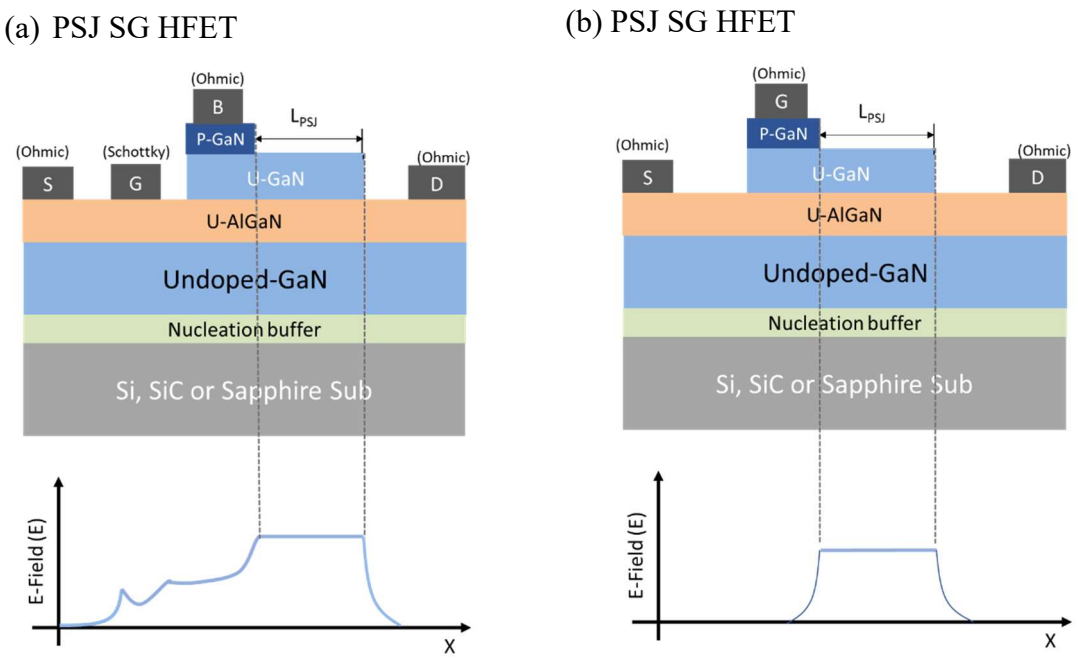


Figure 2.3.3: The ideal Electrical field distribution of a typical (a) PSJ SG HFET and (b) PSJ OG HFET.

Drain. Similarly, current flows through the 2DEG channel in the on-state. In reverse conditions, 2DEG under the gate region is depleted as the intrinsic region when the negative Gate voltage drops below the threshold voltage. The current conduction path is cut off and PSJ OG HFETs enter off. Under the ideal charge balance condition, a 'box-like' electric field can be achieved at turn-off. Figure 2.3.3 shows the ideal Electrical field profile of a typical (a) PSJ SG HFET and (b) PSJ OG HFET. From theorical and experimental data, the breakdown voltage of GaN PSJ devices can be enhanced and scaled up directly as a function of the length of the drift region (L_{PSJ})([83], [89],[84]).

Figure 2.3.4 shows the simulated output Id -Vd characteristics of the (a) Schottky Gate PSJ HFETs (b) Ohmic Gate PSJ HFETs at Vg = 0V. In the same case of L_{PSJ}, PSJ OG HFETs has a lower on-off resistance than the SG device due to the shorter distance between the source and drain. Simulated lateral electric field distribution before the breakdown of the OG and SG PSJ HFETs is demonstrated in Figure 2.3.5. It can be found that the electric field distribution of PSJ HFETs is almost uniform over PSJ region with two peaks at the Gate edge and Drain edge.

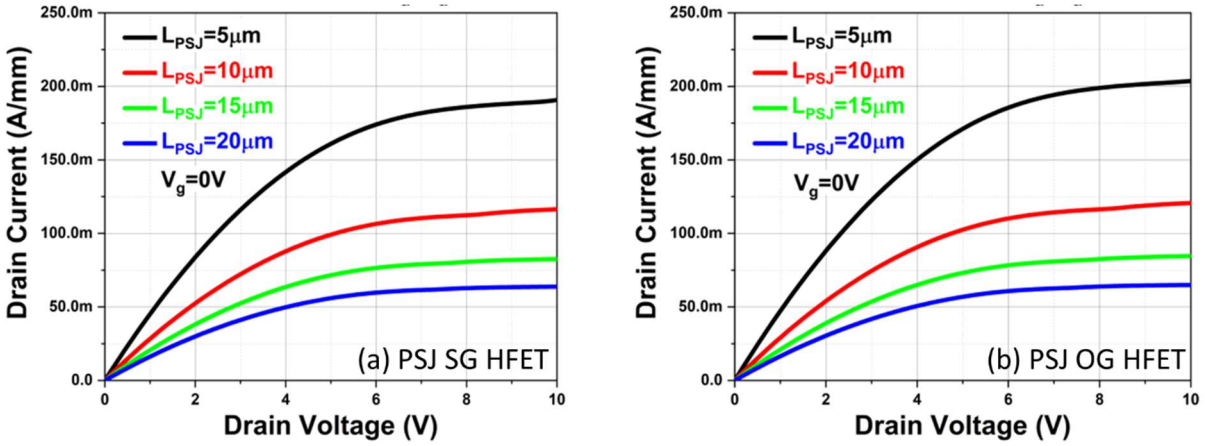


Figure 2.3.4：Simulated output Id -Vd characteristics of the (a) Schottky Gate PSJ HFETs (b) Ohmic Gate PSJ HFETs at Vg = 0V.

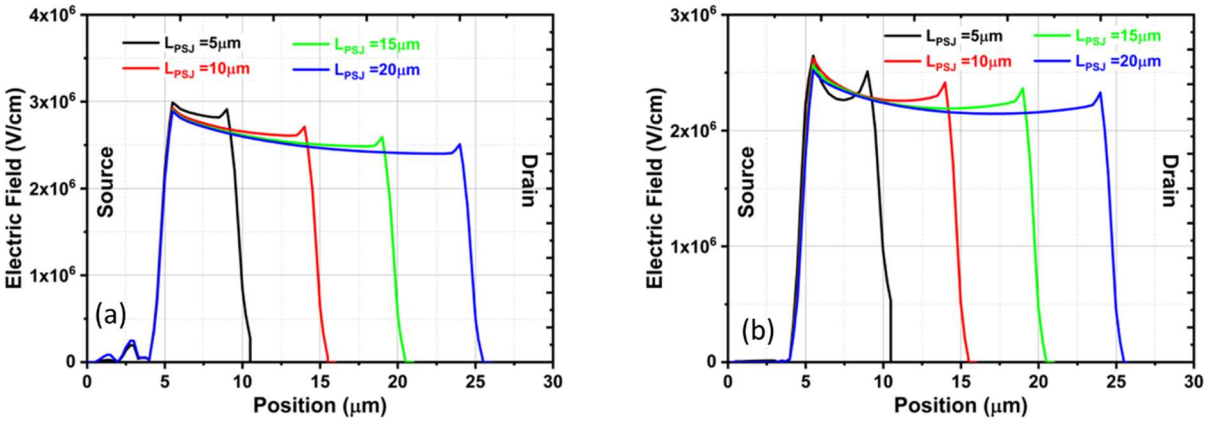


Figure 2.3.5: Simulated lateral electric field distribution before the breakdown of (a) Schottky Gate PSJ HFETs (b) Ohmic Gate PSJ HFETs at Vg = -15V

Figure 2.3.6 compares the reverse IV characteristics of the conventional GaN HEMT and PSJ FETs[90]. With a 10um length from Gate to Drain, the avalanche breakdown of PSJ FET (super HFET) occurs at around 560V, while conventional GaN HEMT happens at about 100V. When the drift region L_{PSJ} of PSJ HEMT increases to 22μm, and the breakdown voltage exceeds 1.1kV. Experiments prove that PSJ technology can improve the breakdown voltage capability effectively. Recently, POWDEC KK reported that the breakdown voltage of the large area enhancement-mode PSJ FET on Sapphire substrates is over 3kV breakdown voltage.

Figure 2.3.7 shows the measured off-state Id-Vd characteristics of (a)PSJ SG HFETs and (b) PSJ OG HFETs with various PSJ lengths. It can be found that breakdown voltage (BV) and PSJ length have a linear relationship. Based on Figure 2.3.7, conservatively, it can be estimated that BV increases by 500 V for every 5μm increase in L_{PSJ}.

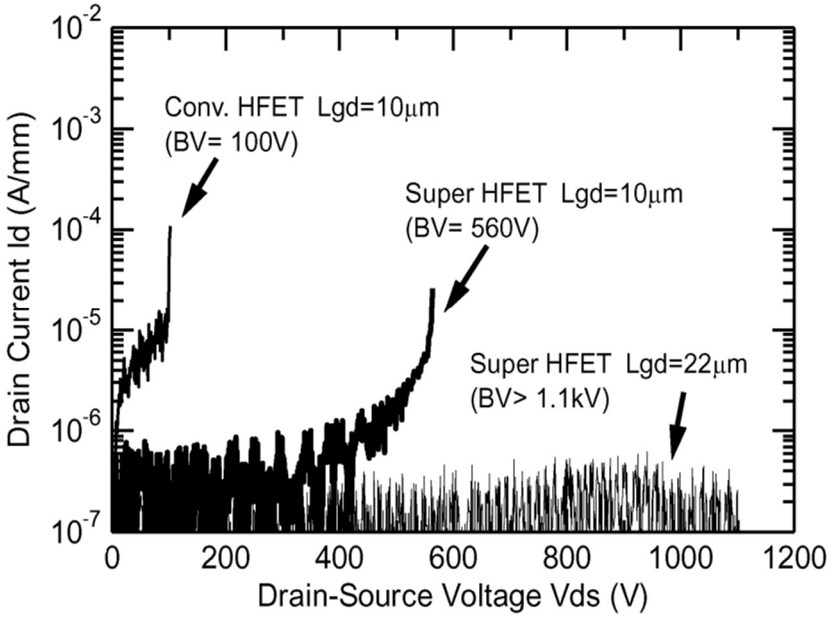


Figure 2.3.6: The comparison in breakdown voltage of the GaN conventional HFET and PSJ FET[90]**.**

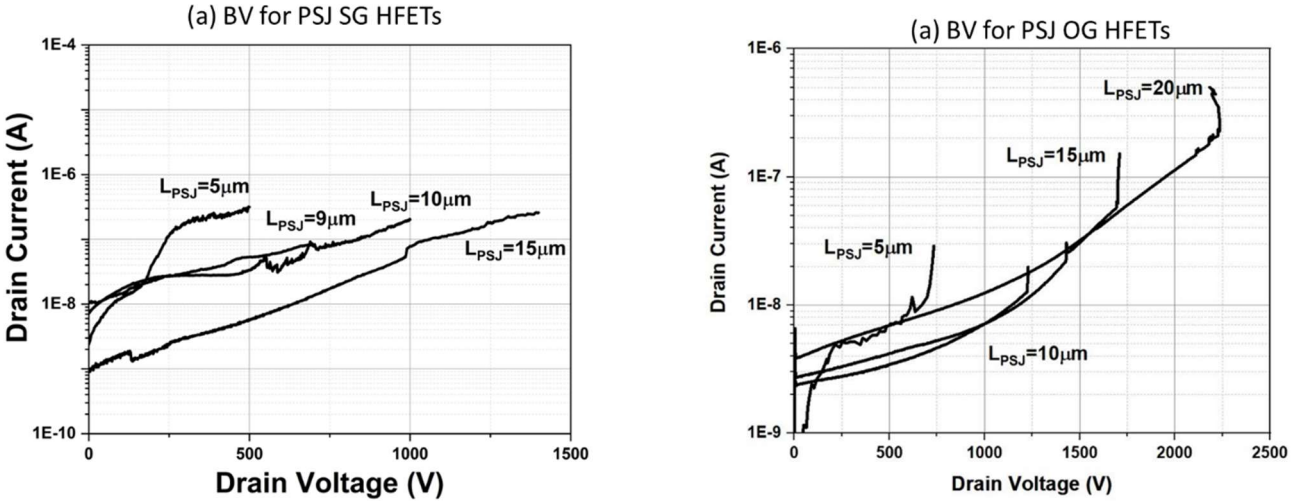


Figure 2.3.7: Measured off-state Id -Vd characteristics of (a) PSJ SG HFETs and (b) PSJ OG HFETs at Vg = -15[91][92]

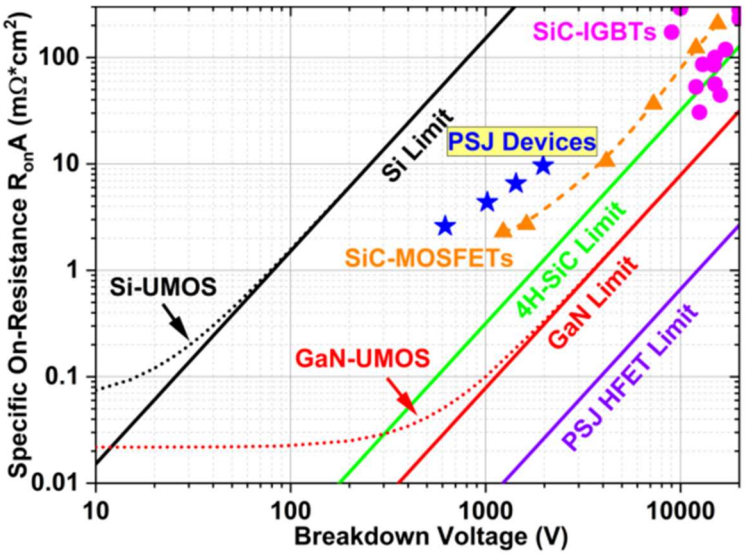


Figure 2.3.8: The trade-off relationship between Ron.A and BV with the material limit

The trade-off relationship between specific on-state resistance (R_{on}.A) and Breakdown Voltage (BV) is a significant parameter for power semiconductors, as shown in Figure 2.3.8.

For lateral FETs, the line integral defines the electric potential at a point in a static electric field. In an ideal case of a 'box-like' electrical field, the theoretical BV (V_B) of a lateral SJ device with a uniform E-field distribution can be derived from the basic theory of electrostatic:

$$V_B = E_{crit} \cdot L_{ch} \qquad \text{------(2.13)}$$

Where $L_{ch}$is the lateral length of the conduction channel and E_{crit} is the critical electric field of the semiconductor material.

The on-state resistance can be expressed as:

$$R_{on} = R_{sheet} \cdot \frac{L_{ch}}{W} = \frac{L_{ch}}{q \cdot \mu_{ch} \cdot n_s \cdot W} \qquad \text{------(2.14)}$$

Where R_{sheet} is sheet resistance of electron channel, q stands for electron charge, μ_{ch} is channel electron mobility, n_s is the sheet density of electrons and W is the channel width.

The specific on-state resistance Ron.A equals:

$$R_{on} \cdot A = R_{on} \cdot W \cdot L_{ch} = \frac{{L_{ch}}^2}{q \cdot \mu_{ch} \cdot n_s} \qquad \text{------(2.15)}$$

Combining with Equation(2.13) and Equation(2.15), the Ron.A can be expressed in terms of V_B as:

$$R_{on}.A = \frac{{V_B}^2}{q.\mu_{ch}.n_s.{E_{crit}}^2} \qquad \text{------(2.16)}$$

Lateral device figure of merit (LFOM), which can be used for evaluating devices performance relative to its theoretical counterpart, is derived from Equation(2.16) by:

$$LFOM = \frac{{V_B}^2}{R_{on}.A} = q.\mu_{ch}.n_s.{E_{crit}}^2 \qquad \text{------(2.17)}$$

2.4 Bidirectional switch configurations

Many implementations of a bidirectional switch have been demonstrated using discrete unidirectional devices. Usually, BPS can be made with two MOSFET in series or two quadrants IGBT with didoes.

2.4.1 Bidirectional switch configurations using MOSFETs

Figure 2.4.1 shows BPS configurations using N-or P-Channel MOSFETs. A single MOSFET can conduct or block the current in one direction due to the body diode. When two MOSFETs are connected in series, they can realise bidirectional voltage control and current flow. Compared with P-channel FETs, N-channel FETs are preferred due to lower on-state resistance and cost. As an example of common-source N-channel MOSFETs, it has four possible states shown in Table 2.3 and Figure 2.4.2 is schematic illustration of operation modes.

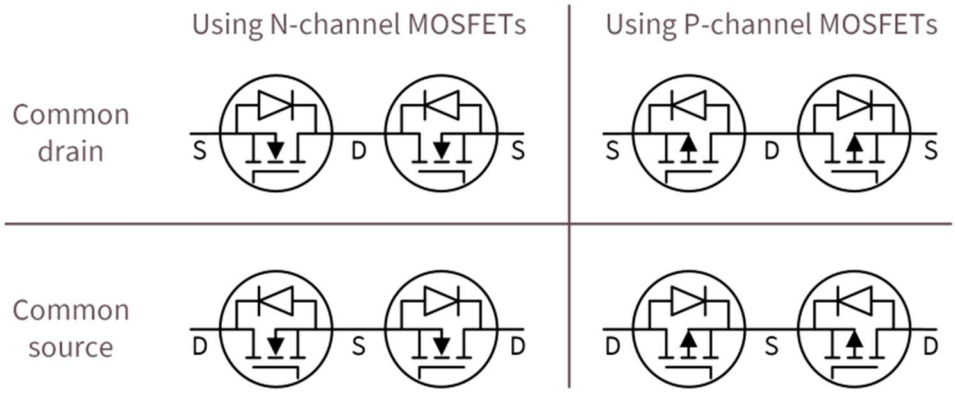


Figure 2.4.1: BPS configurations using N-or P-Channel MOSFET[19]

Table 2.3: Operation modes of common-source N-channel MOSFETs

MOSFET 1	MOSFET 2	State
ON	ON	Current can flow in both directions through the circuit.
ON	OFF	Current can flow from left to right
OFF	ON	Current can flow from right to left
OFF	OFF	Blocking bidirectional currents

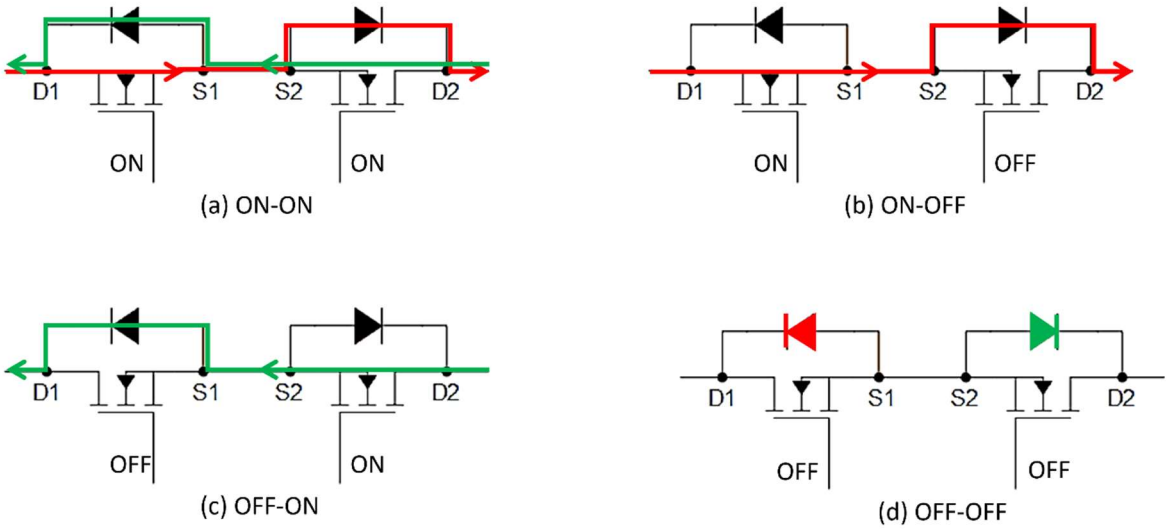


Figure 2.4.2:Operation mode of common-source N-channel MOSFETs.

2.4.2 Bidirectional switch configurations using IGBTs

Figure 2.4.3 shows the topologies of bidirectional switches with IGBT for matrix converters([93],[94],[95]). The most commonly used configurations of bi-directional switches are either back-to-back connections of IGBTs with anti-parallel diodes in a common emitter (CE) or a common collector (CC), shown in Figure 2.4.3 (a) and (b). In addition, Figure 2.4.3 (c) shows a diode bridge and a single IGBT transistor which only have one active device to realize the bidirectional switching capability. Figure 2.4.3 (d) is the anti-parallel connection of reverse blocking IGBTs (RB-IGBTs) without anti-parallel diodes. IGBT provides any direction of the current path, so the current direction cannot be controlled independently. In addition, although IGBTs have very low forward drop, the obvious disadvantage is that the reduction of on-off loss is limited by on-off voltage offset caused by series diodes and by the IGBTs[96]. Table 2.4 shows the on-state voltage drop and switching loss comparison of different 1.2kV bidirectional switches[97].

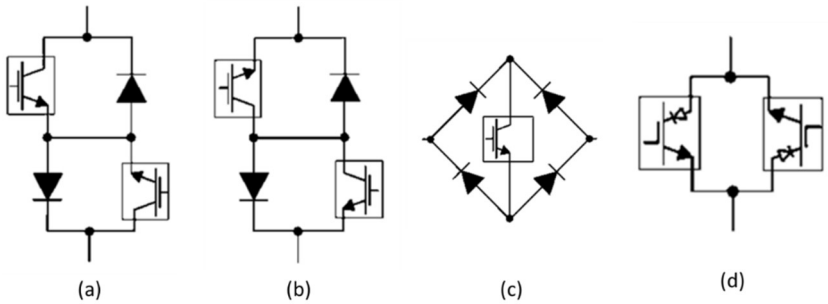


Figure 2.4.3: Topologies of Bidirectional switches in (a) CE anti-paralleled IGBT arrangement, (b) CC anti-paralleled IGBT arrangement, (c) diode bridge with an IGBT arrangement and (d) RB-IGBT arrangement.

The operation principles of Bidirectional switches using IGBT in CE / CC is similar with that of bidirectional switch configurations using MOSFETs. Figure 2.4.4(a)(b)(c)(d) shows the operation principles of the diode bridge embedded IGBT switch. When the gate of IGBT is smaller than the threshold voltage, the IGBT turns off and then blocks the current in any direction. For the conduction mode, the IGBT turns on and only two SBDs are forward-biased, allowing the current to flow along the direction where the arrow indicates shown in Figure 2.4.4(b) and Figure 2.4.4(d) . The IGBT's body diode causes the voltage drop in the forward/reverse turn-on mode.

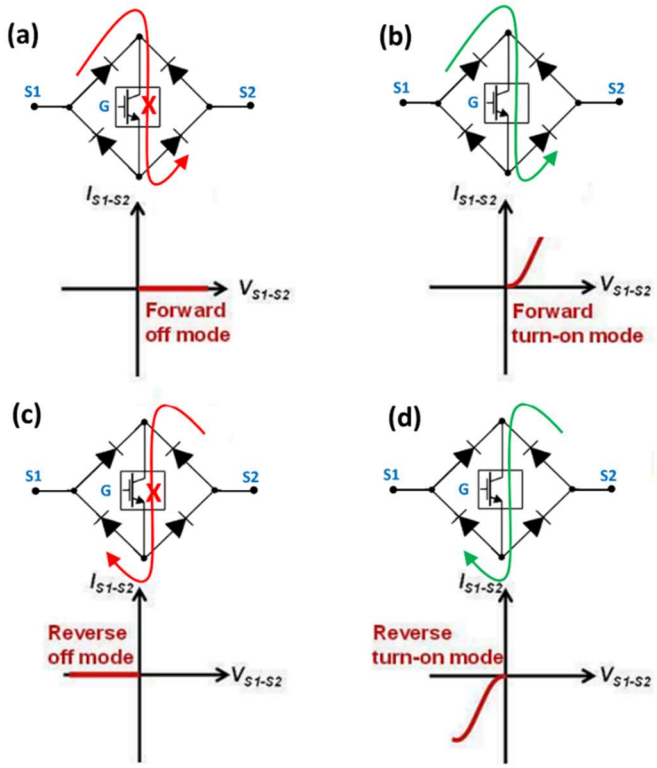


Figure 2.4.4: Operation principles of diode bridge embedded IGBT switch. (a) Forward off mode (G: off, $V_{S1S2} > 0$ V), (b) forward turn-on mode (G: on, $V_{S1S2} > 0$ V), (c) reverse off mode (G: off, $V_{S1–S2} < 0$ V), (d) reverse turn-on mode (G: on, $V_{S1–S2} < 0$ V).

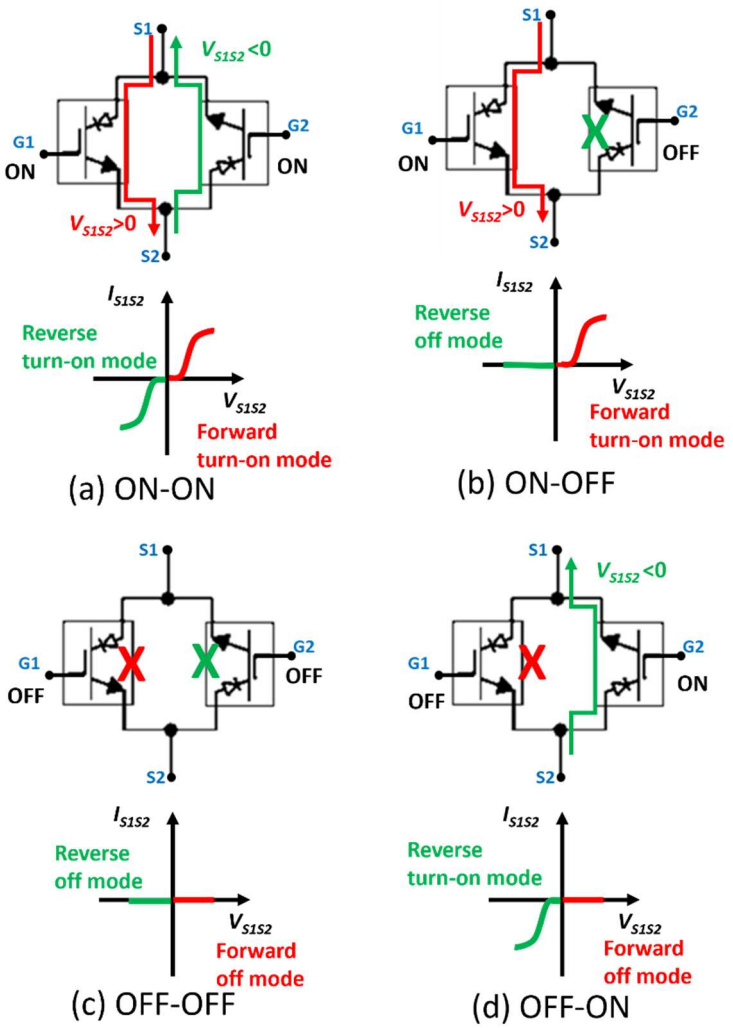


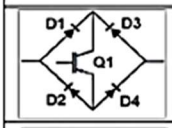
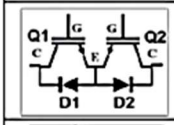
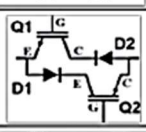
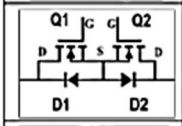
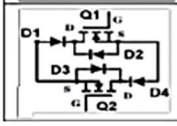
Figure 2.4.5: Operation principles of Bidirectional switches in RB-IGBT arrangement. (a) ON-ON mode,(b)ON-OFF mode,(c) OFF-OFF mode and (d) OFF-ON mode.

Figure 2.4.5 displays the operation principles of bidirectional switches in an RB-IGBT arrangement. For bidirectional RB-IGBTs, gates of two RB-IGBTs control the current flowing or blocking along one direction, respectively. Similarly, it can be observed the off-set voltage in the on-state current due to the body-diode of RB-IGBT.

Whether MOSFETs or IGBTs, a BPS at least needs two unidirectional devices. A Bidirectional switch consisting of discrete unidirectional devices requires a larger chip area and higher switching losses than a monolithic bidirectional switch. The monolithic BPS is the future trend of bidirectional device development. The integrated bidirectional switch requires no soldered joints, fewer interconnections, and no additional interface circuits to perform output signal functions. It can reduce the cost and production time and fabricate complex circuits easily. Meanwhile, device performance

and reliability can be improved. On the other hand, signal operation will be possible as it dramatically reduces noise due to components in monolithic devices being very close to each other([25], [98]).

Table 2.4: Comparison of fabricated 1.2kV 20A bidirectional switch implementations[99].

Switch Configuration	Description	Number of Components	On-State Voltage Drop	Switching Loss
	Si Diode Bridge + Asymmetric Si IGBT [1]	5	8.6 [2 diodes + 1 IGBT]	High
	Asymmetric Si IGBTs + Freewheeling Si diodes [2]	4	5.8 [1 diode + 1 IGBT]	High
	Back-to-back symmetric Si IGBTs [3]	2	2.2 [1 symmetric IGBT]	Very High
	SiC Power MOSFETs + JBS diodes [4]	4	3.1 [1 diode + 1 MOSFET]	Low
	Back-to-back SiC Power MOSFETs + antiparallel and series JBS diodes [5]	6	3.1 [1 diode + 1 MOSFET]	Low

In 2020, the 1.2 kV 4H-SiC Bi-Directional FETs with integrated JBS diodes and 4-terminal monolithic 4H-SiC BiDFETs with two integrated JBSFETs were fabricated. They package two discrete SiC power MOSFET bare-mode chips in a four-terminal custom-designed module. Compared with bidirectional switch implementations using discrete IGBT or MOSFETs shown in Table 2.4.2, a monolithic device integrating two JBSFETs has a much smaller on-state voltage drop of 1.0 V and low switch loss at 20 A [53].

2.4.3 Bidirectional switch configurations using normally-off GaN HEMTs

The vertical structure of MOSFETs/IGBTs makes it highly challenging for monolithic to place two FETs on a single chip and optimise the voltage ratings of devices with cost. However, it is not a limitation for lateral GaN HEMTs. In addition, the absence of body diodes makes it relatively easy to create a monolithic bidirectional GaN switch.

In 2007, Panasonic proposed the 650V 3.1mΩcm^2 monolithic AlGaN/GaN bidirectional switch using normally-off Gate Injection Transistors (GIT)[20]. Figure 2.4.6 shows the structure and equipment circuit of the AlGaN/GaN bidirectional switch. Monolithic integration of two GIT shares the drift region, effectively reducing the chip's overall size. As mentioned in the Section 2.2.6, gates

on the P-GaN layer thicken the AlGaN layer to avoid carrier losses under the P-type region. Due to it has two gate to control the current conduction or blocking, it is called as monolithic dual-gate bidirectional GaN switches.

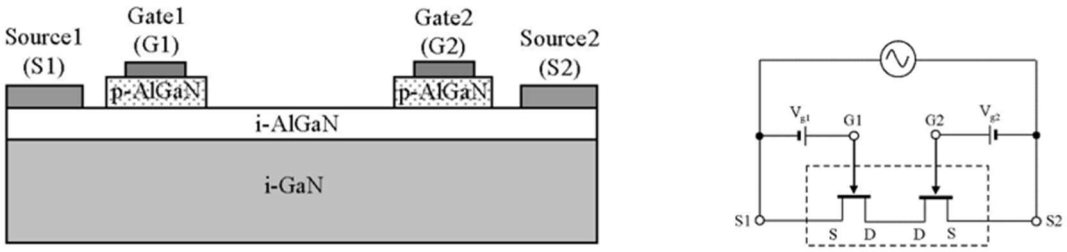


Figure 2.4.6：Schematic illustration of (a) a monolithic AlGaN/GaN bidirectional switch e and (b) the equivalent circuit[20]**.**

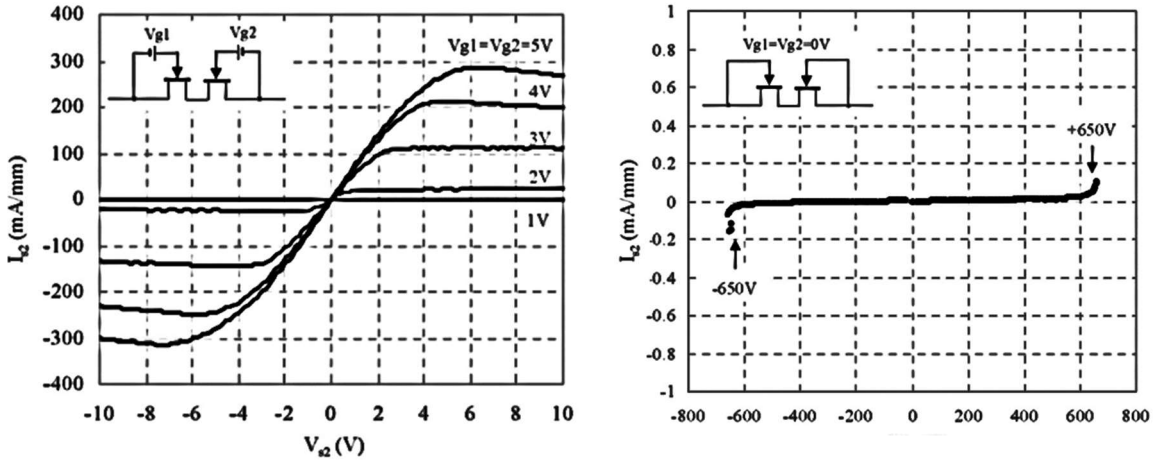


Figure 2.4.7: (a) Output characteristics and (b) Off-state characteristics for monolithic AlGaN/GaN bidirectional switch[20]**.**

From the IV characteristic curve of the monolithic AlGaN/GaN bidirectional switch shown in Figure 2.4.7(a), the on-state resistance is 3.1mΩcm^2 and the 650V Breakdown voltage was measured shown in Figure 2.4.7(b). It should be noticed that there is no off-set voltage in the conduction mode due to the absence of body diodes, which reduce switching losses. Similar to conventional GaN-based devices, it also has electric field management issues, as mentioned in Section 2.2.4, like the current collapse and the lack of high breakdown voltage.

In 2022, Innoscience launched the 40V GaN device platform and successfully imported the 4.8mΩ bi-directional GaN-on-silicon HEMT (BiGaN) into Oppo and Realme mobile phone motherboards for efficient and more compact over-voltage-protection (OVP) systems. The

introduction of GaN technology in the smartphone itself for protection is a groundbreaking advancement, as previously, such circuits had to be integrated into the charger. This product is packaged in wafer-level chip-size packages (WLSCP) and is only 2.1 x 2.1 x 0.54 mm. Considering the space constraints on a mobile phone's circuit board, the small size is much more significant. Compared with back-to-back connected NMOS MOSFETs, it is reduced by 64%, and the peak power heating is reduced by 85%.

To realise the small size and the ultra-low on-state resistance, Innoscience's BiGaN HEMTs have a symmetrical structure with only one gate to achieve bi-directional current on/off control. For the single-gate bidirectional GaN switch, excessive gate leakage is a challenge. Innoscience employed the unique gate structure to achieve low gate leakage. As shown in Figure 2.4.8, the gate can be can be regarded as a back-to-back connected diode. Gate Metal(-)/P-GaN(+) is Schottky contact; The lower diode has a P-GaN(+)/AlGaN(-) junction structure. Through differentiated process steps and process control, the gate leakage of BiGaN is smaller than 3uA at 85°C[21]. The applications which Innoscience's BiGaN HEMTS targets, such as overvoltage protection circuits (OVP) for smartphone charging, high-side load switching circuits, and switching circuits for multi-power systems, require the ultra-low on-resistance to reduce conduction loss while loss induced by the gate leakage is not a key metric for these applications. On the other hand, it is wise to choose wafer-level chip size packages (WLSCP) as packages for BiGaN HEMTs. WLSCP is an important factor to realize the system miniaturisation since it has minimal parasitic resistance which helps to dissipate heat and reduce conduction losses.

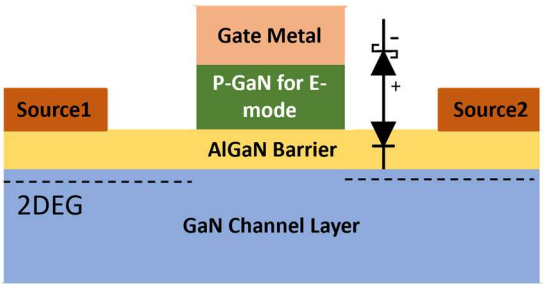


Figure 2.4.8: The schematic diagram for the gate of Innoscience's BiGaN HEMT

In addition to dual-Gate or single gate bidirectional GaN switches, people are inspired by bidirectional switching technology using MOSFET/IGBTs. Figure 2.4.9(a) shows the fabricated AlGaN/GaN bi-directional switch with embedded diode bridges. It employs one normally-off AlGaN/GaN HEMT in Figure 2.4.9(b) as well as four embedded Schottky barrier diodes in Figure 2.4.9(c). Similar to the bidirectional switch configuration using the diode bridge and the single IGBT

transistor, it only requires one gate driver and minimizes parasitic resistance and inductance due to the diode embedment.

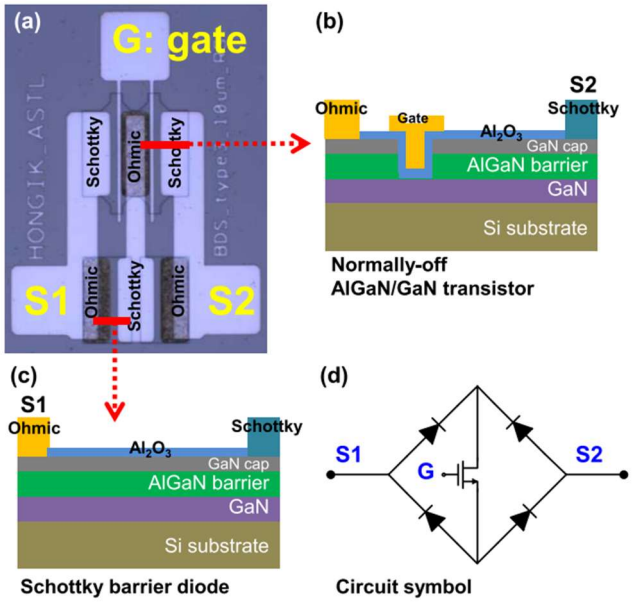


Figure 2.4.9: (a) Microscope image of fabricated diode bridge AlGaN/GaN-on-Si bi-directional switch, cross-sectional schematics of (b) recessed MOSFET,and (c) SBD, and (d) equivalent circuit[100]**.**

The output characteristic is shown in Figure 2.4.10(a) and inset figure(b) is off-state breakdown characteristics. There is the off-set voltage in forward and reverse conduction modes due to the turn-on voltages of SBDs, which cause the undeserved conduction loss. It is necessary to employ SBD with lower work function metal, a recessed Schottky contact[101], or a gated ohmic anode[102] can significantly reduce the off-set voltage minimising the on-state conduction loss.

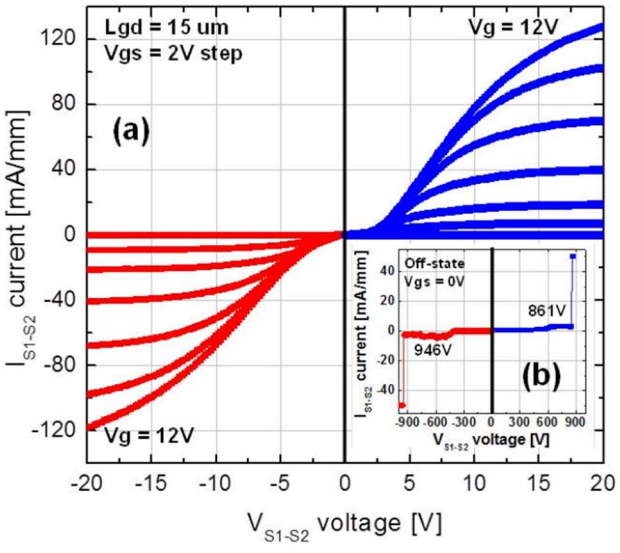


Figure 2.4.10: (a) The on-state and (b) (inset) off-state characteristics of the fabricated

The configurations employing two normally-off GaN-based reverse conduction MISHEMTs (RC-MISHEMTs) or reverse blocking MISHEMTs (RB-MISHEMTs) to realize the normally-off bidirectional switching have been developed. Figure 2.4.11(a) displays the cross-section of novel GaN-based RB-MISHEMTs and Figure 2.4.11(b) GaN-based RC-MISHEMTs. The GaN-based RB-MISHEMTs MISHEMT features a hybrid drain containing of Ohmic (Ohm-D) and recessed MIS structure (MIS-D). It forms a body diode. When the Drain voltage is smaller than the threshold voltage of diode, the 2DEG under MIS-D is depleted. The dielectric under MIS-D is high K which used to reduce the drain leakage and the turn on voltage of the body diode. Similar to RB-IGBT, two RB-MISHEMTs are connected in anti-parallel shown in Figure 2.4.12(a). The GaN-based RC-MISHEMTs MISHEMT features a hybrid source containing of a Schottky diode(Sch-S) between Gate and Drain. The bidirectional switches can be constructed by two anti-serially connected RC-MISHEMTs as shown in Figure 2.4.12(b).

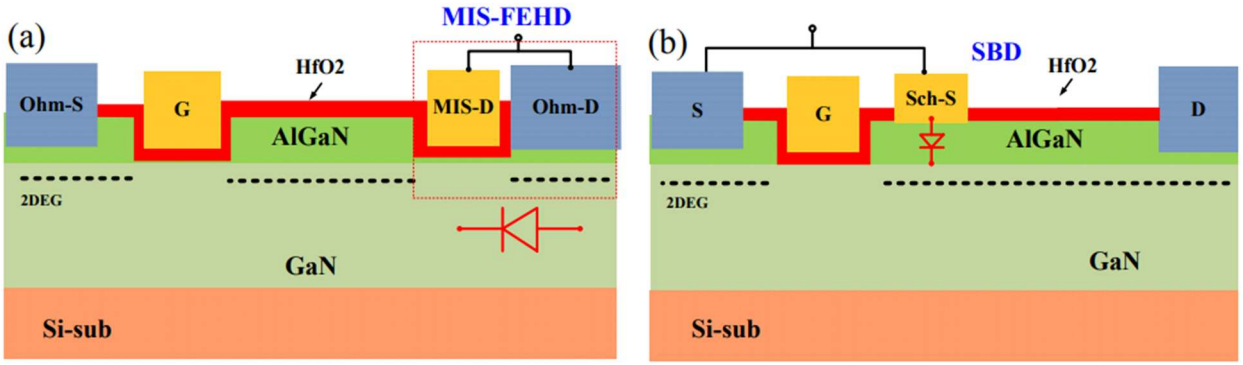


Figure 2.4.11: The cross-section (a) GaN-based RB-MISHEMTs and (b) GaN-based RC-MISHEMTs

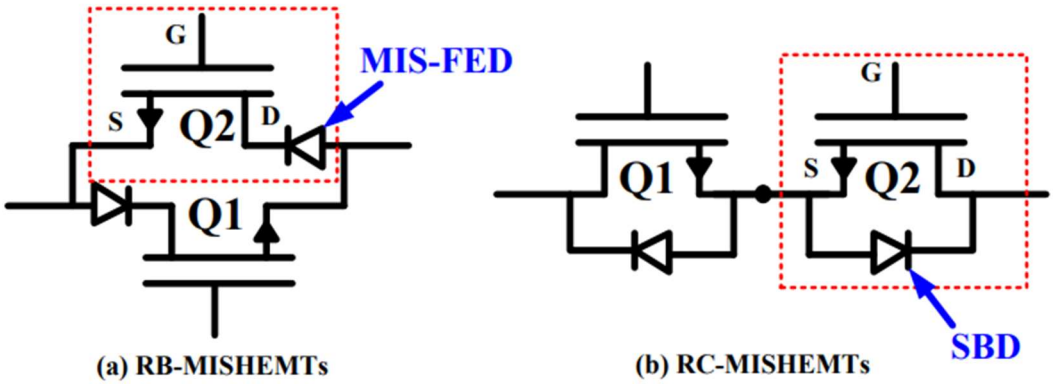


Figure 2.4.12: The Bidirectional switch configuration using (a) RB-MISHEMTs and (b) RC-MISHEMTs.

Figure 2.4.13 (a) and (b) display the simulated output characteristic of novel RB-MISHEMTs and RC-MISHEMTs in the forward conduction mode, respectively. There is the offset voltage for RB-

MISHEMTs for due to the turn-on voltages of body diode. Compared with the RB- MISHEMTs, RC-MISHEMTs has the higher on-state resistance due to the longer current path.

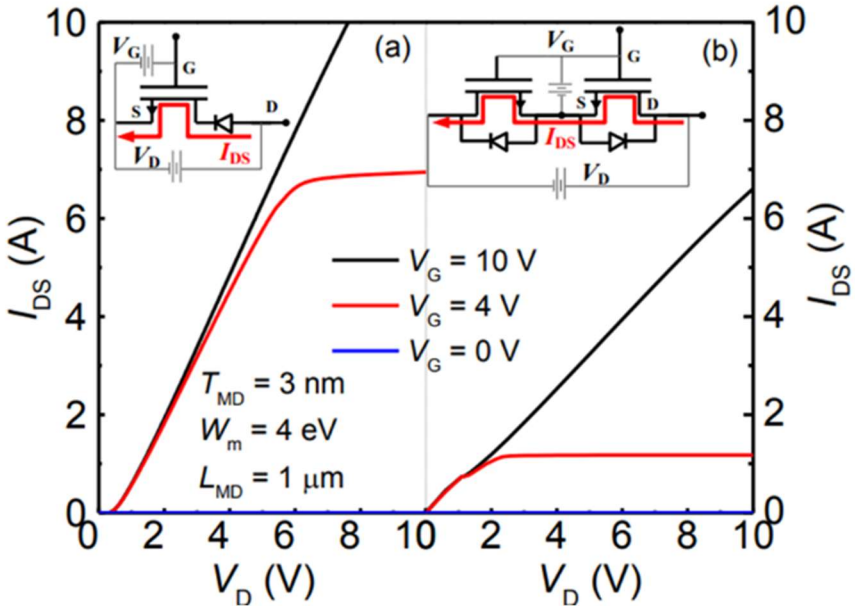


Figure 2.4.13: The simulated output characteristic of the Bidirectional switch using (a) RB-MISHEMTs and (b) RC-MISHEMTs.

The off-state characteristic of the Bidirectional switch using RB-MISHEMTs (Black lines) and RC-MISHEMTs (Red lines) are shown in Figure 2.4.14. The anti-serially connected RC-MISHEMT has the higher leakage due to the Source connected Schottky Contact (Sch-S in Figure 2.4.11). For the anti-parallel connected novel RB-MISHFETs, the on-off leakage is smaller due to the high K dielectric.

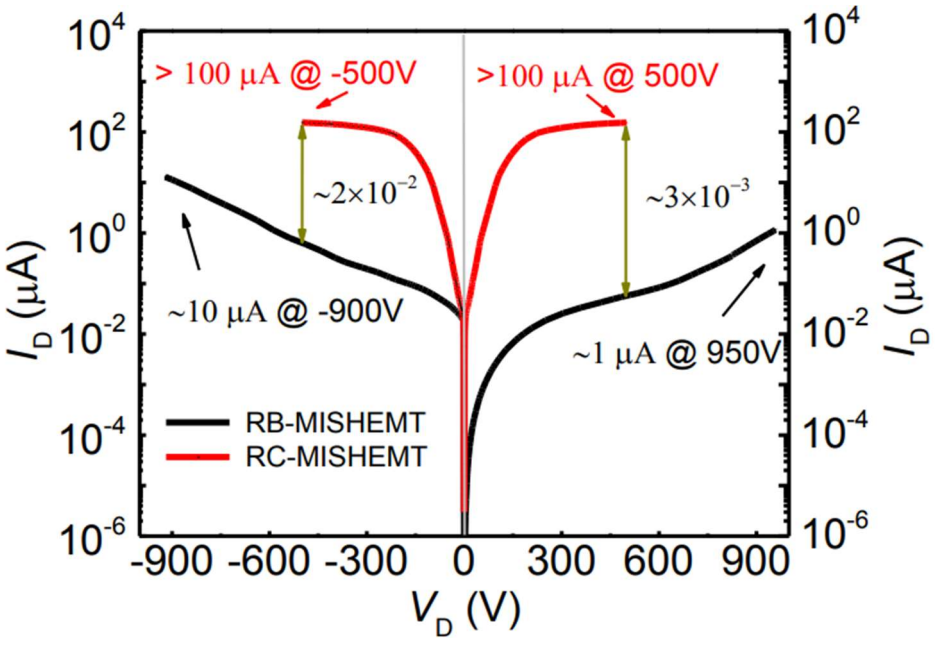


Figure 2.4.14: The simulated off-state characteristic of the Bidirectional switch using RB-MISHEMTs and RC-MISHEMTs

2.4.4 Bidirectional switch configurations using normally-on GaN HEMTs

The low threshold voltage is the significant limitation of Bidirectional switch configurations based on normally-off GaN technology. In some applications, the high threshold voltage is significant, which can prevent noise and false turn-on. In 2023, Transphorm demonstrated 60mΩ GaN-based integrated BPS with 4V threshold voltage assembled in a TO247 package. Figure 2.4.16(a) shows the simple cross-section and Figure 2.4.16(b) is the equivalent circuit of Thransphorm's integrated GaN FQS. The integrated GaN FQS has four terminals and consists of 3 components: two low-voltage Si MOSFETs and one bidirectional normally-on AlGaN/GaN HEMT. Two low-voltage Si-MOSFETs are employed to achieve the normally-off behaviour, because Power switches in power conversion applications must be normally-off for safety and reliability purposes. The bi-directional D-mode HEMT is the core of BPS, which allows the current conducts/blocks in both directions. The bidirectional D-mode GaN gates are connected to Si-MOSFETs Source, and its sources are connected to drains of Si-MOSFETs. Transphorm's integrated GaN FQS can be seen as two Cascodes in a common drain configuration, with eight operation modes under various bias conditions. Table 2.5 summarise operation modes of the integrated GaN FQS.

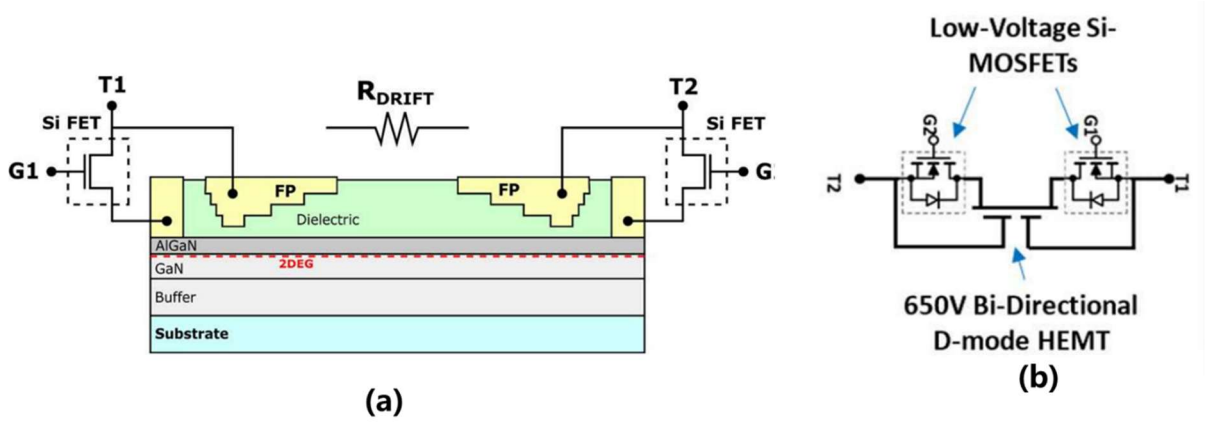


Figure 2.4.15:(a) Schematic of the cross-section (b) equivalent circuit schematic of Transphorm's integrated GaN FQS[22]

Table 2.5: The operation mode of integrated GaN FQS

Bias Conditions			The operation mode of integrated GaN FQS
G1	G2	V_{T2T1}	
OFF	OFF	>0 or <0	Off
ON	ON	>0 or <0	ON
OFF	ON	>0	OFF
OFF	ON	<0	The current conducts from T1 to T2 with the body diode voltage drop of off Si-MOSFET
ON	OFF	>0	The current conducts from T2 to T1 with the body diode voltage drop of off Si-MOSFET
ON	OFF	<0	OFF

Similar to the Cascode, the threshold voltage of Si-FET determines the BPS's threshold voltage. The Si MOSFETs used in the integrated GaN FQS have a maximum gate voltage rating of +/- 20V and a threshold voltage of 4V, resulting in a robust input interface. The on-state resistance and blocking capability depend on the bidirectional AlGaN/GaN HEMT. The bi-directional AlGaN/GaN HEMT can be seen as two back-to-back connected conventional AlGaN/GaN HEMTs sharing the drift region to reduce the on-state resistance. The on-state resistance of bidirectional AlGaN/GaN HEMT is about 40mΩ. Transphorm's FQS uses the Package on Package (POP) method and the TO247 to reduce parasitic impedance and switching loss. The typical Rdson of FQS is 60mΩ[22]. In addition, the symmetrical field plate is employed to reduce current collapse and enhance the block voltage. The asymmetrical field plate can be designed to achieve different blocking capabilities in different

directions. However, current collapse and a lack of high blocking voltage capability are also issues for bidirectional D-mode GaN HEMT, as mentioned in Sections 2.2.4 and 2.2.5.

To enhance breakdown voltage (BV) and to suppress current collapse, the normally-on GaN-based bidirectional Super Heterojunction Field Effect Transistors (BiSHFETs) using the PSJ concept on Sapphire Substrate were first demonstrated in 2012[103]. It integrates anti-series two PSJ HFETs in common-drain. Figure 2.4.16 shows the Schematic cross-section of BiSHFETs with (a) Metal Semiconductor (MES) and (b) PN junction gate structures. The 1μm-thick GaN/47nm-thick AlGaN/GaN double-heterostructure on 3" Sapphire substrates with an Al composition of 23%. An Mg-doped ($3\times10^{19}cm^{-3}$) p-GaN layer has been grown on the top undoped GaN layer. 2DHG and 2DEG are formed at the upper GaN/AlGaN and bottom AlGaN/GaN interfaces.

As the example of BiSHFETs with MES-gate (i.e. Schottky Gate), it has seven electrodes. In this study, base1(B1) and (B2) are ohmic contact to 2DHG and are connected with the adjacent Gate, as shown in Figure 2.4.16. Source1 (S1) and Source2 (S2) form ohmic contacts to 2DEG, while both gates are Schottky contacts. The floating metal (FM) is ohmic to 2DEG and prevents punch-through between the base electrode by acting as a channel stopper[103]. Thus, the BiSHFETs can be performed as four-terminal devices. Similar to the unidirectional PSJ HFETs, BiSHFETs are normally-on devices. The on-state current can flow through the 2DEG channel in both directions and is controlled by gate electrodes. Figure 2.4.17 shows the measured (a) I_s-V_{s1s2} characteristics and (b) transfer characteristics of fabricated BiHFETs with MES gate and PN gate in both directions[103].

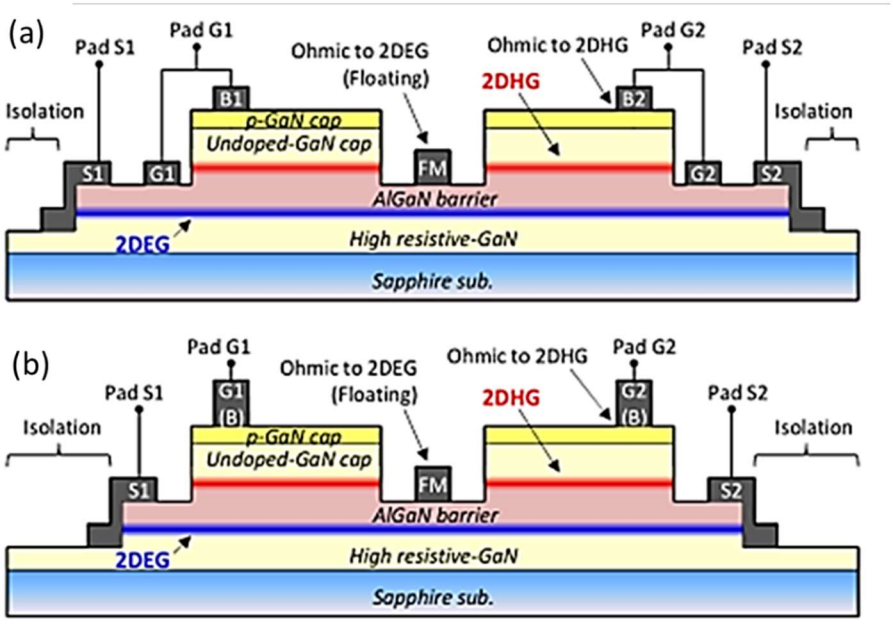


Figure 2.4.16: Schematic cross-section of BiSHFETs with (a) MES-gate and (b) PN-gate structures.

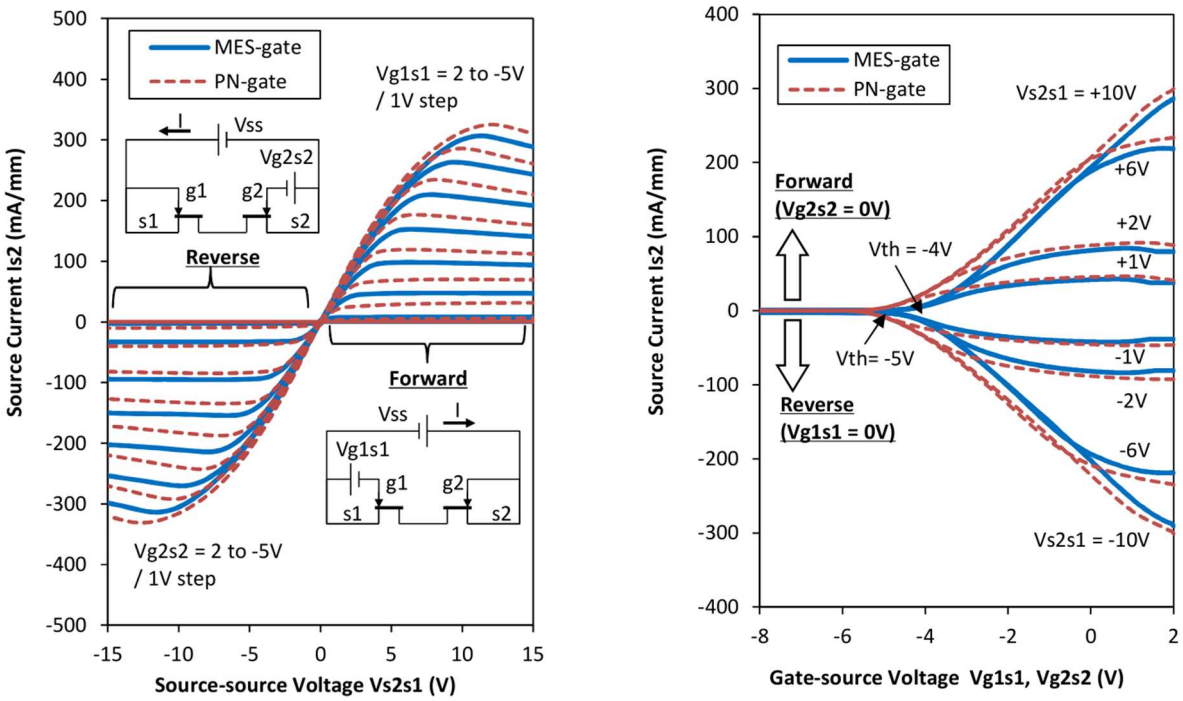


Figure 2.4.17: (a) Measured Is-Vs1s2 characteristics and (b) measured transfer characteristics of fabricated BiHFETs in both directions[103].

In the off-state, 2DEG and 2DHG can be depleted under the gate region due to the charge balance. The voltage almost uniformly drops over the PSJ region of one of anti-parallel two PSJ HFETs. It is similar to unidirectional devices in that the length devices determine the breakdown voltage.

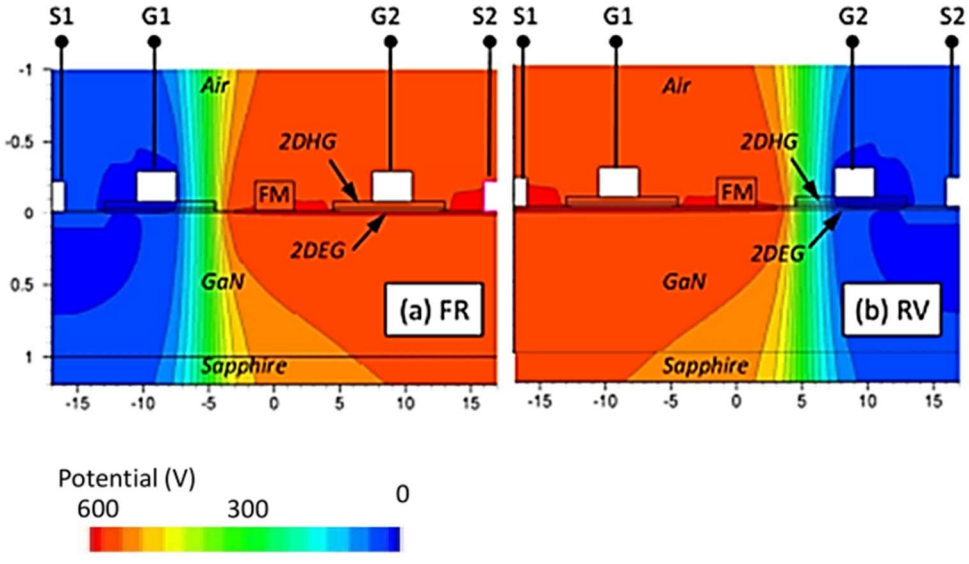


Figure 2.4.18: Simulated contour plots of electrical potential in (a) Forward region (FR) and (b) Reverse Region (RV).

2.5 Transfer Length Method (TLM)

The total resistance (R_T) of lateral semiconductor power device can be divided into three components: The semiconductor resistance (R_{semi}), contact resistance (R_c) due to the contact metal and the metal resistivity (R_m) associated with the metal / semiconductor interface. Since the metal resistivity (R_m) is tiny which can be ignored, the total on-state resistance can be expressed by the below equation:

$$R_T = 2R_m + 2R_c + R_{semi} \approx 2R_c + R_{semi} \ (R_m \ll R_c) \quad \text{------ (2.18)}$$

The source/drain contact resistance is an important criterion and is always monitored to evaluate ohmic contact and process stability in GaN industry. The high contact resistance can cause the significant voltage drops and heating in the circuits with the high current. Transfer Length Method (TLM) is a common method to extract the contact resistance. The typical arrangement for a TLM test pattern is shown in Figure 2.5.1. The grey region is the contact area with the uniform doping concentration while five brown square is ohmic contacts separated by various distances (L) is on the top of the active region. The width of contacts is W. Applying a voltage to one contact and keeping all details the same, the total resistance R_T between pairs of contacts with different distance can be measured with the four-point-probe or van der Pauw methods. The contact resistance depends on the size of the contact. However, in practice, the physical contact area is not usually equal to the effective contact area.

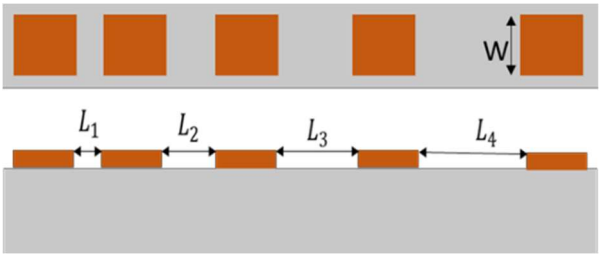


Figure 2.5.1: The typical arrangement for a TLM test pattern

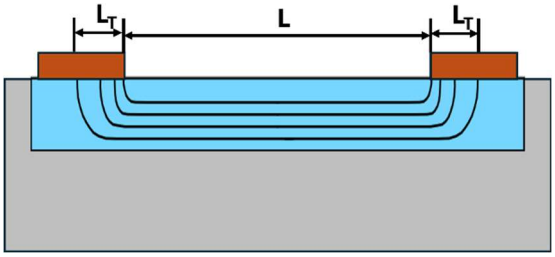


Figure 2.5.2: The cross-section of two adjacent contacts with the effective length

For a planar geometry, the current flows into/out the contact is not uniform because of the current crowding. Moving far away from the edge of the contact, the current drops to zero in an exponential fashion with the effective length L_T, shown in Figure 2.5.2. L_T is known as the transfer length and equals to[104]:

$$L_T = \sqrt{\frac{\rho_c}{R_s}} \quad \text{------ (2.19)}$$

Where ρc is contact resistivity and R_s is the sheet resistance.

Thus, the effective area of the contact (Ac) is L_TW. And the contact resistance (Rc) can be written in:

$$\boldsymbol{R_c = \frac{\rho_c}{L_T W} = \frac{R_s L_T}{W}} \qquad \text{------(2.20)}$$

The semiconductor resistance R_{semi} equals to $\frac{R_s L}{W}$ and the total resistance R_T equals to:

$$R_T = 2R_c + R_{semi} = 2 * \frac{R_s L_T}{W} + \frac{R_s L}{W} = \frac{R_s}{W}(2L_T + L) \qquad \textbf{------(2.21)}$$

According to **Error! Reference source not found.**, from the plot of R_T versus distance (L) shown in Figure 2.5.3, the sheet resistance (R_s), the contact resistance(Rc), the effective length (L_T) and contact resistivity (ρc) can be measured.

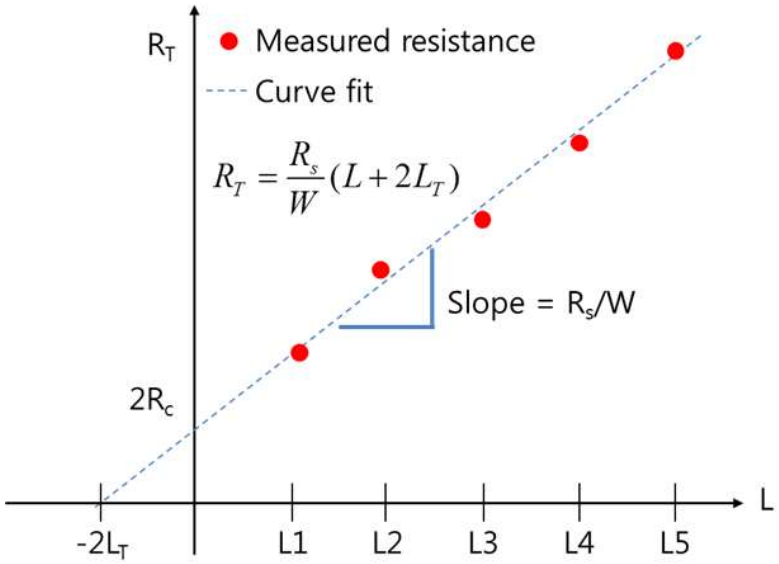


Figure 2.5.3: The total resistance (Rc) vs the distance (L)[104]

The residual resistance would be just twice the contact resistance Rc if distance(L) is limited to 0. The transfer length L_T is the half of the intercept by extrapolating back to the horizontal axis. And the sheet resistance Rs can be extracted from the slope of the line and equals to:

$$R_s = slope * W \qquad \text{------ (2.27)}$$

The contact resistivity ρc, the main parameter characterized the ohmic contact, can be derived from **Error! Reference source not found.** and equals to:

$$\rho c = RcL_T W \qquad \text{------(2.28)}$$

2.6 Summary

This chapter introduces and discusses the intrinsic material properties of GaN in wurtzite structure, including spontaneous and piezoelectric polarization. The polarization engineering of 2DEG and 2DHG is concerned. The discovery of a high-density and high-mobility 2DEG spontaneously induced at AlGaN/GaN hetero-interface promotes the development of AlGaN/GaN High Electron Mobility Transistor (HEMT) Technology. The operating principles of the conventional lateral GaN-HEMTs are presented, as well as electric profile issues. A brief review of Field-Plate and Gate Injection Transistor technologies is provided, which are adopted as solutions for high-voltage devices in lateral GaN-based devices. Then, this chapter introduces the recently adopted PSJ technologies, as well as physical mechanisms and electrical characteristics. Compared with conventional lateral AlGaN/GaN devices, PSJ structure can improve the breakdown voltage. Last, it provides a brief view of common Bidirectional Power Switch (BPS) using discrete unidirectional devices and monolithic GaN-based BPS.

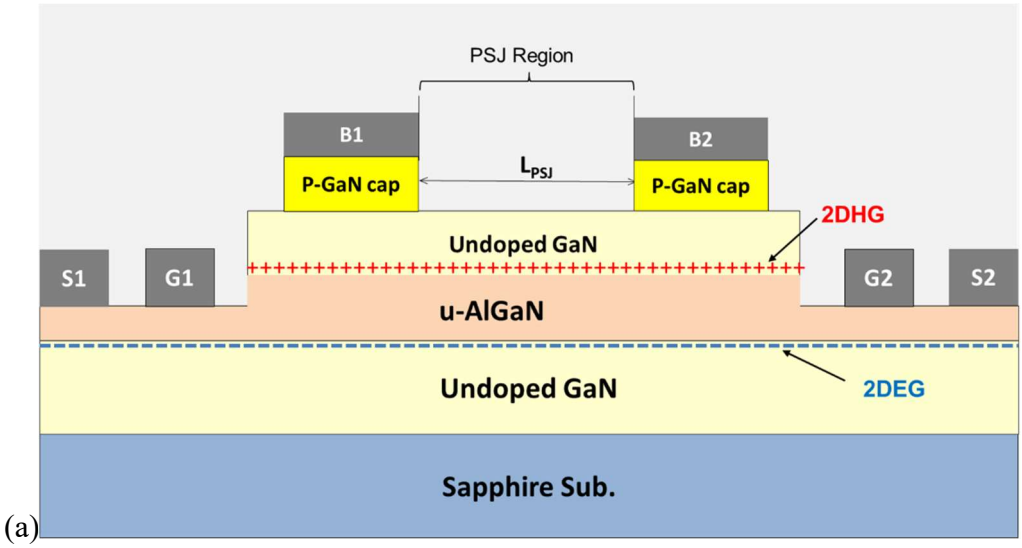
Chapter 3: Compact Monolithic Bidirectional PSJ HFETs

In 2012 GaN-based bidirectional Super Heterojunction Field Effect Transistors (BiSHFETs) using the PSJ concept were first demonstrated, integrating anti-series two PSJ HFETs in common-drain[103]. This chapter proposes the compact monolithic Bidirectional PSJ HFETs with Schottky Gate (Bi PSJ SG HFETs) and ohmic Gate (Bi PSJ OG HFETs). Compared with BiSHFETs, devices reduce the overall size by cancelling the drain electrode located in the middle and two anti-connected PSJ HFETs share the same drift region. It introduces the fundamental structure and operation mode of Bi PSJ HFETs. Bi PSJ HFETs are simulated to get insight into the physical mechanisms and electrical characteristics of the devices. On the basis of the simulation results, test structures, large area devices, and process control monitor (PCM) designs will be designed.

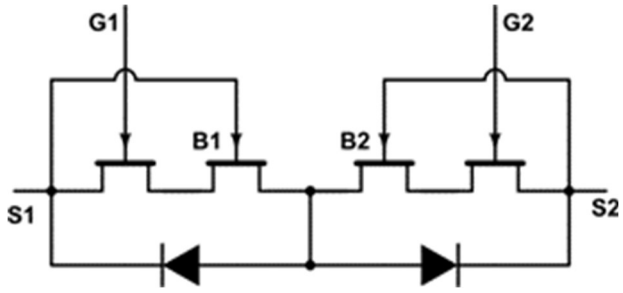
3.1 Bidirectional PSJ HFETs with Schottky Gate

3.1.1 Device structure

Figure 3.1.1(a) shows a simplified cross-section of Bidirectional PSJ HFETs with Schottky Gate (Bi PSJ SG HFETs). It can be seen as anti-series connections of two normally-on PSJ SG HFETs, which share the same drift region. As shown in Figure 3.1.1(a), the basic structure of the Bi PSJ HFET arises from GaN/AlGaN/GaN double heterostructures, which employ an inherent charge balance in the PSJ region. It is a symmetrical device with six electrodes. There are two source electrodes (S1 and S2), two base electrodes (B1 and B2), and two gate electrodes (G1 and G2). S1 and S2 form ohmic contacts to 2DEG, while G1 and G2 form Schottky contacts. Two base electrodes (B1 and B2) are ohmic to 2DHG and can be connected to the sources (S1 and S2) or the gates (G1 and G2) to form four-terminal devices. The Device with Schottky Gate can present an inherent body diode so that it can display reverse conducting properties when bases are connected with nearby sources or gates. The distance between two base electrodes is defined as the length of the PSJ region (L_{PSJ}). Similar to unidirectional PSJ HFETs, the L_{PSJ} is used to support the forward blocking voltage and can be scaled up directly as a function of its length ([83], [88]). Base (B1 and B2) electrodes in the simulation are connected to the adjacent sources acting as a four-terminal device, as the equivalent circuit shown in Figure 3.1.1(b).



(a)



(b)

Figure 3.1.1:(a) The cross-section of Bidirectional PSJ HFETs with Schottky Gate. (b) The equivalent circuit of Bi PSJ SG HFETs

3.1.2 Device simulation

Figure 3.1.2 shows the simulation structure of Bi PSJ SG HFETs. An un-doped GaN/AlGaN/GaN double heterostructures have been grown on the sapphire substrate. It consists of an 800nm-thick undoped GaN layer (u-GaN), a 47nm-thick un-doped AlGaN layer with a 23% Al composition and a 20nm-thick un-doped GaN layer. In a similar manner as PSJ devices, 2DEG and 2DHG are spontaneously formed at the AlGaN/GaN and GaN/AlGaN interfaces and keep the charge balance due to polarization charges at zero bias [85]. A 17nm-thick p-type doped GaN cap (P-GaN) layer with $5 \times 10^{19} cm^{-3}$ and a 3nm-thick P-GaN layer with $2 \times 10^{20} cm^{-3}$ have been grown on u-GaN, which enable Bases as ohmic contacts to 2DHG. Mg dopants do not influence the calculation of 2DEG and 2DHG due to the positive sheet charge density induced from P-GaN layer is much lower than 2DHG as Mg active percentage is estimated 1% at 300K [88].

Similar to typical bidirectional switchers, it can conduct the on-state current in both directions and works in the first and third quadrants. For the convenience of description, according to a condition of Source 2 voltage with respect to Source1 voltage (V_{s2s1}), electrical characteristics can be divided

into two regions, which are defined as 'Forward Region' (i.e. The first quadrant) and 'Reverse Region' (i.e. The third quadrant), as shown in Figure 3.1.3. Here, the 'forward' refers to the S2 voltage being positive with respect to S1 (V_{s2s1}>0), and the 'reverse' refers to V_{s2s1} as negative (V_{s2s1}<0).

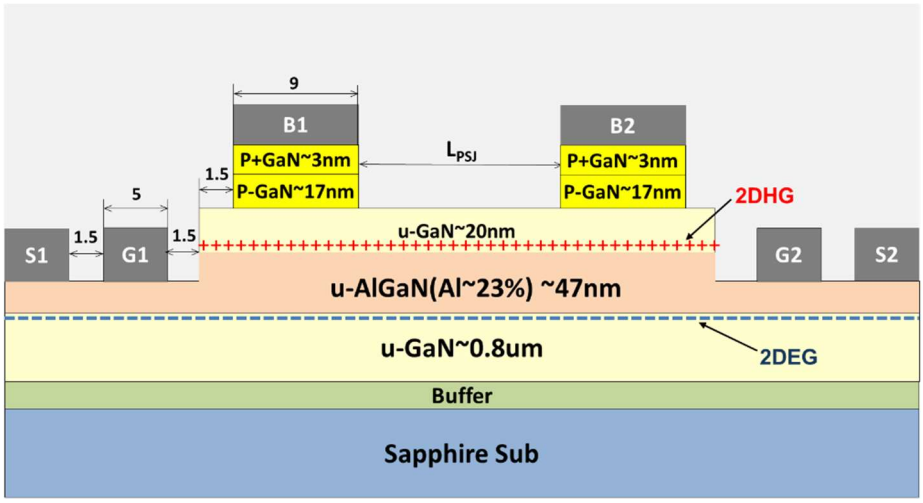


Figure 3.1.2:The cross-section of simulated Bidirectional PSJ HFETs with Schottky Gate. c

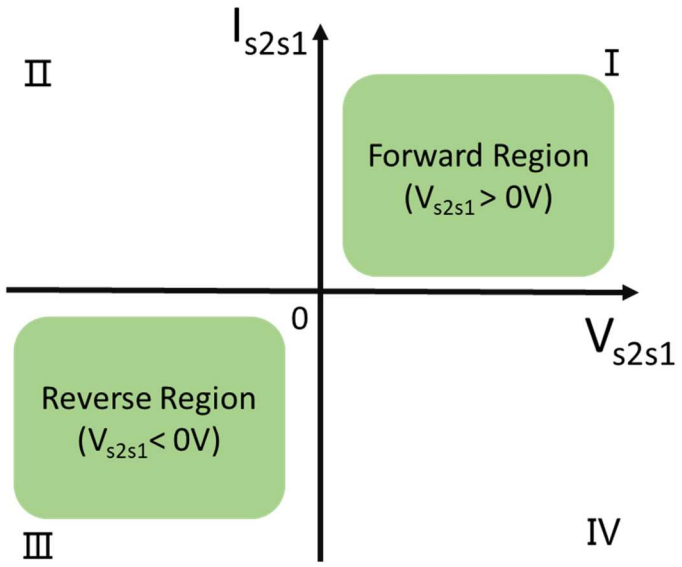


Figure 3.1.3: 'Forward region' and 'Reverse region' defined according to Vs2s1.

TCAD Silvaco Atlas physics-based device simulation software is used in this chapter to simulate the performance of Bi PSJ HFETs. The main models with their descriptions used in the simulation work are shown in Table 3.1.

Table 3.1: Models and Parameters used in Silvaco TCAD simulation[105].

Statement:	Description
CONSRH	Specifying concentration-dependent lifetime
AUGER	Specifying Auger recombination.
FERMIDIRAC	Specifying that Fermi-Dirac carrier statistics be used.
POLARIZATION	Specifying Polarization and Piezoelectric Effects
POLAR.SCALE	Specifying a constant scale factor multiplied by the calculated spontaneous and piezoelectric polarization charges.
CALC.STRAIN	Specifying that the strain in the region is calculated from the lattice mismatch with adjacent regions.
ALBRCT.N	Enable the Albrecht mobility model.
GANSAT.N	Turns on the Nitride Field-Dependent mobility model for electrons.
LAT.TEMP	Specifying that the lattice temperature equation will be solved.
Numerical method:	
NEWTON	Specifying that Newton's method will be used as the solution method.

3.1.3 Input characteristics

The transfer characteristics of Bi PSJ SG HFETs with various L_{PSJ} in both directions obtained via numerical simulation are plotted in Figure 3.1.4(a)-(b) with the simplified testing circuit. In the Forward Region (V_{s2s1}>0V), G2 is connected with S2. Applying with Gate voltage from 0V to -10V, Bi PSJ SG HFETs turn off at around -6V for different PSJ lengths. In the Reverse Region (V_{s2s1}<0V), G1 is connected with S1, as the testing circuit shown in Figure 3.1.4(b). Applying the Source voltage V_{s2s1} of -10V, the source current flows from S1 to S2 and cut off around -6V of $V_{g2s2.}$ The Simulated reverse characteristics of I_{s2s1}-V_{s2s1} are identical to that in the forward region because Bi PSJ SG HFETs have a symmetrical structure.

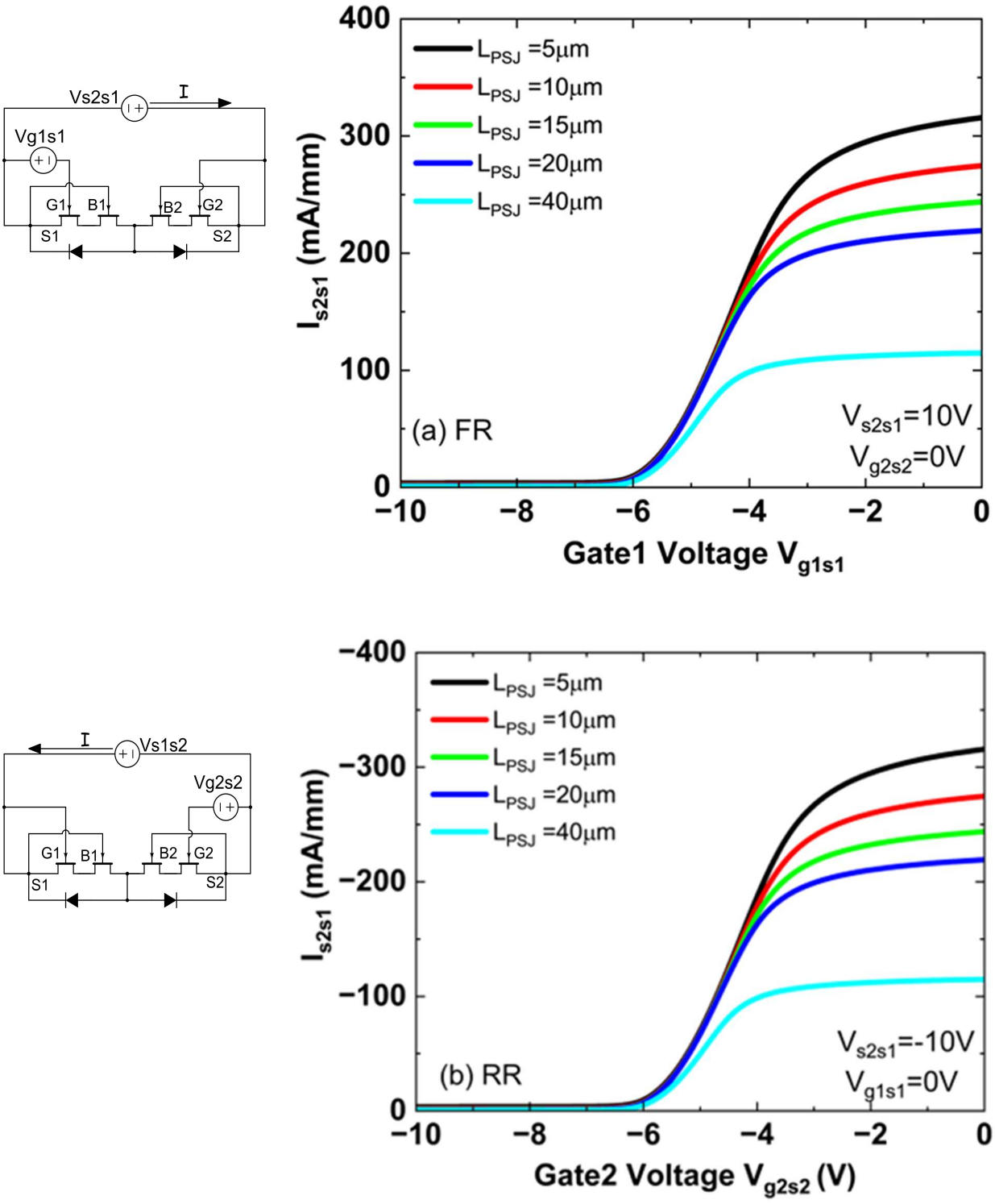


Figure 3.1.4: Transfer characteristics of Bi PSJ SG HFETs with various L_{PSJ} in (a) Forward Region and (b) Reverse region with relative testing circuits.

3.1.4 Output I-V Characteristics

Figure 3.1.5 shows simulated symmetrical I_{s2}-V_{s2s1} characteristics of Bi PSJ SG HFETs with 40µm-L_{PSJ} working in both directions. In the forward region, Gate2 is connected to adjacent S2 (V_{g2s2}=0V) while the Voltage of Gate1 changes from -6V to 0V with a 1V step, as shown in the inset circuit in Figure 3.1.5. According to Figure 3.1.4, PSJ SG HFETs has the negative threshold voltage of -6V. Therefore, PSJ SG HFET on the right-side is turned on due to V_{g2s2} =0V. In a manner similar to a conventional HFET, the forward current I_{s2} flows from S2 to S1 through the 2DEG and is controlled by Gate1 voltage (V_{g1s1}). As V_{g1s1} reduces to less than -6 V, the device enters off-state. The simulated forward on-state resistance (R_{on}) for L_{PSJ}=40µm is 34.6 mΩ.mm at V_{s2s1}=1V, V_{g1s1}=0V. In the reverse region, Gate1 is connected with Source1. PSJ SG HFET on the right-side is turned on due to 0V V_{g1s1} is large than V_{th}. Simulated reverse characteristics of I_{s2}-V_{s2s1} are identical to that of forward because Bi PSJ SG HFETs.

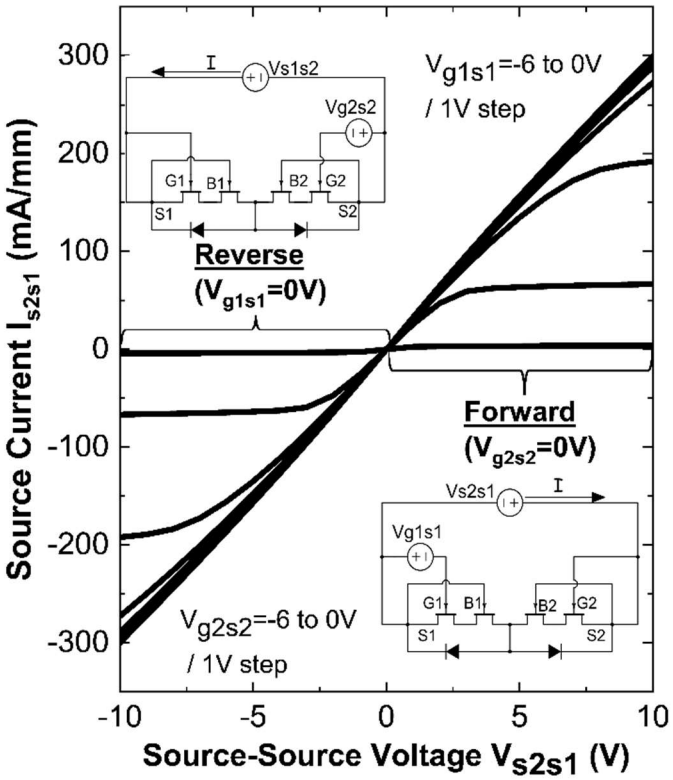


Figure 3.1.5: Simulated Is-Vs2s1 characteristic of Bi PSJ SG HFETs in both conditions.

Figure 3.1.6 shows the I_{s2}-V_{s2s1} characteristics of Bi PSJ SG HFETs with various L_{PSJ} in both directions when V_{g1s1}=0V, V_{g2s2}=0V. The current density decreases with increasing the L_{PSJ} due to the 2DEG channel resistance is proportion to the L_{PSJ}.

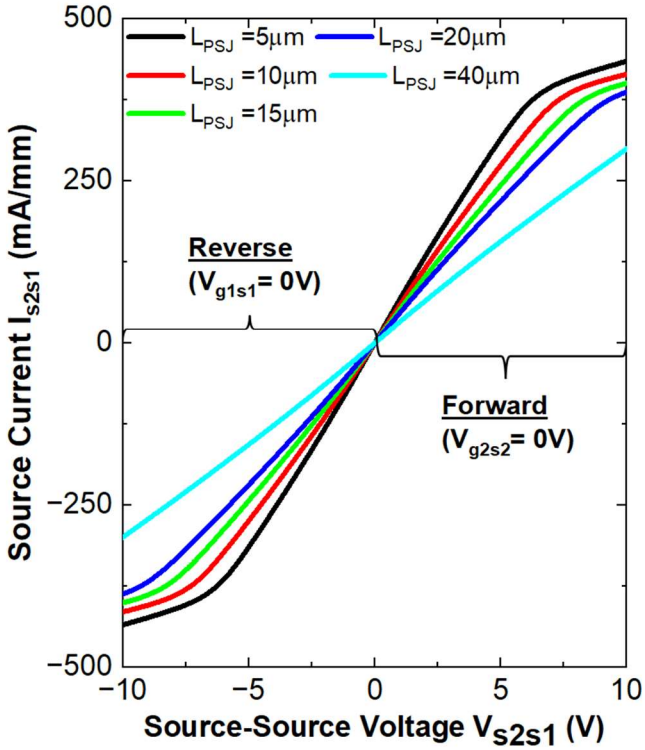


Figure 3.1.6: Simulated Is2-Vs2s1 characteristics of Bi PSJ SG HFETs with various L_{PSJ} in both directions when Vg1s1=0V, Vg2s2=0V.

According to Figure 3.1.5, the behaviour of Bi PSJ SG HFETs can be summarised in Table 3.2.

Table 3.2: Summarised device behaviours.

Bias conditions			**Device State**
V_{s2s1}	**V_{g1s1}**	**V_{g2s2}**	
V_{s2s1}>0	On	On	On
(Forward Region)	Off		Off
V_{s2s1}<0	On	On	On
(Reverse Region)		Off	Off

When one of PSJ SG HFETs in Bi PSJ SG HFETs turns off by applying a negative voltage smaller than the threshold voltage, devices behave as a diode. Figure 3.1.7 shows the simulated I_{s2}-V_{s2s1} characteristics are obtained when keeping a negative Gate2 voltage with respect to Source2 at -9V (V_{g2s2}=-9V) in the forward region while keeping V_{g1s1}=-9V in the reverse region. Although the on-state voltage increases, the source current I_{s2s1} in the forward and reverse bias condition is successfully controlled by Gate1 voltage (V_{g1s1}) and Gate2 voltage (V_{g2s2}). The main reason for the increased 'forward' on-state voltage is that the 2DEG under Gate2 is fully depleted when Gate2 voltage applies with a negative voltage smaller than the threshold voltage. Therefore, the region under Gate2 performs

as a diode depletion region. The calculated 'forward' on-state voltages (V_{on})at I_{s2} = 10mA/mm is 0.4 V (V_{g2s2} = 0 V) and 3.1 V (V_{g2s2} = -9 V), respectively. Figure 3.1.8 shows the I_{s2}-V_{s2s1} characteristics when V_{g2s2} = -9 V, V_{g1s1}=0V in the Forward region and V_{g1s1} = -9 V, V_{g2s2}=0V in the Reverse region with different L_{PSJ}. The forward IV curves show a decreasing trend toward L_{PSJ} due to the 2DEG Resistance increases, while the on-state voltage keeps constant for various L_{PSJ}.

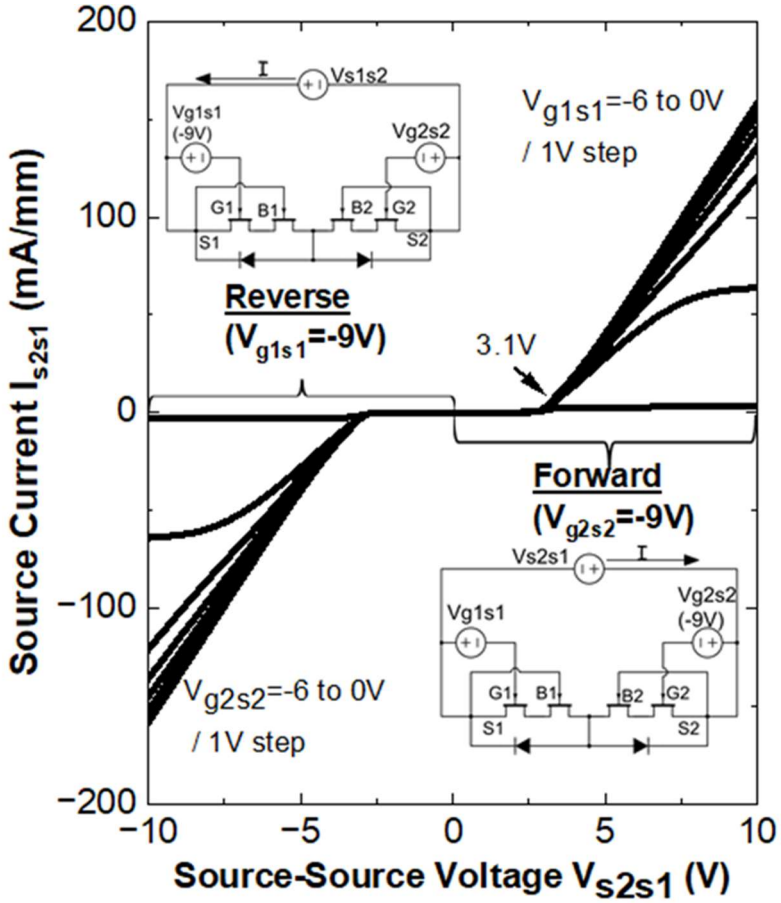


Figure 3.1.7: Simulated Is2-Vs2s1 characteristics of Bi PSJ SG HFETs with 40um-Lpsj when one PSJ SG HFETs turned off.

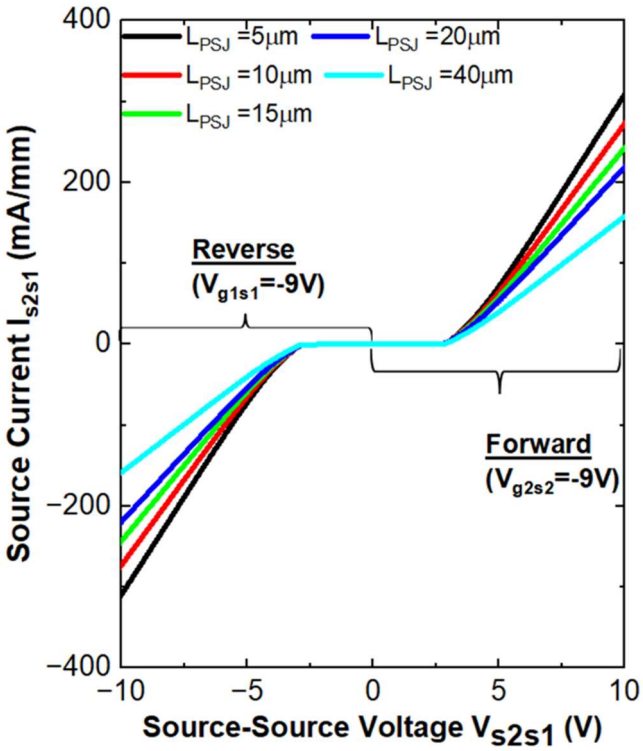


Figure 3.1.8: The simulated Is2-Vs2s1 characteristics of Bi PSJ SG HFETs with various L_{PSJ} in both directions when one PSJ SG HFETs turned off.

Under these bias conditions shown in Figure 3.1.8, the Device's behaviour can be summarised in Table 3.3.

Table 3.3: Summarised device behaviours of Bi PSJ SG HFETs

Bias conditions			**Device State**
V_{s2s1}	V_{g1s1}	V_{g2s2}	
V_{s2s1}>0 (Forward Region)	On	Off	On (V_{on} increase)
	Off		Off
V_{s2s1}<0 (Reverse Region)	Off	On	On (V_{on} increase)
		Off	Off

3.1.5 Voltage Blocking Capability

In the 'forward' off-state, G2 and S2 are connected as 'Drain' of three-terminal devices under a forward bias of V_{s2s1}, as a unidirectional PSJ SG HFET. G1 is applied with -15V to cut off the 2DEG channel, as shown in Figure 3.1.9(a). In the reverse region, G1 and S1 are connected, and G2 is applied with negative voltage to turn off the devices shown in Figure 3.1.9(b).

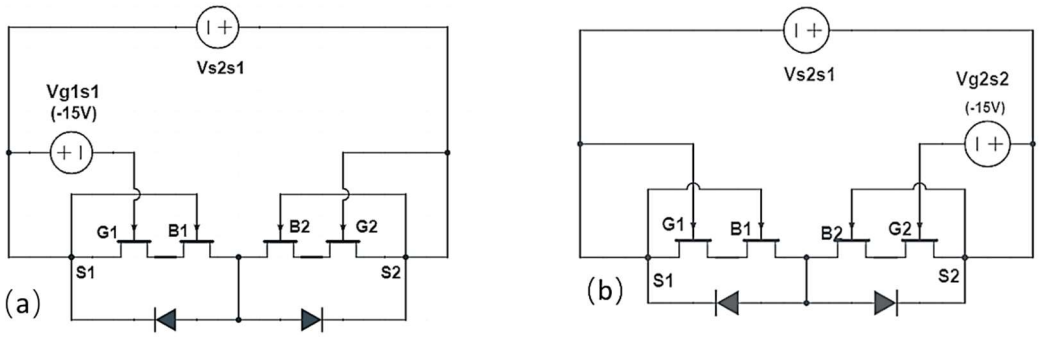


Figure 3.1.9: Simulated testing circuit in (a) Forward Region and (b) Reverse region during off-state.

During off-state, the 2DHG and 2DEG of Bi PSJ SG HFETs are discharged through Base and 'Drain', respectively. The drift region between two bases of the Bi PSJ SG HFET is depleted, thus, electrical field distribution over this region. The 1-D Electric Field along the x-coordinate at a position identified by the black dotted line (A-A') before the breakdown is shown in Figure 3.1.10 under the forward bias. As shown in Figure 3.1.10, the electric field is over the PSJ region, and the breakdown occurs at the edge of the Base.

Simulated off-state I_{s2}-V_{s2s1} characteristics of Bi PSJ SG HFETs various L_{PSJ} in an ideal case are demonstrated in Figure 3.1.11. It shows a linear relationship between breakdown voltage and PSJ length, similar to results on unidirectional PSJ HFETs.

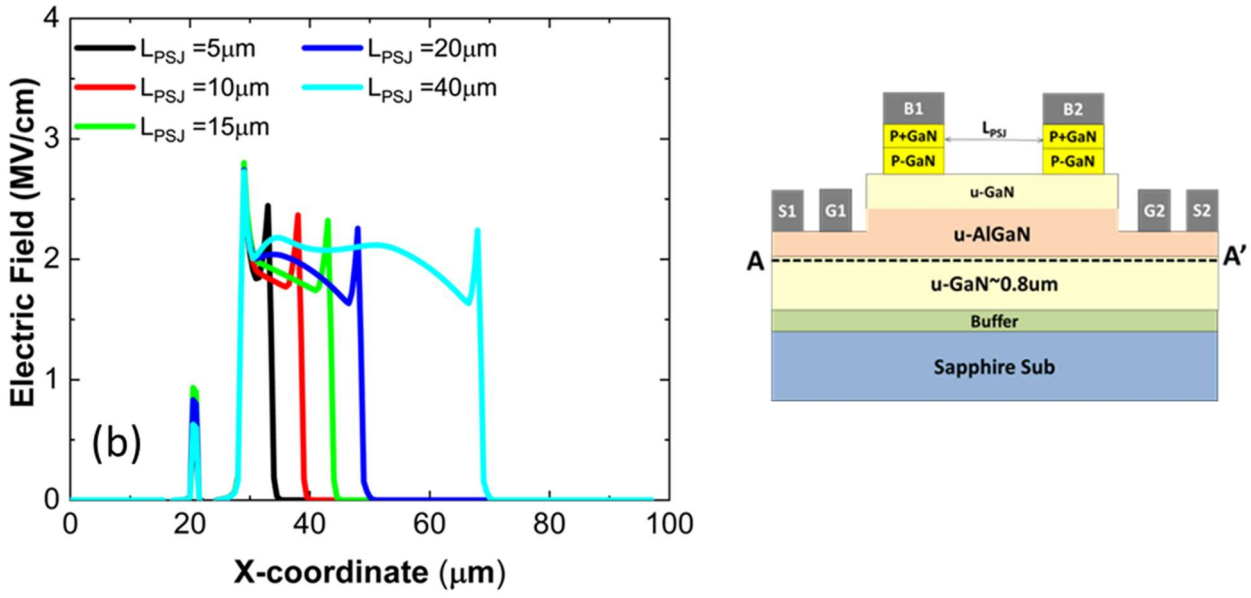


Figure 3.1.10: Simulated 1-D off-state electric field distribution of Bi PSJ SG HFETs at the black dotted line (A-A') with Vg1s1 = -15V in the forward region before the breakdown.

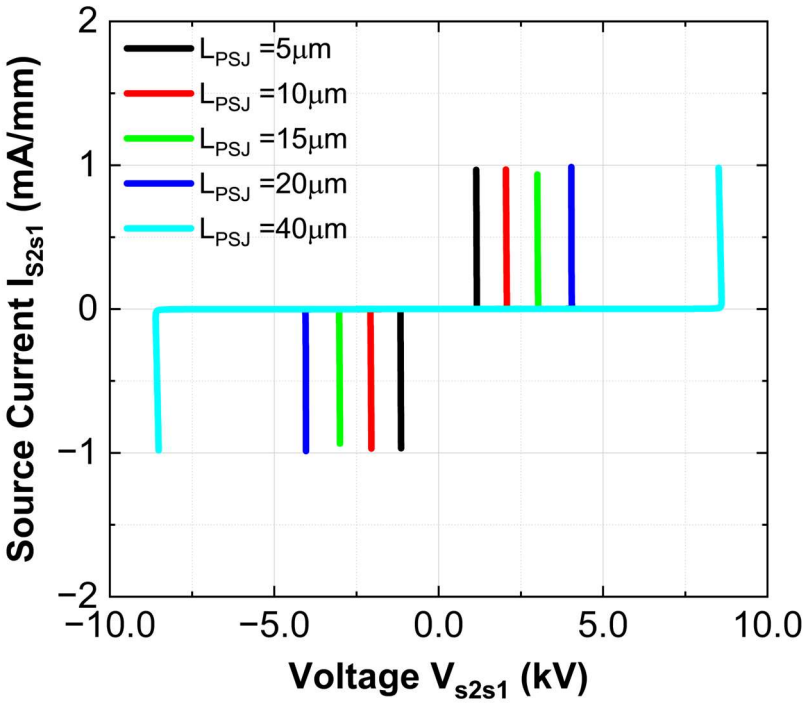


Figure 3.1.11: Simulated off-state I_{s2}-V_{s2s1} characteristics for both polarities.

The simulated off-state Is2-Vs2s1 shows both types of Bi PSJ HFET with a 40µm length can withstand the voltage well above 8 kV in an ideal conditions. Previous results on unidirectional PSJ HFETs show a linear relationship between breakdown voltage and PSJ length([88],[85]). Based on this, conservatively, it can be estimated that BV increases by 500 V for every 5µm increase in L_{PSJ}. Considering that the measured BV is around 2.5kV for a unidirectional PSJ HFET with 20µm-L_{PSJ} on Sapphire[88], a bidirectional device with a 40µm-L_{PSJ} can be reasonably expected to withstand the voltage well above 3.3 kV.

3.1.6 Bidirectional behaviour of Bi PSJ SG HFETs

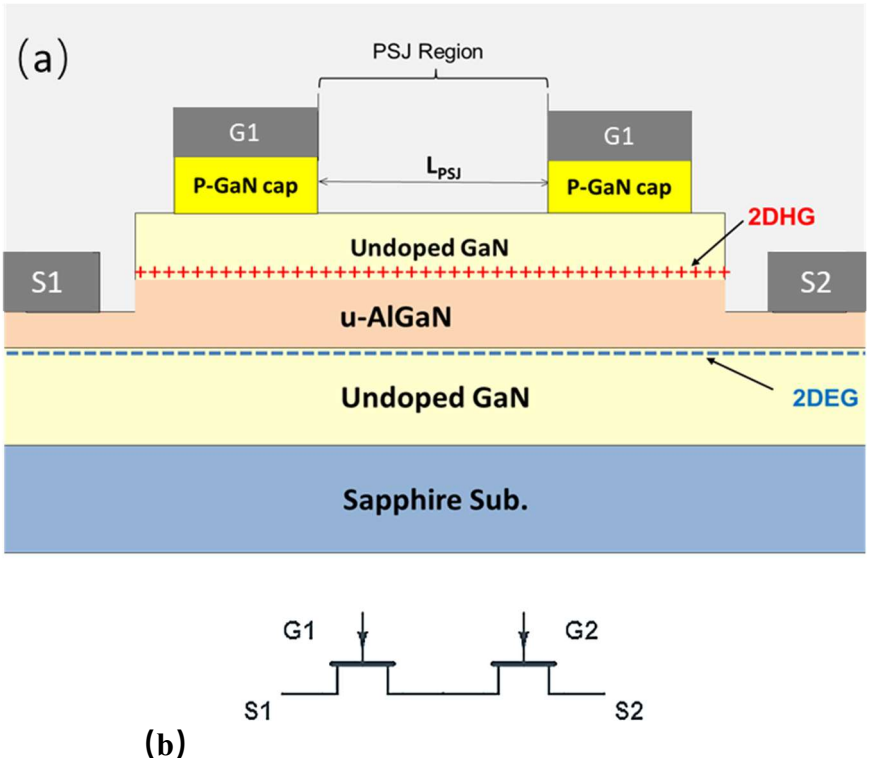
According to the simulated results, the operation behaviour of bidirectional PSJ Schottky Gate HFETs in various bias conditions can be summarised in Table 3.4, which is in agreement with the simulation results of BiSHFETs reported in 2012[5]. When V_{s2s1} is positive, Bi PSJ SG HFETs are controlled by Gate 1, while they are controlled by Gate 2 in a reverse bias condition.

Table 3.4: Summarised device behaviours in various bias conditions.

V_{g1}	V_{g2}	Mode	
OFF	OFF	S1 — S2	Bidirectional Switch mode
ON	ON		
ON	OFF		Diode mode
OFF	ON		

3.2 Bidirectional PSJ HFETs with Ohmic Gate

The cross-section of Bidirectional PSJ HFETs with Ohmic Gate is presented in Figure 3.2.1(a). It can be seen as two anti-parallel PSJ OG HFETs sharing the same L_{PSJ}. It has only four electrodes, two gate electrodes (G1 and G2) and two source electrodes (S1 and S2). Two gates (G1 and G2) on P-GaN have ohmic characteristics to 2DHG. S1 and S2 form ohmic contacts to 2DEG. Figure 3.2.1(b) shows the equivalent circuit of Bi PSJ OG HFETs. Similarly, the on-state current follows through the 2DEG channel in both directions. In off-state, 2DHG and 2DEG between Gate electrodes are depleted. Therefore, the current track is cut off, and the devices turn off. It should be noted that there is a 2DHG channel connecting two gates. In the ideal off-state, 2DHG is depleted by the 2DEG and the mobility of 2DHG is much low around 10~20$cm^2/V.s$, the leakage through two gates is smaller.



(b)

Figure 3.2.1: (a)The cross-section of Bidirectional PSJ HFETs with Ohmic Gate. (b) The equivalent circuit of Bi PSJ OG HFETs

3.2.1 Device simulation

Figure 3.2.2 shows the simulation structure of Bi PSJ SG HFETs. It consists of an 800nm-thick undoped GaN layer (u-GaN), a 47nm-thick un-doped AlGaN layer with an Al composition of 23%, and a 20nm-thick un-doped GaN layer. A 17nm-thick p-type doped GaN cap (P-GaN) layer with $5 \times 10^{19} cm^{-3}$ and a 3nm-thick P-GaN layer with $2 \times 10^{20} cm^{-3}$ have been grown on u-GaN, which enables an ohmic contact to 2DHG. The simulation software is TCAD Silvaco Atlas and the Simulation settings have been introduced in Section 3.1.2.

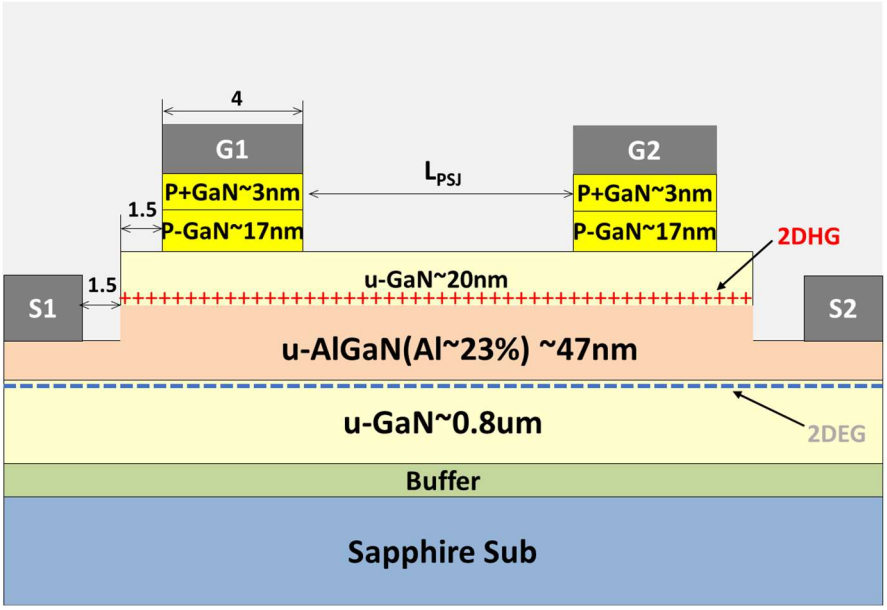


Figure 3.2.2: The cross-section of simulated Bidirectional PSJ OG HFETs. Dimension in µm.

Under different gate bias conditions, Bi PSJ OG HFETs can be operated as unidirectional HFETs with/without Hybrid Drain-embedded Gate Injection Transistor (HD-GIT) mode and diodes in both directions. Take the device working in the forward region as an example,

Table 3.5: Operation of Bi PSJ OG HFETs with different gate bias conditions

Gate bias conditions	Operation mode
G2 is floating	Conventional PSJ OG HFETs
G2 is connecting with S2 (V_{g2s2}=0v)	PSJ OG HFETs with Hybrid Drain-embedded Gate Injection Transistor (HD-GIT).
$V_{g2s2}<V_{th}$	Diode

For HD-GIT mode, S2 is incorporated with G2 on the P-GaN layer as the 'Drain' of a PSJ HFET. When 'Drain' voltage increases during on-state, holes are injected into the GaN device that releases the trapped electrons instantaneously, which increases the current density and reduces the on-state resistance compared with conventional PSJ HFETs. The following simulation results focus on the Bi PSJ OG HFETs acting as unidirectional PSJ OG HFETs with HD-GIT mode and diodes in both polar.

3.2.2 Input characteristics

Figure 3.2.3 shows simulated input $V_{g1}(V_{g2})$-I_{s2s1} characteristics of Bi PSJ OG HFETs with HD-GIT. The PSJ length alters from 5μm to 40μm. The threshold voltage is around -6.5V, lower than Bi PSJ SG HFETs. It means the controllability is better for an SG design

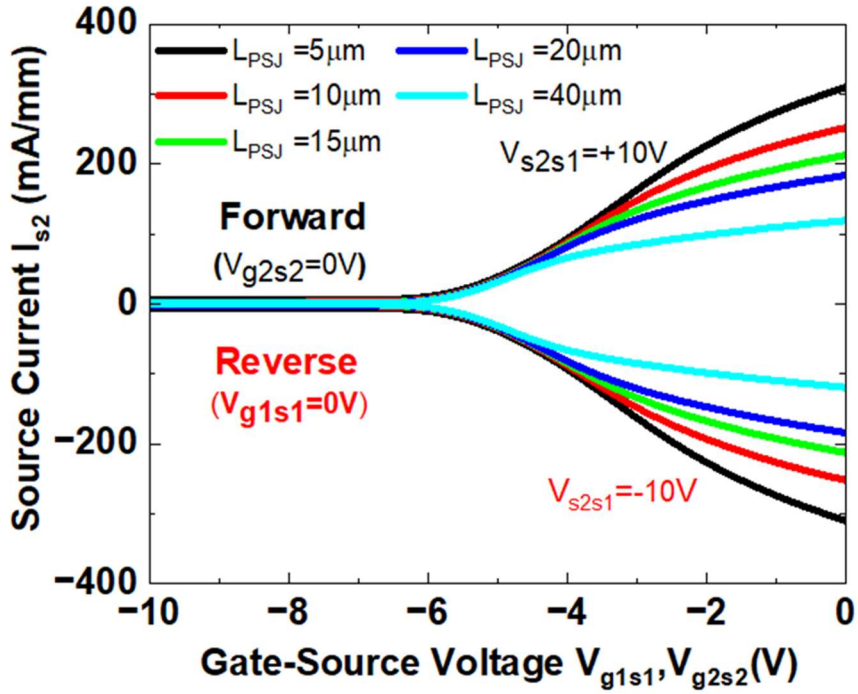
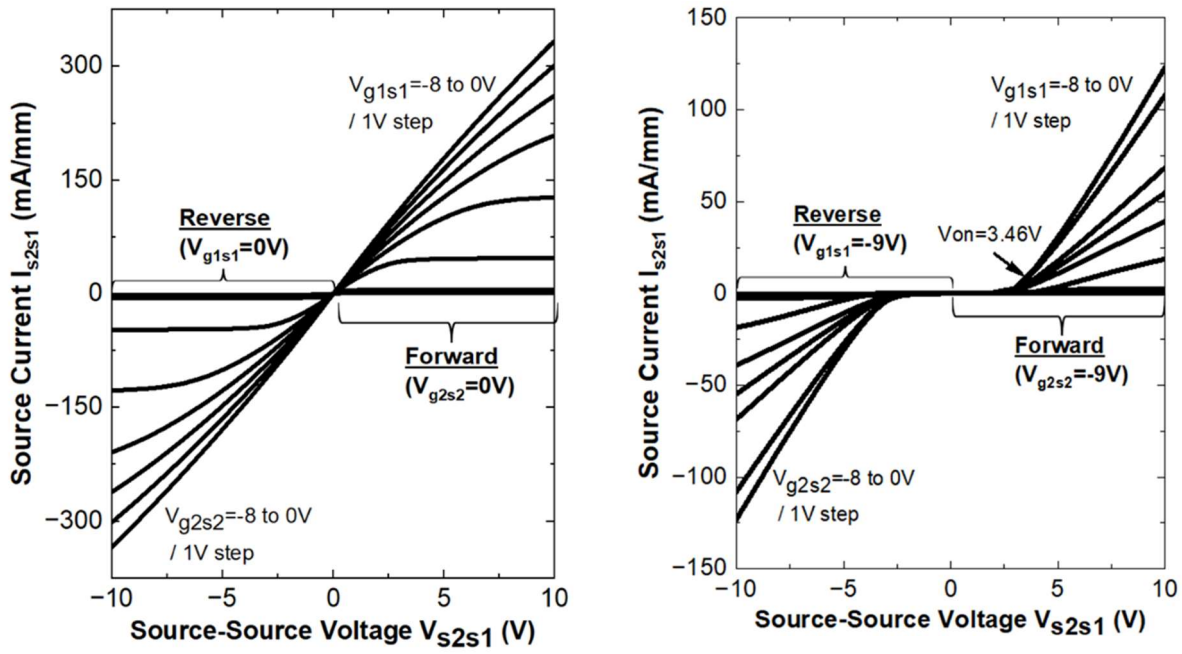


Figure 3.2.3: Transfer characteristics of Bi PSJ SG HFETs with various L_{PSJ} in both polar.

3.2.3 Output I-V Characteristics

Figure 3.2.4(a)-(b) show I_{s2}-V_{s2s1} characteristics of Bi PSJ HFETs with Ohmic gate working in the first and third quadrant. The length of L_{psj} is 40um. The bias conditions are set as the same as that for Bi PSJ SG HFETs. When Vs2s1 is positive, Bi PSJ HFETs are controlled by Gate 1, while Bi PSJ HFETs are controlled by Gate 2 in a reverse bias condition. The On-state Resistance Ron of the Bi PSJ OG HFET calculated from Figure 3.2.4(a) is 31.1mΩ.mm at V_{s2s1}=1V, V_{g1s1}=0V. When Gate1 voltage is smaller than -6.5V, Bi PSJ OG HFETs enter off-state.

The simulated current shown in Figure 3.2.4(b) is obtained by keeping the Gate 2 voltage with respect to Source2 voltage at -9V (V_{g2s2}=-9V) in the forward region and keeping V_{g2s2}= -9V in the reverse region. Bi PSJ OG HFETs works as a diode as mentioned before.



(a) (b)

Figure 3.2.4: Simulated Is2-Vs2s1 characteristics of Bi PSJ HFETs with Ohmic gate working in both the first and third quadrants.

In the 'Forward Region' (V_{s2s1}>0V), keeping Gate 1 voltage at 0V and changing the negative voltage V_{g2s2} from -7V to -15V, the variation of on-state voltage of the Bi PSJ OG HFET with 40um-L_{psj} is shown in Figure 3.2.5(a). Differing from Bi PSJ SG HFETs, the on-state voltage of Bi PSJ OG HFETs depends on the V_{g2s2} in the Forward region, which goes up with the smaller V_{g2s2}. The increasing on-state voltage in Bi PSJ OG HFETs can be attributed to the depletion region being controlled by Ohmic Gate electrodes. Figure 3.2.5(b) demonstrates a linear relationship between negative V_{g2s2} and on-state voltage. The on-state voltage in the 'Reverse Region' (V_{s2s1}<0V) is identical to that of forward because Bi PSJ HFETs are symmetrical. Therefore, Bi PSJ OG HFETs can control the on-state voltage by changing V_{g2s2} in the 'Forward Region' and V_{g1s1} in the 'Reverse Region'. In addition, the on-state voltage determines by the surface trap and the work function of the ohmic gate.

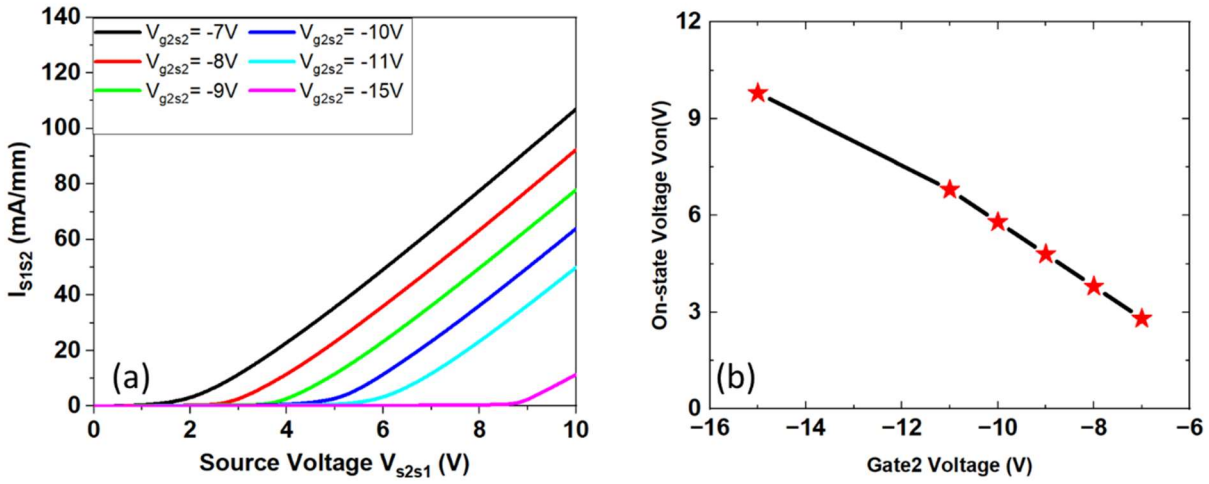


Figure 3.2.5：The simulated on-state voltage of the Bi PSJ OG HFET with 40um-Lpsj when V_{g2s2} =-7~-15V, Vg1s1=0V in the forward region.

Figure 3.2.6 shows the I_{s2}-V_{s2s1} characteristics of Bi PSJ OG HFETs with different PSJ lengths from 5μm to 40μm acting as PSJ FEHTs with HD-GIT and diode mode, respectively. Compared with Bi PSJ SG HFETs, OG structure with the same L_{PSJ} has a higher current density due to the shorter distance between S1 and S2.

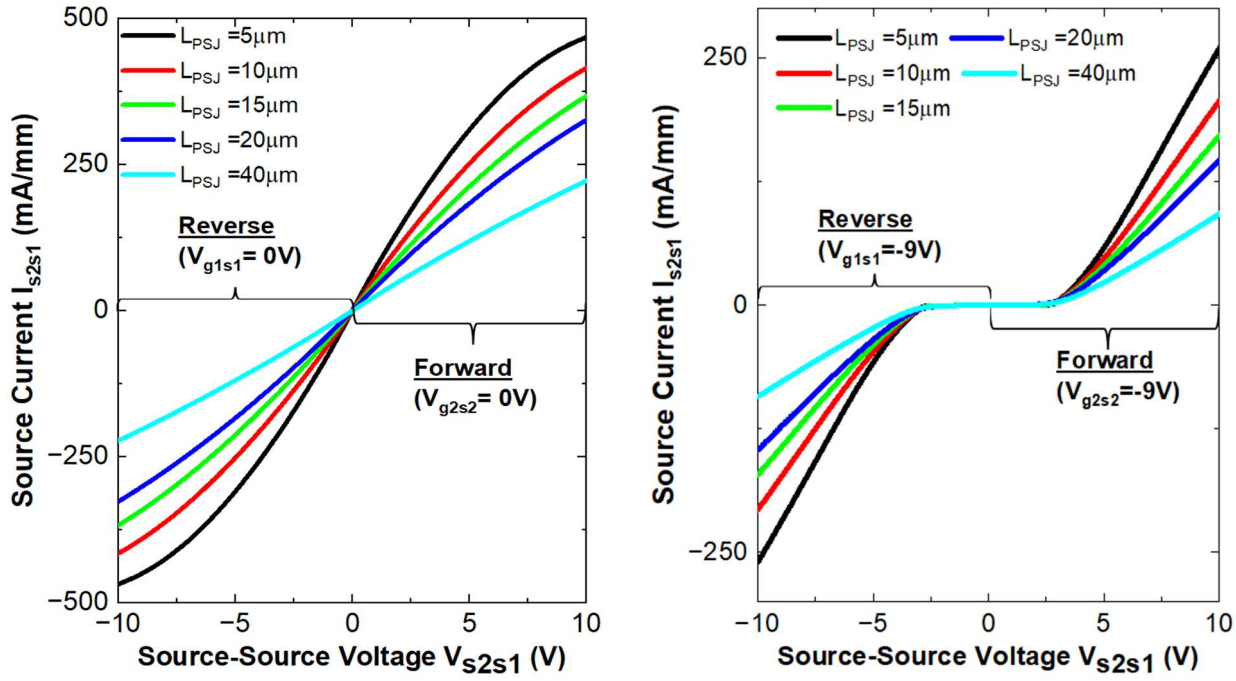


Figure 3.2.6：The I_{s2}-V_{s2s1} characteristics of Bi PSJ OG HFETs with different PSJ lengths from 5μm to 40μm under two bias conditions

According to the simulated results, the function of bidirectional PSJ Schottky Gate HFETs in various bias conditions can be summarised in Table 3.6.

Table 3.6: Summarised device behaviours of Bi PSJ SG HFETs

Bias conditions			Device State
Vs2s1	**V_{g1s1}**	**V_{g2s2}**	
Vs2s1>0	On	On	On
	On	Off	V_{on} increase (Controlled by Vg2)
	Off	On	Off
	Off	Off	Off
Vs2s1<0	On	On	On
	On	Off	Off
	Off	On	$V_{on\ increase}$ (Controlled by Vg1)
	Off	Off	Off

3.2.4 Voltage Blocking Capability

The Simulated forward off-state I_{s2} -V_{s2s1} characteristics of the Bi PSJ OG HFETs with various L_{PSJ} are demonstrated in Figure 3.2.7. It shows that the breakdown voltage is almost identical in OG and SG PSJ HFETs, which are scaled up by the length of PSJ. Figure 3.2.8 shows the simulated 1-D off-state electric field distribution of Bi PSJ OG HFETs at the black dotted line (A-A') with V_{g1s1} = -15V in the forward region before the breakdown. The simulated off-state Is2-Vs2s1 shows Bi PSJ SG HFET with a 40µm length can withstand the voltage well above 8 kV in an ideal condition. In any case, based on measured data of unidirectional PSJ HFETs with 40µm L_{PSJ} fabricated on Sapphire using similar material configurations, off-state performances in excess of 3.3 kV with 1MV/cm critical eletirc field are reasonable. In addition, Figure 3.2.7 shows a snap-back behavior. This is due to the PN junction composed of 2DEG and 2DHG has the avalanche breakdown at the high drain voltage. Thus, BI PSJ OG device is operated with the gate short-circuited to the drain and the resistance goes down. The device enters the snapping back state with a drop in voltage.

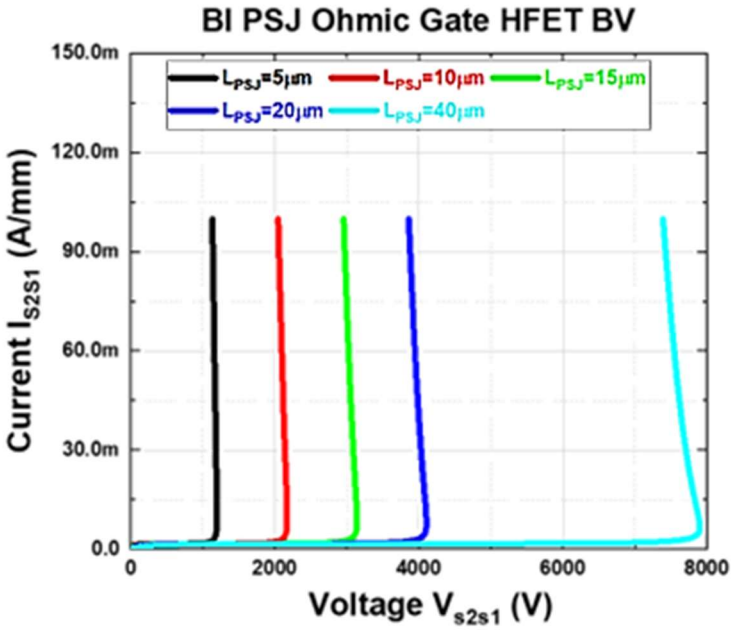


Figure 3.2.7: Simulated forward off-state Is2 -Vs2s1 characteristics of the Bi PSJ OG HFETs

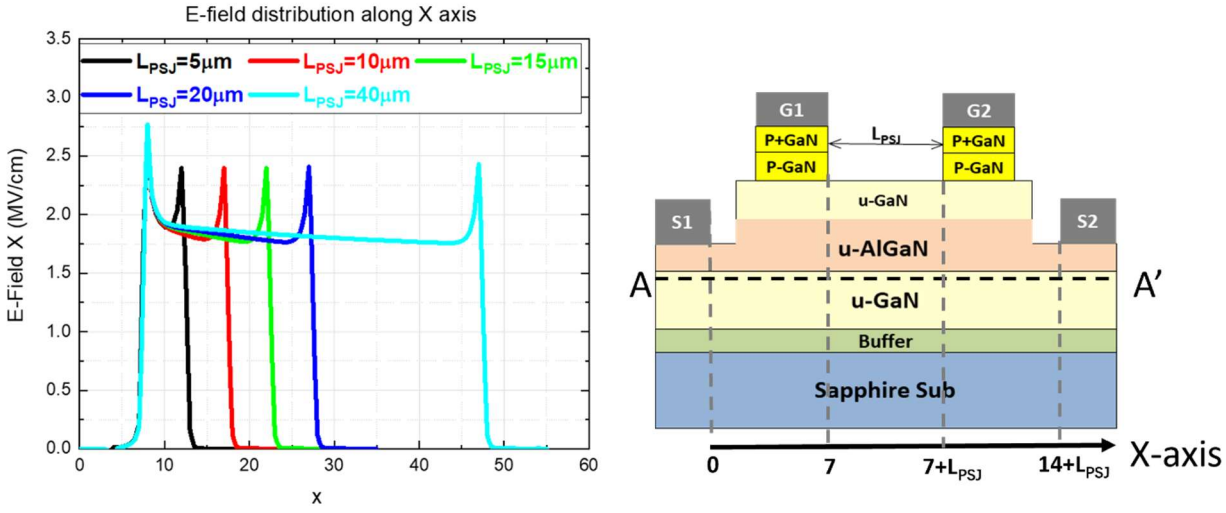


Figure 3.2.8: Simulated 1-D off-state electric field distribution of Bi PSJ OG HFETs at the black dotted line (A-A').

3.3 Design for Bidirectional PSJ HFETs

3.3.1 Design Objectives

This project aims to validate the Bi PSJ HFETS concept and functionality with different gate polarity control. It mainly focuses on test structure. Meanwhile, it is the first time to design and fabricate large-area Bidirectional PSJ HFETs with high current capability on the 6" wafer. Device

design and measurements have been done in Sheffield. Innovate UK supports in sample fabrication work.

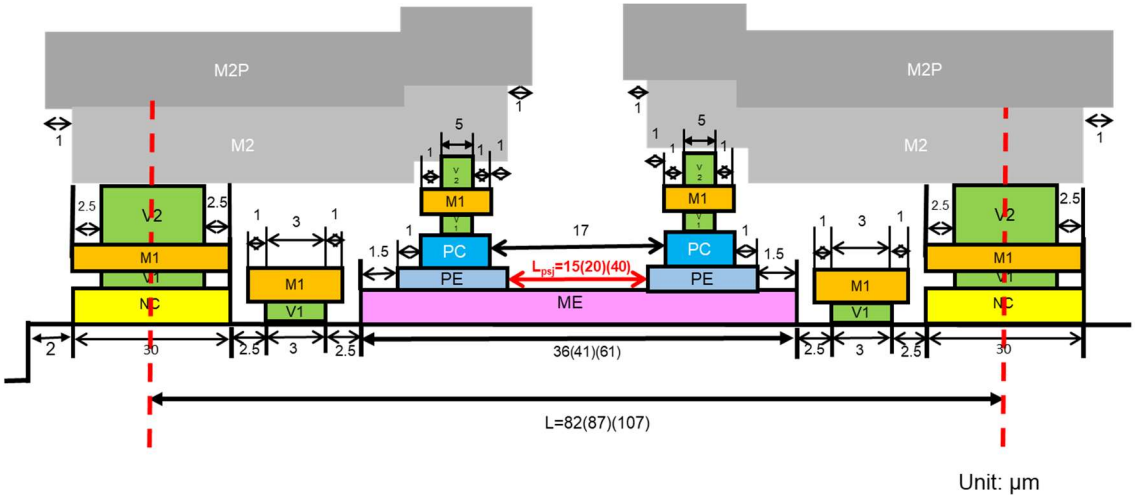
3.3.2 Mask design

The Mask design software used is Klayout. According to the process flow, twelve masks were required for device fabrication in this project, as shown in Table 3.7. the tones or polarities definition of the masks is separated into Light Field and Dark Field. Light Field mask tones are primarily transparent, and drawn features are opaque. Most of the area in a dark field mask is opaque and draws features that are clearly the opposite of the light field The minimum feature size and feasible misalignment are + 0.5μm for photolithography in this fabrication process. To reserve the margin, the design rule for minimum misalignment is identified as + 1μm.

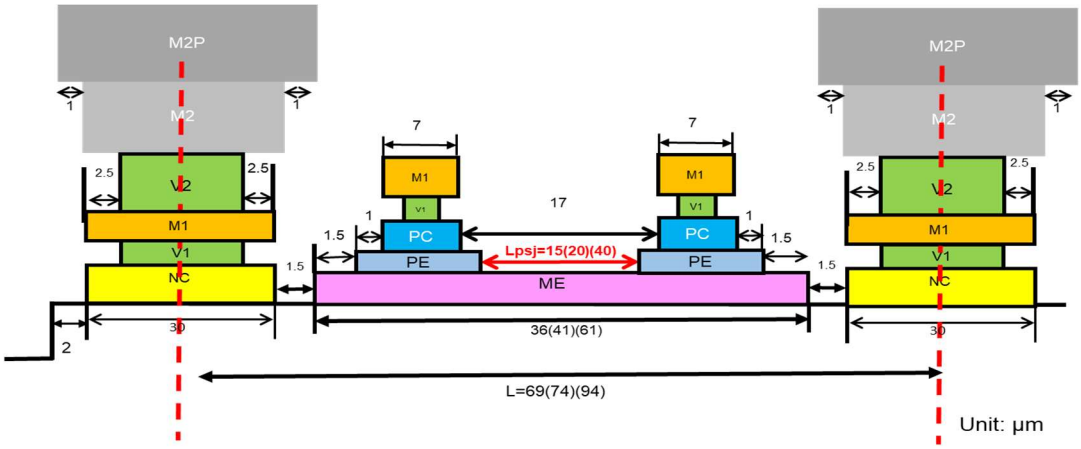
Table 3.7: Mask Information

Layer	Mask/GDS No.	Alias	Mask Tone
AM	0	Alignment Mark	Dark Field
ISO	1	Isolation Etch	Light Field
PE	2	P-GaN Etch	Light Field
ME	3	Mesa Etch	Light Field
NC	4	N Contact	Dark Field
PC	5	P Contact	Dark Field
V1	6	Via 1	Dark Field
M1	7	Metal 1	Dark Field
V2	8	Via 2	Dark Field
M2	9	Metal 2 seed	Dark Field
M2P	10	Metal 2 plated	Dark Field
Pad	11	Pad	Dark Field
PAS	12	Passivation	Dark Field

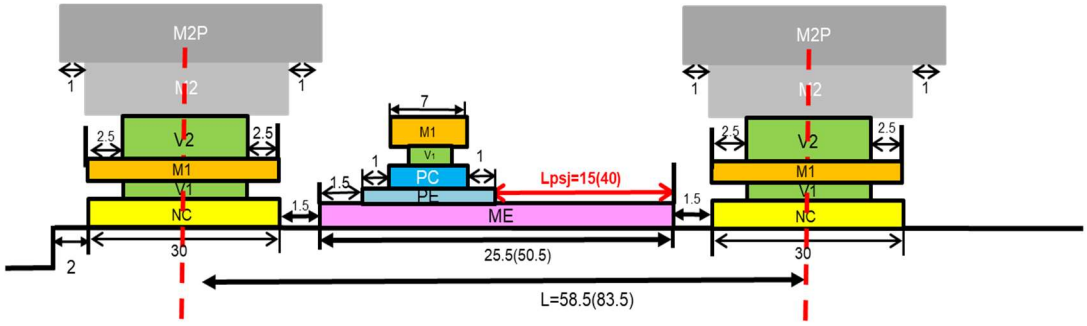
Figure 3.3.1 (a) and (b) present design rules for the primary cell for large-area Bi PSJ SG HFETs, Bi PSJ OG HFETs, unidirectional PSJ OG HFETs and PSJ Diode with 15/20/40μm L_{PSJ}, respectively. In this work, the designed gate width was large enough to prevent breaking but increase the resistance under this region.


M2P
M2
V2
M1
V1
NC
PC
PE
ME
17
Lpsj=15(20)(40)
36(41)(61)
L=82(87)(107)
Unit: μm

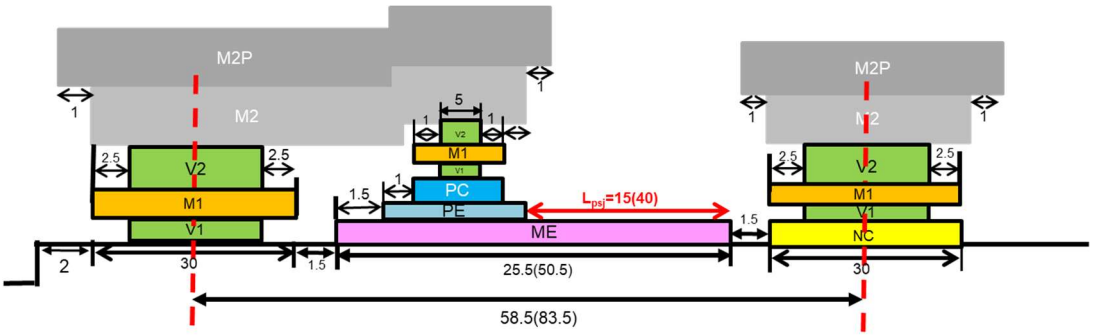
(a)


M2P
M2
V2
M1
V1
NC
PC
PE
ME
17
Lpsj=15(20)(40)
36(41)(61)
L=69(74)(94)
Unit: μm

(b)


M2P
M2
V2
M1
V1
NC
PC
PE
ME
Lpsj=15(40)
25.5(50.5)
L=58.5(83.5)

(c)



(d)

Figure 3.3.1: Feature size of (a) Bi PSJ SG HFETs basic cell (b) Bi PSJ OG PSJ basic cell (c) PSJ OG HFETs basic cell (d) PSJ Diodes basic cell.

3.3.3 Multi-finger layouts for large-area devices

In this project, large-area Bi PSJ HFETs are designed and fabricated to analyse device properties. The current capability of Bi PSJ HFETs was set to 1A,2A,5A and 10A. Similar to the typical large-area power GaN device layout, it employs multi-finger layouts, which can be seen as paralleling cells, for a high current rating. Figure 3.3.2 is the top view of a multi-finger layout for PSJ HFETs. Two Gate Pads and a Source pad are employed on one side of the device, while the Drain Pad is on the other. Metal tracks connect Gate, Source, and Drain Pad to corresponding electrodes in the Device's active area. Inescapable in this layout, the source metal layers will overlap the gate track. The air bridge and insulation layer are utilised to isolate the gate and source metal layers.

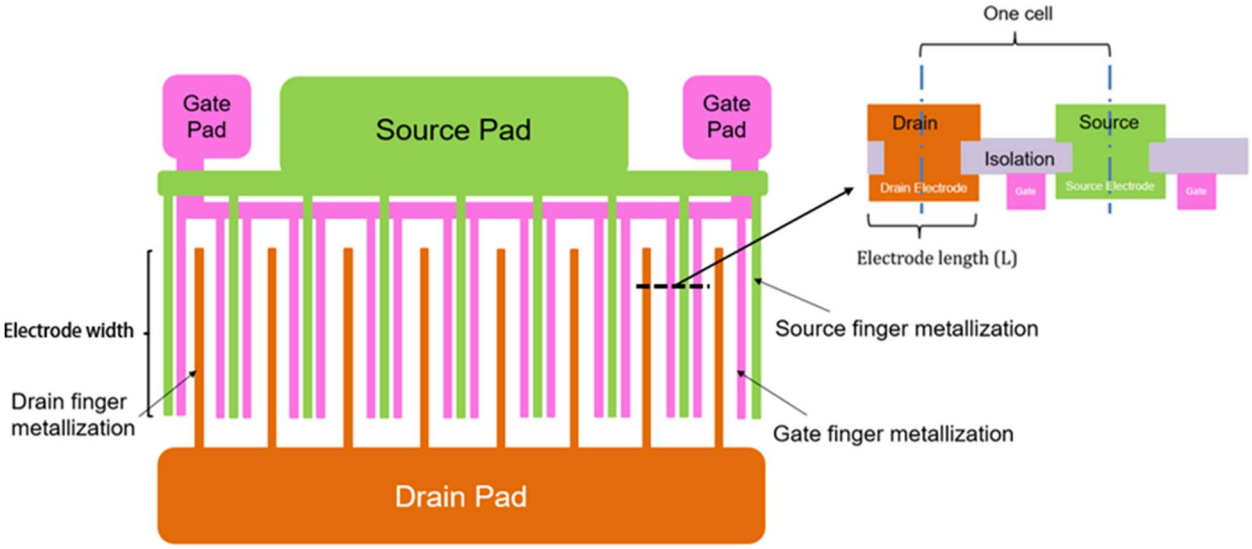


Figure 3.3.2: Top view of PSJ Multi-finger Layout

3.3.4 Current capability

For a multi-finger layout, it is essential to ensure that the fingers have sufficient current processing capacity and evenly distribute the current in each finger. Reliability of metallisation is the necessary factor. Material properties of metal, geometry, current level, metal deposition technique, and operating temperature are severe aspects that cause the Electromigration phenomenon.

Electromigration is a persistent issue for device fabrication. It is a cause for degradation in the power semiconductor device, leading to an increase in on-state resistance, connection loss and even device failure. Compared with other materials, Gold (Au) interconnects are commonly used which have a much better median time to failure and superior conductivity. Electromigration of Au interconnects active under the conditions of the current density of 2.0 MA/ cm^2 and ambient temperature of 325 ^oC ~ 375^oC[106][107][108]. Regarding functionality and reliability in the operating range, the current densities close to 250 kA/ cm^2 are considered safe.

The primary challenge for multi-finger layout design is determining the fingers' size (width, length and thickness) and the cell number to achieve the desired current rating. Assume the overall current distribution in the Device is uniform and the current density (normalised to Gate Length) achievable at V_{ds}=1V is estimated.

$$\text{The effective gate length (mm)} = \frac{Current\ rating(A)}{normalised\ current\ density\ (mA/mm)} \text{ -------(3.1)}$$

The finger length has been set in designs, so

$$\text{The total cells}=\frac{The\ effective\ gate\ Length\ (mm)}{Finger\ length(mm)} \text{ ------(3.2)}$$

These cells effectively operate in parallel.

Due to 1 Gate electrode for one cell and each Drain/Source electrode shared by two cells, The figure number of Source and Drain can be calculated by:

$$\text{The Gate finger number= cell number ------(3.3)}$$

$$\text{The Drain/Source number} = \frac{Cell\ number}{2} \text{------(3.4)}$$

Considering the Device's overall size and the long finger is easy to break midway, the effective gate length is set as 750µm,1000µm and 2800µm for different current ratings. The current density in each finger unit cell (normalised to gate width) is estimated at 30mA/mm.

The area size of the pad design is based on the package approach and wire-bonding facility. Typically, in the design of wire bonding for power semiconductor devices, the suggested pad area generally is 2-3 times for wedge bonding and 3-5 times for ball bonding. Therefore, the pad area of wire-bonded devices requires a minimum side length of 250μm.

3.3.5 Mask design for large-area devices

For large-area devices, it designs Bi PSJ SG HFETs and Bi PSJ OG HFETs with the other L_{PSJ} (15 μm, 20μm and 40μm) at current ratings (1A,2A, 5A and 10A), as shown in Table 3.8. Except for Bi PSJ HFETs, large-area PSJ HFETs and PSJ Diode are also designed in this project. Different finger length is designed for large-area devices under the consideration of the chip size and the finger quality. The mask layouts for some of the scaled-up devices have been shown in Figure 3.3.3.

Table 3.8: Mask information for large-area devices

Device	Lpsj (μm)	Current Rating (A)	Finger length (μm)
Bi PSJ SG HFETs	15	1	750
		5	2800
		10	2800
	20	1	750
	40	2	1000
Bi PSJ OG HFETs	15	1	750
		10	2800
	20	1	750
	40	2	1000
PSJ-FET	15	1	750
	40	1	750
		2	750
PSJ-Diode	15	1	750
	40	1	750
		2	750

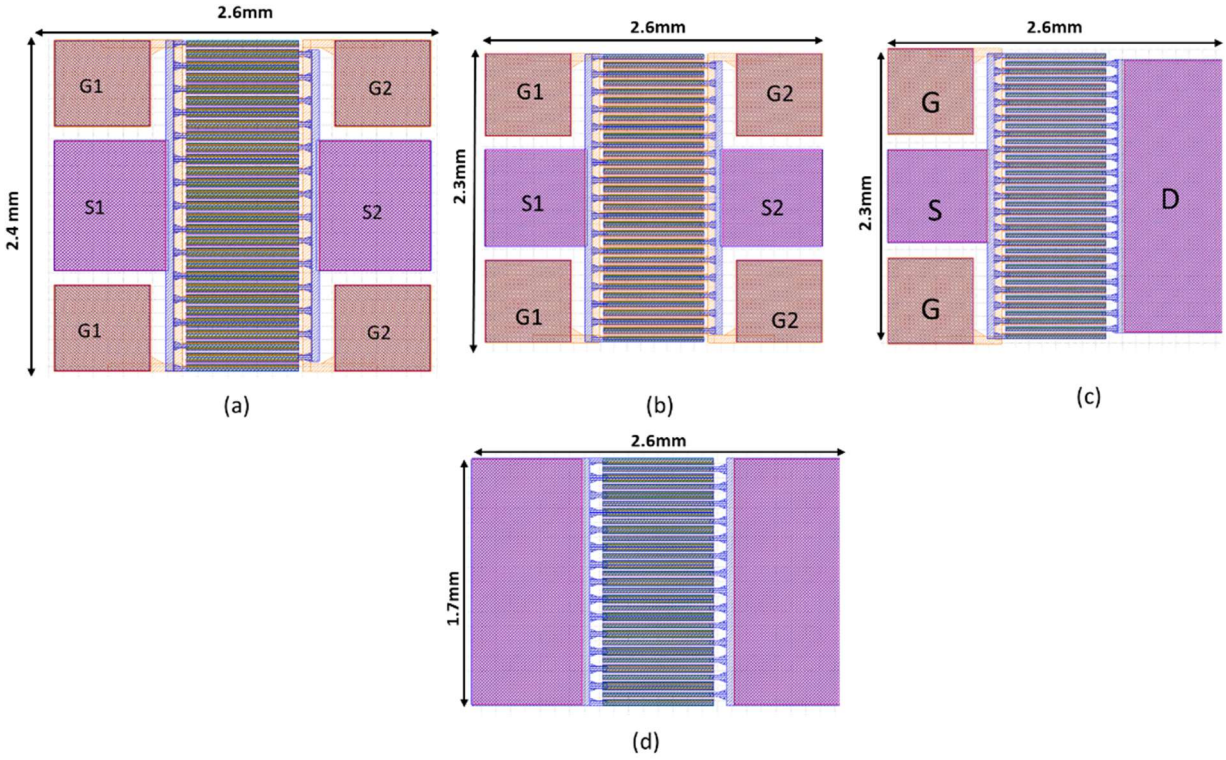


Figure 3.3.3: Mask layouts (a) 1A rated Bi PSJ SG HFET (b) 1A rated Bi PSJ OG HFET (c) 1A rated PSJ HFET (d) 1A rated PSJ Diode.

3.3.6 Mask design for test structures

Device test structures included Schottky Barrier diode, PSJ Diodes, PSJ HFETs and PSJ Bidirectional HFETs with SG and OG. Figure 3.3.4 is the top view of the test structure for Bi PSJ HFETs with (a)Schottky Gate and (b) Ohmic Gate. Device test structures also include PSJ GaN-based HFETs and Diodes. In addition, some unique structures are designed for testing leakage currents, mobility, contact resistance and more.

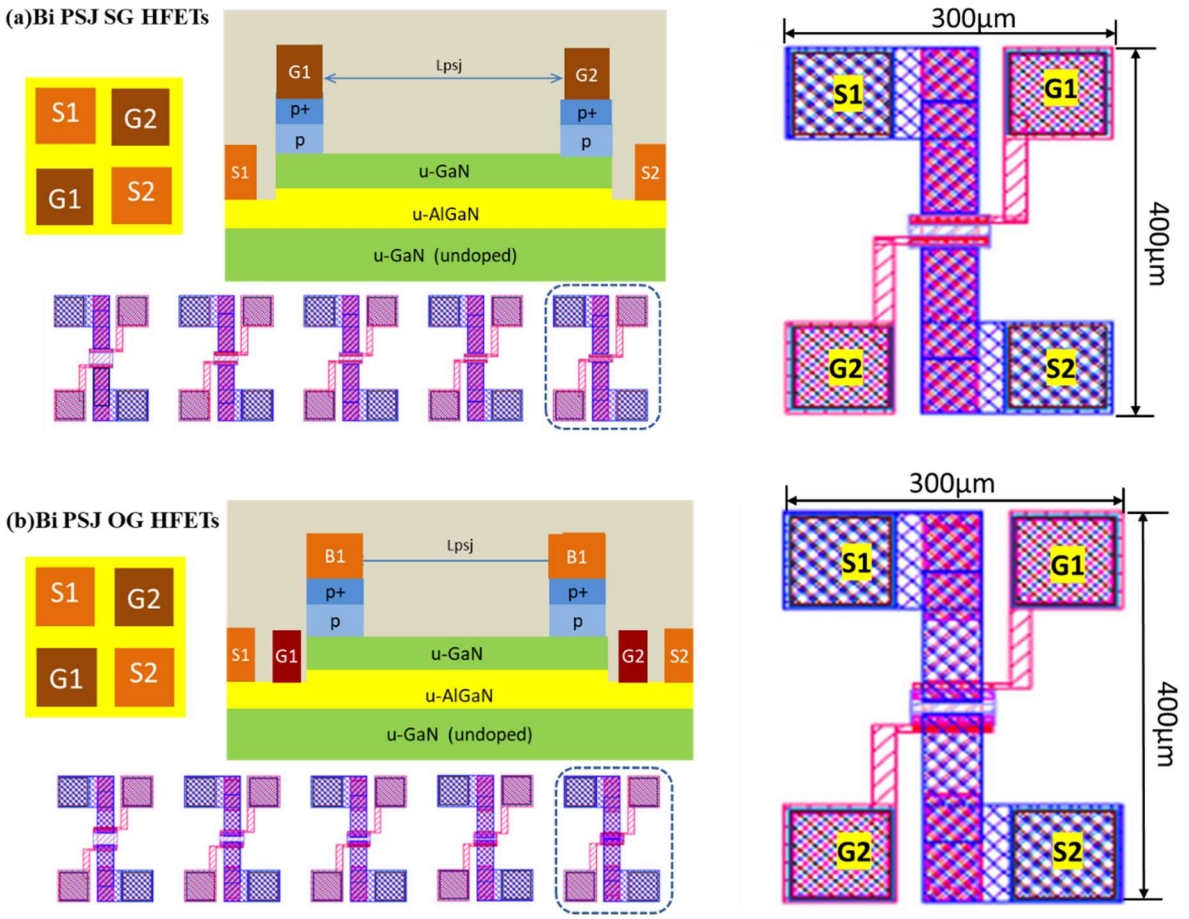


Figure 3.3.4: The top view of the test structure for Bi PSJ HFETs with (a)Schottky Gate and (b) Ohmic Gate.

We also design different gate structures for Bi PSJ OG HFETs at the Mask level to research the influence of the gate structure on the leakage. Figure 3.3.5 shows the schematic of 4 gate structures of Bi PSJ OG HFETs. Change the alignment of the etched layers (ISO, ME and PE layers) while maintaining a micron gap between layers for alignment. The gate structure affects the control of the 2DHG for charge compensation and thus influences the leakage at high voltage. There is no relative experiment data shows which designs are better for PSJ HFETs. For large-area devices, designed gate structures are chosen Design 'PSJ-G1', i.e. PC layer inside the ISO layer while ME &PE extend the ISO layer. The main difference between (a)PSJ-G1 and (d) PSJ-G4 is where the red circle points. PSJ-G1 has the longer M1 layer used for Metalization gate electrodes.

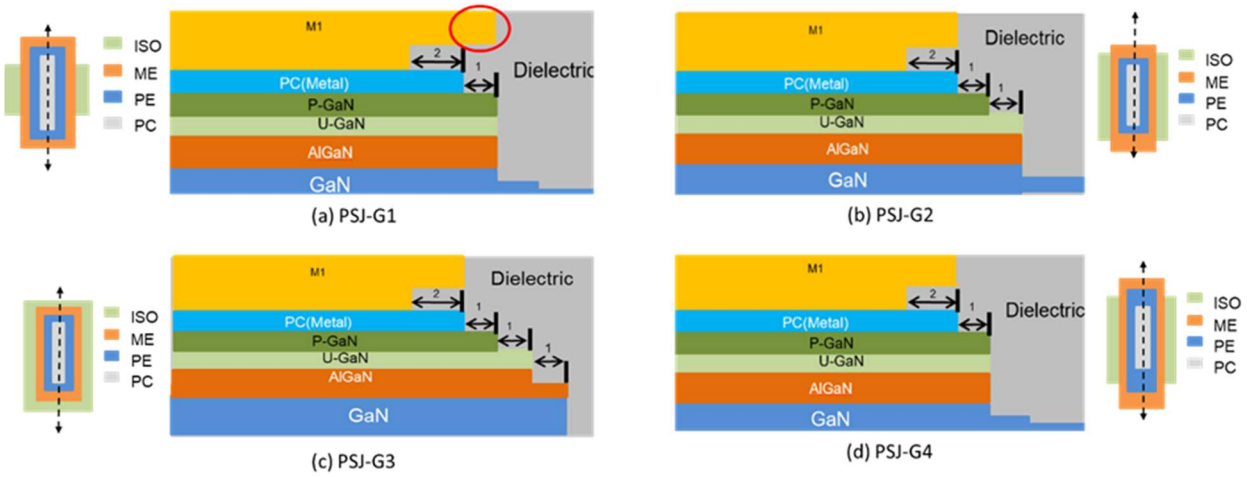


Figure 3.3.5：The schematic of 4 gate structures of Bi PSJ OG HFETs

Some additional process test structures are shown in Figure 3.3.6, designed for evaluating the mobility, leakage, and contact resistance. The final mask layouts include two parts for the 6’ wafer, shown in Figure 3.3.7.

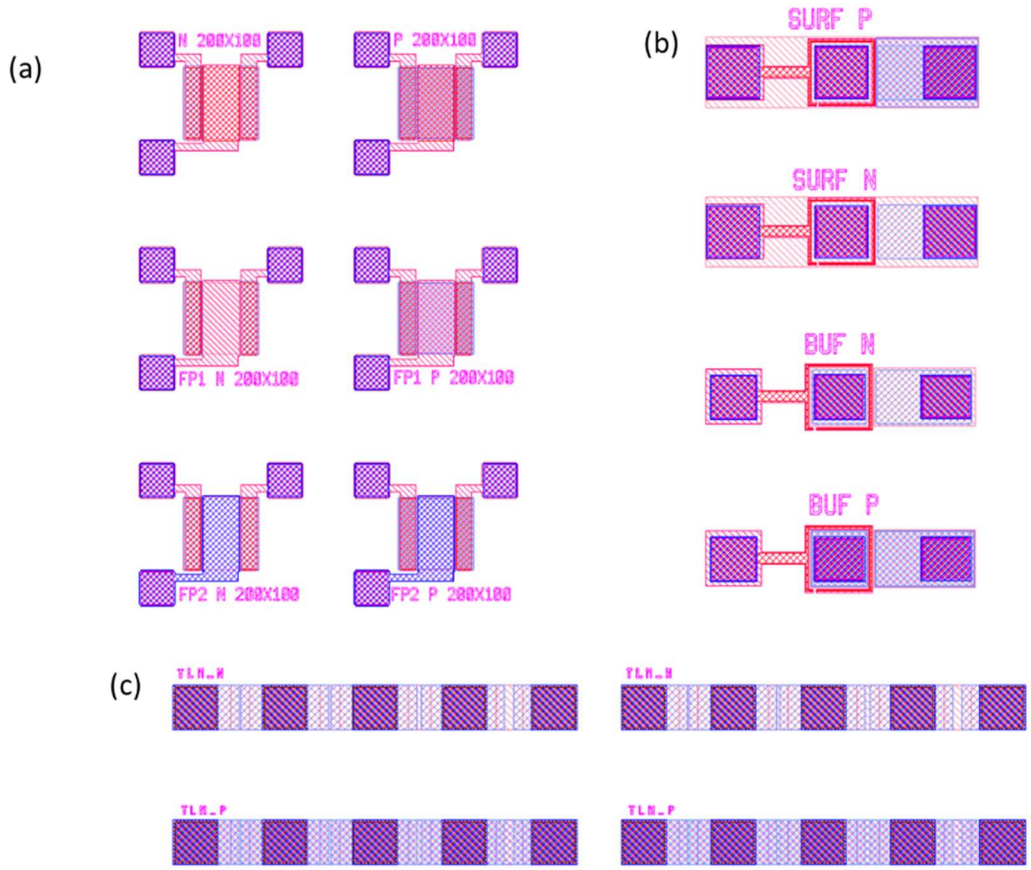


Figure 3.3.6: Additional Process Test Structures for evaluating (a) mobility and capacitance (b) surface/buffer leakage (c) contact resistance

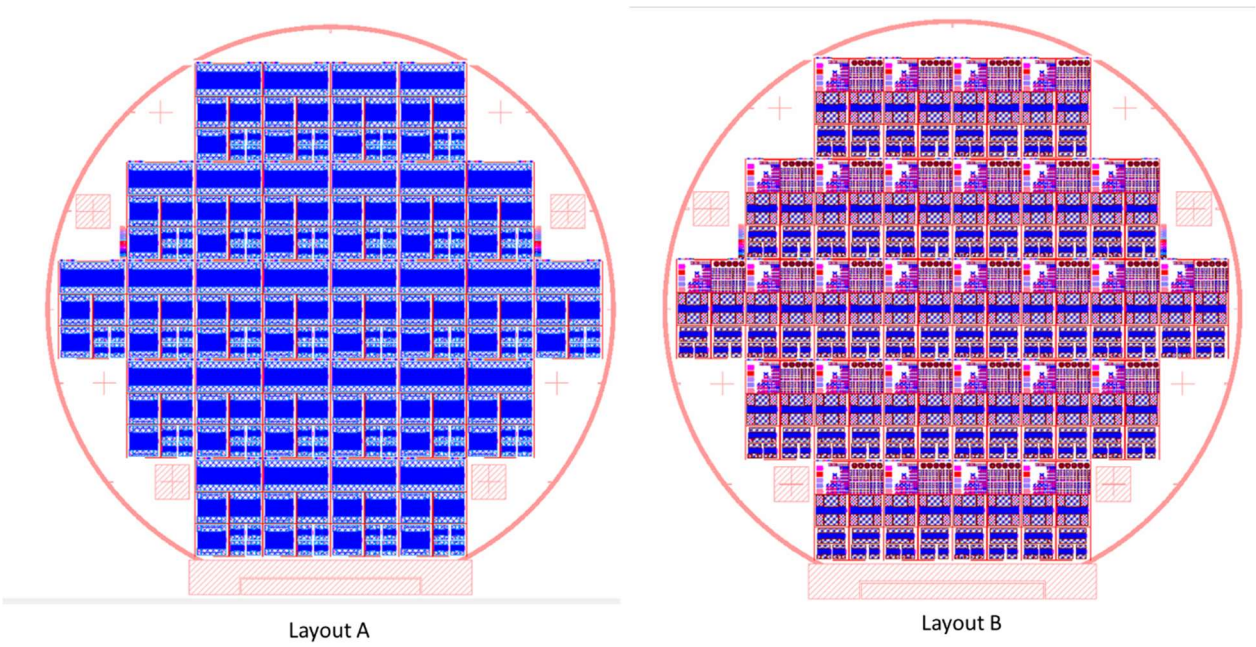


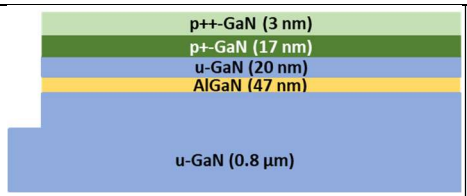
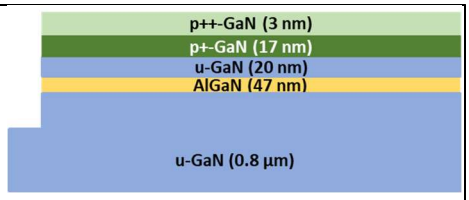
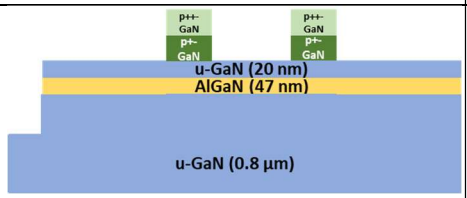
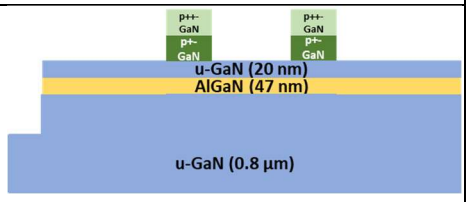
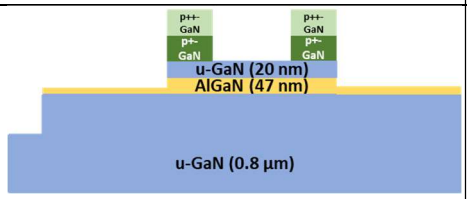
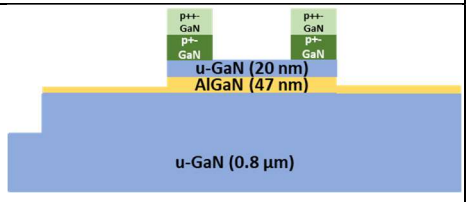
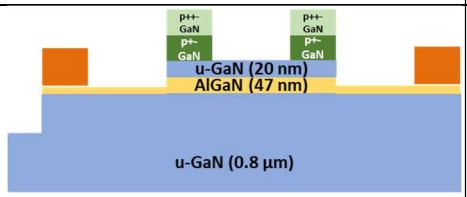
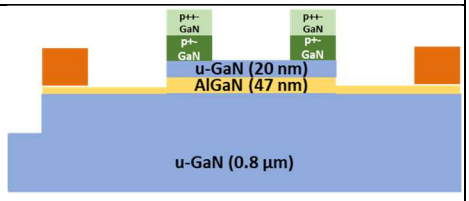
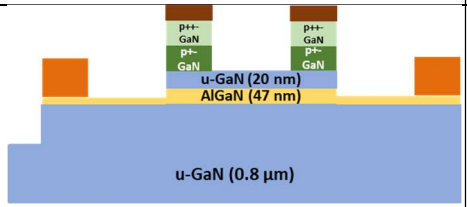
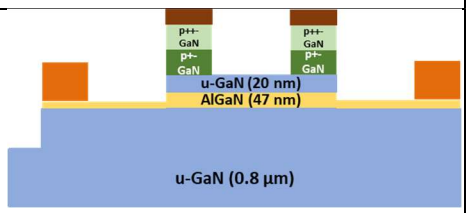
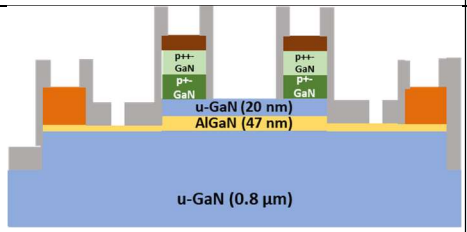
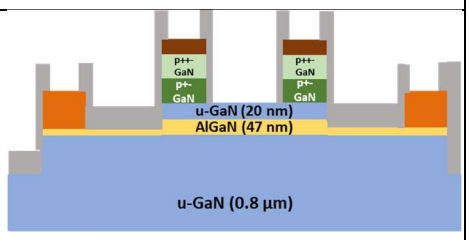
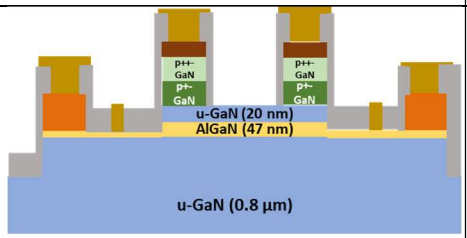
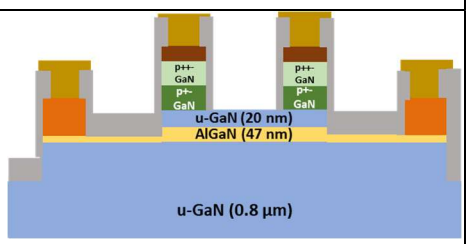
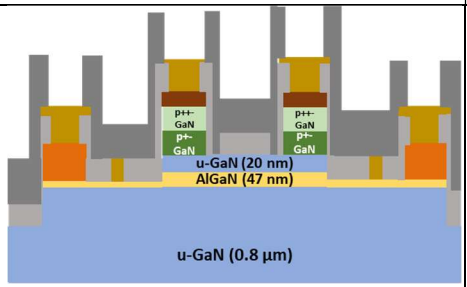
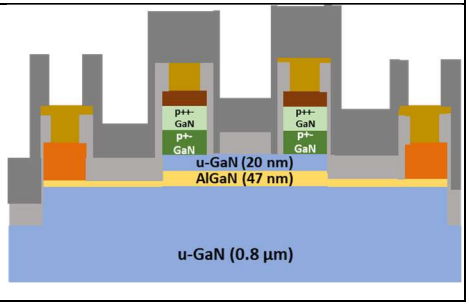
Figure 3.3.7: Final mask layouts

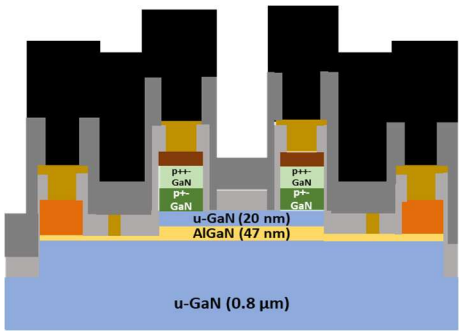
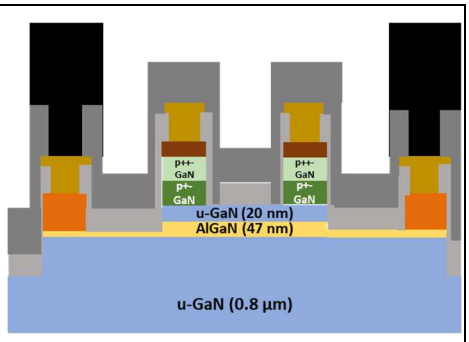
3.3.7 The overall process flow

The Bidirectional PSJ HFET with Schottky gate as the example, Table 3.9 shows the overall process flow.

Table 3.9: The Process flow of BI PSJ HEMT with Schottky/Ohmic Gate

No.	Stage	Mask	BI PSJ HEMT with Schottky Gate	BI PSJ HEMT with Ohmic Gate
0	EPI		p++-GaN (3 nm Mg doped~2e20 cm^{-3}) p+-GaN (17 nm Mg doped~5e19 cm^{-3}) u-GaN (undoped, 20 nm) u-AlGaN (undoped, 47 nm, 23% Al) u-GaN (undoped, 0.8 µm) Nucleation Layer Sapphire (900 µm)	p++-GaN (3 nm Mg doped~2e20 cm^{-3}) p+-GaN (17 nm Mg doped~5e19 cm^{-3}) u-GaN (undoped, 20 nm) u-AlGaN (undoped, 47 nm, 23% Al) u-GaN (undoped, 0.8 µm) Nucleation Layer Sapphire (900 µm)
1	Alignment Mark Etching	AM	p++-GaN (3 nm) p+-GaN (17 nm) u-GaN (20 nm) AlGaN (47 nm) u-GaN (0.8 µm)	p++-GaN (3 nm) p+-GaN (17 nm) u-GaN (20 nm) AlGaN (47 nm) u-GaN (0.8 µm)

2	Device Isolation	ISO		
3	P-GaN Etching	PE		
4	Mesa etch	ME		
5	Drain/Source Contact	NC		
6	Base/Gate Contact	PC		
7	Isolation and Via	V1		
8	Metal 1	M1		
9	Isolation and Via2	V2		

10	Metal 2	M2 & M2P		

The final step is depositing a final insulator layer and open a window for the pad. The schematic of the final device cross-section and layout (serpentine gate) are presented in Figure 3.3.8.

Figure 3.3.8: Schematic of the cross-section for (a)BI PSJ SG HFET and (b)BI PSJ OG HEMT

3.4 Summary

The structure of Compact Monolithic Bidirectional PSJ HFETs with Schottky Gate and Ohmic Gate was introduced initially in this chapter, as well as their operating mechanism. Results from numerical simulations were reported for Bi PSJ HFETs with various PSJ lengths operating under various bias conditions. It should be noted that the purpose of this chapter's simulation study is to gain a physical understanding of Bidirectional PSJ technology, as opposed to precisely replicating experimental results. Following that, the approach to device design rules and mask design for test structure and large-area devices are presented in detail. Chapter 4 presents performance measurement findings and an analysis of the functions that the manufactured devices behaved.

Chapter 4: Electrical Characterisation of Fabricated Bidirectional PSJ HFETs

This chapter details the performance and electrical characterisation results of fabricated test structures and various large-area bidirectional devices. The purpose of this project is to verify that Bi PSJ HFETs can achieve bidirectional switching through the control gate. Detailed analysis of the on-state behaviour of the fabricated Ohmic Gate (OG) and Schottky Gate (SG) PSJ HFETs is presented. We also built the analytical model of the on-state resistance of Bi PSJ HFETs to calculate and analyse its components. Future work requires optimal epitaxial structures to demonstrate high-voltage breakdown devices.

4.1 Fabricated Wafers and Devices

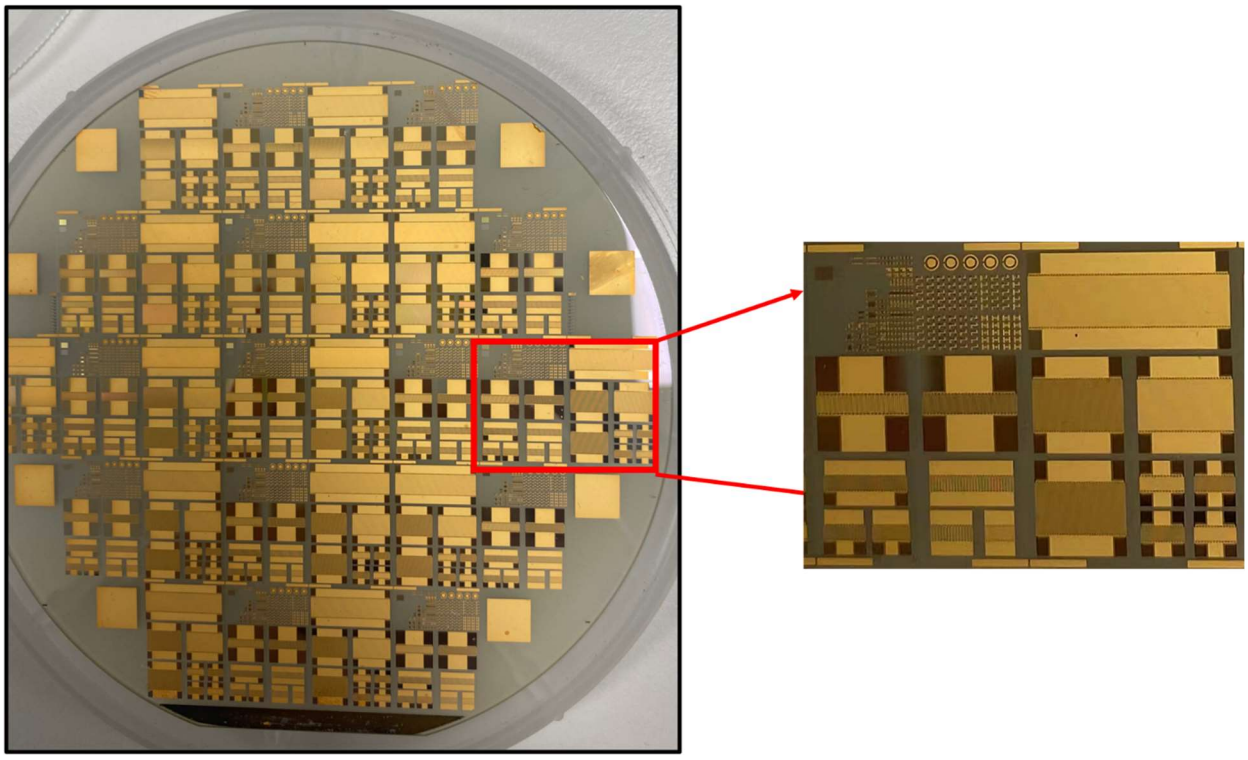


Figure 4.1.1: Pictures of 6" processed GaN-on-Sapphire wafer

It is the first time to design and fabricate PSJ large-area devices as well as the test group on the 6" processed GaN-on-Sapphire wafer, as shown in Figure 4.1.1. It includes Test Element Group, large-area unidirectional PSJ HFETs, large-area PSJ Merged Schottky Barrier Diode group and large-area

Bidirectional devices. Black pads for devices shown in Figure 4.1.2 are gate pads for unidierectional PSJ HFETs and Bi PSJ HFETs due to passivation.

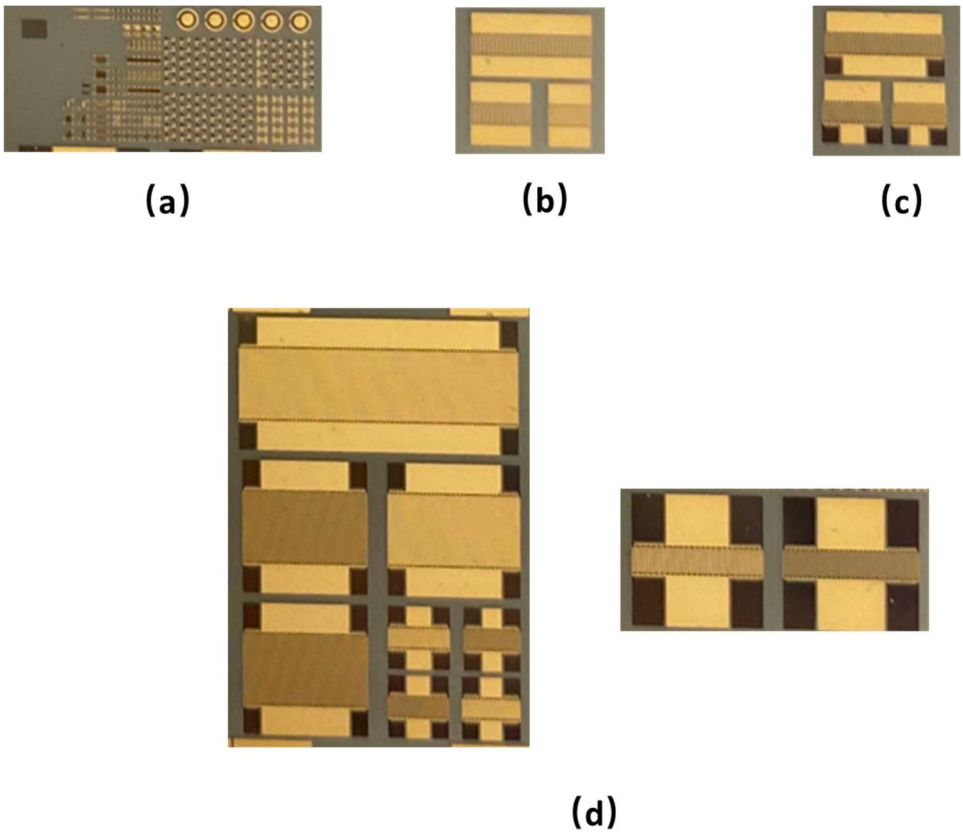


Figure 4.1.2: Top view of fabricated (a)Test Element Group, (b)large-area PSJ Merged Schottky Barrier Diode group, (c) large-area unidirection PSJ HFETs and large-area Bi PSJ HFETs.

4.2 Tests on GaN wafer

Compact Bi PSJ HFETs and PSJ devices with various current carrying capabilities are fabricated on the 6" GaN PSJ wafer, which epitaxy (Epi) is shown in Figure 4.2.1. It consists of an 0.8μm-thick undoped GaN buffer layer (u-GaN), a 47nm-thick un-doped AlGaN layer with an Al composition of 23%, and a 20nm-thick un-doped GaN layer. A 17nm-thick p-type doped GaN cap (P-GaN) layer with 5×10^{19} cm^{-3} and a 3nm-thick P-GaN layer with 2×10^{20} cm^{-3} have been grown on u-GaN, which enable an ohmic contact to 2DHG. Generally, the GaN buffer layer of GaN HEMTs is doped by acceptors like Carbon (C), which can help prevent leakage through the buffer region by lifting the GaN conduction band upwards by better confining the 2DEG channel and preventing the 2DEG spillover effect in the buffer. However, with doping, the GaN buffer defects increase. As discussed in Section 2.2.4, buffer traps trap electrons from the channel and thus leads to the current collapse phenomenon. It has been proven that the degradation of high-voltage AlGaN/GaN HEMTs is

closely related to the doping concentration and distribution in GaN buffer. In this study, in order to only observe the polarisation superfunction-related effects on 2DEG/2DHG charge control conventional background, Carbon acceptor doping is not used in the GaN buffer region.

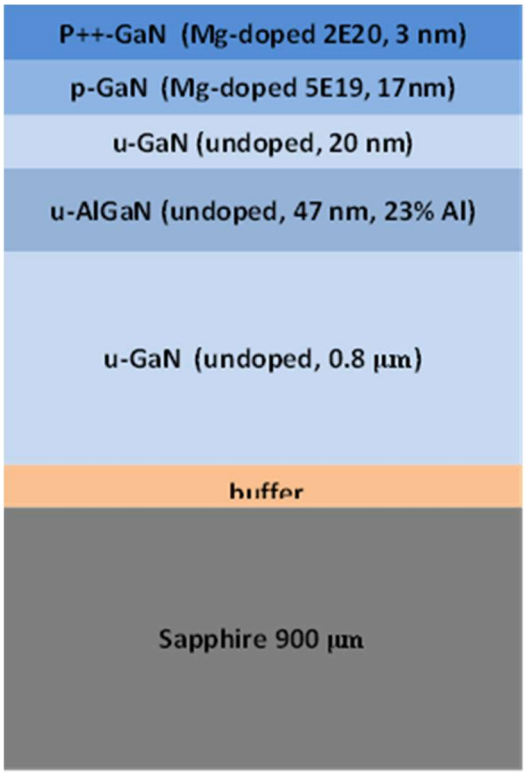


Figure 4.2.1: Specification of Sapphire substrate GaN PSJ wafer

4.2.1 Buffer and Surface leakage

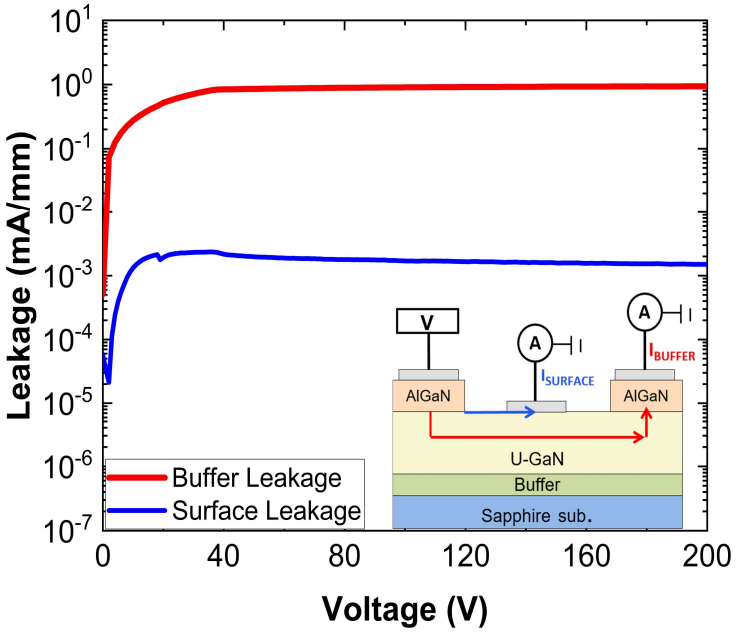


Figure 4.2.2: Measured buffer and surface leakage

Without C-doping in GaN buffer layer, the unintentionally doped buffer layer ends up slightly n-type and causes buffer leakage issues. Figure 4.2.2 shows the buffer leakage (Red Curve) and the surface leakage (Blue Curve) of the inset structure in Figure 4.2.2. The buffer leakage increase to 1mA/mm at 40V and then keeps constant. This buffer leakage is the dominant factor in the leakage current in the off-state for Bi PSJ HFETs. The surface leakage, associated with poor passivation, surface states and sidewall damage, is reasonably low, suggesting good process control. Future work is needed with the optimum epitaxial structure for demonstrating high-voltage breakdown devices.

Figure 4.2.3 shows the leakage between two electrodes on the p-GaN layer is small, about 19nA/mm at 100V. For Bi PSJ SG (OG) HFETs, 2DHG forms a channel between two bases (gates), which causes leakage during the off-state. Due to the low mobility of 2DHG, the measured current between electrodes is much low. In addition, the 2DHG will be depleted in the off-state by 2DEG.

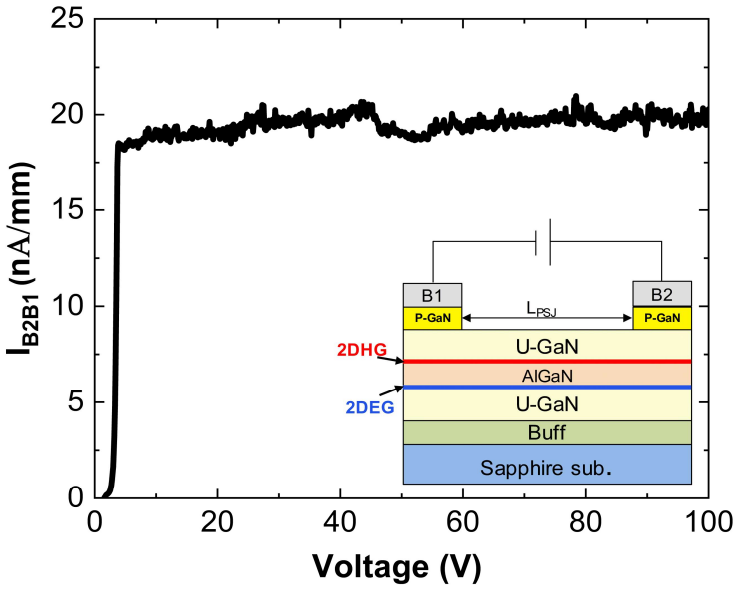


Figure 4.2.3: The leakage between two electrodes on P-GaN layers

4.2.2 Evaluation of Effective Field-Effect Mobility of 2DEG

In the mask design, specific test structures are designed to test CV and evaluate mobility. Figure 4.2.4 presents the schematic of N-type FAT FET used to evaluate 2DEG mobility. The source and the Drain electrode are in ohmic contact with 2DEG, while gate is in Schottky Contact.

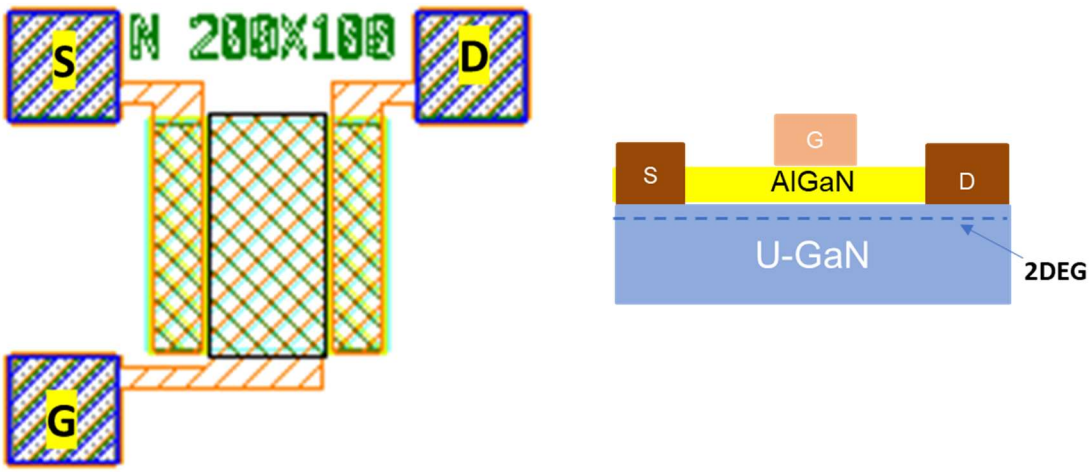


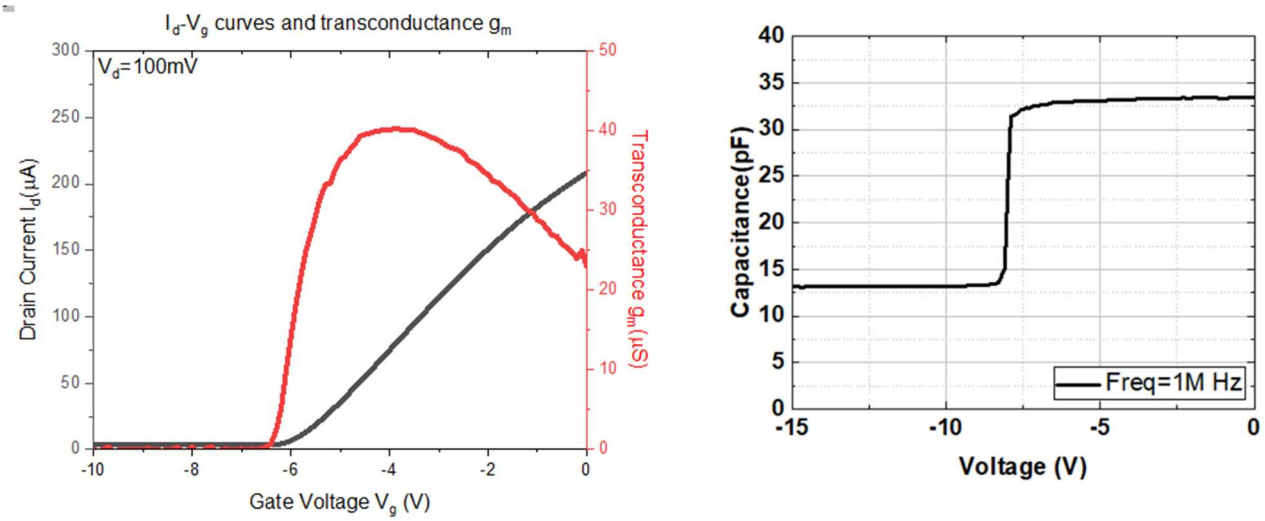
Figure 4.2.4: Schematic of N-type FAT FET.

The effective field-effect mobility is defined by Equation (4.1)[31]:

$$\text{Field-effect mobility } \mu_{FE}=\frac{L\cdot g_m}{W\cdot C_i\cdot V_{DS}} \text{ ------(4.1)}$$

Where L is the channel length, W is the channel width, g_m is the transconductor and C_i is the capacitance between the channel and gate per unit area.

The transconductance g_m is calculated from the I_d-V_g curve when V_{ds}=0.1V, as shown in the Figure 4.2.5(a). The low V_{ds} bias ensures the carrier is attracted by the electrical field. The Capacitance C_i measured is 12.6 pF at 1M Hz frequency by applying a negative voltage sweeping on the Schottky Gate, as shown in Figure 4.2.5(b). Around the threshold voltage(-6V), electrons in 2DEG are depleted dramatically. According to the equation of Capacitance (C=QV), changes in charge density lead to the accumulation in CV curve. Therefore, the effective mobility of DEG can be calculated, which is plotted in Figure 4.2.6. At Vg=0V, the 2DEG mobility is around 700V, which will be used to analyse the on-state behaviour of Bi PSJ HFETs.



(a) (b)

Figure 4.2.5: The measured gm and Ci of n-type FATFET

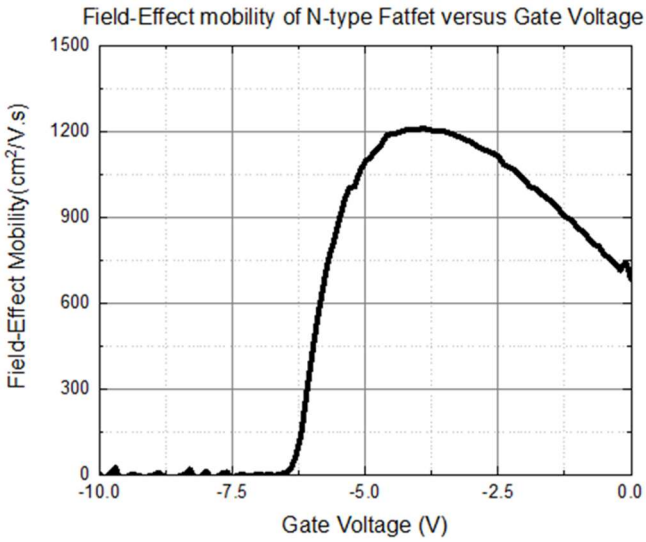


Figure 4.2.6: The calculated effective Field-Effect Mobility of 2DEG.

4.3 Bidirectional PSJ HFETs with Schottky Gate

Fabricated Bi PSJ SG HFETs on Sapphire substrate have four pads of Gate1, Gate2, Source1 and Source2. The metallization interconnects connected two bases to the adjacent source electrode in the mask level. Figure 4.3.1 shows the cross-section schematic of test structure of Bi PSJ SG HFETs.

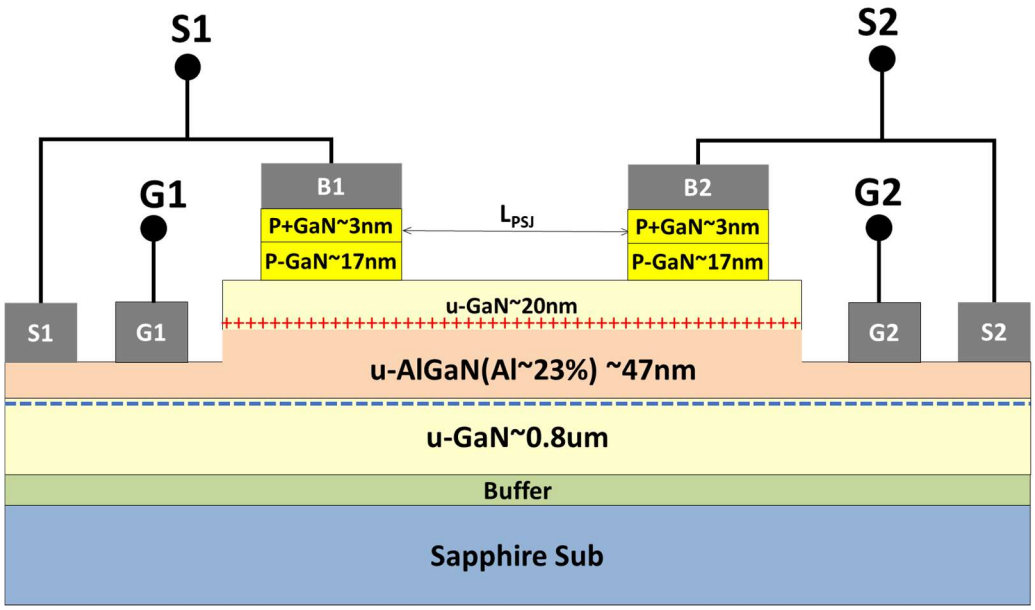


Figure 4.3.1: Cross-section schematic of fabricated Bi PSJ SG HFETs

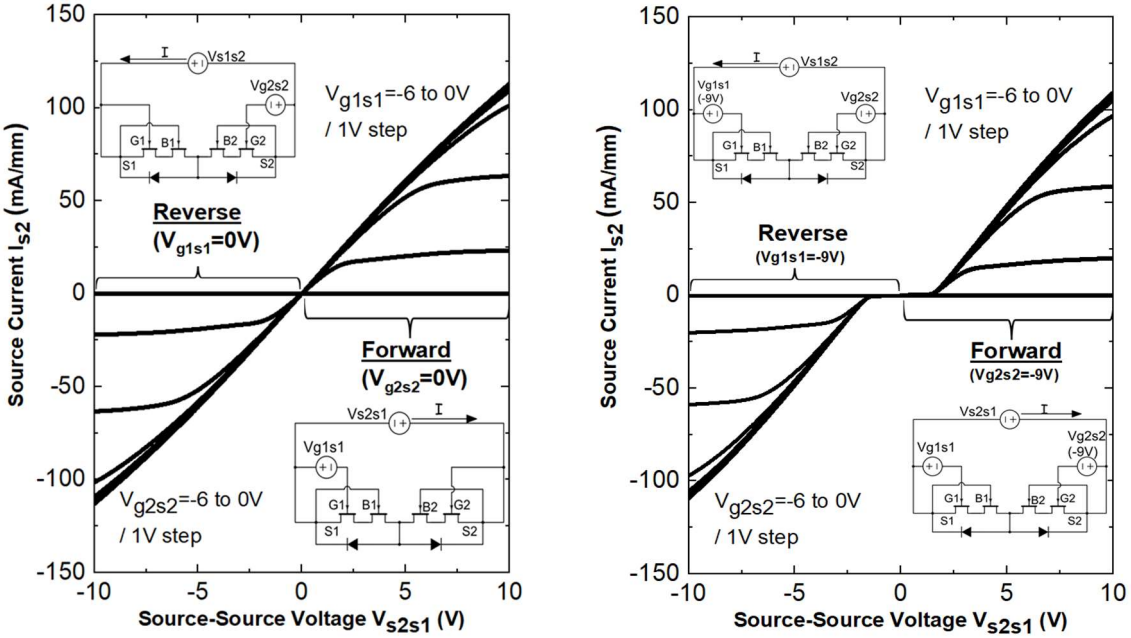


Figure 4.3.2: Measured Is-Vs1s2 characteristics of fabricated Bi PSJ SG HFETs 40μm-L_{PSJ} in both directions with various bias conditions

4.3.1 Electrical characterisation results

I-V Characteristics

Figure 4.3.2 shows I_{s2}-V_{s2s1} characteristics of the fabricated Bi PSJ SG HFET with 40µm-L_{PSJ} in both directions with various bias conditions at room temperature. The bias voltage settings are consistent with the simulation described in Chapter 4, as shown in the inset figures. (Vs2s1>0V), In Figure 4.3.2(a), results are obtained by G2 is connected to adjacent S2 (V_{g2s2}=0V) in the forward region while G1 is connected to adjacent S1 in the 'reverse' bais. The forward current I_{s2s1} flows from S2 to S1 through the 2DEG and is controlled by Gate1 and Gate2, respectively. As V_{g1s1} reduces to less than -6 V, the device enters off-state. Figure 4.3.2(b) shows the forward simulated Is2-Vs2s1 characteristics with a negative gate2 voltage V_{g2s2} of -9V (V_{g2s2}=-9V). The Bi PSJ SG HFET can operate as a diode in both directions, similar to the simulation results. Calculated on-state voltages at I_{s2}=10mA/mm are 0.8 V (V_{g2s2} = 0 V) and 2.2 V (V_{g2s2} = -9 V) in the 'forward Region' at room temperature.

Changing the V_{g2s2} from -7V to -15V, the Current I_{s2s1} can be measured at V_{g1s1}=0V in the forward region. The on-state voltage keeps constant and is around 2.2V at 10mA/mm, regardless of V_{g2s2}, as shown in Figure 4.3.3, because the base is connected with the nearby source. Therefore, the depletion region under the gate can not change.

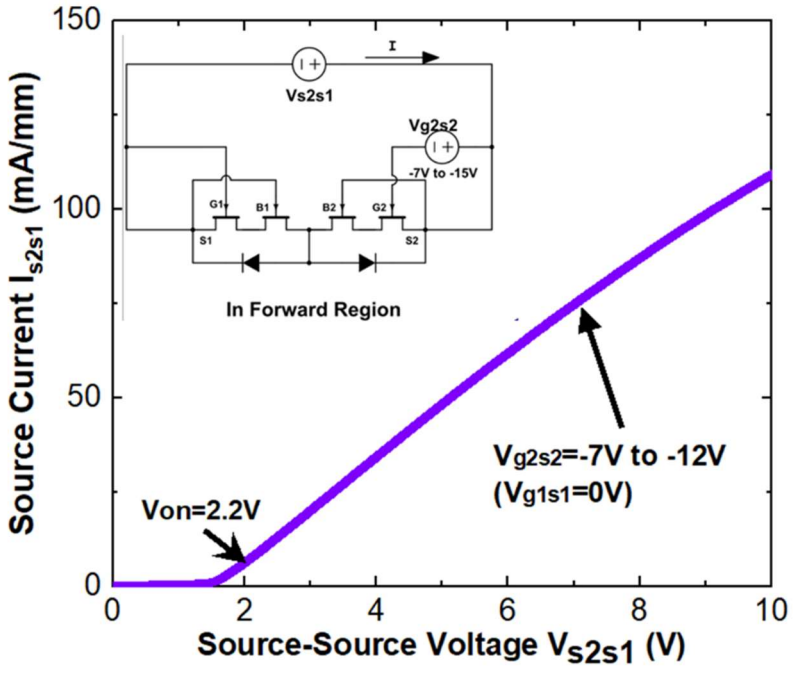


Figure 4.3.3: The Is2-Vs2s1 characteristics of Bi PSJ SG HFET in the 'Forward' Region by changing Vg2s2 from -7V to -12V.

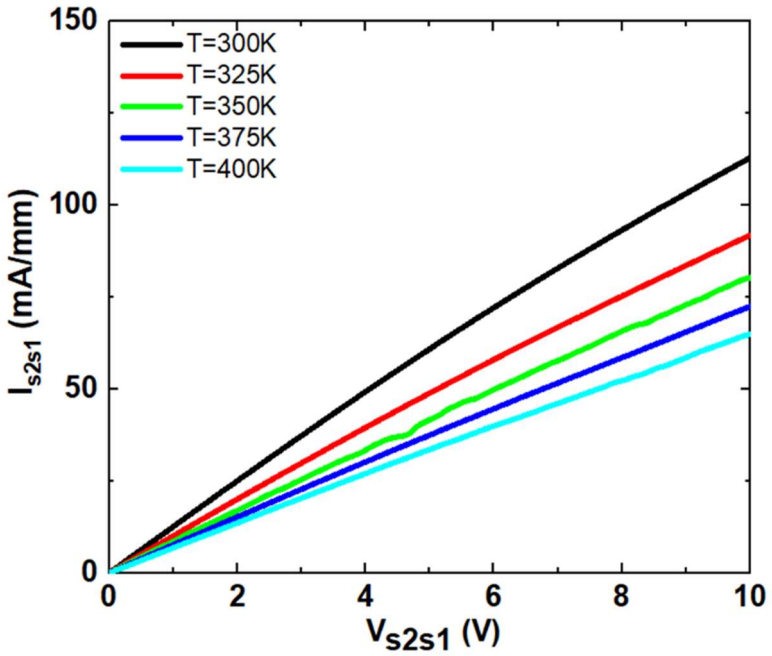


Figure 4.3.4: Measured temperature-dependent forward Is2s1-Vs2s1 characteristics of Bi PSJ SG HFET with 40µm-L_{PSJ} at Vg2s2=0, Vg1s1=0V.

The static 'forward' I_{s2} - V_{s2s1} of the Bi PSJ SG HFET with 40µm-L_{PSJ} is measured at high temperatures at V_{g2s2}=0, V_{g1s1}=0V and is shown in Figure 4.3.4. The current I_{s2s1} drops as the temperature increases. The decline in current can be mostly a result of temperature fluctuations that reduce 2DEG mobility and raise phonon-dependent scattering.

The average variation in Ron.A of 8 samples of BI PSJ SG HFETs with 40µm-L_{PSJ} as a function of case temperatures are presented in Figure 4.3.5. The 'forward' specific on-state resistance (Ron.A) is calculated at Vs2s1 of 1V when V_{g2s2}=0V and V_{g1s1}=0V. When the temperature increases from 300K to 400K, Ron.A of Bi PSJ SG HFETs is found to increase from 65.24mΩ.cm^2 to 113.82mΩ.cm^2 in a linear relation since the scattering is higher at the higher temperature. The maximum discrepancy is within 5.31% of its mean value at 350K.

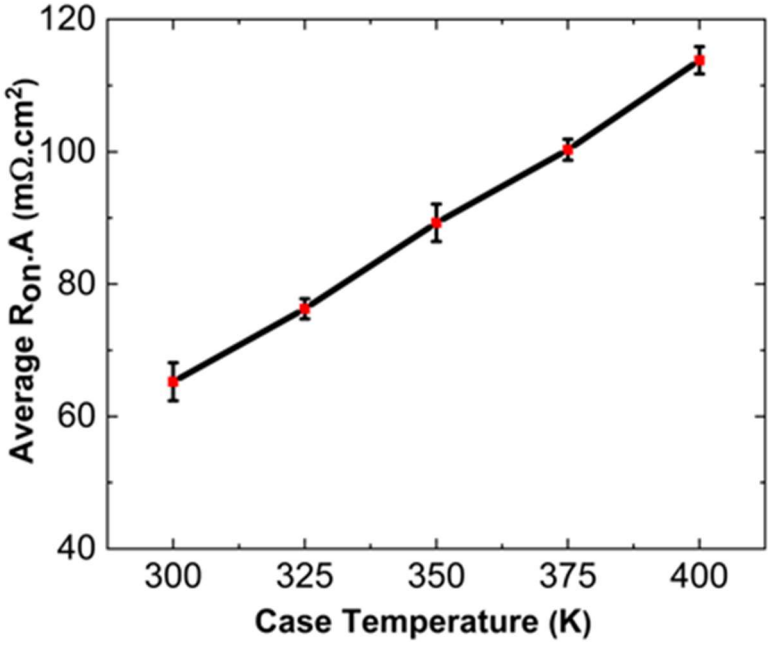


Figure 4.3.5: The average Ron. A of 8 fabricated Bi PSJ SG HFETs with 40um-LPSJ at a temperature from 300K to 400 K

Figure 4.3.6(a)-(b) shows the forward I_{s2}-V_{s2s1} characteristics with various L_{PSJ} performing as (a) HFETs and (b) diodes. With the increase of L_{PSJ}, the on-state R increases while Von keeps constant, which corresponds with the simulation results. Simulated reverse characteristics of I_{s1} -V_{s1s2} with V_{s2s1} < 0V are identical to that of forward because Bi PSJ SG HFETs have a symmetrical structure. The specific on-state resistance with various L_{PSJ} at room temperature can be calculated at 1mA/mm when V_{g1s1}=0V.

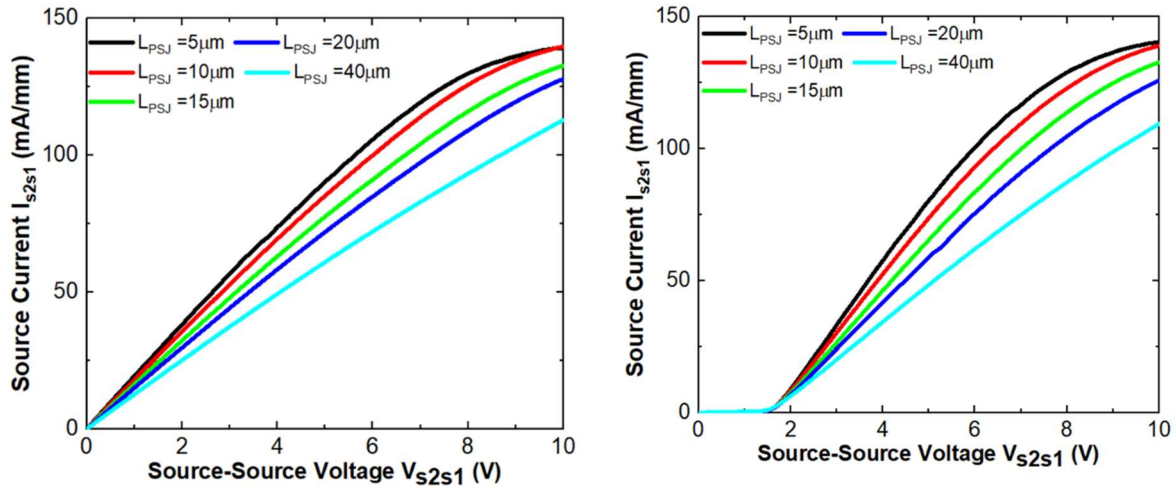


Figure 4.3.6: The measured I_{s2}-V_{s2s1} characteristics with various L_{PSJ} in the forward region at (a) Vg2s2=0V, Vg1s1=0V and (b)Vg2s2=-9V, vg1s1=0V.

The change in Ron.A vs L_{PSJ} for 8 samples with the error bars indicating standard deviations are presented in this Figure 4.3.7. The maximum discrepancy is within 7.37% of its mean value when L_{PSJ}=40µm. Analytical Modeling and detailed analysis on Ron.A of Bi PSJ HFETs will be introduced in next Section 4.3.2. The linear increase in the Ron.A as a function of the temperature of Bi PSJ HFETs as well as the on-state resistance versus L_{PSJ} show that the device can be scaled easily scaled in both voltage and currents.

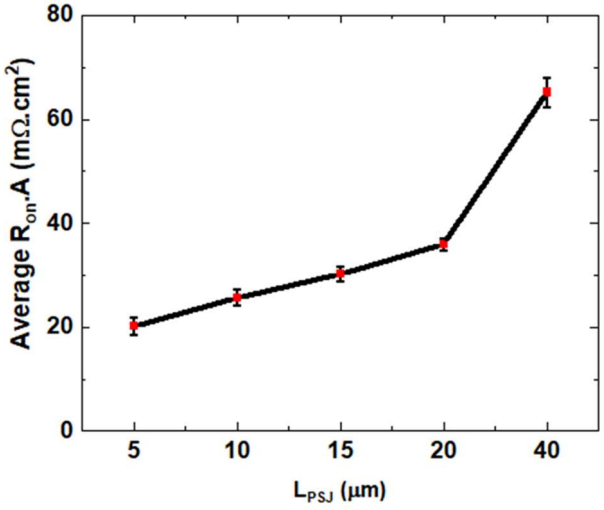


Figure 4.3.7: The average Ron. A of 8 fabricated Bi PSJ SG HFETs with different L_{PSJ} at room temperature.

Input characteristics

The forward input characteristic of Bi PSJ HFETs with Schottky gate is plotted in Figure 4.3.8 with different PSJ lengths (15µm,20µm, and 40µm). The threshold voltage of SG PSJ HFETs is around -5.7V.

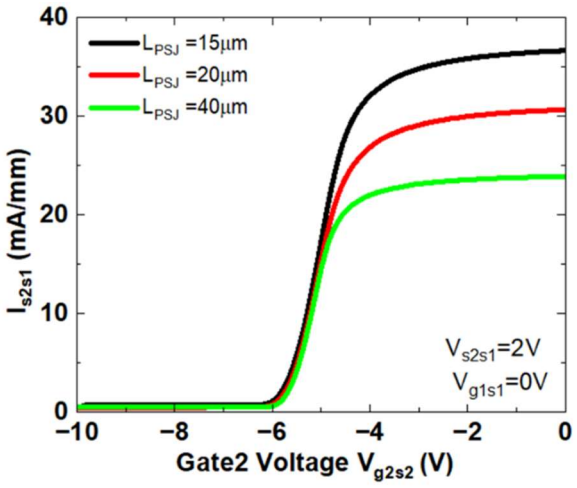


Figure 4.3.8: The forward transfer characteristic of Bi PSJ HFETs with Schottky gate.

Off-state Leakage

A measured slightly high leakage current of around 6mA/mm at 200V under forward blocking conditions for Bi PSJ SG HFETs at 200V with various L_{PSJ} was plotted in Figure 4.3.9. Measured reverse characteristics of I_{s1} -V_{s1s2} with V_{s2s1} < 0V are identical with that of forward. Equipment compliance limits further 'forward' blocking voltage measurement. As mentioned in Section 4.1.1, the leakage from S1 to S2 through the undoped GaN buffer layer is the main determining factor. Figure 4.3.10 shows the leakage I_{s2}, I_{s1} and I_{g1} of Bi PSJ SG HFET with 40µm-L_{PSJ}.

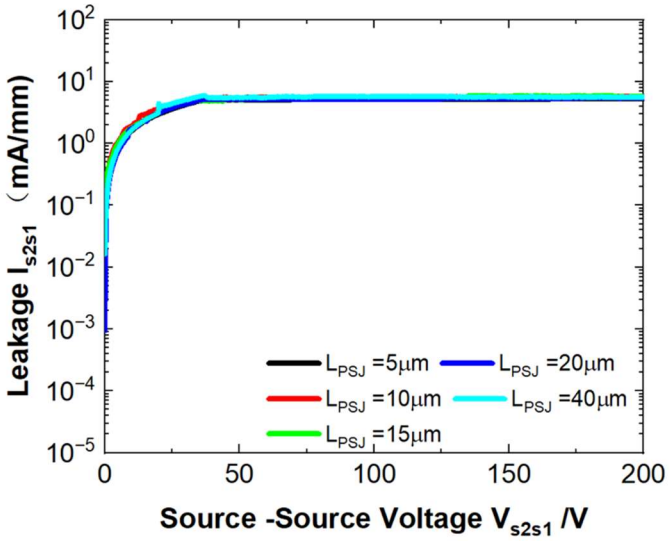


Figure 4.3.9: The leakage current of Bi PSJ SG HFETs with various L_{PSJ}

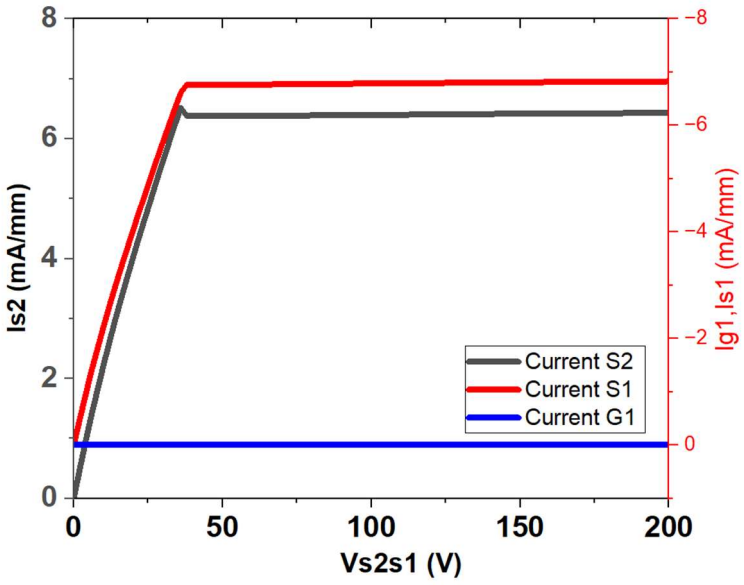


Figure 4.3.10: The leakage Is2, Is1 and Ig1 of Bi PSJ SG HFET with 40µm-LPSJ.

4.3.2 Analysis in specific on-state resistance

In order to optimise the on-state performance of Bi PSJ HFETs, it is necessary to build the analytical models to investigate the Ron.A of Bi PSJ HFETs. Under on-state conditions, the source current flows through the 2DEG channel. According to differences in the sheet carrier density and the mobility of 2DEG and 2DHG, Bi PSJ SG HFETs can be divided into different areas.

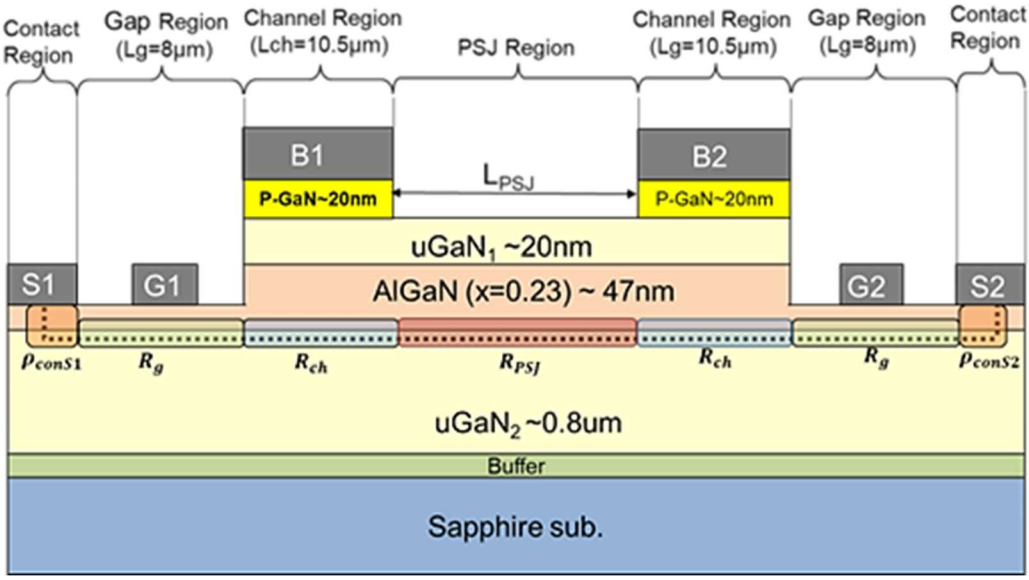


Figure 4.3.11: Cross-section of Bi PSJ SG HFET with the divided region along the current path.

Along the dashed line in the current flow direction shown in Figure 4.3.11, Bi PSJ SG HFETs can be divided into seven regions: the PSJ region, channel regions, gap regions, and contact regions. Gap regions consist of 2 areas between the source and the adjacent gate. The regions under the bases are defined as channel regions, and the regions under the source electrodes are defined as contact regions. Therefore, the total specific on-state resistance (Ron.A) can be considered as the sum of the PSJ region resistance (R_{PSJ}), two channel region resistances (R_{ch}), and two gap region resistances (R_g) multiplies the device area (A) and then plus the contact resistivity (ρ_{conS1} and ρ_{conS2}), as shown in Equation (4.2).

$$\boldsymbol{R_{on}A = (R_{PSJ} + 2R_{ch} + 2R_g) \times A + \rho_{conS1} + \rho_{conS2}} \text{------(4.2)}$$

The contact resistivity of the Source1 and the Source2 electrode ($\boldsymbol{\rho_{conS1}}$ and $\boldsymbol{\rho_{conS2}}$) can be measured and calculated by the transmission line method (TLM), as shown in

$$\boldsymbol{\rho_{conS1} = \rho_{conS2} = R_c \times L_T \times W = 0.26\ m\Omega \cdot cm^2} \text{ ------(4.3)}$$

The resistance of other regions can be expressed as

$$R = \frac{\boldsymbol{L}}{\boldsymbol{q\mu\sigma W}} \text{ ------(4.4)}$$

Where **q** is the electron charge, **W** stands for the device width. **μ** stands for the mobility of 2DEG and **σ** is the 2DEG sheet density. **L** is the length of the corresponding region, which is shown in Figure 4.3.11.

In the calculation, the 2DEG mobility (μ) is set around 700cm^2/Vs same as the measured value shown in Figure 4.2.6. Assuming the device width is constant, the resistance of the PSJ region, gap regions and channel regions are determined by the length (L) and the sheet density (σ) of each region.

The sheet density (σ) can be calculated using analytical models of sheet carrier densities in PSJ HFETs [88], influenced by the thickness of PSJ layers and Al mole fraction. The simplified expression for 2DEG sheet density(n_s) and 2DHG sheet density (ρ_s) is shown as Equation (4.5) and Equation(4.5), respectively[88].

$$\boldsymbol{n_s} = \frac{\sigma_{AlGaN}}{e} - \frac{\phi_{n,\ GaN1} \cdot C_{GaN1}}{e^2} - \frac{C_{AlGaN} E_G}{e^2} \text{------(4.5)}$$

$$\boldsymbol{p_s} = \frac{\sigma_{AlGaN}}{e} + \frac{\sigma_{p-GaN} \cdot C}{eC_{p-GaN}} - \frac{\phi_{p,\ p-GaN} \cdot C}{e^2} - \frac{C_{AlGaN} E_G}{e^2} \text{------(4.6)}$$

Where σ_{p-GaN} and σ_{AlGaN} are the surface sheet charge in p-GaN layer and AlGaN layer, respectively. σ_{AlGaN} is the sum of spontaneous polarisation charge (P_{sp}) and piezoelectric polarisation charge (P_{pz}). The bandgap of the GaN layer expressed in terms of E_G. $\phi_{p,p-GaN}$ is the valance band barrier height of the p-GaN cap and $\phi_{n,p-GaN}$ is the conduction band barrier height of the u-GaN$_1$ sub-layer. C (C=$C_{p-GaN} + C_{GaN2}$,)represents the total unit area capacitance of the p-GaN and u-GaN$_2$ layers. C_{p-GaN} , C_{AlGaN} and C_{GaN1} are the unit area capacitance of p-GaN, AlGaN and u-GaN1 layer. Here, the unit area capacitance of each layer can be calculated by Equation (4.7).

$$\mathbf{C_{layer}} = \frac{\mathcal{E}_{layer}}{t_{layer}} \text{ ------(4.7)}$$

Where $\mathcal{E}_{layer}$ stands for the electric fields and t_{layer} is the thickness of the corresponding layers.

Table 4.1 shows the parameters and equations for calculating 2DEG and 2DHG sheet density. Considering that partial carriers are accelerated by the electric field and captured by traps, the sheet density of 2DEG is adjusted with experimental results.

Table 4.1: parameters and equations for calculating Sheet density([33],[34],[35],[88]).

Symbol	Unit	Value
$\epsilon_{Al_xGa_{1-x}N}$		$8.5x\epsilon_0 + 8.9(1-x)\epsilon_0$
ϵ_{GaN}		$8.9\epsilon_0$
$E_g(Al_xGa_{1-x}N)$	eV	$E_g(AlN)x + E_g(GaN)(1-x) - 1.3x(1-x)$
σ_{AlGaN}	C/m^2	$\lvert\Delta P_{sp}\rvert + \lvert\Delta P_{pz}\rvert$
$P_{sp}(GaN)$	C/m^2	-0.034
$P_{sp}(Al_xGa_{1-x}N)$	C/m^2	$(-0.09x - 0.034(1-x))$
$P_{pz}(Al_xGa_{1-x}N)$	C/m^2	$2\frac{a(x)-a_0}{a_0}\left(e_{31} - \frac{C_{13}}{C_{33}}e_{33}\right)$
$a(Al_xGa_{1-x}N)$	Å	$a(Al_xGa_{1-x}N) = 3.112x + 3.189(1-x)$
$a_0(GaN)$	Å	3.189
e_{31}	C/m^2	$-0.53x - 0.34(1-x)$
e_{33}	C/m^2	$1.5x + 0.67(1-x)$
C_{13}	Gpa	$127x + 100(1-x)$
C_{33}	Gpa	$382x + 392(1-x)$
m_0	kg	9.11×10^{-31}
$m_{e(Al_xGa_{1-x}N)}$		$(0.314x + 0.2(1-x))m_0$
$m_{\mathrm{h}(Al_xGa_{1-x}N)}$		$(0.417x + 1.0(1-x))m_0$
ħ	$J \cdot s$	1.05×10^{-34}

Figure 4.3.12 presents the calculated and measured Ron.A of Bi PSJ SG HFETs with L_{PSJ} from 5µm to 40µm at room temperature, as well as Ron.A of unidirectional PSJ Ohmic Gate HFETs (PSJ OG HFETs) from POWDEC.KK was reported in[88]. The identical Vg (Vg1) = 0V is applied to the

calculation and measurement. It can be found that calculated Ron.A of Bi PSJ SG HFETs fits well with the experimental results when varying PSJ length from 5 to 40μm. Factors like Structural misalignment, random measurement errors, and the assumption of constant mobility might contribute to the differences shown in Figure 4.3.12. In addition, it should be noted that the 2DEG mobility for each region is assumed as constant in calculations, unlike in actual devices, where it can be affected by some factors, such as charge concentration and electrical fields. Compared with Ron.A of PSJ OG HFETs, the resistance of 2 gap regions (Rg) and 2 channel regions (Rch) contribute to additional resistance for Bi PSJ SG HFETs, because of the non-uniform thickness of AlGaN layer and defects in AlGaN growth as well as long region length designed according to design rules. In addition, the low electron mobility is the reason for the high on-state resistance of Bi PSJ SG HFETs. It should be noticed that the epitaxial structure for Bi PSJ SG HFETs and PSJ OG HFETs is different. The lower on-state resistance can be obtained by improving the EPI structure and device structure.

Table 4.2 shows the calculated resistance component ratio to the total Ron.A of Bi PSJ SG HFETs with L_{PSJ} from 5μm to 40μm. With the decrease in L_{PSJ}, the percentage of Rch and Rg to the total Ron.A becomes large. In this project, the long channel region length and gap length are designed for alignment margin and to ensure electrodes of Base and Gate are wider enough not to destory, especially for large-area devices. For future work, the gap region and channel region can be reduced in the mask design which can reduce the on-state resistance.

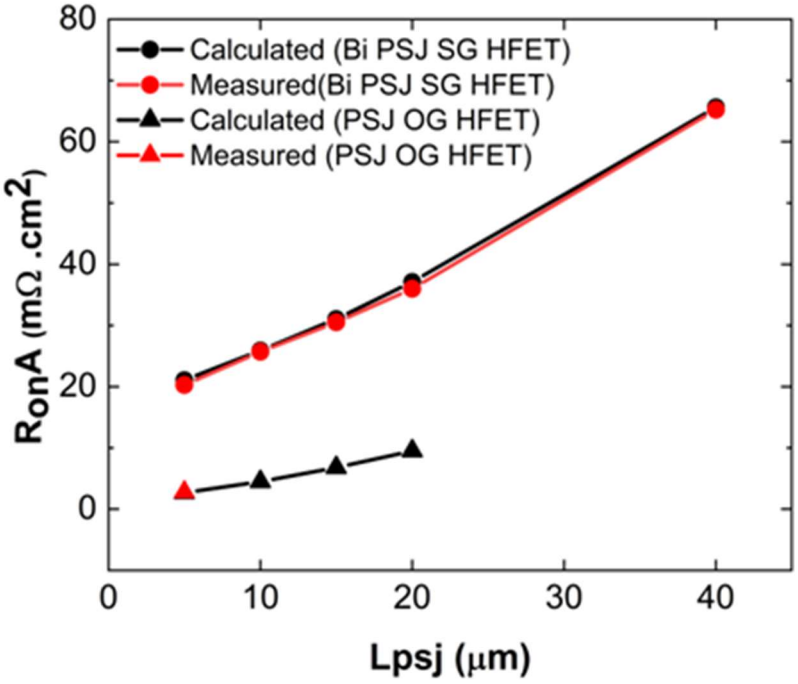


Figure 4.3.12: The calculated and measured Ron.A of Bi PSJ SG HFETs and PSJ OG HFETs with LPSJ from 5μm to 40μm at room temperature.

Table 4.2: The calculated resistance component ratio to the total Ron.A of Bi PSJ SG HFETs.

L_{PSJ} (µm)	Component Ratio (%)			ρ_{conS} (mΩ.cm²)	Ron.A (mΩ.cm²)
	R_{PSJ}	R_g	R_{ch}		
5	10	46	44	0.26	21.07
10	19	42	40		25.91
15	26	38	36		31.26
20	32	35	33		37.12
40	48	27	25		65.64

4.3.3 Large-area Bidirectional PSJ HFETs with Schottky Gate

I-V characteristics of large-area PSJ SG HFET with 15µm-L_{PSJ} in the first and third quadrant is shown in Figure 4.3.13. it is apparent that the device has symmetrical output current-voltage characteristics in both directions. In the design, the current density in each finger unit cell (normalised to gate width) is estimated at 30mA/mm. However, the measured current density is around 10mA/mm, which is the main factor that the large-area devices can not reach the desired current capability. In addition, the impedance of electrodes and the midway fracture also increase the on-state resistance. Figure 4.3.14 is measured Input characteristics with ~-6.3V threshold voltage, and Figure 4.3.15 presents the device leakage in both directions during off-state.

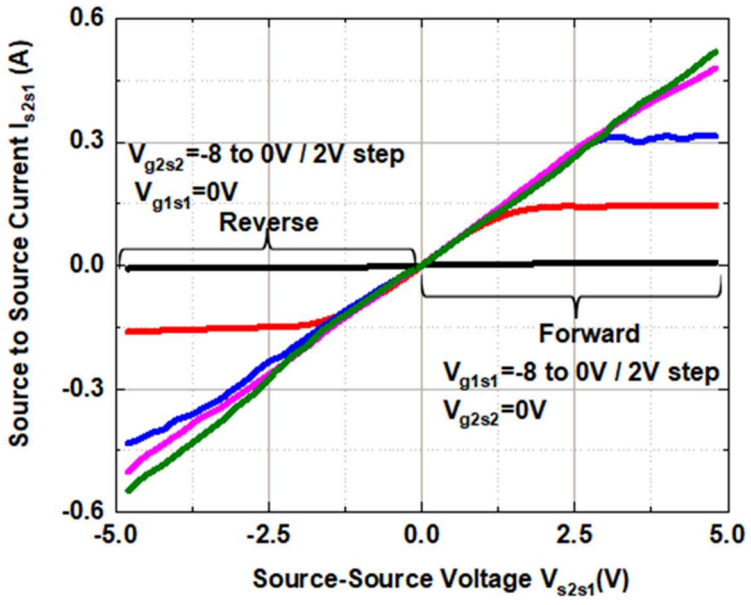


Figure 4.3.13: Measured I-V characteristics of large-area PSJ SG HFET with 15µm-L_{PSJ}.

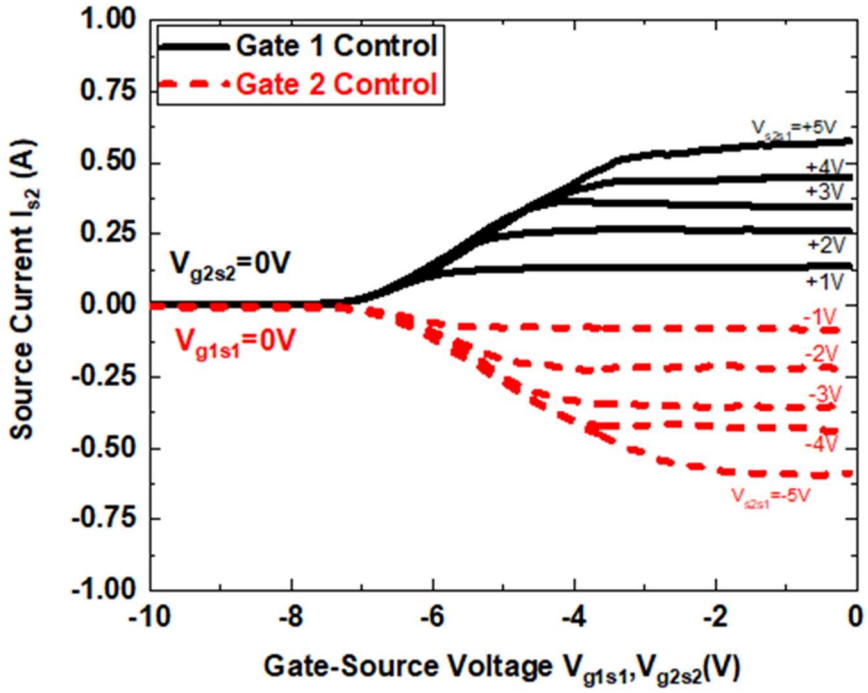


Figure 4.3.14: Measured Input characteristics of large-area PSJ SG HFET with 15µm-L_{PSJ}

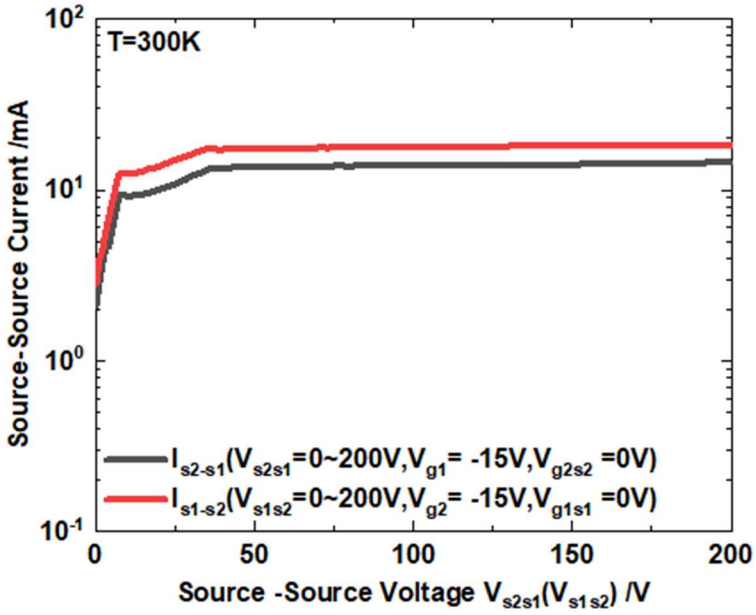


Figure 4.3.15: Measured off-state leakage of large-area PSJ SG HFET with 15µm-L_{PSJ}.

4.4 Bidirectional PSJ HFETs with Ohmic Gate

Fabricated Bi PSJ OG HFETs on Sapphire substrate have four pads of Gate1, Gate2, Source1 and Source2. Figure 4.4.1 shows the cross-section schematic of fabricated Bi PSJ OG HFETs. As

mentioned in Section 3.2.1, Bi PSJ OG HFETs can be operated as unidirectional HFETs with/without HD-GIT mode and diodes in both directions under different gate bias conditions. Section 4.4.1 presents the electrical characteristics results of test structure Bi PSJ OG HFETs with Gate Design1 (PSJ-G1) working in the First and third quadrants as a diode and PSJ HD-GIT HFETs.

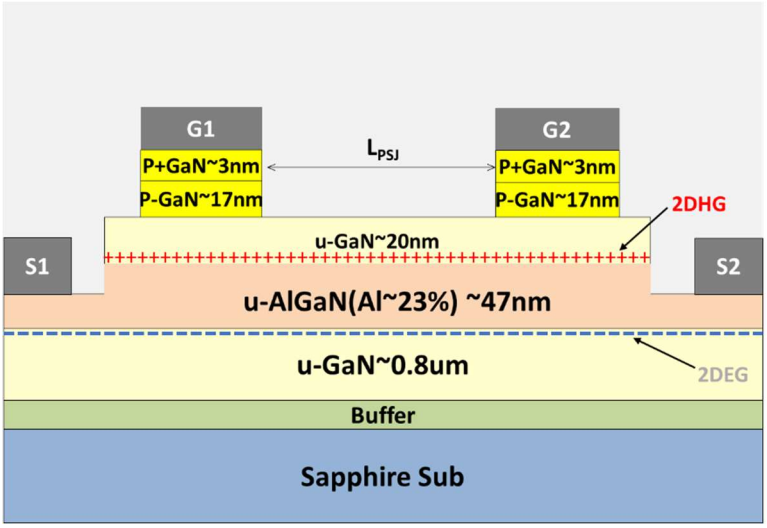


Figure 4.4.1: Cross-section schematic of fabricated Bi PSJ OG HFETs

4.4.1 Electrical characteristics results

I-V Characteristics

Figure 4.4.2 show I_{s2}-V_{s2s1} characteristics of Bi OG PSJ HFETs working in both the first and third quadrant under various bias conditions as a diode and PSJ HD-GIT HFETs. . The length of L_{psj} is 15µm. When Vs2s1 is positive, Bi PSJ HFETs are controlled by Gate 1 while Bi PSJ HFETs are controlled by Gate 2 in a reverse bias condition. The Calculated Area Specific On-state Resistance (Ron.A) of the Bi PSJ OG HFET with 15µm-Lpsj is 20.53 mΩ.cm^2 at V_{s2s1}=1V, V_{g1s1}=0V. When Gate1 voltage is smaller than -7V, Bi PSJ OG HFETs enter off-state. Dash lines shown in the 'Forward Region' in Figure 4.4.2 are measured by keeping the Gate 2 voltage with respect to Source2 voltage at -9V (V_{g2s2}=-9V). Same as Bi PSJ SG HFETs, it shows that forward current can also be controlled by Gate1 voltage, although the on-state voltage (Von) increases.

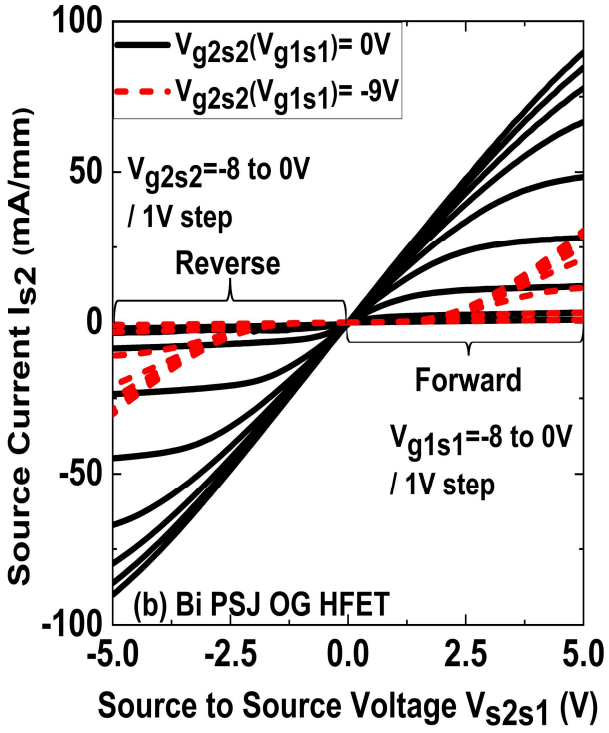


Figure 4.4.2: The I_{s2}-V_{s2s1} characteristics of Bi OG PSJ HFETs in both polar under various bias conditions

In the 'Forward Region' (V_{s2s1}>0V), keeping Gate 1 voltage at 0V and changing the negative voltage V_{g2s2} from -7V to -15V, the variation of on-state voltage the Bi PSJ OG HFET with 15µm-L_{psj} is shown in Figure 4.4.3(a). Differing from Bi PSJ SG HFETs, the on-state voltage of Bi PSJ OG HFETs depends on the V_{g2s2}, which goes up with the smaller V_{g2s2}. The increasing on-state voltage in Bi PSJ OG HFETs can be attributed to the depletion region is controlled by Ohmic Gate electrodes. Figure 4.4.3(b) demonstrates a linear relationship between the negative voltage V_{g2s2} and on-state voltage, as similar to simulation results. The on-state voltage in the 'Reverse Region' (V_{s2s1}<0V) is identical to that of forward. Therefore, For Bi PSJ OG HFETs can control the on-state voltage by changing V_{g2s2} in the 'Forward Region' and V_{g1s1} in the 'Reverse Region'.

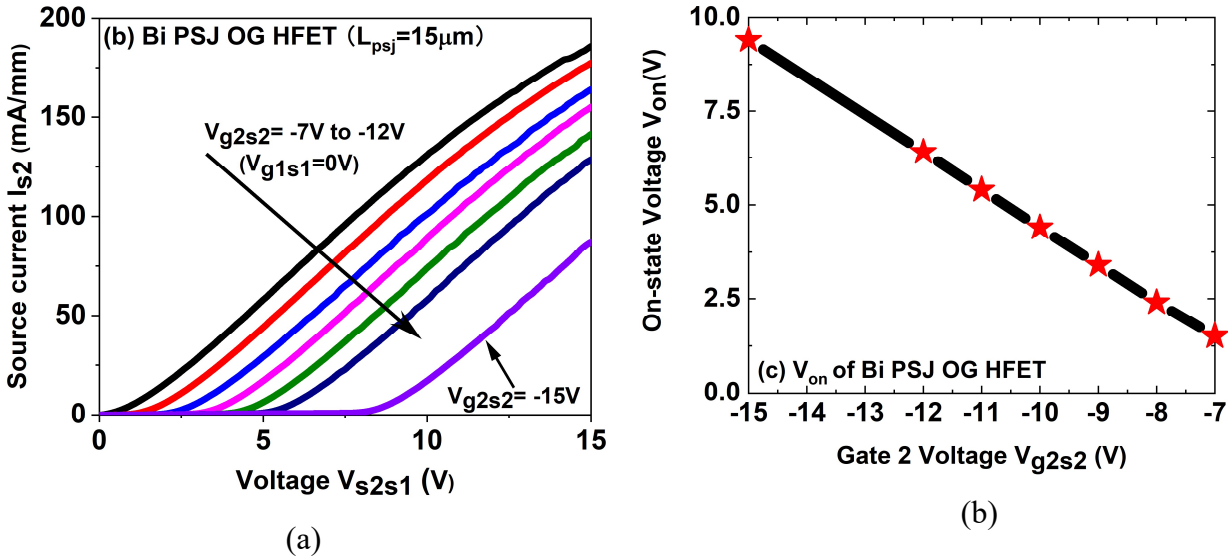


Figure 4.4.3: The variation of on-state voltage of the Bi PSJ OG HFET with 15μm-Lpsj when Vg2s2=-7V to -15V, Vg1s1=0V

Temperature-dependent forward I_{s2s1}-V_{s2s1} characteristics at V_{g2s2}=0,V_{g1s1}=0V are shown in Figure 4.4.4. Figure 4.4.5 shows the area-specific on-state resistance (Ron.A) of Bi PSJ OG HFETs versus the temperature from 25°C to 125°C. The length of PSJ is 5,10,15,20, and 40μm. It can be found that the L_{PSJ} and temperature are essential for on-state behaviour. With the temperature increased, Ron.A of Bi OG PSJ HFETs increase.

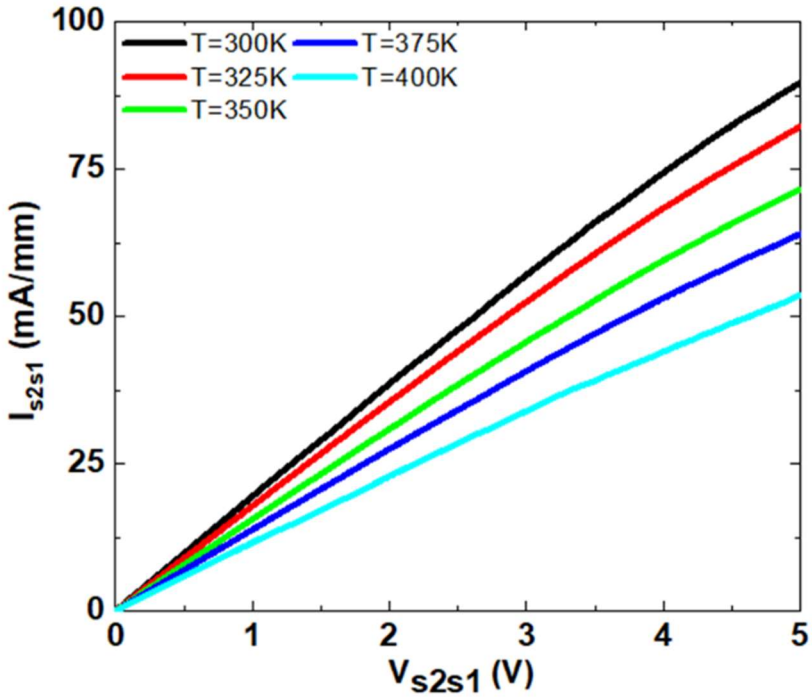


Figure 4.4.4: Temperature-dependent forward Is2s1-Vs2s1 characteristics of Bi PSJ OG HFET with 15µm at Vg2s2=0, Vg1s1=0V

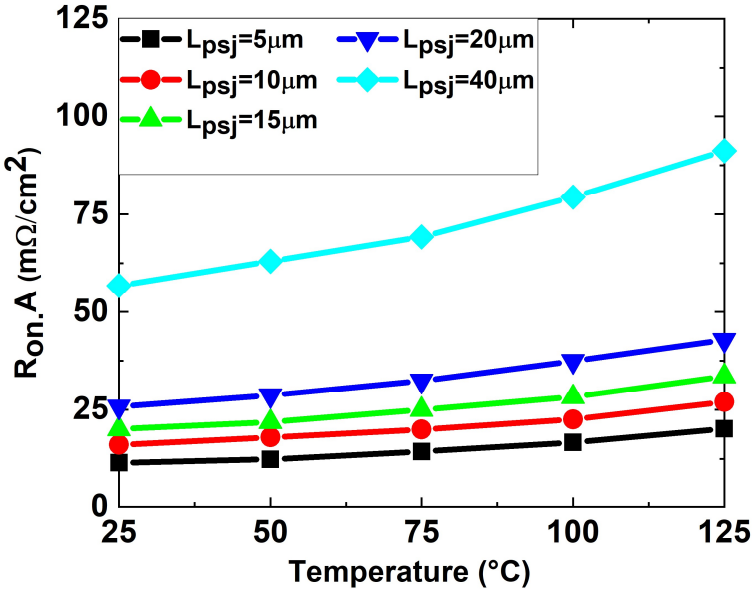


Figure 4.4.5: Calculated area-specific on-state resistance (Ron.A) of Bi PSJ OG HFETs versus the temperature from 25ºC to 125ºC

Input characteristics

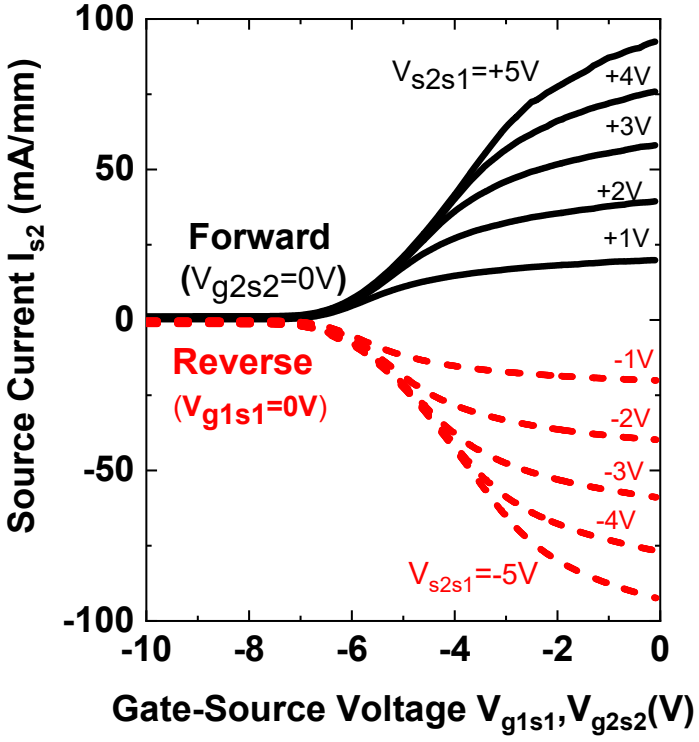


Figure 4.4.6: Transfer characteristics of Bi PSJ OG HFETs with 15µm

Figure 4.4.3 shows transfer characteristics of fabricated Bi PSJ OG HFETs with 15µm L_{PSJ}, Source current I_{s2} is successfully controlled by Gate1 voltage (V_{g1s1}) and Gate2 voltage in the forward region and reverse region, respectively. The threshold voltage V_{th} of Bi PSJ OG HFETs is about -6.7V in both directions. Similar to the Simulation results, OG structure has the lower threshold voltage Vth than that of SG structure, which means the controllability is better for an SG design.

Off-state leakage characteristics

Forward off-state leakage characteristics (V_{g2s2} = -15V) of Bi PSJ OG HFETS with different L_{PSJ} are plotted in Figure 4.4.7. Measured reverse characteristics of I_{s1} -V_{s1s2} with V_{s2s1} < 0V are identical with that of forward. Figure 4.4.8 shows the leakage Is2, Is1 and Ig1 of Bi PSJ OG HFET with 15µm-L_{PSJ}. At Vs2s1=200V, the measured device leakage is slightly high, around 8mA/mm. Similarly, the high device leakage is due to buffer leakage.

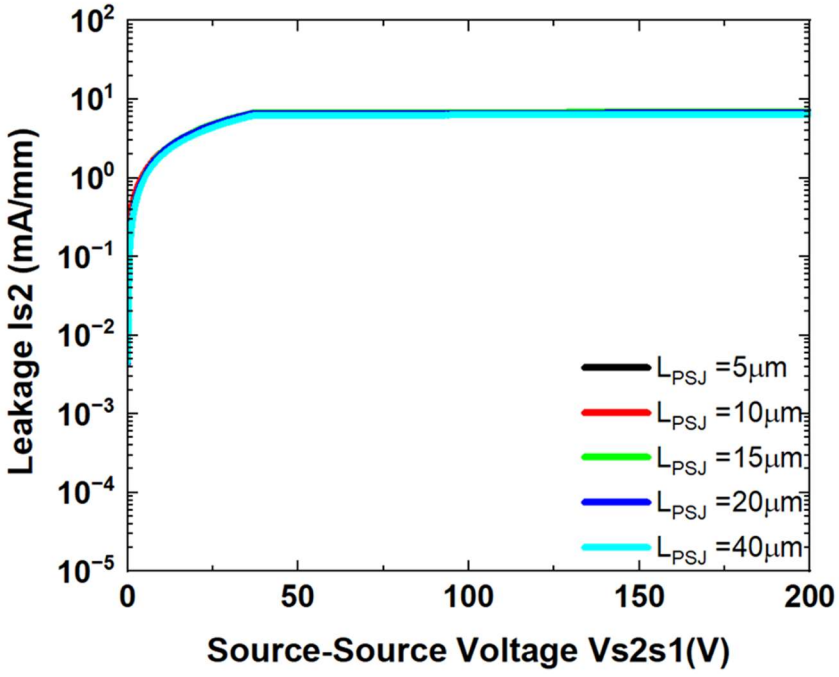


Figure 4.4.7: The leakage current of Bi PSJ OG HFETs with various L_{PSJ}.

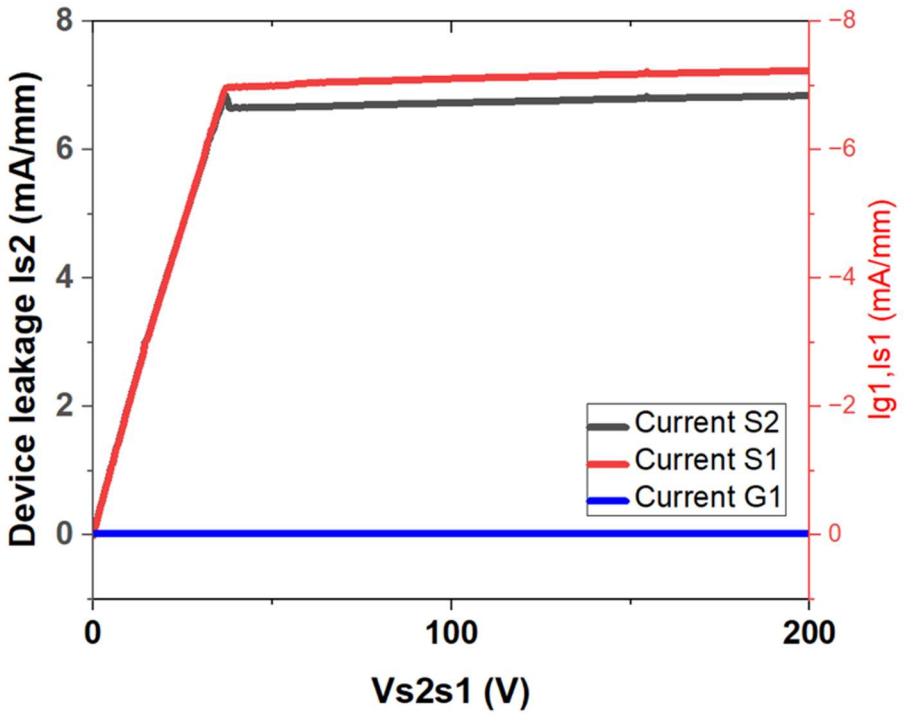


Figure 4.4.8: The leakage Is2, Is1 and Ig1 of Bi PSJ OG HFET with 15μm-LPSJ.

4.4.2 Analysis in specific on-state resistance

According to differences in the sheet carrier density and the mobility of 2DEG and 2DHG, Bi PSJ OG HFETs can be divided into 7 areas, as shown in Figure 4.4.9.

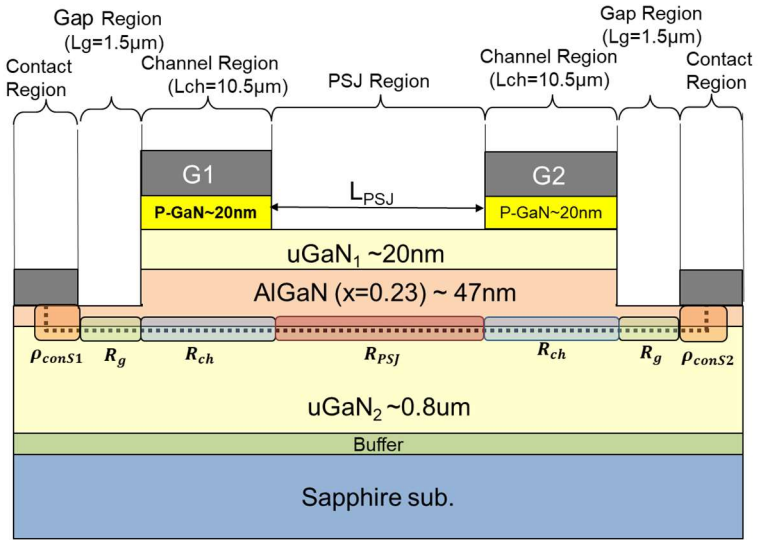


Figure 4.4.9：Schematics of device cross-section for calculating Ron.A of Bi PSJ OG HFET

In the similar manner, Bi PSJ OG HFETs can be divided into seven regions along the dashed line in the current flow direction shown in Figure 4.4.9, i.e. the PSJ region, channel regions, gap regions, and contact regions. The total specific on-state resistance be expressed at Eqaution (4.8)

$$\boldsymbol{R_{on}A = (R_{PSJ} + 2R_{ch} + 2R_g) \times A + \rho_{conS1} + \rho_{conS2}} \qquad \text{-----(4.8)}$$

The contact resistivity of the Source1 and the Source2 electrode ($\boldsymbol{\rho_{conS1}}$ and $\boldsymbol{\rho_{conS2}}$) is 0.26 mΩ·cm^2 as the same that in Bi PSJ SG HFETs.

Assuming the device width is constant, the resistance of the PSJ region, gap regions and channel regions are determined by the length (L) and the sheet density (σ) of each region. The sheet density (σ) can be calculated by Equations (4.1) and (4.2). According to Equation (4.3), The resistance of other regions can be calculated with the measured 2DEG mobility(~700cm^2/Vs) and calculated sheet density of 2DEG. It should be noted that the sheet density of 2DEG in PSJ OG HFETs is adjusted to fit with experimental results.

As presented in Figure 4.4.10, summarise the calculated and measured Ron.A for both PSJ SG HFETs and Bi OG HFETs. It can be found that analytical Ron.A of Bi PSJ HFETs are fitted with experimental results. Whether by calculation or measurement, it shows an upward linear trend with the increase in L_{PSJ}. In addition, Ron.A of Bi PSJ OG HFET is more significantly lower than that in PSJ SG HFETs when altering PSJ length because OG structure has low gap resistance (Rg) in the shorter gap region.

Table 4.3 shows each theoretical component ratio to the total Ron. It should be addressed that the resistance of the channel region is an essential factor to Ron. A of Bi PSJ OG HFETs. The channel region length leading to high Rch can be reduced and optimized in the future mask design.

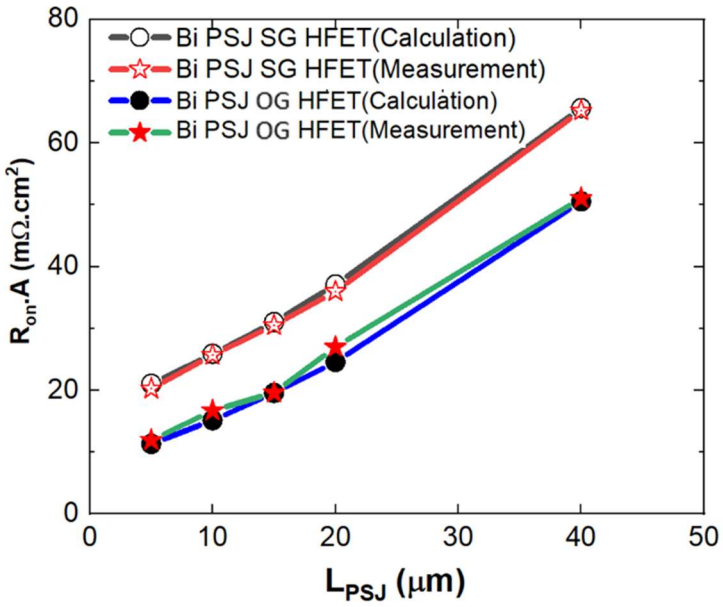


Figure 4.4.10: Calculated and measured Ron.A of Bi PSJ HFETs with SG and OG at room temperatures when V g1s1 =0V, Vg2s2=0V.

Table 4.3: Each component ratio to the total Ron in the Analytical model of Bi PSJ OG HFETs.

L_{PSJ} (μm)	Component Ratio (%)			ρ_{consS} (mΩ.cm^2)	Ron.A (mΩ.cm^2)
	R_{PSJ}	R_g	R_{ch}		
5	17	14	69	0.26	11.35
10	28	12	60		15.17
15	37	38	36		19.58
20	44	9	46		24.59
40	61	7	32		50.55

4.4.3 Comparison of Bidirectional PSJ HFETs with Ohmic Gate with/without HD-GIT mode

When G2(G1) is floating in the forward (reverse) region, the Bi PSJ OG HFETs act as the conventional PSJ HFETs without HD-GIT. Figure 4.4.11 and Figure 4.4.12 compares the forward IV characteristic and input characteristics of PSJ HD-GIT and PSJ HFETs with 5μm-L_{PSJ}. It can be found that PSJ HFETs with HD-GIT has a dramatic increase of electron density and the on-state current owing to the conductivity modulation by injecting holes from the p-GaN to the device that releases the trapped electrons in the surface and bulk instantaneously.

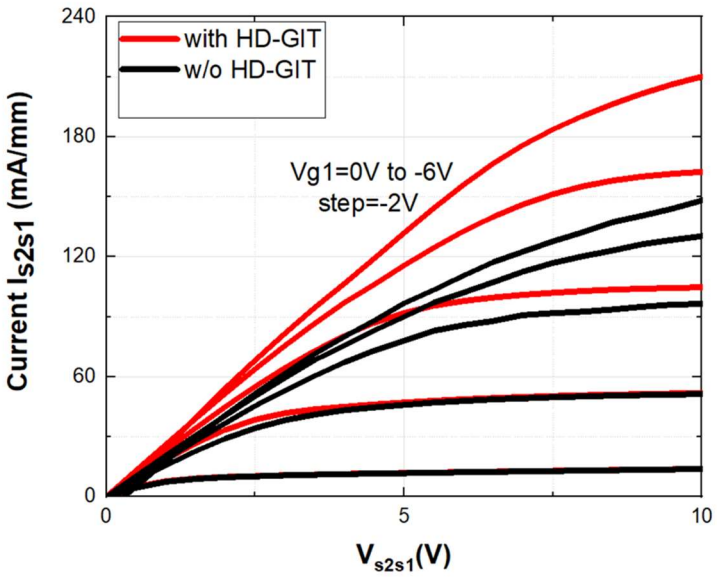


Figure 4.4.11: IV characteristics comparison of Bi PSJ HFETS with /without HD-GIT mode.

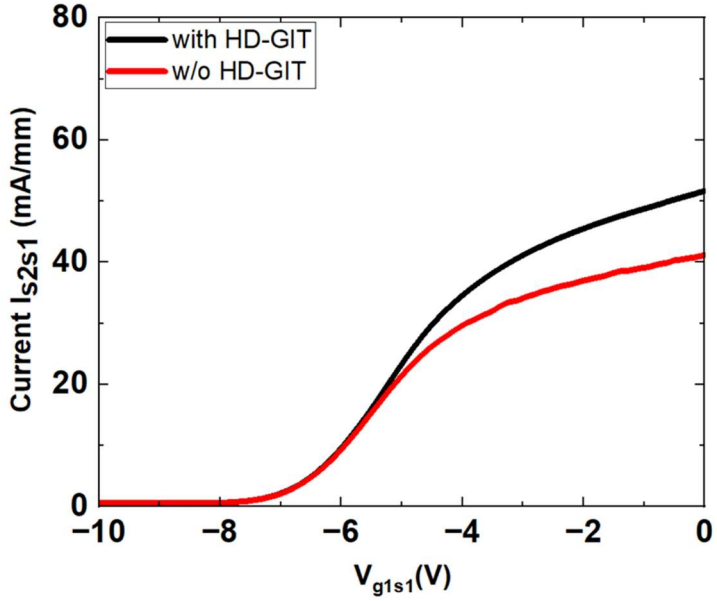


Figure 4.4.12: Input characteristics comparison of Bi PSJ HFETS with /without HD-GIT mode.

4.4.4 Gate structure design

As described in Figure 4.4.13, there are four gate designs, including (a)PSJ-G1, (b)PSJ-G2, (c)PSJ-G3 and (d)PSJ-G4, that change the misalignment between the etch layers.

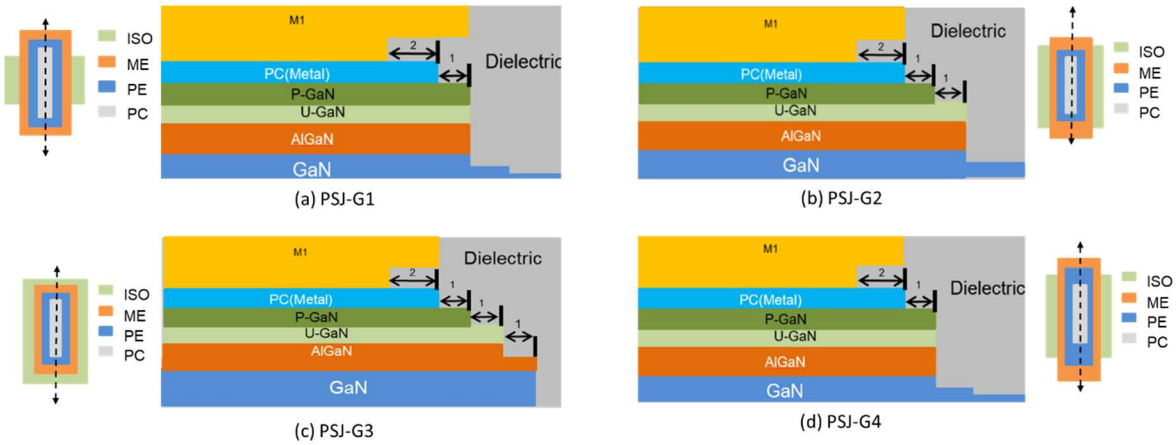


Figure 4.4.13: Schematic gate structures for Bi PSJ OG HFETs

Figure 4.4.14 shows the transfer characteristics comparison of Bi PSJ OG HFETs with 15µm-L_{PSJ} in 4 gate designs. The threshold voltage is similar at -6.7V, regardless of gate designs. The main difference is that the Is2s1 increases when the Vs2s1 increases from 1V to 5V in the turn-off.

Figure 4.4.15 plots the I_{s2s1}-V_{s2s1} curves of Bi PSJ OG HFETs with 15µm-L_{PSJ} in both directions. The measured forward on-state of 4 gate designs at Vs2s1=1V and Vg1s1=0V are 55.56 Ω/mm, 49.65 Ω/mm, 54.64 Ω/mm and 52.44 Ω/mm, respectively, with similar values. The difference occurs when the Gate voltage is smaller than the threshold voltage(-6.7V), as indicated in Figure 4.4.14. Devices with PSJ-G2 and PSJ-G3 have considerable current I_{s2s1} when the Gate1 voltage is smaller than the threshold voltage. Gate Design1(PSJ-G1) has the lowest on-state source voltage when V_{g1s1}(V_{g2s2})<Vth.

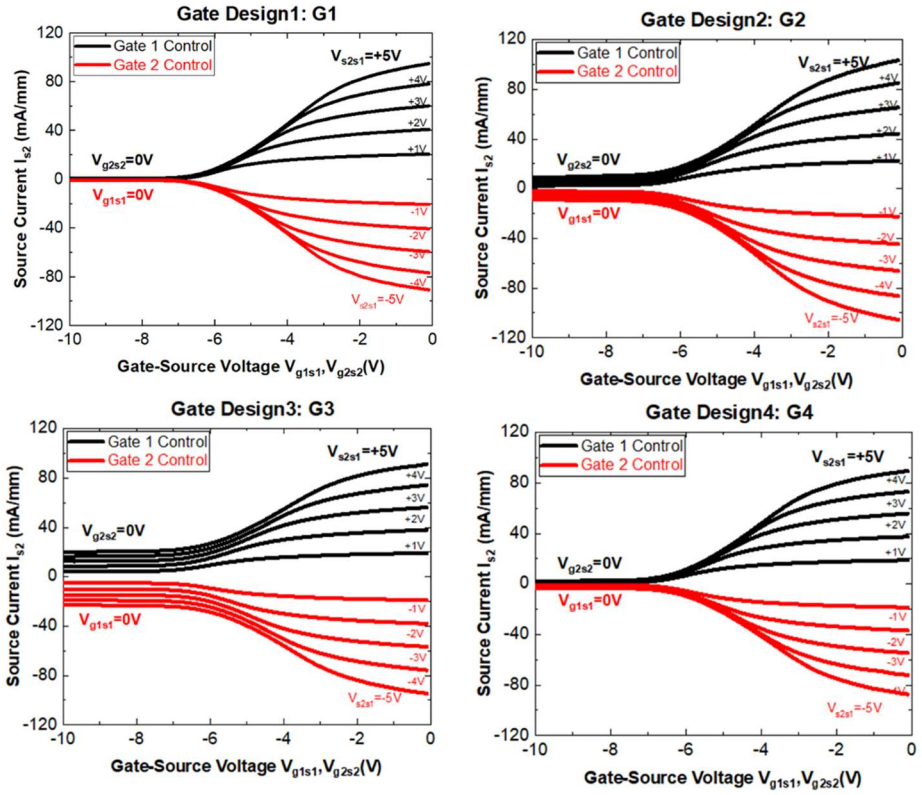


Figure 4.4.14:Transfer characteristics comparison of Bi PSJ OG HFETs with 15µm-L_{PSJ} in 4 gate designs.

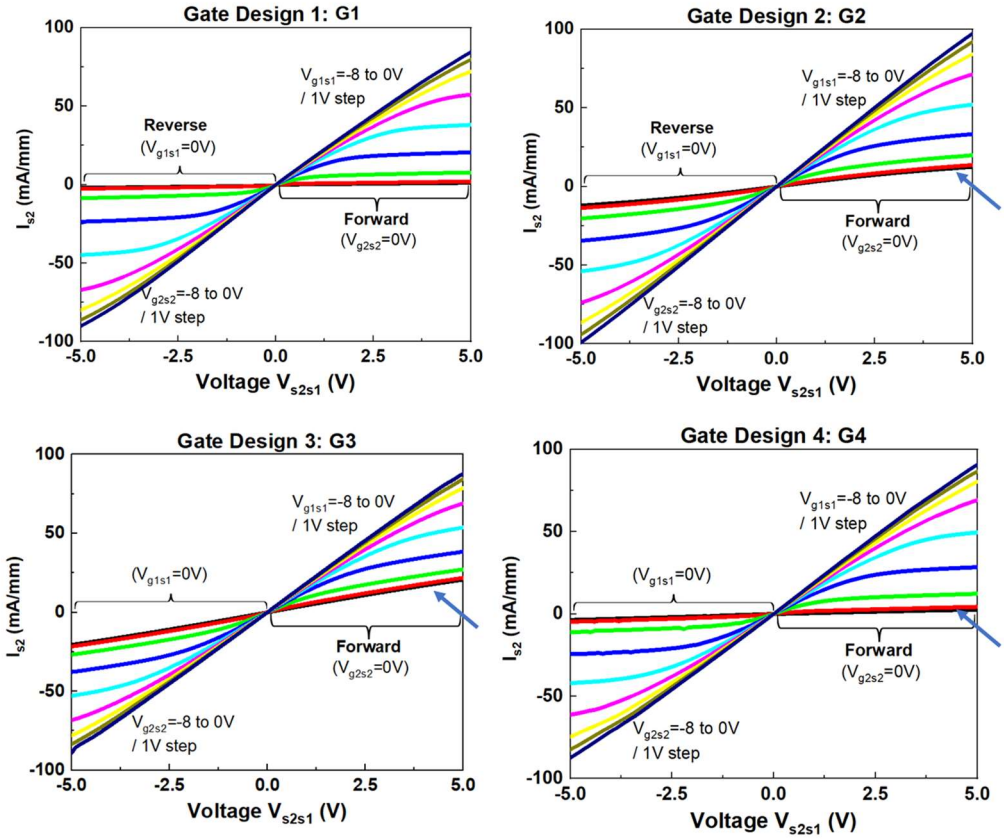


Figure 4.4.15: Output characteristics comparison of Bi PSJ OG HFETs with 15µm-L_{PSJ} in 4 gate designs.

A comparison of forward off-state leakage for Bi PSJ OG HFETs with 4 gate structures is plotted in Figure 4.4.16. Figure 4.4.17 shows the average off-state leakage I_{s2s1} for eight samples of Bi PSJ OG HFETs with 15µm-L_{PSJ} with the error bars indicating standard deviations. Both devices with PSJ-G2 and PSJ-G3 have much high leakage because the 2DHG channel is shorter than 2DEG channel, which breaks the charge balance. Compared with PSJ-G4, PSJ-G1 with the longer metal gate electrode has the lowest device leakage when the V2s1 increase to 200V, which means the Design PSJ-G1 has better control of 2DHG.

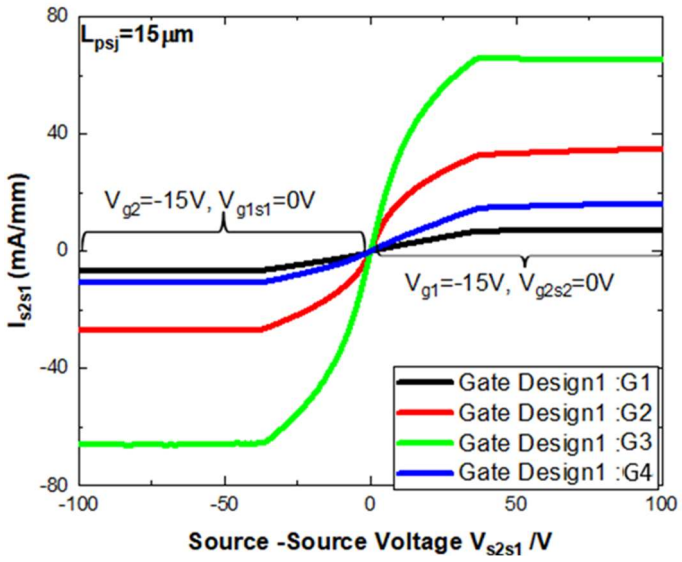


Figure 4.4.16: Device leakage comparison of Bi PSJ OG HFETs with 15µm-L_{PSJ} in 4 gate designs.

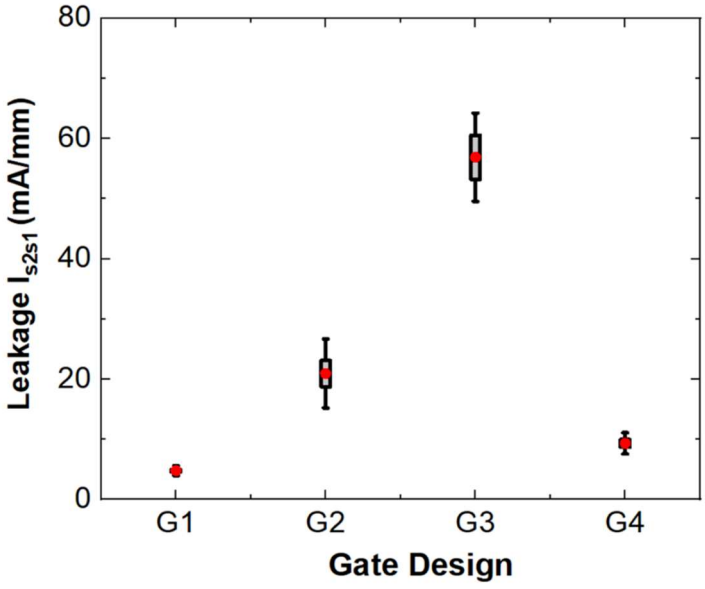


Figure 4.4.17:Avergae leakage Is2s1 for 8 samples of Bi PSJ OG HFETs with 15µm-L_{PSJ}.

4.4.5 Large-area Bidirectional PSJ HFETs with Ohmic Gate

Figure 4.4.18 (a)-(b) shows the output and transfer electrical characteristics of large-area PSJ OG HFET with 15µm-L_{PSJ}. The device's threshold voltage (V_{th}) obtained from transfer characteristic is ~ - 6.7 V. Measured high off-state leakage of large-area PSJ OG HFET with 15µm-L_{PSJ} due to the high buffer leakage is shown in Figure 4.4.19.

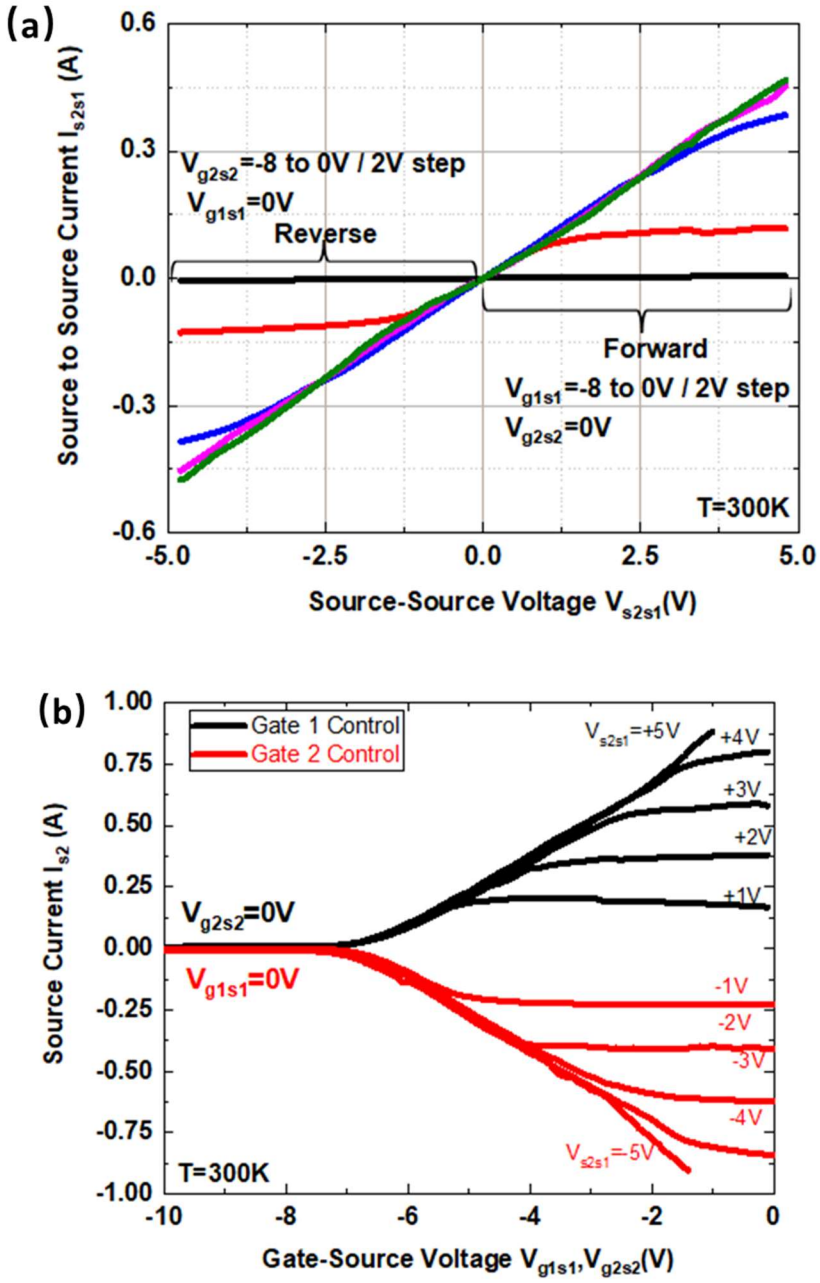


Figure 4.4.18: Measured (a)I-V characteristics and (b) input characteristics of large-area PSJ OG HFET with 15µm-L_{PSJ}.

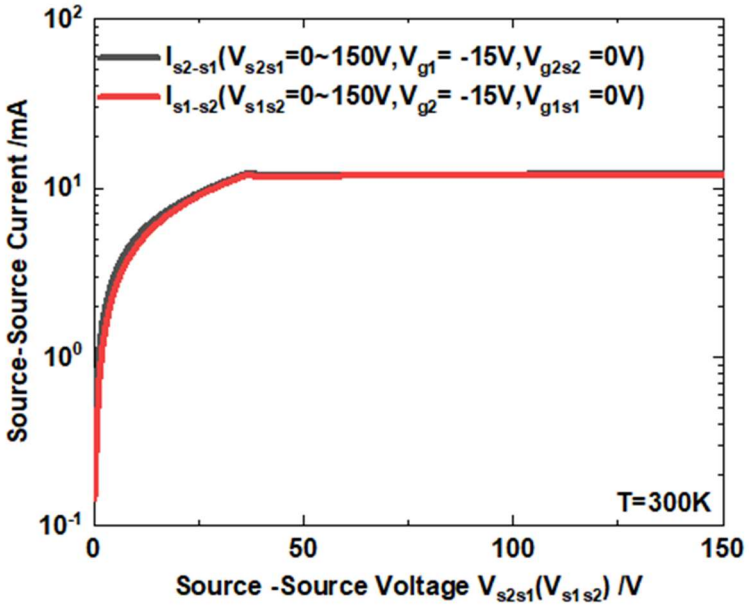


Figure 4.4.19: Measured off-state leakage of large-area PSJ OG HFET with 15µm-L_{PSJ}.

4.5 Summary

Bi PSJ HFETs in test structure and large-area layout on 6' Sapphire are measured under different gate bias conditions and discussed in detail. Static electrical characterisations, including transfer, output, and off-state characteristics, are performed. Experimental data prove that both types of compact monolithic fabricated Bi PSJ HFETs succeed in conducting on-state current in both directions. The slightly high off-state leakage is measured due to the high buffer leakage, which needs to improve the epitaxial structure for future work. The functions of fabricated Bi PSJ HFETs in various bias conditions also has been proven by experimental data, which is consistent with the simulation results. Moreover, analytical models of the specific on-state resistance (Ron. A) for Bi PSJ HFETs with Schottky gate and Ohmic gate are presented to analyse compent ratio to Ron.A of fabricated Bi PSJ HFETs.

Chapter 5: On-state PSJ device performance as the function of Temperature

Due to GaN's lower thermal conductivity compared to silicon, devices based on it degrade as temperature rises, increasing on-state resistance and turn-on/off losses during switching (Si). The performance of GaN-based PSJ devices at high temperatures must be assessed. This chapter will analyse the effects of temperature on Ohmic contacts for PSJ structure, Merged Schottky Barrier diodes, and PSJ HFETs.

5.1 Ohmic contact property

5.1.1 Theory of Ohmic contact property

When the metal comes into contact with the semiconductor, a potential barrier is formed at the interface. There are two types of metal-semiconductor contacts are known: ohmic and Schottky contacts. A Schottky barrier refers to a metal-semiconductor contact having a large barrier height. The ohmic contacts act as the resistance, which has linear and symmetrical I-V characteristics. The ohmic contact is negligible compared to the resistance of the semiconductor. The main parameter to characterize the ohmic contact is conduct resistivity (ρ_c).

For ohmic contact, there are 4 basic mechanisms considered determinative for the current transport, such as thermionic emission (TE), field emission (FE), Recombination in the space-charge region and Hole injection from the metal into the semiconductor. The current transport through the contact is realized mainly by thermionic emission (TE) or field emission (FE). At a low semiconductor doping level ($<10^{17}cm^{-3}$), the current transport is determined by the thermionic emission. It is the phenomenon whereby electrons gain kinetic energy to emit from a metal surface due to an increase in its temperature. With thermionic emission, the contact resistivity can be expressed in Equation (5.1) as the function of temperature. With the temperature increasing, the contact resistivity reduces.

$$\rho_C = \frac{k}{qA^*T} EXP\left(\frac{q\phi_{Bn}}{KT}\right) \qquad \text{------(5.1)}$$

where A*is effective Richardson constant of (GaN $\sim 26.4 Acm^{-2}K^{-2}$), q is The electron charge, T is temperature, ϕ_{Bn} is barrier height.

In the case of moderately doped semiconductors (10^{17} cm^{-3}~10^{20} cm^{-3}), a potential barrier at the interface of metal and semiconductor becomes thinner, and a part of electrons tunnel through it. The contact resistivity is determined by the barrier height and the doping level of the semiconductor. With highly doped semiconductors (>10^{20} cm^{-3}) and low temperatures, field electron emission is the main mechanism[109]. Electrons gain kinetic energy to emit from a metal surface due to the large E-field near the contact. Field emission is often called auto-electronic emission or cold-cathode emission because it can take place at low temperatures, even at room temperature.

In order to achieve good ohmic contact, common methods include highly doped semiconductor surface layers or the use of composite metals. For AlGaN/GaN ohmic contact, traditional Ti/Al multilayers, such as Ti/Al/W, Ti/Al/TiN, Ti/Al/Ti/TiN, etc., are often applied to gold-free ohmic contact processes. During the annealing process, Ti can effectively combine with N in AlGaN, thus leaving a large number of vacancies in AlGaN. Therefore, the electron concentration is increased and is conducive to the formation of low resistance ohmic contacts.

In addition, etching is one of the key factors affecting the ohmic contact performance of AlGaN/GaN ohmic contact. Improper etching depth may result in uneven shape or uneven surface of the contact area. This will reduce the effective area of the contact and affect the scattering and transport of electrons in the contact area. Meanwhile, the etching process may introduce oxides or other undesirable compounds on the AlGaN/GaN surface. These undesirable substances can reduce the electrical conductivity of ohmic contacts and cause an increase in contact resistance. In the factory, there is a time limit between etching and metal deposition, during which wafers are kept in nitrogen tanks to prevent oxidation

5.1.2 Contact properties for a PSJ HFETs

For PSJ HFET, the ohmic Drain/Source contributes to the on-state resistance and is a critical component. Investigation of ohmic contact property as the function of temperature can be helpful to analyze and construct the thermal analytical models of on-state resistance.

Figure 5.1.1 shows the schematic diagram of PSJ test chip (5mm*5mm) on Sapphire substrate made in POWDEC KK. It mainly consists of three PSJ test structures: PSJ Merged Schottky Barrier Diodes, PSJ FETs and pattern for Transmission Line Method (TLM) analysis.

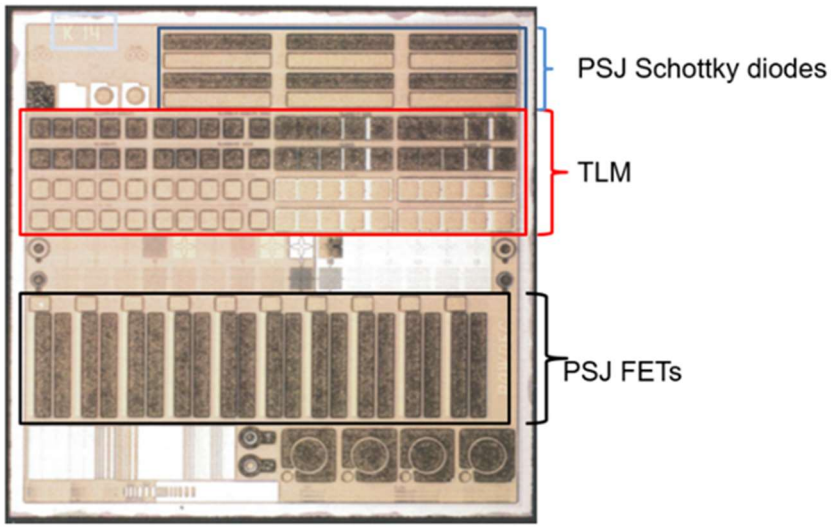
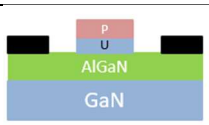
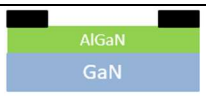
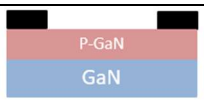


Figure 5.1.1: Schematic diagram of PSJ_FET test chip from POWDEC KK.

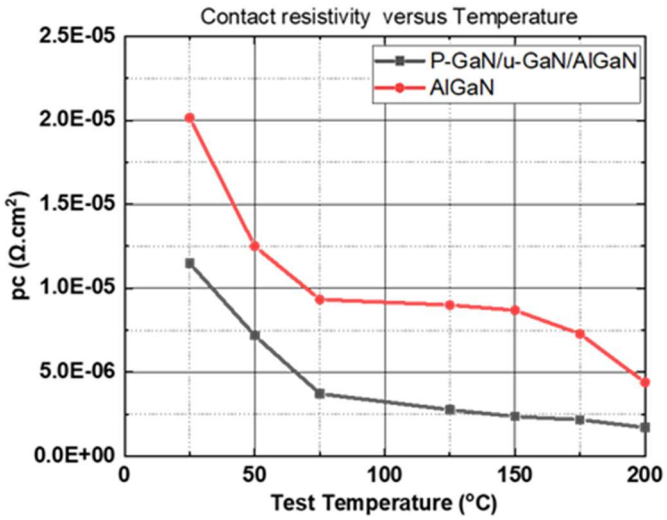
Due to the small ohmic contact resistance of the 200μm*200μm structure, it used the 4-point Probe Method to improve the accuracy of measurements. 2.5. By Transfer Length Method (TLM) introduced in Section 2.5.1, the properties of ohmic contacts for the specific structure can be measured and calculated. Table 5.1 shows the calculation results of ohmic contacts on five structures relative to the PSJ devices, such as contact resistivity R_c, the transfer length L_T and contact resistivity ρ_c. In can be found that the contact resistivity (ρ_c) for ohmic contact on P-GaN much higher.

Table 5.1: Properties of ohmic contacts of 5 test structures

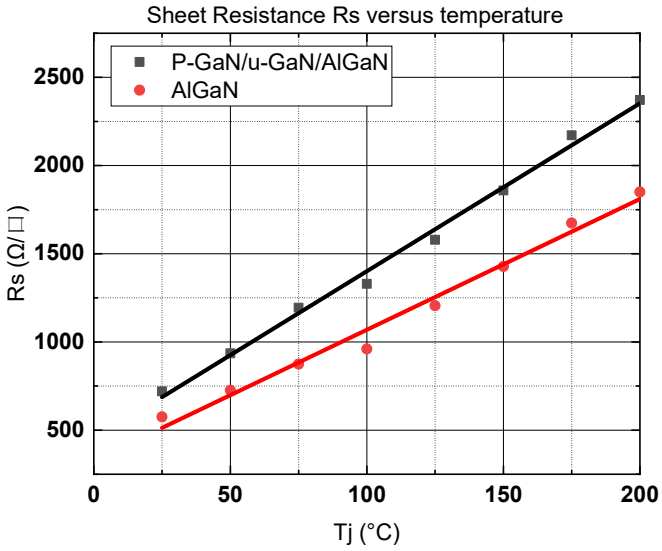
No.	Description	Structure	R_C (Ω)	L_T (μm)	ρ_c (Ω.cm^2)
1	P-GaN/U-GaN/AlGaN /GaN		4.117	1.175	9.68E-06
2	AlGaN/GaN		9.140	3.483	6.37E-05
3	SiO_2/AlGaN/GaN		5.914	2.317	2.74E-05
4	P-GaN /GaN		510.188	2.25375	0.0023

5	P-Each		254.669	2.486	0.0012

Among the five test structures in Table 5.1, properties of ohmic contacts on No.1 (P-GaN/u-GaN/AlGaN/GaN) and No.2 (AlGaN/GaN) as a function of temperature were studied and compared. The test temperature was 25,50,75,100,125,150,175 and 200ºC. Figure 5.1.2 shows the (a)contact resistivity and (b) sheet resistance of Structure No.1 (P-GaN/u-GaN/AlGaN) and No.2(AlGaN/GaN) versus the temperature.



(a)



(b)

Figure 5.1.2: The contact resistivity (a) and sheet resistance (b) of Structure No.1 (P-GaN/u-GaN/AlGaN) and No.2 (AlGaN/GaN) versus the temperature.

P-GaN/u-GaN/AlGaN is for basic PSJ structure while AlGaN/GaN is for conventional GaN HEMTs. From Figure 5.1.2(a), the contact resistivity of ohmic contacts for two structures shows a downward trend with the increasing temperature due to the thermionic emission. The trend At the same temperature, p-GaN/u-GaN/AlGaN/GaN has a smaller contact resistivity than that of AlGaN/GaN. For the sheet resistance, it shows the opposite trend. The sheet resistance of the two structures increases linearly with the rising temperature. At the higher temperature, the mobility of 2DEG reduces due to scattering which introduced in Section2.1.4 . In addition, the sheet resistance of P-GaN/u-GaN/AlGaN is higher than that of AlGaN because the presence of 2DHG in P-GaN/u-GaN/AlGaN reduces the electron density in the 2DEG channel. The contact resistivity is much smaller as components of the specific on-state resistance. Therefore, the resistance of the 2DEG channel determined the specific on-state resistance during the on-state period.

5.2 PSJ Merged Schottky Barrier Diode as the function of Temperature

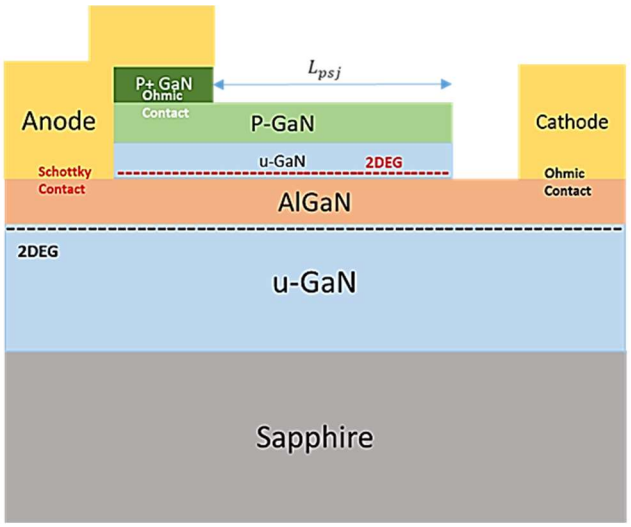


Figure 5.2.1: Cross-section of measured typical PSJ MSBD (Diode A) from POWDEC KK.

Figure 5.2.1 shows the cross-section schematics of measured PSJ Merged Schottky Barrier Diodes (MSBD) with Sapphire substrate from POWDEC KK. It consists of a p-type doped GaN cap layer (p-GaN) with 5×10^{19} cm^{-3} Mg-doped, a 50nm undoped GaN layer, a 47nm AlGaN layer with 23% Al composition and an 800nm u-GaN sub-layer. There are two electrodes named Anode and Cathode. An Anode electrode is usually made from Nickel (Ni) and Gold (Au). The anode electrode on GaN forms the Schottky contact to 2DEG, and the rest of the Anode electrode on P-GaN forms the Ohmic contact. The cathode electrode connected to AlGaN forms the ohmic contact.

The Schottky barrier diode (SBD) is a majority carrier device without conductivity modulation. Compared with PN diode, it has no reverse recovery, low knee voltage and low junction capacitance[110]. In 2014, it was the first time to report the performance and electrical characteristics of a 2.4KV PSJ Merged Schottky Barrier Diodes (MSBD) on 6H-SiC substrate[110].

When the positive voltage beyond the knee voltage is applied to Anode, electrons flow from the cathode to the anode through the 2DEG channel. The high electron mobility and high electron density in 2DEG reduce the on-state resistance. Under the reverse conditions, 2DEG and 2DHG are discharged through the Anode electrode on P-GaN and the cathode electrode, respectively. The drift region is fully depleted in the off-state, acting like the intrinsic region. As a result, the "box-like" field profile in the drift region of the PSJ Merged Schottky diode enhances its breakdown voltage.

There are three test structures of PSJ Merged Schottky didoes made in PWODEC KK, shown in Figure 5.2.2. The length of drift region L_{PSJ} is 15µm for PSJ Diode A and Diode B, while Diode C has 5µm-L_{PSJ}. In addition, both Diode B and Diode C employ Silicon Oxide (SiO_2) under Anode. Due to Diode A being the typical PSJ Schottky diode structure, it focuses on analyzing and studying PSJ Diode A as a function of temperature.

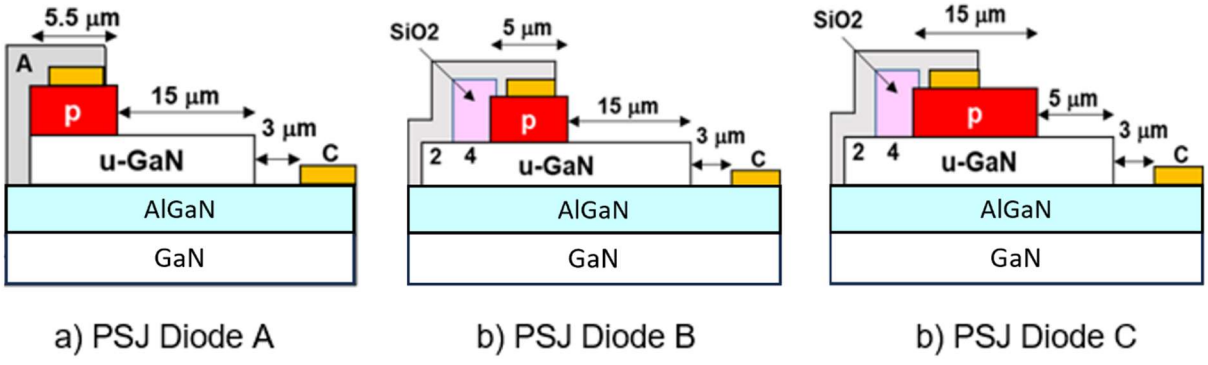


Figure 5.2.2: Schematics illustration of POWDEC PSJ Merged Schottky Barrier Diodes (MSBD) with Sapphire substrate.

Figure 5.2.3 shows the top view of PSJ Diode A under the microscope. The bright region is Anode made from Ni/Au, while the black area is Cathode made from Ti/Al. By measuring, the width of three PSJ Schottky diodes is 1mm and the distance from Anode to Cathode is 23.5µm, used to calculate active area for specific on-state resistance (Ron.A). The displacement of probes under the high temperature caused black scratches.

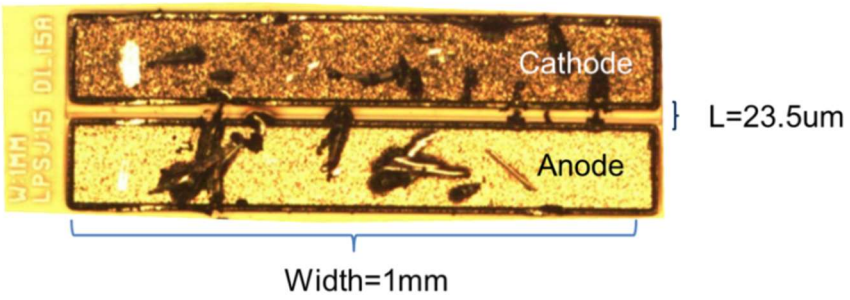


Figure 5.2.3: The picture of PSJ Schottky diode under the microscope

Forward IV characteristics measurements of three PSJ Merged Schottky diodes were undertaken within a temperature range between 25ºC and 200ºC. The measurement equipment is Agilent B1500 Analyser. During high-temperature measurements, the TEG PSJ chip was heated by a heating sheet and the test temperature was controlled by DC power supply (VOLTCRAFT PPS-1600s).

The 4-point Probe Method (Kevin Sensing) was utilized to eliminate errors caused by leads and probes for precise measurements of the low on-state resistances. The 4-point Probe Method employs two separate pairs of current-carrying and voltage-sensing electrodes. Each pair is connected to Anode and Cathode, respectively. It is usual to arrange the voltage-sensing (sense) wires as the inside pair while current-carrying (force) wires are the outside pair. According to Ohm's law, there is a voltage drop ΔV induced by wire impedances when the current is applied to current-carrying wires. Voltage-sensing wires inside do not include the voltage drop across the current-carrying leads or contacts. As a result, the accuracy of on-state resistance measurements was improved.

5.2.1 Forward IV characteristics

Figure 5.2.4(a)-(b) shows the forward IV characteristic of PSJ Schottky Diode A as a function of temperature. The test temperature was set from 25 to 200ºC with the step of 25ºC, with the applied Anode voltage increasing from 0V to 15V. It can be found that the Anode current decreases at a higher temperature. The main reason is that both electron saturation velocity and electron mobility in the 2DEG region is reduced at the higher temperature due to scattering effects, which leads to the incensement of on-state resistance.

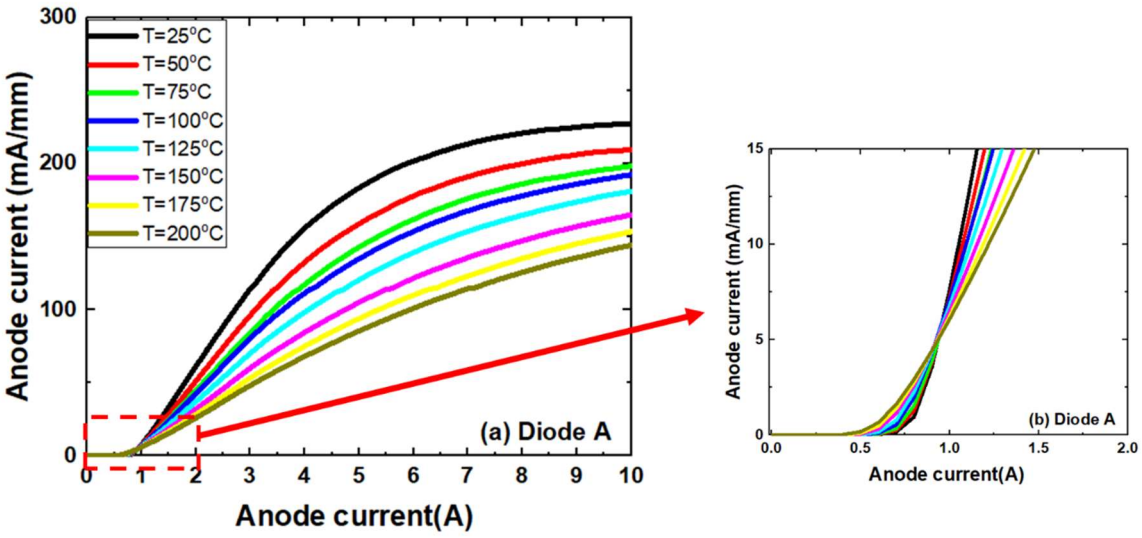


Figure 5.2.4: (a)Forward IV characteristic of PSJ MSBD (Diode A) with 15µm- L_{PSJ} as well as (b) knee voltage.

5.2.2 Knee voltage

The knee voltage is defined as the point where the current changes rapidly. Here, it is referred as the onset voltage at 1mA per 1mm-width from measured Forward IV characteristic of diodes. From Figure 5.2.4(b), it is obvious that the knee voltage goes up with increasing temperature. Figure 5.2.5 illustrates the knee voltage of three PSJ Schottky diodes. It can be found that the knee voltage is inversely proportional to the temperature.

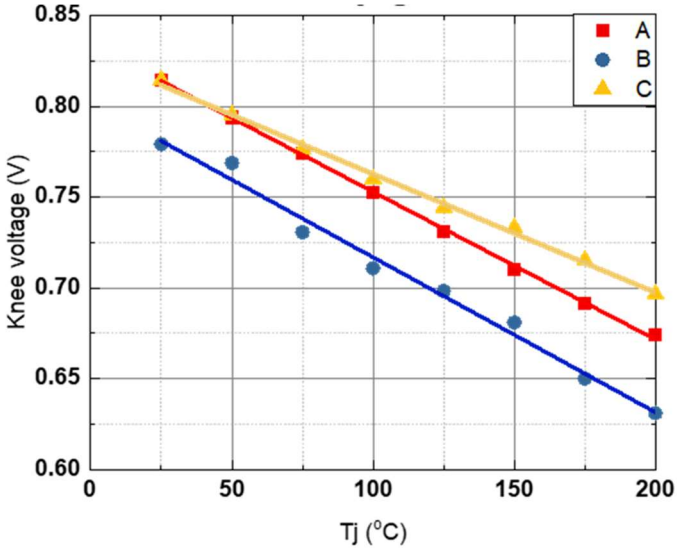


Figure 5.2.5: The knee voltage of three tes*t* structures of PSJ Schottky diodes.

The knee voltage is determined by the Schottky barrier height, which equals the difference in the Anode electrode's work function and the affinity of GaN in theory. The Schottky barrier height of

the anode decreases at a higher temperature. The effective Schottky Barrier Height was calculated according to Forward IV characteristics.

Effective Schottky Barrier Height

According to the thermionic emission theory, the relationship among the Anode current, the Schottky barrier height and the temperature is shown in the below Equation (5.2)[111] :

$$I = I_S\left(e^{\frac{-qV_1}{nKT}} - 1\right) \quad \text{--- (5.2)}$$

The saturation current is a function of the ambient temperature and its equation is shown in Equation (5.3)

$$I_s = AA^*T^2e^{\frac{-q\phi_{bn}}{KT}} \quad \text{--- (5.3)}$$

According to equation (5.1) and (5.2), the Schottky barrier height can be derivated and is shown in Equation (5.4)

$$\Phi_{bn} = \frac{KT}{q}\ln(\frac{AA^*T^2}{I_s}) \text{ --- (5.4)}$$

Where

A: The effective area of the Schottky diode

A*: is effective Richardson constant of GaN $\sim 26.4Acm^{-2}K^{-2}$

q: The electron charge

T: temperature

ϕ_{Bn}: Schottky barrier height (SBH)

n: The ideal parameter

From the graph of the Log of Anode current versus Anode voltage shown in Figure 5.2.6, the parameter I_s and n can be obtained. Using Equation (5.2), the effective SBH of three tests PSJ diodes are calculated at different test temperatures shown in Figure 5.2.7. At room temperature, the effective SBH of Diode A, Diode B and Diode C is 0.66eV, 0.83eV and 0.87eV, respectively. In theory, the work function of Ni Anode is 5.15eV and the electron affinity of GaN is 4.1eV. Therefore, the theoretical SBH is 1.04eV which is larger than the calculation results from the experiment data. The reason is that SBH on GaN does not exclusively depend on metal work function due to the interfacial

reaction between Ni and GaN. The formation of nickel nitrides Ni_3N and Ni_4N are formed at the interface of Ni and GaN when the specimen is annealing at a temperature above 200 ºC, which influences the effective SBH[111]. As shown in Figure 5.2.7, the effective SBH of 3 types of PSJ MSBDs shows a downward trend with increasing temperature. The majority carriers achieve the energy to jump over the potential Schottky barrier more easily at high temperatures, which leads to the smaller knee voltage. The differences in structures of PSJ Schottky diodes influence the rate at which the Schottky Barrier Height falls.

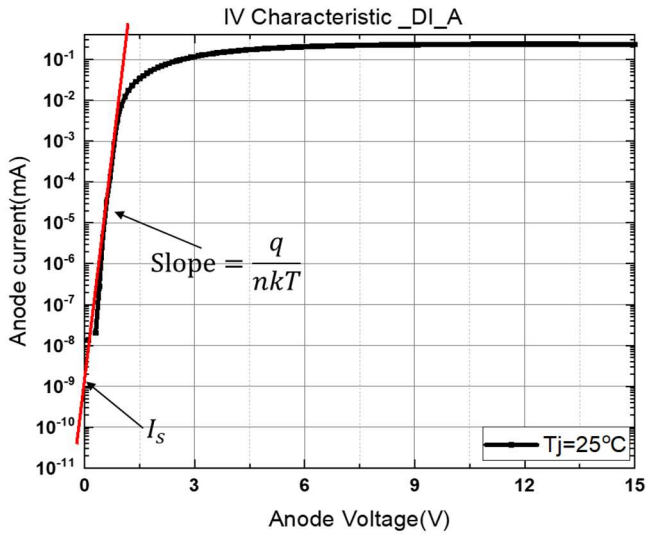


Figure 5.2.6: Log of Anode current versus Anode voltage of Diode A.

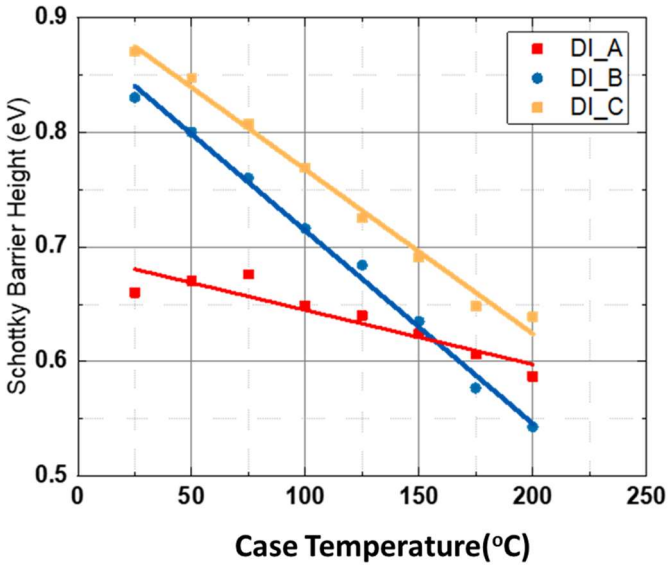


Figure 5.2.7: Effective Barrier Height of 3 PSJ Merged Schottky Diodes versus temperature.

5.2.3 The specific on-state resistance

The specific on-state resistance (Ron. A) is a significant index to evaluate the performance of power-switching devices. The low specific on-state resistance means low switching losses and small power dissipation. Illustrated in Figure 5.2.8, Ron.A is $5.8m\Omega/cm^2$ for testing PSJ PSJ MSBD (Diode A) with the L_{PSJ} of 15µm at room temperature. When the temperature goes up, the specific on-state resistance increases.

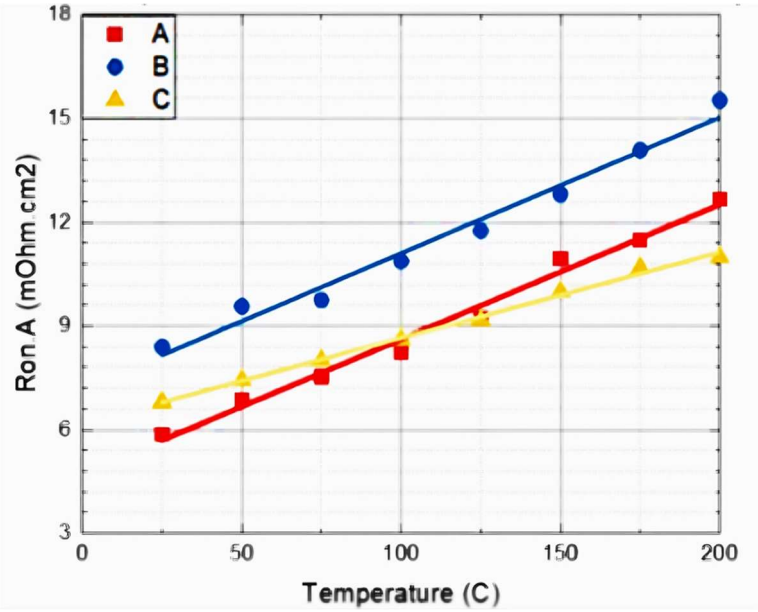


Figure 5.2.8: The specific on-state resistance of three test PSJ Schottky diode structures

5.3 PSJ HFETs as the function of Temperature

Figure 5.3.1 shows the top view of the PSJ OG HFET under the microscope. The width (Wg) of PSJ FETs is 1mm and the distance from Source to Drain (L_{DS}) equals (37+L_{PSJ}) µm. The length of PSJ alters from 5 to 40µm for PSJ FETs. Agilent B1500 Analyser is employed to measure the on-state performance of heating test structure PSJ FETs. It used three probes connected to Source, Drain and Gate Electrode.

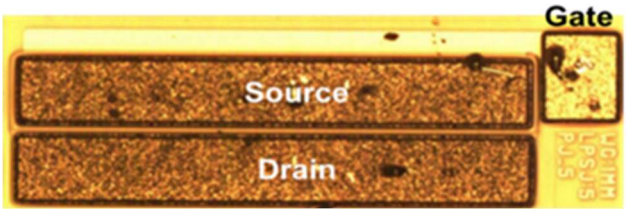


Figure 5.3.1: The picture of the measured PSJ FET under the microscope with 1mm width.

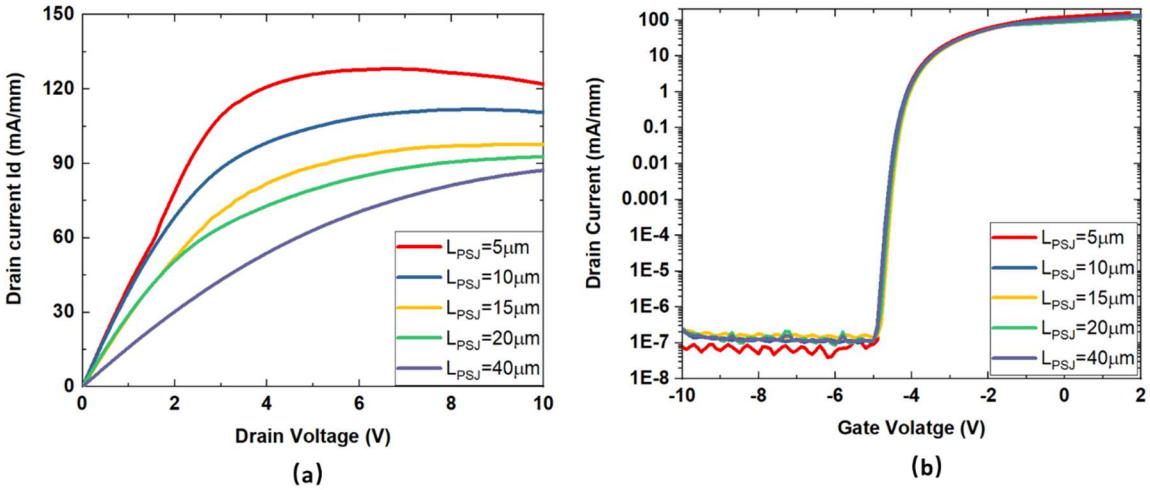


Figure 5.3.2: Measured (a)intput Id -Vd characteristics and (b) output Id-Vg characteristics of Ohmic Gate PSJ HFETs at V g = 0V.

Measured intput Id -Vd characteristics and output Id-Vg characteristics of Ohmic Gate PSJ HFETs at V g = 0V is presented in Figure 5.3.2. the threshold voltage of OG PSJ HFETs is around -4.6V. With the increase of L_{PSJ} , the output drain current decreases as well as increasing Ron.A increases due to the resistance of PSJ region is proportional to the PSJ length.

Figure 5.3.3 shows forward I-V characteristics of the PSJ FET with L_{PSJ} of 5μm as a function of Temperature. The heating equipment is the heating sheet and VOLTCRAFT PPS-1600s. The test temperature of PSJ FET increased from 25°C to 200°C. The Gate voltage of 0V is applied while the Drain voltage rises from 0 to 10V. There is a downward trend of Drain current I_{DS} due to the degradation of electron mobility and the higher scattering rate is higher when the temperature is higher. During saturation region, the Drain current decreases slightly because of the self-healing.

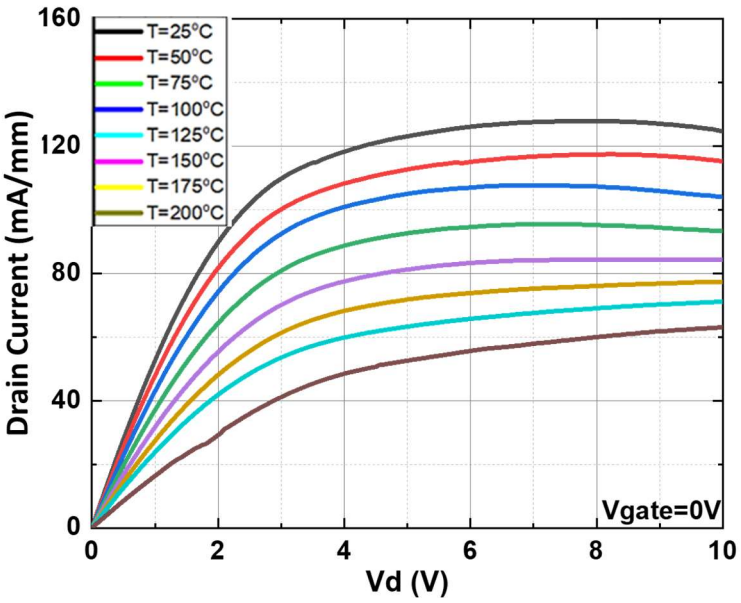


Figure 5.3.3: Temperature dependent Forward IV characteristics of the PSJ FET with 5µm L_{PSJ} at V g =0V.

Figure 5.3.4 shows the specific on-state resistance of PSJ FETs versus temperature. It is evident that there is a linear relationship between the specific on-state resistances. Figure 5.3.5 illustrates the trend of the specific on-state resistance changes with the drift region of L_{PSJ}. With the increasing L_{PSJ} , the temperature affects on Ron.A is more obviously. At the high temperature, The relationship between resistance and length changes from approximately linear to square.

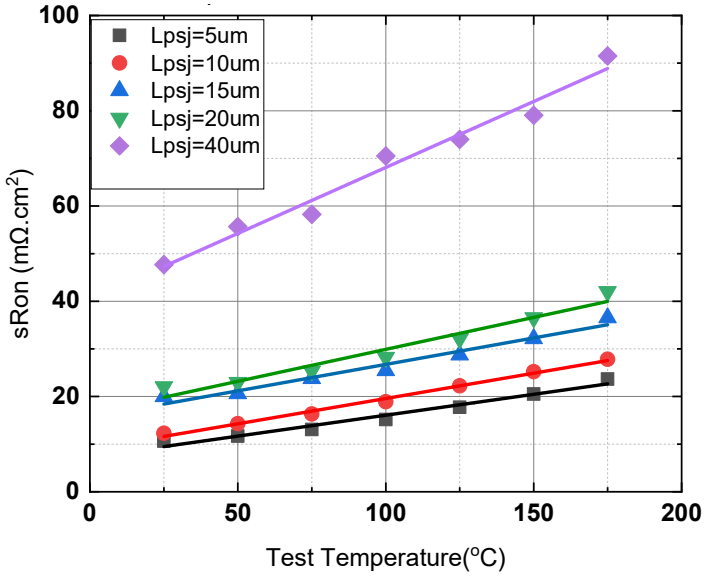


Figure 5.3.4: Specific on-state resistance of TEG FETs with L_{PSJ}=5,10,15,20 and 40µm versus Temperature.

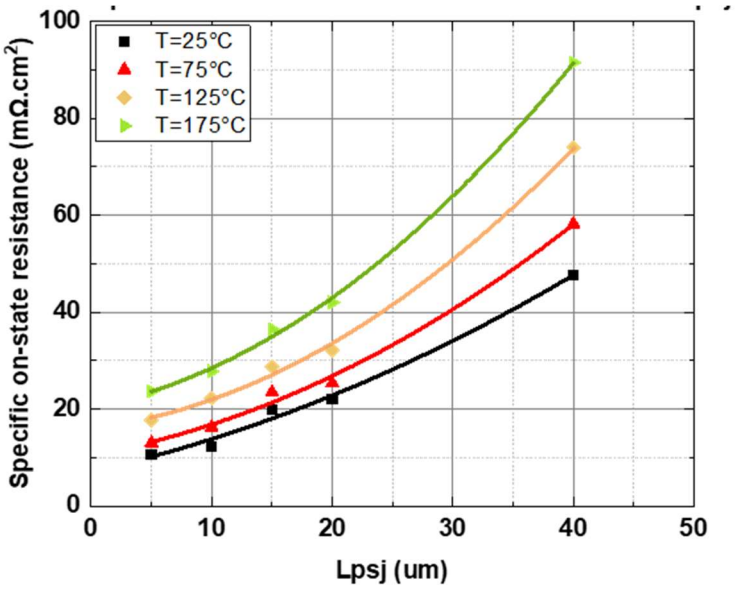


Figure 5.3.5: Specific on-state resistance of PSJ FETs versus L_{PSJ} at 25,75,125 and 175°C.

5.4 Summary

In this chapter, the discussion commenced with resistivity for ohmic contact, contributing to the on-state resistance, at temperatures ranging from room temperature to 200 ° C. Then, it evaluates the on-state I-V characteristics of the PSJ Merged Schottky Barrier Diode and PSJ HFETs as the function of temperature. The trends of specific on-state resistance of PSJ samples with increasing temperature are calculated and presented. These results are critical for thermal analytical models of Ron.A and further improvement of on-state performance for PSJ devices.

Chapter 6: Metalization interconnect Layouts for large-area PSJ device

A large-area lateral field transistor essentially is a parallel combination of many individual device cells to achieve the desired current rating by the metal interconnect. There is a trend towards increasing the number of cells per unit area to decrease the size of individual cells. Nonetheless, there is a difficulty in ensuring that appropriate cells function normally by preventing current hogging or even breakdown. Among them, Parasitic impedances (R, L&C) induced by interconnect significantly influence on-state resistance, switching speed, propagation and phase delays. It is necessary to reduce and allocate parasitic impedance reasonably for achieving a uniform current and temperature distribution as well as reducing the oscillatory behaviour when switching. This chapter will introduce

the effects of parasitic impedance on the device's performance. Different layout designs for 1A large-area three-terminal devices are proposed. The simulated parasitic resistance and impedance of layouts is extracted and compared as well as the impedance distribution by Software Ansys Q3D.

6.1 Effects of the interconnect parasitic impedance

Figure 6.1.1 shows the equivalent circuit diagram of a GaN device with four paralleled cells. L(L_G, Ls and L_D), R(R_G, R_S and R_D) and C(C_G, C_S and C_D) are effective interconnection parasitic Inductance, Resistance and Capacitance of Gate, Source and Drain, respectively.

Time delay is one of the challenges induced by parasitic impedance. As the input signal applied to the Gate pad changes, there are propagation delays in the voltage response to individual cells due to parasitic gate impedance. Besides interconnect impedance, this gate delay relies on the distance to the gate pad. During switching on/off, time delays in voltage response cause the non-uniform distributed instantaneous impedance between the drain and source of cells. Then it causes current hogging, uneven temperature distribution and additional conduction losses. When the device is in repeated switching operations or under short-circuit fault conditions, the increasing temperature and uneven current over the active area may degrade or potentially damage the device's performance.[112].

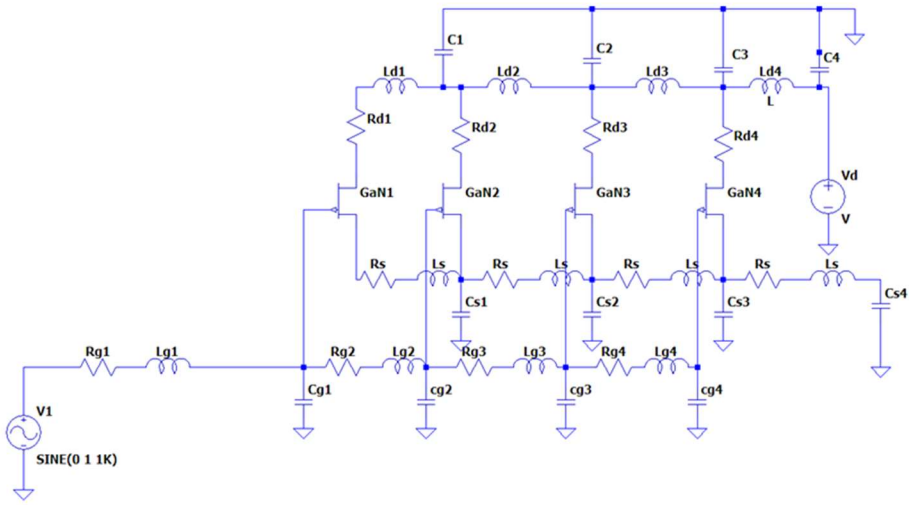


Figure 6.1.1: Simple RC tree for GaN devices with four paralleled cells.

In 1948, the Elmore delay was proposed to estimate the worst-case propagation delays of interconnect RC networks. Propagation Delay at the node 'N' can be calculated using Equation (6.1) below[113]:

$$\text{Propagation Delay} = R_{ns}C_n \text{------(6.1)}$$

where R_{ns} is the shared resistance along the path and $C_n$is the capacitance on the node N.

However, Equation(6.1) for time delay calculation does not consider the impact of parasitic inductance. In high-speed switching operation or the interconnection of parallel devices is longer, parasitic inductance becomes more significant. Therefore, in these case it is necessary to construct a more accurate interconnection model[114].

Previous research has proven that parasitic inductance from interconnect influences the voltage/current overshoot, switching time and conduction loss. During high-speed switching operation, the change rate of the drain current (di/dt) and the stray parasitic inductances of the metal track leads to the voltage surge across the drain and the source, which can be expressed by :

$$\Delta V = L\frac{di}{dt} \text{------(6.2)}$$

In the off-transient state, the direction of the induced electromotive force is the same as the direction of the bus voltage, which is superimposed on the drain-source voltage of the switch, resulting in a voltage spike and ringings,which leads to electromagnetic interference issues, false switch-on, or even device failure([115],[116]). Because high switching speed, tiny driving safety margin, low threshold voltage, GaN HEMTs are extremely sensitive to parasitic inductance[117].

The parasitic drain inductance causes the oscillation in V_{gs} and Drain current (I_d) since the surge voltage resonates with the output capacitance $C_{iss}(= C_{gd} + C_{ds})$ and parasitic inductance L_D. The larger the inductance, the more pronounced the oscillation [115].

The parasitic source inductance (L_S) is induced by the di/dt of the drain current during turn-off and the stray inductance of the source metal track. L_s causes the oscillation in the waveform of the driving voltage (V_{gs}). A large ringing voltage on the gate voltage might cause the device to turn on and off repeatedly, thus leading to oscillation([115],[118]). In addition, L_S slows down the switching speed. In[115], it proves that L_S has an obvious effect and causes a significant delay in the turn-on and turn-off times.

The parasitic gate inductance (L_G) causes ringing of the gate voltage V_{gs} when it resonant with the input capacitance $C_{iss}(= C_{gs} + C_{gd})$. The smaller L_G can avoid the large spikes in V_{gs} and the shoot-through due to the false trigger during the turn-off[119].

The parasitic capacitance between closely spaced metal tracks will increase the capacitive loading on driven nodes and cause the crosstalk.

6.1.1 Effects of gate parasitic resistance on static IV curves

Large-area PSJ HFETs usually employ the multi-finger Drain-Source layout described in Figure 3.3.2. There are two current paths from two gate pads to each gate finger to ensure the uniform gate current through each gate finger and reduce the difference in Gate impedance. To investigate the influence of gate parasitic resistance on the static electrical characteristics, it compares the static current-voltage characteristics of 1A and 2A PSJ HFETs with 40µm-L_{PSJ} by applying the gate voltage to one gate pad and two gate pads. Figure 6.1.2 shows the top view of 1A and 2A unidirectional PSJ HFETs. The effective Gate/Drain/Source fingers of 2A PSJ devices are double those of 1A PSJ HFETs.

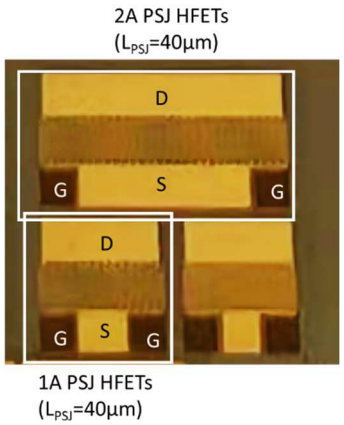


Figure 6.1.2: The top view of 1A and 2A fabricated unidirectional PSJ HFETs.

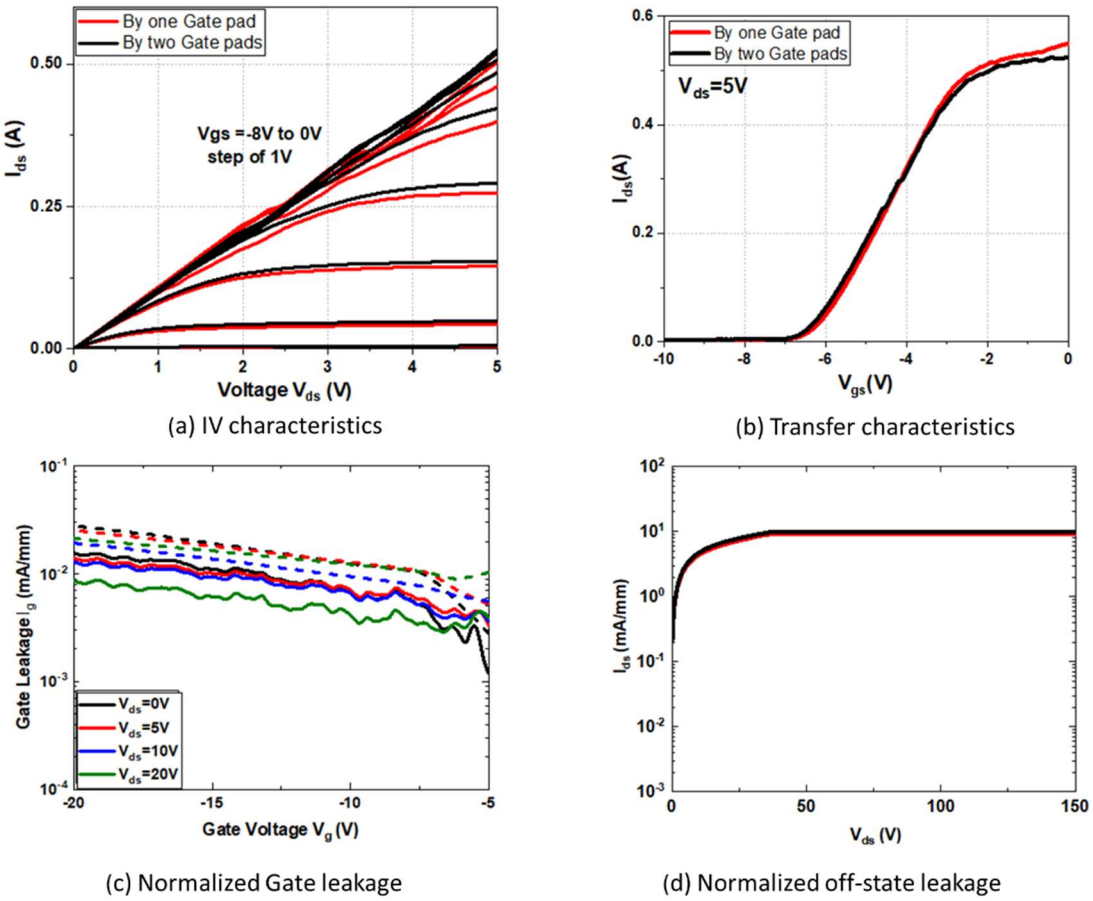


Figure 6.1.3: The static current-voltage characteristics of 1A PSJ HFETs with 40µm-L_{PSJ} by applying the voltage to one gate and two gate pads.

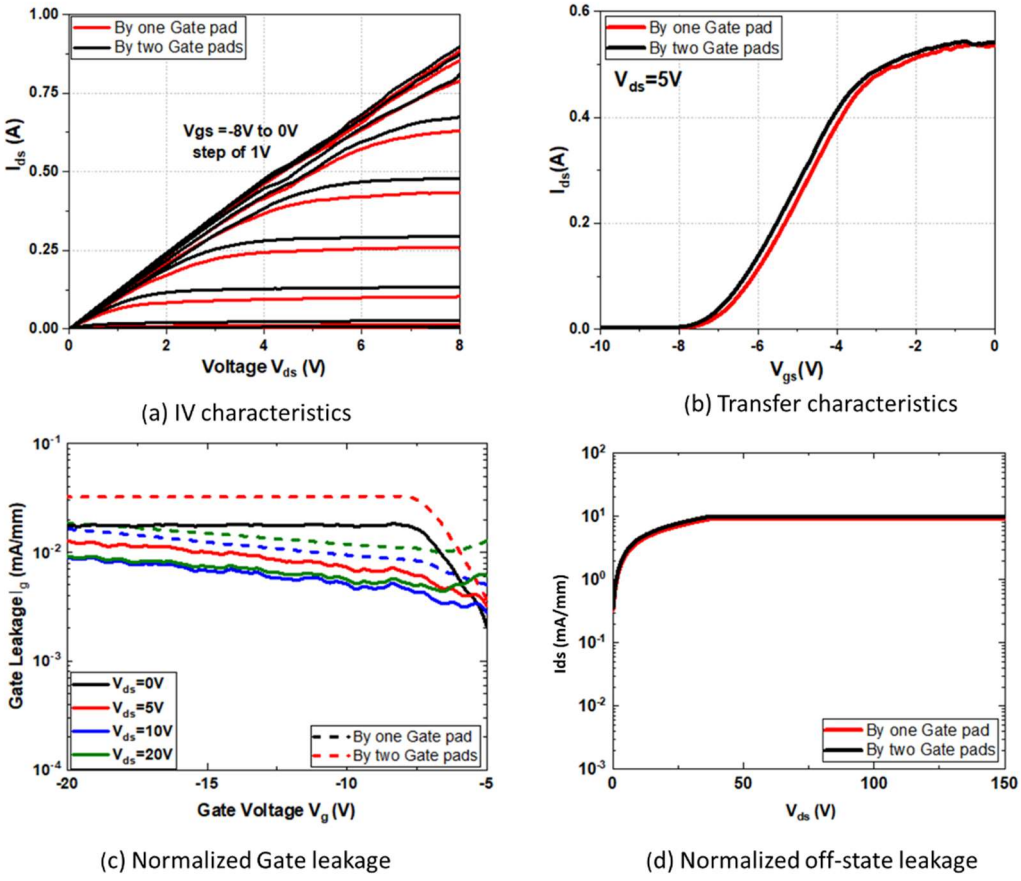


Figure 6.1.4: The static current-voltage characteristics of 2A PSJ HFETs with 40µm-L_{PSJ} by applying the voltage to one gate and two gate pads.

Figure 6.1.3 and Figure 6.1.4 present (a)I_d-V_d characteristics, (b)transfer characteristics, (c)normalized Gate leakage and (d)Normalized off-state leakage of 1A PSJ HFET and 2A PSJ HFET with 40µm-L_{PSJ}, respectively. In these Figures, black lines (Solid lines for normalized Gate leakage) stand for results obtained by applying Gate Voltage to two gate pads, while red lines (Dashed lines for normalized Gate leakage) are the results of applying voltage to one Gate pad. As the number of gate fingers increases, the difference in I_d-V_d curves and gate leakage obtained by the two test methods becomes more apparent. The large gate finger impedance reduces the on-state current, especially in the saturation region. In addition, it raises gate leakage.

Figure 6.1.5 shows the specific on-state resistance vs breakdown voltage of PSJ-FETs on Sapphire. There is a gap between the specific on-state resistance between the large-area PSJ FETs (Red) and device test structure FETs (Blue). For the same breakdown voltage, specific on-state resistance Ron.A of large-area PSJ FETs is more significant than that of TEG FETs. Presently, the devices made are limited to 10 A. In order to increase the current rating of the devices to much larger

values, It is necessary to optimize the layout designs in order to reduce and allocate parasitic impedance reasonably.

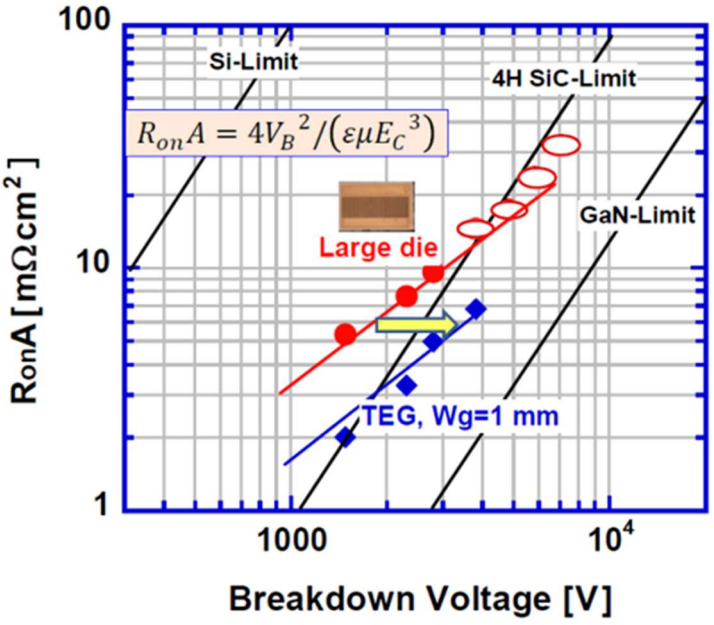


Figure 6.1.5: R_{on}.A versus breakdown voltage of fabricated large area and test structure PSJ-FETs on Sapphire.

6.2 Layout design rules

It is known that parasitic impedance from interconnect degrades device performance with an increase of the switching frequency. In order to achieve uniform current and temperature distribution and reduce oscillating behaviour when switching, it is necessary to reasonably reduce and distribute parasitic impedance, which can be improved by interconnect layout.

In this work, it designs five layouts of metal interconnect to compare the parasitic resistance, such as Multi-finger Drain-Source(DS) Layout, Multi-finger Drain-Source-Drain(D-S-D) Layout, Multi-finger Source-Drain-Source Layout (S-D-S), Checkerboard and the hexagonal-shaped layout.

To compare layout impedance, layout designs for metal interconnect are designed for 1A PSJ HFETs. The gate finger/path width for different layouts is set as the same as 4μm. The distance between electrodes and electrodes' thickness is 21.5μm based on that in PSJ OG HFETs with 10μm.

Drain-Source Current density (normalised to Gate width) is estimated as 50 mA/mm at V_{DS} = 1 V. Parasitic capacitance depends on the metal/electrode thickness, which keeps the same for different layouts. Therefore, it focuses on parasitic resistance and inductance from metal interconnect.

According to Equation (3.1), the effective gate length can be calculated by:

$$\text{The effective gate length } = \frac{Current\ rating(A)}{normalised\ current\ density\ (mA/mm)} = \frac{1A}{50mA/mm} = 20mm$$

The minimum number of cells in parallel can be deduced by the effective gate length, which stands for the effective finger length for multi-finger or the perimeter for one cell in Checkerboard and a hexagonal-shaped layout

$$\text{The total cells} = \frac{The\ effective\ gate\ Lengt\ \ (mm)}{Finger\ length(mm)} \text{ ------(6.3)}$$

The minimum side length of the liner design is 250μm to ensure that the area is large enough for wedge bonding or ball bonding.

Inescapable in layout designs, the source/drain metal layers will overlap the gate track, the air bridge and the insulation layer are utilized to keep the isolation of the gate and source metal layers. As the example of a multi-finger DS layout shown in Figure 6.2.1, the purple area is the isolation layer. Drain/Source fingers are on the isolation layer and viva it to connect the devices while the gate track is under isolation.

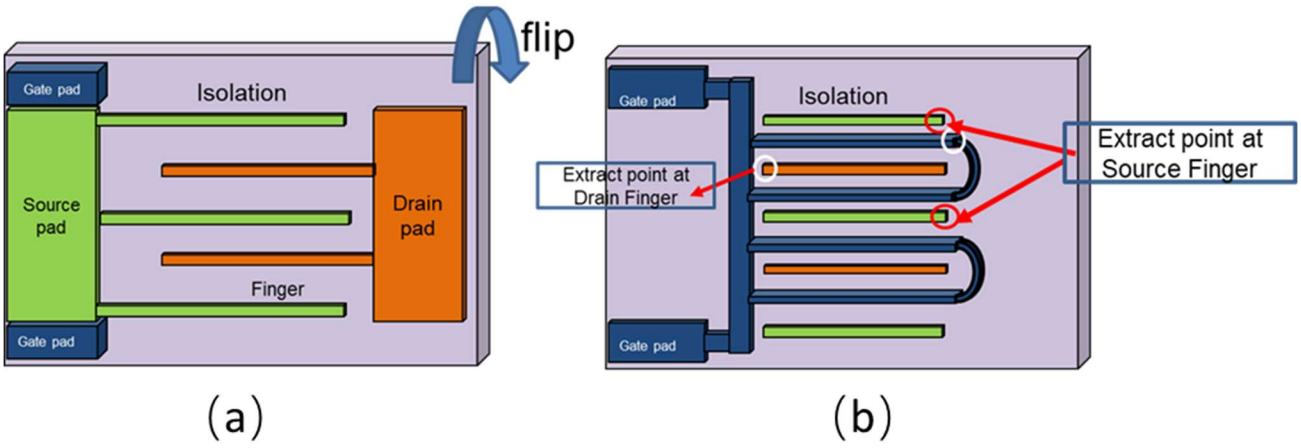


Figure 6.2.1: (a) Top view of simply multi-finger DS layout and (b) the view of the layout after flipping.

6.3 Simulation settings

The simulated impedance with the distribution of five layout designs is extracted and analyzed by the Software Ansys Q3D. The 3D metallization layouts were built and the metallization material was set as Gold. The thickness of the all-metal tracks/finger is set as 0.26μm, similar to the deposited Drain/Source metal track in fabricated PSJ OG HFETs.

For gate impedance extraction, 1V voltage with desired frequency is applied to gate pads, and the impedance can be extracted at selected points shown in Figure 6.2.1(b).

For drain/source impedance extraction, a conductive channel with perfect conductivity as a 2DEG channel between the Source and Drain to eliminate the effects of 2DEG sheet resistance. Apply 1V drain voltage to calculate the total Source/ Drain at a 100K Hz frequency.

6.4 Layout schemes

6.4.1 Multi-finger Drain-Source Layout

Figure 6.4.1 is the top view of a typical multi-finger Source-Drain layout. Two Gate Pads and a Source Pad are employed on one side of the device, while the Drain Pad is on the other side. Metal layers connect the Gate, Source, Drain Pad to corresponding electrodes in the active area of the device. Blue stands for the gate pads, path and fingers. Orange is for Drain, and Green is for Source. Current PSJ devices are mainly based on multi-finger layout designs, strongly dependent on the metallization flatness and the insulator layer quality in designing large-area devices. Finger resistance is essential to the manufacture and performance of devices. One issue with this traditional configuration is that in order to attain a higher current rating, the length and number of the source and drain fingers have to be increased, which adds parasitic impedance losses.

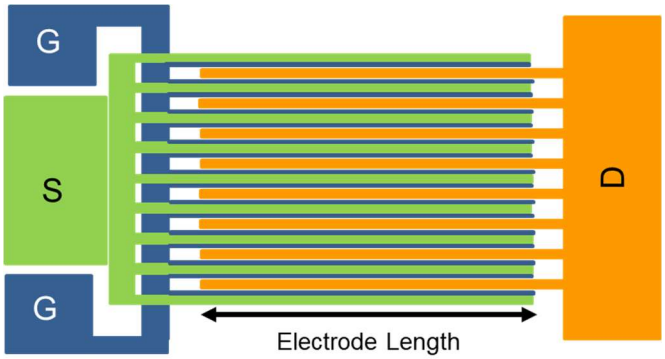


Figure 6.4.1: Schematic of D-S Layout.

In the simulation, the effective finger length (L) for Multi-finger D-S Layout is 1500μm. The finger width for Drain/Source is 30μm while for Gate is 4μm. The minimum cell number to achieve 1A device equals by :

$$\text{The total cells(N)}=\frac{The\ effective\ gate\ Lengt\quad (mm)}{L}=\frac{20}{1.5}\approx 14 \text{------(6.2)}$$

Due to 1 Gate electrode for one cell and each Drain/Source electrode shared by two cells, The figure number of Source and Drain can be calculated by:

The Gate finger number= 14

The Source finger number = 8

The Drain finger number =7

The top view of the 3D Multi-finger D-S Layout in ANSYS is shown in Figure 6.4.2, as well as extracted Parasitic resistance and inductance at 100kHz in Table 6.1. The insulation layer utilized to keep the isolation of the gate and source metal layers is hidden.

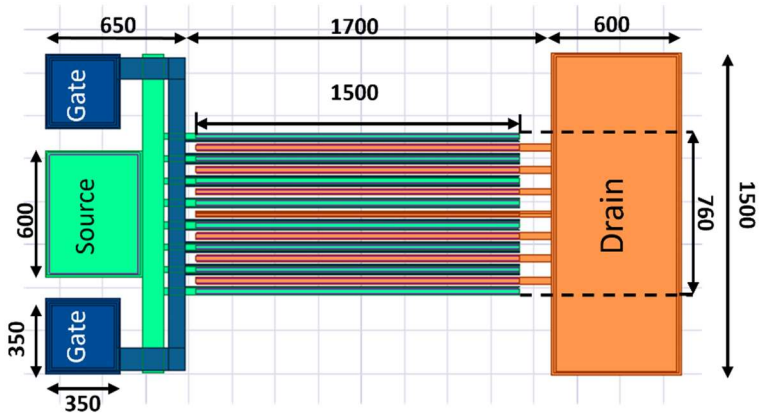


Figure 6.4.2: Top view of simulated 3D D-S layout. Dimension in µm. (Isolation layer is hidden)

Table 6.1: Extracted parasitic resistance and inductance for D-S Layout in ANSYS.

Layouts	Finger	Resistance (mΩ)	Inductance(pH)@100Khz	Active Region(mm^2)
DS Multi-finger layout	Drain	2.36	23.23	1.14 (=1500um*760mm)
	Source	2.6	41.8	

6.4.2 Multi-finger Source-Drain-Source Layout

Figure 6.4.3 is the top view of a Multi-finger S-D-S Layout. Compared with the Multi-finger D-S Layout, it has half the finger length but twice the number of fingers, thus maintaining the equivalent gate width. It can be seen as the two back-to-back D-S layouts sharing one Drain pad, as well as using a metalization track to connect source pads on both sides. Table 6.2 shows the width, length and number of gate, source and drain fingers.

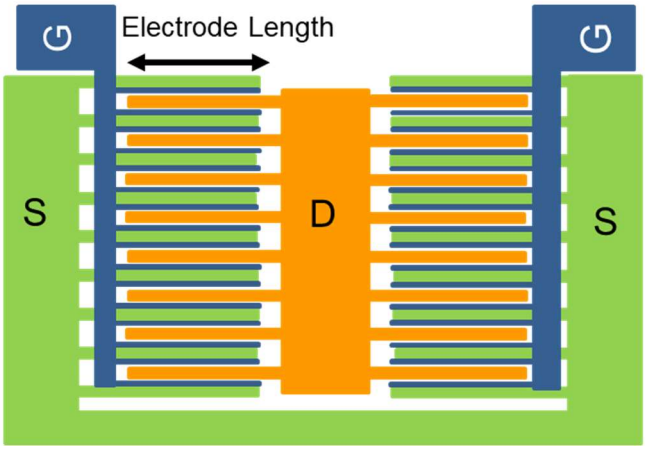


Figure 6.4.3: Schematic of S-D-S Layout.

Table 6.2: Parameter of Multi-finger S-D-S Layout for 1A PSJ HFET

	Width(μm)	Length(μm)	Finger Number
Source electrode	30	750	14
Drain electrode	30	750	15
Gate/Drain/Source path	4/8/8	750	28

The top view of the 3D SDS Layout in ANSYS is shown in Figure 6.4.4, as well as extracted parasitic resistance and inductance of drain and Source at 100kHz in Table 6.3.

Compared with the D-S layout, the S-D-S design reduces the parasitic resistance of the drain and Source due to the shorter finger length. The simulation also compares parasitic impedance when applying the input to one Source pad on the left and two Source pads on each side. It can be found that there is an additional inductance when only one source pad is employed due to the source connection track.

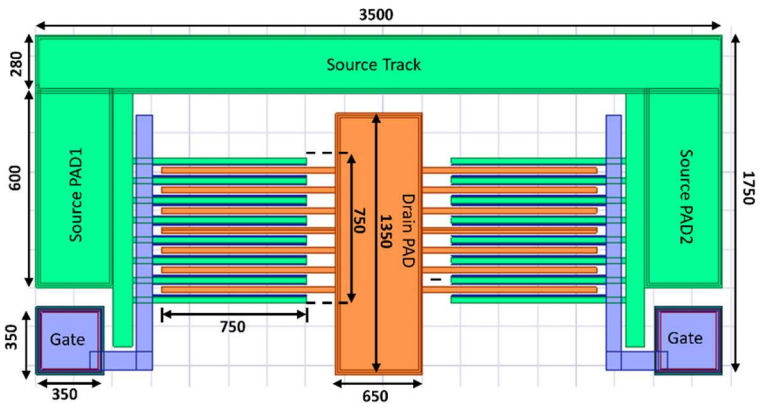


Figure 6.4.4: Top view of simulated 3D S-D-S layout. Dimension in μm. (Isolation layer is hidden)

Table 6.3: Extracted parasitic resistance and inductance for S-D-S Layout in ANSYS.

SDS layout	Resistance (mΩ)	Inductance(pH)@100Khz	Active Region(mm^2)
Drain	1.02	7.85	1.12 (=2*750um*750mm)
Source	0.96 (Employing Source Pad1 and Pad2)	9.24 (Employing Source Pad1 and Pad2)	
	1.82 (Employing Source Pad1)	26.31 (Employing Source Pad1)	

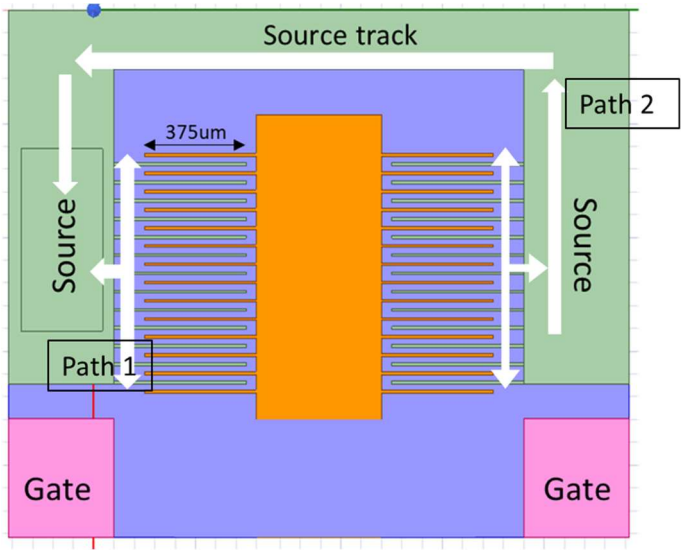


Figure 6.4.5: The top view of simulated 3D S-D-S Layout with one Source pad.

To study the distribution of parasitic impedance, the 3D model for S-D-D layout with the 375um finger length is built and shown Figure 6.4.5. The number of finger for Source/Dain/Gate is double to30/28/56. When employing the Source Pad1 on the left, half the device fingers on the right have a higher inductive path to the source pad than those on the left area due to the additional source inductance arising from the source track connection. The further distance from Pad1, the higher inductance of the source finger in the right area, as shown in Figure 6.4.6. This phenomenon leads to unbalanced common source inductance(CSI), which causes oscillatory behaviour when switching.

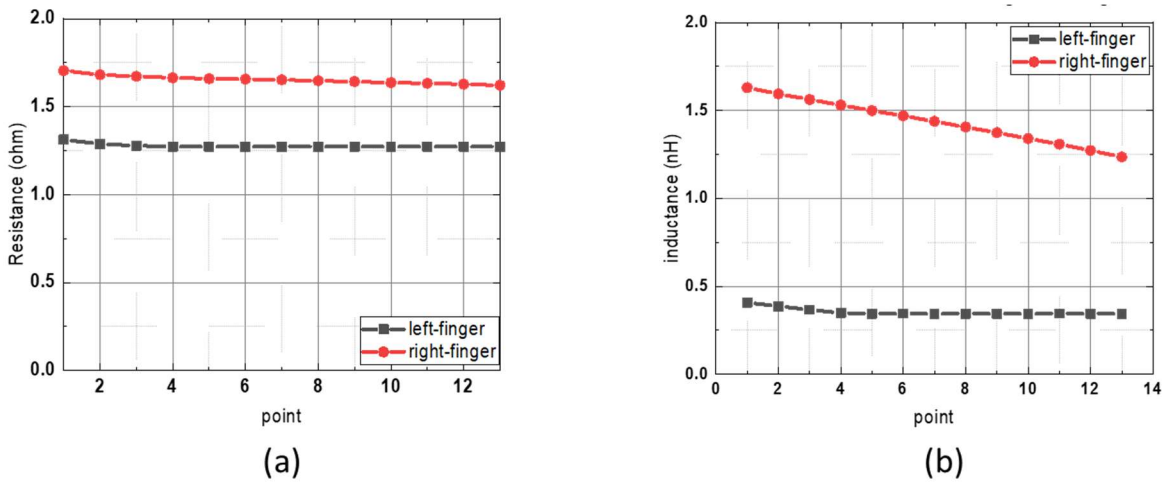


Figure 6.4.6: Simulated parasitic (a) resistance and (b) inductance of each source finger when employing one Source pad (Pad 1)

6.4.3 Multi-finger Drain-Source-Drain Layout

Figure 6.4.7 is the top view of a Multi-finger D-S-D Layout and Table 6.4 shows relative parameters of electrodes for a Multi-finger D-S-D Layout. It is similar to the S-D-S layout but shares the source pad in the middle and uses a metalization tarck to connect Drian pads on two sides.

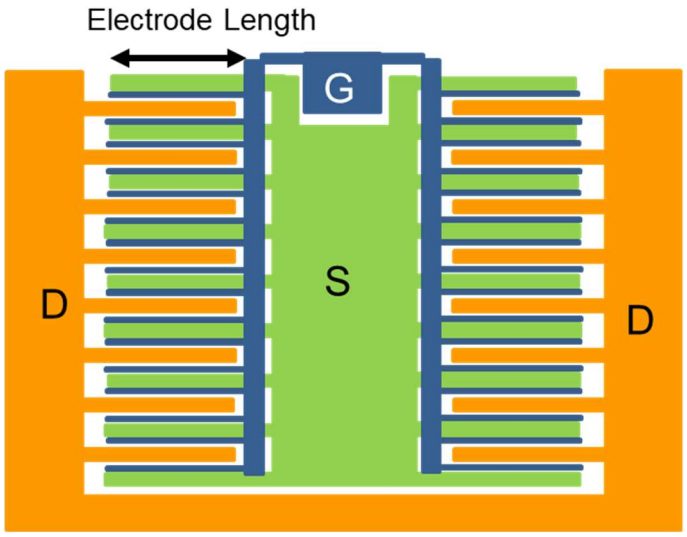


Figure 6.4.7： Schmatical of D-S-D Layout of 1A devices.

Table 6.4: Prameter of Multi-finger D-S-D Layout for 1A PSJ HFET

	Width(μm)	Length(μm)	Finger Number
Source electrode	30	750	15
Drain electrode	30	750	14
Gate/Drain/Source path	4/8/8	750	28

The top view of the 3D SDS Layout model in ANSYS Q3D is shown in Figure 6.4.8 and extracted parasitic resistance and inductance of drain and Source at 100kHz in Table 6.5. Similar to the S-D-S layout, it has a smaller parasitic impedance than the D-S layout due to shorter finger length. However, the additional Drain track leads to the unlanced Drain parasitic inductance when applying input signals to the Drain Pad only on one side.

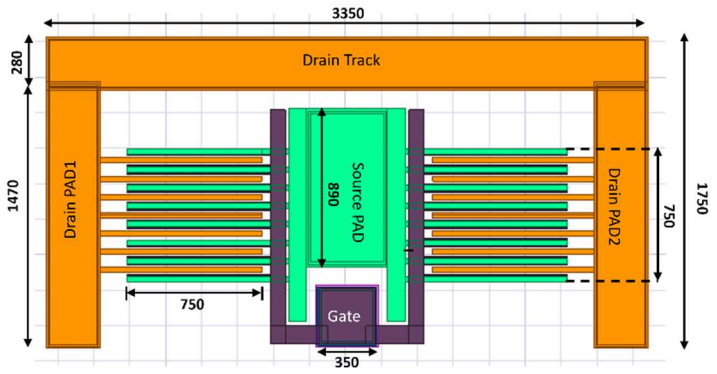


Figure 6.4.8: Top view of simulated 3D D-S-D layout. Dimension in µm. (Isolation layer is hidden)

Table 6.5: Extracted parasitic resistance and inductance for D-S-D Layout.

DSD layout	Resistance (mΩ)	Inductance(pH)@100Khz	Active Region(mm^2)
Drain	1 (Employing Drain Pad1 and Pad2)	8.74 (Employing Drain Pad1 and Pad2)	1.12 (=2*750um*750mm)
	1.88 (Employing Drain Pad1)	24.6 (Employing Drain Pad1)	
Source	1.11	15.42	

Figure 6.4.9 (a)-(b) presents each Drain finger's parasitic resistance and inductance for 3D model with 375um finger width when applying 1V voltage to the drain pad on the right. The extracted points from top to bottom are labelled '1' to '14' shown in Figure 6.4.9 (c). The Extremes min/max Δ =0.33Ω and 1.27nH for parasitic resistance and inductance, respectively. The differences in Drain parasitic impedance due to the additional connection track will cause differential drain-to-source voltages during the transition and, therefore, differences in transition energy. In addition, it affects the current balance.

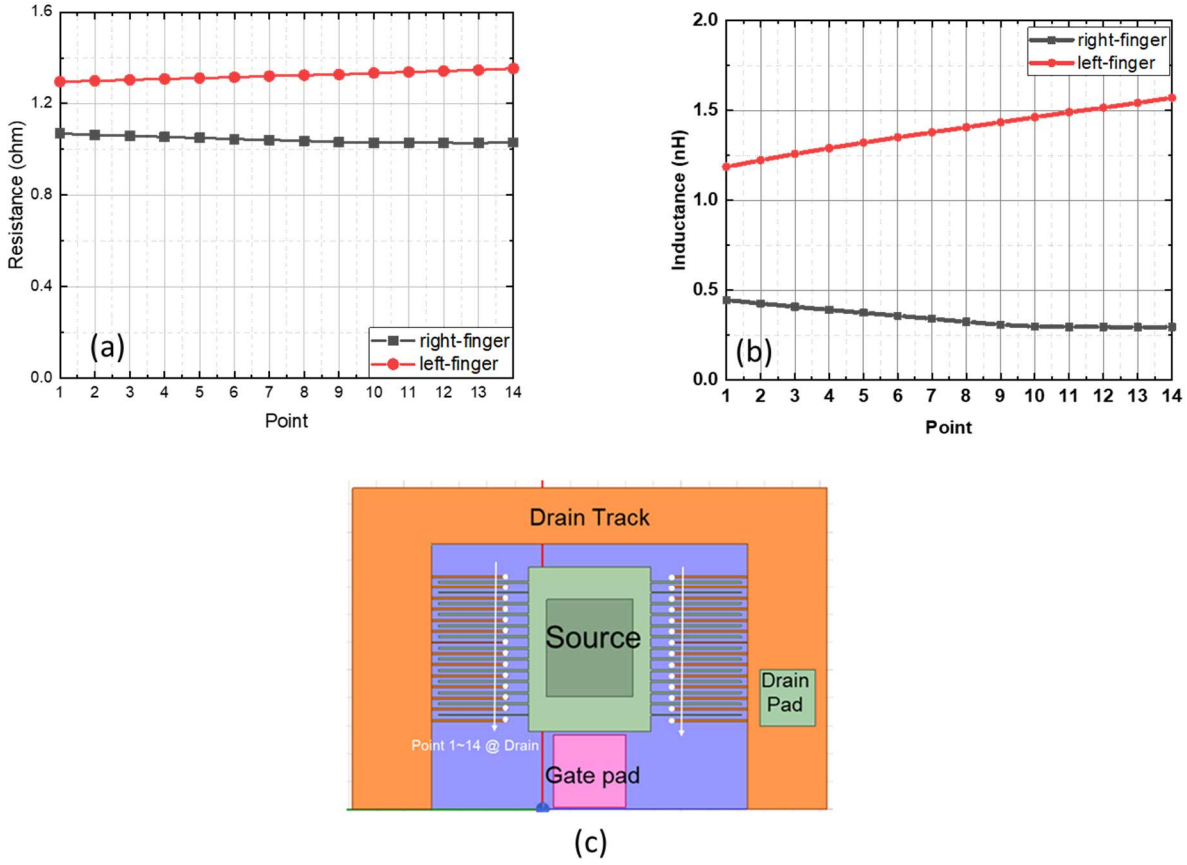


Figure 6.4.9: Simulated parasitic (a) resistance and (b) inductance of each Drain finger when employing the right Drain pad (Pad 1). (c)Schematic of extracted points on each drain finger.

6.4.4 Checkerboard layout

The Checkerboard layout is the first proposed which has a smaller size than the multi-finger layout. It looks like the Checkerboard, which employs the square Drain/Source electrodes as well as the gate path around each electrode, as shown in Figure 6.4.10. The metallic conductive path on the diagonal is the main branch for the Source path, which extends from a source electrode to join the source pads, thereby connecting the source cells in series to the source electrode. Meanwhile, the diagonal source path divides drain cells into two parts connecting to adjacent drain pads. At other vertexes of the diagonal is gate pads. There are two gate paths around the boundaries between neighbouring Source and Drain electrodes, forming the respective PSJ devices.

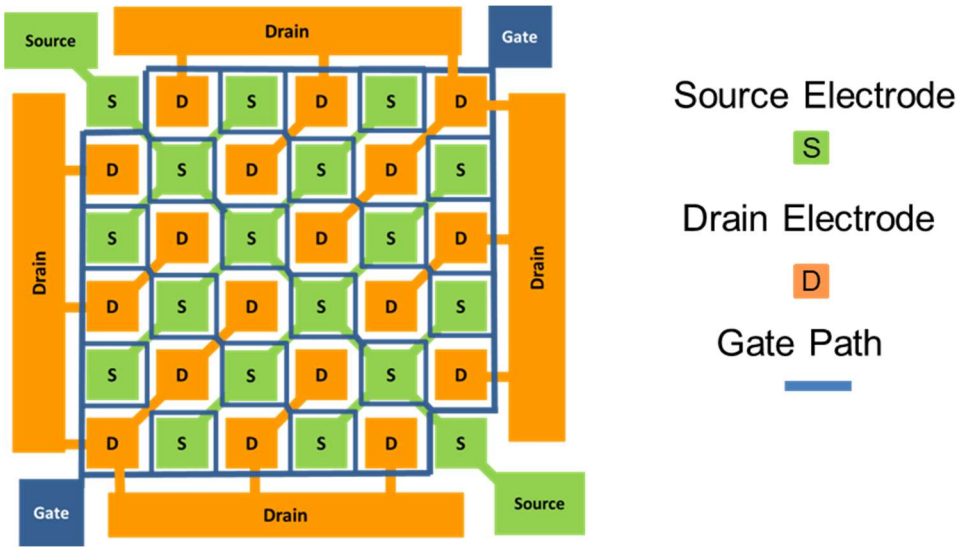


Figure 6.4.10: Schematic of Checkerboard Layout.

Assuming that the width of the electrode is 'W' and the number of electrodes for one row/column is "a". Considering the distance (Lds) between Drain electrode and the neighbour, the Source electrode. Therefore, the effective gate length for one row is

$$L_{row} = W \times a + (a-1)(L_{ds}) \text{------(6.3)}$$

There is 2(a-1) gate paths, the total effective gate path equals by:

$$L_{total} = 2(a-1)(W \times a + (a-1)L_{ds}) \text{-----(6.4)}$$

For 1A PSJ devices requiring the 20mm total effective gate Length, the minimum electrodes in one row is a~14. The total Source/Drain electrodes are at least 98. The simulated Checkerboard layout is designed with 121 source/drain electrodes, as shown in Table 6.6.

Table 6.6: Parameter of Checkerboard layout for 1A PSJ HFET

	Electrode size (μm*μm)	Electrode Number
Source Electrode	30*30	121
Drain Electrode	30*30	121
Gate/Drain/Source path	4/8/8	-

Table 6.7 shows extracted parasitic resistance and inductance of the Drain /Source conductive path for the Checkerboard layout at 100kHz. Due to the main conductive way on the diagonal of parallel multiple short branches being narrow and long, the source path has the highest parasitic resistance and inductance among five layouts. For the higher current rating, multiple such cells will be mounted and the source conductive path increases, which decreases the on-state resistance and slows down the switching speed.

Table 6.7: Extracted parasitic resistance and inductance for D-S-D Layout.

Checkboard	Resistance (mΩ)	Inductance(pH)@100Khz	Active Region(mm^2)
Drain path	1.61	5.21	0.53 (=730um*730mm)
Source path	12.43	56.38	

Figure 6.4.11 shows the gate impedance extracted from points shown in Figure 6.4.12. The gate impedance at Point 5 becomes larger.

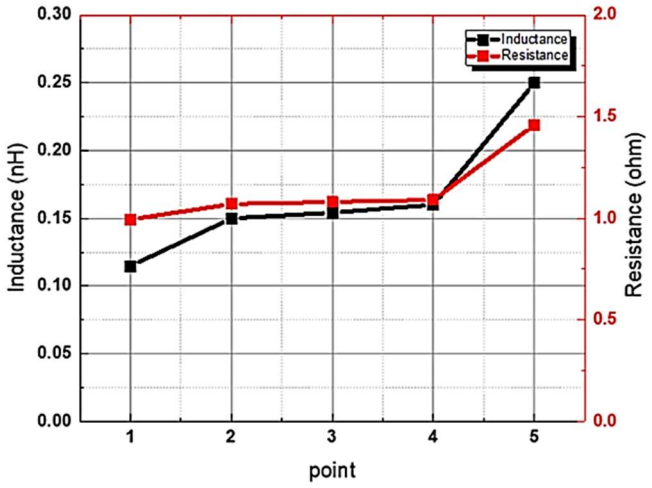


Figure 6.4.11:Parasitic resistance and inductance of extracted gate impedance

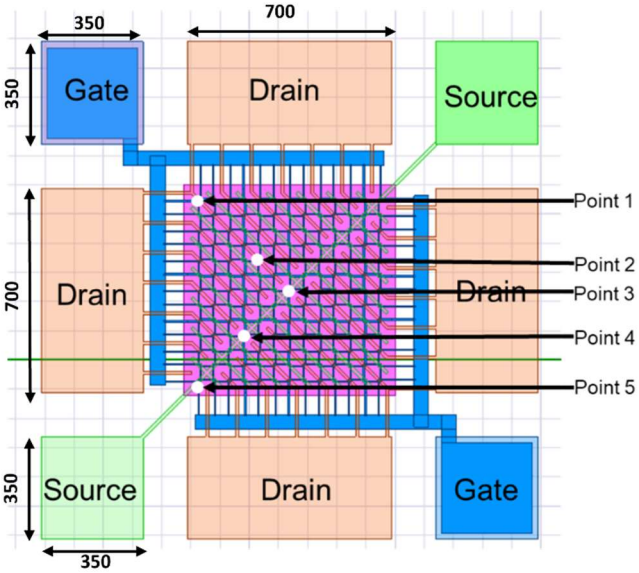


Figure 6.4.12: The extracted points at the conductive gate path for the Checkerboard layout. Dimension in µm. (Isolation layer is hidden)

6.4.5 Hexagonal-Shaped Layout

Hexagonal-Shaped Layout was proposed in 2016[120], as shown in Figure 6.4.13.

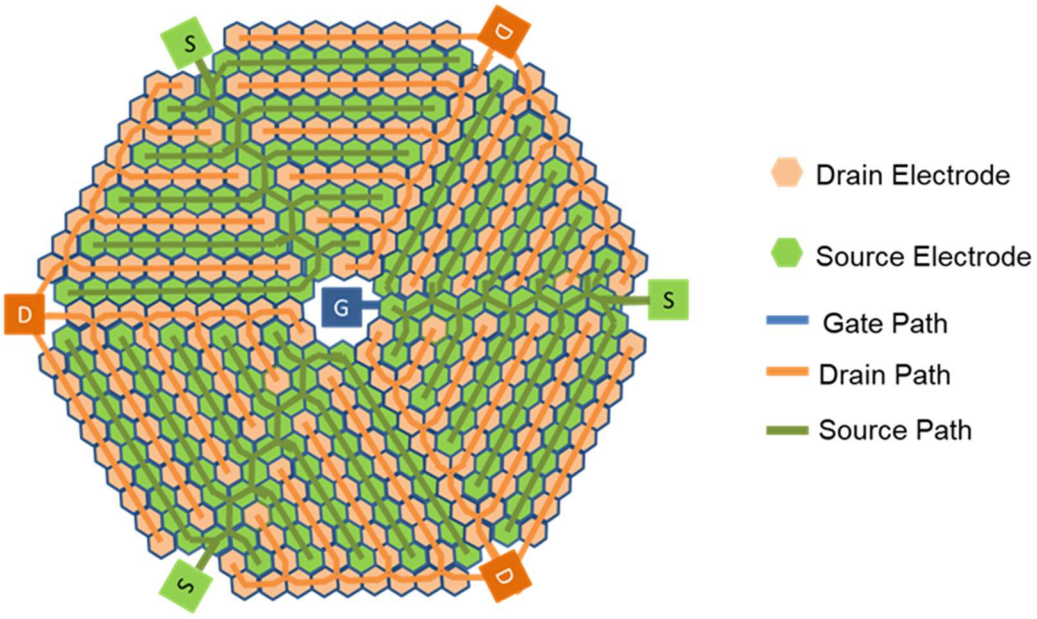


Figure 6.4.13: Schematic of Hexagonal-Shaped Layout

The Hexagonal-Shaped Layout is covered by a close-packed array of tessellating smaller hexagonal source electrodes and drain electrodes. The orange and green hexagonal cells represent drain and source electrodes, respectively. Three source pads and three drain pads are arranged at the 6 vertices of the large hexagonal region. While the Gate pad locals at the centre of the hexagonal area. A conductive metalization path extends from the source(drain) pads to the source(drain) region, thereby connecting the source electrode in series.Six gate paths (Blue lines shown in Figure 6.4.13) extend from the gate pad along the edge of electrodes to form a boundary between the adjacent source and drain cells, thus creating the respective field effect transistor between the source and drain regions of the adjacent cell.

The apparent advantage of this layout is scalability and balanced current flow. Due to the repeating nature of cells, the size of the device can be scaled and multiple such devices can be easily mounted for the required current rating. The cells are arranged evenly and rotated symmetrically to promote balanced current flow through the device, avoiding a single point of failure.

Assuming that the side length of small hexagonal cell is set as 30μm. The effective gate path for one cell is approximately 4*30=120 μm because on each Drain/Source electrode is shared by four cells. 1A PSJ devices need at least 167 source/drain cells. Considering the electrodes on the sides of

the large hexagon only share two cells, therefore, in the 3D model of the Hexagonal-Shaped Layout, it employs 198 Drain/Source electrodes to achieve a 1A current rating, as shown in Table 6.8.

Table 6.8 Parameter of Hexagonal-Shaped layout for 1A PSJ HFET

	width	**Electrode Number**
Source Electrode	a=30	198
Drain Electrode	a=30	198
Source/Drain/Gate Path	4/8/8	-

Figure 6.4.14 shows the top view of the 3D model for the Hexagonal-Shaped Layout with Gate/Source/Drain conductive path in ANSYS. In this simulation, the gate path is designed as a buried gate path, although there is no overlap region between the gate path and source conductive path, which reduces the crosstalk when the isolation layer is not perfect. Table 6.9 shows extracted parasitic resistance and inductance of Drain /Source at 100kHz. It has very low parasitic impedance for the Source and drain compared with other layout designs because the drain/source has a lot of parallel branches.

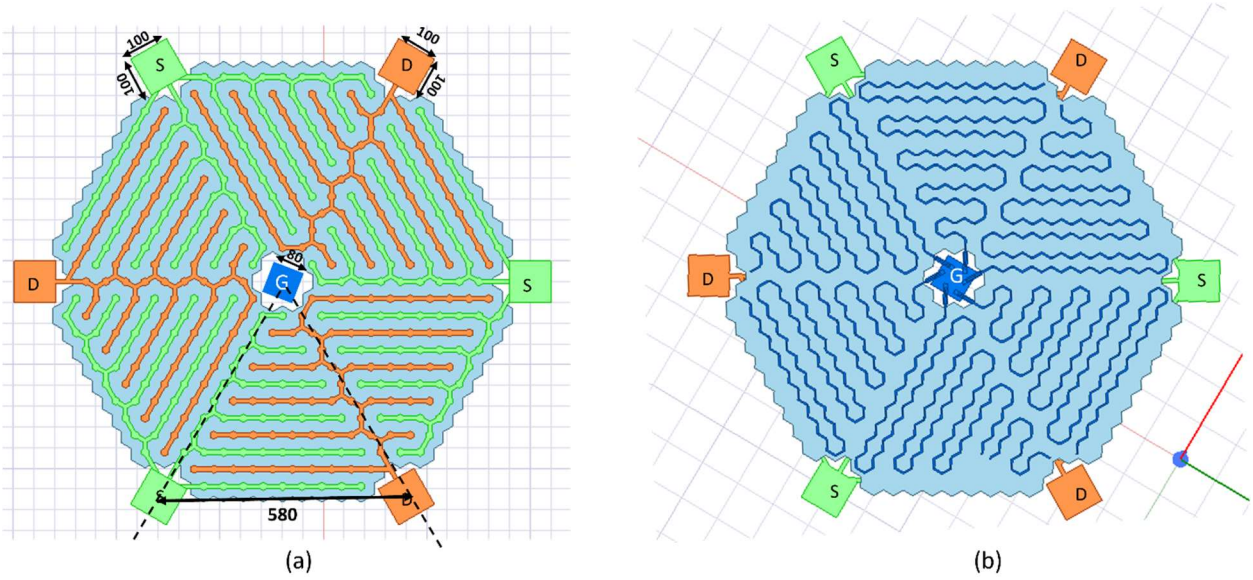


Figure 6.4.14: (a)Top view and (b) the view of the simulated Hexagonal-Shaped Layout after flipping.with Gate/Source/Drain conductive path. Dimension in µm.

Table 6.9: Extracted parasitic resistance and inductance for Hexagonal-Shaped layout.

Hexagonal-shape	Resistance (mΩ)	Inductance(pH)@100Khz	Active Region(mm^2)
Drain	1.3	1	~0.88 (a=580mm)
Source	0.51	0.3	

Due to the narrow gate width and the long conductive path, the parasitic gate impedance is larger when it is far from the gate pad at the centre. The non-uniform distribution of gate impedance can not be ignored, which causes propagation delays of input and non-uniform current distribution. Gate impedance extracted in different 4 points on the conductive gate path is shown in Figure 6.4.15(b).

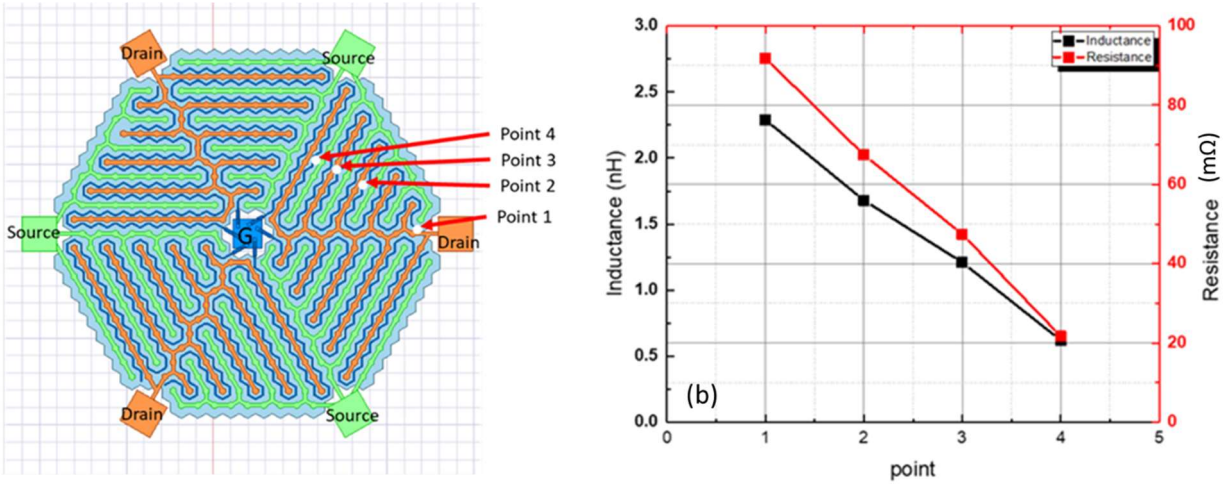


Figure 6.4.15: (a) Extracted points on the gate path and (b) gate impedance distribution.

6.5 Active area calculation

Multi-finger layout:

The active area(A) of the multi-finger layout containing the minimum number of cells for desired current rating can be estimated by Equation(6.5):

$$A = L \times [(N_{MT} + 1)W + N_{MT} \times L_{ds}]\text{-------(6.5)}$$

Where L stands for effective finger length, W is Drain/Source finger width. L_{ds} is the distance between Drain and Source which keeps the constant for different layouts. N_{MT} stands for cell number equals to $\frac{L_{total}}{L}$.

Therefore, the active area can be expressed by the formula for L :

$$A = L \times \left[\left(\frac{L_{total}}{L} + 1\right) W + \frac{L_{total}}{L} \times L_{ds}\right] = (L_{total} + L)W + L_{total} \times L_{ds}\text{-----(6.6)}$$

Where L_{total} stands for the total effective gate length.

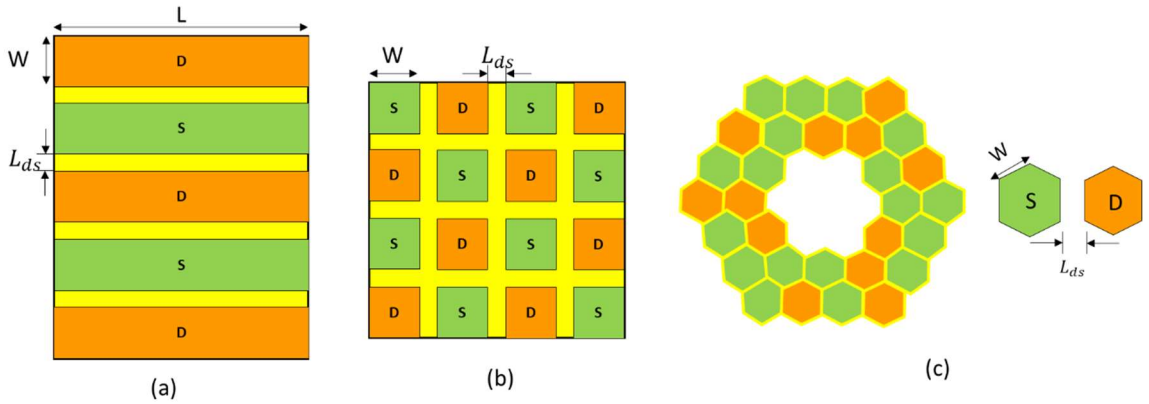


Figure 6.5.1: Schematic diagram of (a) multi-finger layout, (b)checkerboard and (c) hexagonal-shaped layout to calculate the active area

Checkboard layout:

The active area(A) of checkboard layout can be deduced by Equation(6.7):

$$A = [(a-1)L_{ds} + a \times W] \times [(a-1)L_{ds} + a \times W]\text{-------(6.7)}$$

where a stands for the electrode number in one row/column and W is the electrode width.

For high current ratings, multiple such PSJ cells are mounted. Therefore, the formation of the active area from Equation(6.8) can be simplified by:

$$\text{A} \approx [a(L_{ds} + W)]^2\text{------(6.8)}$$

The total effective gate length Equation(6.4) can be simplified by:

$$L_{total} = 2(a-1)[(a-1)L_{ds} + a \times W] \approx 2a^2(L_{ds} + W)\text{------(6.9)}$$

The active area can be expressed by the formula for electrode width (W)

$$\text{A} \approx [a(L_{ds} + W)]^2 = \frac{L_{total}}{2(L_{ds}+W)} \times (L_{ds} + W)^2 = \frac{1}{2}L_{total}(L_{ds} + W)\text{-----(6.10)}$$

Hexagonal-Shaped Layout:

As shown in Figure 6.5.1(c), the active area A for Hexagonal-Shaped Layout can be seen as the total area of small Hexagons. Considering the distance between Drain and Source electrodes (L_{ds}), the area for one Hexagonal cell can be expressed by:

$$\text{Area of small Hexagon} = \frac{3\sqrt{3}}{2}\left(\frac{\sqrt{2}}{2}L_{ds} + W\right)^2 \text{------(6.11)}$$

According to the number of the small Hexagon at least $\frac{L_{total}}{4W}$

The theoretical minimum active area is

$$A = \frac{3\sqrt{3}}{2}\left(\frac{\sqrt{2}}{2}L_{ds} + W\right)^2 \times \frac{L_{total}}{4W} \text{------(6.12)}$$

Table 6.10 compares the active area of simulated layouts for 1A PSJ HFETs measured in ANSYS Q3D.

Table 6.10: The active area of simulated layouts for 1A PSJ HFETs

Layout schemes	**Electrode Width(W) (µm)**	**Lds (µm)**	**Calculation Area (mm^2)**	**Simulated Area (mm^2)**
DS layout	30	21.5	1.05	1.14
DSD layout			1.05	1.12
SDS layout			1.05	1.12
Checkboard Layout			0.515	0.53
Hexagonal-shape Layout			0.86	0.88

Compared with multi-finger layouts, the checkboard designs and Hexagonal-shape Layout has a smaller active area for 1A PSJ HFETs in both the simulation and calculation. It should be noted that the electrode number of the Checkboard Layout and Hexagonal-shape Layout increases to form the square and hexagonal-shaped active area.

Table 6.11: A calculated active area for different layouts designed for 10A PSJ HFETs.

L_{PSJ} (µm)	**Lds (µm)**	**W (µm)**	**Calculation Area (mm^2)**		
			Mulitfinger layouts	**Checkboard Layout**	**Hexagonal-shape Layout**
5	16.5	30	9.38	4.65	7.51
10	21.5		10.38	5.15	8.84
15	26.5		11.38	5.65	10.28
20	31.5		12.38	6.15	11.83
40	51.5		16.38	8.15	19.1

The calculated active area for different layouts designed for 10A PSJ HFETs is shown in Table 6.11. Multi-finger layouts include the D-S, D-S-D and S-D-S layouts with 2800µm finger length. The

active region is calculated with at least the cell number to achieve 10A current rating. For Checkboard Layout and Hexagonal-shape Layout, to form the square and hexagonal-shape active area, it needs additional cells, and which active region is larger than the calculation. It is obvious that the Checkboard Layout has the smallest region, almost half of that for Multi-finger layouts. When the distance between Source and Dani electrode(Lds) increases and over electrode width, the advantages of the Hexagonal-shape Layout gradually weaken. For L_{PSJ}=40μm, the active region of the Hexagonal-shape Layout becomes the largest.

6.6 Summary

In this chapter, it discusses the influence of parasitic impedance from large-area devices with paralleling cells on the device performance. Following that, it introduces five metalization layout schemes for large-area PSJ devices, such as Multi-finger Drain-Source(DS) Layout, Multi-finger Drain-Source-Drain(D-S-D) Layout, Multi-finger Source-Drain-Source Layout (S-D-S) layout, Checkerboard and the hexagonal-shaped layout.

The 3D layout models for metallization interconnect are built in ANSYS Q3D and relative parasitic drain/source impedances are extracted, shown in Table 6.12. These simulated metalization layouts for 1A PSJ HFETs have the same parameters in the thickness of all metal tracks, the gate/drain/source path width, the distance between the Srouce and Drain and the electrode width. The advantages and disadvantages are discussed for layout schemes based on the extracted impedance distribution and value.

Compared with a typical D-S layout, S-D-S Layout and D-S-D layout have smaller impedance due to the shorter finger length. However, the additional Drain/Source track leads to the unbalance Drain/Source inductance when only employing only one Drain/Source pad on the side, which should be avoided. A Checkerboard layout covered by densely packed electrodes can reduce the active region effectively. The high impedance from the Source and non-uniform gate impedance distribution issues. The hexagonal-Shaped Layout benefits on much low Drain/Source parasitics impedance. Due to the narrow gate width and the long conductive path, the parasitic gate impedance is large and non-uniform distributed in the area.

Table 6.12: Parasitic Drain/Source impedance in simulated layouts for 1A PSJ OG HFETS with 10μm.

Layouts		Resistance (mΩ)	Inductance(pH)@100Khz

DS Multi-finger layout	Drain	2.36	23.23
	Source	2.6	41.8
DSD Multi-finger layout	Drain	1 (Employing Drain Pad1 and Pad2)	8.74 (Employing Drain Pad1 and Pad2)
		1.88 (Employing Drain Pad1)	24.6 (Employing Drain Pad1)
	Source	1.11	15.42
SDS Multi-finger layout	Drain	1.02	7.85
	Source	0.96 (Employing Source Pad1 and Pad2)	9.24 (Employing Source Pad1 and Pad2)
		1.82 (Employing Source Pad1)	26.31 (Employing Source Pad1)
Checkboard Layout	Drain	1.61	5.21
	Source	12.43	56.38
Hexagonal-shape Layout	Drain	1.3	1
	Source	0.41	0.3

Chapter 7: Conclusions and Future work

7.1 Conclusions

As one of the wideband gap materials, GaN is a popular candidate for next-generation power devices due to its superphysical properties. The structure of this article covers the basics of GaN HEMT technology and PSJ technology for power-switching applications. This work focuses on the development and research of GaN-based PSJ devices. This chapter summarizes the key findings and contributions of this work.

7.1.1 Compact Monolithic Bidirectional PSJ HFETs

It first proposes compact bidirectional HFETs with Schottky Gate(Bi PSJ SG HFET) and Ohmic gate(Bi PSJ OG HFET), which share the same drift region in operation when it works in the first and third quadrants. Therefore, it can be one of the most compact bidirectional switches reported to date. It is the first time to design and fabricate large-area Bi PSJ HFETs in wafer level on the 6' Sapphire substrate. The simulated and measured electrical characteristics successfully validates the Bi PSJ HFETS concept and functionality with different gate polarity control. Under different bias conditions, Bi PSJ HFETs can be operated as Bidirectional devices, unidirectional HFETs with/without Hybrid Drain-embedded Gate Injection Transistor (HD-GIT) mode and diodes in both directions.

The average measured area-specific on-state resistance Ron.A versus PSJ length and temperature is calculated. The linear increase in the Ron.A as a function of the temperature of Bi PSJ HFETs as well as the on-state resistance versus L_{PSJ} show that the device can be scaled easily scaled in both voltage and currents.

Accurate analytical models of the on-state resistance of Bi PSJ SG HFETs and Bi PSJ OG HFETs are built to calculate and analyze their components. Analytical models will promote an understanding of the mechanism of Bi PSJ HFETs. They can also effectively assist in predicting and improving the on-state performance of PSJ devices precisely

7.1.2 On-state PSJ device performance as the function of Temperature

This thesis also evaluates temperature-dependent on-state characteristics of PSJ samples such as PSJ Merged Schottky Barrier diodes(PSJ MSBD) and PSJ HFETs, as well as ohmic contact resistivity as the function of temperature. The contact resistivity of ohmic contact on AlGaN for PSJ

structure decreases while sheet resistance increases when the temperature from room temperature to 200ºC. Compared with ohmic contact in conventional PSJ structure, it has lower contact resistivity but a higher sheet resistance. The experimental results of PSJ MSBD present that the knee voltage goes down from 0.82V to 0.67V when the temperature increases from 25 ºC to 200 ºC due to the reduction in effective Schottky Barrier Height calculated in this thesis. The linear increase in the Ron.A of PSJ HFETs as a function of the temperature of Bi PSJ HFETs as well as the on-state resistance versus L_{PSJ} are presented. These results are critical for thermal analytical models of Ron.A and further improvement of on-state performance for PSJ devices.

7.1.3 Layout designs for large-area PSJ device

It provides a brief of parasitic impedance influence on the performance of large-area devices with paralleling cells. The parasitic impedance from different metalization inter-connect layouts is investigated in this thesis. Besides the typical multi-finger layout for lateral field-effect transistors, it introduces four layout schemes, such as Multi-finger Drain-Source-Drain(D-S-D) Layout, Multi-finger Source-Drain-Source Layout (S-D-S), Checkerboard layout and Hexagonal-shaped layout. The 3D models of layouts designed for 1A PSJ device with 15μm L_{PSJ} are built by ANSYS Q3D and the parasitic impedance of the metal interconnect is extracted. The advantages and disadvantages are discussed for layout schemes based on the extracted impedance distribution and value.

One issue with the typical D-S layout is that it adds parasitic impedance losses when the finger's size/number increases to achieve the high current rating. S-D-S Layout and D-S-D Layout have smaller impedances than a standard D-S configuration because their fingers are shorter. However, when just using one Drain/Source pad on the side, the additional Drain/Source track results in the unbalanced Drain/Source inductance, which should be avoided. A Checkerboard configuration covered in closely spaced electrodes can effectively reduce the active region. It features a low drain parasitic impedance but a high source impedance and an uneven distribution of gate impedance. Moreover, the active area is smaller, and the drain/source parasitic impedance is substantially lower in the hexagonal-shaped layout. The area's parasitic gate impedance is high and not evenly distributed because of the narrow gate width and long conducting channel.

7.2 Future work

Further research and opportunities can be described as follows:

For Bi PSJ HFETs

- The purpose of this project is to validate the device concept and functionality with different gate polarity control. Future work is needed with the optimum epitaxial structure for demonstrating high-voltage breakdown devices. It is necessary to evaluate temperature-dependent off-state characteristics of Bi PSJ HFETs.
- It is necessary to measure the Capacitance-Voltage (C-V) characteristics of Bi PSJ HFETs. In this project, Bi PSJ HFETs are in the wafer level on the 6' sapphire wafer. Therefore, it is hard to connect the external circuit to Capacitance-Voltage (C-V) characteristics. In the future, Capacitance-Voltage (C-V) characteristics is essential to measure for the evaluation of the switching behaviour of Bi PSJ HFETs
- Dynamic performance through switching measurements will be done. The main applications of GaN-based devices are in high-frequency switching. Hence, extensive evaluation of resistive and inductive switching performance will be necessary.
- According to the analysis of the specific on-state resistance for fabricated Bi PSJ HFETs, the resistance from channel and gap resistance contribute to the additional resistance due to the long channel gap length. It will need to optimize the basic structure of Bi PSJ HFETs cells. In addition, the thermal analytical models can be built to predict and improve the on-state performance of PSJ devices precisely
- The fabricated large-area devices can not achieve the desired current rating. Future work focuses on improving the current density and large-area layout designs.

For Layout designs for large-area devices

- The parasitic impedances of five layouts were extracted and compared. Different layout designs show advantages in different aspects. With extracted parasitic impedance, it can simulate parallel PSJ HFETs to investigate its effect on the static and dynamic performance of PSJ HFETs in the future.
- Thermal distribution and current distribution are necessary to simulate and analyze.
- The layout design of PSJ devices will be optimized by simulation. In the future, it needs to evaluate and compare the performance of large-area PSJ devices with optimized layouts.

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Appendix-1

List of Acronyms

2DEG	Two-Dimensional Electron Gas
2DHG	Two-Dimensional Hole Gas
Al	Aluminium
AlGaAs	Aluminium Gallium Arsenide
AlGaN	Aluminium Gallium Nitride
AlInN	Aluminium Indium Nitride
AlN	Aluminium Nitride
Au	Gold
BFOM	Baliga'S Figure Of Merit
BHFOM	Baliga'S High Frequency Figure Of Merit
Bi-GaN	Bidirectional GaN switch
Bi PSJ HFETs	Bidirectional PSJ HFETS
BPS	Bidirectional Power Switch
BV	Breakdown Voltage
C	Carbon
CC	Common Collector
CE	Common Emitter
CSI	Common Source Inductance
CTE	Co-Efficient Of Thermal Expansion
CV	Capacitance Voltage
CVD	Chemical Vapor Deposition
DS	Drain-Source
D-S-D	Drain-Source-Drain
E-H Pair	Electron-Hole Pair
Epi	Epitaxy
FM	Floating Metal
FOM	Figure Of Merit
FP	Field Plate

FQS	Four-Quadrant Switch
FR	Forward Region
FRD	Fast Recovery Diodes
Ga	Gallium
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GIT	Gate Injection Transistor
HCl	Hydrochloric Acid
HCP	Hexagonal Close Packed
HD-GIT	Hybrid-Drain-Embedded Git
HEMT	High Electron Mobility Transistor
HF	Hydrofluoric Acid
HFET	Heterostructure Field Effect Transistor
HVPE	Hydride Vapor Phase Epitaxy
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
InN	Indium Nitride
JFOM	Johnson'S Figure Of Merit
LFOM	Lateral Device Figure Of Merit
MBE	Molecular Beam Epitaxy
MES	Metal Semiconductor
MESFET	Metal Semiconductor Field Effect Transistor
MOCVD	Metal Organic Chemical Vapor Deposition
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSBD	Merged Schottky Barrier Diodes
N	Nitride
OG	Ohmic Gate
OVP	Overvoltage Protection
PCM	Process Control Monitor
PDFOM	Power Device Figure Of Merit
PECVD	Plasma Enhanced Chemical Vapor Deposition
PSJ	Polarisation Super Junction

RB-IGBTs	Reverse Blocking Igbts
RESURF	Reduced Surface Field
RIE	Reactive Ion Etching
RTA	Rapid Thermal Annealing
SBD	Schottky Barrier Diode
SBH	Schottky Barrier Height
S-D-S	Source-Drain-Source Layout
SG	Schottky Gate
Si	Silicon
SiC	Silicon Carbide
SiO2	Silicon Oxide
SJ	Super Junction
SSCB	Solid state circuit breaker
TEG	Test Element Group
Ti	Titanium
TLM	Transmission Line Method/Model
WBG	Wide Band gap