University of Sheffield

Switching Characteristics of High Voltage Gallium Nitride Cascode Devices

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By

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Table of Contents

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Abstract

The theoretical limitation of Silicon has led to intense research towards the Next Generation of Gallium Nitride devices. Since GaN devices are inherently normally - on because of the 2DEG formed due to their polarisation property, driving them can become challenging. One of the options to overcome this challenge is the cascode structure, where the low-voltage Si-MOSFET is connected in series with the high-voltage GaN HEMT. Therefore, the gate of the device is that of Si-MOSFET, which is much easier to control when compared to GaN.

This work focuses on the switching of GaN cascode devices. Since the cascode structure has two die, the connection between them is made through wire bonding. This can give rise to internal parasitic inductances which cause ringing during the switching transition. The packages investigated here are TO-247, TO-220 and the new CCPAK by Nexperia. The first two is the traditional 3-leaded package and the third one is surface mount. The performance evaluation of these three devices is discussed in detail, along with their switching energy loss. Finally, the three GaN devices are compared to Si-CoolMOS to understand and observe the superior qualities of GaN, which have been thoroughly discussed in previous works of literature. Then, a brief introduction of 1.2 kV PSJ GaN which is a normally-on d-mode device is done in Chapter 4, along with the extracted static characteristics of the device. And, finally, the device is modelled in SaberRD with the help of extracted static characteristics. The switching characteristics of the device are analysed through simulations by implementing the device in a switching test.

Even though GaN devices have a lot of advantages in terms of their fast switching, lower energy losses, etc., Dynamic $R_{DS(on)}$ still becomes a concern when it comes to the performance of the device. To observe and understand the Dynamic $R_{DS(on)}$ proper circuit needs to be implemented as the switching voltage switches in the order of hundred volts during the off-state and turn-on state in the order of millivolts. Therefore, in this section, a previously explored clamping circuit is implemented to observe the Dynamic $R_{DS(on)}$ of cascode devices.

List of Figures

List of Tables

Chapter 1: Introduction

Following recent statistics provided by the International Energy Outlook 2023 (IEO2023), the CO_2 emissions due to the use of natural gas, and coal is shown to increase by 34% over the next 30 years when compared with the year 2022 [1]. The increase in population is one of the factors that affect the increase in consumption of natural gas, fossil fuels etc. The report mentioned that global energy consumption will increase by 34%, that is from 638 quadrillion British thermal units (quads) in 2022 to 855 quads in 2050.

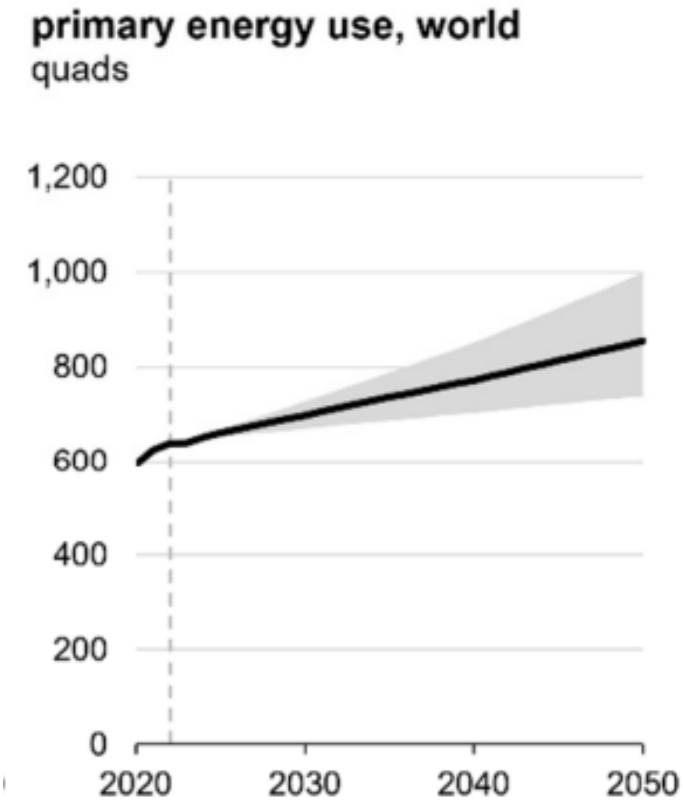


Figure 1: World energy use: IEO 2023 [1]

From Figure 1 it can be seen that the growth of renewable energy as a main energy consumption is observed to increase from 21% in 2022 to a maximum of 34% in 2050. The increased use of electric power generation has given rise to the increase in energy consumption of renewable sources.

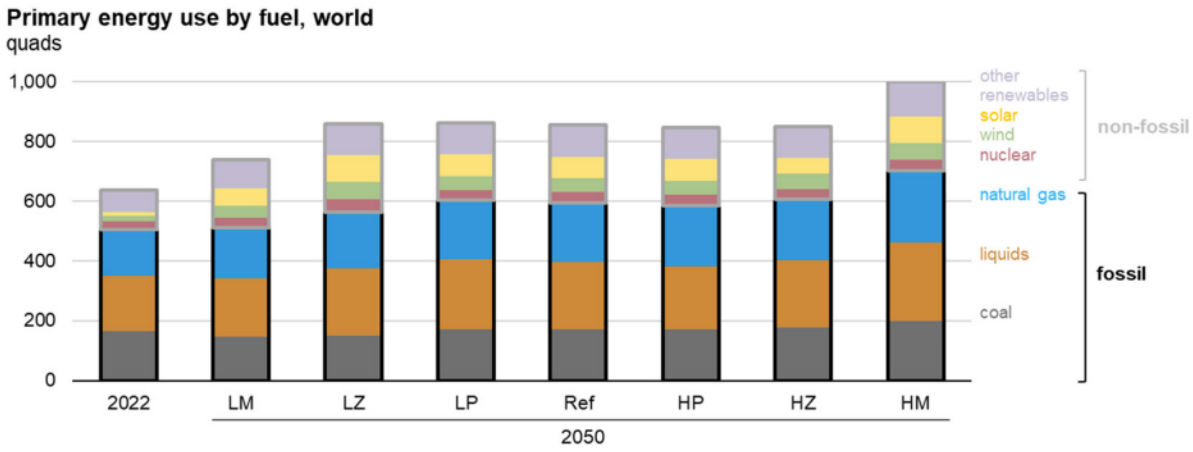


Figure 2: World primary energy use reference – 2022, predicted till 2050 for various energy sources across all cases [1]

As energy consumption increases and to combat degradation in environmental conditions, the need for greener technologies becomes important [2]. Climate change poses a warning sign for the world and it is necessary to take action to preserve the resources for future generations [3]. As can be seen from Figure 2, an increase in wind, solar and other renewable energy consumption ought to increase in the coming years. To help with this, reliable sources of renewable energy are necessary. This is where the role of power electronics comes into being. With the development of new power electronics systems, various applications ranging from Electric vehicles to aerospace applications can benefit from efficient energy conversion without a significant increase in CO_2 emission and harming the environment. A complete transition from non-renewable to renewable does not happen easily. The driving factor of a power electronic system is the power semiconductor devices which help in fully realising the efficiency of a power electronic system.

1.1 Wide Band Gap (WBG) Power Devices

Silicon devices have dominated the power electronics market since the 1950s. However, the intrinsic property of silicon has put a limitation on its performance leading to reaching its theoretical limits. Table 1 lists the properties of Si, two polytypes of SiC and GaN. The Bandgap of Si is 1.12 eV, whereas the devices under the Wide Band Gap category have a bandgap three times higher than Si.

Property	Unit	Si	GaN	6H-SiC	4H-SiC
Bandgap (E_g)	(eV)	1.12	3.45	3.03	3.26
Electric breakdown field (E_c)	(kV/cm)	300	3300	2,500	2,200
Electron mobility (μ_n)	(cm^2/V*s)	1,500	1,700	500	950
Thermal conductivity λ	(W/m*K)	150	130	490	380
Saturated electron drift velocity (v_{sat})	($*10^7\ cm/s$)	1	2.2	2	2

Table 1: Properties of Silicon and major wide band gap semiconductors [4]–[6]

Compared to Si devices, SiC devices are shown to have a higher breakdown field as well as higher thermal conductivity, whereas GaN devices are shown to have a higher breakdown field as well as high electron mobility. One of the main problems mitigated by the SiC devices, due to its high thermal conductivity is that the junction temperature of SiC has the potential to go up to $400°C$, whereas Si can reach up to a maximum of 150°C [7]. The other disadvantages of Si include its inability to offer lower switching losses at high current, its low switching frequency and as mentioned before, poor performance at high temperatures [8]. Due to these reasons, wide band gap devices have been replacing Si devices as a way to evolve and meet certain applications.

Figure 3 shows the features of the wide band gap devices. The blue blocks represent the properties of WBG devices and the orange represents the benefits shown by the products because of their characteristics. The higher breakdown field provides the device with high voltage blocking capacity which results in thinner devices and in turn lowers the on-state resistance, lowering the conduction losses. These characteristics when used for application will have the advantage of reduced cost, less energy consumption and reduction in size.

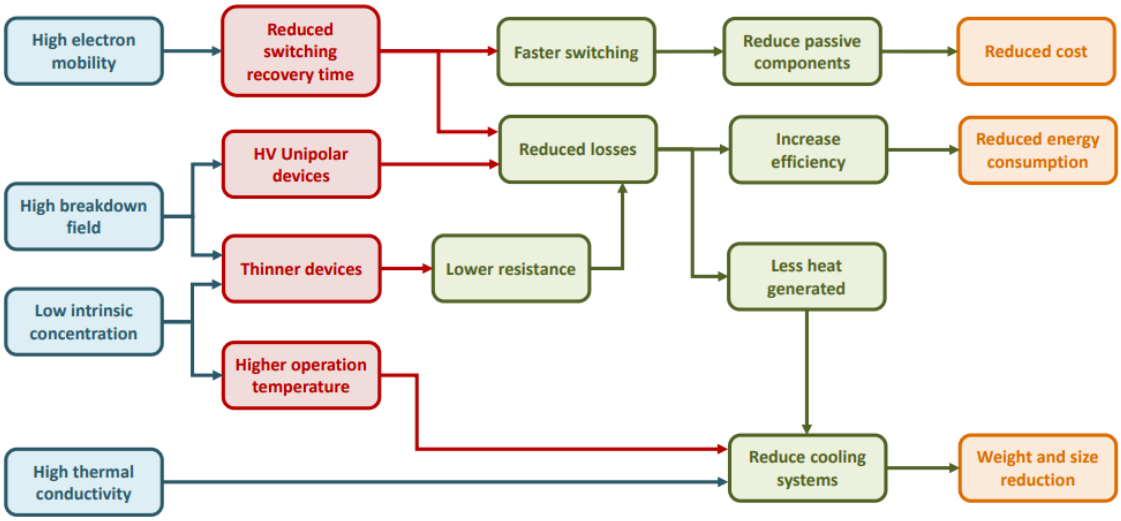


Figure 3: Figure representing Wide band gap properties (Blue), properties affected by its advantages (Red), Influence on the Power electronics behaviour (Green), benefits shown by the products (Orange) [8]

Now that the advantages of WBG devices have been established, among them the Gallium Nitride (GaN) devices have proven to perform well at higher switching frequencies, provide greater efficiency and have significantly reduced size [9]. GaN devices also have a high breakdown field when compared to SiC, a competitive quality which makes it a good candidate for power applications [10].

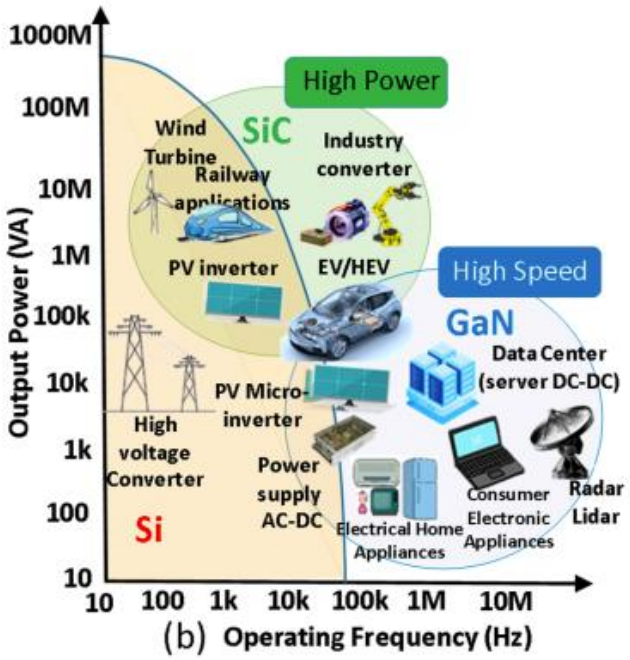


Figure 4: GaN, SiC and Si Application areas [11]

Figure 4 represents a consolidated picture of various applications for Si, SiC and GaN with respect to their output power and operating frequency. It can be seen that GaN devices operate at high frequencies and a very wide range of applications fall under GaN such as EV/HEV, Consumer electronics, and electrical home appliances. This helps in achieving a solution to the problem mentioned in the introduction, about increasing population which in turn increases the demand for energy consumption. However, GaN devices, due to their fast-switching nature, and their inherently normally-on nature, can pose challenges while realising their full potential. More on this will be discussed in the following chapters.

1.2 Thesis Outline

The thesis has investigated a (i) new surface mount package GaN device and compared to the existing two packages, the GaN devices are also compared to Si-CoolMOS (ii) Modelled a normally-on d-mode GaN in SaberRD (iii) Implemented a previously explored clamping circuit to measure dynamic on-state resistance of GaN cascode device. The outline of the thesis is as follows:

Chapter 1: Provides an overview of the limitations of Si devices and explains the need for Gallium Nitride devices, introduction to their challenges and advantages is given. Finally, the outline of the thesis is provided.

Chapter 2: A literature review on the principle properties of GaN devices, working of normally-off e-mode GaN and cascode GaN structure is explained. Ways to achieve e-mode devices are explored as well. The functioning of the parasitic capacitances during the switching transition is explained and the operating modes of GaN cascode structure are explained. Gate drive design for cascode GaN, and different packaging of the devices is also provided. Finally, the current collapse phenomena observed in GaN devices is explained and the circuits that can be implemented to measure the Dynamic $R_{DS(on)}$ of GaN are provided.

Chapter 3: Provides Double Pulse Tester experiment methodology, the components and equipment used. The practices used for correct voltage probing are discussed. Followed by the working of the GaN cascode device in the double pulse switching is explained in detail. The chapter investigates the influence of two different current shunt resistors (CSR) on the power-loop path of the device. The energy comparison between both scenarios is discussed and finally, the CSR which performed better is used for further switching analysis

Chapter 4: Investigates the switching characteristics of the device in three different packages namely TO-247, TO-220 and the new CCPAK. A Double Pulse tester is implemented for the comparison. The chapter starts by comparing the TO-247 to CCPAK under different operating conditions, such as varying gate resistors and varying gate currents. The impact of gate resistance on the switching waveform is also analysed. Finally, the new surface mount CCPAK is compared with TO-220 and the findings are reported.

Chapter 5: This chapter is divided into two sections; the first section is dedicated to observing the performance of GaN devices that were used for analysis in Chapter 4 when compared with Si-CoolMOS. The analysis similar to that of Chapter 4 is done with the help of a Double Pulse Tester. The superior behaviour of GaN is confirmed by comparing the energy loss of all four devices.

The second section consists of modelling of 1.2 kV Polarisation Super Junction GaN which is a normally-on device and is modelled in Power MOSFET Tool, SaberRD by Synopsys. The extracted I-V characteristics of the device are presented which is then used for the modelling purpose. The device is then implemented in a simulated environment consisting of a Double Pulse Test. The waveform is analysed and the simulation is done for different operating conditions.

Chapter 6: A detailed explanation of measuring Dynamic $R_{DS(on)}$ in GaN cascode devices is provided. The chapter starts with briefly explaining the previous literature and understanding the functioning of the implemented clamping circuit, and the components used. Followed by experiment results for different drain voltage, drain current and stress times before turning on the device (When the Dynamic $R_{DS(on)}$ is calculated).

Chapter 7: Concluding remarks of the thesis and future scope are presented. Various research that can be carried out in continuation of the work presented in this thesis is suggested.

Chapter 2: Literature Review

This chapter covers previous literature related to the research undergone in this thesis. The chapter starts with the fundamental properties of Gallium Nitride devices, followed by the normally-off structure of GaN. The cascode structure of GaN is discussed in detail followed by their packaging. The impact of the gate drive circuit on the GaN cascode switching is discussed. Finally, the current collapse phenomena observed in GaN devices are explored along with the clamping circuit that is used in measuring the dynamic on-state resistance of GaN is discussed.

2.1 Basic Structure of GaN HEMT

Figure 5 represents the basic structure of GaN HEMT. The device is based on the principle of polarization seen in the AlGaN/GaN heterostructure. The Polarization property is such that spontaneous 2DEG - two-dimensional Electron Gas is formed at the intersection of undoped AlGaN and undoped GaN. This happens due to the Wurtize structure of GaN [5]. It is one of the crystal structures among the three. The other two are rock salt structure and zinc blende [12]. The Wurtize structure was found to be the most stable among the three structures under ambient conditions. The 2DEG that is formed is a layer of electrons that extends from the drain to the source, a path of low-resistance thus making the device naturally normally-on. This means that at zero bias at the gate i.e. when $V_{GS} = 0$ and when a voltage is applied to the drain, current flows from the drain to the source of the device. When the gate voltage is less than 0 V, the concentration of 2DEG starts to decrease. And, finally, when the gate voltage is less than the threshold voltage of the HEMT $V_{GS} < V_{TH}$ the device is turned off because the 2DEG gets depleted below the gate region. Figure 6 represents the D-mode GaN in its off state. This nature of GaN being normally - on raises reliability concerns and makes it challenging for power converter applications. Therefore, various research has been done to make the device reliable by exploring the normally-off versions of GaN [13].

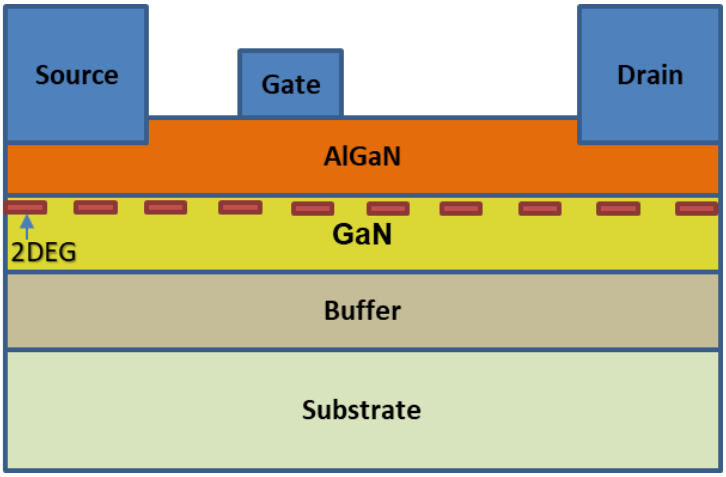


Figure 5: D-mode Gallium Nitride Basic Structure – On-state

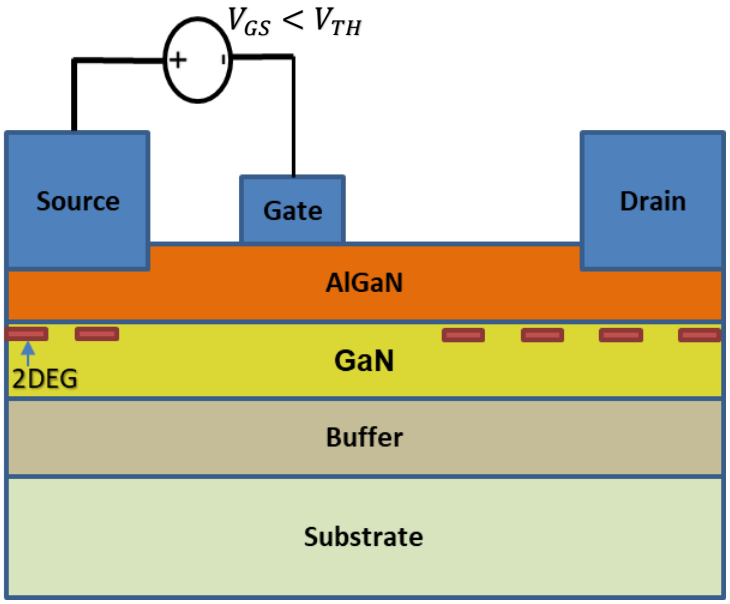


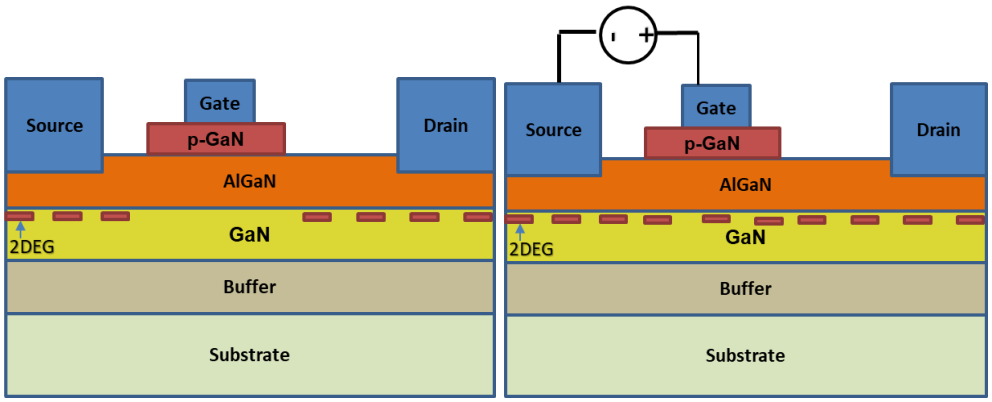
Figure 6: D-mode Gallium Nitride Basic Structure – Off state

2.1.1 Normally-off GaN

Although GaN devices have a lot of advantages, the spontaneous formation of 2DEG makes them normally-on devices. Therefore, to make them suitable for various applications and also to have a simpler gate drive circuity to drive the device, a lot of research has been carried out to make them normally-off. There are three distinct ways to realise the normally-off function. The first and second ones are – non-insulated and insulated gate enhancement mode (E-mode) and the third is the cascode structure [14].

Enhancement-Mode

The non-insulated enhancement mode can be realised in three ways – p-GaN gate, Gate injection transistor and recessed gate. p-GaN gate, configuration is achieved by depositing a p-doped GaN under the gate as shown in Figure 7 (a). This helps to lift the threshold voltage of the device. The first normally-off commercial p-GaN gate was introduced by Efficient Power Conversion EPC [15].



(a) (b)

Figure 7: p-GaN gate deposited below the gate (a) Off-state (b) On-state

Figure 7 (a) and (b) represent the E-mode structure where the p-GaN is deposited below the gate. Similar to the p-GaN gate, GIT uses p-doped AlGaN below the gate [16]. This will again help in making the threshold voltage positive and thus will deplete the 2DEG. The next way to obtain the normally-off function is the recessed gate. The recessed gate is achieved by etching a very small portion of AlGaN beneath the gate [17]. The etching needs to be carried out carefully so that the 2DEG layer is not affected and the gate control can be done efficiently.

The next category is the insulated gate-enhancement mode devices. Under this category falls the MISHEMTs- Metal Insulated Semiconductor HEMT. The AlGaN layer is removed, and in that place, materials such as SiO2 or SiN are deposited. Figure 8 represents the GaN MISHEMT structure [6], [18].

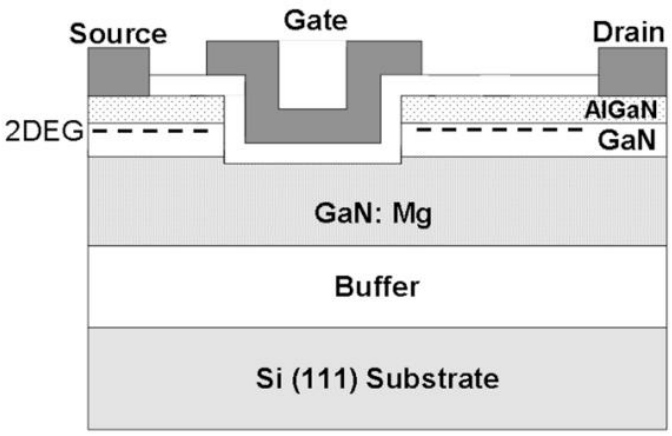


Figure 8: MISHEMT GaN Structure [18]

Even though e-mode GaN helps in making the threshold voltage positive, the value is in the range of + 1 V- + 2 V or a maximum threshold voltage of + 2.5 V. This can lead to poor gate drive configuration and gate immunity because the maximum gate voltage that can be applied is around + 6 V [19]. Some companies that supply normally-off e-mode GaN include EPC, Cambridge GaN Devices, Navitas, GaN Systems, Infineon [20] etc. Some companies such as Navitas [21] and Cambridge GaN Devices [22] have introduced integrated GaN ICs. For instance, the Cambridge GaN Devices have introduced ICeGaN HEMT. A monolithic die is integrated with a gate driver that shifts the threshold voltage to + 3 V. And, the need for negative gate voltage can be avoided as well [22]. They can be driven by regular off-the-shelf gate drivers. The voltage range is similar to GaN cascode devices which is 0 – + 20 V.

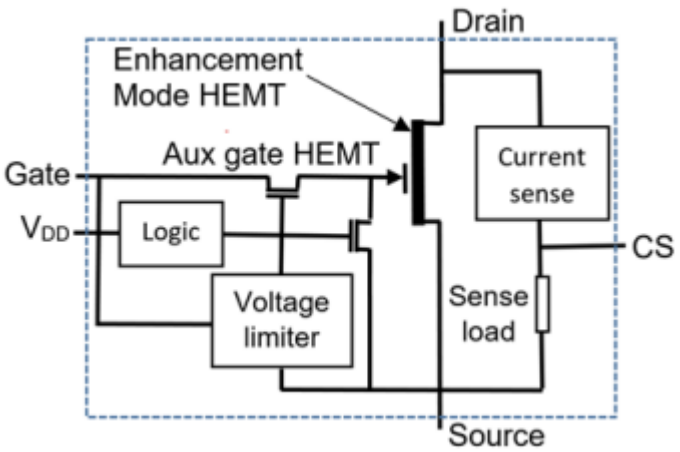


Figure 9: Cambridge GaN Devices ICeGaN HEMT [22]

Cascode device structure

Another way to make the device normally-off is the cascode structure. The advantage of this configuration is that the device has the gate drive capability of a Si-MOSFET which makes the gate drive circuit much simpler compared to the e-mode. Also, the GaN device is not modified like the e-mode therefore the inherent qualities of the device are unaltered. The packaging of cascode devices is done such that the two dies are connected through wire bonding. Figure 10 shows the structure of the GaN cascode, the drain of Si-MOSFET is connected to the source of GaN. The cascode structure drain is of GaN HEMT, the source of Si MOSFET is connected to the gate of GaN HEMT which acts as the device source. And, as mentioned before the gate of the device is of Si-MOSFET.

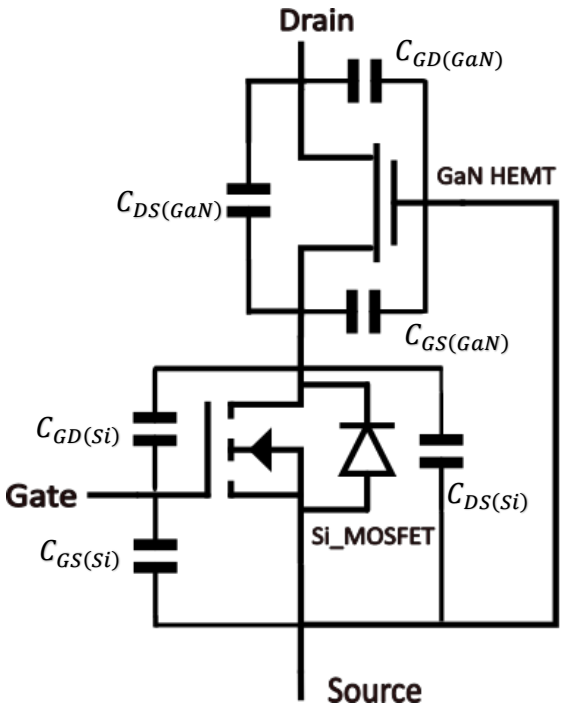


Figure 10: GaN cascode structure with internal capacitances

Figure 10 also shows the GaN cascode internal structure with its parasitic capacitors where the input capacitance of a device is given by $C_{iss} = C_{gd} + C_{gs}$, the output capacitance $C_{oss} = C_{ds} + C_{gd}$ and the reverse transfer capacitance C_{rss} is C_{gd} itself.

During the turn-on transition, i.e. when a signal is applied to the Si-MOSFET gate, the $C_{GS(Si)}$ gate-source capacitance is charged till the Si-MOSFET threshold is reached. When

the channel becomes conductive, current flows through the output capacitors of the MOSFET i.e. $C_{GD(Si)}$ and $C_{DS(Si)}$. The parallel capacitor $C_{GS(GaN)}$ is charged and reaches its threshold value. And, once the threshold value of GaN HEMT is crossed, the channel of GaN HEMT becomes conductive and the drain to source voltage of GaN HEMT decreases and the device is now fully on.

During the turn-off transition, the gate signal reduces to zero, at this instant the gate of Si-MOSFET discharges through the driver circuit until the saturation region of the Si-MOSFET is reached [23]. The Si-MOSFET drain to source voltage starts to rise when the applied load current charges the output capacitor of the Si-MOSFET. When the output capacitors of MOSFET are charging, the gate to the source capacitor of the GaN HEMT is discharged and the drain to the source voltage of GaN starts to rise and reaches the final value, thus turning off the device.

GaN cascode operating modes

Forward blocking mode

There are two conditions under this operating mode:

(I) When the gate voltage is zero $V_{GS} = 0\ V$ i.e. **when $\boldsymbol{V_{GS(Si)} < V_{TH(Si)}}$ and $\boldsymbol{V_{DS} < -V_{TH(GaN)}}$**. The Si-MOSFET channel is not conducting and blocks the applied V_{DS} voltage. When the applied voltage is less than the threshold voltage of GaN, the GaN device is on and will not block the applied V_{DS} voltage. In this scenario all the forward voltage is blocked by Si-MOSFET alone [24], [25].

(II) $\boldsymbol{V_{GS(Si)} < V_{TH(Si)}}$ **and** $\boldsymbol{V_{DS} > -V_{TH(GaN)}}$

In this case, the applied voltage across the cascode device is higher than the threshold voltage of GaN, now both devices are in blocking mode.

Forward conduction mode

$\boldsymbol{V_{GS(Si)} > V_{TH(Si)}}$

The voltage applied to the gate of Si-MOSFET exceeds the threshold voltage. In this case, the Si-MOSFET channel conducts which in turn conducts the channel of GaN HEMT.

Therefore, in this case, all the channels are conducting and the device is in on state. When the device is in its on state, the on-state resistance is the sum of $R_{DSon(Si)}$ and $R_{DSon(GaN)}$.

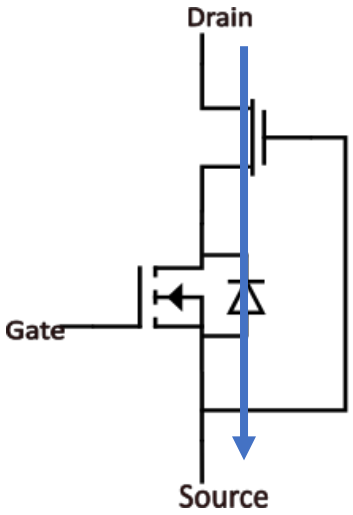


Figure 11: Forward conduction mode of GaN cascode

Reverse conduction mode

When the applied gate voltage is less than the threshold voltage of Si-MOSFET, the body diode of the Si-MOSFET starts conducting. Therefore, when the diode is in forward bias, the gate and source voltage of the GaN HEMT becomes approximately the same as the diode voltage. This makes the channel of GaN HEMT to conduct. The reverse conduction now occurs through the body diode and GaN HEMT. Equation 1 represents the reverse conduction phenomena [24].

$$\boldsymbol{V_{SD} = V_{SD(Si)} + I_{SD} * R_{DS(GaN)}} \qquad \textit{Equation 1}$$

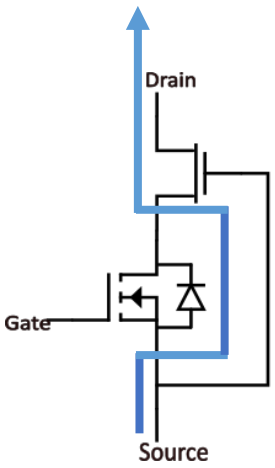


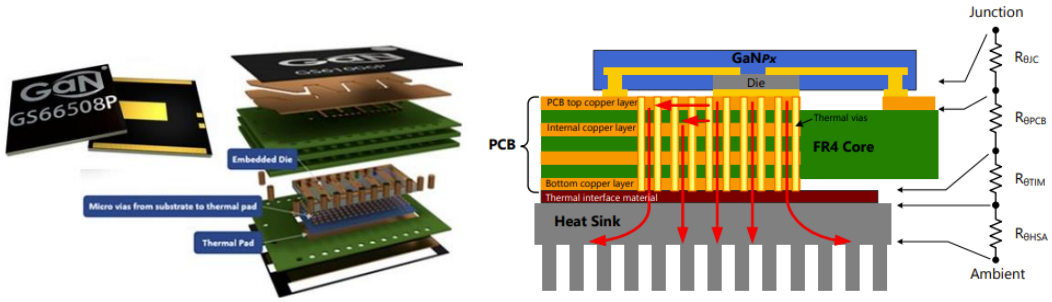
Figure 12: Reverse conduction of GaN cascode

2.2 GaN Cascode Packaging

As mentioned above, GaN devices are inherently normally-on, therefore the gate drive requirement for such devices becomes challenging. Ways to mitigate this problem are discussed by introducing normally-off GaN. The first one is the e-mode GaN and the other is the cascode structure. One key factor to realise the potential of GaN devices is their packaging. e-mode GaN device packaging involves only one chip and the packaging can be in a simpler form, for example, EPC has the devices in die form, which can be directly soldered onto the PCB. This helps in reducing the inductance and can be placed close to the gate driver and the gate resistance.

Figure 13: EPC GaN die [26]

Other companies such as GaN Systems have introduced the Embedded GaNPX package where the wire bonding is replaced by a galvanic process.



(a) (b)

Figure 14: (a) GaN Systems Embedded packaging (b) Cross-sectional view of GaNPX and its thermal dissipation path [27]

It can be seen from Figure 14 (a) that, there is a series of PCBs that form the drain and source bus bar which helps in increasing the current carrying capacity of the device. And, the device remains protected inside the lamination area [27]. Figure 14 (b) shows the

thermal dissipation path for the device. The device consists of a bottom-side cooling where the heat generated is first flown to the thermal pad of the device and then to the PCB.

The other option for normally-on GaN devices to obtain a positive threshold is the cascode structure. GaN cascode structure, unlike the e-mode, involves two devices in one package. The advantage of cascode devices over the e-mode GaN is that cascode devices can use off-the-shelf gate drivers as the gate of the cascode is of Si-MOSFET. Although, due to the complex circuitry of cascode devices, packaging them becomes a critical factor. The internal parasitics of the devices contribute to oscillations, which in turn will affect the functioning of the device. Therefore, for a sensitive device like a cascode, packaging needs to be done with utmost care.

Table 2 shows most of the available cascode devices, their parameters and packaging. Transphorm provides TO-247, TO-220, PQFN packages and whereas Nexperia provides TO-247 which is commercial and their new Surface mount package called the CCPAK. And, Figure 15 (a-c) shows three packages, two are commercially available which are the TO-220 and TO-247 and the CCPAK which is the surface mount type provided by the manufacturer.

Manufacturer	Voltage rating (V)	Current Rating (A) (max)	Rdson (mΩ) (typ)	Package
Nexperia [28]	650	34.5	50	TO-247
		47.2	35	TO-247
		60	33	CCPAK1212
		60	33	CCPAK1212i
Transphorm [29]	650	95, 46.5, 47, 34, 36	15, 35, 35, 50, 50	TO-247
		34	50	TO-263
		6.5, 16, 25, 29	240, 150, 72, 72	PQFN88
		3.6, 16	480, 150	PQFN56
		16, 29	150, 72	TO-220
	900	50	34	TO-247

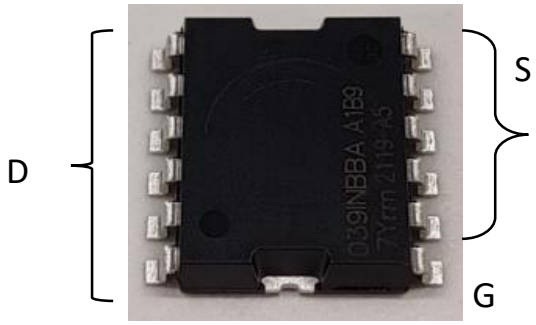
Table 2: Available Gallium Nitride Cascode Devices and their parameters. All Parameters are for 25 °C and obtained from respective datasheets.

G S D

(a)

G S D

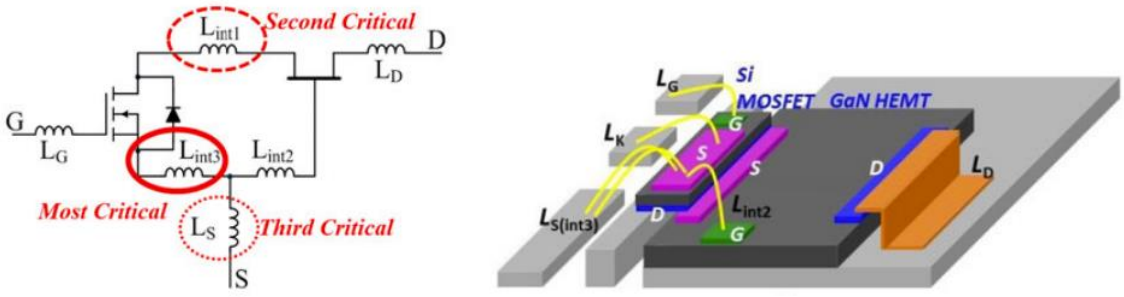
(b)



(c)

Figure 15: GaN cascode devices in three different packages (a) TO220 (b) TO247 (c) CCPAK

The TO-247 3-leaded package has proven to be robust and efficient in terms of different converter applications [30], [31]. There are a few publications that explain the impact of packaging on cascode devices. In [32] TO-220 package inductances were extracted and through simulation, it was found that two inductances (L_{int1} and L_{int3}) that belonged to the gate and power loop of GaN HEMT is the critical inductance in determining the turn-on switching energy loss of the device and the ringing observed during the switching transition. Therefore, another packaging model called the stack-die structure was proposed in [33] which removed the two main critical inductances (L_{int1} and L_{int3}). By soldering the source of GaN HEMT and the drain of Si-MOSFET, the inductance L_{int1} was eliminated. The inductance L_{int3} was also eliminated by connecting the gate of the GaN to the source of the Si-MOSFET directly. Figure 16 (a) and (b) show the internal parasitic inductance and the stack-die structure.



(a) (b)

Figure 16: (a) Internal Package parasitic inductances (b) Internal bonding diagram for Stack-die structure

The new CCPAK provided by Nexperia comes in both top and bottom-side cooling. Figure 15 (c) shows the bottom-side cooling variant. For the CCPAK package, the copper clip technology is used. Where the internal wire bonds are replaced by copper – clips which helps in reducing the parasitic inductances [34]. The reduction of package inductance provided by the copper clip is three times lower when compared to the traditional wire-bonded packages [35]. The packaging of the CCPAK is such that the gate of GaN HEMT is on the bottom side of the die and is connected to the source of the Si-MOSFET through internal pillars as shown in Figure 17. This also helps in improving the dynamic $R_{DS(on)}$ of the device and helps in eliminating the floating substrate which delivers more active cells within the same die.

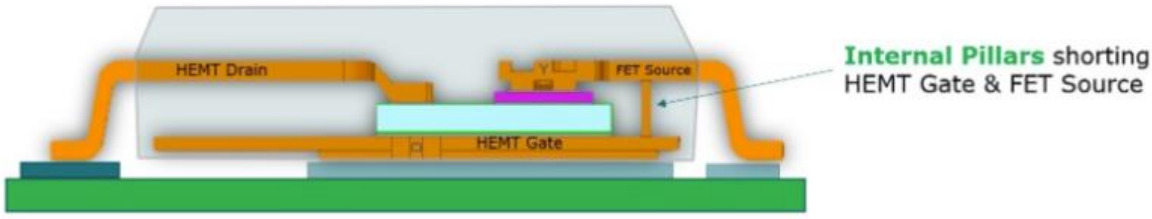


Figure 17: CCPAK internal structure. The Gate of GaN HEMT is at the bottom of the die and connected to Si-MOSFET through an internal pillar [36]

2.3 Gate drive design for Cascode devices

After the packaging of the device comes the next step of realising the characteristics of the packaged devices. Therefore, the next key factor would be to understand the driving requirements for GaN devices. Considering the e-mode GaN, one of the challenges faced in driving them consists of low threshold voltage and the range for maximum allowable voltage is very small. Hence, it is necessary to make sure no spike over the maximum voltage occurs [19]. Due to the fast switching nature of GaN and the lower threshold, false-turn on/off could occur when the device is used for high dv/dt applications. Therefore, a voltage-suppressing network should be put in place to reduce the impact of over-voltage [37], [38].

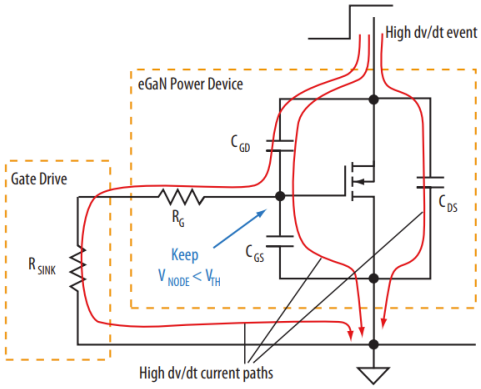


Figure 18: dv/dt effect on E-mode GaN HEMT [38]

Figure 18 shows the dv/dt effect on GaN HEMT. As can be seen from the figure when the high-side device is turned on, the voltage at the switching node of the circuit is changed and a current flows through the miller capacitance (C_{GD}) of the device to the gate. And, when the current is large, then the gate voltage can go above the threshold voltage, which causes a false turn-on of the device. Therefore, a few factors to mitigate this are the correct selection of gate driver, having an active miller clamp, suitable gate drive selection or providing a negative gate voltage [19].

The low threshold voltage of the e-mode can be overcome by using a cascode structure. Also, other e-mode configurations as discussed in Section 2.1.1. Since the gate of the cascode device is Si-MOSFET. Although, cascode devices have a lot of advantages, driving them can be challenging due to their fast-switching nature and high dv/dt. Even though the device has a Si-MOSFET gate, influences coming from the packaging, the internal capacitances along with their fast switching behaviour can have unwanted ringing at the gate causing false turn-on when used in power applications. To characterise any device implementation of a well-designed PCB is necessary. In some cases, the PCB design needs to be implemented with minimum inductance due to the complex internal parasitics of GaN cascode, and a well-designed layout which accommodates the requirements of the device is necessary.

In [31] it was found that the common source inductance is an important part of reducing the gate-source and drain-source oscillations. The observation was made using three different PCBs and each one was designed by reducing the source inductance value and the gate turn-on inductance value. The device used was a GaN cascode from Transphorm. The first PCB 1 had a source inductance of 10.3 nH and the third PCB 3 had a source

inductance of 1.09 nH. Whereas for the gate turn-on, the inductance for PCB 1 was 5.6 nH and the gate turn-on inductance for PCB 3 was 4.4 nH.

From PCB 1 to PCB 3 the peak to peak gate source voltage was decreased by around 18 V. The peak-to-peak gate-source turn-on voltage for PCB 1 was found to be 28.4 V and for PCB 3 was 10.3 V. This goes on to show that, the inductance in the source and gate can severely affect the gate-source voltage oscillations. The same scenario is seen in the drain-source voltage as well. This practice of following low inductance in the gate-to-source path can help in reducing the oscillations which in turn would help in reducing the switching energy losses.

Oscillations are a part of wide band gap switching. A few types and causes of oscillations were identified and listed in [39]. They include False triggering oscillations and false turn-on of the gate source voltage which is caused by high dv/dt and di/dt. Parasitic ringing of the drain to source voltage and the sustained oscillations, which is only applicable to GaN [40]. GaN cascode devices suffer from divergent oscillations at turn-off which is caused by the capacitance mismatch between Si-MOSFET and GaN HEMT [41]. Mentioned are a few oscillations found in GaN devices and a few suppression methods to mitigate is discussed below.

The first and most important way is to reduce the PCB inductances and make the gate and power loop as precise as possible. Another way to reduce the oscillations includes the addition of ferrite beads and snubber circuits. It is common practice to include a ferrite bead at the gate of the device to dampen the oscillations. It is also common practice to place the ferrite bead in the power loop to reduce the parasitic ringing [42]. The advantage of implementing a ferrite bead is that it is easy to place them in a circuit. The disadvantage found in this method is the use of ferrite beads might increase the conduction losses [39].

The other way is to implement an RC snubber circuit. RC snubbers are mainly used to dampen the drain to source voltage ringing. In [43] RC snubber was placed from the gate to the source of the device. The implemented snubber circuit showed a significant reduction in the oscillations seen at the gate of the device. For the GaN cascode, the phenomena of the diverging oscillations can also be slightly mitigated by the use of a snubber circuit [41]. However, the use of ferrite beads was also found to mitigate the turn-off oscillations found in the GaN cascode [44].

Another evolving area for mitigating oscillations is having an active gate driver. A good active gate driver consists of control of gate current, voltage and loop impedance. Even though an active gate driver can increase the complexity of the circuit design, it can help in reducing the oscillations and thus reducing the energy dissipated [39]. In [45] an intelligent gate driver was proposed for SiC devices to suppress the crosstalk. Figure 19 shows how a good active driver can help in controlling various aspects of switching devices.

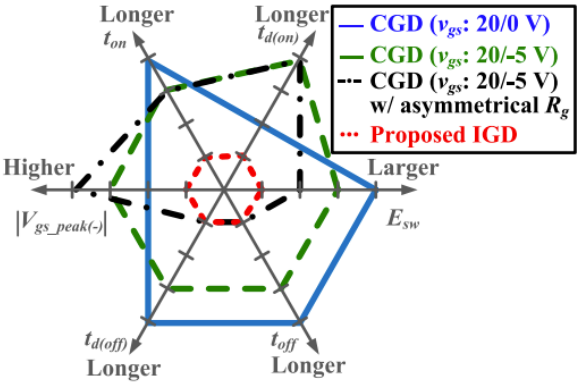


Figure 19: Comparison based on switching performances of different gate drivers [45]

Figure 19 represents a comparison between different conventional gate drivers (CGD) and Intelligent gate drivers (IGD). It can be seen that IGD can achieve smaller turn-on and turn-off times and also minimise the switching losses. As GaN devices switch in the order of nanoseconds, the active gate driver would require a speed that is faster than that, preferably in the order of pico-seconds. In [46] an active gate driver was proposed for GaN where the chip can output a waveform in a very short period. This is done by changing the gate current every 100 ps during the switching of the device.

2.4 Current Collapse Mechanism in GaN

The current collapse phenomenon is the temporary increase in the on-state resistance of the GaN device after a high voltage stress is applied to the device during the off-state. In this section, the physical mechanism of current collapse and the ways to measure using different clamping circuits are explored.

2.4.1 Physical mechanism

Before understanding the current collapse mechanism, knowing about the electric field distribution in GaN devices is necessary. During the off-state of the GaN device, the drain-gate electric field is stronger near the gate edge. This is because of the polarization property of the hetero-structure and also because of charge accumulation at the gate [6], [14]. This uneven electric field, i.e. there is a high electric field at the drain side of the gate edge causes trapping of surface charges. This makes the surface charge to be negative and thus the 2DEG will be depleted. Figure 20 shows the electric field distribution of the device during its off-state.

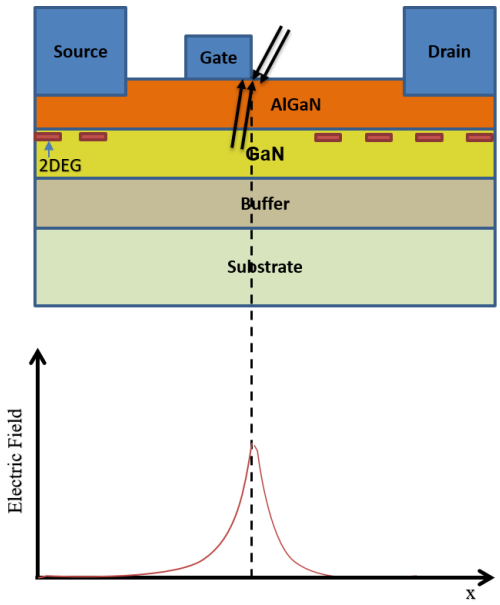


Figure 20: Electric Field Distribution of GaN device during off-state [6]

The current collapse phenomenon can be attributed to two possible reasons one is the virtual gate concept [47] and the other is the trapping of electrons in the AlGaN [48]. The current collapse phenomenon can be seen in Figure 21 and Figure 22. Figure 21 is during the off-state and Figure 22 represents when the device is in the on-state.

The virtual gate concept is such that during the off-state i.e. when a large negative bias is applied to the gate of the device and due to the uneven electric field caused by the hetero-structure the surface charges get trapped in the passivation layer near the gate of the device. This causes the 2DEG to be depleted for a temporary period. When the device is in the on-

state these trapped charges will act as a virtual gate, which increases the resistance between the drain and source [47].

Hot electron trapping – This mechanism is when the hot electrons are injected into the deeper traps of the buffer layer. When a high voltage is applied to the drain and source of the device the hot electrons are injected into the region near the active channel, and this is where the electrons are trapped in the deep defect sites of the device. This mechanism thus reduces the drain current which in turn would reduce the power produced by the device [49], [50].

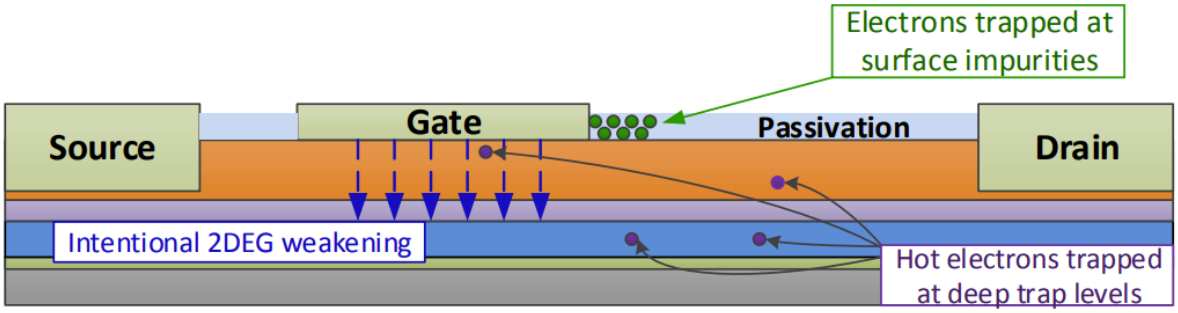


Figure 21: Device during turn-off representing trapping of electrons [51]

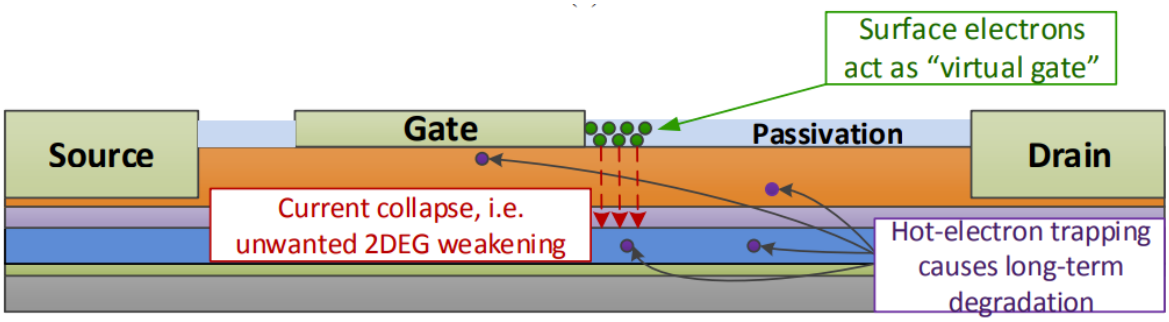


Figure 22: Device during turn-on where the electrons act as virtual gate [51]

Field Plate

One of the ways to mitigate the current collapse is by implementing Field Plates. There are different approaches undertaken by different manufacturers. The gate and the source field plate help to distribute the electric field from the gate edge region.

Figure 23 represents the device under off-state with field plates and the electric field with and without field plates. As can be seen with the field plate the electric field is distributed and with this, the current collapse phenomenon can be suppressed to an extent. As shown in Figure 23 the field plate can be added to both the gate and the source. Another advantage of the field plate is that the Breakdown Voltage (BV) can be improved by alleviating the electric field at the drain. This is because the breakdown voltage of the GaN depends on both the gate and drain electric field [6], [52].

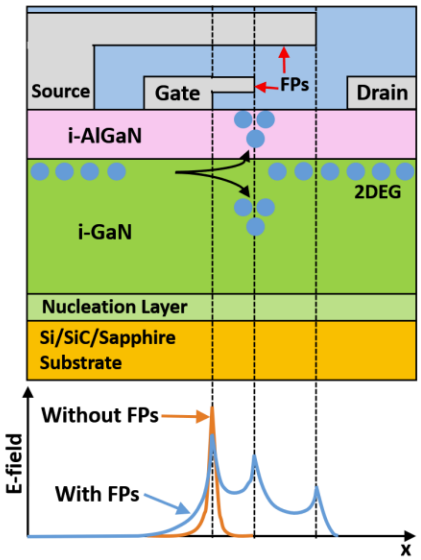


Figure 23: With and without-field plate for device under off-state [6]

2.4.2 Measurement techniques

Measurement of dynamic $R_{DS(on)}$ requires a dedicated clamping circuit because the drain-source voltage switches in the order of hundred volts and to realise the dynamic on-state resistance the voltage needs to be small enough for accurate measurement. This is done so that the oscilloscope channel does not get saturated. As shown in Figure 24, the difference between the drain-to-source measurement and the clamping circuit is significant. The use of a clamping circuit provides a better measurement of the dynamic on-state resistance.

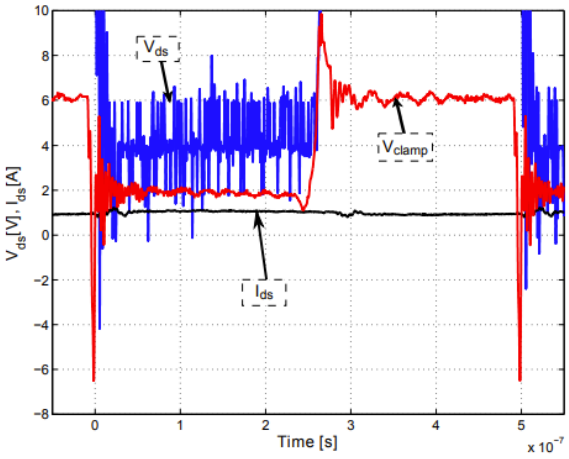


Figure 24: Difference between the clamped voltage, drain to source voltage and drain current [53]

Test method using Keysight Technologies B1505A

A setup for dynamic on-state resistance measurement is provided by the B1505A power analyser. The maximum off-state stress voltage that can be applied is 3000 V and the maximum current that can be measured is 20 Amp. Figure 25 represents the setup used for the measurement. The dynamic on-state is measured during device turn-on after a certain amount of stress time.

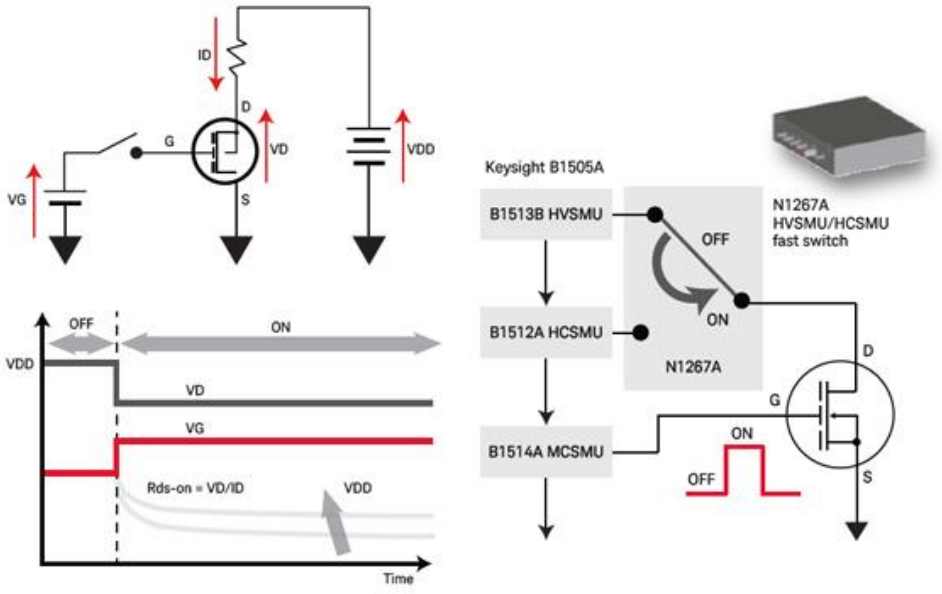


Figure 25: B1505 A dynamic on-state resistance measurement [54]

The High Voltage SMU supplies the 3000 V, but the maximum current the module can provide is 4 mA for 3000 V and 8 mA for 1500 V which is not sufficient for the device. And, the slew rate of HVSMU is 0.4 $V/\mu s$. Which is not fast enough to switch between off and on-state. Therefore, HCSMU is necessary. HCSMU can supply a maximum current of 20 Amp. The switch between HVSMU and HCSMU can be seen in Figure 25. The fast switch switching between HVSMU and HCSMU is synchronised with the switching of the device under test. Switching between the HVSMU and HCSMU can cause a spike which needs to be mitigated. To avoid this spike the module N1267A places a diode in between, as shown in Figure 26 [55].

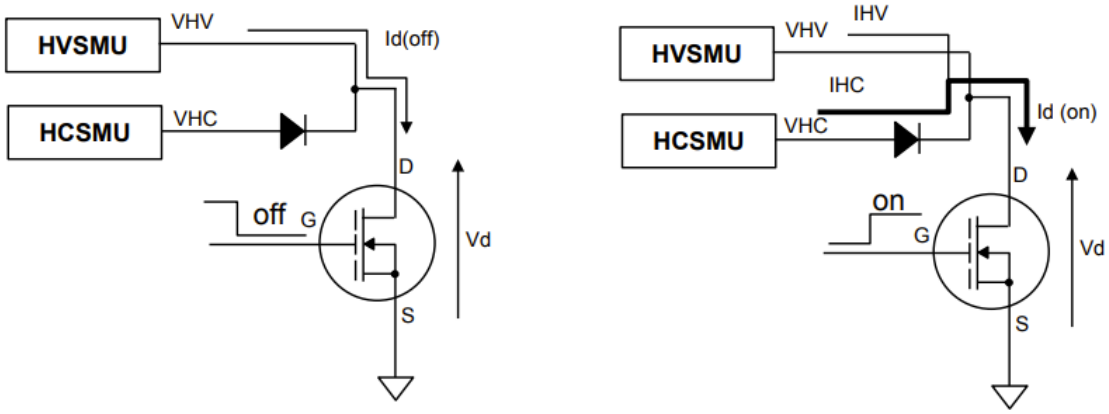


Figure 26: Working of diode switching in N1267A module [55]

When the device is in the off-state, the HVSMU applies voltage stress to the device and the diode is in reverse bias. When the device is turned on, i.e. during the on-state, the drain current starts to flow through the device, and if the drain current is above the maximum allowable current then the device drops HVSMU. And, at this stage, the diode is in forward bias. And, the device under test conducts the current that is provided by the HCSMU. The drain voltage and the drain current are measured and the dynamic on-state is calculated by dividing the measured voltage by the current [55].

The other way to measure the dynamic on-state resistance is the clamping circuit which is usually implemented in a double pulse tester circuit. And, the clamping circuit is usually placed against the drain to the source terminal of the device. Here a few existing clamping circuits are discussed.

The clamping circuit used in this thesis is a version of a circuit presented in [56]. The same research had reviewed a few of the existing clamping circuits. Four clamping circuits were presented in the paper along with the one proposed by the author. The clamping circuit in Figure 27 (a) is the simplest one. The circuit consists of a diode and a resistor, devoid of any external voltage supply. The circuit is connected directly to the drain and source of the device. The drain to source high voltage is limited by the zener diode. The disadvantage of this circuit is that the long RC delay of the V_{DSON} which is because of the resistor which is in series with the zener diode [56]. The circuit in Figure 27 (b) was proposed in [57]. This circuit consists of a p-channel MOSFET, a voltage supply and a resistor. The positive of the voltage supply is connected to the gate of the MOSFET. When the device under test is in the off-state the current flows through the resistor, this causes the potential at the source of the MOSFET to increase till the transistor is turned off. This circuit helps in producing an RC delay of less than 300 ns. Although this circuit can provide a shorter RC delay, the circuit has the disadvantage of suffering from voltage overshoot during the turn-off of the device under test.

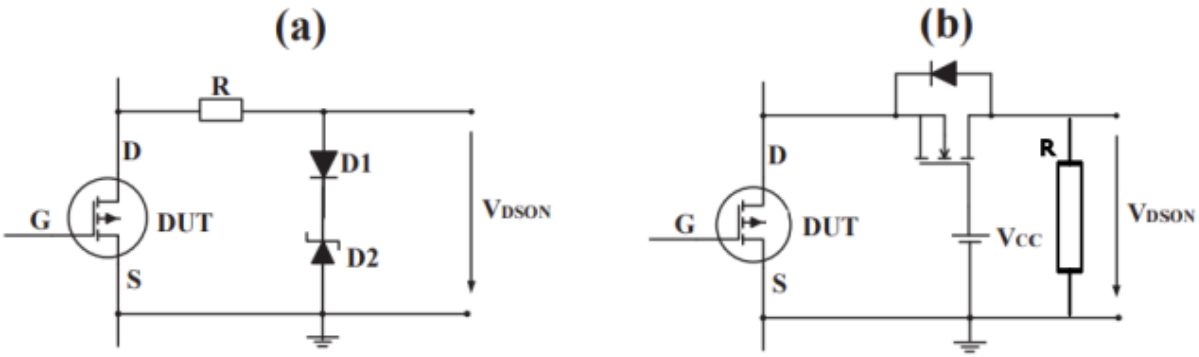


Figure 27: Clamping circuit [56]

The next clamping circuit [58] is represented in Figure 28 (c), this is a combination of the circuits in Figure 27 (a) and (b). The circuit comprises a Silicon power MOSFET, diode and resistor. When the device under test is turned off the source of the power MOSFET is clamped at $V_{cc} - V_{th}$ and when the device under test is turned on the power MOSFET provides a path of low impedance and the V_{DSON} can be measured. However, this circuit still has the problem of RC delay coming from the capacitances of the diode. The clamping circuit shown in Figure 28 (d) was first proposed in [53]. This circuit provides a shorter RC delay time and the circuit is based on the mirror technique approach. The results of the

circuit showed higher accuracy due to the use of fast diodes. One disadvantage of the technique is that; the clamping circuit requires a differential probe for its measurement.

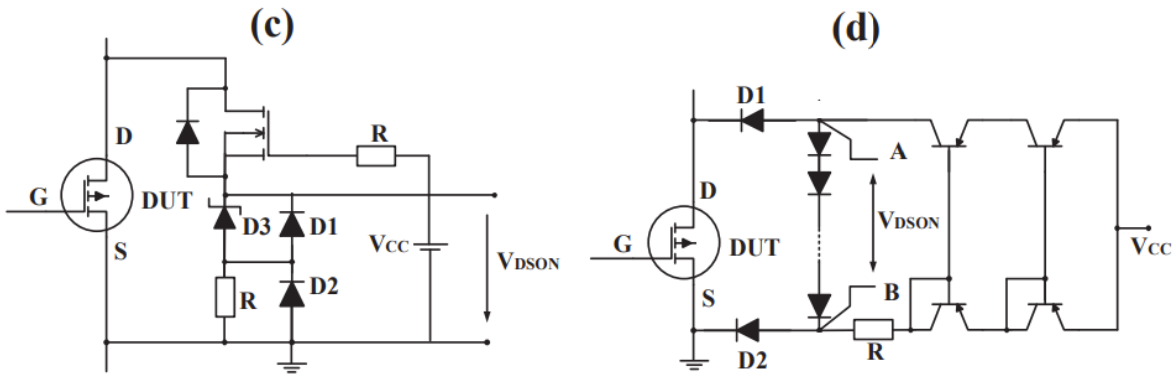


Figure 28: Clamping circuit [56]

In [56] a new circuit was proposed which is based on the SiC Schottky diode. Figure 29 shows the proposed clamping circuit in both on and off state. The main components of the circuit are the SiC Schottky diode making it a simple circuit to realise the dynamic on-state resistance. When the device is in the off-state the current flows through the Diode D1 and charges the capacitor. The capacitor voltage drop is the value of the clamped voltage at terminal V_Z. The clamped voltage is of the diodes D3 and D4.

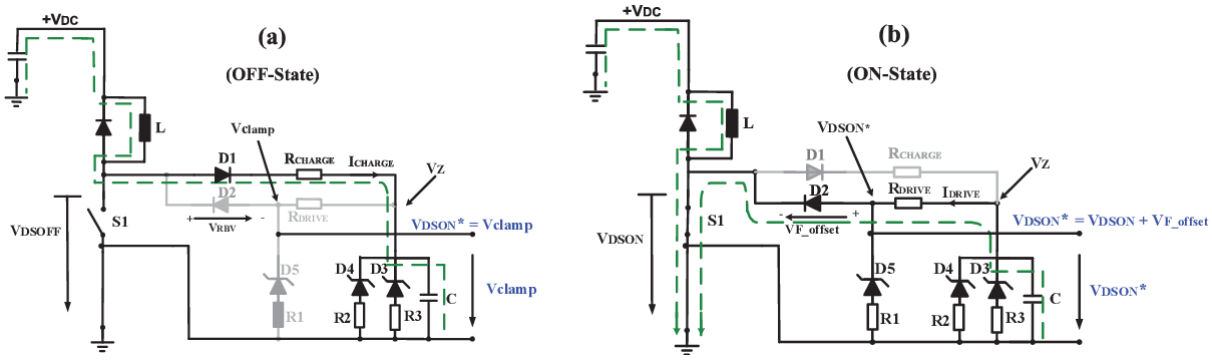


Figure 29: Clamping circuit working in (a) Off-state and (b) On-state [56]

During the device turn-on – when the dynamic on-state resistance is calculated, the capacitor starts to discharge and the current flows to the device through the diode D2. The terminal of the D2 diode is where the on-state voltage is measured, which is represented by V_{DSON}. This value is also an addition of the diode forward voltage. Hence, to realise

the dynamic on-state resistance the diode forward voltage must be subtracted from the whole value.

Chapter 3: Experiment Setup and Methodology

To understand the switching properties of GaN devices, a carefully designed Double Pulse tester is implemented. This chapter details the experiment setup and components used. Correct probing of the oscilloscope probe is discussed, followed by GaN cascode working in a double pulse tester. Finally, two Current Shunt Resistors are compared and the performance of both is evaluated.

3.1 Experiment Setup

The conventional double pulse tester is used for the characterisation of the devices. The gate is supplied with two pulses, where the first pulse determines the device current. The setup consists of devices under test (DUT), four devices are compared with regard to their switching characteristics under various conditions and later their switching energy losses are calculated and compared. There are numerous GaN-friendly gate drivers available in the market. The main parameters for a gate driver include its UVLO rating, isolation rating etc. The gate driver used for this project is from Silicon Labs Si8271BB-IS [59]. The UVLO for the GD is 8 V and the isolation rating is 2.5 kV_{RMS}. The double pulse waveform is provided by a waveform generator. The gate voltage applied is 12 V. As explained in Chapter 2 due to the complex internal circuitry of cascode devices, the gate loop and power loop were carefully designed with minimum inductance. The gate loop consists of two main external resistors $R_{g(on)}$ for turn on and $R_{g(off)}$ for turn off. The gate loop also has a ferrite bead (FB) which is placed close to the device gate. Using an FB can help to dampen the high-frequency oscillations [44]. The power loop consists of the Freewheeling diode, shunt resistor, de-coupling capacitors and an inductor load. During the turn-on transition, the freewheeling diode plays an important part due to its reverse recovery, therefore diode with zero reverse recovery is chosen here. The diode is a Silicon-Carbide Schottky of 650 V with a current rating of 30 Amps [60]. The diode packaging is the traditional TO-247 2-leaded package. The de-coupling capacitors comprise ceramic and power film capacitors. The image of the Hardware Prototype is shown in Figure 31 and the measurement setup is shown in Figure 32.

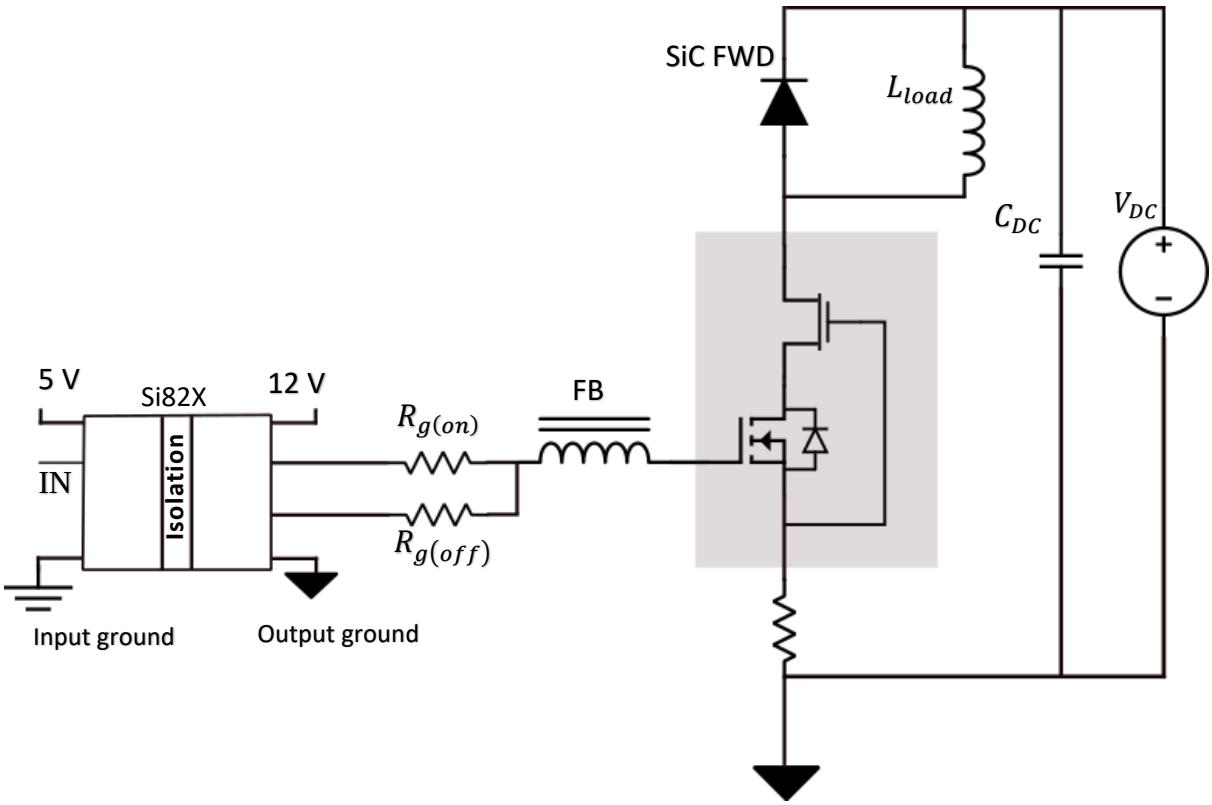


Figure 30: Schematic of Double Pulse Tester

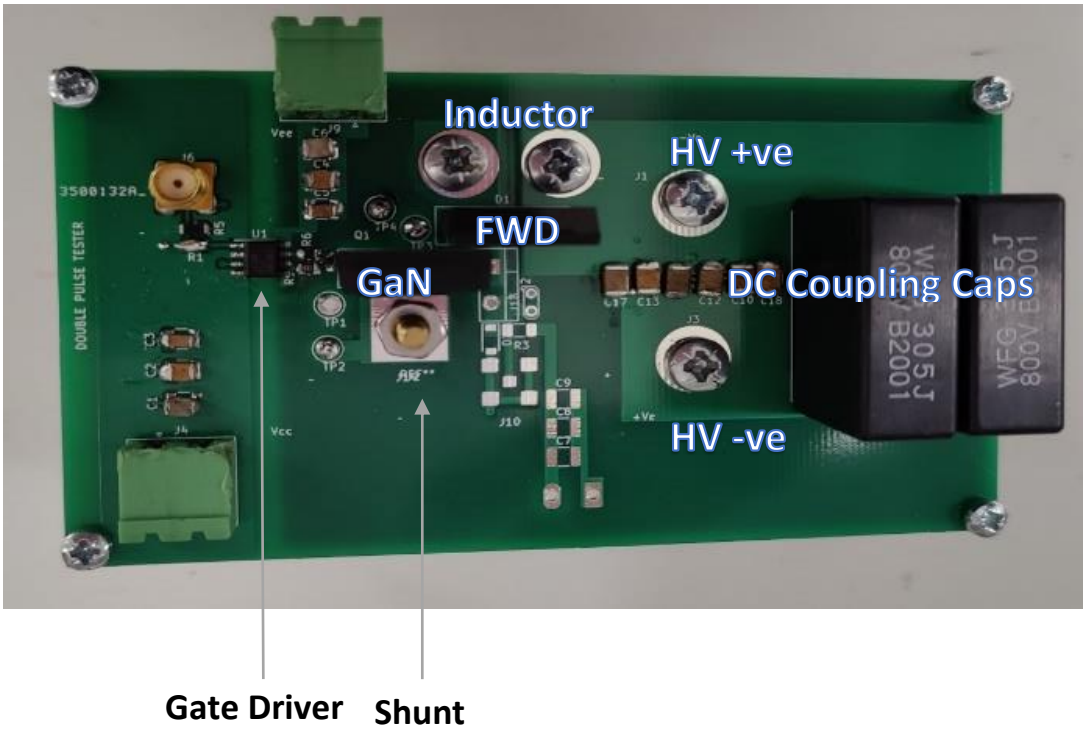


Figure 31: PCB design and components used

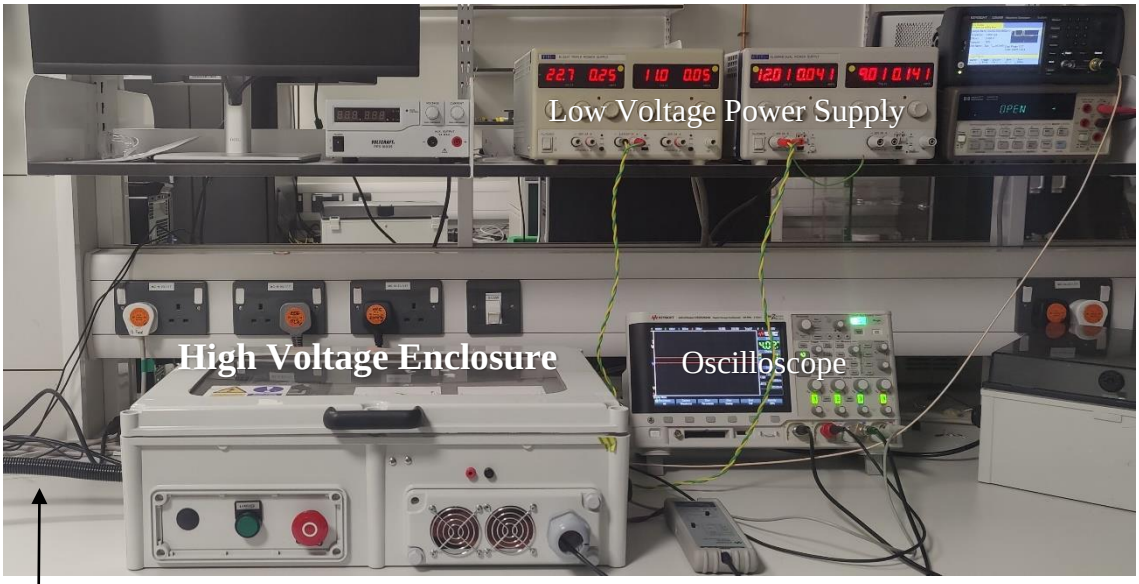


Figure 32: Measurement Set-up

3.1.2 Components used for measurement

Inductor selection

The load selected for the experiment is an inductor load. The inductor is made of Iron Powder Toroid T175-26 with an AL value of 105 (nH/N²). The Inductor is made of 43 turns which gives the value of the inductor to be 200 µH. The pulse width used for different currents are 2.7 µs for 3 Amp, 4.9 µs for 5 Amp, 6.5 µs for 7 Amp, 8 µs for 9 Amp, 8.7 µs for 10 Amps and 9.8 µs for 12 Amp. The pulse widths were adjusted accordingly to obtain the desired load current.

Voltage Measurement

The drain and gate terminal of the device is floating due to the current shunt present in the source-to-ground path. To measure the switching voltage (V_{DS}), it is common to use a differential probe or a passive probe for measurement. Since the switching of GaN devices is in the order of ns. It is a good option to consider a probe that has a higher bandwidth. Therefore, a probe of 300 MHz is used for drain to source voltage measurement. Whereas for the gate to source voltage, a differential probe from Keysight with a bandwidth of 25 kHz is used.

Oscilloscope probing

Signal measurement plays a major role in realising the parameters of the switching waveform. In this case, voltage probing becomes important. The normal long-ground lead will produce parasitic inductance and this will interfere with the probe's internal capacitance which can introduce oscillations in the measured waveform [61]. Therefore, to reduce the impact of inductances while measuring the switching waveform of drain-source voltage ground lead of the passive probe is reduced by replacing the conventional ground wire with a shorter wire [62].

Voltage and current waveform alignment

To calculate the switching energy of the device correct alignment of V_{DS} and I_{DS} is necessary. Using different probes to measure the signals may induce a time delay between them. Therefore, to eliminate the propagation delay between the drain voltage and drain current, a correct skewing mechanism needs to be implemented. The alignment of both signals is done at the turn-on transition of the device [63]. The time at which the drain to source current of the device rises is matched to the time at which the drain to source voltage falls.

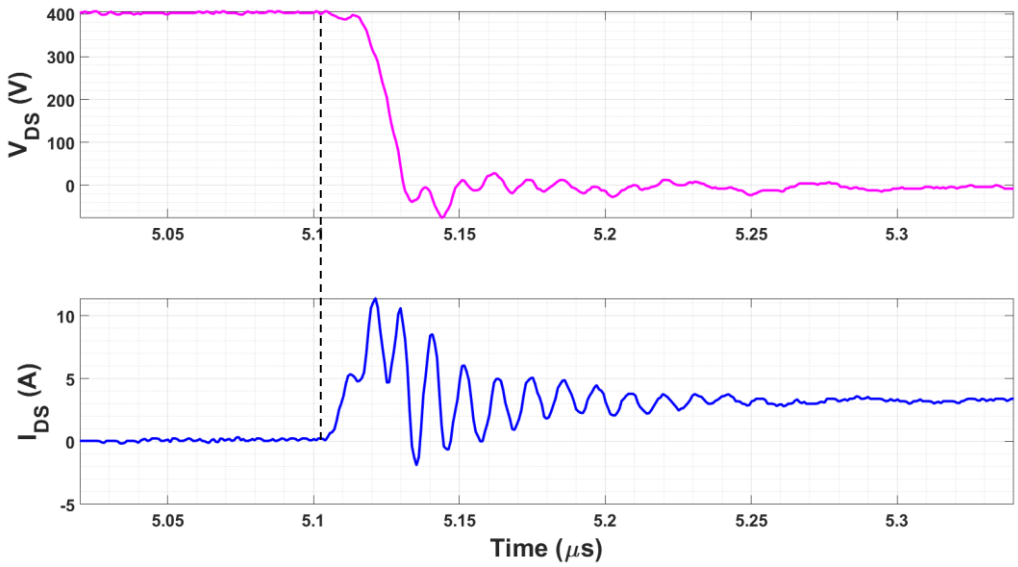


Figure 33: Waveform after Manual De-skew

Current Measurement

As GaN cascode devices are highly sensitive to parasitics, care should be taken to ensure correct measurement practices are put in place. There are many options available to measure drain to source current. E.g.: Rogowoski Coil, Current Transformer, SMD resistors and coaxial shunt resistors. It has become a common practice to use Coaxial shunt to measure high band gap devices due to their higher bandwidth. Although CSR is not suitable for high-side device current measurement. And, in this application, the device is placed on the lower side and for a two-pulse experiment the use of CSR is highly desirable. The shunt resistor used for analysing the drain current is SSDN – 10 from Powertek with a bandwidth of 2 GHz. The shunt is connected to the oscilloscope via BNC cable with a 50 Ohm terminator TA051 from Pico Technology.

3.2 Double Pulse Tester working and equipment used

This section provides a brief overview of the equipment used for the experiment and the devices selected for evaluation. All devices selected have a Voltage rating of 650 V. There are three cascode devices used for comparison concerning their package. The CCPAK cascode devices are provided by Nexperia. All other devices are commercially available.

Equipment	Value
Oscilloscope	Keysight DSOX2024A 200Mhz
Shunt Resistor	SSDN – 10
Differential Probe	Keysight N2791A 25Mhz
Passive Probe	2.5kV 300MHz 1:100 oscilloscope probe
Waveform Generator	Keysight 33500B
Inductor	200 μH
Gate Driver	Si8271BB-IS [59]

Table 3: Experiment equipment used and their parameter

Parameter	**GAN041-650WSB** [64] **(Commercial)**	**GAN039-650NBB** [65] **(Provided by Nexperia)**	**TP65H070G4PS** [66] **(Commercial)**	**SPW47N60C3** [67] **(Commercial)**
Package	TO247	CCPAK	TO220	TO247
Voltage	650 V	650 V	650 V	650 V
Current	47.2 A	58.5 A	29 A	47 A
R_{DSon}	41 $m\Omega$	39 $m\Omega$	85 $m\Omega$	70 $m\Omega$

Table 4: Parameter of the devices investigated

3.2.1 Working of GaN cascode in Double Pulse Tester

In Chapter 2 the operating modes and the working principle of the GaN cascode were discussed in detail. In this section, the working of the device in a DPT is explained. To better understand the switching energy losses of the device, the switching mechanism of the two-die structure is necessary. Both turn-on and turn-off transitions are detailed in this section.

Figure 34 and Figure 35 represent the timing waveform of the device. There are four signals presented here, one is the Si-MOSFET gate to source voltage $V_{GS(Si)}$, next is the gate to source voltage of GaN HEMT $V_{GS(GaN)}$, below that, is the drain to source voltage V_{DS} of the device and finally the drain to source current I_{DS} of the device.

The turn-on transition of cascode

The turn-on transition, as represented in Figure 34, the first instant time T1 is when the gate signal is applied to the device (Si-MOSFET) gate. At this time interval, the gate of Si-MOSFET slowly charges, also the gate-source voltage of GaN HEMT charges. GaN HEMT channel becomes conductive at the time instant T2. At this instant, the drain current I_{DS} starts to increase and the V_{DS} starts to lower. The applied pulse width and the inductor value

will determine the device current, therefore, at instant T3, the device reaches the load current and between the interval T3 and T4, both the reverse recovery charge of the upper device and the inductor current is supported by the device.

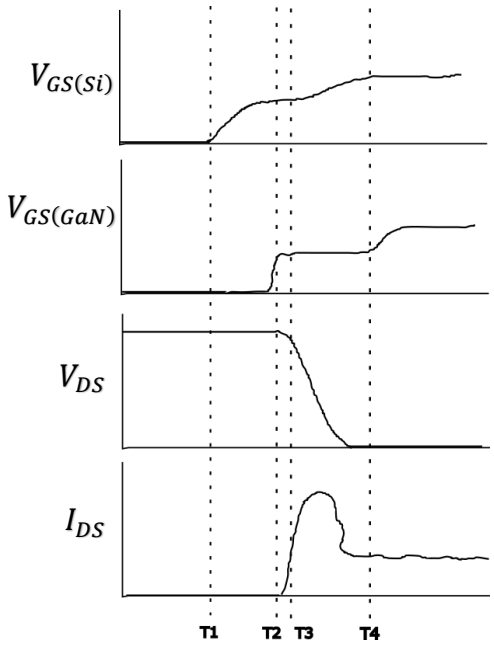


Figure 34: Turn-on transition

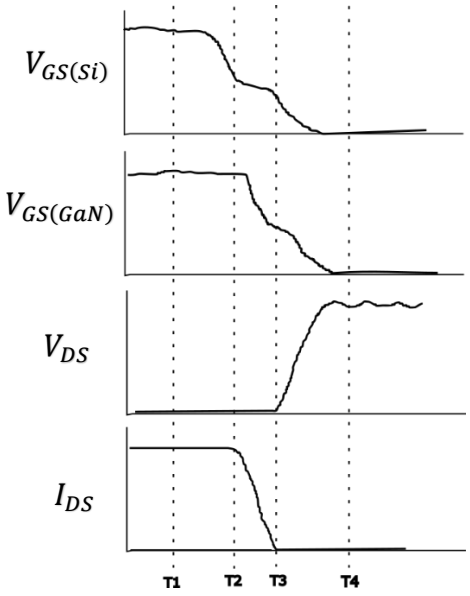


Figure 35: Turn-off Transition

The turn-off transition of cascode

When the gate signal applied to the Si-MOSFET starts lowering to zero, this is represented as time T1 instant. And, MOSFET slowly enters the saturation region. The drain to source voltage starts to increase and the gate to source voltage of GaN HEMT starts to decrease, as a result of this the GaN HEMT reaches the saturation region, this happens at time instant T2. At this instant, the drain to source voltage of GaN starts to increase as well. At instant T3 the GaN falls below its threshold voltage. The load current eventually charges the output capacitors of GaN HEMT and the drain to source voltage of GaN increases to its steady state value [68], [69].

Typical waveforms for a GaN cascode

After understanding the turn-on and turn-off transition. Figure 36 and Figure 37 show typical switching transitions for a cascode device for a drain current of 3 Amp and 12 Amp obtained from the double pulse tester. The switching analysis under different operating conditions will be discussed in the next chapter.

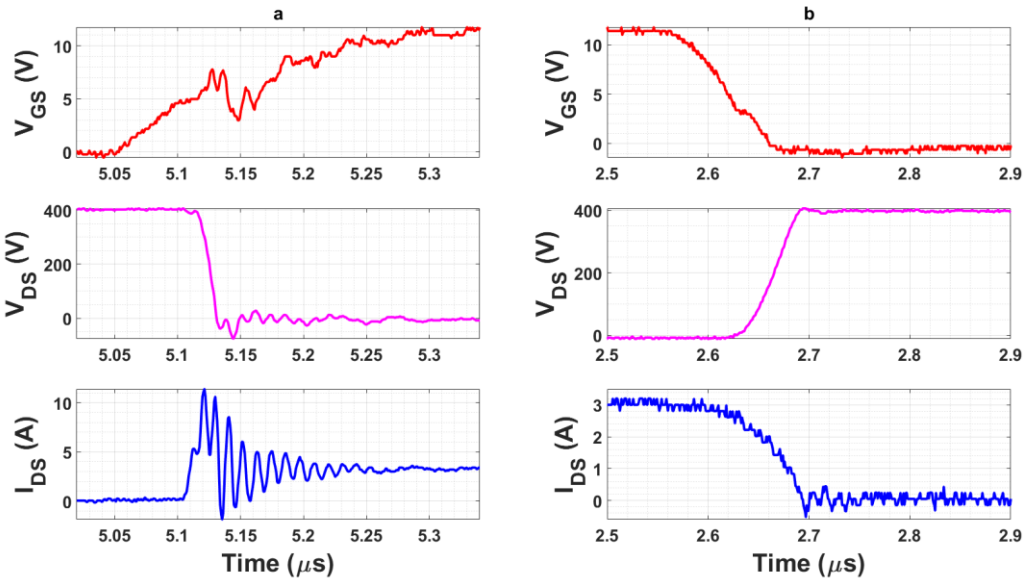


Figure 36: Typical switching transition of GaN cascode device in TO-247 package where the V_{GS} (Red line) is the gate voltage, V_{DS} (Pink line) is the drain to source voltage, I_{DS} (Blue line) is the drain to source current. The switching transition is for 400 V switching voltage and 3 Amp drain current for a $R_G(on) = 30\ \Omega$ and $R_G(off) = 10\ \Omega$.

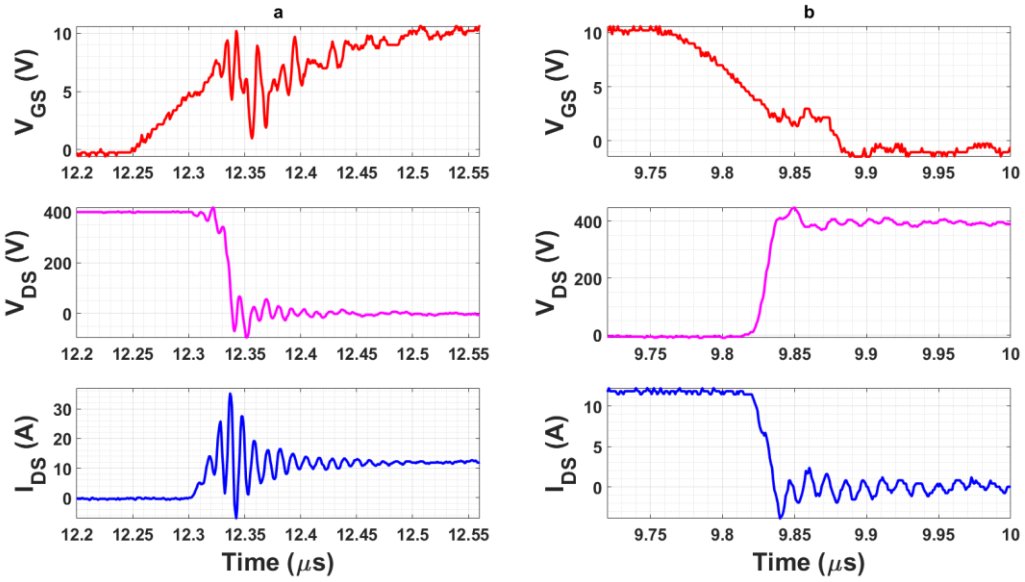


Figure 37: Typical switching transition of GaN cascode device in TO-247 package where the V_{GS} (Red line) is the gate voltage, V_{DS} (Pink line) is the drain to source voltage, I_{DS} (Blue line) is the drain to source current. The switching transition is for 400 V switching voltage and 12 Amp drain current for a $R_G(on) = 30\ \Omega$ and $R_G(off) = 10\ \Omega$.

However, the peak-to-peak measurement of the gate signal was observed to be a bit lower than the peak voltage of 12 V. This could be due to measurement error. The gate-source signal could have been measured with a passive probe. However, the oscillations arising from the components in the power loop path could affect the measurement. Hence, this was avoided and the gate-source measurement was continued with the differential probe.

3.3 Investigation of impact of shunt resistor measurement on switching waveform

In this section, a study of the influence of using two different current shunts namely SSDN – 10 which has a resistance of $0.102\ \Omega$ and SDN-50 having a resistance of $0.5\ \Omega$ in the power-loop of the device is described. Research on implementing CSR on the power path is explained in detail in [70]. The CSR used in the mentioned reference study is SDN-414-025 which consists of two pins – one for input i.e. the Source of the device and the other pin for ground. The study was done for two scenarios one with CSR in the power-loop path and the other without the CSR, and a copper wire was placed instead. The results showed that the CSR introduced a considerable amount of oscillations in the gate to source and drain to source voltage. The device used in the mentioned study was a normally-off e-mode

GaN. GaN cascode devices have internal parasitics which introduce ringing during the switching transition. Therefore, it would be a good idea to understand the effect of CSR in the power-loop path for a cascode device.

For this evaluation, two identical PCBs with different current shunt footprints were designed. The components used for this test are the device under test GAN041-650WSB from Nexperia rated at 650 V and 47.2 A current rating and a passive probe from Agilent 10074C. The shunt as mentioned before is connected to the oscilloscope via a BNC cable. All other equipment such as the waveform generator, oscilloscope and power supply is the same as the ones given in Table 3.

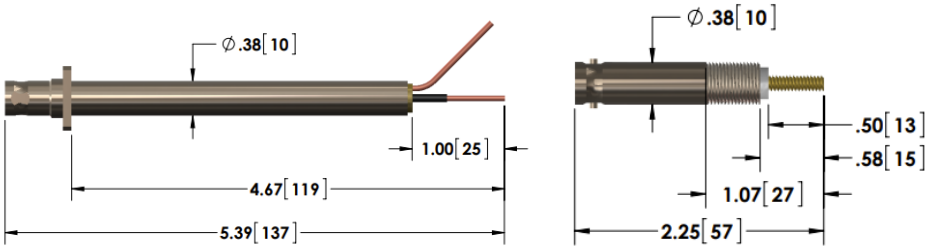


Figure 38: Dimensions of (a) SDN – 50 Shunt resistor [71] (b) SSDN – 10 Shunt resistor [72]

Figure 38 (a) and Figure 38 (b) represent the shunt resistors and their dimensions. The legs of the shunt resistor SDN-50 used were shorter when compared to the one represented here (Figure 38 (a)) And, the inductance between the positive and the negative terminal was measured to be 14 nH. The inductance was measured with the help of a Precision LCR meter - Agilent E4980A. The inductance of SSDN – 10 is measured and provided in [73]. The inductance of the bottom loop of the shunt (which is placed in the power loop) is measured to be 1.9 nH. Figure 39 (a) and (b) represent the snippet from the PCB design for both the shunt resistors. The device footprint and the shunt footprint are shown.

(a) (b)

Figure 39: PCB design for (a) SDN – 50 (b) SSDN – 10

The devices are tested at 250 V drain to source voltage and for a maximum current of 3 Amp. The voltage 250 V is selected to keep the oscillations minimum to avoid large oscillations at the gate and the drain of the device when the shunt resistor of higher inductance is used. For further switching analysis in Chapter 4 and Chapter 5, the devices are tested at approximately 2/3rd of the rated voltage, i.e. at 400 V.

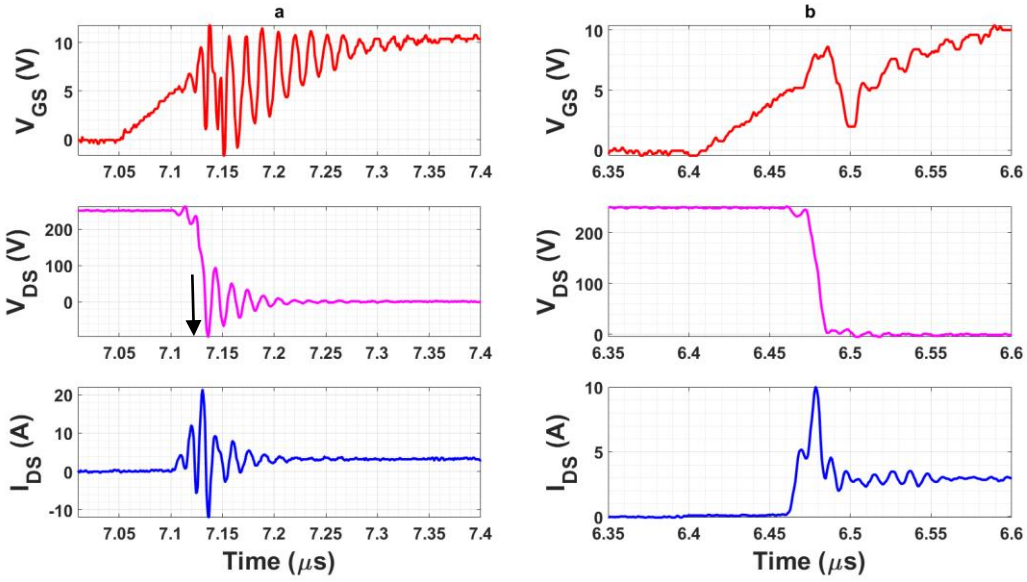


Figure 40: (a) Turn-on transition of GaN cascode using SDN – 50 shunt (b) Turn-on transition of GaN cascode using SSDN – 10 shunt for a device current ($I_{DS} = 3\ A$), $R_{g(on)} = 30\ \Omega, R_{g(off)} = 10\ \Omega$.

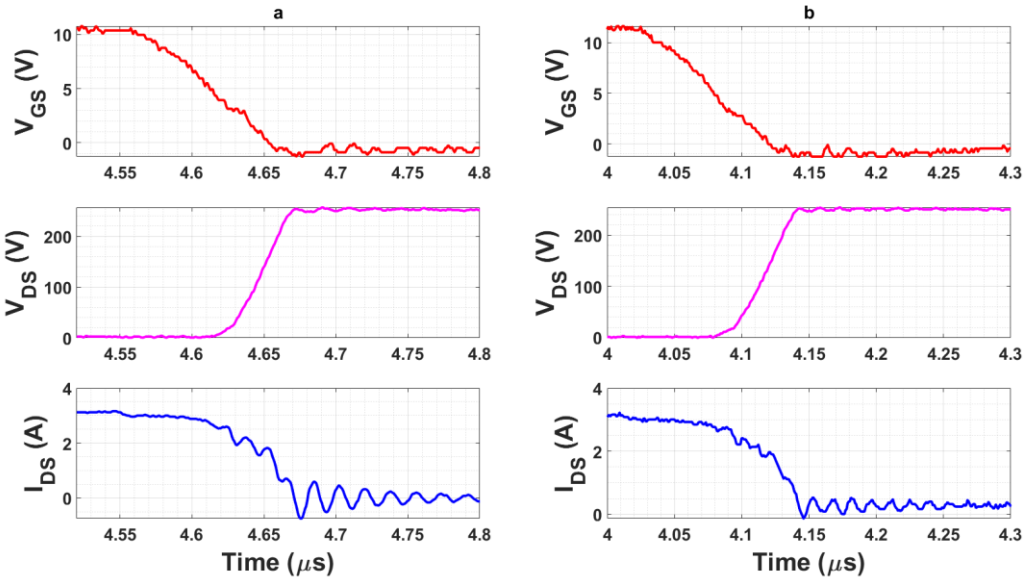


Figure 41: (a) Turn-off transition of GaN cascode using SDN – 50 shunt (b) Turn-on transition of GaN cascode using SSDN – 10 shunt for a device current ($I_{DS} = 3\ A$), $R_{g(on)} = 30\ \Omega, R_{g(off)} = 10\ \Omega$.

Figure 40 and Figure 41 show the turn-on transition and turn-off transition of using both the shunt. Due to higher inductance along the power loop path of the device, turn-on characteristics of the device using SDN – 50 shunt prove to have more oscillations. Figure 40 (b) shows the turn-on for SSDN-10 shunt, the V_{DS} (drain to source) peak-to-peak oscillations are 257 V and peak-to-peak for the other shunt SDN - 50 is 360 V which is an increase of 40.08%. The V_{GS} voltage for the shunt with higher inductance can be seen to have larger oscillations with the signal reaching below 0 V. This can cause a false-turn during device switching.

Where-as the V_{GS} falling edge and V_{DS} rising edge have no significant ringing between both the scenarios except for an increased ringing seen in drain current for SDN-50 shunt. The rise time of the switching voltage using SDN-50 shunt is measured to be 15.9 ns and the rise time when using SSDN-10 shunt is 9.5 ns.

Shunt	Voltage	Current			
		1 Amp		3 Amp	
		$E_{on}\ \mu J$	$E_{off}\ \mu J$	$E_{on}\ \mu J$	$E_{off}\ \mu J$
SDN-50	**50 V**	1.66E-06	8.94E-07	3.30E-06	7.04E-07
	250 V	8.23E-05	6.71E-06	2.83E-05	6.91E-06
SSDN-10	**50 V**	1.15E-06	1.07E-06	1.83E-06	1.20E-06
	250 V	1.44E-05	7.65E-06	1.99E-05	9.26E-06

Table 5: Switching energy comparison using two shunts for 50 V and 250 V at two different drain currents

As discussed in Chapter 2 about the causes of oscillations, the impact of inductances was pointed out. In the above two figures, it can be seen that the influence of the shunt resistor with the lower resistor and inductance provides fewer oscillations when compared to the one with higher resistance. The larger oscillations seen when using the SDN – 50 could be due to the influence of higher inductance arising from the placement of the resistor in the power loop path. As can be seen from the figures of the footprint, the inductance between the positive and the negative of the shunt resistor is 14 nH which is a considerable amount of inductance that can influence the gate and drain source ringing. Therefore, the influence of this higher inductance in the power loop path can bring a significant amount of oscillations that can damage the device gate or cause a false turn-on during the device operation.

Table 5 sums up the switching energy of the device for two scenarios. One uses the SDN – 50 shunt resistor and the other one uses the lower inductance SSDN – 10 resistors. The energy losses of the shunt resistor SSDN – 10 for a few scenarios are lower compared to the other. Especially, the turn-on losses for SDN - 50 are higher than SSDN – 10. The energy loss, therefore, when using the device at a higher current or voltage, while using the SDN – 50 shunt could be higher. Hence, for further switching investigation, SSDN – 10 shunt with lower inductance is used.

3.4 Summary

In this chapter, the experiment methodology and the setup are explained in detail. The components and equipment used are discussed with a brief explanation of why they are suitable candidates for the experiment. Important aspects like voltage probing to get signals devoid of parasitic inductances are explained. After that, the GaN cascode structure working in a double pulse tester is explained using a timing diagram.

Finally, the influence of the current shunt resistor in the power-loop path is investigated first by discussing the previous literature regarding the same. Two similar PCBs with different CSR footprints are designed to accommodate SSDN-10 and SDN-50 shunts. The experiment is conducted for two voltages 50 V and 250 V and two drain currents 1 Amp and 3 Amp. It was seen that the shunt resistor SDN-50 introduces ringing at the gate to source and drain to source voltage, which is not a desirable attribute when characterizing a device. Therefore, the shunt resistor SSDN-10 was found ideal for further analysis of the device.

Chapter 4: Evaluation of Gallium Nitride Cascode devices in different packages

Introduction

The chapter evaluates the switching characteristics of cascode devices in three packages under different operating conditions. The influence of gate resistance and switching current on the oscillation of V_{DS} and I_{DS} is investigated and studied in detail. First, the main two packages are compared in detail and secondly, the three packages TO-247, CCPAK and TO-220 are compared in terms of their switching energy loss.

4.1 Overview of TO247 and CCPAK packages

The two packages investigated here are the TO-247 and CCPAK from the manufacturer Nexperia. One is the traditional three-pin long lead package and the other one is the surface mount package. In the traditional TO-247 package, the two dies i.e. the Si-MOSFET and GaN HEMT are connected via wire bonds whereas in CCPAK the connection is made through copper-clip [74]. This reduces the internal parasitic inductances. Given in Table 6 are the package parasitics of both the devices which were calculated by Nexperia [74].

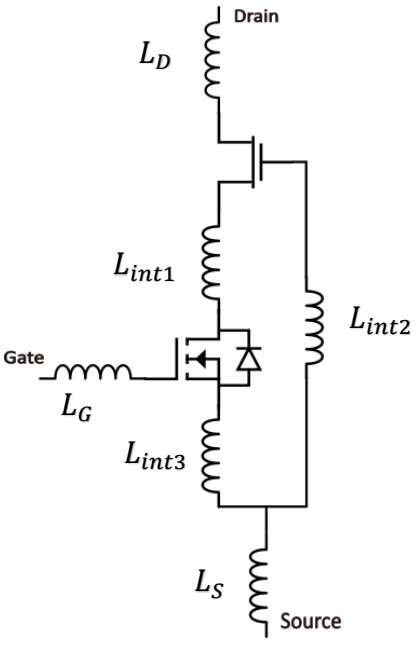


Figure 42: GaN cascode devices internal parasitics

Inductance Value	CCPAK (nH)	TO-247 (nH)
L_G	1.92	8.19
L_D	1.44	5.13
L_S	0.55	5.92
L_{int2}	0.53	1.18
L_{int3}	0.38	0.74

Table 6: Table of package parasitic inductances of two packages The inductances were calculated at a 100Mhz frequency [74]

Figure 42 shows the GaN cascode structure with internal parasitics inductances. Considering the Si-MOSFET parameters, L_S and L_{int3} form the power-loop and gate-loop inductances and these together form the common source inductance of the Si-MOSFET. Previous research has proved the influence of common source inductance during the switching transition and how it is the most critical one [31]. Therefore, this makes L_{int3} the first and most critical parasitic inductance. Parameter $L_{int1}\ and\ L_{int2}$ forms the power and gate loop of GaN HEMT. This makes them the common source inductances of GaN HEMT, making L_{int1} the second most critical parasitic inductance. These two parameters have a significant impact on parasitic ringing during device-switching transitions. Now when the internal parasitics of both the packages are compared, it can be seen that the common source inductance of CCPAK is 0.55 nH and for TO-247 is 5.92 nH which is almost a 90% decrease from the traditional 3 leaded package. This will help in reducing the switching losses significantly. Also, the CCPAK has both top and bottom cooling variations, which would be an advantage for continuous pulse operations to dissipate heat.

4.2 Switching waveform analysis

In this section, the switching waveform of both TO-247 and CCPAK devices are compared and explained in detail. Two identical PCBs were designed to accommodate both footprints. Each PCB was designed to make the gate and power loop as small as possible. As mentioned in Chapter 3, there are two gate resistors, one for turn-on and the other one for turn-off. And, a ferrite bead, which is kept as close to the device as possible. The device is switching at 400 V for a 5 Amp drain to source current. The pulse width is adjusted accordingly to realise the desired drain current.

Figure 43 and Figure 44 show the turn-on transition for CCPAK and TO-247. Each figure is divided into three sections. The gate voltage V_{GS}, the drain voltage V_{DS} and the drain current I_{DS}.The V_{DC} applied is 400 V and drain current I_{DS} is 5 A. An external turn-on resistor of 30 Ohm and an off resistor of 10 Ohm are used. The turn-on transition of the device consists of two parameters, namely the turn-on delay and the rise time – the falling edge of V_{DS}. The definition of rise time is 10% to 90% of the final value of the waveform. And, the same is applicable for the fall time as well.

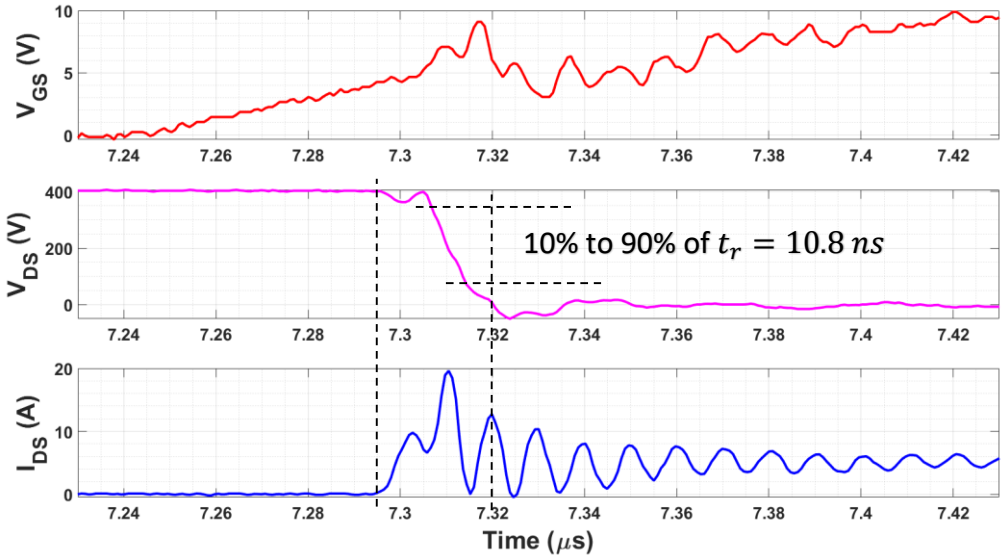


Figure 43: Turn-on Transition for CCPAK package at $R_{g(on)} = 30\Omega$ and $R_{g(off)} = 10\Omega$, $I_{DS} = 5\ A$

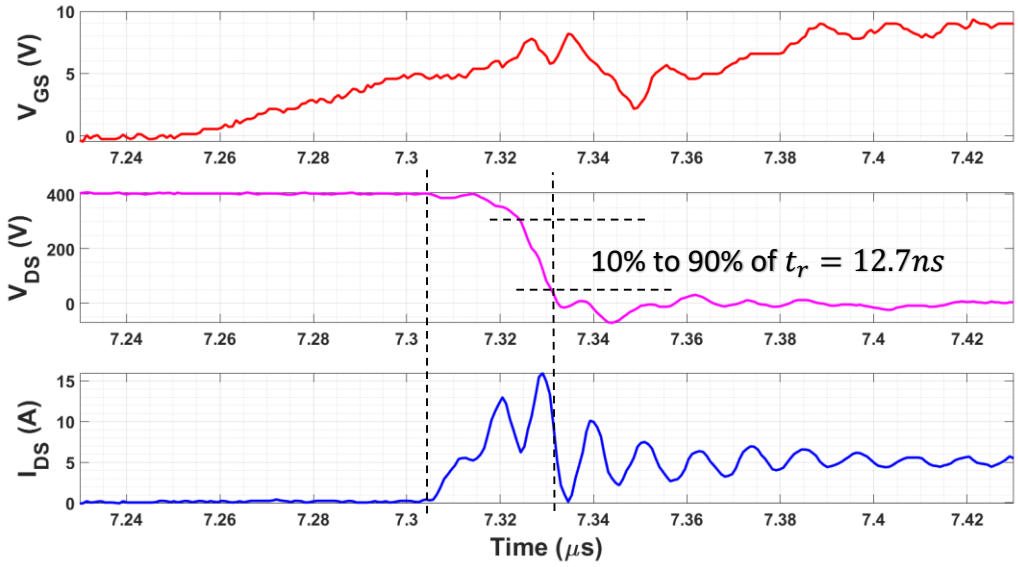


Figure 44: Turn-on Transition for TO247 package at $R_{g(on)} = 30\Omega$ and $R_{g(off)} = 10\Omega$, $I_{DS} = 5\ A$

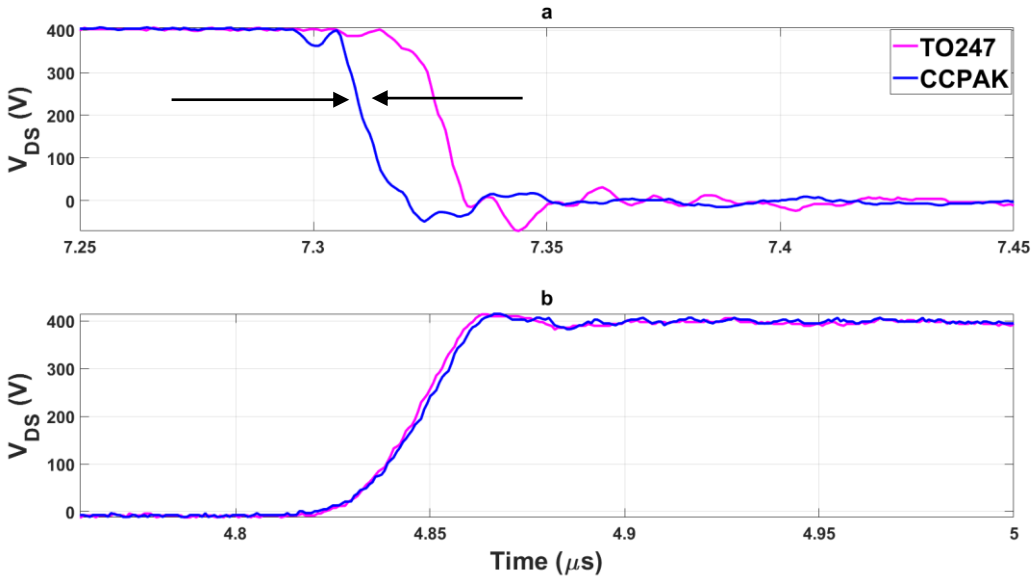


Figure 45: (a) Device turn-on for CCPAK and TO247. (b) Device turn-off for CCPAK and TO247

The device switching voltage of both packages was synchronised and put together for comparison. The V_{DS} rising edge for CCPAK has a peak to peak $V_{DS(pk-pk)}$ voltage of 458 V and for TO-247 the peak-to-peak voltage is observed to be 478 V. This is almost 4% decrease in peak to peak voltage when compared to the traditional TO-247 package.

Also, from analysis of the transition time for both the packages, the rise time (turn on transition V_{DS} falling edge) for CCPAK is 10.8 ns which is approximately 18% lower than TO-247, which has a rise time of 12.7ns. Whereas the fall time (turn off - V_{DS} rising edge) of CCPAK in certain cases is a few nanoseconds higher than TO-247. In this scenario the fall time for TO-247 is 25.6ns and for CCPAK is 28.4 ns. The dv/dt for the switching waveform i.e. the rate of change of drain to source voltage with respect to the change in time during that interval was calculated by considering the 37.5% and 75% of the total waveform. The rise time and fall time dv/dt calculated for CCPAK is 35.7 $kV/\mu s$ and 14.8 $kV/\mu s$. And for TO-247 is 35.2 $kV/\mu s$, and 15.5 $kV/\mu s$ respectively.

4.3 Analysis of double pulse switching at different Drain Current

Both devices were tested at different drain currents (current 3 A, 5 A, 7 A, 9 A, 10 A and 12 A) for a DC voltage of 400 V. The transition time and switching energy loss for different currents are calculated and analysed.

4.3.1 Transition time and dv/dt analysis

Figure 46 represents the transition time for both the packages for different drain currents for three different gate resistors ($R_{g(on)}$) 15 Ω, 22 Ω and 30 Ω and off gate resistor ($R_{g(off)}$) 0f 10 Ω. All measurements were conducted at room temperature. The transition time is in the units of ns.

The transition time was extracted from the switching waveform for each drain current at the mentioned gate resistor. For a better understanding of the transition time between two packages, another graph is plotted in Figure 47.

The trend that can be observed here for the turn-on event is that the rise time t_r for both the devices increases with an increase in the drain current I_{DS} for all different turn-on gate resistors. For instance, in the data presented in Figure 47, two packages have been put together for comparison for a turn-on gate $R_{g(on)}$ resistor 30 Ω and turn-off gate resistor $R_{g(off)}$ of 10 Ω. The rise time t_r increase for CCPAK for 3 Amps to 12 Amps, is from 8.06 ns to 13.3 ns which is a 65% increase. And, for the TO-247 package, the same increase is from 11 ns to 13. 7 ns which is a 24.5% increase.

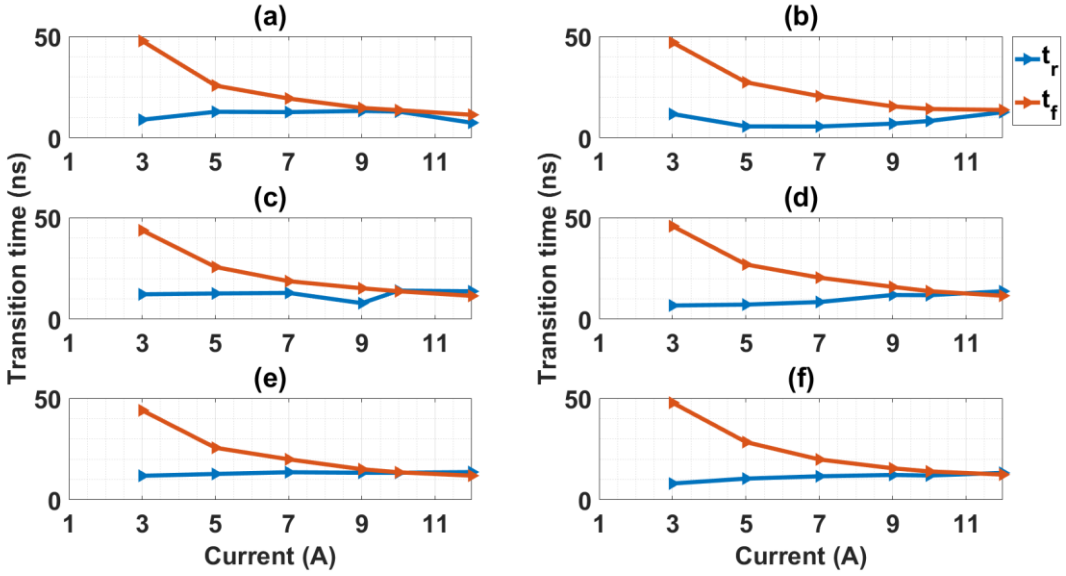


Figure 46: Transition time of both the packages where ***(a)*** *TO-247* $R_{g(on)} = 15\ \Omega$ ***(b)*** *CCPAK* $R_{g(on)} = 15\ \Omega$ ***(c)*** *TO-247* $R_{g(on)} = 22\ \Omega$ ***(d)*** *CCPAK* $R_{g(on)} = 22\ \Omega$ ***(e)*** *TO-247* $R_{g(on)} = 30\ \Omega$ *(f) CCPAK* $R_{g(on)} = 30\ \Omega$. *Where* $t_r = V_{DS}$ *falling edge (Device turn- on) and* $t_f = V_{DS}$ *rising edge (Device turn off - on)*

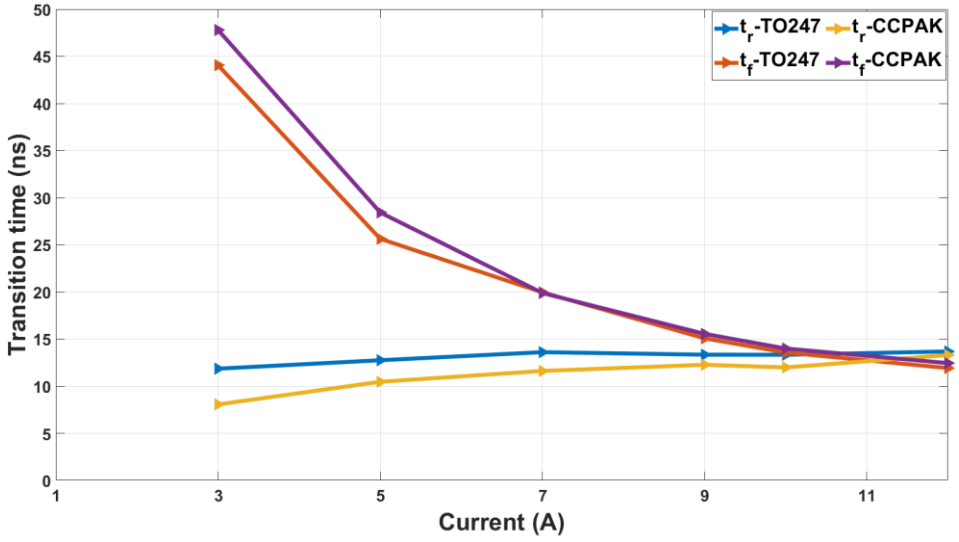


Figure 47: Transition time for both packages at $R_{g(on)} = 30\Omega$ *and* $R_{g(off)} = 10\Omega$ *at varying current from 3 Amps to 12 Amps, where* $t_r = V_{DS}$ *falling edge (Device turn- on) and* $t_f = V_{DS}$ *rising edge (Device turn off - on)*

Whereas for the fall time t_f for the CCPAK for 3 Amp to 12 Amp drain current decreases from 47.8 ns to 12.4 ns which is a steep decrease of 74%. And, the same for TO-247 which has a decrease of 73%, where the fall time lowers from 44.1 ns to 11.9 ns.

As was observed from Figure 45 (b), the fall time for CCPAK is a few nanoseconds higher than the corresponding TO-247. The same can be observed from the data presented here. However, this is only seen for lower drain currents and tends to converge at higher currents. The same is illustrated in Section 4.2. There is much previous research done on oscillations observed in wide band gap devices [39], [75]. The main causes of oscillations as discussed in Chapter 2 include drain to source parasitic ringing, false-turn-on of gate voltage etc. As the rise time of the GaN cascode is switching in the orders of a few nanoseconds the parasitic ringing of the device especially during the gate turn-on may affect the measurement. It can be observed from the transition time data that at some points the rise time might not follow the trend. This can be confirmed from Table 7, where the dv/dt for both the packages at the selected drain current are presented. However, from the table, it can be seen that the highest turn on dv/dt observed for CCPAK is 49.1 ($^{kV}/_{\mu s}$) and the highest observed value for TO-247 is 39.4 ($^{kV}/_{\mu s}$). Therefore, the turn-on dv/dt percentage increase of the new CCPAK package is 24.6%. The highest observed turn-off for CCPAK is 33.9 $\left(^{kV}/_{\mu s}\right)$ and for TO-247 is 34.2 ($^{kV}/_{\mu s}$).

As can be observed from Table 7, there is a clear trend in terms of slew rate controllability using the gate resistance for a particular drain current. Although, at certain currents and gate resistors, the rise time t_r i.e during the turn-on the dv/dt fluctuates for different drain currents, this could be due to the resonant circuit formed by the gate resistor, the ferrite bead and the internal capacitances and package inductances of the device. This causes ringing even at higher gate resistors.

Resistor (Ω)	Drain Current (A)	CCPAK		TO-247	
		Turn on $\left\|\frac{dv}{dt}\right\| (\frac{kV}{\mu s})$	Turn off $\left\|\frac{dv}{dt}\right\| (\frac{kV}{\mu s})$	Turn on $\left\|\frac{dv}{dt}\right\| (\frac{kV}{\mu s})$	Turn off $\left\|\frac{dv}{dt}\right\| (\frac{kV}{\mu s})$
15	3 Amp	48.9	0.79	39.4	0.83
	7 Amp	48.7	19.2	27.8	20.5
	12 Amp	28.3	31	32.5	29
22	3 Amp	48.6	0.81	28.1	0.82
	7 Amp	38.7	19.5	39.2	20.3
	12 Amp	19.6	31.5	16.1	29.4
30	3 Amp	48.7	0.81	32.5	0.84
	7 Amp	24.6	12.9	32.7	19.8
	12 Amp	49.1	33.9	38.9	34.2

Table 7 Rise and Fall times along with $\left|\frac{dv}{dt}\right|$ for turn on and turn off

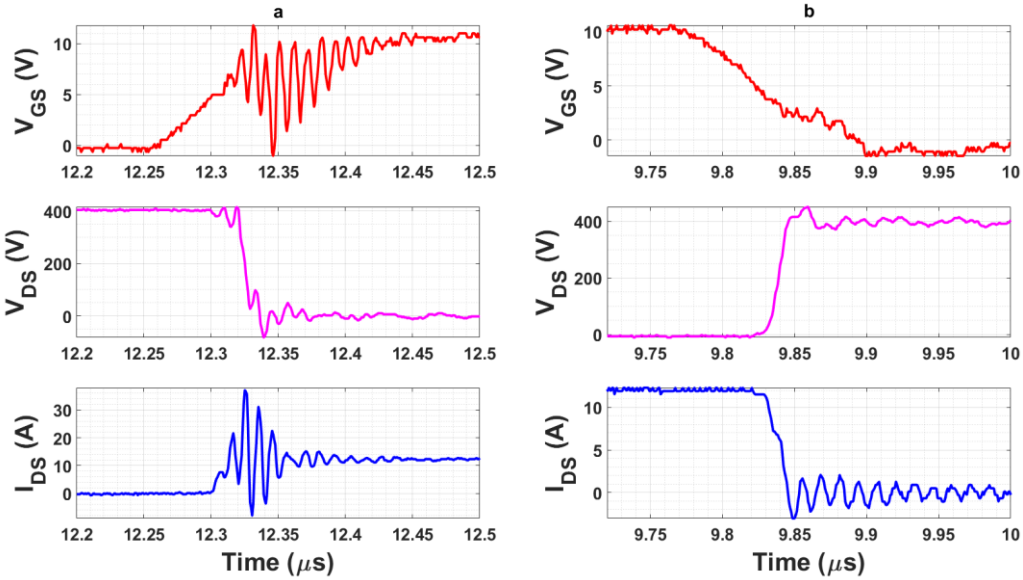


Figure 48: Typical switching transition of GaN cascode device in TO-247 package. $R_g(on) = 15\ \Omega$ and $R_g(off) = 10\ \Omega$.

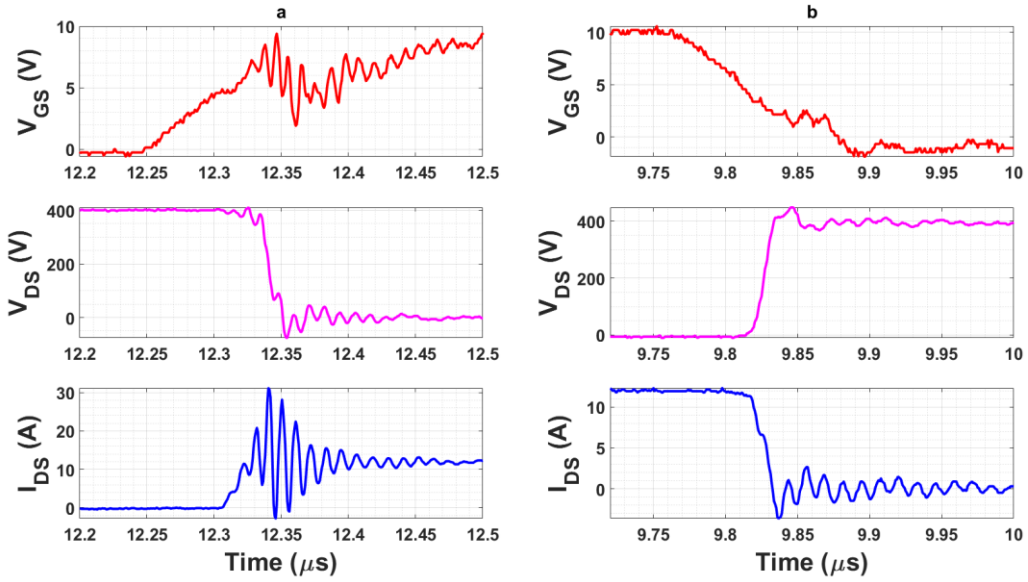


Figure 49: Typical switching transition of GaN cascode device in TO-247 package. $R_g(on) = 39\ \Omega$ and $R_g(off) = 10\ \Omega$.

In [76] it was shown that higher gate resistance tends to increase the oscillations in the power loop switching. In the above Figure 48 and Figure 49 for example, when the turn-on resistor $R_{g(on)}$ is 15 Ω the peak-to-peak voltage of the turn-on drain to source voltage V_{DS} is 498 V and the peak-to-peak voltage of the turn-on drain-to-source voltage for $R_{g(on)}$ 39 Ω is 490 V. Even though the peak-to-peak voltage has reduced with higher resistance, the oscillations for larger resistance are observed to be more than when compared to having a smaller gate resistance. In cascode devices, Si-MOSFET is responsible for the gate. And, the traditional way to control the dv/dt would not be applicable here because the external gate resistance will only actively control the gate of Si-MOSFET [77]. There is very little research done on the slew rate controllability of GaN cascode devices [78]–[80]. As the high voltage GaN switch becomes necessary in controlling the dv/dt the cascode structure makes it unable to do so. One method to mitigate this is proposed in [80] a variable resistor is placed in the path of the gate of the high voltage GaN HEMT. It was shown that by placing the resistor at the gate of the GaN, the turn-on dv/dt of the device had a significant change with an increase in resistor, and, the turn-off dv/dt did not show any effect of having the resistor. Another method to control the slew rate of the cascode device is to implement the direct-drive method. Where the gate of the HEMT is controlled by the gate driver. This method shows that the voltage slew rate controllability can be achieved by varying the gate resistance of the GaN HEMT device [81].

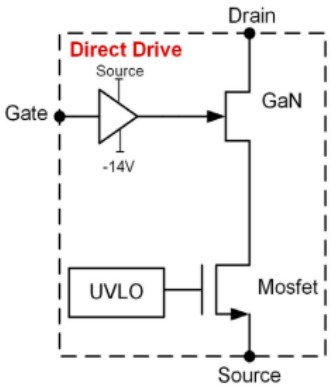


Figure 50: Direct-Drive configuration

4.3.2 Switching energy loss analysis

Similar to the previous section, the switching energy loss is calculated for the same gate turn-on resistors. The energy loss for all three $R_{g(on)}$ resistors is shown in Figure 52. And, in Figure 53 the comparison for both package energy losses for a gate turn-on resistor of 30 Ω and a turn-off resistor of 10 Ω is provided. The energy loss is in the units of μJ. The switching energy loss is the area under the curve obtained by multiplying the drain to source V_{DS} and drain to source current I_{DS}. The trend for turn-on energy can be seen to increase with an increase in drain current. Whereas, the turn-off energy is almost constant and is not affected by the drain current. This is because the turn-off mechanism for the GaN cascode is different. For the turn-off of the device, the GaN HEMT's miller capacitance i.e. $C_{GD(GaN)}$ which is part of the power loop provides the path for gate discharging current. This is much larger when compared to the gate drive circuitry. Therefore, the current flows through the $C_{GD(GaN)}$ directly to the source of the device [82]. This phenomenon helps in reducing the turn-off losses, Figure 51.

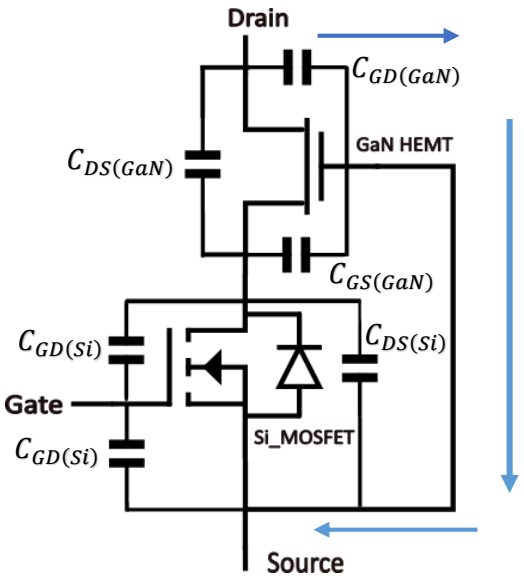


Figure 51: Turn-off current flow mechanism for GaN cascode

Now, comparing the energy loss for both the devices, for instance, considering Figure 53, the turn-on loss for TO-247 increased from 40 μJ to 126 μJ for a drain current of 3 Amp to 12 Amp. And, for CCPAK for the same current 33.8 μJ to 91.1 μJ. There is a decrease of 34.9 μJ energy, which is almost a 27.6% reduction of turn-on losses for CCPAK when compared to TO-247 for a 12 Amp drain current. For turn-off losses, similar to the trend seen for turn-off transition, due to the difference by a few nanoseconds, the same pattern can be seen for turn-off energy loss, at certain drain currents the turn-off losses of CCPAK are higher than TO-247. The turn-off loss for CCPAK for 12 Amp is 14 μJ. And, for TO-247 is 13.6 μJ. When the total energy loss for both of them was calculated, CCPAK was 106 μJ and TO-247 was 139 μJ which is a decrease of 23.7% of losses observed for CCPAK.

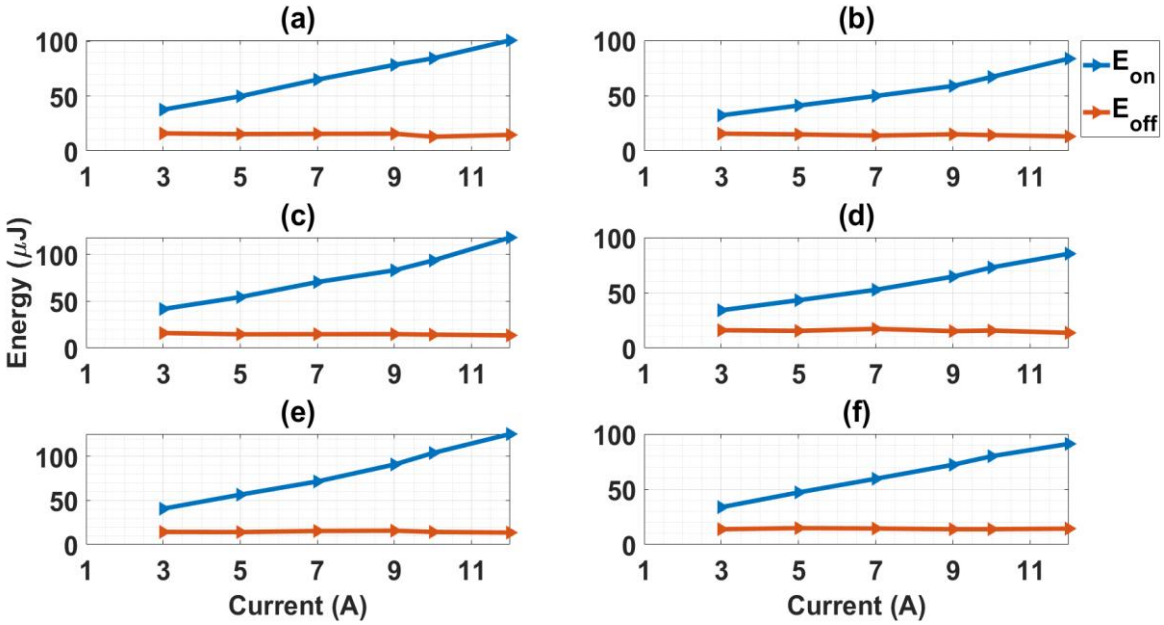


Figure 52: Turn-on and Turn-off Energy of both the packages where ***(a)*** *TO-247* $R_{g(on)} = 15\ \Omega$ ***(b)*** *CCPAK* $R_{g(on)} = 15\ \Omega$ ***(c)*** *TO-247* $R_{g(on)} = 22\ \Omega$ ***(d)*** *CCPAK* $R_{g(on)} = 22\ \Omega$ ***(e)*** *TO-247* $R_{g(on)} = 30\ \Omega$ *(f) CCPAK* $R_{g(on)} = 30\ \Omega$.

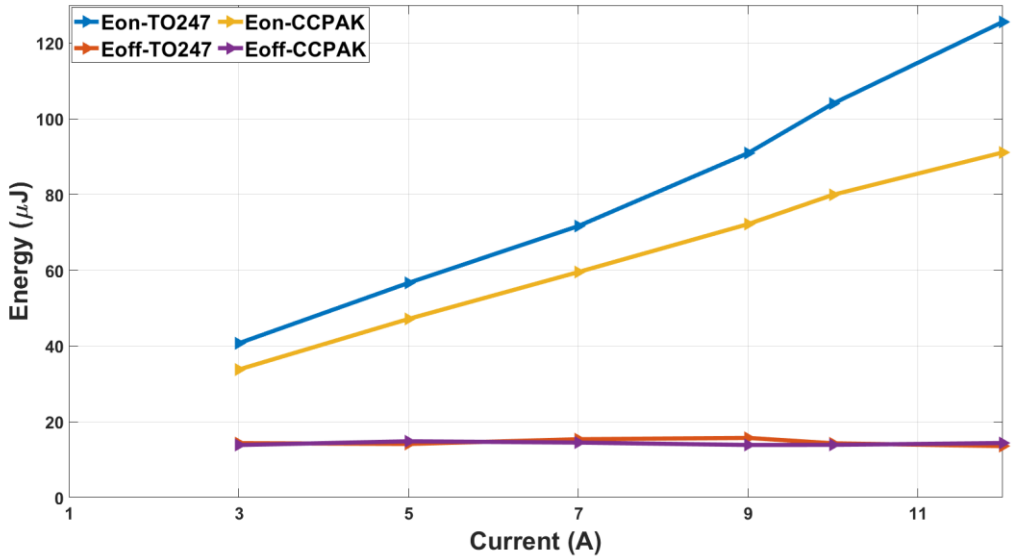


Figure 53: Switching energy for both packages at $R_{g(on)} = 30\Omega$ *and* $R_{g(off)} = 10\Omega$ *at varying current from 3 Amps to 12 Amps*

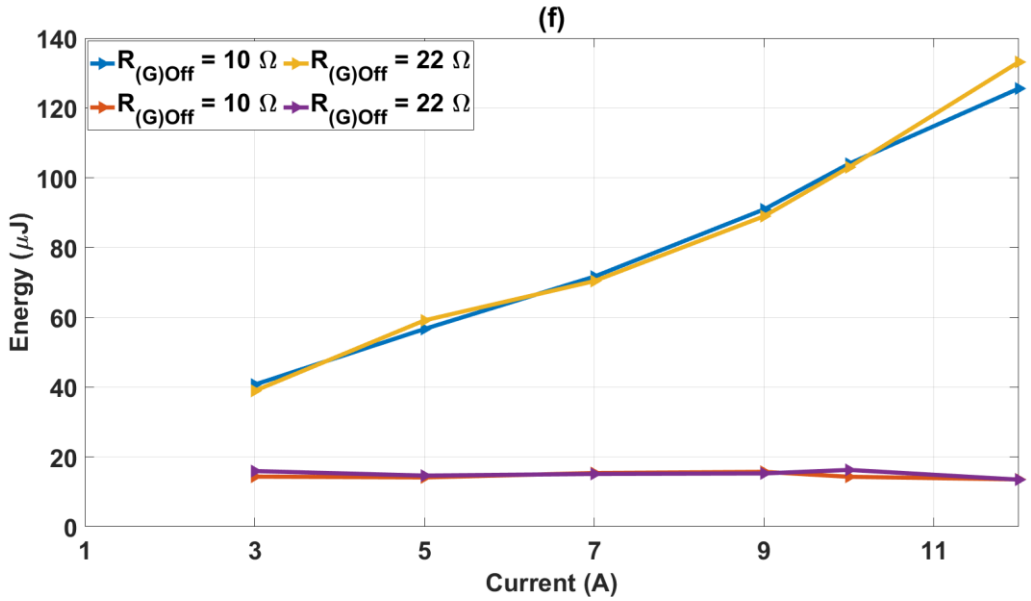


Figure 54: Switching energy for TO247 for $R_{g(on)} = 30\Omega, R_{g(off)} = 22\Omega$ and $R_{g(off)} = 10\ \Omega$ at varying current from 3 Amps to 12 Amps.

Another set of analyses was done for the same drain currents with different turn-off resistors to understand how the change in resistance in the turn-off path would affect the switching energy. Therefore, by keeping the turn-on resistor constant at 30 Ω. It was observed that changing the turn-off resistor from 10 Ohm to 22 Ohm did not have a huge difference in the switching energy loss. Except for a slight increase at 10 Amp and 3 Amp.

4.4 Analysis of double pulse switching at different Gate resistors

In the previous section, the energy analysis for different drain currents was discussed, here turn-on, turn-off and total switching energy of both the packages for different gate resistors for two drain-to-source currents, 5 Amp and 12 Amp is analysed. For this analysis, only the turn-on resistor is increased to see how it may affect the turn-on losses, as it was observed that changing the turn-off resistor doesn't have much effect on the turn-off losses. Figure 55 and Figure 56.

A similar trend seen in Section 4.3.2 is observed here for both turn-on and turn-off. However, while keeping the drain current constant and increasing the gate resistor, it can be observed that the slope of increase of energy loss from 15 Ω to 100 Ω is not so steep [30]. For the TO-247 package, the turn-on energy of the device when a 15 Ohm gate resistor is used is 49.8 µJ and when increased to 100 Ohm the switching energy is 76.2 µJ. For

CCPAK, the increase in energy loss is from 41 µJ to 64.5 µJ. The total energy loss between them at 100 Ohm is a difference of 11 µJ. And, the percentage reduction in energy loss for CCPAK compared to the other package is 15.3%.

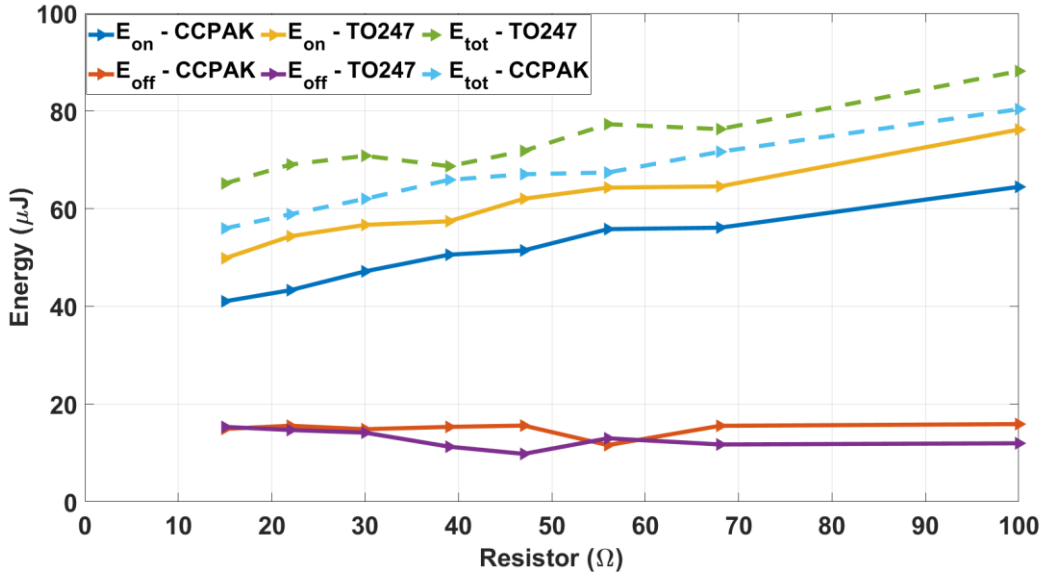


Figure 55: Switching energy for both packages at for varying gate resistor from 15 Ω to 100 Ω at $I_{DS} = 5\ A$

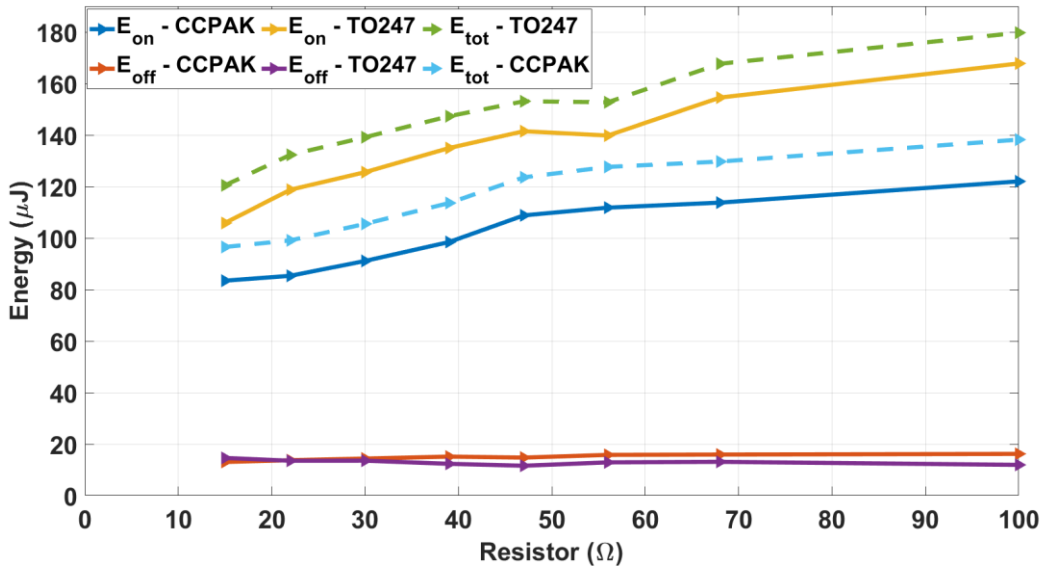


Figure 56: Switching energy for both packages at for varying gate resistor from 15 Ω to 100 Ω at $I_{DS} = 12\ A$

For turn-off energy loss, the trend seems to be almost the same throughout different resistors. [83]. The energy dissipated at 12 Amp drain current during turn off for TO-247

is 11.9 µJ and for CCPAK is 16.2 µJ. And, for 12 Amp drain current, the difference in total energy loss for CCPAK and TO-247 is 42 µJ. Which is a percentage decrease of 23%.

Also, it can be seen in Table 4 – Chapter 3 that the maximum current for the CCPAK is 58.5 A whereas for TO-247 is 47.2 A. Even though both the devices are from the same manufacturers and assuming both device dies are similar – the first page of the datasheet is attached in Chapter 8 - Appendix, the higher current capacity could be due to the better thermal management shown by the CCPAK package. Therefore, to examine just the package-induced losses, the impact of reduced common source inductance (CSI) can be seen in the turn-on losses. The reduced turn-on losses which in turn reflect in the overall energy loss of the CCPAK can be a good conclusion that the incurred losses are due to the package.

4.5 Comparison study between other GaN cascode packages

Chapter 2 discussed the packages GaN cascode devices are available in. In this section, the package TO-220 device performance is analysed and both TO-220 and CCPAK devices are compared to see their performance at different operating conditions.

TO-220 package

The TO-220 package devices have been studied in detail in previous research [32], [82]. The package is commercially available and the Manufacturer is Transphorm. The inductances of TO-220 are slightly higher than the CCPAK due to its long leads but smaller than the TO-247. Table 8 shows the lead inductances of TO-220. From section 4.1 it was seen that the common source inductance of TO-247 is higher than that of the CCPAK, hence the turn-on energy loss of TO-247 was found to be higher than CCPAK. The common source inductance of CCPAK is lower by 85.8% when compared to TO-220. This can have an impact on the turn-on losses, which will be discussed in the coming sections.

Package	L_G	L_D	L_S
TO-220	3.6 nH	2.3 nH	3.9 nH

Table 8: Parasitic Inductances of TO-220 [82]

Switching waveform

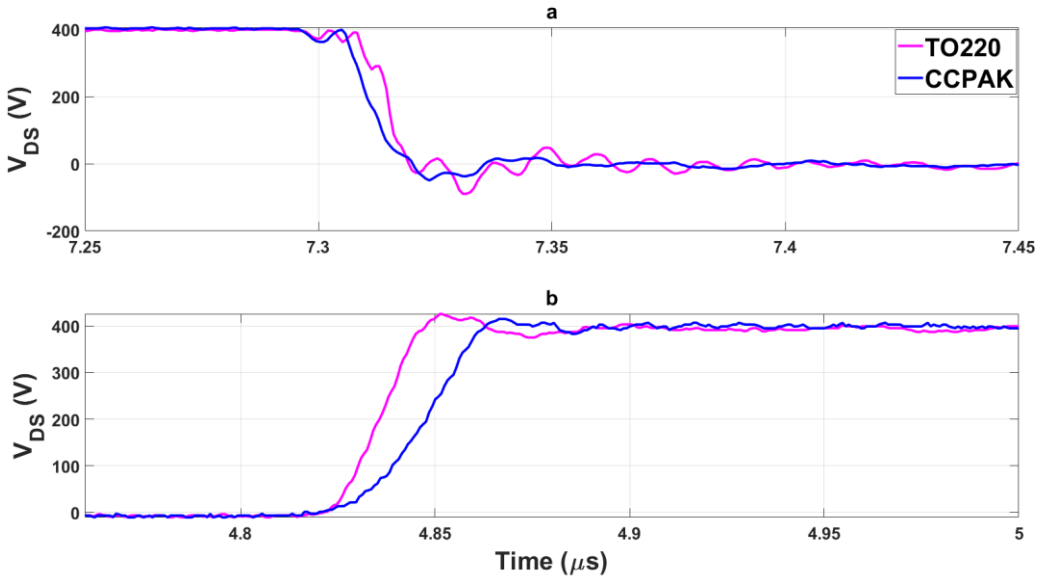


Figure 57: Switching waveform comparison of TO-220 and CCPAK for $R_{g(on)} = 30\Omega$ and $R_{g(off)} = 10\Omega$ and $I_{DS} = 5$ Amp

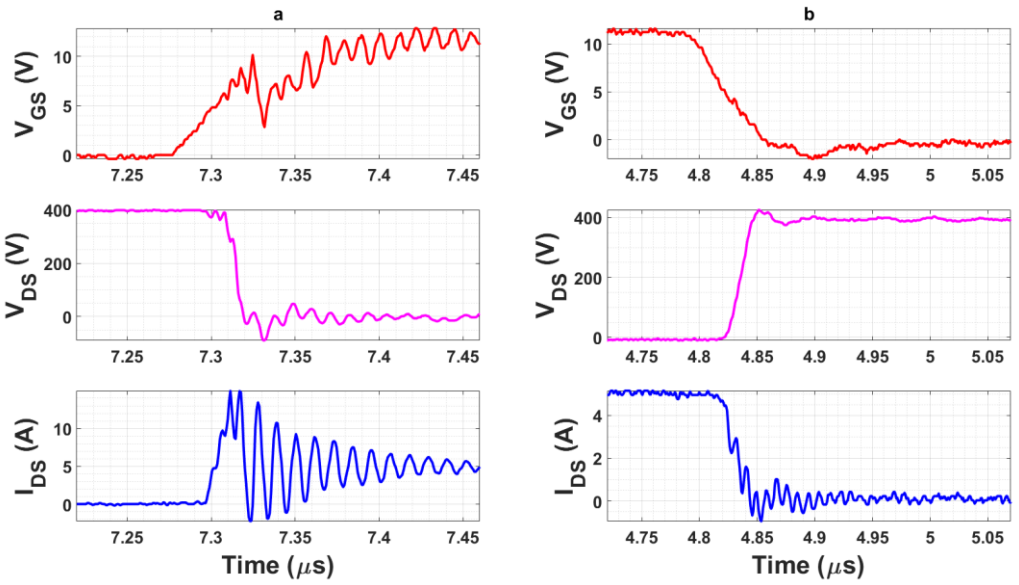


Figure 58: Switching waveform of TO-220 package device where (a) Turn-on transition (b) Turn-off transition

When comparing the switching of both TO-220 and CCPAK, Figure 57, the turn-on transition is faster for the CCPAK due to its low common source inductance, whereas the turn-off is a lot lower than that of CCPAK, although the drain current oscillations are larger

when compared to that of the CCPAK. This can lead to high switching losses at higher currents [82].

Figure 59 shows the energy loss for both the packages. It can be seen that the turn-on energy for TO-220 is higher than CCPAK, which explains the impact of CSI. The switching energy of TO-220 for 12 Amp is 114 µJ and the turn off is 14.4 µJ. The turn-on loss comparison with CCPAK which has a turn-on loss of 91.1 µJ shows that there is a reduction of 25%. But for the turn-off losses, the CCPAK is around 51% higher when compared to TO-220. When calculating the total switching energy loss. It was observed that the total energy loss of TO-220 increased with an increase in drain current. The total energy loss at 3 Amp for TO-220 is calculated to be 43.8 µJ and at 12 Amp is 122 µJ, whereas for the CCPAK at 3 Amp, the total energy loss is 47.6 µJ and at 12 Amp is 106 µJ. The total energy loss at 12 Amp for CCPAK is reduced by 13.1%. Therefore, it can be seen that at higher currents the CCPAK provides better performance when compared to the TO-220 package. A similar trend was observed in [84] where some TO-220 devices had a lower turn–off loss when compared to the SMD device.

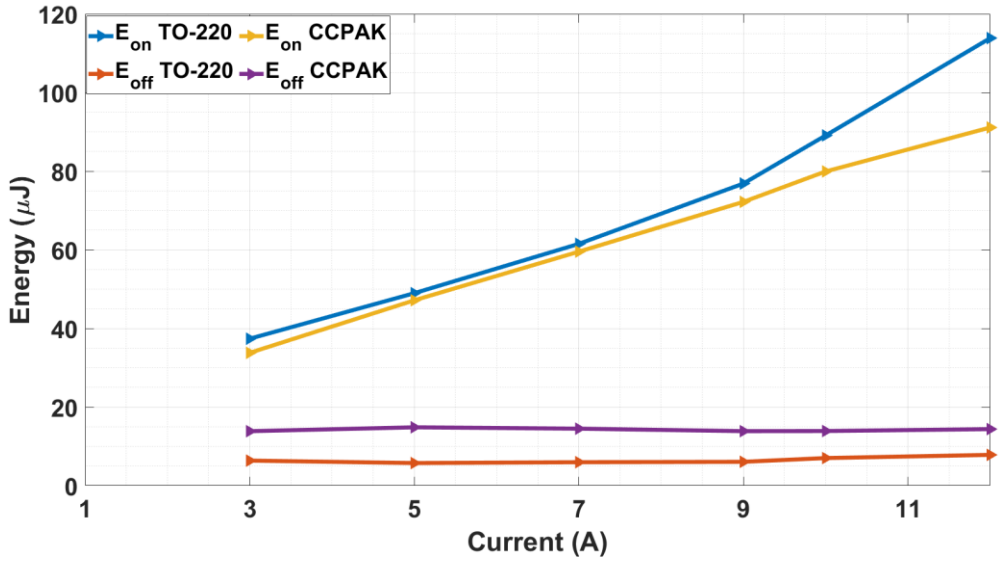


Figure 59: Switching energy comparison between CCPAK and TO-220

Another set of analyses was done to see the effect of higher gate resistance on the switching energy loss of the package TO-220 and is compared to the CCPAK, Figure 60, Figure 61. It can be observed from the graph that for a 5 Amp device current the total energy dissipated at 100 Ohm gate resistor for TO-220 is 65.2 µJ and the total energy dissipated by CCPAK

for 5 Amp is 80 µJ. Which is an increase of 22.6%. And, for a higher current of 12 Amp for a gate resistance of 100 Ohm the total energy dissipated for TO-220 is 145 µJ and for CCPAK is 138 µJ. Which is a decrease of 4.8% in total energy for CCPAK.

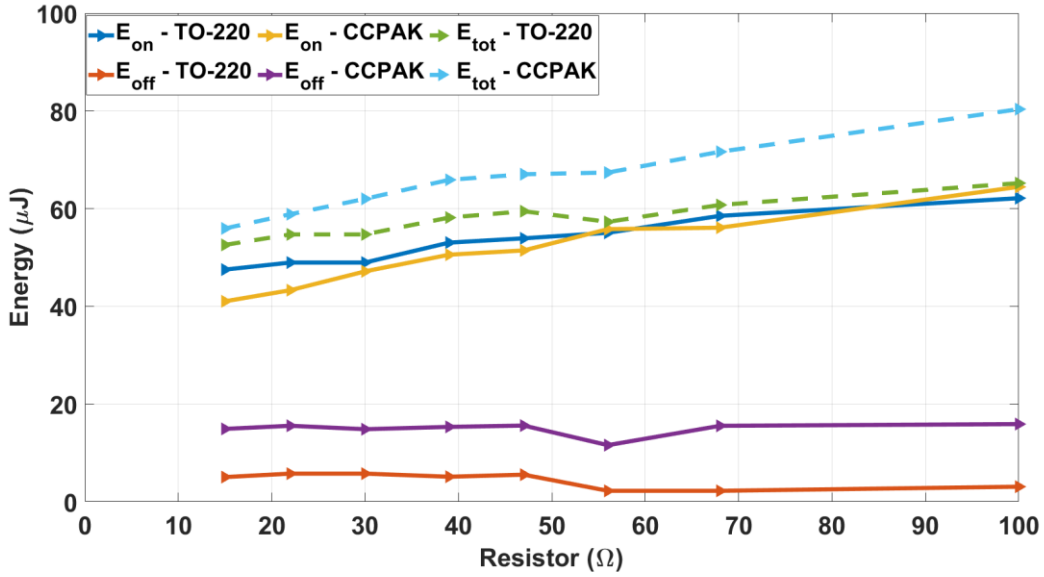


Figure 60: Turn-on, Turn-off and Total switching energy loss for TO-220 and CCPAK for a drain current of 5 Amps and $R_{g(on)} = 30\ \Omega$.

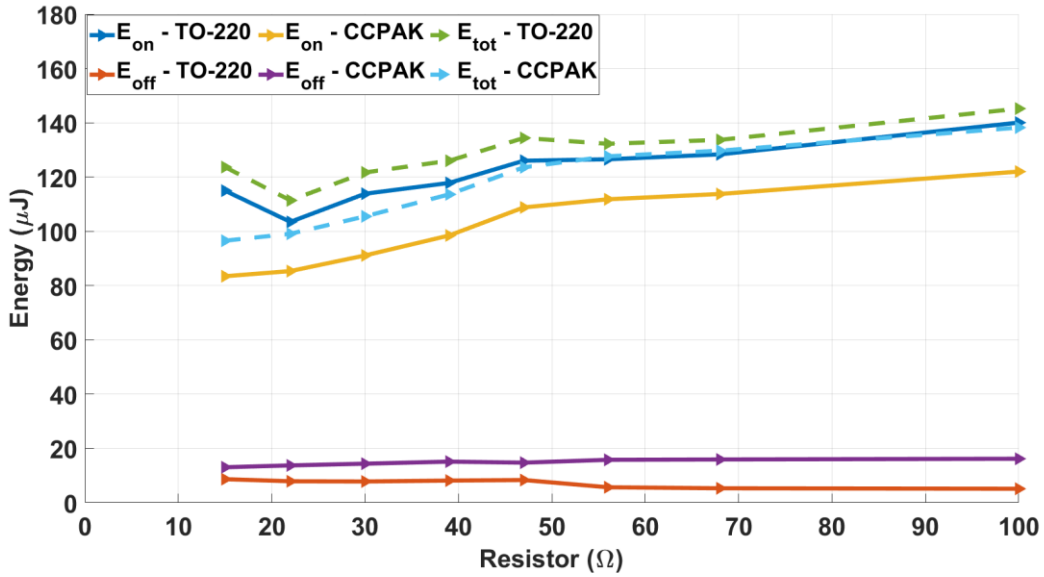


Figure 61: Turn-on, Turn-off and Total switching energy loss for TO-220 and CCPAK for a drain current of 12 Amps and $R_{g(on)} = 30\ \Omega$.

The CCPAK and TO-247 packages are from the same manufacturer whereas the TO-220 is from a different manufacturer. As the devices are from different manufacturers, the comparison between them is purely based on the packaging. Although the turn-off losses for TO-220 are lower at lower currents, this can be due to the differences in the die from two different manufacturers. Comparing just the packaging, the turn-on losses for TO-220 are higher than CCPAK, showing the impact of the Common Source Inductance (CSI).

4.6 Summary

In this chapter, the investigation of GaN cascode in different packages was researched in detail. At first two packages, TO-247 and CCPAK were evaluated. All devices were tested for a 400 V DC voltage. The switching waveform of both the devices were compared and it was observed that during turn-on the CCPAK provided faster switching when compared to the traditional TO-247 package. For turn-off, the fall time for TO-247 was observed to be a bit lower. However, the total switching energy of CCPAK at 12 Amp for a 30 Ohm gate resistor was reduced by a percentage of 23.7% when compared to TO-247. The comparison of switching energy between package TO-220 and CCPAK was also carried out and it was seen that the energy loss for CCPAK was lower at higher currents such as 10 Amp and 12 Amp. The slew rate controllability of GaN cascode devices was also discussed. The device switching analysis was also done for varying turn-on gate resistance, from 15 Ohms to 100 Ohms for all the devices.

Chapter 5: Switching characteristics of Silicon and GaN devices

The first half of the section is focused on the evaluation of GaN cascode devices and Si-CoolMOS device. The devices and their parameter is mentioned in Table 4. The comparison will be based on their switching energy and the switching speed under different operating conditions. The second half is based on building a SaberRD model for a normally-on Polarisation Super Junction GaN device. And, evaluating their switching performances by simulating the device by implementing them in a double pulse tester.

Although much previous research has focused on the superiority of wide band gap devices over Silicon [85]–[87]. In this section, the author has attempted to establish the superior characteristics of GaN devices over Si. Si-CoolMOS package in the traditional TO-247 is used for comparison. Since the drain and source terminals are in different positions when compared to that of the GaN Cascode devices. Another similar PCB was designed to characterise the device.

5.1 Switching waveform

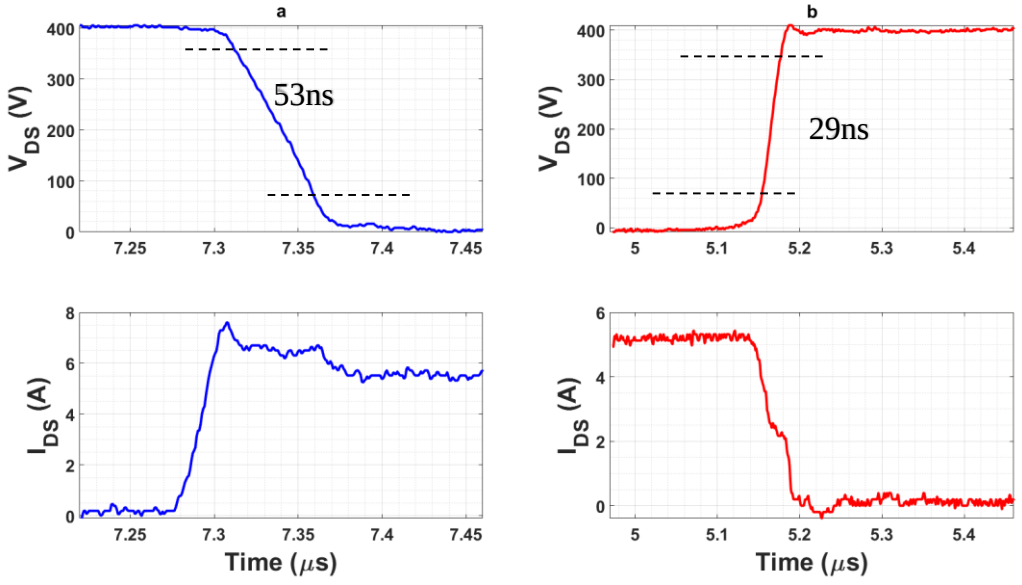


Figure 62: Switching waveform of Si-CoolMOS (a) Device turn-on (b) Device turn-off for a device current of 5 Amp

Figure 62 shows the typical switching characteristics of Si-CoolMOS. As can be seen from the waveforms, there is not much ringing observed at the drain-source voltage or drain-source current. From the figure, it can be analysed that the rise time of the Si-CoolMOS is observed to be 53 ns which corresponds to a dv/dt of 5.9 ($^{kV}/_{\mu s}$), and the fall time, i.e. is the rising edge of the waveform is observed to be 29 ns, where the dv/dt is 13.4 ($^{kV}/_{\mu s}$). In the coming sections, the analysis based on their transition time and energy loss is investigated.

5.1.2 Transition time and dv/dt analysis

Same as the previous section, the transition time is analysed for different drain currents for a gate resistance of 15, 22 and 30 Ohm. For the transition time comparison cascode device in CCPAK is selected.

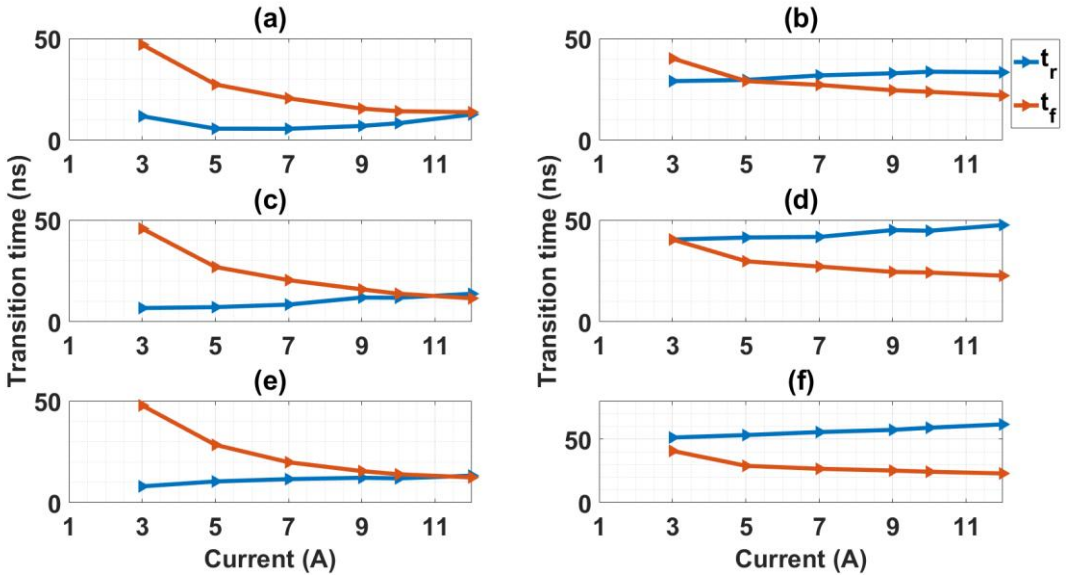


*Figure 63: Transition time of both the packages where **(a)** CCPAK $R_{g(on)}$ = 15 Ω **(b)** Si-CoolMOS $R_{g(on)}$ = 15 Ω **(c)** CCPAK $R_{g(on)}$ = 22 Ω **(d)** S-CoolMOS $R_{g(on)}$ = 22 Ω **(e)** CCPAK $R_{g(on)}$ = 30 Ω (f) Si-CoolMOS $R_{g(on)}$ = 30 Ω*

Figure 63 shows the transition time for different gate resistors and for better comparison, Figure 64 shows the transition time for both devices at 30 Ω. When comparing the turn-on transition, for Si- CoolMOS at 12 Amp the t_r rise time was observed to be 61.6 ns and for CCPAK the same is 13.3 ns. Therefore, the GaN device shows almost a 78% decrease in transition time during turn-on. For turn-off, the fall time t_f for Si-CoolMOS is observed to be 23 ns and for CCPAK is 12.4 ns. This is again a reduction of 46%.

The highest turn on $\left|\frac{dv}{dt}\right|$ observed for Si-CoolMOS is 5.9 ($^{kV}/_{\mu s}$), whereas the highest turn on $\left|\frac{dv}{dt}\right|$ for CCPAK is 65.6 ($^{kV}/_{\mu s}$). And, the highest turn off $\left|\frac{dv}{dt}\right|$ for Si-CoolMOS is 16.8 ($^{kV}/_{\mu s}$) and the same for CCPAK is 33.9 ($^{kV}/_{\mu s}$). This clearly shows that the GaN device exhibits outstanding fast switching results when compared to Si-CoolMOS.

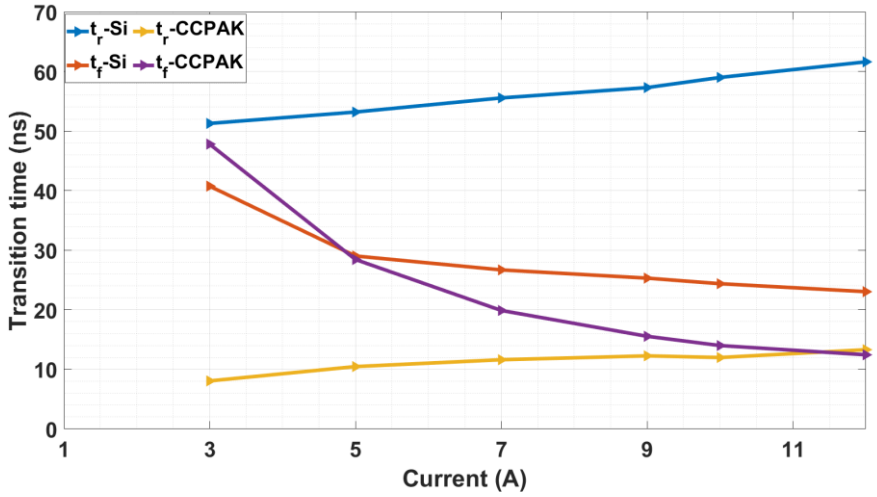


Figure 64: Transition time for both packages at $R_{g(on)} = 30\Omega$ and $R_{g(off)} = 10\Omega$ at varying current from 3 Amps to 12 Amps, where $t_r = V_{DS}$ falling edge (Device turn- on) and $t_f = V_{DS}$ rising edge (Device turn off - on)

5.1.3 Switching energy loss analysis

Here the switching energy losses for CCPAK and Si-CoolMOS are evaluated for the same three gate resistors and varying drain currents.

Figure 65 shows both devices' switching energy data for varying turn-on resistors. Figure 66 provides a comparison of both devices for a turn-on gate resistor of 30 Ω. It can be observed that the turn-on energy increases steeply with an increase in drain current. The E_{on} for Si CoolMOS at 12 Amp drain current is observed to be 340 μJ and for CCPAK is 91.1 μJ which is lower by 248.9 μJ. For turn-off, the increase from 3 Amp to 12 Amp is not as steep as the turn-on energy. The increase of turn-off energy for Si CoolMOS from 3 Amp to 12 Amp is about 86 μJ. And, the increase in total energy for Si CoolMOS when compared to the CCPAK at 12 Amp drain current is about 5.4 times more. This clearly shows that GaN is superior in terms of switching energy loss when compared to Si CoolMOS.

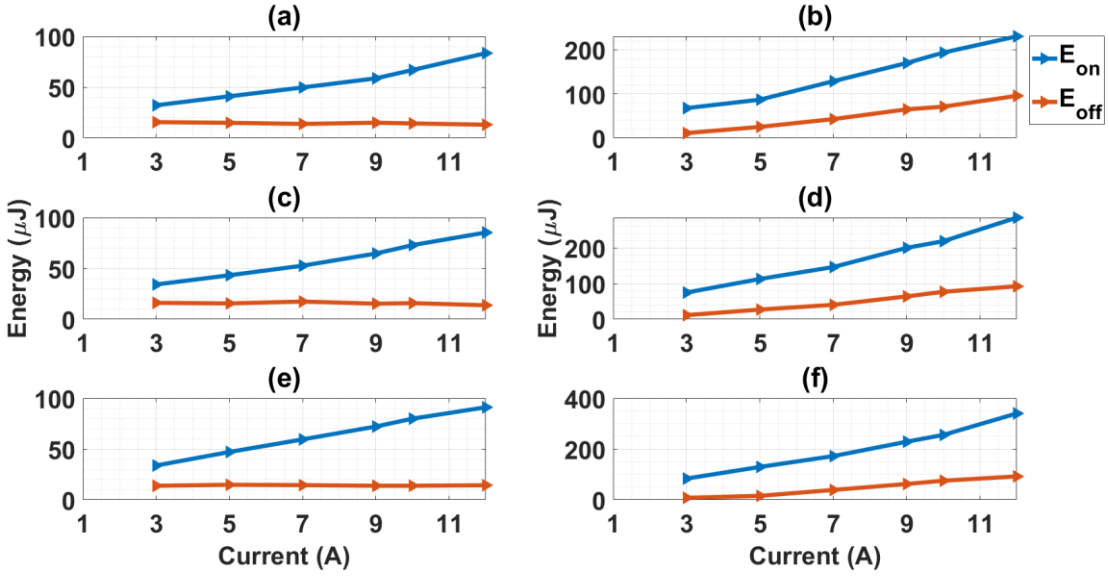


Figure 65: Turn-on and Turn-off Energy of both the packages where ***(a)*** *CCPAK* $R_{g(on)} = 15\ \Omega$ ***(b)*** *Si-CoolMOS* $R_{g(on)} = 15\ \Omega$ ***(c)*** *CCPAK* $R_{g(on)} = 22\ \Omega$ ***(d)*** *Si-CoolMOS* $R_{g(on)} = 22\ \Omega$ ***(e)*** *CCPAK* $R_{g(on)} = 30\ \Omega$ *(f)* ***)*** *Si-CoolMOS* $R_{g(on)} = 30\ \Omega$.

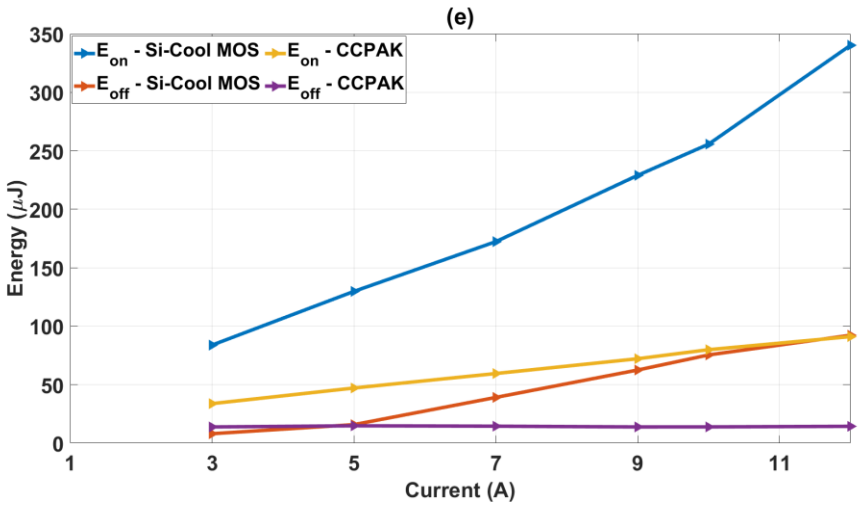


Figure 66: Switching energy for both packages at $R_{g(on)} = 30\Omega$ *and* $R_{g(off)} = 10\Omega$ *at varying current from 3 Amps to 12 Amps*

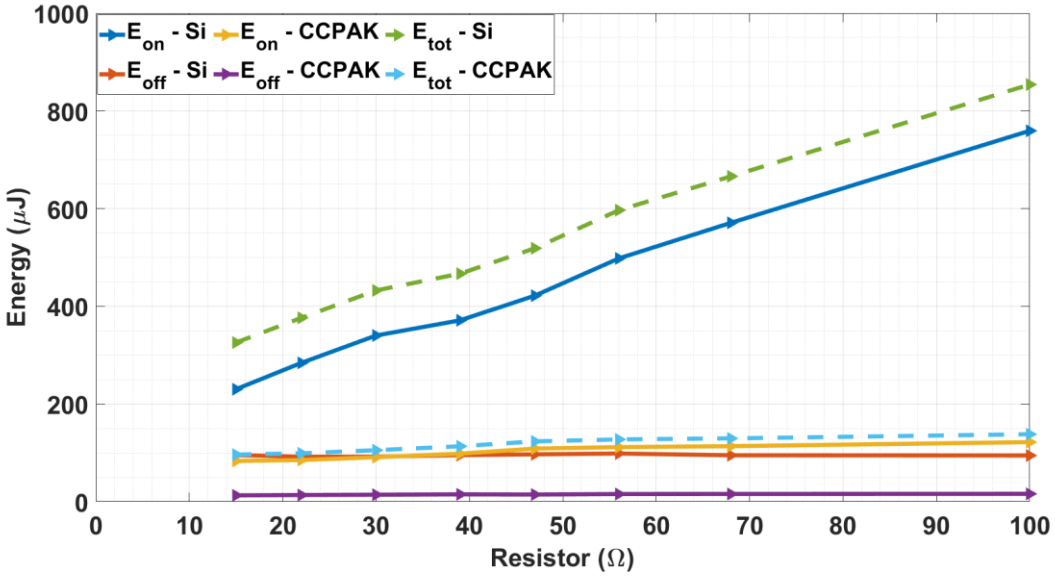


Figure 67: Energy comparison between CCPAK and Si CoolMOS for varying resistors from 15 Ω to 100 Ω for a drain current of 12 Amp

Switching energy loss for varying resistors was analysed for Si CoolMOS as Figure 67 shows. The turn-on energy for Si CoolMOS increases significantly as the resistor value increases and the turn-off energy remains almost constant for the increasing resistor value. The difference in total energy loss at 100 Ω for the GaN device is around 138.2 µJ and for Si CoolMOS is 853.9 µJ. The increase of energy seen for the Si device is around 715 µJ. This goes on to show that, even at higher gate resistance GaN devices provide lower switching energy loss.

5.4 Summary of energy loss of all four devices

Figure 68 sums up the turn-on and turn-off energy loss for all four devices that were discussed in this and Chapter 4. And, Figure 69 shows the total energy dissipated. The data mentioned here is for gate resistance $R_{g(on)} = 30\ \Omega$ and $R_{g(off)} = 10\ \Omega$. The energy loss for Si CoolMOS consistently remains higher when compared to the GaN devices. Which aligns with the previous literature.

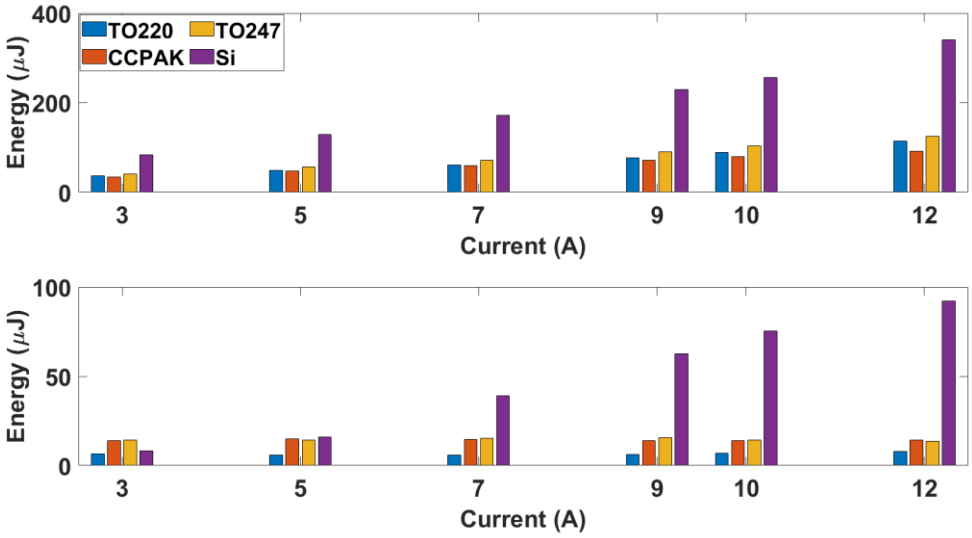


Figure 68: Comparison of turn-on (up) and turn-off (down) switching energy of four different devices $R_{g(on)} = 30\Omega$ and $R_{g(off)} = 10\Omega$ at varying current from 3 Amps to 10 Amps

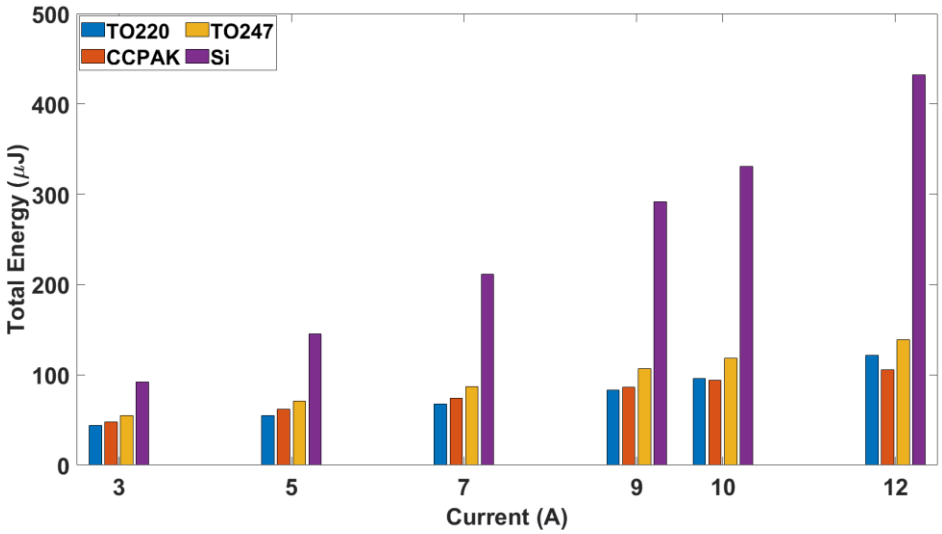


Figure 69: Comparison of turn-off switching energy of four different devices

Therefore, it can be concluded that the total energy losses of CCPAK remain lower for both TO-247 and Si CoolMOS at all conditions applied. And, for TO-220 the total energy loss is higher at higher currents, which makes CCPAK a suitable candidate for high-current applications. Also, due to its compact packaging with both top and bottom side cooling, thermal management would become easier [88], [89].

5.2 Modelling of GaN devices in SaberRD

In this section, a simulation model of Polarisation Super Junction Gallium Nitride devices using SaberRD from Synopsys [90] is created. The Power MOSFET Tool in SaberRD is the platform used for the system-level design of devices. First, the extracted Static characteristics of the device are presented, second, the modelling of the device is carried out and then finally the simulated switching characteristics and its data are presented. This is the first time $1.2\,kV$ PSJ GaN is modelled in SaberRD to realise its switching characteristics.

5.2.1 Polarisation Super Junction Field Effect Transistor (PSJ-FET)

The concept of Polarisation Super Junction was first proposed in [91] and GaN PSJ FET was first proposed in [92], different from conventional HEMT device PSJ-FET consists of a double heterostructure undoped GaN/AlGaN/GaN. The 2DEG as explained in Chapter 2 is formed due to polarization property, here 2DHG, 2 Dimensional Hole gas is formed as well. The 2DHG is formed via negative polarization and 2DEG is formed via positive polarization. As shown in Figure 70 the gate or the base electrode forms an Ohmic contact on the top of the p-GaN layer.

For a PSJ device, a distributed electric field can be achieved due to the presence of both positive and negative charges the densities of both charges can be matched, and a charge balance can be achieved. Due to this charge balance, when the device is in the off-state the drift region gets depleted. This can help to achieve increased drain voltage and uniform electric field. Hence, due to the flattened electric field and enhancement of the drain voltage, PSJ devices can be advantageous when compared with conventional GaN devices [6]. The electric field distribution and simulated breakdown characteristics of PSJ and Conventional GaN are shown in Figure 71 and Figure 72.

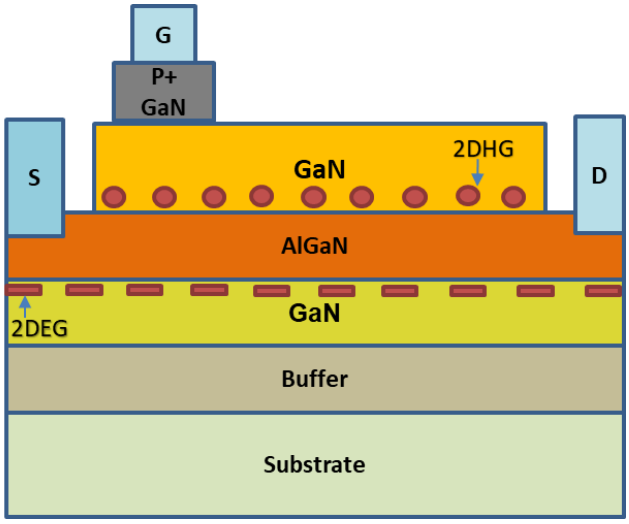


Figure 70: Polarisation Super Junction – FET Structure

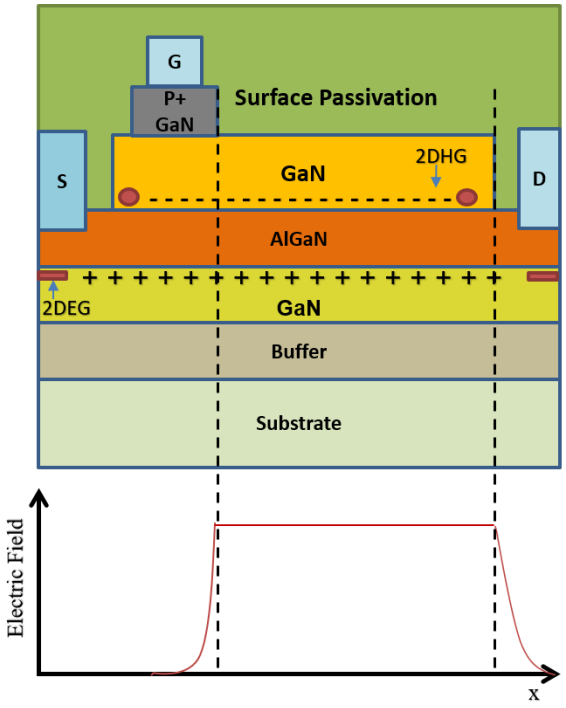


Figure 71: Electric field distribution of PSJ under off-state

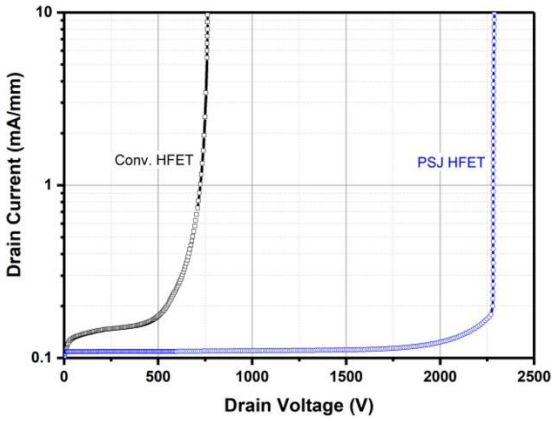


Figure 72: Breakdown voltage characteristics of PSJ GaN and conventional GaN HFET (Simulated) [93]

A 3.3 kV PSJ device in normal-on and cascode structure was tested and the switching characteristics were explained in [6]. It was presented that the cascode PSJ showed a faster switching time than its d-mode counterpart. The PSJ GaN tested in this thesis is rated at 1.2 kV and was provided by POWDEC K.K. There were two previous research conducted on the mentioned 1.2 kV device. One which focused on the turn-off dv/dt controllability of the device. It was found that the PSJ GaN can achieve low dv/dt, which would be suitable for motor drive applications through a suitable gate control method, either gate voltage or gate resistor [94]. Another one was [95] which was based on implementing a fast protection circuit for a bidirectional switching module which used two discrete d-mode PSJ GaN.

The transfer characteristics of the device were tested by the author, the capacitance data was obtained from [94]. The $I_D{-}V_{DS}$, and the $I_D - V_{GS}$ characteristics were obtained from the Curve Tracer 371A and the device was tested at different temperatures using Heraeus oven. The device used was a bare die wire bonded onto a Direct Bond Copper (DBC) substrate. Figure 73 shows the setup of the equipment used for the measurement. Where (a) represents the Heraeus oven and (b) represents the curve tracer.

Figure 73 : Heraeus Oven and Curve Tracer/ Analyser used for device characterisation

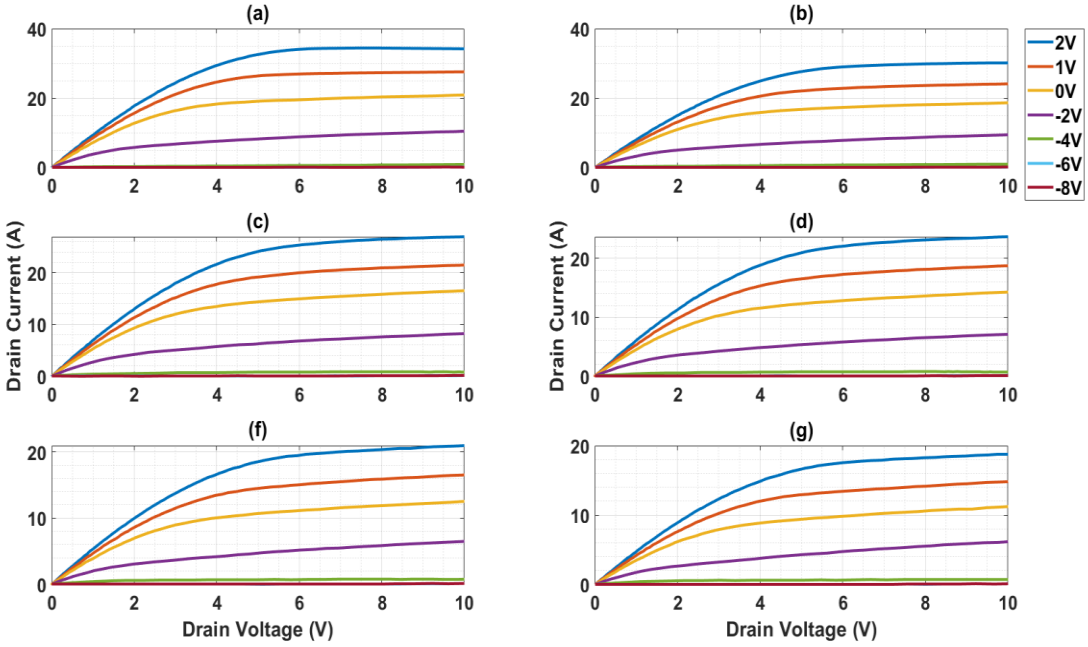


Figure 74: $I_D - V_{DS}$ characteristics of 1.2 kV PSJ Device for (a) 25 °C (b) 50 °C (c) 75 °C (d) 100 °C (e) 125 °C (f) 150 °C

The $I_D, -V_{DS}$ of the device was tested for seven different gate voltages, from -8 V to a maximum of 2 V and for a maximum temperature of $150\ °C$. It can be seen that as the temperature increases the I_D decreases, this is because as the temperature is increased the electron mobility decreases due to the increase in the phonon scattering when the lattice temperature is increased [6]. From the $I_D - V_{GS}$ data, the threshold voltage is observed to be around - 4.8 V. This data is important to understand the turn-off and the turn-on voltage that can be applied to the device.

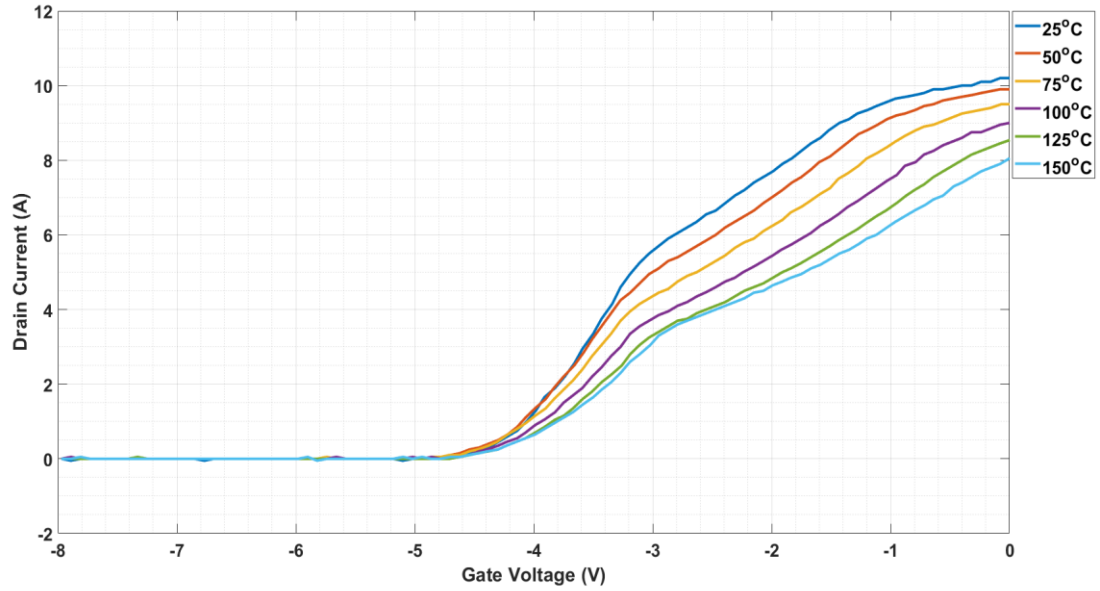


Figure 75: $I_D - V_{GS}$ characteristics of 1.2 kV PSJ Device for temperatures from 50 ℃ - *150* ℃ *for* $V_{DS} = 10\ V$

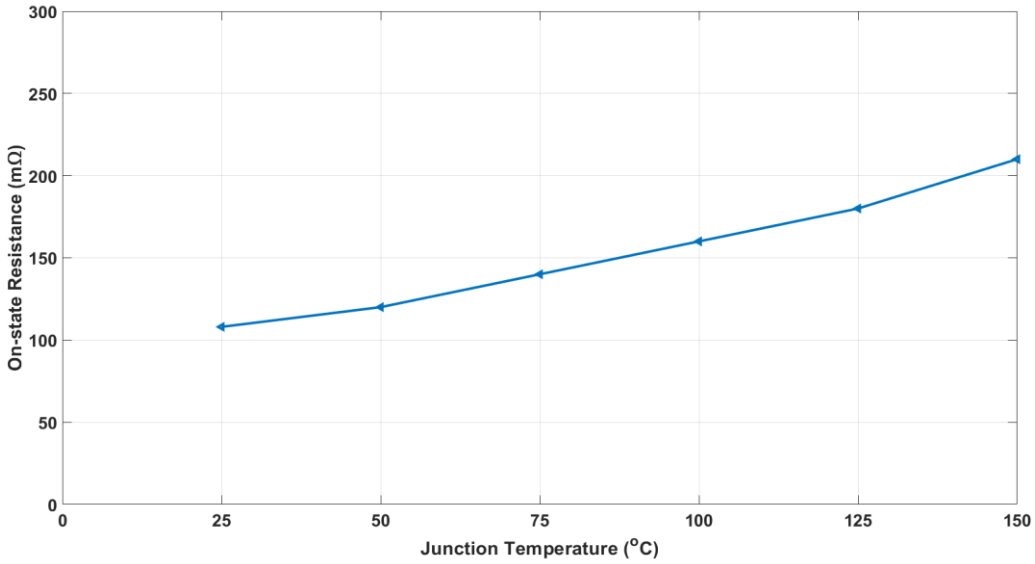


Figure 76: On – state resistance of PSJ device at different temperatures. $V_{DS} = 1\ V$ *and* $V_{GS} = +2\ V$

To observe the typical values of drain to source resistance of the device, the data is extracted from the $I_{DS} - V_{DS}$ curve at $V_{GS} = +2\ V$ and $V_{DS} = 1\ V$. The value of the on-state resistance rises from 108 $m\Omega$ to 210 $m\Omega$ from 25 °C to 150 °C. As mentioned above the

increase in temperature affects the phonon scattering and reduces the electron mobility. This can be observed from the on-state resistance increase at higher temperatures.

Figure 77 represents a sample switching characteristics of PSJ device at 800 V DC which is 2/3rd of the device-rated voltage. The gate voltage V_{GS} is between + 0.7 V and -15 V. The value + 0.7 V is achieved by placing a diode at the gate of the device. The diode then clamps the voltage that is given by the gate driver and is fed to the device. The gate driver used for the measurement is UCC5390 since it is compatible with providing negative gate voltage. As mentioned above the device is placed on DBC and connected to the PCB using wires. The inductance introduced from the wire could affect the switching results such as a slight delay that be seen at the turn-on and turn–off of the device.

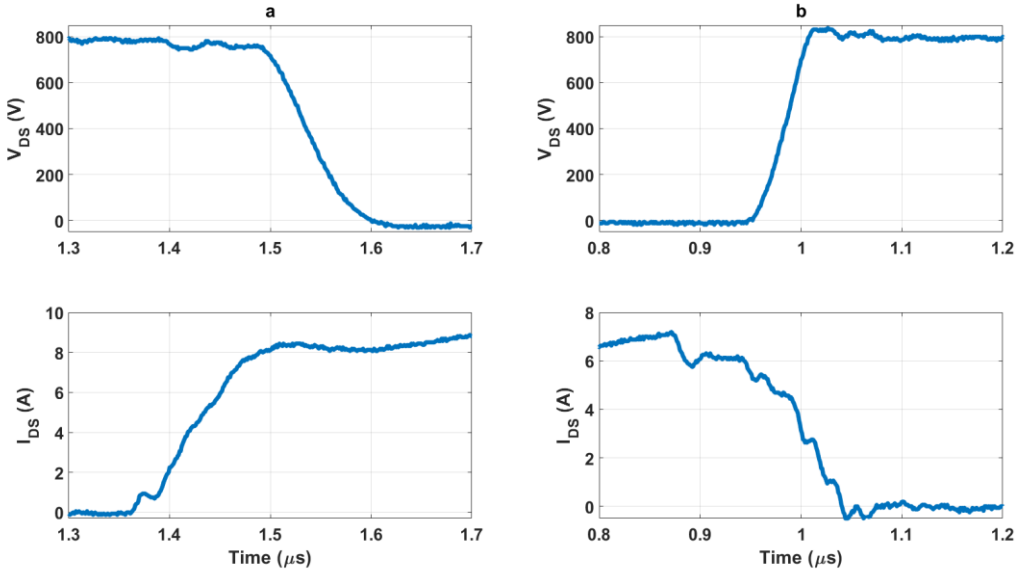


Figure 77: PSJ switching characteristics at 800 V V_{DS} and 7 Amp I_{DS} (a) Turn–on and (b) Turn–off

5.2.2 Modelling of Device in Power MOSFET Tool (PMT)

Because of fast-growing research on wide band gap devices, understanding their behaviour in a simulation model will help in reducing the early cost of practically testing them [96]. There are many simulation environments available for such requirements, and SaberRD, Synopsys is one such useful platform that will be helpful to understand new research devices.

Power MOSFET Tool in SaberRD helps to model a device by utilizing the transfer characteristics of the device [90]. Figure 78 provides a snapshot of the platform. And,

Figure 79 represents the internal circuit provided by the tool. The tool helps in optimising and predicting the device characteristics even if certain parameters of the device are yet to be developed. The functionality of the tool and the step-by-step procedure of implementing the measured data onto the tool are discussed in detail.

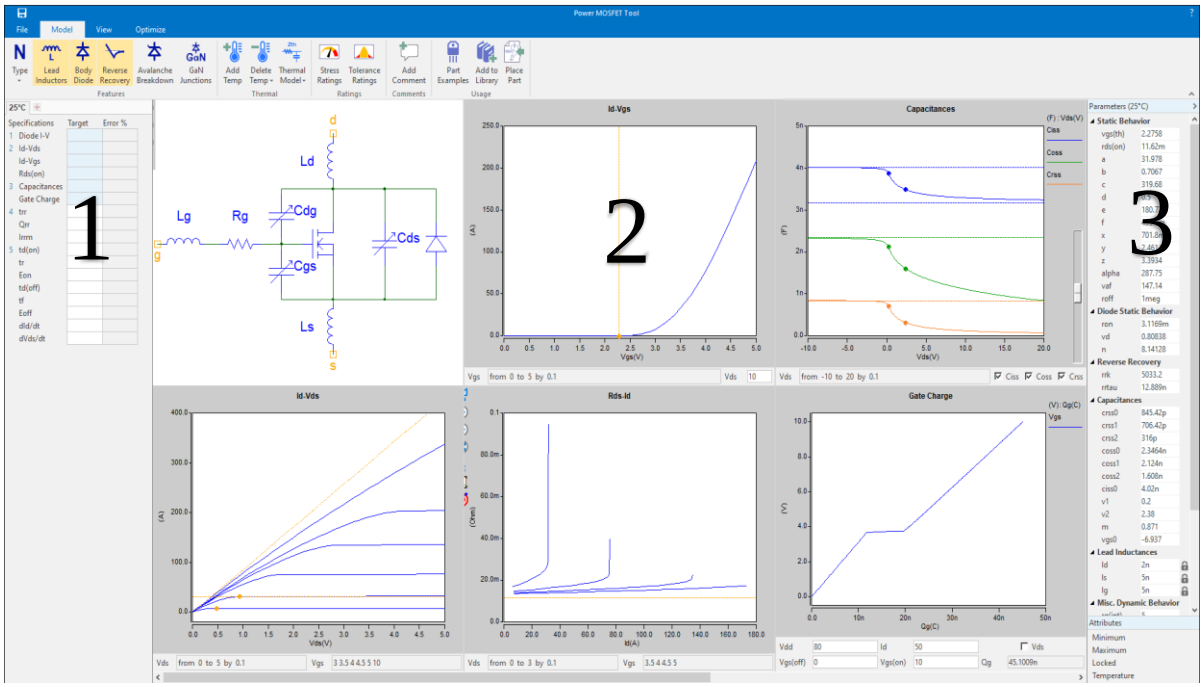


Figure 78: Power MOSFET Tool simulator platform

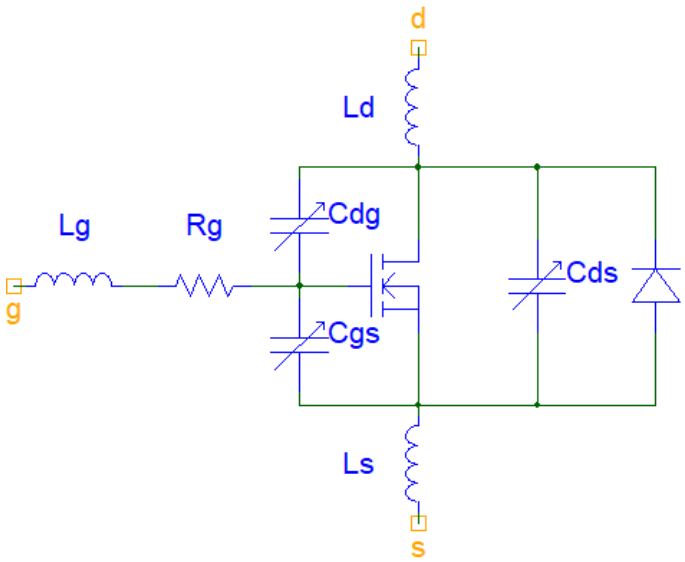


Figure 79: SaberRD Model Circuit with internal capacitances and inductances

The Power MOSFET Tool can be divided into three sections, the middle section (2) consists of the Model characteristics, where the datasheet transfer I-V characteristics, the capacitances, gate charge, $R_{DS(on)}$ are traced and once all the curves have been inputted, the inbuilt optimizer function is invoked. The blue line represents the Simulated SaberRD Data and the measured/ experimental I-V is depicted by the grey line. Section 1, depicts the percentage error between the SaberRD simulated curve and the measured curve. Finally, Section 3, represents the parameters of the device after optimization.

The internal circuit provided by the tool consists of device capacitances and lead packages inductance. Lead package inductance can be removed if not required for the simulation. The internal circuit also provides the option to provide the body diode for the device or not, depending on the characteristics of the device. The PSJ GaN does not have a body diode, hence the option was removed for the simulation. The channel type of the device can be changed accordingly to the N or P channel. The tool helps to add the characterisation data for different temperatures as well.

The characterisation of the device is as follows:

1. Static characteristics - Once the required $I_D - V_{DS}, I_D - V_{GS}, Rds - I_D$ characteristics are extracted through experiments, the data is traced to fit the tool. There are three different sections dedicated to each curve data. While implementing the $I_D - V_G$ data, it is important to set the V_D value the same as the one used for measurement. After specifying the curves, the optimizer is run to minimise the error between the simulated and measured data. A relative error metric is used by the optimizer to minimise the difference between the SaberRD curves. All the modelling is done at 25 °C.

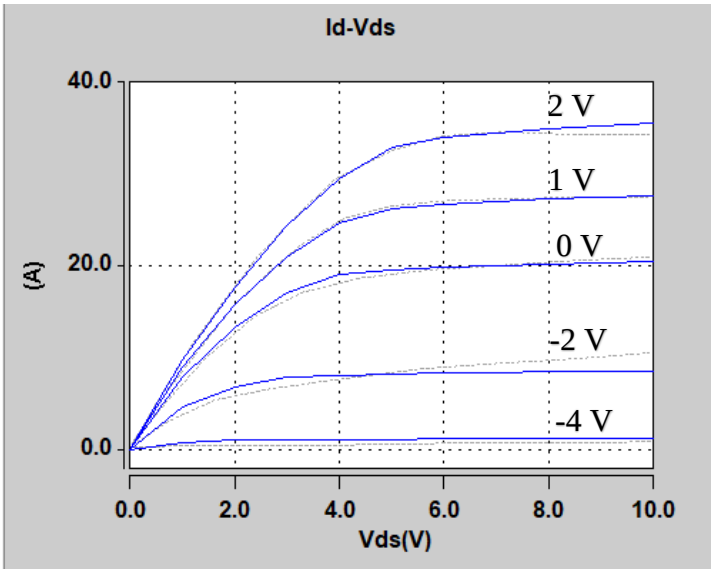


Figure 80: SaberRD (Blue) on Grey (Measured) I_{DS} V_{DS} characteristics of PSJ –GaN Simulated in PMT

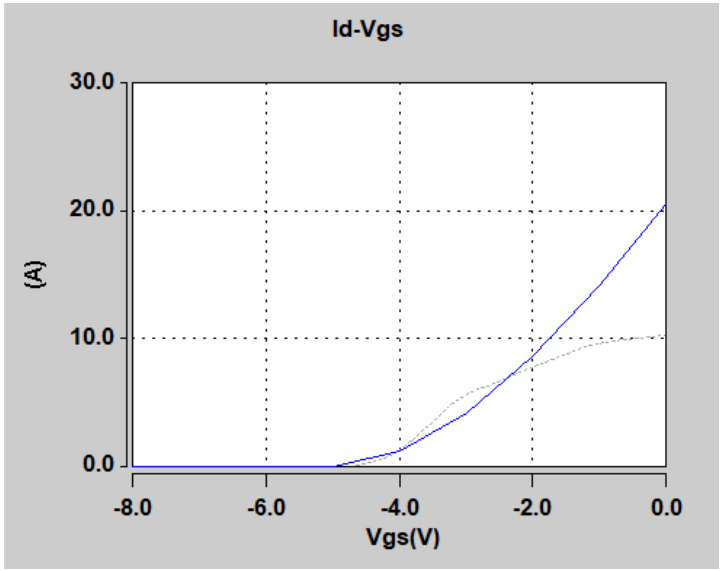


Figure 81: SaberRD (Blue) on Grey (Measured) I_{DS} V_{GS} characteristics of PSJ –GaN Simulated in PMT

The SaberRD manual recommended removing the points below the threshold voltage for $I_{DS} - V_{GS}$ and at low currents for $I_{DS} - V_{\mathrm{DS}}$ since the optimizer uses relative error metric and this error becomes a bit sensitive to the points traced at low currents and below threshold value. Hence the tracing was done accordingly.

2. The next section is for capacitance curves. Since the capacitance is temperature-independent, therefore the data need not be changed for different temperatures.

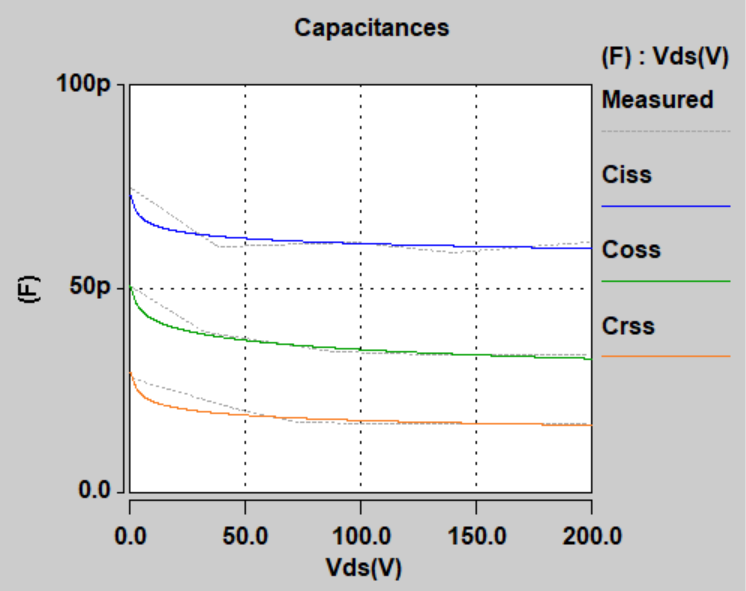


Figure 82: SaberRD (Blue – Ciss, Green – Coss, Oragnge – Crss) on Grey (Measured) Capacitance of PSJ – GaN

Parameters	Measured	Saber	Error(%)
$V_{GS(th)}$	-4.8V	-4.9V	42.6 %
C_{rss}	~26 pF	21.5 pF	2.12 %
C_{iss}	~45 pF	41.4 pF	2.12 %
C_{oss}	75 pF	94.4 pF	2.12 %

Table 9: Table representing optimised SaberRD data and the error percentage

Table 9 shows the data after optimization. Section 3 from Figure 78 is where the data is stored after all curves have been traced and optimised. It can be seen from Table 9 that, the

error for the threshold voltage is 42.6% but the value of the threshold does not have much difference. As the error is taken from the entire characteristic curve it can be seen that the curve presents a non-linearity hence the error is on the higher side. The capacitance error is 2.12% and it can be seen that the values of the capacitance almost match with the measured results. And, finally the percentage error for $I_D - V_{DS}$ is 2.9%.

3. Gate Charge calculation

   The relation between the $I_D - V_{DS}$, $I_D - V_{GS}$ and capacitance helps in understanding the gate charge behaviour. Figure 83 represents model plots to understand the gate-charge plot optimised by SaberRD using the data given to the PMT. There are five main steps involved in the gate-charge behaviour. First, where the applied gate voltage which is (b) $I_D - V_{gs}$ in the graph increases till the device is conducting and allows the load current to flow. This is represented by steps 1-2. The first transition i.e. from steps 1-2 ends when the device starts to conduct which is given by steps 2-3. As the drain current is shown in $I_D - V_{DS}$ reaches saturation, given by 3-4, leading to gate voltage clamping at the Miller plateau and the drain current remains constant. From steps 4-5, the voltage rises till the value of the applied gate voltage and at this point, the device is fully conducting [97].

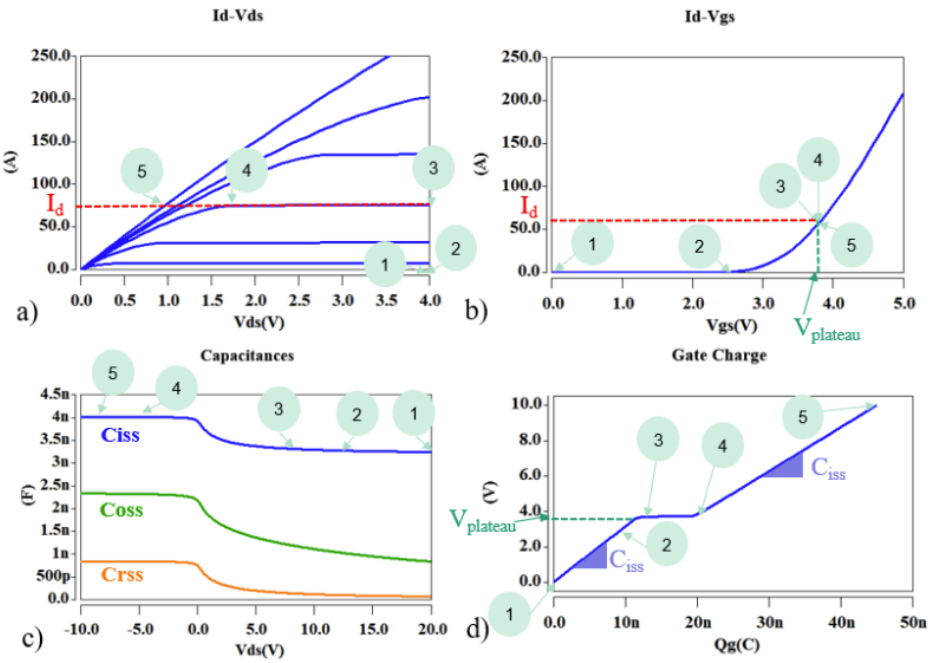


Figure 83: Detailed explanation of gate-charge plot [98]

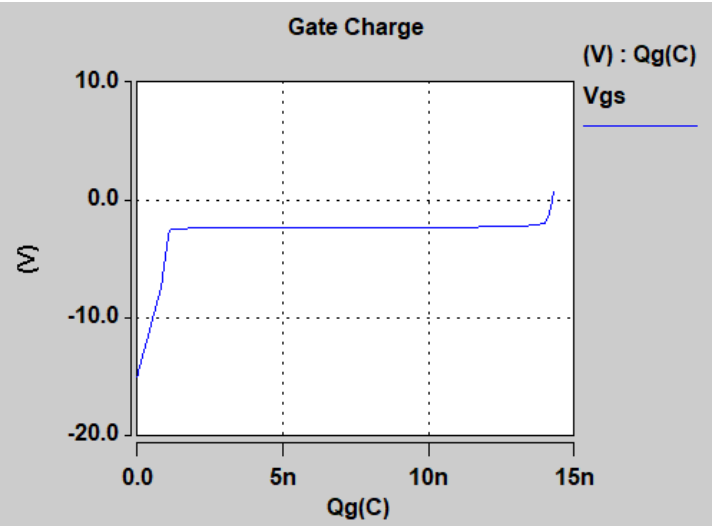


Figure 84: SaberRD optimised gate-charge

Figure 84 shows the gate-charge which is predicted by SaberRD after optimising the capacitance and the transfer characteristics of the device.

A few publications focus on the characterisation of devices using PMT [98]–[100]. In [98] a vertical GaN and a SiC were modelled using PMT and a double pulse tester results are shown and matched with the experimental data. The research showed that the PMT is an ideal tool for understanding the performance of the device, even during the initial development stage of the device where a few characteristics of the devices might be unknown. And, in [99] a synchronous boost converter was built in SaberRD and compared with the experimental result and the SaberRD simulation was found to have a good match with that of the experiment.

In this section, a double pulse switching test is designed in SaberRD using the modelled device to understand the switching characteristics of 1.2 kV PSJ. As mentioned before the controllability of turn-off $\frac{dv}{dt}$ was presented in [94]. Here, the switching for both turn-on and turn-off will be discussed along with how the device operates under different conditions.

Since the PSJ-GaN is a normally-on device, the gate needs a negative voltage to turn off the device. Therefore, the voltage switched for gate control is + 0.7 V for turn on and -15 V for turn-off. The free-wheeling diode selected is rated at 1.2 kV and 20 Amps [101]. The modelling for the diode was also done in SaberRD using the Diode tool.

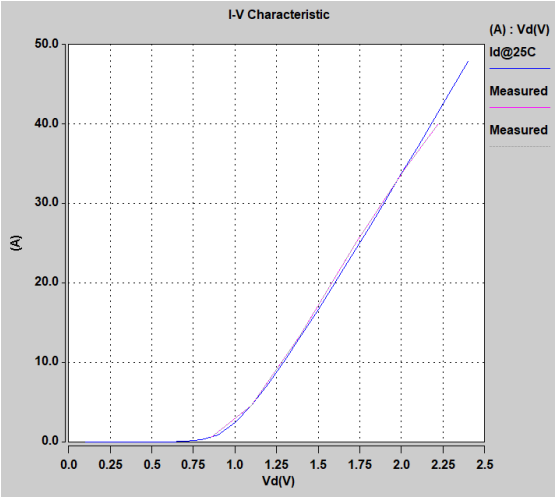


Figure 85: Diode I-V characteristics SaberRD (Blue), Pink (Measured)

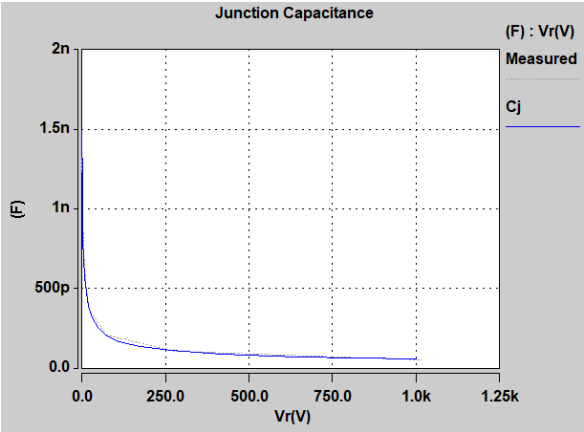


Figure 86: Capacitance measurement SaberRD (Blue), Grey (Measured)

The simulated setup for the device is as follows, the diode used is detailed above, the gate voltage applied is + 0.7 V and -15 V, and decoupling capacitors. The circuit simulated is in ideal conditions as no external parasitics are involved. The inductor used is 1.2 mH and the pulse width was adjusted accordingly for different drain currents. Even though the results would not have any non-ideal parasitics, the pattern of the switching result can be compared with the data presented here [94].

Switching analysis of SaberRD modelled device.

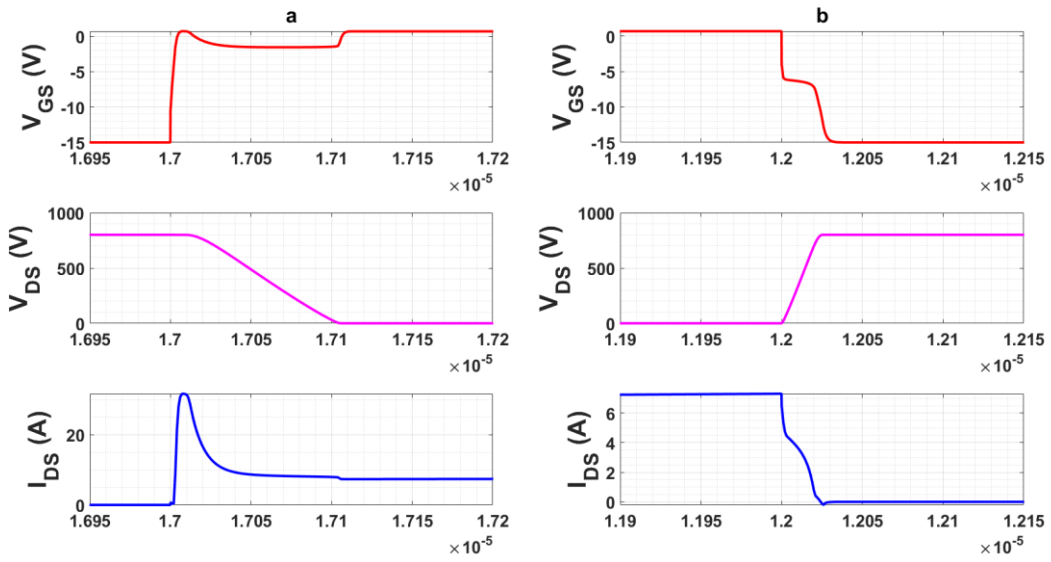


Figure 87: Switching characteristics of PSJ-GaN in SaberRD environment for 800 V DC at drain current of 7 Amp (a) Turn-on (b) Turn-off

Figure 87 represents the switching of PSJ-GaN for an 800 V DC for a gate resistor of 15 Ω, gate voltage of + 0.7 V and a drain current of 7 Amp. It can be seen from the figure that the turn-on transition is slower than the turn-off. Also, the start of the current is not aligned to the V_{DS} fall, this could be due to the inconsistency in modelling the diode or the device as the de-skew of the signal is not possible in the simulation environment. But, the delay is in terms of a few nanoseconds. The turn-off waveform can be compared with the research conducted in [94]. The calculated rise time for the switching is 68 ns and the fall time is 18 ns. The turn-on dv/dt is 0.9 $(\frac{kV}{\mu s})$ and the turn-off dv/dt is 3.7 $(\frac{kV}{\mu s})$. This shows that the turn-on for PSJ GaN has a slower switching rate than the turn-off. The same trend was observed in [6] where the switching of 3.3 kV PSJ GaN is conducted and the turn-on switching showed a slower transition rate when compared to the turn-off.

Analysis based on varying gate resistor and drain current

A trend analysis based on varying gate resistors and drain currents is done to better understand the switching transition of the device.

Transition time and dv/dt analysis

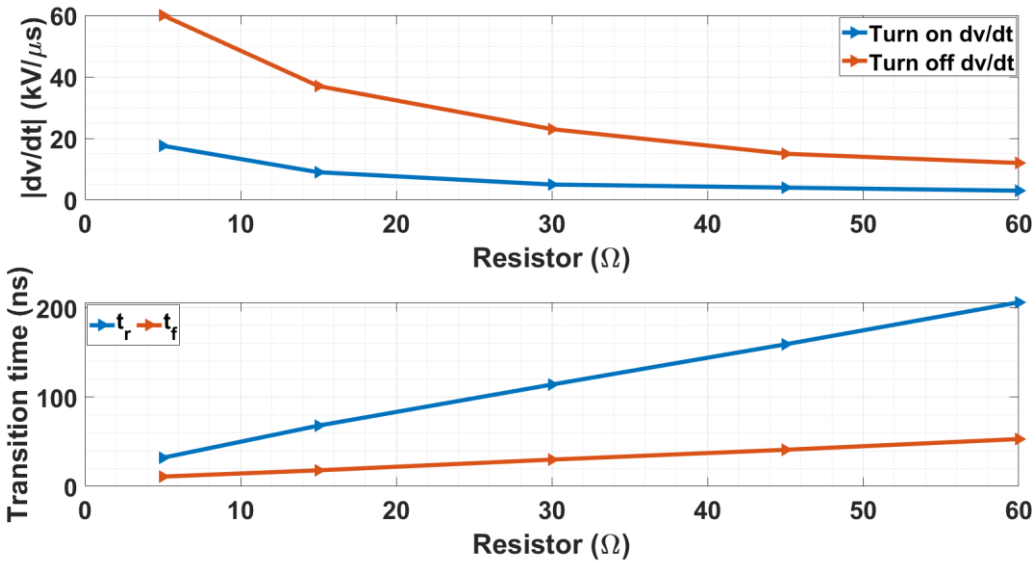


Figure 88: Transition time and dv/dt analysis for both turn on and turn off for $R_{g(on)} = 5\ \Omega, 15\ \Omega, 30\ \Omega, 45\ \Omega$ and $60\ \Omega$ for a drain current of 7 Amp

Even though the turn-off $dv/dt$is higher than the turn-on. From Figure 88 it can be seen that for the PSJ GaN device, the dv/dt can be controlled using external gate resistance. The highest dv/dtobserved to be for turn-off is 60 ($\frac{kV}{\mu s}$). And, with an increase in gate resistance, the $dv/dt$of the device decreases to 12 ($\frac{kV}{\mu s}$) which is an 80% decrease. Similar to the observation shown in [94]. The same can be seen for turn-on dv/dt as well. The turn-on dv/dt for the device decreases from 17.6 ($\frac{kV}{\mu s}$) to 3 ($\frac{kV}{\mu s}$). Which is a decrease of 82.9%. The graphical representation of the change in V_{DS} slope with respect to gate resistance is shown in Figure 89 and Figure 90.

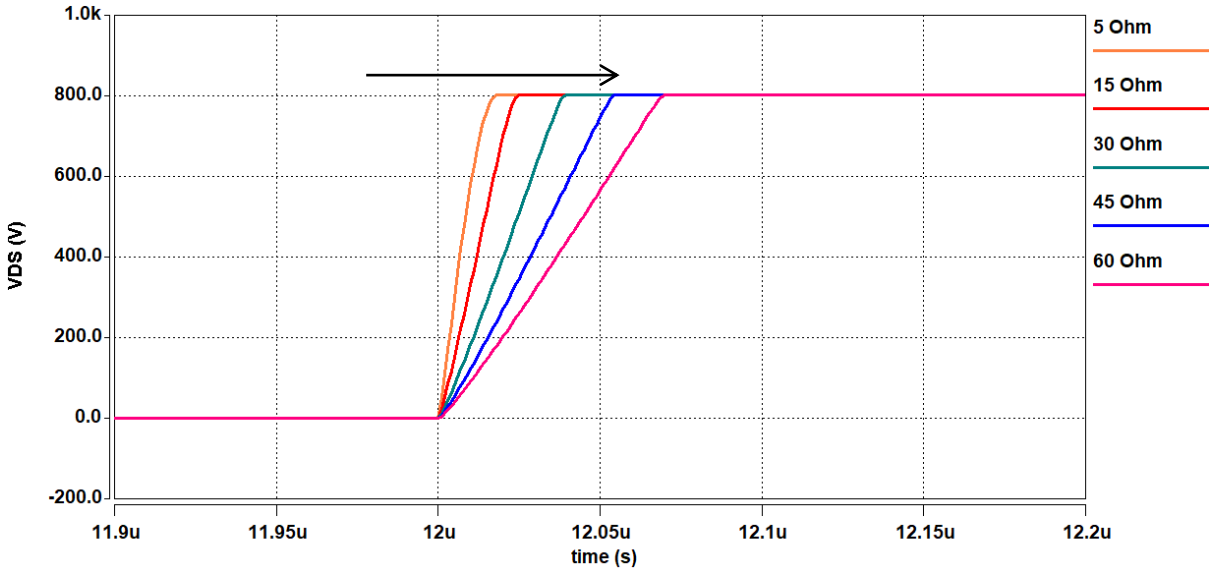


Figure 89: Change in turn-off drain-source voltage with varying gate resistance

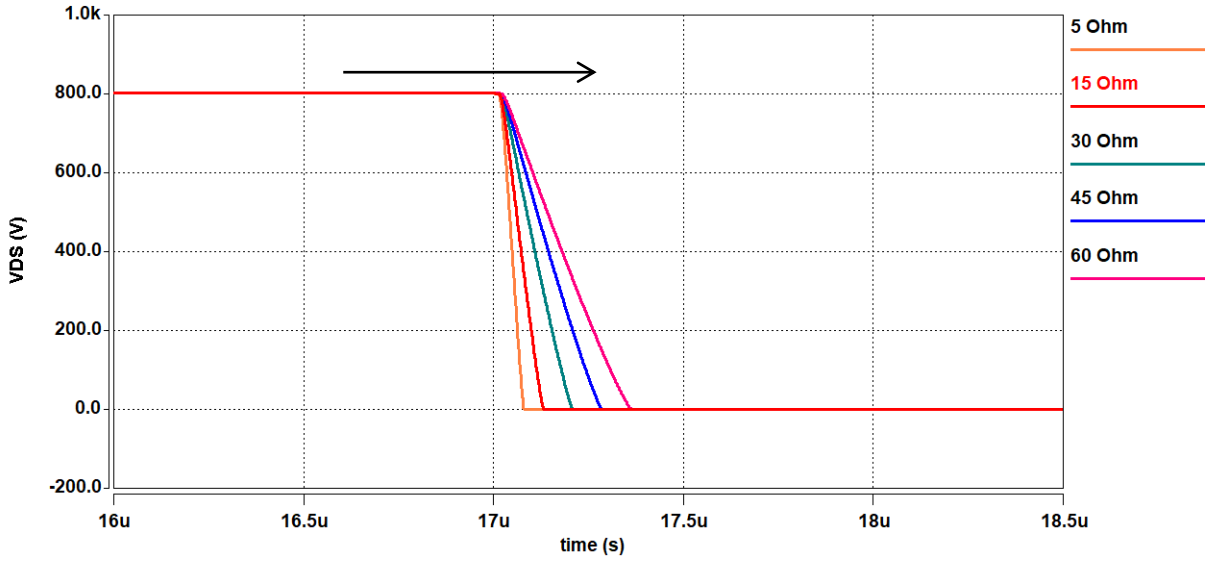


Figure 90: Change in turn-on drain-source voltage with varying gate resistance

Switching energy analysis for varying drain current

The switching energy analysis was done for drain current from 3 Amp to 7 Amp for gate resistors of 15 Ω, 30 Ω and 45 Ω.

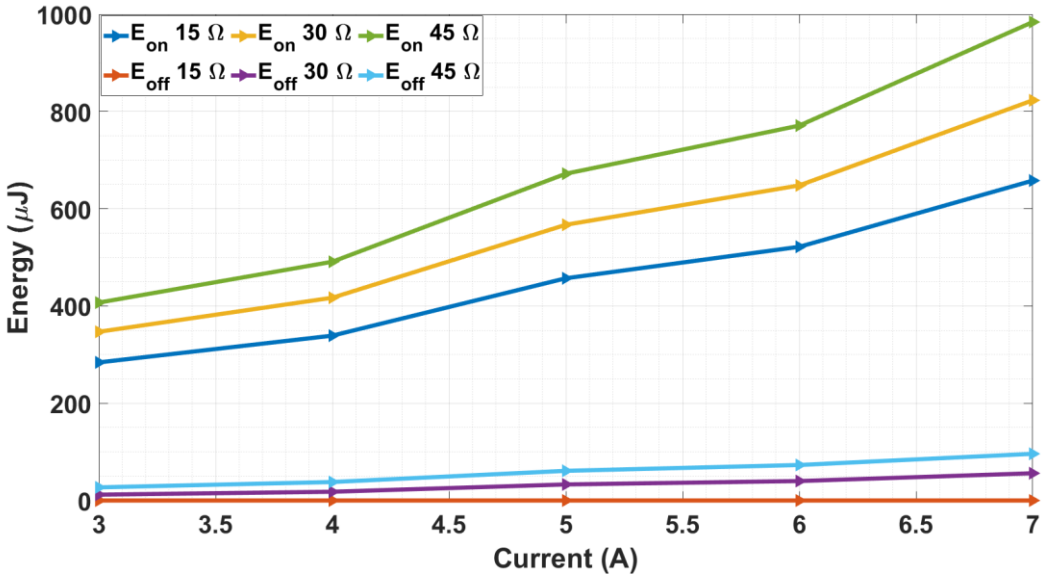


Figure 91: Switching energy loss for PSJ GaN for varying drain current from 3 Amp to 7 Amp for different gate resistors

From the switching energy losses, it can be seen that the turn-on energy loss is higher than the turn-off. There is a steep increase in the turn-on energy loss when compared to the turn-off. This can be attributed to the steep increase in the turn-on transition. The total switching energy loss of the device at 7 Amp for a gate resistance of 45 Ω is calculated to be 1080 μJ.

Although, the above results are obtained under ideal conditions. These data can be used as a foundation before the experimental work is conducted.

5.3 Summary

This chapter is divided into two sections, it starts with the switching analysis of the Si CoolMOS device. The same double pulse tester was used for the Si CoolMOS switching analysis. Trend analysis is done for varying gate resistors and drain current for the Si device. The results then obtained from the Si device are compared with the CCPAK GaN. In the final part of the first section, the switching energy loss of all four devices is compared with each other. All four GaN devices showed superior characteristics in terms of their switching energy when compared with Si CoolMOS.

The second section of the chapter describes the modelling of a Polarisation Super Junction GaN device in SaberRD. The modelling of each device's characteristics is discussed in detail. After the device characterisation in PMT, the device was implemented in a switching circuit and the switching waveform of the modelled device was presented along with the switching energy, transient time and dv/dt analysis.

Chapter 6: Dynamic On-State Resistance Measurement

This chapter is dedicated to calculating the dynamic on-state resistance of GaN cascode devices. The method implemented for calculating the dynamic $R_{DS(on)}$, the schematic is explained in detail. The $R_{DS(on)}$ is calculated for two devices at different voltages and two different currents. The effect on $R_{DS(on)}$ is also observed for different stress times.

6.1 Previous literature

To investigate the dynamic $R_{DS(on)}$ a clamping circuit is implemented so that the amplifier of the oscilloscope is not saturated. The clamping circuit implemented here is a modification and a simpler version of the circuit presented in [56]. This clamping circuit was proposed first in [102], [103]. In that, the setup used was modified for both hard and soft switching and the dynamic-on state resistance was calculated for both switching operations. There were three devices used for investigation, two commercially available e-mode GaN and Si-CoolMOS. The same setup was used in [104]–[106]. In this chapter, the clamping circuit is used to evaluate the dynamic $R_{DS(on)}$ of GaN cascode devices. There are only a few papers that investigate the occurrence of current collapse in GaN cascode devices. As seen in the previous chapters, the internal parasitics of the cascode structure can play a huge role in influencing the measurement. In [107] a clamping circuit dedicated to cascode devices was proposed and a commercially available 650 V GaN cascode was tested. The device was tested for a stress voltage of 50 V and 400 V for both hard and soft switching. It was observed that, when the device was tested at 25°C the dynamic $R_{DS(on)}$ did not change with the applied stress voltage for both hard and soft switching operation. But, as the temperature was increased to 75 °C and 125 °C the effect of stress voltage in realising $R_{DS(on)}$ could be seen. Although, this research only focused on two drain voltages 50 V and 400 V. The measured $R_{DS(on)}$ for the cascode device under hard switching for both 50 V and 400 V was found to be 0.045 Ω at 25°C. And, the highest value was found to be around 0.069 Ω for 50 V and 0.071 Ω for 400 V at 125 °C. However other key factors such as the stress time and varying drain current were not part of the mentioned study.

Another research [108], [109] presented tested three different GaN devices, and one of them included a cascode device. The results of the measurement showed a slight increase in the dynamic $R_{DS(on)}$ for voltages ranging from 100 V to 400 V. In this research, the dynamic

on-state resistance value for the cascode device at 100 V to 400 V was found to increase from around 1.01 to 1.09 (normalised data) at 25°C. In [110] cascode device from Transphorm is chosen for characterisation, although the load used for the testing is a resistive load and the maximum voltage the dynamic $R_{DS(on)}$ was tested for is 120 V. The clamping circuit used in this research is a JEDEC-specified circuit. The results showed a clear increase in the measurement as the voltage increased from 20 V to 120 V. The range of the dynamic on-state resistance for hard-switching was found to increase from 0.3 Ω to 0.5 Ω. Among the three research, the clamping circuit with the resistive load was found to have a maximum increase in the dynamic on-state resistance with varying stress voltage.

The Dynamic $R_{DS(on)}$ testing can be carried out for two operations, one is the hard-switching operation and the soft-switching [102], [111]. Hard-switching operation is when the voltage and current overlap with each other, whereas for soft-switching, this overlap is not observed. For the analysis discussed here, the measurement is taken under hard-switching operation with inductor load. As can be seen from previous literature, for cascode devices, some setups tend to show Dynamic $R_{DS(on)}$ and some do not. The work conducted here tries to observe if the Dynamic $R_{DS(on)}$ can be realised for cascode devices under hard switching operation for this clamping circuit. All tests are conducted at room temperature.

6.2 Current Collapse mechanism under soft and hard switching

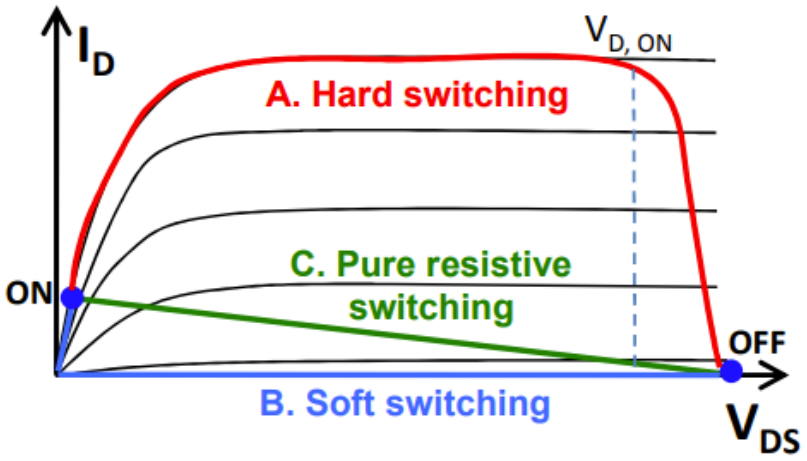


Figure 92: Hard soft and resistive switching mechanism [111]

It has been shown that the current collapse mechanism under hard and soft switching operations gives varying results. Figure 92 shows the load line for resistive, hard and soft switching. For hard switching the load line passes through high voltage and current area (Marked in red). This can cause the channel temperature to increase and, can also be affected by hot carrier charges [111]. For soft-switching the device switches during the off-state. This results in only a small current to pass through the channel. This results in degradation caused by electrostatics and could be increased due to the leakage current [111]. The recovery mechanism in current collapse can be divided into two one being the de-trapping of the electrons and two trapping of holes (positive charge) which then compensates the trapping of electrons. Therefore, in [111] it was shown that the soft switching operation of the device gave higher dynamic on-state resistance. During hard-switching, holes that are generated due to impact ionisation when the device is under high voltage and high current compensate for the trapped electrons. This is one of the reasons for the low dynamic on-state behaviour shown by devices under hard-switching. On the other hand, some researchers suggest that during hard switching the dynamic on-state resistance increases because of the hot electron effects [112]. A unified theory for hard and soft switching behaviour on the dynamic-on-state resistance was not found in the literature. Also, as mentioned in the above section, the research done on the GaN cascode current collapse phenomenon is very few. Two [108][110] of the research showed an increase in dynamic-on state for the device at room temperature and the other where the increase of dynamic-on state was observed for higher temperatures. All three devices used in the mentioned study are commercial cascode devices.

6.3 Experiment methodology

The clamping circuit is implemented as part of the double pulse switching test shown in Chapter 3. Due to the internal parasitics of the device, the components used in the circuit were placed as close to the device to avoid the influence of stray inductances. The clamping circuit consists of a 650 V SiC Schottky diode, a 6.2 V zener diode, a 330 Ω resistor and a 9 V voltage source [105]. The circuit is implemented on the same board as the Double Pulse Tester. The mentioned V_m terminal is measured instead of the actual drain to source voltage. For every drain voltage, the device current was kept constant by changing the inductor load accordingly. The inductor used is Iron Powder Toroid T175-2.

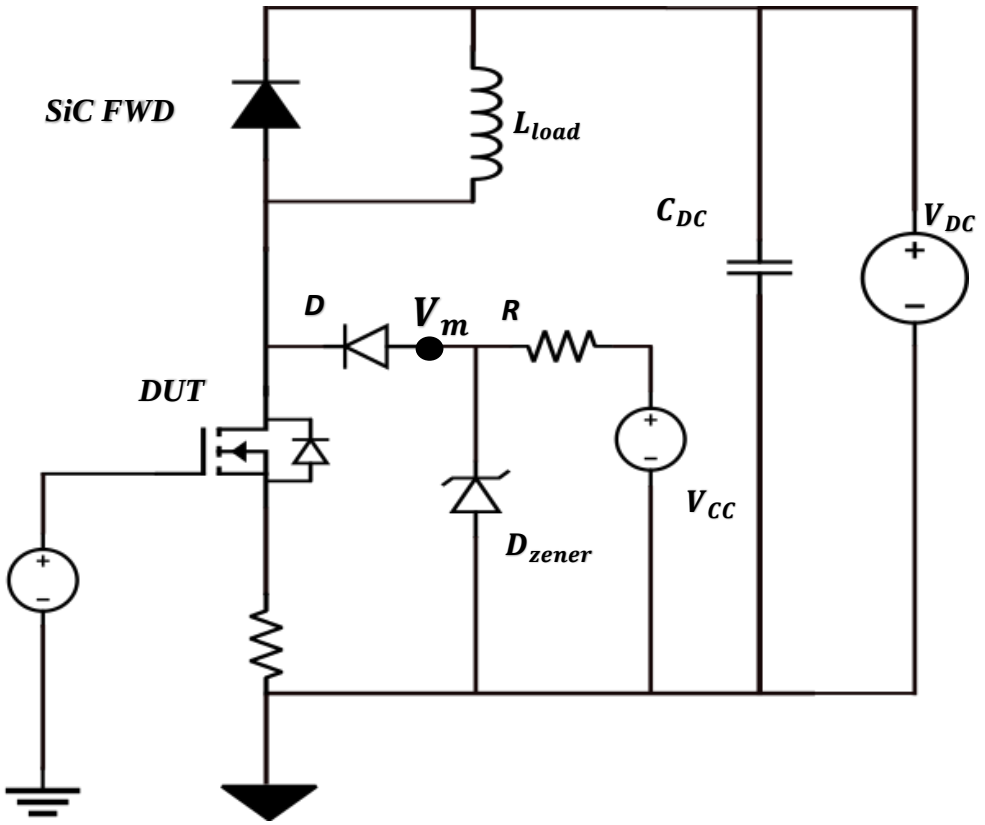


Figure 93: Test circuit for Dynamic $R_{DS(on)}$ measurement

The test waveform for the experiment can be seen in Figure 94. Two pulses are given to the gate of the DUT. The first pulse determines the device current and the second pulse is where Dynamic $R_{DS(on)}$ is measured. The working of the circuit is as follows. When the DUT is turned off. The diode ***D*** is also in the off-state. At this time instant, the voltage at point V_m is clamped to the Zener diode value. When the DUT is turned on the diode ***D*** is discharged till the diode ***D*** is turned on. As the junction capacitance of the diode D discharges, this causes ringing in the waveform as shown in Figure 94. Therefore, a SiC Schottky diode IDH02G65C5 [113] of smaller capacitance is chosen for the study. The final dynamic on-state resistance is measured when the device is turned on during the second pulse and the voltage is measured across the zener diode. The timing diagram is given in Figure 94. The device current is measured using a shunt resistor and the clamped voltage is measured using an Agilent 10074C probe. A scale of 200 mV/div was used to measure the whole clamped waveform and for current measurement, a 500 mV/div was used.

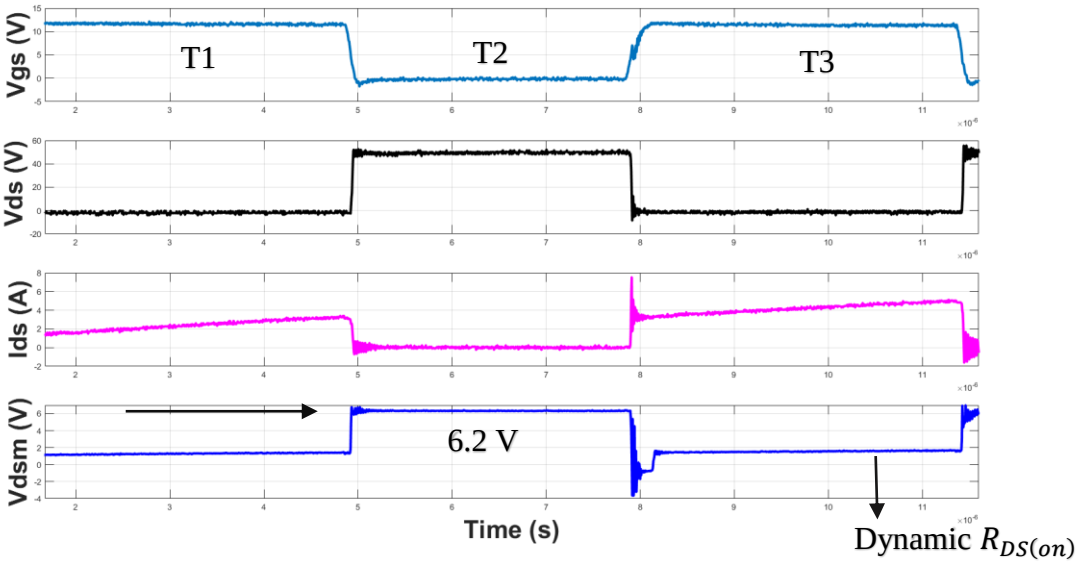


Figure 94: Test Waveform of Dynamic $R_{DS}(on)$ switching

At the first pulse T1, the DUT current rises according to the pulse width and inductor value. At T2 the device is in the off-state and the measurement V_{dsm} which is taken at Terminal V_m that is the voltage across the Zener diode. At T3 the measured V_m is now the sum of the drain-source voltage and the diode forward voltage. The Dynamic $R_{DS(on)}$ is calculated following the steps given from Equation 2 to Equation 5 [114].

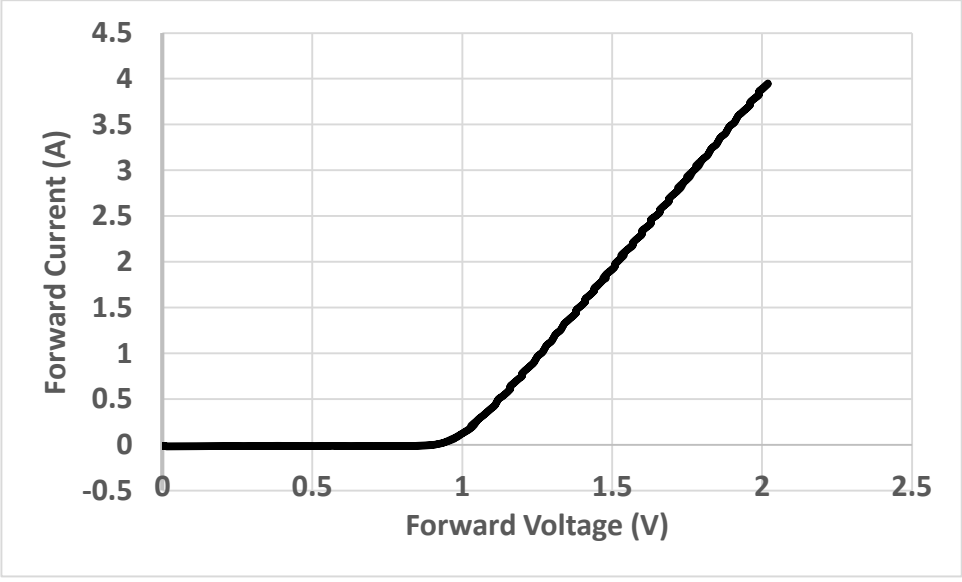


Figure 95: I-V characteristics of Diode (D) at 25°C using 371A curve tracer

$$R_{DS(on)} = \frac{V_{DS(on)}}{I} \quad \textit{Equation 2}$$

$$V_{DS(on)} = V_m - V_F \quad \textit{Equation 3}$$

$$V_F = 0.92 + 4I_F \quad \textit{Equation 4}$$

$$I_F = \frac{(V_{dd} - V_m)}{R} \quad \textit{Equation 5}$$

Where the V_m is the measured clamping voltage, V_F is the forward voltage of the diode and I_F is the diode current. And, finally, the $R_{DS(on)}$ is calculated.

6.4 Measurement Results

As mentioned above there are three time instants for the switching sequence. The first pulse T1 determines the device current and dynamic $R_{DS(on)}$ is measured at the third pulse T3. The results of the dynamic on-state resistance are shown for two devices. The devices tested are Device 1 - GAN041-650WSB and Device 2 - GAN039-650NBB. Where both devices are from the same manufacturer. There are two scenarios considered here:

1. The JEDEC standard for the $R_{DS(on)}$ measurement has suggested that the pulse T2 is to be controlled as the stress time for the device and the third time instant as the measurement for dynamic resistance [108]. At first, the results are shown where the T1 pulse is 3 μs, the T2 pulse is 2.5 μs and the T3 pulse is 2.5 μs. And, secondly, for the same T2 and T3 interval, the interval T1 is changed. The stress drain voltage for these two scenarios ranges from 50 V – 400 V. And, this measurement is done for two drain currents 3 Amp and 7 Amp, to see the effect of low and high drain current on the dynamic on-state resistance. For the same two T1 pulse values, the dynamic on-state resistance is calculated for different drain currents from 3 Amp to 12 Amp at 400 V voltage stress.
2. The second scenario is where the T2 interval was extended to 10 μs for a drain current of 3 Amp. In previous research the dynamic on-state resistance after 500ns of turning on the device and after 2000ns or 2500ns of turning on the device is analysed to understand how the dynamic on-state resistance changes with respect to time [102], [115].

For 3 Amp device current, the current starts at 3 Amp and increases to 5 Amp. And, for the 7 Amp device current, the current starts from 7 Amp to 11 Amp. Effort was taken to make sure the current is kept constant by keeping the reference of current taken for a stress voltage at 50 V. And, for every stress voltage, the current was matched to the initial reference current. Thus making sure, the start and end of the device current are the same for all the stress voltage measurements.

Effect of off-state voltage

This is the first scenario where T1 = 3 μs, T2 = 2.5 μs and T3 = 2.5 μs for a drain current of 3 Amp.

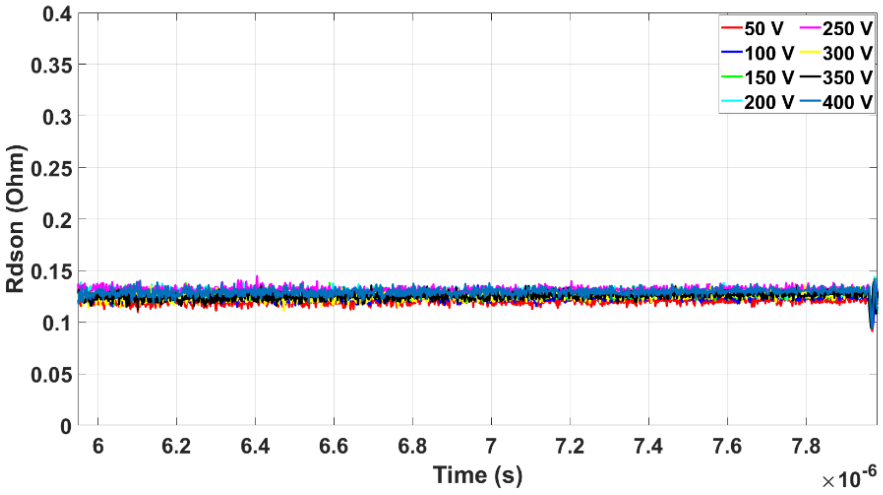


Figure 96: The Dynamic on-state resistance for Device 1 after T1 = 3 µs, T2 = 2.5 µs and T3 = 2.5 µs for 3 Amp device current.

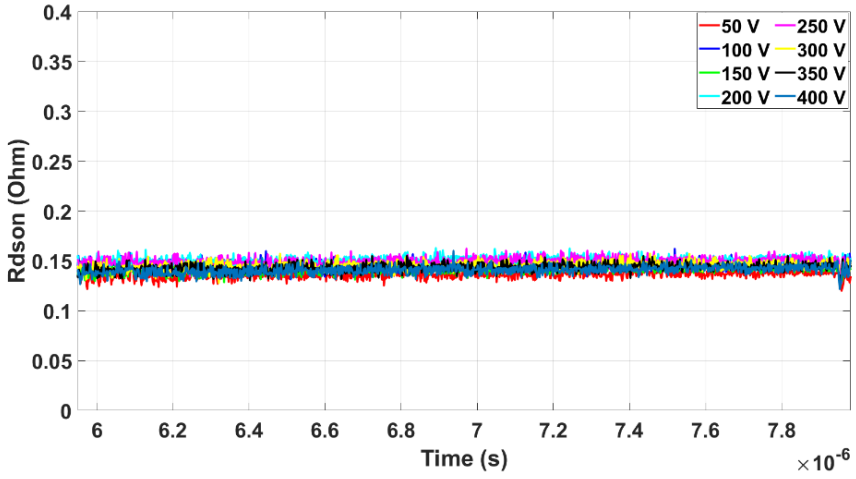


Figure 97: The Dynamic on-state resistance for Device 2 after T1 = 3 µs and T2 = 2.5 µs for 3 Amp device current

Figure 96 to Figure 99 shows the dynamic on-state resistance of both the devices for 3 Amp and 7 Amp for the same time interval. The dynamic $R_{DS(on)}$ data is taken after 500 ns of switching on the device. This is to avoid the initial switching noise.

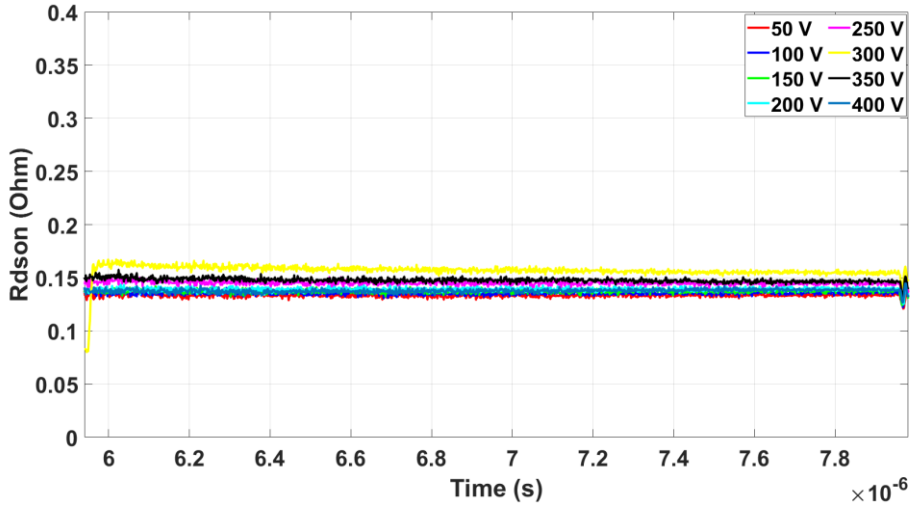


Figure 98: The Dynamic on-state resistance for Device1 after T1 = 3 µs , T2 = 2.5 µs and T3 = 2.5 µs for 7 Amp device current.

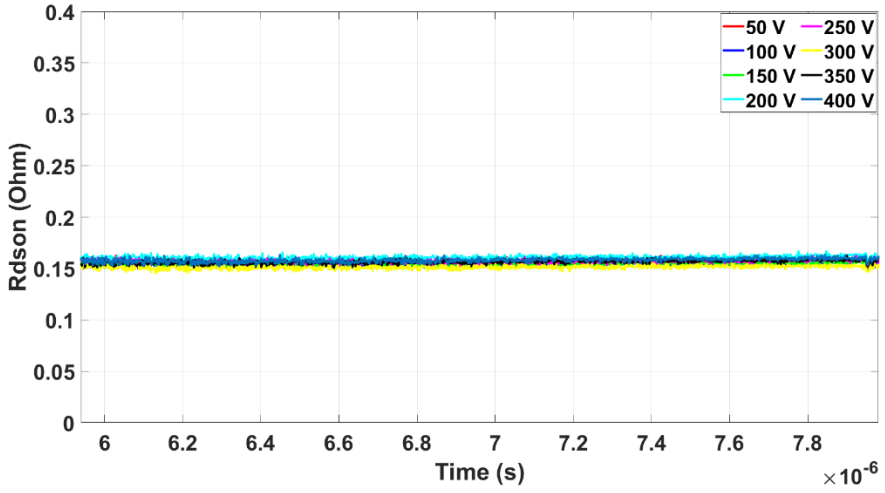


Figure 99: The Dynamic on-state resistance for Device 2 after T1 = 3 µs , T2 = 2.5 µs and T3 = 2.5 µs for 7 Amp device current.

It can be observed from the figures that the dynamic on-state resistance does not increase much for both the devices with respect to their stress voltage. For 3 Amp both the devices did not show an increase in the dynamic on-state resistance. For 7 Amp it can be seen that there is slight increase in the dynamic on-state resistance for Device 1, whereas for Device 2 the trend shows to not increase with stress voltage. Figure 100 shows the consolidated

data of the dynamic on-state resistance. As it can be seen Device 2 does not show much variation with the drain voltage.

For Device 1 it can be seen that there is a slight increase till 300 V for 7 Amp drain current and then decreases until 400 V. And, the same trend can be seen for 3 Amp as well, there is a small increase till 250 V and decreases until 400 V. Whereas, for Device 2, the on-state resistance remains almost constant at around 0.13 for 3 Amp and 0.15 for 7 Amp.

It can also be observed that the dynamic on-state resistance remains constant over the period and does not decay much after the device turns on.

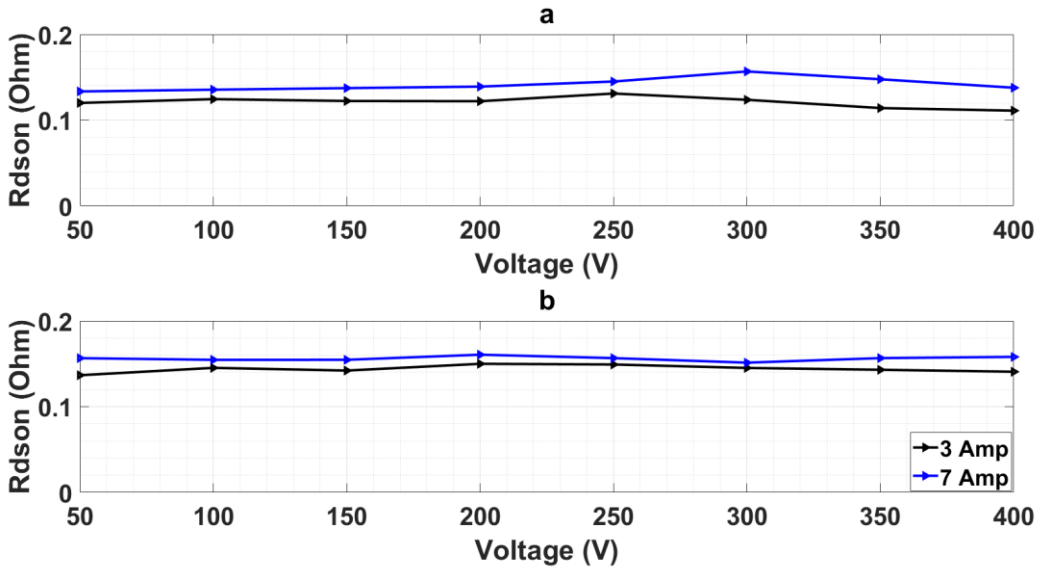


Figure 100: Dynamic on-state resistance for 3 Amp and 7 Amp for after T1 = 3 µs , T2 = 2.5 µs and T3 = 2.5 µs (a) Device 1 (b) Device 2

Effect of drain current

For this test, drain current from 3 Amp to 12 Amp was applied for a drain voltage of 400 V. The Dynamic on-state resistance can be seen from the Figure 101 for Device 1 and Figure 102 for Device 2. For Device 1 it can be clearly seen that, there is an increase of Dynamic on-state resistance when the drain current increases. A small increase can be seen from 3 Amp to 5 Amp. From 5 Amp to 7 Amp there seem to be no much rise in the dynamic on-state resistance. And, from 9 Amp to 12 Amp, there is a clear steep increase. For currents from 3 Amp to 7 Amp as time passes there seem to be no much decay, whereas at higher currents the decay of the dynamic on-state resistance seems to be more significant. This

trend corresponds to the previous literature where the drain current was increased from 5 Amp to 15 Amp, and the dynamic on-state resistance is shown to increase with the drain current [115].

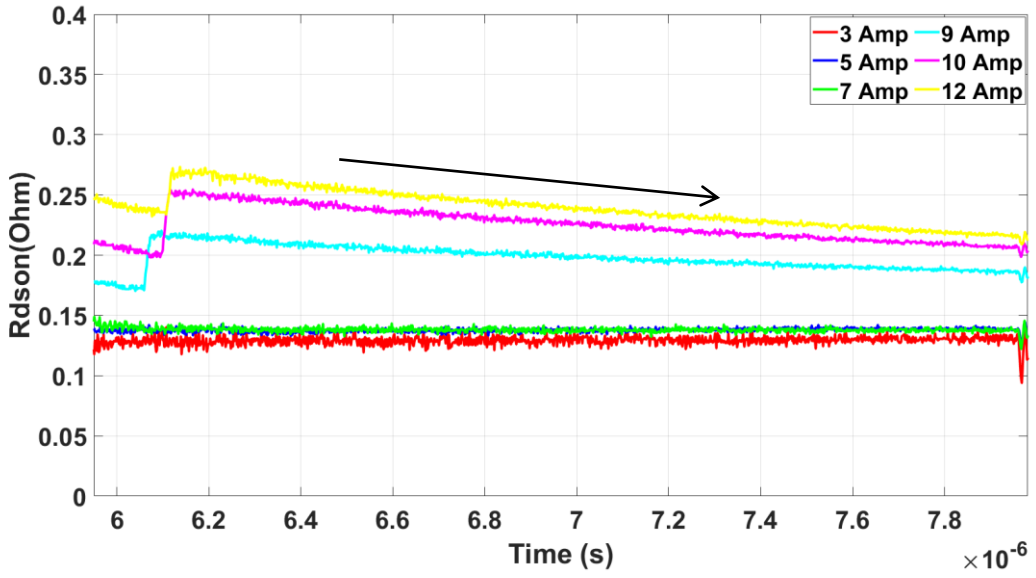


Figure 101: Dynamic On-state resistance for Device 1 after T1 = 3 µs , T2 = 2.5 µs and T3 = 2.5 µs for currents 3 Amp to 12 Amp

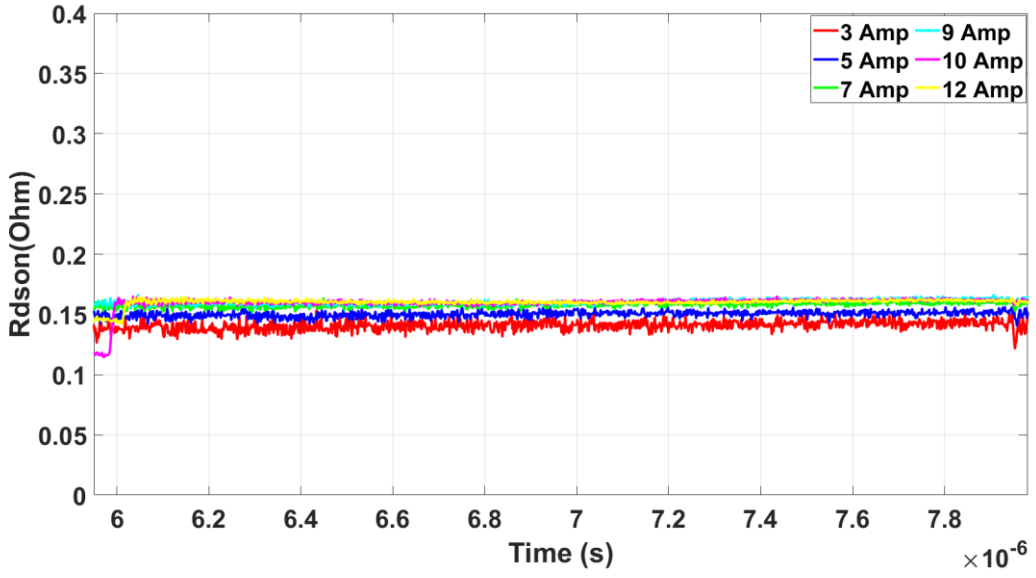


Figure 102: Dynamic On-state resistance for Device 2 after T1 = 3 µs , T2 = 2.5 µs and T3 = 2.5 µs for currents 3 Amp to 12 Amp

Whereas for Device 2, a slight increase was observed from 5 Amp to 7 Amp. Unfortunately, no increase was shown for rest of the drain current. Same as previous results, no pattern of severe increase in the on-state resistance was observed for Device 2.

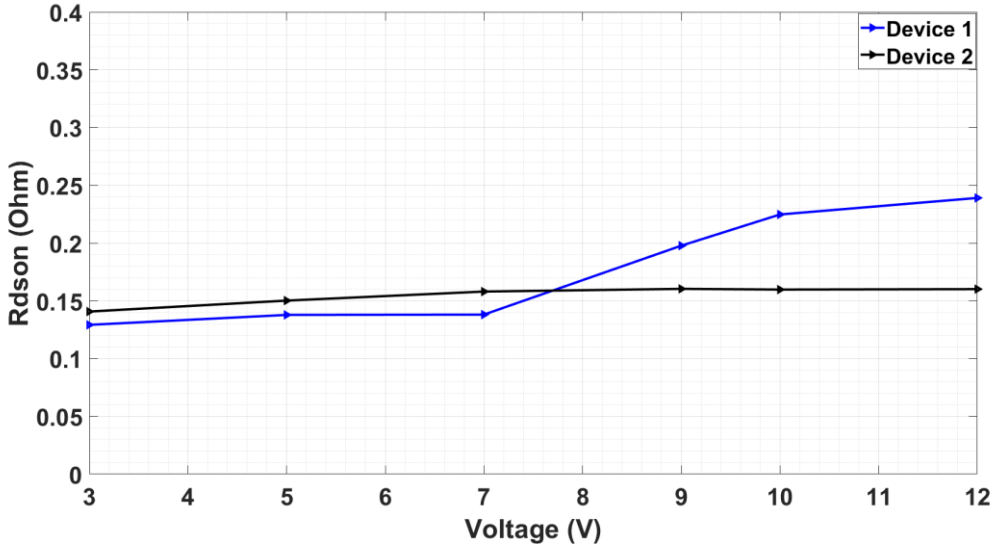


Figure 103: Dynamic on-state resistance of both the devices for varying drain current

Figure 103 shows the consolidated data for both the device for different drain currents. As discussed the dynamic on-state resistance for Device 2 does not change much from 3 Amp to 12 Amp. At 3 Amp device current, for Device 2, the dynamic on-state resistance is about 0.14 Ohm and increases to 0.16 Ohm. This is only an increase of 14% which isn't much of an increase as compared to Device 1, which has been observed to have an increase of 91% from 3 Amp to 12 Amp.

For further analysis, Device 1 was considered. The experiments were done to understand if changing the stress time during the first interval would affect the dynamic on-state resistance. In this scenario the T1 interval was increased to 5 µs and the rest of the time interval remained the same. Only one previous research [106] using the same clamping circuit was found to use different stress times to observe the effect on the dynamic on-state resistance. Therefore, here the stress time T1 is changed to 5 µs. The effect of change in T1 is observed for varying drain currents. As can be seen from Figure 105, the dynamic on-state resistance for the time interval T1 = 3 µs is lower when compared to the T1 = 5 µs. For T1 = 3 µs there is an increase from 0.12 Ω to 0.23 Ω. And, for T1 = 5 μs there is an increase from 0.16 Ω to 0.37 Ω. Although this is not a significant increase, it can be seen that by increasing the stress interval T1, there is a slight change in the dynamic on-state

resistance. However, for currents from 3 Amp to 7 Amp and T1 = 5 µs, a small decrease in the on-state resistance can be observed.

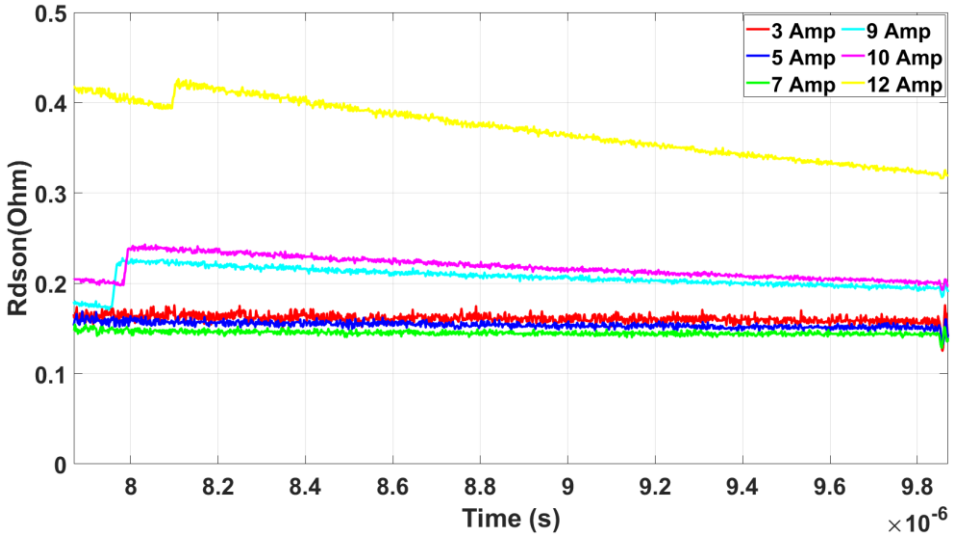


Figure 104: Dynamic On-state resistance for Device 1 after T1 = 5 µs , T2 = 2.5 µs and T3 = 2.5 µs for currents 3 Amp to 12 Amp

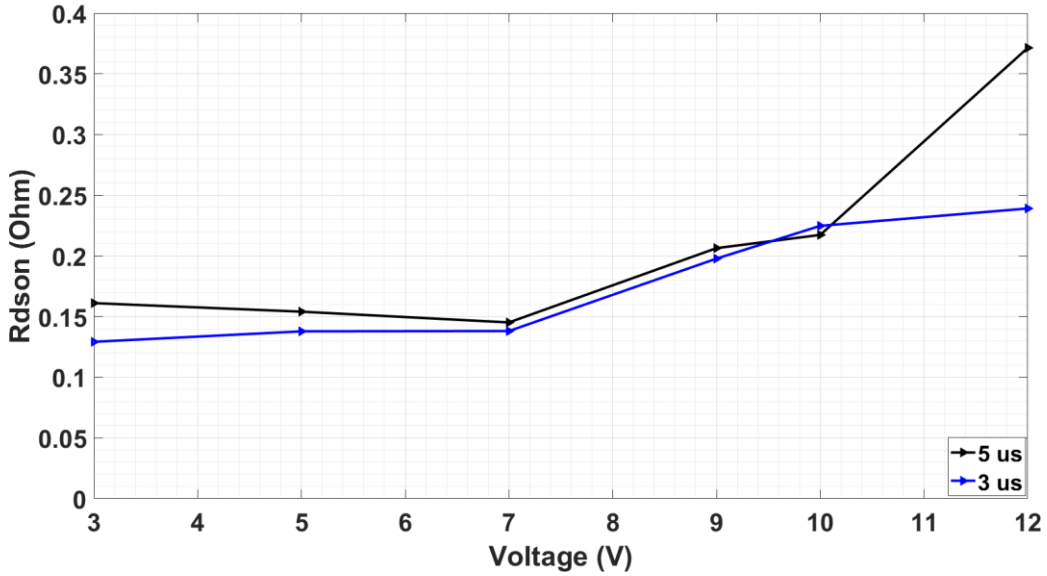


Figure 105: Dynamic On-state resistance for Device 1 for T1 = 5 µs and T1 = 3 µs, T2 = 2.5 µs and T3 = 2.5 µs

Challenges faced while measuring GaN cascode using the clamping circuit

As can be seen from the above results, there is not much difference in the on-state resistance for Device 2 when compared to Device 1. Although, both devices are from the same manufacturer but in different packages. Unfortunately, the author could not find a clear pattern of trend between the both of them. There could be many possibilities for this phenomenon. The clamping measurement will highly be affected by the parasitics giving rise to unstable results. Previous literature does not provide a unified answer as to how dynamic on-state resistance of GaN cascode behaves under different stress times or different drain currents. The results obtained here can be taken as a guideline to further investigate the current collapse phenomena in cascode devices. Following are a few suggestions that can be considered in the future for measuring the dynamic on-state resistance for cascode devices.

1. Need for a dedicated circuit to test GaN cascode devices. Taking into consideration the internal parasitics of the device and how it may affect the clamping circuitry.
2. The use of correct components and measurement equipment - As cascode devices are prone to external inductances arising from measurement probes. And, the clamping voltage is measured on the scale of 200 mV/div. This small division paired with the cascode parasitics can bring in severe noise which can affect the measurement. Especially when the calculated dynamic on-state resistance is less than 1 Ohm. Also, at higher currents, measurement for Device 1, the dynamic on-state resistance seems to increase. Considering not much increase in the dynamic on-state was seen for lower currents and with varying stress voltage, the extreme change of dynamic on-state at higher currents could also be due to an error in the measurement. This possibility could not be ruled out.
3. Another challenge is that High Voltage GaN HEMT device characteristics can be masked by the Low Voltage Silicon, thus making it a bit difficult to observe the trend that occurred due to changes in resistance.

One final analysis was done by changing the T2 pulse width.

As mentioned above, the stress time T2 is controlled to understand the effect of off-time stress on the dynamic on-state. The second pulse T2 was increased to 10 μs keeping T1 = 3 μs and T3 = 2.5 μs.

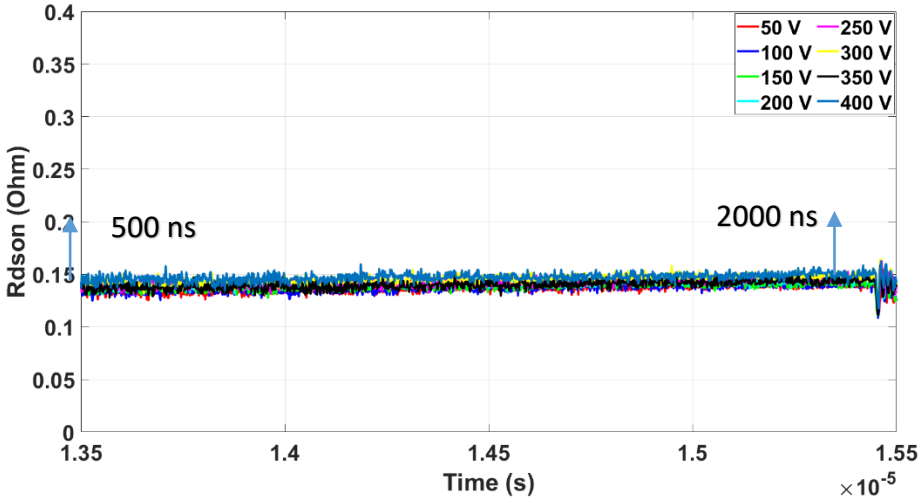


Figure 106: Dynamic On-state resistance for Device 1 for T1 = 3 µs and T2 = 10 µs for a device current of 3 Amp

Figure 106, represents the dynamic on-state resistance when T2 was changed to 10 μs. As mentioned in the above section, there were four research that were found to implement the same clamping circuit. The first three papers experimented with having a fixed pulse width set at T1 = 2 μs, T2 = 2 μs and T3 = 2 μs. But, in [106] it can be seen that by increasing the pulse width T2 i.e. the off-stress time, the dynamic on-state resistance tends to increase with time during the on-state.

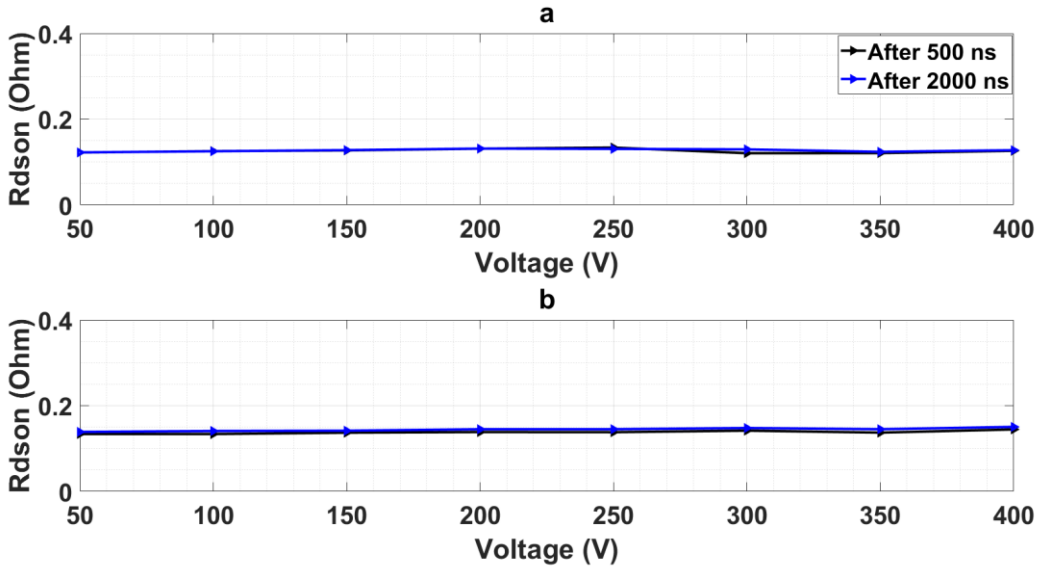


Figure 107: Dynamic On-state resistance for Device 1 for device current of 3 Amp after 500 ns and 2000 ns of turn on (a) T1 = 3 µs and T2 = 2.5 µs (b) T1 = 3 µs and T2 = 10 µs

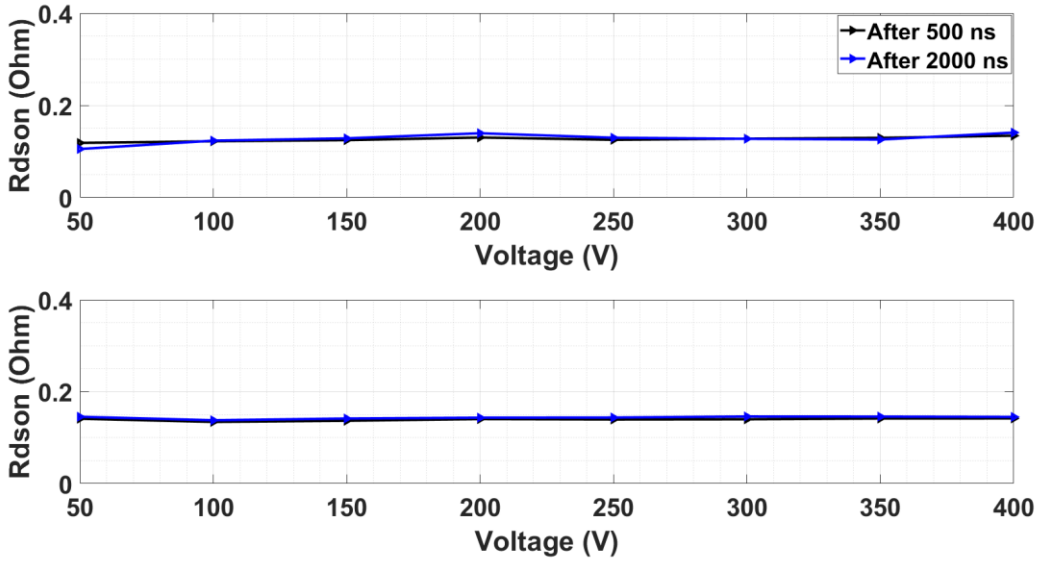


Figure 108: Dynamic On-state resistance for Device 1 for device current of 3 Amp after 500 ns and 2000 ns of turn on (a) T1 = 5 µs and T2 = 2.5 µs (b) T1 = 5 µs and T2 = 10 µs

The same trend can be observed here, even though the increase is not that prominent, consolidated data is presented to understand the pulse width dependence of the dynamic on-state resistance over time. Figure 107 represents the measurement data where the T1 pulse was set to 3 μs and T2 varying. The measurement is shown for two points after the turn on of the device, one is after 500 ns and the other after 2000 ns. The conventional phenomenon is that, once the device is turned on after a period of stress, the device takes some time to de-trap the electrons and the on-state resistance will recover depending on the de-trapping process of the measured device. So the data taken at 500 ns will be higher than the one taken at 2000 ns, proving the de-trapping process. However, here when the stress time is smaller T2 = 2.5 µs. The values for 500 ns and 2000 ns remain almost similar whereas when T2 = 10 µs, the values for 2000 ns are slightly higher than 500 ns. The same trend can be seen in [106]. This goes on to show that the settling time of the dynamic on-state could probably depend on the length of off-time stress as well.

6.5 Summary

This chapter is dedicated to understanding the measurement technique of dynamic on-state resistance. A brief review of the previous literature is provided. The main papers describing the measurement of dynamic on-state resistance of cascode devices are described. The effect of soft and hard switching is discussed and it was found that there are different

narratives with regards to the realisation of dynamic on-state resistance when measured under hard and soft switching. Next, the measurement results for two cascode devices are shown, even though both devices are from the same manufacturer with the same rating. Device 1 showed a slight change in the dynamic on-state resistance with respect to varying stress voltage and varying drain current. Whereas no significant trend was observed for Device 2. Since no significant change in the dynamic on-state resistance was found, further analysis was done to understand the effect of different time intervals on the decay process of the dynamic on-state resistance. For Device 1 the T1 pulse was changed to 5 µs and the dynamic on-state resistance was calculated for different drain currents and a small variation was observed. The dynamic on-state resistance for when the T1 = 3 µs was found to be 0.23 Ω and for T1 = 5 µs was found to be 0.37 Ω. And, for the next analysis, the pulse width T2 was increased from 2.5 µs to 10 µs. Again, dynamic on-state resistance dependency on off-time stress was observed.

The results shown here did not show a sufficient change in the dynamic on-state resistance for both devices from which it can be given a proper conclusion. A few challenges for the measurement of cascode devices and what can be done to mitigate this are provided in the chapter. Therefore, the work presented here can be taken as an example and a stepping stone to further undertake the dynamic on-state resistance measurement for cascode devices.

Chapter 7: Conclusion and Future Work

The main objective of this thesis was to experimentally evaluate the performance of GaN cascode devices in different packages. Three different packages TO-247, CCPAK, and TO-220 were investigated thoroughly and compared with Silicon. Other two topics included the modelling of a normally-on GaN device SaberRD and examining the dynamic on-state resistance of cascode devices. In this section, a summary of the conclusion drawn from each chapter is presented.

The first chapter, mentions the motivation behind the use of GaN devices. The need for renewable sources of energy is discussed and the role of power electronics is discussed. The chapter concluded by giving an outline of the thesis.

The second chapter forms the literature review and lays a foundation for the rest of the thesis. The main topics covered in the following chapters and the previous research conducted related to them are mentioned. Starting from the fundamental property of Normally-on D-mode GaN to Normally-off E-mode and cascode structure. GaN devices are inherently normally-on devices. This is because of the formation of 2DEG due to the polarisation property. One of the options to make them normally-off is the cascode structure. The cascode has a low voltage Si-MOSFET with high voltage GaN HEMT in series. The gate of the device is provided by the Si-MOSFET. This makes the device suitable for most of the gate drivers, unlike the e-mode GaN. Although the cascode structure has many advantages, there are a few factors that affect the realisation of their full potential. The main factor is the internal parasitics arising from the interaction between the two devices, such as the capacitors and the inductance due to the wire bonding between the two devices. The explanation about the working of the parasitic capacitance is explained in Chapter 2 leading to the discussion of three different operation modes of the device, namely Forward blocking mode, Forward conduction mode and reverse conduction mode. Due to the internal parasitics, false turn-on of the gate, and unwanted oscillations at the drain to source voltage are observed for the cascode devices. Therefore, a carefully designed gate driver with minimum gate-loop and power-loop inductance is needed to characterise the devices. Another, factor determining a smooth switching waveform is the packaging. Cascode devices come in both through-hole and surface-mount packaging. The traditional 3-leaded through-hole package has long leads and can induce further inductance to the

measurement results. The surface mount packaging can limit the oscillations to a certain extent. The chapter lists various available packaging and their manufacturer along with their ratings. Finally, the current collapse phenomena that are observed in GaN devices are discussed. First, the physical mechanism that causes the current collapse is explained. Then, the clamping circuit required to measure the dynamic on-state resistance is discussed in detail.

The third chapter starts with the experiment methodology i.e. the explanation of the Double Pulse Tester setup. The explanation for each component used in the setup is discussed. For devices like GaN cascode where the switching characteristics can be influenced by the internal parasitics, the measurement practices need to be carried out in a certain way. Starting with oscilloscope probing – the conventional long ground lead is not suitable for measuring the drain-source voltage because of the influence of the inductance brought in by the ground lead. Therefore, a shorter wire is considered here to measure the voltage signal. The other important measurement is the drain to source current. Due to the fast-switching nature of GaN devices, a Current Shunt Resistor (CSR) is considered for current measurement. However, it was seen that the use of some CSR can induce oscillations in the gate-to-source and gate-to-drain voltages. The influence of two different shunt resistors one which has a resistance of 0.5 Ohm and the other with 0.102 ohm in the power-loop path is discussed and the results for both scenarios are discussed. The components and the devices used for the investigation of switching characteristics are listed as well.

The fourth chapter is dedicated to the evaluation of cascode devices in three different packages. The three packages chosen are TO-247, TO-220 and CCPAK. Two of them are through-hole packaged and the other one is surface mount. The chapter starts with understanding both TO-247 and CCPAK package inductances. The literature states that the most critical inductance for GaN cascode is the common source inductance (CSI), and CCPAK has the CSI reduced by 90% for TO-247 and by 85% for TO-220. This can help in reducing the turn-on losses significantly. The turn-on and turn-off waveforms of TO-247 and CCPAK are compared with each other. It was shown that the turn-on transition time of TO-247 is higher by 18% when compared with CCPAK. Whereas the turn-off transition time is higher for CCPAK by a few nanoseconds. Further analysis is done for currents from 3 Amp to 12 Amp, and resistors from 15 Ω to 100 Ω. The results obtained from the analysis showed that the turn-on losses for CCPAK are consistently low when compared to the other two packages. However, the turn-off losses of CCPAK were found to be higher for lower

currents when compared to TO220. But for higher currents, the CCPAK showed good performance. When compared with TO247 for a drain current of 12 Amp, a reduction of 23.7% and for TO-220 13.1% was observed. Thus, making CCPAK good for high-current applications.

The fifth chapter consists of two sections, the first one is focused on establishing the switching characteristics of Si-CoolMOS devices under varying resistors and varying drain currents. It was observed that the Si-CoolMOS when compared with CCPAK, the turn-on transition time for Si device is higher by 78% and the turn-off transition is higher by 46%. The energy losses obtained for Si-CoolMOS at 12 Amp drain current are observed to be around 5 times more than the CCPAK. The energy losses of all four devices were compared with each other to establish the superior nature of GaN. The results aligned with the previous literature on GaN, where GaN devices outperform Si devices in terms of providing lower switching losses even at higher currents. The second section consists of the characterisation and modelling of the device in the Power MOSFET Tool provided by SaberRD. The PMT allows the modelling of devices with the help of data-sheet values. The tool provides different sections dedicated to each characterisation curve. The important benefit of the tool is that, even if the device is in the early stage of development, for example only the transfer characteristics of the device are available such as the $I_D - V_{DS}$ or $I_D - V_{GS}$ and device capacitance data. With the help of these curves, other device data such as the gate charge and the $R_{DS(on)}$ data can be predicted. This can help in understanding the device's behaviour before implementing it in an experimental environment. Therefore, in this section, a 1.2 kV Polarisation Super Junction GaN is modelled with the help of, $I_D V_{GS}$ and capacitance curves. This is the first time the device is modelled in SaberRD. The modelling has helped in predicting the gate charge of the device. The step-by-step procedure for calculating the gate charge is explained in detail. The switching characteristics of the modelled device are explained and the switching transient time, dv/dt analysis and switching energy for drain currents 3 Amp to 7 Amp is presented. The modelled device and the simulation results presented in this chapter can be used as a reference to help with implementing the device in an experimental setup.

The sixth chapter is dedicated to understanding the measurement of dynamic on-state resistance. A double pulse tester is implemented along with the clamping circuit across the drain to the source voltage terminal for the measurement. The chapter starts with exploring previous literature based on the same clamping circuit implemented for the work conducted

here. Three main research were found to discuss the dynamic on-state resistance of GaN cascode devices. Although, from previous literature not much increase in the dynamic $R_{DS(on)}$ was seen for GaN cascode devices. The measurement of dynamic on-state can be conducted under two switching operations, hard and soft-switching. The working of both switching operations and how they affect the current collapse phenomenon seen in GaN devices is discussed in detail. For some devices, the dynamic on-state resistance under hard switching gives a higher value when compared with soft-switching operations. There is no unified clarification found in the literature that confirms which operation provides better performance when realising the dynamic on-state resistance. In this chapter, two cascode devices are used for evaluation. The clamping circuit and its working is explained in detail. Two pulses are given to the gate of the Device Under Test. The first pulse determines the device current, the second pulse is when the device is in the off-state and the third pulse is where the dynamic on-state resistance is calculated. Unfortunately, no significant change in the dynamic on-state resistance was found for Device 2. Whereas for Device 1, slight change could be observed for different drain currents and different stress times. However, the results presented here could not help in understanding the change in dynamic on-state resistance in a proper way. That is, a clear understanding of the de-trapping process as well as the change of on-state resistance with respect to varying stress voltage could not be found. However, the author has tried to establish connections between stress time and the dynamic-on-state resistance based on previous literature. The presented results can be taken as a foundation for any future work related to the measurement of cascode on-state resistance.

7.1 Future Work

GaN devices are attracting more researchers to exploit the advantages such as their high frequency switching, low switching losses etc. And, this thesis explored the switching characteristics of the cascode devices in different packages as well as the current collapse phenomena. A few key topics can help in expanding the work conducted in this thesis.

1. Converter design with the new CCPAK package. In this thesis, only the switching characteristics of the device are discussed. Which is a good starting point for understanding how the device performs. Since the characterisation of the device is

established next step in this area would be to build a converter and understand how the thermal management functions in the new package.

2. Switching characterisation of 1.2 kV Polarisation Super Junction GaN. However, the turn-off dv/dt controllability analysis of the device was studied in previous research [94]. Further study can be done on the experimental switching characteristics and their effect on different operating conditions. 1.2 kV Polarisation Super Junction GaN, in cascode configuration is also a potential research area under this category.

   SaberRD simulation of commercial cascode devices. With the help of available information on the parasitic inductances – which is available from the spice models provided by the company. And, if the device information of LV Silicon and HV GaN is available as well a device model similar to the physical one can be generated which can help in modelling system-level simulations. This can be beneficial not just for research purposes but also on an industrial level.

3. Dynamic on-state resistance still becomes a challenge in realising the full potential of the GaN devices. There is only a little research done on the mechanism of current collapse in cascode devices. In this thesis, a previously explored clamping circuit was implemented to observe the Dynamic on-state resistance of cascode devices. The effect of internal parasitics and how it may affect the measurement is not considered. Therefore, a good way to approach this problem would be to build a clamping circuit dedicated to cascode devices. One of the previous research [107] focuses on making a novel clamping circuit but further analysis based on different stress times and the effect of drain current/voltage based on a novel circuit can be the next key focus.

   The Dynamic on-state resistance of PSJ GaN is another potential research area. The PSJ device due to its flattened electric field reduces the on-state resistance, but further investigation with an appropriate clamping circuit can help in understanding the change in resistance and how the device differs from the conventional GaN devices.

4. Slew rate controllability for GaN cascode devices, as very little research has been done on the dv/dt controllability for cascode devices because the conventional method of controlling the slew rate involves the use of external gate resistors and, as the dv/dt of the GaN devices also depend upon the high voltage GaN HEMT. It becomes difficult to access the gate of the device. One of the existing approaches is the direct-drive method. Which, from the research mentioned here [81] would require a carefully designed setup to control the gate of GaN HEMT. And, proper circuit layout by

reducing the parasitics is also required. Therefore, this is a potential area for further investigation.

Chapter 8 Appendix

8.1 PCB Layout

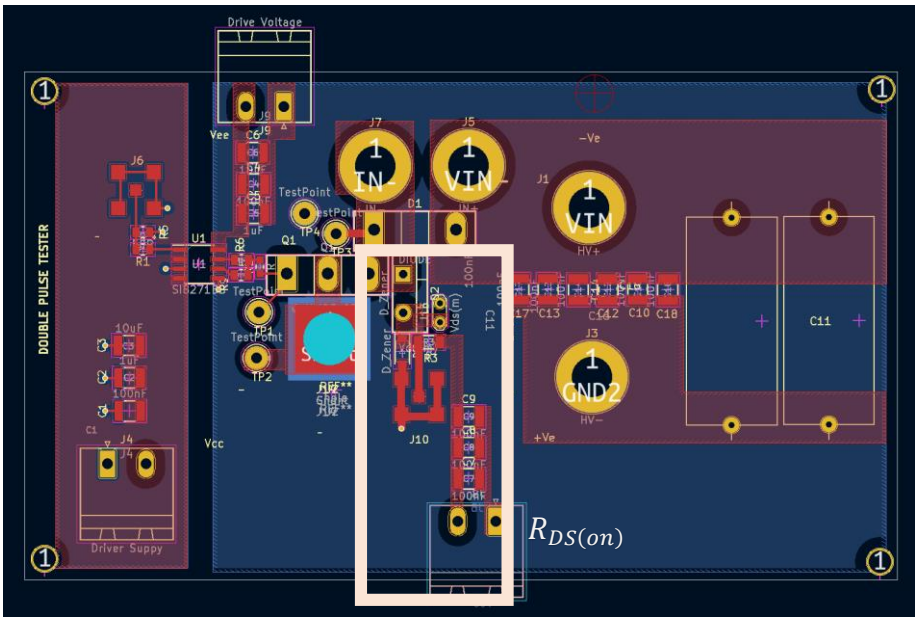


Figure 109: PCB layout for TO-247 Package along with dynamic on-state measurement circuit

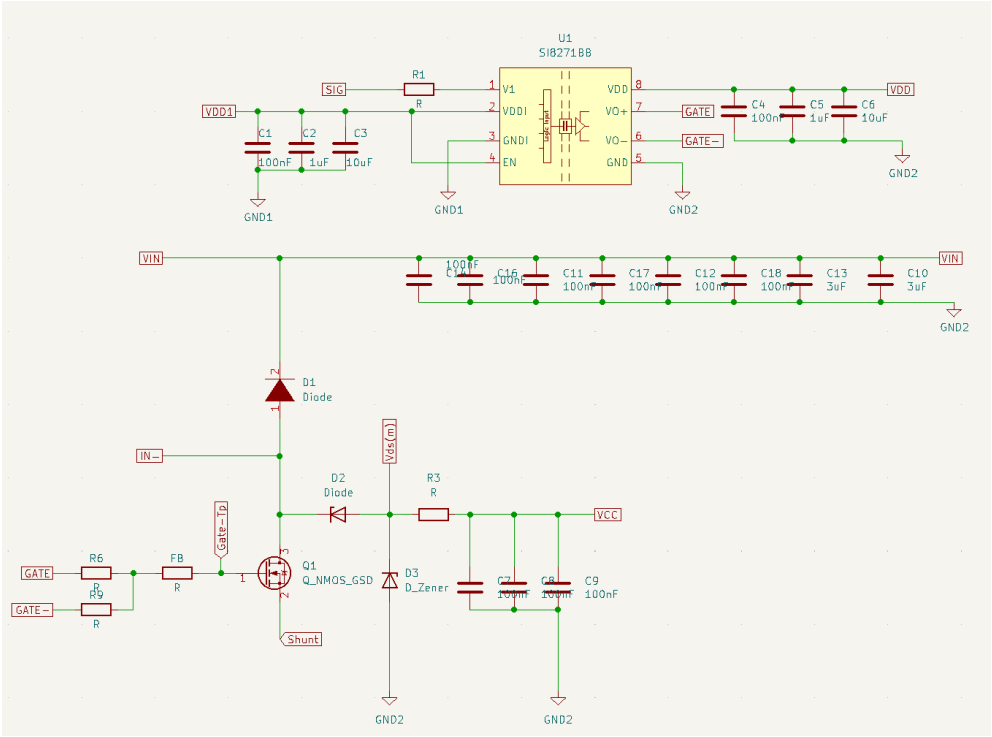


Figure 110: Schematic view of the switching measurement along with dynamic on-state measurement circuit

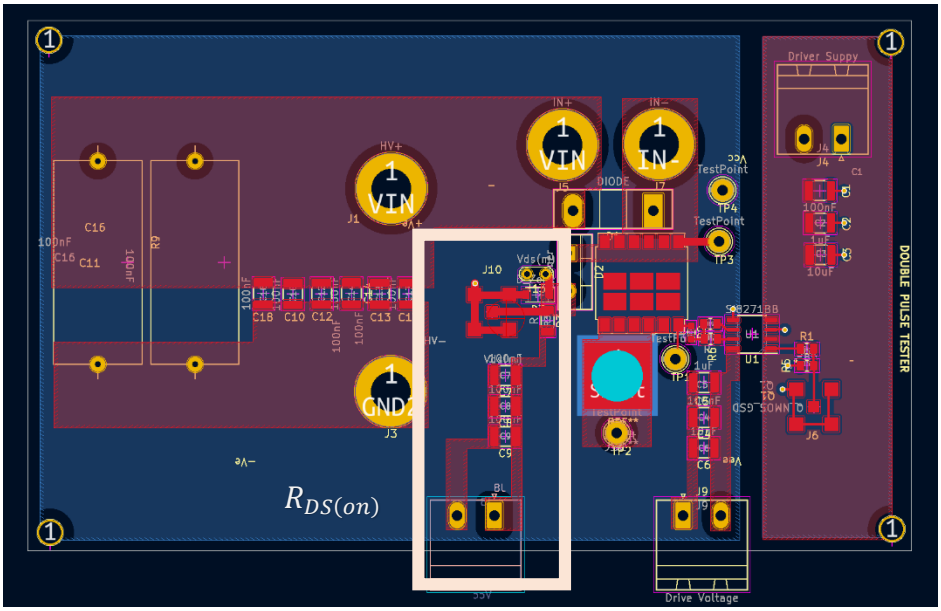


Figure 111: PCB layout for CCPAK Package along with dynamic on-state measurement circuit

8.2 Device Data Sheet

This section provides the first page of the datasheet of the devices implemented in the thesis. The full datasheet is available online and is cited against each part number - provided in Chapter 3, Table 4.

GAN041-650WSB

650 V, 35 mΩ Gallium Nitride (GaN) FET in a TO-247 package

4 June 2024 Product data sheet

1. General description

The GAN041-650WSB is a 650 V, 35 mΩ Gallium Nitride (GaN) FET in a TO-247 package. It is a normally-off device that combines Nexperia's latest high-voltage GaN HEMT H2 technology and low-voltage silicon MOSFET technologies — offering superior reliability and performance.

2. Features and benefits

- Ultra-low reverse recovery charge
- Simple gate drive (0 V to +10 V or 12 V)
- Robust gate oxide (±20 V capability)
- High gate threshold voltage (+4 V) for very good gate bounce immunity
- Very low source-drain voltage in reverse conduction mode
- Transient over-voltage capability

3. Applications

- Hard and soft switching converters for industrial and datacom power
- Bridgeless totempole PFC
- PV and UPS inverters
- Servo motor drives

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 175 °C		-	-	650	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	-	47.2	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	187	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 32 A; T_j = 25 °C; Fig. 11		-	35	41	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 32 A; V_{DS} = 400 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 13; Fig. 14		-	6.6	-	nC
$Q_{G(tot)}$	total gate charge			-	22	-	nC
Source-drain diode							
Q_r	recovered charge	I_S = 32 A; dI_S/dt = -1000 A/µs; V_{GS} = 0 V; V_{DS} = 400 V; Fig. 20		-	150	-	nC

nexperia

GAN039-650NBB

650 V, 33 mOhm Gallium Nitride (GaN) FET in a CCPAK1212 package

28 May 2024 Product data sheet

1. General description

The GAN039-650NBB is a 650 V, 33 mΩ Gallium Nitride (GaN) FET in a CCPAK1212 package. It is a normally-off device that combines Nexperia's latest high-voltage GaN HEMT H2 technology and low-voltage silicon MOSFET technologies — offering superior reliability and performance.

2. Features and benefits

- Simplified driver design as standard level MOSFET gate drivers can be used:
  - 0 V to 12 V drive voltage
  - Gate threshold voltage V_{GSth} of 4 V
- Robust gate oxide with ±20 V V_{GS} rating
- High gate threshold voltage of 4 V for gate bounce immunity
- Low body diode V_f for reduced losses and simplified dead-time adjustments
- Transient over-voltage capability for increased robustness
- CCPAK package technology:
  - Improved reliability, with reduced $R_{th(j-mb)}$ for optimal cooling
  - Lower inductances for lower switching losses and EMI
  - 150 °C maximum junction temperature
  - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
  - Easy solder wetting for good mechanical solder joints

3. Applications

- Hard and soft switching converters for industrial and datacom power
- Bridgeless totempole PFC
- PV and UPS inverters
- Servo motor drives

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 150 °C		-	-	650	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	-	58.5	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	250	W
T_j	junction temperature			-55	-	150	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 32 A; T_j = 25 °C; Fig. 10		-	33	39	mΩ
		V_{GS} = 10 V; I_D = 32 A; T_j = 150 °C; Fig. 11		-	73	86	mΩ

nexperia

transphorm

TP65H070G4PS

650V SuperGaN® GaN FET in PQFN (source tab)

Description

The TP65H070G4PS 650V, 72mΩ Gallium Nitride (GaN) FET is a normally-off device. It combines state-of-the-art high voltage GaN HEMT and low voltage silicon MOSFET technologies—offering superior reliability and performance.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge

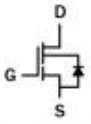
Related Literature

- AN0009: Recommended External Circuitry for GaN FETs
- AN0003: Printed Circuit Board Layout and Probing
- AN0010: Paralleling GaN FETs
- AN0014: Low cost driver solution

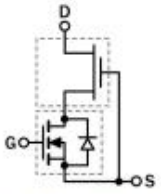
Ordering Information

Part Number	Package	Package Configuration
TP65H070G4PS	3 lead TO-220	Source

TP65H070G4PS
TO-220
(top view)



Cascode Schematic Symbol



Cascode Device Structure

Features

- Gen IV technology
- JEDEC-qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Robust design, defined by
  - Wide gate safety margin
  - Transient over-voltage capability
- Very low Q_{RR}
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging

Benefits

- Achieves increased efficiency in both hard- and soft-switched circuits
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

Applications

- Datacom
- Broad industrial
- PV inverter
- Servo motor
- Computing
- Consumer

Key Specifications	
V_{DSS} (V)	650
$V_{DSS(TR)}$ (V)	800
$R_{DS(on)eff}$ (mΩ) max*	85
Q_{OSS} (nC) typ	78
Q_G (nC) typ	9

* Dynamic on-resistance; see Figures 18 and 19

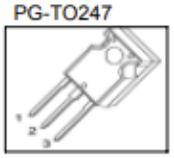
Cool MOS™ Power Transistor

V_{DS} @ T_{jmax}	650	V
$R_{DS(on)}$	0.07	Ω
I_D	47	A

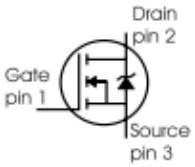
Feature

- New revolutionary high voltage technology
- Worldwide best $R_{DS(on)}$ in TO 247
- Ultra low gate charge
- Periodic avalanche rated
- Extreme d*v*/d*t* rated
- Ultra low effective capacitances
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC[0)] for target applications

PG-TO247



Type	Package	Ordering Code	Marking
SPW47N60C3	PG-TO247	Q67040-S4491	47N60C3



Maximum Ratings

Parameter	Symbol	Value	Unit
Continuous drain current T_C = 25 °C T_C = 100 °C	I_D	 47 30	A
Pulsed drain current, t_p limited by T_{jmax}	$I_{D\,puls}$	141	
Avalanche energy, single pulse I_D = 10 A, V_{DD} = 50 V	E_{AS}	1800	mJ
Avalanche energy, repetitive t_{AR} limited by T_{jmax}[1] I_D = 20 A, V_{DD} = 50 V	E_{AR}	1	
Avalanche current, repetitive t_{AR} limited by T_{jmax}	I_{AR}	20	A
Gate source voltage static	V_{GS}	±20	V
Gate source voltage AC (f >1Hz)	V_{GS}	±30	
Power dissipation, T_C = 25°C	P_{tot}	415	W
Operating and storage temperature	T_j, T_{stg}	-55... +150	°C
Reverse diode dv/dt [4)]	dv/dt	15	V/ns

Chapter: 9 References

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