Susceptibility Predictions of ICs to EMI and Validation of Stochastic EM fields Coupling with a Bespoke RF IC Detector

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Doctor of Philosophy

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January 2024

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

Abstract

This research addresses electromagnetic interference (EMI) challenges at high frequencies by developing an advanced methodology to estimate the probability of susceptibility of Integrated Circuits (ICs). The objective is to develop an advanced methodology for estimating the probability of susceptibility of ICs or components on a printed circuit board (PCB) to EMI by statistically characterizing the power absorbed by electronic circuits and enhancing power balance (PWB) methods for enclosures and internal components. The IC EMC standard IEC 62132-4, enables the assessment of susceptibility of an IC by determining the forward power required to induce a malfunction at each pin. This work enhances the previously developed numerical model by incorporating PCB losses, which enables us to estimate the distribution of coupled forward power at the package pin over a number of stirrer positions in a reverberant field. Based on these insights, the research establishes a methodology for predicting the probability of susceptibility of ICs, provided that the component's susceptibility level, transmission line parameters, and the loading of the attached track are known.

This work also validates the numerical model through the design and testing of an instrumented custom-designed radio frequency integrated circuit (RF IC) detector, capable of measuring coupled power at its package pin via test PCB tracks. Building upon previous knowledge of PWB methods, using the purpose-built RF IC detector we introduced an enhanced PWB method capable of incorporating the influence of average absorption cross-section (AACS) of the IC at package pins and connected PCB tracks, along with other relevant AACS for internal components within the enclosure. The in-depth consideration of AACS of the components such as PCB tracks and ICs on the device under test, is an upgrade to previously developed PWB methods.

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Dedicated to my Father

He was always with me when I needed him the most, I wish he was here to see my work.

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Table of Contents

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

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Table of Figures

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This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790. https://etn-peter.eu/

List of Tables

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Acknowledgement

I am immensely grateful to my supervisors, Dr. John Dawson and Dr. Martin Trefzer, for their invaluable guidance and continuous support throughout my academic journey. My heartfelt thanks extend to the members of the Applied Electromagnetics Group at the University of York, particularly Prof. Andy Marvin, Dr. Simon Bale, and Dr. Martin Robinson, whose insightful suggestions were invaluable.

I express my gratitude to visiting researchers Dr. Haiyan Xie and Dr. Hui Tang for their collaborative efforts during their tenure at the University of York.

My sincere appreciation and gratitude goes to the funding Institution and the PETER project, which received funding from the European Union's Framework Programme for Research and Innovation, Horizon 2020, under Grant Agreement No. 812.790.

I would like to extend my thanks to Prof. Richard Pedriau, Dr. Mohsen Koohestani, Prof. Mohamed Ramdani, and Dr. Hugo Pues for their assistance during my secondments at ESEO and Melexis (Remote). Additionally, I am grateful to the PETER project coordinator Prof. Davy Pissoort and the Management Support Team for their continuous assistance in managing project responsibilities.

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Declaration

I declare that this thesis constitutes original work and is authored solely by me. It has not been previously submitted for any academic award at this university or any other institution. Proper acknowledgement of all sources used in this work has been made through references.

This thesis contains research presented in the following publications:

- A. H. Venkateshaiah, H. Xie, J. F. Dawson, A. C. Marvin, L. Dawson, and M. P. Robinson, "Coupling of Energy Into PCB Traces in a Reverberant Environment: Absorption Cross-section and Probability of Susceptibility," in *2020 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, 2020, pp. 1–6.
- H. Tang, A. H. Venkateshaiah, J. F. Dawson, A. C. Marvin, M. P. Robinson, and J. Ge, "Analysis and Estimation of Electromagnetic Energy Coupled into IC packages," *2021 Joint IEEE International Symposium on Electromagnetic Compatibility, Signal and Power Integrity, EMC Europe*, 2021.

The author of this thesis has also contributed to the following publications:

- A. C. Marvin, J. F. Dawson, H. Xie, L. Dawson, and A. Venkateshaiah, "An Experimental Study of the Variability of the Shielding Effectiveness of Circuit Board Shields," in *2020 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, 2020, pp. 1–5.

The author has also papers which are in submission process:

- A. H. Venkateshaiah, J. F. Dawson, M. Trefzer, H. Xie, S. Bale, A. C. Marvin, and M. P. Robinson, "Prediction of Probability of IC Failure and Validation of Stochastic EM-Fields Coupling into PCB Traces using a Purpose-Built RF IC Detector," in *IEEE Transactions on Electromagnetic Compatibility*.
- A. H. Venkateshaiah, J. F. Dawson, A. C. Marvin, M. Trefzer, S. Bale, and M. P. Robinson, "Influence of Stochastic Electromagnetic Field Coupling into PCB Traces and Integrated Circuit Package Pins using Power Balance Method," in *IEEE Transactions on Electromagnetic Compatibility*.
- A. H. Venkateshaiah, J. F. Dawson, M. Trefzer, S. Bale, A. C. Marvin, and M. P. Robinson, "Design and Application of RF IC Detector Capable of Measuring Coupled Power into IC's Package Pins via Test RF PCB Tracks," in *2024 14th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMC Compo), Torino, Italy*.

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Acronyms

AACS	Average Absorption Cross-Section
ACS	Absorption Cross-Section
ATCS	Average Transmission Cross-Section
CDF	Cumulative Distribution Function
CMRR	Common Mode Rejection Ratio
DPI	Direct Power Injection
DUT	Device Under Test
EM	Electromagnetic
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EUT	Equipment Under Test
GTEM	Giga-Hertz Transverse Electromagnetic
IA	Instrumentation Amplifier
IC	Integrated Circuits
LUF	Lowest Usable Frequency
MCX	Micro Coaxial Connector
PCB	Printed Circuit Boards
PD	Peak Detector
PDF	Probability Density Function
PGA	Programmable Gain Amplifier
PWB	Power Balance
RF	Radio Frequency
RF IC	Radio Frequency Integrated Circuit
RF PCB	Radio Frequency Printed Circuit Board
SE	Shielding Effectiveness
SMA	Sub Miniature version A
TCS	Transmission Cross-Section
TOSM	Through, Open, Short and Match
TRL	Through, Reflect and Line
TRL/M	Through, Reflect, and Line/Match
TRM	Through, Reflect and Match
UoY	University of York

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1. Introduction

The advancement of electronic component technology, marked by increasing performance and integration levels over recent decades, has been instrumental in propelling innovation across various industries. However, this progress in integration levels has rendered intricate electronic components highly susceptible to electromagnetic interference (EMI) emanating from external sources. Notably, printed circuit boards (PCBs), housing a myriad of complex integrated circuits (ICs), have become vulnerable to radiated EMI. Understanding and predicting the susceptibility of electronic components and evaluating the susceptibility of complex PCBs to enhance their shielding effectiveness (SE) against EMI are pressing concerns within the electromagnetic compatibility (EMC) community. Addressing these concerns is vital for ensuring the reliable operation and longevity of electronic systems in the face of escalating EMI challenges.

The previous work conducted at the University of York (UoY), as highlighted in [1], has introduced a risk assessment model suitable for predicting an upper bound on the probability of electronic device failure. Globally, other researchers have contributed significantly to this field: [2] presents a statistical method for predicting and quantifying the radiated susceptibility of electronic systems implemented on a PCB. It classifies and quantifies the system's hazard levels in harsh electromagnetic (EM) environments, estimating threshold levels based on system-level PCB information to gauge EM threat levels. Additionally, [3] explores the frequency-dependent EM susceptibility of custom digital ICs, highlighting an inverse relationship between IC immunity and modulating signal period alongside a direct correlation with electric field (E-field) amplitude and pulse width, ultimately linking the probability of IC susceptibility to the modulating signal and transmitted information. Radiated immunity testing of ICs above 1 GHz encounters challenges, like achieving high field strengths and managing Equipment Under Test (EUT) orientation effects, which current methods struggle to address, while [4] demonstrates that the reverberation chamber, offers a potential solution by overcoming these limitations in the higher frequency range.

The IC EMC standard BS EN 62132-4 [5] provides a framework for evaluating IC susceptibility by assessing the directly injected forward power required to induce IC malfunction. Hence, the power coupled or absorbed into the IC or any other electronic component plays a vital role in susceptibility prediction analysis.

The results presented in [6] highlight the significant role played by the loads on the PCB traces in the average absorption cross-section (AACS) of the PCB. In [7], research has been conducted to develop a numerical Monte Carlo method to estimate the average coupled power at the terminus of lossless PCB traces in a reverberant environment and to

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further explore the factors influencing the electromagnetic power absorbed by the loads of PCB traces.

In this thesis, we evaluate the probability of susceptibility of PCB components, such as ICs, by considering the coupled forward power at the package pin of the Device Under Test (DUT). We have expanded the model described in [7] by incorporating PCB track losses, enabling us to estimate the distribution of coupled forward power at the package pin for a given reverberant field. We can then use our knowledge of field statistics in a reverberant environment to predict the probability of IC failure in a reverberant environment. We also validate the Monte Carlo method to predict stochastic EM coupling into realistic loads such as IC pins via measurements of test PCB tracks. This validation is accomplished through the design and testing of an instrumented custom-designed radio frequency integrated circuit (RF IC) detector capable of measuring coupled power at its package pins. With a custom-designed IC, we have full knowledge of the internal chip and package details which better places us to understand the system behaviour as compared with commercial of the shelf detectors ICs.

At the UoY, research has been conducted to investigate the absorption cross-section (ACS) of printed circuit boards (PCBs) in stochastic or reverberant environments. Flintoft and Parker et al. [8], [9] conducted measurements of the AACS for various PCBs in a reverberation chamber spanning 2 to 20 GHz. These PCBs featured different component densities and surface shielding. The study revealed a reduction of 20% to 40% in the AACS of a PCB when placed in a stack compared to its isolated value. Furthermore, the research revealed that the AACS values obtained for modern Information and Communication Technology (ICT) PCBs in a reverberation chamber are directly applicable for power balance (PWB) analysis within the context of shielding in scenarios involving electrically large equipment enclosures. The power and the particular operating configuration of the DUT do not significantly impact the ACS [10].

Previous research, based on the PWB method [11], established that knowing the energy absorbed by the contents and average transmission cross-section (ATCS) of the shielded enclosures is crucial for determining both SE and internal fields. The measurement of ATCS and its use in predicting internal fields and SE of enclosures containing PCBs and other components have also been demonstrated [9], [12]. The PWB method developed by Hill and Juqua et al and described in [13] and [14], has demonstrated that the fields present within a shielded enclosure and the SE are influenced by both the transmission cross-section (TCS) of coupling apertures and the ACS of the contents inside the enclosure. This method offers straightforward solutions for reverberant enclosures, enabling efficient calculations of coupling and shielding without the need for computationally intensive full-wave solvers. By treating the fields as uniform and isotropic and employing average values for TCS and ACS [15], the PWB method significantly reduces computational effort.

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Building upon the prior research in [7], in this thesis we have conducted further exploration of absorbed power, particularly with respect to known loads on lossless PCB traces and energy coupling into IC packages in [16] and [17]. We also presented the relationship between the predicted power, AACS, and the PWB method for SE in [16].

The methodologies developed in [6–8] and the contributions of these results in determining the AACS of internal components within the enclosure are instrumental to develop the enhanced PWB method in this research work. It has been demonstrated in [6], [7], [16] that calculating the power absorbed by the loads on the PCB traces is essential for determining the AACS of the PCB trace and establishing its relationship with the PWB method, which aids in determining the power absorbed by the internal contents of the shielded enclosures. The power absorbed by the realistic loads such as ICs and PCB traces plays a significant role in the AACS of the PCB under test. Therefore, it is essential to study the influence of stochastic EM field coupling into IC pins and PCB traces in the PWB method for enclosures and their internal components. This enhanced PWB method will be capable of incorporating the AACS of the IC at package pins and connected PCB tracks, along with other relevant AACS for internal components within the enclosure.

Expanding on the foundation of existing PWB methods, in this thesis we introduced an enhanced PWB method. This method was refined by integrating the AACS information related to the IC at package pins and interconnected PCB tracks, encompassing other significant AACS pertaining to internal components housed within the enclosure. This detailed scrutiny of AACS, including those of critical components like PCB tracks and ICs on the DUT, represents a slight enhancement over the conventional PWB methods.

1.1 Research Scope

In addressing EMI concerns, a prevalent strategy is the rule-based approach, which follows predefined guidelines and standards during the design of electronic devices to minimize EMI issues. However, to ensure safety without compromising performance, it is essential to complement the rule-based approach with a risk-based approach. The risk-based approach involves assessing and managing EMI risks based on factors like device criticality and susceptibility, enabling customized actions to enhance safety and mitigate risks. Hence, the PETER consortium initiated a novel and robust risk-based approach in EMI management. This approach involved the collaboration of 15 early-stage researchers (ESRs) specializing in different topics related to the development of high-technology systems. The aim was to ensure reliability and safety throughout the entire life cycle of these systems, even in the face of severe and complex EMI threats. In this thesis, ESR9 (thesis author) presents one of the topics from this project.

The work presented in this thesis describes a design methodology for assessing the probability of susceptibility of ICs to EMI in a Reverberant Environment. Furthermore, the

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validation of the numerical model [7] capable of estimating EM fields coupling into the loads of the PCB traces, in other words, the validation of stochastic EM fields coupling into realistic loads such as ICs via test RF PCB tracks is also presented. This validation is achieved through the fabrication of a custom RF IC detector capable of measuring coupled forward power at the package pin through RF PCB tracks. With an understanding of the internal workings and packaging of the chip, which provides unique insights into the behaviour of the chip and internal floor planning, a level of scrutiny is often unattainable with commercially available proprietary designs. Through the dedicated RF IC detector, we developed an enhanced PWB method, incorporating critical AACS data concerning the IC at package pins and interconnected PCB tracks. This comprehensive consideration of AACS for crucial components like PCB tracks and package pins of the IC on the DUT represents an advancement over existing PWB methods.

The objective is to develop an advanced methodology for estimating the probability of susceptibility of ICs or a component on a PCB to EMI by statistically characterizing the power absorbed by electronic circuits and enhancing PWB methods for enclosures and internal components. The main aim of this research can be separated into smaller goals as listed below:

- Developing a methodology to measure and validate the estimation of radiated coupling at the package pins of the RF IC detector in a radiated environment for the estimation of the probability of susceptibility of ICs to EMI for electrically large systems.
- Designing an RF IC detector to measure the coupled forward power at package pins and via connected RF PCB tracks for validating the estimation of stochastic EM fields coupling into RF PCB tracks and IC package pins.
- Developing PWB method for enclosures and internal components (RF IC detector) and adapting existing IC immunity standards for system-level immunity risk assessment.

Overall, the thesis focuses on developing a comprehensive design approach in Chapter 8 to evaluate the EMI susceptibility of electronic circuits in electrically large systems, with the goal of enhancing the understanding and management of EMI risks.

1.2 Outline of the Thesis

The thesis opens with an introductory chapter providing an overview of the research work. This is followed by a brief exploration of EMC theory and fundamental concepts in Chapter 2. Following this, the thesis delves into the topic of SE and the PWB method, offering technical insights crucial for subsequent discussions. These foundational chapters lay the groundwork for a comprehensive understanding of the research discussed in the thesis.

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Chapter 4 focuses on the coupling of energy into PCB traces and IC packages. Leading to the publication of two research papers [16] and [17]. A detailed account of the design of the RF IC detector is presented in Chapter 5. In Chapter 6 the PCB test bench is designed for testing the operation and behaviour of the RF IC detector. Additionally, the design of test benches for conducting radiated measurements is discussed.

Chapter 7 introduces the analysis of impedance and conducted coupling into the package pins of the RF IC detector. This chapter includes an investigation of the realistic impedance at the package pins. Additionally, the calibration methodology of the RF IC detector through calibration curves is presented.

Chapter 8 discusses the prediction of the probability of susceptibility of ICs to EMI and validates the numerical model, specifically focusing on the stochastic EM fields coupling into realistic loads such as ICs via test RF PCB tracks. This validation is achieved by conducting radiated measurements to determine the average coupled forward power at the package pin of the RF IC detector in the reverberation chamber. Furthermore, Chapter 9 discusses the influence of stochastic EM fields coupling into IC package pins and PCB traces in the PWB method, which illustrates the power flow between the test bench shielding enclosure and the reverberation chamber.

Finally, the concluding chapter summarizes the research work and outlines potential directions for future investigations. Additionally, an appendix is included to cover supplementary topics supporting a comprehensive understanding of the thesis.

1.3 Contributions of the Thesis

1.3.1 Novel Methodologies

In Section 8.1, we expanded the scope of the numerical model introduced in [7] to include PCB losses. Additionally, in Chapter 4, we delved into a more in-depth exploration of absorbed power, specifically addressing known loads on lossless PCB traces and energy coupling into IC packages [16] and [17]. Furthermore, an analytical methodology was developed in Section 8.2 to predict the probability of susceptibility of PCB components, such as ICs, to EMI. This methodology takes into account the coupled forward power at the package pin of the DUT. In Chapter 9, we investigated the influence of stochastic EM fields coupling into PCB traces and IC package pins using the PWB method. This method incorporates critical AACS data related to the IC at package pins and interconnected PCB tracks.

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1.3.2 Technical Contribution

An instrumented custom-designed RF IC detector, capable of measuring coupled power at its package pins, was developed in Chapter 5. This was designed to validate the updated numerical model predicting stochastic EM coupling into realistic loads, such as IC pins, through measurements of test PCB tracks, as discussed in Chapter 8.

In Chapter 6, we designed PCB test benches for the RF IC detector to accommodate various measurement scenarios, encompassing conducted measurements, radiated measurements in reverberant environments, and radiated measurements in GTEM environments. Additionally, a Through Reflect Line/Match (TRL/M) calibration was implemented to mitigate the impact of PCB traces on the RF IC detector test bench connected to the RF IC. This calibration enhances the accuracy of S-parameter measurements at the package pins, facilitating precise power analysis for both incoming and reflected signals.

1.3.3 Contribution to the Body of Knowledge

This work bridged the gap between theoretical insights and practical applications by establishing a correlation between practical applications and prediction models (Numerical and Analytical Models from Chapter 8) in Section 8.5. Notably, our discovery in Section 9.1.6 revealed that the dominant power coupling arises from PCB tracks, rendering the coupling from RF IC package pins and the IC itself negligible. This underscores the importance of shielding PCB tracks, as discussed in Section 9.1.6, as solely shielding the IC leaves the component vulnerable to EMI.

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2. Theory of EMC and Fundamentals

In this chapter, we discuss the fundamental theories and concepts that underpin the scope of this research work. Our exploration commences with a discussion on the historical evolution and theoretical foundations of EMC. This historical context provides insights into the development and significance of EMC in the realm of electronic systems and devices. Moving forward, we explore the domain of EMC at the IC level, acknowledging its distinct challenges and implications. We delve into the intricacies of EM Reverberation Chambers, elucidating their pivotal role in generating controlled and uniform EM fields for accurate measurement and testing. Furthermore, our exploration extends to the realm of EM/RF shielding, where we uncover its crucial role in safeguarding electronic components from the impact of external EM fields.

2.1 A Brief History of EMC

The history of EMC traces back to the early 20th century, coinciding with the rapid advancements in electronics and telecommunications technologies. As the use of radio and electrical equipment increased, engineers and scientists began noticing unwanted interference and compatibility issues among different devices and systems, prompting the need to comprehend and manage EMI.

Over the years, as electronic devices became ubiquitous across various industries, the significance of EMC significantly grew. Governments and regulatory bodies responded by establishing EMC standards to ensure that electronic products could coexist without causing interference and function reliably even in the presence of EM fields.

Today, EMC plays a critical role in the design, testing, and certification processes of electronic products. It involves a range of techniques, such as shielding, filtering, and proper grounding, aimed at mitigating EMI and maintaining seamless compatibility among different electronic systems.

2.2 EMC

The theory of EMC centres around its definition from [18], which states that EMC refers to the ability of an electronic system to function properly in its intended EM environment and not be a source of pollution to the EM environment. Key aspects of EMC involve understanding EMI, EM Susceptibility (EMS), and Emission, as well as exploring various coupling mechanisms such as capacitive, inductive, and radiative coupling, which facilitate the transfer of EM energy between components and systems.

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EM immunity (or EMS), refers to a device or ability of the system to withstand and function correctly in the presence of EM disturbances. Immunity testing involves subjecting the device to various EM fields at different frequencies and amplitudes to evaluate its robustness against interference. The goal is to ensure that the device can operate reliably without malfunctioning or being adversely affected by external EM influences.

Another crucial aspect is EMC emission control, which aims to limit the unintentional generation and propagation of EM signals from electronic devices. During operation, electronic devices emit EM radiation, commonly in the form of conducted and radiated emissions. EMC emission standards set limits on the amount of EM radiation a device can emit to prevent interference with other nearby devices. To comply with regulatory emission standards, effective filtering, shielding, and grounding techniques are implemented to suppress emission levels.

A significant focus of EMC practice is to develop effective mitigation strategies to address EMI, EMS, and Emission issues. These strategies include employing shielding, which isolates electronic components from external EM fields using conductive materials, and grounding, which provides a low-impedance path for electrical currents to reduce interference and ensure safety. Additionally, filtering techniques are explored to suppress unwanted EM signals and noise from power lines or signal lines, thus maintaining signal integrity and reducing interference. To address EMC emission issues, techniques such as reducing signal harmonics, using proper PCB layout and decoupling, and employing EMI filters can be used. Proper PCB layout practices, such as keeping signal traces short and minimizing loop areas, help reduce emission levels. Decoupling capacitors placed close to active components can also help suppress high-frequency noise. Additionally, EMI filters can be used to reduce conducted emissions on power and signal lines, thereby ensuring compliance with regulatory emission standards.

By incorporating these additional measures, electronic devices can meet EMC emission and immunity standards and prevent interference with other nearby devices. This comprehensive approach to EMC theory ensures that electronic systems and devices operate efficiently and reliably in their EM environments, fostering compatibility and minimizing potential EM disturbances.

2.3 The EMC of Integrated Circuits

During the 1970s, researchers began directing their focus towards IC EMC. Over the past five decades, concerns regarding EMC have escalated significantly. In comparison to system-level circuit models, ICs exhibit greater susceptibility to EMI at higher frequencies. As the drive for enhanced IC performance persists, the significance of achieving both low emissions and high immunity to EMI has become a paramount consideration.

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Technological advancements, including progress in process integration, higher switching speeds, and more intricate IC designs, have led to increased emissions from ICs. Specifically, the increasing switching speeds and expanded bandwidth render ICs susceptible to a broader spectrum of frequencies and sources. Simultaneously, a decline in IC immunity to EMI has been observed due to reduced supply voltage and a higher number of interfaces. Consequently, EMC has emerged as a pivotal factor contributing to IC failures and necessitating redesigns [19], [20]. This underscores the urgent need for robust EMC practices in IC design. These scenarios have prompted researchers to focus more on design methodologies and dedicate their expertise to emission reduction and immunity enhancement over the past few decades.

A comprehensive review of research conducted in the realm of EMC at the IC level over the past few decades is presented in [20]. This body of research offers invaluable insights into the challenges and advancements pertaining to managing EMC concerns within ICs. It illuminates the evolution of strategies aimed at achieving optimal EMC performance while adapting to the dynamic and ever-changing technological landscape.

2.4 EM Reverberation Chambers

In this research work, the reverberation chamber is extensively used for radiated measurements, aiming to comprehend EM coupling to PCB tracks and IC packages and to understand the power flow between the shielding enclosure and the reverberant environment. This approach aids in validating the stochastic EM fields coupling into realistic loads, such as ICs connected to test RF PCB tracks and developing an enhanced PWB method. Figure 1 shows the pictures of the reverberation chamber at the University of York.

Figure 1: Shows the pictures of the Reverberation Chamber at the University of York.

An EM reverberation chamber is an electrically large and highly conductive enclosure utilized for conducting both emission and immunity measurements on an electronic DUT.

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It serves as a controlled environment to generate statistically uniform EM fields, achieved through mechanisms such as mechanical or frequency stirring. These chambers play a pivotal role in EM field measurement and testing, often being referred to as mode-stirred chambers.

In the context of mode stirring or tuning, the reverberation chamber employs techniques such as rotating paddles or other geometric alterations within the chamber. This process facilitates the modification of the geometry of the chamber, ultimately leading to the achievement of uniform fields. The chamber is a closed cavity which generates numerous propagation modes, which give rise to intricate three-dimensional standing wave patterns characterized by a multitude of resonant modes. This phenomenon results in regions where the EM field is of significant magnitude, as well as regions where it is minimal.

The role of the mode stirrer is pivotal within this setup. By modifying the boundary conditions of the chamber, the mode stirrer effectively shifts the positions of the maxima and minima of the field magnitudes. Consequently, the energy distribution within the chamber is stirred, prompting alterations in the field pattern. This stirring process and averaging over many stirrer positions results in the creation of uniform EM fields throughout the chamber, ensuring that the energy levels in all field components remain consistent from all directions. Reference [21] provides further insights into the functioning and significance of the EM reverberation chamber, elucidating its role in generating controlled and uniform EM fields essential for accurate measurement and testing.

2.5 EM/RF Shielding

EM/RF shielding safeguards electronic components from the influence of external EM fields and also safeguards external electronic components from internal emissions. This is achieved through the utilization of conductive materials that act as barriers, preventing unwanted EM radiation from penetrating and affecting sensitive components. The shielding serves as a protective enclosure, effectively isolating the internal electronic circuitry from potentially disruptive external EM sources. Grounding in EM/RF shielding creates a low-impedance path for currents, reducing interference from external EM fields and safeguarding sensitive components by redirecting stray currents.

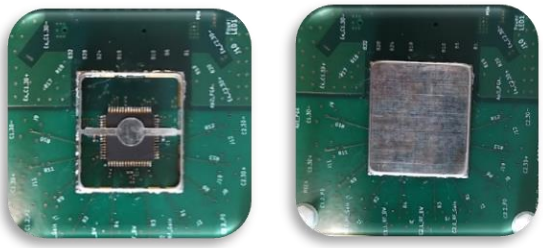

Figure 2: Shows the pictures of shielding an IC mounted on a PCB board.

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The integration of shielding techniques within an electronic system results in several advantages. Firstly, it shields external components from emissions generated by internal components within the enclosure, effectively reducing EM emissions from enclosed components. This containment prevents unwanted EM signals from interfering with nearby electronic devices, thereby minimizing overall EMI in the vicinity. Secondly, shielding also protects internal components from external EMI, bolstering the immunity of the internal components against such interference. Ultimately, EM/RF shielding is crucial for ensuring the performance, reliability, and EMC compliance of modern electronic devices.

In this research work, we utilize EM/RF shielding to understand the power flow between the interior and exterior of the shielding, prompted by alterations in power density. This approach facilitates the development of an enhanced PWB method, yielding invaluable insights into the intricate interplay between EM fields and shielding mechanisms. Figure 2 shows the pictures of shielding an IC mounted on a PCB board.

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3. Shielding Effectiveness and the Power Balance Method

In this chapter, we discuss the definitions of SE for enclosures and the PWB method within a reverberant environment. This discussion encompasses considerations regarding the impact of enclosure content and the absorbed energy into components on SE. It has been demonstrated in [6], [7], [16] that calculating the power absorbed by the loads on PCB traces is crucial. This calculation is fundamental for determining the AACS of the PCB trace and establishing its relationship with the PWB method. This relationship, in turn, aids in determining the power absorbed by the internal contents of shielded enclosures. The power absorbed by realistic loads, such as ICs on the PCB traces, significantly influences the AACS of the tested PCB. Consequently, understanding SE and developing enhanced PWB methods for enclosures and their internal components is essential. These methods should be adept at incorporating AACS values for ICs at package pins and connected PCB tracks, along with other relevant AACS for internal components within the enclosure. Therefore, in this chapter, we discuss the two pivotal aspects of EMC: the definition of SE and the PWB method. Additionally, we engage in a comprehensive discussion on Reverberant Environments, further enriching our exploration of EMC.

The evaluation of enclosure SE traditionally occurs within empty enclosures. However, a comprehensive assessment necessitates the inclusion of factors such as the enclosure's contents, wall losses, and the impact of loading. Recent proposals emphasize the incorporation of loading effects during shielding measurements to enhance the relevance of SE metrics [6], [22], [23].

Introducing an efficient approach for estimating the average EM field within electrically large enclosures, we explore the PWB analysis method. This method is detailed in references [24], [25], with its systematic application to enclosure shielding discussed in [8].

As we navigate through these concepts, we lay the groundwork for a deeper understanding of how SE and the PWB method contribute to the realm of EMC. This knowledge serves as a foundation for our subsequent exploration and application in the context of our research objectives.

3.1 Shielding Effectiveness

The effectiveness of shielding becomes clear when we understand the power flow dynamics between the enclosure and the external reverberant environment, alongside the knowledge of power density both inside and outside the enclosure. This comprehension of power flow dynamics, coupled with the understanding of ATCS and AACS, will also contribute to defining the PWB method at the end of this chapter. However, this section focuses on defining SE.

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There exist various definitions for the SE of an enclosure. In accordance with IEEE 299 [26], SE can be expressed in terms of received power, as shown below:

$$\mathrm{SE} = \frac{P_o}{P_s} \tag{1}$$

here, P_o represents the power received by the receiving antenna in the absence of an enclosure, while P_s signifies the power received by the receiving antenna when located within an enclosure. An alternative definition from [15], which articulates SE in terms of power densities:

$$\mathrm{SE} = \frac{S_o}{S_s} \tag{2}$$

In this context, S_o denotes the power density either without an enclosure or the power density incident upon the enclosure. On the other hand, S_s corresponds to the power density within the enclosure. The power density exhibits direct proportionality to the square of the total E-field, as defined by equation [13]:

$$S = \frac{{E_0}^2}{\eta_0} \tag{3}$$

In this equation, E_0 signifies the total E-field (defined in Section 3.2.4), while η_0 represents the intrinsic impedance of free space.

3.1.1 Stirred Shielding Effectiveness

In this work, the radiated measurements aimed at calculating the SE are conducted within a reverberation chamber. Although, ideally, the direct components within the reverberation chamber should be zero, in reality, we often observe some direct components during the measurement. However, our interest lies solely in the stirred components within the measurement. Therefore, it is imperative to calculate the stirred SE by considering the properly stirred components.

The definition of stirred SE, as outlined in [27], revolves around the ratio of stirred coupling existing between the source and the internal components being tested within the shielding. This is achieved by subtracting the direct component from the overall coupling between the source and the interior of the shield. This subtraction effectively isolates the reverberant coupling, providing a clear representation of the stirred coupling phenomenon.

$$SE_{st} = \frac{\langle |S_{21u} - \langle S_{21u} \rangle|^2 \rangle}{\langle |S_{21s} - \langle S_{21s} \rangle|^2 \rangle} \tag{4}$$

The stirred SE signifies the coupling between the source and the components being tested inside the shielding, excluding the direct coupling.

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3.2 Reverberant Environments

In a real-world setting, victim electronic components can receive EMI signals from multiple directions and polarizations simultaneously, originating from a single external interference source. In the context of a reverberant environment, these signals interact and reflect off surfaces, resulting in a multitude of signal paths with different characteristics. The "reverberant case" refers to considering all these diverse possibilities and variations in the signals, providing a comprehensive understanding of how the signals behave and interact within the environment. Hence, this is the reason to focus on reverberant environments in this research work.

The reverberant environment, a controlled setting, can be generated using a Reverberation Chamber, as elaborated in Section 2.4. A Reverberation Chamber, an enclosed cavity for EM measurements (emission and immunity tests), generates complex standing wave patterns due to its closed nature. By employing a stirrer within the chamber, the boundary conditions of the chamber can be altered, ultimately leading to the establishment of uniform fields. Once this uniformity is achieved, the environment is termed a reverberant environment.

Several studies have explored the field distribution to create a reverberant environment. Hill [21], for instance, demonstrates that in such an environment, the real and imaginary components of the field are distributed with a mean of zero, when samples are taken over various stirrer positions.

3.2.1 Resonances

The resonant modal frequencies of a rectangular cavity, such as a reverberation chamber, are mathematically defined as follows:

$$f_{mnp} = \frac{c_0}{2}\sqrt{\left(\frac{m}{a}\right)^2 + \left(\frac{n}{b}\right)^2 \left(\frac{p}{c}\right)^2} \tag{5}$$

In this equation, m, n and p are integers, with only one of them being zero. c_0 represents the propagation velocity in the reverberation chamber (equivalent to free-space), and a, b and c are the dimensions of the enclosure in meters.

Weyl's law, as presented in [21], provides an approximate analytical solution for calculating the number of resonant modes below a given frequency (f), for all types of cavities. For rectangular cavities like the reverberation chamber, a more precise version of this law is available, as shown in the equation given below [21]:

$$N_{modes} = \frac{8\pi f^3 abc}{3{c_0}^3} - \frac{(a+b+c)f}{c_0} + \frac{1}{2} \tag{6}$$

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3.2.2 Reverberation Chamber at UoY

The reverberation chamber at the UoY has dimensions of 4.7m x 3.0m x 2.37m. As shown in Figure 3, a metallic stirrer, connected to a motor, is employed to uniformly distribute energy throughout the chamber. The lowest usable frequency (LUF) of this chamber stands at approximately 180 MHz. LUF determination follows multiple methods: one involves identifying the first resonant frequency via equation (5), resulting in 59.31 MHz, then multiplied by three as per the BS EN 61000-4 standard [28]. Another approach involves the rule of thumb, where the chamber can be considered reverberant at frequencies above 60^{th} mode, we can calculate the number of modes with respect to frequency inside the chamber using equation (6).

Notably, the wall of the chamber accommodates bulkhead connections, allowing external test equipment to be seamlessly connected. For the DUT or EUT, placement within the chamber's working volume is essential. The working volume, the region within the reverberation chamber that exhibits a statistically uniform EM field, commences approximately from a quarter wavelength of the chamber walls. It is important to note that areas closer to the chamber walls may experience diminished EM field uniformity due to boundary effects [28].

BS EN 61000-4-21 [28] is a key standard guiding testing and measurement techniques in reverberation chambers, serving as a comprehensive reference in this domain.

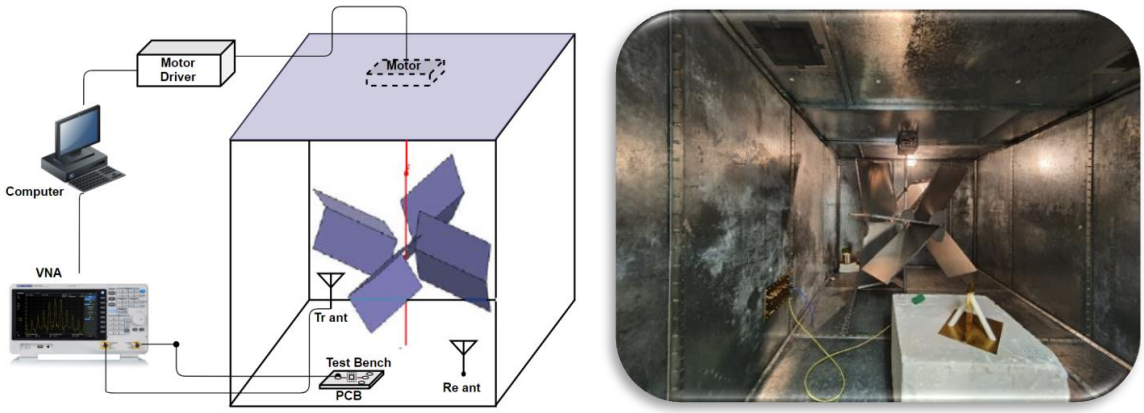

Figure 3: Shows the Reverberation Chamber at the University of York.

3.2.3 Stirring

The majority of reverberation chambers utilize a mechanical paddle for field stirring. Two methods fall under mechanical stirring: mode-tuned operation and stirred mode testing.

In mode-tuned operation, measurements are conducted for various stirrer positions, where each position undergoes a frequency sweep. The measurements obtained for each frequency are then averaged over the n stirrer positions. On the other hand, stirred mode

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testing involves continuous rotation of the stirrer while multiple measurements are taken. The results are subsequently averaged over the different stirrer positions for each frequency.

Throughout this research, mechanical stirring is employed, specifically using the mode-tuned operation method. While the second method might offer faster measurements for each instance, the first method stands out for its superior measurement repeatability accuracy. In this work, the mechanical stirrer shown in Figure 3 is used to facilitate the measurements.

3.2.4 Field Distribution

In a reverberant environment, Hill [21] demonstrated that waves are expected to impact a point in space uniformly from all directions and with all polarizations. When considering samples taken across a number of stirrer positions, the rectangular field components of a sinusoidal waveform exhibit real and imaginary components that follow a normal distribution with a mean of zero. The mean square values of the rectangular components of the E-field can be expressed as:

$$\langle |E_x|^2 \rangle = \langle |E_y|^2 \rangle = \langle |E_z|^2 \rangle = \frac{{E_o}^2}{3} = 2\sigma^2 \tag{7}$$

here, ${E_o}^2$ represents the mean squared value of the total E-field, while σ signifies the standard deviation of the sample set of E-field components. The variance (σ^2) of the real and imaginary parts, equal to half of one-third of the total energy from the equation above, is given by Hill [21] as:

$$\begin{aligned} \langle |E_{xr}|^2 \rangle = \langle |E_{xi}|^2 \rangle = \langle |E_{yr}|^2 \rangle = \langle |E_{yi}|^2 \rangle = \langle |E_{zr}|^2 \rangle = \langle |E_{zi}|^2 \rangle \\ = \frac{{E_o}^2}{6} = \sigma^2 \end{aligned} \tag{8}$$

Subscripts r and i indicate real and imaginary parts, respectively. It is noteworthy that the total energy in the field is evenly divided among all E-field components, resulting in a division factor of 6. The probability density function (PDF) for each E-field component can be represented as:

$$p(E_{ab}) = \frac{1}{\sigma\sqrt{2\pi}} e^{\frac{1}{2}\left(\frac{E_{ab}}{\sigma}\right)^2} \tag{9}$$

In this equation, 'a' denotes the direction (x, y, z), and b represents the real (r) or imaginary (i) components.

3.2.5 Q Factor

The Q-factor, denoted as Q, represents the ratio of the steady-state energy stored within the reverberation chamber to the energy dissipated per cycle of the chamber's resonant frequency [24]:

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$$Q = \frac{\omega U_s}{P_d} \tag{10}$$

where ω is the angular frequency of excitation, $U_s = WV$ signifies the steady-state energy in the chamber, with $W = \epsilon_0 {E_0}^2$ representing the energy density, V being the cavity volume, and P_d representing the dissipated power.

The power density within the reverberation chamber can be expressed as:

$$S_0 = \frac{{E_0}^2}{\eta_0} = c_0 W \tag{11}$$

where $\eta_0 = \sqrt{\mu_0/\epsilon_0}$, $c_0 = \sqrt{1/\mu_0\epsilon_0}$, μ_0 and ϵ_0 signifies the magnetic permeability and the absolute permittivity of free space.

By utilizing equations (10) and (11), we can deduce the power density S_0 within the reverberation chamber:

$$S_0 = \frac{Q\lambda}{2\pi V} P_d \tag{12}$$

here, λ represents the free space wavelength.

Assuming a rectangular cavity with a circular aperture, under steady-state conditions, the power transmitted (P_t) through the aperture is equal to the power dissipated (P_d). This allows us to express the Q-factor equation in terms of received power (P_r) and transmitted power (P_t), as demonstrated below [24]:

$$Q = \frac{16\pi^2 V}{\lambda^3}\frac{P_r}{P_t} = \frac{16\pi^2 V}{\lambda^3}\frac{\langle P_r\rangle}{\langle P_t\rangle} \tag{13}$$

Similarly, for the reverberation chamber, we can represent the ratio of the average received power $\langle P_r\rangle$ and average transmitted power $\langle P_t\rangle$ from the antennas inside the chamber in terms of S-parameters as follows:

$$Q = \frac{16\pi^2 V}{\lambda^3}\frac{\langle |S_{21}|^2\rangle}{(1-|\langle S_{11}\rangle|^2)(1-|\langle S_{22}\rangle|^2)\eta_1\eta_2} \tag{14}$$

where $|\langle S_{11}\rangle|$ is the magnitude of the average reflection coefficient of the transmitting antenna, S_{21} is the transmission coefficient between the transmitting and receiving antennas, $|\langle S_{22}\rangle|$ is the magnitude of the average reflection coefficient of the receiving antenna, η_1 and η_2 represent the antenna efficiency of the transmitting and receiving antennas, respectively.

To focus solely on the scattered component, we can eliminate any direct component $(|\langle S_{21}\rangle|)$ from the computation by subtracting it from S_{21} before calculating the average magnitude:

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$$Q = \frac{16\pi^2 V}{\lambda^3} \frac{\langle |S_{21} - \langle S_{21} \rangle|^2 \rangle}{(1 - |\langle S_{11} \rangle|^2)(1 - |\langle S_{22} \rangle|^2)\eta_1 \eta_2} \tag{15}$$

3.2.6 Chamber Energy Density and Received Power

In this section, we will explore an alternative approach for evaluating the energy density of the reverberation chamber, without relying on the Q-factor, by treating the reverberation chamber as a three-port system. The methodology presented in this section has also been detailed in our published work [16].

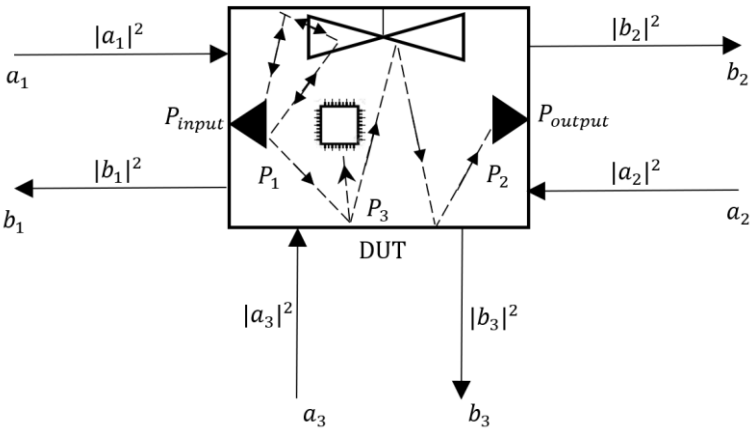

Figure 4: Shows the power flow in the reverberation chamber.

Figure 4 shows the power flow interaction between two antennas linked via a reverberation chamber. It showcases typical scenarios such as backscattered and reciprocal rays for antenna 1, as well as a ray propagating from antenna 1 to antenna 2, accompanied by the absorption of energy within the chamber's contents. Through the measurement of S-parameters between the two antennas positioned within the chamber, with the DUT present, and by terminating the unused port from the DUT with 50Ω loads, the chamber's energy density for an arbitrary forward power can be determined. In the figure, Port 3 represents the port connected to the DUT, with the forward (towards DUT) and reverse (from DUT) powers denoted as $|a_3|^2$ and $|b_3|^2$ respectively.

Utilizing the S-parameter notation, the forward power directed towards the left-hand antenna 1 is represented as $|a_1|^2$, while the reverse power is $|b_1|^2$. Similarly, at the right-hand antenna 2, the forward (towards the antenna) and reverse (from the antenna) powers are given by $|a_2|^2$ and $|b_2|^2$ respectively. The average power entering the chamber over a series of stirrer positions is then calculated as follows:

$$\begin{aligned} \langle P_1 \rangle &= (\langle |a_1|^2 \rangle - |\langle b_1 \rangle|^2)\eta_1 \\ &= \langle |a_1|^2 \rangle (1 - |\langle S_{11} \rangle|^2)\eta_1 \end{aligned} \tag{16}$$

here, η_1 represents the radiation efficiency of the antenna, and $\langle S_{11} \rangle$ stands for the mean value of the measured antenna reflection coefficient, which is equivalent to the antenna's

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free-space reflection coefficient [29]. Similarly, in the case of the receiving antenna, the power delivered to its load is diminished by both its radiation efficiency (η_2) and any mismatch to its load. This mismatch, measured in magnitude, aligns with the antenna reflection coefficient (S_{22}). Consequently, the average power $\langle|b_2|^2\rangle$ corresponds to the power emanating from antenna 2 but diminished by the combined effect of mismatch and antenna efficiency:

$$\langle|b_2|^2\rangle = \langle P_2\rangle(1-|\langle S_{22}\rangle|^2)\eta_2 \tag{17}$$

Now from the received power, averaged over a number of stirrer positions, $\langle P_2\rangle$, we can deduce the chamber total field:

$$E_0^2 = \frac{8\pi\eta_0\langle P_2\rangle}{\lambda^2} \tag{18}$$

where η_0 is the characteristic impedance of free space and λ is the free-space wavelength. Similarly, the power density in the chamber is:

$$S_0 = \frac{E_0^2}{\eta_0} = \frac{8\pi\langle P_2\rangle}{\lambda^2} \tag{19}$$

From equation (16) and (17), we can write the P_2 in terms of the S-parameters and P_1 as shown below,

$$\begin{aligned}\langle P_2\rangle &= \frac{\langle|S_{21}|^2\rangle}{(1-|\langle S_{11}\rangle|^2)\eta_1(1-|\langle S_{22}\rangle|^2)\eta_2}\langle P_1\rangle \\ &= G\langle P_1\rangle\end{aligned} \tag{20}$$

as $b_2/a_1 = S_{21}$ by definition, and G is the mean net transfer function of the chamber [30].

As our interest lies solely in the scattered component, we can eliminate any direct component ($|\langle S_{21}\rangle|$) from the calculation by subtracting it from S_{21} before proceeding to compute the average magnitude.

$$\begin{aligned}\langle P_2\rangle &= \frac{\langle|S_{21}-\langle S_{21}\rangle|^2\rangle}{(1-|\langle S_{11}\rangle|^2)(1-|\langle S_{22}\rangle|^2)\eta_1\eta_2}\langle P_1\rangle \\ &= G'\langle P_1\rangle\end{aligned} \tag{21}$$

where G' is a modified mean net transfer function. The energy density (19) in the chamber can be written as:

$$\begin{aligned}S_0 &= \frac{8\pi}{\lambda^2}G'\langle P_1\rangle \\ &= K\langle P_1\rangle\end{aligned} \tag{22}$$

where we can consider K as a calibration factor for this specific arrangement. This factor is utilized in Section 4.1.4.

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3.3 Power Balance Method

The PWB method delineates the power flow dynamics between the internal and external components of the shielding enclosure under a reverberant environment. Additionally, it is essential to grasp the significance of the SE of the enclosure, the ACS of the internal components, and the TCS of the apertures in the enclosure.

The technique of PWB analysis serves as a means to estimate EM power distribution and energy within an enclosure or a system of interconnected enclosures [11]. Illustrated in Figure 4, the diagram presents the power flow dynamics within such an enclosure. The magnitude of power traversing an aperture is reliant solely on the power density present on both sides of the aperture and its corresponding TCS.

$$\langle P_{10} \rangle = S_0 \langle \sigma^t \rangle \text{ and } \langle P_{01} \rangle = S_1 \langle \sigma^t \rangle \tag{23}$$

here, $\langle \sigma^t \rangle = \langle \sigma_{10}^t \rangle = \langle \sigma_{01}^t \rangle$ within the context of the reverberant scenario [15]. This value represents the TCS of the enclosure, averaged across all angles of incidence and polarization. The power absorbed by an object, like the enclosure's contents in [15], depends on its AACS ($\langle \sigma^a \rangle$) and the incoming power density.

$$\langle P_a \rangle = S_1 \langle \sigma^a \rangle \tag{24}$$

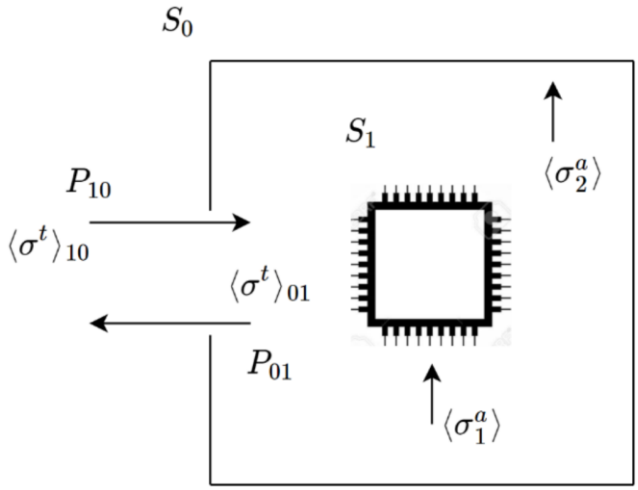

Figure 5: Shows the power flow in an enclosure.

PWB analysis is a method for estimating the average EM field within electrically large enclosures. A comprehensive elucidation of this method and its systematic application to enclosure shielding is provided in references [8], [24], [25]. The PWB analysis demonstrates that the ACS of PCB traces, IC, and other components within a test setup can be averaged across various angles of incidence and polarizations of the plane wave. This parameter reflects the intrinsic characteristics of the components within an enclosure, crucial for determining the loading effect on the enclosure. Additionally, it elucidates the perturbation in SE attributed to the internal contents of the enclosure.

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In Figure 5, one can assume uniform and isotropic power density in the reverberant case. Here, equal energy propagates in all directions with each polarization. The power balance in a steady state reverberant environment requires,

$$\langle P_{10} \rangle = \langle P_{01} \rangle + \langle P_a \rangle \tag{25}$$

Equations (23), (24) and (25) provide further insight:

$$S_0 \langle \sigma^t \rangle = S_1 \langle \sigma^t \rangle + S_1 \langle \sigma^a \rangle$$
$$\mathrm{SE} = \frac{S_0}{S_1} = \frac{\langle \sigma^t \rangle + \langle \sigma^a \rangle}{\langle \sigma^t \rangle} \tag{26}$$

3.3.1 Absorption Cross-Section

The ACS serves as a metric quantifying the power absorption from an incident field. It characterizes the amount of power absorbed by an electronic component from a plane EM wave. For a linearly polarized plane wave with a power density (S_0) incident at spherical polar angles (θ, ϕ) from random directions within the rectangular cavity, the ACS of the enclosed contents is defined as follows:

$$\sigma^a(\theta, \phi) = {P_a}/{S_0} = {P_a \eta_0}/{E_0^2} \tag{27}$$

where P_a represents the total power absorbed by the contents inside the cavity.

Within a reverberation chamber, it is possible to establish a uniform EM field environment, termed as a reverberant environment. In this environment, the DUT is subject to simultaneous random reflections and EM waves arriving from various directions and with differing polarizations. From this multitude of interactions, the ACS is averaged across all incidence directions and polarizations. This resultant parameter is known as the AACS, and it is defined as follows:

$$\langle \sigma^a \rangle = \frac{1}{8\pi} \oiint_{4\pi} \left(\sigma_{TE}^a(\theta, \phi) + \sigma_{TM}^a(\theta, \phi) \right) d\Omega \tag{28}$$

where the polarization average is computed across transverse electric (TE) and transverse magnetic (TM) modes, relative to the plane of incidence [31].

The total AACS can be expressed in terms of the Q-factor of the chamber using equations (12) and (27), as presented below.

$$\langle \sigma^a \rangle_{tot} = \frac{2\pi V}{Q\lambda} \tag{29}$$

From reference [21], we can establish the relationship between the average received power $\langle P_r \rangle$ and the power density S_0 as shown below:

$$S_0 = \frac{8\pi}{\lambda^2} \langle P_r \rangle \tag{30}$$

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Furthermore, equation (27) can be expressed in terms of the average transmitted power $\langle P_t \rangle$ inside the chamber, which is also the average absorbed power by all the components within the chamber, including the antenna, walls, internal components, and so on, as shown below:

$$\langle \sigma^a \rangle_{tot} = {}^{\langle P_t \rangle}/_{S_0} \tag{31}$$

Combining equations (30) and (31), we can express the total AACS as follows:

$$\begin{gathered} \langle \sigma^a \rangle_{tot} = \frac{\lambda^2}{8\pi} \frac{\langle P_t \rangle}{\langle P_r \rangle} = \frac{\lambda^2}{8\pi} \frac{1}{G} \\ G = \frac{\langle |S_{21} - \langle S_{21} \rangle|^2 \rangle}{(1 - |\langle S_{11} \rangle|^2)(1 - |\langle S_{22} \rangle|^2)\eta_1 \eta_2} \end{gathered} \tag{32}$$

To calculate the AACS of an object or component, we can utilize the following equation:

$$\begin{gathered} \langle \sigma^a \rangle_{object} = \langle \sigma^a \rangle_{with\ object} - \langle \sigma^a \rangle_{without\ object} \\ \langle \sigma^a \rangle_{object} = \frac{\lambda^2}{8\pi} \frac{1}{G_{with}} - \frac{\lambda^2}{8\pi} \frac{1}{G_{without}} = \frac{\lambda^2}{8\pi} \left(\frac{1}{G_{with}} - \frac{1}{G_{without}} \right) \end{gathered} \tag{33}$$

3.3.2 Transmission Cross-Section

The TCS represents an effective method for characterizing the SE of an aperture [15], [32]. The aperture's TCS is formulated as follows:

$$\sigma^t(\theta, \phi) = {}^{P_t}/_{S_i} \tag{34}$$

here, P_t denotes the total power transmitted through the aperture, while S_i signifies the power density of the incident field. A comprehensive elucidation of power flow and power density is provided in Section 3.3.

Analysing the TCS of apertures holds paramount significance for the assessment of shielding structures and the refinement of an advanced PWB method. We can write equation (34) in terms of total AACS and SE as shown below from [15].

$$\langle \sigma^t \rangle = \frac{\langle \sigma^a \rangle_{tot}}{SE - 1} \tag{35}$$

In Chapters 2 and 3, we have addressed all the fundamental topics crucial for a comprehensive understanding of the research work presented in this thesis. By delving into these foundational concepts, we lay a robust groundwork for the subsequent chapters, where we effectively apply these principles within the specific context of our research objectives.

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4. Coupling of Energy into PCB traces and IC packages

4.1 Coupling of Energy into PCB traces

In this chapter, we consider energy coupling into PCB traces and IC packages with known loads, validating the numerical model for lossless PCB traces outlined in [7]. The coupling of EM waves to transmission lines (TLs) has been widely studied [33–35], both in the case of a single plane wave and more recently in the context of a reverberant field [36–38]. In [7], they expand on these concepts by comparing various methods to compute the energy absorbed by PCB load tracks and their contribution to the PCB AACS.

Knowing the SE of an enclosure allows us to predict the internal fields, given the external fields. By knowing the AACS of an individual track connected to a load ($\langle\sigma^a\rangle$), we can then predict the energy absorbed into the terminals (P_a) of components attached to the track. This will allow us to discuss the correlation between the PWB method, SE and the calculated AACS in this chapter. The topics from this chapter have been documented in published research papers [16] and [17]. In the following sections, we will provide a brief review of the methods described in [7] before comparing them with newly measured data.

4.1.1 Numerical Monte Carlo Method

Using the analytic solution for a single plane wave [39], we simulated a reverberant environment by calculating the power dissipated in the load of a TL. This was achieved by applying multiple randomly chosen plane waves simultaneously and averaging the results over several sets of plane waves, as described in detail in [7]. This approach is computationally faster than using a full-wave solver but assumes an idealized geometry with an infinite ground plane.

4.1.2 Gauss-Legendre Quadrature combined with full-wave solver

Using a full-wave solver [40], we illuminated a track on a finite PCB with a number of plane waves, selected based on the Gauss-Legendre Quadrature method [6], [41] to achieve optimal results with the minimum number of simulations. We determined that 64 individual plane wave simulations were sufficient; however, this still required a substantial amount of time to compute. The PCB model used in these simulations was of the same dimensions as the one utilized in the measurements presented in the next section.

4.1.3 Experimental Method

A PCB featuring lossy microstrip TL traces, as shown in Figure 6, was utilized for the measurements. The PCB has dimensions of 100 mm × 50 mm, and its substrate (FR-4)

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height is 1.55 mm. There are three traces on the PCB, each with different lengths (60 mm, 40 mm, and 20 mm), oriented orthogonally to minimize the coupling effect between them. Each trace has a width of 0.48 mm and a thickness of 18 µm.

For coupled signal measurement, four sub-miniature coaxial cable (SMA) connectors are used - one at each end of the long track and one at one end of each of the shorter tracks, as shown in the right picture of Figure 6. To match the characteristic impedance (115 Ω) of the traces to the impedance of the measurement system ($Z_{VNA} = 50\,\Omega$), an additional series resistance of 65 Ω is added near each SMA connector (Rs = R11 = R12 = R21 = R31 = 65 Ω). Moreover, the ends of the 40 mm and 20 mm tracks without SMA connectors are equipped with load resistances of $Z_L = R32 = R22 = 115\,\Omega$ to provide a matched termination.

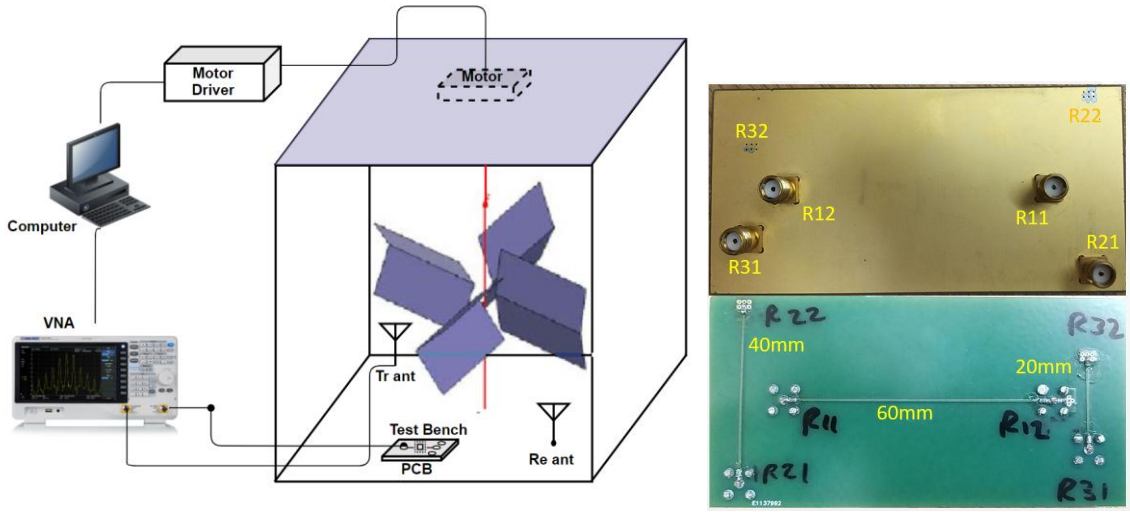

Figure 6: The left figure shows the experimental setup of the measurement conducted in the Reverberation Chamber and the right figure shows the PCB front and back sides.

The left diagram of Figure 6 illustrates the experimental setup within the reverberation chamber. The dimensions of the reverberation chamber are 4.7 m × 3.0 m × 2.37 m. The experiments employed 100 stirrer positions, meaning that for every 3.6 degrees of stirrer rotation, the frequency is swept from 500 MHz to 10 GHz, and S-parameters between two VNA ports are measured with a frequency step of 1 MHz.

Initially, a calibration measurement is conducted by connecting the antennas shown in the left diagram of Figure 6 to ports 1 and 2 of a vector network analyser (VNA). Meanwhile, the PCB is positioned inside the reverberation chamber, and 50 Ω loads are attached to all four SMA connectors. This calibration process allows us to compute the chamber's coupling factor for accurate subsequent measurements within the reverberation chamber.

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4.1.4 Computation of Track's Coupled Power

If the coupling to the loads on the ends of the PCB track is measured, we can determine the AACS of the loads connected to the track. The load consists of a 65Ω resistance in series with the track connector and the 50Ω resistance of the measurement instrument, as shown in Figure 7 for the long track and Figure 8 for the short tracks. To calculate the total power at one end of the track from the measured power, we need to take into account the combined effects of the load and the measurement instrument resistances.

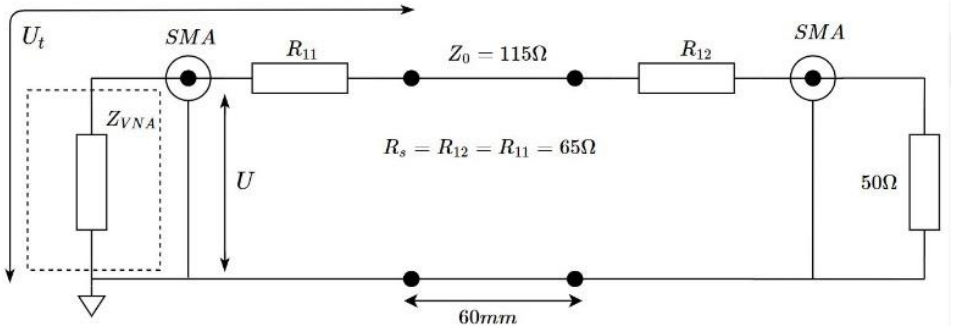

Figure 7: Shows the schematic diagram when one end of the 60mm trace is connected to VNA.

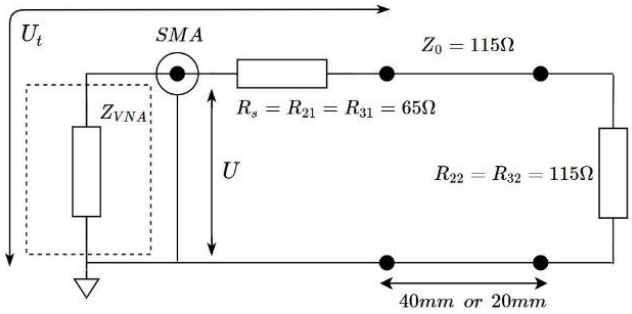

Figure 8: Shows the schematic diagram when one end of the 40mm or 20mm trace is connected to VNA.

The power absorbed at the end of the trace denoted as P_a, can be expressed in terms of the power measured by the measurement instrument, denoted as P_3.

$$P_a = P_3 \frac{(Z_{VNA} + R_s)}{Z_{VNA}} = P_1 |S_{31} - \langle S_{31} \rangle|^2 \frac{(Z_{VNA} + R_s)}{Z_{VNA}} \tag{36}$$

where $Z_{VNA} = 50\,\Omega$ represents the input impedance of the VNA, and S_{31} denotes the measured coupling between the antenna and PCB track output connector.

Utilizing the calibration factor (K) obtained from Section 3.2.6 [16], the AACS at the end of the PCB track can be expressed as follows:

$$\begin{aligned} \langle \sigma_t^a \rangle = \frac{\langle P_a \rangle}{S_0} &= P_1 \langle |S_{31} - \langle S_{31} \rangle|^2 \rangle \frac{(Z_{VNA} + R_s)}{Z_{VNA}} \cdot \frac{1}{K \langle P_1 \rangle} \\ &= \frac{\langle |S_{31} - \langle S_{31} \rangle|^2 \rangle}{K} \cdot \frac{(Z_{VNA} + R_s)}{Z_{VNA}} \end{aligned} \tag{37}$$

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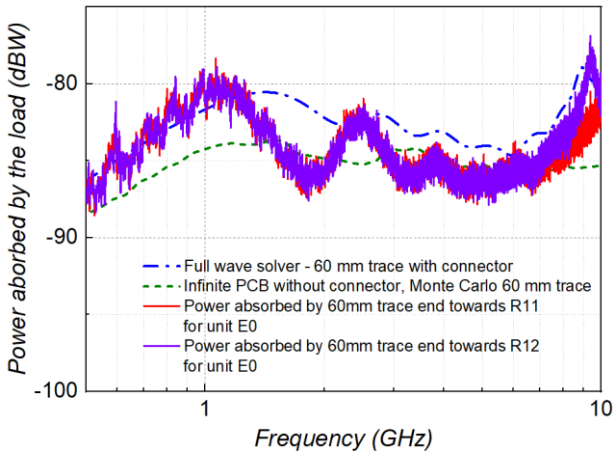

Figure 9: Shows the average power absorbed by 60mm trace-matched loads for 1 V/m total field.

Figure 9 displays the measured power in the loads at each end of the 60mm track, along with the predicted values obtained using the methods described in [7]. As anticipated in [7], the absorbed power increases with frequency up to just above 1 GHz, where it exhibits periodic oscillations dependent on the trace length, after which the overall trend levels out. The measurements align well with the results from the full-wave solver [40].

The full-wave solver and measured data show a slightly higher power prediction compared to the Monte-Carlo solution. This discrepancy is attributed, in part, to the semi-analytic nature of the Monte-Carlo solution, which assumes an infinite ground plane for the trace. In contrast, both the measured and simulated cases involve a finite ground plane (refer to [7], Figure 5).

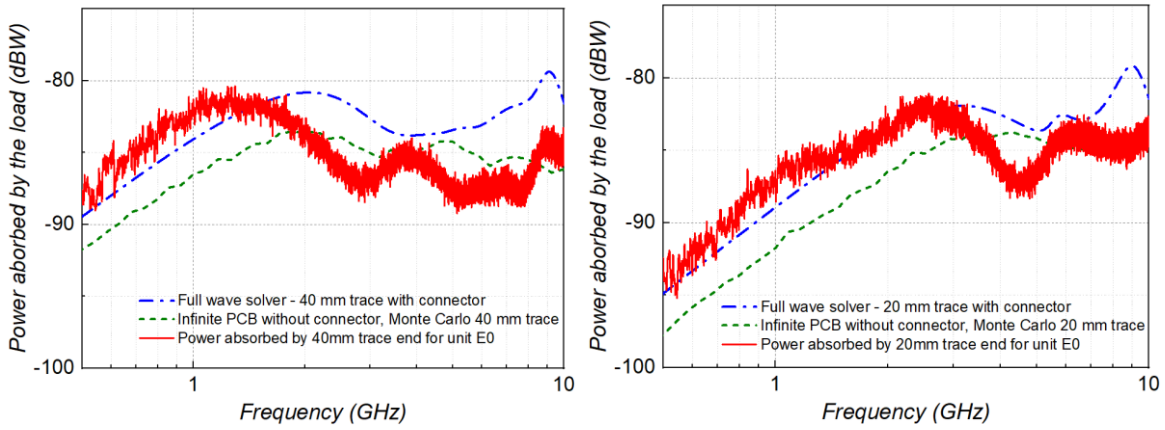

Figure 10: The left figure shows the average power absorbed by 40mm trace-matched loads for 1 V/m total field and the right figure shows the average power absorbed by 20mm trace-matched loads for 1 V/m total field.

The measured power in the loads of the shorter tracks is illustrated in Figure 10. It can be observed that as the trace length becomes shorter, the frequency at which the power trend levels out increases. However, all track lengths exhibit a similar maximum power (also refer to [7], Figure 7).

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All the information presented in this section is published in [16]. The measurements described in this section validate the predictions made in [7]. Further research is necessary to incorporate the PCB track losses into the numerical model and validate the updated numerical model with losses through measurements which will be discussed in subsequent chapters. PCB tracks frequently interconnect with IC packages, creating potential pickup scenarios in the package pins. This includes coupling effects on package, lead frame, bond wires and internal chip. Therefore, in the next section we discuss and consider the effects of any energy coupled through the IC package itself. And future research work is necessary to predict the shadowing effect of nearby traces and components.

4.2 Coupling of Energy into IC packages

In this section, the collaborative work with Hui Tang is discussed [17]. The majority of the work in this section is carried out by Hui Tang and Dr. John Dawson. The focus of this section is to investigate the EM power coupled into ICs through the package. All the results presented in this section are computed using a full-wave Finite Integration Technique (FIT) solver [40].

An easy prediction method is proposed for rapid estimation of the level of EMI coupled and absorbed at the inner loads of IC pins. Instead of considering the complicated package categories and large pin numbers, a simplified model is proposed and used to compute the absorbed power quickly. The analysis begins with an example of an IC Package of the Leaded Quad Flatpack type with 52 pins (LQFP 52). The study also explores the impact of the loads on the absorption of power. For the sake of simplicity, losses are ignored in this study. Previous research, which has not yet been published, indicates that their effect on energy absorbed is small. The study involves an ensemble of plane waves evenly distributed in an angle of arrival and polarization, which are representative of a reverberant environment, with frequencies up to 10 GHz.

4.2.1 IC Package Models and Analysis

As shown in Figure 11, a 52-pin LQFP package is mounted on a PCB with microstrip traces connected to the pins and PEC wires linking the inner ends of the lead frame to the IC bond pads. The external wave excites electric currents on both the PCB traces and PEC wires, leading to the absorption of EM power in the microstrip traces, as previously described by Xie et al [7]. For consistency with this prior work, we employ an FR4 substrate with a dielectric constant $\varepsilon_r = 4.4$, a thickness $t_s = 1.55$ mm, and a size of 40 mm $\times$ 40 mm as the test PCB. The characteristic impedance of the microstrip traces is set as $Z_c = 115\ \Omega$, with a thickness of t = 18 µm and a width of w = 0.45 mm to match the pins of the IC package.

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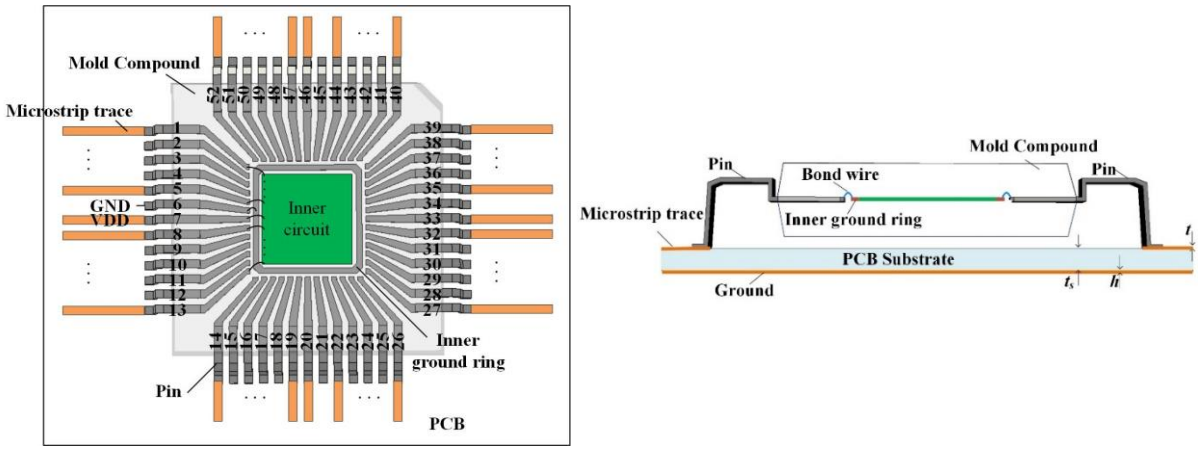

Figure 11: Shows the layout of the traces of the IC package in our design. Left figure: Top view and (b) Right figure: Side view.

This section focuses on the absorbed power at the inner ends of the pins. Unlike the PCB traces on which the radio frequency (RF) signals propagate, some power and ground (PG) traces that connect to the IC package are necessary, and all the pins are in close proximity to each other. The number and location of the PG pins significantly impact signal transmission into the IC. Notably, the distance between two adjacent pins on an LQFP 52 package is only 0.25 mm, causing significant cross-coupling between the pins. To establish a simplified model for estimating the EM energy coupled into the package, we investigate the influence of the PG traces and cross-coupling between pins in this section.

4.2.1.1 Influence of PG traces

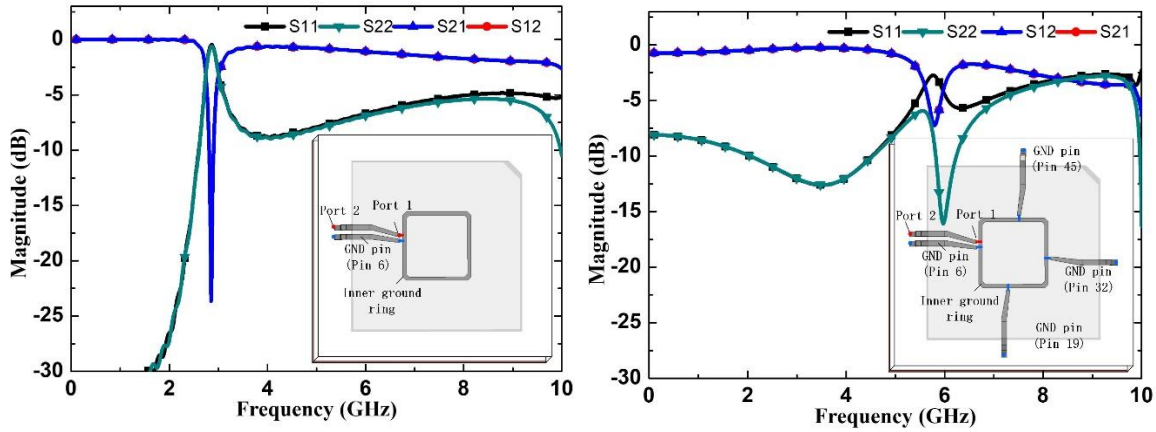

Figure 12: Shows different models for Pin 5 (terminated by 115 Ω outer port and 50Ω inner port). (a) S-parameters of one-side grounding model. (b) S-parameters of four-side grounding model.

In this study, we focus on Pin 5, as shown in Figure 11, as an example. However, the conclusions drawn from this example also apply to other pins, as demonstrated later. To investigate the impact of the number of GND pins, we have developed both one-side and four-side grounding models for Pin 5, as depicted in Figure 12 (a) and (b) respectively. In these models, the GND pins are connected to an inner ground ring and the PCB ground plane. The object pin (Pin 5) is considered as a dual-port network with a 115 Ω outer port

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to match the characteristic impedance of the microstrip traces and a 50 Ω inner port to match the input impedance of conventional microwave circuits.

Figure 12 also displays the S-parameters of Pin 5 for different grounding models. Notably, in the one-side model, there is a stopband observed at 2.85 GHz, while in the four-side model, another stopband appears at 5.83 GHz, both of which result from the resonance of the inner ground ring. This observation indicates that better grounding increases the resonant frequency, and consequently, more GND pins provide a wider transmission band for signals.

The impact of the location of the signal pin was investigated using models with different signal pin positions. Figure 13 illustrates the |S21| values of different pins with four-side GND pins. It is observed that there is a very slight change in the |S21| values of the different pins, indicating that the position of the signal pin does not significantly affect the transmission ability in this scenario. Instead, it emphasizes that a good grounding condition is essential for all pins to effectively transmit signals.

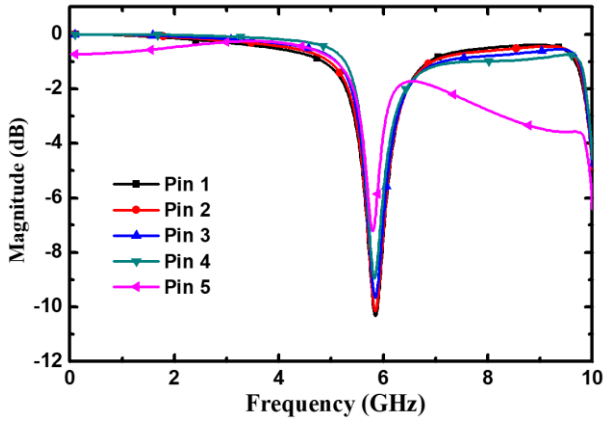

Figure 13: Shows |S21| of different signal pins with four-side GND pins.

4.2.1.2 Influence of cross-coupling between pins

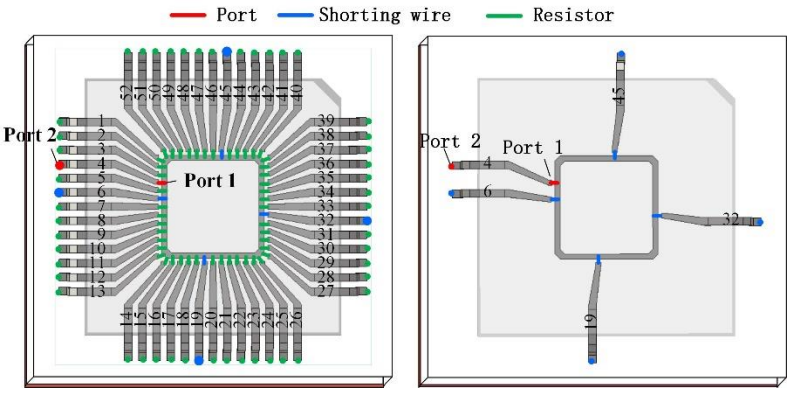

Figure 14: Shows the Pin 4 terminated by ports in different models and its S-parameters. (a) Full package model (left). (b) Single signal pin model (right).

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To investigate the influence of cross-coupling between pins, models with different numbers of adjacent pins were studied, with a particular focus on Pin 4. Although the effect on other pins is similar to that on Pin 4, due to space constraints, this work considers only the latter. In Figure 14 (a), Pin 4 is terminated by a 115 Ω outer port and a 50 Ω inner port in the full IC package model, which includes all other signal pins loaded by 115 Ω outer resistors and 50 Ω inner resistors. On the other hand, Figure 14 (b) depicts a single Pin 4 model with other signal pins removed. The S-parameters of Pin 4 in both models are presented in the right graph of Figure 15. A comparison reveals that the |S21| and |S12| curves in the full package model are flatter, with less insertion loss and no obvious stopband. This is due to the cross-coupling between pins, which aids in cancelling out the stopband and enhancing the transmission ability of the target pin with resistive terminations.

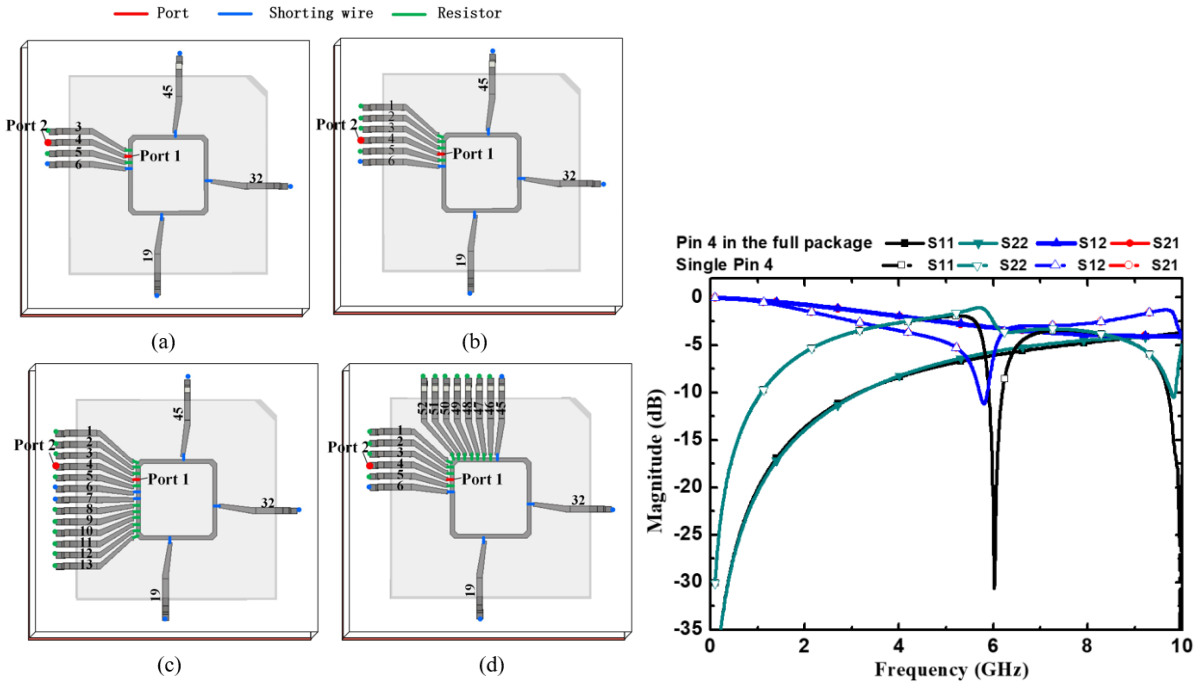

Figure 15: The left figure shows the Pin 4 terminated by ports in different models and its S-parameters. (a) Model A, (b) Model B, (c) Model C, (d) Model D and the right figure shows the Pin terminated by ports in different models and its S-parameters. Comparison of S-parameters.

To identify the influential pins affecting Pin 4, models with different numbers of adjacent pins are constructed and analyzed, as shown in Figure 15 (a)-(d). The comparison of the |S21| parameters of Pin 4 in these different models is presented in the left graph of Figure 16. The results indicate that the signal pins cannot be analyzed independently. Only in Model (d), where at least 13 pins are surrounded by two adjacent GND pins, does the transmission gain |S21| of Pin 4 closely resemble that in the full package model. Thus, the smallest unit for analyzing Pin 4 effectively contains at least 13 pins, which equates to nearly a quarter of the full package.

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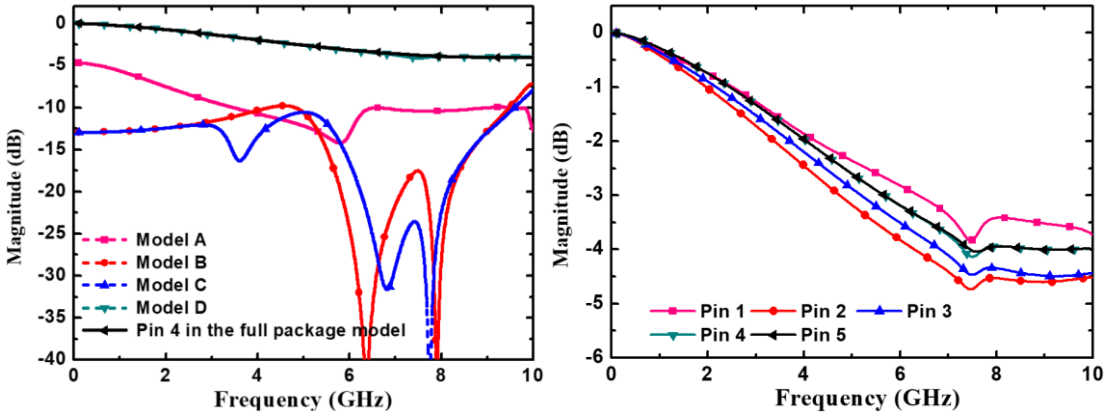

Figure 16: In the left figure Pin 4 terminated by ports in different models and its S-parameters (Comparison of |S21| in different models) and the right figure shows |S21| between different pins and their respective bond pads in the simplified model of Figure 15 (d).

To verify the applicability of the simplified model shown in Figure 15 (d) to other pins and its suitability for simplification, the transmission gains |S21| of different pins in the simplified model are investigated, as illustrated in the right graph of Figure 16. The results demonstrate that there are only very slight differences between the transmission gains of pins in Model (d) and those in the full package model. The pins in Model (d) exhibit similar transmission abilities as they do in the full package model. Moreover, due to the symmetry of the structure, a universal simplified model for each pin of the LQFP 52, except for the GND ones, has been successfully achieved.

4.3 Comparison of PCB Track and Package Coupling

In [7], the study focused on the energy coupled into PCB traces. In this section, we compare the levels of PCB trace coupling with track coupling to determine whether package coupling should be considered when determining the total energy coupled into a circuit for immunity analysis.

Figure 17 presents a comparison between the power absorbed into the inner terminal of the IC package alone and the power absorbed by a matched load on a 115 microstrip line trace, with a height of 1.55mm on FR4 material, as based on Figure 6 in [7]. It can be observed that at frequencies above 2 GHz, the power absorbed by the package is comparable to that of a 60 mm long track when matched with a resistive load that dissipates maximum power. The physical size of the track allows it to reach its highest power level at a lower frequency than the package.

The analysis of the transmission characteristics of a 52-pin LQFP package has led to the development of a simplified method for estimating the level of RF interference coupled into ICs through the package, initially with resistive loads. To include cross-coupling effects, S-parameters of different models were studied, and the coupled EM powers in the simplified

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and full-package models were compared. Within our investigated frequency range up to 10 GHz, the calculated absorbed power of the pins farthest away from the GND pins in the simplified model proves suitable for estimating EM energy coupled into the IC package. This simplified approach saves both time and computer memory.

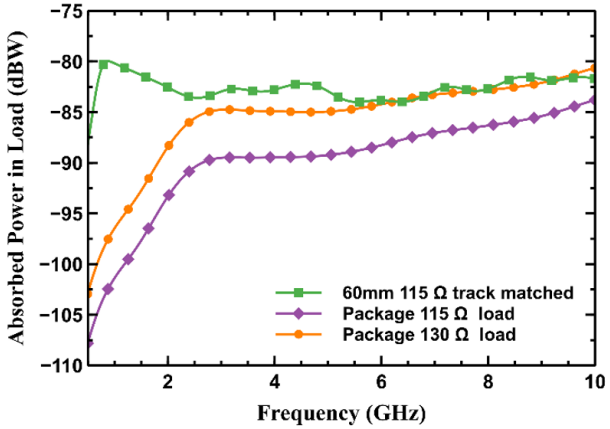

Figure 17: Comparing the power absorbed by a 1.55mm high, 60mm long, 115 ohm microstrip track with that absorbed by 115 Ω and 130 Ω loads on the package pin 1 inner terminal.

Further validation of the numerical model [7] through the design and testing of the RF IC detector, which will be discussed in the following chapters, will provide direct insights into the pickup on the IC bond pad. Moreover, it will enable us to understand the effects of real circuit loads such as ICs connected to a PCB trace instead of the resistive terminations used in this study.

Since we have focused only on the package and a single track in this preliminary work, there is more research needed to incorporate the losses into the numerical model and to explore the interaction between multiple tracks and how it affects the energy absorption levels when considering both the track and package pins together.

In this preliminary phase, we have not yet considered the realistic range of termination impedances for the inner pads. However, in our upcoming chapters, we will derive and incorporate these data into the numerical model using the RF IC detector. This important step will significantly enhance the accuracy and applicability of the model for practical scenarios.

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5. RF IC Detector

In Chapter 1, we introduced the need for the design of the RF IC detector, which is specifically intended to measure the coupled power at package pins via measurements of test RF PCB tracks. The main purpose of this design is to validate the numerical model [7] capable of estimating the stochastic EM coupling into PCB traces and validate the analytical methodology to predict the probability of susceptibility of IC to EMI. Our understanding of the internal structure of the RF IC detector and package will allow us to analyse its behaviour and internal floor planning in a depth that is often not possible with proprietary commercial designs, where comprehensive details are usually not disclosed to the user. In Chapter 4, our focus was on the coupling of energy to PCB traces and IC packages with known loads. Now, in this chapter, we present the design of the RF IC detector with the goal of detecting the energy coupled into the RF PCB tracks and IC packages. The designed RF IC detector functions as a realistic load for the RF PCB tracks, enabling us to analyse the coupled forward power to PCB tracks and IC package pins with a realistic load. The primary objective of this design is not only to validate the numerical model capable of estimating the stochastic EM coupling into PCB traces and the analytical model capable of predicting the probability of IC failure to EMI but also to develop an enhanced PWB method by assessing the AACS of the realistic load such as ICs via measurements of test RF PCB tracks.

The RF IC detector is capable of detecting and measuring EM power in the RF range, making it ideal for wireless communication applications. Its high sensitivity allows the measurement of low-level signals and helps analyse emissions from external sources. Operating across wide frequency ranges, it finds applications in diverse industries like telecommunications, radar, and aerospace, addressing EMI concerns in various domains.

In this chapter, we begin by discussing the technology utilized in this work, specifically focusing on the 0.18um HV SOI CMOS technology, parasitic extraction, and process variation and mismatch in Cadence Virtuoso [42]. We then present the design flow chart of the RF IC detector, followed by an explanation of its working principle. We then provide a detailed design procedure, starting from the block level and progressing to the system level. Both schematic and layout designs of the RF IC detector are presented, and their performance is verified through post-layout simulations. Additionally, a detailed PAD ring design is included. Furthermore, a bond diagram of the RF IC detector is presented prior to its fabrication. Lastly, a final microscopic view of the RF IC detector is provided.

Overall, this chapter outlines the comprehensive design process of the RF IC detector, showcasing its potential applications and contributions to the field of EMI analysis and measurement.

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5.1 0.18 um HV SOI CMOS Technology

The 0.18 µm HV SOI CMOS technology is a semiconductor fabrication process that integrates high-voltage circuitry with CMOS devices on a silicon-on-insulator (SOI) substrate. It offers several key advantages over standard CMOS technology, including reduced power consumption, improved performance, enhanced radiation hardness, and high-voltage capability. With all these advantages the balance between complexity and accessibility of the technology makes it suitable for this research work. This technology enables the design of RF IC detectors for measuring coupled power to package pins and PCB tracks, thereby validating the estimation of device susceptibility to EMI. With its integration of high-voltage and low-voltage functionality, it finds applications in power management, motor control, and other high-voltage systems. The 0.18 µm HV SOI CMOS technology provides a foundation for designing efficient and high-performance RF IC detectors, contributing to advancements in RF and microwave systems. The motivation for choosing 0.18 µm HV SOI CMOS technology in our research lies in its numerous advantages, primarily its ability to build products with improved EMC and enhanced robustness [43].

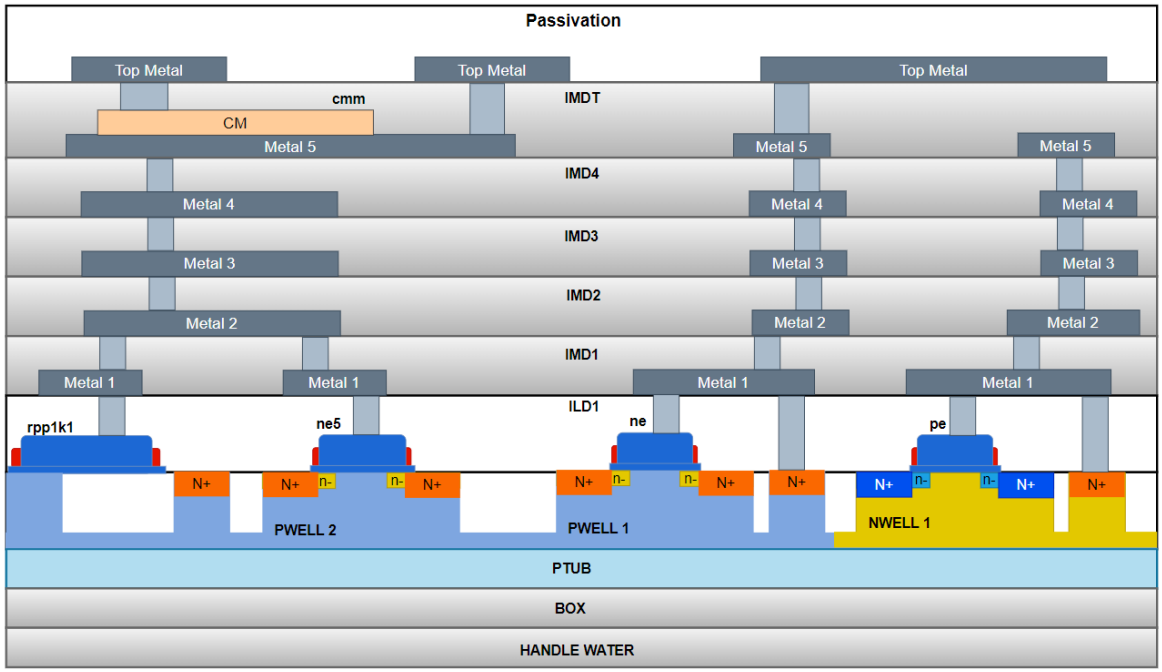

Figure 18: Shows the wafer cross-section of XT018 technology. [Reference]: Process and Device Specification XT018 - 0.18 µm HV SOI CMOS technology [44].

The entire RF IC design was implemented using the X-FAB XT018 0.18 µm HV SOI CMOS technology within the Cadence Virtuoso [42] simulator. The design was specifically tailored to operate at a supply voltage (VDD) of 5V. The primary objective of this chapter is to design an RF IC detector consisting of multiple sub-channels dedicated to channels 1 and 2. Each sub-channel within the detector is allocated a unique sensitivity level to

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effectively capture and measure the coupled energy directed towards its corresponding package pin. The interconnection of these package pins via a PCB test track will be further elaborated in the subsequent chapter, which focuses on the design of PCB test benches for the RF IC detector.

5.2 Cadence Virtuoso IC Simulator

Cadence Virtuoso, an industry-standard EDA software, is tailored for analogue, mixed-signal, and custom digital IC design, enabling schematic capture, simulation, layout, and verification. It offers robust tools for simulation, layout editing, design rule checking (DRC), parasitic extraction, and post-layout simulation, ensuring high-performance, low-power, and reliable semiconductor designs. Virtuoso seamlessly integrates diverse processing technologies, such as SOI and SiGe, various technology nodes, standard cells, memory compilers, and custom libraries. Supporting foundry-specific design kits, it provides designers with flexibility and accuracy throughout the design process, from concept to tape-out, for cutting-edge semiconductor devices.

5.2.1 Parasitic Extraction

By performing parasitic extraction, we can capture the parasitic effects inherent in the IC layout. These effects can then be incorporated into Cadence circuit models for post-layout simulation and analysis. This approach enhances the realism of our simulations and predictions concerning the overall behaviour of the design. In the Cadence Quantus Resistance Capacitance (QRC) extraction process, a netlist describing the connections of the IC design and devices is generated. Subsequently, it extracts resistance and capacitance by calculating values between various nodes, interconnect lines, vias, and conductive paths in the design. Throughout our research, we solely focus on RC extraction.

Regarding the exclusion of inductance during QRC extraction, our choice stems from practical considerations, primarily the substantial computational cost associated with its extraction and analysis, particularly in terms of simulation time and memory. In tools like Cadence, inductance extraction involves the use of a ladder network that takes into account effects such as skin effect and proximity effect. However, this approach results in a notably larger netlist size and extended simulation runtime.

While we omit inductance in our current research due to these reasons, it is worth noting that its consideration becomes crucial for higher frequency applications. At elevated frequencies, the impact of inductance becomes significant, and its inclusion in parasitic extraction becomes more relevant.

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5.2.2 Process Variation and Mismatch

Process variation in IC design encompasses the inherent variability that may arise during the fabrication process of ICs and is influenced by factors such as variations in etching, lithography, doping, and other fabrication procedures. It results in deviations in the electrical properties, dimensions, and performance of the components utilized in IC design. Similarly, mismatch pertains to variations in the properties of identical or closely matched components on an IC.

This work utilizes a technique known as Corner Analysis to tackle process variation and mismatch. This technique entails simulating circuits under various extreme operating conditions, referred to as corners, which correspond to specific combinations of process parameters like transistor sizes, threshold voltage, and temperature ranges. By incorporating these corners into the analysis, one can effectively capture the anticipated range of variations and evaluate their impact on circuit performance.

Figure 19 illustrates the potential worst process variations and mismatches that may occur in IC design when employing the Corner Analysis approach. It provides a visual representation of the extreme scenarios that could impact timing, power, and signal integrity within the design.

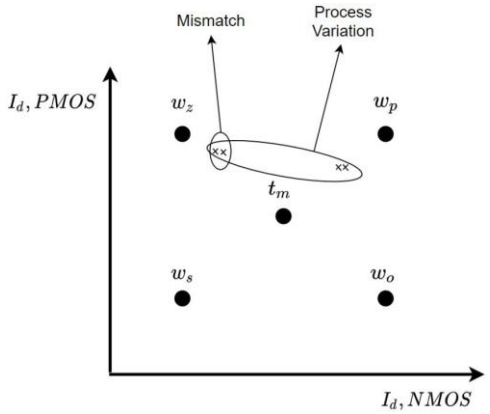

Figure 19: Shows the potential worst process variations and mismatches that may occur in IC design when employing the Corner Analysis approach.

The following are the important terms used in corner analysis:

- Typical Mean ($\boldsymbol{t_m}$): Serves as a baseline for normal behaviour, guiding circuit optimization for typical operating scenarios.
- Worst Power ($\boldsymbol{w_p}$): Identifies conditions leading to maximum power consumption, aiding in designing circuits to handle peak power demands and improve power efficiency.
- Worst Speed ($\boldsymbol{w_s}$): Considers factors causing the slowest circuit performance, ensuring critical paths meet timing requirements even under challenging conditions.

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- Worst One (w_o): Focuses on the scenario maximizing the delay of logical one signals, aiding in maintaining signal integrity and addressing timing issues for their transition.
- Worst Zero (w_z): Examines conditions resulting in the longest delay for logical zero signals, helping address timing challenges for their transition and ensuring overall signal integrity.

This research work presents the impact of process variations on critical aspects such as power consumption and circuit speed by considering extreme corners, specifically the worst power and worst speed corner cases along with the typical mean. This analysis ensures that the circuit meets performance requirements across a range of process variations, enhancing the overall reliability and functionality of the IC. Further, to mitigate the effects of process variations and mismatch, this work incorporates layout optimization, transistor sizing, and process calibration techniques. It is worth noting that skewed corners, specifically the worst-one and worst-zero, are not taken into consideration. This decision is based on the predominant analogue nature of most circuit blocks in the RF IC detector, where skewed corners pose a greater concern for digital circuitry

5.3 Design Flow Chart

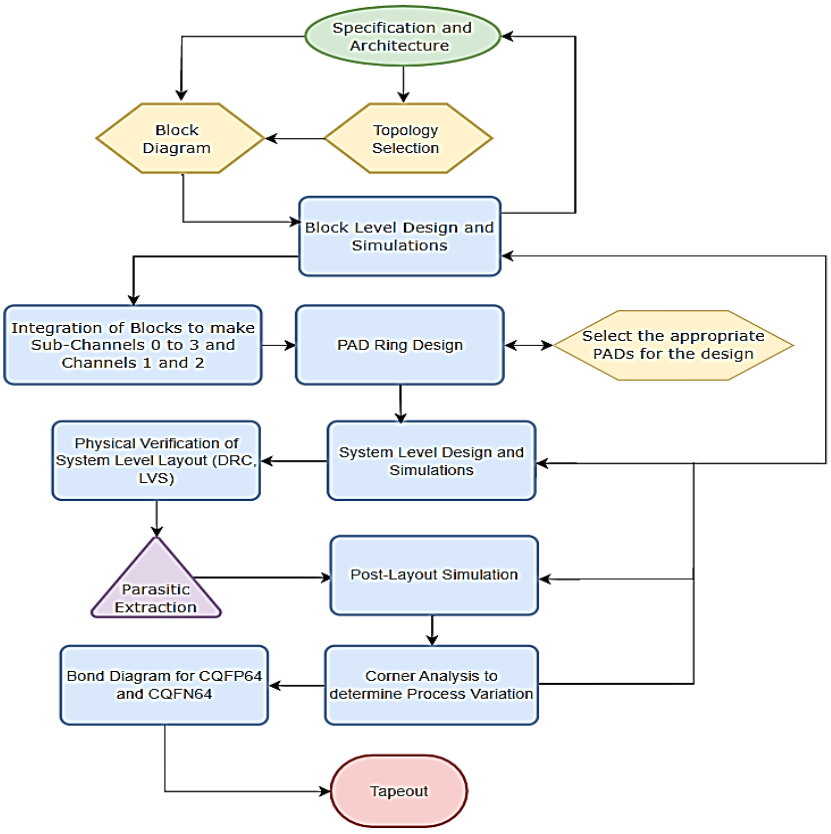

Figure 20: Shows the design flow chart of the RF IC Detector.

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5.4 Architecture of RF IC Detector

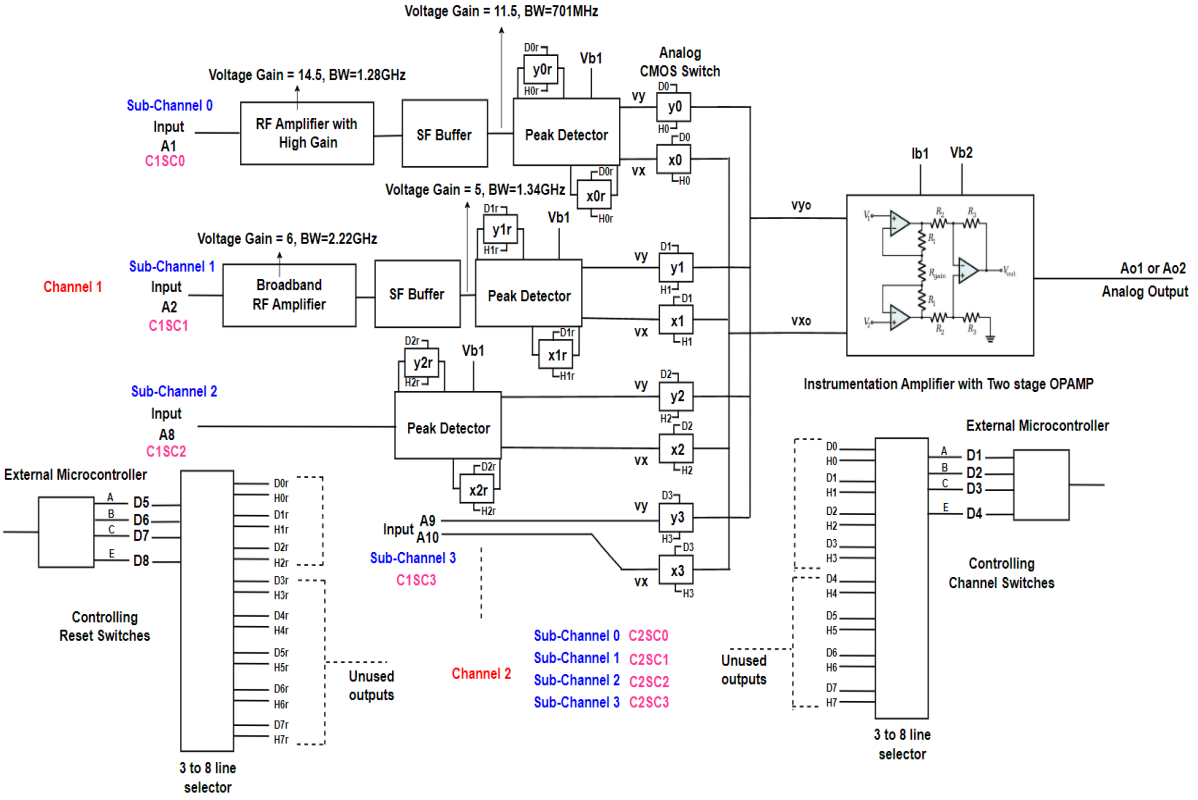

Figure 21: Shows the block diagram of the RF IC detector.

The RF IC Detector consists of two channels, each comprising four sub-channels, resulting in a total of eight detector channels, as illustrated in Figure 21. These channels are connected to the package pins via I/O cells and bond pads. Sub-channels 0-3 (SC0, SC1, SC2, SC3) of Channel 1 (C1) exhibit varying sensitivity levels based on the amplification circuit blocks integrated into them. Notably, sub-channels 0-3 (SC0, SC1, SC2, SC3) of Channel 2 (C2) employ identical input circuits to those found in Channel 1. The primary distinction lies in the nature of the input I/O cells: sub-channels 0-3 of Channel 1 employ low series resistance (<1 Ω) analogue input I/O cells, while sub-channels 0-3 of Channel 2 utilize analogue input I/O cells with a series resistance of 100 Ω. Each set of channels is connected to a differential instrumentation amplifier (IA) through an analogue multiplexer, followed by a high series resistance (1k Ω) analogue output I/O cell.

Specifically, sub-channels 0 of channels 1 and 2 (C1SC0 and C2SC0) feature a high-gain RF amplifier to maximize the sensitivity level of the detector. Sub-channels 1 of channels 1 and 2 (C1SC1 and C2SC1) are equipped with a broadband RF amplifier, enabling the detector to operate optimally for the higher frequency band albeit with reduced sensitivity. In contrast, sub-channels 2 of channels 1 and 2 (C1SC2 and C2SC2) do not undergo any amplification; the input signal is directly connected to the peak detector which makes it the less sensitive sub-channel compared to sub-channel 1 and 2. Lastly, for sub-

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channels 3 of channels 1 and 2 (C1SC3 and C2SC3), the input signal is directly routed to the IA, allowing for a comprehensive understanding of the behaviour and limitations of the OPAMPs within the IA.

Channel switching is managed through analogue complementary metal-oxide-semiconductor (CMOS) switches, which are controlled by a 3-to-8-line decoder. Sub-channels 0 of Channels 1 and 2 operate simultaneously, as their switches are linked to the same output pins of the decoder. Similarly, sub-channels 1, 2, and 3 of both Channels 1 and 2 are connected to the same output pins of the decoder for concurrent operation. However, sub-channels 0 to 3 of both Channels 1 and 2 have distinct outputs routed through the same IA. A similar control mechanism is employed for the switches responsible for resetting the capacitor in the peak detector. The control signals for the 3-to-8-line decoder are supplied by an external microcontroller.

5.5 Sub-Channel Blocks

As discussed in the Section 5.4, each channel comprises four sub-channels. In this section, we delve into an in-depth exploration of each block within these sub-channels, elaborating on their respective designs and functionalities.

5.5.1 RF Amplifier Block

The RF amplifiers utilize the cascode technique to enhance high frequency circuit performance. Both Figure 22 and Figure 26 illustrate a cascode circuit which includes the Common Source-Common Gate (CS-CG) configuration. This combination utilizes the advantages of cascode techniques, resulting in high gain, wide bandwidth, and good linearity. The initial stage employs the common source (CS) amplifier, acting as the input stage and driven by an external signal source. Conversely, the common gate (CG) amplifier serves as the output stage.

The cascode configuration significantly contributes to the amplification and bandwidth improvement of the amplifier [45]. In the CS amplifier stage, the input signal is applied to the gate terminal, and the output signal from the drain terminal of the transistor is connected to the source terminal of the CG amplifier stage. In contrast, the CG amplifier stage has the input signal applied to the source terminal, with the output signal taken from the drain terminal of the transistor.

The CG amplifier stage presents a low input impedance to the CS amplifier stage, resulting in a low voltage gain for the CS amplifier. This, in turn, reduces the Miller capacitance of the CS amplifier. The combination of CS-CG amplifiers enhances the output impedance of the cascode amplifier, allowing the lower CS amplifier stage to operate with

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minimal Miller capacitance feedback, thereby improving its bandwidth. The Miller effect is less significant in the cascode configuration compared to a single-stage CS amplifier [45].

5.5.1.1 High Gain RF Amplifier

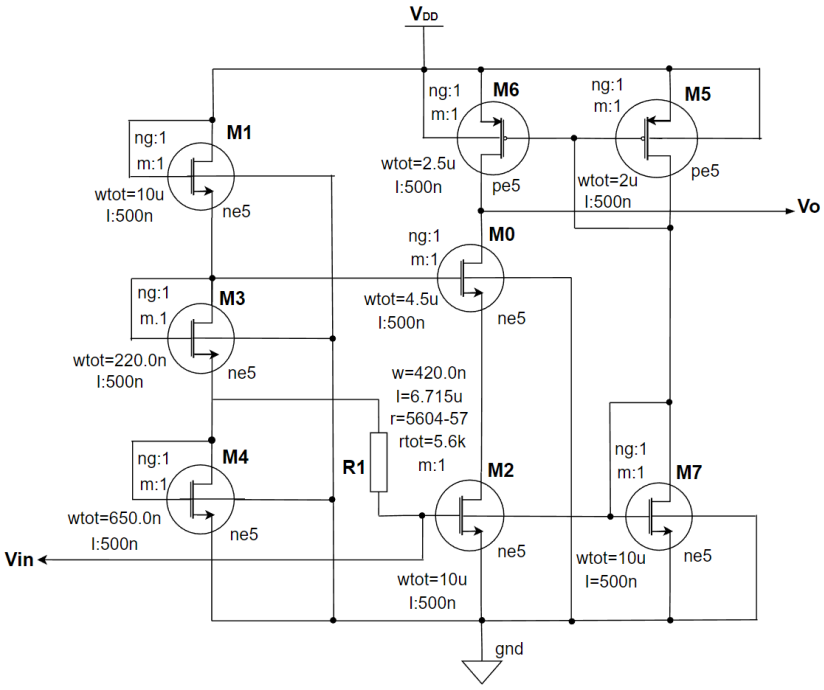

Figure 22: Shows the schematic of the High Gain RF Amplifier.

In the cascode configuration, MOSFET 2 (M2) serves as the CS amplifier, while M0 functions as the CG amplifier. A cascode amplifier necessitates a high-impedance load to achieve high gain [46][45]. Therefore, the PMOS current mirror (M6 and M5) is employed as the load for the RF amplifier. The small-signal output resistance of the common gate amplifier (M0) and the small-signal resistance of the current mirror (M6 and M5) can be adjusted to attain a high gain-bandwidth product from CG amplifier stage. By varying the load impedance, that is by varying the width of MOSFETs M0 and M6, it is possible to achieve a high gain while accepting a trade-off in terms of bandwidth.

MOSFETs M1, M3, and M4 act as voltage dividers, establishing distinct bias points for the gate of the common source amplifier M2 and the gate of the common gate amplifier M0.

5.5.1.2 Small Signal Model of RF amplifier

The small-signal model provides insight into the behaviour of the RF amplifier at low signal levels. It simplifies design calculations and allows for amplifier design tailored to specific requirements by linearizing the characteristics of the amplifier around its operating point.

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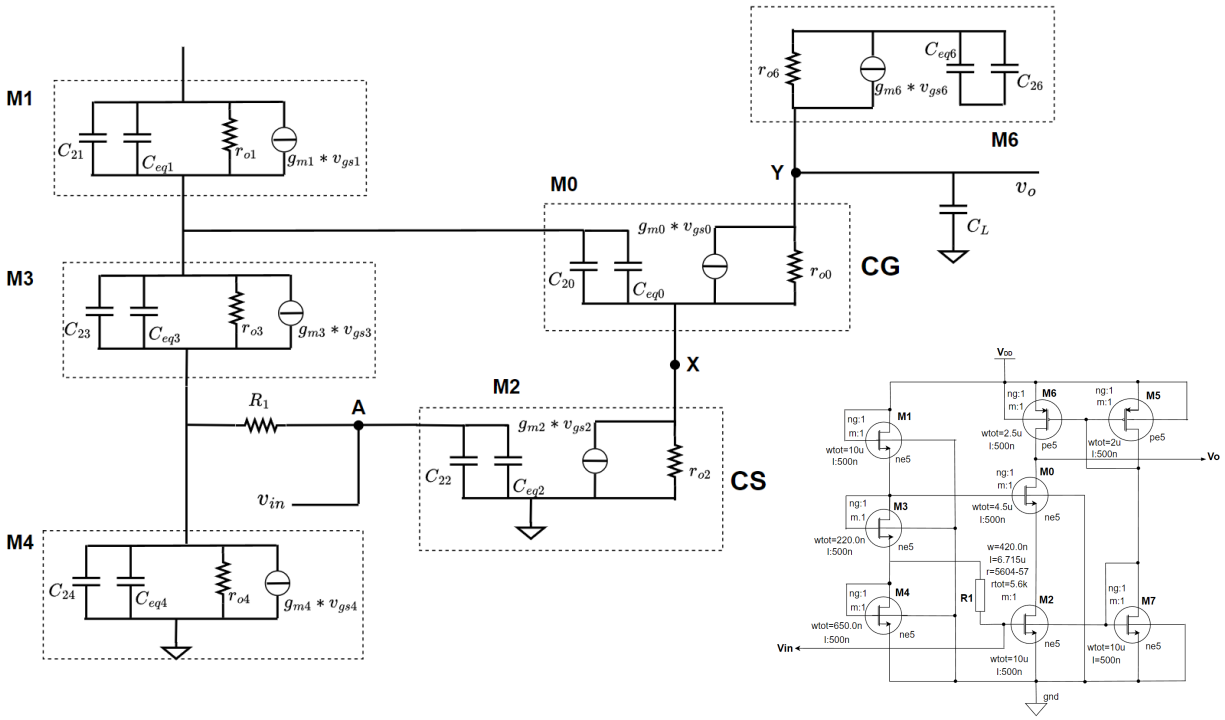

Figure 23: Shows the part of the small signal model of the RF amplifier

In high-frequency amplifier applications, understanding the Miller effect is crucial. The Miller effect pertains to the effective capacitance across a voltage gain stage due to inherent capacitances in the small-signal model. However, as explained earlier, the upper transistor M0 (CG) exhibits a low input impedance to M2 (CS), resulting in a low inverting voltage gain from M2 and there by reducing the Miller capacitance C_{eq2}. Similarly, C_{eq0} of M0 will also be very small due to the constant gate voltage for M0. The Miller capacitance, denoted as C_{eqX} in Figure 23, can be expressed as shown below [45], [46]:

$$C_{2X} = C_{gbX} + C_{gsX}$$
$$C_{eqX} = (1 + A_{vX})C_{gdX} \quad (38)$$

where, C_{gbX} represents the capacitance between the gate and body (substrate), C_{gsX} represents the capacitance between the gate and source, C_{gdX} represents the capacitance between the gate and drain, and A_{vX} is the voltage gain of the respective MX transistor.

From Figure 24, we can derive the output resistance of the RF amplifier, which is given by:

$$r_{id} = [(1 + g_{m0}r_{o0})r_{o2} + r_{o0}]$$
$$R_{out} = r_{o6} \| r_{id} = r_{o6} \| [(1 + g_{m0}r_{o0})r_{o2} + r_{o0}] \quad (39)$$

where, g_{m0} represents the transconductance of transistor M0, r_{id} is the output resistance of the transistor M0 as shown in Figure 24 and r_{o0}, r_{o2} and r_{o6} are the output resistance of transistor M0, M2 and M6 respectively.

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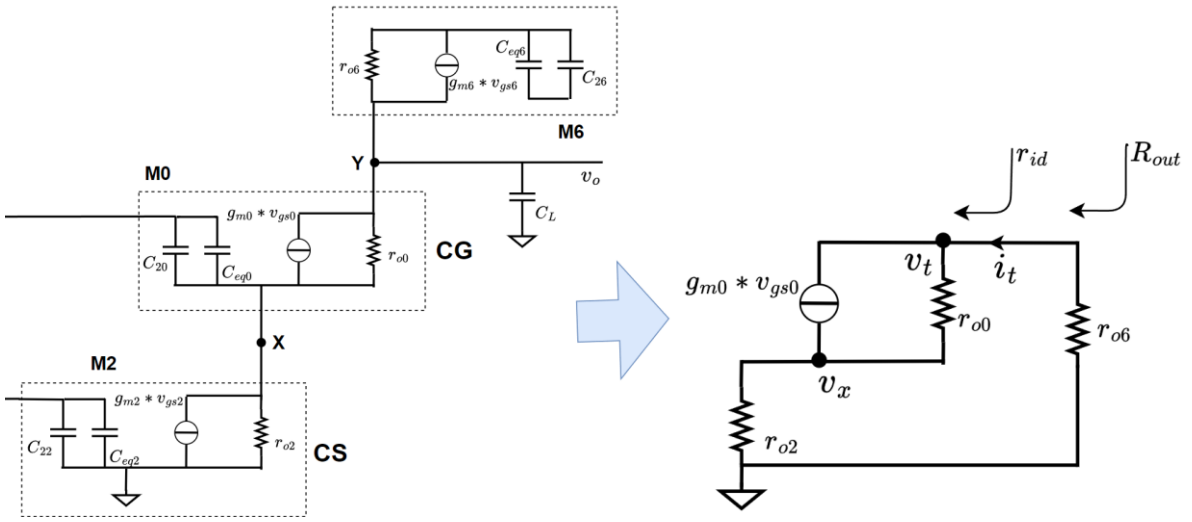

Figure 24: Shows the simplified small-signal model for output resistance approximation.

The gain of the cascode CS-CG amplifier from [45] is in the form of $G_m R_{out}$ and is given by:

$$A_v = \frac{v_o}{v_{in}} = -g_{m2} R_{out} = -g_{m2} r_{o6} \| \left[(1 + g_{m0} r_{o0}) r_{o2} + r_{o0} \right] \tag{40}$$

where, g_{m2} represents the transconductance of transistor M2, v_o and v_i is the output and input voltage of RF amplifier.

For frequency response analysis, we can deduce the poles associated with point A at the input of the CS amplifier stage, X at the output of the CS amplifier stage, and Y at the output of the CS-CG amplifier stage from [45], as shown below:

$$\begin{aligned} \omega_{p,A} &\approx \frac{1}{\left[C_{gs2} + \left(1 + \frac{g_{m2}}{g_{m0} + g_{mb0}} \right) C_{gd2} \right]} \\ \omega_{p,X} &\approx \frac{g_{m0} + g_{mb0}}{\left[2C_{gd2} + C_{db2} + C_{sb0} + C_{gs0} \right]} \\ \omega_{p,Y} &\approx \frac{1}{r_{o6}\left(C_{db0} + C_L + C_{gd0} \right)} \end{aligned} \tag{41}$$

where, g_{mb0} is the body effect transconductance of transistor M0, C_{gd2} is the capacitance between the gate and drain of the M2 transistor, C_{sb0} is the capacitance between the source and body of the M0 transistor, C_{db2} and C_{db0} are the capacitance between the drain and body of the M2 and M0 transistor respectively, C_{gs2} and C_{gs0} are the capacitance between the gate and source of M2 and M0 transistor respectively. C_L is the load capacitance, which represents the input capacitance of subsequent circuit block (Source Follower). We can approximate the input capacitance of the Source Follower (SF) using the equation given below from [45]:

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$$C_L = \frac{C_{gs1_{SF}}(g_{m1_{SF}} + {}^{1}/_{r_{o2\_SF}})}{g_{m1_{SF}} + g_{mb1_{SF}} + {}^{1}/_{r_{o2\_SF}}} \quad (42)$$

where, $C_{gs1_{SF}}$ the capacitance between the gate and source of M1 in the SF circuit block from Figure 28, $g_{m1_{SF}}$ represents the transconductance of transistor M1 in the SF block, $g_{mb1_{SF}}$ is the body effect transconductance of transistor M1 in the SF block and r_{o2_SF} stands for output resistance of transistor M2 in the SF block. After extracting the small signal parameters and calculating the input capacitance (C_L) of the SF, it will be equal to 8.53 fF.

Out of these above equations, the dominant pole closest to the cutoff frequency is at the output of the CS-CG amplifier stage (point Y from Figure 24). Small signal parameters extracted from Cadence for gain and bandwidth approximation are given in the table below:

Parameters extracted from Cadence				
Parameter	**Value**		**Parameter**	**Value**
g_{m2}	1.0134764 m℧		r_{o2}	40.61 kΩ
g_{m0}	0.5302625 m℧		r_{o6}	15.07 kΩ
g_{mb0}	0.1132499 m℧		I_{d2}	0.3353 mA
r_{o0}	83.84 kΩ		I_{d0}	0.3353 mA
C_{gs2}	8.4740 fF		C_{db2}	0.0042728 fF
C_{gd2}	2.7800 fF		C_{db0}	0.000539 fF
C_{gs0}	4.3699 fF		C_{sb0}	0.7283080 fF
R_{out}	14.95 kΩ		C_L	8.53 fF

Table 1: Small signal parameters of High Gain RF Amplifier extracted from Cadence.

where, I_{d2} and I_{d0} are the drain current through M2 and M0 transistor respectively.

We estimate and compare the gain and bandwidth of the RF gain amplifier using equations (40) and (41) as shown in the table below:

Comparison between Estimated Value and Simulation		
Parameter	**Estimated**	**Simulation**
Voltage Gain	15.1 = 23.57 dB	14.5 = 23.22 dB
Cut-off Frequency	1.1 GHz	1.2 GHz

Table 2: Shows the comparison between estimated value and simulated value of High Gain RF amplifier.

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5.5.1.3 Layout Design of High Gain RF Amplifier

Figure 228 from Appendix 11.9 displays the layout design of the high-gain RF amplifier. After completing the initial layout design and subsequent optimization, we conducted DRC (Design Rule Check) and LVS (Layout Versus Schematic) verification to ensure the layout complies with the design rules of the 0.18µm HV SOI CMOS technology and matches the original schematic design, respectively. Following the DRC and LVS checks, parasitic extraction was performed. Using the extracted parasitic data, post-layout simulations were conducted to evaluate the performance of the amplifier and compare it with the schematic simulation.

The frequency response of the high-gain RF amplifier is shown in Figure 25. The red curve represents the results from the schematic simulation, while the blue curve illustrates the post-layout simulation results.

In the schematic results, we observed a gain of 23 dB (decibels) and a bandwidth of 1.28 GHz. However, in the post-layout simulation, the results showed a gain of nearly 23 dB and a slightly reduced bandwidth of 0.99 GHz, as presented in Figure 25. This reduction in bandwidth can be attributed to the additional parasitic resistance and capacitance introduced by the interconnects considered in the post-layout simulation.

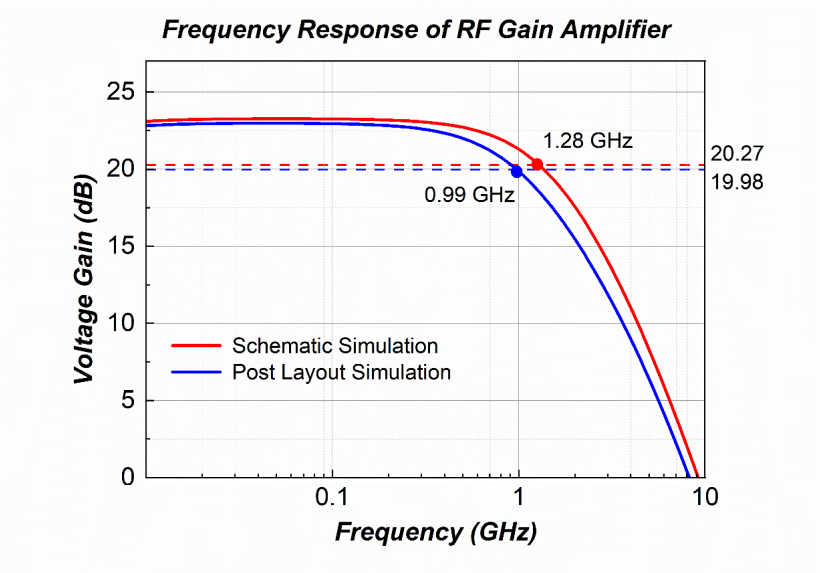

Figure 25: Shows the frequency response of schematic (red) and post layout (blue) simulation with 1.28 GHz RF amplifier: 991.77 MHz (23 dB).

5.5.1.4 Broadband RF Amplifier

The design of the broadband RF amplifier, as shown in Figure 26, remains almost identical to that of the high-gain RF amplifier. As elucidated in Section 5.5.1.1, a cascode amplifier necessitates a high-impedance load to achieve high gain. Consequently, the PMOS current mirror (M6 and M5) serves as the load for the RF amplifier. Adjusting the load of

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the RF amplifier offers control over its gain and bandwidth. Thus, modifying the small-signal output resistance of the common gate amplifier (M0) and the small-signal resistance of the current mirror (M6 and M5) facilitates achieving a high gain-bandwidth product. By varying the width of MOSFETs M0 and M6, we can achieve a high bandwidth while striking a trade-off in terms of gain.

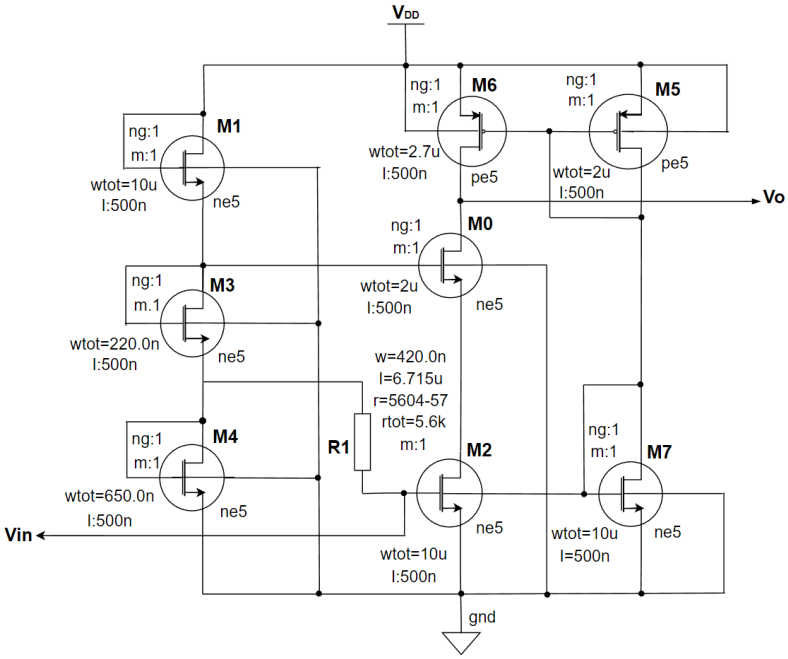

Figure 26: Shows the schematic of the Broadband RF Amplifier.

Figure 228 from Appendix 11.9 showcases the layout design of the broadband RF amplifier. The frequency response of the broadband RF amplifier is presented in Figure 27. The red curve represents the schematic simulation results, while the blue line portrays the post-layout simulation results.

Small signal parameters extracted from Cadence for gain and bandwidth approximation are given in the table below:

Parameters extracted from Cadence				
Parameter	**Value**		**Parameter**	**Value**
g_{m2}	0.9760099 m℧		r_{o2}	22.50 kΩ
g_{m0}	0.2583800 m℧		r_{o6}	7.08 kΩ
g_{mb0}	0.06699 m℧		I_{d2}	0.3186 mA
r_{o0}	191.38 kΩ		I_{d0}	0.3186 mA
C_{gs2}	8.5000 fF		C_{db2}	0.036373 fF
C_{gd2}	2.9306 fF		C_{db0}	0.000217 fF

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C_{gs0}	2.0200 fF		C_{sb0}	0.403450 fF
R_{out}	7.042 kΩ		C_L	8.53 fF

Table 3: Small signal parameters of Broadband RF Amplifier extracted from Cadence.

where, I_{d2} and I_{d0} are the drain current through M2 and M0 transistor respectively.

We estimate and compare the gain and bandwidth of the RF gain amplifier using equations (40) and (41) as shown in the table below:

Comparison between Estimated Value and Simulation		
Parameter	**Estimated**	**Simulation**
Voltage Gain	6.8 = 16.5 dB	6.4 = 16.1 dB
Cut-off Frequency	2.4 GHz	2.25 GHz

Table 4: Shows the comparison between estimated value and simulated value of Broadband RF amplifier.

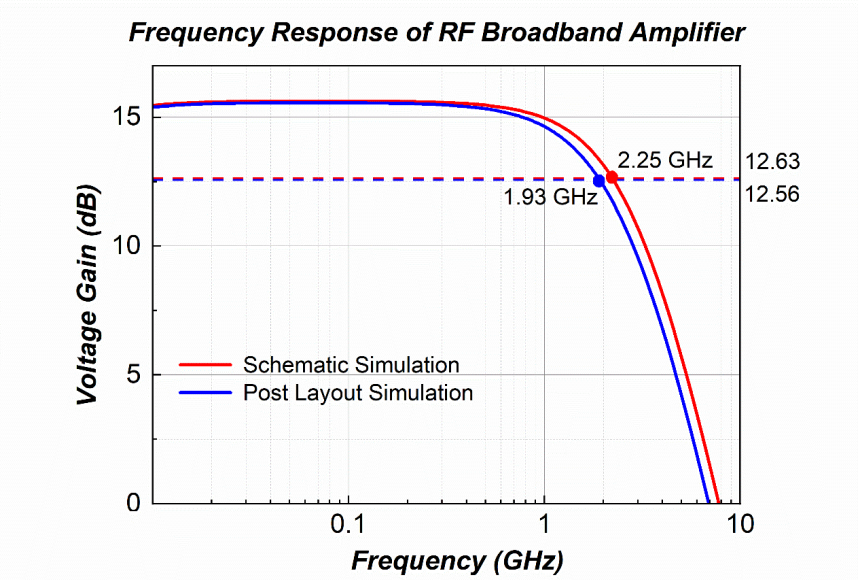

Figure 27: Shows the frequency response of schematic (red) and post layout (blue) simulation with 2.25 GHz RF amplifier: 1.92 GHz (15.5 dB).

In the schematic results, we observe a gain of 15.63 dB and a bandwidth of 2.25 GHz. However, in the post-layout simulation, the results display a gain of nearly 15.56 dB and a slightly reduced bandwidth of 1.93 GHz, as illustrated in Figure 27. This reduction in bandwidth can be attributed to the additional parasitic resistance and capacitance introduced by the interconnects considered in the post-layout simulation.

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5.5.2 Source Follower and Peak Detector

5.5.2.1 Source Follower

The source follower (SF) operates in a common-drain configuration, typically employed as a voltage buffer. Circuits utilizing the common-drain configuration are called 'followers' because the output voltage follows the input voltage. A source follower offers high input impedance, low output impedance, and inherently high current gain [45], [46]. The high input impedance enables the SF amplifier to interface with high-impedance circuit blocks without loading them. Conversely, the low output impedance allows the SF amplifier to drive subsequent low-impedance circuit blocks without signal degradation. Most importantly, the SF amplifier provides buffering and signal isolation between the input and output stages of the circuit.

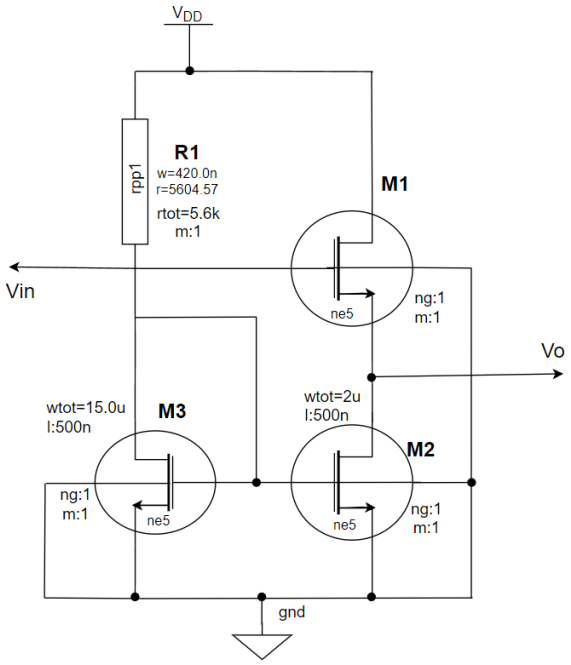

Figure 28: Shows the schematic of the Source Follower amplifier.

Incorporating the SF amplifier circuit block helps prevent the RF amplifiers from being loaded by the peak detector. MOSFET M1 is configured in a common-drain configuration, while MOSFETs M2 and M3 serve as the current mirror used to bias transistor M1, as shown in Figure 28. Due to the lower transconductance of MOSFETs compared to BJT transistors, the gain is not very close to unity [45]. However, for our application, the gain achieved is close to unity, as demonstrated in Figure 29.

Figure 229 from Appendix 11.9 displays the layout design of the source follower amplifier. The frequency response is presented in Figure 29. The red curve represents the schematic simulation results, while the blue curve portrays the post-layout simulation results.

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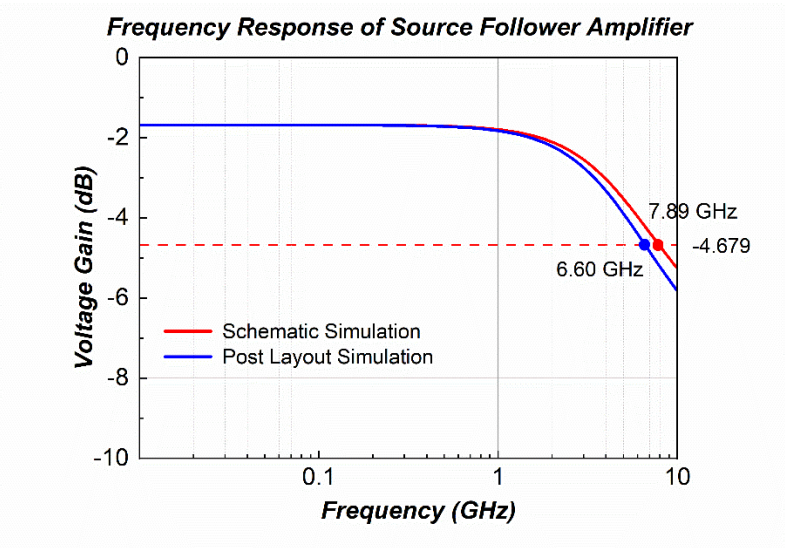

Figure 29: Shows the frequency response of Source Follower, which has nearly a unity gain of -1.6 dB.

In both schematic and post-layout simulation results, a gain of -1.6 dB is observed. However, the bandwidth differs; for schematic simulation, it is 7.87 GHz, and for the post-layout simulation, it is 6.59 GHz, as illustrated in Figure 29.

5.5.2.2 Peak Detector

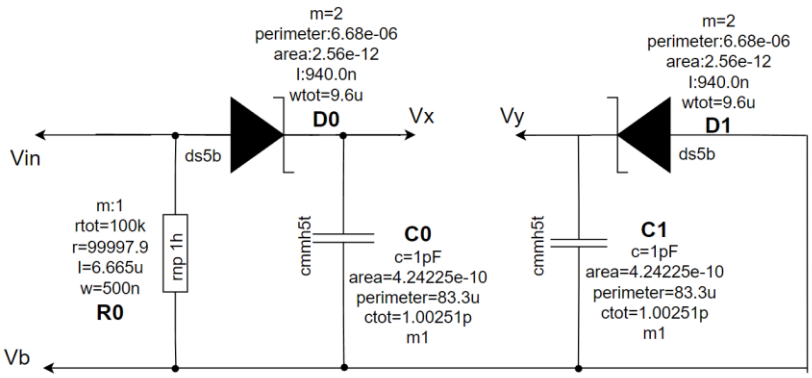

Figure 30: Shows the schematic of the Peak Detector.

There are several methods to design a peak detector. The simplest approach involves using a diode and capacitor. Typically, a resistor is employed to discharge the capacitors in practical applications. However, for our application, we utilize an analogue reset switch (not shown in this section) to discharge the capacitor. As the name suggests, the peak detector is designed to capture the highest point of the analogue signal and maintain that voltage until the capacitor is discharged through the reset switch.

The simple peak detector configuration using Schottky diode D0 and capacitor C0 is illustrated in Figure 30 (layout is shown in Figure 230). Schottky diodes are chosen for their low forward voltage drop and fast switching speeds, making them suitable for high-frequency applications despite their relatively high reverse leakage current.

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During the simulation, an observation of 'zero input charging' was noted. Zero input charging is a phenomenon in which the capacitor in the peak detector circuit accumulates charge even in the absence of an input signal. This can be attributed to the leakage current in the diode. To counteract the issue of zero-input charging observed during the simulation, another dummy peak detector is connected in an opposite configuration. This setup ensures that the differential output of Vx and Vy remains unaffected by the zero-input charging. Additionally, resistor R0 provides a DC path to charge the capacitor.

5.5.2.3 Integration of Source Follower and Peak detector

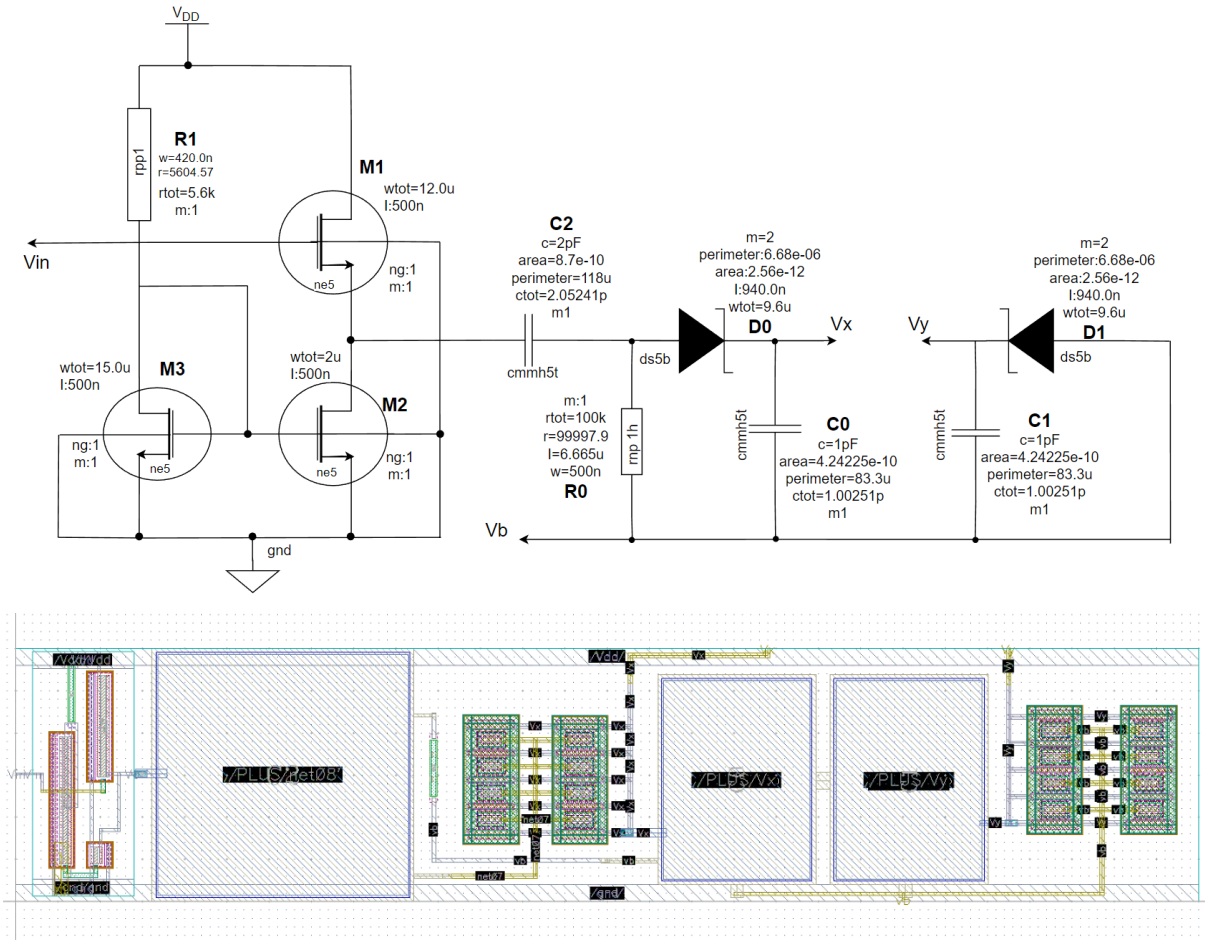

Figure 31: Shows the source follower buffer connected to a peak detector schematic and layout.

The connection between ground and substrate, often referred to as a substrate tie, is a common requirement in IC design, especially for CMOS technologies. It maintains proper biasing and isolation of devices within the IC. However, our peak detector consists solely of passive components (Schottky diode and capacitor), lacking an active device with a substrate connection. To facilitate post-layout simulation in the Cadence simulator, which necessitates the initiation of the substrate tie, we needed to address this absence of an active device. As we need to integrate a simple active device, such as a small transistor, into our circuit. We decided to use an active device block like the Source Follower. As a

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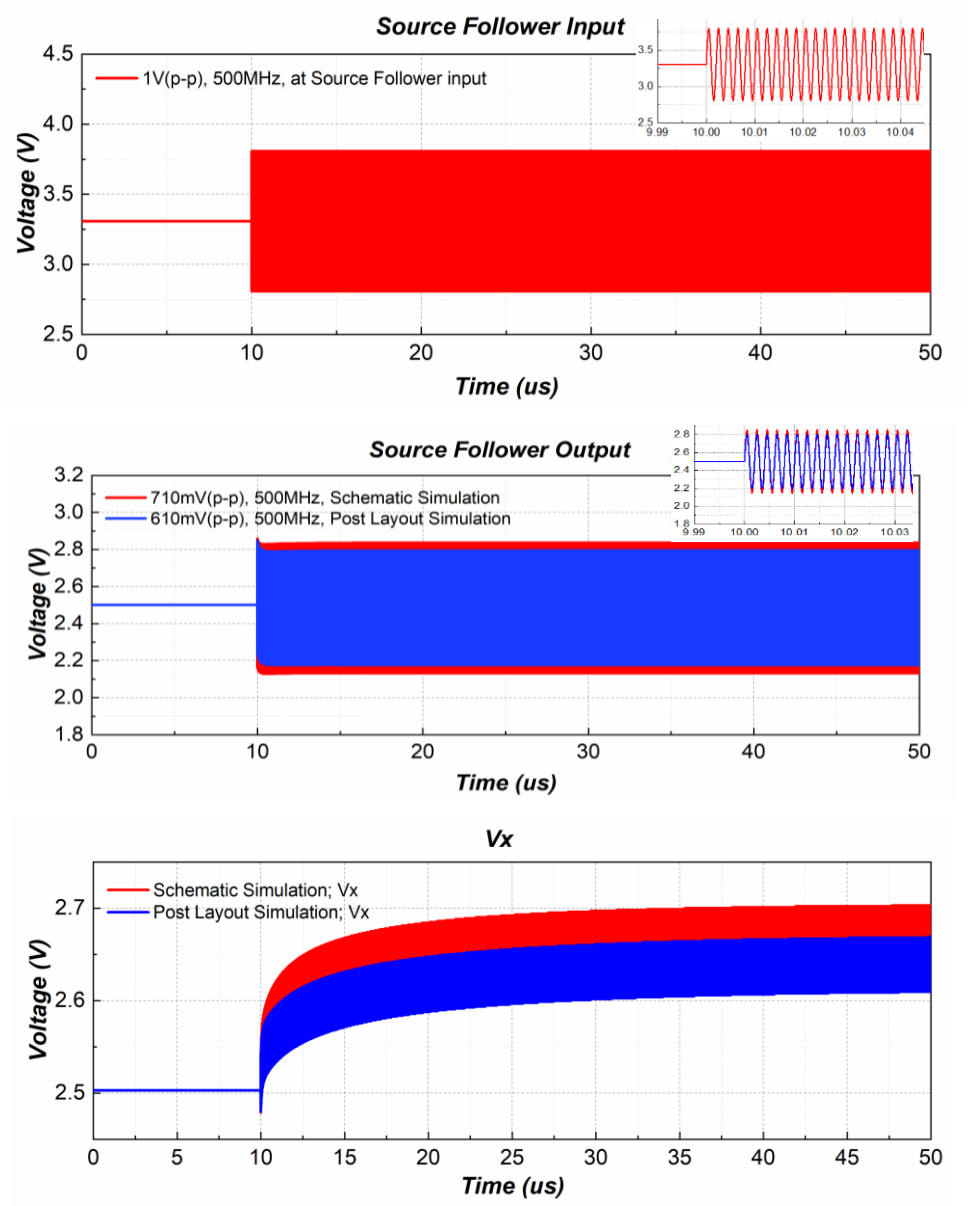
result, we employed a source follower circuit to drive the peak detector circuit, as shown in Figure 31. This allows us to compare the schematic simulation results with the post-layout simulation results effectively.

Figure 32 illustrates the transient response of the peak detector over a 50us duration at 500 MHz. During the interval from 10us to 50us, capacitor C0 charges. The graph consists of five subplots: the input to the source follower, the output of the source follower (input to the peak detector), output Vx, output Vy, and the final subplot displays the differential output (Vx-Vy) of the peak detector. The red curve represents the schematic simulation results, while the blue curve represents the post-layout simulation results.



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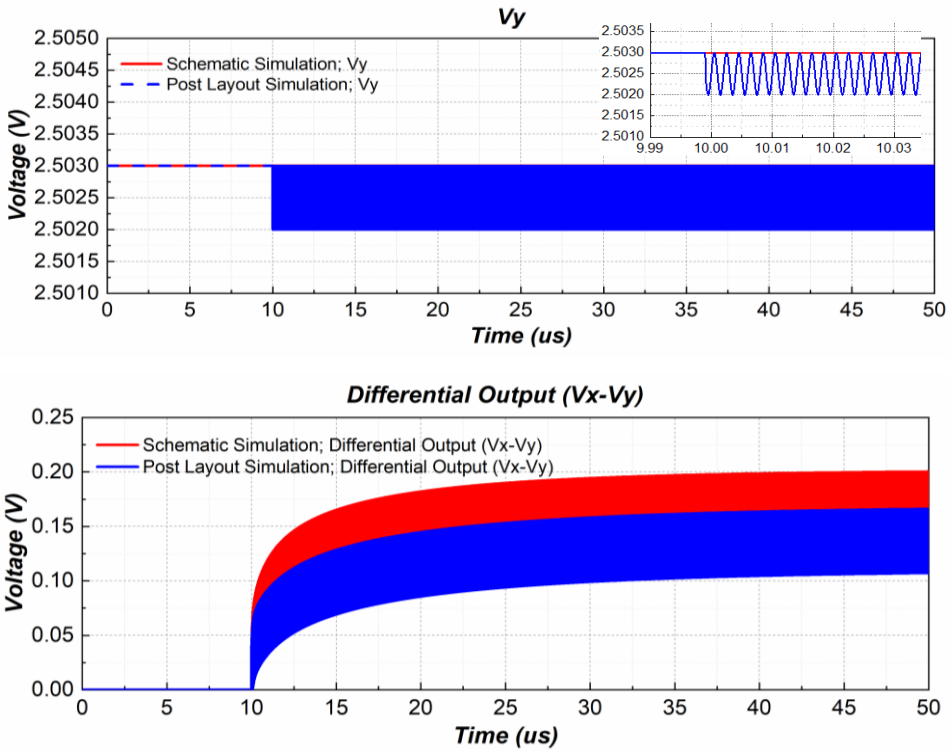

Figure 32: Shows the transient response of the Peak Detector integrated with the Source Follower.

The small, consistent oscillations observed at the output of the peak detector during the charging phase, likely stemming from the component characteristics and parasitic components of the circuit, will be filtered using an Instrumentation Amplifier during the full system simulation presented in Section 5.8.

5.5.3 Analogue CMOS Switch

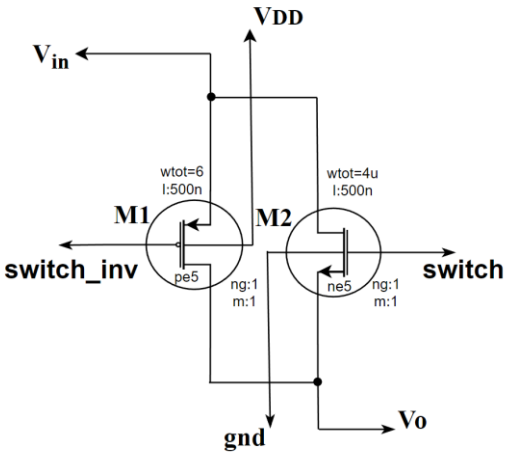

Figure 33: Shows the schematic of the Analog CMOS Switch.

Analog CMOS switches minimize power consumption with low resistance and minimal leakage currents in their respective on and off states. Using a complementary pair of NMOS

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and PMOS transistors, these switches ensure high isolation in the off-state. CMOS technology's design flexibility allows for a wide range of operating voltages while maintaining high signal transmission linearity.

These specifications collectively position CMOS switches as an ideal choice for our application, specifically, for switching sub-channels within each channel and resetting capacitors in the peak detector through a similar CMOS switching mechanism. An analogue CMOS switch is designed using two transistors (NMOS and PMOS) operating in unison to establish a bidirectional switch. When activated, it effectively conducts both analogue and digital signals in both directions, while isolating the input and output when turned off.

Figure 33 (layout in Figure 231) shows the analogue CMOS switch featuring NMOS M2 and PMOS M1 transistors. The switch is in the 'on' state when the gate voltage of the M2 transistor is high (5V) and that of the M1 transistor is low (≈0V), allowing the signal to pass through. Conversely, the switch is in the 'off' state when the gate voltage of the M2 transistor is low and that of the M1 transistor is high. This state effectively blocks the signal from passing through [45]. The layout of the analogue CMOS switch is also illustrated in Figure 33.

5.5.4 OPAMP

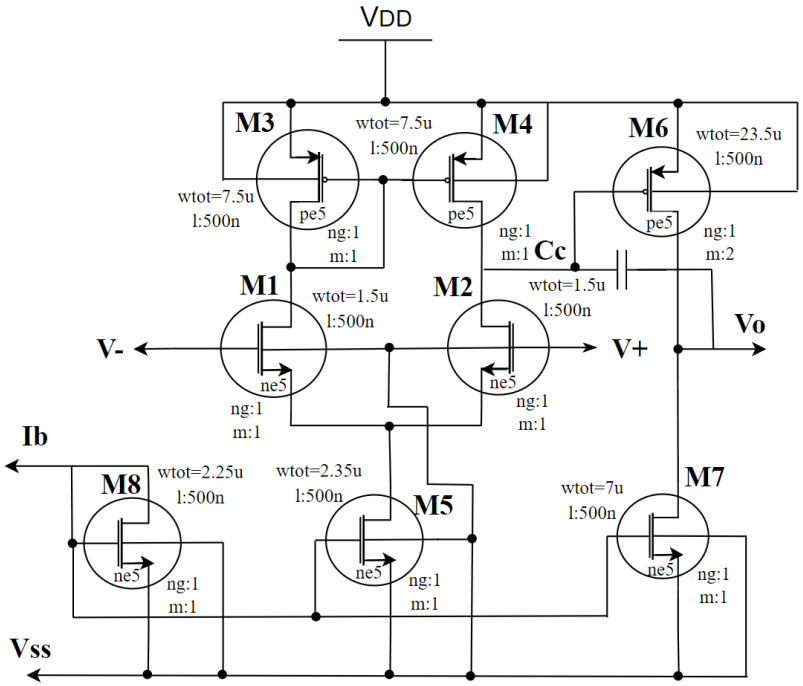

Figure 34: Shows the Two-stage OPAMP schematic design.

The instrumentation amplifier (IA) is designed using Op Amps. This section discusses Op Amp design utilizing the two-stage circuit architecture technique from [45], [47], as illustrated in Figure 34. The two-staged Op Amp has a differential input that provides a single-ended output swing. This is achieved through the utilization of a current mirror to

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generate a single-ended output while maintaining the differential nature of the first stage. The first stage also possesses amplification capabilities for the input signal, and the second stage further amplifies the signal to provide the single-ended output signal.

The compensation capacitor in the feedback path of the Op Amp helps ensure stability and prevent oscillations. This capacitor, often referred to as a Miller capacitor, is connected between the output stage and the input stage.

Figure 34 (layout in Figure 231) illustrates a two-stage CMOS Op Amp with an n-channel input pair of MOSFETs, M1 and M2, forming the differential amplifier stage. A current source (M3 and M4) is employed as an active load, enabling higher gain. MOSFET M6 serves as the common-source second stage. The capacitor, situated between the Cc terminal and the output is the compensation capacitor. The circuit is biased using an external resistor to control Ib, and the current mirror transistors, M5, M8, and M7, play a role in this biasing.

5.5.5 Instrumentation Amplifier

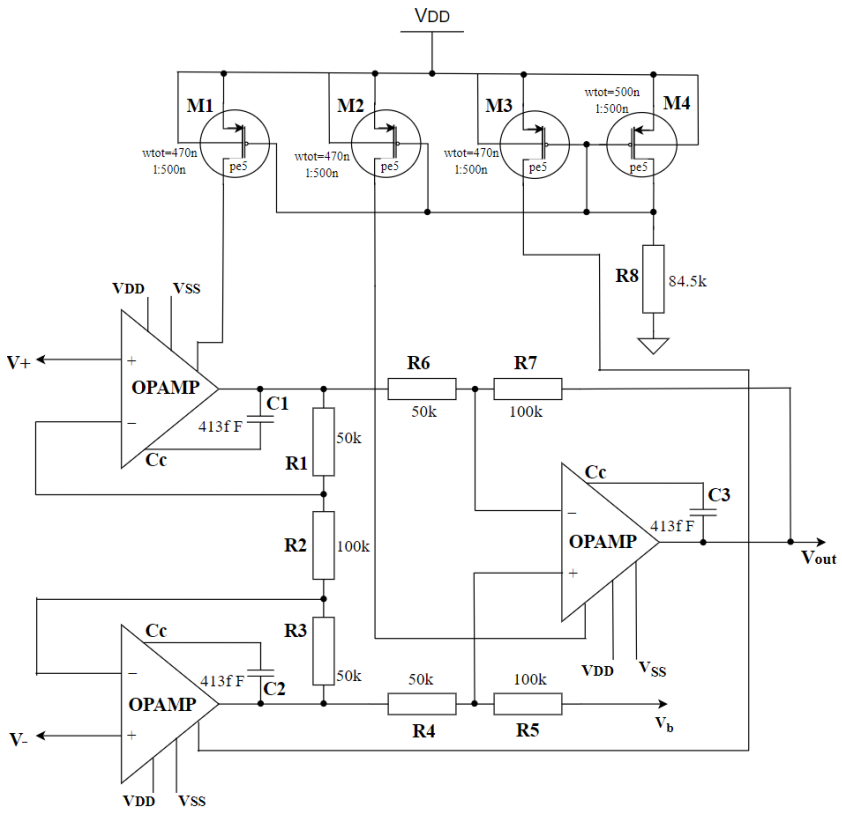

Figure 35: Shows the Instrumentation Amplifier designed using three two-stage OPAMPs.

The Instrumentation Amplifier (IA) is constructed using two-stage Op Amps, as shown in Figure 34. It incorporates three Op Amps, with two functioning as input buffer amplifiers and the third serving as a differential amplifier. The IA offers several advantages, including differential amplification, high accuracy, high gain, high common mode rejection ratio

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(CMRR), and high input impedance [48]. The CMRR feature is crucial as it assesses the amplifier's ability to suppress common mode signals that are identical and in phase on both input terminals.

The gain of the IA is expressed as [48],

$$A_v = \frac{V_{out}}{V_- - V_+} = \left(1 + \frac{2R_1}{R_2}\right)\frac{R_7}{R_6} \tag{43}$$

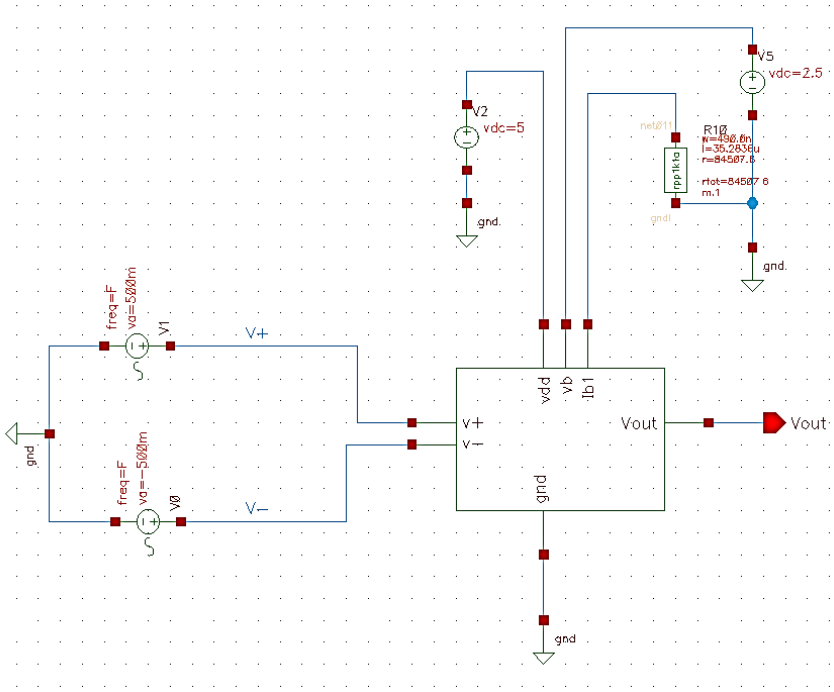

Figure 36: Shows the simulation test bench for the Instrumentation Amplifier

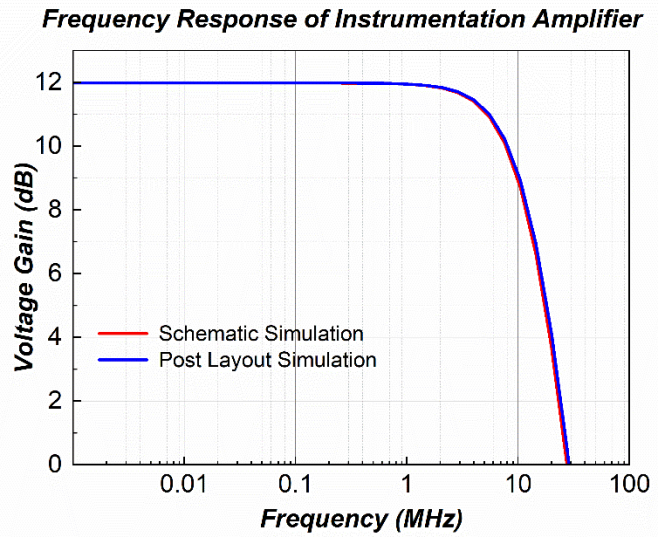

Figure 37: The frequency response of the Instrumentation Amplifier, operating at a gain of 4 (12 dB), is illustrated. The graph depicts both schematic (red) and post-layout (blue) simulations.

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The schematic of the IA is presented in Figure 35. The Op Amp connected to V_{out} functions as a differential amplifier, with a gain determined by R_7/R_6 and a differential input resistance of $2R_6$. The Op Amps connected to inputs V_+ and V_- serve as buffer Op Amps. The inclusion of a resistor R_2 between the inverting inputs increases the differential mode gain of the buffers while maintaining a common mode gain of unity. External bias currents for the Op Amps are mirrored using the current mirror configuration involving transistors M1, M2, M3, and M4. The gain of the IA is controlled by the resistors placed between the Op Amps. Additionally, capacitors C_1, C_2, and C_3 serve as compensation capacitors for their respective Op Amps.

The layout of the IA, as shown in Figure 232 from Appendix 11.9, and the associated simulation test bench setup shown in Figure 36, are also presented. Both the schematic and post-layout simulations demonstrate close agreement.

5.5.6 A 3 to 8 Line Decoder

A 3-to-8 line decoder, also known as a 3-to-8 line selector, is implemented using eight four-input NAND gates, as illustrated in Figure 38. To obtain both high and low outputs, inverters are also employed at the output of the decoder. The decoder operates in a manner that only one of the output lines is active at any given time, depending on the input combination provided. This allows for efficient selection and control of the circuit based on the specified input combination. The decoder features three inputs (A, B, C) and an Enable (E) signal, along with eight outputs (D0 to D7 & H0 to H7). Each output in D0 to D7 is activated for every 3-bit binary input value ranging from 0 to 7. The layout of the 3-to-8-line decoder is also presented in Figure 233 from Appendix 11.9.

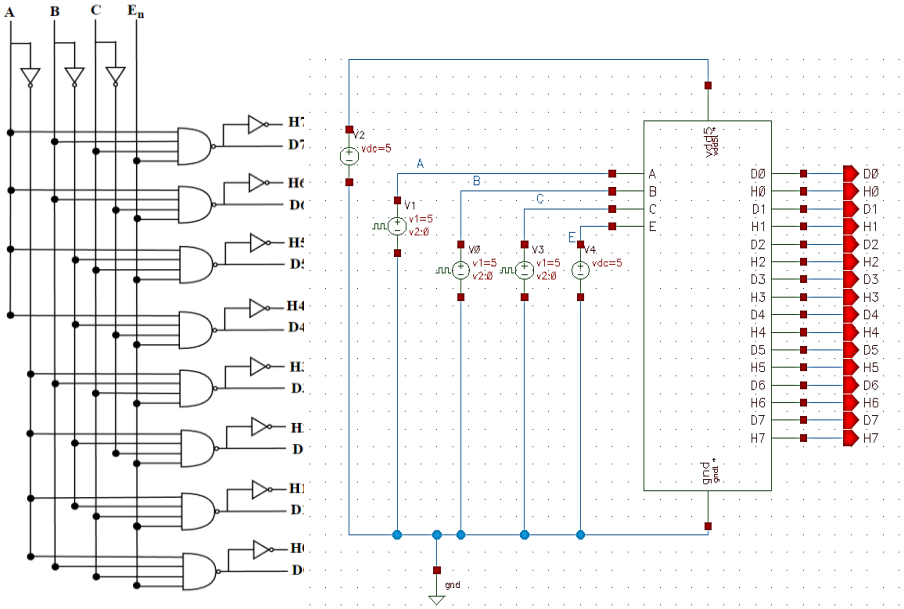

Figure 38: Left figure shows the 3-8 line decoder schematic and the right figure shows the simulation test bench for a 3-8 line decoder.

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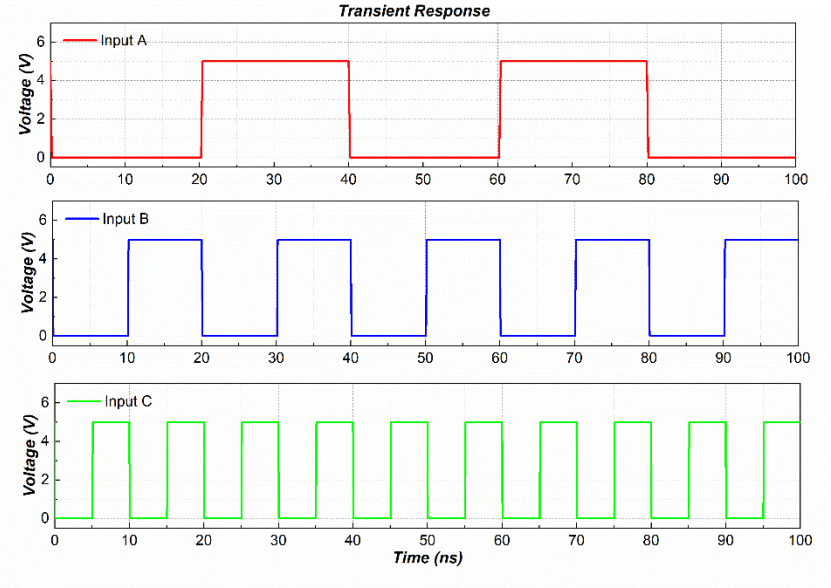

Figure 39: Shows the Input of the 3 to 8 Line Decoder

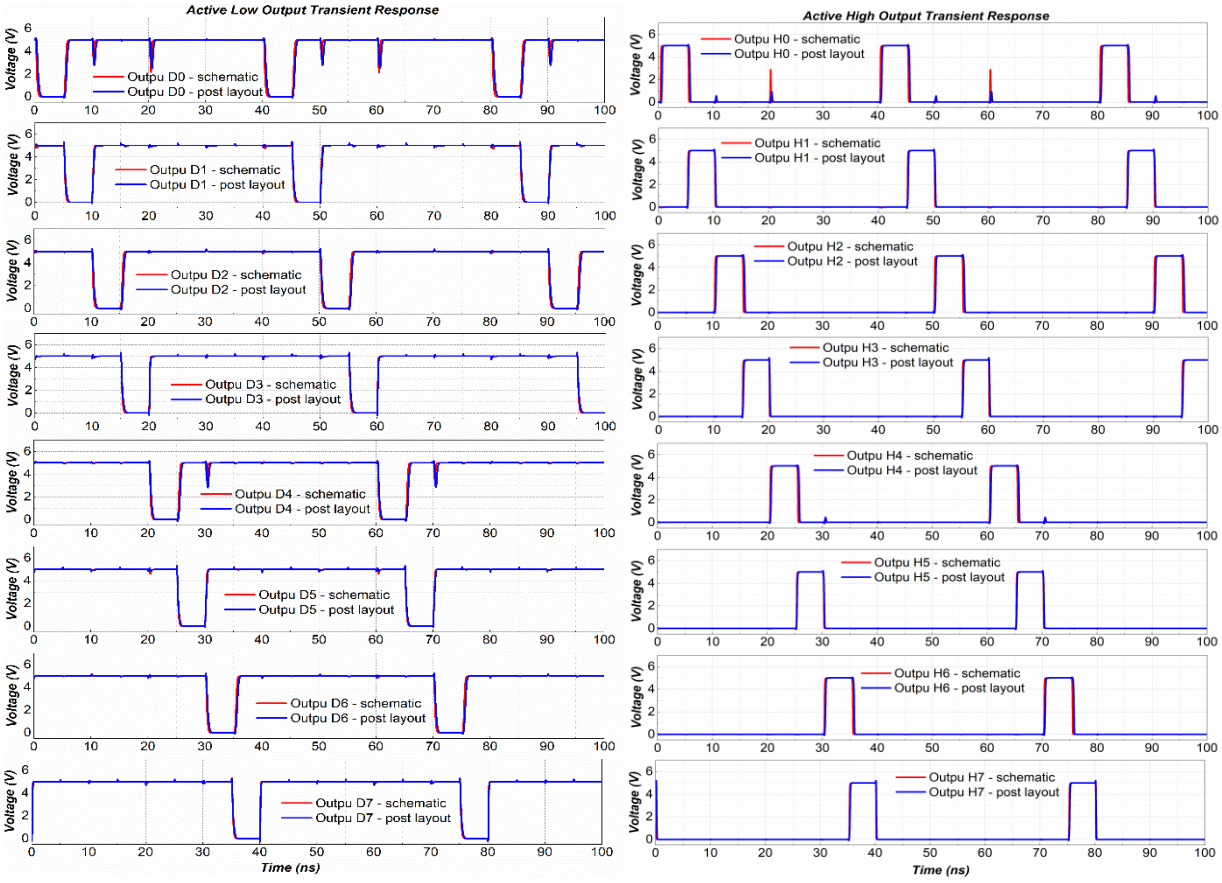

Figure 40: The left figure shows the active low output of the 3 to 8 Line Decoder and the right figure shows the active high output of the 3 to 8 Line Decoder. The figure also shows both schematic (red) and post-layout (blue) simulation

The simulation test bench used for verification is shown in Figure 38. Various input combinations are applied with different pulse widths to ensure that all the output

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combinations are activated within 50 ns, as demonstrated in Figure 39 and Figure 40. Both schematic and post-layout simulations are included in the figures, although there is no visual distinction between them since block-level simulations are employed.

5.6 Integration of all Sub-Channels of Channels 1 and 2

The minimum voltage required for the peak detector to effectively detect the signal is 140mV peak-to-peak (p-p). Therefore, to detect signals with lower amplitudes, an amplifier is necessary prior to the peak detector stage. This is where our high-gain RF amplifier and broadband RF amplifier come into play, as they are positioned before the peak detector stage. To safeguard the gain bandwidth of the RF amplifier, a source follower is employed between the peak detector and the RF amplifier. Each of these configurations offers varying levels of sensitivity, resulting in different detection capabilities across the sub-channels.

The RF IC detector block diagram, as shown in Figure 21, integrates all the blocks from Section 5.5 to create channel 1 and channel 2. The peak detector is connected to the IA through channel switches, which are further illustrated in the subsequent figures within this section.

The switching of channels is accomplished using analogue CMOS switches controlled by a 3-to-8-line decoder. Sub-channels 0, 1, 2, and 3 (SC0, SC1, SC2, SC3) of channels 1 and 2 (C1 and C2) are respectively connected to the same output pins of the decoder for simultaneous operation. However, channels 1 and 2 have distinct outputs connected through different IA configurations.

5.6.1 Sub-Channel 0 (SC0)

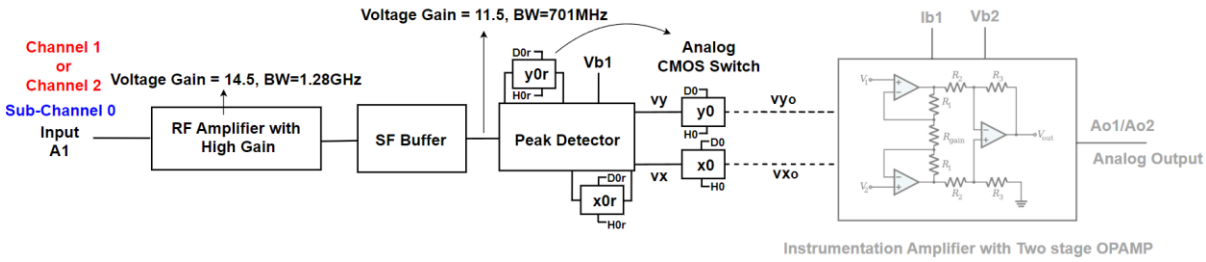

Figure 41: Shows the sub-channel 0 of channels 1 and 2 (C1SC0 and C2SC0).

The Sub-channels 0 of channels 1 and 2 (C1SC0 and C2SC0) incorporate a high-gain RF amplifier block, which serves to amplify incoming RF signals and enhance the detector's sensitivity to EM fields. This amplification is beneficial when dealing with weak EM fields originating from distant or low-power sources. However, integrating the RF amplifier block with other components results in a slight reduction in the bandwidth of the amplifier by a few megahertz. It is important to note that SC0 has a frequency limitation and can operate

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within the linear region only up to 0.7 GHz. Beyond this frequency, the amplifier no longer functions within the linear region.

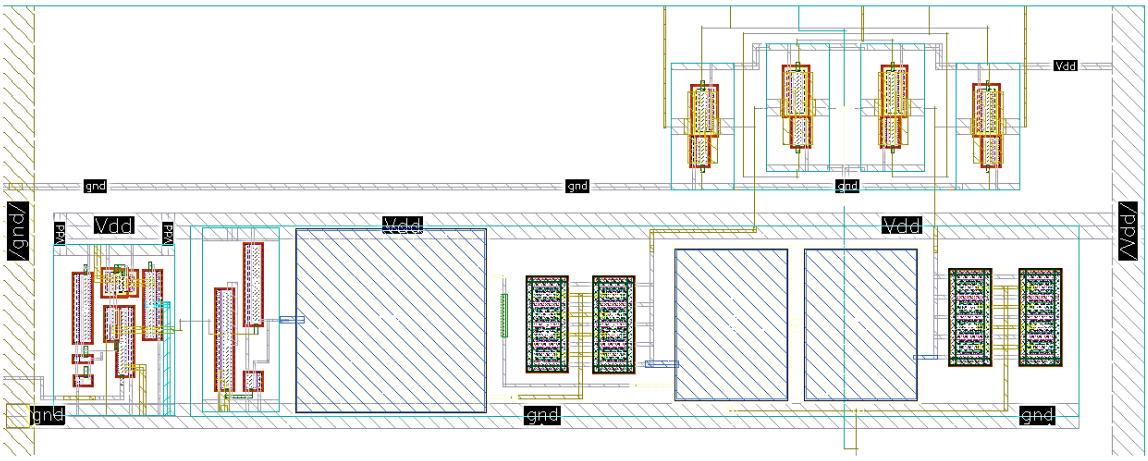

Figure 42: Shows the layout design of the highlighted blocks from Figure 41. This layout doesn't include IA because it is common for all subchannels.

The IA is shared among all sub-channels of channels 1 and 2, meaning that it is utilized by each sub-channel. Therefore, in the provided figure, the IA amplifier is not highlighted. Only the activated sub-channel will be connected to the IA.

5.6.2 Sub-Channel 1 (SC1)

Sub-channels 1 of channels 1 and 2 (C1SC1 and C2SC1) are equipped with a broadband RF amplifier, which assists the detector in operating within a slightly higher frequency range while experiencing reduced sensitivity. However, when integrating the RF amplifier block with other components, the overall bandwidth of the amplifier diminishes by a few megahertz. It is worth noting that SC1 is restricted in terms of frequency range, as it can only operate within the linear region up to 1.5 GHz. Beyond this threshold, the amplifier ceases to function within the linear region.

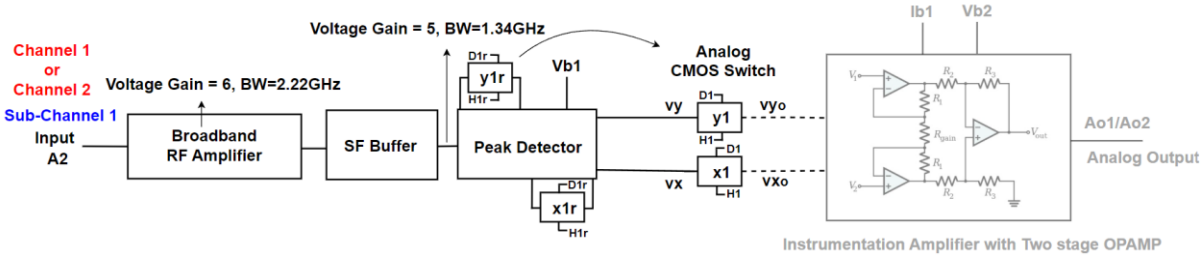

Figure 43: Shows the sub-channel 1 of channels 1 and 2 (C1SC1 and C2SC1).

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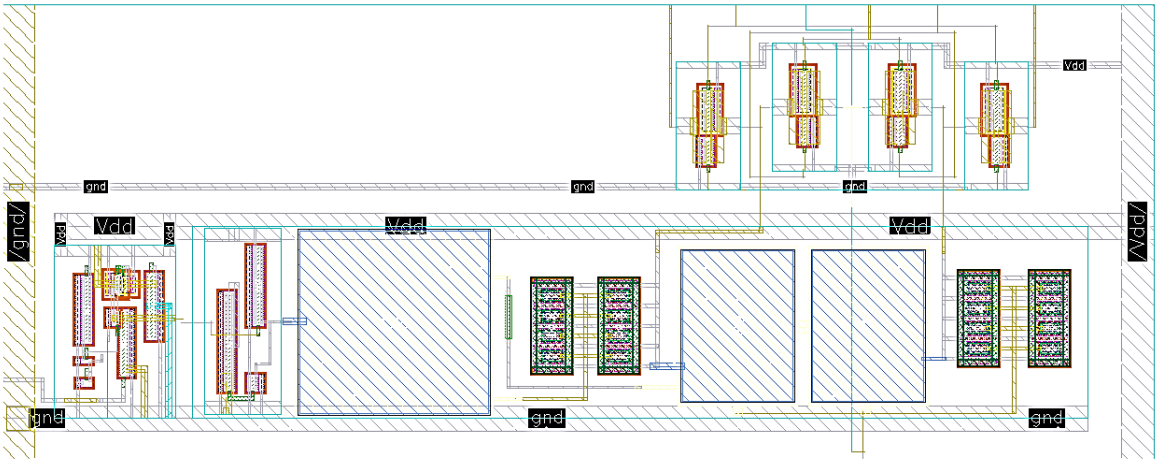

Figure 44: Shows the layout design of the highlighted blocks from Figure 43. This layout doesn't include IA because it is common for all subchannels.

5.6.3 Sub-Channel 2 and Sub-Channel 3 (SC2 and SC3)

Sub-channels 2 of channels 1 and 2 (C1SC2 and C2SC2) are distinct in that they do not incorporate any amplification stages. Instead, the input signal is directly routed to the peak detector. Conversely, sub-channels 3 of channels 1 and 2 (C1SC3 and C2SC3) directly connect the input signal to the IA. During operation at higher frequencies, typically exceeding 1.5 GHz, SC2 plays a significant role. However, it is important to note that this sub-channel exhibits lower sensitivity in comparison to SC0 and SC1. In other words, SC2 necessitates a higher power level at the input to detect the signal, contrasting with the lower power requirements of SC0 and SC1. Since the IA is common to both channels 1 and 2 (C1 and C2), SC3 is designed to feed the signal directly to the IA, facilitating an understanding of the behaviour and limitations of the OPAMPs of the IA.

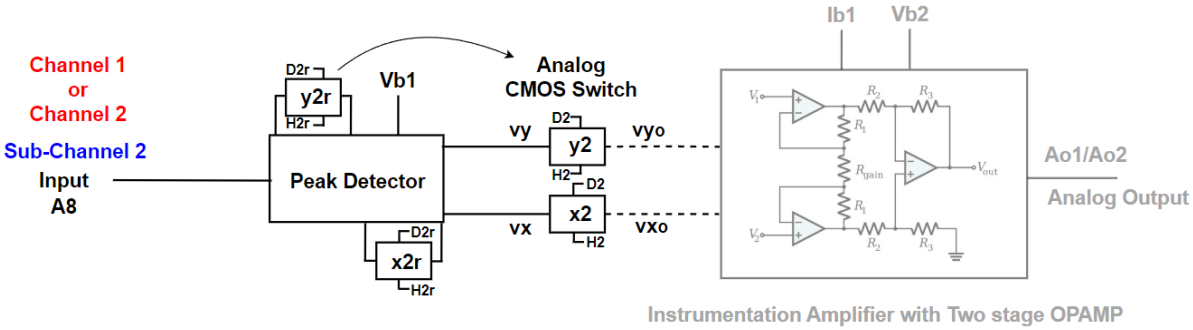

Figure 45: Shows the sub-channel 2 of channels 1 and 2 (C1SC2 and C2SC2).

The SC3 exclusively consists of channel selection analogue CMOS switches, as shown in Figure 47. This configuration is due to the direct connection of the input signal to the IA. The objective of SC3 is to thoroughly examine the behaviour and performance of the op-amps employed within the IA, as it is crucial for accurate signal processing.

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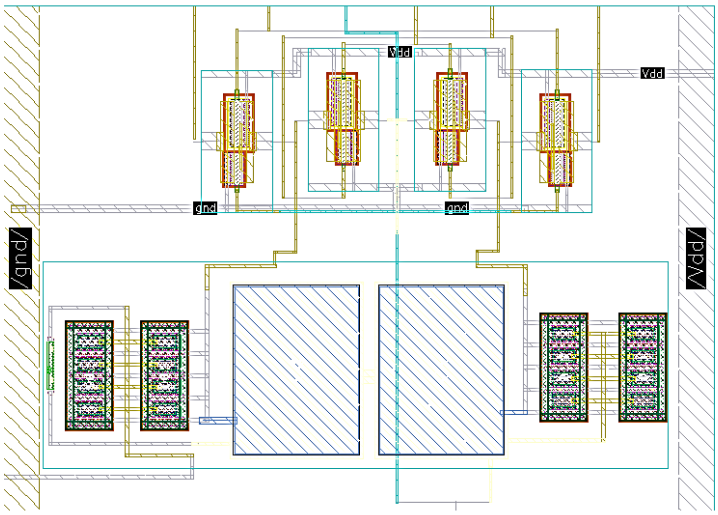

Figure 46: Shows the layout design of the highlighted blocks from Figure 45. This layout doesn't include IA because it is common for all subchannels.

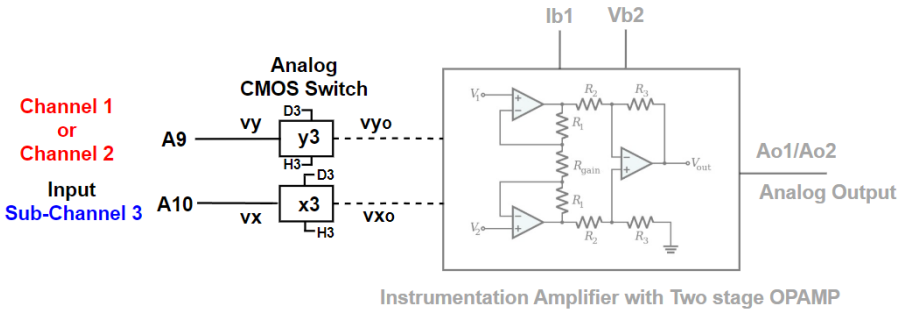

Figure 47: Shows the sub-channel 3 of channels 1 and 2 (C1SC3 and C2SC3).

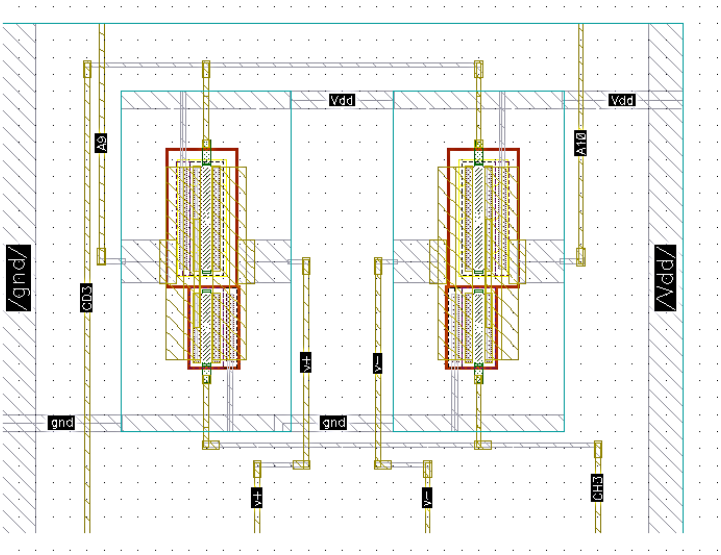

Figure 48: Shows the layout design of the highlighted blocks from Figure 47. This layout doesn't include IA because it is common for all subchannels.

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Op-amps possess specific bandwidth limitations, with their gain diminishing as the frequency increases. It is crucial to assess the slew rate, settling time, and distortion characteristics of the op-amps, as these parameters directly impact the overall performance of the IA, especially at higher frequencies. By investigating these aspects, an understanding of the IA's behaviour and its suitability for high-frequency applications can be gained.

5.7 Full Layout of RF IC Detector

Floor planning is a crucial step in the design process of an IC that involves arranging and placing various circuit blocks, components, and modules on the surface of the chip. In Figure 49, the floor planning of the RF IC detector is shown. The design incorporates ten analogue input pins labelled A1 to A10, which correspond to sub-channels 0 to 3 of channels 1 and 2. Among these pins, six are single-ended inputs, while two are designated as differential input pins, strategically positioned in suitable locations.

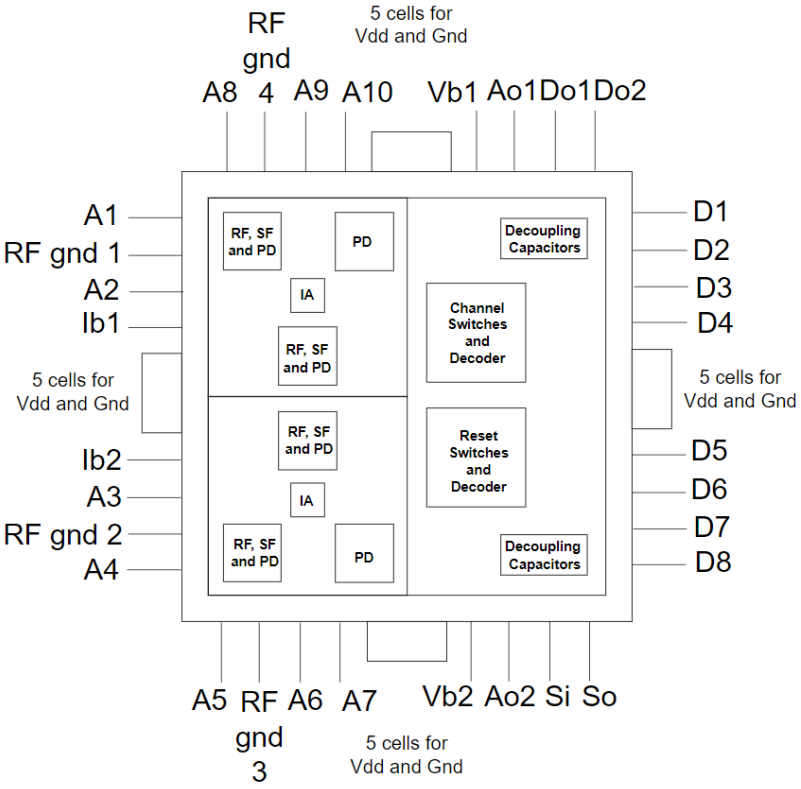

Figure 49: Shows the Floor Plan of the RF IC Detector

To maintain symmetry, channel 1 is positioned at the top left corner, while channel 2 is located at the bottom left corner. The floor plan also includes eight digital inputs labelled D1 to D8, serving the purpose of reset and channel decoding. Consequently, two 3 to 8-line decoders are placed towards the right side of the layout. Additionally, the design incorporates two analogue outputs (Ao1 & Ao2), two bias voltage pins (Vb1 & Vb2), two

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current bias pins (Ib1 & Ib2), and separate sets of RF grounds dedicated to channels 1 and 2. Furthermore, the floor plan includes several test pins for specific purposes. This includes the Si and So pins for testing the test switch, and the Do1 and Do2 pins used to test the decoder output.

In Chapter 4 of our research work, we observed that improved grounding leads to an increase in the resonant frequency. As a result, having more GND pins around the IC package offers a broader transmission band for signal pins. Based on this understanding, we strategically positioned four sets of power pins around the IC package pin, as illustrated in the floor plan shown in Figure 49. This placement ensures better grounding and contributes to achieving a wider transmission band for the signal pins.

5.7.1 Design of PAD Ring

To establish the connection between the IC die and the package pins, a pad ring is essential. The pad ring serves as a platform for bonding pads, ESD protection circuits, and IO buffers for digital circuits. Each side of the pad ring consists of 13 I/O cells, with five of them allocated for power supply and ground connections (VDD5, VDDR, VDDO, GNDO, and GNDR) on each side. This configuration results in a total of 52 I/O cells, equivalent to a standard 52-card deck, with 13 cells on each side. The pad ring measures 1.52 mm x 1.52 mm, and each I/O cell adheres to a standard size of 85 µm.

To facilitate clear differentiation between the sides, we have assigned the names Diamond for the left side, Club for the right side, Spade for the top side, and Heart for the bottom side, as shown in Figure 50 and Figure 51. The layout of the final pad ring is illustrated in Figure 52.

5.7.1.1 Types of pads used in the design

We selected the single supply voltage category I/O cells from the XT018 digital I/O libraries [49] for our design. These I/O cells are designed to operate at a core voltage of 5V, which aligns with the I/O cell voltage requirements. In particular, we utilized the IO_CELLS_FC5V I/O library from this category, which is specifically designed to meet our design specifications.

a) Power Supply Rails

Based on the design requirements, we have the flexibility to configure the use of separate supplies available in the library. In our specific design, we have employed four sets of power supply I/O cells located on all four sides of the PAD ring, as shown in Figure 49. These power supply I/O cells establish connections between adjacent I/O cells, forming a continuous power rail around the PAD ring. The library provides three main categories of supply rails for our utilization. Firstly, we have VDDO and GNDO, which serve as the primary I/O supply rails for output drivers and ESD protection elements. Secondly, we

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have VDDR and GNDR, which are intermediate buffer I/O cells that offer improved noise immunity. Lastly, we have VDD5, which functions as the core supply rail.

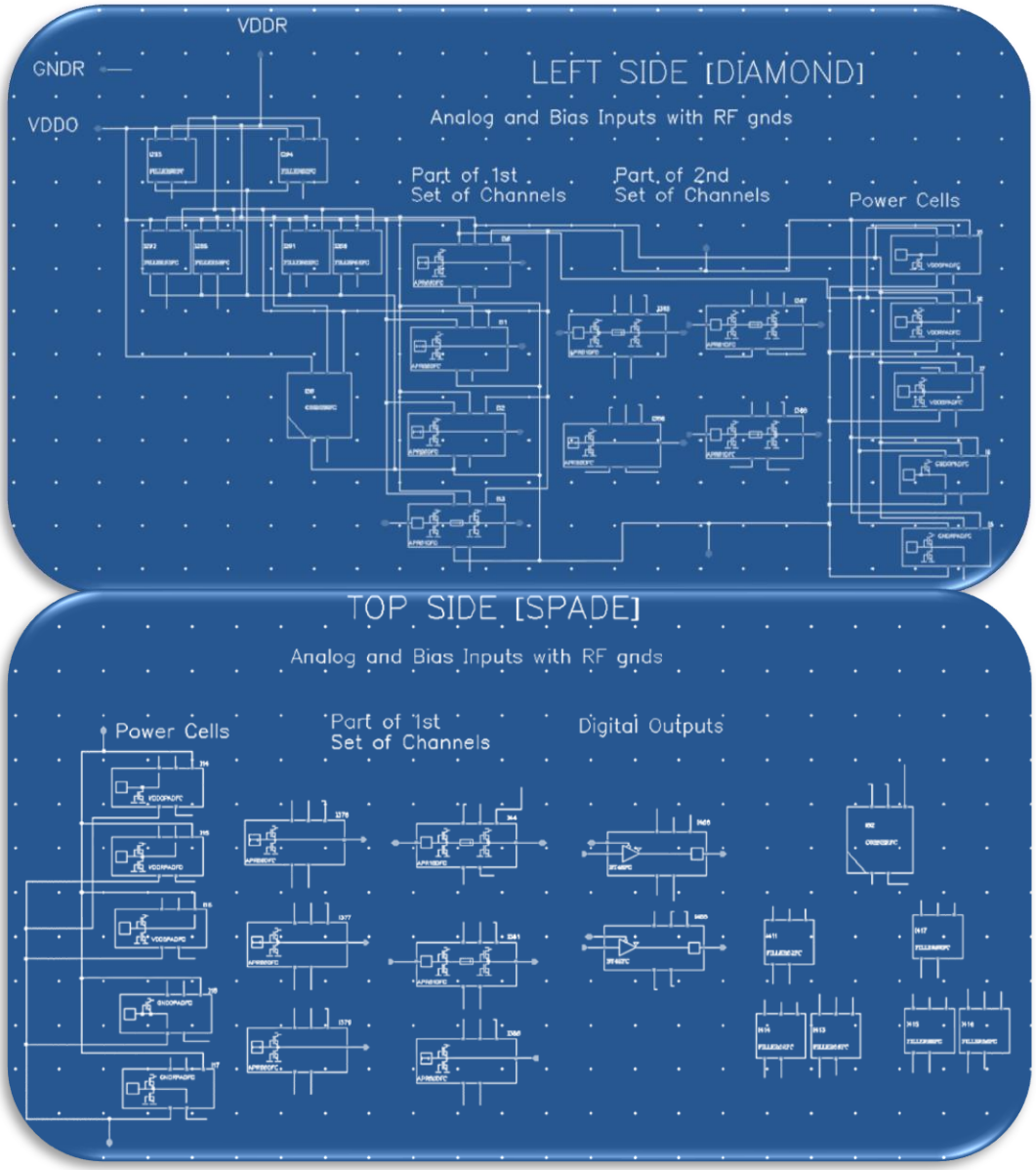

Figure 50: Show the schematic of I/O cells on the Diamond and Spade sides.

a) Analogue I/O cells

The selected library provides a variety of analogue I/O cells, each offering different ESD protection structures with varying input series resistance. In our design, we have employed specific analogue I/O cells to cater to the requirements of different channels. For channel 1 inputs, a 5V analogue I/O cell with low series resistance (<1Ω) has been utilized. Channel 2 inputs, on the other hand, utilize a 5V analogue I/O cell with a series resistance of 100Ω. As for the analogue outputs Ao1 and Ao2, a 5V analogue I/O cell with a 1kΩ series

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resistance has been employed. It is noteworthy that all three analogue pads used in our design feature ESD protection structures for both supply and ground connections.

Channel 1 inputs utilize a low series resistance (<1Ω) analogue I/O cell for high-frequency signal performance, emphasizing low series resistance to minimize parasitic effects and ensure signal integrity in low-noise environments. Channel 2 inputs employ a 100Ω analogue I/O cell, achieving a balance between power consumption and signal integrity. The 100Ω series resistance provides adequate matching without compromising efficiency. Analogue Outputs (Ao1 and Ao2) feature an 1kΩ analogue I/O cell, optimizing for diverse loads and minimizing power dissipation when driving high-impedance loads.

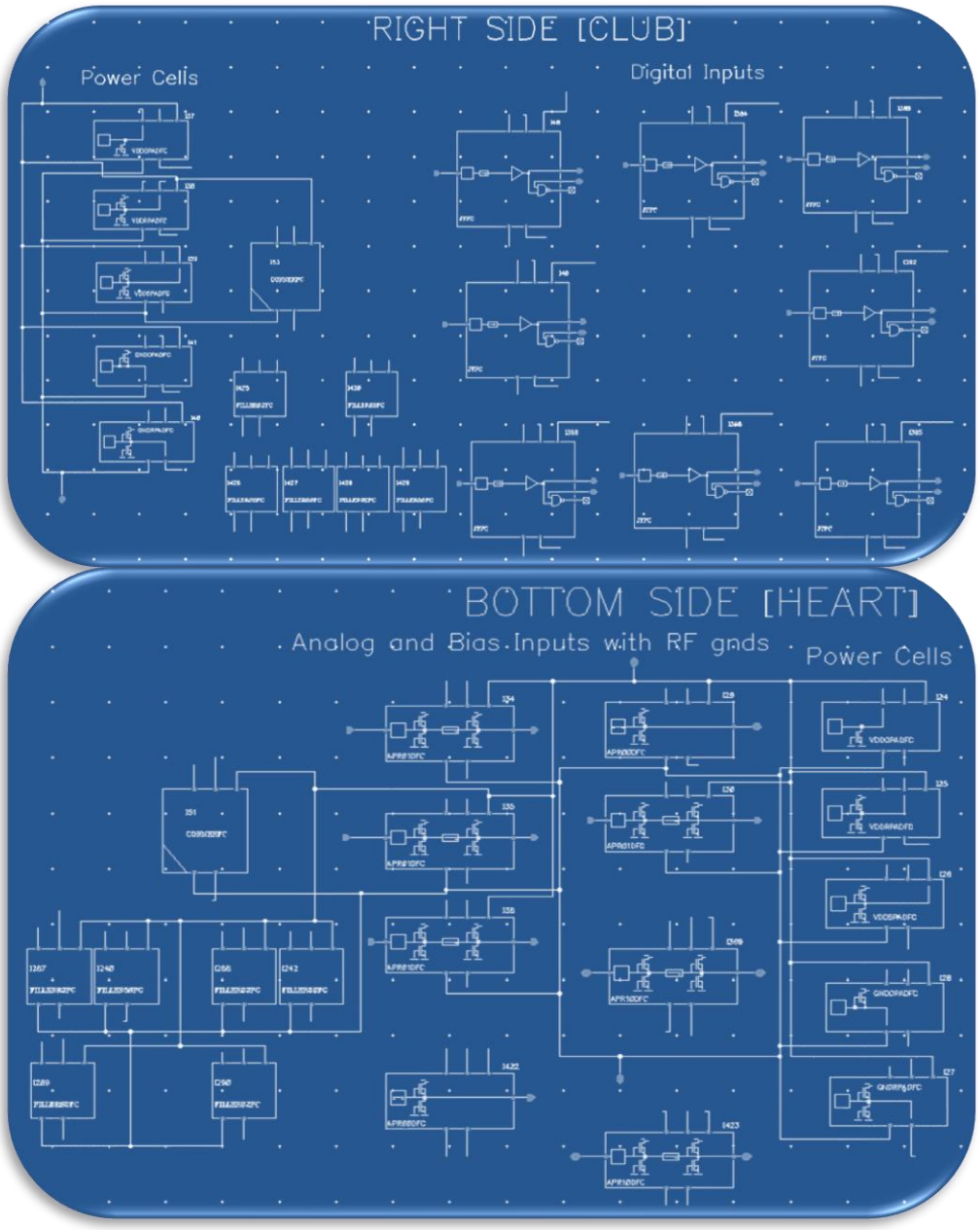

Figure 51: Show the schematic of I/O cells on the Club and Heart side.

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b) Digital I/O cells

The digital I/O cells within the chosen library provide a range of input options, including Schmitt trigger input, input hold or gated input, gated pull-up, and pull-down. In our design, we have opted for the digital I/O cell featuring a non-inverting transistor-transistor logic (TTL) input buffer with Pi-type ESD protection.

c) Corner I/O cells

The corner I/O cells utilized in our case solely consist of power rails, facilitating connections between adjacent I/O cells. These corner cells are available in various sizes, ranging from 2 mm x 2 mm to 10 mm x 10 mm. In our design, as shown in Figure 52, we have incorporated four corner I/O cells, each measuring 2 mm x 2 mm in size.

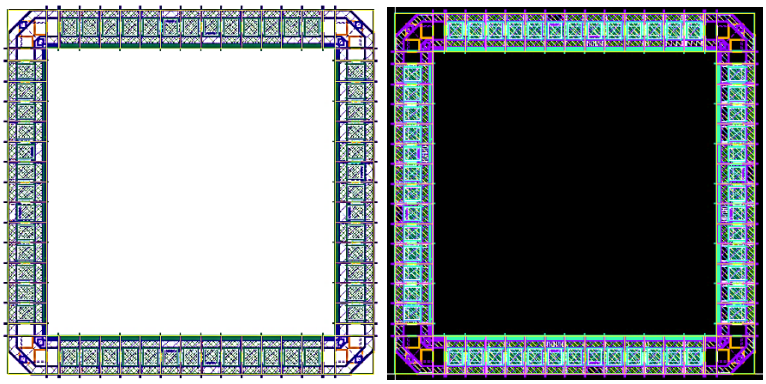

Figure 52: Shows the PAD ring with all the I/O pads connected to one another with white and black backgrounds.

a) Filler I/O cells

The purpose of filler cells, as their name implies, is to occupy empty spaces between I/O cells or to provide necessary spacing between them. These cells come in various sizes, ranging from 1 µm to 100 µm. In Figure 52, it can be observed that we have employed filler cells near the corner cells to bridge the gaps between the corner cell and other I/O cells. Specifically, to cover the 54 µm gap on each side of the corner cell, we have placed one 50 µm filler cell and two 2 µm filler cells on each side.

5.7.2 Incorporating all Sub-channels layouts into PAD Ring

All the sub-channel blocks from Section 5.6, two IA from Section 5.5.5 and two 3-8 line decoders from Section 5.5.6 are incorporated inside the PAD ring. Channel 1 is positioned at the top left corner, while channel 2 is located at the bottom left corner, ensuring a symmetrical arrangement as shown in Figure 53. Additionally, towards the right-hand side, eight digital inputs (D1 to D8) are incorporated for reset and channel decoding purposes. Consequently, two 3-to-8-line decoders are positioned to the right.

To increase the capacitance between the power supply and ground, decoupling capacitors are added to the unused chip space inside the PAD ring. These decoupling

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capacitors will help to suppress the high-frequency noise in power supply rails. At high frequencies, these capacitors will bypass the power supply providing a low impedance path between power and ground and also reduces the power rail coupling between the circuits fed from the power supply. Basically, these decoupling capacitors will behave as noise filters and serve as low-pass filters by attenuating high-frequency noise and preventing the noise from reaching susceptible circuit blocks.

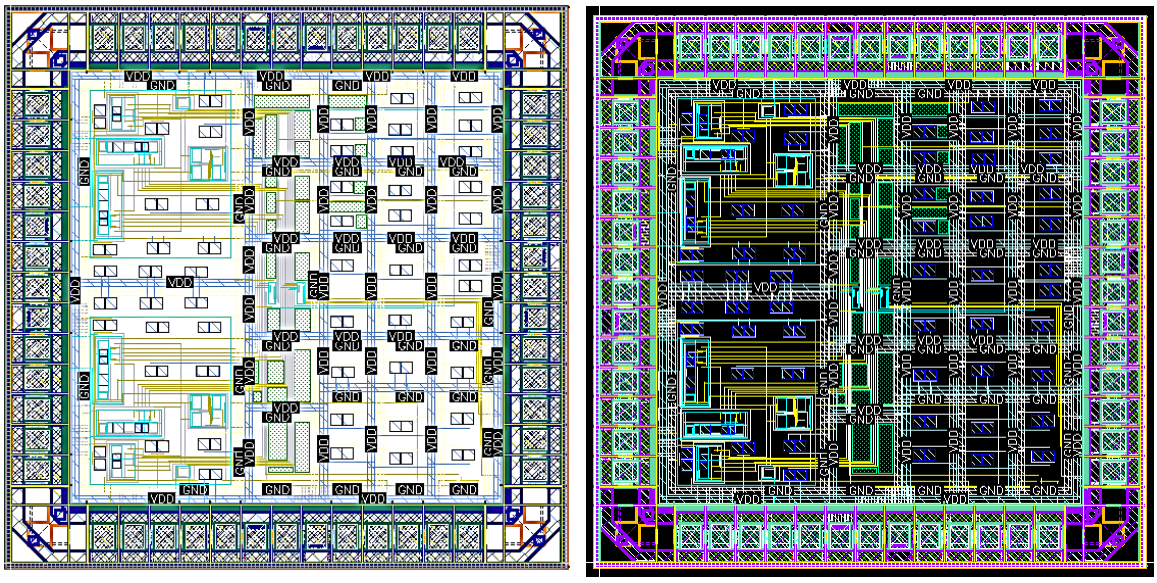

Figure 53: Shows the full RF IC detector layout with PAD Ring and Seal Ring in white and background.

We can observe VDD and GND tracks all around the PAD ring as shown in Figure 53, this is the power gridding technique that we are employing to reduce the supply rail impedance. The longer the distance between the power supply and the decoupling capacitor higher the noise. This makes the design a stable power distribution network within the RF IC by improving the overall performance and signal integrity of the RF IC Detector.

5.7.2.1 Incorporating Seal Ring into the Full Layout

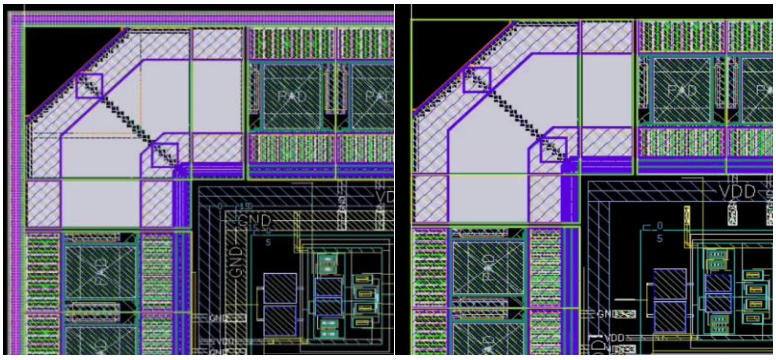

Figure 54: Shows the left top corner of the PAD ring with seal ring and without seal ring.

The seal ring forms a protective shielding around the PAD ring ensuring the integrity and reliability of the design, hence seal ring is also called a guard ring. Basically, the seal

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ring behaves as the physical barrier around the PAD ring to contain the active area of the IC. In other words, it helps to protect the active circuit area from external factors such as EMI, ESD and contaminants. It also helps to define the outermost boundary of the overall IC design and will become the reference point for lithography and alignment processes during the fabrication of the wafers.

We have incorporated the seal ring around the PAD ring as shown in Figure 54. The figure shows the zoomed-in area of the left top corner of the PAD ring.

5.8 Full RF IC Detector Simulation and Results

In this section, a comprehensive simulation of the RF IC detector schematic is conducted, followed by post-layout simulations. The primary focus of the discussion is to analyse the results obtained from simulating each sub-channel individually. This analysis aims to provide a deeper understanding of the performance and behaviour of each sub-channel within the RF IC detector.

5.8.1 Sub-Channel 0 Simulation (C1SC0 and C2SC0)

Figure 55 illustrates the active blocks that are engaged when sub-channel 0 of channel 1 and channel 2 (C1SC0 and C2SC0) are selected. To activate SC0, a binary input of 000 is applied to the 3-to-8 channel selecting line decoder. This action triggers the activation of the channel CMOS switches, subsequently activating C1SC0 and C2SC0.

In Figure 56, the input signal is introduced after a 2us delay. The amplified signal is then fed into the peak detector input, initiating the charging process from 2us to 10us. At the 10us mark, the reset switch is triggered to discharge the capacitors within the peak detector. Consequently, no signal detection occurs beyond the 10us threshold. The reset CMOS switches are activated from 10us to 11us, represented by a green curve, utilizing the 3-to-8 reset line decoder.

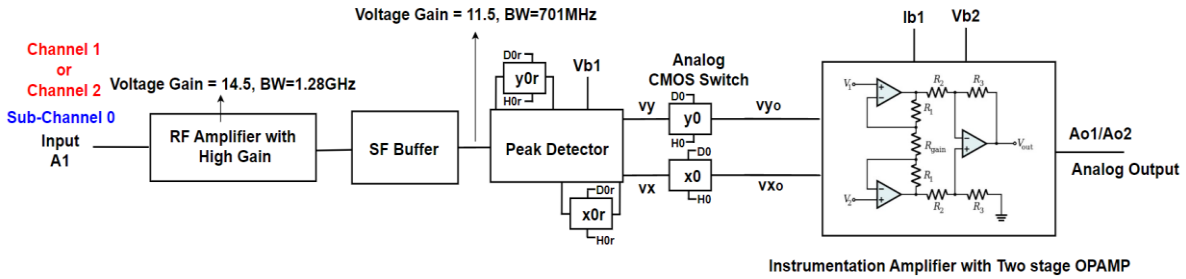

Figure 55: Shows the active blocks when sub-channel 0 is selected by the decoder based on the user input.

The schematic simulation output results, represented by the red and lime curves, refer to the simulation performed using the circuit schematic or idealized representation of the

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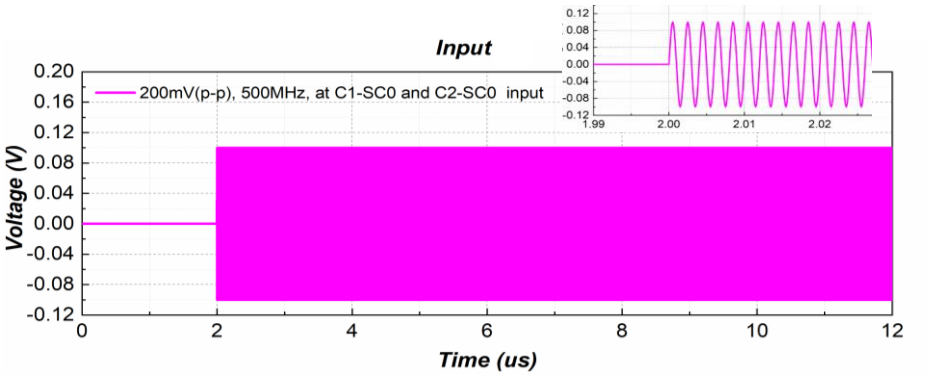
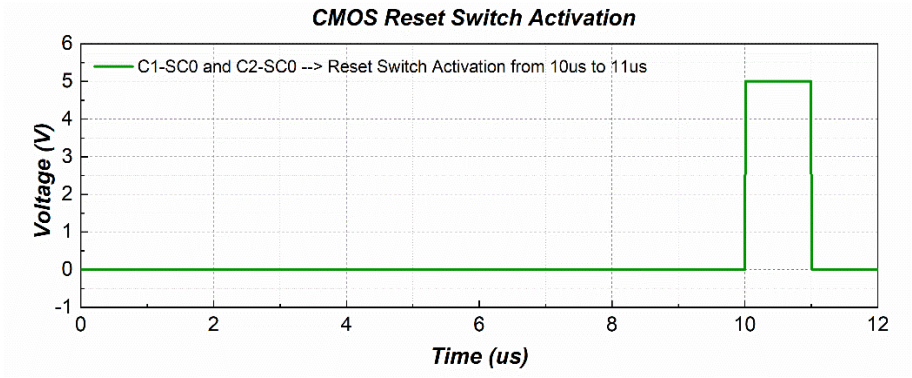
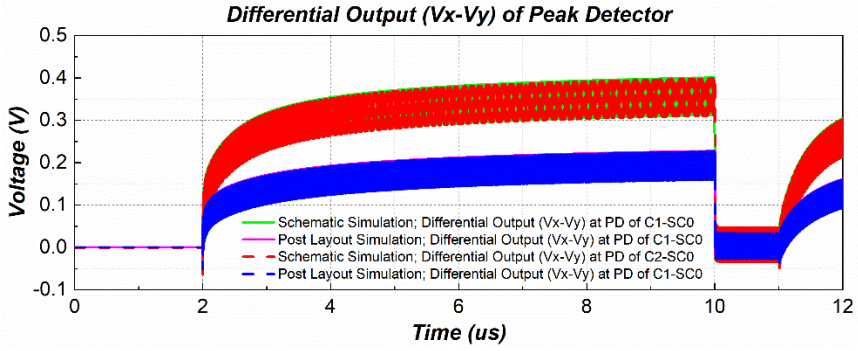
circuit. This simulation assumes ideal component behaviour without considering any parasitic effects that might occur in the physical implementation. On the other hand, the post-layout simulation output results, depicted by the blue and pink curves, involve simulating the circuit after incorporating the layout information and considering the effects of parasitic elements such as resistances (R) and capacitances (C) that exist in the physical implementation.

When RC parasitic effects are taken into account in the post-layout simulation, some differences between the schematic and post-layout simulation curves become evident. These differences arise due to the influence of the parasitic elements, which can introduce additional resistance and capacitance to the circuit, altering its behaviour compared to the idealized schematic simulation.







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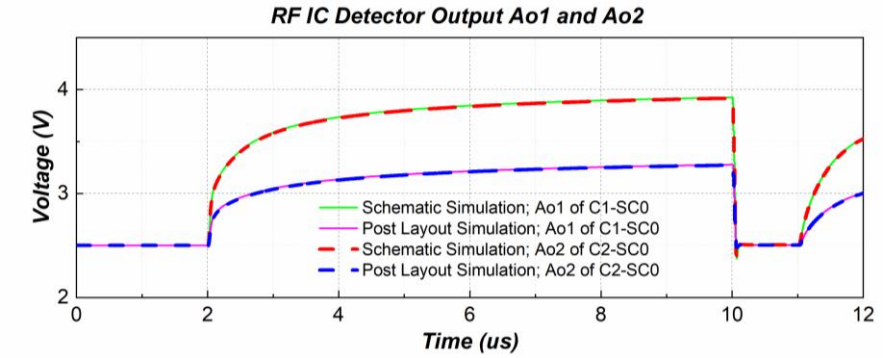

Figure 56: Shows the schematic and post-layout simulation results of sub-channel 0 in channels 1 and 2. It showcases input A1 and A4 (Figure 49), the differential output at the peak detector, CMOS reset switch activation, and RF IC detector outputs Ao1 and Ao2.

The small, consistent oscillations observed at the output of the peak detector during the charging phase, likely stemming from the component characteristics and parasitic components of the circuit, has been mitigated by IA. Additionally, we can observe a gain of nearly 4 between the output of the peak detector (input of IA) and the output of the IA. This gain indicates the amplification provided by the IA, which enhances the signal strength for further processing and analysis.

5.8.2 Sub-Channel 1 Simulation (C1SC1 and C2SC1)

The only distinction between SC0 and SC1 lies in the characteristics of their respective RF amplifiers. SC0 features an RF amplifier with high gain but limited bandwidth, while SC1 incorporates an RF amplifier with comparatively low gain but high bandwidth.

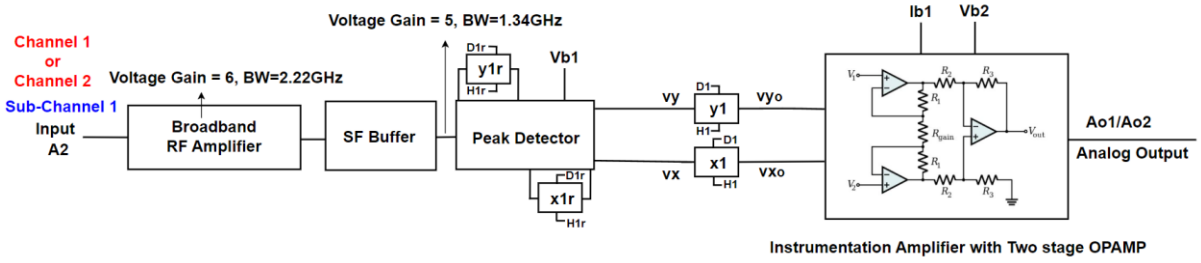

Figure 57: Shows the active blocks when sub-channel 1 is selected by the decoder based on the user input.

Figure 57 shows the active blocks involved when selecting sub-channel 1 in channel 1 and channel 2 (C1SC1 and C2SC1). To activate sub-channel 1, a binary input of 001 is applied to the 3-to-8 channel selecting line decoder. This input triggers the activation of the channel CMOS switches, subsequently activating C1SC1 and C2SC1.

Here, Figure 58 shows the simulation results, where the input signal delay time, charging process time, the triggering time of the reset switch, the colour scheme of the curves, as well as the explanations on schematic and post-layout simulations, remain consistent with the explanations provided in SC0 (Section 5.8.1).

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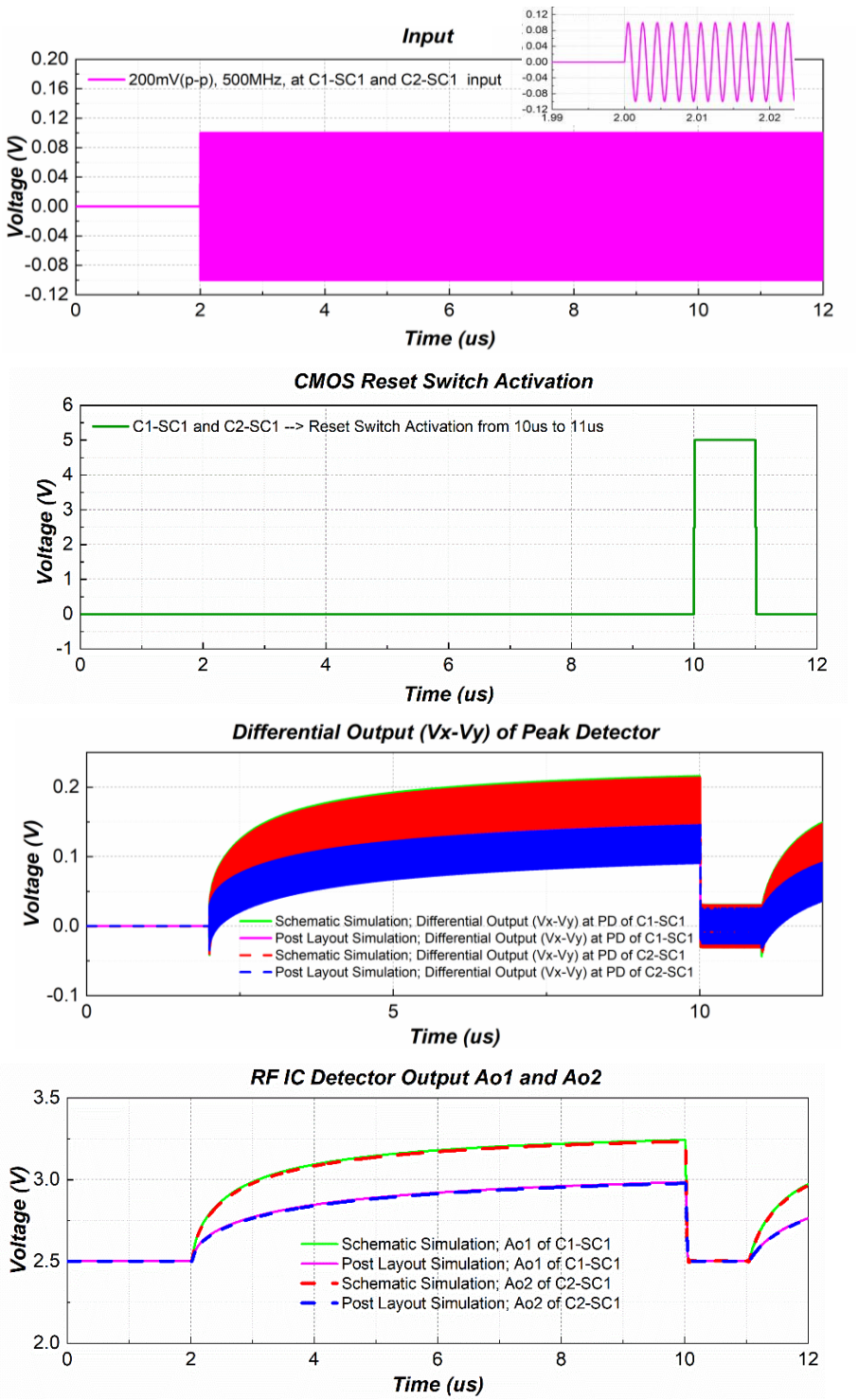

Figure 58: Shows the schematic and post-layout simulation results of sub-channel 1 in channels 1 and 2. It showcases input A2 and A3 (Figure 49), the differential output at the peak detector, CMOS reset switch activation, and RF IC detector outputs Ao1 and Ao2.

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5.8.3 Sub-Channel 2 Simulation (C1SC2 and C2SC2)

In SC2, there is no RF amplifier block; it consists only of a peak detector channel that is directly connected to the Instrumentation amplifier. Due to the absence of an RF amplifier block, SC2 has lesser sensitivity compared to SC0 and SC1.

Figure 59 illustrates the active blocks involved when selecting sub-channel 2 in both channel 1 and channel 2 (C1SC2 and C2SC2). To activate SC2, a binary input of 010 is applied to the 3-to-8 channel selecting line decoder. This input triggers the activation of the channel CMOS switches, subsequently activating C1SC2 and C2SC2.

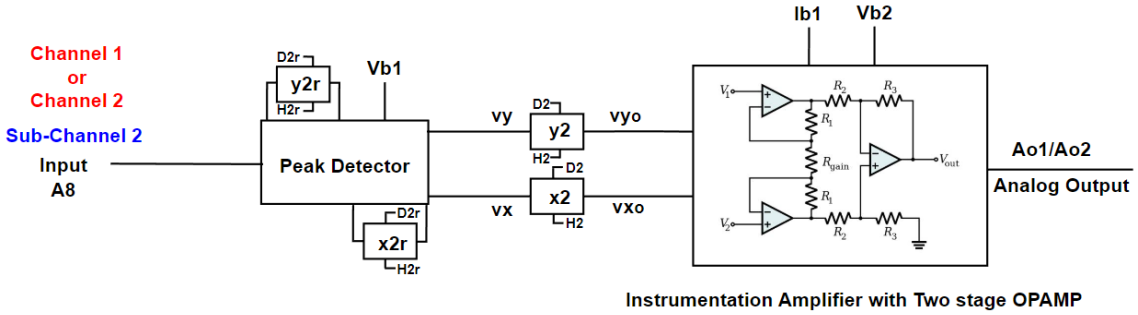
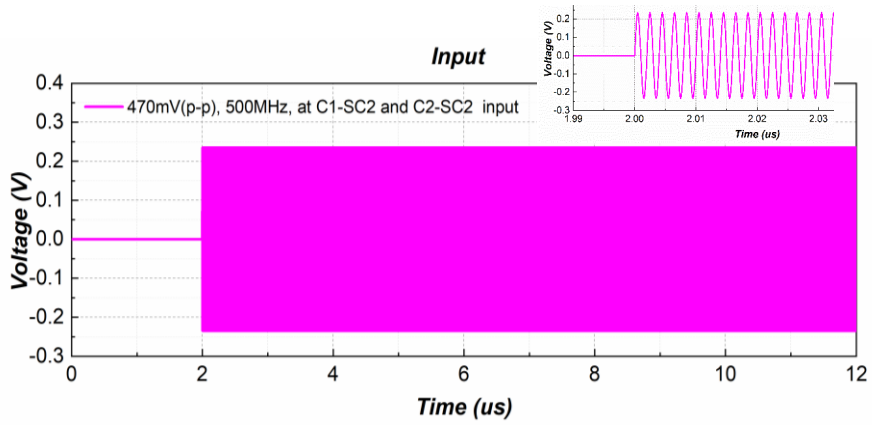
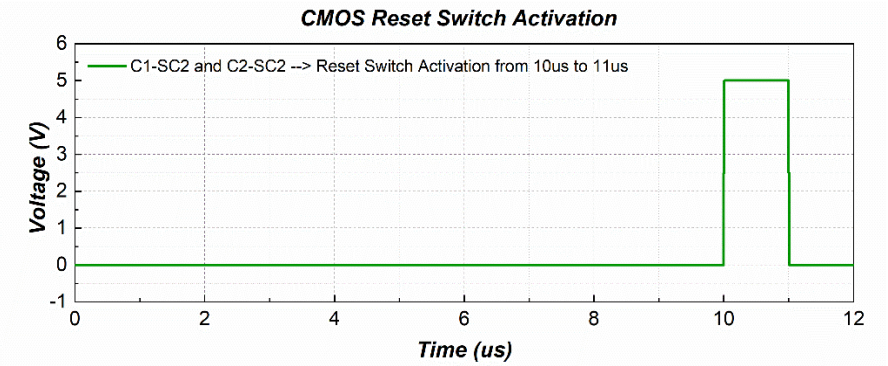


Figure 59: Shows the active blocks when sub-channel 2 is selected by the decoder based on the user input.





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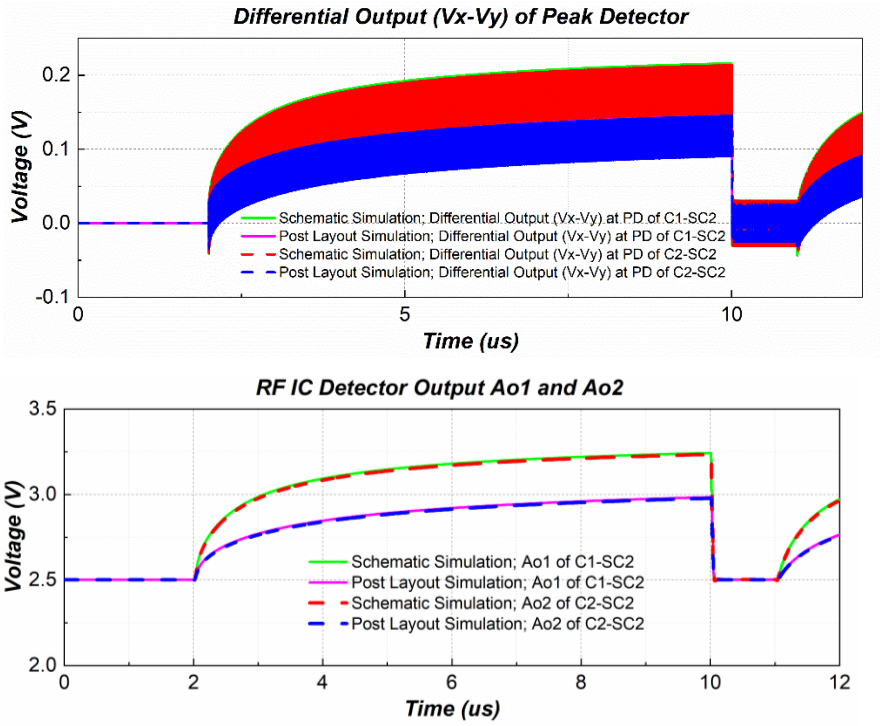

Figure 60: Shows the schematic and post-layout simulation results of sub-channel 2 in channels 1 and 2. It showcases input at A8 and A5 (Figure 49), the differential output at the peak detector, CMOS reset switch activation, and RF IC detector outputs Ao1 and Ao2.

Similar to the previous simulations for SC0 and SC1, Figure 60 shows the simulation results, where the input signal delay time, charging process time, the triggering time of the reset switch, the colour scheme of the curves, as well as the explanations of schematic and post-layout simulations, remain consistent with the explanations provided in SC0 (Section 5.8.1).

5.8.4 Sub-Channel 3 Simulation (C1SC3 and C2SC3)

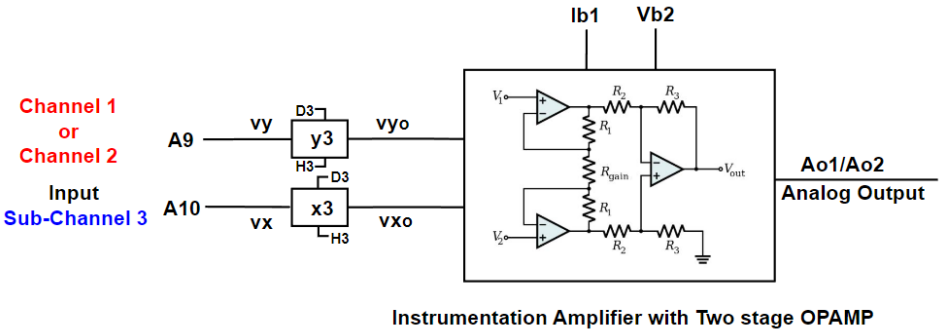

Figure 61: Shows the active blocks when sub-channel 3 is selected by the decoder based on the user input.

In SC3, there are no RF amplifier and peak detector blocks; instead, it is directly connected to the IA. As a result, there is no RF amplification or charging process, and the

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signal is fed directly to the IA. The main purpose of this channel is to test the performance of the Instrumentation Amplifier, as it is a common block for all sub-channels in a channel.

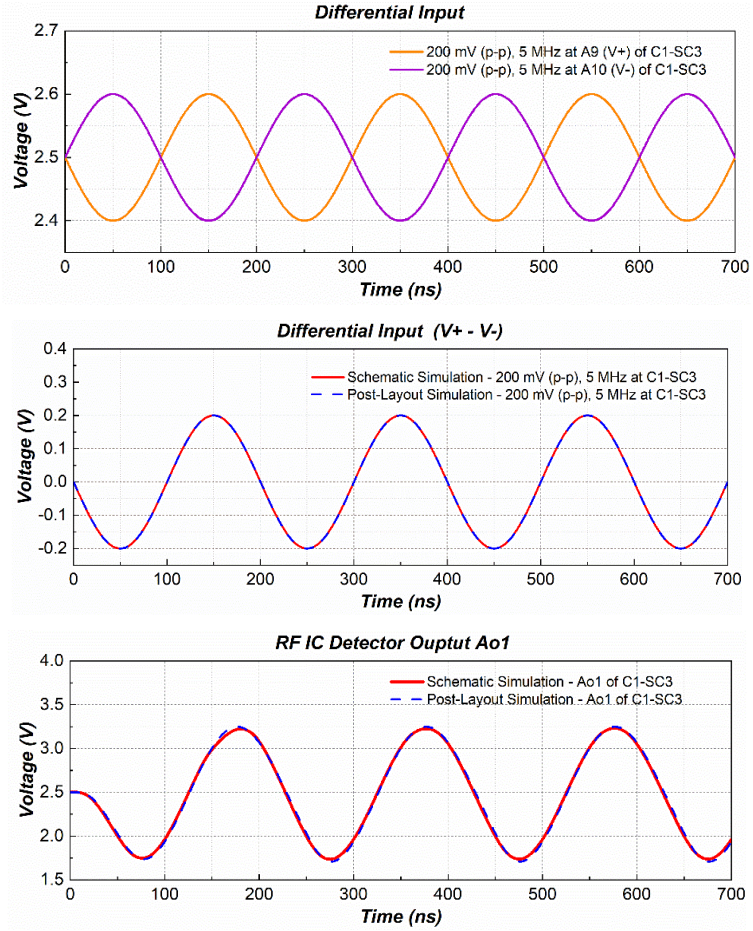

Figure 62: Shows the schematic and post-layout simulation results of sub-channel 3 in channel 1. It showcases input at A9 and A10 (Figure 49), the differential output at the peak detector, CMOS reset switch activation, and RF IC detector output Ao1.

Figure 61 illustrates the active blocks involved when selecting sub-channel 3 in both channel 1 and channel 2 (C1SC3 and C2SC3). To activate SC3, a binary input of 011 is applied to the 3-to-8 channel selecting line decoder, which triggers the activation of the channel CMOS switches, subsequently activating C1SC3 and C2SC3.

Figure 62 shows the input signal, and the schematic simulation output results, represented by the red curve, refer to the simulation performed using the circuit schematic or idealized representation of the circuit. On the other hand, the post-layout simulation output results, depicted by the blue curve, involve simulating the circuit after incorporating the layout information and considering the effects of parasitic elements.

5.8.5 Process Variation, Corner Analysis Simulation

In Section 5.2.2, the fundamental definition of process variation, which refers to the inherent variability in the manufacturing process of IC, is provided. In this section, we

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perform corner analysis using Cadence Virtuoso to assess the impact of process variation on the RF IC detector.

Corner analysis involves simulating the circuit under extreme conditions to determine the worst-case scenarios for speed and power consumption, as well as the typical or mean behaviour. Specifically, we focus on sub-channel 0 of both channel 1 and channel 2 (C1SC0 and C2SC0) and examine the worst possible process variation in terms of speed and power. This helps us understand how process variation can affect the performance of the circuit under adverse conditions. By analysing the impact of process variation, we gain valuable insights into the behaviour of the circuit under different manufacturing conditions, allowing us to optimize its design for reliability and performance.

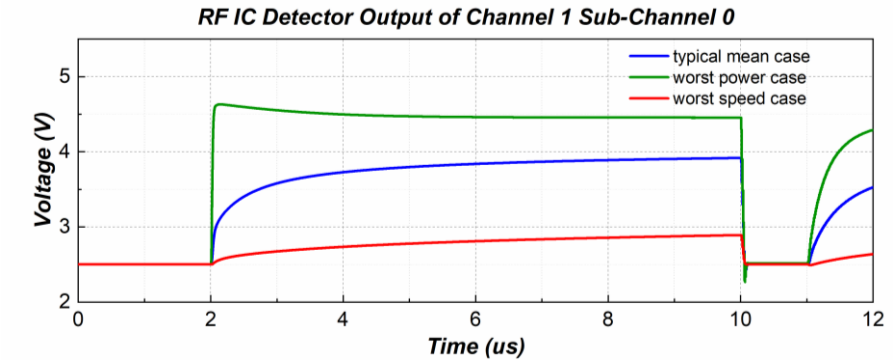

Figure 63: Shows the maximum possible variation due worst power and speed case and also it shows the typical mean case.

We compare these worst possible process variations with the typical mean behaviour which represents the average performance of the circuit. Figure 63 presents the results of the corner analysis for C1SC0 and C2SC0 after applying several layout optimization techniques, illustrating the maximum possible variation that we can expect after fabricating the RF IC detector for C1SC0 and C2SC0. The range of variation for the other sub-channels remains the same.

5.9 RF IC Detector Fabrication

5.9.1 Bond Diagrams CQFP64 and CQFN64

A bond diagram represents the wire bonding connections within a packaged IC, establishing the link between the internal die of the IC and the package pins. Ceramic Quad Flat Package 64 (CQFP64) and Ceramic Quad Flat No-lead (CQFN64) are commonly utilized 64-pin surface mount IC packages. The CQFP64 has a square or rectangular shape, with leads extending from all four sides, enabling electronic connections between the wire bonds of the internal IC and the 64 leads of the package. In contrast, the CQFN64 package is a modern design without leads extending beyond the package's edge, as the electrical connections are established through solder balls on the underside of the package.

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As detailed in Section 5.7.1, the PAD ring comprises a total of 52 I/O cells, with 13 cells allocated to each side. These cells are specifically designed to interface with the CQFP/N64 package, which provides a total of 64 pins. On each side of the package, there are 16 pins available. Consequently, three spare pins remain unconnected on each side, as they are not associated with any specific pads.

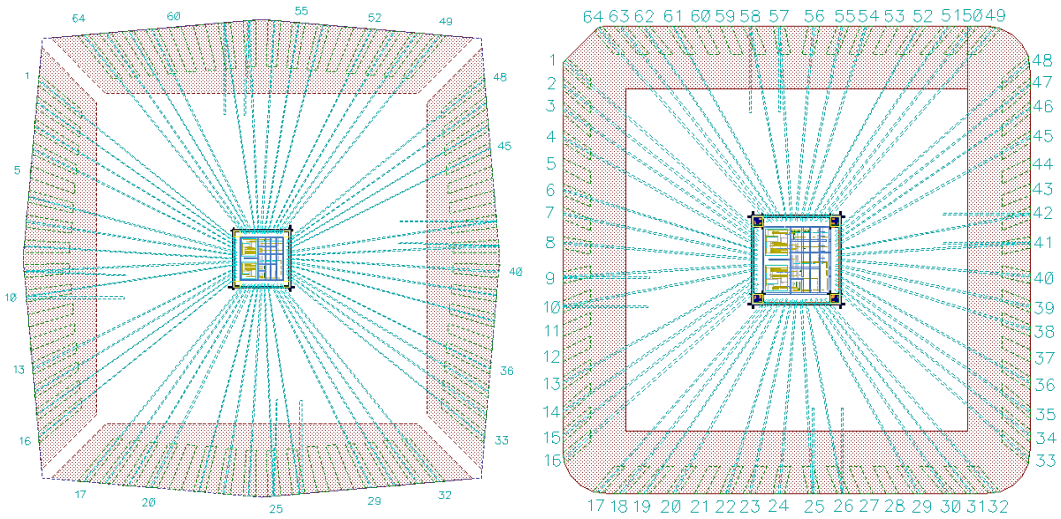

Figure 64: Shows the bond diagram of CQF64 (left) and CQN64 (right).

As mentioned in Section 4.2, the calculated absorbed power of the pins farthest away from the GND pins in the simplified model proves suitable for estimating EM energy coupled into the IC package. Therefore, the leftover spare pins are utilized to create the necessary distance between signal pins and GND pins, thus optimizing the design for improved performance and accurate estimation of coupled power from signal pins.

5.9.2 RF IC Detector Microscopic View

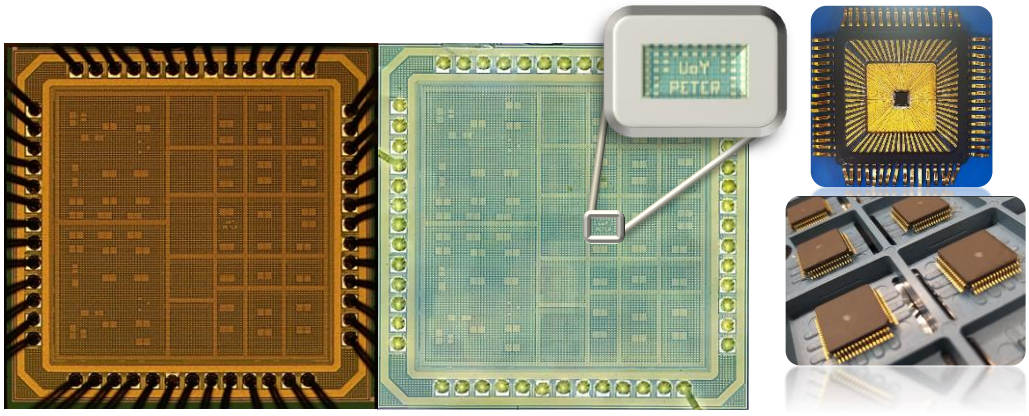

Figure 65: Shows the microscopic images of the RF IC detector.

After the IC was sent for tape-out, it took approximately 8 months for semiconductor processing and IC packaging to be completed, resulting in the final IC being ready for

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testing. Figure 65 displays microscopic images of the RF IC detector captured using different microscopes. In the right image of the figure, the name of the UoY and the PETER project is visible.

5.10 Pin Definition of RF IC Detector

A comprehensive breakdown of each block within the detector is provided in Section 5.5 of the thesis. The corresponding block diagram of the RF IC detector is illustrated in Figure 21. To facilitate understanding and ease of reference, Table 17 from Appendix 11.8 presents the RF IC detector pins with meaningful names and accompanying descriptions. Additionally, the table identifies the specific pins employed for S-parameter measurements and those that will be connected to the micro coaxial connector (MCX) connector via a bias T. Subsequent chapters will delve into the practical application of the measured S-parameters, demonstrating their efficacy in validating the proposed methodology for estimating conducted and radiated coupling into PCB tracks and IC package pins with a realistic load.

5.11 Lessons Learnt during RF IC Detector Design

Initiating the design with the PAD Ring provides a flexible floor planning approach, enabling a better understanding of the available space for the entire circuit. Incorporating decoupling capacitors within the unused chip space enhances capacitance between VDD and GND, effectively suppressing high-frequency noise in power supply rails. In the X-FAB semiconductor process, which spans approximately 6 to 9 months, packaging adds an additional 2 to 4 months, resulting in a total timeframe of 8 to 12 months. It's essential to anticipate the possibility of faulty ICs during testing, as our initial chip experienced issues that were later traced back to a faulty IC. For microscopic images, the outer package can be opened by removing the glued top lid in the IC package.

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6. PCB Test Benches for RF IC Detector

In this chapter, we delve into the design of PCB test benches utilized for the RF IC detector in various measurement scenarios. These scenarios encompass conducted measurements, radiated measurements in reverberant environments, and radiated measurements in GTEM environments. The measurement test benches serve a crucial role in upcoming chapters, as they facilitate the validation of the numerical model from [7] which is capable of estimating stochastic EM fields coupling into PCB traces under realistic load conditions and understanding the power flow dynamics between internal and external shielding enclosure due to AACS of PCB tracks and IC package pins.

6.1 Test Bench Block Diagram

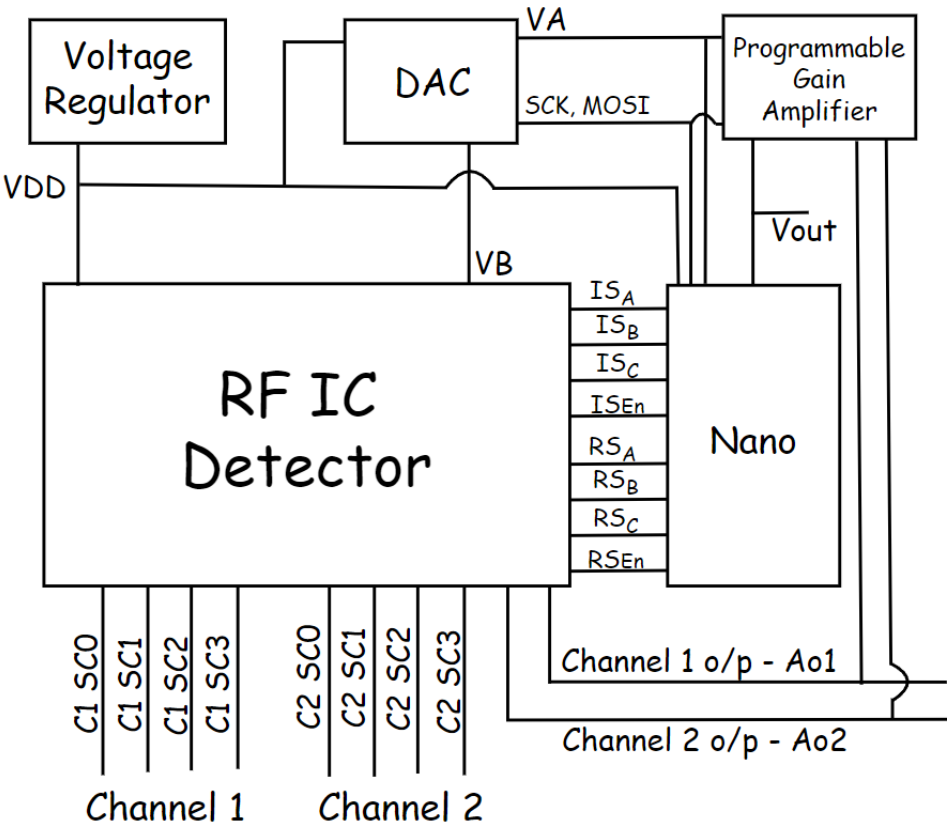

Figure 66: Shows the block diagram of the PCB test bench used for the RF IC detector.

Figure 66 illustrates the interconnection between the RF IC detector and subsequent blocks responsible for its digital control, supply voltage regulation, provision of required bias voltage, and amplification of the output signal. These blocks complete the operational design and monitor the RF IC detector.

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6.1.1 Arduino Nano

The Arduino Nano [50] block is an 8-bit microcontroller. It can be programmed through a USB interface to the development system on a computer and offers a range of input/output (I/O) pins. The microcontroller is monitored by the Atmel ATmega328P microprocessor chip.

The I/O pins of the Arduino Nano provide signals to the sub-channels and reset multiplexors of the RF IC detector. The built-in 10-bit analogue-to-digital converter (ADC) on the Arduino Nano measures the channel outputs Ao1 and Ao2 of the RF IC detector. These measurements can be obtained either directly or by utilizing the programmable gain amplifier (PGA) and leading to the output Vout. Additionally, spare channels on the Arduino Nano are employed for monitoring parameters such as bias voltages (VA, VB), bias currents, and power rails.

6.1.2 Voltage Regulator

The voltage regulator LT3045 [51] is a high-performance, low-dropout linear regulator. Its primary function in this work is to ensure a consistent and stable voltage of 5V (VDD) for the RF IC detector, even in cases where the input supply voltage slightly exceeds 5V.

The LT3045 voltage regulator maintains a reliable and precise power supply for the RF IC detector. By effectively regulating the voltage, it prevents any fluctuations or variations in the input voltage from affecting the performance and functionality of the RF IC detector. This is important as the RF IC detector requires a consistent 5V supply voltage to operate optimally.

6.1.3 Digital to Analog Converter (DAC)

The test bench incorporates the Microchip MCP4812 [52], a dual 12-bit buffered voltage output digital-to-analogue converter (DAC). This DAC's dual-channel configuration enables the simultaneous generation of multiple bias voltages (VA and VB), which are essential for the RF IC detector and programmable amplifier. With its high precision and dual-channel configuration, the MCP4812 ensures accurate and reliable biasing, contributing to optimal performance and measurement accuracy.

6.1.4 Programmable Gain Amplifier (PGA)

The test bench incorporates the MCP6S28 [53] programmable gain amplifier (PGA) block to facilitate signal amplification. With its flexible gain configuration options ranging from +1 V/V to +32 V/V, the MCP6S28 allows for precise adjustment of amplification levels. The PGA incorporates an input multiplexer that enables the selection of up to eight channels via a convenient Serial Peripheral Interface (SPI) port.

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The main purpose of the MCP6S28 PGA within the test bench is to enhance the gain of the RF IC detector's output signal (Ao1 and Ao2). It is useful in scenarios where the detected signal is weak or requires additional amplification for accurate measurement. By adjusting the gain settings of the MCP6S28, the test bench can effectively amplify the output signal, improving sensitivity and enabling reliable detection of desired signals. The integration of the MCP6S28 PGA enhances the overall signal processing capabilities of the test bench, facilitating optimal measurement performance and ensuring accurate analysis of the RF IC detector's output and leading to the output Vout.

6.2 Three Board Concept

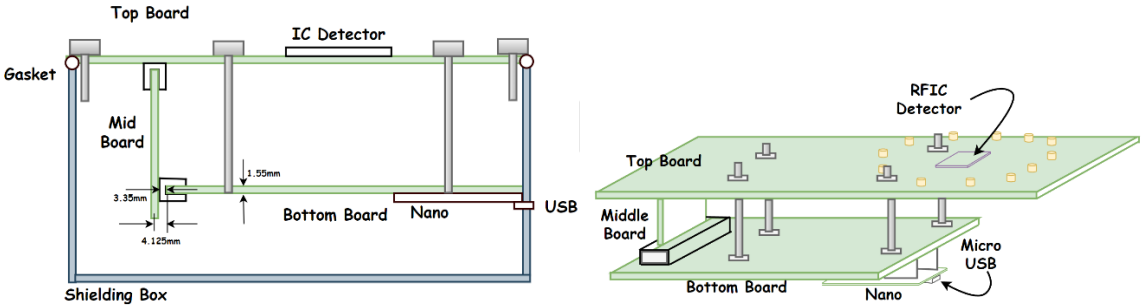

Figure 67: Shows the three-board concept test bench

The test setup consists of three boards: the top board, the middle board, and the bottom control board, which are interconnected via a peripheral component interconnect express (PCIe) connector, as shown in Figure 67. The top board houses the RF IC detector, which is connected to MCX RF connectors through RF PCB tracks. Additionally, the top board features a shielding frame for conducting radiated measurements, providing the means to evaluate the dominant coupling between PCB traces and IC package pins.

The middle board serves as a connector between the top and bottom boards, facilitating communication and data transfer via the PCIe connector. The bottom control board centred around an Arduino Nano [50], incorporates essential components such as the MCP6S28 Microchip Programmable Gain Amplifier [53] with an 8-channel input multiplexer, and the MCP4822 Microchip Dual 12-bit DAC [52]. The Arduino Nano instrumentation PCB, located on the bottom board, controls and monitors the RF IC detector using NI-VISA and Python software, establishing communication through a micro USB interface.

The PCB test bench can be powered by a battery, DC supply, or through the Arduino Nano's USB port, which also serves as the control interface for the test bench.

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6.3 Design of Control Board in KiCAD

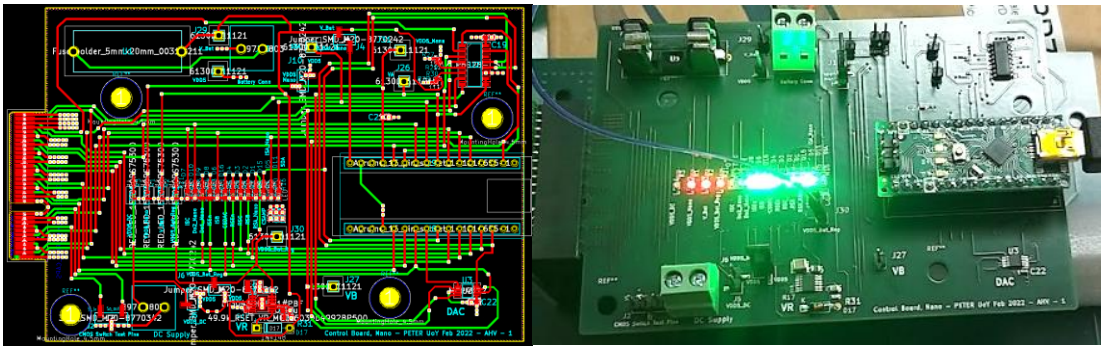

Figure 68: Shows the layout and picture of the Bottom Control Board from KiCAD

As described in Section 6.2, the control board, located at the bottom of the test bench, serves as the central control and monitoring unit for the RF IC detector. It is equipped with essential components such as the Arduino Nano [50], the MCP6S28 Microchip Programmable Gain Amplifier [53] with an 8-channel input multiplexer, and the MCP4822 Microchip Dual 12-bit DAC [52]. The design of this board allows it to be utilized for both conducted and radiated measurements simply by swapping the top board. This implies that the bottom board is universally applicable for both types of measurements. Figure 220 (Appendix 11.8) presents the schematic of the bottom control board, illustrating the incorporation of all necessary components and connections to establish seamless connectivity between the bottom board, mid board, and top board via the PCIe connector. Additionally, Figure 68 demonstrates a meticulously designed layout that accommodates all components within the limited space, while satisfying design rule checks and plating index ratio requirements.

6.4 Design of Middle Board in KiCAD

The middle board serves a simple purpose and does not contain any components except for the PCIe connector slot and PCIe connector. Its schematic is shown in Figure 221 (Appendix 11.8) and layout designs and pictures are shown in Figure 69. The middle board acts as a connection between the top board and the bottom control board. Two different types of middle boards have been designed for specific purposes.

In the case of middle board 1, the layout space has been fully utilized without any wastage. On the other hand, middle board 2 has been designed with a larger width to increase the distance between the top board and the bottom control board. This design consideration is necessary for GTEM cell measurements, where a coaxial cable is connected to the backside of the top GTEM board, requiring additional space between the top GTEM board and the bottom control board. The larger width of middle board 2 allows for

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increased height between these two boards, facilitating the test in GTEM cell and S-parameter measurements.

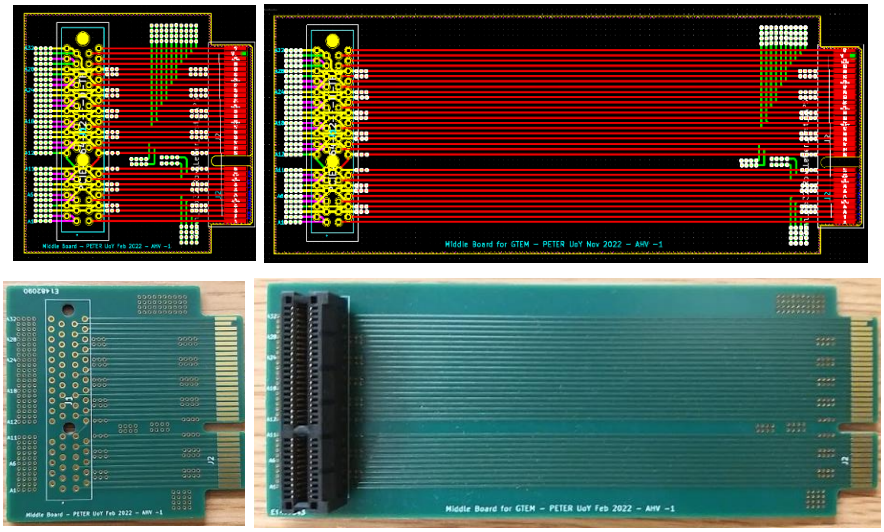

Figure 69: Shows the layout and picture of the middle board 1 (left) and GTEM middle board 2 (right) from KiCAD.

6.5 Test Bench for Conducted Measurement

The test bench for the conducted board serves multiple purposes. Firstly, it enables the execution of basic functionality tests for all sub-channels of both channels in the RF IC detector. Additionally, it facilitates S-parameter measurements of the RF IC detector's package pins via RF PCB tracks, allowing the calculation of input impedance based on the measured S-parameters. Moreover, the test bench is used to generate calibration curves for the RF IC detector at different frequencies. The detailed analysis of calibration curves and the process of calibrating the RF IC detector is discussed in Section 7.2.1. During radiated measurements, the measured calibration curves become crucial in measuring the coupled forward power at the package pin.

The RF PCB tracks used for this measurement are microstrip TLs with the characteristic impedance of 50 Ω. Throughout the entirety of this research work, microstrip TLs were employed for the purpose of conducting the measurements.

6.5.1 Design of Conducted Board in KiCAD

The conducted board is positioned at the top of the test bench and is equipped with several components and features. The board incorporates 18 MCX connectors with 36mm microstrip TL (50 Ω) that establish connections between the RF IC detector and the conducted board through RF PCB tracks arranged in a circular pattern. Essential test pins are also included for functionality tests. The board features bias tees to separate DC

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operating points and RF signals between internal and external circuitry, as well as combining RF signals and DC signals internally. Furthermore, a PCIe connector is present to establish a connection with the middle board. The schematic and layout design of the conducted board can be seen in Figure 222 (Appendix 11.8) and Figure 70, respectively.

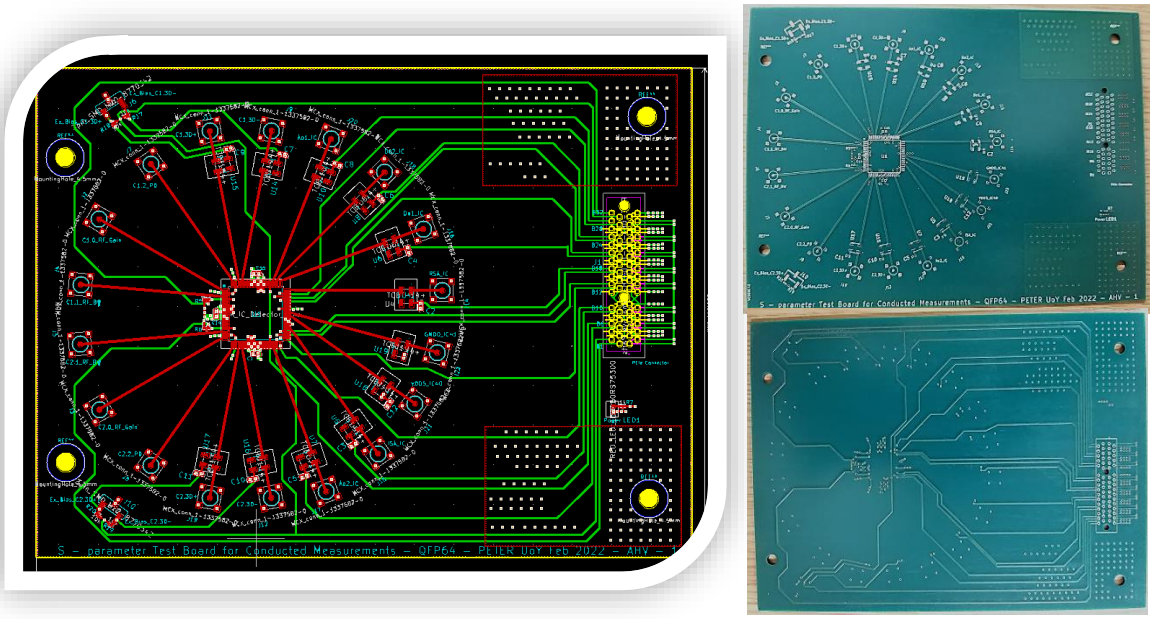

Figure 70: Shows the layout and pictures of the Top Conducted Board from KiCAD.

6.5.1.1 Conducted Board PCB Parameters

The table below provides an overview of the conducted board PCB parameters after the fabrication process:

Parameter Name	Conducted Board
Number of Layers	4
RF PCB track width (w)	0.72 mm
RF PCB track thickness (t)	18 um
Substrate height from ground plane for RF PCB tracks (h)	0.36 mm
Characteristic Impedance of the RF PCB Track	50 Ω
Board Dimension	166.17 x 123.78 mm^2
Dielectric Constant (Dk) / Relative Permittivity (ε_r)	(FR4-improved, IS400 [54]) 4.0 @100 MHz 3.9 @500 MHz

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Diffraction Factor (Df) / Loss Tangent ($tan\ \delta$)	0.020 @100 MHz 0.022 @500 MHz

Table 5: Shows the conducted board PCB parameters.

These parameters are essential for understanding the physical characteristics and electrical behaviour of the conducted board. They determine signal integrity, impedance matching, and overall performance of the RF IC detector and other components on the board.

6.5.2 TRL Calibration Board for Conducted Board

The conducted board features a 35 mm (L=35mm) RF PCB track with a characteristic impedance of 50 Ω between the RF IC detector and MCX connectors. To eliminate the impact of this PCB trace, a Through Reflect Line/Match (TRL/M) calibration is employed. This calibration enables accurate measurement of S-parameters at the package pins, facilitating impedance determination and precise power analysis for both incoming and reflected signals. The TRL/M calibration utilizes five essential components: Through, Reflect, Line 1, Line 2, and Match. A dedicated board with appropriate trace lengths corresponding to the frequency range of interest is necessary for conducting this calibration.

The "Thru" trace, twice the length (2L), serves as a reference to measure transmission characteristics and compensate for impedance mismatches. "Line 1" is a known-length TL used for calibration and characterization. "Line 2" verifies calibration accuracy and measures additional device characteristics. The "Match" trace ensures proper termination and allows reflection and impedance measurements, while the "Reflect" trace captures reflections caused by impedance mismatches or discontinuities.

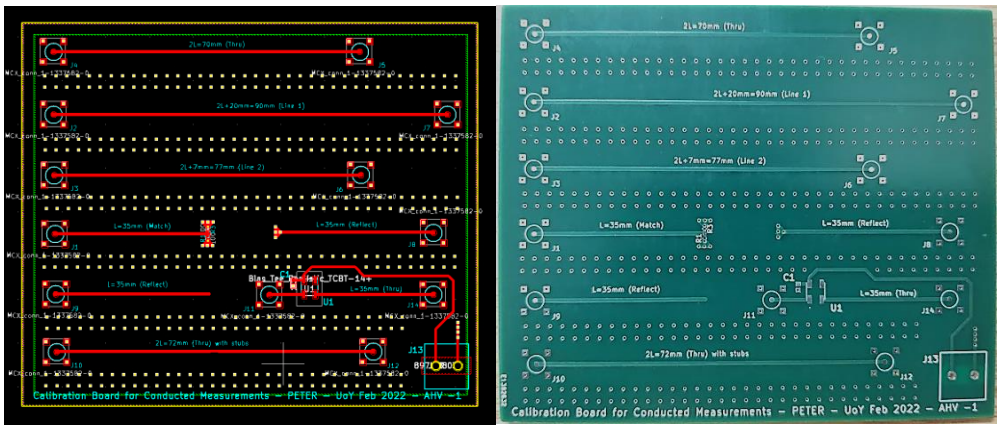

Figure 71: Shows the layout and picture of the TRL calibration board for the conducted board from KiCAD.

The calibration is performed using the Rhode & Schwarz VNA ZVB20 instrument [55]. The user manual [56] provides guidance on calculating the lengths of line 1 and line 2 traces based on the specific frequency range of interest, utilizing the below-given equations.

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$$L_{line1} = L_{long} = \frac{c_o}{\left(360^o/_{20^o}\right) * f_{min}} + L_{thru}$$
$$L_{line2} = L_{short} = \frac{c_o}{\left(360^o/_{160^o}\right) * f_{max}} + L_{thru} \quad (44)$$

where c_o represents the speed of light, L_{thru} denotes the length of the Through trace, and f_{min} and f_{max} represent the minimum and maximum frequencies of interest, respectively.

Standard Type	Minimum Frequency	Maximum Frequency	Trace Length
Line 1	828.35 MHz	6.6328 GHz	90 mm
Line 2	2.351 GHz	18.83 GHz	77 mm
Thru	0	18.83 GHz	70 mm
Match	0	828.35 MHz	35 mm
Reflect	0	18.83 GHz	35 mm

Table 6: Shows the frequency range and lengths of TRL standard required for conducted board calibration.

The schematic and layout for the TRL calibration board for the conducted board are illustrated in Figure 223 (Appendix 11.8) and Figure 71, respectively. The board design optimally utilizes the available space by including a trace with a bias tee to investigate the trace behaviour in the presence of a bias tee. The PCB parameters of the calibration board for the conducted board will be identical to those of the conducted board, with the exception of the board size.

6.6 Test Bench for Radiated Measurement

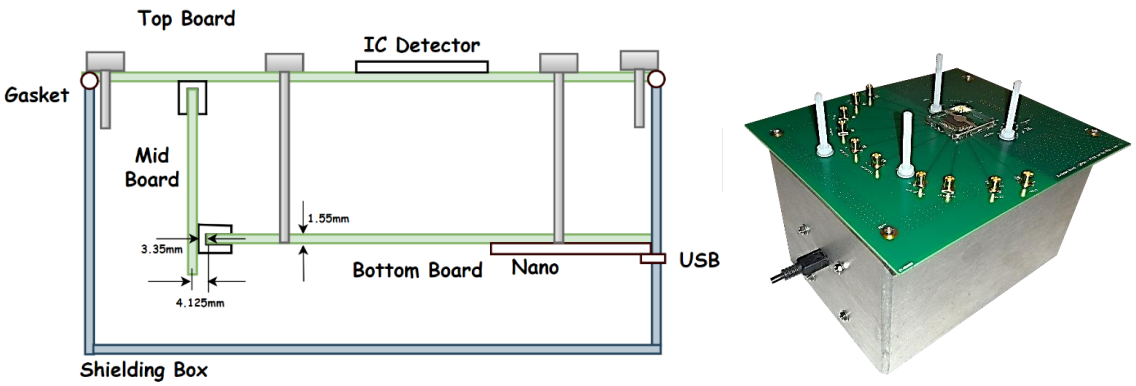

Figure 72: Shows the radiated measurement test bench setup.

Radiated measurements are primarily performed within a reverberation chamber (Section 3.2.2), where the radiated board is positioned at the top of the test bench. The entire test

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bench, including the bottom control board, middle board, and the bottom side of the radiated board, is shielded. Only the top side of the radiated board is exposed to the reverberant environment, as shown in Figure 72. The top side of the radiated board consists of the RF IC detector and RF PCB tracks with a characteristic impedance of 115 Ω and are connected to all the sub-channels of channels 1 and 2 of the detector IC. A 65 Ω resistor is inserted between each track end and MCX connector so a standard 50 Ω load or instrument can be used to provide a matched termination for each track when required. A track impedance of 115 Ω was chosen as it is typical of the tracks used for signal connections on a PCB.

6.6.1 Design of Radiated Board Type 1

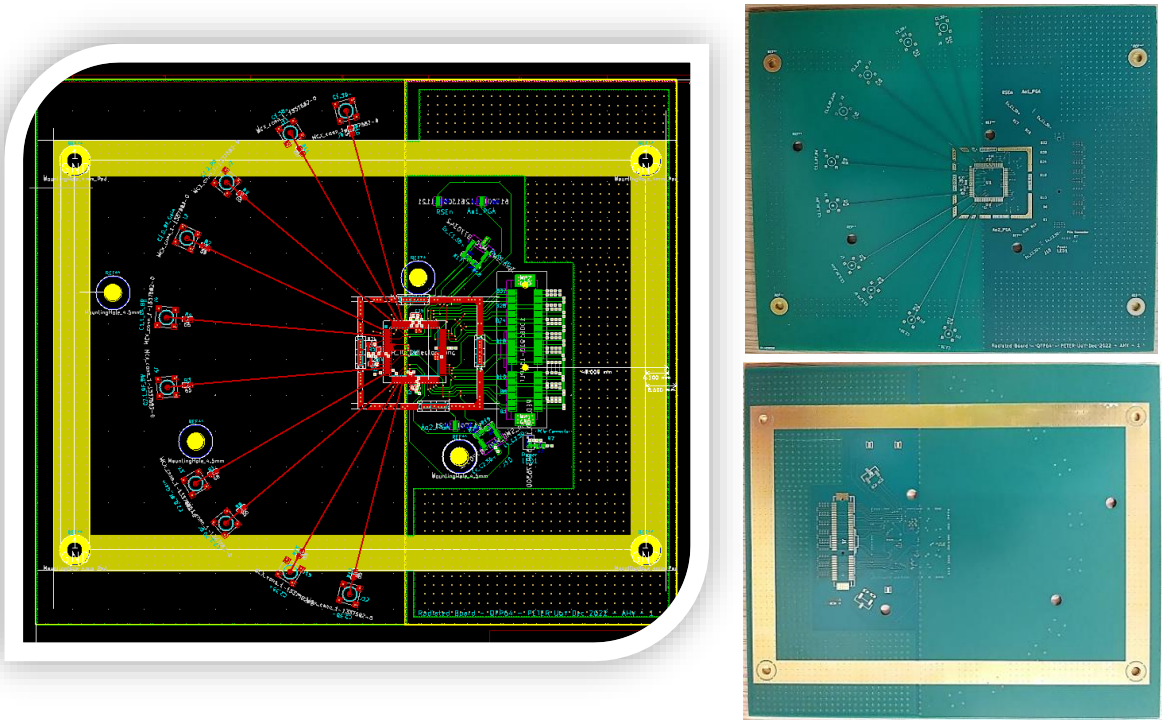

Figure 73: Shows the layout and pictures of the Top Radiated Board type 1 from KiCAD.

The radiated board is positioned at the top of the test bench and features various components. It includes 10 MCX connectors, with 5 connectors assigned to each of channels 1 and 2. These MCX connectors establish connections between the RF IC detector and the radiated board through RF PCB tracks (60 mm) equipped with 65 Ω resistors arranged in a semi-circular pattern as shown in Figure 73. The purpose of including MCX connectors in the radiated board is to verify the conducted board's measurement of the RF IC detector and perform basic functionality tests. Test pins are also incorporated at the bottom side of the radiated board for bias testing. Additionally, a shielding frame surrounds the RF IC detector, enabling measurements with and without shielding. A PCIe connector is present to establish a connection with the middle board. The top side of the radiated board exclusively contains the RF IC detector and RF PCB tracks, which are exposed to

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the reverberant environment. To shield the unexposed part of the test bench, namely the bottom side of the radiated board, middle board, and bottom control board, a rectangular shielding box (171.9mm x 120.9mm x 107mm) is incorporated. To ensure proper grounding for the shielding, a grounded conducting path in a rectangular configuration has been incorporated on the underside of the top board, as shown in Figure 73. Additionally, a conducting gasket is interposed between the rectangular grounded conducting path on the bottom side of the top board and the shielding box. Moreover, the strategic positioning of the mini USB connector on the bottom control board guarantees that its ground connection makes direct contact with the shielding box, establishing a secure grounding connection for the entire shielding system. For detailed information, refer to Figure 224 (Appendix 11.8) for the schematic and Figure 73 for the layout design and pictures of the radiated board.

6.6.1.1 Radiated Board PCB parameters

The table below provides an overview of the radiated board PCB parameters after the fabrication process:

Parameter Name	Radiated Board
Number of Layers	4
RF PCB track width (w)	0.48 mm
RF PCB track thickness (t)	18 um
Substrate height from ground plane for RF PCB tracks (h)	1.43 mm
Characteristic Impedance of the RF PCB Track	115 Ω
Board Dimension	180 x 153 mm^2
Dielectric Constant (Dk) / Relative Permittivity (ε_r)	(FR4-improved, IS400 [54]) 4.0 @100 MHz 3.9 @500 MHz
Diffraction Factor (Df) / Loss Tangent ($tan\,\delta$)	0.020 @100 MHz 0.022 @500 MHz

Table 7: Shows the radiated board PCB parameters.

6.6.2 Design of Radiated Board Type 2

The only difference between Type 1 and Type 2 radiated boards is the extension of RF PCB tracks to the edge of the board, enhancing the coupling of the EM fields to the tracks.

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This extension exposes the RF tracks to a higher level of radiated EM fields. This board configuration proves beneficial when the power coupled to the RF PCB tracks is insufficient, causing it to be lower than the sensitivity of the RF IC detector. In such cases, extending the RF PCB tracks increases the coupling of the EM fields, ensuring that the coupled power falls within the dynamic range of the detector. These layout changes are illustrated in Figure 74, while the PCB parameters mentioned in Table 7 remain the same for both Type 1 and Type 2 radiated boards.

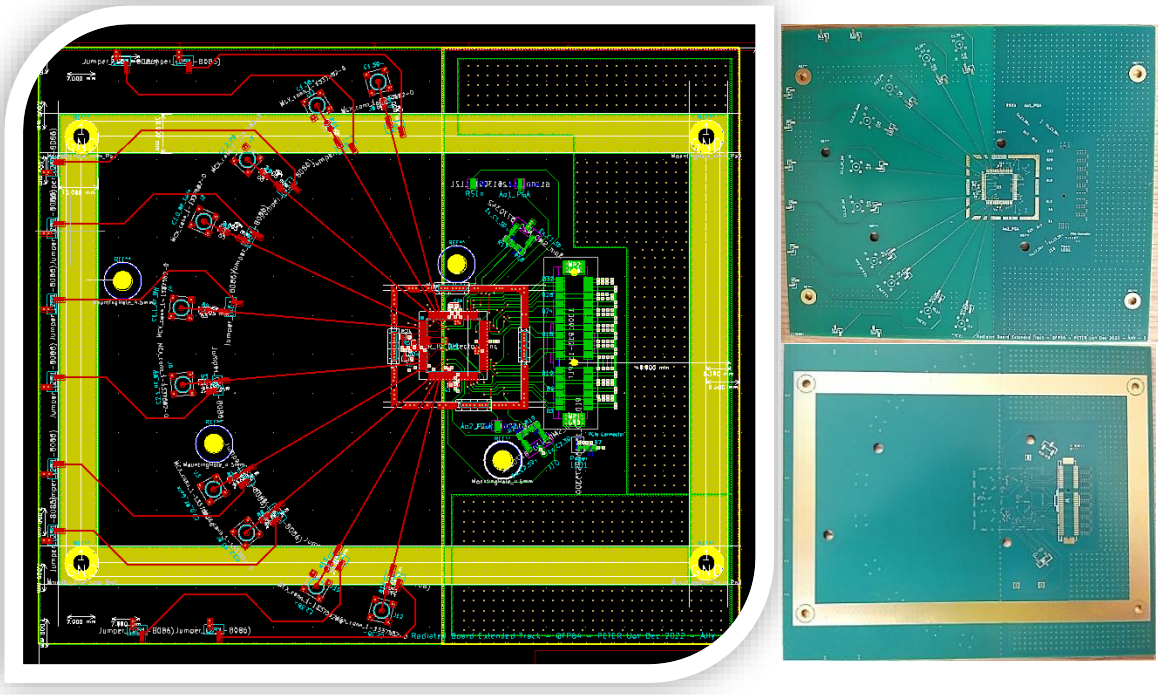

Figure 74: Shows the layout of the Top Radiated Board type 2 from KiCAD.

6.6.3 Calibration Board for Radiated Board Type 1

The design procedure for the TRL calibration board remains unchanged, as explained in Section 6.5.2. The radiated board features a 60 mm (L=60 mm) RF PCB track with a characteristic impedance of 115 Ω, along with a series resistance of 65 Ω near the MCX connector connecting the RF IC detector and MCX connectors. However, using a 65 Ω resistor in the TRL calibration may introduce inaccuracies. In case inaccuracies occur, the calibration board built for TRL can be utilized to perform de-embedding calculations. These calculations exclude the effects of the RF PCB tracks in the radiated boards, allowing for a more accurate comparison of the conducted board's measurements. This comparison helps to assess the process variability between different RF IC detectors. It is important to note that this calibration board is suitable for type 1 radiated boards only, as there is no calibration board built specifically for type 2 radiated boards.

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The schematic and layout for the TRL calibration board designed for the radiated board are shown in Figure 225 (Appendix 11.8) and Figure 75, respectively. The board design efficiently utilizes the available space and incorporates a 120 mm through trace without resistors, as well as a 60 mm trace with a single resistor. This configuration allows for the investigation of trace behaviour in the presence of a resistor. The PCB parameters of the calibration board for the radiated board will be identical to those of the radiated board, except for the board size.

Standard Type	Minimum Frequency	Maximum Frequency	Trace Length
Line 1	800.3 MHz	4.392 GHz	140.81 mm
Line 2	4.392 GHz	10 GHz	133.32 mm
Thru (2L)	0	10 GHz	120 mm
Match (L)	0	800.3 MHz	60 mm
Reflect (L)	0	10 GHz	60 mm

Table 8: Shows the frequency range and lengths of TRL standard required for radiated board type 1 calibration.

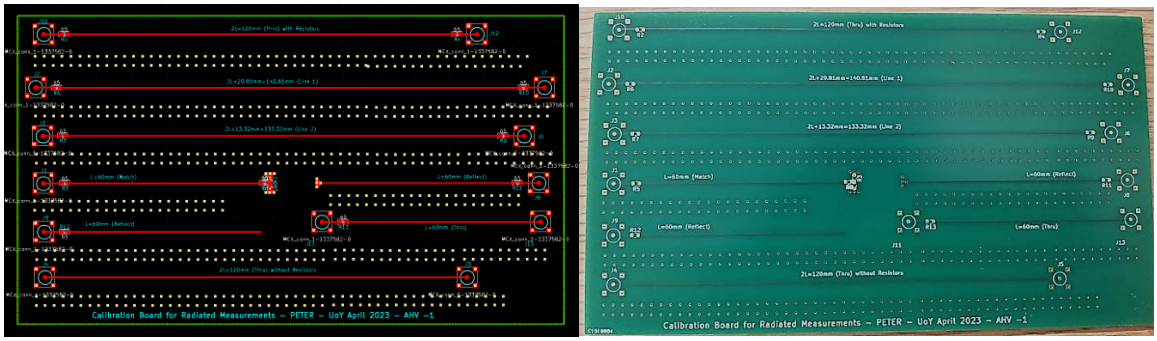

Figure 75: Shows the layout of the TRL calibration board for radiated board type 1 from KiCAD.

6.7 Test Bench for GTEM Cell Measurement

The GTEM board is positioned at the top of the test bench, while the bottom control board, GTEM middle board (as discussed in Section 6.4), and the bottom side of the GTEM board remain outside the GTEM cell. Only the top side of the GTEM board is exposed to the GTEM cell environment. This top side consists of the RF IC detector and RF PCB tracks, which possess a characteristic impedance of 115 Ω and are connected to all the sub-channels of channels 1 and 2. A 65 Ω resistor is inserted between each track end and MCX connector so a standard 50 Ω load or instrument can be used to provide a matched termination for each track when required. For the radiated measurements, the GTEM board test bench, the top side of the GTEM board with RF IC detector, is clamped

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onto a special opening on the topside of the GTEM cell wall, and the measurements are conducted within the GTEM cell [57].

6.7.1 Design of GTEM Board in KiCAD

The GTEM board, designed according to the specifications outlined in the BS EN 61967-2 standard [58], measures 100x100mm and is situated at the top of the test bench, housing multiple components. It mirrors the design of the radiated board discussed in Section 6.6 concerning the placement of MCX connectors, RF PCB tracks, characteristic impedance of the track, series resistance used on the track, provision for shielding the RF IC detector, and connection between the top and bottom board. The only difference is the trace length in the GTEM board, which is 19.318 mm. The top side of the GTEM board contains the RF IC detector and RF PCB tracks, which are exposed to the GTEM environment. To integrate the GTEM board into the outer wall layer of the GTEM cell, a square conducting frame is incorporated on the top side of the GTEM board, enabling contact with the GTEM cell wall. For more detailed information, refer to Figure 226 (Appendix 11.8) for the schematic and Figure 76 for the layout design and picture of the GTEM board.

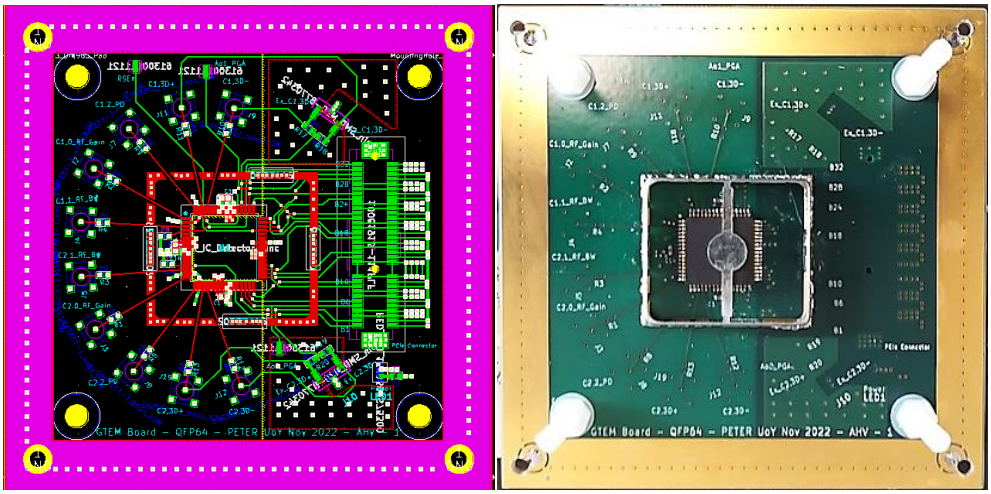

Figure 76: Shows the layout of the GTEM Board from KiCAD.

6.7.1.1 GTEM Board PCB Parameters

The table below provides an overview of the conducted board PCB parameters after the fabrication process:

Parameter Name	GTEM Board
Number of Layers	4
RF PCB track width (w)	0.33 mm
RF PCB track thickness (t)	18 um

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Substrate height from ground plane for RF PCB tracks (h)	1.07 mm
Characteristic Impedance of the RF PCB Track	115 Ω
Board Dimension	100 x 100 mm^2
Dielectric Constant (Dk) / Relative Permittivity (ε_r)	(FR4-improved, IS400 [54]) 4.0 @100 MHz 3.9 @500 MHz
Diffraction Factor (Df) / Loss Tangent ($tan\,\delta$)	0.020 @100 MHz 0.022 @500 MHz

Table 9: Shows the GTEM board PCB parameters.

6.7.2 Calibration Board for GTEM Board

The design procedure for the TRL calibration board remains unchanged, as explained in Section 6.5.2. The GTEM board features a 19.318 mm (L=19.318 mm) RF PCB track with a characteristic impedance of 115 Ω. A series resistance of 65 Ω is added near the MCX connector that connects the RF IC detector and MCX connectors. However, it is important to note that using a 65 Ω resistor in the TRL calibration may introduce inaccuracies. In such cases, the calibration board specifically built for TRL can be utilized to perform de-embedding calculations. These calculations help exclude the effects of the RF PCB tracks in the GTEM boards, ensuring a more accurate comparison of the conducted board's measurements. This comparison is crucial for assessing the process variability between different RF IC detectors.

Standard Type	Minimum Frequency	Maximum Frequency	Trace Length
Line 1	800.3 MHz	4.366 GHz	59.446 mm
Line 2	4.366 GHz	9.855 GHz	52.156 mm
Thru (2L)	0	9.855 GHz	38.636 mm
Match (L)	0	800.3 MHz	19.318 mm
Reflect (L)	0	9.855 GHz	19.318 mm

Table 10: Shows the frequency range and lengths of TRL standard required for GTEM board calibration.

The schematic and layout for the TRL calibration board designed for the GTEM board are shown in Figure 227 (Appendix 11.8) and Figure 77, respectively. The board design optimally utilizes the available space by including a 38.636 mm through trace without

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resistors and a 19.318 mm trace with a single resistor. This configuration allows for the investigation of trace behaviour in the presence of a resistor. The PCB parameters of the calibration board for the GTEM board will be identical to those of the GTEM board, except for the board size.

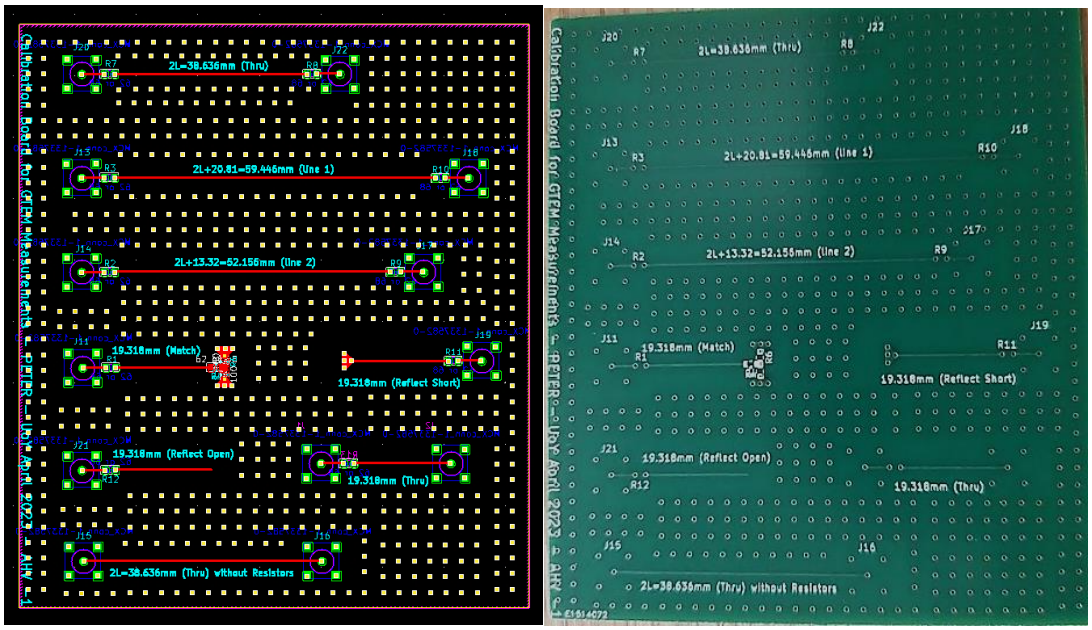

Figure 77: Shows the layout of the TRL calibration board for the GTEM board from KiCAD.

6.8 Lessons Learnt During PCB Design for RF IC Detector

Different substrate heights for transmission lines can be implemented on a single PCB board to achieve impedance matching. Utilizing ground vias in unoccupied spaces is crucial for maintaining a continuous ground plane, enhancing EM shielding and signal integrity. The orientation of PCB traces plays a key role in immunity measurements, influenced by the testing environment. Including dummy metal layers connected to ground helps balance the plating index, preventing issues like warping or uneven plating. For accurate knowledge of the dielectric properties, it is advisable to request the PCB passport from the manufacturer.

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7. Conducted Coupling and Impedance Analysis at RF IC Detector Package Pins

Previous discussions in Chapter 4 covered power absorption in a single PCB track (Section 4.1) and the interaction between package pins, considering changes in pin positions (Section 4.2) in radiated environments. This chapter focuses on investigating direct coupling into the package pins of the IC connected via test PCB tracks in a non-radiated environment. We introduce a methodology for measuring conducted coupling into an RF IC detector and determining the realistic load impedance at the IC's package pins using the conducted board's test bench setup.

The conducted board test bench setup (discussed in Section 6.5), offers an opportunity to examine realistic load impedances at IC package pins connected to test RF PCB tracks, including the cross-coupling between adjacent PCB tracks and IC package pins. Our investigation begins with S-parameter measurements following TOSM (Through-Open-Short-Match) calibration at the MCX connectors of the RF IC detector. Utilizing TRL/M calibration, we obtain S-parameters at the package pins, effectively removing the influence of the RF PCB track between the MCX connector and RF IC detector. This allows the calculation of the input impedance at the package pins under different power conditions of the test bench (on and off). Subsequently, we discuss the Direct Power Injection (DPI) measurement, evaluating the detector's input sensitivity across its operating frequency band by injecting known forward power levels. This process establishes a calibration map for radiated measurements using the RF IC detector in forthcoming chapters.

Further exploration delves into investigating the interaction among multiple MCX connectors, RF PCB tracks, and package pins of the RF IC detector. This exploration offers insights into how these components interact and affect overall performance. Finally, we replicate all measurements and calculations for the radiated board and GTEM board to assess process variation between different RF IC detectors. It is crucial to note that this chapter primarily focuses on direct coupling rather than radiated coupling, providing valuable insights into conducted coupling at the package pins of the RF IC detector and enhancing our understanding of factors influencing their performance.

7.1 S-parameter Measurement of Conducted Board

The main purpose of S-parameter measurement is to calculate the impedance at the package pins of the IC, monitor the reflections and transmissions at these pins, and investigate the influence of PCB tracks and cross-coupling between them.

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Detailed information regarding the conducted board's test bench setup can be found in Chapter 6, Section 6.5. Figure 78 showcases pictures of the assembled conducted board's test bench, featuring all three boards: the top conducted board, middle board, and bottom control board. A supporting white structure is visible between the top and bottom boards. Table 17 provides information about the RF IC detector package pins that are connected to the RF PCB tracks and MCX connectors for conducting S-parameter measurements.

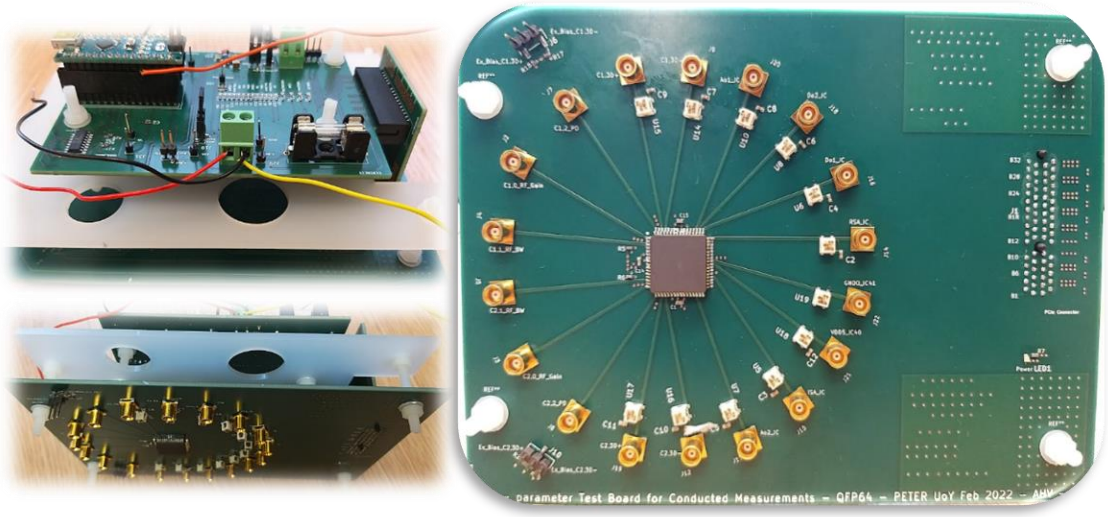

Figure 78: Shows the pictures of the conducted board's test bench

The measurement setup shown in Figure 79 includes a VNA, with port 1 or port 2 used to measure the S-parameters of all associated pins of the RF IC detector, while the remaining port is left unconnected. The RF IC detector testbench and VNA are monitored by a computer. The detailed working principle of the RF IC detector is presented in Chapter 5, specifically in Section 5.4.

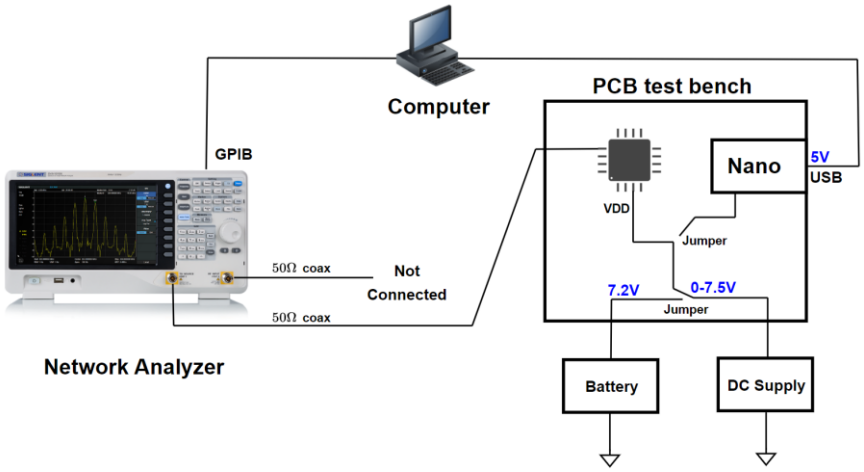

Figure 79: Shows the S-parameter measurement setup.

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7.1.1 Reference Plane at MCX adaptor after TOSM Calibration

Initially, TOSM calibration is performed using a ZV-Z235 calibration kit for the Rhode & Schwarz VNA ZVB20 [55]. This calibration enables us to set the reference plane of the VNA at the ends of the coaxial cables utilized in the measurement. Subsequently, one end of a coaxial cable connected to port 1/port 2 of the VNA is connected to an MCX female-to-male adaptor, establishing a connection between one of the MCX connector of the conducted board and the coaxial cable linked to the VNA. The other coaxial cable connected to port 2/port 1 of the VNA remains unconnected. The accuracy of the TOSM calibration can be assessed by referring to Appendix 11.3.1. The measurement is conducted when the conducted test bench power is on.

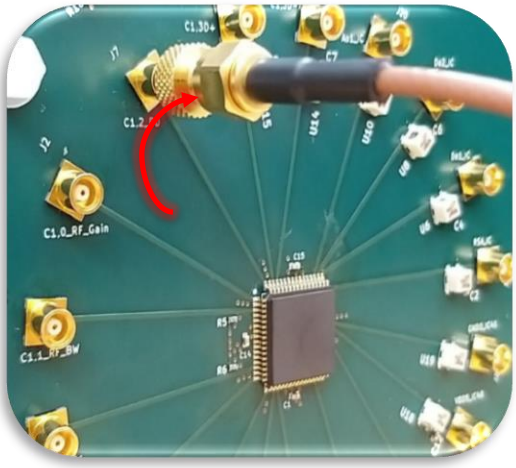

Figure 80: Shows that one of the MCX connectors from the conducted board connected to the SMA cable via the MCX adaptor. The other end of the SMA cable is connected to one of the ports of the VNA (not shown). The red arrow indicates the reference plane set for the VNA after TOSM calibration.

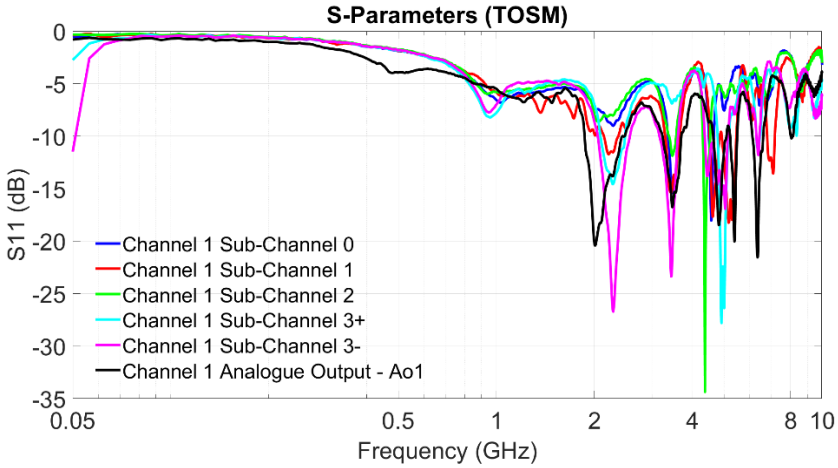

Figure 81: Shows the S11 of channel 1 at MCX connectors of the RF IC detector.

The reference plane of the VNA is located at the end of the coaxial cable, as shown in Figure 80. Figure 81 and Figure 82 display the S11 measured at MCX connectors connected

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to input and output pins (channel 1 and channel 2) of the RF IC detector via PCB tracks. To ensure efficient signal transmission and reception, it is desirable to achieve maximum signal transmission with minimum reflections at these connectors. By examining the S11 shown in Figure 81 and Figure 82, we can observe that the reflection coefficient is approximately below -3 dB above 500 MHz. This indicates that there is approximately less than 50% reflection above this frequency point. The reason for the observed reflections in the RF IC detector input and output is attributed to transmission losses and impedance mismatch between the characteristic impedance of the PCB track and the impedance at the pin of the IC package. These measurement data will be used to calculate and compare the calculated input impedance at the package pins using a de-embedding method for both the GTEM and radiated board measurements. This is necessary because both the GTEM board and radiated board consist of RF PCB tracks with a characteristic impedance of 115 Ω, for which the TRL/M calibration is not accurate.

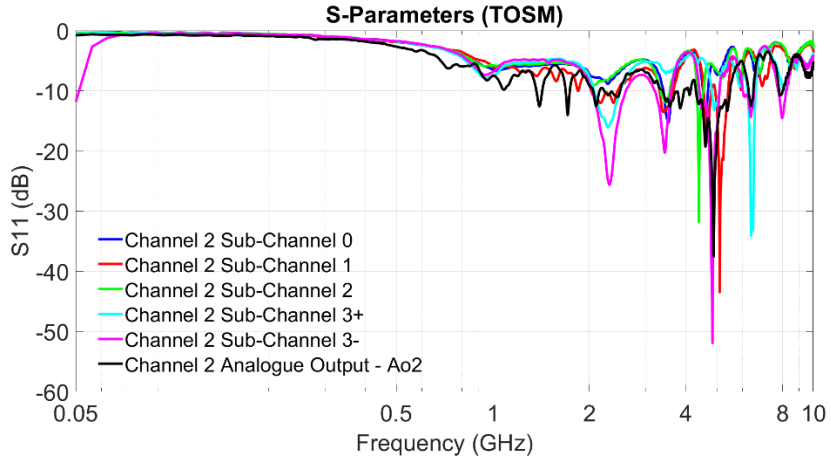

Figure 82: Shows the S11 of channel 2 at MCX connectors of the RF IC detector.

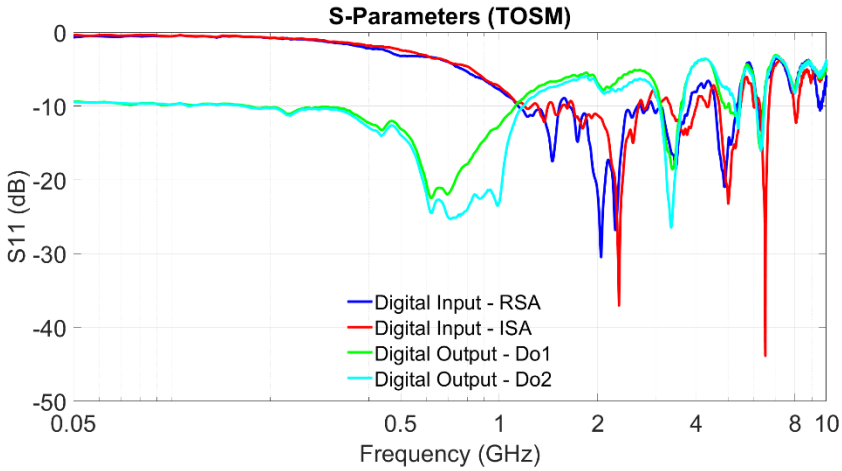

Figure 83: Shows the S11 of digital pins at MCX connectors of the RF IC detector.

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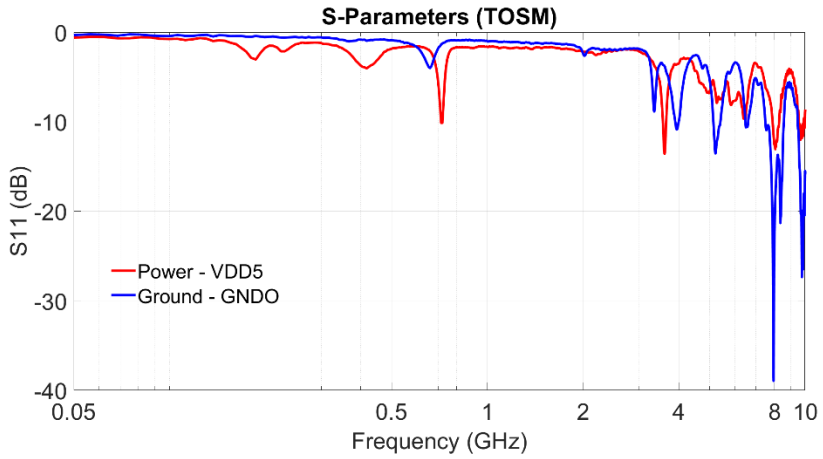

Figure 84: Shows the S11 of VDD5 and GNDO pins at MCX connectors of the RF IC detector.

Figure 83 shows the S11 of the digital input and output pins, which are responsible for transmitting and receiving digital signals. Given the binary nature of digital signals, represented by discrete voltage levels (0 and 1), the impact of reflections and losses on digital signals is expected to be less significant compared to analogue signals. The S11 shown in Figure 83 provide insights into reflections caused by transmission losses and impedance mismatch between the characteristic impedance of the PCB track and the impedance at the digital input and output pins of the IC package. Notably, observations during the measurement indicate that the digital state of input/output does not exhibit visible variations on the S11 parameter.

Figure 84, on the other hand, displays the S11 of the VDD5 and GNDO pins, representing the power and ground connections of the RF IC detector. Power and ground pins typically exhibit a more consistent impedance profile and lower coupling with surrounding components. This stability ensures consistent voltage levels across frequencies, minimizing signal distortion and enabling reliable power distribution in the circuit. Additionally, these connections demonstrate minimal coupling with neighbouring components, serving as stable references and power sources to mitigate unwanted interference in ICs and nearby elements. As a result, the variation in reflection observed for these pins is generally smaller compared to other signal pins. The S11 shown in Figure 84 help us understand the impedance characteristics and potential coupling effects associated with the power and ground connections.

7.1.1.1 Test Bench Power On and Off

The previous research conducted at the UoY indicated that the variation in ACS due to the power on, off and operating configuration of the DUT is negligible in a radiated environment [10]. Hence, in this section, we observe and study the variations in the reflection coefficient when the conducted test bench power is on and off when dealing with direct coupling in a non-radiated environment.

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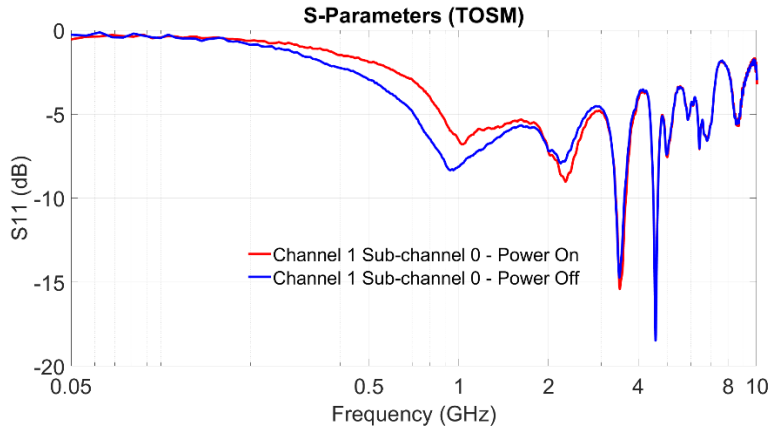

Figure 85: Shows the S11 of channel 1 sub-channel 0 (C1SC0 with RF amplifier) at MCX connectors when the power of the test bench is on and off.

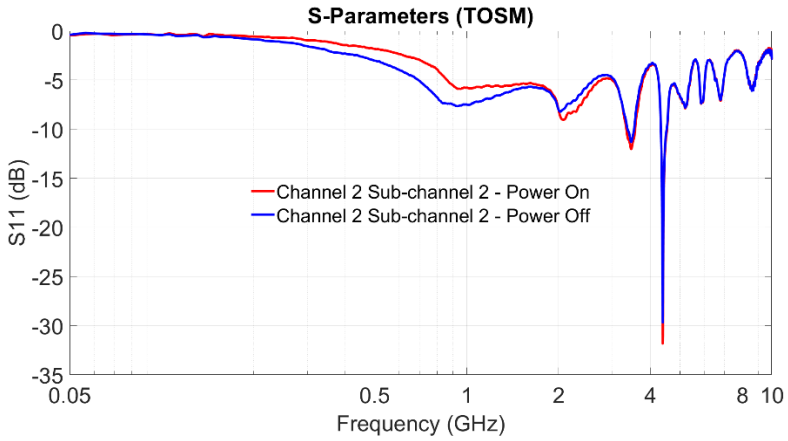

Figure 86: Shows the S11 of channel 2 sub-channel 2 (C2SC2 with only peak detector) at MCX connectors when the power of the test bench is on and off.

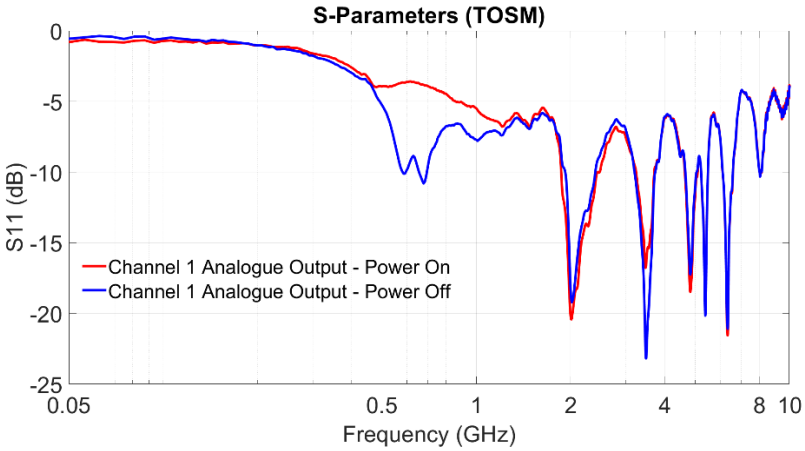

Figure 87: Shows the S11 of channel 1 analogue output (Ao1) at MCX connectors when the power of the test bench is on and off.

Figure 85 and Figure 86 demonstrate the variation due to power in reflection coefficient for channel 1 sub-channel 0 (C1SC0 with RF amplifier) and channel 2 sub-channel 2 (C2SC2 with only peak detector), respectively. The observed variation can be attributed

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to the influence of the RF IC detector itself. When the power is on, the active RF IC detector introduces additional impedance and coupling effects to the PCB track and connected pin, altering the impedance matching and signal propagation characteristics. This, in turn, leads to changes in the observed reflection coefficient.

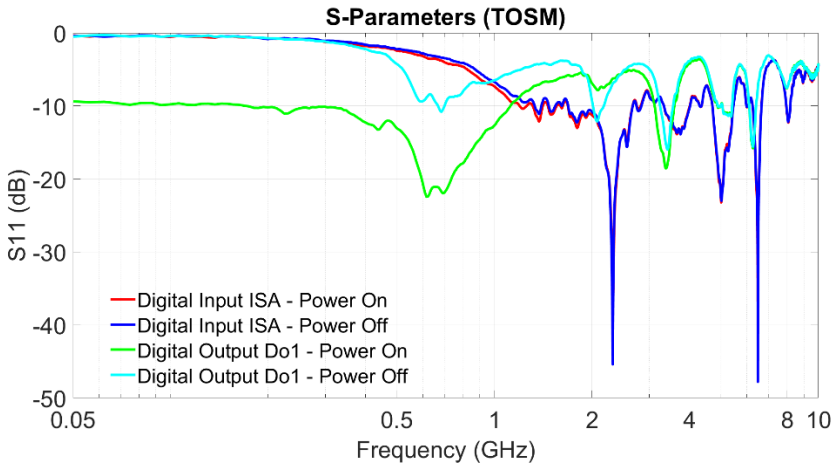

Figure 88: Shows the S11 of digital input and output at MCX connectors when the power of the test bench is on and off.

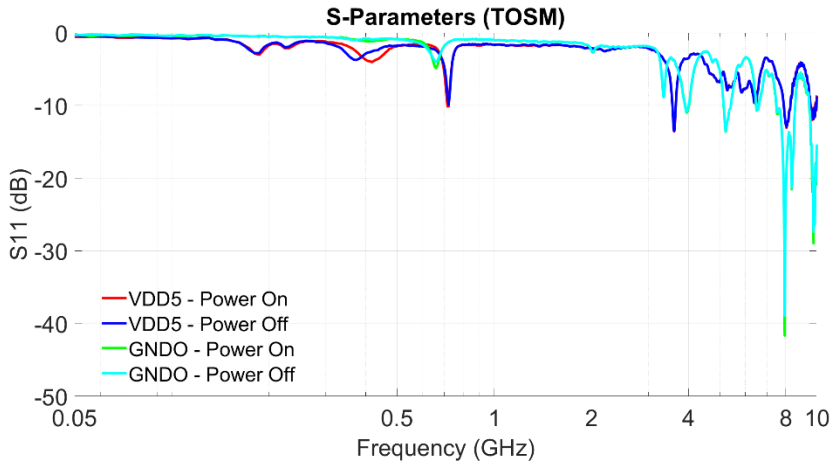

Figure 89: Shows the S11 of VDD5 and GNDO at MCX connectors when the power of the test bench is on and off.

Furthermore, the variation in the reflection coefficient depends on the inner circuitry of the RF IC detector and the PADs used in the PAD ring. Figure 87, Figure 88, and Figure 89 show different variations for different pins in the RF IC detector. For example, in Figure 87, the variation is observed between 450 MHz and 1.5 GHz for channel 1 analogue output. In Figure 88, the variation in digital output is significant, particularly at initial frequencies up to 3.5 GHz. However, VDD and GNDO pins exhibit minimal variation (Figure 89) due to their well-defined and stable reference potential, consistent impedance profile, and lower coupling with surrounding components.

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These variations due to power on and off of the test bench will be further discussed in the context of radiated measurements during the calculation of the Quality factor (Q-factor) of the reverberation chamber in the upcoming chapter (Section 8.3.2.1).

7.1.2 Reference Plane at Package Pin after TRL/M Calibration

In our case, we perform a combination of TRM (low-frequency) and TRL (high-frequency) calibration to cover the desired frequency range of calibration. The design details of the TRL/M board and the significance of each standard (Through, Line 1, Line 2, Match, and Reflect) are presented in Section 6.5.2. All the necessary information, including the length, characteristic impedance, and frequency range for each standard, is incorporated in the user-defined calibration kit of the Rhode & Schwarz VNA ZVB20 [55]. TRL/M calibration is then performed based on this setup, which provides accurate calibration up to 3 GHz. After TRL/M calibration, the reference plane is set at the package pin, and the S-parameter measurement procedure remains unchanged, as explained in the previous section 7.1.2. The accuracy of the TRL/M calibration can be assessed by referring to Appendix 11.3.2. The measurement is conducted when the conducted board test bench power is on.

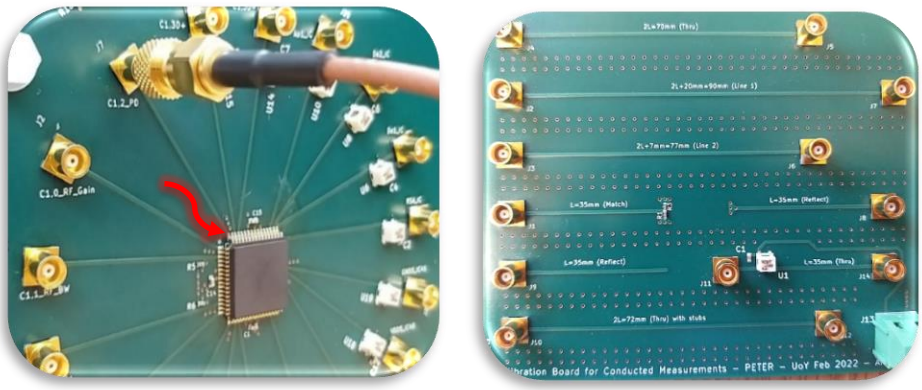

Figure 90: In the left picture the red arrow indicates the reference plane set for the VNA after TRL calibration. The right picture shows a fabricated TRL calibration board built for the conducted board.

After TRL/M calibration, the reference plane of the VNA is adjusted to the end of the RF PCB track connected to the RF IC detector package pin, as shown in Figure 90. In other words, the influence of the RF PCB track has been removed after TRL/M calibration. The reflections due to the RF PCB tracks may interact with each other, leading to constructive or destructive interference, which can result in an overall increase or reduction in the reflection observed at the MCX connector. As shown in Figure 91, for channel 1 sub-channel 0 and sub-channel 1 (C1SC0 and C1SC1), the reflections have increased between 800 MHz and 1.8 GHz and between 1.9 GHz and 3 GHz after TRL/M calibration. However, initially, from 50 MHz to 800 MHz and from 1.8 GHz to 1.9 GHz, the reflection

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coefficient after TRL/M calibration remains consistent with the results obtained from TOSM calibration.

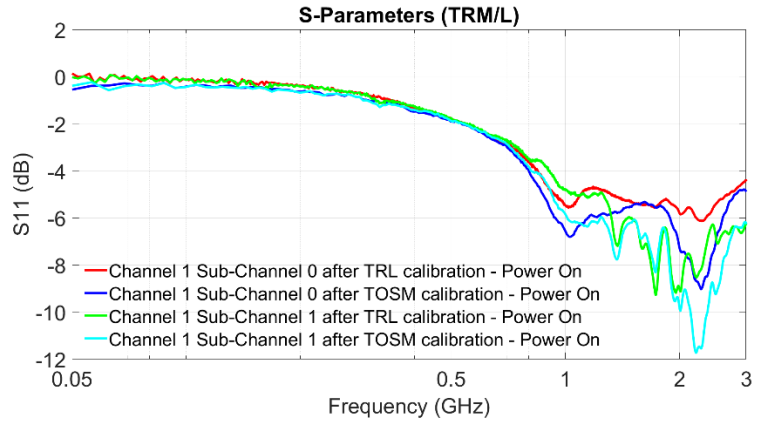

Figure 91: Shows the S11 comparison of channel 1 sub-channel 0 (C1SC0) at package pins after TRL/M and TOSM calibration.

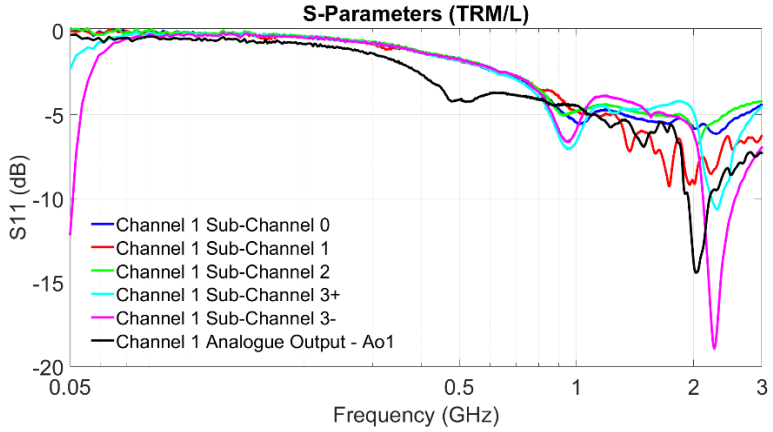

Figure 92: Shows the S11 of channel 1 at package pins of the RF IC detector after TRL calibration.

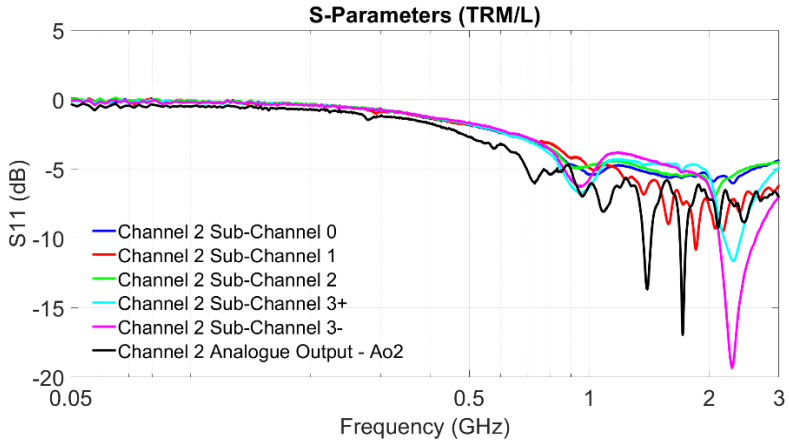

Figure 93: Shows the S11 of channel 2 at package pins of the RF IC detector after TRL/M calibration.

The observed variations in the reflection coefficients after TRL/M calibration indicate the influence of the calibration technique on the measurement results. The interaction of reflections from different parts of the RF PCB track and RF IC detector can lead to complex

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signal behaviours, affecting the overall impedance and signal propagation characteristics. The increase in reflection at specific frequency ranges suggests the presence of resonances or impedance mismatch regions in the RF PCB track, which become more prominent after TRL/M calibration.

Figure 92 to Figure 95 display the S11 of the input channels, output channels, digital pins, and power pins of the RF IC detector at the package pins after TRL/M calibration. These measurement data will be used to calculate the input impedance at the package pins and compare it with the impedance calculated at the MCX connector. Additionally, we will compare the calculated impedance using the de-embedding method for both the GTEM and radiated board measurements.

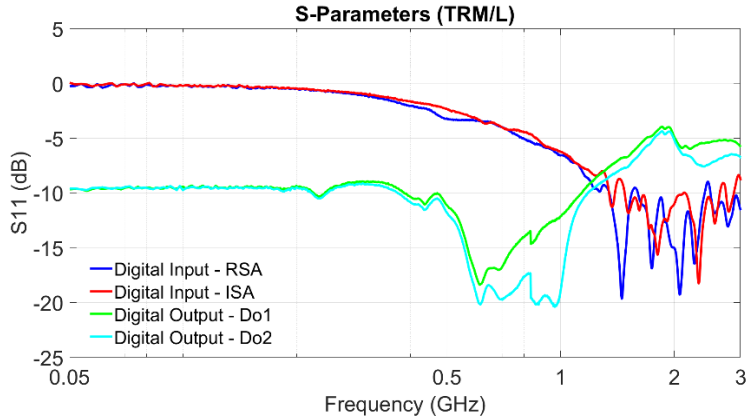

Figure 94: Shows the S11 of digital pins of the RF IC detector after TRL/M calibration.

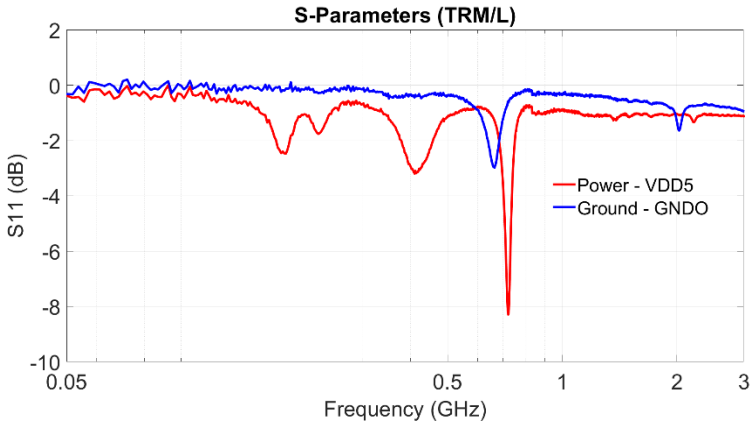

Figure 95: Shows the S11 of VDD5 and GNDO pins of the RF IC detector after TRL/M calibration.

7.1.2.1 Test Bench Power On and Off

After TRL/M calibration, we have the opportunity to examine the effects of the RF IC detector package pins when the conducted test bench power is turned on and off. As discussed in Section 7.1.1.1, we observe and study the variations in the reflection coefficient when the conducted test bench power is on and off.

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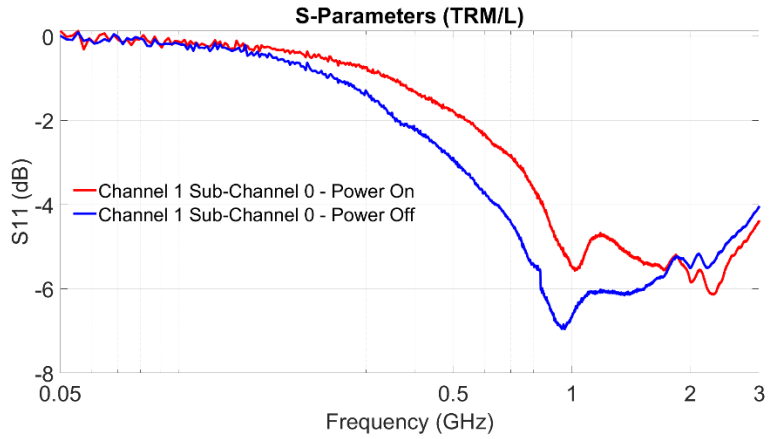

Figure 96: Shows the S11 of channel 1 sub-channel 0 (C1SC0 with RF amplifier) at package pins when the power of the test bench is on and off.

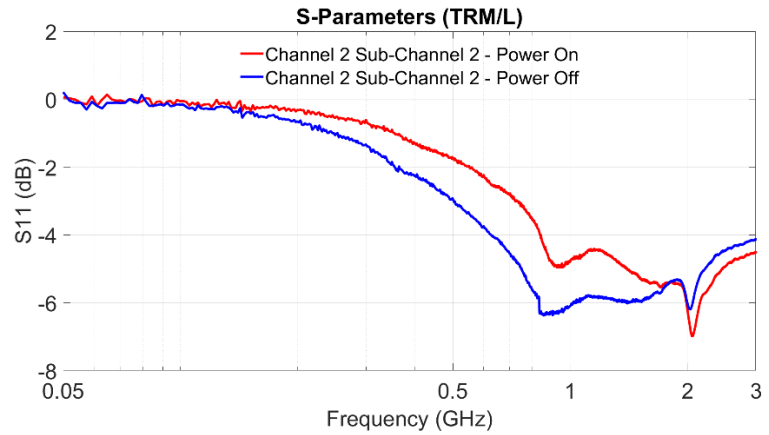

Figure 97: Shows the S11 of channel 2 sub-channel 2 (C2SC2 with only peak detector) at package pins when the power of the test bench is on and off.

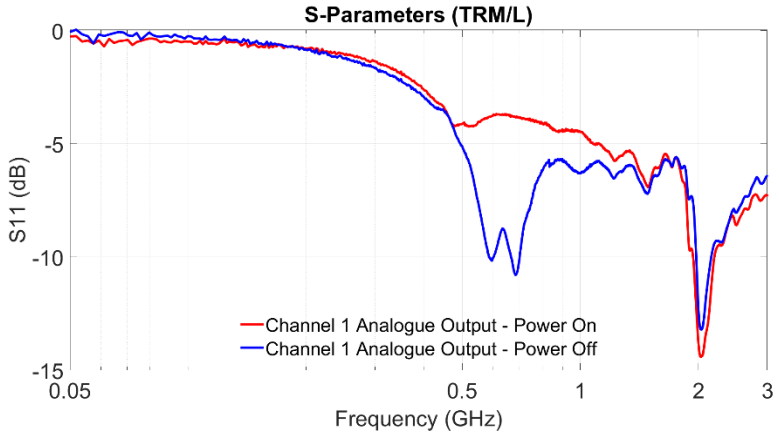

Figure 98: Shows the S11 of channel 1 analogue output (Ao1) at package pins when the power of the test bench is on and off.

Figure 96 to Figure 100 illustrate the variations in the reflection coefficient for different pins of the RF IC detector when the conducted board test bench power is on and off. The reasons for these variations remain the same as explained in Section 7.1.1.1.

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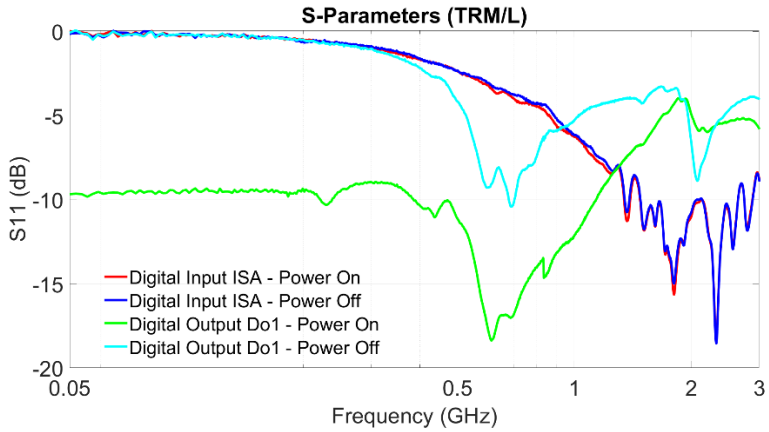

Figure 99: Shows the S11 of digital input and output at package pins when the power of the test bench is on and off.

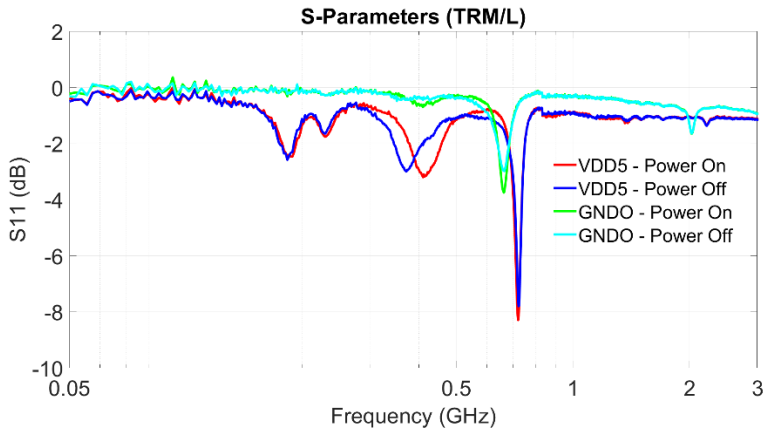

Figure 100: Shows the S11 of VDD5 and GNDO at package pins when the power of the test bench is on and off.

7.1.3 Influence of RF PCB tracks

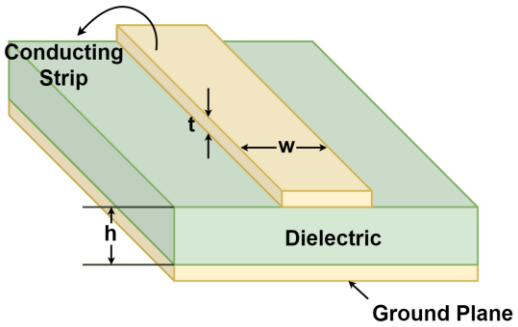

Figure 101: Shows the RF microstrip TL on PCB.

In this section, we investigate the importance of eliminating the influence of RF PCB tracks using TRL/M calibration. PCB tracks will have different types of losses such as conductor loss, dielectric loss, mismatch loss, radiated loss, and other leakage losses. All these losses will be investigated in this section. Considering and removing all the losses due

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to RF PCB tracks is really important to get accurate measurement results from the RF IC detector.

7.1.3.1 Analytical Model to Calculate the PCB Attenuation

a) Conductor Loss (Ohmic Losses)

The conductor loss in a microstrip TL, also known as Ohmic Losses, primarily arises from resistive losses in the copper traces. It is a significant factor in the overall loss of the TL. Various methods, including empirical equations and EM simulations, can be used to estimate the conductor loss. A simple expression to calculate conductor loss can be found in [59].

$$\alpha_c = \frac{R_s}{Z_c w}\ Np/m \tag{45}$$

where w is the width of the trace, R_s is the surface resistance of the trace, and Z_c represents the characteristic impedance.

However, for improved accuracy, we have utilized the equations from [60] with slight modifications to account for frequency dependence, as shown below.

$w/h \le 1/2\pi$:

$$\alpha_c(f) = \frac{R_s(f)}{2\pi \cdot Z_c(f) \cdot h}\left[1-\left(\frac{w_0}{4h}\right)^2\right]\left\{1+\frac{h}{w_0} + \frac{h}{\pi w_0}\left[ln\left(\frac{4\pi w}{t}+1\right)-\frac{1-{}^{t}/_{w}}{1+{}^{t}/_{4\pi w}}\right]\right\}\ Np/m,$$

$1/2\pi < w/h \le 2$:

$$\alpha_c(f) = \frac{R_s(f)}{2\pi \cdot Z_c(f) \cdot h}\left[1-\left(\frac{w_0}{4h}\right)^2\right]\left\{1+\frac{h}{w_0} + \frac{h}{\pi w_0}\left[ln\left(\frac{2h}{t}+1\right)-\frac{1-{}^{t}/_{w}}{1+{}^{t}/_{2h}}\right]\right\}\ Np/m, \tag{46}$$

$w/h > 2$:

$$\alpha_c(f) = \frac{R_s(f)}{Z_c(f) \cdot h\left\{\frac{w_0}{h}+\frac{2}{\pi}ln\left[2\pi e\left(\frac{w_0}{2h}+0.94\right)\right]\right\}^2}\left[\frac{w_0}{h} + \frac{{}^{w_0}/_{\pi h}}{{}^{w_0}/_{2h}+0.94}\right] \cdot\left\{1+\frac{h}{w_0}+\frac{h}{\pi w_0}\left[ln\left(\frac{2h}{t}+1\right)-\frac{1+\frac{t}{h}}{1+\frac{t}{2h}}\right]\right\}\ Np/m$$

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where h represents the height of the trace from the ground plane, t denotes the thickness of the trace, $R_s(f)$ represents the frequency-dependent surface resistance of the trace, $Z_c(f)$ denotes the frequency-dependent characteristic impedance, and w_0 is given by,

$$w_0 = \begin{cases} w + \frac{t}{\pi} ln\left(\frac{4\pi w}{t} + 1\right) & \frac{w}{h} \leq \frac{1}{2\pi} \\ w + \frac{t}{\pi} ln\left(\frac{2h}{t} + 1\right) & \frac{w}{h} \geq \frac{1}{2\pi} \end{cases} \tag{47}$$

$$R_s(f) = \frac{1}{\sigma \delta_s(f)}$$
$$\delta_s(f) = \sqrt{\frac{2}{\omega \mu \sigma}} \tag{48}$$

where $\omega = 2\pi f$ is the angular frequency, $\mu = \mu_r \mu_o$ is permeability, δ_s and σ are the skin depth and conductivity of the copper.

There are various methods available for calculating the characteristic impedance and effective permittivity. In this study, the expression is slightly modified for characteristic impedance based on [59] and [39] to incorporate frequency dependency. The modified expression is shown below.

$$Z_c(f) = \begin{cases} \frac{60}{\sqrt{\varepsilon_{r\_\text{eff}}(f)}} ln\left(\frac{8h}{w_{\text{eff}}} + \frac{w_{\text{eff}}}{4h}\right) & \frac{w}{h} \leq 1 \\ \frac{120\pi}{\sqrt{\varepsilon_{r\_\text{eff}}(f)}} \left[\frac{w_{\text{eff}}}{4h} + 1.393 + 0.667\, ln\left(\frac{w_{\text{eff}}}{4h} + 1.444\right)\right]^{-1} & \frac{w}{h} \geq 1 \end{cases}$$

$$\frac{w_{\text{eff}}}{4h} = \frac{w}{h} + \frac{\frac{1.25t}{h}}{\pi} \cdot \begin{cases} 1 + ln\left(4\pi \frac{\frac{w}{h}}{\frac{t}{h}}\right) & \frac{w}{h} \leq \frac{1}{2\pi} \\ 1 + ln\left(\frac{2}{\frac{t}{h}}\right) & \frac{w}{h} \geq \frac{1}{2\pi} \end{cases} \tag{49}$$

where $\varepsilon_{r\_\text{eff}}$ is the effective permittivity of the microstrip TL.

The relative effective permittivity equation from [39], has been modified to incorporate frequency dependence and is expressed as follows.

$$\varepsilon_{r\_eff}(f) = \frac{\varepsilon_r'(f) + 1}{2} + \frac{\varepsilon_r'(f) - 1}{2}\left(1 + \frac{10}{w/h}\right)^{-1/2} - \frac{\varepsilon_r'(f) - 1}{4.6}\frac{t/h}{w/h} \tag{50}$$

The frequency-dependent real ($\varepsilon_r'(f)$) and imaginary ($\varepsilon_r''(f)$) parts of the relative permittivity of the dielectric can be calculated as shown in Appendix 11.7.1. Substituting

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equations (48) and (49) into equation (46) yields us the conductor loss of the RF PCB track.

b) Dielectric Loss

We utilize the equations from [60] and [59] to determine the dielectric losses, and have made modifications to incorporate frequency dependence, as shown below.

$$\alpha_d(f) = \frac{\pi}{\lambda_0}\frac{\varepsilon_r}{\varepsilon_r - 1}\cdot\frac{\varepsilon_{\text{eff}} - 1}{\sqrt{\varepsilon_{\text{eff}}}}\cdot tan(\delta) \quad Np/m \tag{51}$$

where, λ_0 represents the absolute wavelength of free space.

c) Losses in Microstrip using RLGC model

By referring to RLGC (Resistance, Inductance, Conductance, Capacitance) models from [61] and [62], we can derive the RLGC equations as presented in this section. The characteristic impedance can be expressed in terms of RLGC parameters as shown below.

$$Z_c(f) = \sqrt{(R + j\omega L)\cdot(G + j\omega C)^{-1}} \tag{52}$$

here, R, L, G, and C represent the per-unit-length (p.u.l.) resistance, inductance, conductance, and capacitance of a single PCB trace, which are components of the RLGC model. The frequency-dependent complex propagation constant, expressed in terms of p.u.l. R, L, G, and C, are given by the following equation.

$$\gamma(f) = \sqrt{(R + j\omega L)(G + j\omega C)} = \alpha + j\beta \tag{53}$$

where β represents the phase constant and α represents the attenuation factor. The real part of γ provides us with the total attenuation of the microstrip trace, taking into account both ohmic losses and dielectric losses.

$$Re\{\gamma\} = \alpha_c + \alpha_d \tag{54}$$

The frequency-dependent p.u.l. conductance G is given by:

$$G(f) = 2\pi f \cdot tan\,\delta \cdot C \tag{55}$$

where $tan\,\delta = \varepsilon_r''/\varepsilon_r'$ is the loss tangent where ε_r' and ε_r'' are the real and imaginary parts of the relative permittivity of the dielectric. The frequency-dependent real $(\varepsilon_r'(f))$ and imaginary $(\varepsilon_r''(f))$ parts of the relative permittivity of the dielectric can be calculated as shown in Appendix 11.7.1.

The frequency-dependent p.u.l. resistance R, without including the roughness effect, is given by [62], [63]:

$$R(f) = \begin{cases} R_s(f)\left(\frac{1}{w} + \frac{1}{b}\right), & \delta_s(f) < t \\ \frac{2}{\sigma t}\left(\frac{1}{w} + \frac{1}{b}\right), & \delta_s(f) \geq t \end{cases} \tag{56}$$

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where b is the width of the ground plane. $\delta_s(f)$ and $R_s(f)$ represent the skin depth of the copper and the surface resistance, respectively, which can be obtained from equation (48). The frequency-dependent per-unit-length (p.u.l.) resistance $R_{rough}(f)$, taking into account the roughness effect using the Hemispherical Method, is given by [62], [63]:

$$R_{rough}(f) = \begin{cases} K_r R_s(f)\left(\frac{1}{w}+\frac{1}{b}\right), & \delta_s(f) < t \\ \frac{2}{\sigma t}\left(\frac{1}{w}+\frac{1}{b}\right), & \delta_s(f) \geq t \end{cases} \qquad (57)$$

$$K_r = \begin{cases} 1, & K_s \leq 1 \\ K_s, & K_s > 1 \end{cases}$$

where, K_r is the coefficient for the roughness effect. The detailed equations for K_r and K_s can be found in Appendix 11.7.2.

From [64], we can derive the simplified form of the p.u.l inductance (L_T) and capacitance (C) equations for a single PCB track, as shown below.

$$C = \varepsilon_o \varepsilon_r' \left[1.15\left(\frac{w}{h}\right)^{0.963} + 1.07\left(\frac{t}{h}\right)^{0.049}\right]$$
$$L_T = \mu_o \left[3.71\left(\frac{h}{w}\right)^{0.041} + 0.018\left(\frac{h}{w}\right)^{-0.73} - \left(\frac{h}{t}\right)^{-0.0006}\right] \qquad (58)$$

By substituting equations (55), (57) and (58) into equations (52) and (53), we can determine the characteristic impedance and the propagation constant of the single PCB track respectively.

7.1.3.2 Radiation Loss and Mismatch Loss

To investigate radiation loss from the RF PCB track, a CST simulation was performed for a 70 mm track using PEC (Perfect Electric Conductor) material with no conductor loss or dielectric loss. By excluding mismatch loss and assuming negligible leakage losses, the remaining loss is attributed solely to radiation loss.

The RF PCB track has a characteristic impedance and port impedance of 50 Ω. While the mismatch losses may be relatively small, they are not negligible. To calculate the mismatch losses (M_L) caused by impedance mismatch using the extracted S-parameters from CST for a 70 mm trace with PEC material, the following equation can be used.

$$M_L = (1 - |\Gamma_{PEC}|^2) \qquad (59)$$

where Γ_{PEC} is the reflection coefficient of the 70mm PEC track extracted from CST.

To separate the mismatch loss from the overall loss in the 70 mm track and determine the radiation loss (R_L), the following equation can be used:

$$R_L \approx \left(|T_{PEC}|^2 \Big/ (1 - |\Gamma_{PEC}|^2)\right) \qquad (60)$$

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where T_{PEC} is the transmission co-efficient of the 70mm PEC track extracted from CST.

Copper material was also used in the simulation for verification, and the determined radiated loss results matched those obtained with PEC material. It is important to note that other factors related to the material and environment should also be considered when determining radiation loss in practical scenarios.

7.1.3.3 RF PCB Track Attenuation Results

Figure 102: Shows the 70mm RF PCB track from the calibration board built for the conducted board.

Figure 103 illustrates the various losses associated with the 70 mm RF PCB track, including conductor loss, dielectric loss, mismatch loss, radiation loss, and total loss. It is evident from the figure that the loss attributed to the RF PCB track is significant and cannot be overlooked during conducted board measurements. Therefore, it is crucial to consider the influence of the RF PCB track during conducted measurements and take steps to eliminate it using TRL/M calibration or de-embedding methods.

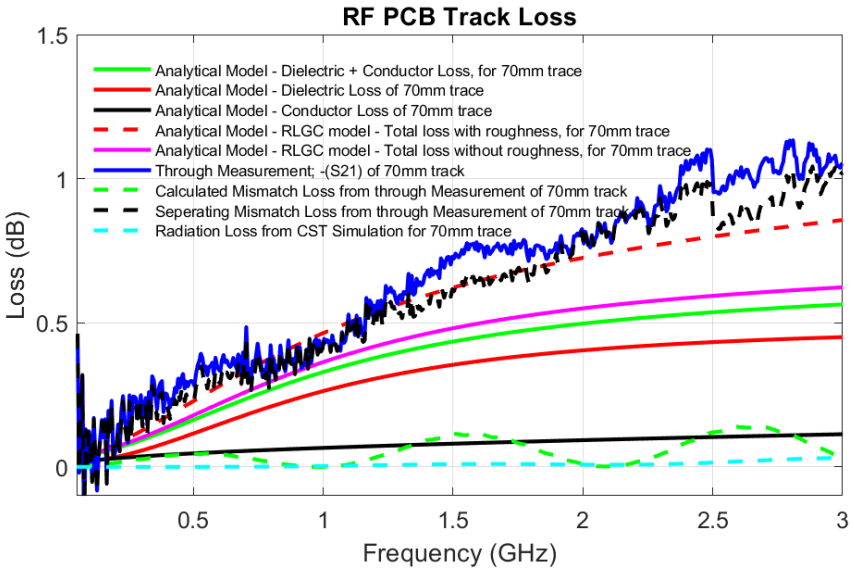

Figure 103: Shows the 70 mm RF PCB track losses with conducted board PCB parameters.

7.1.4 Cross-Coupling

7.1.4.1 Measuring cross-coupling after TOSM Calibration

In this section, we examine the cross-coupling phenomenon between adjacent MCX connectors and connected PCB traces on the conducted test bench. Cross-coupling, also known as crosstalk, refers to the unwanted transfer of signals or EMI between neighbouring

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TLs or circuits. In our case, we are examining the cross-coupling between MCX connectors and the RF PCB tracks that are positioned in close proximity on the conducted test bench. The primary objective of this investigation is to gain valuable insights into the extent of cross-coupling and determine whether it should be considered significant or negligible in our setup.

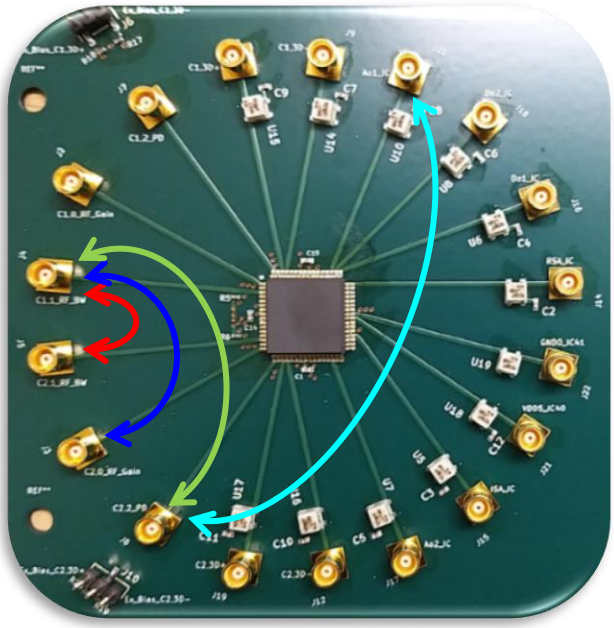

Figure 104: Shows the MCX connectors connected to RF PCB traces used to measure the cross-coupling between them in coloured arrow marks.

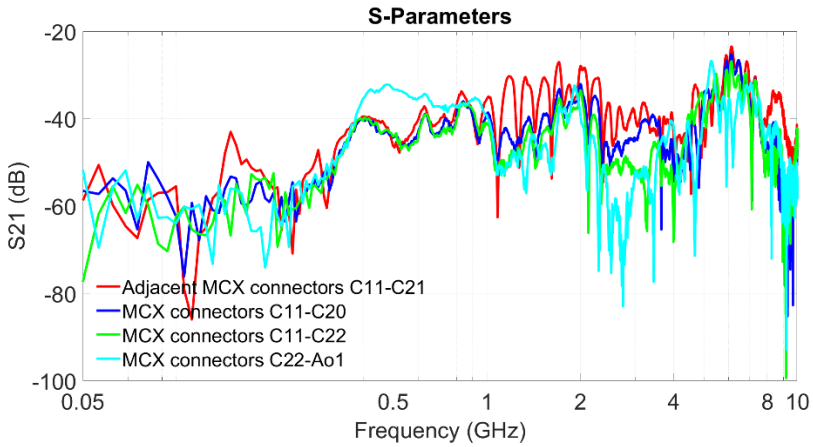

Figure 105: Shows the cross-coupling between different MCX connectors and connected RF PCB traces in the conducted test bench. SNM from the y-axis represents transmission co-efficient.

Figure 104 illustrates the specific MCX connectors that we used for measuring the cross-coupling phenomenon. Among the MCX connectors, we have marked the closest pair where cross-coupling is expected to be most prominent, and it is denoted by the red colour (Figure 104). The measured cross-coupling data for these selected MCX connectors are represented by the red curve in Figure 105. To ensure clarity and consistency, the chosen MCX

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connectors for cross-coupling measurement are marked with the same colour used in the graph representation (Figure 104 and Figure 105).

By analysing the results obtained from this investigation, we aim to draw meaningful conclusions about the significance of cross-coupling in our conducted test bench setup. The assessment of cross-coupling is crucial to ensure accurate and reliable measurements in subsequent testing and experimental work.

The coupling between the MCX connectors reduces as the distance between them increases, as evident from the red, blue, and green curves shown in Figure 105. Notably, the green curve and cyan curve exhibit similar levels of coupling, despite the cyan-coloured case having the MCX connectors placed far apart from each other. Overall, the coupling remains below -27 dB up to 7.5 GHz, indicating that only 0.19% of the signal is coupled in all cases. Importantly, the cross-coupling between the MCX connectors shows consistency for both power-on and power-off scenarios of the conducted test bench, as demonstrated in Figure 106. This suggests that the cross-coupling is independent of whether the test bench power is on or off.

In the context of our research work, the frequency of interest is below 3 GHz. Based on the findings, we can conclude that the cross-coupling between the MCX connectors and the adjacent PCB tracks is not significantly impactful. Therefore, for further considerations in upcoming measurements, we can safely neglect the influence of this cross-coupling phenomenon.

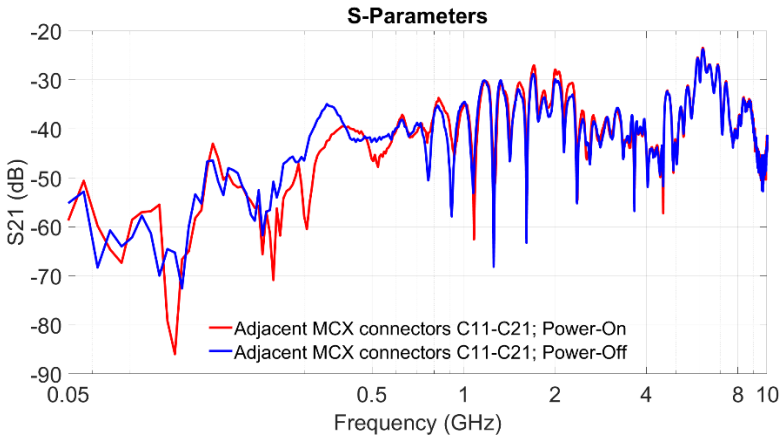

Figure 106: Shows the cross-coupling between MCX connectors and connected RF PCB traces when the power of the conducted test bench is on and off.

7.1.4.2 Measuring cross-coupling after TRL/M Calibration

TRL/M calibration only removes the influence of the RF PCB track under measurement, and it does not alter any cross-coupling influences between adjacent MCX connectors and RF PCB tracks. This can be observed from Figure 107, where the coupling remains the same as before, compared to the measurements performed after TOSM calibration. In other words, TRL/M calibration focuses solely on the characteristics of the individual RF

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PCB track and ensures that its influence is accurately accounted for in subsequent measurements. However, it does not address the cross-coupling effects between different components on the conducted test bench, such as adjacent MCX connectors and other PCB tracks.

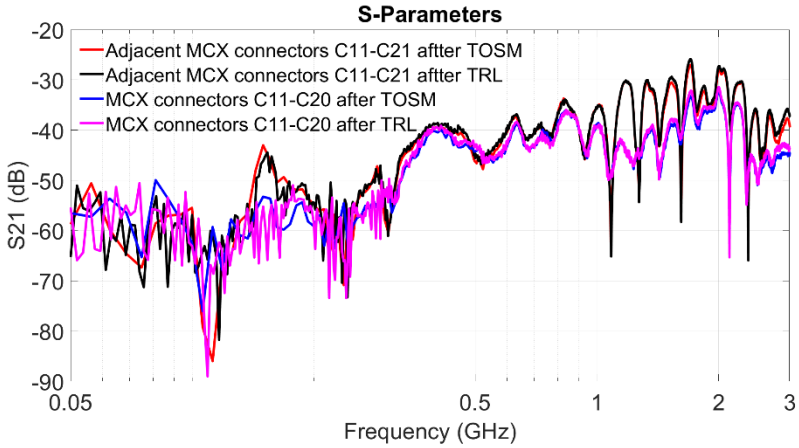

Figure 107: Shows the cross-coupling comparison between MCX connectors in the conducted test bench after TOSM and TRL/M calibration; N=2 (Port 2) and M=1 (Port 1) in y-axis.

7.1.5 Impedance Calculation

From the determination of the input impedance of the RF IC detector at the MCX connector and package pins, we can assess the amount of signal power that will be transferred at these points. This knowledge is essential for understanding the required input power range necessary at the RF IC detector's input package pins and calibrating the RF IC detector for radiated measurement.

After performing TOSM or TRL/M calibration, we can accurately determine the input impedance (Z_{in}) of the RF IC detector at the MCX connector and package pin, respectively using equation (61). This enables us to gain insights into the power absorbed at the MCX connector and package pin of the RF IC detector during the DPI measurement.

$$Z_{in} = Z_0 \frac{(1 + \Gamma_{11})}{(1 - \Gamma_{11})} \tag{61}$$

where, Γ_{11} is the reflection co-efficient measured after calibration at the MCX connector or package pin, and Z_0 is the characteristic impedance of the system.

Figure 108 and Figure 109 illustrate the comparison between the impedance calculated at the MCX connector after TOSM calibration and at the package pin of the RF IC detector after TRL/M calibration. The real part of the impedance represents the input resistance of Channel 1 Sub-Channel 0 (C1SC0) MCX connector or package pin (Figure 108), while the imaginary part of the impedance indicates the reactive component of the respective MCX connector or package pin (Figure 109).

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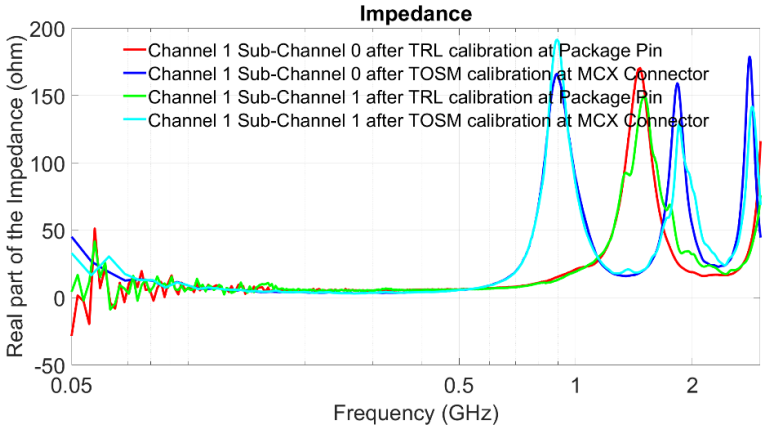

Figure 108: Show the real part of the impedance at the MCX connector and the package pin after TOSM calibration and TRL/M calibration respectively when the test bench power is on.

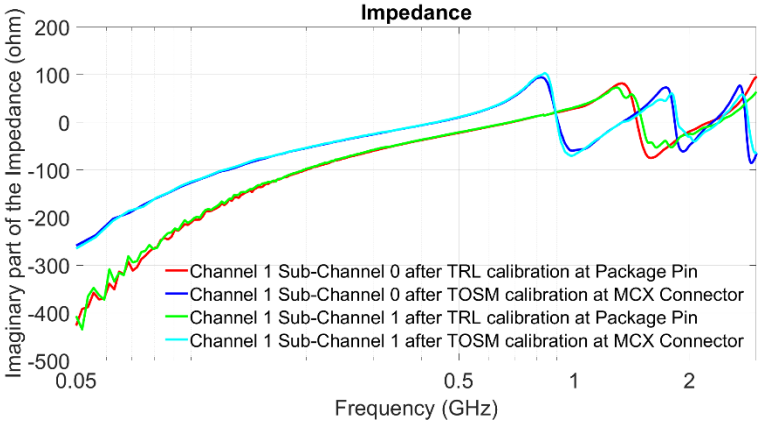

Figure 109: Shows the imaginary part of the impedance at the MCX connector and the package pin after TOSM calibration and TRL/M calibration respectively when the test bench power is on.

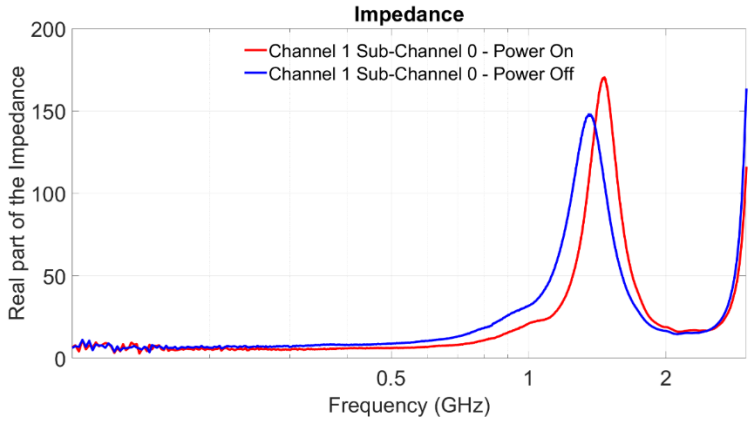

Figure 110: Show the real part of the impedance at the C1SC0 package pin when the conducted test bench power is on and off.

Observing the plots, we notice that until 500 MHz, the impedance of C1SC0 is more capacitive. Whenever there is a transition between inductive and capacitive behaviour in the imaginary part of the impedance (Figure 109), there is also a corresponding peak in the real part of the impedance at the same frequency point where the changeover occurs.

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At specific frequencies, the inductive and capacitive reactances counteract each other, leading to a net impedance that becomes purely resistive, where the real part dominates. These resonance frequencies correspond to points where the reactance becomes zero, resulting in the maximum value of the real part. Hence, we observe peaks in the real part of the impedance whenever there is a transition between inductive and capacitive behaviour in the imaginary part of the impedance.

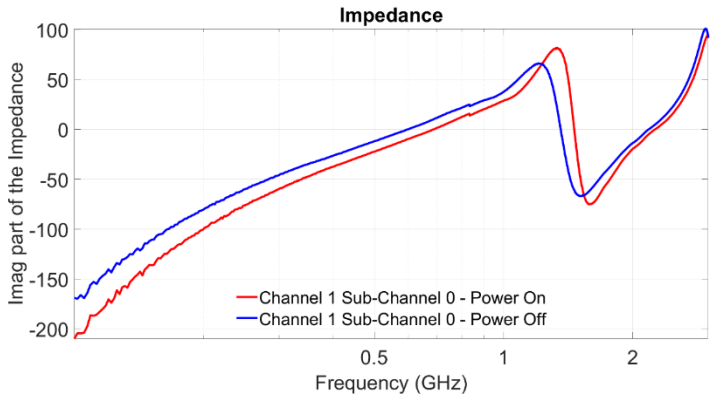

Figure 111: Show the imaginary part of the impedance at the C1SC0 package pin when the conducted test bench power is on and off.

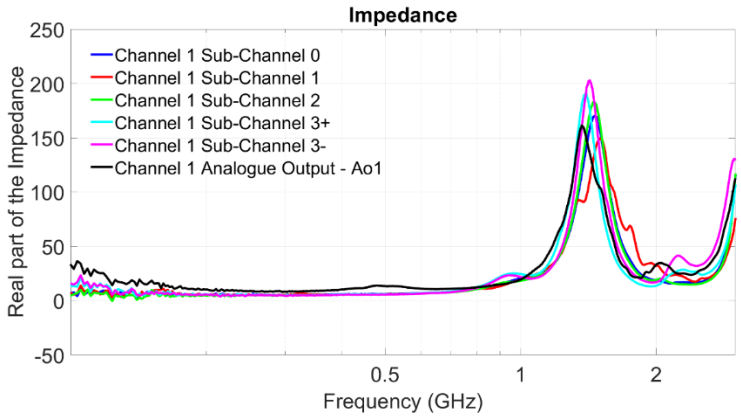

Figure 112: Show the real part of the impedance at the package pins of channel 1 of the RF IC detector.

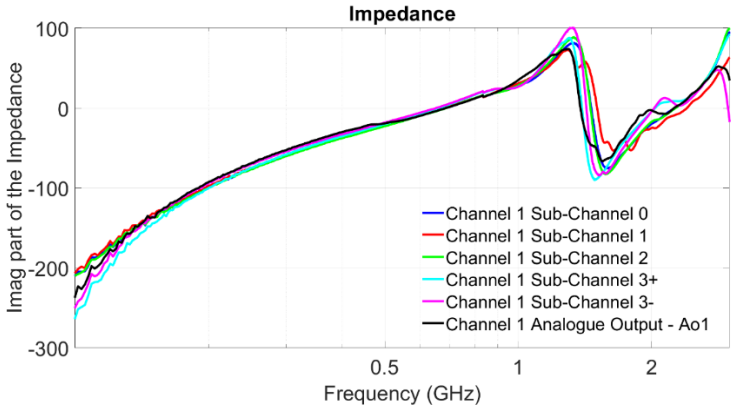

Figure 113: Show the imaginary part of the impedance at the package pins of channel 1 of the RF IC detector.

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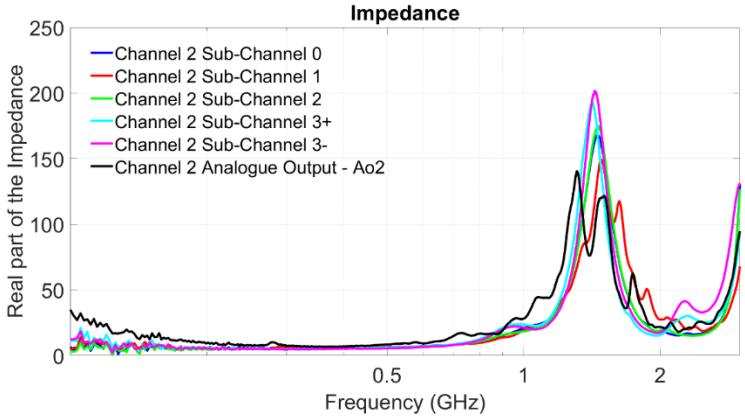

Figure 114: Show the real part of the impedance at the package pins of channel 2 of the RF IC detector.

From here, we will focus our discussion solely on the impedance at the package pins. The shift in the real part peak shown in Figure 110 and the transition points of the imaginary part of the impedance at the C1SC0 package pin shown in Figure 111 when the power of the conducted test bench is turned on is attributed to the active RF IC detector. When powered on, the detector introduces additional impedance and coupling effects to the PCB track and connected pin, causing alterations in impedance matching and signal propagation characteristics. Consequently, these changes lead to variations in the observed reflection coefficient. The influence of power supply noise and signal distortion further contributes to these alterations.

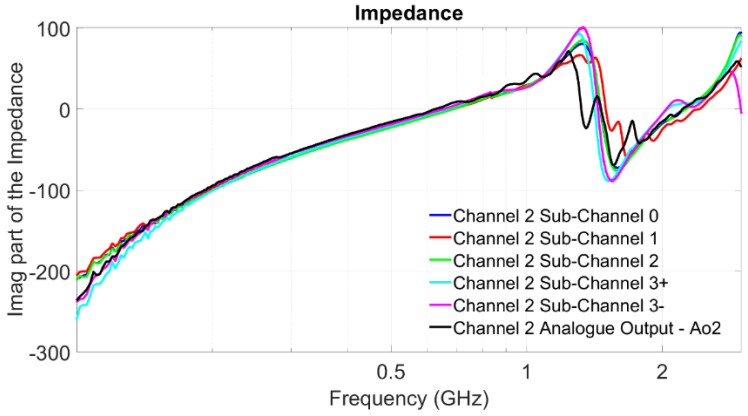

Figure 115: Show the imaginary part of the impedance at the package pins of channel 2 of the RF IC detector.

Figure 112 and Figure 113 display the input impedance of channel 1, while Figure 114 and Figure 115 illustrate the input impedance of channel 2 of the RF IC detector. It is observed that the impedance values of all the sub-channels within each channel are nearly identical, indicating consistent impedance behaviour across the sub-channels.

Moving on to the digital pins of the RF IC detector, their input impedance is shown in Figure 116 and Figure 117. The impedance characteristics of digital pins are also of interest since they are responsible for transmitting and receiving digital signals.

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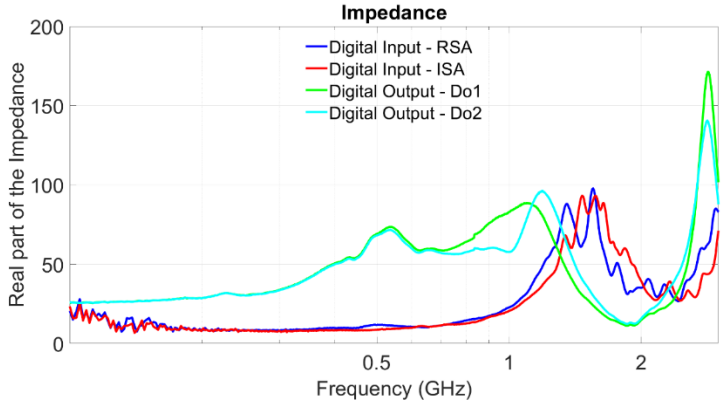

Figure 116: Show the real part of the impedance at the digital package pins of the RF IC detector.

Furthermore, the input impedance of the power pins, VDD and GNDO, is shown in Figure 118 and Figure 119, respectively. Power and ground pins are critical components that provide stable reference potentials and proper functioning of the RF IC detector. It is observed that the impedance profile for these pins is consistent and exhibits lower coupling with surrounding components. As a result, the variation in impedance is generally smaller for power and ground pins compared to other signal pins.

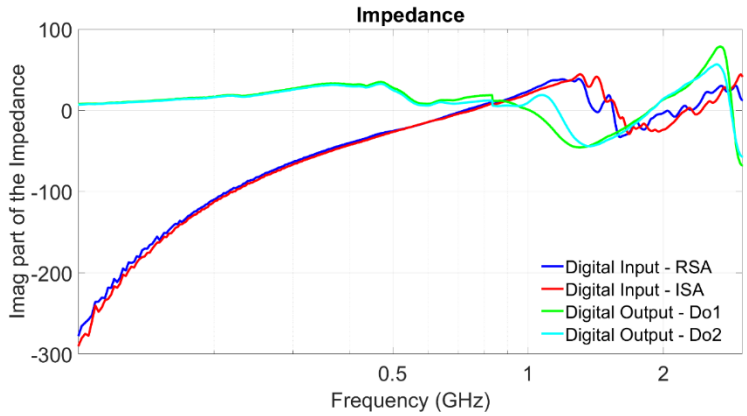

Figure 117: Show the imaginary part of the impedance at the digital package pins of the RF IC detector.

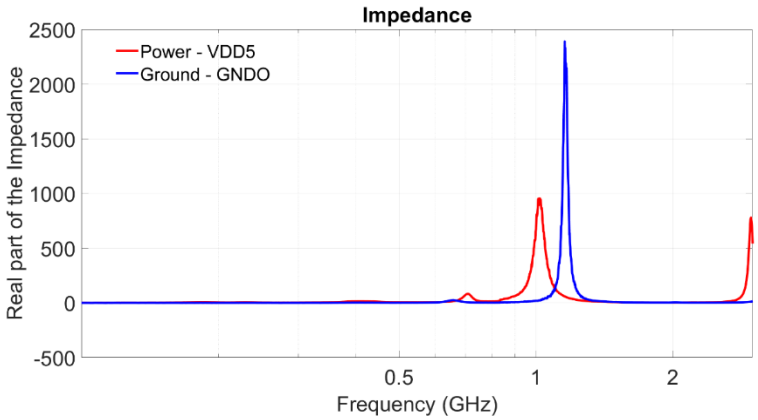

Figure 118; Shows the real part of the impedance at the VDD5 and GNDO package pins of the RF IC detector.

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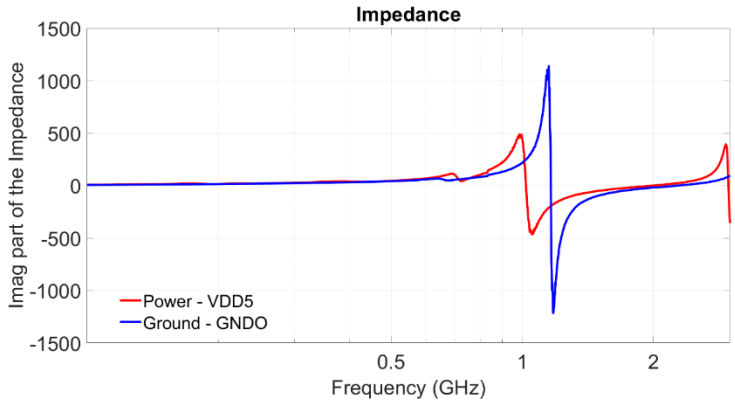

Figure 119: Show the imaginary part of the impedance at VDD5 and GNDO package pins of the RF IC detector.

7.2 Direct Power Injection Measurement for Conducted Board

As discussed in Chapter 5, the RF IC detector comprises inputs with varying sensitivity levels, which are determined by the specific amplification circuits used in its design. Consequently, different power levels are required at the input for proper detection by each of these inputs. To facilitate the DPI testing, each input of the RF IC detector is connected to an RF PCB test track with a characteristic impedance of 50 Ω, as described in Section 6.5.

The primary objective of conducting the DPI testing is to ascertain the RF IC detector's level of detection concerning different power levels of the input signals. This information is crucial for constructing the calibration map for radiated measurements. By systematically varying the forward power levels at the input of the RF IC detector and observing its response, we can establish the relationship between the input power and the detector's detection capability. This calibration mapping will enable us to accurately determine the signal levels at which the RF IC detector can reliably detect and measure incoming signals during subsequent radiated measurements.

The measurement setup used for S-parameter measurement, as shown in Figure 79, is also utilized for DPI measurement.

7.2.1 Calibration of the RF IC Detector

A calibration curve is a crucial tool in understanding the RF IC detector's performance characteristics and assessing its range of stochastic EM field coupling in upcoming chapters. It presents the relationship between output voltage and input power, allowing us to gain insights into the detector's behaviour under different input power levels, including its sensitivity, linearity, and saturation points.

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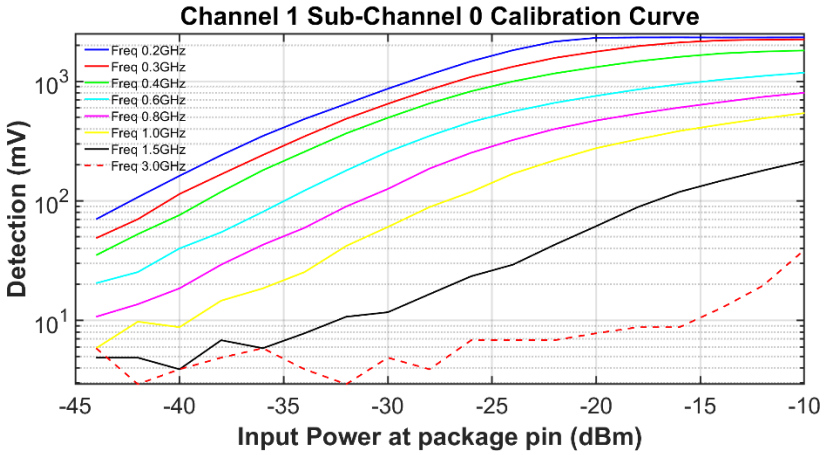

Figure 120: Shows the calibration curve that displays the relationship between input forward power at the package pin and detection for channel 1 sub-channel 0 (C1SC0) at different frequency points.

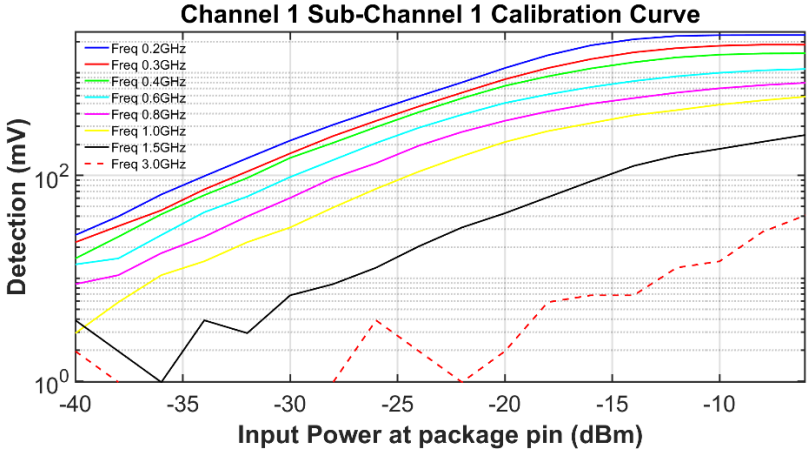

Figure 121: Shows the calibration curve that displays the relationship between input forward power at the package pin and detection for channel 1 sub-channel 1 (C1SC1) at different frequency points.

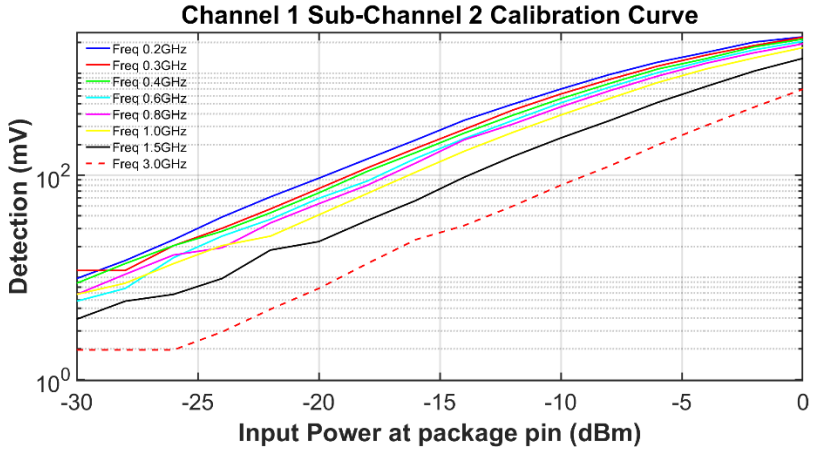

Figure 122: Shows the calibration curve that displays the relationship between input forward power at the package pin and detection for channel 1 sub-channel 2 (C1SC2) at different frequency points.

The sensitivity of the detector's input was evaluated by injecting various known forward power levels across the operating frequency band. This procedure facilitated the creation

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of a calibration map for radiated measurements using the RF IC detector. Integrating these calibration curves from all sub-channels into the Python software during radiated measurements enabled the measurement of the coupled forward power at the package pin.

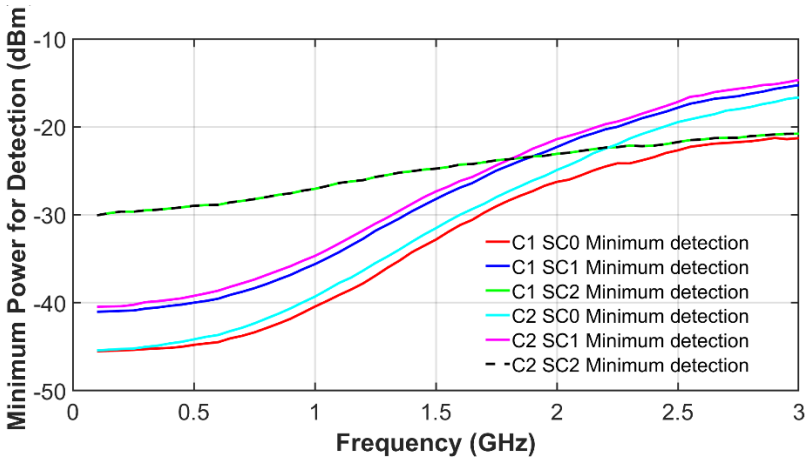

Figure 123: Shows the relationship between minimum forward power required at package pin and frequency.

Figure 120, Figure 121, and Figure 122 show the calibration curves illustrating the relationship between input forward power at the package pin and the corresponding voltage detection from the RF IC detector. The different coloured curves within each figure represent the calibration curves at various frequency points. During radiated measurements, these curves will be integrated into the Python software of the RF IC detector to measure the coupled forward power, average absorbed power and AACS at the package pin.

Figure 123 presents the dynamic range of the RF IC detector, which indicates the minimum forward power required at the package pin for the RF IC detector to detect the signal. This dynamic range is plotted for each sub-channel of channel 1 and channel 2.

7.2.2 Sensitivity of the RF IC Detector

The theory and operation of a typical diode detector are explained in [65], where it is presented that diode detectors operate in square law mode ($V_o \propto {V_{in}}^2$) for low power detection. Similar to the explanation provided by [65], the relationship ($V_o \propto P_{in}$) holds for the RF IC detector in this research as it also operates in square law mode. The derivation to show the proportionality is presented in [65]; however, based on these insights, this section presents the proportionality and relationship between V_{in}, P_{in} and V_o. From [65], at low power levels, the relationship between V_{in}, P_{in} and V_o becomes:

$$V_o = K_1 {V_{in}}^2 \tag{62}$$

here, V_{in} represents the RF voltage input at the package pin calculated from equation (64) using the power absorbed (P_{in}) into the package pin, while V_o denotes the respective output voltage for the given input power, K_1 is the sensitivity factors extracted from Figure 124, as shown in Table 11.

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$$P_{in} = \frac{{V_{in}}^2}{K_2} \tag{63}$$

where, K_2 is the sensitivity factors extracted from Figure 125, as shown in Table 11.

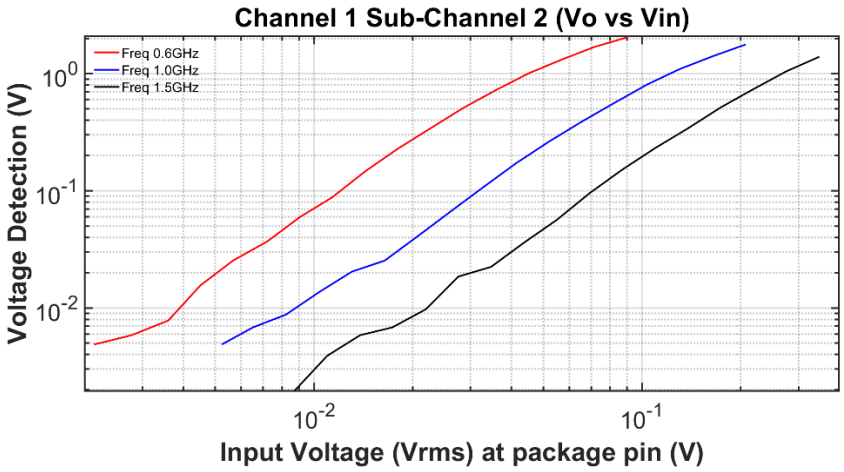

Figure 124: Shows the relationship between C1SC2 output voltage and input rms voltage.

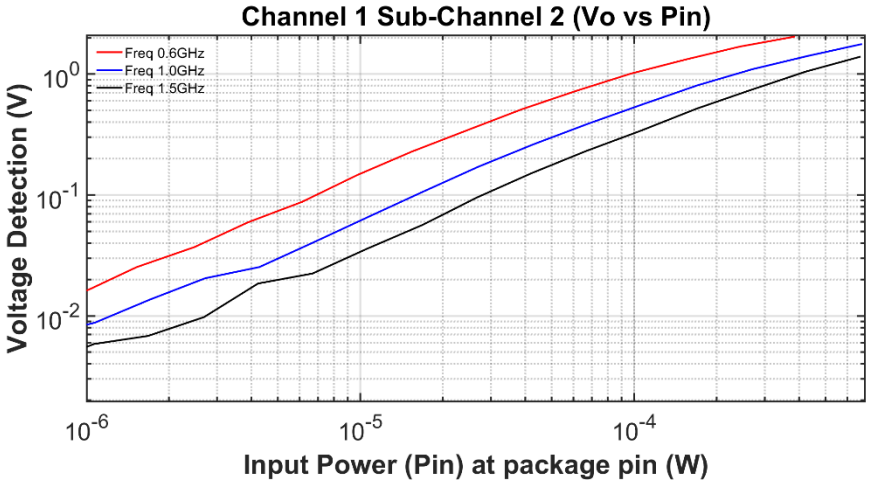

Figure 125: Shows the relationship between C1SC2 output voltage and input power.

Freq (MHz)	Vo vs Vin	Vo vs Pin
600	$V_o = 700{V_{in}}^2$	$P_{in} = \frac{{V_{in}}^2}{21}$
1000	$V_o = 100{V_{in}}^2$	$P_{in} = \frac{{V_{in}}^2}{63}$
1500	$V_o = 20{V_{in}}^2$	$P_{in} = \frac{{V_{in}}^2}{179}$

Table 11: Shows the relationship between V_{in}, P_{in} and V_o with their respective sensitivity factor K_1 and K_2 extracted from Figure 124 and Figure 125.

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The voltage sensitivity of each sub-channel when operating in square law mode can be deduced from Figure 120, Figure 121, and Figure 122. The deduced voltage sensitivity at 200MHz for a -30dBm input power is provided in Table 12.

Voltage Sensitivity of the RF IC Detector				
Sub-Channel	**Freq (MHz)**	**Input Forward Power (mW)**	**Output Voltage (V)**	**Voltage Sensitivity (V/mW)**
SC0	200	0.001	0.9	900
SC1	200	0.001	0.2	200
SC2	200	0.001	0.01	10

Table 12: Table shows the voltage sensitivity of each sub-channel from the RF IC detector.

The voltage sensitivity of SC2, as indicated in Table 12, is nearly 10 after having a gain from the Instrumentation Amplifier. While the voltage sensitivity of the peak detector from SC2 is approximately 3, the sensitivity factor $K_1 = 10$ for an ideal diode detector from [65]. The discrepancy observed between measurement and simple ideal analysis is attributed to the parasitics involved in practical circuits.

In general, the tangential signal sensitivity depends on voltage sensitivity and the noise in the following stage. If the voltage sensitivity is known, one can determine the tangential signal sensitivity. However, for our specific application, tangential signal sensitivity is not required.

7.2.3 Frequency Response

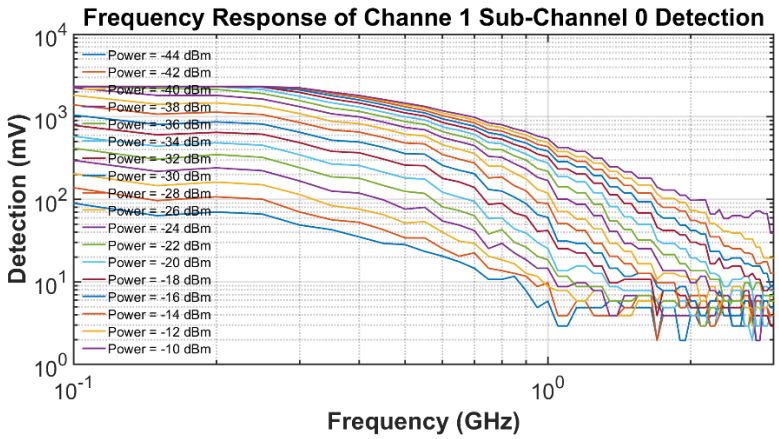

Figure 126: Shows the frequency response of sub-channel 0 of channel 1 (C1SC0 with RF amplifier) for different power levels at the input.

Here, we are presenting the measured frequency response of the RF IC detector for different power levels at the input. The frequency response provides valuable insights into the behaviour of sub-channels and the operation of the RF IC detector and performance

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across various frequencies. By analysing the frequency response, we can gain a better understanding of how the RF IC detector performs at different frequency ranges and its sensitivity to varying input power levels. This information is crucial for assessing the overall performance of the detector and ensuring its suitability for specific applications.

The frequency response of the RF amplifier channel, as shown in Figure 126, exhibits higher sensitivity compared to the frequency response of the channel containing only the peak detector, illustrated in Figure 127. This indicates that the RF amplifier channel is more responsive to changes in frequency at lower frequencies, leading to a more pronounced variation in its output as the input frequency changes. On the other hand, the channel with only the peak detector shows a relatively less sensitive response to frequency changes, resulting in a slightly consistent output over a range of frequencies.

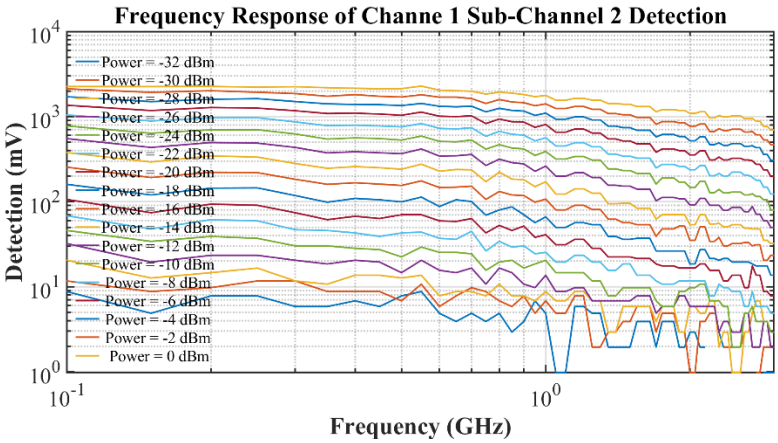

Figure 127: Shows the frequency response of sub-channel 2 of channel 1 (C1SC2 with peak detector) for different power levels at the input.

7.2.4 Transient Analysis

In this section, we analyse the transient response of the RF IC detector for each sub-channels of channel 2. The transient analysis allows us to visually observe the behaviour of the RF IC detector over time.

To compare the measurement results with the simulation, the voltage provided at the input during the simulation is converted to absorbed power into the chip by the respective package pin via lead frame and bond wire during the measurement using the following equation:

$$P_{in} = {V_{rms}}^2 Re\left\{\frac{1}{{Z_{in}}^*}\right\} \tag{64}$$

where V_{rms} is the root mean square (RMS) voltage at the input, and ${Z_{in}}^*$ is the conjugate of the input impedance at the respective sub-channel under test.

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7.2.4.1 Sub-Channel 0 (C2SC0)

Figure 128 illustrates the measured transient response of sub-channel 0 of channel 2 (C2SC0) extracted from an oscilloscope, while Figure 129 presents the comparison of the measured and simulated transient responses. To ensure consistency between the simulation and measurement, the time at which the charging process starts and the reset switch is triggered is the same as presented in Chapter 5, Section 5.8.1.

From Figure 129, we can observe that the measurement results are close to the post-layout simulation from Cadence, but not exactly the same. However, the variation between the measurement and post-layout simulation falls within the range of process variation presented in Chapter 5, Section 5.8.5. This implies that the fabrication process variations are consistent with the expected levels.

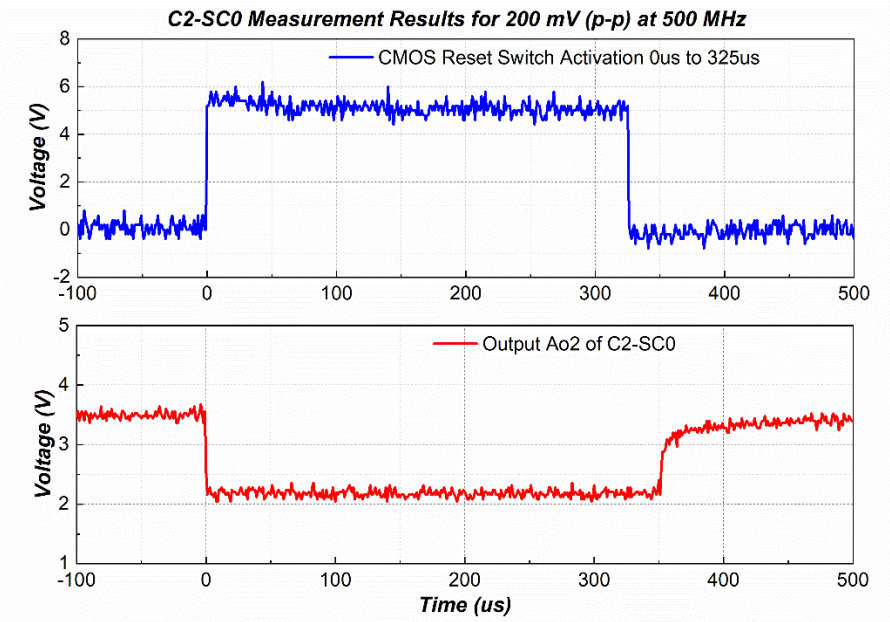

Figure 128: Shows the transient response measurement result extracted from an oscilloscope, when -12.26 dBm (200 mV peak to peak) of input is given at 500 MHz for sub-channel 0 of channel 2 (C2SC0) of the RF IC detector.

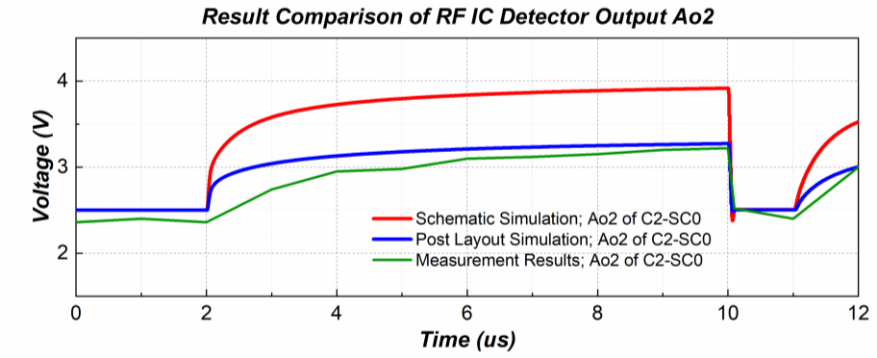

Figure 129: Shows the transient response comparison between cadence schematic simulation, post-layout simulation and measurement of sub-channel 0 of channel 2 (C2SC0) of the RF IC detector.

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Additionally, we notice a slight variation in the output bias point in the measurement. This can be attributed to several factors, such as minor discrepancies in component values, parasitic effects in the physical implementation, or small differences in manufacturing process parameters. Despite these variations, the overall performance of the RF IC detector remains within the expected range and aligns with the simulation results, validating the design and manufacturing processes.

7.2.4.2 Sub-Channel 1 (C2SC1)

Figure 130 presents transient measurement results of sub-channel 1 in channel 2 (C2SC1), obtained from an oscilloscope. In Figure 131, comparisons between Cadence schematic simulation, post-layout simulation, and measurements reveal similar discrepancies as seen in sub-channel 0 of channel 2 (C2SC0). The explanation for these discrepancies remains the same as before.

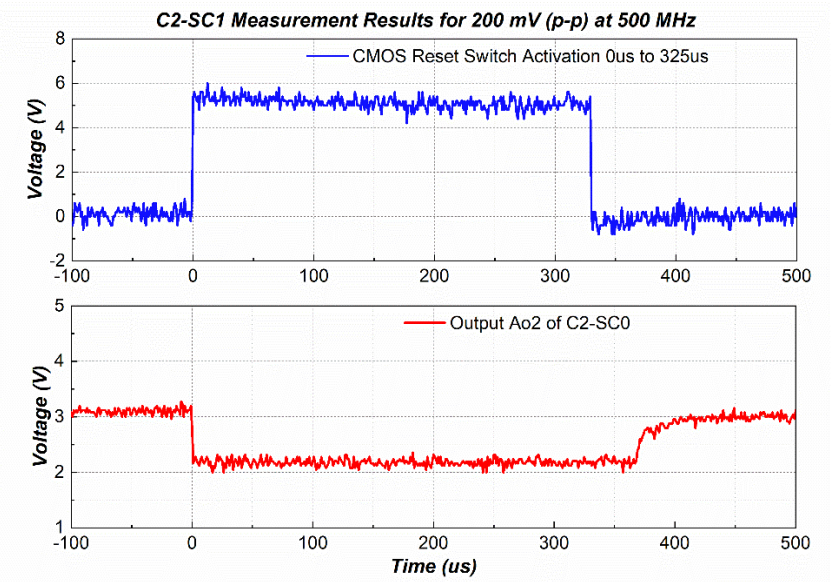

Figure 130: Shows the transient response measurement result extracted from an oscilloscope, when -12.31 dBm (200 mV peak to peak) of input is given at 500 MHz for sub-channel 1 of channel 2 (C2SC1) of the RF IC detector.

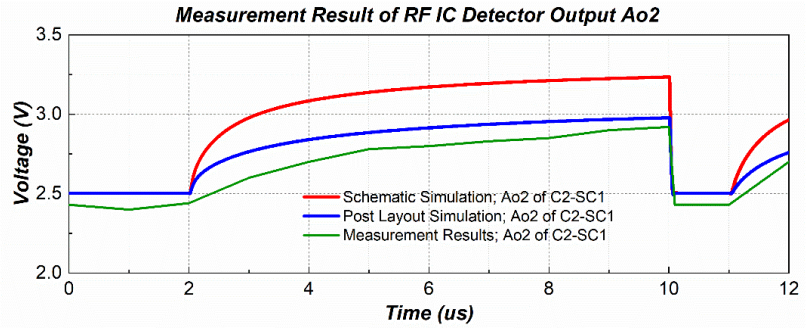

Figure 131: Shows the transient response comparison between cadence schematic simulation, post-layout simulation and measurement of sub-channel 1 of channel 2 (C2SC1) of the RF IC detector.

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7.2.4.3 Sub-Channel 2 (C2SC2)

Figure 132 presents transient measurement results of sub-channel 2 in channel 2 (C2SC2), obtained from an oscilloscope. In Figure 133, a comparison is shown between Cadence schematic simulation, post-layout simulation, and measurement results. Similar to the previous observations from C2SC0 and C2SC1, slight discrepancies exist between measurements and post-layout simulation, but they fall within the expected process variation range. These consistent results further validate the accuracy and reliability of the RF IC detector design under varying manufacturing conditions.

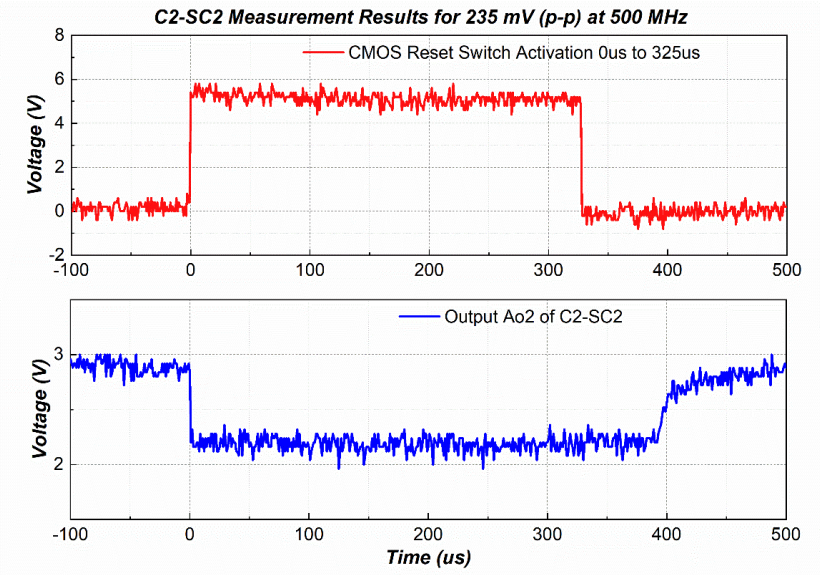

Figure 132: Shows the transient response measurement result extracted from an oscilloscope, when -5 dBm (470 mV peak to peak) of input is given at 500 MHz for sub-channel 2 of channel 2 (C2SC2) of the RF IC detector.

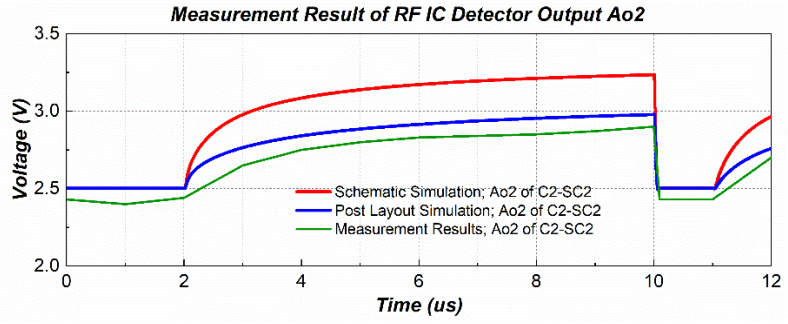

Figure 133: Shows the transient response comparison between cadence schematic simulation, post-layout simulation and measurement of sub-channel 2 of channel 2 (C2SC2) of the RF IC detector.

7.2.4.4 Sub-Channel 3

Figure 134 shows the comparison between Cadence schematic simulation, post-layout simulation, and measurement results of sub-channel 3 in channel 2 (C2SC3). This sub-channel contains only the IA, and a low-frequency single-ended input is provided to observe

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the physical behaviour of the IA. Although slight discrepancies exist between measurements and post-layout simulation, the measurement results demonstrate that the IA maintains a gain of nearly 4, consistent with the post-layout simulation. These findings affirm the performance of the IA and validate its functionality within the RF IC detector design.

The primary role of this sub-channel is to verify the proper functioning of the IA in both channels. The IA performs according to expectations, as demonstrated in Figure 134.

Overall, the measurement results presented in this section confirm the effectiveness of the RF IC detector in capturing the expected behaviour of the circuit, and the small variations observed are well within acceptable limits. The comparison between measurements and simulations provides valuable insights into the real-world performance of the device, enabling further refinement and optimization for specific applications.

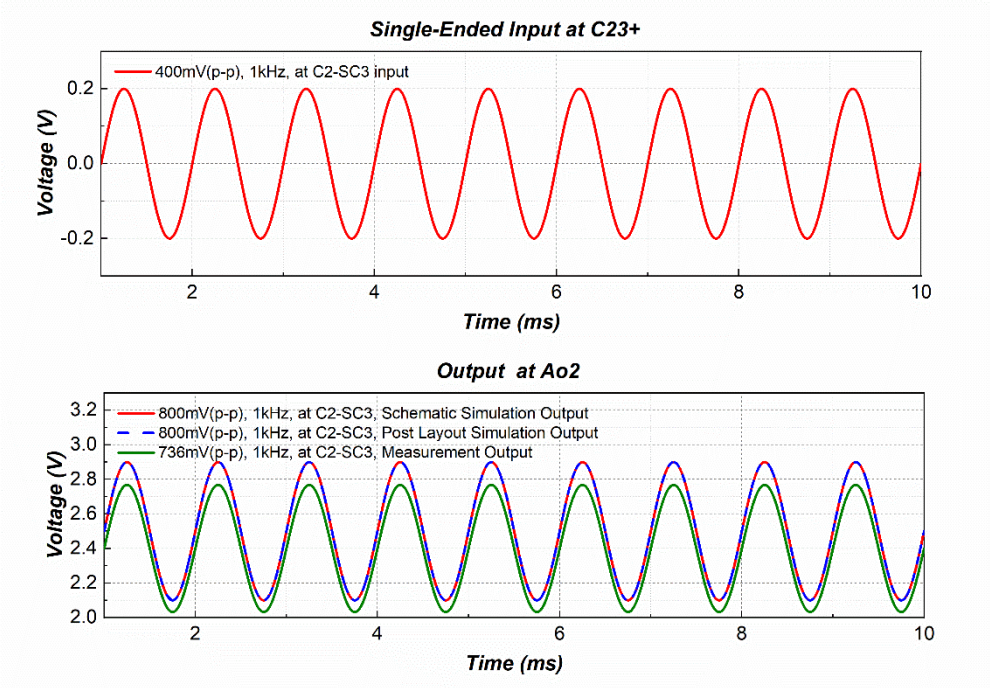

Figure 134: Shows the transient response comparison between cadence schematic simulation, post-layout simulation and measurement of sub-channel 1 of channel 3 (C2SC3) of the RF IC detector.

7.3 S-parameter Measurement of Radiated Board

In the previous Section 7.1, we were able to calculate the impedance at the package pin successfully. Now, our focus is on verifying these previous measurements and observing the process variation between different RF IC detectors. To achieve this, we conduct similar calculations to determine the impedance at the package pin once again. This step allows us to validate the accuracy and consistency of our previous results and provides valuable insights into any potential variations that may exist among different RF IC detectors. By

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comparing these new calculations with the previous ones, we can ensure the reliability of our findings and improve the overall robustness of our research.

7.3.1 Reference Plane at MCX adaptor after TOSM calibration

In this section, we perform TOSM calibration using a ZV-Z235 calibration kit for the Rhode & Schwarz VNA ZVB20 [55], similar to Section 7.1.1. The reference plane of the VNA is located at the end of the coaxial cable, as shown in Figure 80. Figure 135 and Figure 136 display the S11 of the input pins (channel 1 and channel 2) of the RF IC detector. These pins are connected to the RF IC detector via RF PCB tracks and an MCX connector.

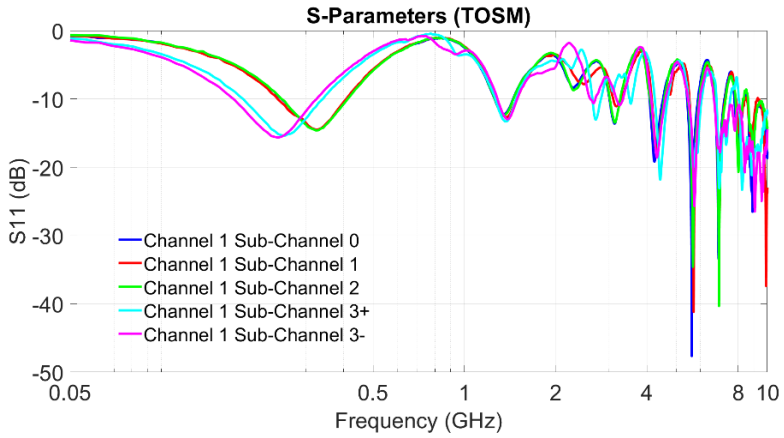

Figure 135: Shows the S11 of channel 1 at MCX connectors of the RF IC detector from the radiated board. SNN from the y-axis represents reflection co-efficient.

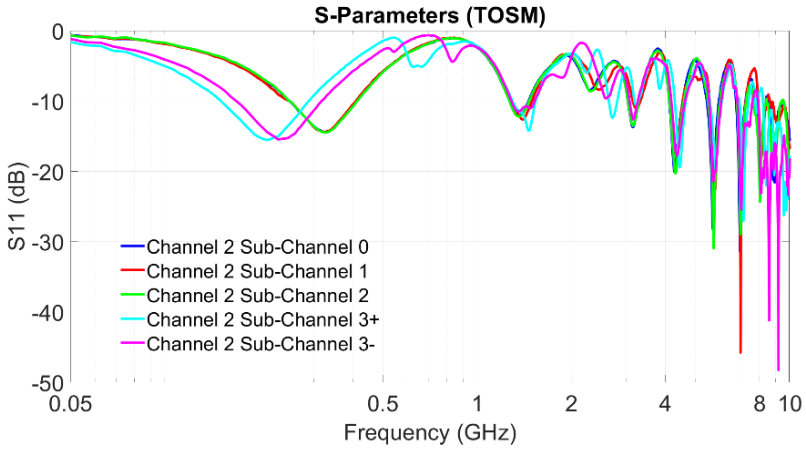

Figure 136: Shows the S11 of channel 2 at MCX connectors of the RF IC detector from the radiated board.

However, it is worth noting that the characteristic impedance of RF PCB tracks used in the radiated board and GTEM board is 115 Ω and it has a resistor in the path of the RF PCB track between the package pins of the RF IC detector and the MCX connector, as discussed in Section 6.6. As a result, the TRL/M calibration method used for the conducted board test bench is not accurate for the radiated board and GTEM board. To

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address this, we will introduce a de-embedding technique in the upcoming section to calculate the input impedance at the package pin. For this de-embedding process, we require the measurement data extracted in this section, which is obtained after the TOSM calibration.

7.3.2 Impedance Calculation using De-embedding method

In this section, we introduce a methodology to calculate the input impedance at the package pin using a de-embedding technique based on T parameters. As discussed in the previous section, the presence of a resistor in the path of the RF PCB track between the package pins of the RF IC detector and the MCX connector, and the characteristic impedance of the RF PCB track being 115 Ω, make the TRL/M calibration inaccurate, as shown in Appendix 11.4. To overcome this limitation, we propose a de-embedding technique in this section to accurately calculate the input impedance at the package pin.

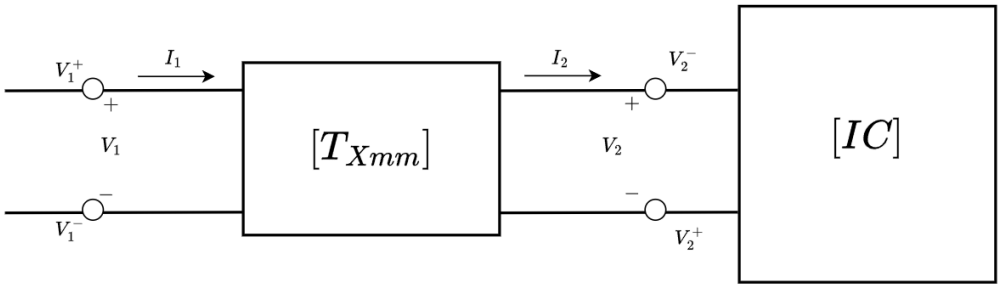

Figure 137: Shows the block diagram when microstrip TL is connected to the RF IC detector.

To calculate the input impedance of the RF IC detector at port 2 using the measured S-parameters from port 1, we employ T-parameters and ABCD parameters to mitigate the effect of the microstrip TL (RF PCB track) connected to the RF IC detector. The definitions of S-parameters, T-parameters, and ABCD parameters are represented by the equations given below:

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \tag{65}$$

$$\begin{bmatrix} V_1^+ \\ V_1^- \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{bmatrix} V_2^- \\ V_2^+ \end{bmatrix} \tag{66}$$

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{67}$$

These parameters are interchangeable with each other using equations from references [66] and [59].

For a cascaded network of n two-port networks, the T matrix of the cascaded network can be obtained as the product of the n T matrices of the individual two-ports. This allows us to analyse the overall behaviour of the cascaded network based on the characteristics of its individual components.

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$$\begin{bmatrix} V_1^+(n) \\ V_1^-(n) \end{bmatrix} = [T_1][T_2][T_3]\dots[T_n] \begin{bmatrix} V_2^-(n) \\ V_2^+(n) \end{bmatrix} \quad (68)$$

The length of the trace between the RF IC detector and the MCX connector in the radiated board is 60mm, and there is a 65-ohm resistor near the MCX connector to match the characteristic impedance of the trace (115 ohms) to the 50-ohm system.

Figure 138 shows the 60mm RF PCB track with one resistor near one of the MCX connectors from the calibration board built for the radiated board test bench. As shown in Figure 138, there are 2 MCX connectors in this trace. By measuring the S-parameters of the trace, we can calculate the T-parameters.

Figure 138: Shows one of the RF PCB track which is 60mm from the calibration board built for the radiated board test bench and the male MCX adaptor connected to the female MCX adaptor.

To eliminate the effect of the second MCX connector at the end where it will be connected to the RF IC detector package pin on the radiated board, we can use the equation below:

$$\left[T_{60mm\ (without\ 2nd\ connector)}\right] = \left[T_{60mm(with\ 2nd\ connector)}\right]\left[T_{MCXadap}\right]^{-1} \quad (69)$$

where $\left[T_{60mm(with\ 2nd\ connector)}\right]$ represents the T matrix of 60 mm trace with two MCX connectors shown in Figure 138 and $\left[T_{MCXadap}\right]$ represents the T matrix of the male MCX adaptor connected to the female MCX adaptor, also shown in Figure 138.

Equation (67) is rewritten in terms of V2 and I2 as shown below,

$$\begin{bmatrix} V_2 \\ I_2 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}^{-1} \begin{bmatrix} V_1 \\ I_1 \end{bmatrix}$$
$$\begin{bmatrix} V_2 \\ I_2 \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} V_1 \\ I_1 \end{bmatrix} \quad (70)$$

After obtaining the T-parameters of the trace and converting them to the ABCD matrix, we substitute them into equation (70) and further simplify to obtain the impedance at the package pin.

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V_1 and I_1 are written in terms of measured S-parameters at port 1 (Figure 137)

$$V_1 = V_1^+ + V_1^- = V_1^+ + S_{11}V_1^+ = V_1^+(1 + S_{11})$$
$$I_1 = \frac{V_1}{Z_{11}} = \frac{V_1^+(1 + S_{11})}{Z_{11}} \quad (71)$$

By substituting equation (71) in (70) and by expanding the matrices into equations, we arrive at the equations given below,

$$V_2 = V_1^+\left(A_1(1 + S_{11}) + \frac{B_1(1 + S_{11})}{Z_{11}}\right)$$
$$I_2 = V_1^+\left(C_1(1 + S_{11}) + \frac{D_1(1 + S_{11})}{Z_{11}}\right) \quad (72)$$

To determine the input impedance of the RF IC detector at port 2, we take the ratio of V_2 and I_2 from equation (72),

$$Z_{22} = \frac{V_2}{I_2} = \frac{Z_{11}A_1(1 + S_{11}) + B_1(1 + S_{11})}{Z_{11}C_1(1 + S_{11}) + D_1(1 + S_{11})} \quad (73)$$

This methodology allows us to calculate the input impedance at the package using the S-parameters measured at the MCX connector after TOSM calibration. The accuracy of the presented methodology is verified by applying the de-embedding technique to the conducted board test bench and comparing the results of the calculated input impedance at the package pin after TRL/M calibration and after the de-embedding method in Appendix 11.6.

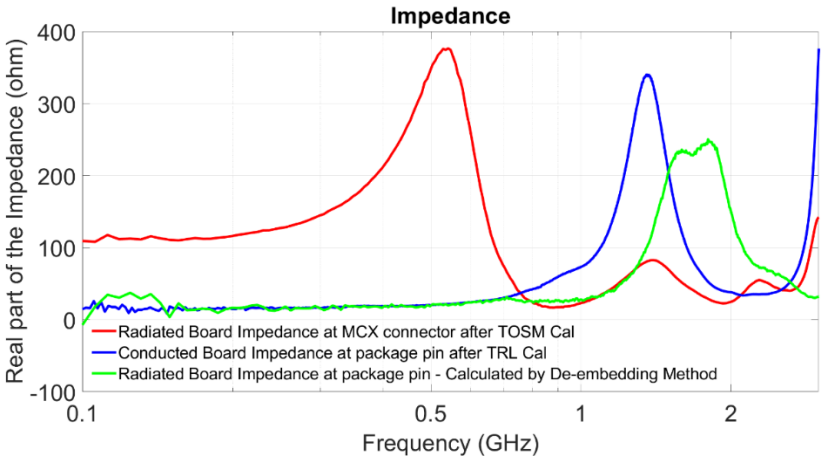

Figure 139: Shows the comparison between the real part of the impedance at the package pin of channel 1 sub-channel 0 (C1SC0) calculated after TRL/M calibration in the conducted board and the impedance calculated after TOSM calibration and de-embedding method in the radiated board.

Figure 139 and Figure 140 show the real and imaginary parts of the impedance, comparing the calculated impedance after TOSM, TRL/M, and de-embedding methods for both the conducted board and radiated board.

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We observe some differences in the impedance of sub-channel 0 of channel 1 (C1SC0) at the package pin between the results obtained through TRL/M calibration in the conducted board and the de-embedding method in the radiated board. These differences could be attributed to the variation in the dielectric arrangement of the VDD layer and GND layer, where the height of the GND layer relative to the signal layer is higher in the radiated board. Additionally, process variation among RF IC detectors may also contribute to these discrepancies.

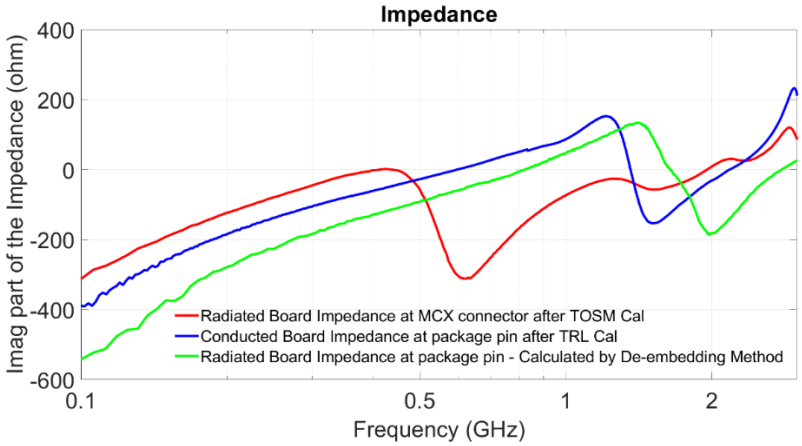

Figure 140: Shows the comparison between the imaginary part of the impedance at the package pin of channel 1 sub-channel 0 (C1SC0) calculated after TRL/M calibration in the conducted board and the impedance calculated after TOSM calibration and de-embedding method in the radiated board.

7.4 S-parameter Measurement of GTEM Board

The procedure and objectives of this section remain the same as in Section 7.3. The intention is to validate the accuracy and consistency of our previous results and gain valuable insights into any potential variations that may exist among different RF IC detectors. To achieve this, we will repeat the S-parameter measurement and de-embedding method for the GTEM board.

7.4.1 Reference Plane at MCX adaptor after TOSM calibration

The section follows a similar procedure to Section 7.1.1, where we perform TOSM calibration using a ZV-Z235 calibration kit for the Rhode & Schwarz VNA ZVB20 [55]. The reference plane of the VNA is located at the end of the coaxial cable, as shown in Figure 80. Figure 141 displays the S11 of the input pins of channel 1 of the RF IC detector, which are connected to the RF IC detector via RF PCB tracks and an MCX connector.

It is important to note that the characteristic impedance of RF PCB tracks used in the GTEM board is 115 Ω, similar to the radiated board case, and it includes a resistor in the

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path of the RF PCB track between the package pins of the RF IC detector and the MCX connector, as discussed in Section 6.6. Consequently, the TRL/M calibration method used for the conducted board test bench is not accurate for the GTEM board. To address this issue, we introduced a de-embedding technique in Section 7.3.2 to calculate the input impedance at the package pin. For this de-embedding process, we utilize the S-parameter measurement data of the GTEM board obtained after the TOSM calibration.

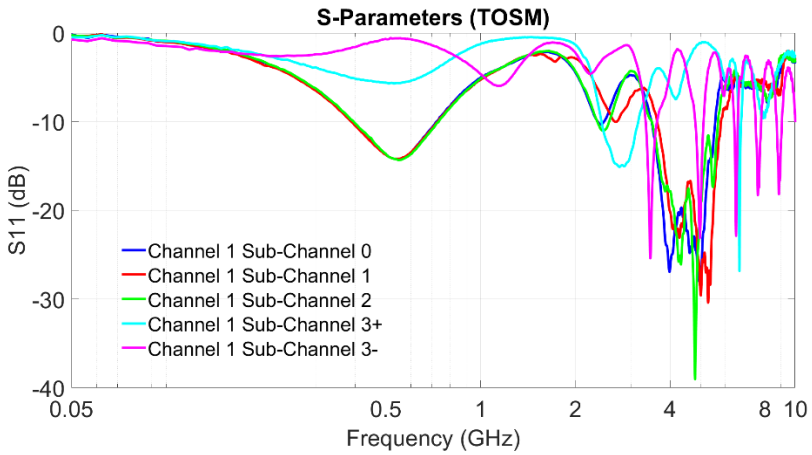

Figure 141: Shows the S11 of channel 1 at MCX connectors of the RF IC detector from radiated board.

7.4.2 Impedance Calculation using De-embedding method

The methodology remains the same as presented in Section 7.3.2. The only difference is the length of the trace used here, which is 19.318 mm, as shown in Figure 142.

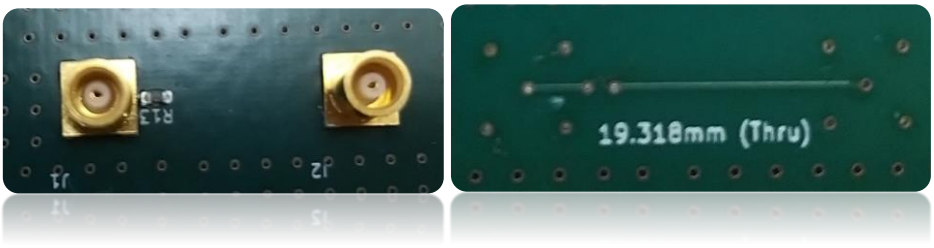

Figure 142: Shows one of the RF PCB tracks from the GTEM calibration board used to calculate T-parameters.

Figure 143 and Figure 144 display the real and imaginary parts of the impedance, comparing the calculated impedance after TOSM, TRL/M, and de-embedding methods for both the conducted board and GTEM board. Similar to the findings in the case of the radiated board (Section 7.3.2), we observe differences in the impedance of sub-channel 0 of channel 1 (C1SC0) at the package pin. These differences could be attributed to the variation in the dielectric arrangement of the VDD layer and GND layer, where the height of the GND layer relative to the signal layer is higher in the GTEM board. Additionally, process variation among RF IC detectors may also contribute to these discrepancies.

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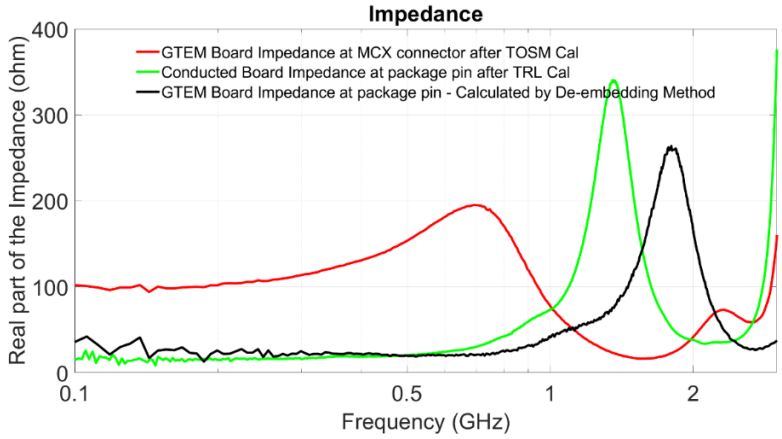

Figure 143: Shows the comparison between the real part of the impedance at the package pin of channel 1 sub-channel 0 (C1SC0) calculated after TRL/M calibration in the conducted board and the impedance calculated after TOSM calibration and de-embedding method in the GTEM board.

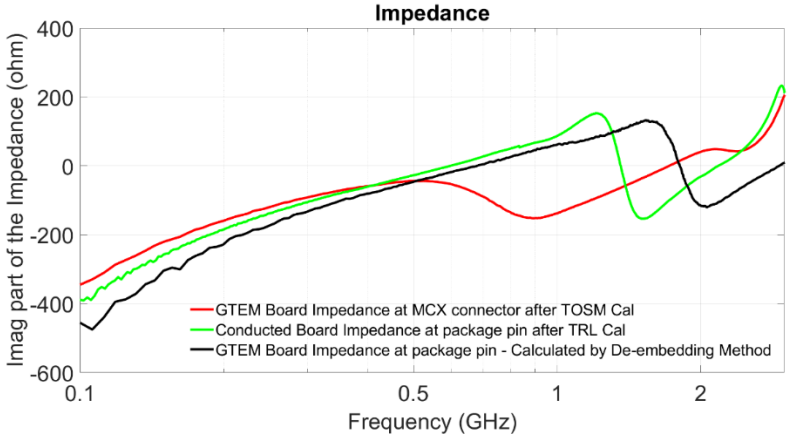

Figure 144: Shows the comparison between the imaginary part of the impedance at the package pin of channel 1 sub-channel 0 (C1SC0) calculated after TRL/M calibration in the conducted board and the impedance calculated after TOSM calibration and de-embedding method in the radiated board.

7.5 Comparison of Calculated Impedances

In this section, we compare the calculated impedance of sub-channel 0 of channel 1 (C1SC0) at the package pin for all three boards: conducted board, radiated board, and GTEM board. This comparison allows us to observe the impedance variations among different RF IC detectors used in different test benches, providing insights into possible process variation.

These measurement data will be used to calculate and compare the calculated input impedance at the package pins using a de-embedding method for both the GTEM and radiated board measurements. This is necessary because both the GTEM board and

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radiated board consist of RF PCB tracks with a characteristic impedance of 115 Ω, for which the TRL/M calibration is not accurate.

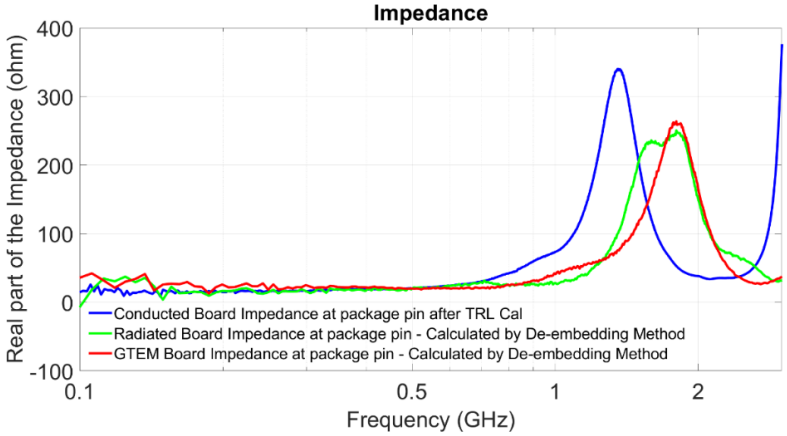

Figure 145: Shows the real part of the impedance at the package pin of sub-channel 0 of channel 1 (C1SC0) calculated for the conducted board (blue), radiated board (green) and GTEM board (red).

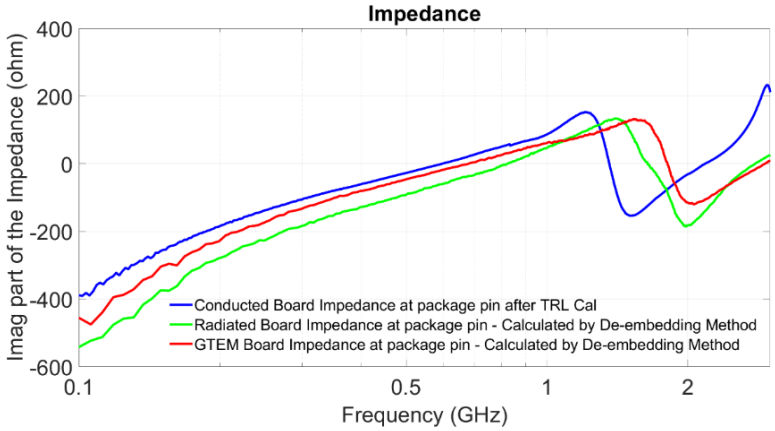

Figure 146: Shows the imaginary part of the impedance at the package pin of sub-channel 0 of channel 1 (C1SC0) calculated for conducted board (blue), radiated board (green) and GTEM board (red).

Even though there is a slight difference between the impedance calculated from the conducted board compared to the impedance from the radiated and GTEM board, the impedance of the radiated board and GTEM board are closer to each other. This difference could be attributed to the variation in the dielectric arrangement of the VDD layer and GND layer, where the height of the GND layer relative to the signal layer is higher in the radiated and GTEM boards. Additionally, process variation among RF IC detectors may also contribute to these discrepancies. However, the impedance at the package pin for both the radiated board and GTEM case is almost the same due to the proximity in the height between the signal layer and GND layer, although they are not exactly the same.

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8. Prediction of Probability of IC Failure and Experimental Validation of Stochastic EM Fields Coupling into PCB Traces and IC Package Pins.

Previous research conducted at the UoY, as cited in [1], introduced a risk assessment model capable of predicting the upper bound for electronic device failure probability. Globally, significant contributions from other researchers in this field include [2], which presents a statistical method for predicting and quantifying the radiated susceptibility of electronic systems on PCBs. This method categorizes and quantifies hazard levels in harsh EM environments, estimating threshold levels based on system-level PCB information to assess EM threat levels. Additionally, [3] investigates the frequency-dependent EM susceptibility of custom digital ICs. It highlights an inverse relationship between IC immunity and the modulating signal period, alongside a direct correlation with E-field amplitude and pulse width, ultimately linking the probability of IC susceptibility to the modulating signal and transmitted information. Challenges arise in radiated immunity testing of ICs above 1 GHz, such as achieving high field strengths and managing effects related to the orientation of the EUT. Current methods struggle to address these challenges, but [4] proposes that the reverberation chamber, operating on a different principle, offers a potential solution by overcoming these limitations in the higher frequency range.

The IC EMC standard BS EN 62132-4 [5] outlines a framework for assessing IC susceptibility by evaluating the required directly injected forward power to induce IC malfunction. The understanding of the power coupled or absorbed into the IC or other electronic components is crucial for susceptibility prediction analysis.

In this chapter, we evaluate the probability of susceptibility of PCB components, such as ICs, by considering the coupled forward power at the package pin of the DUT. In [7], a numerical Monte Carlo method was developed to estimate the average coupled power at the end of lossless PCB traces in a reverberant environment. We begin this chapter by integrating the PCB losses and calculated input impedance at package pins, as presented in Chapter 7, Section 7.1.3 and Section 7.1.5 respectively, into a previously established numerical model [7] validated in Chapter 4, we refined our ability to estimate the distribution of coupled forward power at the package pin of the IC for a given reverberant field. We can then use our knowledge of field statistics to predict the probability of IC failure, particularly in a reverberant external environment or its equivalent. In a real-world setting, victim electronic components can receive EMI signals from multiple directions and polarizations simultaneously, originating from a single external interference source, and thus the reverberant case takes into account this multiplicity. Moreover, the work presented in this chapter validates the Monte Carlo method to predict stochastic EM coupling into

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realistic loads such as IC pins via measurements of test RF PCB tracks. This validation is accomplished through an instrumented custom-designed RF IC detector presented in Chapter 5 and Chapter 6, which can measure the coupled power at its package pins via test RF PCB tracks. Towards the end of the chapter, we will correlate these prediction models with EMC limits specified for automotive ICs [67], [68], serving as a valuable bridge between theoretical insights and practical applications.

8.1 Numerical Method Based on Monte Carlo Method

The research outlined in [7] focused on the factors that influence the EM power absorbed by lossless PCB trace loads and the development of a numerical method based on the Monte Carlo method. This numerical method was basically created to estimate the average coupled power at the terminus of lossless PCB traces in a reverberant environment.

However, in this section, we expand the scope of the numerical model to encompass PCB losses. This enhancement involves the incorporation of PCB losses using the RLGC model, as elaborated upon in Section 7.1.3.1 part c).

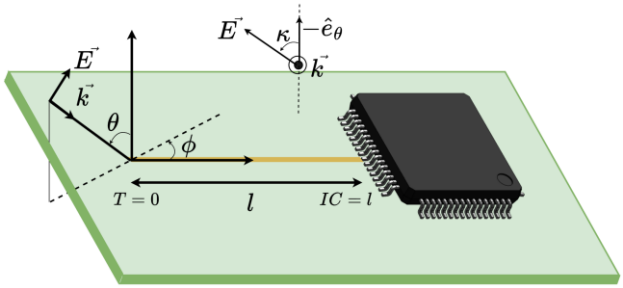

Figure 147: Shows the E-field coupling to IC via PCB trace with a definition of polar angle (θ), azimuth angle (ϕ), and polarization angle (κ).

Figure 147 illustrates a PCB trace, excited by a plane wave connected to an IC load at one end and some known terminating load at the other. Although our primary interest lies in assessing the coupled power into the load, it is more straightforward to employ voltage analysis in the first instance. The voltages at the ends of a single PCB trace, excited by the Nth plane wave in a reverberant field can be represented by the Baum-Liu-Tesche (BLT) equation for the frequency domain. The load voltage responses (V_T and V_{IC}) in the microstrip TL [69], [70], and are given by:

$$\begin{bmatrix} V_T \\ V_{IC} \end{bmatrix} = \begin{bmatrix} 1+\Gamma_T & 0 \\ 0 & 1+\Gamma_{IC} \end{bmatrix} \cdot \begin{bmatrix} -\Gamma_T & e^{\gamma l} \\ e^{\gamma l} & -\Gamma_{IC} \end{bmatrix}^{-1} \cdot \begin{bmatrix} S_T \\ S_{IC} \end{bmatrix} \tag{74}$$

In the given context, l represents the length of the traces, γ stands for the propagation constant in terms of per unit length (p.u.l) RLGC, and RLGC denotes the p.u.l parameters (Resistance, Inductance, Conductance, Capacitance) characterizing a single PCB track, as defined in equation (53). The notation $T = 0$ designates the near end (terminating end),

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while $IC = l$ signifies the far end (IC end), with the distance between these ends being the actual length of the trace ($IC - T = l - 0 = l$).

The reflection matrix at the ends of the traces, denoted by $\Gamma_{T,IC}$, is computed using the formula:

$$\Gamma_X = [Z_X - Z_c] \cdot [Z_X + Z_c]^{-1}, \quad X = T, IC = 0, l \tag{75}$$

here, Z_c represents the characteristic impedance in terms of p.u.l RLGC of a single PCB track (defined in equation (52)), Z_{IC} is the input impedance at the package pin obtained through TRL/M calibration on the test bench, as described in Section 7.1.2, and Z_T is the impedance at the terminating end of the PCB track on the test bench.

We incorporate the frequency-dependent per unit length (p.u.l) resistance with roughness, inductance, conductance, and capacitance of the single RF PCB track into this numerical model. These elements are crucial in determining the propagation constant (γ) and characteristic impedance (Z_c) as part of the RLGC model presented in Section 7.1.3.1 part c).

The voltage source vectors S_T and S_{IC} induced by external fields [39],

$$\begin{bmatrix} S_T \\ S_{IC} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} \int_{T=0}^{IC=l} e^{\gamma x} E_x(x) dx + v_T - e^{\gamma l} v_{IC} \\ -\int_{T=0}^{IC=l} e^{\gamma (l-x)} E_x(x) dx - v_T e^{\gamma l} + v_{IC} \end{bmatrix} \tag{76}$$

with

$$v_{T,IC} = \int_{-h}^{0} E_z(x,z) dz\,, \quad x = 0, l \tag{77}$$

$E_x(x)$ is the x-component of the total E-field along the trace. Ignoring the effects induced by the loss and diffraction of the PCB on the excitation fields of the trace, it is given by [39],

$$E_x(x) = E_x^{\mathrm{TE}} + E_x^{\mathrm{TM}} = E_n f_x(\theta, \phi, \kappa) e^{-jk_x x} \tag{78}$$

here, $k_x = k_0 \sin\theta \cos\phi$, where θ, ϕ and κ represent the polar angle (elevation angle), azimuth angle and, polarization angle of incidence, respectively.

$$f_x(\theta, \phi, \kappa) = \cos\theta \cos\phi \cos\kappa \,(1 - R^{\mathrm{TM}}) + \sin\phi \sin\kappa \,(1 + R^{\mathrm{TE}}) \tag{79}$$

Assuming an ideally conducting ground plane, the generalized reflection coefficients for TE and TM waves are [39],

$$R^{\mathrm{TE,\,TM}} = \frac{r^{\mathrm{TE,\,TM}} \mp e^{-jk_{2z}2h}}{1 \mp r^{\mathrm{TE,\,TM}} e^{-jk_{2z}2h}} \tag{80}$$

where, $k_{2z} = k_0\sqrt{\varepsilon_r - \sin^2\theta}$, and $r^{\mathrm{TE,\,TM}}$ represent the Fresnel reflection coefficients for the air/dielectric boundary, as given by,

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$$r^{\mathrm{TE}} = \frac{cos\,\theta - \sqrt{\varepsilon_r - sin^2\,\theta}}{cos\,\theta + \sqrt{\varepsilon_r - sin^2\,\theta}}$$
$$r^{\mathrm{TM}} = \frac{\varepsilon_r\,cos\,\theta - \sqrt{\varepsilon_r - sin^2\,\theta}}{\varepsilon_r\,cos\,\theta + \sqrt{\varepsilon_r - sin^2\,\theta}} \quad (81)$$

$E_z(x,z)$ represents the z-directed E-field within the substrate layer and is given by:

$$E_z(x,z) = Ef_z(\theta,\phi)\left(e^{jk_{2z}z} + e^{-jk_{2z}(2h+z)}\right)e^{-jk_x x}$$
$$f_z(\theta,\phi) = \frac{cos\,\kappa\,sin\,\theta}{\varepsilon_r}\frac{1 + r^{\mathrm{TM}}}{1 + r^{\mathrm{TM}}e^{-jk_{2z}2h}} \quad (82)$$

By substituting all the above equations into equation (76) and solving the integration, we arrive at the following equation:

$$S_T = \frac{E_n e^{\gamma T}}{2}\left[f_x(\theta,\phi,\kappa) - \left\{(\gamma - jk_x)f_z(\theta,\phi)\frac{1 - e^{-jk_{2z}2h}}{jk_{2z}}\right\}\right]\frac{\left[e^{(\gamma - jk_x)l} - 1\right]}{(\gamma - jk_x)} \quad (83)$$

and

$$S_{IC} = -\frac{E_n e^{\gamma(IC)}}{2}\left[f_x(\theta,\phi,\kappa) - \left\{(-\gamma - jk_x)f_z(\theta,\phi)\frac{1 - e^{-jk_{2z}2h}}{jk_{2z}}\right\}\right]\frac{\left[e^{(-\gamma - jk_x)l} - 1\right]}{(-\gamma - jk_x)} \quad (84)$$

As discussed in [7], we utilize a finite number of plane waves (N) in the numerical simulation for each incidence condition, characterized by random angles ϕ, θ and κ. The Monte Carlo (MC) method is employed to generate a finite number (N) of plane waves for different angles. For B different boundary conditions (representing various stirrer positions in a reverberation chamber), each condition yields N plane waves. In this method, the angles ϕ and κ are equally distributed between [0, 2π] and [0, π], respectively. We apply an efficient technique to eliminate $\sin\theta$ from the summand from [71], which statistically distributes the polar angle (θ) or elevation angle according to $\arccos\big(U(-1,1)\big)$, where $\big(U(-1,1)\big)$ represents a uniform distribution between -1 and 1.

The voltage vectors of the PCB traces, which are exposed to individual plane waves, can be determined through the use of equation (74). To ensure compliance with the normalization rule [71], it is necessary for the electric magnitude (E_n) of each plane wave to meet the following condition:

$$E_n = \frac{E_0}{\sqrt{2N}} \quad (85)$$

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where, E_0 represents the average magnitude of the total field in the reverberation chamber. The consideration of 2N in the equation arises from the splitting of power (P) of a plane wave into two parts when coupled to a trace: P/2 to one end and P/2 to the other end of the trace. Consequently, for N plane waves, each carrying amplitude E_n, the power is proportionally linked to twice the sum of the squares ($P \sim 2N \cdot {E_n}^2$).

By substituting S_1 and S_2 into equation (74) to obtain V_T and V_{IC}, we can calculate the average absorbed power ($\langle P_{T,IC} \rangle_a$) and average forward power ($\langle P_{T,IC} \rangle_f$) at the package pin of the IC for a finite number of plane waves (N) using the equation provided below,

$$\langle P_{T,IC} \rangle_a = \left\langle \left| V_{T,IC} \right|^2 \right\rangle Re\left\{ \frac{1}{{Z_{T,IC}}^*} \right\}$$
$$\langle P_{T,IC} \rangle_f = \frac{\langle P_{T,IC} \rangle_a}{1 - \left| \Gamma_{T,IC} \right|^2} \tag{86}$$

Using the calculated average absorbed power, we can determine the AACS at the trace end,

$$\langle {\sigma_t}^a \rangle_{T,IC} = \langle P_{T,IC} \rangle_a \frac{\eta_0}{E_0^2} \tag{87}$$

here, η_0 represents the intrinsic impedance of free space.

8.2 Analytical Methodology to Predict the Probability of Susceptibility of ICs

In this section, we introduce an analytical methodology for predicting the probability of IC failure. The flow chart depicted in Figure 148 illustrates the comprehensive steps involved in determining the likelihood of IC failure during testing.

The numerical method discussed in the previous section allows us to predict the potential power that can be coupled at the end of a lossy PCB trace, taking into account a given load impedance (which corresponds to the input impedance at the package pin) and a specific incident field. This capability is instrumental in our approach in assessing the probability of IC failure.

The IC EMC standard, BS EN 62132-4 [5], facilitates the evaluation of IC immunity by evaluating the forward power needed to trigger IC malfunction. Therefore, in this section, our initial focus is on estimating the distribution of coupled forward power at the package pin for a given frequency point and across multiple samples, as illustrated in Figure 149.

As well as the average forward power, the Monte Carlo method confirms that the distribution of received forward power is exponential as would be expected for an antenna in a reverberant environment [72]. The results of the numerical model forward power

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distribution along with the analytic exponential distribution with the same variance can be seen in Figure 149 along with the cumulative distribution in Figure 150.

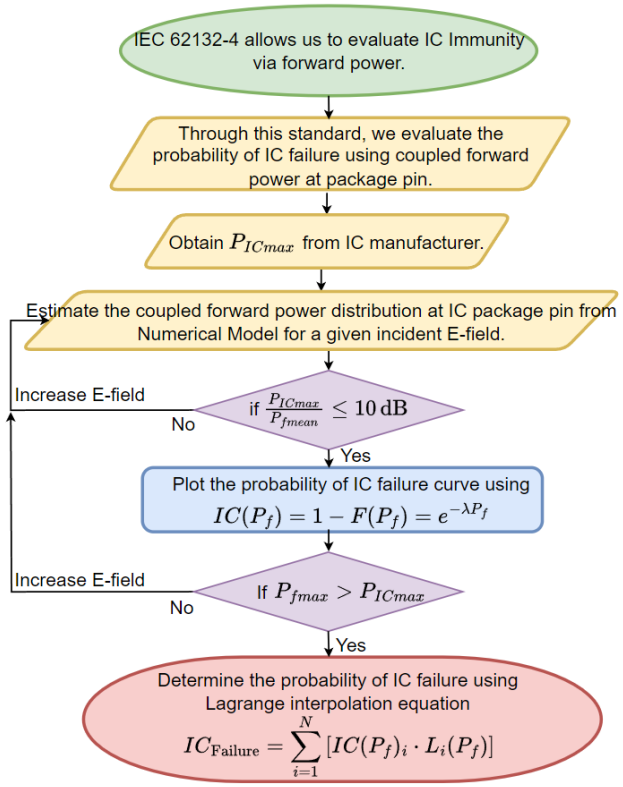

Figure 148: Shows the flow chart for the analytical methodology to predict the probability of susceptibility of ICs.

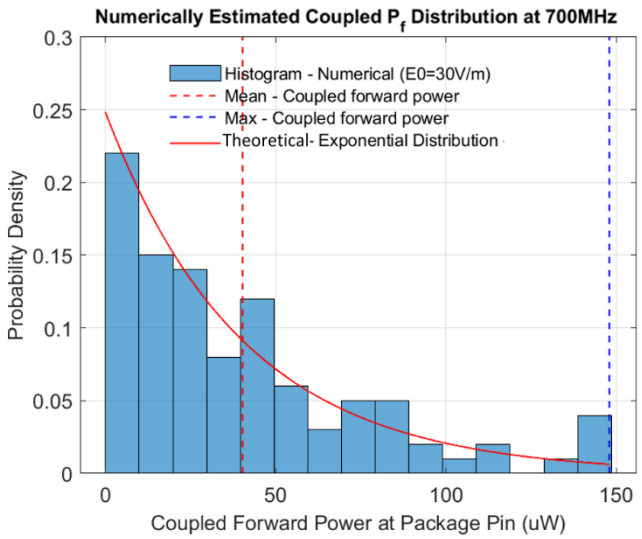

*Figure 149: Numerically estimated distribution of coupled forward power at package pin ($\boldsymbol{Z_{IC}}$ **of** C1SC2, 700MHz): Analysed over B=100 samples, depicting variations in power coupling at the package pin.*

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We now understand that the distribution of coupled forward power at the package pin (P_f) follows an exponential pattern. The theoretical curve in Figure 149 is derived using the following equation:

$$f(P_f) = \alpha\lambda e^{-\lambda P_f}$$
$$P_f = \left\{P_{f_1}, P_{f_2}, \dots, \left(P_{f_N} = P_{fmax}\right)\right\} \quad (88)$$

where, $P_{f_1} \le P_{f_2} \le \cdots \le P_{f_N}$, P_f is the coupled forward power arranged in ascending order, $\lambda = {}^1/_{\mu}$ and $\mu = P_{fmean}$, which is the mean value of the forward power.

To gain visual insights into the area under the curve, we use the Cumulative Distribution Function (CDF) of coupled forward power, which is expressed by the equation:

$$F(P_f) = 1 - e^{-\lambda P_f} \quad (89)$$

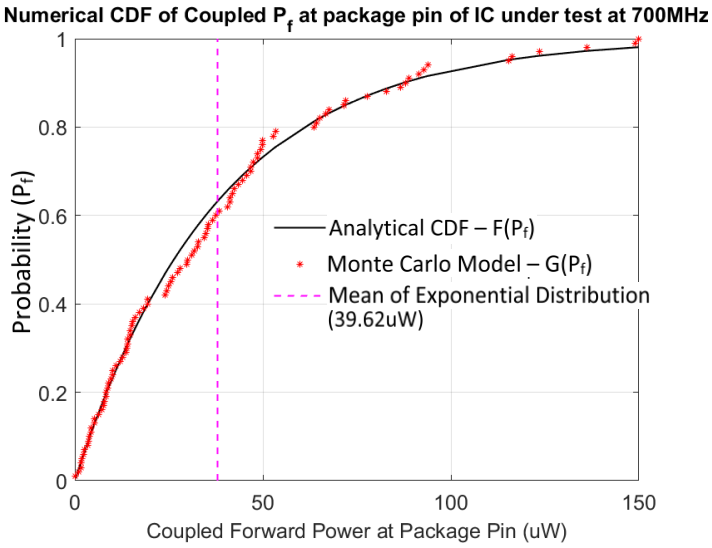

Figure 150: Numerically Estimated Cumulative Distribution of Coupled Forward Power at Package Pin (C1SC2, 700MHz): Aggregated data over B=100 samples, showcasing the cumulative distribution of power coupling at the package pin.

The empirical CDF shown in Figure 150, represented by red stars, is defined as follows:

$$G(P_f) = \frac{number\ of\ elements\ in\ the\ sample \le P_f}{B} \quad (90)$$

Equation (89) provides us with the probability that the power is less than a reference value along the x-axis. Our primary interest lies in understanding the probability of power exceeding a reference value, particularly if this reference value is the power level at which the IC malfunctions (P_{ICmax}). This can be calculated using the equation below:

$$IC(P_f) = 1 - F(P_f) = e^{-\lambda P_f} \quad (91)$$

In Figure 150, the mean coupled forward power is indicated by a vertical line. 63.21% of the coupled forward power samples are less than the mean value, while 36.79% of the

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coupled forward power samples exceed the mean value. The CDF computed using the Monte Carlo model is also shown.

Whilst the analytic exponential distribution extends to infinity in a practical evaluation with a finite number of samples, the maximum forward power is likely to be around 10 dB greater than the mean for 100 samples [73]. So in any practical evaluation of failures, the mean forward power coupled should be large enough to ensure a meaningful number of failures are seen and certainly less than 10dB below the failure level or the absolute maximum power limit (P_{ICmax}) specified by the IC manufacturer, which defines the point at which IC malfunction occurs. As can be seen from Figure 150, if the mean coupled power is equal to the failure power an actual failure will occur in about 36% of the tests.

From equation (91) we can get the visual insight into the probability of IC failure. To determine the probability of power being greater than one particular reference value ($P_{ICmax} = failure\ level$), which corresponds to the probability of IC failure when forward power crosses the failure level, we will increase the incident E-field in the numerical model such that $P_{fmax} > P_{ICmax}$, that is to a level where P_{fmax} exceeds P_{ICmax}. We will then utilize the Lagrange interpolation equation as shown below:

$$IC_{Failure} = \sum_{i=1}^{N} \left[IC\left(P_f\right)\right]_i L_i(P_f)$$
$$L_i\left(P_f\right) = \prod_{\substack{j=1 \\ j \neq i}}^{B} \frac{P_{ICmax} - \left(P_f\right)_i}{\left(P_f\right)_i - \left(P_f\right)_j} \quad (92)$$

This analytical approach empowers us to perform a quantitative assessment of the probability of failure for the IC under test. Such an analysis makes informed decisions regarding the IC's ability to withstand the EMI environment without risking potential damage. Given the high cost associated with ICs, this knowledge is invaluable.

Furthermore, this method allows us to streamline the IC fabrication process. By testing a single IC piece to determine its vulnerability, particularly by establishing P_{ICmax}, and then utilizing our prediction model to assess the probability of IC failure under various incident field conditions, we can save a significant amount of both time and resources that would otherwise be expended on IC redesigns.

Moreover, the capability to conduct advanced numerical simulations of radiated immunity tests provides a multitude of practical advantages in real-world applications. In the forthcoming section, we will correlate these prediction models with EMC limits specified for automotive ICs [67], [68], serving as a valuable bridge between theoretical insights and practical applications.

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8.3 Radiated Measurement in Reverberation Chamber

8.3.1 Measurement Setup

The measurements presented in this chapter provide a deeper understanding of the average power coupled to realistic loads, such as IC pins connected via test RF PCB tracks, when exposed to radiated fields inside the reverberation chamber (Section 3.2.2). One end of each PCB track is connected to various input sub-channels of the RF IC detector, representing the realistic loads. The other end of the PCB tracks is either left open or terminated with a 115 Ω matched load.

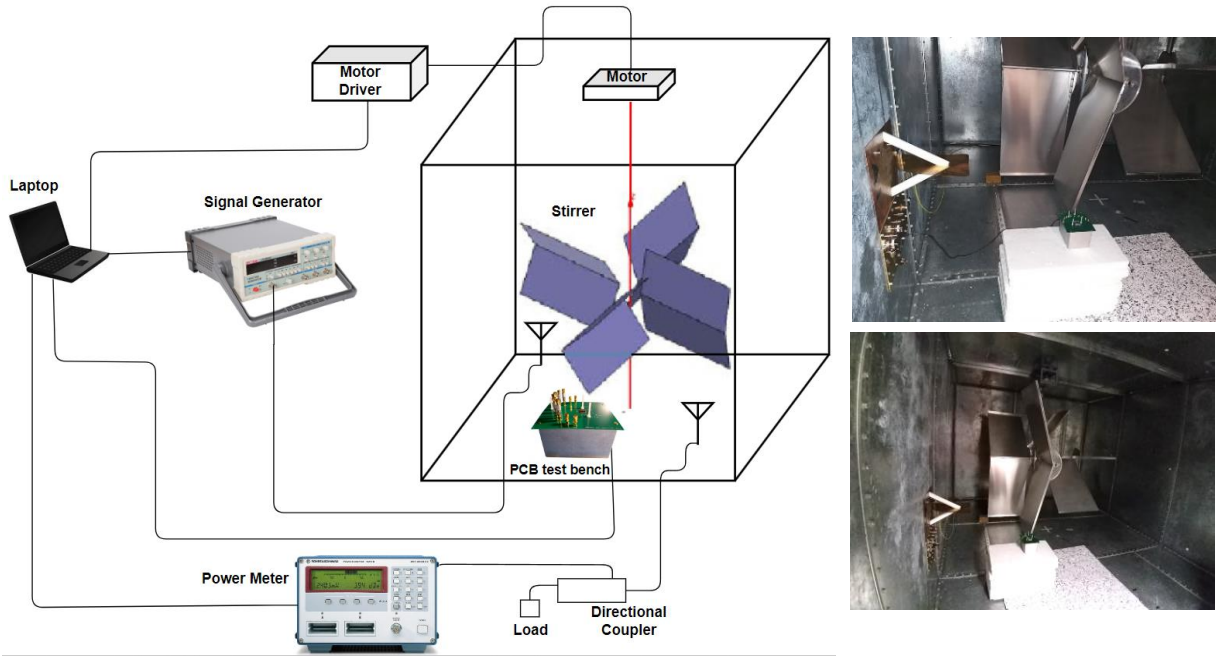

Figure 151: Shows the measurement setup for radiated measurement and pictures taken during the measurement.

Figure 152: Visual of the assembled test setup featuring the radiated PCB board at the top.

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Figure 151 shows the measurement setup used for radiated measurements within a reverberation chamber. These measurements cover 100 stirrer positions spanning from 200 MHz to 2 GHz, with a 20 MHz step increment. A power signal generator drives a broadband antenna to generate the field in the chamber which is monitored by a second broadband antenna. Coupling to each detector channel is measured by the test bench and transmitted to the instrument controller by the USB interface of the Arduino processor. The measurement equipment, including the PCB test bench of the RF IC detector, is monitored using Python software.

The details of the top radiated board are presented in Section 6.6. In the RF IC detector test bench, the radiated board is positioned at the top of the test bench. The entire test bench, which includes the bottom control board, middle board, and the bottom side of the radiated board, is shielded. Only the top side of the radiated board is exposed to the reverberant environment, as shown in Figure 152 and Figure 72.

8.3.2 Quality Factor and Chamber Constant of Reverberation Chamber

8.3.2.1 Q-Factor

For the extraction of the Q-factor of the chamber, an initial measurement is conducted using a VNA [55]. Port 1 of the VNA is connected to the transmitting antenna, while port 2 is connected to the receiving antenna within the chamber. The measurement is performed across 100 stirrer positions, with frequency sweeping at each stirrer position. The Q-factor of the chamber is then calculated using Equation (13).

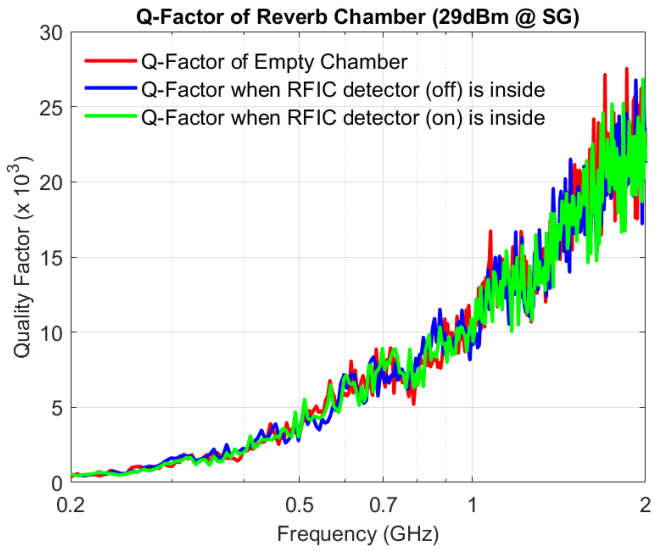

Figure 153: Shows the Q-factor of the reverberation chamber for different scenarios when the input power to the chamber is 29dBm.

The mean net transfer function (G) of the chamber, expressed in terms of S-parameters, as derived from Equation (15), is given by:

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$$G = \frac{\langle P_r \rangle}{\langle P_t \rangle} = \frac{\langle |S_{21} - \langle S_{21} \rangle|^2 \rangle}{(1 - |\langle S_{11} \rangle|^2)(1 - |\langle S_{22} \rangle|^2)\eta_1\eta_2} \quad (93)$$

The PCB test bench of the RF IC detector interacts with the EM field inside the chamber, leading to reflections and absorption of EM waves. These interactions may have an impact on the uniformity of the EM field and the rate of energy decay within the chamber. Consequently, the presence of the PCB test bench affects the EM field inside the Reverberation Chamber, subsequently influencing the Q-factor. To ensure a more accurate measurement of the Q-factor, the PCB test bench and connection cables are positioned inside the chamber. The process of calculating the Q-factor provides essential information on the coupling between antennas and the reflection coefficient of both the transmitting and receiving antennas inside the chamber. This information is crucial for monitoring the E-field within the chamber.

Figure 153 provides a visual representation of the Q-factor for three distinct conditions within the chamber. First, it shows the Q-factor of the empty chamber. Next, it illustrates the Q-factor of the chamber when the test bench of the RF IC detector is situated inside. In this latter scenario, the measurement of the Q-factor was conducted separately for two conditions: one with the test bench powered on and the other with it powered off. Interestingly, the power conditions of the test bench do not appear to have any impact on the Q-factor of the chamber.

8.3.2.2 E-field Distribution

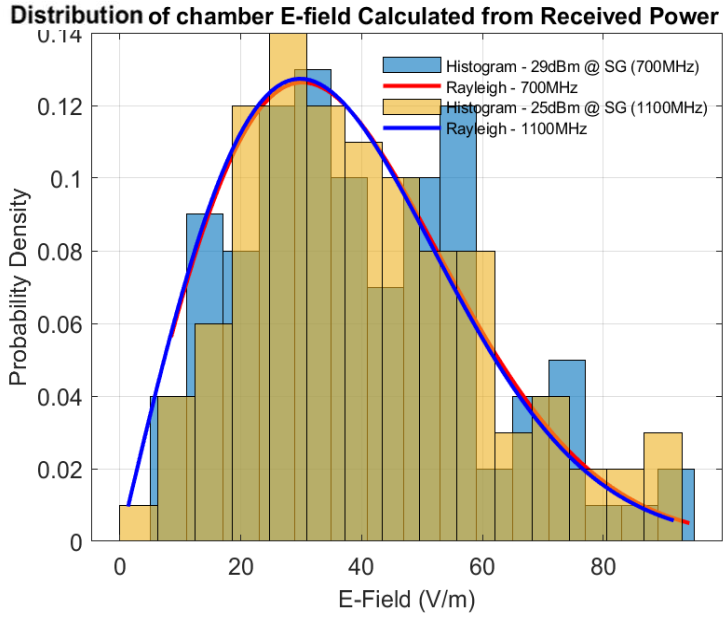

Figure 154: E-Field Distribution in Chamber at 0.7 GHz and 1.1 GHz: Calculated from Received Power at the Receiving Antenna, presented in PDF format.

During the radiated measurements utilizing the setup illustrated in Figure 151, the E-field is monitored at each stirrer position by measuring the received power from the

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receiving antenna using a power meter. This is calculated using the equation presented below:

$$E_0^2 = \frac{8\pi Z_o \eta_2}{\lambda^2}\langle P_r \rangle = \frac{8\pi Z_o \eta_2}{\lambda^2}\frac{P_{PM}}{|T_c|^2(1-|\Gamma_a|^2)\eta_2} \quad (94)$$

here, $Z_o = \sqrt{\mu_O/\varepsilon_O}$ represents the free-space impedance, P_{PM} represents the received power measured by the power meter at the receiving antenna, T_c denotes the transmission coefficient of the cable connected between the receiving antenna and the power meter, and Γ_a represents the reflection voltage coefficient of the receiving antenna at the respective stirrer position.

In Figure 154, we present the probability distribution of the E-field for 100 samples at two distinct frequency points: 700 MHz and 1100 MHz. These measurements were conducted while the chamber was excited with an input power of 29 dBm.

The distribution shown in the figure follows a Rayleigh distribution, which is represented by the theoretical curve. The PDF of a Rayleigh distribution is calculated using the equation provided below:

$$f(|E_0|,\sigma) = \frac{|E_0|}{\sigma^2} e^{-\frac{1}{2}\left(\frac{|E_0|}{\sigma}\right)^2} \quad (95)$$

here, σ^2 signifies the variance of the set of $|E_0|$ samples. In order to align the shape of the distribution, σ functions as a scale parameter that determines the scale of the distribution.

The single complex component of the E-field, including both the real and imaginary parts, follows a normal distribution. Consequently, when we compute the magnitude of the complex E-field, it exhibits a Rayleigh distribution. This is due to the fact that the Rayleigh distribution emerges from the combination of two chi-squared random variables (which represent squared normal distributions) and taking the square root of their sum.

8.3.2.3 Power Received by Blade Antenna Distribution

The received power by the blade antenna within the reverberant environment aligns with the anticipated exponential distribution, consistent with findings in [72]. Figure 155 illustrates the power variations observed at 700 MHz across 100 different stirrer positions within the chamber.

To model this distribution, we calculate the theoretical curve for an exponential distribution using Equation (88).

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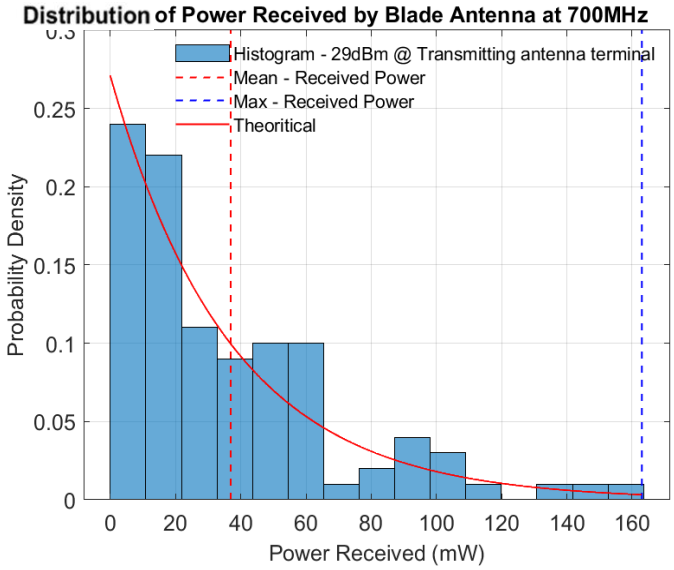

Figure 155: Shows the Probability Distribution of received power from blade antenna at,700MHz: Analysed over 100 stirrer positions, depicting variations in received power for each stirrer position.

8.4 Experimental Validation of Stochastic EM Fields Coupling into ICs via Test RF PCB Traces

In this section, we undertake the validation of the numerical model presented in Section 8.1. This model estimates the stochastic EM fields coupling into realistic loads, such as ICs, through test RF PCB tracks. The validation process involves conducting radiated measurements within a reverberation chamber, utilizing the RF IC detector test bench with the RF IC connected to the test RF PCB tracks, which are mounted on the test bench, as shown in Figure 152.

8.4.1 Measurement Results with Open Tracks

Figure 156: The image shows RF PCB tracks from the test bench setup that are left open, with nothing connected to the MCX connector.

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In this configuration, the terminating ends of the PCB tracks that connect to all sub-channels of the RF IC detector are left open (unconnected MCX connectors), as illustrated in Figure 156. This deliberate choice results in an increase in the forward power at the package pin due to reflections, which is advantageous for the sensitivity of the measurement.

At each stirrer position and frequency point, the coupled power at the package pin is detected by sub-channels 0 to 2 of channels 1 and 2 of the RF IC detector.

8.4.1.1 Average Coupled Forward Power at Package Pin

As discussed in Section 7.2.1, we determine the respective coupled forward power at the package pin of each sub-channel by analysing the voltage output of the RF IC detector in the calibration curves. The integration of these calibration curves into the Python software enables us to calibrate the RF IC detector test bench and record the respective coupled forward power at package pins for all sub-channels at each stirrer position and frequency point.

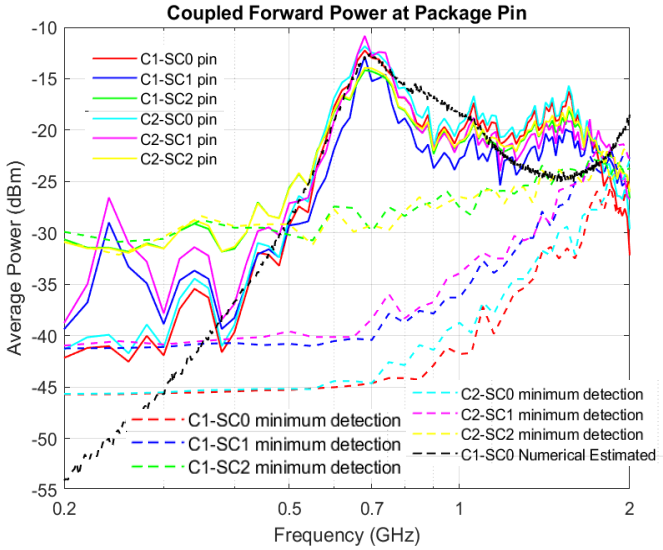

Figure 157: Coupled Forward Power at Package Pin with Open Tracks: Demonstrating power coupling at the package pin when 29dBm of power is supplied at the chamber input.

The average coupled forward power at package pins for sub-channels 0 to 2 of channels 1 and 2 is depicted in Figure 157 with solid lines. The dotted lines in the figure represent the minimum forward power level required for the RF IC detector to detect at least a 10mV output voltage. Since all sub-channel detection exceeds this minimum threshold at 500MHz, all the curves converge and the shape remains almost the same.

In this comparison, we validate the coupling of energy into the loads of the PCB traces by comparing our results with a numerical model based on the Monte Carlo method discussed in Section 8.1. Within the numerical model, we incorporated the input impedance of the respective sub-channel at the IC end. At the terminating end of the track, we applied

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an impedance of 10^9 Ω to resemble the open track scenario of the test bench. Additionally, we integrated all the dielectric properties of the radiated board from Table 7 into the numerical model to derive the curve.

The numerical model curve (black dashed line in Figure 157) closely matches the measurement results from 380MHz to 700MHz. Below 380MHz, the coupled forward power measurement results do not exceed the minimum detection threshold. Above 700MHz, the numerical model shows a slight deviation from agreement with the measurements.

8.4.2 Validation of Statistical Distribution of Coupled Forward Power

8.4.2.1 Distribution of Coupled Forward Power

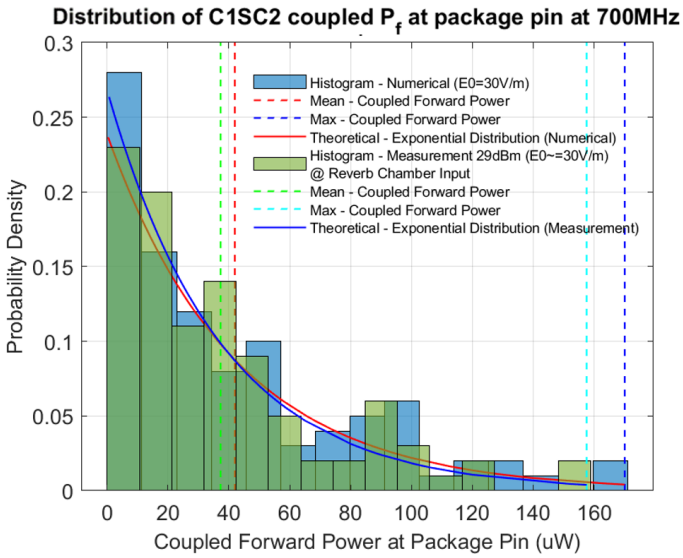

Figure 158: Distribution of coupled forward power at package pin (C1SC2, 700MHz, 30V/m): Analysed over 100 stirrer positions, depicting variations in power coupling at the package pin in measurement and numerically estimated data.

Building upon the discussion in Section 8.2, where we determined that the distribution of coupled forward power at the package pin adheres to an exponential pattern, as shown in Figure 149, this section embarks on the validation of this distribution. Specifically, we are focused on validating the distribution of coupled forward power at the package pin, given the incident field, by leveraging the measurement data that has been detailed in Section 8.4.1.

To carry out this validation, we have compared the numerically estimated data with the measurement results, and the outcome is showcased in Figure 158. It is noteworthy that the measurement results align well with the numerically estimated data.

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8.4.2.2 Cumulative Distribution of Coupled Forward Power

In this section, we undertake the validation of the cumulative distribution of coupled forward power at the package pin, given the incident field, utilizing the measurement data as detailed in Section 8.4.1.

The cumulative distribution of coupled forward power at the package pin, as shown in Figure 159, offers valuable visual insights into various aspects, including the percentage of the area less than the mean value, less than twice the mean value, and the area between the mean (or any chosen point) and the maximum values of the coupled forward power.

In our validation, we compare the measurement results with numerically estimated data, and both datasets exhibit a good alignment with each other, as demonstrated in Figure 159.

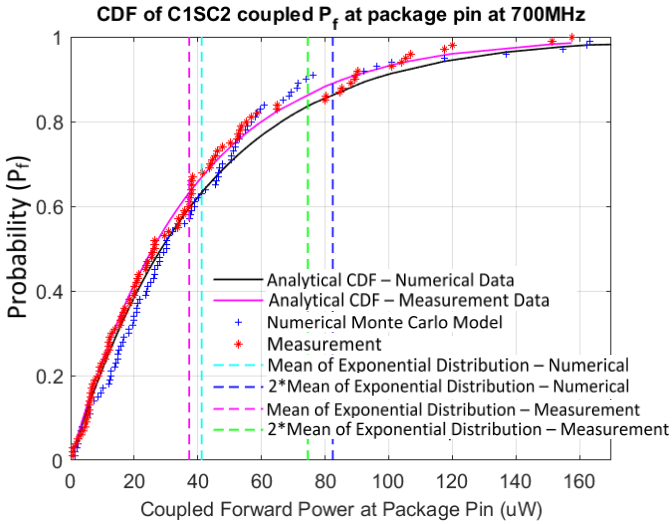

Figure 159: Cumulative Distribution of Coupled Forward Power at Package Pin (C1SC2, 700MHz, 30V/m): Aggregated data over 100 stirrer positions, showcasing the cumulative distribution of power coupling at the package pin in measurement and numerically estimated data.

8.4.2.3 Max/Mean Ratio of Coupled Forward Power at Package Pin

In this section, we embark on the validation of the cumulative distribution of the Max/Mean Ratio of coupled forward power at the package pin, considering the given incident field. This validation process leverages the measurement data detailed in Section 8.4.1.

The Max/Mean Ratio, which represents the ratio between the maximum and mean values of the coupled forward power, provides a quantification of the extent to which the mean value deviates from the maximum value within a specific dataset. As previously discussed in Section 8.2, Wellander [73] has pointed out that there exists a 99% confidence level suggesting that the maximum dB difference between the mean and maximum values will remain at approximately 10 dB across 100 different stirrer positions.

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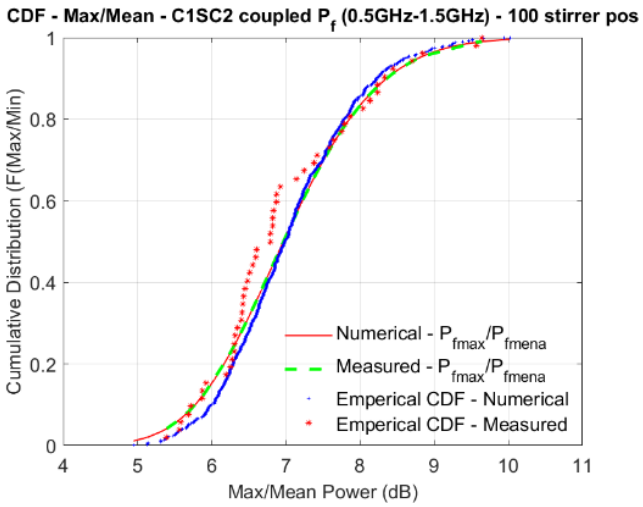

Figure 160: Cumulative Distribution of Max/Mean Power Ratio for Coupled Forward Power at Package Pin (C1SC2, 30V/m): Analysed across 100 stirrer positions in measurement and 100 samples in numerical between 0.5GHz to 1.5GHz with 52 points in measurement and 544 points in the numerical model, highlighting variations in the ratio of maximum to mean power.

During our validation process, we observed a difference in dB ranging from 5.5 dB to 9.5 dB between the maximum and mean values when using 52 measurement data points. The overall shape of the measurement curve remains relatively consistent with the numerically estimated coupled forward power, as shown in Figure 160. However, when the number of data points increases to 544 in numerical simulations, the range of dB difference has expanded from 4.9 dB to 10.1 dB between the maximum and mean values. It is evident that as the number of data points increases, the range of dB differences also widens.

Additionally, it is worth noting that in Figure 160, only one data point from the numerically estimated data exceeds the 10 dB threshold. Out of the 544 data points, this represents less than 0.19% of the total points, with the majority, 99.81%, falling below the 10 dB threshold. In the measurement data, with a smaller number of points, no data points cross the 10 dB difference threshold, resulting in a 0% occurrence. Both the measurement results and the numerically estimated results exhibit a strong alignment with each other, emphasizing the reliability of the methodology.

8.4.3 Validation of Analytical Methodology to Predict the Probability of IC Failure.

In this section, our objective is to validate the analytical methodology used to predict the probability of IC failure based on the coupled forward power at the package pin, under different incident field conditions. This validation is conducted by assuming an absolute maximum power limit of the IC, denoted as P_{ICmax}, for the IC under test.

The left graph of Figure 161 illustrates the coupled forward power distribution of C1SC2 at 700 MHz for various incident field scenarios. We leverage this measurement data to

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validate our methodology for estimating the hypothetical probability of IC failure, using the assumed P_{ICmax}.

To increase the input power of the Reverberation Chamber up to 40dBm, the setup depicted in Figure 200 from Appendix 11.2 is employed.

Our assumption for the absolute maximum power limit of the IC (P_{ICmax}) is 60 µW (-16.61 dBm) at 700 MHz. By plotting theoretical exponential curves using equation (91) in terms of percentage for all three sets of measurement results, as displayed in the right graph of Figure 161, and incorporating the assumed P_{ICmax}, we can visually estimate the hypothetical probability of the power exceeding the assumed P_{ICmax} for these three distinct incident field cases. This estimation can be made either directly from the graph or by using Equation (92).

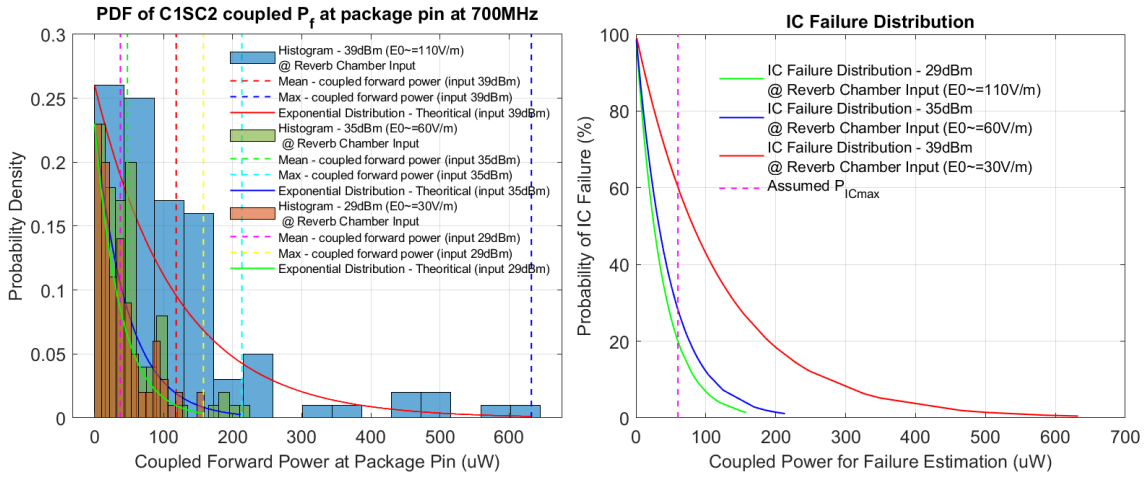

Figure 161: The left figure shows the Distribution of Coupled Forward Power at Package Pin (C1SC2, 700MHz): Based on 100 stirrer positions within the reverberation chamber, showcasing variations with different input power levels in measurements and numerically estimated data. The right figure shows the probability of coupled forward power being greater than assumed $\boldsymbol{P_{ICmax}}$ for different incident fields in the reverberation chamber.

Table 13 provides a summary of the hypothetical probability of IC failure in relation to the given incident field within the reverberation chamber.

Input Power (dBm)	E-field (V/m)	Probability of IC failure (%)
29	30	20.02
35	60	28.25
39	110	60.81

Table 13: Shows the possible probability of IC failure for different incident fields with respect to the assumed $\boldsymbol{P_{ICmax}}$.

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8.5 Correlating Our Prediction Models with Practical Applications

8.5.1 Correlating with Test Specification of EMC Limits for Automotive ICs

In this section, we aim to bridge the gap between theoretical insights and practical applications by establishing a correlation between the test specifications of EMC limits for automotive ICs and our prediction models, which are presented in Sections 8.1 and 8.2.

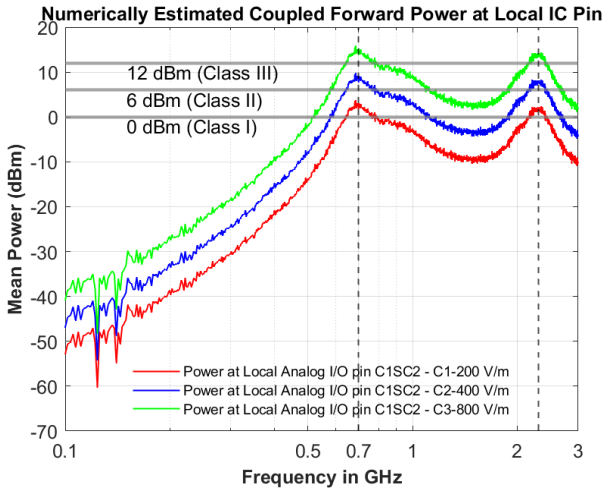

Figure 162: Numerically estimated coupled forward power at local IC pin (C1SC2) for different E-field with an aim to cross the IC EMC limit classes defined for conducted DPI to determine the E-field limit for reverberation chamber.

The EMC limits for automotive ICs, pertaining to conducted immunity (DPI) and radiated immunity (GTEM and IC stripline), are outlined in Section 11.2 of reference [68] and are also mentioned in reference [67]. When the coupled power to the IC under test exceeds the absolute maximum power limit of the IC (P_{ICmax}), the IC may malfunction, based on the specific failure criteria defined by the manufacturer. These failure criteria can take various forms, such as voltage ripple criteria ($\pm 10\%$) or carrier frequency shift criteria (10 kHz), among others.

In cases where the coupled power to the IC surpasses certain thresholds specified in the EMC limits for DPI, as detailed in the test specifications provided in Table 44 of reference [68], the IC is prone to malfunction and may meet one of the predefined failure criteria. To establish a connection between the EMC limits for automotive ICs in test specifications and our prediction models, we make use of general immunity limit classes from these test specifications. By utilizing the DPI limit lines set for both global and local pins of the IC function modules, as outlined in the test specifications, we can estimate the limit lines for radiated immunity test methods that can be applied to Reverberation Chambers.

By utilizing the numerical model presented in Section 8.1, we have estimated the mean coupled forward power at the package pin with PCB tracks for various incident fields. These incident fields have been input into the numerical model to ensure that the maximum

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mean coupled forward power crosses the EMC limit line classes specified for the conducted immunity DPI method, as per the test specification [68]. These EMC limit lines effectively represent the P_{ICmax} for the ICs under test.

In our numerical simulations, we considered 100 samples (equivalent to 100 stirrer positions) at each frequency. At each frequency, the distribution of coupled forward power follows an exponential pattern. The area to the right of the mean value in the exponential distribution is 36.79%, as shown in Figure 150. This percentage corresponds to the probability of IC failure when the coupled forward power exceeds the mean value.

Local Pin C1SC2			
Immunity Limit Classes	**DPI Forward Power (dBm)**	**Freq (GHz)**	**Reverberation Chamber E-field (V/m)**
I	0	0.7 & 2.3	200
II	6	0.7 & 2.3	400
III	12	0.7 & 2.3	800

Table 14: Shows the RF immunity classes correlation between standard DPI limits set for conducted immunity and estimated E-field limit for reverberation chamber radiated immunity test method.

Numerically estimated coupled forward power at the local IC pin (C1SC2) for various incident fields is presented in Figure 162. It is important to note that when the mean value of the coupled forward power crosses the limit line classes at 700 MHz and 2.3 GHz, there is a 36.79% probability of IC failure.

The test specifications in reference [68] outline radiated immunity test methods for GTEM cells and IC striplines. In this context, we establish a correlation between these test methods and the radiated test method for the reverberation chamber. We then estimate the required E-field in the reverberation chamber for the coupled forward power at the local IC pin to cross each EMC limit line class. The specific E-field values are detailed in Table 14.

Similarly, we have plotted the numerically estimated coupled forward power at the global IC pin (VDD5) for different incident fields in Figure 163. When the mean value of the coupled forward power crosses the limit line at 2 GHz, there is a 36.79% probability of IC failure. The corresponding E-field values required in the reverberation chamber for the coupled forward power at the global IC pin are detailed in Table 15.

It's worth noting that while the obtained results for the reverberation chamber immunity test method may not be entirely accurate, the underlying methodology remains unchanged. However, when applied in conjunction with practical automotive IC test bench properties

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into the numerical model, along with the methodology for predicting the required incident E-field for the reverberation chamber immunity method, one can achieve accurate results. Additionally, the methodology for predicting the probability of IC failure for practical automotive IC boards remains applicable.

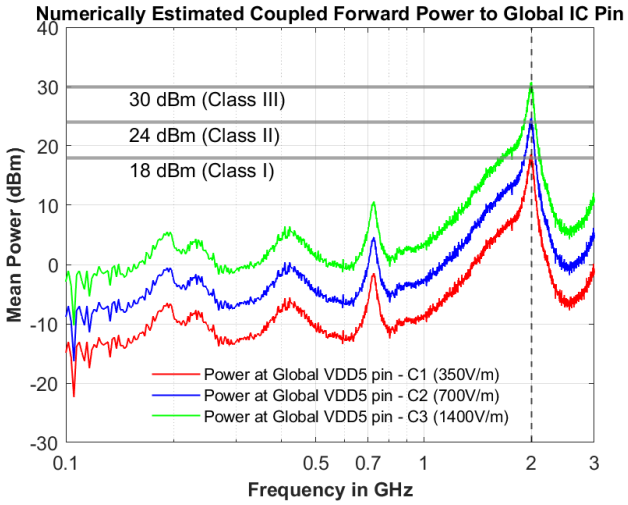

Figure 163: Numerically estimated coupled forward power at global IC pin (VDD5) for different E-field with an aim to cross the IC EMC limit classes defined for conducted DPI to determine the E-field limit for reverberation chamber.

Global Pin VDD5			
Immunity Limit Classes	**DPI Forward Power (dBm)**	**Freq (GHz)**	**Reverberation Chamber E-field (V/m)**
I	18	2	350
II	24	2	700
III	30	2	1400

Table 15: Shows the RF immunity classes correlation between standard DPI limits set for conducted immunity and the estimated E-field limit for reverberation chamber radiated immunity test method.

Conducting immunity tests in a reverberation chamber provides an environment that is closer to real-world conditions compared to limited-direction and polarization-based test methods, such as the GTEM cell and IC stripline methods.

Hence, we increase the E-field in the numerical model in such a way that all the DPI limit lines from [68] fall within the estimated distribution range of the coupled forward power at the local IC package pin, and then we plot the analytically estimated probability of IC failure curve calculated using equation (91) with respect to numerically estimated coupled forward power as demonstrated in Figure 164. This gives us the visual

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representation of the probability of IC failure when the IC under test belongs to Class I, II, or III, as detailed in Table 16.

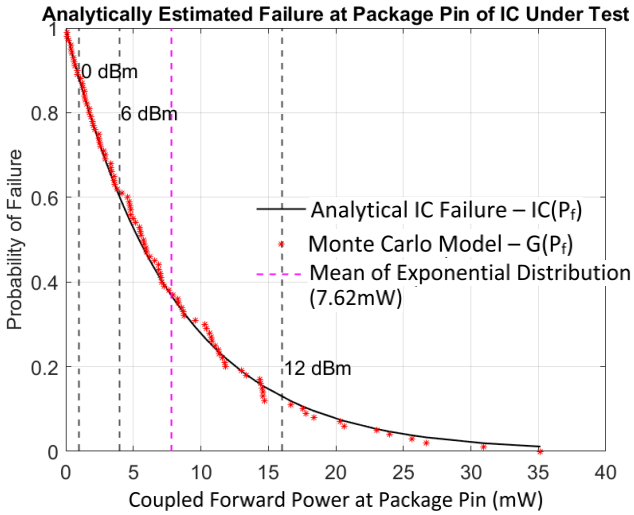

Figure 164: Probability of IC failure with respect to numerically estimated coupled forward power at local IC pin (C1SC2) for 400V/m E-field at 700MHz. From the DPI limit line set for the local pin, we can determine the probability of IC failure if the IC under test belongs to Class I, II or III.

Local Pin C1SC2 at 700MHz for 400V/m	
If IC under test belongs to the Class	**Then the probability of IC Failure is**
I	88.00 %
II	59.97 %
III	12.96 %

Table 16: Shows the probability of IC failure if the IC under test belongs to Class I, II or III for the given E-field at 700MHz.

8.5.2 Correlating with Everyday Electronic Appliances

Let's assume we have a DUT connected to a PCB track with known dielectric properties, categorized as a Class B digital device according to standard FCC 47 CFR Part 15 [74], which includes DUTs from personal computers, calculators and similar electronic devices. If the DUT has a failure level of -20 dBm, it will exhibit a 99.98% probability of failure when exposed to an 80 V/m E-field in a reverberant environment, as shown in Figure 165.

To achieve an acceptable probability of failure, i.e., 0.02% (2 in 10,000 samples), we need nearly 13 times less E-field (6 V/m) around the DUT compared to the E-field required for a 99.98% probability of failure, as illustrated in Figure 166. This type of estimation is

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straightforward using our prediction models, as performing real measurements with 10,000 stirrer positions in a reverberation chamber is challenging and time-consuming.

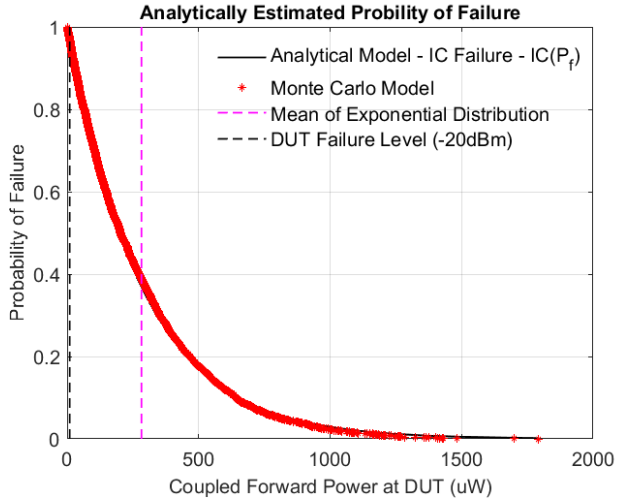

Figure 165: Predicting the probability of IC failure with respect to numerically estimated coupled forward power at DUT for 80V/m E-field at 700MHz for B=10000 samples.

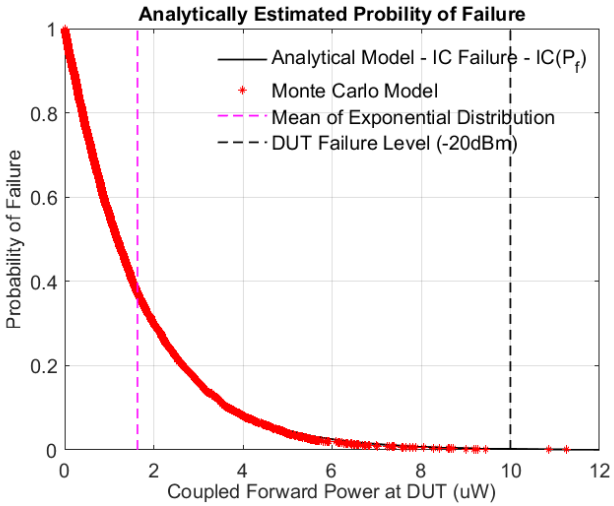

Figure 166: Predicting the probability of IC failure with respect to numerically estimated coupled forward power at DUT for 6V/m E-field at 700MHz for B=10000 samples.

In conclusion, this chapter began with the introduction of a numerical model capable of accounting for PCB losses in estimating the stochastic EM fields coupling to PCB traces. We then presented an analytical methodology for predicting the susceptibility of ICs. Subsequently, we validated the numerical model with radiated measurements conducted in a reverberation chamber using the RF IC detector test bench. Lastly, we established a correlation between the practical applications and our prediction models.

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9. Influence of Stochastic EM Fields Coupling into PCB Traces and IC Package Pins Using Power Balance Method

In Chapter 3, we established the fundamental definitions of SE and the PWB method. In this chapter, we introduce an enhanced PWB method by incorporating the influence of AACS of the IC at package pins (including package, lead frame, bond wires and internal chip), as well as the interconnected RF PCB tracks, along with all other AACS associated with the internal components housed within the enclosure.

Previous research, rooted in the PWB method [11], has underscored the pivotal significance of comprehending the energy absorbed by enclosure contents and the ATCS to determine both SE and internal fields. The PWB method, initially developed by Hill and Juqua et al. [13] and [14], has also highlighted that fields within a shielded enclosure and the SE are influenced by both the TCS of coupling apertures and the ACS of the contents. This method offers direct and efficient solutions for reverberant enclosures, avoiding the need for computationally intensive full-wave solvers by treating fields as uniform and isotropic and utilizing average values for TCS and ACS [15].

The methodologies outlined in [6–8] and the insights drawn from these results are pivotal for discerning the AACS of internal components within the enclosure, a critical aspect in developing the enhanced PWB method. Studies in [6], [7], [16] demonstrate that calculating the power absorbed by loads on PCB traces is fundamental for determining the AACS of the PCB trace and its relationship with the PWB method. This is vital in determining the power absorbed by internal contents within shielded enclosures. The power absorbed by realistic loads, such as ICs on PCB traces, significantly influences the AACS of the tested PCB. Hence, developing an enhanced PWB method that incorporates the AACS of the IC at package pins and interconnected PCB tracks, alongside other relevant AACS linked to internal components, is imperative.

This chapter introduces an enhanced PWB method that builds upon existing methodologies. It starts by discussing radiated measurements conducted with terminated RF PCB tracks in the RF IC detector's test bench. This study examines the influence of the AACS of RF PCB tracks and IC package pins (including package, lead frame, bond wires and internal chip) by comparing shielding and non-shielding scenarios for the RF IC. Additionally, the chapter presents power flow analysis and measurements aimed at developing the enhanced PWB method. This analysis of AACS, including critical elements like PCB tracks and ICs on the DUT, signifies a slight advancement in traditional PWB methodologies.

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9.1 Measurement Results with Terminated Tracks

This section provides an insight into the AACS of both the PCB tracks and the IC itself (including package, lead frame, bond wires and internal chip). This understanding will assist in determining whether significant coupling is occurring from the PCB tracks or at the IC package pins. This knowledge will, in turn, contribute to a detailed analysis of the PWB method in the subsequent sections.

9.1.1 Measurement Setup

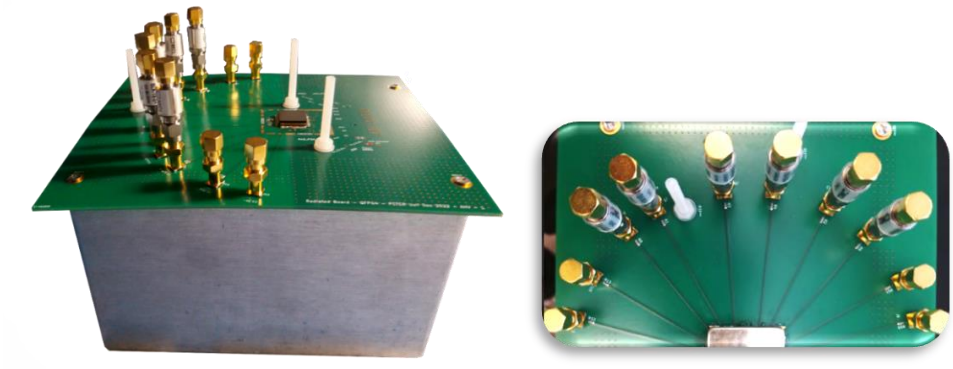

Figure 167: The assembled test setup featuring the radiated PCB board at the top, with all PCB tracks terminated by 50Ω loads for accurate evaluation.

The measurements presented in this section offer a deeper understanding of the AACS and average power absorbed by realistic loads such as IC pins (including package, lead frame, bond wires and internal chip) connected to PCB tracks when exposed to radiated fields inside the reverberation chamber. One end of each PCB track is connected to one of the input sub-channels of the RF IC detector, representing the realistic loads. The other end of the PCB tracks is terminated with a 115 Ω matched load, to match the characteristic impedance (115 Ω) of the traces as shown in Figure 167 (detailed information on the construction of the top radiated board is presented in Section 6.6).

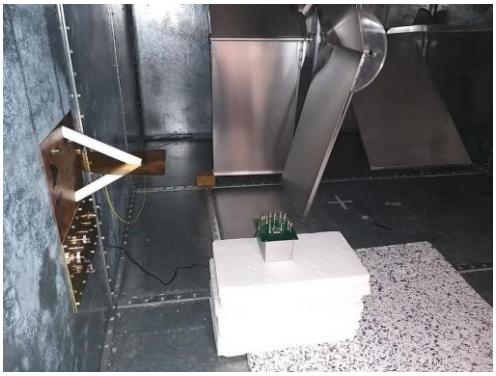

Figure 168: Shows the measurement picture inside the reverberation chamber taken during the measurement of AACS of IC and test PCB tracks.

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The measurement setup for comprehending the power coupling into IC package pins via PCB tracks when the tracks are terminated remains identical to the setup presented in Section 8.3, as illustrated in Figure 151.

By assessing the measurements in this section, we gain insights into the influence of AACS of RF PCB tracks and RF IC with and without shielding the RF IC on the test bench.

9.1.2 Chamber E-field and Received Power

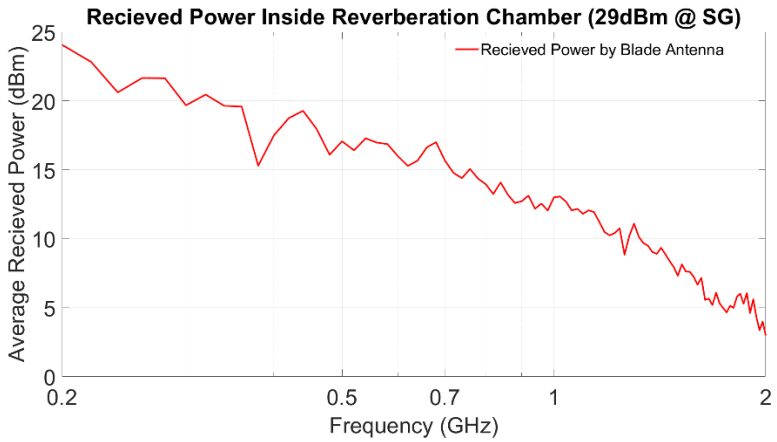

Figure 169: Shows the average received power from the receiving blade antenna inside the Reverberation Chamber over 100 stirrer positions when 29dBm of forward power is given to the transmitting antenna of the chamber.

Throughout the radiated measurements conducted using the setup shown in Figure 151, the E-field is monitored at each stirrer position by measuring the received power from the receiving antenna, and the E-field is calculated using equation (94). The resulting average received power by the receiving blade antenna within the reverberation chamber, in relation to frequency, is presented in Figure 169. Based on this average received power, the calculated E-field is graphically represented in Figure 170 with respect to frequency.

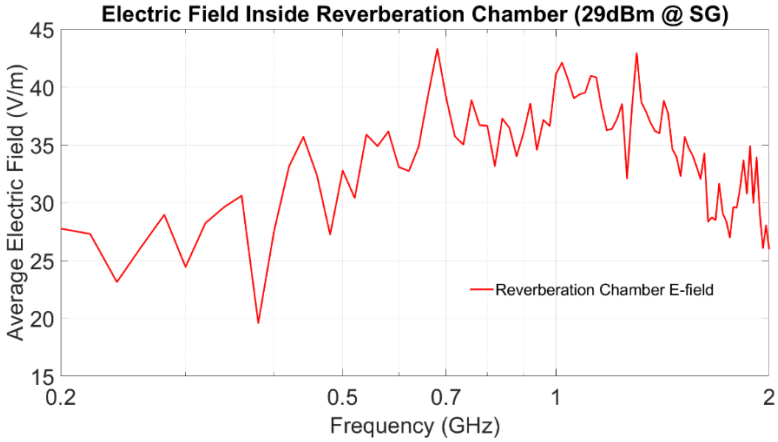

Figure 170: Shows the average E-filed inside Reverberation Chamber over 100 stirrer positions when 29dBm of forward power given to the transmitting antenna of the chamber.

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9.1.3 Average Coupled Forward Power at Package Pin

As discussed in Section 6.6, the RF PCB tracks of the radiated board have a characteristic impedance of 115 Ω. To ensure compatibility with the external 50 Ω system during conducted measurement and testing, a series resistance of 65 Ω is added to the track end that connects to the MCX connector. The sub-channels from the RF IC detector do not have an internal DC block and no DC block between each package pin and MCX connector. To prevent any load affecting the RF IC detector bias voltage, the PCB tracks are terminated with a DC block in between the PCB track and 50 Ω load.

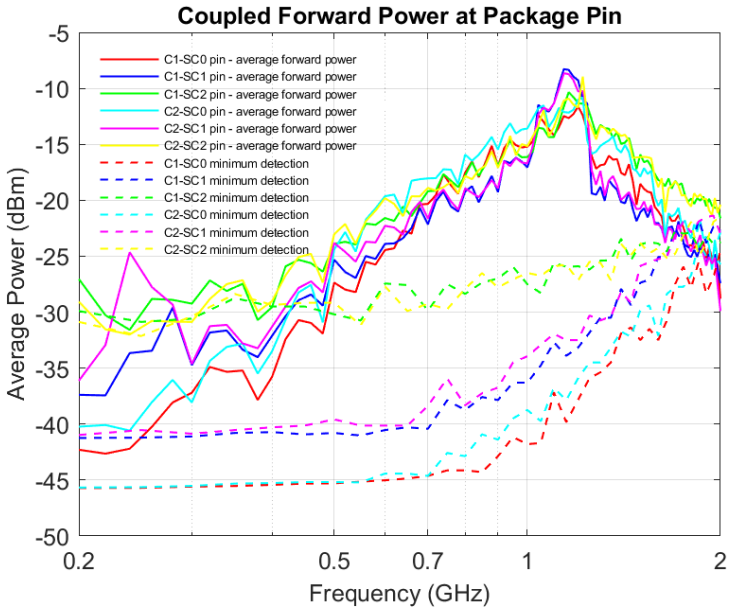

Figure 171: Coupled Forward Power at Package Pin with Terminated Tracks: Demonstrating power coupling at the package pin with terminated tracks, when 29dBm of forward power is given to the transmitting antenna of the chamber.

The average coupled forward power at package pins for sub-channels 0 to 2 of channels 1 and 2 is depicted with solid lines in Figure 171 for 29dBm of forward power given to the transmitting antenna of the chamber. The dotted lines in the figure represent the minimum forward power level required for the RF IC detector to detect at least a 10mV output voltage. Similar to the open track case, all sub-channel detection exceeds this minimum threshold at 500MHz, and thus, all the curves converge while retaining a nearly identical shape.

We are presenting the results for all sub-channels from channels 1 and 2 in this chapter, with the exception of sub-channel 3, which is the differential amplifier channel. The primary purpose of this sub-channel is to test the operation of the IA in both channels, as discussed in Section 7.2.4.4. During radiated measurements, this channel remains non-responsive, as it lacks any peak detector circuit block or pre-amplification circuit block.

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9.1.4 Average Absorbed Power at Package Pin

Similar to coupled forward power, we can determine the respective absorbed power at the package pin (including package, lead frame, bond wire and internal chip) of each sub-channel by analysing the voltage output of the RF IC detector in the calibration curves. The calibration curves for absorbed power are also integrated into the Python software, enabling us to record the absorbed power at package pins for all sub-channels at each stirrer position and frequency point.

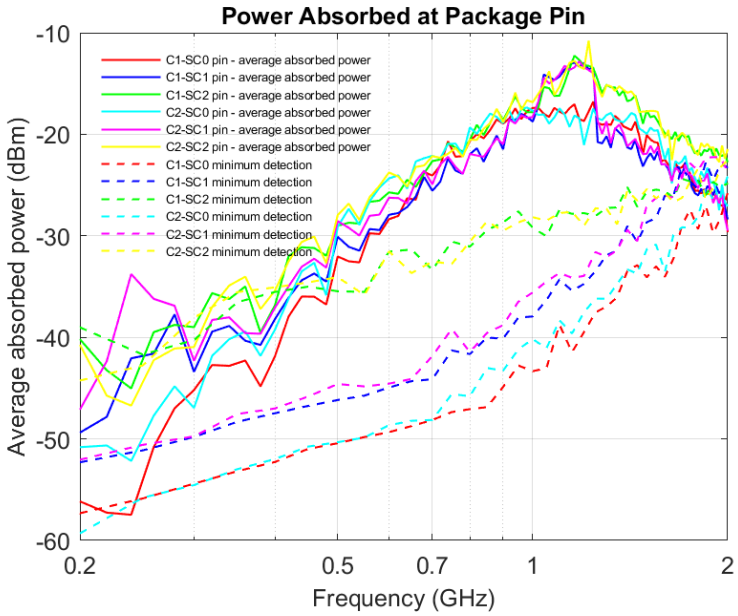

Figure 172: Absorbed Power at Package Pin with Terminated Tracks: Evaluating absorbed power at the package pin when tracks are terminated when 29dBm of forward power is given to the transmitting antenna of the chamber.

The average absorbed power at package pins (including package, lead frame, bond wires and internal chip) for sub-channels 0 to 2 of channels 1 and 2 is shown in Figure 172 with solid lines. The dotted lines in the figure represent the minimum absorbed power level required for the RF IC detector to detect at least a 10mV output voltage.

9.1.5 Average Absorption Cross-Section at Package Pin

The AACS at the package pin (including package, lead frame, bond wire and internal chip) can be determined from the absorbed power at the package pin for a given incident field using the equation provided below:

$$\langle \sigma_a \rangle_{pin} = \frac{\langle P_a \rangle_{pin}}{S_o} = \frac{\langle P_a \rangle_{pin} \eta_0}{E_0^2} \tag{96}$$

here, $\langle P_a \rangle_{pin}$ represents the average absorbed power at the package pin (including package, lead frame, bond wire and internal chip), and S_o denotes the power density within the chamber

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The AACS at the package pin of sub-channels 0 to 2 of channels 1 and 2 are depicted in Figure 173 when the tracks are not terminated.

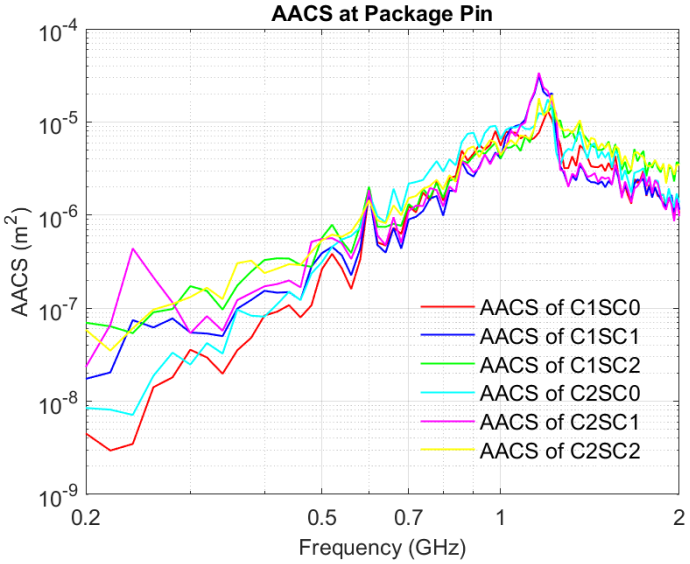

Figure 173: Average Absorption Cross-Section at Package Pin with Terminated Tracks: Analysis when 29dBm of forward power is given to the transmitting antenna of the chamber, revealing absorption characteristics with tracks terminated.

9.1.6 With and Without RF IC Detector Shielding

Here, we conduct a comparison of absorbed power at the package pin with and without shielding the RF IC in the test bench. This enables us to isolate and determine the power coupling attributed specifically to the RF IC detector package pins and the IC itself (including package, lead frame, bond wires and internal chip).

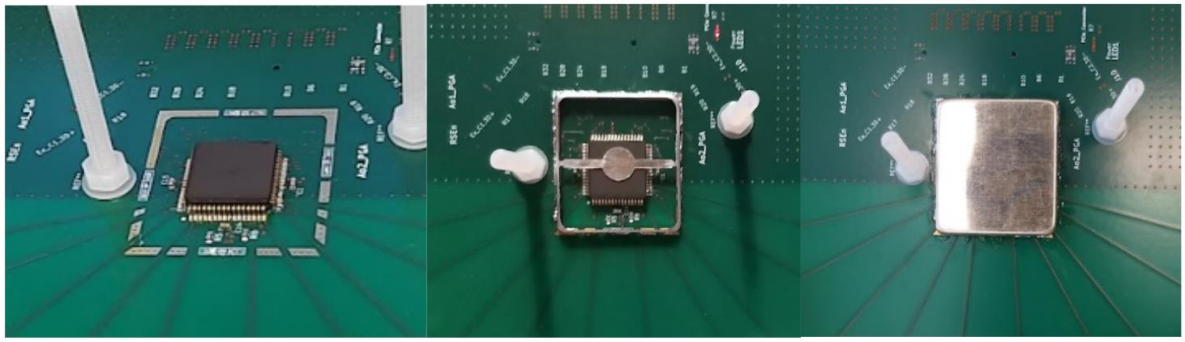

Figure 174: Comparison of Configurations: The first image displays the setup without frame and shield, the second image with the frame only, and the third image with both frame and shield.

In Figure 174, we present images of the RF IC detector test bench: one without a frame and shield, another with only a shielding frame, and a third with the RF IC shielded on the test bench.

Figure 175 illustrates that the results with and without shielding are nearly identical. This suggests that the dominant power coupling is from the PCB tracks, making the

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coupling due to RF IC package pins and the IC itself negligible. This suggests that shielding the IC without shielding the PCB tracks makes the component unprotected from EMI.

Notably, at 900MHz and 1.2GHz, we observe a significant variation in power coupling due to the shielding frame. This variation in coupling is attributed to the presence of the shielding frame, as corroborated by Figure 175, where the results with the frame and with full shielding are similar compared to the results without the shielding frame. Thus, the discrepancy observed in Figure 175 is primarily attributable to the shielding frame.

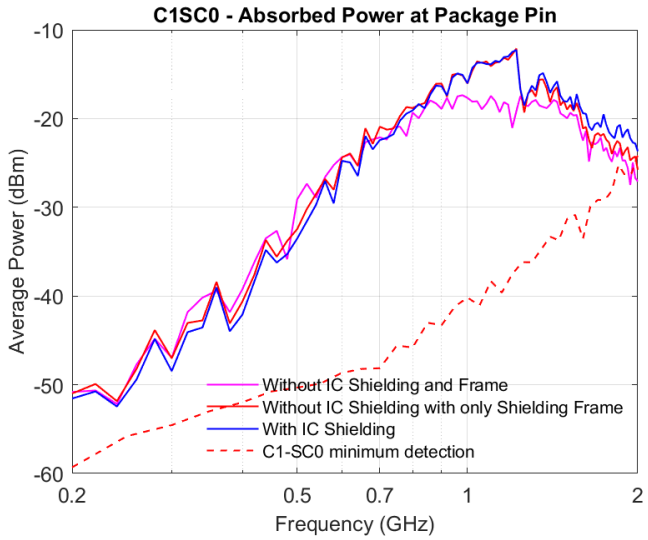

Figure 175: Comparison of Absorbed Power at Package Pin: Evaluating average absorbed power on the RF IC detector with and without shielding, with tracks terminated, when 29dBm of forward power is given to the transmitting antenna of the chamber.

9.2 Power Flow Analysis for Enhanced Power Balance Method

As we discussed at the beginning of this chapter, previous research, based on the PWB method [11], stressed the importance of the AACS of the contents and the ATCS of the shielded enclosures for the assessments of SE and internal fields. Consequently, this section outlines the power flow analysis to determine the AACS of internal components and ATCS of the enclosure, leveraging measured E-field and SE.

Figure 176 illustrates the power flow diagram used to analyse the enhanced PWB method. It provides a visual representation of the power distribution, power absorption, and the flow of power both inside and outside the enclosure concerning the power density within the enclosure and in the external space, which in this context, refers to the power density in the reverberation chamber.

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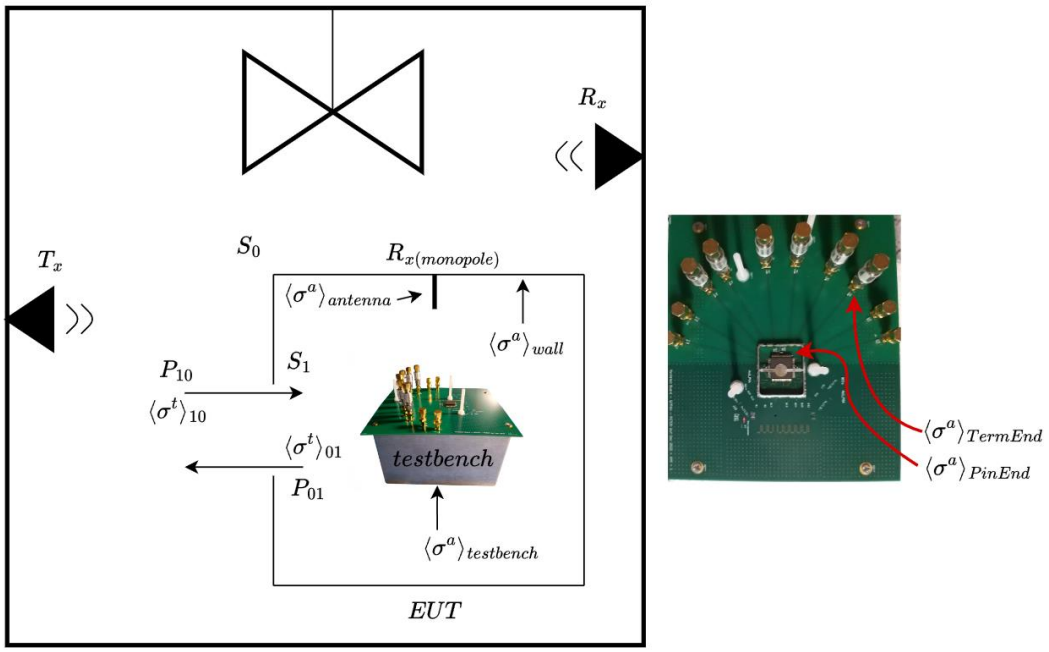

Figure 176: Power Flow Diagram for Power Balance Method: Illustrating the distribution and flow of power within the PWB method.

The fundamental definition of the PWB method is discussed in Section 3.3. In a steady state, power balance requires:

$$\langle P_{10}\rangle = \langle P_{01}\rangle + \langle P_a\rangle \tag{97}$$

here, $\langle P_{10}\rangle$ represents the average power flow into the enclosure due to S_0, and $\langle P_{01}\rangle$ is the average power flow out of the enclosure due to S_1.

The power flow through the apertures or enclosure lid gaps can be expressed as:

$$\begin{aligned}\langle P_{10}\rangle &= \langle {\sigma^t}_{10}\rangle S_0 = \langle\sigma^t\rangle S_0\\ \langle P_{01}\rangle &= \langle {\sigma^t}_{01}\rangle S_1 = \langle\sigma^t\rangle S_1\end{aligned} \tag{98}$$

where, $\langle {\sigma^t}_{10}\rangle$ is the total ATCS of the aperture for energy travelling into the enclosure and $\langle {\sigma^t}_{10}\rangle$ is the total ATCS of the aperture for energy travelling out of the enclosure. In reverberant case $\langle {\sigma^t}_{10}\rangle = \langle {\sigma^t}_{01}\rangle = \langle\sigma^t\rangle$.

Consequently, equation (97) can be rewritten as:

$$\langle\sigma^t\rangle S_0 = \langle\sigma^t\rangle S_1 + \langle\sigma^a\rangle_{tot} S_1 \tag{99}$$

The SE in terms of AACS and ATCS can be expressed as follows:

$$SE = \frac{S_0}{S_1} = \frac{\langle P_{10}\rangle}{\langle P_{01}\rangle} = \frac{\langle\sigma^t\rangle + \langle\sigma^a\rangle_{tot}}{\langle\sigma^t\rangle} = 1 + \frac{\langle\sigma^a\rangle_{tot}}{\langle\sigma^t\rangle} \tag{100}$$

From the above equation, we can also determine the total ATCS of all the apertures of the shielding enclosure:

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$$\langle \sigma^t \rangle = \frac{\langle \sigma_a \rangle_{tot}}{SE - 1} \tag{101}$$

The total AACS of the inner components is given by:

$$\begin{aligned} \langle \sigma^a \rangle_{tot} &= \langle \sigma^a \rangle_{test\ bench} + \langle \sigma^a \rangle_{antenna} + \langle \sigma^a \rangle_{inner\ wall} \\ \langle \sigma^a \rangle_{test\ bench} &= \langle \sigma^a \rangle_{10\ tracks} + \langle \sigma^a \rangle_{PCB\ Dielectctic} + \langle \sigma^a \rangle_{testbench\ shield} \\ &\quad + \langle \sigma_a \rangle_{IC\ pins} \end{aligned} \tag{102}$$

where, $\langle \sigma^a \rangle_{test\ bench}$ is the AACS of the RF IC detector test bench, $\langle \sigma^a \rangle_{antenna}$ is the AACS of the monopole antenna mounted on the top lid of the enclosure, $\langle \sigma^a \rangle_{inner\ wall}$ is the AACS of the inner wall of the enclosure, $\langle \sigma^a \rangle_{10\ tracks}$ is the total AACS of the ten 60mm test tracks on the RF IC detector test bench, $\langle \sigma_a \rangle_{IC\ pins}$ is the AACS of the package pins (including package, lead frame, bond wires and internal chip) of the IC mounted on the RF IC detector test bench, $\langle \sigma^a \rangle_{PCB\ Dielectric}$ is the AACS of the PCB dielectric of the RF IC detector test bench, and $\langle \sigma^a \rangle_{testbench\ shield}$ is the AACS of the control board shielding (including the micro USB cable connected to the test bench) of the RF IC detector test bench.

It is worth noting that, as discussed in Section 9.1.6, the power absorbed by the PCB track dominates over the power absorbed by the package pins including the package, lead frame, bond wires and internal chip ($\langle \sigma^a \rangle_{track} \gg \langle \sigma^a \rangle_{IC\ pin}$). This observation is supported by results obtained both with and without shielding on the RF IC detector on the test bench as shown in Figure 175.

Therefore, $\langle \sigma^a \rangle_{test\ bench}$ can be represented as:

$$\langle \sigma^a \rangle_{test\ bench} \approx \langle \sigma^a \rangle_{10\ tracks} + \langle \sigma^a \rangle_{PCB\ Dielectric} + \langle \sigma^a \rangle_{testbench\ shield} \tag{103}$$

9.3 Measurement Setups for Power Flow Analysis

9.3.1 Setup 1 with General DUT

Figure 177 illustrates the measurement setup employed for measuring the AACS of any absorbing component (DUT) within a reverberation chamber. These measurements encompass 100 stirrer positions, ranging from 200 MHz to 10 GHz, with a 5 MHz step increment at each stirrer position. Port 1 of the VNA [55] is connected to the transmitting antenna, while port 2 is connected to the receiving antenna within the chamber. The VNA and the stirrer inside the chamber are monitored by an external computer.

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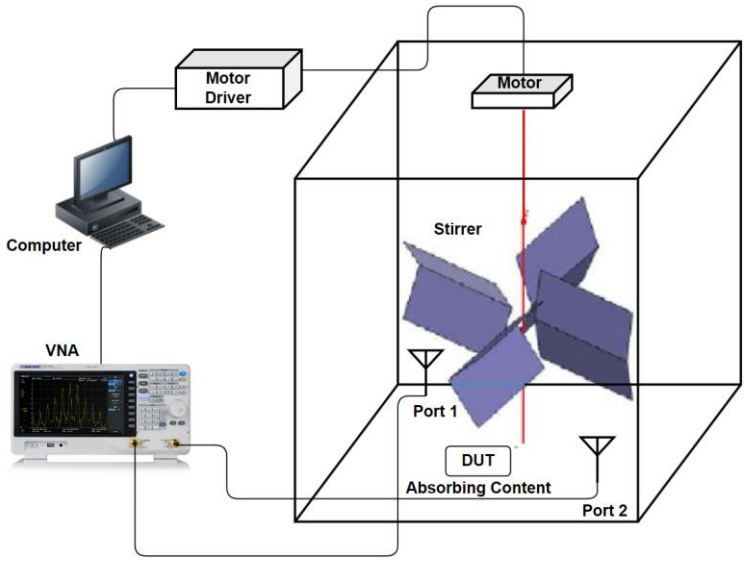

Figure 177: Shows the measurement setup to measure the AACS of any absorbing component.

9.3.2 Setup 2 with Shielding Enclosure

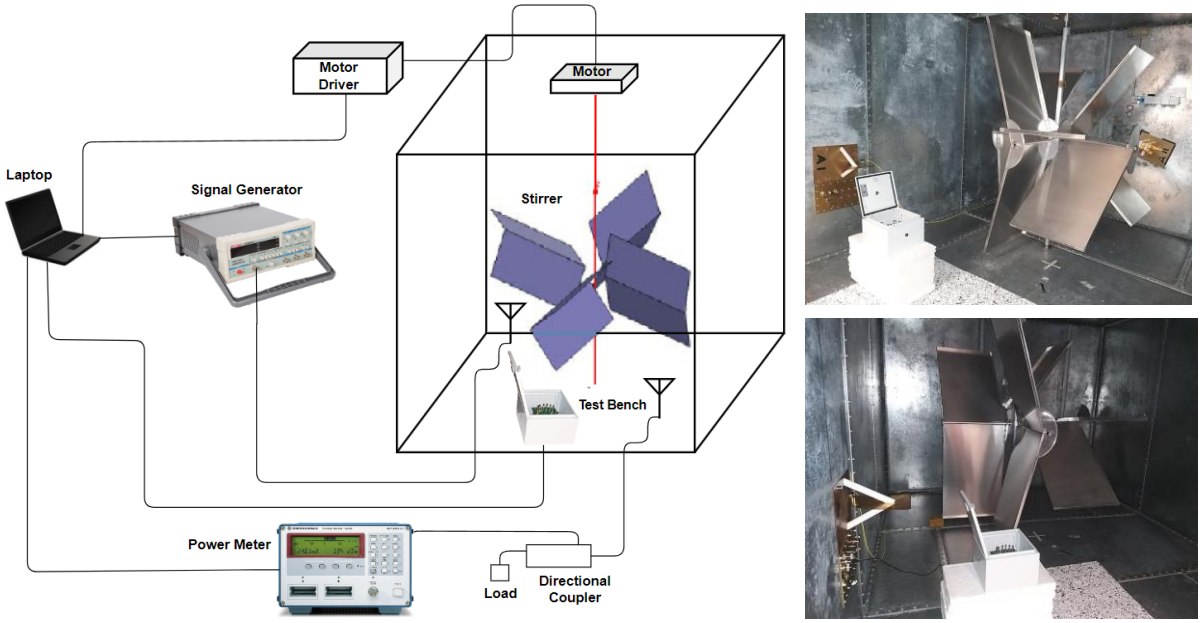

Figure 178: Shows the measurement setup to measure AACS of PCB tracks and IC package pins when the entire RF IC detector test bench is kept inside the shielding enclosure. Also shows the pictures taken during the measurement.

The measurements conducted using this setup provide a deeper understanding of the AACS of realistic loads, such as ICs connected via test RF PCB tracks, when exposed to radiated fields inside the reverberation chamber (Section 3.2.2). One end of each PCB track is connected to various input sub-channels of the RF IC detector, representing the realistic loads. The other end of the PCB tracks is terminated with a 115 Ω load, which aligns with the characteristic impedance of the RF PCB track.

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Figure 178 shows the measurement setup used to measure AACS of PCB tracks and IC package pins when the entire RF IC detector test bench is kept inside the shielding enclosure within a reverberation chamber. These measurements cover 100 stirrer positions spanning from 200 MHz to 2 GHz, with a 20 MHz step increment. The E-field inside the chamber and enclosure is monitored at each stirrer position by measuring the received power from the receiving antenna using a power meter. To measure the internal E-field of the enclosure, the power meter is connected to the internal monopole receiving antenna, while to measure the chamber's E-field, the power meter is connected to the receiving blade antenna of the chamber. Coupling to each detector channel is measured by the test bench and transmitted to the instrument controller by the USB interface of the Arduino processor. The measurement equipment, including the PCB test bench of the RF IC detector, is monitored using Python software. Later the coupled power signals for each sub-channel are used to determine the AACS of the test PCB tracks and package pin of IC.

9.3.3 Shielding Enclosure

Figure 179: Shows a picture of the monopole antenna mounted on the closing lid of the enclosure when the enclosure is empty and with a testbench.

The shielding enclosure employed for power flow analysis has dimensions of 300mm in length, 300mm in width, and 210mm in height. It is constructed from low carbon sheet steel and painted in grey colour. The enclosure is characterized by imperfect shielding due to the presence of a rubber gasket between the lid and the enclosure. This gasket creates a gap between the lid and the enclosure. This gap is advantageous in our context as it behaves as an aperture for energy exchange with an external chamber. This is essential for the RF IC detector to detect signals, enabling us to deduce the coupled power to realistic

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loads such as ICs via test RF PCB tracks and to monitor the E-field inside the chamber using received power data from the internal monopole antenna (40mm). Images of the shielding enclosure, monopole antenna mounted on the closing lid, and RF IC detector testbench inside the enclosure can be seen in Figure 179.

9.3.3.1 First Resonance of Enclosure

If we consider integer n=0, we can calculate the lowest resonant frequency using equation (5) from Section 3.2.1:

$$f_{resonant} = \frac{c_0}{2}\sqrt{\left(\frac{m}{a}\right)^2 + \left(\frac{p}{c}\right)^2} \approx 700MHz \qquad (104)$$

According to the BS EN 61000-4 standard [28], it is possible for the enclosure to become reverberant at a frequency slightly above three times the enclosure's first resonance. Therefore, 2.1GHz is the LUF to make the enclosure reverberant.

9.3.3.2 Number of Modes Inside the Enclosure

The number of modes inside the enclosure below a given frequency can be calculated using equation (6) from Section 3.2.1. To determine the number of modes, a rule of thumb (also discussed in Section 3.2.2) suggests that the cavity or enclosure can be considered reverberant at frequencies above 60th mode. Therefore, based on Figure 180, we can assume that the enclosure becomes reverberant above 2.1 GHz.

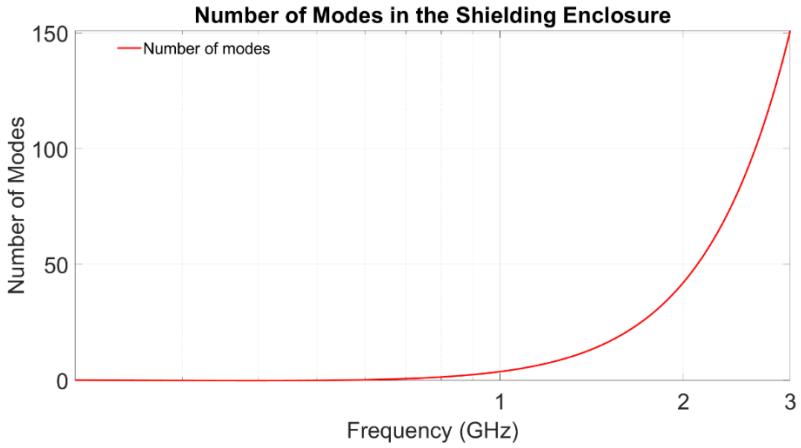

Figure 180: Shows the number of modes inside the shielding enclosure below the given frequency

Even though the enclosure might be considered fully reverberant at frequencies above 2.1 GHz, it is important to note that due to the enclosure's gap with a lid acting as an aperture and its placement within the reverberation chamber with a LUF of 180 MHz, some semi-reverberant fields may exist inside the enclosure at frequencies below 2.1 GHz.

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9.4 E-field inside the Chamber and Enclosure

As previously detailed in Sections 3.3 and 9.2, the significance of power density in power flow analysis has been explored. Access to E-field data within the enclosure and outside the enclosure is important to calculate the power density both inside the enclosure and outside the enclosure (chamber).

As discussed in Section 9.3.2, we monitored the E-field inside the chamber and the enclosure at each stirrer position by measuring the received power from the receiving antenna using a power meter. The average received powers inside the chamber by the blade antenna and inside the enclosure by the monopole antenna, with the enclosure's lid both open and closed, is shown in Figure 181.

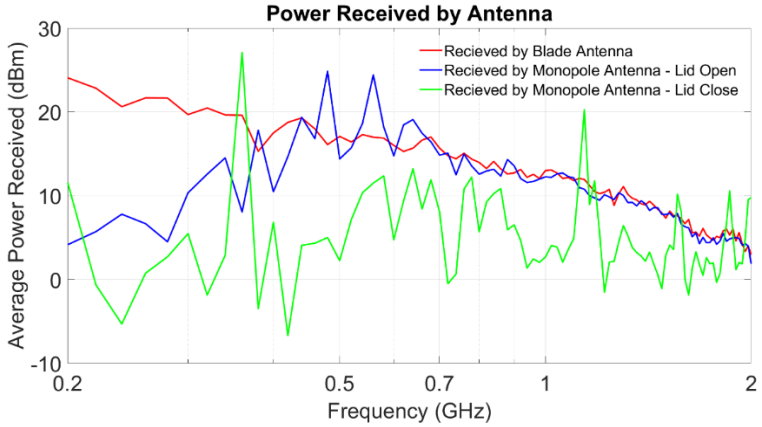

Figure 181: Shows the average received power in the chamber by the blade antenna and inside the enclosure by the monopole antenna, with the enclosure's lid both open and closed.

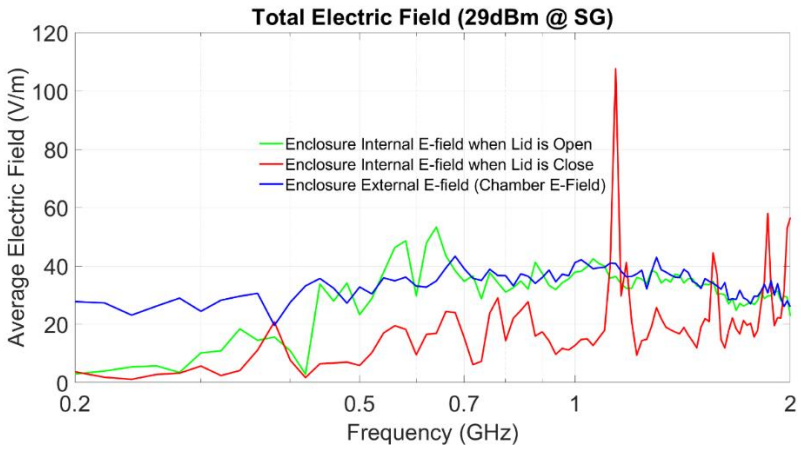

Figure 182: Shows the average E-field inside the chamber and inside the enclosure, with the enclosure's lid both open and closed.

From Figure 181, we can observe that the average received power from the monopole antenna aligns well with the average received power from the blade antenna inside the chamber starting from 500 MHz. This is because the efficiency of the monopole antenna

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is not good enough below 500MHz. As expected, we can also see a reduction in received power when the enclosure's lid is closed.

The average E-field inside the chamber and the enclosure is calculated using Equation (94) by incorporating the average received power. Figure 182 illustrates the calculated average E-fields. As discussed in Section 9.3.3, even though we are operating below 2.1 GHz, we can still observe some uniformity in the internal E-field, which is attributed to the enclosure being kept inside a well-stirred reverberation chamber.

The PDF distribution of the internal and external (chamber) E-fields at 700 MHz is visualized in Figure 183. As detailed in Section 8.3.2.2, the E-field follows a Rayleigh distribution, and the theoretical curve is plotted using Equation (95).

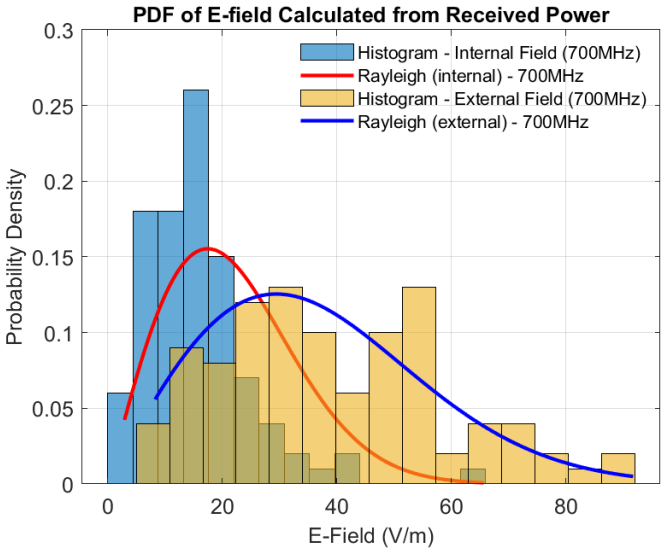

Figure 183: Shows the internal and external (chamber) E-field distribution of the enclosure.

9.5 Shielding Effectiveness

As previously discussed in Section 9.2, the determination of ATCS relies on knowledge of the SE and the internal AACS of the enclosure.

Measurement setup 1 (Section 9.3.1) is used to calculate the SE, but port 2 of the VNA is connected to the monopole antenna placed on the closing lid of the enclosure instead of the chamber's blade antenna. The fundamental definition of SE is detailed in Section 3.1. In this section, we present the SE of the enclosure both when the RF IC detector test bench is present and when it is absent. To assess the impact of a larger aperture on SE, we also conducted measurements with the aperture open. Figure 184 shows the pictures taken during measurement. The SE is calculated using the equation (4) from Section 3.1, as shown below:

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$$SE = \left(\frac{\langle |S_{21} - \langle S_{21} \rangle|^2 \rangle_{open}}{\langle |S_{21} - \langle S_{21} \rangle|^2 \rangle_{close}} \right) \quad (105)$$

where, S_{21} is the transmission coefficient between the transmitting blade antenna and the receiving monopole antenna.

Figure 184: Shows the pictures during the measurement of SE.

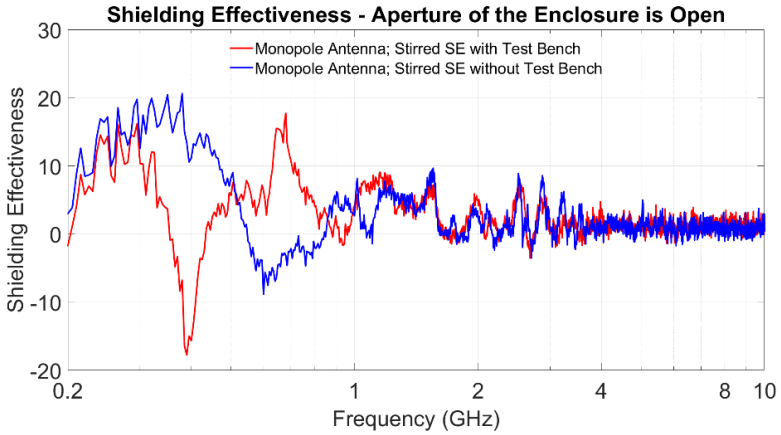

Figure 185: Shows the SE of the enclosure when the aperture of the enclosure is open with the presence of a test bench and without the presence of a test bench.

Figure 185 shows the SE with the aperture open, indicating some variations below the LUF, and beyond that frequency, the SE stabilizes. Notably, due to the presence of a test bench inside the enclosure and the inefficiency of the monopole antenna below 500MHz, negative SE is observed at 300MHz (below LUF), which is persistent in both case when the aperture is open and closed as shown in Figure 185 and Figure 186. Additionally, due to the presence of a rubber gasket in the closing lid, the enclosure is characterized by

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imperfect shielding, allowing power to flow not only through the aperture but also through the lid gap.

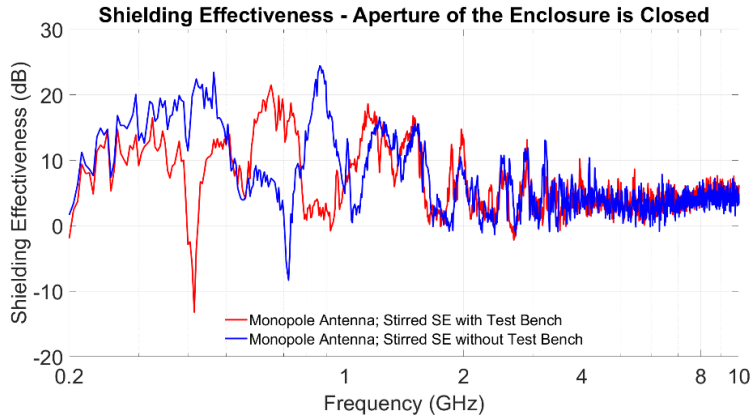

Figure 186: Shows the SE of the enclosure when the aperture of the enclosure is closed with the presence of a test bench and without the presence of a test bench.

It is observed that the SE with the closed aperture is low enough to detect the E-field inside the enclosure, as illustrated in Figure 186. As discussed in Section 9.3.3, the low SE is attributed to the presence of the rubber gasket in the closing lid, which creates a gap between the lid and the enclosure. This gap is beneficial in our context, as it behaves as an aperture for energy exchange with an external chamber, essential for the RF IC detector to detect the coupled power inside the shielding enclosure. Consequently, for further measurements, the enclosure with the closed aperture is the focus.

9.6 Average Absorption Cross-Section

As previously outlined in Section 9.2, the calculation of ATCS depends not only on determining the SE of the enclosure but also on determining the total AACS of the internal components within the enclosure. Therefore, in this section, we will assess the AACS of the internal contents of the enclosure individually.

9.6.1 AACS Verification in Reverberation Chamber using LS22 RAM

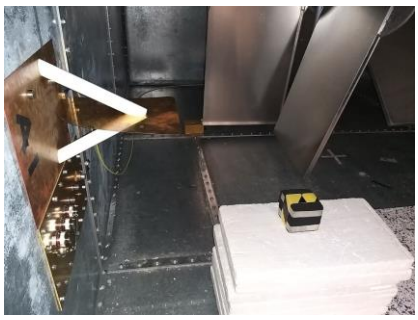

Figure 187: Shows the picture of LS22 RAM (radio-absorbing material) inside the reverberation chamber during the measurement.

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To ensure the validity of the measurements carried out in the UoY's large Reverberation Chamber for assessing the AACS of the absorbing contents, this section involves a comparison with earlier work [75]. This prior study involved measuring the AACS of LS22 RAMs with various dimensions within the UoY's small Reverberation Chamber with dimension of 0.8m x 0.7m x 0.6m.

The AACS of the LS22 RAM inside the chamber can be calculated using equations (32) and (33) as indicated below:

$$\langle \sigma^a \rangle_{LS22\ RAM} = \frac{\lambda^2}{8\pi}\left(\frac{1}{G_{with}} - \frac{1}{G_{without}}\right) \tag{106}$$

where, G_{with} is the transfer function with the absorbing content, and $G_{without}$ is the transfer function without the absorbing content.

To measure the AACS of LS22 RAMs, we utilize the measurement setup 1 described in Section 9.3.1. The measurement results are presented in Figure 188. It is evident that the AACS of LS22 RAMs, as measured in the large Reverberation Chamber, remains accurate down to $10^{-3}\,m^2$. Beyond this threshold, the chamber's sensitivity diminishes, and it cannot detect the absorbing content.

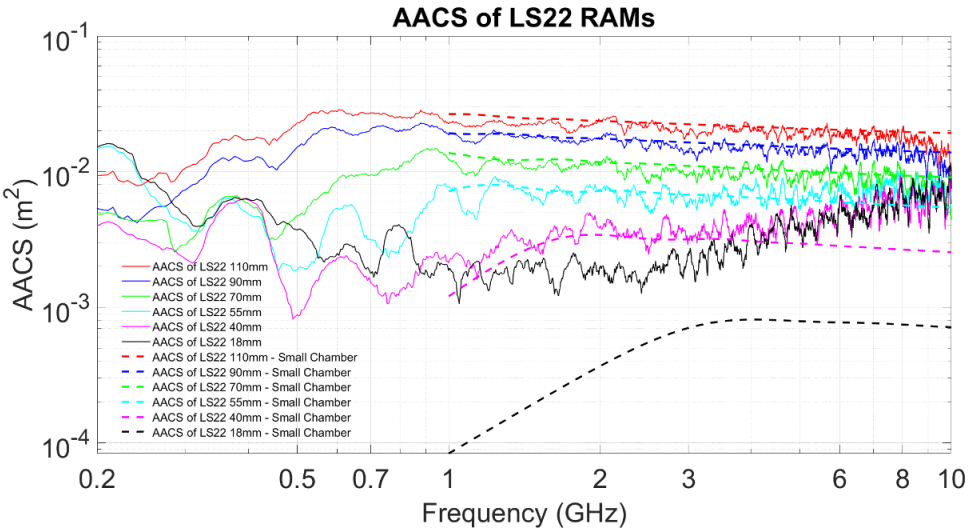

Figure 188: Shows the AACS of LS22 RAMs with different dimensions measured in a big Reverberation Chamber (section 3.2.2) and compared with previous results [75] *measured in a small reverberation chamber with dimension of 0.8m x 0.7m x 0.6m.*

9.6.2 AACS of the PCB tracks and Package Pins of the IC

In this section, we employ measurement setup 2 described in Section 9.3.2 to measure the AACS at the package pin end connected via test RF PCB tracks and the AACS of the terminated end also connected via the same respective test RF PCB tracks. From these measurement results, we can deduce the AACS of the 60mm test RF PCB track. As confirmed in Section 9.1.6, the results indicate that the dominant power coupling is from

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the PCB tracks, making the coupling due to RF IC package pins and the IC itself (including package, lead frame, bond wires and internal chip) negligible. Therefore, we focus only on the AACS of the test RF PCB tracks and ignore the AACS of the package pins and the IC itself.

Figure 189: Shows the pictures taken during the measurement of coupled power at the terminating ends of the test PCB tracks on the RF IC detector test bench.

The absorbed power at the package pin is measured by the RF IC detector, while the absorbed power at the terminating end is deduced from the measured coupled power from the power meter in a separate measurement. The power absorbed by one test RF PCB track on the RF IC detector test bench can be calculated as follows:

$$\langle P_a \rangle_{one\ track} = \langle P_a \rangle_{PinEnd} + \langle P_a \rangle_{TermEnd} \tag{107}$$

where, $\langle P_a \rangle_{PinEnd}$ is the average power absorbed at the package pin end and $\langle P_a \rangle_{TermEnd}$ is the average power absorbed at the terminating end.

The AACS of one test RF PCB track is:

$$\langle \sigma^a \rangle_{one\ track} = \frac{\langle P_a \rangle_{one\ track}}{S_0} \tag{108}$$

The absorbed power at the terminating end can be challenging to measure with the lid closed. To address this, we can calculate the power that can be absorbed at the terminating end using the power factor between absorbed power at the package pin when the lid is open and closed in the enclosure:

$$\langle P_a \rangle_{term\ end\ lid\ closed} = \frac{\langle P_a \rangle_{pin\ end\ lid\ close}}{\langle P_a \rangle_{pin\ end\ lid\ open}} \cdot \langle P_a \rangle_{term\ end\ lid\ open} \tag{109}$$

Figure 190 shows the coupled forward power at the C1SC0 package pin with and without the shielding enclosure. The spikes observed in the red curve are due to a lack of field uniformity inside the enclosure.

The average absorbed power at the terminating end and package pin end, calculated using equations (107) and (109), is plotted in Figure 191. The power absorbed at the terminated ends is notably larger than the power absorbed at the package pin ends. To ensure the accuracy and consistency of the absorbed power at the terminating end,

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measurements at the terminating ends of C1SC0 and C1SC1 are carried out, and the results align with each other.

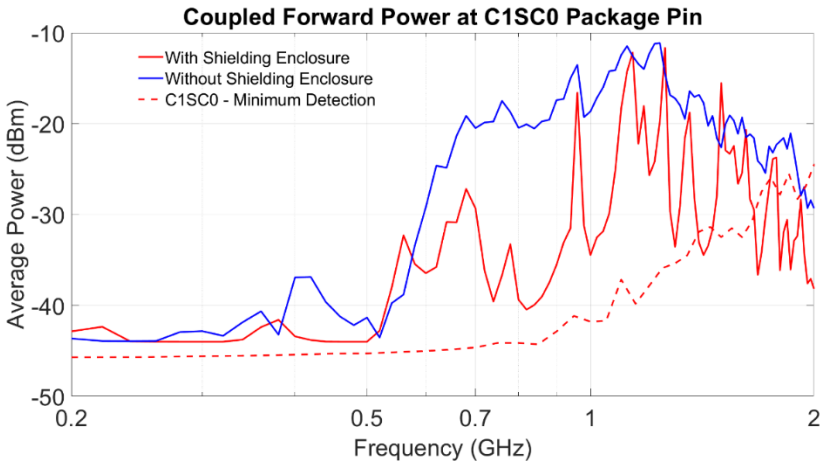

Figure 190: Shows the coupled forward power at the C1SC0 package pin with the shielding enclosure and without the shielding enclosure.

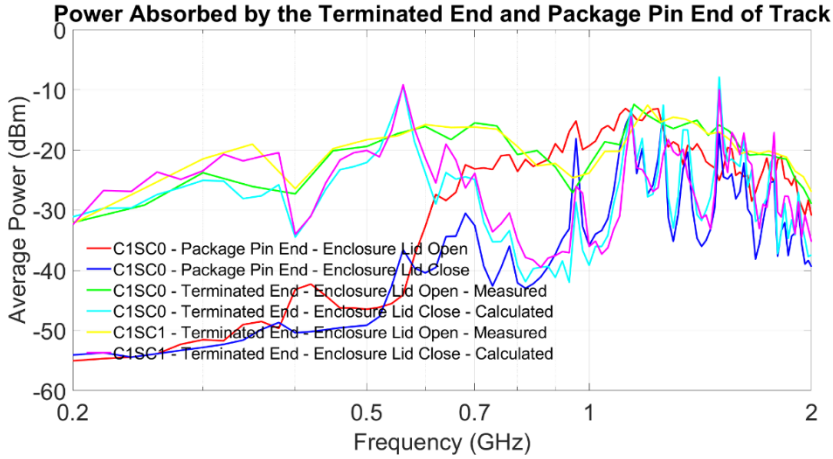

Figure 191: Shows the average absorbed power at the package pin end and terminating end when the lid of the enclosure is open and closed.

The absorbed power at the package pins of all sub-channels exhibits a close alignment, as shown in Figure 172. Additionally, as previously discussed, the absorbed power at the terminating ends of sub-channels demonstrates consistency. Consequently, the AACS of all 60mm test RF PCB tracks will be approximately the same. With this assumption of similar AACS for all test RF PCB tracks, we can deduce the AACS of the ten test RF PCB tracks inside the enclosure when the lid is closed using the following calculation:

$$\langle \sigma^a \rangle_{10\ track} = 10 * \langle \sigma^a \rangle_{one\ track} \qquad (110)$$

The calculated AACS of the ten test RF PCB tracks, determined from equation (110), is shown in Figure 193.

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9.6.3 AACS of Test Bench

In this section, we conduct measurements to determine the AACS of the entire RF IC detector test bench. This encompasses the AACS of the test PCB RF tracks, AACS of the PCB dielectric, AACS of the IC, and AACS of the test bench shielding. These measurements are carried out using the setup described in Section 9.3.1. Figure 192 provides a visual representation of the measurement setup.

Figure 192: Shows the picture of the RF IC detector test bench inside the Reverberation Chamber.

The AACS of the RF IC detector test bench can be calculated using equations (32) and (33), as shown below:

$$\langle \sigma^a \rangle_{test\ bench} = \frac{\lambda^2}{8\pi}\left(\frac{1}{G_{with}} - \frac{1}{G_{without}}\right)$$
$$\langle \sigma_a \rangle_{test\ bench} = \langle \sigma_a \rangle_{10\ tracks} + \langle \sigma_a \rangle_{PCB\ Dielectctic} + \langle \sigma_a \rangle_{testbench\ shield} + \langle \sigma_a \rangle_{IC\ pins} \quad (111)$$

As discussed earlier in Section 9.2 and confirmed in Section 9.1.6, the power absorbed by the PCB tracks is dominant compared to the power absorbed by the package pins including the package, lead frame, bond wires and internal chip ($\langle \sigma^a \rangle_{track} \gg \langle \sigma^a \rangle_{IC\ pin}$). This is evident from the results obtained with and without shielding on the RF IC detector on the PCB.

$$\langle \sigma_a \rangle_{test\ bench} \approx \langle \sigma_a \rangle_{10\ tracks} + \langle \sigma_a \rangle_{PCB\ Dielectctic} + \langle \sigma_a \rangle_{testbench\ shield} \quad (112)$$

Figure 193 illustrates the calculated AACS of the entire RF IC detector test bench, along with the AACS of the ten test RF PCB tracks calculated using equation (110). The figure clearly shows that the AACS of the tracks is significantly smaller in magnitude compared to the AACS of the entire test bench. The wiggles observed in the AACS of the ten tracks are likely due to variations in field uniformity inside the enclosure. Additionally, the figure presents the AACS of the remaining components of the test bench, which include the AACS of the PCB dielectric and the AACS of the test bench control shielding. These values are determined by subtracting the AACS of the ten test RF PCB tracks from the overall AACS of the test bench, as per equation (112).

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$$\langle\sigma_a\rangle_{PCB\ Dielectric} + \langle\sigma_a\rangle_{testbench\ shield} \approx \langle\sigma_a\rangle_{test\ bench} - \langle\sigma_a\rangle_{10\ tracks} \quad (113)$$

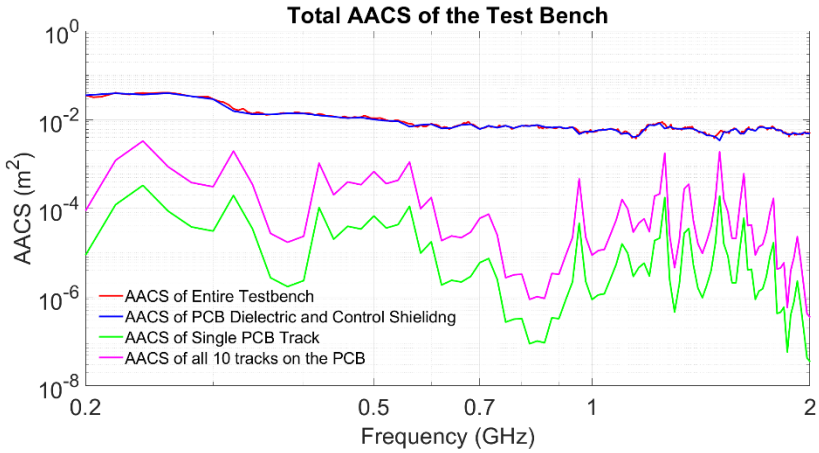

Figure 193: Shows the AACS of the RF IC detector test bench, AACS of ten test RF PCB tracks, and AACS of the remaining components in the test bench.

9.6.4 AACS of the Enclosure Wall

In this section, we will determine the AACS of the inner wall of the enclosure. Figure 194 provides a picture of the shielding enclosure inside the Reverberation Chamber. To determine the AACS of the entire shielding enclosure, including both inner and outer walls, measurements are conducted using the setup described in Section 9.3.1. After obtaining the overall AACS of the shielding enclosure, the AACS of the inner walls is separated. The AACS of both the outer and inner walls of the entire shielding enclosure is given by the following:

$$\langle\sigma^a\rangle_{inner+outer\ wall} = \frac{\lambda^2}{8\pi}\left(\frac{1}{G_{lid\ open}} - \frac{1}{G_{empty\ chamber}}\right) \quad (114)$$

Since the surface area of the outer wall of the enclosure is nearly the same as that of the inner wall, the AACS of the inner wall can be calculated by dividing the total AACS by two, as demonstrated below:

$$\langle\sigma^a\rangle_{inner\ wall} \approx \frac{\langle\sigma^a\rangle_{inner+outer\ wall}}{2} \quad (115)$$

To theoretically calculate the wall losses, we can use the equation from reference [76], as shown below:

$$\langle\sigma^a\rangle_{inner\ wall\ theo} = \frac{4A}{3c_0}\sqrt{\frac{\pi f \mu_r}{\mu_0 \sigma_{cond}}}\left[1 + \frac{3\lambda A}{32V}\right] \quad (116)$$

where, A is the surface area of the inner wall, c_0 is the speed of light, f is frequency, μ_r (1000 [77]) is the relative permeability of the wall material (sheet steel: low carbon steel),

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μ_0 is the free space permeability, σ_{cond} $(4.545 * 10^6$ [78]) is the electrical conductivity of the material, λ is wavelength and V is the volume of the enclosure.

Figure 194: Shows the pictures of the shielding enclosure inside the Reverberation Chamber.

By using the theoretical equation and adjusting the surface area as needed, one can determine both the theoretical AACS of the entire enclosure and the theoretical AACS of the inner walls. As presented in Figure 195, the measurement results and theoretical results closely match each other above 500 MHz. However, below this frequency, the theoretical results tend to underestimate the AACS of the walls.

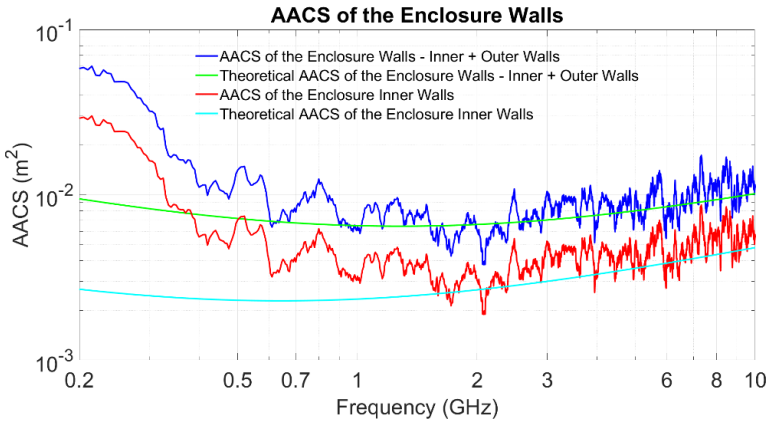

Figure 195: Shows the AACS of the entire shielding enclosure and the AACS of the inner walls of the enclosure.

9.6.5 AACS of the Monopole Antenna

Figure 196: Shows the picture of the monopole antenna mounted on the top closing lid of the shielding enclosure.

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In this section, we will calculate the AACS of the monopole antenna used to monitor the internal E-field, as described in Section 9.3.3. Figure 196 shows pictures of the monopole antenna mounted on the top closing lid of the shielding enclosure.

The AACS of the monopole antenna can be calculated by extracting the average antenna reflection coefficient using the measurement setup described in Section 9.3.1. In this case, we connect port 2 of the VNA to the monopole receiving antenna, rather than the blade receiving antenna inside the reverberation chamber.

The AACS of the monopole antenna can be calculated using the equation from reference [76] provided below:

$$\langle \sigma^a \rangle_{antenna} = \frac{\lambda^2}{8\pi}(1 - |\langle S_{22} \rangle|^2) \tag{117}$$

here, $\langle S_{22} \rangle$ represents the average reflection voltage coefficient of the receiving monopole antenna. The maximum AACS of the monopole antenna is $\lambda^2/8\pi$, which is also plotted in Figure 197. The AACS of the monopole antenna experiences some wiggles, likely due to antenna inefficiency below 500 MHz and non-uniformity in the field inside the enclosure. Past 1 GHz, the curve stabilizes, attributed to a well-stirred field in the reverberation chamber, which results in more consistent measurements.

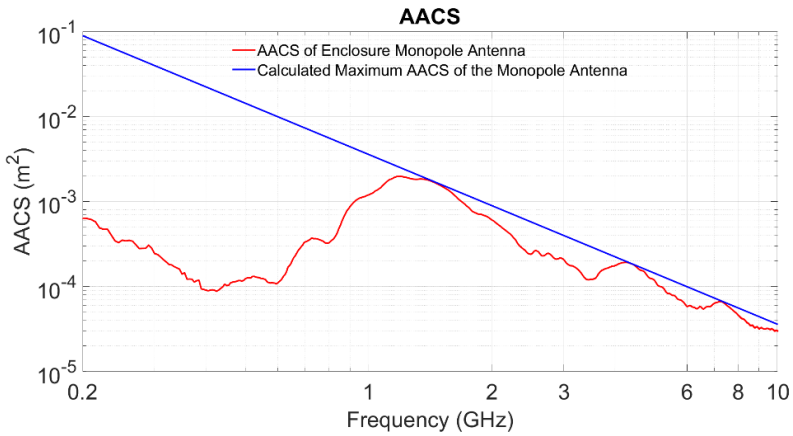

Figure 197: Shows the AACS of the monopole antenna.

9.7 Total AACS and ATCS

Now that we have presented all the AACS values for the enclosure's contents, along with the SE of the enclosure, we have obtained the essential measurement data required to comprehend the power flow analysis discussed in Section 9.2 and visualized in Figure 176. To complete the development of the enhanced PWB method in this section, we need to determine the ATCS considering the total AACS values of the enclosure's contents and the SE of the enclosure.

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With the AACS values for each content of the enclosure, which is illustrated in Figure 176, we can calculate the total AACS of the inner components, which is given by:

$$\langle \sigma_a \rangle_{tot} = \langle \sigma_a \rangle_{test\ bench} + \langle \sigma_a \rangle_{antenna} + \langle \sigma_a \rangle_{inner\ wall} \tag{118}$$

Now, let us determine the ATCS of the enclosure due to the gap created by the rubber gasket between the lid and the enclosure. The ATCS can be calculated using the following equation:

$$\langle \sigma^t \rangle = \frac{\langle \sigma_a \rangle_{tot}}{SE - 1} \tag{119}$$

Figure 198 illustrates the ATCS of the enclosure, the total AACS of all internal components of the enclosure, and all other AACS values of its internal contents. However, due to the inefficiency of the monopole antenna below 500MHz (Sections 9.4 and 9.5), the ATCS observed below this frequency may not be fully accurate.

By having the knowledge of SE, ATCS and AACS of the contents of the enclosure, the enhanced PWB method enables us to determine the internal enclosure field for a given external field.

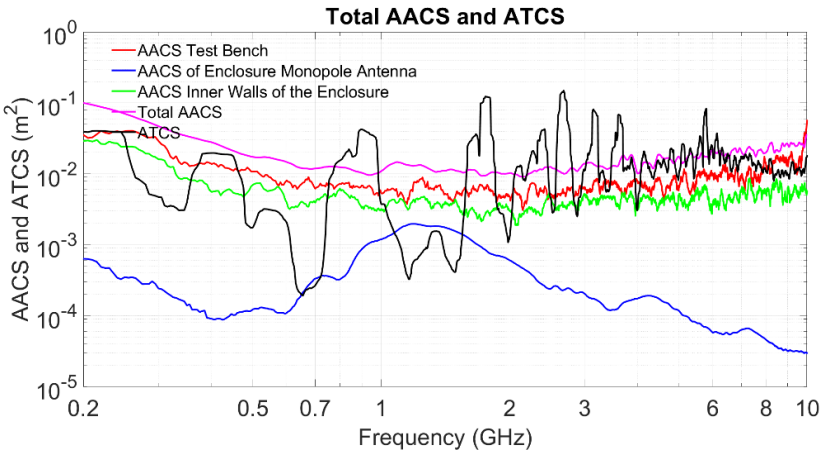

Figure 198: Shows the total AACS and ATCS of the shielding enclosure with all other AACS of the internal components.

The enhanced PWB method presented in this chapter incorporates comprehensive information about the AACS related to the IC at package pins and interconnected PCB tracks. It encompasses the AACS values of other critical internal components within the enclosure. This comprehensive analysis of AACS, which includes crucial components such as PCB tracks and ICs on the DUT, enhances the traditional PWB methods and leads to an enhanced PWB method.

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10. Conclusions and Future Work

10.1 Summary

The initial research on energy coupling into PCB traces and IC packages was discussed in Chapter 4. To validate stochastic EM coupling into PCB traces, an RF IC detector capable of measuring coupled power at the package pin via test PCB tracks was designed and presented in Chapter 5 and Chapter 6. Chapter 7 presented the testing of the RF IC detector through conducted measurements. In this chapter, we also investigated realistic impedance at the package pins and cross-coupling between adjacent PCB tracks and IC package pins in a conducted environment. The calibration method for the RF IC detector was presented in Chapter 7, offering insights into its performance and coupling range for accurate radiated measurements. This information laid the groundwork for radiated measurements in Chapters 8 and 9. Chapter 8 introduced an analytical methodology to predict the susceptibility of ICs to EMI, applicable to other PCB components as well. Further, we also validated the stochastic EM coupling into lossy PCB traces and IC package pins using a purpose-built RF IC detector. Finally, Chapter 9 presented the enhanced PWB method capable of incorporating comprehensive AACS information related to the IC at package pins and interconnected PCB tracks, along with all other AACS values of critical internal components within the enclosure.

10.2 Conclusion

This research has updated the numerical model from [7] and introduced an analytical methodology for predicting the susceptibility of ICs to EMI. Importantly, this method can be applied to various electronic components on a PCB, provided that the necessary information is available. This methodology offers valuable insights and predictive capabilities that contribute to the broader field of EMC. Additionally, the RF IC detector was developed, enabling the measurement of coupled power at the package pin via test RF PCB tracks. This detector was used to validate the updated version of the previously developed numerical model [7], which is designed to estimate stochastic EM coupling into PCB traces. Furthermore, the RF IC detector facilitated the creation of an enhanced PWB method that incorporates detailed information regarding the AACS at the package pin (including package, lead frame, bond wires and internal chip) of the IC and its interconnected RF PCB tracks. This comprehensive approach extends to encompass all other relevant AACS values associated with internal components within the enclosures. This advancement in the PWB method fosters the development of improved shielding and power balance techniques.

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The proposed methodology for estimating the probability of susceptibility of ICs in this work holds significant value for the EMC community, providing a more accurate estimation of the probability of susceptibility of ICs. Additionally, the proposed methodology of the enhanced PWB method will contribute to the development of improved shielding and power balance techniques, allowing for the assessment of the effectiveness of different components. Overall, this research enhances EMI understanding, aiding design and mitigation in high-frequency electronics. It improves susceptibility predictions, fostering resilient electronic systems. These advancements lead to more reliable electronics in our EMI-prone world.

10.3 Future Work

Despite achieving the stated objectives successfully, there remains significant potential for further research utilizing the designed RF IC detector. In this work, we have observed minimal cross-coupling effects between PCB tracks and IC package pins. However, future work can focus on investigating package pin cross-couplings between the RF IC detector's package pins, PCB tracks, connectors, and multiple components on the PCB. Enhancing the numerical model to estimate stochastic EM coupling into PCB traces, considering cross-couplings, and studying closely spaced PCB tracks and their AACS are potential areas for future exploration. Moreover, the design of a type 2 radiated board with extended tracks (Section 6.6.2) provides an avenue to delve deeper into EM field coupling and cross-coupling between PCB tracks. Lastly, refining the analytical methodology for predicting the susceptibility probability in PCBs with multiple components presents an opportunity for further development.

The RF IC detector used in this work was fabricated with two types of packaging, CQFP64 and CQFN64. While this study primarily explored the CQFP64 packaging RF IC detector, further research with the RF IC detector is promising. Investigating package pin cross-couplings of CQFN64 and CQP64 and developing accurate models for IC package pin interactions would be valuable areas of exploration. This research offers a solid foundation for these future endeavours and holds the potential to contribute to the field of EMC.

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11. Appendix

11.1 Radiated Measurement in GTEM Environment

In this section, we provide a brief overview of the measurements conducted in a GTEM cell during the secondment of ESR9 at ESEO.

Our primary objective is to formulate a model for understanding radiated coupling into the package pins of the RF IC detector via RF PCB tracks. To achieve this, we primarily conduct radiated measurements in a reverberant environment. However, to gain insights into the behaviour of radiated coupling into the PCB tracks of the RF IC detector in a GTEM environment, we conducted some initial measurements at ESEO. Figure 199 depicts the measurement setup and includes images taken during the measurement process.

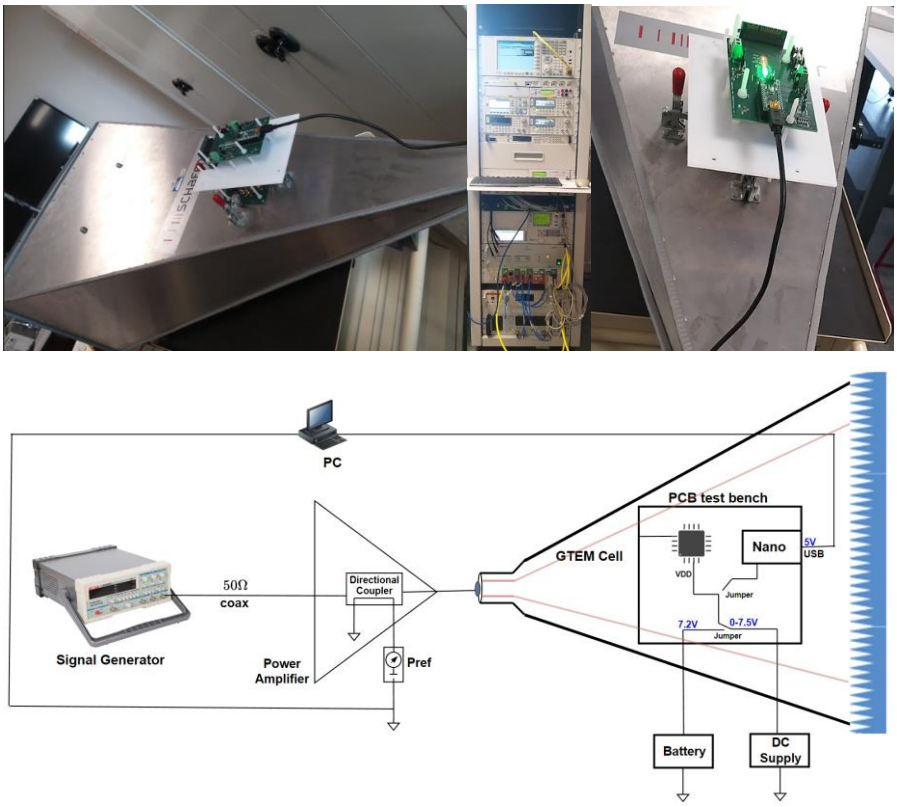

Figure 199: Shows the measurement setup and pictures during the GTEM cell radiated measurements.

It is important to note that the results obtained from these initial GTEM measurements may not be directly applicable to the work presented in this thesis. This is due to several factors, including time constraints and limited equipment availability, which resulted in an insufficient number of measurements to fully analyse and comprehend the behaviour in the GTEM environment. Therefore, the results from these GTEM measurements are not included in this work. However, we recommend that for future research, radiated

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measurements for the RF IC detector in a GTEM cell be considered to gain a more comprehensive understanding of its behaviour in this specific environment.

11.2 Measurement Setup to Generate High E-field

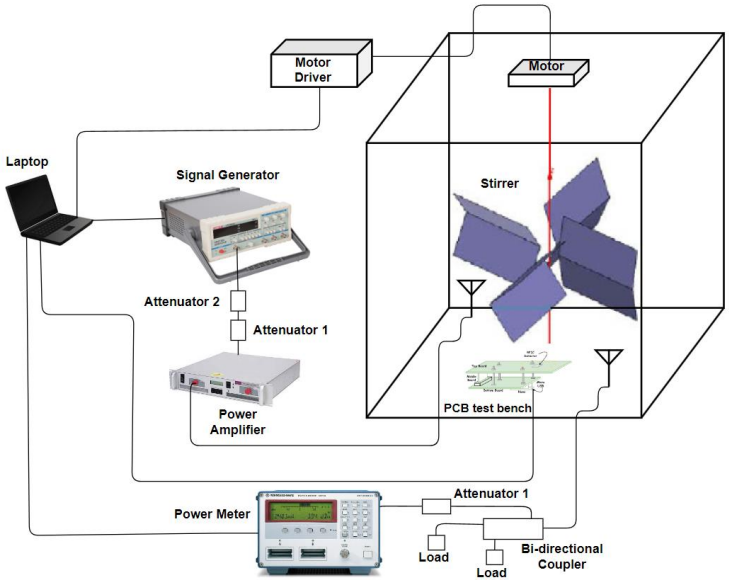

Figure 200: Measurement setup to generate a high E-field inside a reverberation chamber.

To enhance the E-field within the Reverberation Chamber, the setup shown in Figure 200 is employed. In this configuration, a power amplifier positioned between the signal generator and the reverberation chamber is used to increase the input power up to 40 dBm. In both the measurement setups, as shown in Figure 151 and Figure 200, the chamber's field is monitored by measuring the received power from the second receiving antenna using a power meter. The PCB test bench is powered by either a battery or a micro USB connection and is linked to a laptop through a micro USB port facilitated by an Arduino Nano. Additionally, the operation of the stirrer inside the reverberation chamber is controlled by the laptop, as depicted in the figure.

11.3 Calibration Accuracy of Conducted Board Test Bench

11.3.1 After TOSM Calibration

To verify the accuracy of the calibration, the calibration standards were measured after TOSM calibration. The calibration standards consist of through, open, short, and match standards. The measurement results are presented in the form of Smith charts and S-parameter plots, as shown in the figures below.

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In the context of calibration, Smith charts help in assessing the correctness of the calibration standards by comparing the measured data to the expected values. The ideal calibration standards, such as the through (which represents a direct connection with no impedance change), the open (which represents an infinite impedance), the short (which represents zero impedance), and the match (which represents a perfect impedance match), should appear as specific points at different frequencies on the Smith chart.

By assessing the Smith charts and S-parameter plots of the calibration standards, one can evaluate the calibration accuracy and identify any discrepancies. The verification of calibration accuracy is essential as it ensures the reliability and validity of subsequent measurements made with the calibrated VNA.

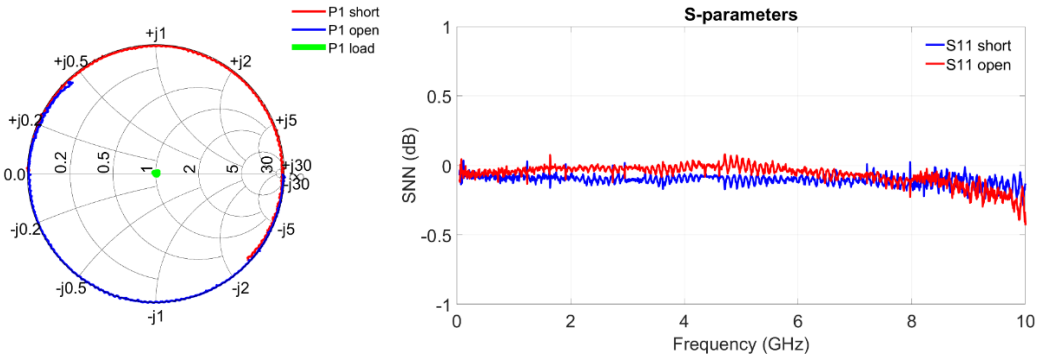

Figure 201: The left figure shows the Smith chart of short, open and load calibration standards and the right figure shows the S-parameters of short and open calibration standards.

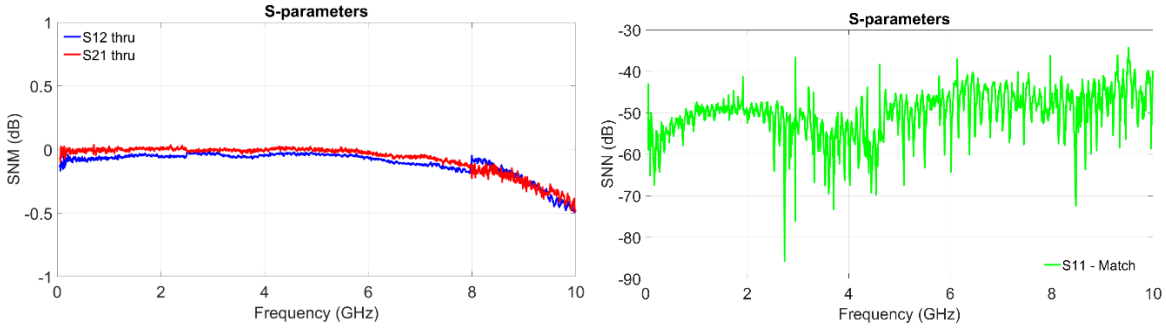

Figure 202: The left figure shows the S-parameters of the through calibration standard and the right figure shows the S-parameters of match calibration standard.

11.3.2 Before and After TRL/M Calibration

To verify the accuracy of the calibration, the calibration standards of the specifically designed conducted calibration board (Section 6.5.2) were measured after TRL/M calibration. The detailed information on the calibration board and the standards used in it are provided in Section 6.5.2. The measurement results are presented in the form of Smith charts and S-parameter plots, as shown in the figures below.

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11.3.2.1 Results of Calibration Board before TRL/M calibration

In the following figures, we will present the results before TRL/M calibration, which involves measuring the S-parameters of the calibration board standards after TOSM calibration.

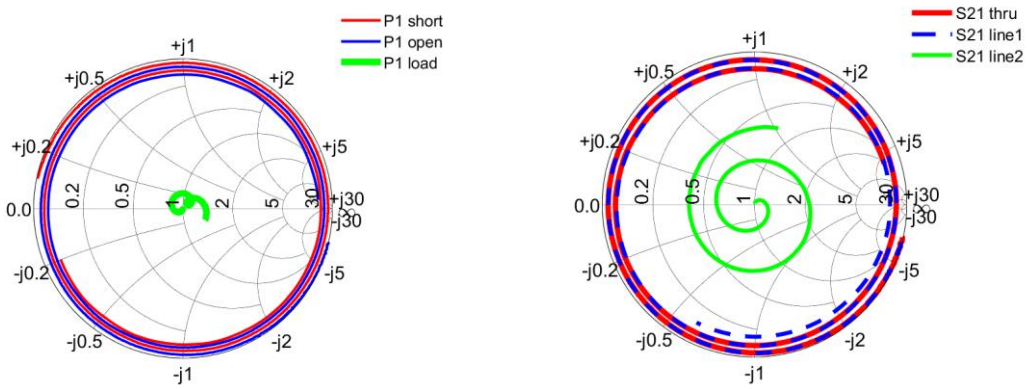

Figure 203: The left figure shows the Smith chart of short, open and load calibration standards of the TRL/M calibration board and the right figure shows the Smith chart of through, line 1 and line 2 calibration standards of the TRL/M calibration board.

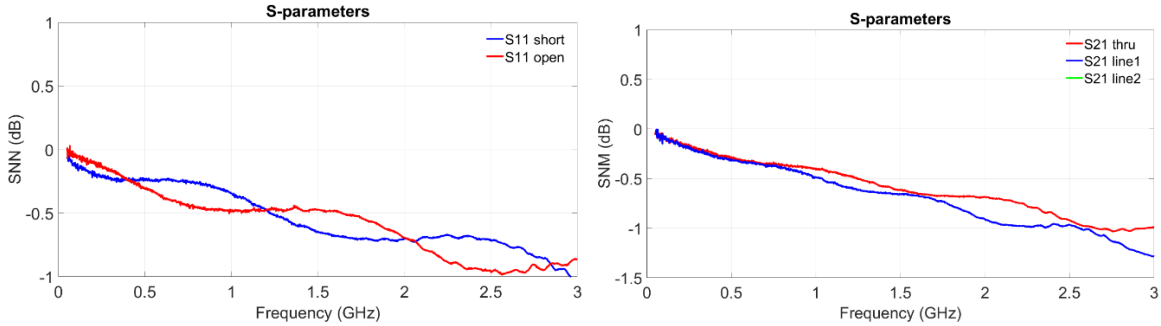

Figure 204: The left figure shows the S-parameters of short and open calibration standards of the TRL/M calibration board and the right figure shows the S-parameters of through, line 1 and line 2 calibration standards of the TRL/M calibration board.

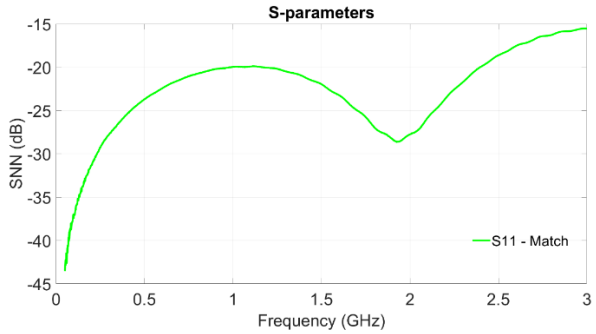

Figure 205: Shows the S-parameters of a match calibration standard of the TRL/M calibration board.

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11.3.2.2 Results of Calibration Board after TRL/M calibration

The results shown below, in the form of Smith charts and S-parameters of the TRL/M standards of the conducted calibration board, were measured after TRL/M calibration. By comparing the results with the results demonstrated in Section 11.3.2.1, it is clear that the influence of the RF PCB tracks used as standards in the conducted calibration board has been successfully removed. The results are illustrated in figures given below.

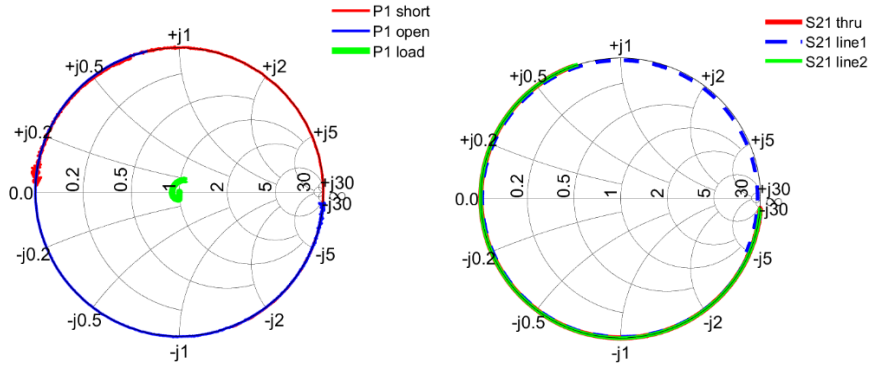

Figure 206: The left figure shows the Smith chart of short, open and load calibration standards of the calibration board after TRL/M calibration and the right figure shows the Smith chart of through, line 1 and line 2 calibration standards of the calibration board after TRL/M calibration.

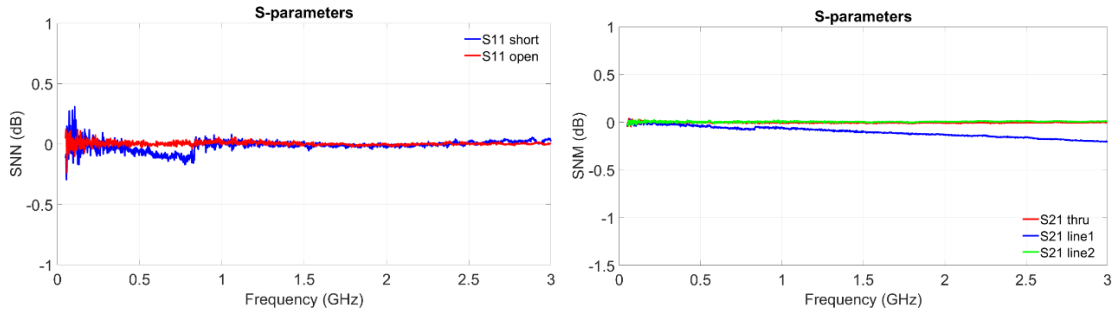

Figure 207: The left figure shows the S-parameters of short and open calibration standards of the calibration board after TRL/M calibration and the right figure shows the S-parameters of through, line 1 and line 2 calibration standards of the calibration board after TRL/M calibration.

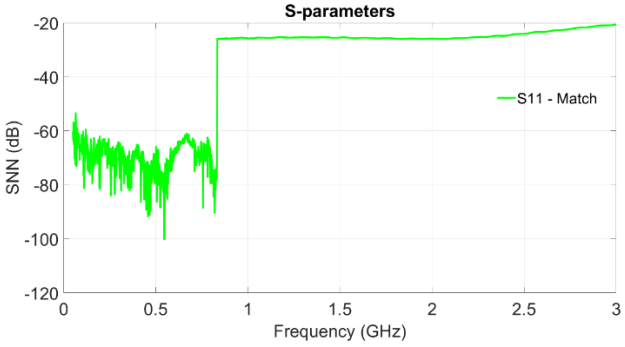

Figure 208: Shows the S-parameters of a match calibration standard of the calibration board after TRL/M calibration.

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11.4 Radiated Calibration Board results after TRL/M Calibration

The calibration accuracy of the radiated calibration board is not as expected because of the resistors on RF PCB tracks, this section will show the discrepancies in the results after TRL/M calibration.

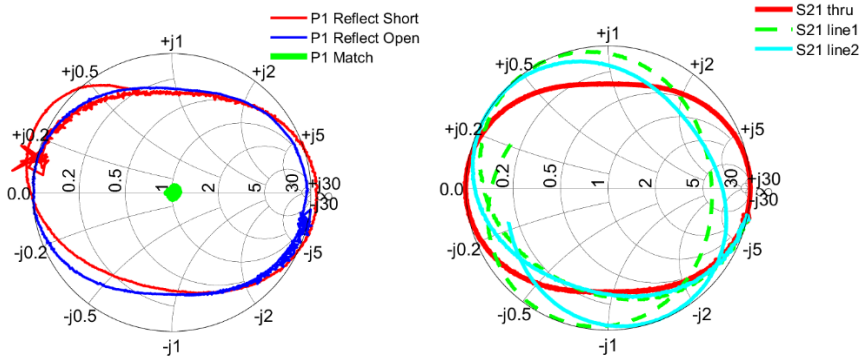

Figure 209: The left figure shows the Smith chart of short, open and load calibration standards of the Radiated calibration board after TRL/M calibration and the right figure shows the Smith chart of through, line 1 and line 2 calibration standards of the Radiated calibration board after TRL/M calibration.

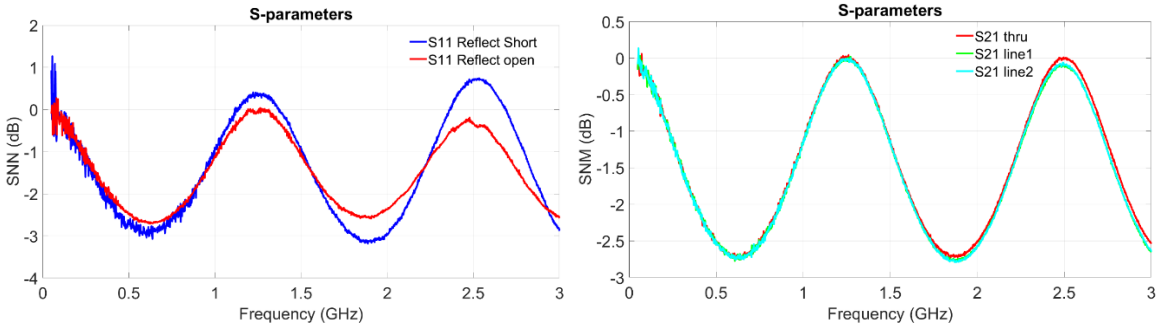

Figure 210: The left figure shows the S-parameters of short and open calibration standards of the Radiated calibration board after TRL/M calibration and the right figure shows the S-parameters of through, line 1 and line 2 calibration standards of the Radiated calibration board after TRL/M calibration.

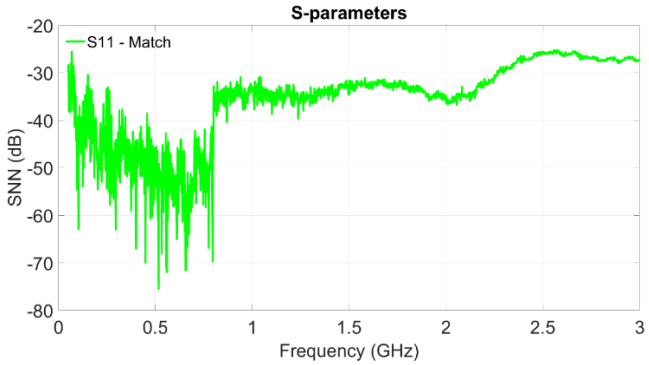

Figure 211: Shows the S-parameters of a match calibration standard of the Radiated calibration board after TRL/M calibration.

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11.5 GTEM Calibration Board results after TRL/M Calibration

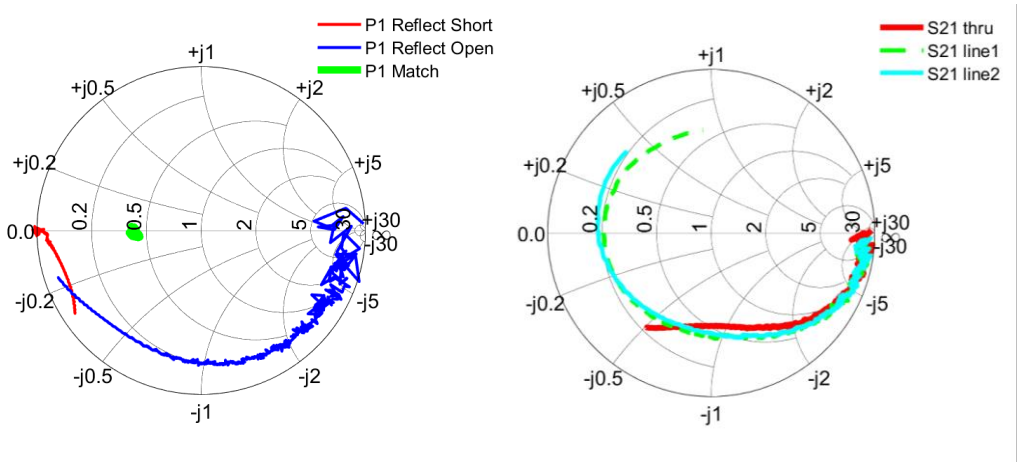

Figure 212: The left figure shows the Smith chart of short, open and load calibration standards of the GTEM calibration board after TRL/M calibration and the right figure shows the Smith chart of through, line 1 and line 2 calibration standards of the GTEM calibration board after TRL/M calibration.

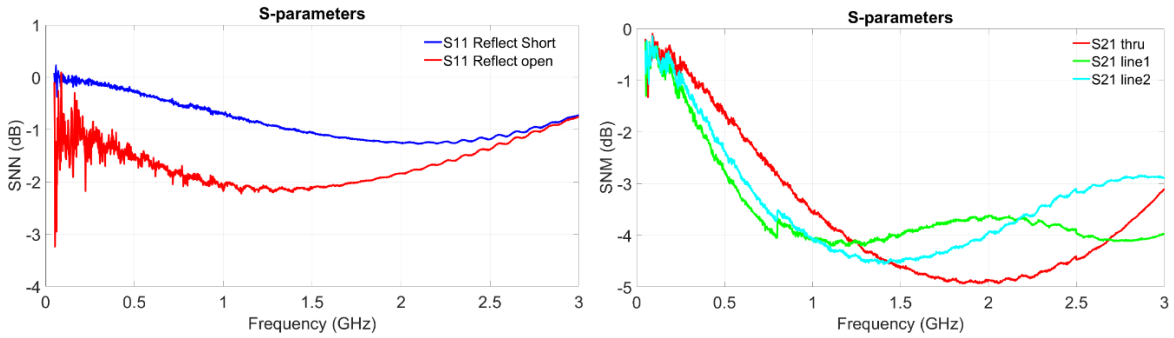

Figure 213: The left figure shows the S-parameters of short and open calibration standards of the GTEM calibration board after TRL/M calibration and the right figure shows the S-parameters of through, line 1 and line 2 calibration standards of the GTEM calibration board after TRL/M calibration.

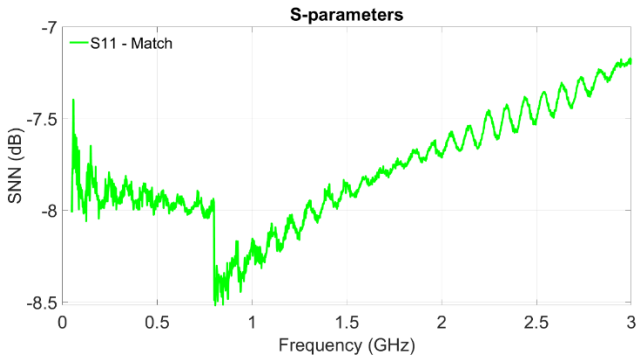

Figure 214: Shows the S-parameters of a match calibration standard of the GTEM calibration board after TRL/M calibration.

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11.6 Verification of De-embedding Methodology

In this section, we verify and validate the de-embedding methodology presented in Section 7.3.2. In the conducted board test bench, we have a trace length of 36mm between the RF IC detector and MCX connector. However, since this trace does not exactly resemble the trace in the calibration board as it is in the case for the radiated board and GTEM board, we use a different procedure to find the T matrix until a certain point, after which the procedure remains the same as presented in Section 7.3.2.

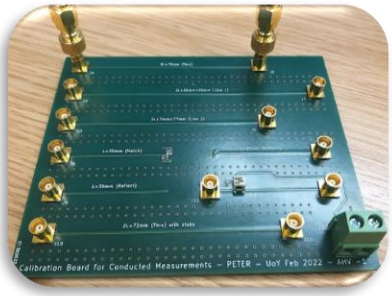

Figure 215: Shows the Calibration Board of Conducted Board.

Let us determine the T-parameters for the 36mm trace by utilizing the existing traces in the conducted calibration board. In the board, we have traces with different lengths for which we can measure the 2-port S-parameters.

- Trace 1 (thru) = 70mm,
- Trace 2 (line1) = 90mm,
- Trace 3 (line2) = 77mm

By using the measured S-parameters of these traces, we can obtain the T-parameters of a 20mm trace and eliminate the effect of MCX connectors at the end. Similarly, we can find the T-parameters of a 37mm trace from the T-parameters of the 20mm and 7mm traces.

$$[T_{20mm}] = [T_{90mm}][T_{70mm}]^{-1}$$
$$[T_{7mm}] = [T_{77mm}][T_{70mm}]^{-1} \quad (120)$$

From equation (120) we can get the T-parameters of 37mm trace,

$$[T_{37mm}] = [T_{20mm}]\sqrt{[T_{20mm}]}[T_{7mm}] \quad (121)$$

Next, we calculate the input impedance of the RF IC detector at the port using the T-parameters of the 37mm trace by converting them into an ABCD matrix. Following the steps presented in Section 7.3.2, we substitute the obtained T matrix (equation (121)) into the ABCD matrix in equation (70). By continuing with the procedure, we ultimately determine the input impedance at the package pin.

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Figure 216 and Figure 217 display the real and imaginary parts of the calculated impedance at the package pin of sub-channel 0 of channel 1 (C1SC0) in the conducted board, obtained using TRL/M calibration, TOSM calibration, and the de-embedding method. The comparison in the figures reveals that the impedance calculated from the de-embedding method closely matches the impedance calculated after TRL/M calibration. This observation validates the accuracy and effectiveness of the de-embedding method in comparison to the TRL/M calibration.

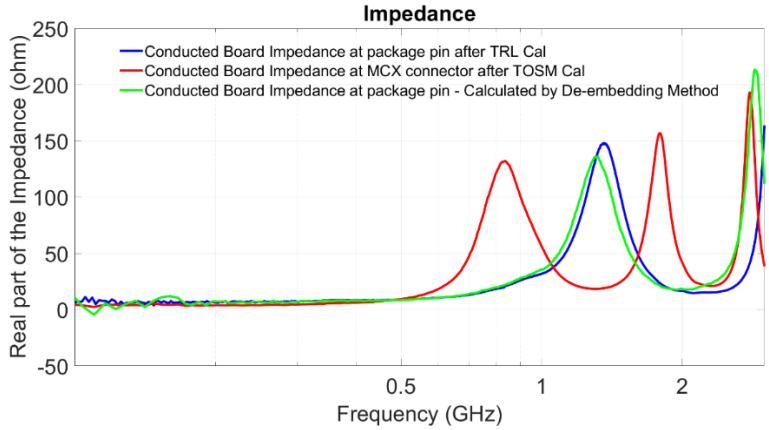

Figure 216: Shows the comparison between the real part of the impedance at the package pin of channel 1 sub-channel 0 (C1SC0) calculated after TRL/M calibration, TOSM calibration and de-embedding method in the conducted board.

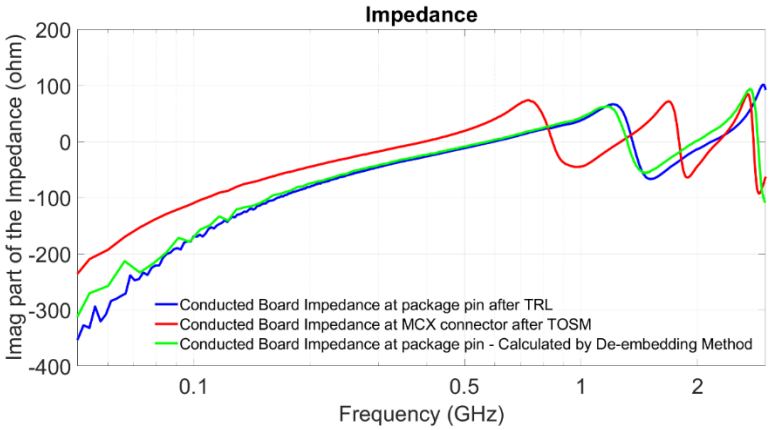

Figure 217: Shows the comparison between the imaginary part of the impedance at the package pin of channel 1 sub-channel 0 (C1SC0) calculated after TRL/M calibration, TOSM calibration and de-embedding method in the conducted board.

Figure 218 and Figure 219 depict the S-parameters converted from T-parameters, calculated using equation (120) and (121), and they are compared with the actual through trace with a length of 72mm.

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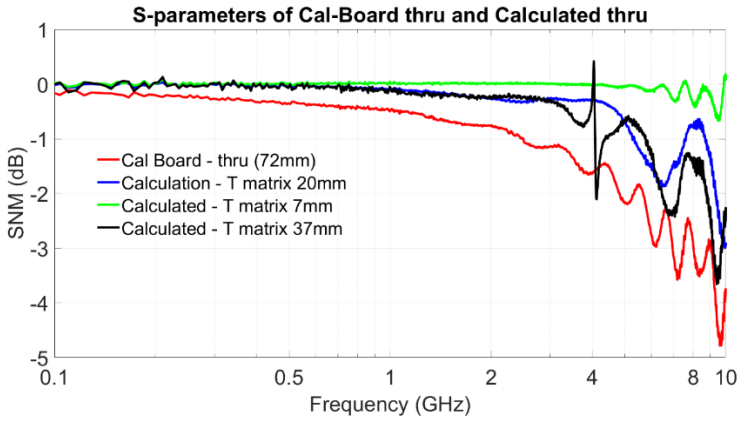

Figure 218: Shows the S-parameters (S21) of different trace lengths deduced from the de-embedding method using equations (120) and (121). The figure also compares the S-parameters with the calibration board's through which has a length of 72mm.

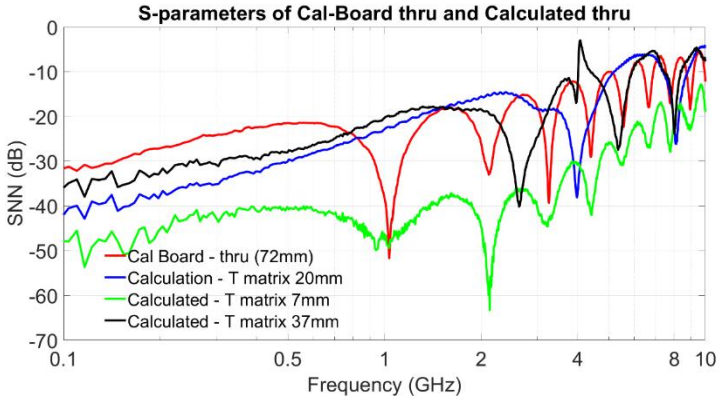

Figure 219: Shows the S-parameters (S11) of different trace lengths deduced from the de-embedding method using equations (120) and (121). The figure also compares the S-parameters with the calibration board's through which has a length of 72mm.

11.7 Influence of RF PCB tracks

11.7.1 Frequency-Dependent Permittivity

The microstrip line loss tangent is given by the following expression,

$$tan\,\delta = \frac{\varepsilon_r''}{\varepsilon_r'} \tag{122}$$

The loss tangent of the dielectric is represented by $tan\,\delta$, where ε_r' and ε_r'' are the real and imaginary parts of the relative permittivity of the dielectric. The relative permittivity ε_r of the dielectric is approximated using a one-term Debye model [62],[79].

$$\varepsilon_r(f) = \varepsilon_r'(f) - j\varepsilon_r''(f) = \varepsilon_\infty + \frac{A_1}{1 + j\omega\tau_{rel}} - j\frac{\sigma_d}{\omega\varepsilon_0} \tag{123}$$

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The angular frequency is represented by $\omega = 2\pi f$, where f is the frequency. $A_1 = \varepsilon_s - \varepsilon_\infty$ represents the amplitude of the Debye dielectric susceptibility and is calculated as the difference between the static dielectric constant ε_s and the high-frequency relative permittivity ε_∞.

$$\varepsilon_r'(f) = \varepsilon_\infty + \frac{A_1}{1 + (\omega\tau_{rel})^2}$$
$$\varepsilon_r''(f) = \frac{A_1\omega\tau_{rel}}{1 + (\omega\tau_{rel})^2} + \frac{\sigma_e}{\omega\varepsilon_0} \quad (124)$$

The effective conductivity of the dielectric is denoted by σ_e and the relaxation time constant is represented by τ_{rel}.

Using the Debye model [79], we can analytically calculate $\tau_{rel}, \varepsilon_s, \varepsilon_\infty$, and A_1 at two frequency points using the following equations. Initial values such as $\varepsilon'_{r(f_{min},f_{max})}$ and $tan\,\delta_{(f_{min},f_{max})} = {\varepsilon_r''}/{\varepsilon_r'}$ are obtained from the manufacturer's dielectric datasheet [54].

$$f_{rel_{(f_{min},f_{max})}} = \frac{1}{\tau_{rel}} = \frac{\varepsilon_r''(f_{\min}) \cdot f_{\min} - \varepsilon_r''(f_{\max}) \cdot f_{\max}}{\varepsilon_r'(f_{\max}) - \varepsilon_r'(f_{\min})} \quad (125)$$

$$\sigma_{e_{(f_{min},f_{max})}} = 2\pi f_{\min}\varepsilon_0 \left\{ \varepsilon_r''(f_{\min}) + \frac{f_{\min}f_{rel}}{{f_{\min}}^2 - {f_{\max}}^2}\left(\varepsilon_r'(f_{\min}) - \varepsilon_r'(f_{\max})\right) \cdot \left(1 + \left(\frac{f_{\max}}{f_{rel}}\right)^2\right)\right\} \quad (126)$$

$$\varepsilon_{\infty_{(f_{min},f_{max})}} = \frac{\varepsilon_r'(f_{\min}) - \varepsilon_r'(f_{\max}) + \varepsilon_r'(f_{\min}) \cdot \left({f_{\min}}/{f_{rel}}\right)^2 - \varepsilon_r'(f_{\max}) \cdot \left({f_{\max}}/{f_{rel}}\right)^2}{\left({f_{\min}}/{f_{rel}}\right)^2 - \left({f_{\max}}/{f_{rel}}\right)^2} \quad (127)$$

$$\varepsilon_{s_{(f_{min},f_{max})}} = \varepsilon_r'(f_{\min}) + (\varepsilon_r'(f_{\min}) - \varepsilon_\infty) \cdot \left({f_{\min}}/{f_{rel}}\right)^2 \quad (128)$$

The relative effective permittivity equation from [39], has been modified to incorporate frequency dependence and is expressed as follows.

$$\varepsilon_{r\_eff}(f) = \frac{\varepsilon_r'(f) + 1}{2} + \frac{\varepsilon_r'(f) - 1}{2}\left(1 + \frac{10}{{w}/{h}}\right)^{-{1}/{2}} - \frac{\varepsilon_r'(f) - 1}{4.6}\frac{{t}/{h}}{{w}/{h}} \quad (129)$$

11.7.2 Roughness Co-efficient (K_r and K_s)

The frequency-dependent per-unit-length (p.u.l.) resistance $R_{rough}(f)$, taking into account the roughness effect using the Hemispherical Method, is given by [62], [63]:

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$$R_{rough}(f) = \begin{cases} K_r R_s(f)\left(\frac{1}{w}+\frac{1}{b}\right), & \delta_s(f) < t \\ \frac{2}{\sigma t}\left(\frac{1}{w}+\frac{1}{b}\right), & \delta_s(f) \geq t \end{cases} \quad (130)$$

$$K_r = \begin{cases} 1, & K_s \leq 1 \\ K_s, & K_s > 1 \end{cases}$$

where, K_r is the coefficient for the roughness effect which is given below:

$$K_s = \frac{\left|Re\left[\eta_d \frac{3\pi}{4k_d{}^2}\left(\alpha(1)+\beta(1)\right)\right]\right| + \frac{\mu_0 \omega \delta_s}{4}\left(A_{\text{tile}} - A_{\text{base}}\right)}{\frac{\mu_0 \omega \delta_s}{4} A_{\text{tile}}} \quad (131)$$

where, $\eta_d = \sqrt{\frac{\mu_0}{\varepsilon_0 \varepsilon_r'}}$; $k_d = k_0\sqrt{\varepsilon_{r\_eff}}$, $k_0 = \frac{w}{c}$; and $\alpha(1)$ and $\beta(1)$ are given by

$$\alpha(1) = -\frac{2j}{3}(kr_e)^3\left[\frac{1-\frac{\delta_s}{r_e}(1+j)}{1+\frac{\delta_s}{2r_e}(1+j)}\right] \quad (132)$$

$$\beta(1) = -\frac{2j}{3}(kr_e)^3\left[\frac{1-\frac{4j}{k^2 r_e \delta_s}\left(\frac{1}{1-j}\right)}{1+\frac{2j}{k^2 r_e \delta_s}\left(\frac{1}{1-j}\right)}\right] \quad (133)$$

where $k = \frac{2\pi}{\lambda}$ and $\lambda = \frac{c}{\left(f\sqrt{\varepsilon_r'}\right)}$ and A_{tile} is the square tile area and A_{base} is the base area, given by:

$$A_{\text{base}} = \pi\left(\frac{b_{\text{base}}}{2}\right)^2 \quad (134)$$

$$A_{\text{tile}} = d_{\text{peaks}}^2 \quad (135)$$

where b_{base} is the tooth base width and d_{peaks} is the peak distance, r_e is the equivalent radius which is given by,

$$r_e = \sqrt[3]{h_{\text{tooth}}\left(\frac{b_{\text{base}}}{2}\right)^2} \quad (136)$$

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11.8 PCB Test Bench for RF IC Detector Schematics

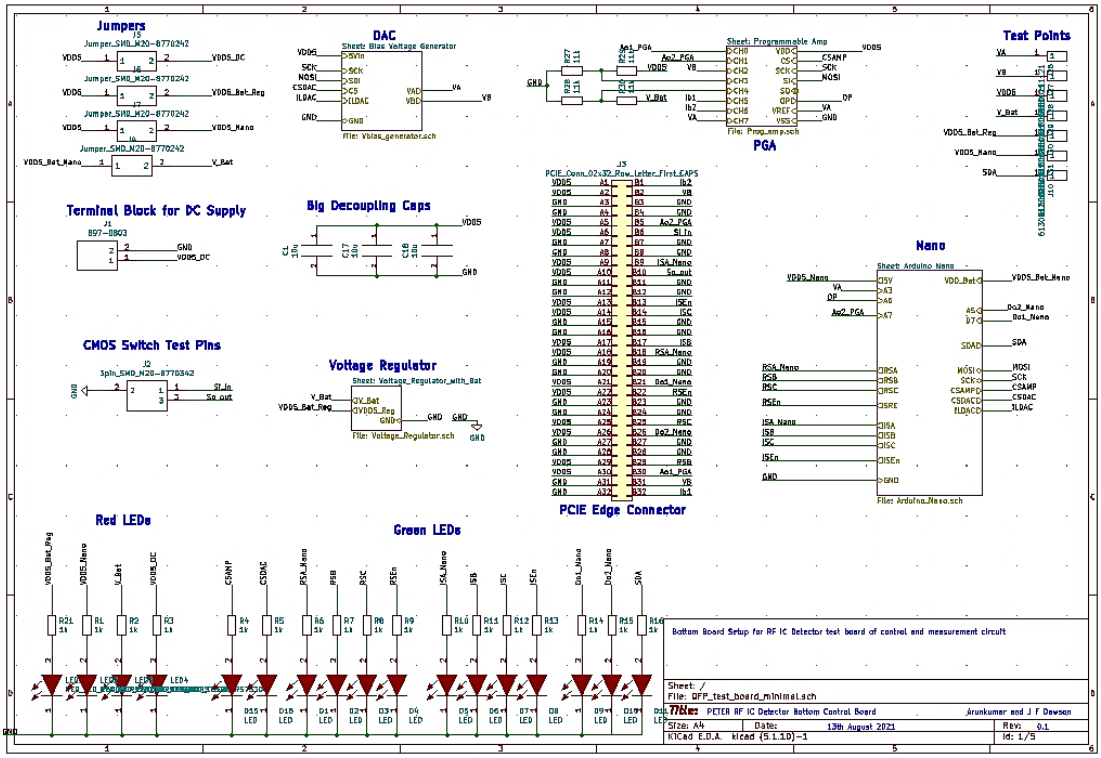

Figure 220: Shows the schematic of the Bottom Control Board from KiCAD

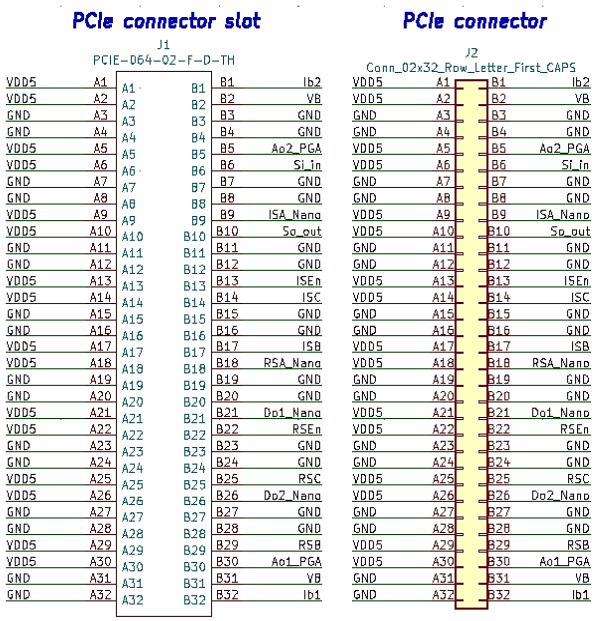

Figure 221: Shows the schematic of the middle board from KiCAD.

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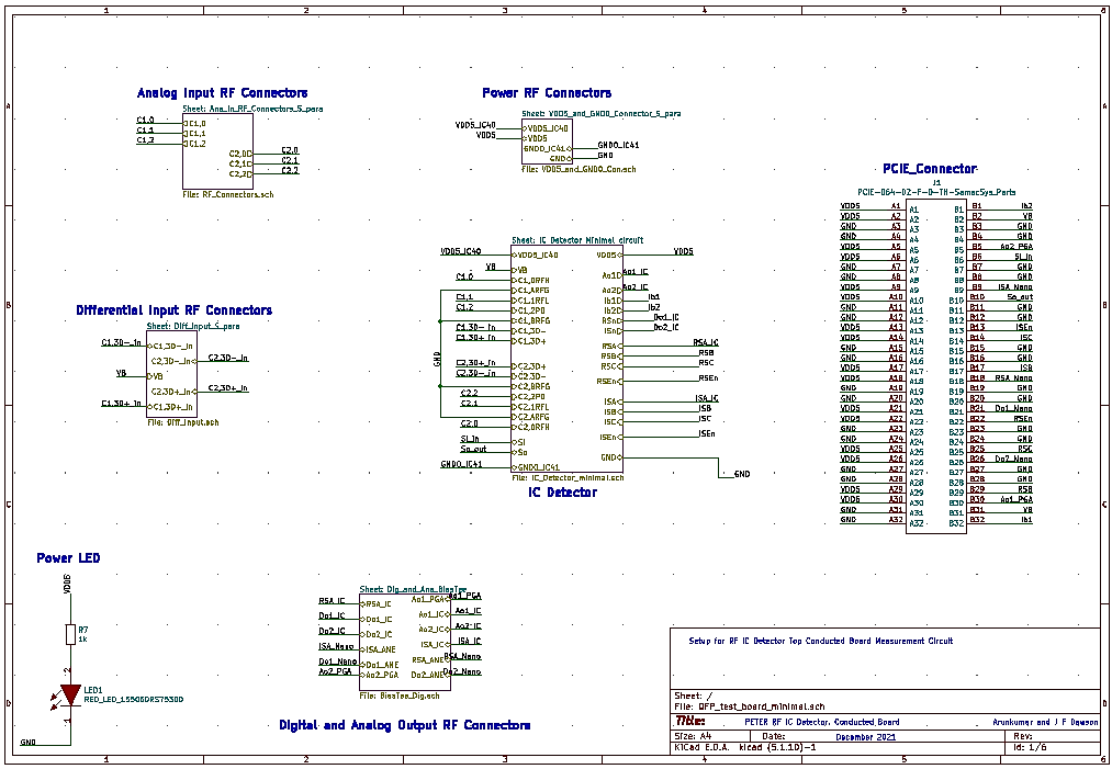

Figure 222: Shows the schematic of the Top Conducted Board from KiCAD.

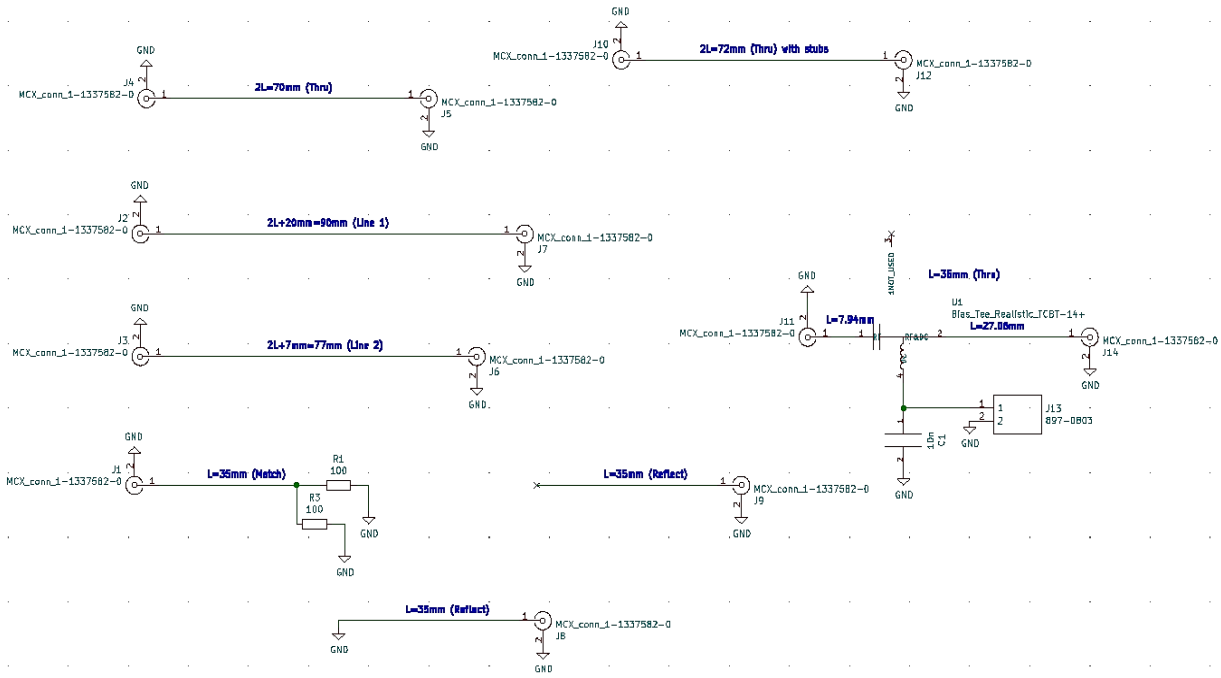

Figure 223: Shows the schematic of the TRL calibration board for the conducted board from KiCAD.

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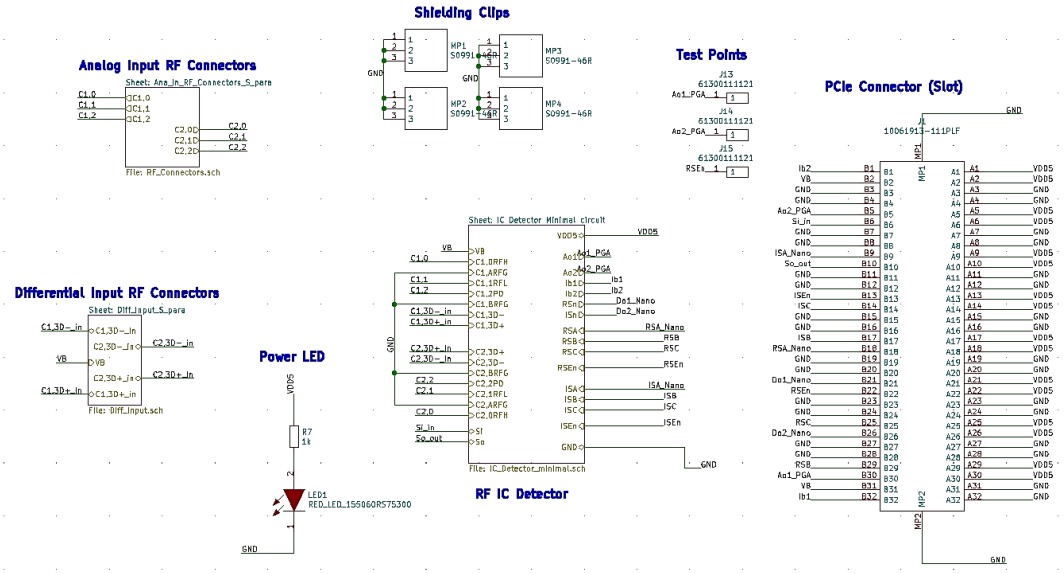

Figure 224: Shows the schematic of the Top Radiated Board type 2 from KiCAD.

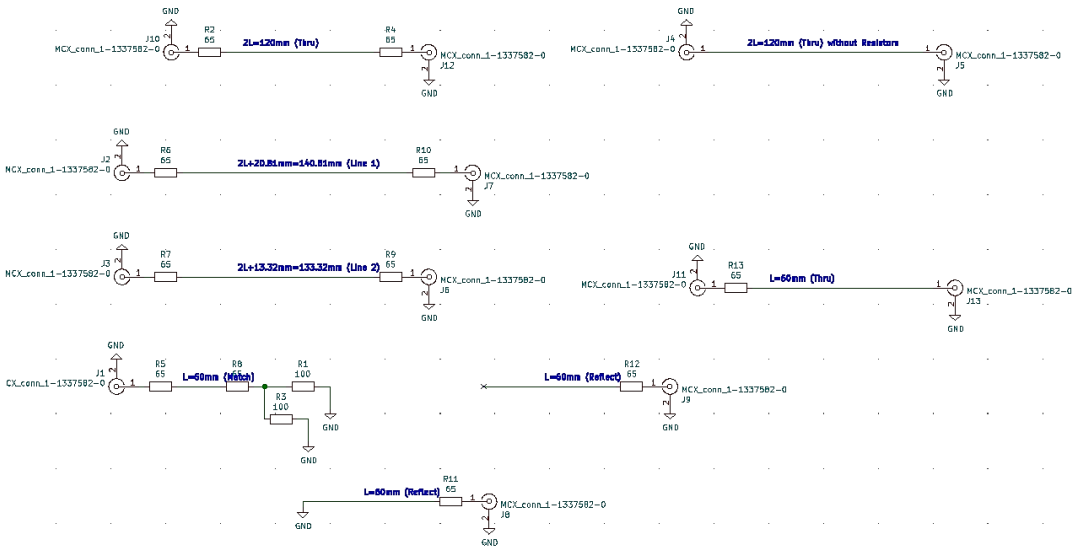

Figure 225: Shows the schematic of the TRL calibration board for radiated board type 1 from KiCAD.

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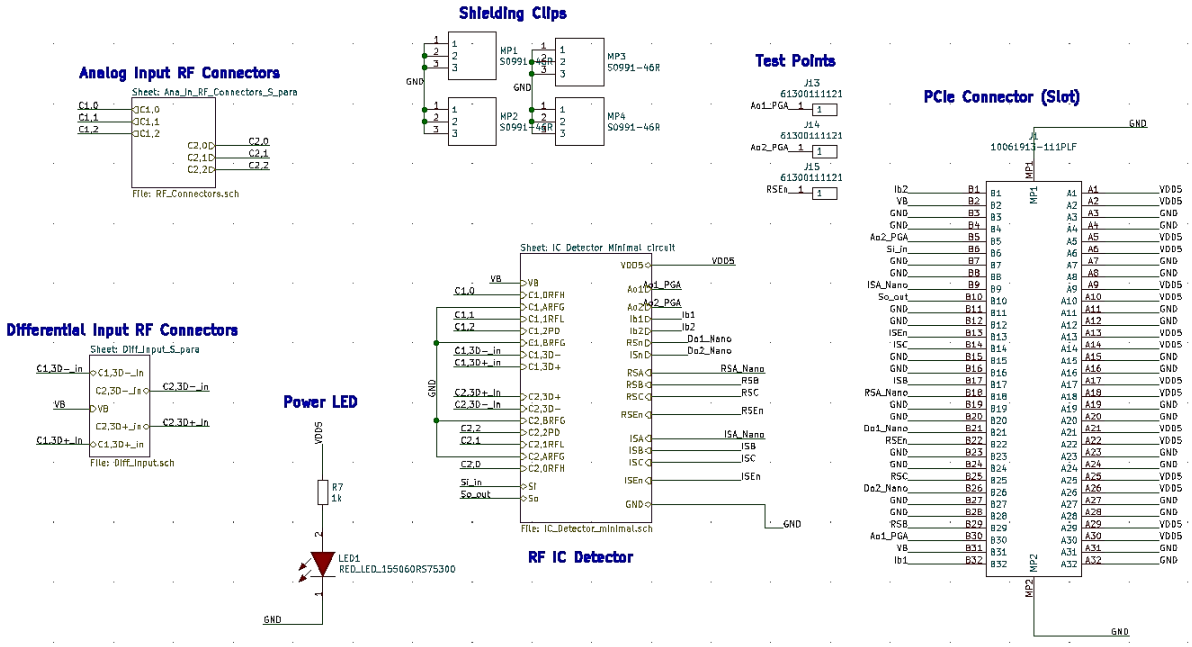

Figure 226: Shows the schematic of the GTEM Board from KiCAD.

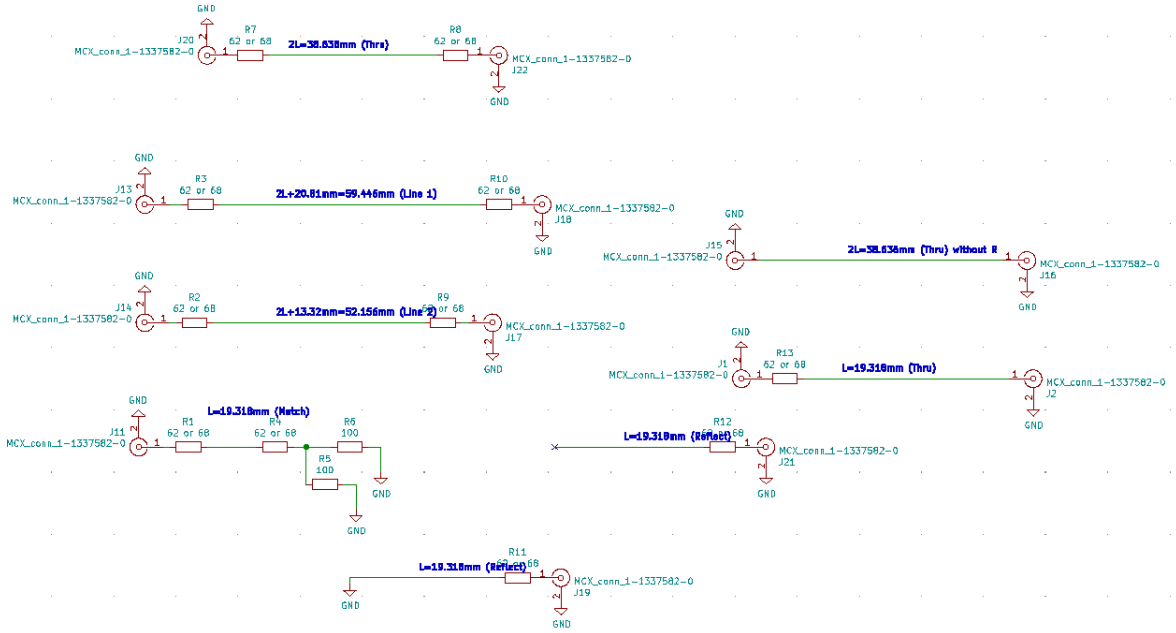

Figure 227: Shows the schematic of the TRL calibration board for the GTEM board from KiCAD.

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11.9 RF IC Detector Layout Designs

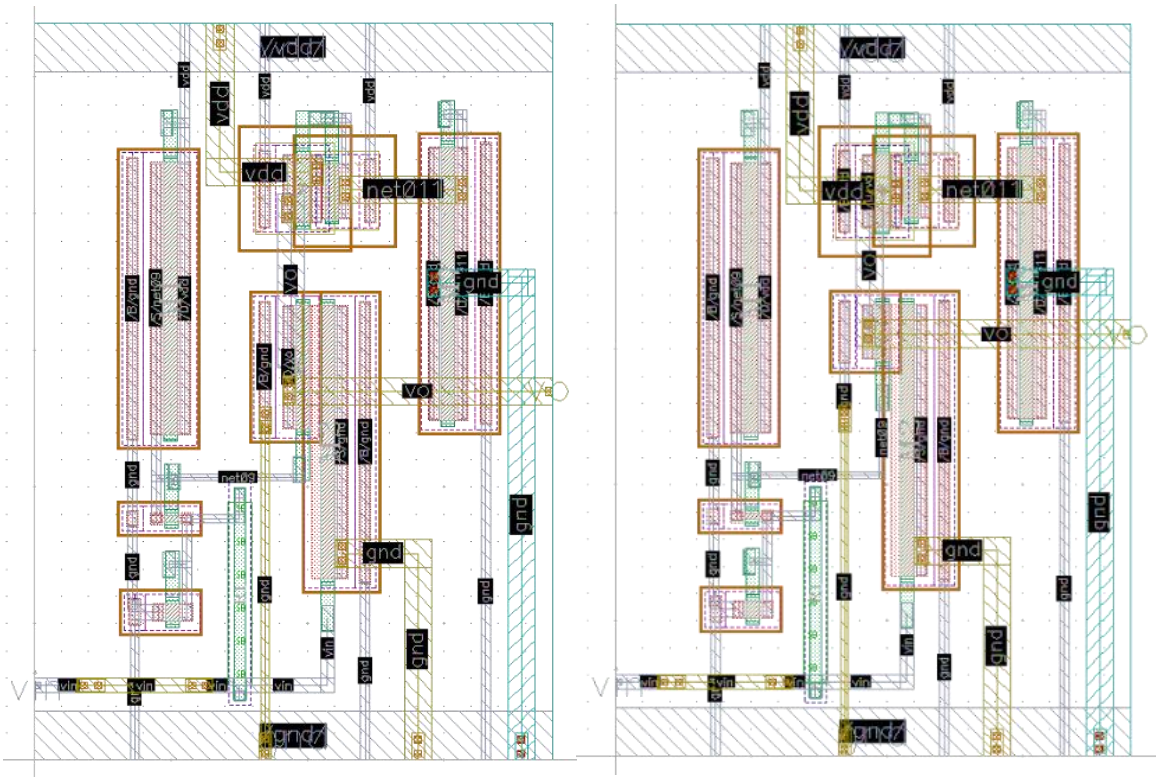

Figure 228: Left figure shows the layout of the High Gain RF Amplifier and the right figure shows the layout of the Broadband RF Amplifier.

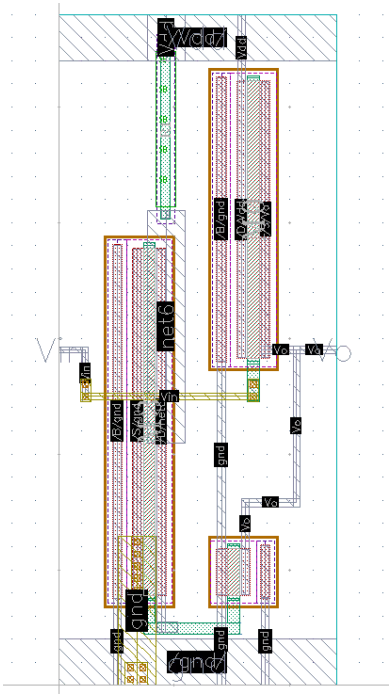

Figure 229: Shows the layout of the Source Follower amplifier.

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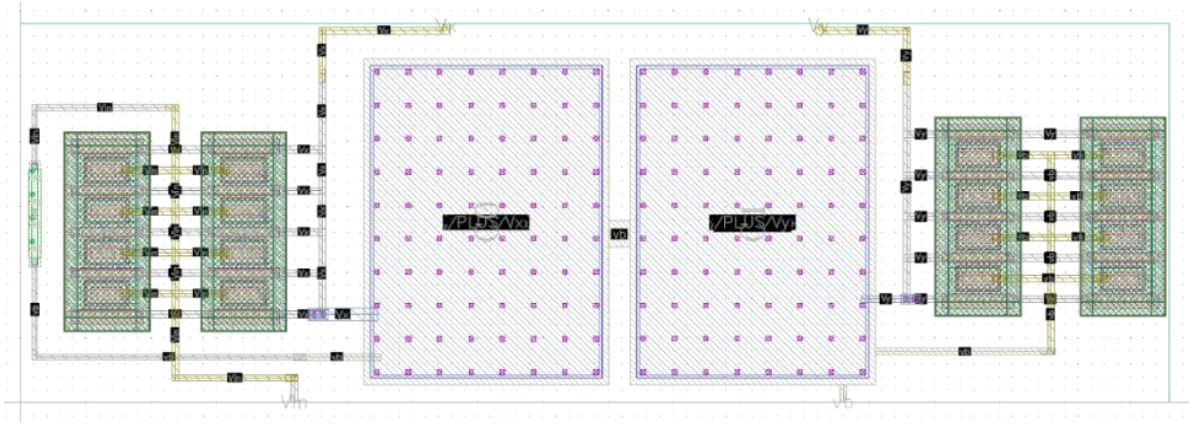

Figure 230: Shows the layout of the Peak Detector.

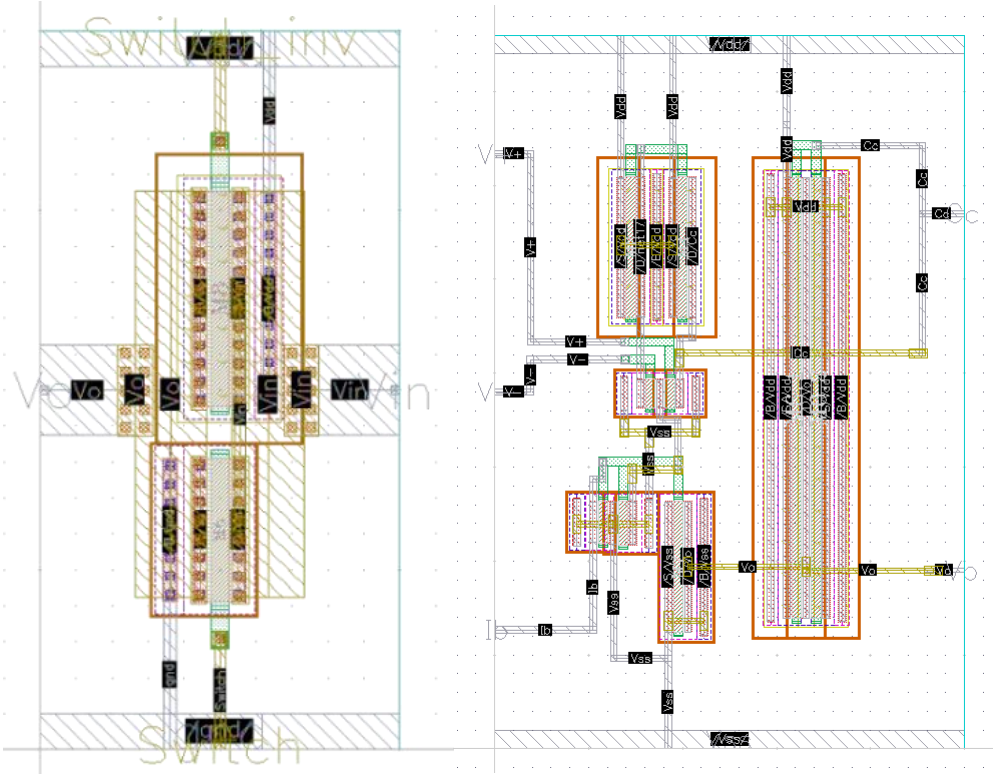

Figure 231: Left figure shows the layout of the Analog CMOS Switch and left figure shows the Two-stage OPAMP layout design.

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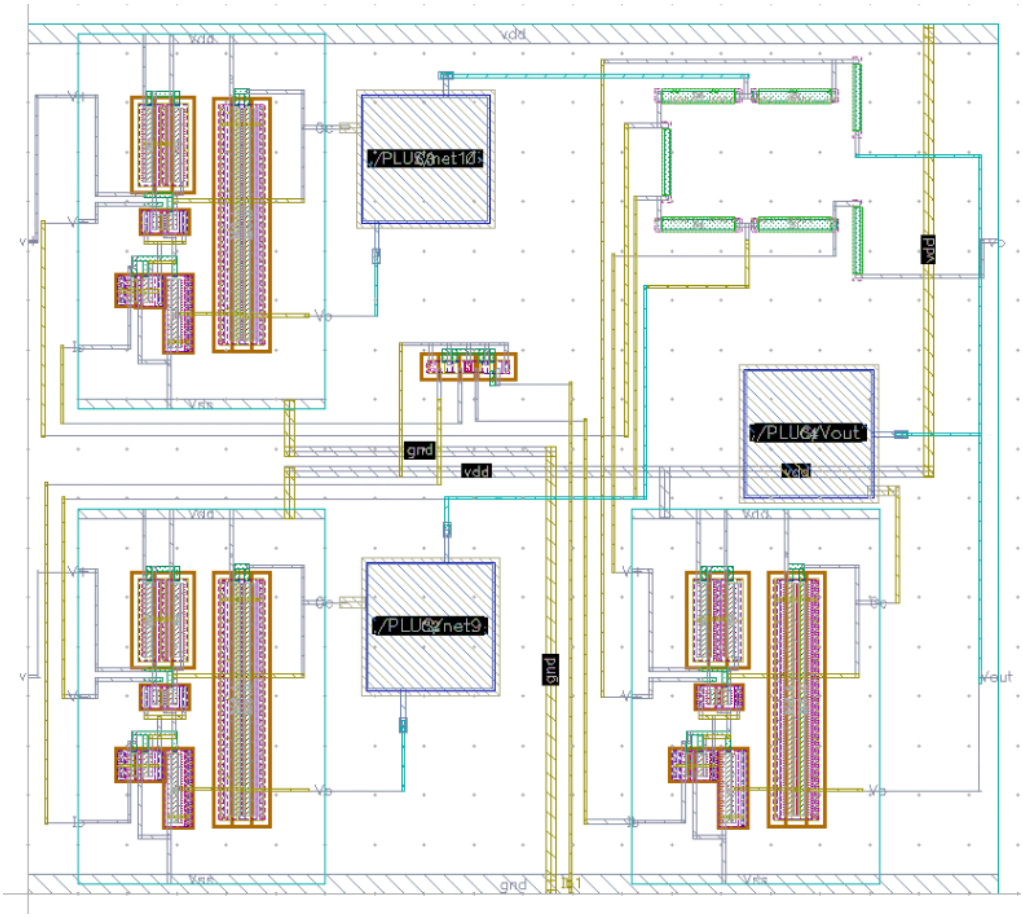

Figure 232: Instrumentation Amplifier layout

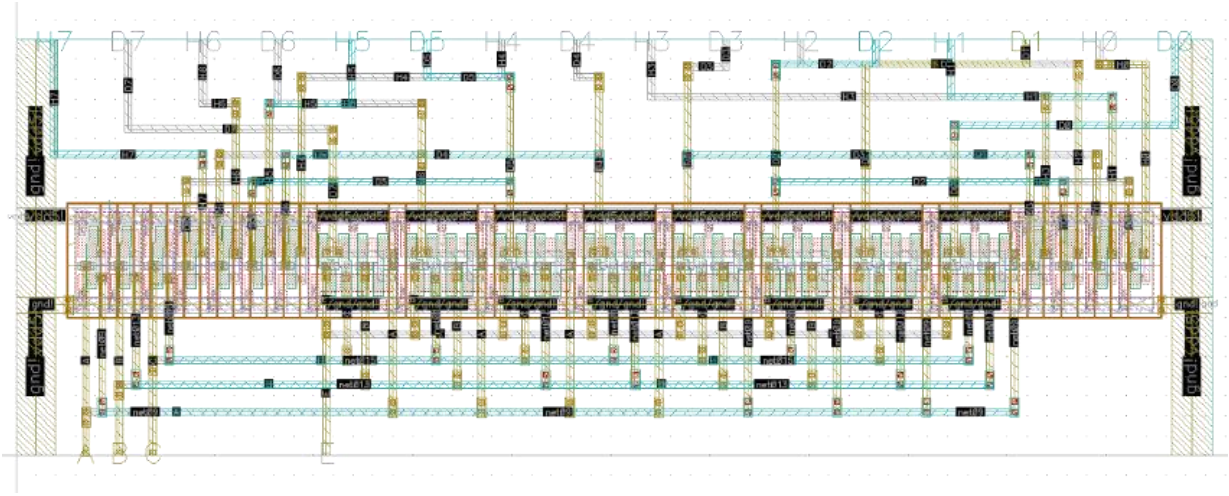

Figure 233: Shows the 3-8 line decoder layout..

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11.10Pin Definition of RF IC Detector

Pin no	Default Pin Name	Meaningful Pin Name	Bias Voltage / Current	Description	S-para Pins	Bias T
Pin 1	A1	C1,0RF_Gain	Int 1.324V	Channel 1 sub-channel 0, which has a High Gain RF amplifier (BW=1.28 GHz and Gain=14.5), Source Follower and Peak Detector.	Yes	-
Pin 2	RF gnd1	C1,ARFG	Int 0V	RF ground for C1,0 and C1,1 inputs	-	-
Pin 3	A2	C1,1RF_BW	Int 1.324V	Channel 1 sub-channel 1, which has Broadband Instrumentation RF amplifier (BW=2.22 GHz and Gain=6), Source Follower, and Peak Detector.	Yes	-
Pin 4	Ib1	Ib1	30.13 uA (84.5 kΩ)	Current bias to Channel 1 Amplifier (PMOS current mirror, requires 84.5kΩ of the external resistor connected to the ground).	-	-
Pin 5	-	NC	-	Not Connected	-	-
Pin 6	VDDO	VDDO	5V	I/O supply cell: connects to VDDO supply rail for output buffers and ESD protection structures	-	-
Pin 7	VDDR	VDDR	5V	I/O supply cell: connects to low noise VDDR rail for input buffer power supply	-	-

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Pin 8	VDD5	VDD5	5V	5V core VDD supply cell: connects to the VDD power rails	-	Yes
Pin 9	GNDO	GNDO	0V	I/O ground cell: connects to the GNDO ground rail for output buffers and ESD protection structures	-	Yes
Pin 10	GNDR	GNDR	0V	I/O ground cell: connects to the GNDR low noise ground rail for input buffer supply	-	-
Pin 11	-	NC	-	Not Connected.	-	-
Pin 12	-	NC	-	Not Connected.	-	-
Pin 13	Ib2	Ib2	-	Current bias to Channel 2 Instrumentation Amplifier (PMOS current mirror, requires 84.5kΩ of the external resistor connected to ground).	-	-
Pin 14	A3	C2,1RF_BW		Channel 2 sub-channel 1, which has Broadband RF amplifier (BW=2.22GHz and Gain=6), Source Follower and Peak Detector.	Yes	-
Pin 15	RF gnd2	RF gnd2	-	RF ground	-	-
Pin 16	A4	C2,0RF_Gain	-	Channel 2 sub-channel 0, which has a High Gain RF amplifier (BW=1.28 GHz and Gain=14.5), Source Follower and Peak Detector.	Yes	-
Pin 17	A5	C2,2_PD		Channel 2 sub-channel 2, which has only a Peak Detector	Yes	-

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Pin 18	RF gnd3	C2,BRFG	-	RF ground for C2,0 and C2,1 inputs	-	-
Pin 19	A6	C2,3D+	2.5V	Channel 2 sub-channel 3, Differential Plus, which is directly fed to Channel 2 Instrumentation Amplifier.	Yes	Yes
Pin 20	A7	C2,3D-	2.5V	Channel 2 sub-channel 3, Differential Minus, which is directly fed to Channel 2 Instrumentation Amplifier.	Yes	Yes
Pin 21	-	-	-	Not Connected.	-	-
Pin 22	VDDR	VDDR	5V	I/O supply cell: connects to low noise VDDR rail for input buffer power supply	-	-
Pin 23	VDDO	VDDO	5V	I/O supply cell: connects to VDDO supply rail for output buffers and ESD protection structures	-	-
Pin 24	VDD5	VDD5	5V	5V core VDD supply cell: connects to the VDD power rails	-	-
Pin 25	GNDO	GNDO	0V	I/O ground cell: connects to the GNDO ground rail for output buffers and ESD protection structures	-	-
Pin 26	GNDR	GNDR	0V	I/O ground cell: connects to the GNDR low noise ground rail for input buffer supply	-	-
Pin 27	-	-	-	Not Connected.	-	-
Pin 28	-	-	-	Not Connected.	-	-
Pin 29	Vb2	Vb2	2.5V	Voltage bias for Channel 2 Peak Detector and	-	-

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				Instrumentation Amplifier.		
Pin 30	Ao2	Ao2_IC	2.5V (internal)	Channel 2 Analog Output from Instrumentation Amplifier. Bias follows Vb2	Yes	Yes
Pin 31	Si	Si	2.5V	To operate Test Switch, i.e. Si and So. Reset Switch Decoder input of 011 is given.	-	-
Pin 32	So	So	2.5V	To operate Test Switch, i.e. Si and So. Reset Switch Decoder input of 011 is given.	-	-
Pin 33	D8	ISEn	-	Analog Input Switch Decoder Enable	-	-
Pin 34	D7	ISC	-	Analog Input Switch Decoder Input C	-	-
Pin 35	D6	ISB	-	Analog Input Switch Decoder Input B	-	-
Pin 36	D5	ISA_IC	-	Analog Input Switch Decoder Input A	Yes	Yes
Pin 37	NC		-	Not Connected.	-	-
Pin 38	VDDR	VDDR	5V	I/O supply cell: connects to low noise VDDR rail for input buffer power supply	-	-
Pin 39	VDDO	VDDO	5V	I/O supply cell: connects to VDDO supply rail for output buffers and ESD protection structures	-	-
Pin 40	VDD5	VDD5_IC40	5V	5V core VDD supply cell: connects to the VDD power rails	Yes	-
Pin 41	GNDO	GNDO_IC41	0V	I/O ground cell: connects to the GNDO ground rail	Yes	-

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				for output buffers and ESD protection structures		
Pin 42	GNDR	GNDR	0V	I/O ground cell: connects to the GNDR low noise ground rail for input buffer supply	-	-
Pin 43	-	-	-	Not Connected.	-	-
Pin 44	-	-	-	Not Connected.	-	-
Pin 45	D4	RSEn	-	Reset Switch Decoder Enable	-	-
Pin 46	D3	RSC	-	Reset Switch Decoder Input C	-	-
Pin 47	D2	RSB	-	Reset Switch Decoder Input B	-	-
Pin 48	D1	RSA_IC	-	Reset Switch Decoder Input A	Yes	Yes
Pin 49	Do1	Do1_IC	-	To select the Test Decoder output Do1, Reset Switch Decoder input of 111 is given.	Yes	Yes
Pin 50	Do2	Do2_IC	-	To select the Test Decoder output Do2, Analog Input Switch Decoder input of 111 is given.	Yes	-Yes
Pin 51	Ao1	Ao1_IC	2.5V (internal)	Channel 1 Analog Output from Instrumentation Amplifier. (follows Vb1)	Yes	Yes
Pin 52	Vb1	Vb1	2.5V	Voltage bias for Channel 1 Peak Detector and Instrumentation Amplifier.	-	-
Pin 53	-	-	-	Not Connected.	-	-
Pin 54	VDDR	VDDR	5V	I/O supply cell: connects to low noise VDDR rail	-	-

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				for input buffer power supply		
Pin 55	VDDO	VDDO	5V	I/O supply cell: connects to VDDO supply rail for output buffers and ESD protection structures	-	-
Pin 56	VDD5	VDD5	5V	5V core VDD supply cell: connects to the VDD power rails	-	-
Pin 57	GNDO	GNDO	0V	I/O ground cell: connects to the GNDO ground rail for output buffers and ESD protection structures	-	-
Pin 58	GNDR	GNDR	0V	I/O ground cell: connects to the GNDR low noise ground rail for input buffer supply	-	-
Pin 59	-	-	-	Not Connected.	-	-
Pin 60	-	-	-	Not Connected.	-	-
Pin 61	A10	C1,3D-	2.5V	Channel 1 sub-channel 3, Differential Minus, which is directly fed to Channel 1 Instrumentation Amplifier.	Yes	Yes
Pin 62	A9	C1,3D+	2.5V	Channel 1 sub-channel 3, Differential Plus, which is directly fed to Channel 1 Instrumentation Amplifier.	Yes	Yes
Pin 63	RF gnd4	C1,BRG	-	RF ground	-	-
Pin 64	A8	C1,2PD	2.5V	Channel 1 sub-channel 2, which has only Peak Detector (bias as Vb2)	Yes	-

Table 17: RF IC detector pins with description, pins marked in yellow are used for S-parameter measurement

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