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NUMERICAL STUDY OF 1.2kV SCALED FS-TRENCH IGBT

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AUTHOR'S DECLARATION

This thesis contain research undertaken by the author between December 2019 and May 2023 at the University of Sheffield, under the supervision of Prof. Shankar N. Ekkanath Madathil and Dr. Thomas Walter.

This research as contain here is entirely my own original work and has not been wholly or partly submitted for any other degree at any academic institution.

This thesis was prepared within the regulation underlined by the University of Sheffield for the degree of Master of Philosophy.

The information as contain within this thesis is confidential

Paulinus, Ejike Okpagu

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ABSTRACT

Trench Insulated Gate Bipolar Transistors (TIGBTs) are the foundation of modern, low, medium, and high-power converters and serve as the main component in diverse power electronic applications today such as Motor drives, Induction heating, UPS, Vacuum cleaners etc. latest growth in Trench IGBTs technologies is focused on increasing its power densities and switching frequencies with the target of competing with Wide Band Gap (WBD) power devices. This thesis aims towards studying of 1.2kV scaled Field Stop Trench IGBT using numerical analysis. In this work, 1.2kV FS-TIGBT was modelled, characterised, and scaled employing the scaling principle in the literature. Towards developing and characterizing the Trench IGBT model, a Sentaurus Technology Computer Aided Design (TCAD) that houses a written program specifically meant and designed for semiconductor physics Finite Element Method (FEM) simulation was deployed. Literature review regarding FEM simulations was carried out as well as the physics involved in IGBT operation. Static and dynamic characteristics of the developed Trench IGBT model was evaluated in depth and a comparison was drawn against the scaled device and it was confirmed that the scaled device k=3 have an improved static (I-V) characteristics mainly due to enhanced Injection Enhancement (IE) effect. For the both conventional and scaled devices (k=1 and k=3), the forward on-sate voltage drop $V_{ce(sat)}$ at current rating of 40A are 1.6V for k1 and 1.4V for k3 at 300K. At the same time, the values for the $V_{ce(sat)}$ for the both devices were increased to 1.9V for k1 and 1.6V for k3 at the junction temperature of 400K for the same current rating. For the scaled device k=3, the on – state voltage drop $V_{ce(sat)}$ was lowered by 12.5% at 300K and 16% at 400K respectively. The increase in collector emitter saturation voltage $V_{ce(sat)}$ at high temperature is due to increase in channel resistance. However, it was confirmed in the course of the study that the scaled device k=3 suffers limitation of short circuit capability and during this period, it has been noticed an occurrence of oscillation and overshoot in the gate-emitter voltage threatening the robustness of the device. The limitation in short circuit capability is due to Collector Induce Barrier Lowering (CIBL) effect caused by conductivity modulation in the middle of the mesa region (channel inversion layer) and this led to increase in the channel conductivity and thus result to current un-saturation. In overcoming the limitation of short circuit capability posed by the scaled device, a new scaled device was proposed. The depth of the p+ emitter in the p-base region for the proposed device was slightly increased in order to mitigate the effect of CIBL in the mesa region and ensure current saturation. The optimal depth of the p+ emitter which gave the expected result in terms of current saturation was 0.24um. Thus, the short circuit capability was improved while maintaining same on-state voltage drop and turn-off losses for the proposed and conventional scaled devices.

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INTRODUCTION

1.1 Research Background

With a view to meeting the ever-rising electricity demand for electric cars, industrial drive, domestic use etc. as the world population is increasing, there is urgent need to explore other possible sources of energy other than fossil fuel. According to recent statistics published by the UK Government in 2020, renewable energy supplied most of the UK electricity in 2020 compared to the electricity generated through fossil fuel (non-renewable energy sources) [1]. Similarly, the European Union's electricity generated through renewable energy source in 2020 was the main source of electricity generated in Europe for the first time and stood at 38%, surpassing coal and gas.

Going forward, the capacity of renewable energy source (wind and solar) in 2020 in Europe rose to 51TeraWatt hours, which is even beyond estimated average according to report [2]. It is said regarding the released report that the capacity will have to be increased by 100TWh yearly for the purpose of meeting the new climate goal. All these reports clearly reveal that the world energy utilization is rapidly shifting towards renewable energy sources. Renewable energy are clean sources of energy as there is no emission of toxic gases such as carbon-monoxide into the atmosphere which possess a serious threat to human health.

In an effort to save energy in converting electrical power from generation to end use, there is need for efficient and reliable power electronic devices. The rise in energy demand efficiency of power converters informed the need for the reduction in the conduction losses in power semiconductor devices. It is estimated that significant amount of global electrical energy utilization could be saved yearly due to increase in power converter efficiency [3]. At this point it is necessary to briefly discuss the concept of power electronics devices and their applications to energy conversions as well as energy savings.

Power electronics refers to the processing of high voltages and currents to supply power that support diverse systems. Stable and reliable electric power is needed in electronic appliances which requires stepdown transformers and rectifiers to provide the required power output needed for such device from the AC main source. In this way, utilizing power semiconductor switches, power supply in AC form is being converted to a DC form. In practical applications, power electronic devices plus a circuit with additional components are required to deliver power to electrical appliances and devices which includes but not limited to motor speed

control, air conditioning systems in homes, industrial drive etc. The additional components attached to a power electronic device in a circuit tends to control the power electronic switches to actualize the desired output. The Figure 1.1 below show a simple power electronic system. The additional components attached to the power electronic device include the firing circuit and feedback circuit from the load sensor [4] [5].

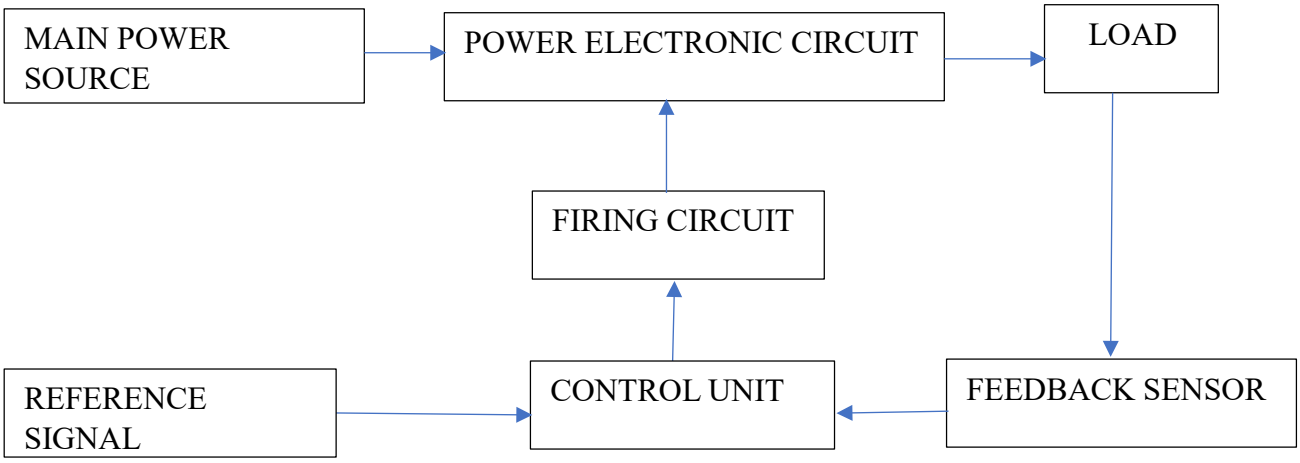


Figure 1.1: Power Electronic System [2]

The control unit compares the output from the feedback sensor and the input of the reference signal and feed the generated error signal to the firing circuit. The firing circuit which is a pulse generating unit controls the power electronic circuit. The load receives the needed electrical power and therefore gives the actual result. The overall result is that the load receives the precise electrical power and delivers the needed result. Power electronics play a significant role in delivering power based on the required specification.

Based on their control method, power semiconductor devices can be grouped into two categories: They include voltage or current controlled. Recently, there is a growing drift in the majority of power devices being voltage-controlled owing to simple gate drive circuit and less power consumption when compared with current controlled power devices such as Gate Turn – off Thyristors (GTO), Silicon Controlled Rectifiers, Bipolar Junction Transistors (BJTs) and etc [1], [2]. Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are voltage controlled power device with a higher switching frequency due to its unipolar characteristics and utilizes only electron for current conduction. Irrespective of its switching speed, MOSFETs are susceptible to higher on – state resistance and low power handling capability compared to a BJT or IGBT as a result of lack of conductivity modulation [3]. IGBTs are voltage controlled and has a higher voltage blocking capability and capable of handling higher power per unit area

due to the presence of conductivity modulation. In an ideal device, voltage and current are switched instantaneously and give zero resistance in its on-state and infinite resistance in the off-state. However, such device does not exist in the real world [4][5].

Switching and conduction losses are the two major types of losses in power devices. These losses occur during turn-on as well as turn-off. During turn-on, the voltage across the switching device is lowered significantly from its high value when the device is in the off state. Concurrently, the current across the device rises from zero to the load current level. Power losses occur as the switching process takes finite time. Conduction losses occurs during the on state. It is because of finite on-state forward voltage drop across the switch. Through improvement in the device structure, conduction losses can be made minimum.

Owing to cost reduction and reliability point of view, silicon-based power semiconductor devices will continue to be valuable in both present and future power electronics systems. Of recent, there has been a remarkable growth in Wide Band Gap power semiconductor devices such as Silicon Carbide and Gallium Nitride and they are recently being adopted into high efficiency power conversion systems [6]. On the other hand, due to lower cost market as has been stated above, silicon semiconductor devices such as Insulated Gate Bipolar Transistor (IGBT) are still very relevant. Therefore, optimization in the field of silicon IGBT technology is needed to ensure an energy- saving society. Accordingly, power devices made up of IGBTs plays a significant role in the global energy savings.

In an endeavour to further decrease the on-state voltage drop and increase the power handling capability of Trench IGBT, a scaling approach was proposed by several researchers to decrease a mesa width of the device in order to realize the goal. The reduction in the on-state voltage in the scaled device is due to Injection Enhancement (IE) effect [7]. The Injection Enhancement effect also leads to unsaturation of the MOS channel current resulting to remarkable degradation of short circuit ruggedness [8], [9]. The poor performance in short circuit capability of the scaled Trench IGBT device is due to Collector Induced Barrier Lowering (CIBL) effect in the middle of the region [8] which came into play as a result of conductivity modulation in the MOS channels [9]. For us to achieve a more robust device and increased performance, it is important to consider not only the lowered conduction losses in the application of power semiconductor devices but also its stability during short circuit condition.

Therefore, in this work, a scaled device k=3 is proposed which tends to overcome the challenges of short circuit limitation posed by the conventional scaled k=3 device. In the proposed scaled device, the depth of the p+ layer in the P-base is slightly increased which enhances the CIBL

by clamping down the conductivity modulation in the channel inversion layer within the narrow mesa width thereby achieving a current saturation and consequently an improved short circuit robustness as well as maintaining a good trade-off relationship between the on-state voltage drop and turn-off loss.

1.2 Motivation for the Research

Increased energy efficiency and dependable power electronics play essential role in energy savings as electric power has to go through the process of power electronic converters from the point at which it was generated to the end use. Thus, in an endeavour to save energy in converting electrical power from generation to end use necessitate the need for efficient and reliable power semiconductor devices. The growing demand for energy efficiency in power electronics requires lowering in the on – state and switching losses in power devices and this can undoubtedly lead to an appreciable savings of the entire world electrical energy consumption yearly. Owing to cost effectiveness, reliability and affordability perspective, silicon-based power semiconductor devices will continue to be relevant in both present and future electronics systems. Recently, Wide Band Gap (WBG) power devices such as silicon carbide (SiC) and Galliun Nitride (GaN) have exhibited some excellent performance regarding faster switching speeds, reduced energy losses as well as its capability of operating at higher temperature. However, a challenge currently present is the manufacturing complexity and high cost for Wide Band Gap power devices. The fabrication of GaN requires specialized techniques and equipment which can be more complex and expensive compared to silicon-based power semiconductor devices. Silicon-based power device such as Insulated Gate Bipolar Transistors (IGBTs) are presently the most extensively used power devices in the industry owing to their MOS gate control, low on – state and switching losses as well as its affordability and low cost. Therefore, optimization in the domain of silicon IGBT technology is necessary to realize an energy saving society. Hence, the focus of this thesis is towards lowering the on – state losses in Trench IGBT and improve its short circuit capability through scaling approach and optimization of the device emitter region.

1.3 Research Aim and Objectives

This research is aimed at studying of the 1.2kV Scaled Field Stop-Trench Gated IGBT using numerical analysis. This is achieved through mixed mode 2-dimensional device and circuit simulation tool (TCAD Sentaurus). Specific objectives that were followed in realizing the aim includes the following:

- Developing a 1.2kV FS-Trench Gated IGBT model employing a demonstration model code available in the Sentaurus TCAD library and modifying accordingly having reviewed appropriate literatures within and outside the research group.
- Scaling down the emitter region of the developed 1.2kV Trench Gated IGBT employing the scaling rule available in literature [11]. 2-dimensional scaling approach was adopted using Synopsys TCAD Sentaurus. The dimensions of the mesa width (trench – trench spacing), the trench depth, the MOS-channel (P-base) depth and the gate oxide thickness were all reduced according to the scaling rule.
- Static Electrical Characteristics such as the Breakdown Voltage, Static I(V) and threshold voltage characteristics of both the scaled and the conventional devices were simulated in Sentaurus Device for comparison.
- This is followed by dynamic (turn-on and turn-off) and short circuit simulation under inductive loads using mixed mode 2- dimensional device and circuit simulations. After the simulations, comparison was carried-out for both the scaled and the conventional device.
- The emitter region of the scaled device k=3 (TIGBT) is re-structured by slightly increasing the depth of its p+ emitter layer from 0.08um to 0.24 um and the influence of the slightly increased depth of the p+ emitter on the scaled device is studied.

1.4 Thesis Structure

This thesis is organised in the following sequence:

- Chapter 2 discusses about the related works in the literature and offers a detailed insight and explanations on the trench Gated Insulated Gate Bipolar Transistor (IGBT) as a power semiconductor device.
- Chapter 3 discusses the design of the 1.2kV FS-Trench IGBT and its electrical characteristics which includes the static and dynamic characteristics of the designed 1.2kV FS-Trench IGBT device.
- Chapter 4 explains the 2-dimensional scaling concept for the Trench IGBT and discusses the in-depth analysis of the simulated results. A comparison of the electrical characteristics (static and dynamic characteristics) of both the conventional and the scaled device was made.

- Chapter 5 draws conclusion of the thesis and highlight the proposed future work for possible continuation of the research work. Appendix A provides the code for generating a 1.2kV FS-Trench IGBT model structure and its scaled counterpart.

CHAPTER TWO

LITERATURE REVIEW

2.1 Trench Gated Insulated Gate Bipolar Transistor (TIGBT)

Before the advent of the IGBTs (Insulated Gate Bipolar Transistors), low to medium voltage applications depended on power MOSFETs due to its high switching characteristics. On the other hand, medium to high voltage applications where high current conduction is needed relied on thyristors, gate turn-off thyristor (GTOs) and bipolar power transistors. A power MOSFET has an advantage of simple gate control circuit design as well as fast switching characteristics. On the contrary, as the breakdown voltage increases, power MOSFET has the drawback of rapidly increasing on-state resistance [10]–[12].

Due to low on-state voltage drop, bipolar power transistor possesses an excellent on-state features though have complex base control circuit and low switching speed compared with MOSFET. An IGBT was introduced in order to utilize both interesting features of MOSFET and bipolar junction transistor (BJT). Thus, an IGBT integrates the best features of both MOSFET and BJT which is easy gate drive circuit of MOSFET, it's fast switching speed and low on-state voltage drop of BJT to achieve ideal device features [11].

In power electronics, IGBT is useful in diverse applications such as three-phase drives, uninterruptible power supplies (UPS), switched-mode power supplies (SMPS), resonant- mode converter circuit etc. IGBT is a bipolar semiconductor device which uses both electrons and holes as charge carrier during current conduction and as a result can scale up its blocking voltage due to conductivity modulation. During on-state current conduction, the n-drift region resistance is significantly reduced by the large concentration of injected carriers (electrons and holes) and hole current carrier being injected from the collector P^+ layer. In contrast, for the power MOSFET, owing to the increase in the resistivity and thickness of the n-drift region needed to accommodate the high operating voltage, the on-state resistance drastically increases giving rise to high conduction losses [10], [12].

In order to further reduce the conduction loss in IGBT device and thus improve its performance in power conversion applications, a concept was proposed to decrease the mesa width and hence improve turn-off loss E_{off} and on-state voltage drop $V_{ce(sat)}$ trade-off according to the authors [8], [13]–[15]. It is worthy to note that much emphasis have not been made on the device ruggedness in the event of short circuit by the previous researchers, rather they

concentrated in lowering of the conduction losses $V_{ce(sat)}$ through scaling down of the mesa region. Thus, in the application of power semiconductor device, it is necessary to consider not just the reduced energy loss obtainable through narrowing or scaling down the mesa width but also to put into consideration high device ruggedness in the event of short circuit for improved device performance. However, it is reported [9] that narrow mesa IGBT structure is prone to poor short circuit robustness owing to collector induced barrier lowering effect occurring in the mesa region. Following this development, an improved mesa design was put forward by these researchers [9], [16]–[18].

However, moving forward in our aspiration towards improved device performance, scaling design in TIGBT was considered to increase the Injection Enhancement effect and CMOS process technology [19], [20] which has been reported by several authors [21]–[24]. Quite a couple of works on scaling design configuration on Trench IGBT and Trench Clustered IGBT (TCIGBT) has been reported in literature. According to Peng Luo [25]–[28], a 3-dimensional scaling design in TCIGBT realizes a substantial improvement in $V_{c(sat)}-E_{off}$ trade-offs as well as maintaining short circuit robustness. Despite advantages TCIGBTs possesses over TIGBTs, TIGBTs are still very attractive most especially for low to medium voltage applications owing to its availability and affordability among other interesting features such as low $V_{ce(sat)}$, current controllability and safe operating area (SOA). Thus, it has become necessary to consider not just its lowered conduction loss but also its capability to withstand high current and turns-off safely in the event short circuit. The influence of scaling rule on device performance not only reduce energy loss but also high robustness for improved performance have not been adequately dealt with. Thus, for a scaled device, the focus of this thesis will be on improving the device robustness in the event of short circuit.

In this work, a new scaled device k=3 is proposed which tends to achieve improved device performance in terms of robustness against short circuit event and also maintaining a good trade-off relationship between device turn-off loss and on-state voltage drop. In the proposed device, the p+ emitter in the p-base is increased. This suppresses conductivity modulation in the middle of the mesa region thereby maintaining current saturation.

2.2 The Structural Composition of IGBT

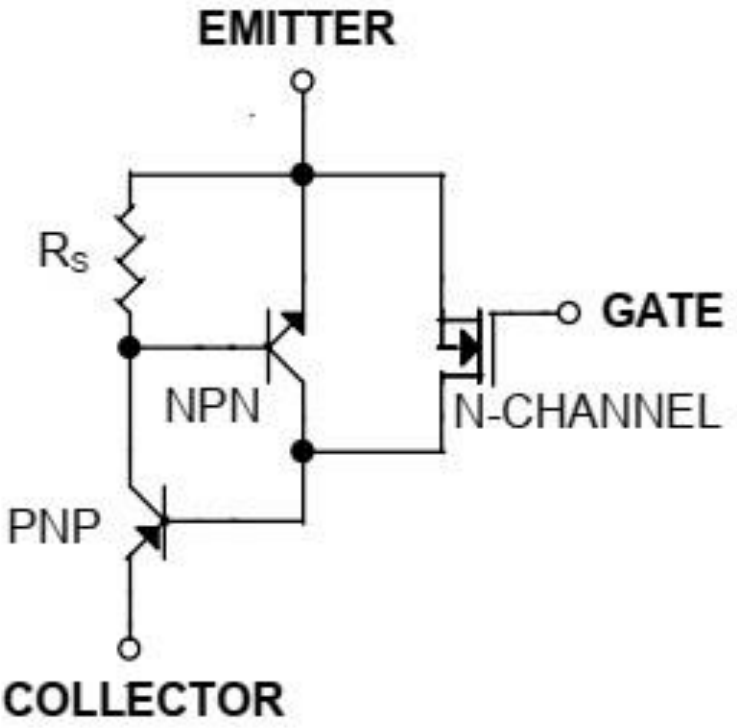


Figure 2.1: Equivalent Circuit of an IGBT [11]

Basically, IGBT has three terminals, the Gate, Emitter and Collector. Emitter is the n^+ layer at the top and the Collector is the p^+ layer. IGBT is made up of PNP and NPN transistors. For a proper function of the device, the NPN transistor is designed to be inactivated by shorting its base. The base activation current for the PNP transistor is fed from the MOS input channel. The four layered NPNP structure form a parasitic thyristor which is not required to be turnedon during the on-state. Structurally, IGBT is of two types namely the Non-Punch Through (NPT) IGBT and the Punch-Through (PT) IGBT. N- buffer layer distinguishes the two IGBTs, the IGBT without the presence of N- buffer layer is the NPT whereas the one with N-buffer layer is PT-IGBT [29].

The performance of the IGBT can be improved significantly when the doping and thickness of N-buffer layer is properly selected [29]. Despite the structural resemblance of IGBT and power MOSFET, its operating mechanism is rather closer to a power BJT. This is because IGBT is a bipolar device just like the power BJT utilizing both electrons and holes as majority as well as minority current carriers respectively. In IGBT, the collector p^+ layer account for the minority carrier injection into the n-drift region and the resulting conductivity modulation.

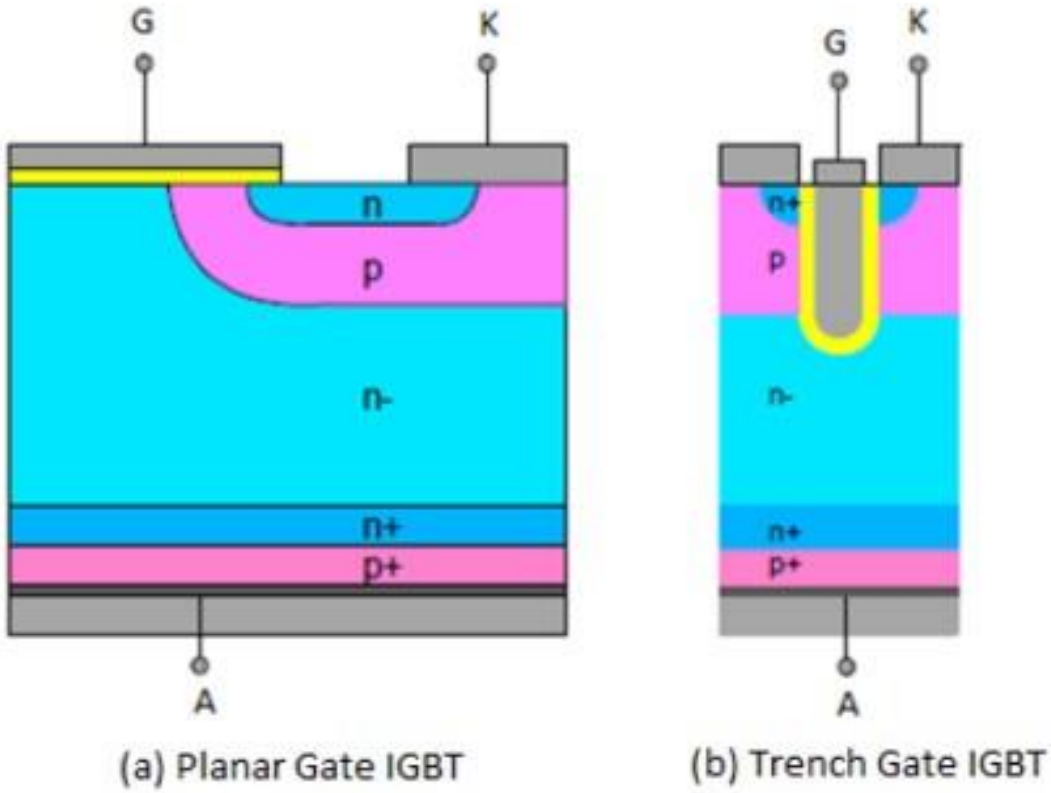


Figure 2.2: Structural composition of planar and trench gated IGBT [74]

2.2.1 Technologies of the IGBT Drift Region

During the turn-off state of IGBT, its drift region supports high voltage and therefore the voltage blocking capability is determined by the width of the drift region. The longer the width of the drift region, the higher the voltage blocking capability. However, a lengthy n-drift region would result to a higher on-state voltage drop owing to the high resistance. Electric field can be controlled to avoid punch-through to the collector (anode) by adjusting the doping concentration of the n-drift region. This occurs at a particular voltage called punch-through voltage. This will affect the on-state characteristics. Thus, in an attempt to overcome the tradeoff between blocking voltage and on-state performance, there exist different drift region technologies which are: Non-Punch Through (NPT), Punch-Through (PT) and Field Stop (FS).

2.2.2 Punch-Through Technology

Punch-Through or asymmetrical IGBT is the one that has an N^+ buffer layer between the thick p+ type substrate and n-drift region which is epitaxially grown on top. During the switching transition, the turn-off speed is improved by the N+ buffer layer through reduction of the minority carrier injection efficiency. Part of the injected holes from the p+ collector is recombined in the buffer region to improve switching performance. In addition, by lowering

the current gain of the PNP transistor, the latch-up characteristics are equally improved. The disadvantage to this is the increase in the on-state voltage drop.

However, with the same forward voltage blocking capability of a device, the thickness of the n-drift region can be lowered as the N+ buffer layer improves the forward voltage blocking capability. As a consequence of this, on-state voltage drop can be reduced. Thus, in terms of switching speed and forward voltage drop, the PT-IGBT has a better trade-off features when compared to the NPT-IGBT [30].

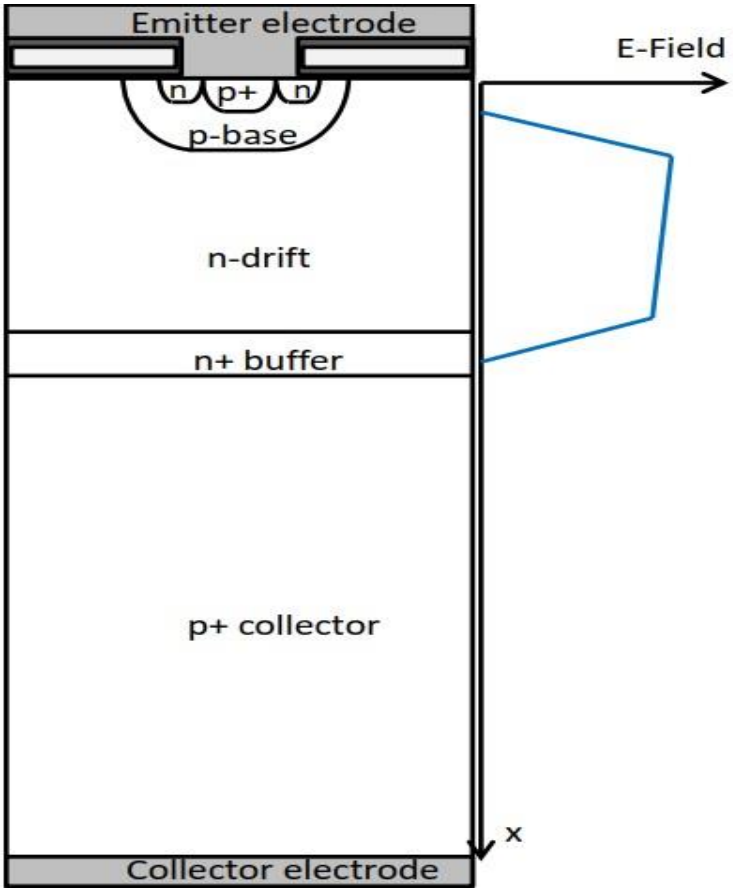


Figure 2.3: Punch-Through IGBT

During forward blocking state, the voltage punch through to the p+ collector layer is prevented due to the presence of the n-buffer region. This gives the PT-IGBT structure a trapezoidal electric field profile as shown in Fig. 2.3. Injection efficiency is high due to the presence of thick p+ collector and thus requires significant lifetime killing such as electron irradiation or proton implantation to minimize the gain of the PNP transistor and therefore lower turn-off losses and improve switching speed [31]. The PT device exhibits a negative temperature coefficient with on-state voltage drop which tends to decrease as the device temperature increases. It makes the device difficult to work in parallel configuration.

2.2.3 Non-Punch Through IGBT

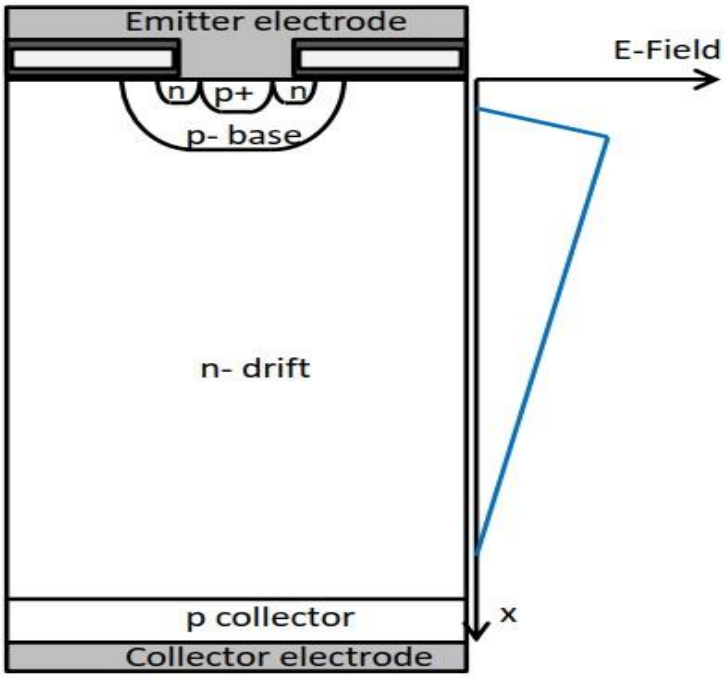


Figure 2.4: Non-Punch Through IGBT

Non-Punch Through (NPT) or symmetrical IGBT structure does not possess buffer layer and thus have a uniformly doped n-drift. During the forward blocking condition, the voltage is supported by the thickness and doping concentration of the n-drift region which then results in a triangular electric field profile. The p collector is normally very thin and lightly doped and does not require lifetime killing process. The required injection efficiency can be achieved by controlling the thickness of the p collector. Unlike the PT-devices, NPT possess a positive temperature coefficient for on-state voltage and therefore can be paralleled to achieve a high current density. The carrier lifetime of the NPT-IGBT is normally higher than the PT devices to achieve a suitable low on-state voltage. This is as a result of the lengthy drift region. In NPTIGBT, there is a trade-off between low forward voltage and switching speed. This is due to large carrier lifetime which have an impact on the switching speed.

NPT technology is perfect for device paralleling as it shows a positive temperature coefficient with regard to forward voltage drop [32]. This is quite contrary to the PT-device which possess a high transistor gain and lower carrier lifetime. The carrier lifetime and injection efficiency improve which gives rise to a lower on-state voltage drop at high temperature thus making PT devices not suitable for parallel connection. Due to wide base (n-drift region) and lower gain of the PNP transistor, the PNP-devices are more rugged than the PT-devices. Uniform distribution of the electric field enables NPT to absorb more avalanche energy than the PT

devices. Contrary to PT-IGBT, high reverse blocking voltage can be supported across the junction between the n-drift and p collector regions. With adequate deep p collector, a high reverse blocking voltage can be obtained in NPT-IGBT. To avoid reach through condition during the forward blocking, the width of the n-drift layer have to be sufficient.

2.2.4 Field Stop Technology

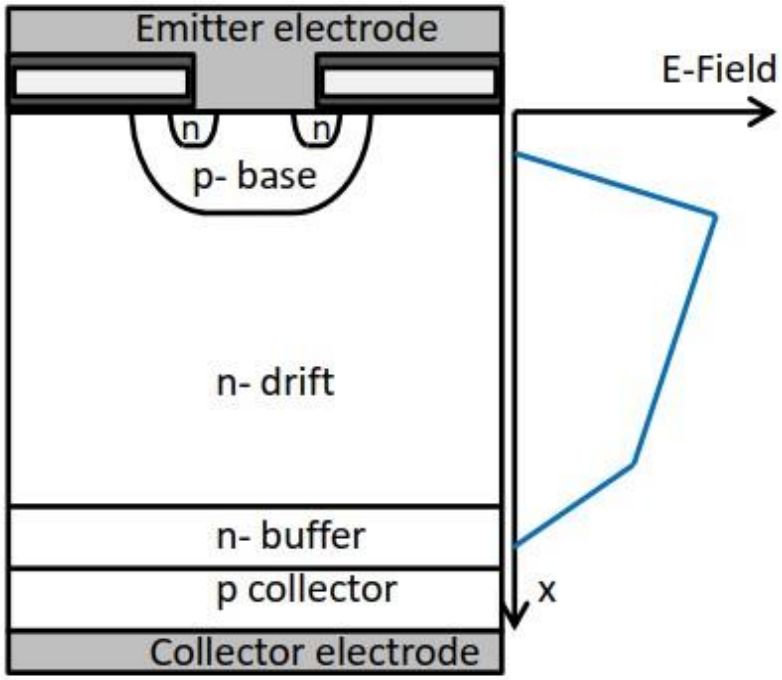


Figure 2.5: Field Stop IGBT

The Field Stop IGBT (FS-IGBT) or otherwise known as Soft Punch Through (SPT) is the state of-the–art technological improvement for n-drift region enhancement and combines the advantages of both PT and NPT technologies [33]. The FS- IGBT as shown in Fig.2.5 is fabricated using an n-type substrate with an n+ buffer region implanted and annealed. In FSIGBT, the transparent collector (anode) and buffer layer are combined together making the overall dimension smaller than the PT and NPT technologies [33]. The remarkable difference between FS and PT technologies is that in FS-devices, the p collector (anode) is thin, and its doping concentration is less compared to the PT-devices which has a thick and heavily doped p-collector. During the forward blocking condition, the buffer region stops the electric field from penetrating through the p+ collector and thus the electric field distribution assumes a trapezoidal shape like the PT-IGBT. The electric field reaches the collector earlier than in NPT devices during turn-off and the electric field sweeps out of the excessive carriers and therefore increases turn-off speed and efficiency [33], [34]. Contrary to the PT devices, the n-buffer region in FS-IGBTs is lightly doped in such a way that its impact on the p collector injection

efficiency is negligible. Thus, it is used for the goal of stopping the electric field from penetrating through to the p collector region. To achieve a lowered switching loss in FS-IGBT, a lightly doped p collector is used.

Table 2.1: Comparison of PT, NPT and FS Characteristics

S/N	Structure	PT-IGBT	NPT-IGBT	FS-IGBT
1	Drift Layer Thickness	Thin	Thick	Thin
2	Wafer Type	Epitaxial	Float zone	Float zone
3	Buffer Layer	Thick & highly doped	N/A	Thin & lowly doped
4	P+ Collector	Thick & highly doped	Thin & relatively lowly doped	Thin & relatively lowly doped
5	Bipolar Gain Control	Lifetime killing	Injection efficiency	Injection efficiency
6	On-state Losses	Low	Medium	Low
7	Switching Losses	High	Medium	Low
8	Turn-off Tail	Short	Long	Short
9	Temperature Coefficient	Negative	Positive	Positive
10	SCSOA (Short circuit condition)	Medium	Large	Large
11	RBSOA (Reversebiased condition)	Narrow	Large	Large
12	Devices in parallel	Hard	Easy	Easy

2.2.5 IGBT Optimization

Couple of decades ago has witnessed several phases of development in IGBT since its inception. Drift region engineering such as Punch – Through, Non – Punch Through and Field Stop IGBTs are the most paramount of all the development so far as have discussed in the sections above. Great attempts have been made to maximize and enhance the switching speed / forward voltage drop trade – off and widen the SOA limit. The three vital areas in which IGBTs development can be classified are: Drift Region, Cathode/Emitter and Collector Engineering. Drift region engineering, cathode/emitter engineering and collector/anode engineering. Collector/Anode Engineering is all about improving the collector hole injection by integrating local lifetime control [31] and introduction of impurities like gold and platinum [35]. Not long ago, fast switching enhancement was recorded due to modification of the collector/anode with the introduction of p+ region. Great attempt was made to minimize the JFET resistance in planar structure of IGBT by changing the doping concentration right under the gate. This is seen as the success achieved in the area of emitter/cathode engineering [36].

Nevertheless, trench gate is seen as the most remarkable development due to lowered on-state voltage drop and increase current density.

2.2.6 Trench Gate Structure

IGBT was originally invented with the possession of planar gate structure. It was noticed that the increase in the forward on-state voltage drop was due to the presence of JFET resistance in the planar IGBT-device as shown in Figure 2.6 below. The JFET region in planar structure is located directly under the gate. The voltage drop in the JFET region is due to the holes accumulation layer beneath the gate in the drift region. The JFET voltage drop was eliminated and the on-state voltage across the structure minimized through the use of vertical gate structure as can be shown in fig. 2.6 below [33], [37]–[39]. As a result of vertical current flow in trench structure, the chances of latch-up occurrence lower significantly as the probability of parasitic transistor turning on also reduces. On-state performance of trench devices have been reported to have improved via an occurrence known as injection enhancement [7] in which holes are injected into the drift region from the p+ collector and accumulate beneath the trench gate and increases the potential, thereby improving the electron current movement from the MOS channel.

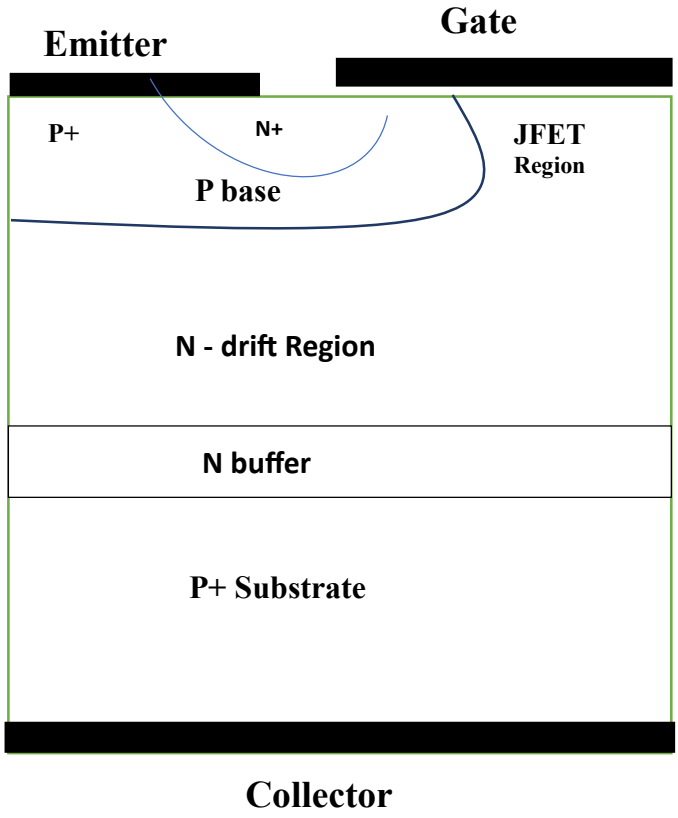


Figure 2.6: Planar Punch-Through IGBT showing JFET Region

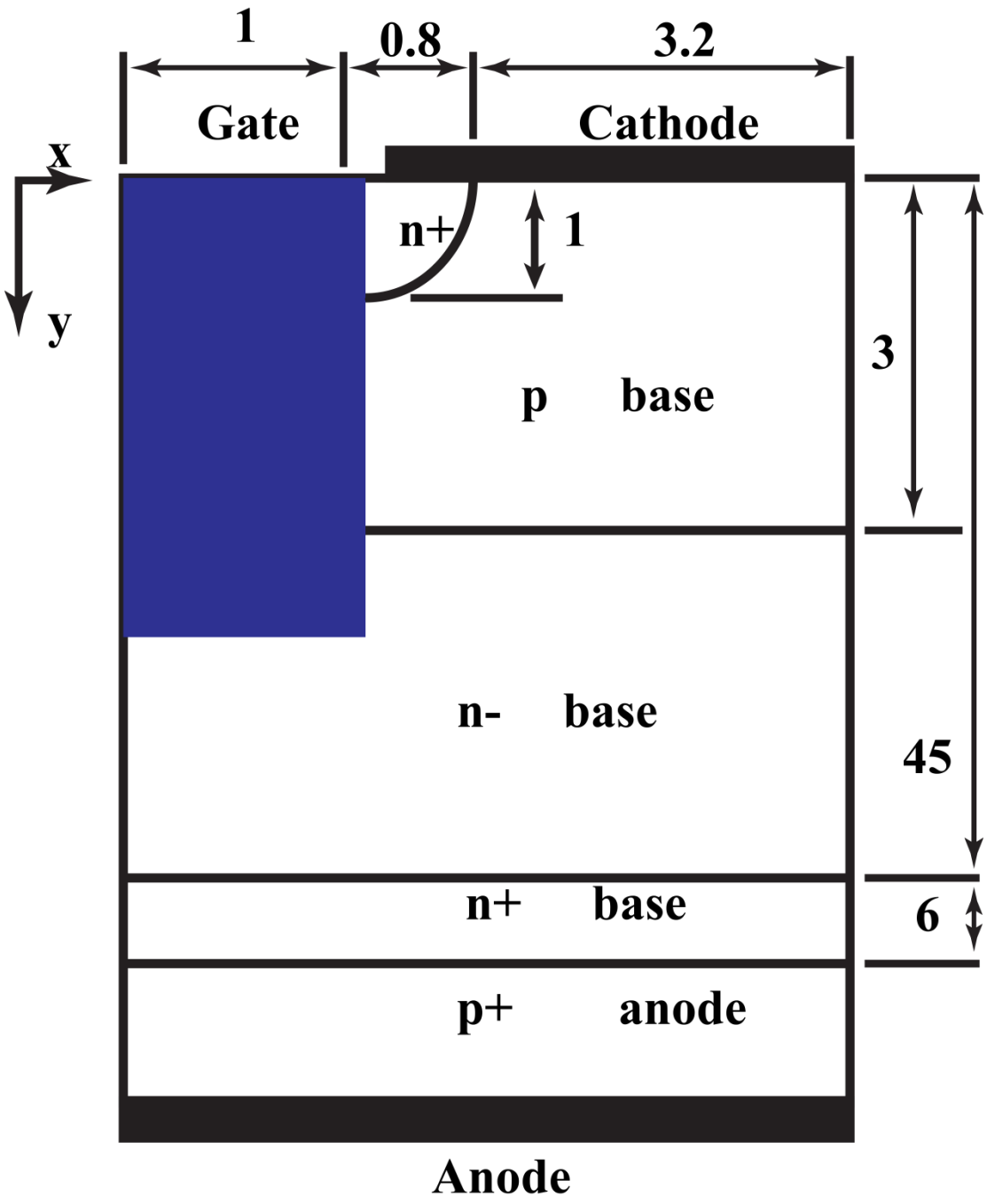


Figure 2.7: Trench gate IGBT structure [37]

Owing to closely packed cells in trench IGBTs, higher channel density is obtained. Hence, the superior on – state performance compared to that of planar devices. Moreover, trench IGBT exhibits increased saturation current density as a result of higher transconductance due to shorter channel length. Thus, trench IGBT possess poor short circuit withstand capability compared to planar IGBTs. The major impediment for the fabrication of trench devices is the cost factor. Notwithstanding the cost implication, trench devices are leading in power semiconductor market today [37].

2.2.7 Narrow Mesa Width IGBT

Trench gated IGBT geometry rated up to 3.3kV is extensively used in IGBT technologies due to its higher performance with regard to higher current density and reduced losses in comparison to planar IGBTs. The on - state characteristics of trench IGBTs can be enhanced remarkably by improving Injection Enhancement (IE) effect. Injection Enhancement can be defining as the increase of electron injection from the cathode [4], [5]. As the injected holes gets to the cathode side of the n-drift region, electron injection from the cathode is enhanced in order to satisfy charge neutrality. As a consequence, the electron and hole concentration in the n-drift region becomes considerably higher than those gained at thermal equilibrium which in turn produces a low ON resistance in the IGBTs therefore improving the performance of IGBTs. Scaling down the mesa width is one of the ways to improve IE effect from the device design perspective.

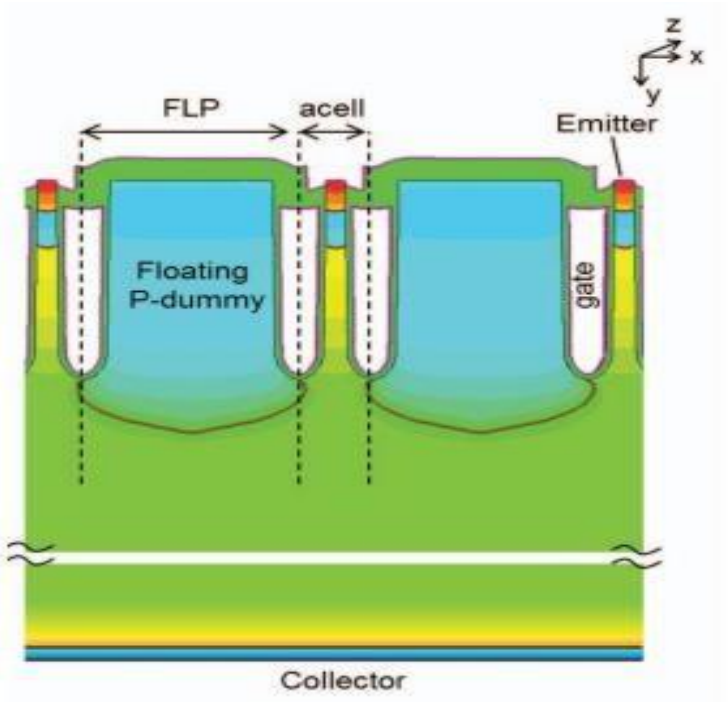


Figure 2.8: Narrow mesa width IGBT [14]

Fig. 2.8 is an example of a narrow mesa trench IGBT [8]. Numerous IGBT structures regarding narrow mesa design have been worked on which includes Ultra – narrow mesa Fin P – body IGBT (U-Fin – P IGBT) [40], Micro – Pattern Trench IGBT (MPT – IGBT) [15], Partially Narrow Mesa IGBT (PNM – IGBT) [14], 3-D scaled trench IGBTs [21], [22], [41] etc. Nevertheless, owing to non – saturated I-V characteristics possessed by trench IGBTs with narrow mesa, they exhibit poor short circuit performance. This is because, as a result of narrow

mesa, conductivity modulation occurs in the channel inversion layer during the device turn-on which leads to Collector Induced Barrier Lowering (CIBL) effect [9].

2.2.8 Parasitic Thyristor and Latch – up in IGBT

The IGBT is made up of parasitic PNPN thyristor structure between the collector and the emitter. A latch –up occurs when the parasitic thyristor is turned – on and when that is done, the IGBT will no longer be controlled by the MOS gate. Due to the excessive power dissipation, the IGBT would be destroyed. During turn – on, majority of the hole passes through the p – base to the metal electrode. As a result of this, lateral voltage drops across the shunting resistance R_s of the p – base. Electrons are therefore injected from the N+ emitter to the p – base when the voltage drop at the p – base becomes greater than the potential barrier of the junction between the N+ emitter and the p – base. Under this condition, the parasitic NPN transistor (N+ emitter, p – base and N-drift) is turned – on. Latch-up occurs if the addition of the two NPN, PNP parasitic transistors current gain becomes 1 ($\propto_{NPN} + \alpha_{PNP} \geq 1$). For an IGBT to function correctly, the parasitic transistor NPN need to remain off.

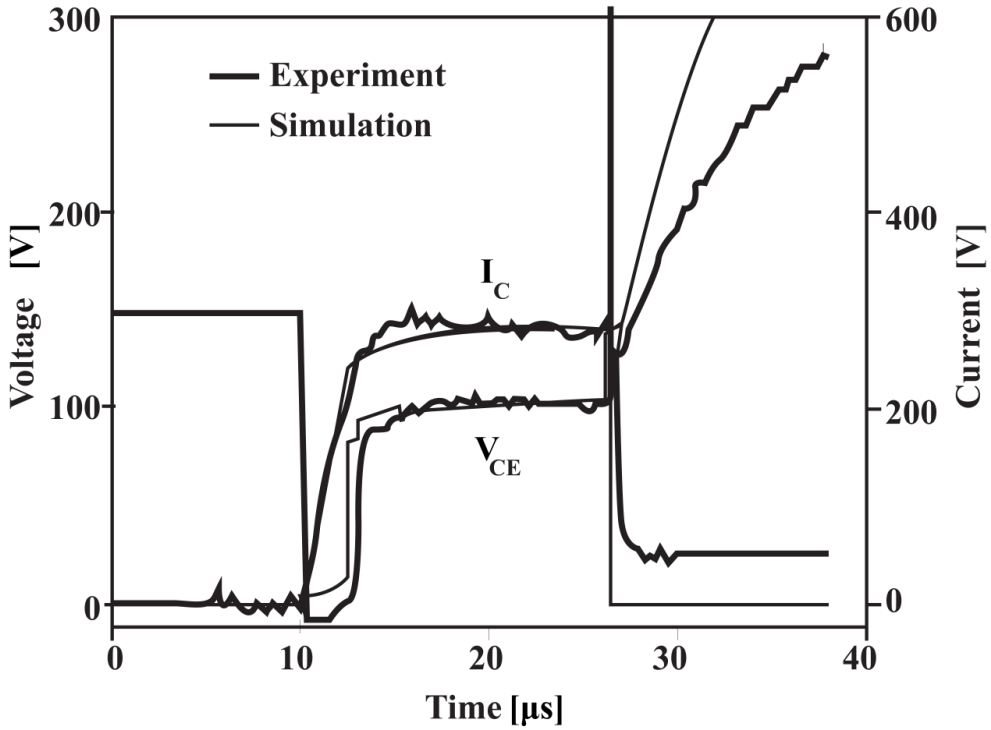


Figure 2.9: Experimental and simulated waveform of Latch – up occurrence in IGBT (V_{ce}=600V, V_g=15V, T_j=300K) [75]

Figure 2.9 showed a waveform of an IGBT going into latch – up as the device is being recovered from short circuit conditions. It is obvious in the figure that as the device is turned off at about 27us, the current I_C continues to rise to the point of the device failure and the rising rate is

determined by the load inductance. The voltage spike seen during the device turn-off is due to stray inductance in the circuit. The parasitic thyristor in the circuit is fired on due to dV/dt and the device fail to turn-off by the gate voltage. Through ensuring that shunting resistance Rs is low in order for the NPN transistor to remain off, Latch – up can be avoided. This is possible through device doping adjustment and optimization of the device geometry [38], [42], [43].

2.2.9 Short Circuit Operation

During short circuit event, high current and voltage are simultaneously applied for several microseconds usually less than 10us thereby causing significant rise in device temperature and could lead to device failure.

The device is operating in the saturation mode under short circuit condition and the collector current is limited by the value of the gate voltage (V_{GE}). Due to the limiting factor of gate voltage, the IGBTs is made robust against short circuit currents for a limited amount of time. The behaviour of the device is strongly dictated by the stray inductances during the short circuit condition. The current rising rate is being determined by the inductances in series with the collector and the emitter of the device and at the same time the inductances in series with the gate terminal is the one responsible for gate –emitter voltage overshoots. The gate-emitter voltage (V_{GE}) overshoots have a significant influence in the short circuit current through the device and consecutively the power dissipated given that the device is operating in saturation mode. Going by the above information, stray elements such as inductances will be considered in carrying out short circuit simulation. It has to be observed that considerable temperature rise takes place as a result of power dissipation within the device [44]–[47].

During short circuit events, three types of operation mode can be identified, they are: Short circuit type1 (hard switching failure (HSF)), short circuit type 2 (failure under load (FUL)) and short circuit type 3. In short circuit type 1 which will be later discussed in detail and carried out in this study because of its simplicity, the short circuit usually occurs before the device (IGBT) is switched on and the collector current increases from zero. In short circuit type 2 which is also known as fault under load (FUL) operation mode, short circuit failure occurs when the load is under nominal current and the collector current rises from the nominal current value [48]–[50]. Short circuit type 3 is the occurrence of a short circuit across the load during the conducting mode of the freewheeling diode and it has the same importance for the application of high power IGBTs as in the short circuit 2. In all cases, significant amount of power is dissipated within the device leading to a fast rise in temperature.

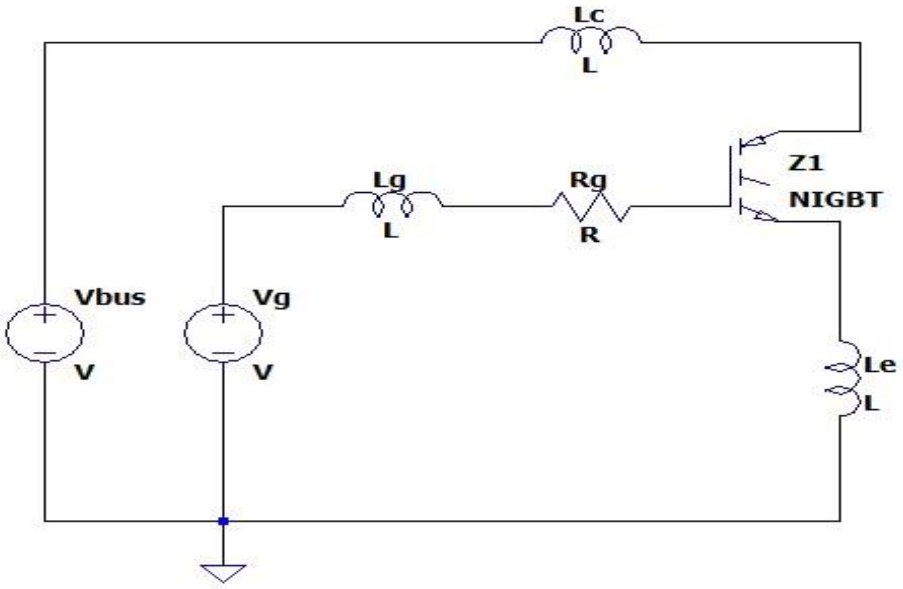


Figure 2.10: Short circuit simulation circuit with stray inductances

2.2.10 Short circuit type 1

The Figure 2.11 below show the waveform of short circuit type 1 reported by [51], [52]. The V_{CE} is high before turn-on and the current rises to 400A which is the value of the saturation current after short circuit turn-on. This value conforms to the saturation current at V_{GE} = 15V and defined in some datasheets [52]. The IGBT is capable of supporting high current and a high voltage concurrently during short circuit for some period of time and should be turned-off within a specified time, typically set at 10us or less to guarantee safe operation and to avert failures due to overheating. Owing to self-heating of the device, the short circuit current Isc decreases with time as can be seen in the fig.2.10 above. The inductive peak voltage is generated during short circuit turn-off. The criteria for the survival of the short circuit pulse is that within the defined safe operating area (SOA), the peak voltage should be lower than the rated voltage. In order to maintain this, it is required that short circuit current should be turned off with a limited di/dt. Generally, the gate driver requires a higher resistor to limit di/dt during turn-off in the event of short circuit. Utilizing an active clamping circuit on the gate driver, the voltage spike can also be controlled.

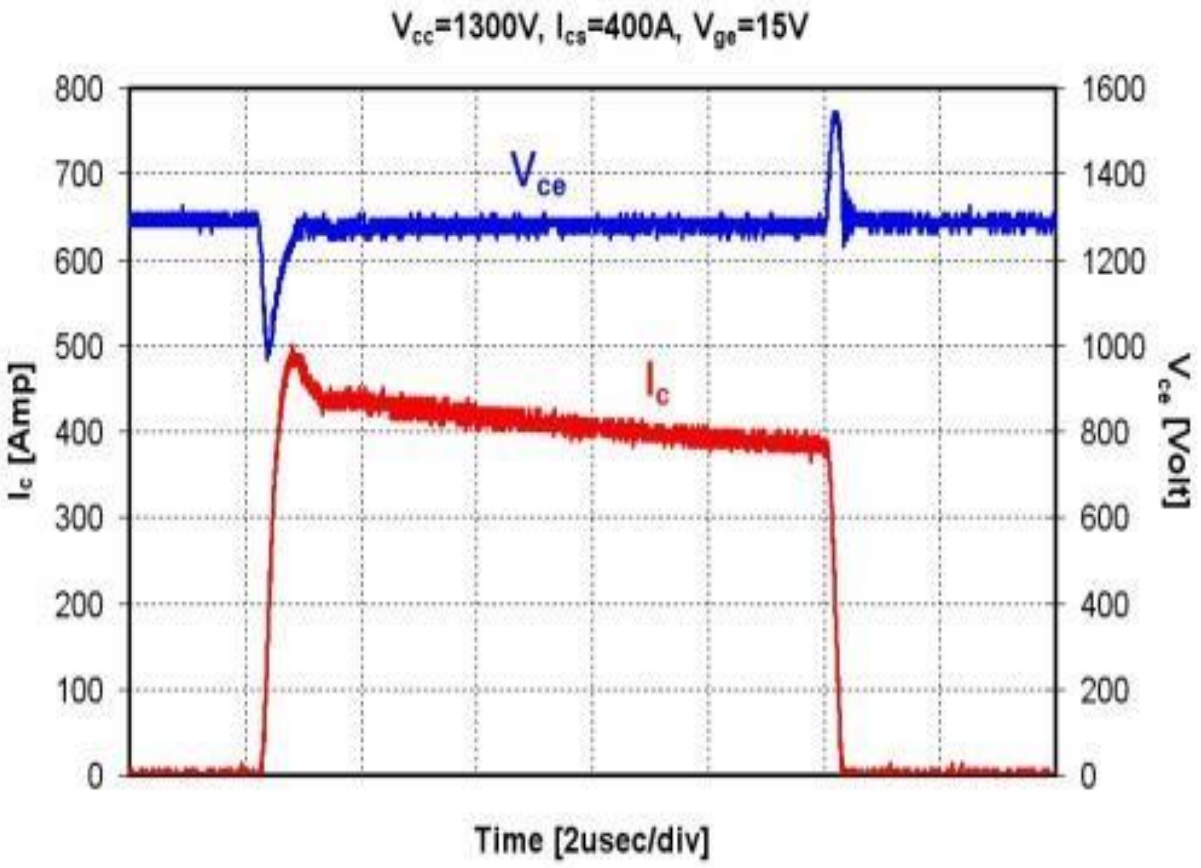


Figure 2.11. Short-circuit type 1 waveform. I_C=100A, V_{CE}= 1.7kV [51, 52]

2.2.11 Safe Operating Area (SOA)

The current – voltage circumference within which a power switching device can be safely operate without catastrophic failure is termed as a safe operating area (SOA). SOA for IGBT is defined as the maximum collector – emitter voltage V_{CE} and collector current I_C under which the operation of the IGBT must be limited to safeguard it from destruction. Types of SOA operation in IGBT includes the following: Forward- biased safe operating area (FBSOA), Reverse- biased safe (RBSOA) as well as short- circuit safe operating area (SCSOA).

2.2.12 Forward – Biased Safe Operating Area (FBSOA)

For applications involving inductive loads, the FBSOA is very necessary. The highest voltage the device can withstand without failure when the collector current is saturated is termed as the FBSOA. In this condition, a high collector voltage is supported by the movement of electrons and holes within the drift region. In the drift region, the electron and hole concentrations are related to the equivalent current densities by the equation below [11], [39]:

$$n = \frac{J_n}{qV_{sat,n}} \quad (2.1)$$

$$p = \frac{J_p}{qV_{sat,p}} \tag{2.2}$$

where $V_{sat,\ n}$ and $V_{sat,\ p}$ represent the saturated drift velocities for electrons and holes respectively. Therefore, the total positive charge in the drift region is written as:

$$N^+ = N_D + \frac{J_p}{qV_{sat,p}} - \frac{J_n}{qV_{sat,n}} \tag{2.3}$$

Electric field distribution in the drift region is being determined by this charge. The drift region charge is equal to N-drift doping concentration during the steady – state forward blocking condition. The total charge is exceedingly large in FBSOA owing to the fact that the hole current density is considerably higher than the electron current density. In the FBSOA, the breakdown voltage limit is written as

$$BV_{SOA} = \frac{5.34\ x\ 10^{13}}{(N^+)^{0.75}} \tag{2.4}$$

In reality, the BV_{SOA} is known as the avalanche breakdown voltage.

2.2.13 Reverse – Biased Safe Operating Area (SOA)

During the turn – off transient period, the SOA show the safe operating area of the device. The device during the turn – off condition is left with high voltage and hole current movement. Usually during turn – off, the snubber circuit is used for safe operation of the device. Reducing the current gain of the PNP transistor in IGBT is capable of increasing its RBSOA. During device turn – off, the maximum value of V_{CE} is the addition of the bus voltage and the product of $L_s \frac{dI_c}{d_t}$ where L_s is the stray inductance in the power circuit. In the reverse-biased condition, the current transport in the drift region takes place solely through the holes for an n-channel IGBT. This is because as the gate bias is zero or negative, the MOS-channel is cut – off and there is no electron current flow. Thus, the charge carrier in the drift region is due to the presence of holes which leads to the increase in the electric field at the junction between the p – base and N-drift region. The total charge in the space charge region at RBSOA condition is given by the equation below [11], [39]:

$$N^+ = N_D + \frac{J_c}{qV_{sat,p}} \tag{2.5}$$

And J_c = total collector current. Therefore, the avalanche breakdown voltage for RBSOA is given by:

$$BV_{SOA} = 5.34\ x\ 10^{13} \left(\frac{J_c}{q_{V_{sat,p}}} \right) \quad (2.6)$$

2.2.14 Short Circuit Safe Operating Area (SCSOA)

The area of safe operation for a device under fault condition is known as SCSOA [39]. A very important requirement of a power switching device is its ability to turn – off safely in the event of short circuit fault. During the current overload condition, there will be fast rise of collector current until it rises beyond that which the device can withstand with the applied gate voltage. The key sustainability of a power device in the event of fault is to limit the current amplitude to a tolerable limit for some time until the fault is detected by the control circuit which turns – off the device. The gate voltage and transconductance limit the current in IGBT during the short circuit condition. The short circuit current is capable of reaching up to 10 times the device rated current. The SCSOA can be widen by lowering the transconductance and density of hole current. The IGBT with high short circuit ruggedness have higher voltage drop compared with the ones with low short circuit withstand capability [43].

2.2.15 Dynamic Switching Characteristics of IGBT

Inductive load like electric motor which converts electrical energy into mechanical energy find its usefulness in various applications such as water pumping, mixers, fans, cranes etc. IGBT find its major application in inductive load switching. It is therefore necessary to bring into discussion the dynamic switching operation of the IGBT under inductive loading conditions. During the device (IGBT) switching involving inductive load, a typical clamped inductive load circuit as shown in Figure 2.12 below is used. The sections that follow explains the transient behaviour during clamped inductive switching with the aid of Figure 2.13.

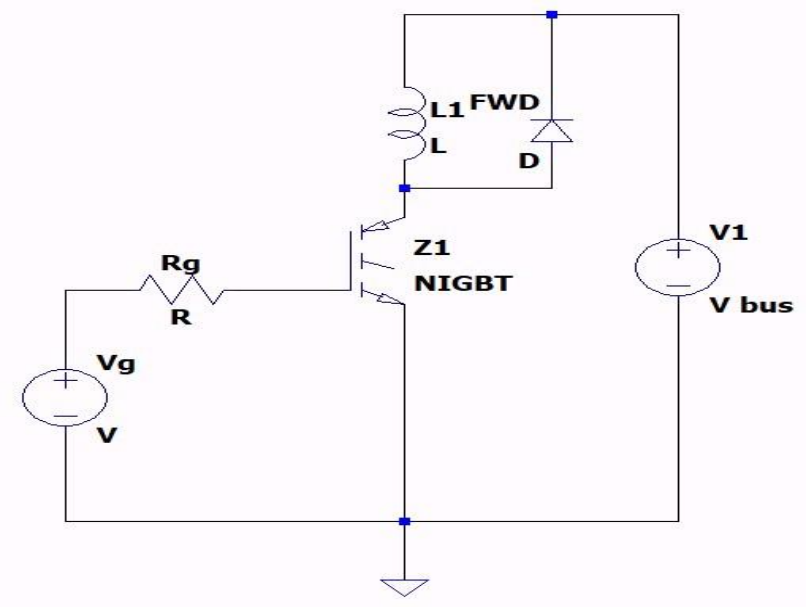


Figure 2.12: IGBT Inductive Switching Circuit

2.2.16 IGBT Turn – on

Applying a positive voltage to the gate which is above the threshold voltage of the MOS – channel inverts the surface of the p – base region under the gate hence forming an n-type channel which allows the flow of electron current into the drift region. As a consequence of the injected electron current into the drift region (base of the vertical PNP transistor), the junction between the P+ substrate and the N-drift region forward biases upon application of positive voltage to the collector terminal. This therefore leads to the injection of minority carrier (hole) from the p+ collector to the N-drift region. The section below explains the turn on process in detail [39].

Period 'a': During period 'a' as shown in the Fig.2.13 below, there is no current flow, and the device (IGBT) maintains the full bus voltage.

Period 'b': In this region, the gate capacitance which is the summation of the gate – emitter capacitance (C_{ge}) and miller capacitance (C_{gc}) charges as result of the application of the gate voltage (V_g). As the gate capacitance is being charged, the gate – emitter voltage (V_{GE}) therefore rises to its threshold voltage ($V_{G(th)}$). The charging rate of the gate capacitance is governed by the value of the gate resistance and the magnitude of the gate input capacitance. The moment the gate voltage reaches its threshold voltage value, current start rising through the device.

Period 'c': The gate voltage keeps rising at an exponential amount which is governed by the time constant $R_g * C_{ge}$ given by:

$$V_{(t)} = V_{gmax}\,[1 - e^{(t/\tau)}] \qquad (2.7)$$

Where $\tau = R_g C_{iss}$

Following the exponential increase of gate voltage, the collector current begins to rise and its rising rate is being determined by the rate at which the gate capacitance charges and thus the gate voltage.

$$I_c = g_m\,(V_{GE} - V_{th}) \tag{2.8}$$

When the collector current (I_C) has risen to its peak value, the collector voltage start decreasing as shown in the fig. below (period 'c'), the gate voltage (V_g) remain constant at this time notwithstanding the fact that current is still flowing into the gate. The miller capacitance (C_{gc}) is now being charged by the gate current (I_g) and increase as a result of decreasing collector voltage. The equation 2.9 below governs the rate at which the collector voltage falls.

$$\frac{dV_{ce}}{dt} = \frac{I_g}{C_{gc}} \tag{2.9}$$

Period 'd': In period 'd', the gate – emitter voltage (V_{GE}) increases again to V_{GG} with $R_g(C_{ge} + C_{gc})$ as time constant. The total sum of the turn – on time depends on factors which includes gate current, collector voltage and gate capacitance. The time comprises of: The initial delay time during gate charging, $T_{dela(on)}$ which is generally explained in the datasheets as the time taken between 10 % of gate voltage and 10 % of the final collector current. The rise time, T_r, which is explained as the time it took collector current to rise from 10 % to 90 %.
Finally, the time it takes the collector voltage to fall to its steady – state value.

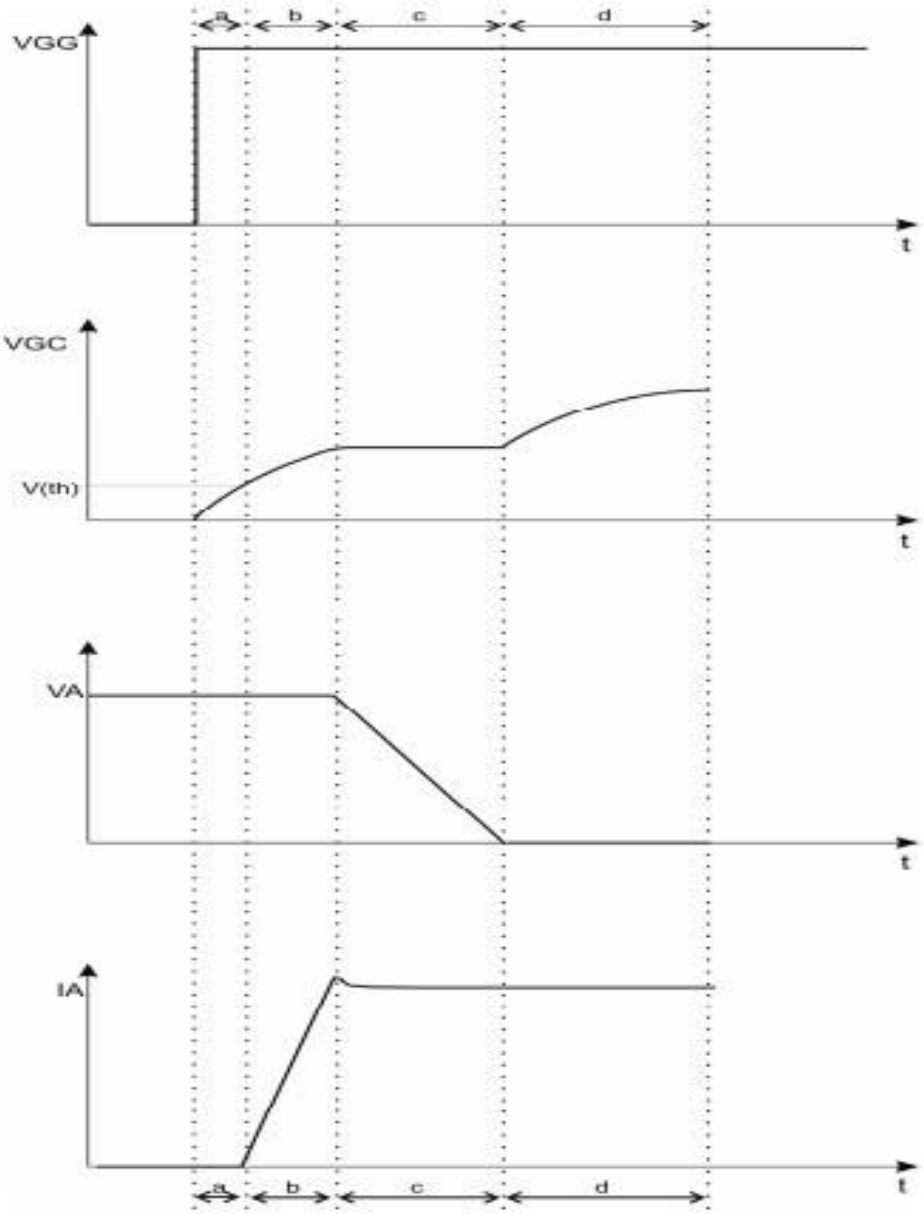


Figure 2.13: Turn – on IGBT switching waveforms.

2.2.17 IGBT Turn – off.

As the gate voltage falls below the threshold voltage by either shorting the gate to the emitter or applying a negative bias to the gate, the inversion layer ceases to be maintained thereby blocking the supply of electron current to the drift region. The turn – off process begins at this point which is illustrated in Figure 2.14 below [39].

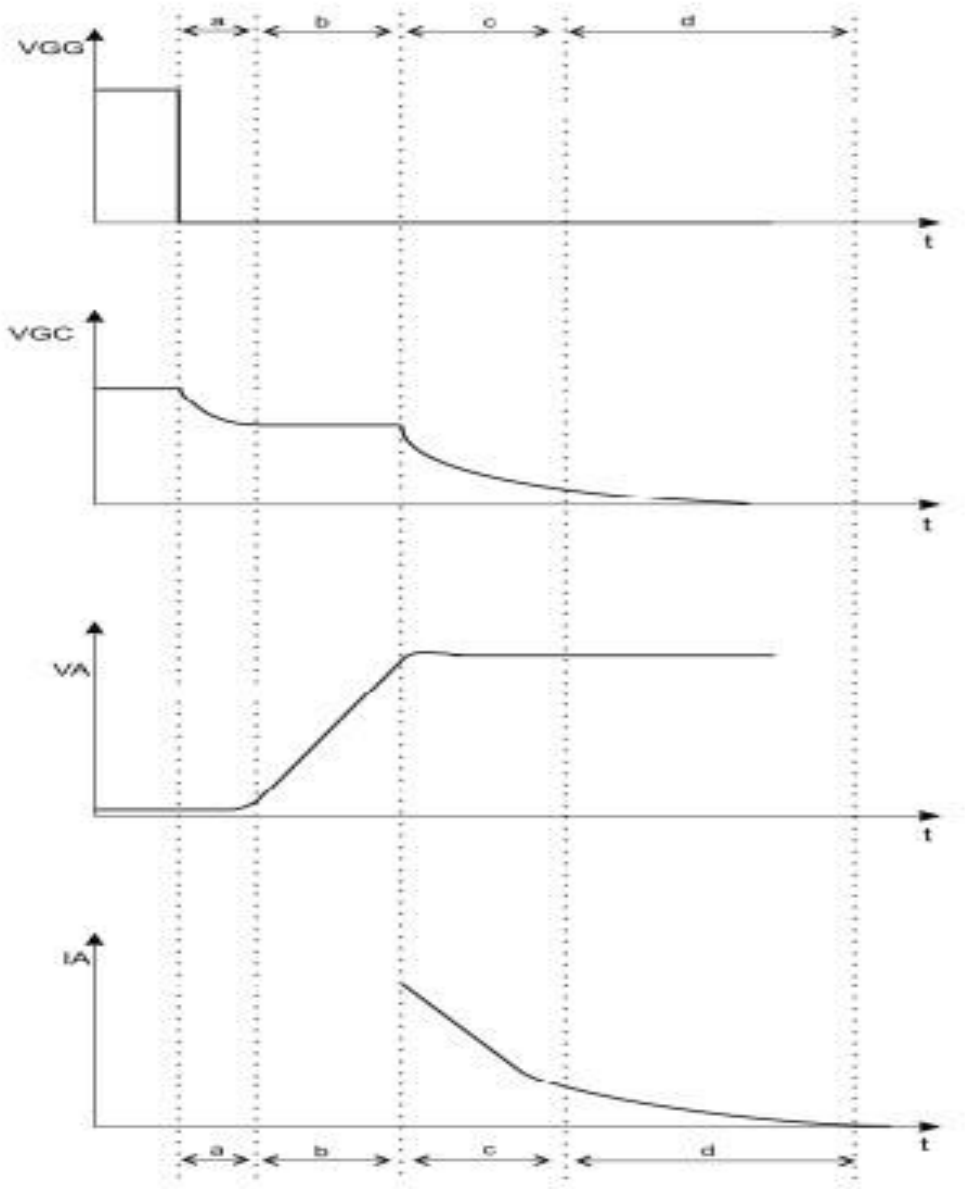


Figure 2.14: Turn – off IGBT switching waveforms.

Period 'a': It is obvious in this period that the V_{GC} starts decreasing as the gate capacitance is being discharged. The exponential discharge rate is governed by the equation below:

$$V_{g(t)} = V_{gmax} e^{-(\frac{t}{\tau})} \quad (2.10)$$

Period 'b': As the miller capacitance is being discharged at an amount determined by the constant negative gate current, the collector voltage starts rising.

$$I_g = \frac{\left(V_{th} + \frac{I_c}{G_m}\right)}{R_g} \quad (2.11)$$

Period 'c': At period c, the voltage reaches its peak value, and the collector current starts to fall due to abrupt fall in electron current as the MOS channel has been cut – off.

Period 'd': As the MOS channel is being cut – off, hole current keeps being injected into the drift region from the p+ collector leading to a current tail as the surplus carriers (electrons and holes) in the N-drift region start recombining and the current starts decaying resulting to a current decay. Due to a large number of carriers trapped in the drift region, the turn – off of the IGBT is much slower compared to a MOSFET. The trapped carriers can only be removed via recombination which causes a slow current tail.

In NPT-IGBT technology, the current tail will be slower to decay because NPT has a longer carrier lifetime. However, the long lifetime has an advantage of low on – state voltage and thus there is a trade – off between switching time and forward voltage drop.

2.3 TCAD Sentaurus Software

For modelling and characterization of IGBT under various conditions, Sentaurus software will be utilized. Sentaurus software was provided by Synopsys, and it is a TCAD (Technology Computer Aided Design) targeted towards carrying out semiconductor physics finite element (FEM) simulations. Sentaurus environment is made up of various programs with each program carrying out a specific task. Presented below is an explanation of each of the Sentaurus program and the task that is being performed by them.

- Sentaurus Structure Editor: This is a tool that is used to create 2 or 3-dimensional device structure using either graphical user interface (GUI) or scripting. In this section of the Sentaurus program, the doping profiles are defined and in carrying out the finite element (FEM) simulation, meshing of the semiconductor device is equally determined here. After meshing, the TDR grid file will be generated which has the required information about the geometrical properties, doping concentration as well as device meshing [53].
- Sentaurus Device: After generating the semiconductor device structure in the sentaurus structure editor. Sentaurus Device is then used for simulating the electrical characteristics of the generated device structure. As shown in the fig.x below, this simulation (Sentaurus Device) can be performed under 3 different conditions such as single device, single device with external circuit or multiple devices connected to auxiliary circuit elements [54].

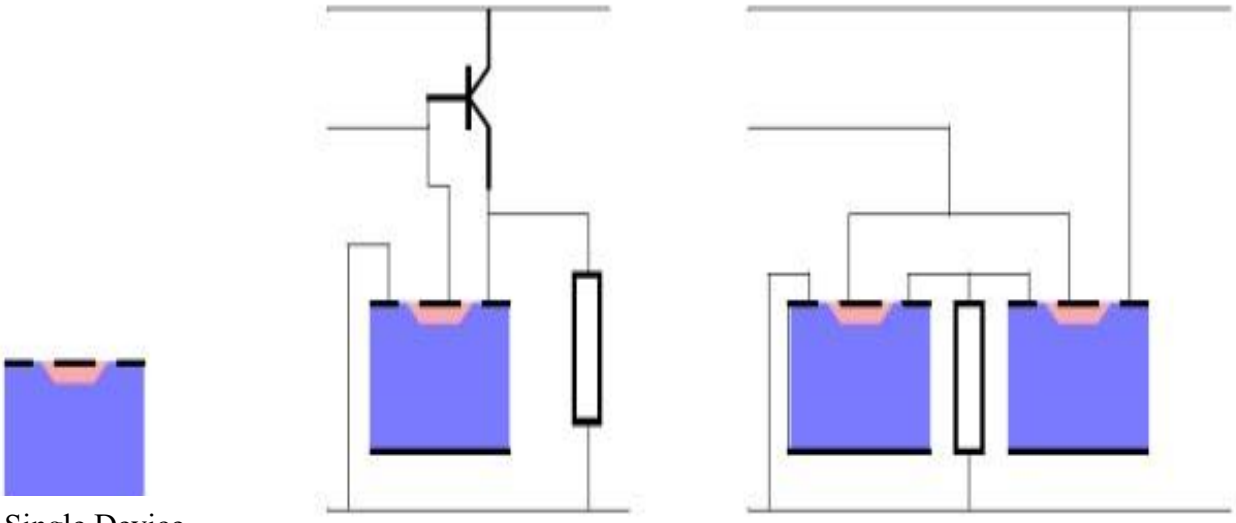


Figure 2.15: Types of Circuit Simulation within the Sentaurus Device

In determining the device currents, voltages, and the device internal characteristics, the device equation must be solved. In doing this, a large-scale set of models for device physics (drift diffusion, thermodynamic and hydrodynamic models) are provided.

- Sentaurus Visual and Inspect: The data which have been simulated by the Sentaurus Device can be visualized in the Sentaurus Visual and Inspect. Visual tools allow plotting of the desired characteristics alongside a device cross-section [55].
- Sentaurus Workbench: Sentaurus Workbench is made up of a graphical environment in which the tools discussed above are shown and executed. With this tool, all the information regarding the simulated device is being visualized by the user. In as much as TCAD Sentaurus has many other programs which includes simulating the manufacturing process for a semiconductor device, analysis of its optical properties and so on, it is only the above discussed tools that have been used in this thesis.

CHAPTER THREE

METHODOLOGY

3.1 Design of 1.2kV FS-Trench IGBT and its Electrical Characteristics

In this work, 1.2kV Trench IGBT is considered due to its outstanding features such as lowered on – state and switching losses thereby offering higher system efficiency. It is necessary to find the suitable combinations of the doping concentration of the N-drift along with its width to the point that the device would be able to support 1.2kV. After several iterations with the parameters and doping profile of the low voltage device example available in the TCAD Sentaurus software, the optimum width of the device that would comfortably support 1.2kV without failure initialization is 110um. The Table 3.1 and 3.2 present the structural parameters of the device and the doping profile at each of the region.

Table 3.1: Device structural parameters and their dimensions

S/N	Parameters	Symbol	Dimension (um)
1	Cell width	W	30
2	Trench width	W_T	1.0
3	Trench depth	D_T	4.5
4	Mesa width	S	3.0
5	n+/p+ depth	D_{pn}	0.25
6	n+ length	L_{n+}	1.0
7	p+ length	L_{p+}	1.0
7	p-base depth	D_{pb}	2.0
8	Gate oxide thickness	T_{ox}	0.1
9	Gate voltage	V_G(V)	15

Table 3.2: Peak doping profile for the designed device

S/N	Region	Doping Concentration (cm^{-3})
1	n^+/p^+	$1x10^{20}$
2	p-base	$2x10^{17}$
3	n-Drift	$5x10^{13}$
4	n-Buffer	$2x10^{16}$
5	p+ Collector	$3x10^{17}$

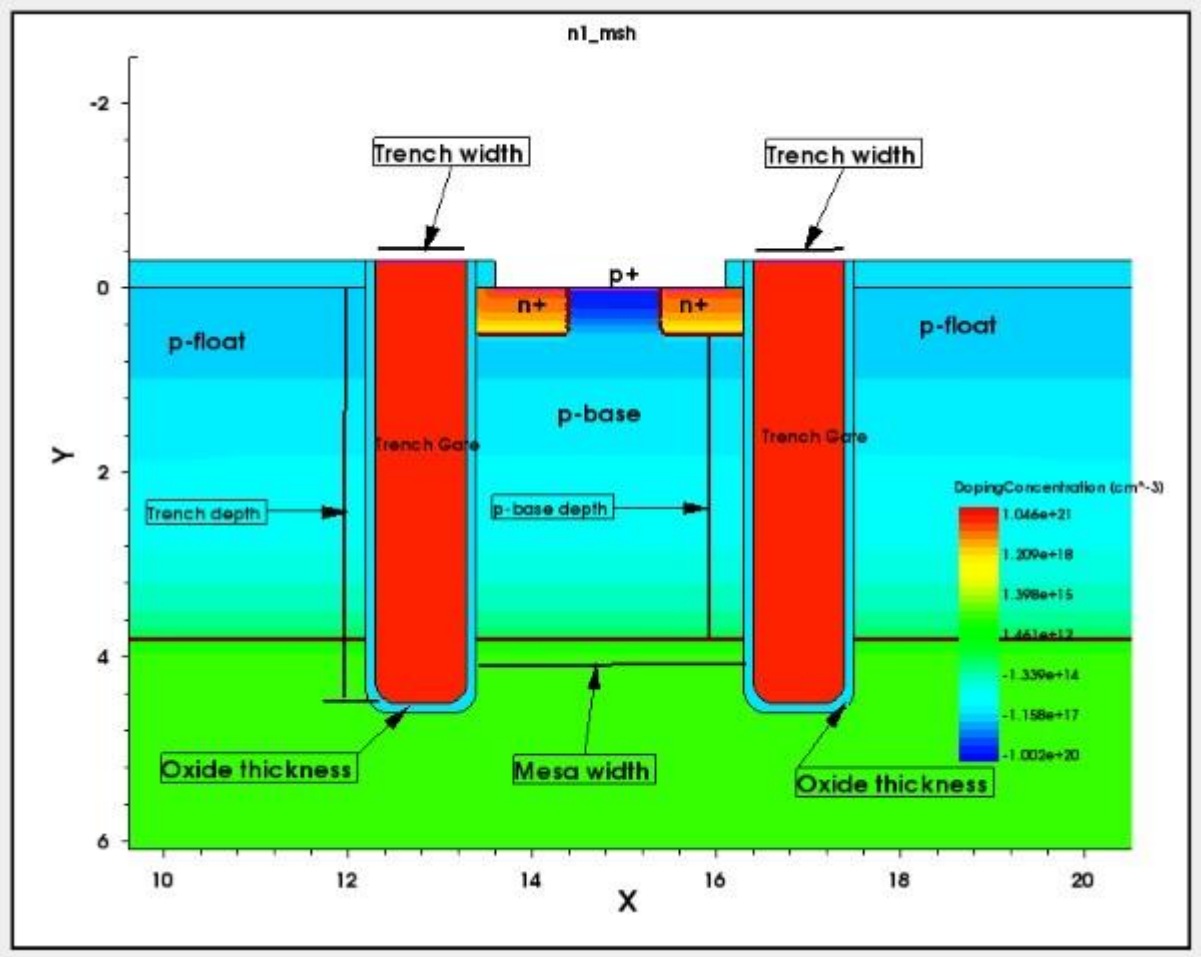


Fig. 3.1 (a): Zoomed structure of emitter region of the conventional TIGBT, k=1

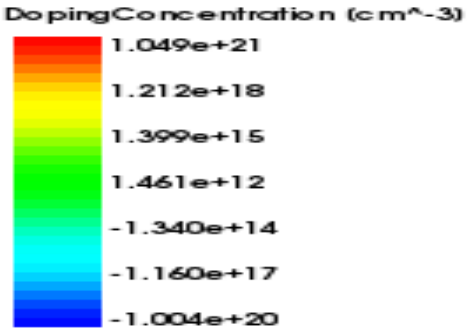


Fig.3.1(b): Enlarged view of the legend.

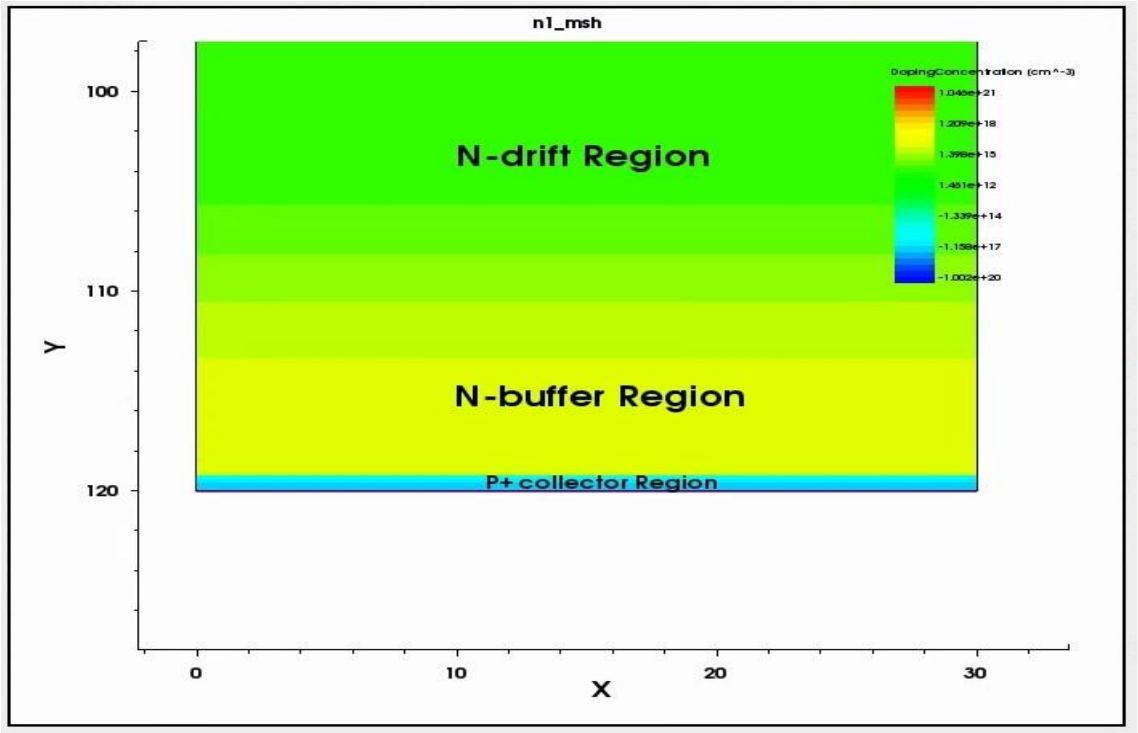


Figure 3.1 (c): Collector Region of the conventional TIGBT, k=1

Figure 3.1(a) show the zoomed structure of the emitter region of a conventional or a commercially available Trench IGBT which has a trench depth of 4.5um, $p_{\text{-base}}$ depth of 2um, mesa width of 3um and a cell pitch of 30um. The gate oxide thickness was kept constant at 0.1um while the p-base concentration was varied until a threshold voltage of about 5.3V was achieved. The threshold voltage V_{th} was the gate voltage value at which current Ic started to flow from the collector to emitter of the device when collector voltage is applied. Figure 3.1(b) is a display of the magnified view of the legend whereas the fig.3.1(c) shows the collector

region of the conventional device and it has part of the n-drift region, N-buffer region, p+ collector region as well as the collector electrode.

3.1.1 Mechanism of Operation of the Device

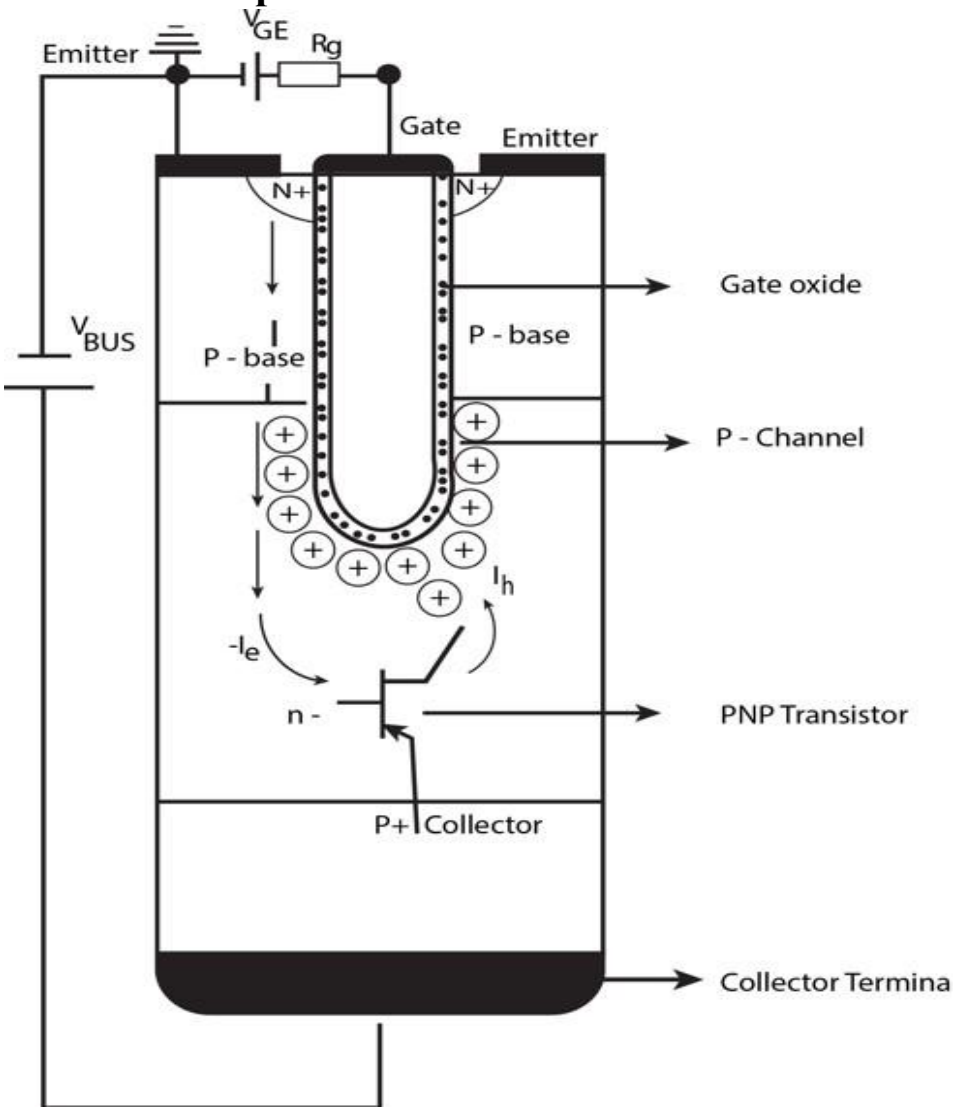


Figure 3.2: Schematic diagram showing device operation and movement of carriers.

When the gate voltage application is sufficient to invert the MOS-channel, then an n-channel forms and electron current begins to flow from the n+ emitter to the n-drift region which is the base of the vertical PNP transistor as can be seen in the Fig. 3.2 above. The biasing of the base of the vertical PNP transistor by the electron current leads to the forward biasing of the p+ collector/n-drift junction leading to injection of hole current from the p+ collector to the drift region. As a result of high injection of hole current into the drift region, conductivity modulation improves thereby increasing the conductivity of the drift region [11]. IGBTs can be

used in high voltage applications due to conductivity modulation which lowers the drift region resistance.

The turn-off process starts when the gate voltage falls lower than the threshold voltage due to the application of negative bias to the gate. Under this condition, the flow of electron current into the drift region is blocked as the inversion layer is no longer maintained. Due to the termination of electron current through the MOS-channel, the collector current decreases speedily and then decrease slowly as the hole carrier density decays as a result of recombination. However, due to high density of hole carriers injected into the drift region during forward conduction, the turn-off process takes time to complete [11].

3.1.2 Electrical Characteristics of the designed 1.2kV FS-TIGBT Device

3.1.2.1 Breakdown Characteristics

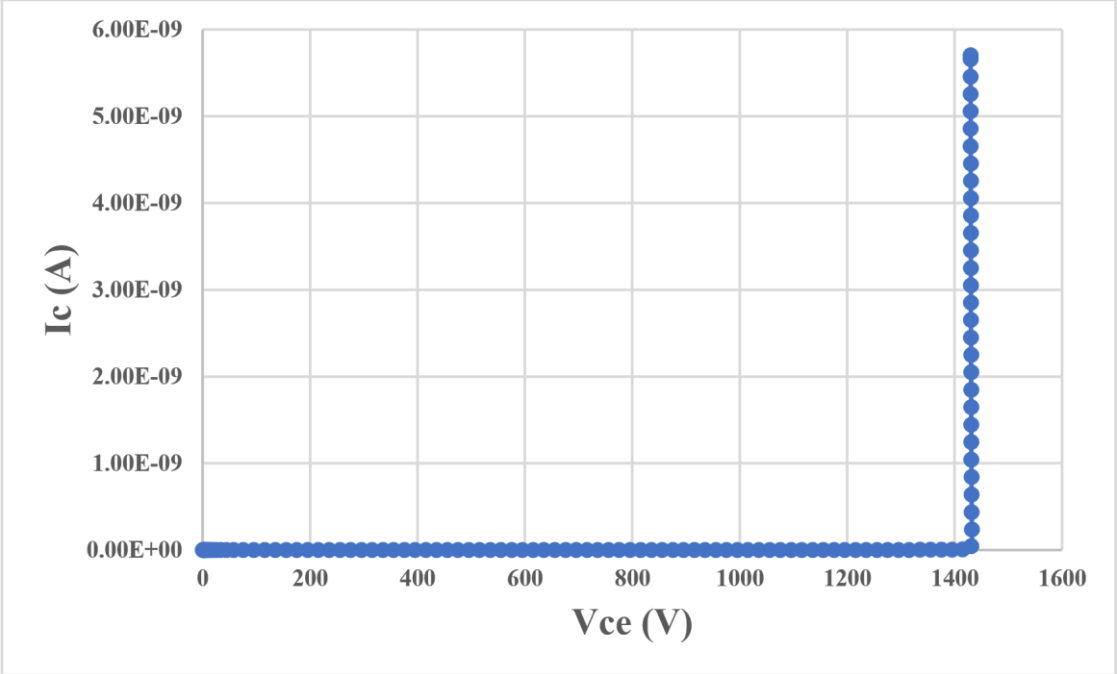


Figure 3.3: Breakdown characteristics during the off state, V_{CE}=1430V, Tj=300K.

Introducing a negative bias at the gate terminal and a positive voltage at the collector, reverse biases the junction between the p-base and n-drift region, thereby supporting the rated voltage by the depletion region which extend towards the n-drift region. The depletion layer reaches through the lightly doped area of the drift region at a collector bias given by [43]:

$$V_{RT} = \frac{qN_D}{2\varepsilon_s} WN^2 \tag{3.1}$$

Where WN is the width of the lightly doped area of the drift region.

Owing to the presence of the n-buffer region in the IGBT structure, which is asymmetric, voltage can continue to be supported by the device after the depletion region reaches through the lightly doped area of the drift region. Thus, the electric field distribution assumes a trapezoidal shape which is much like punch through structure. The n-drift region doping concentration as well as its width are the two main parameters that determine the forward blocking capability of an IGBT. The n-drift doping concentration of $5x10^{13}cm^{-3}$ and thickness of 110um are capable of supporting the target voltage of 1.2 kV during the blocking state.

The leakage current is due to space-charge generation within the depletion region. During the forward blocking mode, the space – charge generation current is being amplified by the gain of the bipolar transistor (PNP).

$$J_L = \frac{J_{SCG}}{(1-\alpha_{PNP})} \tag{3.2}$$

$$J_{SCG} = \frac{qW_D n_i}{\tau_{SC}} = \frac{n_i}{\tau_{SC}}\sqrt{\frac{2q\varepsilon_s V_c}{N_D}} \tag{3.3}$$

Where J_L is the leakage current density, J_{SCG} is space charge generation current density, α_{PNP} is the current gain of the PNP transistor, N_D is the doping concentration of the n-drift region and τ_{SC} is the space charge carrier lifetime.

The space charge generation current increases with collector voltage according to the above equation 3.3. Figure 3.3 above show the abrupt rise of the leakage current at the breakdown voltage. The breakdown voltage is significantly higher than the rated blocking voltage thus, allowing the device to operate up to 1.2kV.

Punch-through breakdown arises when the depletion layer penetrates the emitter contact, leading to injection of minority carriers (holes) from the emitter towards the collector. To prevent punch-through breakdown, the doping concentration of the n-buffer region must be made higher. This is also necessary to avoid reach – through of the electric field to the p^+ collector region, reduction of the emitter injection efficiency is necessary in order to increase the blocking voltage. This can be achieved by applying a higher doping concentration at the n-buffer region.

3.1.3 Electric Field Distribution at Breakdown (Vce = 1430V)

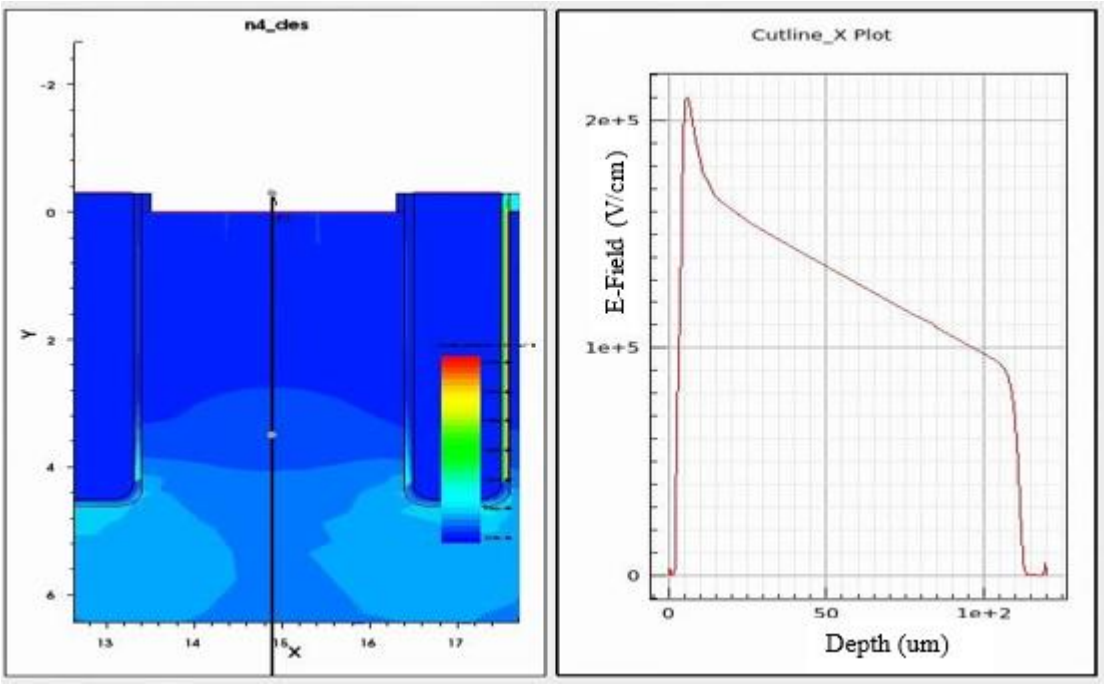


Figure 3.4: Cutline of Electric field distribution at breakdown (V_{CE} = 1430V)

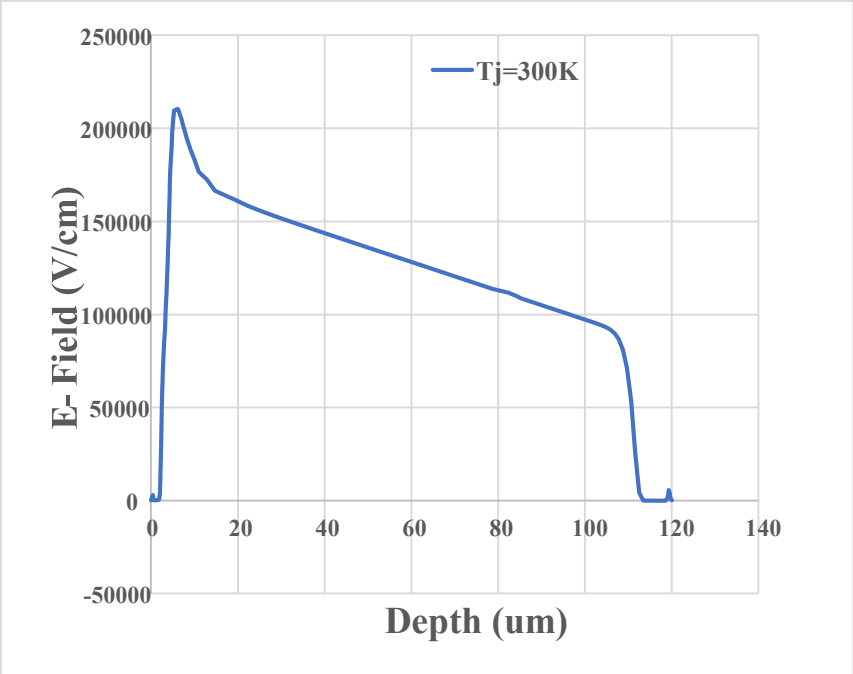


Figure 3.5: Electric field distribution at breakdown (V_{CE} = 1430V) for fig.3.4 above

Figures 3.4 and 3.5 showed the electric field distribution across the vertical path of the device at the rated V_{CE} voltage of 1.2kV. The electric field starts from the reverse- biased junction between the p-base and n-drift region (emitter side) and degenerate downward and ends at the n-buffer region, thereby assuming a trapezoidal shape just like the punch-through device. The maximum electric field occurs at the junction between the p-base and the n-drift region.

3.1.3.1 Input Characteristics

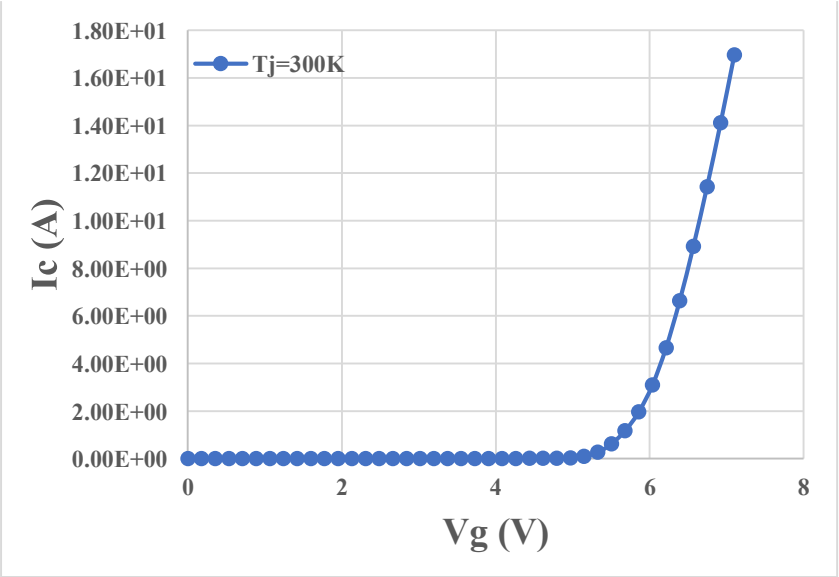


Figure 3.6: Transfer Characteristics, V_{th} = 5.3V

Figure 3.6 shows a plot of transfer characteristics (i.e. collector current I_C vs gate emitter voltage V_{GE}). It shows that the device remains in the off state until the gate emitter voltage (V_{GE}) reaches a threshold voltage of 5.3V. As the gate voltage V_{GE} is greater than its threshold value of 5.3V, the device turns on. Given the equation for the threshold voltage as [43].

$$V_{th} = \varphi_{MS} + \frac{2kT}{q} ln \frac{N_A}{n_i} + \frac{t_{ox}\sqrt{4\varepsilon_O \varepsilon_S kT N_A \ln \frac{N_A}{n_i}}}{\varepsilon_o \varepsilon_{ox}} \quad (3.4)$$

Where φ_{MS} is the work function between the metal and semiconductor. N_A is the acceptor concentration of the p-base region, n_i is the intrinsic carrier concentration. According to the threshold voltage equation under specific temperature condition, the threshold voltage is highly dependent on the p-base doping concentration and as well as the oxide thickness and tend to increase with the increase of both parameters.

3.1.4 Impact of p-base doping concentration on the threshold voltage

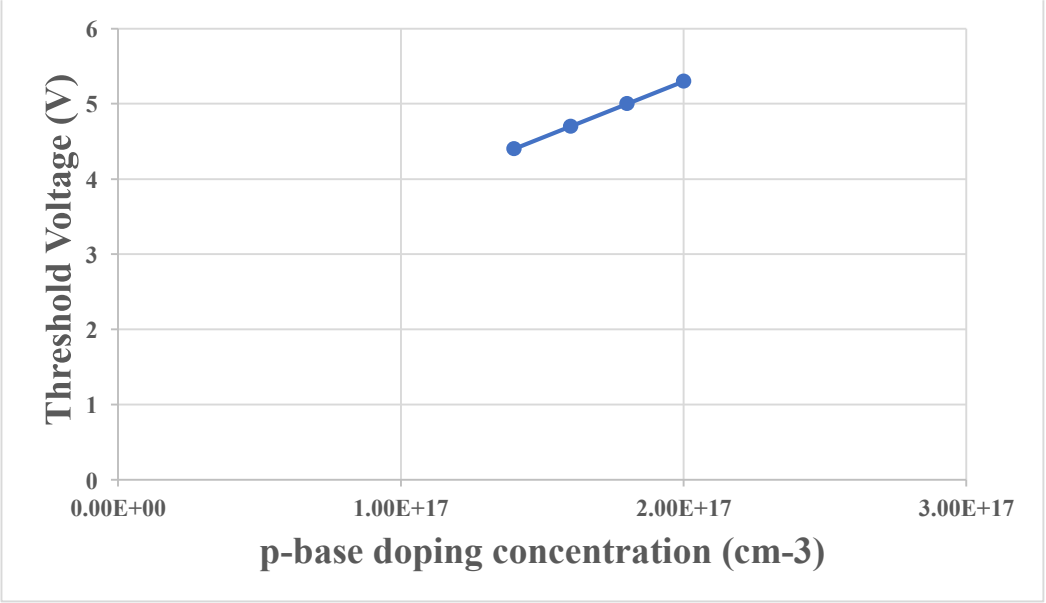


Figure 3.7: Impact of p-base doping concentration on the threshold voltage, @Tj=300K

In Figure 3.7, the impact of p-base doping concentration on threshold voltage is shown. The above figure shows a linear relationship between p-base doping variation and threshold voltage. Increasing the doping concentration of the p-base increases the majority carrier concentration of the channel. This means that more gate voltage will be required for channel inversion to be created, thus increasing the threshold voltage.

3.1.4.1 I-V Characteristics

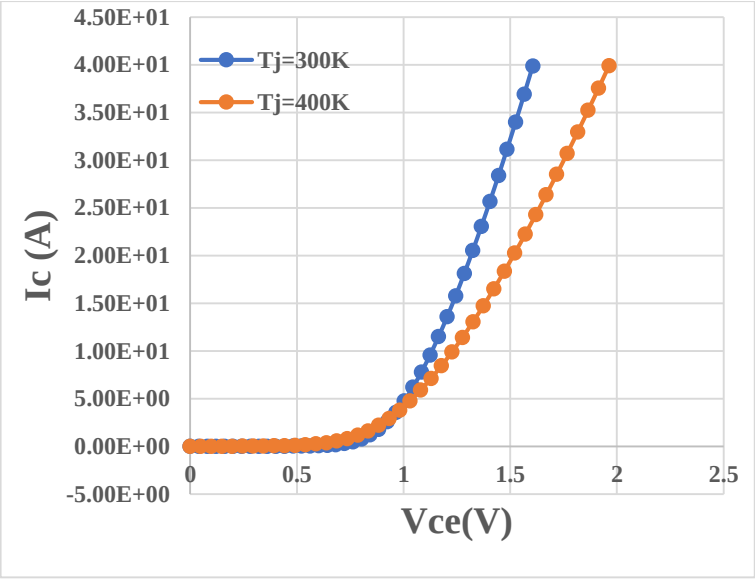


Figure 3.8: I-V Characteristics, Vg =15V

Shown in figure 3.8 is the I-V characteristics of the device simulated at both room and elevated temperature**s.** As can be seen, the device turns on and current start flowing when the gate emitter voltage (V_{GE}) exceeds the threshold voltage of the MOS-channel and the collector-emitter forward biased voltage is greater than 0.7V. As the $V_{GE} > V_{th}$, an n-channel is created for electron current to flow to the drift region (base of the PNP transistor). This follows an injection of holes from the p-collector to the drift region as the collector – emitter forward biased voltage is 0.7V. As a consequence of carriers (holes and electrons) injection into the drift region, a process known as conductivity modulation commences by which the resistance of the drift region is lowered significantly below the bulk resistance [11]. Hence, a much-lowered forward voltage drop is created across the device. Owing to the modulated conductivity within the drift region, IGBT has a remarkably reduced on-state voltage drop and increased current density.

The current saturation occurs when the voltage across the MOS-channel is greater than ($V_{GE} – V_{TH}$). The saturation voltage $V_{ce(sat)}$ is made up of summation of voltage drop across the MOS channel, N-drift region, and the potential barrier of the p+ collector / N-drift junction. The voltage drop across the MOS-channel and N-drift region are due to their resistances. The voltage drop at the N-drift region is usually very low due to high conductivity modulation caused by holes injected from the p+ collector. The saturation voltage $V_{ce(sat)}$ according to the figure 3.8 is 1.6V at room temperature of 300K and 1.9V at the elevated temperature of 400K. As temperature rises to 400K, the channel resistance increases and as a result, the voltage drop at the MOS channel increases. Thus, the saturation voltage $V_{ce(sat)}$ at the elevated temperature of 400K increases.

3.1.4.2 Current Saturation Characteristics

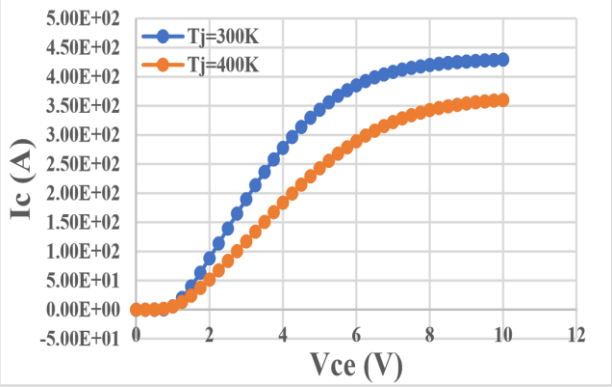


Figure 3.9: Current Saturation Characteristics, V_G=15V.

Figure 3.9 showed current saturation characteristics simulated at room temperature as well as high temperature. Collector current flows at the formation of MOSFET channel and collector emitter forward voltage drop exceeding 0.7V like in PiN diode. Current is saturated when the voltage across the MOSFET Channel is greater than ($V_{GE} - V_{th}$) and has an infinite output resistance [43]. The equation for obtaining the saturated collector current of the IGBT.

$$I_{C,Sat} = \frac{1}{(1-\alpha_{PNP})} \frac{\mu_{ns} C_{ox} Z}{2L_{CH}} (V_{GE} - V_{th})^2 \quad (3.5)$$

Where μ_n = surface mobility of electrons, C_{ox} = Gate- oxide capacitance per unit area, Z = Channel width, L_{CH} = channel length, V_{th} = threshold voltage and V_{GE} = applied gate voltage. Differentiating the $I_{C,\,Sat}$ with respect to V_{GE} yields transconductance at the active region.

$$\mathbf{g_{fe}} = \frac{\mathbf{1}}{\mathbf{(1-\alpha_{PNP})}} \frac{\mu_{ns} C_{ox} Z}{2L_{CH}} (V_{GE} - V_{th}) \quad (3.6)$$

As the PNP transistor current gain (α_{PNP}) is between 0.2 to 0.3, the IGBT's saturated collector current and transconductance are higher than that of the power MOSFET [43]. This is due to the absence of p+ collector region in MOSFET power device, in other word, MOSFET does not have a vertical PNP transistor. Looking at the current saturation characteristics, it is noticed that there is a significant lowering of the saturation current at high temperature.

This is because of the decrease of the carrier mobilities (electrons and holes) at high temperature.

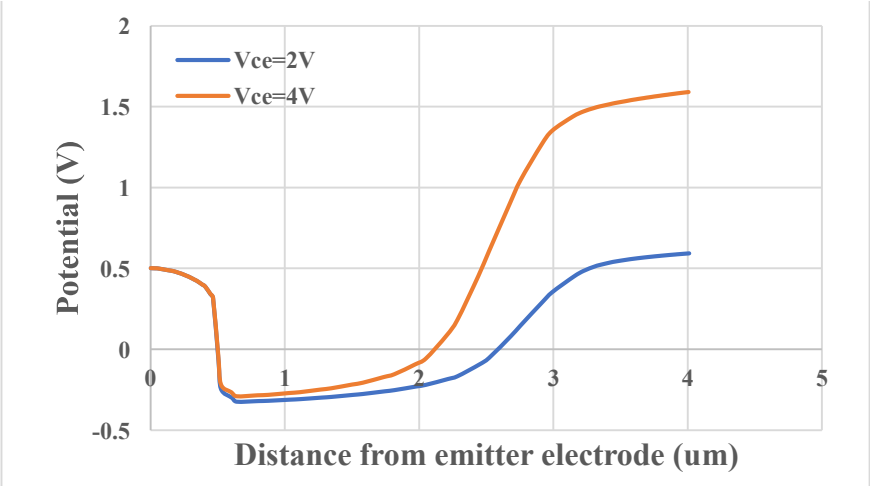


Figure 3.10: Potential distribution within the mesa region (n+/p_{base} junction) @ T_j=400K for conventional device k=1.

Figure 3.10 showed the potential distribution within the mesa region for the conventional device k=1. According to the figure, the potential barrier of the n+/p-$_{base}$ junction only slightly lowers with the increased collector voltage due to the width of the mesa region. This leads to current unsaturation as shown in Figure 3.9 above.

3.1.5 On-State Carrier Distribution

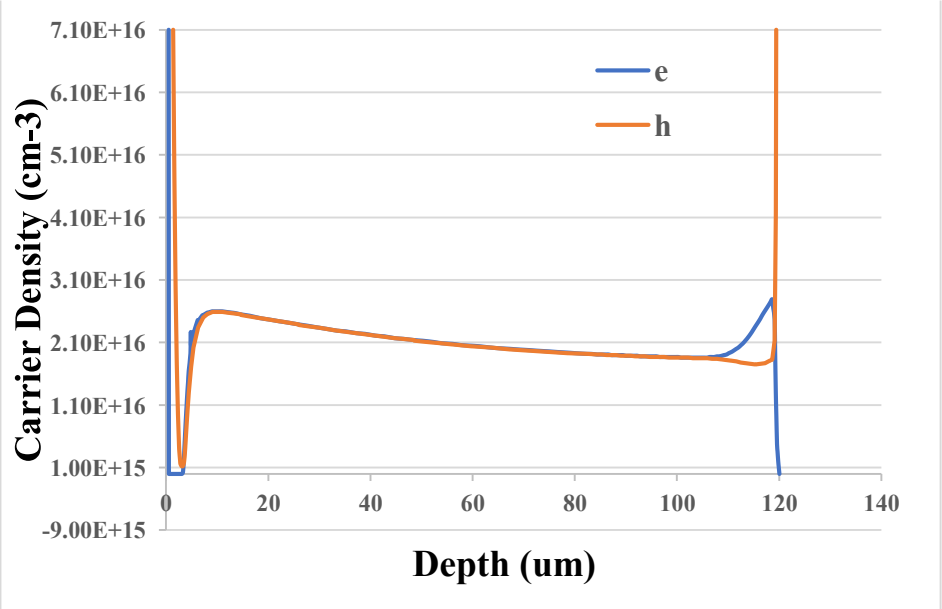


Figure 3.11: Carrier distribution in the N-drift at the rated current of 40A, T_j=300 K.

Shown in Fig. 3.11 is the carrier (electrons and holes) distribution within the device obtained in the on-state at the rated current of 40A. The TIGBT structure is an asymmetric type with an n-drift region consisting of a lightly doped ($5x10^{13}$ cm^{-3}) region and a width of 120um together with an n-buffer layer of width 10um and doping concentration of $1x10^{16}$ cm^{-3}. During the on state, holes diffuse to the lightly doped n-drift region through the n-buffer region whereas electrons diffuse to the p+ collector region. The doping concentration of the n-buffer determines the number of holes that are being injected into the n-drift region. Increasing the doping concentration of the n-buffer region reduces the hole injection efficiency into the n-drift region. Hence, delivering a lower injected hole density at the n-drift region. As a consequence of this, the on-state voltage drop is increased and at the same time lowering the turn-off switching losses as less holes are left to be recombine at turn-off. The concentration of the injected hole carrier at the n-buffer region is given by [43]:

$$P_{(xn)} = \frac{p_{0,NB} L_{P,NB} L_{n,P+}}{qD_{P,NB} p_{0,NB} L_{n,P+} + qD_{n,P+} n_{0,P+} L_{P,NB}} J_C + p_{0,NB} \qquad (3.7)$$

Where D_P, NB and D_n, p^+ are the diffusion coefficients for holes in the n-buffer layer and electrons in the p^+ collector region. po, $_{NB}$ and $n_{o,\,P+}$ are the minority carrier (holes and electrons) concentration in the n-buffer and p+ collector layers in equilibrium. Lp, $_{NB}$ and Ln, p+ are the minority carrier diffusion coefficient in the n-buffer and p^+ collector layers. The concentration of minority carrier (electrons) at the p+ collector is given by:

$$N_{(xn)} = \frac{n_{0,P+}L_{P,NB}L_{n,P+}}{qD_{P,NB}p_{0,NB}L_{n,P+}+qD_{n,P+}n_{0,P+}L_{P,NB}}J_C + n_{0,P+} \qquad (3.8)$$

3.1.6 Inductive Turn-off Switching

Given the inductive switching circuit in fig. 3.12 below, the simulated waveforms of turn-off behaviour of a 1.2kV field-stop (FS) TIGBT are shown in the figures below.

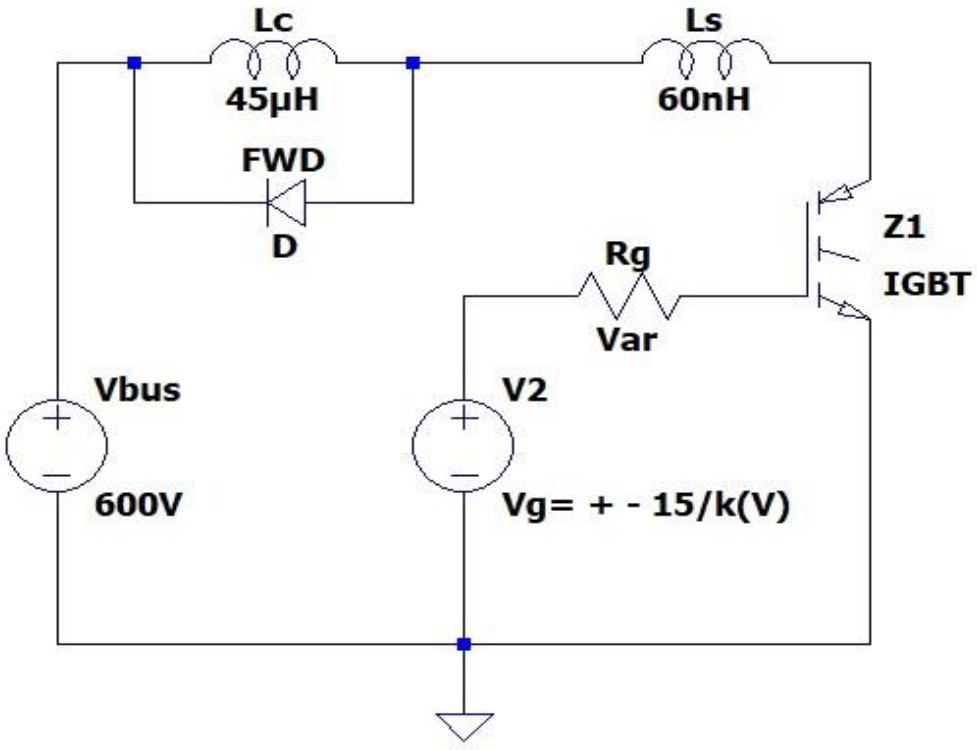


Figure 3.12: Inductive Switching Circuit Configuration

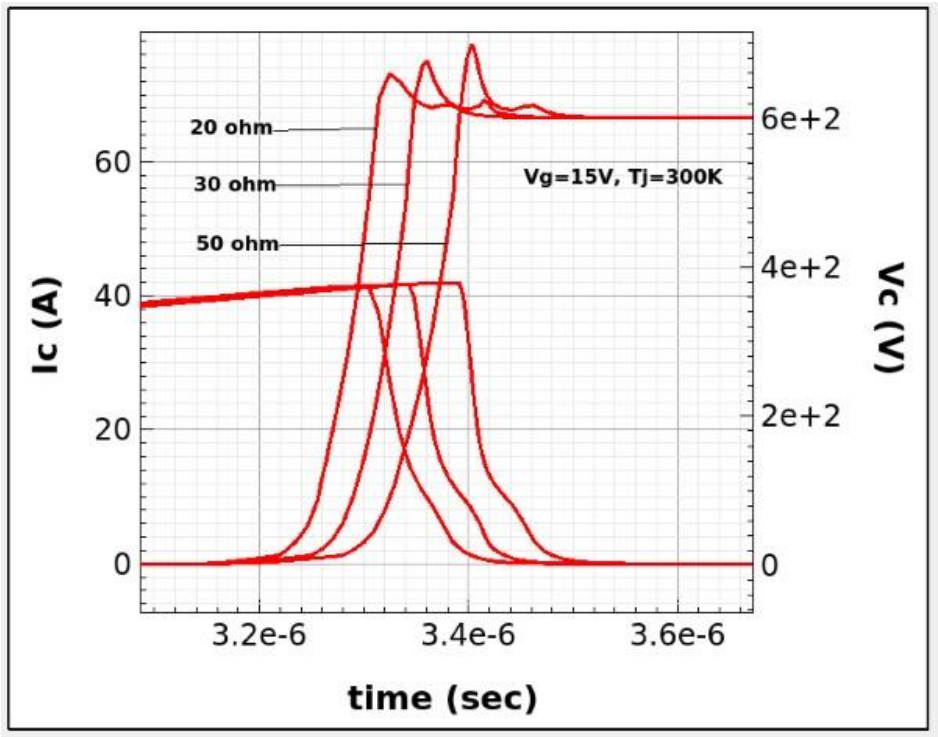


Figure 3.13: Turn-off switching waveform for the conventional FS-TIGBT at T_j=300 K, V_g=15V, V_{DC} =600 V, I_C = 40A, R_g = 20 Ω, 30 Ω & 50 Ω.

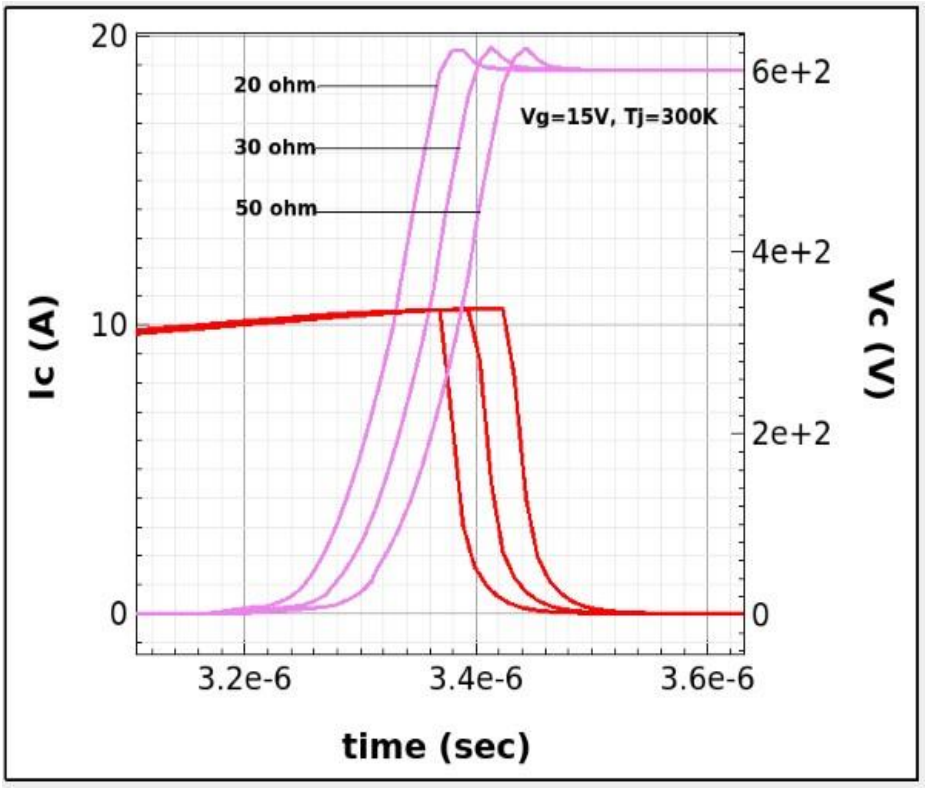


Figure 3.14: Turn-off switching waveform for the conventional FS-TIGBT at T_j=300 K, Vg=15 V, V_{DC} =600 V, I_C = 10A, R_g = 20 Ω, 30 Ω & 50 Ω.

Figure 3.13 and 3.14 showed the turn-off switching waveform for the conventional device. The parameters for the simulation are given in the circuit configuration shown in the Fig.3.12 above. As can be seen from the fig.3.13, dynamic avalanche occurred at the gate resistance R_g=20Ω due to lowering of dV/dt [56], [57]. This is because the excess holes which are stored in the device during turn-off are accumulated at the bottom of the trench gate during sudden rise in collector voltage at turn-off [58]. This led to a peak electric field strength which is greater than the critical electric field (E_c). Thus, more charges are being generated which lowers dV/dt due to dynamic avalanche [59]. In the other hand, as the load current is reduced to 10A, the dynamic avalanche vanishes as shown in fig.3.14 above. This shows that dynamic avalanche depends on current density among other factors.

The Fig.3.15 below show the turn-off switching losses as a function of gate resistance for the conventional device k=1. It is shown in the figure that the turn-off switching losses remained constant as the gate resistance increased up to 30 Ω and then the losses slightly increase as the gate resistance is above 30 Ω. This means that the turn – off switching losses depends on the gate resistance.

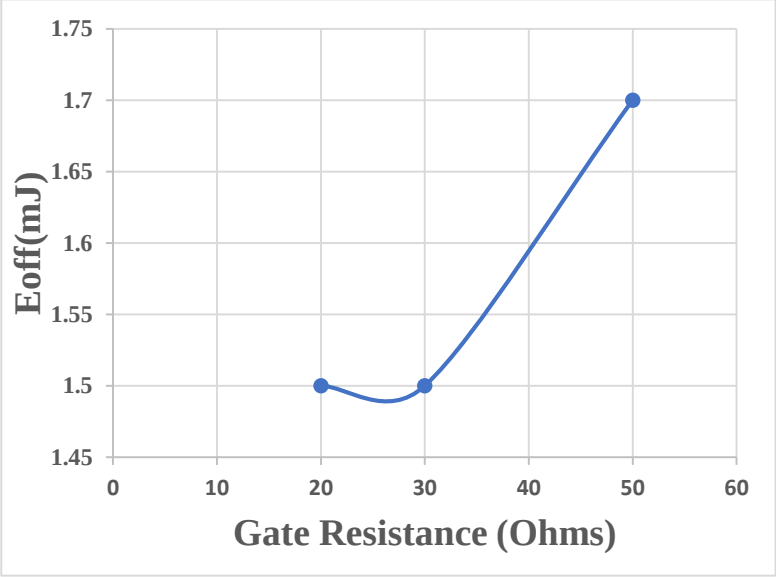


Figure 3.15: Turn-off switching losses vs Gate resistance for the conventional device

3.1.7 Short Circuit Performance

The short circuit simulation is carried out by the circuit configuration below with the given parameters.

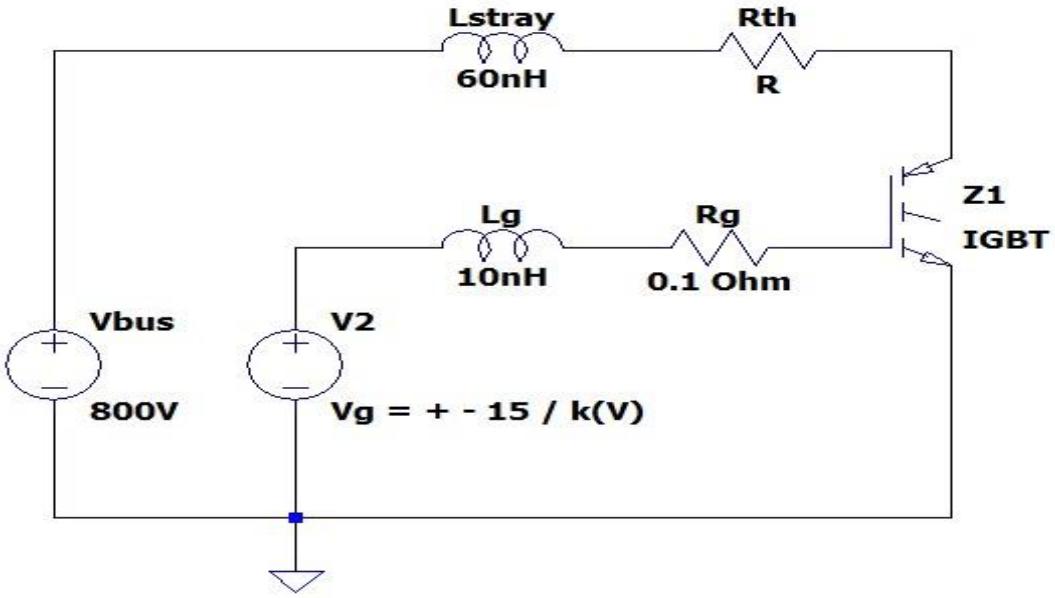


Figure 3.16: Inductive switching circuit configuration

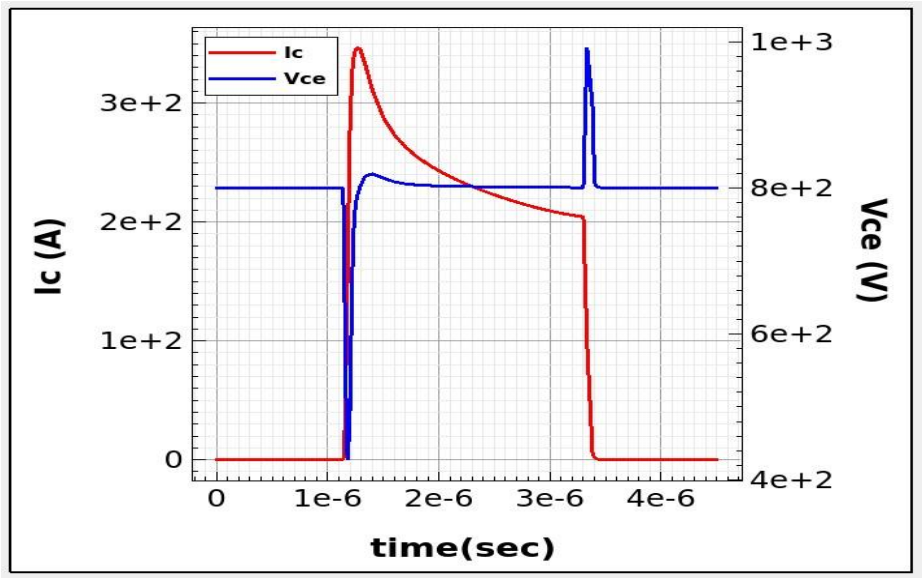


Figure 3.17: Short circuit performance of the conventional device k=1, T_j=400 K, Rated current I_c = 40A, V_{ce}=800 V, V_{ge}=15 V.

The simulated short circuit waveform of the conventional device is shown in fig.3.17 with the simulated condition given. According to the figure, the collector voltage V_{ce} rises to the bus voltage before turn-on as the gate voltage V_{GE} = 0V. The device turned-on after about 1us with

a peak current corresponding to the value of the saturation current at 400K as shown in fig.3.9 above. However, the short circuit current decreases with time after turn-on as a result of reduction in carrier mobilities due to self-heating of the device. The device turns-off successfully after about 3.5us with a sudden rise in collector voltage.

Given that voltage is directly proportional to resistant (V=IR) and resistance increases with temperature due to increased vibration of the molecules within the conductor. Therefore, voltage increases with the increase in temperature and verse versa. With regard to this understanding, it is reasonable to say that the instantaneous rise in collector voltage at turn-off is accompanied by a corresponding increase in device temperature.

3.2 Summary

In summary, a 1.2kV Field Stop Trench IGBT was developed and characterised based on the existing Trench IGBT model available in the Sentaurus Environment. Electrical characteristics which comprise of both static and dynamic characteristics were simulated employing Technology Computer Aided Design (TCAD) Sentaurus. Static and dynamic characteristics confirms an ideal device behaviour and therefore was adopted for scaling purpose in order to realize a scaled device with an improved performance which is one of the focus of this thesis.

CHAPTER FOUR

4.0 Numerical Analysis of Trench IGBT Subject to 2-D Scaling Rules

Unlike the conventional IGBT structure which relied on deep trench gate on the emitter side to achieve superior trade-off correlation between on-state voltage drop $V_{c(sat)}$ and turn-off loss [7], [60]–[72] "More Moore" process technologies was extended to IGBT to improve their performance and ensure their compatibility with CMOS technology not long ago [73]. The scaling rule adopted for the Trench Gated IGBT [19], [21] reveals significant reduction in the on-state voltages ($V_{c(sat)}$) as a result of the Injection Enhancement (IE) effect [7]. It is reported [20]–[22], [25] that collector-emitter saturation voltage $V_{c(sat)}$ is lowered with increasing scaling factor (k). This explains higher carrier concentration in the emitter region as scaling factor (k) increases, which means that higher electron injection efficiency (Υ_n) is obtained in the TIGBT scaling principle [20], [25]. Thus, the performance of the scaled device in terms of its on-state voltage drop is better than the conventional structure. One of the challenges associated with devices with injection enhancement (IE) effect such as scaled devices with narrow mesa structure among others is degradation of its short circuit reliability by Collector Induced Barrier Lowering (CIBL) effect [8], [9].

Conductivity modulation takes place at the inversion layer of the p-base and both electron and hole densities becomes higher than the p-base doping concentration. This is in view of the fact that the hole current flows into the inversion layer of the p-base. However, this does not happen for the conventional device as the hole current does not flow inside the channel but rather into the neutral p-base. The conductivity modulation which occurs at the MOS-channel of narrow mesa IGBTs give rise to the increase in the conductivity of the channel and subsequently the MOS channel current increase. The conductivity modulation in the MOS channel is responsible for the cause of Collector Induce Barrier Lowering (CIBL) effect [9] which degrade short circuit stability.

In this work, a scaled k=3 Trench IGBT device is proposed with the depth of p+ layer slightly increased which tends to mitigate CIBL as the potential in the p+ layer becomes stable even at short circuit condition characterized by an increased collector voltage V_{CE} and consequently causes large current flow in the mesa region (channel inversion layer). The propose scaled k=3 device therefore avoid CIBL occurrence in the mesa region and realizes an improved short circuit performance and thus improves short circuit safe operating area (SCSOA). In this

chapter, employing TCAD tool, 2-D scaling rule is proposed for Trench Gated IGBT. The electrical characteristic of the scaled device is equally investigated and compared with the conventional structure.

4.2 2-D Scaling Concept for Trench Gated IGBT

The scaling concept was built on the basic of CMOS scaling principles taking into account the emitter region electron injection efficiency [6]. Compared to the conventional structure, the concept realizes both shrinked emitter structure and higher electron injection efficiency. It gives rise to higher carrier concentration at the emitter region and a resultant reduction in the on – state voltage drop [6]. Presented in table 4.1 is a proposed scaling idea used in this work which was adapted from the literature [6]. The only major difference from the one in the literature is the trench width which was not scaled because of no appreciable influence in the $V_{ce(sat)}$. The mesa width (trench – trench spacing) (S), gate length (L_g) and oxide thickness T_{ox} in the MOSFET are reduced by a factor of 1/k in order to improve the Injection Enhancement effect (IE) whereas the cell pitch (W) is kept constant at 30um. Taking cognizance of the narrow mesa problems and manufacturability, the trench depth is lowered by 1/k. Fig.4.1b below show that Injection Enhancement is weakened by trench depth decrease thereby the impact of $V_{ce(sat)}$ on D_T is very insignificant. Also, very relevant is the scaling of the operating voltage V_g. The gate switching energy would have been lowered remarkably. Therefore, for the scaled device of k=3, the gate voltage V_g is lowered to 5V which is very useful in CMOS logic circuits. Also very significant is that the noise margin is reduced at low gate voltage V_g.

Table 4.1 show the parameters that are scaled according to the scaling rules which are explained in this section. Fig.4.1a shows a conventional IGBT that has a trench depth of 4.5um and p-base depth of 2um. Mesa width (trench-trench spacing) is 3um. The thickness of the gate oxide is 0.1um. The concentration of the p-base is chosen to give a suitable gate threshold voltage of around 5.8V and the applied gate voltage is 15V. The scaling factor (k) is introduced for the mentioned structure parameters which will be scaled employing the scaling rule as given in the Table 4.1 below. Fig.4.1b and 4.1c show the emitter region of the scaled TIGBT with k=2 and k=3 respectively. For the scaling factor k; four parameters are reduced in their dimensions which includes: trench-trench spacing S (mesa width), gate-oxide thickness T_{ox}, Trench depth D_T and p-base depth D_p. Scaling the individual parameters can be written as: S' = S/k, T_{ox}' =

T_{ox}/k, D'_T=D_T/k and D'_P =D_P/k where the primed parameters are the scaled devices. The length of the cell pitch remained unchanged. In order to further explain the scaling procedure with reference to the conventional device k=1 with the given dimensions for the scaling parameters. Considering the scaling rule explain above, for the scaled device k=2, its trench depth will be 2.25um, depth of the p-base will be 1um, trench-trench spacing (mesa width) will be 1.5um and the gate-oxide thickness will be 0.05um while the cell pitch maintains its length of 30um. For the scaled device k=3, the trench depth will be 1.5um, the depth of the p-base will be 0.6um, mesa width will be 1um and gate oxide thickness will be 0.03um in accordance with the scaling rule obtainable in [25]

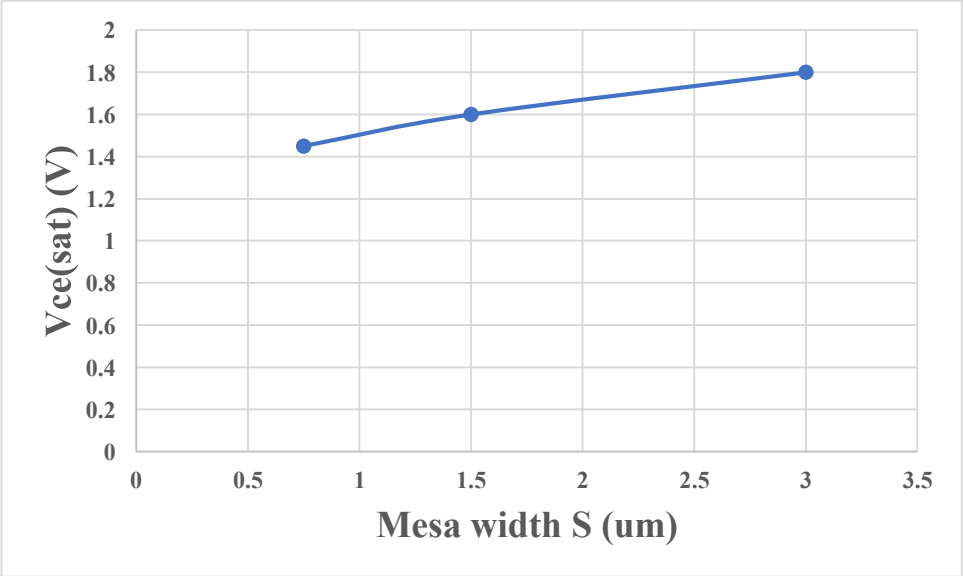
According to the authors in [21], it has been experimentally verified that the scaled devices have improved performance in terms of its $V_{ce(sat)}$ lowering. The figure 4.0 and 4.1 below show the impact of the scaled parameters on the device conduction loss $V_{ce(sat)}$. Moreover, scaling the operating gate voltage from 15V in k=1 to 5V in k=3 significantly lowers the gate switching voltage and such voltage can be very useful in CMOS logic circuit. In addition, scaling from k=1 to k=3, the device area remains unchanged and therefore maintains same current handling capability like the conventional device k=1 since the cell pitch is not scaled. The n-drift region of the scaled device maintains the same thickness as the conventional device thereby supporting the same 1.2kV during the turn-off without breakdown initialization. Similar saturation current level as well as the switching characteristics is maintained in the scaled device like that of the conventional structure by slightly adjusting the p-base concentration instead of applying scaling rule [19].

Table 4.1: Structure parameters and Scaling Principle

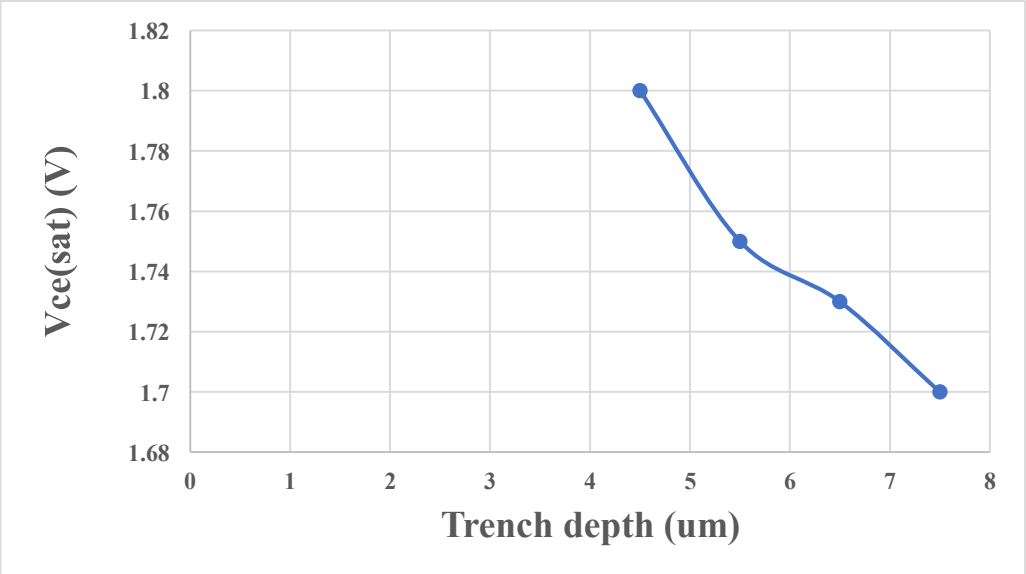
Parameters	Symbols	k=1	k=2	k=3	Scaling factor
Cell width	W [um]	30	30	30	1
Trench width	W_T [um]	1.0	1.0	1.0	1
Trench depth	D_T [um]	4.5	2.25	1.5	k
Mesa width	S [um]	3.0	1.5	1	k
n+/p+ Depth	D_{pn} [um]	0.25	0.125	0.08	k
n+ Length	Ln+ [um]	1.0	0.5	0.33	k
p+ Length	Lp+ [um]	1.0	0.5	0.33	k
Gate Oxide Thickness	T_{ox} [um]	0.1	0.05	0.03	k
P-base Depth	D_{pb} [um]	2.0	1.0	0.67	k
Gate Voltage	Vg [V]	15	7.5	5	k

Table 4.2: Doping profile application

S/N	Region	Peak Doping Concentration		
		k1	k2	k3
1	n^+ and p^+	$1x10^{20}$	$1x10^{20}$	$1x10^{20}$
2	p-base	$2x10^{17}$	$2.8x10^{17}$	$4.8x10^{17}$
3	N-Drift	$5x10^{13}$	$5x10^{13}$	$5x10^{13}$
4	N-buffer	$2x10^{16}$	$2x10^{16}$	$2x10^{16}$
5	p^+ Collector	$3x10^{17}$	$3x10^{17}$	$3x10^{17}$



a



b

Figure 4.1: Impact of active structural parameters on $V_{ce(sat)}$; (a) Mesa width

(b) Trench depth

Figure 4.1 showed the $V_{ce(sat)}$ dependence on the parameters such as mesa width and trench depth. This simulation is done at the current density of 200A/cm^2 given that the device area is 27mm^2 and rated current of 57A at room temperature of 300K and the gate voltage is 15V. Fig.4.1(a) show a decrease in the $V_{ce(sat)}$ as the mesa width decreases due to injection enhancement (IE) effect i.e. increase in carrier concentration at the emitter region. Also, the Fig.4.1(b) show an impact of trench depth increase on the $Vce_{(sat)}$. As the trench depth increases under the same simulation condition as mentioned above, there is only a slight decrease in the $V_{ce(sat)}$ due to IE effect.

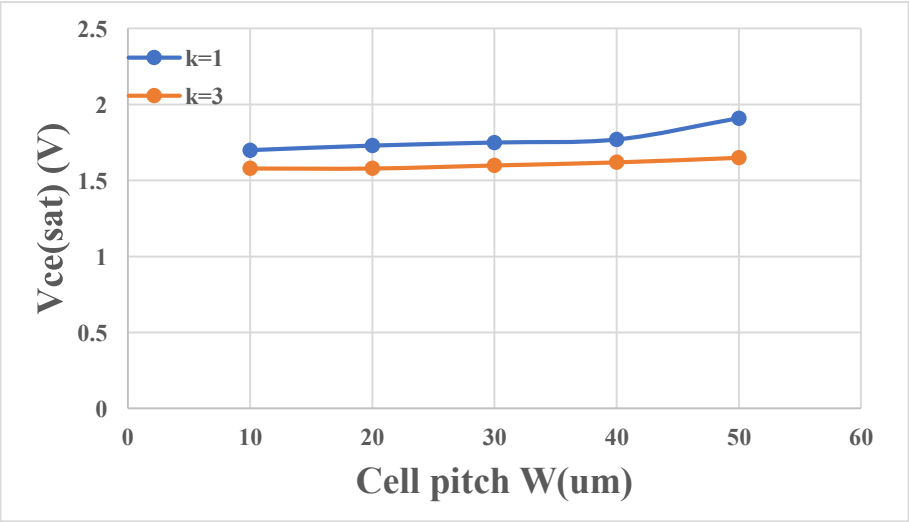


Figure 4.2: Impact of cell pitch increase on $V_{ce(sat)}$

This figure showed an impact of cell pitch increase on the conduction loss. It is obvious in the figure of an almost constant $V_{ce(sat)}$ as the cell pitch increases for both the conventional and scaled devices. This is why cell pitch has always maintained the same dimension thus keeping the device area constant to maintain the same current density for both conventional and scaled devices.

4.3 2-dimentional structure for the scaled device k=3

Employing the parameters of the above tables, the 2-dimentional structures of the scaled and the proposed scaled devices are simulated and presented below:

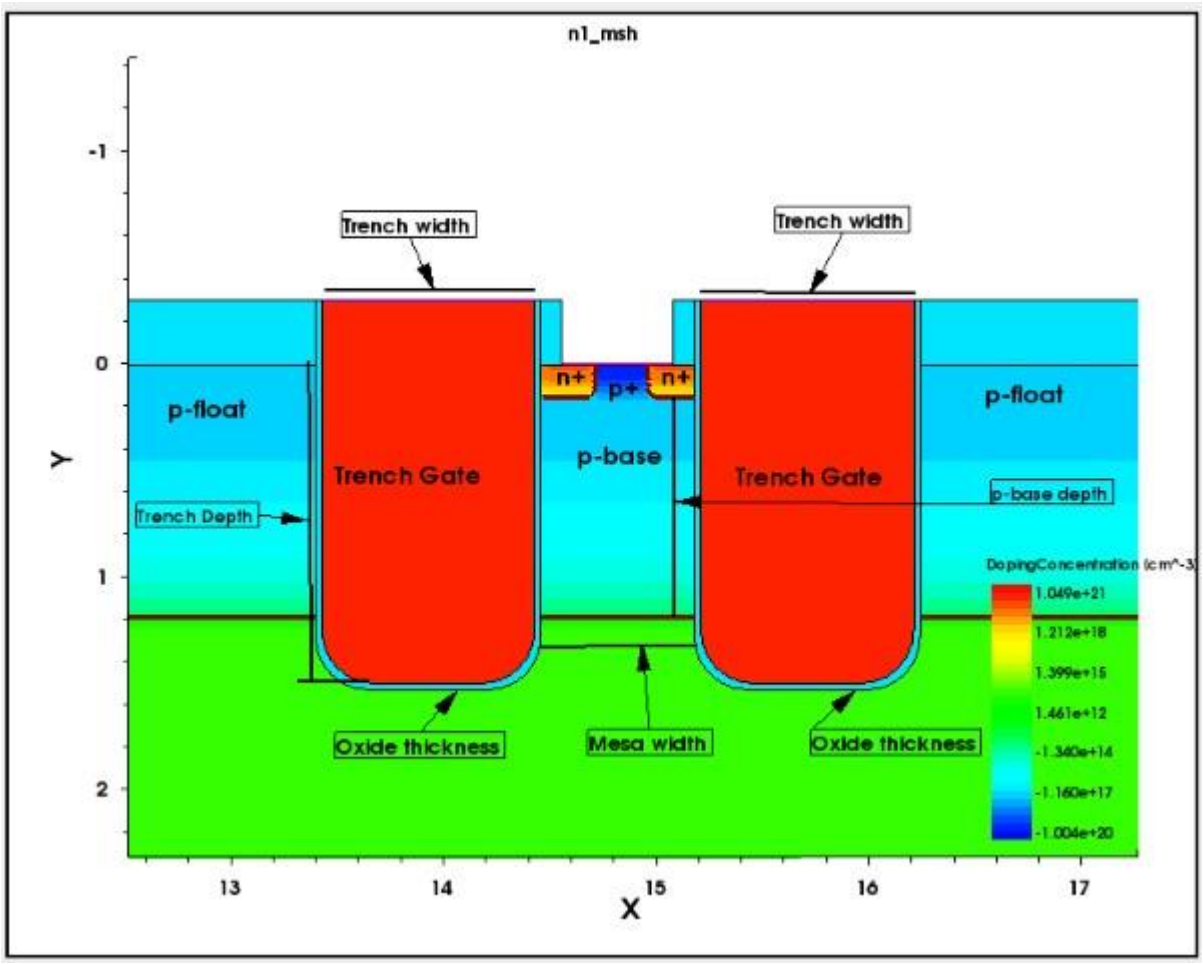


Figure 4.3(a): Zoomed structure of emitter region of the Scaled TIGBT, k=3

Fig.4.3a showed the scaled version of the conventional Trench IGBT that was discussed in the previous chapter. In the conventional structure, the structural parameters in the emitter region such as the mesa width, the trench depth, the depth of the P_{base} and the gate oxide thickness are all scaled according to the scaling principle shown in the Table 4.1 above in order to realise the scaled device k=3 shown in Fig.4.3a. The dimensions of the parameters to be scaled in the conventional structure are as follows: The mesa region =3 um, Trench depth = 4.5 um, depth of the p-base =2 um, Gate oxide thickness = 0.1 um. Thus, scaling the mentioned parameters according to the scaling principle gives the scaled device structure k=3 in Fig.4.3(a) with the following dimensions: (1) Mesa width = 1um, (2) Trench depth = 1.5um, (3) Depth of the p-base = 0.6um, (4) Gate oxide thickness = 0.03um. The scaled device k=3 have an improved performance in terms of its IV characteristics compared to conventional device because of enhanced carrier injection (IE effect) as will be seen in the later section.

4.4 Simulation Results and Analysis

Employing 2-dimensional TCAD tools within Synopsys Sentaurus Device [54], electrical characteristics of the scaled devices are analysed as follows:

4.4.1 Input Characteristics

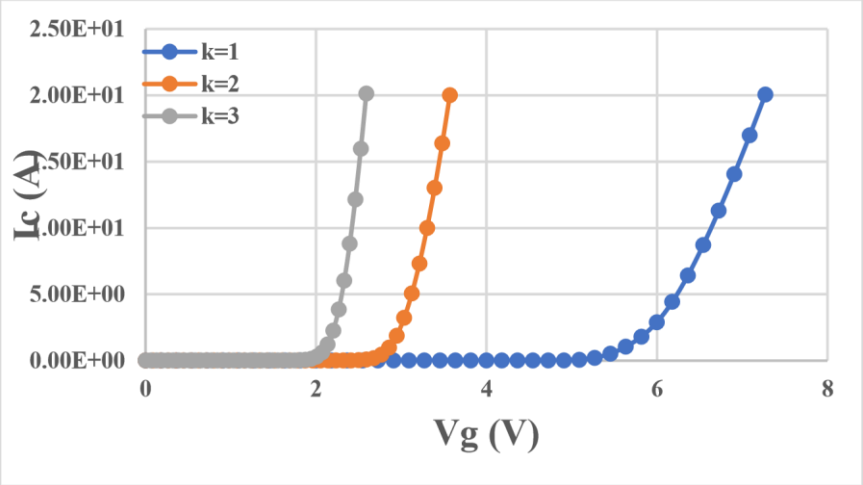


Figure 4.4 (a): Input characteristics of the conventional and scaled devices at Tj=300K

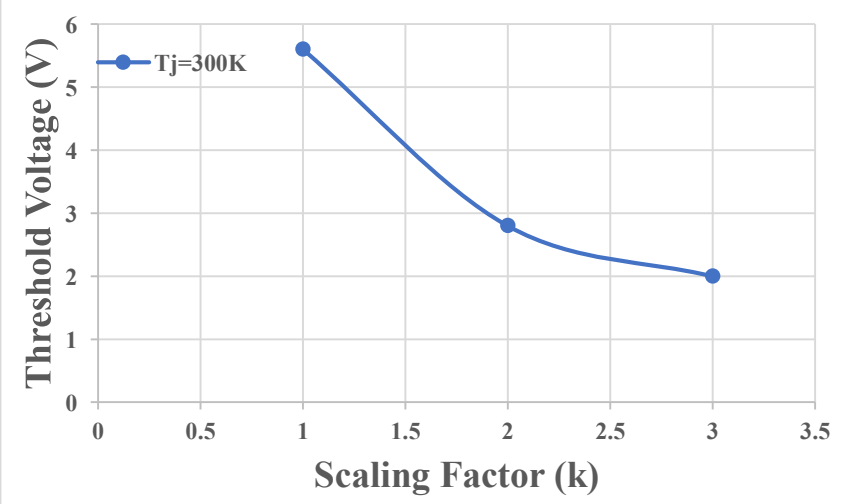


Figure 4.4(b): Impact of the scaling factor (k) on the threshold voltage

It is necessary to reduce the threshold voltage (V_{th}) of the scaled devices k=2 and k=3 due to their lowered gate voltages obtained through scaling rule. Thus, the threshold voltages of the scaled structures are lowered through slight adjustment of the p-base doping concentration as well as lowering the channel length and the oxide thickness through scaling rule as shown in Table 4.1 and 4.2 above. Slightly increasing the p-base doping concentration increases the potential of the channel thereby leading to induced barrier lowering. Reduction of the gate oxide thickness via scaling rule increases the gate capacitance and thus allows a smaller voltage to induce the same channel charges which leads to channel inversion. Fig.4.4(a) above show

the input characteristics of the conventional and the scaled devices and Fig.4.4(b) showed the impact of scaling factor on the threshold voltage, the threshold voltage decreases with the increase in the scaling factor (k) which validate the transfer characteristics in Fig.4.4(a).

As a result of the scaled gate oxide as well as the reduced channel length, transconductance of k=2 and k=3 is enhanced compared to k=1 as shown in Fig.4.5(a) and 4.5(b) below.

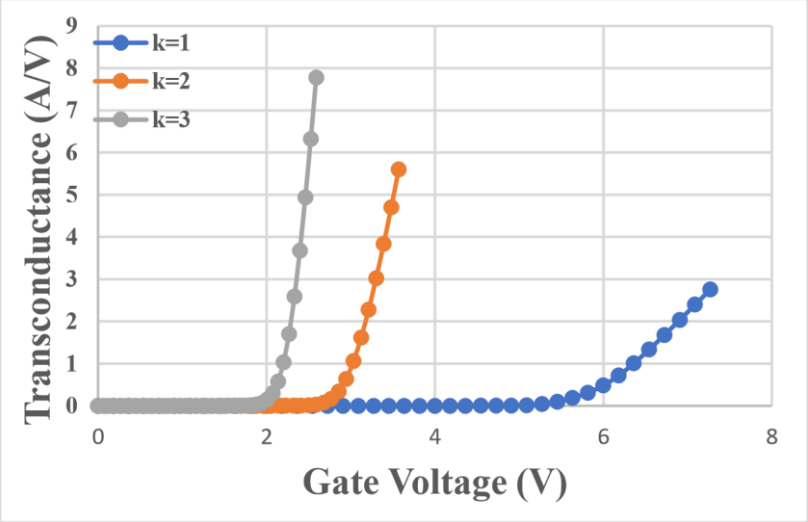


Figure 4.5(a): Transconductance of the conventional and scaled devices at T_j=300K

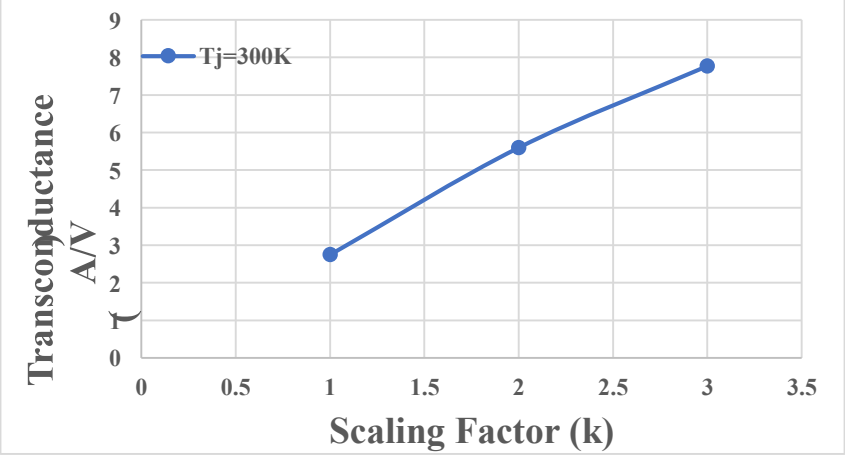


Figure 4.5(b): Impact of the scaling factor (k) on the transconductance

This means that the channel resistance of the scaled devices is lowered as can be seen in the Fig.4.6 since the transconductance is the inverse of resistance [25]. In other word, it is the ratio of the change in collector current to that of the gate voltage.

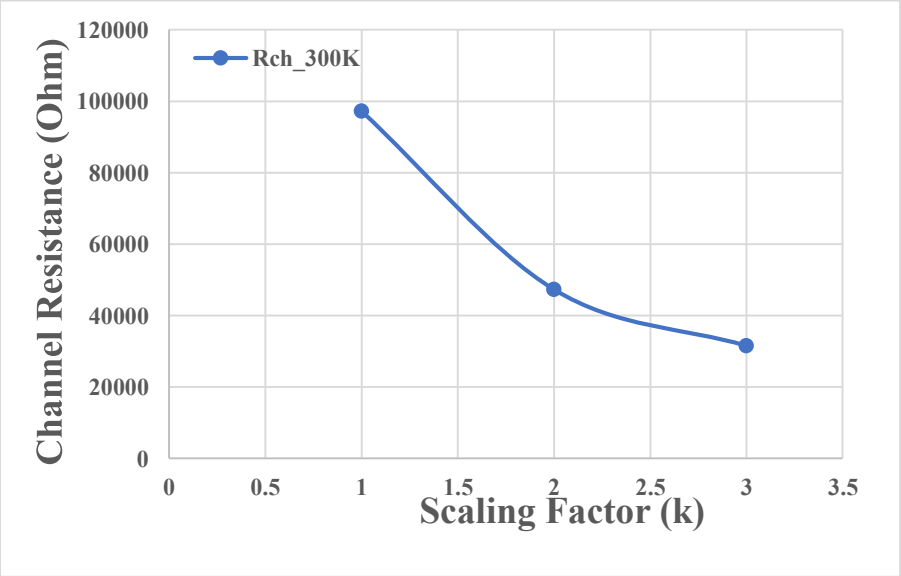


Figure 4.6: Impact of the scaling factor (k) on the channel resistance

Due to the remarkable reduction in channel resistance R_{ch} as a result of gate oxide thickness lowering, the I-V characteristics is enhanced [25]. This is depicted in equation 4.1 below.

$$\boldsymbol{R_{ch} = \frac{L_{ch}}{Z.\mu_{ni}.C_{ox}.(V_g - V_{th})}} \quad (4.1)$$

Where L_{ch} is the channel length, Z is the addition of the n+ length, μ_{ni} is the inversion layer mobility and C_{ox} is the gate oxide capacitance. According to equation 4.1 above, the lowering of the gate oxide thickness T_{ox} increases the gate oxide capacitance C_{ox} and thus the channel resistance R_{ch} lowers. The increased oxide capacitance C_{ox} allows a smaller voltage to induce the same channel charge and activate current flow.

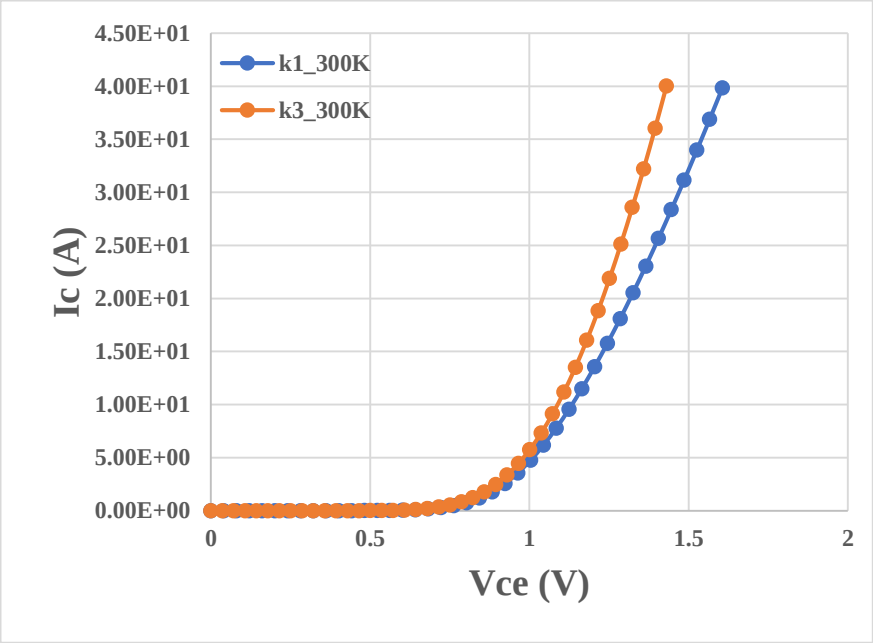


Figure 4.7(a): I-V characteristics of the conventional and scaled devices at Tj=300K.

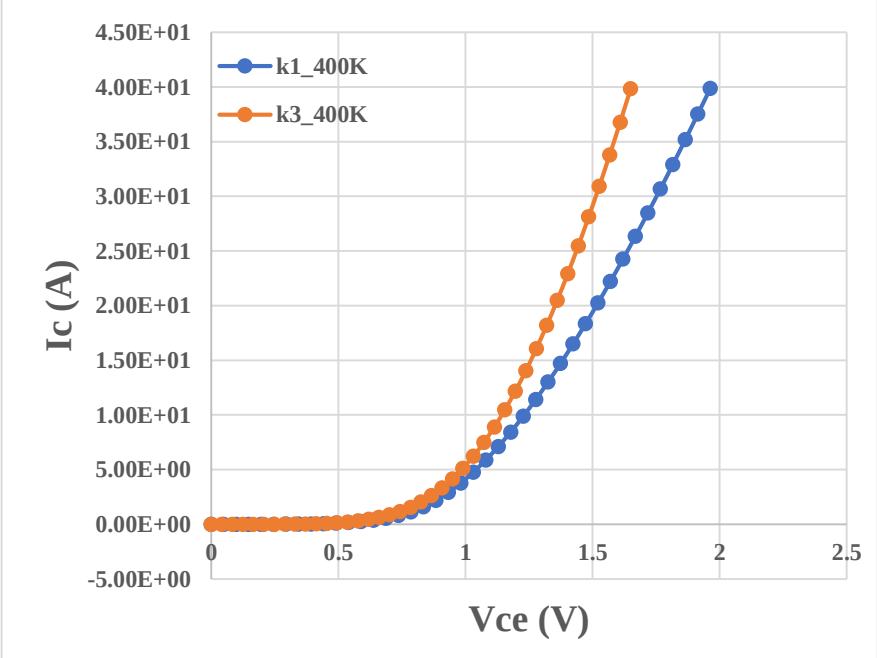


Figure 4.7(b): I-V characteristics of the conventional and scaled devices at Tj=400K.

According to the carrier distribution in the drift region as shown in the Figure 4.9(a) and 4.9(b) below, it is quite obvious that incrementing the scaling factor k yields higher carrier concentration at the emitter region. The IGBT scaling rule according to the result yields a higher electron injection efficiency Υ_n compared to the conventional structure and thus improve the performance of the scaled devices [20] in terms of its I-V characteristics. The Fig.4.7a show the simulated I-V characteristics of the conventional and scaled devices k=1 and k=3 at 300K.

The figure shows an improved on-state voltage drop $V_{ce(sat)}$ of 1.4 V for k=3 as against 1.6V for k=1 at the collector current of 40A. On the other hand, Fig.4.7(b) depicts the device I-V characteristics for the high temperature of 400 K, the saturated voltage $V_{ce(sat)}$ for the conventional structure k1 is 1.96V while that of k3 is 1.64V at the collector current of 40A. The significant decrease in the on state voltage drop for the scaled device k=3 is due to improvement in IE effect (i.e. increase in carrier concentration at the cathode side of the drift region) as a result of reduced mesa width through scaling rule. This leads to improvement in conductivity modulation in the n-drift region [20].

4.5 Influence of Scaling Factor on the $V_{c(sat)}$

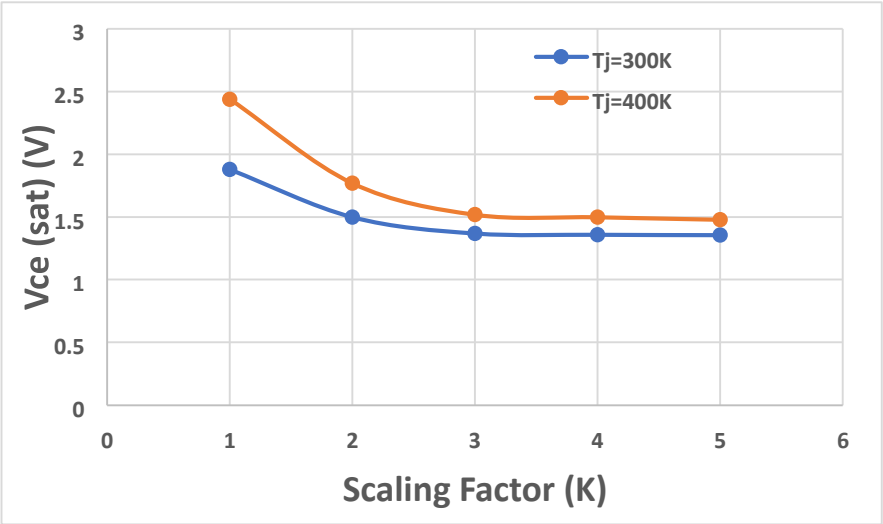


Figure 4.8: Influence of scaling factor K on the $V_{ce(sat)}$

The influence of scaling factor k on the on-state voltage drop $V_{ce(sat)}$ is shown in the Figure 4.8. The Figure shows a remarkable decrease in the on-state voltage drop as the scaling factor increases and tend to saturate as the scaling factor k is greater than 3. This is because looking at the on-state carrier distribution across the device in fig.4.9(a) and 4.9(b) below, there is a linear increase in the carrier distribution at the emitter side of the n-drift region for the k1, k2 and k3 devices only. The carrier increase is very significant at the scaled device k=3. This therefore explains the low on – state voltage drops ($V_{ce(sat)}$) for k=3 device.

4.5.1 On _ State Carrier Distribution

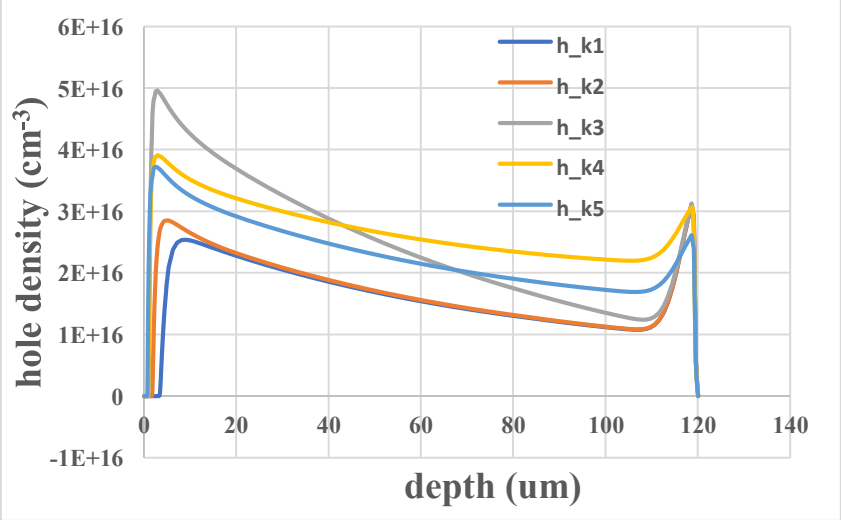


Figure 4.9(a): Hole carrier density during the on – state, Tj=300K, Rated current I_C = 40A

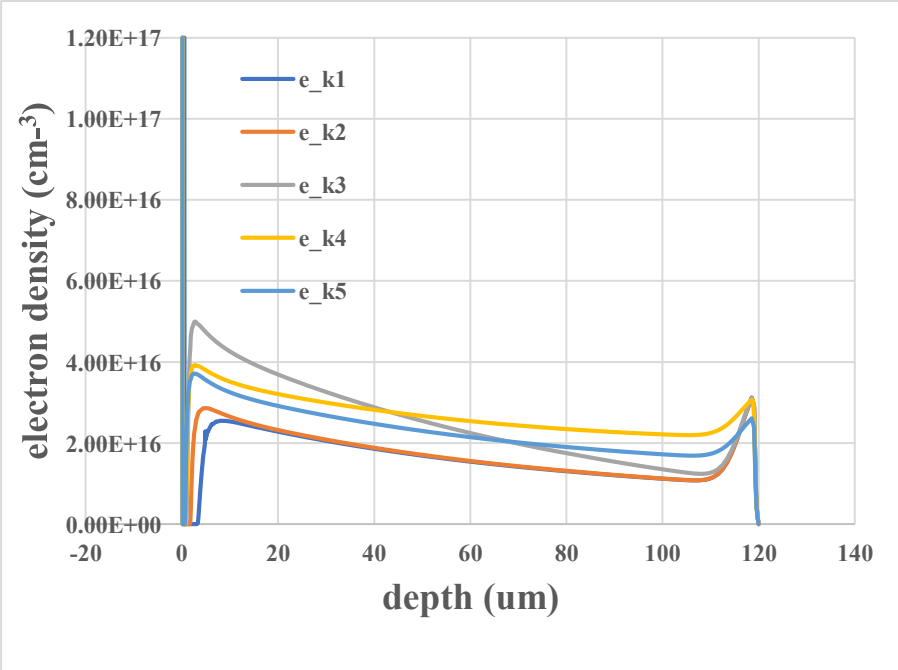


Figure 4.9(b): Electron carrier density during the on – state, Tj=300K, Rated current I_C = 40A

The figures 4.9(a) and 4.9(b) showed the n-drift carrier distribution during the turn-on state for both the conventional and the scaled devices. Given that the peak doping concentration of the p-anode and the n-buffer doping is the same for all the devices, it is shown in the above figures that the IGBT scaling principle obtains higher carrier injection efficiency than the conventional structure. The figures reveal a much-higher carrier increase at the scaled device k=3. This show that the performance of the scaled device k=3 in particular is better than the conventional device k=1 [20]. The increased carrier injection for the scaled device k=3 leads to enhancement of the

conductivity modulation at the n-drift region which result to lowering of the on-state voltage drop. This means that scaling the emitter structure gives characteristics improvement of the scaled devices in terms of its I-V characteristics compared to the conventional device but will suffer from CIBL due to conductivity modulation in the mesa region. This will lead to unsaturation of the output current characteristics and subsequently lead to poor short circuit performance.

4.5.2 Breakdown characteristics

Figure 4.10(a) shown below depicts a simulated breakdown characteristic of the conventional and scaled devices. The scaled device k=3 show a higher breakdown voltage of 1500 V compared to the conventional structure which is 1385 V. The higher breakdown voltage in the scaled device is due to the narrowed mesa width (trench-trench spacing). The narrowed mesa width reduces the electric field beneath the trench gate as shown in Fig. 4.10(b) below.

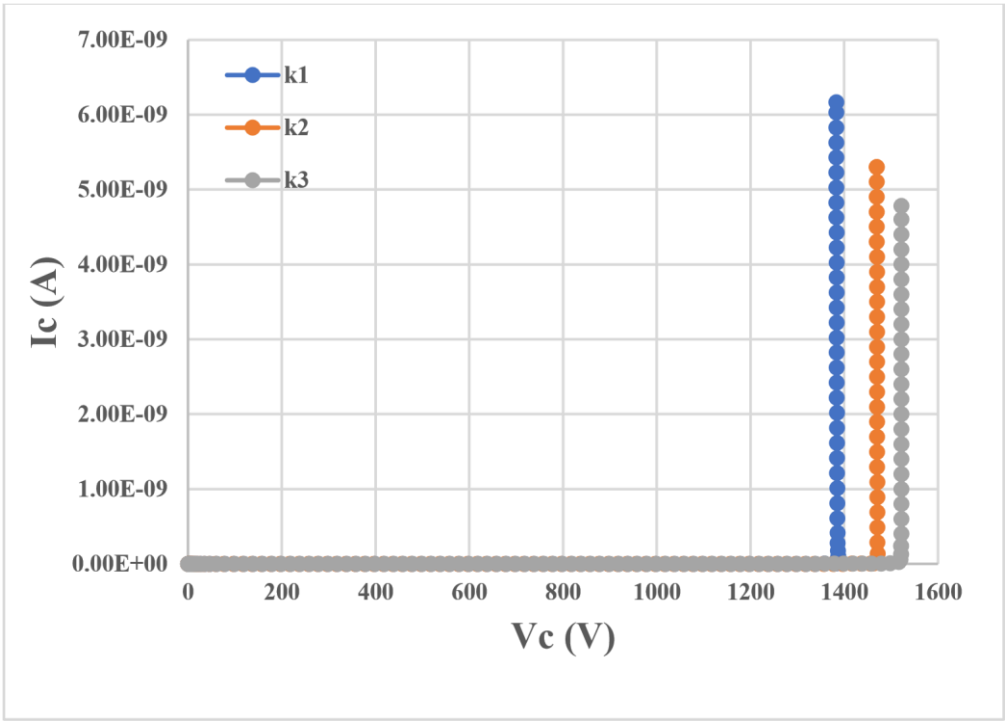


Figure 4.10(a): Breakdown characteristics for k=1, k=2 & k=3, V_{ce}=1430V, T_j=300K

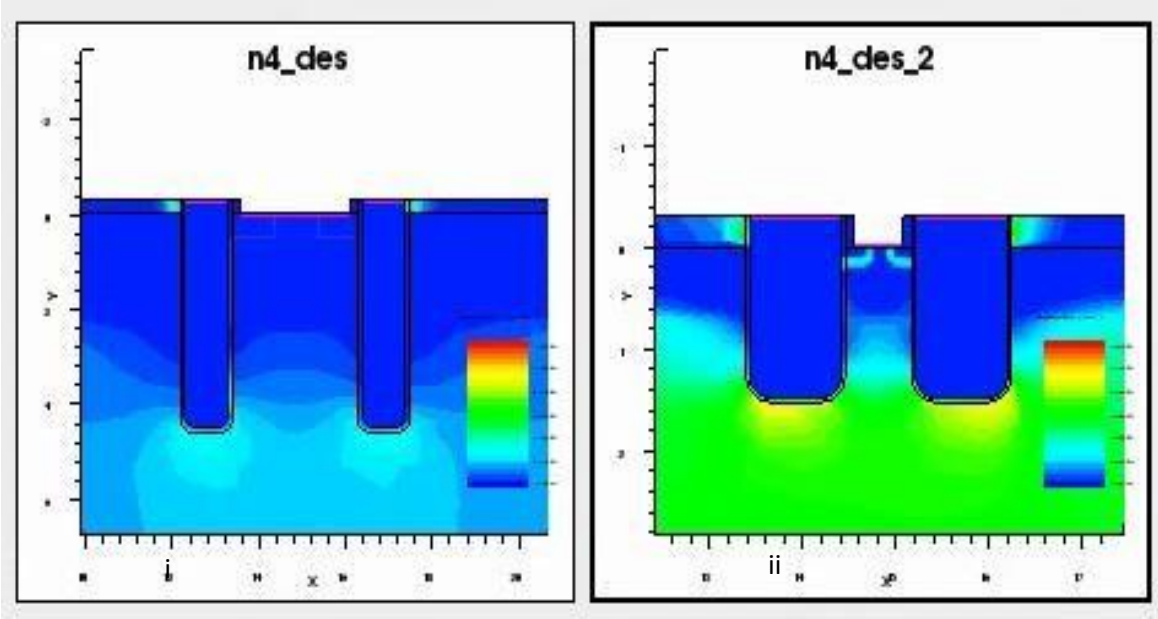


Figure 4.10(b): Electric field profile at breakdown for (i) Conventional structure k=1 and (ii) Scaled device k=3

4.6 Electric field Distribution

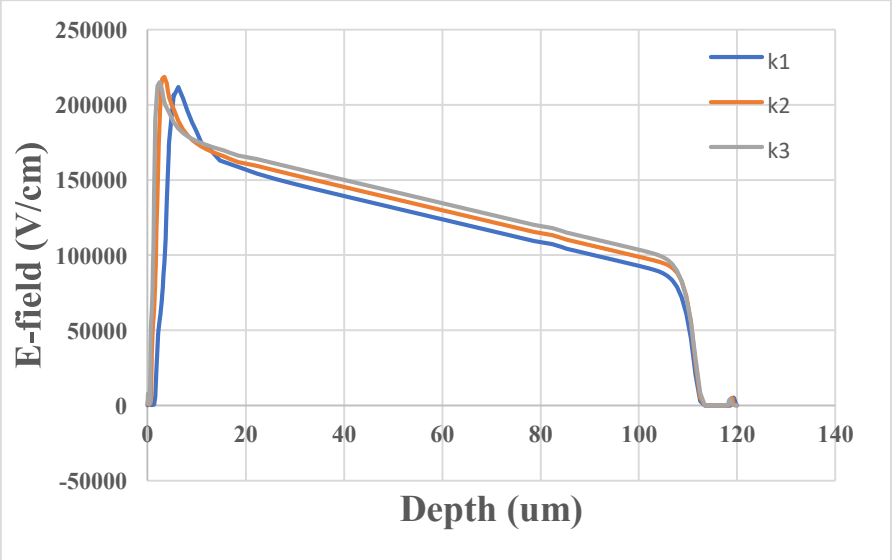


Figure 4.11: Electric field distribution at breakdown for k=1, k=2 and k=3, T_j=300K.

The electric field distribution at breakdown voltage for the conventional k=1 and the scaled devices k=2 and k=3 is shown in Fig.4.11. According to the figure above, the maximum electric field occur at the junction between the P_{base} and the drift region which is obviously less than $5x10^5$ V/cm which is the maximum electric field at breakdown for silicon power devices.

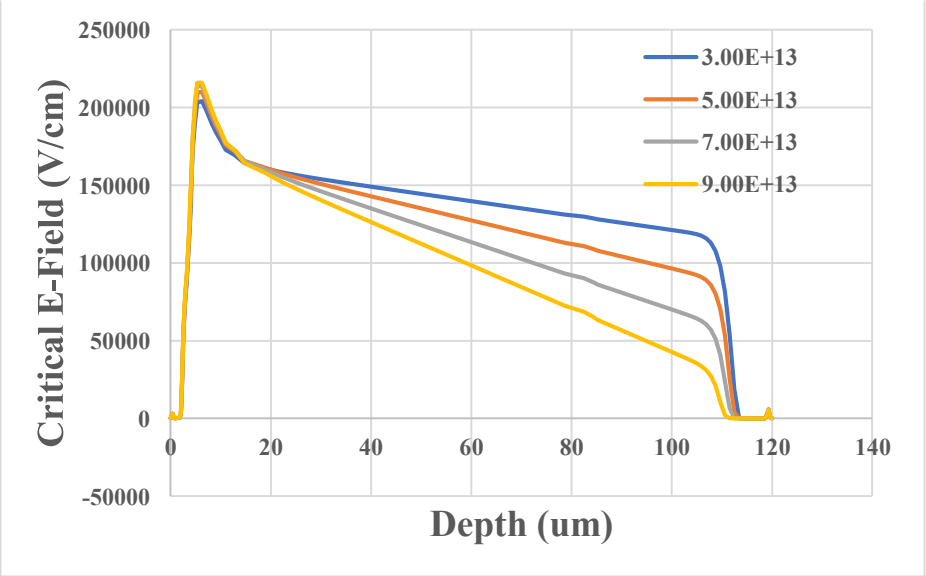


Figure 4.12: Impact of doping concentration on the critical e-field at T_j=300K.

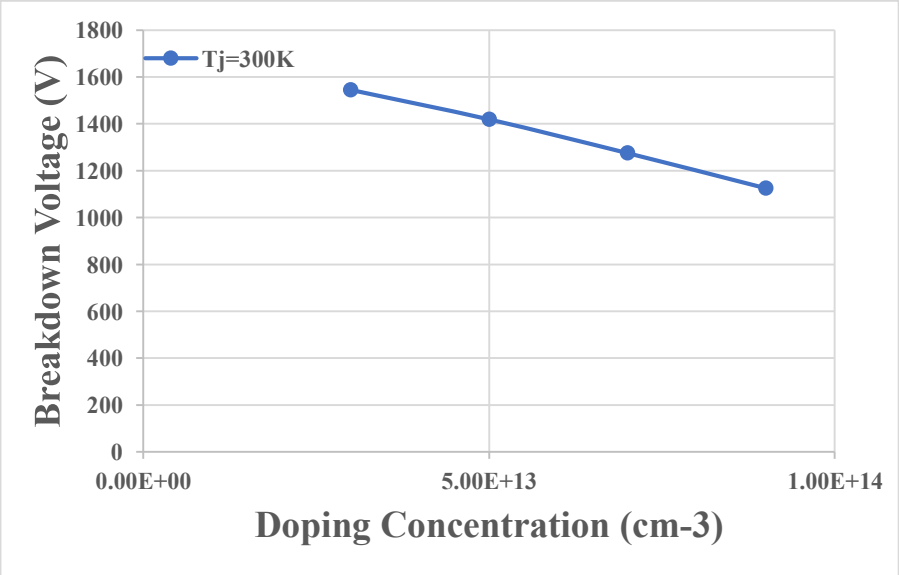


Figure 4.13: Impact of doping concentration on the breakdown voltage, T_j=300 K.

Figure 4.12 showed a strong dependence of the critical electric field on the doping concentration for a conventional device k=1. The critical electric field tends to increase with the increase in the n-drift doping concentration. As the doping concentration of the n-drift region increases, the width of the depletion layer decreases and therefore lowering the breakdown voltage as can be seen in fig. 4.13.

4.7 2-dimentional structure for the proposed scaled device k=3

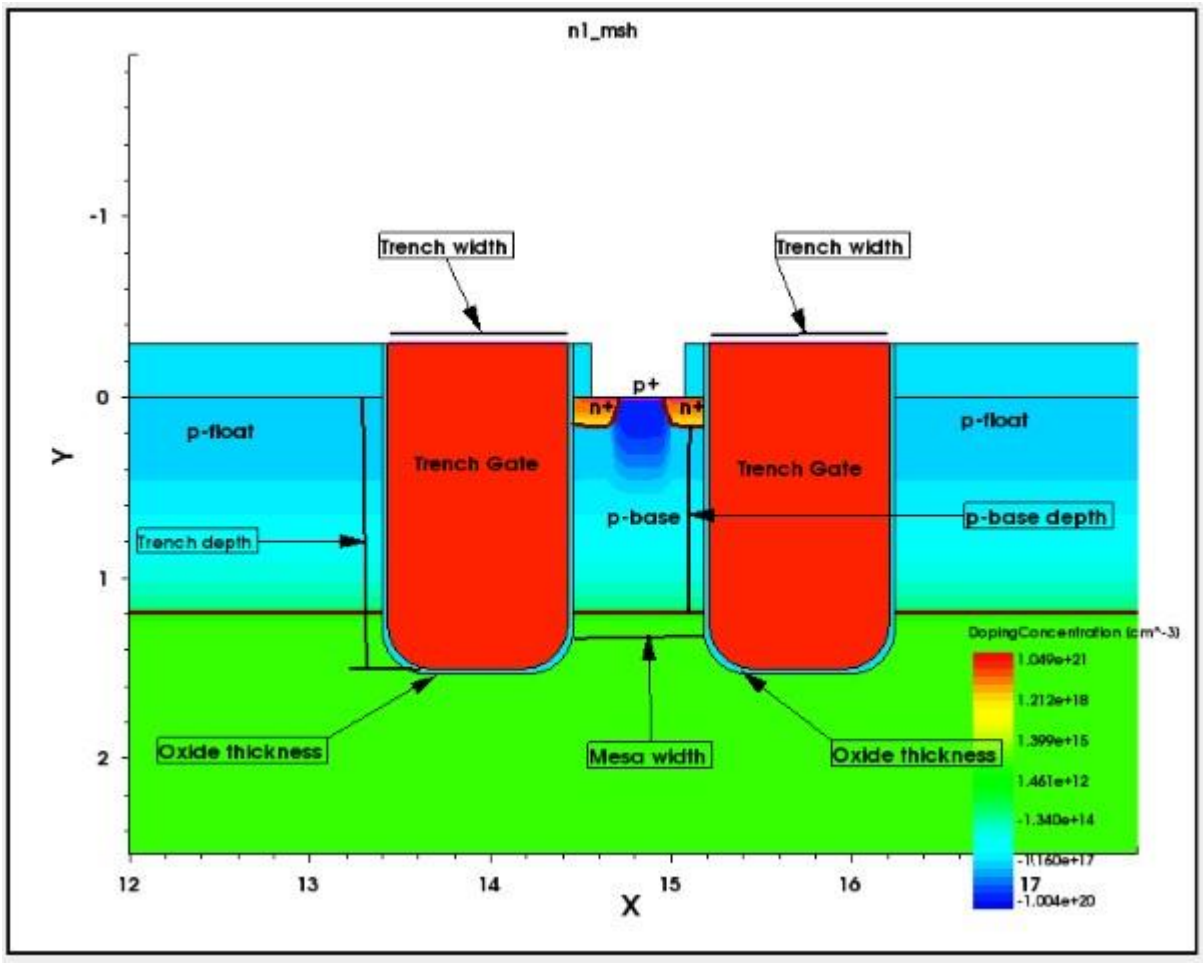


Figure 4.14: Zoomed structure of the emitter region of the proposed scaled k=3 device.

This Figure 4.14 showed the emitter region of the proposed scaled k=3 device. The scaled dimension of this structure is the same as that of the scaled k=3 device shown in the previous section of figure 4.3(a) above where the mesa width = 1um, trench depth = 1.5um, depth of the p-base = 0.6um and oxide thickness = 0.03um. The only difference in this structure compared to the conventional scaled k=3 device is the increased depth of p+ emitter contact. The depth of the p+ emitter contact is increased from 0.08 um in the scaled k=3 device to 0.24 um in the proposed device k=3.

The lateral diffusion of the increased depth of the p+ emitter moves into the p-base region thereby helping to maintain the junction barrier between the p-base and n+ emitter and thus suppressing the effect of collector induced barrier lowering (CIBL) effect. More importantly, the threshold voltage as well as the on – state voltage is not affected as the p+ emitter does not penetrate the p-base region.

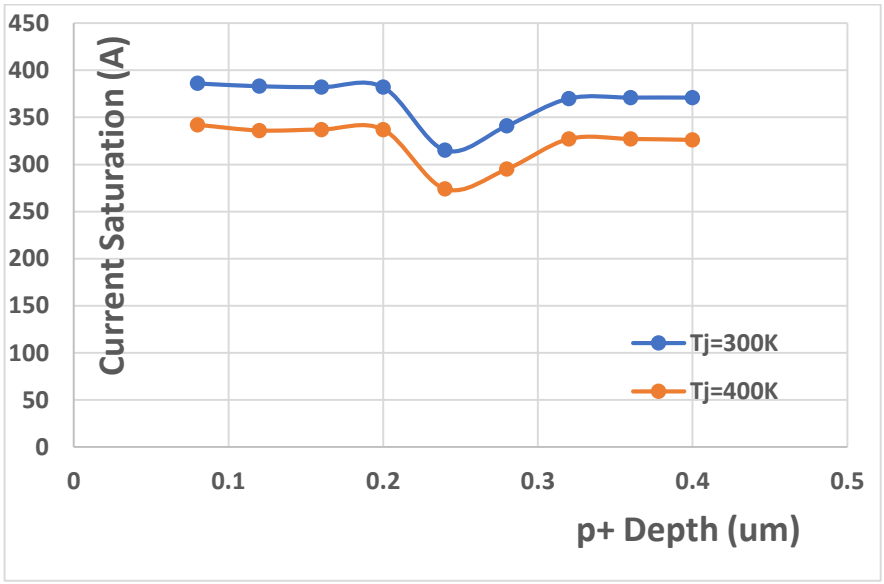


Fig.4.15(a): Impact of the increased depth of p+ emitter on saturation current

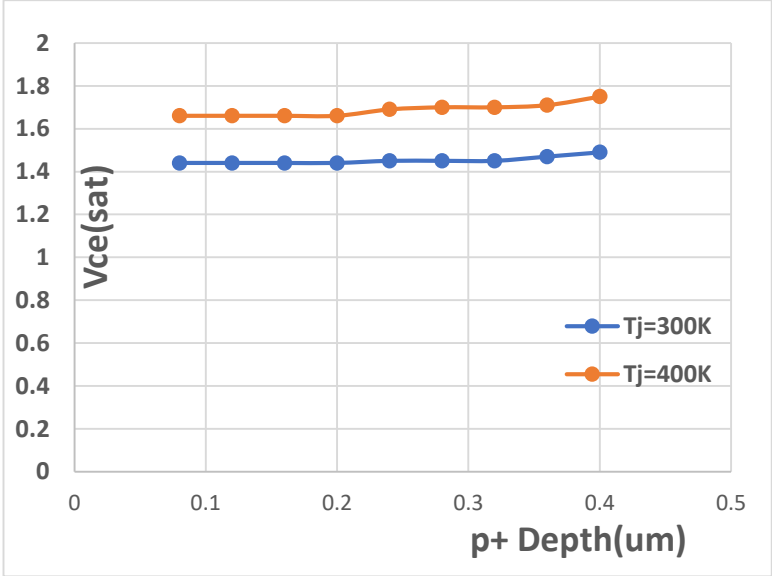


Figure 4.15(b): Impact of the of the increased depth of the p+ emitter on $V_{ce(sat)}$

Figure 4.15(a) & 4.15(b) show the influence of the increased depth of the p+ emitter upon the saturation current and Vce(sat) at 300K and 400K respectively. As can be seen in the Figure 4.15(b), the increased depth of the p+ emitter does not affect the on – state performance at both temperatures. This is because the threshold voltage as well as the channel resistance of the proposed IGBT are not affected by the lateral diffusion of the p+ emitter. However, considering the Figure.4.15(a), it is noticed that the current saturation maintained its high value as the depth of the p+ emitter increased until the depth exceeds 0.2um. The saturation current shows significant reduction as the p+ emitter depth exceeds 0.2um and thereafter increases when the p+ emitter exceeds 0.24um. This is because the lateral diffusion of the p+ emitter only have

influence on the junction barrier between the p-base and n+ emitter when the p+ emitter depth is between 0.2um to 0.24um. As the depth exceeds 0.24um, the lateral diffusion of the p+ emitter has less influence on the junction between the p-base and the n+ emitter and as a result, the saturation current start to rise again.

4.7.1 Current Saturation Characteristics

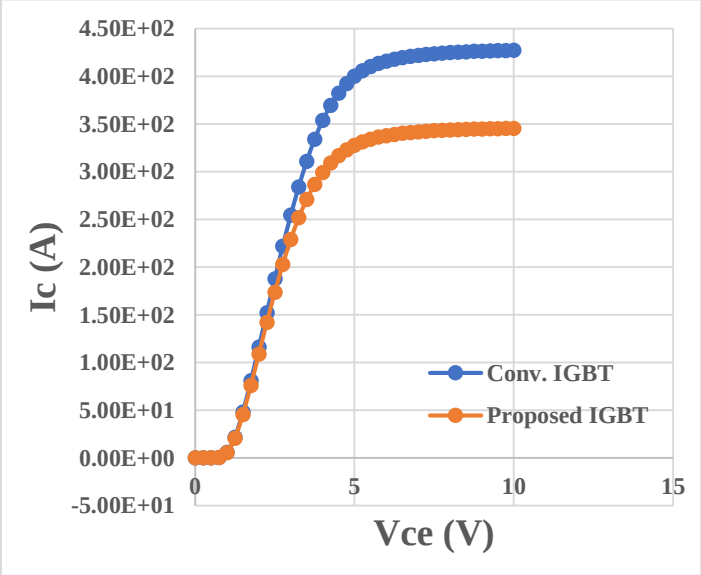


Figure 4.16: Current Saturation Characteristics for the conventional and proposed device @ T_j=300 K. ($V_g = 5V$).

Shown in fig.4.16 is a comparison of the current saturation characteristics of the conventional and the proposed devices whereas fig.4.17(a) and 4.17(b) compares potential distribution within the mesa regions for the conventional IGBT and the proposed device respectively. It is discovered from fig.4.16 that the conventional IGBT reveals non – saturated and high saturation current characteristics as a consequence of CIBL effect [7]. Owing to the hole current flowing into the inversion layers and the n+ emitter during the on – state, the potential barrier of the n+/p-base junction thereby lowers. Under this condition, conductivity modulation is enhanced in the channel inversion layer and thus, the bipolar carrier flow is enhanced and current show no saturation as can be seen in the Fig.4.16.

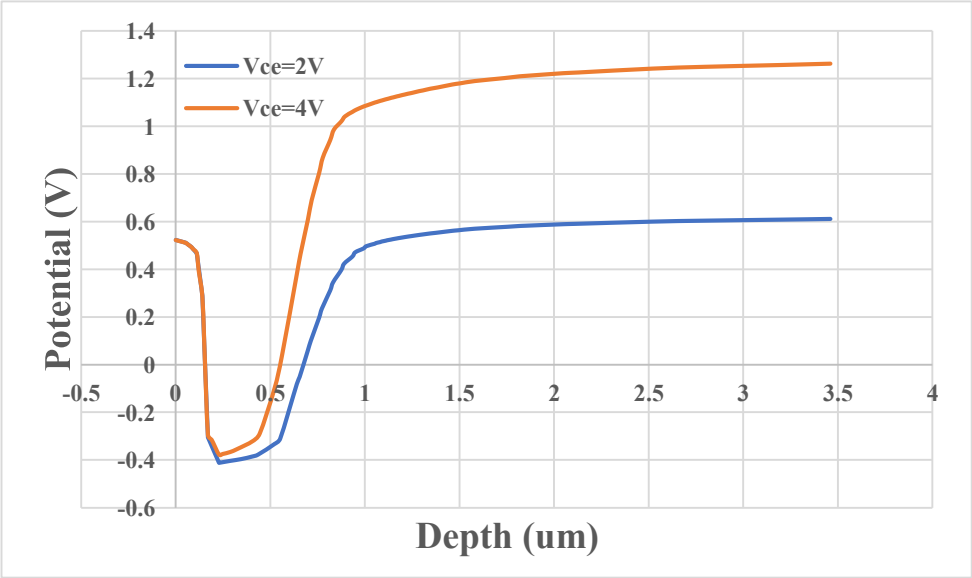


Figure 4.17(a): Potential distribution within the mesa region (n+/p_{base} junction) @ T_j=300K for conventional k=3 device.

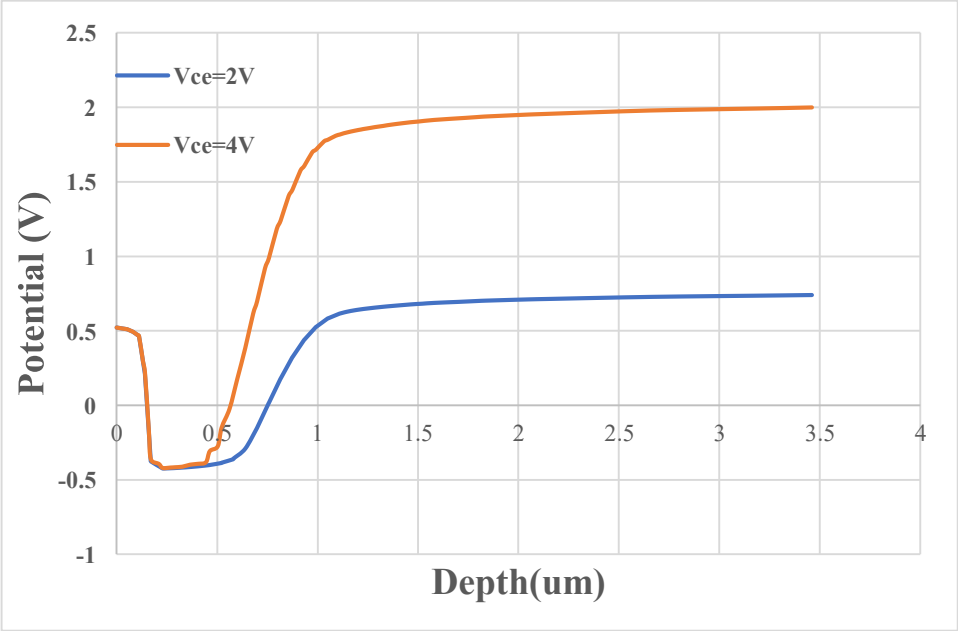


Figure 4.17(b): Potential distribution within the mesa region (n+/p_{base} junction) @ T_j=300K for the proposed k=3 device.

This is the mechanism of CIBL. As a consequence of this, the junction barrier between the p-base and the n+ emitter lowers significantly with increased collector voltage as shown in fig.4.17(a). This leads to non-saturated and high collector current characteristics which is

capable of causing latch – up and deteriorate short circuit capability thereby reducing the safe operating area (SOA) of the Trench IGBT device as will be seen in the later section One of the possible means of lowering high collector current behaviour is by increasing p-base doping concentration at the cost of increase in the threshold voltage which will also have an impact on the on – state performance as shown in fig.4.18(a) and 4.18(b) below.

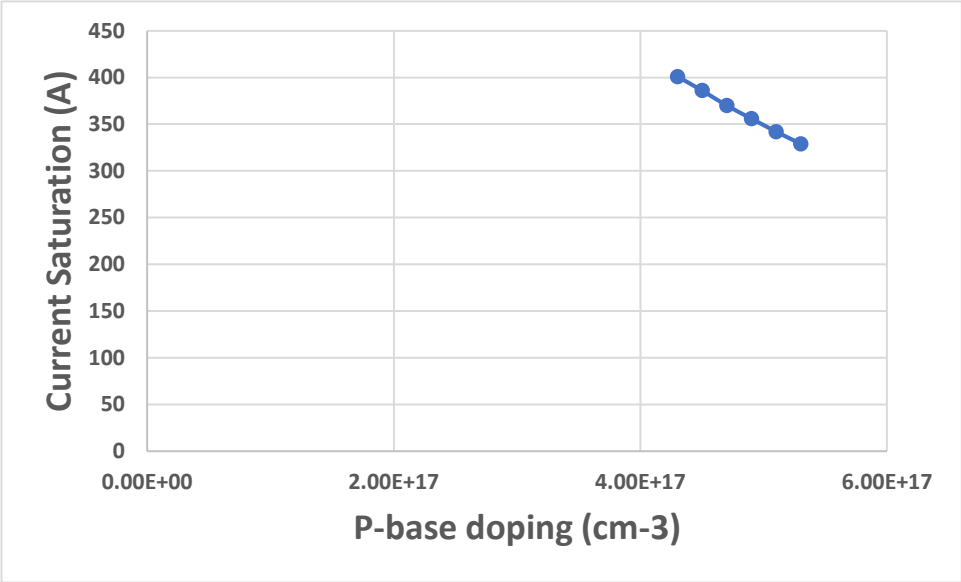


Figure .4.18(a): Impact of p-base doping concentration on current saturation. (Vg =5V, Tj=300K).

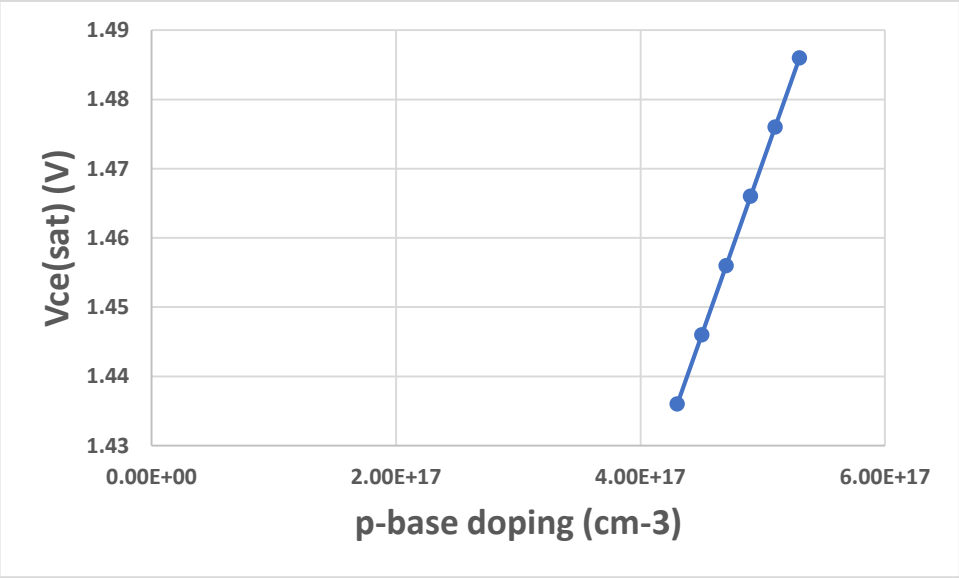


Figure.4.18(b): Impact of p-base doping concentration on $V_{ce(sat)}$, (Vg =5V, Tj=300K).

Shown in fig.4.18(a) and 4.18(b) are the impact of p-base doping concentrations on the current saturation and on – state voltage drop $V_{ce(sat)}$. It is obvious in fig.4.18(a) that current saturation lowers with the increase in p-base doping but at the cost of increase in the conduction losses as shown in Figure.4.18(b). In the contrary, the proposed IGBT can lower the saturation current to about 345A from 427A of the conventional IGBT at the junction temperature T_j=300K without increasing the p-base doping concentration. The increased depth of the p+ emitter redirect the flow of holes into the p+ emitter instead of the channel inversion layers. This therefore reduces substantially the hole current density under the n+ emitter thus, weakening conductivity modulation in the channel inversion layer and then lowers bipolar carrier flow into the N-drift region and subsequently lead to lowering of current saturation significantly as shown in fig.4.16. It is obvious in fig.4.19 that the hole density in the channel inversion layer of the proposed IGBT is significantly lowered when compared to that of the conventional IGBT. This is due to redirection of flow of holes into the increased depth of the p+ emitter during turn-on and this is what account for effective lowering of conductivity modulation in the channel inversion layers.

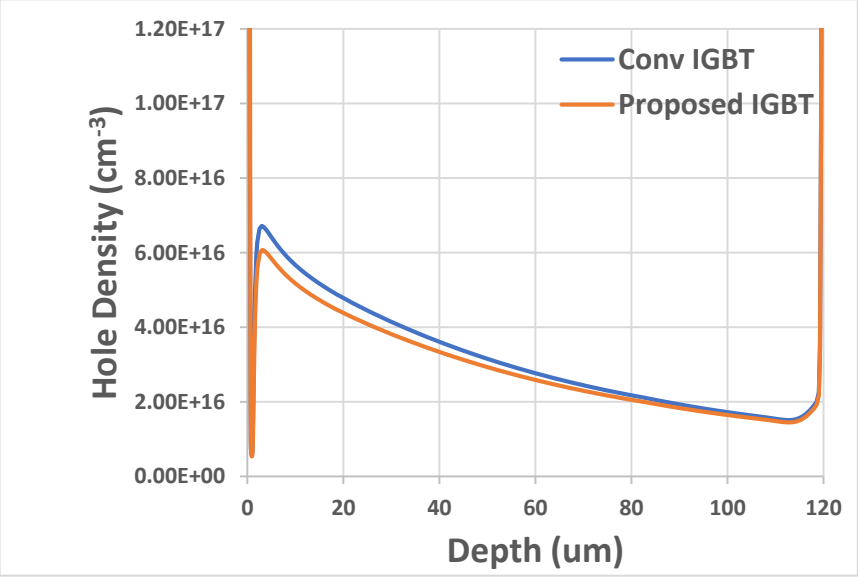


Figure.4.19: Comparison of hole carrier density in the conventional and proposed IGBT (Tj =300K)

Additionally, owing to the lowering of conductivity modulation in the mesa region for the proposed IGBT, the junction barrier between the p-base and the n+ emitter show no decrease as the collector voltage increases as shown in fig.4.17(b) above. As a result, the current saturation behaviours are significantly improved when compared to that of the conventional

narrow mesa IGBT. Furthermore, the proposed IGBT structure can successfully lower conductivity modulation in the channels and allow current saturation characteristics even when the mesa width is reduced to about 0.6um, the results are almost the same as that of fig.4.16 above.

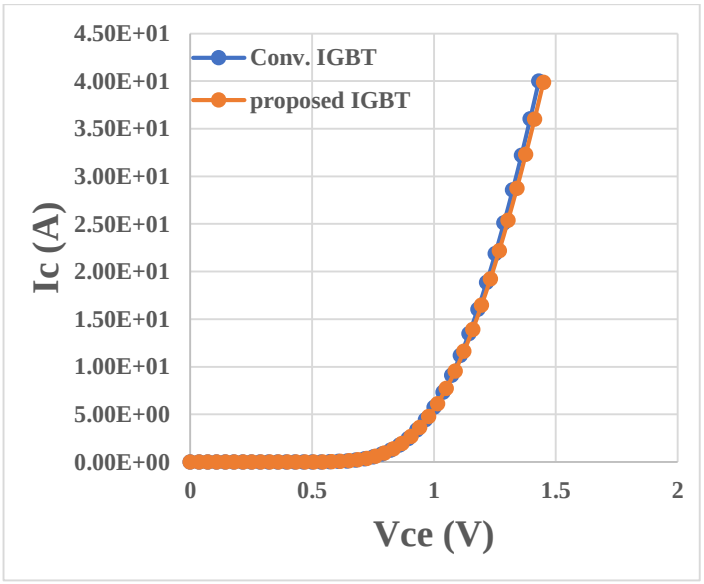


Figure 4.20: I-V Characteristics of both the proposed and the conventional TIGBT at T_j=300K

Shown in fig.4.20 is a comparison of the I-V characteristics of the proposed and the conventional scaled TIGBT. It became obvious that the proposed trench IGBT has the same on – state voltage drop $\boldsymbol{V_{ce(sat)}}$ like that of the conventional scaled k=3 device. The on – state voltage drop of the proposed device is not affected by the channel resistance.

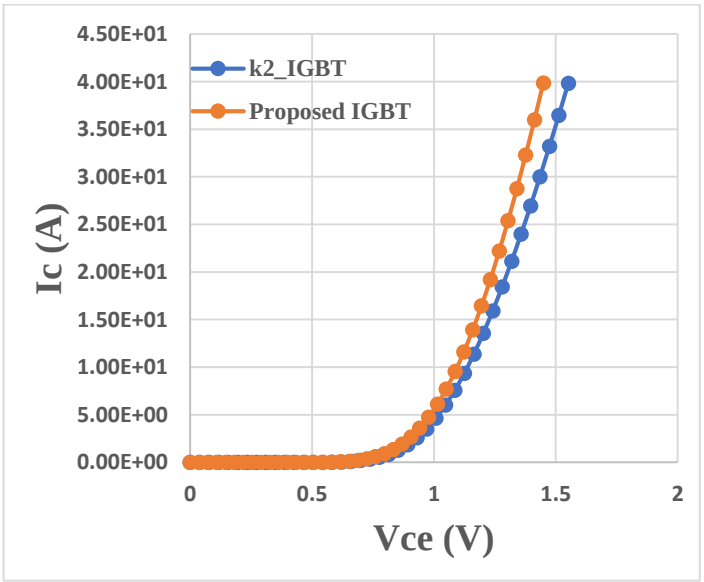


Figure .4.21: I-V Characteristics of the proposed TIGBT and k2_TIGBT at T_j=300K

Considering the above fig.4.21 show that the proposed TIGBT has an improved I-V characteristics compared to k2-IGBT due to increased carrier injection (IE) as a result of scaling.

4.8 Inductive Turn-off Switching for the Scaled and Proposed Scaled Devices

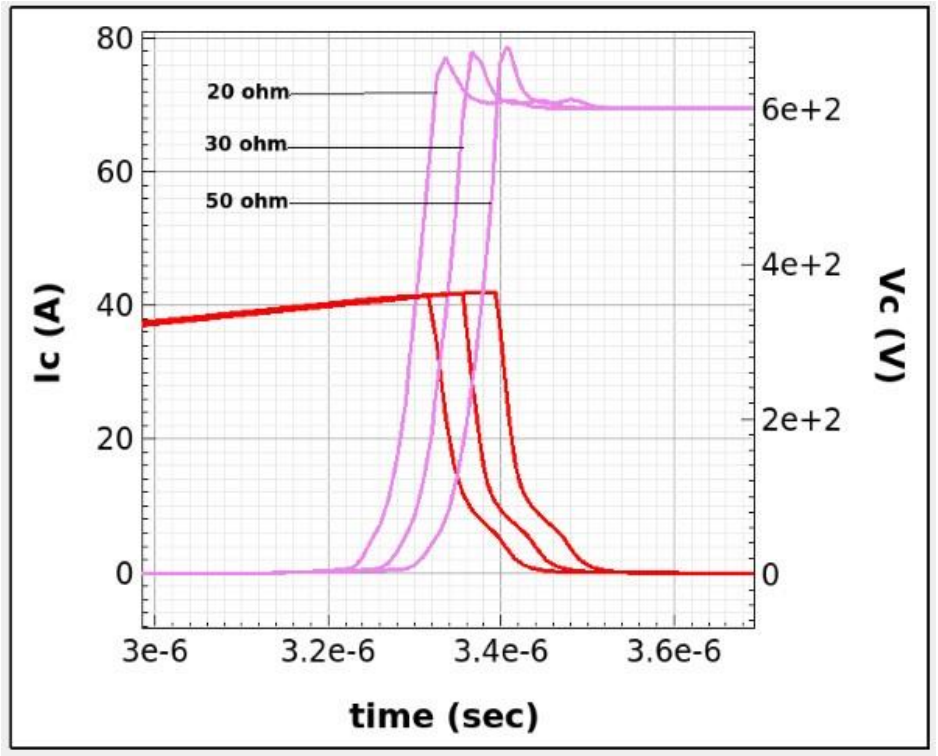


Figure 4.22: Turn-off switching characteristics for the conventional scaled device k=3 at T_j=300K, Vg=5V, V_{DC} =600V, I_C = 40A, Rg = 20Ω, 30Ω & 50Ω.

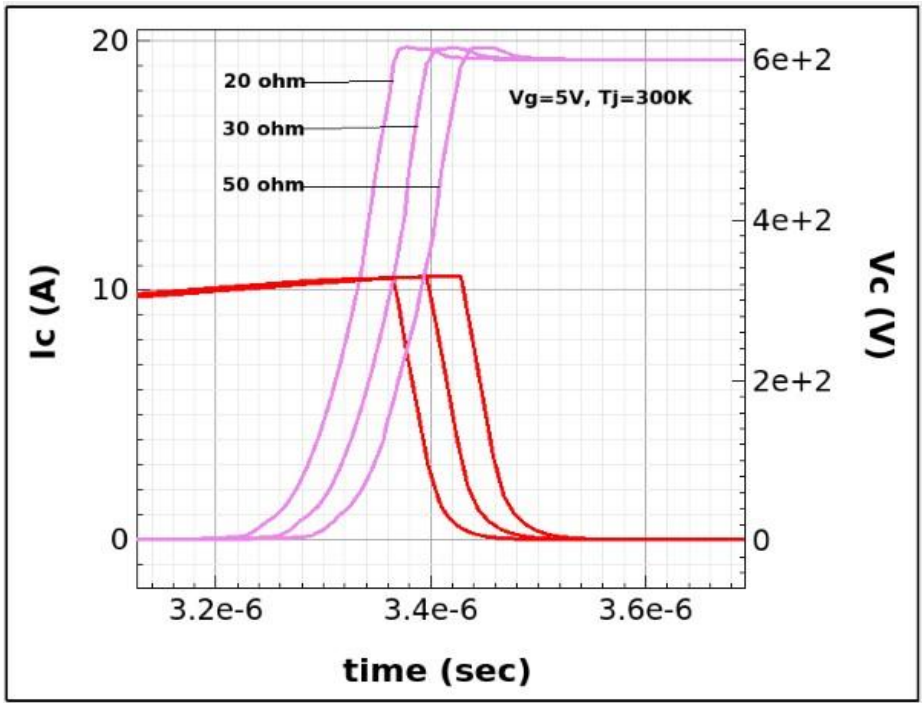


Figure 4.23: Turn-off switching characteristics for the conventional scaled device k=3 at T_j=300K, Vg=5V, V_{DC} =600V, I_C = 10A, R_g = 20Ω, 30Ω & 50Ω.

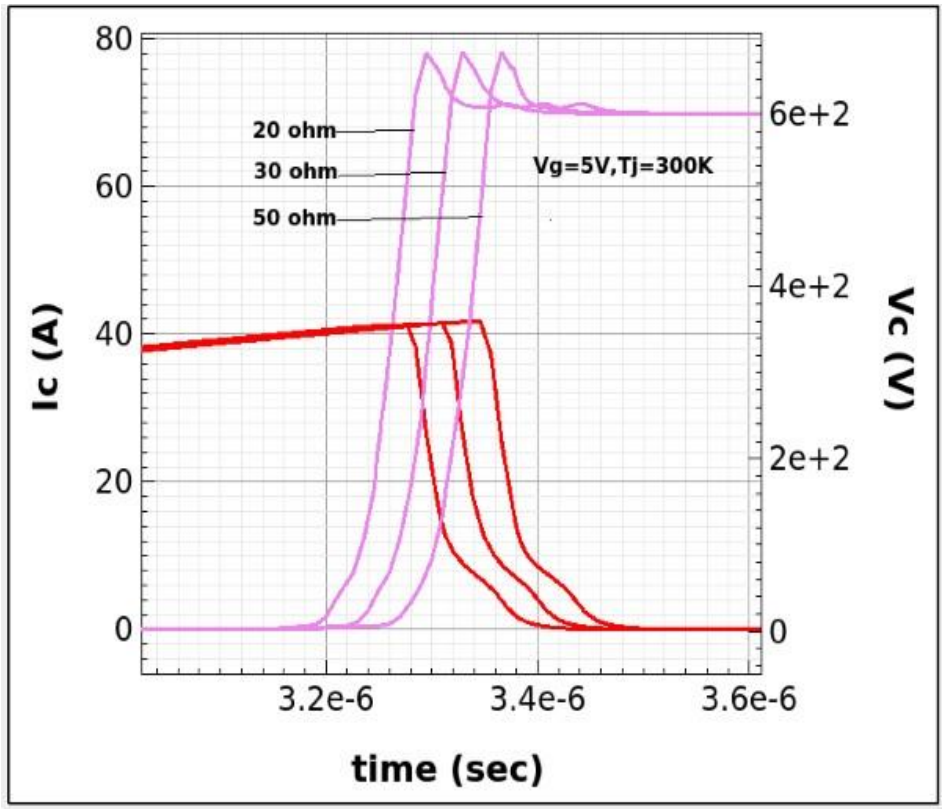


Figure 4.24: Turn-off switching characteristics for the proposed scaled k=3 device at T_j=300K, Vg=5V, V_{DC} =600V, I_C = 10A, $R_g = 20\Omega, 30\Omega$ & 50Ω.

As collector voltage V_{ce} rises instantaneously during turn-off, the depletion region in the IGBT expand and the internal electric field sweeps out the excess stored carriers. In addition, owing to the extension of depletion region, the miller capacitance C_{gc} decreases resulting to the increase in dV/dt. Given the inductive switching circuit in the previous section, the simulated waveforms of turn-off behaviour of a 1.2kV field-stop (FS) Trench IGBT featuring scaled device k=3 and proposed scaled device k=3 at different values of gate resistance and load current are shown in the figures 4.22, 4.23 and 4.24 above along with the given parameters for the simulation such as bus voltage, gate voltage, varied load current and gate resistance as well as junction temperature.

As can be seen in the Fig.4.22, the lowering of dV/dt at the gate resistance of R_g=20ohm is due to dynamic avalanche. This is because due to the rapid increase in collector voltage V_{ce} at turnoff, the excess holes stored in the device accumulate at the bottom of the trench gate as it does not have sufficient time to be removed from the device [58]. This gives rise to a peak electric field strength which surpasses the critical electric field (E_c). Consequently, dynamic avalanche occur which generates more charges that decrease dV/dt. However, for the fig.4.23, the load current was lowered to 10A and it is noticed that there is no occurrence of dynamic

avalanche, meaning that high current density is capable of causing dynamic avalanche which was the case in fig.4.22. Also, in the figure 4.24, which is the turn – off switching waveform for the proposed device, there is also no noticeable occurrence of dynamic avalanche even with the load current of 40A. This is because majority of the holes are evacuated through the increased length of p+ emitter during the device turn – off.

Table 4.3: Comparison of turn-off losses E_{off} between conventional scaled and proposed scaled devices.

Gate Resistance (Ohm)	E_{off} for conventional scaled device k=3 (mJ)	E_{off} for Proposed scaled device k=3 (mJ)
20	1.5	1.5
30	1.5	1.5
50	1.5	1.5

Table 4.3 above show comparison of turn-off losses E_{off} between the conventional scaled and proposed scaled devices. It is shown in the table that the turn-off losses for the both devices are the same as well their on-sate voltage drop as shown in the figure 4.20. Thus, the proposed scaled device manifesting a superior $V_{ce(sat)}$-E_{off} trade-off relationship and also show a robustness to short circuit condition as will be shown in the next section.

4.9 Short Circuit Performance for the Scaled and Proposed Scaled Devices

The device tends to operate in the saturation mode under short circuit condition and the collector current is limited by the V_{GE} voltage value. It is this limiting factor that determine the IGBTs robustness against short circuit currents for at least a limited period. In this work, initial temperature is considered to be 400 K, DC bias voltage is 800 V, collector current I_C is 40A and the thermal resistance from the collector electrode to ambient is 0.8 cm^2 K/W. Thermal resistance is a measure of a device resistance to heat flow. In other word, it is the reciprocal of thermal conductance which is the ability to conduct heat. The equation below evaluates thermal resistance.

$$R_t = \frac{L}{KA} \tag{4.2}$$

Where K is the material conductivity [$W.m^{-1}.K^{-1}$]

L is the plane thickness [m] and A is the plane area [m^2]

The stray inductances which govern the behaviour of the device came as a result of connecting wires and its value is considered to be 60nH. The device is expected to withstand high supply voltage and its saturation current simultaneously for some period of time during short circuit condition and as a consequence, junction temperature which is the IGBT device temperature during conduction increases rapidly with time owing to excessive power dissipation. Thus, employing mixed–mode, 2-dimentional device and circuit simulation tools (TCAD Sentaurus), the short circuit current and voltage waveforms simulated under DC link voltage of 800 V for both the scaled and the proposed scaled devices are shown in the figures below.

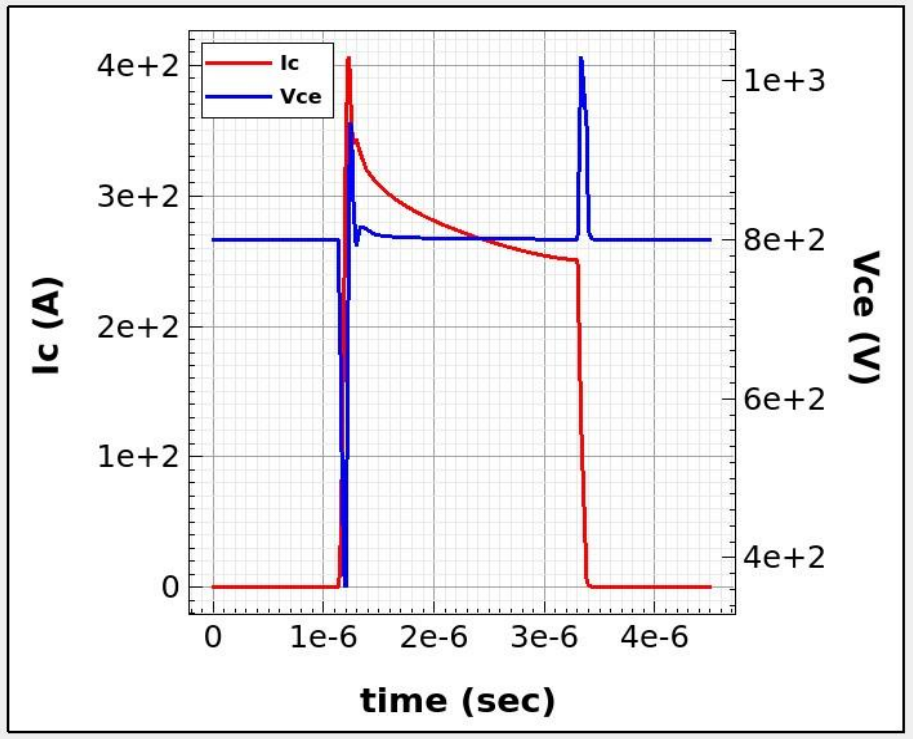


Figure 4.25: Short circuit performance of the conventional scaled device k=3 device, T_j=400K, Collector current I_C = 40A, V_{ce}=800V, V_{ge}=5V.

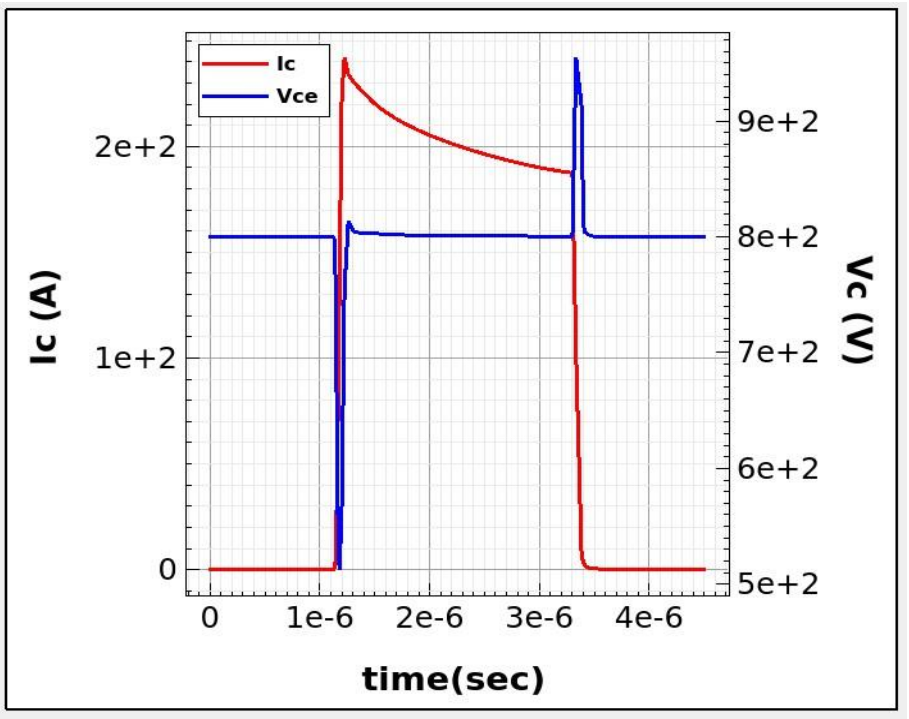


Figure 4.26: Short circuit performance of the proposed scaled device k=3, T_j=400K, Collector current I_C= 40A, V_{ce}=800V, V_{ge}=5V.

Shown in fig.4.25 and 4.26 are the comparison of the waveforms of the short circuit performance of the scaled and the proposed scaled devices k=3. The simulation condition is the same as in the conventional device k=1 treated in the previous section. The conditions are as follows: Collector current of 40 A, DC bus voltage of 800 V, stray inductance of 60nH and also same p-collector and n-buffer doping concentrations of $3x10^{17}$ cm^{-3} and $2x10^{16}$ cm^{-3} respectively.

For the 2 cases of the short circuit performance mentioned above such as the conventional scaled and the proposed scaled devices k=3, the collector voltage V_{CE} rises to the bus voltage before turn-on as the gate voltage V_{GE} =0V. The devices turned on after about 1us and the conventional scaled device k=3 in fig.4.25 turned on with a current spike whereas the proposed scaled device in fig.4.26 turned on with a much lowered current peak. The current spike in the conventional scaled device is due to overshoot in the gate voltage V_{GE} as shown Fig.4.27 and high transconductance. The gate voltage overshoot is induced due to the enhancement in the conductivity modulation in the channel inversion layer [16].

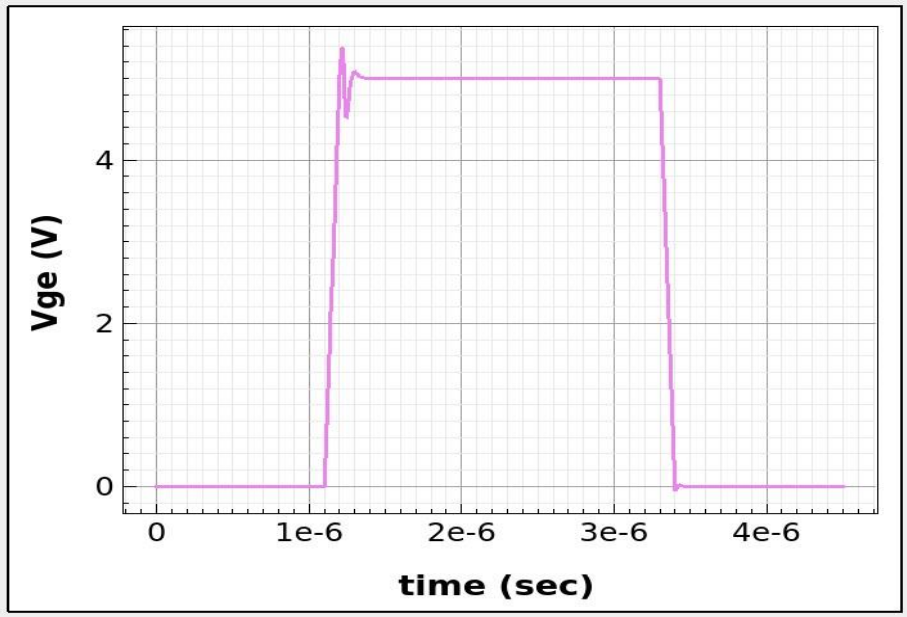


Figure 4.27: Gate voltage waveform during short circuit condition for the conventional scaled device k=3 device, $V_{GE} = 5V$, T_j=400K.

After turning on for the above 2 cases, the short circuit current I_{SC} decreases with time as shown in the figures above. The decrease in short circuit current after turn-on is due to reduction in electron and hole mobilities because of self-heating of the device and after about 3.5 us, the devices turn off with an inductive peak voltage which is determined by the equation below:

$$V_{DC} + L_S \frac{d_i}{d_t} \tag{4.3}$$

Where V_{DC} is the DC bus voltage, L_S is the stray inductance of the circuit and $L_S \frac{d_i}{d_t}$ is the voltage drop at the inductor. The inductive peak voltage generated during short circuit turn-off is accompanied by a corresponding rise in device temperature as have explained in the previous section, the direct relationship between the inductive voltage rise at turn-off and device temperature. Considering the 1.2 kV voltage rating of the devices, the high peak collector voltage at turn off for the conventional scaled device k=3 as well as its high short circuit current (spike) at turn on are clear manifestations of poor short circuit performance due to its scaled mesa width. Ideally, for reliability purposes, the short circuit current at high junction temperature is supposed to be maintained at about 4 times the operating current of the device and a controlled peak collector voltage at turn off.

However, for the proposed scaled device k=3 in fig.4.26, it is obvious in the figure that the lowered peak short circuit current at turn on which approximate to its value at saturation region and the controlled peak collector voltage at turn off show an improved short circuit safe operating area (SCSOA). The peak short circuit current I_{sc} of the proposed scaled device and

that of the conventional scaled device approximate their value at current saturation characteristics shown in fig.4.17 above. This therefore confirms that short circuit current operates at its current saturation region. The improved short circuit performance of the proposed scaled device is further validated considering its gate voltage waveform shown in fig.4.28 below as against the gate voltage overshoot of the conventional scaled device shown in the fig.4.27 above. The gate voltage waveform of the proposed scaled device displays an insignificant overshoot compared with that of the conventional scaled device. This is largely due to weak conductivity modulation which occur in the channel inversion layer owing to the increased depth of the p+ emitter as explained previously.

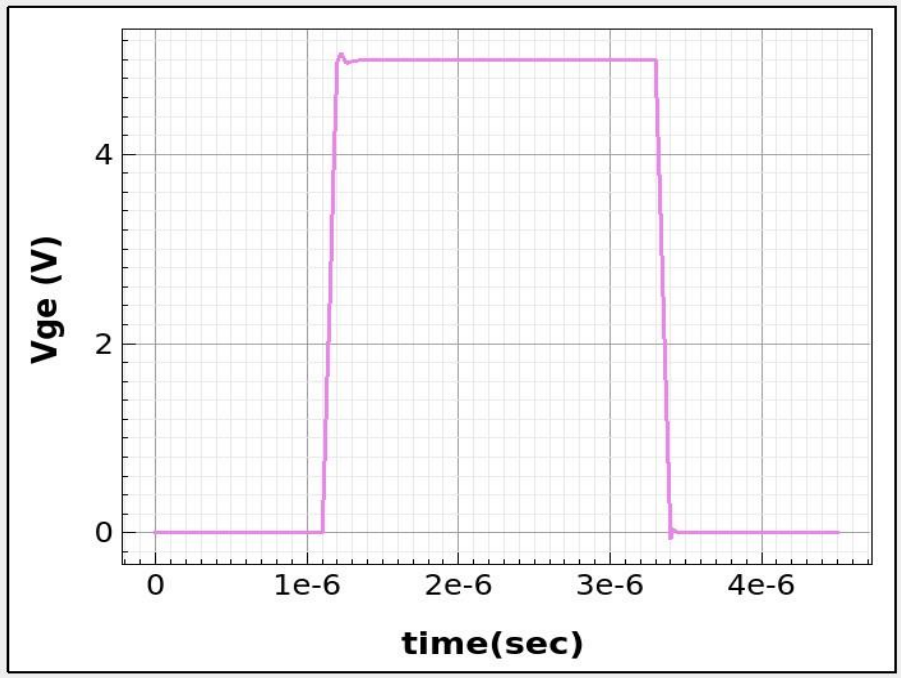


Figure 4.28: Gate voltage waveform during short circuit condition for the proposed scaled device k=3 device, $V_{GE} = 5V$, T_j=400K.

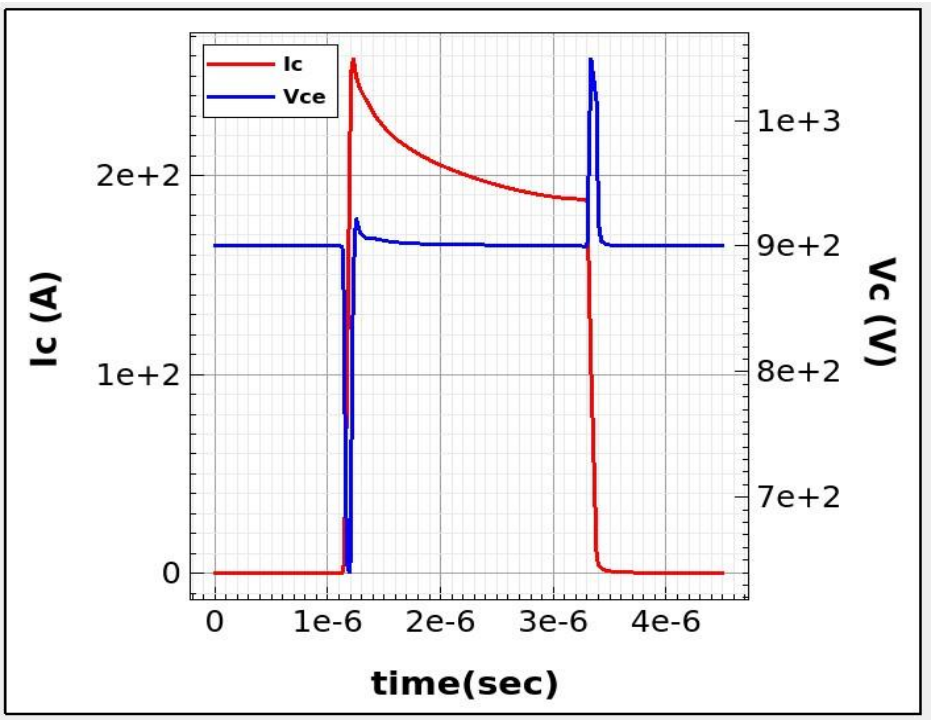


Figure 4.29: Short circuit performance of the proposed scaled device k=3, T_j=400 K, collector current I_C= 40 A, V_{ce}=900V, V_{ge}=5 V.

Figure 4.29 showed that the proposed scaled device displays a high degree of ruggedness against short circuit condition by stepping up the bus voltage up to 900 V. It is shown in the figure that the device survived the short circuit pulse when the bus voltage is increased to 900 V.

4.10 Overcoming CIBL Effect in the Scaled Device

It has been shown in the proposed structure that the collector induced barrier lowering (CIBL) effect in the conventional scaled device can be successfully overcome. Fig.4.17(a) and 4.17(b) above show the potential distribution within the mesa region for the conventional scaled and the proposed devices. Considering the conventional scaled device, the potential in the n+ emitter rises with the increase in collector voltage as majority of the hole current flows in the n+ emitter leading to conductivity modulation in the mesa region (channel inversion layer). This result to increased current flow and consequently, non-saturation of the current characteristics and poor short circuit performance as have discussed in the previous sections.

In the other hand, the increased depth of p+ layer of the proposed scaled device structure controls the potential increase in the n+ emitter. This is because most of the hole current this time flow towards the p+ layer. This causes conductivity modulation in the channel inversion layer to be weakened as only few holes current flow within the n+ emitter making the potential within the n+ emitter to be stable and independent of the collector voltage increase. Thus, the

current saturation of the proposed scaled structure improves as shown in the Fig.4.16. The transconductance of the proposed structure is therefore lowered compared to the conventional scaled device as in the Fig.4.30. Thus, the short circuit performance of the proposed structure is improved as already explained above.

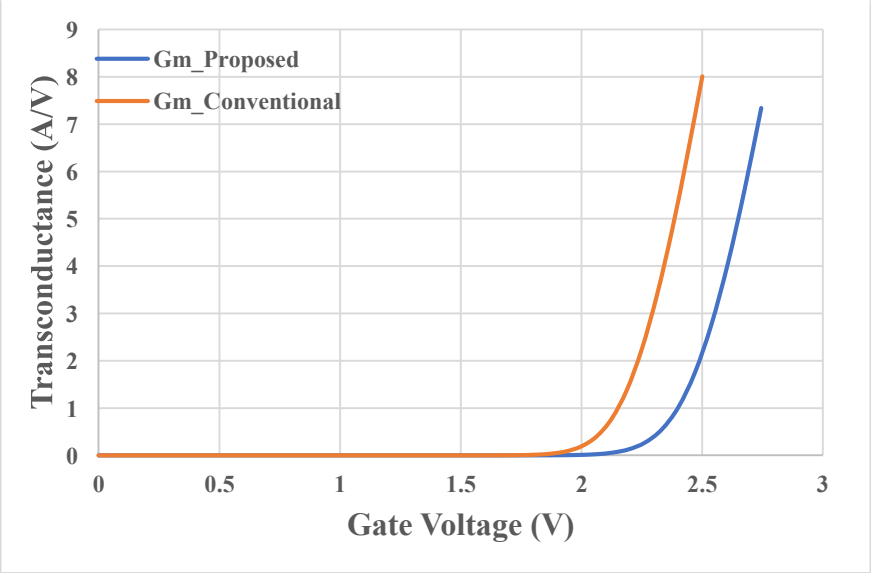


Figure 4.30: Transconductance of the conventional scaled and proposed devices at T_j=300K

CHAPTER FIVE

CONCLUSION AND FUTURE WORK PROPOSAL

5.1 Conclusion of the Thesis

In conclusion, a 1.2kV Field Stop Trench Insulated Gate Bipolar Transistor (TIGBT) was modelled, characterised, and scaled while applying the scaling principle available in the literature. Sentaurus Technology Computer Aided Design (TCAD) which houses a program designed for semiconductor physics Finite Element Method (FEM) simulation was employed in developing and characterising the Trench IGBT model. Relevant literature was acquired regarding FEM simulations in addition to the physics involve in the operation of an IGBT.

Static and dynamic characteristics of the developed model was deeply evaluated, and a comparison was made against the scaled device, and it was confirmed that the scaled device k=3 have an improved performance in terms of its IV characteristics among other characteristics which is due to enhanced Injection Enhancement (IE) effect.

However, the scaled device k=3 has poor short circuit performance due to Collector Induced Barrier Lowering (CIBL) effect caused by conductivity modulation in the channel inversion layer. In this work, a scaled device k=3 was proposed in which the depth of the p+ emitter in the p-base region was increased from 0.08um to 0.24um and that enhances the CIBL by clamping down the conductivity modulation in the channel inversion layer thereby achieving current saturation and consequently an improved short circuit safe operating area. However, the on-state voltage drops and turn-off losses are maintained for the proposed and conventional scaled devices.

5.2 Future Work Proposal

The research undertaken in this thesis could be regarded as the basis for further research. The following are outlined for further studies:

(1) To further increase the reliability of the Trench IGBTs during short circuit event, it is necessary to develop a more reliable gate driver that can always arrest triggering of the gate – emitter voltage overshoot and oscillation.

(2) Impurities in different layers of the IGBT was not considered in the designed model. Owing to imperfect manufacturing process such impurities do exist in the real IGBTs. Also, oxide charge traps exist which do have an impact on the threshold voltage during

the manufacturing process of the gate oxide. Therefore, there is need to consider those elements that are capable of adjusting the operation of the device from the ideal case and an analysis should be carried out to ascertain the impact of the impurities on the device operation during short circuit event.

(3) Eliminating dynamic avalanche in order to ensure high current density and safe operation in Trench IGBTs is very paramount.

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APPENDIX

Appendix A

A1: Code for generating a 1.2kV Trench IGBT model structure

```
;-----------------------------------------------------------------------;

; Structure definition ;

;-----------------------------------------------------------------------;

(sdegeo:set-default-boolean "BAB")

(define Xmax 30)

(define Ymax 120)

(sdegeo:create-rectangle (position 12.3 -0.3 0.0 ) (position 13.3 4.5 0.0 ) "PolySi" "R.PolyGate")

(sdegeo:fillet-2d (find-vertex-id (position 12.3 4.5 0)) 0.25)

(sdegeo:fillet-2d (find-vertex-id (position 13.3 4.5 0)) 0.25)

(sdegeo:create-rectangle (position 12.2 -0.3 0.0 ) (position 13.4 4.6 0.0 ) "Oxide" "R.Gox")

(sdegeo:fillet-2d (find-vertex-id (position 12.2 4.6 0)) 0.25)

(sdegeo:fillet-2d (find-vertex-id (position 13.4 4.6 0)) 0.25)

(sdegeo:create-rectangle (position 16.4 -0.3 0.0 ) (position 17.4 4.5 0.0 ) "PolySi" "R.PolyGate")

(sdegeo:fillet-2d (find-vertex-id (position 16.4 4.5 0)) 0.25)

(sdegeo:fillet-2d (find-vertex-id (position 17.4 4.5 0)) 0.25)

(sdegeo:create-rectangle (position 16.3 -0.3 0.0 ) (position 17.5 4.6 0.0 ) "Oxide" "R.Gox")

(sdegeo:fillet-2d (find-vertex-id (position 16.3 4.6 0)) 0.25)

(sdegeo:fillet-2d (find-vertex-id (position 17.5 4.6 0)) 0.25)

(sdegeo:create-rectangle (position 13.4 -0.3 0.0 ) (position 13.6 0.0 0.0 ) "Oxide" "R.Spacer")

(sdegeo:create-rectangle (position 16.1 -0.3 0.0 ) (position 16.3 0.0 0.0 ) "Oxide" "R.Spacer")

(sdegeo:create-rectangle (position 0.0 -0.3 0.0 ) (position 12.2 0.0 0.0 ) "Oxide" "R.Spacer" )

(sdegeo:create-rectangle (position 17.5 -0.3 0.0 ) (position Xmax 0.0 0.0 ) "Oxide" "R.Spacer")

(sdegeo:create-rectangle (position 0.0 0.0 0.0 ) (position Xmax Ymax 0.0 ) "Silicon" "R.Si" )


;-----------------------------------------------------------------------;

; Profiles
```

```
;-----------------------------------------------------------------;
; ------ PolyGate ------
(sdedr:define-constant-profile "Const.PolyGate"
 "PhosphorusActiveConcentration" 1e+21 )
(sdedr:define-constant-profile-material "PlaceCD.PolyGate"
 "Const.PolyGate" "PolySi" )
; ------ Substrate ------
(sdedr:define-constant-profile "Const.Substrate"
 "PhosphorusActiveConcentration" 5e+13 )
(sdedr:define-constant-profile-material "PlaceCD.Substrate"
 "Const.Substrate" "Silicon" )
; ------ P-base ------
(sdedr:define-refinement-window "Win.Pbase" "Line"
 (position -1.0 0.0 0.0)
 (position 50.0 0.0 0.0) )
(sdedr:define-gaussian-profile "Gauss.Pbase"
 "BoronActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 2e17
 "ValueAtDepth" 2e16 "Depth" 2.0
 "Gauss"  "Factor" 0.4)
(sdedr:define-analytical-profile-placement "PlaceAP.Pbase"
 "Gauss.Pbase" "Win.Pbase" "Both" "NoReplace" "Eval")
; ------ N-plus ------
(sdedr:define-refinement-window "BaseLine.nplus1" "Line"
 (position 13.4 0.0 0.0)
 (position 14.4 0.0 0.0) )
(sdedr:define-gaussian-profile "Impl.nplus1prof"
 "ArsenicActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 1e20
 "ValueAtDepth" 2e19  "Depth" 0.25
 "Erf"  "Length" 0.02)
```

```
(sedr:define-analytical-profile-placement "Impl.nplus1" "Impl.nplus1prof"
"BaseLine.nplus1" "Both" "NoReplace" "Eval")
(sedr:define-refinement-window "BaseLine.nplus2" "Line"
 (position 15.4 0.0 0.0)
 (position 16.4 0.0 0.0) )
(sedr:define-gaussian-profile "Impl.nplus2prof"
 "ArsenicActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 1e20
 "ValueAtDepth" 2e19  "Depth" 0.25
 "Erf"  "Length" 0.02)
(sedr:define-analytical-profile-placement "Impl.nplus2"
 "Impl.nplus2prof" "BaseLine.nplus2" "Both" "NoReplace" "Eval")
; ------ P-plus ------
(sedr:define-refinement-window "BaseLine.pplus" "Line"
 (position 14.4 0.0 0.0)
 (position 15.4 0.0 0.0) )
(sedr:define-gaussian-profile "Impl.pplusprof"
 "BoronActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 1e20
 "ValueAtDepth" 2e19  "Depth" 0.25
 "Erf"  "Length" 0.02)
(sedr:define-analytical-profile-placement "Impl.pplus"
 "Impl.pplusprof" "BaseLine.pplus" "Both" "NoReplace" "Eval")
; ------ N-buffer ------
(sedr:define-refinement-window "Win.Nbuffer" "Line"
 (position -1.0 Ymax 0.0)
 (position 50.0 Ymax 0.0) )
(sedr:define-gaussian-profile "Gauss.Nbuffer"
 "ArsenicActiveConcentration"
"PeakPos" 0.0  "PeakVal" 2e16
"ValueAtDepth" 1e15 "Depth" 10.0
"Gauss"  "Factor" 0.1)
```

```
(sedr:define-analytical-profile-placement "PlaceAP.Nbuffer"
 "Gauss.Nbuffer" "Win.Nbuffer" "Both" "NoReplace" "Eval")
; ------ P-anode ------
(sedr:define-refinement-window "Win.Panode" "Line"
 (position -1.0 Ymax 0.0)
 (position 50.0 Ymax 0.0) )
(sedr:define-gaussian-profile "Gauss.Panode"
 "BoronActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 3e17
 "ValueAtDepth" 3e16 "Depth" 0.7
 "Gauss"  "Factor" 0.1)
(sedr:define-analytical-profile-placement "PlaceAP.Panode"
 "Gauss.Panode" "Win.Panode" "Both" "NoReplace" "Eval")
;-----------------------------------------------------------------------;
; Electrodes
;-----------------------------------------------------------------------;
(sdegeo:define-contact-set "Emitter"   4  (color:rgb 1 0 0 ) "##" )
(sdegeo:define-contact-set "Collector" 4  (color:rgb 1 0 0 ) "==" )
(sdegeo:define-contact-set "Gate"      4  (color:rgb 1 0 0 ) "<><>" )
(sdegeo:define-2d-contact (find-edge-id (position 14.9  0.0 0.0)) "Emitter")
(sdegeo:define-2d-contact (find-edge-id (position 10.0 Ymax 0.0)) "Collector")
(sdegeo:define-2d-contact (find-edge-id (position 12.8 -0.3 0.0)) "Gate")
(sdegeo:define-2d-contact (find-edge-id (position 16.9 -0.3 0.0)) "Gate")
;-----------------------------------------------------------------------
; Meshing
;-----------------------------------------------------------------------;
(sedr:define-refinement-window "RW.SiTop"
"rectangle"
(position 0.0 0.0 0.0 )
(position Xmax 10.0 0.0 ))
(sedr:define-refinement-size "Ref.SiTop"
```

```
  1.00  1.00  0.0
  0.05  0.05  0.0)
(sdedr:define-refinement-function "Ref.SiTop"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "RefPlace.SiTop"
 "Ref.SiTop" "RW.SiTop" )
(sdedr:define-refinement-window "RW.SiMid"
 "rectangle"
 (position 0.0  10.0 0.0 )
 (position Xmax 85.0 0.0 ))
(sdedr:define-refinement-size "Ref.SiMid"
  3.00  5.00  0.0
  0.30  0.30  0.0 )
(sdedr:define-refinement-function "Ref.SiMid"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "RefPlace.SiMid"
 "Ref.SiMid" "RW.SiMid" )
(sdedr:define-refinement-window "RW.SiBot"
 "rectangle"
 (position 0.0 85.0 0.0 )
 (position Xmax Ymax 0.0 ))
(sdedr:define-refinement-size "Ref.SiBot"
  3.0  1.0  0.0
  0.2  0.2  0.0)
(sdedr:define-refinement-function "Ref.SiBot"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "RefPlace.SiBot"
"Ref.SiBot" "RW.SiBot" )
(sdedr:define-refinement-window "RW.Mesa"
"rectangle"
 (position 11.0 0.0 0.0 )
```

```
 (position 19.0 3.8 0.0 ))
(sdedr:define-refinement-size "Ref.Mesa"
  0.25  0.25  0.0
  0.03  0.03  0.0)
(sdedr:define-refinement-function "Ref.Mesa"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "RefPlace.Mesa"
 "Ref.Mesa" "RW.Mesa" )
;-----------------------------------------------------------------
; Saving BND file
(sdeio:save-tdr-bnd (get-body-list) "@tdrboundary/o@")
; Save CMD file
(sdedr:write-cmd-file "@commands/o@")
(system:command "snmesh -offset n@node@_msh")
```

A2: Code for generating a 1.2kV Scaled FS-Trench IGBT Structure

```
;-----------------------------------------------------------------;
; Structure definition ;
;-----------------------------------------------------------------;
(sdegeo:set-default-boolean "BAB")
(define Xmax 30)
(define Ymax 120)
(sdegeo:create-rectangle (position 13.43 -0.3 0.0 ) (position 14.43 1.5 0.0 ) "PolySi" "R.PolyGate")
(sdegeo:fillet-2d (find-vertex-id (position 13.43 1.5 0)) 0.25)
(sdegeo:fillet-2d (find-vertex-id (position 14.43 1.5 0)) 0.25)
(sdegeo:create-rectangle (position 13.40 -0.3 0.0 ) (position 14.46 1.53 0.0 ) "Oxide" "R.Gox")
(sdegeo:fillet-2d (find-vertex-id (position 13.40 1.53 0)) 0.25)
(sdegeo:fillet-2d (find-vertex-id (position 14.46 1.53 0)) 0.25)
(sdegeo:create-rectangle (position 15.21 -0.3 0.0 ) (position 16.21 1.5 0.0 ) "PolySi" "R.PolyGate")
(sdegeo:fillet-2d (find-vertex-id (position 15.21 1.5 0)) 0.25)
```

```
(sdegeo:fillet-2d (find-vertex-id (position 16.21 1.5 0)) 0.25)
(sdegeo:create-rectangle (position 15.18 -0.3 0.0 )  (position 16.24 1.53 0.0 ) "Oxide"  "R.Gox")
(sdegeo:fillet-2d (find-vertex-id (position 15.18 1.53 0)) 0.25)
(sdegeo:fillet-2d (find-vertex-id (position 16.24 1.53 0)) 0.25)
(sdegeo:create-rectangle (position 14.46 -0.3 0.0 ) (position 14.56 0.0 0.0 ) "Oxide" "R.Spacer" )
(sdegeo:create-rectangle (position 15.08 -0.3 0.0 ) (position 15.18 0.0 0.0 ) "Oxide" "R.Spacer" )
(sdegeo:create-rectangle (position 0.0 -0.3 0.0 )  (position 13.40 0.0 0.0 ) "Oxide"  "R.Spacer")
(sdegeo:create-rectangle (position 16.24 -0.3 0.0 ) (position Xmax 0.0 0.0 ) "Oxide" "R.Spacer" )
(sdegeo:create-rectangle (position 0.0 0.0 0.0 )  (position Xmax Ymax 0.0 ) "Silicon" "R.Si" )

;-----------------------------------------------------------------------;
; Profiles
;-----------------------------------------------------------------------;
; ------ PolyGate ------
(sdedr:define-constant-profile "Const.PolyGate"
 "PhosphorusActiveConcentration" 1e+21 )
(sdedr:define-constant-profile-material "PlaceCD.PolyGate"
 "Const.PolyGate" "PolySi" )

; ------ Substrate ------
(sdedr:define-constant-profile "Const.Substrate"
 "PhosphorusActiveConcentration" 5e+13 )
(sdedr:define-constant-profile-material "PlaceCD.Substrate"
 "Const.Substrate" "Silicon" )
; ------- P-base --------
(sdedr:define-refinement-window "Win.Pbase" "Line"
 (position -1.0 0.0 0.0)
 (position 50.0 0.0 0.0) )
(sdedr:define-gaussian-profile "Gauss.Pbase"
 "BoronActiveConcentration"
```

```
 "PeakPos" 0.0  "PeakVal" 4.3e17
 "ValueAtDepth" 4.3e16 "Depth" 0.6
 "Gauss"  "Factor" 0.4)
(sdedr:define-analytical-profile-placement "PlaceAP.Pbase"
 "Gauss.Pbase" "Win.Pbase" "Both" "NoReplace" "Eval")
; ------ N-plus ------
(sdedr:define-refinement-window "BaseLine.nplus1" "Line"
 (position 14.46 0.0 0.0)
 (position 14.71 0.0 0.0) )
(sdedr:define-gaussian-profile "Impl.nplus1prof"
 "ArsenicActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 1e20
 "ValueAtDepth" 2e19  "Depth" 0.08
 "Erf"  "Length" 0.02)
(sdedr:define-analytical-profile-placement "Impl.nplus1"
 "Impl.nplus1prof" "BaseLine.nplus1" "Both" "NoReplace" "Eval")
(sdedr:define-refinement-window "BaseLine.nplus2" "Line"
 (position 14.96 0.0 0.0)
 (position 15.21 0.0 0.0) )
(sdedr:define-gaussian-profile "Impl.nplus2prof"
 "ArsenicActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 1e20
 "ValueAtDepth" 2e19  "Depth" 0.08
 "Erf"  "Length" 0.02)
(sdedr:define-analytical-profile-placement "Impl.nplus2"
 "Impl.nplus2prof" "BaseLine.nplus2" "Both" "NoReplace" "Eval")
; ------ P-plus ------
(sdedr:define-refinement-window "BaseLine.pplus" "Line"
 (position 14.71 0.0 0.0)
(position 14.96 0.0 0.0) )
(sdedr:define-gaussian-profile "Impl.pplusprof"
```

```
 "BoronActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 1e20
 "ValueAtDepth" 2e19  "Depth" 0.08
 "Erf"  "Length" 0.02)
(sdedr:define-analytical-profile-placement "Impl.pplus"
 "Impl.pplusprof" "BaseLine.pplus" "Both" "NoReplace" "Eval")

; ------ N-buffer ------
(sdedr:define-refinement-window "Win.Nbuffer" "Line"
 (position -1.0 Ymax 0.0)
 (position 50.0 Ymax 0.0) )
(sdedr:define-gaussian-profile "Gauss.Nbuffer"
 "ArsenicActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 2e16
 "ValueAtDepth" 1e15 "Depth" 10.0
 "Gauss"  "Factor" 0.1)
(sdedr:define-analytical-profile-placement "PlaceAP.Nbuffer"
 "Gauss.Nbuffer" "Win.Nbuffer" "Both" "NoReplace" "Eval")

; ------ P-anode ------
(sdedr:define-refinement-window "Win.Panode" "Line"
 (position -1.0 Ymax 0.0)
 (position 50.0 Ymax 0.0) )
(sdedr:define-gaussian-profile "Gauss.Panode"
 "BoronActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 3e17
 "ValueAtDepth" 3e16 "Depth" 0.7
 "Gauss"  "Factor" 0.1)
(sdedr:define-analytical-profile-placement  "PlaceAP.Panode"  "Gauss.Panode"  "Win.Panode"
"Both" "NoReplace" "Eval")

;-----------------------------------------------------------------;
```

```
; Electrodes
;-----------------------------------------------------------------;
(sdegeo:define-contact-set "Emitter"   4  (color:rgb 1 0 0 ) "##" )
(sdegeo:define-contact-set "Collector" 4  (color:rgb 1 0 0 ) "==" )
(sdegeo:define-contact-set "Gate"      4  (color:rgb 1 0 0 ) "<><>" )
(sdegeo:define-2d-contact (find-edge-id (position 14.835  0.0 0.0)) "Emitter")
(sdegeo:define-2d-contact (find-edge-id (position 10.0 Ymax 0.0)) "Collector")
(sdegeo:define-2d-contact (find-edge-id (position 14.0 -0.3 0.0)) "Gate")
(sdegeo:define-2d-contact (find-edge-id (position 15.71 -0.3 0.0)) "Gate")
;-----------------------------------------------------------------
; Meshing
;-----------------------------------------------------------------;
(sdedr:define-refinement-window "RW.SiTop"
 "rectangle"
 (position 0.0 0.0 0.0 )
 (position Xmax 16.0 0.0 ))
(sdedr:define-refinement-size "Ref.SiTop"
  1.00  1.00  0.0
  0.02  0.02  0.0)
(sdedr:define-refinement-function "Ref.SiTop"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "RefPlace.SiTop"
 "Ref.SiTop" "RW.SiTop" )
(sdedr:define-refinement-window "RW.SiMid"
 "rectangle"
 (position 0.0  16.0 0.0 )
(position Xmax 85.0 0.0 ))
(sdedr:define-refinement-size "Ref.SiMid"
  3.00  6.00  0.0
  0.50  1.00  0.0 )
(sdedr:define-refinement-function "Ref.SiMid"
```

```
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "RefPlace.SiMid"
 "Ref.SiMid" "RW.SiMid" )
(sdedr:define-refinement-window "RW.SiBot"
 "rectangle"
 (position 0.0 85.0 0.0 )
 (position Xmax Ymax 0.0 ))
(sdedr:define-refinement-size "Ref.SiBot"
  1.0  1.0  0.0
  0.2  0.2  0.0)
(sdedr:define-refinement-function "Ref.SiBot"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "RefPlace.SiBot"
 "Ref.SiBot" "RW.SiBot" )
 (sdedr:define-refinement-window "RW.Mesa"
 "rectangle"
 (position 16.4 0.0 0.0 )
 (position 18.8 2.8 0.0 ))
(sdedr:define-refinement-size "Ref.Mesa"
  0.10  0.20  0.0
  0.01  0.01  0.0)
(sdedr:define-refinement-function "Ref.Mesa"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "RefPlace.Mesa"
 "Ref.Mesa" "RW.Mesa" ) ;-----------------------------------------------------------------------
; Saving BND file
(sdeio:save-tdr-bnd (get-body-list) "@tdrboundary/o@")
; Save CMD file
(sdedr:write-cmd-file "@commands/o@")
(system:command "snmesh -offset n@node@_msh")
```