The University Of Sheffield.

Investigation into the operation of the single-stage current source charge-pump power factor correction system

Ali Navabi Naeini

Thesis submitted in partial fulfilment of the requirements for the degree of
Master of Philosophy

The University of Sheffield
Faculty of Engineering
Electrical and Electronic Engineering Department
Electrical machines and Drives Research Group

Supervised by Prof Martin Paul Foster and Dr Jonathan Neil Davidson

30 January 2022

Abstract

This thesis describes the systematic characterisation a power factor correction system for mains powered appliances. The research is motivated by increasing number of mains powered devices such as mobile phones, tablets, gaming consoles, computers, etc that require an Alternating Current (AC) to Direct Current (DC) power converters. It is crucial to design these power converters as small, efficient, inexpensive and with high power quality as possible. This thesis focuses on a power factor corrector system that offers all the mentioned advantages.

This work starts by defining the types of power in AC systems and the power quality parameters. In addition, the benefits of having high power quality and how it is mandated by the law are reported. The existing systems to improve power quality and/or provide Power Factor Correction (PFC) along with advantages and disadvantages of each system are demonstrated. The full comparison of the PFC systems is provided, and it is shown why the Current Source Charge Pump PFC (CSCP-PFC) is a convenient method to implement for AC-DC conversion systems.

A review of state of the art in the CSCP-PFC systems and the technologies underpinning this system are reported. In addition, the inconsistencies in the existing research on this system are discussed.

A novel mathematical model based on Fundamental Mode Approximation (FMA) and describing function of the PFC system is demonstrated and verified. A subsequent investigation using this model has determined that the model requires further modification fully capture specific details regarding the circuit's behaviour. During the course of this investigation, a novel technique was developed to extract and record the modes of operation of the system using LTspice package and MATLAB software. The findings showed that the circuit exhibits an extensive pattern of circuit configurations that cannot be easily represented by the FMA model developed.

Finally, a hardware based mode sequence identifier was implemented and used to characterise a practical CSCP-PFC platform. The operation of several converters was investigated and comparison between practical experiments and simulation made to determine whether the behaviour of the circuit could be simplified sufficiently to be conveniently modelled by using describing function techniques.

Contents

List of figures

List of tables

Declaration

I, Ali Navabi Naeini, confirm that the Thesis is my own work. I am aware of the University's Guidance on the Use of Unfair Means (www.sheffield.ac.uk/ssid/unfair-means). This work has not previously been presented for an award at this, or any other, university.

Chapter 1. Introduction

1.1 Introduction

In today's world and with modern technology, many researchers in the electrical and electronic field are focused on designing more efficient, smaller, and less-expensive electrical appliances both in domestic and commercial products. Low-efficiency devices lead to higher power consumption hence more electrical energy needs to be produced and it increases carbon emissions. Moreover, to transmit this excess of electrical power large diameter conductors are needed and equipment such as transformers, switch gear, etc are needed to be rated for higher currents. One of the important parameters in AC powered devices is PF (Power Factor). Low PF can lead to higher reactive power consumption and hence larger currents than necessary. Larger current lead to need for higher current rated conductors as it generates more heat. Moreover, they can put stress on grid generators as it has large pulsating current spikes. Furthermore, large current spikes affects renewable power inverters, as the switches and components are needed to be rated to be able to tolerate the spikes. Therefore, it leads to need for larger and more expensive power production and distribution systems to be able to operate safely.

This thesis concentrates on circuits that shape the input current waveforms on power electronics to reduce current pulsations and improve power factor. This chapter introduces the concept of PF and how it is determined from the current waveform. The reasons for why PFC (Power Factor Correction) is needed and the consequences of not having PFC is provided. Finally, different types of PFC approaches and advantages and disadvantages of each system is discussed.

1.2 Power consumption in Alternating Current circuits

The power consumption of AC powered appliances is not as straight forward as DC powered devices. The power consumption of in DC circuits is the product of voltage and current. However, in AC circuits it is different due to the phase difference between the voltage and current waveforms. There are three different types of power associated with AC circuits: active power, reactive power, and the apparent (or complex) power.

1.2.1 Active power

In AC circuits, voltage and current waveforms are theoretically pure sinusoidal. If the load is purely resistive, voltage and current are in phase and there is no phase shift between them. Therefore, at every point the power which is the product of voltage and current is positive hence the direction of power does not reverse periodically. In addition, when the phase shift between voltage and current is zero only active power is transferred. Active power is the amount of power that is actually consumed in AC circuits. In other word, active power is the power that is dissipated. It is indicated by "P" and its SI unit is watts (W)(1 joule per second).

1.2.1 Reactive power

In case of reactive (Inductive or capacitive) load, voltage and current are not in phase and a phase shift exist between the two waveforms. Therefore, the instantaneous product of voltage and current is not positive all the time periodically it is negative, and the duration of the negative value depends on the value of the phase shift. This results in reactive power being transferred to the load. In simple terms, reactive power is the unused power or the imaginary power which is not used for any useful work, and it exists when there is a phase shift between voltage and current. Reactive power is indicated by "Q" and its SI unit is Volt-Ampere reactive (VAr). Reactive power is also called as 'Imaginary power' or 'Watt less power' or 'Useless power'.

1.2.2 Complex power

Apparent Power or the complex power is the combination of active power (P) and reactive power(Q).In an AC circuit, the product of the amplitudes of voltage and current is called 'Apparent Power'. It is identified by the capital letter S and It is expressed in Volt Ampere (VA).

Figure 1.1 shows the vector relationship between the AC powers that described above.

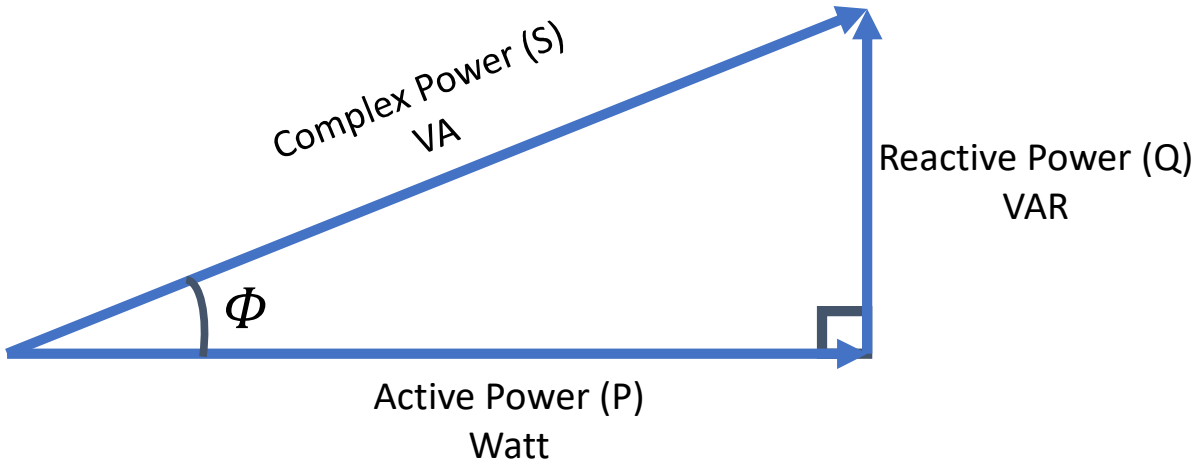


Figure 1.1: The vector relationship between the active, reactive and complex power in AC systems.

The angle ϕ in figure 1.1 is the phase shift between the voltage and current . Lastly, the active, reactive and complex power can be calculated using (1.1), (1.2) and (1.3) respectively.

$$P = |\mathrm{V}| \times |\mathrm{I}| \times \cos(\Phi) \quad (1.1)$$

$$Q = |\mathrm{V}| \times |\mathrm{I}| \times \sin(\Phi) \quad (1.2)$$

$$S = |V| \times |I| \quad (1.3)$$

The term ϕ in (1.1) and (1.2) is the phase shift angle between the voltage and current waveform. The cause of this phase shift and its effects are completely discussed in the next section. Lastly, the relationship between the AC powers is demonstrated in (1.4).

$$S^2 = P^2 + Q^2 \quad (1.4)$$

1.3 What is power factor

Power factor is a parameter for AC powered devices such as electrical motors, switch mode power supplies etc. PF shows the ratio between the active power that has flow through the device and the total power absorbed by the circuit (complex power). PF is a dimensionless value that is between 0 and 1. Higher value of power factor shows less reactive power and PF of 1 means no reactive power [1] [2].

1.3.1 Power factor in linear loads

In linear loads, or in other words passive loads, the power factor is the cosine of the phase shift between voltage waveform and the current waveform (Angle ϕ in previous section)as shown in (1.5). In capacitive loads the current waveform leads the voltage and in inductive loads the voltage leads the current. In purely resistive loads the phase shift is zero hence the power factor is 1. Figure 1.2, 1.3 and 1.4 show voltage and current waveforms for a capacitive, inductive and resistive loads respectively [1] [3] [2].

$$Power\ Factor = \cos\Phi \quad (1.5)$$

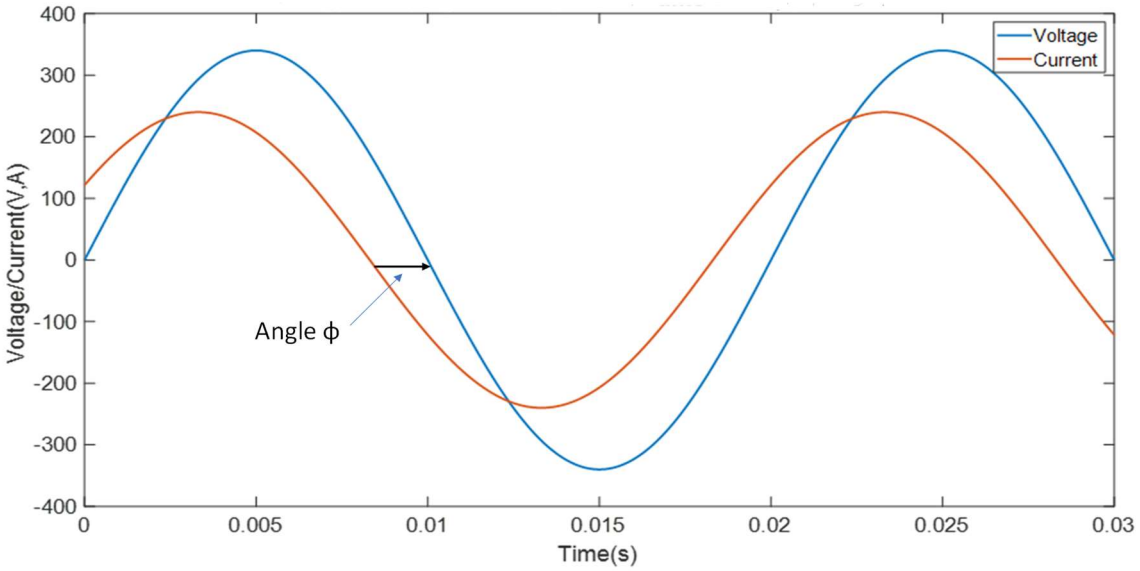


Figure 1.2:Voltage and Current waveform for a capacitive load (Leading PF).

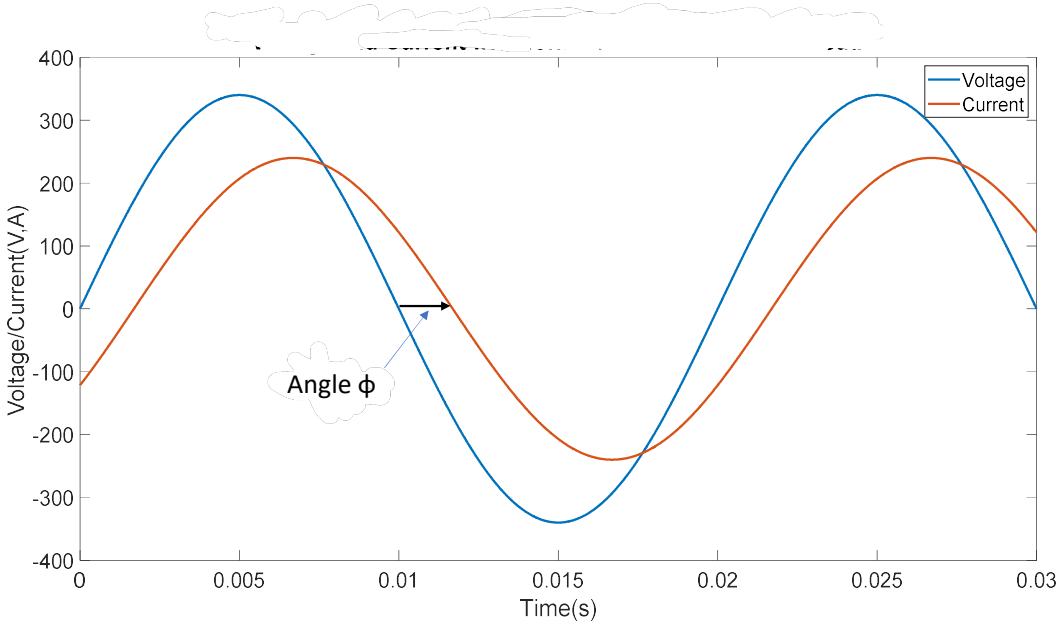


Figure 1.3: Voltage and Current waveform for a inductive load (Lagging PF).

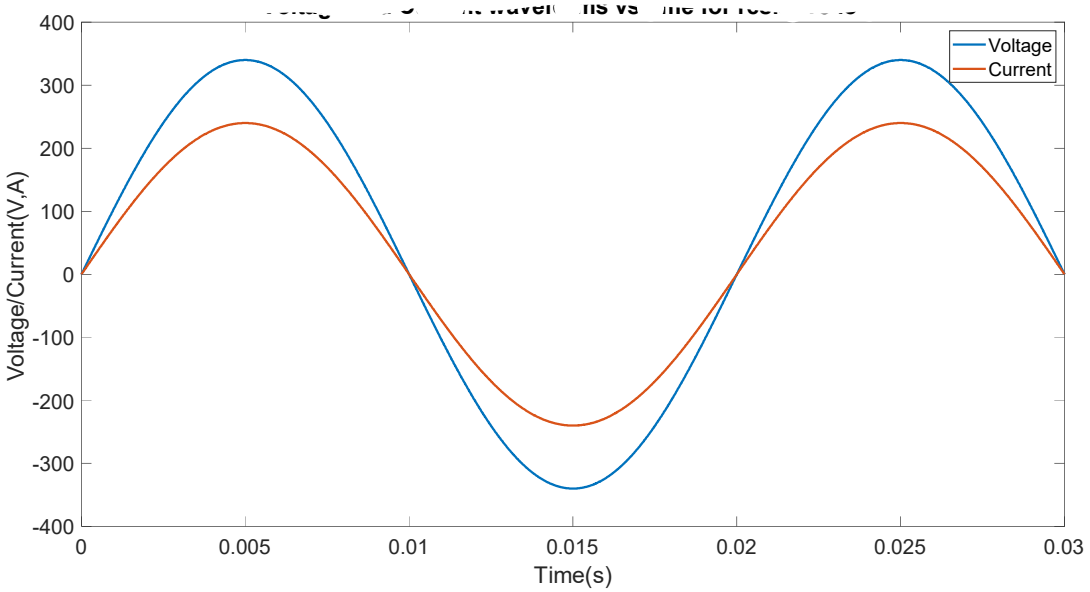


Figure 1.4: Voltage and Current waveform for a resistive load(Power factor 1).

1.3.2 Power factor in non-linear loads

Nowadays, most of all electrical appliances that are powered by AC voltages have at least one capacitive rectifier system inside them. Figure 1.4 shows two typical rectifier systems that are widely used in AC to DC conversion. In nonlinear loads such as bridge rectifiers the PF is more complex to calculate and measure. As the waveforms and quantities with non-linear loads are non-sinusoidal, the power factor is not just a function of phase shift. Therefore, PF becomes a function of two different variables. Displacement Power Factor (DPF) which is equivalent to the PF for linear loads and Total Harmonic Distortion (THD) that shows the amount of distortion in line current. THD can be calculated using (1.6) [3].

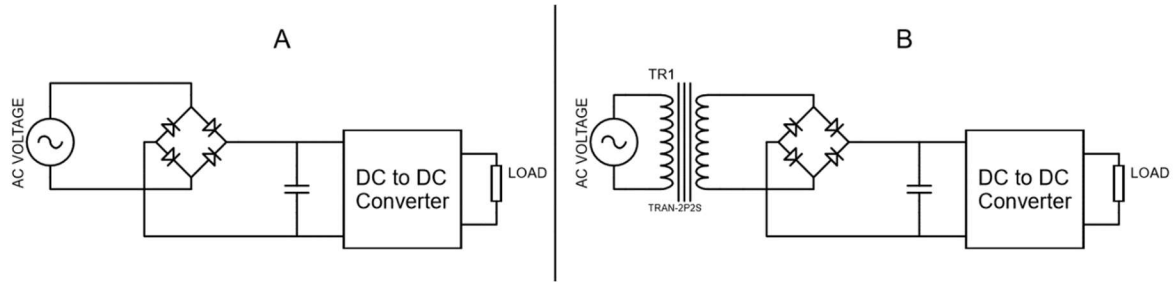


Figure 1.5:Capacitive rectifier circuits. A) without transformer. B) With Transformer.

$$THDI = \sqrt{\frac{\sum_{n=2}^{\infty} I_{sn,rms}^2}{I_{s1,rms}^2}} \quad (1.6)$$

In (1.2) THDI is the line current distortion, $I_{s1,rms}$ is the RMS (Root Mean Square) value of fundamental frequency of the current and $I_{sn,rms}$ is the RMS value of the harmonic components of the current waveform (n specifies the harmonic number). Finally, the power factor in non-linear loads can be calculated using (1.7) [3].

$$PF = \frac{1}{\sqrt{1 + THDI^2}} \times DPF \tag{1.7}$$

Figure 1.6 shows a typical current and voltage waveform for a capacitively smoothed bridge rectifier versus time. As can be seen, a current pulse occurs towards the peak of the voltage waveforms corresponding to the rectifier diodes conduction. Figure 1.7 shows the frequency domain plot of the current waveform of figure 1.6.

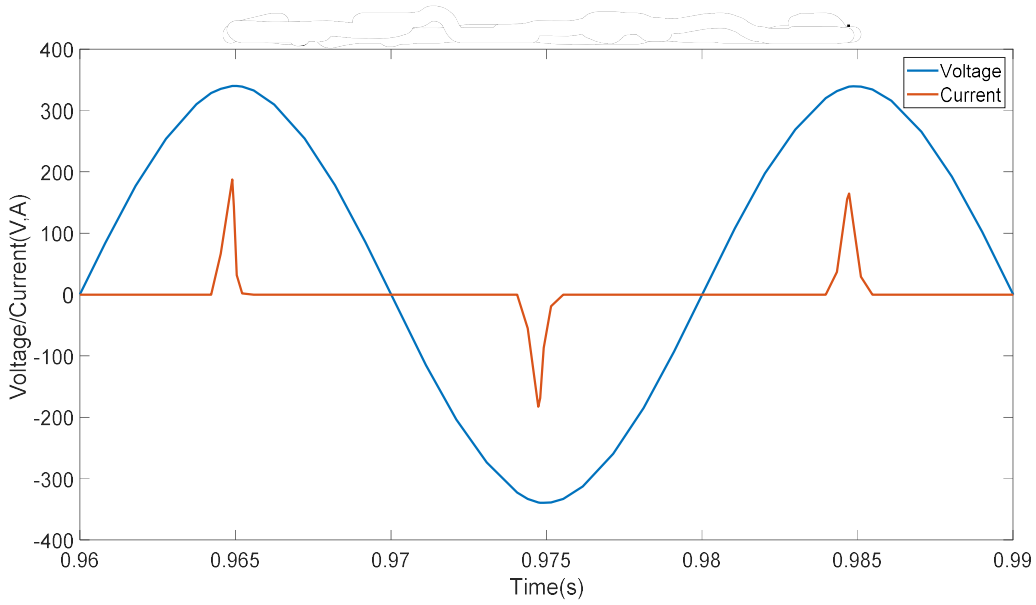


Figure 1.6: Voltage and current waveform for a non-linear capacitive rectifier load.

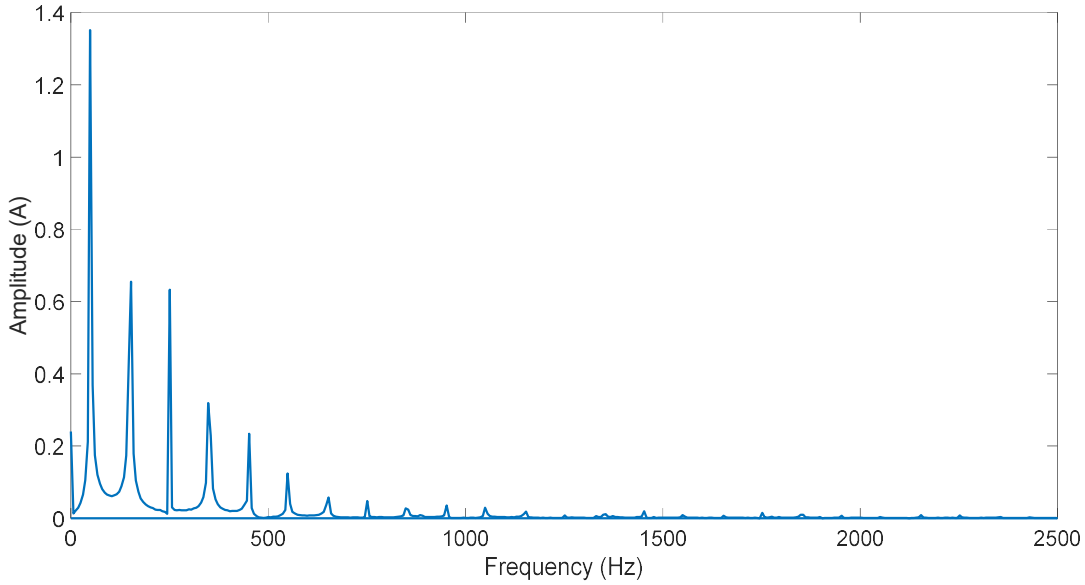


Figure 1.7:Frequency domain plot of line current of figure 1.5

1.4 Power factor and electromagnetic compatibility (EMC) standards

Apart from the benefits of having high PF, it is also mandatory by the law that devices that are powered by mains to meet power factor and harmonic emissions standards. One of the widely used standards is EN 61000-3-2. This standard applies for all the devices that are powered from 230 volts AC mains and consumes up to 16 amps per phase. This standard specifies the maximum amplitude of harmonic waveforms that a device can have on its line current. This standard states the maximum amplitude of harmonic for each harmonic (as discussed in previous section). In this standard the power consumer devices are categorized in 4 different classes(class A to D). Table 1.1 shows the categorization.

Class	Device Characteristic
Class A	Balanced 3-phase systems
Class B	Portable tool, non-professional arc welding equipment
Class C	Lighting equipment
Class D	TV, Computer, VDU(Visual Display Unit), equipment consuming< 600W

Table 1.1: Categorization of devices in EN 61000-3-2 standard

Moreover, in table 1.1 any device that does not meet any of the device characteristics, is categorized as class A. Lastly, the harmonic emission limits of the devices shown in table 1.1 are shown in table 1.2.

Harmonic order (n)	Max current class A	Max current class B	Max current class C (% of fundamental current)	Max current class D
2	1.08 Amps	1.62 A	2%	Not specified
3	2.30 A	3.45 A	30*PF %	3.4 mA/Watt
4	0.43 A	0.645 A	Not specified	Not specified
5	1.14 A	1.71 A	10%	1.9 mA/Watt
6	0.30 A	0.45 A	Not specified	Not specified
7	0.77 A	1.155 A	7%	1.0 mA/Watt
7<n<41(Even)	0.23 (8/n) A	0.345(8/n) A	Not specified	Not specified
9	0.40 A	0.6 A	5%	0.5 mA/Watt
11	0.33 A	0.495 A	3%	Not specified
13	0.21 A	0.315 A	3%	0.35 mA/Watt
14<n<40(Odd)	0.15 (15/n) A	0.225(15/n) A	3%	(3.85/n) mA/Watt

Table 1.2: The harmonic emission limitations in EN 61000-3-2.

Table 1.2 shows the maximum amplitude for each harmonic component present in the line current (n is the harmonic number). Moreover, it is mandatory by the law that all mains powered devices to meet the criteria demonstrated in table 1.2.

1.5 Why PFC is needed

Apart from the standards that are mandated by the law to implement PFC systems on mains powered appliances, low PF can have many drawbacks. Firstly, it increases the RMS value of the current hence it can cause thermal problem in transmission lines and transformers in substation and power generating stations. It also can decrease the transmission efficiency due to high conductor loss and iron loss. Low PF cause high line current distortion which can lead to stability problems in both line current and voltage. This situation can harm other line connected devices and the low PF device itself. Moreover, distorted line current consists of high frequency components which can cause EMI (electromagnetic interference). Moreover, another important parameter in AC circuits is crest factor(CF). CF is a dimensionless parameter, and it is the ratio between the peak value of the waveform and the RMS value. The CF for pure sine wave 0.707. Low PF devices usually have high crest factor as they exhibit large current spikes near the peak of the input voltage as demonstrated in figure 1.6. These waveforms with high peaks can cause false trigger events in automatic relay protection devices. Lastly, as the total power absorbed is higher than real power hence it will increase the cost of electricity for the consumer. Figure 1.8 illustrate line current at a small electricity distribution centre that low power factor devices are powered from the centre. As it is shown in figure 1.8 the line current is extremely distorted and has a high crest factor. Therefore, it is extremely important to have Power Factor Correction (PFC) systems in place for line connected devices. Different types of PFC circuitry are discussed in the next section [2].

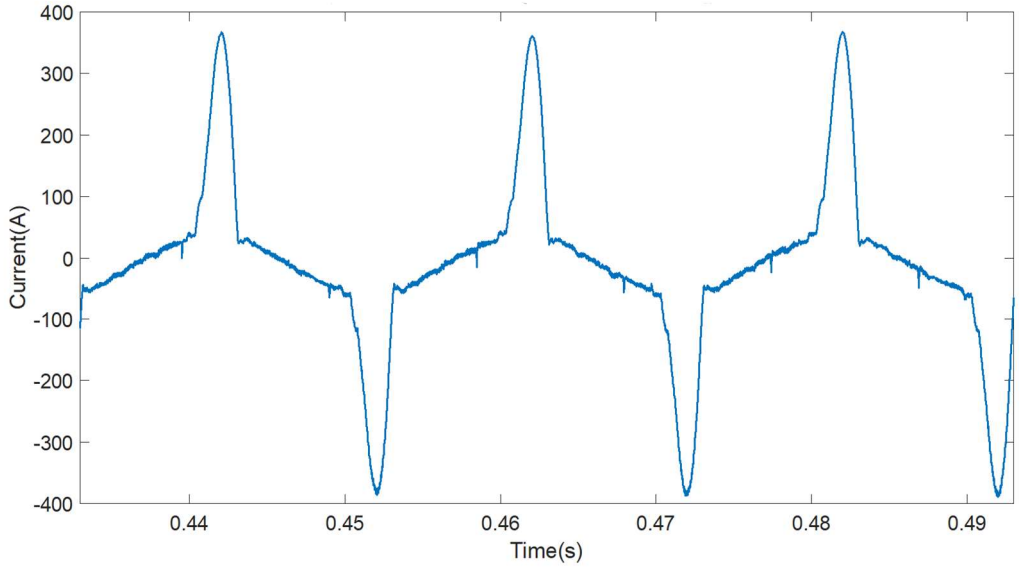


Figure 1.8:Line current at a small electricity distribution centre that low power factor devices are powered from the centre

1.6 Power Quality (PQ) measurement

In previous sections the benefits of high PF and how it is mandated by law to meet PF standards are discussed. In this section the techniques to measure PF are explained. The process of measuring power and power related quantities is called power quality measurement. For PQ measurements two test devices are needed. First, programmable AC power source. This device generates the AC power needed to power the DUT (Device Under Test). The main purpose of using this device is to have sinusoidal voltage with lowest THD possible, as distorted input voltage to the DUT causes an increase in line current THD, hence unreliable data measurement. The second benefit of using programmable AC power source is that it allows for a full control over voltage and frequency of the input voltage to the DUT. As in mains voltage there are no control over frequency, voltage and THDV. For this work the used programmable AC source is ASR-2100 from GW-Instek. The ASR-2100 can output AC voltage from 0 to 350 volts RMS, with maximum current of 10 amps with THD of less than 0.1%.

The next test equipment is a power quality analyser. This equipment measures the voltage across and current through the DUT, then processes the signals to provide different results such as THDI, THDV, crest factor, power factor, harmonic measurements, etc. For this work the GPM-8310 is used as the power quality analyser. The GPM-8310 can measure THD up to 50^{th} harmonic, the current measurement accuracy can be as low as 500 µA based on the setting of the device. Lastly, this equipment meets the IEC standard for power quality measurement (IEC 62301-2011) (British regulation EN50564-2011). Figure 1.9 shows the setup of ASR-2100 and GPM-8310 with a DUT for power quality measurements. This setup used later in this work.

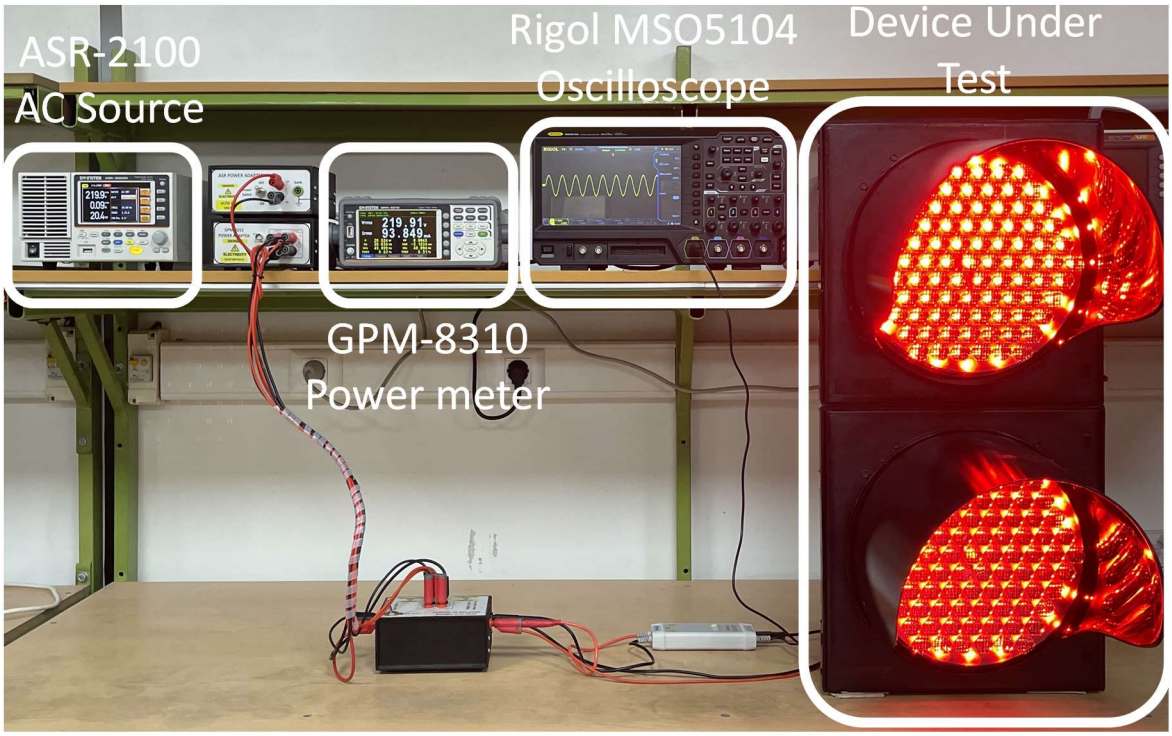


Figure 1.9: The setup of ASR-2100 and GPM-8310 with a traffic light as a DUT for power quality measurement.

1.7 Power Factor Correction

Power factor correction (PFC) is the process of improving a loads current waveform to make it more compatible with the AC supply. Traditionally heavy industry has used capacitor banks to help correct for the inductive currents drawn by electric motors. Correction here involves bringing the phase shift between the supply current and voltage close to zero. There are many types of PFC approaches that have their own advantages and drawbacks. It is not possible to find best PFC system as each of them is suitable for different applications. All PFC systems try to shape the current waveform as close as possible to the input voltage shape and in phase with it. There are two types of PFC, the first one is passive PFC that only uses passive components to shape the input current and the second type is active. The active PFC has active devices such as diodes and MOSFETs to correct the power factor. Generally, passive PFC circuits are much simpler to design and less expensive comparing to the active type PFC. However, passive PFC topologies do not usually meet the PFC standards requirements specially in high power devices. Therefore, in many applications active PFC has to be used.

1.7.1 Passive PFC: LC input filter

The most simple and inexpensive PFC circuit is a passive LC filter that is placed in the input of the power converter. These filters are usually second order low pass filters and attenuate the high frequency components of the input current hence the THD will be decreased and the

EMI emissions of the system will be reduced. This PFC approach is simple to design and inexpensive. However, on the other hand filters cannot precisely shape the input current and reduce the THD to the standard levels. Figures 1.10 shows a typical LC PFC system and figure 1.11 shows the input voltage and current for the LC filter PFC. In figure 1.11 the current waveform has a capacitive phase shift. This is caused by the capacitive rectifier. The Input LC filter is designed to have a near zero phase shift; however, the effect of the smoothing capacitor has not been taken into account and has caused a capacitive phase shift.

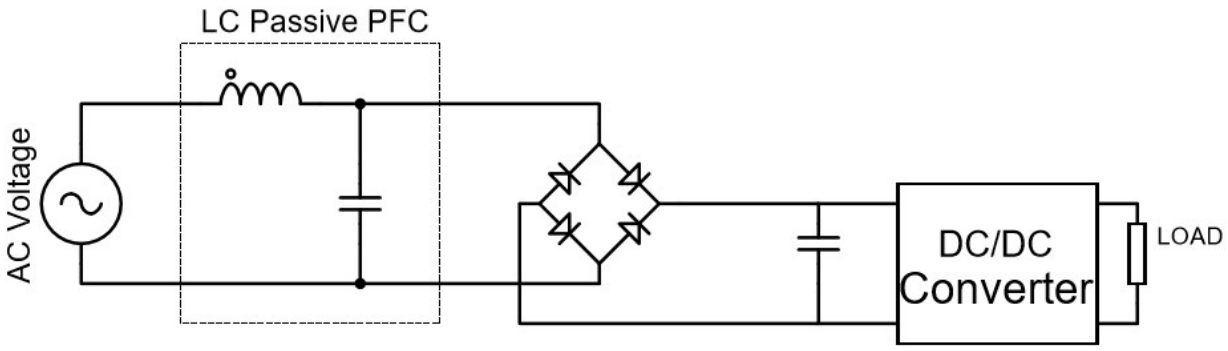


Figure 1.10:Passive LC PFC example circuit.

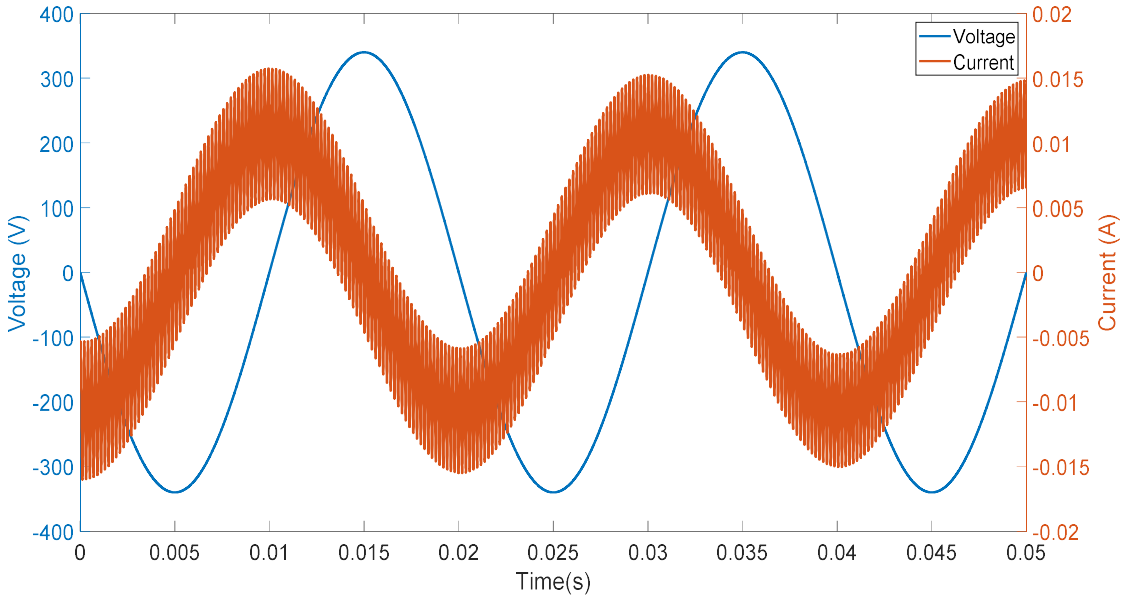


Figure 1.11:Line voltage and current waveform of a LC PFC circuit.

1.7.2 Valley fill PFC

Another type of PFC is valley fill PFC. This type of PFC is suitable for low power applications and where high DC ripple voltage can be tolerated. The schematic of valley fill PFC is shown in figure 1.12 [4].

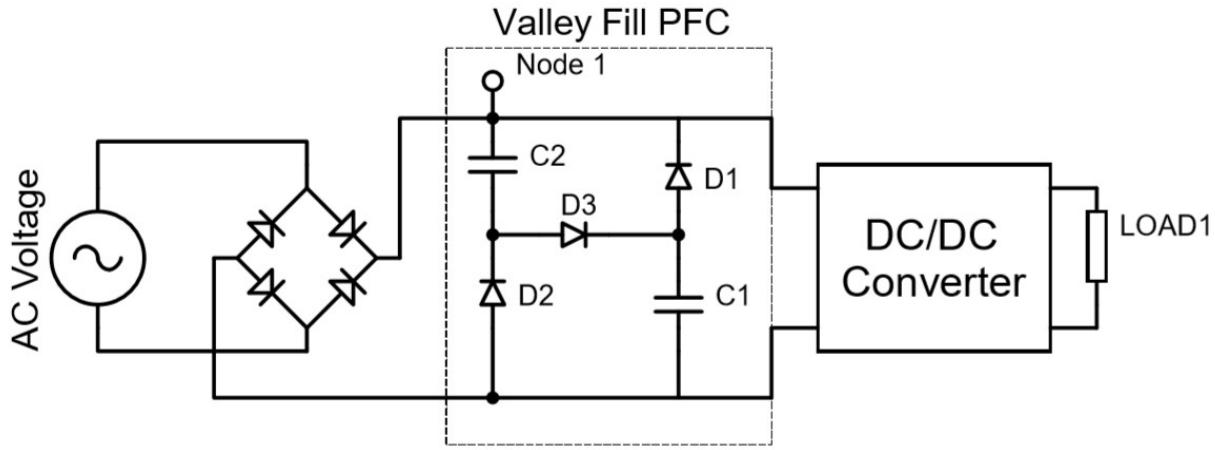


Figure 1.12:Valley fill PFC.

The PFC operation of this circuit is done by C1 and C2 charging to half of the peak of the input voltage as when they are charging diode D3 conducts hence C1 and C2 are series capacitors. The voltage at node 1 of the figure 1.12 is a full wave rectified sine wave. When the voltage at node 1 is rising the capacitors C1 and C2 will charge in series and D3 is forward biased. Therefore, the voltage of each capacitor will be half of the peak of the input voltage. Then, when the voltage at node 1 is decreasing the capacitors C1 and C2 will start to discharge through diodes D1 and D2 and D3 is turned off until when the voltage reaches half of the peak of the input voltage. This order of charging and discharging of capacitors C1 and C2 will shape the current to near sinusoidal shape and hence improve the power factor. This system is simple to design and inexpensive. However, on the other hand it is only suitable for low power applications. Moreover, as C1 and C2 charge and discharge to peak of the input voltage and half of it, it produces high voltage ripples on the output. Therefore, the only practical DC/DC converter that can be used with this PFC system is linear series regulators. These regulators are extremely inefficient and in high power applications thay can show efficiency even lower than 50 percent. It is possible to add more diodes and capacitors to shape the line current waveform more close to sinusoidal, however, it will incease the voltage ripple to two third of the line peak voltage on the input of the regulator hence it will lead to lower efficiency and bigger regulator.Figure 1.13 shows the line voltage and current for a valley fill PFC system [4].

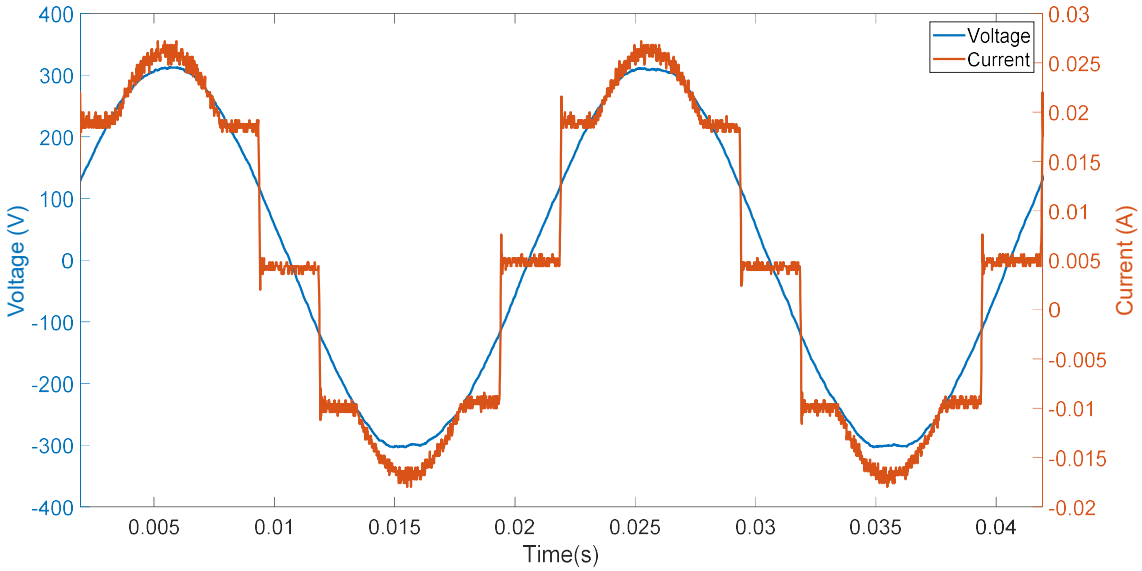


Figure 1.13: Line voltage and current waveform for a valley fill PFC system.

1.7.3 Active two stage PFC

Active two stage PFC circuits are the most common PFC systems that are used in modern technology. The DC/DC converter block provides a regulated output to the load and is fed by the PFC pre-converter which has the responsibility of shaping the AC input current. These systems can be found in many power supplies and other grid connected devices. Figure 1.14 shows the typical circuit diagram of two stage PFC system. The average of the high frequency current pulses of the PFC pre-converter is controlled to have a waveform shape similar to the input voltage. In order to attenuate the high frequency pulses that are superimposed on the line current, an LC filter is needed at the input of the circuit (before the rectifier) to attenuate the high frequency components and help to improve the power factor. Since this filter is for attenuating high frequency components it is usually smaller than that found in passive PFC systems [1] [3].

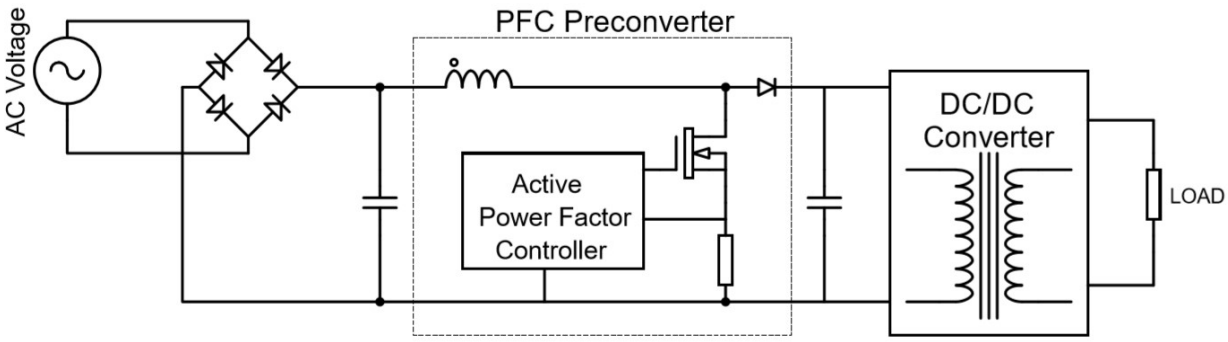


Figure 1.14: The block diagram of two stage active PFC with boost converter.

The PFC system has many advantages against other types. Firstly, it can be designed to operate with any power usage applications from couple of milliwatts to a hundreds of kilowatts. Secondly, it can correct the power factor to more 0.95 while at the same time reducing the THDI to less than 10% and it can meet all power factor standards[2]. In contrast, this type of PFC is difficult to design as they use DC/DC converter to shape the current and is difficult to control. In addition, they are more expensive as they require a high frequency inductor, power switch(MOSFET, IGBT), power diode and a controller circuitry as shown in figure 1.14. Figure 1.15 shows a line voltage and current of a 24 watts two stage PFC power supply.

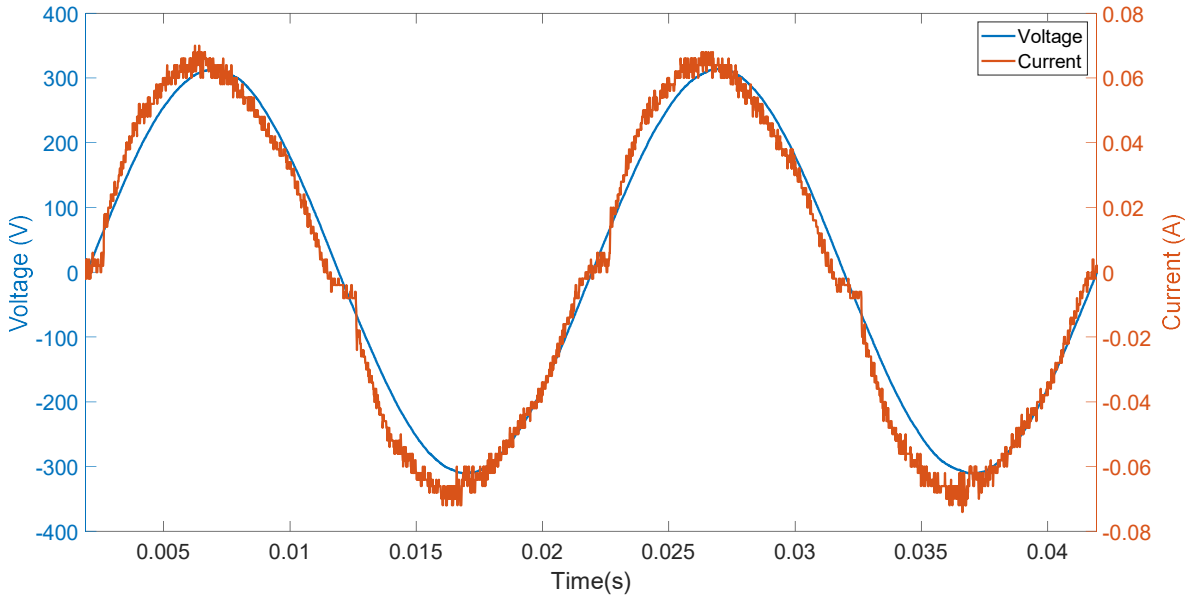


Figure 1.15: Line current and voltage for an active two stage boost pre-converter PFC system.

1.7.4 Single stage charge pump PFC

Two stage PFCs are expensive and for some applications/circuits can be omitted by adopting different approach to energy transfer. Single stage charge pump topologies are a good example. There are several circuits based on this type of PFC including voltage source charge pump, current source charge pump and hybrid charge pump. Figures 1.16, 1.17 and 1.18 show current source and voltage source and hybrid charge pump PFC systems respectively [5] [6].

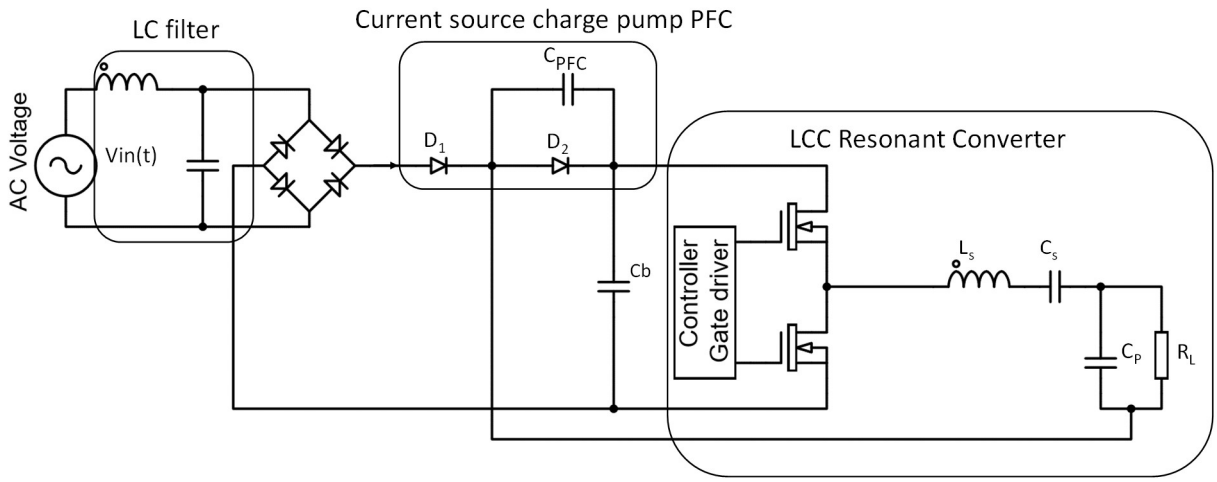


Figure 1.16:Current source single stage charge pump power factor correction circuit.

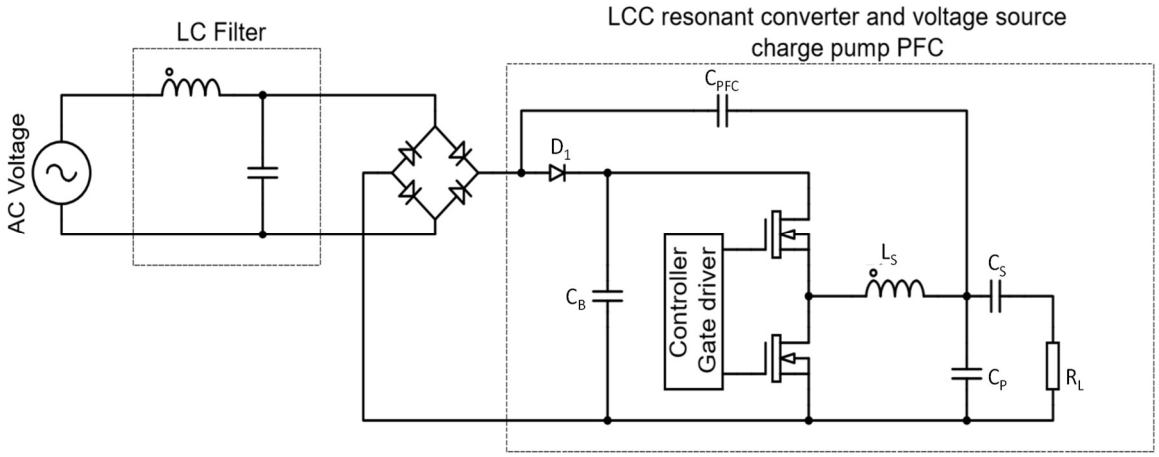


Figure 1.17: Voltage source single stage charge pump power factor correction circuit.

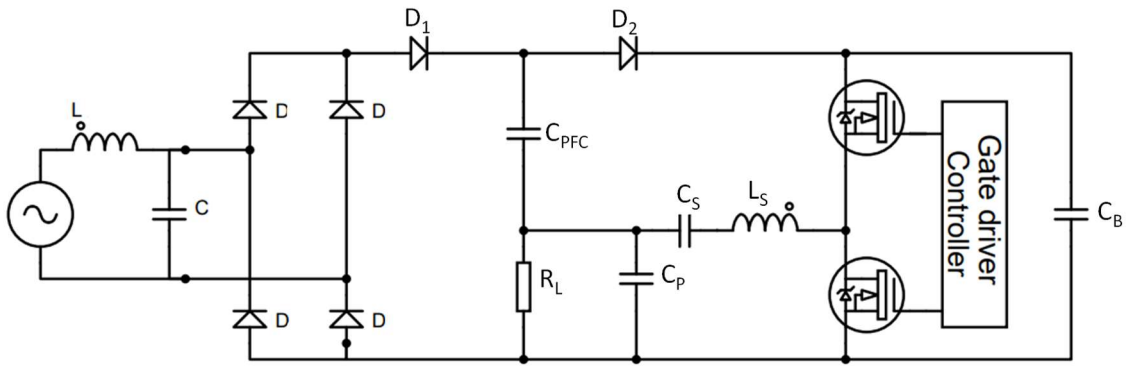


Figure 1.18: Hybrid(Voltage/Current) source single stage charge pump power factor correction circuit.

In general, all types of single stage charge pump PFC systems work on the same basis. They use high frequency current or voltage pulses to shape the input line current. These high frequency pulses are generated in the DC/DC converter (the LLC resonant converter shown in the figures) and PFC capacitor (C_{pfc}) that transfers charge at high switching frequency from the AC input to the power supply. By using the correct value for C_{pfc}, power factor higher than 0.95 and THD lower than 10% can be achieved. Moreover, as this PFC topology needs a resonant converter to operate, it can achieve high efficiency as the resonant converters offer soft switching. In switching converters, a large portion of energy losses happen in the transient period that the switch is turning on or off but in resonant converters and soft switching converters the voltage across the switch or the current through the switch is zero while the switch transits from off to on state or reverse. These types of switching are called ZVS (zero voltage switching) and ZCS (zero current switching). Therefore, by minimising the switching losses, the overall efficiency of the converter can be increased to up to 90% and higher. Finally, the single stage charge pump PFC topology can offer excellent power factor and THD, it is less expensive and smaller comparing to active two stage PFC systems as it does not need extra control system for the PFC pre-converter and it only need few diodes and capacitors to correct the power factor. However, charge pump PFC systems are extremely difficult to design as their response is sensitive to their operating condition. For the resonant converters shown above, changes in load and input voltage mandate a change in frequency if the output is to be regulated (i.e. held at a constant voltage) and this could significantly alter the behaviour of the entire circuit. Modelling these types of circuits is highly complex. So far this type of PFC has been widely used in electronic ballast systems for mainly fluorescent lighting application and other lighting applications such as LED systems. In addition, this type of PFC system has rarely been applied on switch mode power supplies. Therefore, there is still large amount of research needed for this type of PFC to be able to apply it on different applications and systems [5] [6].

1.8 Comparison of different PFC systems

In previous section main different types of PFC has been explained. The cons and pros of each has been listed. As mentioned, each PFC system is suitable for different application, and it is not possible to choose one PFC approach and use it in every system and application. Table 1.3 shows the advantages and disadvantages of each PFC circuitry.

	Cost	Size	Design simplicity	Efficiency	Power factor	THD
LC input Filter	✓	✓	✓	X	X	X
Valley fill	✓	✓	✓	X	X	X
Two stage DC/DC pre-converter	X	X	X	✓	✓	✓
Single stage charge pump	✓	✓	X	✓	✓	✓

Table 1.3: The advantages and disadvantages of different types of PFC systems.

As illustrated in table one single stage charge pump PFC system has many advantages against other types of PFC circuits. However, there has not been many studies around these types of circuits and some of the published researches are not correct. Therefore, there is a need for more research to be done on single stage charge pump based power factor correctors.

1.9 The contribution of this thesis

This thesis aims to provide new analysis and tools to design single stage current source charge pump based power supplies with resonant converters to improve power factor while maintaining high efficiency.

In chapter one a detailed review of power in AC systems, PF, PF standards and measurements and different types of PFC has been given. In chapter two a detailed literature review of charge pump systems, resonant converters and single stage current source charge pump PFC system has been given. Moreover, in chapter two a full analysis of prior research and analytical analysis of the single stage current source charge pump PFC along with the inconsistencies of the prior work has been demonstrated. In chapter 3 novel analytical model based on fundamental mode approximation and describing functions has been introduced. In addition, the testing and evaluation of the model and the boundaries that the model is valid has been described. In chapter 4 the modes of operation of the system under different condition has been investigated using LTspice simulation package. Lastly, in chapter 5 practical experiments and validations are illustrated. Furthermore, a novel system has been described that extracts the real time modes of operation in order to verify simulation results. Finally, in chapter 6 a conclusion and the further work and research that can be done on this PFC system in future has been explained.

1.10 References

[1] N. Mohan, Power Electronics, A first course, Minneapolis: Wiley, 2012.

[2] M. h. Rashid, Power Electronics Handbook, Florida: Academic Press, 2001.

[3] N. Mohan, M. T. Undeland and P. W. Robbins, Power Electronics, Converters, design and applications. 2nd Edition, Wiley, 1995.

[4] J. Drapela and . J. Bok , “An improved Valley-Fill passive Power-Factor-Correction circuit for electronic ballast,” in *ELECTRIC POWER ENGINEERING* , 2008.

[5] W. Chen, F. C. Lee and . T. Yamauchi, “An Improved “Charge Pump” Electronic Ballast with Low THD and Low Crest Factor,” *IEEE TRANSACTIONS ON POWER ELECTRONICS,,* vol. 12, no. 2, pp. 867-875, 1997.

[6] C. F. Lee, J. Qian and T. Yamauchi , “Current Source Charge Pump Power Factor Correction Electronic Ballast,” *IEEE,* pp. 66-22, 1997.

[7] R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics, Colorado: Springer, 2001.

Chapter 2. Review of technologies underpinning single stage charge pump power factor correctors

Having reviewed the popular types of PFC and stating the benefits of single stage charge pump PFC in chapter 1, it is now necessary to gain familiarization with charge pump circuits, resonant converters, and lastly single stage current source charge pump PFC (SSCSCP-PFC) which for the basis for the work embodied in this thesis. In this chapter the current state-of-the-art techniques to model, design and analyse SSCSCP-PFC systems will be explained. First charge pump circuit are discussed. The resonant converters and the techniques used to analyse are described.

2.1 Charge pump systems

Charge pump (CP) circuits are widely used in countless applications in modern technology. The very first applications of charge pumps were voltage doubler and voltage multiplier (Dickson multiplier) power supply circuits. These circuits can increase input voltage to tens of kilovolt [1]. Unlike, other DC-DC switching converters that require power inductors, CPs only need capacitors and diodes [2] [3]. However, these circuits cannot deliver high powers and they are only used for high-voltage, low-current applications such as cathode ray tubes, electrostatic systems, and X-ray machines [3]. Figures 2.1 and 2.2 show the voltage doubler and voltage multiplier respectively.

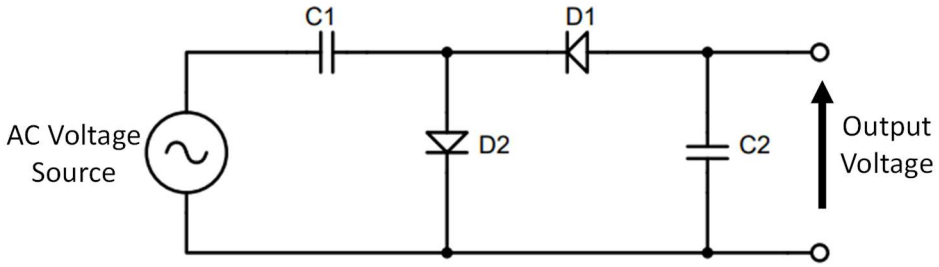


Figure 2.1: Voltage doubler circuit [2] [3].

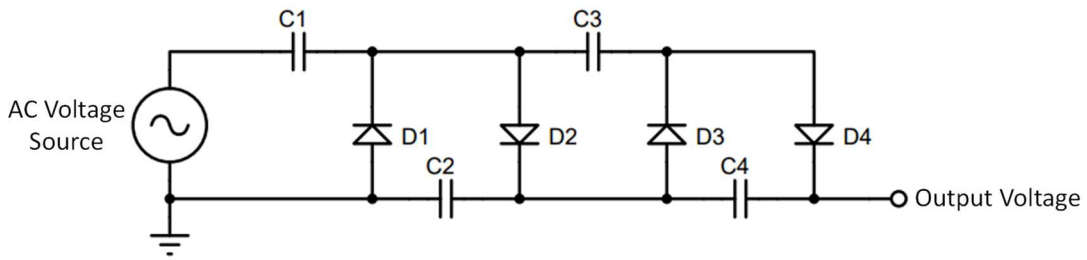


Figure 2.2: Voltage multiplier circuit [2] [3].

Voltage doubler and multiplier circuits as shown in figures 2.1 & 2.2 require an AC voltage source. Vin is an oscillating voltage, the C1 and D2 form an AC coupled diode clamp that generates a negative only oscillating voltage. D1 and C2 form a peak detector that rectifies the generated negative voltage to create a negative DC voltage The voltage source does not have to be sinusoidal and it can be square or triangle wave [3] [2]. In figure 2.1 the output voltage is twice the input voltage and in figure 2.2 the output voltage is 4 times higher than the input voltage. The output voltage can be increased by cascading more sections [1] [3] [2].

Apart from the 2 applications explained above there are many other applications for CPs. Another application of charge pumps is to be fabricated on semiconductor wafers to form integrated circuits (IC) [4]. As these systems only need diodes and capacitors to provide higher voltage than the supply voltage, they can easily be implemented on semiconductor wafers to form ICs for many different tasks [1]. These ICs are widely used in many different applications including computers, power management ICs and even in power switch gate drivers where there is need of higher voltage than available with low current. The MAX232 is a popular IC providing TTL to RS232 data signal conversion and uses voltage inverting and double CPs to generate signals that adhere to the RS232 standard [1].

Moreover, CPs are also used in both volatile and non-volatile computer memory systems including random access memories (RAM) flash memories and electronically erasable programmable read only memories (EEPROMs). Traditionally, non-volatile memories used mechanical and electromagnetic technologies which requires more space and more energy to operate [5] [6].

Another useful and beneficial application of charge pump circuits is for power factor correction. There are many different PFC topologies that use the transferal of packets of charge to achieve PFC. Several topologies that uses these systems are explained below [7] [8] [9] [10].

- Valley-fill PFC: valley fill PFC improves the power factor and line current THD by using a combination of capacitors and diodes and has been described in chapter 1. These PFC systems are usually used for low power application [11].

- Voltage source charge pump PFC: This type of PFC system consists of a resonant converter and a charge pump circuit. The resonant converter in this topology provides high frequency oscillating voltage pulses for the charge pump (D_1 and C_{PFC}) to deliver packets of charge from input bridge rectifier to the power stage. Careful design and a mains input LC filter allow the circuit to achieve close to unity power factor. The schematic for this system is shown in figure 2.3 [12] [8] [9] [10].

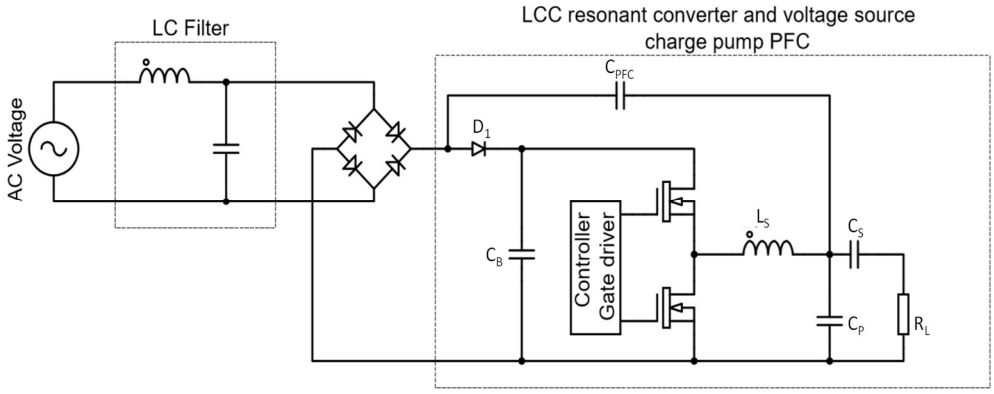


Figure 2.3: Single stage voltage source charge pump PFC [11].

- Current source charge pump PFC: This PFC system has a similar operating principle to the voltage source concept. It consists of a resonant converter and a charge pump PFC. In this system instead using high frequency voltage pulses, high frequency current pulses are used to operate the CP and achieve near unity PF. Figure 1.4 shows the circuit diagram of this system. This system will be explained in greater detail later in this chapter [13].

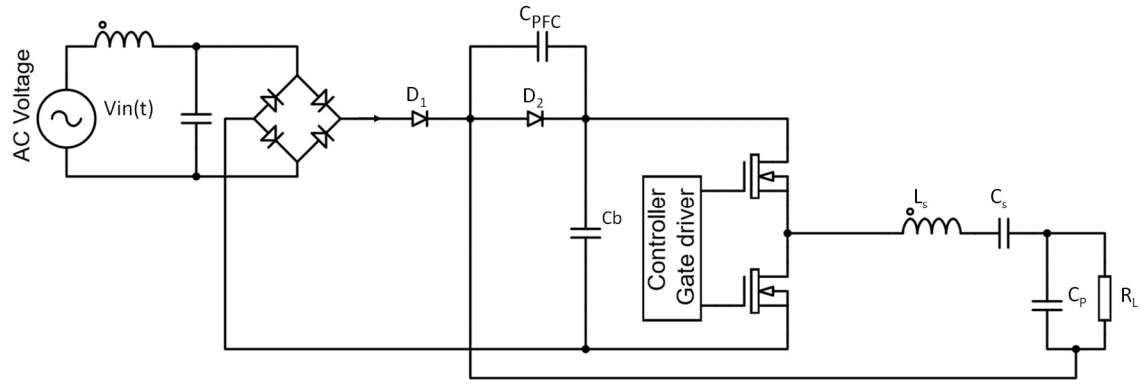


Figure 2.4: Current source charge pump PFC. [13]

- Hybrid charge pump PFC: This PFC system is a combination of the voltage source and current source PFC. It consists of a resonant converter and a charge pump PFC circuit. However, it uses both high frequency voltage and current pulses to achieve PFC. A circuit schematic of this system is shown in figure 2.5 [14].

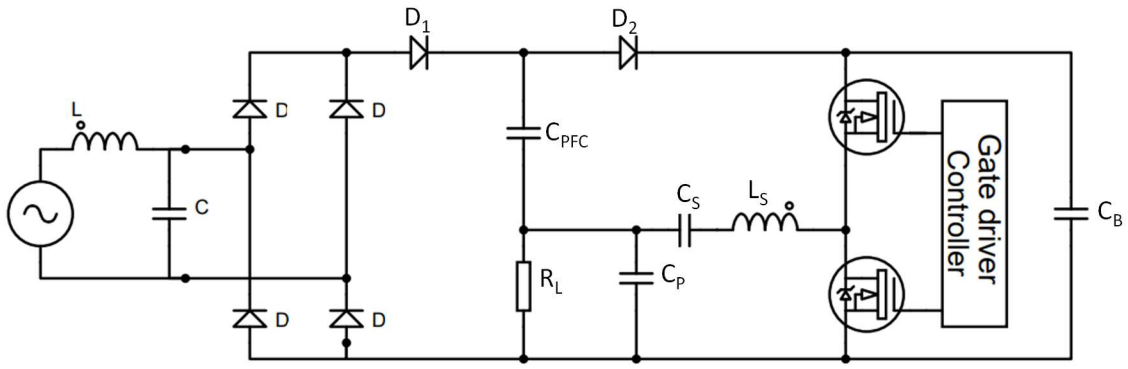


Figure 2.5: Single stage hybrid(current-voltage) source charge pump PFC [14].

2.2 Resonant Converters

Decades ago, when power electronic systems were rapidly advancing and replacing old power systems such as power transformers and triac systems, there was a huge demand for more compact and highly efficient systems. A key driver for the adoption of power electronic converter circuits is that as the switching frequency increases, the size of power electronic components such as inductors and capacitors decrease [19]. Unfortunately, the finite turn-on and turn-off switching times of the power devices give rise to switching losses since the power device voltage and current waveforms are non-zero during a switching event. This is known as hard-switching and for traditional power electronic converters such as Buck and Boost converter power conversion efficiency is dominated by switching losses at high frequency. There exists a trade-off between converter losses and its volume. Resonant converters, on the other hand, use LC resonance to shape the voltages and/or currents to ensure one or either are zero during the turn-on and turn-off transition. This process is known as soft switching, and it is very successful for reducing or even eliminating switching losses. In power electronic switches such as MOSFETs or IGBTs the majority of the power loss occurs in the transition period between off and on state of the switch (dynamic loss). In high current or voltage applications these transitions can impose massive stress on the component and reduce its lifetime [20]. Therefore, the power loss, which is the product of the voltage and current, in the transition period is zero. In the case that current through the switch is zero it is called zero current switching (ZCS) and for the voltage it is called zero voltage switching (ZVS) [17] [18]. Figure 2.6 shows a typical and simplified circuit diagram for resonant converter.

Another benefit of resonant converter topologies is that they can be used with Piezo-electric Transformers(PTs). The electrical equivalent circuit of PTs is an LCC resonant circuit. Therefore, by using PTs it is possible to eliminate the need of power inductors and capacitors and only use PT as both the transformer and resonant tank [19] [20]. Lastly PTs offer higher power density (more 50 watts per cubic centimetre), very low EMI and high galvanic isolation

[21]. Due to these benefits PTs and systems based on them are gaining interest in power electronic systems.

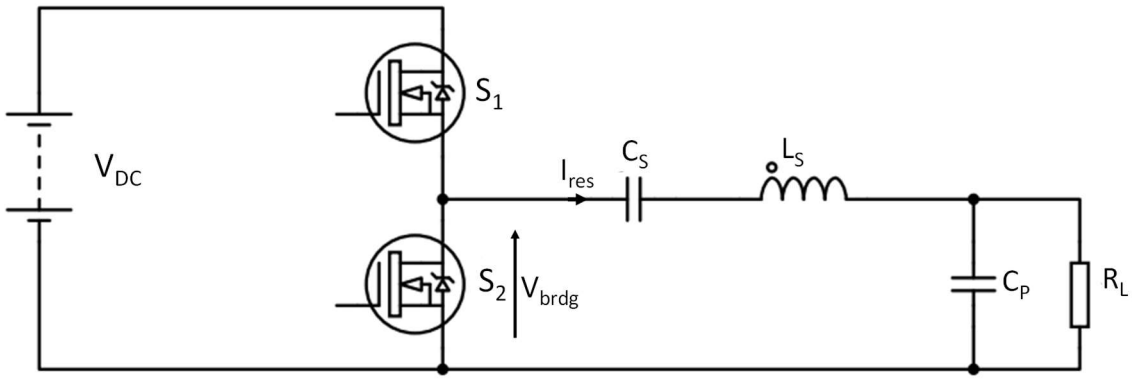


Figure 2.6: Simplified circuit diagram of a resonant converter [22].

Circuit diagram of figure 2.6 consists of an input DC voltage (V_{DC}), half bridge (S_1 & S_2) and a resonant tank with a load R_L. The half bridge chops the DC voltage into a square wave with 50% duty cycle. The square wave then excites the resonant tank causing a sinusoidal current to flow in the tank. In this circuit the output voltage (voltage across R_L) is sinusoidal. Therefore, in order to deliver DC output voltage, a high-speed rectifier needs to be implemented on the output [22] [19]. Figure 2.7 shows switching waveforms for when ZVS is achieved and when it is not.

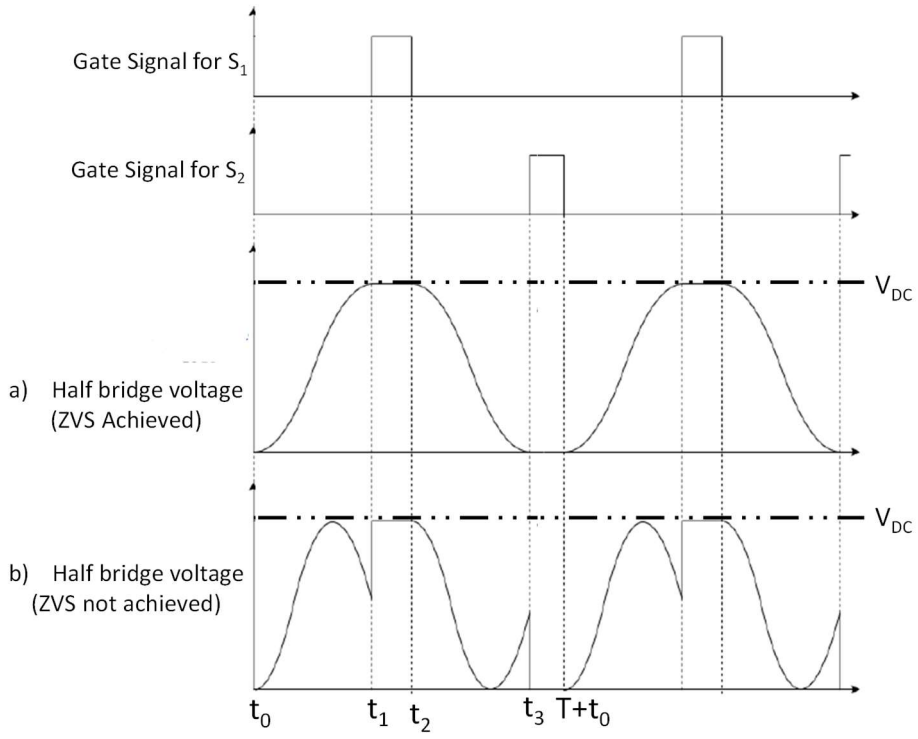


Figure 2.7: Gate signal and half bridge voltage for a) ZVS achieved b)ZVS not achieved

In figure 2.7 the upper two waveforms shows the gate signals that control the conduction states for the half bridge switches. The waveform figure 2.7a shows the half bridge voltage when ZVS is achieved. As it can be seen at time t_1 before the switch S_1 turns on, the half bridge voltage has increased from 0 V to V_{DC} voltage. Therefore, the voltage across the S_1 is equal zero as the voltages on drain and source terminals are equal to V_{DC}. A similar procedure occurs for switch S_2 at time t_3 as the drain and source terminals of the switch S_2 have zero volts hence the voltage across the component is zero [18] [19]. This process happens for both turn on and off transition of the switches. Therefore, theoretically soft switching reduces the switching loss of the power devices to zero.

In contrast, in figure 2.7b the conditions for soft switching are not correct and the half-bridge voltage experiences a sudden jump at time t_1 when switch S_1 transitions from off to on state leading to switching loss and possible EMI issues. Switch S_2 also experiences a similar issue at time t_3. In this case ZVS is not achieved and power losses could be considerably higher. Power converters that use soft switching technique can offer efficiency of 95% or higher [22] [20] [17].

Referring to Fig. 2.7a it can be seen that the MOSFET are driven in a complementary manner and that dead-time must exist between the turn-off of one switch and the turn-on. The dead-time is required for two reasons. Firstly, in order to achieve ZVS a minimum amount of dead time is required between the gate signals of the half bridge to allow the bridge voltage to gracefully travel between 0V and V_{DC}. During the dead-time the resonant charge is circulating through the body diodes of switches S_1 and S_2 depending on the direction of the resonant current. Furthermore, the dead time has to be precisely calculated to achieve ZVS. Moreover, dead time has to be sufficient to prevent the switches to be on at the same time so as to avoid a shoot-through event where a short circuit could lead to damage[23].

2.2.1 Control of resonant converters

Traditional hard switching converters such as Buck or Boost converters typically use pulse width modulation (PWM) to regulate the output voltage. In PWM regulators the duty cycle of the control pulse is proportional to the output voltage. However, the control of resonant converters is more complex due to several reasons.

There are several techniques to control resonant converters. The first one is PWM which by controlling the duty cycle it is possible to control the energy that has been transferred to the load. However, in this technique, additional systems may be needed to ensure ZVS achievement. The next popular method is using frequency modulation (FM). Resonant circuits are frequency dependant, and they have different gains at different frequencies. Therefore, by varying the switching frequency it is possible to change the output voltage amplitude. The parameters that can be adjusted in control signals (Gate signals) are only pulse width and the frequency however, there are countless techniques proposed to control these two parameters to regulate the output voltage and/or current and to ensure achievement of soft switching. An example of these methods is using phase locked loop (PLL) system [24] where

the switching frequency is locked at the resonant frequency of the system. Using PLL ensures ZVS achievement [24]. There are other systems to control resonant converters, such as charge control, however, most of them are work on a similar basis as those explained above.

2.2.2 Analysis of resonant converters

There are various methods to analyse resonant converters including describing functions [25] and First Harmonic approximation (FHA). FHA is also known as Fundamental Mode Approximation (FMA). As explained earlier resonant converters include a resonant tank and the tank circuit is usually designed to exhibit high Q-factor bandpass filter characteristic. The half-bridge voltage waveform is filtered by the resonant circuit causing a sinusoidal shaped current to flow. If the resonant converter is operated close to its resonant frequency and Q-factor is sufficiently high, the bandpass filter will attenuate all but the fundamental component of the square (or trapezoidal) shaped bridge voltage. Therefore, it is possible to assume that the resonant current is caused by the first harmonic of the square wave. By using Fourier series, it is possible to obtain amplitude (and phase) of the fundamental component of the bridge voltage that is applied to the resonant tank which can be used as the equivalent input voltage to resonant circuit. As the switching frequency is known, the total impedance of the resonant tank can be calculated. Finally, as the voltage and impedances are known by using Ohm's law and Kirchhoff's law it is possible to obtain voltage and current for all of the components in the resonant tank including output section. Although only approximate, FHA is a very powerful technique, and it will be used in various sections of the thesis to derive equivalent circuit models of resonant converters and single-stage PFC circuit.

2.2.3 An example of mathematical analysis of an LCC resonant converter

In order to gain a better understanding of the mathematical modelling of resonant converters using FMA, the circuit diagram of figure 2.6 is mathematically modelled in this section.

The first step is to derive an equation for the input voltage to the resonant tank (labelled V_{brdg}). The V_{brdg} is a square wave with amplitude of V_{DC} and frequency of the switching frequency with duty cycle of approximately 50%. Based on FMA the input voltage to the resonant tank can be assumed to be the fundamental component of the V_{brdg}. Therefore, it can be calculated using (2.1).

$$V_{brdg<1>} = \frac{2 \times V_{DC}}{\pi} \times \sin(\omega_s \times t) \tag{2.1}$$

In (2.1) ω_s is the angular velocity of the switching frequency and t is time and $V_{brdg<1>}$ is the fundamental component of V_{brdg}. The next step is to derive an equation for the total

impedance of the resonant tank. The total impedance can be divided into two impedances, series and parallel. The series impedance is the impedances of L_s and C_s. The parallel impedance is the impedances of C_p and R_L. The equations for the series and parallel impedances are demonstrated in (2.2) and (2.3) respectively.

$$Z_s = (j \times \omega_s \times L_s) - \frac{j}{\omega_s \times C_s} \tag{2.2}$$

$$Z_p = \frac{\left(j \times \omega_s \times C_p \times R_L\right) + 1}{R_L} \tag{2.3}$$

In (2.2) and (2.3) the term j is the imaginary operator, and it is the square root of minus one. In the next step the total impedance of the resonant tank can be calculated using (2.4).

$$Z_{tot} = Z_p + Z_s \tag{2.4}$$

As the voltage and impedance of the system are calculated, now the resonant current I_{res} can be calculated using the Ohm's law. (2.5) shows the derivation for I_{res}.

$$I_{res} = \frac{V_{brdg<1>}}{Z_{tot}} \tag{2.5}$$

Now by having mathematical expressions for the input voltage to the resonant tank ($V_{brdg<1>}$) and the I_{res} the voltage and current for all the component of the circuit can be obtained using AC circuit analysis techniques.

The remaining sections of this chapter are devoted to describing the Single-stage current source charge pump PFC (CSCPPFC) in detail. It begins with a description of the circuit, waveforms, and operating models. This is followed by a review of prior work of others, and this highlights the deficiencies that exist in the literature. Addressing some of these deficiencies is the focus of this work.

2.3 Single Stage current source power factor correction

All types of charge pump PFC topologies operate on a similar basis where a high-frequency oscillating voltage or current within the power supply circuit is used to transfer small packets of charge from the input to a DC link [9] [8]. Many schemes are possible, but they often rely on a resonant oscillating voltage or current connected to the common point of two series connected diodes through a capacitor (referred to here as the PFC capacitor). The internal

high-frequency voltage (or current) modulates the low-frequency input current which, when filtered, results in a low frequency sinusoidal current. Since the amount of charge that is transferred to the PFC capacitor varies with the input voltage the interaction between resonant tank circuit and the charge pump circuit is complicated and it is impossible to treat the PFC conversion process separate to the main conversion process as one can more easily do in a two-stage power factor converter system. Therefore, owing to the complex and interdependent operation of the charge-pump and the resonant converter they have to be analysed in unison.

Figure 2.8 shows a simplified block diagram representation of the single stage current source PFC where the input voltage $V_{in(t)}$ is a full wave rectified sinusoidal wave [13]. In order to simplify the diagram the rectifier and input filter has been removed and a voltage source with full wave rectified sinusoidal wave has been replaced [13] [12] [8] [9]. It shows that the circuit has two main parts, the charge pump PFC and the resonant inverter. Figure 2.9 show the detailed circuit diagram of the single stage charge pump power factor correction. Moreover, figure 2.9 shows the blocks of the figure 2.8 on the circuit diagram.

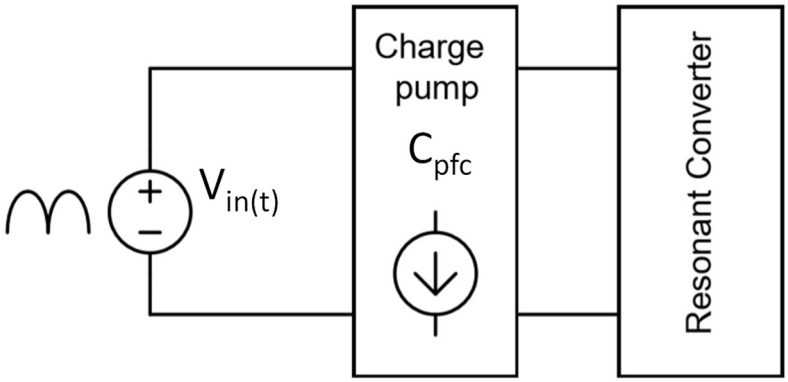


Figure 2.8: Block diagram of a single stage current source charge pump PFC [13]

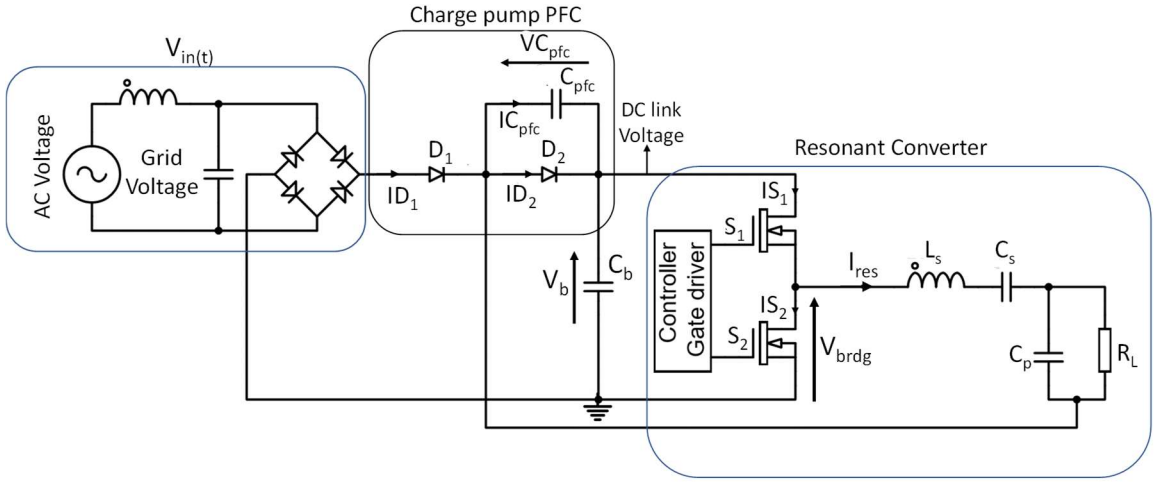


Figure 2.9: Schematic of single stage current source charge pump PFC [13].

The power source for this circuit is the grid voltage which is then rectified using a full bridge rectifier as shown in figure 2.9. In order to simplify the analysis and the mathematics the input voltage and the rectifier system is changed to a full wave rectified voltage source(identified in figures 2.8 and 2.9 as $V_{in(t)}$. In this circuit there is a fixed DC voltage across C_b (V_b) and in order for the circuit to function correctly V_b, the DC link voltage, is always higher than the input peak voltage. The half bridge MOSFETs turn the V_b into a square wave with peak value of V_b and duty cycle of 50%. This square waveform then excites the resonant tank, causing a sinusoidal current I_{res} to flow into the tank and then into the common point between D_1 and D_2 (identified as Node m in Fig. 2.9). Since I_{res} is oscillating, so is the voltage at node m, V_m. If $V_{in(t)}>V_m$ and I_{res} is negative, then D_1 must be conducting and so current (charge) is transferred from the grid to the circuit. I_{res} is resonating and so as it naturally falls to zero turning off D_1. The charge that was transferred from the grid is absorbed by the DC link. Vm is therefore modulating the current through D_1 and this provides the charge-pump power factor correction. Depending on the input voltage the conduction time of D_1 varies. Therefore, the average input current varies with the input voltage. Thus, PFC can be achieved by choosing the appropriate circuit values. [13] Figure 2.11 shows the waveforms of the modulating voltage V_m and currents for D_1, C_{pfc} and I_{res}.

2.4 PFC operation

First it is necessary to investigate the PFC operation of the system and then the resonant converter. The PFC operation can be analysed using an equivalent circuit that is shown in figure 2.10 [13]. In figure 2.10 the resonant tank has been replaced with a current source as the resonant tank circuits in resonant converters behave in a same way as a current source. Figure 2.11 shows the switching waveforms associated with the equivalent circuit of figure 2.10. The resistor labelled LOAD represents the equivalent loading that the resonant inverter presents to the DC link.

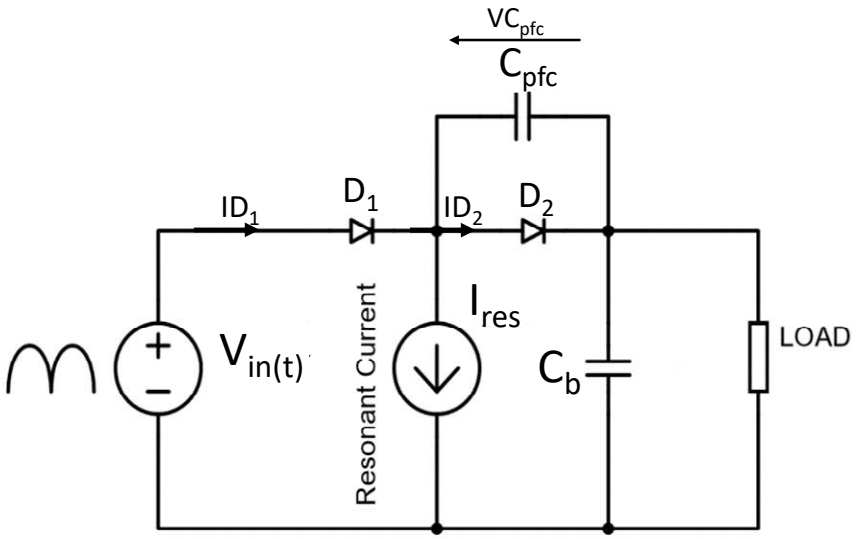


Figure 2.10: Topological equivalent circuit [13].

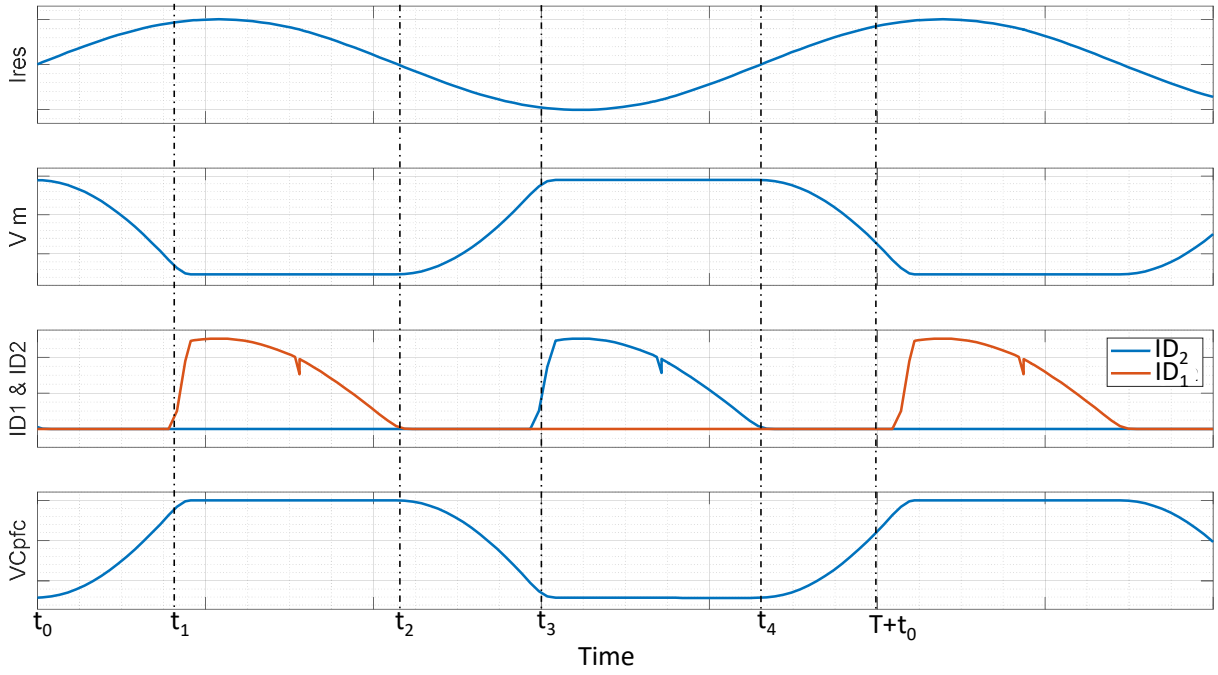


Figure 2.11: Switching waveforms.

By analysing the switching waveforms shown in figure 2.11 and the equivalent circuit in figure 2.10. Four modes of operation can be extracted. The modes of operation for the equivalent circuit shown in figure 2.12 [13].

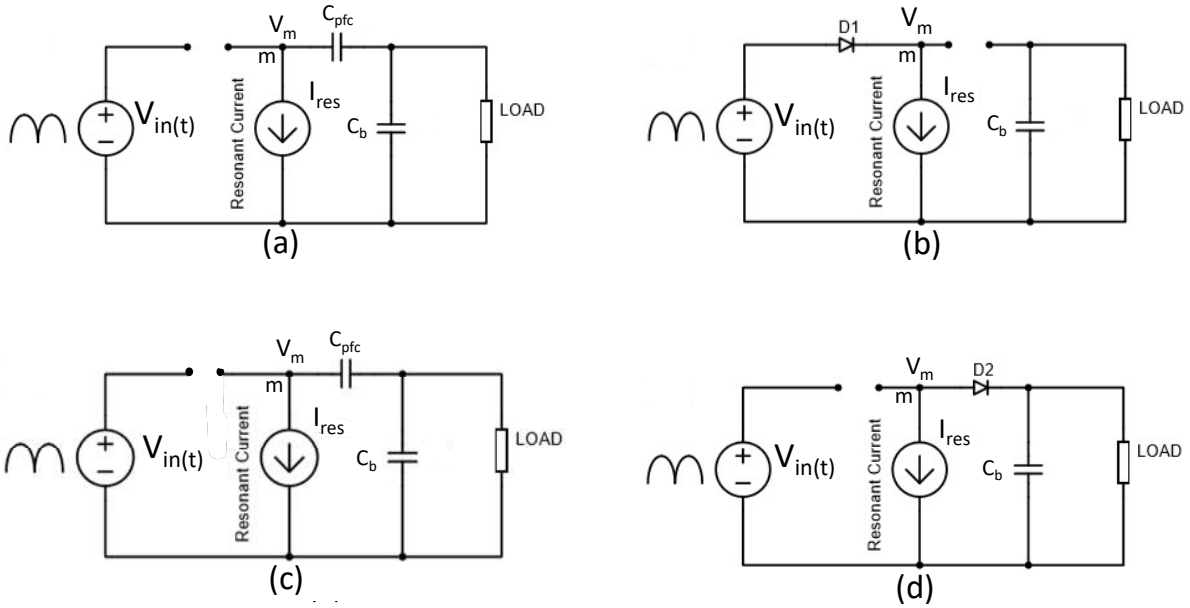


Figure 2.12: Modes of opeartion for the topological equivalent circuit [13].

Mode a [t_0, t_1]: In this this mode the diode D_1 is turned off. The resonant current flows from C_{pfc} to the resonant tank. The voltage at node m is decreasing.

Mode b [t_1, t_2]: The C_{pfc} is discharged enough and the voltage at node m is less than the input voltage hence the diode D_1 starts conducting and transferring energy from input to the resonant tank. The voltage at node m is clamped to the input voltage as D_1 is on.

Mode c [t_2, t_3]: At t_2 the resonant current becomes negative hence diode D_1 is turned off. As the voltage at node m is lower than the voltage across C_b, diode D_2 cannot turn on. Therefore the I_{res} flows through C_{pfc} and charging it.

Mode d [t_3, t_4]: At t_3 the voltage at node m is equal to the voltage across C_b. Therefore, diode D_2 starts conducting until the resonant current becomes positives.

2.5 Converter operation

Having analysed and reviewed the PFC operation of the system, it is now necessary to analyse the operation of the resonant converter and the whole system together. The same approach that was taken to analyse the PFC operation can be used here. The first step is to extract the modes of operation. However, as the whole system is analysed there is no need for an equivalent circuit and the modes of operation can be applied on the circuit of figure 2.9. figure 2.13 shows the waveforms for the resonant current, V_{brdg}, IS_1, IS_2, ID_1, ID_2, VC_{pfc} and IC_{PFC} .The modes of operation for one switching cycle is shown in figure 2.15. Moreover, figure 2.14 shows the charging and discharging process of capacitor C_b. Figure 2.14 demonstrates I_{res} and IC_b versus time.

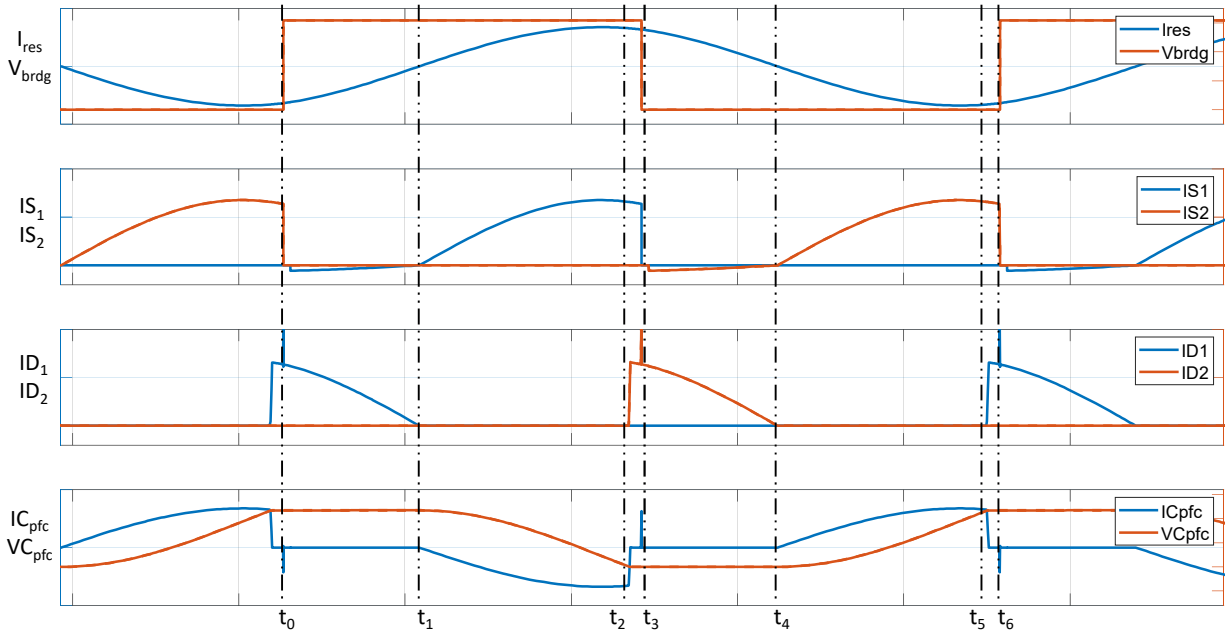


Figure 2.13: The operating waveforms of the system.

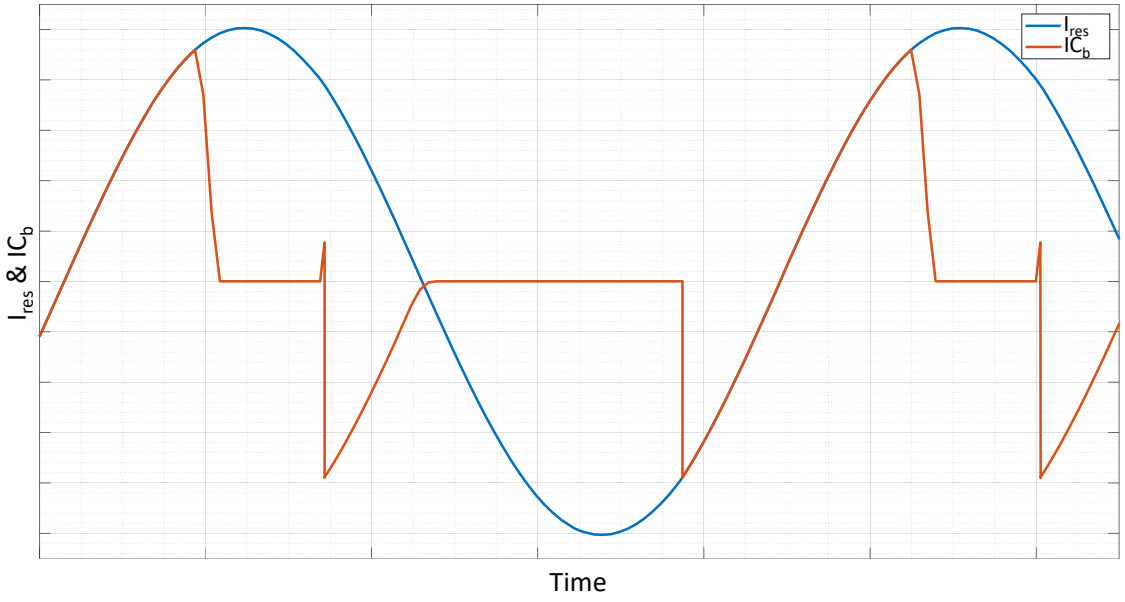


Figure 2.14: I_{res} and IC_b waveforms versus time.

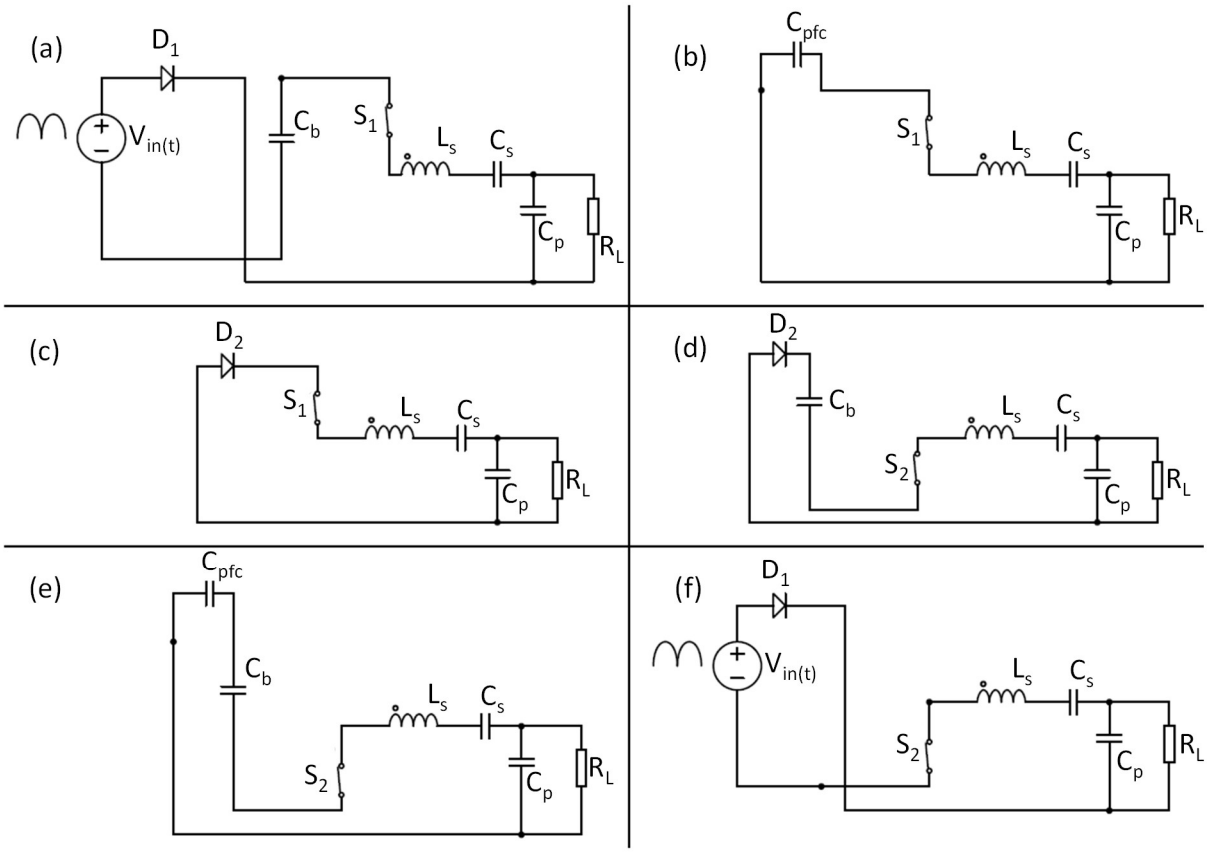


Figure 2.15: The modes of operatin of the system [13].

Mode a [t_0, t_1]: In this mode the I_{res} is negative. The high side switch of the half bridge S_1 is conducting and the energy from input flows through D_1 and the resonant tank . C_b is charging in this mode. At t_1 resonant current is equal to zero and D_1 turns off.

Mode b [t_1, t_2]: As the I_{res} is positive and the voltage at the common connection of D_1 & D_2 (V_m) is lower than the DC link voltage both diodes are off, and the resonant current starts to discharge C_{pfc}.

Mode c [t_2, t_3]: Capacitor C_{pfc} is discharged now and the voltage at node m is higher than the DC link voltage. Therefore diode D_2 becomes forward biased.

Mode d [t_3, t_4]: Switch S1 is turned off and S2 starts conducting. As the I_{res} is still positive diode D_2 continues to conduct. In this mode I_{res} flows through C_b and charges it.

Mode e [t_4, t_5]: At t_4 I_{res} reverses from positive to negative. Therefore diode D_2 is turned off and as the voltage at node m is higher than input voltage diode D_1 stays off. In this mode the current flows from C_b (discharging) through C_{pfc} (Charging) and resonant tank .

Mode f [t_5, t_6]: At t_5 the voltage at node m has decreased to a value lower than the input voltage. Therefore D_1 will start conducting. In this mode I_{res} flows through D_1 and S_2.

2.6 A review of the previous attempts to model the CSCPPFC inverter

Having analysed and reviewed the operation of the current-source PFC in isolation and the combined system, in this section mathematical models available in the literature are now reviewed[13]. This section starts by describing previous attempts in detail and then discusses some error or omissions in the previous work.

The purpose of this model is first to obtain a mathematical expression to calculate the required value of C_{pfc} to meet unity power factor criteria based on known values of the system[13]. The second aim of the model is to derive mathematical expressions for unknowns of the system such as I_{res} and voltages of different components. The key assumptions for this model are:

1. The switching frequency (f_s) of the resonant inverter is much greater than the grid frequency (f_g). Moreover, this assumption implies that the rate of change of the low-frequency (grid) signals considered over the duration of a high-frequency period can be considered to be zero.

2. Resonant circuit has a high Q factor. Therefore, high frequency resonant current is sinusoidal. The resonant current can be calculated using (2.6).

$$I_{res(t)} = I_{res-p} \times \sin(\omega_s \times t) \tag{2.6}$$

In (2.6) I_{res-p} is the peak value of the resonant current and ω_s is the angular velocity of the switching frequency.

As explained previously, the input voltage to the circuit is an AC grid voltage and in order to simplify the analysis the grid voltage, LC filter and the full bridge rectifier is being treated as single voltage source with a waveform shape equivalent to that of the full wave rectified grid voltage. There are three different terms used in the derivations for the input voltage:

- V_{in-p} is the peak value of the AC input voltage
- $V_{in(t)}$ is the time-based function of the input voltage and is given by (2.7)
- $V_{in-average}$ is the average value of the full wave rectified input voltage, given by (2.8)

In (2.1) ω_g is the angular frequency of the grid voltage.

$$V_{in(t)} = \left|V_{in-p} \times \sin\left(\omega_g \times t\right)\right| \tag{2.7}$$

$$V_{in-average} = \frac{2 \times V_{in-p}}{\pi} \tag{2.8}$$

The model derivations are done on one high frequency cycle to obtain mathematical equations describing voltages, currents and power of the system. Model derivation begins by obtaining an expression for the grid input current. The current that flows through the circuit from the grid input is also the current that flows through diode D_1 (Modes A&F from figure 2.15)[13]. As can be seen from waveforms in figure 2.13 the current through D_1 is equal to resonant current during Modes A & F and, therefore, it is possible to use average value of half wave rectified sinusoidal wave, then subtracting the portion that is not in the waveform. That portion of current flows through C_{pfc} [13]. The current waveforms of diode D_1 and C_{pfc} and the resonant current is shown in figure 2.16. Hence the average input current can be calculated using (2.9) [13].

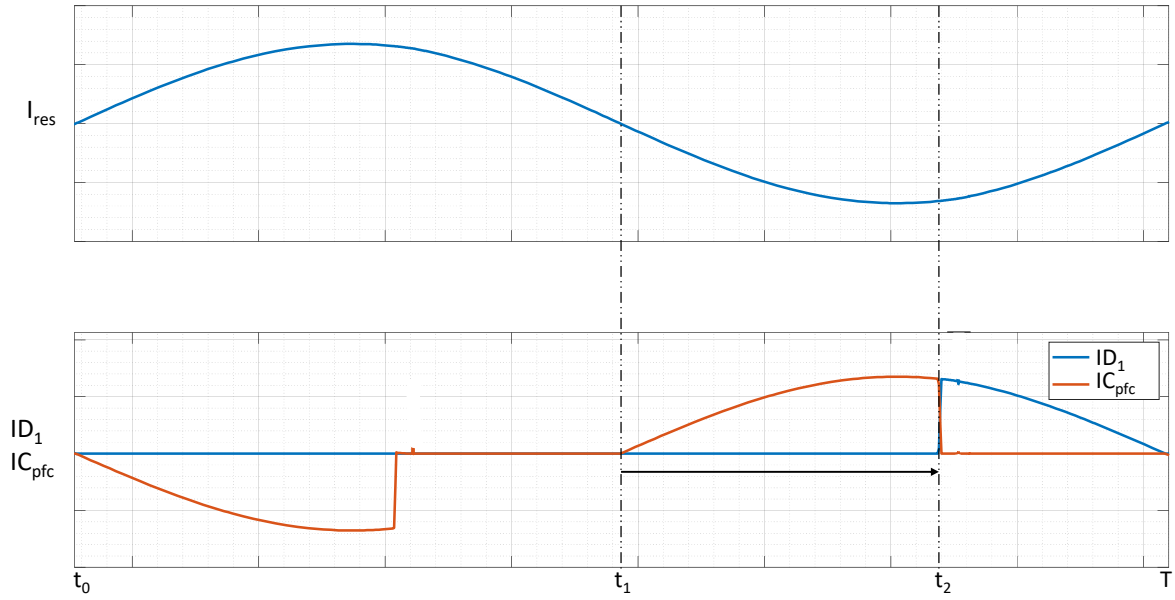


Figure 2.16: The current waveforms of D_1, C_{pfc} and the resonant tank.

In figure 2.16 the high frequency switching period is T (from t_0 to T) and the interval from t_1 to t_2 is the duration when the resonant current flows through C_{pfc}. Moreover, time t_1 is the half of the switching period T. Therefore, to obtain the average value for the input current ($I_{in\text{-}average}$), the average value of the half wave rectified resonant current should be calculated, then the amount of charge in duration between t_1 and t_2 should be subtracted. As shown in (2.9).

$$I_{in-average} = ID_{1-average} = \frac{1}{T}\int_0^T ID_1.dt = \frac{1}{T}\int_{\frac{T}{2}}^T \left(-I_{res(t)}\right).dt - \frac{1}{T}\int_{\frac{T}{2}}^T IC_{pfc}.dt \quad (2.9)$$

$$I_{in-average} = \frac{I_{res-p}}{\pi} - \frac{\Delta Q}{T} \quad (2.10)$$

In order to calculate average input current (2.10) can be used. In (2.10) the first term is the average value of half wave rectified sinusoidal resonant current. The second term is the amount of charge that is transferred to the C_{pfc}. T is the high frequency switching period. The second term can be expanded to (2.11). In (2.11) V_b is the voltage across the C_b as shown in figure 2.9.

$$\Delta Q = C_{pfc}\left(V_b - V_{in-average}\right) \quad (2.11)$$

By substituting (2.11) into (2.10) the (2.12) can be achieved.

$$I_{in-average} = \left(\frac{I_{res-p}}{\pi} - C_{pfc} \times f_s \times V_b\right) + C_{pfc} \times f_s \times V_{in-average} \quad (2.12)$$

In order to achieve unity PF the input current must be proportional to the input voltage. Therefore, if the first term in (2.12) is zero then unity power factor can be met. Moreover, for PFC operation voltage V_b, the DC link voltage, must be greater than peak of the input voltage to properly charge and discharge C_{pfc} in each switching cycle. Therefore, it can be assumed that the minimum DC link voltage is equal to the peak of the input voltage. (2.13) shows peak resonant current at the unity power factor condition[13].

$$I_{res-p} = \pi \times C_{pfc} \times f_s \times V_b \quad (2.13)$$

By using (2.13) to achieve unity power factor and (2.12) for the input current, new expression for the input current can be derived. (2.14) describes the average input current when PFC is met.

$$I_{in-average} = C_{pfc} \times f_s \times V_{in-average} \quad (2.14)$$

Up to this stage, mathematical equations to describe the input current and resonant current for the PF corrected condition has been demonstrated. The next step is to derive an expression for the instant input power to the system. The instantaneous power for one high

frequency cycle (f_s) is the product of average input current over one high frequency switching cycle and the instantaneous input voltage. The mathematical expression is shown in (2.15).

$$P_{in} = \left(\frac{I_{res-p}}{\pi} - C_{pfc} \times f_s \times V_b\right) \times V_{in-average} + C_{pfc} \times f_s \times {V_{in-average}}^2 \quad (2.15)$$

By averaging the (2.15) over one grid voltage cycle (f_g) it is possible to calculate the average input current. The average input current is shown in (2.16).

$$P_{in} = \frac{2 \times V_{in-p}}{\pi}\left(\frac{I_{res-p}}{\pi} - C_{pfc} \times f_s \times V_b\right) + \frac{1}{2} \times C_{pfc} \times f_s \times {V_{in-p}}^2 \quad (2.16)$$

Under the unity power factor condition as explained and given in (2.12), the first term of the (2.16) is zero and so the average input power can be rewritten as (2.17).

$$P_{in} = \frac{1}{2} \times C_{pfc} \times f_s \times {V_{in-p}}^2 \quad (2.17)$$

Based on energy balance the input power is the addition of losses and output energy. Therefore, it can be written as (2.18) where η is the overall efficiency of the system.

$$P_o = \eta \times P_{in} \quad (2.18)$$

Using (2.17) and (2.18) the PFC capacitor C_{pfc} can be determined using (2.19).

$$C_{pfc} = \frac{2 \times P_o}{\eta \times f_s \times {V_{in-p}}^2} \quad (2.19)$$

Having examined the operation of the circuit and the conditions needed to achieve PFC and derivations for the input current, input power and PFC capacitor. The output voltage and the resonant current can be calculated now.

In order to derive an expression for the output voltage and the resonant current the FMA method that has been discussed above is used. Based on Fourier series any periodic waveform consists of infinite sinusoidal and cosine waveforms. The frequency of these waveforms is a multiple of the frequency of the original signal and the first component or the original frequency component is called the fundamental component. FMA simplifies the derivations by only using the fundamental component of input voltage to the resonant tank. As it is illustrated in figure 2.13, the input voltage to the resonant tank or the bridge voltage is a square wave voltage. Since the resonant tank behaves like a bandpass filter the high-frequency harmonics are significantly attenuated and only the fundamental frequency

component flows through the circuit. s (2.20) and (2.21) shows the RMS output voltage and resonant current, respectively.

$$V_{o-RMS} = \frac{\sqrt{2}V_b}{\pi} \times \frac{1}{\sqrt{\left(1 - \frac{{\omega_s}^2}{{\omega_0}^2}\right)^2 + \left(\frac{\omega_s \times L_s}{R_L}\right)^2}} \quad (2.20)$$

$$I_{res-p} = \frac{2V_b}{\pi} \times \frac{\sqrt{(\omega_s \times C_r)^2 + \frac{1}{{R_L}^2}}}{\sqrt{\left(1 - \frac{{\omega_s}^2}{{\omega_0}^2}\right)^2 + \left(\frac{\omega_s \times L_s}{R_L}\right)^2}} \quad (2.21)$$

In (2.20) and (2.21) the ω_S is the switching angular velocity, ω_0 is the resonant angular velocity.

Moreover, to meet unity power factor condition (2.21) must be equal to (2.12) as explained above.

So far, the previous attempts to mathematically model the system has been demonstrated. However, in practice and simulation the results do not match with the results from the model and there are several inconsistencies. In the next section the simulation results are demonstrated and they are compared with the mathematical model calculations.

2.7 Evaluation of the mathematical model

In order to check and evaluate the mathematical model described in previous section, a simulation model has been designed and simulated. The circuit parameters are shown in the table 2.1.

Component	Value	Component	Value
L_s	1.69 mH	C_s	1.2 nF
C_P	38.6 nF	R_L	31
f_s	116 kHz	C_b	100 µF
$V_{in\text{-}peak}$	330 V	P_O	230 W

Table 2.1: The circuit parameters for the simulation model.

By using the component values and (2.19) the PFC capacitor can now be determined. In order to have power factor near unity the C_{pfc} has to be 40 nF . After simulating the model, it had been discovered that the results calculated by the mathematical model do not agree with the SPICE simulation. The results showed that unity power factor has not been achieved and the THD of the line current is more than 25%. The input voltage and input current of the simulation is shown in figure 2.17.

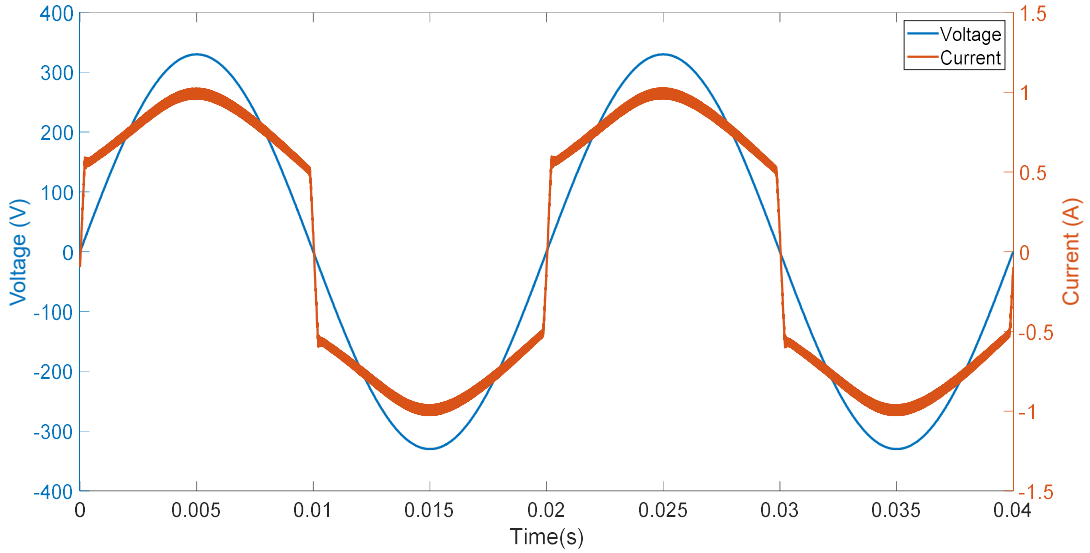


Figure 2.17: The input voltage and current of the simulation model.

After more investigation on the simulation results it has been found that the assumption on V_b is incorrect and the DC link voltage is not equal to the peak value of the input voltage. The DC link voltage (=450 V) is higher than the peak input voltage (330 V). This error leads to inconsistencies throughout the hole mathematical derivations as V_b is used in all the calculations. These inconsistencies creates a demand for a more precise model that can estimate the circuit values and component values to achieve near unity PFC and a reliable calculations. In the next chapter new mathematical model will be presented.

2.8 Conclusion

The background knowledge, operation and analysis of single stage current source charge pump PFC has demonstrated. However, as demonstrated in practice and simulations the results do not match with the mathematical models that has been demonstrated. As discussed, There are several inconsistencies between what has been described above and what happens in reality. Firstly, the assumption that the DC link voltage or the V_b is equal to the peak of input voltage ($V_{in\text{-}peak}$) does not happen and usually it is much higher than the input peak voltage. Lastly, the derivations for the PFC capacitor, resonant current and the

output voltage do not match with simulations or practical experiment results. The issues create a demand for a more precise mathematical model. In the next chapter a new mathematical model will be presented.

2.9 References

[1] G. Palumbo and D. Pappalardo, “Charge pump circuits: An overview on design strategies and topologies,” *IEEE circuit and systems magazine,* vol. 10, no. 1, pp. 31-45, 2010.

[2] A. S. Sedra and K. C. Smith, “The voltage doubler,” in *Microelectronic Circuits*, Oxford, Oxford University Press, 2004, pp. 187-190.

[3] P. Horowitz and W. Hill, “Diodes and diode circuits,” in *The art of electronics*, Cambridge, CambridgeUniversity Press, 2015, pp. 33-34.

[4] G. D. Besten and B. Nauta, “Embedded 5 V-to-3.3 V voltage regulator for supplying digital IC’s in 3.3 V CMOS technology,” *IEEE J. Solid,* vol. 33, no. 7, p. 956–962, 1998.

[5] T. Linbo, “A 5-V-only 16-Mb fl ash memory with sector erase mode,” *IEEE Solid State Circuits,* vol. 27, no. 11, pp. 1547-1553, 1992.

[6] G. Palumbo, D. Pappalardo and M. Gaibotti, “Charge pump with adaptive stages for non-volatile memories,” *IEE Proc. Circuits, Devices System,* vol. 153, no. 2, pp. 136-142, 2006.

[7] F. Tao, J. Qian, F. C. Lee and N. Onishi, “A comparative study of a family of charge pump power factor correction electronic ballasts,” in *APEC '99. Fourteenth Annual Applied Power Electronics Conference and Exposition*, Dallas, TX, USA, 1999.

[8] F. C. Lee and J. Qian, “Charge Pump Power-Factor-Correction Technologies Part I: Concept and Principle,” *IEEE TRANSACTIONS ON POWER ELECTRONICS,* vol. 15, no. 1, pp. 121-129, 2000.

[9] J. Qian and F. C. Lee, “Charge Pump Power-Factor-Correction Technologies Part II: Ballast Applications,” *IEEE TRANSACTIONS ON POWER ELECTRONICS,* vol. 15, no. 1, pp. 130-139, 2000.

[10] J. Qian, F. C. Lee and N. Onishi, “New charge pump power factor correction electronic ballast with a wide range of line input voltage,” in *APEC '98 Thirteenth Annual Applied Power Electronics Conference and Exposition*, Anaheim, CA, USA, 1998.

[11] J. Drapela and . J. Bok , “An improved Valley-Fill passive Power-Factor-Correction circuit for electronic ballast,” in *ELECTRIC POWER ENGINEERING* , 2008.

[12] . Q. Jinrong, F. C. Lee and Y. Tokushi , “A Single-Stage Electronic Ballast with Power Factor Correction and Low Crest Factor for Fluorescent Lamps*,” *IEEE Industry Application Societ,* pp. 2307-2312, 1997.

[13] C. F. Lee, J. Qian and T. Yamauchi , “Current Source Charge Pump Power Factor Correction Electronic Ballast,” *IEEE,* pp. 66-22, 1997.

[14] F. Tao, F. C. Lee and N. Onishi, “Optimization of combined voltage-source-current-source charge-pump power-factor-correction electronic ballast,” in *IEEE 31st Annual Power Electronics Specialists Conference*, Galway, Ireland, 2000.

[15] R. W. Erichson and D. Maksimovic, “Resonant Converters,” in *Fundamentals of Power Electronics*, New York, Springer, 2001, pp. 705-755.

[16] N. Mohan, T. M. Undeland and W. P. Robbins, “Resonant converters: Zero voltage and/or zero current switching,” in *Power Electonics, Converters, Applications and Design*, John Wiley & Sons, 1995, pp. 249-299.

[17] M. H. Rashid, “Resonant and soft-switching converters,” in *Power electronic handbook: Devices, circuits and applications*, Burlington, Elsevier, 2011, pp. 409-450.

[18] R. W. Erickson and D. Maksimovic, “Soft Switching,” in *Fundamentals of power electronic*, New York, Springer, 2001, pp. 761-796.

[19] E. M. Baker, W. Huang, D. Y. Chen and F. C. Lee, “Radial mode piezoelectric transformer design for fluorescent lamp ballast applications,” *IEEE Transactions on Power Electronics,* vol. 20, no. 5, pp. 1213-1220, 2005.

[20] R. L. Lin, F. C. Lee, E. M. Baker and D. Y. Chen, “Inductor-less piezoelectric transformer electronic ballast for linear fluorescent lamp,” in *Annual IEEE Applied Power Electronics Conference and Exposition*, Anaheim, CA, USA, 2001.

[21] E. L. Horsley, M. P. Foster and D. A. Stone, “State-of-the-art Piezoelectric Transformer technology,” in *European Conference on Power Electronics and Applications*, Alborg, Denmark, 2007.

[22] R. L. Steigerwald, “IEEE TRANSACTIONS ON POWER ELECTRONICS,” *A Comparison of Half-Bridge Resonant Converter Topologies,* vol. 3, no. 2, pp. 174-182, 1988.

[23] T. Gao, Z. Cheng, Q. Wang, Y. Li, K. Zeng and Y. Yang, “The Analysis of Dead time's Influence on the Operating Characteristics of LLC Resonant Converter,” in *14th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, Xi'an, China, 2019.

[24] A. J. Gilbert, M. P. Foster, D. A. Stone and C. M. Bingham, “Phase Locked Loop (PLL) based self-oscillating controller for LCC resonant converters,” in *IET Conference on Power Electronics, Machines and Drives*, York, 2008.

[25] M. P. Foster, C. R. Gould, A. J. Gilbert, D. A. Stone and C. . M. Bingham, “Analysis of CLL Voltage-Output Resonant Converters Using Describing Functions,” *IEEE TRANSACTIONS ON POWER ELECTRONICS,* vol. 23, no. 4, pp. 1772-1781, 2008.

[26] M. H. Rashid, “Electronic Ballast,” in *Power electronic handbook*, Burlington, Elsevier, 2011, pp. 573-590.

Chapter 3. Analytical Mathematical modelling of the CSCP-PFC

3.1 Introduction

In the previous chapter, the state-of-the-art techniques to analyse and model CSCP-PFC has been reviewed. It has been shown that there are several inconsistencies and errors in the existing analytical model and, therefore, there is a demand for a more precise and accurate analytical mathematical derivation for the system. The new model should be able to calculate circuit components to achieve PFC and to predict the circuit parameters such as voltages and currents at various points of the system. The focus of this chapter is to propose a more precise mathematical model operating with a DC input voltage with a view to modifying the DC to allow it to work with a full wave rectified input voltage. A describing function (FMA) approach is taken to develop the model. At the end of this chapter, the derived mathematical model is evaluated using circuit simulation tools.

3.2 Mathematical analysis of the system

In this section the process of obtaining mathematical derivations for each part of the system is shown step by step. These equations describe voltages, currents, and impedances at various locations in the circuit. The input and output energy of the system is defined and by using the law of energy balance unknown terms are eliminated provide an analytical solution. The full derivation of the model is done using Maple mathematical software as the expressions are long and tedious to derive by hand. Since the purpose of this chapter is to demonstrate the derivation of a model and some equations are too long and detract from this presentation, they have been omitted but can be found in appendix 1.

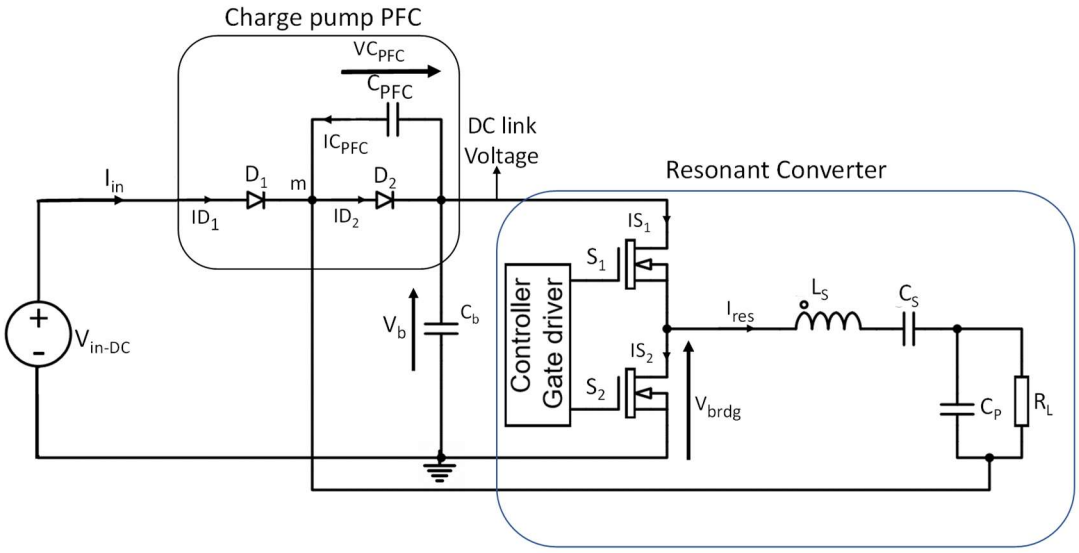


Figure 3.1: The CSCP-PFC circuit diagram with DC input Voltage.

3.2.1 Assumptions of the mathematical model

The circuit diagram for the converter is given in figure 3.1. In order to ease the mathematical modelling of the circuit several assumptions are made:

1. The input power source is assumed to be a DC source rather than a low-frequency full-wave rectified sinusoidal waveform. After evaluation of the model with DC input voltage, the AC voltage source will be implemented on the model.

2. Although D_1 and D_2 conduct at different times during a high-frequency period, their conduction times are identical.

3. As FMA is used to analyse the circuit it is assumed that the resonant current is sinusoidal and is defined by,

$$I_{res(t)} = I_{res-p} \times \sin((\omega_s \times t) + \alpha) \tag{3.1}$$

where $I_{res\text{-}p}$ is the peak value of the sinusoidal current, ω_s is the angular velocity of the switching frequency. Angle α is the phase shift between bridge voltage (V_{brdg}) and the resonant current and is given by (3.2).(The time intervals in (3.2) are demonstrated in figure 3.2)

$$\alpha = \omega_s(t_1 - t_0) \tag{3.2}$$

Moreover, another angle that is introduced later in the derivations is β. Angle β is given by,

$$\beta = \omega_s(t_2 - t_0) \tag{3.3}$$

To simplify the derivations, the resonant current may be represented by,

$$I_{res(t)} = I_{res-p} \times \sin(\theta + \alpha) \tag{3.4}$$

replacing time by the angle $\theta = \omega_s t$. This allows the various time intervals to be represented by angles.

3.2.2 Describing function model

The principle behind describing function analysis is that the non-linearity of a circuit can be replaced by a complex impedance allowing the response to be estimated using AC circuit techniques. The key assumption to applying this technique is that the dominant waveforms are sinusoidal or can be represented to a sufficient accuracy by a sinusoid (As demonstrated by FMA technique in previous chapter). Since the resonant circuit operates as a bandpass

filter attenuating the high-frequency components of V_{brdg} such that only the fundamental component $V_{brdg<1>}$ contributes to the output power and the resonant current $I_{res(t)}$. If the quality factor of the resonant tank is sufficiently high then the resonant current, $I_{res(t)}$, can be considered to a sinusoidal waveform. Since I_{res} flows through the circuit components the corresponding voltage (and current) waveforms can be defined. For the CPCS-PFC the resonant current flows into C_{pfc} causing the voltage at node m, V_m, to oscillate between Vin and Vb as it turns on D_1 and D_2 respectively. The interaction between I_{res}, C_{pfc} and D_1, D_2 is complex and non-linear and the describing function method transforms this behaviour into an impedance which is substituted into an equivalent circuit which is more easily analysed. Figure 3.2 demonstrates the I_{res} and the voltage at node m. As shown voltage at node m oscillates between two DC levels which are V_{in-DC} when diode D_1 is conducting and V_b when diode D_2 is conducting. When diodes D_1 and D_2 are turned off the resonant current flows through the C_{pfc} charging or discharging it. As demonstrated in figure 3.1 the resonant current flows directly through node m. Therefore, in order to obtain a complex impedance of the combination of D_1, D_2 and C_{pfc}, first the fundamental component of V_m ($V_{m<1>}$)should be obtained then by dividing it by I_{res} it is possible to obtain the equivalent impedance (Z_{eq}).

The steps used by the analysis are:

1. describe the voltage at node m using a piecewise description consisting of two DC levels (V_{in-DC} and V_b) and (co)sinusoidal charging and discharging sections.

2. Take the Fourier transform of V_m and extract the fundamental component to provide $V_{m<1>}$, which is a complex expression.

3. Obtain the equivalent impedance (Z_{eq}) of $C_{pfc}/D_1/D_2$ by dividing $V_{m<1>}$ by I_{res}.

4. Adding the impedance of the resonant tank to the Z_{eq} to obtain the total impedance of the circuit (Z_{tot}).

5. Use energy (power) balance and diode commutation conditions to eliminate unknown variables that emerge during the analysis.

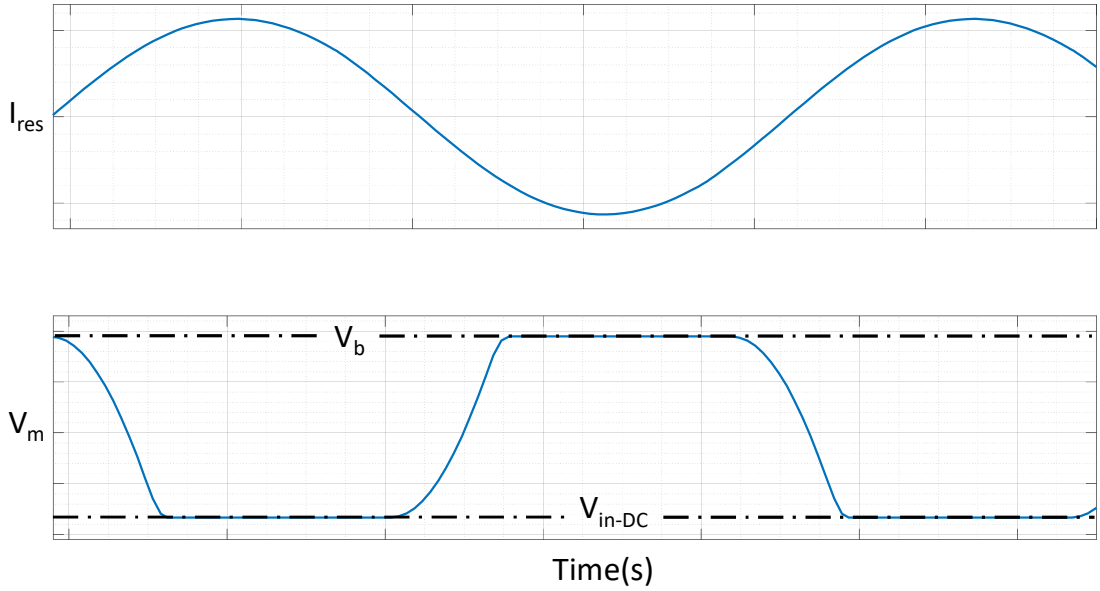


Figure 3.2: The waveforms of I_{res} and V_m.

3.2.3 Mathematical evaluation of VC_{pfc}

In order to derive piecewise mathematical expression for the VC_{pfc} the behaviour of each mode of operation needs to be analysed based on the conduction states of the diodes. The circuit configurations and waveforms from the previous chapter have been repeated here for convenience, figures 3.3 and 3.4 respectively. Moreover, the angles α and β are shown in figure 3.4.

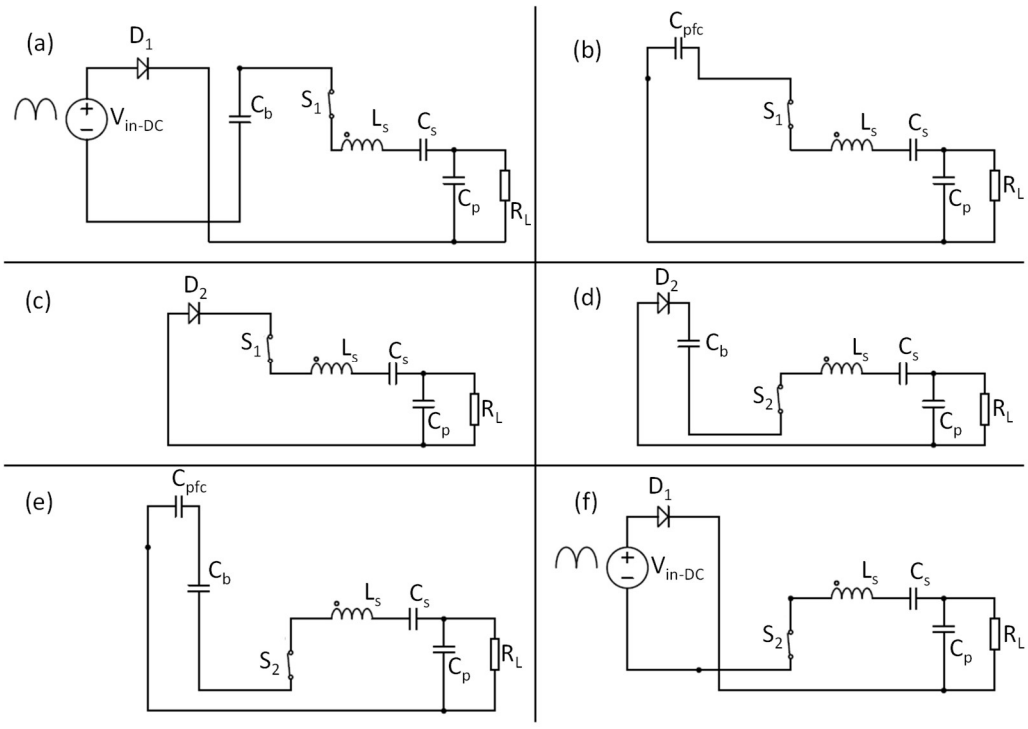


Figure 3.3: The modes of operation.

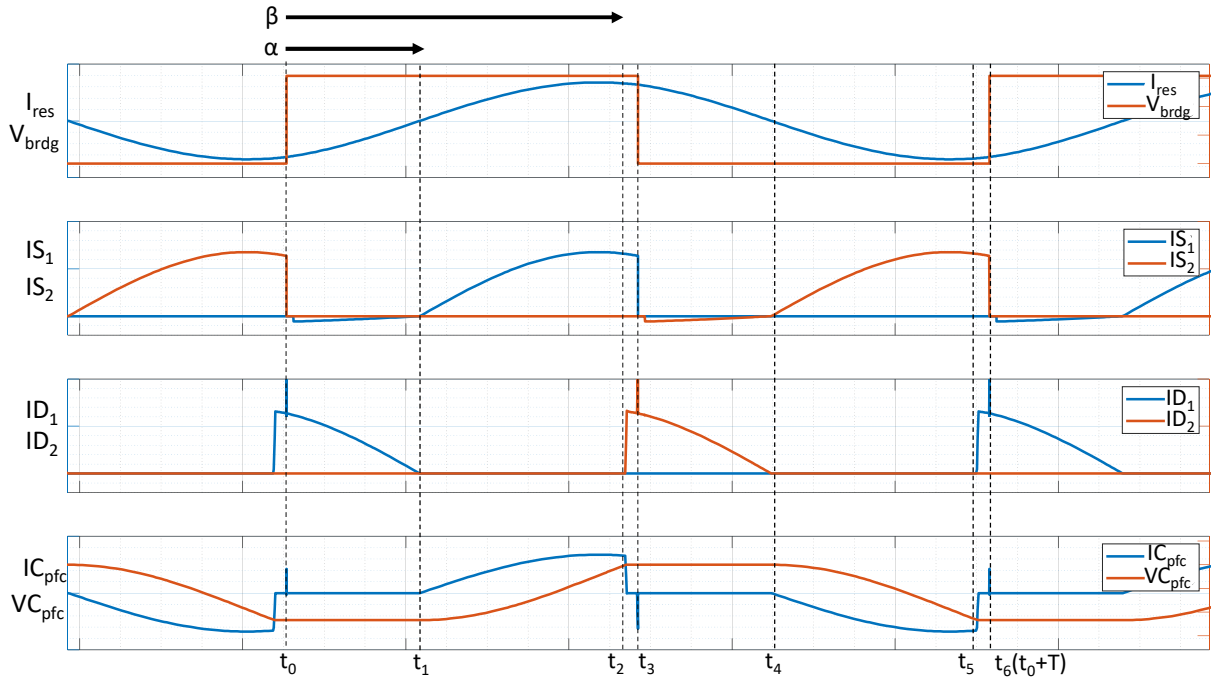


Figure 3.4: The switching waveforms of the CSCP-PFC system.

Mode a (t_0-t_1)(0<θ< α)

During Mode A, V_b is greater than zero, I_{res} is negative and D_1 is already conducting. Moreover, V_m is equal to $V_{in\text{-}DC}$. Therefore, an initial condition exists on C_{pfc}. VC_{pfc} is shown in (3.5).

$$VC_{pfc[a]} = V_b - V_{in-DC} \tag{3.5}$$

Mode A is complete when D1 turns off which is given by the condition $ID_1(t_1)= ID_1(\alpha)=0$.

Mode b (t_1-t_2)(α<θ<β)

In mode B, D1 and D2 are off. I_{res} is positive and current starts to flow through C_{pfc}. To obtain the VC_{pfc} the equations that describe the voltage-current relationship of a capacitor is needed. The general form of voltage and current in a capacitor is shown in (3.6) and (3.7) respectively, where the quantities C, V, i in the (3.6) & (3.7) are for a generic capacitor. In (3.6) the term $V_{initial}$ is the initial voltage across the capacitor [1].

$$V = \frac{1}{C} \times \int_0^t i(t) \times dt + V_{initial} = \frac{1}{\omega C} \times \int_0^{\varphi} i(\theta) \times d\theta + V_{initial} \tag{3.6}$$

$$i(t) = C \times \frac{dv(t)}{dt} \tag{3.7}$$

By evaluating (3.6) and (3.4), an equation for VC_{pfc} in mode B can be obtained. $VC_{pfc[M-2]}$ is shown in (3.8).

$$VC_{pfc[b]}(\theta) = -\frac{I_{res-p} \times \cos(-\theta + \alpha)}{\omega_s \times C_{pfc}} + V_{initial[M2]} \tag{3.8}$$

Since at the start of Mode B, $VC_{pfc[M2]}(\alpha)=0$ a value for $V_{initial}$, can be determined by substituting $\theta = \alpha$ into (3.8) and rearranging to get,

$$V_{initial[b]} = \frac{I_{res-p}}{\omega_s \times C_{pfc}} \tag{3.9}$$

The final expression is found by substituting (3.9) into (3.8)

$$VC_{pfc[b]}(\theta) = -\frac{I_{res-p} \times \cos(-\theta + \alpha)}{\omega_s \times C_{pfc}} + \frac{I_{res-p}}{\omega_s \times C_{pfc}} \tag{3.10}$$

Mode B is complete at θ=β (t=t_2 from figure 3.3) which is the instant when D2 turn-on which occurs when Vm=Vb. Referring to figure 3.2, the relationship connecting between Vm and Vb is given by,

$$V_b - V_{in-DC} = -\frac{I_{res-p} \times \cos(-\theta + \alpha)}{\omega_s \times C_{pfc}} + \frac{I_{res-p}}{\omega_s \times C_{pfc}} \tag{3.11}$$

At the start of Mode B, $V_m(\alpha)=V_{in\text{-}DC}$. Thus, (3.11) can be solved for V_b by substituting the Mode B initial value for V_m and using (3.11) to give,

$$V_b = \frac{V_{in-DC} \times \omega_s \times C_{pfc} - I_{res-p} \times \cos(-\beta + \alpha) + I_{res-p}}{\omega_s \times C_{pfc}} \tag{3.12}$$

Mode B completes at t = β and diode D_2 starts conducting.

Modes c & d (t_2-t_4)(β <θ< π+α)

During Modes C & D, I_{res} is positive and D_2 is conducting while D_1 is off. This mode ends when I_{res} reaches zero. Therefore, the $VC_{pfc\text{-}3}$ equation for this mode is shown in 3.13.

$$VC_{pfc[c\ \&\ d]}(\theta) = V_b - V_{in-DC} \tag{3.13}$$

By substituting equation 3.12 in 3.13, $VC_{pfc[M3]}$ can be written as equation 3.14.

$$VC_{pfc[c\ \&\ d]} = \frac{V_{in-dc} \times \omega_s \times C_{pfc} - I_{res-p} \times \cos(-\beta + \alpha) + I_{res-p}}{\omega_s \times C_{pfc}} - V_{in-DC} \quad (3.14)$$

Since D2 is conducting VC_{pfc} is constant. Mode D completes when I_{res} reaches zero and ID_2 becomes zero. Therefore, D_2 turns off.

Mode e (t_4-t_5)(π+α <θ< π+β)

In the duration of mode E, I_{res} is negative, both D_1 & D_2 are off and C_{pfc} is discharging. By using (3.6), an expression $VC_{pfc[M4]}$, can be obtained since the current flowing out of C_{pfc} is I_{res},

$$VC_{pfc[e]}(\theta) = -\frac{I_{res-p} \times \cos(-\theta + \alpha)}{\omega_s \times C_{pfc}} + V_{initial[M4]} \quad (3.15)$$

The initial condition can be found by evaluating (3.15) at θ=π+α. Specifically, setting the left hand side of (3.15) to (3.13) and then rearranging,

$$V_b - V_{in-DC} = -\frac{I_{res-p} \times \cos(-\pi)}{\omega_s \times C_{pfc}} + V_{initial[M4]} \quad (3.16)$$

$$V_{initial[e]} = \frac{V_b \times \omega_s \times C_{pfc} - V_{in-DC} \times \omega_s \times C_{pfc} - I_{res-p}}{\omega_s \times C_{pfc}} \quad (3.17)$$

Combining (3.15) and (3.17) provides the complete expression,

$$VC_{pfc[e]}(\theta) = -\frac{I_{res-p} \times \cos(-\theta + \alpha)}{\omega_s \times C_{pfc}} + \frac{V_b \times \omega_s \times C_{pfc} - V_{in-DC} \times \omega_s \times C_{pfc} - I_{res-p}}{\omega_s \times C_{pfc}} \quad (3.18)$$

By substituting (3.12) into (3.18), V_b can be removed from (3.18),

$$VC_{pfc[e]}(\theta) = -\frac{I_{res-p} \times \cos(-\theta + \alpha)}{\omega_s \times C_{pfc}} - \frac{I_{res-p} \times \cos(-\beta + \alpha)}{\omega_s \times C_{pfc}} \quad (3.19)$$

This mode ends when VC_{pfc} falls to zero, VCpfc(π+β)=0.

Mode f (t_5-t_6)(π+ β <θ< 2π)

In the final mode, I_{res} is negative and D_1 is conducting while D_2 is off. This mode is the same as mode A and, therefore, $VC_{pfc\text{-}5}$ is equal to zero as shown in (3.20).

$$VC_{pfc[f]} = V_b - V_{in-DC} \tag{3.20}$$

Mode F ends when θ=2π.

Equations (3.5, 3.10, 3.14, 3.19 and 3.20) can be combined into a single piecewise equation describing the evolution of VC_{pfc} over a complete cycle. Note that only five equations are required to describe six modes since the change in the bridge voltage does not affect VC_{pfc}.

$$VC_{pfc} = \begin{cases} V_b - V_{in-DC} & 0 < \theta < \alpha \\ -\frac{I_{res-p} \times \cos(-\theta + \alpha)}{\omega_s \times C_{pfc}} + \frac{I_{res-p}}{\omega_s \times C_{pfc}} & \alpha < \theta < \beta \\ \frac{V_{in-dc} \times \omega_s \times C_{pfc} - I_{res-p} \times \cos(-\beta + \alpha) + I_{res-p}}{\omega_s \times C_{pfc}} - V_{in-DC} & \beta < \theta < \pi + \alpha \\ -\frac{I_{res-p} \times \cos(-\theta + \alpha)}{\omega_s \times C_{pfc}} - \frac{I_{res-p} \times \cos(-\beta + \alpha)}{\omega_s \times C_{pfc}} & \pi + \alpha < \theta < \pi + \beta \\ V_b - V_{in-DC} & \pi + \beta < \theta < 2\pi \end{cases} \tag{3.21}$$

3.2.4 Mathematical expression for voltage V_m

The next step is to obtain an expression for voltage at node m, (V_m). V_m has the same waveform as VC_{pfc} but with a DC offset equal to $V_{in\text{-}DC}$. Moreover, in the first and last modes when diode D_1 is conducting the voltage at node m is equal to the input voltage($VC_{pfc[M1]}$ and $VC_{pfc[M5]}$) hence the equation for V_m, is given by,

$$V_m = \begin{cases} V_{in-DC} & 0 < \theta < \alpha \\ -\frac{I_{res-p} \times \cos(-\theta + \alpha)}{\omega_s \times C_{pfc}} + \frac{I_{res-p}}{\omega_s \times C_{pfc}} + V_{in-DC} & \alpha < \theta < \beta \\ \frac{V_{in-dc} \times \omega_s \times C_{pfc} - I_{res-p} \times \cos(-\beta + \alpha) + I_{res-p}}{\omega_s \times C_{pfc}} & \beta < \theta < \pi + \alpha \\ -\frac{I_{res-p} \times \cos(-\theta + \alpha)}{\omega_s \times C_{pfc}} - \frac{I_{res-p} \times \cos(-\beta + \alpha)}{\omega_s \times C_{pfc}} + V_{in-DC} & \pi + \alpha < \theta < \pi + \beta \\ V_{in-DC} & \pi + \beta < \theta < 2\pi \end{cases} \tag{3.22}$$

3.2.5 Extracting the fundamental component of V_m

The equivalent impedance presented by the charge-pump (CPFC, D1 and D2) to the resonant circuit is now derived. Voltage V_m is represented by the fundamental component of its Fourier series expansion giving $V_{m<1>}$. Then, dividing by $V_{m<1>}$ provides the equivalent impedance.

Based on the Fourier theorem every periodic function can be expressed as an infinite sum of sinusoidal and cosine waveforms which operate at integer multiples of the fundamental frequency. Each of these waveform components have specific amplitude and phase coefficients. (3.23) shows the general form of the Fourier series[2]. (The (3.23) is only for demonstration of Fourier series and its variables are not related to analysis of CSCP-PFC).

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} (a_n \times \cos\frac{2 \times n \times \pi \times t}{T} + b_n \times \sin\frac{2 \times n \times \pi \times t}{T}) \quad (3.23)$$

In (3.23), f(t) is the periodic function, n is the component integer number, T is the fundamental time period of f(t) and t is the time. The terms a_0, a_n and b_n are described in (3.24), (3.25) and (3.26) respectively [2].

$$a_0 = \frac{2}{T} \times \int_0^T f(t)dt \quad (3.24)$$

$$a_n = \frac{2}{T} \times \int_0^T f(t) \times \cos\frac{2 \times n \times \pi \times t}{T} dt \quad (3.25)$$

$$b_n = \frac{2}{T} \times \int_0^T f(t) \times \sin\frac{2 \times n \times \pi \times t}{T} dt \quad (3.26)$$

By evaluating the Fourier series with n=1 the fundamental component of V_m can be obtained. Since the resonant circuit acts like a bandpass filter, the circuit does not respond to the DC (average) term and so the a_0 component can be neglected. Equations (3.25) and (3.26) are applied to piecewise description of (3.22), where each section of V_m is individually evaluated and the contributions combined to provide the sinusoidal (b_n) contribution (3.27) and the co-sinusoidal (a_n) contribution (3.28).

$$V_{m<1>-sine} = -\frac{I_{res-p}(\frac{\cos(-2\beta+\alpha)}{2} + (\beta-\alpha)\sin(\alpha) - \frac{\cos(\alpha)}{2})}{\pi \times \omega_s \times C_{pfc}} \quad (3.27)$$

$$V_{m<1>-cos} = -\frac{I_{res-p}(\frac{\sin(-2\beta+\alpha)}{2} + (\beta-\alpha)\cos(\alpha) - \frac{\sin(\alpha)}{2})}{\pi \times \omega_s \times C_{pfc}} \quad (3.28)$$

3.2.6 Analysis of impedances of the system

The equivalent impedance is now determined using Ohm's law by dividing the fundamental component $V_{m<1>}$ by the resonant current. In (3.29) term j is the imaginary operator and provides the necessary 90° phase shift between the cos and sin contributions.

$$Z_{eq} = \frac{V_{m<1>}}{I_{res}} = \frac{V_{m<1>-sine} + j \times V_{m<1>-cos}}{I_{res-p} \times j \times e^{-(j\times\alpha)}} \tag{3.29}$$

By substituting (3.27) and (3.28) into (3.29), Z_{eq} can be described as (3.30).

$$Z_{eq} = \frac{(j + 2\beta - 2\alpha)e^{2j\alpha} - je^{-2j\beta}}{2 \times \pi \times \omega_s \times C_{pfc}} \tag{3.30}$$

The equivalent impedance Z_{eq} replaces components C_{pfc}, D_1 and D_2 resulting in an AC equivalent circuit. The impedance of resonant tank can be divided into two parts, the series impedance Z_s which is associated with L_s and C_s, and parallel impedance Z_p which is for R_L and C_p. The series and parallel impedances are described in (3.31) and (3.32) respectively.

$$Z_s = (j \times \omega_s \times L_s) - (\frac{1}{\omega_s \times C_s}) \tag{3.31}$$

$$Z_p = \frac{1}{\frac{1}{R_L} + (j \times \omega_s \times C_p)} \tag{3.32}$$

The total impedance of the tank is the summation of Z_p and Z_s. (3.33) demonstrates the resonant tank impedance (Z_{tank}).

$$Z_{tank} = (j \times \omega_s \times L_s) + (\frac{1}{\omega_s \times C_s}) + \frac{1}{\frac{1}{R_L} + (j \times \omega_s \times C_p)} \tag{3.33}$$

The total impedance of the system is the summation of (3.31) and (3.30).

3.2.7 Mathematical evaluation of I_{res} based on impedance

The square wave voltage V_{brdg} is applied to Z_{tot} is an square wave. Applying the describing technique to extract the fundamental component of V_{brdg} provides the equivalent voltage as seen by the circuit, $V_{brdg<1>-p}$ is the peak value of the fundamental component of the V_{brdg}.

$$V_{brdg<1>-p} = \frac{2 \times V_b}{\pi} \tag{3.34}$$

By using (3.34) for the voltage and (3.33) for the impedance, a new mathematical expression for $I_{res\text{-}p}$ can be obtained as described in (3.35).

$$I_{res-p} = \frac{2 \times V_b}{\pi \times |Z_{tot}|} \tag{3.35}$$

where the term abs(Z_{tot}) represents the modulus of the complex number. Moreover, as Z_{tot} is a complex impedance, the phase shift α between V_{brdg} and I_{res} can be determined by (3.36).

$$\tan(\alpha) = \frac{Im\ (Z_{tot})}{Re(Z_{tot})} \tag{3.36}$$

where Im(Z_{tot}) is the imaginary part and Re(Z_{tot}) is the real part. Rearranging (3.36) provides angle α,

$$\alpha = \arctan\ (\frac{Im\ (Z_{tot})}{Re(Z_{tot})}) \tag{3.37}$$

3.2.8 Analysis of input/output energy of the system

Up to this point several equations have been demonstrated for I_{res}, $I_{res\text{-}p}$, V_b and α. However, due to a high number of unknowns in these equations, it is not possible to solve them to predict the behaviour of the model. Therefore, another set of equations are needed to solve the system of equations and obtain a precise mathematical model for the system. The additional equations are based on the law of energy balance. This law states that the input energy to the system is equal the output energy. In CSCP-PFC system, the energy that flows in the system from $V_{in\text{-}DC}$ has to be equal the energy dissipated in the load resistor R_L when considered over the duration of a cycle.

In order to obtain an equation for output energy, first an expression for voltage across R_L is required (V_{out}). The equation for V_{out} is shown in equation 3.36.

$$V_{out} = V_{out-p}\ \times \sin\ (\omega_s \times t) \tag{3.38}$$

The term $V_{out\text{-}p}$ in (3.38) is the peak value of the V_{out}. The $V_{out\text{-}p}$ can be calculated using $I_{res\text{-}p}$ and the parallel impedance described in (3.32). $V_{out\text{-}p}$ is shown in (3.39).

$$V_{out-p} = \frac{I_{res-p}}{\left| \frac{1}{\frac{1}{R_L} + (j \times \omega_s \times C_p)} \right|} \tag{3.39}$$

The next step is to derive an expression for the output power (power dissipated in the resistor R_L). (3.40) describes the power dissipation (P_{out}) for R_L.

$$P_{out} = \frac{V_{out-p}^2 \times \sin(\omega_s \times t)^2}{R_L} \tag{3.40}$$

In order to use energy balance law, an expression for energy is needed. Therefore, to obtain output energy equation(E_{out}), (3.40) needs to be integrated over one switching period. (3.41) shows the output energy.

$$E_{out} = \frac{-V_{out-p}^2 \times (\frac{\cos(2\pi) \times \sin(2\pi) \times \omega_s}{2\pi} - \omega_s) \times \pi}{R_L \times {\omega_s}^2} \tag{3.41}$$

(3.41) can be simplified to (3.42).

$$E_{out} = \frac{V_{out-p}^2 \times \pi}{R_L \times \omega_s} \tag{3.42}$$

Finally, (3.39) can be substituted in (3.42) and output energy becomes (3.43).

$$E_{out} = \frac{{I_{res-p}}^2 \times \pi}{\left|\frac{1}{R_L} + (j \times \omega_s \times C_p)\right|^2 \times \omega_s \times R_L} \tag{3.43}$$

In the next stage is to define the input energy to the system. The first step is to calculate the input power which is the product of $V_{in\text{-}DC}$ and I_{in}. As it is demonstrated in figure 3.2 the only time that current flows from the $V_{in\text{-}DC}$ source to the system is while diode D_1 is conducting (modes F&A). Therefore, the input energy (E_{in}) can be calculated using (3.44).

$$E_{in} = \frac{V_{in-DC} \times (I_{res-p} \times \cos(-\beta + \alpha) + I_{res-p})}{\omega_s} \tag{3.44}$$

Energy balance allows (3.43) and (3.44) to be equated.

To solve this system of equations, two simultaneous equations are needed. The first simultaneous equation can be obtained from energy balance. In both (3.43) and (3.44) the term $I_{res\text{-}p}$ is present; hence it is possible to substitute (3.35) into (3.43) and (3.44). Therefore, the first simultaneous equation becomes,

$$E_{in} - E_{out} = 0 \tag{3.45}$$

The second simultaneous equation can be obtained from the relationship between the total impedance of the circuit and angle α from (3.36). Therefore, the second simultaneous equation can be written as (3.46).

$$(\tan(\alpha) \times Re(Z_{tot})) - Im(Z_{tot}) = 0 \tag{3.46}$$

By solving (3.45) and (3.46) angles α and β can be found and by substituting α and β into mathematical expressions of V_b and I_{res-p} these unknowns can be calculated. Therefore, the mathematical system becomes solvable for all unknowns. The full derivation of simultaneous equations are too long to be included here. Therefore, the detailed derivations are demonstrated in appendix 1.

3.3 Evaluation of the mathematical model

To evaluate the model, electrical circuit simulation packages are used. The first simulation package is LTspice. The first stage of the evaluation is to check that if the correct parameters are given to the model, the output is in the acceptable range compared to the simulation results. In this case, (3.12) that describes V_b is used. This equation is implemented in the simulation model to receive its parameters from the simulation in real time and outputs V_b based on the input parameters(α, β and I_{res-p}). In order to implement the equation, behavioural voltage sources are used. A behavioural voltage source in LTspice can be programmed to output any arbitrary waveform, in this case V_b. Figure 3.5 shows the complete simulation model. Figure 3.5a is the circuit simulation and V_{b-sim} is the actual V_b value from the simulation. Figure 3.5b is the simulation model that receives real time data such as I_{res}, V_{brdg} and ID_2 from the circuit simulation to calculate the unknowns such as angles α and β. The extracted unknowns are supplied to behavioural voltage sources B_5 and B_6 to calculate the V_b based on the mathematical expression of V_b from (3.12) (The output of B_6 is V_{b-mod}). Therefore, by comparing V_{b-sim} and V_{b-mod} it is possible to observe the operation of the mathematical model with the correct parameters given. The process of extracting the unknowns and generation of V_{b-mod} is completely discussed in the next sections.

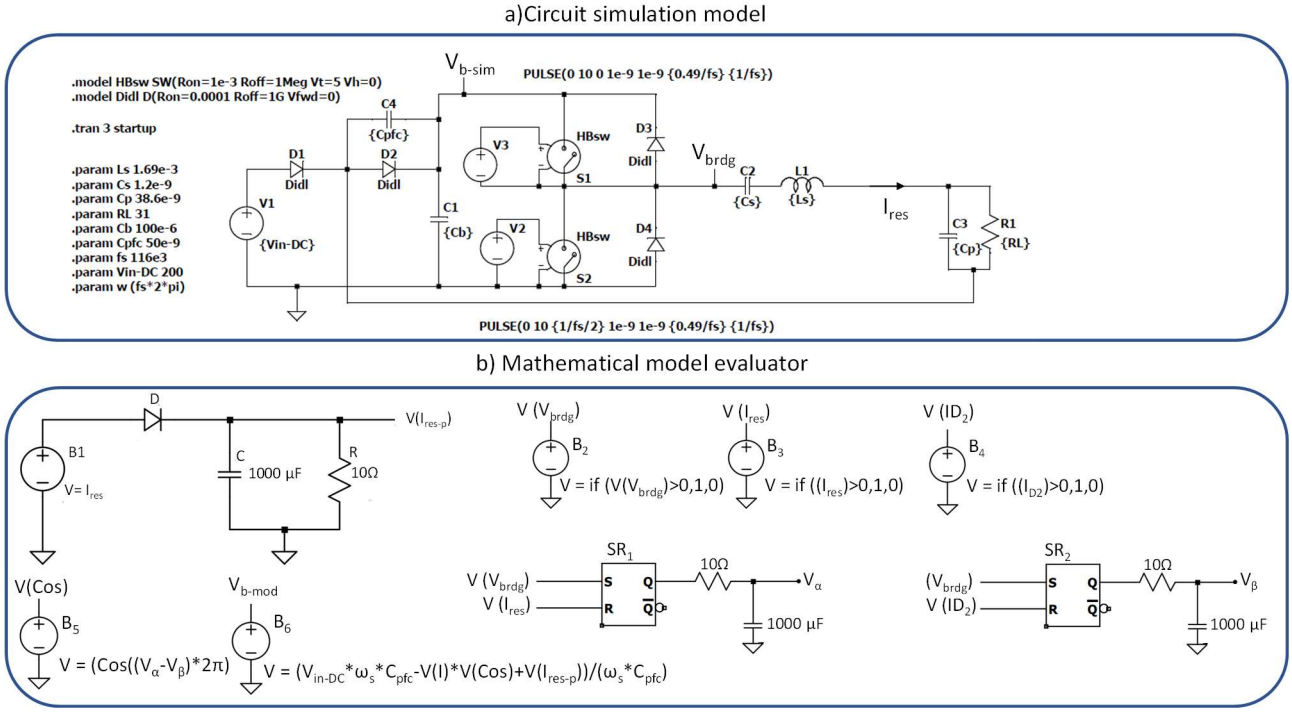


Figure 3.5: The complete simulation model for evaluation of the derived mathematical model.

3.3.1 Extraction of $I_{res\text{-}p}$

$I_{res\text{-}p}$ is the peak value of the resonant current. The circuit diagram for extraction $I_{res\text{-}p}$ is shown in figure 3.6. In figure 3.6, the behavioural voltage source B_1 is programmed to output a voltage representative of the instantaneous value of I_{res}. Therefore, by connecting the output of the behavioural voltage source to a peak detector circuit (the combination of R, C & D in figure 3.4), the value of $I_{res\text{-}p}$ can be extracted in real time from the simulation model. The R and C are designed in a way that there is little ripple voltage in the output.

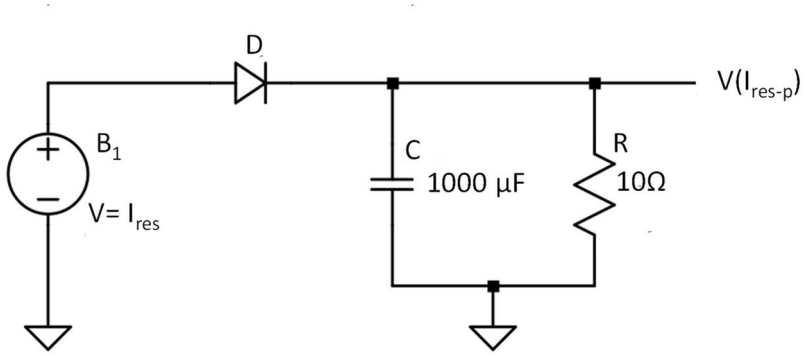


Figure 3.6: The $I_{res\text{-}p}$ extractor circuit.

3.3.2 Extraction of α and β

To extract the angles α and β from the simulation model, the circuit diagram of figure 3.7 is used. The first step to finding the angles is to transform V_{brdg} into a digital voltage $V(V_{brdg})$. The behavioural voltage source B_2 outputs 1 for when V_{brdg} is not zero and zero when V_{brdg} is zero. A similar procedure is used for I_{res} and ID_2 with outputs $V(I_{res})$ and $V(ID_2)$. For the angle α an SR flip-flop is used with input signals of $V(V_{brdg})$ and $V(I_{res})$. The output of the SR_1 is a square waveform with peak value of 1 volt and its duty cycle proportional to the angle α. By averaging the output voltage of SR_1 using the RC network shown in figure 3.7, a DC voltage that is proportional to angle α can be obtained (labelled as V_α). The values of the RC network are designed to mitigate any ripple on V_α. A same process is used to obtain the angle β (V_β). The angles are within the range of 0-2π and V_α and V_β are between zero and one (essentially a duty cycle representing an angle). Therefore, the product of V_α or V_β by 2π is the exact value of that angle in radians.

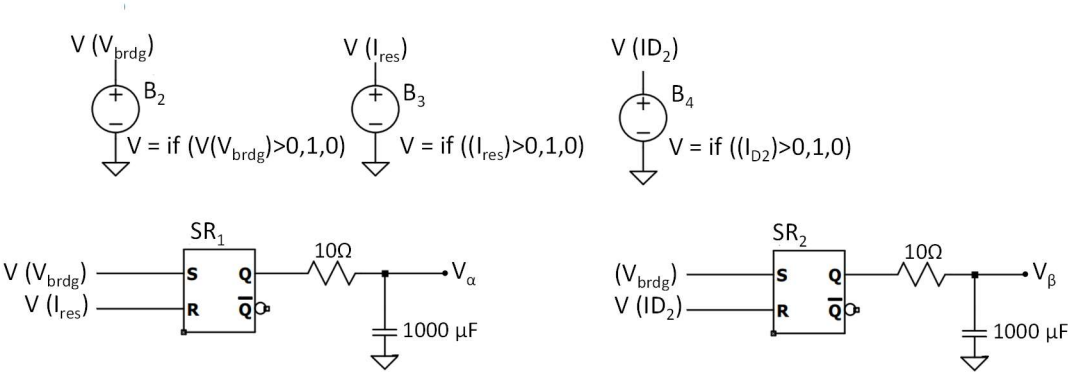


Figure 3.7: α & β extractor circuit model.

As the unknowns are extracted from the simulation circuit, it is now possible to implement the (3.12) (V_b) into the simulation using a behavioural voltage source, shown in figure 3.8. The behavioural voltage source B_5 calculates the Cosine part of the equation using the extracted angles. The voltage source B_6 receives the parameters from simulation and calculates the V_b using the mathematical model as the equation (3.12) is implemented into B_2. Then it can be compared the value of V_b from the simulation($V_{b\text{-}sim}$).

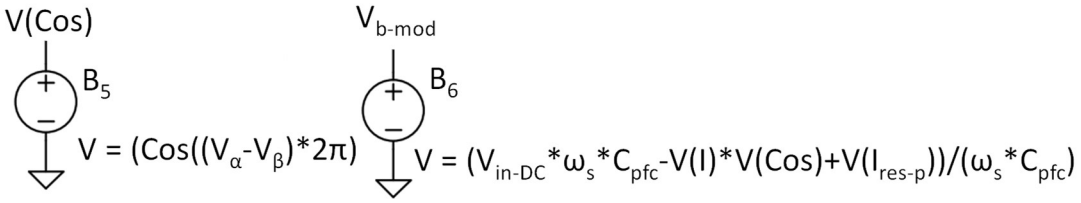


Figure 3.8: The Behavioural voltage source for generation of $V_{b\text{-}mod}$.

3.4 DC Evaluation results

In order to check the model, first it is simulated with a DC input voltage source. Table 3.1 shows the circuit parameters of the simulation. The term f_0 in table 3.1 is the resonant frequency of the resonant tank.

Component	Value	Component	Value
L_s	1.69 mH	C_s	1.2 nF
C_P	38.6 nF	R_L	31 Ohms
C_{pfc}	50 nF	f_0	112.5 kHz
$V_{in\text{-}DC}$	200 V	f_s	116 kHz

Table 3.1: The system parameters for the simulation model.

The simulation showed that the (3.12) can calculate the V_b value with less than 2% error comparing to the simulation value of V_b. The results are shown in figure 3.9. The term $V_{b\text{-}sim}$ is the V_b from the circuit simulation and $V_{b\text{-}mod}$ is the value calculated from the model equation shown in figure 3.9.

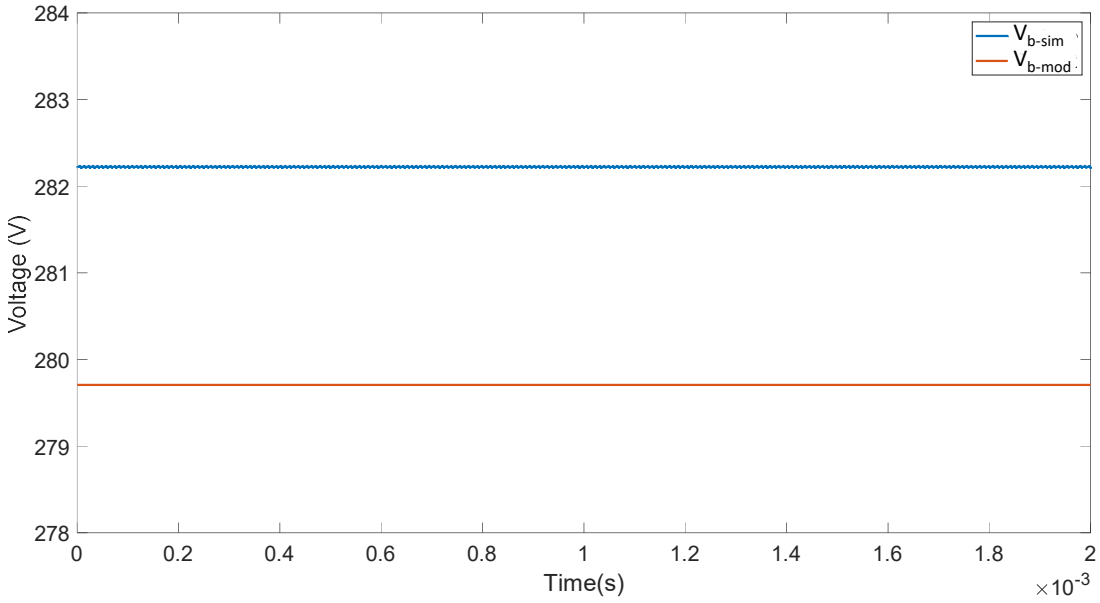


Figure 3.9: The simulation result of $V_{b\text{-}sim}$ and $V_{b\text{-}mod}$ versus time with an DC input voltage.

To completely evaluate the model, a series of simulations with different parameters for the system are done. For these simulations parametric sweep is used. The parametric sweep facility in LTspice allows to run the simulations automatically for different values of circuit parameters.

One of the key components of the system is the C_{pfc} capacitor. Therefore, the first sweep analysis is applied on this component. The C_{pfc} will be varied from 10 nF to 200 nF with increments of 10 nF. The results are shown in figure 3.10. (In figure 3.10 each data point represents the results for 1 simulation and the chart shows the results for 20 simulations)

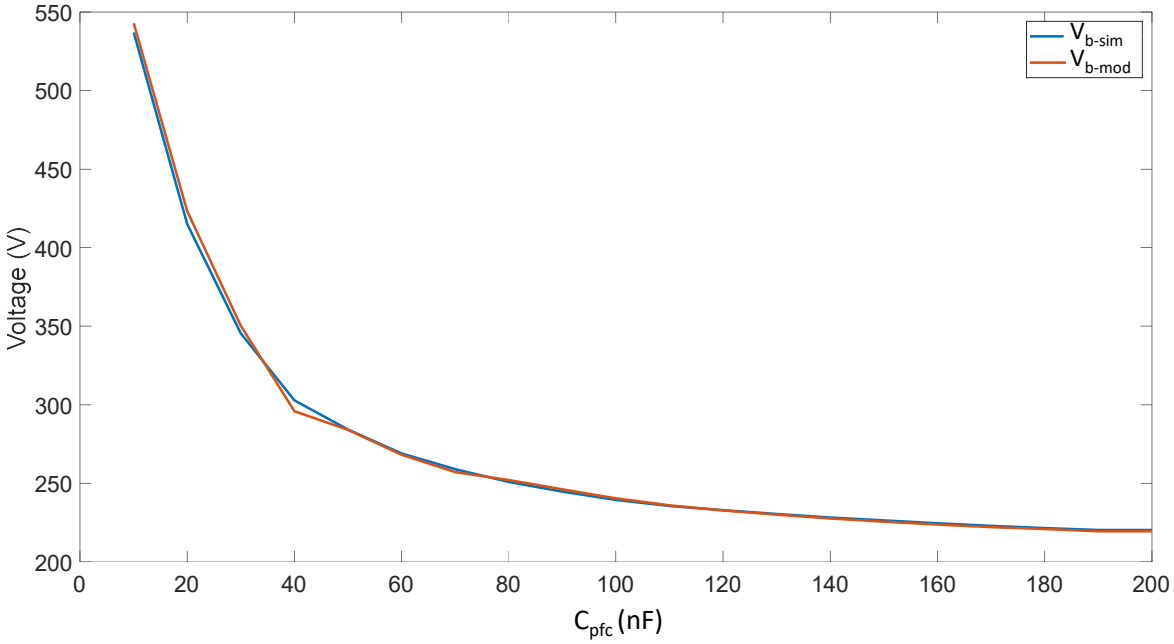


Figure 3.10: Simulation results for parametric sweep of C_{pfc}.

As it is demonstrated in figure 3.10, the simulation results can verify the operation of the model with different values of C_{pfc}.

The next parametric sweep is done on the $V_{in\text{-}DC}$. In this series of simulations $V_{in\text{-}DC}$ increases from 50 volts to 500 volts with steps of 50 volts. The results are shown in figure 3.11. In figure 3.11 the vertical axis illustrates the voltage for $V_{b\text{-}sim}$ and $V_{b\text{-}mod}$ and the horizontal axis is the $V_{in\text{-}DC}$. The results in figure 3.11 shows that the mathematical model is valid for different input voltages.

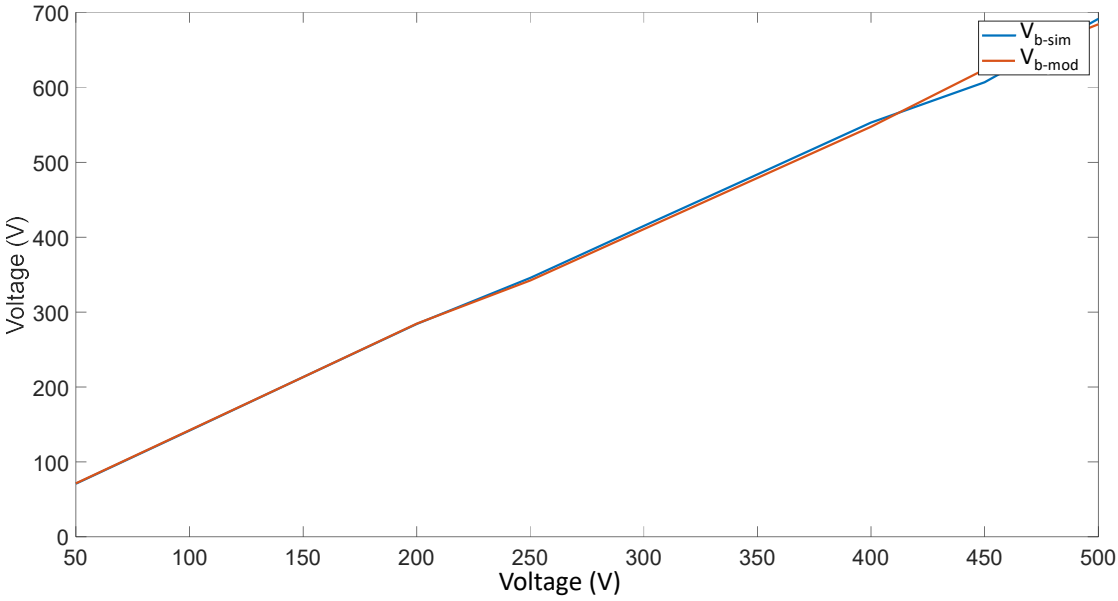


Figure 3.11: Simulation results for parametric sweep of $V_{in\text{-}DC}$(X-axis input voltage).

The last parameters that the mathematical model needs to be checked against are R_L and switching frequency f_s. For this series of simulations, the parametric sweep is done for both

parameters simultaneously. The R_L is varied from 10Ω to 100Ω with steps of 10Ω. The switching frequency increased from 91 kHz to 136 kHz with increments of 5 kHz. As there are 10 steps for each sweep, a total of 100 simulations are done. The results for $V_{b\text{-}sim}$ and $V_{b\text{-}mod}$ are demonstrated in figures 3.12 and 3.13 respectively.

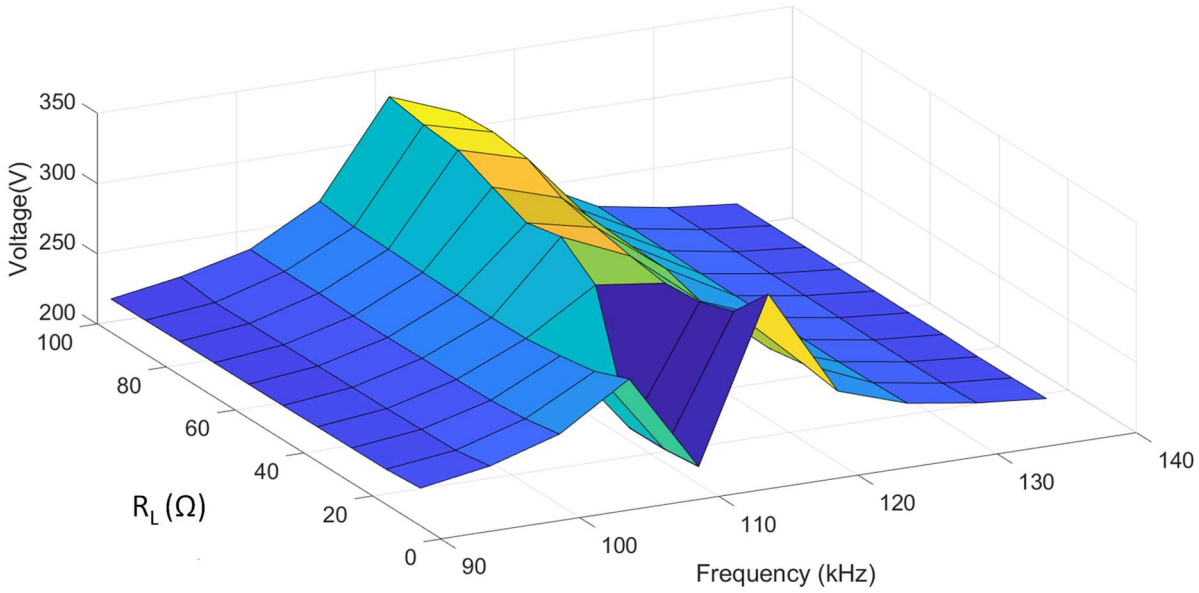


Figure 3.12: The results for $V_{b\text{-}mod}$ versus f_s & R_L

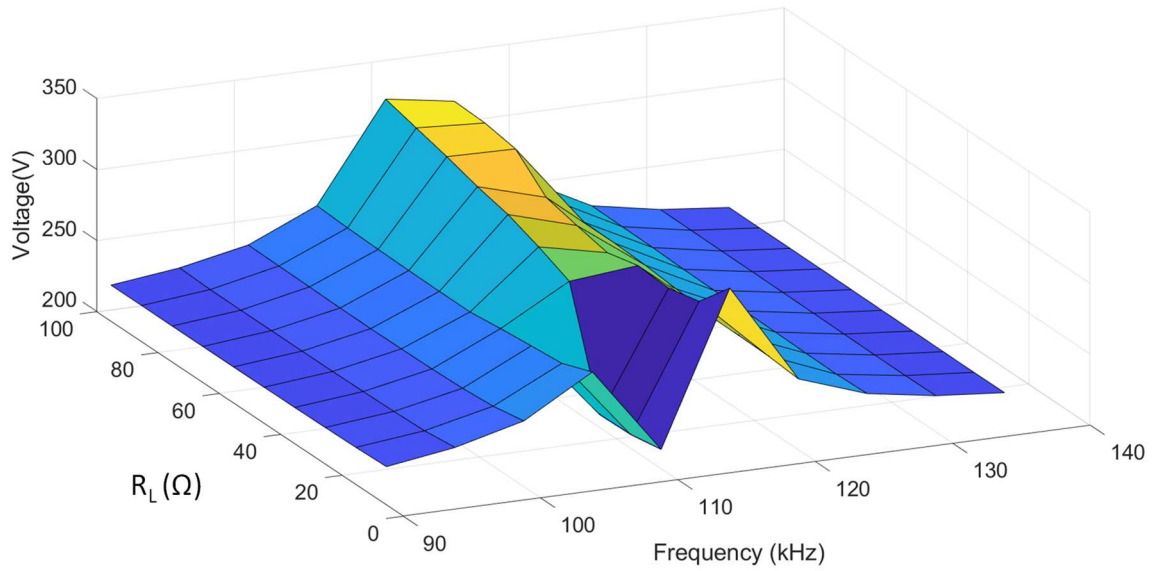


Figure 3.13: The simulation results for $V_{b\text{-}sim}$ versus f_s & R_L

The last stage of verification is to compare the results from figure 3.12 and 3.13 mathematically. For the comparison, (3.47) is used.

$$Error = \frac{|V_{b-sim} - V_{b-mod}|}{V_{b-sim}} \times 100 \quad (3.47)$$

In (3.47) the term error is the error value in percentage. This equation calculates the difference between values of $V_{b\text{-}sim}$ and $V_{b\text{-}mod}$. The difference value is then compared to the $V_{b\text{-}sim}$ and the equation outputs the error value in percentage. Results from figures 3.12 and 3.13 are compared using (3.47) and the results are demonstrated in figure 3.14.

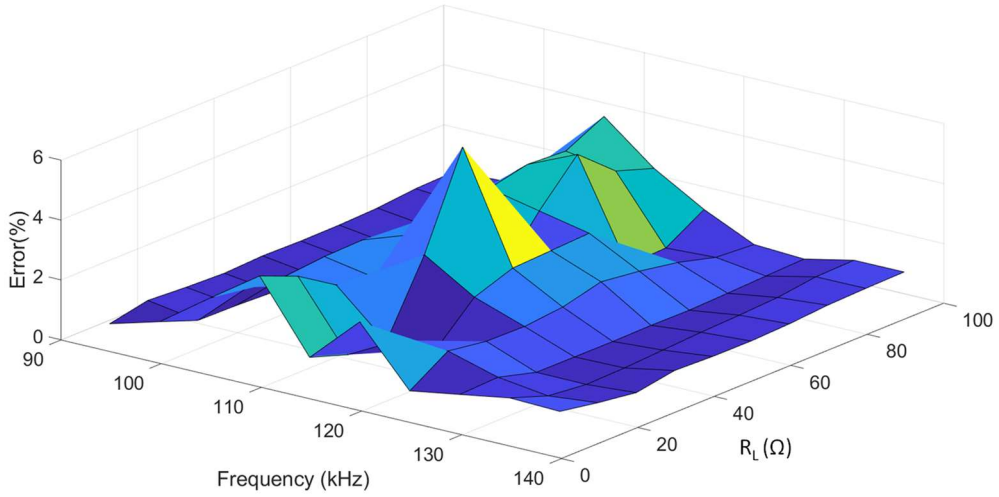


Figure 3.14: The error value in comparison of $V_{b\text{-}sim}$ & $V_{b\text{-}mod}$.

The error values in figure 3.14 are less than 5% for all the simulations. Moreover, as shown in previous figures, the mathematical derivation can predict the circuit parameters precisely with sufficiently small error values. Therefore, it can be concluded that the model can predict the system accurately with a DC input voltage. In the next section the model is tested with an AC input voltage instead of $V_{in\text{-}DC}$.

3.5 Verification of the model with an AC input voltage

In this section the same process that is used to evaluate the system with a DC input voltage is used. For these simulations the $V_{in\text{-}DC}$ is changed to a sinusoidal AC voltage source with frequency of 50 Hz and amplitude of 340 volts. This voltage source represents the grid voltage as discussed in chapter 2. As the switching frequency is 116 kHz and the input voltage is a full wave rectified sinusoidal waveform with frequency of 50 Hz it can be assumed that the input voltage to the system is a slow varying DC voltage. Therefore, the mathematical model can operate under this condition. All the other parameters of the system are the same as previous section. Figure 3.15 shows the results for $V_{b\text{-}sim}$ and $V_{b\text{-}mod}$ versus time from the first simulation. (Figure 3.15 is for one simulation and not a parametric sweep)

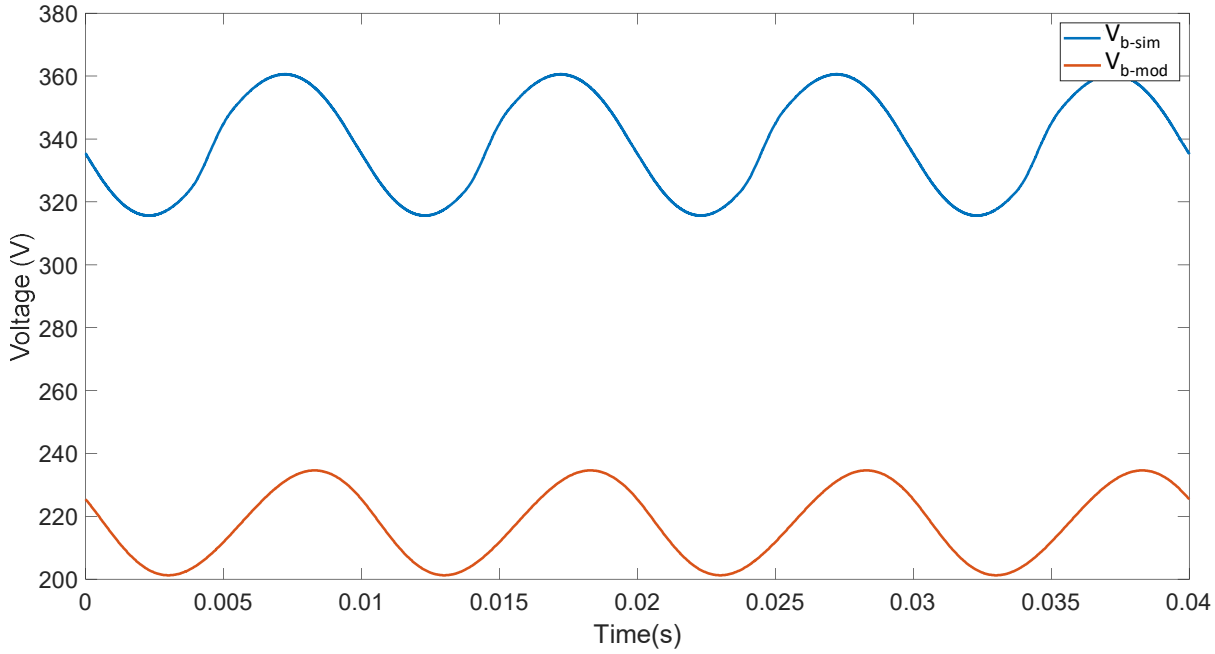


Figure 3.15: The simulation result of $V_{b\text{-}sim}$ and $V_{b\text{-}mod}$ versus time with an AC input voltage.

As it is demonstrated in figure 3.15 $V_{b\text{-}mod}$ does not match the simulation results. At this stage the model does not operate with an AC input voltage. In order to address this problem, several attempts were made to get the mathematical model to operate with AC input voltage. However, all of the attempts failed. After several failures it has been suspected that the operation of the system with an AC input voltage is different with a DC input voltage. Further investigations revealed that the modes of operation for the system with an AC input voltage is different comparing to the modes of operation that has been demonstrated in the chapter 2 and figure 3.3 in this chapter. As the first step of deriving the model was to obtain a mathematical expression VC_{pfc} and it was completely based on the modes of operation (equations 3.4-3.19).Therefore, the mathematical derivations of the model are not valid when modes of operation are different.

In order to obtain a mathematical model for the system with an AC input voltage, it is first crucial to analyse the behaviour and operation of the system with an AC input voltage. When the new mode of operation is extracted, it will be possible to acquire a new mathematical model.

In the next chapter, the operation of the system with an AC input voltage is fully investigated.

3.6 References

[1] P. Horowitz and W. Hill , “Capacitors and AC circuits,” in *The Art of Electronics*, Cambridge, Cambridge University Press, 2015, pp. 18-26.

[2] A. Croft , R. Davison and M. Hargreaves, “Fourier Series,” in *Engineering Mathematics*, Essex, Pearson Education Limited, 2001, pp. 706-713.

Chapter 4. Modes of operation

4.1 Introduction

In the previous chapter, a mathematical model for the CSCP-PFC has been demonstrated. As discussed, the model predicts the circuit operation with a very small amount of error with a DC input voltage. However, it was not possible to adapt the model for the system with an AC input voltage by just simply adjusting the value of an equivalent DC input voltage. Preliminary investigations have identified that the system operates in different modes of operation throughout the AC waveform when compared to a DC input voltage. It is essential to have the correct modes of operation for the system to be able to derive a mathematical model for it. This chapter provides a comprehensive investigation of system operation with an AC input voltage and the system parameters are varied to ensure the operation of the system is valid for variety of parameters.

4.2 The modes of operation

As discussed in previous chapters, the system operates on high frequency cycles(switching frequency, f_s) with an AC input voltage with a low frequency cycle, during each high frequency cycle the circuit configuration changes according to conduction state of the controlled switches and uncontrolled diodes(as shown in the modes of operation figures in previous chapters). The present circuit configuration can be represented by a bit-pattern (the bit-pattern is combination of the conduction state of switches and diodes) called the conduction state which encodes the conduction states of all of the switching devices. As time progresses, the switches commutate in a controlled or uncontrolled manner and each commutation event corresponds to the system entering a different circuit configuration. Therefore, the circuit behaviour can be characterised by the conduction state bit-pattern which evolves over time. Due to the repetitive excitation of the half-bridge, repeating sequences of circuit configuration (conduction states) emerge, and these are called modes of operation. As alluded to by the previous chapter, when operating with a DC input voltage and fixed load, only a single mode of operation exists. However, for a low-frequency AC input voltage the conduction states (circuit configuration) that form a modes of operation can vary and so different high-frequency modes of operation may exist within the period of the low-frequency input voltage. The purpose of this chapter is to develop a technique to identify the conduction states (bit-pattern) and modes of operation pattern that exist for AC input voltages. The investigation consists of two stages:

Stage 1: Mode extraction - identify each operating mode (circuit configuration) and extract the mode sequence.

Stage 2 Mode sequence characterisation - couples the mode extractor to a parameter to identify to identify the different mode sequences

4.3 Stage 1: Mode extraction procedure

The process of extracting the modes of operation consists of two main parts. The first part is The process of extracting the modes of operation consists of two main parts. First part is mode identification using circuit simulation where the conduction states of the controlled and uncontrolled switches are recorded for export. Second part is to import the conduction state data into MATLAB and process the data to extract the operating mode sequence of the circuit.

4.3.1 Section 1: Circuit simulation

The operating modes of the system are characterised by the conduction states of the controlled and uncontrolled switches and therefore it is essential to capture this information to understand how the mode sequence evolves during an AC cycle. Figure 4.1 shows a circuit diagram featuring the signals of interest and these are the half-bridge state (IS_1, IS_2, ID_3, ID_4), the charge-pump state (ID_1, ID_2). These states are the conduction state of the components or diodes and are discussed in detail in the next sections. As can be seen, voltage-controlled switches are used instead of MOSFETs and since the voltage-controlled switches support bidirectional current flow diodes D_5 and D_6 are used to restrict current flow in the directions shown by the IS_1 and IS_2 current arrows. Moreover, diodes D_3 and D_4 are placed as the body diodes of the MOSFETs.

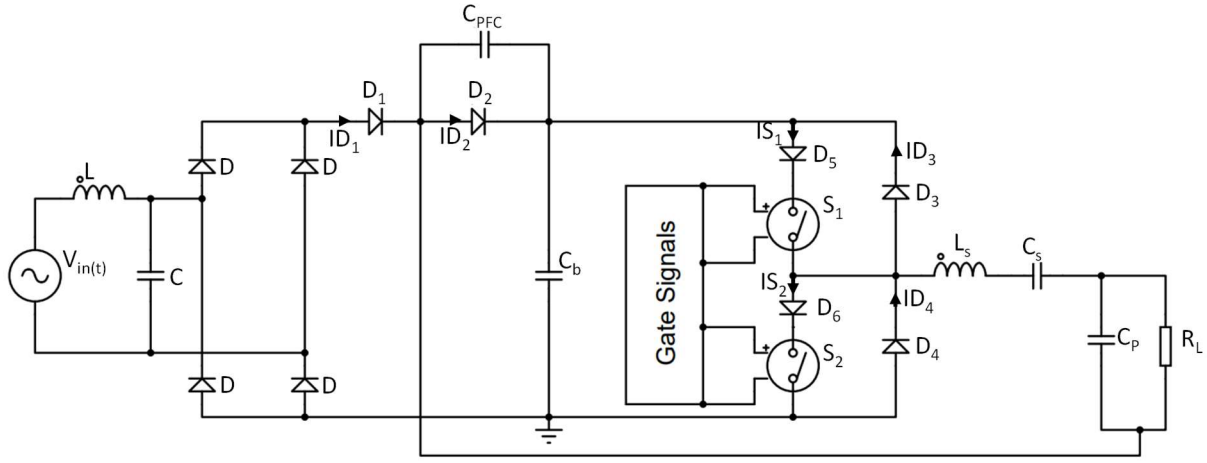


Figure 4.1: Circuit diagram of the system showing the signals of interest.

Figure 4.2 shows the actual LTSPICE simulation circuit.

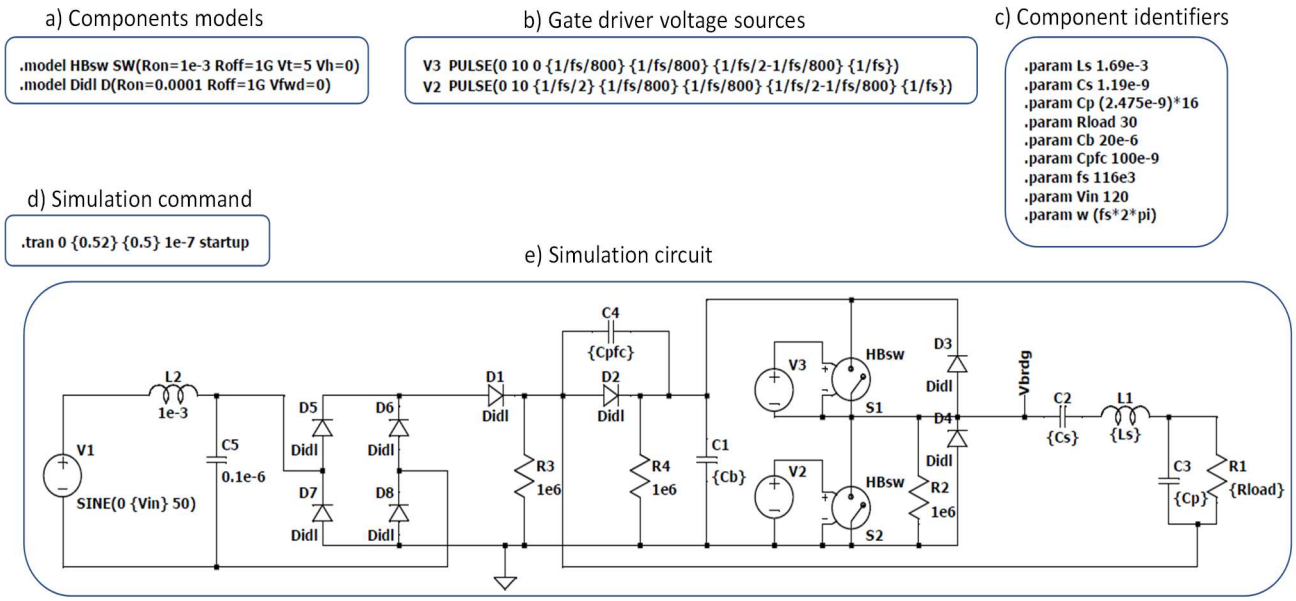


Figure 4.2: The LTspice simulation model of the system.

Figure 4.2 demonstrate the different sections of the LTspice simulation model. The different sections are as follows:

Section a: In this section the component models are defined. In this simulation the only needed models are for the ideal switch and ideal diode.

Section b: In order to drive the half bridge switches, isolated voltage sources are used. These voltage sources (V2 and V3 in the figure 4.2) produce PWM pulses with a dead time. The section b defines the parameters of the voltage sources.

Section c: In section c all the parameters of the simulation model are defined. These parameters are: the component values, input voltage and switching frequency.

Section d: In this section the parameters of the simulation such as stop time, maximum time step and time to start save data are defined.

Section d: The last part of the simulation model is the actual circuit schematic. The circuit schematic is the same as the diagrams presented in previous chapters. Moreover, resistors R2, R3 and R4 are placed to provide a ground path for diodes D1, D2 and D3. These resistors do not effect the simulation results but the speed up the simulation time.

Behavioural voltage sources utilising if statements are used to extract conduction states of the diodes and switches providing a Boolean representation of conduction, with an output of 1, if the current through the diode or the switch is greater than zero and an output of 0 for when the current is zero. This Boolean data is then used to generate a bit-pattern for the conduction state. Figure 4.3 shows the behavioural voltage sources.

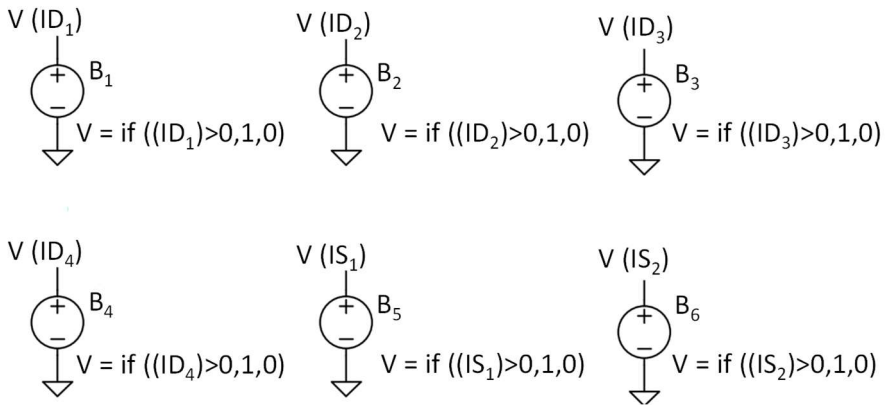


Figure 4.3: The conduction state to digital signal converter of the simulation model.

The circuit in figure 4.3 outputs 6 array of digital data representing the conduction state of the diodes or switches. As it is extremely difficult to perform signal processing in LTspice, the data is imported into MATLAB to process the signals and extract the modes. The simulation data is stored in a text file with a variable time-step.

4.3.2 Stage 2: MATLAB mode extraction simulation code

To extract the operation of the system, first the signals from figure 4.3 are imported to MATLAB. Figure 4.4 shows the block diagram for the sequence of operations performed by the MATLAB code to extract the mode sequence.

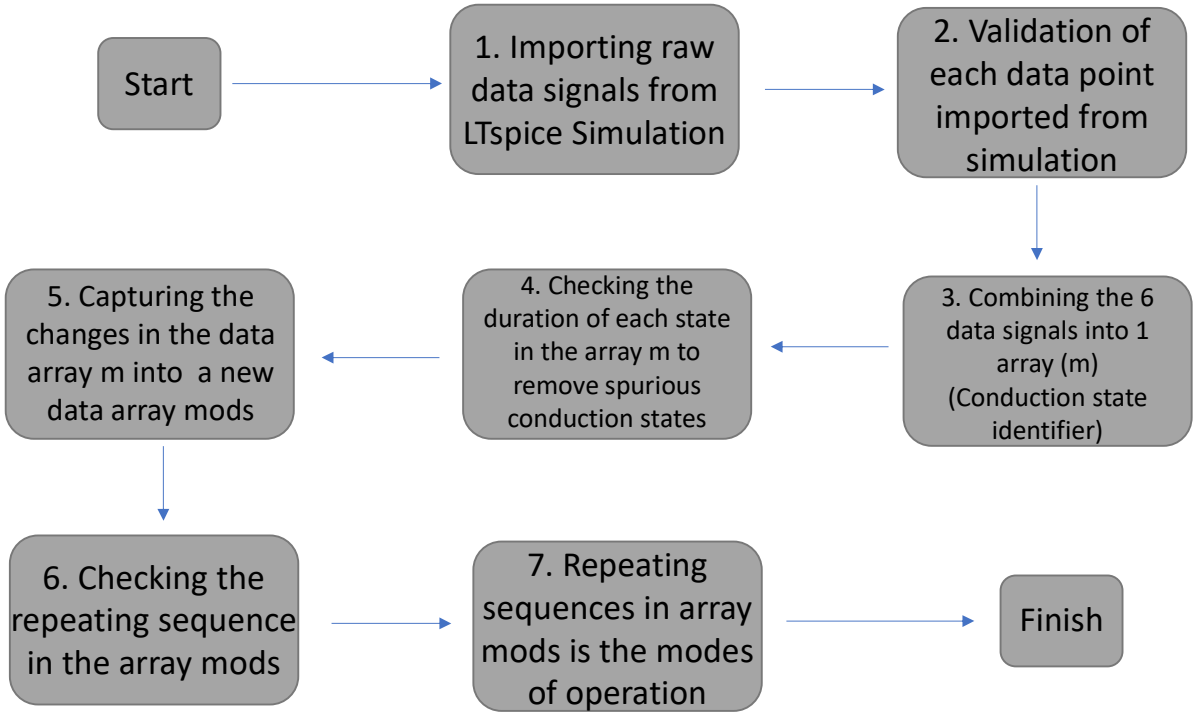


Figure 4.4: The block diagram for MATLAB mode extractor simulation code.

Step 1 – Import data: In this step, first the data file is converted from text to CSV format and then automatically imported into MATLAB.

Step 2 – Data validation: Since the raw data should be Boolean, only 1's and 0's values should be present. This section removes any non-conforming entries using the process shown by the flowchart in Figure 4.5 (only a single variable is shown for brevity). As all the data in the arrays must be checked, it goes through a for loop to check each data point. If the data point is 0 or 1, that point is valid. However, as the data is from simulation, it is possible to have data between 0 and 1 in the transition period of the behavioural voltage source. Thus, if the data point is not valid and less than 0.5, 0 is assigned for that data point and if it is more than 0.5, 1 is assigned to that data point.

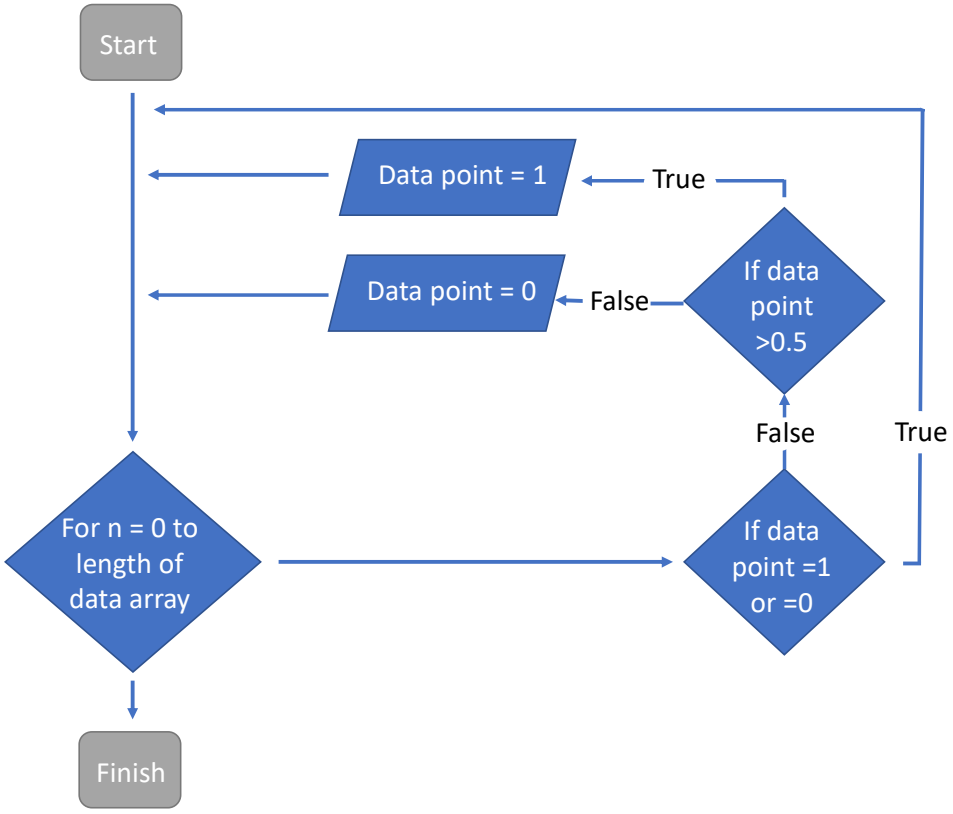


Figure 4.5: The flowchart for data verification algorithm.

Step 3 – Bit pattern generation: In this step the six conduction states are converted into a bit pattern representation such that a single integer number can represent a particular conduction state. For this purpose, equation 4.1 is used.

$$m = (V(ID_1)2^1) + (V(ID_2)2^2) + (V(ID_3)2^3) + (V(ID_4)2^4) + (V(IS_1)2^5) + (V(IS_2)2^6) \quad (4.1)$$

In equation (4.1) each data point of the data arrays is multiplied by 2 to a power as shown. Then, they are added together. Therefore, array m is the same length of the imported data arrays and each data point represents the conduction states of all diodes and switches in the system using only one integer number(Conduction state identifier). Figure 4.6 shows the flowchart of this process where n is an index generated by a for loop and used for addressing the data points.

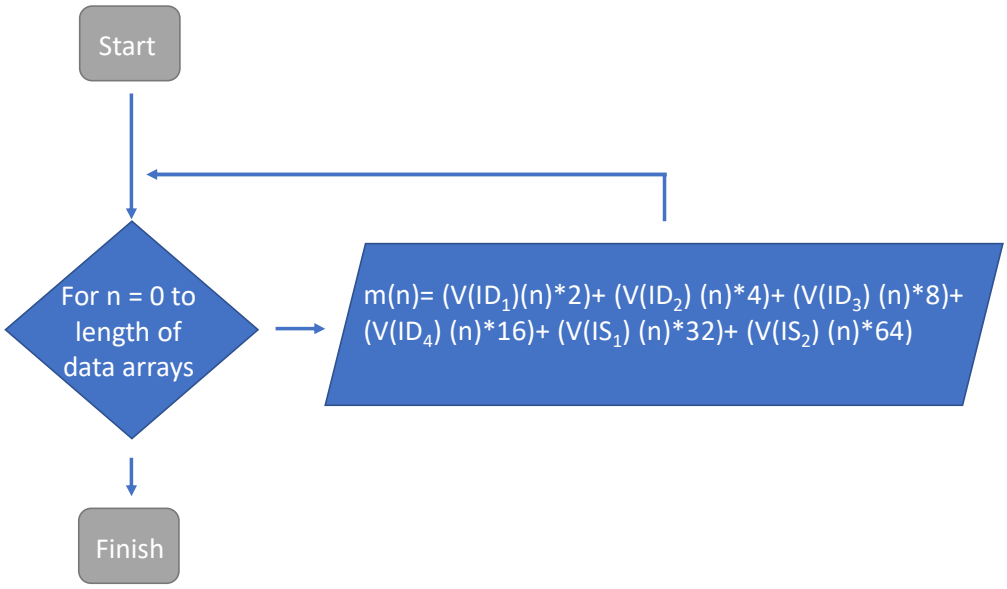


Figure 4.6: The flow chart for processing 6 conduction state signals into one data signal.

Step 4 – Mode synchronisation: The end of each mode is often characterised by switches or diodes do not turn on/off simultaneously. Thus, spurious modes can be detected when process the bit-pattern array m. To address this problem a technique similar to switch debouncing is used where the duration of a mode immediately after a transition is monitored to see if it changes again a short time later. If it does change, then this indicates the mode transition may not have settled. Specifically, the length of each mode in array m can be compared to an arbitrary threshold defined in the simulation code. If the length of the mode is greater than the threshold no change is applied. In contrast, if the length is less than the threshold, it will be changed to the previous mode value. Moreover, as there is no logical method to obtain a value for this arbitrary threshold, its value is chosen by trial and error. The flowchart for this process is shown in figure 4.7.

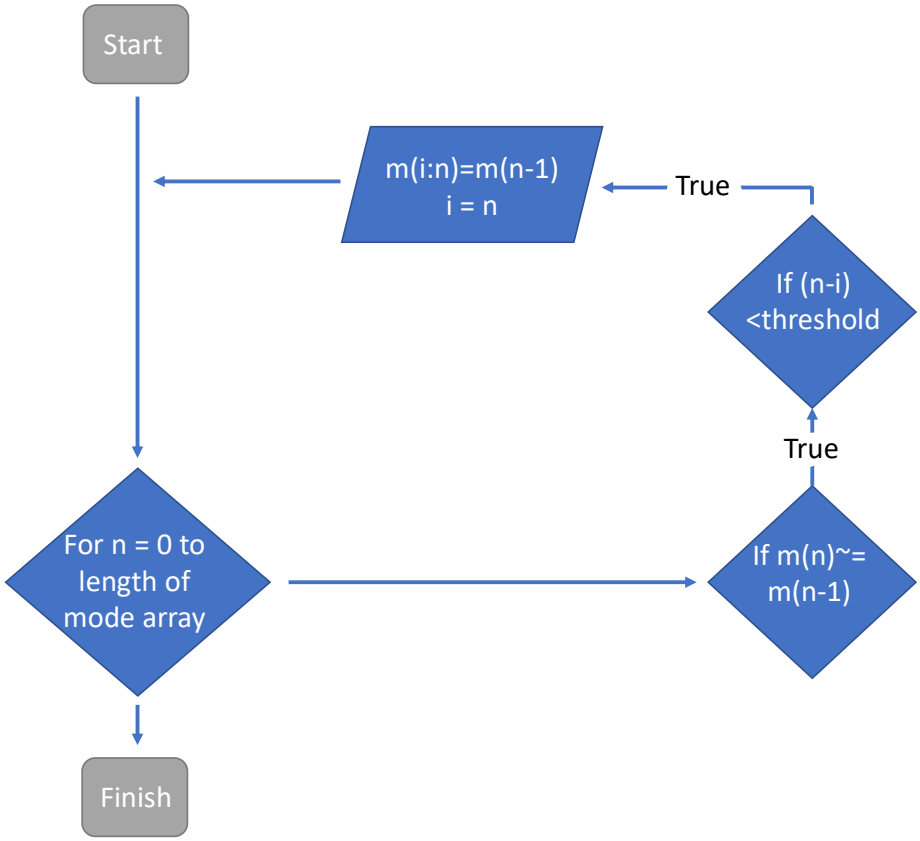


Figure 4.7: The flowchart for the process of modes validation.

In figure 4.7 the variable n is the counter for the for loop and index for addressing the data points in the arrays.

The output of step 4 is a validated switching state array free from spurious mode transitions an example which is shown by figure 4.8. A repeating sequence or cycle can clearly be seen. Each repeating sequence is the modes of operation, and the duration of each sequence is one high frequency cycle. The vertical edges represent state transitions, and the horizontal sections represent the switch state which is the combination of switches and diodes that are conducting during that period. For example, number 68 shows that switch S_2 and diode D_2 are conducting.

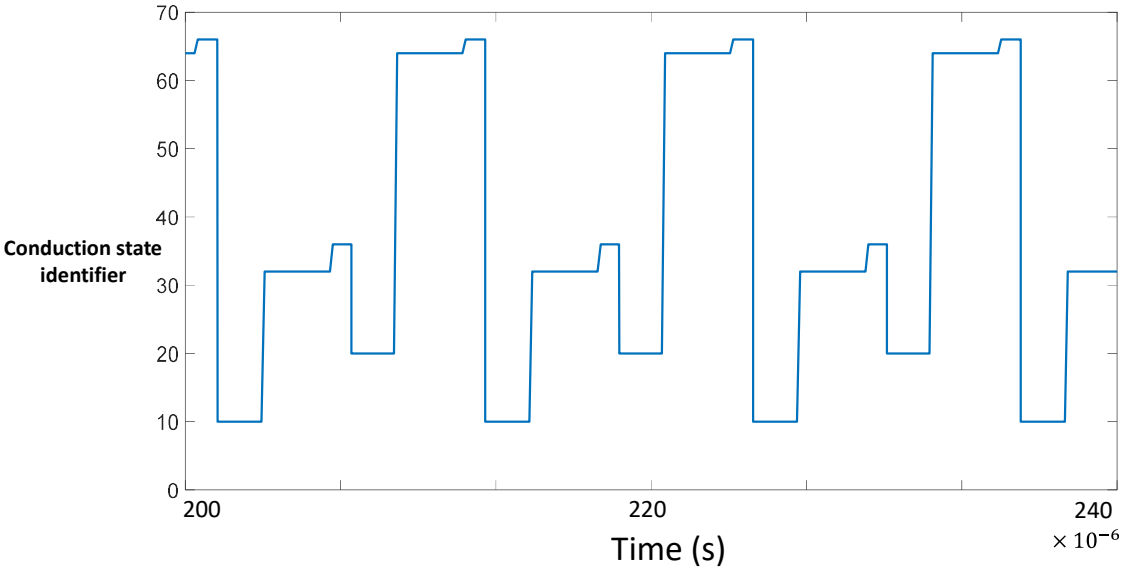


Figure 4.8: Example of modes of operation in array m.

Step 5 – Single mode transition representation: Array m represents the mode (switch state) and also the duration of each mode. In order to extract the modes of operation, only the transitions/changes conduction state in the data array m are required. The flowchart in Figure 4.9 shows how array m is processed to provide a conduction state sequence representation array d.

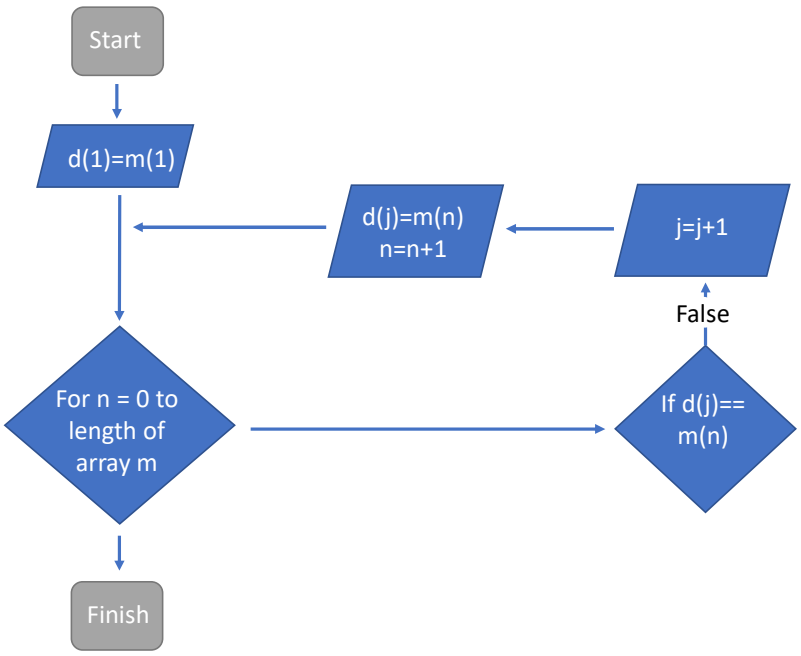


Figure 4.9: The flowchart for the processing array m into array d.

In figure 4.9 variable n is the counter for the for loop and variable j is used for addressing array d.

Steps 6&7 – Conduction state sequence extraction and identification: The last steps to extract the modes of operation is to check the array d for repeating sequences. The repeating sequences are the modes of operation. Therefore, it is possible to extract the sequences automatically and obtaining the modes of operation for the system. For this part a chain of if conditions can be used. As the modes of operation in array d is represented by a repeating sequence of numbers(repeating sequence of conduction states), each if condition checks the value in array d for specific pre-defined number (Specific conduction state) and if that number is detected the programme output one and move to the next if condition for the next conduction state. This process continues until the pre-defined sequence of the numbers finishes and then starts over until all the data points in the array d is checked.

The complete MATLAB code for mode extraction in shown in appendix 2.

4.4 Simulation Investigation

In order to verify the operation and behaviour of the system, the simulations are done on 3 different circuit parameters for the system. Moreover, the simulations are done with both AC and DC input voltage sources. The circuit parameters are shown in tables 4.1 to 4.3. (The first circuit parameters are the same as simulation model in previous chapters)

Component	Value	Component	Value
L_s	1.69 mH	C_s	1.2 nF
C_P	38.6 nF	R_L	31 Ohms
C_{pfc}	50 nF	C_b	100 µF
f_s	116 kHz	f_0	112 kHz

Table 4.1: The component values for the circuit 1.

Component	Value	Component	Value
L_s	1 mH	C_s	2 nF
C_P	20 nF	R_L	31 Ohms
C_{pfc}	10 nF	C_b	100 µF
f_s	120 kHz	f_0	113.5 kHz

Table 4.2: The component values for the circuit 2.

Component	Value	Component	Value
L_s	400 µH	C_s	7 nF
C_P	30 nF	R_L	31 Ohms
C_{pfc}	30 nF	C_b	100 µF
f_s	105 kHz	f_0	98 kHz

Table 4.3: The component values for the circuit 3.

4.5 Extracted modes of operation

The results of the simulations revealed 8 different modes of operations depending on system parameters and conditions. In this section the 8 modes of operation are demonstrated and in the next section it is shown that how the modes of operation varies with changes in circuit parameters.

The first mode of operation (M1) is illustrated in table 4.4. The first row in table 4.4 specifies which modes of operation the table is demonstrating (The letter M is prefix and the number after the prefix identifies which mode of operation the table is demonstrating). The second row shows the conduction states that occur in that mode of operation. For example, modes of operation M1 has 6 conduction states (S1-6). The number attached to each state shows the conduction state bit-pattern number from the MATLAB simulation code (Array d from previous section). Lastly, the column for each state S1-6 demonstrates which components are conducting in the duration of that conduction state (Components marked X are conducting during that conduction state).

Mode of operation 1 (M1)						
Conduction state	S1(66)	S2(10)	S3(32)	S4(36)	S5(20)	S6(64)
D_1	X	X				
D_2				X	X	
D_3		X				
D_4						
S_1			X	X		
S_2	X				X	X

Table 4.4: The modes of operation M1.

The seven other modes of operationM2-8 are demonstrated in tables 4.5 to 4.11 respectively.

Mode of operation 2 (M2)						
Conduction state	S1(64)	S2(8)	S3(10)	S4(32)	S5(16)	S6(20)
D_1			X			
D_2						X
D_3		X	X			
D_4					X	X
S_1				X		
S_2	X					

Table 4.5: The modes of operation M2.

Mode of operation 3 (M3)								
Conduction state	S1(66)	S2(10)	S3(34)	S4(32)	S5(36)	S6(20)	S7(22)	S8(70)
D_1		X	X				X	X
D_2	X				X	X	X	X
D_3		X						
D_4						X	X	
S_1			X	X	X			
S_2	X							X

Table 4.6: The modes of operation M3.

Mode of operation 4 (M4)				
Conduction state	S1(64)	S2(8)	S3(32)	S4(16)
D_1				
D_2				
D_3		X		
D_4				X
S_1			X	
S_2	X			

Table 4.7: The modes of operation M4.

Mode of operation 5 (M5)						
Conduction state	S1(64)	S2(66)	S3(10)	S4(32)	S5(20)	S6(18)
D_1		X	X			X
D_2					X	
D_3			X			
D_4					X	X
S_1				X		
S_2	X	X				

Table 4.8: The modes of operation M5.

Mode of operation 6 (M6)								
Conduction state	S1(66)	S2(10)	S3(34)	S4(32)	S5(36)	S6(38)	S7(22)	S8(70)
D_1		X	X			X	X	X
D_2	X				X	X	X	X
D_3		X						
D_4							X	
S_1			X	X	X	X		
S_2	X							X

Table 4.9: The modes of operation M6.

Mode of operation 7 (M7)							
Conduction state	S1(66)	S2(10)	S3(32)	S4(36)	S5(20)	S6(22)	S8(70)
D_1		X				X	X
D_2	X			X	X	X	X
D_3		X					
D_4					X	X	
S_1			X	X			
S_2	X						X

Table 4.10: The modes of operation M7.

Mode of operation 8 (M8)							
Conduction state	S1(66)	S2(10)	S3(34)	S4(32)	S6(38)	S7(22)	S8(70)
D_1		X	X		X	X	X
D_2	X				X	X	X
D_3		X					
D_4						X	
S_1			X	X	X		
S_2	X						X

Table 4.11: The modes of operation M8.

4.6 The modes of operation for the system with DC input voltage

The results for the 3 simulations with component values of table 4.1-4.3 illustrated that the system with a DC input voltage has the same modes of operation regardless of component values. For all the simulations with a DC input voltage the mode of operation is M1 as demonstrated in table 4.4.

The modes of operation demonstrated in table 4.4 are partially different to the operation demonstrated in previous chapters. The cause of the difference is the body diodes of the switches (D_3&D_4) that are implemented in the simulation models. In the analysis in the previous chapters the switches and their associated body diode were treated as a single component. Moreover, in table 4.4 if the conduction state of the switches and their associated body diodes are merged together, the results would be the same as the modes of operation discussed in chapters 2 and 3.

4.7 Mode extraction results of the system with an AC input voltage

The simulation for the system with a DC input voltage verified the modes of operation. Moreover, the results also validated the simulation model and the MATLAB mode extraction simulation code. In the next stage, the system can be tested with an AC input voltage. For

these simulations the values of tables 4.1-4.3 are used. However, the value of C_{pfc} is varied to investigate the operation of the circuit under different conditions. As discussed in previous chapters the component responsible for achievement of unity power factor is C_{pfc}. Therefore, the operation of the system can be divided into 3 conditions. The condition are as follow:

- PF under-corrected: This condition is when the C_{pfc} is less than the value needed to achieve unity PF.
- PF corrected: This condition is when the C_{pfc} value is correct for unity PF.
- PF Over-corrected: In this condition the value for C_{pfc} is more than the needed value for power factor correction.

The input voltage and current waveforms for conditions stated above are shown in figure 4.10.

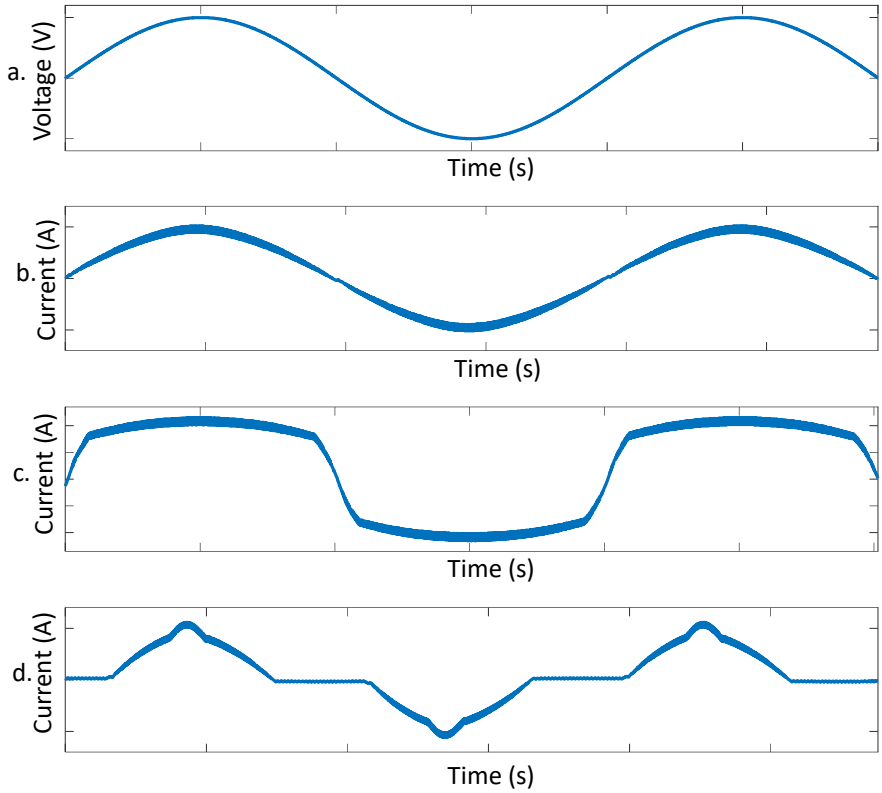


Figure 4.10: a. Grid input voltage, b. Input current when PF corrected, c. input current PF under-corrected, d. input current PF over-corrected.

The simulations for the system with an AC input voltage, showed that different mode of operation can occur depending on the PFC condition. In the next section the extracted modes of operation for the system with AC input voltage are demonstrated.

4.6.1. The modes of operation for circuit 1 with an AC input voltage

The system with values from table 1 is examined under 3 different PF conditions. For the circuit 1 the PFC can be achieved by using 45 nF capacitor as C_{pfc}.

The first condition simulated is PF under corrected. For this purpose, the C_{pfc} is 10 nF. The simulation showed that in this condition the mode of operation is M1 for 1 grid voltage cycle (50 Hz/20 ms).

The second simulation is for PF corrected condition. In this simulation 3 different modes of operation are detected M1-3. The modes of operation change with the input voltage. Figure 4.11 shows the input voltage, current and the detected modes of operation .

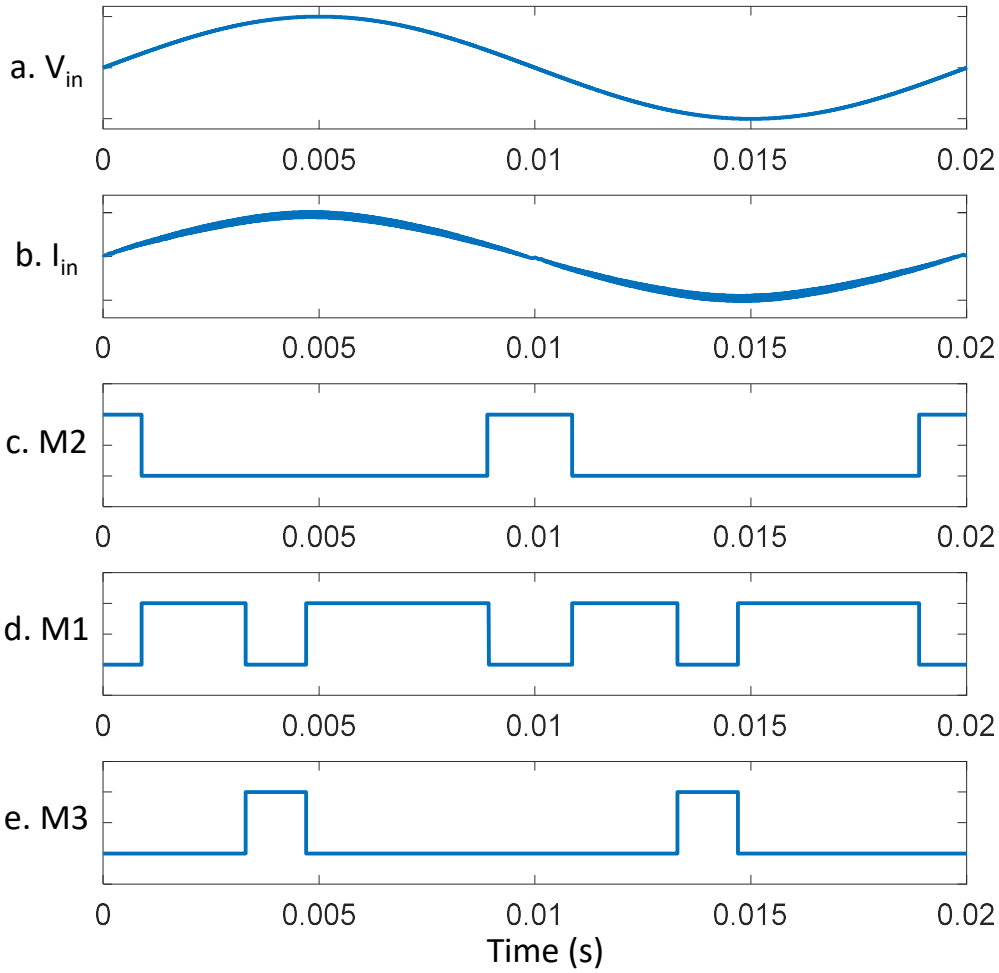


Figure 4.11: The modes of operation for circuit 1 with an AC input voltage (PF corrected).

In figure 4.11 the waveforms a and b are the input voltage and current versus time respectively. The waveforms c, d and e are the extracted modes of operation and when they are one it shows that the associated mode of operation is detected.

The last simulation for the circuit 1 is for the PF over-corrected condition. The modes of operation for this simulation are different to the modes demonstrated so far and three new

modes are detected(M4, M5 and M6). The results for this simulation are demonstrated in figure 4.12.

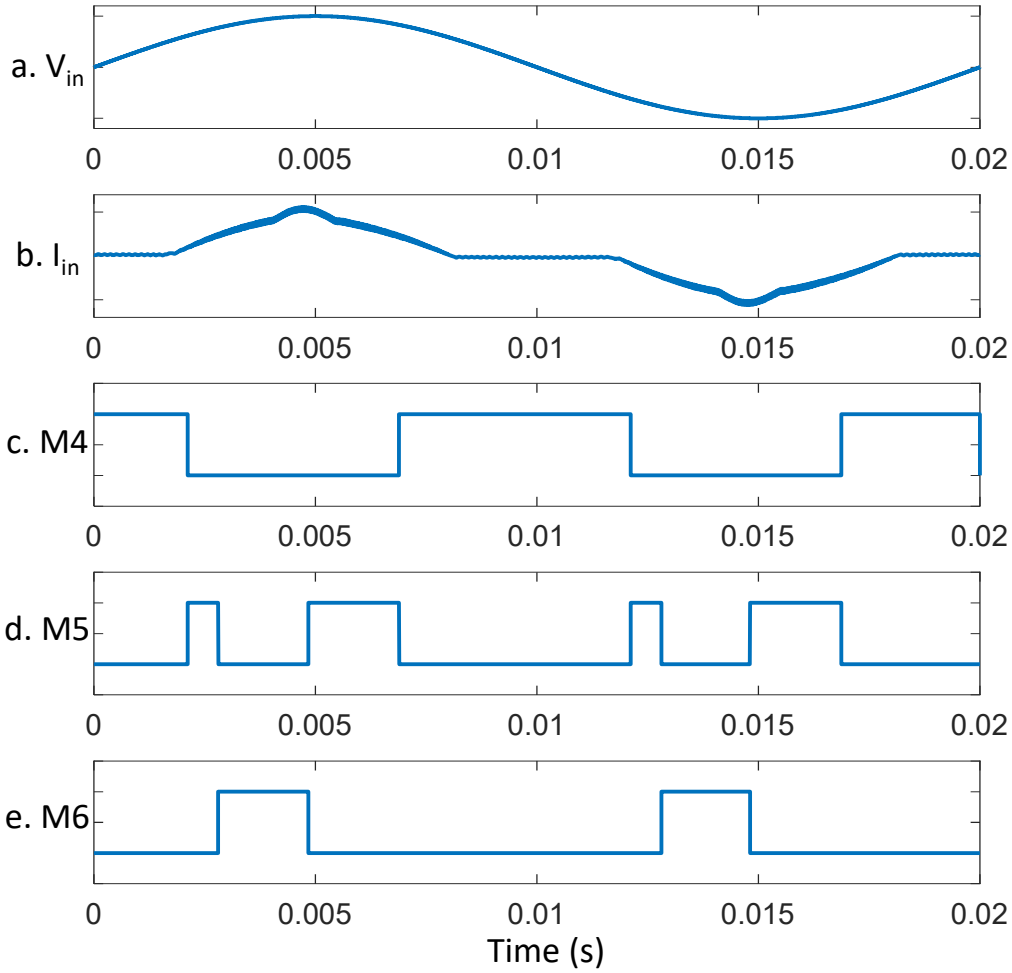


Figure 4.12: The modes of operation for circuit 1 with an AC input voltage (PF over-corrected).

4.6.2. The modes of operation for circuit 2 with an AC input voltage

The circuit 2 has also been simulated for the three PF conditions the same as circuit 1. In order to achieve near unity power factor, the C_{pfc} has to be 27 nF. The simulation for circuit 2 with PF under-corrected condition showed that the circuit has a single mode of operation and it is M1 the same as circuit 1 when operating PF under-corrected. For this simulation C_{pfc} is 5 nF.

The next simulation is done while the system is operating at PF corrected condition. For this simulation 2 modes of operation are detected. The first one is M1 and the second one is M7. The results for this simulation are shown in figure 4.13.

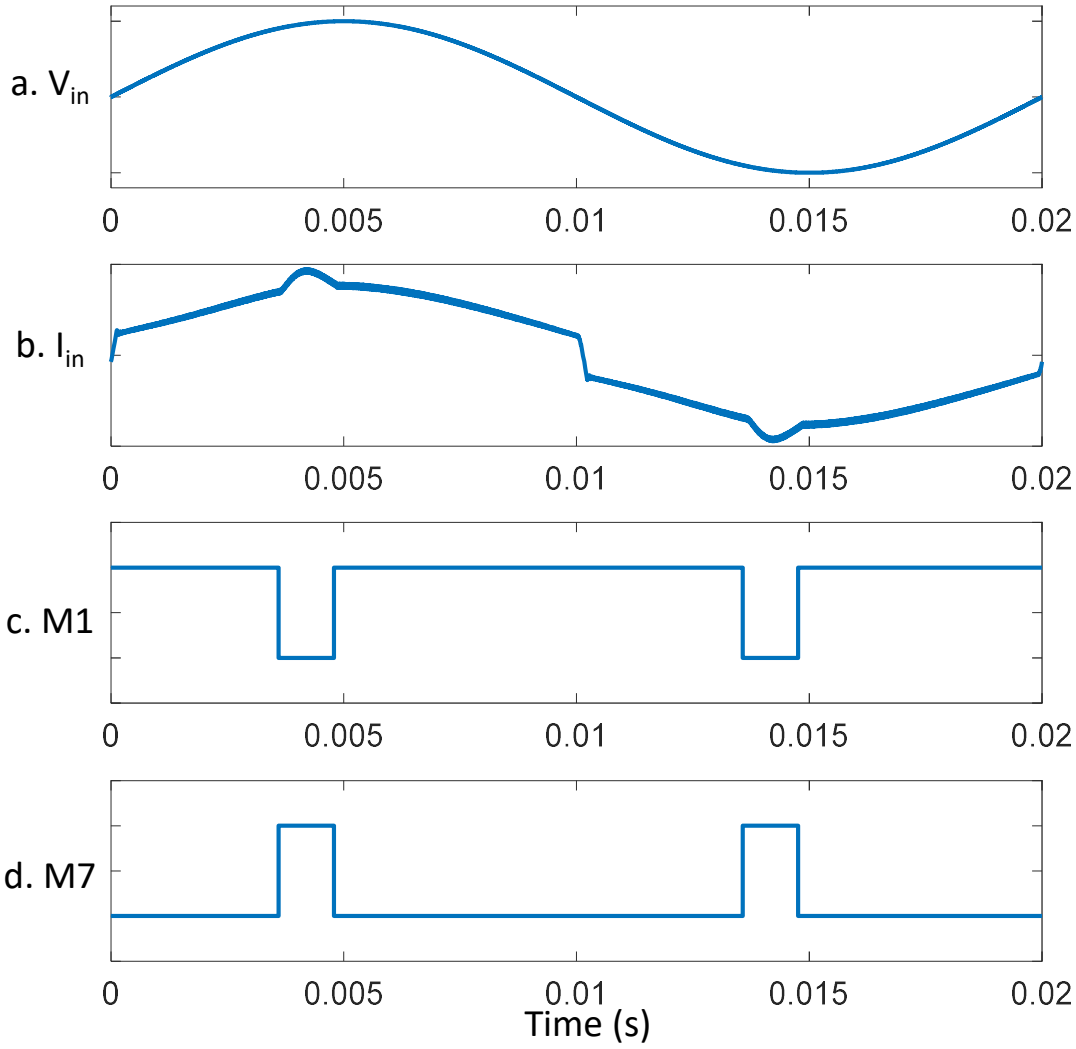


Figure 4.13: The modes of operation for circuit 2 with an AC input voltage (PF corrected).

The last simulation for the circuit 2 is the PF over-corrected condition. For this simulation the C_{pfc} is 60 nF. The detected modes for this simulation are M1, M4 and M6. Figure 4.14 shows the results for this simulation.

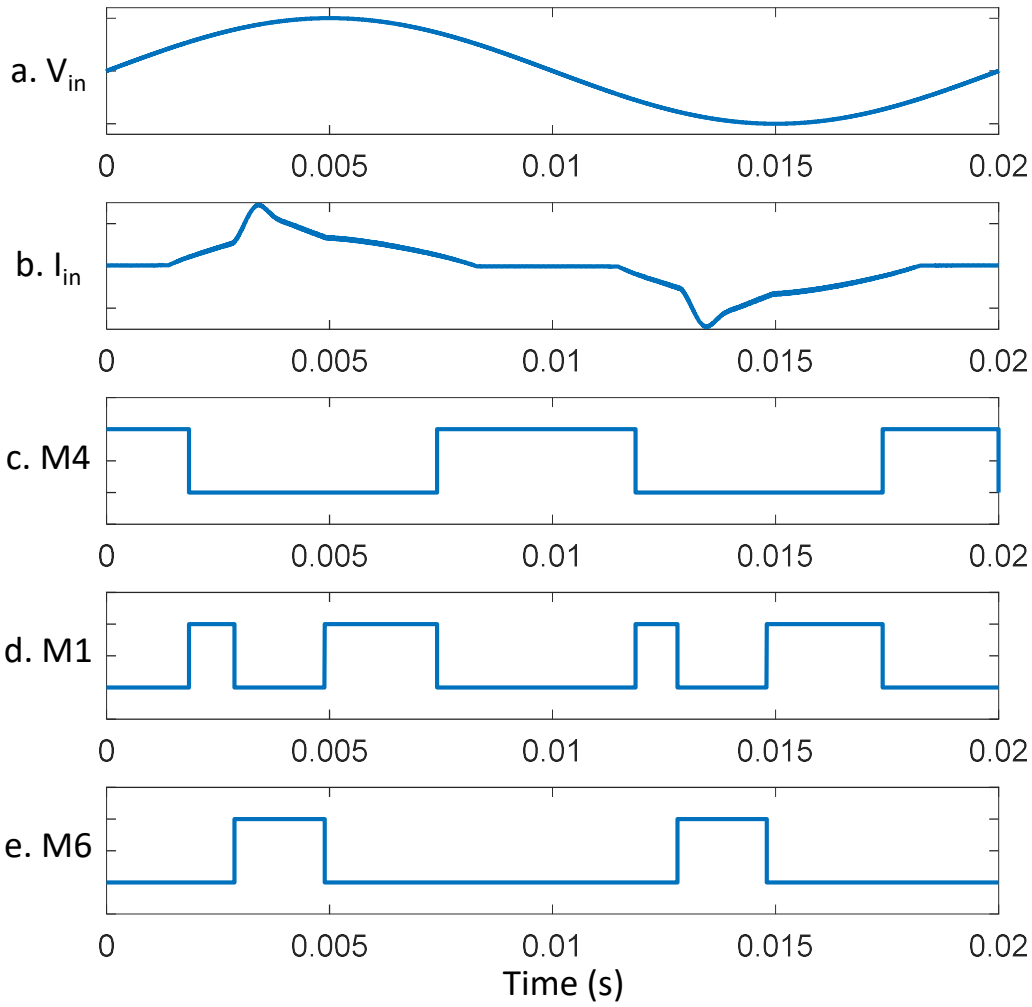


Figure 4.14: The modes of operation for circuit 2 with an AC input voltage (PF over-corrected).

4.6.3. The modes of operation for circuit 3 with an AC input voltage

The last simulation is done on the circuit 3. Similar to the simulation for circuit 1 and 2, the system is simulated under all of the PF conditions. For this circuit by using a 30 nF capacitor as C_{pfc} near unity power factor can be achieved.

The first simulation is for PF under-corrected. Similar to the previous simulations, the mode of operation for this condition is M1 for the complete duration of 1 grid cycle.

The second simulation is for the PF corrected condition. The detected modes of this condition are M1, M2 and M7. Figure 4.15 shows the detected modes of operation for this simulation.

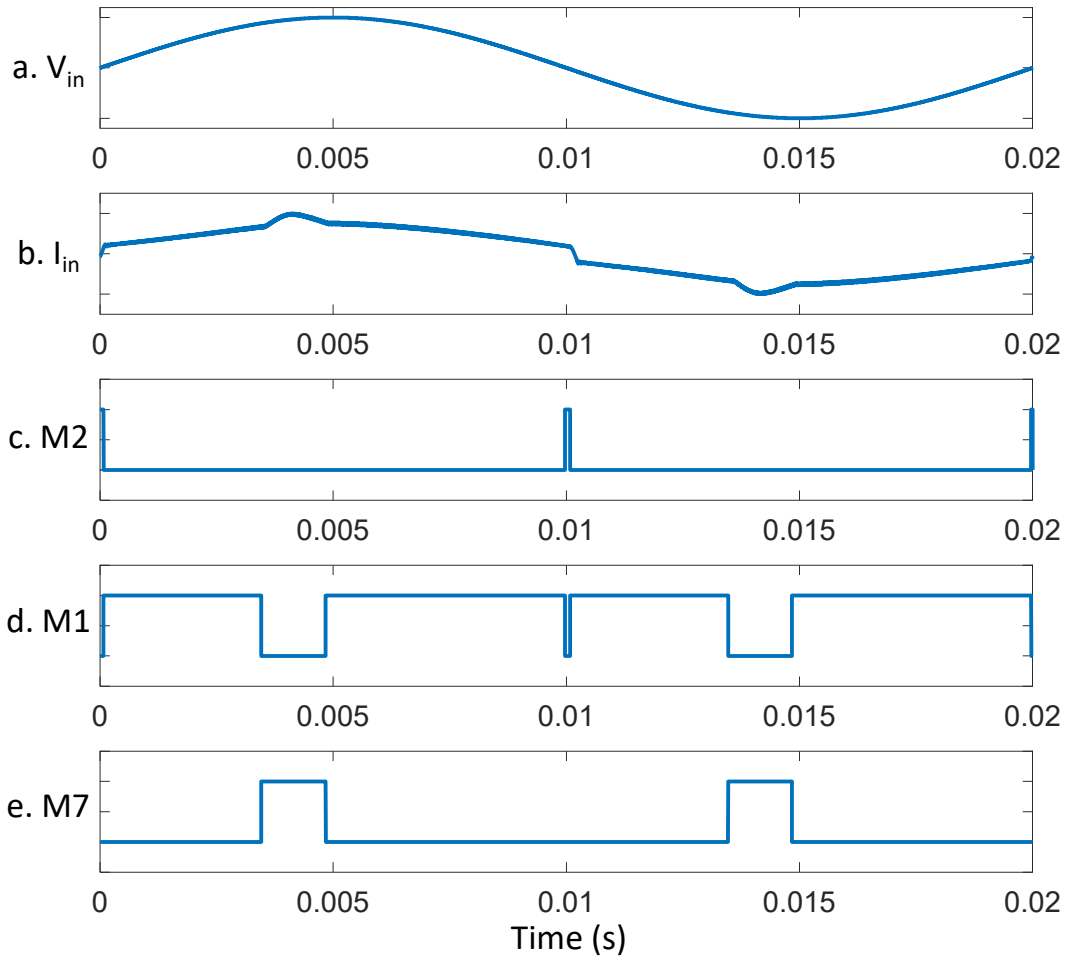


Figure 4.15: The modes of operation for circuit 3 with an AC input voltage (PF corrected).

The final simulation for the circuit 3 is PF over-corrected operation. For this simulation the C_{pfc} is 90 nF. The detected modes of operation for this simulation are M1, M4 and M8. Figure 4.16 shows the modes of operation, the input voltage and current for this simulation.

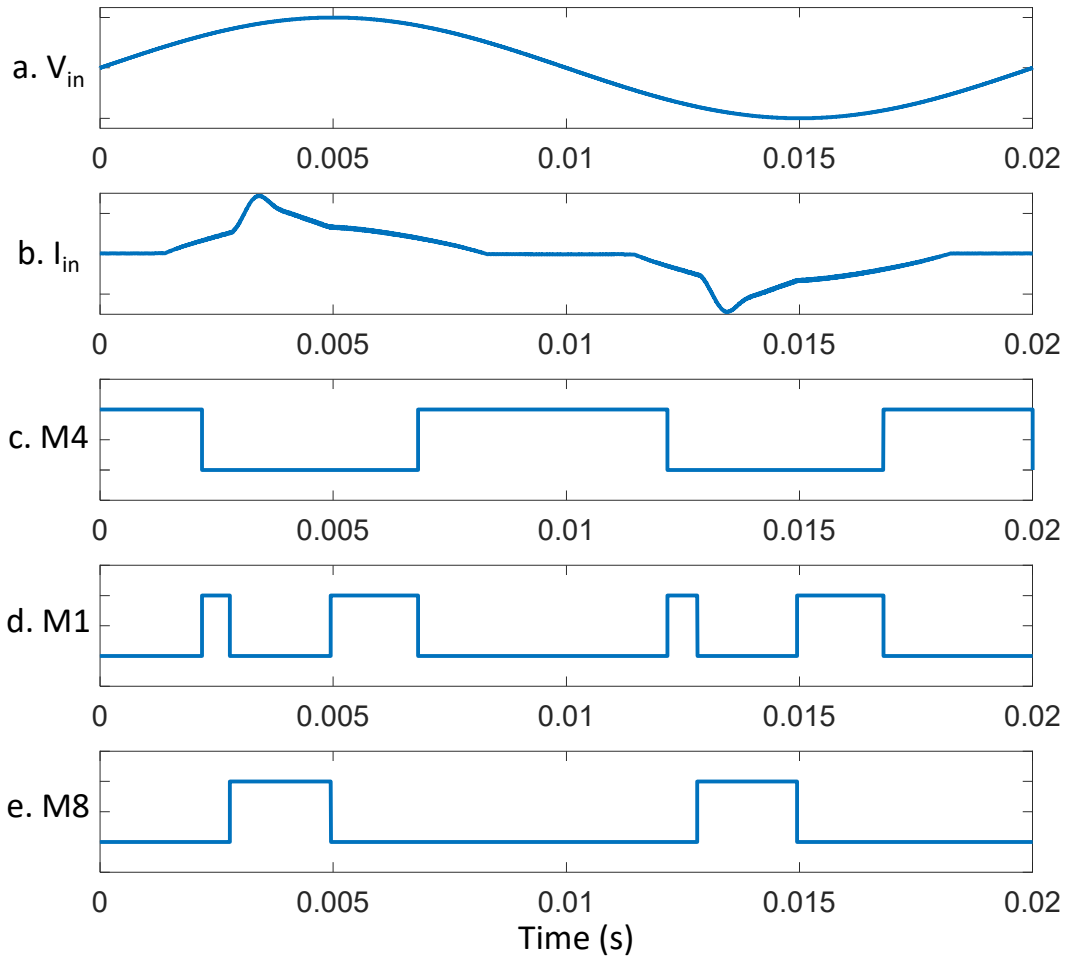


Figure 4.16: The modes of operation for circuit 3 with an AC input voltage (PF over-corrected).

4.8 Conclusion

In this chapter, the operation of the circuit has been investigated in detail. A novel procedure to extract the modes of operation of a power converter using simulation models and MATLAB has been demonstrated. Furthermore, the modes of operation of the system with different input voltages and under different conditions were investigated. As demonstrated, the modes of operation of the system with a DC input voltage is constant and does not change with variation in circuit parameters. On the other hand, the system with an AC input voltage exhibited 8 different modes of operation depending on circuit parameters and PF conditions. Moreover, there was no order for the modes of operation for the simulations with an AC input voltage. Therefore, it is not possible to predict the modes of operation of the system with different circuit parameters and without a predictable mode of operation for the system it is

not possible to mathematically model the system. Lastly, the randomness in the results of the modes of operation of the system with an AC input voltage, raised a suspicion about the simulation data. Therefore, it is essential to compare the simulation results with practical results. In the next chapter, the operation of the system will be investigated using experimental results and the modes of operation for the practical experiments will be extracted.

Chapter 5. Experimental platform for extraction of the modes of operation of CSCP-PFC systems.

5.1 Introduction

In previous chapter a detailed investigation of the modes of operation of the system under different conditions and with different circuit parameters has been demonstrated using LTspice simulation package. As several different modes of operation were detected, and there was no logical order for the occurrence of the modes of operation, it is necessary to identify the modes of operation of the system in practical experiments, to verify the simulation results and to further understand the behaviour of the circuit. For this set of experiments, the mode extraction software developed using MATLAB is used. However, as behavioural voltage sources only exist in simulation packages, there is a need for a novel technique to measure the conduction state of the switches and diodes and convert this into a digital signal to be used by the MATLAB mode extractor.

The design process for the CSCP-PFC circuit boards is first presented. The circuit boards are designed in a modular manner to both ease the fault findings and to allow a parametric sweep to be performance. Therefore, the resonant tank, the charge pump PFC and half bridge, the input rectifier and the LC filter self contained on separate Printed Circuit Boards (PCB). Subsequently, the process of converting the conduction state of each diode or switch to a digital signal is given. Following this, the functionality of each sub system is verified. Finally, the CSCP-PFC system is experimentally characterised and the modes of operated are extracted.

5.2 The design of the CSCP-PFC system

As mentioned earlier the system is designed in modular manner using several PCBs. Modular design has many advantages compared to a single board design. First it eases the fault finding and debugging of the system as PCB module can be tested and verified separately. Moreover, the modular design allows for an easy change of components. As in the simulations described in chapters 3 and 4, the parametric sweep facility had been used and since it is necessary to able to perform the similar measurements in practice a modular design allows for easy change of components. Figure 5.1 shows the complete circuit diagram of the system demonstrating the different modules of the system.

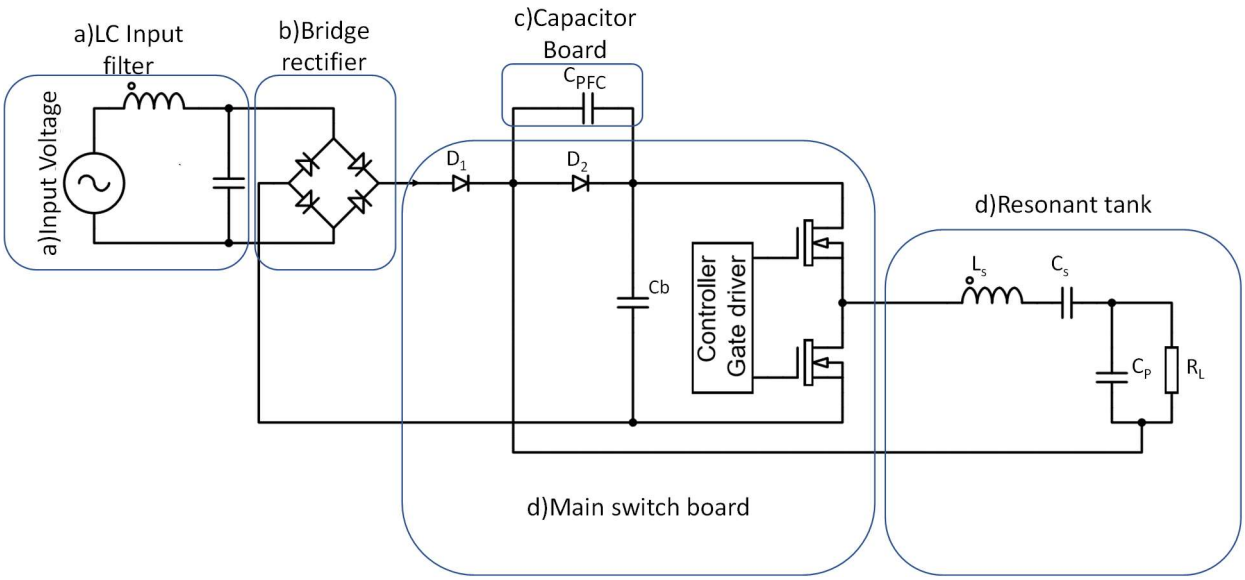


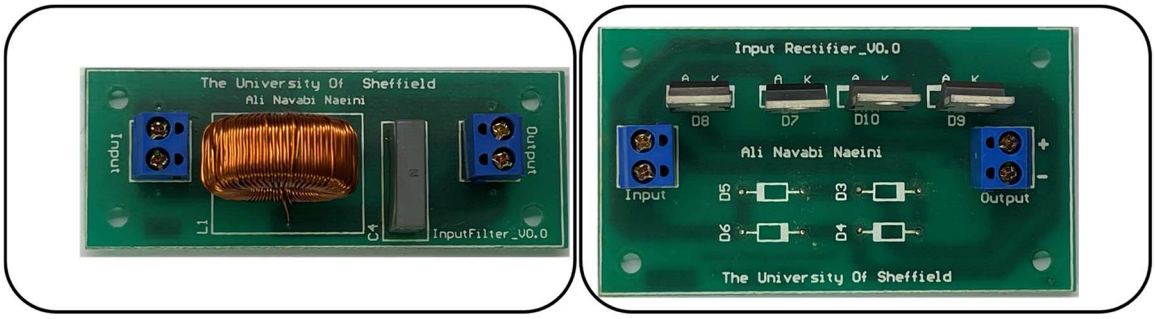
Figure 5.1: The diagram of the sytem setup demonstrating each module of the system.

Figure 5.1 demonstrates each module of the practical setup. The modules on figure 5.1 are connected together using block terminals. The description of the modules are as follows:

Module a) This module is an LC input filter; this section removes any high frequency signal that is present on the line current of the system. A more comprehensive description of operation of the LC filter is given in chapters 1 and 2. Figure 5.2a shows the assembled PCB of this module.

Module b) This module is a full wave voltage rectifier, and it rectifies the input sinusoidal voltage. Figure 5.2b shows the assembled PCB of this full wave rectifier.

Module c) This module is a capacitor board that contains 12 capacitors with Single Pole Single Throw (SPST) switches. The schematic diagram of the capacitor board is shown in figure 5.3. As shown in figure 5.3 there are 5 x 1 nF, 5 x 10 nF and 2 x 100 nF capacitors. By using two of these boards for C_{pfc}, it is possible to adjust the capacitance from 1 nF to 500 nF with steps of 1 nF. Using this board allows one to change the capacitor values to investigate the operation of the system with different values. Moreover, duplicates of this board are also used for capacitor C_p and C_s in the resonant tank. Lastly, the assembled PCB of the circuit board is shown in figure 5.4.



a b

Figure 5.2: a) Input LC filter, b) Full wave rectifier.

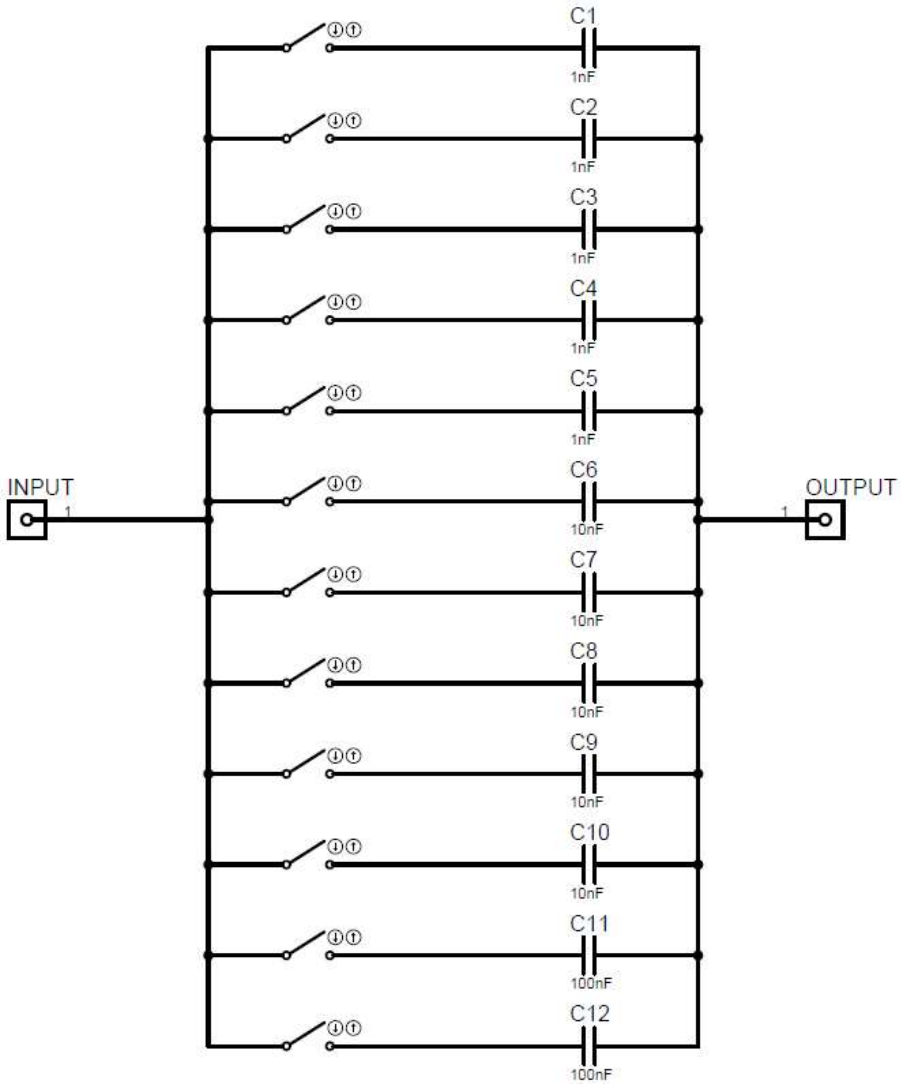


Figure 5.3: The schematic of the capacitor board circuit.

Figure 5.4: Assembled PCB of the Capacitor board

Module d) Main switch board. This section contains the charge pump diodes and the half bridge switches. As mentioned earlier the conduction state of the switches and diodes need to be measured in order to extract the modes of operation. Therefore, current sensing devices are needed to be implemented for each switch or diode. For this purpose, sense resistors are placed for each component. Moreover, in order to be able to measure both high value and low value currents, two sense resistors are implemented, 1 Ohm and 0.1 Ohm and they are switchable using Single Pole Double Throw (SPDT) switches. (The process of current measurements and processing of the signals is explained in detail in the next section). Lastly, in order to be able to change the capacitance of C_b and investigate its effect on the experiment results, 4 different switchable capacitors with values of 22 µF, 100 µF, 100 µF and 220 µF are used. Figure 5.5 shows the schematic of the main switch board.

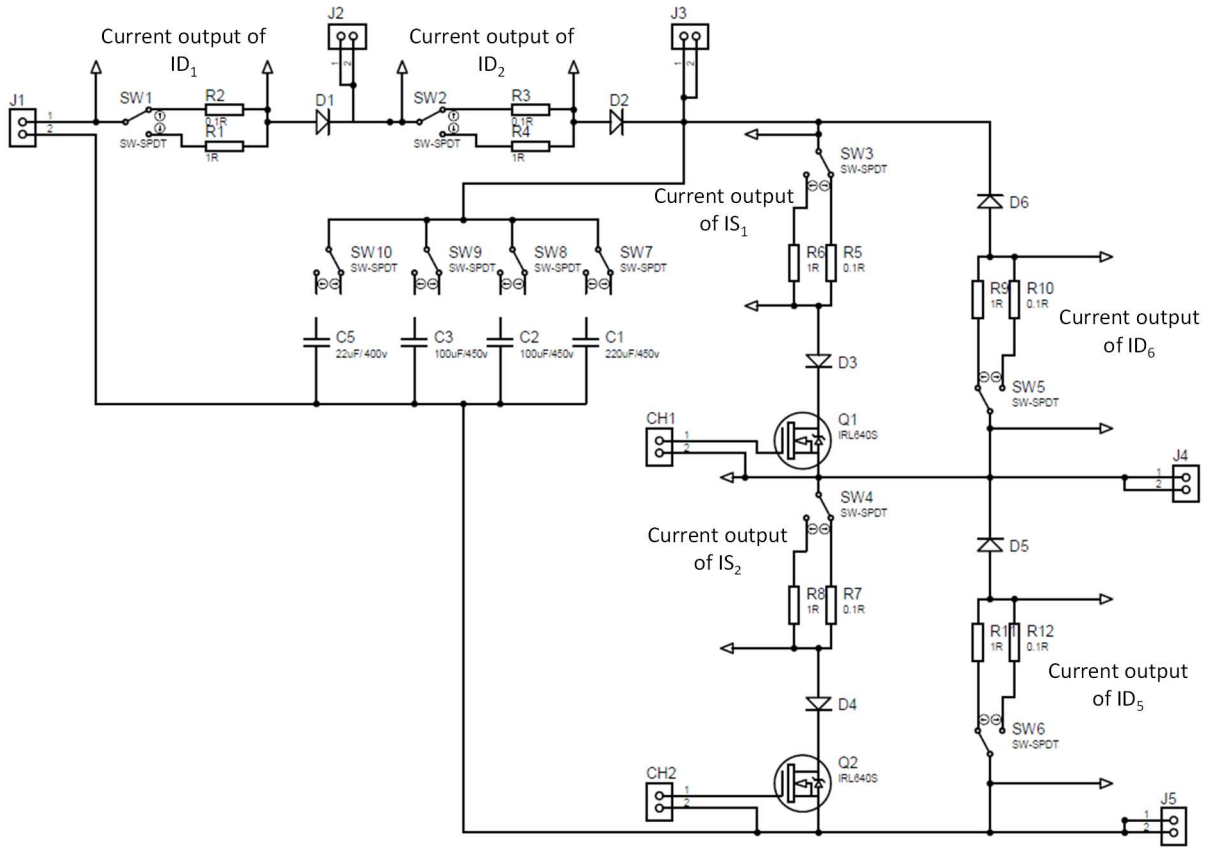


Figure 5.5: The schematic of the main switch board circuit.

In figure 5.5 the connector J1 is for input power, J2 and J3 are for C_{pfc} connection, J4 is for the resonant tank and J5 is the ground of the circuit. These connectors are all block terminals. To avoid ambiguities associated with the conduction of the MOSFET body diodes, additional diodes D3 and D4 are used to prevent bidirectional current flow through Q1 and Q2 respectively. Discrete diodes D5 and D6 are used in place of the body diodes in a similar manner to the SPICE simulation model described previously. Moreover, the connectors CH1 and CH2 are communication pin headers, and they are for the gate drive signals of MOSFETs Q1 and Q2. A number of voltage measurement nodes placed in the circuit diagram. For the current-measurement voltages, SMA connectors are used as the actual low-voltage

measurements are in range of millivolts and so noise can distort the signals. Lastly, the assembled PCB of the main switch board is shown in figure 5.6.

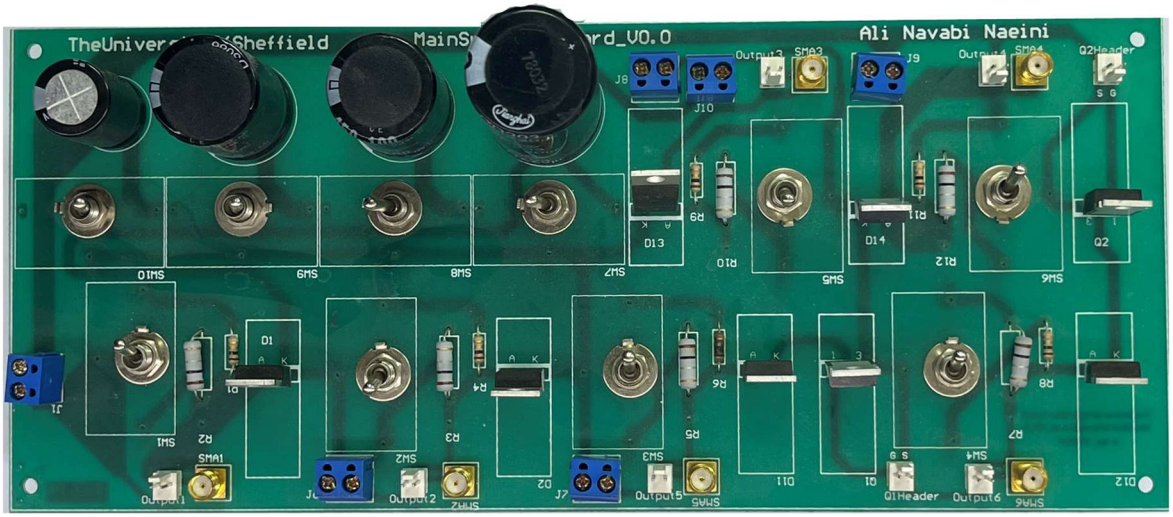


Figure 5.6: The assembled PCB of the main switch board

Module e) The resonant tank: As mentioned above for the capacitors C_s and C_p of the resonant tank, the same capacitor board as the module c is used. For the inductor L_s three different inductors have been designed and implemented using ferrite cores. The inductance of the inductors are 400 µH, 1 mH and 1.69 mH (These values are from tables 4.1 to 4.3 from chapter 4). The inductors and capacitor boards are connected together using wires. For the load, R_L, assorted 50 watt aluminium casing resistors are used.

There are two more boards for this experiment that are not included in figure 5.1. The first board is a gate driver. In order to properly turn on and off the MOSFETs Q1 and Q2, a gate driver IC is needed. For this purpose, the IR2110 IC is used which uses a charge pump bootstrap circuit to drive the high-side MOSFET.

The other board that is used for this experiment is a microcontroller development board. The function of this board is to generate the complementary PWM signals for the MOSFETs. The development board that is used for this project is TI LaunchXL F28379D microcontroller board by Texas Instruments. Another benefit of using this development boards is that, it allows users to graphical programming using Simulink or LabVIEW, which ease the change of parameters of the board for different types of tests and experiments. The signals from the development board are connected to the gate driver board in order to drive the MOSFETs. Figure 5.7 shows the development board connected to the gate driver circuit.

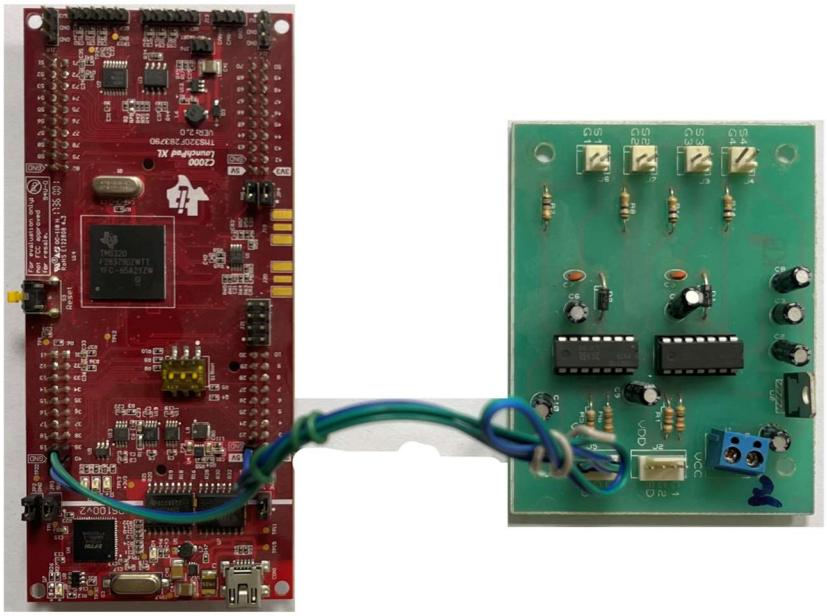


Figure 5.7: The gate driver and the microcontroller development board.

The full setup of the experiment containing all of the modules is shown in figure 5.8. In the next section the process measuring current data for each diode or switch and the process of converting the measured data to a digital data that represents the conduction state of each component is fully explained.

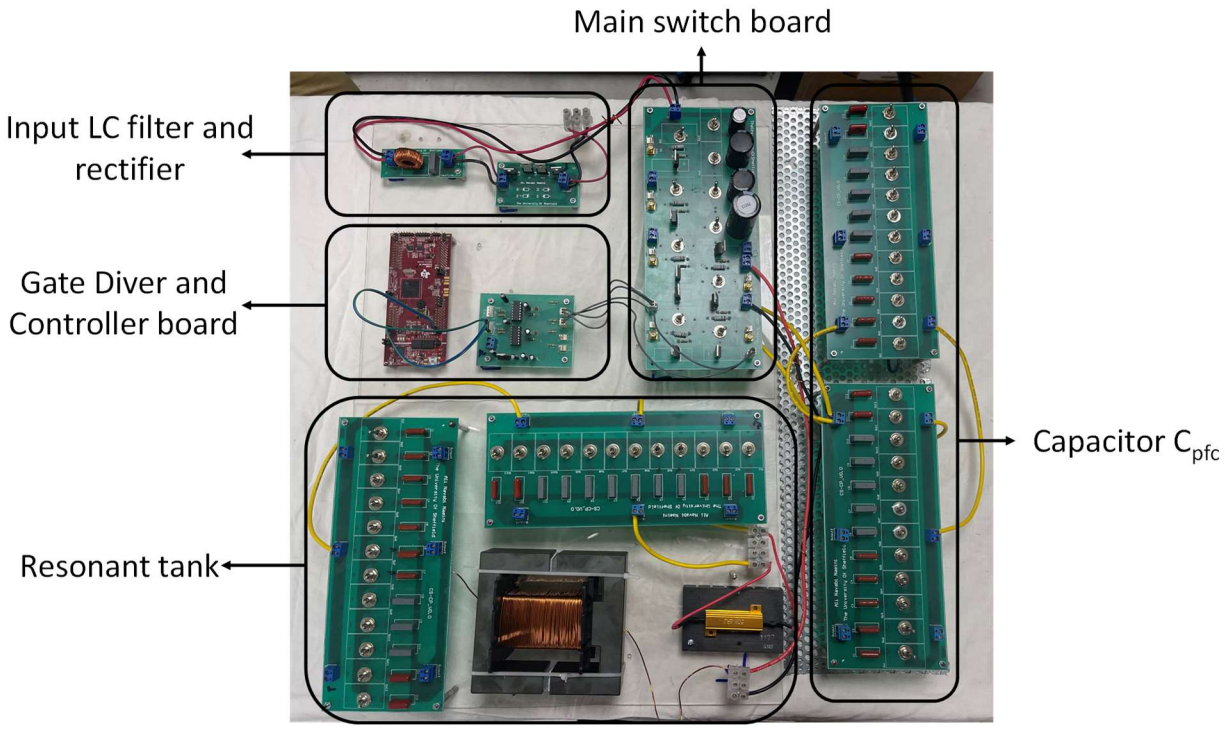


Figure 5.8: The experiment setup of the CSCP-PFC system.

5.3 Conduction state to digital signal converter

In order to convert the conduction state of the diodes and switches into a digital signal, two different techniques can be used. The first technique is based on current measurement of the component, as the current through the component is zero when it is turned off and higher or lower than zero when its conducting. For this technique several analogue circuits are needed. These circuits include differential amplifier, comparator circuit and a digital level shifter. These boards are explained in detail in the next section.

The second technique is based on voltage measurement. As the voltage across the switch or diode is near zero when it is conducting and has a value much greater than zero when it is not conducting, it is possible to use voltage measurements to generate a digital signal, representing the conduction state of the component.

The measurements were acquired using a Rigol MSO-5104 mixed signal oscilloscope which offers 16 digital channels with 4 analogue channels with sample rate of up to 8 Giga samples per second.

5.3.1 Current sense resistor component conduction measurement technique

For this technique the current through each diode or switch is measured using shunt sense resistors. Figure 5.9 is the simplified circuit diagram of the main switch board given in figure 5.5 and it shows the placement of sense resistors for each switch or diode and the signals of interest.

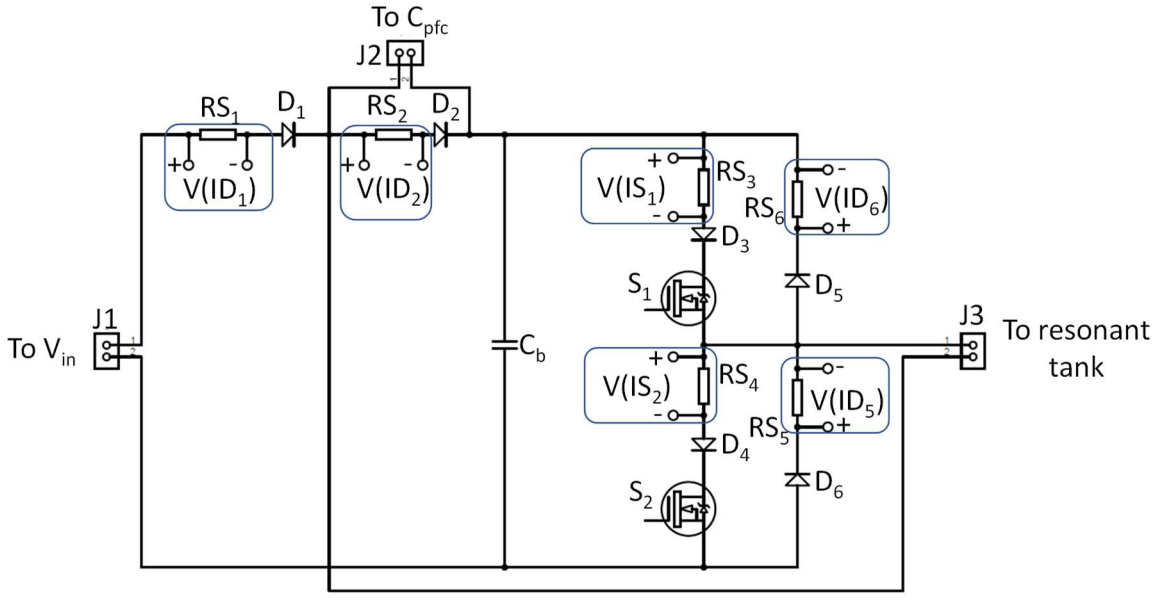


Figure 5.9: The system configuration with sense resistors.

In figure 5.9 the input voltage, resonant tank and C_{pfc} are not included, and they can be connected to the system using connectors J1, J2 and J3. As shown in figure 5.9, each MOSFET or diode has an associated series connected current sense resistor (RS_1 to RS_6). Based on the Ohm's law, the voltage across the sense resistors is proportional to the current that flows through it and this allows the measure of current through an series connected component. Using this setup, the current of each switch or diode can be measured. However, in order to measure current of each component the voltage across the sense resistor has to be measured and, unfortunately, many of these measurements cannot be made with respect to common ground or reference point. For better understanding (5.1) and (5.2) show the mathematical expression of the nodes $V(ID_1)_+$ and $V(ID_1)_-$ respectively (The voltage nodes are from figure 5.9).

$$V(ID_1)_+ = \begin{cases} V_{in} & D_1\ Not\ conducting \\ V_{in} + (RS_1 \times ID_1) & D_1\ Conducting \end{cases} \quad (5.1)$$

$$V(ID_1)_- = \begin{cases} V_{in} & D_1\ Not\ conducting \\ V_{in} & D_1\ Conducting \end{cases} \quad (5.2)$$

As demonstrated in (5.1) and (5.2) the current through diode D_1 is the voltage difference between $V(ID_1)+$ and $V(ID_1)-$ nodes divided by the value of the sense resistor. (5.3) shows the potential difference between the two nodes.

$$(V(ID_1)_+) - (V(ID_1)_-) = \begin{cases} 0 & D_1\ Not\ conducting \\ (RS_1 \times ID_1) & D_1\ Conducting \end{cases} \quad (5.3)$$

As shown in (5.3) the potential difference between $V(ID_1)+$ and $V(ID_1)-$ is proportional to the ID_1. Therefore, in order to measure the current for each switch and diode the voltage at the positive side of sense resistor has to be measured with respect to the negative side of that sense resistor. This scenario applies for all the diodes and switches. Due to this issue, conventional methods of measurement using oscilloscopes and passive probes are not possible as the grounds of the channels of the oscilloscope are connected together since connecting voltage measurement probes direct across sense resistors causes a short circuit at various locations of the circuit and can cause a damage to the circuit and oscilloscope [1].

Differential Amplifier

To address this issue the six signals from the sense resistors RS_1 to RS_6 has to be modified to have a common ground for further processing. For this task a circuit called differential amplifier can be used. Differential amplifiers use operational amplifiers (OP-AMPs) and have two inputs, and they only amplify the difference between the two inputs. Any common signal

that is present on both inputs is completely eliminated. Figure 5.10 shows the circuit diagram of a differential amplifier [33] [2].

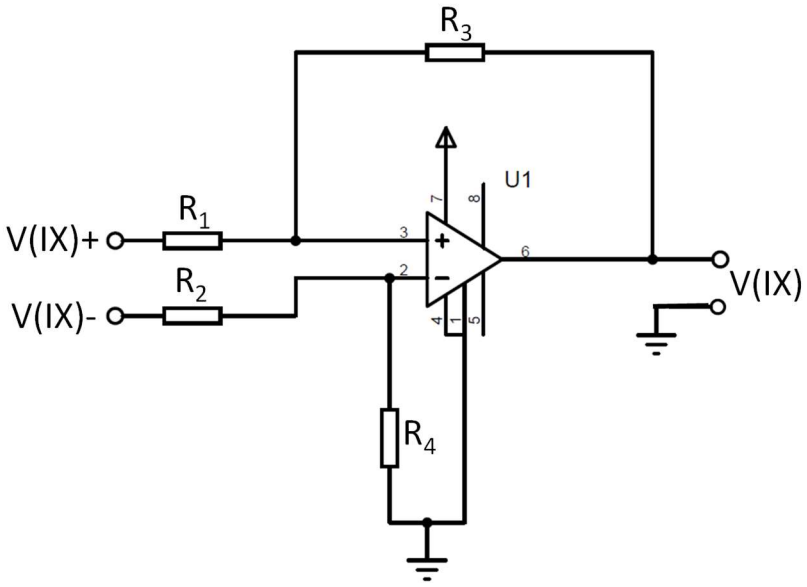


Figure 5.10: Differential amplifier circuit.

In figure 5.10 the circuit has two inputs V(IX)+ and V(IX)- (X represents the input signal and it can be changed to any of the current measurement signals from figure 5.9). The circuit has one output V(IX). Finally, the relationship between input and output of the differential amplifier is given by (5.4)[2].

$$V(IX) = \left((V(ID_1)_+) \left(\frac{R_4}{R_2 + R_4} \right) \left(\frac{R_1 + R_3}{R_1} \right) \right) - \left((V(ID_1)_-) \left(\frac{R_3}{R_1} \right) \right) \tag{5.4}$$

As shown in (5.4) any common signal that is present on both input is eliminated and the difference between the input signals is amplified [2]. Lastly, if $R_1 = R_2$ and $R_3 = R_4$ in figure 5.10, then (5.4) can be simplified to,

$$V(IX) = \left(\frac{R_3}{R_1} \right) \left((V(ID_1)_+) - (V(ID_1)_-) \right) \tag{5.5}$$

For this experiment it is preferred to have a differential amplifier with an adjustable gain to be able to tune the amplifier to get the best possible results. Therefore, the differential amplifier circuit was designed to have an adjustable gain by using DIP switches to change the resistor values. The schematic diagram of the differential amplifier that is used for the practical tests is shown in figure 5.11.

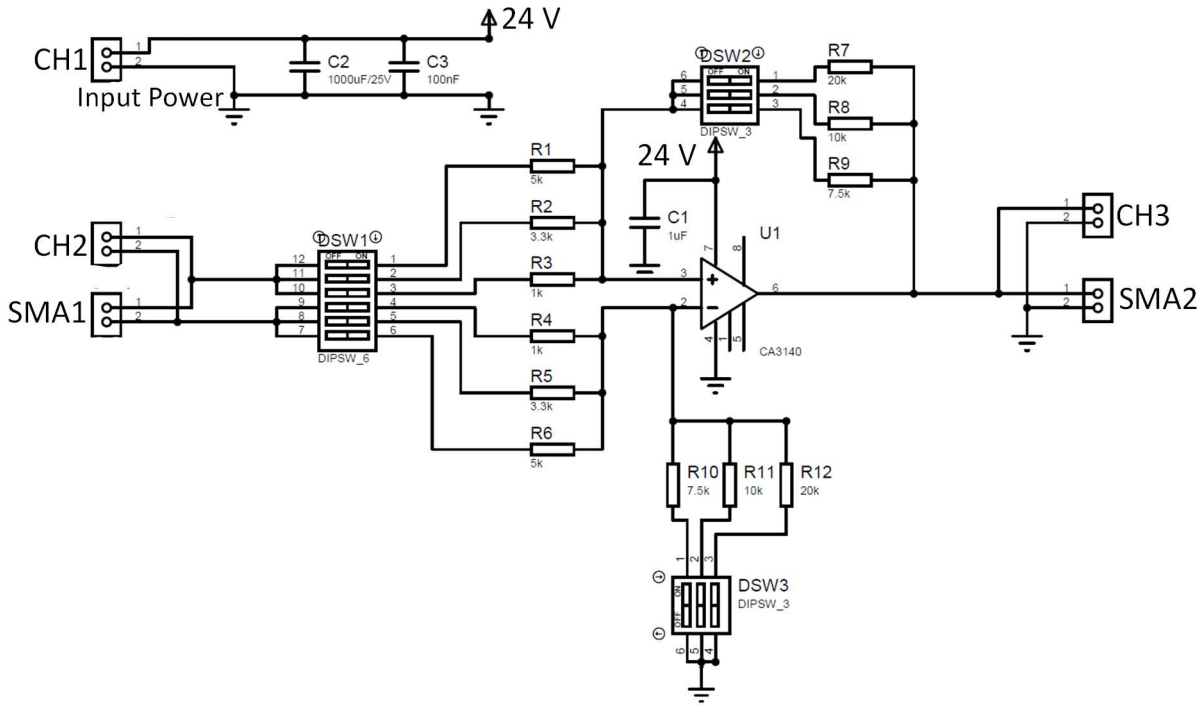


Figure 5.11: The circuit schematic of the differential amplifier used for this experiment.

As demonstrated in figure 5.11 the OP-AMP used for this circuit is CA3140. Moreover, connectors CH1, CH2 and CH3 are communication pin headers. CH1 is used for the input power that is 24 volts. Connectors CH2 and CH3 are for the input and output signals along with SMA1 and SMA2. Furthermore, capacitors C1, C2 and C3 are decoupling capacitors to remove any high or low frequency noise and ripple that is present on the supply voltage . Lastly, the gain of the amplifier can be adjusted by using the DIP switches SW1, SW2 and SW3 to switch between different resistors. The assembled printed circuit board of figure 5.11 is shown in figure 5.12.

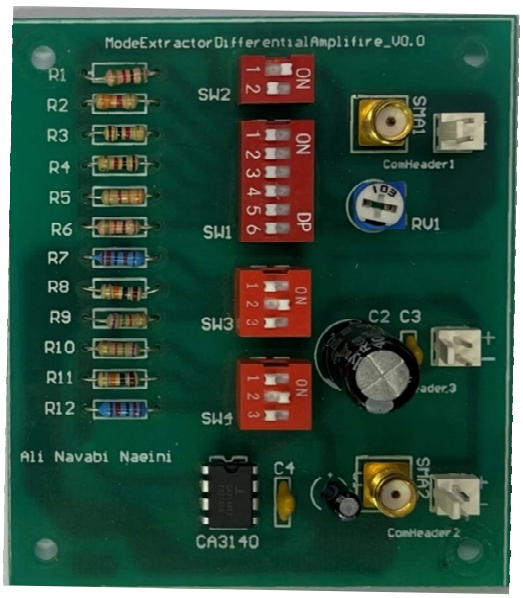


Figure 5.12: The assembled PCB of the differential amplifier.

Comparator Circuit

In the next stage the current signals from the differential amplifier need to be converted to Boolean representation of conduction states for each diode or switch, with an output of 1, if the current is flowing through the component, and an output of 0 for when the current is zero. For this purpose, comparator circuits can be used. Comparator circuits compare two analogue inputs and outputs either 1 or 0 to indicate which input is larger [35] [4]. Figure 5.13 demonstrates the simplified schematic of the comparator circuit that is used in the experiment.

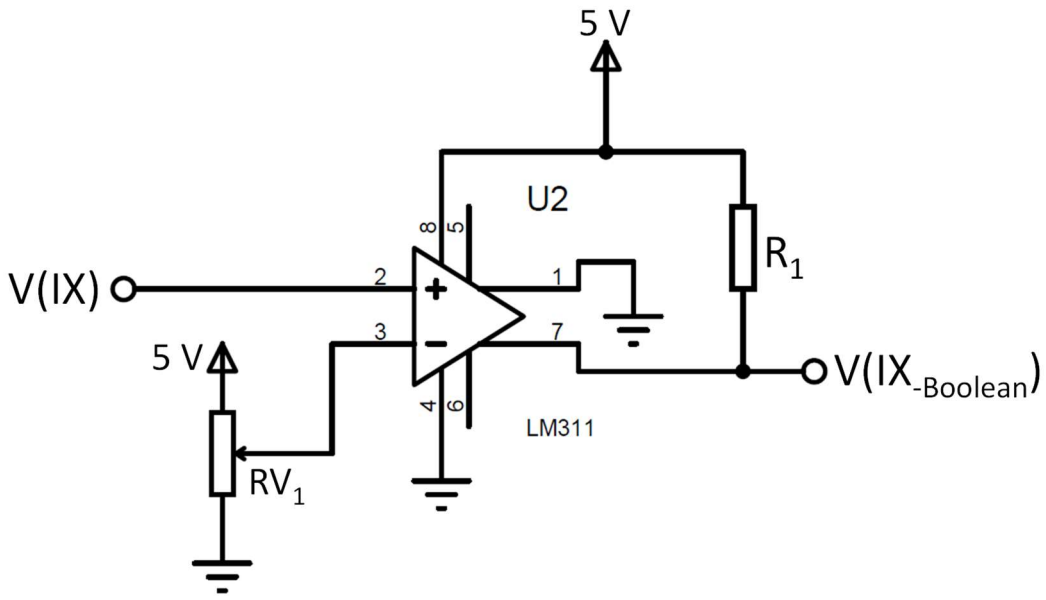


Figure 5.13: The circuit diagram of the comparator circuit.

In figure 5.13 the comparator used is LM311. The supply voltage to the circuit is 5 volts. The positive side input of the system is the V(IX) signal from the differential amplifier and the negative input is a constant voltage that can be adjusted by the potentiometer RV_1. The operation of this circuit is that if the V(IX) input is higher than the negative side input the circuit outputs 1 and if the V(IX) input is lower than the negative side input it outputs 0. The use of RV_1 allows the threshold level to be adjusted. Therefore, the comparator circuit for each diode or switch can be adjusted to output 1 when the associated component is conducting and output 0 when it is not conducting. Figure 5.14 shows the detailed schematic of the comparator circuit.

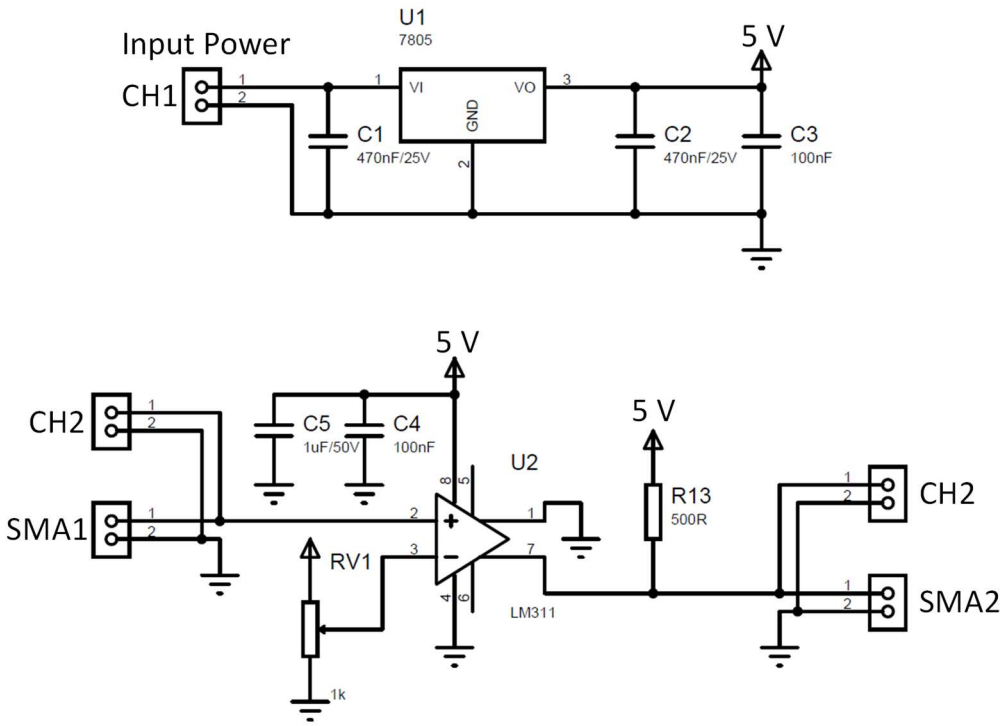


Figure 5.14: Detailed schematic of the comparator circuit.

As shown in figure 5.14 the input power is connected to a linear voltage regulator (LM7805) to provide 5 volts supply voltage for the circuit. Capacitors C1 to C4 are decoupling capacitors to remove any noise or ripple present on the supply voltage. Moreover, the input and output connectors are CH1, CH2, SMA1 and SMA2 with the same configuration as the amplifier circuit in previous section. Lastly, a picture of the assembled printed circuit board of the comparator circuit that consists of 4 comparators is shown in figure 5.15.

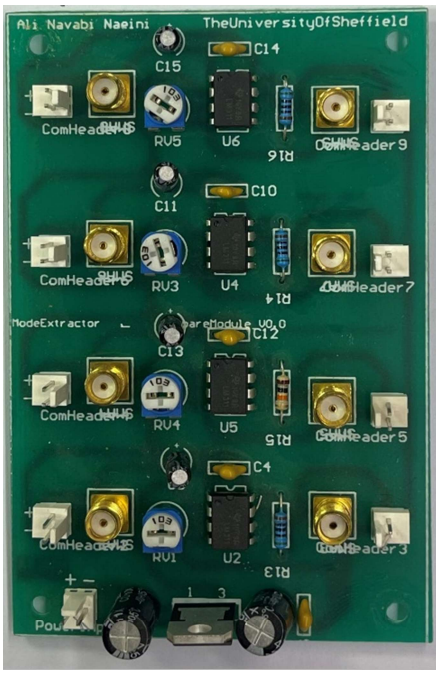


Figure 5.15: The assembled PCB of the comparator circuit.

Digital Level Shifter

In the last stage the digital signals from the comparator circuit go through two Schmitt trigger NOT gates, Figure 5.16. The purpose of this stage is to first convert the signals to a measurable value for the logic analyser of the oscilloscope and to remove any unwanted noise that are present on the signals [35] [5].

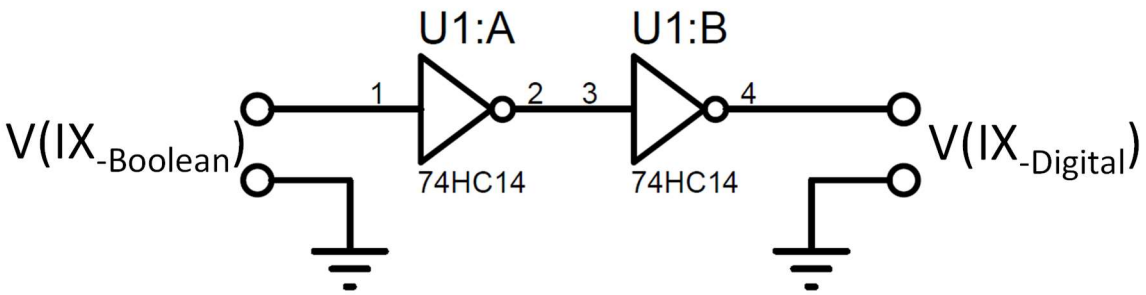


Figure 5.16: The circuit diagram of the digital level shifter circuit.

In figure 5.16 the digital IC used is the 74HC14. The input signal to this circuit is $V(IX_{-Boolean})$ and the output is $V(IX_{-Digital})$. After this stage the output signal can be analysed using the logic analyser of the oscilloscope. Lastly, a picture of the assembled printed circuit board of the digital level shifter circuit that consists of 12 not gates is shown in figure 5.17.

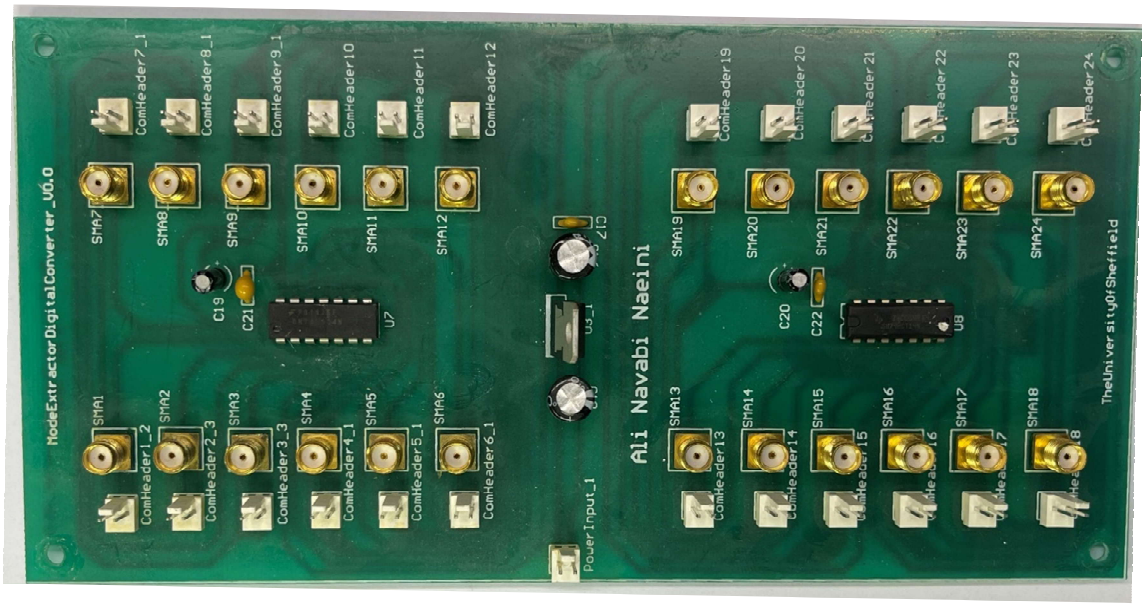


Figure 5.17: The assembled PCB of the digital level shifter circuit.

The digital signals ($V(IX)_{-Digital}$) represent the conduction state of each diode or switch in the system. These digital signals are similar to the digital signals that were produced by behavioural voltage sources used in the LTSPICE simulation circuit described in chapter 4. The experimental platform was designed to be a similar as possible to the simulation platform so that it is possible to easily use the output from the logic analyser/oscilloscope with the MATLAB mode extractor software that has been demonstrated in chapter 4. Figure 5.18 shows the setup of the circuits described above for the conduction state data conversion.

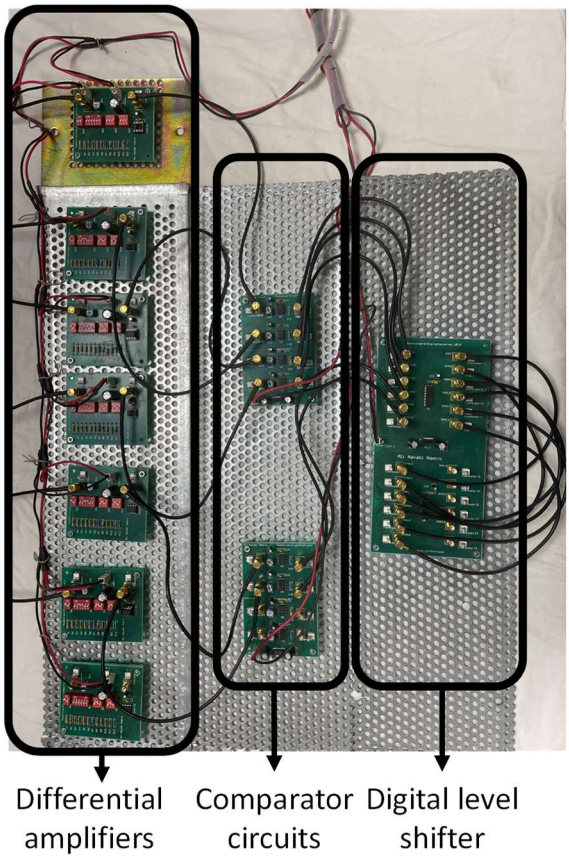


Figure 5.18: The experimental setup of conduction state to digital signal converter using current measurement technique.

5.3.2 Voltage based component conduction measurement technique

In this technique the voltage across each component is used to generate the digital conduction state data. This technique does not require any additional analogue circuits for signal processing and conversion. However, new data processing functions are required by MATLAB mode extraction software. As discussed earlier for each diode or switch, the voltage across it is (almost) zero when it is conducting and non-zero value when it is not conducting. Therefore, it is possible to obtain the conduction state data for each component based on voltage measurement. The circuit that is used for this experiment is slightly different to the circuit of figure 5.8. For this measurement all the sense resistors are removed. Moreover,

diodes D_3 to D_6 are also removed and a MOSFET with its body diode is used. The circuit diagram for this experiment is shown in figure 5.19.

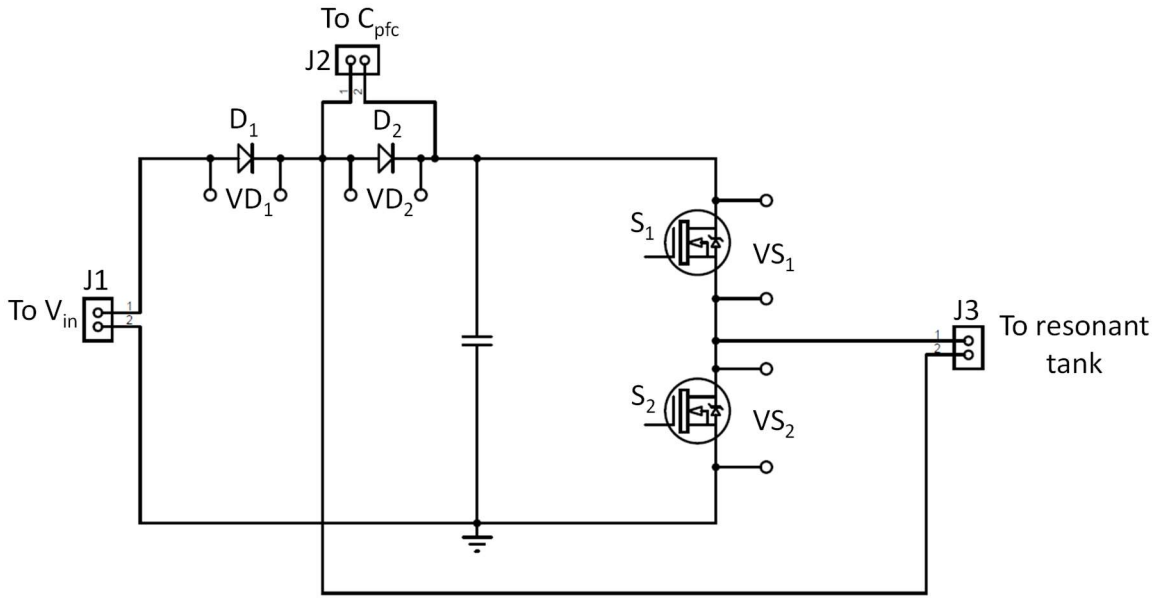


Figure 5.19: The setup of the system for voltage measurement technique, identifying the signals of interest.

Figure 5.19 demonstrates the voltage nodes that are measured. There are only 4 measurements as the oscilloscope is 4 channels. However, the measurements are not with respect to circuit ground and the voltage across each component needs to be measured. Therefore, differential probes are needed for this measurement [6]. Moreover, two more signals are measured using the logic analyser of oscilloscope. The two signals are the gate control data from the microcontroller development board for MOSFETs S_1 and S_2 (VG_1 and VG_2).

The measured data are then imported into MATLAB using CSV files to be converted into digital conduction state data.

For the conduction status of D_1 and D_2, the absolute value of VD_1 and VD_2 are compared to a threshold value. If the data is less than the threshold the diode is conducting and the software outputs 1 for that data point. In contrast, if the diode voltage is higher than the threshold, then the diode is not conducting and the software outputs 0 for that data point. (Based on the placement of the differential probes the voltage across the diode or switch can be positive or negative when the component is not conducting). Figure 5.20 demonstrates the flowchart for conversion of the voltage signals to digital conduction state data for diodes D_1 and D_2.

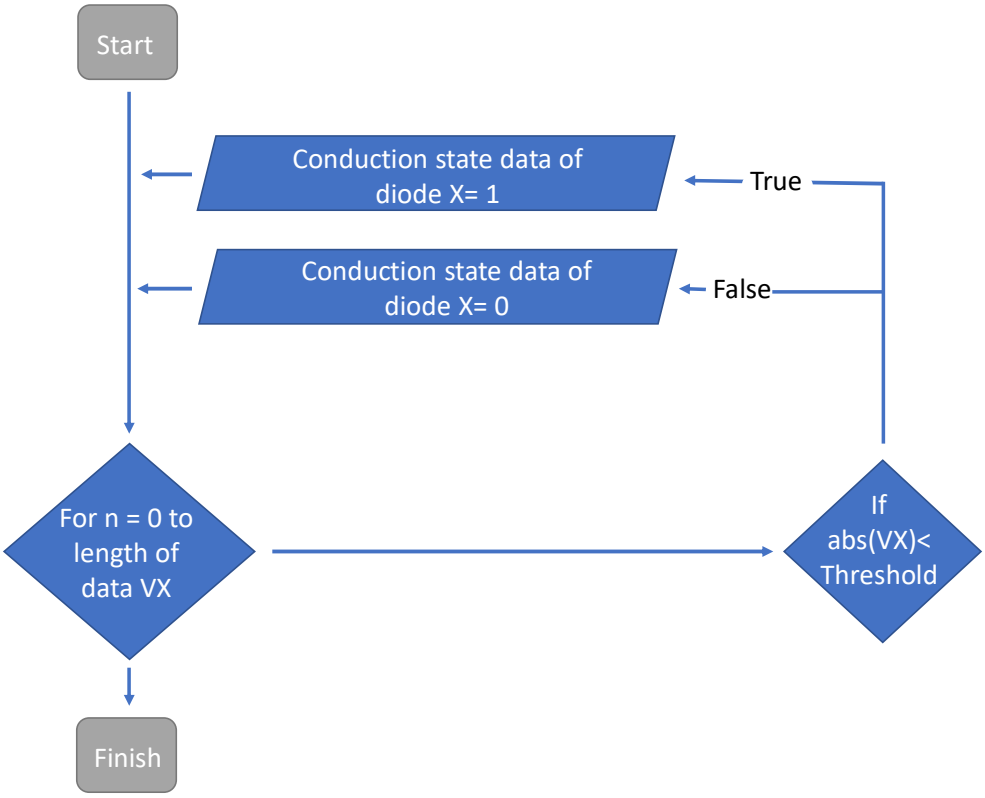


Figure 5.20: Flowchart for conduction state to digital signal converter of the diodes D_1 and D_2.

In figure 5.20 the X represents either D_1 or D_2. Moreover, the reason for using a threshold value is that in practical measurements the voltage across diodes when they are conducting is not absolute zero and it is the forward voltage drop of the diode(V_f). Therefore, an adjustable threshold is needed for the data conversion. For this experiment the threshold value is set at 0.5 as the diodes used in this practical platform are schottky diodes with low forward voltage drop.

The conduction state data conversion for the MOSFETs and their associated body diodes is more complex, as there is only one set of data for two components. For this conversion first the data goes through the same process as data conversion for diodes D_1 and D_2. Then this data is compared with the gate control signal, VGX. If the gate control signal is 1 and the conduction state data of the switch is 1, it shows that the MOSFET is conducting. On the other hand, if the gate control signal is 0 and the conduction state data is 1, it shows that the body diode of the MOSFET is conducting. Figure 5.21 demonstrates the flowchart for conduction state data conversion of the MOSFETs and their associated body diode.

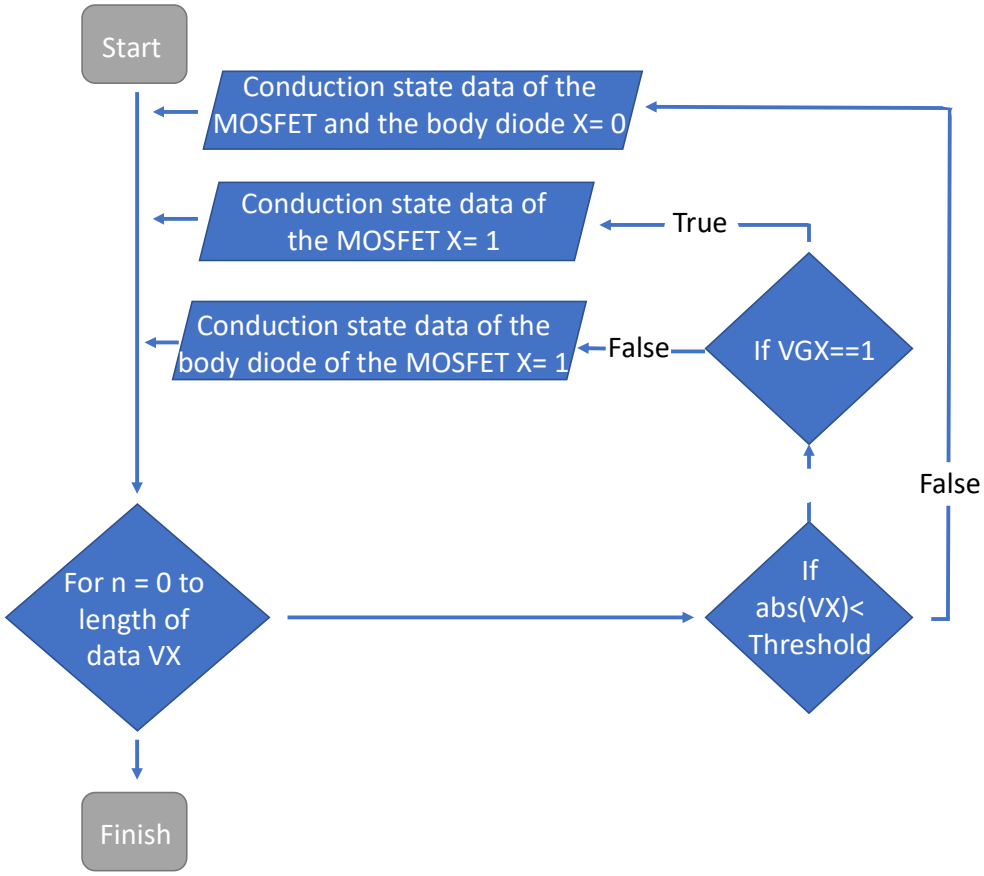


Figure 5.21: Flowchart for conduction state to digital signal converter of the MOSFETs and their associated body diodes.

This MATLAB software generate 6 sets of conduction state data for the diodes and the MOSFETs. The data can then be imported to the MATLAB code from chapter 4 to extract the modes of operation. For the practical modes of operation extraction both techniques of voltage measurement and current measurement are used to verify the results.

5.4 Verification of the experimental setup

As discussed earlier the system has been designed in a modular manner. One of the advantages of the modular design is that it allows to verify the operation of each part of the system individually before connecting them all together for the test setup. This section explains the verification procedure for each part of the system.

5.4.1 Verification process of the resonant tank

The first module of the system that is tested are the three resonant tanks (the values for the resonant tanks are given in tables 4.1 to 4.3 in chapter 4). For verification of the resonant tanks, the tanks are connected to a half bridge switches to form a simple LCC converter. Figure 5.22 shows the configuration of the test setup.

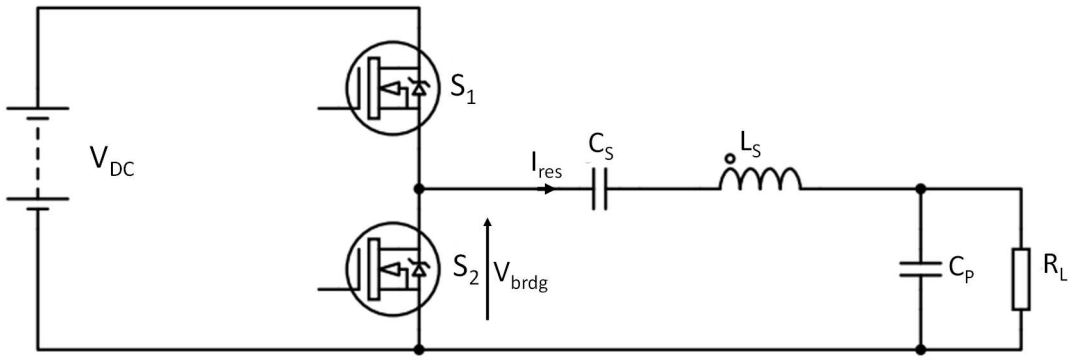


Figure 5.22: Test setup for verification of the resonant tanks.

The process of this test is to test each resonant tank with 3 different values of R_L (15, 39 and 68 Ohms) with different switching frequencies. For each tank there are 5 switching frequencies, from 20 kHz below to 20 kHz above resonant frequency with increments of 10 kHz. The value of resonant current for each test is recorded and then compared to simulation results of the same test. In total there are 45 tests. Each 5 results from a resonant tank with a specific load resistor are plotted on a single figure. The figures represent resonant current versos switching frequency. Therefore, there are 9 sets of figures demonstrating this verification. The figure for the resonant tank 1 (from table 4.1) with a load resistor 39 Ohms is demonstrated in figure 5.23 and the remaining results are illustrated in appendix 4.

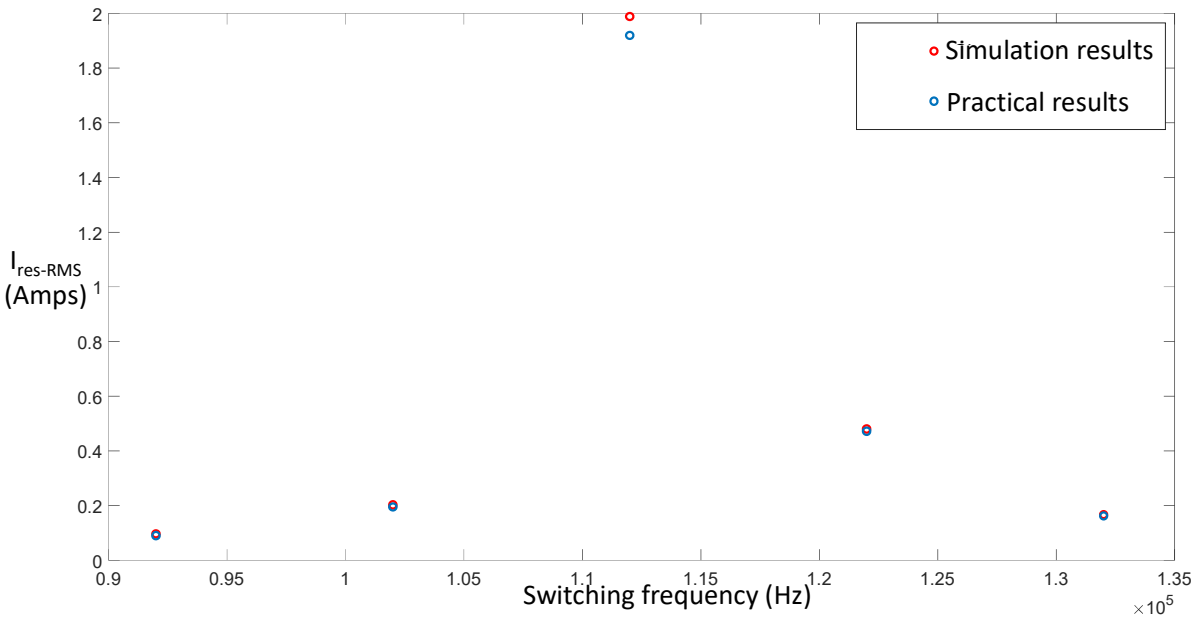


Figure 5.23: The verification results of resonant tank 1 with R_L of 39 Ohms.

As demonstrated in figure 5.23, the simulation and practical results confirm the correct operation of the resonant tank and the results are very close together.

5.4.2 Verification of the main switching board and the gate driver

After verification of the operation of the resonant tanks, the main switch board and the gate driver section have to be tested. For this test the main switch board is connected to the resonant tank but in configuration of an LCC converter without the charge pump PFC. Figure 5.24 shows the circuit configuration for this experiment.

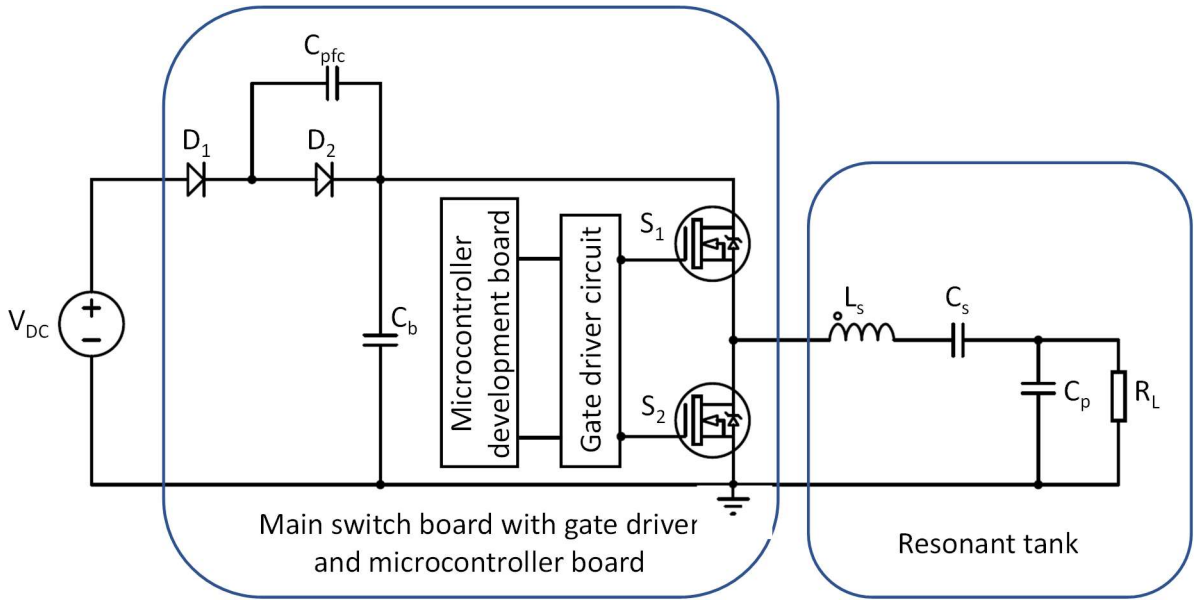


Figure 5.24: Test setup for verification of main switch board, gate driver circuit and microcontroller development board.

In figure 5.24 the simplified schematic of the main switch board is connected to the resonant tank as an LCC converter. The charge pump is present on the circuit; however, it does not operate as the negative side of the resonant tank is connected to the ground of the circuit instead of the voltage node between the diodes D_1 and D_2. Moreover, the gate driver and microcontroller development boards are connected to control the MOSFETs S_1 and S_2. For this experiment a DC voltage source is connected to the main switch board and the value of the resonant current and the phase shift between the bridge voltage, V_{brdg} and the resonant current (the phase shift has been introduced as angle α in the chapter 3) are recorded. The same as the experiment for verification of the resonant tank, the result of this experiment is compared to the LTspice simulation results. The simulation and practical results of this verification process are shown in figure 5.25.

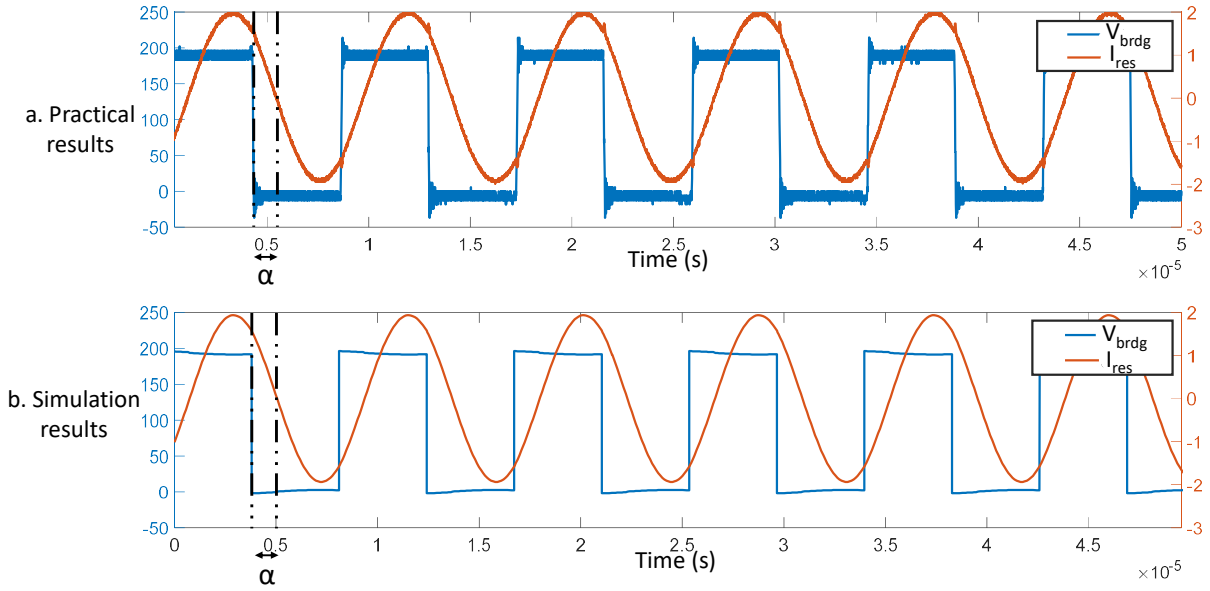


Figure 5.25: The verification results of main switch board.

As illustrated in figure 5.25 the amplitude of the resonant current and the bridge voltage from the simulation results and the practical results are very close together. Moreover, the phase shift angle α in simulation and practical results are almost identical. This set of results confirm the operation of the main switch board.

Having verified the operation of the modules of the CSCP-PFC system, it is now necessary to verify the operation of the conduction state to digital converter circuits. For this task first the operation of the differential amplifier, comparator circuit and the digital level shifter are tested individually and then the complete system is tested.

5.4.3 Verification of the differential amplifier

To test the operation of the differential amplifier circuit, it needs to be connected to the main switch board to receive current measurements input data. Therefore, the modules are connected to form the CSCP-PFC system with a DC input voltage. As the system is operating there are current waveforms for each component. For the verification the current measurement of diode D_1 is used ($V(ID)_+$ and $V(ID)_-$). Figure 5.26 shows the waveforms for resonant current (I_{res}), D_1 current (ID_1) and the output data of the differential amplifier($V(ID_1)$).

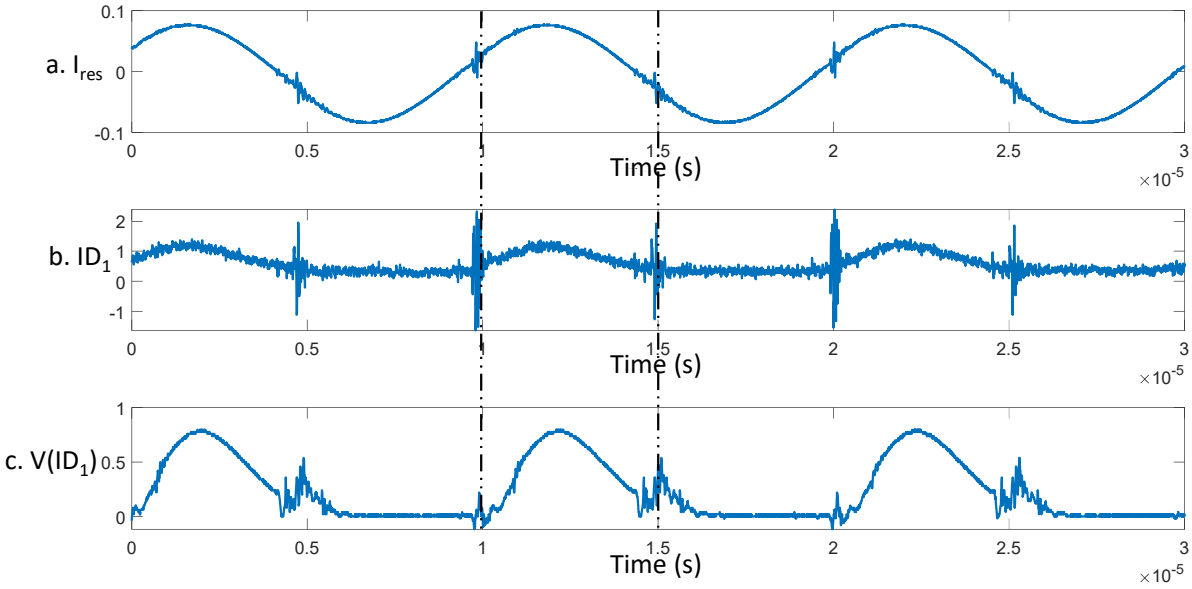


Figure 5.26: The waveforms of I_{res}, ID_1 and $V(ID_1)$ versus time.

As demonstrated in figure 5.26 the voltage waveform of the output of the differential amplifier is the same as current waveforms of the diode D_1. Moreover, the differential amplifier has removed most of the noise that is present on the current waveform. Lastly, as shown the $V(ID_1)$ is with respect to ground and it is zero when the diode is not conducting.

5.4.4 Verification of the comparator circuit

In order to verify the operation of the comparator circuit, the input of the circuit is connected to the output of the differential amplifier. For the circuit to operate correctly it needs to output high or low depending on the conduction state of diode D_1. Figure 5.27 shows the current waveform of diode D_1 (ID_1) the input and output of the comparator circuit $V(ID_1)$ and $V(ID_{1\text{-Boolean}})$ respectively.

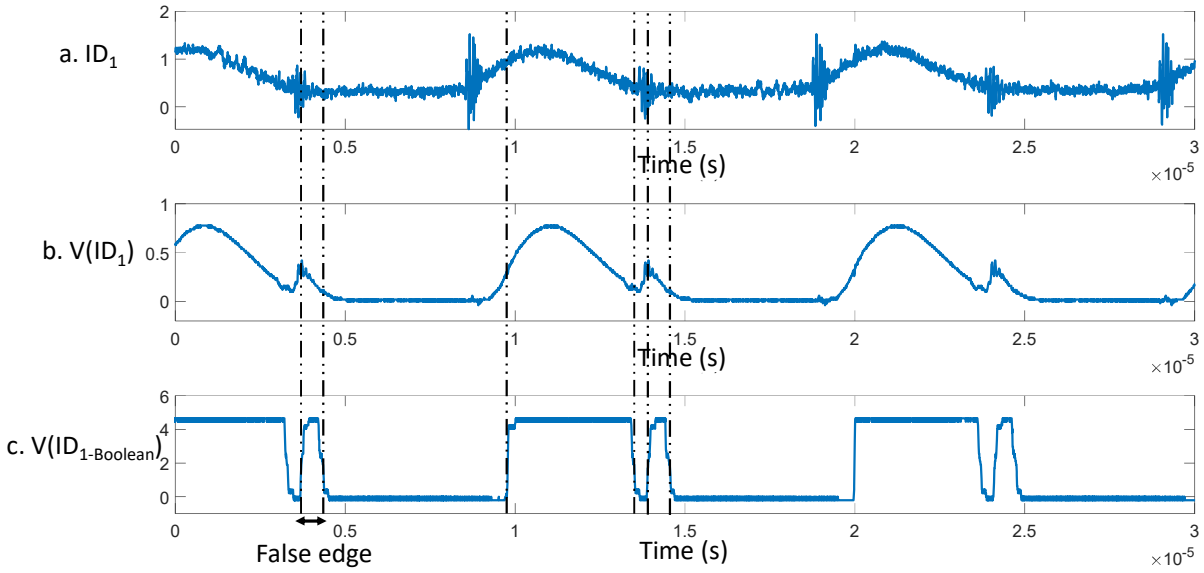


Figure 5.27: The waveforms of ID_1, $V(ID_1)$ and $V(ID_{1\text{-Boolean}})$ versus time.

As demonstrated in figure 5.27 the output of the comparator circuit ($V(ID_{1\text{-Boolean}})$) is 1 when the diode D_1 is conducting and 0 when it is not conducting. The sensitivity of the comparator circuit can be adjusted using potentiometer RV_1 shown in figure 5.13. If the sensitivity is set too high, it can cause false outputs due to noise and if it is set too low it will not detect when diode is conducting. Therefore, the RV_1 needs to be adjusted carefully for every switch and diode to output the correct data. Moreover, the false edges that are demonstrated in figure 5.27 are removed in the mode of operation extractor MATLAB code in spurious modes remover section.

5.4.5 Verification of the digital level shifter circuit

In order to verify the operation of the digital level shifter circuit, the input of the circuit is connected to the output of the comparator circuit, then the signals are compared to verify the operation. The output signal ($V(ID_{1\text{-Digital}})$) should be a clean digital data representing the $V(ID_{1\text{-Boolean}})$. Figure 5.28 shows the $V(ID_{1\text{-Boolean}})$ and $V(ID_{1\text{-Digital}})$ signals.

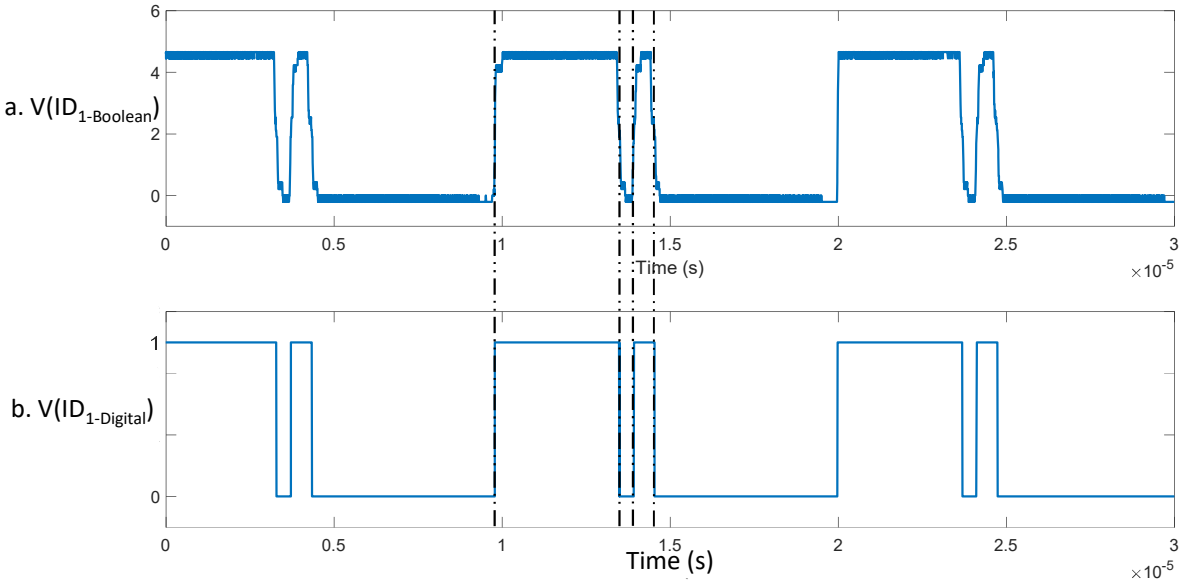


Figure 5.28: The waveforms of $V(ID_{1\text{-Boolean}})$ and $V(ID_{1\text{-Digital}})$ versus time.

As demonstrated in figure 5.28 the $V(ID_{1\text{-Digital}})$ signal represents the $V(ID_{1\text{-Boolean}})$ signal and the noise and the fall time and rise time has been removed. This verifies the operation of the digital level shifter circuit. (The $V(ID_{1\text{-Digital}})$ signal is measured using the logic analyser of the oscilloscope).

5.4.6 Verification of the conduction state to digital signal converter system using current sense resistor measurement technique

As each part of the conduction state to digital signal converter system has been tested and verified, it is now necessary to validate the operation of the complete system together. For this task the current waveform of D_1 and the $V(ID_{1\text{-Digital}})$ has to be compared to check if the signal is 1 when the diode is conducting and zero for when the diode is off. Figure 5.29 shows the signals ID_1 and $V(ID_{1\text{-Digital}})$.

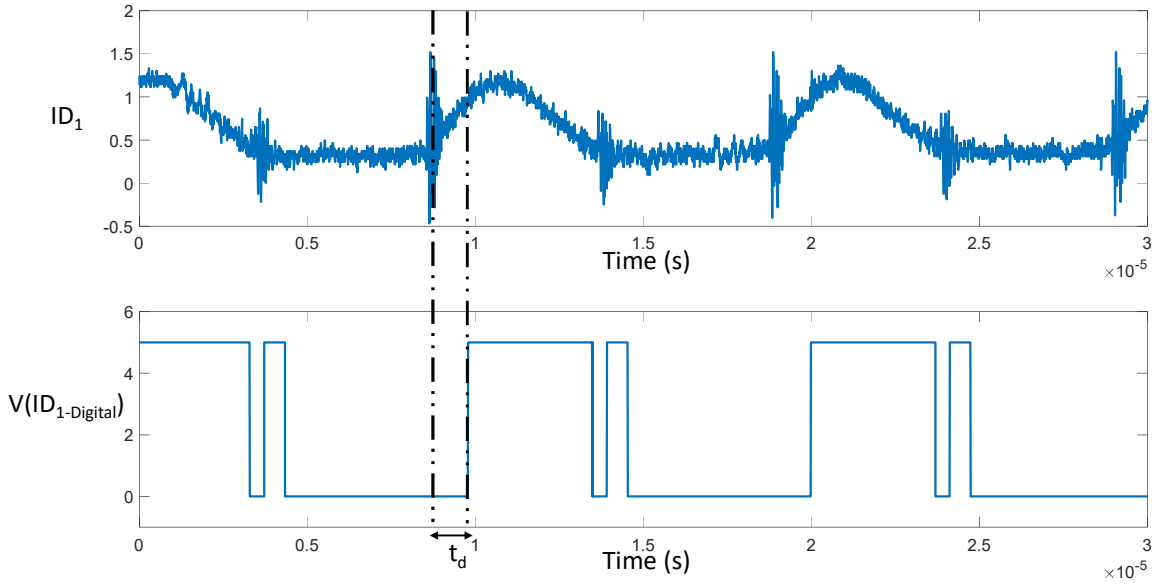


Figure 5.29: The waveforms of ID_1 and $V(ID_{1\text{-Digital}})$ versus time.

As illustrated in figure 5.29 the $V(ID_{1\text{-Digital}})$ is high when the diode D_1 is conducting. However, there is a delay time between the two signals. The delay time is demonstrated as t_d in figure 5.29. This delay time is mainly due to the transition time and the propagation delay of the comparator circuits and the logic gates. Although the delay time is a few microseconds and it is significant, it can be neglected as it is present for all the signals. As each signal for the current measurements of the components travels the same path and the same PCBs, it can be assumed that the delay time of the signals are equal. Therefore, no spurious mode is created and only the detected modes of operation is shifted by a few microseconds, hence the output data is valid.

5.4.7 Verification of the conduction state to digital signal converter using voltage measurement technique

Having verified the operation of the conduction state to digital signal converter using current measurement technique, now it is necessary to evaluate the operation of the voltage measurement technique. As explained earlier for this method no extra circuitry is needed and only MATLAB codes are used. Therefore, in this section the operation of the MATLAB code is verified.

For this evaluation the voltages and currents of diodes and MOSFETs are recorded. Then the recorded data are imported into MATLAB using CSV files and then the generated conduction state digital data by MATLAB are compared with the current signal of the diode or MOSFET to verify the operation of the MATLAB code.

Figure 5.30 demonstrates the voltage and current of diode D_1 and the generated conduction state digital data.

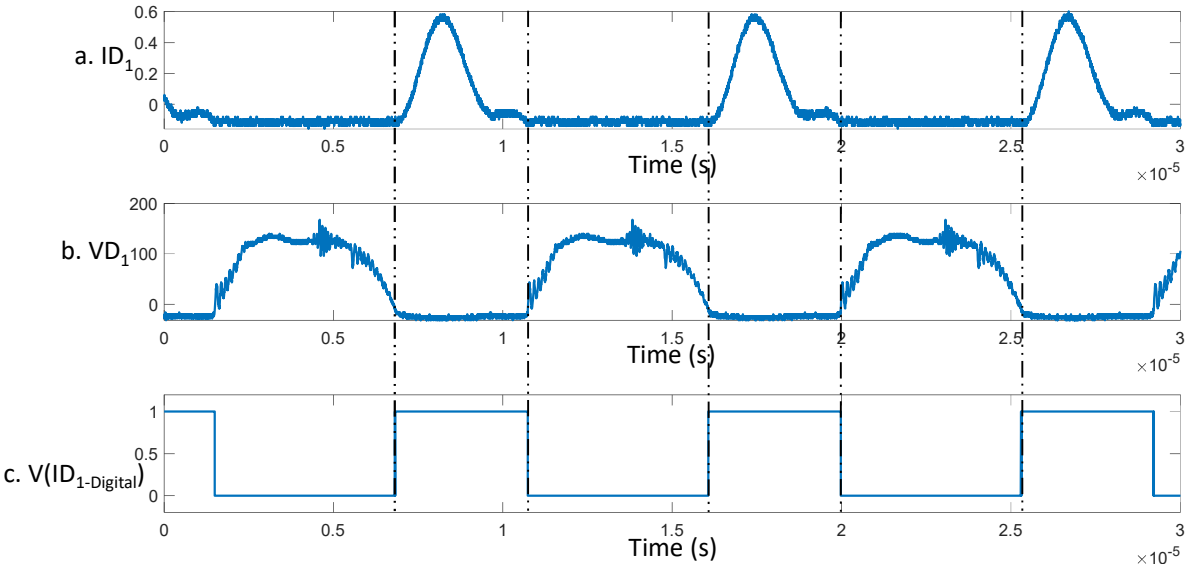


Figure 5.30: The voltage, current and conduction state signals of diode D_1.

As demonstrated in figure 5.30 when the current through diode D_1 is greater than zero, the voltage across the diode is nearly zero and the MATLAB code outputs 1 for that duration. In contrast, when the current through the diode is nearly zero, the voltage across the diode is more than zero and the MATLAB code outputs 0 for the conduction state digital signal. Therefore, this verifies the operation of the MATLAB code for the diode D_1.

Figure 5.31 demonstrates the voltage and current of diode D_2 and the generated conduction state digital data.

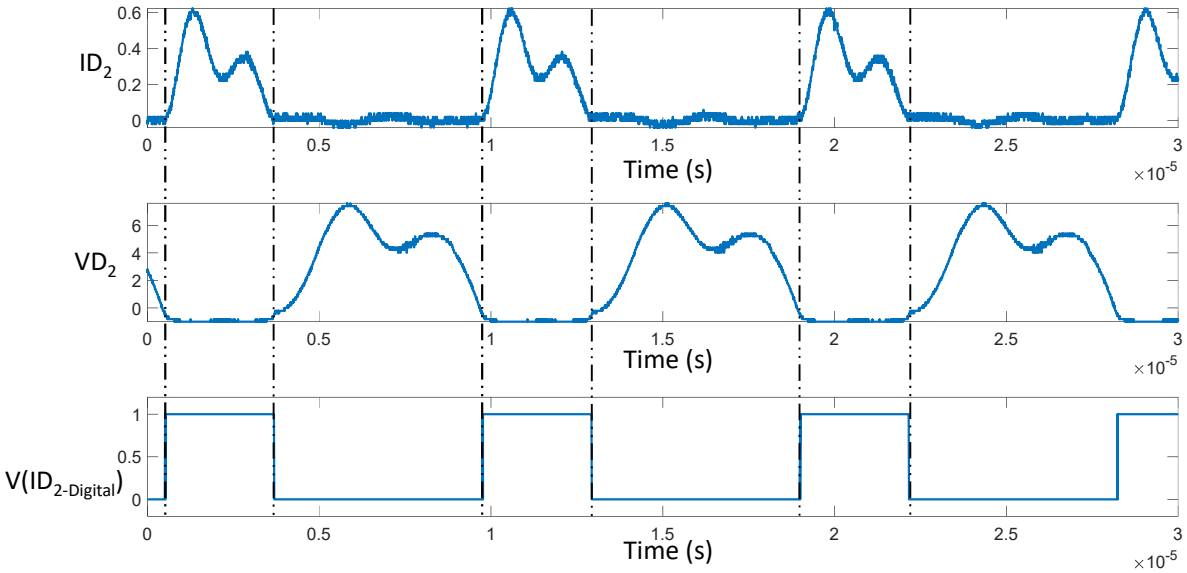


Figure 5.31: The voltage, current and conduction state signals of diode D_2.

As demonstrated in figure 5.31 when the current through diode D_2 (ID_2)is greater than zero the voltage across it (VD_2) is nearly zero and the MATLAB software generates 1 for conduction

state data. Therefore, this result confirms the operation of the MATLAB software for diode D_2.

In the next step the operation of the MATLAB code should be tested with the data for MOSFETs S_1 and S_2. As discussed earlier the conduction state data generation for the MOSFETs and their body diodes is more complex. Figure 5.32 demonstrates the gate signal (VG_1), VS_1, conduction state data of MOSFET S_1 and lastly the conduction state data for the body diode of MOSFET S_1 (D_6 in figure 5.9) versus time.

As demonstrated in figure 5.32, when the voltage across the MOSFET S_1 is near zero and the gate signal is high the generated conduction state data for the MOSFET is one. Moreover, when the VS_1 is near zero and the gate signal is low, it demonstrates that the MOSFET is turned off but the body diode of the MOSFET is conducting, hence the MATLAB software generates 1 for the conduction state data of the body diode.

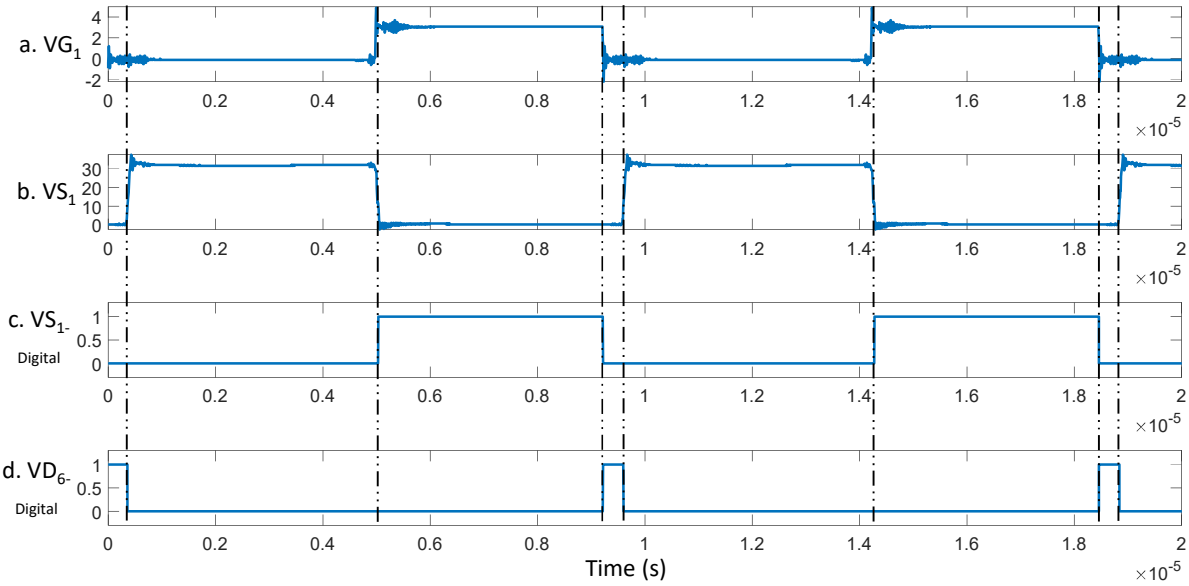


Figure 5.32: The gate signal and voltage of MOSFET S_1 with conduction state signals for MOSFET S_1 and diode D_6.

The last verification is for the MATLAB software with the voltage signals for the MOSFET S_2. Figure 5.33 shows the gate signal (VG_2), VS_2, conduction state data of MOSFET S_2 and lastly the conduction state data for the body diode of MOSFET S_2 (D_5 in figure 5.9) versus time.

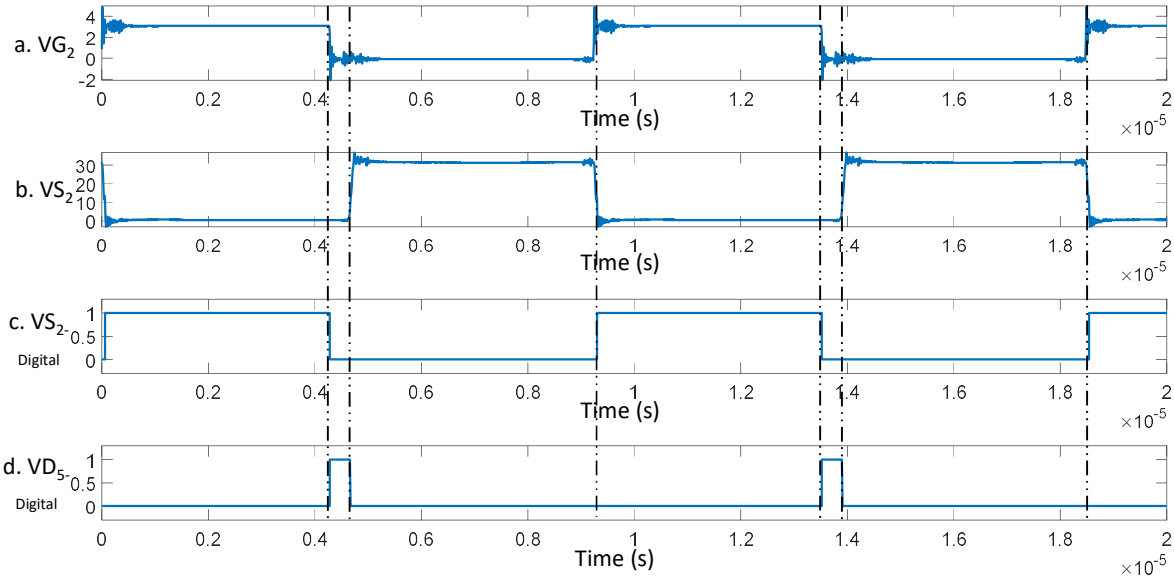


Figure 5.33: The gate signal and voltage of MOSFET S_2 with conduction state signals for MOSFET S_2 and diode D_5.

The results in figure 5.33 is the same as figure 5.30 for MOSFET S_1 and these results verifies the operation of the MATLAB software for conduction state data of MOSFET S_2 and its body diode.

Having verified and evaluated the operation of the CSCP-PFC system, the conduction state data to digital signal converter using both voltage and current measurement techniques, it is now possible to setup the complete system to extract the modes of operation of the system in a practical experiment. In the next section the extracted modes of operation of the system in a practical experiment are demonstrated and discussed.

5.5 Detected modes of operation in the experimental setup

In this section the detected modes of operation from the experimental system that has been discussed in the previous section are demonstrated. Similar to the simulations in previous chapter, first the response to DC input voltage is provided and then the system is tested with an AC input voltage under the PFC conditions, PF over-corrected, PF under corrected and PF fully corrected. These conditions are discussed in detail in chapter 4 in section 4.7.

5.5.1 The modes of operation of the system with a DC input voltage

For this test the system with the three different parameters (the parameters are demonstrated in tables 4.1 to 4.3 in chapter 4) of the resonant tank has been tested. The results revealed that only one mode of operation exist for the system with an DC input voltage, regardless of system parameters. The detected mode of operation is demonstrated

in table 5.1. The layout of table 5.1 is the same as the tables in chapter 4 that demonstrates the modes of operation.

Mode	Mode of operation 9 (M9)							
Conduction state	S1(68)	S2(64)	S3(66)	S4(18)	S5(34)	S6(32)	S7(36)	S8(12)
D_1			X	X	X			
D_2	X						X	X
D_3								X
D_4				X				
S_1					X	X	X	
S_2	X	X	X					

Table 5.1: The modes of operation M9.

As demonstrated in table 5.1 the extracted modes of operation for the system with a DC input voltage is different to the results from the simulations demonstrated in chapter 4. Furthermore, if the experimental results are compared with the mode of operation that are presented in chapters 2 and 3, it can be seen that the modes of operation are almost identical, except the in practical results there are 2 extra conduction states S4 and S8. These two conduction states are the transitions when switch S_2 turns off and switch S_1 turns on and the other way around for transiting from S_1 to S_2. These results are discussed in the next sections. Lastly, the waveforms of resonant current, bridge voltage and the voltage at node m associated with this mode of operation are shown in figure 5.34 and the extracted bit-pattern that demonstrates the mode of operation is demonstrated in figure 5.35.

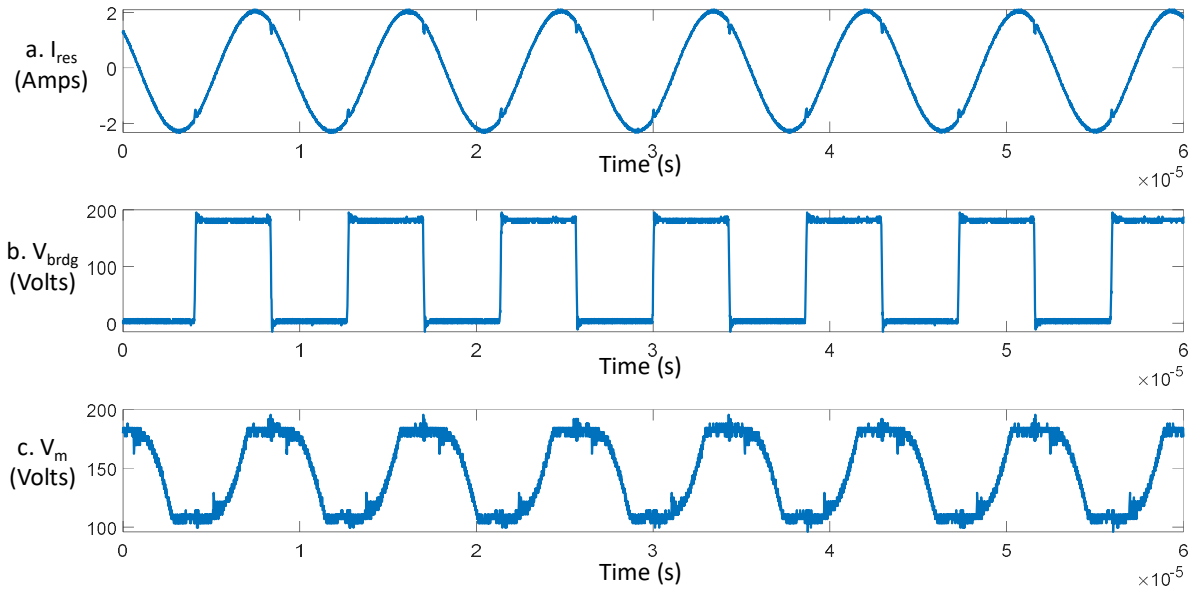


Figure 5.34: Wavefors of I_{res}, V_{brdg} and V_m for mode of operation M9.

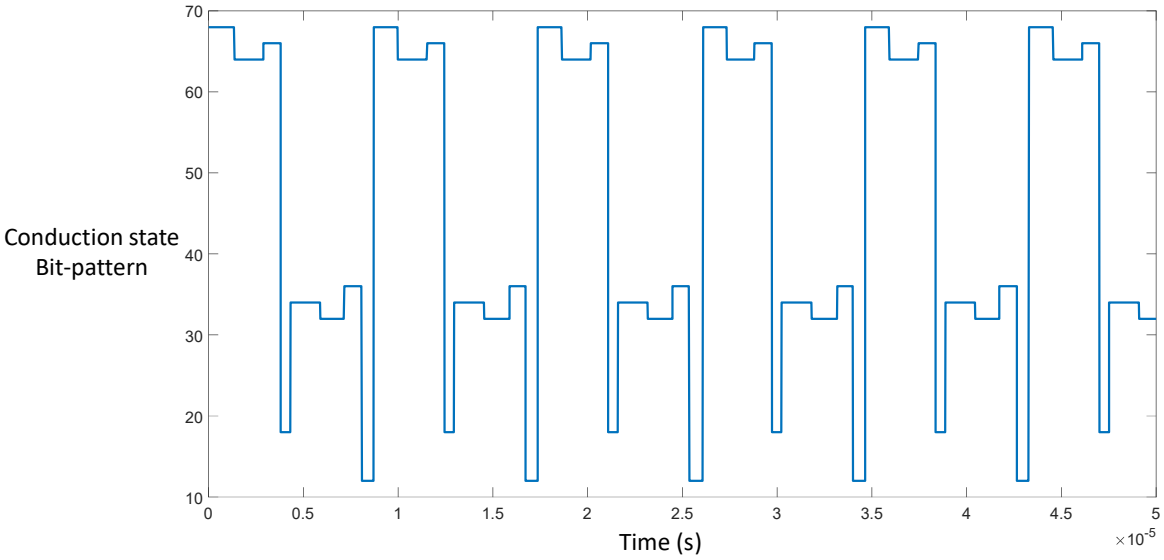


Figure 5.35: The waveform of extracted bit pattern illustrating mode of operation M9.

5.5.2 The mode modes of operation of the system with an AC input voltage

In order to make the results comparable with those presented in chapter 4, the practical experiments are done under the three different PF conditions and the extracted modes of operation are different from simulation results. The results from each condition are as follows.

PF under-corrected

The results for the system with each resonant tank showed only a single mode of operation and it is the same as the mode of operation demonstrated in table 5.1 over the duration of one mains cycle (20 ms). These results are the same as the results from simulation tests, as in simulation for each circuit the detected modes of operation of the system under PF under-corrected condition was the same as the modes of operation of the system with the DC input voltage. As detected modes of operation of the system are identical for all three resonant tanks over the duration of one mains cycle, only the results for resonant tank 1 are demonstrated in figure 5.36. Figure 5.36 demonstrates the input voltage and current and the detected modes of operation of the system with resonant tank 1 and under PF under corrected condition.

The waveform of figure 5.36c demonstrates if that mode is detected or not. A 1 or when the signal is high it shows that the associated mode of operation is detected and a low signal means that it is not detected. Moreover, as the waveform is high for the whole duration of the mains cycle, it represents that only mode of operation M9 has been detected.

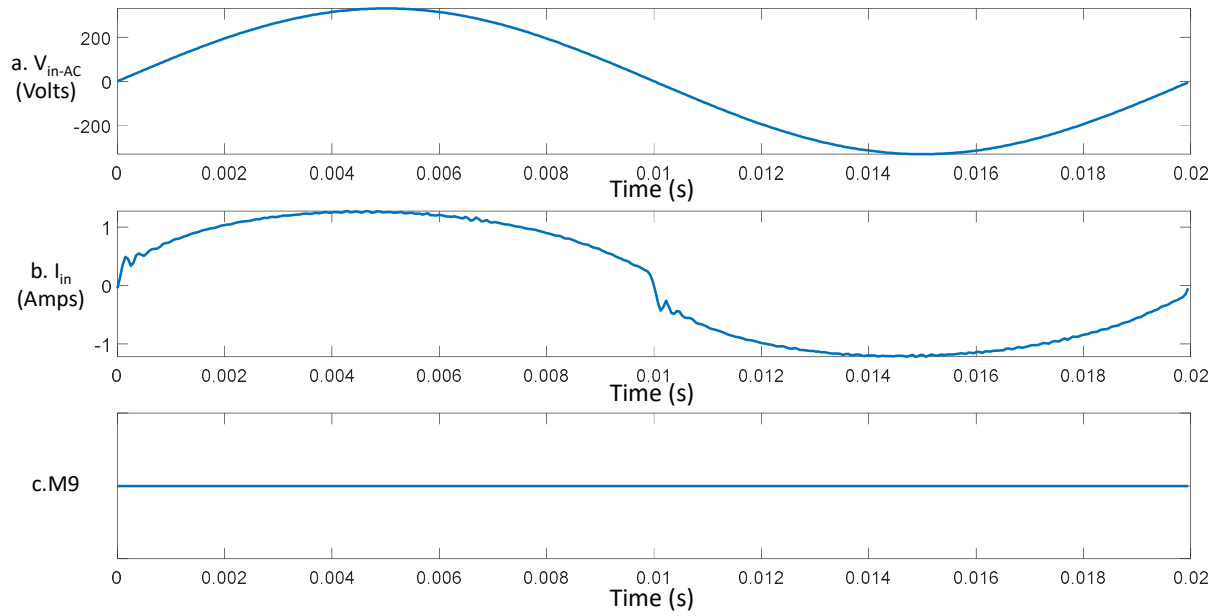


Figure 5.36: The results of the system with resonant tank 1 operating under PF under-corrected condition.

PF over-corrected

For the condition when PF over-corrected, only 2 modes of operation has been detected for all the three resonant tanks. The occurrence of these two modes of operation depends on the input line current to the system. Figure 5.37 demonstrates the input line current of the system operating on PF over-corrected condition.

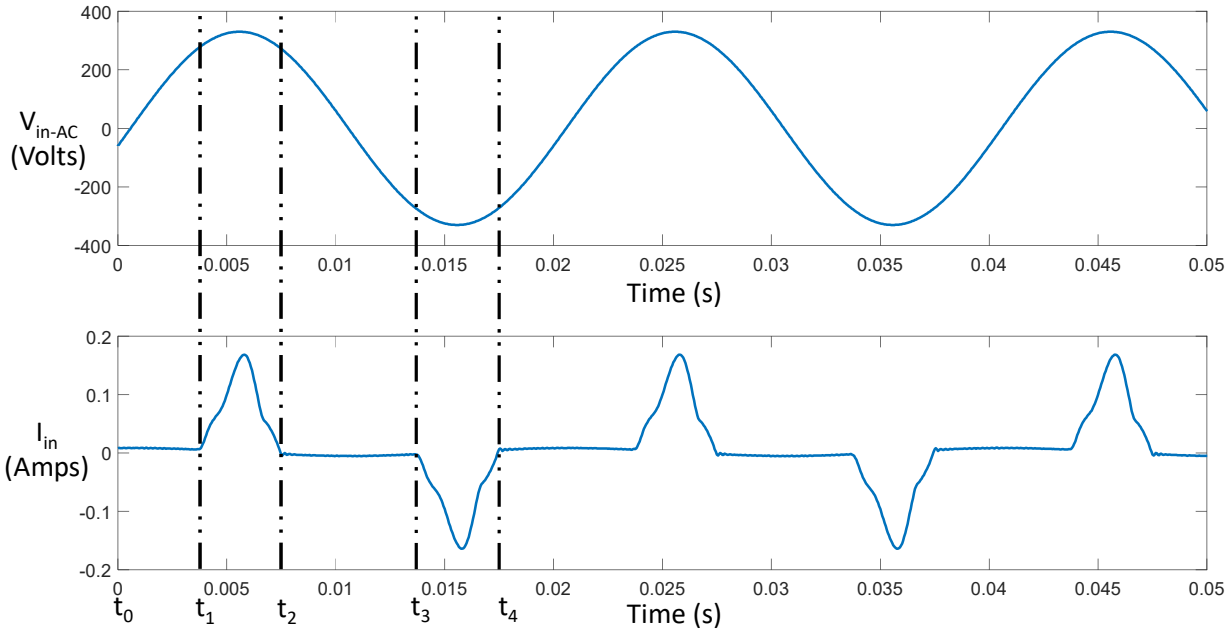


Figure 5.37: Input line voltage current of the system operating under PF over-corrected condition.

As demonstrated in figure 5.37 the input current can be divided into two different conditions, first condition is for the durations of t_0-t_1 and t_2-t_3. In this condition the input current to the circuit is zero. During this interval a small current flows through the LC input filter since the line voltage is too low for forward bias the input rectifier and the charge pump diodes. This behaviour is consistent for all three sets of resonant tank parameters considered. The sequence has been termed Mode 10 and the sequence of switch states is provided in Table 5.2. During the intervals t_1-t_2 and t_3-t_4 the charge pump diodes are active since the value of the input voltage is sufficient to forward bias the charge pump diodes and, therefore, current flows from the input AC voltage source as triangular shaped current pulses. The mode sequence when the charge pump is active is termed mode M11 details of which are provided in table 5.3.

Mode	Mode of operation 10(M10)			
Conduction state	S1(64)	S2(16)	S3(32)	S4(8)
D_1				
D_2				
D_3				X
D_4		X		
S_1			X	
S_2	X			

Table 5.2: The mode of operation M10.

Mode	Mode of operation 11 (M11)				
Conduction state	S1(70)	S2(18)	S3(34)	S4(38)	S5(14)
D_1	X	X	X	X	X
D_2	X			X	X
D_3					X
D_4		X	X		
S_1				X	
S_2	X				

Table 5.3: The mode of operation M11.

Moreover, the resonant current, voltage at node m and the bridge voltage for the system while operating with modes of operation M10 and M11 are illustrated in figures 5.38 and 5.39 respectively.

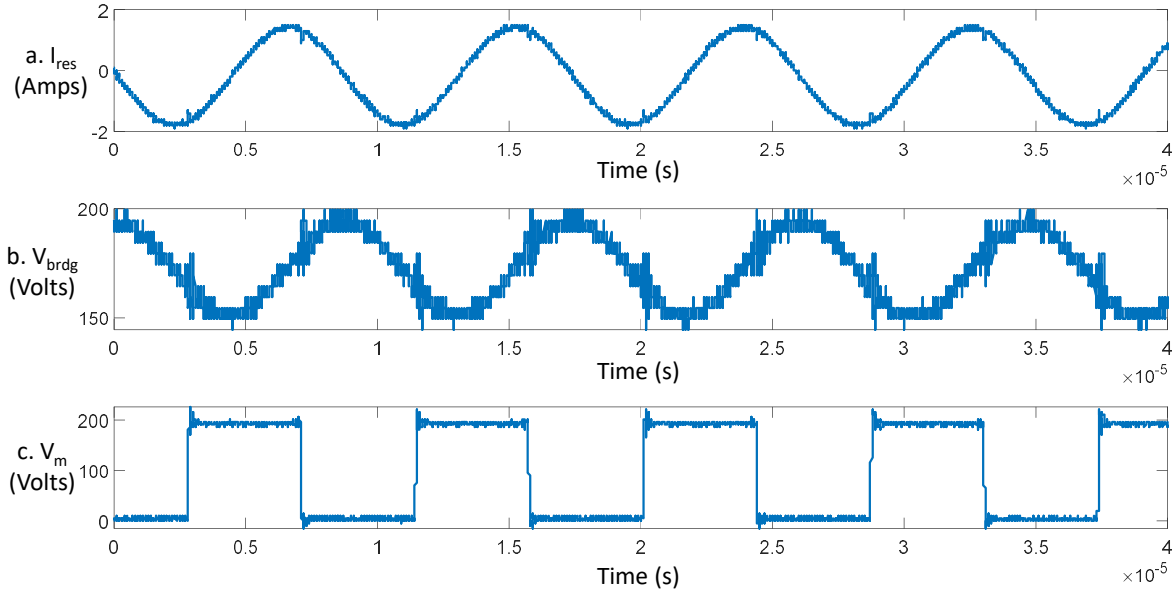


Figure 5.38:Wavefors of I_{res}, V_{brdg} and V_m for mode of operation M10.

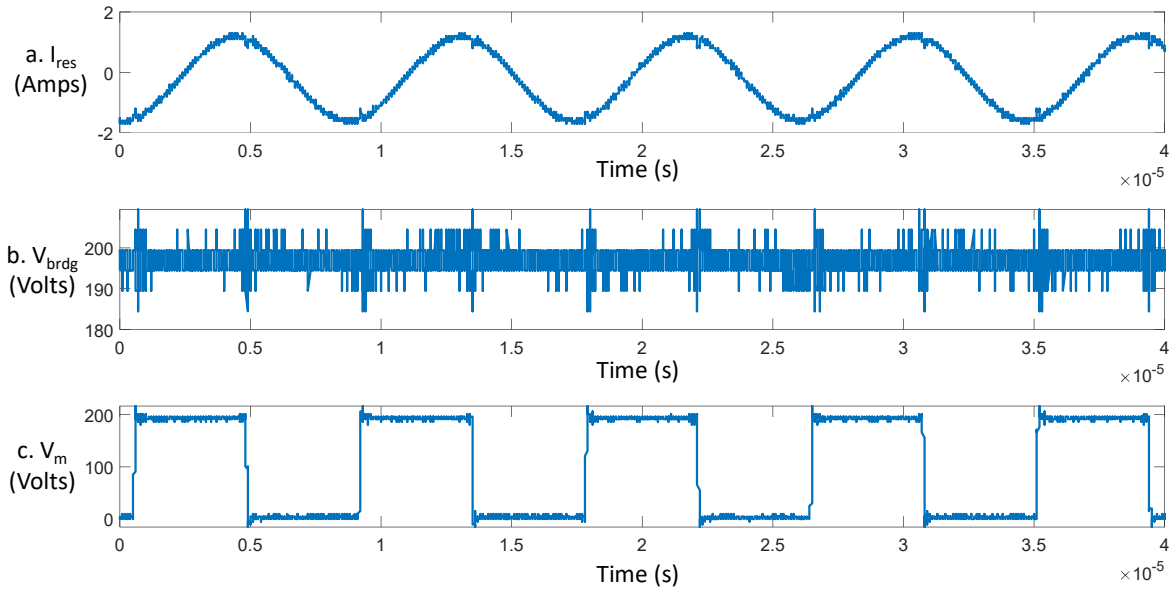


Figure 5.39: Wavefors of I_{res}, V_{brdg} and V_m for mode of operation M11.

As demonstrated in figure 5.38b the voltage V_m is a sinusoidal voltage. This is because that diodes D_1 and D_2 do not conduct in this mode of operation. Therefore, the resonant current only flows through C_{pfc} causing this sinusoidal shape voltage waveform. On the other hand, for mode of operation M11 the voltage of node m is clamped to the input voltage as the diode D_1 conducts for the whole duration of the mode of operation.

PF corrected

Figure 5.40 shows the input voltage and input current waveform for the PF fully corrected operating condition. Three different modes of operation have been observed. One of these

modes has been previously observed with a DC input voltage and is labelled M9, table 5.1. The remaining two modes have been termed M12 and M13 and are described in tables 5.4 and 5.5 respectively. The observed modes of operation occur consistently for all three resonant tank parameter values considered and their occurrence depends on the input voltage value.

Mode	Mode of operation 12 (M12)					
Conduction state	S1(68)	S2(64)	S3(10)	S4(34)	S5(32)	S6(16)
D_1			X	X		
D_2	X					
D_3			X			
D_4						X
S_1				X	X	
S_2	X	X				

Table 5.4:The mode of operation M12.

Mode	Mode of operation 13 (M13)			
Conduction state	S1(70)	S2(14)	S3(38)	S4(22)
D_1	X	X	X	X
D_2	X	X	X	X
D_3				
D_4		X		X
S_1			X	
S_2	X			

Table 5.5:The mode of operation M13.

Lastly, the resonant current, voltage at node m and the bridge voltage for the system while operating with modes of operation M12 is illustrated in figure 5.40.

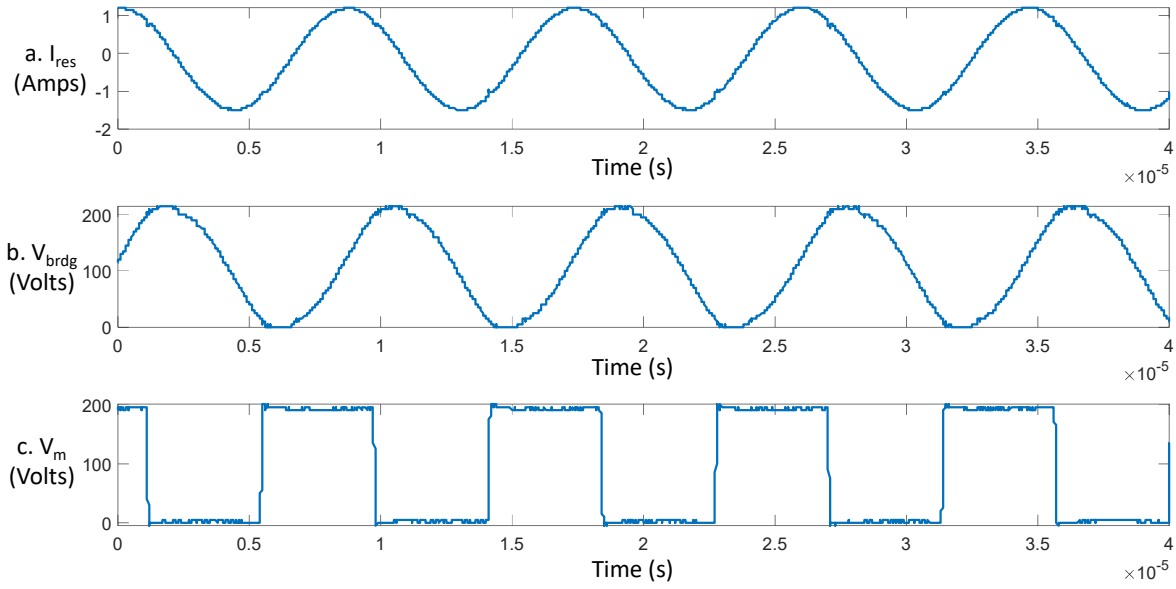


Figure 5.40: Waveforms of I_{res}, V_{brdg} and V_m for mode of operation M12.

As demonstrated in figure 5.40, the voltage at V_m oscillates between zero and the V_b. This is because that the input voltage at this point is near zero and when diode D_1 starts conducting V_m falls to zero and when diode D_2 starts conducting, V_m increases to V_b and the sections between these two points are for charging and discharging of the C_{pfc}.

As mentioned earlier, the occurrence of the mode of operations in a PF corrected condition depends on the input voltage value, similar to the modes of operation of the PF over-corrected condition. When the input voltage is at or close to zero (including the zero crossing) mode M12 occurs (labelled as interval t_{zero} in Fig. 5.41). When the voltage is at and/or near its peak value (labelled at t_{peak}) mode M13 occurs. The remaining sections of the input voltage (labelled as t_{middle}) is characterised by mode M9. Figure 5.41 demonstrates the classification of the input voltage and current that has been described in this section.

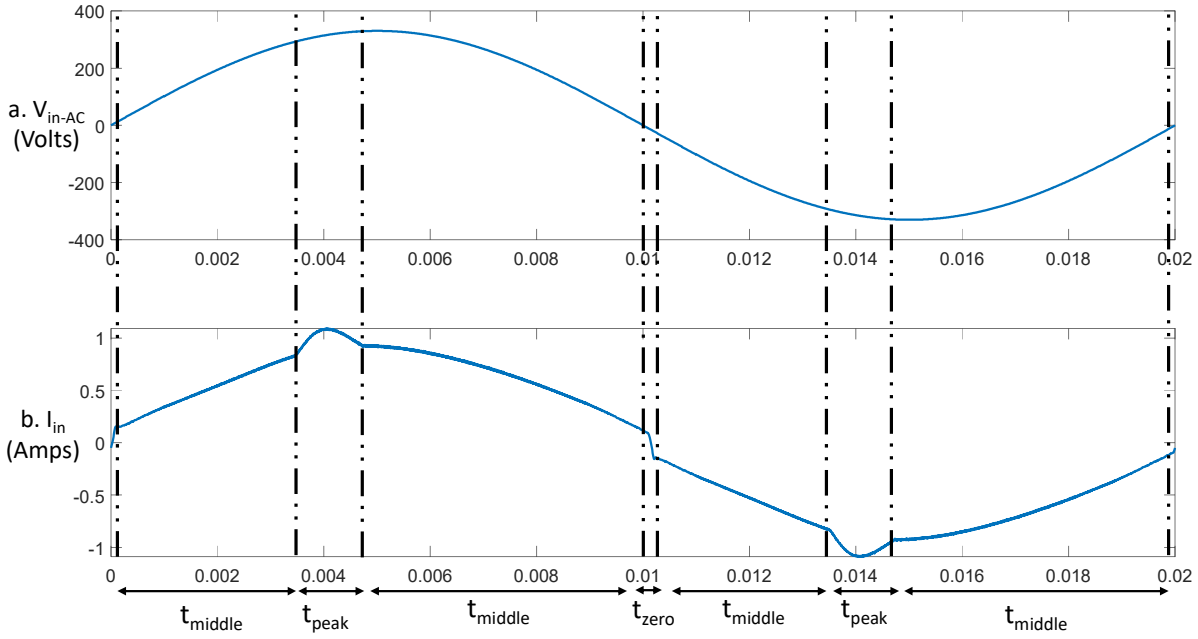


Figure 5.41: The classification of the input voltage and current for a PF corrected condition.

Having explained the occurrence of the modes, the next section looks at the response for each resonant tank parameter set considered.

The detected modes of operation of the system with resonant tank 1

Figure 5.42 illustrates the occurrence of the detected modes of operation for the system with resonant tank 1.

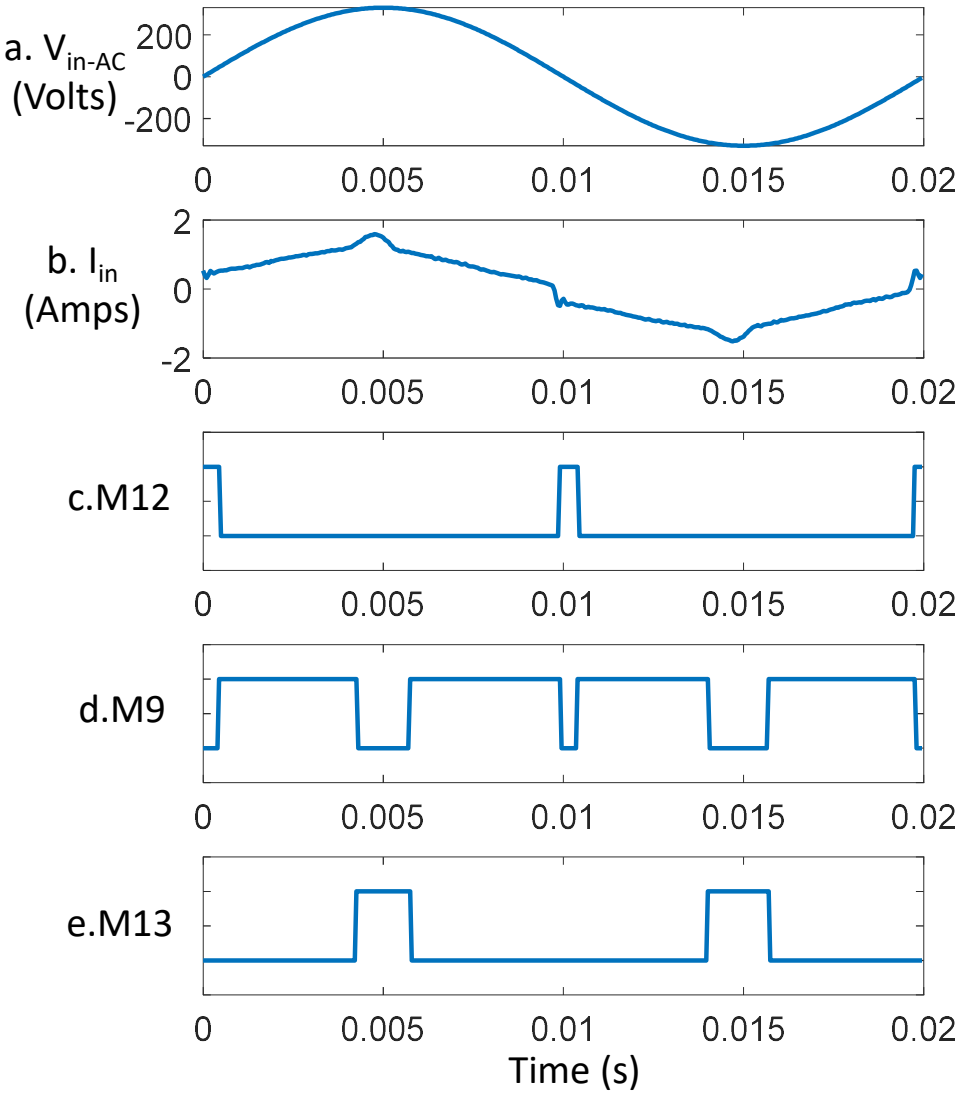


Figure 5.42: The occurance of the modes of operation of the system with resonant tank 1.

In figure 5.42 the waveform for each mode is shown with the input current and the input voltage. The waveform for each mode of operation demonstrates if that mode is detected or not. A high level indicates that a modes of operation is active.

The detected modes of operation of the system with resonant tank 2

Figure 5.43 illustrates the occurrence of the detected modes of operation for the system with resonant tank 2.

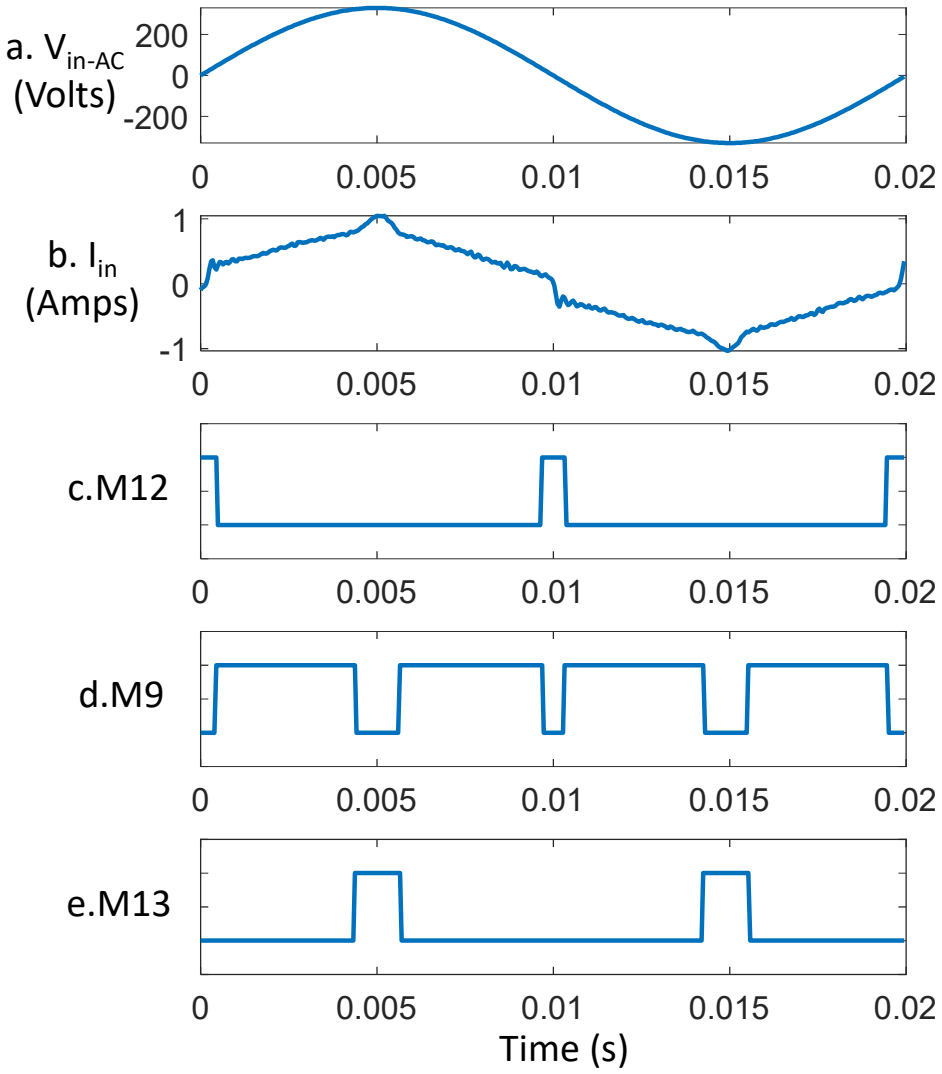


Figure 5.43: The occurance of the modes of operation of the system with resonant tank 2.

In the next stage the modes of operation of the system with resonant tank 3 is demonstrated.

The detected modes of operation of the system with resonant tank 3

Figure 5.44 illustrates the occurrence of the detected modes of operation for the system with resonant tank 3.

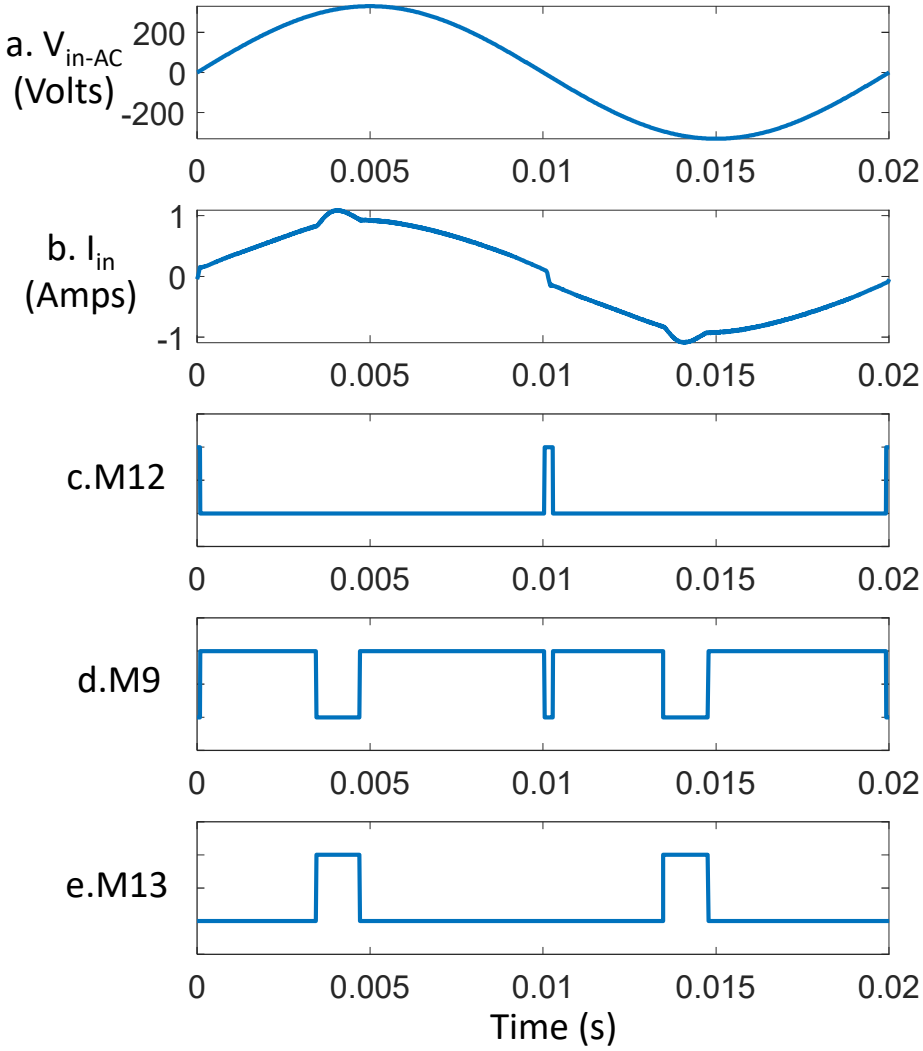


Figure 5.44:The occurance of the modes of operation of the system with resonant tank 3.

5.6 Simulation and practical results comparison

Up to this point, the modes of operation of the system with three resonant tanks and with both DC and AC input voltage under all different PF conditions have been extracted and demonstrated. The experimental results verified the suspicious that was made at the end of previous chapter. In simulation results many modes of operation were detected and there was no logical order for the occurrence of them (except for DC input voltage tests). In contrast, for the practical experiments only 4 modes of operation have been detected and a logical order exist for their occurrence for every PF condition. These differences between simulation and practical results may be caused by two factors.

One major difference is the use of ideal components in the circuit simulation package. Actual components are not ideal and there are parasitic elements for every component in the system and this will have an impact of circuit behaviour that is not represented in the simulation model. Although more accurate models for the semiconductor devices could be used and some parasitic components included in the simulation circuit some parameters are determined by the circuit layout and cannot easily be quantified for simulation purposes.

The second factor is that the MOSFETs and their body diodes are treated as individual components. The problem that is raised by this factor is that it is possible that in simulation the current flows through a MOSFET and in practice it flows through the body diode of that MOSFET, or vice versa. In this situation the observable current path is the same although the actual current is flowing through different components. However, the mode of operation extractor system and MATLAB code detect 2 different modes of operation. This case has occurred for the mode of operation M1, M9 and the mode of operation that has been illustrated in chapters 2 and three. Technically the current path for all of these modes of operation is the same and the only differences is that if the current flows through the MOSFETs or their associated body diodes. Therefore, by treating the MOSFETs and their body diodes as a single component, fewer modes of operation may be detected and the high number of modes of operation in the simulation results may be illuminated.

5.7 Conclusion

In conclusion, the design process of the modular CSCP-PFC system has been given. The reasons and advantages of modular design have been explained. Then the design of each module of the system have been completely discussed.

Moreover, in this chapter two novel techniques to convert the conduction state of components into digital signals have been introduced. Each technique and the signal processing of them have been fully explained.

The verification process of each module of the CSCP-PFC system is given. Furthermore, the verification of the conduction state into digital signal converter has been demonstrated and the issues for the current measurement technique have been illustrated with their solutions.

Lastly, the detected modes of operation of the system with both AC and DC input and under all PF condition have been fully discussed. Moreover, the protentional causes of the differences in the simulation and practice results have been given.

The next chapter provides a conclusion to the work described in thesis and provides a number of suggestions for further research for CSCP-PFC systems.

5.8 References

[1] P. Horowitz and W. Hill, “The Oscilloscope,” in *The Art of Electronic* , Cambridge, Cambridge University Press, 2015, pp. 1158-1164.

[2] A. S. Sedra and K. C. Smith, “Differential and Multistage Amplifiers,” in *Microelectronic circuits*, Oxford, Oxford University Press, 2004, pp. 687-790.

[3] P. Horowitz and W. Hill , “Differential Amplifiers,” in *The Art of Electronic*, Cambridge, Cambridge University Press, 2015, pp. 372-380.

[4] P. Horowitz and W. Hill, “Driving digital logic from comparators or op-amps,” in *The Art of Electronics*, Cambridge, Cambridge University Press , 2015, p. 809.

[5] A. S. Sedra and K. C. Smith , “Comparators,” in *Microelectronic Circuits*, Oxford, Oxford University Press, 2004, pp. 1189-1191.

[6] A. S. Sedra and K. C. Smith, “Schmidt Trigger,” in *Microelectronic Circuits* , Oxford, Oxford University Press, 2004, p. 1188.

Chapter 6 Conclusion and further research

6.1 Introduction

In this chapter a detailed summary of the work that has been presented in this thesis is given. The work that has been presented in the chapters is discussed as a whole. Lastly, a number of proposals are suggested to expand and continue the research on CSCP-PFC systems.

6.2 Conclusions

This work started by presenting what is power factor and why it is such an important parameter in AC powered appliances and what consequences low PF can impose on grid voltage and equipment. Moreover, a brief summary of different techniques to improve power factor has been demonstrated. In the comparison of PFC techniques, it has been showed that charge pump power factor correction techniques are inexpensive, small and efficient. However, there has not been adequate research on this type of PFC circuit and the existing models contain inconsistencies and they are not reliable to be used for circuit designing and practical projects. Therefore, the underpinning research on charge pump technologies and their functions has been completely presented. Then the literature review of SSCP-PFC has been given with the flaws and inconsistencies in the existing analytical model. After presenting the inconsistencies of the existing analytical models. A novel and precise analytical model based on FMA and describing functions has been demonstrated. In the evaluation process of the analytical model odd behaviours in the operation of the system had been observed. These odd behaviours lead to discovery of different modes of operation for system and as the analytical model has been developed for a particular mode of operation, the analytical model loses its precision when the system operates on a different mode of operation. These finding showed that there is a great demand for analysing the circuit with different parameters to extract the modes of operation of the system under different situations. For this task LTspice simulation package has been used with MATLAB. The LTspice outputs the simulation data and parameters, and MATLAB does the signal processing to extract the modes of operation. Results of these tests showed several different modes of operation that occur in no logical order. Therefore, the system had to be constructed to extract the modes of operation in practical platform. For this experiment the platform has been designed in a modular manner to ease the change of circuit components and parameters to be able to test all the simulations in practice and compare the results. Moreover, two different techniques for extraction of conduction state of the components have been demonstrated. The results of the practical experiments then compared to the simulation data and some results are identical while some are completely different. The reasons for the differences have been completely discussed and techniques to solve the inconsistencies between practical and simulation results are proposed.

In the next section a brief summary of each chapter is given.

6.3 The summary of each chapter

In chapter 1 a full discussion of power quality parameters such as PF and different types of power related to AC systems has been given. Moreover, the benefit of high power factor systems has been discussed along with how aspects of power quality is mandated by the law. After stating the advantages of having high PF, popular techniques used for PFC have been demonstrated and the advantages and disadvantages of each method has been stated. The comparison of the PFC methods indicates the benefits of using charge pump based power factor corrector systems for some applications.

Chapter 2 provides a review of the key technologies used in the field including a brief history of the charge pump circuits where it was shown that charge pump systems are used in many items electronic equipment including communication systems, computers, memories to power electronic systems. Following this, a review of resonant power conversion was provided, and it has been demonstrated that how these converters can maximise the efficiency of power converters and the impact they have on the life time of the power switches such as MOSFETs and IGBTs. A detailed literature review into the operation and the mathematical model CSCP-PFC system has been represented. Subsequently, an investigation using LTSPICE simulations has revealed inconsistencies in mathematical models described in the literature and this created the demand for a more precise mathematical model that describes the operation of the CSCP-PFC systems and the focus for the work presented in this thesis.

In chapter 3 a novel mathematical model has been demonstrated to eliminate the inconsistencies that existed in the previous model. The mathematical model has been derived using FMA and describing function techniques and it allows for calculation of the voltage and current at various points of the system. After the derivation of the mathematical model, a novel technique for the verification of the model has been demonstrated using only LTspice simulation package. The verification of the model using LTspice demonstrated that the model does work precisely with error of less than 5% when the circuit is powered from a DC voltage source. Moreover, it has been demonstrated that the model works over wide range of parameters of the system including switching frequency, resonant tank values and charge pump capacitor C_{pfc}. Unfortunately, the verification process showed that the mathematical model does not work when the circuit is powered from an AC voltage source. The investigation of the operation of the model with AC input voltage led to the discovery of that the circuit operates somewhat differently compared to the descriptions in the existing literature.

Chapter 4 described a detailed simulation investigation into the behaviour of CSCP-PFC system. A major part this was the development of a novel technique to extract the modes of operation of the system. This technique uses LTspice simulation package and a MATLAB code where within the LTSPICE simulation the conduction state of each diode and MOSFET is converted into a Boolean representation that can be processed by MATLAB code. The chapter

described MATLAB code in detail including the bit pattern generation on a LTSPICE sample-by-sample timeframe and conversion to the mode sequence pattern. In application, the LTSPICE/MATLAB mode extractor system has revealed some nine different modes of operation are possible and there was not a logical order for the occurrence of them it had been hypothesised that the results are not correct and in reality and practical experiments the results may be different.

Chapter 5 presented a hardware based mode extractor system and a modular CSCP-PFC platform for investigating real-world system behaviour. The design and operation of each module has been explained. Two novel techniques to extract the modes of operation of the system in a practical experimental platform has been presented. The operation of the mode extractor was validated using several experiments to demonstrate the signal conversion steps. Subsequently the system was applied to extract mode sequences from the modular CSCP-PFC platform. As expected, the initial investigation conducted with a DC input voltage showed that only single mode of operation is required to describe the behaviour of the circuit. Investigations were performed using an AC input voltage for a variety of PF conditions and it showed that there are only four modes of operation and their occurrence depends on the input voltage and current value and the PF condition that the circuit is operating under.

6.4 Further research

This thesis represented detailed research and a mathematical model on CSCP-PFC systems. However, there are several other tasks that need to be done in order to be able to mathematically model the system with an AC input voltage. The other tasks are as follows:

6.4.1 LTspice simulation model

Simulation are a great and precise tool to observe the behaviour of electronic circuits if they are given correct parameters. However, in chapters 4 and 5 it has been shown that the results from simulation are different comparing to practical results. One of the probable causes of this difference is using ideal components in the simulation model and not considering the parasitic elements of the components. This problem does not have a major impact on many electrical circuits but in resonant converters and charge pump circuits a small variation in the circuit parameters can have major impact on the results due to the nature of the these circuits and their high Q factor design. To address this issue and have reliable simulation model it is necessary to have practical setup and to design the simulation model based on the practical setup. For the simulation model all the diodes and MOSFETs need to be the exact component model from the manufacturer. Moreover, the parasitic elements of the passive components such as Equivalent Series Resistance (ESR) and series inductance needs to be measured with an LCR meter with measurement frequency of the switching frequency (The parasitic elements are a function of frequency). Then these parameters can be added to the simulation model. Lastly, the designed simulation model can be tested against the practical setup to

ensure the operation of the simulation model. Finally, this simulation model along with the practical setup can be used for further research on the CSCP-PFC systems.

6.3.1 The modes of operation

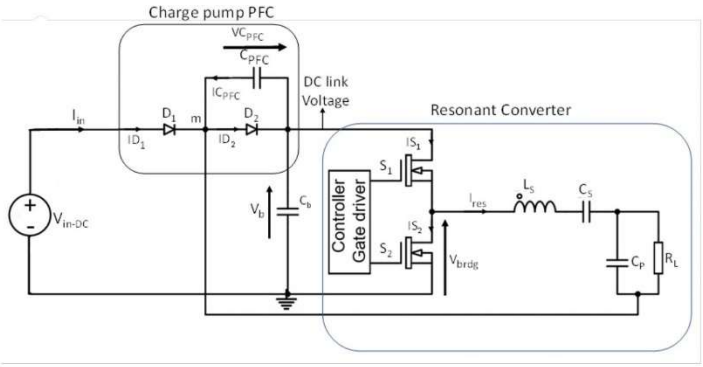
As demonstrated and discussed in chapters 4 and 5, 13 different modes of operation have been detected for the CSCP-PFC system. One of the main causes of this is that the MOSFETs and their associated body diodes are treated as individual components. Although the current path is the same, the mode extractor systems will detect different results. If the MOSFETs and their associated body diodes are treated as a single component, first it will decrease the number of modes of operation massively. Secondly, it will simplify the modes of operation results for further processing and mathematical modelling. Moreover, treating the MOSFET and its body diode as an individual component will not have an effect on the mathematical modelling. As demonstrated in chapter 3 for the mathematical modelling using FMA and describing function techniques, the path that the current flows is important and in this case the path is the same, whether the current flows through the MOSFET or its body diode.

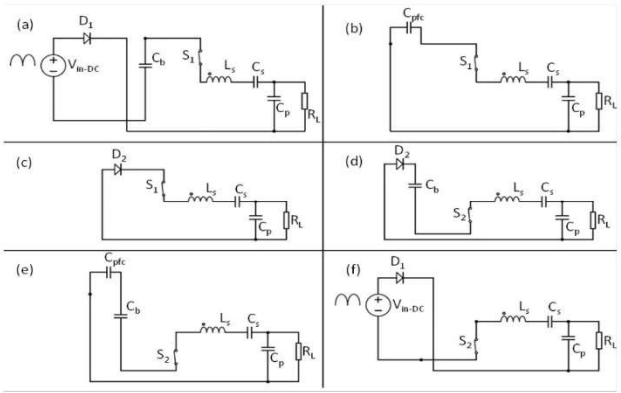
6.3.2 The mathematical model

After successful completion of the previous two tasks, by having a verified mode of operation for the system with an AC input voltage. It will be possible to develop analytical models that correctly describe the operation of the converter and come with a full understating of its operation when the system is powered from an AC voltage source. Then the work could be extended to design a tool that receives the given parameters and design the CSCP-PFC system based on the provided parameters.

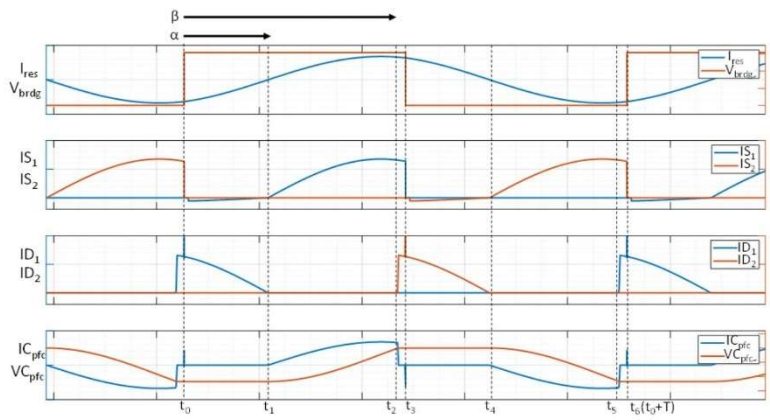
Appendix 1. The Maple mathematical model

```
> restart;
> #CSPFC
> #CSPFC 8
>
> #12/01/2022
> # This version derives the voltage at node m as Vm=Vb-Vcpfc
> #As this is a mathematical model, subscripts for voltagea and
  currents are not used here; However. all the variables and
  parameters are the same as the ones introduced in chapter 4.

                              The circuit diagram showing the
  signals of intreset and modes of operation waveform from chapter
  three and the modes of operation diagram are demonstrated below
  to ease the understandings of the model.
```






```
>
>
```




```
> #main assumption is resonant current is sinusoidal
>
> #second assumption is that d1 and d2 conduct for the same amount
  of time
>
> Ires:=Iresp*sin(theta-alpha);
```

$$Ires := -Iresp \sin(-\theta + \alpha) \quad (1)$$

```
> # note the phase angle is defined as theta -alpha such that the
  solver returns alpha as positive
> # need to remember this when dividing by the resonant current to
  get the equivalent impedance
> # polarity of Vcin is defines as positive for Vdc-Vm
> # Looking at the resonant circuit, current Ires flows from left
  to right through Ls
> # Thus, the current flows into node m the negative terminal Cpfc.
   Therefore, current flows out of the positive terminal connected
  to Vb
> # Therefore the polarity of vcin is defined by the negative of
  the current iLs
> #derive an expression for Vm
> #during mode 1 d1 is already conducting therefore an initial
  condition exists on Cpfc
> #The voltage of Vm when diode D1 conducts.
> Vm_M1:=Vin;
```

$$Vm\_M1 := Vin \quad (2)$$

```
> #during mode 2 current flows into the left terminal of Cpfc.  The
  voltage on the right terminal is always held constant at Vb.
>
> vcpfc_M2:=-1/(omega*Cpfc)*int(Ires,theta)+Vinitial_M1;
```

(3)

$$vcpfc\_M2 := \frac{Iresp\cos(-\theta+\alpha)}{\omega\, Cpfc} + Vinitial\_M1 \quad (3)$$

```
> # initial condition for Vinitial_M1
> # at theta=alpha, vcpfc = Vb-Vm
> eq1:=Vb-Vm = subs(theta=alpha,vcpfc_M2);
```

$$eq1 := Vb - Vm = \frac{Iresp\cos(0)}{\omega\, Cpfc} + Vinitial\_M1 \quad (4)$$

```
> eq2:=subs(Vm=Vin,eq1);
```

$$eq2 := Vb - Vin = \frac{Iresp}{\omega\, Cpfc} + Vinitial\_M1 \quad (5)$$

```
> eq3:=Vinitial_M1=solve(eq2,Vinitial_M1);
```

$$eq3 := Vinitial\_M1 = \frac{Vb\,\omega\, Cpfc - Vin\,\omega\, Cpfc - Iresp}{\omega\, Cpfc} \quad (6)$$

```
> vcpfc_M2a:=subs(eq3,vcpfc_M2);
```

$$vcpfc\_M2a := \frac{Iresp\cos(-\theta+\alpha)}{\omega\, Cpfc} + \frac{Vb\,\omega\, Cpfc - Vin\,\omega\, Cpfc - Iresp}{\omega\, Cpfc} \quad (7)$$

```
> Vm_M2:=Vm=Vb-vcpfc_M2a;
```

$$Vm\_M2 := Vm = Vb - \frac{Iresp\cos(-\theta+\alpha)}{\omega\, Cpfc} - \frac{Vb\,\omega\, Cpfc - Vin\,\omega\, Cpfc - Iresp}{\omega\, Cpfc} \quad (8)$$

```
> #final condition of mode 2
> eq100:=subs({Vm=Vb,theta=beta},Vm_M2);
```

$$eq100 := Vb = Vb - \frac{Iresp\cos(-\beta+\alpha)}{\omega\, Cpfc} - \frac{Vb\,\omega\, Cpfc - Vin\,\omega\, Cpfc - Iresp}{\omega\, Cpfc} \quad (9)$$

```
> eq101:=Vb=solve(eq100,Vb);
```

$$eq101 := Vb = \frac{Vin\,\omega\, Cpfc - Iresp\cos(-\beta+\alpha) + Iresp}{\omega\, Cpfc} \quad (10)$$

```
> Vm_M2a := rhs(simplify(subs(eq101,Vm_M2)));
```

$$Vm\_M2a := \frac{Vin\,\omega\, Cpfc - Iresp\cos(-\theta+\alpha) + Iresp}{\omega\, Cpfc} \quad (11)$$

```
> Vm_M3:=Vb;
```

$$Vm\_M3 := Vb \quad (12)$$

```
> Vm_M3a := subs(eq101,Vm_M3);
```

$$Vm\_M3a := \frac{Vin\,\omega\, Cpfc - Iresp\cos(-\beta+\alpha) + Iresp}{\omega\, Cpfc} \quad (13)$$

```
> #PFC capacitor voltage during mode 4
> vcpfc_M4:=vcpfc=vcpfc_M2-Vinitial_M1+Vinitial_M2;
```

$$vcpfc\_M4 := vcpfc = \frac{Iresp\cos(-\theta+\alpha)}{\omega\, Cpfc} + Vinitial\_M2 \quad (14)$$

```
> #at the start of mode 4 vcpfc=0 since D2 was conducting
```

```
> eq10:=subs({vcpfc=0,theta=Pi+alpha},vcpfc_M4);
```

$$eq10 := 0 = \frac{Iresp\cos(-\pi)}{\omega\, Cpfc} + Vinitial\_M2 \tag{15}$$

```
> eq11:=Vinitial_M2=solve(eq10,Vinitial_M2);
```

$$eq11 := Vinitial\_M2 = \frac{Iresp}{\omega\, Cpfc} \tag{16}$$

```
> vcpfc_M4a:=subs(eq11,vcpfc_M4);
```

$$vcpfc\_M4a := vcpfc = \frac{Iresp\cos(-\theta+\alpha)}{\omega\, Cpfc} + \frac{Iresp}{\omega\, Cpfc} \tag{17}$$

```
> #as before, vm=vb-vcpfc
> Vm_M4:=Vb-vcpfc;
```

$$Vm\_M4 := Vb - vcpfc \tag{18}$$

```
> Vm_M4a:=subs(vcpfc_M4a,Vm_M4);
```

$$Vm\_M4a := Vb - \frac{Iresp\cos(-\theta+\alpha)}{\omega\, Cpfc} - \frac{Iresp}{\omega\, Cpfc} \tag{19}$$

```
> Vm_M4b:=simplify(subs(eq101,Vm_M4a));
```

$$Vm\_M4b := \frac{Vin\,\omega\, Cpfc - Iresp\cos(-\beta+\alpha) - Iresp\cos(-\theta+\alpha)}{\omega\, Cpfc} \tag{20}$$

```
> Vm_M5:=Vin;
```

$$Vm\_M5 := Vin \tag{21}$$

```
> f1:=piecewise(theta>=0 and theta<=alpha,Vm_M1,theta>alpha and
  theta<=beta,Vm_M2a,theta>beta and theta<=Pi+alpha,Vm_M3a,
  theta>Pi+alpha and theta<=Pi+beta,Vm_M4b,theta>Pi+beta and
  theta<=2*Pi,Vm_M5);
```

$$f1 := \begin{cases} Vin & 0 \le \theta \le \alpha \\ \dfrac{Vin\,\omega\, Cpfc - Iresp\cos(-\theta+\alpha) + Iresp}{\omega\, Cpfc} & \alpha < \theta \le \beta \\ \dfrac{Vin\,\omega\, Cpfc - Iresp\cos(-\beta+\alpha) + Iresp}{\omega\, Cpfc} & \beta < \theta \le \pi+\alpha \\ \dfrac{Vin\,\omega\, Cpfc - Iresp\cos(-\beta+\alpha) - Iresp\cos(-\theta+\alpha)}{\omega\, Cpfc} & \pi+\alpha < \theta \le \pi+\beta \\ Vin & \pi+\beta < \theta \le 2\,\pi \end{cases} \tag{22}$$

```
> #take fourier transform of Vm
>
> vm_s1:=1/Pi*int(sin(theta)*Vm_M1,theta=0..alpha);
```

$$vm\_s1 := \frac{Vin - \cos(\alpha)\, Vin}{\pi} \tag{23}$$

```
> vm_s2:=1/Pi*int(sin(theta)*Vm_M2a,theta=alpha..beta);
```

$$vm\_s2 := -\frac{1}{4\,\pi\,\omega\,Cpfc}\left(4\,Cpfc\cos(\beta)\,Vin\,\omega - 4\,Cpfc\cos(\alpha)\,Vin\,\omega - 2\,Iresp\sin(\alpha)\,\alpha + 2\,Iresp\sin(\alpha)\,\beta + 4\,Iresp\cos(\beta) - Iresp\cos(-2\,\beta+\alpha) - 3\,Iresp\cos(\alpha)\right) \quad (24)$$

```
> vm_s3:=1/Pi*int(sin(theta)*Vm_M3a,theta=beta..Pi+alpha);
```

$$vm\_s3 := \frac{\left(Vin\,\omega\,Cpfc - Iresp\cos(-\beta+\alpha) + Iresp\right)\left(\cos(\beta)+\cos(\alpha)\right)}{\pi\,\omega\,Cpfc} \quad (25)$$

```
> vm_s4:=1/Pi*int(sin(theta)*Vm_M4b,theta=Pi+alpha..Pi+beta);
```

$$vm\_s4 := \frac{1}{4\,\pi\,\omega\,Cpfc}\left(4\,Cpfc\cos(\beta)\,Vin\,\omega - 4\,Cpfc\cos(\alpha)\,Vin\,\omega + 2\,Iresp\sin(\alpha)\,\alpha - 2\,Iresp\sin(\alpha)\,\beta + 2\,Iresp\cos(\beta) - Iresp\cos(-2\,\beta+\alpha) - 3\,Iresp\cos(\alpha) + 2\,Iresp\cos(2\,\alpha-\beta)\right) \quad (26)$$

```
> vm_s5:=1/Pi*int(sin(theta)*Vm_M5,theta=Pi+beta..2*Pi);
```

$$vm\_s5 := \frac{-\cos(\beta)\,Vin - Vin}{\pi} \quad (27)$$

```
> vm_s:=simplify(vm_s1+vm_s2+vm_s3+vm_s4+vm_s5);
```

$$vm\_s := \frac{1}{2\,\pi\,\omega\,Cpfc}\left(\left(\cos(2\,\alpha-\beta) + \left(-2\cos(\beta) - 2\cos(\alpha)\right)\cos(-\beta+\alpha) + 2\cos(\alpha) + \left(-2\,\beta+2\,\alpha\right)\sin(\alpha) + \cos(\beta)\right)Iresp\right) \quad (28)$$

```
> #cosine part
> vm_c1:=1/Pi*int(cos(theta)*Vm_M1,theta=0..alpha);
```

$$vm\_c1 := \frac{\sin(\alpha)\,Vin}{\pi} \quad (29)$$

```
> vm_c2:=1/Pi*int(cos(theta)*Vm_M2a,theta=alpha..beta);
```

$$vm\_c2 := -\frac{1}{4\,\pi\,\omega\,Cpfc}\left(4\,Cpfc\sin(\alpha)\,Vin\,\omega - 4\,Cpfc\sin(\beta)\,Vin\,\omega - 2\,Iresp\cos(\alpha)\,\alpha + 2\,Iresp\cos(\alpha)\,\beta + 3\,Iresp\sin(\alpha) - Iresp\sin(-2\,\beta+\alpha) - 4\,Iresp\sin(\beta)\right) \quad (30)$$

```
> vm_c3:=1/Pi*int(cos(theta)*Vm_M3a,theta=beta..Pi+alpha);
```

$$vm\_c3 := -\frac{\left(Vin\,\omega\,Cpfc - Iresp\cos(-\beta+\alpha) + Iresp\right)\left(\sin(\beta)+\sin(\alpha)\right)}{\pi\,\omega\,Cpfc} \quad (31)$$

```
> vm_c4:=1/Pi*int(cos(theta)*Vm_M4b,theta=Pi+alpha..Pi+beta);
```

$$vm\_c4 := \frac{1}{4\,\pi\,\omega\,Cpfc}\left(4\,Cpfc\sin(\alpha)\,Vin\,\omega - 4\,Cpfc\sin(\beta)\,Vin\,\omega + 2\,Iresp\cos(\alpha)\,\alpha - 2\,Iresp\cos(\alpha)\,\beta + 3\,Iresp\sin(\alpha) - 2\,Iresp\sin(2\,\alpha-\beta) - Iresp\sin(-2\,\beta+\alpha) - 2\,Iresp\sin(\beta)\right) \quad (32)$$

```
> vm_c5:=1/Pi*int(cos(theta)*Vm_M5,theta=Pi+beta..2*Pi);
```

$$vm\_c5 := \frac{\sin(\beta)\,Vin}{\pi} \quad (33)$$

```
> vm_c:=simplify(vm_c1+vm_c2+vm_c3+vm_c4+vm_c5);
```

$$vm\_c := \frac{1}{\pi\,\omega\,Cpfc}\left(Iresp\left(-\frac{\sin(2\,\alpha-\beta)}{2}+(\sin(\beta)+\sin(\alpha))\cos(-\beta+\alpha)+(-\beta+\alpha)\cos(\alpha)-\frac{\sin(\beta)}{2}-\sin(\alpha)\right)\right) \quad (34)$$

```
> #obtain equivalent impedance at node m
```

```
> vm_eq:=simplify(vm_c*I+vm_s);
```

$$vm\_eq := -\frac{1}{2\,\pi\,\omega\,Cpfc}\left((\cos(-2\,\beta+\alpha)+I\sin(-2\,\beta+\alpha)+(2\,I\beta-2\,I\alpha-1)\cos(\alpha)+(I+2\,\beta-2\,\alpha)\sin(\alpha))\,Iresp\right) \quad (35)$$

```
> # the equivalent voltage at node m is of the form vm_eq*sin
  (theta)
> # need to divide by the current Iresp*sin(theta-alpha)=Iresp*exp
  (-I*(theta-alpha))=Iresp*exp(-I*theta)*exp(-I*alpha)
> Zeq:=simplify(vm_eq/(Iresp*exp(-I*alpha)));
```

$$Zeq := -\frac{1}{2\,\pi\,\omega\,Cpfc}\left((\cos(-2\,\beta+\alpha)+I\sin(-2\,\beta+\alpha)+(2\,I\beta-2\,I\alpha-1)\cos(\alpha)+(I+2\,\beta-2\,\alpha)\sin(\alpha))\,e^{I\alpha}\right) \quad (36)$$

```
> s:=omega*I;
```

$$s := I\,\omega \quad (37)$$

```
> Zs:=s*Ls+1/(s*Cs);
```

$$Zs := I\,\omega\,Ls - \frac{I}{\omega\,Cs} \quad (38)$$

```
> Zp:=1/(1/Rl+s*Cp);
```

$$Zp := \frac{1}{\frac{1}{Rl}+I\,\omega\,Cp} \quad (39)$$

```
> Ztot:=Zs+Zp+Zeq;
```

$$Ztot := I\,\omega\,Ls - \frac{I}{\omega\,Cs} + \frac{1}{\frac{1}{Rl}+I\,\omega\,Cp} - \frac{1}{2\,\pi\,\omega\,Cpfc}\left((\cos(-2\,\beta+\alpha)+I\sin(-2\,\beta+\alpha)+(2\,I\beta-2\,I\alpha-1)\cos(\alpha)+(I+2\,\beta-2\,\alpha)\sin(\alpha))\,e^{I\alpha}\right) \quad (40)$$

```
>
> #resonant current Iresp=2/Pi*Vdc/Ztot
> eq300:= Iresp*exp(-I*alpha)=2/Pi*Vb/Ztot;
```

$$eq300 := Iresp\, e^{-I\alpha} = (2\ Vb) \Big/ \left(\pi \left(I\omega Ls - \frac{I}{\omega Cs} + \frac{1}{\frac{1}{Rl} + I\omega Cp} - \frac{1}{2\pi\omega Cpfc} \left((\cos(-2\beta + \alpha) + I\sin(-2\beta + \alpha) + (2I\beta - 2I\alpha - 1)\cos(\alpha) + (I + 2\beta - 2\alpha)\sin(\alpha) \right) e^{I\alpha} \right) \right) \right) \quad (41)$$

```
> eq301:= subs(eq101,eq300);
```

$$eq301 := Iresp\, e^{-I\alpha} = \left(2\ \left(Vin\,\omega\,Cpfc - Iresp\cos(-\beta + \alpha) + Iresp\right)\right) \Big/ \left(\pi\,\omega\,Cpfc \left(I\omega Ls - \frac{I}{\omega Cs} + \frac{1}{\frac{1}{Rl} + I\omega Cp} - \frac{1}{2\pi\omega Cpfc} \left((\cos(-2\beta + \alpha) + I\sin(-2\beta + \alpha) + (2I\beta - 2I\alpha - 1)\cos(\alpha) + (I + 2\beta - 2\alpha)\sin(\alpha) \right) e^{I\alpha} \right) \right) \right) \quad (42)$$

```
> #eq301 lhs is the signal definition of the resonant current
  Iresp*sin(theta-alpha)=Iresp*exp(-I*(theta+alpha)=Iresp*exp(-I*
  theta)*exp(-I*alpha)
>
> #eq301 rhs is the component based impedance which is 2/Pi*Vb*sin
  (theta)/Ztot=2/Pi*Vb*exp(I*theta)/Ztot
> #the exp(-I*theta) cancels and so has been omitted from the
  equation
> eq302:=Iresp=solve(eq301,Iresp);
```

$$\begin{aligned} eq302 := Iresp = -\,&(4\,Cpfc\,Cs\,Vin\,\omega\,(I\,Cp\,Rl\,\omega + 1)) \Big/ (4\,Cs - 2\,Cs\,e^{I\alpha}\sin(\alpha)\,e^{-I\alpha}\alpha \\ &+ 2\,Cs\,e^{I\alpha}\sin(\alpha)\,e^{-I\alpha}\beta - 4\,I\,Cp\,Cs\cos(-\beta + \alpha)\,Rl\,\omega - 2\,I\,Cs\,e^{I\alpha}e^{-I\alpha}\cos(\alpha)\,\alpha \\ &+ 2\,I\,Cs\,e^{I\alpha}e^{-I\alpha}\cos(\alpha)\,\beta - 2\,Cp\,Cpfc\,e^{-I\alpha}\pi\,Rl\,\omega - 2\,Cpfc\,Cs\,e^{-I\alpha}\pi\,Rl\,\omega \\ &- 2\,I\,Cpfc\,Cs\,Ls\,e^{-I\alpha}\pi\,\omega^2 - 4\,Cs\cos(-\beta + \alpha) - Cp\,Cs\,e^{I\alpha}e^{-I\alpha}\sin(-2\beta + \alpha)\,Rl\,\omega \\ &- Cp\,Cs\,e^{I\alpha}\sin(\alpha)\,e^{-I\alpha}\,Rl\,\omega - I\,Cp\,Cs\,e^{I\alpha}e^{-I\alpha}\cos(\alpha)\,Rl\,\omega + I\,Cp\,Cs\,e^{I\alpha}\cos(-2\beta \\ &+ \alpha)\,e^{-I\alpha}\,Rl\,\omega + Cs\,e^{I\alpha}\cos(-2\beta + \alpha)\,e^{-I\alpha} - Cs\,e^{I\alpha}e^{-I\alpha}\cos(\alpha) + 4\,I\,Cp\,Cs\,Rl\,\omega \\ &+ I\,Cs\,e^{I\alpha}\sin(\alpha)\,e^{-I\alpha} + I\,Cs\,e^{I\alpha}e^{-I\alpha}\sin(-2\beta + \alpha) + 2\,I\,Cpfc\,e^{-I\alpha}\pi \\ &+ 2\,Cp\,Cpfc\,Cs\,Ls\,e^{-I\alpha}\pi\,Rl\,\omega^3 + 2\,Cp\,Cs\,e^{I\alpha}e^{-I\alpha}\cos(\alpha)\,Rl\,\alpha\,\omega \\ &- 2\,Cp\,Cs\,e^{I\alpha}e^{-I\alpha}\cos(\alpha)\,Rl\,\beta\,\omega - 2\,I\,Cp\,Cs\,e^{I\alpha}\sin(\alpha)\,e^{-I\alpha}\,Rl\,\alpha\,\omega \\ &+ 2\,I\,Cp\,Cs\,e^{I\alpha}\sin(\alpha)\,e^{-I\alpha}\,Rl\,\beta\,\omega) \end{aligned} \quad (43)$$

```
> eq303:=evalc(abs(lhs(eq302))=abs(rhs(eq302))) assuming Cpfc>0,
  omega>0, alpha>0, beta>0, Cs>0, Ls>0, Cp>0, Cin>0, Rl>0, Vin>0,
  Iin>0;
```

$$eq303 := |Iresp| = \left(4\, Cpfc\, Cs\, Vin\, \omega \sqrt{Cp^2\, Rl^2\, \omega^2 + 1}\right) \Big/ \left(\left(4\, Cs - 4\, Cs \cos(-\beta + \alpha) - Cp\, Cs \sin(-2\,\beta + \alpha)\, Rl\, \omega \left(\cos(\alpha)^2 + \sin(\alpha)^2\right) - Cp\, Cs \sin(\alpha)\, Rl\, \omega \left(\cos(\alpha)^2 + \sin(\alpha)^2\right) - 2\, Cs \sin(\alpha)\, \alpha \left(\cos(\alpha)^2 + \sin(\alpha)^2\right) + 2\, Cs \sin(\alpha)\, \beta \left(\cos(\alpha)^2 + \sin(\alpha)^2\right) + Cs \cos(-2\,\beta + \alpha) \left(\cos(\alpha)^2 + \sin(\alpha)^2\right) - Cs \cos(\alpha) \left(\cos(\alpha)^2 + \sin(\alpha)^2\right) - 2\, Cp\, Cpfc\, \pi\, Rl\, \omega \cos(\alpha) - 2\, Cpfc\, Cs\, \pi\, Rl\, \omega \cos(\alpha) - 2\, Cp\, Cs \cos(\alpha)\, Rl\, \beta\, \omega \left(\cos(\alpha)^2 + \sin(\alpha)^2\right) + 2\, Cp\, Cs \cos(\alpha)\, Rl\, \alpha\, \omega \left(\cos(\alpha)^2 + \sin(\alpha)^2\right) + 2\, Cp\, Cpfc\, Cs\, Ls\, \pi\, Rl\, \omega^3 \cos(\alpha) - 2\, Cpfc\, Cs\, Ls\, \pi\, \omega^2 \sin(\alpha) + 2\, Cpfc\, \pi \sin(\alpha)\right)^2 + \left(2\, Cp\, Cpfc\, \pi\, Rl\, \omega \sin(\alpha) + 2\, Cpfc\, Cs\, \pi\, Rl\, \omega \sin(\alpha) - 2\, Cp\, Cpfc\, Cs\, Ls\, \pi\, Rl\, \omega^3 \sin(\alpha) - 2\, Cpfc\, Cs\, Ls\, \pi\, \omega^2 \cos(\alpha) + 4\, Cp\, Cs\, Rl\, \omega + Cs \sin(\alpha) \left(\cos(\alpha)^2 + \sin(\alpha)^2\right) + Cs \sin(-2\,\beta + \alpha) \left(\cos(\alpha)^2 + \sin(\alpha)^2\right) + 2\, Cpfc\, \pi \cos(\alpha) - 4\, Cp\, Cs \cos(-\beta + \alpha)\, Rl\, \omega - 2\, Cs \cos(\alpha)\, \alpha \left(\cos(\alpha)^2 + \sin(\alpha)^2\right) + 2\, Cs \cos(\alpha)\, \beta \left(\cos(\alpha)^2 + \sin(\alpha)^2\right) + Cp\, Cs \cos(-2\,\beta + \alpha)\, Rl\, \omega \left(\cos(\alpha)^2 + \sin(\alpha)^2\right) - Cp\, Cs \cos(\alpha)\, Rl\, \omega \left(\cos(\alpha)^2 + \sin(\alpha)^2\right) - 2\, Cp\, Cs \sin(\alpha)\, Rl\, \alpha\, \omega \left(\cos(\alpha)^2 + \sin(\alpha)^2\right) + 2\, Cp\, Cs \sin(\alpha)\, Rl\, \beta\, \omega \left(\cos(\alpha)^2 + \sin(\alpha)^2\right)\right)^2\right)^{1/2} \tag{44}$$

```
>
```

```
> # Simultaneous equation for an unknown angle obtained by equating
  current phase angle alpha to phase of the total equivalent
  impedance
> eq308:=simplify(evalc(tan(-alpha)*Re(1/Ztot)=Im(1/Ztot)));
```

$$eq308 := -\left(Cpfc\, \pi\, Cs^2\, \omega \left(-Cp^2\, Rl^2\, \omega^2 \sin(3\,\alpha - 2\,\beta) + Cp^2\, Rl^2\, \omega^2 \sin(-2\,\beta + \alpha) + 2\, Cp^2 \sin(\alpha)\, Rl^2\, \omega^2 + 4\, Cpfc \sin(\alpha)\, \pi\, Rl\, \omega - \sin(3\,\alpha - 2\,\beta) + \sin(-2\,\beta + \alpha) + 2 \sin(\alpha)\right)\right) \Big/ \left(-2 \left(\left(Cp^2\, Ls\, \pi\, Rl^2\, Cpfc\, \omega^4 + \left(-\pi \left(Cp\, Rl^2 - Ls\right) Cpfc - Cp^2\, Rl^2 \left(\beta - \alpha\right)\right) \omega^2 - \beta + \alpha\right) Cs - Cpfc\, \pi \left(Cp^2\, Rl^2\, \omega^2 + 1\right)\right) Cs \sin(3\,\alpha - 2\,\beta) - Cs^2 \left(Cp^2\, Rl^2\, \omega^2 + 2\, Rl\, \pi\, \omega\, Cpfc + 1\right) \cos(3\,\alpha - 2\,\beta) - 2 \left(\left(Cp^2\, Ls\, \pi\, Rl^2\, Cpfc\, \omega^4 + \left(-\pi \left(Cp\, Rl^2 - Ls\right) Cpfc - Cp^2\, Rl^2 \left(\beta - \alpha\right)\right) \omega^2 - \beta + \alpha\right) Cs - Cpfc\, \pi \left(Cp^2\, Rl^2\, \omega^2 + 1\right)\right) Cs \sin(-2\,\beta \tag{45}$$

$$+\alpha) - Cs^2\left(Cp^2 Rl^2\omega^2 + 2\,Rl\,\pi\,\omega\,Cpfc + 1\right)\cos(-2\beta+\alpha)$$
$$+ 4\cos(\alpha)\left(\left(Cp^2 Ls^2\pi^2 Rl^2 Cpfc^2\omega^6 - 2\,Cpfc\,\pi\,Ls\left(\pi\left(Cp\,Rl^2 - \frac{Ls}{2}\right)Cpfc + Cp^2 Rl^2(\beta\right.\right.\right.$$
$$\left.\left.\left.-\alpha)\right)\omega^4 + \left(\pi^2 Rl^2 Cpfc^2 + 2\,\pi(\beta-\alpha)\left(Cp\,Rl^2 - Ls\right)Cpfc + Cp^2 Rl^2\left(\frac{1}{2} - 2\beta\alpha + \beta^2\right.\right.\right.$$
$$\left.\left.\left.+\alpha^2\right)\right)\omega^2 + Rl\,\pi\,\omega\,Cpfc + \frac{1}{2} - 2\beta\alpha + \beta^2 + \alpha^2\right)Cs^2 - 2\left(Cp^2 Ls\,\pi\,Rl^2 Cpfc\,\omega^4 + (\right.$$
$$\left.-\pi\left(Cp\,Rl^2 - Ls\right)Cpfc - Cp^2 Rl^2(\beta-\alpha)\right)\omega^2 - \beta + \alpha\right)Cpfc\,\pi\,Cs + \pi^2 Cpfc^2\left(Cp^2 Rl^2\omega^2\right.$$
$$\left.+1\right)\Big)\Big) = -\Big(\left(Cs\sin(-2\beta+2\alpha)\left(Cp^2 Rl^2\omega^2+1\right) + \left(-2\,Cp^2 Ls\,\pi\,Rl^2 Cpfc\,\omega^4\right.\right.$$
$$\left.\left.+\left(2\,\pi\left(Cp\,Rl^2 - Ls\right)Cpfc + 2\,Cp^2 Rl^2(\beta-\alpha)\right)\omega^2 + 2\beta - 2\alpha\right)Cs\right.$$
$$\left.+ 2\,Cpfc\,\pi\left(Cp^2 Rl^2\omega^2+1\right)\right)\omega\,Cs\,Cpfc\,\pi\Big) \Big/ \Big(2\left(\left(Cp^2 Ls\,\pi\,Rl^2 Cpfc\,\omega^4 + \left(-\pi\left(Cp\,Rl^2\right.\right.\right.\right.$$
$$\left.\left.\left.\left.-Ls\right)Cpfc - Cp^2 Rl^2(\beta-\alpha)\right)\omega^2 - \beta + \alpha\right)Cs - Cpfc\,\pi\left(Cp^2 Rl^2\omega^2+1\right)\right)Cs\sin(-2\beta$$
$$+2\alpha) + Cs^2\left(Cp^2 Rl^2\omega^2 + 2\,Rl\,\pi\,\omega\,Cpfc + 1\right)\cos(-2\beta+2\alpha) + \Big($$
$$-2\,Cp^2 Ls^2\pi^2 Rl^2 Cpfc^2\omega^6 + 4\,Cpfc\,\pi\,Ls\left(\pi\left(Cp\,Rl^2 - \frac{Ls}{2}\right)Cpfc + Cp^2 Rl^2(\beta-\alpha)\right)\omega^4$$
$$+\left(-2\pi^2 Rl^2 Cpfc^2 - 4\,\pi(\beta-\alpha)\left(Cp\,Rl^2 - Ls\right)Cpfc - 2\,Cp^2 Rl^2\left(\frac{1}{2} - 2\beta\alpha + \beta^2\right.\right.$$
$$\left.\left.+\alpha^2\right)\right)\omega^2 - 2\,Rl\,\pi\,\omega\,Cpfc - 2\beta^2 + 4\beta\alpha - 2\alpha^2 - 1\Big)Cs^2 + 4\left(Cp^2 Ls\,\pi\,Rl^2 Cpfc\,\omega^4 + (\right.$$
$$\left.-\pi\left(Cp\,Rl^2 - Ls\right)Cpfc - Cp^2 Rl^2(\beta-\alpha)\right)\omega^2 - \beta + \alpha\right)Cpfc\,\pi\,Cs - 2\,\pi^2 Cpfc^2\left(Cp^2 Rl^2\omega^2\right.$$
$$\left.+1\right)\Big)$$

```
> # Use energy balance Ein=Eout to obtain one simultaneous equation
  for an unknown angle
> # Output energy
> eq1000:=Vout=Voutp*sin(omega*t);
```

$$eq1000 := Vout = Voutp\sin(\omega t) \tag{46}$$

```
> eq1001:=subs(eq1000,Vout^2/Rl);
```

$$eq1001 := \frac{Voutp^2\sin(\omega t)^2}{Rl} \tag{47}$$

```
> eq1002:=int(eq1001,t=0..1/fs);
```

$$eq1002 := -\frac{Voutp^2\left(\cos\left(\frac{\omega}{fs}\right)\sin\left(\frac{\omega}{fs}\right)fs - \omega\right)}{2\,Rl\,\omega\,fs} \tag{48}$$

```
> eq1003:=subs(fs=omega/(2*Pi),eq1002);
```

$$eq1003 := -\frac{Voutp^2 \left(\frac{\cos(2\pi)\sin(2\pi)\,\omega}{2\pi} - \omega \right) \pi}{Rl\,\omega^2} \tag{49}$$

```
> eq1004:=simplify(eq1003);
```

$$eq1004 := \frac{Voutp^2\,\pi}{\omega\,Rl} \tag{50}$$

```
> eq1005:=evalc(subs(Voutp=Iresp*abs(1/(1/Rl+(s*Cp))),eq1004));
```

$$eq1005 := \frac{Iresp^2\,\pi}{\left(\frac{1}{Rl^2} + \omega^2\,Cp^2 \right) \omega\,Rl} \tag{51}$$

```
> Eout1:=subs(Iresp2=rhs(eq303),eq1005):

> # Input energy
> # current only flows from input during mode 1
> Ein:=1/omega*Vin*(int(-Iresp,theta=0..alpha)+int(-Iresp,theta=Pi+
  beta..2*Pi));
```

$$Ein := \frac{Vin\,(-Iresp\,\alpha - Iresp\,(\pi - \beta))}{\omega} \tag{52}$$

```
> Ein1:=subs(Iresp2=rhs(eq303),Ein):

> eq400:=Eout1=Ein1:

> simeq1:=lhs(eq400)-rhs(eq400)=0;
```

$$simeq1 := \frac{Iresp^2\,\pi}{\left(\frac{1}{Rl^2} + \omega^2\,Cp^2 \right) \omega\,Rl} - \frac{Vin\,(-Iresp\,\alpha - Iresp\,(\pi - \beta))}{\omega} = 0 \tag{53}$$

```
> simeq2:=lhs(eq308)-rhs(eq308)=0;
```

$$\begin{aligned} simeq2 := & -(Cpfc\,\pi\,Cs^2\,\omega\,(-Cp^2\,Rl^2\,\omega^2\sin(3\alpha - 2\beta) + Cp^2\,Rl^2\,\omega^2\sin(-2\beta + \alpha) \\ & + 2\,Cp^2\sin(\alpha)\,Rl^2\,\omega^2 + 4\,Cpfc\sin(\alpha)\,\pi\,Rl\,\omega - \sin(3\alpha - 2\beta) + \sin(-2\beta + \alpha) \\ & + 2\sin(\alpha))) \Big/ \left(-2\,((Cp^2\,Ls\,\pi\,Rl^2\,Cpfc\,\omega^4 + (-\pi\,(Cp\,Rl^2 - Ls)\,Cpfc - Cp^2\,Rl^2\,(\beta \right. \\ & - \alpha))\,\omega^2 - \beta + \alpha)\,Cs - Cpfc\,\pi\,(Cp^2\,Rl^2\,\omega^2 + 1))\,Cs\sin(3\alpha - 2\beta) - Cs^2\,(Cp^2\,Rl^2\,\omega^2 \\ & \left. + 2\,Rl\,\pi\,\omega\,Cpfc + 1)\cos(3\alpha - 2\beta) - 2\,((Cp^2\,Ls\,\pi\,Rl^2\,Cpfc\,\omega^4 + (-\pi\,(Cp\,Rl^2 \right. \end{aligned} \tag{54}$$

$$-Ls)\,Cpfc-Cp^2\,Rl^2\,(\beta-\alpha))\,\omega^2-\beta+\alpha)\,Cs-Cpfc\,\pi\,(Cp^2\,Rl^2\,\omega^2+1))\,Cs\sin(-2\,\beta$$

$$+\alpha)-Cs^2\,(Cp^2\,Rl^2\,\omega^2+2\,Rl\,\pi\,\omega\,Cpfc+1)\cos(-2\,\beta+\alpha)$$

$$+4\cos(\alpha)\left(\left(Cp^2\,Ls^2\,\pi^2\,Rl^2\,Cpfc^2\,\omega^6-2\,Cpfc\,\pi\,Ls\left(\pi\left(Cp\,Rl^2-\frac{Ls}{2}\right)Cpfc+Cp^2\,Rl^2\,(\beta\right.\right.\right.$$

$$-\alpha)\Big)\,\omega^4+\left(\pi^2\,Rl^2\,Cpfc^2+2\,\pi\,(\beta-\alpha)\,(Cp\,Rl^2-Ls)\,Cpfc+Cp^2\,Rl^2\left(\frac{1}{2}-2\,\beta\,\alpha+\beta^2\right.\right.$$

$$\left.\left.+\alpha^2\right)\right)\omega^2+Rl\,\pi\,\omega\,Cpfc+\frac{1}{2}-2\,\beta\,\alpha+\beta^2+\alpha^2\Big)\,Cs^2-2\,(Cp^2\,Ls\,\pi\,Rl^2\,Cpfc\,\omega^4+($$

$$-\pi\,(Cp\,Rl^2-Ls)\,Cpfc-Cp^2\,Rl^2\,(\beta-\alpha))\,\omega^2-\beta+\alpha)\,Cpfc\,\pi\,Cs+\pi^2\,Cpfc^2\,(Cp^2\,Rl^2\,\omega^2$$

$$+1)))+((Cs\sin(-2\,\beta+2\,\alpha)\,(Cp^2\,Rl^2\,\omega^2+1)+(-2\,Cp^2\,Ls\,\pi\,Rl^2\,Cpfc\,\omega^4$$

$$+(2\,\pi\,(Cp\,Rl^2-Ls)\,Cpfc+2\,Cp^2\,Rl^2\,(\beta-\alpha))\,\omega^2+2\,\beta-2\,\alpha)\,Cs$$

$$+2\,Cpfc\,\pi\,(Cp^2\,Rl^2\,\omega^2+1))\,\omega\,Cs\,Cpfc\,\pi)\Big/\Big(2\,((Cp^2\,Ls\,\pi\,Rl^2\,Cpfc\,\omega^4+(-\pi\,(Cp\,Rl^2$$

$$-Ls)\,Cpfc-Cp^2\,Rl^2\,(\beta-\alpha))\,\omega^2-\beta+\alpha)\,Cs-Cpfc\,\pi\,(Cp^2\,Rl^2\,\omega^2+1))\,Cs\sin(-2\,\beta$$

$$+2\,\alpha)+Cs^2\,(Cp^2\,Rl^2\,\omega^2+2\,Rl\,\pi\,\omega\,Cpfc+1)\cos(-2\,\beta+2\,\alpha)+\Big($$

$$-2\,Cp^2\,Ls^2\,\pi^2\,Rl^2\,Cpfc^2\,\omega^6+4\,Cpfc\,\pi\,Ls\left(\pi\left(Cp\,Rl^2-\frac{Ls}{2}\right)Cpfc+Cp^2\,Rl^2\,(\beta-\alpha)\right)\omega^4$$

$$+\left(-2\,\pi^2\,Rl^2\,Cpfc^2-4\,\pi\,(\beta-\alpha)\,(Cp\,Rl^2-Ls)\,Cpfc-2\,Cp^2\,Rl^2\left(\frac{1}{2}-2\,\beta\,\alpha+\beta^2\right.\right.$$

$$\left.\left.+\alpha^2\right)\right)\omega^2-2\,Rl\,\pi\,\omega\,Cpfc-2\,\beta^2+4\,\beta\,\alpha-2\,\alpha^2-1\Big)\,Cs^2+4\,(Cp^2\,Ls\,\pi\,Rl^2\,Cpfc\,\omega^4+($$

$$-\pi\,(Cp\,Rl^2-Ls)\,Cpfc-Cp^2\,Rl^2\,(\beta-\alpha))\,\omega^2-\beta+\alpha)\,Cpfc\,\pi\,Cs-2\,\pi^2\,Cpfc^2\,(Cp^2\,Rl^2\,\omega^2$$

$$+1))=0$$

```
> # This section is for testing the mathematical model. The
  information that are defined below are extracted from simulation
  model to compare the results of the maple model to simulation
  results.
> fs:=116e3;ta:=1.509e-6;Iresp:=902.4e-3;Vin:=100;tb:=3.815e-6;
  omega:=2*Pi*fs;Cpfc:=100e-9;
```

$$fs := 116000.$$

$$ta := 1.509 \times 10^{-6}$$

$$Iresp := 0.9024$$

$$Vin := 100$$

$$tb := 3.815 \times 10^{-6}$$

$$\omega := 728849.4958$$

$$Cpfc := 1.00 \times 10^{-7} \quad (55)$$

```
> Ls:=1.69e-3;Cs:=1.19e-9;Cp:=2.475e-9/16;Rl:=500/16;
```

$$Ls := 0.00169$$

$$Cs := 1.19 \times 10^{-9}$$

$$Cp := 1.546875000 \times 10^{-10}$$

$$Rl := \frac{125}{4} \quad (56)$$

```
> N:=1;Cout:=Cp;
```

$$N := 1$$

$$Cout := 1.546875000 \times 10^{-10} \quad (57)$$

```
> with(Optimization);
```

$$[ImportMPS, Interactive, LPSolve, LSSolve, Maximize, Minimize, NLPSolve, QPSolve] \quad (58)$$

```
> rute:=NLPSolve(lhs(simeq1)^2+lhs(simeq2)^2, alpha = 0.01 .. Pi,
  beta = 0.01 .. Pi, initialpoint = {alpha = 1, beta = 3});
```

$$rute := [6.037907952717138 57 \times 10^{-8}, [\alpha = 1.09870478950824, \beta = 3.14159265358979]] \quad (59)$$

```
> rute:=fsolve({simeq1,simeq2},{alpha=0.5,beta=3},fulldigits);
```

$$rute := \{\alpha = 1.079057601, \beta = 5.106568385\} \quad (60)$$

```
> evalf(subs(eq303,eq101)):
> evalf(subs(rute,%));
```

$$Vb = 120.2132128 \quad (61)$$

```
> eq2000:=evalf(subs(rute,eq303));
```

$$eq2000 := 0.9024 = 1.107687055 \quad (62)$$

```
> evalf(subs(Iresp2=rhs(eq2000),Eout*fs));
```

$$116000.\ Eout \quad (63)$$

```
> Vout:=subs(Iresp2=rhs(eq2000),Iin*abs(1/(1/Rl+(s*Cp))));
```

$$Vout := 31.24980604\ Iin \quad (64)$$

```
> Pout:=Vout^2/2/Rl;
```

$$Pout := 15.62480604\ Iin^2 \quad (65)$$

```
>
>
```

Appendix 2. The MATLAB mode extractor software

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%
%this code extract the modes of operation of the CSCP-PFC
%system based on the given conduction state data from
%either simulation or practical results. It checks the
%present modes of operation against user defined modes of
%operation.
%In this section the imported raw data from LTspice simulation
are checked
%and verified. There are 6 for loops, one for each component.
This section
%checks every data point and if it is not valid(0or1, it will
assign a
%valid value based on the value of the data point.

L = length(Vid1)

for r = 1:L



    if Vid1(r)== 1 |  Vid1(r)== 0


    else
        if Vid1(r)>0.5
        Vid1(r)= 1;
        else
        Vid1(r)= 0;
        end
    end
end

L = length(Vid2)

for r = 1:L

    if Vid2(r)== 1 |  Vid2(r)== 0


    else
        if Vid2(r)>0.5
```

```
        Vid2(r)= 1;
        else
        Vid2(r)= 0;
        end;
    end
end

L = length(Vid3)

for r = 1:L

    if Vid3(r)== 1 |  Vid3(r)== 0


    else
        if Vid3(r)>0.5
        Vid3(r)= 1;
        else
        Vid3(r)= 0;
        end
    end
end


L = length(Vid4)

for r = 1:L

    if Vid4(r)== 1 |  Vid4(r)== 0


    else
        if Vid4(r)>0.5
        Vid4(r)= 1;
        else
        Vid4(r)= 0;
        end
    end
end


L = length(Vis1)

for r = 1:L

    if Vis1(r)== 1 |  Vis1(r)== 0


    else
        if Vis1(r)>0.5
        Vis1(r)= 1;
```

```
        else
        Vis1(r)= 0;
        end;
    end
end


L = length(Vis2)

for r = 1:L

    if Vis2(r)== 1 |  Vis2(r)== 0


    else
        if Vis2(r)>0.5
        Vis2(r)= 1;
        else
        Vis2(r)= 0;
        end
    end
end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%
%This section combines the 6 conduction state data from
previous section to
%create array of bit-pattern data that demonstrates the
conduction state of
%the whole system using only one bit-pattern number

m = (Vid1*2)+(Vid2*4)+(Vid3*8)+(Vid4*16)+(Vis1*32)+(Vis2*64);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%
%This section checks the duration of eeach mode against an
arbitrary
%threshold if the the duration of the mode is less than the
threshold it
%removes that mode and assigns the old value
%the purpos of this section is to remove any spurious modes
that are
%present

threshold = 6;
```

```
index=2;

for a=2:length(m)                                          %This for
loop checks modes and the modes that have length of less

    if (m(a)~=m(a-1))

        %Was a change sufficiently recent?
        if ((a-index)<threshold)
            % Then maintain old value
            m(index:a)=m(index-1);
        end
        index=a;
    end
end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%
%This section only capture the changes in the data array m
into data array
%d. therefore, the first data of each mode (or Bit-pattern
duration) is
%captured. Morover, this section capture the time of each
change so it can
%be analysed with respect to other circuit parameters.

clear d
d(1) = m(1);
i=1;
j = 1;


for r = 1:length(m)


    if d(j) == m(r)

     else
       j=j+1;
     d(j)= m(r);
     t(j)= time(r);

     end
end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%
%this section uses another alogrithm to capture the changes
and the
```

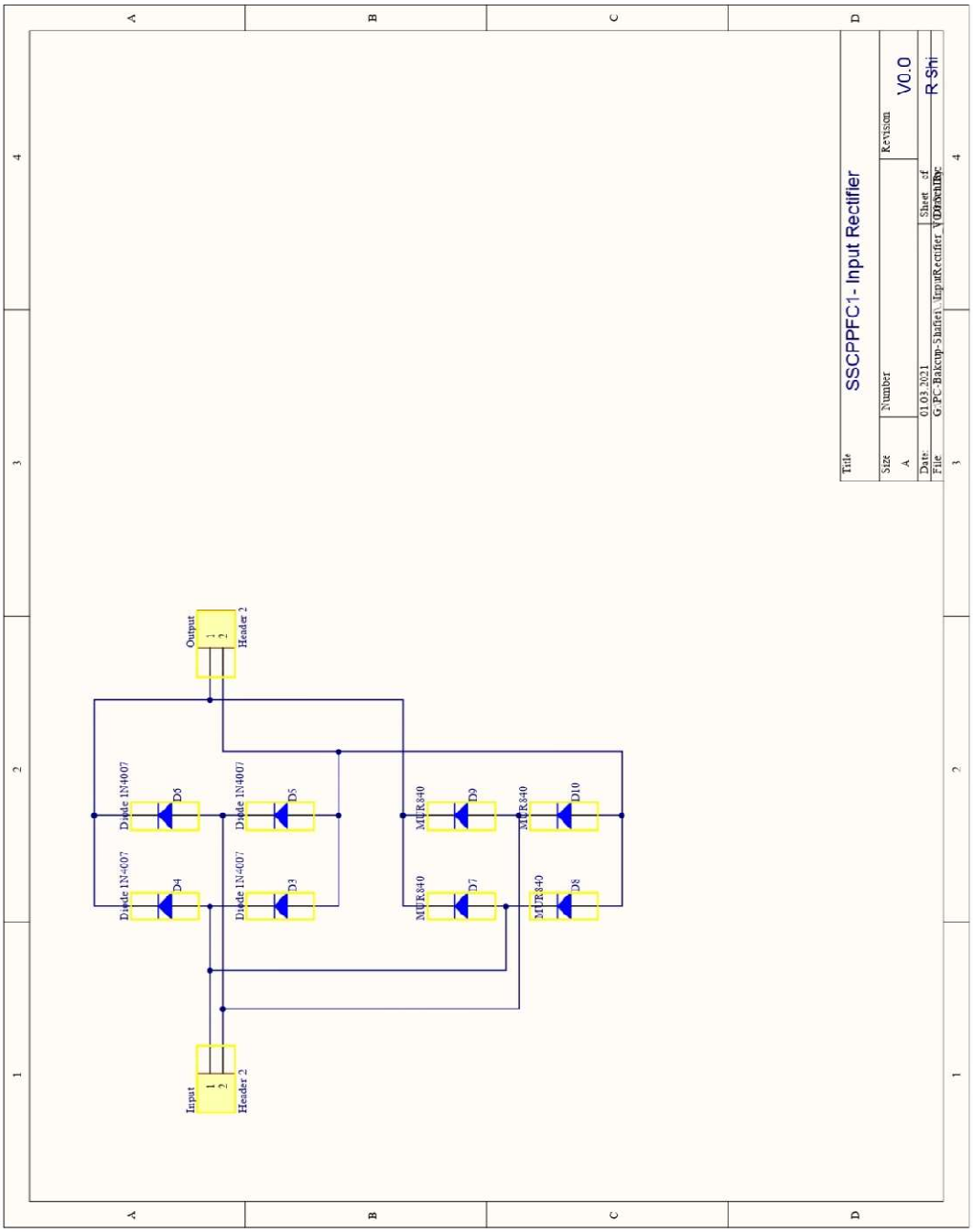
```
%operation of this section and the previous section are
identical.

d2=m(diff(m)~=0);
d2 = d2';
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%
%This section is a switch case it checks the data point of the
array d and
%compares it to the bit pattern sequence defined by the user.
if the modes
%of operation are as expected the new data array(d3) will have
values of
%1,2,3,4,5,6,1,2,3,4,5,6 and if the data point in array d is
not any of the
%user defined sequence it will output -1.

for r = 1: length (d2)

    n = d(r);
     switch n
         case 64
                     d3(r) = 1;
         case 66
                     d3(r) = 2;
         case 10
                     d3(r) = 3;
         case 32
                     d3(r) = 4;
         case 36
                     d3(r) = 5 ;
         case 20
                     d3(r) = 6;
         otherwise

                     d3(r) = -10 ;
     end

end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%
%This section check the data in the array d3 from previous
section if the
%expected mode of operation that is defined by the user is
present in the
%data(which is 1,2,3,4,5,6, and it repeats again from 1) it
outputs 1 in
```

```
%the array modes. If the user defined modes of operation is
not present it
%will assign zero in the array modes for that data point.



r = 1
while  r < length(d3);

    if d3(r)==1

        modes(r) = 1;
        r=r+1
        if d3(r)==2

            modes(r)=1;
            r=r+1;

            if d3(r)==3;

                modes(r)=1;
                r=r+1;

                if d3(r)==4;

                    modes(r)=1;
                    r=r+1;

                    if d3(r)==5;

                        modes(r)=1;
                        r=r+1;

                        if d3(r)==6

                            modes(r)=1;
                            r= r+1

                        else
                        modes(r)=0;
                        r= r+1
                    end
                else
                    modes(r)=0;
                    r= r+1
                end
            else
                modes(r)=0;
                r= r+1
                end
            else
```

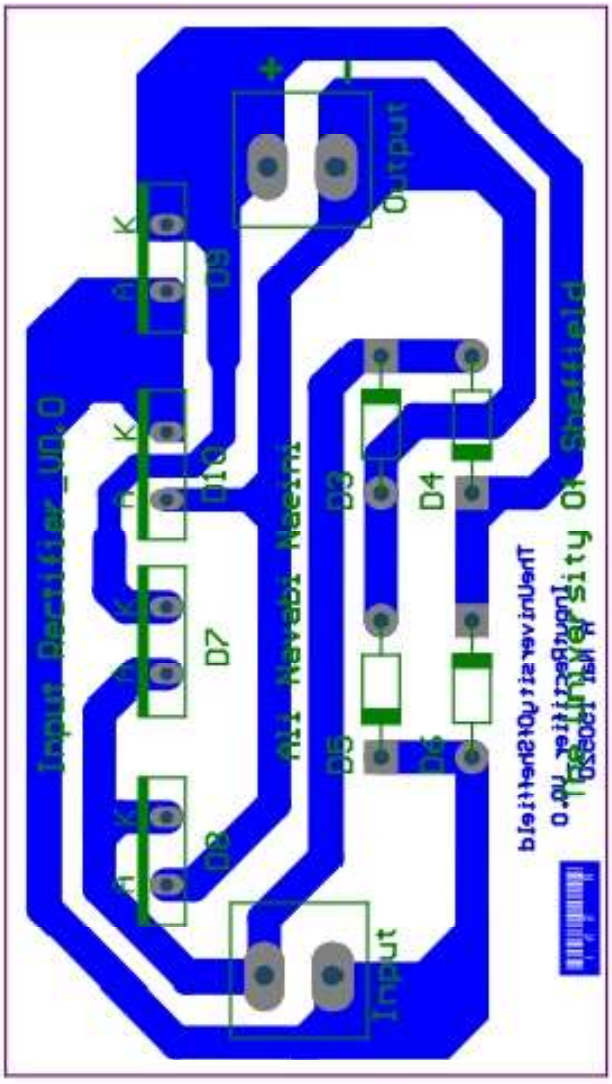
```
                modes(r)=0;
               r= r+1
             end
         else
             modes(r)=0;
             r= r+1
         end
     else
         modes(r)=0;
         r= r+1
     end
end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%
```

Appendix 3. The schematics and PCB diagrams of the practical platform

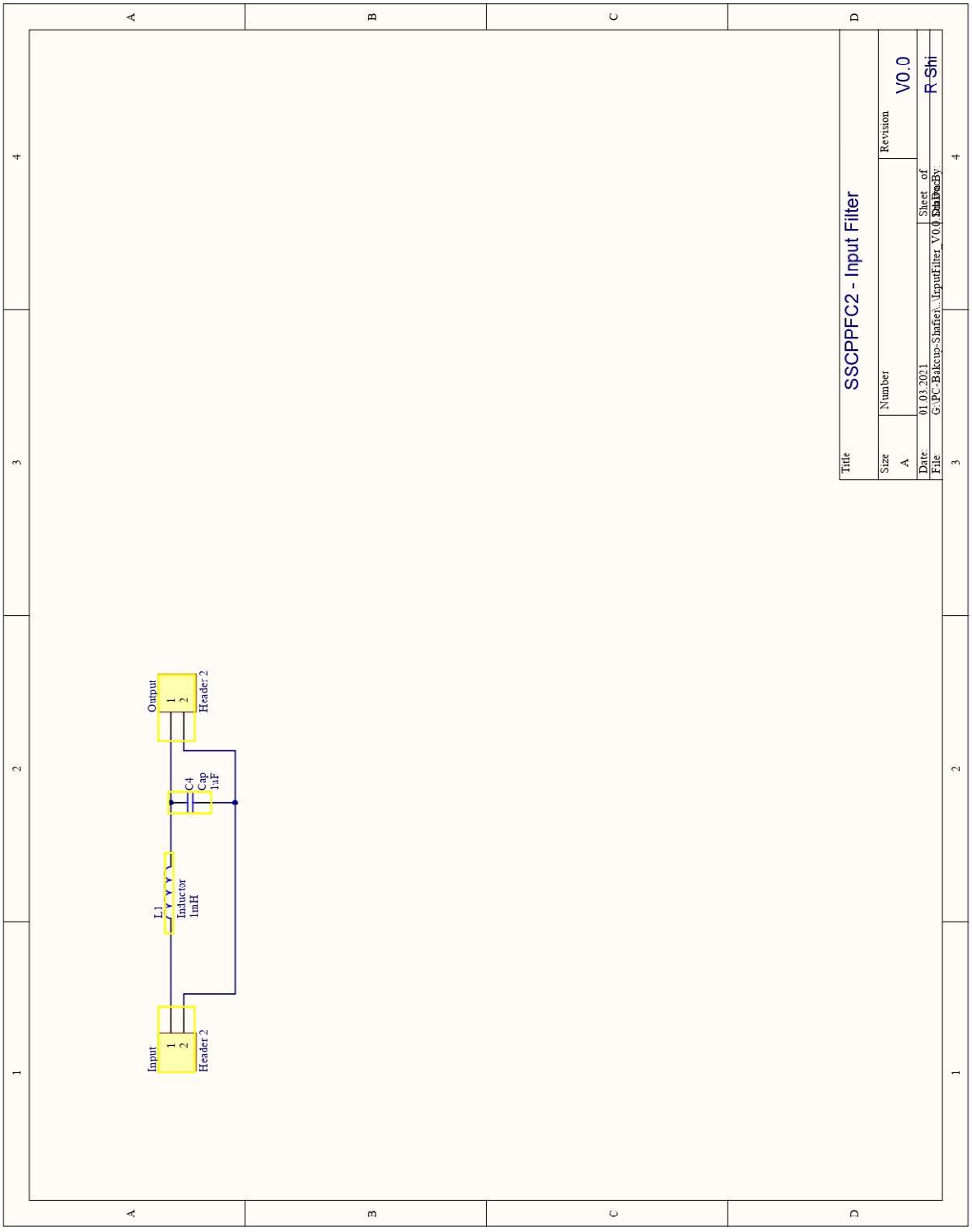
The schematic of the input rectifier



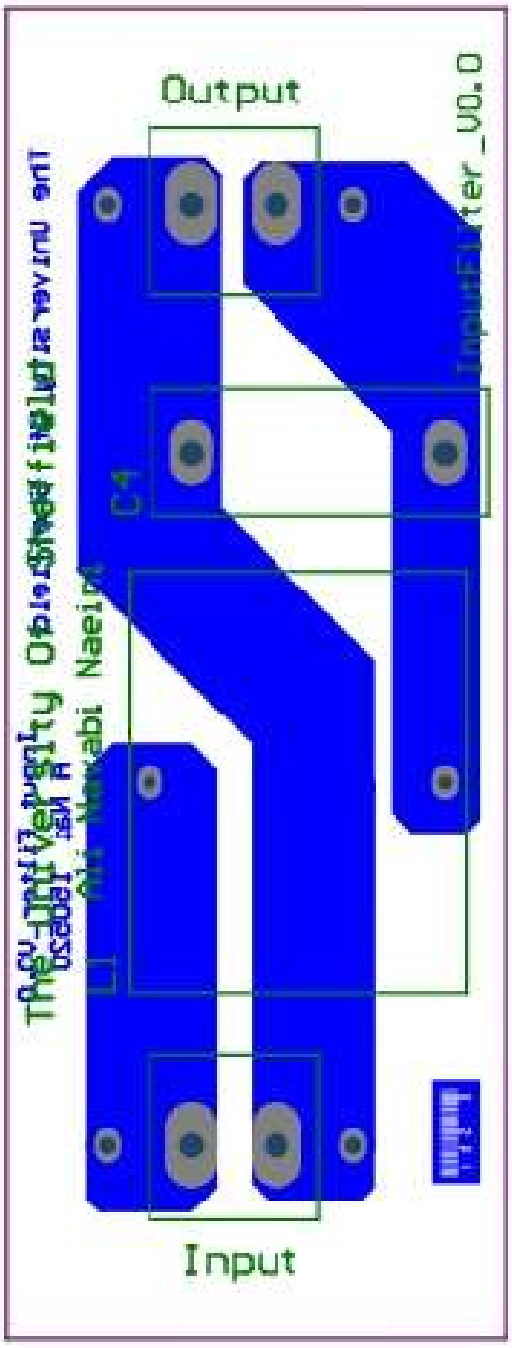
The PCB diagram of the input rectifier



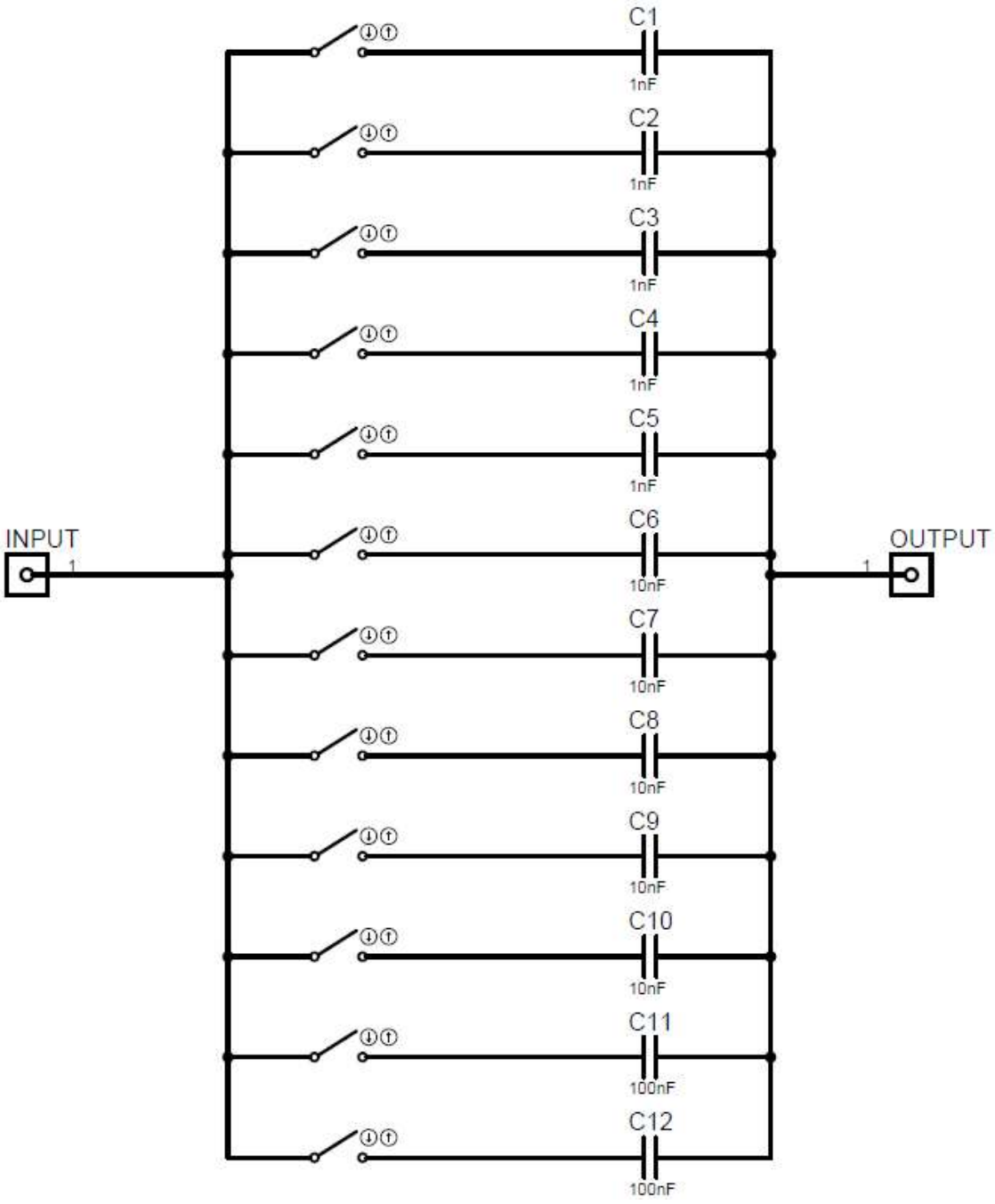
The schematic of the input LC filter



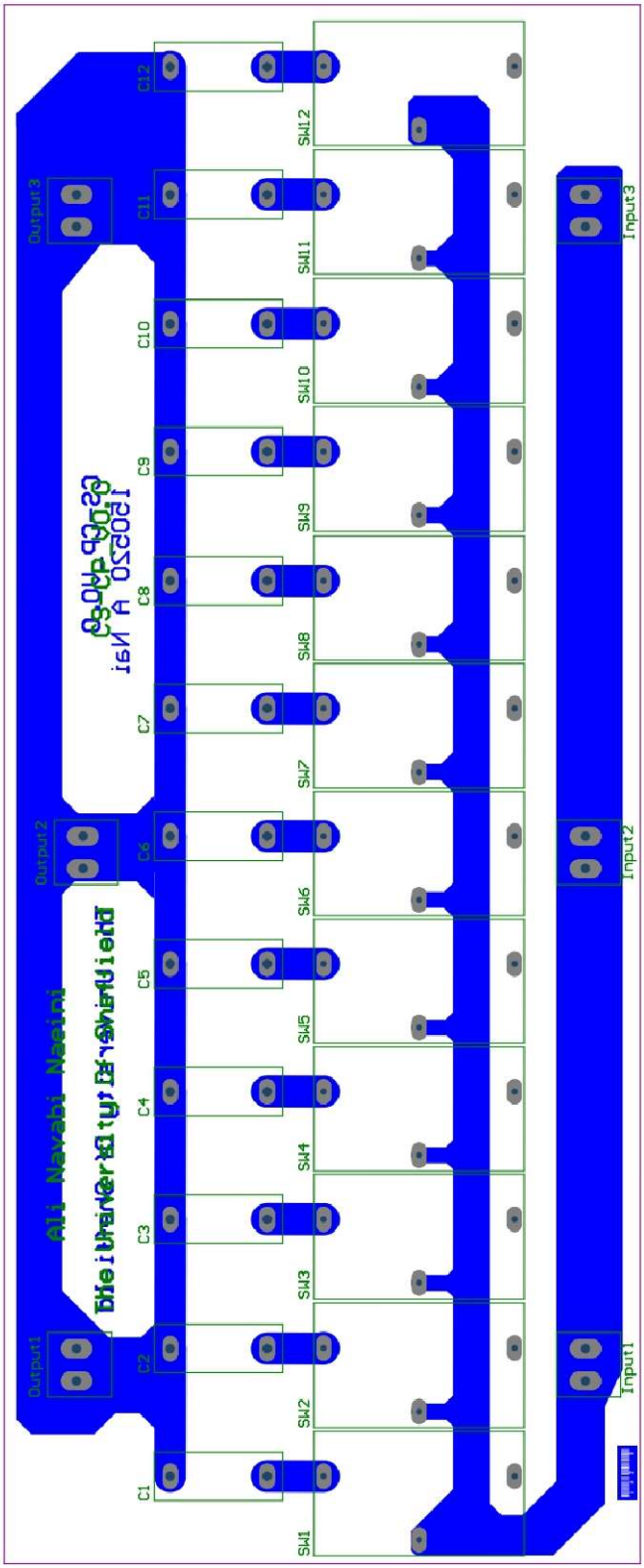
The PCB diagram of the input LC filter



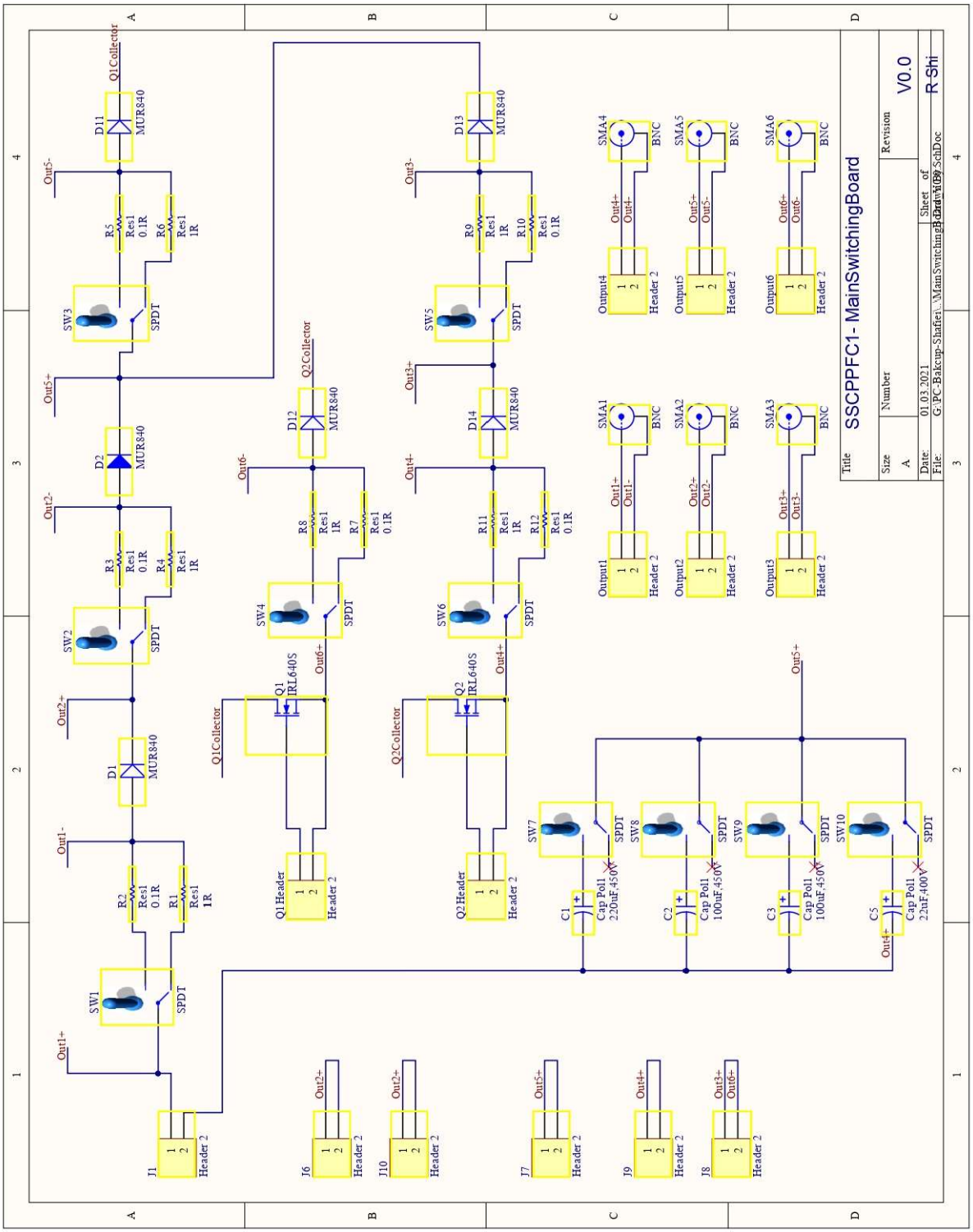
The schematic of the capacitor board



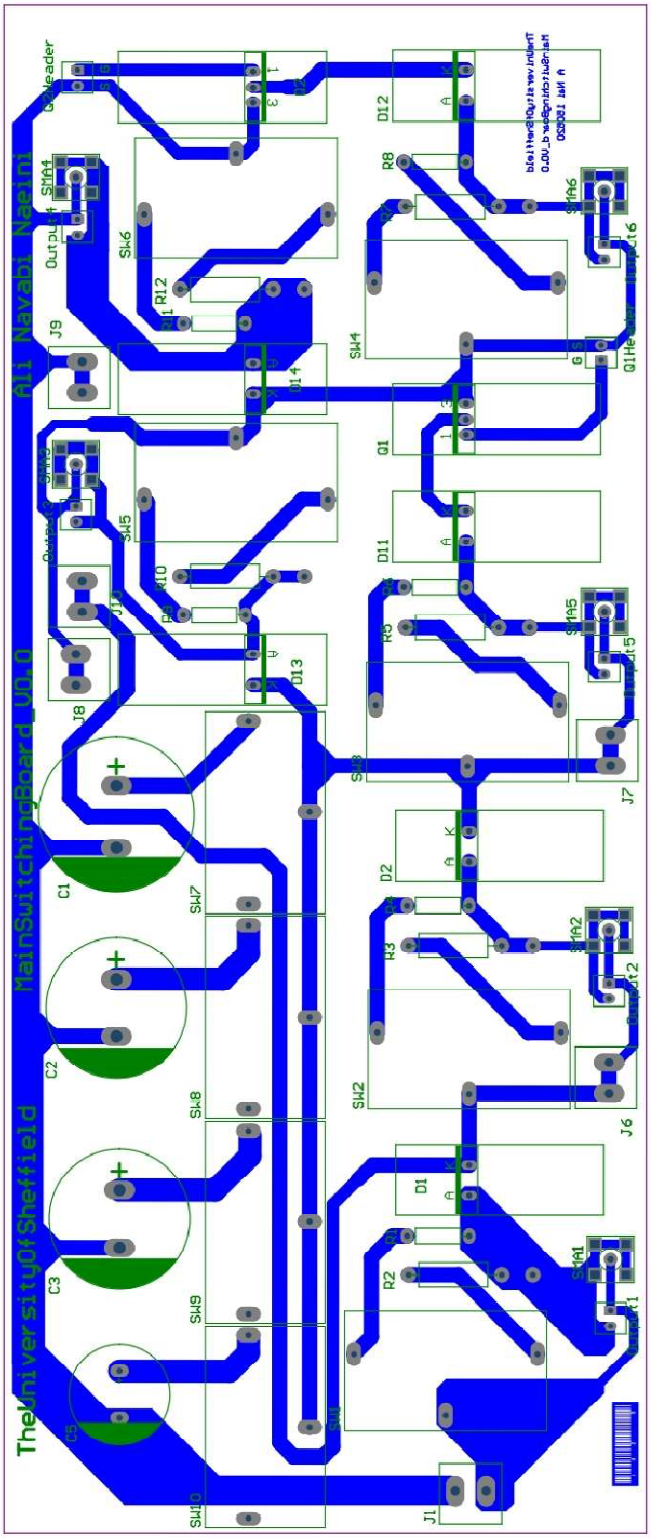
The PCB diagram of the capacitor board



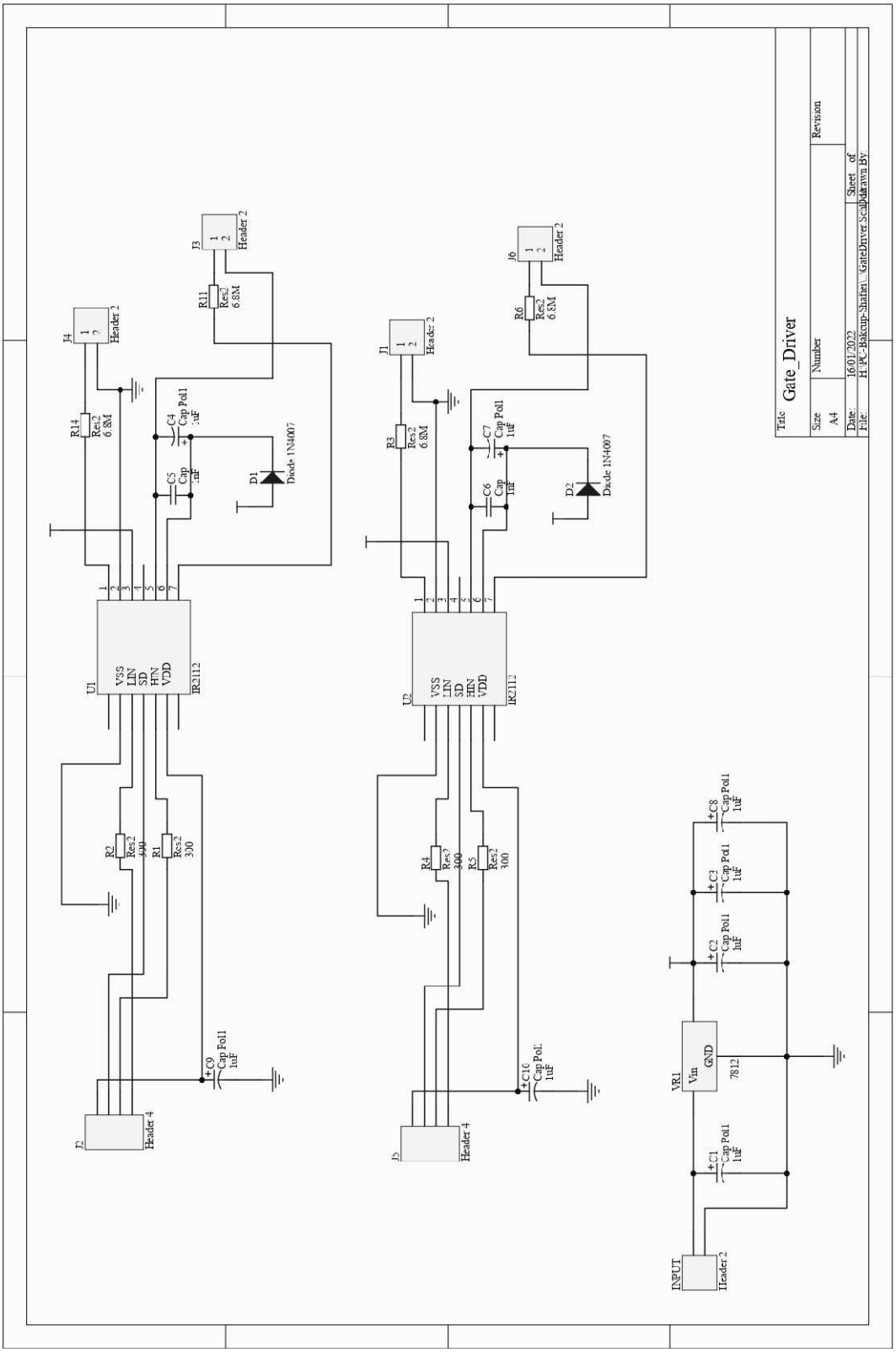
The schematic of the main switch board



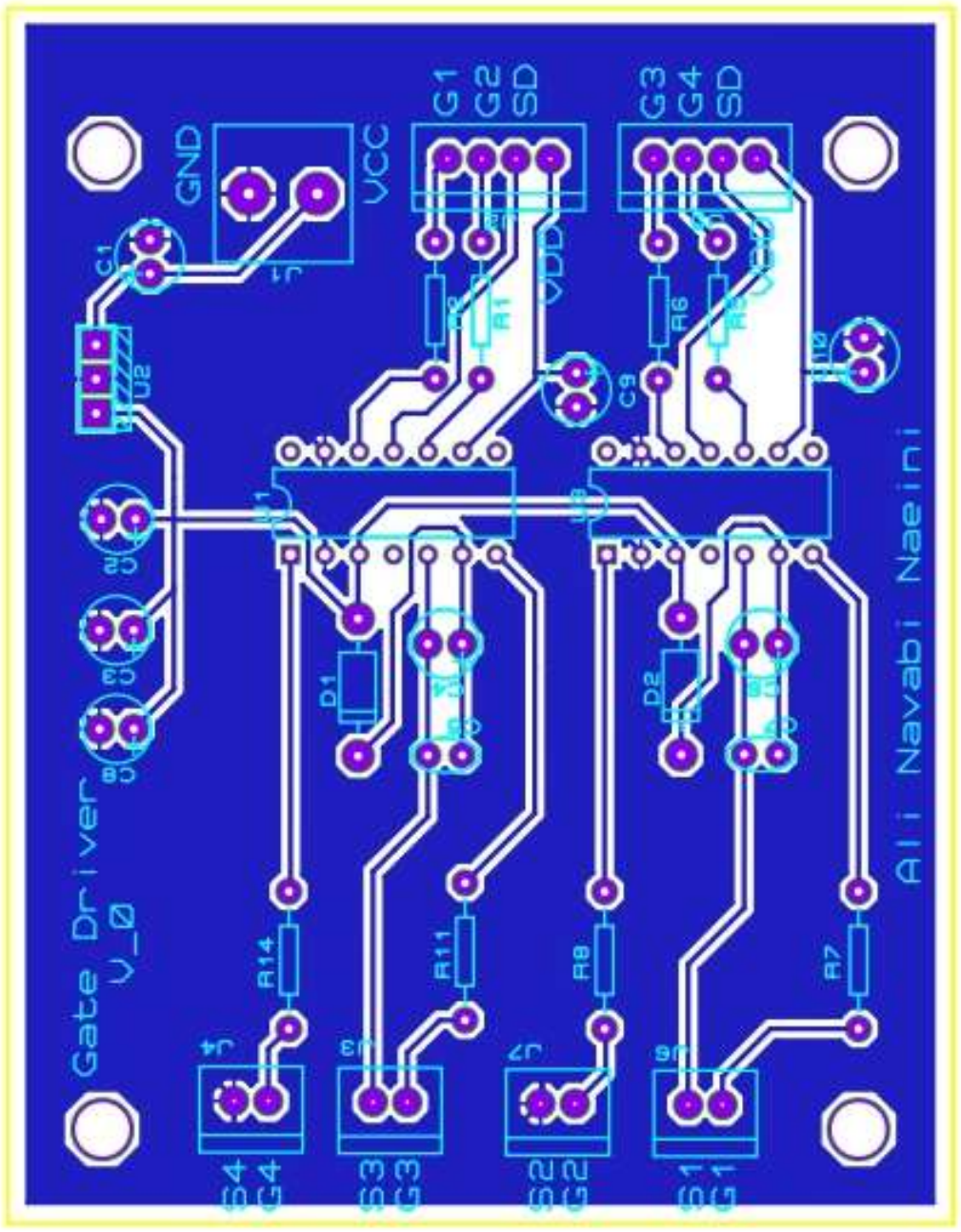
The PCB diagram of the main switch board



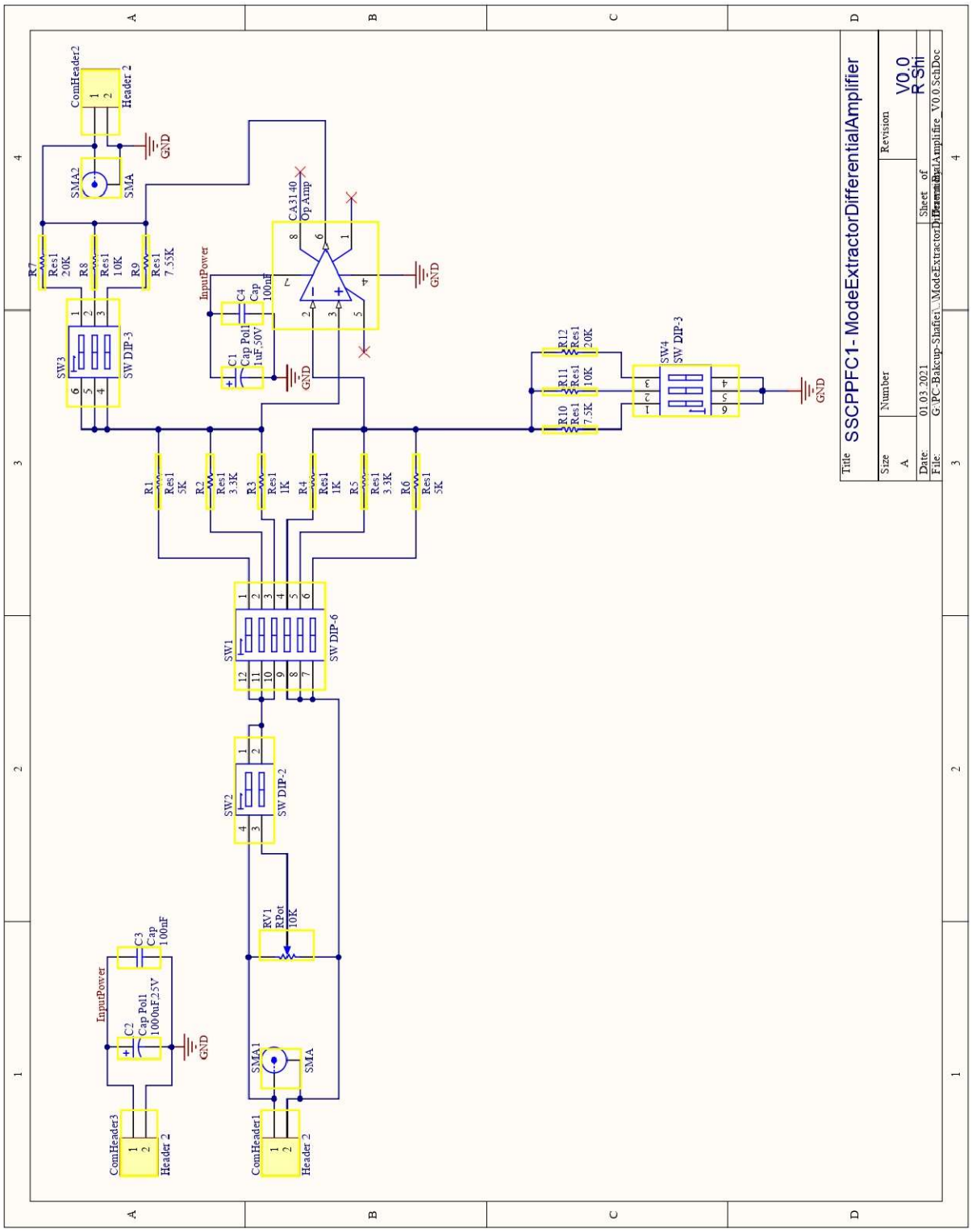
The schematic of the gate driver board



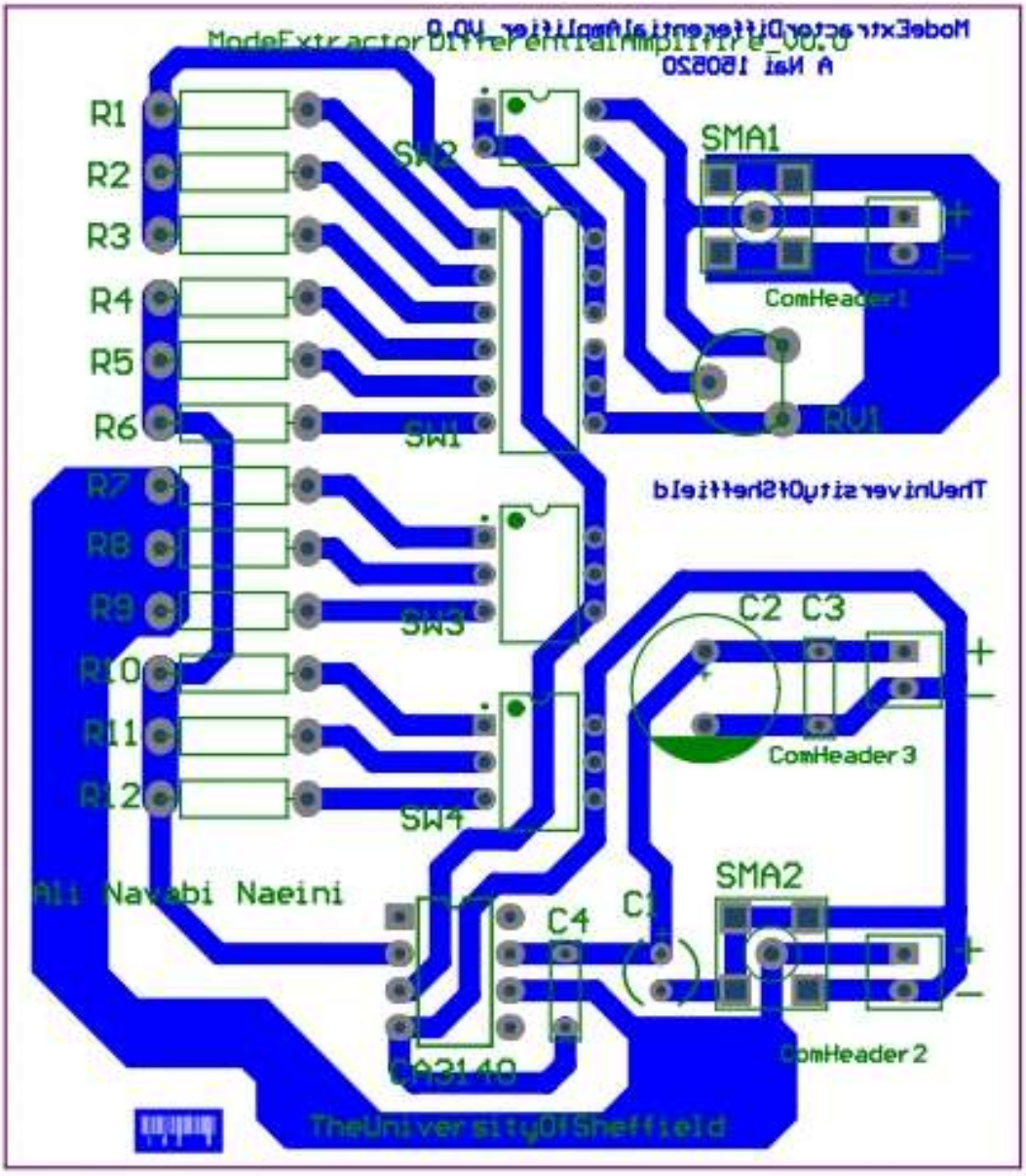
The PCB diagram of the gate driver board



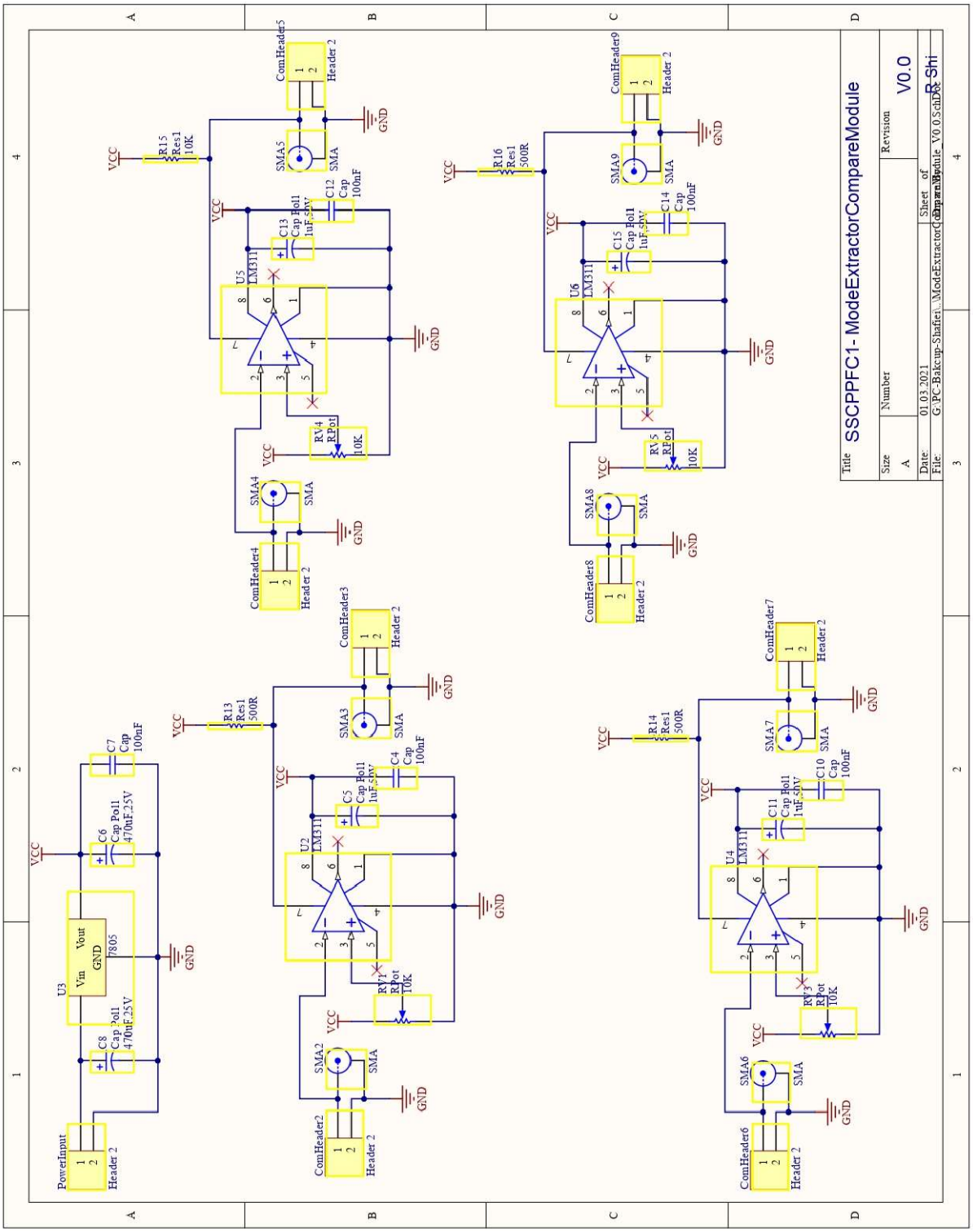
The schematic of the differential amplifier



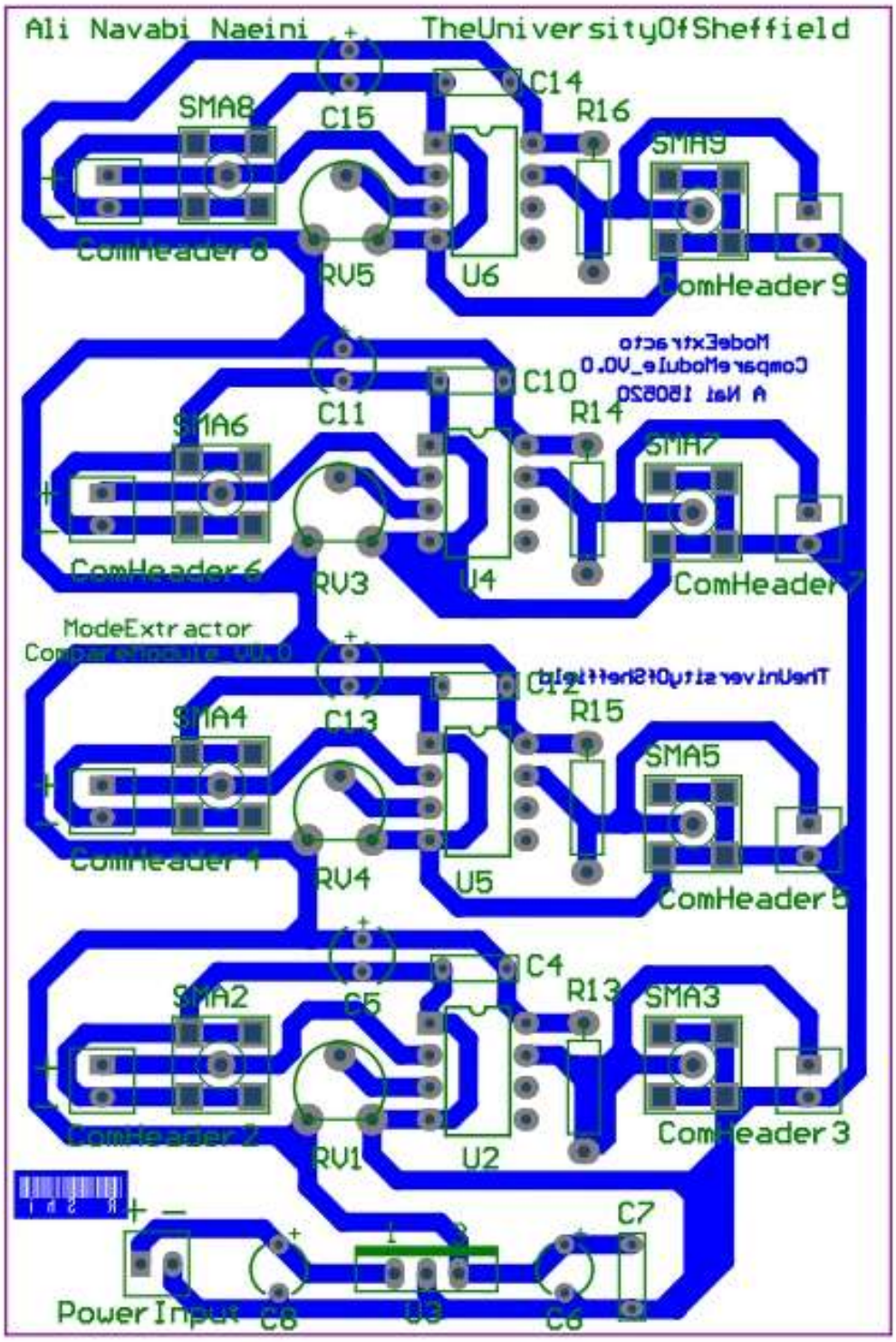
The PCB of the differential amplifier



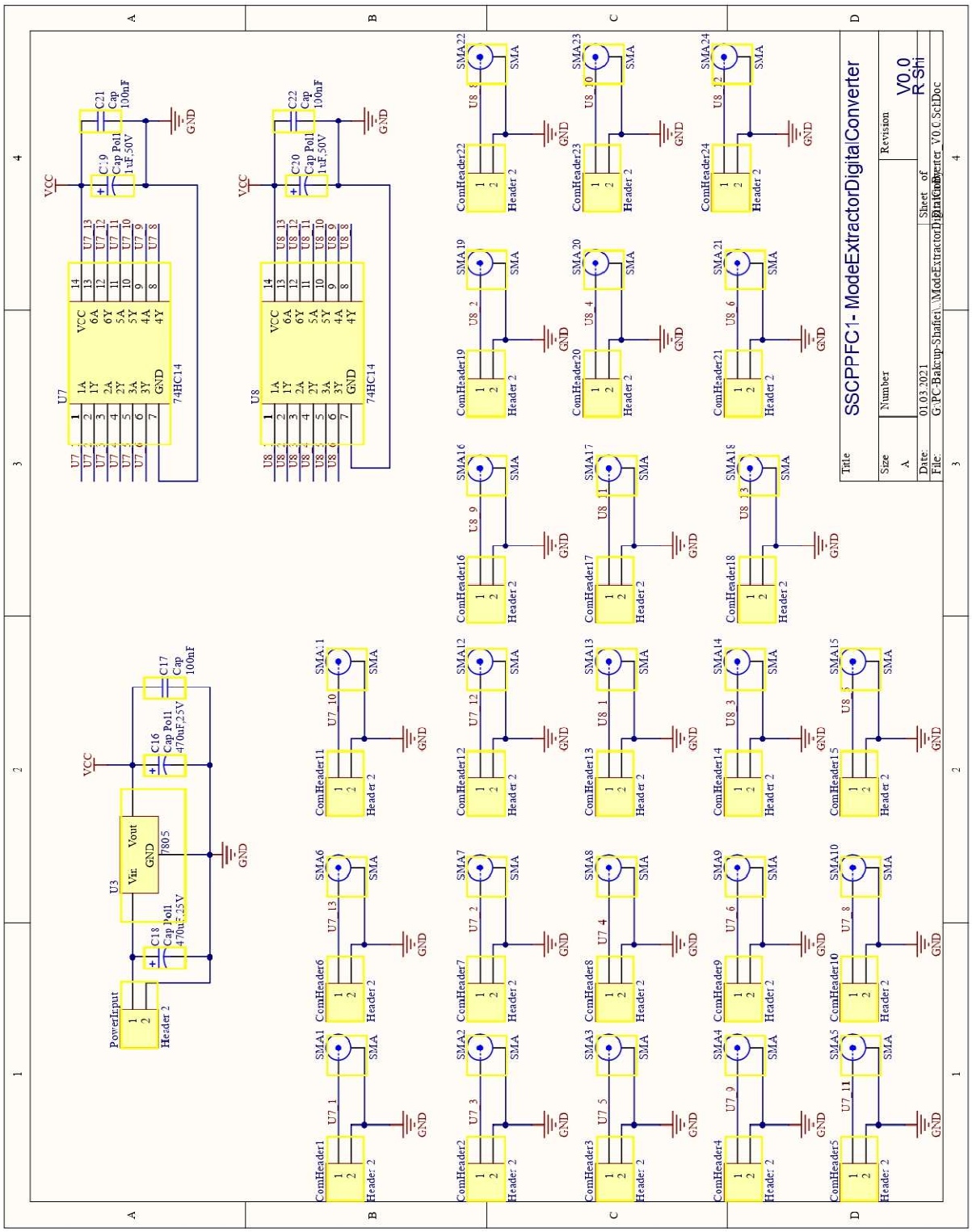
The schematic of the comparator circuit



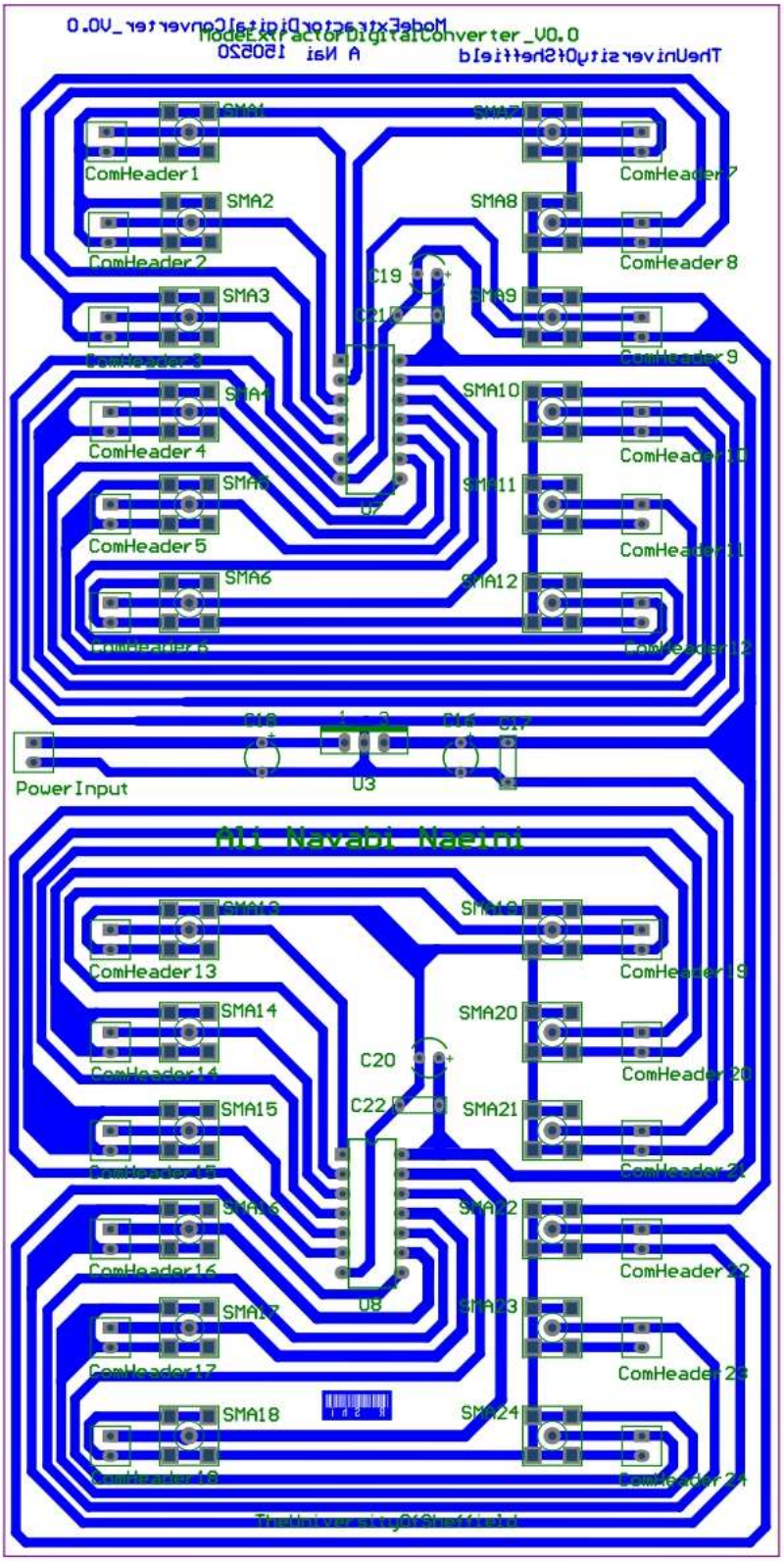
The PCB diagram of the comparator circuit



The schematic of the digital level shifter



The PCB diagram of the digital level shifter



Appendix 4. The results for verification of the resonant tanks

In this appendix the results for verification of the resonant tanks that were constructed in chapter 5 are given. The layout of the figures is the same as the demonstrated in chapter 5.

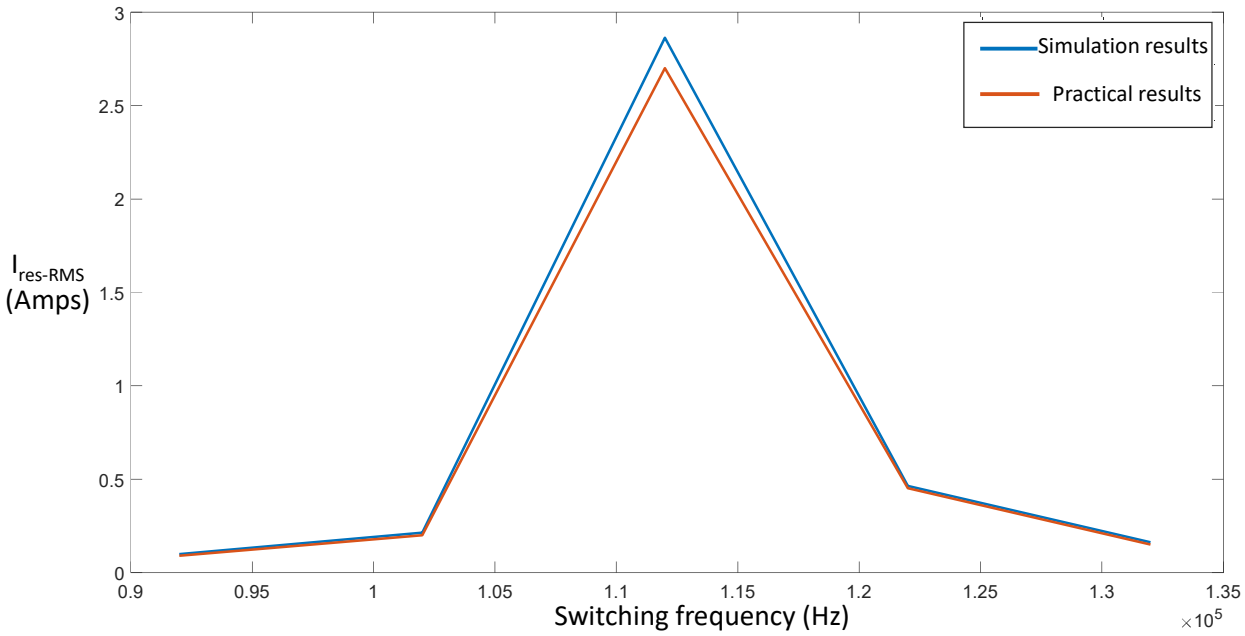


Figure 1: The results for resonant tank 1 with load resistor value of 15 Ohms.

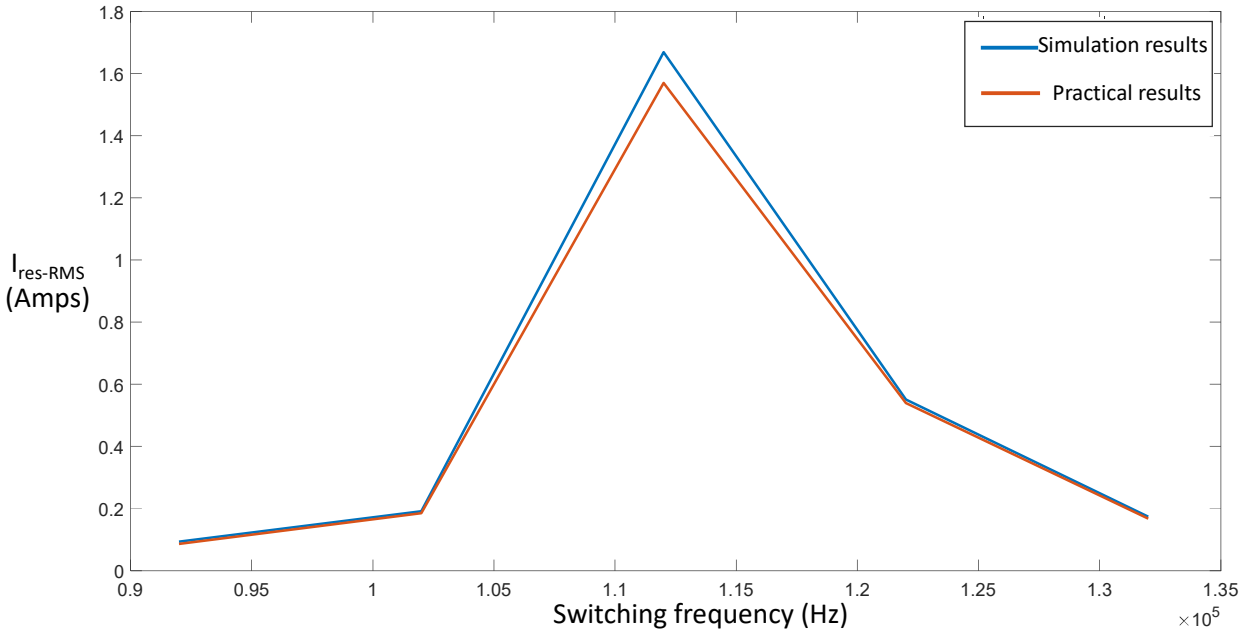


Figure 2: The results for resonant tank 1 with load resistor value of 68 Ohms.

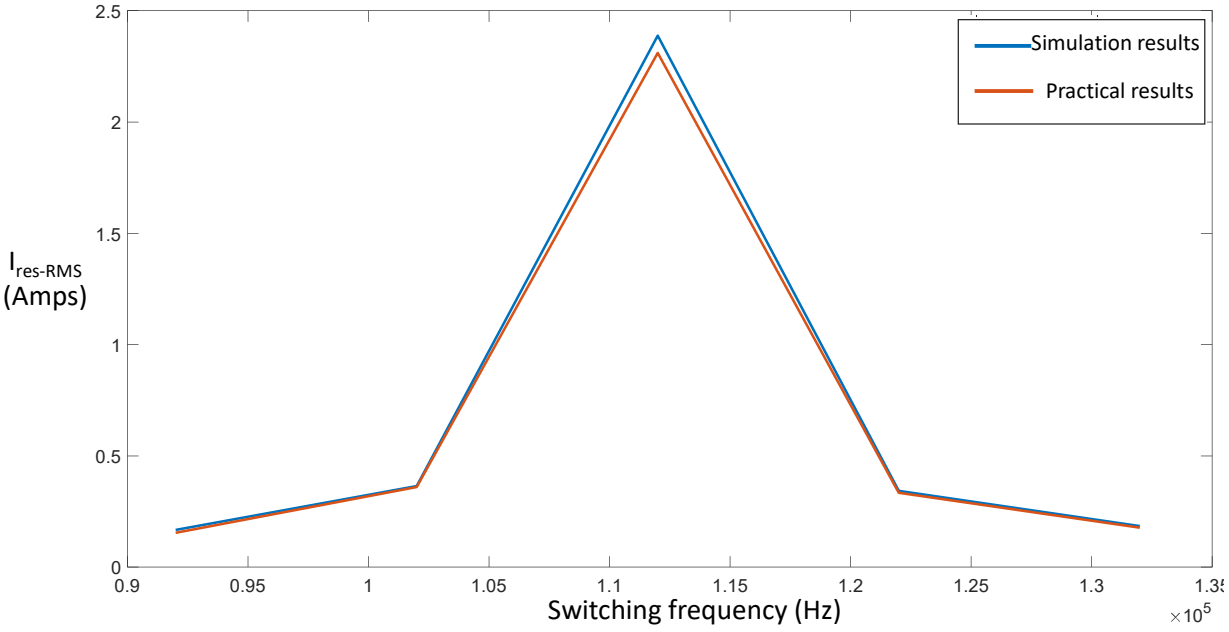


Figure 3: The results for resonant tank 2 with load resistor value of 15 Ohms.

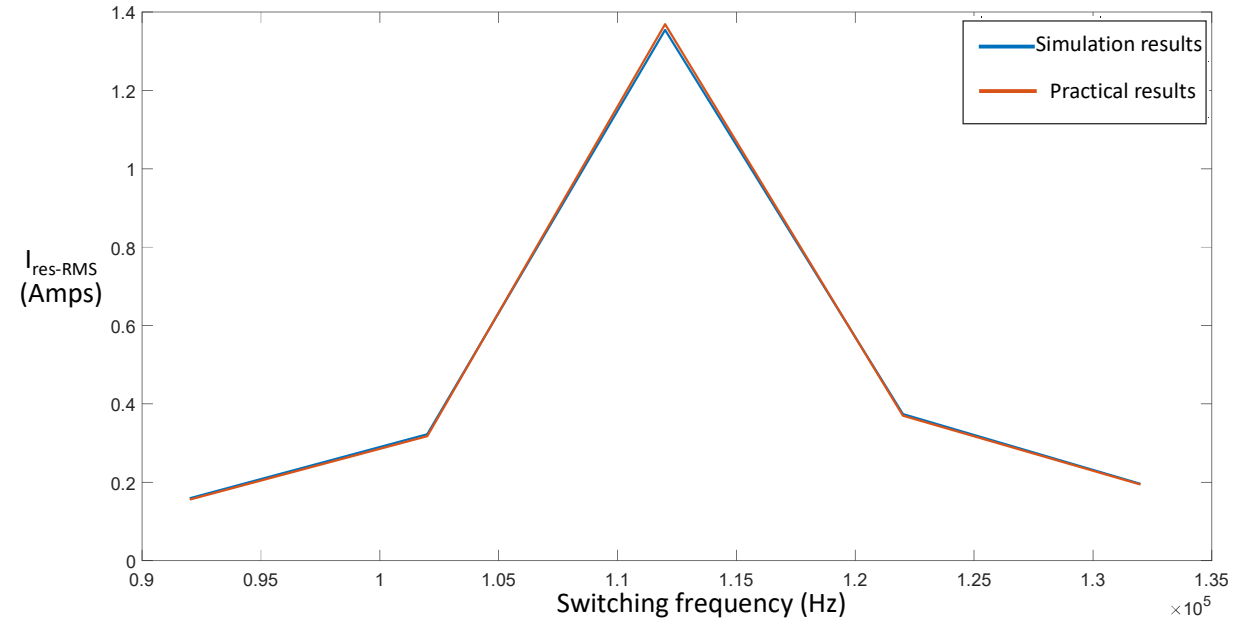


Figure 4: The results for resonant tank 2 with load resistor value of 39 Ohms.

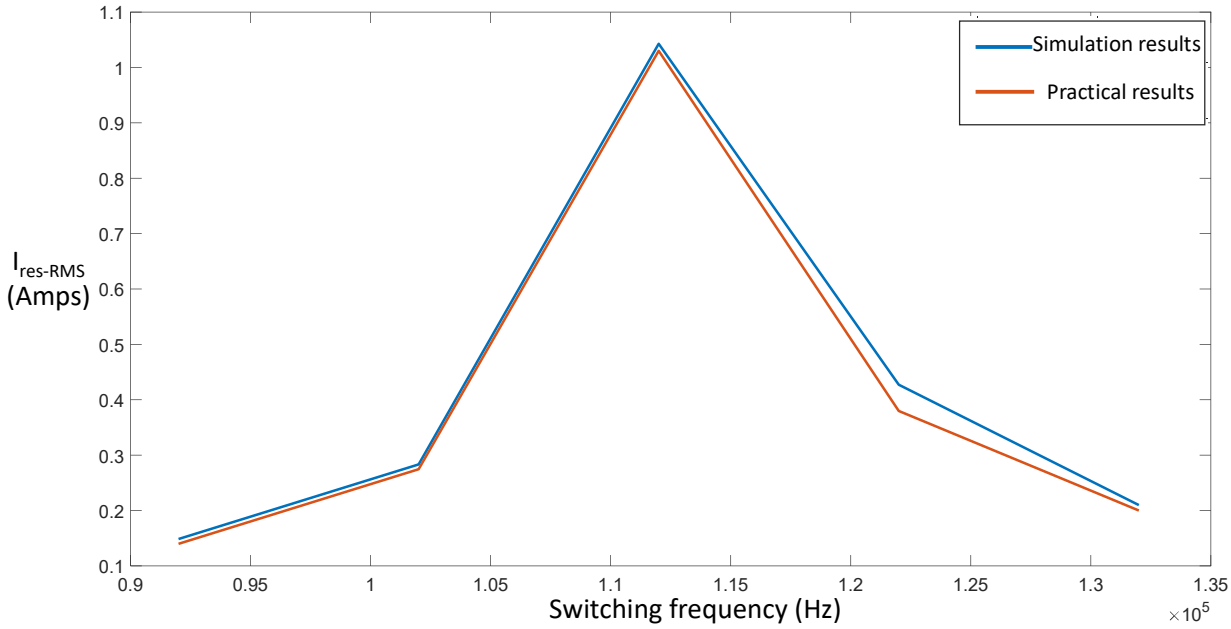


Figure 5: The results for resonant tank 2 with load resistor value of 68 Ohms.

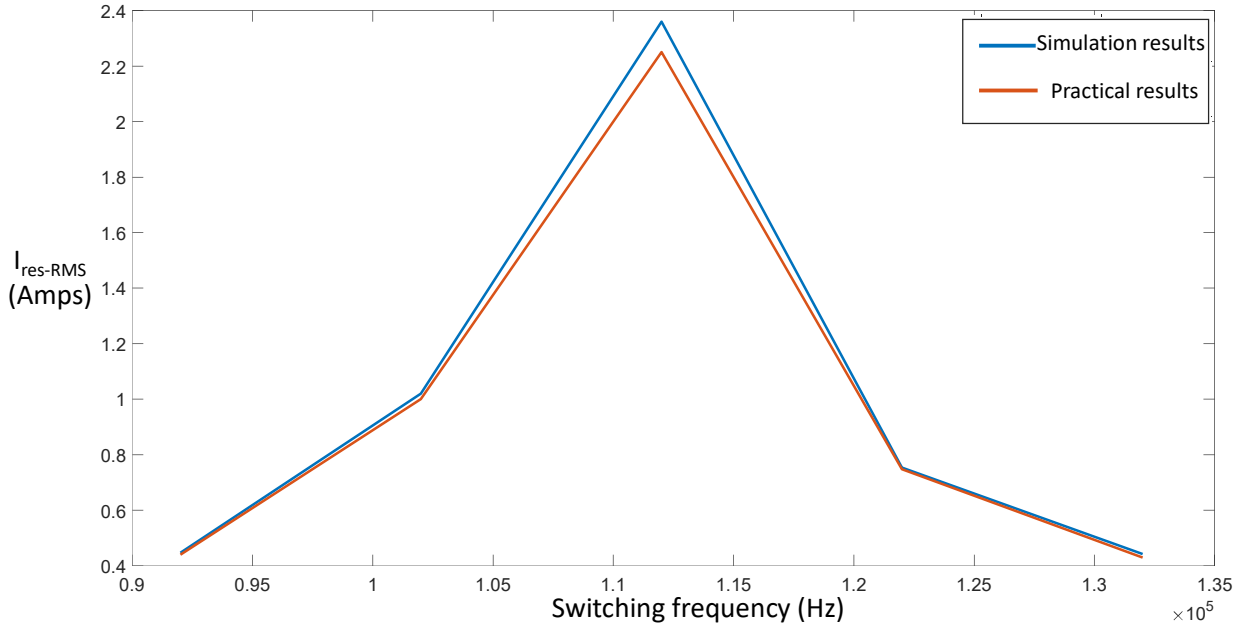


Figure 6: The results for resonant tank 3 with load resistor value of 15 Ohms.

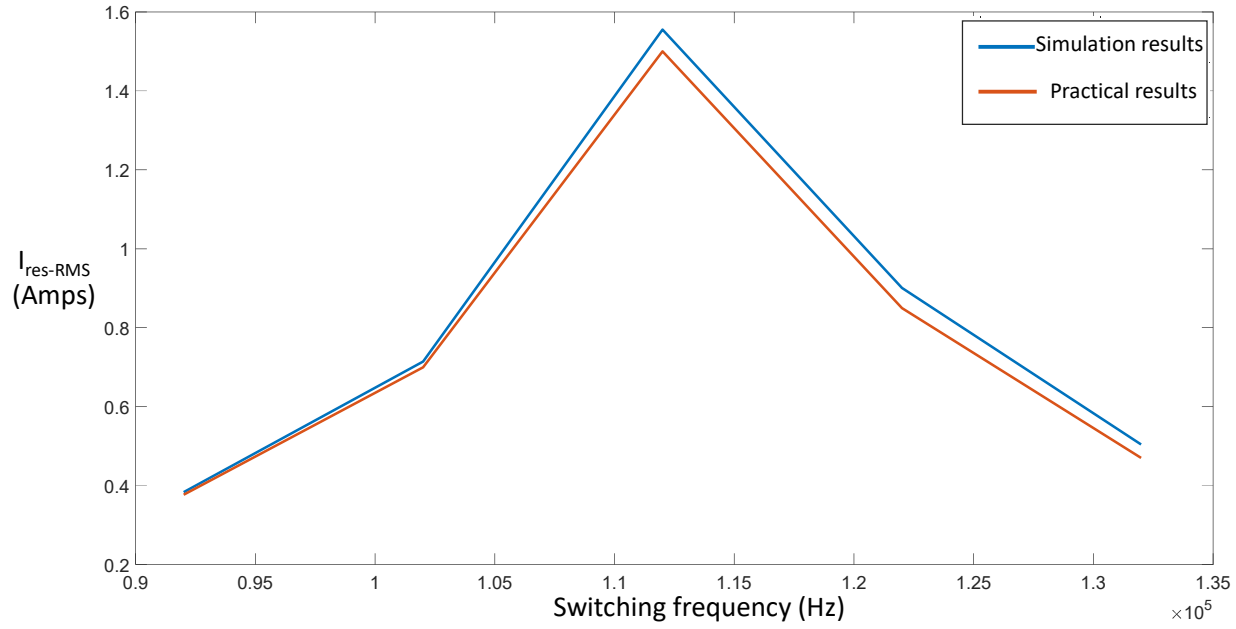


Figure 7: The results for resonant tank 3 with load resistor value of 39 Ohms.

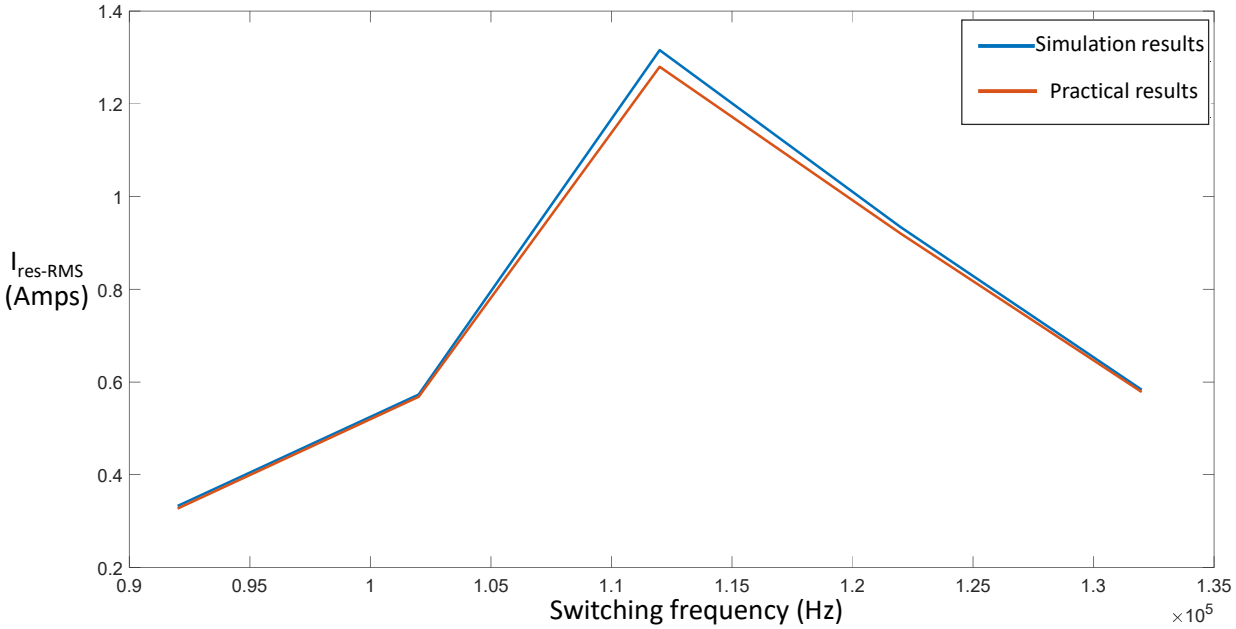


Figure 8: The results for resonant tank 3 with load resistor value of 68 Ohms.