Modelling, and Optimization of Grid-Tied Modular Multilevel Converters with a Passive Front-End Rectifier without LC Filter in the DC-Link

By

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Abstract

Due to the critical importance of minimising the cost, size, weight, and component count in applications such as high-power wind turbines, where the size and weight of the required electrical components are restricted by the tower space and capability, this study presents a compact system with low size, weight, and cost that is suitable for high power wind turbine applications. Here, the simplest structure in the rectifier side is used which is the well-known 6-pluse diode bridge rectifier. However, the 6-pluse diode bridge rectifier have substantial drawbacks; namely, unregulated dc-link voltage and significant dc-link ripple. Thus, a dc/dc boost converter is used to regulate the rectifier voltage in the dc-link of the inverter and large LC filter is used to smoothen the rectifier output. These extra parts increase the system size, wight, and cost. Therefore, to overcome these drawbacks, this project presents an optimised design and control of grid-tied full-bridge modular multilevel converters (MMC) with a passive front-end rectifier without passive components in the dc-link. This study shows that the full-bridge modular multilevel converter can act as a boost converter and large dc-link filter by itself.

Moreover, this study develops a new steady-state model of the full-bridge MMC with non-ideal dc-link voltage where MMC input impedance is modelled as a function of MMC parameters including the dc-link dominant harmonic frequency. The analysis reveals that the ripple in the dc-link can create a new resonance

frequency of the MMC sub-modules and arm inductances, in addition to the conventional second-order resonance frequency, which however can be prevented by optimal selection of MMC parameters.

Furthermore, this study develops a new analytical solution to the harmonic spectrum of the Full-Bridge MMC (FBMMC) dc-side based on phase-shifted carrier pulse width modulation and considering varying dc-link voltage operation. The harmonic distribution of the FBMMC dc-side voltage is analyzed through using double Fourier series analysis. Through the analysis, proper selection of the modulation indexes, carrier displacement angle, and the number of Submodules can ensure a significant reduction in the dc-link switching-ripple voltage. Thus, the related filter can be removed or significantly reduced.

The outcomes of this thesis are validated through simulation and experimental test.

ACKNOWLEDGMENTS

I am indebted to my supervisor, Dr. Milijana Odavic, for her great supervision and consistent support during the process of this research. I am extremely appreciative of her assistance and will always remember her with thanks. In all of my years of higher education, Dr. Odavic has been the most impressive advisor I've ever had.

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LIST OF ABBREVIATIONS

WECS	Wind Energy Conversion System
DCM	Discontinuous mode
THD	Total harmonic distortion
PF	Power factor
MMC	Modular multilevel converter
HBMMC	Half-Bridge MMC
FBMMC	Full-bridge MMC
ac	Alternating Current
dc	Direct current
SM	Submodule
FBSM	Full-bridge submodule
HBSM	Half-Bridge submodule
Up	Upper arm
Low	Lower arm
LL	Left leg of the SM
RL	Right leg of the SM
IGBT	Insulated gate bipolar transistor
PSC	Phase shift carrier
PWM	Pulse with modulation
PGSC	Passive generator side converter
BTBC	Back to back converter
EC	External Control
IC	Internal Control
TIC	Total Internal Control
PIC	Partial Internal Control
CCS	Circulating current suppression

LIST OF SYMBOLS

C_{dc}	dc-link capacitor
L_{dc}	dc-link inductor
L_g	Inductance of the grid/ac side inductor/filter
R_g	Resistance of the grid/ac side inductor/filter
L_{eq}	Equivalent inductance seen by the ac side of the FBMMC
R_{eq}	Equivalent resistance seen by the ac side of the FBMMC
Z_{MMC}	The MMC input impedance
$Z_{MMC_{2nd}}$	The MMC impedance related to circulating current 2nd component
$L_{res_{2H}}$	HBMMC resonance inductance related to circulating current 2nd component
$L_{res_{2F}}$	FBMMC resonance inductance related to circulating current 2nd component
$L_{res_{dc}}$	Resonance inductance related to ripple in the dc-link
L_{arm}	Inductance of the MMC arm inductors
C_{SM}	Capacitance of the SM capacitors of the MMC
$x = \{a, b, c\}$	Phase a, b, and c
$P = \{6, 12, 18, ..etc\}$	Number of rectifier pulses
$u_{s,x}$	Input phase voltage of the rectifier (generator phase voltage)
U_s	The amplitude of rectifier input phase voltage
ω_s	Generator angular frequency (rad/s), $\omega_s = 2\pi f_s$
f_s	Generator frequency
$i_{dc-link}$	Dc-link side current
u_{dc}	Dc-link side rectifier voltage
U_{dc}	Dc-link voltage dc component
$i = \{1, 2, 3, \infty\}$	Dc link side harmonics order
u_{Pif_s}	Dc-link voltage ripple components
U_{Pif_s}	Amplitude of dc-link voltage ripple components

θ_{s_i}	Relative phase angle of U_{Pif_s}
$u_{dc,MMC}$	The dc-link switching-ripple voltage generated by the FBMMC
T	Fundamental time period
N	Number of cascaded SMs in one arm
$k = \{1,2,..N\}$	k^{th} SM in an arm
$r = \{up, low\}$	Upper/lower arm of the MMC
i_x^r	Upper/lower arm current in phase x
u_x^r	Upper/lower arm voltage in phase x
$u_x^{r,k}$	Output ac voltage of k^{th}SM in up/low arm of phase x
$u_{c,x}^{r,k}$	Capacitor voltage of k^{th} SM in up/low arm of phase x
U_c^0	The average SM capacitor voltage
$\Delta U_c\%$	The desired SM capacitor voltage fluctuation factor
$i_{c,x}^{r,k}$	Capacitor current of k^{th} SM in up/low arm of phase x
$i_{cir,x}$	Circulating current of FBMMC in phase x
i_{dc}	Rectifier (dc-link) current component per MMC phase $i_{dc} = i_{dc-link}/3$
I_{dc}	Dc component of i_{dc}
i_{Pif_s}	Current ripple components of i_{dc}
I_{Pif_s}	Amplitude of i_{Pif_s}
$i_{z,x,2}$	Circulating current second order component of MMC phase x
$i_{z,x}$	Circulating current ripple component of MMC phase x
$u_{g,x}$	Grid phase voltage
U_g	Amplitude of grid phase voltage
i_x	Grid phase current
I_m	Amplitude of ac side/grid side phase current
f_g	Grid frequency
ω	Grid angular frequency
$\theta_x = \{0, -\frac{2\pi}{3}, \frac{2\pi}{3}\}$	initial angle of phase a, b, and c, respectively

φ	Phase angle of grid phase current, at unity power factor $\varphi = \theta_x$
$u_{m,x}$	Instantaneous ac voltage of the MMC phase ‘x’
$u_{o,x,f}$	Referring fundamental component of $u_{m,x}$
U_m	Amplitude of MMC fundamental component of $u_{m,x}$
$u_{o,x,h}$	Referring to high-frequency harmonics component of $u_{m,x}$
$u_{dc,MMC,x}$	The dc-terminal switching voltage of the FBMMC phase ‘x’
P_g	Active power grid side
Q_g	Reactive power grid side
k_m	MMC modulation index, ratio of ac peak-peak phase voltage to dc voltage
S_m	the apparent power of the MMC
M_{dc}	Dc-component in the modulation signal.
M_{ac}	Amplitude of modulation signal fundamental component.
$M_x^{r,k}$	Modulation signal of upper/lower arm of kth SM.
$M_{x,LL}^{r,k}$	Modulation signal of upper/lower arm of kth SM left leg.
$M_{x,RL}^{r,k}$	Modulation signal of upper/lower arm of kth SM right leg.
θ_c^r	Upper/Lower carrier phase shift angle
θ_d	The carrier's displacement angle between the upper and lower arms
m	Multiples of carrier frequency
n	Multiples of fundamental frequency
$C_{m,n}$	Harmonic coefficient (total) of the order {m,n}
$C_{m,n}^{LL}$	Harmonic coefficient (total) of the order {m,n} for the left leg of FBSM
$C_{m,n}^{RL}$	Harmonic coefficient (total) of the order {m,n} for the right leg of FBSM
ω_c	The carrier angular frequency
f_c	The carrier angular frequency
J_n	Bessel function of nth order
$round$()	Round to nearest integer

Chapter 1: Introduction

1.1 Renewable Energy Sources

All development, whether social or economic, is linked to the accessibility of energy sources. The primary sources of energy for almost all countries - industrialised and developing – continues to be fossil fuels due to their relatively low initial cost for conversion to electrical energy. However, the conventional existing energy sources (i.e., fossil sources) have two major problems. Firstly, fossil fuels are non-renewable and limited, and this means that existing stockpiles will likely struggle to meet global energy demands in the coming decades. Secondly, these energy sources pollute the environment and increase the amount of CO2 and other greenhouse gas emissions. These high emissions have been proven to cause global warming, with consequences that include, but are not exclusively limited to, irregular patterns in climate, and reduced food production [1]. Lastly, the availability of fossil fuels is limited to certain countries, which poses a danger to energy price stability [1] [2]. As a result, the adoption of Renewable Energy Sources (RES) is now considered the most viable solution to mitigate the impacts of fossil fuels on the environment and solve the issue of their limited quantity and availability [1] [2]. It is generally well-known that RES are gradually becoming more economically viable and are environmentally clean and virtually unlimited. Onshore wind and solar, in particular, can already provide electricity at a cost that is competitive with or even lower than that of coal and natural gas power facilities in some regions [3]. However, they are intermittent sources of energy. This shortfall imposes demanding technical issues to safely and reliably meet electricity demand [3] [4].

1.2 Overview of wind energy conversion systems

Wind power has been used by people for thousands of years to move ships across oceans and, later, to pump water and grind grain. In 1887, an automated wind turbine with a 12-kW dc generator was the first handset to turn the motion of the wind into electricity [3] [5]. Of all types of RES, wind energy conversion system (WECS) is currently witnessing the most significant and fastest growth: total global production of wind energy increased from 282.6 GW in 2012 to 742 GW in

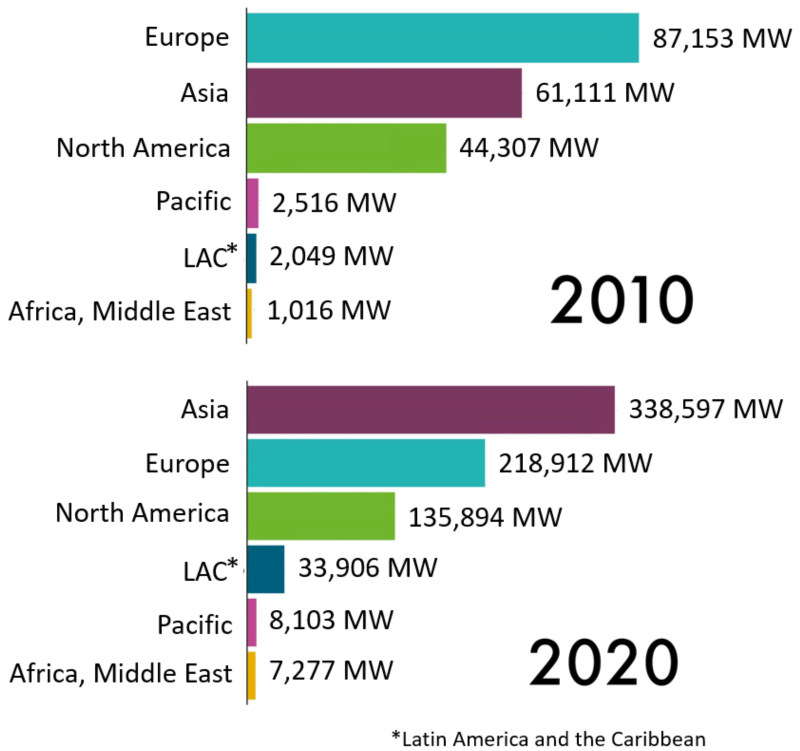


Figure 1-1 Last decade globe growth in WECS [4]

2020 [3] [4]. Figure 1-1 shows how the number of wind turbines around the world has grown over the last decade. In addition, the wind energy business provides numerous direct and indirect employment possibilities, which stimulate economic growth significantly. China has around 275 GW of installed onshore wind power and 9.88 GW of offshore wind power [4]. Moreover, with 10.2 GW of installed offshore wind power and 14.1 GW of installed onshore wind power, the United Kingdom has the biggest share of installed offshore wind power [4]. This remarkable growth rate can be attributed to a number of factors, some of the most important of which being the declining costs, the technical improvements, and the incentive programmes offered by the government [3].

The aerodynamic principles of a wind turbine dictate that the square of the rotor diameter and the cube of the wind speed are the key variables in determining the turbine's power production. Compared to the group of tiny turbines, the huge turbines can collect more wind power with reduced installation and maintenance expenses, especially in offshore wind turbines [3]. Due to this, the size of commercial wind turbines has expanded rapidly over the past decades, as seen in Figure 1-2 [3].

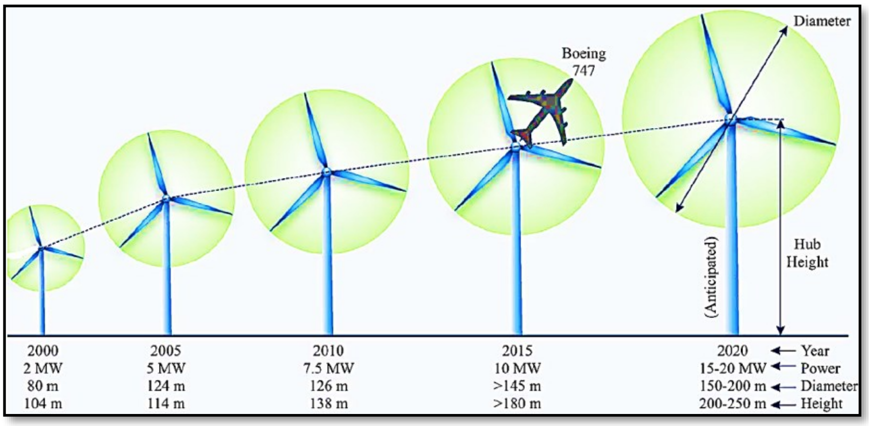


Figure 1-2 Size evolution of commercial wind turbines[3]

Offshore wind farms have been adopted more and more in the UK due to land limitations [6]. However, globally, Figure 1-3 shows that, onshore turbines continue to dominate the market. This is due to the fact that the low capital and maintenance costs involved with the building of onshore wind farms eventually result in a lower levelized cost of energy production, making it similar and in certain regions even cheaper than the cost of energy production from coal and natural gas facilities [4].

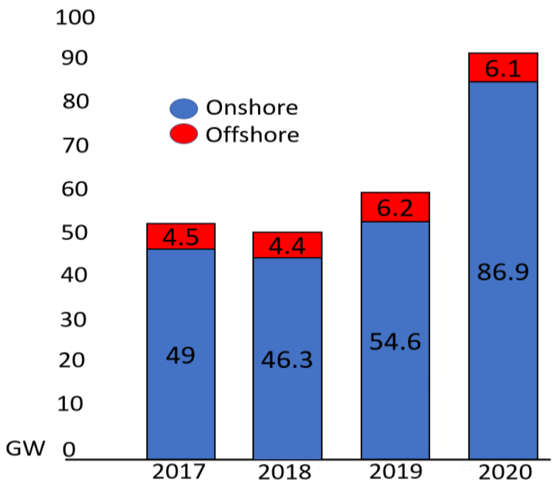


Figure 1-3 The evolution of new wind energy installations[4]

In the last few years, there have been a lot of technological advances in the wind energy sector, especially in the areas of aerodynamic design, mechanical systems, electric generators, power electronic converters, integration with power systems, and control theory. From an electrical engineering point of view, electric generators and power electronic converters are two of the most important parts of WECS [3]. According to the available data, WECSs will develop exponentially in the coming decades [3] [7]. The technological advancement of wind energy conversion systems will play a crucial role in the creation of highly efficient wind power systems. The adoption of wind energy will ensure energy independence and a pollution-free environment. This is because the wind is free, now and forever, and available to all nations.

1.3 Wind energy conversion system topologies

The wind energy evolution has developed incredibly rapidly in the last few years. The technological advancements in terms of enhancing wind energy conversion efficiency and reliability, covering both the high demand of energy and the environmental concerns, are impressive. For WECSs, the basic configuration is shown in Figure 1-4 and consists of the conversion of mechanical to electrical power via a generator [3] [8] [9].

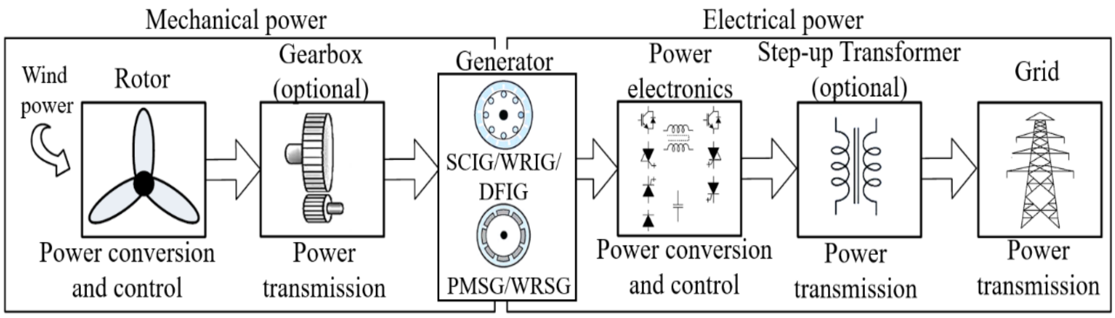


Figure 1-4 basic configuration of a wind turbine system

In the mechanical section of the system, the turbine blades receive power from wind and transform it into mechanical energy. The blades' angle is changeable to reduce the amount of kinetic energy captured from the wind once the speed of the wind exceeds the nominal value. In low wind speed conditions, the gearbox is commonly used to adapt the turbine rotor speed to the high speed of the generator. The mechanical energy is then converted into electrical power by the generator. Moving to the electrical system section, the main components here are the generators, filters, the power electronics converters, and step-up transformer. The employment of power electronics in the WECSs are to control the power generation of the wind turbine, enhance dynamic and steady-state performances and satisfy the demands of the grid side and generator side.

In contrast to any other application, the selection of the mechanical and electrical components for wind energy systems requires more stringent system criteria. These prerequisites are outlined briefly below [3] [8] [9] [10]:

- Efficiency:

The ability to generate MW of power from a single wind turbine makes efficiency crucial for reducing energy prices. At the wind farm level, where hundreds of wind turbines are located, even a 1% improvement in the efficiency of any portion of the wind turbine unit can save considerable amount of money. High efficiency switching devices, an optimal layout of switching device cooling systems, cables with highly efficient characteristic, modulation, and control methods, etc., are all ways to reduce the power losses that have a direct impact on efficiency.

- Initial Cost

This is the most crucial aspect of making energy affordable, appealing to investors, and competitive with other energy sources. One should note that initial cost of power converters is 7 to 12% of wind turbine cost. Even though it seems little, it may save a lot of money to a wind farm with hundreds of turbines.

- Power Quality

Various power converter factors contribute to the power quality. The output voltage waveform must be close enough to a sinusoidal waveform. This is usually defined by the number of steps in the output voltage waveform, i.e., dv/dt. The need for an output filter decreases as the number of waveform steps increases, since dv/dt decreases as the number of steps increases. Furthermore, with decreasing dv/dt, electromagnetic interference is reduced. Currently, modular multilevel converters (MMCs) are regarded the most effective way to obtain excellent power quality. In comparison to generator side current quality, high grid current quality is more important for grid code compliance.

- Reliability, Modularity, and Maintenance Cost

The power converter failures increase the operational downtime of wind turbines and the total cost of electricity. Power converters for wind turbines, particularly offshore turbines, must thus be highly reliable. It is generally recognised that a system with a high failure rate increases the cost of maintenance dramatically, especially when the system is difficult to reach, as is the case with offshore wind turbines. Moreover, system reliability can be increased by an efficient modular structure, as in the event of failure, a system with an efficient modular structure can eliminate or reduce the operational downtime of wind turbines.

- Size and Weight

To minimise the size and weight of the wind turbine unit, all electrical and mechanical components must have a high-power density. This is a crucial prerequisite, particularly for offshore wind turbines. It is undesirable to have a large system with too many components, even if it is very efficient, because this would significantly increase the system's price, size, and unreliability.

- Grid code compliance

Reactive power, ride-through capability, maximum power point tracking (MPPT), voltage and frequency support, all of these elements should be provided by the system whenever the grid operator requests them. These needs should ideally be met by the power converter without the need for further hardware or components like a static synchronous compensator (STATCOM) or any others.

In order to fulfil the above-mentioned requirements, the evaluation of WECSs has gone through many combinations and designs of power electronic converters and generators. These can be broadly categorised as: Fixed speed WECSs, Limited-Variable speed WECSs, and Full-Variable speed WECSs. Each of them is briefly explained below [3] [8] [9] [10].

1.3.1 Fixed speed WECSs

The configuration of fixed-speed WECSs consists of a Squirrel-Cage Induction Generator (SCIG) connected via a fixed ratio gearbox to the wind turbine and via a soft starter and step-up transformer to the grid. This operates at almost constant rotor speed. This topology usually requires a shunt capacitor bank since the generator draws reactive power from the grid. Moreover, it requires a soft-starter to limit the SCIG high starting current. Figure 1-5 shows the typical scheme of fixed-speed topology which was widely used in early WECSs [3] [8]-[10]. However, although this scheme is robust and has simple construction with low cost, it is outdated due to its apparent deficiencies. The main inherent drawbacks for this scheme are that it has low energy conversion efficiency, fluctuating output power due to changes in the wind speed, high mechanical stress due to grid faults, and it requires an additional hardware, such as STATCOM to achieve grid requirements [3] [8]-[10].

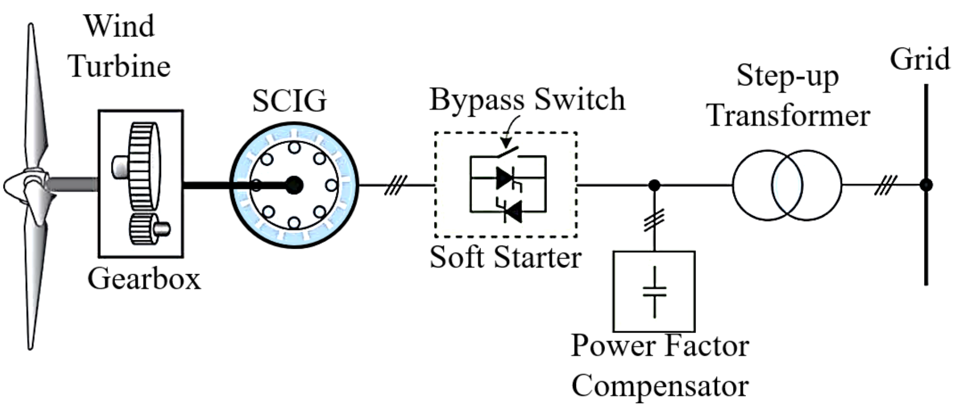


Figure 1-5 Fixed-speed WECSs scheme [3]

1.3.2 Limited-Variable speed WECSs

Two types of generators are used in limited-variable speed conditions. These are the Wound Rotor Induction Generator (WRIG) and the Doubly Fed Induction Generator (DFIG). The limited-variable speed WECSs with WRIG topology is similar to the fixed-speed WECSs with SCIG since the rotor of the generator is connected via a fixed ratio gearbox to the wind turbine and the stator is linked via a step-up transformer to the grid, see Figure 1-6. Moreover, it also requires soft starter and reactive power compensation for the same reason [3] [8]-[10]. However, by contrast to Fixed-speed WECSs, the Limited-Variable speed WECSs with WRIG have better energy conversion efficiency, less mechanical stress, less maintenance demands and a longer life cycle. This topology can adjust the speed within about ±10% of its rated through adjusting the rotor resistance via a power converter. However, this topology is becoming increasingly unfavourable due to the fact that it has high losses in the rotor resistance and very limited speed range [3] [8]-[10].

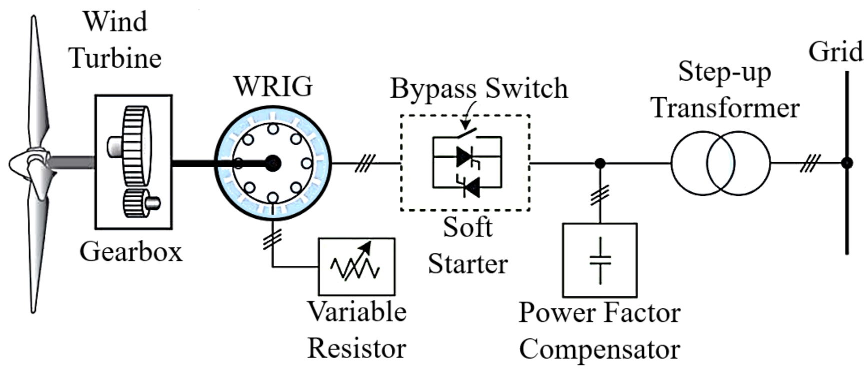


Figure 1-6 The Limited-Variable speed WECSs with WRIG scheme [3]

The second topology is limited-variable speed WECSs with DFIG, see Figure 1-7. In this topology, the stator and rotor windings of the generator delivered the power into the grid. The rotor of the generator is linked into the grid by a partial rated converter. This has 30% rated power, a feature which is considered one of the main advantages of this scheme. However, as with the previously described topologies, this scheme requires a gearbox to synchronise the speeds of the wind turbine and generator. The feasibility of the implementation of the converter is that grants bidirectional power flow, increases the speed range adjustment to up to 30% and allows the MPPT technique to be performed. In contrast to fixed-speed WECSs with SCIG and limited-variable speed WECSs with WRIG, limited-variable speed WECSs with DFIG offer greater power conversion efficiency, more dynamic performance, and greater robustness. Thus, because of these features, in 2015 this topology dominates approximately 50% of market share [3]. On the other hand, perhaps the most serious disadvantages of this topology are that it has limited fault ride-through (FRT) capability because of the partial scale power converter and the need for a gearbox which raises the cost and weight. Moreover, the converter in this topology is linked to the rotor windings by slip rings and brushes. This leads to the necessity of frequent maintenance since the average life span of a brush is 6–12 months [3] [8]-[10]. These drawbacks will almost certainly restrict this topology being applied more widely in the future, especially in the case of offshore applications where maintenance is more logistically difficult and expensive.

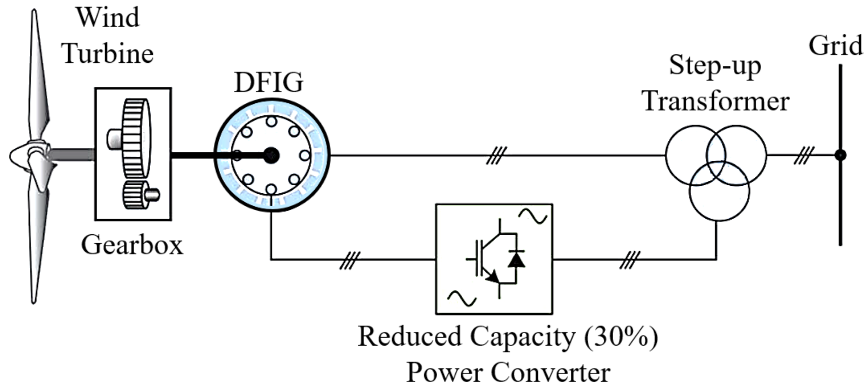


Figure 1-7 The Limited-Variable speed WECSs with DFIG scheme[3]

1.3.3 Full-Variable speed WECSs

The full-variable speed WECSs, also known as full-scale (100%) power converters, represent a significant step in the enhancement of performance of WECSs. The most common types of generators in this category are wound rotor synchronous generator (WRSG), SCIG, and the Permanent Magnet Synchronous Generator (PMSG). However, the PMSG is the most preferred one since it eliminates the requirement for slip rings/brushes and therefore gives the system more robustness and simplicity. In addition, the elimination of the gearbox is possible through employing the PMSG with a high-pole number. This overcomes the drawbacks inherent with gearboxes: high cost, the need for maintenance, and their consequent negative effects on the reduction of both lifespan and efficiency [3] [8]-[10].

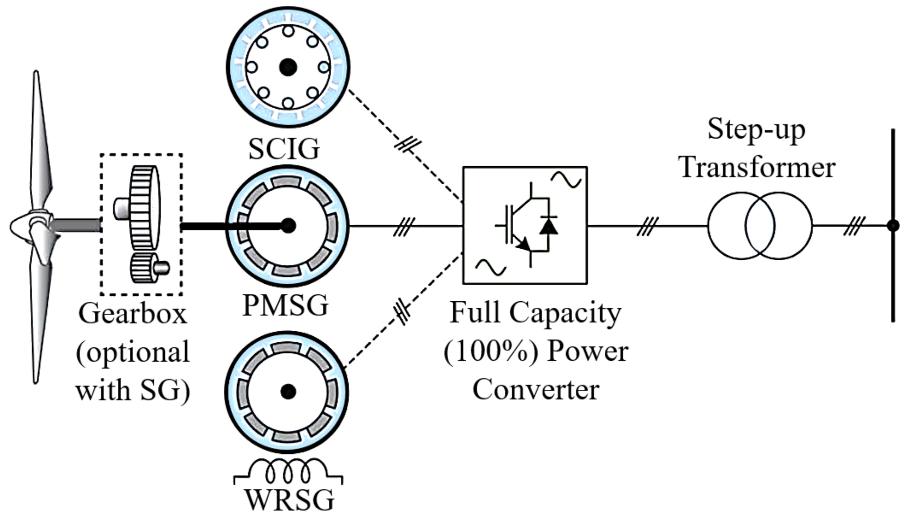


Figure 1-8 Full-Variable speed WECSs scheme [3]

Difficulties may arise, however, in increasing the overall size, cost, and complexity of the topology as the power converters have to be rated in line with generator capacity. Nevertheless, with the presence of the converters in this topology, the generator-side is completely decoupled from the grid network and able to operate through the full range of speed, from 0-100%. The power converters can also perform MPPT and reactive power compensation and provide optimal smooth grid connection.

As a consequence, in contrast to the aforementioned topologies, these full-scale (100%) power converter topologies possess the highest power conversion efficiency and the best capability of FRT. Furthermore, employing multipole PMSG in this configuration has a series of additional advantages. These include better power density and gearless capability. The usage of a gearbox is expensive and results in the following system shortcomings: decreased efficiency, a shorter lifespan, the necessity for frequent maintenance, and the production of excessive noise. Consequently, a gearless or direct-drive architecture of WECSs using multipole generator systems is the most advantageous design for eliminating these drawbacks [3] [8]-[10].

1.3.4 Future trends WECSs topologies

According to the literature, limited-variable speed WECSs with DFIG dominated the market with a roughly 50% share until 2015, and the full-variable speed WECSs topologies took a second place [3]. However, due to the aforementioned benefits, full-variable speed WECS topologies have grown in popularity since then. It can be concluded that among all types of WECSs topologies, the gearless full-scale (100%) power converter with the employment of multipole PMSG is considered the most promising combination topology for the foreseeable future, especially for MW and offshore WECSs [3] [8]-[10].

1.4 State of the art power electronic converters

The escalating power level of WECSs is moving the technology of power electronics towards medium voltage (MV) operation (i.e., 1-35KV) [3] [8]-[11] [12]. Consequently, MV power converters will lead the future generation of high MW WECSs, mostly due to their efficiency and compact design [3] [8]-[11] [12]. The following subsections provide a quick overview of some of the most often used and proposed converter topologies in WECSs.

1.4.1 Two level voltage source converters

The two-level voltage source converters are the most widespread employed converters in the exiting WECSs. Its' structure is shown in Figure 1-9. The trend toward high-MW turbines greatly limits the usage of two-level voltage source converters, despite the fact that these converters are the most mature technology currently available [3] [7] [8]-[10]. This is mostly owing to the low-voltage functioning of two-level voltage source converters, which in turn entails greater current-carrying conductor size (cables) as well as losses. Moreover, high dv/dt stress, as well as bulky and inefficient output filters, are two additional factors that contribute to the limited application of two-level voltage source converters [3] [7] [8]-[10].

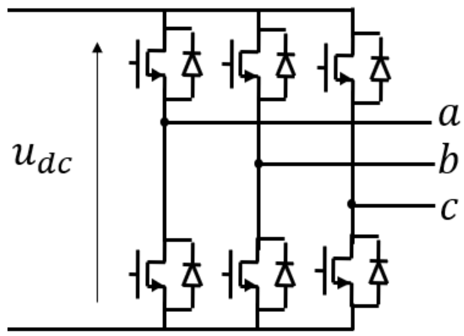


Figure 1-9 Basic structure of two-level voltage source converters

1.4.2 Multilevel voltage source converter

For high-MW turbines, multilevel voltage source converters become the most enabling technology. They are regarded as the best solution for all the issues inherent in the two-level voltage source converter types and recently they have received widespread endorsement for High Voltage Direct Current (HVDC) transmission line applications. They can provide low dv/dt stress and smooth ac voltages without requesting large filter components [3] [7] [8]-[10]. Furthermore, they have inherent energy storage that can be used to minimise propagation of power transients through the converters. The most popular multilevel voltage source converters are Neutral Point Clamped (NPC) converters, cascaded H-Bridge (CHB) converters, Flying Capacitor (FC) converters, and modular multilevel converters (MMC).

1.4.2.1 Neutral point clamped converters

The NPC converters are basically similar to the two-level converter topology, but with two extra power semiconductor switches per phase, see Figure 1-10(a) [11] [12]. The converter neutral point (the middle point in the dc-link) is connected to the midpoint of each converter leg via clamping diodes. This is allowing the possibility of generating the zero-voltage level (with respect to the neutral point). This converter has an important market involvement in high-power motor drive applications and has become the preferred choice for WECSs applications with around 6 MW [3].

However, the NPC has the drawback of experiencing capacitor voltage unbalances. This generates a variation in the potential between the ground and the neutral point in the dc-link, as well as distorted output waveforms [3] [11] [12]. A possible solution is to use active NPC (ANPC) converters, where the clamping diodes in NPC are replaced by switching devices, as seen in Figure 1-10(b). Up to nine-level ANPC is proposed in the literature [3] [12] [13]; however, due to the complex structure, and complicated control scheme, the three-level ANPC is still preferred from an industrial standpoint [3]. Recently the ABB has proposed medium voltage three-levels ANPC wind turbine converter with power range 4-12MW [14].

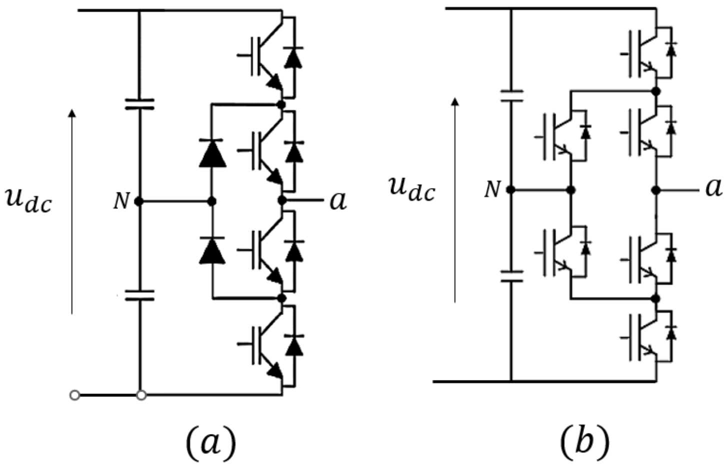


Figure 1-10 Single phase representation of (a) three-level NPC, and (b) three-level ANPC

1.4.2.2 Cascaded H-Bridge converters (CHB)

Commercially, CHB converters are used for photovoltaic power conversion and reactive power compensation [3] [8]. They have also been successfully applied to MV application as their modular structure qualifies for higher voltage operation. Figure 1-11 shows a single phase structure of the CHB. However, one major disadvantage of CHB converters is that they require a significant quantity of isolated dc power supply fed through isolated transformers, which are more expensive and bulkier than the typical transformer used for the NPC [13] [15].

This limits the number of H-bridge units in each leg which limits the number of levels in the output voltage. The high number of CHB components adversely affect the reliability and cost of the system [3] [8] [11].

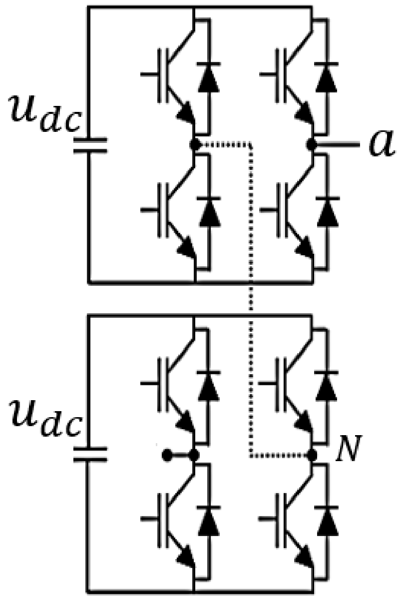


Figure 1-11 Single phase representation of CHB converter

1.4.2.3 Flying Capacitor (FC) converters

The single-phase structure of the FC converters is shown in Figure 1-12. Currently the FC converters have been the most ignored for industrial development for several reasons [3]. For larger multilevel output voltages, the FC converter needs a large number of capacitors and a pre-charging circuit for each one [3] [11]. The FC converter's flying capacitors are less reliable than the diodes in the NPC converter [3] [8] [15]. The control strategy necessitates a bigger number of sensors to provide feedback signals from the FCs, which increases the system's cost and complexity [9] [15]. The maximum output voltage level of FC converters is therefore often restricted to four or five levels [11].

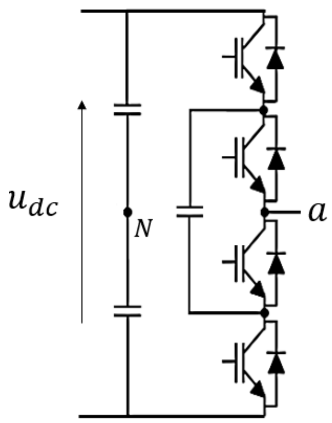


Figure 1-12 Single phase representation of three-level FC converter

1.4.2.4 Modular multilevel converters (MMC)

Multilevel voltage source converters such as the NPC, ANPC, CHB, and FC have been around for about half a century, and some of them have seen significant adoption [15]. Nevertheless, in practise, their multilevel voltage capability is constrained for the reasons described above.

The MMC family is advanced technology that provides an excellent solution to almost all problems associated with other multilevel voltage source converters. The most significant characteristics of MMCs come as additional features over other types of ML converters: their high level of modularity and scalability, their superior harmonic performance, and their high efficiency [15]-[25]. These characteristics likely make them the best type for effectively meeting the requirements of high-power applications [26]. The MMC topology was created in the early 2000s and has gained substantial popularity since then. This converter has become an essential option in HVDC applications and has been effectively deployed in China, Europe, and the United States as a consequence of the extensive research and development that has been done on the MMC and its technology [24]. Siemens, CEPRI, Hitachi-ABB, and GE (formerly Alstom) have all provided several commercial products that are available on the market [24]. For instance, the INELFE power interconnection between France and Spain is the largest MMC-based HVDC system in the world, with a capacity of two gigawatt [27]. Even though MMCs have been suggested for HVDC transmission, they are becoming more and more popular for MV WECS [28] [29] [30] [31] [32]. The MMC phases are built with two arm, where each arm has series-connected submodules (SMs) and decoupling inductance [26] [33]. The SM can be built in different arrangements, however the most common SM arguments are the Half Bridge (HB) SM (HBSM) and Full Bridge (FB) SM (FBSM), as seen in Figure 1-13 [25] [33] [34].

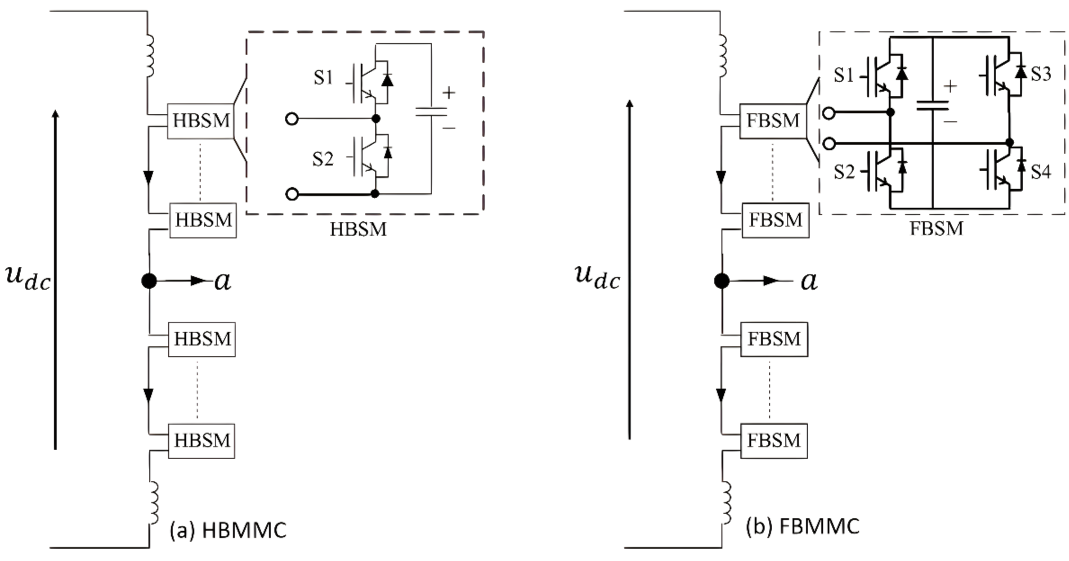


Figure 1-13 Single phase representation of MMC with (a) HBSM (b)FBSM

Unlike the MMC with HBSMs (HBMMC), in the MMC with FBSMs (FBMMC), the voltage on the ac side is independent of the voltage on the dc side because the power capacitors can be connected in either polarity to the terminals. In this manner, the dc-link voltage can be lowered to zero or even completely reversed, while ac and dc current regulation is maintained even under short-circuit conditions [35] [36] [37]. This advantage provides the FBMMC with superior boost and buck capabilities [28] [29]. As a result, it is appropriate for a grid-connected inverter for WECSs where the dc link voltage varies over a wide range [28].

1.5 Full-variable speed WECSs rectifier systems and dc-link problems

The detail structural of the full-scale (100%) power converter full-variable speed WECSs is shown in Figure 1-14 .

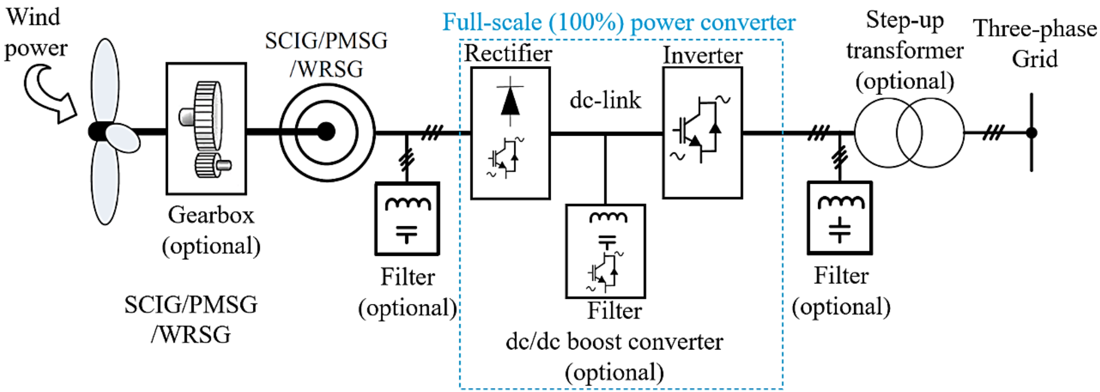


Figure 1-14 Full-scale (100%) power converter full-variable speed WECSs

Focusing on the rectifier, the typical and most popular topologies with the traditional two-level converter can be classified into back-to-back converter

(BTBC) and passive generator-side converter (PGSC) configurations. More details will follow in the next subsection.

1.5.1 PGSC configurations

The main function of the converter in the generator side (i.e., the rectifier) is to convert the ac voltage of the generator to a dc voltage. The simplest and most robust structure that can be used for the converter on the generator side is the three-phase six-pulse diode bridge rectifier, see Figure 1-15. This configuration is well known as PGSC. The three-phase six-pulse diode bridge rectifier has the lowest cost, failure rate, and power losses of any rectifier configuration because their natural commutation eliminates the need for complex controllers, sensors, and gate drivers. Consequently, the three-phase diode-bridge rectifiers are much less costly and naturally more reliable than the PWM converters (i.e., BTB configuration) [3] [5] [7] [38].

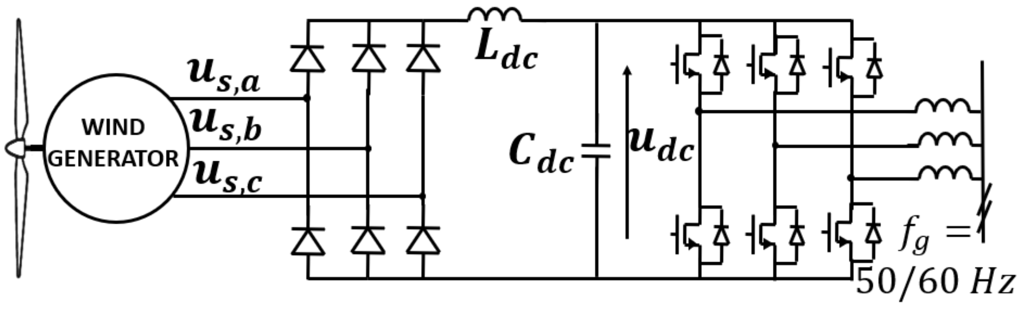


Figure 1-15 PGSC configuration incorporating two-level inverter topologies

However, the diode bridge rectifier has significant dc-link ripple, thus a large LC filter is typically employed [3] [7]. The purpose of dc-link capacitor (C_{dc}) is to protect the ac side of the inverter from the low harmonics caused by the rectifier and provide good energy buffering capability [3] [7] [39].

The dc-link inductor (L_{dc}) is used to prevent the dc-link current going to discontinuous mode (DCM) and in that avoiding zero power intervals where the diodes' switching pattern is lost [7] [40]. However, the three-phase diode bridge rectifier currents have significant total harmonic distortion (THD) in the generator side due to their non-sinusoidal shape. This results in poor total power factor (PF). As a consequence, the L_{dc} value is increased significantly to smooth out currents in the generator side leading to almost rectangular generator current waveforms with THD≈30% and PF=0.955, see Figure 1-16 [40].

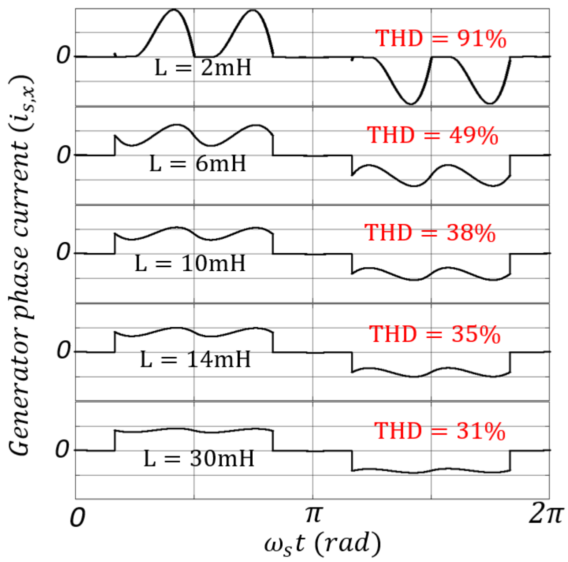


Figure 1-16 Generator phase current waveforms with different values of dc-link inductance

However, another issue associated with the diode bridge rectifier is that it has unregulated dc-link voltage [3] [7]. This results in inefficient power transfer, particularly at low wind speeds. Therefore, a dc/dc boost converter is required to improve the performance of the system, as shown in Figure 1-17 [3] [7].

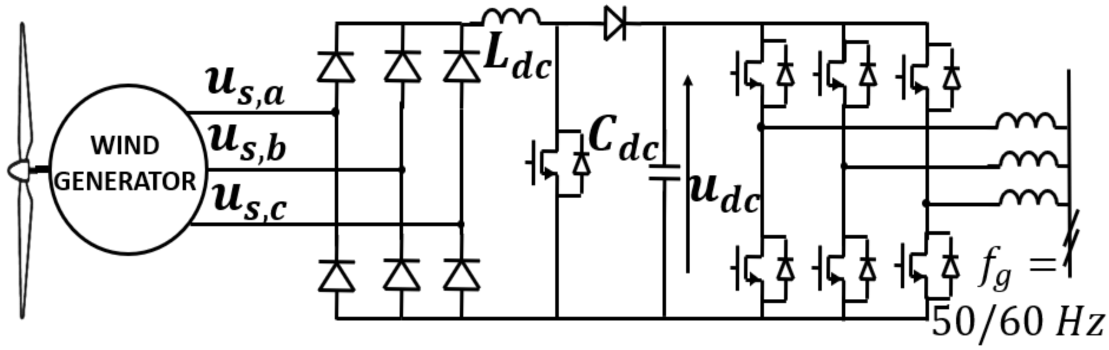


Figure 1-17 PGSC configuration incorporating dcldc boost converter and two-level inverter topologies

Through, the dc/dc boost converter, the dc-link voltage regulation is improved and this enhances the system performance under low speed condition [3] [7]. However, PGSC configuration requires a large tank of electrolytic capacitors in the dc-link and this a major issue especially in high-power application [7] . The electrolytic capacitors is bulky and expensive, and these issues become significantly worse for high-power or MV applications [7] [41]. The capacitor plays a crucial role in the reliability of the system. This is because the capacitors are considered the most prone to failure, as they are sensitive to temperature, humidity, and voltage ripple stresses [42] [43] [44].

Therefore, many authors has considered the BTBC configuration to minimize the dc-link issues of the PGSC configuration [7] [41] [45].

1.5.2 BTBC configuration

Figure 1-18 shows the BTBC configuration; it uses pulse width modulated (PWM) converters on both sides, i.e., as a rectifier and an inverter. They convert the wind generator's variable voltage and frequency output to dc, and then to ac with a constant voltage and frequency for grid connection.

This configuration gives bidirectional power flow function and a variety of selection of wind generator types [3] [5] [38]. In general, different PWM converter topologies, such as NPC, ANPC, FC, CHB, and MMCs, can be used with other variants on either side of the BTBC configuration to provide more efficient power converters than utilising the same converter on both the generator and the grid side. In BTB configuration there is no need for dc/dc boost converter or inductance in the dc-link. However, dc-link capacitors are still required, which presents a significant challenge in MV high-power applications [7] [41] [45], as seen in Figure 1-18.

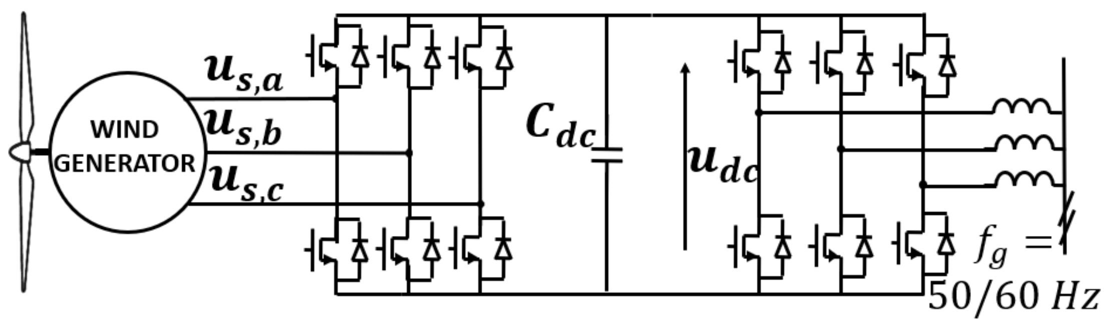


Figure 1-18 BTBC configuration incorporating two-level inverter topology

1.5.3 MMCs contribution in high-power WECSs

Currently, the operation of WECS is reliant on the traditional two- or three-level converter, in which the electrical drive train converts power at low voltage(<1KV) [3]. Traditional two-or three-level converters are mature, but they suffer from high harmonic distortion and require large passive components in the dc-link [3] [7]. In response to the increasing demand for wind energy conversion systems, the size and power of wind turbines have increased considerably over the past decade, with industries currently offering 10- to 14-MW wind turbines and possibly even more in the near future, such as 20 MW [3] [4] [38]. As a consequence of this, the two- or three-level converters become significantly less effective and are no longer applicable to modern WECS [3] [38] [46].

Nowadays, MMCs are standing to offer the an excellent solution for many disadvantages comes with conventional two-level or three-level converters [3] [46]. The most significant characteristics of MMCs are high modularity, high scalability, superior harmonic performance, and high efficiency. Even though MMCs are used a lot in HVDC transmission, there is more and more interest in using them for medium-voltage WECS [28] [29] [30] [31] [32] [47].

For BTBC configuration employing MMCs in both side, as a rectifier and as an inverter, is proposed by many authors [30] [31] [32]. Through this, the dc-link capacitors can be eliminated (i.e., no passive components are required in the dc-link) [30] [48]. However, as the flow of power in the WECSs is unidirectional (i.e., from generators to the grid and not the other way around), using MMC in both sides may be an overestimated method, and increase cost, size, control complicity, and unreliability [3] [28] [29].

As previously stated, the diode bridge rectifier has the simplest structure and is the most reliable solution for the generator converter side. Authors in [28] present a PGSC based system connecting to a FBMMC as an inverter. The authors of [28] have shown through the experiment results that their proposed system can connect to the grid and meet grid code requirements without the use of a boost converter. This is because the FBMMC can provide both boost and buck operation modes, as mentioned earlier [35] [36] [37].

1.6 Proposed system and motivation

This project improves the system proposed in [28] several steps further. In [28] large passive filter is used to smooth out the dc-link voltage ripple. Ideal dc-link voltage (ripple-free) can be seen clearly in the results presented in [28]. Large passive components in the dc-link, especially capacitors, for high power applications is not practical solution [7] [41]-[44]. The dc-link passive components are heavy and require a relatively large portion of the overall cabinet space. They also limit future directions of the full system integration, including the inverter and generator [41]-[44].

Therefore, this project proposed a direct drive grid-tied FBMMC with a passive front-end rectifier without LC filter in the dc-link. The proposed system is shown in Figure 1-19.

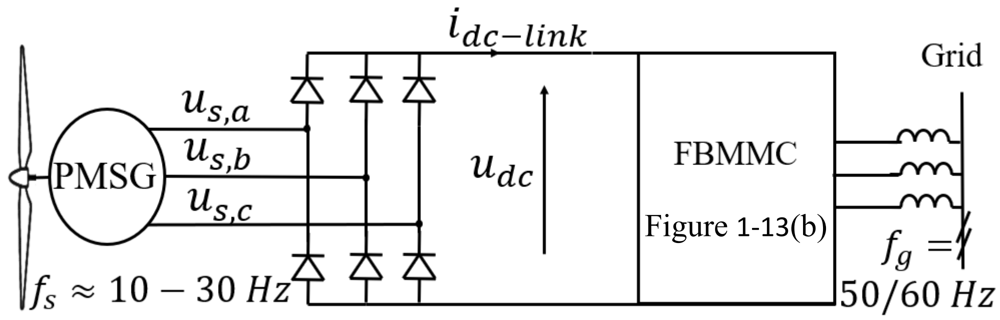


Figure 1-19 The proposed WECS system configuration

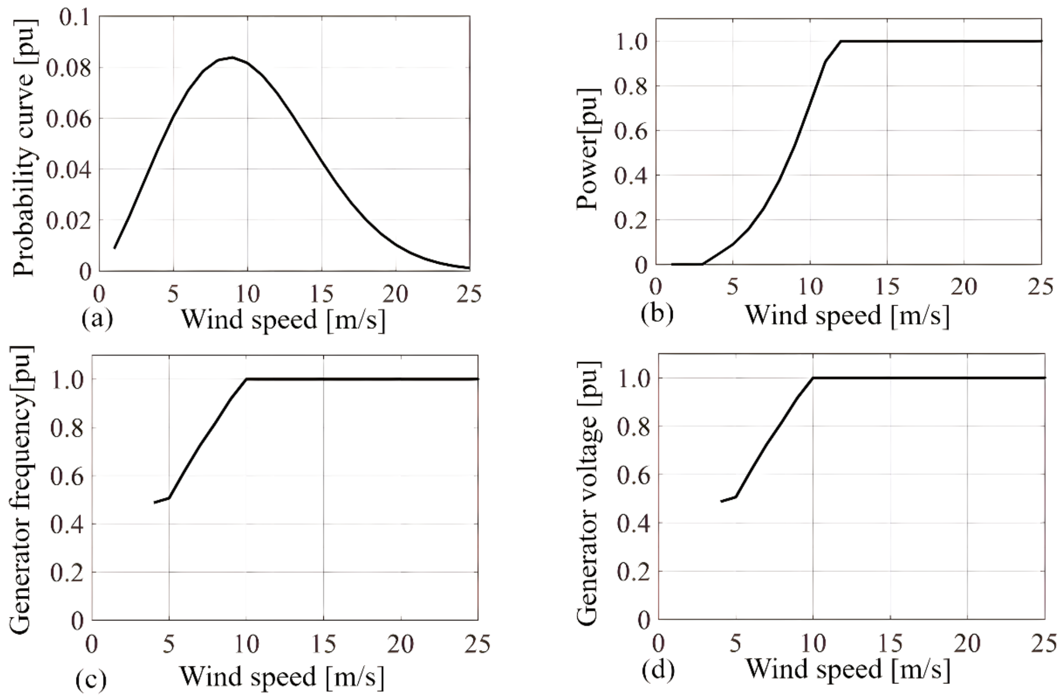


Figure 1-20 Typical wind turbine characteristics. (a) the Weibull wind-speed distribution. (b) wind-speed power curve. (c) wind-speed generator frequency curve. (d) wind-speed generator voltage curve

In this configuration, a permanent magnetic synchronous generator with a high number of poles can be used as a generator, where the generator frequency (f_s) varies in agreement with time-varying wind speed (typically from 10 to 30Hz) [28] [38]. Note that the range of the generator frequency depends on the generator's design. The generator frequency range can be narrower or wider; however, the assumption is made here for simplicity. Figure 1-20 shows the typical wind-speed generator frequency curve, wind-speed generator voltage curve, wind-speed power curve, and the Weibull wind-speed distribution.

In this proposed system, eliminating the dc/dc boost converter and the dc-link LC filter is practical and achievable as the FBMMC phases (Figure 1-13(b)) are built and equipped with many capacitors and inductors and can provide high voltage gain capability and sufficient energy buffering ability [24] [28] [35] [46]. However, one of the issues that emerges from removing the LC filter is a significant current ripple in the dc-link, especially at low generator frequencies [3] [7] [40]. In other word, due to the rectifier, the FBMMC dc side is subjected to high ripple with low frequency in the proposed system; therefore, the FBMMC parameters and control structure must be further optimised to ensure safe and efficient operation.

The dc-link ripple adds extra harmonic components into the FBMMC electrical quantities establishing a new resonance frequency related to the dc-link side in addition to the conventional MMC second-order resonance frequency related to the grid [49] [50]. Therefore, the standard approach to FBMMC parameters' design might not be sufficient to avoid the two resonance points of the proposed system. Furthermore, as will be demonstrated in this thesis, with a proper active control strategy of the FBMMC circulating currents, the dc-link current can be smoothened and the generator current THD improved without an additional inductor in the dc link. In other words, the FBMMC can be controlled to operate as an active dc filter in addition to providing the power transfer to the grid. Moreover, due to the high modularity of the MMCs the grid transformer can be also removed [28] [38].

Furthermore, the influence of the switching process of the MMC SMs on the dc-link voltage will be examined in this thesis. The SMs switching process generates switching-voltage ripple in the dc-link voltage [43] [51] [52] [53]. The switching-ripple in the dc-link voltage influences the rectifier's performance, causing conducted and radiated Electromagnetic interference (EMI) emission [43] [51] [52] [53]. Through optimum design of the carrier displacement angle between the upper and lower arms of the FBMMC, this switching-ripple can be minimised or even eliminated, as will be proposed and demonstrated in this thesis.

As a result, the proposed system offers low cost and size and improved reliability and efficiency.

1.7 Thesis scope and limitation

The main goals of this thesis are as follows: (1) to validate that the FBMMC can be controlled to operate as an active dc filter in addition to transferring power to the grid; (2) to examine the impact of eliminating the dc-link LC filter on the FBMMC's electrical quantities and parameters design, and (3) to analyse the switching-voltage ripple on the dc-link introduced by the FBMMC.

Therefore, the grid code requirements, such as providing and receiving reactive power, having ride-through capability, and having MPPT capability, will be out of the scope of this thesis. However, these grid code compliances have been addressed by many authors. It is widely accepted that MMCs can meet grid code requirements without the need for additional hardware [24].

For instance, authors in [28], [35], and [54] show that the SMs of FBMMC can exchange active and reactive powers with the ac grid under buck and boost mode. The capability of the MMCs to ensure proper operation under unbalanced grid conditions or to have ride-through capability is verified, for example, in [55], [56], and [57]. Many approaches are presented in [58], [59], and [60] for MPPT requirements in PGSC with direct drive configuration.

The PMSG structure and control will be out of the scope of this thesis as well.

The investigation in this thesis considering only unity power factor operation.

The experimental prototype minimum frequency is 15 Hz due to the limitation of the generator that is used. Moreover, no grid emulator is used in the experimental prototype. The ac side of the FBMMC is connecting to a pure resistive load.

1.8 Main novelty and objectives of the thesis

As the size and weight of the required electrical components are limited by the tower area and weight capabilities, a system with a compact size and a low component count is preferable in today's high-power wind turbines. In a wind farm with hundreds of turbines, even a one percent of increase in efficiency across the board can result in significant savings. Therefore, the main contributions of this thesis can be summarized as:

- It proposes a compact system based on the very cost-effective and reliable three-phase diode-bridge rectifier on the generator side (i.e., PGSC) incorporated with FBMMC without passive components in the dc-link. This configuration offers low size and increases the overall reliability of the system.
- It develops an enhanced control strategy for the FBMMC's circulating current suppression to compensate for the absence of dc-link passive components. This means that the system's dc-link current can be significantly smoothened, and the generator's current THD can be significantly improved only through active control optimization. In other words, the FBMMC can be controlled to operate as an active dc filter in addition to providing the power transfer to the grid.
- It develops steady-state analytical mode for the low-frequency harmonics of proposed system. The developed steady-state analytical model is applicable to any three-phase diode rectifier (i.e., with any number of pulses) as the front-end of the FBMMC and for the full operating range (i.e., both buck and boost modes). The developed analytical mode provides the following features:

- It further enhances the understanding of the operational capability of FBMMC under variant and non-ideal dc-link voltage and it shows the influence of that on circulating current, sub-modules (SM) voltage.
- The mathematical formula defining the main circulating current ripple components is established in both the buck and boost modes of the FBMMC operation, and thus their associated resonance inductance can be avoided through suitable arm inductance selection. Thus, for safe and proper operation a new inductance selection guidance will be provided in this thesis.
- The MMC impedance formula related to the dc-link side is found. From that the dc-link current ripple DCM condition can be determined in the early design stage. This provides an easy method to selection a dc-link inductor for any other application if it is need.

- It develops an analytical solution to the high-frequency harmonics spectrum of the dc-link voltage of the FBMMC under both boost and buck operation. This analytical solution shows the influence of the carrier displacement angle between the upper and lower arms in the dc-link switching-ripple. Then the analytical solution is extended to cover the high-frequency harmonic spectrum of the ac side voltage of the FBMMC. From that and under variable dc-link voltage a new displacement angle is presented to achieve a good reduction in high-frequency harmonics on both sides of the FBMMC.

- It develops a switching model in the MATLAB simulation environment and a sub-scale laboratory experimental prototype to validate the proposed system's active dc filter capability, control efficacy, and the developed analytical solution for both low and high frequency components of MMC electrical quantities.

1.9 Chapters organisation

This project is composed of six chapters; each chapter has a related abstract, and an introduction with a sufficient literature review. This thesis' chapters are organised as follows:

- **Chapter 1** emphasises the importance of adopting RES to ensure a clean environment and secure sustainable energy. One of the most common types of RES is wind energy. This chapter provided a brief history of WECS evaluation and growth. The trend of WECS is toward high-power wind turbine units with direct drive technology to significantly reduce the production cost. This chapter provided adequate literature review about different WECS generator and converter technologies. The gearless full-scale (100%) power converter with the employment of multipole PMSG is considered the most promising technology for the foreseeable future. The MMC converter may be the most enabling technology for high-power WECS. This chapter proposes a compact WECS system, based on the MMC and three-phase front-end diode rectifier without a dc-link filter, characterised by low cost and high reliability for high-power wind turbines. It outlines the thesis motivation, literature gap, main objectives, and contributions.

- **Chapter 2** briefly describes the construction and design of the experimental prototype. A generator, rectifier, three-phase FBMMC, resistive load, and OPAL-RT as a controller are the main components of the experimental prototype. An adequate explanation for each of them will be provided in this chapter. It should be noted that the experiment chapter is presented early to avoid unnecessary redundancy, as each following chapter will contain its own experiment results.
- **Chapter 3** gives extensive information on the proposed system's main components. The structure, operation, and analysis of output voltage of the 6 and 12 pulse rectifiers are presented. The necessary details about the FBMMC structure, operation, and optimised control will be revealed. This chapter also verified the effectiveness of the proposed control through the MATLAB simulation and experiment results. It demonstrates

that the FBMMC can function as an active dc filter, smoothing the dc-link and generator phase current ripple.

- **Chapter 4** investigates the influence of dc-link rectifier ripple on the FBMMC parameters. It provides a new average steady-state analytical mode for the proposed system. The analytical model enables an excellent understanding of the system electrical quantity with variant and non-ideal dc-link. The dc-link ripple adds extra harmonic components into the FBMMC electrical quantities establishing a new resonance frequency related to the dc-link side in addition to the conventional MMC second-order resonance frequency related to the grid. The arm inductance needs to be designed to avoid all resonance inductances in the proposed system for safe and efficient operation. The influences of dc-link ripple, boost mode, and buck mode in the arm inductance design are presented. Finally, the developed analytical model is verified by a comparison with MATALB simulation as well as experiment testing.
- **Chapter 5** gives the analytical harmonic spectra model of the dc terminal voltage of the FBMMC with the objective of minimising the dc-link switching-ripple. The analytical harmonic model finds that by optimal selection of the modulation index and the carrier displacement angle between the upper and lower arms the required dc side filter could be minimized or eliminated. Then the study is extended to understand the ac side of the FBMMC (which is already covered in the literature), and from

that a new carrier displacement angle is proposed to achieve optimal harmonic reduction in both the ac and dc sides of MMC. Finally, the developed analytical model is verified by a comparison with MATLAB simulation as well as experiment testing.

- **Chapter 6** draws a conclusion and summarises the primary findings that were revealed. In addition to that, it offers some suggestions for further work.

1.10 List of publications

- Published paper

T. Alzahrani, M. Odavic, S. S. Thakur, and K. Atallah, "Analysis and Control of Grid-Tied Modular Multilevel Converters with a Passive Front-End Rectifier without LC Filter in the DC-Link," 2022 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 1-8, 2022.

- Accepted paper

T. Alzahrani, M. Odavic, S. S. Thakur, and K. Atallah, " Analytical Modelling and Optimization of DC-Link Voltage Harmonic Spectra of Full-Bridge Modular Multilevel Converters for Buck and Boost Operation," in 2023 IEEE Applied Power Electronics Conference and Exposition (APEC)

- Journal paper under progress

T. Alzahrani, M. Odavic, S. S. Thakur, and K. Atallah, " Modelling, and Control Optimization of Grid-Tied Modular Multilevel Converters with a Passive Front-End Rectifier without Passive Components in the DC-Link," in IEEE

T. Alzahrani, M. Odavic, S. S. Thakur, and K. Atallah, " Modelling and Optimization of Voltage Harmonic Spectra of Full-Bridge Modular Multilevel Converters for Variable DC-Link Voltage ," in IEEE

Chapter 2: The laboratory prototype model development and design

2.1 Introduction

This chapter provide an overview of the experimental prototype components. The experimental prototype's main components are Chroma 61703 as a three-phase generator, a three-phase 6-pulse diode bridge rectifier, a three-phase FBMMC, a 10Ω resistive load, and OPAL-RT OP5607 as a controller. Each will be briefly described in the next sections.

2.2 Chroma programmable AC source 61703

Chroma 61703 is a programmable ac source and is used here as a three-phase generator, see Figure 2-1. Chroma has the following specification: output voltage range 0-300 V, output frequency range 15-1200 Hz, output peak current per phase 0-36 A. It should be noted that the minimum frequency that can be obtained from Chroma 61703 is 15 Hz.

Figure 2-1 Experimental prototype generator, Chroma 61703

2.3 Three-phase full-scale converters

The experimental prototype full-scale converters are a three-phase ac/dc/ac converter system. It is based on PGSC incorporated with FBMMC without passive components in the dc-link (i.e., no dc/dc boost converter and LC filter). It is constructed inside a cabinet with a fan cooling method to meet the safety requirements of the EEE department, as seen in Figure 2-2. The main elements are the rectifier and the FBMMC.

Figure 2-2 Full-scale converters of the experimental prototype

2.3.1 Three-phase rectifier

The 6-pulse diode rectifier used in this experimental prototype is shown in Figure 2-3. It is equipped with its own heat sink, and it comes with a maximum output current of 100 A and a maximum repetitive reverse voltage of 1200 V.

Figure 2-3 Experimental prototype three-phase diode bridge rectifier

2.3.2 Three phase FBMMC

Three-phase dc/ac MMC is built in this experimental prototype. Each phase has two arms, an upper arm and a lower arm, and each arm has an inductor (L_{arm}) and two SMs. Each SM has four IGBTs and a capacitor (C_{SM}) in full-bridge converter form. Each arm contains a current sensor to detect arm currents. The dc terminals of each SM are linked to voltage sensors for measuring the capacitor voltages of each SM. The overall block diagram of the MMC experimental prototype is shown in Figure 2-4.

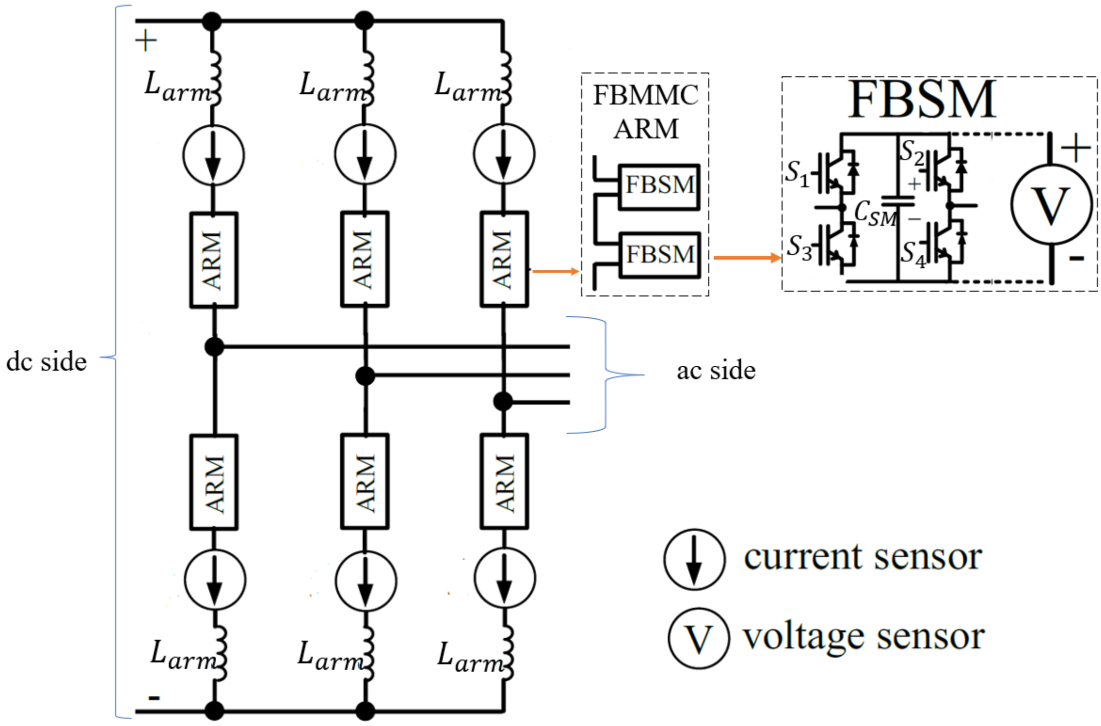


Figure 2-4 Schematic block diagram of the MMC experimental prototype

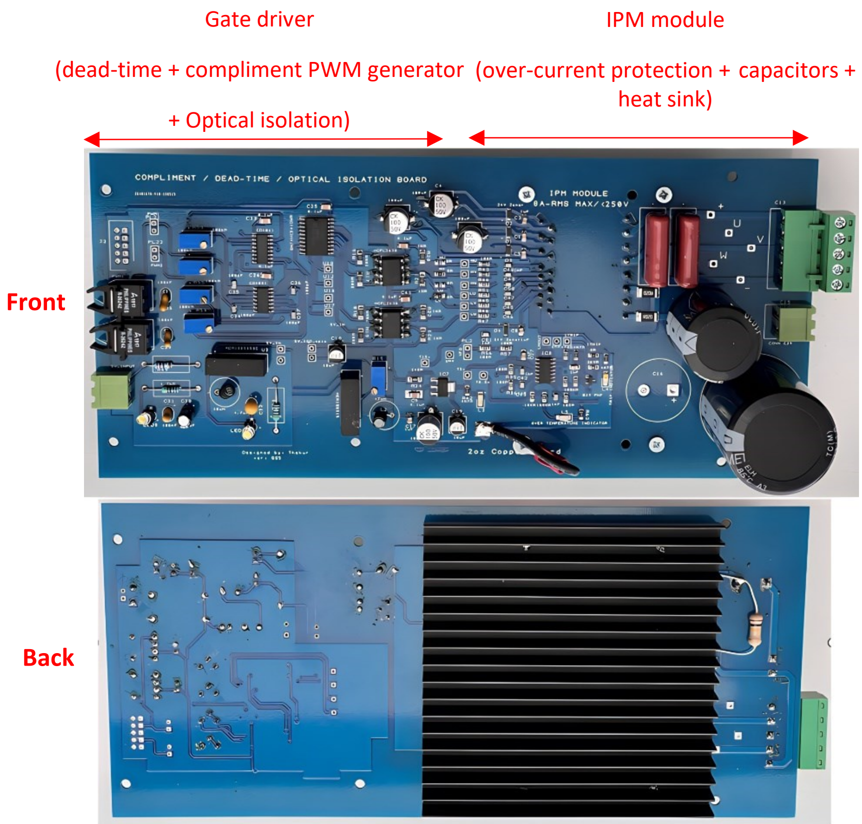


Figure 2-5 PCB design of SM

2.3.3 The SMs of the MMC

In this sub-scale MMC prototype, every single SM is a printed circuit board (PCB) with a customized design, as can be seen in Figure 2-5. The PCB consists of the intelligent power module (IPM) IKCM20L60GD from INFINEON, gate-drive circuit, protection circuit, capacitors, and heat sink.

2.3.3.1 Gate drive circuit

Figure 2-6 shows the gate drive circuit schematic diagram. The primary function of the gate driver circuit is to convert the incoming digital PWM signals into adequate power signals to ensure proper switching for the IGBTs. Here, the gate driver receives two PWM singles (indicated as $S_1, and\ S_2$) for each phase/leg of the SM. Then, an inverter and buffer are required to generate and power the complementary PWM signals of S_1 and S_2. The complementary of S_1 is indicated as S_3, and the complementary of S_2 is indicated as S_4 .

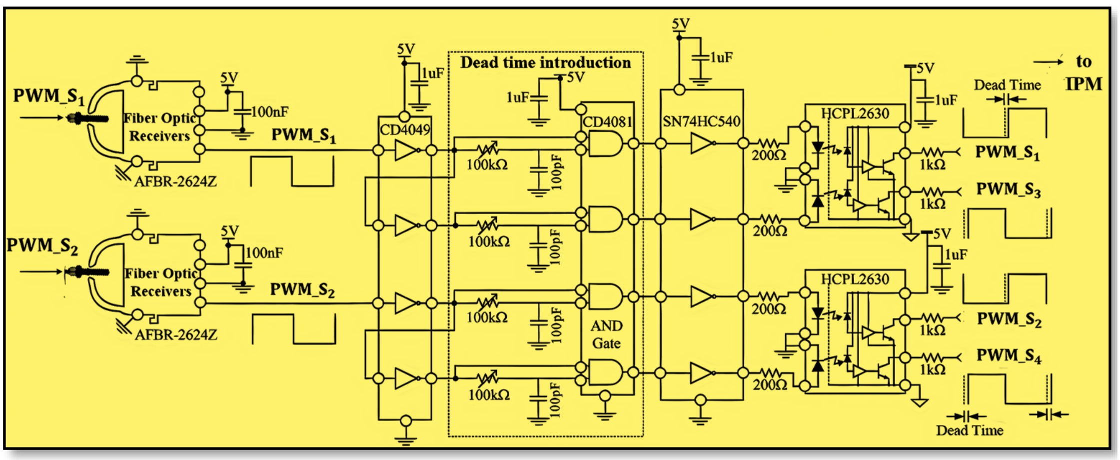


Figure 2-6 Gate driver circuit schematic diagram

To ensure safe and efficient operation, the high-side and low-side IGBTs on the same phase leg of the SM must never be turned ON at the same time, and thus controllable dead-time using an RC network is developed in the gate driver circuit. The dead-time is selected to be 2us in this project. After that, the received PWM signals and their complementary signals are fed to IPM modules through optocouplers for efficient optical isolation. A dc/dc isolated power supply (MER1S0505) is used to power the isolated side of the optocouplers on each PCB. The schematic diagram of the optical isolation circuit is shown in Figure 2-7.

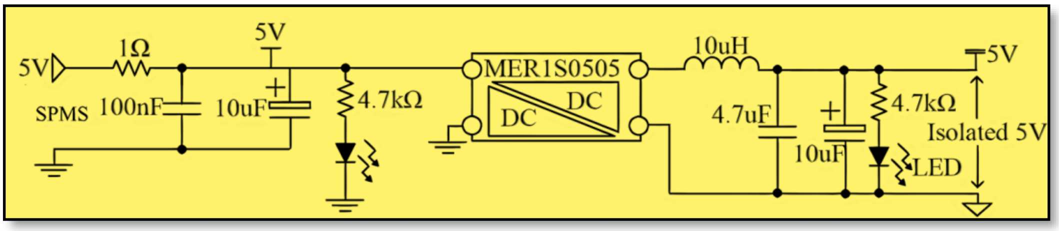


Figure 2-7 Isolated power supply circuit schematic diagram

2.3.3.2 Intelligent power module and over-current protection

The IPM IKCM20L60GD is used in the SMs of the MMC. It has three phases/legs and each leg has two IGBTs. Only two phases/legs are used to work as a full bridge. The IPM module is equipped with a temperature monitor, over-current shutdown, and a bootstrap circuit [61]. The IGBTs of the IPM are powered by the gate driver circuit shown in Figure 2-6. Close to the dc terminals of the IPM, metallized polypropylene film capacitors are installed in order to improve the quality of the PWM SM output and eliminate ringing noise. Moreover, for the

C_{SM}, electrolytic capacitors are connected to the dc terminals of the SM. The C_{SM} value is 0.6mF, however, it can be increased to 2.1mF through an external connector. The schematic diagram of the IPM circuit is shown in Figure 2-8.

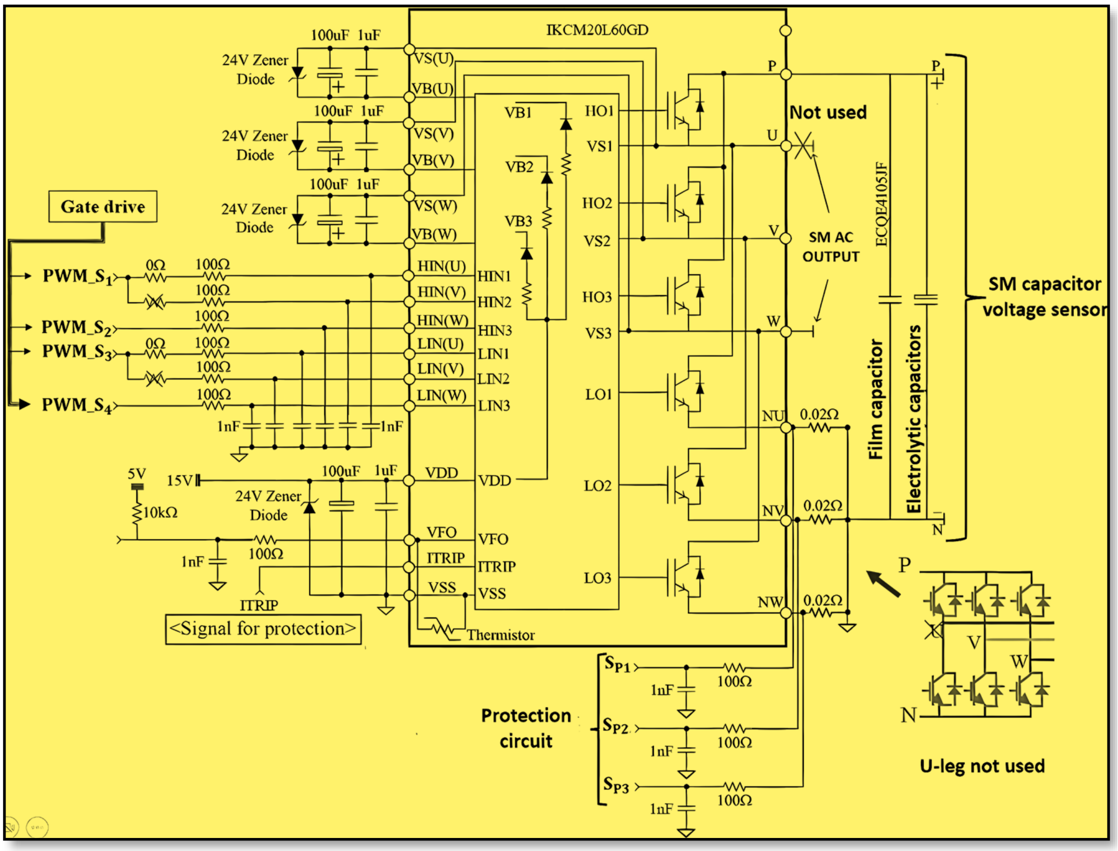


Figure 2-8 IPM circuit schematic diagram[61]

For safe operation, an over-current protection circuit is integrated in the SM PCB (23A Max). In case of high current, via a comparator (LM329), the over-current protection circuit sends a signal to the IPM to completely shut down. The schematic diagram of the over-current protection circuit is shown in Figure 2-9. The IPM and the over-current protection circuit are powered by a dc/dc isolated power supply.

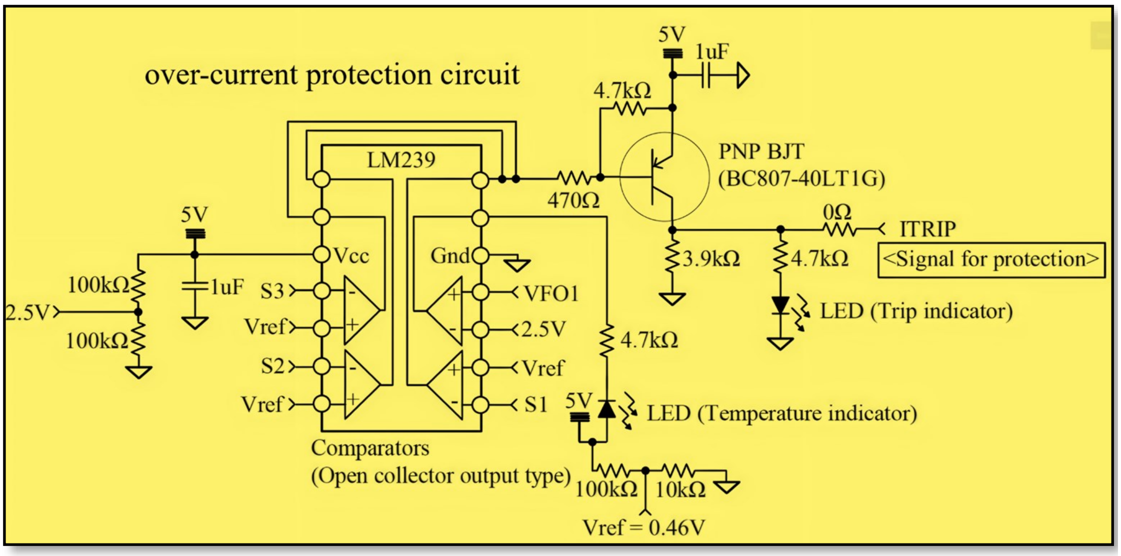


Figure 2-9 Over-current protection circuit schematic diagram[61]

2.3.4 Sensing circuits and conditioning PCB

As mentioned, each arm in the MMC has a current sensor and each SM dc-terminal is connecting to a voltage sensor. The current sensors (LA 55-P) and voltage sensors (LV 25-P) are mounted on a PCB. The current and voltage sensors pick up currents/voltages and turned them into equivalent current signals. Then these current signals are sent to a signal conditioning PCB circuit. The signal conditioning PCB circuit amplifies the current signals and turns them into ones that are compatible with the OPAL-RT analogue input channels, which have an input voltage range of (-16 V, 16 V). The photograph and simplified circuit schematic diagram of the current sensors, voltage sensors, and the signal conditioning PCB are shown in Figure 2-10.

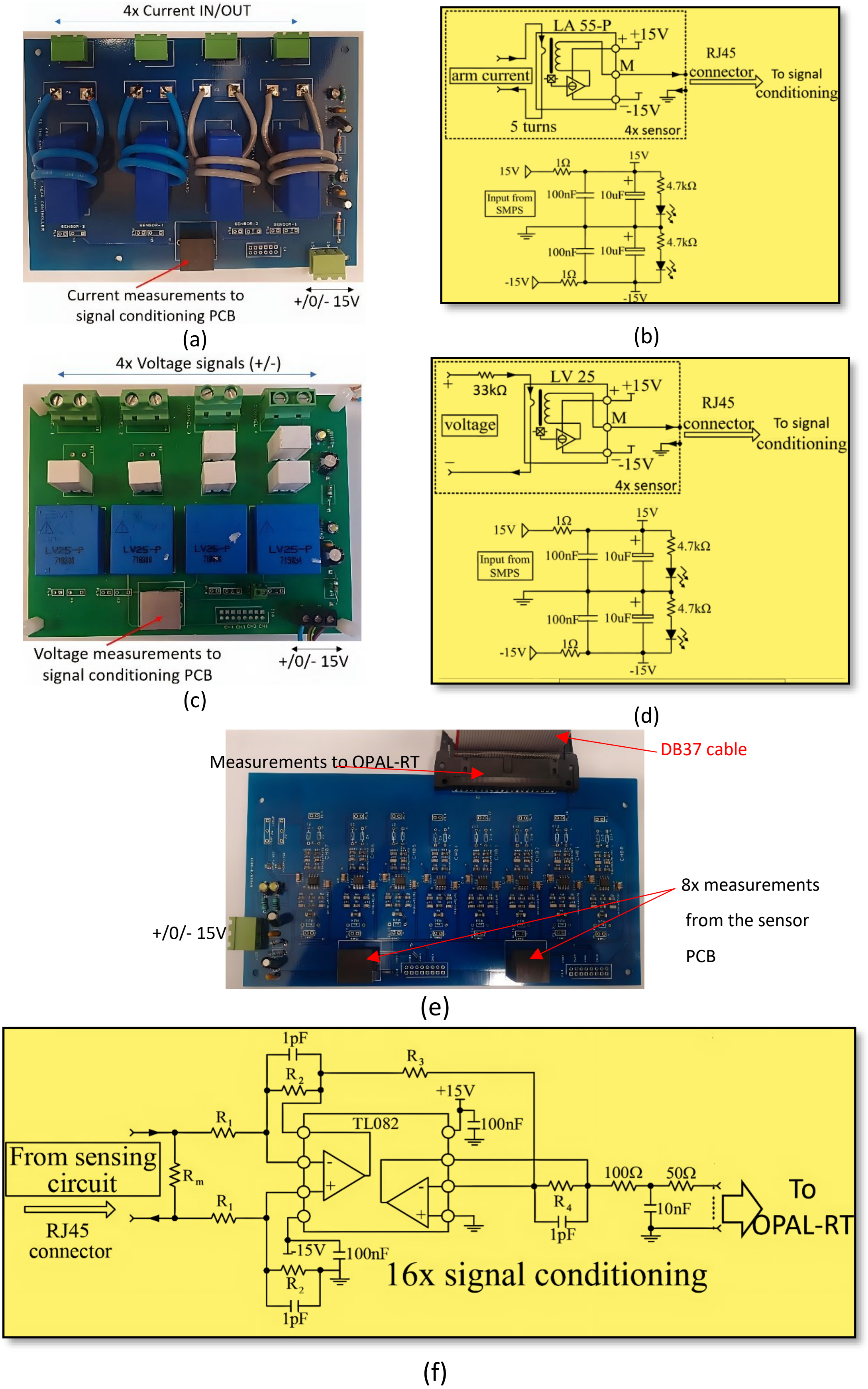


Figure 2-10 Photograph and circuit schematic diagram of (a),(b) current sensors [62], (b), (c) voltage sensors [63], and (e), (f) signal conditioning PCB.

In Figure 2-10(f), the terminating resistor (R_m) for the voltage sensor and current sensor conditioning PCB are set to $R_m = 190\Omega$ and $R_m = 220\Omega$, respectively. Moreover, for the voltage sensor and current sensor conditioning PCB, the dual operational amplifier equivalent gains (R_2R_4/R_1R_3) is set to 2.25Ω, and 1.5Ω, respectively.

2.4 OPAL-RT OP5607

The OPAL-RT OP5607 is the main controller of this experimental prototype. It consists of a 32-core Central Processing Unit (CPU) and a VC707 Virtex-7 FPGA. Ethernet is used to link it to a PC running RT-LAB software. The RT-LAB software is used to create Simulink control models. By doing so, the control can be run and debugged, and the received signals from the prototype sensors can be visualized and tracked. One of the cores of the OPAL-RT OP5607 CPU is used to implement the control algorithm. This core then communicates with the FPGA. The FPGA is then responsible for controlling both the digital and the analogue inputs and outputs. The OPAL-RT OP5607 contains 64 (16x4) digital output channels, 64 (16x4) digital input channels, 16 (16x1) analogue output channels, and 48 (16x3) analogue input channels. All digital output channels are accessible as 16x4, which means four DB37 connectors can set up as PWM output. The overall input and output panel configuration of the OPAL-RT OP5607 are shown in Figure 2-11.

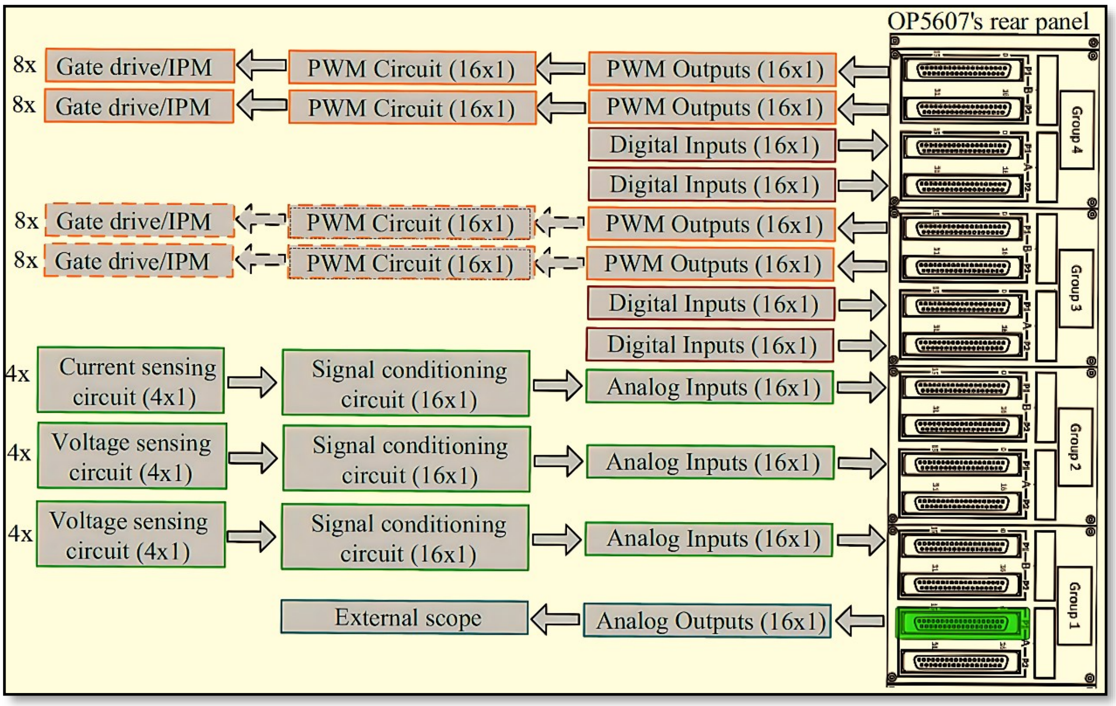


Figure 2-11 Digital and analogue input/output management of OPAL-RT [64]

2.4.1 Pulse width modulation PCB

As the gate driver has an optical PWM input, the OPAL-RT output PWM signals need to be converted to an optical signal to achieve compatibility. This is done through an external PWM PCB, see Figure 2-12 and Figure 2-13. A buffer is used to strengthen the PWM signals, and then the PWM signals are fed into the optical transmitter (TX) AFBR-1624Z.

2.4.2 Control implementation using OPAL-RT 5607

Figure 2-14 represents the entire closed loop control implementation.

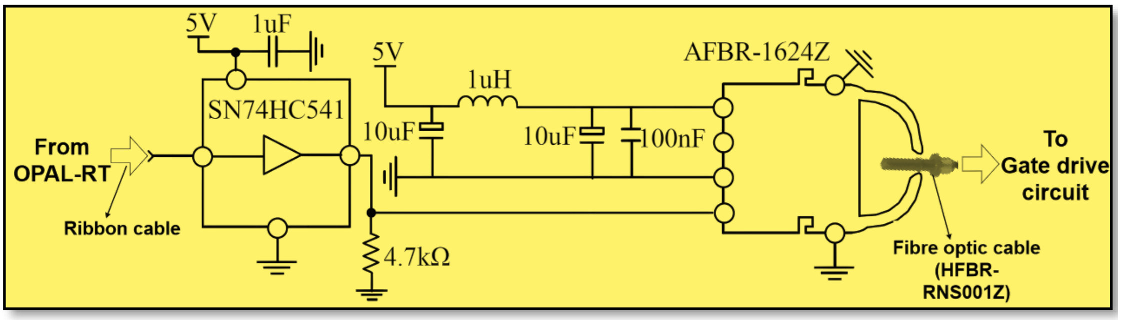


Figure 2-12 PWM optical transmitter (Tx) circuit schematic

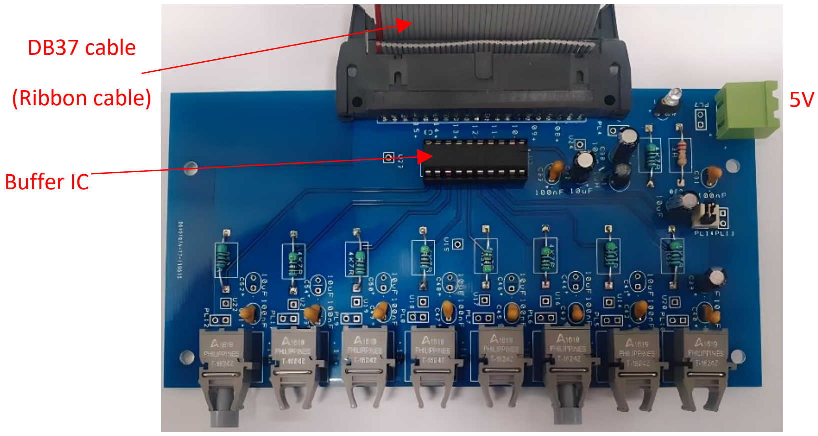


Figure 2-13 Photograph of PWM optical transmitter (Tx) circuit

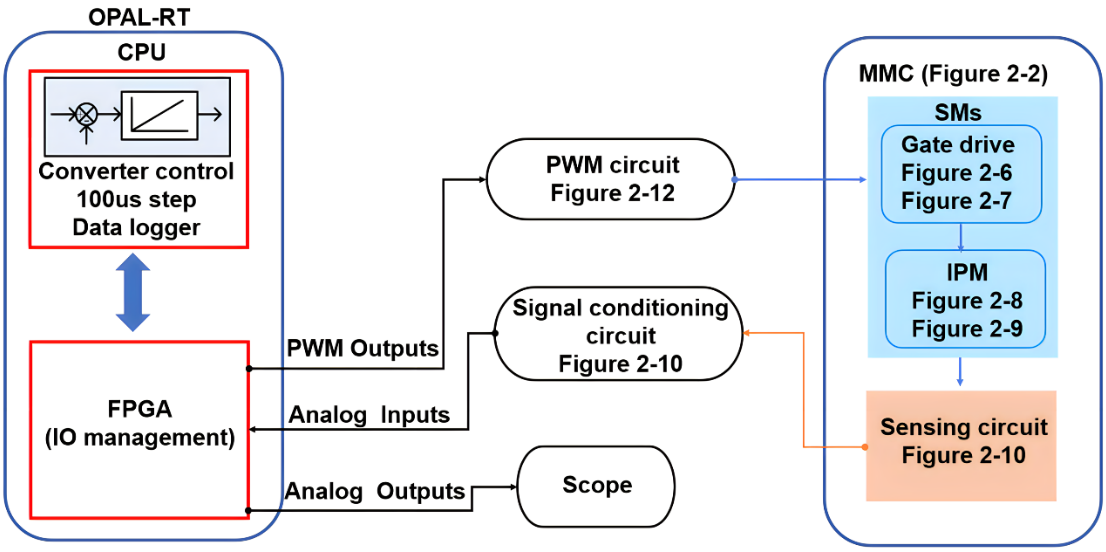


Figure 2-14 The block diagram of the control implementation method

2.5 AC passive resistive load

In this project, the ac side is selected as a 10-ohm resistive load in a star connection.

2.6 Overall system

The photograph and the block diagram of the ac/dc/ac system with passive resistive load is shown in Figure 2-15.

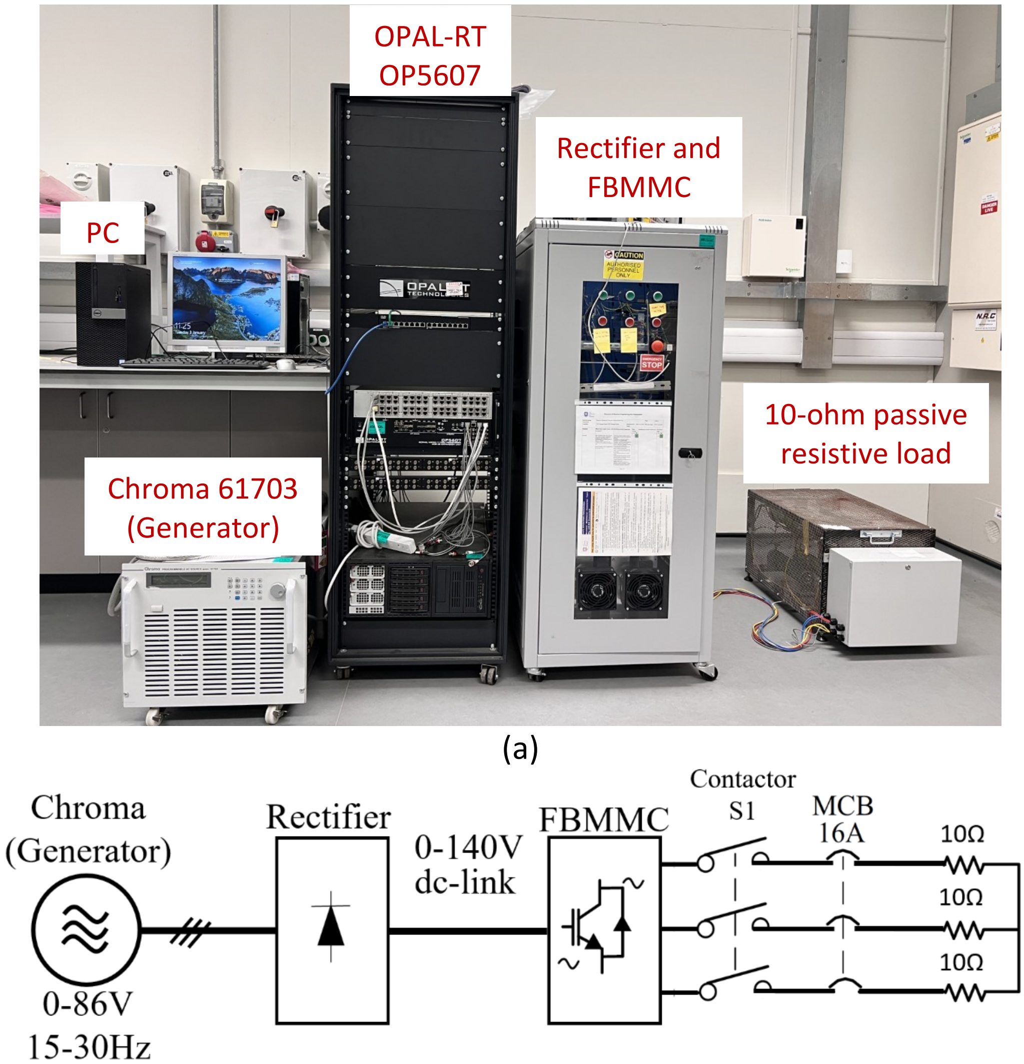


Figure 2-15 Experimental setup (a) photograph, (b) block diagram.

2.6.1 Start-up sequence

The SMs capacitors needs to be safely and gradually charged up before the connection to the ac side to prevent a high-rush current in the system. Because of this, initially, the MMC control power is activated, and the control is enabled via OPAL-RT. Next, the reference for ac modulation is set to zero and the reference for dc modulation is set to 0.25. Then, the generator voltage is gradually increased till the nominal value. By this, The SM capacitor is gradually charged up and follows the dc side voltage. At this point the control of the ac current is activated with zero dq current references. After that, the contactor S1 (Figure 2-15(b)) is closed, and then the current ac references are gradually increased to the required value. By doing this, the start-up sequence is complete. Finally, to bring the system down, nearly opposite steps are taken.

2.7 Summary

This chapter provides an overview of the experimental prototype's design and development. Chroma 61703 is used as a generator and is connected to three-phase diode bridge rectifier. The diode bridge rectifier is connected directly to the FBMMC. The ac side of FBMMC is connected to resistive load.

The three-phase FBMMC is built with two SMs per arm (N=2). Each FBMMC SM has an integrated gate driver circuit, and IPM. The IPM has six IGBTs; four of them are used with electrolytic capacitors to form the FBSM. The PCB is also integrated with deadtime circuit and overcurrent protection circuit. Finally, the different interface circuits, signal conditioning circuits, sensor circuits, and OPAL-RT as a controller are also described briefly.

Chapter 3: Proposed system description, modelling, and control

3.1 ABSTRACT

Large passive components in the dc-link, like capacitors, are a big problem for modern high-power applications in terms of efficiency, maintenance, and reliability. The preceding chapters proposed a system with no passive components in the dc-link that is suited for high-power WECS. This chapter will give the necessary information regarding the operational, structural, and mathematical analysis of the proposed system's primary components. The section then details the proposed control structure, verified via MATALB simulation, and experimental tests. Finally, a summary and proposed WECS configuration will be presented.

3.2 Introduction

In medium and high-power applications such as WECS, a back to back converter (BTBC) configuration or a passive generator side converter (PGSC) (i.e. with diode front-end rectifier) configuration are commonly used [3] [7]. These configurations require large passive component in the dc-link, see Figure 3-1 [3] [7] [65]. However, the passive components are heavy and require a relatively large portion of overall cabinet space, they also limit future converter load integration. Moreover, the dc-link capacitors are considered one of the most prone components to failure [42] [66]. Currently, with the high demand for energy and advancement in power semiconductors technology, the level of power handling capability of the converter has raised substantially. Therefore, any measures to minimize or even eliminate the passive component in the dc-link is considerably beneficial [39] [67] [68].

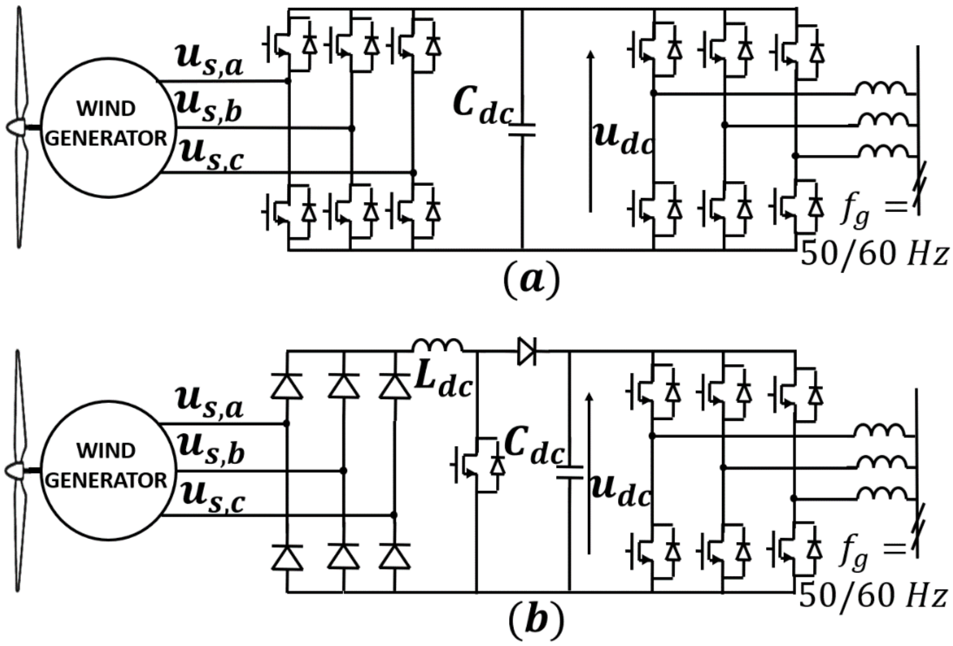


Figure 3-1 Typical WECS incorporating two-level inverter topologies with (a)BTBC, (b) PGSC

However, reducing or eliminating the passive component in the dc-link -with no extra preparation- allows fluctuations in the dc-link, result in an undesired low order harmonics imposed on the system [69] [70] [71]. Many researchers have presented various solutions for reducing or eliminating the passive components in the dc-link in different applications.

With two-level voltage source inverter (VSI) and rectifier (VSR), authors in [39] have presented a PWM approach to eliminate the low order harmonics in the ac side caused by eliminating the dc-link passive component. By replacing the typical sinusoidal reference with a quasi-sinewave reference and kept the triangular carrier, the low order harmonics was efficiently eliminated. The quasi-sinewave magnitude is selected inversely with fluctuation in the dc-side. This method also offers a 33% reduction in the number switching per cycle achieving less switching loss. However, the critical drawback of this method is that the maximum desired fundamental output voltage must restrain at 0.866 from the peak value of the ac side to ensure a proper operation without passive component in the dc-link, and this leads to poor inverter utilization.

An alternative approach based on selective harmonic elimination PWM (SHE-PWM) without the passive components is developed in [67]. The SHE-PWM work through pre-calculating the switching angles to minimize or eliminate a certain order of undesired low order harmonics and keep the fundamental frequency at the desired value. The calculation of these angles is done by numerical method and then stored in a look up-table for on-line implementation [67]. To estimate the dc-link voltage fluctuations within the modulating signal, the modulating signal is divided by the sum of the average value and ripples of the dc-link voltage. The method achieves a significant reduction in the number of switching per cycle and a successful elimination for the low order harmonics. On the other hand, this method suffers from several drawbacks; firstly, it is more complex to consider analytically the optimal angles for all possible operating condition [68]. Next, this solution is only fit for limited variation in the dc-link, once the variation exceeds a certain value the output fundamental component is severely affected. Finally, this method, cannot suppress the 10th harmonic component and above in the ac side [67].

In [69] an approach that includes a combination of a current source rectifier (CSR) and two-level VSI to reduce the size of the dc-link capacitor. In the standard mode operation of BTBC configuration, the VSR is used to maintain dc-link voltage at a constant value and the modulation index of the VSI is adjusted to control the output voltage control. The VSI modulation index has an inverse relationship with the dc-link current ripple [69]. By known this, if the CSR is employed instead of the VSR, the dc-link voltage can be kept below threshold value and the VSI modulation index is selected at the maximum value [69]. This method achieves a 25% reduction in the dc-link capacitors size by mean of reducing the dc-link current ripple [69]. However, this method still needs a dc-link capacitor and it equips with a large dc-link inductor [3].

Authors in [71] have presented an optimum design for the dc-link voltage loop control to minimize the voltage variation in the dc-link during wind speed variant. The dc-link voltage loop control of the VSI is developed to be fast enough, its input current will rapidly follow the magnitude of the VSR output current, then the dc-link voltage variation is minimized. This result to a 30% reduction to capacitor size in the dc-link. This is accomplished by developing a relationship correlates the variation of the dc-link voltage with the VSR output current. Then, a PI controller used to maximize the voltage-loop speed and provide adequate stability [71].

However, the two-level VSR produces a sixth harmonic of the generator fundamental frequency in the dc-link which the proposed voltage loop cannot minimize or eliminate. Thus, although this method can achieve a good reduction into the dc-link capacitor, the dc-link capacitor is still needed.

Another suggested arrangement is developed to minimize the dc-link capacitor in [72]. A parallel two-level VSRs is used in the generator side. This method found that, by shifting the gate control signals between the VSRs by a certain value, the dc-link current ripple can be reduced. Two PWM method is presented, carrier based PWM and space vector modulation (SVM). This paper provides further optimization to select the right phase shifting angle under different operation condition. It achieves up to 45% reduction in the dc-link current ripple with SVM and up to 54% reduction in the dc-link current ripple with carrier based PWM. This led to a good reduction in the size of the dc-link capacitors. However, using a parallel two-level VSR increase the system cost, size, and control complexity [3]. Moreover, this arrangement generates a circulating current flowing in both generator side and grid-side converter which leads to increase the power loss and degrading the generator performance [3].

Nowadays, MMCs are standing to offer the absolute solution for many disadvantages comes with conventional two-level or three-level converters [46]. With BTBC configuration using MMCs as rectifier and inverter, authors in [48] shows that the passive components in the dc-link side is not needed. However, For WEGS, the power flow is unidirectional, as they only supply power to the grid, not the other way around. This means, applying BTBC configuration is an overloaded method, and increase cost, size, and control complicity [3] [28].

This thesis proposes that ,for WECS the very cost-effective and reliable three-phase diode-bridge rectifiers on the generator side (i.e., PGSC configuration) can be used with FBMMC as an inverter instead of the conventional two/three-level inverter, see Figure 1-19. In this proposed system , the LC filter and the dc/dc boost converter in the dc-link can be removed as the FBMMC provides high voltage gain capability, and its phases are built and equipped with many capacitors and inductors. Furthermore, as will be demonstrated in this thesis, with a proper active control strategy of the FBMMC circulating currents, the dc-link current can be smoothened and the generator current THD improved without an additional inductor in the dc link. In other words, the FBMMC can be controlled to operate as an active dc filter in addition to providing the power transfer to the grid. Moreover, due to the high modularity of the MMCs the grid transformer can be also remove [28]. As a result, the proposed system offers the low cost and size and improved reliability and efficiency.

Further detail of the proposed system, along with simulations and experimental tests, will be provided in the following sections.

3.3 Three phase 6-pulse diode bridge rectifier

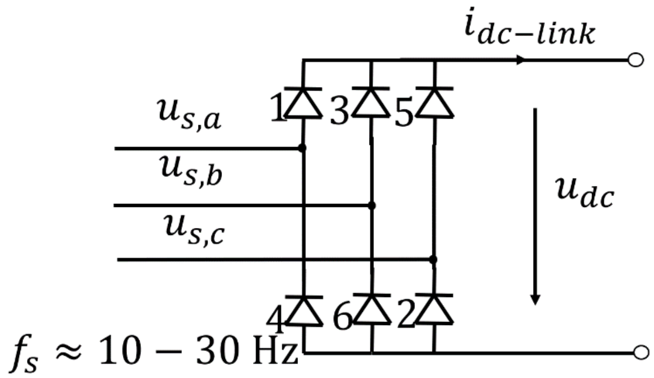


Figure 3-2 Schematic block diagram of the 6-pulse rectifier

The configuration of the 6-pulse uncontrolled diode bridge rectifier is shown in Figure 3-2. It is commonly used for high-power applications due to its simplicity, reliability, and efficiency [7]. The dc-link side, or in other words, the output of the rectifier would have 6-pulses per cycle ($P = 6$) related to the rectifier input frequency f_S. The conduction angle is $2\pi/3$ in each diode, and the diodes conduction sequences are 12, 23, 34, 45, 56, and 61, as numbered in Figure 3-2 [73]. In Figure 3-2, $u_{s,a}, u_{s,b}$ and $u_{s,c}$ are the input voltages of the rectifier and they can be expressed as:

$$\begin{aligned} u_{s,a} &= \mathrm{U}_s \cos(\omega_s t) \\ u_{s,b} &= \mathrm{U}_s \cos(\omega_s t - 120) \\ u_{s,c} &= \mathrm{U}_s \cos(\omega_s t - 240) \end{aligned} \tag{3.1}$$

Where U_s is the amplitude of rectifier input phase voltage

3.3.1 The 6-pulse diode bridge rectifier output analysis

For the sake of simplicity, the diodes are assumed to have zero forward voltage drop and no reverse current. Moreover, it is assumed that the rectifier is connected to a purely resistive load, such that the load voltage and the load current have similar waveforms. Thus, the rectifier typical output voltage and current ($i_{dc-link}$) waveforms in time domain and frequency domain are shown in Figure *3-3*.

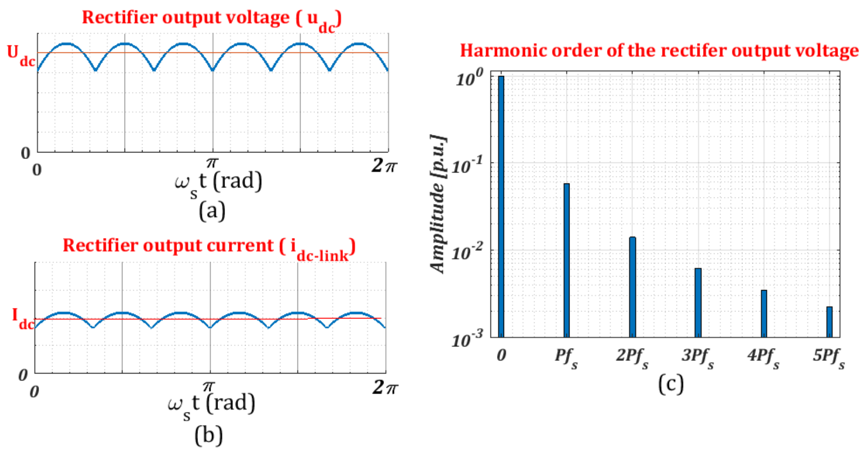


Figure 3-3 Typical rectifier output waveform (for this case P=6), (a) rectifier output voltage waveform, (b) rectifier output current waveform, and (c) rectifier output voltage in frequency domine

The 6-pulse rectifier converts the input ac waveform into a dc waveform with 6-pulse ripple. The general rectifier output voltage u_{dc}, with any number of output voltage pulses P, can be expressed as:

$$u_{dc} = \mathrm{U}_{dc} + \sum_{i=1}^{\infty} u_{Pif_s} \tag{3.2}$$

Where U_{dc} is the dc component and u_{Pif_s} refers to the ripple components of the rectifier output voltage. i is the harmonics order (i.e., $i = (1,2,,3 \ldots \infty)$, and the most dominant ripple is found at Pf_s. The rectifier output voltage ripple components u_{Pif_s} can be expressed as:

$$u_{Pif_s} = \mathrm{U}_{Pif_s} \cos\left(Pi\omega_s t + \theta_{s_i}\right) \tag{3.3}$$

Where U_{Pif_s} is the amplitude of rectifier ripple components and θ_{s_i} is the related phase angle. The dc-link voltage is a result of the line-to-line input voltage (i.e., $\sqrt{3}U_S$) of the rectifier as can be seen in Figure 3-4.

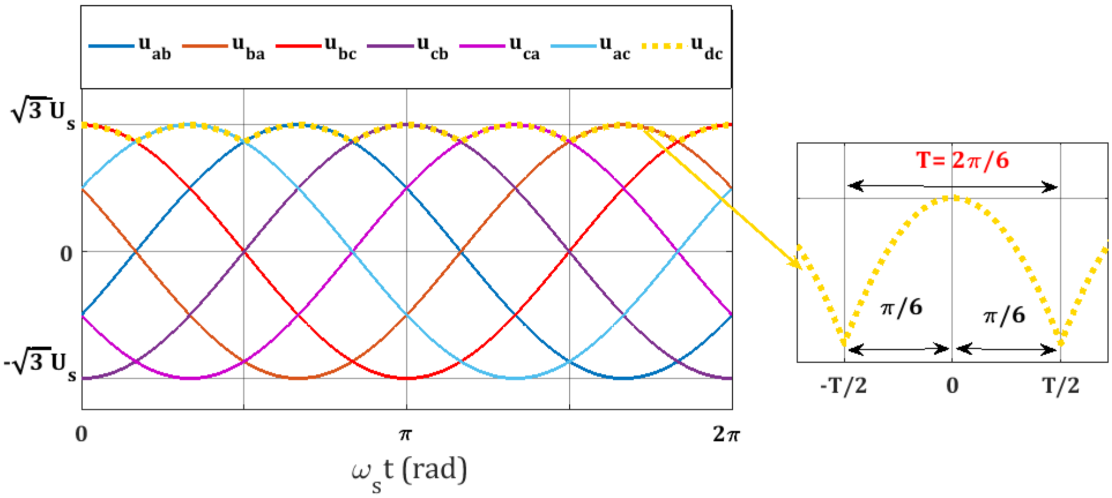


Figure 3-4 6-pulse rectifer input and output voltages

The dc-link ripple components of the rectifier output voltage can be found through Fourier series analysis; equation (3.4) and (3.5) shows the general Fourier series synthesis equation for the amplitude and phase angle of the rectifier output voltage, respectfully [74].

$$x(t) = a_0 + \sum_{i=1}^{\infty} a_i \cos(2\pi f i t) + \sum_{i=1}^{\infty} b_i \sin\left(2\pi f i t\right) \tag{3.4}$$

$$\theta_{ri} = -\tan^{-1}\left(\frac{b_i}{a_i}\right) \tag{3.5}$$

Where the coefficient a_0 represent the dc component, and a_i and b_i are coefficients of the cos and sine components, respectively [74] [75] [76]. f is the rectifier input voltage frequency. θ_{ri} is the phase shift angle of the i^{th} component. The waveform of output voltage of the rectifier is considered even periodic function, this means the b_i (sin) coefficients of the rectifier output voltage are always zero [74]. This make the θ_{ri} is always zero as well, as seen in equation (3.5) [74].The Fourier series coefficients are expressed as [74]:

$$a_0 = \frac{1}{\mathrm{T}}\int_{\frac{-T}{2}}^{\frac{T}{2}} \mathrm{x(t)}\, dt \tag{3.6}$$

$$a_i = \frac{2}{\mathrm{T}}\int_{\frac{-T}{2}}^{\frac{T}{2}} \mathrm{x(t)}\cos\left(\frac{2\pi it}{T}\right)\, dt \tag{3.7}$$

$$b_i = \frac{2}{T}\int_{\frac{-T}{2}}^{\frac{T}{2}} x(t)\, sin\left(\frac{2\pi it}{T}\right)\, dt \tag{3.8}$$

From Figure 3-4 and equation (3.6) the dc component of the rectifier output voltage can be found as:

$$U_{dc} = \frac{2}{\mathrm{T}}\int_{0}^{\frac{T}{2}} \sqrt{3}\mathrm{U}_s \cos(\omega_s t)\, d(\omega_s t) = 1.654 \cdot \mathrm{U}_s \tag{3.9}$$

Where $T = \frac{2\pi}{6}$, as the dc-link voltage has 6-pluses per cycle.

Again, from Figure 3-4 and equation (3.7), Fourier series analysis is used to establishes a general equation describing the relation between U_s and each ripple amplitude of the rectifier output voltage U_{Pif_s}, as below:

$$U_{Pif_s} = \frac{4}{T}\int_0^{\frac{T}{2}} \left(\sqrt{3}U_s \cos\left(\frac{2\pi t}{6T}\right) \times \cos\left(\frac{2\pi i t}{T}\right)\right) dt \tag{3.10}$$

through using the trigonometric identities as below

$$\cos(A)\cos(B) = \frac{\cos(A+B) + \cos\,(A-B)}{2} \tag{3.11}$$

Equation (3.10) can be simplified as:

$$U_{Pif_s} = \frac{2\sqrt{3}U_s}{T}\left(\int_0^{\frac{T}{2}} \cos\left(\frac{2\pi t}{6T} + \frac{2\pi i t}{T}\right)\, dt + \int_0^{\frac{T}{2}} \cos\left(\frac{2\pi t}{6T} - \frac{2\pi i t}{T}\right)\, dt\right) \tag{3.12}$$

through, solving equation (3.12), the general equation that represent any ripple amplitude of the rectifier output voltage can be expressed as:

$$U_{Pif_s} = \frac{6\sqrt{3}U_s}{\pi} \times \left(\left(\frac{\sin\left(\frac{\pi + 6i\pi}{6}\right)}{1+6i}\right) + \left(\frac{\sin\left(\frac{\pi - 6i\pi}{6}\right)}{1-6i}\right)\right) \tag{3.13}$$

Therefore, from equation (3.13), U_{Pf_s}, U_{2Pf_s}, U_{4Pf_s}, and U_{4Pf_s} can be found as:

$$U_{Pf_s} = 0.09451U_s \tag{3.14}$$

$$U_{P2f_s} = -0.02313U_s$$

$$U_{P3f_s} = 0.01024U_s$$

$$U_{P4f_s} = -0.00575U_s$$

As stated, equation (3.14) show that the most dominant ripple component of the output voltage of the rectifier is found at a frequency of Pf_s. It can be observed that as the order of the harmonics increases, the amplitude decreases significantly. In addition, according to equation (3.14), the 6-pluse diode bridge rectifier may be better suited for medium to low-voltage applications. This is because the dc-link voltage ripple components are defined by the amplitude of the rectifier input phase voltage.

3.4 Full-bridge modular multilevel inverter

3.4.1 Structure and operation

The typical configuration of the FBMMC is shown in Figure 3-5, where each phase of the three-phases structure is identical. The phase consists of two arms, upper arm (up) and lower arm (low), where each arm has N full bridge submodules (FBSMs) and one inductor (L_{arm}) in series connection. The arms inductors in one leg can be realized as a single coupled inductor or two non-coupled inductors in each arm. It is necessary to compensate for the voltage interactions between the arms, and reduce the ripple in the arm currents (i_x^r), where r refers to the {up or low} arm, and x denotes phases a, b, or c. The value of the arm inductance should be selected by considering the grid inductance and relevant modes of converter operation (e.g. boost and/or buck modes) to ensure the best performance of the converter concerning the circulating currents ($i_{cir,x}$) [77] [78] [79]. Here, two non-coupled inductors in each arm are used for this work.

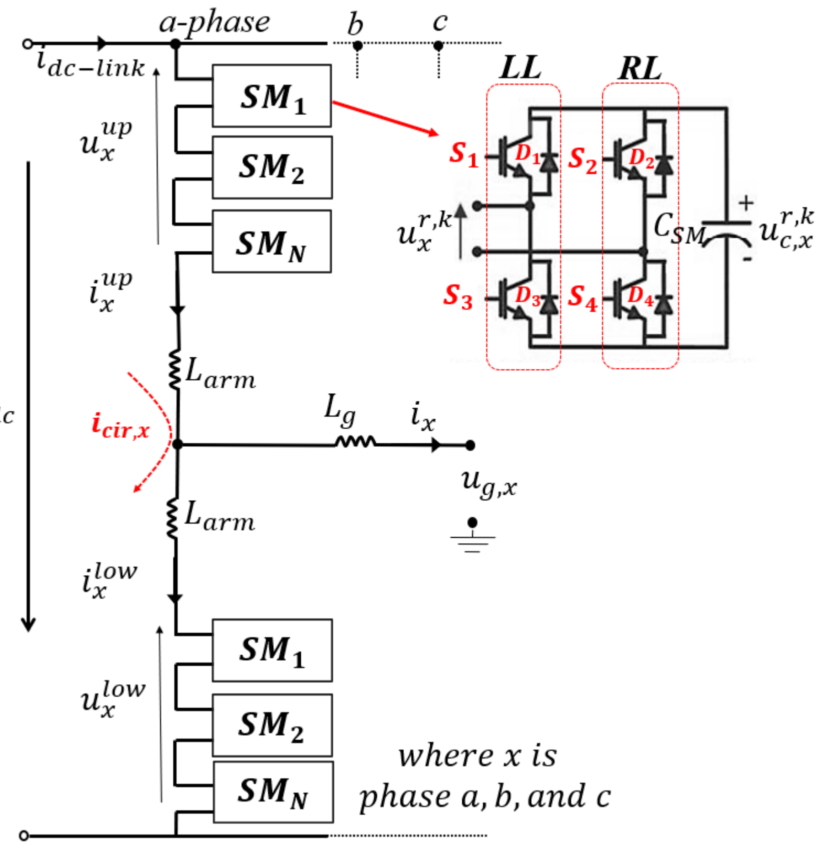


Figure 3-5 Schematic block diagram of FBMMC

The submodules (SMs) are built of H-bridge circuits consisting of four insulated gate bipolar transistor (IGBT) switches (S_1, S_2, S_3, S_4) with anti-parallel diodes (D_1, D_2, D_3, D_4) and capacitor (C_{SM}). By means of available switching combinations, each SM can produce positive, negative and zero (i.e., SM is bypassed) voltages and at the ac terminal of the FBSMs ($u_x^{r,k}$). Here k is the k^{th} SM ($k = \{1,2, \dots, N\}$ in arm r and phase x.

The positive voltage state is produced when the IGBT switches S_1 and S_4 are in on-state and S_2 and S_3 are in off-state. In this switching state, the C_{SM} is charged when the arm current runs in the positive direction (as denoted in Figure 4-6), and it is discharged when the arm current runs in the negative direction.

The negative voltage is produced when the IGBT switches S_1 and S_4 are in off -state and S_2 and S_3 are in on-state. In this case, the C_{SM} is charged when the arm current runs in the negative direction, and it is discharged when the arm current runs in the positive direction.

Finally, the zero-voltage state occurs when the IGBT switches S_1 and S_2 are on-state (while S_3 and S_4 are off) or S_3 and S_4 are in on-state (while S_1 and S_2 are off). Table 3-I and Figure 3-6 summarize all possible switches combinations of FBSM.

In the FBMMC, The SM's capacitor act as a dc source and its average voltage value (U_c^0) need to be maintained at the desired level during different operation (i.e., boost and back mode)[28]. The number of SMs defines the number of the FBMMC output levels. Thus, using a high number of SMs can provide high quality output voltage and smooth current waveform without distortion [26] [80].

Table 3-I All potential switching combinations of the SM IGBT[81]

Figure 3-6	switching patterns				$u_x^{r,k}$	Arm current		SM capacitor state
	S_1	S_2	S_3	S_4		direction	path	
(a)	1	0	0	1	$+u_{c,x}^{r,k}$	i_x^r>0	D_1, D_4	charging
(b)	1	0	0	1	$+u_{c,x}^{r,k}$	i_x^r<0	S_1, S_4	discharging
(c)	0	0	1	1	0	i_x^r>0	S_3, D_4	unchanged
(d)	0	0	1	1	0	i_x^r<0	D_3, S_4	unchanged
(e)	1	1	0	0	0	i_x^r>0	D_1, S_2	unchanged
(f)	1	1	0	0	0	i_x^r<0	S_1, D_2	unchanged
(g)	0	1	1	0	$-u_{c,x}^{r,k}$	i_x^r>0	S_2, S_3	discharging
(h)	0	1	1	0	$-u_{c,x}^{r,k}$	i_x^r<0	D_2, D_3	charging

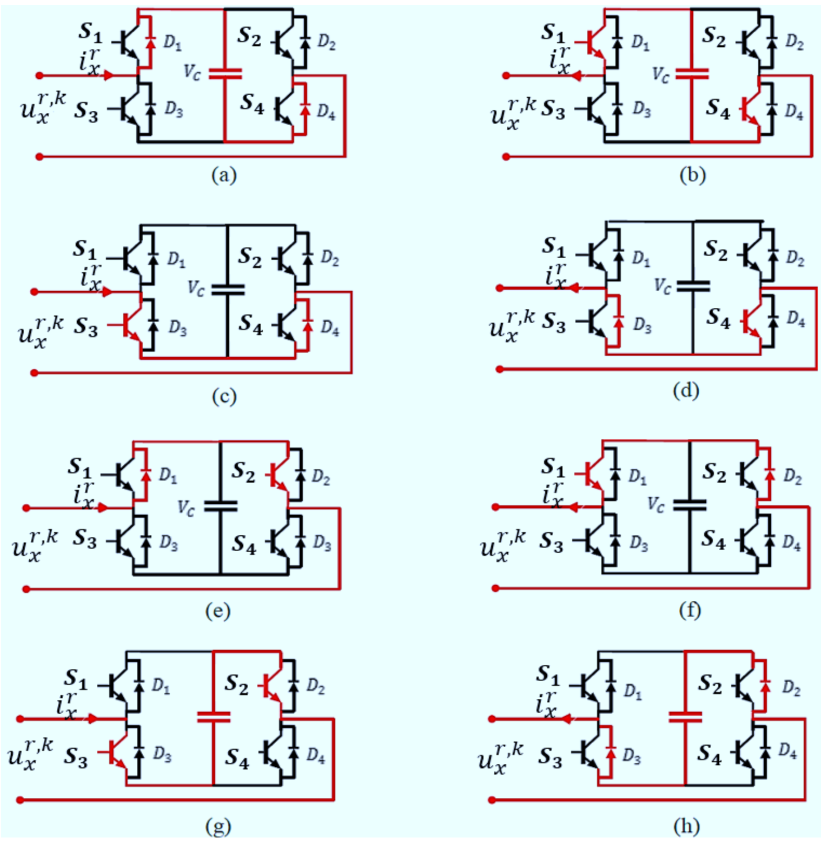


Figure 3-6 i_x^r path direction under all switching combinations of FBSM[81]

In Figure 3-5, each phase of the FBMMC is tied to the grid through the ac side inductor L_g. i_x and $u_{g,x}$ are the current and voltage of the grid, respectively.

$i_{dc-link}$ and u_{dc} are the dc-link current and voltage of the FBMMC respectfully. The circulating current consists of a dc component responsible for transferring the power to the grid and additional ripple components that cause power loss. Although the circulating current ripple components have no direct influence on the converter's ac-side, they cause a power loss and degrade the system performance and efficiency [82] [35]. The ripple components of the circulating current are generated by the interaction components of the capacitor voltage ripple and the switching function in the output voltage of each SM, where these harmonic components are in phase in the upper and lower arms [83]. For the case of pure dc voltage at the MMC input (dc) terminals, the ripple of the circulating current is largely defined by the dominant second order harmonic component (regarding the grid frequency) [35] [77] [82] [83].

3.4.2 Boost mode features of the FBMMC

More recent attention has been focused on the FBMMC operation in boost mode. The boost mode operation provides additional beneficial features to the FBMMC such as reduced SMs' capacitor size and improved output voltage quality[36] [84]. The FBMMC works in buck mode when their SMs are operated to produce only positive and zero voltage states like in the HBMMC, whereas, in the boost mode operation the FBMMC SMs provide extra negative voltage states to compensate the reduction in the dc-link voltage or increase in the output voltage of the inverter [28] [46] [84].

In the MMCs, the upper arm voltage (u_x^{up}) and lower arm voltage (u_x^{low}) define the range of the amplitude of the MMC phase voltage (U_m) [28]. For the FBMMC, the amplitude of output phase voltage is expressed by the following equations [28].

$$-NU_c^0 \leq u_x^{up} = \frac{U_{dc}}{2} - U_m \leq +NU_c^0 \tag{3.15}$$

$$-NU_c^0 \leq u_x^{low} = \frac{U_{dc}}{2} + U_m \leq +NU_c^0 \tag{3.16}$$

Equations (3.15) and (3.16) show that the output voltage of the FBMMC has a high level of independence from the dc-link voltage. Theoretically, it can achieve twice its dc-link voltage value. Figure 3-7 shows the arms' voltage of FBMMC in buck and boost modes, where the FBMMC operates in buck mode when $U_{dc} = 2U_m$ and goes to the boost mode when U_{dc}<$2U_m$.

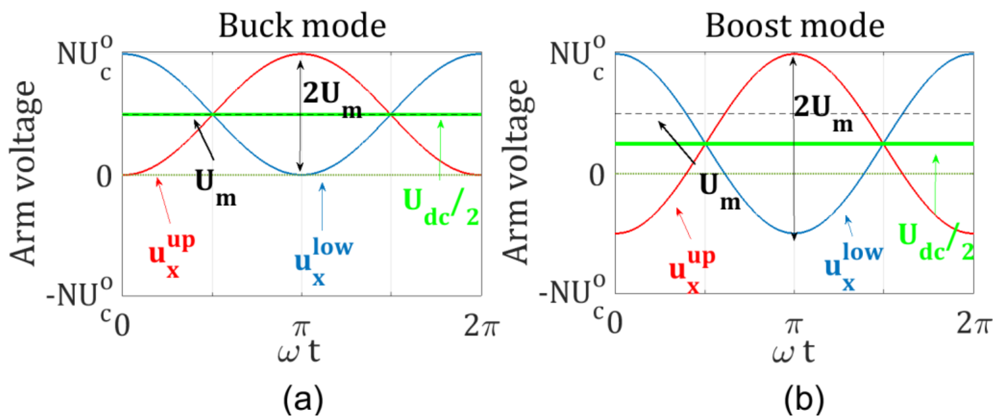


Figure 3-7 Arm voltages of the FBMMC (a) buck mode, (b) boost mode

Therefore, unlike the conventional two/three level inverter, with the boost capability of the FBMMC, no extra boost converter is required in the dc-link to ensure proper power transfer to the grid, as the FBMMC can provide both boost and buck functions keeping the system synchronized to the grid regardless of the dc-link voltage level [28].

3.4.3 Modulation signal

In Figure 3-5, under ideal FBMMC three phase balancing, identical SMs in each arm, and by ignoring the voltage drop in the arm inductor, the output voltage of each SM in upper arm and lower arm can be found through Kirchhoff's voltage-law as:

$$u_x^{up,k} = \frac{1}{\mathrm{N}}\left(\frac{u_{dc}}{2} - U_m \cos(\omega t + \theta_x)\right) \tag{3.17}$$

$$u_x^{low,k} = \frac{1}{\mathrm{N}}\left(\frac{u_{dc}}{2} + U_m \cos(\omega t + \theta_x)\right) \tag{3.18}$$

Moreover, the SM capacitor voltage ($u_{c,x}^{r,k}$) can be expressed as [51] [83]:

$$u_{c,x}^{r,k} = U_c^0 + \sum_{j=1}^{\infty} u_{c,j}^r \tag{3.19}$$

Where $u_{c,j}^r$ is the ripple component of the SM capacitor voltage. The standard design for the SMs capacitors is to limit its voltage ripple to ~10% [83]. For the sake of simplicity and under the standard design of SMs capacitors, the voltage ripple across the SM capacitor can be neglected (i.e., $u_{c,x}^{r,k} \approx U_c^0$) [51] [83]. Thus, the modulation signal of each FBSM in the upper arm ($M_x^{up,k}$) and lower arm ($M_x^{low,k}$) can be presented as:

$$M_x^{up,k} = \frac{u_x^{up,k}}{U_c^0} \quad (3.20)$$

$$M_x^{low,k} = \frac{u_x^{low,k}}{U_c^0} \quad (3.21)$$

From equations (3.17) to (3.21) the modulation signal of each FBSM can be represented as:

$$M_x^{up,k} = \frac{\mathrm{M_{dc}}}{2} + \frac{M_{ac}}{2}\cos(\omega t + \theta_x) \quad (3.22)$$

$$M_x^{low,k} = \frac{\mathrm{M_{dc}}}{2} - \frac{M_{ac}}{2}\cos(\omega t + \theta_x) \quad (3.23)$$

Where, M_{ac} defines and regulates the SMs output voltage and M_{dc} defines and adjusts the dc-offset of the SM output voltage [85]. The M_{ac} and M_{dc} values are varying regarding to the variation of dc-link voltage level [85],as seen in Figure 3-8.

In Figure 3-8, the relation between M_{ac} and M_{dc} is explained by M_{pk}, where M_{pk} is the peak value of the modulation signal, its value is limited to $0 < M_{pk} \leq 1$, and must be as high as possible for better device utilization

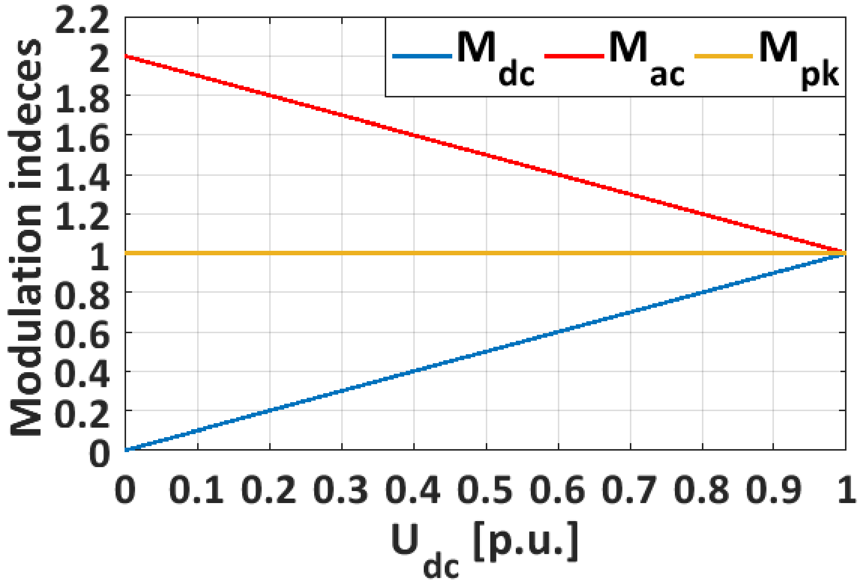


Figure 3-8 Modulation indexes range under different dc-link voltage level

The M_{pk}, M_{ac} and M_{dc} are defined as below:

$$M_{dc} = \frac{U_{dc}}{NU_c^0}$$

$$M_{ac} = \frac{2U_m}{NU_c^0} \tag{3.24}$$

$$M_{pk} = \frac{\mathrm{M_{dc}} + M_{ac}}{2}$$

Finally, the average capacitor voltage of the SM is regulated to ensure better performance and low SMs voltage stress, and the average SM capacitor voltage is given as [85]:

$$U_c^0 = \frac{2U_m + U_{dc}}{2NM_{pk}} \tag{3.25}$$

3.4.4 Detail Description of Phase shift carrier-PWM for the FBMMC

The FBMMC SMs can be either controlled by unipolar modulation method or polar modulation method. The unipolar modulation method, Figure 3-9, is selected in this work as it has higher effective output switching frequency, less radiated EMI emission, and less insulation requirement [86]. In this work double edge naturally sampled modulation is selected. A total of $4\ N$ reference signals and $2\ N$ carriers signals are required for each FBMMC phase. Each SM is assigned with a specific reference signal and a triangular carrier [51]. The complementary modulation signals for the left leg (LL) and the right leg (RL) in upper/lower arm SMs are given by [85]:

$$
\begin{aligned}
M_{x,LL}^{up,k} &= \frac{1}{2} + \frac{\mathrm{M_{dc}}}{2} + \frac{M_{ac}}{2}\cos(\omega t + \theta_x + \pi) \\
M_{x,RL}^{up,k} &= \frac{1}{2} - \frac{\mathrm{M_{dc}}}{2} - \frac{M_{ac}}{2}\cos(\omega t + \theta_x + \pi) \\
M_{x,LL}^{low,k} &= \frac{1}{2} + \frac{\mathrm{M_{dc}}}{2} + \frac{M_{ac}}{2}\cos(\omega t + \theta_x) \\
M_{x,RL}^{low,k} &= \frac{1}{2} - \frac{\mathrm{M_{dc}}}{2} - \frac{M_{ac}}{2}\cos(\omega t + \theta_x)
\end{aligned}
\tag{3.26}
$$

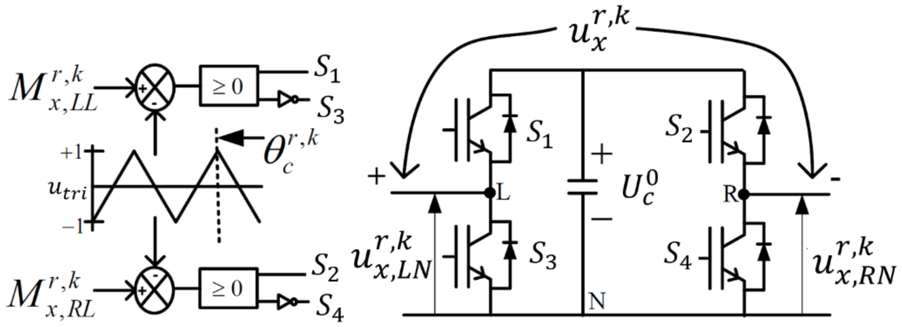


Figure 3-9 unipolar modulation structure for the SM of the FBMMC

Each carrier in the arm is shifted by π/N for best harmonic cancellation features and most effective arm switching frequency [51] [87]. The k^{th} SM carrier phase shift angle in the upper arm ($\theta_c^{up,k}$) and lower arm ($\theta_c^{low,k}$) can be presented as:

$$\theta_c^{low,k} = \frac{\pi}{N}\,(k-1) \tag{3.27}$$

$$\theta_c^{up,k} = \theta_d + \frac{\pi}{N}\,(k-1) \tag{3.28}$$

Where θ_d represents the carrier's displacement angle between the upper and lower arms. The displacement angle plays a crucial role on the high switching harmonic features of the FBMMC dc side and ac side [51].

Figure 3-10 and Figure 3-11 explain the PSC-PWM for buck mode and boost mode, respectively, for N = 4. As can be observed, the output voltage of the SMs in buck mode operation has only positive and zero levels. In boost mode operation, however, the SMs' output voltage has positive, negative, and zero levels.

The negative voltage level is generated to compensate the reduction in the dc-link voltage level. This means the ac side of the FBMMC can be kept fixed at an arbitrary dc-link voltage, which is a unique feature for applications such as WECS [28] [29].

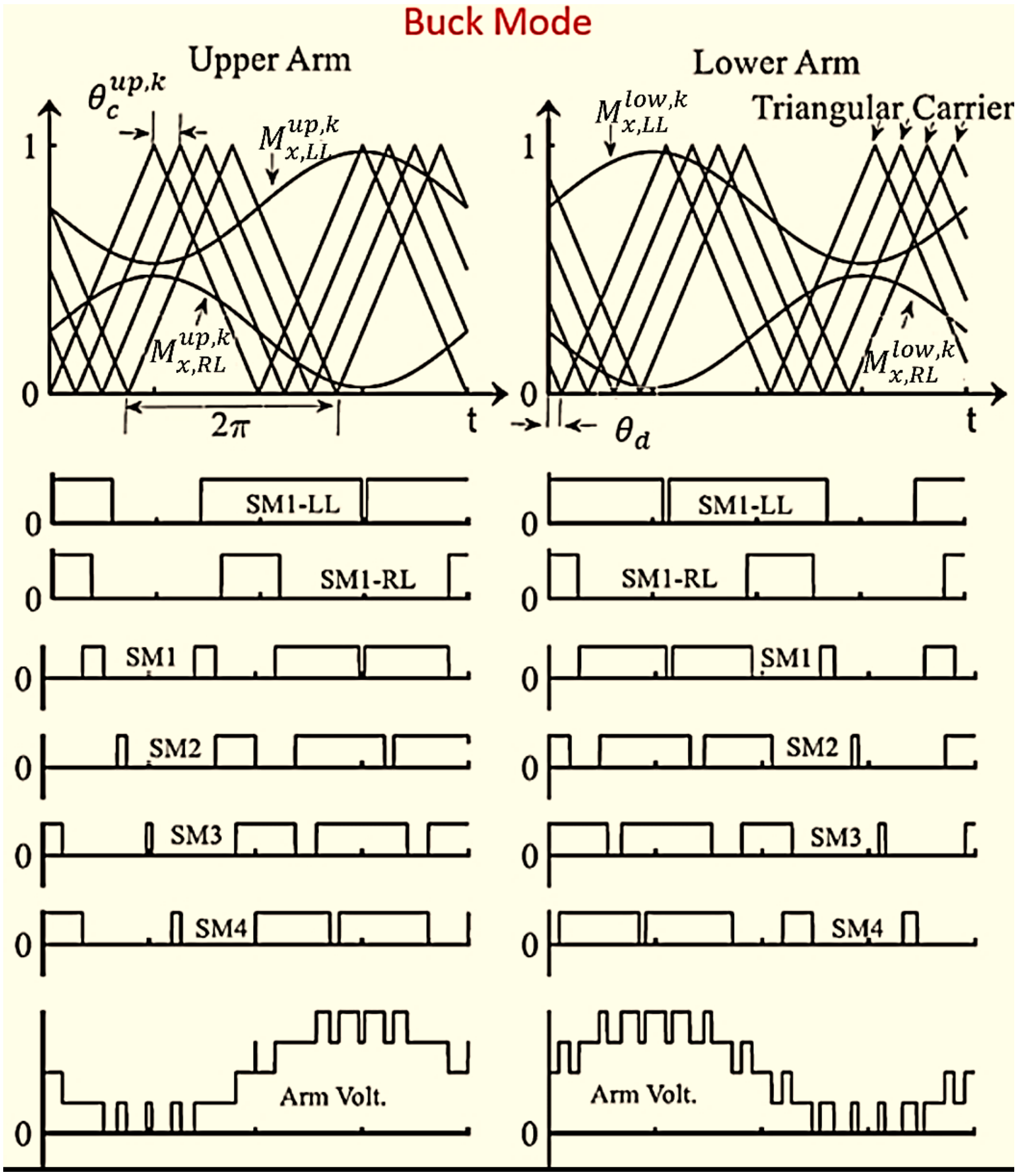


Figure 3-10 Buak mode PSC-PWM,N=4[88]

The negative voltage states affect the main electrical quantities of the system at low-frequency components and high-frequency components [84] [89]. This may need a redesign of the parameters of the system. The negative voltage states may also influence the ripple characteristic of the dc link of the FBMMC.

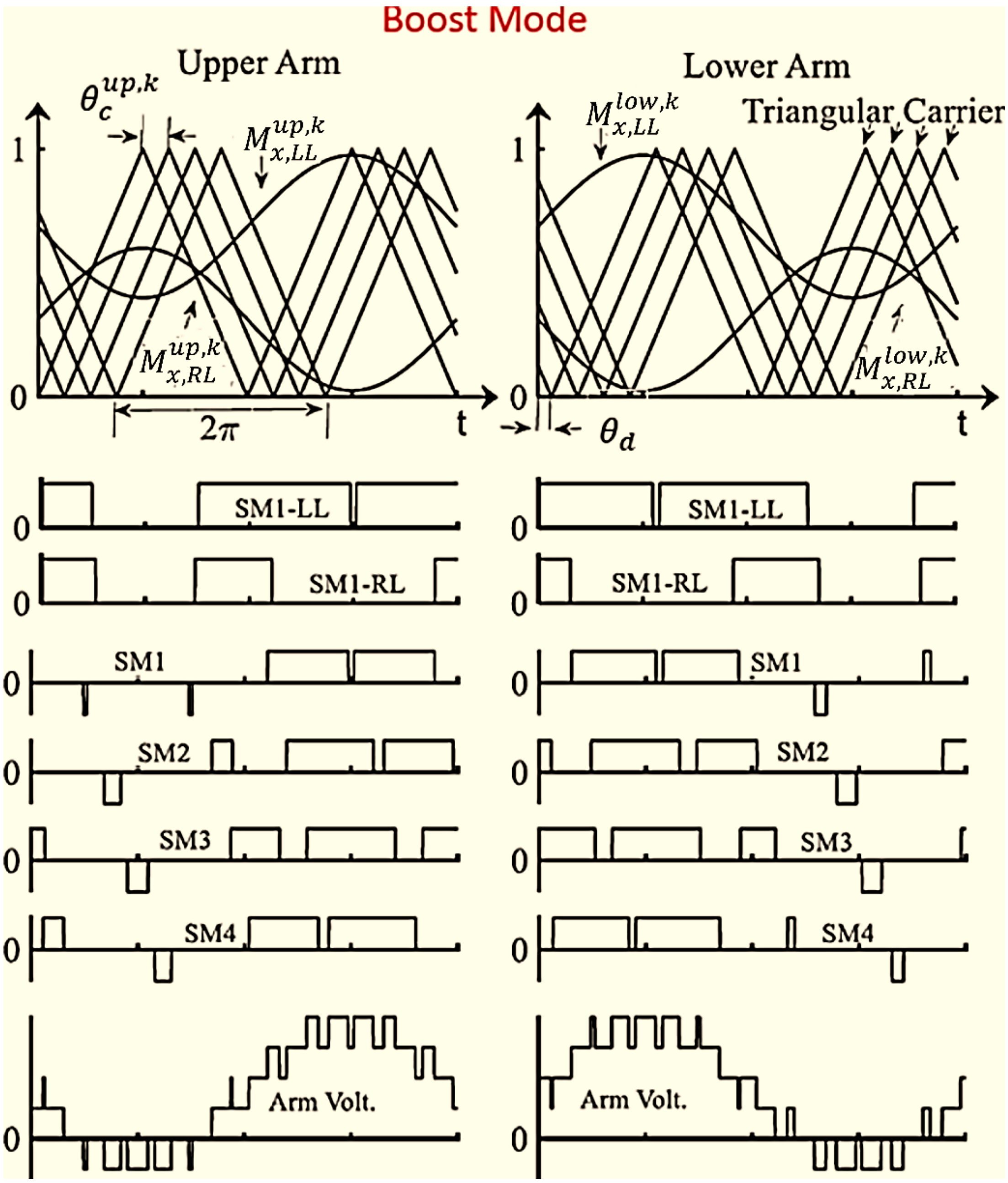


Figure 3-11 Boost mode PSC-PWM,N=4 [88]

3.5 Proposed system

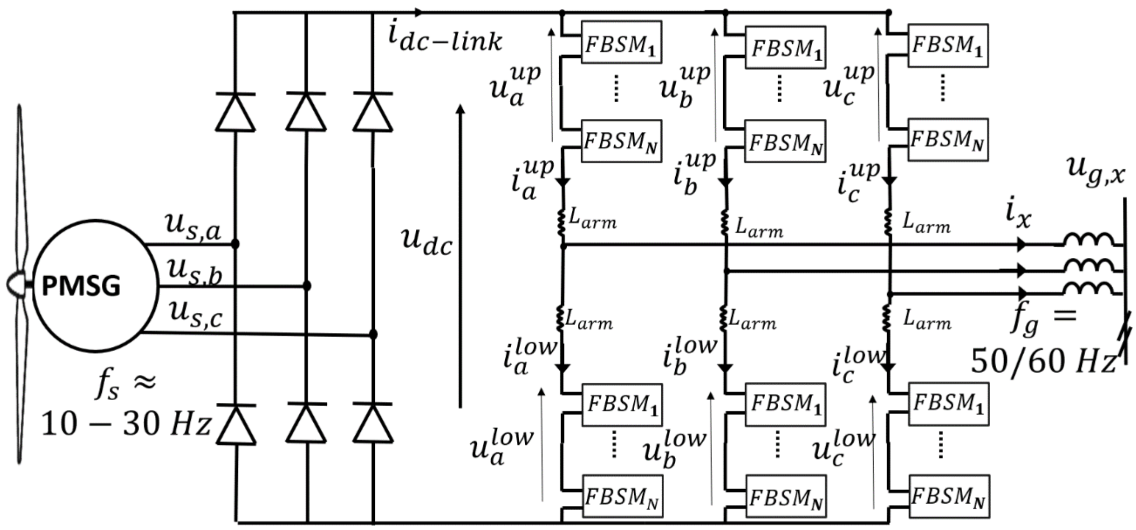


Figure 3-12 Detailed circuit of the proposed system

The WECS has a unidirectional power flow meaning that, they only supply power to the grid, not the other way around. Thus, the PGSC system (i.e., with 6 or 12-pulse diode-bridge rectifier) can be applied instead of BTBC system. The PGSC system offers extremely low cost, low failure rate and low power losses compared to BTBC system [3] [7] [28]. Figure *3-12* shows the PGSC system with FBMMC circuit configuration. The PGSC system connected to FBMMC does not require an extra boost converter as the FBMMC provides boost and buck functions, synchronizing the ac output voltage with the grid regardless of the dc link voltage [28] [35] [36]. A permanent magnet synchronous generator with a high number of poles is preferred as a generator since it eliminates the requirement for a gearbox, offering free maintenance, operation, and life expansion [3] [10] [65] [90]. Here the generator frequency (f_s) varies in agreement with time-varying wind energy, say 10 to 30Hz [10] [28]. This configuration allows to removing the large passive components in the dc link side, which has attracted research interest over long time [69] [70] [71]. However, removing the passive components from the dc-link side causes a high current ripple on the generator side, the dc-link side, and between the phases of the FBMMC. However, these problems can be overcome thanks to the circular interaction phenomenon feature of the FBMMC. The circular interaction phenomenon feature makes the MMC an open inverter since all its electrical quantities can be accessed [49] [83] [91] [92]. Therefore, once the dc-link current ripple enters the FBMMC phases and becomes part of the MMC arm current components, this current ripple can be accessed and minimized or eliminated. Smoothing out the current ripple circulating between the FBMMC phases will smooth out the dc-link current ripple as well as the generator side current ripple. This can be achieved through modifying the internal control of the FBMMC to include the external ripple caused by the rectifier. Through this the FBMMC works as an active filter for the dc-link allowing to remove the large LC passive filter.

3.5.1 Mathematical model of the proposed system

Figure 3-13 shows single-phase average model of the proposed system. For simplicity, the generator side and its inductances are ignored, and the system is assumed naturally well balanced. The rectifier is represented as dc-voltage source. The voltage across the SMs in the upper arm u_x^{up} and lower arm are u_x^{low} are represented as a single controllable voltage source. The losses in the converter arm is represented as R_{arm} and the resistance of ac side/ grid side is modeled as R_g [82].

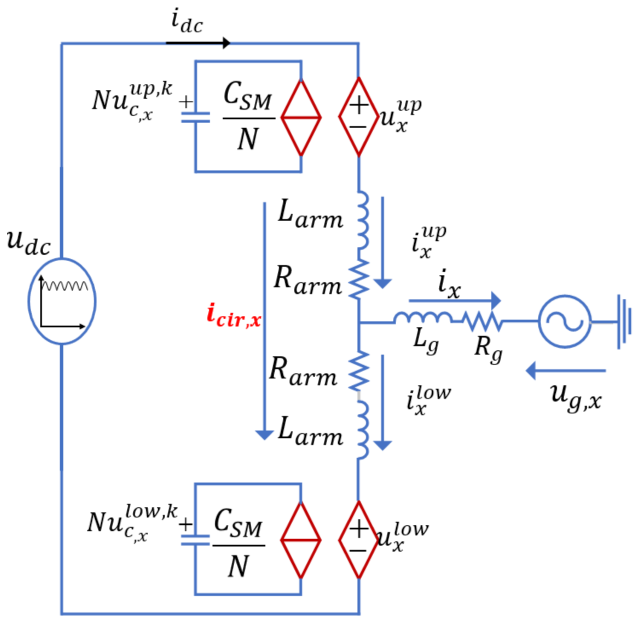


Figure 3-13 Single phase average model of the proposed system

The ac side voltage $u_{g,x}$ and current i_x are defined as:

$$u_{g,x} = \mathrm{U_g} \sin(\omega \mathrm{t} + \theta_\mathrm{x}) \tag{3.29}$$

$$i_x = \mathrm{I_m} \sin(\omega \mathrm{t} + \varphi) \tag{3.30}$$

Where U_g and θ_x are the amplitude and phase angle of the ac voltage. I_m and φ are the amplitude and phase angle of the ac current. θ_x is equal to 0, $-2\pi/3$ and $2\pi/3$ for phase a, b and c respectively. From Figure 3-13 and through using Kirchhoff's voltage-law, the following equations can be obtained:

$$\frac{u_{dc}}{2} - R_{arm} i_x^{up} - \frac{L_{arm} d i_x^{up}}{dt} = u_x^{up} + R_g i_x + \frac{L_g d i_x}{dt} + u_{g,x} \tag{3.31}$$

$$\frac{u_{dc}}{2} - R_{arm} i_x^{low} - \frac{L_{arm} d i_x^{low}}{dt} = u_x^{low} - R_g i_x - \frac{L_g d i_x}{dt} - u_{g,x} \quad (3.32)$$

Under steady state condition and well balance operation the ac side current i_x splits equally between the lower and the upper arms [49]:

$$i_x^{up} = i_{cir,x} + \frac{i_x}{2} \quad (3.33)$$

$$i_x^{low} = i_{cir,x} - \frac{i_x}{2} \quad (3.34)$$

Through equations (3.31) to (3.34) the arm voltages can be presented as:

$$u_x^{up} = \frac{u_{dc}}{2} - R_{arm} i_{cir,x} - \frac{L_{arm} d i_{cir,x}}{dt} - u_{m,x} \quad (3.35)$$

$$u_x^{low} = \frac{u_{dc}}{2} - R_{arm} i_{cir,x} - \frac{L_{arm} d i_{cir,x}}{dt} + u_{m,x} \quad (3.36)$$

Where $u_{m,x}$ is the FBMMC phase voltage and can be defined as:

$$u_{m,x} = U_m \cos(\omega t + \theta_x) \quad (3.37)$$

From Figure 3-13, using Kirchhoff's voltage-law, the $u_{m,x}$ can be obtained as:

$$u_{m,x} = \left(\mathrm{R_g} + \frac{R_{arm}}{2}\right) i_x + \frac{\left(L_g + \frac{L_{arm}}{2}\right) d i_x}{dt} + u_{g,x} \quad (3.38)$$

The terms of $\left(R_g + \frac{R_{arm}}{2}\right)$ and $\left(L_g + \frac{L_{arm}}{2}\right)$ are the equivalent impedance seen by the ac side R_{eq} and L_{eq}, respectively. Combining (3.35) and (3.36) the dynamics of the circulating current i_{cir} equivalent circuit can be obtained as:

$$R_{arm} i_{cir,x} + \frac{L_{arm} di_{cir,x}}{dt} = u_{cir,x} = \frac{u_{dc}}{2} - \frac{u_x^{up} + u_x^{low}}{2} \tag{3.39}$$

By subtracting equation (3.35) from equation (3.36) and substituting into equation (3.38) the dynamics of the ac side current equivalent circuit can be found as:

$$\frac{u_x^{up} - u_x^{low}}{2} = u_{m.x} = (R_{eq}) i_x + \frac{(L_{eq}) di_x}{dt} + u_{g,x} \tag{3.40}$$

Equations (3.39) and (3.40) the two equations define the internal and external dynamics of the FBMMC, respectively. They can be controlled individually. The external and internal dynamics circuits are presented in Figure 3-14.

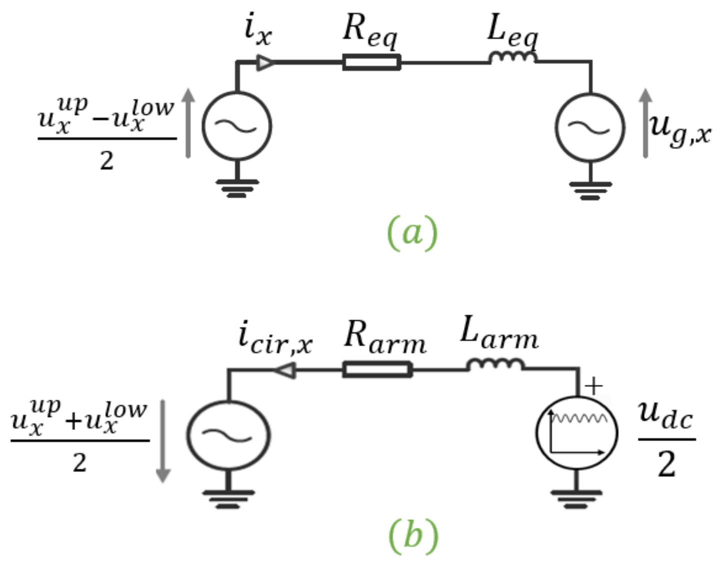


Figure 3-14 The dynamics circuit (a) external, and (b) internal

As seen from Figure 3-14(a), the ac side current is regulated by controlling the differential phase voltage in the converter arms $\frac{u_x^{up} - u_x^{low}}{2}$. The most common approach for the ac current is the vector control scheme [28].

As seen in Figure 3-14(b), the circulating current $i_{cir,x}$ can be controlled through the common mode arms voltage of the FBMMC $\frac{u_x^{up}+u_x^{low}}{2}$. By substituting equation (3.2) into equation (3.39), the internal dynamics equation can be given as:

$$u_{cir,x} = \left(\frac{U_{dc} + \sum_{i=1}^{\infty} u_{Pif_s}}{2}\right) - \left(\frac{u_x^{up} + u_x^{low}}{2}\right) \tag{3.41}$$

The circulating current is defined as the current that flows among the FBMMC legs. The second part from equation (3.41) (i.e., $\frac{u_x^{up}+u_x^{low}}{2}$) caused all circulating current ripple components related to the grid frequency [83] [93]. The existing literature has proven that the most dominant ripple in the circulating current is the second order harmonics related the grid frequency $i_{z,x,2}$ [28] [49] [83] [85]. The circulating current can be expressed as

$$i_{cir,x} \;\; = i_{dc} + i_{z.x,2} \tag{3.42}$$

Where i_{dc} is the current come from the dc side of the FBMMC and it is generated by the first part of equation (3.41) (i.e., $\frac{U_{dc}+\sum_{i=1}^{\infty} u_{Pif_s}}{2}$) and run through the FBMMC phases and can be expressed as :

$$i_{dc} = \frac{i_{dc-link}}{3} = I_{dc} + \sum_{i=1}^{\infty} i_{Pif_s} \tag{3.43}$$

Where I_{dc} is the dc component of the dc-link current in the FBMMC phase and i_{Pif_s} is the ripple component of the dc-link current in the FBMMC phase. By substituting equation (3.43) into equation (3.42), the circulating current component can be represented as:

$$i_{cir,x} = I_{dc} + \sum_{i=1}^{\infty} i_{Pif_s} + i_{z.x,2} \tag{3.44}$$

Equation (3.44) shows the circulating current includes extra ripple caused by the rectifier in addition to the initial second harmonic related to the grid frequency. The circulating current ripple components increase the device current stress, losses, and SM capacitor voltage ripple [94]. According to Equation (3.43), suppressing the ripple components caused by the rectifier i_{Pif_s} between the FBMMC phases would also smooth out the ripple in the dc-link current, and as a result, the ripple in the generator current will also be suppressed.

3.6 Proposed system control

The conventional two/three-level voltage source converters require only the ac current control loops. However, the control requirement of MMCs is different and more complicated as its arms are built with many SMs with floating capacitors. The MMCs require internal control to manage the stored energy and ensure proper stability between the converter arms [19] [28] [82].Moreover, the voltage difference between the arms generate the inherent low frequency in the arm current leading to the voltage ripple across the SMs capacitors. In addition, in the proposed system the dc-link ripple is injected directly to the FBMMC phases creating extra ripple components in the FBMMC arms. These low frequency ripple need to be suppressed to provide high efficiency [19] [95]. Thus, in this work the control is classified as:

- **External Control** (**EC**) to control the grid current and ensure proper power flow between the generator side and grid side.
- **Internal Control (IC)** to ensure proper balancing of SM capacitor voltages and efficient suppression of circulating current ripple components.

Note, the control structure of the FBMMC phases is identical and thus only one phase will be presented.

3.6.1 External Control

Similar to the conventional two/three-level voltage source converters the ac current side is control by popular vector control in dq synchronous frame [28] [82]. Equation (3.40) gives the ac current dynamic model. The dq transformation is given as [82]:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \underbrace{\begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix}}_{\alpha\beta \rightarrow dq} \underbrace{\begin{bmatrix} 2/3 & -1/3 & -1/3 \\ 0 & 1/\sqrt{3} & -1/\sqrt{3} \end{bmatrix}}_{abc \rightarrow \alpha\beta} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{3.45}$$

Through applying the dq transformation to equation (3.40), the dq reference frame equation representing the FBMMC ac current, and voltage is given as:

$$u_{md} = R_{eq} i_{gd} + L_{eq} \frac{di_{gd}}{dt} + \omega L_{eq} i_{gq} + u_{gd} \tag{3.46}$$

$$u_{mq} = R_{eq} i_{gq} + L_{eq} \frac{di_{gq}}{dt} + \omega L_{eq} i_{gd} + u_{gq} \tag{3.47}$$

In equations (3.46) and (3.47), i_{gd} and i_{gq} are the dq axes of the ac side current of the FBMMC i_x. u_{md} and u_{mq} are the dq axes of the FBMMC ac voltage. u_{gd} and u_{gq} are the dq axes of the grid voltage. The complete structure of the ac side current control is shown in Figure 3-15. The superscript '$*$' represents the reference values. Under the assumption of stiff grid side, d-axis aligned with phase a, the reference currents i_{gq}^* and i_{gd}^* are adjusted to track the instantaneous real power P_g, and reactive power Q_g, and can be obtained by the following equations [96]:

$$P_g = \frac{-3}{2}(U_g i_{gq}^*) \tag{3.48}$$

$$Q_g = \frac{-3}{2}(U_g i_{gd}^*) \tag{3.49}$$

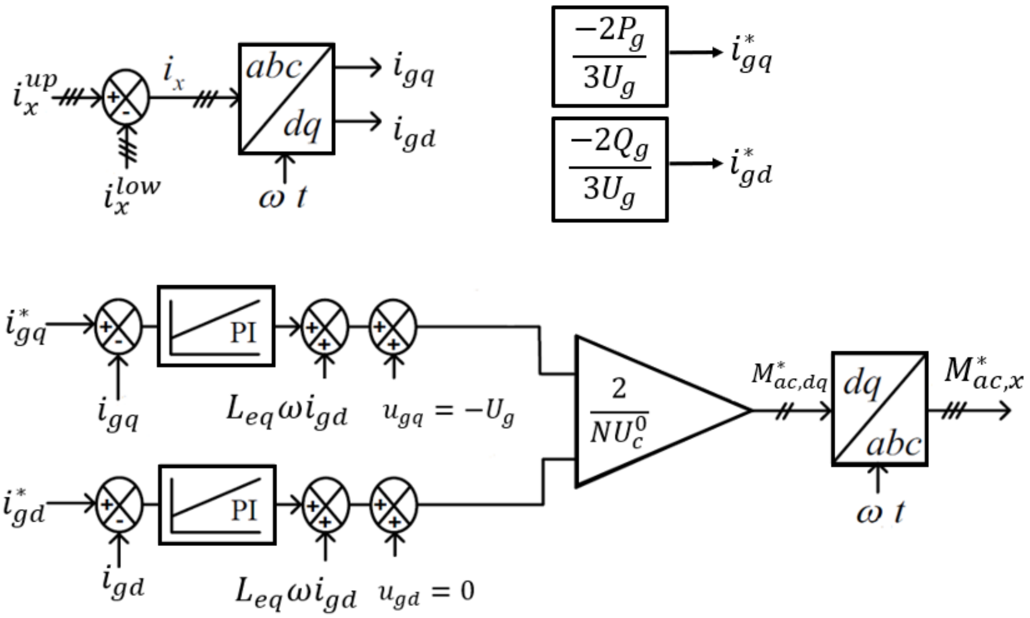


Figure 3-15 the block diagram of the external control[28]

3.6.2 Internal control

The main function of the internal control is to insure well voltage balancing across the SMs at the desired average voltage U_c^0, and minimize the internal current ripple for better efficiency and performance [96] [97]. Equation (3.39) explains the internal dynamics of the proposed system. There are two sources of the system internal low frequencies ripple components; the first one is the conventional second-order harmonics related to the grid frequency. The second one is due to the 6-pulse ripple caused by the rectifier and is related to the generator frequency. The foundations of the internal control can be found in [19] [28] [95]. However, in [19] [28] [95] the control is designed assuming pure dc-link voltage or in other words the ideal dc-link side. However, in the proposed system, the dc-link side has $P-pulse$ ripple, thus the original control needs to be modified to insure efficient suppressing for the proposed system ripple components. For simplicity the internal control is divided into:

- **Total Internal Control (TIC)** to set the desired voltage level $U_c^{0^*}$ for the capacitors of the SMs, prevent voltage deviation between the upper and lower SMs during charge and discharge processes, and efficiently suppress the circulating current ripple components.
- **Partial Internal Control (PIC)** to prevent the individual variation in the capacitor voltage of the SMs in the arm.

3.6.2.1 Total Internal Control

Equation (3.39) defines the internal electrical quantity performance of the FBMMC. Figure 3-16 shows the structure of the total internal control. It has three main parts. Part (a) is the average control; it forces the average voltage of all SMs capacitors in the FBMMC phase to follow the command $U_c^{0^*}$ and finds the dc-link current component command of the circulating current i_{dc}^* [19] [28] [95].

Part (b) is the arm balancing control, and it mitigates the moving average voltage difference between the upper arm and lower arm SMs capacitor voltages and finds the ripple component command related to the gride side of the circulating current $i_{z,x,2}^*$.Here the term $sin(\omega t + \theta_x)$ is synchronized to grid to ensure proper power transition between the upper and lower arm SMs [28] [95].

Part (c) is the circulating current suppression (CCS) control where a proportional gain K_P with three parallel resonant controllers are used. In the proposed system not only that the second order harmonics exist, but also the extra ripple components caused by the rectifier. Note, not all ripple components caused by the rectifier need a resonant controller as the amplitude of current harmonics decreases when the order of harmonics increases, as stated in equation (3.14). Thus, only the first two high harmonics are considered (i.e., i_{P1f_s} and i_{P2f_s}). The proportional resonant (PR) control is well established for the MMCs and will not impact the circulating current dc-component as long as the PR parameters are properly designed [56] [98].

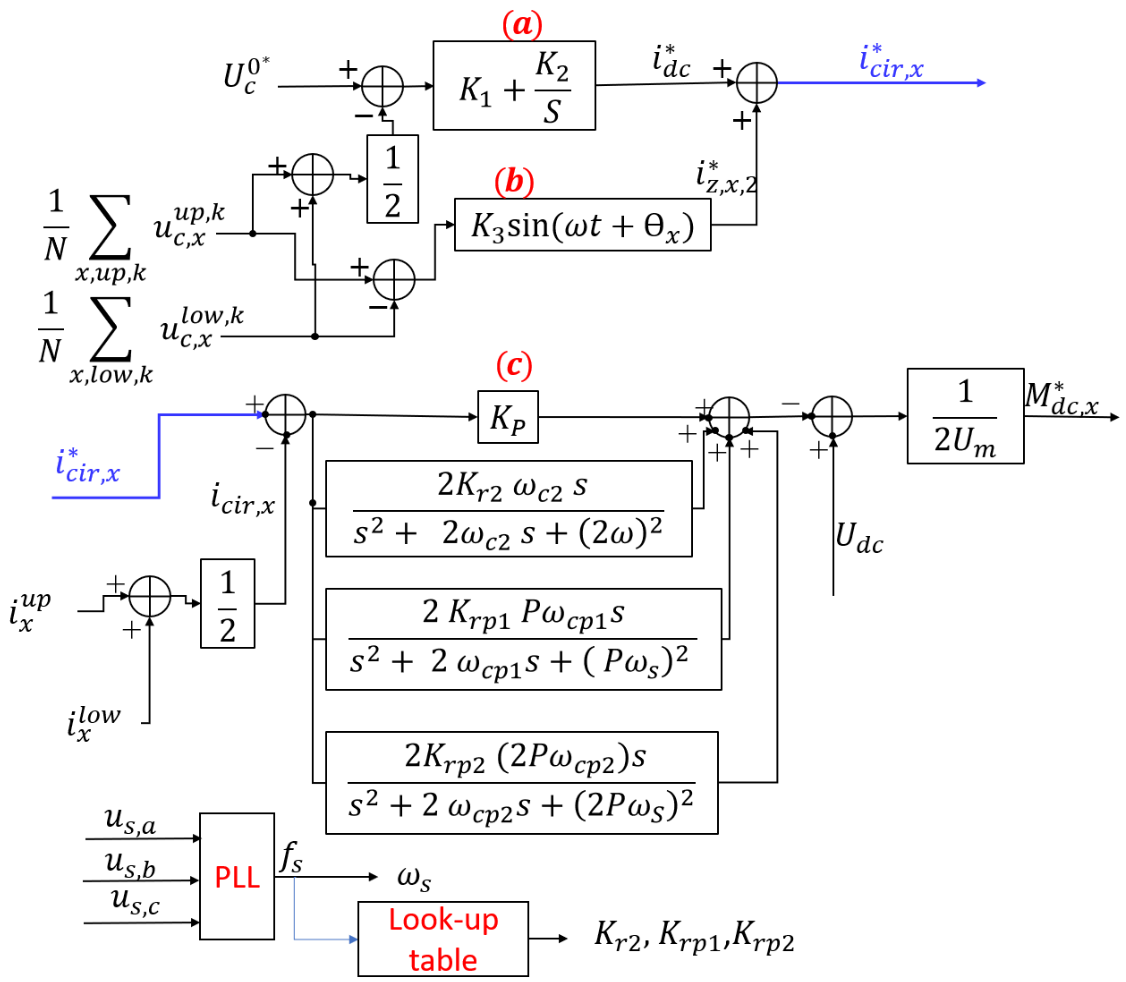


Figure 3-16 Block diagram of the total internal control

The general transfer function of the PR control is given by [56]:

$$PR = K_P + \frac{2K_r\omega_c s}{s^2 + 2\omega_c + \omega_f^2} \tag{3.50}$$

In equation (3.50), $K_r, \omega_c, and\ \omega_f$ are the resonant gain, cut-off frequency and resonant frequency. For $i_{z,x,2}, i_{P1f_s}$, and i_{P2f_s} the resonant frequencies are 2ω , $P\omega_S$, $and\ 2P\omega_S$ respectively. For $i_{z,x,2}, i_{P1f_s}, and\ i_{P2f_s}$ the resonant gains are $K_{r2}, K_{rp1}, and\ K_{rp2}$ respectively. Finally, the cut-off frequencies $\omega_{c2}, \omega_{cp1}, and \omega_{cp2}$ are related to $i_{z,x,2}, i_{P1f_s}$,and i_{P2f_s} respectively. The value of ω_c is selected to come to terms with the reduction of sensitivity and the error in tracking the reference signal [56]. The CCS control gains are tuned by a closed loop body plot method, and it has a bandwidth of 1580 red/sec, see Figure 3-17.

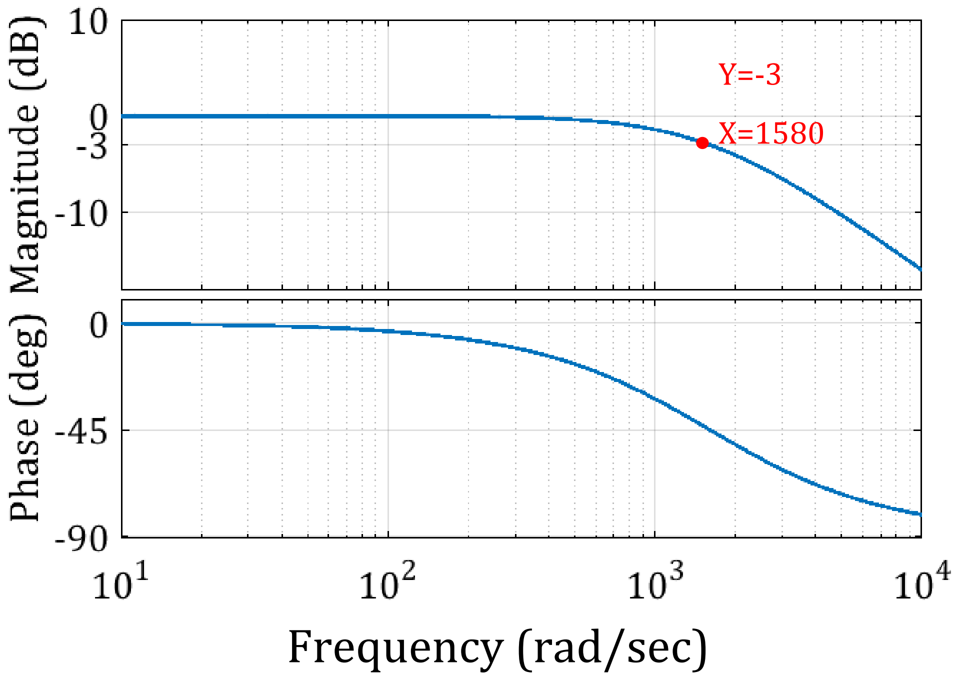


Figure 3-17 Bode diagram of CCS control

Because the values of the $i_{z,x,2}, i_{P1\omega_S}$ and $i_{P2\omega_S}$ are varying with variation of dc-link voltage, their related gains are selected under different condition and set in Look-up-Table. By using the well-established, Phase Looked Loop (PLL), the generator frequency tracked.

For instance, the response of the PR control under different generator frequency (i.e., $f_s = 10Hz\ and\ 30Hz$) are shown in Figure 3-18. As can be seen in Figure 3-18, the PR control track the generator frequency and work as a notch filter to eliminate the ripple in the system.

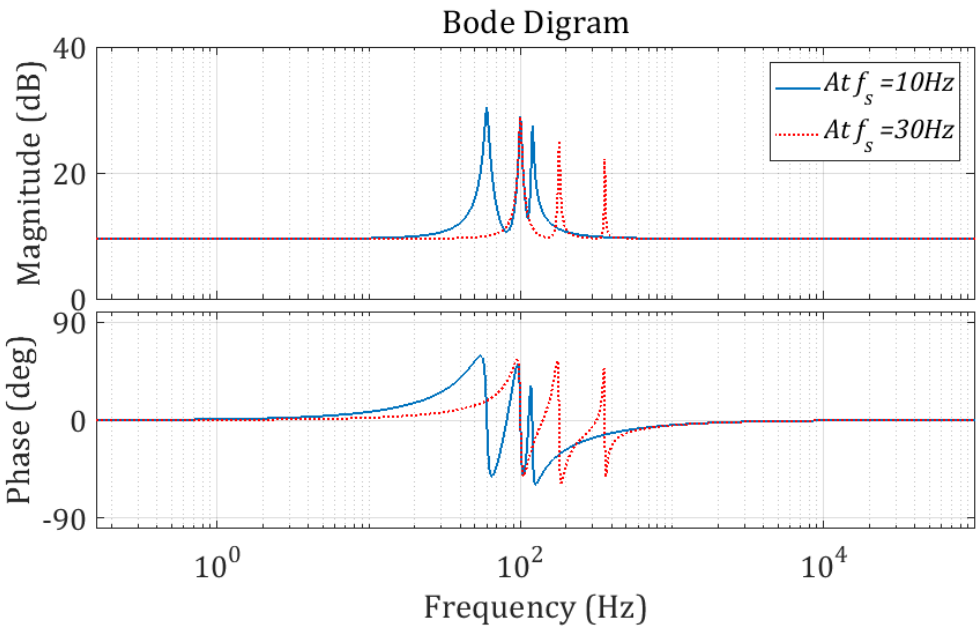


Figure 3-18 Bode plot loop diagram of the PR control

3.6.2.2 Partial Internal Control

As a result of an uneven power distribution caused by numerous factors, including discrete sampling, slight individual design variations, and so on, the voltage across the SMs' capacitor in the FBMMC tends to slightly diverge from the desired average value. Thus, PIC is adopted to avoid the average voltage variation across each SM capacitor.

The PIC block diagram is presented in Figure 3-19.

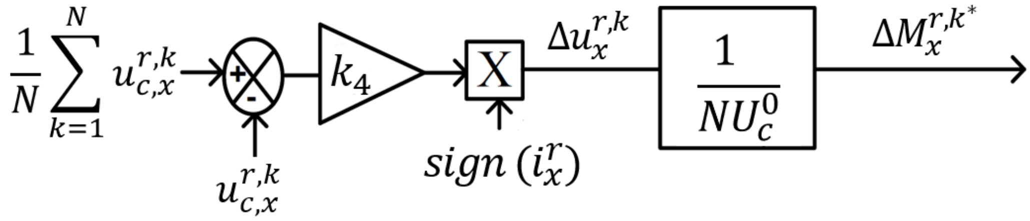


Figure 3-19 Partial internal control[95]

The PIC uses a proportional closed loop controller for each SM to charge or discharge the SM capacitor voltages by adding a small duty ratio $\Delta u_x^{r,k}$ based on the arm current's direction. The following is the dynamic equation that defines the voltage of the SM capacitor [19] [95]:

$$C_{SM} u_{c,x}^{r,k} \frac{du_{c,x}^{r,k}}{dt} = u_x^{r,k} . i_x^r \tag{3.51}$$

From equation (3.51) each individual SM capacitor voltage is controlled by changing the ac side voltage of the SM $u_x^{r,k}$, in relation to the direction of the arm current i_x^r. It must be noted that this control does not provide suppression of the circulating current ripple components.

3.6.3 Overall control

Figure 3-20 provides the structure of the overall proposed system control strategy. Here, the ac/grid current controller provides $M_{ac,x}^*$ and the total internal control provides $M_{dc,x}^*$ to the modulation signal reference for phase $x \in \{a, b, c\}$. The individual SM balancing reference $\Delta M_x^{r,k}$ is add to each SM modulation signal.

Then, the gate pulses are generated by comparing the total modulation signal and the carrier signal for each SM.

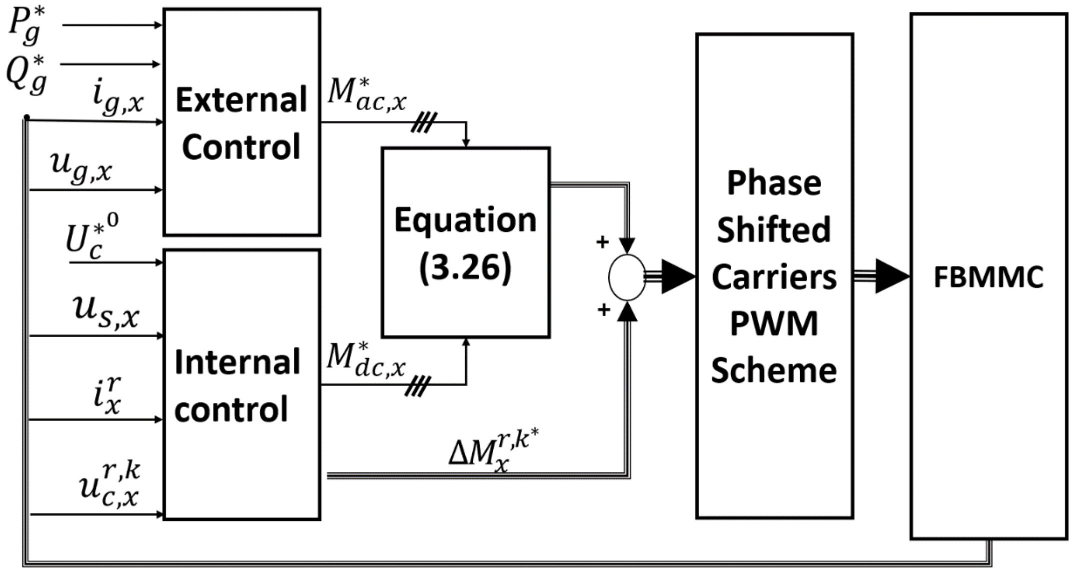


Figure 3-20 Overall control block diagram

For the effective operation of the cascaded closed control loops inside the MMC, it is necessary to design their bandwidths appropriately. Here the sampling frequency used for the control circuits is 16k Hz, which is equal to the effective switching frequency [81]. The effective switching frequency can be found as $2Nf_c$, where f_c is the switching frequency, and it is selected in this work as 2k Hz. As a general guideline, the control loop bandwidth should not exceed 10% of the sampling frequency, and the outer loop's control bandwidth should be one order of magnitude smaller than the inner loop's control bandwidth [81]. By following these rules, the designed bandwidth of the different control used in this project, in (Hz) are given in Table 3-II.

Table 3-II Summary of the control systems

Controller	Bandwidth
ac/grid current controller	350Hz
CCS control	250Hz
Average control	100Hz
Arm balancing contro	25Hz
Partial Internal Control	10Hz

3.7 MATALB Simulink verification

In this section, the results of MATLAB simulations are presented in order to illustrate the proposed system operating principles, the effects of dc-link ripple, the effectiveness of the control, and the key system variables. Therefore, a three-phase switching model of the proposed system connecting to a grid has been constructed in the MATLAB/Simulink environment. The simplified block diagram of the simulation module is shown in Figure 3-21.

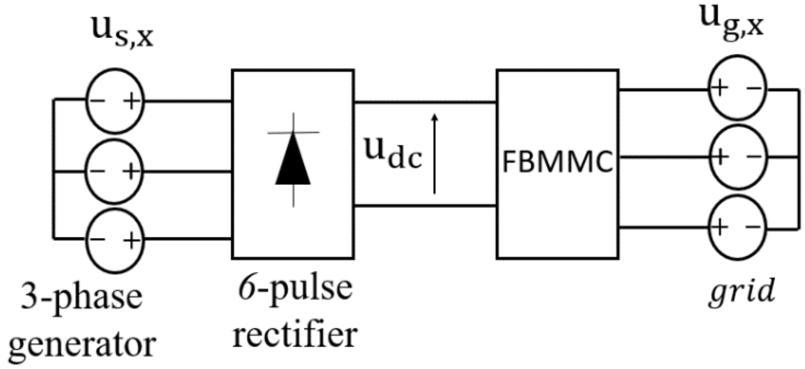


Figure 3-21 The simplified block diagram of the simulation module with 6-pulse rectifier

The main parameters of the switching model are presented in Table 3-III. The primary objective of this study is to demonstrate that the FBMMC can provide proper operation even when subjected to significant ripple components originating from the dc-link and can function as an active filter to compensate for the absence of a large LC filter in the dc-link.

As the proposed system has boost and back operation modes, as well as a generator frequency range of 10 to 30 Hz, three steady-state conditions under different dc-link voltage and generator frequency are presented on the following pages. The boost mode is achieved by reducing the dc-link voltage, whereas the ac side voltage is fixed. The dc-link voltage and generator frequency are reduced at the same time to emulate the wind speed behavior as closely as possible.

Table 3-III MATLAB simulation parameter design

Active power P_g	$4.7MW$
Nominal FBMMC phase voltage U_m	$3.3kV$
Grid frequency,f_g	$50Hz$
Nominal $dc - link$ voltage, U_{dc}	$6.6kV$
Number of SM per arm, N	4
Generator frequency, f_s	$10 - 30Hz$
Arm Inductor, L_{arm}	$7mH$
SMs' Capacitor, C_{SM}	$7mF$
Switching frequency, f_c	$2000Hz$

Figure 3-22 shows the system working in the buck mode condition with $U_{dc} = 6.6kV$, and $f_s = 30Hz$. Figure 3-23 illustrates the system operating in the boost mode condition with almost 30% reduction in the dc-link voltage from its nominal value, here the dc-link voltage is selected as $\mathrm{U_{dc}} = 4.7\mathrm{kV}$, and the generator frequency is selected as $\mathrm{f_s} = 25\mathrm{Hz}$. Finally, Figure 3-24 depicts the operation of the system in the boost mode condition with almost 56% reduction in the dc-link voltage from its nominal value, here $\mathrm{U_{dc}} = 2.9\mathrm{kV}, \text{and } \mathrm{f_s} = 10\mathrm{Hz}$.

Here in Figure 3-22(a)(d), Figure 3-23(a)(d), and Figure 3-24(a)(d), due to the boost features of the FBMMC, the synchronization with the grid voltage is achieved at varying dc-link voltage levels. In another word, the FBMMC can be kept fixed at any value of the DC-link voltage.

In Figure 3-22(b)(c)(e)(f), Figure 3-23(b)(c)(e)(f), and Figure 3-24 (b)(c)(e)(f), all system ripples resulting from the rectifier and grid sides are removed by the proposed controller. Thanks to the circular interaction phenomena of the FBMMC, the circular interaction feature gives access to the system's ripple components to be eliminated through the proposed controller. Furthermore, the rectangular generator current shape with THD = 30% is achieved without passive components in the dc-link.

These outcomes emphasise the FBMMC's ability to function as an active dc-link filter in addition to providing power transfer to the grid.

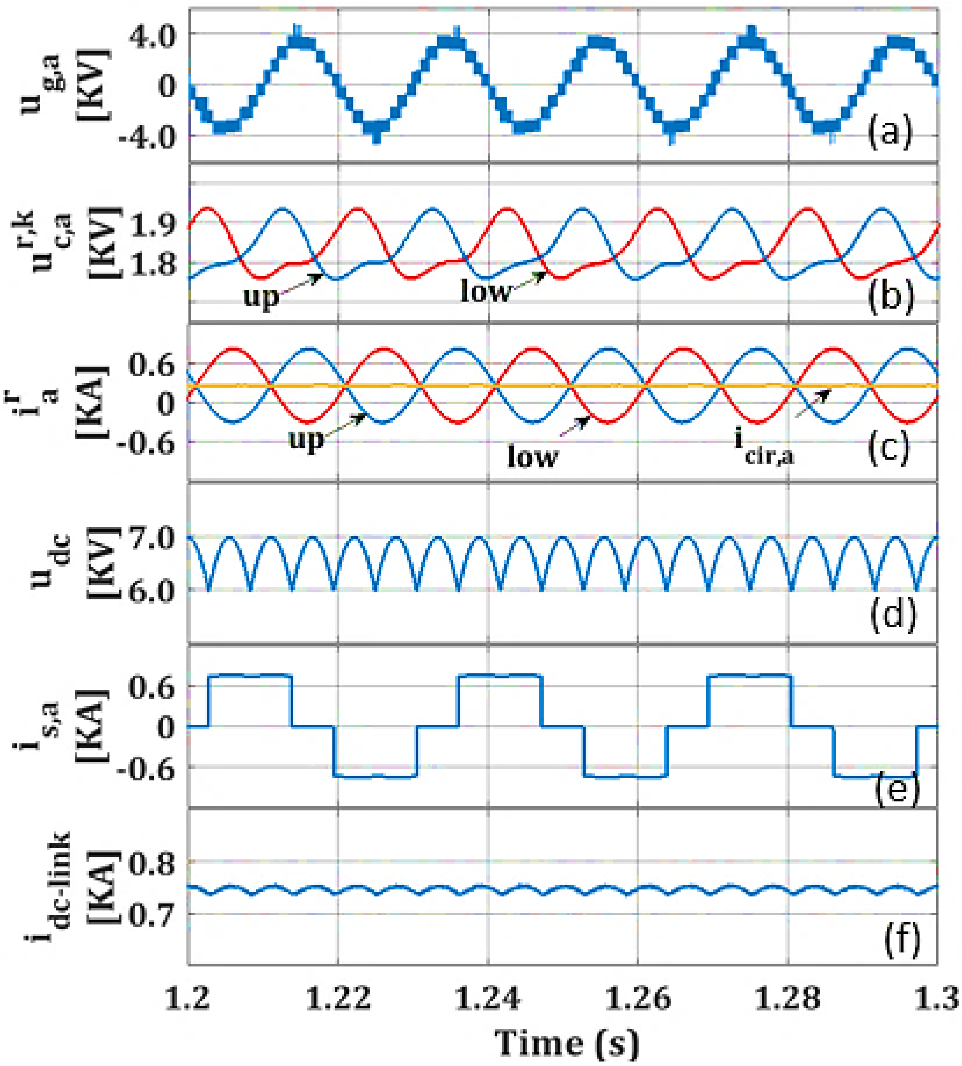


Figure 3-22 Buck mode operation, $U_{dc} = 6.6kV$, $f_s = 30Hz$, (a) FBMMC output voltage, (b) submodules capacitors voltages, (c) circulating current and arms currents, (d) dc-link voltage, (e) generator current, and (f) dc-link current

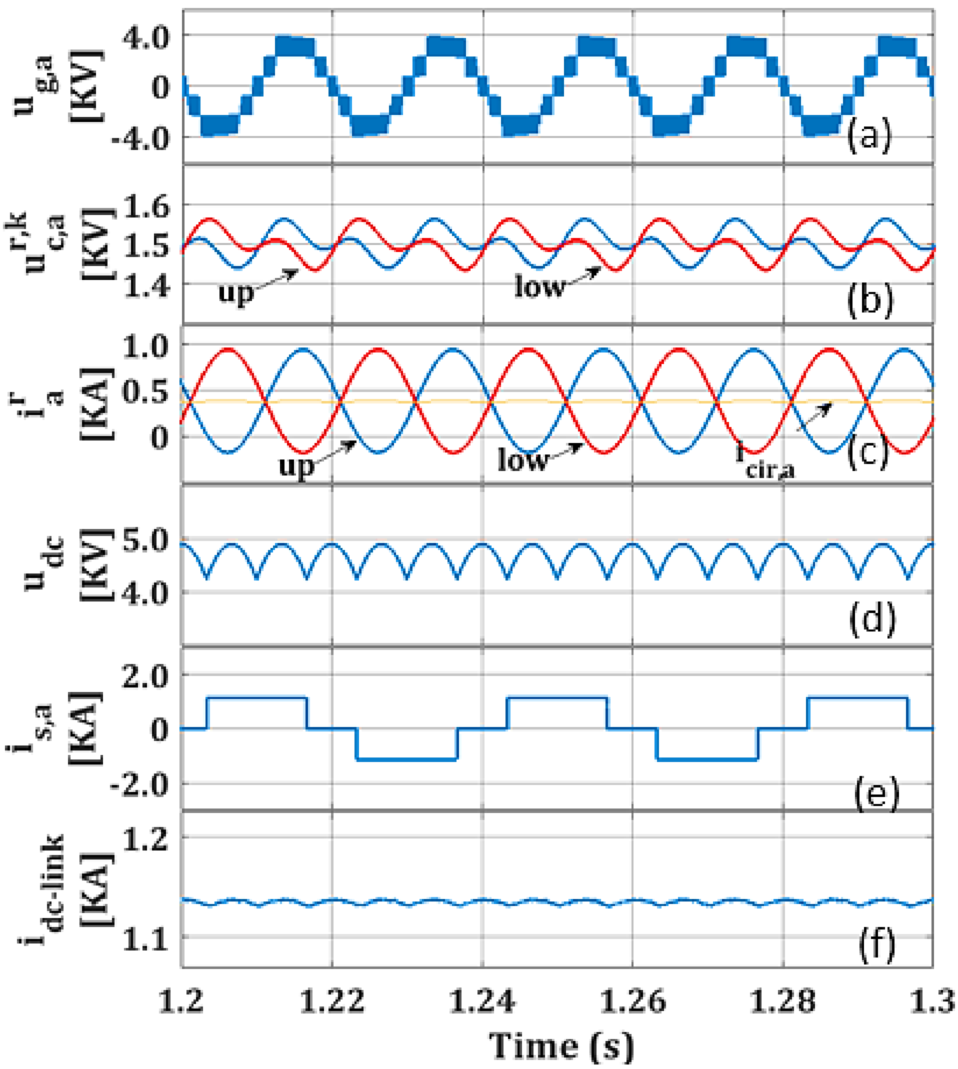


Figure 3-23 Boost mode operation, $U_{dc} = 4.7KV$, $f_s = 25Hz$, (a) FBMMC output voltage, (b) submodules capacitors voltages, (c) circulating current and arms currents, (d) dc-link voltage, (e) generator current, and (f) dc-link current

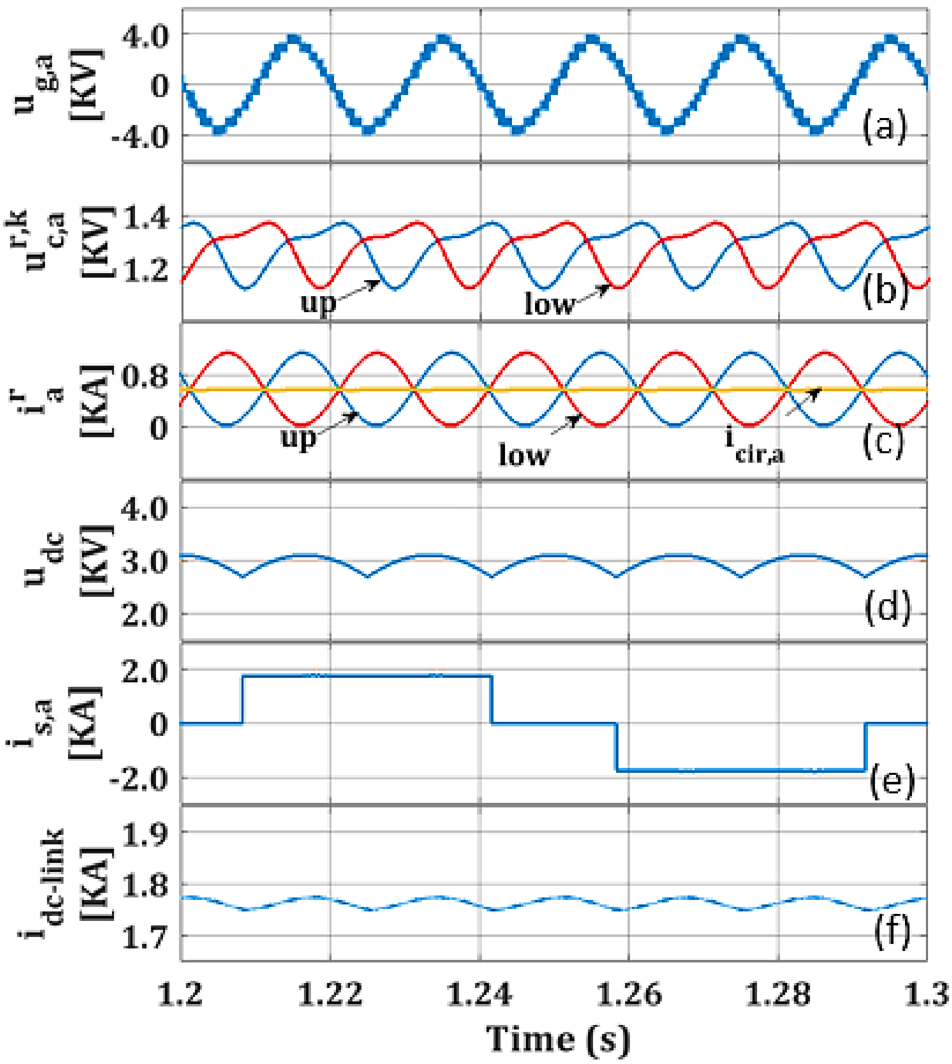


Figure 3-24 Boost mode operation, $U_{dc} = 2.9KV$, $f_s = 10Hz$, (a) FBMMC output voltage, (b) submodules capacitors voltages, (c) circulating current and arms currents, (d) dc-link voltage, (e) generator current, and (f) dc-link current

From Figure 3-13, and by ignoring the impedance caused by the C_{SM} and R_{arm}, for simplicity, the current ripple caused by the rectifier can be found as

$$i_{Pif_s} = \frac{u_{Pif_s}}{2\omega_s PiL_{arm}} \tag{3.52}$$

According to equations (3.14) and (3.52), where the FBMMC runs in buck mode and the generator frequency is at its lowest, the ripple in the dc-link current is at its greatest. Figure 3-25 depicts the proposed system in the transient state at the operating point where the dc-link current ripple is at its maximum (which presents extreme ripple conditions, albeit not realistic for WECS it demonstrates the control effectiveness).

In Figure 3-25 shows the system starting only with the external control (Figure 3-15), and individual balancing control of SMs (Figure 3-19). These controllers are necessary for the MMC to operate in an appropriate manner. The internal control (shown in Figure 3-16) is activated at the time t =1s.

The ripple in the circulating current and the dc-link current has been eliminated, and the capacitor voltages of the SMs are well balanced.

Furthermore, by extending the circulating current control, not only the current ripple circulating between the FBMMC phases, but also the dc-link current ripple and the generator side current ripple are removed. The generator current waveforms with THD = 30% are achieved.

In conclusion, the FBMMC proposed control not only smooth out the ripple between the FBMMC phases but also the ripple in the dc-link as well as the ripple in the generator current. This characteristic enables the proposed system to efficiently operate without passive components in the dc-link, this is offer low cost, wight and size.

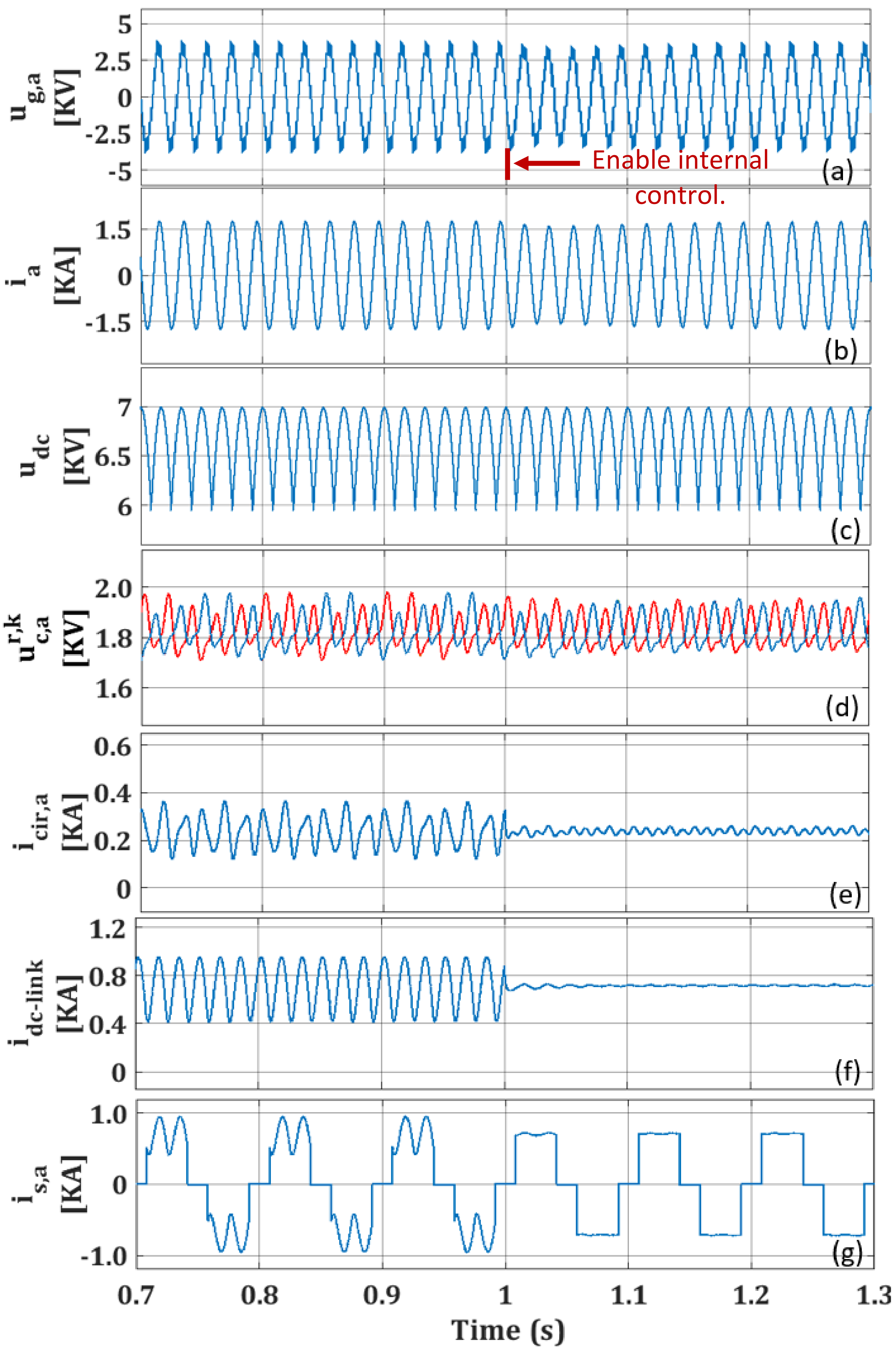


Figure 3-25 System with proposed internal control - off and on mode, (a) FBMMC output voltage, (b) FBMMC output current,(c) dc-link voltage, (d) submodules capacitors voltages,(e) circulating current,(f) dc-link current, and (g) generator current

In order to verify the accuracy of equations (3.13), and (3.14), they are evaluated against the simulation results by applying the FFT function analysis on the output voltage of the rectifier as shown in Table 3-IV. From equation (3.13), and (3.14), the value of the output voltage ripple of the rectifier is only dependent on the amplitude of the generator phase voltage. Two operating conditions are simulated and compared. The first operation condition; the buck mode when the dc-link voltage is at its nominal value $U_{dc} = 6.6KV\ and\ f_s = 30Hz$. The second operation condition; the boost mode when the dc-link voltage is at its nominal value $U_{dc} = 2.9KV\ and\ f_s = 10Hz$.

Table 3-IV Simulation and analytical comparison

Condition	Electrical quantities	Simulation	Analytical	Error%
(1)	u_{Pf_s}	377.12 V	377.125 V	0%
	u_{P2f_s}	92.31 V	92.296 V	0.02%
	u_{P3f_s}	40.87 V	40.861 V	0.02%
(2)	u_{Pf_s}	165.7 V	165.707 V	0%
	u_{P2f_s}	40.56 V	40.554 V	0.02%
	u_{P3f_s}	17.95 V	17.954 V	0.011%

Table 3-IV show a perfect match between the Simulation and the analytical model in (3.13) and (3.14). The generator phase voltage defines the dc-link voltage ripple. This means a higher generator side phase voltage leads to higher dc-link current ripple.

3.8 Experimental Validation

In order to verify the capabilities of the proposed system, experiments are carried out on a prototype developed in the laboratory. The experimental setup is described in detail in Chapter 2. A three phase FBMMC with front end 6-pulse rectifier is bulti with two SMs per arm. The IKCM20L60GDXKMA1 from INFINEON intelligent power module is used to design each SM and OPAL-RT 5607 is the control platform. An ac power source (Chroma 61703) is used as a generator with frequency range 15-1200Hz. The FBMMC ac side is connected to passive load of 10Ω.

The experimental setup parameters are given in Table 3-V. The experiment is performed for three different steady-state cases and one transient case. Figure 3-26 shows main waveforms of the system working in buck mode with nominal dc-link voltage $U_{dc} = 140, and\ f_s = 30\ Hz$. Figure 3-27 presents the system working in boost mode with $U_{dc} = (140 \times 0.8) = 112V, and\ f_s = 25Hz$. Figure 3-28 presents the system working in boost mode with $U_{dc} = (140 \times 0.6) = 86V, and\ f_s = 15Hz$.

Unlike other converters, the MMC has a circular interaction phenomenon. The circular interaction of the FBMMC allows the dc-link ripple current to be part of the FBMMC electrical quantities. This gives easy access to the dc-link ripple current to be controlled and minimized. Here, the FBMMC not only minimizes the undesired ripple current between its phases, but also minimizes the dc-link and the generator side undesired current ripple.

Finally, Figure 3-29 show the proposed system in the transient state at the operating point where the dc-link current ripple is at its maximum. In Figure 3-29, the system starting only with individual balancing control of SMs (Figure 3-19). This controller is necessary for the MMC to operate in an appropriate manner. Here, the modulation signal parameters M_{dc} and M_{ac} are inserted directly to the control. At the beginning of the operation, the internal control (shown in Figure 3-16) is of and then it is activated after.

Figure 3-29 verifies the controller robustness under the worst-case condition related to the experiment parameters (i.e., the maximum dc-link ripple current. This condition is found when the FBMMC works in buck mode with the lowest generator frequency ($U_{dc} = 140V, f_s = 15Hz$).

Table 3-V Parameters of the proposed system experimental prototype

$\mathrm{dc-link\ voltage\ (U_{dc})}$	$\mathrm{140\ V(nominal), 112V, 86V}$
Ac side voltage	70V
Ac power	600W
Ac side frequency	50Hz
Switching frequency	2500Hz
Load resistance	10Ω
Submodules Number of each arm (N)	2
Arm impedance ($\mathrm{R\_arm, L_{arm}}$)	0.64Ω, 1.85mH
Module capacitance ($\mathrm{C_{SM}}$)	0.66mF
Load peak current	7A

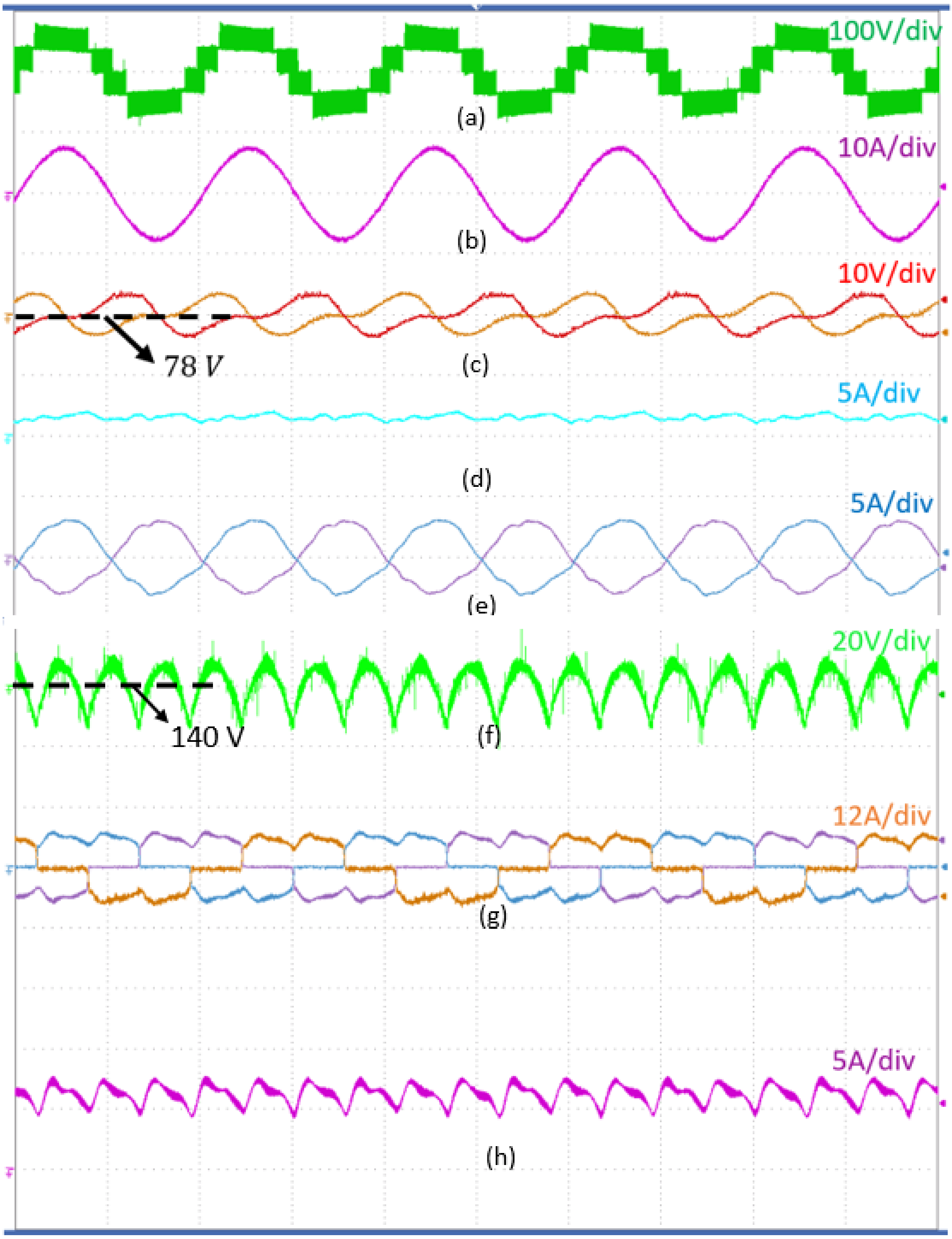


Figure 3-26 Buck mode operation condition (a) MMC output voltage, (b) MMC output current (c) submodules capacitors voltages, (d) circulating current, (e) arms currents, (f) dc-link voltage, (g) generator currents, (h) dc-link current
{timescale 10ms/div, f_s=30Hz and U_{dc}=140V}

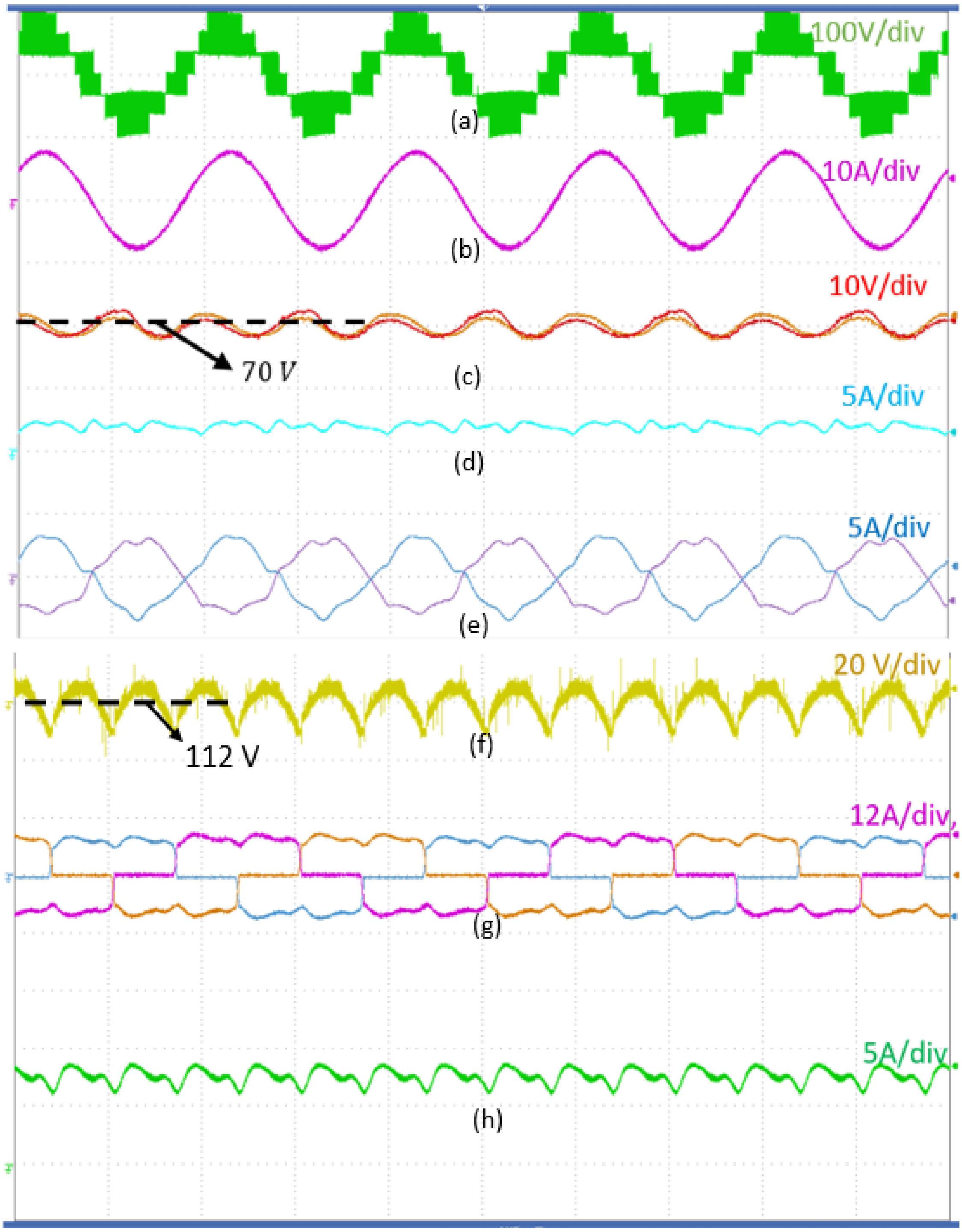


*Figure 3-27 Boost mode operation condition (a) MMC output voltage, (b) MMC output current (c) submodules capacitors voltages, (d) circulating current, (e) arms currents, (f) dc-link voltage, (g) generator currents, (h) dc-link current {*timescale 10ms/div, fs=25Hz and U_{dc}=112V*}*

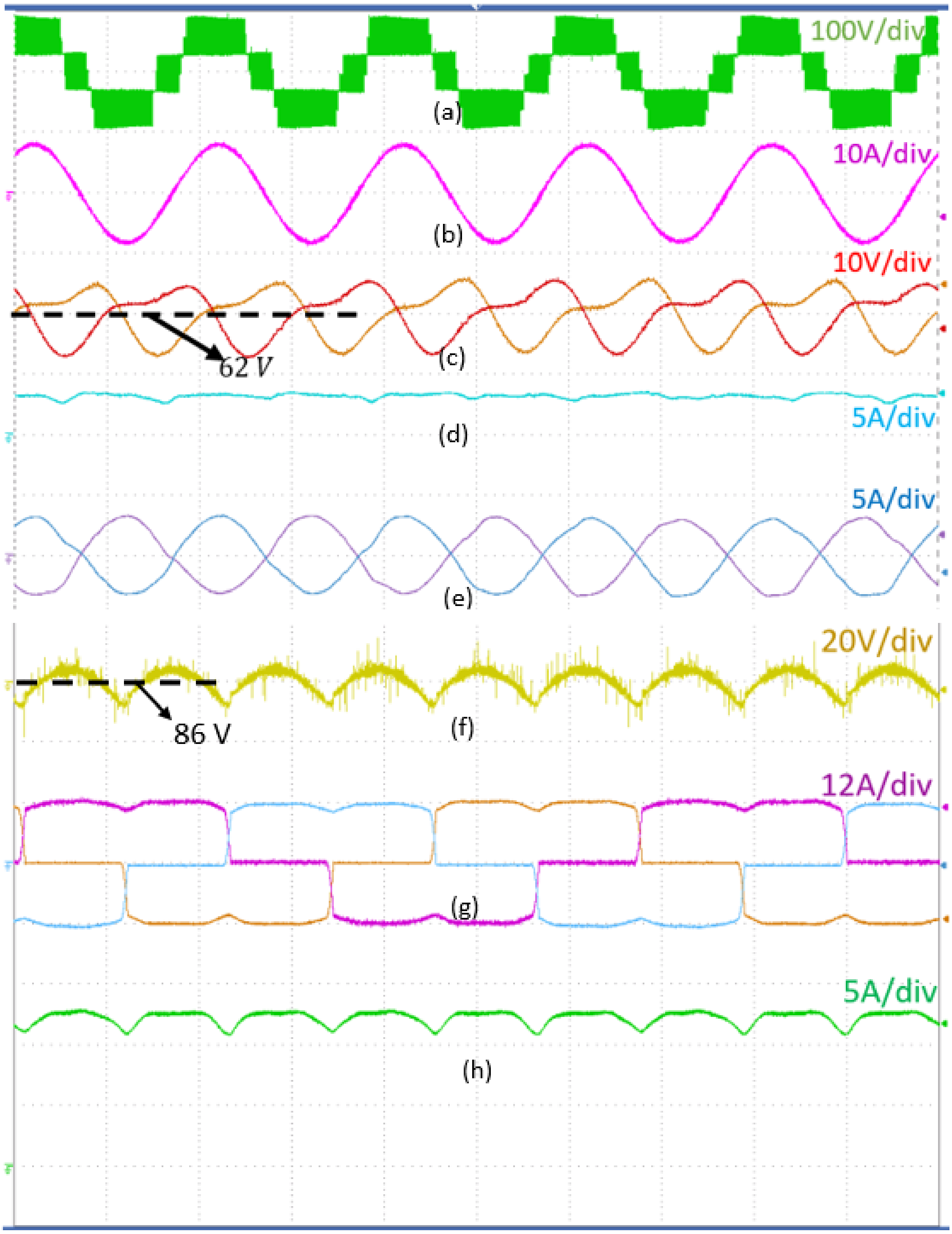


Figure 3-28 Boost mode operation condition (a) MMC output voltage, (b) MMC output current (c) submodules capacitors voltages, (d) circulating current, (e) arms currents, (f) dc-link voltage, (g) generator currents, (h) dc-link current {timescale 10ms/div, fs=10Hz and U_{dc}=86V}

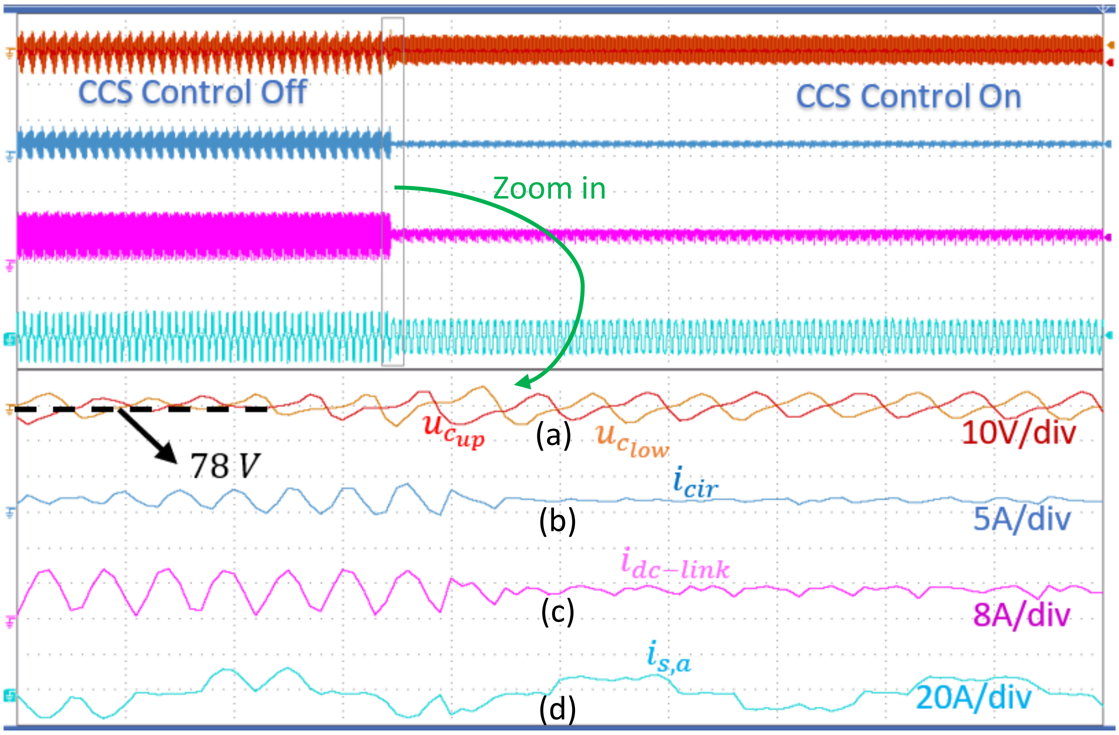


Figure 3-29 Buck mode operation condition with and without CCS control, (a)submodules capacitors voltages, (b) circulating current, (c) dc-link current, and (d) generator currents. $\{timescale\ 10ms/div, f_s = 15Hz\ and\ U_{dc} = 140V\}$

3.9 The 6-pulse versus the 12-pulse diode bridge rectifiers

Although the six-pulse diode rectifier is characterized by the robustness and simplicity, it is associated with some drawbacks. In the generator side, the phase currents include 5th and 7th harmonics of 14% and 7%, respectively, leading to a 6th harmonic distortion of 10% in torque. Even though these generator current harmonics and the torque ripple do not affect the grid due to the decoupling provided by the FBMMC, they limit the power delivery because of the high losses caused by the harmonic distortion in the generator side. Therefore, the six-pulse diode rectifier is a better choice for the power range below 5MW [3] [65].

With the demand for wind energy conversion systems on the rise, the size and power of turbines have increased dramatically, with 10-14MW wind turbines already available [3]. The multi-pulse rectifier stands to overcome the above mentioned drawbacks of the six-pulse diode rectifier. Using 12-pulse rectifier eliminates the 5th and 7th harmonics in the generator phase currents and mitigates the electromagnetic torque ripples and even reduces the voltage/current ripple on the dc side of the converter. The 12-pulse rectifier is robust and widely adopted in many applications [3] [7] [65] .

However, the 12-pulse rectifier requires a 30-degree phase shift between its phases. This could be achieved either through a phase-shifting transformer or a multiphase generator (i.e., 6-phase PMSG). Although the phase-shifting transformer provides a galvanic isolation between the rectifier input and the generator, it is associated with large size and wight [3] [7] [65] [90]. The 6-phase PMSG is associated with relatively high cost, however it is preferable here, as it has many advantages which include: lower generator phase currents, fault-tolerant operation under power switch or phase winding open-circuit faults, lower MMF harmonics because of the cancelation of harmonics in the air-gap, enhanced efficiency, and power density [99] [100] [101].

3.10 The 12-pulse diode bridge rectifier output voltage analysis

The structure of the 12-pulse diode bridge rectifier is shown in Figure 3-30. Simply, it consists of two 6-pluse rectifiers connected in series with a 30-degree phase shift between their input voltages.

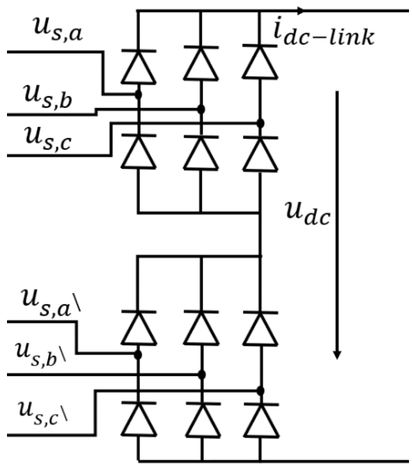


Figure 3-30 Structure of the 12 -pulse rectifier

Similarly to the 6-pulse rectifier, by ignoring the voltage drop across the diodes, the output voltage of the 12-pulse rectifier is a result of a two sets of input line to line voltages, as seen in Figure 3-31. From equation (3.9) and because the 12-pulse rectifier is simply a series connection of two 6-pulse rectifiers, the output voltage dc component U_{dc} of the 12-pulse rectifier can be found as:

$$U_{dc} = 2 \times 1.654\mathrm{U}_s \tag{3.53}$$

Similarly to the 6-pulse rectifier, from Figure 3-31 and by using Fourier series synthesis, the ripple components in the output of the 12-pulse rectifier can be found as:

$$U_{Pif_s} = \frac{8}{T}\int_0^{\frac{T}{2}} \left(\sqrt{3}U_s \cos\left(\frac{2\pi t}{12T}\right) \times \cos\left(\frac{2\pi it}{T}\right)\right) dt \tag{3.54}$$

By solving equation (3.54), the general formula that represents any ripple component in the output of 12- pulse rectifier can be found as:

$$U_{Pif_s} = \frac{24\sqrt{3}U_s}{\pi} \times \left(\left(\frac{\sin\left(\frac{\pi + 12i\pi}{12}\right)}{1 + 12i}\right) + \left(\frac{\sin\left(\frac{\pi - 12i\pi}{12}\right)}{1 - 12i}\right)\right) \tag{3.55}$$

Therefore, from equation (3.55), U_{P1f_s}, U_{P2f_s} , and U_{P3f_s} for 12-pulse rectifier can be found as:

$$\begin{aligned} U_{Pf_s} &= 0.04789U_s \\ U_{P2f_s} &= -0.01191U_s \\ U_{P3f_s} &= 0.00528U_s \end{aligned} \tag{3.56}$$

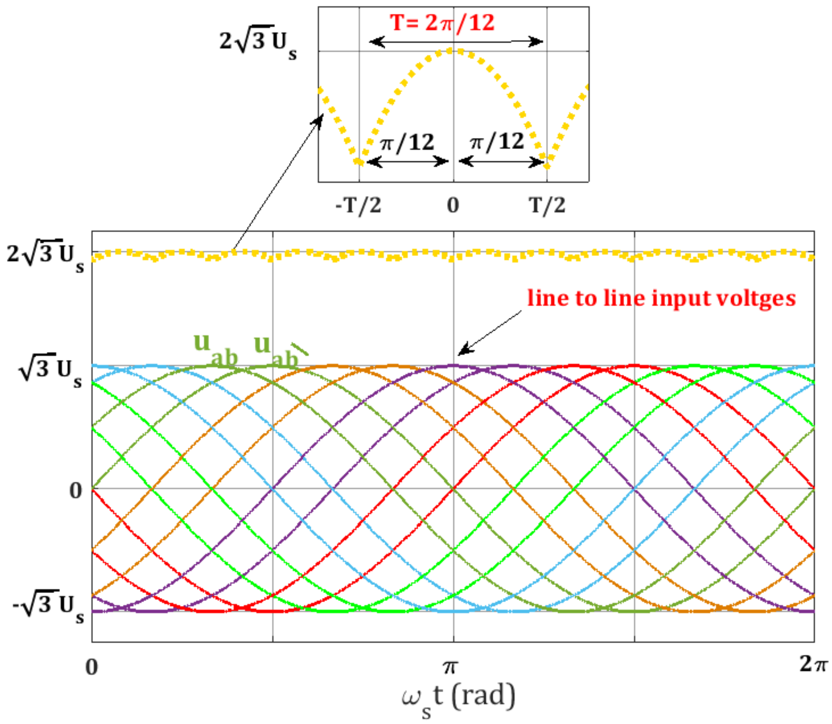


Figure 3-31 12-pulse rectifer input and output voltages

3.11 The proposed system with 12-pulse rectifier

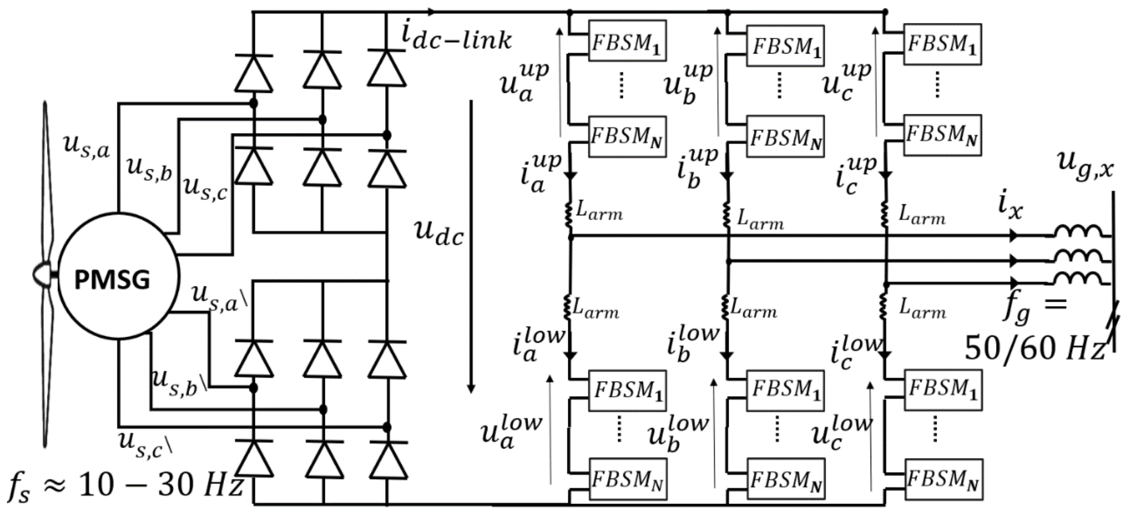


Figure 3-32 The proposed system with 12-pulse rectifier

Figure 3-32 depicts the proposed system with a 12-pulse rectifier. Compared to the 6-pulse rectifier in equation (3.14), the 12-pulse rectifier significantly reduces the output voltage ripple of the rectifier by almost 50%, see equation (3.56). In addition, the 12-pulse rectifier shifts the most dominant ripple component of the dc link side voltage and current from six times the generator frequency to twelve times the generator frequency. In addition, the generator phase currents are close to sinusoidal. These additional features make the proposed system more suitable for higher power wind power applications.

The proposed system with the 12-pulse rectifier is built in MATALB simulation environment, the simplified block diagram of the simulation module is shown in, and the steady-state results are presented in Figure 4-31 and Figure 4-32 for two different operation modes of the FBMMC.

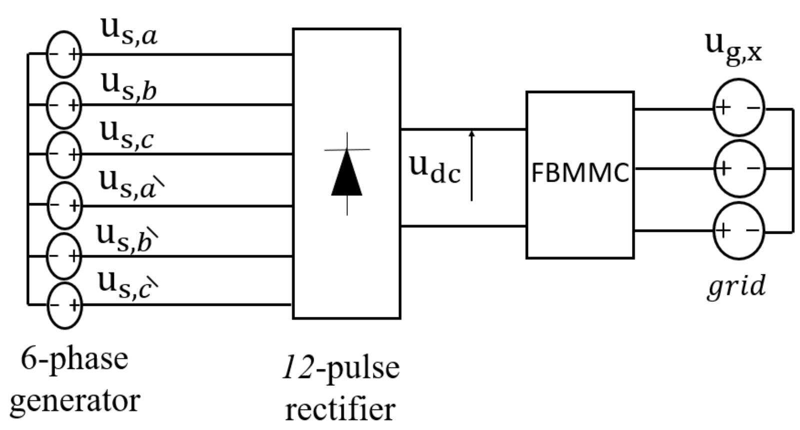


Figure 3-33 The simplified block diagram of the simulation module with 12-pulse rectifier

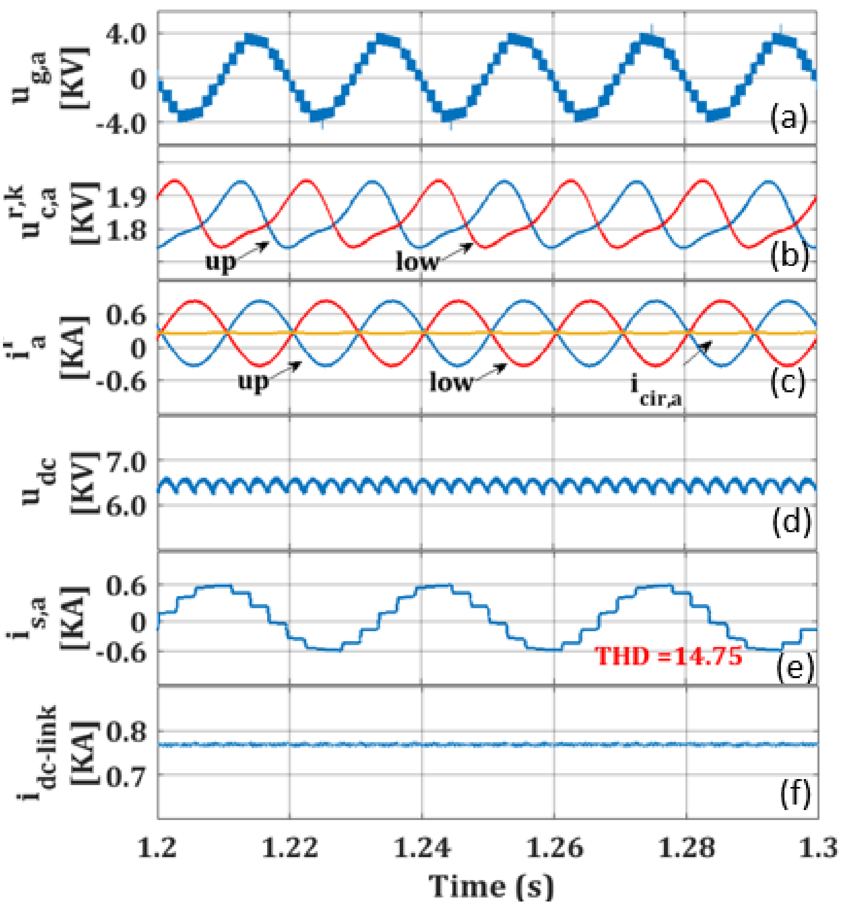


Figure 3-34 Buck mode operation, $U_{dc} = 6.6KV$, $f_s = 30Hz$, (a) FBMMC output voltage, (b) submodules capacitors voltages, (c) circulating current and arms currents, (d) dc-link voltage, (e) generator current, and (f) dc-link current

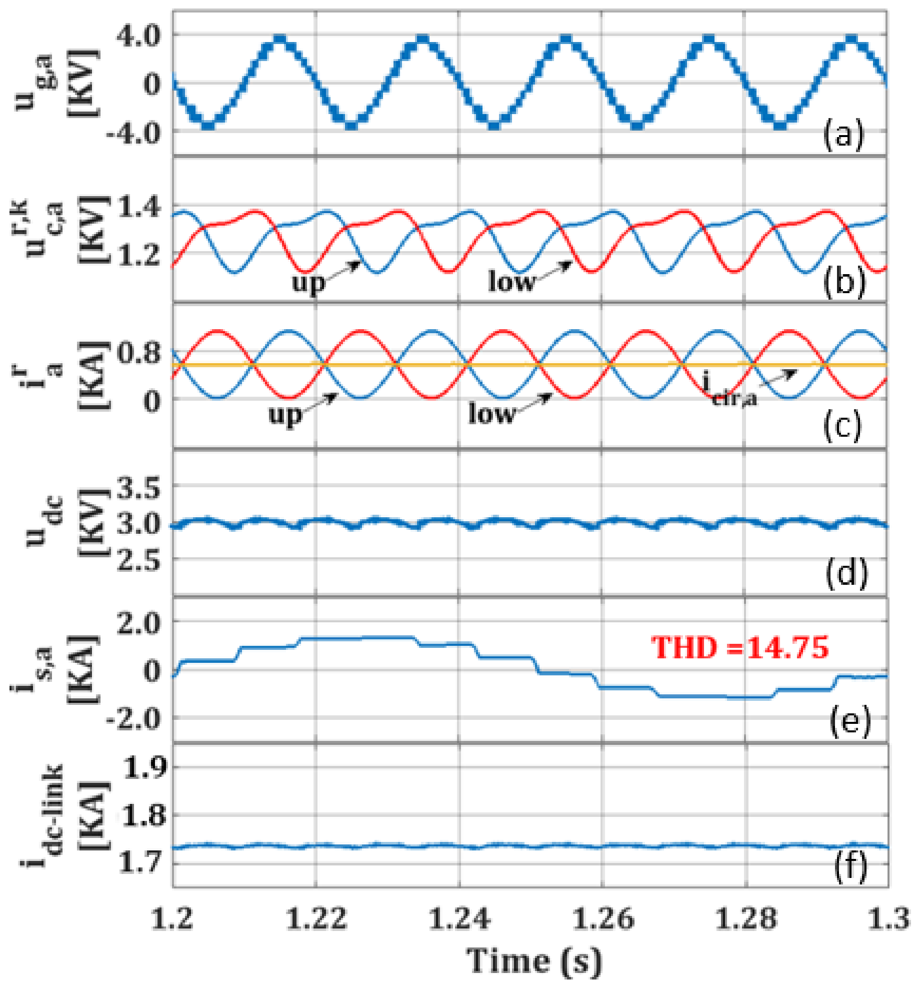


Figure 3-35 Boost mode operation, $U_{dc} = 3KV$, $f_s = 10Hz$, (a) FBMMC output voltage, (b) submodules capacitors voltages, (c) circulating current and arms currents, (d) dc-link voltage, (e) generator current, and (f) dc-link current

Figure 3-34 shows the system working in the buck mode condition with $\mathrm{U_{dc}} = 6.6\mathrm{KV},\ \mathrm{f_s} = 30\mathrm{Hz}$. Figure 3-35 illustrates the system operating in the boost mode condition with $\mathrm{U_{dc}} = 3\mathrm{KV},\ \mathrm{f_s} = 25\mathrm{Hz}$. Figure 3-34(a)(d) and Figure 3-35(a)(d) emphasis the boost capability of the FBMMC, as the output voltage of the FBMMC can be kept fixed regardless to the dc-link voltage. Moreover, Figure 3-34(b)(c)(e)(f) and Figure 3-35(b)(c)(e)(f) show the proposed control effectiveness, as all undesired ripples in SMs' capacitor voltages, circulating current and arms currents, generator current, and dc-link current are eliminated. Furthermore, these figures demonstrate that with the proposed control, the 12-pulse rectifier significantly enhances the generator phase current quality, with a THD of 14.75.

3.11.1 Proposed WECS configuration

A direct-drive configuration represents a significant step in the enhancement of the WECS performance. It is characterized by a gearless capability, in contrast to the gearbox-coupled wind turbine generator. The elimination of the gearbox is possible by employing a PMSG with a high-pole number. This configuration can reduce the overall size, and offers high-power density, reduced installation, and maintenance costs, together with flexible control and fast response to wind fluctuations [3] [65].

The conventional two/three level BTBC system is composed of a PWM rectifier that provides a regulated dc-link voltage and a PWM inverter that provides three-phase voltages synchronized to the grid. However, as the power is unidirectional, this configuration might not be necessary, and it suffers from the higher cost and lower efficiency compared to the PGSC system [3] [28] [65].

The FBMMC can be connected to the grid with an arbitrary dc-link voltage [28]. Also the FBMMC has robust dc-fault handling and ride-through capabilities [36]. The employment of the FBMMC in WECS allows the replacement of the PMW rectifier with a three-phase six-pulse diode rectifier, which offers improved reliability. Moreover, there is no need for a dc/dc boost converter in the dc-link, due to the voltage boost capability of the FBMMC. Furthermore, there is no need for a large LC filter in the dc-link as the FBMMC can also perform as an active filter. Therefore, in terms of the size, cost, complexity, and reliability, the integration of FBMMC with the PGSC system may be the optimal choice for WECS. A feasible circuit configuration for a 5MW and 10MW WECS based on PGSC system with FBMMC is show in Figure 3-36 and Figure 3-37, respectively. In Figure 3-36 and Figure 3-37 the grid side transformer can be removed as well. In [58], [59], and [60] the authors have presented a MPPT method for the PGSC system configuration.

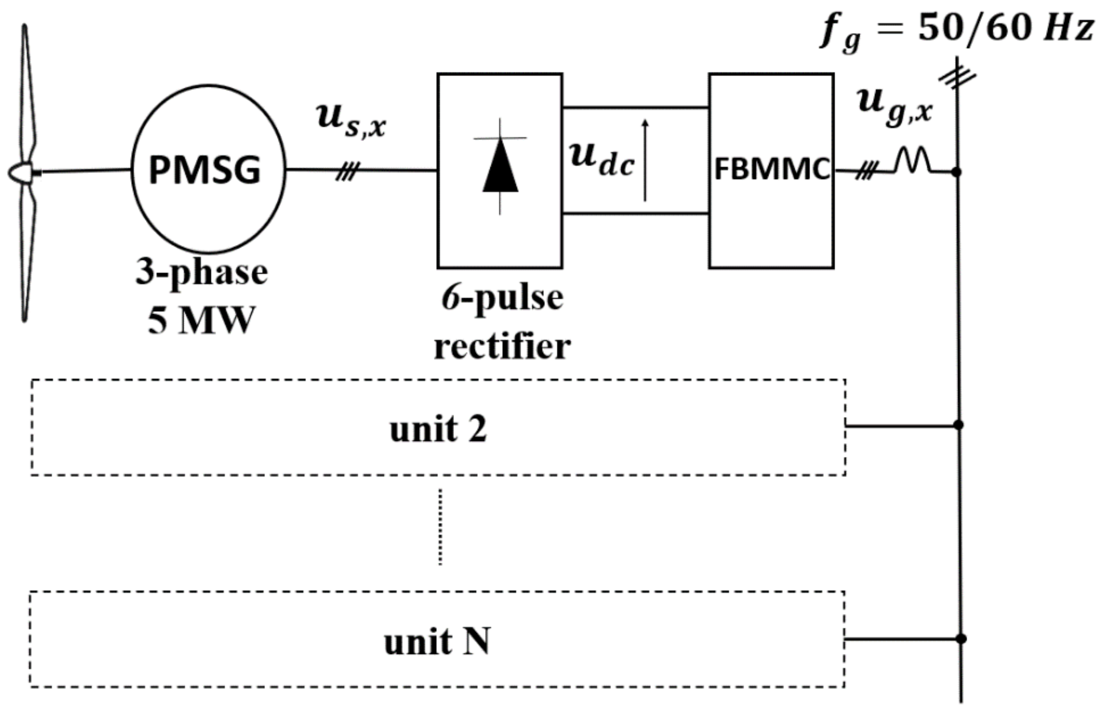


Figure 3-36 Proposed 5MW WECS based on PGSC with FBMMC

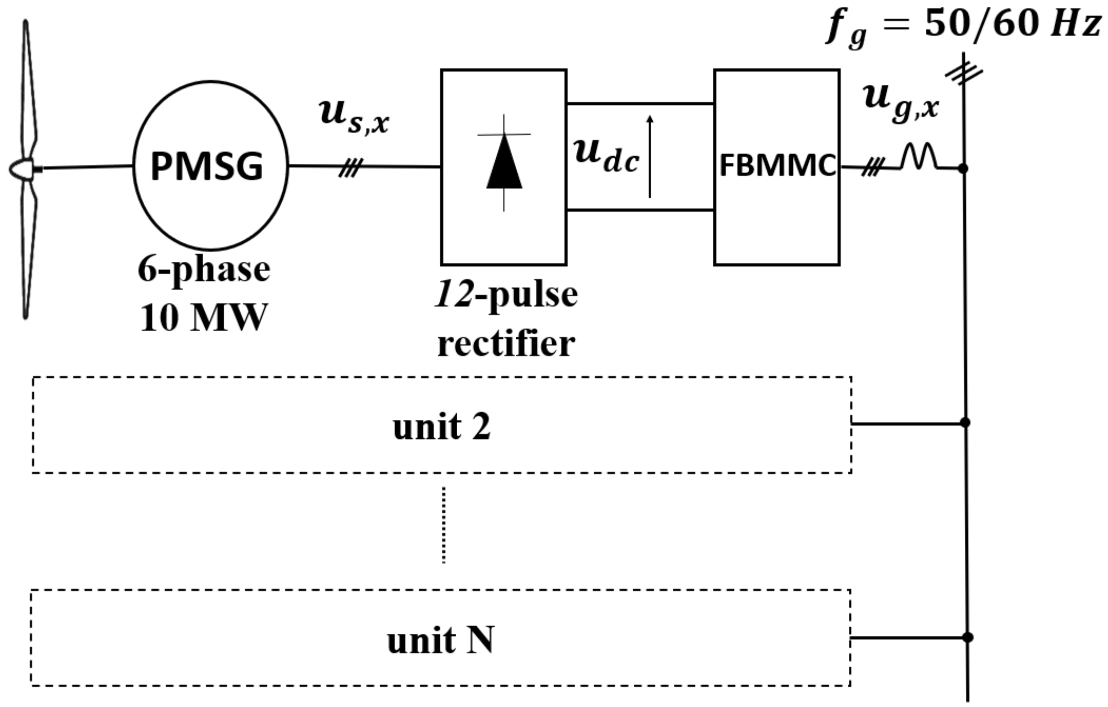


Figure 3-37 Proposed 10MW WECS based on PGSC with FBMMC

3.11.2 Maximum power point tracking

For MPPT algorithms with PGSC configuration, three main methods can be proposed, including power signal feedback (PSF) control [58] [60], hill-climb search (HCS) [59], and tip speed ratio (TSP) control [81].

In this work, the possibility of implementing the MPPT algorithm using the PSF method in the proposed system will be discussed further. In this control method, a power reference signal can be given using the MPPT curve (see Figure 3-38 [81]) which is based on measured wind (generator) speed (i.e. MPPT curve can be obtained from an equation of the optimum output power versus the wind speed) [58][60]. Here, a rotor speed (or wind speed) is set as the input. Then, the calculated power is sent as a reference to the control system of the grid-connected FBMMC [58][60].

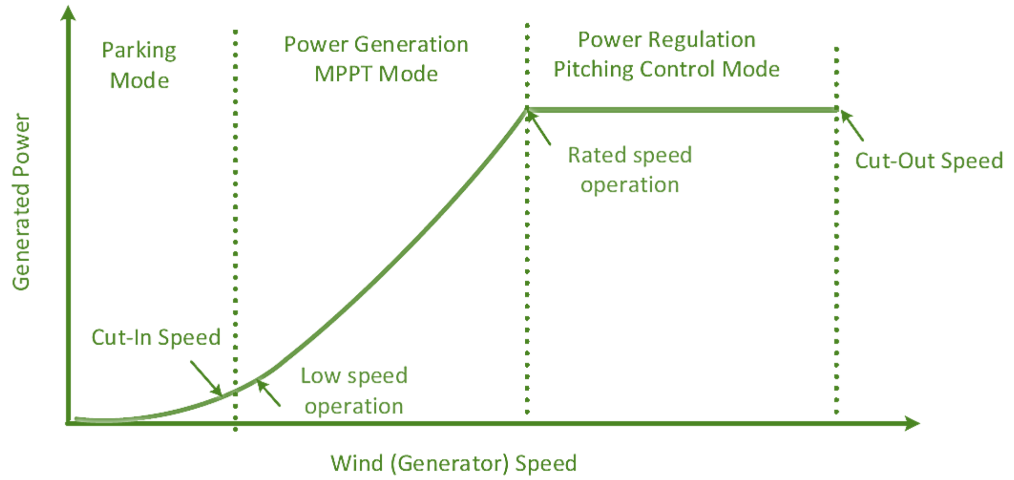


Figure 3-38 Typical behaviour of wind turbine speed

The behaviour of the wind turbine can be divided into three modes of operation, as explained in Figure 3-38. Here, the first region is a parking mode. This mode is activated when the wind turbine speed is lower than the cut-in speed. Because the generated power is insufficient, it can be identified as zero. The second region of wind turbine speed mode is found between higher than the cut-off speed and the rated speed. Here, the maximum power generated is found from the MPPT curve at the rated speed of operation. The third region is found between the rated speed to the cut-out speed. In this mode, even if the wind speed exceeds the rated value, the power output is limited to the rated value through adjusting the pitch angle of the wind turbine [81].

The block diagram, of the proposed system with the suggested MPPT algorithm using the PSF method is shown in Figure 3-39

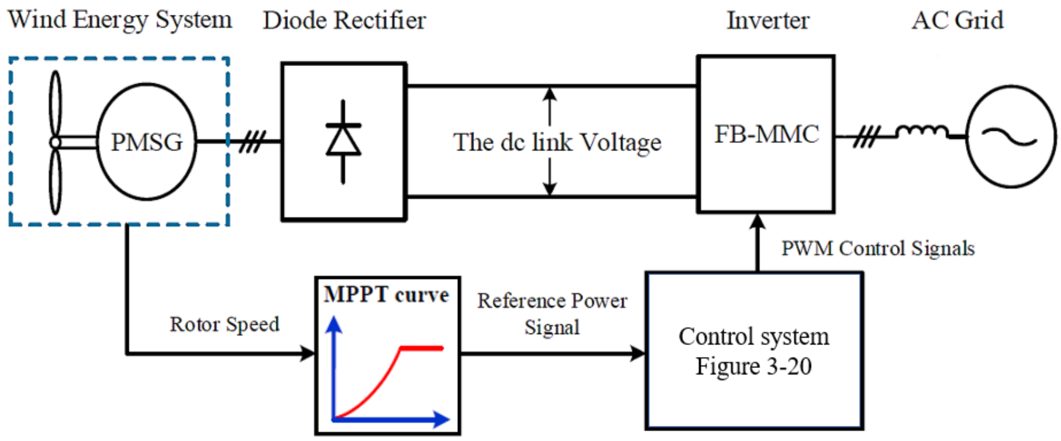


Figure 3-39 Proposed system with the MPPT algorithm

3.12 Summary

This chapter brings essential analysis regarding the primary aspects of the proposed WECS system with a FBMMC and a diode front-end. First, the main structure and operation of the 6-pulse and 12-pulse diode bridge rectifiers, together with analysis of their output voltages, is given. Then, the proposed system's characteristics, mathematical modelling, and control are provided. Also, the FBMMC's voltage boosting capability is analysed and exploited. The simulation and experiment results confirm that the FBMMC can operate as an active dc filter by removing the ripple from the dc-link current and generator currents. Consequently, the suggested system can assure proper operation without the need for passive components and a dc/dc boost converter in the dc-link, resulting in a low cost and high reliability.

Chapter 4: Steady-State Analysis of the proposed system, and parameters design guidance

4.1 Abstract

This chapter determines new design requirements of a grid-tied FBMMC connected to a diode-bridge front-end without passive components in the dc-link for wind energy conversion systems. It develops a new steady-state model of the full-bridge MMC with non-ideal dc-link voltage where MMC input impedance (Z_{MMC}) is modelled under different operation conditions (i.e., buck and boost modes) as a function of MMC parameters, including the dc-link dominant harmonic frequency. The analysis reveals that, in addition to the traditional second-order resonance frequency, the ripple in the dc-link may generate new resonance frequencies between the MMC sub-modules and arm inductances. However, all resonance frequencies can be prevented by the optimal selection of MMC parameters. Moreover, the conventional second-order impedance ($Z_{MMC_{2^{nd}}}$) is also modelled in boost modes condition which is not reported in the literature. The analysis reveals that the boost mode operation has a significant impact on the second-order resonance inductance.

4.2 Introduction

The critical components for MMC design are the capacitors of the SMs and the inductor of the arms. The arm inductances must be designed to be sufficiently high to attenuate high-frequency components in the circulating currents, limit surge currents at the short-circuit fault between the dc link terminals, and supress a resonance condition between the SMs' capacitors and arm inductors [50] [77] [102]. However, if the dc-link voltage is not a pure dc, the ripple in the dc-link voltage can potentially generate new critical resonance frequencies of the SM capacitances and arm inductances. An effective method for determining the resonance frequencies caused by the ripple in the dc-link voltage is to perform an average analytical model analysis.

In this chapter, the steady-state analytical mode for the proposed system is developed. The developed steady-state analytical model is applicable to any three-phase diode rectifier (i.e., with any number of pulses) as the front-end of the FBMMC and for the full operating range (i.e., both buck and boost modes). In this analysis, the boost mode is achieved by varying the dc-link voltage while the proposed system is connected to the stiff grid. Under these operating conditions, the developed analytical models enable the description of the impact of dc-link ripple on the arm currents, submodule capacitor currents, submodule capacitor voltages, submodule output voltages, arm voltages, and phase voltages. The developed analytical model provides the actual dc side impedance of the MMC, Z_{MMC}, for any ripple in the dc-link along with the associated resonance inductance for any current ripple in the dc link. A new guidance for designing the arm inductance is provided for the proposed system.

Furthermore, the literature does not report the resonance inductance associated with conventional second-order harmonics in boost mode. The developed analytical modelling also shows how the boost mode affects the resonance inductance of the circulating current's second-order harmonic component.

The capacitors of the SMs are chosen to contain the voltage ripple and restrict the maximum voltage stress on the devices. Typically, the design of the SMs capacitors is determined under the circulating currents’ (active) suppression mode of operation [50]. In the previous chapter, the simulation and experiment results demonstrated that the proposed controllers effectively suppressed the dc-link current ripple, which eliminated the dc-link ripple components in the SM capacitor voltage. Therefore, the dc-link current ripple has no effect on the capacitors’ design of the SMs.

This chapter will also provide a brief overview of the standard capacitor design of SMs, which is to restrict its voltage variations to 10% of its dc component [82].

Finally, the developed analytical model is verified by a comparison with MATALB simulation as well as experiment testing.

4.3 Selection of SM capacitor

The SM capacitor is chosen to contain the ripple voltage and limit the maximum voltage stress on the devices. For the operating mode with suppressed circulating currents, the SM capacitance is chosen according to the formula [82] [103]:

$$C_{SM} = \frac{S_m}{3\, k_m\, N\, \left(\frac{\Delta U_c}{2}\right) (U_c^0)^2} \left[1 - \left(\frac{k_m \cos(\varphi)}{2}\right)^2\right]^{\frac{3}{2}} \tag{4.1}$$

In equation (4.1), k_m is referring to the converter modulation index ($k_m = 2U_m/U_{dc}$), φ is the ac-side/grid current phase angle, and S_m is the apparent power. ΔU_c is the desired SM capacitor voltage ripple and is defined as the percentage of peak-to-peak SM capacitor voltage [104], and can be given as:

$$\Delta U_c(\%) = \frac{(\max\left[\mathrm{u}_{\mathrm{c,x}}^{r,k}(t)\right] - \min\left[\mathrm{u}_{\mathrm{c,x}}^{r,k}(t)\right])}{U_c^0} \times 100 \tag{4.2}$$

This work follows the standard and most common design for the SM capacitors which is to design the SM capacitor high enough to keep the $\Delta U_c \approx 10\%$ [51] [82] [89].

4.4 Selection of arm inductors

The selection of the arm inductances is dependent on the circulating current ripple components. For the proposed system with a non-ideal dc-link (i.e., no large LC filter in the dc-link), and taking into consideration only the most dominant ripple, the circulating current ripple component ($i_{z,x}$) can be found from equation (3.44) as below:

$$i_{z,x} = i_{z,x,2} + i_{Pif_s} \tag{4.3}$$

The arm inductance must be selected to be sufficiently high to suppress the circulating current ripple component to reasonable value before applying the circulating current suppression control [102]. Supressing extremely high circulating current components purely through a controller will lead to an increase in the related harmonic components in the modulation signal, which might reduce the converter utilisation factor and introduce additional high frequency harmonics in the MMC output voltage harmonic spectrum [102] [105]. Moreover, low arms inductances make the system more vulnerable to the dc-link short-circuit faults [77]. The maximum value of the circulating current ripple components is found at and around resonance frequencies. Therefore, for the best performance and a more robust system, the arm inductances must be selected to be sufficiently above the circulating current resonance inductances [49] [50] [102] [104].

4.4.1 Resonance Phenomenon of the FBMMC

For the MMC, the cascaded SMs' capacitors and arm inductors can form a resonance at each ripple component in the arm current. Each ripple component in the MMC's arms is associated with its own resonant point [49] [50] [104]. At the resonant frequency the summation of total impedances created by the C_{SM} and L_{arm} is alomst zero and the current ripple is only limited by the arm resistance R_{arm} [49] [50] [104]. However, from the efficiency point of view, R_{arm} should be kept as low as possible and thus resonant frequencies must be avoided by properly selecting the C_{SM} and L_{arm} while considering all possible resonances in the MMC arms [49] [50] [104].

The existing design guidance in the literature, is provided under the assumption of a ripple-free dc-link and only buck mode condition (which is sufficient for HBMMCs). With a pure dc-link the most dominant ripple in the circulating current is the second-order harmonic component related to the grid frequency $i_{z,x,2}$. For HBMMCs, the existing literature has found the resonance inductance ($L_{res_{2H}}$) associated with $i_{z,x,2}$ as below [49] [50] :

$$L_{res_{2H}} = \frac{5\mathrm{N}}{48\omega^2 C_{SM}} \tag{4.4}$$

The L_{arm} is then selected based on (4.4) to be sufficiently higher than a resonant inductance L_{res_2} for optimal performance and a more reliable system [49] [50] [104].

However, Equation (4.4) only provides the resonance inductance for $i_{z,x,2}$, and is valid only when the FBMMC operates in buck mode. The literature does not present the resonance inductance associated with $i_{z,x,2}$ when the FBMMC operates in boost mode. Furthermore, under nonideal dc-link voltage, the resonance inductance for i_{Pif_s} is more complicated because it is influenced not only by the different dc-link voltage levels but also, and perhaps more importantly, by the generator frequency f_s, which varies with the wind speed.

One efficient method for evaluating resonance frequencies related to $i_{z,x,2}$ *and* i_{Pif_s} is through the circular interaction analytical model analysis, in which the key is to derive analytical expression of $i_{z,x,2}$ and i_{Pif_s} under different operating conditions. From this analysis, the related impedances can be found, and thus, the resonance inductance can be determined.

4.5 Circular interaction analytical model analysis

In this work the developed analytical model analysis is different from [83], as it is taking into consideration a nonideal dc-link and both buck and boost operation modes of the FBMMC. Figure 4-1 shows a simplified single-phase average model of the proposed system. It is brought here again to simplify the explanation.

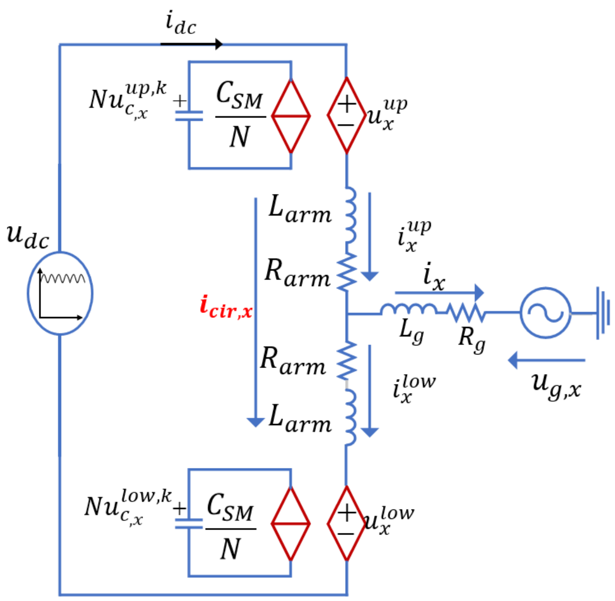


Figure 4-1 Simplified single-phase circuit of the proposed system

As mentioned, finding the mathematical expressions of $i_{z,x,2}$ and i_{Pif_s} determines their related resonance inductance. The workflow towards finding their mathematical expressions is described in Figure 4-2.

In summary, the upper/lower arm current run through the upper/lower SMs together with switching processes generating the voltage across the SMs in the upper arm u_x^{up} and lower arm u_x^{low}. Then, by summation u_x^{up} and u_x^{low}(i.e., $u_x^{up} + u_x^{low}$) the voltage across the MMC phases u_x^{ph} can be found [83]. The u_x^{ph} will contain dc components, ripple components associated with the second order harmonic ($u_{2,x}^{ph}$), ripple components associated with the rectifier current harmonics ($u_{Pif_s}^{ph}$), and other low-frequency and high-frequency ripple components.

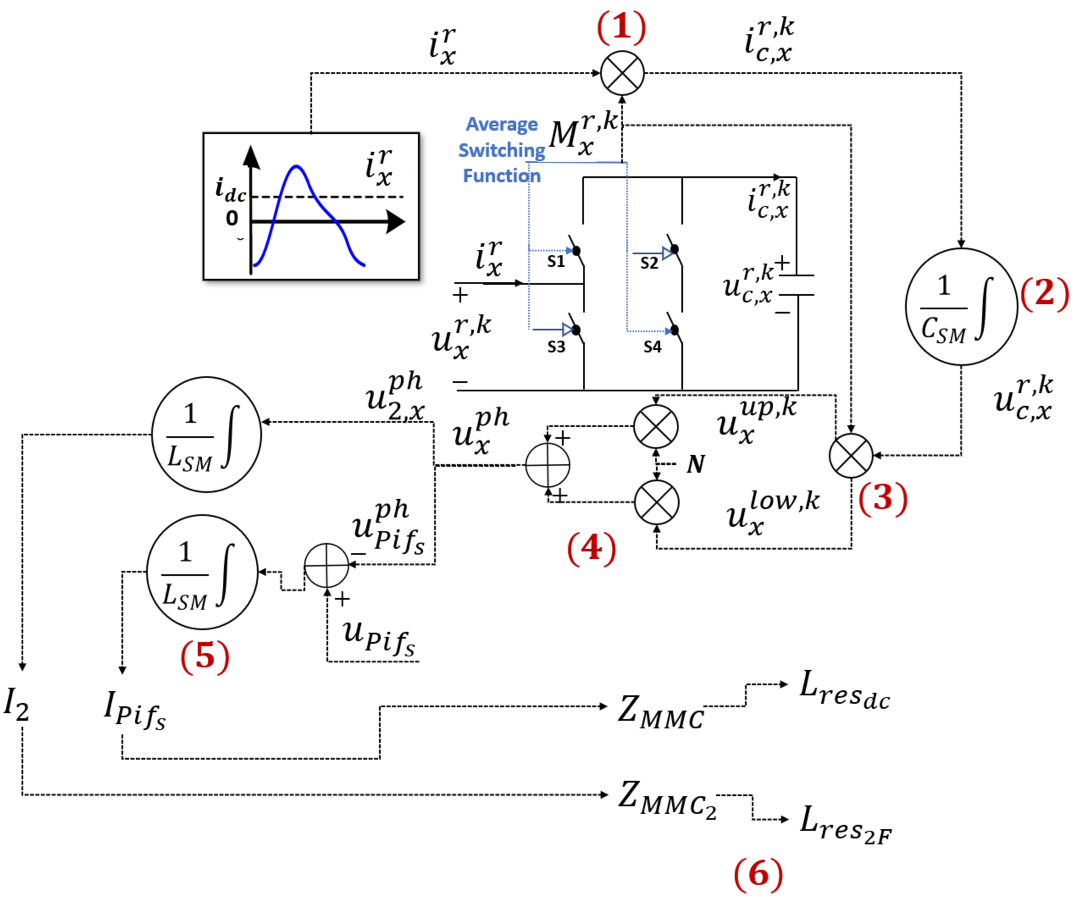


Figure 4-2 Workflow of the analytical model

Therefore, by finding $u_{2,x}^{ph}$, the expression formula of $i_{z,x,2}$ can be obtained as follows:

$$i_{z,x,2} = \frac{u_{2,x}^{ph}}{2\omega 2L_{arm}} \tag{4.5}$$

From, equation (3.2) and by applying Kirchhoff's voltage-law in Figure 4-1, the i_{Pif_s} formula can be found as below.

$$i_{Pif_s} = \frac{u_{Pif_s} - u_{Pif_s}^{ph}}{Pi\omega_s 2L_{arm}} \tag{4.6}$$

In this stage u_2^{ph} and $u_{Pif_s}^{ph}$ are unknown, they will be found by the analytical model.

Before describing the methods and techniques for analysing analytical models, it is necessary to make some assumptions for the sake of simplicity and clarity.

- The FBMMC is operating in inverter mode in this work. Thus, power is transmitted from the dc side to the ac side of the converter with no power losses (i.e., R_{arm} is ignored). Moreover, the high frequency harmonics are ignored for simplicity as well.
- The influence of the circulating current suppression control is omitted from this steady-state analytical model. Moreover, it is assumed that all FBSMs are identical and naturally balanced.

- The primary goals are to find the resonance inductance related to $i_{z,x,2}$ and i_{Pif_s}. These can be obtained from the actual expressions defining the amplitudes of these current components separately. The expressions describing the phase angles will be ignored.
- For the sake of simplicity, all unnecessary ripple components will be ignored in this developed analytical model. Note, the high-frequency ripple components will be presented in the next chapter.

The arm current is the convergence point for all electrical quantities in this system, hence arm currents should be the starting point for the analytical model [83]. From equations (3.33), (3.34), and (3.44) the upper arm current and lower arm current can be expressed as:

$$i_x^{\mathrm{up}} = \frac{1}{2} I_m \sin(\omega t + \varphi) + I_{dc} + I_2 \sin(2\omega t + \theta) + I_{Pif_s} sin(Pi\omega_s) \tag{4.7}$$

$$i_x^{low} = \frac{-1}{2} I_m \sin(\omega t + \varphi) + I_{dc} + I_2 \sin(2\omega t + \theta) + I_{Pif_s} sin(Pi\omega_s) \tag{4.8}$$

Where, I_2 and θ are the amplitude and phase shift of the circulating current 2nd-order harmonic component, respectively. I_{Pif_s} is the amplitude of the dc-link ripple component (at a frequency of $Pi\omega_s$) in the FBMMC phase.

The essential steps of this analytical derivation are depicted in Figure 4-2. More details will be presented in the following subsection.

4.5.1 Step 1: Calculating the SM capacitor current $\boldsymbol{i_{c,x}^{r,k}}$

As seen from Figure 4-2, the first step of the analytical model starts by finding the SM capacitor current ($i_{c,x}^{r,k}$). The SM capacitor current is the result of multiplying the arm current by the average switching function. The average switching function for the upper arm and lower arm can be represented from equation (3.22) and (3.23) as:

$$\mathrm{M_x^{up,k}} = \frac{\mathrm{M_{dc}}}{2} - \frac{\mathrm{M_{ac}}}{2}\sin(\omega t) \tag{4.9}$$

$$\mathrm{M_x^{low,k}} = \frac{\mathrm{M_{dc}}}{2} + \frac{\mathrm{M_{ac}}}{2}\sin(\omega t) \tag{4.10}$$

Thus, the SM capacitor current in the upper arm can be found as $i_{c,x}^{up,k}$:

$$\begin{aligned}
\mathrm{i_{c,x}^{up,k}} = \mathrm{i_x^{up}} \times \mathrm{M_x^{up,k}} = {} & \underbrace{\frac{\mathrm{I_{dc}M_{dc}}}{2} - \frac{\mathrm{I_m M_{ac}}\cos(\varphi)}{8}}_{\text{dc component}} \\
& \underbrace{- \frac{\mathrm{I_{dc}M_{ac}}\sin(\omega t)}{2} + \frac{\mathrm{I_m M_{dc}}\sin(\omega t + \varphi)}{4} - \frac{\mathrm{I_2\ M_{ac}}\cos(\omega t + \theta)}{4}}_{\text{fundamental components}} \\
& \underbrace{+ \frac{\mathrm{I_m M_{ac}}\cos(2\omega t + \varphi)}{8} + \frac{\mathrm{I_2 M_{dc}}\sin(2\omega t + \theta)}{2}}_{\text{second components}} \underbrace{+ \frac{\mathrm{I_2\ M_{ac}}\cos(3\omega t + \theta)}{4}}_{\text{third components}} \\
& + \underbrace{\frac{\mathrm{I_{Pif_s} M_{dc}}\sin(\mathrm{Pi}\omega_s t)}{2}}_{\text{main rectifier components}} \\
& \underbrace{- \frac{\mathrm{I_{Pif_s} M_{ac}}\cos(\mathrm{Pi}\omega_s t - \omega t)}{4} + \frac{\mathrm{I_{Pif_s} M_{ac}}\cos(\mathrm{Pi}\omega_s t + \omega t)}{4}}_{\text{interaction components}}
\end{aligned} \tag{4.11}$$

The SM capacitor current in the lower arm can be found as $i_{c,x}^{low,k}$:

$$\mathrm{i}_{c,x}^{low,k} = \mathrm{i}_x^{low} \times \mathrm{M}_x^{low,k} = \underbrace{\frac{\mathrm{I_{dc}M_{dc}}}{2} - \frac{\mathrm{I_m M_{ac}}\cos(\varphi)}{8}}_{\text{dc component}}$$

$$\underbrace{+\frac{\mathrm{I_{dc}M_{ac}}\sin(\omega t)}{2} - \frac{\mathrm{I_m M_{dc}}\sin(\omega t+\varphi)}{4} + \frac{\mathrm{I_2\,M_{ac}}\cos(\omega t+\theta)}{4}}_{\text{fundamental components}}$$

$$\underbrace{+\frac{\mathrm{I_m M_{ac}}\cos(2\omega t+\varphi)}{8} + \frac{\mathrm{I_2 M_{dc}}\sin(2\omega t+\theta)}{2}}_{\text{second components}} \underbrace{- \frac{\mathrm{I_2\,M_{ac}}\cos(3\omega t+\theta)}{4}}_{\text{third components}} \qquad (4.12)$$

$$+\underbrace{\frac{\mathrm{I_{Pif_s}M_{dc}}\sin(\mathrm{Pi}\omega_s t)}{2}}_{\text{main rectifier components}}$$

$$\underbrace{+\frac{\mathrm{I_{Pif_s}M_{ac}}\cos(\mathrm{Pi}\omega_s t-\omega t)}{4} - \frac{\mathrm{I_{Pif_s}M_{ac}}\cos(\mathrm{Pi}\omega_s t+\omega t)}{4}}_{\text{interaction components}}$$

The capacitor current gives the first impression about the ripple components in the system. From equations (4.11) and (4.12), the original current ripple components of the SM capacitor are the **first**, **second**, and **third order harmonic components**. These are produced by the FBMMC ac side current during the switching process even under pure dc-link current. However, the **main rectifier component** of the SM capacitor current is generated by the voltage ripple in the dc-link. Moreover, during the switching process, the dc-link ripple causes additional **interaction components.** The additional interaction components are found at $Pif_s \pm f_g$. During the steady state, the dc components in the SM capacitor current are zero, as the active power between the dc-side and ac side is balanced, and thus the dc components are ignored in the next calculation, for simplicity [83].

4.5.2 Step 2: Calculating the SM capacitor voltage $\boldsymbol{u_{c,x}^{r,k}}$

The analytical expressions of voltages across the SM capacitor in the upper arm $u_{c,x}^{up,k}$ and the lower arm $u_{c,x}^{low,k}$ can be found by:

$$\begin{aligned}\mathrm{u_{c,x}^{r,k}(t)} &= \frac{1}{\mathrm{C_{SM}}}\int \mathrm{i_{c,x}^{r,k}\,(t)} \\ &= \mathrm{u_{c,1}^{r}(t) + u_{c,2}^{r}(t) + u_{c,3}^{r}(t) + u_{c,Pif_s}^{r}(t) + u_{c,(Pif_s+f_g)}^{r}(t)} \\ &\quad + \mathrm{u_{c,(Pif_s-f_g)}^{r}(t)}\end{aligned} \tag{4.13}$$

Where $u_{c,1}^{r}, u_{c,2}^{r}, and\; u_{c,3}^{r}$ are the fundamental, second, and third order components of the SM capacitor voltage, respectively. $u_{c,Pif_s}^{r},\; and\; \left(u_{c,(Pif_s+f_g)}^{r}, u_{c,(Pif_s-f_g)}^{r}\right)$ are the main rectifier and the interaction components in SM capacitor voltage, respectively. Therefore, for the upper arm, the SM capacitor voltage ripple components are found as:

$$\mathrm{u_{c,1}^{up}(t)} = \frac{\mathrm{I_{dc}M_{ac}\cos(\omega t)}}{\mathrm{2\;C_{SM}\;\omega}} - \frac{\mathrm{I_m M_{dc}\cos(\omega t+\varphi)}}{\mathrm{4\;C_{SM}\;\omega}} - \frac{\mathrm{I_2\;M_{ac}\sin(\omega t+\theta)}}{\mathrm{4\;\;C_{SM}\;\omega}} \tag{4.14}$$

$$\mathrm{u_{c,2}^{up}(t)} = -\frac{\mathrm{I_2 M_{dc}\cos(2\omega t+\theta)}}{\mathrm{4\;C_{SM}\;\omega}} + \frac{\mathrm{I_m M_{ac}\sin(2\omega t+\varphi)}}{\mathrm{16\;C_{SM}\;\omega}} \tag{4.15}$$

$$u_{c,3}^{up}(t) = \frac{I_2\ M_{ac}\sin(3\omega t + \theta)}{12\ \ C_{SM}\ \omega} \tag{4.16}$$

$$u_{c,Pif_s}^{up}(t) = \frac{-I_{Pif_s} M_{dc} \cos(Pi\omega_s t)}{2\ C_{SM} Pi\omega_s} \tag{4.17}$$

$$u_{c,(Pif_s+f_g)}^{up}(t) = \frac{I_{Pif_s} M_{ac}\sin(Pi\omega_s t + \omega t)}{4\ C_{SM}\ (Pi\omega_s + \omega)} \tag{4.18}$$

$$u_{c,(Pif_s-f_g)}^{up}(t) = \frac{-I_{Pif_s} M_{ac}\sin(Pi\omega_s t - \omega t)}{4\ C_{SM}\ (Pi\omega_s - \omega)} \tag{4.19}$$

Next, the lower arm SM capacitor voltage ripple components are found as:

$$\begin{aligned} u_{c,1}^{low}(t) = \frac{I_{dc} M_{ac} \cos(\omega t)}{2\ C_{SM}\ \omega} - \frac{I_m M_{dc} \cos(\omega t + \varphi)}{4\ C_{SM}\ \omega} \\ - \frac{I_2\ M_{ac}\sin(\omega t + \theta)}{4\ \ C_{SM}\ \omega} \end{aligned} \tag{4.20}$$

$$u_{c,2}^{low}(t) = -\frac{I_2 M_{dc}\cos(2\omega t + \theta)}{4\ C_{SM}\ \omega} + \frac{I_m M_{ac}\sin(2\omega t + \varphi)}{16\ C_{SM}\ \omega} \tag{4.21}$$

$$u_{c,3}^{low}(t) = \frac{I_2\ M_{ac}\sin(3\omega t + \theta)}{12\ \ C_{SM}\ \omega} \tag{4.22}$$

$$u_{c,Pif_s}^{low}(t) = \frac{-I_{Pif_s} M_{dc} \cos(Pi\omega_s t)}{2\ C_{SM} Pi\omega_s} \tag{4.23}$$

$$u_{c,(Pif_s+f_g)}^{low}(t) = \frac{I_{Pif_s} M_{ac}\sin(Pi\omega_s t + \omega t)}{4\ C_{SM}\ (Pi\omega_s + \omega)} \tag{4.24}$$

$$u_{c,(Pif_s-f_g)}^{low}(t) = \frac{-I_{Pif_s} M_{ac}\sin(Pi\omega_s t - \omega t)}{4\ C_{SM}\ (Pi\omega_s - \omega)} \tag{4.25}$$

As can be seen, all voltage ripple components across the SM capacitor are function of M_{dc} and M_{ac}, this means the boost mode has a significant impact on selecting the SM capacitor design. Numerous publications use this characteristic to reduce the size of the capacitor [84] [106] [107], in which the FBMMC is used to operate under certain boost mode conditions to achieve the lowest ΔU_c. The SM capacitor can then be made smaller. The lowest ΔU_c is found by the previous literature, when $k_m = 1.414$ [84] [106] [107]. However, in this system, the voltage on the dc-link varies and is dependent on the wind speed. Because of this, the system cannot be operated at a particular boost mode condition. As was stated previously, the standard SM capacitor design will therefore be utilised.

The voltage ripple components across the SM capacitor such as $u^r_{c,Pif_s}, u^r_{c,(Pif_s+f_g)}, and\ u^r_{c,(Pif_s-f_g)}$ are functions of I_{Pif_s}. However, as the SM capacitor design is decided under the circulating current suppression mode, the above components, which are introduced by a non-ideal dc-link, don't have any impact in the selection of SMs capacitors.

4.5.3 Step 3: Calculating the voltage ripple components across the SM terminal $\boldsymbol{u_x^{r,k}}$

As seen in Figure 4-2, the voltage ripple across the SM terminal can be found by:

$$\mathrm{u_x^{up,k}}\ (\mathrm{t}) = \mathrm{M_x^{up,k}}(\mathrm{t})\ \times \mathrm{u_{c,x}^{up,k}}(\mathrm{t}) \tag{4.26}$$

$$u_x^{low,k}(t) = M_x^{low,k}(t) \times u_{c,x}^{low,k}(t) \tag{4.27}$$

4.5.4 Step 4: Calculating the voltage ripple components across the FBMMC phase $\boldsymbol{u_x^{ph}}$

The ripple components of voltage across the FBMMC phase u_x^{ph} can be found by the sum of the voltages across the SM ac terminals in the upper $u_x^{up,k}$ and lower arms $u_x^{low,k}$ as following:

$$u_x^{ph}(t) = \left(\left(u_x^{up,k}(t)\right) \times N\right) + \left(\left(u_x^{low,k}(t)\right) \times N\right) =$$

$$\underbrace{\begin{gathered}-\frac{I_2 M_{ac}^2\ N\cos(2\omega t+\theta)}{8\,C_{SM}\,\omega} - \frac{I_{dc}\ M_{ac}^2\ N\sin(2\omega t)}{4\,C_{SM}\,\omega} \\ + \frac{I_m\,M_{dc}\,M_{ac}\,N\sin(2\omega t+\varphi)}{8\,C_{SM}\,\omega} \\ - \frac{I_2\,M_{dc}^2\,N\cos(2\omega t+\theta)}{4\,C_{SM}\,\omega} \\ + \frac{I_m\,M_{ac}\,M_{dc}\,N\sin(2\omega t+\varphi)}{16\,C_{SM}\,\omega} \\ - \frac{I_2\,M_{ac}^2\,N\cos(2\omega t+\theta)}{24\ C_{SM}\,\omega}\end{gathered}}_{\text{Part (1) } 2^{nd} \text{ components}, u_{2,x}^{ph}} \tag{4.28}$$

$$+\underbrace{\frac{I_2\,M_{ac}^2\,N\cos(4\omega\,t+\theta)}{24\,C_{SM}\,\omega}}_{\text{part(2) }4^{th}\text{ components}}$$

$$\underbrace{-\frac{I_{Pif_s}\,M_{dc}^2\,N\cos(Pi\omega_s t)}{2\,C_{SM}Pi\omega_s}-\frac{I_{Pif_s}M_{ac}^2\,N\cos(Pi\omega_s t)}{8\,C_{SM}\,(Pi\omega_s-\omega\,)}-\frac{I_{Pif_s}M_{ac}^2\,N\cos(Pi\omega_s t)}{8\,C_{SM}\,(Pi\omega_s+\omega\,)}}_{\text{Part (3)main rectifier components, }u_{Pif_s}^{ph}}$$

$$\underbrace{+\frac{I_{Pif_s}M_{ac}^2\,N\cos(Pi\omega_s t-2\omega\,t)}{8\,C_{SM}\,(Pi\omega_s-\omega\,)}+\underbrace{\frac{I_{Pif_s}M_{ac}^2\,N\cos(Pi\omega_s t+2\omega\,t)}{8\,C_{SM}(Pi\omega_s+\omega\,)}}}_{\text{Part (4)interaction components}}$$

From equation (4.28), the undesired components related to the grid frequency in the voltage across the FBMMC phases are the second and fourth ripple components. Moreover, undesired components related to the generator frequency are the main rectifier voltage ripple components and the related interaction ripple component. The interaction ripple components across the FBMMC phase are found at $Pif_s \pm 2f_g.$ It is evident that the fourth component of the ripple is a result of the second component, so it will be disregarded for simplicity. Similarly, the interaction components are a consequence of the primary rectifier ripple components, so they will also be disregarded for the sake of simplicity.

From equation (4.28) Part (1), the second-harmonic voltage $u_{2,x}^{ph}$ associated with the second-order harmonic circulating current can be presented as

$$u_{2,x}^{ph}(t) = -\frac{I_2 M_{ac}^2\ N \cos(2\omega\, t + \theta)}{6\ C_{SM}\ \omega} + \frac{3I_m\ M_{dc}\ M_{ac}\ N \sin(2\omega\, t + \varphi)}{16\ C_{SM}\ \omega} - \frac{I_{dc}\ M_{ac}^2\ N \sin(2\omega\, t)}{4\ C_{SM}\ \omega} - \frac{I_2\ M_{dc}^2\ N \cos(2\omega\, t + \theta)}{4\ C_{SM}\ \omega} \quad (4.29)$$

From equation (4.28) Part (3), the main rectifier ripple component across the FBMMC phase is found as;

$$u_{Pif_s}^{ph}(t) = -\frac{I_{Pif_s}\ M_{dc}^2\ N \cos(Pi\omega_s t)}{2\ C_{SM} Pi\omega_s} - \frac{I_{Pif_s} M_{ac}^2\ N \cos(Pi\omega_s t)}{8\ C_{SM}\ (Pi\omega_s - \omega\ )} - \frac{I_{Pif_s} M_{ac}^2\ N \cos(Pi\omega_s t)}{8\ C_{SM}\ (Pi\omega_s + \omega\ )} \quad (4.30)$$

4.5.5 Step 5: Driving the key equations of the main current ripple in the FBMMC arms

From equation (4.3), it is understood that the proposed system arms currents have two main unknown components: $i_{z,x,2}$ related to the grid frequency and i_{Pif_s} related to the generator frequency. As seen in Figure 4-2, the analytical expression of $i_{z,x,2}$ can be found by integrating the second-harmonic voltage across the phase, as it follows.

$$
\begin{aligned}
\mathrm{i}_{z,x,2} &= \frac{1}{2\mathrm{L_{arm}}}\int \mathrm{u}_2^{\mathrm{ph}}(\mathrm{t})\mathrm{dt} \\
&= \frac{\mathrm{I_2 M_{ac}^2\ N \sin(2\omega\, t+\theta)}}{24\omega_g^2\ \mathrm{C_{SM}\ L_{arm}}} - \frac{\mathrm{I_{dc}\ M_{ac}^2\ N\cos(2\omega\, t)}}{16\omega_g^2\ \mathrm{C_{SM}\ L_{arm}}} \\
&+ \frac{3\mathrm{I_m\ M_{dc}\ M_{ac}\ N\cos(2\omega\, t+\varphi)}}{64\ \omega_g^2 \mathrm{C_{SM}\ L_{arm}}} \\
&+ \frac{\mathrm{I_2\ M_{dc}^2\ N\sin(2\omega\, t+\theta)}}{16\omega_g^2\ \mathrm{C_{SM}\ L_{arm}}}
\end{aligned} \tag{4.31}
$$

From equation (4.31), the amplitude of $i_{z,x,2}$ can be solved as it follows:

$$
\mathrm{I_2} = \frac{\sqrt{(\mathrm{A}\cos\varphi+\mathrm{B})^2+(\mathrm{A}\sin\varphi)^2}}{1-\dfrac{\mathrm{N\ M_{dc}^2}}{16\ \mathrm{C_{SM}\ L_{arm}}\,\omega^2}-\dfrac{\mathrm{N\ M_{ac}^2}}{24\ \mathrm{C_{SM}\ L_{arm}}\,\omega^2}}
$$

where

$$
\mathrm{A} = \frac{3\ \mathrm{N\ M_{ac}\ M_{dc}\ I_m}}{64\ \mathrm{C_{SM}\ L_{arm}}\,\omega^2} \tag{4.32}
$$

$$
\mathrm{B} = \frac{-\ \mathrm{N\ M_{ac}^2\ I_{dc}}}{16\ \mathrm{C_{SM}\ L_{arm}}\,\omega^2}
$$

The amplitude of the circulating current second-order harmonic related to the grid frequency I_2 is a function of M_{dc} and M_{ac}. This implies that the operation of the boost mode will most likely have an impact on the design of the arm inductance. This is due to the M_{dc} and M_{ac} have different values under different dc-link voltage levels.

Similarly, from equation (4.6) and equation (4.30), the key equation representing the main rectifier current ripple in the FBMMC phase i_{Pif_s} can be obtained by the following:

$$
\begin{aligned}
\mathrm{i}_{\mathrm{Pif_s}} &= \frac{1}{2\mathrm{L_{arm}}}\int (\mathrm{u_{Pif_s}}(\mathrm{t}) - \mathrm{u}^{\mathrm{ph}}_{\mathrm{Pif_s}}(\mathrm{t}))\,\mathrm{dt} \\
&= \frac{-\mathrm{U_{Pif_s}}\cos(\mathrm{Pi}\omega_\mathrm{s}\mathrm{t})}{2\mathrm{L_{arm}}\mathrm{Pi}\omega_\mathrm{s}} + \frac{\mathrm{I_{Pif_s}}\,\mathrm{M^2_{dc}}\,\mathrm{N}\sin(\mathrm{Pi}\omega_\mathrm{s}\mathrm{t})}{4\,\mathrm{C_{SM}}\mathrm{L_{arm}}(\mathrm{Pi}\omega_\mathrm{s})^2} \\
&+ \frac{\mathrm{I_{Pif_s}}\mathrm{M^2_{ac}}\,\mathrm{N}\sin(\mathrm{Pi}\omega_\mathrm{s}\mathrm{t})}{16\,\mathrm{C_{SM}}\mathrm{L_{arm}}\mathrm{Pi}\omega_\mathrm{s}\,(\mathrm{Pi}\omega_\mathrm{s} - \omega)} \\
&+ \frac{\mathrm{I_{Pif_s}}\mathrm{M^2_{ac}}\,\mathrm{N}\sin(\mathrm{Pi}\omega_\mathrm{s}\mathrm{t})}{16\,\mathrm{C_{SM}}\mathrm{L_{arm}}\mathrm{Pi}\omega_\mathrm{s}\,(\mathrm{Pi}\omega_\mathrm{s} + \omega)}
\end{aligned}
\tag{4.33}
$$

The amplitude of i_{Pif_s} can be solve as follows:

$$
\mathrm{I_{Pif_s}} = \frac{\mathrm{U_{Pif_s}}}{2\ \mathrm{L_{arm}}\,\mathrm{Pi}\omega_\mathrm{s} \times \mathrm{D}}
$$

where

$$
\begin{aligned}
\mathrm{D} = \quad 1 - \Bigg(&\frac{\mathrm{M^2_{dc}}\,\mathrm{N}}{4\,\mathrm{C_{SM}}\ \mathrm{L_{arm}}\,(\mathrm{Pi}\omega_\mathrm{s})^2} + \frac{\mathrm{M^2_{ac}}\,\mathrm{N}}{16\,\mathrm{C_{SM}}\,\mathrm{L_{arm}}\,\mathrm{P}\omega_\mathrm{s}\,(\mathrm{Pi}\omega_\mathrm{s} - \omega)} \\
&+ \frac{\mathrm{M^2_{ac}}\,\mathrm{N}}{16\mathrm{C_{SM}}\,\mathrm{L_{arm}}\,\mathrm{P}\omega_\mathrm{s}\,(\mathrm{Pi}\omega_\mathrm{s} + \omega)}\Bigg)
\end{aligned}
\tag{4.34}
$$

M_{dc} *and* M_{ac} have a similar effect on the amplitude of the dc-link current ripple across the inverter phases I_{Pif_s}. The value of U_{Pif_s} can be found by equation (4.14). Note, the ripple voltage across the phase in equation (4.28) Part(2) also will create a fourth-order ripple related to the grid frequency in the circulating current $i_{z,x,4}$. The $i_{z,x,4}$ is a result of the $i_{z,x,2}$. Moreover, Part (4) in equation (4.28), will cause the interaction ripple components in the circulating current related to the generator frequency $i_{(Pif_s \pm 2f_g)}$, these are result of the main rectifier current ripple i_{Pif_s} .

The $i_{z,x,4}$ and $i_{(Pif_s \pm 2f_g)}$ are function of $i_{z,x,2}$ and i_{Pif_s}, respectively. Their analytical expression can be found similarly to $i_{z,x,2}$ and i_{Pif_s}, however they are ignored for simplicity.

It is worth noting that the presence of $i_{z,x,4}$ and $i_{(Pif_s \pm 2f_g)}$ is an additional reason why the arm inductance should be designed above the resonance frequencies of the circulating current dominant components (i.e., $i_{z,x,2}$ and i_{Pif_s}). This is because very high $i_{z,x,2}$ and i_{Pif_s} cause an extra ripple in the system, and these extra ripples cause additional ripples, and so on, which make the system significantly less efficient.

4.5.6 Step 6: Deriving resonance inductance associated with the circulating current dominant ripple components

From equation (4.32) the impedance related to the circulating current second-harmonics $Z_{MMC_{2^{nd}}}$ can be expressed as:

$$\mathrm{Z}_{\mathrm{MMC}_{2^{\mathrm{nd}}}} = 1 - \frac{\mathrm{N}\ \mathrm{M}_{\mathrm{dc}}^{2}}{16\ \mathrm{C}_{\mathrm{SM}}\ \mathrm{L}_{\mathrm{arm}}\ \omega^{2}} - \frac{\mathrm{N}\ \mathrm{M}_{\mathrm{ac}}^{2}}{24\ \mathrm{C}_{\mathrm{SM}}\ \mathrm{L}_{\mathrm{arm}}\ \omega^{2}} \qquad (4.35)$$

From equation (4.35), the analytical expression describing the FBMMC resonance inductance $L_{res_{2F}}$ of the circulating current second-order harmonic related to the grid frequency in buck and boost mode conditions can be obtained as :

$$L_{res_{2F}} = \frac{2NM_{ac}^2 + 3NM_{dc}^2}{48\omega^2 C_{SM}} \tag{4.36}$$

From equation (4.34), the general expression of the MMC phase input impedance Z_{MMC} related to any ripple in the dc-link can be derived as:

$$\begin{aligned} Z_{MMC} = \; & 2\ L_{arm}\, Pi\omega_s \\ & - 2\ L_{arm}\, Pi\omega_s \left(\frac{M_{dc}^2\, N}{4\ C_{SM}\ L_{arm}\, P^2 i{\omega_s}^2} \right. \\ & + \frac{M_{ac}^2\, N}{16\ C_{SM}\, L_{arm}\, P\omega_s\ (Pi\omega_s - \omega)} \\ & \left. + \frac{M_{ac}^2\, N}{16C_{SM}\, L_{arm}\, P\omega_s\ (Pi\omega_s + \omega)} \right) \end{aligned} \tag{4.37}$$

From equation (4.37), the analytical formula defining the resonance inductance $L_{res_{dc}}$ related to any ripple in the dc-link under buck and boost mode conditions can be derived as follows:

$$L_{res_{dc}} = \frac{M_{dc}^2 N}{4\, C_{SM}\, (Pi\omega_s)^2} + \frac{M_{ac}^2 N}{16\, C_{SM} Pn\omega_s\, (Pi\omega_s - \omega)} + \frac{M_{ac}^2 N}{16 C_{SM} Pn\omega_s\, (Pi\omega_s + \omega)} \tag{4.38}$$

Equations from (4.7) to (4.38) give analytical description for all voltage and current quantities of the proposed system under various, non-ideal dc-link voltage levels and the generator frequencies. All electric quantities such as the capacitor current, the capacitor voltage, the SMs' terminal voltage, the total voltage across SMs in each phase and the arm current can be known after solving equation (4.32) and (4.34).

Through (4.32) the second component of the circulating current can be found and thus all electric quantities that are related to the grid side frequency can be known under all possible operations. Through (4.34) the main rectifier current ripple components in the arms are obtained and thus all electric quantities that are related to the generator side frequency can be known as well.

4.6 Arm inductance design discussion

The existing research has demonstrated the effect of boost mode operation on the SM capacitor [84] [106] [107]. The ripple across the SM capacitor is naturally reduced at certain boost mode levels ($i.e., k_m = 2U_m/U_{dc} = 1.411$) . However, in this system the U_{dc} is assumed to varying in a wide range regarding to the wind speed. Therefore, fixing the modulation index at $k_m = 2U_m/U_{dc} = 1.411$ cannot be achieved. As a result, the standard design is followed in this work, in which SM capacitor voltage ripple is limited to 10% i.e., $\Delta U_c \approx 10\%$.

However, the influence of boost mode operating on the design of the arm inductance is not investigated. The main factor in the arm inductance design is to be higher than the resonance inductance [49] [50] [102] [104]. Here, the proposed system is associated with $i_{z,x,2}$ related to the grid frequency and i_{Pf_s} related to generator frequency, thus two resonant inductances are discussed and examine for the parameters shown in Table 4-I.

Table 4-I System parameter design

Active power $\mathrm{P_g}$	4.7MW
Nominal FBMMC phase voltage $\mathrm{U_m}$	3.3kV
Grid frequency,$\mathrm{f_g}$	50Hz
Nominal $\mathrm{dc-link}$ voltage, $\mathrm{U_{dc}}$	6.6kV
Minimum $\mathrm{dc-link}$ voltage, $\mathrm{U_{dc}}$	(6.6kV×0.1) (assumed)
Number of SM per arm, N	4
Generator frequency, $\mathrm{f_s}$	$10-30$ Hz
Arm Inductor, $\mathrm{L_{arm}}$	resounant inductance $\times$ 1.5
SMs' Capacitor, $\mathrm{C_{SM}}$	7mF
Switching frequency, $\mathrm{f_c}$	2000Hz

4.6.1 Resonant Inductance Related to the grid side

Here, for the FBMMC that operates in both buck and boost operation modes, equation (4.36) shows that the resonant inductance value is linked to the modulation indexes ($i.e., M_{ac}$ and M_{dc}) which means that its value varies according to the level of the dc-link voltage. Note, equation (3.24) and Figure 3-8 in the previous chapter show the behaviour of M_{dc} and M_{ac}, and their relation is defined by M_{pk} ($i.e., 2M_{pk} = M_{dc} - M_{ac}$). In the following discussion $M_{pk} = 1$, for simplicity, but also as it assures the maximum utilisation factor. When the FBMMC works in the buck mode ($i.e., M_{ac} = M_{dc} = 1$), the resonance inductance related to the grid frequency in equation (4.36) can be rewritten as:

$$\mathrm{L}_{\mathrm{res}_{2\mathrm{F}}} = \frac{5\mathrm{N}}{48\omega^2\mathrm{C}_{\mathrm{SM}}} \quad (4.39)$$

Here in equation (4.39), $L_{res_{2F}} = L_{res_{2H}}$, see equation (4.4), this is expected as the operation of the FBMMC in the buck mode is similar to the HBMMC. However, when the FBMMC works in the maximum boost mode operation ($i.e.\ M_{ac} = 2\ and\ M_{dc} = 0$), equation (4.36) can be rewritten as:

$$\mathrm{L}_{\mathrm{res}_{2\mathrm{F}}} = \frac{8\mathrm{N}}{48\omega^2\mathrm{C}_{\mathrm{SM}}} \quad (4.40)$$

It is clear from equations (4.39) and (4.40) that the resonance inductance is at its maximum when the FBMMC operates at the maximum boost mode. Here when the FBMMC operates at the minimum dc-link voltage level, the resonance inductance increases by up to 60 % (i.e., 8/5=1.6) from its buck mode value. This means that the arm inductance needs to be designed by considering the lowest dc-link voltage level.

Furthermore, finding the minimum value in the nominator in equation (4.36) determines the minimum value of the resonance inductance. Thus from the nominator in equation (4.36) (i.e., $(2M_{ac}^2 + 3M_{dc}^2 = 0)$), the behaviour of M_{dc}

and M_{ac} under different dc-link voltage (Figure 3-8), and from ($2M_{pk} = M_{dc} - M_{ac}$), the minimum value of the $L_{res_{2F}}$ can be found as below:

$$when\ M_{pk} = 1\ \ the\ minimum\ value\ of\ L_{res_{2F}}\ is\ found$$
$$at\ \ M_{dc} = 0.8,\ \ and\ M_{ac} = 1.2 \tag{4.41}$$

At $M_{dc} = 0.8\ and\ M_{ac} = 1.2$ the resonance inductance is reduced by 4.16% from the resonance inductance buck mode value (equation (4.39)). Using the parameters shown in Table 4-I, the resonance inductance created by the second-order harmonic is evaluated under different voltage level, see Figure 4-3, and Figure 4-4 .

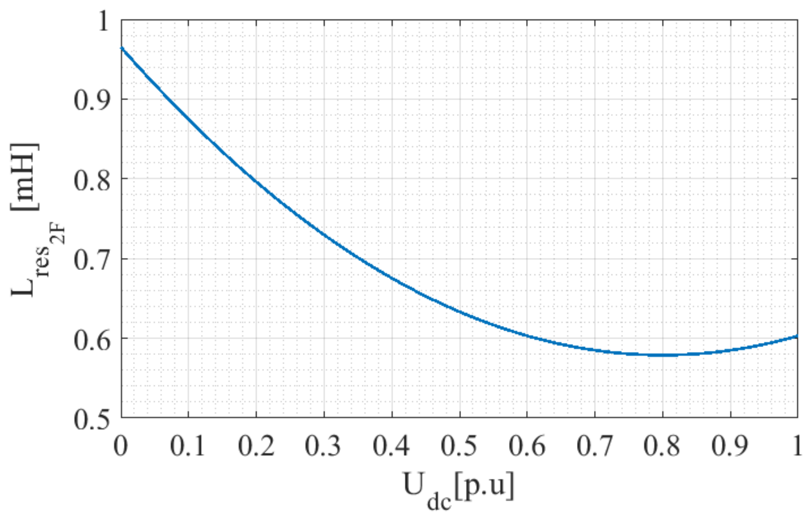


Figure 4-3 The variation of $L_{res_{2F}}$ value under different dc-link voltage level.

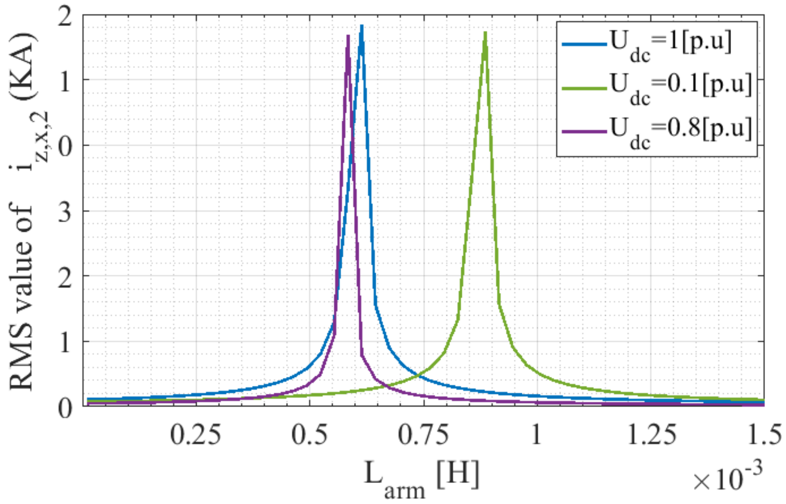


Figure 4-4 The RMS value of the second-order circulating current versus arm inductance for different dc-link voltage levels

Figure 4-3 shows how the value of $L_{res_{2F}}$ varies with dc-link voltage levels. As discus the maximum resonance inductance value is found at the minimum dc-link voltage level. Figure 4-4 depicts the RMS value of the second order circulating current versus arm inductance for various dc-link voltage levels. It emphasises the importance of including boost mode operation when designing the arm inductance in order to keep the RMS value of the second-ordered circulating current within an acceptable range.

4.6.2 Resonant Inductance Related to the generator side

Equation (4.38) shows that the $L_{res_{dc}}$ value varies according to generator frequency and the dc-link voltage level ($i.e., M_{dc}\ and\ M_{ac}$).

For the parameters shown in Table 4-I, Figure 4-5 shows the $L_{res_{dc}}$ value under different generator frequencies, and it states that, the largest $L_{res_{dc}}$ value is found when the generator runs at the lowest frequency. This means that the arm inductance should be designed to be larger than the resonant inductance of the lowest generator frequency. Figure 4-6 shows the behaviour of the $L_{res_{dc}}$ under variant dc-link voltage levels for different generator frequencies. It shows that the resonant inductance value increases with boost mode conditions. This also highlights the importance of considering the boost mode range when designing the arm inductance. Figure 4-7 illustrates the RMS value of $i_{P f_s}$ under different arm inductances and generator frequencies.

In conclusion, the arm inductance should be designed to be larger than the resonant inductance of the lowest frequency coming from the generator side and the lowest dc-link voltage level.

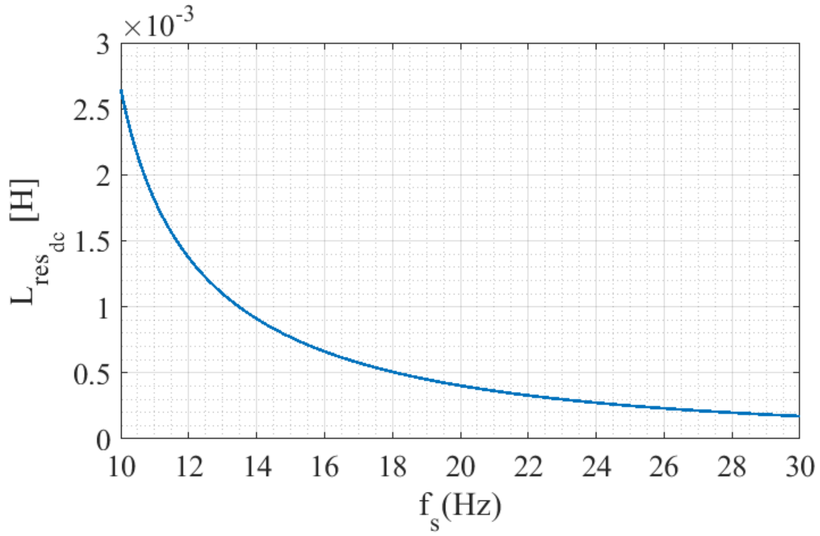


Figure 4-5 $L_{res_{dc}}$ inductance behavior under different generator frequencies

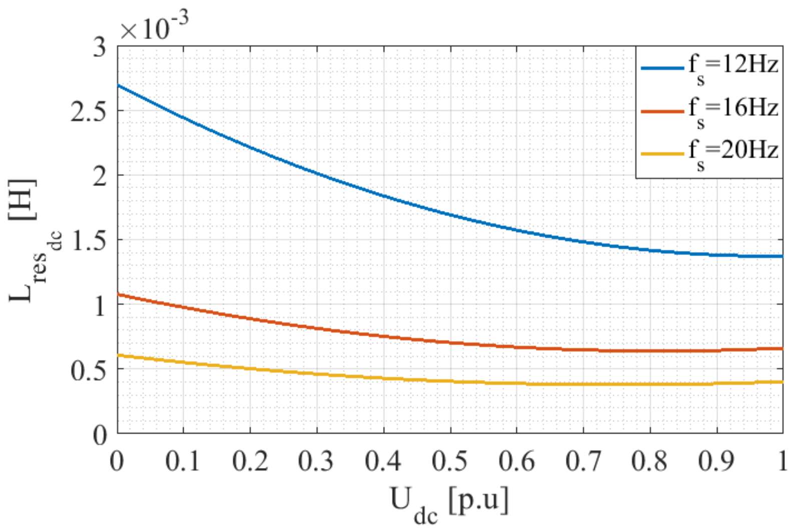


Figure 4-6 $L_{res_{dc}}$ *versus different dc-link voltage levels for different generator frequencies*

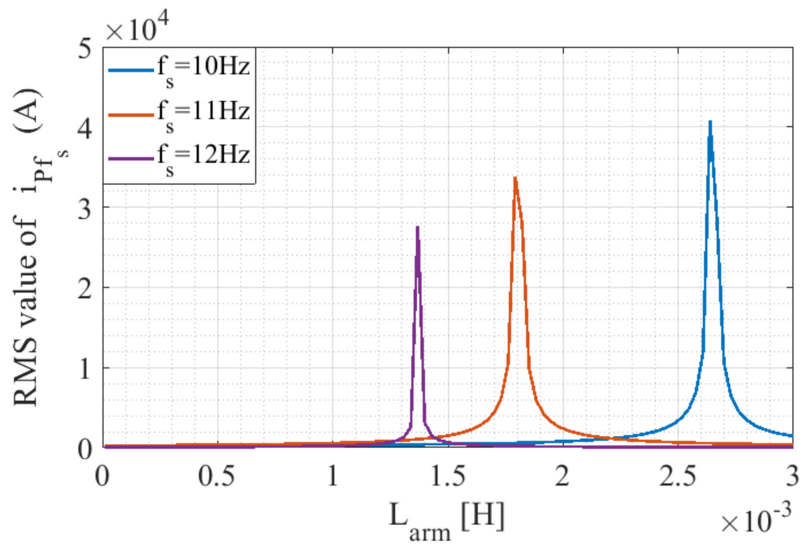


Figure 4-7 The RMS value of i_{P1f_s} *versus different arm inductances and generator frequencies*

To clarify the importance of considering the boost mode and ripple in the dc-link when designing the L_{arm}, Table 4-II shows a comparison between the arm inductance value with ideal and nonideal dc link voltage for parameters' values shown in Table 4-I. Note, the L_{arm} is selected to be 1.5 higher than its resonant inductance, and the minimum dc-link voltage is $0.1U_{dc}$ with minimum generator frequency of 10Hz. Table 4-II states that even with pure dc-link, the L_{arm} needs to be increased almost 43% of its original value when the FBMMC operating in boost mode. With considering the current ripple in the dc-link, the L_{arm} needs to be increased further by almost 4 times of its original value in the buck mode and seven times of its original value in the boost mode. To sum up, for the proposed system the lowest dc-link voltage level and lowest generator frequency determine the safe and optimum design value for the arms inductance.

Table 4-II Arm inductance value comparison

Parameters Table 4-I	Pure dc-link		6-pulse rectifier		12-pulse rectifier	
	Buck mode (Original design)	Boost mode	Buck mode	Boost mode	Buck mode	Boost mode
L_{arm}	0.91mH	1.31mH	4mH	7mH	0.91mH	1.31mH

Furthermore, Table 4-II shows that adding the 12-pulse rectifier to the proposed system has extra benefits. With the 12-pulse rectifier, the dominant ripple at the lowest generator frequency (i.e., 10Hz) is found at $P1f_s = 120Hz$, which is higher than the second order harmonics ripple of the circulating current (i.e., 100Hz with grid frequency $f_g = 50Hz$). As expected, and shown in Table 4-II integrating the system with the 12-pulse rectifier eliminates the effect of the rectifier ripple on the design of the arm inductance, leading to a much lower arm inductance requirement for safe operation. That also means that to eliminate the effect of the 6-pulse rectifier ripple on the design of the arm inductance, the minimum generator frequency must be 17 Hz (i.e.,(17×6)Hz > 100Hz).

4.7 Equivalent circuit of the proposed system

Even though the suggested system is intended for usage in WECSs, the provided analyses and solutions are general and equally applicable to other applications, such as high voltage direct current, motor drive, etc.

Establishing a simplified equivalent circuit will provide a better and easier understanding of the proposed system. The main part of the proposed system is the FBMMC, which can be represented with three separate equivalent circuits.

4.7.1 Equivalent circuit for the integrated ac grid.

Figure 4-8 shows the simplified equivalent circuit demonstrating the integration of the FBMMC into the ac grids. Each phase of the FBMMC is simply represented as characteristic ac voltage sources providing the required fundamental frequency voltage ($u_{o,x,f}$) to the grid and exchange active power and reactive power with the grid when needed.

In addition to the fundamental-frequency voltage, high-frequency harmonics voltage ($u_{o,x,h}$) are also generated by the FBMMC and injected to the grid. The high-frequency harmonics voltage are generated due to the interaction between the fundamental frequency and the carrier frequency and the most dominant high-frequency harmonic outputs found about $2Nf_C$ [51] [83] [88]; where f_C is the carrier frequency. More details on the high-frequency harmonics generated by the MMC will be presented in the next chapter.

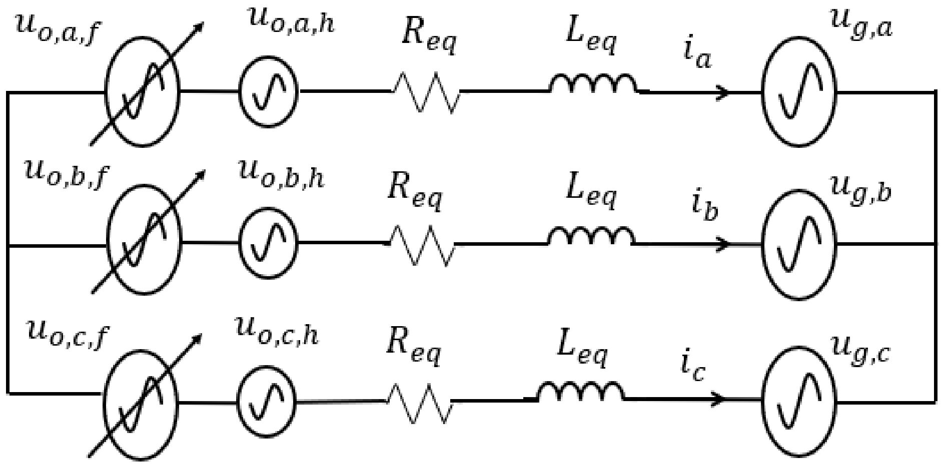


Figure 4-8 Equivalent circuit of the MMC for the integrated ac grid.

4.7.2 FBMMC internal equivalent circuit

The internal equivalent circuit focusing on the ripple components of the FBMMC can be developed as seen in Figure 4-9. It includes only the voltage and current ripple components between the FBMMC phases. Between the FBMMC phases, the second-order harmonic voltage and current are created by the switching processes that are used to create the fundamental components on the grid side. The existence of the second-order harmonics voltage and current in the MMC system is inevitable. Unsuppressed second-order harmonics current generates the fourth order harmonics voltage and current between the FBMMC phases as well.

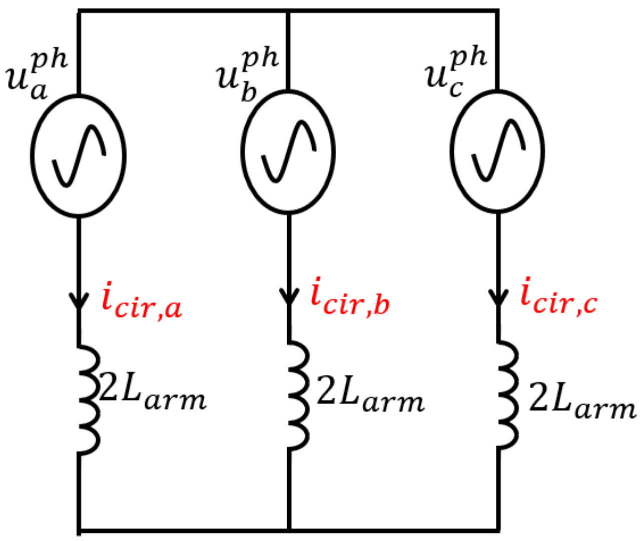


Figure 4-9 Internal equivalent circuit

The absence of the dc-link passive components i.e., LC filter causes a $\mathrm{P}-\mathrm{pulses}$ ripple in the dc-link current $\sum_{i=1}^{\infty} i_{Pif_s}$. The $\sum_{i=1}^{\infty} i_{Pif_s}$ is injected into the FBMMC and becomes part of the FBMMC arm currents. The current components $\sum_{i=1}^{\infty} i_{Pif_s}$ and the switching processes generate the interaction components $\sum_{i=1}^{\infty} i_{(Pif_s \pm 2f_g)}$ between the FBMMC phases as well. Note, $i_{z.x,2}, i_{z.x,4}, and \sum_{i=1}^{\infty} i_{(Pif_s \pm 2f_g)}$ have no effect on the ac side and the dc-side of the FBMMC when the phases of the FBMMC are well balanced. Suppressing $i_{z.x,2}$ will naturally eliminate $i_{z.x,4}$, in the circulating current. Moreover suppressing $\sum_{i=1}^{\infty} i_{Pif_s}$ will naturally eliminate $\sum_{i=1}^{\infty} i_{(Pif_s \pm 2f_g)}$ in the circulating current and suppress the current ripple in the dc-link and generator side.

4.7.3 FBMMC dc-link equivalent circuit

Finally, Figure 4-10 show the equivalent circuit of the FBMMC from the dc-link perspective. The FBMMC can be represented as a single impedance against any ripple in the dc-link, Z_{MMC}. In fact, under circulating current suppression control, the FBMMC will behave like a very large inductance filter, smoothing out the dc-link current ripple and the generator current ripple, as explained in the previous chapter.

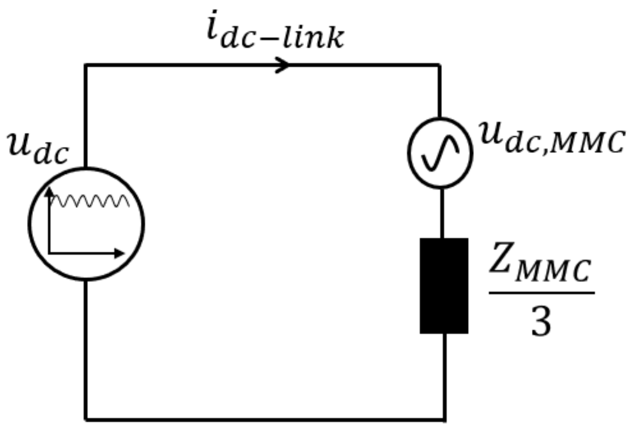


Figure 4-10 FBMMC dc-link equivalent circuit

The $u_{dc,MMC}$ is the switching-ripple voltage across the dc-link caused by the FBMMC [51] [108].The FBMMC switching processes generates high-frequency harmonics voltage in the dc-link. Similar to the ac side of the FBMMC, the most dominant high-frequency harmonics voltage in the dc-link are found at $2Nf_C$ [51] [108]. More details will be presented in the next chapter.

4.7.4 Applying the proposed system for other application

Due to the fact that this proposed system could be used for different applications, it is worth remembering the role of the large LC filter in the dc-link of the conventional PGSC system configuration.

The PGSC configuration connected to the two or three-level inverter needs the large capacitor C_{dc} in the dc-link to smooth out the inverter input voltage and provide good energy buffering capability [3] [7]. Ripple in the input voltage of the two or three level inverter creates low-order harmonics on the ac side affecting the inverter output voltage quality. By contract, The PGSC configuration connected to the FBMMC has no need to the large capacitor in the dc-link as the ac side is totally decoupled from the dc-side voltage ripple, thanks to decoupling capability of the FBMMC [28].

The PGSC configuration connected to the two or three-level inverter firstly needs the inductance L_{dc} in the dc-link to prevent the operation in the discontinues conduction mode (DCM) [7]. However, the L_{dc} value is typically increased significantly (beyond the value needed to avoid DCM) to even smooth out the current in the generator side to achieve almost rectangular generator current shape with THD=31% and PF=0.955 [7]. On the other hand, the PGSC configuration connected to the FBMMC does not require additional dc-side inductance. The experiments in the previous chapter show that the proposed control actively suppressed the ripple in the dc-link current and the generator current.

However, for different applications, from a safe design perspective or due to a restricted input supply or standby generator limitations, the dc-link side may still need a small inductance L_{dc} as an extra layer to only prevent DCM in the dc-link current once the control falls. This is presented in Figure 4-11.

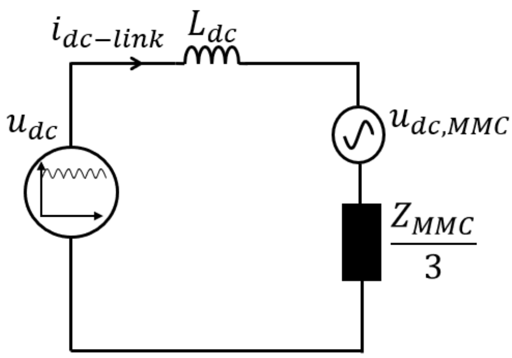


Figure 4-11 FBMMC dc-link equivalent circuit including L_{dc}

The DCM disrupts the diode switching pattern, significantly increases generator current ripple and causes zero power intervals. The DCM occurs when the current ripple becomes more than the dc component of the current in the dc-link. This is strongly dependent on the rated power, level of the dc-link voltage, and Z_{MMC}.

From equation (4.37), the Z_{MMC} value is influenced by mainly two factors: the generator frequency and the level of the dc-link voltage. Figure 4-12 demonstrates the amplitude of the Z_{MMC} versus variant generator frequency and different dc-link voltage levels. The lowest impedance is found at the lowest frequency alongside with the lowest dc-link voltage level.

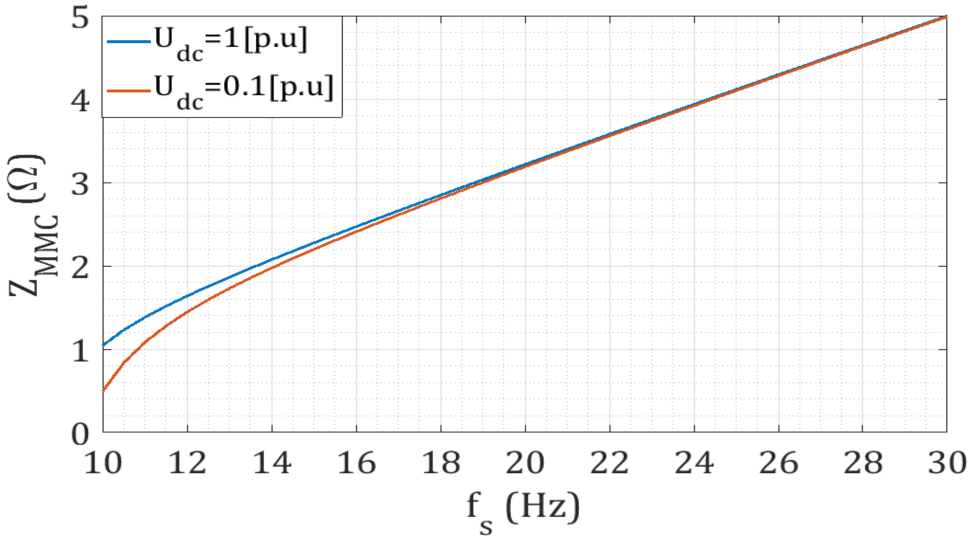


Figure 4-12 Z_{MMC} behaviour under different f_s and dc-link voltage level

Therefore, by considering the Z_{MMC} value in buck and boost modes, the DCM can be avoided by ensuring the dc components of the dc-link current never get equal or smaller than the dc-link current ripple components. Thus, when design the L_{dc} to prevent the DCM condition, the following equation should be fulfilled:

$$\frac{U_{Pf_s}}{Z_{MMC} + P\omega_s L_{DC}} < \frac{rated\ power}{U_{dc}} \tag{4.42}$$

4.8 Analytical model verification

The circular interaction analytical method is well established method, and its accuracy and efficacy are verified by many authors [50] [83] [109] [110]. Here, the proposed analytical will be verified by MATLAB simulation and the experiment prototype.

4.8.1 Simulink Verification

The main parameters of the switching model are presented in Table 3-III with $\mathrm{L_{arm}} = 7\mathrm{mH}$. Here the system is balanced naturally through the PSC-PWM and M_{dc} and M_{ac} are adjusted manually regarding to the level of the dc-link voltage. Two operating conditions are simulated and compared with the established analytical model. The first operation condition (Figure 4-13); the buck mode when the dc-link voltage is at its nominal value, $M_{ac} = 0.9$, $M_{dc} = 1$ and the generator frequency f_s=30 Hz. The second operation condition (Figure 4-14); the boost mode operation when the dc-link voltage is at 80% of its nominal value, $M_{ac} = 1.1$, $M_{dc} = 0.8$, and the generator Frequency f_s= 15 Hz. Moreover, Table 4-III show a detail comparison for the main ripple components in circulating current (i.e., $i_{z.x,2}$ and i_{Pif_s}). Note the time domain comparison only includes the voltage across the SMs capacitor, arm current, and the dc-link current, as these electrical quantities represent other electrical quantities in the system [50] [110].

Figure 4-13, Figure 4-14, and Table 4-III, emphasis that the simulated and calculated results are well agreed and accurate enough to satisfy the design. The analytical model solution provides far more time-efficient process than a simulated solution in terms of more understanding and design optimization.

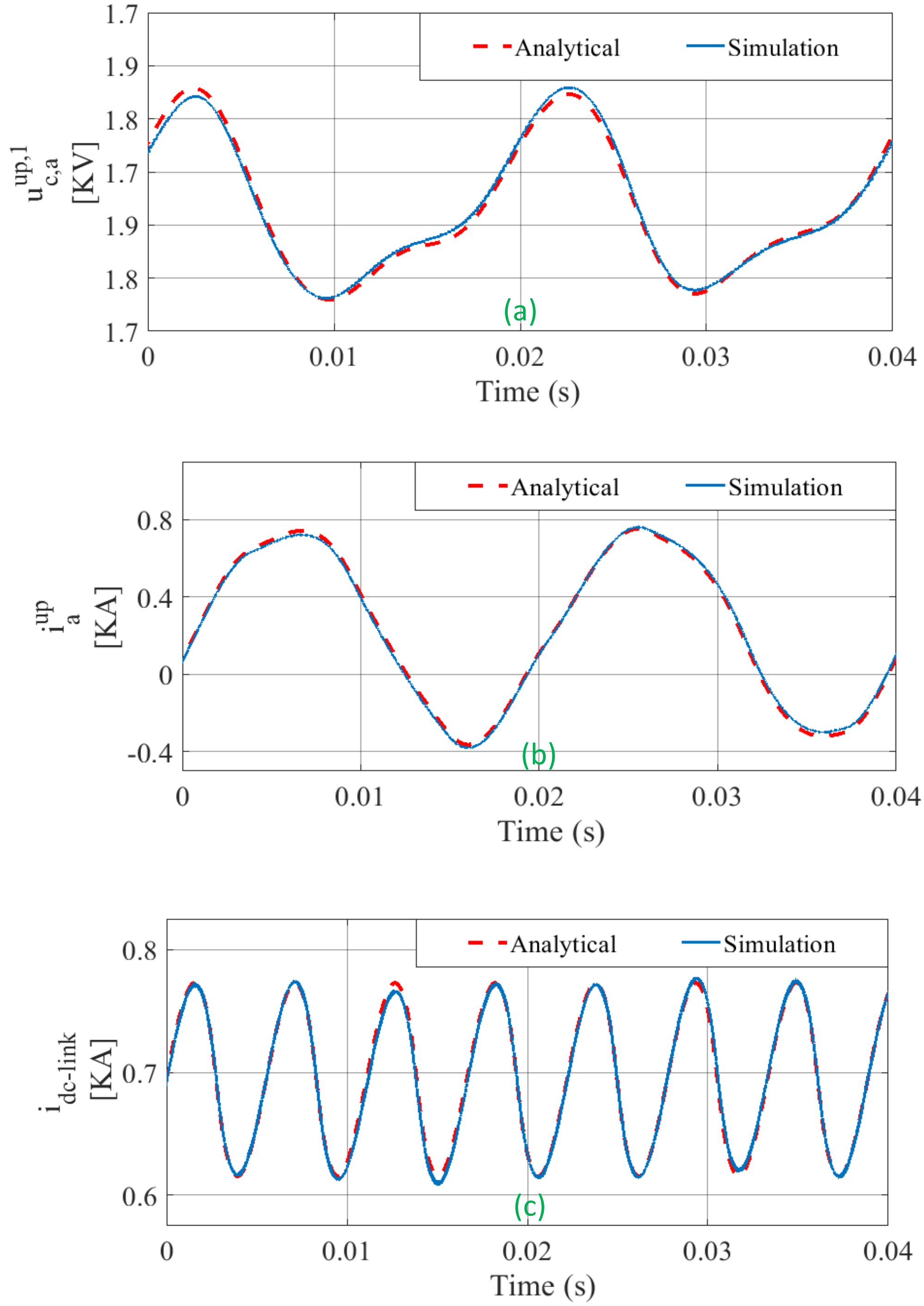


Figure 4-13 Condition (1), buck mode, M_{ac}=0.9 , M_{dc}= 1 and f_s=30Hz, (a) submodules capacitors voltages, (b) arms currents, and (c) dc-link currents

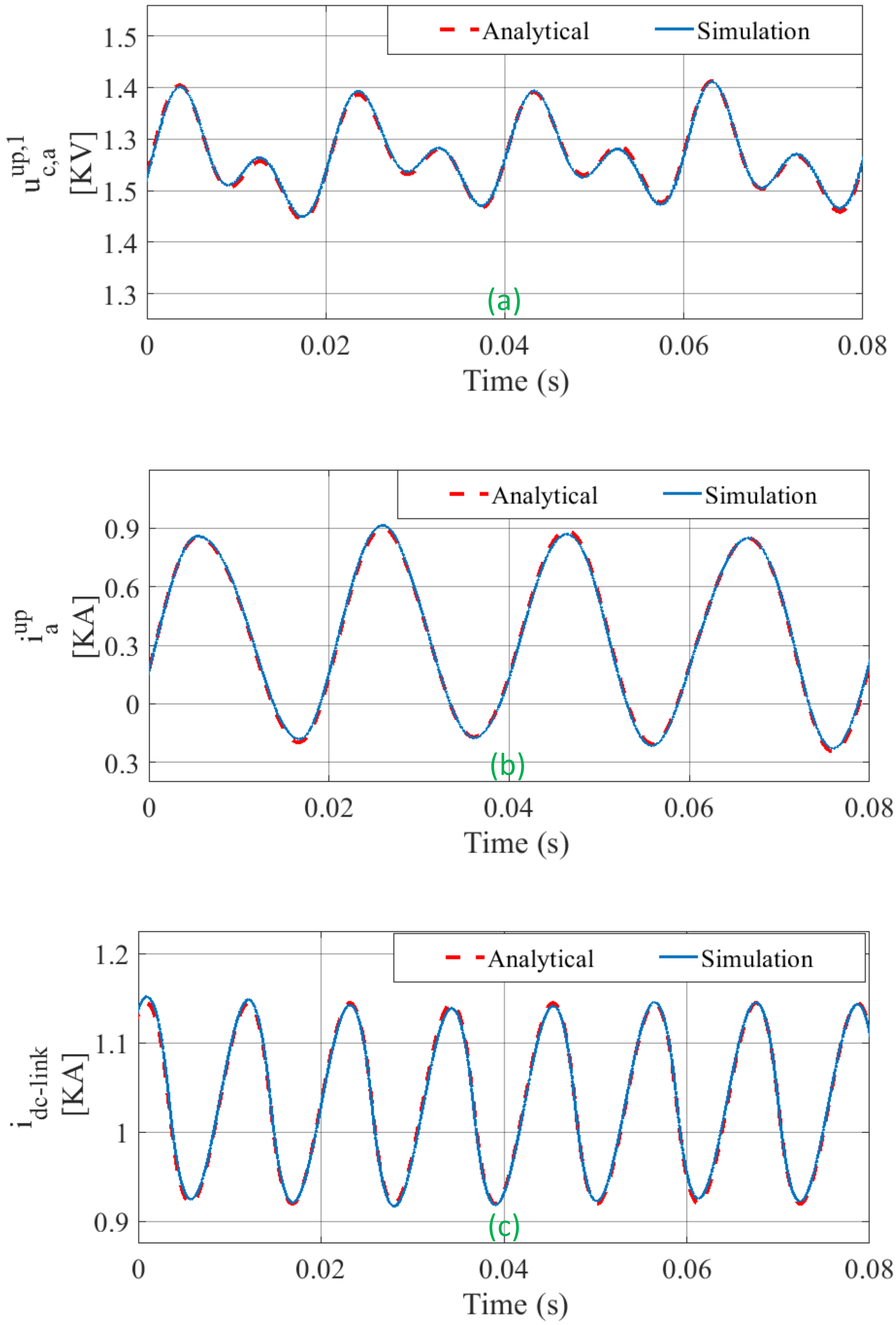


Figure 4-14 Condition (2), boost mode, M_{ac}=0.8 , M_{dc}= 1.1 and f_s=15Hz, (a)submodules capacitors voltages, (b) arms currents, and (c) dc-link currents

Table 4-III Simulation and analytical model comparison

Condition	Electrical quantities	Simulation	Analytical	Error %
(1)	$i_{z,x,2}$	31.42 A	30.57 A	2.78%
	$3i_{Pf_s}$	80.59 A	80.48 A	0.135%
	$3i_{P2f_s}$	9.52 A	9.54 A	0.21%
(2)	$i_{z,x,2}$	17.13 A	16.72 A	2.45%
	$3i_{Pf_s}$	113.02 A	111.95 A	0.94%
	$3i_{P2f_s}$	12.62 A	12.64 A	0.16%

4.8.2 Experiment Verification

Similarly, the modulation signal parameters M_{dc} and M_{ac} are inserted directly to the control and the boost operation is obtained by reduced dc voltage for fixed ac/load voltage. Due to high conduction losses with low voltage system, the arm resistance is added in the analytical modelling, to improve the accuracy i.e., the IGBT voltage drop, and conduction losses which are approximated using the device datasheet. Two operating conditions are experimentally performed and compared with the analytical model. The comparison is achieved by exporting the oscilloscope waveforms to MATLAB which are compared with the results obtained by the analytical model. The experimental parameters are shown in Table 3-V.

Figure 4-15 shows Operating condition 1 when the system is in buck mode with, $U_{dc} = 140V, M_{ac} = 0.9, M_{dc} = 0.9$ and f_s=30 Hz.

Figure 5-16 shows Operating condition 2 when the system is in boost mode with $U_{dc} = 84V, M_{ac} = 1.2, M_{dc} = 0.6$ and f_s=15 Hz.

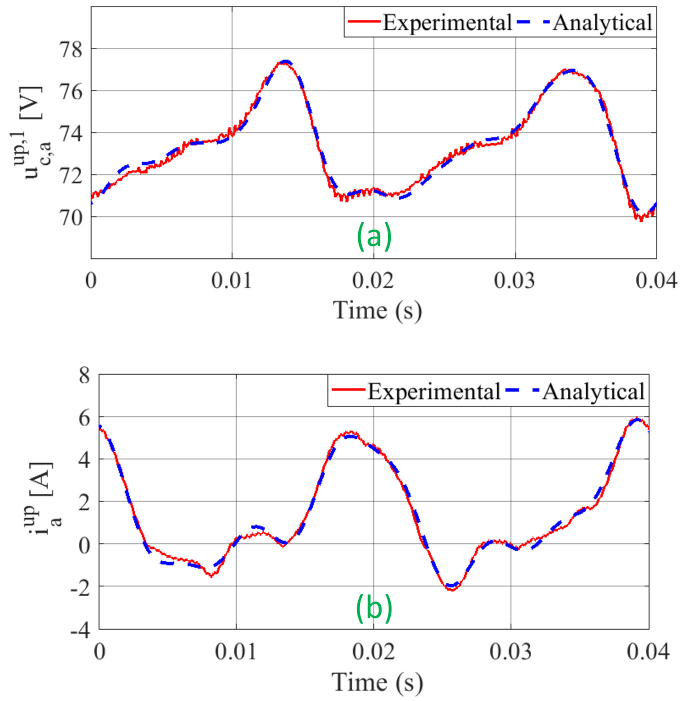


Figure 4-15 Condition (1), buck mode, $M_{ac} = 0.9$, $M_{dc} = 0.9$ and f_s=30Hz, (a)submodules capacitors voltages, (b) arms currents

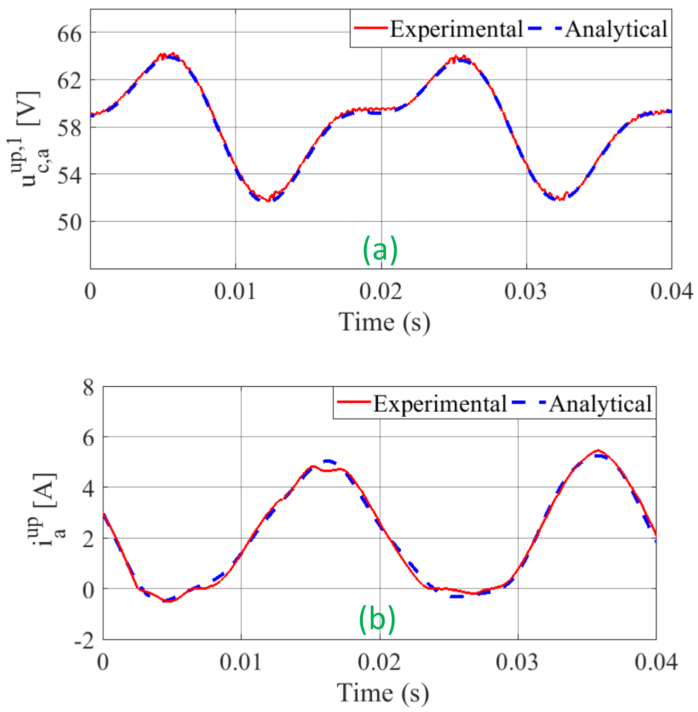


Figure 4-16 Condition (2), boost mode, $M_{ac} = 1.2$, $M_{dc} = 0.6$ and f_s=15Hz, (a)submodules capacitors voltages, (b) arms currents

In order to reduce the number of figures, the dc-current has been omitted from this illustration since it is represented by the arm current. Because the arm current is well-matched, the dc-link current should also be well-matched [50] [110]. Figure 4-15 and Figure 4-16 show the time domain representation of the SM capacitor voltage and arm current under the buck and boost operation conditions (i.e., Operation 1 & Operation 2), respectfully. A good matched with the analytical model is presented, and thus the effectiveness and accuracy of the analytical model is verified.

4.9 Summary

This chapter proposes a new steady-state analytical mode for low-frequency harmonics of the FBMMC including ripple in the dc-link. The proposed analytical model enhances the understanding of the operational capability of FBMMC under variant and non-ideal DC-link voltage and it shows the influence of these on circulating current, sub-modules voltage ripple, and arm inductance design. It has extended applicability as it illustrates the explicit relation between the average switching function and an external ripple caused by the dc-link.

Moreover, it reveals that, the dc-link voltage ripple and boost mode operation influence the design of the arm inductance of the FBMMC. A proper design guidance is provided for the arm inductance in this chapter. The conventional design of L_{arm} considers a pure dc voltage at the dc terminals and the operation in buck mode. The investigation shows that the L_{arm} needs to be increased almost 60% of its original value when the FBMMC operates in maximum boost mode. With considering the current ripple in the dc-link the L_{arm} may needs to be increased furthermore. Therefore, when designing the arm inductance of the MMC, it is crucial to account for boost mode operation and dc-link ripple.

Furthermore, it reveals the actual input impedance of the FBMMC, Z_{MMC}, i.e., the impedance of the MMC seen from the dc-link terminals. The dc-link inductor can be easily designed to avoid a discontinues mode in the dc-link and by that adding an extra layer for safe and proper operation if needed.

This chapter also develops an equivalent circuit for the proposed system in order to facilitate a clearer, simpler, and more comprehensive understanding of the proposed system. Finally, the proposed analytical model is verified by MATLAB simulation and the experiment prototype.

Chapter 5: Analytical Modelling and Optimization of DC Link Voltage Harmonic Spectra Between a Diode Rectifier and Full-Bridge Modular Multilevel Converters

5.1 Abstract

This chapter develops a new analytical solution to the harmonic spectrum of the Full-Bridge Modular Multilevel Converter (FBMMC) dc-side based on phase-shifted carrier pulse width modulation and considering varying dc-link voltage operation. The harmonic distribution of the FBMMC dc-side voltage is analyzed through using double Fourier series analysis. Through the analysis, proper selection of the modulation indexes, carrier displacement angle, and the number of SMs can ensure a significant reduction in the dc-link switching-ripple voltage. Thus, the related filter can be removed or significantly reduced. The harmonic spectrum of FBMMC ac-side is also discussed. Thus, a new carrier displacement angle is presented to achieve good reduction in the harmonic spectrum of FBMMC in both sides. The developed model is validated through simulation tests of a Grid-Tied FBMMC with a front-end three-phase diode rectifier without passive components in the dc-link.

5.2 Introduction

In the MMCs, the switching processes create a switching-ripple in the dc-link. The switching-ripple is generated due to the interaction between the fundamental frequency and the carrier frequency [43] [108]. The switching-ripple in the dc-link voltage influence the rectifier performance, causing conducted and radiated EMI emission, and leading to switching-ripple currents superimposed on the generator current [43] [108]. Authors in [108] have proposed a proper dc filter composed of a series connection of a film capacitor and a damping resistor. However, film capacitor is considered the most prone to failure, as they are sensitive to temperature, humidity, and voltage ripple stresses [42] [43] [44]. Moreover, filters increase the size, cost and losses of the overall system [42] [43] [44]. Therefore, any measures to minimize or even eliminate the dc filter is considerably beneficial.

In this work as the FBMMC is controlled by phase shift carrier PWM, investigating the behaviour of high switching-ripple in the dc side terminals of the inverter is possible by using double Fourier series expansion in two variables [43] [111]. This work's primary objective is to investigate the harmonic spectra of the dc-link voltage of the FBMMC under both boost and buck operation. In addition, the influence of the displacement angle θ_d between the upper and lower arms is investigated. Consequently, the proper selection of the displacement angle and the number of SMs in various operation modes of the FBMMC (i.e., buck and boost mode) can significantly reduce the switching-ripple voltage of the dc-link. Therefore, the dc filter can be eliminated or greatly reduced.

Moreover, the analytical formal harmonic spectrum of the FBMMC phases ac-side is also presented. From that, under either variable or fixed dc-link voltage levels, the optimal displacement angle between the upper and lower arms is discussed. This work also presents a new displacement angle to achieve a significant reduction in switching-ripple on both sides of the FBMMC (i.e., ac and dc sides), under variable dc-link voltage.

Finally, the proposed analytical model is validated using MATALB simulation and a prototype experiment.

5.3 Mechanism of the high switching frequency ripple voltage in the dc-link

The switching processes generate high switching frequency voltage ripple related to the carrier frequency in the upper and lower arms of the FBMMC [43] [108]. These high frequency ripple escapes to the dc-link voltage due to the existence of the generator inductance (L_s) [108].

Figure 5-1 depicts the proposed system's equivalent circuit with a focus on the switching-ripple voltage on the dc link. In Figure 5-1, the total generator inductance is $2L_S$ since two out of the six diodes conduct at any time. The grid side is not taken into consideration. The resistance of the lead wires in the circuit is disregarded, and the high frequency ripple related to the carrier frequency in the dc-terminal voltage of the FBMMC phases are represented as a voltage source ($u_{dc,MMC,x}$).

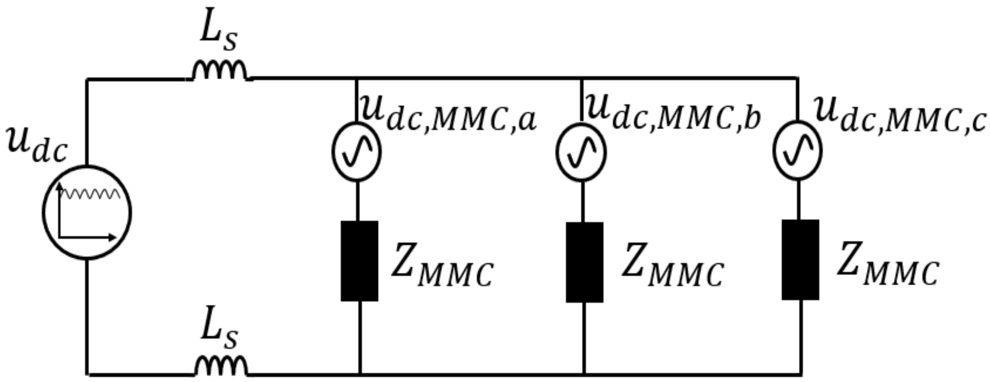


Figure 5-1 Equivalent circuit of the switching-ripple voltage on the DC link

The previous dc-link voltage equation (3.2) needs to be redefined to include high switching frequency voltage ripple as well. Thus, in this chapter, the dc-link voltage u_{dc} can be represented as:

$$\mathrm{u_{dc}} = \mathrm{U_{dc}} + \sum_{\mathrm{i}=1}^{\infty} \mathrm{u_{Pif_s}} + \mathrm{u_{dc,MMC}} \tag{5.1}$$

Where U_{dc} is the dc components, u_{Pif_s} the ripple components generated by the rectifier, and $u_{dc,MMC}$ the high frequency components generated by the FBMMC. From Figure 5-1, the high frequency components in the dc link voltage $u_{dc,MMC}$ can be found by the following expression:

$$\mathrm{u_{dc,MMC}} = \frac{2\mathrm{L_s}}{2\mathrm{L_s} + \frac{\mathrm{Z_{MMC}}}{3}} \times \left(\frac{\mathrm{u_{dc,MMC,a}} + \mathrm{u_{dc,MMC,b}} + \mathrm{u_{dc,MMC,c}} - 3\mathrm{U_C^0 M_{dc} N}}{3} \right) \tag{5.2}$$

Equation (5.2) demonstrates that if L_s does not exist, there will be no high frequency ripple in the dc-link voltage [108]. In equation (5.2) the $u_{dc,MMC,x}$ can be found as:

$$u_x^{up} + u_x^{low} = u_{dc,MMC,x} \tag{5.3}$$

Where the u_x^{up} and u_x^{low} are the output voltage of the upper and lower arm, respectively. Note that the sum of u_x^{up} and u_x^{low} creates dc and low-frequency components, as well as $u_{dc,MMC,x}$. The dc and low-frequency components have been left out because they are not the main focus of this chapter. Equation (5.3) emphasis that the $u_{dc,MMC,x}$ is a result of high switching frequency ripple in the upper and lower arm of the FBMMC [43] [51] [108]. The previous literature in [51], [87], [105] and [88] show that the displacement angle between the upper and lower arm of the MMC has a significant effect on the harmonic spectrum of the ac side of the MMC. They provide an optimised displacement angle to minimise the high-frequency ripple in the ac side voltage of the MMC. Therefore, in this chapter, the influence of the displacement angle between the upper and lower arms of the FBMMC on the harmonic spectrum of the dc-terminal voltage will be examined using the well-known method of double Fourier series analysis. Furthermore, the effect of the FBMMC's different operation modes (i.e., buck and boost modes) on the harmonic spectrum of the dc side will be disclosed. The analysis builds up on the mathematical model and methodology developed in [81] [88].

5.4 Double Fourier series analysis for FBMMC

A double Fourier series expansion is a way of representing a function of two variables as a sum of sines and cosines of frequencies in each variable [43][86].

The coefficients of the terms are found using a Fourier series. The expansion can be used to represent a wide variety of functions, including periodic functions, functions with smooth variations, and functions with sharp discontinuities. The expansion serves as a valuable mathematical tool for understanding the harmonic characteristics of the converter's output waveform [43][86].

By expressing the MMC's output waveform as a sum of harmonics, engineers can study the harmonic content and potential distortion in the generated ac voltage or current. The coefficients in the double Fourier series represent the amplitudes and phases of these harmonics, providing insights into the quality of the converter's output [51][87]. This analysis aids in optimizing the MMC design to minimize harmonic distortion, improve power quality, and ensure efficient operation [51][87].

For the harmonic spectra of the PWM converters, the double Fourier series analysis is well known method [43] [111] . Through the double Fourier series analysis, the investigation of previous existing literature in [51], [87], [105], [88], and [81] is limited to the ac side of the MMC.

However, in this chapter, the primary focus is to analyse and examine the voltage harmonics of the dc-terminal of the FBMMC phases, under different displacement angle between the FBMMC arms, and different operation conditions in buck and boost modes.

The phase of FBMMC has two arms, each arm has a number of SMs. Since the switching process begins with the SMs of the MMC, the analytical examination should begin with the SM of the MMC as well [51] [87] [105]. Focusing on the high harmonics of the system, the fundamental steps of this analytical examination are depicted in Figure 5-2.

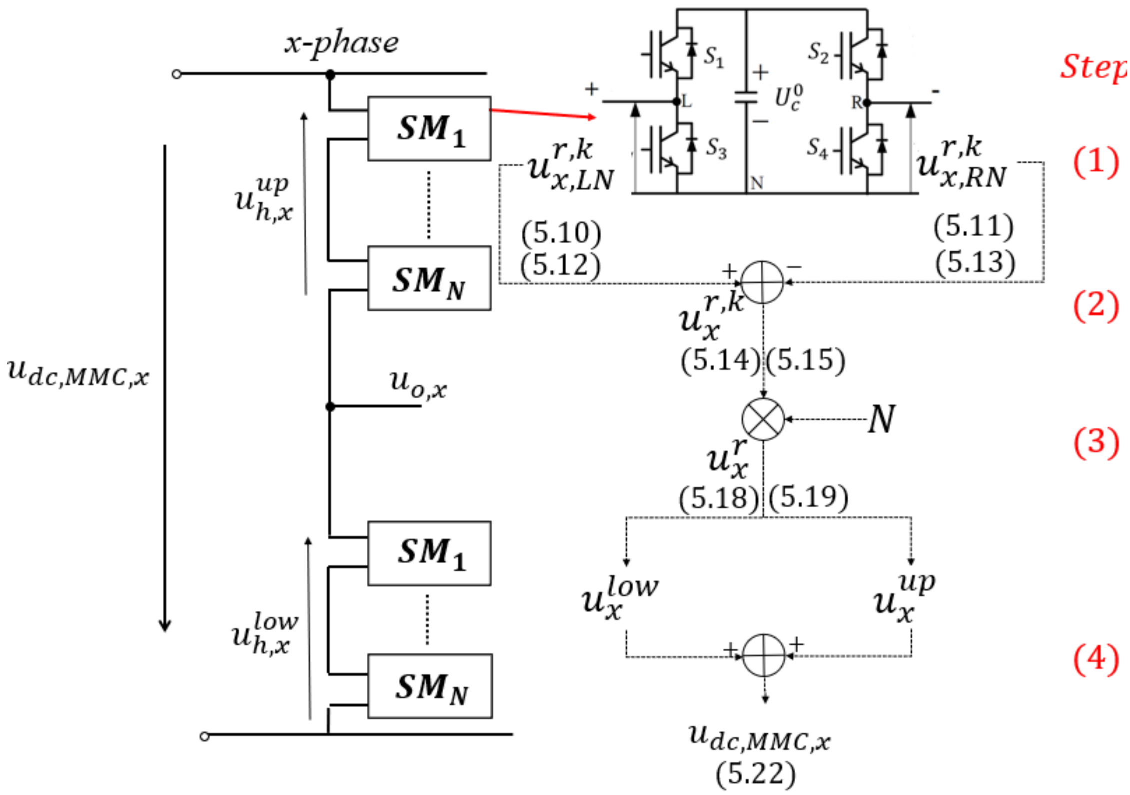


Figure 5-2 Workflow of the double Fourier series analysis of the MMC

In Figure 5-2 the main steps of the analytical model can be summarised as follows:

1) Finding the left-leg SM output voltage harmonics $u_{x,LN}^{r,k}$ and the right-leg SM output voltage harmonics $u_{x,RN}^{r,k}$.

2) Finding the SM output voltage harmonics in the upper and lower arm $u_x^{r,k}$. The SM output voltage can be found as follow:

$$\mathrm{u_x^{r,k} = u_{x,LN}^{r,k} - u_{x,RN}^{r,k}} \quad (5.4)$$

3) Finding the upper arm output voltage harmonics u_x^{up} and lower arm output voltage harmonics u_x^{low}. The arms voltage can be found as follows:

$$\mathrm{u_x^{r}} = \sum_{\mathrm{k=1}}^{\mathrm{N}} \mathrm{u_x^{r,k}} \quad (5.5)$$

4) Finding the dc-terminal voltage harmonics of the FBMMC phases $u_{dc,MMC,X}$, as seen in equation (5.3).

The generalized analysis considers PSC-PWM based on double edge naturally sampled. All capacitor voltages are considered to be inherently balanced under steady-state conditions. The ripple voltage across the SM capacitor is assumed to be zero. This assumption is acceptable as in normal operation the SMs' capacitor is usually designed large enough to limit the voltage ripple not more than 10% of the rated capacitor voltage [87] [105].

5.4.1 Step (1) the left and right SM output voltage harmonics

For a carrier-based PWM waveform, the double Fourier series general form of expansion in two variables of the harmonic spectrum is given by [87] [105]:

$$f(t) = \frac{C_{00}}{2} + \mathrm{Re}\sum_{n=1}^{\infty} C_{0,n} e^{-j(mz+ny)}$$
$$+ \mathrm{Re}\sum_{m=1}^{\infty}\sum_{n=1}^{\infty} C_{m,n} e^{-j(mz+ny)} dzdy, \tag{5.6}$$

where the coefficients can be described as [87] [105]:

$$C_{m,n} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} f(z,y) e^{-j(mz+ny)} dzdy \tag{5.7}$$

Here, Re indicates the real part of the complex number, m and n are denoted to the multiples of the carrier and fundamental frequency, respectively. The z and y variable are described as follows:

$$y = \omega t + \theta_x$$
$$z = \omega_c t + \theta_c^{r,k} \tag{5.8}$$

Where ω_c is the carrier angular frequency. Thus, with no ripple and identical U_c^o across the SMs capacitor, and from the modulation signals in equation (3.26), the coefficients of the left-leg and right-leg SM voltage harmonics can be represented as[88] :

$$C_{m,n}^{LL} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi\left(M_{x,LL}^{r,k}\right)}^{\pi\left(M_{x,LL}^{r,k}\right)} U_C^0 \, e^{-j(mz+ny)} dzdy \tag{5.9}$$

$$C_{m,n}^{RL} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi(M_{x,RL}^{r,k})}^{\pi(M_{x,RL}^{r,k})} U_C^0\, e^{-j(mz+ny)}dzdy$$

Thus, from equation (5.6) and by solving equation (5.9), the left-leg and right-leg SM output voltage analytical harmonic spectrum in the lower arm can be found as[88] :

$$u_{x,LN}^{low,k} = \frac{2U_c^o + U_c^o M_{dc}}{4} + \frac{U_c^o M_{ac}}{4}\cos(y) + \mathrm{Re}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} e^{-j(mz+ny)}$$

$$\times \left[\frac{2U_c^o}{m\pi} J_n\left(mM_{ac}\frac{\pi}{4}\right)\sin\left(\frac{\left(m\pi\left(1+\frac{M_{dc}}{2}\right)+n\right)}{2}\right)\right] \qquad (5.10)$$

$$u_{x,RN}^{low,k} = \frac{2U_c^o - U_c^o M_{dc}}{4} - \frac{U_c^o M_{ac}}{4}\cos(y) + \mathrm{Re}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} e^{-j(mz+ny)}$$

$$\times \left[\frac{2U_c^o}{m\pi} J_n\left(mM_{ac}\frac{\pi}{4}\right)\sin\left(\frac{\left(m\pi\left(1+\frac{M_{dc}}{2}\right)+n\right)}{2}\right)\right] \qquad (5.11)$$

In equations (5.10) and (5.11), J_n is the first kind - Bessel functions of order n and argument $\left(mM_{ac}\frac{\pi}{4}\right)$ [111] [51]. Similarly, the left-leg and right-leg SM output voltage analytical harmonic spectrum in the upper arm can be found as [88]:

$$u_{x,LN}^{up,k} = \frac{2U_c^o - U_c^o M_{dc}}{4} - \frac{U_c^o M_{ac}}{4}\cos(y) + \mathrm{Re}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} e^{-j(mz+ny)} \times \left[\frac{2U_c^o}{m\pi} J_n\left(mM_{ac}\frac{\pi}{4}\right)\sin\left(\frac{\left(m\pi\left(1+\frac{M_{dc}}{2}\right)+n\right)}{2}\right)\right] \tag{5.12}$$

$$u_{x,RN}^{up,k} = \frac{2U_c^o + U_c^o M_{dc}}{4} + \frac{U_c^o M_{ac}}{4}\cos(y) + \mathrm{Re}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} e^{-j(mz+ny)} \times \left[\frac{2U_c^o}{m\pi} J_n\left(mM_{ac}\frac{\pi}{4}\right)\sin\left(\frac{\left(m\pi\left(1+\frac{M_{dc}}{2}\right)+n\right)}{2}\right)\right] \tag{5.13}$$

5.4.2 Step (2) the SM output voltage harmonics $u_x^{r,k}$

From equation (5.4), the SM output voltage in the lower arm $u_x^{low,k}$ can be found using equations (5.10) and (5.11) as below[88] :

$$u_x^{low,k} = \frac{U_c^o M_{dc}}{2} + \frac{U_c^o M_{ac}}{2}\cos(\omega t + \theta_x) + \mathrm{Re}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} e^{-j(2m(\omega_c t + \theta_c^{low,k}) + n(\omega t + \theta_x))} \times \left[\frac{2U_c^o}{m\pi} J_n\left(\frac{\pi m M_{ac}}{2}\right)\cos(m\pi)\sin\left((mM_{dc}+n)\frac{\pi}{2}\right)\right] \tag{5.14}$$

Similarly, from equation (5.4), the SM output voltage in the upper arm $u_x^{up,k}$ can be found using equations (5.12) and (5.13) as below [88] :

$$
\begin{aligned}
u_x^{up,k} &= \frac{U_c^o M_{dc}}{2} - \frac{U_c^o M_{ac}}{2}\cos(\omega t + \theta_x) \\
&\quad + \mathrm{Re}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} e^{-j(2m(\omega_c t + \theta_c^{up,k}) + n(\omega t + \theta_x + \pi))} \\
&\quad \times \left[\frac{2U_c^o}{m\pi} J_n\left(\frac{\pi m M_{ac}}{2}\right)\cos(m\pi)\sin\left((mM_{dc} + n)\frac{\pi}{2}\right)\right]
\end{aligned} \tag{5.15}
$$

5.4.3 Step (3) the arms output voltage harmonics u_x^r

From equation (5.5) with equations (3.27) and (3.28), the lower arm output voltage is found as[88]:

$$
\begin{aligned}
u_x^{low} &= \frac{NU_c^o M_{dc} + NU_c^o M_{ac}}{2}\cos(\omega t + \theta_x) \\
&\quad + \mathrm{Re}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\Big(\sum_{k=1}^{N} e^{-j(2m(\omega_c t + \frac{\pi}{N}(K-1)) + n(\omega t + \theta_x))} \\
&\quad \times \left[\frac{2U_c^o}{m\pi} J_n\left(\frac{\pi m M_{ac}}{2}\right)\cos(m\pi)\sin\left((mM_{dc} + n)\frac{\pi}{2}\right)\right]
\end{aligned} \tag{5.16}
$$

Since

$$
\begin{aligned}
&\sum_{k=1}^{N} e^{-j(2m(\omega_c t + \frac{\pi}{N}(K-1)) + n(\omega t + \theta_x))} \\
&= \begin{cases} 0 & \text{for } m \neq KN, K = 1, 2, 3 \ldots, \\ Ne^{-j(2m(\omega_c t) + n(\omega t + \theta_x))} & \text{for } m = KN, K = 1, 2, 3 \ldots, \end{cases}
\end{aligned} \tag{5.17}
$$

Therefore, using equation (5.17), m is replaced by Nm for simplicity [88]. Thus, the lower arm output voltage harmonics equation in (5.16) can be simplified as[88]:

$$u_x^{low} = \frac{NU_c^o M_{dc} + NU_c^o M_{ac}}{2}\cos(\omega t + \theta_x)$$

$$+\mathrm{Re}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} e^{-j\left(2mN\omega_c t + n(\omega t + \theta_x)\right)} \tag{5.18}$$

$$\times\left[\frac{2U_c^o}{m\pi}J_n\left(\frac{\pi N m M_{ac}}{2}\right)\cos(Nm\pi)\sin\left((NmM_{dc} + n)\frac{\pi}{2}\right)\right]$$

In the same way, the upper arm output voltage harmonics are found as

$$u_x^{up} = \frac{NU_c^o M_{dc} - NU_c^o M_{ac}}{2}\cos(\omega t + \theta_x)$$

$$+\mathrm{Re}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} e^{-j\left(2mN(\omega_c t + \theta_d) + n(\omega t + \theta_x + \pi)\right)} \tag{5.19}$$

$$\times\left[\frac{2U_c^o}{m\pi}J_n\left(\frac{\pi N m M_{ac}}{2}\right)\cos(Nm\pi)\sin\left((NmM_{dc} + n)\frac{\pi}{2}\right)\right]$$

5.4.4 Step (4) the dc-terminal voltage harmonics of the FBMMC phases $\boldsymbol{u_{dc,MMC,x}}$

From equation (5.3) and using equation (5.18) and (5.19), the dc-terminal voltage harmonics of the FBMMC u_{dc-MMC} can be found as:

$$u_{dc,MMC,x} = NU_c^o M_{dc} + \mathrm{Re} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} e^{-j\left(2mN\omega_c t + n(\omega t + \theta_x)\right)}$$
$$\times \left[1 + e^{-j((2mN\theta_d + n\pi)}\right] \tag{5.20}$$
$$\times \left[\frac{2U_c^o}{m\pi} J_n\left(\frac{\pi m M_{ac}}{2}\right) \cos(m\pi) \sin\left((mM_{dc} + n)\frac{\pi}{2}\right)\right]$$

Through using the expressions below:

$$e^{-jx} = \cos x - j\sin x$$
$$\text{and} \tag{5.21}$$
$$\cos A + \cos B = 2\cos\left(\frac{A+B)}{2}\right) \times \cos\left(\frac{A-B)}{2}\right)$$

Equation (5.20) can be simplified as :

$$u_{dc,MMC,x} = U_C^O M_{dc} N$$
$$+\mathrm{Re} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \cos\left(2mN\omega_c t + n(\omega t + \theta_x) + \frac{2mN\theta_d + n\pi}{2}\right)$$
$$\times \left[\frac{2U_c^o}{m\pi} J_n\left(mNM_{ac}\frac{\pi}{2}\right) \cos(mN\pi)\right] \tag{5.22}$$
$$\times \sin\left((mNM_{dc} + n)\frac{\pi}{2}\right) \cos\left(\frac{2mN\theta_d + n\pi}{2}\right)$$

5.5 The FBMMC dc-terminal voltage harmonics analysis and minimization

The dc-link voltage with less high-frequency voltage ripple leads to smaller size , lower price and longer lifespan of the required dc side filter [43] [44]. Therefore, it is desirable to reduce dc-terminal harmonics voltage of the FBMMC, particularly in the first high-frequency carrier group (m = 1), which primarily specifies the dc-side filter need [43] [44] [108].

As seen in equation (5.22), the dc-terminal harmonics voltage of the FBMMC are function of the modulation parameter M_{dc}, M_{ac} and number of the SMs N. From equation (5.22), the order {m, n} of the zero and nonzero harmonics is a function of M_{dc}, N and θ_d and it is defined by the product of the following terms:

$$\{\mathrm{m,n}\} \rightarrow \cos\left(\frac{2\mathrm{mN}\theta_{\mathrm{d}} + \mathrm{n}\pi}{2}\right) \times \sin\left((\mathrm{mNM_{dc}} + \mathrm{n})\frac{\pi}{2}\right) \qquad (5.23)$$

The analysis will be carried out in two conditions. First condition when the product of NM_{dc} is an integer and the second condition when the product of NM_{dc} is a fraction. For completeness, the analysis includes all high-frequency carrier groups, when m is odd (i.e., $m_{odd} = 1, 3, 5 \ldots$), or m is even (i.e., $m_{even} = 2, 4, 6 \ldots$). Note, due you to the periodic, eliminated or minimized high-frequency carrier groups at m=1, will eliminate all odd group.

5.5.1 Complete Harmonic Elimination, when $\mathbf{NM_{dc}}$ **is an integer**

5.5.1.1 when m is odd

As stated, odd groups of m defines the filter requirement (i.e., m=1). When m is odd, the term in equation (5.23), can be rewritten as $\cos\left(\frac{2N\theta_d+n\pi}{2}\right)\sin\left((NM_{dc}+n)\frac{\pi}{2}\right)$. Here for $\sin\left((NM_{dc}+n)\frac{\pi}{2}\right)$ nonzero condition is occurred when $NM_{dc} = \text{even (or odd)},\ \text{and}\ n = \text{odd(or even)}$, and thus these harmonics can be eliminated by making the other term $\left(\cos\left(\frac{2N\theta_d+n\pi}{2}\right)\right)$ zero, through manipulating the value of θ_d. For $n = \text{odd}$ the displacement angle is selected as $\theta_d = H_2\pi/2N$ where $(H_2 = 0,\ \pm2,\ \pm4 \dots)$, and for $n = \text{even}$ the displacement angle is selected as $\theta_d = H_1\pi/2N$ where ($H_1 = \pm1,\ \pm3,\ \pm5 \dots$). This can be simplified as :

$$
\begin{gathered}
u_{dc,MMC,x} = 0 \text{ at } m = 1 \text{ (i.e., } m = \text{odd), for} \\
\theta_d = \frac{\pi}{2N}, \text{at } NM_{dc} \text{ is odd,} \\
\text{or} \\
\theta_d = 0, \text{at } NM_{dc} \text{ is even}
\end{gathered}
\tag{5.24}
$$

5.5.1.2 when m is even

When m is even, the term in equation (5.23), can be rewritten as $\cos\left(\frac{(2\times 2\mathrm{N}\theta_{\mathrm{d}})+\mathrm{n}\pi}{2}\right)\sin\left((2\mathrm{NM}_{\mathrm{dc}}+\mathrm{n})\frac{\pi}{2}\right)$.

Here for the term of $\sin\left((2\mathrm{NM}_{\mathrm{dc}}+\mathrm{n})\frac{\pi}{2}\right)$, the nonzero condition is occurred when $2\mathrm{NM}_{\mathrm{dc}}=\text{even},\ \text{and}\ \mathrm{n}=\text{odd}$. The term of $\cos\left(\frac{(2\times 2\mathrm{N}\theta_{\mathrm{d}})+\mathrm{n}\pi}{2}\right)$ is always zero when θ_{d} defined as stated in equation (5.24) i.e., at $\theta_{\mathrm{d}}=\frac{\pi}{2\mathrm{N}}$ or $\theta_{\mathrm{d}}=0$.

Therefore, when the product of $\mathrm{NM}_{\mathrm{dc}}$ is integer and through appropriate selection of $\mathrm{N}, \mathrm{M}_{\mathrm{dc}}, \text{and}\ \theta_{\mathrm{d}}$, the dc-link side high-frequency switching harmonics are almost eliminated. Thus, the dc-link filter is either not needed anymore or reduced significantly. In this condition the dc-link voltage should be free from the high frequency ripple at the optimum displacement angle. This will be verified in the next sections.

5.5.2 Harmonic minimization, when $\mathbf{NM_{dc}}$ is a fraction

In a system where the dc-link voltage level is changing during a normal operation, the product of $\mathrm{NM}_{\mathrm{dc}}$ is not expected to be an integer i.e., neither odd nor even, but a fraction. Thus, the term of $\sin\left((\mathrm{mNM}_{\mathrm{dc}}+\mathrm{n})\frac{\pi}{2}\right)$ is nonzero for all n (i.e., $\mathrm{n}=0,\pm 1,\pm 2,\ldots$) at all m groups. Therefore, focusing on the first group of the carrier (i.e., at $\mathrm{m}=1$), the term of $\cos\left(\frac{2\mathrm{N}\theta_{\mathrm{d}}+\mathrm{n}\pi}{2}\right)$ is used to eliminate the higher harmonics amplitude at $n = odd$ or $n = even$ via appropriate selection of θ_d, as demonstrated in Figure 5-3.

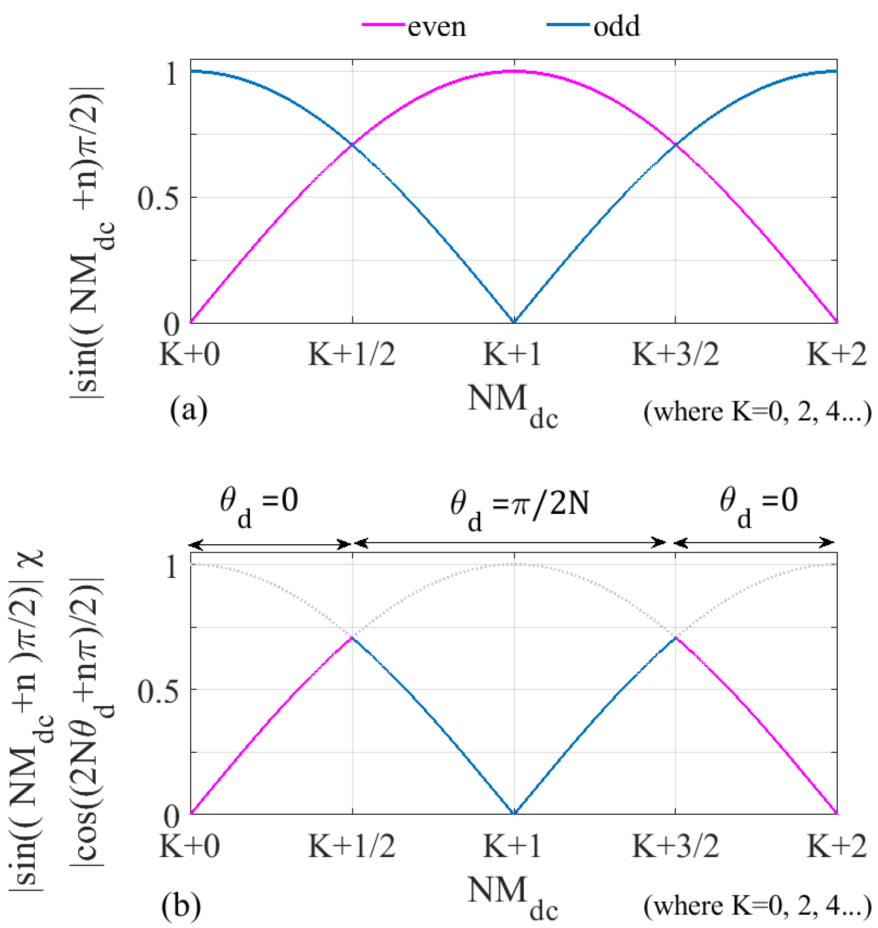


Figure 5-3 (a)Variation of $even$ and odd harmonics in dc-terminal voltage , and (b) Selection of optimal θ_d for the dc-terminal voltage of the FBMMC

In Figure 5-3 (a), the term of $\sin\left((mNM_{dc} + n)\frac{\pi}{2}\right)$ is shown with $n = odd$ and $n = even$ and Figure 5-3 (b) reveals that θ_d has a considerable impact on the elimination of the higher harmonic amplitude for $n = odd$ or $n = even$ in the complete term $|\sin\left((mNM_{dc} + n)\frac{\pi}{2}\right)| \times |\cos\left(\frac{2mN\theta_d + n\pi}{2}\right)|$. For instance, in

Figure 5-3 (b), in the range between $\mathrm{K}+2$ and $\mathrm{K}+\frac{3}{2}$, the harmonics at $\mathrm{n}=\mathrm{odd}$ has the largest amplitude, then the displacement angle in the term $|\cos\left(\frac{2\mathrm{mN}\theta_{\mathrm{d}}+\mathrm{n}\pi}{2}\right)|$ is selected as $\theta_{\mathrm{d}}=0$ to achieve the best harmonic minimization. Moreover, in the range between $\mathrm{K}+\frac{3}{2}$ and $\mathrm{K}+\frac{1}{2}$, the harmonics at $\mathrm{n}=\mathrm{even}$ has the largest amplitude, then the displacement angle in the term $|\cos\left(\frac{2\mathrm{mN}\theta_{\mathrm{d}}+\mathrm{n}\pi}{2}\right)|$ is selected as $\theta_{\mathrm{d}}=\frac{\pi}{2\mathrm{N}}$ to achieve the best harmonic minimization. Thus, for best harmonics elimination under the product of $\mathrm{NM}_{\mathrm{dc}}=$ fraction can be simplified as the following:

$$u_{dc,MMC,x} = minimum\ at\ m = 1\ (i.e., m = odd), for$$

$$\theta_d = \frac{\pi}{2N}, when\ \{nearest\ integer\ of\ the\ product\ NM_{dc}\ is\ odd\}$$

$$or \tag{5.25}$$

$$\theta_d = 0, when\ \{nearest\ integer\ of\ the\ product\ NM_{dc}\ is\ even\}$$

5.5.3 Optimal displacement angle for the dc-terminal voltage of the FBMMC

It is now understood from Figure 5-3 that when the product of $\mathrm{NM}_{\mathrm{dc}}$ is an integer (i.e., at $\mathrm{K}+2, \mathrm{K}+1,$ and $\mathrm{K}+0$), only the $\mathrm{n}=\mathrm{odd}$ or the $\mathrm{n}=\mathrm{even}$ exists. Then the term of $\cos\left(\frac{2mN\theta_d+n\pi}{2}\right)$ is used to achieve complete harmonics elimination via appropriate selection of θ_d . On the other hand, when the product of NM_{dc} is a fraction (i.e., $\text{between } K+2 \text{ and } K+1, \text{and between } K+1 \text{ and } K+0$), the term of $\cos\left(\frac{2mN\theta_d+n\pi}{2}\right)$ is used to eliminate the higher harmonics amplitude at $n = \text{odd}$ or $n = \text{even}$ through appropriate selection of θ_d. For the sake of completeness, and to verify the efficacy of (5.24) and (5.25), Figure 5-4 shows the variation of the rms amplitude of the harmonics $u_{dc,MMC,x}^{\{1,n\}}$ at $m = 1$, for the different number of SM N and full range of M_{dc} at the mentioned displacement angle values $\theta_d = 0$ and $\theta_d = \pi/2N$. Where the rms value is calculated as:

$$u_{dc,MMC,x}^{\{1,n\}} = \sqrt{\sum_{n=-20}^{n=20}\left(\frac{2U_c^o}{m\pi}J_n\left(mNM_{ac}\frac{\pi}{2}\right)\cos(mN\pi)\sin\left((mNM_{dc}+n)\frac{\pi}{2}\right)\cos\left(\frac{2mN\theta_d+n\pi}{2}\right)\right)^2} \tag{5.26}$$

Theoretically, n is denoted $-\infty \leq n \leq \infty$, however the nature of the Bessel function makes the selection of the harmonic order (i.e., $-20 \leq n \leq 20$) sufficient [109]. The M_{dc} and M_{ac} are defined as equation (3.24) and $M_{pk} = 1$ for simplicity. Finally, it should be emphasized that a varying dc-link side with a fixed ac side of MMC is assumed in this work.

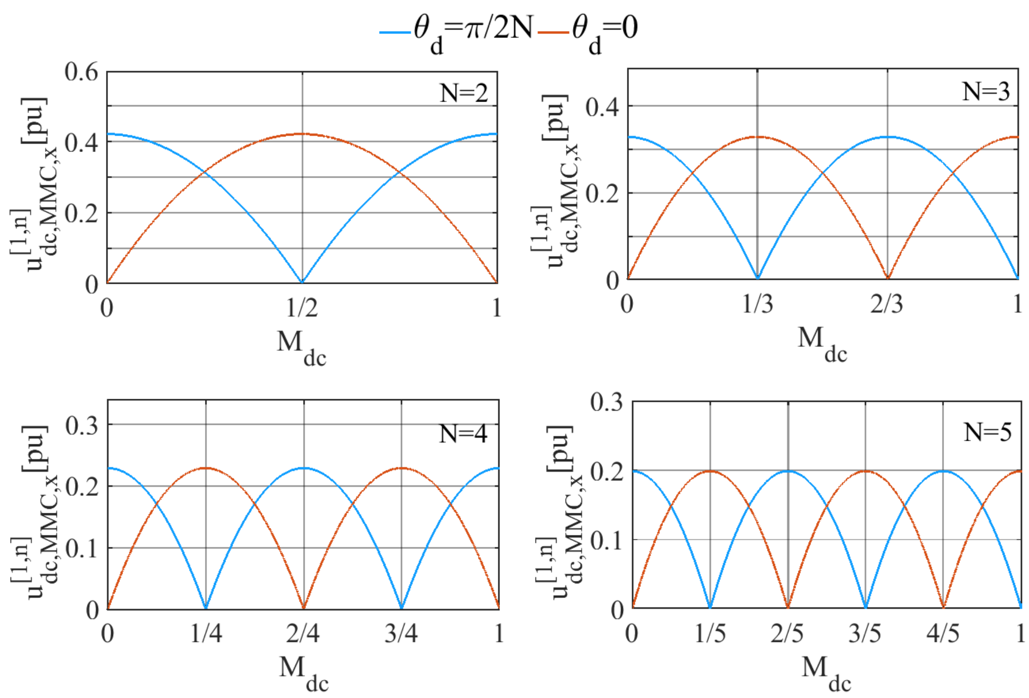


Figure 5-4 variation of $u_{dc,MMC,x}^{\{1,n\}}$rms value under different N, M_{dc} and θ_d

Figure 5-4 validates that, at $m = 1$, and when the product of $NM_{dc} = integer$, a complete harmonic elimination can be achieved by a proper selection of θ_d. However, when the product of $NM_{dc} = fraction$, θ_d can be used to achieve significant harmonic minimization. Therefore, from Figure 5-3 and Figure 5-4, and by combining equations (5.24) and (5.25), the optimal θ_d can be given as:

$$\mathrm{u_{dc,MMC,x}} = \text{minimum at } \mathrm{m} = 1 \text{ (i.e., m = odd), for}$$

$$\theta_d = \frac{\pi}{2N}, \text{at } \{\text{round } (\mathrm{NM_{dc}}) \text{is odd}\}$$

$$\text{or} \tag{5.27}$$

$$\theta_d = 0, \text{at } \{round\ (\mathrm{NM_{dc}})\ \text{ is even}\}$$

here, the function $round(\,)$ is round to nearest integer. However, in this proposed system as the dc link voltage is varying regarding to the wind speed, complete harmonic elimination cannot be achieved. The lowest harmonics group in the dc-terminal of the FBMMC is still found at $2Nf_c$. Nevertheless, as the harmonics amplitude of the dominant group (i.e., at $m = 1$) can be reduced by θ_d, the required filter size can be reduced as well [108].

5.6 Verification of the analytical harmonic spectra

5.6.1 Simulink Verification

Simulations are executed in MATLAB/Simulink to test the analytical model and investigate the harmonic spectra for a variety of possible design configurations. The simulation main parameters are shown in Table 5-I. Note the L_s is added in Table 5-I to show the effect of selecting the optimum displacement angle on the dc-link voltage in time-domain.

Table 5-I MATLAP simulation parameters design

Active power P_g	4.7MW
Nominal FBMMC phase voltage U_m	3.3kV
Grid frequency,f_g	50Hz
Nominal $dc-link$ voltage, U_{dc}	6.6kV
Number of SM per arm, N	4
Generator frequency, f_s	$10 - 30$ Hz
Arm inductance, L_{arm}	7mH
SMs' capacitance, C_{SM}	7mF
Switching frequency, f_c	2000Hz
L_s	1mH

The voltages of the SM capacitors are considered to be ideal dc. The MATALB FFT function is used to extract the harmonic spectra of the time-domain waveforms and compare them to the proposed analytical models. In order to cover all critical operations, the following three operational conditions are considered.

- First operation condition (Figure 5-5), the system is working in buck mode with generator frequency $\mathrm{f_s} = 30\mathrm{Hz}$, and the modulations value is $\mathrm{M_{dc}} = 1$ and $\mathrm{M_{ac}} = 0.9$. Here, $\mathrm{NM_{dc}} = 4 \rightarrow \mathrm{integer}$.
- Second operation condition (Figure 5-6), the system is working in boost mode with generator frequency $\mathrm{f_s} = 25\mathrm{Hz}$, and the modulations value are $\mathrm{M_{dc}} = 0.8$ and $\mathrm{M_{ac}} = 1.1$. Here, $\mathrm{NM_{dc}} = \mathrm{fraction}$.
- Third operation condition (Figure 5-7), the system is working in boost mode with generator frequency $\mathrm{f_s} = 10\mathrm{Hz}$, and the modulations value are $\mathrm{M_{dc}} = 0.75$ and $\mathrm{M_{ac}} = 1.15$. Here, $\mathrm{NM_{dc}} = 3 \rightarrow \mathrm{integer}$.

Figure 5-5 shows the system working in buck mode with $\mathrm{M_{dc}} = 1$, $\mathrm{M_{ac}} = 0.9$, and $\mathrm{NM_{dc}} = 4 \rightarrow \mathrm{integer} \rightarrow \mathrm{even}$. At $\mathrm{m} = 1$, the term $\sin\left((\mathrm{mNM_{dc}} + \mathrm{n})\frac{\pi}{2}\right)$ is non-zero when $\mathrm{NM_{dc}} = \mathrm{even\ (or\ odd)},\ \mathrm{and\ n} = \mathrm{odd(or\ even)}$, as seen in Figure 5-5(d). Thus, complete harmonic elimination can be achieved by selecting the displacement angle $\theta_\mathrm{d} = 0$ to making the term $\cos\left(\frac{2\mathrm{mN}\theta_\mathrm{d} + \mathrm{n}\pi}{2}\right)$ zero at $\mathrm{n} = \mathrm{odd}$, as seen in Figure 5-5(f). At $\mathrm{m} = 2(\mathrm{or\ even})$, as declared by the term $\cos\left(\frac{2\mathrm{mN}\theta_\mathrm{d} + \mathrm{n}\pi}{2}\right)$, it achieves zero at $\theta_\mathrm{d} = \frac{\pi}{2\mathrm{N}}$ or $\theta_\mathrm{d} = 0$, see Figure 5-5(d) and (f). Figure 5-5(c) and (e) show clearly how the choice of the displacement angle affects the high frequency ripples in dc-link voltage.

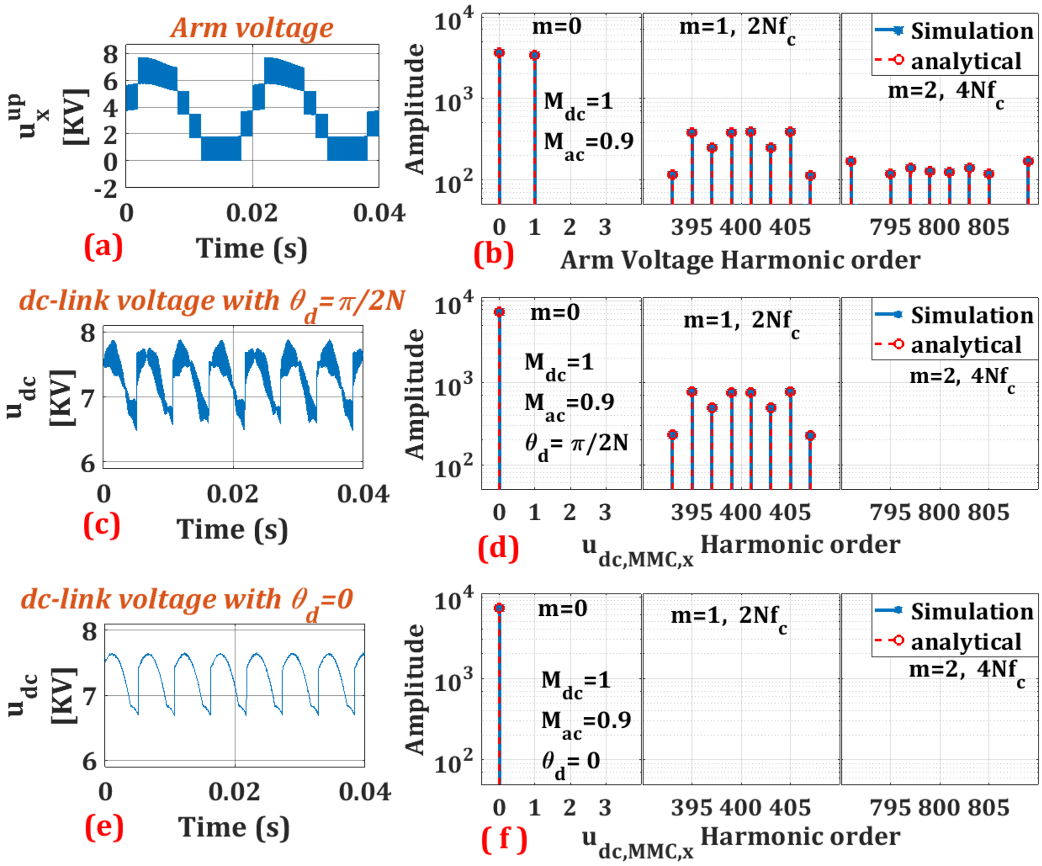


Figure 5-5 Buck mode operation, $M_{dc} = 1, M_{ac} = 0.9$, and $f_s = 30Hz$, (a) arm voltage time domain, (b) arm voltage frequency domain, (c) dc-link voltage time domain with $\theta_d = \pi/2N$, (f) dc-link voltage frequency domain with $\theta_d = \pi/2N$, (e) dc-link voltage time domain with $\theta_d = 0$, (f) dc-link voltage frequency domain with $\theta_d = 0$

The second operation condition is shown in Figure 5-6, here the system is operated in the boost mode with $\mathrm{M_{dc}} = 0.8$, $\mathrm{M_{ac}} = 1.1$, and round $(\mathrm{N} \times \mathrm{M_{dc}} = 3.2 \rightarrow \mathrm{odd})$. At $\mathrm{m} = 1$, the term of $\sin\left((\mathrm{mNM_{dc}} + \mathrm{n})\frac{\pi}{2}\right)$ is non-zero when $\mathrm{NM_{dc}} = \mathrm{fraction}$, for all $\mathrm{n} = \mathrm{odd}(\mathrm{or\ even})$, however as the round $(\mathrm{N} \times \mathrm{M_{dc}}) =$ is odd, the higher harmonicas amplitude is found at $\mathrm{n} = \mathrm{even}$, see Figure 5-6(f) . Therefore, the maximum harmonic minimization can be achieved through choosing the displacement angle $\theta_d = \pi/2\mathrm{N}$ to make the term $\cos\left(\frac{2\mathrm{mN}\theta_d + \mathrm{n}\pi}{2}\right)$ zero at $\mathrm{n} = \mathrm{even}$, as seen in Figure 5-6 (d). The high frequency ripples in dc-link voltage are strongly impacted by the choice of displacement angle, as demonstrated by Figure 5-6 (c) and (e).

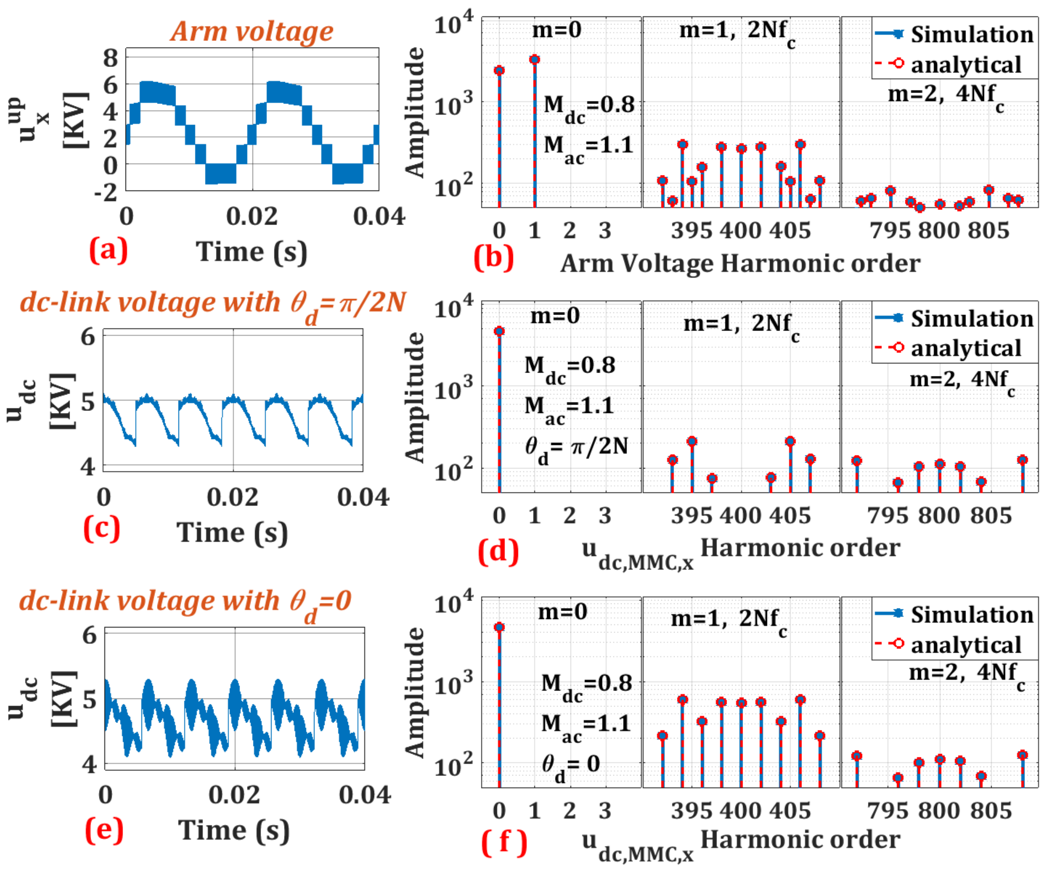


Figure 5-6 Boost mode operation, $M_{dc} = 0.8, M_{ac} = 1.1, and\ f_s = 25Hz,$, (a) arm voltage time domain, (b) arm voltage frequency domain, (c) dc-link voltage time domain with $\theta_d = \pi/2N$, (f) dc-link voltage frequency domain with $\theta_d = \pi/2N$, (e) dc-link voltage time domain with $\theta_d = 0$, (f) dc-link voltage frequency domain with $\theta_d = 0$

The third operation condition is shown in Figure 5-7, here the system is operated in the boost mode with $\mathrm{M_{dc}} = 0.75$, $\mathrm{M_{ac}} = 1.15$, and $\mathrm{NM_{dc}} = 3 \rightarrow \text{integer} \rightarrow$ odd. At $\mathrm{m} = 1$, the term of $\sin\left((\mathrm{mNM_{dc}} + \mathrm{n})\frac{\pi}{2}\right)$ is non-zero when $\mathrm{NM_{dc}} =$ even (or odd), and $\mathrm{n} =$ odd(or even), as seen in Figure 5-7(f). Thus, complete harmonic elimination can be achieved by selecting the displacement angle $\theta_\mathrm{d} = \pi/2\mathrm{N}$ to making the term $\cos\left(\frac{2\mathrm{mN}\theta_\mathrm{d}+\mathrm{n}\pi}{2}\right)$ zero at $\mathrm{n} =$ even, as seen in Figure

5-7(d). At $\mathrm{m}=2$(or even), as stated by the term of $\cos\left(\frac{2\mathrm{mN}\theta_\mathrm{d}+\mathrm{n}\pi}{2}\right)$, it achieves zero at $\theta_\mathrm{d}=\frac{\pi}{2\mathrm{N}}$ or $\theta_\mathrm{d}=0$, see Figure 5-7 (d) and (f). Figure 5-7(c) and (e) show clearly how the choice of the displacement angle affects the high frequency ripples in dc-link voltage.

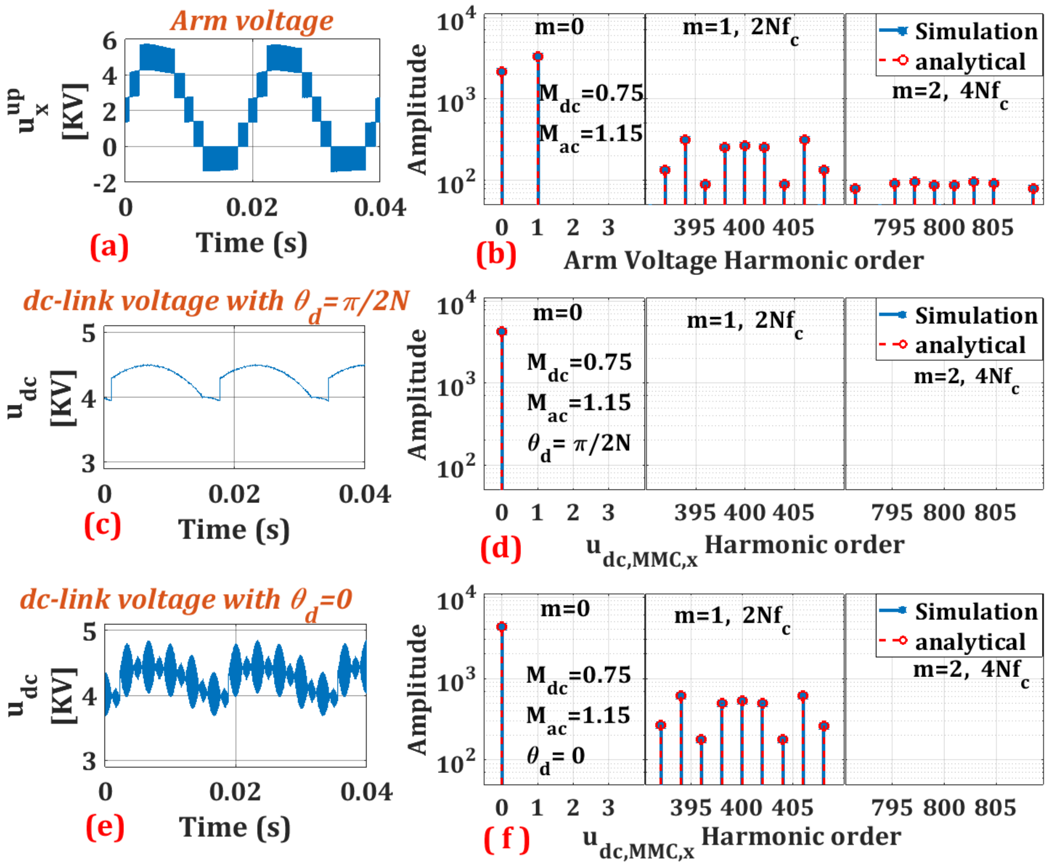


Figure 5-7 Boost mode operation, $M_{dc}=0.75, M_{ac}=1.15, and\ f_s=10Hz,$, (a) arm voltage time domain, (b) arm voltage frequency domain, (c) dc-link voltage time domain with $\theta_d=\pi/2N$, (f) dc-link voltage frequency domain with $\theta_d=\pi/2N$, (e) dc-link voltage time domain with $\theta_d=0$, (f) dc-link voltage frequency domain with $\theta_d=0$

Figure 5-5, Figure 5-6, and Figure 5-7 show that the analytical model and simulation findings are in perfect agreement, which verifies the optimum design selection for the displacement angle in equation (5.27).

5.6.2 Experimental Verification

To test the effectiveness of the suggested analytical model, laboratory experiments are performed on a prototype. The experimental setup is described in detail in Chapter 2. A three phase FBMMC with front end 6-pulse rectifier is bulti with $N = 2$. The IKCM20L60GDXKMA1 from INFINEON intelligent power module is used to design each SM and OPAL-RT 5607 is the control platform. An ac power source (Chroma 61703) is used as a generator with frequency range 15-30Hz. The FBMMC ac side is connected to passive load of 10Ω. The experimental setup parameters are given in Table 5-II

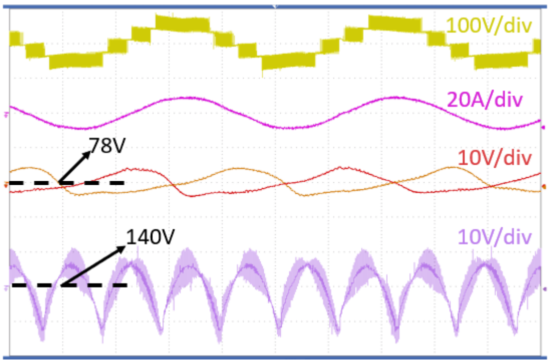
Table 5-II Parameters of the proposed system experimental prototype

dc − link voltage (U_{dc})	140 V(nominal), 77V, 70V
Ac side frequency	50Hz
Switching frequency	2500Hz
Load resistance	10Ω
Submodules Number of each arm (N)	2
Arm impedance (R_{arm}, L_{arm})	0.64Ω, 1.85mH
Module capacitance (C_{SM})	2.1mF
Load peak current	7A

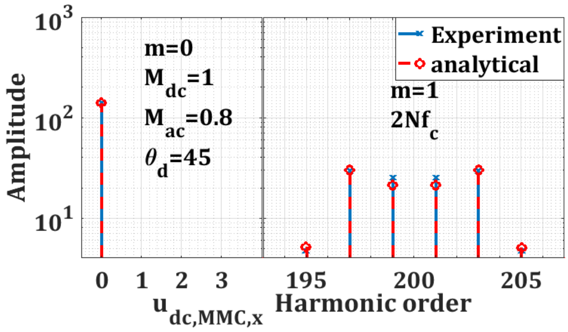
The FFT results of the measured $u_{dc,MMC,x}$ are compared to the developed analytical harmonic spectra. Figure 5-8, Figure 5-9, and Figure 5-10 show a very good agreement between the analytical model and the experimental results. The insignificant discrepancies can be noticed, as a result of the influence of the SM capacitor voltage ripple and control. However, these differences can be ignored as they are not affecting the optimum selection of the displacement angle θ_d. Here, three operating conditions are presented to cover all possible scenarios.

- Case (1) (Figure 5-8), the system is working in buck mode with generator frequency $f_s = 30\text{Hz}$, and the modulations value are $M_{dc} = 1$ and $M_{ac} = 0.8$. Here, $NM_{dc} = 2$→integer.
- Case (2) (Figure 5-9), the system is working in boost mode with generator frequency $f_s = 25\text{Hz}$, and the modulations value are $M_d = 0.55$ and $M_{ac} = 1.25$. Here, NM_{dc} =fraction.
- Case (3) (Figure 5-10), the system is working in boost mode with generator frequency $f_s = 25\text{Hz}$, and the modulations value are $M_{dc} = 0.5$ and $M_{ac} = 1.1$. Here, $NM_{dc} = 1 \rightarrow integer$.

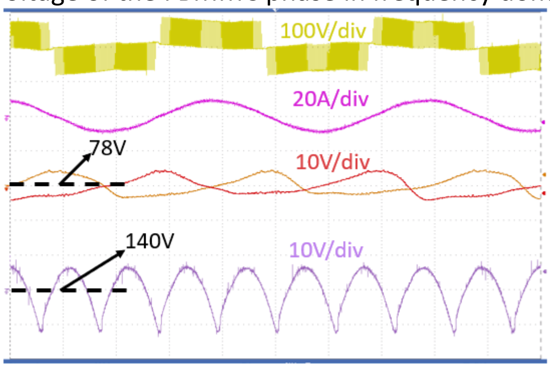
For Case (1) in Figure 5-8, the product of $NM_{dc} = 2 \rightarrow integer \rightarrow even$, thus from equation (5.27), a complete harmonic elimination can be achieved with $\theta_d = 0$, as seen in Figure 5-8(d). For Case (2) in Figure 5-9, the product of $NM_{dc} = 1.1 \rightarrow fraction$ and the nearest integer is odd, thus from equation (5.27), the maximum harmonic minimization can be achieved with $\theta_d = \pi/2N$, as seen in Figure 5-9 (d). For Case (3) in Figure 5-10, the product of $NM_{dc} = 2 \rightarrow integer \rightarrow odd$, thus from equation (5.27), a complete harmonic elimination can be achieved with $\theta_d = \pi/2N$, as seen in Figure 5-10(b).



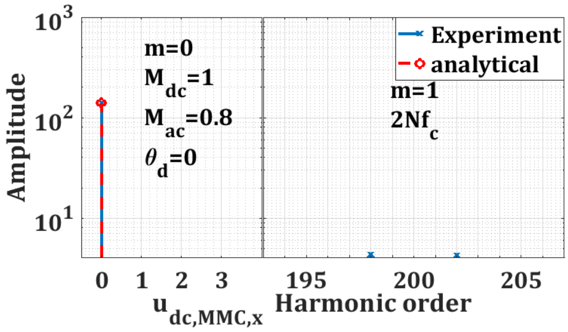
(a) (from top) MMC output voltage and current, submodule capacitors voltages, dc-link voltage with $\theta_d = \pi/2N$ {timescale 5ms/div}



(b) The dc-terminal voltage of the FBMMC phase in frequency domain with $\theta_d = \pi/2N$

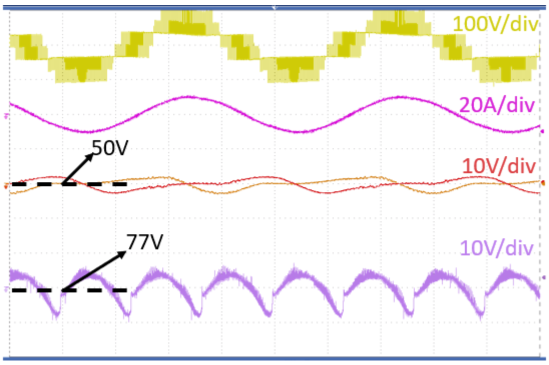


(c) (from top) MMC output voltage and current, submodule capacitors voltages, dc-link voltage with $\theta_d = 0$ {timescale 5ms/div}

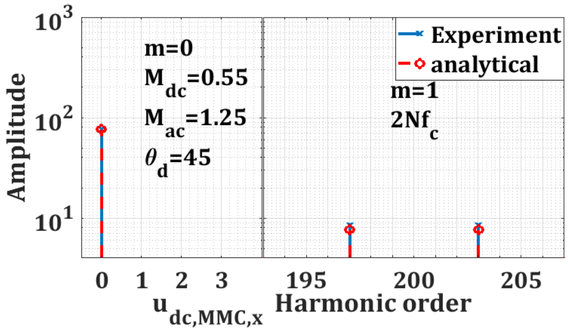


(d) The dc-terminal voltage of the FBMMC phase in frequency domain with $\theta_d = 0$

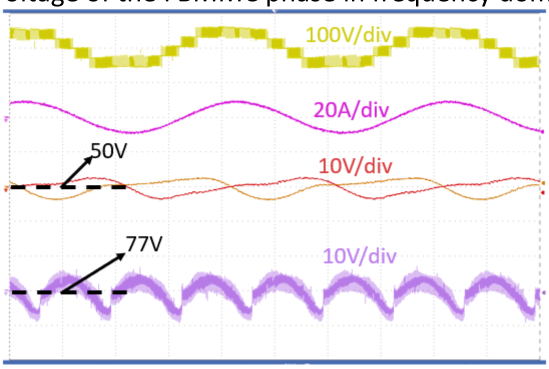
Figure 5-8 Case (1): Back mode steady-state time domain experimental results and harmonic spectrum of $u_{dc,MMC,x}$ with $M_{dc} = 1$.



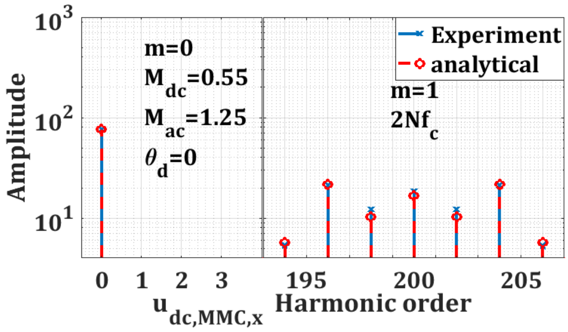
(a) (from top) MMC output voltage and current, submodule capacitors voltages, dc-link voltage with $\theta_d = \pi/2N$ {timescale 5ms/div}



(b) The dc-terminal voltage of the FBMMC phase in frequency domain with $\theta_d = \pi/2N$

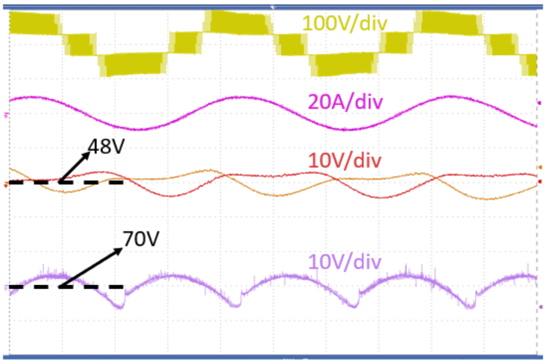


(c) (from top) MMC output voltage and current, submodule capacitors voltages, dc-link voltage with $\theta_d = 0$ {timescale 5ms/div}

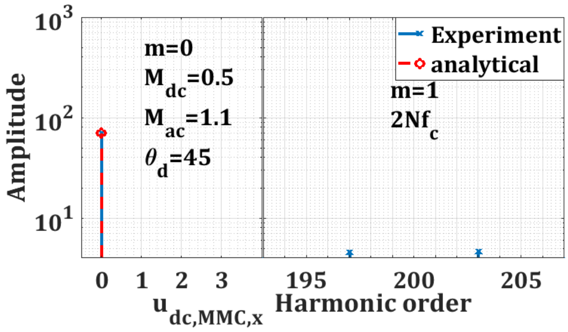


(d) The dc-terminal voltage of the FBMMC phase in frequency domain with $\theta_d = 0$

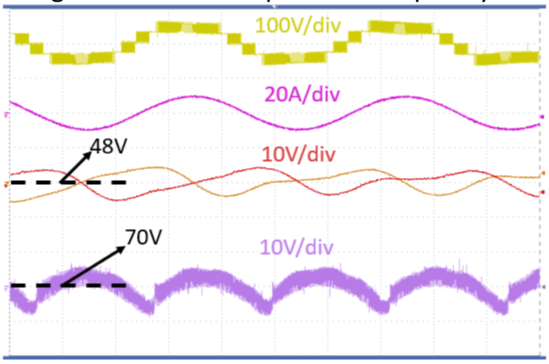
Figure 5-9 Case (2): Boost mode steady-state time domain experimental results and harmonic spectrum of $u_{dc,MMC,x}$ with $M_{dc} = 0.55$.



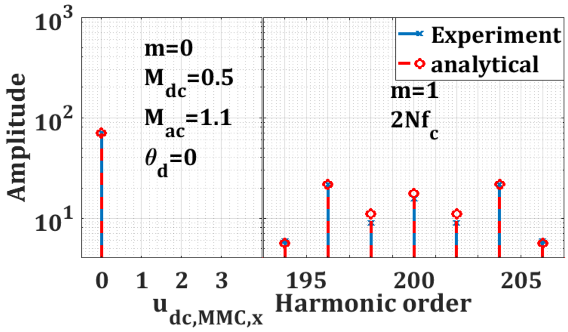
(a) (from top) MMC output voltage and current, submodule capacitors voltages, dc-link voltage with $\theta_d = \pi/2N$ {timescale 5ms/div}



(b) The dc-terminal voltage of the FBMMC phase in frequency domain with $\theta_d = \pi/2N$



(c) (from top) MMC output voltage and current, submodule capacitors voltages, dc-link voltage with $\theta_d = 0$ {timescale 5ms/div}



(d) The dc-terminal voltage of the FBMMC phase in frequency domain with $\theta_d = 0$

Figure 5-10 Case (3): Boost mode steady-state time domain experimental results and harmonic spectrum of $u_{dc,MMC,x}$ with $M_{dc} = 0.5$.

It is worth to note that simulation results (Figure 5-5 and Figure 5-7) and experiment results (Figure 5-8 and Figure 5-10) show the dc-link voltage can be totally smoothed out from the high frequency ripples by a proper selection of the displacement angle, when the product of NM_{dc} is integer.

This emphasises that the correct selection of the displacement angle eliminates not only the odd groups of the carrier, but also the even groups of the carrier, as mentioned previously.

5.7 Optimal displacement angle for the ac side of the FBMMC

For the sake of completeness and because this proposed system might be employed for various applications, the optimal displacement angle for the ac side is also included, as developed in [88].

The high frequency ripple related to the carrier frequency in the ac side of the FBMMC $\mathrm{u_{o,x,h}}$ can be found as :

$$\mathrm{u_{m,x}} = \frac{\mathrm{u_x^{low}} - \mathrm{u_x^{up}}}{2} = \mathrm{u_{o,x,f}} + \mathrm{u_{o,x,h}} \tag{5.28}$$

Therefore, from equations (5.18), (5.19), and (5.28), the general form including the ac side high frequency ripple can be addressed as:

$$\mathrm{u_{out,x}} = \frac{\mathrm{NU_c^oM_{ac}}}{2}\cos(\omega t + \theta_x) \tag{5.29}$$

$$+\mathrm{Re}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\sin\left(2mN\omega_c t+n(\omega t+\theta_x)+\frac{2mN\theta_d+n\pi}{2}\right)$$

$$\times\left[\frac{2U_c^o}{m\pi}J_n\left(mNM_{ac}\frac{\pi}{2}\right)\cos(mN\pi)\right]$$

$$\times\sin\left((mNM_{dc}+n)\frac{\pi}{2}\right)\sin\left(\frac{2mN\theta_d+n\pi}{2}\right)$$

Similarly, the order {m, n} of the zero and nonzero harmonics is a function of M_{dc}, N and θ_d and is defined by the product of $\sin\left((mNM_{dc}+n)\frac{\pi}{2}\right)\times\sin\left(\frac{2mN\theta_d+n\pi}{2}\right)$.

5.7.1 when m is odd

Similarly, the first high-frequency carrier group defines the filter requirement (i.e., m = 1 or m = odd). For the terms of $\sin\left((mNM_{dc}+n)\frac{\pi}{2}\right)\times\sin\left(\frac{2mN\theta_d+n\pi}{2}\right)$, Figure 5-11 summarizes the optimum selection of the displacement angle θ_d for the ac side of the FBMMC when the product of NM_{dc} is integer (i.e., at $K+2, K+1,$ and $K+0$), only $n=\mathrm{odd}$ or $n=\mathrm{even}$ exists. Then, the term $\sin\left(\frac{2mN\theta_d+n\pi}{2}\right)$ is used to achieve a complete harmonics elimination via appropriate selection of θ_d . On the other hand, when the product of NM_{dc} is a fraction (i.e., between $K+2$ and $K+1,$ and between $K+1$ and $K+0$), the term of $\sin\left(\frac{2mN\theta_d+n\pi}{2}\right)$ is used to eliminate the higher harmonicas amplitude at $n=\mathrm{odd}$ or $n=\mathrm{even}$ through appropriate selection of θ_d. From this the optimum displacement angle θ_d for the ac side of the FBMMC, can be given as:

$$u_{o,x} = minimum\ at\ m = 1\ (i.e., m = odd), for$$
$$\theta_d = \frac{\pi}{2N}, when\ \{round\ (NM_{dc}) is\ even\}$$
$$or \tag{5.30}$$
$$\theta_d = 0, when\ \{round\ (NM_{dc})\ \ is\ odd\}$$

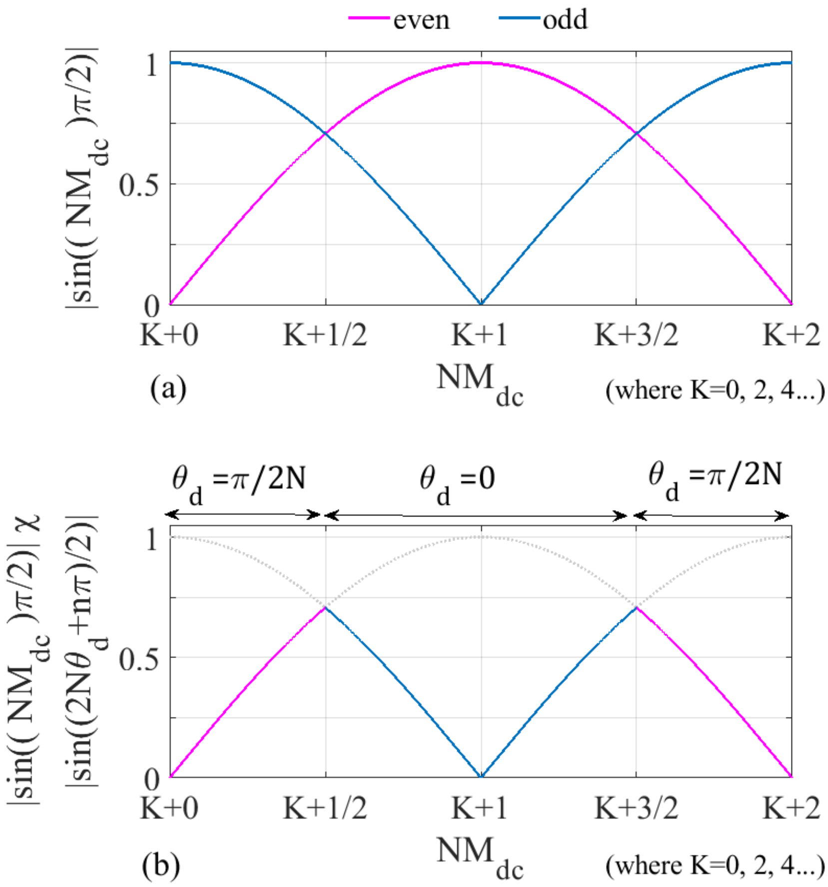


Figure 5-11 (a)Variation of $even$ and odd harmonics in dc-terminal voltage, and (b) Selection of optimal θ_d for the dc-terminal voltage of the FBMMC

Equation (5.27) , and equation (5.30) show that the optimum selection of the displacement angle θ_d for the as side of the FBMMC is opposite for the dc-terminal of the FBMMC. This implies that selecting the displacement angle to achieve least high frequency ripples at the dc-terminal of the FBMMC will result in maximum high frequency ripples at the ac-terminal of the FBMMC and vice versa.

5.7.2 When m is even

When *m* is even and when the product of $\mathrm{NM_{dc}}$ is integer, the term $\sin\left((\mathrm{mNM_{dc}}+\mathrm{n})\frac{\pi}{2}\right)$ has nonzero condition when $\mathrm{NM_{dc}} = \mathrm{even},\ \mathrm{and}\ \mathrm{n} = \mathrm{odd}.$ At n=odd the term of $\sin\left(\frac{2\mathrm{mN}\theta_\mathrm{d}+\mathrm{n}\pi}{2}\right)$ is nonzero for $\theta_\mathrm{d} = 0$ or $\theta_\mathrm{d} = \pi/2\mathrm{N}$. This indicates that, unlike the dc-terminal of the FBMMC, the even group will always exist on the ac side of the FBMMC. In another word with optimum displacement angle in the ac side of the FBMMC, the effective switching frequency is moved from $2\mathrm{Nf_c}$ to $4\mathrm{Nf_c}$, when the product of $\mathrm{NM_{dc}}$ is integer. Finally, when *m* is even and when the product of $\mathrm{NM_{dc}}$ is a fraction the term $\sin\left((\mathrm{mNM_{dc}}+\mathrm{n})\frac{\pi}{2}\right)$ has nonzero condition for all n (i.e., $\mathrm{n} = 0, \pm 1, \pm 2, \ldots$).

5.7.3 Simulation verification

Although the analytical model was verified previously, more simulation results are presented to emphasis the effectiveness of the general form representing the ac side high frequency ripples i.e., equation (5.29). The following two operation conditions are presented:

- First operation condition (Figure 5-12), the system is working in the buck mode with $\mathrm{M_{dc}} = 1$ and $\mathrm{M_{ac}} = 0.9$. Here, $\mathrm{NM_{dc}} = 4 \rightarrow \mathrm{integer}$.
- Second operation condition (Figure 5-13), the system is working in the boost mode with $\mathrm{M_{dc}} = 0.8$ and $\mathrm{M_{ac}} = 1.1$. Here, $\mathrm{NM_{dc}} = \mathrm{fraction}$

Figure 5-12 shows the system working in buck mode with $M_{dc} = 1$, $M_{ac} = 0.9$, and $NM_{dc} = 4 \rightarrow \text{integer} \rightarrow \text{even}$. At $m = 1$, the term $\sin\left((mNM_{dc} + n)\frac{\pi}{2}\right)$ is non-zero when $NM_{dc} = \text{even (or odd)}$, and $n = \text{odd(or even)}$, as seen in Figure 5-12 (d). Thus, complete harmonic elimination can be achieved by selecting the displacement angle $\theta_d = \frac{\pi}{2N}$ to make the term $\sin\left(\frac{2mN\theta_d+n\pi}{2}\right)$ zero at $n = \text{odd}$, as found in Figure 5-12 (b). The even group of m, as declared by the term $\sin\left(\frac{2mN\theta_d+n\pi}{2}\right)$, is not eliminated at $\theta_d = \frac{\pi}{2N}$ or $\theta_d = 0$, see Figure 5-12 (b) and (d). Figure 5-12 (a) and (c) show clearly how the choice of the displacement angle affects the number of voltage levels in the output voltage.In Figure 5-13 the system is operated in the boost mode with $M_{dc} = 0.8$, $M_{ac} = 1.1$, and $round\ (NM_{dc} = 3.2 \rightarrow \text{odd})$. At $m = 1$, the term $\sin\left((mNM_{dc} + n)\frac{\pi}{2}\right)$ is non-zero when $NM_{dc} = \text{fraction, for all } n = \text{odd or even}$, however as the $round\ (NM_{dc})$ is odd, the higher harmonics amplitude is found at $n = \text{even}$, see Figure 5-13(b). Therefore, the maximum harmonic minimization can be achieved through choosing the displacement angle $\theta_d = 0$ to make the term $\sin\left(\frac{2mN\theta_d+n\pi}{2}\right)$ zero at $n = \text{even}$, as seen in Figure 5-13(d). The number of voltage levels in the output voltage are strongly impacted by the choice of displacement angle, as demonstrated by Figure 5-13 (a) and (c).

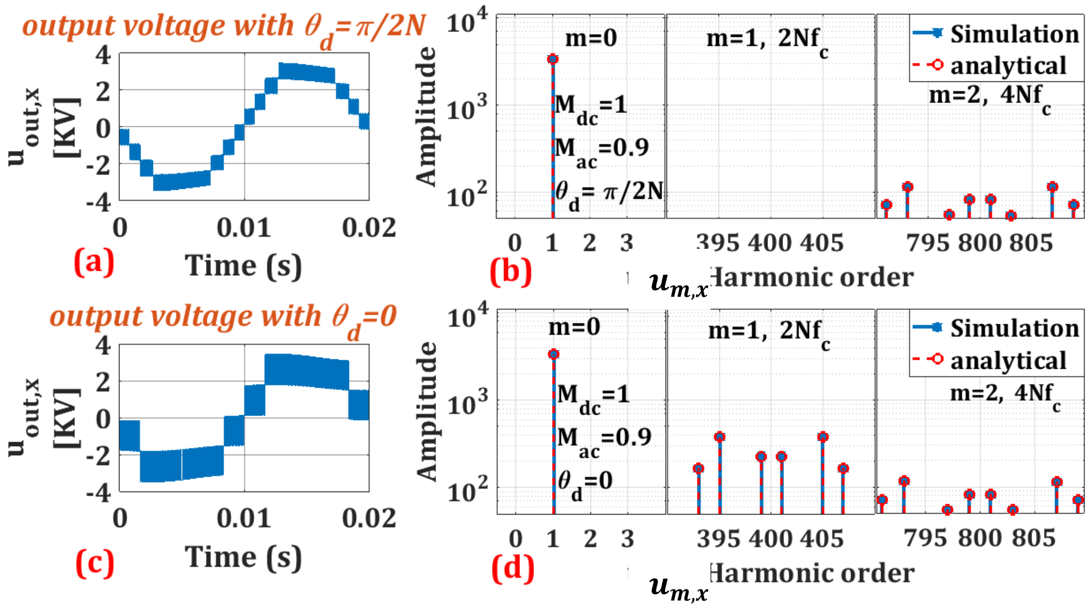


Figure 5-12 Buck mode operation, $M_{dc} = 1, M_{ac} = 0.9$, (a) FBMMC output voltage in time domain with $\theta_d = \pi/2N$, (b) FBMMC output voltage in frequency domain with $\theta_d = \pi/2N$, (c) FBMMC output voltage in time domain with $\theta_d = 0$, (d) FBMMC output voltage in frequency domain with $\theta_d = 0$

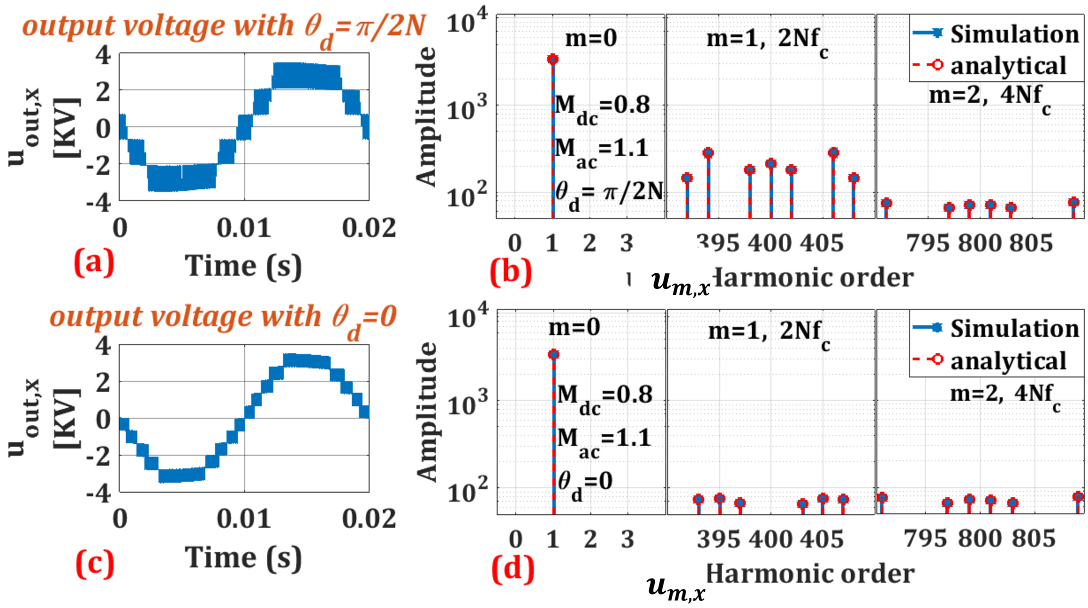


Figure 5-13 Boost mode operation, $M_{dc} = 0.8, M_{ac} = 1.1$, (a) FBMMC output voltage in time domain with $\theta_d = \pi/2N$, (b) FBMMC output voltage in frequency domain with $\theta_d = \pi/2N$, (c) FBMMC output voltage in time domain with $\theta_d = 0$, (d) FBMMC output voltage in frequency domain with $\theta_d = 0$

5.8 Optimal displacement angle discussion

5.8.1 Fixed dc-link voltage level

The FBMMC is characterised with boost mode operation. Recent studies show that operating the FBMMC at a certain boost mode level reduces the size of the SM capacitor significantly [84] [106] [107]. Thus, it will be more beneficial to also design the parameters of the FBMMC in which the product of the NM_{dc} is integer. The carrier displacement angle can then be chosen to eliminate all high-frequency carrier groups at m_{odd} on the ac side of the MMC or all high-frequency carrier groups at m_{odd} and m_{even} on the dc side.

The previous investigation revealed that selecting the displacement angle to achieve the least switching frequency ripples at the dc-terminal of the FBMMC results in the greatest switching frequency ripples at the ac side of the FBMMC and vice versa.

However, when the product of NM_{dc} is integer, choosing the displacement angle to eliminate the high frequency ripples in the FBMMC's dc-terminal has an additional advantage in that a suitable selection of θ_d eliminates not only the odd groups of the carrier but also the even groups of the carrier. This means that the filter in the dc-link voltage is no longer required.

On the other hand, when the product of NM_{dc} is integer, selecting the displacement angle to eliminate the high frequency ripples in ac side of the

FBMMC only eliminate the odd groups of the carrier. This means the ac side may still needs a filter for the even groups of the carrier.

5.8.2 Variable dc-link voltage level

Under variable dc-link voltage, the product of NM_{dc} is not always an integer and thus complete switching frequency ripples elimination cannot be achieved, as the lowest harmonics group in both side of the FBMMC is still found at first carrier group m=1 or in another word at $2Nf_c$. In fact, under variable dc-link voltage, the mentioned values of the displacement angle (i.e., either $\theta_d = 0$ or $\theta_d = \pi/2N$) may no longer be the optimum selection.

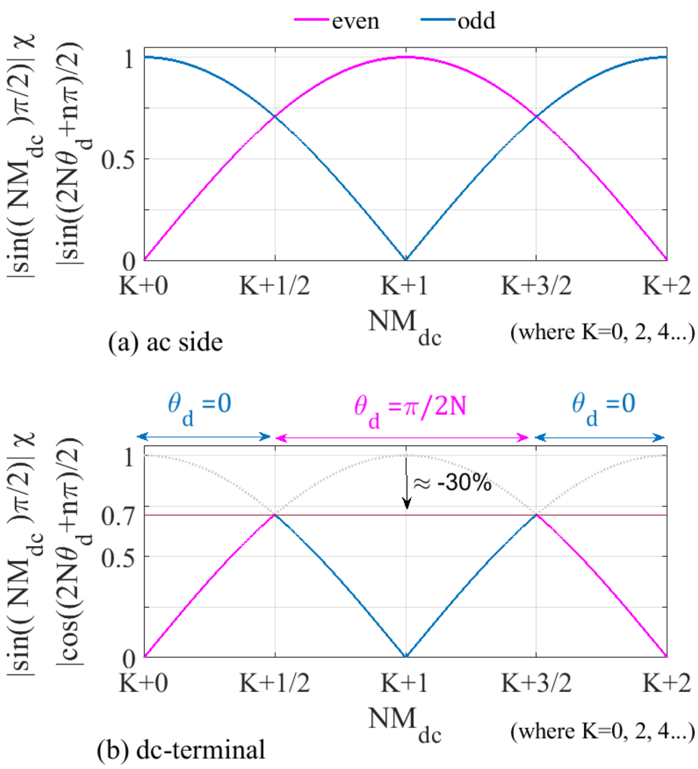


Figure 5-14 Variation of $even$ and odd harmonics for both side of the FBMMC at the optimum displacement angle for the dc-terminal of the inverter. (a) ac side, (b) dc-terminal side

Assuming the displacement angle is selected as either $\theta_d = 0$ or $\theta_d = \pi/2N$ to minimize the switching frequency ripples at the dc-terminal of the FBMMC, Figure 5-14 shows that the dc-Link filter design requirements will probably benefit from an approximately 30% reduction in the amplitude of the first carrier group m=1. By contrast, the ac side filter design requirements need to consider maximum switching frequency ripples in the ac side.

5.8.3 Optimal displacement angle for both sides of the FBMMC

To maximise the benefit of the displacement angle selection, a new displacement angle value will be presented. Focusing on the first carrier group m=1, the terms $\cos\left(\frac{2N\theta_d+n\pi}{2}\right)\times\sin\left((NM_{dc}+n)\frac{\pi}{2}\right)$ define the high frequency ripples amplitude of the dc-terminal of the FBMMC, and the terms $\sin\left(\frac{2N\theta_d+n\pi}{2}\right)\times\sin\left((NM_{dc}+n)\frac{\pi}{2}\right)$ define the high frequency ripples amplitude of the ac side of the FBMMC. The terms $\cos\left(\frac{2N\theta_d+n\pi}{2}\right)$ and $\sin\left(\frac{2N\theta_d+n\pi}{2}\right)$ can be designed to equalize using the trigonometric expression provided in equation (5.31).

$$\left|\cos\left(\frac{H_3\pi}{4}\right)\right| = \left|\sin\left(\frac{H_3\pi}{4}\right)\right| = 0.7071 \qquad (5.31)$$

Where $(H_3 = 1,\ 3,\ 5 \dots)$. Therefore, from equation (5.31) the optimal displacement angle for both side of the FBMMC is $\theta_d = \frac{H_3\pi}{4N}$ (or simply $\theta_d = \pi/4N$). By selecting the displacement angle as $\theta_d = \pi/4N$, this gives an approximately 30% reduction in the amplitude of the first carrier group m=1 in both side of the FBMMC, as seen in Figure 5-15. Thus, the ac side and the dc side filter design requirements will probably benefit from an approximately 30% reduction in the amplitude of the first carrier group m=1.

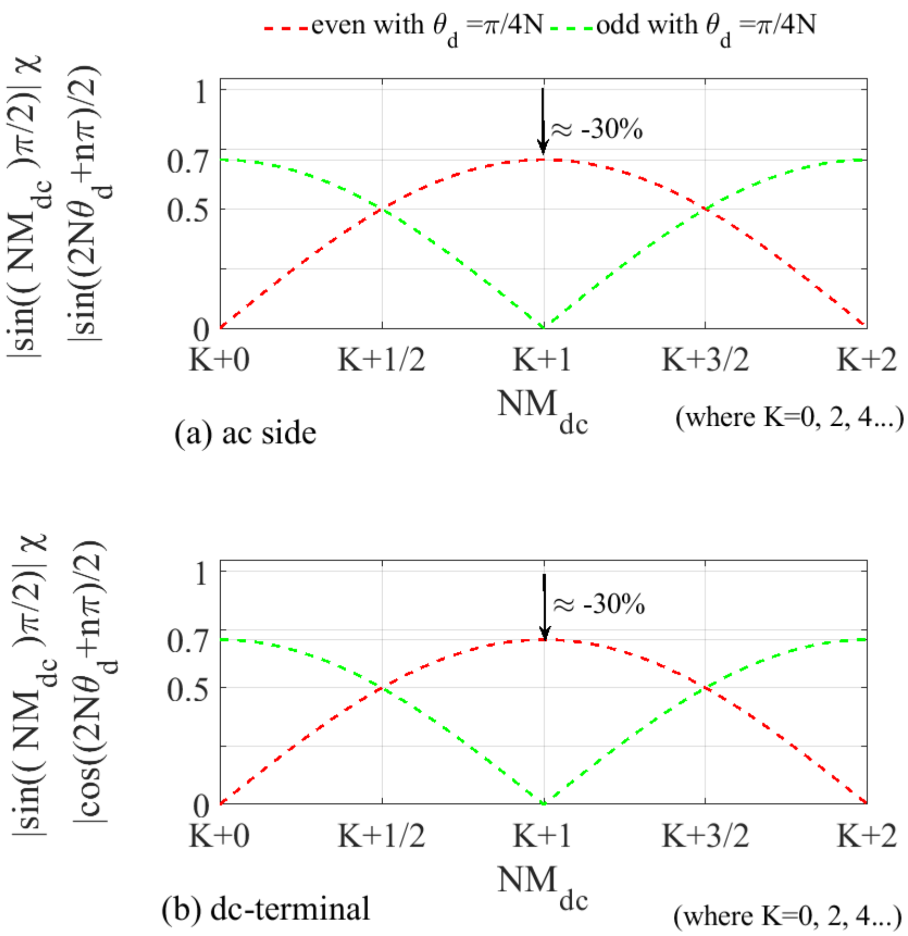


Figure 5-15 Variation of $even$ and odd harmonics for both side of the FBMMC at $\theta_d = \pi/4N$. (a) ac side, (b) dc-terminal side

It is worth noting in Figure 5-15 that setting the displacement angle to $\theta_d = \pi/4N$ does not eliminate $n = even$ or $n = odd$ harmonics groups. However, it reduces each of them by about 30%.

5.8.4 Simulation verification

To verify the efficacy of the new suggested displacement angle ($\theta_d = \pi/4N$), two operation conditions are simulated.

- First operation condition (Figure 5-16(a) and (b)), the system is working in the buck mode with $M_{dc} = 1$ and $M_{ac} = 0.9$. Here, $NM_{dc} = 4 \rightarrow integer$.
- Second operation condition (Figure 5-16(c) and (d)), the system is working in the boost mode with $M_{dc} = 0.8$ and $M_{ac} = 1.1$. Here, $NM_{dc} = fraction$.

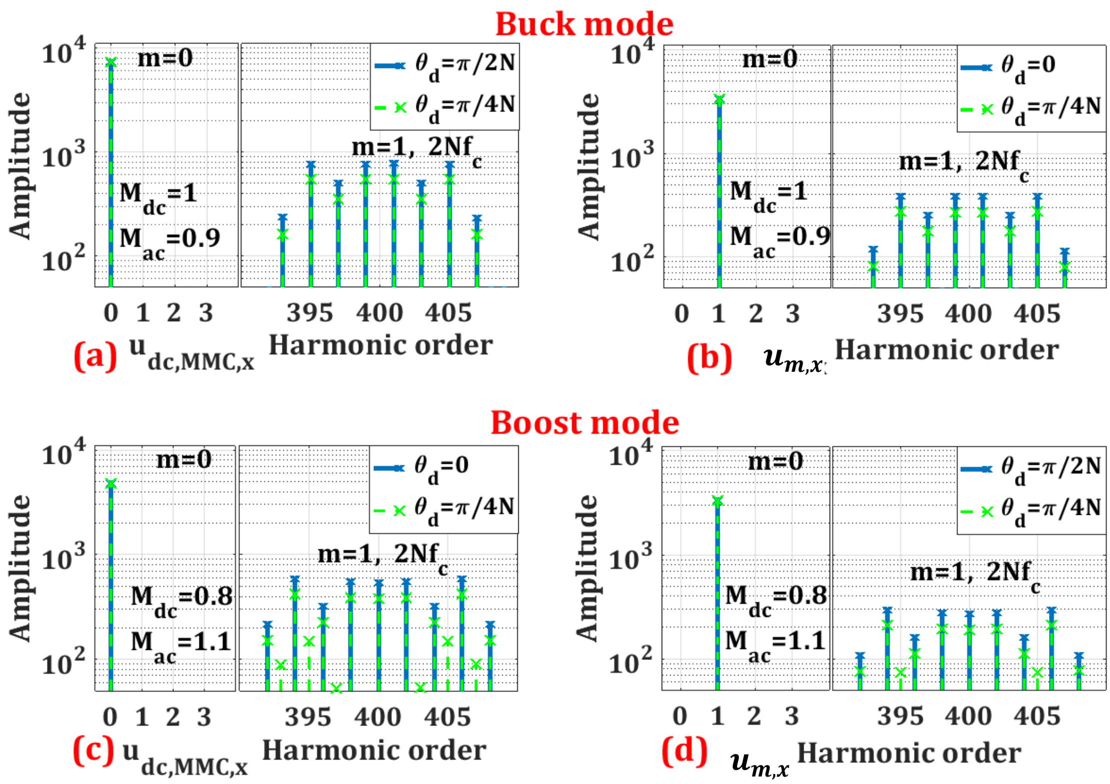


Figure 5-16 dc-terminal and ac side harmonic spectra at different displacement angles in buck and boost modes

Figure 5-16 (a) and (b) show the harmonic spectra of the dc-terminal and ac side of the FBMMC at buck mode operation. Here, in blue bars, the displacement angle is chosen to give the maximum switching frequency harmonics in both side (i.e., $\theta_d = \pi/2N$ at the dc terminal, Figure 5-16 (a), and $\theta_d = 0$ at the ac side Figure 5-16 (b)). Then, the maximum switching frequency harmonics (on both sides of the FBMMC) are compared against the switching frequency harmonics of the FBMMC when the displacement angle is set to $\theta_d = \pi/4N$. As stated, a 30% reduction is achieved in both sides.

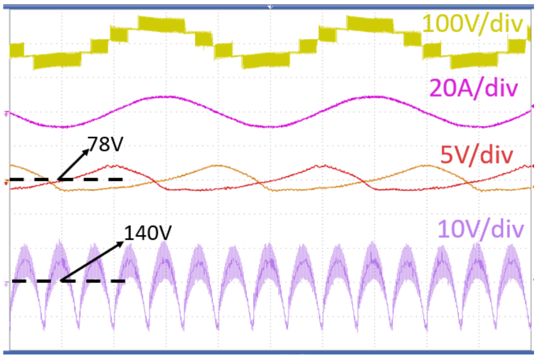
In boost mode operation condition, Figure 5-16 (c) and (d) also show a 30% reduction is achieved in both sides when the displacement angle is set to $\theta_d = \pi/4N$. Thus, both the ac side filter and the dc-link filter can be decreased simultaneously.

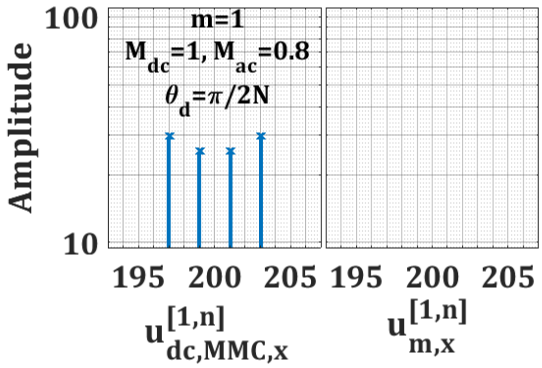
5.8.5 Experimental verification

Extensive comparison is presented to verify the previous discussion through the experimental setup. The main parameters are presented in Table 5-II. Here, the frequency of the generator is set to $f_s = 50Hz$ to make the discussion more general, since the proposed system can be used for different applications. Two operating conditions are presented at different displacement angle (i.e., at $\theta_d = 0$, $\theta_d = \pi/2N$, and $\theta_d = \pi/4N$).

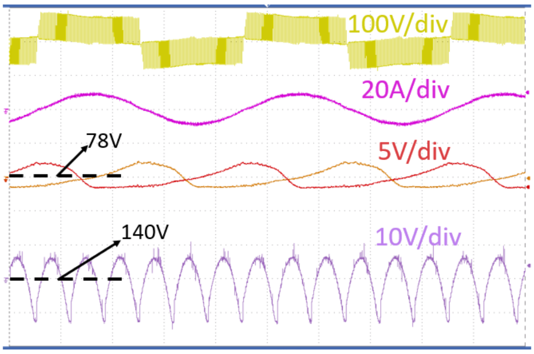
- Case (1) (Figure 5-17), the system is working in buck mode with generator frequency $f_s = 50\text{Hz}$, and the modulations values are $M_{dc} = 1$ and $M_{ac} = 0.8$. Here, $NM_{dc} = 2 \rightarrow \text{integer}$.
- Case (2) (Figure 5-18), the system is working in boost mode with generator frequency $f_s = 50\text{Hz}$, and the modulations values are $M_{dc} = 0.6$ and $M_{ac} = 1.2$. Here, $NM_{dc} = \text{fraction}$.

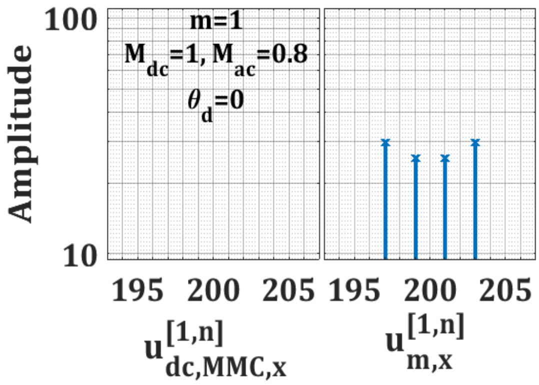
Figure 5-17 shows the system working in the buck mode condition, whereas Figure 5-18 shows the system working in the boost mode condition. As expected, setting the displacement angle to create the least switching frequency ripples at the FBMMC's dc-terminal results in the biggest switching frequency ripples at the FBMMC's ac side, and vice versa. The efficacy of all mentioned displacement angles (i.e., at $\theta_d = 0$, $\theta_d = \pi/2N$, and $\theta_d = \pi/4N$) is verified. Figure 5-17 (c) and Figure 5-18 (c) show that selecting the displacement angle of $\theta_d = \pi/4N$ achieves a 30% reduction in both sides. The effect of this reduction can be seen clearly in the time-domain waveforms as well. Moreover, setting the displacement angle to $\theta_d = \pi/4N$ improves the quality of output voltage. This is because the number of voltage levels in the output voltage is increased, and thus reducing the dv/dt voltage stress on the ac side components. At the same time, the switching-ripple voltage on the dc-link is reduced.



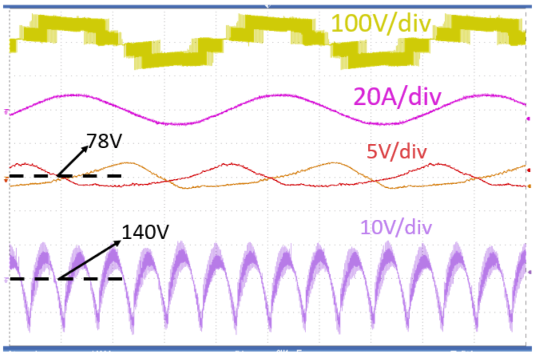


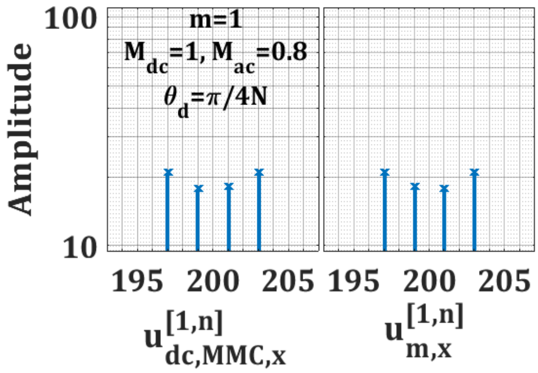
(a) (from top) MMC output voltage and current, submodules capacitor voltage, dc-link voltage with $\theta_d = \pi/2N$ {timescale 5ms/div}





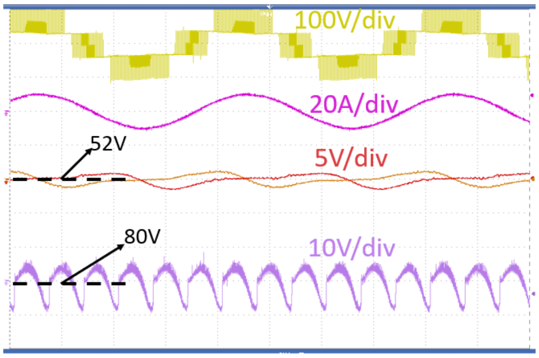
(b) (from top) MMC output voltage and current, submodules capacitor voltage, dc-link voltage with $\theta_d = 0$ {timescale 5ms/div}

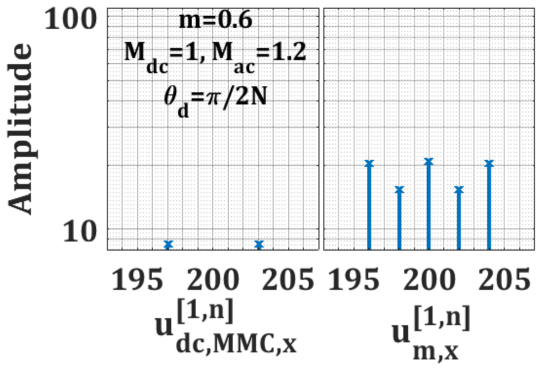




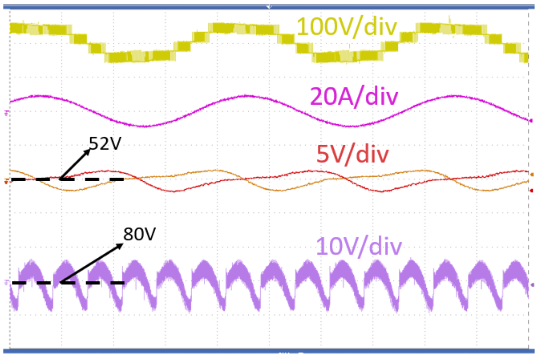
(c) (from top) MMC output voltage and current, submodules capacitor voltage, dc-link voltage with $\theta_d = \pi/4N$ {timescale 5ms/div}

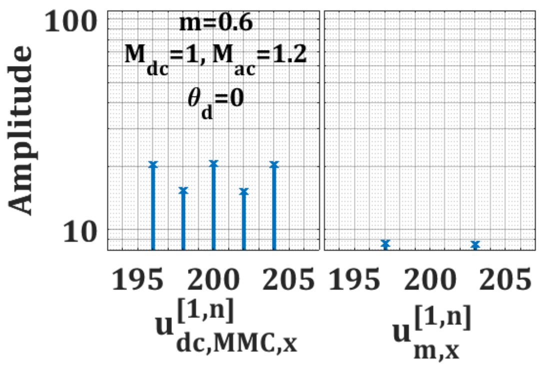
Figure 5-17 Buck mode operation M_{dc} =1 and $M_{ac} = 0.9$. (a) $\theta_d = \pi/2N$, (b) $\theta_d = 0$, (c) $\theta_d = \pi/4N$



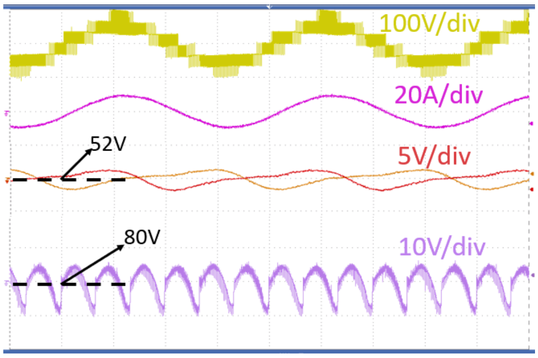


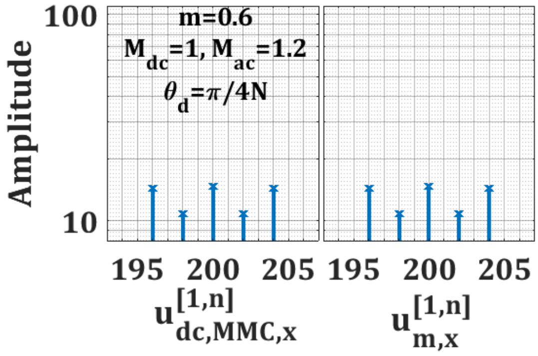
(a) (from top) MMC output voltage and current, submodules capacitor voltages, dc-link voltage with $\theta_d = \pi/2N$ {timescale 5ms/div}





(b) (from top) MMC output voltage and current, submodules capacitor voltages, dc-link voltage with $\theta_d = 0$ {timescale 5ms/div}





(c) (from top) MMC output voltage and current, submodules capacitor voltages, dc-link voltage with $\theta_d = \pi/4N$ {timescale 5ms/div}

Figure 5-18 Boost mode operation M_{dc} =0.6 and M_{ac} = 1.2. (a) $\theta_d = \pi/2N$, (b) $\theta_d = 0$, (c) $\theta_d = \pi/4N$

Therefore, for variable dc-link voltage, the new suggested displacement angle improves the harmonics performance in both sides, this will lead to less filter requirement in both sides of the FBMMC.

5.9 Summary

In this chapter the effective switching frequency at the dc-terminal of the FBMMC phases have been analyzed by using the well-known approach of double Fourier series analysis expansion in two variables. The analysis shows that when the product of NM_{dc} is integer, a suitable selection of θ_d eliminates not only the odd harmonic groups of the carrier but also the even groups of the carrier. This means that the filter in the dc-link voltage is no longer required. when the product of $NM_{dc} = fraction$, the lowest harmonics group in the dc-terminal of the FBMMC phases is still found at first carrier group m=1, in other words at $2Nf_c$. However, θ_d can be used to achieve significant harmonic minimization.

Moreover, in this chapter the effective switching frequency at the ac side of the FBMMC is also analyzed. When the product of NM_{dc} is integer, selecting the displacement angle to eliminate the high-frequency ripples in ac side of the FBMMC only eliminate the odd groups of the carrier. This means the ac side may still needs a filter for the even groups of the carrier. when the product of $NM_{dc} = fraction$, the lowest harmonics group in the ac side of the FBMMC phases still found at first carrier group m=1. However, θ_d can be used to achieve significant harmonic minimization.

The developed analytical model revealed that selecting the displacement angle to achieve the least switching frequency ripples at the dc-terminal of the FBMMC results in the greatest switching frequency ripples at the ac side of the FBMMC and vice versa. Consequently, and under changeable dc-link voltage, a new displacement angle is proposed to accomplish up to a 30% reduction for both sides of the FBMMC simultaneously.

Chapter 6: CONCLUSIONS AND FUTURE WORK

6.1 Overall conclusions and summary

Chapter 1 of this thesis provides an adequate historical background, recent developments, and trends of WECS. Today, the conventional two-level voltage source converter is the technology that is utilised by the vast majority of wind turbine manufacturers, where the electrical drive train operates at low-voltage [3] [112]. Even though two-level voltage source converter technology is well-developed, it has drawbacks such high switching frequencies, low overall efficiency, and the need for bulky and large filters in generator side, dc-link side, and grid side [3].

There has been a significant increase in the size and power of turbines in response to the increased demand for wind energy conversion systems over the past decade, with several companies now providing 10 to 14MW wind turbine alternatives. Therefore, in modern high-power WECS, the transition to a multilevel converter topology is necessary to achieve high efficiency, fewer filter components, increased reliability, and excellent power quality.

A compact system with low size, weight, and cost that is suitable for high-power wind turbine applications is proposed in this thesis. Here, the cheapest and most reliable rectifier type is used, which is the three-phase 6-pulse diode bridge rectifier. This thesis shows that the inevitable drawbacks associated with 6-pulse diode bridge rectifiers, such as unregulated dc-link voltage and large ripple in the dc-link, can be overcomed by using the FBMMC as an inverter without passive components in the dc-link. This is because the FBMMC can work as a boost converter and large dc-link filter by itself.

As experimental validation is an important part of any research project, **chapter 2** explains the construction and design of the experimental prototype. The main parts of the experimental prototype are a generator, a rectifier, a three-phase FBMMC, a resistive load, and an OPAL-RT controller. An adequate explanation for each of them is provided. The three-phase FBMMC is built with two SMs per arm. Every FBMMC SM is custom designed, with an integrated gate driver and an IPM. The IPM has six IGBTs; four of them are used with electrolytic capacitors to form the FBSM. The PCB is also integrated with a deadtime circuit and an overcurrent protection circuit. Finally, the different interface circuits, signal conditioning circuits, sensor circuits, and OPAL-RT as a controller are also described briefly. This chapter is brought in at an early stage to prevent unnecessary redundancy.

An in-depth explanation of the proposed system's core elements is provided in **chapter 3.** The structure, operation, and analysis of the output voltage of the six and twelve pulse rectifiers are presented. The necessary details about the FBMMC structure and operation are provided. The proposed system's characteristics, mathematical modelling, control, simulation, and experiment results are given. The simulation and experiment results confirm that the FBMMC can operate as a dc filter by removing ripples from the dc-link current and generator current. Additionally, the FBMMC's boosting ability has been confirmed. Consequently, the suggested system can assure proper operation without the need for passive components in the dc-link voltage, resulting in a low cost and a high degree of reliability.

Chapter 4 provides a new steady-state analytical model for low-frequency harmonics of the proposed system. The analytical model gives an excellent understanding for the system electrical quantities with variant and non-ideal dc-link. Moreover, this chapter investigates the influence of dc-link ripple, boost mode operation on the FBMMC arm inductance. The conventional design of arm inductance is limited to a pure dc voltage at the dc terminals of the FBMMC and the operation in buck mode. This chapter investigation shows that the selection of the arm inductance is significantly influenced by boost mode operation of the FBMMC. For instance, the arm inductance value needs to be increased almost 60% of its original value when the FBMMC operates in maximum boost mode to avoid the resonance inductance. Moreover, with considering the current ripple in the dc-link, the arm inductance needs to be increased furthermore. Therefore, when designing the arm inductance of the FBMMC, it is crucial to account for boost mode operation and dc-link ripple. The effect of the dc-link ripple on the arm inductance design can be avoided by using twelve pulse rectifiers or six pulse rectifiers connecting to PMSG with $17Hz$ as minimum frequency.

The analytical model also reveals the actual input impedance of the FBMMC, Z_{MMC}, i.e., the impedance of the MMC seen from the dc-link terminals. The dc-link inductor can be easily designed to avoid a discontinues mode in the dc-link and by that adding an extra layer for safe and proper operation if needed. This chapter also develops an equivalent circuit for the proposed system in order to facilitate a clearer, simpler, and more comprehensive understanding of the proposed system.

Chapter 5 develops an analytical solution to the high-frequency harmonics spectrum of the dc-link voltage of the FBMMC under both boost and buck operation. This analytical solution shows the influence of the carrier displacement angle between the upper and lower arms in the dc-link switching-ripple. The analysis shows that under the product of NM_{dc} is integer, a suitable selection of the carrier displacement angle eliminates not only the odd harmonic groups of the carrier but also the even groups of the carrier. This means that the filter in the dc-link voltage is no longer required. Under the product of $NM_{dc} = fraction$, the lowest harmonics group in the dc-terminal of the FBMMC phases is still found at first carrier group m=1, in other words at $2Nf_c$. However, the carrier displacement angle can be used to achieve significant harmonic minimization. The analytical solution that covers the high-frequency harmonic spectrum of the ac side voltage of the FBMMC is also studied. The developed analytical model revealed that selecting the displacement angle to achieve the least switching frequency ripple at the dc-terminal of the FBMMC results in the greatest switching frequency ripple at the ac side of the FBMMC and vice versa.

From that and under variable dc-link voltage a new optimal displacement angle is proposed to achieve up to 30% reduction for both sides of the FBMMC.

6.2 Contributions

- For WECS, a compact system is proposed that uses a three-phase diode bridge rectifier, which is the cheapest and most reliable type of rectifier, and connects to FBMMC as an inverter with no passive components in the dc-link.
- To totally compensate for the lack of dc-link passive components, an improved control approach for the FBMMC's circulating current suppression is proposed.
- A new steady-state analytical mode for low-frequency harmonics of the proposed system is provided.
    - The analytical mode shows that the boost mode operation has a significant impact on arm inductance design, even under ideal dc-link voltage (ripple-free).
    - It also shows that the dc-link ripple creates new resonance inductance, which also needs to be considered when designing the arm inductance.

    - It also reveals the actual input impedance of the FBMMC, Z_{MMC}, and thus The FBMMC can be represented as a single impedance against any ripple in the dc-link.
- An analytical solution to the high-frequency harmonics spectrum of the dc-link voltage of the FBMMC under both boost and buck operation is developed.
    - It shows that a suitable selection of the carrier displacement angle can completely or significantly reduce the high-frequency harmonics spectrum of the dc-link voltage.
    - It reveals that selecting the displacement angle to achieve the least switching frequency ripple at the dc-terminal of the FBMMC results in the greatest switching frequency ripple at the ac side of the FBMMC and vice versa. Therefore, a novel displacement angle is proposed in order to simultaneously accomplish a good reduction on both sides.

6.3 Future work

More future work for this proposed system may be worth considering. These are summarised as follows:

- By taking into account the control components in the modulation index, the steady-state analytical mode for low-frequency harmonics of the proposed system can be improved. Through this, the effect of removing the dc-link LC filter on the maximum peak value of the modulation signal M_{pk} can be revealed. Thus, the inductor in the dc-link can be designed not only to avoid the DCM operation but also to enhance the MMC device utilisation factor.

- Instead of using the 12-pulse rectifier with 6-phase generator or a transformer to enhance the harmonic features in the phase current of the generator, an active filter may be considered. Then, the effect of that on the cost and size of the system can be looked into and compared to the 12-pulse rectifier solution that was suggested.
- Dynamic and sensitivity/stability analysis of the proposed resonant PI controllers (of CCS) under realistic wind generator speed variations, including a PLL control loop to extract the generator speed, together with LUT for PI+R controllers' parameters selection are required to guarantee/propose an optimal and robust design methodology of the proposed system control strategy.
- The analysis of PMSG's performance in the proposed WECS structure, such as torque ripple and efficiency, under harmonic distortion introduced by the PGSC, and comparison of the overall system efficiency and levelized cost of energy, including the power electronics and the machine.

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