Advanced Power Converters for Flexible AC Transmission Systems

By

XUEJIAO PAN

Supervisor

DR LI ZHANG
DR BENJAMIN CHONG
PROFESSOR KANG LI

School of Electronic & Electrical Engineering
Faculty of Engineering
UNIVERSITY OF LEEDS

Submitted in accordance with the requirements for the degree of Doctor of Philosophy

FEBRAURY 2023

AUTHOR'S DECLARATION

The candidate confirms that the work in this dissertation was carried out in accordance with the requirements of the University's Regulations and Code of Practice for Research Degree Programmes and that it has not been submitted for any other academic award. Except where indicated by specific reference in the text, the work is the candidate's own work. Work done in collaboration with, or with the assistance of, others, is indicated as such. Any views expressed in the dissertation are those of the author.

The candidate's publications (including submitted material which is under review):

1.X. Pan, L. Zhang, Y. Li, K. Li and H. Huang, "Modulated Model Predictive Control With Branch and Band Scheme for Unbalanced Load Compensation by MMCC-STATCOM," in IEEE Transactions on Power Electronics, vol. 37, no. 8, pp. 8948-8962, Aug. 2022, doi: 10.1109/TPEL.2022.3152407.

2.X. Pan, L. Zhang and H. Huang, "Harmonic Cancellation by Adaptive Notch Filter Based on Discrete Wavelet Packet Transform for an MMCC-STATCOM," in IEEE Transactions on Power Delivery, vol. 37, no. 3, pp. 1834-1844, June 2022, doi: 10.1109/TPWRD.2021.3099201.

3.X. Pan, L. Zhang , "Control of A Transformerless- static synchronous series compensator for Unbalance Voltage Compensation," in IEEE Transactions on Power Delivery(submitted)

4.X. Pan, L. Zhang and Y. Li, "Modulated Model Predictive Control with Common Voltage Injection for MMCC-STATCOM Under Unbalanced Load," 2021 IEEE 12th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), 2021, pp. 1-7, doi: 10.1109/PEDG51384.2021.9494216.

5.X. Pan, H. Huang and L. Zhang, "Power Flow Control using a Bidirectional Z-source Inverter–based Static Synchronous Series Compensator," 2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe), 2020, pp. P.1-P.10, doi: 10.23919/EPE 20ECCE Europe43536.2020.9215650.

6.L. Zhang, Y. Shi, X. Pan and K. Li, "Analysis of Harmonic Amplification in AC Traction Systems Using LCL Filter with Active Damping," The 10th International Conference on Power Electronics, Machines and Drives (PEMD 2020), 2020, pp. 1013-1018

For the former five papers, they are entirely attributed to Xuejiao Pan: the introduction section, the novel ideas such as the combination of notch filters and wavelet transform, adjusted branch and bound method, modified model predictive control for transformerless-sssc with LC filter and the topology of parallel-transformerless-sssc.

Dr Li Zhang is the co-author for these five papers. She provided her professional supervision, excellent technical advice, guidance and valuable feedback.

Dr Yongfei Li gave the novel idea about adding zero sequence voltage into model predictive current equation. Dr Han Huang gave the basic principle and information about even and inter harmonics. Professor Kang Li provided proofreading.

For the sixth paper, the novel idea was supplied by Dr Li Zhang. The simulation model and results were coming from Yi Shi. The duty of Xuejiao Pan is to finish the paper and submit it to the conference.

ACKNOWLEDGEMENTS

First of all, I would like to sincerely thank my supervisor, Dr Li Zhang , for constantly giving me encouragement and advice. Dr Li Zhang gave me a lot of help from the initial topic selection, material collection, knowledge preparation and various difficulties encountered in the follow-up experiments. I was deeply moved by her enthusiasm for academics and life which gave me the direction and motivation to persist in completing my Phd study. I would like to show my gratitude to Professor Kang Li and Dr Benjiamin Chong. They also provide many useful knowledge and advice for my Phd work.

To my friends, Chen Xin, Yongfei Li, Peiliang Sun, Mingjia Yin, Yihuan Li, Jialei Su, Jiayang Zhang, Jihai Zhong; In the past four years, I have gained countless happy and precious time with all of you. My special thanks goes to my girlfriend Wei Zuo for her love, understanding and care. It was with her company that I was able to overcome many difficult obstacles especially in the final year of my Phd study.

To my parents, Mr Gongmao Pan and Mrs Hua Jiang, Words cannot express my gratitude to you. Even though my family is not very rich, they sponsored me to realize my dream without any complaints. I can only say that I will use my whole life to repay your kindness.

Abstract

Power systems are undergoing significant changes for two reasons which are the widespread and growing use of power electronic based equipment and the fast penetration of renewable energy sources and distributed generation systems which have unpredictable generating nature. Whilst these are beneficial for meeting the forever increasing power demand and environmental requirement, they bring problems of injecting harmonics into the power lines and proliferating unbalanced current flow. Combining these with the usual issues of power systems such as faults caused by voltage distortion and unbalance, resonances, line impedance mismatch, etc, maintaining high quality power supply to customers can be challenging. Flexible AC Transmission Systems (FACTS) have been applied for reactive power compensation, voltage control and power flow regulations. Recent development also demonstrates the attention of engineers and researchers being moved toward deploying FACTS devices for harmonic cancellation and reactive power compensation under unbalanced grid voltage conditions. Nevertheless, effective control techniques capable to track and eliminate the power line voltage/current distortions and harmonics accurately, in real-time are yet to be developed.

This work investigates advanced harmonic measurement and control techniques for both Static Compensator (STATCOM) and Synchronous Series Compensator (SSSC), to realize high performance harmonic cancellation and unbalanced voltage/current compensation. The converter topologies explored are all based on modular multilevel (voltage/current) types without a transformer. The work has led to the development of a new adoptive harmonic cancellation scheme for Modular Multilevel cascaded converter STATCOMs. This scheme uses the discrete wavelet packet transformation (DWPT) algorithm to identify dominant harmonic elements in the measured non-stationary load current in real-time. To overcome the limitations of DWPT due to the effect of data array boundary, a data expansion technique is proposed. By applying the identified harmonics to update the parameters of a chain of notch-filters, the reference currents are generated for MMCC-STATCOM to inject into the grid thus eliminating the unwanted current elements.

Operating under an unbalanced current, the sub-module capacitor voltages of an MMCC-STATCOM may become unbalanced and hence not able to function. A novel technique to mitigate such a problem is created which relies on injecting a common mode voltage to the phase current models when applying the model predictive control (MPC) method. Not only this approach ensures each modules' capacitor voltages are at the required level, it also extends the unbalanced current compensation range. Meanwhile when implementing MPC, an adjusted branch and bound (B&B) algorithm is proposed to minimize the cost function in order to find the optimal solution. This method has been shown able to produce accurate results whilst giving reduced computational burden compared with traditional methods.

The final contribution in this work lies in the area of SSSC for power flow control. A new SSSC topology – the parallel Transformer-less SSSC is investigated which has the advantages of increased power rating and control capability, fast dynamic response and high efficiency. To suppress the current circulating between parallel converter branches associated with this topology, a novel MPC is proposed for the current control. This inserts a differential current term in the cost function apart from the common reference current tracking terms. This scheme has been validated successfully when two parallel converter branches are used.

TABLE OF CONTENTS

List of Tables

LIST OF FIGURES

FIGURE **Page**

ACRONYMS

FACTS Flexible AC Transmission Technology

DC Direct Current

AC Alternating Current

SVC Static Var Compensator

STATCOM Static Synchronous Compensator

TSC Thyristor Controlled Capacitor Bank

TCR Thyristor Controlled Rreactor Bank

TCSC Thyristor Controlled Series Compensation

SSSC Synchronous Static Series Compensator

TL-SSSC Transformerless-Synchronous Static Series Compensator

UPFC Unified Power Flow Controller

PLL Phase Locked Loop

SRF-PLL Synchronous Rotating Frame-Phase Locked Loop

DDSRF-PLL Decoupled Double Synchronous Reference Frame-Phase Locked Loop

CDSC-PLL Cascaded Delay Signal Cancellation-Phase Locked Loop

MMC Modular Multilevel Converter

SM Sub-module

HB H-bridge Converter

FCC Flying Capacitor Converter

NPC Neutral Point Clamped Converter

THD Total Harmonic Distortion

PI Control Proportional Integral Control

PR Control Proportional Resonant Control

APF Active Power Filter

DB Control Deadbeat Control

MPC Model Predictive Control

FCS-MPC Finite Control Set-Model Predictive Control

CCS-MPC Continuous Control Set-Model Predictive Control

OSS-MPC Optimal Switch States-Model Predictive Control

OVL-MPC Optimal Voltage Level-Model Predictive Control

DWPT Discrete Wavelet Packet Transform

ANF Adaptive Notch Filter

MMCC-STATCOM Modular Multilevel Cascaded Converter based STATCOM

PCC Point of Common Coupling

SRF Synchronous Reference Frame

FFT Fast Fourier Transform

DFT Discrete Fourier Transform

STFT Short Time Fourier Transform

WT Wavelet Transform

CWT Continuous Wavelet Transform

DWT Discrete Wavelet Transform

PWM Pulse Width Modulation

PS-PWM Phase shifted-Pulse Width Modulation

PD-PWM Phase Diposed-Pulse Width Modulation

SVPWM Space Vector Pulse Width Modulation

B&B Branch And Bound Method

VSI Voltage Source Inverter

CSI Current Source Inverter

CMV Common Mode Voltage

IP Interior Point Method

DDSRF Decoupled Double Synchronization Reference Frame

DSP Digital Signal Processor

HIL Hardware In Loop

DG Distributed Generators

DVC Double Vector Controller

HPQC Hybrid Power Quality Conditioner

CHAPTER 1

INTRODUCTION

1.1 Background

Recent decades have seen significant changes in electrical power systems due to an unpresidented rise in power demand, and rapid proliferation of renewable energy sources, and hence the growth of distributed generators and microgrids. These raise challenges to the conventional power networks as their designed generation and transmission capacities may not be able to cope with such changes, hence leading to problems such as overloading transmission lines, instability, and degrading power quality. Furthermore, the adverse effect of the current surge in power electronics application to the network operation cannot be overlooked. For their benefits in the flexibility of voltage/current control and improved energy efficiency, there has been a significant increase in the number of switched-mode power electronic devices connected to utility distribution systems. In addition, the rapid growth in renewable energy sourced power generators will press further demand on power converters. These, however, have brought about

issues of non-sinusoidal current flow within electrical networks which can cause detrimental effects including electro-magnetic interference (EMI), over-loading of conductors/transformer windings and the malfunction of connected equipment. The presence of multiple non-linear loads in combination with the input of power from a host of small, renewable generators will inevitably affect the power quality problems such as voltage fluctuations, and three-phase unbalance.

Taking all above into account, it has been paramount to develop and deploy advanced technologies for managing the voltage and power flow of the network. Since the construction of new power lines is very expensive, any cost effective solutions derived should use the existing lines to their maximum thermal limit to ensure controllable the required import/export power flow from different sources and regions, and prevent circulating power. Ultimately, the techniques employed should be able to mitigate all above stated defects hence improving system power quality and maximizing the capability and efficiency of the distribution network infrastructure.

Flexible AC transmission systems (FACTS) are ideal for meeting the aforementioned requirements. The construction of the latest generation of FACTS devices is based on the use of power semiconductor switching devices with sophisticated configurations to behave as voltage sourced converters. With advanced control schemes, they offer high flexibility voltage and power control, hence very effective in improving the reliability, controllability, operating performance and power quality of transmission and distribution systems.

The two most well-known FACTS devices are the Static Compensator (STATCOM) for reactive power compensation and the Synchronous Series Compensator (SSSC) for line impedance variation. The combination of these two devices forms the Unified Power Flow Controller (UPFC) which aims for simultaneous power flow and bus voltage control. The investigation of these devices for power quality

enhancement and power flow control under balanced voltage/current has been carried out for decades and FACTS devices have been installed in some distribution grids.

However, effective power quality control by FACTS device under the line conditions of voltage and/or current imbalances and harmonic distortions poses challenges. These include requiring fast and accurate data processing techniques to extract the unbalance/harmonic elements from measured power line signals, advanced controllers plus switching schemes for driving the power converters in the FACTS devices. Recently for applications in medium/high power system, transformer-less FACTS devices such as modular-multilevel cascaded converter (MMC) for STATCOM and parallel inverters for transformer-less SSSC are explored. However, they either have the problems of stacked module DC voltages being imbalanced or current circulating between the inverter cells causing extra power losses. These problems may exist in normal balanced operation conditions, and exacerbate when facing unbalanced/distorted lines. Research in these areas is active [1]–[5], but novel effective schemes are yet to be developed. This PhD work sets out to address all these challenges.

1.2 Literature Review

1.2.1 Facts Devices

To address the above stated challenges, knowledge and understanding of FACTS devices are required, covering their types, structures and topologies, operation features, control schemes and up-to-date development. A detailed literature review is thus given below. Initially, power electronics were used in DC transmission systems to achieve fast power regulation. The technology has yielded remarkable results. Therefore, researchers want to apply it to AC transmission, so as to increase

the safety margin and reduce the transmission cost. Hence, FACTS technology has emerged which can be classified into three types: parallel, series and integrated devices. According to the different connection modes between FACTS devices and transmission lines, they are also divided into the transformer and transformerless modes.

1.2.1.1 Shunt Compensator

FACTS devices connected in parallel with transmission lines include the SVC (Static Var Compensator) and STATCOM, which are mainly used for voltage control and reactive power control.

SVC refers to a reactive power compensation system composed of a fixed capacitor bank, a thyristor controlled capacitor bank (TSC) and a reactor bank (TCR) [6]–[8]. By adjusting the TCR and TSC, the reactive output of the entire device is continuously changed, the voltage is kept within a certain range statically and dynamically, and the stability of the system is improved.

The conventional circuit of a STATCOM (Fig.1.2 (a)) is principally composed of three phase DC-AC inverter with a DC capacitor, a step down transformer and low-pass filters [9], [10]. It is a reactive power compensation system completely different from the traditional SVC principle. Instead of using conventional capacitors and reactors to achieve reactive power compensation, it uses a three phase inverter to compensate reactive power. The aim of the step-down transformer is to reduce the system voltage vs from high/medium level to low level which is slightly lower than the DC capacitor voltage value. Therefore, through three phase inverter, STATCOM output voltage v_C can be higher or lower than step-down sending-end voltage so that compensation current i_C can realize two-way flow.

Recent development has seen modular multilevel cascaded converters-based STATCOM (MMCC-STATCOM) as shown in Fig.1.2 (b). This topology has multiple

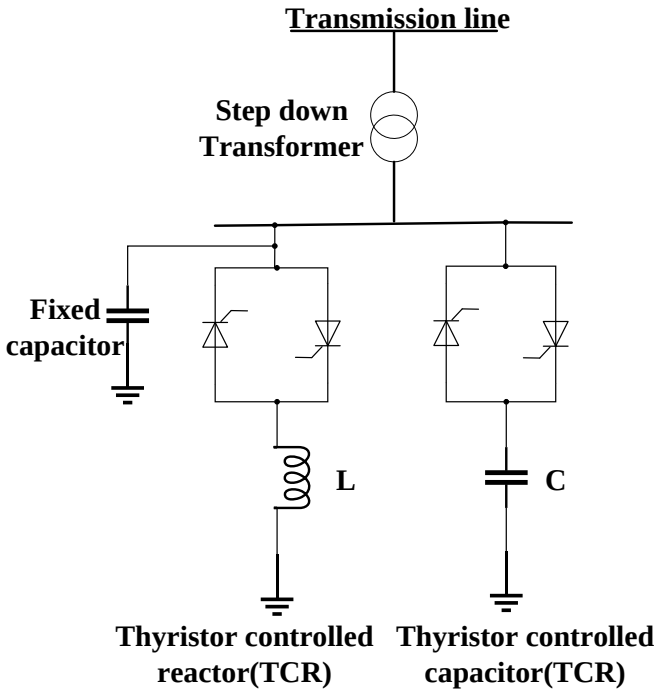

Figure 1.1: Static VAR Compensator

serially connected converter modules per phase. In Star connection, one end of a phase chain is connected to the transmission line via an R-L filter, while the other end is connected with the other two phases forming a neutral point N. With this modular structure, the MMCC can reach required voltage levels without step-up transformers, also it offers the benefits of scalability, high fault tolerance and good waveform quality at the low switching frequency.

The equivalent circuit of STATCOM is shown in Fig.1.3. The three-phase AC output voltage v_C from the inverter is synchronized with the system voltage v_s at the point of common coupling (PCC) which is set as the reference voltage, v_{s0} is the voltage generated from the grid side. Reactive power is adjusted by controlling i_C which can be calculated by (1.1).

$$i_C = \frac{v_S - v_C}{j\omega L} \tag{1.1}$$

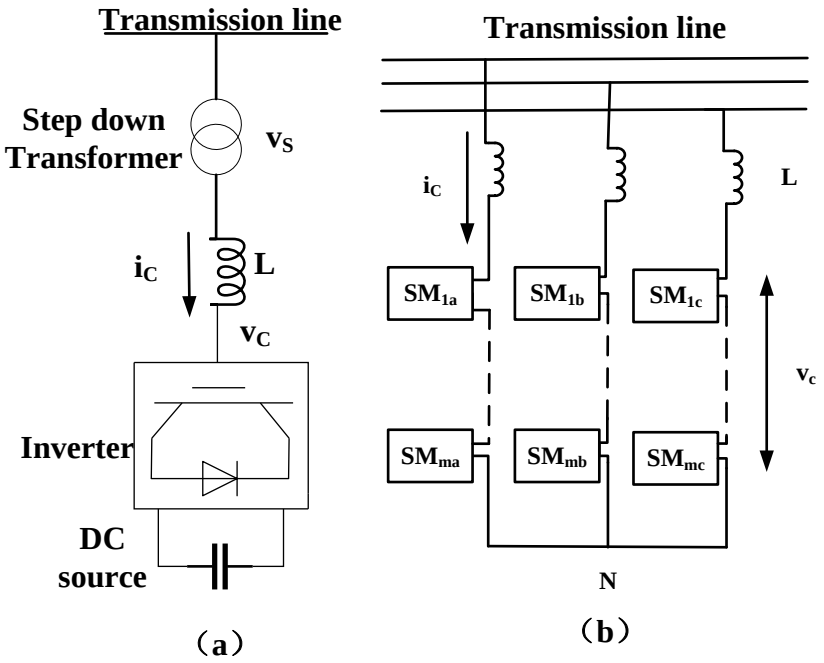

Figure 1.2: Static synchronous compensator (a)conventional STATCOM (b)MMCC-STATCOM

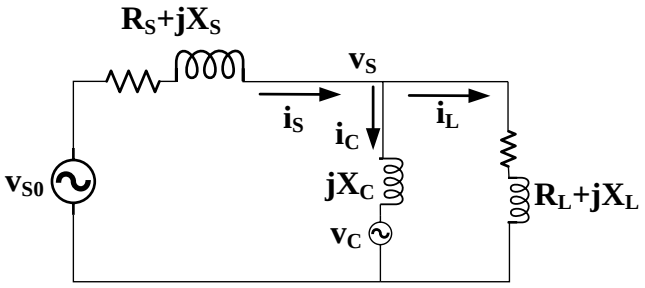

Figure 1.3: The equivalent circuit of STATCOM

The reactive power output by STATCOM can be expressed as (1.2).

$$Q = Im(S) = Im(v_C * i_C) = Im(v_C * \frac{v_S - v_C}{j\omega L}) = v_C * \frac{v_C - v_S}{\omega L} \tag{1.2}$$

When $v_C > v_S$, it outputs capacitive reactive power, $Q > 0$; when $v_C < v_S$, it outputs inductive reactive power,$Q < 0$. The phasor diagrams are shown in Fig.1.4. Therefore, the device's reactive power is adjusted by its compensated current i_C. It

has no impact on the response at start-up, a large continuous adjustment range, fast response speed, and low loss.

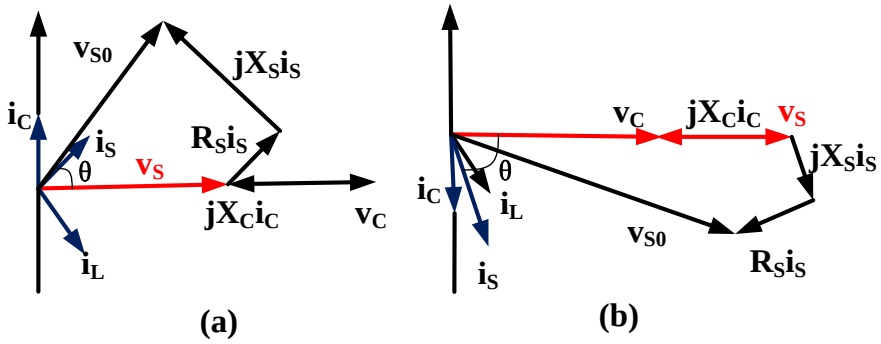

Figure 1.4: (a)Phasor diagrams when $v_C > v_S$ (b) phasor diagrams when $v_C < v_S$

1.2.1.2 Series Compensator

Series FACTS includes Thyristor Controllable Series Compensation (TCSC) and GTO-based Synchronous Static Series Compensator (SSSC). They are mainly used for active power flow control for transmission lines, system transient stability and suppression of system power oscillations.

TCSC (Fig. 1.5) usually refers to a series reactive power compensation system consisting of a thyristor-controlled shunt reactor and a series capacitor bank. By changing the firing angle of the thyristor, the shunt reactor current is adjusted to make the equivalent impedance of the series compensator change continuously, smoothly and rapidly, so the TCSC can be equivalent to a continuously variable capacitor. Under a given voltage and phase angle across the line, fast and continuous control of the power from the transmission line can be achieved to adapt to dynamic interference, and to improve the transient stability limit of the system [11].

SSSC (Fig. 1.6 (a)) refers to a series compensator including a three phase inverter with a DC element which can be a DC capacitor, energy storage or renewable

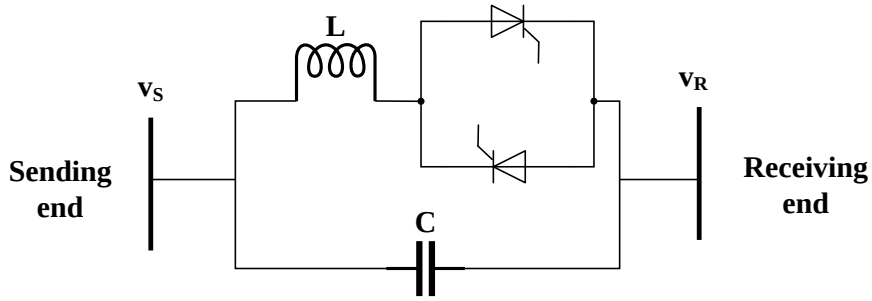

Figure 1.5: Thyristor Controlled series capacitor

energy source. Its basic structure is similar to the STATCOM, except that the device is connected in series with the transmission line through a transformer. The SSSC can be equivalent to a voltage source. The configuration is shown in Fig.1.6 [12]–[14].

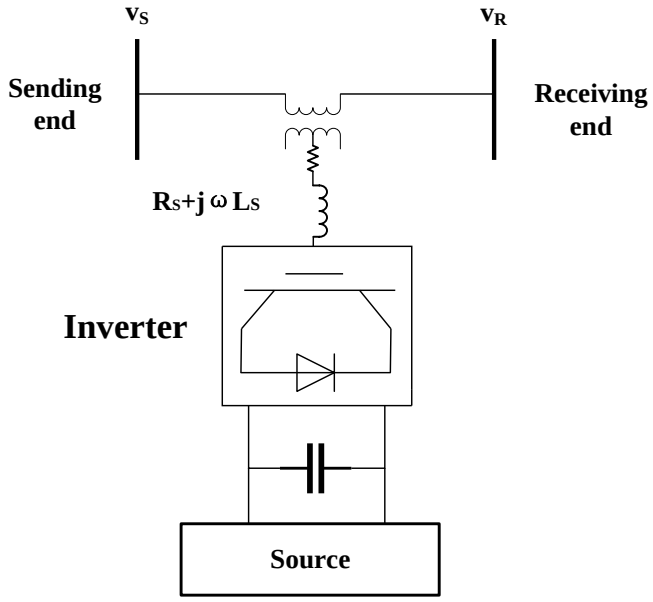

Figure 1.6: The configuration of Static synchronous series compensator

According to Fig.1.7 which is the equivalent circuit of SSSC, considering the sending end voltage v_S as the reference, the transmission line current equation

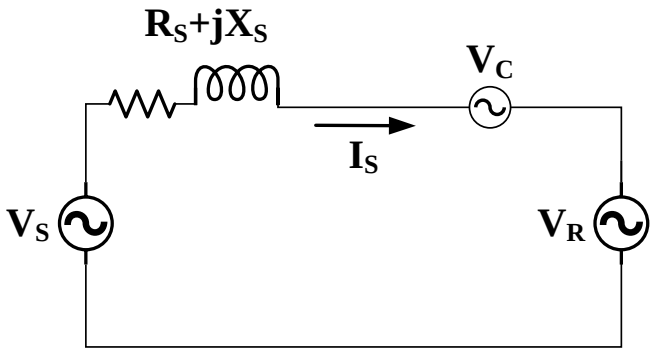

Figure 1.7: The equivalent circuit of Static synchronous series compensator

can be shown as:

$$i_C = \frac{v_S - v_R - v_C}{R_S + jX_S} \tag{1.3}$$

The phasor diagram of SSSC is shown in Fig.1.8

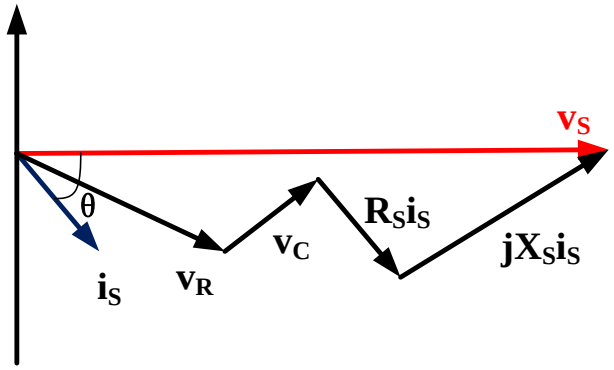

Figure 1.8: The phasor diagram of SSSC

The compensated voltage can be adjusted by controlling the inverter. The amplitude and phase angle are continuously changed based on reference values. Thereby the transmission line current can be maintained at the required level realizing power flow control, the suppression of system power oscillations and the improvement of the system transient stability limit.

1.2.1.3 Integrated Compensator-UPFC

The representative third generation FACTS device is the UPFC (Unified Power Flow Controller) which is the integrated product combining a shunt device STATCOM and a series device SSSC [15]. A typical UPFC topology normally contains two back-to-back connected Voltage-Sourced inverters sharing one DC capacitor. Inverter 1 is connected to the system through transformer T_1 which can be considered to be a STATCOM. It can both realize reactive power compensation and absorb or supply required power to inverter 2 through the DC capacitor. Inverter 2 can be regarded as an SSSC connected in series with the transmission line by a transformer T_2. Hence, inverter 2 can inject a compensation voltage with controllable amplitude and phase angle into the transmission line so that real and reactive power flow control can be realized. Therefore, UPFC is the most effective and powerful device to reduce the burden and increase the capacity of the transmission line. The basic configuration of a UPFC is shown in Fig.1.9 (a) .

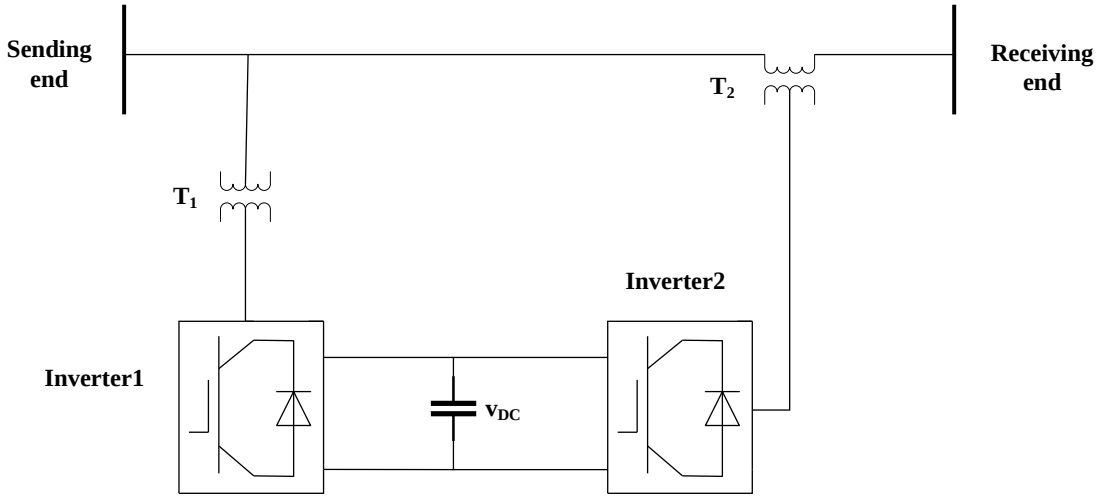

Figure 1.9: The configuration of Unified Power Flow Controller

The phasor diagrams of the Unified Power Flow Controller can be seen in Fig.1.11.

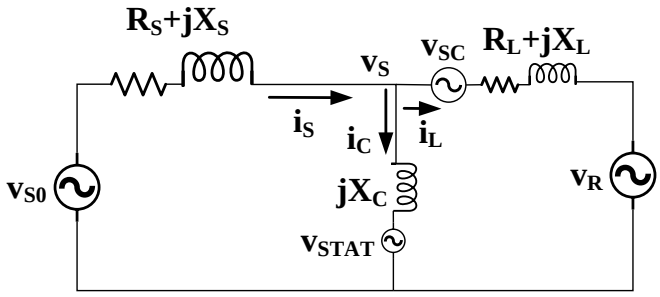

Figure 1.10: The equivalent circuit of Unified Power Flow Controller

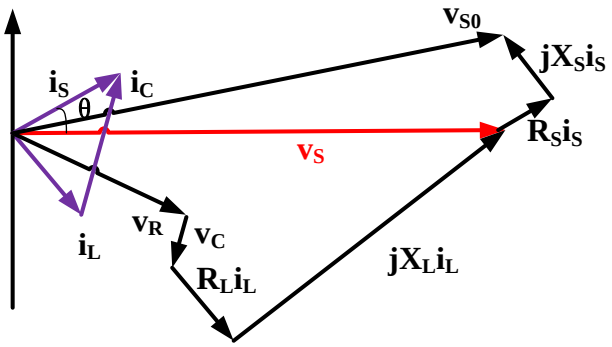

Figure 1.11: The phasor diagram of UPFC

1.2.2 Control Techniques

1.2.2.1 Phase Locked Loop (PLL) Techniques

The Phase Locked Loop Technique has already become an indispensable control part for power electronics converter devices to operate properly in the power system. It is a closed loop frequency and phase synchronization control system realized by the feedback control. Its function is to synchronize the signal output to the circuit with its external reference signal. When the frequency or phase of the output signal changes, the phase-locked loop will detect this change and adjust the output frequency through its internal feedback system. Normally, a PLL includes a phase detector (PD), a loop filter (LF) and a voltage controlled oscillator to form

a feedback loop which can be seen in Fig.1.12.

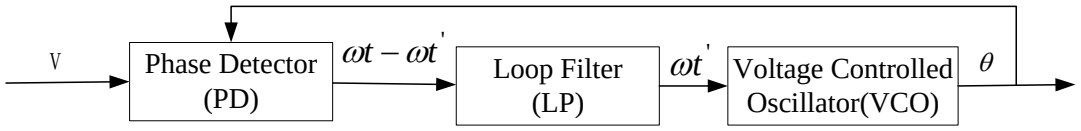

Figure 1.12: The basic block diagram of a PLL

The Phase detector (PD) compares the voltage signal v and the reference signal to obtain the error which's then sent into the Loop filter (LF). The LF removes the high frequency part, and only the DC component of the error $\omega t^{'}$ is preserved. The voltage controlled oscillator then outputs a periodic signal θ controlled by that DC component $\omega t^{'}$. This periodic signal is finally sent back to the phase detector to realize closed-loop control. Nowadays, researchers mainly improve the phase-locked loop technology based on the following points.

1. Track the grid side voltage frequency and phase accurately and quickly.

2. Detect the frequency and phase variation when a frequency oscillation exists in the power system

3. Remain synchronized with the grid side voltage when the grid side voltage has voltage sag and swell, harmonics or even becomes unbalanced.

There are many kinds of PLL technologies. In this subsection, examples including SRF-PLL, DDSRF-PLL and CDSC-PLL are discussed below.

The SPF-PLL is the simplest structure of the various PLL techniques. It usually works well with a pure sinusoidal grid side voltage. The control diagram of the SRF-PLL is shown below.

The grid side voltage v_{abc} first needs to be transformed into the dq rotating reference frame with the Park and Clark transformations. Usually, the phase angle of grid side voltage is set as 0 degree and the fundamental frequency for that is 50 Hz, hence the abc-dq0 transformation formula is shown as (1.4).

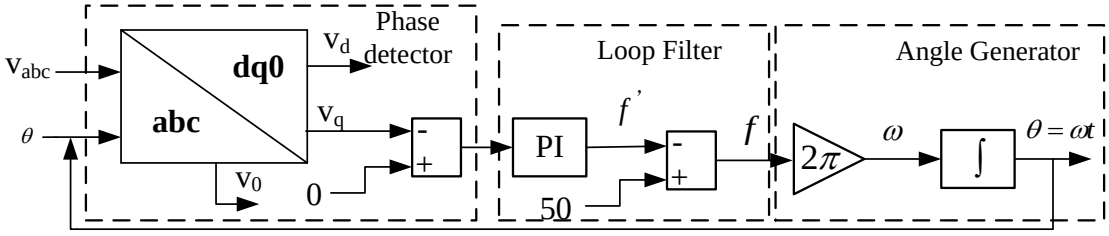

Figure 1.13: The control diagram of SRF-PLL

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = T_{park} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \frac{2}{3} \begin{bmatrix} sin(\theta) & sin(\theta - \frac{2}{3}\pi) & sin(\theta + \frac{2}{3}\pi) \\ cos(\theta) & cos(\theta - \frac{2}{3}\pi) & cos(\theta + \frac{2}{3}\pi) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{1.4}$$

The q component of grid side voltage v_q is chosen as the input signal. As the PLL is to be synchronous to the measured grid voltage, v_q should be 0. Therefore, the reference signal is set as 0. The error sent into the PI controller is then transformed into the frequency variation f'. Finally, through the angle generator, the phase angle θ can be obtained for power electronic converters to generate output voltage synchronized with the grid voltage.

However, if the grid side voltage is unbalanced or has harmonic elements, the q component of grid side voltage v_q contains not only a DC element, but also an AC part including a double frequency harmonic introduced by the negative sequence voltage or other order harmonics caused by the grid side harmonic voltages. This AC element will seriously affect the PLL output signals. To solve this problem, filters can be used such as those shown in Fig.1.14.

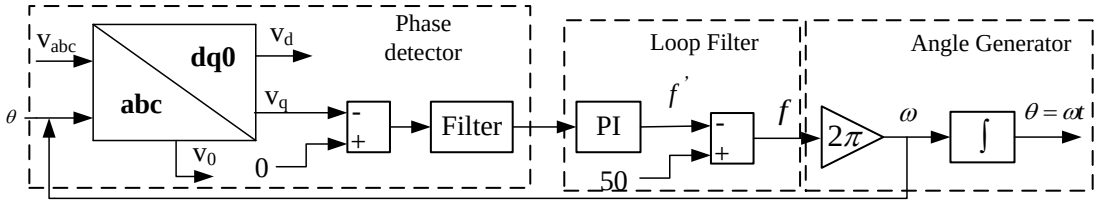

Figure 1.14: The control diagram of SRF-PLL with filter

A suitable filter will result in a more accurate detected phase angle from the PLL. The optional filters are a low pass filter (LPF) [16], a moving average filter (MAF) [17], a resonant filter [18] and a notch filter [16]. However, the use of filters means an extra delay will be introduced caused by these filters which will slow down the transient response capability.

The Decoupled Double Synchronous Reference Frame- Phase Locked Loop (DDSRF-PLL) proposed in reference [19] adopts a double synchronous reference frame which is a positive reference frame rotating with angular velocity ω and a negative reference frame with $-\omega$ respectively. The control diagram is shown in Fig.1.15.

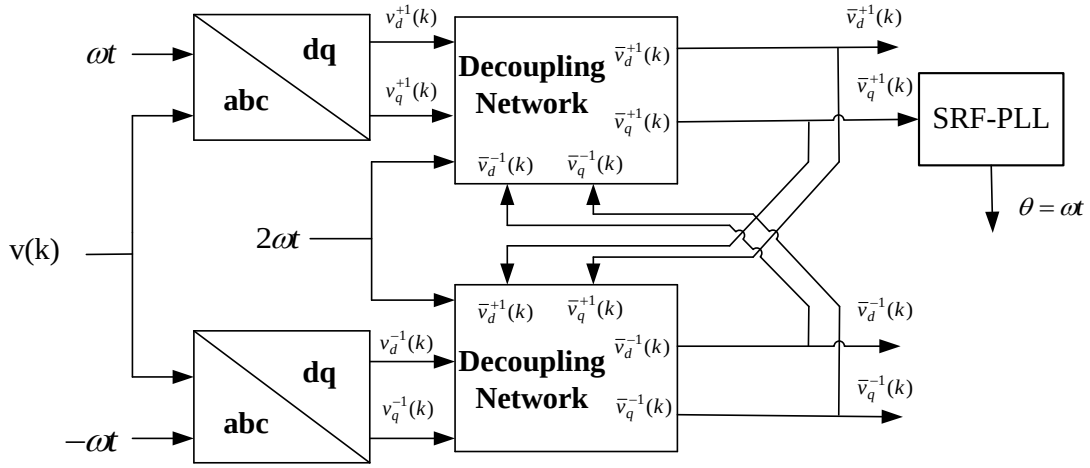

Figure 1.15: The control diagram of the DDSRF-PLL

In Fig.1.15, $v_d^{\pm 1}(k)$ and $v_q^{\pm 1}(k)$ are the positive and negative sequence dq components which contain double sequence oscillation. $\overline{v}_d^{\pm 1}(k)$ and $\overline{v}_q^{\pm 1}(k)$ represent only the DC element for positive and negative sequence dq components. In fact, the DDSRF-PLL is the extension of the SRF-PLL. Only the positive sequence q component $\overline{v}_q^{+1}(k)$ is used in the SRF-PLL to obtain the desired phase angle of the input voltage signal.

The basic principle for the Cascaded Delay Signal Cancellation- Phase Locked

Loop (CDSC-PLL) proposed in reference [20] is to use a delayed signal to cancel specific order harmonics. For example, to eliminate the second order harmonic, the principle is shown in Fig.1.16. The original signal only contains second order frequency component. This signal is delayed by a quarter cycle to get a delayed signal which becomes the anti phase of the original signal. Then combing these two signals, the second order frequency part is canceled. However, if there are other harmonics existing in the original signal, they stack up to double their previous magnitude. Hence, a gain block of 0.5 is necessary to halve the signal. From Fig.1.16, the second order harmonic part can be eliminated in this way.

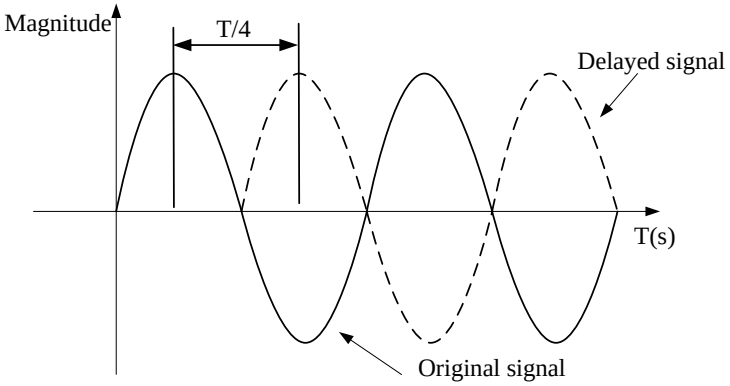

Figure 1.16: Demonstrating how the 2nd harmonic part is cancelled by DSC

The control diagram of the CDSC-PLL is shown in Fig.1.17. It is also an extension of the SRF-PLL. After the Park and Clark transformations, the harmonics existing in the q component of grid side voltage v_q need to be canceled using a cascaded delay signal cancellation method. In Fig.1.17, 1st, 2nd and 3rd order signals are eliminated by delays of the half cycle, quarter cycle and one-sixth cycle respectively. It can be used for unbalanced voltage since the double frequency oscillation can be canceled by the DSC method. However, in real life, the harmonic information can not be known so accurately removing all harmonics becomes a serious problem. If there are harmonics that are not eliminated, the result will

affect the accuracy of the phase angle detected from the PLL technique. In addition, the more frequencies that need to be eliminated means the longer the chain for the cascaded delay signal cancellation method. It also inevitably causes a system delay.

Comparing the three above methods, the SRF-PLL is the most suitable PLL technique used for a balanced and pure sinusoidal grid side voltage. The DDSRF-PLL and CDSC-PLL can be used for an unbalanced situation. However, since the frequency information needs to be removed accurately in time, the CDSC-PLL will obtain an imprecise result. It is worth noting that the DDSRL also uses a low pass filter which may reduce the response speed in the transient part. In this thesis, the SRF-PLL is used in chapter 2 since the grid side voltage is balanced and has no harmonic. The DDSRF-PLL is used in chapters 3, 4 and 5 because of the unbalanced conditions.

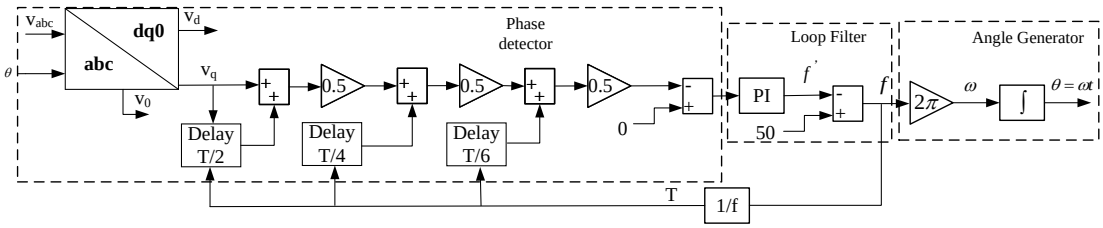

Figure 1.17: The control diagram of the CDSC-PLL

1.2.2.2 Current Control Strategies

Since the fundamental frequency of the supply side voltage is obtained by a phase locked loop (PLL), the next important step is to calculate the desired output voltage of the FACTS device for realizing reactive power compensation and other aims. Current control is a practical way and its essence is to adjust the FACTS device's output voltage through the error between the measured and reference control currents. In the existing current control strategies, two current controllers

which are the proportion integration (PI) controller and proportional resonant (PR) controller are very well-known, easily implemented and often used.

A PI controller is a linear controller whose input is the error of the reference value from the actual measured value. The controller linearly combines this error's proportional and integral to the desired control quantity for the control object. It should be noted that the PI controller mainly performs error-free tracking on the DC quantity, but the current and voltage of most power systems are AC. Hence, before using the PI controller, the AC voltage and current need to be transformed into DC through Park and Clark transformation. The transfer function of the PI controller is expressed as:

$$T_{PI}(s) = K_P + \frac{K_i}{s} \tag{1.5}$$

From (1.5), there are two parameters which are the proportional gain K_p and the integral gain K_i. The values of these two parameters determine the current tracking performance of the PI controller. The bode diagrams are shown in Fig.1.18.

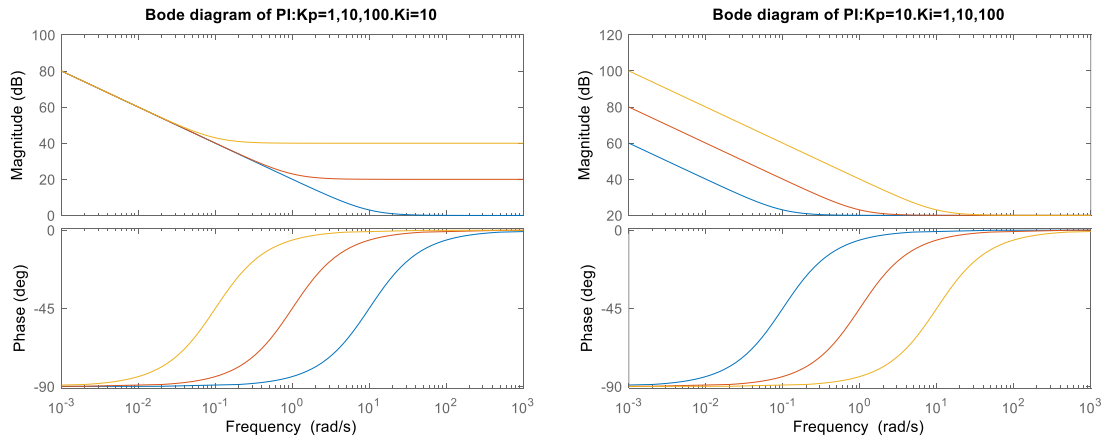

Figure 1.18: Bode diagram of PI controller (a)with different K_p and constant K_i (b) with different K_i and constant K_p

In Fig.1.18 (a), K_i is constant which is 10. The blue line is for K_p=1. The red one

is K_p=10 and the yellow one is for K_p=100. For Fig.1.18 (b), the blue, red and yellow lines are for K_i=1, 10 and 100 respectively. The increase of K_p cause the increased gain margin of the frequency part which is higher than 0.1 rad/s so that control precision is improved and tracking speed is faster. From Fig.1.18 (b), the increase of K_i mainly increases the gain margin of the DC value which can reduce system steady state error. However, if the proportional gain is too large, the stability of the system will be degraded and it will eventually become uncontrollable. An Excessive K_i value will reduce the dynamic response speed. It is clear that a PI controller only has a large gain margin for the low frequency part, especially for that less than 100 rad/s. It means, for tracking waveform whose frequency is equal or larger than 314.15 rad/s (ie 50Hz), the low frequency noise will be amplified leading to poor tracking performance of the PI controller.

The current control diagram for a PI controller is shown in Fig.1.19.

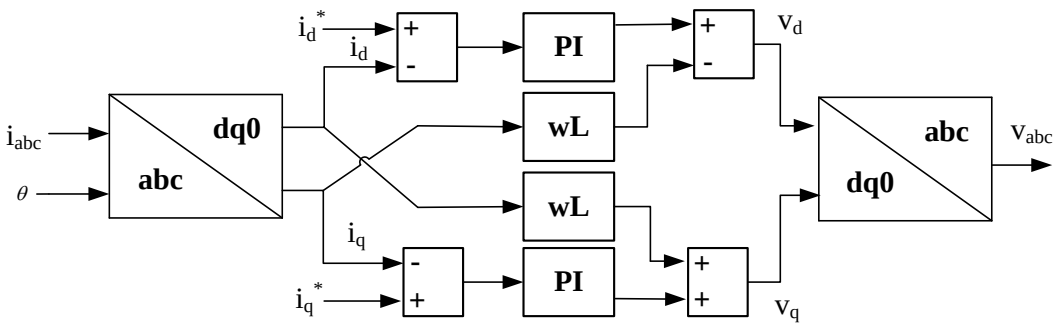

Figure 1.19: The current control diagram for a PI controller

where $\omega L i_d$ and $\omega L i_q$ are the cross coupling terms. The presence of these cross coupling terms is due to the voltage drop formula on the transmission line inductor. The matrix equation for these is shown in (1.6)

$$L\begin{bmatrix} si_d \\ si_q \\ si_0 \end{bmatrix} = L\omega\frac{2}{3}\begin{bmatrix} cos(\theta+\varphi_i) & cos(\theta+\varphi_i-\frac{2}{3}\pi) & cos(\theta+\varphi_i+\frac{2}{3}\pi) \\ -sin(\theta+\varphi_i) & -sin(\theta+\varphi_i-\frac{2}{3}\pi) & -sin(\theta+\varphi_i+\frac{2}{3}\pi) \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$
$$+L\frac{2}{3}\begin{bmatrix} sin(\theta+\varphi_i) & sin(\theta+\varphi_i-\frac{2}{3}\pi) & sin(\theta+\varphi_i+\frac{2}{3}\pi) \\ cos(\theta+\varphi_i) & cos(\theta+\varphi_i-\frac{2}{3}\pi) & cos(\theta+\varphi_i+\frac{2}{3}\pi) \\ \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \end{bmatrix}\begin{bmatrix} si_a \\ si_b \\ si_c \end{bmatrix} = L\omega\begin{bmatrix} i_q \\ -i_d \\ 0 \end{bmatrix} + L\begin{bmatrix} si_d \\ si_q \\ si_0 \end{bmatrix} \tag{1.6}$$

In AC systems, the PI controller does not have a good tracking frequency for AC signals. Hence, PR controller [21], [22] is proposed to eliminate specific frequency components in an AC system. The transfer function of the PR controller is shown as:

$$T_{PR} = K_P + \frac{K_{rh}s}{s^2+\omega_h^2} \tag{1.7}$$

where K_p is the proportional gain and K_{rh} is the resonant gain for the hth order frequency. The ω_h is the cut-off frequency for the hth order harmonic. If the 3rd order harmonic which is about 942.45 rad/s needs to be eliminated, the bode diagram of the PR controller with different K_p values is shown in Fig.1.20 (a), (b) is the bode diagram with different K_{rh} values.

In Fig.1.20 (a) and (b), there is a large gain margin when the cut-off frequency is about 942 rad/s. It proves that the PR controller can have a good tracking performance for 3rd order harmonic. The role of K_p is still to adjust the control precision and tracking speed. The increase of K_r is to raise the gain margin at the cut-off frequency so that it can reduce the steady state error for the cut-off frequency part. The PR controller can be used in an AC system so that the control diagram is shown in Fig.1.21

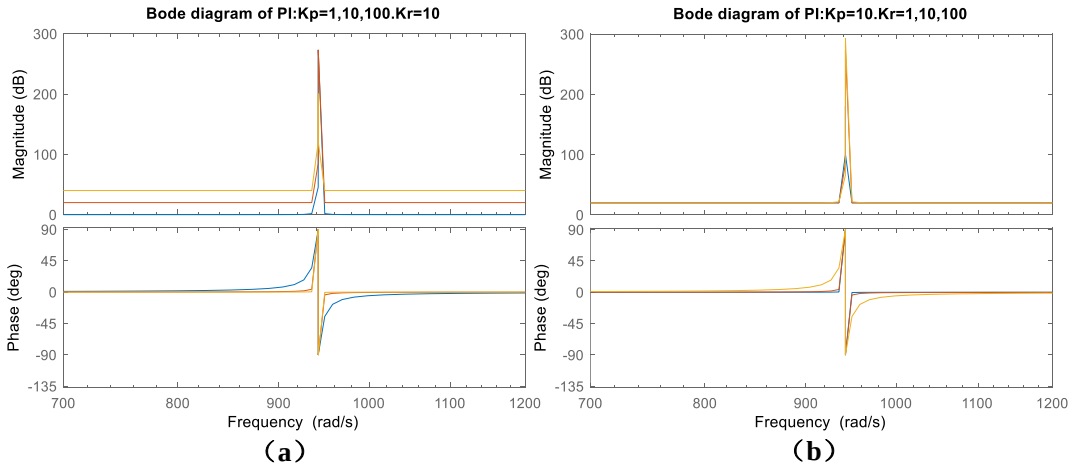

Figure 1.20: Bode diagram of PR controller (a)with different K_p and constant K_r (b) with different K_r and constant K_p

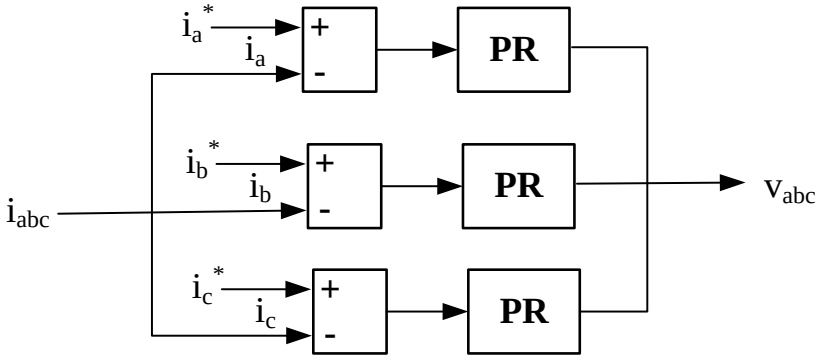

Figure 1.21: The current control diagram by PR controller

1.2.3 Modular Multilevel Converter (MMC)

Traditional FACTS devices basically use a three-phase voltage-sourced inverter, which is composed of multiple semiconductor switches, diodes and a capacitor or DC power source, to control the output voltage's amplitude and phase angle. Therefore, low conversion efficiency, limited voltage withstand capability of a single component, and poor output waveform are inevitable. In order to solve these problems, the MMC was proposed and continues to be developed to this day. Its easy scalability allows multiple sub-modules to be connected to each phase as

required to achieve output voltages up to medium/high voltage levels without the application of a transformer. At the same time, the voltage distributed to each sub-module will not exceed the maximum acceptable voltage range of its components. The superposition of multi-level voltages also improves the output waveform. However, even with these excellent performance features, there are still some non-negligible challenges such as higher cost and the complexity of the controls for MMC topologies.

In this subsection, Several alternative MMC sub-module topologies will be introduced. The well-known sub-module topologies contain a three-level single phase H-bridge converter (HB), a five-level flying capacitor converter (FCC) and a five-level neutral point clamped converter (NPC).

1.2.3.1 Three-level Single Phase H-bridge Converter (HB)

The configuration of three level single phase H bridge converter (HB) is shown in Fig.1.22 (a). Several H bridge converters connected in series in one phase are called a cascaded H bridge (CHB) which was proposed in [23]. For this sub-module, if S_{1a} and S_{4a} are on, S_{2a} and S_{3b} are off, the output voltage of sub-module 1 is $+V_{DC}$. If S_{1a} and S_{4a} are off, S_{2a} and S_{3b} are on, that from sub-module 1 is $-V_{DC}$. Hence, for one three level single phase H bridge converter, the available voltage levels are 0, $+V_{DC}$ and $-V_{DC}$ (Fig.1.22 (b)). If there are M series-connected sub-modules, the voltage level value can reach 2M+1 due to the shared 0 voltage level. Each sub-module has a capacitor that charges or discharges all the time. Hence, the balancing of each capacitor voltage is a major challenge that deserves the attention of researchers

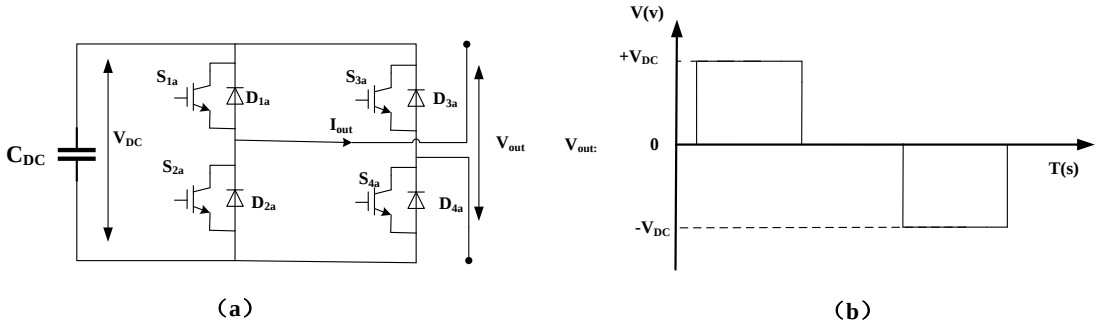

Figure 1.22: (a) Three-level single phase H bridge converter (HB) circuit (b) Voltage level

1.2.3.2 Five-level Flying Capacitor Converter (FCC)

Meynard and Foch proposed the topology of the flying capacitor converter in 1992 [24]. As can be seen in Fig.1.23 (a). 8 switches are divided into four groups (S_{1a}, S_{4a}), (S_{2a},S_{3a}), (S_{1b},S_{4b}) and (S_{2b},S_{3b}). Two switches in each group are complementary. The function of the parallel anti-diode is to prevent the current from flowing back and destroying the electronic components. Each sub-module can output 5-level voltages which are 0, +V_{DC}, -V_{DC}, +2V_{DC}, -2V_{DC} (Fig.1.23 (b)). For M sub-modules in one phase, the total output voltage levels can be 4M+1. The two inner capacitors C_{in1} and C_{in2} which are called the “flying capacitor” are connected parallel with the complementary switch group (S_{2a},S_{3a}) and (S_{2b},S_{3b}) respectively. If the voltage value for the inner capacitors C_{in1} and C_{in2} are set as V_{DC}, the outer capacitor voltage value is twice the inner capacitor voltage value which is $2V_{DC}$.

The combination of the flying capacitor converter switch states is very complex up to 32 groups to generate different output voltage levels. Hence, compared with other sub-module topologies, FCC has more switching options so that it can more evenly distribute the switching pressure to each electronic component.

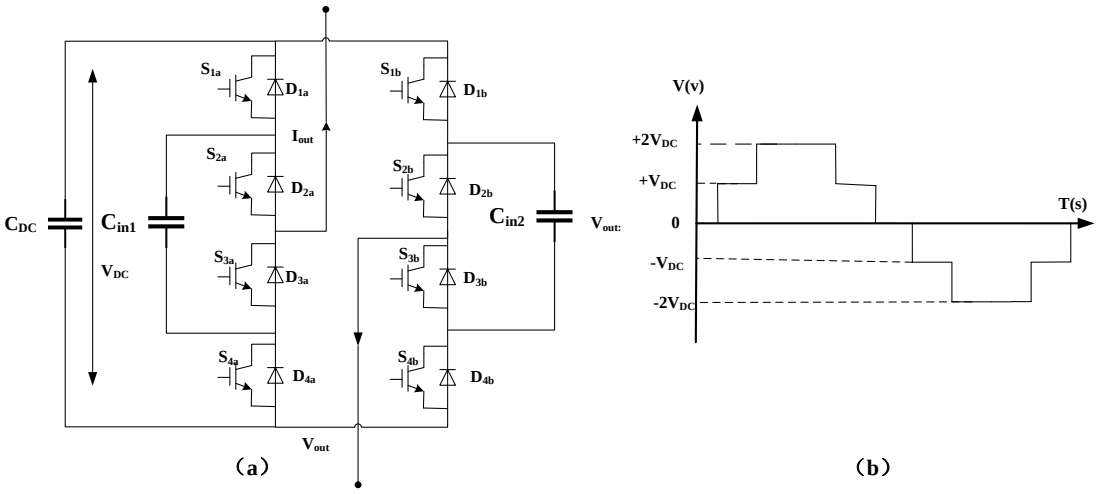

Figure 1.23: (a) Five-level Flying Capacitor Converter (FC) circuit (b) Voltage level

1.2.3.3 Five-level Neutral Point Clamped Converter (NPC)

The application of the five level neutral point clamped converter for the sub-module of the MMC was introduced by Nabea et al [25]. In Fig.1.24 (a), two capacitors are connected in series, and there is a middle point between them called the “neutral point”. Similar to the topology of the flying capacitor converter, there are four complementary switch groups. However, two inner capacitors are replaced by two clamping diodes. These two diodes in each arm clamp their own mid point to the neutral point. This neutral point clamped converter can also generate five voltage levels which have been shown in Fig.1.24 (b). The 4M+1 voltage levels can be output by M sub-modules in one phase. However, the disadvantage of high cost makes this topology less attractive.

1.2.4 Multilevel Pulse Width Modulation Techniques

The pulse width modulation (PWM) techniques are well-known for controlling the switching state of voltage source converters (VSC) to generate desired output waveform equivalent to the desired output waveform. However, to cope with the

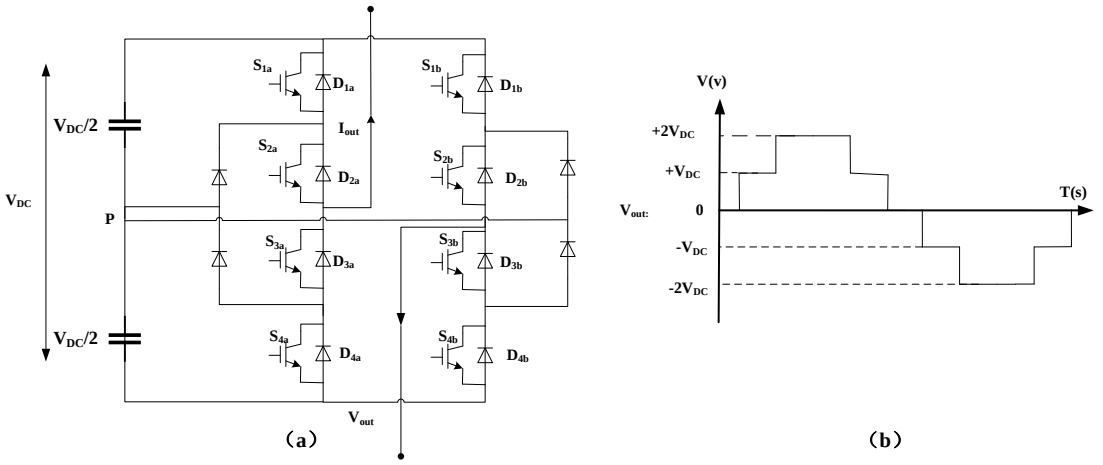

Figure 1.24: (a) Five-level Neutral Point Clamped Converter (NPC) circuit (b) Voltage level

medium/high voltage levels, the FACTS devices usually need to be expanded to modular multilevel cascaded converters based devices. It is impossible for the traditional PWM scheme to generate enough PWM control signals to control each sub-module switch. Therefore, two multilevel pulse width modulation schemes are introduced in this subsection, one is phase shifted-PWM (PS-PWM) and the other is phase dispose-PWM (PD-PWM).

1.2.4.1 Phase Shifted-PWM

The basic operation of this scheme is to use multiple triangular carrier waves to synthesize sinusoidal reference signal [26]. For a (2M+1)-level cascaded H-bridge (CHB) having M sub-modules in a phase chain, each sub-module is modulated by M sets of triangular carrier waves respectively. These carrier waves have the same frequency fc and amplitude -1 to 1, but the phases are sequentially different by a fixed angle, so that each sub-module's output pulses are staggered from each other by a certain angle. The superimposed pulse waves finally form a multi-level ladder wave. The phase displacement angle θ_d between each carrier wave is calculated as 180/M.

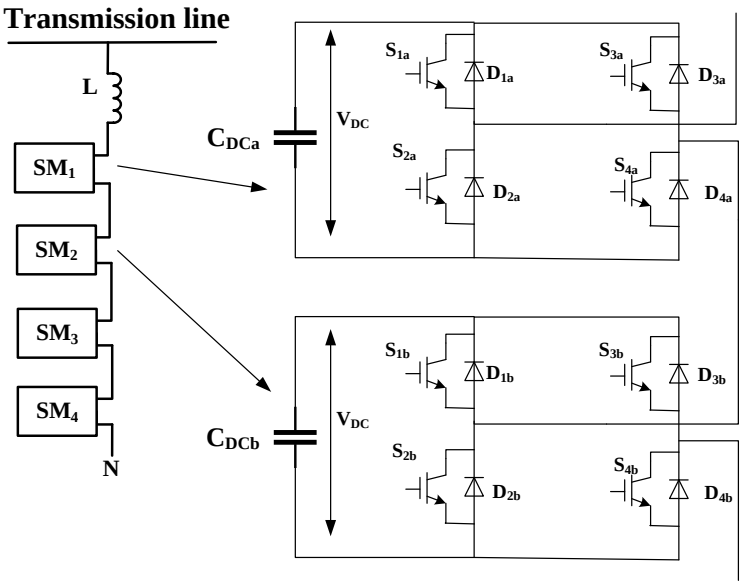

Figure 1.25: The configuration of 9-level CHB

Thus taking a 9-level CHB as an example which is shown in Fig.1.25, the phase displacement angle between each carrier wave is uniformly 45°. Therefore, the four carriers need to be delayed by 0°, 45°, 90°, and 135°, respectively. Hence desired PWM signals can be generated by comparing carrier waves with reference signals. Note there are two anti-phase sinusoidal modulation signals V_{ref} and -V_{ref} which share the same modulation index M_a used as reference. These offer the benefit of reducing output waveform harmonics compared with using a single reference waveform [27]. Fig.1.26 (a) below shows the PS-PWM scheme by using 4 carrier waves to synthesize two sine waves. The resultant four switching pulse trains for four switches, S_{1a},S_{2a},S_{3a},S_{4a} , respectively in one sub-modules are shown in Fig.1.26 (b).

The first carrier wave (wave orange) which is delayed by 0° is to control four switches S_{1a},S_{2a},S_{3a},S_{4a} in the first sub-module SM_1. This carrier wave compares with the reference signal V_{ref} with modulation index M_a to generate complemen-

tary pulse signals for switches S_{1a} and S_{2a} in the left bridge. It also needs to compare with the reference signal -V_{ref} to obtain control signals for S_{3a} and S_{4a} in the right bridge. The other three carrier waves control the rest three sub-modules SM_{2-4} respectively in the same way.

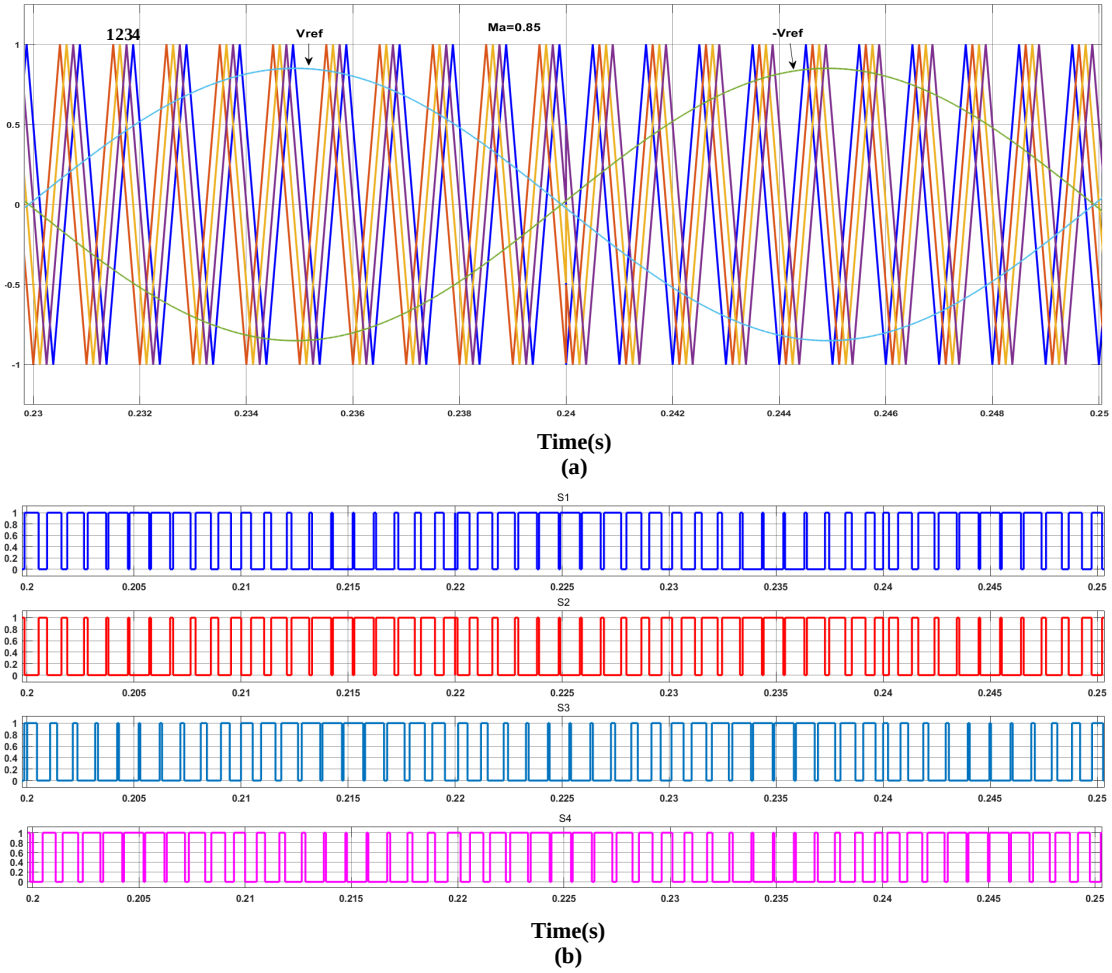

Figure 1.26: PS-PWM (a) Four carrier waves with the reference signals for nine-level CHB and (b) Pulse signals generated for the first sub-module

The advantage of PS-PWM is that the ladder wave formed by the superposition of the output pulse waves of each sub-module can effectively reduce the harmonic elements in the output voltage and current. Hence, the filter requirements can be reduced.

1.2.4.2 Phase Disposed-PWM

The Phase disposed PWM is also called level shift PWM. It consists of several groups of triangle waves with the same phase and frequency symmetrically distributed above and below the zero level [28].

For a 9-level CHB circuit, the number of triangle carriers is 4. Since these four groups of carrier waves are symmetrically distributed in the space of -1 to 1, The amplitudes of the four carriers are -1 to -0.5, -0.5 to 0, 0 to 0.5 and 0.5 to 1, respectively. They are compared with two reference signals V_{ref} and -V_{ref} to control the switch patterns of the sub-modules. Four switches (S_{1a},S_{2a},S_{3a},S_{4a}) in the first sub-module SM_1 are controlled by the PWM control signals generated by the first carrier wave (-1 to -0.5) which is the orange wave and two anti-phase reference signals shown in Fig.1.27. The second carrier wave (-0.5 to 1) is used for controlling the switches in the sub-module SM_2. Another two carrier waves control the remaining two sub-modules SM_3 and SM_4 in one arm.

It is noticeable that in one cycle which is determined by a fundamental frequency of 50Hz, each switch only works in one half cycle and has significantly reduced operations compared with that for PS-PWM so that PD-PWM has less switching loss. However, PD-PWM cannot make the pulse wave overlap. The harmonic distortion performance of PD-PWM will be worse than that of PS-PWM.

1.3 Motivation and Objectives

The motivation of this research is to investigate FACTS devices (main focus is on STATCOM and SSSC) for power flow control, harmonic cancellation and unbalanced voltage/current compensation. The key objectives required to achieve this research motivation are

1. Investigating new harmonic cancellation methods for MMCC-STATCOM

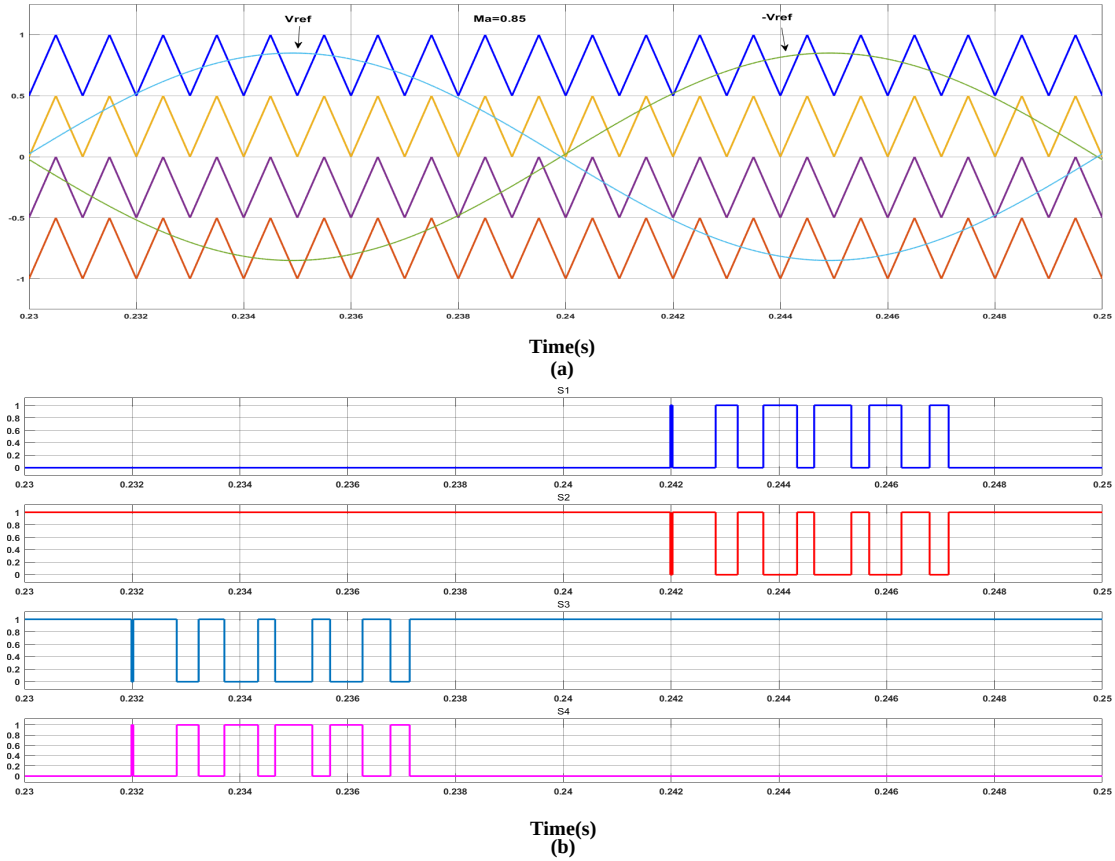

Figure 1.27: PD-PWM (a) Four carrier waves with the reference signals for nine-level CHB and (b) Pulse signals generated for the first sub-module

to eliminate the harmonic components of the load current. The resultant method should be able to identify and extract harmonic elements accurately and in real time.

2. Exploring control techniques for MMCC-STATCOM in order to make it capable to eliminate unbalanced load current hence compensating reactive power as required.

3. Developing optimization algorithms that can be efficient and effective and computationally efficient in minimizing quadratic cost functions with constraints.

4. Investigating control schemes for transformer-less SSSC to realize power flow control which is suitable for balanced and unbalanced situations. Moreover,

with the developed control algorithm, TL-SSSC can protect other system parts when faults happen at different locations in a power system.

5. Proposing a novel topology for transformerless SSSC with a capacitor instead of a DC input source for not only realizing reactive power control and extending the controllable range, but also realizing active power control simultaneously.

6. Developing a novel transformer-less UPFC topology by combining the novel transformer-less-SSSC and MMCC-STATCOM. Validating the feasibility of this new UPFC topology.

1.4 Publications and Thesis Structure

1.4.1 Publications

The materials presented in this thesis are supported by the publications listed below:

1.X. Pan, L. Zhang, Y. Li, K. Li and H. Huang, "Modulated Model Predictive Control With Branch and Band Scheme for Unbalanced Load Compensation by MMCC-STATCOM," in IEEE Transactions on Power Electronics, vol. 37, no. 8, pp. 8948-8962, Aug. 2022, doi: 10.1109/TPEL.2022.3152407.

2.X. Pan, L. Zhang and H. Huang, "Harmonic Cancellation by Adaptive Notch Filter Based on Discrete Wavelet Packet Transform for an MMCC-STATCOM," in IEEE Transactions on Power Delivery, vol. 37, no. 3, pp. 1834-1844, June 2022, doi: 10.1109/TPWRD.2021.3099201.

3.X. Pan, L. Zhang , "Control of A Transformerless- static synchronous series compensator for Unbalance Voltage Compensation," in IEEE Transactions on Power Delivery(submitted)

Other publications which are not used in this thesis:

1.X. Pan, L. Zhang and Y. Li, "Modulated Model Predictive Control with Common Voltage Injection for MMCC-STATCOM Under Unbalanced Load," 2021 IEEE 12th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), 2021, pp. 1-7, doi:10.1109/PEDG51384.2021.9494216.

2.X. Pan, H. Huang and L. Zhang, "Power Flow Control using a Bidirectional Z-source Inverter–based Static Synchronous Series Compensator," 2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe), 2020, pp. P.1-P.10, doi:10.23919/EPE20ECCEEurope43536.2020.9215650.

3.L. Zhang, Y. Shi, X. Pan and K. Li, "Analysis of Harmonic Amplification in AC Traction Systems Using LCL Filter with Active Damping," The 10th International Conference on Power Electronics, Machines and Drives (PEMD 2020), 2020, pp. 1013-1018, doi: 10.1049/icp.2021.0957.

1.4.2 Thesis Structure

Chapter 2: This chapter introduces the problems associated with harmonics, harmonic limits and international standards. The harmonic current suppression devices which are passive and active filters are reviewed in this chapter. The next part is the description of reference signal extraction methods for harmonic problems and wavelet based- harmonic identifying methods. The published paper follows an adaptive harmonic current extraction scheme which is the combination of notch filters and modified discrete wavelet packet transform (DWPT) for the MMCC-STATCOM to generate compensating current to offset harmonic components of load current. The modified DWPT with data expansion technique is for eliminating the impact of boundary effects. The simulation results prove the feasibility of the proposed method for harmonic detection and filtering performance in real time.

Chapter 3: This chapter reviews the problems associated with unbalance, the international identification and standards for unbalance and the reference signal

extraction methods for unbalanced situations. For the MMCC-STATCOM dealing with unbalanced problems, sub-module capacitor voltage balancing is an interesting topic to be solved. This chapter introduces the related methods proposed by other researchers. Moreover, the model predictive control is also reviewed in this chapter. The paper attached in this chapter proposes a novel modulated Model-Predictive Control (MMPC) scheme for MMCC-STATCOM to compensate unbalanced load current and regulate reactive power flow. The common mode voltage is added into the model predictive current equation for extending the compensation range and maintaining sub-modules' capacitor voltages at the required level. The adjusted branch and bound method is proposed for cost function minimization. The experimental results are presented.

Chapter 4: This chapter presents a deadbeat control scheme allowing an LC filtered transformerless SSSC to compensate voltage distortions arising from faults at different locations while maintaining power flow control. The delay compensator incorporated in the control algorithm mitigates the control signal errors arising from the computational latency. Then to prevent the TL-SSSC operating over its current/voltage ratings when mitigating voltage distortion, an analysis of the power controllable ranges for a TL-SSSC under different unbalanced voltage ratios is performed. The experimental results realized by a TI-SDP and a typhoon 604 Hardware-In-Loop (HIL) emulator show that the TL-SSSC can protect other system parts when faults happen at different locations which are the sending end side, the receiving end side and the output terminals of the grid tied converters. In addition, the proposed model predictive control method has a better dynamic response performance compared with traditional unbalance voltage compensation methods.

Chapter 5: This chapter proposes a per phase model predictive control for power flow control of parallel TL-SSSC. The model predictive current equation is

analyzed firstly to form the cost function. To prevent the circulating current in two branches, the circulating current term is added in the cost function equation. Then, the cost function minimization with equal and unequal reference currents are described in the following part. This proposed method can be used for the balanced and unbalanced cases and the only difference between these two cases is the reference current generation. The simulation results show the feasibility of the proposed method in balanced and unbalanced cases. The circulating current can be suppressed with equal reference current and circulating current terms in the cost function. Moreover, the parallel TL-SSSC can protect systems without influencing the unbalanced voltage appearing at the sending end side, the receiving end side or the distributed generators terminals side.

Chapter 6: In this chapter, a critical discussion and conclusion are given and some future plans related to the author's research work are suggested.

Fig. 1.28 shows the contents and organisation of the thesis related with the methods utilised in blue.

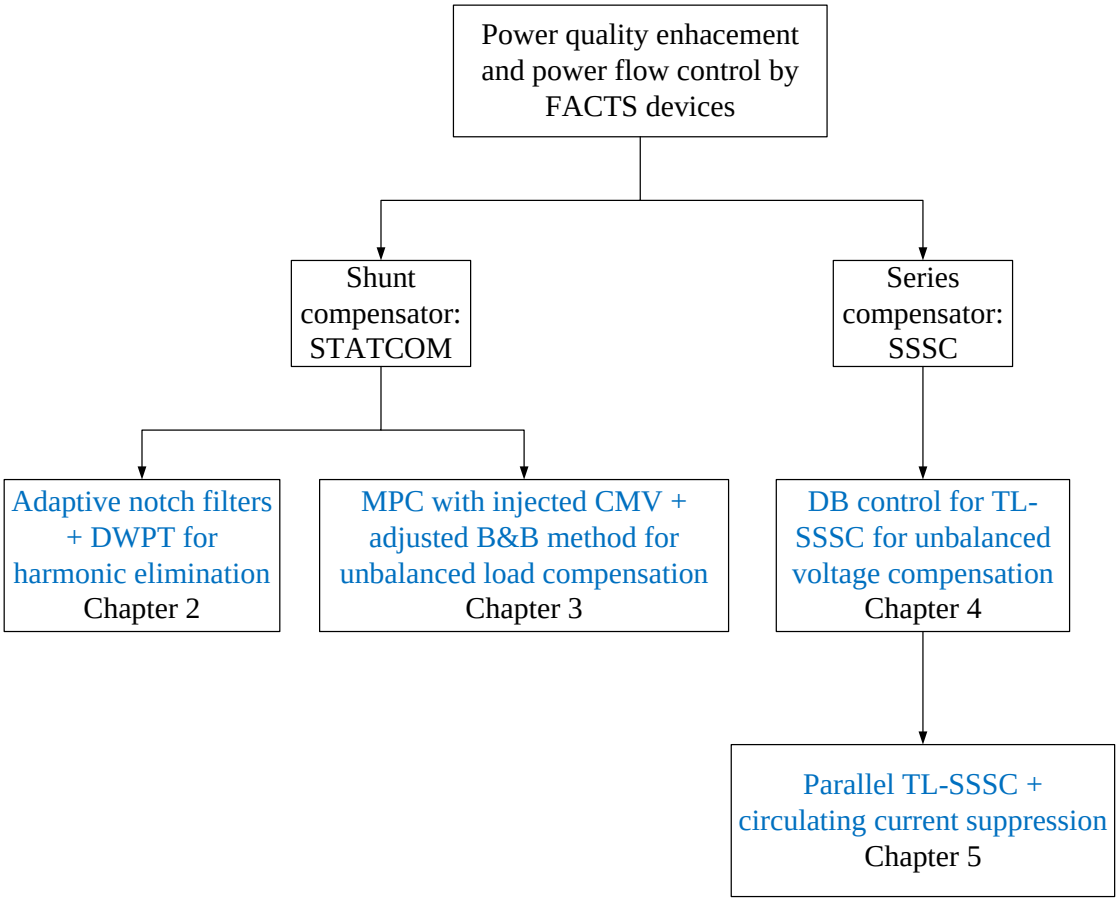

Figure 1.28: Thesis Organisation

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CHAPTER 2

HARMONIC CANCELLATION BY ADAPTIVE NOTCH FILTER BASED ON DISCRETE WAVELET PACKET TRANSFORM

2.1 Introduction

STATCOM [1]–[3], as a well-known effective device for voltage regulation and reactive power compensation, is also highly flexible in harmonic mitigation. Recent research in harmonic current cancellation has resulted in various algorithms and control schemes being developed for STATCOMs to separate the harmonic current components from the fundamental one. With the advances in the STATCOM structure from a two-level three-phase Voltage Source Inverter connected in parallel with the power line via a coupling impedance or a transformer, to the modular multilevel cascaded converters (MMCC) [4] for medium and high voltages - these newly developed harmonic mitigation techniques must be adaptable, robust, and efficient [5]–[8]. Their good performance is essential

in facilitating the applications of the STATCOM of any structure to maintain high-quality power flow control in the power networks [9], [10].

This chapter will present a novel adaptive harmonic current extraction scheme being developed by the author. This scheme uses notch filters combined with a modified discrete wavelet-packet transform (DWPT). The scheme is applied to control an MMCC-STATCOM which cancels the harmonic current on the power line. The result obtained has demonstrated highly desired performance in comparison to some conventional algorithms.

The development of this new scheme stems from various existing harmonic extraction methods, thus this chapter will start by giving a thorough review of the main harmonic mitigation techniques including passive and active filters; reference signal extraction methods using a low/high pass filter or a notch filter. Importantly, various wavelet schemes effective for harmonic identification will be presented. Their basic algorithms, implementation methods, advantages and shortcomings in a practical application will be highlighted.

2.2 Harmonic Issues and International Standard

2.2.1 The Problems Associated with Harmonics

The growing use of the power electronic controlled-equipment, such as uncontrolled rectifiers, grid-tied converters for renewable sourced generators [11], and large traction drives [12], results in a significant level of harmonic current components drawn at the Point of Common Coupling (PCC). Consequently, they cause PCC voltage distortion owing to the flow of harmonic current through the finite line impedance. The voltage and current harmonics degrade the quality of power supplied to customers, the power system operating stability, and the efficiency. The main problems are classified into five aspects as follows:

(1) Harmonics cause additional losses in the public power grid, reducing the efficiencies of power generation, transmission and electrical equipment. Also, high magnitudes of the 3rd order harmonic and its multiples flowing through the neutral line may cause a line overheating or even extreme case of causing a fire.

(2) Harmonics affect the normal operation of various electrical equipment. The influence of harmonics on the motor not only causes additional losses, but also produces mechanical vibration, noise and overvoltage, which will cause severe local overheating of the transformer. Harmonics make capacitors, cables and other equipment overheat, and can cause the insulation to age, shorten life, or even damage it.

(3) Harmonics will cause the local parallel and series resonance in the public power grid, thereby amplifying the harmonics, which greatly increases the harm of the above (1) and (2), and even causes serious accidents.

(4) Harmonics may cause a malfunction of the relay protection and the automatic devices, and impair the accuracy of the electrical measuring instruments.

(5) Harmonics may interfere with adjacent communication systems. It will generate noise and reduce the communication quality. Even under the severe situation, it will lead to the loss of the communication objects and make the communication system unable to work normally.

2.2.2 The International Definition and Standard for Harmonics

The harmonic voltage or the current components have frequencies at the low-order multiples of the line frequency as shown by the Fourier series decomposition of periodic non-sinusoidal waveforms. The level of harmonic distortion is defined by the Total Harmonic Distortion (THD) expressed by (2.1).

$$THD = \frac{\sqrt{Q_2^2 + Q_3^2 + ... + Q_n^2}}{Q_1^2} \tag{2.1}$$

where the Q_1 is the r.m.s (voltage, current and flux) value of the fundamental-frequency element, and the n is the maximum harmonic order measured by the Fourier series decomposition. The $Q_2 \ldots Q_n$ are the r.m.s magnitudes from the harmonic order 2 to n.

It should be noted that the allowable total harmonic distortion level is different according to the different environments and the sensitivity of the equipment used. The allowable THD levels of the international standard for harmonics have been shown in IEC 61000-2-4 proposed in 2002 [13]. This file defines and divides the electromagnetic environment into three classes.

Class 1: The equipment and power supplies used in the laboratories which need to be protected and are sensitive to disturbances.

Class 2: The points connected to the public supply network. The compatibility level of these points is determined by the public network authority.

Class 3: This class is only for the points connected to a network in the industrial environment. The compatibility level is higher than that of class 2.

The allowable level for each harmonic order and the total harmonic distortion levels for the three classes are shown in table 2.1-2.2.

2.3 Harmonic Current Suppression by MMCC-STATCOM

Harmonic mitigation techniques have been actively researched for decades [14], [15]. The simplest ones are the passive power filters ranging from the simple line reactors in series with the supply, to the shunt L-C filters tuned to a particular

Table 2.1: The allowable harmonic levels of the odd harmonics for three classes

Order h	Class 1 $U_h\%$	Class 2 $U_h\%$	Class 3 $U_h\%$
3	3	5	6
5	3	6	8
7	3	5	7
9	0.3	0.4	2
11	3	3.5	5
13	3	3	4.5
15	0.2	0.3	1.75
17	2	2	4

Table 2.2: The allowable THD levels for three classes

	Class 1 %	Class 2 %	Class 3 %
Total harmonic distortion(THD)	5	8	10

harmonic frequency. More complex L-C networks as shown in Fig 2.1 may also be used to form the band-pass and band-stop filters [16], [17]. Such techniques are effective, but present a number of shortcomings. Large and expensive inductive components maybe are necessary to suppress harmonics to an acceptable level, particularly at low harmonic frequencies. Additionally, the passive filters can have a resonance effect with the system impedance, amplifying the harmonic currents and worsening the problem.

A more flexible and effective solution for harmonic current mitigation is achieved through using active power filter (APF) techniques [13], [18]. A STATCOM can function as an APF while it can still control the power factor, thus it is also called an active power conditioner. Its circuit configuration is as shown in Fig.2.2 (a), which uses a power electronic converter and a coupling transformer shunt connected to the power system to inject compensating harmonic currents in a controlled manner. There are other APF devices, such as the SSSC, shown in Fig.2.2 (b), which is connected in series to the power line for mitigating harmonic voltages, and hybrid

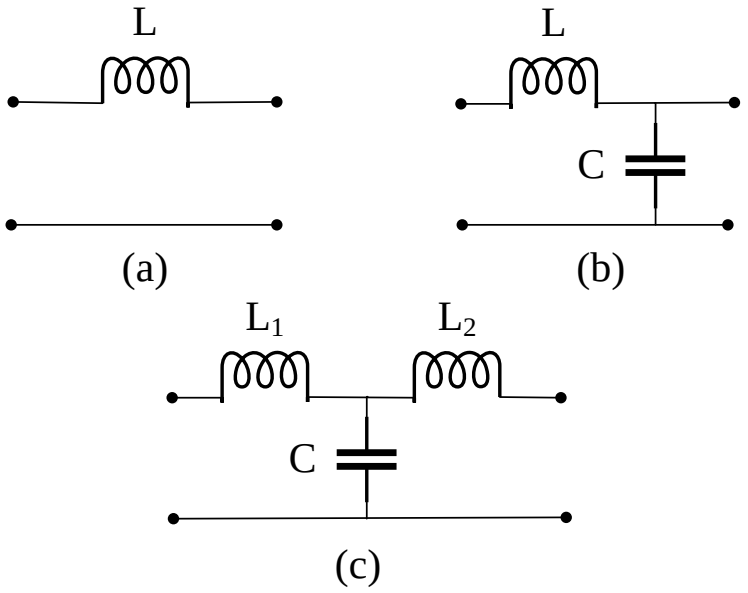


Figure 2.1: The passive power filters (a) L filter (b) LC filter (c) LCL filter

switches are combinations of passive and active power filters (see Fig. 2.2 (c) and (d)).In comparison with their passive counterparts, these APFs are not restricted to compensate the specific harmonic frequencies and offer greater flexibility in situations where the load demand may be unpredictable. Additionally, the overall size and cost may be reduced by employing active techniques, and problems associated with system resonance may be avoided.

Considering the STATCOM-based APF, recent development has seen the MMCC topologies being used which, irrespective of the sub-module types, make the STATCOM easily scalable to higher voltages without requiring a step-up transformer. This structure can also realize a more complex output waveform (corresponding to the line harmonics to be eliminated) using a low switching frequency, giving a lower switching harmonic content and hence a reduced filtering requirement. Moreover, the topology is more fault tolerant, with easier manufacturing and maintenance, lower cost, higher reliability and better efficiency.

Apart from the hardware device, the key feature for any STATCOM to eliminate

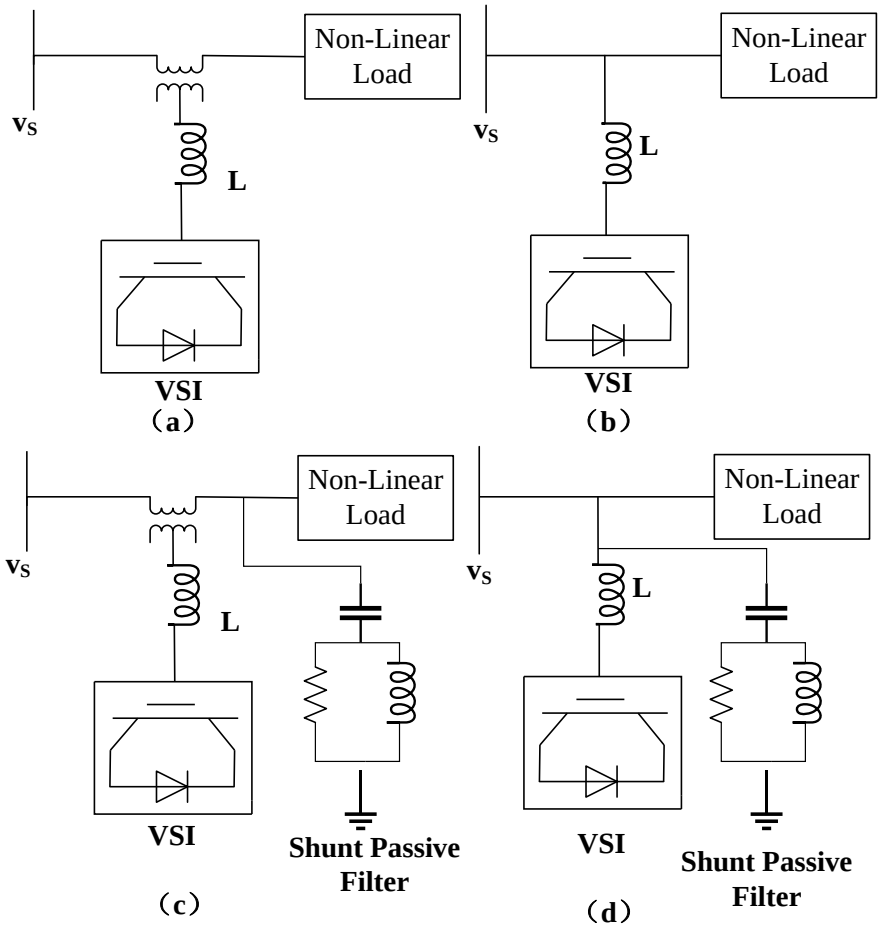


Figure 2.2: The configurations of (a) series APF, (b) shunt APF, Hybrid APF :(c)combination of series APF and shunt passive filter (d) combination of shunt APF and shunt passive filter

harmonic current is its capability in identifying and extracting the harmonic elements in the load current which are often time-varying. The advanced signal processing techniques in both time and frequency domains have been employed and are described in the following.

2.4 Reference Current Extraction Techniques

The key for achieving effective harmonic elimination by an MMCC-STATCOM is to produce a specific current waveform that contains harmonic components presenting on the power line current. Three techniques are commonly used including the Low-pass filter, the High-pass filter and the notch-filter based extraction methods. Recent work shows the wavelet-based techniques which have been explored in this chapter.

2.4.1 Low Pass Filter Based Method

The low-pass filter-based extraction method which is also called the Synchronous Rotating Frame (SRRF) method relies on transforming the measured three-phase currents into a rotating d-q reference frame synchronized with the power line voltages using Park transformation. The Phase angle of the power line voltage with respect to a reference frame should be derived in advance using the well-known Phase Locked Loop (PLL). For an MMCC-STATOM, assuming the load currents are i_{Rm} (m=a,b,c) which are harmonics corrupted, their equivalent d-q elements are firstly derived through Park transformation formulae as shown in (2.2)

$$\begin{bmatrix} i_{Rd} \\ i_{Rq} \\ i_{R0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} sin(\theta+\varphi_{iR}) & sin(\theta+\varphi_{iR}-\frac{2}{3}\pi) & sin(\theta+\varphi_{iR}+\frac{2}{3}\pi) \\ cos(\theta+\varphi_{iR}) & cos(\theta+\varphi_{iR}-\frac{2}{3}\pi) & cos(\theta+\varphi_{iR}+\frac{2}{3}\pi) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_{Ra} \\ i_{Rb} \\ i_{Rc} \end{bmatrix} \tag{2.2}$$

where the θ is the phase angle of the reference voltage obtained through the PLL synchronization scheme and the φ_{iR} is the phase angle between the load current and the power line voltage. The d-q load current elements i_{Rd} and i_{Rq} derived contain a DC element due to the fundamental frequency waveform and a set of (n-1) order harmonics where the n is the highest order harmonic element

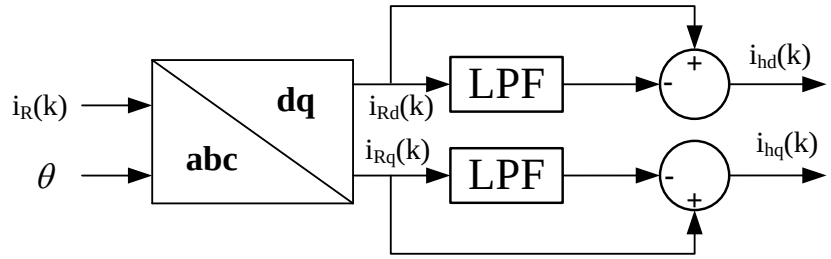


Figure 2.3: The Schematic diagram of the low-pass filter-based extraction method

presenting in the original i_{gm} . The i_{Rd} and the i_{Rq} are then transferred through low-pass filters (LPFs) with a cut–off frequency ω_O to remove the AC components, i.e. the harmonics, from the signals. Thus the resultant signals should ideally be the fundamental element and by subtracting them from the original i_{Rd} and i_{Rq}, the harmonic current elements are extracted. The block diagram shown in Fig.2.3 notes the output i_{hd} and i_{hq} are the d-q currents containing all unwanted harmonics to be eliminated.

The method is simple to be implemented. However, it has two main problems; one is the inaccuracy in extracting harmonic components with low frequencies closer to fundamental. The transfer function of a first-order low-pass filter is shown as:

$$T(s)_{LPF} = \frac{\omega_0}{s+\omega_0} = \frac{1}{\frac{1}{\omega_0}s+1} \tag{2.3}$$

where the ω_0 represents the cut-off frequency. With harmonic frequencies closing to the ω_0, the amplitude attenuation by the LPF is insignificant, hence they cannot be removed. This can be seen in the Bode plot shown in Fig.2.4 where the cut-off frequency of the low pass filter is set as 219.1rad/s. The magnitudes of the harmonics are close to this set value which is about 0dB, hence they are not removed. However, harmonics within a frequency band from 100Hz to 300Hz should be removed but can not be filtered by an LPF since the attenuation magnitudes are

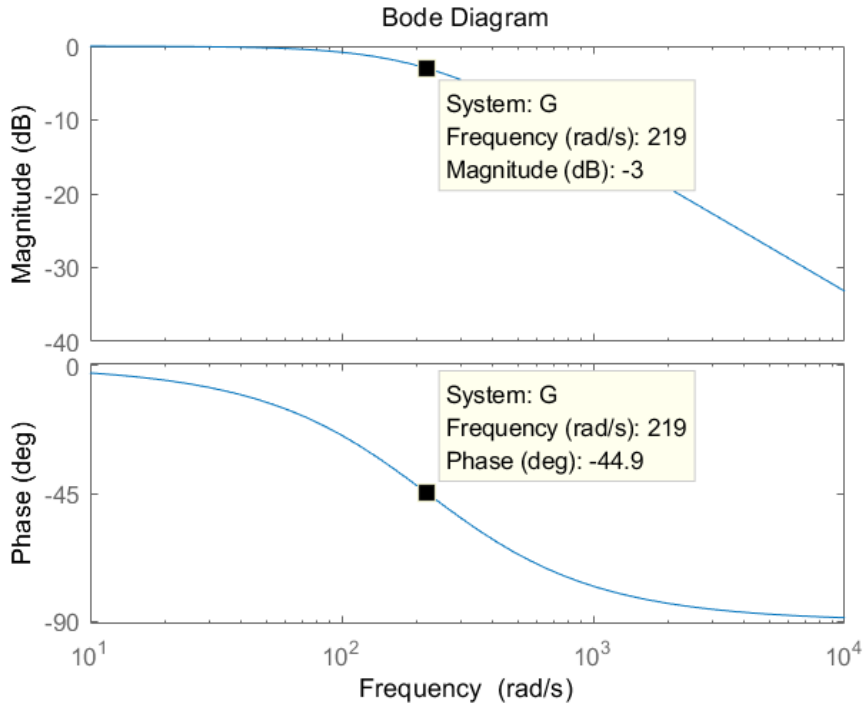
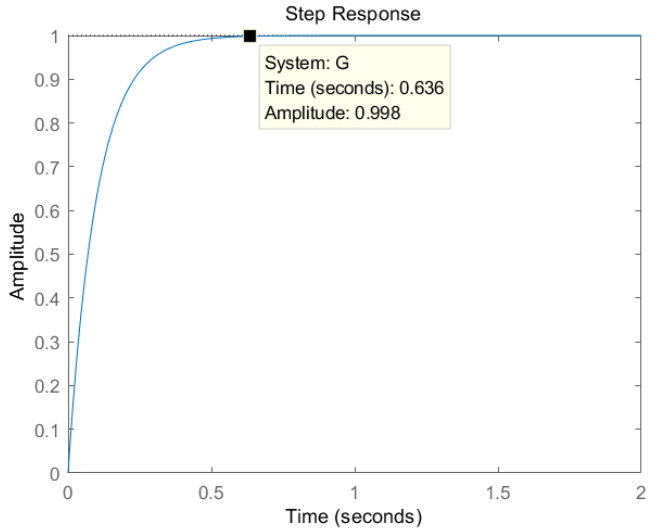


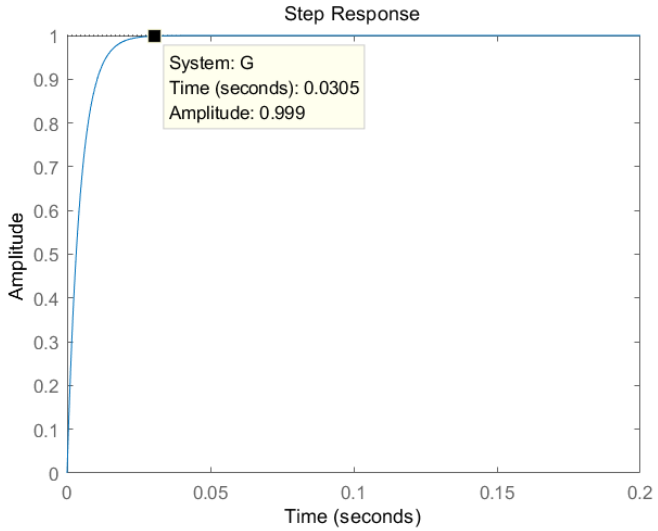
Figure 2.4: The Bode diagram of the low-pass filter when the cut-off frequency is 219.1 rad/s

close to 0 dB. Consequently, the extracted harmonic currents do not contain these frequency elements, making them fail to be removed from the power line current.

Another problem relating to this method is the long settling time. Fig.2.5 shows the step responses of the low-pass filter when the cut-off frequencies are 10 rad/s and 291.1 rad/s respectively. It is clear that the settling time for 10 rad/s is 0.636s which is much longer than that for 219.1rad/s, which is 0.0305s. The 10 rad/s gives a lower cut-off frequency and hence more harmonic elements with lower frequencies can be extracted leading to better harmonic elimination performance than that having a higher cut-off frequency. However, a longer settling time may have an adverse influence on the system speed in eliminating harmonics. Therefore, an appropriate cut-off frequency needs to be chosen carefully.



(a)



(b)

Figure 2.5: (a)The step response of the low-pass filter when the cut-off frequency is 10 rad/s (b) the step response of the low-pass filter when the cut-off frequency is 219.1 rad/s

2.4.2 High Pass Filter Based Extraction Method

The best-known method based on a high pass filter is the instantaneous power theory proposed by Akagi in 1983 [19]. This relies on separating the instantaneous active, reactive and harmonic powers from the apparent power measured in real-

time. The three phases need to be transformed into the coordinate system and then the instantaneous active and reactive power can be obtained as

$$\begin{bmatrix} P(k) \\ Q(k) \end{bmatrix} = \begin{bmatrix} \overline{P}(k) + \widetilde{P}(k) \\ \overline{Q}(k) + \widetilde{Q}(k) \end{bmatrix} = \begin{bmatrix} v_{R\alpha} i_{R\alpha} + v_{R\beta} i_{R\beta} \\ v_{R\beta} i_{R\alpha} - v_{R\alpha} i_{R\beta} \end{bmatrix} = C_{pq} \begin{bmatrix} i_{R\alpha} \\ i_{R\beta} \end{bmatrix} \tag{2.4}$$

where $C_{pq} = \begin{bmatrix} v_{R\alpha}(k) & v_{R\beta}(k) \\ v_{R\beta}(k) & -v_{R\alpha}(k) \end{bmatrix}$,

The $\overline{P}(k)$ and the $\overline{Q}(k)$ are the average components of the instantaneous active and reactive power. The $\widetilde{P}(k)$ and the $\widetilde{Q}(k)$ are the oscillation components. These oscillation components can be extracted by high-pass filters. The transfer function of a high pass filter is expressed by (2.5) and its bode diagram is shown in Fig.2.6 (a). Fig.2.6 (b) shows the step response and the settling time is around 0.03s which is similar to that of the low pass filter with the same cut-off frequency.

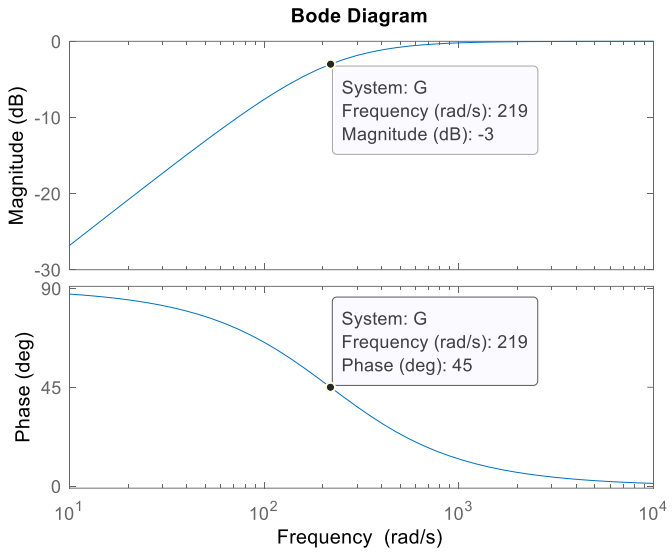
$$T(s)_{HPF} = \frac{s}{s + \omega_0} = \frac{1}{1 + \frac{\omega_0}{s}} \tag{2.5}$$

A high pass filter can stop the signals which have frequencies lower than the cut-off frequency. It has similar problems compared with the above described SRF method which uses a low pass filter. Therefore, with proper selection of the cut-off frequency, it is possible to derive all harmonic current elements from the harmonic powers $\widetilde{P}(k)$ and $\widetilde{Q}(k)$ at each sample instant by (2.6)

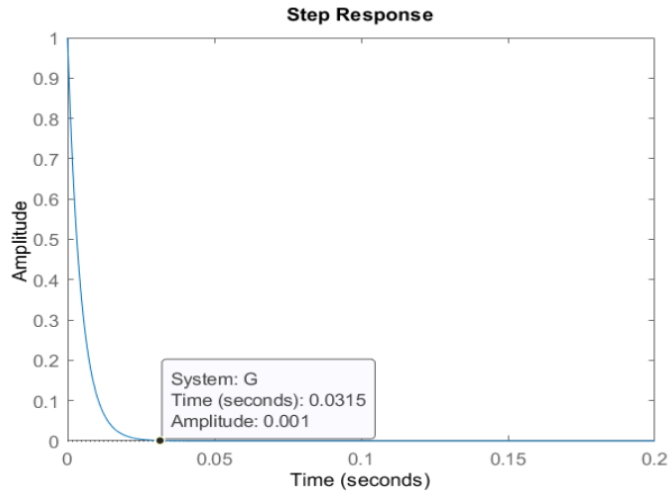
$$\begin{bmatrix} i_{h\alpha}(k) \\ i_{h\beta}(k) \end{bmatrix} = C_{pq}^{-1} \begin{bmatrix} \widetilde{P}(k) \\ \widetilde{Q}(k) \end{bmatrix} = \frac{1}{v_{R\alpha}(k)^2 + v_{R\beta}(k)^2} \begin{bmatrix} v_{R\alpha}(k) & v_{R\beta}(k) \\ v_{R\beta}(k) & -v_{R\alpha}(k) \end{bmatrix} \begin{bmatrix} \widetilde{P}(k) \\ \widetilde{Q}(k) \end{bmatrix} \tag{2.6}$$

The control diagram for the instantaneous power theory is shown in Fig.2.7.

However, this method relies on distortion-free grid reference voltages for extraction of harmonic currents and hence would not work well in the presence of voltage harmonics or imbalance.



(a)



(b)

Figure 2.6: (a) The bode diagram and (b) the step response of a high pass filter when the cut-off frequency is 219.1 rad/s

2.4.3 Notch Filter Based Extraction Method

The well-known notch filter is a band-stop filter that can remove only a narrow band of frequency elements in the applied signal and pass all other frequency

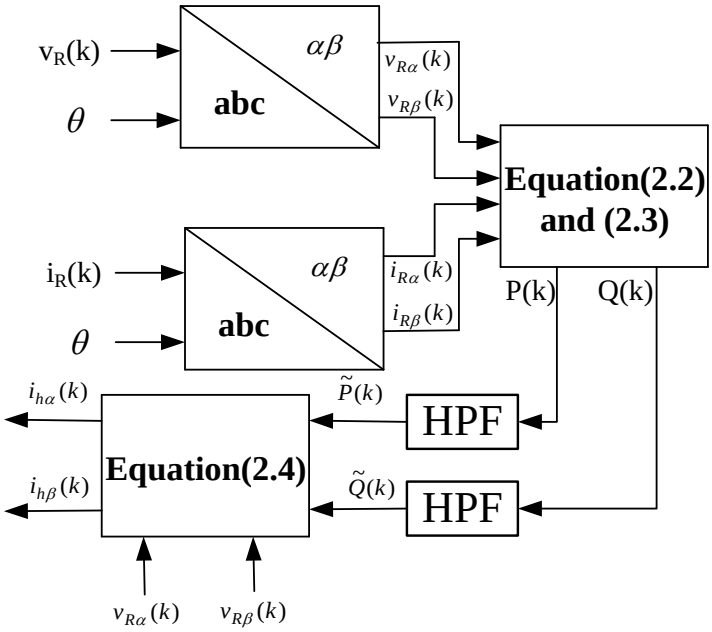


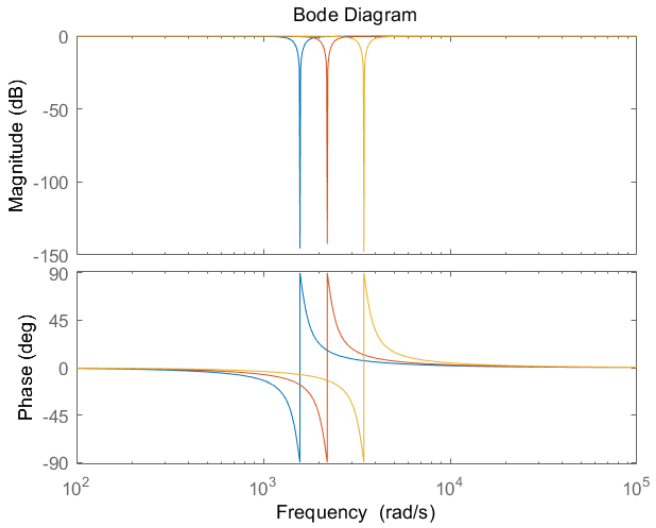
Figure 2.7: The control diagram of the high-pass filter-based extraction method

components with negligible attenuation. This feature makes it attractive for the power line harmonic elimination since the typical harmonics present in a power line phase current are odd and up to 17th order, so instead of extracting all harmonics in the current, it is more beneficial to eliminate a selection of dominant harmonics using the notch filters. The transfer function of one notch filter is shown below:

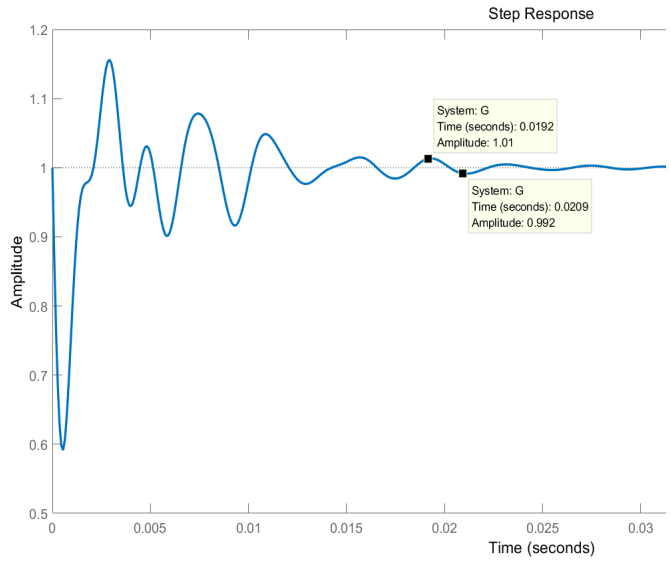
$$T(s)_{NF} = \frac{s^2 + \omega_0^2}{s^2 + 2\sigma\omega_0 s + \omega_0^2} \tag{2.7}$$

where the specific cut-off frequency is determined by the ω_0. The σ is the damping ratio which determines the width of the notch and is normally set to a relatively low value of 0.1 to 0.2 to sharpen the frequency band to be stopped. For application in a power system, the low order harmonics are the main concern, hence ω_0 is usually set to a lower value.

For eliminating multiple harmonic components, a number of notch filters can be connected in either cascaded or parallel topologies. In the current study, a cascaded



(a)



(b)

Figure 2.8: (a) The Bode diagram and (b) the step response of the notch filters

structure with three notch filters which removes 250, 350, and 550 Hz components, is applied.

Fig.2.8 (a) shows the bode diagram of three cascaded notch filters. The magnitude of the gain margin drops to -150dB which means 5th, 7th and 11th order harmonics are completely attenuated. Other elements with frequencies outside

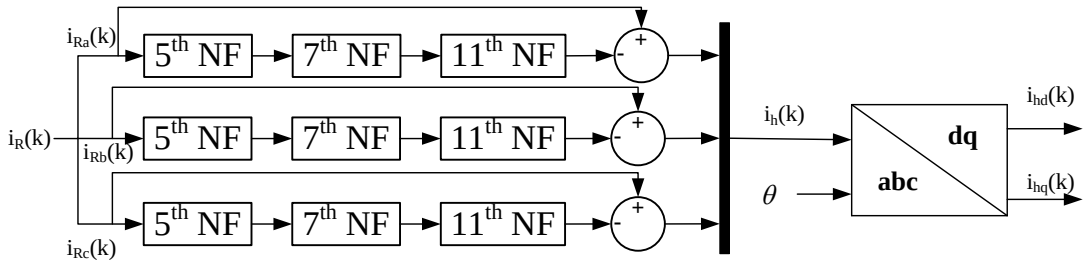


Figure 2.9: The control diagram of the notch filter-based extraction method

these three frequencies have magnitudes nearly 0dB, hence are all preserved. A strong attribution of a notch filter is that it causes little phase lag at the gain crossover frequency, assuming the notch frequency is well above that. This is because the phase shift of a notch filter with a high frequency is near zero, which causes little time delay. This compares favorably to an LPF which has a phase shift from 0-90 degree. Fig.2.8 (b) shows the step response of the cascaded notch filter, having a settling time of about 19 ms for a system to reach the steady state. This is significantly shorter than that of an LPF with the same -3 dB cut-off frequency which is 219.1rad/s

A method for using this cascaded notch filter to extract harmonic currents is illustrated in Fig. 2.9. The objective is to cancel the harmonic currents $i_h(k)$ with h=5, 7, and 11 within the applied current $i_R(k)$. As can be seen, this can be done by applying the measured three-phase current to their respective cascaded notch filters which have the identical three pre-set stopping frequencies. Then by subtracting the filtered currents from their corresponding original input signals, the three-phase harmonic current $i_h(k)$ is derived. With the voltage phase angle θ already available from a Phase Locking Loop, and applying Park Transformation, the $i_h(k)$ can be transformed to its equivalent d-q components $i_{hd}(k)$ and $i_{hq}(k)$. These are the extracted harmonic reference signals which are then applied to the STATCOM current control loop for elimination.

The NFs can be made adaptive by flexibly changing their stopping frequencies. This feature is desirable for the power line harmonic current mitigation, since the harmonic current frequencies may change constantly due to the load and source variations. In the published paper, the cascaded NFs are made adaptive with the help of the Discrete Wavelet Packet Transform technique which is effective in identifying the dominant harmonics in the measured line current.

2.5 Harmonic Identification by Wavelet Technique

Variations of the power line current harmonic frequencies arise from many factors, most significantly the changes in the loads. For accurate harmonic mitigation, it is important to identify the harmonic frequencies present in the line current on-line in real-time and subsequently update the stopping frequencies of the harmonic filters used.

The Wavelet Transform (WT) technique is a strong tool for signal processing which can process the non-stationary signals in both time and frequency domains [20]–[23]. Unlike the FFT [24], [25] which expands the signal in terms of the sine waves, the WT uses wavelets which are generated in the form of the translations and the dilation of the mother wavelets. These are irregular in shape with special scaling properties and localized in time, making them ideal for representing the transient distorted electrical signals with no stationary features. There are three types of Wavelet transform; the Continuous wavelet transform, the discrete wavelet transform and the wavelet packet transform. The basic ideas of the first and third types are described below leading to the justification for choosing the third type to estimate the power line harmonic current.

2.5.1 Continuous Wavelet Transform (CWT)

The CWT transforms a time domain waveform into the time-frequency domain and estimates the signal in the time and frequency domains simultaneously. The basic equation of a CWT [26] is defined in (2.8).

$$CWT_f(a,b) = \frac{1}{\sqrt{a}}\psi(\frac{t-b}{a})dt \tag{2.8}$$

where a is the scale factor and b is the translation factor and they are both continuous variables, and the f(t) is the input signal in the time domain. Hence, the original one-dimensional signal f(t) is transformed into a two-dimensional signal $CWT_f(a,b)$. The ψ_t is named as mother wavelet which is a decaying wavelet basis function with a finite-length. The dilated (stretched) and the translated (shifted in time) versions of the mother wavelet are then generated. The dilation is denoted by the scale factor a while the time translation is adjusted through b. In general, the larger the scale factor a corresponding to the low frequency part, the higher the frequency resolution, and vice versa. The existence of the translation factor b makes it possible to obtain the specific position of that low frequency part in the time domain.

There are many different types of mother wavelets, such as Haar, Daubechies, Meyer, etc [27]. These wavelet basis functions must observe the following two features:

1. The mean of the mother wavelet must be 0 which can be shown in (2.9). However, in a certain interval, a mother wavelet must have a value.

$$\int_{-\infty}^{+\infty} \psi(t)dt = 0 \tag{2.9}$$

2. Mother wavelet should be restricted in the function space composed of the quadratic integrable function which is the $L^2(R)$, namely the Lebesgue space. The

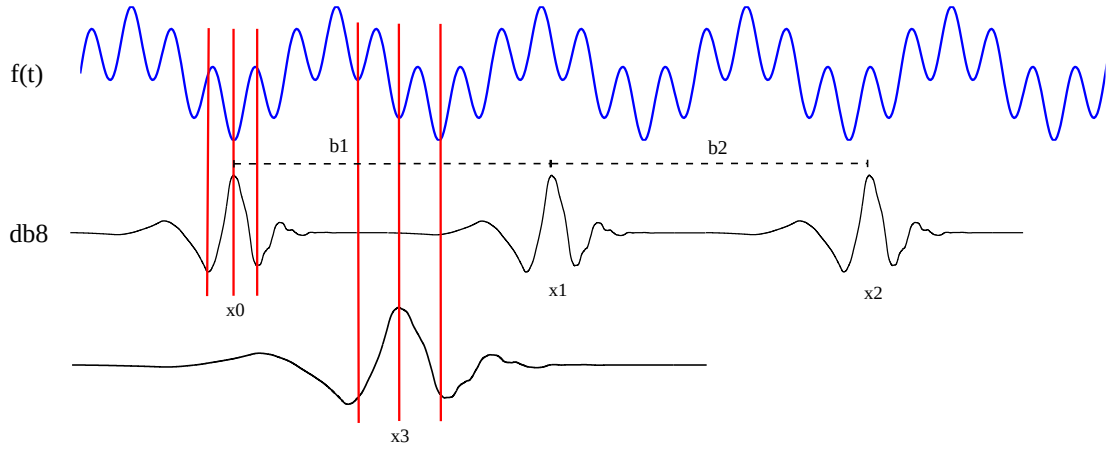


Figure 2.10: The original waveform f(t) and the wavelet function with different a and b values

related equation is expressed in (2.10)

$$\int_{-\infty}^{+\infty} \left|\psi(t)\right|^2 dt = 1 \Leftrightarrow \psi(t) \in L^2(R) \tag{2.10}$$

In Fig.2.10, the original waveform is the f(t) which contains the fundamental frequency and the 5th order harmonic. The db8 is chosen as the wavelet function. There are four wavelets x0-x4 due to different scale factors and translation factors. By multiplying continuously the original waveform with the wavelets, the result obtained at a specific scale represents the frequency component $CWT_f(a,b)$ corresponding to that scale. If the sampling frequency is f_s, the central frequency of the wavelet function is f_c, and the frequency related to the scale factor a is equal to:

$$f_a = f_c \times f_s/a \tag{2.11}$$

The scale factor a of x3 is half of a for x0. Hence, the frequency order corresponding to x3 is twice that in x0. It can be seen that the x1 and x2 are obtained by translating x0 by b1 and b2 distance respectively. Thus depending on the transla-

tion factor b, the exact location of a specific frequency determined by a in the time domain can be known.

The information contained in CWT, as a continuous transform, must be redundant on the time-frequency frame which results in complicated computation hence CWT is not suitable for real-time use.

2.5.2 Discrete Wavelet Packet Transform (DWPT)

The discrete wavelet packet transform (DWPT) can overcome the limitations of the CWT mentioned in the above subsection and is selected in the work of the power line harmonic elimination. In this technique, a sampled signal series is decomposed into scaling and wavelet coefficients by convolution with both a high-pass filter and a low-pass filter at the uniform frequency bands, and thus it can extract both high and low frequency elements of the signal.

Assuming a signal P, having M samples, it is convolved with a low-pass filter, h_l, and a high-pass filter, g_l . These filters are the quadrature mirror filters (QMFs) [28] and their relationship meets the following expression:

$$g(l) = (-1)^l h(L-l-1) \tag{2.12}$$

where the l and L are the order and length of the filter ($l = 0, 1, ...L-1$) respectively. Since at every level of decomposition, the signal is down sampled by a factor of 2. The wavelet coefficients at any level j for the kth point in $2n$ and $2n+1$ nodes are obtained by convolution with the filters h and g as follows

$$P_j^{2n}[k] = \sum_{l=0}^{L-1} h_l P_{j-1}^n[2k-l] \tag{2.13}$$

$$P_j^{2n+1}[k] = \sum_{l=0}^{L-1} g_l P_{j-1}^n[2k-l] \tag{2.14}$$

For M samples of the original signal, the number k of the wavelet coefficients in each node for the jth layer satisfies the following equation:

$$k = M/2^j \tag{2.15}$$

So the wavelet coefficients in the nth node at the jth layer are indicated by: $P_j^n[k] = 0, 1, 2....M/2^j$

Fig.2.11 shows the decomposition tree of the measured signal with a constant bandwidth up to level $j = 3$, leading to the derivation of 8 nodes of the detail and the approximation coefficients.

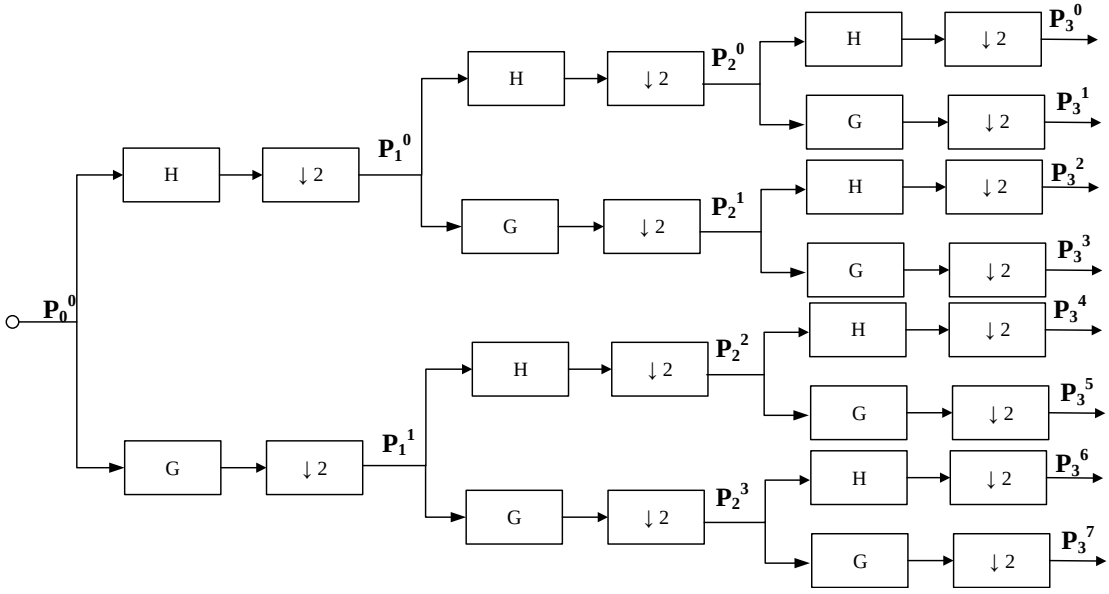


Figure 2.11: The DWPT data decomposition tree up to 3-levels.

Similar to the FFT technique, the original signal can be reconstructed or recovered through the characteristic coefficients obtained by the DWPT decomposition process, where the equation for reconstruction is given as:

$$P_{j-1}^n[2k-l] = \sum_{l=1}^{L} h_l^* P_j^{2n}[k] + \sum_{l=1}^{L} g_l^* P_j^{2n+1}[k] \tag{2.16}$$

Here the h_l^* and the g_l^* are the antithetic operators of the low-pass and high-pass filters h_l and g_l [29].

If a single odd harmonic is to be observed, the coefficients in other nodes in the same layer can be set to 0, and then through the reconstructing process, the signal waveform of a specific frequency in the original signals can be obtained.

2.5.3 Selection of Mother Wavelet

Selecting a suitable Mother Wavelet is important in using DWPT for processing sampled data which are time varying power signals in real-time. Adequate choice of the mother wavelet leads to accurate results and computational efficiency. High accuracy from a power signal depends on using the high order wavelet filters which can cope well with faster waveform response. Thus high-order mother wavelets are often chosen for the harmonic element rms value calculations [30], [31]. However, the computational complexity and the number of coefficients are correlated, hence these wavelet functions cause longer delays in the signal analysis, making them more suitable for the off-line stationary signal analysis, but not ideal for the on-line tracking of the non-stationary or the transient variation signals.

In this work, three different wavelet functions are compared according to their performances in harmonic extraction accuracy and speed. These are Daubechies wavelet functions: the db8 with 16 coefficients, the db30 with 60 coefficients, and the discrete meyer with 98 coefficients which can be seen in Fig.2.12 (a-c). A synthetic waveform as shown in Fig. 2.13 (a) is used for this study. It is composed of a fundamental component and a 5th order harmonic with a magnitude being 100 for both elements and is expressed as:

$$x(t) = 100sin(2\pi \times 50t) + 100sin(2\pi \times 250t) \tag{2.17}$$

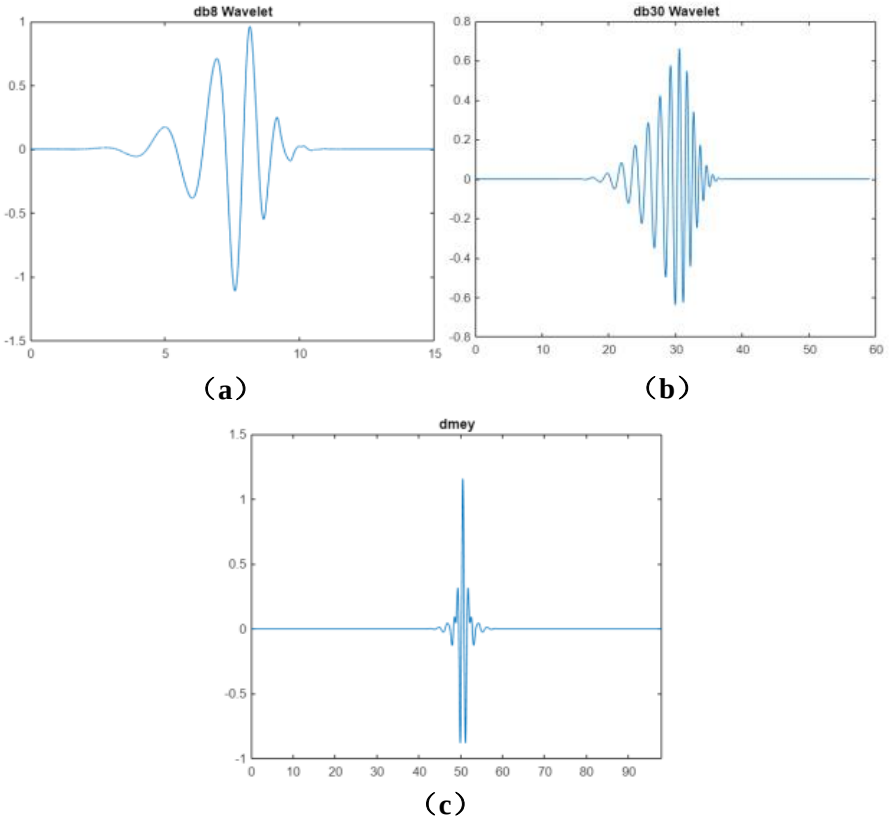


Figure 2.12: The mother wavelet function (a) db8, (b) db30 and (c) discrete meyer

Fig. 2.13 (b) to (d) shows the rms value variations of the reconstructed $5th$ order harmonic using respectively the above said three wavelet functions. As can be seen, the reconstructed $5th$ order rms from the db8 wavelet presents the highest level fluctuations (30%), while the waveform from using the db30 is more stable which is 4%. However, it is the waveform from the discrete meyer which shows the minimum level of variations (1.5%). In quantifying this feature, a percentage oscillation error is defined as the maximum peak-peak rms value over the desired $100/\sqrt{2}$.

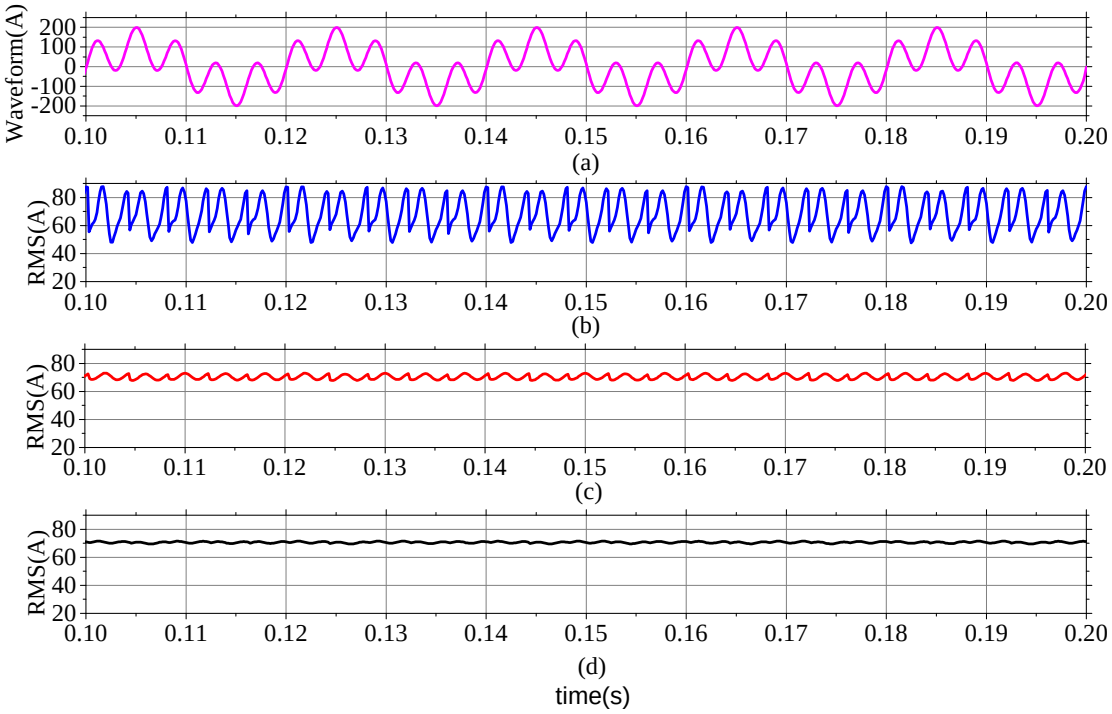


Figure 2.13: (a) The Original signal waveform. The RMS values of the 5th order element in the reconstructed signal by (b) db8, (c) db30, (d) discrete meyer.

2.5.4 Sample Frequency

Another important consideration for the DWPT application is the number of sampled data required for the maximum decomposition layer. This depends on the highest harmonic element in the original signal to be extracted. In the distorted load current, the odd harmonics such as the $3rd$, $5th$ up to $17th$ orders are the dominant elements. For effective extraction, the frequencies of these elements should be in the centers of their respective node, namely the frequency band. Also, the signal should be decomposed continuously until the fundamental component is separated from all the other harmonic elements. Assuming the highest harmonic frequency in the signal is 3200 Hz, according to the Nyquist criterion, the chosen sampling frequency should be twice this value, i.e. 6400 Hz. The decomposition layer j is determined by the maximum harmonic order to be extracted and the

sampling frequency. In this case, the 5 decomposition levels are required in order to extract the fundamental and the odd harmonics from $3rd$ to $63th$ order through the coefficients P_0^5 to P_{31}^5 with a uniform frequency band of $100Hz$. All odd harmonics are in the central position within each band. The relationship is shown in table 2.3 [32], where it can be seen that the observable frequency range is evenly distributed among these nodes.

Table 2.3: The decomposed layers associated with the maximum harmonic order and the sampling frequency

Maximum harmonic order	Sampling frequency $f_s(Hz)$	Decomposed layers j
$3rd$	400	1
$7th$	800	2
$15th$	1600	3
$31st$	3200	4
$63rd4$	6400	5

In addition, choosing a suitable sampling frequency can also improve the reconstructed signal. In Fig.2.14 (a), when the sampling frequency is 800Hz, the signal f(t) is sampled during 0.04s which means only 32 points are stored in the memory. After the 2 layers decomposition and reconstruction, there are 10 cycles for the 5th order harmonic waveform during 0.04s and each cycle only has 32/10=3.2 points so that the reconstructed waveform cannot even form a sinusoidal wave. It is obvious that the peak to peak values are far away from the desired result which is 100. This problem still exists (Fig.2.14 (c)) even if the sample time increase to 0.32s which means there are 256 sample points stored. However, when the sampling frequency is 6400Hz, 256 sample points are stored during 0.04s, the reconstructed signals are shown in Fig.2.14 (b). Each cycle has about 25.6 points which are enough to draw the sine wave. In the middle part, except the point at 110 which is 91.1122, other peak to peak values are within the 4 percent oscillation

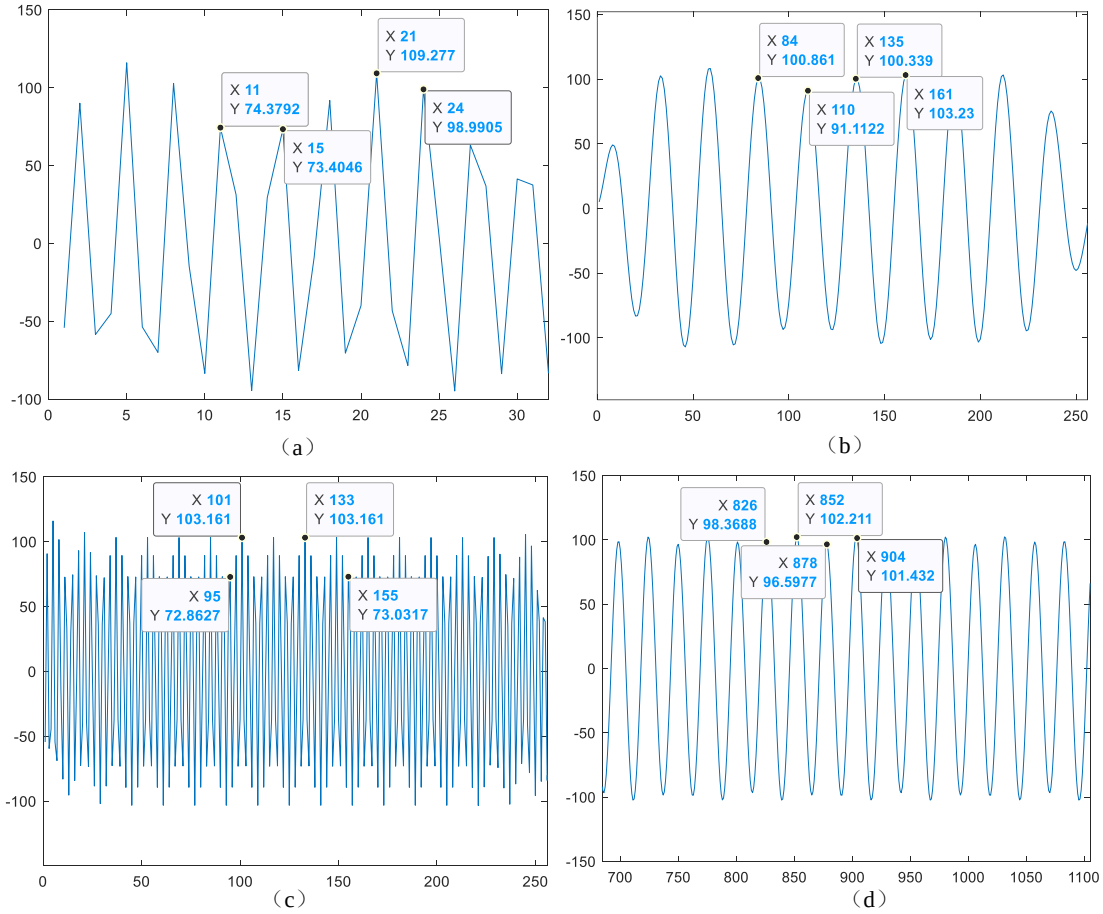


Figure 2.14: The reconstructed waveform by db30 wavelet function under (a) 800Hz and (b) 6400Hz for 0.04s and (c) 800Hz and (d) 6400Hz for 0.32s

of the desired value. When the sample time increase to 0.32s (Fig.2.14 (d)) and 2048 points are sampled, all peak-peak values are within 4% oscillation proving the reconstruction performance is improved compared with that for 0.04s. This result shows that the more points are sampled or the higher sampling frequency is chosen, the more accurate the reconstructed signal will be. Hence, choosing a high sampling frequency can not only obtain more harmonic information, but also give more points in the limited time to improve the accuracy of the reconstructed signals. Whereas, this way also means an increased computational burden.

2.5.5 Boundary Effect

In real-time programming, to obtain one result at the (2n)th node in j level, several signals at the nth node in j-1 level are required. The number of required signals is determined by the number of the low-pass and the high-pass filters' coefficients. In the DWPT, if some of the data are undefined or have no actual values, they can be assigned to 0. The consequence of this action is although the signals can be decomposed continuously, it will eventually lead to the distortion of the reconstruction waveform. For example, assuming that the filter has 3 coefficients, the result when k=0 and 1 at the (2n)th node in j level will be expressed by:

$$P_j^{2n}[0] = h_0 P_{j-1}^n[0] + h_1 P_{j-1}^n[-1] + h_2 P_{j-1}^n[-2] \tag{2.18}$$

$$P_j^{2n}[1] = h_0 P_{j-1}^n[1] + h_1 P_{j-1}^n[0] + h_2 P_{j-1}^n[-1] \tag{2.19}$$

The results since $P_{j-1}^n[-1]$ and $P_{j-1}^n[-2]$ do not exist, so they are undefined and set to 0. This gives the wrong results to $P_j^{2n}[0]$ and $P_j^{2n}[1]$. This phenomenon has a large effect at both ends of the sampled data which can be seen in Fig.2.14 (b), and it is called the boundary effect. The signal distortion is very noticeable in two periods which are 0 to 50 points and 200 to 250 points respectively. To solve this problem, the data expansion method is introduced which will be described in the published paper. Another advantage of the data expansion way is several sampled points can be expanded to a sufficient number so that the DWPT can supply accurate results in a short time period.

2.6 The Published Paper

2.6.1 Introduction

The growing use of the power electronic controlled-equipment, such as the uncontrolled rectifiers, the grid-tied converters for the renewable sourced generators [11], and the large traction drives [12], results in significant levels of the harmonic current components drawn at the Point of Common Coupling (PCC). Consequently, they cause PCC voltage distortion owing to the flow of the harmonic current through the finite line impedance. The voltage and current harmonics degrade the quality of power supplied to the customers, the power system operating stability, and the efficiency.

Research in harmonic current cancellation has resulted in various techniques aiming to separate the harmonic components from the fundamental current. One important device is the Static Compensator (STATCOM) [1]–[3] which is a flexible and effective tool for the harmonic mitigation and for compensating reactive power. It uses a Voltage Source Inverter connected in parallel with the power line via a coupling impedance or a transformer to inject appropriate compensating current to the system. The development of modular multilevel cascaded converters (MMCC) [4] in the last two decades facilitates the applications of the STATCOM to the medium and high voltage networks [9], [10]. The modular structure of an MMCC-STATCOM, having either the full H-bridge or the flying-capacitor converters as sub-modules, offers the advantage of flexibility in generating the compensating current with the required waveform at a low switching frequency. The device is efficient and fault tolerant, with a small footprint [5]–[8].

The key to enabling any STATCOM to eliminate the harmonics is its ability to identify and extract the harmonic elements, often time varying, in the load current. Advanced signal processing techniques in both time and frequency domains have

been employed. Most well-known, in the time domain, is the instantaneous reactive power theory proposed by Akagi in 1983 [19]. This relies on separating the instantaneous active, reactive and harmonic powers from the apparent power measured in real-time. Subsequently, it is possible to derive all harmonic current elements from the harmonic power at every sampling instant. However, this method relies on distortion-free grid reference voltages for extraction of harmonic currents and hence would not work well in the presence of supply voltage harmonics or imbalance. An alternative approach is based on the Synchronous Reference Frame (SRF) theory [33]. This operates by transforming the load currents into a d-q reference frame rotating at the fundamental frequency, so that the harmonic components become AC terms that can be extracted. The method needs a phase-locking loop for the three-phase current transformation. It also requires a low-pass filter which must be tuned properly with a sufficiently low cut-off frequency and an adequate speed of response to follow the load current changes.

Among the techniques for harmonic analysis, the very familiar fast Fourier Transform (FFT) [24], [25] provides magnitude-frequency information with the advantages of high accuracy and lower computational burden than the Discrete Fourier Transform (DFT). It suffers from the poor detection of the time locality when the signal varies abruptly, and hence is most suited to the stationary power signal analysis. To better describe the non-stationary signals, the Short-Time Fourier Transform (STFT) has been a useful tool, though it relies on properly selecting the size of a time window and the window function must be well-localized.

The Wavelet Transform (WT) provides a different approach that can process the non-stationary signals in both time and frequency domains [20]–[23]. Unlike the FFT which expands the signal in terms of the sine waves, the WT uses wavelets that are generated in the form of the translations and the dilation of mother wavelets. These are irregular in shape with special scaling properties

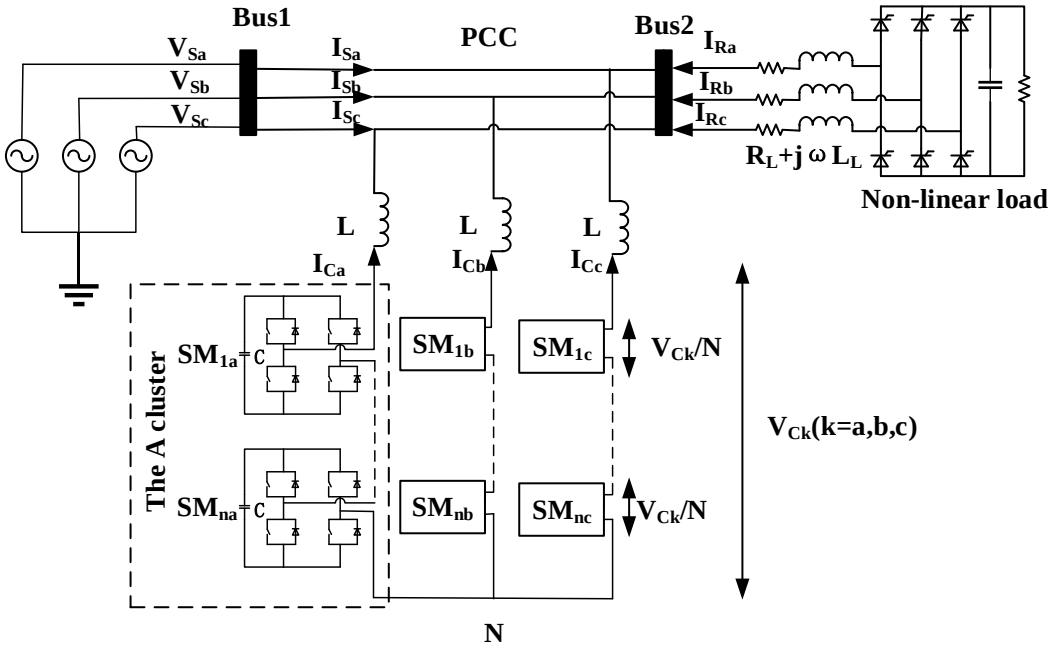


Figure 2.15: The configuration of MMCC-STATCOM.

and localized in time, making them ideal for representing the transient distorted electrical signals with no stationary features. Various WT implementations have been derived, such as the continuous wavelet transform (CWT) [26] which has been shown to be computationally complex and hence not suitable for real-time use. The multi-resolution analysis [34], [35] and the discrete wavelet transform (DWT) [36] reduce computation complexity and have been used in various power quality analysis work [37]–[39]. However, these possess clear limitations since the signal is decomposed into the approximations (low-frequency components) and the details (high-frequency components), but only the former is processed. This leads to the loss of certain information about the signal. The discrete wavelet packet transform (DWPT) can overcome this limitation. In this technique, a sampled signal series is decomposed into the scaling and the wavelet coefficients by convolution with both a high-pass and a low-pass filter at uniform frequency bands, and thus it can extract both high and low frequency elements of the signal.

In using the DWPT and other WT techniques for processing sampled signals in real-time, certain issues require careful consideration with the time varying power signals. A proper selection of the mother wavelet, which must be based on the features of the signal analyzed, results in the reduction of the computational burden and improves accuracy in the result. The boundary effects due to the limited data samples will cause a distortion of the reconstructed harmonic waveforms leading to the inaccuracy of the detected harmonic components.

This paper proposes an adaptive harmonic current extraction scheme using the notch filters combined with a modified discrete wavelet-packet transform (DWPT). The scheme is applied to control an MMCC-STATCOM which cancels the harmonic current on the power line. As is well known, the odd harmonics are generally dominant in the power line current while even and inter-harmonics are negligibly small and this has been validated in [40], [41], hence the proposed scheme uses the DWPT to identify only a selection of lower order odd harmonics. They are eliminated using a chain of notch filters [42], [43] with their rejection frequencies tuned to the identified values. To attenuate the residual even harmonics, arising from the asymmetric load current, and the small inter-harmonic elements on the power line current, the method adjusts the damping ratios of the notch filters to widen their stop frequency bands and this yields useful suppression of extra frequencies.

The modified DWPT employs the discrete Meyer as the mother wavelet, which is selected according to the criterion of the minimum oscillation error. It also incorporates a data expansion technique to overcome the limitations of boundary effects due to insufficient data samples. The technique identifies the rms values of the dominant harmonic elements in the non-stationary current in accordance with the IEEE Standard 519-2014 [44] in real-time.

Section 2.6.2 of the paper outlines the configuration of the star-connected MMC-

STATCOM. The data expansion technique for DWPT is described in detail in section 2.6.3. The complete adaptive harmonic current cancellation control scheme is discussed in section 2.6.4 and validated in section 2.6.5.

2.6.2 The Configuration of MMCC-STATCOM

The configuration of the star-connected MMCC-STATCOM is shown in Fig.2.15. There is no link between the neutral points at the converter side and the supply side. Each of the three phases consists of N serially connected H-bridge converter sub-modules, each having a floating capacitor maintaining its voltage at V_{Ck}/N, and hence generating (2N+1) voltage levels: 0, $\pm(1/N)V_{Ck}$, $\pm(2/N)V_{Ck}$ ..... $\pm V_{Ck}(k = a,b,c)$. The terminals of the three phase clusters are connected to the grid at the point of common coupling (PCC) through three single-phase filter reactors L. These reduce the high frequency harmonics due to the switching but naturally create the time-delays for the current flow. At the load side, a phase controlled rectifier with an $R-L$ load is applied. Not only can this emulate the steady non-sinusoidal current flow, it can also imitate, by varying the phase angles, the transient interruptions caused by a sudden surge of the load current or the faults of switching operations.

The function of the STATCOM is to inject the current to the grid at the PCC point, which eliminates as much as possible the reactive/harmonic elements in the load current, and hence improves the quality of the grid supplied power. The PCC current is given as $I_{Sk} = I_{Ck} + I_{Rk}$.

2.6.3 The DWPT with Data Expansion

2.6.3.1 Data Expansion for Real-Time Application

For the on-line real-time tracking of the harmonic components in the non-stationary signal, the signal decomposition is performed using the data collected continuously

over a short time window. This is necessary especially for tracking the transient surge currents due to the faults or the sudden load changes, hence to register the time of occurrences, and the magnitudes and frequencies of any abnormalities. However, for fast tracking, the time window per data processing may be narrow hence the number of data collected may be small, leading, consequently to insufficient data for performing multiple levels of the data decomposition. For example, if a data window is set to 0.01 second, i.e. one half of a 50Hz period with the sampling frequency of 6400 Hz, it yields 64 data samples. This data set is far too small to allow 5 level data decomposition, but further increasing the sampling rate adds more real-time computational cost and data noise. A simple approach to overcome this dilemma is to replicate the sampled data within each data window to the number required. Thus with the data logged at each sample interval being x(m), it can be replicated as many times as needed. The resultant data number per sample interval can be stored in a two dimensional array as:

$$y(m,i) = (-1)^i x(m) \tag{2.20}$$

where the m represents the number of samples per fixed time window which is 64 in this example, and the i represents the number of replication per data window. In this way, the data in a sampling window, originally 64 samples, would be expanded to $64i$ in total. To ensure the number of data is sufficient for 5 level data decomposition and also the results are sufficiently accurate, results are compared for i = 10, 50 and 100. Fig. 2.16 (a)-(d) shows, respectively, the variations of rms values of the reconstructed 5th order element obtained for using these three replication numbers and that without data expansion. Fig.2.16 (a) shows the highest level of rms variation without data expansion, the oscillation error (%), with the discrete meyer, is about 20%. With i changing from 100 to 10, the data samples from 6400, 3200 to 640 in Fig.2.16 (b) to (d), the corresponding error

percentages are 1.5%, 5% and 8%, respectively. Thus, replicating to 6400 samples is chosen since it is the most accurate and the processing times for all cases are the same.

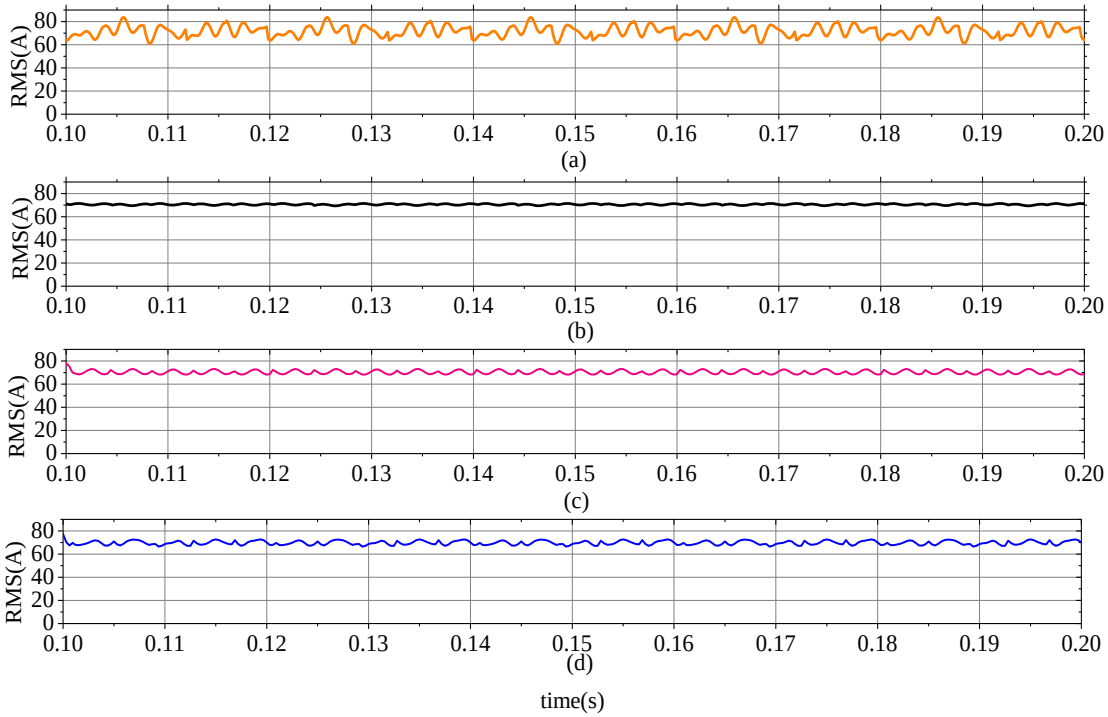


Figure 2.16: Reconstructed 5th order element by discrete meyer (a) without data expansion, (b) with data expansion expanding to 6400 samples (c)3200 samples and (d) 640 samples.

Noting for the analysis without data expansion, the data window is extended to 2 fundamental periods, hence 256 samples in total are available, and consequently, the data tracking speed is naturally slower.

2.6.3.2 Boundary Distortion Reduction

The problem of the edge effects in filtering would affect the accuracy of the DWPT results, due to the convolution is performed on a signal with the finite length. Several conventional methods for correcting this effect have been developed [45].

In this work, the application of the data expansion technique is shown effective in suppressing the edge distortion effect.

Implementation of the DWPT is performed from the beginning at every sample interval with the full set of data. Due to the data duplication, the edge distortion effect is significantly reduced. Fig. 2.17 (b) shows the reconstructed $5th$ order harmonic waveform derived at two selected data points, one, 2874 (black line), is at the middle of the data window and the other, 5998 (red line), near the end. As can be seen, both waveforms conform well with the original one (blue line). There are few errors shown in the amplitude, the small phase delay is due to the data processing.

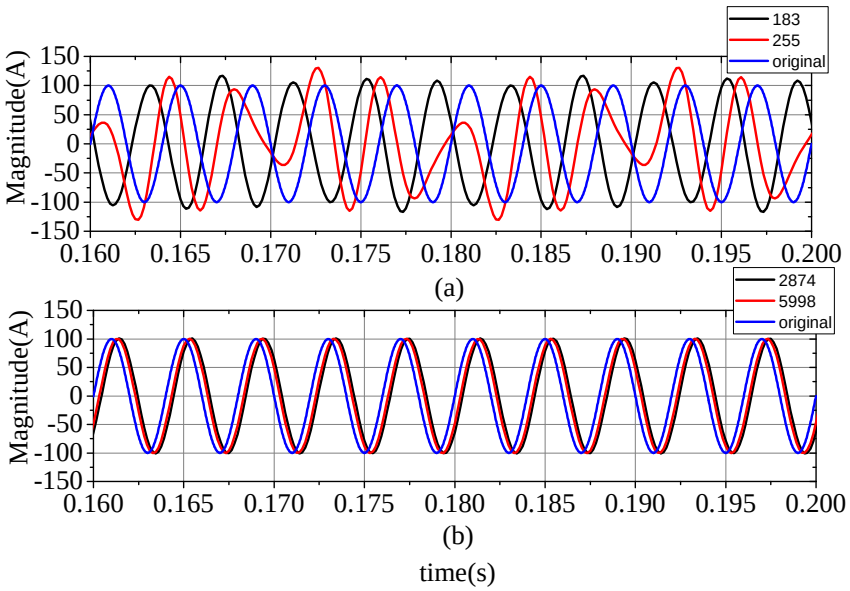


Figure 2.17: Reconstructed signals by choosing different points (a) without and (b) with data expansion.

2.6.4 DWPT Based Adaptive Harmonic Control

In this study, the above DWPT algorithm is used for the harmonic cancellation by the MMCC-STATCOM of Section 2.6.2. The key element in the STATCOM filtering

scheme is an adaptive multiple frequency band notch filter chain, which consists of a number of single band-stop notch filters. The number of these filters and their parameters are updated according to the harmonics extracted by the DWPT operating online in real-time. Fig.2.18 illustrates the overall control strategy for the MMCC-STATCOM and comprises three main parts: the DWPT-based ANF, the cluster sub-module voltage balance control, and the overall current control block. The latter two parts are well-known and need not be described here.

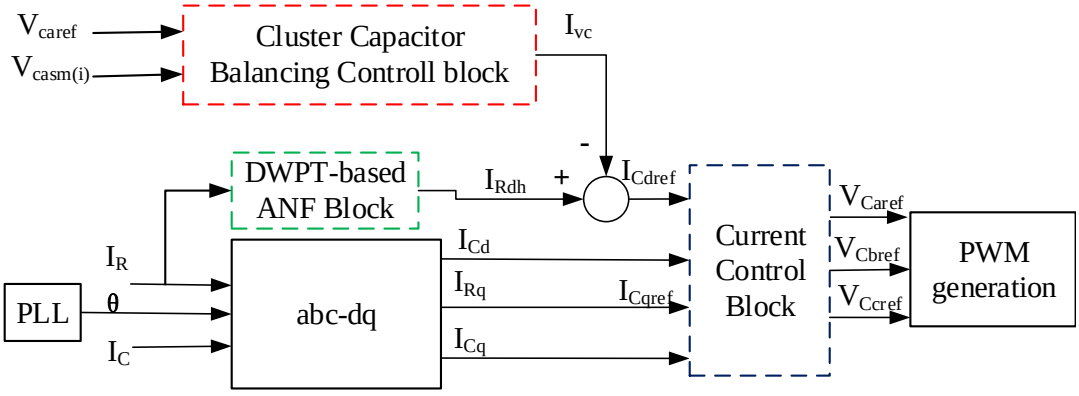


Figure 2.18: Overall control strategy for the MMCC-STATCOM.

2.6.4.1 DWPT-Based ANF

A notch filter can effectively attenuate a harmonic element in the applied signal. The transfer function of a single notch filter is expressed as [46]:

$$T(s)_{NF} = \frac{s^2 + \omega_0^2}{s^2 + 2\sigma\omega_0 s + \omega_0^2} \tag{2.21}$$

where the ω_0 is the required stop frequency and the σ is the damping ratio which determines the width of the notch. To attenuate a range of even and inter-harmonic elements surrounding the dominant odd harmonics, the damping factor can be adjusted in order to widen the frequency stop-band. Fig.2.19 shows the bode plot of a notch filter when the stop-frequency is set at the $5th$ order harmonic (1570 rad/s)

with different damping ratios from 0.1 to 0.5. It is clear that the dB values of the harmonic elements closing to the 5th order are substantially attenuated. However, a larger damping ratio comes with a price of increased phase shift. A study using a system shown in Fig.2.15 with load firing angle variations has been performed. The results are shown in Table 2.4 with the σ changing from 0.1 to 0.5 for periods 2, 3 and 4 denoting firing angles 0°, 30°and 45° respectively. It is clear that the higher σ yields a lower THD of the resultant current waveform but a longer time delay in the current response. Especially when the damping ratio is around 0.5, the delay time is about 21ms, twice as long as that when the σ is 0.1, so a compromise needs to be made. In this case, the σ = 0.2 is chosen.

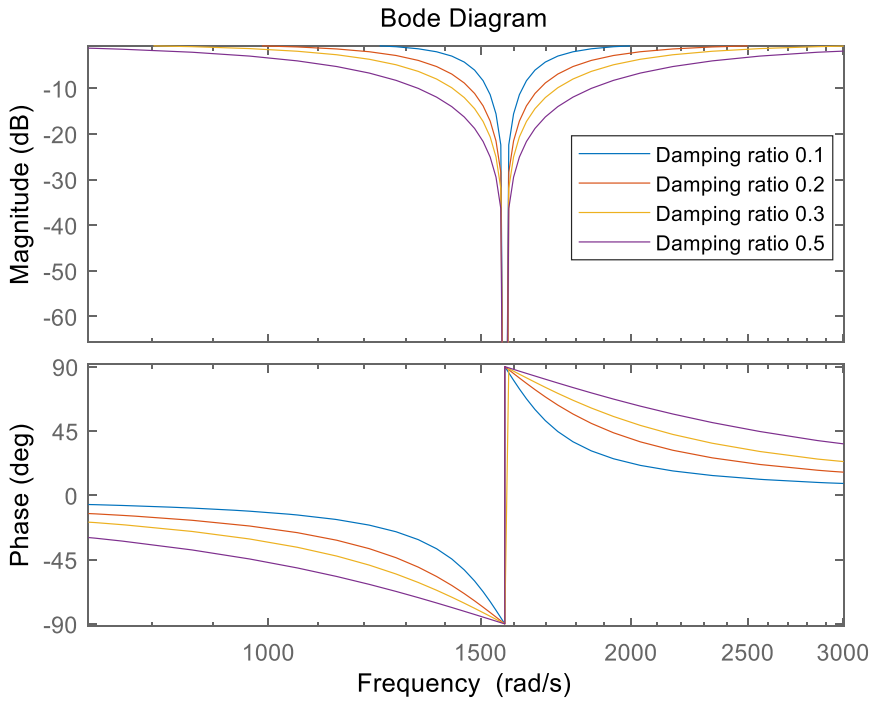


Figure 2.19: The bode diagram for the adaptive notch filters.

The current harmonics in a power system may be time varying, correspondingly the frequencies of the notch filters need to be adjusted, hence being adaptive. The configuration of the adaptive notch filter with the DWPT as the harmonic element

Table 2.4: The THD values of the PCC current and the settling time with different damping ratios of the notch filters

Damping ratio	Period 2	Period 3	Period 4	Settling time(ms)
σ=0.1	2.04%	2.77%	4.77%	11.445
σ=0.2	1.91%	2.74%	4.44%	14.634
σ=0.3	1.85%	2.56%	4.1%	17.236
σ=0.5	1.75%	2.34%	3.7%	21.103

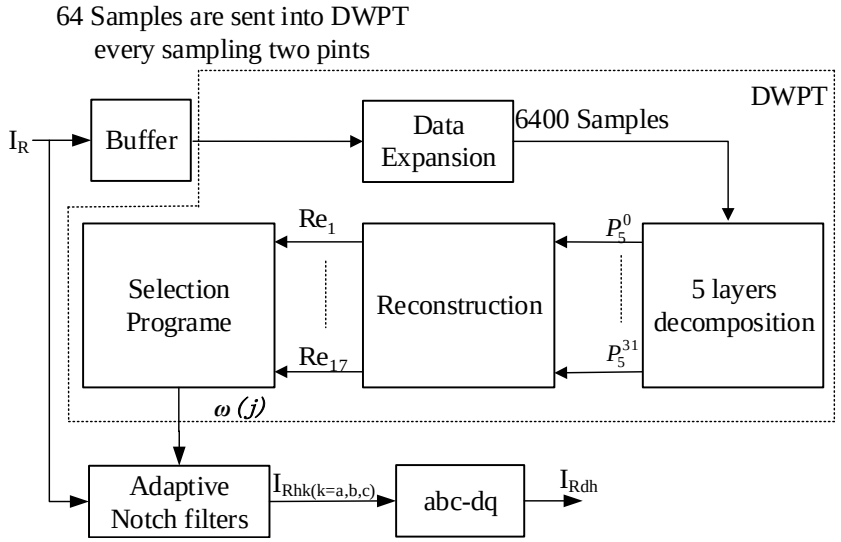


Figure 2.20: The schematic of the real-time DWPT harmonic identification.

tracker is shown in Fig.2.20. As can be seen in this figure, the Re_1 up to Re_{17} are the reconstructed signals ranging from the fundamental to the $17th$ harmonic, the j represents the number of the notch filters required in the chain and the $\omega(j)$ stores the selected harmonics to be eliminated. The selection is based on the IEEE-519-2014 [44] standard, in which the allowed maximum harmonic current distortion is 4% from the $3rd$ to $11th$ harmonic and 2% between the $11th$ and $17th$. Thus when the ratio between the $13th$ or $17th$ harmonic and the fundamental is higher than 2%, this order is included in the notch frequencies $\omega(j)$ to be eliminated. However, in this work, the maximum number of the chained filters is five, since more filters in the chain increase the transient response time to more than about

12ms. A comparison of the maximum notch filter numbers performed is presented in the above subsection.

The implementation of the DWPT algorithm in real-time relies on having enough data samples to produce accurate results. A moving data window based on the FIFO scheme is used and the data is held in a buffer. Once the harmonic elements in the power line current are identified by the DWPT-based ANF, their elimination by the MMCC-STATCOM relies on setting the reference current of its current controller. This can be achieved by turning the band-stop ANF into a band-pass filter. Fig.2.21 shows the implementation of the adaptive band-pass filter for the three-phase current. The measured power line three-phase current is processed by the ANF, and the output is then subtracted from the original current. The resultant output becomes one part of the reference current for the STATCOM controller. The fundamental part is the reactive current.

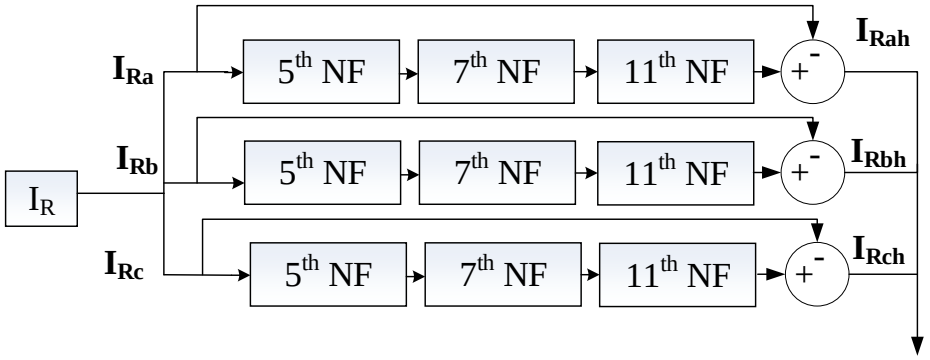


Figure 2.21: The implementation of a three-phase band pass filter.

When simultaneous reactive power compensation is required. This can be obtained by either using a PCC voltage control scheme or the direct measurement of the reactive load current element. Here the latter method is chosen.

2.6.5 Simulation Results

To verify the above control scheme for the harmonic current cancellation. The power system with the MMCC-STATCOM has been simulated as shown in Fig.2.15. The system component parameters are listed in table 2.5.

The whole simulation process is designed with four different operation periods as follows:

Period 1: From 0s to 0.05s, the system supplies the distorted current to the three-phase thyristor-controlled non-linear load with a firing angle 0°. The MMCC-STATCOM is disabled, so the converter compensation current I_C is zero.

Period 2: From 0.05s to 0.1s, the STATCOM is switched on and working to compensate the reactive power and the harmonic current. The firing angle remains 0°.

Period 3: From 0.1s to 0.2s, the STATCOM continuously operates with the load firing angle changing to 30°.

Period 4: From 0.2s to 0.3s, the load firing angle is changed to 45°.

The corresponding current waveforms measured at the PCC are shown in Fig.2.22. The THD values and the ratios of the dominant harmonic elements to the fundamental current drawn by the load are listed in Table 2.6. The fifth harmonic is the most significant, followed by the $7th$ and $11th$. However, when the firing angle is 30°, the $13th$ harmonic increases to above 2% which can not be ignored. Likewise at the firing angle is 45°, the $17th$ harmonic is 4.0% which is higher than 2% and should be eliminated.

2.6.5.1 Harmonic Detection using DWPT with/without Data Expansion

Using the data expansion method discussed in Section 2.6.3, the identified ratios (%) of the $5th$, $7th$, $11th$, $13th$ and $17th$ harmonic magnitudes to the fundamental

Table 2.5: The parameters for simulation

Sending end voltage V_s	110V
Inductor L	2mH
Load resistance R_L	0.1Ω
Load inductance L_L	10mH
Capacitor C	1.12mF
Non-linear load resistor	30Ω
Non-linear load capacitor	1mF
Capacitor voltage for each sub-module	50V
Switching frequency	1KHz
Memory Buffer	64
Sampling frequency	6400Hz
DWPT decomposition layers	5

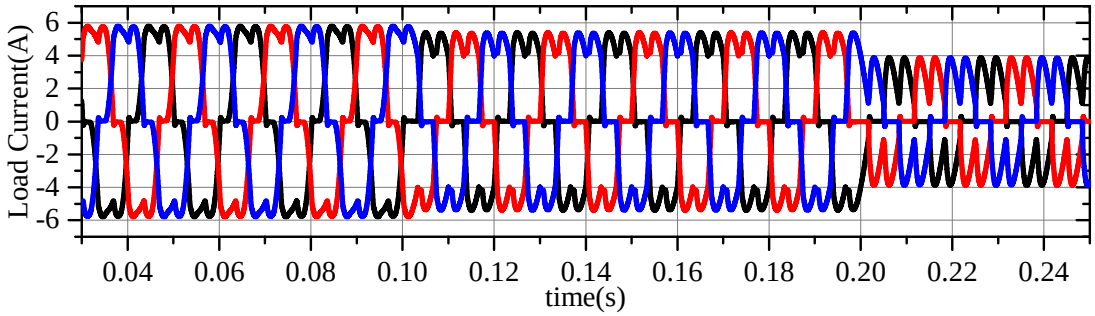


Figure 2.22: The load current I_R from the non-linear load when the firing angle changes from 0° to 30° at 0.1s and from 30° to 45° at 0.2s.

current are shown in Fig.2.23 and Fig.2.24, and that without data expansion are displayed in Fig.2.25.

Clearly, by applying the data expansion method, the transient oscillations of the harmonic ratios are lower and they settle down faster than that when expansion is not used. Observing the ratios of the $11th$, $13th$ and $17th$ harmonics, shown in Fig.2.23A (e), (g), (i), identified by the DWPT with the data expansion at the firing angle 0°, these all have low peak-to-peak values of respectively 0.2%, 0.3% and 0.02%. On the other hand, the harmonic ratios identified by the DWPT without data expansion, for the load current with the same firing angle, are shown in

Table 2.6: The THD value and each odd harmonic ratio of I_R

Firing angle	0°	30°	45°
THDs	20.8%	27.91%	32.95%
250Hz ($5th$)	18.1%	25.65%	30.49%
350Hz ($7th$)	5.92%	6.29%	6.23%
550Hz ($11th$)	2.92%	6.27%	8.77%
650Hz ($13th$)	1.41%	3.34%	2.86%
850Hz ($17th$)	1.36%	1.59%	3.98%

Fig.2.25 (e), (g), (i), their peak-to-peak values are significantly higher than 1.8%, 1.1% and 0.4% respectively. It is worth noting that, when identified without data expansion, the $11th$ and $13th$ harmonics in this period fluctuate and sometimes fall below the required level (2%). This is undesirable since the chained notch filters in the ANF are set in real-time according to the identify harmonic orders. Frequent variations of the ANF will lead to inaccuracy in the harmonic compensation.

When the firing angle is 30°, the peak-to-peak harmonic ratio for the same $11th$, $13th$ and $17th$ harmonics are shown also in Fig.2.23A (f), (h), (j). With data expansion, they are 0.7%, 0.7% and 0.05%. The results with no data expansion, as shown in Fig.2.25 (f), (h), (j), are significantly higher at 4.0%, 1.0% and 0.6%. Clearly, the data expansion method improves the accuracy and stability of the identified harmonic values.

According to the UK National Grid Code, the nominal frequency is 50Hz, with an allowed interval of 49.5Hz to 50.5Hz under the normal operation [47], thus it is necessary to evaluate the performance of the DWPT at the extremes of the grid frequency compared the results with those obtained at 50Hz. Fig.2.24 shows the DWPT identified the harmonic components for these system frequency cases. Noting that the displayed results for these two frequencies correspond to the period with a load firing angle of 30° and 45°, where the harmonic response performance is considered the worst. It can be seen clearly that the estimated

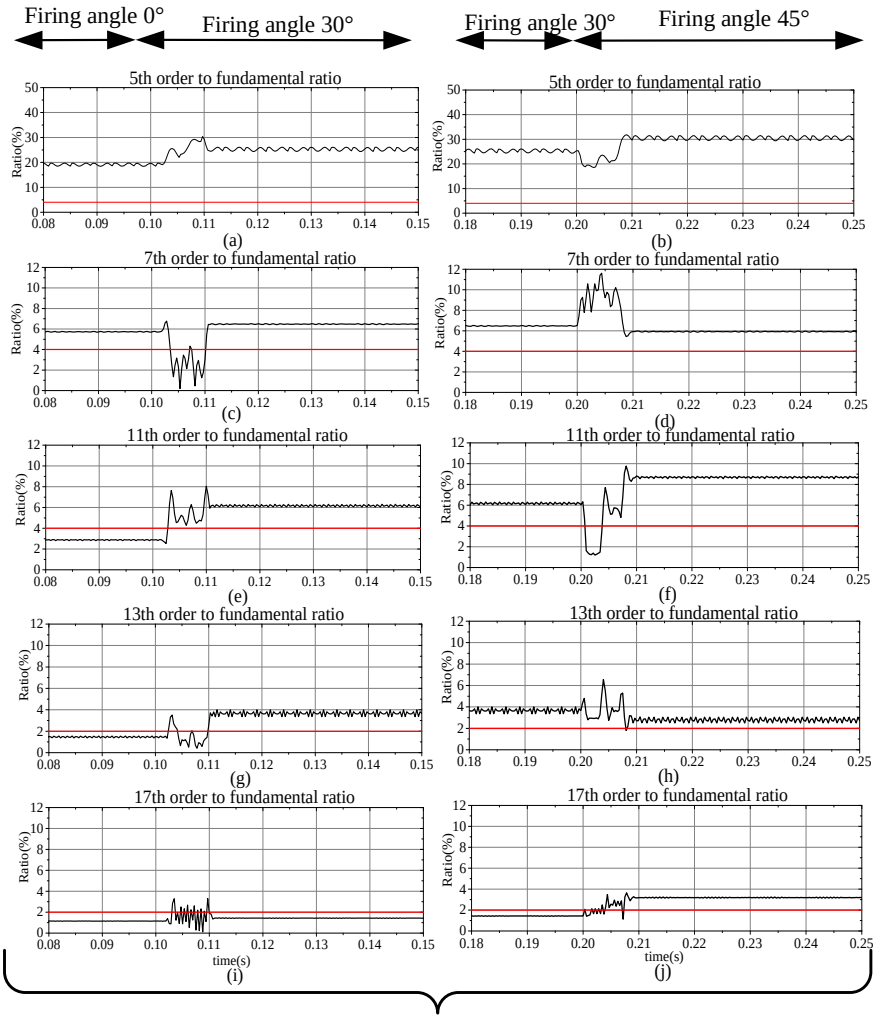


Figure 2.23: The variations of the 5th, 7th , 11th, 13th and 17th harmonic to the fundamental ratio identified by the DWPT with the data expansion. A When the power system frequency is 50Hz: (a) 5th order when the firing angle changing from 0° to 30° and (b) from 30° to 45° (c) 7th order when the firing angle changing from 0° to 30° and (d) from 30° to 45° (e) 11th order when the firing angle changing from 0° to 30° and (f) from 30° to 45° (g) 13th order when the firing angle changing from 0° to 30° and (h) 30° to 45° (i) 17th harmonic when the firing angle changing from 0° to 30° and (j) from 30° to 45°.

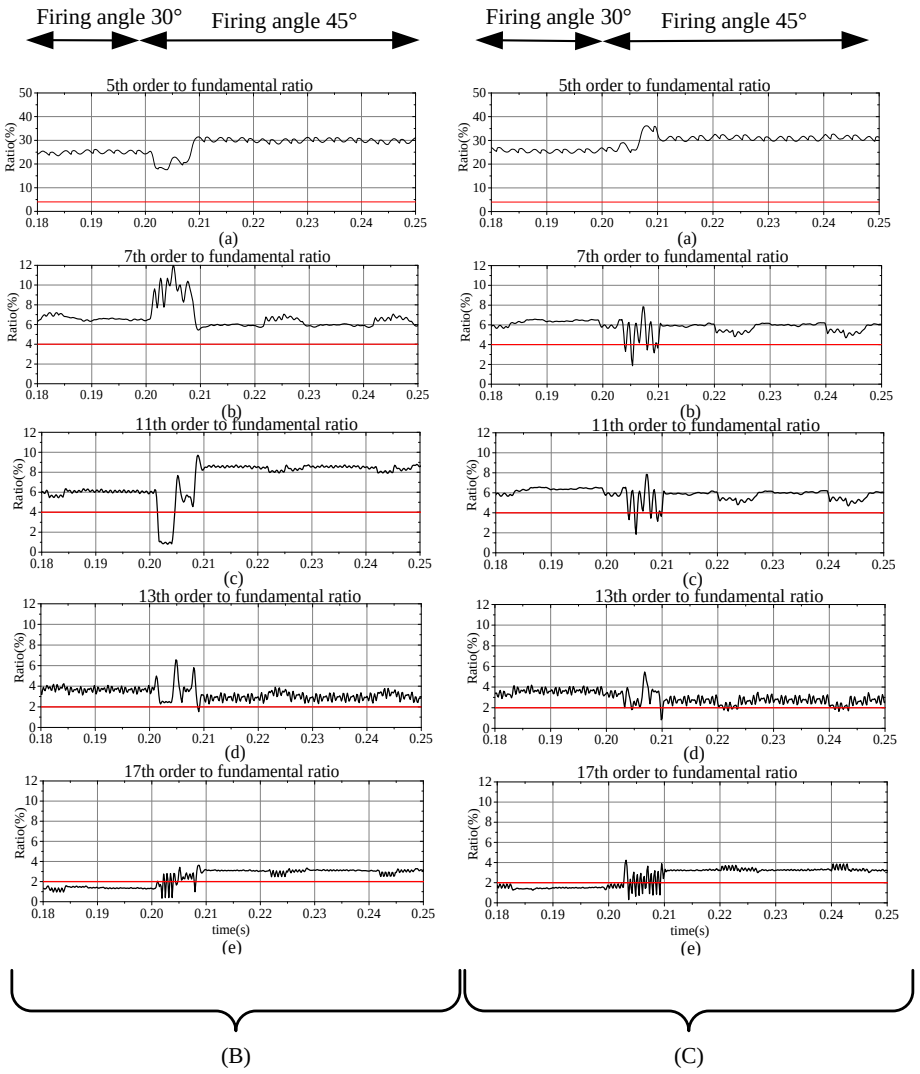


Figure 2.24: The variations of the 5th, 7th , 11th, 13th and 17th harmonic to fundamental ratio identified by the DWPT with the data expansion. B When the power system frequency is 49.5Hz and the firing angle is from 30° to 45°: (a) 5th order (b) 7th order (c) 11th order (d) 13th order (e) 17th harmonic. C When the frequency is 50.5Hz and the firing angle is from 30° to 45°: (a) 5th order (b) 7th order (c) 11th order (d) 13th order (e) 17th harmonic

harmonic magnitudes present slightly higher fluctuations than when the frequency is 50Hz, while settling down to their respective steady states. The patterns of

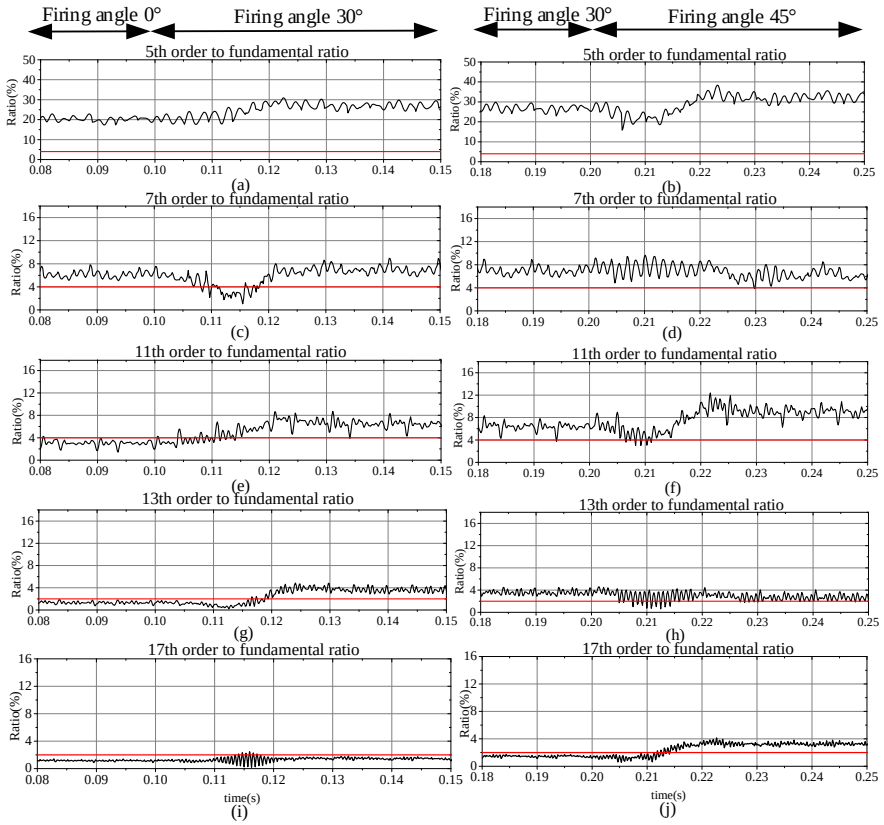


Figure 2.25: Variations of the $5th$, $7th$, $11th$, $13th$ and $17th$ harmonic to the fundamental ratio identified by the DWPT without the data expansion (a) $5th$ order when the firing angle changing from 0° to 30° and (b) from 30° to 45° (c) $7th$ order when the firing angle changing from 0° to 30° and (d) from 30° to 45° (e) $11th$ order when the firing angle changing from 0° to 30° and (f) from 30° to 45° (g) $13th$ order when the firing angle changing from 0° to 30° and (h) 30° to 45° (i) $17th$ harmonic when the firing angle changing from 0° to 30° and (j) from 30° to 45°.

fluctuations repeat every 20ms. This is because the DWPT data window width is set as a half cycle of 50Hz. However, since the ratios of the harmonic amplitudes to the fundamental amplitude frequency are, in general, only about 0.6% higher than that at 50Hz, they lead to activating the same group of notch filters as those selected at 50 Hz. For example, as shown in Fig.2.24B (a), (b), (c), (d) and (e) when the frequency is at 49.5Hz, all oscillation levels are higher than the set criterion for triggering the corresponding notch filter, consequently, the same group of notch

filters is set and the filtered current THD values measured at the PCC are the same as those when the system frequency is 50Hz. There is only one case which may affect the setting of a notch filter, namely when the frequency is 50.5Hz, the ratio of the $13th$ harmonic (Fig.2.24 C (d)) to the fundamental drops to slightly lower than the 2% limit. This may lead to the corresponding notch filter being canceled. This, however, has not resulted in a significant negative effect on the performance of the filtered current since the other harmonic elements identified do not fall below the limit (2% or 4%). The current performance is in fact better than that without the data expansion, when the system frequency is 50Hz. Thus it is clear the proposed DWPT+Notch filter scheme will work well with the allowed grid frequency deviations.

In addition to the steady-state fluctuation range of the detected harmonics, the transient performance is also worth noting. In Fig.2.23, when the firing angle varies at 0.1s and 0.2s using the data expansion method, it takes about 0.01s for the harmonic elements to settle to their steady-state values. However, the transient time intervals are much longer without using data expansion as can be seen in Fig.2.25. In general, it takes about 0.02s for the harmonic magnitudes to settle to their stable levels.

2.6.5.2 Current Control Results

Fig.2.26 shows the waveforms of the current I_S measured at the PCC point, its d component I_{Sd} , and the STATCOM compensating current I_C , using the ANF combined with the DWPT using the data expansion. The same current waveform obtained without data expansion is displayed in Fig.2.27.

During periods 1 and 2, the load firing angle is 0°, and the identified harmonic orders with a ratio above 2% lead to three notch filters being used in the STATCOM control system, namely at the $5th$, $7th$ and $11th$ harmonics. As can be seen in

Fig.2.26 (a), the STATCOM is not turned on initially until at 0.05s, so the PCC current waveform is distorted first and then becomes sinusoidal when STATCOM is effective. Likewise, the d-component of I_S, shown in Fig.2.27 (d), is oscillatory first and then becomes a stable DC current with small ripples after 0.05s. These are all due to the output of the STATCOM, whose current I_C, as displayed in Fig.2.26 (g), is zero initially and then active. In contrast, Figs.2.27 (a), (d) and (g) show the waveform of the current measured at the same points under the same load condition but without data expansion. Clearly in this case, the PCC current contains more ripples than are seen in Fig.2.26 (a), and the ripple magnitude in I_{Sd} is significantly higher. This is also reflected by comparing the THD values of I_S as shown in table 2.7, the former is 1.91% for the current in Fig.2.26 (a) and the latter is 6.21% for the current shown in Fig.2.27 (a). Clearly, the THD value obtained by using the method without data expansion cannot meet the standard set in IEEE-519-2014.

The current waveforms measured during Period 3 when using the data expansion are shown in Fig.2.26 (b), (e) and (h). At 0.1s, the load firing angle is changed from 0° to 30°, corresponding, to both the harmonic components and their respective magnitudes in the measured current change. In response, the DWPT in the current control scheme identifies the harmonic elements and subsequently reset the frequencies of the ANF. In this case, the $13th$ order is about 4%, hence the ANF now has 4 notch filters in cascade at the $5th$, $7th$, $11th$ and $13th$ harmonic frequencies. This process takes about 0.015s, hence the current performance during this transient interval may be affected adversely. As shown in Fig.2.26 (b), the levels of harmonic contamination in I_S are higher than those during the transient interval from Periods 1 to 2. Even after the transient period, the current waveform performance is slightly worsened, since the THD value for PCC current I_S is raised to 2.74%. For the same Period 3, the current waveform obtained when using the

DWPT method without data expansion is shown in Fig.2.27 (b), (e) and (h). The I_S fluctuation, during the transient interval after the firing angle changing at 0.1s, is higher and last longer than those shown in Fig.2.26 (b) with the use of data expansion. According to the THD values of I_S after the transient period dies down, the results from both methods are similar (2.73%), showing that the notch filter frequencies identified by both methods are the same.

The current waveform at periods 3 to 4 when the load firing angle is changed from 30° to 45° are shown in Fig.2.26 (c), (f) and (i) using data expansion, and in Fig.2.27 (c), (f) and (i) without data expansion. In this load condition, the $17th$ order exceeds 2%, hence the number of chained notch filters is increased from 4 to 5 having frequencies at the $5th$, $7th$, $11th$, $13th$, and $17th$ orders. Clearly using both methods, the PCC current shows severe distortion during the transient interval, though the current waveform in Fig.2.26 (c) settles more quickly than that shown in Fig.2.27 (c). At steady-state, the current performance obtained with data expansion is better than that without data expansion, since the THD value of I_S for the former is 4.44% (table 2.7), whereas the latter has a THD value as high as 4.87%.

Table 2.7: The THD values of the PCC current I_S

Firing angle	0°	30°	45°
With data expansion	1.91%	2.74%	4.44%
Without data expansion	6.21%	2.73%	4.87%

Fig.2.28 compares the waveforms of the PCC current and its d component obtained using four and five notch filters. The response waveform is taken from period 3 to period 4 (in Fig.2.26), with the firing angle changed from 30° to 45° at 0.2s. In Fig.2.28 (a) and (c), four notch filters are set for 5th, 7th, 11th and 13th harmonics, and in (b) and (d), an additional notch is added at the 17th. The settling time is initially 8.7ms and is increased by about 2ms in (b) and (d).

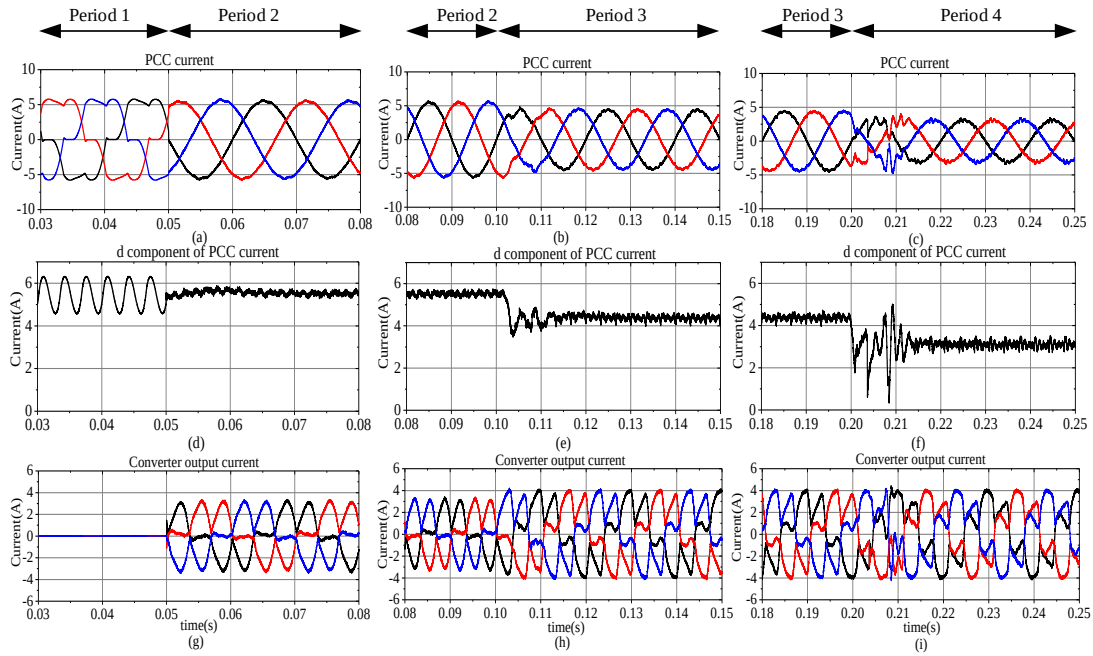


Figure 2.26: The variations of current waveforms using the method with data expansion: I_S (a) from period 1 to period 2 (b) from period 2 to period 3 (c) from period 3 to period 4. I_{Sd} (d) from period 1 to period 2 (e) from period 2 to period 3 (f) from period 3 to period 4. Compensation current I_C (g) from period 1 to period 2 (h) from period 2 to period 3 (i) from period 3 to period 4

However, the THD value for the PCC current is reduced from about 5.4% (4 filters) to 4.8% (5 filters). Since the standard THD limit in the input current is set to 5%, the maximum of 5 notch filters is chosen even though its corresponding current response time is slightly longer.

It is noticeable that the computational burden for the data expansion method is high compared to that of implementing the current control algorithm. To mitigate this burden in real-time, the DWPT algorithm has been implemented at every sample instead of every time. As a result, the harmonic estimation result is updated at the frequency of 3200Hz rather than 6400Hz. This gives sufficient time for the DWPT algorithm implementation without sacrificing accuracy. The time delay for the notch filter corresponding to a load change is about 1/3200s and is negligible

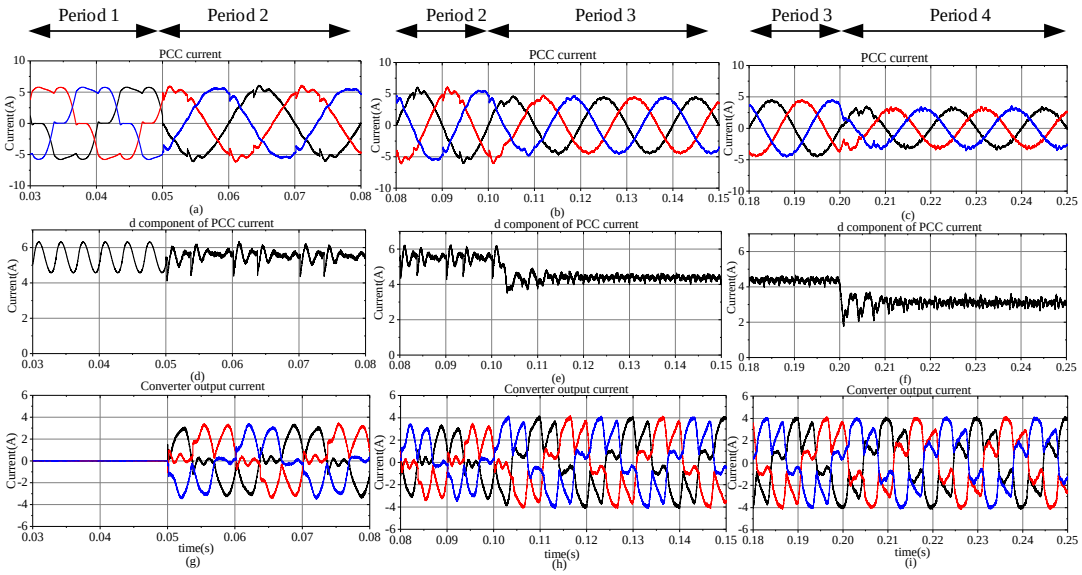


Figure 2.27: The variations of the current waveforms using the method without data expansion: The I_S (a) from period 1 to period 2 (b) from period 2 to period 3 (c) from period 3 to period 4. The I_{Sd} (d) from period 1 to period 2 (e) from period 2 to period 3 (f) from period 3 to period 4. The compensation current I_C (g) from period 1 to period 2 (h) from period 2 to period 3 (i) from period 3 to period 4

compared to that for the whole algorithm.

2.6.6 Conclusions

The paper proposed a modified DWPT with a data expansion method for the harmonic extractions of the power line current. The results have shown that this method identifies the rms values of the dominant harmonics accurately and responds quickly to the current waveform changes. Importantly, the technique was shown to reduce the edge distortion effect compared to the traditional method. The DWPT identifying harmonic elements has been used to update the number and frequencies of a notch filter chain which is embedded in the current control system of an MMCC-STATCOM. The results from the harmonic cancellation performed by the STATCOM show that using the DWPT with data expansion, the

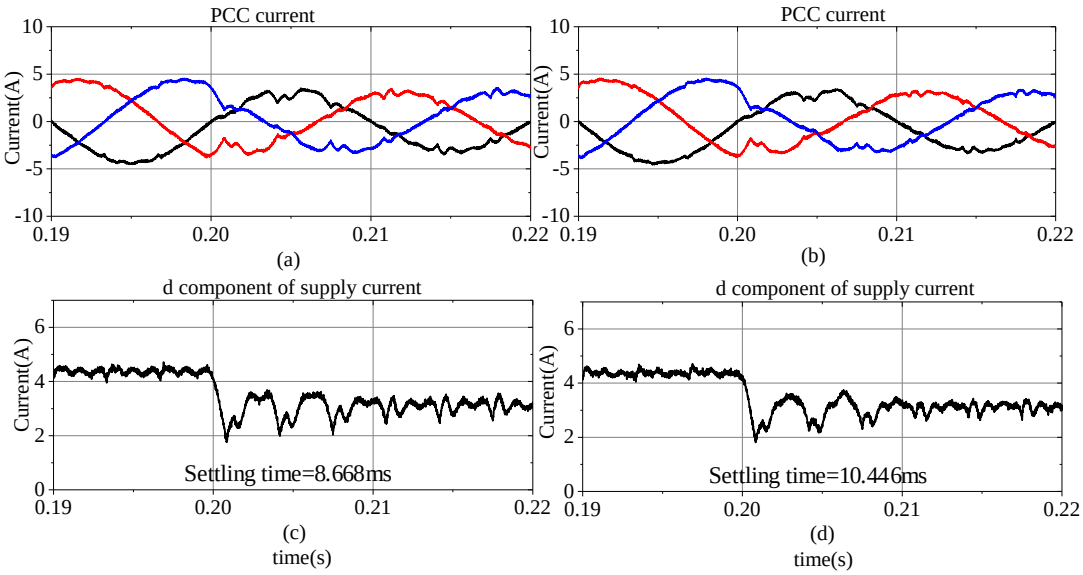


Figure 2.28: The variations of the current waveforms using the method with data expansion: The I_S (a) from period 3 to period 4 when the maximum number of notch filters is 4 (b) when the maximum number is 5. The $I_S d$ (c) from period 3 to period 4 when the maximum number of notch filters is 4 (d) when the maximum number is 5.

controller responded faster, with less than 15ms, for the transient changes of the current waveform compared to that without data expansion (more than 20ms). The accuracy in the harmonic cancellation is evaluated according to the THD of the PCC current measured at the steady states. In all operation conditions, the THD values are lower than that obtained using the DWPT without data expansion.

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CHAPTER 3

MODULATED MODEL PREDICTIVE CONTROL WITH BRANCH AND BAND SCHEME FOR UNBALANCED LOAD COMPENSATION

3.1 Introduction

Having studied the harmonic cancellation method in the previous chapter, the paper to be presented in this chapter deals with the unbalanced power line current mitigation by an MMCC-STATCOM. The power system asymmetries are often caused by faults, such as one line grounding or two-line short circuit. The current unbalance can also be caused by motor winding faults, unequal impedance in the distribution lines and unequal distribution of single-phase loads, etc. An excessive level of the current imbalance leads to a voltage unbalance which has a serious impact on the power quality. It causes high losses in the power line and the motor loads, resulting in the equipment malfunctioning to the extent to be damaged. The STATCOM is often requested to operate under

the asymmetrical conditions and is required to mitigate the level of the power line current imbalance. However, when an MMCC-based STATCOM operates under an unbalanced load, it faces the challenge of phase cluster voltage imbalance. Unlike the STATCOMs of two-level or classical multilevel converters, such as the flying capacitor and neutral point clamped topologies, they have three phase legs sharing a common dc-link, so do not have such an issue. The stacked H-bridge sub-modules in an MMCC phase leg have their respective cell capacitors isolated from each other, so no active power exchange between phases is possible. Consequently, the phase voltages may drift away from their desired levels, resulting in STATCOM malfunction and excessive device stress or damage. Several methods for phase cluster voltage balancing have been proposed, including the zero-sequence voltage injection, and the negative-sequence current injection schemes [1]–[4]. However, they all have their respective deficiencies; the zero sequence voltage injection needs a wide margin of the dc capacitor voltage which may push the converter phase voltages operating above the linear modulation mode or even become uncontrolled in some operating situations. The injection of the negative-sequence current may result in a high maximum current which could damage the power semiconductor devices. Thus further research in mitigating the phase cluster voltage imbalance is necessary.

Another important aspect is the effective control strategies for MMCC STATCOM to achieve the high dynamic performance elimination of the unbalanced line current as well as the reactive power compensation. The conventional control scheme comprises usually four parts [5]; the first is to decouple the +ve and -ve sequence components of the grid voltage and the converter current for the reference current generation. The second controls the average sub-module voltage by generating the necessary positive sequence d-component current I_d^+, it also evaluates I_q^+ according to the grid reactive power need. The third section implements a zero se-

quence voltage /negative sequence current evaluation for the phase cluster voltage balance and finally, it is the current control loop plus the PWM. Mostly for both voltage and current controls, the P+I control law is applied and the parameters are tuned by trial and error which can be time consuming and often not leads to a good performance. A recent trend has seen the Model Predictive Control (MPC) being applied to control the MMC-based HVDC. Two types of method are commonly reported; the finite control set-model predictive control (FCS-MPC) [6]–[8] and the continuous control set-model predictive control method (CCS-MPC) [9]–[13] which is also named as the modulated model predictive control (MMPC). The FCS-MPC has the drawbacks of giving variable switching frequency and poor steady-state performance, while the CCS-MPC avoids variable switching frequency and high computational cost. However, none of the MPC methods in the literature deals with the MMCC STATCOM for the unbalanced grid.

The presented paper proposes a Modulated Model Predictive Control (MMPC) method to suppress the grid unbalanced load current by an MMCC STATCOM. The method has two distinctive features; firstly, the three phase voltages applied to its model for current prediction are imposed with a common mode voltage (CMV). Secondly, a novel Branch & Bound algorithm is designed for minimizing the cost function. The method selects the optimal per phase switch duty ratio by fixing one phase duty ratio to a bound value and minimizing the cost function by the quadratic programming to solve the switch duty ratios of the other two phases. It will be shown that the method is able to mitigate the unbalanced load at the ratio of up to 70% while still maintaining the phase DC-voltages balance.

The chapter presents detailed studies of all techniques required for the unbalanced current compensation by an MMCC-STATCOM, including the methods for the reference signal extraction, the capacitor voltage balancing and the model predictive control schemes. All these backgrounds for the development of the

novel strategy presented in the published paper. The key points in the paper are highlighted.

3.2 Unbalance Issues and International Standard

3.2.1 Problems Caused by Current/Voltage Unbalance

The three-phase unbalance is an important indicator of poor power quality and is mostly due to the unequal three-phase line impedance and load, the one-phase disconnected, and the one or two-phase groundings. The unbalanced three-phase voltage and current operations increase the losses of the power lines, and also lead to the abnormal operation of the motors from the supplying side. Therefore, if the power system cannot withstand the three-phase unbalance that is being suffered, the whole system will be at risk. The problems can be classified as four points shown below:

(1) The increased power line loss. The negative sequence current flow generates additional losses and voltage drop.

(2) The increased transformer loss. If the voltage of one phase is at full load and the other two are not fully loaded, the capacity of the transformer cannot be totally utilized. Working under an unbalanced situation for a long time will cause a transformer overheating, reducing its service life.

(3) When the system has an unbalanced voltage, the relay protection will not be able to obtain the normal voltage information, or the obtained voltage information is incorrect causing the relay protection malfunction.

(4) Reducing the motor efficiency. The negative sequence component produced by the three-phase unbalance generates the rotating field in the reverse direction to the positive one and hence will have a braking effect acting on the motor shaft. As a result, the output power of the motor is reduced

3.2.2 The International Definition and Standard for Unbalance

For a three-phase system, when the amplitudes of the line or the phase voltages and the currents are not the same or the phase angles are offset, this situation is called three-phase unbalance. There are three communities providing three different definitions of voltage/current unbalance. These are stated as below:

(1) The National Equipment Manufacturer's Association (NEMA) Definition [14]:

This definition is based on the line voltage, the equation is shown as:

$$ratio = \frac{v_{lmax}}{v_{lavg}} * 100\% \tag{3.1}$$

where the v_{lmax} is the maximum deviation from the average value of the line voltage v_{lavg}.

(2) The IEEE Definition [15]:

The IEEE definition focuses on the phase voltage, the equation is shown as:

$$ratio = \frac{v_{pmax}}{v_{pavg}} * 100\% \tag{3.2}$$

where the v_{pmax} is the maximum deviation from the average value of the phase voltage v_{pavg}.

(3) The Definition most widely used [16]:

This definition expresses the three-phase unbalanced voltage into two parts: the positive sequence and the negative sequence parts by the Fortescue principle, and evaluates the ratio between the negative to the positive sequences as given by (3.3)

$$ratio = \frac{v^-}{v^+} * 100\% \tag{3.3}$$

where the v^+ is the positive sequence voltage and the v^- is the negative sequence voltage. In this thesis, this definition is used to measure the degree of unbalance in either voltage or current.

The American National Standard for the Electric Power Systems and the Equipment ANSI C84.1 [17] recommends that the maximum allowable voltage unbalance should be 3% for the supply systems under the no-load conditions. However, the National Equipment Manufacturer's Association (NEMA) [14] has a more stringent requirement that the voltage unbalance should be limited to lower than 1%. Therefore, the factors such as the equipment and the environment in different locations should be carefully considered, and then reasonable restrictions should be given.

3.3 Reference Current Generation Methods

For the unbalanced current cancellation by a STATCOM, the negative sequence element in the line current needs to be extracted. This is then set as the reference signal in the current control loop together with the reactive current when the power factor control is also required. Hence, one of the key techniques for the unbalanced current mitigation is to generate the reference current by separating the positive and the negative sequence components from the measured unbalanced load current, and extracting the negative sequence element. Its reverse replica can be generated by the STATCOM to offset the unbalanced component in the load current. Two different methods; the DDSRF and the low-pass filter methods are described below.

3.3.1 Decoupled Double Synchronization Reference Frame (DDSRF) Method

The basic principle of the DDSRF is as follows: The three-phase unbalanced current and voltage at the load end can be decomposed into three symmetrical groups; the positive-sequence, the negative sequence and the zero-sequence phasors, so that the problem of controlling an unbalanced power system can be transformed into dealing the balanced variables. Taking the unbalanced three-phase voltage as an example, by applying Fortescue's theorem, it can be expressed by the three symmetrical phasors as given by (3.4).

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = v_p \begin{bmatrix} sin(\omega t + \varphi_p) \\ sin(\omega t - \frac{2}{3}\pi + \varphi_p) \\ sin(\omega t + \frac{2}{3}\pi + \varphi_p) \end{bmatrix} + v_n \begin{bmatrix} sin(-\omega t + \varphi_n) \\ sin(-\omega t + \frac{2}{3}\pi + \varphi_n) \\ sin(-\omega t - \frac{2}{3}\pi + \varphi_n) \end{bmatrix} + v_0 \begin{bmatrix} sin(\omega t + \varphi_0) \\ sin(\omega t + \varphi_0) \\ sin(\omega t + \varphi_0) \end{bmatrix} \tag{3.4}$$

where the phase angles of the two voltage sequences, $+\omega t$ and $-\omega t$, can be identified separately by applying the Phase Locking Loop (PLL) using the voltage at the point of common coupling where the STATCOM is connected as the reference frame. They are then applied, respectively, to transform the +ve and the -ve sequence voltages, into their equivalent d-q elements. The corresponding equation is shown below:

$$\begin{bmatrix} v_d^{+1}(k) \\ v_q^{+1}(k) \end{bmatrix} = \begin{bmatrix} v_{Rd}^{+1}(k) \\ v_{Rq}^{+1}(k) \end{bmatrix} + \begin{bmatrix} cos(2\omega t) & sin(2\omega t) \\ -sin(2\omega t) & cos(2\omega t) \end{bmatrix} \begin{bmatrix} v_{Rd}^{-1}(k) \\ v_{Rq}^{-1}(k) \end{bmatrix} \tag{3.5}$$

$$\begin{bmatrix} v_d^{-1}(k) \\ v_q^{-1}(k) \end{bmatrix} = \begin{bmatrix} v_{Rd}^{-1}(k) \\ v_{Rq}^{-1}(k) \end{bmatrix} + \begin{bmatrix} cos(2\omega t) & -sin(2\omega t) \\ sin(2\omega t) & cos(2\omega t) \end{bmatrix} \begin{bmatrix} v_{Rd}^{+1}(k) \\ v_{Rq}^{+1}(k) \end{bmatrix} \tag{3.6}$$

The +ve d-q pair rotates at $+\omega$ and the –ve at $-\omega$. These d-q voltage elements contain not only the DC and high order harmonic components, but also the significant 2ω oscillatory cross coupling terms between the +ve and the -ve sequence

voltages, which need to be eliminated. A decoupling network, described in [18], enables the decoupling of the negative sequence effect on the positive sequence voltage and visa versa. Thus the +ve and -ve sequence d-q voltage elements $v_{Rd}^{\pm 1}(k)$ and $v_{Rq}^{\pm 1}(k)$ can be finally obtained through (3.7) and (3.8).

$$\begin{bmatrix} v_{Rd}^{+1}(k) \\ v_{Rq}^{+1}(k) \end{bmatrix} = \left[F\right] \left(\begin{bmatrix} v_{d}^{+1}(k) \\ v_{q}^{+1}(k) \end{bmatrix} - \begin{bmatrix} cos(2\omega t) & sin(2\omega t) \\ -sin(2\omega t) & cos(2\omega t) \end{bmatrix} \begin{bmatrix} v_{Rd}^{-1}(k) \\ v_{Rq}^{-1}(k) \end{bmatrix} \right) \tag{3.7}$$

$$\begin{bmatrix} v_{Rd}^{-1}(k) \\ v_{Rq}^{-1}(k) \end{bmatrix} = \left[F\right] \left(\begin{bmatrix} v_{d}^{-1}(k) \\ v_{q}^{-1}(k) \end{bmatrix} - \begin{bmatrix} cos(2\omega t) & -sin(2\omega t) \\ sin(2\omega t) & cos(2\omega t) \end{bmatrix} \begin{bmatrix} v_{Rd}^{+1}(k) \\ v_{Rq}^{+1}(k) \end{bmatrix} \right) \tag{3.8}$$

where $\left[F\right] = \begin{bmatrix} LPF(s) & 0 \\ 0 & LPF(s) \end{bmatrix}$ and the LPF(s) in it represents the low pass filter and the cut-off frequency is set lower than 628.3rad/s eliminating the harmonics greater or equal to the double fundamental frequency. The control diagram of the DDSRF is shown in Fig.3.1.

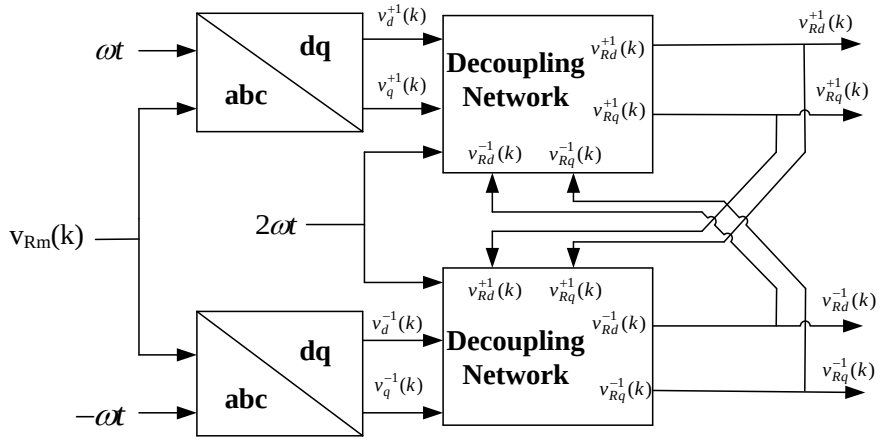

Figure 3.1: The schematic diagram of the DDSRF

3.3.2 Low Pass Filter Method

The reference [19] proposed a method based on the low-pass filter for extracting the reference signals under the unbalanced situation. In this case, the unbalanced three phase voltage/current is transformed into the d-q reference frame through the park transformation. The d component, $v_d(k)$, contains not only the fundamental positive sequence element, $v_d^{+1}(k)$, which is a DC value, but also the AC elements comprising the negative sequence component at the angular frequency 2ω oscillatory cross coupling terms and the high frequency harmonics. The AC components, $v_{Rhd}(k)$ and $v_{Rhq}(k)$, can be extracted by using the low-pass filters. Taking the unbalanced receiving end voltage as an example again, the control diagram is shown in Fig.3.2

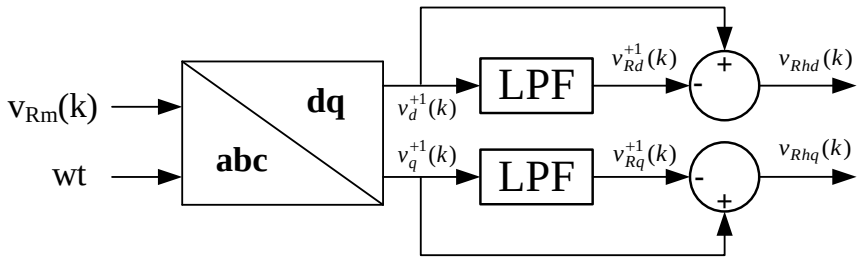

Figure 3.2: The schematic diagram of the low-pass filter method

This method requires less computational effort compared to that needed by the DDSRF method. However, the output variables from this process contain not only the negative sequence element at 2ω rad/sec but also many higher order harmonics in the d-q axes. Moreover, In this method, the cut-off frequency of the low pass filter should be set close to 0 rad/s for passing only the DC component, hence, resulting in a longer time delay for the whole control system.

3.4 Inter Cluster Voltage Balancing Methods for MMCC STATCOM

A critical issue in using MMCC-STATCOMs for power quality control is maintaining the balance of the module capacitor voltages. Lacking common dc-links, the capacitors in the cascaded modules are isolated from each other, making it difficult to exchange the power between each sub-modules [20]–[22] and between the phase arms [23]–[25]. This causes the module capacitor voltages to drift away from their nominal level, disrupting normal operation or even causing the device damage. This intra-cluster voltage imbalance can be counteracted within one phase arm by the closed-loop average capacitor voltage control and adjustment of the PWM schemes. However, when the MMCC-STATCOM compensates the unbalanced loading of the utility grid, the module capacitor voltage imbalance can be worsened. This is due to the STATCOM supplying the negative sequence current to the grid for mitigating the unbalanced loads which cause the active power imbalance between its phase arms. To solve this problem, several methods will be presented in this subsection by adding the desired zero sequence voltage, the negative sequence voltage or the combination of the zero sequence voltage and the negative sequence current.

3.4.1 Zero Sequence Voltage Injection Method

The countermeasures have been developed for the star-connected MMCC-STATCOM, the conventional approach is to introduce a sinusoidal zero sequence voltage at the neutral point, hence shifting the neutral point to a non-zero voltage level [1], [2], [26]–[28]. The effect of this is to eliminate the phase power differences caused by the negative sequence current flowing through the phase arms, and bring about a uniform active power distribution between the three phases. A summary of the principle and the calculation procedure are described below:

Due to compensating the negative sequence element of the power line current, the PCC voltage and the STATCOM phase current are the sums of the +ve and –ve elements expressed as

$$V_{Sm} = v_p sin(\omega t + \varphi_{vp} - k\frac{2\pi}{3}) + v_n sin(-\omega t + \varphi_{vn} - k\frac{2\pi}{3}) \tag{3.9}$$

$$I_{Cm} = i_p sin(\omega t + \varphi_{ip} - k\frac{2\pi}{3}) + i_n sin(-\omega t + \varphi_{in} - k\frac{2\pi}{3}) \tag{3.10}$$

where the k=0, 1, 2 for m = a, b, c respectively. The subscriptions p and n represent, separately, the positive and the negative sequence component. The active power imbalance is caused by the products of the positive current/voltage and the negative voltage/current. To eliminate these power terms (which are oscillatory), the zero sequence voltage is injected. Hence, the STATCOM per phase voltages become:

$$V_{Cm} = v_p sin(\omega t + \varphi_{vp} - k\frac{2\pi}{3}) + v_n sin(-\omega t + \varphi_{vn} - k\frac{2\pi}{3}) + v_0 sin(\omega t + \varphi_0) \tag{3.11}$$

Multiplying (3.10) and (3.11), the power flowing into per phase limb of the STATCOM can be obtained as:

$$\begin{aligned} P_{cm} = \frac{1}{2}(&v_p i_p cos(\varphi_{vp} - \varphi_{ip}) + v_n i_n cos(\varphi_{vn} - \varphi_{in}) \\ &- v_p i_n cos(\varphi_{vp} + \varphi_{in} + k\frac{2\pi}{3}) - v_n i_p cos(\varphi_{vn} + \varphi_{ip} + k\frac{2\pi}{3}) \\ &+ v_0 i_p cos(\varphi_0 - \varphi_{ip} + k\frac{2\pi}{3}) - v_0 i_n cos(\varphi_0 + \varphi_{in} - k\frac{2\pi}{3})) \end{aligned} \tag{3.12}$$

Excluding the balanced active power terms $v_p i_p cos(\varphi_{vp} - \varphi_{ip})$ and $v_n i_n cos(\varphi_{vn} - \varphi_{in})$ since they add to zero, the unbalanced power terms only have four parts and the sum of them should be zero. Hence:

$$P^0_{cm} = 2P_{cm} - (-v_p i_n cos(\varphi_{vp} + \varphi_{in} + k\frac{2\pi}{3}) - v_n i_p cos(\varphi_{vn} + \varphi_{ip} + k\frac{2\pi}{3})) \tag{3.13}$$

In (3.13), P_{cm} is the instantaneous per phase active power obtained by the P+I controller with the error between the reference per phase capacitor voltage and the measured per phase capacitor voltage which is shown in Fig.3.3. The zero sequence voltage needs to be evaluated at every sampling instant using the measured voltage and current to ensure (3.13) hold. This is performed by the following; the three phase-active-powers due to the zero sequence voltage are transformed into the $\alpha-\beta$ coordinate as:

$$\begin{bmatrix} P^0_{c\alpha} \\ P^0_{c\beta} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} P^0_{ca} \\ P^0_{cb} \\ P^0_{cc} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix}\begin{bmatrix} v_0 cos\varphi_0 \\ v_0 sin\varphi_0 \end{bmatrix} \tag{3.14}$$

where the $A_{11} = i_p cos\varphi_{ip} - i_n cos\varphi_{in}, A_{12} = i_p sin\varphi_{ip} + i_n sin\varphi_{in}, A_{21} = -i_p sin\varphi_{ip} + i_n sin\varphi_{in}, A_{22} = i_p cos\varphi_{ip} + i_n cos\varphi_{in}$.

The zero sequence voltage can be expressed as:

$$\begin{bmatrix} v_0 cos\varphi_0 \\ v_0 sin\varphi_0 \end{bmatrix} = \frac{2}{i_p^2 + i_n^2}\begin{bmatrix} A_{22} & -A_{12} \\ -A_{21} & A_{11} \end{bmatrix}\begin{bmatrix} P^0_{c\alpha} \\ P^0_{c\beta} \end{bmatrix} \tag{3.15}$$

And the magnitude and the phase angle of the zero sequence voltage can be given as:

$$v_0 = \sqrt{(v_0 cos\varphi_0)^2 + (v_0 sin\varphi_0)^2} \tag{3.16}$$

$$\varphi_0 = arctan(\frac{v_0 sin\varphi_0}{v_0 cos\varphi_0}) \tag{3.17}$$

The control diagram for the zero sequence voltage calculation is shown by the block diagram in Fig.3.3. The three phase power due to the zero sequence voltage

required to eliminate the phase power imbalance is derived from the per phase dc average-voltage control.

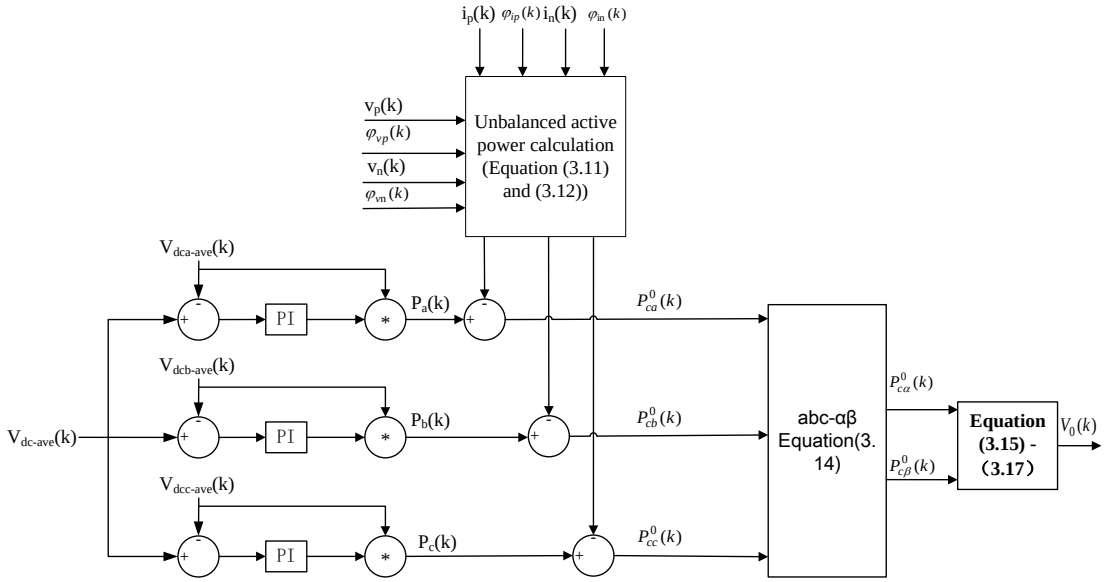

Figure 3.3: The block diagram for the zero sequence voltage calculation

However, such a scheme is problematic since the injected zero-sequence voltage can cause the converter phase voltages to exceed their rated levels under higher load imbalance, hence operating in an over-modulation mode or even becoming uncontrollable. The methods such as adding the third order harmonics can reduce the peak value of the zero sequence voltage, but with a limited effect. As shown in [29], the peak phase-voltage reduction obtained is only about 12%, this has given an increased compensation range to the maximum load imbalance ratio from about 58% up to only 65%.

3.4.2 Negative Sequence Voltage Injection Method

Injecting negative sequence voltage on the converter phase reference voltages has also been suggested to realize redistribution of the phase active power in MMCC-STATCOM [3], [4], [30]. The (3.11) should be changed as

$$V_{Cm} = v_p sin(\omega t + \varphi_{vp} - k\frac{2\pi}{3}) + v_n sin(-\omega t + \varphi_{vn} - k\frac{2\pi}{3}) + \delta v_n sin(\omega t + \varphi_{\delta vn} - k\frac{2\pi}{3}) \tag{3.18}$$

where the δv_n and the $\varphi_{\delta vn}$ are the amplitude and the phase angle of the added negative sequence voltage. Hence, the active power compensating for the capacitor voltage balancing caused by the added negative sequence voltage P_{cm}^{-1} can be expressed as

$$P_{cm}^{-1} = \delta v_n i_n cos(\varphi_{\delta vn} - \varphi_{in} + k\frac{2\pi}{3}) - \delta v_n i_p cos(\varphi_{\delta vn} - \varphi_{ip} + k\frac{2\pi}{3}) \tag{3.19}$$

Using a similar method given from (3.15) to (3.17), the amplitude and the phase angle of the negative sequence voltage can be obtained. In the reference [31], the three phase power caused by the added negative sequence voltage can be transformed into the d-q reference frame instead of the $\alpha - \beta$ coordinate. This negative sequence voltage injection method is mainly for dealing with the condition of the grid voltage sag. Because it uses the negative sequence voltage which cannot be absorbed into the neutral point, a negative sequence current must be injected into the transmission line so that the load unbalanced current can be compensated.

3.4.3 Negative Sequence Current and Zero Sequence Voltage Injection Method

A technique using both the negative-sequence current and the zero-sequence voltage was also proposed for the MMCC-STATCOM [32]. Therefore, the phase voltage and current equation can be changed as:

$$V_{cm} = v_p sin(\omega t + \varphi_{vp} - k\frac{2\pi}{3}) + v_n sin(-\omega t + \varphi_{vn} - k\frac{2\pi}{3}) + \delta v_0 sin(\omega t + \varphi_{\delta 0}) \tag{3.20}$$

$$I_{Cm} = i_p sin(\omega t + \varphi_{ip} - k\frac{2\pi}{3}) + i_n sin(-\omega t + \varphi_{in} - k\frac{2\pi}{3}) + \delta i_n sin(-\omega t + \varphi_{\delta in} - k\frac{2\pi}{3}) \tag{3.21}$$

where the δv_0, $\varphi_{\delta 0}$, δi_n and $\varphi_{\delta in}$ are the amplitude and the phase angle of the added zero sequence voltage and the negative sequence current respectively.

Under this situation, the active power imbalance will be compensated using three phase power by the added zero sequence voltage and the negative sequence current. Injection of the zero sequence voltage can reduce the burden of the negative sequence current for the capacitor voltage balancing so that the current asymmetry of the power grid can be improved. In addition, compared with the zero sequence voltage injection only method, the output negative sequence current can extend the compensation range for more serious power grid fault conditions. However, this method still cannot cope with the load imbalance since the negative sequence current is inevitably injected into the transmission line. In conclusion, to compensate the unbalanced load current, the zero sequence voltage injection method is the most effective for the MMCC-STATCOM to realize the capacitor voltage balancing.

3.5 Model Predictive Control for Modular Multilevel Converter

The model predictive control is a powerful tool to control modular multilevel converters. Its advantages include improving dynamic response performance, ease to design and the robust in dealing with the system parameter variation. Most prominently, the MPC can set multiple objectives within its cost function to achieve the optimal solution, this is particularly beneficial to the MMCC-STATCOM control since this topology requires the output current to track its reference value whilst

the sub-module voltages must be within the rated level. There are multiple MPC schemes which are shown in Fig.3.4. In general, an MPC contains two parts; a model of the MMCC+load for the output current prediction and a cost function to be minimized. The predictive model equations, generally discrete time form, can be expressed in the d-q frame for the double vector control (DVC) or in the a-b-c frame directly. In terms of cost function minimization, there are different optimization algorithms either to search for the optimal converter reference voltages or for switching vectors. These can be categorized into the finite control set-MPC (FCS-MPC) [6]–[8], [33]–[35] and the continuous control set-MPC (CCS-MPC) [9]–[13] which is also named as the modulated model predictive control (MMPC) based on the discrete or the continuous control signals. The FCS-MPC can be further divided into the optimal switch states-MPC (OSS-MPC), the optimal voltage level-MPC (OVL-MPC) and the dual-stages MPC as shown in Fig.3.4.

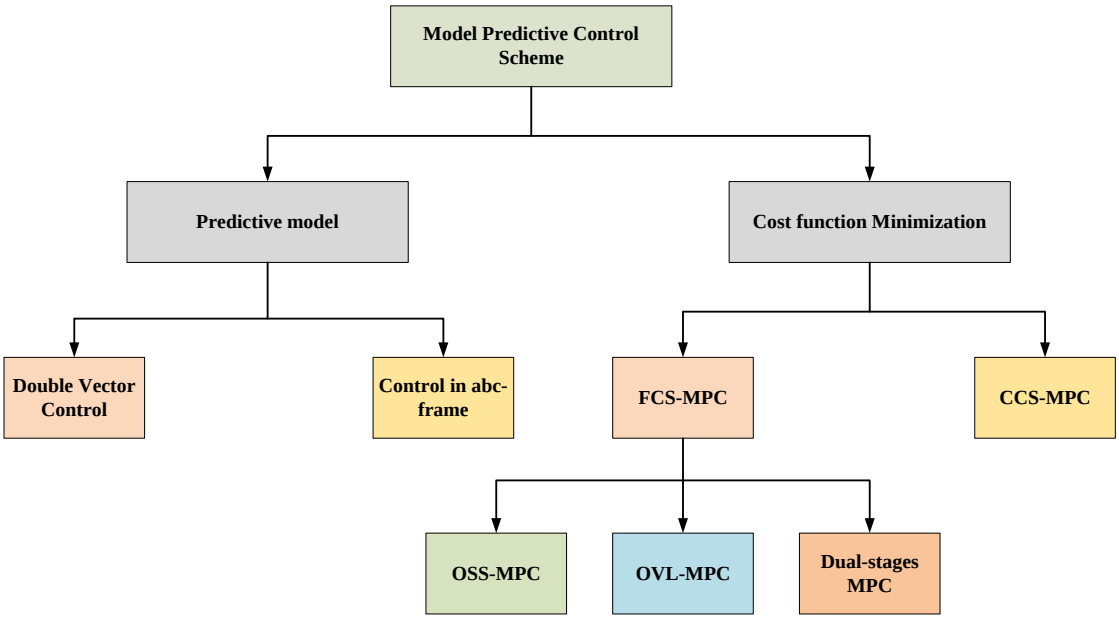

Figure 3.4: The different types of the MPC Control Schemes

To explain in detail the principle of one of the MPC schemes, a simple example, as given in Fig.3.5, is considered. Assuming a FACTs device, with voltage v_c,

is connected in series in a power line with the sending side voltage v_S and the receiving end voltage v_R. The transmission line impedance is set as $R_S + j\omega L_S$. The current flowing from the sending to the receiving ends is i_S. Applying the MPC scheme, the control objective is to evaluate the reference compensation voltage v_c^*, such that the line current can be controlled to follow the required value i_S^* continuously regardless of the line disturbances and the impedance changes. The implementation of the MPC can be as follows.

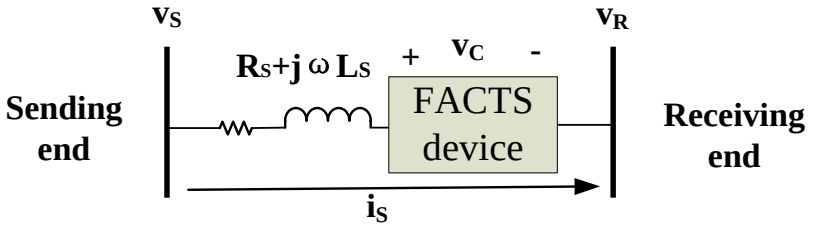

Figure 3.5: The example model for the current control strategies

3.5.1 Predictive Model

The model developed below is applied to all MPC schemes for the MMCCs. According to the KVL, the equation for the per phase current of the system in Fig.3.5 is expressed as:

$$\overrightarrow{V_S} - \overrightarrow{V_R} - \overrightarrow{V_C} = R_S\overrightarrow{I_S} + L_S\frac{\overrightarrow{I_S}}{dt} \tag{3.22}$$

Assuming the sample time T_S is negligibly small, using the discrete time model, the current vector at the (k+1)th sample instant can be predicted using (3.20):

$$i_S(k+1) = T_S\frac{v_S(k) - v_R(k) - v_C(k) - R_S i_S(k)}{L_S} - i_S(k) \tag{3.23}$$

where the $v_C(k)$ is unknown to be estimated. Now the system in Fig 3.5 is an unbalanced three-phase, we can use either the d-q frame or the a-b-c frame. If

the former is applied using the DVC [5] which employs the d-q co-ordinate to control the current and voltage in both the positive and the negative sequence, the predictive model equations are given as:

$$i_{Sd}^{+1}(k+1) = T_S \frac{v_{Sd}^{+1}(k) - v_{Rd}^{+1}(k) - v_{Cd}^{+1}(k) - R_S i_{Sd}^{+1}(k)}{L_S} - i_{Sd}^{+1}(k) + \omega L_S i_{Sq}^{+1}(k) \quad (3.24)$$

$$i_{Sq}^{+1}(k+1) = T_S \frac{v_{Sq}^{+1}(k) - v_{Rq}^{+1}(k) - v_{Cq}^{+1}(k) - R_S i_{Sq}^{+1}(k)}{L_S} - i_{Sq}^{+1}(k) - \omega L_S i_{Sd}^{+1}(k) \quad (3.25)$$

$$i_{Sd}^{-1}(k+1) = T_S \frac{v_{Sd}^{-1}(k) - v_{Rd}^{-1}(k) - v_{Cd}^{-1}(k) - R_S i_{Sd}^{-1}(k)}{L_S} - i_{Sd}^{-1}(k) - \omega L_S i_{Sq}^{-1}(k) \quad (3.26)$$

$$i_{Sq}^{-1}(k+1) = T_S \frac{v_{Sq}^{-1}(k) - v_{Rq}^{-1}(k) - v_{Cq}^{-1}(k) - R_S i_{Sq}^{-1}(k)}{L_S} - i_{Sq}^{-1}(k) + \omega L_S i_{Sd}^{-1}(k) \quad (3.27)$$

where the $\omega L_S i_{Sq}^{+1}(k)$, $\omega L_S i_{Sd}^{+1}(k)$, $\omega L_S i_{Sq}^{-1}(k)$ and $\omega L_S i_{Sd}^{-1}(k)$ are the cross coupling terms for respective the positive and the negative terms. For the unbalanced control, the zero sequence element needs to be considered. Hence the number of equations becomes 5. Meanwhile, these positive and negative sequence currents and voltages all need to be extracted from the original measured values through multiple DDSRF blocks. Clearly, the computational burden of this strategy is high and may result in poor dynamic performance.

On the other hand, if the a-b-c frame is used, the predictive model equation similar to (3.23) can be used, but with zero voltages $v_0(k)$ added to the count for the non-zero neutral point voltage due to the unbalanced condition, thus the current at (k+1) is as below

$$i_{Sm}(k+1) = T_S \frac{v_{Sm}(k) - v_{Rm}(k) - v_{Cm}(k) - R_S i_{Sm}(k)}{L_S} - i_{Sm}(k) \quad (3.28)$$

where the m=a,b,c. Clearly, with only three equations, this model form is easier than that using the DVC in the d-q coordinate. Thus this model form is preferred and applied in the published work.

Compared to the zero sequence voltage injection method presented in the sub-section 3.4.1, (3.28) enables evaluating the desired zero sequence voltage without involving the complicated calculations using (3.9)-(3.17). Moreover, the DDSRF procedures in Sub-section 3.3.1 for deriving the positive and the negative sequence voltages and currents are no longer required, since the current prediction by (3.28) uses the measured phase voltages and currents. This reduces the computational cost. The derivation of the reference current $i_S^*(k+1)$ requires the reference current at the kth sample instant and through a reference extrapolation process which will be presented in the Sub-section 3.5.4

Once obtained the (k+1)th sample reference current, a cost function is defined as the least square principle, minimizing the sum of the squared errors between the reference and the predictive current by evaluating the MMCC phase voltages. The MPC cost function can be set to achieve the simultaneous minimization of the multiple objectives, for example, the sub-module capacitor voltage balancing can be included. In this case, a weighting factor λ should be set for each control objective in the cost function. The λ value determines the importance of the respective control objective. Thus for the three-phase system in Fig. 3.5, the same cost function is defined for each phase and the total cost function for the system is the sum of three cost functions given as

$$\begin{aligned} J(k) = & \sum_{m=a,b,c} \left\{ \left(I_{Sm}(k+1) - I_{Sm}^*(k+1) \right)^2 \right\} \\ & + \lambda \sum_{m=a,b,c} \left\{ \left(V_m^{\Sigma}(k+1) - V_m^{\Sigma *}(k+1) \right)^2 \right\} \end{aligned} \tag{3.29}$$

where the $V_m^{\Sigma *}(k+1)$ are the reference values of the sum of the capacitor voltages

per phase. The λ is the weighting factor for the capacitor voltage balancing part. Then this cost function minimization becomes d quadratic problem to be solved.

3.5.2 Methods for Cost Function Minimization

As shown in Fig.3.4, there are FCS-MPC and CCS-MPC, and they are explained below.

3.5.2.1 FCS-MPC

This minimizes the cost function by searching for the discrete converter switching states and the following three methods are considered.

(1) The OSS-MPC: this is one of the finite control set model predictive control which is designed for identifying the optimal switching states. The control block diagram is shown in Fig.3.6.

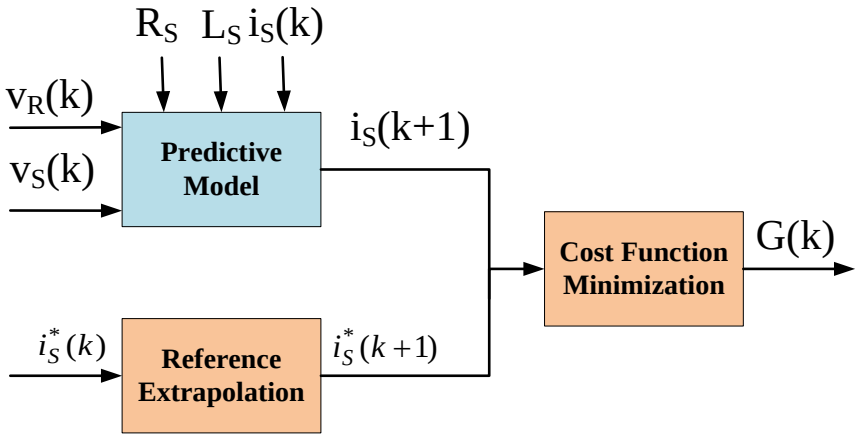

Figure 3.6: The control block diagram of the OSS-MPC

The two blocks on the left-hand side of Fig.3.6 are for the predictive model and the reference current extraction respectively, their outputs are applied to the cost function minimization block. In this block, the unknown voltage vector, $v_C(k)$, for the converter control can be replaced by the voltage values evaluated from the

2^{3*2M} combinations of switching states, the M is the number of the sub-modules in one phase. This approach is named the exhaustive method. Each switching state gives a cost function J(k) value. Finally, the one which gives the minimum cost function result can be found and the corresponding switch states are considered as the control signals G(k) which is applied to control modular multilevel converter switches. It is clear that during one sample period, only one control signal is used for the MMCC so that the OSS-MPC has a fixed frequency leading to the deterioration of the steady-state and the dynamic performance. With a total of the 2^{3*2M} switching states, it means that increasing the number of sub-modules would dramatically increase the computational burden of the system. Hence this is not an efficient control scheme for the model predictive control.

(2) The OVL-MPC: For this scheme, the aim of the cost function minimization is to derive the optimal voltage level. Its control block diagram is shown in Fig.3.7. In this way, if the submodule topology is the H-bridge converter, only $(2M+1)^3$ switching combinations need to be tested in the cost function. Then the optimal voltage level S(k) will be used in a sorting algorithm as shown in Fig. 3.7. The right-hand-side block determines the number of sub-modules that need to be bypassed. The aim of this sorting algorithm is to balance the sub-module capacitor voltages in each phase. It ranks the sub-modules according to their voltage magnitude in either ascending or descending the order and the lowest several sub-modules will be charged first. Finally, the sorting algorithm applies the desired control signals G(k) to the MMCC switches. Compared with the OSS-MPC, the computational burden of this scheme is improved significantly. However, the fixed frequency problem is still existing. Moreover, the optimal voltage level S(k) must be discrete and integer so that the steady-state performance is generally poor.

(3) The dual-stages MPC: This is another FCS-MPC that minimizes the objectives in two stages. The control block diagram is in Fig.3.8. The first stage evaluates

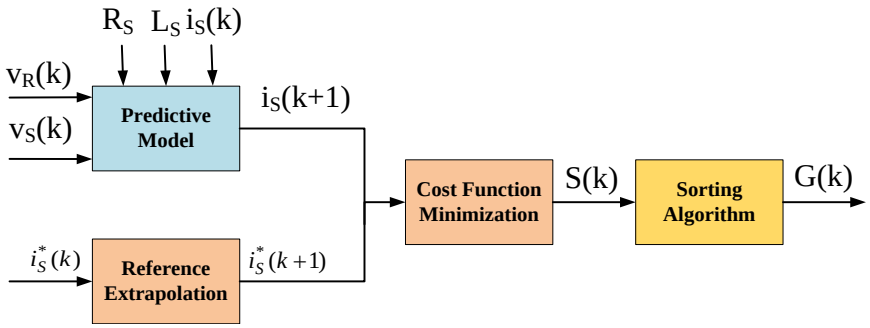

Figure 3.7: The control block diagram of the OVL-MPC

the optimal converter voltage level through the discrete current predictive model equations. This stage is mainly focused on the output current tracking. The optimal voltage obtained is given in the second stage.

The second stage (R-H-S of Fig.3.8) aims to achieve the sub-module capacitor voltage balancing. Without using the sorting algorithm, another optimization procedure is applied in this stage. This uses a discrete-time sub-module circuit equation for predicting the sum of capacitor voltages per phase at the (k+1)th instant. The cost function is defined as the squared sum of phase voltage errors between the predicted and the reference voltage values. All combinations of switch states are used in the SM cost function minimization to derive the optimal switch state as the control signals G(k).

In this MPC method, stage one has $(2N+1)^3$ possible options, whereas stage two is evaluated for the maximum switch states of $C^N_{N/2}$ when N is even or $C^N_{(N+1)/2}$ when N is odd [33]. This method has a higher computational burden than the OVL-MPC. However, it gives better dynamic performance because of the elimination of the voltage balance approach in the OVL-MPC.

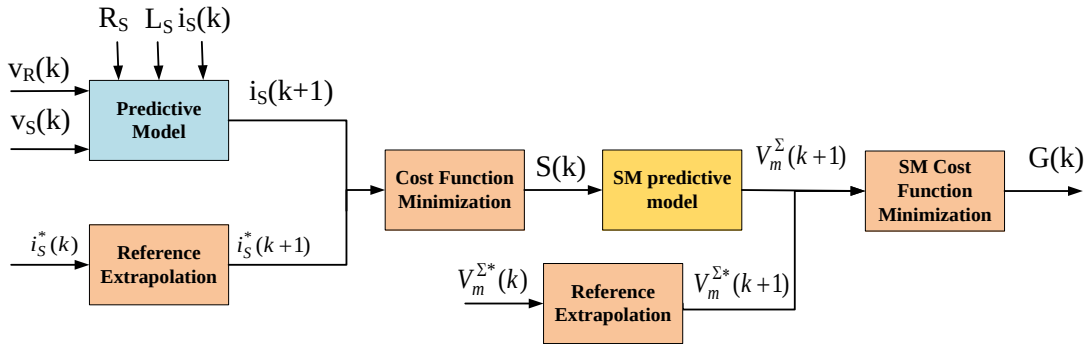

Figure 3.8: The control block diagram of the dual stages MPC

3.5.2.2 CCS-MPC

The schematic block diagram for this scheme is given in Fig.3.9. Similar to the OVL-MPC, the cost function minimization aims to calculate the optimal converter voltage level. However, it replaces the sorting algorithm with the PWM using the resultant optimal voltage level which is a continuous value. Therefore, the CCS-MPC has a fixed switching frequency which can result in better dynamic and steady-state performance compared to the FCS-MPC.

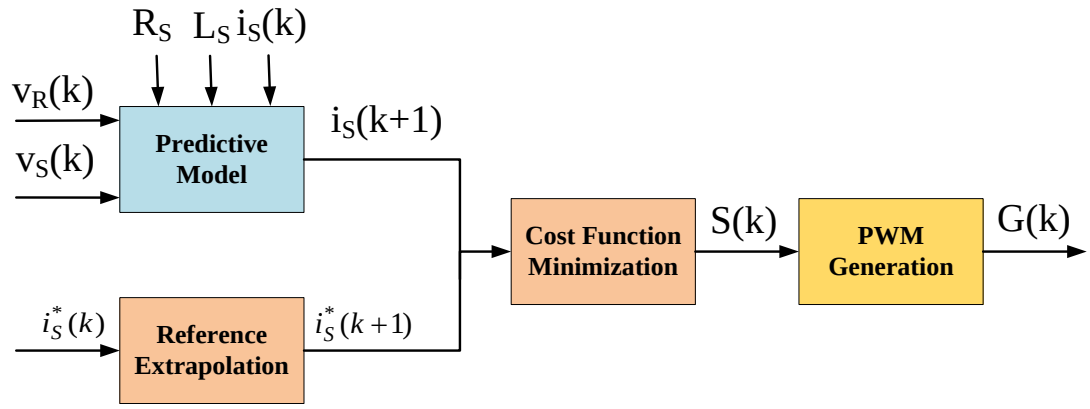

Figure 3.9: The control block diagram of the CCS-MPC

For this control algorithm, no exhaustive switching state searching discussed in the FCS-MPC is involved, the continuous optimization algorithm is required.

Hence, the Jacobian matrix is introduced for locating the optimal switching for the cost function minimization. The related equations are shown:

$$\frac{\partial J(k)}{\partial v_{Cm}(k)} = 0 \tag{3.30}$$

The $v_{Cm}(k)$ can be expressed as the product of switch duty ratios $d_m(k)$ and the DC source voltage. Since for the PWM generation, we have $d_m(k) = v^*_{Cm}(k)/v_{dcm}(k)$ where the $v^*_{Cm}(k)$ is the desired per phase output voltage and the $v_{dcm}(k)$ is the per phase capacitor voltage of the FACTS device.

The benefit of using the Jacobian matrix is that the optimal voltage level can be derived directly in one sampling period by solving the equation without trying $(2N+1)^3$ discrete options which can significantly reduce the computational burden. In fact, the Jacobian matrix can be used in the OVL-MPC while the results need to be rounded in one sampling period leading to the reduced computational burden without affecting the steady-state performance.

3.5.3 Constraint Optimization by Novel Branch & Bound Method

When using the CCS-MPC, the duty ratios $d_m(k)$ for the PWM can be estimated, and this is a constrained variable with its value limited within $-1 \le d_m(k) \le 1$. This makes cost function minimization a constrained optimization problem. To deal with such a problem, the Karush-Kuhn-Tucker (KKT) [36] method, an old-fashioned method, has been reported which gives a set of sufficient conditions for optimizing the cost function. More sufficient conditions can increase the complexity of the optimization process which is not easy to calculate. The Interior-Point (IP) [37] and active-set [38] schemes are also well-known but they all require performing multiple iterative procedures which can be computationally costly.

A novel Branch & Bound method is proposed by the author to deal with the constrained minimization of the cost function defined by (3.29). The method evaluates the per phase switching duty ratio by combining the discrete step searching and the continuous optimization solver. Its rationale is simple by dividing the switch duty cycle of one phase into several equal sections which can be called branches, within its upper and lower boundaries, one can apply the continuous control variable evaluation principle to estimate the optimal switching duty cycles for the other two phases within that set branch bound. The estimation of the optimal duty ratio may be based on quadratic minimization by using the Jacobian Matrix.

For example, for the three-phase converter in Fig. 3.5, the duty cycle for any phase can be divided into five equal branches within -1 and +1 boundaries with a gap of 0.5 between two adjacent ones. Hence five branches for one phase are -1, -0.5, 0, 0.5 and 1. Subsequently, for each of these five branches, the optimal duty cycle values for the other two phases can be evaluated by applying the standard Jacobian matrix. The results, thus, obtained can then be applied back into the cost function to evaluate the optimal duty ratio for the original phase. This procedure is performed for five different bounds, hence deriving five sets of duty ratios. Finally, by comparing the cost function values obtained for each branch, the one giving the minimum value is chosen to be applied to the converter.

3.5.4 Reference Extrapolation

Applying MPC requires reference current at the (k+1)th sample, $i_S^*(k+1)$, for the cost function evaluation, as shown by the Left-Hand-Side block in Fig. 3.6–3.9. The methods for deriving the kth sample reference current have been explained in sub-section 3.3, through the DDSRF. For evaluating the reference current at the (k+1)th sample which is none sinusoidal, the Lagrange Extrapolation [39] can be applied. The principle of the Lagrange Extrapolation states that if a certain

physical quantity is observed in practice and the corresponding observed values are obtained in several different places, the Lagrange extrapolation method can find a polynomial that takes the observed value exactly at each observed point. This polynomial is named the Lagrange polynomial. Given a set of k points which are (0,y_0),(1,y_1)...(k,y_k),y_k is the result of reference current at the kth instant $i_S^*(k)$, the Lagrange polynomial can be expressed as:

$$i_S^*(x) = \sum_{j=0}^{k} y_j l_j(x) \tag{3.31}$$

where the $l_j(x)$ is the basis polynomial which is shown as:

$$l_j(x) = \prod_{i=0, i\neq j}^{k} \frac{x-i}{j-i} \tag{3.32}$$

Hence, assuming there are four reference values which are known as $i_S^*(k)$, $i_S^*(k-1)$, $i_S^*(k-2)$ and $i_S^*(k-3)$, each basis polynomial can be obtained by (3.32) as shown below.

$$\begin{aligned} l_k(x) &= \frac{(x-k+1)(x-k+2)(x-k+3)}{1*2*3} = \frac{(x-k+1)(x-k+2)(x-k+3)}{6} \\ l_{k-1}(x) &= \frac{(x-k)(x-k+2)(x-k+3)}{-1*1*2} = \frac{(x-k)(x-k+2)(x-k+3)}{-2} \\ l_{k-2}(x) &= \frac{(x-k)(x-k+1)(x-k+3)}{-2*(-1)*1} = \frac{(x-k)(x-k+2)(x-k+3)}{2} \\ l_{k-3}(x) &= \frac{(x-k)(x-k+1)(x-k+2)}{-3*(-2)*(-1)} = \frac{(x-k)(x-k+1)(x-k+2)}{-6} \end{aligned} \tag{3.33}$$

To estimate the reference current value at the (k+1)th instant, the (3.31) can be adjusted as:

$$\begin{aligned} i_S^*(k+1) = \sum_{j=k-3}^{k} y_j l_j(k+1) &= i_S^*(k) l_k(k+1) + i_S^*(k-1) l_{k-1}(k+1) \\ &+ i_S^*(k-2) l_{k-2}(k+1) + i_S^*(k-3) l_{k-3}(k+1) \end{aligned} \tag{3.34}$$

Using the values from the present and the previous samples, the formula for the current prediction at the (k+1) is finally shown as:

$$i_S^*(k+1) = 4i_S^*(k) - 6i_S^*(k-1) + 4i_S^*(k-2) - i_S^*(k-3) \tag{3.35}$$

If the reference current is a sinusoidal value and the current control is performed using the a-b-c stationary frame, according to the sinusoidal wave characteristic, the current extrapolation formula shown below can be used to derive the reference values at the (k+1) sample.

$$\begin{bmatrix} i_{Sa}(k+1) \\ i_{Sb}(k+1) \\ i_{Sc}(k+1) \end{bmatrix} = D(\omega T_s) \begin{bmatrix} i_{Sa}(k) \\ i_{Sb}(k) \\ i_{Sc}(k) \end{bmatrix} \tag{3.36}$$

where $D(\omega T_s)$

$$= \frac{2}{3} \begin{bmatrix} cos(\omega T_s) & -\frac{1}{2}cos(\omega T_s - \frac{\pi}{3}) & -\frac{1}{2}cos(\omega T_s + \frac{\pi}{3}) \\ -\frac{1}{2}cos(\omega T_s + \frac{\pi}{3}) & cos(\omega T_s) & -\frac{1}{2}cos(\omega T_s - \frac{\pi}{3}) \\ -\frac{1}{2}cos(\omega T_s - \frac{\pi}{3}) & -\frac{1}{2}cos(\omega T_s + \frac{\pi}{3}) & cos(\omega T_s) \end{bmatrix}$$

3.6 Summary of the Key Points of the Published Paper

The paper presents a novel modulated Model-Predictive Control (MMPC) scheme for the Modular Multilevel Cascaded Converter-based STATCOMs (MMCC-STATCOM) to compensate the unbalanced load current and regulate the reactive power flow. The key contributions of the work can be detailed as follows:

(1) A common mode voltage (CMV), v_{n0}, is applied on each phase-voltages of the star-connected MCC current model given as (in Section 3.7.2)

$$\frac{dI_{cm}}{dt} = \frac{1}{L_f} \times \left(V_{cm} - V_{gm} + V_{n0} - R_f I_{cm}\right) \tag{3.37}$$

$$V_{n0} = -\frac{V_{ca} + V_{cb} + V_{cc}}{3} \tag{3.38}$$

This results in a natural injection of a non-sinusoidal voltage to the star-connected converter neutral point. The adequate v_{n0} value can maintain the three phase cluster voltage balanced. The phase voltage imbalance is due to the unequal phase power flowing caused by the MMCC- STATCOM compensating unbalanced power line current v_{n0} evaluated is shown containing a fundamental frequency element and the harmonics which can extend the operating ranges of the MMCC STATCOMs when used for the negative sequence current compensation.

(2) The predictive models for both phase current and phase voltage (Section 3.7.2 of paper) are derived, making the cost function a combination of two objectives; minimizing three-phase current errors and obtaining three phase voltage balancing, by controlling the switch duty ratios $S_m(k)$, and is defined as (Section 3.7.3)

$$\begin{aligned} J(k) = & \sum_{m=a,b,c} \left\{ \left(I_{cm}(k+1) - I^*_{cm}(k+1)\right)^2 \right\} \\ & + \lambda \sum_{m=a,b,c} \left\{ \left(V^{\Sigma}_m(k+1) - V^{\Sigma *}_m(k+1)\right)^2 \right\} \\ & s.t. |S_m(k)| \le 1 \end{aligned} \tag{3.39}$$

(3) The reference current at the (k+1)th is evaluated using the DDSRF and the reference Extrapolation (Section 3.7.4) The DDSRF is used for extracting the negative sequence element of the power line measured current at the kth sample. This, together with the two reference currents estimated during the previous four samples, i.e. $i^*_S(k)$, $i^*_S(k-1)$, $i^*_S(k-2)$ and $i^*_S(k-3)$, are applied for evaluating the reference current at the (k+2)th sample using the reference extrapolation formula (3.36). The method gives an accurate estimation of the reference current for MPC.

(4) A novel Branch and Bound (B&B) algorithm is applied to optimize the per-phase switch duty ratios. The principle of this is outlined in the previous subsection and explained in detail in Section 3.7.3 of the paper.

3.7 The Published Paper

3.7.1 Introduction

Increasing use of power electronic driven loads such as electric vehicles and electric traction, and the rapid introduction of renewable energy sources in the power network, results in a growing incidence of the reactive and unbalanced load currents and harmonics. The voltage-source-based static synchronous compensator (STATCOM) [40]–[42] can be effective in dealing with these problems, especially unbalanced loads. The STATCOM development has been furthered in the last decade by using the modular multilevel cascaded converters (MMCCs) which extend the compensation applications to the medium and high voltage power grids [43]–[45]. An MMCC-STATCOM can be scaled up to generate a higher voltage without a step-up transformer, and can produce a voltage waveform with a good harmonic performance at the lower switching frequencies and with less filtering. The key elements in an MMCC-STATCOM are its sub-modules, where the most widely used topology is the single-phase three-level H-bridge converter [46]. Other well-known topologies such as the five-level flying capacitor converter (5L-FC) [47] and the five-level neutral point clamped converter [48], [49] have also been reported. Their relative merits have been investigated in terms of the manufacturing cost, the operational performance and the footprint [50].

A critical issue in using the MMCC-STATCOMs for power quality control is maintaining the balance of the module capacitor voltages. Lacking common dc-links, the capacitors in the cascaded modules are isolated from each other, making it difficult to exchange the power between levels in the sub-module stack [20]–[22] and between the phase arms [23]–[25]. This causes the module capacitor voltages to drift away from their nominal level, disrupting the normal operation or even causing the device damage. This intra-cluster voltage imbalance can be counter-

acted within one phase arm by the closed-loop average capacitor voltage control and the adjustment of the PWM schemes. However, when the MMCC-STATCOM compensates the unbalanced loading of the utility grid, the module capacitor voltage imbalance can be worsened. This is due to the STATCOM supplying the negative sequence current to the grid for mitigating the unbalanced loads which cause the active power imbalance between its phase arms. The countermeasures have been developed where, for the star-connected MMCC-STATCOM, the approach is to introduce a sinusoidal zero sequence voltage at the neutral point, hence shifting the neutral point to a non-zero voltage level [1], [2], [26]–[28]. The effect of this is to eliminate the phase power differences caused by the negative sequence current flowing through the phase arms, and bring about a uniform active power distribution between phases. However, such a scheme is problematic since the injected zero-sequence voltage can cause the converter phase voltages to exceed their rated levels under a higher load imbalance, hence operating in the over-modulation mode or even becoming uncontrollable. The methods such as adding the third order harmonics can reduce the peak value of the zero sequence voltage, but with a limited effect. As shown in [29] the peak phase-voltage reduction obtained is only about 12%, this has given an increased compensation range to the maximum load imbalance ratio from about 58% up to 65%. Injecting the negative sequence voltage on the converter phase reference voltages has also been suggested to realize the redistribution of phase active power in the MMCC-STATCOM [3], [4], [30], but this is mainly for dealing with the condition of the grid voltage sag. A technique using both negative-sequence current and zero-sequence voltage was also proposed for the MMCC-STATCOM [32]. This is specifically for operating under the power grid fault conditions but cannot cope with the load imbalance.

The MPC technique is well-known and has been widely applied for the control of modular multilevel converters, mostly for HVDC applications. In general, this

method employs a discrete-time model of the MMCC circuit to predict the output phase current. It then selects the optimal switching state which minimizes a desired cost function. The challenges of the technique can be the determination of the optimal switching state/vector from many candidates in real time. There are various schemes reported which can be categorized into the finite control set model predictive control (FCS-MPC) [6]–[8], [33]–[35] and the continuous control set model predictive control method (CCS-MPC) [9]–[13] which is also named as the modulated model predictive control (MMPC). The former relies on selecting a switching state from a finite set for the corresponding converter, combined with a sorting algorithm for balancing sub-module capacitor voltages at the next switching cycle. This method has been applied to a wide range of power converters and shown to give a high dynamic performance. However its drawbacks are in giving a variable switching frequency and a poor steady-state performance, because only one result can be output per sampling period [51]. The CCS-MPC, on the other hand, predicts the voltage control signals which are the continuous variables in one sample period and translates them into the switching vectors. The method offers the benefit of causing smaller current ripples and requires less computational effort. In terms of implementing the predicted voltage, there is also the optimal voltage level-based-MPC (OVL-MPC) [7] which uses a cost function similar to that in [6], but evaluates the desired number of the sub-modules to be inserted or bypassed in each phase arm. In addition, Pu Liu et al [8] proposed a combined grouping and sorting optimal MPC for the MMC HVDC which divides n sub-modules in each arm into m groups. By implementing the optimized MPC at a group level and then a sub-module level, the method can further reduce the computational burden. There is also a dual-stage based MPC [33] where the first stage aims to obtain the optimal voltage level and the second to select the switching states using another MPC without the sorting algorithm. For the modulation techniques, the space vector modulation

scheme is utilized for the MMC applications [11], [12] to enhance the steady state performance with a fixed switching frequency. The optimal times for three active vectors (two active vectors and one zero vector) need to be calculated for minimizing the cost function value. Different sine-triangle-based PWM techniques are also adopted in [13] for the voltage source inverters (VSIs). These give performance similar to that from the space-vector based modulation scheme, but can further simplify the computational burden. In particular, the phase-shift PWM (PS-PWM) is the most popular for its advantage in maintaining the SM voltage balance [10]

There are only a few MPC schemes dedicated to the MMCC-STATCOMs [52]–[54], but they all concentrate on compensating the reactive power under the balanced grid operation; none is for compensating the unbalance load current. The proposed MMPC method in this paper focuses on suppressing the grid unbalanced load current. It has two distinctive features; firstly, the three phase voltages applied to its model for current prediction are imposed with a common mode voltage (CMV). This gives the implemented phase voltages a natural zero-sequence element with the harmonics for bringing the symmetry to the phase active powers, and hence eliminating the drift in the phase cluster voltages. Moreover, the harmonics in the imposed CMV are found to reduce the peak converter phase voltages, so extending the range of the load imbalance compensation. Secondly, the cost function minimization is achieved by selecting the per phase switch duty ratio using a modified branch and bound (B&B) algorithm. This approach stems from the scheme in [52] which applies the space vector PWM concept and selects the switching vectors within each 60° sextant. The modified B&B, however, evaluates the optimal switch duty ratios in the $a-b-c$ coordinate. By setting any one of them in the cost function as a branch, it solves the other two by quadratic programming. It will be shown that the method is able to mitigate the unbalanced load at the ratio of up to 70% while still maintaining the phase DC-voltages balance.

The paper is structured as follows: Section 3.7.2 describes the configuration of the MMCC-STATCOM and the prediction models for the output current and the per phase DC capacitor voltage. In Section 3.7.3, the cost function and the constraints for the variables are defined. The principle of the modified branch and bound method is detailed. In Section 3.7.4, the overall control scheme is presented. Section 3.7.5 presents the experimental results which validate the proposed control scheme. Section 3.7.6 gives the conclusions.

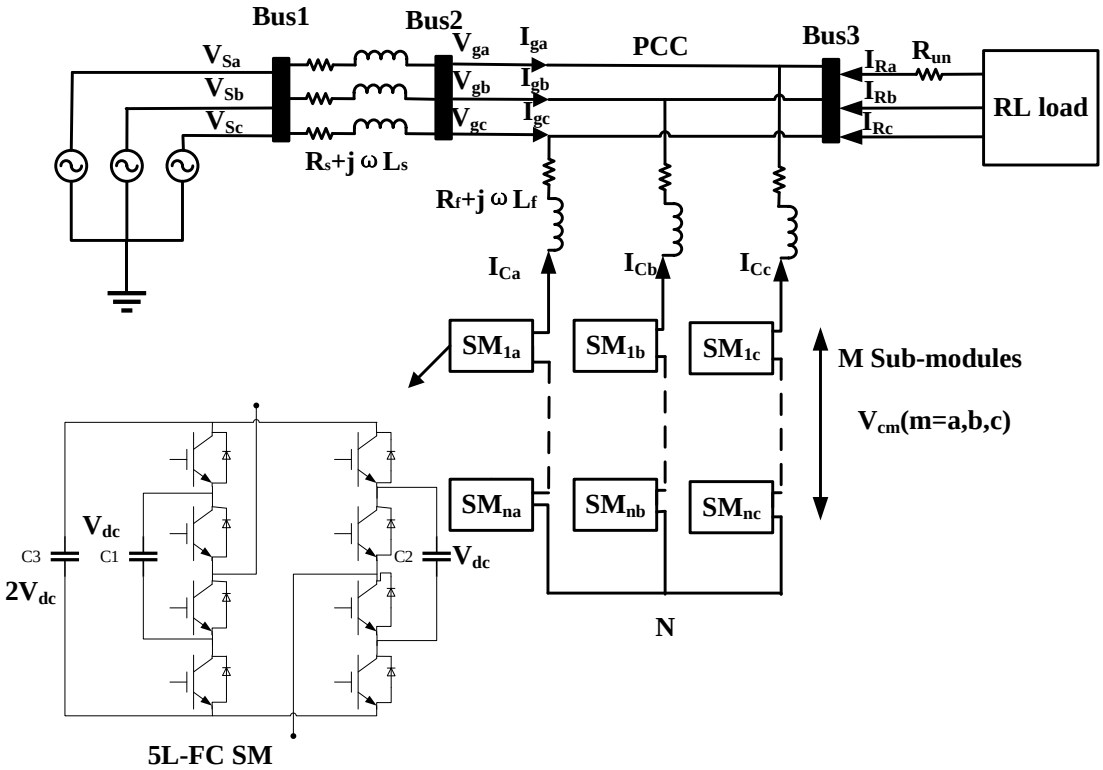

Figure 3.10: The configuration of a power system with the star-connected MMCC-STATCOM using the 5-level flying capacitor converter as sub-modules

3.7.2 Modulated Model Predictive Control with Common Voltage Injection

3.7.2.1 The Configuration of MMCC-STATCOM

The configuration of a star-connected MMCC-STATCOM is shown in Fig.3.10. Each of the three phase arms consists of M serially connected 5-Level flying capacitor converters as the sub-modules (SM) which has two inner capacitors C_1 and C_2 and one outer floating capacitor C_3. The SMs can equally be the 2-level full-bridge converters, each with a single capacitor. Each of the flying capacitor SMs can synthesize five voltage levels: 0, $\pm V_{dc}/2$, $\pm V_{dc}$. With M SM per phase arm, there are $4M+1$ voltage levels. The number of SMs in a phase arm depends on the line voltage rating and the dc capacitor voltage per module. The three phase arms are connected to the transmission lines through their filters with the impedance R_f+jwL_f, to the Bus2 which is regarded as the point of common coupling (PCC). The transmission line impedance between the supply side from Bus1 to Bus2 is R_s+jwL_s. The neutral points between the supply and the converter sides are not connected [29].

At the load end, the three-phase $R-L$ loads, R_L+jwL_L is connected. Its power factor is about 80.9%. To emulate the load imbalance condition, a single-phase variable resistor, R_{un} is added on the load of phase A.

3.7.2.2 Model for STATCOM Output Current

The MMCC-STATCOM is used to compensate the unbalanced load current as well as the reactive power within its rated power and voltage ratings. This has the benefit of making the current flow from the PCC balanced hence eliminating the adverse effect due to the load imbalance to the grid. However, supplying the unbalanced current by an MMCC-STATCOM causes the phase power imbalance,

resulting, consequently, the phase cluster DC voltages drifting away from the nominal level. The existing technique is to inject a zero sequence voltage which would not affect the grid voltage but results in a power element eliminating the unbalanced power between phases, hence preventing the phase voltage drift. To adapt the new approach, it is assumed a common mode voltage (CMV), equivalent to the zero sequence voltage at the fundamental frequency, is applied to the neutral point of the star-connected STATCOM. By applying the phase voltage balance expression, the rate of change of per phase current of the converter can be given as

$$\frac{dI_{cm}}{dt} = \frac{1}{L_f} \times \left(V_{cm} - V_{gm} + V_{n0} - R_f I_{cm}\right) \tag{3.40}$$

where the V_{cm} and I_{cm} ($m = a, b, c$) are respectively the STATCOM terminal voltage and current, while the V_{gm} is the grid side voltage, and the V_{n0} is the CMV, which can be expressed as

$$V_{n0} = -\frac{V_{ca} + V_{cb} + V_{cc}}{3} \tag{3.41}$$

Assuming the sample time T_s is significantly smaller than the time constant of the converter filter, if the converter three phase-voltages and the common mode voltage at the kth sample are known. the discrete time expression of output three phase-currents at the (k+1)th sample can be given as

$$\begin{bmatrix} I_{ca}(k+1)) \\ I_{cb}(k+1)) \\ I_{cc}(k+1)) \end{bmatrix} = \frac{T_s}{L_f} \begin{bmatrix} V_{ca}(k)) \\ V_{cb}(k)) \\ V_{cc}(k)) \end{bmatrix} - \frac{T_s}{L_f} \begin{bmatrix} V_{ga}(k)) \\ V_{gb}(k)) \\ V_{gc}(k)) \end{bmatrix} + \frac{T_s}{L_f} \begin{bmatrix} V_{no}(k)) \\ V_{no}(k) \\ V_{no}(k) \end{bmatrix} + \left(1 - \frac{R_f T_s}{L_f}\right) \begin{bmatrix} I_{ca}(k)) \\ I_{cb}(k)) \\ I_{cc}(k)) \end{bmatrix} \tag{3.42}$$

Considering the converter phase voltage V_{cm} , its maximum value equals the sum of voltages of all SMs in a phase chain, assuming that the V_m^{Σ} is the sum value of the sub-module capacitor voltages. Applying the switch duty ratio, V_{cm} relates to V_m^{Σ} and S_m as:

$$V_{cm} = S_m V_m^{\Sigma} \tag{3.43}$$

where the S_m is the duty ratio for each phase ($m = a, b, c$) and M is the number of the SM per phase arm. Since the duty ratio varies at every sample interval, the discrete time form of the CMV is given as

$$V_{n0}(k) = -\frac{\left(S_a(k)V_a^{\Sigma}(k) + S_b(k)V_b^{\Sigma}(k) + S_c(k)V_c^{\Sigma}(k)\right)}{3} \tag{3.44}$$

Substituting (3.44) into (3.42), the STATCOM current at $(k+1)th$ sample can be expressed as :

$$\begin{bmatrix} I_{ca}(k+1)) \\ I_{cb}(k+1)) \\ I_{cc}(k+1)) \end{bmatrix} = \frac{T_s}{L_f} \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{bmatrix} \begin{bmatrix} S_a(k)V_a^{\Sigma}(k) \\ S_b(k)V_b^{\Sigma}(k) \\ S_c(k)V_c^{\Sigma}(k) \end{bmatrix} - \frac{T_s}{L_f} \begin{bmatrix} V_{ga}(k)) \\ V_{gb}(k)) \\ V_{gc}(k)) \end{bmatrix} + \left(1 - \frac{R_f T_s}{L_f}\right) \begin{bmatrix} I_{ca}(k)) \\ I_{cb}(k)) \\ I_{cc}(k)) \end{bmatrix} \tag{3.45}$$

Assuming the filter parameters, L_f and R_f , are constant and the $V_m^{\Sigma}(k)$, $V_{gm}(k)$, $I_{cm}(k)$ (m=a,b,c) are the measured values at the kth sample, by adequately adjusting the $S_m(k)$, it is possible to obtain the desired STATCOM current at the $(k+1)th$ sample.

3.7.2.3 Model for Per Phase Voltage

The power flow between the grid and the MMCC-STATCOM maintains the SM capacitor voltages at the desired levels, hence the energy exchange for per STATCOM phase arm can be given as

$$\frac{1}{2}C\begin{bmatrix} V_a^{\Sigma 2} \\ V_b^{\Sigma 2} \\ V_c^{\Sigma 2} \end{bmatrix} = \int \left(\begin{bmatrix} -V_{ca} I_{ca} \\ -V_{cb} I_{cb} \\ -V_{cc} I_{cc} \end{bmatrix} \right) dt \tag{3.46}$$

where the C is the capacitance of the SM outer floating capacitor C_3.

According to (3.43), the above can be written as

$$\frac{1}{2}C\begin{bmatrix} V_a^{\Sigma 2} \\ V_b^{\Sigma 2} \\ V_c^{\Sigma 2} \end{bmatrix} = -\int \left(\begin{bmatrix} S_a V_a^{\Sigma} I_{ca} \\ S_b V_b^{\Sigma} I_{cb} \\ S_c V_c^{\Sigma} I_{cc} \end{bmatrix} \right) dt \tag{3.47}$$

Taking the derivative on both sides and simplifying the resultant formula, the rate of change of per phase total capacitor voltage is given by

$$\frac{d\begin{bmatrix} V_a^{\Sigma} \\ V_b^{\Sigma} \\ V_c^{\Sigma} \end{bmatrix}}{dt} = -\frac{1}{C}\begin{bmatrix} S_a I_{ca} \\ S_b I_{cb} \\ S_c I_{cc} \end{bmatrix} \tag{3.48}$$

Expressing above in the discrete-time form, the MMCC-STATCOM phase arm total voltages at the next sample interval can be expressed as:

$$\begin{bmatrix} V_a^{\Sigma}(k+1) \\ V_b^{\Sigma}(k+1) \\ V_c^{\Sigma}(k+1) \end{bmatrix} = -\frac{T_s}{C}\begin{bmatrix} S_a(k) I_{ca}(k) \\ S_b(k) I_{cb}(k) \\ S_c(k) I_{cc}(k) \end{bmatrix} + \begin{bmatrix} V_a^{\Sigma}(k) \\ V_b^{\Sigma}(k) \\ V_c^{\Sigma}(k) \end{bmatrix} \tag{3.49}$$

It is evident from (3.49) that the total phase voltage of the STATCOM is also adjustable by the switch duty ratio of the phase arm SMs.

3.7.3 MMPC for MMCC-STATCOM

3.7.3.1 Cost Function and Constrained Optimisation Principle

In this section, a modulated model predictive control (MMPC) method based on the $a-b-c$ framework with the common mode voltage injection is given in detail. The control objective is to ensure that the three phase currents of the MMCC-STATCOM track as well as their corresponding reference values while the fluctuations on the sum of the SM capacitor voltages per phase are minimized. This can be achieved by evaluating the optimal control variables, i.e. the switch duty ratio $S_m(k)$. However, it is worth noting that with the current reference values defined to compensate the unbalanced load current at the PCC, a CMV is imposed on each phase voltage and this may result in any one of the optimal duty ratios exceeding outside the linear modulation range, causing the MMCC over-modulation. Thus a cost function combining both current and voltage objectives, with the constraints on $S_m(k)$, is defined as

$$\begin{aligned} J(k) = & \sum_{m=a,b,c} \left\{ \left(I_{cm}(k+1) - I_{cm}^{*}(k+1) \right)^2 \right\} \\ & + \lambda \sum_{m=a,b,c} \left\{ \left(V_m^{\Sigma}(k+1) - V_m^{\Sigma *}(k+1) \right)^2 \right\} \\ & s.t. |S_m(k)| \leq 1 \end{aligned} \tag{3.50}$$

where the $I_{cm}^{*}(k+1)$ and the $V_m^{\Sigma *}(k+1)$ are the reference values of the converter current and the sum of capacitor voltages per phase. The λ is the weighting factor for the capacitor voltage balancing. The constraints on the per phase switch duty ratio ensure that the voltage variations are within the linear range.

The weighting factor λ imposes a trade-off between the current tracking accuracy and the balancing of three summed sub-module capacitor voltages. Its value is determined by trial and error. A comparative study of using different λ in the control of the experimental rig is presented in Section 3.7.5. and subsequently, the selection of its value is explained.

Without considering the common mode voltage in the cost function, the optimization method can be very similar to that presented in [38]. However, with the addition of the CMV on each of the phase voltages, the expressions for the three phase currents are different as shown in (3.45), so the minimization of the cost function (3.50) for finding the three voltage duty ratios requires considering all the three phase current simultaneously under the inequality constraints. Applying the Karush-Kuhn-Tucker (KKT) conditions [36] gives a set of sufficient conditions for optimizing the cost function (3.50), this leads to the constraints for the three duty ratios written as

$$s.t. -1 - S_m(k) \leq 0, S_m(k) - 1 \leq 0 (m = a, b, c) \tag{3.51}$$

Subsequently, according to the KKT, the Lagrangian function of (3.50) combined with (3.51) can be shown as:

$$\begin{aligned} L(k, \lambda_1, \lambda_2, \lambda_3, \lambda_4, \lambda_5, \lambda_6) = J(k) + \lambda_1(-1 - S_a(k)) + \\ \lambda_2(S_a(k) - 1) + \lambda_3(-1 - S_b(k)) + \lambda_4(S_b(k) - 1) + \\ \lambda_5(-1 - S_c(k)) + \lambda_6(S_c(k) - 1) \end{aligned} \tag{3.52}$$

Taking the phase a as an example, the errors of both current prediction and capacitor voltage balance are simplified respectively as

$$\begin{aligned} I_{ca}(k+1) - I_{ca}^{*}(k+1) &= a_1 S_a(k) + a_2 S_b(k) + P_{a1} \\ V_a^{\Sigma}(k+1) - V_a^{\Sigma *}(k+1) &= a_4 S_a(k) + P_{a2} \end{aligned} \tag{3.53}$$

where

$$a_1 = \frac{2}{3}\frac{T_s}{L_f} V_a^{\Sigma}(k), a_2 = -\frac{1}{3}\frac{T_s}{L_f} V_b^{\Sigma}(k),$$

$$a_3 = -\frac{1}{3}\frac{T_s}{L_f} V_c^{\Sigma}(k), a_4 = -\frac{T_s}{C} I_{ca}(k)$$

$$P_{a1} = -\frac{T_s}{L_f} V_{ga}(k) + \left(1 - \frac{R_f T_s}{L_f}\right) I_{ca}(k) - I_{ca}^{*}(k+1)$$

$$P_{a2} = V_a^{\Sigma}(k) - V_a^{\Sigma *}(k+1)$$

Subsequently, the J(k) part in the function (3.42) can be rewritten as:

$$\begin{aligned} J(k) = \sum_{m=a,b,c} \left\{ (m_1 S_a(k) + m_2 S_b(k) + m_3 S_c(k) + P_{m1})^2 \right\} \\ + \lambda \sum_{m=a,b,c} \left\{ (m_4 S_m(k) + P_{m2})^2 \right\} \end{aligned} \tag{3.54}$$

Note that the parameters, m_1, m_2, m_3, and P_{m1}, P_{m2} in (3.54) are given in the appendix. Hence, the KKT conditions that need to be met are as follows:

$$
\begin{aligned}
\frac{\partial L}{\partial S_a(k)} &= (a_1^2+b_1^2+c_1^2+\lambda a_4^2)\times S_a(k)+(a_1a_2+b_1b_2+\\
&\quad c_1c_2)\times S_b(k)+(a_1a_3+b_1b_3+c_1c_3)\times S_c(k)\\
&\quad +(a_1P_{a1}+b_1P_{b1}+c_1P_{c1}+\lambda a_4P_{a2})-\lambda_1+\lambda_2=0\\
\frac{\partial L}{\partial S_b(k)} &= (a_1a_2+b_1b_2+c_1c_2)\times S_a(k)+(a_2^2+b_2^2+c_2^2+\\
&\quad \lambda b_4^2)\times S_b(k)+(a_2a_3+b_2b_3+c_2c_3)\times S_c(k)\\
&\quad +(a_2P_{a1}+b_2P_{b1}+c_2P_{c1}+\lambda b_4P_{b2})-\lambda_3+\lambda_4=0\\
\frac{\partial L}{\partial S_c(k)} &= (a_3a_1+b_3b_1+c_3c_1)\times S_a(k)+(a_3a_2+b_3b_2+\\
&\quad c_3c_2)\times S_b(k)+(a_3^2+b_3^2+c_3^2+\lambda c_4^2)\times S_c(k)\\
&\quad +(a_3P_{a1}+b_3P_{b1}+c_3P_{c1}+\lambda c_4P_{b2})-\lambda_5+\lambda_6=0\\
&\quad -1-S_a(k)\le 0, S_a(k)-1\le 0, -1-S_b(k)\le 0,\\
&\quad S_b(k)-1\le 0, -1-S_c(k)\le 0, S_c(k)-1\le 0,\\
&\quad \lambda_1(-1-S_a(k))=0, \lambda_2(S_a(k)-1)=0, \lambda_3(-1-S_b(k))=0,\\
&\quad \lambda_4(S_b(k)-1)=0, \lambda_5(-1-S_c(k))=0, \lambda_6(S_c(k)-1)=0,\\
&\quad \lambda_1\ge 0, \lambda_2\ge 0, \lambda_3\ge 0, \lambda_4\ge 0, \lambda_5\ge 0, \lambda_6\ge 0
\end{aligned}
\tag{3.55}
$$

Solving the above equations with the set conditions leads to the derivations of the values $S_m(k)$ (m=a,b,c) and the λs. If one of the λs is greater than 0, the corresponding phase duty ratio should be on the boundary 1 or -1. On the other hand, when the λ is equal to 0, the derived duty ratio is the optimal value. Several optimization methods may be applied to solve this problem, including the Interior-Point (IP) [37] and the active-set [38] schemes. They all require performing multiple iterative procedures which can be computationally costly. A modified Branch and Bound (B&B) is thus proposed which can derive the optimal solution with only a finite known number of steps.

3.7.3.2 Modified Branch and Bound (B&B) Method

To evaluate the optimal switch duty ratios $S_m(k)$ $(m = a, b, c)$ for minimizing the cost function defined by (3.50), a modified branch and bound method (B&B) for the system represented by the $a-b-c$ coordinate is proposed.

The principle of the method is as follows: By selecting any one of the three control variables, namely, one phase arm's switch duty ratio and setting it as a variable within the confined range imposed by the constraint in the cost function, the cost function would now have only two variables – two switch duty ratios, as the third one is bounded as a constant. This simplifies the computation process, because the order of the derived formula for the cost function minimization is reduced to two instead of the original three. The evaluation follows a two stage bound and branch process as follows:

Stage 1: the chosen input variable is assigned to a constant within its constraint from either the lower or upper boundary. With the cost function having now two independent variables, their optimal values can be estimated by quadratic programming.

Stage 2: the two resultant optimal values are applied to replace their originals as the fixed constants in the cost function, but the first input is allowed to vary. Having only one independent variable to evaluate, the optimal cost function can be derived subsequently. This, consequently, leads to a set of the three optimal inputs and completes one branch of the B&B process.

In the following branches, the first input variable ascends or descends in constant steps until it reaches the upmost/lowest boundary. In each step, the two-stage process described above is repeated. According to the number of steps taken by the chosen first variable, there would be multiple branches, hence multiple sets of results. These results are compared after completing the final branch evaluation and the set giving the minimum cost function value will be chosen.

Applying the above principle, the switch duty ratio, $S_c(k)$, in the cost function (3.50) may be the chosen one amongst the three to form a branch. Starting from $S_c(k)$ = -1 at the lower bound, S_L , it rises at a constant step size of, say, 0.25, in each branch until reaching the upmost bound S_U=1. By setting S_c as a constant in the cost function (3.50) in each branch, the current prediction error part is simplified as given below (taking the phase a as an example).

$$I_{ca}(k+1) - I^*_{ca}(k+1) = a_1 S_a(k) + a_2 S_b(k) + n_{a1} \tag{3.56}$$

where

$$n_{a1} = a_3 S_c(k) - \frac{T_s}{L_f} V_{ga}(k) + \left(1 - \frac{R_f T_s}{L_f}\right) I_{ca}(k) - I^*_{ca}(k+1)$$

Likewise combining (3.56), the phase A voltage error can be expressed as

$$V^{\Sigma}_a(k+1) - V^{\Sigma *}_a(k+1) = a_4 S_a(k) + n_{a2} \tag{3.57}$$

where

$$n_{a2} = V^{\Sigma}_a(k) - V^{\Sigma *}_a(k+1)$$

Subsequently, the cost function (3.50) can be rewritten as:

$$\begin{aligned} J(k) = & \sum_{m=a,b,c} \left\{(m_1 S_a(k) + m_2 S_b(k) + n_{m1})^2\right\} \\ & + \lambda \sum_{m=a,b,c} \left\{(m_4 S_m(k) + n_{m2})^2\right\} \end{aligned} \tag{3.58}$$

Note that the parameters, m_1, m_2, and n_{m1}, n_{m2} in the original (3.54) and (3.58) are given in the appendix. With only $S_a(k)$ and $S_b(k)$ as the input variables, the optimal values of these parameters are obtainable by minimizing the cost function

J(S_a,S_b) and can be estimated using the Least-Square minimization algorithm. This requires taking the first order derivatives of the cost function J with respect to the two variables respectively and setting them to zero, yielding

$$\begin{aligned}\frac{\partial J(k)}{\partial S_a(k)} &= (a_1^2 + b_1^2 + c_1^2 + \lambda a_4^2) \times S_a(k) \\ &+ (a_1 a_2 + b_1 b_2 + c_1 c_2) \times S_b(k) \\ &+ (a_1 n_{a1} + b_1 n_{b1} + c_1 n_{c1} + \lambda a_4 n_{a2}) = 0\end{aligned} \tag{3.59}$$

$$\begin{aligned}\frac{\partial J(k)}{\partial S_b(k)} &= (a_1 a_2 + b_1 b_2 + c_1 c_2) \times S_a(k) \\ &+ (a_2^2 + b_2^2 + c_2^2 + \lambda b_4^2) \times S_b(k) \\ &+ (a_2 n_{a1} + b_2 n_{b1} + c_2 n_{c1} + \lambda b_4 n_{b2}) = 0\end{aligned} \tag{3.60}$$

Based on the above equations, the solutions for the two switching duty ratios can be obtained by the product of the two 2 x 2 matrices as shown below

$$\begin{bmatrix} S_a(k) \\ S_b(k) \end{bmatrix} = -A_1^{-1} A_2 \tag{3.61}$$

where

$$A_1 = \begin{bmatrix} a_1^2 + b_1^2 + c_1^2 + \lambda a_4^2 & a_1 a_2 + b_1 b_2 + c_1 c_2 \\ a_1 a_2 + b_1 b_2 + c_1 c_2 & a_2^2 + b_2^2 + c_2^2 + \lambda b_4^2 \end{bmatrix}$$

and $A_2 = \begin{bmatrix} a_1 n_{a1} + b_1 n_{b1} + c_1 n_{c1} + \lambda a_4 n_{a2} \\ a_2 n_{a1} + b_2 n_{b1} + c_2 n_{c1} + \lambda b_4 n_{b2} \end{bmatrix}$

Note that either $S_a(k)$ or $S_b(k)$ estimated from (3.61) may violate the constraint defined in (3.50), and in that case, the corresponding duty ratio needs to be clamped to its nearest boundary value.

Once the optimal $S_a(k)$ and $S_b(k)$ are obtained with a fixed $S_c(k)$, the next stage is to estimate the optimal duty ratio $S_c(k)$ while $S_a(k)$ and $S_b(k)$ in (3.50) are fixed to their newly evaluated values. In this case, $S_c(k)$ is the only parameter to

be evaluated, and this is a one-variable programming problem. The cost function (3.50) now becomes:

$$\begin{aligned} J(k) = & \sum_{m=a,b,c} \left\{ (m_3 S_c(k) + n_{m3})^2 \right\} \\ & + \lambda \sum_{m=a,b,c} \left\{ (m_4 S_m(k) + n_{m2})^2 \right\} \end{aligned} \tag{3.62}$$

where

$$\begin{aligned} n_{m3} = & m_1 S_a(k) + m_2 S_b(k) - \frac{T_s}{L_f} V_{gm}(k) + \\ & \left(1 - \frac{R_f T_s}{L_f}\right) I_{cm}(k) - I^*_{cm}(k+1) \end{aligned}$$

Taking the derivative of J($S_c(k)$) with respect to $S_c(k)$ and setting it to 0, the $S_c(k)$ is calculated as:

$$S_c(k) = -\frac{a_3 n_{a3} + b_3 n_{b3} + c_3 n_{c3} + \lambda c_4 n_{c2}}{a_3^2 + b_3^2 + c_3^2 + \lambda c_4^2} \tag{3.63}$$

where the a_3,b_3,c_3,n_{a3},n_{b3} and n_{c3} are also shown in the appendix.

Similar to the case with the estimated $S_a(k)$ and $S_b(k)$, the derived $S_c(k)$ value should not violate the set constraint, otherwise it must also be replaced with the nearest boundary value.

The switch duty ratio values for the three phase arms estimated using the aforementioned procedure may not be the global optimum. The optimization process is repeated for the next branch in which the $S_c(k)$ is fixed to a value higher or lower than its previously acquired value. With the defined constraint for the switch duty ratio and the step size setting of 0.25, there are 9 branches, resulting in the 9 sets of optimal solutions. Based on their corresponding cost function values, the one producing the minimal value among the 9 sets is selected. The flowchart of this new B&B method is shown in Fig.3.11.

It is worth noting that the branch step size of 0.25 is set by trial and error according to the criteria of both the accuracy of the final optimal solution and the

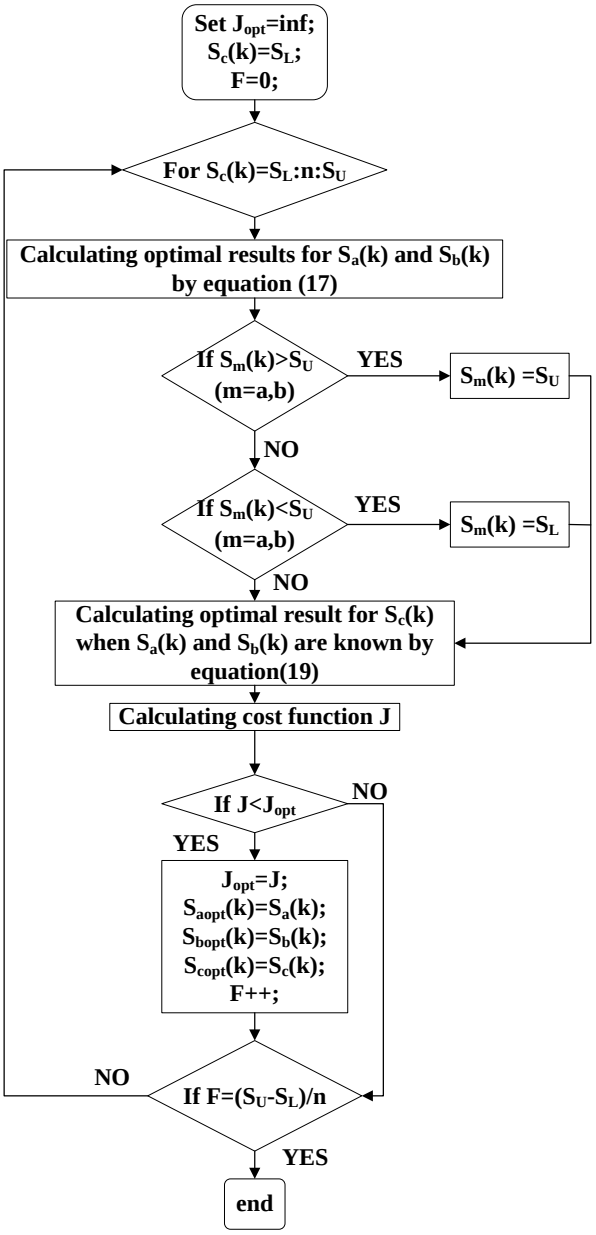

Figure 3.11: The flowchart for the modified branch and bound (B&B) method

computation efficiency. In general, the smaller the step size, the more accurate the solution obtained according to the minimum cost function value, however, the higher the number of branches and hence the higher the computational burden. Fig.3.12 depicts the cost function values evaluated using the global optimal solution

obtained when different step sizes are applied; i.e. 0.5 (black line), 0.25 (red line) and 0.1 (blue line) respectively and the unbalanced load ratio is 0.28. With only 5 branches for 0.5 step size, the black line either coincides with the other two lines or is higher than them. It can be seen that when the red line is higher than the blue line, the gap between them is not very obvious. However, 21 branches with 0.1 step size result in a computational time twice that when step size is 0.25. Thus, in this work, a step size of 0.25 is chosen for each branch which is a compromised choice between accuracy and computational cost.

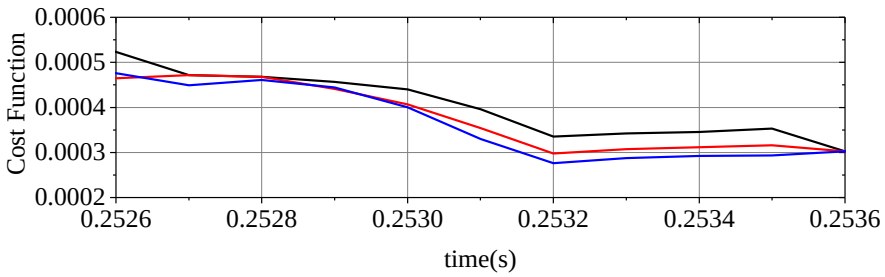

Figure 3.12: The cost function value comparison using different step size when the imbalance compensation ratio is 0.28.

3.7.3.3 Results from B&B Compared with IP Method

It is important to note that the proposed B&B with step size set to 0.25 does not prevent it from estimating the optimal solution values. Table 3.1 illustrates the evaluated optimal results for a single instance of a real time sample. It lists the three duty ratios at each of 9 bounds and the final chosen result (shown in bold) has the lowest cost function of all those obtained for this particular test. Clearly, the evaluated three duty ratios vary over the constrained range and importantly, the final optimal solution chosen is compared with the result obtained by the Interior-Point method (IP) [55], the difference in terms of the cost functions between the two methods is about 10% and the maximum difference between the estimated

three duty ratios are less than 0.02. This is deemed to be a practically acceptable result, and is obtained much more rapidly than the IP method solution.

The results from both B&B and IP methods are also shown in Table 3.2 for 4 further instances, i.e. for 4 other time instants under different operating conditions. The data listed in Table 3.2 presents a similar pattern to those in Table 3.1, the maximum average difference in the three duty ratios identified by the two methods is less than 0.05, so helping to confirm the robust results in the presence of the noise, and the sampling errors. In fact, about 100 similar instances were analyzed but cannot be listed in full. All the results have been found to be acceptably close to those from the IP method. It is also worth pointing out that no instances of the local minimum (i.e. in a region disjoint from the true optimum) were seen to occur.

Table 3.1: The phase duty ratios and the cost function values evaluated at 9 different branches by the B&B method and the results from Interior-Point Method

Branch	$S_a(k)$	$S_b(k)$	$S_c(k)$	Cost function value
S_c=-1	-0.6227	-1	-0.63434	1.329
S_c=-0.75	-1	-0.5085	-0.3733	0.6088
S_c=-0.5	-0.1240	-1	-0.3733	0.1833
S_c=-0.25	0.1154	-0.9964	-0.2519	0.05054
S_c=0	0.3748	-0.7377	-0.0022	0.05527
S_c=0.25	-0.4889	0.2476	0.6242	0.05828
S_c=0.5	0.8736	-0.2402	0.4974	0.06158
S_c=0.75	1	0.0856	0.6856	0.1
S_c=1	1	0.2573	0.8105	0.3974
Optimal value	0.1078	-1	-0.2720	0.04178

3.7.3.4 Evaluation and Comparison of the Computational Cost

The evaluations of the computational procedures are performed on both the proposed and conventional methods. To give a fair comparison, the MMPC method is also applied to the conventional method. The basic operations for both methods are

Table 3.2: The comparison of the duty ratios and the cost function values estimated by the B&B method and the interior-point (IP) method at four different samples

Sample		$S_a(k)$	$S_b(k)$	$S_c(k)$	Cost function value	Cost function error
1	B&B	-0.2886	0.0816	0.7502	0.01096	0.00651
	IP	-0.2111	0.0875	0.8252	0.00445	
2	B&B	-0.5592	-0.1340	0.4999	0.02989	0.0084
	IP	-0.5026	-0.0983	0.5545	0.02149	
3	B&B	0.2926	0.2301	-0.1950	0.01831	0.00358
	IP	0.3084	0.2054	-0.2145	0.01473	
4	B&B	0.3513	-0.7843	-0.2506	0.00370	0.00255
	IP	0.2933	-0.8007	-0.2659	0.00115	
Average error		0.0482	0.0432	0.0411		0.00526

respectively listed in Tables 3.3 and 3.4, including the comparison, the addition, the multiplication and the division, performed per sample interval. The operations which are common to both methods, such as the DDSRF, the average voltage control loop and the PS-PWM are excluded. There is a column in both tables named the pre-calculation; this counts for the computations not performed in each sample interval. It can be seen that the count for total basic operations for the proposed method is 791 which is less than that for the conventional method of 801.

Table 3.3: The expected basic operations of the proposed method

Basic operations	Pre-calculation	Per cycle calculation
Addition	24	23
Multiplication	38	43
Comparison	0	6
Division	0	3
Square	0	6

Table 3.4: The expected basic operations of the conventional method

Basic operations	Pre-calculation	Outer capacitor balancing control	Per cycle calculation
Addition	16	41	19
Multiplication	30	54	39
Comparison	0	0	6
Division	0	3	3
Square	0	0	6

3.7.4 Overall Control Scheme

The overall MMPC control scheme for an MMCC-SATCOM is shown in Fig.3.13. It has four parts: the MMPC block, phase-shifted PWM block, the intral-cluster voltage balancing control block, the reference current and the voltage generations and the delay compensator. The MMPC block is already described in section 3.7.2. The phase-shifted PWM (PS-PWM) block is well-reported in the literature and hence only a brief description is given here [56]. In this technique, multiple triangular carrier waves are applied to synthesize a three-phase sinusoidal reference signal. The number of the triangular waves is the number of SMs (for the SM being full H-bridge), in the case of the 5L-FL SMs, the number is twice that of the SMs in a phase leg. Thus with the number being M, they are phase shifted by an equal angle ($(180/2M)^\circ$) to each other. By comparing these carrier waves with two anti-phased reference sine waves, the desired switching signals can be generated. In the intra-cluster voltage balancing control block, the per phase SM capacitor voltage values, i.e. the intra-phase voltages, are maintained in balance by using the closed loop control to their average value $v^*_{dc-ave} = v^{\sum}_m/M$ which has been shown in Fig.3.14 and then applying the PS-PWM. The V_{cm1} and V_{cm2} represent the voltage values of two SM outer capacitors, C_3, in each phase ($m = a, b, c$). The last two blocks are described in detail below.

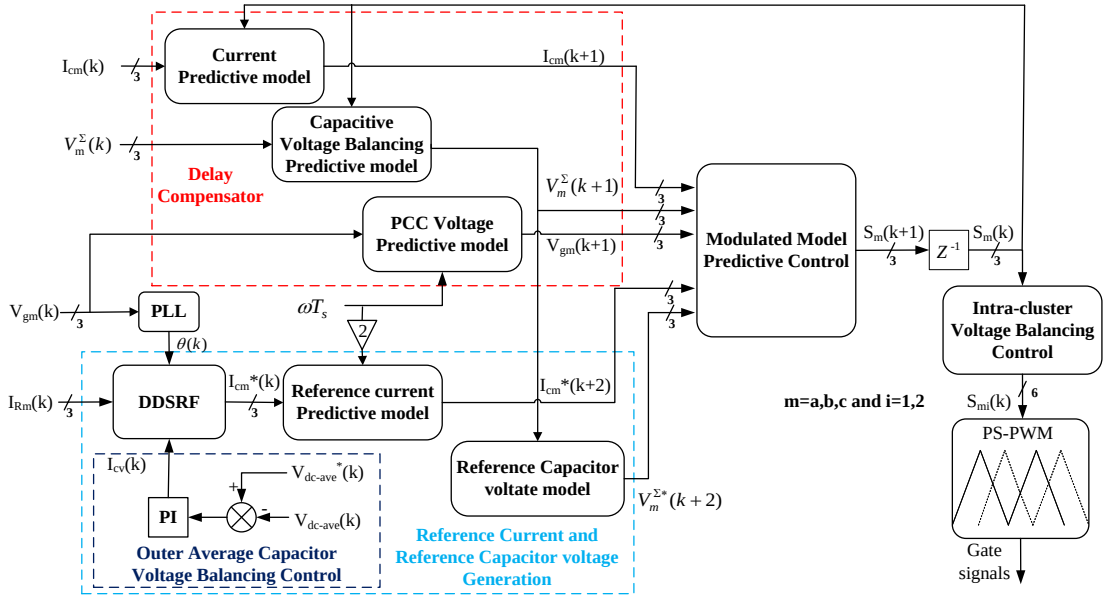

Figure 3.13: The overall control scheme of the MMPC for the MMCC-STATCOM

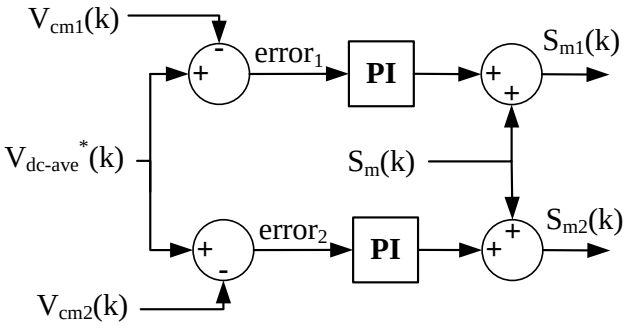

Figure 3.14: The diagram for the intra-cluster voltage balancing control block

3.7.4.1 Reference Current and Voltage Generations

For the MMPC+B&B scheme to eliminate the unbalance current and improve the power factor at the PCC, its reference current $I^{*}_{cm}(k)$, is generated by extracting both the $-ve$ sequence current components, $I^{-}_{1d}(k)$, $I^{-}_{1q}(k)$, and the reactive current $I^{+}_{1q}(k)$ from the measured load current. This can be achieved by using the Decoupled Double Synchronization Reference Frame (DDSRF) [18]. For the intra-cluster voltage balancing, a +ve sequence current element $I_{cv}(k)$, needs to be added to the

reference current. This is evaluated using the SM average voltage control block as shown in Fig.3.14. Subsequently, the reference current generated consists of $I_{1d}^{-}(k)$+$I_{cv}(k)$ and $I_{1q}(k)$. This is transformed to the $a-b-c$ stationary reference frame through the inverse Park transformation, hence given as, $I_{cm}^{*}(k)$.

For good performance control, the delay compensation, explained in the following sub-section, is applied. This reference current at the $(k+2)th$ sample, $I_{cm}^{*}(k+2)$, is estimated by multiplying $I_{cm}^{*}(k)$ with $B(2\sigma)$ which is expressed in (3.65).

With the delay compensator inserted, the average phase arm reference voltage value for the $(k+2)th$ sample should be evaluated according to their corresponding predicted values at the $(k+1)$ sample instant as

$$V_{m}^{\Sigma *}(k+2) = (V_{a}^{\Sigma}(k+1) + V_{b}^{\Sigma}(k+1) + V_{c}^{\Sigma}(k+1))/3 \tag{3.64}$$

3.7.4.2 Delay Compensator

As elaborated in the previous sub-section, the MMPC with the modified B&B algorithm predicts the converter output current and the SM capacitor voltages, and estimates the optimal switching duty ratios for all three-phase arms in the 9 calculation branches. The whole process is however complicated, making the time interval excessively long between the time instant taking the measured voltage and current at the kth sample and the instant of when the newly estimated switching signals are obtained. This is called the digital control delay and may cause inaccurate predictions of the current and voltage hence resulting in poor control performance. In this paper, a delay compensator is implemented to tackle this problem. Its effect is analogous to inserting a “state observer” for the current and the SM capacitor voltages in the MMPC loop. The scheme takes the measured converter current and capacitor voltages at the kth sample and applies the switch duty ratios, $S_{m}(k)$, to (3.45) and (3.49), to predict $I_{cm}(k+1)$, and the sum of phase

capacitor voltages, $V_m^{\Sigma}(k+1)$. It also estimates the $(k+1)th$ PCC voltages, $V_{gm}(k+1)$, expressed in the a-b-c coordinate as:

$$\begin{bmatrix} V_{ga}(k+1) \\ V_{gb}(k+1) \\ V_{gc}(k+1) \end{bmatrix} = B(\sigma) \begin{bmatrix} V_{ga}(k) \\ V_{gb}(k) \\ V_{gc}(k) \end{bmatrix} \tag{3.65}$$

where $B(\sigma)$

$$= \frac{2}{3} \begin{bmatrix} cos(\sigma) & -\frac{1}{2}cos(\sigma - \frac{\pi}{3}) & -\frac{1}{2}cos(\sigma + \frac{\pi}{3}) \\ -\frac{1}{2}cos(\sigma + \frac{\pi}{3}) & cos(\sigma) & -\frac{1}{2}cos(\sigma - \frac{\pi}{3}) \\ -\frac{1}{2}cos(\sigma - \frac{\pi}{3}) & -\frac{1}{2}cos(\sigma + \frac{\pi}{3}) & cos(\sigma) \end{bmatrix}$$

The σ is equal to ωT_s and the ω is the grid angular frequency. The predicted results at $(k+1)$ sample are then used by the MMPC+B&B algorithm to estimate the optimal switching duty ratio at the $(k+2)th$ sample which can minimize the cost function given below

$$\begin{aligned} J(k) = & \sum_{m=a,b,c} \left\{ \left(I_{cm}(k+2) - I_{cm}^*(k+2) \right)^2 \right\} \\ & + \lambda \sum_{m=a,b,c} \left\{ \left(V_m^{\Sigma}(k+2) - V_m^{\Sigma *}(k+2) \right)^2 \right\} \\ & s.t. |S_m(k+1)| \leq 1 \end{aligned} \tag{3.66}$$

3.7.5 Experimental Tests and Results

3.7.5.1 Experimental Setup

To validate and demonstrate the performance of the proposed MMPC+B&B control scheme, the experimental tests were conducted on an MMCC-STATCOM prototype (Fig.3.15) built at the Smart Grid Laboratory of the University of Leeds [57]. The configuration of the power network model constructed for testing the STATCOM's capability for the unbalanced current cancellation is as given in Fig.3.10, the PCC

bus is powered by an auto transformer (3KVA,110V) through a three-phase R-L element imitating the transmission line impedance. The parameters of the main components in the experimental setup are listed in Table 3.5.

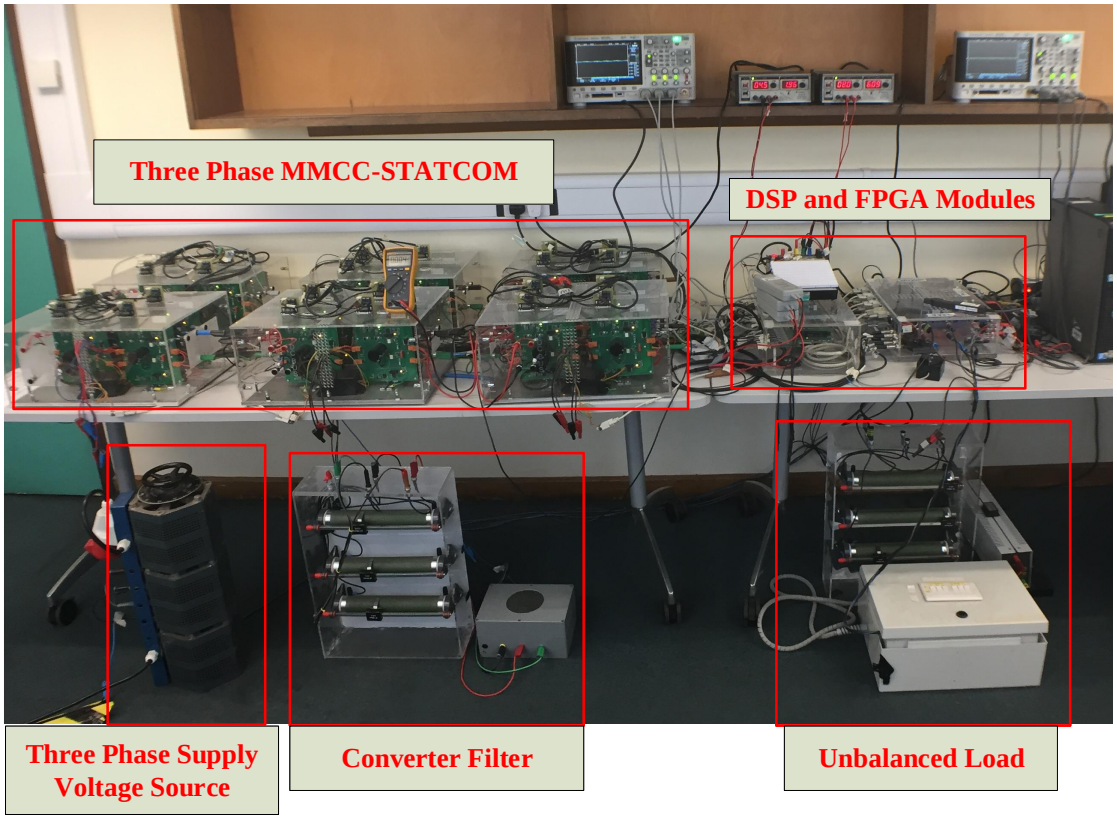

Figure 3.15: The MMCC-STATCOM prototype and the other system hardware components

The experimental MMCC-STATCOM rig is comprised of six SMs, each being a full-bridge 5L-flying capacitor converter consisting of three capacitors and 8 IGBT-Diode pairs. Two SMs are connected in series per phase, giving the 9 voltage levels. The digital device for the control unit is a combination of an ACTEL-Pro-Asic 3 FPGA module and a Texas Instrument 32-bit floating point digital signal processor (DSP-TMS320C6713). The DSP serves as the main control unit for processing all measured data to execute the MMPC+B&B control algorithm while the FPGA

implements the PS-PWM scheme. The resultant switching signals are supplied to the SMs through the fiber optic transmitter and the receiver circuits.

Table 3.5: The parameters for the experimental rig

Rated Power P_norm	1.5kVA
Rated Current I_norm	5A
Sending end voltage V_s	80V
Line frequency f	50Hz
RL filter resistance R_f	2Ω
RL filter inductance L_f	3mH
Flying capacitor SM per phase cluster M	2
Per Module Capacitor C_3	1120uF
Inner capacitor C_1 and C_2	560uF
Per Module voltage	60V
Switching frequency	1KHz

3.7.5.2 Results And Discussions

Fig.3.16 and 3.17 show the experimental results when the proposed scheme is applied to control the experimental MMCC-STATCOM, the former has the weighting factor λ setting to 0.25 and the latter as 0.49. Fig.3.18 shows the corresponding waveforms when the conventional sinusoidal zero sequence voltage injection is applied on the same experimental rig. In all three Figures, stepped lines plotted in (a) depict the levels of compensation ratio to the imbalanced load current. In this work, the unbalanced load current is fixed at K_{ir}=I^- /I^+=0.7. The unbalance compensation ratio is adjusted from 0% (between 0.0 s and 0.1 s) up to 70% at the step size of 14% per 0.1 sec. Thus in the initial period of 0 to 0.1 sec. the PCC current is unbalanced since there is no compensation. After 0.1 sec, the degree of compensation is increased gradually. The PCC currents become more balanced until the maximum 70% compensation is applied. The unbalanced compensation ratio at 0.7 is maintained from 0.5s to 0.7s in order to observe the level of the

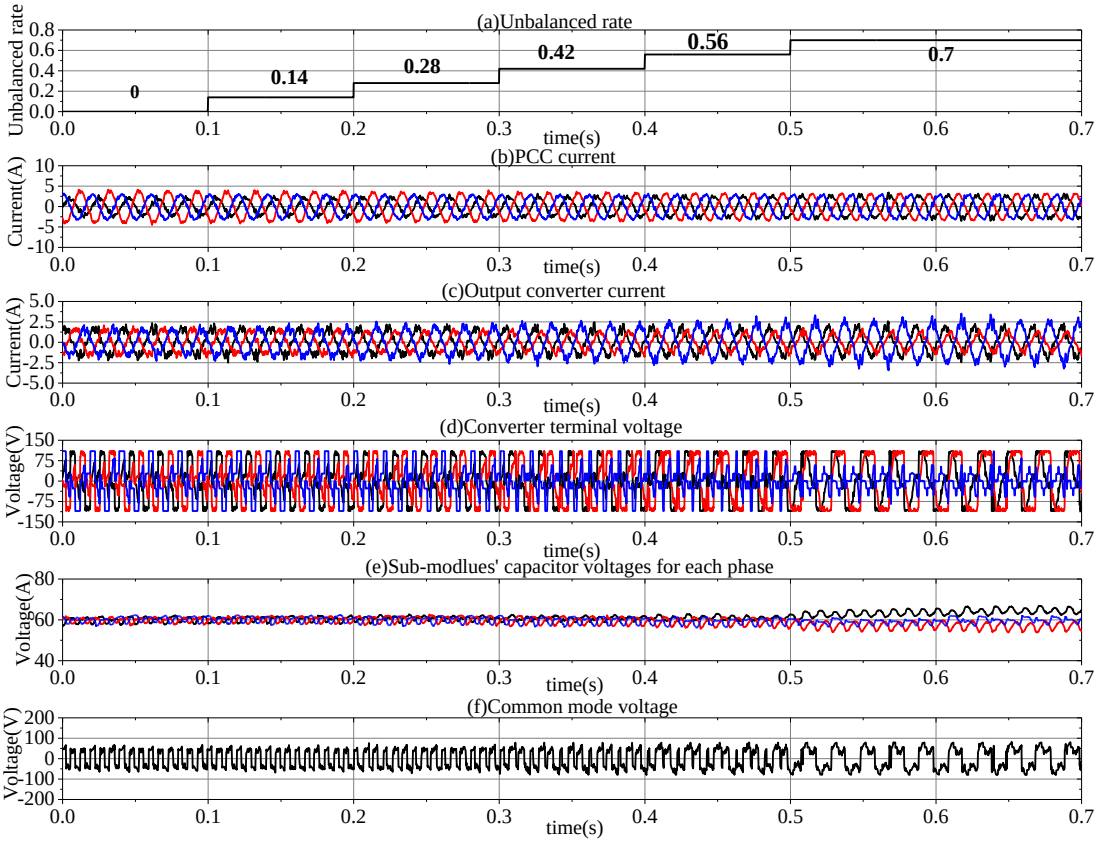

Figure 3.16: The experimental results (a) the Unbalanced rate (b) the PCC current (c) the output converter current (d) the converter terminal voltage (e) the sub-modules' capacitor voltages for each phase and (f) the common mode voltage for the proposed method when the λ= 0.25

voltage oscillations away around the average sub-module capacitor voltages.

The performance of the MMPC+B&B algorithm can be observed from the PCC current waveforms shown in Fig. 3.16 (b) and 3.17 (b). From no compensation applied (0 s to 0.1 s) to 70% of the current imbalance compensation, it is evident that the degree of the PCC current imbalance is reduced gradually to near complete the elimination during period 0.5s to 0.7s. The three-phase current waveforms supplied by the MMCC to the grid are displayed in Fig. 3.16 (c) and 3.17 (c), it can be seen that the degree of the converter current imbalance increases with the escalation of the required level of the compensation, but they are all within the

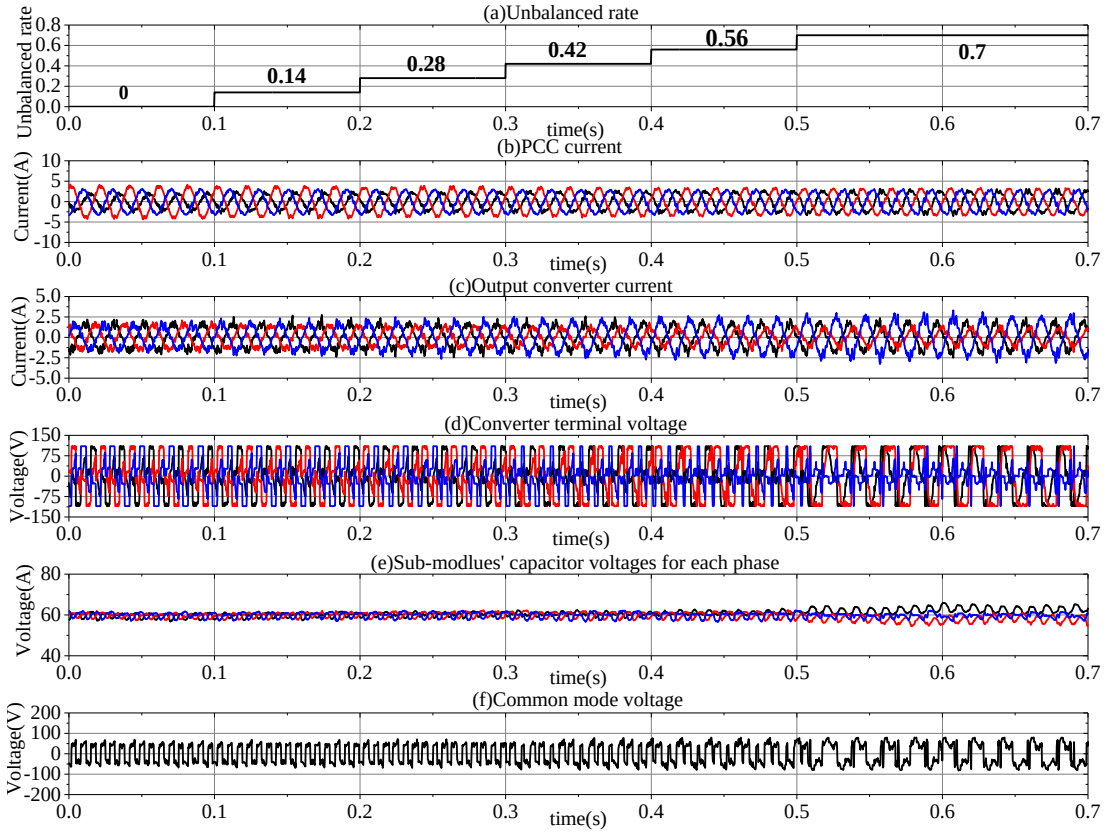

Figure 3.17: The experimental results (a) the Unbalanced rate (b) the PCC current (c) the output converter current (d) the converter terminal voltage (e) the sub-modules' capacitor voltages for each phase and (f) the common mode voltage for the proposed method when the λ= 0.49

rated limit. Likewise, the terminal phase voltages of the MMCC are also within the rated level without the over-modulation. Fig. 3.16 (e) and 3.17 (e) display the three-phase sub-modules capacitor average voltages which are well balanced even when the compensation level is set to 56%, the low voltage fluctuation with the peak-peak value of about 6V (10% of the rated capacitor voltage) is shown before the time instant 0.5s. The voltage deviations grow slightly during the final 0.2s interval when the compensation level is as high as 70%. However, the adverse effect of this condition to the control performance is minimal, the system still maintains the stable operation with the PCC current being well balanced.

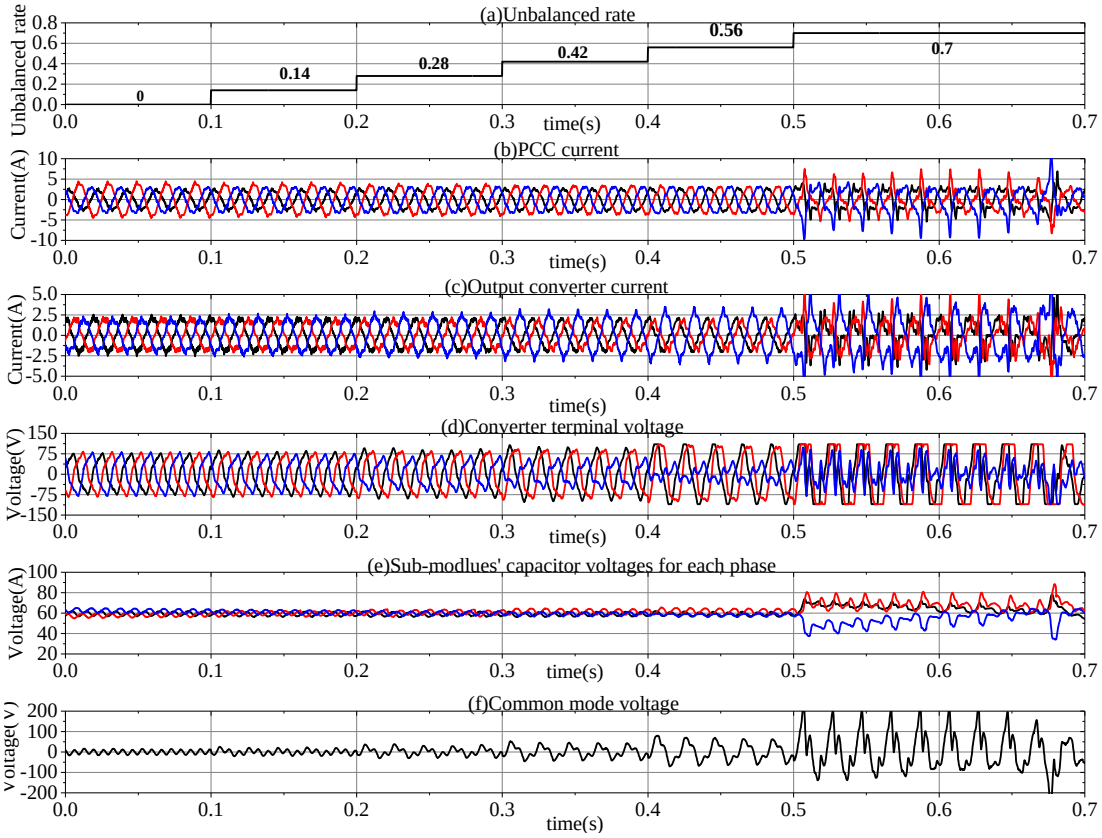

Figure 3.18: The experimental results (a) the unbalanced rate (b) the PCC current (c) the output converter current (d) the converter terminal voltage (e) the sub-modules' capacitor voltages for each phase and (f) the common mode voltage for the conventional zero sequence voltage injection method

It is worth noting that the weighting factor value affects the performance of the compensation. When the weighting factor is 0.49, the degree of the capacitor voltage deviation is lower than that when the value is 0.25. However, for the reduced weighting factor, the performance in the unbalanced current compensation is better. When the weighting factor is 0.49, the maximum difference between the peak values of the three PCC phase currents is about 0.5A, higher than that with the weighting factor being 0.25 which is 0.3A, This means that the unbalanced ratio after the compensation is higher than its counterpart when the weighting factor is 0.49. In terms of the common mode voltage (the zero sequence voltage), as

shown in Fig. 3.16 (f) and 3.17 (f), the peak values for both cases are always around 60V, so none presents the over-modulation problem.

The above results are compared with those shown in Fig. 3.18 where the conventional method using the zero sequence voltage injection for the inter-cluster voltage balance is applied. In this case, to extend the MMCC STATCOM voltage range, the zero sequence voltage injected is composed of a sinusoidal fundamental element plus two third harmonics; one has the magnitude of 1/6 of its main fundamental component and the other's magnitude is 1/6 of the positive sequence component of the converter terminal voltage.

As can be seen the waveforms up to t=0.5s when the compensation ratio is 0.56 (see Fig.3.16, 3.17 and 3.18) are stable for both methods. However, as the load imbalance compensation ratio is increased to a higher level of 0.7, the performance of the controlled PCC current waveforms from the conventional method deteriorates as shown in Fig. 3.18 (b). This is due to increasing the negative sequence current for mitigating the load imbalance, which adversely increases the phase active power imbalance. However, the zero sequence voltage injected is insufficient to eliminate the phase power differences even though the magnitude of its fundamental element has increased significantly (Fig. 3.18 (f)). Consequently, the phase voltages drift away from their nominal levels as seen in Fig. 3.18 (e), resulting in the system becoming uncontrollable. In contrast, the results from the proposed control scheme, depicted in Fig. 3.16 and 3.17, show that the common mode voltage magnitude does not show a noticeable increment but its spectra change significantly for eliminating the phase power imbalance. This in turn prevents the phase voltages from drifting apart hence enabling the effective cancellation of the unbalanced load current. Thus the proposed MMPC has shown that it allows the STATCOM to compensate higher level of the load unbalances compared to the conventional method.

To explore the advantage of the MMPC+B&B algorithm, the frequency spectra

of the common mode voltages derived by the FFT analysis are compared as shown in Fig. 3.19 and 3.20 when the unbalanced ratio is set to 0.42. It can be seen clearly from Fig.3.19 (a) and (b) that the odd harmonics dominate the other frequency components. In particular, the magnitude of the third harmonic exceeds that of the fundamental element, and other odd harmonics, for example, when the λ= 0.25, 5th and 7th order harmonics are about 40% and 75% of the fundamental respectively. For the λ= 0.49, there are about 35% of 5th and 70% of 7th harmonics existing in the common mode voltage waveform. In contrast, the dominant components in the zero sequence voltage obtained from the conventional method (Fig.3.20) are only the fundamental and the 3rd harmonic elements, with the magnitude of the 3rd harmonic being below 40% of the fundamental frequency. This confirms that the proposed method is capable of making use of the harmonic components for the power balance between phases hence achieving superior performance for the unbalanced current mitigation. Furthermore, the peak amplitude of the fundamental element in the CMV for the period between 0.3s to 0.4s is as low as 27.42V when the λ= 0.25 and that for the λ= 0.49 is 29.34V, whereas, for the conventional method, the magnitude is a lot higher reaching 40.35V, hence the proposed method offers a higher level of the unbalanced current compensation without pushing the MMCC terminal voltages into the over-modulation range.

3.7.5.3 Weighting Factor Selection

As stated the weighting factor, λ, is determined by trial and error depending on the requirements of the converter current control accuracy, according to the PCC current THD factor, the levels of the three-phase capacitor voltage deviations, and the voltage ripple percentages. It is clear that setting a higher weighting factor imposes a tighter limit on the voltage deviation levels while compromising the PCC current control performance, hence resulting in its THD value being

increased. Conversely, a lower weighting factor would result in better current control, and hence the lower PCC phase current THD values, but the constraints on the phase voltage deviations are weakened. With the high phase voltage deviations reaching the extent that one phase voltage drifts away, the system will become uncontrollable.

To demonstrate clearly the effect of the λ on the control of the PCC current and the sub-module capacitor voltage balance, a test was performed on the MPC control scheme, for the STATCOM operating under the unbalanced PCC current condition. The λ varies from low at 0.016 to high at 0.81 with step size 0.1. Table 3.6 lists the corresponding PCC current THD values, the maximum voltage ripple percentages, and the differences between the summed sub-module capacitor voltages per phase.

Clearly, at high λ (0.81), the PCC current THD value is higher at 3.57% while the sub-module capacitor voltage ripple is the lowest at 7.7% and the voltage deviation is low (0.74 V). As the λ decreases, the control on the PCC current improves by steadily reducing the THD values. However, the sub-module capacitor voltage balance control is weakened, causing increases in both the sub-module capacitor percentage voltage ripples and the phase voltage deviations. As the λ is reduced further to 0.16, the three phase capacitor voltages cannot be maintained at the balanced levels. As shown in Fig.3.21, the three phase voltages drift continuously in different directions, so that one phase voltage pushes the MMC STATCOM into the over-modulation range. This is referred to as “out of range” in Table 3.6 since the sum of the capacitor voltages in one phase leg becomes higher than the maximum allowed value (80V).

Fig.3.22 (a) and (b) show the variations of the sums of sub-module capacitor voltages with the λ=0.25 and 0.49 respectively. For both cases, the compensation ratio is 70% and the time of the test is from 0 sec to 0.9 sec. It can be seen clearly that there is no occurrence of uncontrolled phase voltage drift in either case.

However, with the λ value of 0.25, the differences of the summed phase capacitor voltages differences are larger, which implies a weaker voltage balance control performance. After the repeated tests, the proposed λ value = 0.49 is chosen as a good compromise between maintaining the balance of the summed sub-module capacitor voltages and giving a good current control performance with a low enough THD value.

Table 3.6: The results for different weighting factors

Weighting factor	PCC current THD	Sub-module capacitor voltage ripple percentage	Sub-module capacitor voltage deviation
0.81	3.57%	7.7%	0.74V
0.64	3.52%	8%	1.11V
0.49	3.48%	8.4%	1.66V
0.36	3.31%	9.3%	3.23V
0.25	3.2%	9.5%	5.26V
0.16	3.14%	10.2%	Out of Range
0.09	3.08%	10.5%	Out of Range

3.7.6 Conclusions

This paper presented a new modulated model-predictive control scheme for an MMCC-STATCOM, shunt connected to the PCC bus of a power grid, to eliminate the unbalanced current and improve the power factor. The proposed method employs a modified Branch and Bound algorithm to select the optimal switch duty ratios for the converter. The current and the capacitor voltage prediction models are presented together with the cost function and the constraint. The procedures for the B&B algorithm implementation were described in detail. The experimental validations of the proposed control scheme were performed. The results obtained demonstrated superior performance as compared to the traditional sinusoidal zero

sequence waveform injection method. The distinctive features of this new method can be summarized as follows:

(1) Injecting a CMV in the phase voltages of a star-connected MMCC reduces the peak phase voltages, hence extending the unbalanced load current compensation range up to 70%, whereas the conventional method can only reach 60%.

(2) The proposed method experimentally verified that the good performance in the unbalanced current and the reactive current cancellation with the compensation current is below the rated limit.

(3) The SM capacitor voltages can be well balanced, achieving a significant reduction of the capacitor voltage ripples down to 8.0% compared to 10% for the conventional scheme under the same operating conditions.

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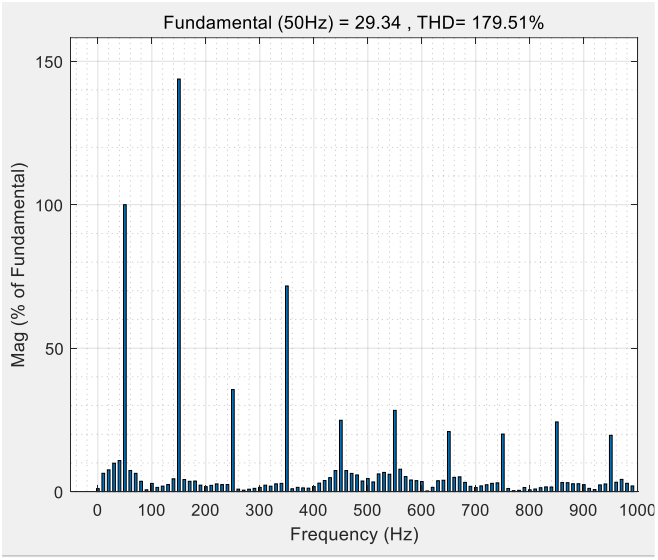
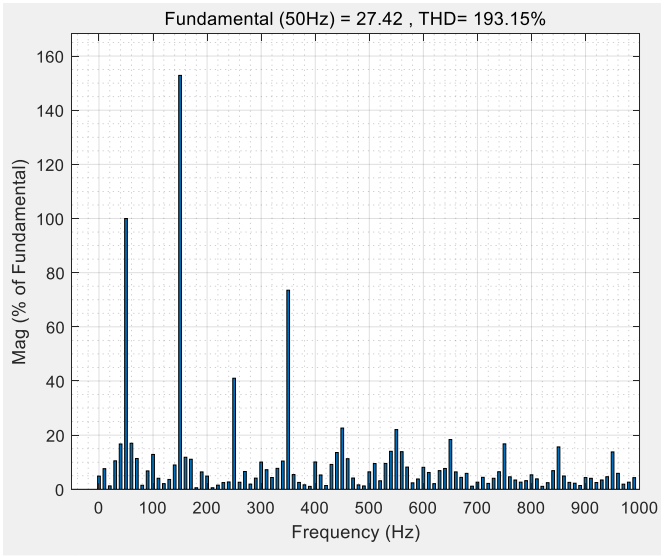


(a)



(b)

Figure 3.19: The frequency spectra of the common mode voltage when the unbalanced ratio is 0.42 for (a) the proposed method with the λ= 0.25 (b) the proposed method with the λ= 0.49

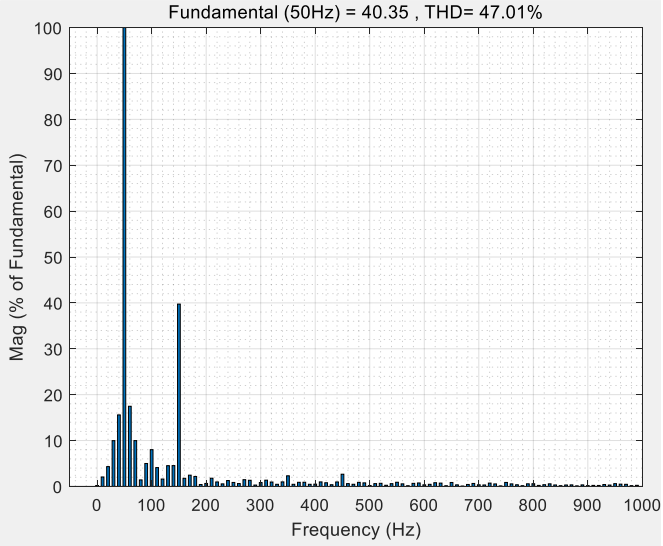


Figure 3.20: The frequency spectra of the common mode voltage when the unbalanced ratio is 0.42 for the conventional method

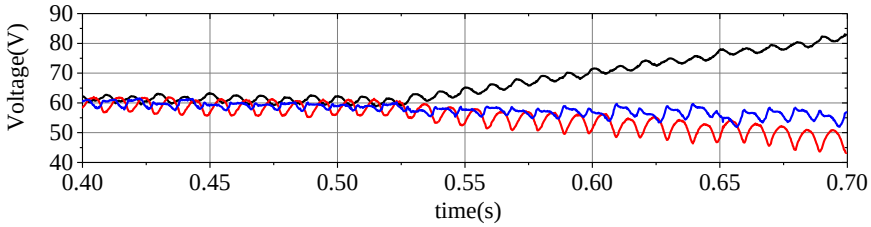


Figure 3.21: The variations of the sum of the sub-modules capacitor voltages with the λ=0.16 and the compensation ratio 70%

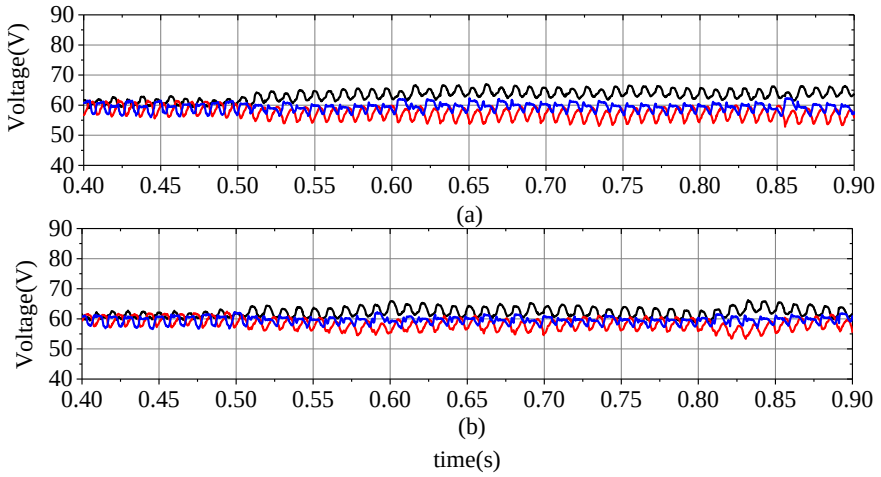


Figure 3.22: The variations of the sum of sub-modules capacitor voltages with (a) the λ=0.25 and (b) the λ=0.49 when the compensation ratio is 70%

CHAPTER 4

TRANSFORMER-LESS STATIC SYNCHRONOUS SERIES COMPENSATOR FOR UNBALANCED VOLTAGE MITIGATION

4.1 Introduction

A Static Synchronous Series Compensator (SSSC) consists of a power electronic inverter and the energy storage elements and is conventionally connected in series between the AC mains and the load through a transformer. By the series insertion of a voltage, this device provides an independent real and reactive power flow control, hence making the network flexible to accommodate the distributed generators (DG). The SSSCs are particularly effective in mitigating the power quality issues of the voltage unbalance, the sags and swells, and the harmonics. These may result from the grid faults such as the single or double-phase groundings, the line disconnection, the resonance, and the line impedance mismatch [1]. It is worth noting that an unbalanced situation may

happen after these mentioned faults. With increasing the DGs in a system, these faults occur more often and can cause severe disturbances to the grid operation [2]. The effective eliminations of such faults by the SSSC are imperative but also challenging.

The high dynamic performance mitigation of the voltage distortion requires the SSSCs to give a fast response for voltage fault detection and compensation. However, the conventional SSSC having three-phase transformer windings inserted in the power lines causes dynamic delays in the voltage responses, and the transformer may also bring the unbalances due to the possible asymmetrical winding impedances [3], [4]. Furthermore, the conventional SSSC may inject an inaccurate compensation voltage due to a voltage drop on the inverter filter choke branch. The transformerless SSSCs (TL-SSSC) [5] have the potential to alleviate these problems. The topology brings several advantages over the conventional ones such as the low cost, the light weight, the high efficiency and the fast dynamic response [6]. They are more effective and efficient than their conventional counterpart in solving many problems caused by the increasing utilization of renewable energy.

In this chapter, a TL-SSSC is proposed for mitigating the voltage distortion of a power distribution line, which has the load and the renewable sourced generators connected. A Dead-Beat current control scheme with the time delay compensation is applied to evaluate the three compensating reference voltages to be injected by the TL-SSSC. A Typhoon Hardware-in-Loop (HIL) emulator is then used to simulate the power distribution system with the proposed TL-SSSC, and a TI-DSP is used to implement the control scheme which controls the switches of the TL-SSSC.

The chapter is structured as follows: Section 4.2 gives a review of the control schemes for the SSSC for voltage distortion mitigation. Section 4.3 describes the configuration of the power system with a TL-SSSC. The basic power flow control

method for the SSSC and the power line models for the phase current predictions are presented in sections 4.4 and 4.5. The analyses of the power controllable range under different levels of voltage unbalance are given in Section 4.6. Finally, in section 4.7, the experimental system of using the DSP to control the circuits emulated in the typhoon HIL device and the results validating the proposed control scheme are given.

4.2 SSSC Power Flow Control Principle and Methods

4.2.1 SSSC Power Flow Control Principle

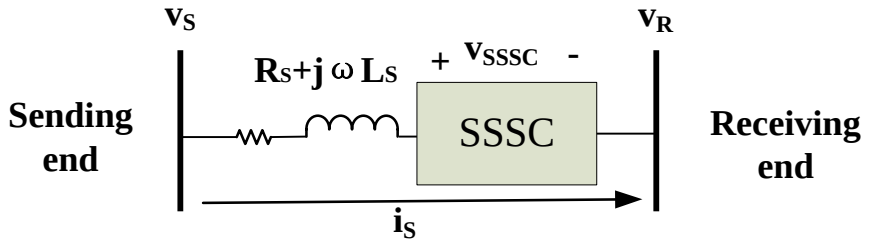


Figure 4.1: The power line with the SSSC

Considering the power line shown in Fig.4.1, by inserting the three phase voltages, $\vec{V}_{SSSC}$ in the line, the SSSC effectively changes the receiving end voltage to a new voltage phasor $\vec{V}_R$. With the line impedance between the sending and the receiving ends being jX_S, the original active and reactive powers are changed to P' and Q' and can be expressed as

$$
\begin{aligned}
P + jQ &= \vec{V}_R \times \vec{I}_R^{\,*} = \vec{V}_R \times \left(\frac{\vec{V}_S - \vec{V}'_R}{jX_L} \right)^* \\
&= \vec{V}_R \times \left(\frac{\vec{V}_S - \vec{V}_{SSSC} - \vec{V}_R}{jX_L} \right)^* \\
&= \left(-\frac{v_S v_R}{X_L} sin\theta_R + \frac{v_{SSSC} v_R}{X_L} sin(\theta_R - \theta_{SSSC}) \right) \\
&+ j \left(\frac{v_S v_R cos\theta_R - v_R^2}{X_L} - \frac{v_{SSSC} v_R}{X_L} cos(\theta_R - \theta_{SSSC}) \right)
\end{aligned}
\tag{4.1}
$$

where the symbol "*" indicates the conjugate of the phasor $\vec{I}_R$ and the θ_{SSSC} is the phase angle of the phasor $\vec{V}_{SSSC}$ with respect to the $\vec{V}_S$. Clearly, the second terms in both real and imaginary parts of (1) are the controllable power P_{SSSC} and Q_{SSSC} given as

$$
P_{SSSC} = \frac{v_{SSSC} v_R}{X_L} sin(\theta_R - \theta_{SSSC}) \tag{4.2}
$$

$$
Q_{SSSC} = -\frac{v_{SSSC} v_R}{X_L} cos(\theta_R - \theta_{SSSC}) \tag{4.3}
$$

Given the required P and Q values to flow in the power line, the above two expressions can be used to evaluate the voltage magnitude and the angle of the SSSC compensating voltage.

In general, the voltage phasor $\vec{V}_{SSSC}$ from the SSSC device can be adjusted to any angle between 0-2π with respect to the $\vec{V}_R$ as illustrated by the phasor diagrams in Fig.4.2 (a)-(c). When the $\vec{V}_{SSSC}$ lags $\vec{V}_R$ by 90° as shown in Fig.4.2 (a), the phase angle θ_{SSSC} of the effective voltage $\vec{V}'_R$ is increased while its magnitude change is negligible. Assuming the voltage $\vec{V}_S$ on the sending side does not vary quickly, this results in increasing the real power P passing through the line more than the changes of imaginary power Q. On the contrary, if the $\vec{V}_{SSSC}$ leads $\vec{V}_R$ by 90°, it forces a reduction in P.

Aligning the inserted $\vec{V}_{SSSC}$ in phase with $\vec{V}_R$, as seen in Fig.4.2 (b), results in more changes to the magnitude of $\vec{V}'_R$ than the phase angle, hence realizing the reactive power flow control along the line. Fig.4.2 (b) shows this; namely making $\vec{V}_{SSSC}$ in the phase with the $\vec{V}_R$ results in reducing the reactive power, and the line current becomes more capacitive. Conversely, if the $\vec{V}_{SSSC}$ is counter-phased to the $\vec{V}_R$, the line appears to become more inductive.

The simultaneous control of P and Q by the $\vec{V}_{SSSC}$ can be obtained by adjusting the $\vec{V}_{SSSC}$ for the effective line impedance change. As shown in Fig.4.2 (c), the $\vec{V}_{SSSC}$ varies inside a limited circle, restricted by the rated voltage of the converter and centered around the $\vec{V}_R$; the effective line reactance X_S varies according to the $\vec{V}_{SSSC}$, hence simultaneously changing the real and reactive powers as required.

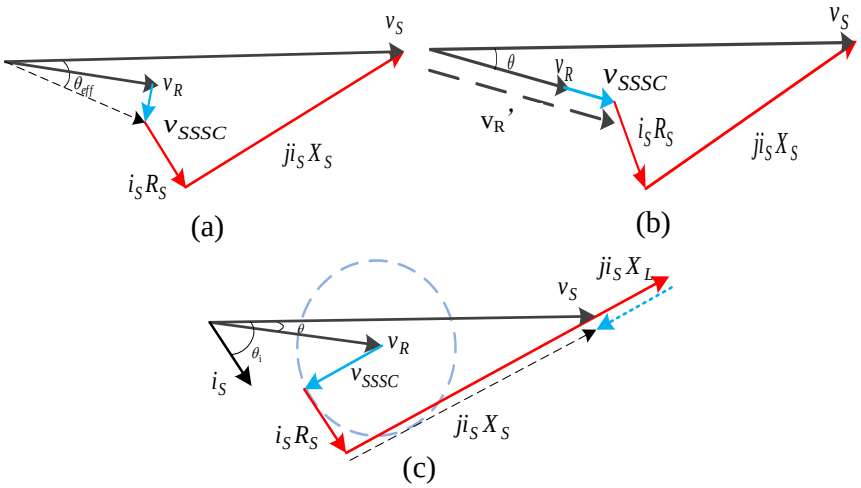


Figure 4.2: (a) The only active power control (b) the only reactive power control, (c) the line impedance control

4.2.2 Power Flow Control Methods

The power flow control using the SSSC under both balanced and unbalanced voltage conditions relies essentially on deriving the required three phase voltages,

i.e. the reference voltage generation, which allows the required real and reactive powers to flow through the line. For the unbalanced line voltage, the reference voltage needs to restore the line voltages to the required balanced levels, hence maintaining the desired power flow along the line. Different algorithms for the reference voltage generation under the distorted line voltages have been presented in the literature [7]–[9], and are reviewed briefly below. Once the reference voltages are calculated, the algorithms for controlling the VSC in an SSSC have also been investigated by many researchers which are also described in this subsection.

4.2.2.1 Reference Voltage Generation

A well-known algorithm by Hilmy Awad et al is based on the traditional concept of phasors [10], [11] of the sequence components. The method decomposes the measured unbalanced three-phase voltages into the positive and the negative sequences and transforms them to their corresponding d-q rotating reference frames. For each sequence, a double-vector controller (DVC) is applied to control both current and voltage with an inner current control loop and an outer voltage control loop. This scheme can also be implemented in stationary reference frames. Clearly, the computational burden of this strategy is high and hence affects the dynamic performance.

Another technique only considers positive sequence control and treats the negative sequence components due to voltage unbalance as unwanted variations in the positive sequence [12] to be canceled. Using only one set of controllers which can be vector controllers and applying higher switching frequencies, the controller is able to cancel these variations. This strategy is computationally more efficient than the former but requires higher switching frequencies hence causing higher switching losses.

There are also methods that use high pass filters to extract the negative se-

quence component from the measured voltages. The instantaneous P-Q theory applied to the Static Compensator (STATCOM) for the unbalanced current compensation [13] follows this principle and can be applied to voltage unbalance mitigation. This method also has a high switching loss problem.

4.2.2.2 Current/voltage Control Algorithms

The current/voltage control algorithms for the VSC in the SSSC are also important. The model predictive control (MPC) is now widely applied. This can be divided into two categories; the finite control set (FCS-MPC) [7], [8] and the continuous control set(CCS- MPC) [9]. The former determines the optimal voltage vector by minimizing the predefined cost index which may combine multiple objectives, such as minimizing the AC current tracking errors and keeping the converter DC capacitor voltage balanced. Although good transient performances can be achieved, the optimal finite set of the switching states obtained leads to variable switching frequencies and large current ripples. In addition, it involves a heavy computational burden especially when the converter is a special multi-level voltage type [14]. The CCS-MPC, on the other hand, uses the system model and calculates the voltage reference by minimizing the predefined cost index [9]. It then applies the derived voltage reference values to generate the switching signals using a pulse width modulation (PWM) scheme [15]–[17]. This scheme has the advantages of giving smaller current ripples and requires less computational effort [18], but is sensitive to parameter mismatches.

The deadbeat (DB)control [19], [20] is another model-based predictive control method. It does not require minimizing a defined cost function, but calculates the reference voltages directly from the model in order to minimize the errors between the measured and the reference current values at the next sample instant [21], [22]. The PWM scheme is used to translate the reference voltages into the switching

signals. Naturally, the conventional DB method is computationally efficient and gives a fast response speed [23]. However, its transient performance is highly sensitive to the parameter uncertainties, and the unexpected delay in the digital control system due to the measurement and the control calculations. In fact, all the above MPC strategies, including the Deadbeat control method, are affected by the time delay due to the considerable calculation time. Depending on the sampling frequency and the speed of the microprocessor used for the control, the time gap between the instant when the current/voltage for the calculations are measured and the instant the actual application of the calculated switching signals to the converter can be long, hence resulting in an inaccurate control and a consequently poor dynamic performance. The strategies to compensate for such a delay have been proposed [24], [25], they vary according to the application field and the types of the MPC control schemes. In this work, the time delay compensation is adopted in the proposed control scheme in order to improve control accuracy.

4.3 Modeling and Control for Unbalanced Voltage Mitigation

This section presents the structure of a power line where a TL-SSSC is installed for the power flow control, the equivalent circuit model of this power line and the proposed Deadbeat control scheme.

4.3.1 The Configuration of a Power Distribution Line with a TL-SSSC

Fig.4.3 (a) shows a single line diagram of a mid-voltage (11kV) distribution line with the distributed generators. The sending-end bus-bar is with the voltage source,

The $\overrightarrow{V}_S$, and the receiving-end bus-bar with voltage, $\overrightarrow{V}_R$ has the load and multiple DGs connected to the power line by the grid-tied inverters. The TL-SSSC consisting of three separate H-bridge inverters, one per phase, is directly connected in series in the phase line with no transformers. As seen in Fig.4.3 (b), each phase inverter has its own energy storage which may be provided by a battery or a renewable sourced generator. The AC output of each of the three inverters is mounted with an L-C filter consisting of a series inductor with the inductance L_f, and a shunt capacitor with the capacitance C_f for eliminating harmonics due to switching. The TL-SSSC offers the advantages of low cost, small size, high efficiency and fast dynamic response. The line impedance at the sending and the receiving ends are respectively R_1-L_1, and R_2-L_2. The parameters for this power system are listed in Table 4.1.

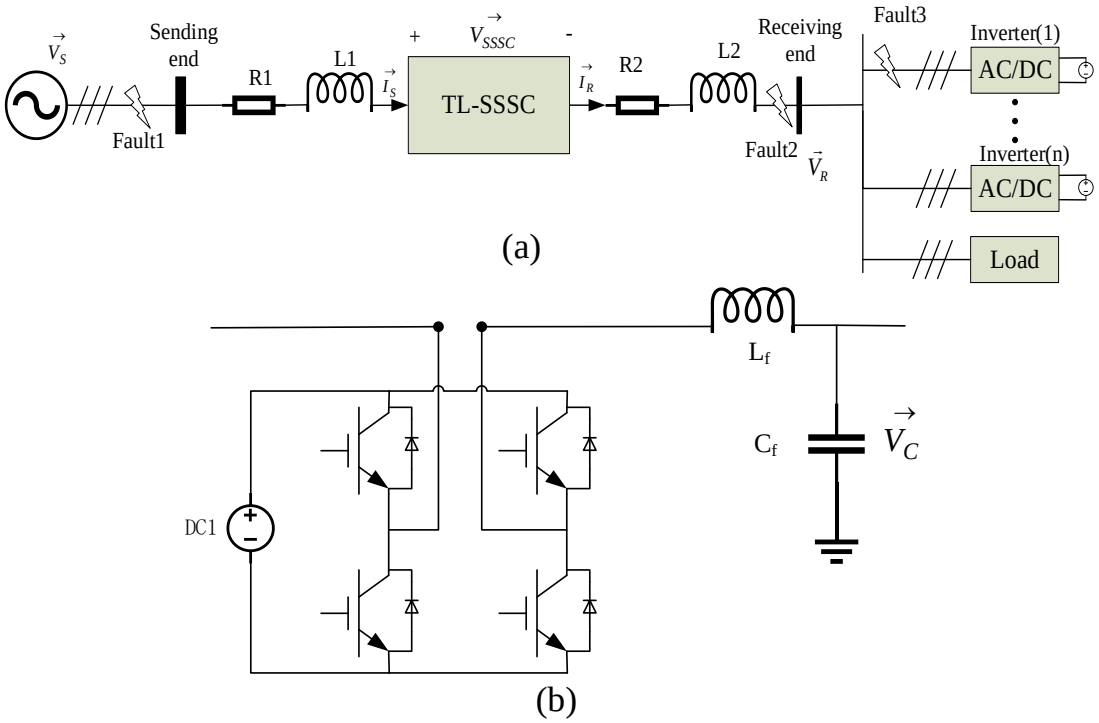


Figure 4.3: (a) The configuration of a power line with a TL-SSSC (b) the converter circuit configuration and the filter for each phase of a TL-SSSC

Using the TL-SSS to mitigate the voltage distortion hence making the loads riding through these momentary power supply faults, the three phase voltages injected by the TL-SSSC need to be estimated and applied promptly. The proposed approach derives the reference currents for each phase using the required powers and the positive sequence component of the receiving end voltage, as if there are no voltage faults. The resultant three reference currents can then be utilized to evaluate the three phase voltages for the TL-SSSC separately. To ensure the high dynamic response performance model-based deadbeat control scheme is appropriate, it is also effective in eliminating the voltage drop and the phase shift caused by the converter L-C filter. The cut-off frequency of this LC filter is about 6500Hz which is mainly used for eliminating the harmonics caused by the switching frequency of the switches. The reason to use the LC filter instead of the L filter is its

Table 4.1: The parameters of the power line in Figure 4.3

Rated Power P_norm	10MW
Rated Voltage V_norm	11Kv
Sending end voltage V_S	11KV
Distribution Line resistance R_1	5.42Ω
Distribution Line resistance R_2	1.08Ω
Distribution Line Inductance L_1	7mH
Distribution Line Inductance L_2	1.4mH
LC Filter Inductance L_f	2.36mH
LC Filter Capacitance C_f	10uF
DC input voltage	2200V
Switching frequency	20KHz
Controlling frequency	10KHz

4.3.2 Modeling of Power Line with TL-SSSC

The phase voltages of the power line with a TL-SSSC shown in Fig.4.3 (a) can be modeled by the three equations expressing, respectively, the line voltages of the three sections. These are the sending end PCC with voltage $\overrightarrow{V}_S$ to the TL-SSSC filter capacitor terminal with the voltage $\overrightarrow{V}_C$, the receiving end bus-bar, $\overrightarrow{V}_R$, to the $\overrightarrow{V}_C$ and the inverter filter capacitor voltage itself. Thus, for the first section, the per phase voltage equation is given as

$$v_{Sm} - v_{SSSCm} - v_{Cm} = R_1 i_{Sm} + (L_1 + L_f)\frac{di_{Sm}}{dt} \quad (m = a,b,c) \tag{4.4}$$

Its discrete time form with a sampling time T_S at the kth sample can be written as

$$\begin{aligned} &v_{Sm}(k) - v_{SSSCm}(k) - v_{Cm}(k) \\ &= R_1 i_{Sm}(k) + (L_1 + L_f)\frac{i_{Sm}(k+1) - i_{Sm}(k)}{T_s} \end{aligned} \tag{4.5}$$

The discrete time model for the section from the capacitor node to the receiving end of the power line is expressed as:

$$v_{Cm}(k) - v_{Rm}(k) = R_2 i_{Rm}(k) + L_2\frac{i_{Rm}(k+1) - i_{Rm}(k)}{T_s} \tag{4.6}$$

Note that v_{cm} in above varies due to the difference between the current from the sending end and that to the receiving end. Thus the third equation expressing the rate of change of the TL-SSSC filter capacitor voltage in the discrete time form is given as

$$i_{Sm}(k) - i_{Rm}(k) = C_f\frac{v_{Cm}(k+1) - v_{Cm}(k)}{T_s} \tag{4.7}$$

Applying the conventional deadbeat control law, the mth phase TL-SSSC compensating voltage can be evaluated using (4.5) as

$$\begin{aligned} v^*_{SSSCm}(k) &= v_{Sm}(k) - v_{Cm}(k) \\ &- R_1 i_{Sm}(k) - (L_1 + L_f)\frac{i_{Sm}(k)^* - i_{Sm}(k)}{T_s} \end{aligned} \tag{4.8}$$

where the $v_{Sm}(k)$, $v_{Cm}(k)$ and $i_{Sm}(k)$ are all measured variables at the time instant k, only the reference current $i^*_{Sm}(k)$ in the above equation is unknown, but can be deduced from the following process described in the sub-section 4.3.3. Since the TL-SSSC control is to ensure the receiving end current $i_{Rm}(k)$ tracking a reference value, $i^*_{Rm}(k)$, determined by the required P and Q flowing along the line, one can replace the $i_{Rm}(k+1)$ in (4.6) by the $i^*_{Rm}(k)$. Subsequently the desired capacitor voltage $v^*_{Cm}(k)$ can be calculated as

$$v^*_{Cm}(k) = R_2 i_{Rm}(k) + L_2\frac{i^*_{Rm}(k) - i_{Rm}(k)}{T_s} + v_{Rm}(k) \tag{4.9}$$

Replacing the $v_{Cm}(k+1)$ by the $v^*_{Cm}(k)$ in (4.9), the desired sending end current $i^*_{Sm}(k)$ can be derived as

$$i^*_{Sm}(k) = C_f\frac{v^*_{Cm}(k) - v_{Cm}(k)}{T_s} + i_{Rm}(k) \tag{4.10}$$

Subsequently, according to (4.8), the desired TL-SSSC voltage can be calculated using (4.10) and the duty ratio for the TL-SSSC is given as

$$m(k) = \frac{v^*_{SSSCm}(k)}{v_{dc}(k)} \tag{4.11}$$

where the $v_{dc}(k)$ is the corresponding dc voltage for the mth phase of the TL-SSSC.

4.3.3 Deadbeat Control with Delay Compensation

To evaluate the TL-SSSC compensating voltages, the deadbeat control scheme takes the measurements of the three phase voltages and currents at multiple points along the power lines at the kth sample instant. It then calculates the compensating voltages to be injected by the TL-SSSC using (4.5)-(4.8). Depending on the sampling frequency and the microcontroller speed, the calculation time can be significant compared to a sampling time interval, there will be a delay between the instant for the measurements and the instant of the application of the new switching signals. The reason can be shown in Fig.4.4 which is the time diagram for the digital control system. In one time period which is Ts determined by the control frequency of the digital controller, the time for the conversion from measured analog signals to digital signals is necessary which can be seen as the yellow part in the Figure. The calculation time to obtain the results which is shown as the blue block in the Figure will be extended if the control part is complicated. Hence, during one time period, the conversion and the calculation will inevitably take most of the time. It is worth noting that the result control signals G(k) calculated by the digital controller need to control the hardware device for a whole period time T_s so that the device can have a good tracking reference value performance. However, in fact, if the control signals are directly sent to the hardware devices after the calculation, the tracking performance of the hardware device is far below expectations due to the lack of time.

This delay needs to be compensated to prevent the inaccurate predictions of the current and the voltage at the kth sample interval hence resulting in a poor current tracking performance. To reduce the transient oscillation, the estimations of the voltage variables are extended to the (k+2)th and the (k+3)th samples, and the compensating control variable at (k+1)th sample is then determined to enable the current tracking the required references. The control algorithm for the TL-SSSC

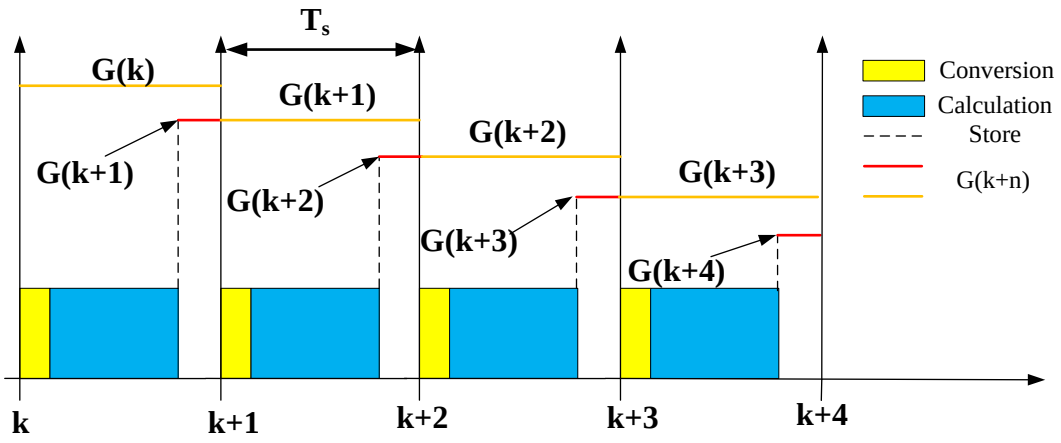


Figure 4.4: The time diagram for the digital control system

can be implemented as follows:

(1) At the kth sample instant, the compensating voltages $V_{SSSC}(k)$ is applied to the TL-SSSC, the samples of the voltages/currents at the sending end, as well as the load ends and the voltages at the filter capacitor terminals, i.e. all variables $v_{Sm}(k)$, $v_{Rm}(k)$, $v_{Cm}(k)$, $i_{Sm}(k)$ and $i_{Rm}(k)$ are taken.

(2) The evaluation of the $v^*_{Cm}(k+3)$ can be from (4.9). Since the future reference current (per phase) samples are the sinusoidal functions, their values can be estimated as

$$\begin{bmatrix} i^*_{Ra}(k+4) \\ i^*_{Rb}(k+4) \\ i^*_{Rc}(k+4) \end{bmatrix} = D(4\omega T_s) \begin{bmatrix} i^*_{Ra}(k) \\ i^*_{Rb}(k) \\ i^*_{Rc}(k) \end{bmatrix} \tag{4.12}$$

where the D($4\omega T_s$) is given as

$$D(\sigma) = \frac{2}{3}\begin{bmatrix} cos(\sigma) & -\frac{1}{2}cos(\sigma-\frac{\pi}{3}) & -\frac{1}{2}cos(\sigma+\frac{\pi}{3}) \\ -\frac{1}{2}cos(\sigma+\frac{\pi}{3}) & cos(\sigma) & -\frac{1}{2}cos(\sigma-\frac{\pi}{3}) \\ -\frac{1}{2}cos(\sigma-\frac{\pi}{3}) & -\frac{1}{2}cos(\sigma+\frac{\pi}{3}) & cos(\sigma) \end{bmatrix} \tag{4.13}$$

Thus the $v^*_{Cm}(k+3)$ can be derived as

$$v^*_{Cm}(k+3) = R_2 i_{Rm}(k+3) + L_2\frac{i^*_{Rm}(k+4) - i_{Rm}(k+3)}{T_s} + v_{Rm}(k+3) \tag{4.14}$$

(3) Estimating the sending end reference current at k+2 th samples by (4.10); Once having the $v^*_{Cm}(k+3)$ and the measured $v_{Cm}(k)$, the sending end reference current can be given as

$$i^*_{Sm}(k+2) = C_f\frac{v^*_{Cm}(k+3) - v_{Cm}(k+2)}{T_s} + i_{Rm}(k+2) \tag{4.15}$$

(4) Calculating the compensating voltage at k+1th sample from (4.8)

$$v^*_{SSSCm}(k+1) = v_{Sm}(k+1) - v_{Cm}(k+1) - R_1 i_{Sm}(k+1) - (L_1+L_f)\frac{i_{Sm}(k+2)^* - i_{Sm}(k+1)}{T_s} \tag{4.16}$$

As can be seen, we need to estimate the voltages and the currents at k+1 , k+2 and k+3 samples. Taking the sending end voltage as an example, this can be performed by applying the Lagrange Extrapolation using the present and the previous samples which have been shown below.

$$v_{Sm}(k+1) = 4v_{Sm}(k) - 6v_{Sm}(k-1) + 4v_{Sm}(k-2) - v_{Sm}(k-3) \tag{4.17}$$

$$v_{Sm}(k+2) = 10v_{Sm}(k) - 20v_{Sm}(k-1) + 15v_{Sm}(k-2) - 5v_{Sm}(k-3) \tag{4.18}$$

$$v_{Sm}(k+3) = 20v_{Sm}(k) - 45v_{Sm}(k-1) + 36v_{Sm}(k-2) - 10v_{Sm}(k-3) \tag{4.19}$$

(5) Applying the estimated $v^*_{SSSCm}(k+1)$ to calculate the required duty ratios $m^*(k+1)$. At the (k+1) sample instant, the $m^*(k+1)$ is applied to the TL-SSSC.

(6) Return to 1 for the calculations at the next sample.

4.3.4 The Overall Control Scheme

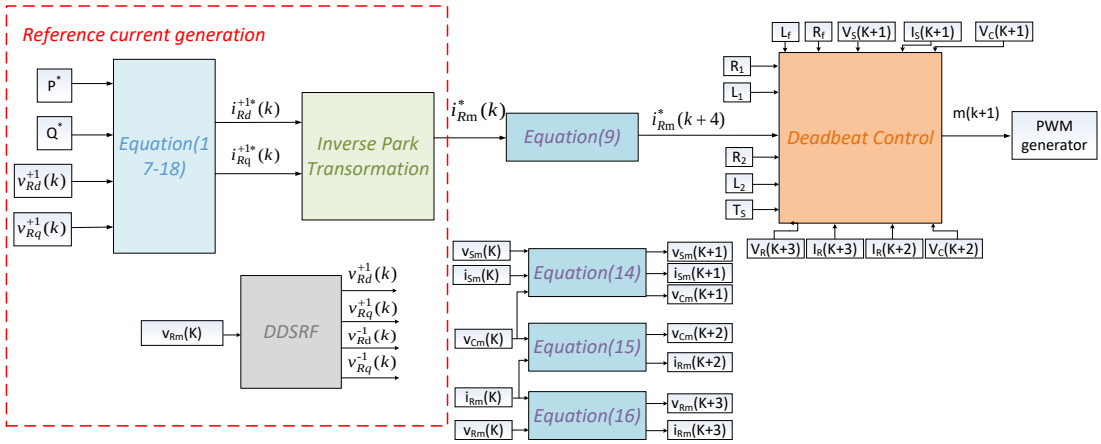


Figure 4.5: The overall control strategy of the transformeless-SSSC

The overall control scheme is shown in Fig.4.5. There are four parts: the delay compensation, the deadbeat controller, the reference current generation, and the PWM generator. The Reference current generation is discussed in this subsection, since the first two have been described above and the PWM generator is very well known and need not be described here.

The three reference currents, $i^*_{Rm}(k)$, at the receiving end are evaluated according to the power requirement and they are the +ve sequence current elements. Given the required active and reactive powers P^* and Q^*, and the measured receiving side voltage, the equations for calculating the +ve sequence reference current d-q elements are given as

$$i_{Rq}^{+1*}(k) = \frac{P^* \times v_{Rq}^{+1*}(k) - Q^* \times v_{Rd}^{+1*}(k)}{v_{Rd}^{+1*}(k) \times v_{Rd}^{+1*}(k) + v_{Rq}^{+1*}(k) \times v_{Rq}^{+1*}(k)} \tag{4.20}$$

$$i_{Rd}^{+1*}(k) = \frac{P^* \times v_{Rd}^{+1*}(k) + Q^* \times v_{Rq}^{+1*}(k)}{v_{Rd}^{+1*}(k) \times v_{Rd}^{+1*}(k) + v_{Rq}^{+1*}(k) \times v_{Rq}^{+1*}(k)} \tag{4.21}$$

where the $v_{Rd}^{+1*}(k)$ and $v_{Rq}^{+1*}(k)$ are, respectively, the +ve sequence d-q elements of the receiving end voltage. They can be extracted in real-time from the measured voltages by using the advanced phase locking technique: the decoupled double synchronization reference frame (DDSRF) phase locking loop [26]. This scheme allows the separation of the positive and the negative voltage/current components under unbalanced faults.

4.4 Power Controllable Range Under Unbalanced Voltage

The voltage and the power ratings of a TL-SSSC are determined according to the peak power rating of the connected distribution line under normal operation, they are commonly set to less than 20% of that of the power line. Due to the unbalanced voltage mitigation, one or two of the TL-SSSC phase voltages may exceed their ratings, which in turn restricts its permissible load power. Thus the estimations of the power references under the different voltage unbalance ratios are necessary to ensure that the converter voltage ratings are not exceeded.

To evaluate the ranges of the TL-SSSC power flows under faulty conditions, the phasor forms of (4.5)-(4.7) are used. The per phase voltage equation for the section of the power line from the sending end at the PCC to the filter capacitor is given as

$$\vec{V}_S - \vec{V}_C - \vec{V}_{SSSSC} = \vec{I}_S(R_1 + j\omega(L_1 + L_f)) \tag{4.22}$$

The TL-SSSC filter capacitor phase voltage is expressed by

$$\vec{V}_C = \frac{1}{j\omega C_f}(\vec{I}_S - \vec{I}_R) \tag{4.23}$$

The voltage equation from the TL-SSSC capacitor filter to the receiving end is

$$\vec{V}_C - \vec{V}_R = \vec{I}_R(R_2 + j\omega L_2) \tag{4.24}$$

Substituting the $\vec{V}_C$ in (4.22) and (4.24) by the expression in (4.23) results in the sending and the receiving side voltage equations being

$$\begin{aligned} &\vec{V}_S - \vec{V}_{SSSSC} = \\ &(R_1 + j\omega(L_1 + L_f) + \frac{1}{j\omega C_f})\vec{I}_S - \frac{1}{j\omega C_f}\vec{I}_R \end{aligned} \tag{4.25}$$

$$\vec{V}_R = \frac{1}{j\omega C_f}\vec{I}_s - (R_2 + j\omega L_2 + \frac{1}{j\omega C_f})\vec{I}_R \tag{4.26}$$

Writing the above two equations in the matrix form gives:

$$\begin{aligned} &v = Ai \\ &v = \begin{bmatrix} \vec{V}_S - \vec{V}_{SSSC} \\ \vec{V}_R \end{bmatrix}, i = \begin{bmatrix} \vec{I}_S \\ \vec{I}_R \end{bmatrix}, \\ &A = \begin{bmatrix} R_1 + j\omega(L_1 + L_f) + \frac{1}{j\omega C_f} & -\frac{1}{j\omega C_f} \\ \frac{1}{j\omega C_f} & -(R_2 + j\omega L_2 + \frac{1}{j\omega C_f}) \end{bmatrix} \end{aligned} \tag{4.27}$$

Subsequently, the sending and the receiving end per phase currents can be calculated by:

$$\begin{bmatrix} \vec{I}_S \\ \vec{I}_R \end{bmatrix} = vA^{-1} \tag{4.28}$$

Under normal operation conditions, the per-phase voltage phasors at both sending and receiving ends are assumed to be defined at the specified constant

levels. By varying the TL-SSSC voltages with the small incremental steps from 0 to their rated values in all possible combinations; namely, the angle from 0 to 360^o and the magnitude from 0 to maximum, the current phasors in (4.28) can be calculated. Subsequently the per-phase active and the reactive powers at the receiving end are calculated by

$$\begin{aligned} P &= V_R cos(\theta_{VR}) \times I_R cos(\theta_{IR}) \\ &+ V_R sin(\theta_{VR}) \times I_R sin(\theta_{IR}) \end{aligned} \tag{4.29}$$

$$\begin{aligned} Q &= V_R sin(\theta_{VR}) \times I_R cos(\theta_{IR}) \\ &- V_R cos(\theta_{VR}) \times I_R sin(\theta_{IR}) \end{aligned} \tag{4.30}$$

where the θ_{VR} and θ_{IR} are, respectively, the phase angles between the receiving end voltage and current to the sending end voltage, which is the reference voltage.

Using the above equations to evaluate the power flow ranges under the unbalanced voltage conditions, the power line impedance at the sending end for each phase can be set to different values, hence creating the three unbalanced voltages at different unbalance ratios at the sending end. Then (4.27) can be applied for evaluating each phase current, and subsequently, the phase powers can be evaluated by (4.29) and (4.30). In this example, the sending and the receiving end voltages are set to 11kV (1.0pu) at the zero phase angle and the receiving end at 0.9pu, also at zero angle. The TL-SSSC voltage rating is 0.18 pu and the current rating is that of the power line. The sending end voltage unbalanced ratios, defined as the percentage of V^{-1}/V^{+1} , are varied from 0% to 10%, and for each case, the per-phase receiving end powers are calculated for the TL-SSSC voltages varying from 0 to its rated voltage with all possible angles. Only the results of the phase which gives the lowest active and reactive power flow ranges, namely, that are most severely affected due to the unbalanced voltage, are presented. Fig.4.6 shows the 3D plots of the real and reactive power variation ranges of one of the

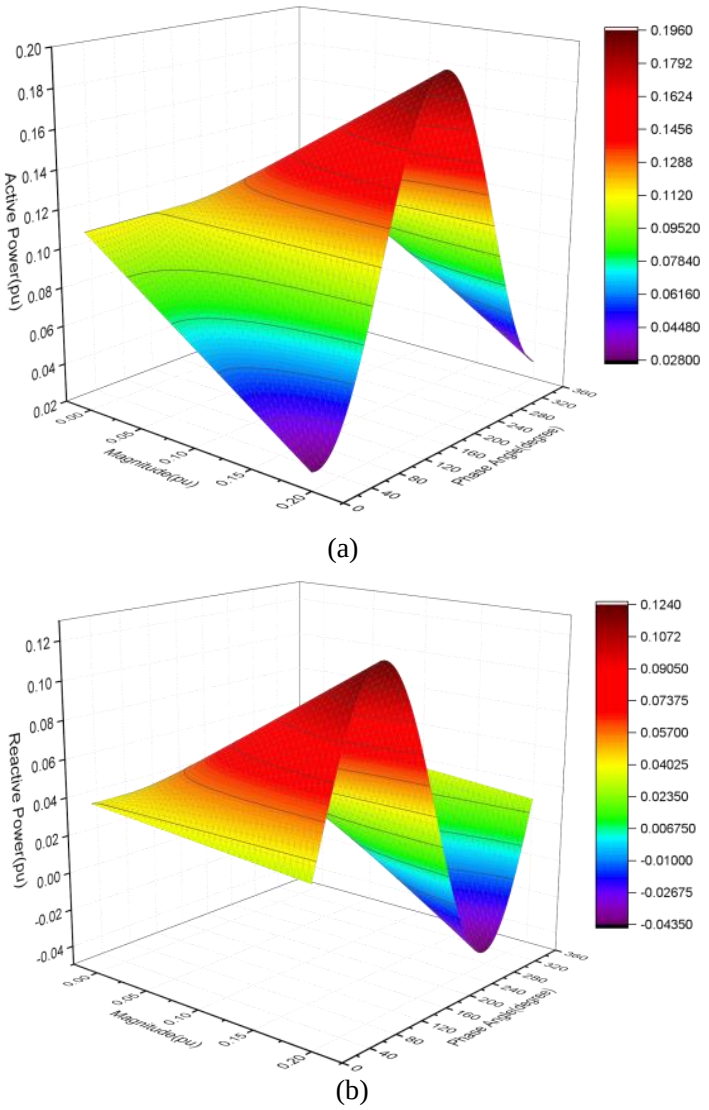


Figure 4.6: The 3D diagrams for (a) the active power in pu (b) the reactive power in pu with different magnitude and the phase angle of V_{SSSC} when the unbalanced ratio is 10%

three phases when the sending end voltage imbalance ratio is as high as 10%. The maximum allowed active power and reactive power flowing from the sending to the receiving ends are about 0.2 pu and 0.112 pu respectively, reducing significantly from when the voltages are balanced. Table 4.2 lists the phase power flow ranges for the sending end voltage imbalance ratio varying from 0% to 10%. As can be

seen, with the increase of the voltage imbalance level, the power flow limits are reduced steadily from P=0.798 pu and Q= 0.608 pu for the voltage balanced case, down to P=0.196 pu and Q=0.124 pu, when the voltage unbalance ratio is 10%. Likewise, the current imbalance ratio measured at the sending end also increases.

Table 4.2: The power limits and the corresponding unbalanced current ratios under different sending end voltage imbalance ratios

Unbalanced ratio of voltage(%)	Maximum P (pu)	Maximum Q (pu)	Unbalanced ratio of current(%)
0	0.7980	0.608	0
2	0.5979	0.4047	17.9
4	0.5277	0.3453	25.23
6	0.412	0.257	38.56
8	0.2834	0.1728	55.74
10	0.196	0.124	69.08

4.5 Hardware Devices for Experiment Validations

To validate the proposed control algorithm for a TL-SSSC for compensating the unbalanced voltage in the power line as shown in Fig. 4.3, the experimental tests using an advanced real-time emulation device, the Typhoon HIL-604 system [27] are performed. The hardware devices used and the experimental process are presented in this section.

4.5.1 Hardware Devices -Typhoon HIL System Controlled by a TI-DSP Card

To validate the proposed control algorithm for a TL-SSSC for compensating the unbalanced voltage in the power line as shown in Fig. 4.3, an advanced real-time emulation device, the Typhoon HIL-604 system is used. This ultra-high fidelity

HIL device consisting of 8-core processors is able for real-time emulation of up to 8 converters, and can test the controller with the 20ns PWM resolution. It can also emulate the power stage with up to 2 MHz update rate. This device can interface with the hardware controllers via its analog and digital input/output ports. The power line with the TL-SSSC depicted in Fig.4.3 and with the parameters in Table 4.1 is built using the Typhoon HIL control center and controlled using a Texas Instruments C2000 DSP (F28069M) interfaced with the HIL device through a TI LaunchPad (LAUNCHXL-F28069M). During the real-time operation, the DSP communicates with the emulated system through the 16-ADC channels, the measured signals including the three-phase voltages at both the sending and receiving ends and the filter capacitor terminals, and the three-phase line currents. The proposed deadbeat with a delay compensation control scheme is in the c-code program implemented in the TI-DSP by the interrupt driven and the sample time is set to 0.2ms. The PWM switching signals generated from the DSP EPWM are applied to the TL-SSSC converter in the Typhoon HIL-604 device via the DSP GPIO ports. In this section, two important hardware devices, the Typhoon HIL 604 device, and the TI-digital signal processor (DSP) are described, and their interface cables are also presented. Then the experimental procedure includes the preparation stage, the operation stage for the Typhoon HIL device and the c-code program implemented in the DSP will be explained.

4.5.2 Typhoon HIL 604 Device

The Typhoon HIL-604 real-time simulator is an 8-core FPGA simulator, a product of the Typhoon hardware in the loop (HIL) series. Its powerful simulation capabilities enable the development, testing, optimization, and quality assurance of the grid connected converters for the commonly used renewable sourced generators, automotive converters, electric propulsion drives, micro-grids, and industry

automation. The device provides 64 analog output pins, 32 analog input pins, 64 digital input pins and 64 digital output pins which allow it to interact with the eternal devices. This simulator can be used in three main aspects in the lab of the University of Leeds shown below:

1. A stand-alone emulator for real time system simulation and control. The typhoon HIL 604 can be programmed to emulate the power systems of different configurations with the power converters and the renewable generators using its large extensive library for the power circuit components. It validates the feasibility of the proposed converter topologies and the control methods, The measured voltage and current signals can be observed in the Supervisory Control and the Data Acquisition (SCADA) panel implemented in the software. By connecting the typhoon HIL 604 simulator with a computer, it allows editing the system setup and monitoring the real time simulation results.

2. A digital controller for the hardware converter/system control. The typhoon HIL can implement the control algorithms for the external converters in a microgrid or the drives. It uses its ADC ports to access the analogous signals and the digital control signals generated are applied to the gate drivers of the external converters via the optical fiber cables.

3. A digital controller test platform. A Digital Signal Processor (DSP) is often programmed for real-time system control, however before it is actually used on a real hardware system, it needs to be tested properly. The typhoon HIL 604 device can be used to emulate the real hardware system for testing the DSP controllers. This set-up Typhoon emulated system allows the measured voltage, the current and the power signals translated into the digital form accessible by the DSP card through the interface card in real-time. The signals received by the DSP are applied to the C-code program implemented in the DSP processor. The desired digital control signals generated by the DSP will be applied to the Typhoon device

to control the power circuit emulated.

4.5.3 Digital Signal Processor

The LAUNCHXL-F28069M launchpad is a 32-Bit real time microcontroller based on the F2806x microprocessor. It allows the maximum clock frequency which is 90MHz. This board contains 16 analog input pins named as ADCIN and 16 digital output pins which are called EPWM pins. The aim for the ADCIN channel is to obtain the analog signals and prepare to transform these signals into digital signals. The EPWM pins are to output the PWM signals to control the switches of the converters emulated in the Typhoon HIL 604 box. Hence, the TI-DSP implemented in the control algorithms can be tested. The DSP functions can be summarized as follows:

1. Receiving the analog signals from the Typhoon simulator and then transforming them into digital signals.

2. The digital signals are used in the microprocessor to calculate the desired PWM signals for controlling the converters by the pre-written C code program.

3. Transferring the PWM signals back into the typhoon simulator for controlling the converters.

4.5.4 Typhoon HIL-TI Launchpad

The Typhoon HIL device enables the development of real-time controllers using the TI C2000 control cards with the DSPs F28027F, F28069M , F28377S and F28379D. The developed controllers are directly used for the control of the systems built with the hardware converters. A Typhoon HIL-TI interface card (either a Typhoon HIL TI launchpad interface card or a Typhoon HIL DSP 180 Interface card) is required for the development work. Fig.4.7 shows a Typhoon HIL device having a TI Launchpad interface card (red card) plugged in. Attached to the top of this

card is a TI-DSP controller card LAUNCHXL-F28069M. The Launchpad links Typhoon HIL analog and digital I/O pins to those of a TI-DSP, hence it establishes the pin-to-pin compatible interface between the TI-DSP and the Typhoon HIL real-time emulator. All digital and analog signals from the HIL simulated system to the TI-DSP and vice versa are routed through this Launchpad.

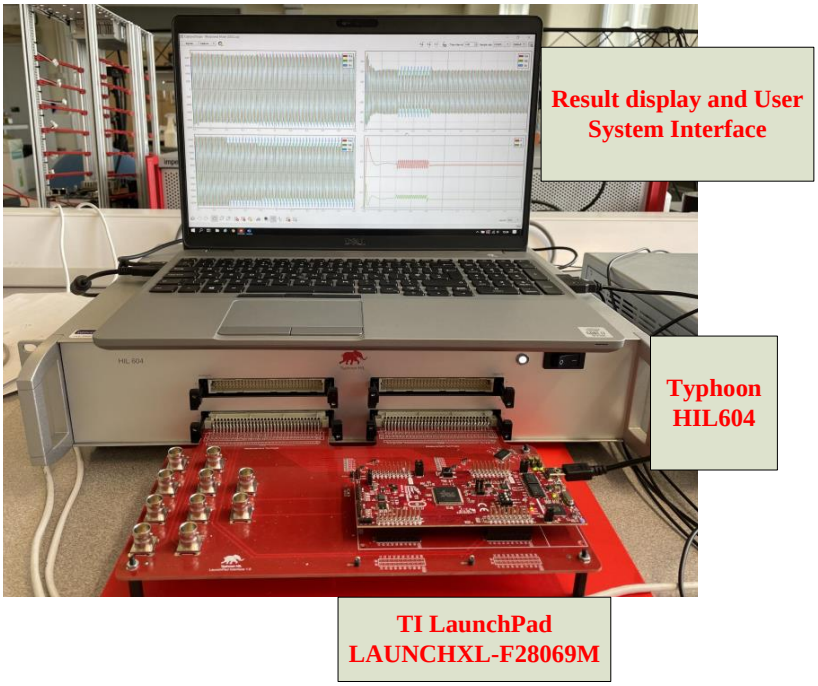


Figure 4.7: The experimental set-up for the real-time DSP control of a Typhoon HIL 604 emulated power line with the TL-SSSC

With this facility, the C-code can be developed which will be loaded and executed by the TI-DSP, and the generated digital signals are applied to the control power converters emulated in the Typhoon HIL device, as if they are the real hardware ones. It is worth noting that the pins on the Launchpad interface card have already been set to link the specific typhoon analog output and digital input pins to the corresponding pins on the TI-DSP card. Table 4.3 lists the numbers of Typhoon HIL analog output pins and their corresponding TI-DSP digital input pins. Table 4.4 lists the Typhoon HIL digital input pin numbers and their corresponding TI-DSP

digital output pins.

Table 4.3: The relationship between the analog output pins and the ADCIN channels

Typhoon Analog output pin number	DSP ADCIN pin number	Typhoon Analog output pin number	DSP ADCIN pin number
A01	7	A09	15
A02	9	A10	12
A03	2	A11	5
A04	10	A12	13
A05	0	A13	3
A06	8	A14	11
A07	1	A15	4
A08	6	A16	14

Table 4.4: The relationship between the digital input pins and the Epwm

Typhoon Digital Input pin number	DSP EPWM pin number
1	EPwm1A
2	EPwm1B
3	EPwm2A
4	EPwm2B
5	EPwm3A
6	EPwm3B

4.5.5 Experiment Test Process

In order to make the tests run successfully and collect the desired results, the whole experiment process can be divided into two stages: the preparation stage and the operation stage.

4.5.5.1 Preparation Stage

In the preparation stage, the construction of the power circuit and the validation of the control method are performed using only the Typhoon HIL device. This involves building the system model and implementing the proposed controller in the Typhoon HIL system and testing the simulated system and the controller working as desired. Then the control block in the Typhoon program can be directly converted into the C-code program through the function in Typhoon software. The control block in the Typhoon program can be replaced by setting several digital input signals needed for receiving the PWM signals from the TI-DSP to control the converters in the power circuit. In addition, the analog signal pins are also needed to be defined in the Typhoon simulated program for transferring the measured voltage and current values to the DSP card. For the controller side, the C-code program once tested working needs to be downloaded into the TI-DSP card. This completes the experimental test preparation. The flow chart of this stage is shown in Fig.4.8.

4.5.5.2 Operation Stage

During the operation stage, both the Typhoon HIL simulation program and the DSP control program are running. On the Typhoon device side, the program for the power line and the converter simulation is working and the measured voltage/current signals are sampled and sent to the DSP card through the analog output (A/O) ports and appeared on the Analogue input pins of the TI-DSP. Meanwhile, the Typhoon HIL device also receives the digital signals which are the PWM control signals coming from the DSP through the digital input (DI) pins. The flow chart for this process is shown in Fig.4.9. During the working period of the typhoon device, the results can be observed through the SCADA panel in real time.

For the TI-DSP, the C-code program has two routines that are implemented by

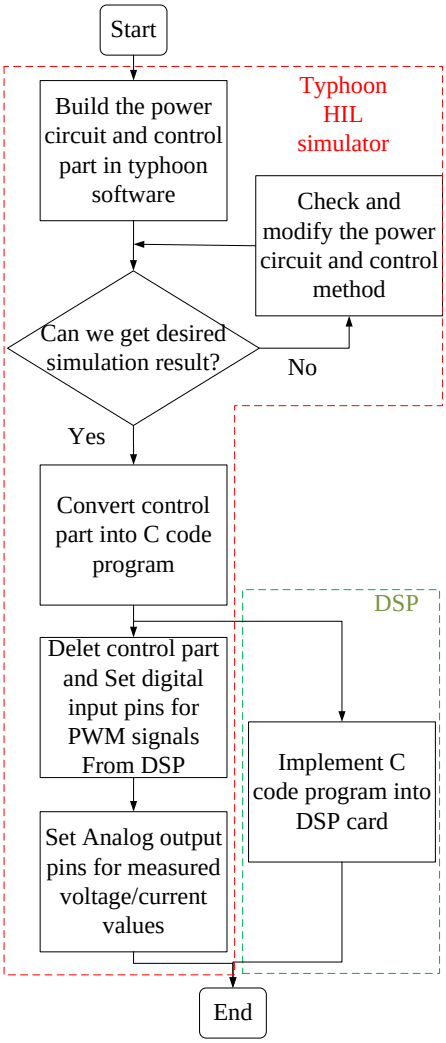


Figure 4.8: The flow chart for the experiment test preparation

the DSP. One is the main routine, which implements the signal acquisition and the control algorithm, and the other is the interrupt routine. The interrupt routine determines the DSP start and end of a control cycle, namely the digital control sampling frequency. Since the clock frequency, F_{cl} , of the DSP is 90MHz, if the sampling frequency is F_{in}, the ratio between them, F_{cl}/F_{in}, set the number of the count. The interrupt routine should wait for each cycle to call the main routine. The flow chart for the interrupt routine is shown in Fig.4.10, at the start of each

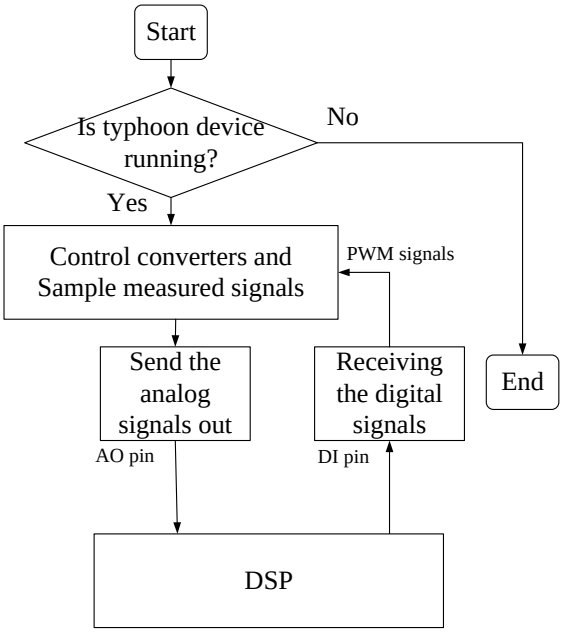


Figure 4.9: The flow chart of the operation stage for the typhoon HIL device

cycle, the counter is set to equal to F_{cl}/F_{in} and then the main routine will be called to perform the control calculation and send the digital PWM signal to the Typhoon digital input pins. When completing all tasks set in the main routine, the program returns to the interrupt routine and will count down the counter by 1 following each clock cycle. When the counter is equal to 0, the counter will be reset to full to call the main routine and the whole control cycle starts again. The C-code for the interrupt routine is called

ConFigCpuTimer (& CpuTimer1, Freq, Ts);

where the Freq is the clock frequency and the Ts is the interrupt frequency. The program is listed in Appendix.

The main routine implements the control algorithm. During one control cycle, the main routine needs to complete the data acquisition, the conversion of the analog signals, the calculations for the desired duty ratios and the generation of the PWM signals. The ADCIN pins receive the analog signals from the typhoon

HIL device, then these signals are saved in total of 16 ADCSOC memories. These memories can realize the analog to digital signals conversion and store them for later use. The C-code for this function is named :

AdcRegs.ADCSOC0CTL.bit.CHSEL= 7;

The meaning of this code is to connect the ADCSOC0 channel with the ADCIN7 pin. There is a variable in the C program of the DSP card which can determine whether the control part implemented in the DSP is working. When Enable is 0, the Epwm pins will always send 0 signals back into the typhoon device. Hence, the switches in the converters will remain disconnected which means the converters are not working. When Enable is 1, the ADCSOC memories will assign the signals with the variables used in the control part by:

generatedModel.p extIn->ila=AdcResult.ADCRESULT0;

This code is to send the signals stored in the ADCSOC0 to the variable i_{la}. Then the C program for the control part is used to calculate the desired duty ratios. Finally, the PWM signals can be obtained by the C-code named below.

EPwm1Regs.CMPA.half.CMPA= ma

where the ma is the duty ratio for the switches in one phase bridge of three phase inverter. “EPwm1Regs.CMPA.half.CMPA” is to obtain the PWM control signals for the upper switch based on ma. These signals will be sent out by the EPWM1A pin. Meanwhile, the EPWM1B pin will send the complementary control signals for the lower switches. The flow chart for the main routine is shown in Fig.4.10 and the C code program for the DSP is attached in the Appendix.

4.6 Experimental Tests and Results

Three different voltage fault scenarios are set up to validate the TL-SSSC and the proposed voltage distortion mitigation scheme. The faults are caused due to either

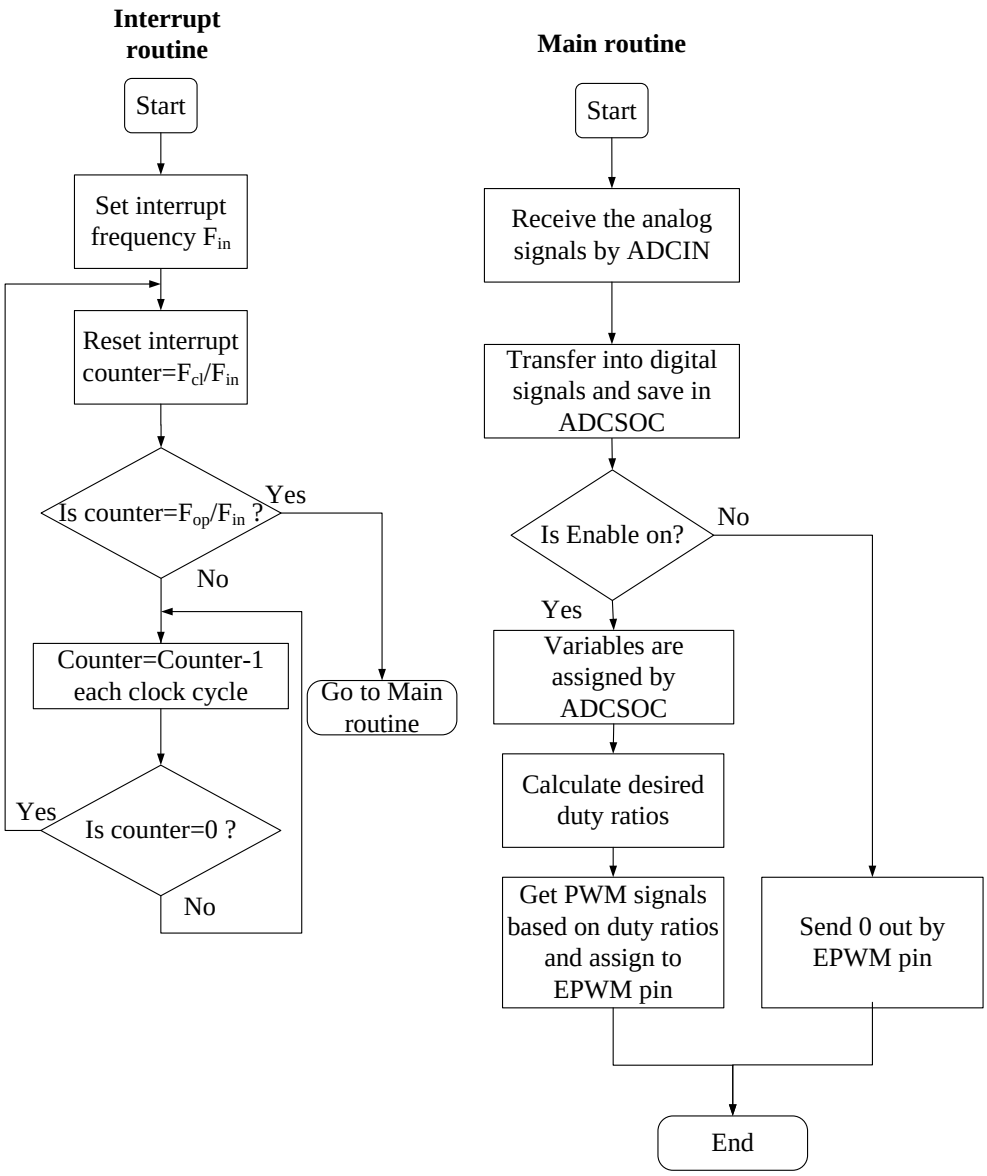


Figure 4.10: The flow chart of the operation stage for the DSP

the double-phase groundings or the severe load/supply imbalances. The level of the voltage/current unbalance is measured according to the ratio of the negative sequence voltage magnitude to the positive sequence one which is commonly accepted in the power community [28]. The reference active and reactive powers for the power line studied are set to 0.275pu and 0.05pu, respectively.

Three different fault scenarios, as indicated in Fig.4.3, are listed below: 1. the fault at point 1, the sending end bus-bar; This results in the unbalanced V_S. The proposed control for the TL-SSSC should be able to maintain the receiving end voltage balanced, leading to the power flow to the load unaffected. 2. the fault at point 2, the receiving end of the power line near the load bus-bar; the TL-SSSC should maintain the current at both receiving and sending balanced, hence protecting the grid normal operation. 3. the fault at point 3, at a DG inverter terminal; the TL-SSSC should control the receiving end power flow to satisfy the load requirement so that the fault is not affecting the rest of the power line.

The voltage/current waveforms at both the sending and receiving bus bars of the power line and across the TL-SSSC, are presented respectively in below. The results shown are in three time periods; Period 1: 0.0 s to 0.2s, no faults, the TL-SSSC performs the normal power flow control operation. Period 2: 0.2s to 0.4s, the fault occurring at different locations, but without the TL-SSSC compensation, the system shows unbalanced voltages and currents. Period 3: 0.4s to 0.6s, the TL-SSSC performs the voltage mitigation.

4.6.1 Scenario 1: Fault at Power Line Sending End

The two phase grounding fault may happen at the sending end. This is emulated in the study by adding two resistors with different values in phases A and B respectively. Fig.4.11 (a)-(c) show the corresponding voltage and current waveforms. The fault occurs at 0.2s to 0.6s, and the voltage imbalance ratio is measured as 6%. Between 0.2s to 0.4s, the TL-SSSC is not active in mitigating the unbalanced voltage, resulting in the receiving end voltage being about 4% unbalance. This causes high current imbalances, approximately 40%, at both the sending and the receiving ends as seen in Fig. 4.11 (b). However, when the TL-SSSC is active from 0.4s, the receiving end voltage is well balanced due to the compensation voltage

effective to eliminate the negative sequence element presenting in the receiving end voltage. The currents at both the sending and the receiving ends are also balanced.

To show the effectiveness of the proposed method in mitigating the voltage dips, the ± sequence–based scheme proposed by Hilmy Awad et al [11] is also applied to control the TL-SSSC. It is to mitigate the voltage unbalance due to the two phase grounding fault, and the results obtained are compared with those shown in Fig.4.11. This scheme divides the supply voltage into +ve and –ve sequences and applies the double vector control (DVC) scheme separately on both sequences. The resultant waveforms are displayed in Fig.4.12 (a) to (d). For the period from 0.4s to 0.6s, when the active voltage dip mitigations are switched on, the sending end voltage waveforms in Fig.4.12 (a) show the same imbalance as that in Fig.4.11 (a). The sending end current waveforms (Fig.4.12 (b)) display a good balance as the one in Fig.4.11 (b). However, the performance of the receiving end voltage waveform is not as good as that shown in Fig. 4.11 (c), since it still presents a slight imbalance (about 3%), even though the waveform performance for the receiving end current is acceptable. In addition, the peak value of the TL-SSSC compensating the voltage, in this case, is higher (by about 250V) than that of the proposed method in Fig.4.11 (d), this indicates that the method has a narrower power flow range when compensating the voltage sags. In addition, this method gives a poorer dynamic response performance than the proposed method. As depicted in Fig.4.12 (d), when changing from period 2 to 3, the TL-SSSC output voltage shows significant oscillations. In contrast, the TL-SSSC compensating voltage changes smoothly for the same condition as that shown in Fig.4.11 (d).

To demonstrate the benefits gained from the proposed dead-beat with the delay compensation scheme in terms of achieving superior power control performance, the comparisons of its results with those from the conventional dead-beat control

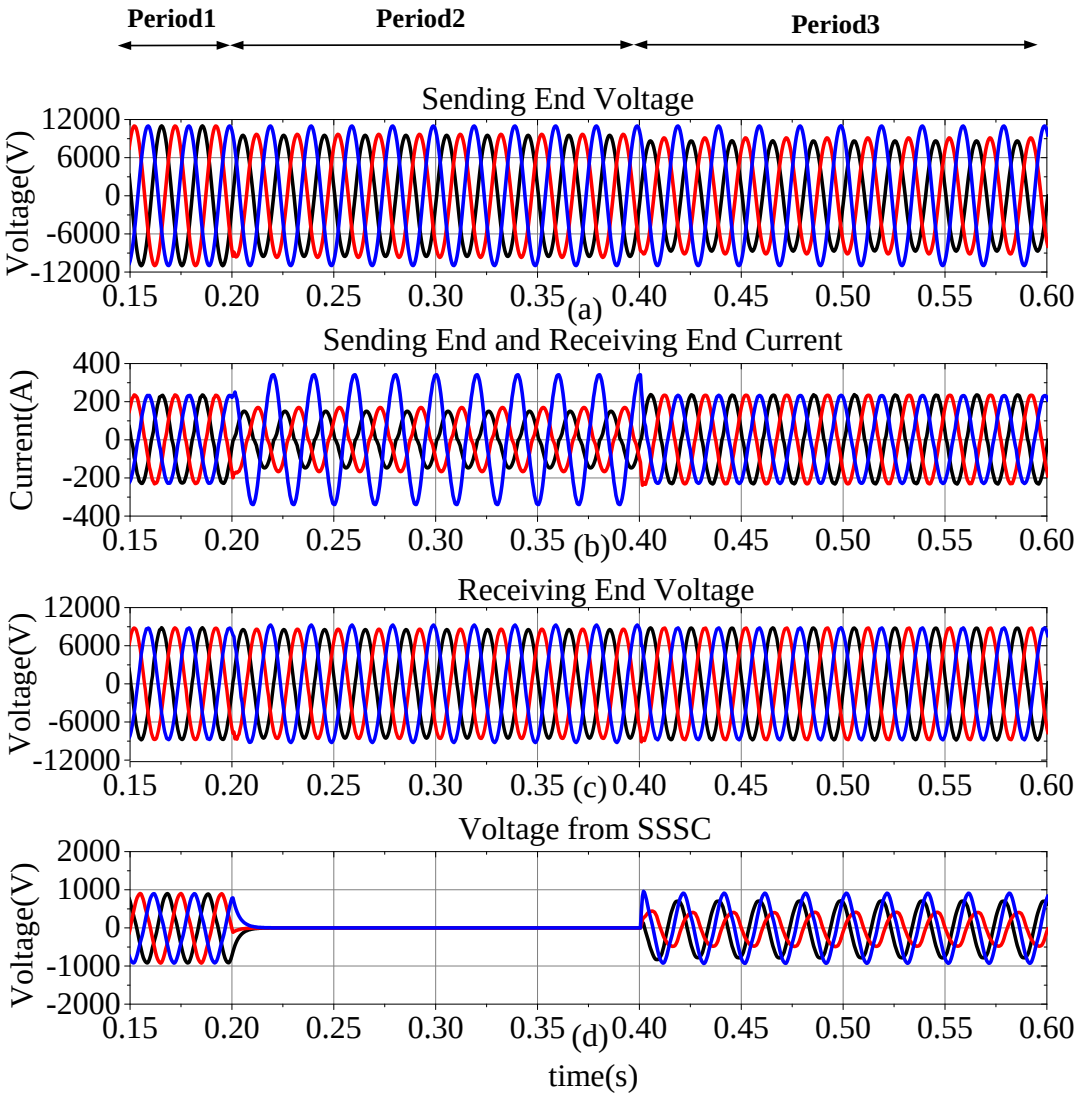


Figure 4.11: The measured waveforms from the proposed method for scenario 1 (a) the sending end voltages, (b) the sending end and receiving end currents (c) the receiving end voltages, (d) the TL-SSSC generated voltage for the double phase grounding fault

method without the delay compensation are given below.

Fig.4.13 (a) to (d) show, respectively, from both methods, the measured receiving-end currents tracking its reference at the steady state over two cycles and the corresponding error waveforms. Clearly, the current obtained from the proposed

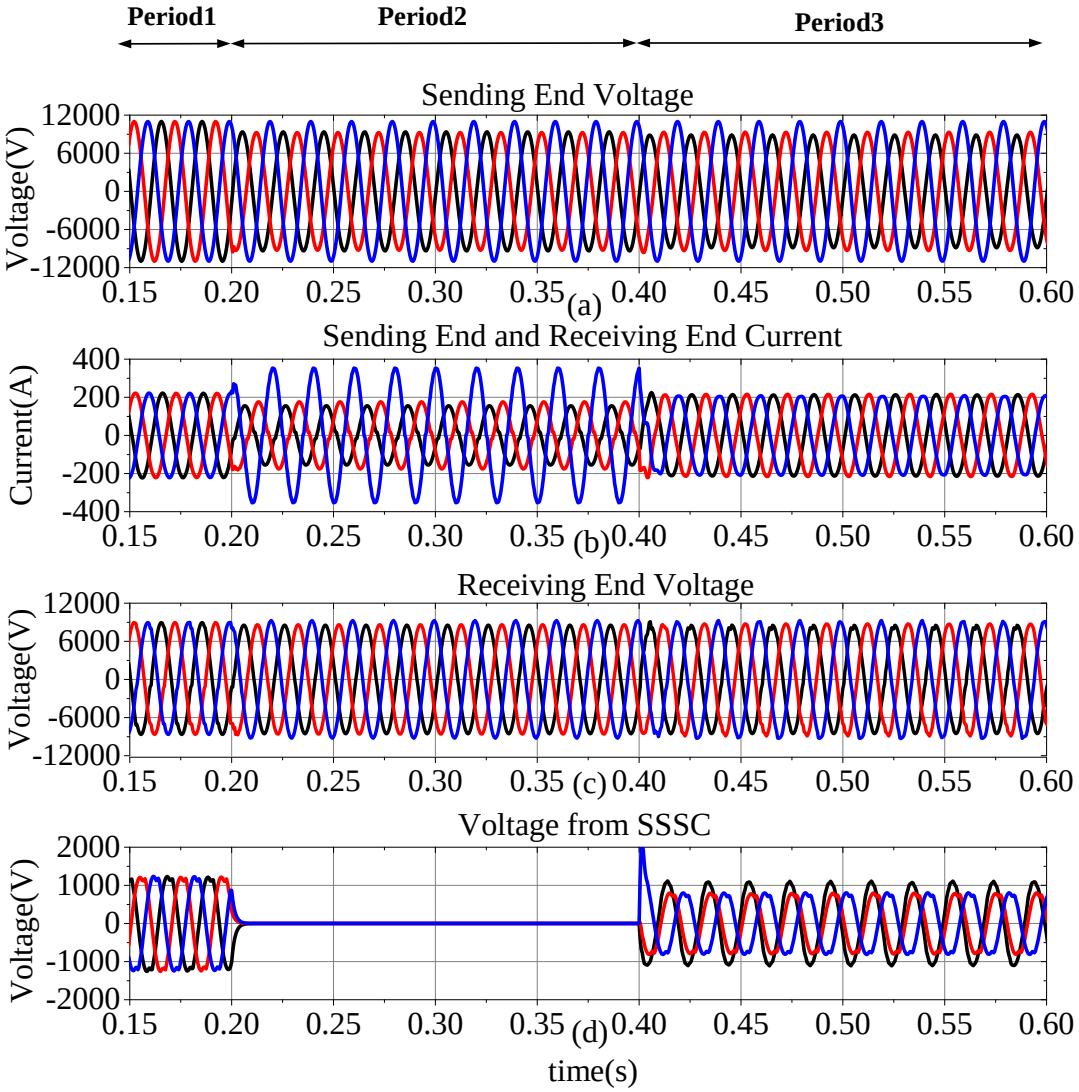


Figure 4.12: The measured waveforms from ± sequence–based by Hilmy Awad method (a) the sending end voltages, (b) the sending end and the receiving end currents (c) the receiving end voltages, (d) the TL-SSSC generated voltage for the double phase grounding fault

method (Fig.4.13 (a)) follows significantly closer to the reference waveform than the current obtained from the conventional dead-beat control (Fig.4.13 (c)). The corresponding current error waveforms, as contrasted in Fig.4.13 (d), show persistently large current tracking error (more than 3 times that from the proposed

method) from the conventional method. The accurate current tracking gives the effective mitigation of the voltage imbalance on the receiving end, leading to a good performance of power flow control. Fig.4.14 (a) and (b) depict the active and reactive power waveforms when tracking the required powers under unbalanced voltages. For the proposed method, both powers follow the corresponding references accurately, though there are small oscillations due to the inevitable noises in the real-time control. However, the power waveforms derived from the conventional deadbeat control present severe oscillations at twice the line frequency value of 50Hz. The peak-to-peak value for the active power is 0.015pu and the reactive power which is about 0.008pu are not acceptable. This is due to that the receiving end unbalanced voltage is not eliminated effectively.

Table 4.4 lists the basic operations for the proposed deadbeat with the time delay compensation method and the well-known positive and negative sequence–based scheme by Hilmy Awad et al. In this section, the DDSRF, the delay compensator and the PWM operations used by both schemes are not included. As can be seen there are in total 57 basic operations in implementing the proposed method per sample interval, but the ± sequence–based scheme requires 76 operations per sample. Thus the proposed scheme is computationally more efficient.

Table 4.5: The basic operations of the proposed method and ±sequence–based method

Basic operations	Proposed method	Conventional method
Addition	30	40
Multiplication	15	20
Division	12	16

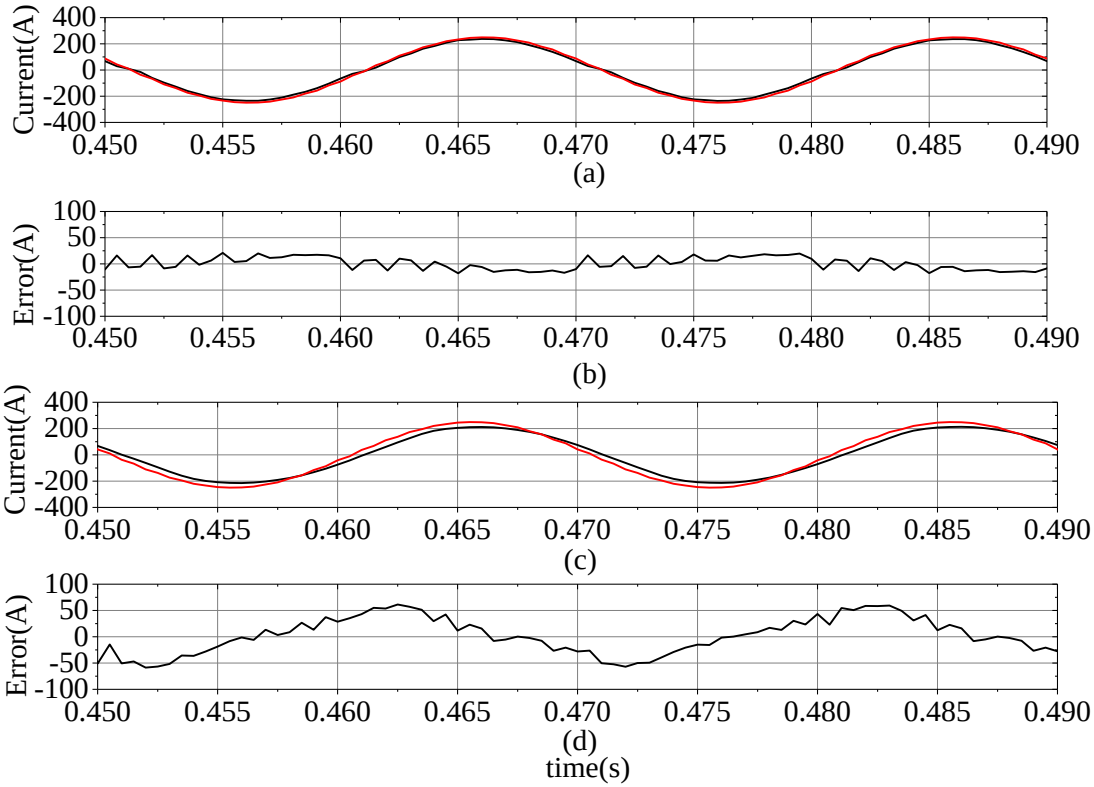


Figure 4.13: The receiving end (a) the waveform of reference (red) and the measured (black) current for the proposed method and (b) the error between these two waveforms (c) the waveform of the reference (red) and the measured (black) current for the conventional method and (d) the error between these two waveforms

4.6.2 Scenario 2: Fault at Power Line Receiving End

When the voltage dip arises at the electrical line receiving end from 0.2 sec. (shown in point 2 in Fig. 4.3), and is also a two-phase-to-ground fault, the responses to the voltage and current waveforms are shown in Fig.4.15 (a)-(c). The voltage imbalance appears at the receiving end with the unbalanced ratio being 6%, (Fig.4.15 (c)) between 0.2s and 0.6s. The sending end voltages (Fig.4.15 (a)) are not affected due to the line impedance which is relatively low, but the current becomes significantly unbalanced as seen in Fig.4.15 (b), with the unbalanced ratio as high as 40%. As

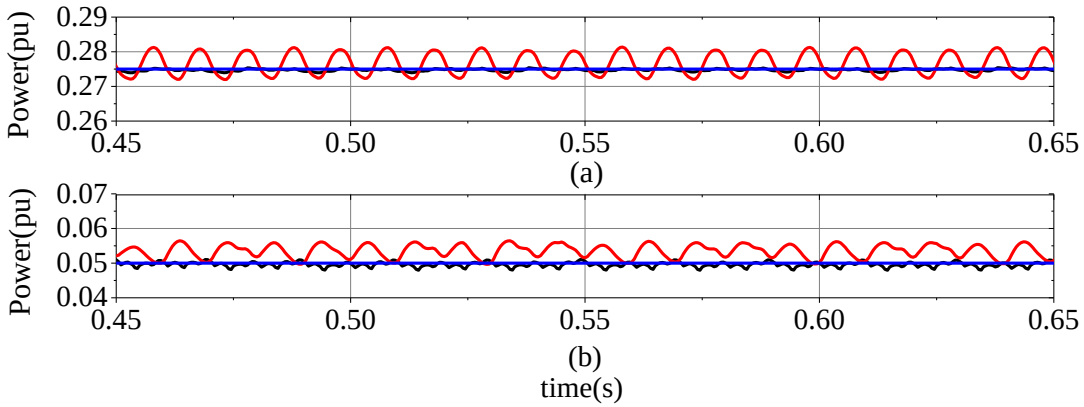


Figure 4.14: The receiving end measured powers compared to the reference powers (blue) (a) the active powers by the proposed method (black) and the conventional deadbeat method (red) (b) the reactive powers by the proposed method (black) and the conventional deadbeat method (red)

the TL-SSSC is switched on to the voltage imbalance compensation from 0.4 sec, the sending and receiving end currents become well-balanced as shown in Fig.4.15 (b). This demonstrates that the TL-SSSC is able to protect the power supply from the load side voltage faults. The injected compensating voltage, as seen in Fig.4.15 (d) is unbalanced, the peak phase voltage, in this case, is within its rated level.

The benefit of mitigating the voltage imbalance by the TL-SSSC to the grid side power transfer can be observed from the power waveforms shown in Fig.4.16. For the time duration from 0.2 sec to 0.4 sec when the TL-SSSC compensation is not applied, both the active and reactive powers present a high level of oscillations with the peak-to-peak value being 0.05pu for the former and 0.06pu for the latter, around their respective mean levels of 0.33pu and 0.075pu. At 0.4s, when the voltage mitigation is enabled, the sending end active and reactive powers can be observed to be maintained at the required levels free of oscillations. Thus it can be stated that the grid supply is well protected from the load side voltage unbalance.

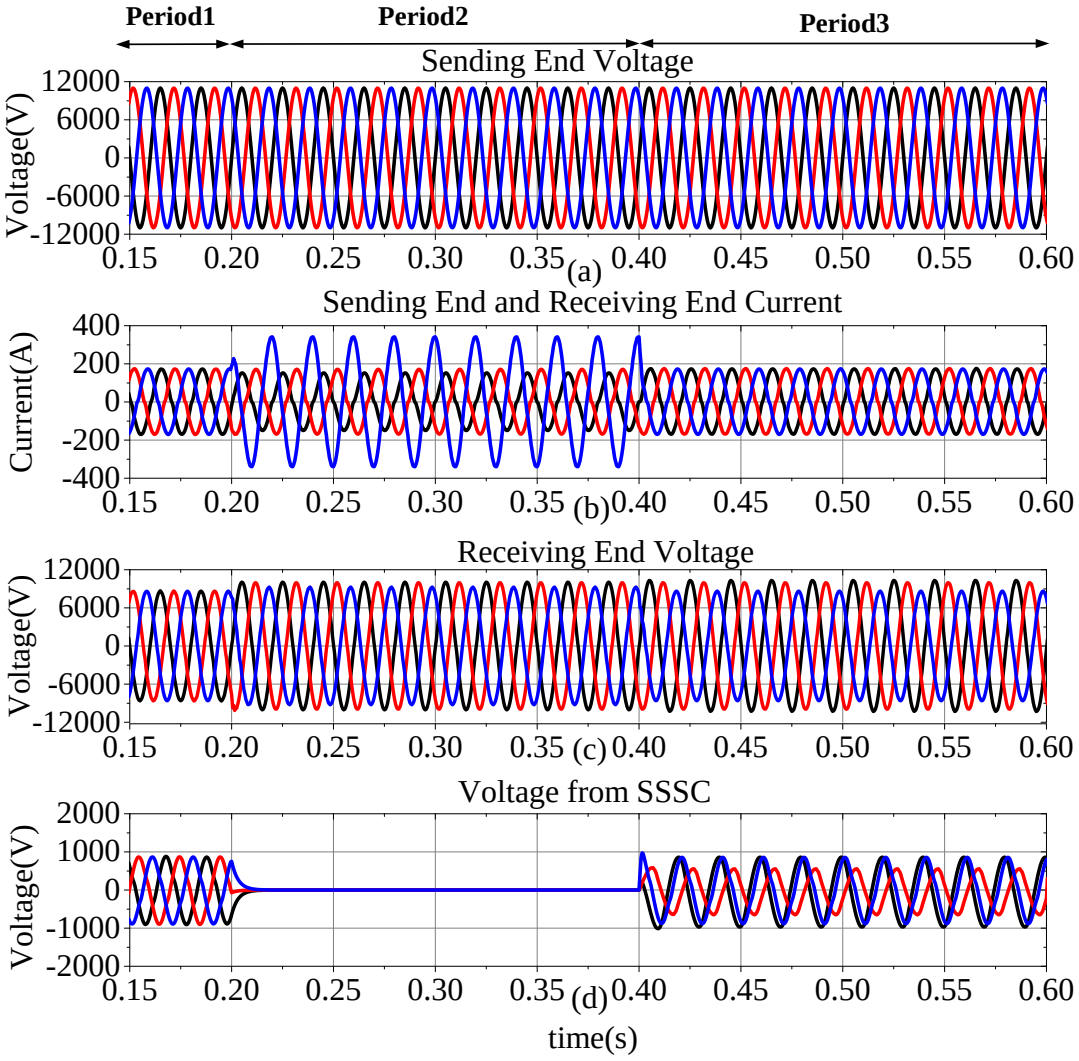


Figure 4.15: The measured waveforms from the proposed method for scenario 2 (a) the sending end voltages, (b) the sending end and receiving end currents (c) the receiving end voltages, (d) the TL-SSSC generated voltage

4.6.3 Scenario 3: Fault at Load Side Bus-Bar Generator

The fault may occur at the output terminals of a grid-tie converter connecting a renewable sourced generator to the load bus-bar. The generator may be a PV, a wind generator, or an energy storage device supplying the local load. To demonstrate the effectiveness of the TL-SSSC control under different load requirements, a 4th

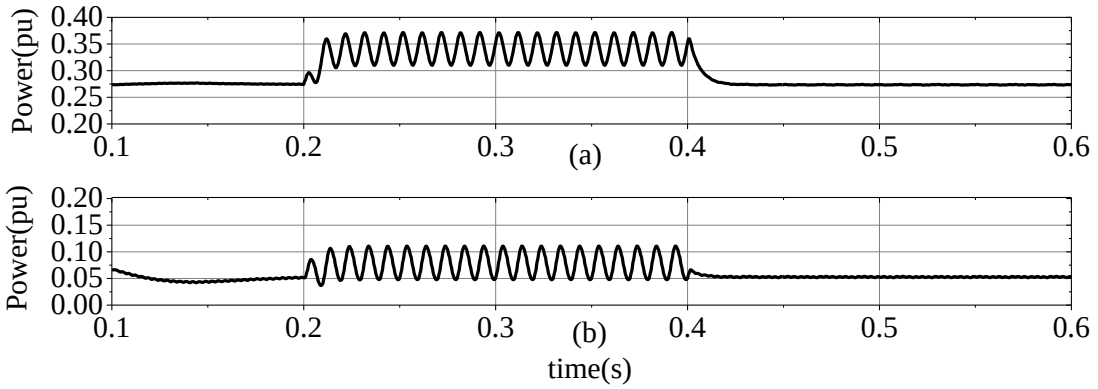


Figure 4.16: (a) The active power and (b) the reactive power at the grid sending end

period is added for this scenario.

As can be seen in Fig.4.17 (a) to (e), during period 1 from 0s to 0.2s, no fault occurs, and the system operates under the normal condition, supplying the load required power of 0.5 pu. During period 2 from 0.2s to 0.4s, the voltage sag occurs at the load side generator inverter. The TL-SSSC, however, is not switched on for the unbalanced voltage mitigation, hence the inverter output current is unbalanced with a ratio of about 71.88%. The load side current, however, is not polluted by the inverter fault, since the receiving end is supplying most of the load power with its current unbalanced ratio being about 3.7%.

To prevent the inverter fault from distorting the currents from the supplying end through the receiving side hence affecting the power network, the TL-SSSC is switched on to the voltage mitigation mode from 0.4s to 0.6s, in period 3. It is also required to ensure that the load power is supplied by the receiving side at 0.275 pu about 55% of the load total required power and the rest is supplied from the inverter side source (Fig.4.18 (a)). As can be seen from Fig.4.17 (b), the performance of the receiving end current is improved, and the current unbalance ratio, now, is reduced to about 2%. The inverter only supplies the remaining 45% of the load power, so its unbalanced ratio is reduced to about 15.72% (Fig.4.17 (c)). The load

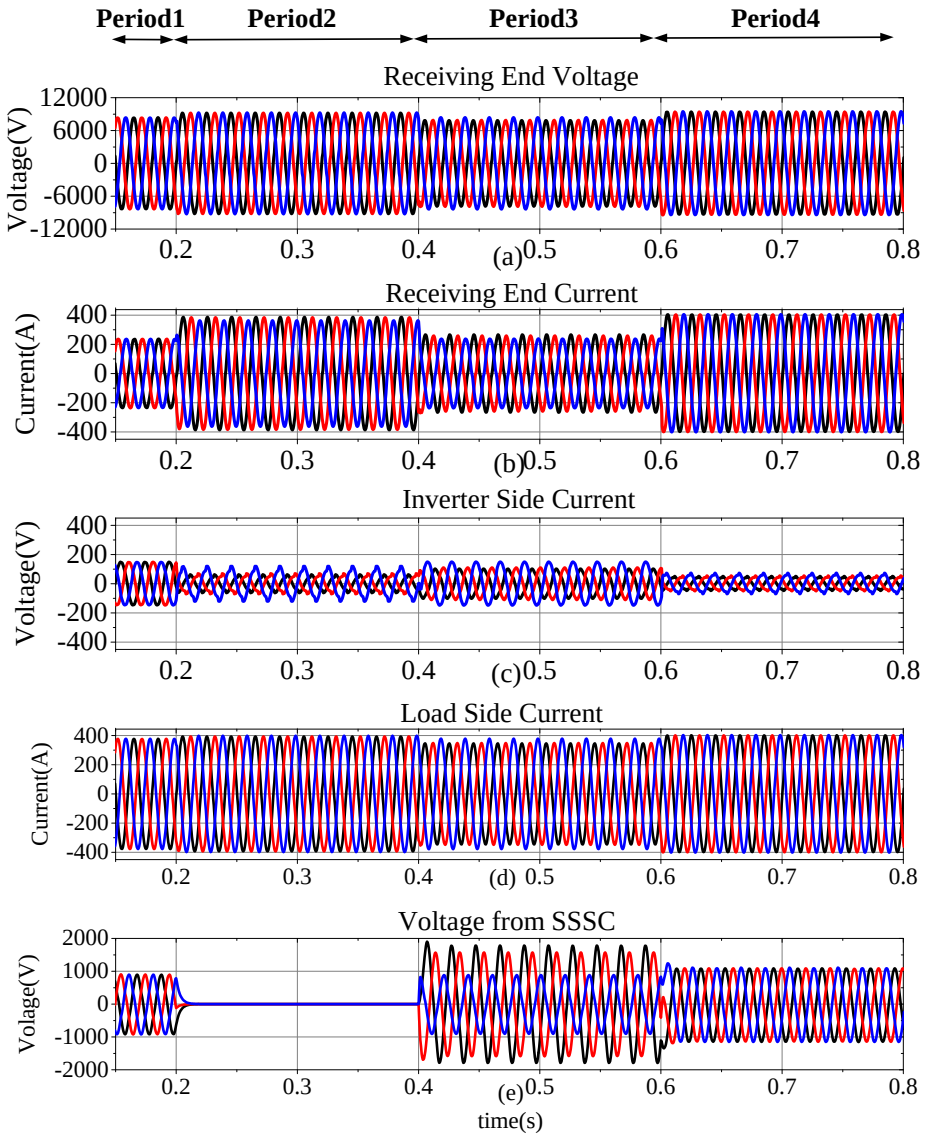


Figure 4.17: The measured waveforms from the proposed method for scenario 3 (a) the receiving end voltages, (b) the receiving end current (c) the inverter side current, (d) the load side current (e) the TL-SSSC generated voltage

current cannot be balanced in this case due to drawing a part of the required power from the faulty inverter connected source. As can be observed in Fig.4.17 (d) period 3, the load current unbalanced ratio is about 3.8%.

The TL-SSSC control is able to isolate the fault of the inverter from affecting

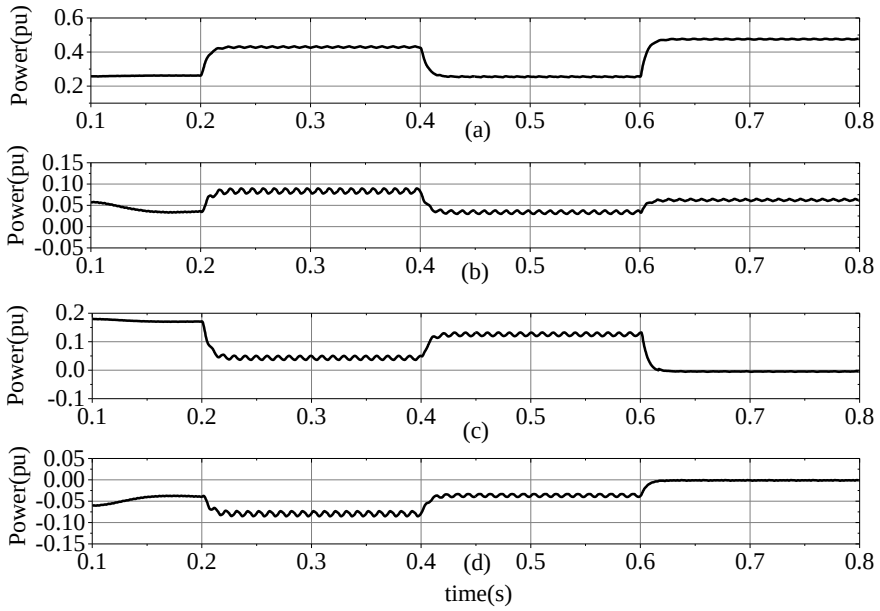


Figure 4.18: (a) The active power and (b) the reactive power at the receiving end (c) the active power and (d) the reactive power at inverters side over 4 periods

the rest of the power line. This is demonstrated by the results displayed in Fig.4.18 (period 4) from 0.6s to 0.8s. The total required load power is controlled by the TL-SSSC to be supplied entirely from the grid side. This means the current drawn from the inverter is minimized. It can be seen in Fig.4.17 (period 4), the current from grid side through the receiving end is balanced, and so is the load side current. The inverter side current is drastically reduced hence the voltage fault is effectively blocked out, affecting little the rest of the power line.

The effectiveness of the TL-SSSC control scheme in isolating the load-end supply voltage sags to the power supply side can be further demonstrated by the power waveforms. Fig.4.18 (a) and (b) show the supplied powers from the receiving side, which is also the grid side, to the load over the four periods. The powers from the inverter side for the same four periods are depicted in Fig.4.18 (c) and (d). During period one, the powers supplied to the load are shared by both the grid side and inverter side under normal operation. Period 2 shows the powers from both

sides when there is an inverter terminal fault and no compensation. In period 3, the TL-SSSC is switched on to enable the real power from the grid side to the load being 55% (0.275 pu). As can be seen, in Fig.4.18 (a)-(d), the real power from the grid side to the load has no oscillation, whereas that from the inverter oscillates. The grid side reactive power presents the oscillations in this condition since it is drawn by the inverter fault. In the final period, when the power required by the load is controlled by the TL-SSSC to be supplied entirely by the grid, the real power from the grid is 0.5pu and the oscillation is free. The active and reactive powers from the load side inverters are almost 0, demonstrating that the fault is not affecting the power flow to the load. During period 2, when the effect of the inverter grounding fault is not controlled by the TL-SSSC, the inverter side draws the reactive power from the grid, and the current unbalance at the inverter side is naturally very high at 71.88%. The load side power is mainly supplied from the grid, though also drawn a small amount from the inverter, hence the grid and the load side current unbalance ratios are low. In Period 3, the TL-SSSC is effective in controlling the power flow and mitigating the unbalance of voltage. The inverter side current unbalance is significantly reduced, and the grid side current distortion is also attenuated. During the final period, due to the effective control by the TL-SSSC, the voltage fault effect is isolated from the supply side so the current imbalance on the supply side is eliminated.

4.7 Conclusions

This paper presented a Transformerless- SSSC and a novel deadbeat control scheme for compensating the voltage distortions of a distribution line while maintaining the required power flow control. The transformerless structure gives the device low cost, light weight, high efficiency, high reliability and fast dynamic re-

sponse. With the proposed control scheme, it overcomes the voltage compensation errors commonly occurring in a traditional SSSC due to the converter filter voltage drop. Incorporating a delay compensator in the control scheme has been shown to be effective in mitigating the control signal errors arising from the computational latency. The validations of a TL-SSSC and the proposed control scheme were performed using a Typhoon-HIL device for the voltage faults arising at three locations on an 11kV power line with the renewable generators. The results have shown the TL-SSSC can achieve the effective isolation of the voltage faults from the rest of the power system and allow the grid to supply the load power required. The performance obtained exceeded that of the phasor of the sequence method.

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CHAPTER 5

MODEL-PREDICTIVE CONTROL OF A PARALLEL TRANSFORMER-LESS STATIC SYNCHRONOUS SERIES COMPENSATOR

5.1 Introduction

To increase the SSSC's power rating, hence extending its control capability and flexibility, it is advantageous to have multiple VSI modules connected in parallel to form a unit and insert it directly into the power line to function as a parallel transformer-less SSSC. The application of the parallel power converters has attracted attention from academia and industry in recent years. The most common configuration has been having paralleled voltage source inverter modules connected to one AC source [1], [2] and their outputs feed the same DC-bus or a motor drive. The power flow can also be from the DC bus to the AC sides, so the parallel inverter unit can also work for interfacing the renewable generators to the grid as well as supplying the compensating current to the grid

as a power conditioner. With each inverter module sharing the required current, this topology is particularly beneficial for applications requiring low voltage and high current, and it greatly increases the converter's reliability and efficiency. In addition by interleaving the output currents from each inverter, it suppresses the current harmonics and improves the system's dynamic performance. The converter topologies being applied for this configuration include the H bridge inverter [3], [4], the neutral point clamped inverter [5], the T-type inverter [6] and so on. However, by connecting the parallel VSI unit in parallel to the power line, it can only deal with the current distortion problems, but not the voltage distortion due to the faults. The reference [7] proposed a configuration having the parallel connected current source inverters (CSI) and is connected into the power system in series, but this still has the same issue as that with a parallel VSI unit wired in parallel to the power grid.

To control directly the power line voltage, a parallel VSI unit needs to be in series connection to the power line hence functioning as a transformerless SSSC as proposed in [8]. In this connection, the three phase limbs of a three phase inverter are separated, each is a single-phase full-bridge inverter, and multiple such inverter cells are parallel to be inserted in one of the three phase lines. These parallel phase cells can be powered individually by a DC source which could be a battery or a renewable-sourced generator, they can also jointly share a single DC source. The configuration enables the power line phase current required for the power flow control and the line voltage adjustment to be distributed to each cell, so that the current handling capacity for the switches in the TL-SSSC be reduced.

One of the main problems for the parallel connections is the circulating current since the parallel inverter cells share a common DC or a AC bus. The circulating current can be generated due to different parameters used in the parallel inverter cells, for example, the filter impedance, the switching frequency or the dead time

implemented in the pulse width modulation scheme [9], [10]. The uneven output voltage/current is another important reason to cause the circulating current problem. This unwanted current increase the losses and decrease the efficiency of the system. The methods for dealing with the circulating current suppression can be divided into three main aspects: the passive methods, the control methods and the modulation methods [6]. For the passive methods, the simplest way is to directly use the inverters with the separate dc sources [4] to avoid the problem from the source. In addition, the isolated transformers can be added to cut off the circulating current path [11]. However, these inevitably increase the system size and the cost and are complicated to implement. For the control methods, the deadbeat control [2] and the PI control [12] schemes were proposed to realize the active mitigation of circulating current. Some studies proposed the nonlinear control method for the circulating current suppression. However, it is difficult to implement these control methods in the practice [13], [14]. The researchers also investigate different pulse width modulation (PWM) techniques. For example, the zero switching vectors used in space vector PWM (SVPWM) can be adjusted for the circulating current cancellation which is proposed in the reference [15]. Moreover, the PWM technique with selective harmonic elimination [16] can also be implemented to alleviate the problem.

This chapter proposes a novel modified model predictive control (MPC) scheme for the parallel TL-SSSCs control. The aim is to obtain the high performance power flow control while suppressing the current circulating directly on the AC sides between the parallel inverter modules. The method stems from the idea that when the line current is equally shared between the modules, their current differences should be zero. Thus by setting the differential current term being zero in the cost function, the optimization procedure of the MPC should ideally be able to derive the reference voltages for each inverter module which ensures accurate reference

current tracking and the near zero circulating current. The chapter presents the new MPC applied to control a parallel TL-SSSC having two converter cells. The circuit models and the cost function defined are derived and the equations for the reference voltage derivation with both equal and unequal reference currents are all given and analyzed. The proposed modified MPC method can be used not only for the voltage balanced power lines, but also for the unbalanced case. The simulation studies for the new MPC method controlling the power flow of a power line with the voltage distortions caused by the faults at three different locations are performed. The results will be presented which validate the effectiveness of using the parallel TL-SSSC for realizing the required power flow control and protecting the power system when faults happen.

The chapter is structured as follows: Subsection 5.2 and subsection 5.3 show the configuration and per phase power line model of the parallel TL-SSSC. In subsection 5.4, the model predictive control for the balance case and the cost function minimization with the equal and the unequal reference current are analyzed. The model predictive control for the unbalanced case is given in subsection 5.5. Subsection 5.6 shows the overall control diagram and subsection 5.7 present the simulation results to validate the proposed method.

5.2 The Configuration of a Power Line with a Parallel TL-SSSC

The single line configuration of a simplified power network with a parallel TL-SSSC is shown in Fig.5.1. In the principle, multiple full-bridge inverter-based SSSCs can be connected in parallel to form an entity and connected serially in the power line without a transformer, in this work, only two parallel SSSCs are studied. The left-hand side is the sending end with the voltage, v_S, and is regarded as an

infinite bus bar. On the right-hand side, it is the receiving end, with the voltage, v_R, where the loads and the renewable sourced generators may be connected via their respective grid-tied AC-DC inverters. The parallel TL-SSSC is serially connected between Bus2 and Bus3. Each of the two converters, the SSSC1 and the SSSC2, has three full-bridge inverters which are isolated. The two inverters connected in parallel on the same phase line share a DC source which is either a battery + a capacitor or a renewable sourced generator. The circuit diagram for one phase of the parallel TL-SSSC is shown in Fig.5.2. For eliminating the harmonics due to the converter switching and simplifying the topology, two R-L filters instead of LC filter are installed on both AC terminals of a TL-SSSC. Thus the $R_{f1}+j\omega L_{f1}$ and the $R_{f2}+j\omega L_{f2}$ are for the SSSC1, the $R_{f3}+j\omega L_{f3}$ and the $R_{f4}+j\omega L_{f4}$ for the SSSC2. Their parameters are tuned according to the inverter switching frequencies. The cut-off frequency of the RL filter is 250Hz. The distribution line impedances on the sending and receiving ends are $R_S+j\omega L_S$ and $R_R+j\omega L_R$.

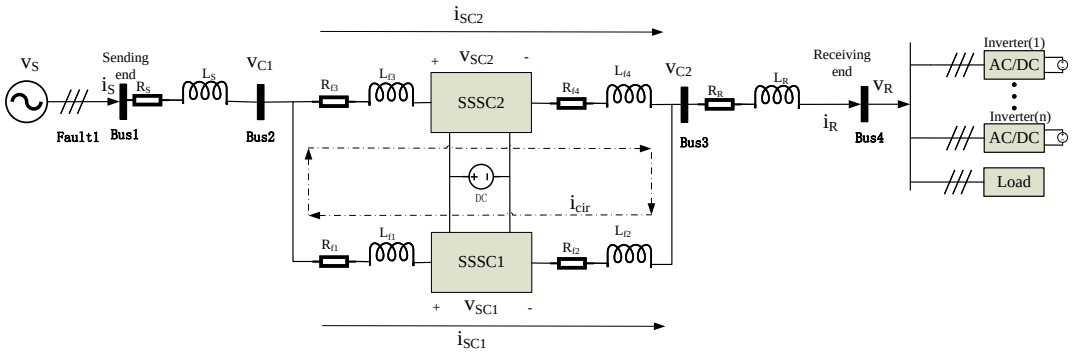

Figure 5.1: The configuration of a power line with a parallel TL-SSSC

5.3 Per-Phase Power Line Model

According to the KVL, the per phase equivalent circuit model for the system in Fig.5.1 with only one of the SSSCs in the parallel TL-SSSC can be expressed as

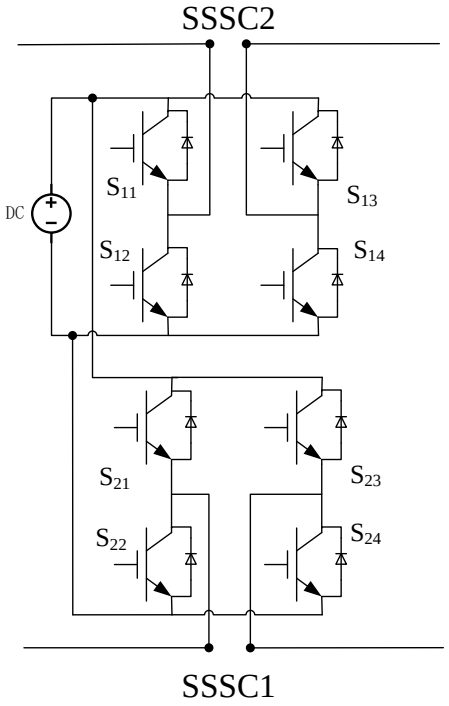

Figure 5.2: The single phase circuit diagram of a parallel TL-SSSC

$$v_{C1m}(t) - v_{SC1m}(t) - v_{C2m}(t) - (R_{f1} + R_{f2}) i_{SC1m}(t) - (L_{f1} + L_{f2}) \frac{d i_{SC1m}(t)}{dt} = 0 \tag{5.1}$$

where the m=a,b,c, the $v_{C1m}(t)$ and $v_{C2m}(t)$ are the measured voltage values at Bus 2 and Bus 3. The voltage across the SSSC1 two terminals is $v_{SC1m}(t)$ and the current flowing into the SSSC1 branch is $i_{SC1m}(t)$.

Assuming the sampling time T_s is very small compared to the time constant of the system, the discrete time expression of the model equation can be changed as:

$$\begin{aligned} v_{C1m}(k) - v_{SC1m}(k) - v_{C2m}(k) - (R_{f1} + R_{f2}) i_{SC1m}(k) \\ -(L_{f1} + L_{f2}) \frac{i_{SC1m}(k+1) - i_{SC1m}(k)}{T_s} = 0 \end{aligned} \tag{5.2}$$

Note that the $v_{C1m}(k)$ is changeable due to the variation of line current $i_{SC1m}(k)$ and the output voltage $v_{SC1m}(k)$ of the parallel TL-SSSC. Likewise, the $v_{C2m}(k)$ is affected by the receiving side current $i_{Rm}(k)$ and the load bus voltage $v_{Rm}(k)$. Hence, the $v_{C1m}(k)$ and $v_{C2m}(k)$ can be expressed respectively as

$$v_{C1m}(k) = v_{Sm}(k) - R_S i_{Sm}(k) - L_S \frac{i_{Sm}(k+1) - i_{Sm}(k)}{T_s} = 0 \tag{5.3}$$

$$v_{C2m}(k) = v_{Rm}(k) - R_R i_{Rm}(k) - L_R \frac{i_{Rm}(k+1) - i_{Rm}(k)}{T_s} = 0 \tag{5.4}$$

where the $i_{Sm}(k)$ and $i_{Rm}(k)$ are the sending and receiving end currents respectively. According to the KIL, these two currents have the same magnitude and phase angle, i.e.

$$i_{sm}(k) = i_{Rm}(k) = i_{SC1m}(k) + i_{SC2m}(k) \tag{5.5}$$

Therefore, combining (5.2) to (5.4), the discrete model equation for the SSSC1 branch is shown as:

$$\begin{aligned} &v_{Sm}(k) - v_{SC1m}(k) - v_{Rm}(k) - (R_{f1} + R_{f2}) i_{SC1m}(k) \\ &-(L_{f1} + L_{f2}) \frac{i_{SC1m}(k+1) - i_{SC1m}(k)}{T_s} - (R_S + R_R) i_{Rm}(k) \\ &-(L_S + L_R) \frac{i_{Rm}(k+1) - i_{Rm}(k)}{T_s} = 0 \end{aligned} \tag{5.6}$$

Substituting the $i_{Rm}(k)$ in above equation by the sum of th e$i_{SC1m}(k)$ and the $i_{SC2m}(k)$ according to (5.5), we have

$$\begin{aligned} &v_{Sm}(k) - v_{SC1m}(k) - v_{Rm}(k) - (R_{f1} + R_{f2}) i_{SC1m}(k) \\ &-(L_{f1} + L_{f2}) \frac{i_{SC1m}(k+1) - i_{SC1m}(k)}{T_s} - (R_S + R_R)(i_{SC1m}(k) + i_{SC2m}(k)) \\ &-(L_S + L_R) \frac{(i_{SC1m}(k+1) + i_{SC2m}(k+1)) - (i_{SC1m}(k) + i_{SC2m}(k))}{T_s} = 0 \end{aligned} \tag{5.7}$$

Similarly, the discrete time current equation for the SSSC2 branch is obtained as (5.8)

$$\begin{aligned} & v_{Sm}(k) - v_{SC2m}(k) - v_{Rm}(k) - (R_{f3} + R_{f4}) i_{SC2m}(k) \\ -(L_{f3} + L_{f4}) & \frac{i_{SC2m}(k+1) - i_{SC2m}(k)}{T_s} - (R_S + R_R)(i_{SC1m}(k) + i_{SC2m}(k)) \\ -(L_S + L_R) & \frac{(i_{SC1m}(k+1) + i_{SC2m}(k+1)) - (i_{SC1m}(k) + i_{SC2m}(k))}{T_s} = 0 \end{aligned} \tag{5.8}$$

5.4 Model Predictive Current Control for Balanced Line Voltages

The main control requirement for the parallel TL-SSSC is to ensure that the active power P and the reactive power Q flowing through the power line meet the required levels set by the load at the receiving end. The model predictive control scheme developed can achieve such a goal for the power line voltages balanced or unbalanced conditions. Its principle is described below.

5.4.1 Reference Current Derivation

The active and the reactive powers at the kth instant at the receiving end can be expressed as:

$$P(k) = v_{Rd}(k) i_{Rd}(k) + v_{Rq}(k) i_{Rq}(k) \tag{5.9}$$

$$Q(k) = v_{Rq}(k) i_{Rd}(k) - v_{Rd}(k) i_{Rq}(k) \tag{5.10}$$

where the $v_{Rd}(k)$ and $v_{Rq}(k)$ are the d and q components of the receiving end voltage taking the sending end voltage as the reference. When the reference active

and reactive powers, P^* and Q^*, are set, with the d-q receiving voltages, the receiving end reference current in d-q can be obtained from (5.11)and (5.12).

$$i_{Rq}^* = \frac{P^*(k)v_{Rq}(k) - Q^*(k)v_{Rd}(k)}{v_{Rd}^2(k) + v_{Rq}^2(k)} \tag{5.11}$$

$$i_{Rd}^* = \frac{P^*(k)v_{Rd}(k) + Q^*(k)v_{Rq}(k)}{v_{Rd}^2(k) + v_{Rq}^2(k)} \tag{5.12}$$

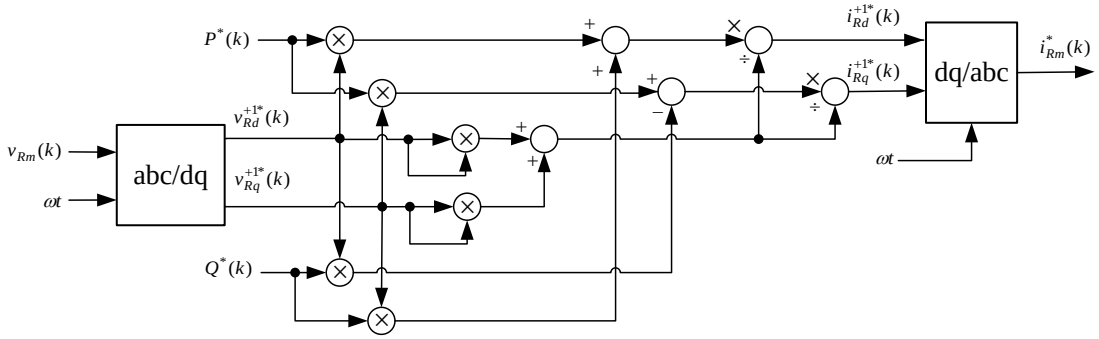

Figure 5.3: The diagram of the reference current generation for the balance case

Fig 5.3 illustrates the reference current derivation procedure. Using the inverse park transformation which is shown in (5.13), the reference receiving end current in the a-b-c frame can be obtained.

$$\begin{bmatrix} i_{Ra}^*(k) \\ i_{Rb}^*(k) \\ i_{Rc}^*(k) \end{bmatrix} = \begin{bmatrix} cos\omega t & -sin\omega t \\ cos(\omega t - \frac{2\pi}{3}) & -sin(\omega t - \frac{2\pi}{3}) \\ cos(\omega t + \frac{2\pi}{3}) & -sin(\omega t + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} i_{Rd}^*(k) \\ i_{Rq}^*(k) \end{bmatrix} \tag{5.13}$$

The derived per phase reference current $i_{Rm}^*(k)$, enables evaluating the two SSSC terminal voltages, v_{SC1m} and v_{SC2m}, according to the model equations (5.7) and (5.8). Based on (5.5), two SSSCs share $i_{Rm}(k)$, so assuming they have the

same power rating, the reference current values applied to both converter branches should be the same, $0.5i^*_{Rm}(k)$. This means that the voltages estimated for both SSSCs be ideally equal. Naturally, If the power ratings of two SSSC branches are different, say, the power rating of SSSC1 is one-third higher than that of SSSC2, the reference currents for two converters are 2/3 and 1/3 of the $i^*_{Rm}(k)$, consequently the resultant v_{SC1m} and v_{SC2m} magnitudes and phase angles are different.

5.4.2 Cost Function for Equal Reference Current

Ideally, with the evaluated reference voltages applied, the current flowing in each SSSC branch tracks its corresponding reference value, resulting in the power transferred to the load side meeting the required levels. However, in practice, there may be a current flowing within the two SSSC branches, called the circulating current as noted by the dotted line in Fig.5.1. This is due to that the AC output voltages across both converter branches may not follow the reference values at every sampling instant and there are harmonics due to the differences in the switching devices, the filter values and the digital switching signals, etc. The circulating current may exist even when the reference currents for both branches are identical. This causes unwanted power losses in the parallel TL-SSSC resulting in the device overheating and low efficiency.

To suppress the circulating current while achieving the high performance reference power tracking in the power line, the definitions of a common mode and a differential mode current elements are set in the MPC for the case when only two parallel SSSCs are used. The former is the sum of the two converter currents written as $(i_{SC1m}(k) + i_{SC2m}(k))$ equal to the receiving end current $i_{Rm}(k)$, which is already defined. The differential mode current is a half difference between the currents of two branches, i.e. 0.5*$(i_{SC1m}(k) - i_{SC2m}(k))$. The MPC needs to suppress the differential mode current while tracking accurately the common mode current.

This can be achieved by defining a cost function incorporating both two current modes as follows.

1. Setting two converter branch circuits identical; this is done by making sure that the four converter R-L filters for two SSSCs have their parameters the same and the reference current for both $i^*_{SC1m}(k)$ and $i^*_{SC2m}(k)$ equal to half of $i^*_{Rm}(k)$. So we have the equation given as:

$$0.5i^*_{Rm}(k) = i^*_{SC1m}(k) = i^*_{SC2m}(k) \tag{5.14}$$

so the predicted currents at the (k+1)th instant are approximately equal:

$$i_{SC1m}(k+1) \approx i_{SC2m}(k+1) \tag{5.15}$$

Subsequently (5.7) and (5.8) can be rewritten respectively as:

$$\begin{aligned} v_{Sm}(k) - v_{SC1m}(k) - v_{Rm}(k) - (2R_{f1} + R_S + R_R - \frac{2L_{f1} + L_S + L_R}{T_s}) i_{SC1m}(k) \\ -(R_S + R_R - \frac{L_S + L_R}{T_s}) i_{SC2m}(k) - 2\left(L_{f1} + L_S + L_R\right) \frac{i_{SC1m}(k+1)}{T_s} \end{aligned} \tag{5.16}$$

and

$$\begin{aligned} v_{Sm}(k) - v_{SC2m}(k) - v_{Rm}(k) - (2R_{f1} + R_S + R_R - \frac{2L_{f1} + L_S + L_R}{T_s}) i_{SC2m}(k) \\ -(R_S + R_R - \frac{L_S + L_R}{T_s}) i_{SC1m}(k) - 2\left(L_{f1} + L_S + L_R\right) \frac{i_{SC2m}(k+1)}{T_s} \end{aligned} \tag{5.17}$$

Using A, B and C to represent the terms with the constant parameters in the above equations, we have (5.18) and (5.19) shown below:

$$\frac{1}{A} i_{SC1m}(k+1) = U_m(k) - v_{SC1m}(k) - B i_{SC1m}(k) - C i_{SC2m}(k) \tag{5.18}$$

$$\frac{1}{A} i_{SC2m}(k+1) = U_m(k) - v_{SC2m}(k) - B i_{SC2m}(k) - C i_{SC1m}(k) \tag{5.19}$$

where $A = \frac{T_s}{2(L_{f1}+L_S+L_R)}, U_m(k) = v_{Sm}(k) - v_{Rm}(k), B = 2R_{f1} + R_S + R_R - \frac{2L_{f1}+L_S+L_R}{T_s} and C = R_S + R_R - \frac{L_S+L_R}{T_s}$

2. Defining a combined cost function; the cost function consists of two parts, the minimizing current tracking errors for both branches and nonliving the differential mode current, taking phase a as example, it is expressed as

$$\begin{aligned} J_a(k) = (i^*_{SC1a}(k+1) - i_{SC1a}(k+1))^2 + (i^*_{SC2a}(k+1) - i_{SC2a}(k+1))^2 \\ + (i_{SC1a}(k+1) - i_{SC2a}(k+1))^2 \end{aligned} \tag{5.20}$$

The reference current values $i^*_{SC1a}(k+1)$ and $i^*_{SC2a}(k+1)$ at the (k+1)th instant are obtained by $i^*_{SC1a}(k)$ and $i^*_{SC2a}(k+1)$ through reference extrapolation and these two reference values should be identified according to (5.14). The reference value for differential mode current is set to 0. This cost function enables the per phase reference voltages for both converters, $v^*_{SC1a}(k)$ and $v^*_{SC2a}(k)$, not only leading to the accurate current following, but also suppressing the differential current.

5.4.3 Evaluation of the Optimal Phase Voltages

The cost function (5.20) is a quadratic function of two variables $v_{SC1a}(k)$ and $v_{SC2a}(k)$. The optimal solutions of these two phase voltages are derived by solving THE simultaneous equations established as followed.

$$\begin{aligned} \frac{\partial J_a(k)}{\partial v_{SC1a}(k)} = A i^*_{SC1a}(k+1) - A^2 U_a(k) + 2A^2 v_{SC1a}(k) - A^2 v_{SC2a}(k) \\ + (2A^2 B - A^2 C) i_{SC1a}(k) + (2A^2 C - A^2 B) i_{SC2a}(k) = 0 \end{aligned} \tag{5.21}$$

$$\frac{\partial J_a(k)}{\partial v_{SC2a}(k)} = Ai^*_{SC1a}(k+1) - A^2U_a(k) + 2A^2v_{SC2a}(k) - A^2v_{SC1a}(k) \\ +(2A^2B - A^2C)i_{SC2a}(k) + (2A^2C - A^2B)i_{SC1a}(k) = 0 \tag{5.22}$$

The equation 2*(5.21) + (5.22) is used to eliminate $v_{sc2a}(k)$ term, then using 2*(5.22) + (5.21) to offset the $v_{sc1a}(k)$ term, the results are shown as:

$$2Ai^*_{SC1a}(k+1) + Ai^*_{SC2a}(k+1) - 3A^2U_a(k) \\ +3A^2v_{SC1a}(k) + 3A^2Bi_{SC1a}(k) + 3A^2Ci_{SC2a}(k) = 0 \tag{5.23}$$

$$2Ai^*_{SC2a}(k+1) + Ai^*_{SC1a}(k+1) - 3A^2U_a(k) \\ +3A^2v_{SC2a}(k) + 3A^2Bi_{SC2a}(k) + 3A^2Ci_{SC1a}(k) = 0 \tag{5.24}$$

Then the required output voltage for each phase of the SSSC1 and the SSSC2 can be obtained by solving

$$v^*_{SC1a}(k) = -\frac{1}{A}i^*_{SC1a}(k+1) + U_a(k) - Bi_{SC1a}(k) - Ci_{SC2a}(k) \tag{5.25}$$

$$v^*_{SC2a}(k) = -\frac{1}{A}i^*_{SC2a}(k+1) + U_a(k) - Bi_{SC2a}(k) - Ci_{SC1a}(k) \tag{5.26}$$

According to the voltage values derived, the switching duty ratios can be calculated respectively as

$$D_{SC1a}(k) = \frac{v^*_{SC1a}(k)}{v_{dc(k)}} \tag{5.27}$$

$$D_{SC2a}(k) = \frac{v^*_{SC2a}(k)}{v_{dc(k)}} \tag{5.28}$$

where the $v_{dc}(k)$ is the DC voltage from the DC supply of the inverters.

5.4.4 Cost Function for Unequal Reference Current

For unequal reference current, a proportional factor, λ, is introduced to simplify the reference voltage derivation from the cost function. The relationship between two reference currents and the predicted currents at the (k+1)th instant are shown in the following formulae:

$$\lambda i^*_{SC1m}(k) = i^*_{SC2m}(k) \tag{5.29}$$

$$\lambda i_{SC1m}(k+1) \approx i_{SC2m}(k+1) \tag{5.30}$$

Hence, (5.16) and (5.17) are rewritten, respectively, as:

$$\begin{aligned} &v_{Sm}(k) - v_{SC1m}(k) - v_{Rm}(k) - (2R_{f1} + R_S + R_R - \frac{2L_{f1} + L_S + L_R}{T_s}) i_{SC1m}(k) \\ &-(R_S + R_R - \frac{L_S + L_R}{T_s}) i_{SC2m}(k) - \left(2L_{f1} + (1+\lambda)(L_S + L_R)\right) \frac{i_{SC1m}(k+1)}{T_s} \end{aligned} \tag{5.31}$$

and

$$\begin{aligned} &v_{Sm}(k) - v_{SC2m}(k) - v_{Rm}(k) - (2R_{f1} + R_S + R_R - \frac{2L_{f1} + L_S + L_R}{T_s}) i_{SC2m}(k) \\ &-(R_S + R_R - \frac{L_S + L_R}{T_s}) i_{SC1m}(k) - \left(2L_{f1} + (1+\frac{1}{\lambda})(L_S + L_R)\right) \frac{i_{SC2m}(k+1)}{T_s} \end{aligned} \tag{5.32}$$

The above can be simplified by using A_1, A_2, B and C to represent the terms formed by the constant parameters, hence leading to

$$\frac{1}{A_1} i_{SC1m}(k+1) = U_m(k) - v_{SC1m}(k) - B i_{SC1m}(k) - C i_{SC2m}(k) \tag{5.33}$$

$$\frac{1}{A_2} i_{SC2m}(k+1) = U_m(k) - v_{SC2m}(k) - B i_{SC2m}(k) - C i_{SC1m}(k) \tag{5.34}$$

where $A_1 = \frac{T_s}{2L_{f1}+(1+\lambda)(L_S+L_R)}, A_2 = \frac{T_s}{2L_{f1}+(1+\frac{1}{\lambda})(L_S+L_R)}, U_m(k) = v_{Sm}(k) - v_{Rm}(k), B = 2R_{f1} + R_S + R_R - \frac{2L_{f1}+L_S+L_R}{T_s} and C = R_S + R_R - \frac{L_S+L_R}{T_s}$

The cost function for this case is the same as that for the equal reference current case, thus (5.20) is used. The optimal solutions can be solved using the same procedure as that for the equal reference current case. So we solve two simultaneous equations given as

$$\begin{aligned}\frac{\partial J_a(k)}{\partial v_{SC1a}(k)} = i^*_{SC1a}(k+1) - 2A_1(U_m(k) - v_{SC1m}(k) - B i_{SC1m}(k) - C i_{SC2m}(k)) \\ + A_2(U_m(k) - v_{SC2m}(k) - B i_{SC2m}(k) - C i_{SC1m}(k)) = 0\end{aligned} \tag{5.35}$$

$$\begin{aligned}\frac{\partial J_a(k)}{\partial v_{SC2a}(k)} = i^*_{SC2a}(k+1) - 2A_2(U_m(k) - v_{SC2m}(k) - B i_{SC2m}(k) - C i_{SC1m}(k)) \\ + A_1(U_m(k) - v_{SC1m}(k) - B i_{SC1m}(k) - C i_{SC2m}(k)) = 0\end{aligned} \tag{5.36}$$

The equation 2*(5.35) + (5.36) is used to eliminate the $v_{sc2a}(k)$ term, then using 2*(5.36) + (5.35) to offset the $v_{sc1a}(k)$ term, the results are shown as:

$$2i^*_{SC1a}(k+1) + i^*_{SC2a}(k+1) - 3A_1(U_m(k) - v_{SC1m}(k) - B i_{SC1m}(k) - C i_{SC2m}(k)) = 0 \tag{5.37}$$

$$2i^*_{SC2a}(k+1) + i^*_{SC1a}(k+1) - 3A_2(U_m(k) - v_{SC2m}(k) - B i_{SC2m}(k) - C i_{SC1m}(k)) = 0 \tag{5.38}$$

The required output voltages for one of the phases of the SSSC1 and the SSSC2 can be obtained as

$$v^*_{SC1a}(k) = -\frac{2+\lambda}{3A_1} i^*_{SC1a}(k+1) + U_a(k) - B i_{SC1a}(k) - C i_{SC2a}(k) \tag{5.39}$$

$$v^*_{SC2a}(k) = -\frac{2\lambda+1}{3\lambda A_2} i^*_{SC2a}(k+1) + U_a(k) - B i_{SC2a}(k) - C i_{SC1a}(k) \tag{5.40}$$

5.5 Model Predictive Current Control for Unbalanced Line Voltage

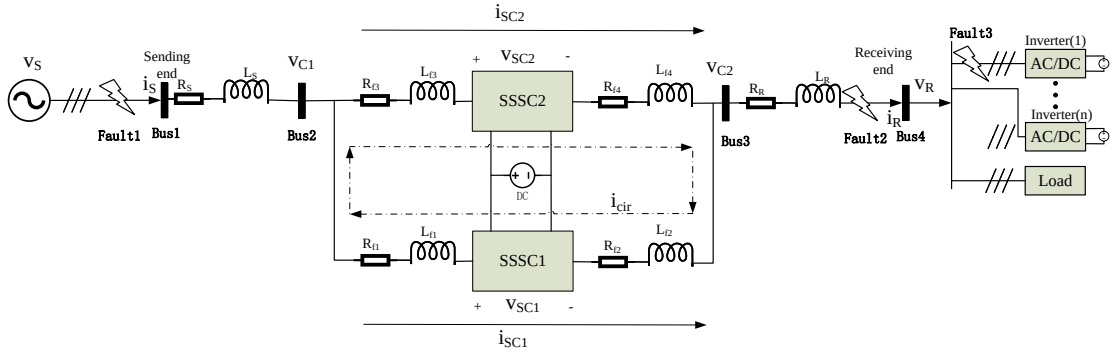

Figure 5.4: The configuration of a power line with a parallel TL-SSSC when the faults happen at different locations

A parallel TL-SSSC can also perform the power flow control when the power line voltages are unbalanced due to faults. Fig. 5.4 shows a power line installed with a parallel TL-SSSC has faults occurring at three different locations. Compared to the balanced case, the only difference when applying the MPC is in the reference current generation, as in this case, the voltage is unbalanced, and the power line voltage and the current present the negative sequence elements and the harmonics. The real and reactive powers are related only to the positive sequence fundamental elements of the voltage and the current by

$$P(k) = v_{Rd}^{+1}(k) i_{Rd}^{+1}(k) + v_{Rq}^{+1}(k) i_{Rq}^{+1}(k) \tag{5.41}$$

$$Q(k) = v_{Rq}^{+1}(k) i_{Rd}^{+1}(k) - v_{Rd}^{+1}(k) i_{Rq}^{+1}(k) \tag{5.42}$$

where the $v_{Rd}^{+1}(k)$ and $v_{Rq}^{+1}(k)$ are the fundamental positive sequence d and q components of the receiving end voltage which can be extracted by applying the decoupled double synchronization reference frame (DDSRF) method. The phase angles of the two voltage sequences, $+\omega t$ and $-\omega t$, derived, are applied to decompose the positive and the negative sequence d-q elements $v_d^{+1}(k)$, $v_q^{+1}(k)$, $v_d^{-1}(k)$ and $v_q^{-1}(k)$ of the receiving end voltage. Note these elements contain not only the DC and the high order harmonic components, but also the significant 2ω oscillatory cross coupling terms between +ve and -ve sequence voltages. These 2ω cross coupling terms need to be eliminated, the +ve and -ve sequence d-q voltage elements can be finally obtained by applying (5.43) and (5.44) as

$$\begin{bmatrix} v_{Rd}^{+1}(k) \\ v_{Rq}^{+1}(k) \end{bmatrix} = \left[F\right] \left(\begin{bmatrix} v_d^{+1}(k) \\ v_q^{+1}(k) \end{bmatrix} - \begin{bmatrix} cos(2\omega t) & sin(2\omega t) \\ -sin(2\omega t) & cos(2\omega t) \end{bmatrix} \begin{bmatrix} v_{Rd}^{-1}(k) \\ v_{Rq}^{-1}(k) \end{bmatrix} \right) \tag{5.43}$$

$$\begin{bmatrix} v_{Rd}^{-1}(k) \\ v_{Rq}^{-1}(k) \end{bmatrix} = \left[F\right] \left(\begin{bmatrix} v_d^{-1}(k) \\ v_q^{-1}(k) \end{bmatrix} - \begin{bmatrix} cos(2\omega t) & -sin(2\omega t) \\ sin(2\omega t) & cos(2\omega t) \end{bmatrix} \begin{bmatrix} v_{Rd}^{+1}(k) \\ v_{Rq}^{+1}(k) \end{bmatrix} \right) \tag{5.44}$$

where $\left[F\right] = \begin{bmatrix} LPF(s) & 0 \\ 0 & LPF(s) \end{bmatrix}$ and the LPF(s) in it represents the low pass filter and the cut-off frequency is set lower than 628.3rad/s eliminating the harmonics greater or equal to the double fundamental frequency. The control diagram of the DDSRF is shown in Fig.5.5.

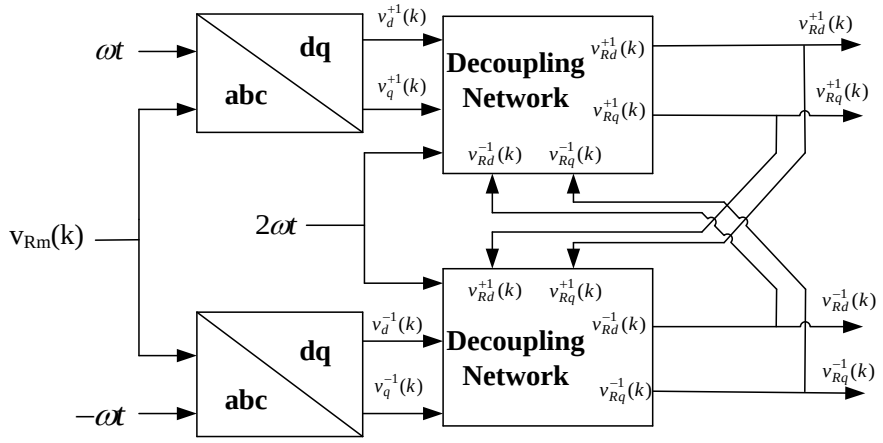

Figure 5.5: The schematic diagram of the DDSRF

Using the derived d-q voltages, when the reference active and reactive powers P^* and Q^*, are set, the reference current d-q components for the receiving end can be obtained as:

$$i_{Rq}^{+1*} = \frac{P^*(k)v_{Rq}^{+1}(k) - Q^*(k)v_{Rd}^{+1}(k)}{v_{Rd}^{+1}(k)^2 + v_{Rq}^{+1}(k)^2} \tag{5.45}$$

$$i_{Rd}^{+1*} = \frac{P^*(k)v_{Rd}^{+1}(k) + Q^*(k)v_{Rq}^{+1}(k)}{v_{Rd}^{+1}(k)^2 + v_{Rq}^{+1}(k)^2} \tag{5.46}$$

The block diagram illustrating the reference current generation for the unbalanced case is shown in Fig.5.6.

Once the per phase reference currents for each SSSC branch are defined, the MPC implementation procedures follow that for the balanced line voltage condition.

5.6 The Overall Control Scheme

The overall control scheme for a parallel TL-SSSC with two SSSCs is illustrated in the diagram shown in Fig.5.7. There are four parts in the diagram, namely the

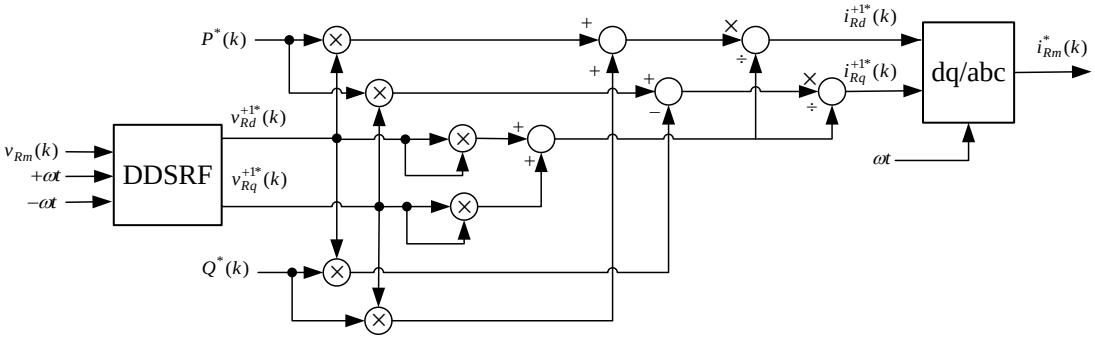

Figure 5.6: The block diagram for the reference current generation for the unbalanced voltage case

reference current generation which can be for the equal and the unequal reference currents, the reference current extrapolation, the cost function minimization and the Pulse-Width-Modulation for the switching signal generation. The reference generation and the cost function minimization have been described in sections 5.4 and 5.5. Hence, in this section, the reference current extrapolation and the PWM switching signals are presented.

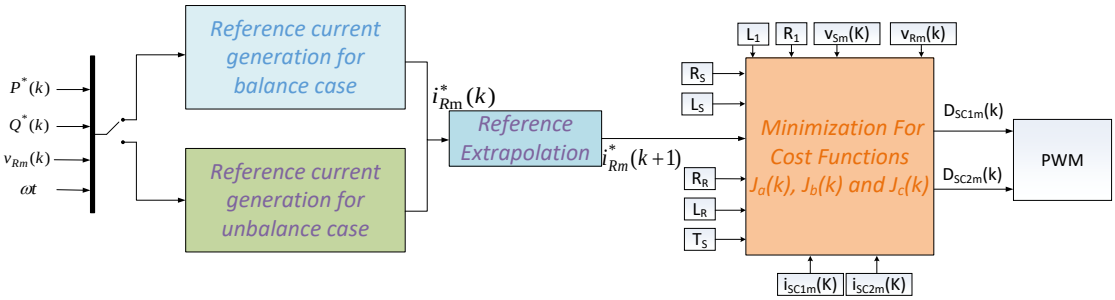

Figure 5.7: The overall control diagram of the parallel TL-SSSC

5.6.1 Reference Current Extrapolation

Since the power flow control relies on tracking the sinusoidal current, the reference current at the (k+1)th instant can be derived by the sine wave extrapolation method

and this is then applied for the cost function minimization. The equation is shown below:

$$\begin{bmatrix} i^*_{Ra}(k+1) \\ i^*_{Rb}(k+1) \\ i^*_{Rc}(k+1) \end{bmatrix} = D(\omega T_s) \begin{bmatrix} i^*_{Ra}(k) \\ i^*_{Rb}(k) \\ i^*_{Rc}(k) \end{bmatrix} \tag{5.47}$$

where $D(\omega T_s)$

$$= \frac{2}{3} \begin{bmatrix} cos(\omega T_s) & -\frac{1}{2}cos(\omega T_s - \frac{\pi}{3}) & -\frac{1}{2}cos(\omega T_s + \frac{\pi}{3}) \\ -\frac{1}{2}cos(\omega T_s + \frac{\pi}{3}) & cos(\omega T_s) & -\frac{1}{2}cos(\omega T_s - \frac{\pi}{3}) \\ -\frac{1}{2}cos(\omega T_s - \frac{\pi}{3}) & -\frac{1}{2}cos(\omega T_s + \frac{\pi}{3}) & cos(\omega T_s) \end{bmatrix}$$

5.6.2 PWM Switching Signal Generation

This follows the well-known Sine-Triangle PWM scheme with the uni-polar switching as shown in Fig.5.8. In this case, two reference voltages generated from the cost function minimization are used. These are converted into the duty ratios, $D_{SC1a}(k)$ and $D_{SC2a}(k)$, as shown in the Figure, one for the SSSC1 and the other for the SSSC2, using, respectively, (5.27) and (5.28). Their respective anti-phase replicas are also plotted in the diagram. The single high frequency triangular carrier wave is applied to compare both $D_{SC1a}(k)$ and $D_{SC2a}(k)$ waveforms as shown in Fig.5.5. The intersections between the reference sine wave signals and the triangular carrier wave determine the pulses and the gaps of the switching signals for both converters SSSC1 and SSSC2. Fig.5.5 also shows the switching pulse for the left-hand-side top switches S_{11} for the SSSC1 and the pulse signal for the right-hand-side top switch S_{13}. The same set of switching signals should be applied to corresponding switches of the SSSC2 when both converters have the same reference current. However, if the reference currents are different, two sets

of the switching signals are generated and they should be applied to the converter according to its assigned reference current.

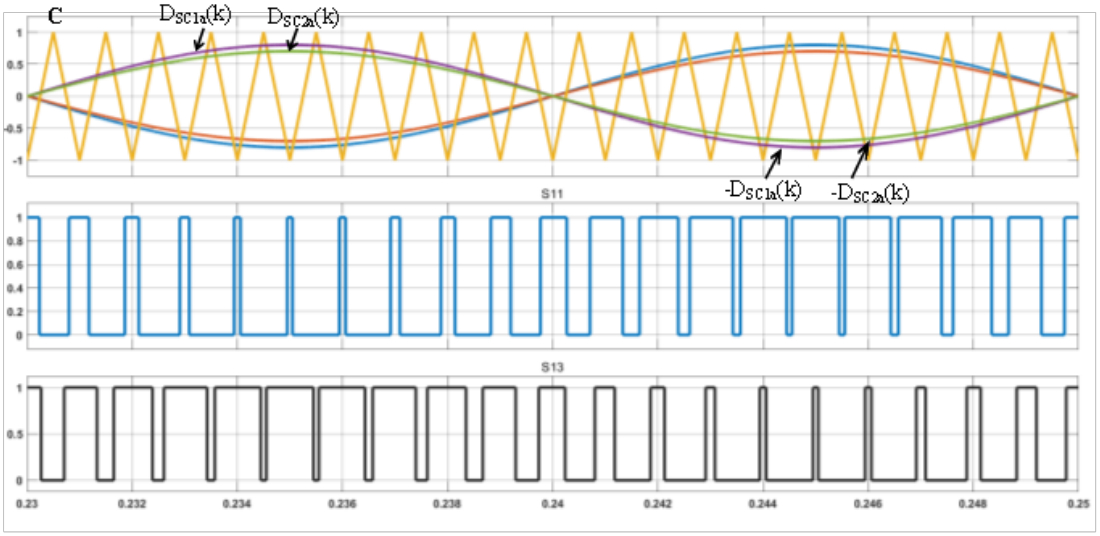

Figure 5.8: The uni-polar PWM for the parallel TL-SSSC and the PWM signals for the switches S_{11} for the SSSC1 and the S_{13} for the SSSC2

5.7 Simulation Studies

To validate the above control scheme, the simulation studies of the power line as shown in Fig.5.1 are performed in MATLAB/Simulink, the system parameters are listed in Table 5.1 below.

5.7.1 Operation Under Balanced Voltages

For the objective of realizing accurate power flow control, for the balanced case, there are two periods to show the results:

Period 1: From 0s to 0.2s, the reference active power is set as 0.1pu and the reactive power is 0pu.

Table 5.1: The parameters of the power line in Fig.5.1

Rated Power P_norm	10MW
Rated Voltage V_norm	11Kv
Sending end voltage V_S	11KV
Distribution Line resistance R_S	1.08Ω
Distribution Line resistance R_R	5.42Ω
Distribution Line Inductance L_S	1.4mH
Distribution Line Inductance L_R	7mH
RL Filter resistance R_{1-4}	0.1Ω
RL Filter Inductance L_{1-4}	2mH
DC input voltage	2000V
Switching frequency	10KHz
Controlling frequency	10KHz

Period 2: From 0.2s to 0.6s, the reference active and the reactive power are set as 0.2pu and -0.1pu.

The measured branch current, the receiving end current and the power flow control results with the equal reference current and the circulating current term implemented into the cost function are shown in Fig.5.9. It can be seen that when the reference active and the reactive power are changed (Fig.5.9 (c) and (d)) at 0.3s, the system takes about 0.02s to settle down which means the model predictive control has a fast and an accurate dynamic response speed. Fig.5.9 (a) shows the SSSC1 and the SSSC2 branch current which is half of the receiving end current shown in Fig.5.9 (b). These results prove that the common mode current and the differential mode current can be realized properly by the model predictive control.

The proposed method discussed in section 5.3 considers setting the same reference current values for the two SSSCs and the cost function includes a term for suppressing the branch circulating current. The effectiveness of the approach can be demonstrated by the current waveforms shown in Fig.5.10. The circulating current is measured between two converter branches when the reference currents for the SSSC1 and the SSSC2 are set as, respectively, two-third and one-third of

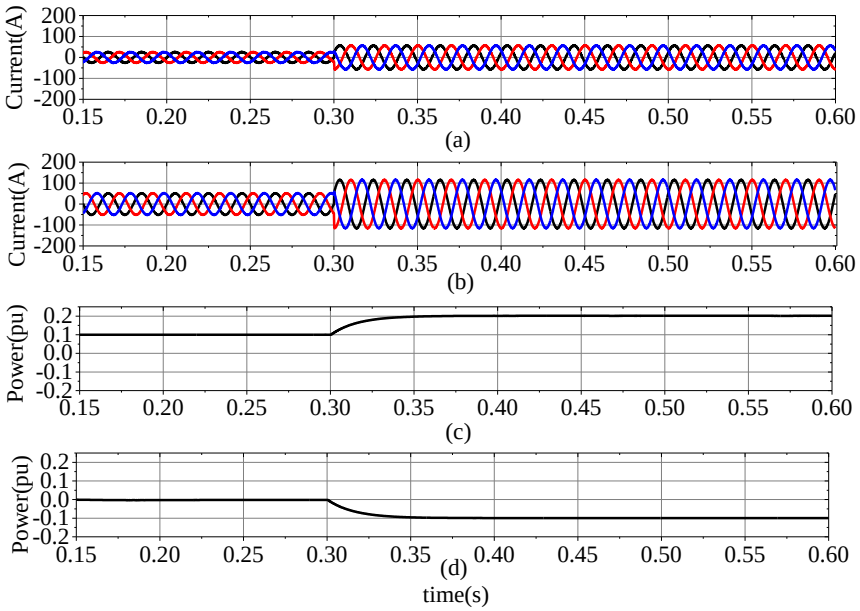

Figure 5.9: (a) The SSSC1 and the SSSC2 branch current (b) the receiving end current (c) the active power and (d) the reactive power at the receiving end for the balanced situation

the receiving-end total reference current. The phase current and the circulating current for when the cost function has and not has the circulating current term are compared and shown in Fig.5.10 (a)-(c) and (d)-(f). Clearly, without setting the differential current terms in the cost function, the currents flowing through two SSSC branches cannot meet the desired reference values. The SSSC1 branch current (red line) is much higher than that through the SSSC2, and they have 180 degree phase difference. The sum of two branch currents (which is about 100A) satisfies the receiving-end current requirement. The circulating current (blue line) is inevitably high which is about 60A peak value as shown in Fig.5.10 (d). At this point, the ratio of the circulating current to the SSSC1 branch current is 54.5%. However, when the circulating current term is set in the cost function, the circulating current can be controlled as that shown in Fig.5.10 (e). The branch current can also be controlled, as shown in Fig.5.10 (b), the SSSC1 supplies two-thirds of the

required current which has a peak value of about 66.67A and the rest (33.32A) is provided by the SSSC2. The circulating current in this situation is reduced with the peak value being about 20A and the ratio for it to the SSSC1 branch current is reduced to 30%, significantly down compared to the case shown in Fig.5.10 (d). The total elimination can only be achieved when both SSSCs are set to share the equal reference current value and the cost function is defined to eliminate the circulating current. As shown in Fig.5.10 (c) and (f), the peak value of two branch currents are both 50A and the circulating current between the two converter branches is almost 0A, the current waveform shows the light oscillation. Hence, the ratio for the circulating current to the SSSC1 current is also almost 0%. The results validate the effectiveness of the proposed method for giving a good power control performance and suppressing the circulating current between two branches.

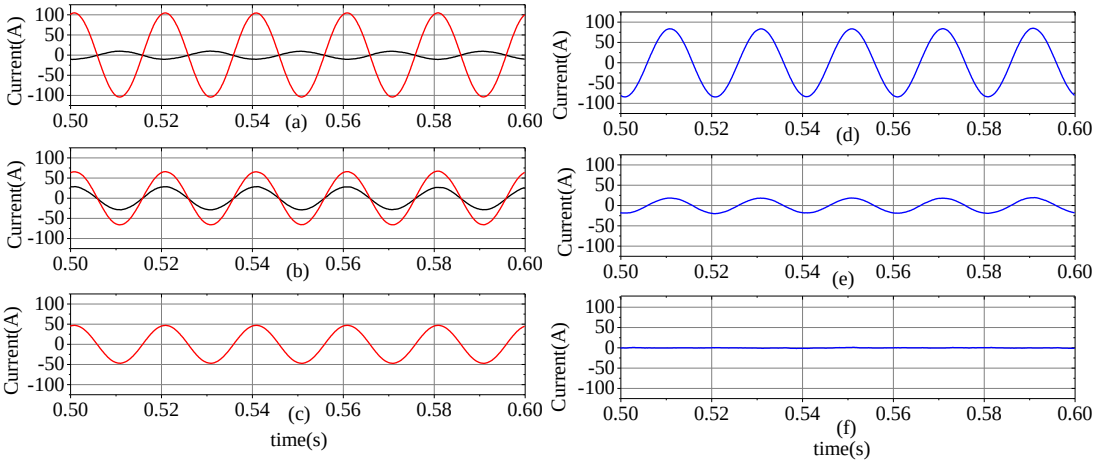

Figure 5.10: The circulating current (blue line) and the currents flowing into the SSSC1 branch (red line) and the SSSC2 branch (black line) (a) and (d) with the different reference current and without the circulating term in the cost function (b) and (e) with the different reference current and with the circulating term in cost function and (c) and (f) with same reference current and with the circulating term in the cost function.

The effective cancellation of the branch circulating current relies on the voltages across both SSSC terminals being identical. This can be difficult to achieve when

the two SSSCs do not share the same reference currents. Fig.5.11 shows the measured one phase output voltages (being filtered by a mean block) for the SSSC1 (black line) with the reference current 1/3 of the total and the SSSC2 (red line) when the reference current is 2/3. It is clear that with the different reference current values and without the circulating current term in the cost function, the difference between the output voltages of the SSSC1 and the SSSC2 (Fig.5.11 (a)) is naturally large. In this case, the two converter filter parameters need to be readjusted to cope with the different current values , hence making their terminal voltage equal. In Fig.5.11 (c), for the equal reference current, the output voltages for two SSSCs are almost the same so the circulating current is almost 0.

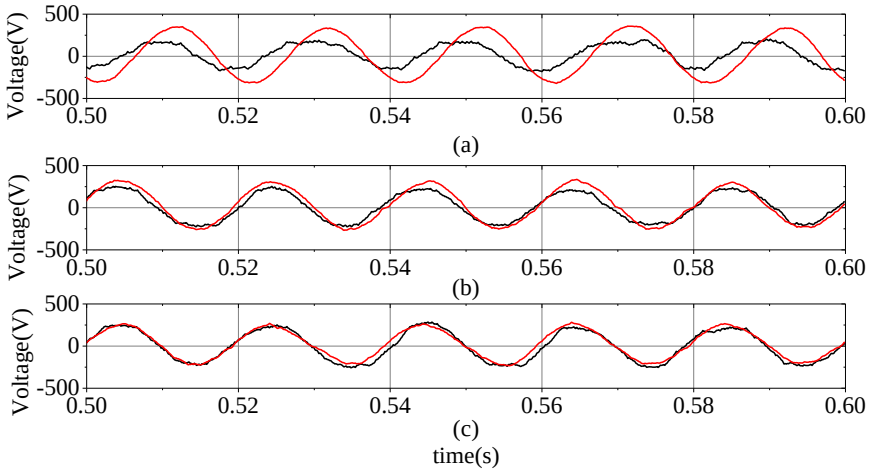

Figure 5.11: The measured phase A voltage for the SSSC1 (black line) and the SSSC2 (red line) (a) with the different reference current and without the circulating term in cost function (b) with the different reference current and with the circulating term in cost function and (c) with the same reference current and with the circulating term in the cost function

5.7.2 Operations Under Unbalanced Line voltages

For the unbalanced voltage operations, the line voltage distortions are caused by THE faults occurring at three different locations, thus three scenarios, as shown in

Fig.5.4; these are the sending end bus bar, the receiving end bus bar and the DG terminals. The reference active and the reactive power are set as 0.2pu and -0.05pu respectively. For all these faults, the parallel TL-SSSC needs to work properly to ensure the power flows through the distribution line safely. The results presented in the following diagrams for all cases are divided into three time periods;

(1) 0s to 0.2s, the system is under the voltage balanced condition, the main purpose of the parallel TL-SSSC is to control the power flow.

(2) 0.2s to 0.4s, the fault occurs at a different position leading to the unbalanced voltage. The parallel TL-SSSC stops working so that the results without the unbalanced voltage compensation can be observed.

(3) 0.4s to 0.6s, the parallel TL-SSSC works for compensating the unbalanced voltage.

5.7.2.1 Scenario 1: Fault at Sending End Bus Bar

The two phase grounding is a fault commonly occurring in the power distribution lines. To emulate this kind of fault, two resistors having different values at the sending end bus bar are inserted. Fig.5.12 (a)-(e) show the measured voltage and current waveforms and the corresponding voltage duty ratios for two SSSCs during the period from 0.15s to 0.6s. The low levels of the unbalanced voltage can incur a huge unbalanced current in the power line which can be seen in Fig.5.12 (a) and (b). Between 0.2s and 0.4s, the parallel TL-SSSC is not switched on, so the sending end voltage unbalanced ratio of only 2% results in almost 45% current imbalance. This unbalanced sending end voltage also influences the receiving end voltage which has about 1.5% unbalanced ratio as can be seen in Fig.5.12 (c). However, during the period from 0.4s to 0.6s, the parallel TL-SSSC starts to mitigate the unbalanced voltage. The unbalanced ratio for the receiving end voltage and current in the distribution line becomes almost 0 which means that they are well balanced

hence demonstrating the control of the parallel TL-SSSC is effective. From Fig.5.12 (d) and (e), the duty ratios for both SSSCs are lower than 0.5 representing that the cooperation of two SSSCs has a large margin to compensate the unbalanced voltage.

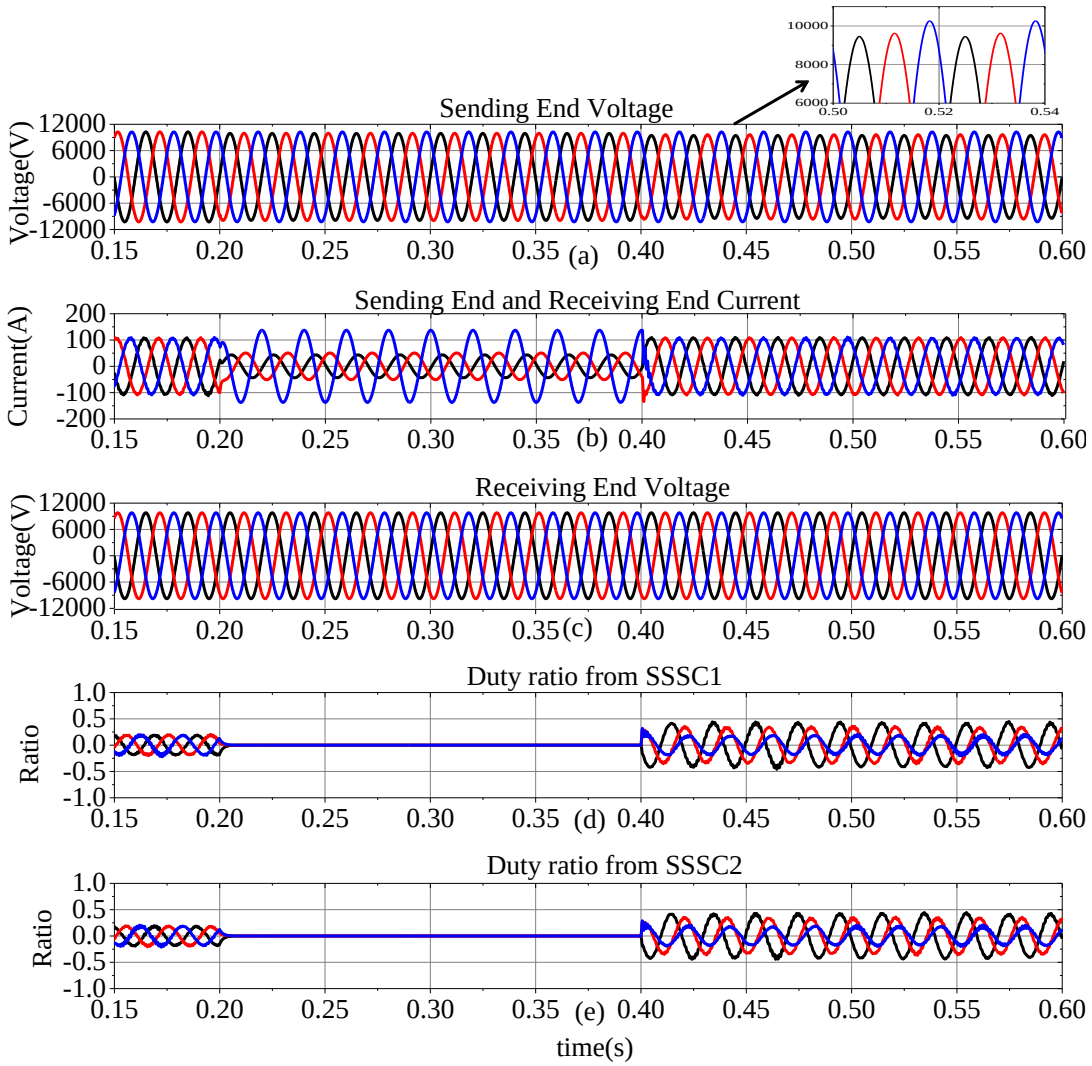

Figure 5.12: Scenario 1: the measured waveforms (a) the sending end voltages, (b) the sending end and receiving end currents, (c) the receiving end voltages, (d) the duty ratio for the SSSC1 and for (e) the SSSC2.

Fig.5.13 shows the measured active (Fig.5.13 (a)) and reactive (Fig.5.13 (b))

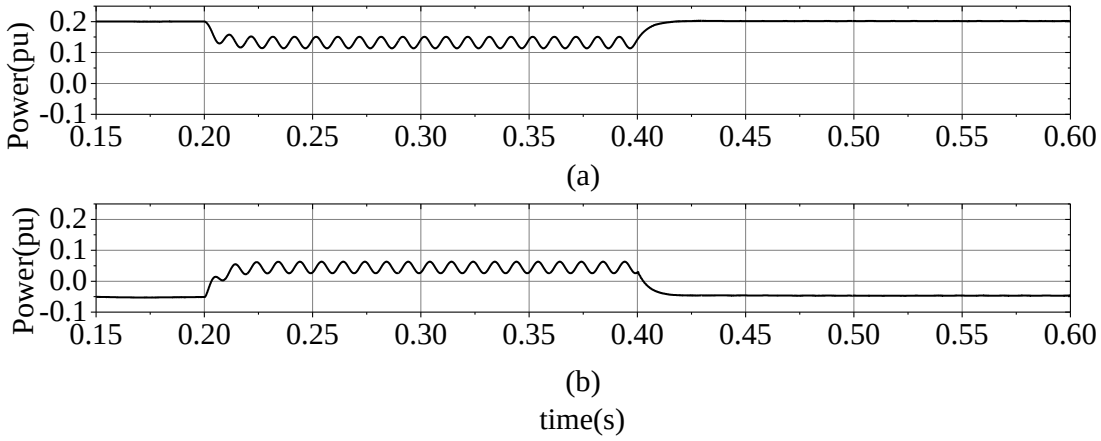

Figure 5.13: (a) The active power and (b) the reactive power at the receiving end .

powers. Except for the time period between 0.2s to 0.4s, the powers can be controlled at the required level without any oscillations which means the receiving end is safe due to the parallel TL-SSSC. However, when the parallel TL-SSSC is not working, the measured powers oscillate because of the interaction between the voltages and the currents with different sequences.

5.7.2.2 Scenario 2: Fault at Receiving End Bus Bar

When the two phase grounding fault occurs at the receiving end, the measured voltages, the currents and the duty ratios are shown in Fig.5.14 (a)-(e). During the period 0.2s to 0.6s, the unbalanced ratio of the receiving end voltage is 4% (Fig.5.14 (c)) which leads to about 55% current imbalance (Fig.5.14 (b)) at both the sending and the receiving end currents when the parallel TL-SSSC is not switched on during the time interval from 0.2 s to 0.4s. The line impedance at the sending end is relatively lower than that at the receiving side as shown in Table 5.1. This implies that the parallel TL-SSSC is installed at a location closer to the sending end bus-bar, consequently, the sending end voltage is not affected by the voltage dips at the receiving end side, naturally, as shown in Fig.5.14 (a), the sending end

voltage is almost well balanced. As the parallel TL-SSSC is switched on to inject the compensating voltages, the unbalanced element in line currents (Fig.5.14 (b)) is mitigated. The peak values for both converter switching duty ratios shown in Fig.5.14 (d) and (e) are about 0.4 which is within the rated level.

The sending end measured active and reactive powers are shown in Fig.5.15. From 0.4s to 0.6s, the sending end active and reactive powers are maintained at a desired value which proves that the injected compensation voltages have already mitigated the influence from the voltage dips at the receiving-end so that the sending-end side is well protected.

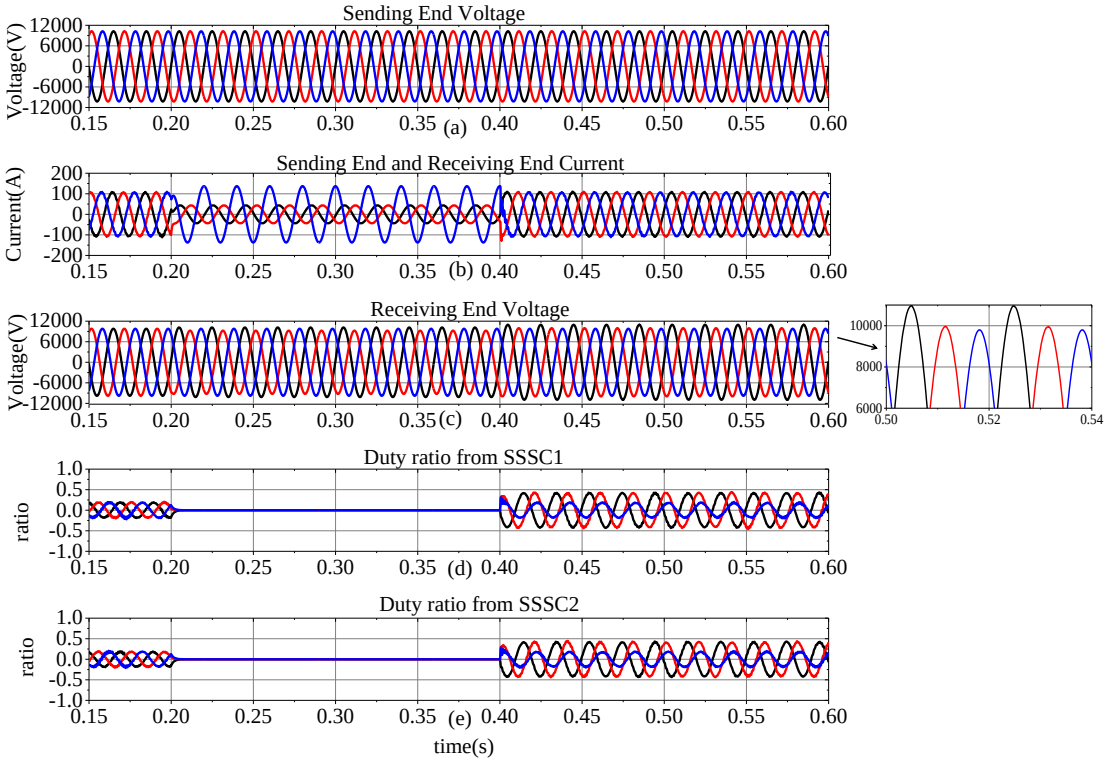

Figure 5.14: Scenario 2: the measured waveforms (a) the sending end voltages, (b) the sending end and receiving end currents, (c) the receiving end voltages, (d) the duty ratio for the SSSC1 and for (e) the SSSC2.

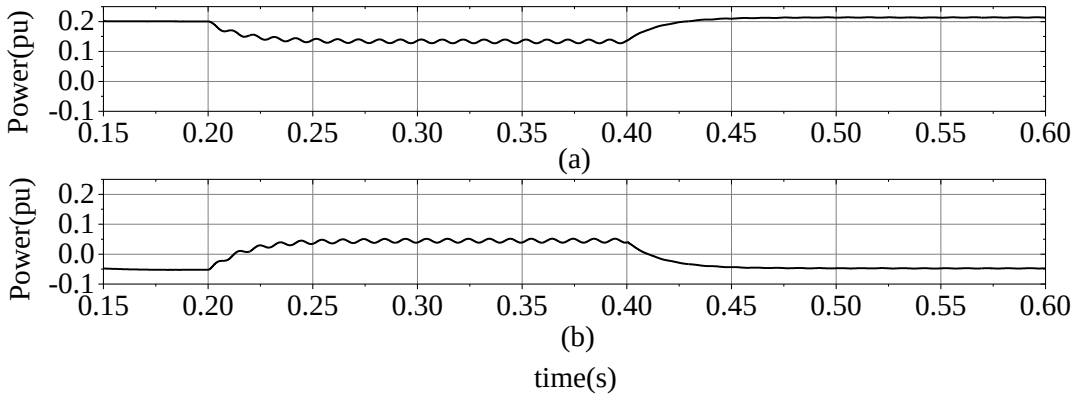

Figure 5.15: (a) The active power and (b) the reactive power at the sending end .

5.7.2.3 Scenario 3: Fault at DG Terminals

It is possible for the distributed generator terminals at the receiving-end bus to have faults which result in unbalanced output voltages for these inverters connected with the renewable sources. In this situation, the aim for the parallel TL-SSSC is to protect the rest of the power line to operate normally without being affected by the faults at the DG terminals. An extra operation time The period from 0.6s to 0.8s is added to show the operations in this condition. As can be seen in Fig.5.16 (a)-(f), the required load active power is 0.25pu and the reactive power is 0pu. In the first time period from 0s to 0.2s, there is no fault occurring, the parallel TL-SSSC is set to provide about 0.1pu active power and 0pu reactive power to the load which can be seen in Fig.5.17 (a) and (b), the rest of the load required power is supplied by the DGs.

During the second time period, the parallel TL-SSSC is not active and the voltage dips occur at the DG terminals side leading to about 70% DG terminal side current imbalance. The DG terminals side needs to supply the total power to satisfy the requirement of the load side and also send power to the receiving end bus bar. It can be seen in Fig.5.16 (b) and (c), the load side current is not polluted by the DG terminals fault. The reason for this is the negative sequence elements

of the DG terminals side current flow into the receiving end side which cause the unbalanced receiving end current with a 10% unbalanced ratio.

In Scenario 3, to protect the other parts of the power line so they operate safely, the best solution is to supply all load required power from the sending end via the parallel TL-SSSC, so that the DG side does not need to send the unbalanced current to the load. This operation mode is demonstrated in the third and the fourth time periods as shown in Fig.5.16. During 0.4s and 0.6s, the parallel TL-SSSC is active to provide 0.1pu active power to the load. In Fig.5.16 (b), the receiving end current is improved and the related unbalanced ratio is reduced to 2%. Since the power provided from the DG terminals side is reduced to 0.15pu, the unbalanced ratio of the current is significantly reduced to about 5%. However, the receiving end side is still influenced by the DG terminals side. The unbalanced ratio of the receiving end voltage in this period is 2.5%. Then in the next stage from 0.6s to 0.8s, the parallel TL-SSSC is controlled to provide 0.25pu (Fig.5.17 (a)) active power to the load side so that the DG terminals side is blocked out and no current is generated which can be seen in Fig.5.16 (d). In this time period, the receiving end and the load side current are well balanced. The unbalanced ratio for the currents in different periods can be seen in Table 5.2.

Table 5.2: The unbalanced ratios for the currents in different periods

Locations	Period 1	Period 2	Period 3	Period 4
Receiving end	0%	10%	2%	0%
DG side	0%	70%	5%	Not available
Load side	0%	0.5%	2%	0%

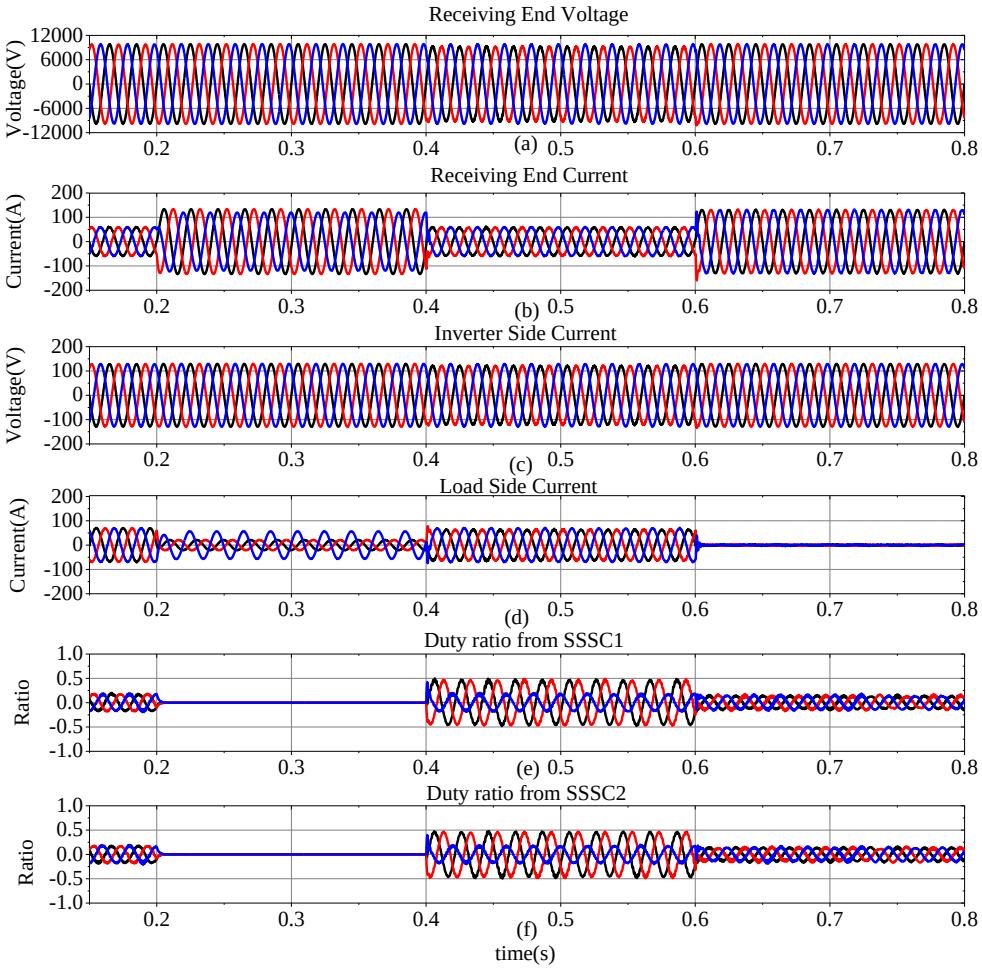

Figure 5.16: Scenario 3: the measured waveforms (a) the receiving end voltages, (b) the receiving end current, (c) the load side current, (d) the DG side current, (e) the duty ratio for the SSSC1 and for (f) the SSSC2.

5.8 Conclusions

This chapter proposed to use the parallel TL-SSSC for the power flow control. The topology offers the advantages of increased power rating, control capability, and high current performance. With the parallel converters connected serially in the power line, there may be circulating currents within the converter branch which inevitably increases the power losses and reduce efficiency. To overcome this

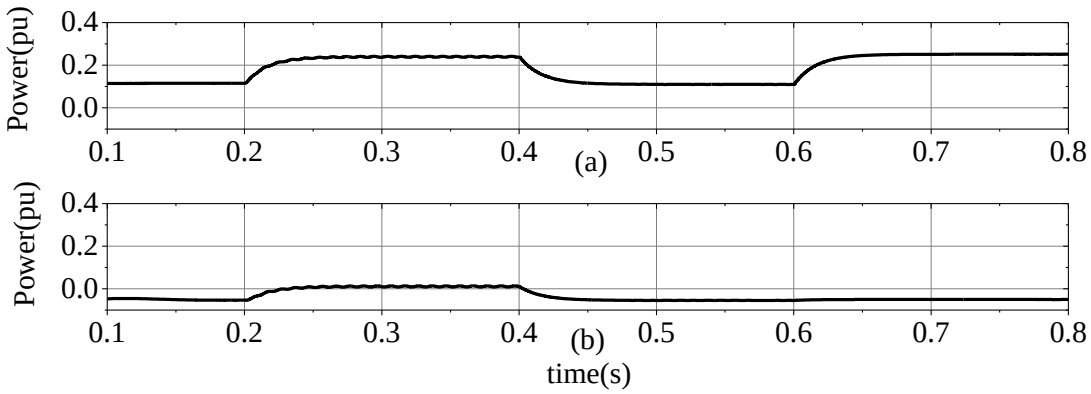

Figure 5.17: (a) The active power and (b) the reactive power at the receiving end

issue, a new modified MPC scheme has been developed specifically for the parallel TL-SSSC with two parallel converters. Using the per phase circuit model for the controller design, the method specified its cost function by adding a differential current term for the circulating current elimination, as well as having the usual reference current tracking term. The simulation studies of the method have shown that for the parallel SSSC with only two converters and they have equal reference currents, the circulation current between branches can be suppressed completely. For unequal reference currents, the method can reduce the circulating current. The method has also been applied successfully for the power flow control when the power line voltages are unbalanced due to the faults at different locations. Another advantage of the modified model predictive control method is even under an unbalanced situation. The equations for the balanced case can be directly used without decomposing the positive and the negative sequence elements of every voltage and current. The only difference is the reference current generation which needs the DDSRF to extract the positive sequence receiving end voltage. The simulation results show that when a fault happens at sending end side, the parallel TL-SSSC can protect the receiving end and the load side. When the receiving end voltage has voltage dips, the parallel TL-SSSC can make sure the sending end

side is unaffected. Moreover, if the DG terminals side has an unbalanced voltage problem, the best solution is for the parallel TL-SSSC to block out the DG terminals side and supply the total power to satisfy the load side requirement.

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CHAPTER 6

CONCLUSIONS AND FUTURE RECOMMENDATION

6.1 Conclusions

This project has been directed at exploring the advanced control techniques that allow the FACTS devices to perform power quality enhancement under the power line conditions of the voltage/current unbalance and waveform distortions. The work has led to a number of successful outcomes; these include: an adaptive harmonic elimination scheme allowing an MMCC-STATCOM to function as a shunt power filter capable of dealing with varying harmonic distortions; a modulated Model- Predictive Control scheme for an MMCC-STATCOM to mitigate unbalanced load current and hence performing required voltage regulation; and a parallel Transformer-less SSSC for the power flow control under the power line voltage distortions. A summary of the achievements and contributions is presented below:

1. A harmonic extraction technique using the modified discrete wavelet-packet transform (DWPT) was developed which is capable of processing the measured power line currents in real-time. The method incorporated a data expansion scheme

to overcome the limitations of the data array boundary effect. The results have shown that the modified DWPT tracks the harmonic changes faster and more accurately than the conventional method.

2. An MMCC-based adaptive power filter was developed. The innovative technique lies in combining a notch filter technique with the DWPT harmonic extraction. The verification of the power filter performance demonstrated its superior ability in fast tracking the load current changes, and giving the accurate elimination of the current harmonics in real-time.

3. In order to mitigate the inter-cluster voltage imbalance of the MMCC-Based STATCOM when compensating unbalanced load current, a novel modular model predictive control (MMPC) was developed. The key feature of the method lies in adding a common mode voltage (CMV) in the current prediction equations of a star-connected MMCC. This affected a zero-sequence voltage inserted into the phase voltages, leading to effective re-balancing of the phase active power, and eliminating the phase cluster voltage drifts.

4. The work also created a modified branch and bound (B&B) algorithm to search for the optimal per-phase switch duty ratios in the MMPC. The computational burden of this adjusted B&B method was reduced compared with that of a traditional quadratic programming solver. Meanwhile, the optimal results obtained from the B&B method only have less than 0.05 error compared with the global optimal results which proves the feasibility of the adjusted B&B method.

5. A novel deadbeat current control scheme with the time delay compensation was proposed which modeled the a-b-c three phase lines with a transformer-less SSSC, plus the L-C filters, separately using the KVL. The method is to predict the current two steps further so that the error caused by the voltage drop of the LC filter can be eliminated.

6. Directly controlling the distribution line current in the a-b-c frame by the

TL-SSSC had a low computational cost because it did not require the negative sequence reference signal for the compensation. This means that a reference signal extraction method under the unbalanced operation became unnecessary. Also the a,b,c phases only require three model equations, instead of four representing the positive and the negative sequence dq components as used in the double vector control method.

7. When the voltage faults occurred at different locations on the distribution microgrid, the results showed that the proposed control scheme by the TL-SSSC was effective in isolating the voltage unbalances of the power line, hence ensuring the balanced current flow required by the load.

8. A modified model predictive control method for the balanced case was proposed for a parallel TL-SSSC to realize the power flow control. The topology offers the advantages of increased power rating, control capability, and high current performance. Another advantage of this control method is that, even in an unbalanced situation, the equations for the balanced case can be directly used without decomposing every voltage and current into the positive and the negative sequence elements.

9. With the parallel converters connected serially in the power line, there may be circulating currents within the converter branch which inevitably increase the power losses and reduce the efficiency. The differential current term added in the cost function and the equal reference current set for the cost function minimization were proposed to eliminate the circulating current.

10. The results proved that a parallel TL-SSSC can also isolate a voltage fault and protect the remainder of the power system. Meanwhile, it can still supply the required power to the load side.

6.2 Future Recommendations

The current research can still be improved and extended. Future recommendations are summarised as follows.

1. The parallel TL-SSSC can be extended to multiple TL-SSSCs connected in parallel. In this case, the circulating current analysis will be more complicated since each branch will cause the extra circulating current to flow into other branches. The cost function implemented in the model predictive control needs to be adjusted for controlling multiple TL-SSSCs.

2. For MMCC-STATCOM, the branch and bound (B&B) method can realize cost function minimization with the constraints. However, this method can not guarantee the global optimal results, although the obtained results are very close to the optimum. This method needs to be improved to further reduce the computational burden and pursue the global optimal results.

3. The TL-SSSC and MMCC-STATCOM can be combined to seek a novel topology of the UPFC. It is possible to investigate the control scheme based on this topology to realize the basic purposes like power flow control.

4. Moreover, the harmonic mitigation and the unbalance compensation can possibly be realized by this UPFC topology. Therefore, the control scheme for solving the above mentioned problems is worth further discussed and improved.

5. Finally, the reference [1] proposed an MMCC-UPFC topology. However, no deeper analysis of this MMCC-UPFC. It is worth paying more attention to this topology to improve its structure or propose a new control method for the different applications.

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APPENDIX

DERIVATION OF MMPC

$$c_2 = -\frac{1}{3}\frac{T_s}{L_f}V_b^{\Sigma}(k)$$

$$b_1 = c_1 = -\frac{1}{3}\frac{T_s}{L_f}V_a^{\Sigma}(k), b_2 = \frac{2}{3}\frac{T_s}{L_f}V_b^{\Sigma}(k)$$

$$b_3 = -\frac{1}{3}\frac{T_s}{L_f}V_c^{\Sigma}(k), c_3 = \frac{2}{3}\frac{T_s}{L_f}V_c^{\Sigma}(k)$$

$$b_4 = -\frac{T_s}{C}I_{cb}(k), c_4 = -\frac{T_s}{C}I_{cc}(k)$$

$$n_{b1} = -\frac{1}{3}\frac{T_s}{L_f}V_c^{\Sigma}(k)S_c(k) - \frac{T_s}{L_f}V_{gb}(k) + \left(1 - \frac{R_f T_s}{L_f}\right)I_{cb}(k) - I_{cb}^{*}(k+1)$$

$$n_{c1} = -\frac{1}{3}\frac{T_s}{L_f}V_c^{\Sigma}(k)S_c(k) - \frac{T_s}{L_f}V_{gc}(k) + \left(1 - \frac{R_f T_s}{L_f}\right)I_{cc}(k) - I_{cc}^{*}(k+1)$$

$$n_{b2} = P_{b2} = V_b^{\Sigma}(k) - V_b^{\Sigma *}(k+1)$$

$$n_{c2} = P_{c2} = V_c^{\Sigma}(k) - V_c^{\Sigma *}(k+1)$$

$$P_{b1} = -\frac{T_s}{L_f} V_{gb}(k) + \left(1 - \frac{R_f T_s}{L_f}\right) I_{cb}(k) - I_{cb}^*(k+1)$$

$$P_{c1} = -\frac{T_s}{L_f} V_{gc}(k) + \left(1 - \frac{R_f T_s}{L_f}\right) I_{cc}(k) - I_{cc}^*(k+1)$$

$$\begin{aligned} n_{a3} = {} & \frac{2}{3}\frac{T_s}{L_f} V_a^{\Sigma}(k) S_a(k) - \frac{1}{3}\frac{T_s}{L_f} V_b^{\Sigma}(k) S_b(k) \\ & - \frac{T_s}{L_f} V_{ga}(k) + \left(1 - \frac{R_f T_s}{L_f}\right) I_{ca}(k) - I_{ca}^*(k+1) \end{aligned}$$

$$\begin{aligned} n_{b3} = {} & -\frac{1}{3}\frac{T_s}{L_f} V_a^{\Sigma}(k) S_a(k) + \frac{2}{3}\frac{T_s}{L_f} V_b^{\Sigma}(k) S_b(k) \\ & - \frac{T_s}{L_f} V_{gb}(k) + \left(1 - \frac{R_f T_s}{L_f}\right) I_{cb}(k) - I_{cb}^*(k+1) \end{aligned}$$

$$\begin{aligned} n_{c3} = {} & -\frac{1}{3}\frac{T_s}{L_f} V_a^{\Sigma}(k) S_a(k) - \frac{1}{3}\frac{T_s}{L_f} V_b^{\Sigma}(k) S_b(k) \\ & - \frac{T_s}{L_f} V_{gc}(k) + \left(1 - \frac{R_f T_s}{L_f}\right) I_{cc}(k) - I_{cc}^*(k+1) \end{aligned}$$

APPENDIX B

C CODE FOR DSP TO CONTROL TYPHOON HIL

The main file for C code program

```
#include "DSP28x_Project.h"     // Device Headerfile and Examples Include
    File

#include "pmsm_speed_ctrl.h"

// Prototype statements for functions found within this file.
void SetupIntTimer(void);           //Configure the Timer interupt
void InitEPwm1(void);               // Configure ePWM module 1
void InitEPwm2(void);               // Configure ePWM module 2
void InitEPwm3(void);               // Configure ePWM module 3
void update_compare(void);
void Adc_Config(void);

interrupt void epwm1_timer_isr(void); // Prototype of the epwm interupt
    service routine

Uint16 tbprd = 4500; // 20 kHz tbprd = Fosc/2/Fsw
```

```
#define RESULTS_BUFFER_SIZE 1024
Uint16 AdcaResults[RESULTS_BUFFER_SIZE];
Uint16 resultsIndex;
float enc_pos_theta;
Uint32 qcnt;

real_t D = 0;

float Ts=200; //us execution rate of the interupt

int Enable = 0;
float Gain = 0;
float ma = 0.25;
float mb = 0.25;
float mc = 0.25;

// inital states for data model from code generation
pmsm_speed_ctrl_ModelData generatedModel;
pmsm_speed_ctrl_ExtIn inputs = {0};
pmsm_speed_ctrl_ExtOut outputs = {0};
pmsm_speed_ctrl_ModelStates states = {0};

void main(void)
{
// Step 1. Initialize System Control:
// PLL, WatchDog, enable Peripheral Clocks
// This example function is found in the F2806x_SysCtrl.c file.
   InitSysCtrl();
   InitPeripheralClocks();

// Step 2. Initalize GPIO:
// This example function is found in the F2806x_Gpio.c file and
// illustrates how to set the GPIO to it's default state.
```

```
49 // InitGpio();  // kipped for this example
50
51 // For this case just init GPIO pins for ePWM1, ePWM2, and TZ pins
52    InitEPwm1Gpio();
53    InitEPwm2Gpio();
54    InitEPwm3Gpio();
55
56 // Step 3. Clear all interrupts and initialize PIE vector table:
57 // Disable CPU interrupts
58    DINT;
59
60 // Initialize the PIE control registers to their default state.
61 // The default state is all PIE interrupts disabled and flags
62 // are cleared.
63 // This function is found in the F2806x_PieCtrl.c file.
64    InitPieCtrl();
65
66 // Disable CPU interrupts and clear all CPU interrupt flags:
67    IER = 0x0000;
68    IFR = 0x0000;
69
70 // Initialize the PIE vector table with pointers to the shell Interrupt
71 // Service Routines (ISR).
72 // This will populate the entire table, even if the interrupt
73 // is not used in this example.  This is useful for debug purposes.
74 // The shell ISR routines are found in F2806x_DefaultIsr.c.
75 // This function is found in F2806x_PieVect.c.
76    InitPieVectTable();
77
78 // Interrupts that are used in this example are re-mapped to
79 // ISR functions found within this file.
80
81 // Step 4. Initialize all the Device Peripherals:
```

```
// This function is found in F2806x_InitPeripherals.c
// InitPeripherals();  // Not required for this example


   EALLOW;
   SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 0;
   EDIS;

// EPWM initilization
   InitEPwm1();
   InitEPwm2();
   InitEPwm3();

   SetupIntTimer();

   InitAdc();  // For this example, init the ADC
   AdcOffsetSelfCal();



// Enable global Interrupts and higher priority real-time debug events:
   EINT;   // Enable Global interrupt INTM
   ERTM;   // Enable Global realtime interrupt DBGM

// TB clock enabled initilization
   EALLOW;
   SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 1;
   EDIS;

   // define initial states for data model from code generation
   generatedModel.p_extIn = &inputs;
   generatedModel.p_extOut = &outputs;
```

```
115     generatedModel.p_States = &states;
        pmsm_speed_ctrl_init(&generatedModel);
117
119     // Configure ADC
            EALLOW;
121         AdcRegs.ADCCTL2.bit.ADCNONOVERLAP = 1;  // Enable non-overlap mode
            AdcRegs.ADCCTL1.bit.INTPULSEPOS = 1;    // ADCINT1 trips after
                AdcResults latch
123         AdcRegs.INTSEL1N2.bit.INT1E     = 1;    // Enabled ADCINT1
            AdcRegs.INTSEL1N2.bit.INT1CONT  = 0;    // Disable ADCINT1
                Continuous mode
125         AdcRegs.INTSEL1N2.bit.INT1SEL   = 1;    // setup EOC1 to trigger
                ADCINT1 to fire
            AdcRegs.ADCSOC0CTL.bit.CHSEL    = 7;    // set SOC0 channel select
                to ADCINA7
127         AdcRegs.ADCSOC0CTL.bit.TRIGSEL  = 9;    // set SOC0 start trigger
                on EPWM1A, due to round-robin SOC0 converts first then SOC1
            AdcRegs.ADCSOC0CTL.bit.ACQPS    = 6;    // set SOC0 S/H Window to 7
                 ADC Clock Cycles, (6 ACQPS plus 1)
129         AdcRegs.ADCSOC1CTL.bit.CHSEL    = 9;    // set SOC0 channel select
                to ADCINA7
            AdcRegs.ADCSOC1CTL.bit.TRIGSEL  = 9;    // set SOC0 start trigger
                on EPWM1A, due to round-robin SOC0 converts first then SOC1
131         AdcRegs.ADCSOC1CTL.bit.ACQPS    = 6;    // set SOC0 S/H Window to 7
                 ADC Clock Cycles, (6 ACQPS plus 1)
            AdcRegs.ADCSOC2CTL.bit.CHSEL    = 2;    // set SOC0 channel select
                to ADCINA7
133         AdcRegs.ADCSOC2CTL.bit.TRIGSEL  = 9;    // set SOC0 start trigger
                on EPWM1A, due to round-robin SOC0 converts first then SOC1
            AdcRegs.ADCSOC2CTL.bit.ACQPS    = 6;    // set SOC0 S/H Window to 7
                 ADC Clock Cycles, (6 ACQPS plus 1)
135         AdcRegs.ADCSOC3CTL.bit.CHSEL    = 10;    // set SOC0 channel select
```

```
        to ADCINA7
    AdcRegs.ADCSOC3CTL.bit.TRIGSEL  = 9;    // set SOC0 start trigger
        on EPWM1A, due to round-robin SOC0 converts first then SOC1
137 AdcRegs.ADCSOC3CTL.bit.ACQPS    = 6;    // set SOC0 S/H Window to 7
        ADC Clock Cycles, (6 ACQPS plus 1)
    AdcRegs.ADCSOC4CTL.bit.CHSEL    = 0;    // set SOC0 channel select
        to ADCINA7
139 AdcRegs.ADCSOC4CTL.bit.TRIGSEL  = 9;    // set SOC0 start trigger
        on EPWM1A, due to round-robin SOC0 converts first then SOC1
    AdcRegs.ADCSOC4CTL.bit.ACQPS    = 6;    // set SOC0 S/H Window to 7
        ADC Clock Cycles, (6 ACQPS plus 1)
141 AdcRegs.ADCSOC5CTL.bit.CHSEL    = 8;    // set SOC0 channel select
        to ADCINA7
    AdcRegs.ADCSOC5CTL.bit.TRIGSEL  = 9;    // set SOC0 start trigger
        on EPWM1A, due to round-robin SOC0 converts first then SOC1
143 AdcRegs.ADCSOC5CTL.bit.ACQPS    = 6;    // set SOC0 S/H Window to 7
        ADC Clock Cycles, (6 ACQPS plus 1)
    AdcRegs.ADCSOC6CTL.bit.CHSEL    = 1;    // set SOC0 channel select
        to ADCINA7
145 AdcRegs.ADCSOC6CTL.bit.TRIGSEL  = 9;    // set SOC0 start trigger
        on EPWM1A, due to round-robin SOC0 converts first then SOC1
    AdcRegs.ADCSOC6CTL.bit.ACQPS    = 6;    // set SOC0 S/H Window to 7
        ADC Clock Cycles, (6 ACQPS plus 1)
147 AdcRegs.ADCSOC7CTL.bit.CHSEL    = 15;    // set SOC0 channel select
        to ADCINA7
    AdcRegs.ADCSOC7CTL.bit.TRIGSEL  = 9;    // set SOC0 start trigger
        on EPWM1A, due to round-robin SOC0 converts first then SOC1
149 AdcRegs.ADCSOC7CTL.bit.ACQPS    = 6;    // set SOC0 S/H Window to 7
        ADC Clock Cycles, (6 ACQPS plus 1)
    AdcRegs.ADCSOC8CTL.bit.CHSEL    = 12;    // set SOC0 channel select
        to ADCINA7
151 AdcRegs.ADCSOC8CTL.bit.TRIGSEL  = 9;    // set SOC0 start trigger
        on EPWM1A, due to round-robin SOC0 converts first then SOC1
```

```
        AdcRegs.ADCSOC8CTL.bit.ACQPS     = 6;     // set SOC0 S/H Window to 7
             ADC Clock Cycles, (6 ACQPS plus 1)
153     AdcRegs.ADCSOC9CTL.bit.CHSEL     = 5;     // set SOC0 channel select
            to ADCINA7
        AdcRegs.ADCSOC9CTL.bit.TRIGSEL   = 9;     // set SOC0 start trigger
            on EPWM1A, due to round-robin SOC0 converts first then SOC1
155     AdcRegs.ADCSOC9CTL.bit.ACQPS     = 6;     // set SOC0 S/H Window to 7
             ADC Clock Cycles, (6 ACQPS plus 1)
        AdcRegs.ADCSOC10CTL.bit.CHSEL    = 13;     // set SOC0 channel
            select to ADCINA7
157     AdcRegs.ADCSOC10CTL.bit.TRIGSEL  = 9;     // set SOC0 start trigger
            on EPWM1A, due to round-robin SOC0 converts first then SOC1
        AdcRegs.ADCSOC10CTL.bit.ACQPS    = 6;     // set SOC0 S/H Window to
            7 ADC Clock Cycles, (6 ACQPS plus 1)
159     AdcRegs.ADCSOC11CTL.bit.CHSEL    = 3;     // set SOC0 channel select
             to ADCINA7
        AdcRegs.ADCSOC11CTL.bit.TRIGSEL  = 9;     // set SOC0 start trigger
            on EPWM1A, due to round-robin SOC0 converts first then SOC1
161     AdcRegs.ADCSOC11CTL.bit.ACQPS    = 6;     // set SOC0 S/H Window to
            7 ADC Clock Cycles, (6 ACQPS plus 1)
        EDIS;
163

165 // Step 6. IDLE loop. Just sit and loop forever (optional):
    for(;;)
167 {
        __asm("           NOP");
169 }

171 }

173 void InitEPwm1(void)
    {
```

```
175     EALLOW;

177     //Time Base block configuration
        EPwm1Regs.TBCTL.bit.CTRMODE = 2;     //up-down counter counter
179     EPwm1Regs.TBCTL.bit.CLKDIV = 0;
        EPwm1Regs.TBCTL.bit.HSPCLKDIV = 0;   //TBCLK pre-scaler = /1
181     EPwm1Regs.TBPRD = tbprd;             //tbprd = 10000, Set period to
            2000 counts (50kHz)


183

        EPwm1Regs.TBCTL.bit.SYNCOSEL = 0;
185     EPwm1Regs.TBPHS.all = 0;

187     //Action Qualifier configuration
        EPwm1Regs.AQCTLA.bit.CAU=1;
189     EPwm1Regs.AQCTLA.bit.CAD=2;
        EPwm1Regs.AQCTLB.bit.CBU=2;
191     EPwm1Regs.AQCTLB.bit.CBD=1;

193     EPwm1Regs.TBCTL.bit.SYNCOSEL = 1;

195     // Counter Compare block configuration:
        EPwm1Regs.CMPA.half.CMPA  = D*tbprd;
197
        // Dead Band block configuration:
199     EPwm1Regs.DBCTL.bit.HALFCYCLE = 0;  //0: Full cycle clocking enabled.
            The dead-band counters are clocked at the TBCLK rate.
        //EPwm1Regs.DBCTL.bit.DEDB_MODE = 0;  //Rising edge delay and falling
            edge delay applied to source
201                                         //selected by S4 switch (INMODE
                                                bits) and output to B signal
                                                path
                                            //only. Note: When this bit is set
```

```
                                        to 1, user should always
                                        either set
203                                 //OUT_MODE bits such that Apath =
                                        InA OR OUTSWAP bits such
                                    //that OutA=Bpath
205     EPwm1Regs.DBCTL.bit.OUT_MODE = 3;   //11: DBM is fully enabled (i.e.
        both RED and FED active)
        EPwm1Regs.DBCTL.bit.POLSEL = 2;     //10: Active high complementary (
        AHC). EPWMxB is inverted.
207     EPwm1Regs.DBCTL.bit.IN_MODE= 0;     //00: EPWMxA In (from the action-
        qualifier) is the source for both
                                    //rising-edge delay and falling-
                                        edge delayed signal.
209     //EPwm1Regs.DBRED.all = 10;          //200*1/foc
        //EPwm1Regs.DBFED.all = 10;
211
        EPwm1Regs.DBRED = 10;           //200*1/foc
213     EPwm1Regs.DBFED = 10;


215
        EPwm1Regs.ETSEL.bit.SOCAEN  = 0;    // Disable SOC on A group
217     EPwm1Regs.ETSEL.bit.INTEN = 1;      //Enable ePWM Interrupt (EPWMx_INT
        ) Generation
                                    //1: Enable EPWMx_INT generation
219


221
        EPwm1Regs.ETSEL.bit.SOCASEL = 2;            //010: Enable event time-
        base counter equal to period (TBCTR = TBPRD)
223
        EPwm1Regs.ETSEL.bit.INTSEL = 1;             //001: Enable event time-
        base counter equal to zero. (TBCTR = 0x00)
225
```

```
    EPwm1Regs.ETPS.bit.INTPRD = 1;            // Generate INT on 1st
        event
227
229                                          //This selects which of the
                                                 possible events will
                                                 trigger an interrupt or
                                                 start an ADC conversion.
    EPwm1Regs.ETSEL.bit.SOCAEN = 1;          //Enable the ADC Start of
        Conversion A (EPWMxSOCA) Pulse
231                                          //1: Enable EPWMxSOCA pulse.
    EPwm1Regs.ETPS.bit.SOCAPRD = 1;           // Generate pulse on 1st
        event
233

235
    // Setup shadow register load on ZERO
237 EPwm1Regs.CMPCTL.bit.SHDWAMODE = 0;
    EPwm1Regs.CMPCTL.bit.SHDWBMODE = 0;
239 EPwm1Regs.CMPCTL.bit.LOADAMODE = 0;
    EPwm1Regs.CMPCTL.bit.LOADBMODE = 0;
241
    EDIS;
243 }

245 void InitEPwm2(void)
    {
247     EALLOW;

249     //Time Base block configuration
    EPwm2Regs.TBCTL.bit.CTRMODE = 2;     // Freeze counter
251 EPwm2Regs.TBCTL.bit.CLKDIV = 0;
    EPwm2Regs.TBCTL.bit.HSPCLKDIV = 0;  // TBCLK pre-scaler = /1
```

```
253     EPwm2Regs.TBPRD = tbprd;            // tbprd = 10000, Set period to
            2000 counts (50kHz)

255     //EPwm3Regs.TBCTL.bit.SWFSYNC = 1;
        EPwm2Regs.TBCTL.bit.PHSEN = 1;                  // Enable phase loading
257     EPwm2Regs.TBPHS.all = 0;

259     //Action Qualifier configuration
        EPwm2Regs.AQCTLA.bit.CAU=1;
261     EPwm2Regs.AQCTLA.bit.CAD=2;
        EPwm2Regs.AQCTLB.bit.CBU=2;
263     EPwm2Regs.AQCTLB.bit.CBD=1;

265     // Counter Compare block configuration:
        EPwm2Regs.CMPA.half.CMPA  = D*tbprd;
267


269     // Dead Band block configuration:
        EPwm2Regs.DBCTL.bit.HALFCYCLE = 0;  //0: Full cycle clocking enabled.
            The dead-band counters are clocked at the TBCLK rate.
271     //EPwm2Regs.DBCTL.bit.DEDB_MODE = 0;  //Rising edge delay and falling
            edge delay applied to source
                                          //selected by S4 switch (INMODE
                                              bits) and output to B signal
                                              path
273                                       //only. Note: When this bit is set
                                              to 1, user should always
                                              either set
                                          //OUT_MODE bits such that Apath =
                                              InA OR OUTSWAP bits such
275                                       //that OutA=Bpath
        EPwm2Regs.DBCTL.bit.OUT_MODE = 3;   //11: DBM is fully enabled (i.e.
            both RED and FED active)
```

```
277     EPwm2Regs.DBCTL.bit.POLSEL = 2;      //10: Active high complementary (
            AHC). EPWMxB is inverted.
        EPwm2Regs.DBCTL.bit.IN_MODE= 0;      // 00: EPWMxA In (from the action-
            qualifier) is the source for both
279                                          //rising-edge delay and falling-
                                                 edge delayed signal.
        EPwm2Regs.DBRED = 10;            // 200*1/foc
281     EPwm2Regs.DBFED = 10;


283

        EPwm2Regs.ETSEL.bit.SOCAEN  = 0;     // Disable SOC on A group
285     EPwm2Regs.ETSEL.bit.INTEN = 1;       //Enable ePWM Interrupt (EPWMx_INT
            ) Generation
                                                 //1: Enable EPWMx_INT
                                                     generation
287

            //This selects which of the possible events will trigger an
                interrupt or start an ADC conversion.
289     EPwm2Regs.ETSEL.bit.SOCAEN = 1;              //Enable the ADC Start of
            Conversion A (EPWMxSOCA) Pulse
                                                         //1: Enable EPWMxSOCA
                                                             pulse.
291

        EPwm2Regs.ETSEL.bit.SOCASEL = 1;             //EPWMxSOCA Selection
            Options,These bits determine when a EPWMxSOCA pulse will be
            generated.
293                                                      //Enable event time-
                                                             base counter equal
                                                             to zero or period
                                                     //(TBCTR = 0x00 or
                                                         TBCTR = TBPRD). This
                                                          mode is useful in
                                                         up-down count mode.
```

```
295
297     EPwm2Regs.ETSEL.bit.INTSEL = 1;             //ePWM Interrupt (EPWMx_INT
            ) Selection Options
                                                        //Enable event time-
                                                            base counter equal
                                                            to zero or period
299                                                     //(TBCTR = 0x00 or
                                                            TBCTR = TBPRD). This
                                                             mode is useful in
                                                            updown count mode.
301     EPwm2Regs.ETPS.bit.INTPRD = 1;              // Generate INT on 1st
            event
303     EPwm2Regs.ETSEL.bit.SOCAEN = 1;              // Enable SOCA
        EPwm2Regs.ETPS.bit.SOCAPRD = 1;              // Generate pulse on 1st
            event
305
        // Setup shadow register load on ZERO
307     EPwm2Regs.CMPCTL.bit.SHDWAMODE = 0;
        EPwm2Regs.CMPCTL.bit.SHDWBMODE = 0;
309     EPwm2Regs.CMPCTL.bit.LOADAMODE = 0;
        EPwm2Regs.CMPCTL.bit.LOADBMODE = 0;
311
        EDIS;
313 }

315 void InitEPwm3(void)
    {
317     EALLOW;

319     //Time Base block configuration
```

```
    EPwm3Regs.TBCTL.bit.CTRMODE = 2;              // Freeze counter
321 EPwm3Regs.TBCTL.bit.CLKDIV = 0;
    EPwm3Regs.TBCTL.bit.HSPCLKDIV = 0;            // TBCLK pre-scaler = /1
323 EPwm3Regs.TBPRD = tbprd;                      // tbprd = 10000, Set period
        to 2000 counts (50kHz)

325 EPwm3Regs.TBCTL.bit.SWFSYNC = 1;
    EPwm3Regs.TBCTL.bit.PHSEN = 1;                // Enable phase loading
327 //EPwm3Regs.TBPHS.bit.TBPHS = 0;     // Phas
    EPwm3Regs.TBPHS.all = 0;
329
    //Action Qualifier configuration
331 EPwm3Regs.AQCTLA.bit.CAU=1;
    EPwm3Regs.AQCTLA.bit.CAD=2;
333 EPwm3Regs.AQCTLB.bit.CBU=2;
    EPwm3Regs.AQCTLB.bit.CBD=1;
335
    // Counter Compare block configuration:
337 EPwm3Regs.CMPA.half.CMPA  = D*tbprd; //0x03E8; //(int)tbprd_d;
    //EPwm3Regs.CMPB  = D*tbprd; //tbprd - tbprd_d; //0x03E8; //(int)((1-D
        ) * tbprd);
339
    // Dead Band block configuration:
341 EPwm3Regs.DBCTL.bit.HALFCYCLE = 0; //0: Full cycle clocking enabled.
        The dead-band counters are clocked at the TBCLK rate.
    //EPwm3Regs.DBCTL.bit.DEDB_MODE = 0; //Rising edge delay and falling
        edge delay applied to source
343                                       //selected by S4 switch (INMODE
                                              bits) and output to B signal
                                              path
                                          //only. Note: When this bit is set
                                               to 1, user should always
                                              either set
```

```
345                                         //OUT_MODE bits such that Apath =
                                                InA OR OUTSWAP bits such
                                            //that OutA=Bpath
347     EPwm3Regs.DBCTL.bit.OUT_MODE = 3; //11: DBM is fully enabled (i.e.
            both RED and FED active)
        EPwm3Regs.DBCTL.bit.POLSEL = 2; //10: Active high complementary (AHC).
             EPWMxB is inverted.
349     EPwm3Regs.DBCTL.bit.IN_MODE= 0; // 00: EPWMxA In (from the action-
            qualifier) is the source for both
                                        //rising-edge delay and falling-edge
                                            delayed signal.
351     EPwm3Regs.DBRED = 10; // 200*1/foc
        EPwm3Regs.DBFED = 10;
353
        EPwm3Regs.ETSEL.bit.SOCAEN  = 0;     // Disable SOC on A group
355     EPwm3Regs.ETSEL.bit.INTEN = 1;       //Enable ePWM Interrupt (EPWMx_INT
            ) Generation
                                                //1: Enable EPWMx_INT
                                                    generation
357
                                                 //This selects which of
                                                     the possible events
                                                     will trigger an
                                                     interrupt or start an
                                                     ADC conversion.
359     EPwm3Regs.ETSEL.bit.SOCASEL = 2;            //010: Enable event time-
            base counter equal to period (TBCTR =
                                                     //TBPRD)
361
        EPwm3Regs.ETSEL.bit.INTSEL = 1;             //001: Enable event time-
            base counter equal to zero. (TBCTR = 0x00)
363
        EPwm3Regs.ETPS.bit.INTPRD = 1;              // Generate INT on 1st
```

```
        event
365
    EPwm3Regs.ETSEL.bit.SOCAEN = 1;                 // Enable SOCA
367 EPwm3Regs.ETPS.bit.SOCAPRD = 1;                 // Generate pulse on 1st
        event*/

369 // Setup shadow register load on ZERO
    EPwm3Regs.CMPCTL.bit.SHDWAMODE = 0;
371 EPwm3Regs.CMPCTL.bit.SHDWBMODE = 0;
    EPwm3Regs.CMPCTL.bit.LOADAMODE = 0;
373 EPwm3Regs.CMPCTL.bit.LOADBMODE = 0;

375 EDIS;
}
377
void SetupIntTimer(void)
379 {

381 DINT; // Step 1: Disable interrupts globally (DINT or SETC INTM).

383 //InitPieCtrl();
    IER = 0x0000;
385 IFR = 0x0000;
    InitPieVectTable();
387
    EALLOW;
389 PieVectTable.TINT1 = &epwm1_timer_isr;  // Redirect function to
        interruption
    EDIS;
391
    InitCpuTimers();
393
    ConfigCpuTimer(&CpuTimer1, 90, Ts);   // Configure cpu timer0 with 90
```

```
        MHz and 50us
395
    CpuTimer1Regs.TCR.all = 0x4001;
397
    IER |= M_INT13;                                  // Enable lines of interrupt
399


401 }

403 void update_compare(void)
    {
405     generatedModel.p_extIn->ila=AdcResult.ADCRESULT0;
        generatedModel.p_extIn->ilb=AdcResult.ADCRESULT1;
407     generatedModel.p_extIn->ilc=AdcResult.ADCRESULT2;
        generatedModel.p_extIn->ila2=AdcResult.ADCRESULT3;
409     generatedModel.p_extIn->ilb2=AdcResult.ADCRESULT4;
        generatedModel.p_extIn->ilc2=AdcResult.ADCRESULT5;
411     generatedModel.p_extIn->vra=AdcResult.ADCRESULT6;
        generatedModel.p_extIn->vrb=AdcResult.ADCRESULT7;
413     generatedModel.p_extIn->vrc=AdcResult.ADCRESULT8;
        generatedModel.p_extIn->vsa=AdcResult.ADCRESULT9;
415     generatedModel.p_extIn->vsb=AdcResult.ADCRESULT10;
        generatedModel.p_extIn->vsc=AdcResult.ADCRESULT11;
417     //Using Typhoon HIL Schematic Editor generated function
        pmsm_speed_ctrl_step(&generatedModel);
419
        // Using Enable variable tu run the inverter
421     if (Enable == 1)
        {
423         // Using Va_ref, Vb_ref, Vc_ref modulation signals
            ma = generatedModel.p_extOut->va;
425         mb = generatedModel.p_extOut->vb;
            mc = generatedModel.p_extOut->vc;
```

```
427
        EALLOW;
429     // scaling duty cycle for the TI comparator block
        EPwm1Regs.CMPA.half.CMPA  = ma*tbprd/2 + tbprd/2;
431     EPwm2Regs.CMPA.half.CMPA  = mb*tbprd/2 + tbprd/2;
        EPwm3Regs.CMPA.half.CMPA  = mc*tbprd/2 + tbprd/2;
433   EDIS;
    }
435 else
    {
437     ma = 0;
        mb = 0;
439     mc = 0;
        ma1 = 0;
441     mb1 = 0;
        mc1 = 0;
443     EALLOW;
        EPwm1Regs.CMPA.half.CMPA = ma;
445     EPwm2Regs.CMPA.half.CMPA = mb;
        EPwm3Regs.CMPA.half.CMPA = mc;
447     EDIS;
        pmsm_speed_ctrl_init(&generatedModel);
449 }

451 }

453 // ISR
interrupt void epwm1_timer_isr(void)
455 {
    update_compare();
457
    //EALLOW;
459 //EPwm1Regs.ETCLR.bit.INT = 1; // EPWM acknoladge of the interupt
```

```
    //PieCtrlRegs.PIEACK.all = PIEACK_GROUP3; // EPWM acknoladge of the
        interupt
461 //EDIS;
}
```

Myfile