Advanced characterisation of novel III-nitride semiconductor based photonics and electronics on polar and non-polar substrates

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Abstract

Advanced characterisation has been carried out on a number of novel III-nitride based photonics and electronics, including micro-LED arrays achieved by a direct epitaxy approach, high performance c-plane HEMTs structure achieved by a novel growth method and non-polar GaN/AlGaN HEMTs. In this work, a systematic study has been conducted to understand the electrical properties of these novel devices, demonstrating their excellent properties. Furthermore, the electrical properties are directly related to epitaxial growth, which provides useful information for further improving device performance, such as 2D growth mode for GaN on a large lattice-mismatched substrate which plays an important in obtaining high breakdown and minimised leakage current for HEMTs.

Micro-LEDs are the key elements for a microdisplay system, where electrical properties are extremely important. Potentially, any leakage current can trigger to turn on any neighbouring microLEDs which are supposed to be off. Instead of using conventional fabrication methods which normally enhances leakage current, our team developed a direct epitaxy approach to achieving microLED arrays. In this work, detailed I-V characteristic and capacitance measurements have been conducted on these novel microLED devices, demonstrating leakage currents as low as 14.1 nA per LED and a smooth negative capacitance curve instead of odd positive capacitance performances. Furthermore, a comparison study between our microLEDs and the microLEDs prepared using the conventional method indicates our device shows a large reduction of size-dependent inefficiency while such a behaviour is never observed on the microLEDs fabricated by the conventional methods.

Unlike the classic two-step method for GaN growth on large lattice-matched sapphire, our team developed a high-temperature AlN buffer technology, where a 2D growth mode, instead of an initial 2D and then 3D growth mode that typically happens for the growth of conventional GaN growth, takes place through the whole growth process. This method allows us to achieve a breakdown electric field strength of 2.5 MV/cm, a leakage current of as low as 41.7 pA at 20 V and saturation current densities as high as 1.1 A/mm. In this work a systematic study has conducted in order to establish a relationship between the excellent device performance and material properties, where a very low screw dislocation density plays a critical role, while our 2D growth method can provide an excellent opportunity for achieving such a low screw dislocation density. This demonstrates the major advantage over the classic two-step method in the growth of power and RF devices. In our case, we have obtained an unintentional doping as low as 2×10^{14} cm^{-3} and screw dislocation densities of 2.3×10^{7} cm^{-2}.

Compared with c-plane GaN based HEMTs due to its intrinsic polarisation, non-polar GaN/AlGaN HEMTs on r-plane sapphire yields potential advantages in terms of the fabrication of normal-off devices which are particularly important for practical applications. However, it is a great challenge to achieve high quality non-polar GaN on sapphire. Some initial work has been conducted, where the detailed characterisation indicates an electron mobility of 43 cm^2 V^{-1} s^{-1} has been initially obtained. Furthermore, instead of using an AlGaN/GaN heterostructure with a modulation doping, we deliberately use a quantum well structure as an electron channel, leading to a mobility of 76 cm^2 V^{-1} s^{-1}. Our simulations as well as measurements also provide a guideline for optimising the general epitaxial structure.

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Publication list

Journal

1. **V. Esendag**, P. Feng, C. Zhu, R. Ni, J. Bai, T. Wang,
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   “Investigation of Electrical Properties of InGaN-Based Micro-Light-Emitting Diode Arrays Achieved by Direct Epitaxy”,
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3. Y. Tian, P. Feng, C. Zhu, X. Chen, C. Xu, **V. Esendag**, G. M. de Arriba, T. Wang,
   “Nearly Lattice-Matched GaN Distributed Bragg Reflectors with Enhanced Performance”,
   Materials 15, 3536 (2022).
4. S. Jiang, Y. Cai, P. Feng, S. Shen, X. Zhao, P. Fletcher, **V. Esendag**, K.-B. Lee, T. Wang,
   “Exploring an Approach toward the Intrinsic Limits of GaN Electronics”,
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   “Strain Analysis of GaN HEMTs on (111) Silicon with Two Transitional AlxGa1-xN Layers”,
   Materials 11, 1968 (2018).
6. Y. Cai, Y. Gong, J. Bai, X. Yu, C. Zhu, **V. Esendag**, K. B. Lee, T. Wang,
   Controllable Uniform Green Light Emitters Enabled by Circular HEMT-LED Devices”,
   IEEE Photonics Journal 10, 4900607 (2018).

Glossary of Nomenclature/Acronyms/Chemical Symbols Used

ω – Omega angle; angle of pitch for the sample plate in an XRD setup with respect to incident beam.

θ – *XRD Context:* Theta angle; angle between diffracted beam and crystal lattice plane for an XRD setup for ω-2θ material composition sweeps, such as Al percentages.

Impedance Analysis Context: It may also be used for the phase angle – trigonometry of the reactive and active components of a circuit or device.

ϕ – *XRD:* Azimuth angle with respect to sample yaw. *Solid State Physics:* Work function.

A – *Characterisation:* shorthand for Amps (unit of current); *Device Geometry:* device active area.

Å – Ångström; named after A. J. Ångström, is a unit of length that is a tenth of a nanometre. The exchange multiplier was set using the wavelength of krypton photon emission. [1]

Al – Aluminium (Sym), Group III Metal.

$Al_xGa_{1-x}N$/'AlGaN' – Aluminium (x) Gallium (1-x) Nitride*, III-V semiconductor.

AlN – Aluminium Nitride, III-V semiconductor.

Al_2O_3 – Aluminium Oxide (a.k.a. 'sapphire')

a-plane – (11-20) plane of a Wurtzite cell

As – Arsenic (Sym), Group V metalloid.

Au – Gold (Sym), Transition Metal.

B – Boron (Sym), Group III metalloid.

C – Carbon (Sym)**,** Group IV non-metal.

CF_6 – Carbon hexafluoride

CHF_3 – Trifluoromethane, fluorocarbon compound.

Cl – Chlorine (Sym), Group VII Halogen.

c-plane – (0001) plane of a Wurtzite cell

Cu – Copper (Sym), Transition Metal.

DBR – Distributed Bragg Reflector

EBL – Electron Beam Lithography

EM – Electromagnetic [spectrum]; biaxial transverse waves covering radio to gamma waves.

EQE – External Quantum Efficiency

F – Fluorine (Sym), Group VII Halogen.

Fe – Iron (Sym), Transition Metal.

Ga – Gallium (Sym), Group III Metal.

GaAs – Gallium Arsenide, III-V semiconductor.

GaAsP – Gallium Arsenide (1-x) Phosphide (x)*, III-V semiconductor.

GaN – Gallium Nitride, III-V semiconductor.

Gbps – Gigabits per second, a transfer rate of a billion (10^9) bits – binary unitary data packets.

H – Hydrogen (Sym), Group I non-metal.

H_2 – Hydrogen (gas, diatomic elemental form)

H_2SO_4 – Sulphuric Acid

HEMT – High Electron Mobility Transistor

I – *Characterisation:* Current [Amp/Ampère]; *Chemistry:* Group I (Alkali metal) Element

ICP(-RIE) – **I**nductively **C**oupled **P**lasma (-enhanced **R**eactive **I**on **E**tching). **

III – Group 3/III Metal/Metalloid Element

III-N – Group III-Nitride Semiconductor

III-V – Group III and Group V compound semiconductor shorthand.

In – Indium (Sym), Group III Metal.

$In_xGa_{1-x}N$/'InGaN' – Indium (x) Gallium (1-x) Nitride*, III-V semiconductor.

InN – Indium Nitride, III-V semiconductor.

IR – Infrared [EM emission].

K – Potassium (Sym), Group I Alkali Metal.

KOH – Potassium Hydroxide

MESFET – Metal-Semiconductor Field Effect Transistor

MIS – Metal-Insulator-Semiconductor (Transistor)

(µ)LED – (Micro) Light Emitting Diode

MOCVD – Metalorganic Chemical Vapour Deposition***

MOVPE – Metalorganic Vapour Phase Epitaxy***

MQW – Multi-Quantum Well

N – Nitrogen (Sym), Group V non-metal.

N_2 – Nitrogen (gas, natural elemental form)

n-doping – A type of 'negative' doping that introduces additional electrons.

NH_3 – Ammonia

Ni – Nickel (Sym), Transition Metal.

O – Oxygen (Sym), Group VI non-metal.

O_2 – Oxygen (gas, natural elemental form)

P – Phosphorus (Sym), Group V non-metal.

p-doping – A type of 'positive' doping that introduces additional holes.

QCSE – Quantum Confined Stark Effect

R – Resistance [Ohm]

RIE – Reactive Ion Etching

r-plane – (10-12) plane of a Wurtzite cell

S – Sulphur (Sym), Group VI non-metal.

SF_6 – Sulphur hexafluoride, fluorosulphide.

SO_4 – Sulphate

sccm – Standard Cubic Centimetre per Minute

SEM – Scanning Electron Microscopy

Si – Silicon (Sym), Group IV metalloid, semiconductor.

SiC – Silicon Carbide, Group IV-IV semi-metal compound, semiconductor.

SiH_4 – Silane, silicon-based para-organic compound with one silicon atom.

Si_2H_6 – Disilane, silicon-based para-organic compound with two silicon atoms.

Ti – Titanium (Sym), Transition Metal.

TMA – Trimethylaluminium ($Al(CH_3)_3$), Group III metalorganic compound.

TMG – Trimethylgallium ($Ga(CH_3)_3$), Group III metalorganic compound.

TMI – Trimethylindium ($In(CH_3)_3$), Group III metalorganic compound.

u-doping – Unintentional Doping

V – Voltage [volts]

XRD – X-ray Diffractometry

Y – Admittance [1/Ohm]

Z – Impedance [Ohm]

ZB – Zinc Blende

Zn – Zinc (Sym), Transition Metal

***Ternary (three-element) semiconductor alloy.

****** ICP and ICP-RIE are used interchangeably.

******* Often interchangeably used with MOCVD; the only difference is that MOVPE specifies atomic layer-by-layer growth.

Sym Elemental symbol.

1 Oxford English Dictionary, Second Edition (1989), *Ångström (unit)* [Online]. Available: https://www.oed.com/oed2/00008552 (accessed 13 Jun 2022)

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Chapter 1 - Introduction

1.1: Introduction

III-Nitride semiconductors are, as a material set held in high regard in solid-state physics, and especially for their role in solid-state lighting [1] and high-power applications, incrementally being adopted by both commercial research and development teams as well as academic institutions due to the material set lending itself well to both illumination and traditional on-chip power and digital electronics purposes. Their flexibility in this regard is mainly thanks to their physiochemical sturdiness (GaN has a Young's Modulus of up to ≈ 295 GPa on nanoscale bowing and is chemically stable on account of its resistance to corrosion, high bond energies and is also thermally stable well into the 1300°C range under the right substrate off-cut conditions [2-4]) on top of their excellent electronic characteristics. Included in these are their sizeable – and fine tuneable via formation of ternary alloys – direct bandgaps (3.4 eV for GaN, 6.2 eV for AlN and ≈ 0.7 eV for InN [5, 6]); high electron saturation velocity of ≈ 2.5×10^{7} ms^{-1}; high intrinsic breakdown electric fields equal to or above 3 MV/cm and respectable intrinsic electron mobility disputed to be between 900 – 1250 $cm^{2}V^{-1}s^{-1}$ for GaN [7-9] . As direct bandgap semiconductors, they are all suitable for electromagnetic radiation from mid-UV to near-mid infrared; while the electron mobility further enhanced by III-N alloys being used as a barrier material to a GaN channel allow for higher mobility than the intrinsic limits of silicon [10-12].

As such, their cases in utilisation for advances in electronics, their potential roles, how they may relate to approaching appliance/device crises and a brief history of how they have been employed in devices in the past shall be explored.

1.1.1: Motivation for Research: State of Industrial/Research Electronics and Where III-Nitrides fit in the State of the Art

The established and/or recently growing industrial applications such as System-on-a-Chip (SoC), with the electronics application's enduring pursuit for low-leakage, low-loss-through-switching, high-performance processing units, Internet of Things (IoT), which necessitates reliable communications and energy efficiency and has potential in healthcare systems among all, the nascent Li-Fi, 5G (which is relatively newly-rolled out, conceived of in mid-2010s and is still being developed in the direction of the technology's defined intrinsic limits), future iterations of mobile networks, such as 6G being in an early developmental phase, and nanoscale hyper-fast data processing technologies set to be using on chip and chip-to-chip communications which features other III-V semiconductors already in an experimental phase [13-17], advanced augmented and virtual reality (AR/VR) which demands sub-5 µm pixel-level precision, colour depth, and high efficiency [18], as

well as longstanding pursuits in reduction of device feature sizes (i.e.: electronic scalability) where while fabrication gets increasingly advanced, a few roadblocks to the success of sub-7 nm node manufacturing include the switching losses impeding high frequency operation, driving current density, quantum tunnelling, and silicon manufacturing crunch (not necessarily due to a global lack of material availability), imploring research into other semiconductors (in tandem with high-k insulators) [19-21] , advanced solar cells and other photovoltaic devices that operate well and with good external quantum efficiency (EQE) owing to III-Nitrides' high toughness, direct bandgaps and nearly solar light spectrum-wide absorption capability, especially thanks to high-In InGaN ternary alloys and multi-quantum wells (MQW), but material logistics and present-day performance limitations means that the potential of the theoretical excellent conversion efficiency has still some way to be achieved [22], and reliable high power control systems, can benefit greatly from advances in GaN/InGaN/AlGaN electronics and materials science.

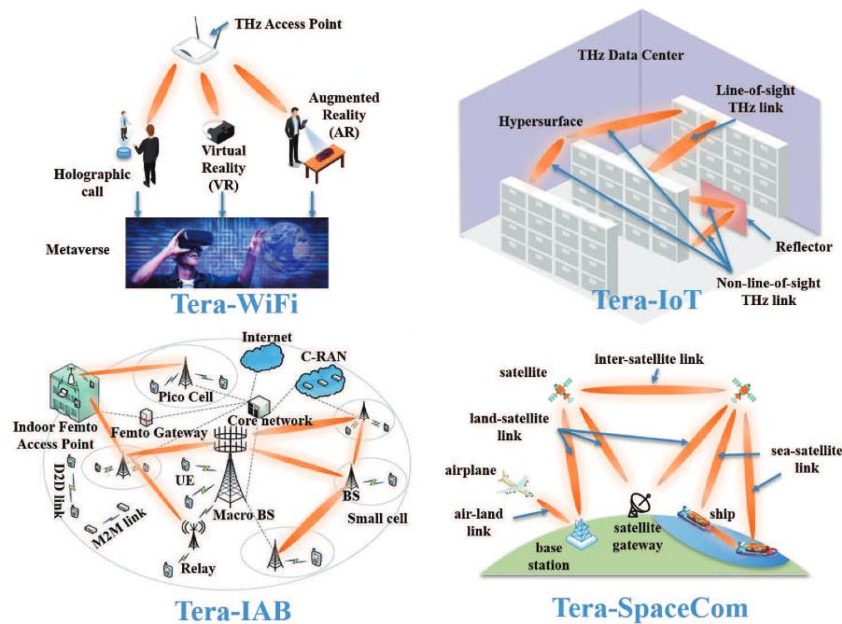

Figure 1.1: 6G Applications to be enabled by THz communications, including a hypothetical Tbps WLAN (Tera-Wi-Fi) system. Credit to I. A. Akyildiz et al. [28] © 2022 IEEE.

It is acknowledged, to address the need for enhanced communications systems, III-Nitride µLEDs or even white phosphorescent broad-area devices with carefully considered modulation schemes have been known to reach higher than 1 Gbps transmission rates, which is ostensibly a good benchmark of late LTE and early 5G technology and thus is compatible for visible light communication (VLC), potentially as an optical fibre substitute or even a whole communications standard in its own right. [23-25] Huawei, an influential organisation in mobile networks and devices, is already undertaking preliminary research into the prototype communications standard of 6G. [26] 6G

is expected to have reached at least its early rollout phase in the next decade. THz communications, covering carrier frequencies from 1/10 terahertz to 10 terahertz, are also being explored for this future milestone, which III-Nitrides are also theoretically capable of as an upper limit thanks to their visible light emission which does fall under THz photon frequencies. [25, 27] GaN, like its arsenide counterpart GaAs (along with AlGaAs, AlGaAsP and InGaAs, also III-V semiconductors) that already sees such research intrigue with quantum cascade lasers (QCL) and purpose-built nanoscale field effect transistors (FET), is promising for the application. [28] Due to the qualities of III-Nitride semiconductors that make them attractive for addressing these ambitions, it is evident that research into the material group is a serious endeavour.

Li-Fi, or Light Fidelity, in particular has been hailed as an excellent candidate for solutions to data communications bottlenecks that are expected to be experienced by users of computing technologies, mobile or otherwise, and gives III-Nitride transmitter/receivers a niche in experimental communications. A 3.4 Gbit wireless transmission system based on Cree Semiconductors-made RGB LEDs – a triple combination of red, green and blue LEDs used to cast visible white light for VLC – utilising InGaN on SiC substrates, incorporated into communications keying was reported back in 2012, and its sapphire/GaN/InGaN systems equivalent to this also reach the several-Gbps goal, with 9 Gbps being the record, and another scheme reported Gbps performance over distances longer than 3 m, meaning it may become a feasible communications standard in the near future. Indoor illumination is also thought to be a secondary benefit to get out of VLC, which is important for energy efficiency. It is hoped that III-N systems also attain 10s of Gbps in the near future. [24, 29-32]

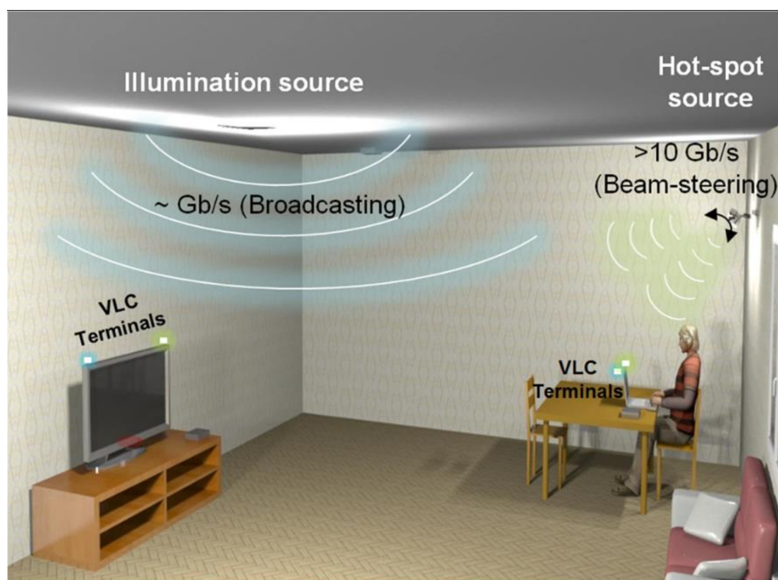

Figure 1.2: A vision of how Li-Fi could operate. Credit to H. Chun et al [32], © 2019.

Above all as a matter of curiosity towards III-N semiconductors, however, is the III-Nitrides' potential for power electronics applications, thanks to the material family's innate excellent balance between breakdown fields, and electron mobility, meaning should their shortcomings be addressed, a versatile power electronics and optoelectronics platform will be centrepiece to the electronics industry, which already shows interest in them. GaN-based transistors on sapphire allow for 1.1 A/mm current density under 1 V gate bias and 10 V drain-source voltage with purely built-in electric fields from the crystal orientation, also known as [electrical] polarisation, and up to 1.4 A/mm with intentional doping on SiC, whilst sub-nA/mm leakages are also observable [33-35]. GaN/AlGaN heterojunctional transistor structures on sapphire have also been known to achieve breakdown electric fields up to 2.5 MV/cm [35], close to the material's intrinsic limit. Low on-resistances have also been reached and specialist complex-doped GaN/InAlGaN HEMTs on SiC attain 2 A/mm current density, 680 mS/mm extrinsic transconductance, 217 Ω/sq sheet resistance and 0.4 Ω/mm on-resistance[36]. High breakdown, high frequency structures are naturally a source of intrigue, with one such example reaching 202 GHz f_{max}, 1800 $cm^2V^{-1}s^{-1}$ electron mobility and > 1 MV/cm breakdown on SiC [37], and GaN/AlGaN/AlN HEMTs have been obtained with maximum operational frequencies of 300 GHz on SiC again, and 6 GHz on Si substrate MIS-HEMTs [38, 39]. GaN electron mobility and saturation velocity mean that there is still even more room for higher frequency applications still, and while it already sees RF and microwave operation, pushing the material to bridge the 'THz gap' will be important.

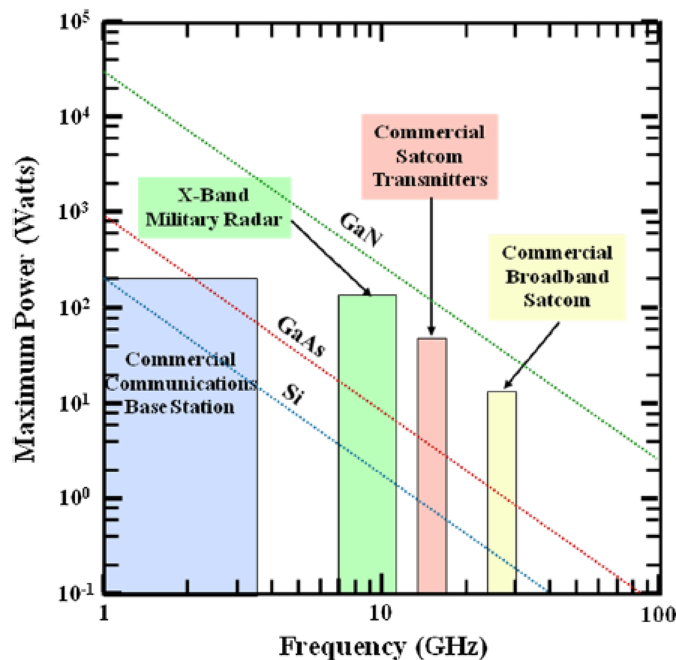

Figure 1.3: Power-frequency relationship of Si, GaAs and GaN, as a comparison correct to 2015. Credit to Jones et al [40], © 2015, Springer.

This power electronics/optoelectronics duality has profound implications for III-Nitrides' applications into industry, especially the aforementioned SoCs. To name a few influential companies in the field with their developments and interest in GaN in the last 4 years, ARM has had ambitions to expand their 'fabless' semiconductor IP into more laptops and similar computing devices, moving into 7 and even 5 nm manufacturing, Thermal Design Power (TDP) ratings of 5 W and 3.3 GHz operational frequency [41]; Qualcomm seeks delivery of 5G mmWave and sub-6 GHz integrated modem-RF systems [42], and NXP, an SoC producer, a notable supplier to OEMs (Original Equipment Manufacturer) and an electronic material development company previously working quite Si-centrically, is making the shift into GaN with its new Arizona plant, and more potentially planned, for the same power-and-communications purpose. [43]

GaN has some other fundamental advantages over silicon. It can be considered to be 'greener' than Si owing to its higher 'figure of merit' that enables high frequency, low loss operation, in addition to the potential to be grown for a lesser carbon footprint as industry grows, as Ga may be found as a by-product of Al smelting from bauxite ore, and has been reviewed experimentally for H_2 fuel systems, as the III-N material family also has a potential niche in transport and aerospace engineering thanks to their relative tolerance to harsh environments. [10, 44] The comparison to silicon in terms of electron mobility also gives them a potential role in integrated circuitry, since the response time is largely dictated by the aforementioned electronic quality and the majority of silicon commercially employed does not consist of bulk ('monocrystalline') but rather polycrystalline silicon ('poly-Si') which, depending on grain size, suffers from a large electron and hole mobility drop compared to its intrinsic capabilities by an order of magnitude [45]; poly-silicon also doubly gets affected by impurity scattering from dopants used in the main channel, since silicon-only transistors are homojunctional and their channels are determined by contrast in doping. [46]

In terms of current logistical fabrication/growth developments, of particular interest is their suitability for integrated circuits using both optoelectronics and power devices as a single piece, i.e.: monolithic integration with no need of interconnects [47-49]; potential for being retrofitted, in a sense, through epitaxial overgrowth, onto existing silicon-based wafers, with one such vertically-integrated example being used for default-off operation [50] as CMOS technology and other silicon applications are still dominant within the electronics industry even with the recent supply issues. Recently, our Group has also reported integrated HEMT-µLEDs suitable for high-frequency systems. [51]

Rather than necessarily with a main motivation of one-dimensional problem-solving then, it is prudent to undertake research with multiple device-level endeavours in mind, as these materials of curiosity may help address many of the challenges of electronic engineering.

1.1.2: AlN, InN and GaN's Debut into Materials Science

AlN was the first of the material family to be discovered in 1862 and synthesised in 1907, as the solubility and nitridation of the metal drew some intrigue [52, 53], but it would take another century before its potential for electronic devices was realised thanks to a reported thermal conductivity of 285 W m^{-1} K^{-1}, as the material's potential as both a ceramic and a wide-bandgap emitter was realised [54]. Many catalyst materials were experimented upon and employed for synthesis since, and the thermal-chemical stability of both the material itself and aluminium oxide, Al_2O_3, have been the subject of intrigue. [52]

InN was the second material of the collection to have been reported on, around 1910, and throughout the following decades, the discovery of the narrow bandgap and potential for very high electron mobility of InN ensued. While the material's perceived role in photovoltaics and solar panels was based on the outdated bandgap value of between 1.7 and 1.9 eV, it still holds true with its currently accepted value of 0.65 eV, and high-In InGaN alloys are consequently still of high importance. [55]

GaN, the last discovered one of the three III-N semiconductors, was first grown in 1931 by W. C. Johnson et al, who led a research using existing literature at the time of the existence of nitrides of each member of group III elements, except gallium. This led to the confirmation of the existence of GaN as a compound through fusion of metallic gallium from fractionally crystallised 'germanite ore' and dried liquid ammonia [56, 57]; almost a century later, purified ammonia is still one of the crucial ingredients to grow III-Nitride semiconductors to this day. However, this early attempt yielded amorphous GaN, and it was not until 1969 that monocrystalline GaN was obtained using hydride vapour phase epitaxy (HVPE) and even its bandgap was able to be reported, as 3.39 eV. [58]

Early HVPE-grown films yielded what was then perceived, with limited spectroscopy and gauging of impurities, as high concentrations of N^{3-} vacancies and resultant strong n-type conduction of around 10^{19} cm^{-3}, though (as well as a relative tendency for dissociation at temperatures well below 600°C). The former was first unsuccessfully attempted to be alleviated with acceptors, which resulted in high resistivity films [58, 59]. (The present-day accepted reason for this strong n-type conduction, however, is actually Ga^{3+} vacancies, which reinforces the narrative of introducing extra free electrons into the bulk semiconductor [33, 60]). The introduction of MOCVD, the current standard growth method, to GaN growth in 1971 [61] transformed GaN to be well-placed to become an emitting material of high renown [56]. The subsequent production of the first high-quality films via MBE in 1983 [62], a re-adaptation to MOCVD in 1985, using a low-temperature AlN buffer [63] and the currently-

accepted two-step growth in 1991 [64] provided a pipeline for progressively higher quality GaN and facilitated the material's modern optoelectronics applications.

1.1.3: A Brief History of High Electron Mobility Transistors (HEMT)

These heterojunctional transistors, as opposed to standard field effect transistors which use differently-doped regions and/or an insulator layer to create a channel layer, first came into existence in the III-arsenide material system as a concept by Takashi Mimura, who coined the term High Electron Mobility Transistor to describe one such device. Originally as a scheme to demonstrate that AlGaAs/GaAs transistors are supposed to demonstrate superior high-speed operation and depletion/accumulation n-type characteristics to Si FETs, such as MESFETs which already demonstrate respectable > 45 GHz cut-off performance [65], the HEMT concept has been adopted since and remains a crucial part of III-Nitride and derivative materials science.

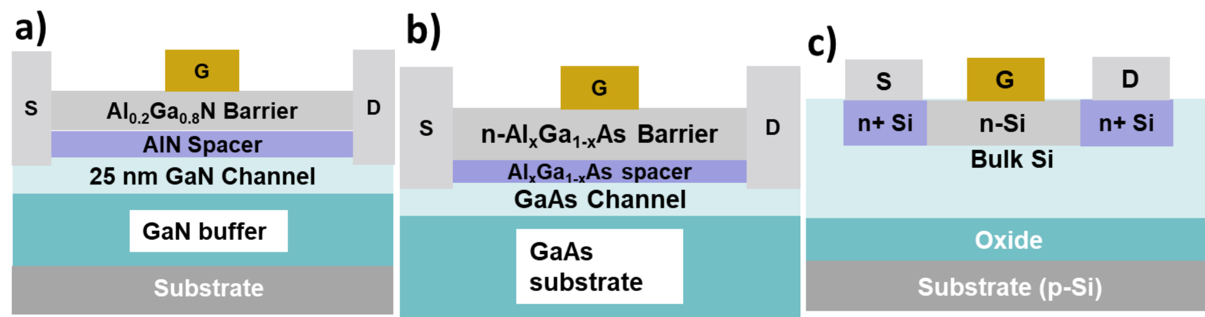

Figure 1.4: The cross-section of **a)** an AlGaN/GaN unintentionally-doped polar (natural internal electric field) HEMT device; **b)** AlGaAs/GaAs n-doped barrier HEMT and **c)** a Si-on-insulator MESFET [65] for comparison.

He theorised that, electrons need to be induced into a completely undoped layer, through careful superlattice engineering of a modulation doping scheme and thickness adjustment of a barrier layer, in order to take advantage of this channel layer's lack of alloy disorder, carrier-to-carrier and ionised impurity scattering. Such a modulation doping scheme, is one whereby the spatial separation of doping impurities and charges is achieved by the aforementioned growth of a main channel layer – GaAs – and an n-doped – mixed with impurities that release extra negative charge in the form of electrons (as illustrated in Chapter 2) – barrier of AlGaAs, with a larger bandgap than GaAs, to induce surplus electrons into the GaAs channel, which is at a lower energy than the barrier, which they are inclined to occupy.

The depletion region needs to be thin enough to not shield the field effect but thick enough to be able to take advantage of Fermi pinning for charge accumulation. In semiconductor theory, it is accepted that, in an unbiased equilibrium state, the Fermi Energy – the average statistical energy (Subchapter 2.1.1) of all charge carriers within the material layer, middle of the bandgap for an

intrinsic semiconductor – must be the same energy across every layer, due to continuity of surface and bulk states of charge carriers, hence the pinning. This pinning consequently determines how semiconductor/metal junctions behave in conjunction with metal-semiconductor barriers and inherent electric fields. Consequently, HEMTs require precise, often atomic-layer, vapour deposition to be able to achieve this modulation doping scheme, and scrutiny into their high-frequency performance was undertaken as early as 1987. [66, 67]

Mimura's initial sketch, Figure 1.5, shows an AlGaAs/GaAs HEMT, with the lattice growth being on the x-axis and carrier energy on a band diagram on the y-axis. These are divided into three cases. The first case is a HEMT with an excessively thick barrier; as extra electrons are induced into the channel layer, they leave behind positively-charged donor ions, which form a depletion region; the three charge regimes in this case are the metal surface depletion region, the n-AlGaAs/GaAs interface depletion region and the charge neutral region in the middle which shields the accumulation region from gate electric fields. The result is a device that is on by default (default-ON) and cannot be effectively switched off by changing the transistor gate voltage, or gate modulation. The second case is a HEMT with a medium barrier that creates a depletion region thin and continuous enough to be gate-modulated, but the induced charge density still results in a device that is default-ON. The third case is a thin barrier with no inherent electronic build-up, but can be voltage biased into an increased current, leading to a default-OFF device.

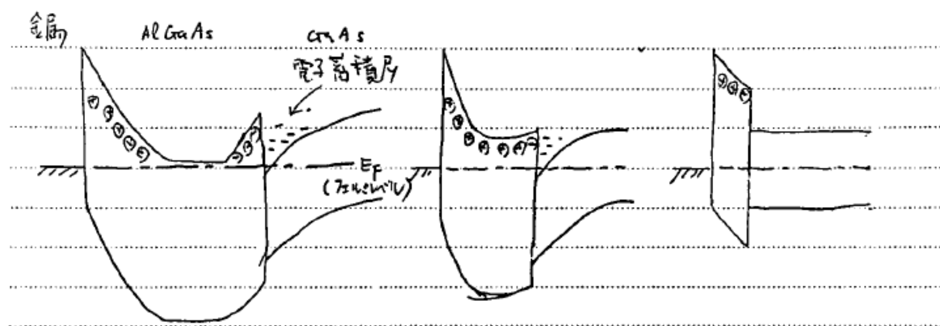

Figure 1.5: The band diagram sketch by Mimura for the HEMT principle demonstrating **a)** excess charge accumulation with a thick barrier; **b)** gate-controllable 2DEG/surface charge relationship with the appropriate thickness; and **c)** no inherent accumulation with a thin barrier [66]. ©2002 IEEE.

Thus, channel electrons are compelled to have the dual advantage of being able to move through a less-obstructed channel and also attain enhanced mobility through a larger potential drop than the material's intrinsic limits allow and a region of confinement which, on top of their additional mobility, also renders them almost completely free to move in two axes and confined

along the growth axis. This electron cloud, moving almost akin to a gas in free space, can be retroactively identified to be referred to in literature as 2DEG; two-dimensional electron gas [66].

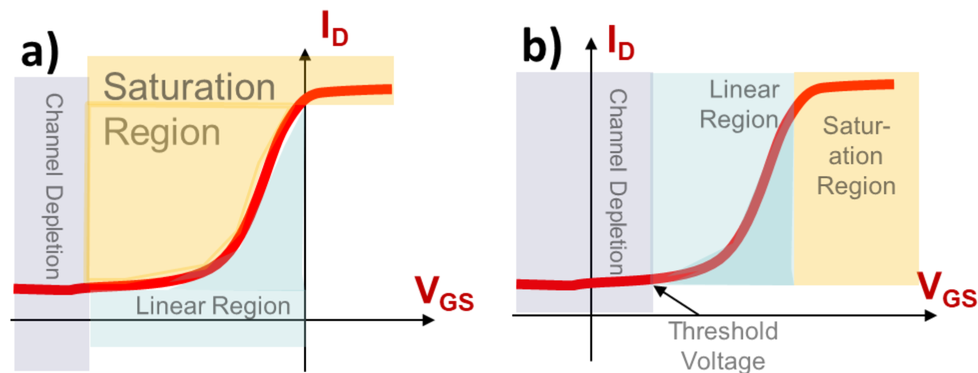

Figure 1.6: A generic illustration of: **a)** Depletion-mode drain current operation by gate voltage; **b)** Enhancement-mode operation.

The first depletion-mode HEMT was demonstrated in 1980 [68], but the principle of the lack of inherent accumulation as in Figure 1.5c was also used to create its enhancement-mode counterparts later the same year. [69] Depletion-mode devices, such as a JFET and the aforementioned HEMT, are on by default and a negative voltage is needed to turn them off; enhancement mode devices like MOSFETs and MOS-HEMTs are off by default and need a positive gate voltage for operation. Integrated logic circuits, exemplified using a 27-stage ring oscillator based on the HEMT technology still in its infancy, were also successfully tested in 1981 [70], although Mimura's group's 'inverted' HEMT structures, which consisted of a Schottky contact on the undoped GaAs overgrown on AlGaAs, initially did not succeed [66]. That task fell upon Delagebeaudeuf et al, who succeeded with the inverted HEMTs in 1980 and also used 2DEG in this context for the first time and filed a patent for this MESFET to mirror Mimura's original HEMT [71]. The prototype for a HEMT satellite communications amplifier was tested in 1983, and this marks the turning point for the long-lasting interest in high-frequency operation for this transistor archetype [72]. Low-noise amplifiers using this HEMT technology eventually made history by helping discover new interstellar molecules in 1986 [73].

A natural consequence of the success of the GaAs/AlGaAs HEMT is that III-Nitrides would also get their own interpretations of the HEMT. As GaN and AlN had become viable semiconductors through improvements in their crystalline growth in the late 1980s, by the early 1990s they were the subject of ire for many researchers, and one of the earliest iterations of an AlGaN HEMT was Khan et al's n-GaN/$Al_{0.14}Ga_{0.86}N$ heterojunction device series, already with characteristics familiar to present-day GaN power electronics engineers such as an -6 V pinch-off point – transistor gate junction voltage that, upon further decrease for a depletion mode and further increase in enhancement,

causes the channel to be tightened and de-sensitised to further drain-source voltage change, depletion-mode operation, and peak/saturation transconductance (then only 28 mS/mm at 300 K) at around a gate bias of between 0 and 1 V [74]. Transconductance, or transfer conductance, is a differential representation of how a change in gate voltage dynamically affects drain current, taking the transistor as a more complex current source, which varies at gate voltage ranges, thus the peak/saturation transconductance is the highest this transistor is able to demonstrate.

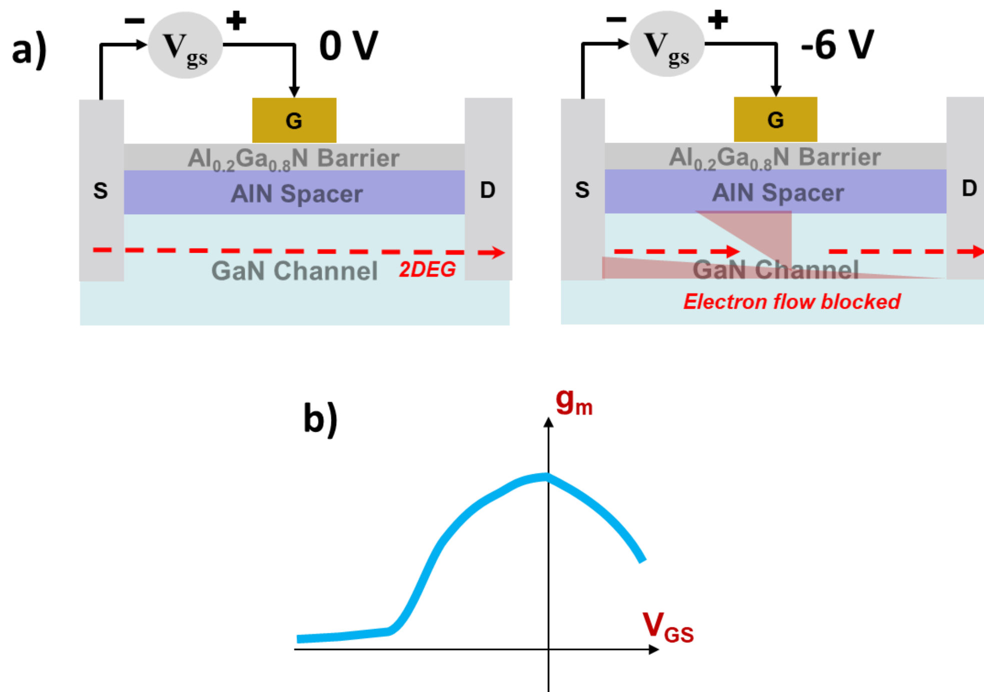

Figure 1.7: a) Conceptual representation of pinch-off in a HEMT; **b)** an example transconductance curve of a HEMT.

The next decade would see various fabrication techniques and devised device architectures to devise alternative architectures or improve upon HEMTs, including the use of FATFET (long-gate FETs) transistors with thin buffers [75] and theoretical modelling of heterojunctional bipolar transistors to be HEMT counterparts to BJT technology [76]. The need for enhancement-mode operation was alleviated by the first GaN/AlGaN MOS-HEMT (Metal-Oxide-Semiconductor HEMT) in 2004 with the ALD (atomic layer deposition) application of an Al_2O_3 gate dielectric and passivation layer, which is convenient as it is chemically and crystallographically identical to sapphire substrates [77]. Fujitsu Laboratories then developed the first application of GaN HEMTs for power supply systems in 2009 and commercial applications of GaN transistors in general have been expanding ever since, with Cambridge GaN Devices and EPC for instance offering their own commercial schemes. [78 – 80]

1.1.4: A Brief History of (Micro)-Light Emitting Diodes

Micro-LEDs are one of the most sought-after areas of research in terms of GaN/InGaN electronics as the optoelectronics scaling on these devices allows for both better chip-level illumination as well as increased maximal driving power density and resolution – the latter is always a focal point of advancing display technology when it comes to smartphones and LED displays, but is also important for augmented and virtual reality (AR/VR) technologies, with especially the former benefitting from unobstructive heads-up displays, thus a high resolution is key.

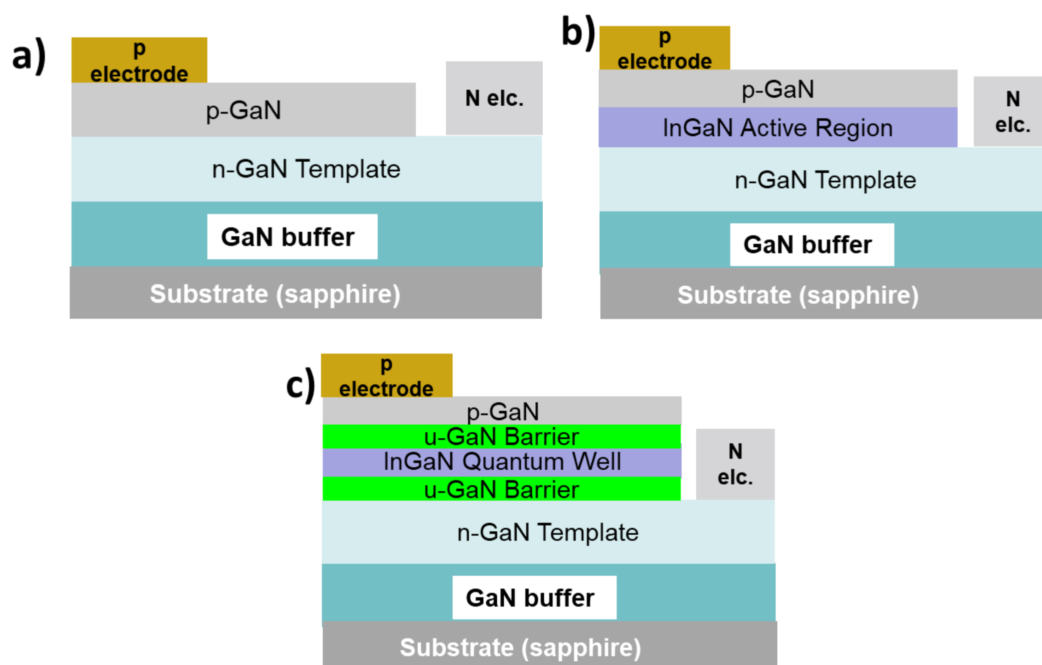

Figure 1.8: Three types of III-Nitride LEDs for representation of concept: **a)** Cross-sectional diagram of a GaN homojunction light-emitting diode based on a simple *pn* junction; **b)** a heterojunction LED with an InGaN emitting region and *pn*-GaN and **c)** A *single quantum well* GaN/InGaN LED.

Arguably, the very first light emitting diode itself, whose acronym is now widely acknowledged as a household name, was first made in 1907 by H. J. Round, who reported uneven emission of yellow, green, and orange, or sometimes blue light from carborundum, nowadays referred to by its chemical symbol SiC, upon application of 10 V between two points of a crystal [56, 81]. This effect, presently called electroluminescence (EL), was correctly re-identified and quantum mechanically backed up by O. V. Losev in 1923 [82].

The first 'true' light-emitting diode however, phasing out SiC in favour of direct bandgap materials, could be said to have been produced around 40 years later between late 1961, when J Biard and G. E. Pittman demonstrated light emission from a near-IR GaAs pn junction (which they patented the next year), and late 1962, when N. Holonyak and S. V. Bevacqua produced coherent

emission based on the GaAsP, another III-V semiconductor alloy, in the red region of the visible EM spectrum [56, 83-85].

The application of their principles soon followed through to III-Nitride device applications, since the crystallographic improvements of the material group enabled their early optoelectronic applications and their optoelectronic success eventually paving the way to their power electronics applications as elaborated in Subchapter 1.1.3. The use of GaN/InGaN heterostructures was a perceived upgrade as the core material did not need to be alloyed or heavily doped with N as with GaAsP in order to produce shorter wavelength visible light and was direct bandgap. In addition, the direct bandgap nature of the latter diminished if the P ratio was greater than 49%. [83, 86, 87]. A tangible effect of the introduction of GaN was also that optoelectronics engineers were no longer limited to SiC for inefficient blue light emission [88].

The first GaN-based LED, with these motivations, was launched in 1971 by Pankove et al [89]. By then, GaN was severely limited by the lack of p-type doping, and it would take another year for Mg to be able to exhibit better performance in that manner and achieve consistent violet emission at 425 nm through the works of Maruska et al [90]. The introduction of MOCVD [61] and later two-step growth [63, 64] improved the material's prospects to compete for LEDs. Even with the initial introduction of Mg, however, p-GaN films were still a major roadblock, as Mg-H complexes during MOCVD growth needed to be addressed with an additional activation step [83]. Amano and Akasaki put this forward in 1989, achieving hole concentrations in the order of 10^{16} cm^{-3} [91], and the first noticeably contrasted-in-doping p-n junction GaN LED was produced by S. Nakamura [92]. He employed a different post-growth annealing method; one which gave hole concentrations an order of magnitude larger than the last scheme, and stayed as a mass-production standard.

Nakamura went on to produce the first double heterostructure electrically injected LED using InGaN/AlGaN alloys [93], and was eventually nominated as a Nobel Prize in Physics Laureate alongside Amano and Akasaki for the trio's invaluable efforts towards LED technology [83, 94]. Scaling down of the GaN/InGaN LEDs from 'broad area' devices to several tens of µm came about in 2000 [95], but a size-dependent inefficiency problem remained, and the next 20 years would be host to many methods including chemical etching and neutral beam etching to alleviate sidewall damages [96, 97], and the *GaN Centre* used overgrowth for green/blue 3.6 µm µLED arrays in 2020 [18]; the same technique was used to produce 2 µm circular red LEDs this year [98].

1.2: Thesis Overview

As per the aforementioned electronics developments of renown and topics of research of great intrigue to academics, a multi-phase set of studies have been undertaken in order to put forward

major improvements in both III-Nitride optoelectronic devices and power electronics components using the material set. The Thesis covers these three main areas of research:

- Fabrication, characterisation, and epitaxial analysis of overgrown micro-LED arrays using a (0001) c-plane n-GaN template and reflecting on the electronic performance improvement per µLED
- Studying the effects of high-temperature, mainly-2D AlN buffer growth on the buffer characteristics of c-plane GaN/AlGaN HEMT epitaxial stacks
- Investigation into improving electron mobility and saturation current in (11-20) a-plane GaN/AlGaN HEMTs on r-plane sapphire through the use of simulation tools and device characterisation.

To be discussed in further detail in Chapter 4, the use of an array template has been deemed necessary in order to enable overgrowth of micro-LED templates in a novel masking process developed by the Group, mainly to eliminate the sidewall damage issue that limits both the electronic efficiency and quantum efficiency of LED devices when scaled down below dimensions that would ostensibly be considered broad-area active zones.

Delivery of the micropatterned layout is achieved through selective photolithography and etching of patterned templates on a 500 nm thick SiO2 layer, which carries with it the double advantage of providing a thickness-matched template for µLEDs to be grown in the pattern holes and introducing automatic sidewall passivation, which then eliminates the need to apply passivation after device overgrowth.

Chapter 5 focusses on the use of the GaN Centre's high-temperature 500 nm AlN buffer technology in order to suppress screw dislocations and unintentional doping with the end goal of improving buffer leakage characteristics. While the technique has already proven to enable improved breakdown electric field characteristics, how the re-adjusted growth relates to these crystallographic problems remained unknown until recently, where it was found that the buffer technique improved crystal quality as well as unintentional doping. Moreover, it agrees with previous works that buffer leakage and unintentional doping mainly arise from screw dislocations and not edge dislocations.

The final part of the thesis dissects the recent improvements in non-polar a-plane GaN (on r-plane sapphire) layer electron mobility, both practically, and through simulation tools. One of the major impediments to employment of non-polar GaN in power device applications is the poor electron mobility and stacking fault-caused scattering of such devices. One way to address the issue

is to either use expensive freestanding substrates, or to use labour-intensive microrod array overlayed with overgrowth on sapphire, but reducing dislocations and biaxial strain on a thin a-plane buffer alone are beneficial.

1.3: Limitations

While III-Nitride semiconductors can be quite powerful for many of the aforementioned electronic applications, it is also important to acknowledge the inherent and accompanied shortcomings of the material set, as well as challenges faced with the growth and fabrication of the specific devices covered.

1.3.1: Lattice mismatch, p-type inactivity, crystallographic challenges

Despite many compelling arguments from a materials science perspective, one of the major pragmatic problems that impede the more widespread adoption of III-Nitride technologies is native substrates being extremely difficult (and therefore prohibitively expensive) to grow due to the material set's taxing thermodynamic equilibrium condition requirement. Most critically, a melting temperature of 2500°C for GaN in fully-grown compound form at atmospheric pressure, and a 4.5 GPa equilibrium pressure for nitrogen to prevent GaN decomposition during growth [60], to be grown in a freestanding manner in the absence of a nucleation structure. In fact, even nominally 'freestanding' GaN substrates are not usually grown in bulk directly, but rather, are off-cut and extracted from a semiconductor wafer, be it optically or void-assisted, grown on a 'foreign' substrate with as little initial lattice mismatch as possible, so even in those some dislocations – in the realms of 10^6 cm^{-2} – remain whether it is due to previous strain or subsequent heat treatment [99, 100]. Ga melt-back is also problematic at temperature/pressure ratings well below this equilibrium, impeding growth and potentially incurring damages. [101, 102] Thus, III-N growth necessitates the use of sizeable vertical lattice parameter-mismatched (≈14% total) sapphire, mildly lattice-mismatched (3.4%) but more expensive SiC and unit cell type/lattice-mismatched Si (17%) substrates for any reasonably practical application, with graphene also being attempted; unfortunately, the crystal quality tends to take an impact as a result [83, 103]. Combined with large thermal expansion coefficient mismatches of 34% and 54% with sapphire and Si respectively, the resultant inter-lattice strain requires diligent strain engineering [104]. This degradation in crystal quality is detrimental to both electrical and optical performance, as it worsens charge carrier free paths.

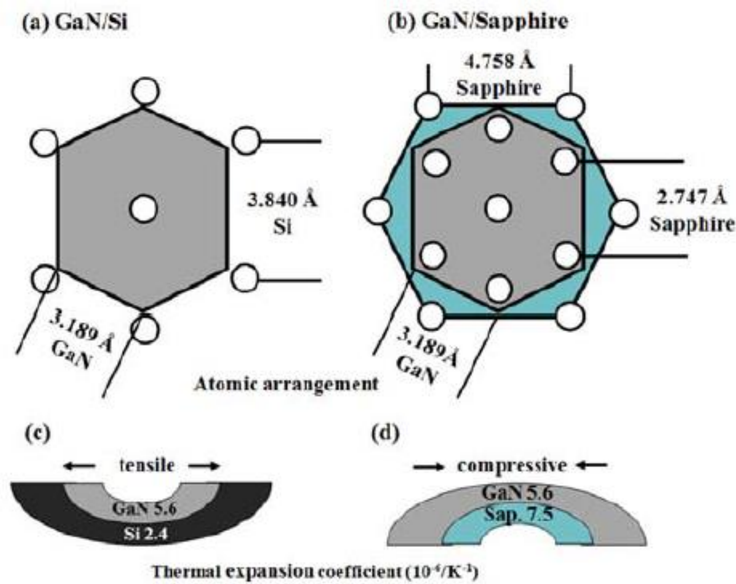

Figure 1.9: Illustration of lattice mismatch and compressive/tensile strains between GaN and Si or sapphire [104]. Credit to H. Shin et al, © 2013 Springer/The Korean Physical Society.

Therefore, growth schemes on permanent 'foreign' substrates for III-N wafers usually focus on limiting dislocation densities to beneath 5×10^{8} cm^{-2} [40] (which is four orders of magnitude larger than what would render most other compound semiconductors optically ineffective and thus it is remarkable that III-Nitrides operate well with these densities) [105], or to simply prevent sample cracking, which is deemed enough of an improvement to keep devices as functional as possible, as tolerable dislocation densities can be compensated for on a device-level. As to be discussed in Chapter 5, low screw dislocation densities are useful for dampening unintentional doping and current leakage path occurrence into the substrate, and edge dislocations are a less-urgent contribution [33]. While GaN and sapphire have a sizeable mismatch as they are, the introduction of an appropriate high-temperature AlN buffer alleviates this somewhat, so most of the resultant 'natural' dislocations when grown 2D like this end up being of an edge dislocation nature [106].

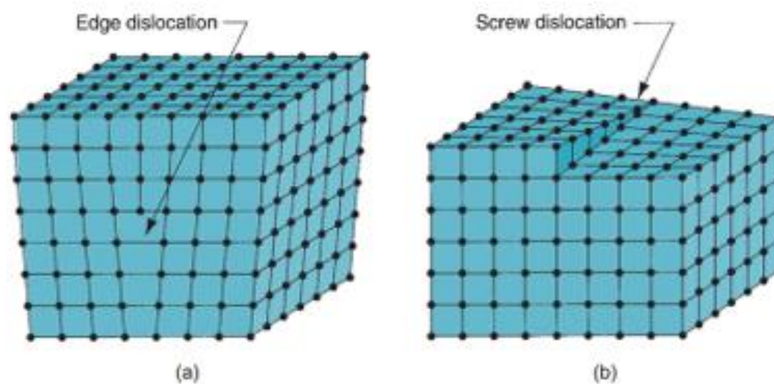

Figure 1.10: Screw and edge dislocations, illustrated [107].

Silicon may have had the potential to be an excellent substrate due to how ubiquitous it is despite the aforementioned large mismatch, and there exist many attempts at making Si-substrate samples, especially with semi-polar and fully polar GaN, comparable to GaN/AlGaN on sapphire, as well as commercial GaN-on-Si wafers. However, it, between Wurtzite GaN and diamond cubic Si, necessitates strain-engineering the growth, for example, multiple staggered AlGaN layers, at a fraction of the saturation current performance it offers on sapphire. GaN may be forced to exist in a metastable Zinc Blende arrangement to mirror the DC arrangement of Si or ZB GaAs, but its performance is subject to finding a good substrate for minimal mismatch for ZB GaN [108]. Therefore, the vast majority of GaN wafers covered in this Thesis are on a sapphire substrate, and the majority of other successful GaN devices use SiC as a substrate.

As well, unintentional n-type doping which worsens an existent default-on operation problem as well as subthreshold leakage and also dampens the material's potential for high breakdown voltage limits is also a sizeable contributing factor in hampering the potential of the material set. As to be seen later, the primary contributing factor to allowing this is the prevalence of screw dislocations, especially of the full-core type [109]. Stacking faults lead the way to Ga^{3+} vacancies, which are substituted in an energetically favourable way by impurities from either the growth chamber or the substrate itself, which is mostly either Si (from a homogeneous Si or heterogeneous SiC substrate) or O (from a sapphire substrate), both of which lead to slight n-type doping [33,60].

The unintentional n-type doping problem is also an impediment to another problem that plagues III-Nitrides; the already-present difficulty in p-type activation. While it is true that p-type layers are achievable thanks to auto C-doping that can be induced [110], and intentional p-type doping examples using Fe and Mg as dopants have been in use for three decades, their performance is still less than ideal for hole concentration. Moreover, p-type activation is problematic for a second reason, and it is that they also suffer from incomplete dopant activation in the first place. As well, as to be mentioned in Subchapter 1.3.3, III-V semiconductors also have an imbalance of electron to hole mobility which renders bipolar transistors suboptimal.

Another crystallographic problem that contributes to usually worse-than-expected performances is related to orthorhombic strain, which arises due to a variety of reasons such as thermal expansion coefficient mismatch and inherent correctional stress between bonded species.

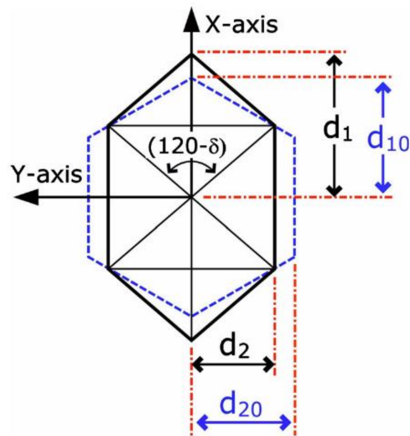

Figure 1.11: Illustration of orthorhombic strain between off-cut r-plane sapphire and a-plane GaN overgrowth, which causes a biaxial strain, and the parameters that need to be obtained through crystallographic characterisation such as XRD. Reprinted from Laskar et al, with the permission of AIP Publishing [111].

Finally, the incorporation of high In and high Al ratios into InGaN and AlGaN alloys also remains a challenge despite recent improvements [101, 112] , which affects the bandgap tuning of the semiconductor family.

1.3.2: (Micro)-LED size-dependent inefficiency, the 'green/yellow gap', light extraction, and other concerns

An issue that plagues especially fully-polar III-Nitride based optoelectronic devices is the efficiency droop in the green region of the visible light spectrum. Polarisation, as to be discussed in Chapter 2 in terms of semiconductor theory, facilitates a wavelength-shift phenomenon based on electron-hole recombination energies in energy states in an InGaN/GaN multi-quantum well (MQW) structure due to the internal electric field it drives. This is commonly referred to as the Quantum Confined Stark Effect (QCSE) [113]. Thus, green and yellow light emitting devices suffer from an efficiency drop. Emissions further into the bands are less-affected by this shift, but for band edges, this creates an inefficiency around this colour range, leading to the (In)GaN 'green gap'. Compounding this factor is the poor incorporation of high In concentrations [101,] for the majority of III-N growth. This is one of the motivations for the Author being interested in improvements in non-polar GaN power devices, as this also eliminates QCSE for integrated power/optoelectronic circuits.

Another issue inherent to scaling LED devices to the several-micrometre sizes, is that traditional fabrication through etching the devices out in an ICP-RIE chamber causes sidewall damage, which causes a size-dependent inefficiency through an effect commonly referred to as Shockley-Read-Hall (SRH) recombination [114]. The causes of ICP sidewall damage are a lot more

complicated; one interpretation is that ICP-enhanced reactive ions either lose directionality at high power ratings or the underpowered ions get embedded into the device sidewalls [115], but usually it requires extra passivation to disable the new trapping sites this damage creates. Even with sidewall passivation, these sites facilitate both a reduction in optical efficiency due to becoming a medium for non-radiative recombination and charge carrier traps which affects leakage.

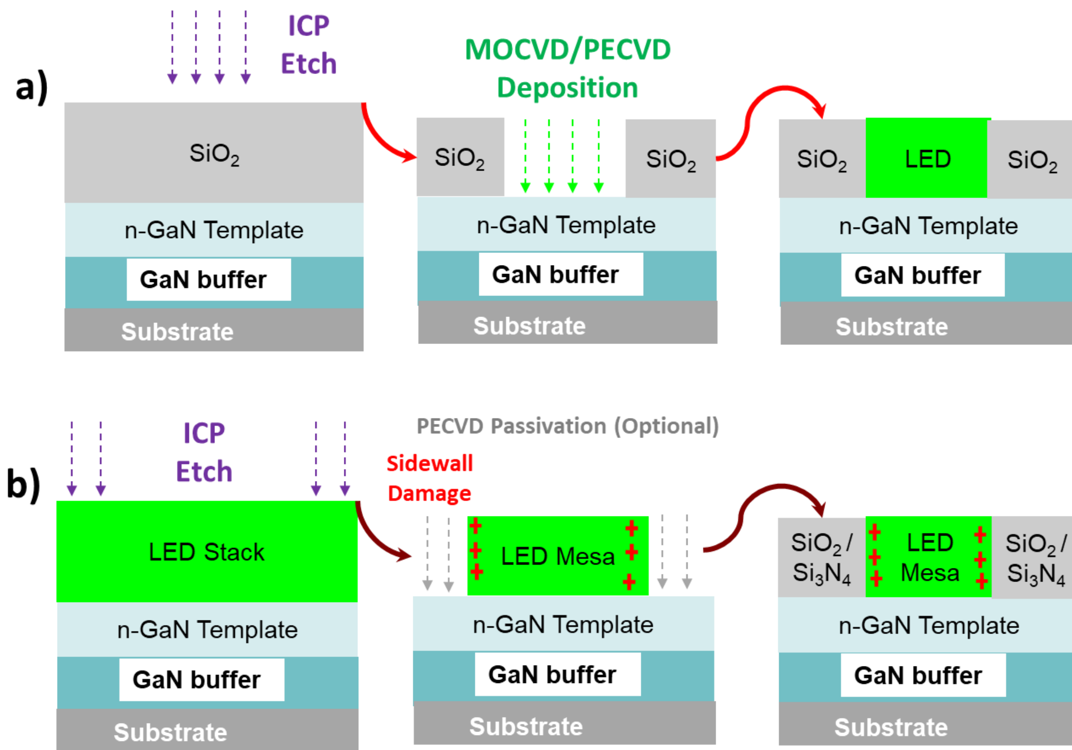

Figure 1.12: Illustration of: **a)** Overgrowth vs. **b)** traditional mesa etching of LED fabrication.

In terms of µLED specific fabrication issues, overgrowth is a promising way to simplify µLED fabrication through not needing a device etching and post-fabrication passivation process, and improve µLED performance beyond what is normally possible through traditional fabrication, but it presents its own fabrication challenges. One of the major issues is that the quality and performance of the overgrown LEDs will rely on both the etching profile of the micropatterns out of the SiO_2 mask layer, as well as on the overgrowth conditions of the epitaxial layers themselves. Overgrowth itself presents some growth challenges, but has proven itself to be a powerful tool for µLED batch-production at less of a performance impact as compared to ICP-RIE etching.

1.3.3: III-Nitride HEMT default-ON operation, non-polar 2DEG difficulty, imbalance in hole mobility

Quite high up in the list of reasons why III-N HEMTs are not as widely adopted as their strong performance should present them as good candidates, is the fact that they rely on the

aforementioned 'foreign' substrates for any practical application and native/SiC substrates being expensive.

Difficulty in achieving default-off operation for transistors (that is to say, their turn-on threshold voltages are in the negative regime) makes HEMTs unsuitable for logic circuits in their default depletion-mode architectures [116], though enhancement-mode versions have been fabricated before with additional insulator layers or vertical arrangements [117], and even commercially produced, which carry with them the trade-off of a smaller saturation current density than their depletion-mode counterparts. Silicon vertical drivers for GaN-based HEMTs is supposed to be an excellent driver circuit that helps alleviate some of the switching issues encountered [116].

Non-polar GaN is even more difficult to get acceptably-performing HEMT devices on, due to the fact that its planar archetypes lattice-match the respective substrates even less. While freestanding m-GaN substrates exist for example, and have been used to demonstrate HEMT proofs of concept [118], they are even harder to grow than freestanding c-plane GaN substrates. Therefore, the bulk of the work performed here on non-polar GaN/AlGaN HEMTs consists of examples grown on cleaved r-plane (-12-10) sapphire substrates with an a-plane GaN buffer, which leads to a biaxial strain used this way. Compared to c-plane GaN growth, this paves the way to significant dislocation characteristics and subsequent poorer mobility characteristics [111]. In addition, due to the lack of an intrinsic built-in electric field, doping techniques are necessary in order to induce any sort of conduction in the main channel. Provided these challenges are overcome, however, non-polar HEMTs have the potential to have high-mobility default-off operation and have complementary optoelectronic devices integrated alongside them with QCSE suppression.

The last point worth mentioning is that III-Nitride semiconductors have an unusually high electron to hole mobility ratio [119] (though not as extreme as III-arsenides) , which makes them less ideal for p-type channel operation. Compounding this factor is a natural tendency to have a mild case of the aforementioned n-type unintentional doping problem, and the fact that p-type dopants such as Mg (in the form of Mg^{2+} ions) substituting Ga^{3+} ions struggle to fully activate in bulk GaN. Contrast this with germanium, which does have a high hole mobility about half of its electron mobility [120], and it is evident that III-Nitride semiconductors are less suitable for bipolar or complementary logic devices.

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Chapter 2 – Background

2.1: General Semiconductor Theory

Semiconductors are quintessential to the field of electronics due to their flexibility in being able to achieve varying degrees of conduction, as opposed to full insulators which have very high resistivity, and metals, which are almost always conductive.

2.1.1: Introduction to Semiconductor Physics: Atomic Theory and Band Diagrams

Semiconductors are solid-state materials that lie between metals and insulators in terms of their conductivity; that is determined by per unit volume mobile electron count as well as other factors. To exemplify the metal model before how semiconductors fit in, Figure 2.1 shows a Li atom.

The isolated Bohrian atomic states are used to represent individual atoms, with their corresponding electron shells. Each atom by further derivations of this model has electron outer shells that may be represented by their shell position (1s, 2s, 2p, 3s, 3p etc…) and the electron's energy level, alongside the Pauli exclusion principle. All electrons must maintain some energy to be able to keep their orbit. The energy levels of each state vary depending on spin, atomic number etc. Niels Bohr is well-known to have deduced following Rutherford's experiments that electrons have momenta that are equal to integer multiples of $h/2\pi$, where h is the Planck Constant (6.63×10^{-34} J s). [1] The Bohr model of a lithium atom and how that converges into a full metal band diagram may be simplistically represented (in reality, there are band dispersions in solid materials to be discussed in Chapter 2.1.2) by Figure 2.1:

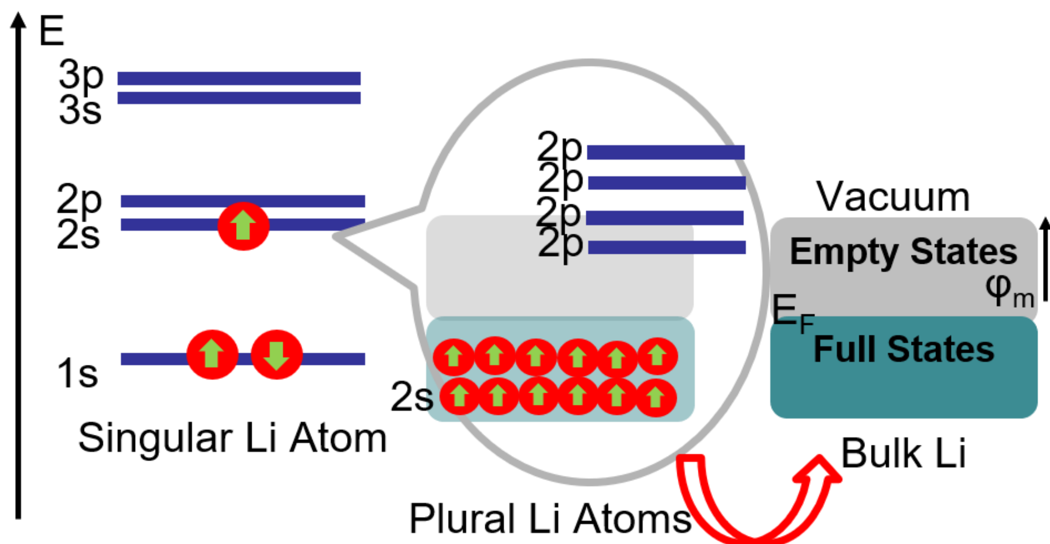

Figure 2.1: Simplified model of a lithium atom as derived from Bohr's theory overlapping first into their shell bands with their overlapping energies, then into bulk metal bands[2].

This modelling is where the concept of full or empty states comes from, marking a gradual transition from electron-populated areas to higher energy bands these electrons can go to conduct. Thus, one such quantised atomic energy level is referred to in literature as a quantum state. The vacuum state of Li is hereby marked by the highest energy point of the overlap between empty 2s shells and the lower 2p shells, and the energy to overcome this is the work function.

As atoms get bunched up more until they form material growth more in line with their bulk state, these individual states add up first to closely-grouped discrete states, then to a continuous band when they have enough neighbouring atoms to be considered to have formed a bulk material. For metals, the transition from full to empty states is continuous yet abrupt. However, semiconductors are different in that they have a wide divide in empty and full electron states, which in physics is widely referred to as a band gap. With very few exceptions, electrons may not occupy energy levels within this band gap, and if they are to conduct, they need to be raised all the way from the valence band edge, where electron full states normally exist, to the conduction band edge, which is analogous to the empty electron states of a metal [2]. A would-be semiconductor is considered to be an insulator if its bandgap is too large.

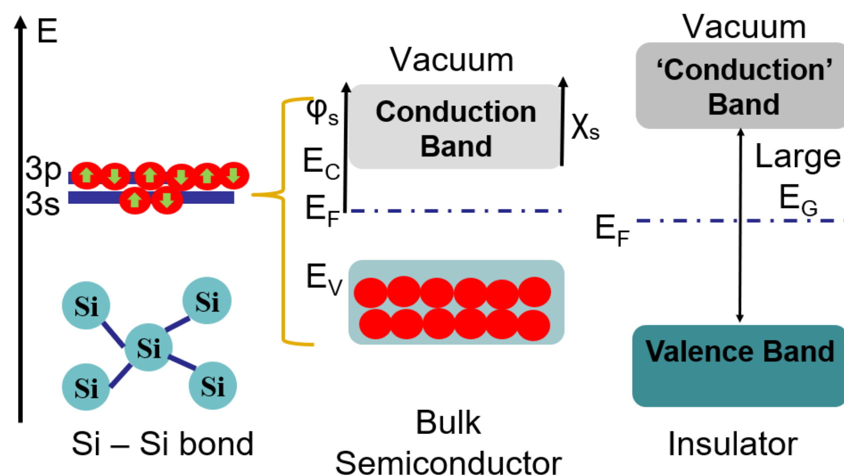

Figure 2.2: A simplified illustration of Si as a stand-in for semiconductor band diagram and formation, with an insulator for comparison [2].

GaN has an even larger bandgap as there is even an even larger energy separation between the filled bands and the next permitted empty ones. Once an electron is 'liberated' from the filled states and moves around, a broken bond does also, which gives rise to the term 'hole'. The actual distribution of an electron follows the Fermi-Dirac statistics as such[3]:

$$g_{CB}(E) = 4\pi(2m_e^*)^{3/2}h^{-3}(E - E_C)^{1/2} \quad (2.1)$$

$$n = \int_{E_C}^{E_c+\chi} g_{CB}(E)f(E)dE \quad (2.2)$$

$$Therefore\, n \;= N_C\, exp(-\tfrac{E_C - E_F}{k_B T})\, ;\; N_C = 2[2\pi m_e{}^* k_B T/h^2]^{3/2} \qquad (2.3)$$

$$E_{Fi} = E_V + \tfrac{1}{2}E_g - \tfrac{1}{2}k_B T\, ln(\tfrac{N_C}{N_V}) \qquad (2.4)$$

Vice versa is true for hole concentrations. g(E) is the density function of states; f(E) is the Fermi-Dirac probability that an electron will be at this energy, and n is the electron density per unit volume. N_C is the effective density of conduction states. m* is the effective mass of the carrier – while an electron's mass is 9.11×10^{-31} kg in free space, its perceived mass needs to be taken into account due to how it moves in the semiconductor crystal [4]. A typical distribution of density function g(E), probability function f(E) and electron states n(E) in a semiconductor with respect to energy levels may be found on Figure 2.3. This charge carrier distribution means that the greatest charge carrier density is actually half a k_BT (Boltzmann Constant, 1.38×10^{-23} J K^{-1}, times the absolute temperature in Kelvins) away from band edges, and this knowledge has its uses in fine band engineering for devices. Fermi Energy (E_F) is the statistical average carrier energy, so it moves as the semiconductor leans more towards electrons or holes.

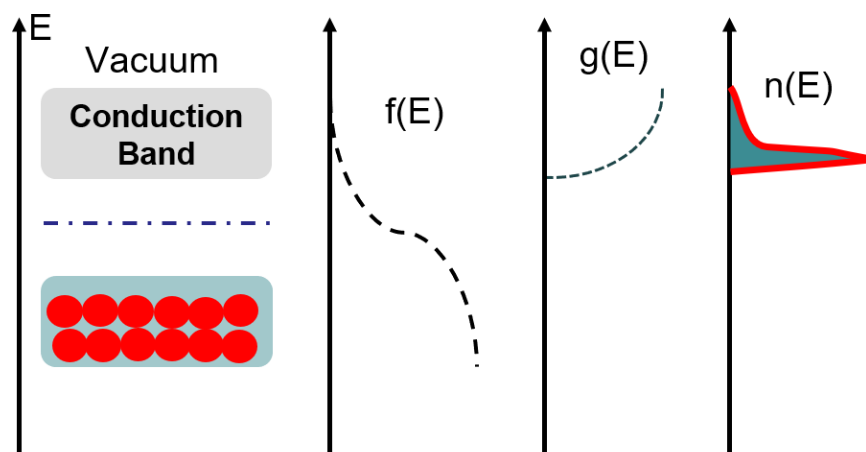

Figure 2.3: Fermi-Dirac distributions of an electron exemplified. [3].

Because energy bands are not straight in reality but follow a dispersion in terms of energy positioning, gaps come in direct and indirect variants on a k.p diagram[5]; this is a measure of the carrier bands' relative position against each other in terms of energy and a concept more easily referred to as a carrier vectoral momentum. A momentum change between any carrier split-ups and recombinations cause phonons in the structure – a particle-type representation of lattice vibrations that occur due to transferring that extra momentum, as is the case with indirect bandgap semiconductors. Direct bandgap semiconductors, however, only emit photons – a particle model of light waves – for the most part, as they do not experience the same carrier momentum change, they are far more efficient emitters than indirect bandgap semiconductors and a contributing factor to III-

Nitrides replacing SiC as blue light emitters [6]. Figure 2.4 shows such a momentum-energy graph to conceptualise direct and indirect bandgap semiconductors, with the green particle representing a photon of energy hv – Planck's Constant times frequency – and Er representing the intermediate energy state a phonon emission takes an electron to before recombination.

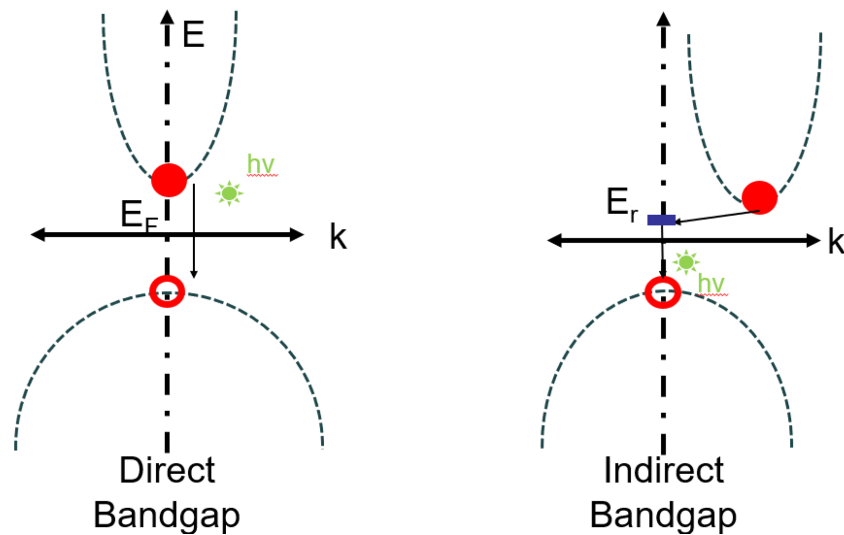

Figure 2.4: Direct vs Indirect Bandgap, simplified [6].

Equation 2.5 mathematically represents the parabola arc of carrier energy by carrier momentum as depicted in Figure 2.4; for each charge carrier type, there is an energy-momentum relationship that is proportional to the square of the carrier momentum and inversely proportional to the effective mass of the carrier, much in line with traditional mechanics. Naturally, there is an offset for the conduction band of an indirect bandgap semiconductor and is flipped along the k axis with the valence band. In reality, carrier momenta are multi-dimensional, and the next Subchapter will explore the realistic bandgap dispersions by lattice vector.

$$E_k = \frac{\hbar^2 k^2}{2m^*} \ where \ \hbar = \frac{6.63 \times 10^{-34} \ J \ s}{2\pi} \tag{2.5}$$

Even this is a simplified view of a band diagram, as in reality a semiconductor will have band dispersions. As well, simplistically overlaying electron orbital states into a band diagram does not explain why compound semiconductors, like AlN, or carbon as diamond, have very large bandgaps.

2.1.2: Band dispersion, Brillouin Zones, and related Wave Vectors

The model presented above ignores the inter-orbital forces that form the real band dispersion, reciprocal space and the resultant wave-vector related more realistic band structures.

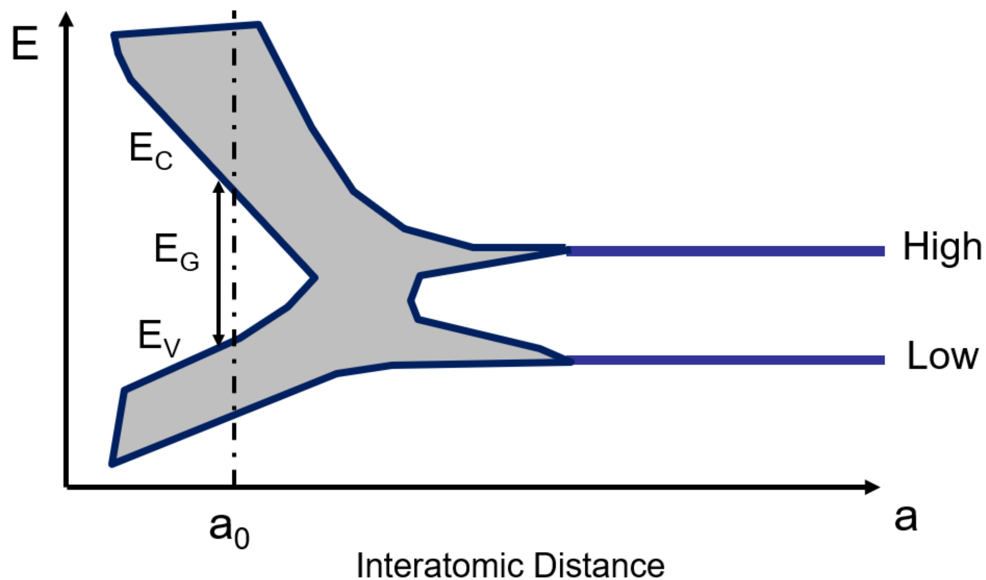

Figure 2.5: A more realistic generic band dispersion showing conduction and valence band split by interatomic distance at lattice constant a_0, versus cases of different a-constant values. [7] .

Electronic orbit interaction between the constituent atoms, in fact, causes a band split of the p and s states, as with Figure 2.5 as a representation of a generic semiconductor.

This graph consists of four main regimes: When interatomic distances are sufficiently large, as with a standalone atom, the material is defined purely by the atoms' spin orbitals, depicted generically as High and Low as it could be any order of orbitals. Bloch periodicity is used to calculate a real version of this to complete the potential model. The second regime depicts interatomic distances still quite a bit larger than the lattice constant a_0, but more densely packed than the standalone model; not only do individual states start to merge slowly, but the inter-electronic forces are starting to disperse them, which translates to a range where orbitals do have filled states all throughout with this level of strain; as with metals. Meeting a_0 presents the third regime where the semiconductor's intrinsic bandgap forms due to inter-electronic forces now being strong enough to cause forbidden energy states. The fourth regime is atoms coming closer together still will cause an even larger potential separation as compliant with the Pauli exclusion principle – as with insulators [7]. Thus, lattice parameters are key determining factors in band gaps or a lack of them.

Lattice wave vectors and a brief spatial theory is also necessary to holistically understand realistic semiconductor behaviour. One such example for GaN and AlN is on Figure 2.6. The direct bandgap nature of these III-V semiconductors is clear with the Γ wave vector.

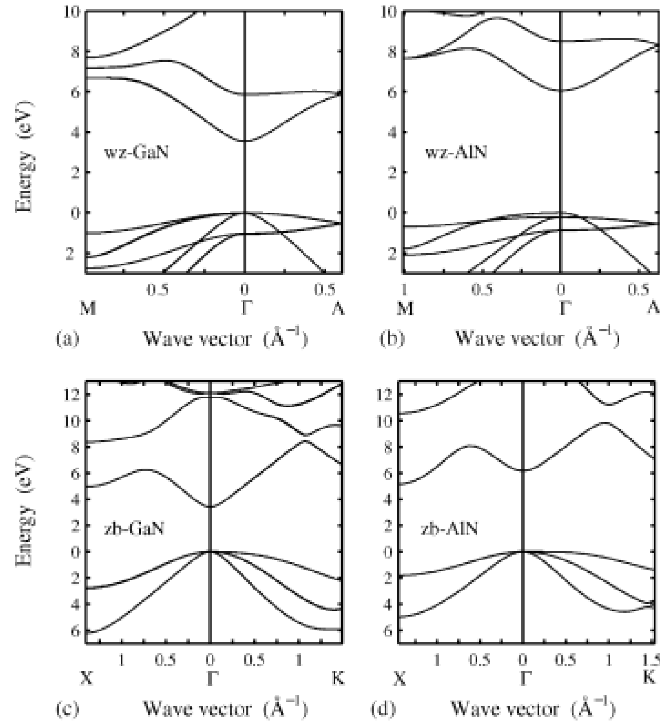

Figure 2.6: Dispersion plots for GaN and AlN, both Wurtzite ('wz-', above) and Zinc Blende ('zb-', below) [8], © 2001 Elsevier Science B. V.

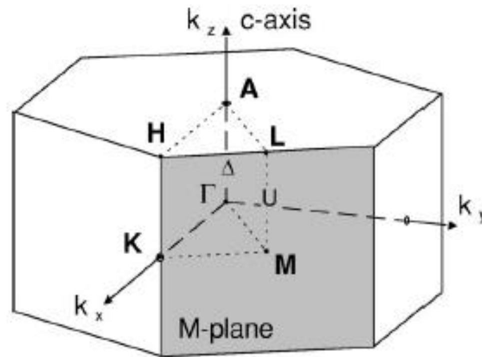

Figure 2.7: An illustration of a Brillouin Zone with a Wurtzite GaN cell [9]. Reprinted (Figure 1) with permission from C Cobet et al, © 2001 American Physics Society.

A Brillouin Zone in a Wigner-Seitz cell is exactly the reciprocal space representation that is necessary to reflect this; the lattice in question transposed onto the inverse of its planes of existence, with Figure 2.7 being an illustration of the zone and Figure 2.8 the density of states. The K-space, as it is referred to, has an origin Γ and cellular arrangement-dependent vectors such as Δ (0001 direction for WZ intersecting halfway the 0001 plane, 100 halfway for any Face Centred Cubic), A (0001 WZ full plane centre), and M (1100 WZ), which are planes of existence intersecting crystal planes depending on their packing [10]. The concept of Miller Indices will be explained in more

detail in 2.1.6. Because lattices exist in three dimensions, the wavevector notations are useful for plotting band dispersions short of an alternative real-space model. The ε_n (K) plot – a more realistic depiction of carrier energy dispersion by wave vector – also depicts the orbitals in the form of 'light', 'heavy' and 'split-off' orbitals. Equation 2.5 holds true close to Γ.

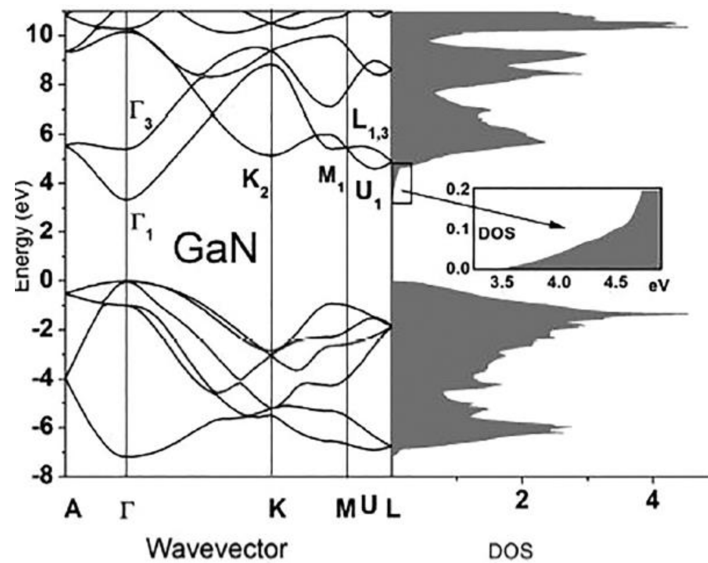

Figure 2.8: GaN dispersion curve overlaid with the density of states resulting from the Fermi-Dirac principles. Reprinted from [11] with the permission of AIP Publishing.

2.1.3: Semiconductor Doping: Extrinsic Semiconductors

The band structure of semiconductors implies that they do not conduct very well intrinsically, except in very large forward electric fields, or at high temperatures, where there is significant thermal electron-hole pair splitting. Electronic circuits usually rely on doping to be able to achieve a particular type of conduction under most thermodynamic conditions.

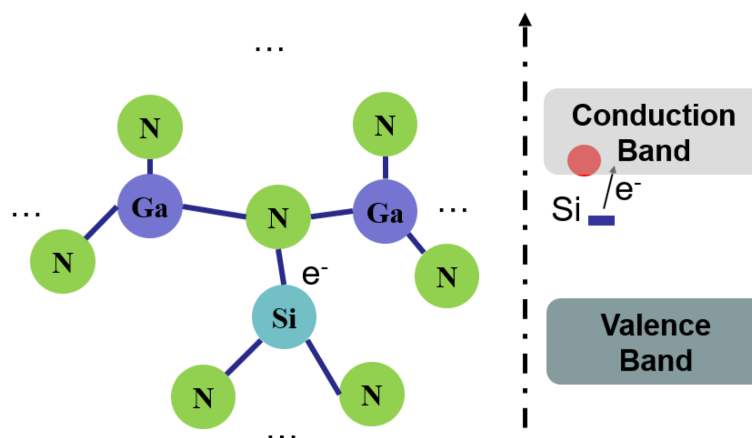

Figure 2.9: Illustration of Si doping with GaN, using a small section of its lattice. [12].

Doping is the process of introducing impurities into the semiconductor so that they substitute one of the species involved and introduce either an excess of electrons, leading to more n-type conduction, or an excess of alternating valence states where electrons should be, also known as electron holes or simply holes, leading to more p-type conduction. These impurities usually require an additional step to activate, like high temperature treatment, and it is best to dope a semiconductor during growth to achieve a better doping uniformity and make sure that all of the dopant species are activated properly, also known as full ionisation. In the example of Figure 2.9, Si is considered a donor to GaN, as it substitutes a Ga^{3+} species and replaces it with Si with 4 electrons in its orbitals. As a result, Si replaces the triple bonds, but adds an extra free electron to the system, which is free to conduct. In addition to the presence of orbitals, the energy rating of the said substitute species is also important. Si is considered a 'shallow' donor to both GaN (≈ 30 meV) and AlN, meaning its energy separation with the conduction band is small – while C is a shallow acceptor meaning it contributes holes close to the valence band [13, 14].

The law of mass action dictates that no matter what the electron or hole concentrations are, their product remains equal to the square of the intrinsic concentration:

$$np = n_i^2 = N_C N_V \, exp(-\frac{E_g}{k_B T}) \quad (2.6)$$

Thanks to it, the minority carrier concentrations could be calculated too by dividing the square of the intrinsic concentration with N_d or N_a, assuming all of the donors/acceptors ionise, such as:

$$n = n_i^2/N_a; \; p = n_i^2/N_d \quad (2.7)$$

On a band diagram, dopant species may be represented as though they are occupying energy states close to the valence band (p-type) or close to the conduction band (n-type), thus promoting more holes or electrons into each band respectively than their intrinsic Fermi energy would suggest. It is no surprise then, that the extrinsic Fermi level for a doped semiconductor shifts closer to the band of interest.

The downside to adding dopants to a semiconductor is the defects it will add to the crystal. Si doping of GaN requires advanced methods to push beyond 1-2×10^{19} cm-3 as this is when there is significant unintentional 3D growth taking place during a nominally 2D growth phase [15].

Somewhat relevant to the paradigm of doping is the concept of degenerate doping. Semiconductors have an intrinsic rating of effective density of states per band, which also dictates the upper limit of how far they can be doped before their Fermi Energy moves so close to either of

the bands and crosses over the edge of that band (e.g: if n > N_C then the semiconductor is degenerately n-doped). A semiconductor so heavily p-doped becomes a para-metallic hole conductor, whereas a degenerately n-doped semiconductor behaves exactly like a metal.

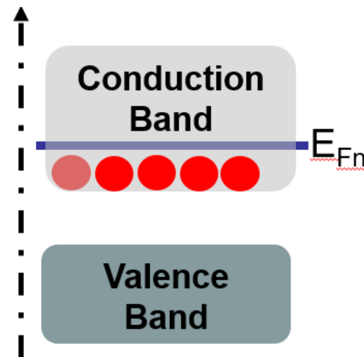

Figure 2.10: Degenerate n-type doping with the Fermi level crossing over the conduction band.

2.1.4: pn junctions, heterojunctions, metal-semiconductor contacts

While doping does enable semiconductors to conduct in one polarity, a uniformly-doped monolithic slab does not form an electronic device by itself and needs a diverse set of doped regions, oppositely-doped guard rings, or barriers altogether. The most basic of these is just a plain pn junction, the foundation of a basic diode, and later LED.

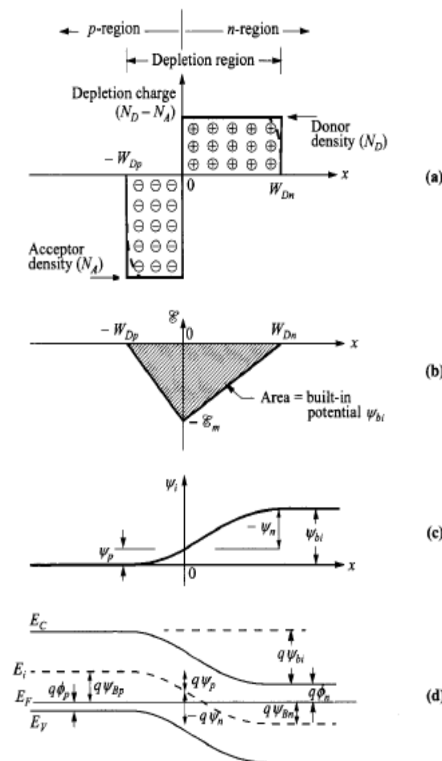

Figure 2.11: The band diagram, depletion charge and built-in potential of a pn junction [16] © 2006 Wiley.

In an equilibrium state when a semiconductor exists in multiple regions, whether it is a pn junction, a heterojunction or otherwise, the Fermi levels of the semiconductor sections need to align throughout the structure. [16]. As a result, in order to restore equilibrium within the structure, there needs to be potential equalisation of the pn junction, which creates an internal potential, and resulting depletion regions. This junction depth and field gives rise to the built-in potential, which is a measure of the pn junction's potential drop from one end of the junction to another. The built-in potential has many implications, and the internal electric field resulting from it has applications especially in LEDs.

Most semiconductor applications have metal contacts to provide a conduction channel. Metal-semiconductor junctions present a levelling of the Fermi Level throughout the structure, as this must be aligned throughout a structure in equilibrium. Thus, the metal contact surface presents a surface state – a wave function that is located at the abrupt junction between metal and semiconductor – which is how Ti_xN forms an Ohmic contact for example upon activation [17]. This is the Fermi pinning effect, which is also quintessential to metal-semiconductor interfaces that use the Schottky-Mott rule to determine the theoretical barrier height between the two regions, which states that the Schottky barrier – potential of entry from the metal to the semiconductor – must be equal to the difference between the metal work function and the semiconductor electron affinity. In practice, the real barrier height may be slightly different. The limit of the barrier potential is thus given by [18]:

$$q\varphi_{Bn0} = q(\varphi_m - \chi) \qquad (2.8)$$

Where q is the electron charge; φ_{Bn0} the potential of the Schottky barrier at interface; φ_m the metal work function; and χ the semiconductor electron affinity – potential from conduction band to vacuum level.

Figure 2.12 shows the band diagram of a metal-semiconductor junction with a p-type semiconductor in two separate circumstances; a) is the surface state displayed as if it were consisting entirely of the vacuum and b) using the so-called fixed separation model to depict how the metal would fit into this model with the surface state between the two being depicted as if the two layers were 'on the verge of merging with a small vacuum in between'. Although the main point of [18] is to explain a mechanism for practically observed Schottky barrier heights and formation of an electric dipole in metal-semiconductor surfaces, it clearly shows their Fermi level pinning.

The band bending is upwards in energy deeper into the semiconductor thanks to its closer to VB Fermi Energy; vice versa is true for an n-type semiconductor.

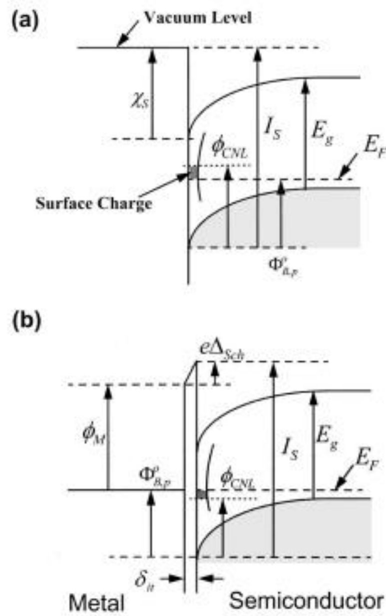

Figure 2.12: A p-type semiconductor and metal junction, exemplified, with a) being the surface/semiconductor band diagram and b) using the fixed-separation model of surface states with a metal for this junction. Reprinted (Figure 2) from R. T. Tung, [19], © 2001 American Physical Society.

A major drawback of using only pn junctions as emitters has the inherent problem of re-absorbing more of the emitted photons than ideal. Simple doping differentials may also be insufficient for power devices due to defect scattering. This is where heterostructures come in, so differing bandgaps provide a potential structure and lack of main channel scattering that a homojunction with differing doping levels and types cannot.

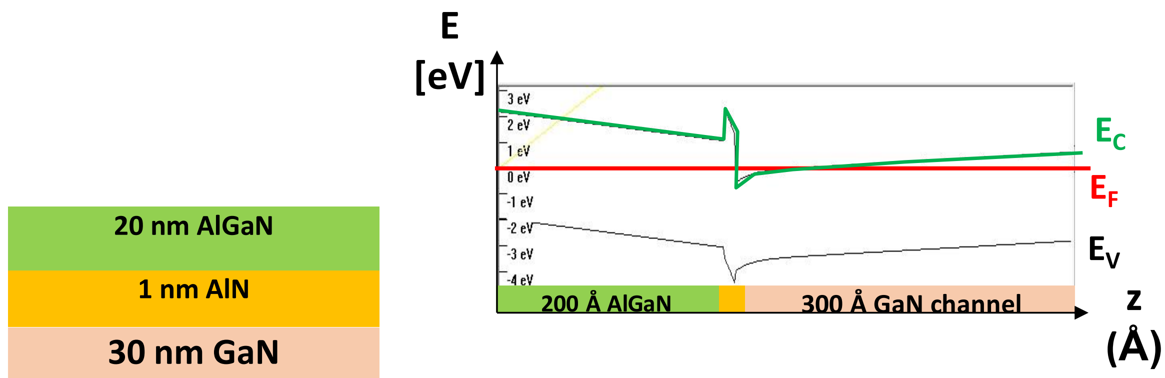

Figure 2.13: A simulated example heterojunction, as one may see in GaN/AlN HEMTs, and its corrected band structure, full polarisation. Modified to clearly show the growth axis (z), conduction band (E_C), valence band (E_V) and the pinned Fermi level (E_F) for the left contact being a Schottky metal. The scale is in electronvolts (eV) and Å respectively.

Heterojunctions are commonly used in LEDs, for example with AlGaAs/GaAs structures or with InGaN/GaN multi-quantum wells (that forms the basis of III-N LEDs), in order to enhance light emission efficiency also tying into internal quantum efficiency [20]. Power devices benefit from larger potential drops and thus better 2DEG confinement, as is the case with AlGaN/GaN HEMTs.

Figure 2.14 demonstrates with rough band diagrams and epitaxial structures the two concepts; a) shows why heterojunctions are less likely to reabsorb emitted photons than homojunctions: As emission most likely happens in the smaller bandgap material (GaAs) due to electron and hole potentials at the time of recombination, only a portion is reabsorbed but most of the time a photon will leave the active region and has to meet AlGaAs's bandgap for photon (re-) absorption. In contrast, it can happen with a homojunction more easily before leaving the LED.

Figure 2.14 b) shows why AlN spacers are useful for 2DEG concentration in the case of GaN HEMTs by displaying the potentials with and without the thin spacer. Thanks to electrons moving from the AlGaN barrier through the AlN spacer electrons will meet at the GaN channel junction to form 2DEG and because the barrier from GaN to AlN is too steep vice versa is difficult. Thus, a thin spacer helps with the confinement of 2DEG electrons.

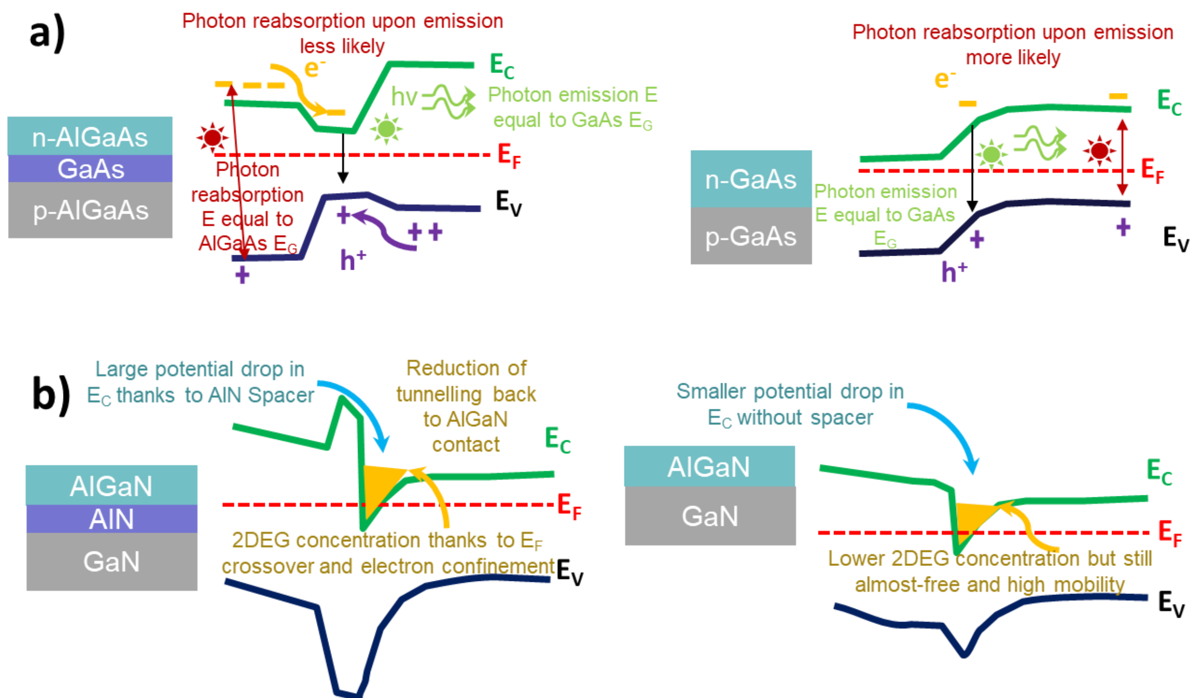

Figure 2.14: An illustration of why **a)** heterojunctions tend to reabsorb fewer emitted photons and **b)** the benefit of using AlN spacer in GaN/AlGaN HEMTs.

Modulation doping with the latter type of heterojunctions is also useful, which will be central to understanding HEMT theory.

2.1.5: Brief Introduction to Quantum Mechanics

Quantum mechanics are a natural consequence of the Bohr model for atoms as well as later improvements on it, and is named so due to the fact that at the nanometre or Ångström scale, materials behave less like their bulk form and more like a small group of discrete energy levels where intra-band transitions are more abrupt; this discretisation, or quantisation, is why it takes the name quantum (Latin for a word pertaining to amount) mechanics.

Critical to this discussion is the mention of the Einstein relation and de Broglie wave-particle duality, which also ties charge carriers to the momentum concept discussed earlier. A particle of momentum p has an associated wavelength of λ [5]:

$$\lambda = \frac{h}{p} \tag{2.9}$$

The Planck-Einstein relation then specifies that the energy of a photon must be equal to the Planck Constant multiplied by the frequency [21]:

$$E = \hbar\omega = hv \tag{2.10}$$

An electron, time-independently, and freely, could be said to hold a potential, r units away from the influence of other external electromagnetic potentials, as such [5]:

$$\psi = e^{ikr} \; where \; k = 2\pi/\lambda \tag{2.11}$$

This forms the basis of a wave function. The time-independent Schrödinger Equation, following this, for a free electron along one axis, under a bias V(x), which may be zero, would be noted down as:

$$-\frac{\hbar^2}{2m}\frac{d^2\psi}{dx^2} + V(x)\psi(x) = E\psi(x) \tag{2.12}$$

In reality, electrons and holes are bound to a crystal, so their wave functions would actually change as according to the lattice. A more realistic simplistic model could read:

$$\psi(x) = A\,sin(\frac{n\pi x}{a}) \; and \; E_n = \frac{\hbar^2\pi^2n^2}{2ma^2} \tag{2.13}$$

Which binds the wave functions to a physical small section of the crystal, as is the case with infinitely-deep barriers encasing a nanometre-scale lower band gap structure. This is called a quantum well. Moving to a finite barrier sees the functions then use the difference between the wave function potential and the potential to the top of the barrier. This forms the basis of Schrödinger-Poisson solutions in 1D.

2.1.6: Crystallographic arrangements, Miller Indices

Materials, depending on how they form in bulk, assemble themselves in certain formations, which is called their crystallographic arrangement, as their lattice orientation has parallels with naturally-formed crystals. Lattices may also assemble themselves in different orientations subject to how they are grown. Such polymorphisms are important for the end performance of the material. The main ones that will be covered are Wurtzite and Zinc Blende (and the very similar diamond cubic) cell types, as these are the relevant formations to the study.

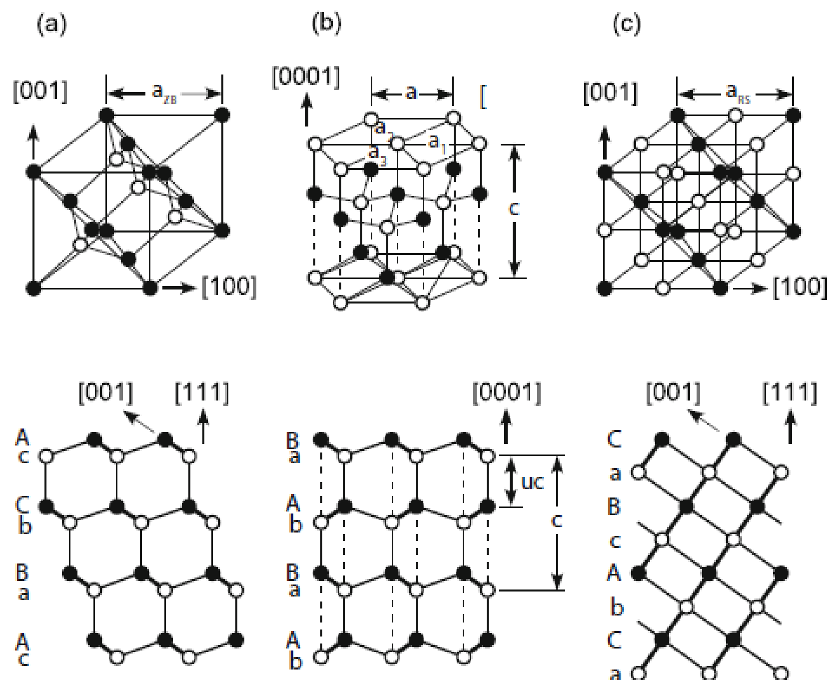

Figure 2.15: Zinc Blende, Wurtzite, and rock salt structures [22]. © 2009 Springer Berlin Heidelberg.

Wurtzite cells, as with Figure 2.7 and Figure 2.18, the default arrangement in GaN, InN and AlN, are named so for their namesake hexagonally-arranged zinc and iron sulphide ore. Their hexagonal arrangement could be thought of as a hexagonal prismatic crystal arrangement of mainly ionic bonds, where for every atom of the first, positively ionised species, there is exactly one of the negatively ionised species in an empirical standpoint. The lattice constants are identical across the horizontal axis of the structure, also known as 'a' constants, but the vertical constant, called 'c', is different from the other three. The unit cell is thus a rhombic block formed of one of the a constants and the c constant. The bond angle of the species along the a axes is 120° and that for the c axes is 90°. The polymorphic hexagonal structure of SiC is also similar, except it usually has interruptions between hexagons in the form of twisted Si-C bonds.

Zinc Blende on the other hand is the cellular type that III-arsenide semiconductors arrange themselves in. It is quite analogous to the diamond cubic structure that Si and similar elements use. In essence, Zinc Blende is a collection of bonds arranged in a tetrahedron arrangement, each with a 3D bond angle of 109.5°. It is what is known as a face-centred cubic structure.

The combination of these unit cells and for them to form a continuous array of positions from a discrete set of points produces what is known in crystallography as a Bravais lattice.

This lattice-wise arrangement is addressed through the use of Miller Indices, which are numerations of the cell axes. Miller Indices (such as (0001)) were used in order to address the material's planar direction. That, for example, refers to the 3 'horizontal' lattice constants, a1, a2, and a3 in a Wurtzite cell, with a non-equivalent c axis.

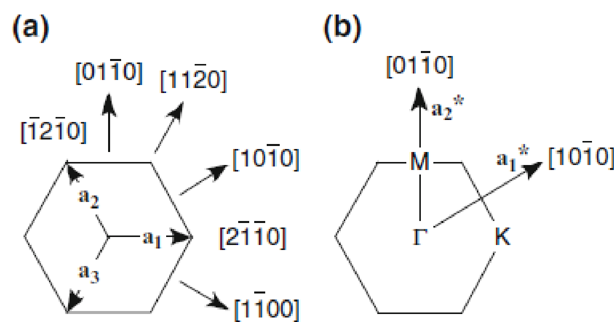

Figure 2.16: Fundamental and reciprocal lattice vectors for Wurtzite GaN [22]. © 2009 Springer Berlin Heidelberg.

2.2: Group III-Nitride Semiconductors: GaN, AlN, InN and Alloys

While not all of these concepts will be endemic to III-N semiconductors, they are nevertheless relevant to understanding and proposing improvements on existing devices for the material set using an epitaxial approach. The main ones of importance are the concept of polarisation due to their growth planes, unintentional doping, and dislocations.

2.2.1: Electrical Polarisation: Types, How they Arise, and QCSE

Polarisation is an important aspect of III-Nitride materials science due to the fact that it dictates the intrinsic conduction characteristics of the material set, where there exists an internal electric field or a lack of it depending on which plane the semiconductor slab was grown. As the terminology could easily be confused with optical polarisation (restraining the photon oscillations in either the electric or the magnetic axis, which is especially important for optoelectronics) or other physics phenomena, the Author has opted to use 'electrical polarisation' to distinguish between the

different types. There exist two different types of polarisation: Spontaneous and piezoelectric polarisation.

Spontaneous polarisation occurs between opposite bonded species and despite the name, is constant for a certain direction of growth. The internal electronic tendencies of this type of polarisation arise from the electronegativity difference between the two components of the semiconductor, which in turn gives a preferential direction for electrons, thus creating dipoles. The magnitude and vectoral direction of the polarisation is dependent on the semiconductor's 'natural' crystallographic arrangement. For GaN/AlN/InN, which are all intrinsically Wurtzite unit cells (though they can also be grown Zinc Blende), the cellular arrangement of the Group III and N atoms as closely as possible to it drives spontaneous polarisation. The formula for the magnitude of spontaneous polarisation for c-plane AlGaN is as follows [23]:

$$P_{SP}(Al_xGa_{1-x}N) = (-0.052x - 0.029)\ C\,m^{-2} \tag{2.14}$$

Where P_{SP} is the spontaneous polarisation and x the Al percentage, with a C being a Coulomb; unit of charge. This way, it is possible to calculate the P_{SP} of any cellular arrangement of III-Nitrides. For example, c-plane GaN has a P_{SP} of -0.029 C m^{-2} and pure AlN has -0.081 C m^{-2}. a (11-20) and m-plane (10-10) GaN have a P_{SP} of 0 in theory, though parasitic spontaneous polarisation may still exist as growth is not perfect. Figure 2.17 illustrates the concept with GaN, using a unit cell, as an example. The electronegativity difference between Ga and N means that electrons tend towards N more, creating an internal electric field that defines this spontaneous polarisation.

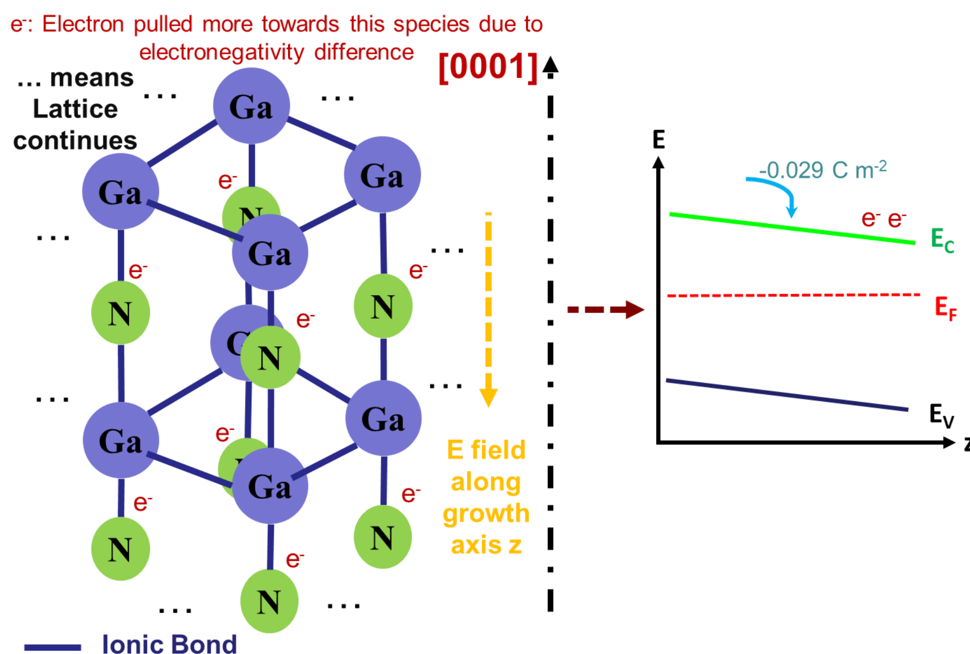

Figure 2.17: Illustration of spontaneous polarisation in GaN.

Depending on whether the wafer is N-faceted or Group III-faceted (as in the case of Figure 2.17 for the latter), a c-plane (0001) III-N semiconductor either has a 'forward' or 'reverse' polarity. Spontaneous polarisation accounts for the majority of the total polarisation within III-nitride devices.

The second type of polarisation of concern is piezoelectric polarisation. As the name suggests, this type of polarisation happens due to the post-growth strain of the semiconductor, as III-N semiconductors are piezoelectric materials to some degree due to the fact that they have a relative permittivity much greater than 1. By extension, piezoelectric polarisation also relies on the elastic components of this aforementioned strain, and may be calculated as such for GaN:

$$P_{PE} = 2\frac{a-a_0}{a_0}\left(e_{31}e_{33}\frac{C_{13}}{C_{33}}\right) \quad (2.15)$$

Where e_{31} and e_{33} are lattice-wise piezoelectric coefficients; a is the strained lattice constant of GaN; a_0 is the un-strained constant, and C_{13} and C_{33} are elastic constants of GaN. Piezoelectric polarisation amounts for far less of the internal polarisation in III-N semiconductors as compared to spontaneous polarisation, but still exists parasitically due to the given reasons even in nominally non-polar wafers. Together, these components make up the total polarisation that exists in the wafer.

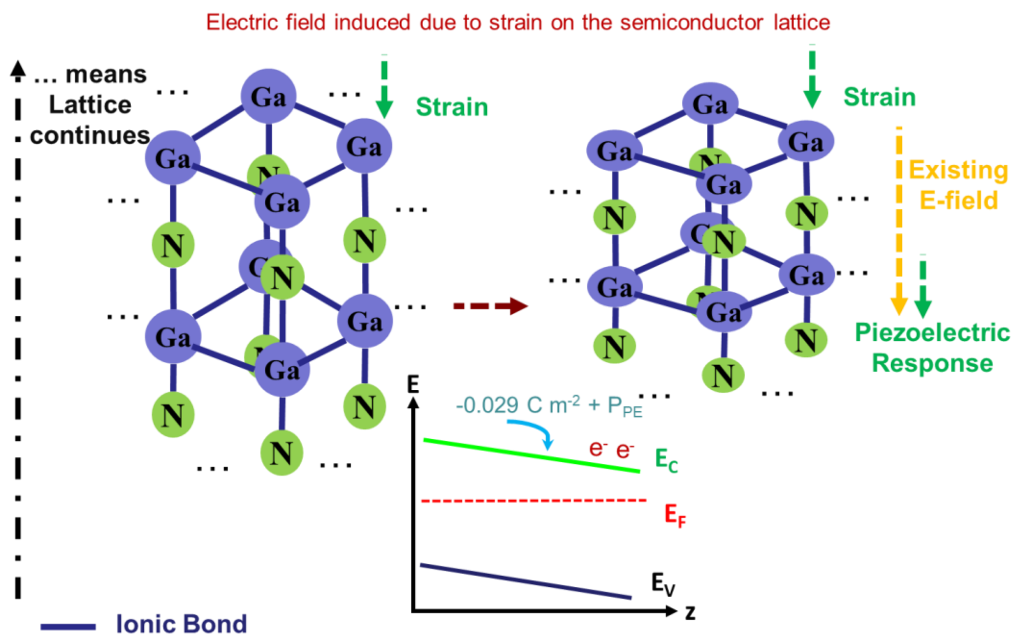

Figure 2.18: Illustration of how piezoelectric polarisation applies on top of spontaneous polarisation.

As with Figure 2.18, due to the dielectric constant of the semiconductor, the application of force on the semiconductor will generate a further electric field, which may enhance or oppose the spontaneous polarisation based on the resultant strain. Sometimes, this strain will arise naturally

due to the stress – force per unit area – caused by the lattice mismatch between adjacent layers, such as between InGaN and GaN.

Figure 2.19 shows a fully-polar (0001) ‘c-plane’ AlGaN/AlN/GaN heterostructure, which means it has the full effect of spontaneous polarisation. This is in stark contrast to, for example, (11-20) GaN (Subchapter 2.2.2 has this GaN growth plane, also known as ‘a-plane’ as an illustration), which is a ‘non-polar’ plane, which does not have this built-in polarisation. On this said figure, the effects of a slightly thicker AlN spacer on the 2DEG concentration can be seen; up until this critical thickness, a thicker AlN spacer increases the electron concentration at the interface.

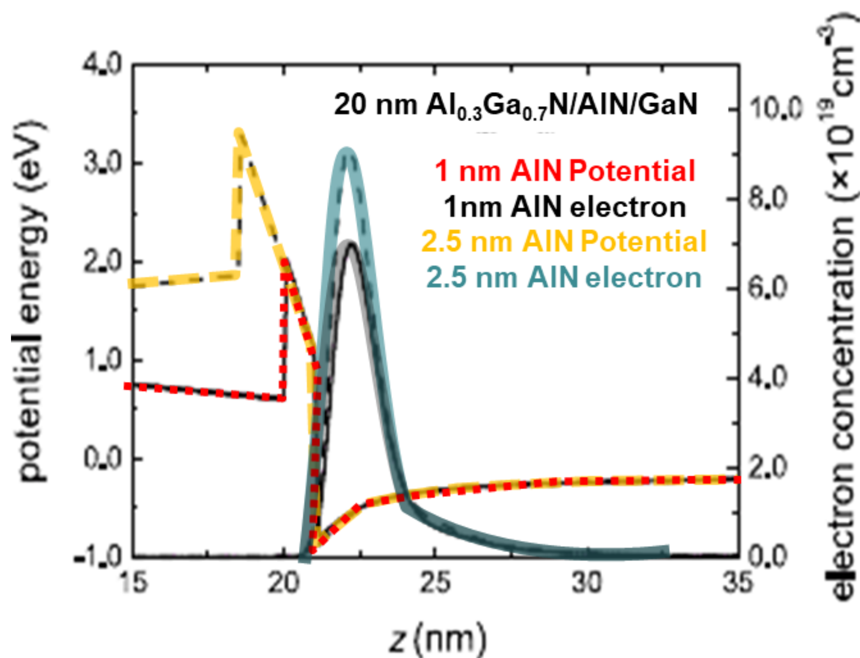

Figure 2.19: Example of a simulated band diagram of a fully-polar GaN/AlGaN heterostructure with AlN spacer (1 or 2.5 nm) and electron concentrations [23]. Modified for clarity. This also reinforces the idea in 2.1.4 that AlN spacers help increase 2DEG concentration. © 2006, Springer-Verlag.

Electrical polarisation can be beneficial or detrimental; while it enables III-N semiconductors to be able to conduct intrinsically, it also makes it more difficult to achieve a nominally default-off channel. As well, polarisation is a significant contributor to the wavelength shift and green light inefficiency observed in optoelectronic devices due to the aforementioned QCSE problem.

In order to understand QCSE – Quantum Confined Stark Effect – a visual illustration and a description of underlying theory are incredibly useful. Figure 2.20 shows how QCSE affects emission energy for a single InGaN quantum well LED with p-GaN and n-GaN as the barriers when a) full scale spontaneous polarisation causes a wavelength shift in c-plane GaN/InGaN and b) no spontaneous polarisation is present, and the near-elimination of QCSE (with only piezoelectric polarisation in

practice remaining). The electron and hole confined energies are clearly visible, complete with their approximate wave functions – quantum probabilities of an electron or hole being at a particular position and energy solidified into a wave, as mathematically described in Subchapter 2.1.5.

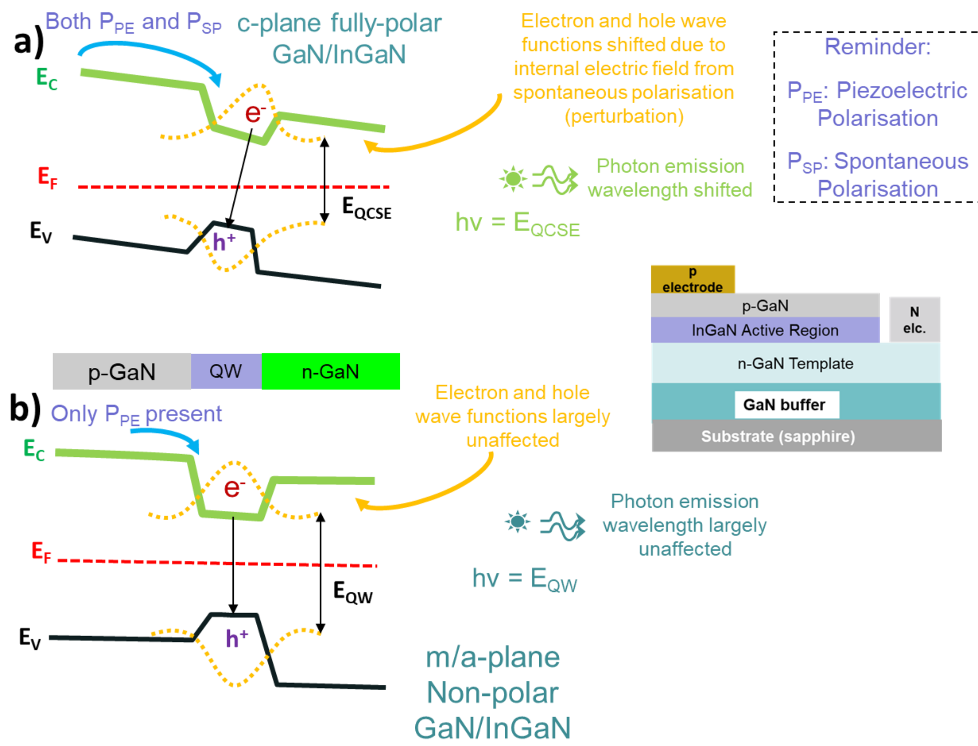

Figure 2.20: Demonstration of QCSE for a single QW LED for **a)** polar and **b)** non-polar III-Nitrides.

What QCSE does is that under applied bias and/or natural polarisation, it causes the wave functions to shift, and electron-hole recombinations take place at lower energies, that will be referred to as E_{QCSE}, as opposed to E_{QW}, the quantum well recombination energy by default. This energy disparity causes a red shift in emission wavelength, i.e.: lower energy photons. QCSE does indeed happen to non-polar quantum confined optoelectronic devices under forward bias for example, but it should be sufficiently clear from Figure 2.20 why the emission wavelength shifts further when spontaneous polarisation exists. It also affects absorption similarly.

QCSE wave function correction effects on first-order perturbation can be described by the following simplified formula as adapted from [24] because originally it contains the Bohr radius:

$$\Delta E_1 = -\frac{2048\, e^2 m^* a^4}{243\, h^2 \pi^4} \varepsilon_r F^2 \tag{2.16}$$

Where E_1 is the first confined state energy transition; m* is the effective charge carrier mass (total of electron and hole); e is the electron charge; a is the well thickness; h the Planck Constant; F the applied electric field and εr the relative permittivity of the semiconductor.

2.2.2: III-Nitride Semiconductor Crystallographic Structure, Lattice Constants

GaN normally adopts the hexagonal Wurtzite structure, which can be Ga or N-faceted, but the majority of GaN growth uses Ga-faced c-plane crystals. GaN and associated compounds are grown using MOVPE and depending on substrate termination, can adopt many different planar orientations. Four listed in Figure 2.21 are: The default c-plane (0001) which is fully-polar; the m (1-100) and a (11-20) planes which are non-polar and (11-22) which is semi-polar. It is possible to achieve other semi-polar orientations, however.

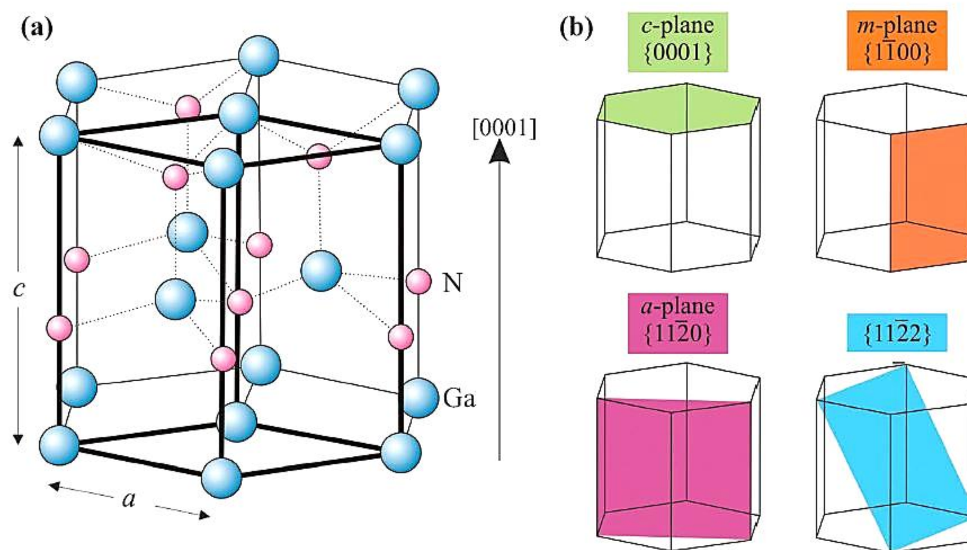

Figure 2.21: Wurtzite cell of GaN and four planar arrangements it exists in [25].

	Lattice Constant a [Å]	Lattice Constant c [Å]
GaN	3.189	5.185
AlN	3.112	4.982
InN	3.545	5.703

Table 2.1: III-Nitrides' lattice constants [22].

2.2.3: Overview of Unintentional Doping in GaN

GaN, as mentioned previously, is held back by its inherent unintentional doping that happens during wafer growth. It was mentioned earlier that O acts as a shallow donor for GaN, so will cause parasitic n-type conduction if incorporated into a GaN lattice. Ga^{3+} vacancies that form during growth lead to stacking faults, and are energetically favourably substituted with this aforementioned species, so there is a direct correlation between dislocations and unintentional doping. It is thought that this influx of O directly comes from the substrate itself [25].

2.3: III-Nitride LEDs Operation

III-Nitride LEDs, as mentioned previously, rely on a mixture of InGaN/GaN multi-quantum wells (MQW), a pn junction at a larger scale, and a p-AlGaN electron blocking barrier. The main emitting action takes place within the MQW structure, the main pn junction consisting of the GaN sections provides the built-in bias that allows it to operate as an LED, and the AlGaN layer reduces backwards leakage into the p-region, due to the significant imbalance between the doped regions and also doubly helps with extraction issues. A genericised GaN/InGaN Multi-Quantum Well (MQW) LED illustration may be found on Figure 2.22.

Figure 2.22: An illustration of a MQW GaN/InGaN LED structure.

In order to understand, in line with the heterojunction principles shown in Subchapter 2.1.4, how this MQW LED emits photons in the visible light part of the EM spectrum and how the alternating MQWs tie into repeated emission with little reabsorption once it leaves the active region, a band diagram is necessary. Figure 2.23 shows one such band diagram for an MQW structure with two repeats – a dual quantum well where well material is InGaN – to illustrate.

This LED structure harnesses the advantages of heterojunctions for improved internal quantum efficiency and quantum confinement for adjustment of emission bandgap. The AlGaN electron blocking layer reduces the electron flowback towards the p-GaN layer to further keep electrons towards the active QW region, but this comes with the trade-off of reduction of hole flow towards it. The emission wavelength is tuned by adjusting the In ratio within the InGaN QW layer, and higher In ratio leads to longer wavelength emission through smaller QW bandgap.

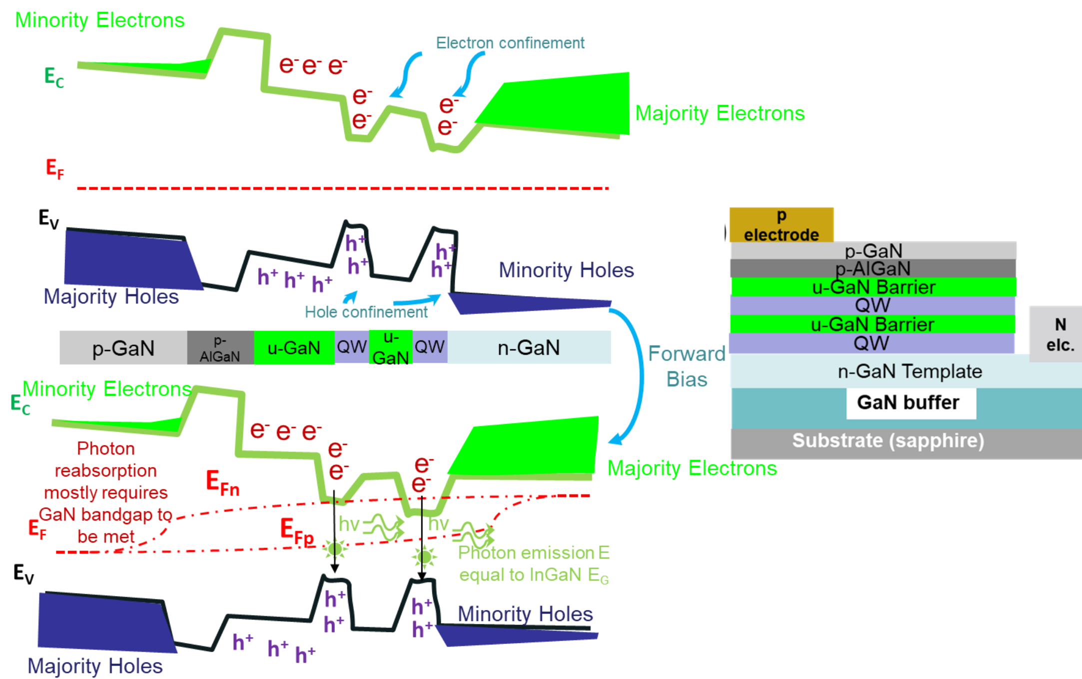

Figure 2.23: Rough band diagram of a dual quantum well LED on c-plane polar GaN.

Under forward bias, because the structure is no longer in equilibrium, two quasi-Fermi levels emerge for electrons and holes, labelled E_{Fn} and E_{Fp}. Meanwhile, the potential difference between the two electrodes decreases [16]; compounding these two factors, more electrons and holes in active region mean more radiative recombination.

2.4: III-Nitride HEMTs, 2DEG principles

HEMTs, as modulation-doped heterojunction field effect transistors, have a regime where 2DEG electrons collect thanks to both polarisation and doping. In either case, ionised donor species collect at the edge of the barrier conduction band and the Poisson principles-compliant potential band bending creates a potential profile which leads to an accumulation layer and a consequent almost-freely moving electrons in the GaN channel relatively devoid of impurities.

Figure 2.24 shows a GaN/AlGaN intentionally-doped HEMT structure, as seen in [26], with an illustration of the combined effects of the surface states, polarisation, Fermi level alignment and doping in the creation of a 2DEG layer at the GaN/AlGaN interface.

The metal-pinned Fermi states align within the structure to give the signature 'triangle' potential characteristic of these modulation-doped devices. It is thought that the surface states brought on by donors or surface-aligned Al/Ga species, usually around 1.65 eV, contribute to the start potential of 2DEG electrons and the bandgap mismatch offset between AlGaN and GaN creates the

potential drop, ΔE_c, between the two that helps confine these electrons. A thick-enough barrier – 35 Å in the instance of this structure below – is needed to encourage 2DEG formation.

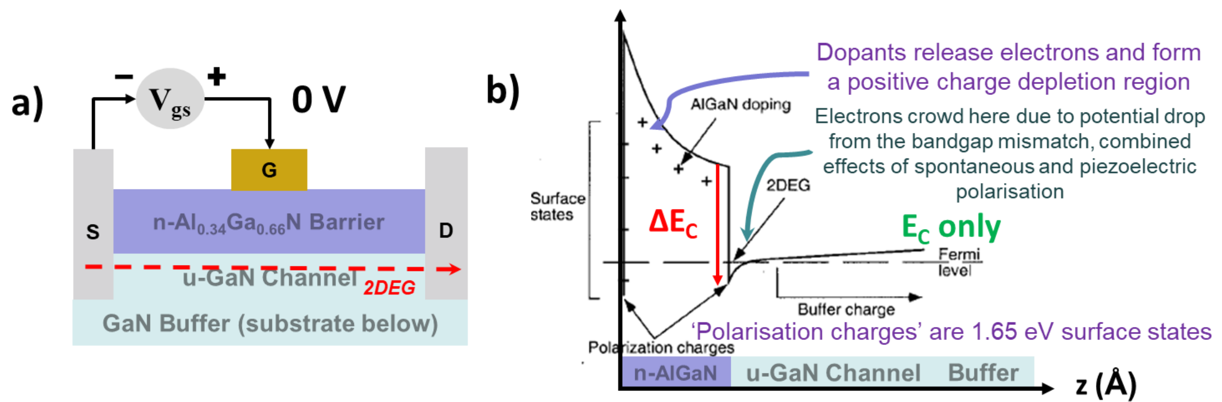

Figure 2.24: a) A HEMT structure both naturally polar and doped, and **b)** An illustration of the space charge distribution and Poisson band bending in a HEMT [26]. Labelled for clarity. Reprinted with permission from AIP Publishing.

Fundamental to understanding this charge depletion dynamic is understanding how the Poisson equation describes the charge/band relationship. The Poisson Equation takes the form as shown in Equation 2.17, after replacing the Laplace operator ∇ with real space in the z axis and adopting the charge derivative in a real semiconductor, the generalised form of [27]:

$$\partial^2\varphi / dz^2 = -\rho / \varepsilon_0\varepsilon_r \qquad (2.17)$$

Where φ is the potential (voltage), z is the growth axis, ρ the charge density, and, ε_0 and ε_r the permittivity of free space and the semiconductor respectively. What this says is that a localised or layer-wide charge density will induce a parabolic potential drop, thus giving rise to what is being referred to as 'Poisson-compliant band bending' in the confines of this Thesis. In a doped layer, this takes the form of Equation 2.18:

$$\partial^2\varphi / dz^2 = -eN_D / \varepsilon_0\varepsilon_r \qquad (2.18)$$

Where φ is the potential (voltage), z is the growth axis, N_D the donor concentration, e the electron charge, ε_0 and ε_r the permittivity of free space and the semiconductor respectively. Thus, we can find the new potential based on position such as Equation 2.19 [28]:

$$\varphi(z) = -eN_D / 2\varepsilon_0\varepsilon_r \, z^2 \qquad (2.19)$$

Polarisation can also be included within this Equation, since we know the spontaneous polarisation of GaN and AlN, with results such as this on Equation 2.20:

$$\varphi(z) = {}^{-eN_D}/_{2\varepsilon_0\varepsilon_r}\, z^2 + {}^{(P_{Total})}/_{2\varepsilon_0\varepsilon_r}\, z \tag{2.20}$$

Where P_{Total} is the total polarisation. Since spontaneous polarisation is constant and the total polarisation charge is dependent on the III-N layer's own composition, and its resultant potential is not parabolic but rather linear. The addition of a Schottky barrier introduces its own potential drop whose magnitude is dependent on the local donor density, and the Schottky barrier height [29]:

$$\varphi(z) = V_b[1 - {}^{z}/_{d}]^2 \tag{2.21}$$

Where d is the depletion length based on the local charge density and Vb the Schottky barrier. In a purely n-doped layer without polarisation this depletion length is defined as follows on Equation 2.22:

$$V_b = {}^{-eN_D}/_{2\varepsilon_0\varepsilon_r}\, d^2 \; therefore \; d = \sqrt{{}^{V_b 2\varepsilon_0\varepsilon_r}/_{-eN_D}} \tag{2.22}$$

This is to say that the self-consistent solutions revolve around parabolically restoring the 'ground-level' potential from the Schottky contact potential, reliant on the layer charge density to gradually deplete to the conduction band level of the layer.

Unlike homojunction devices, the dissimilar barrier material also reduces electron back-tunnelling – towards the metal contact as unlike with only doped regions, any tunnelling electron has to meet the conduction band difference between the barrier and GaN channel. In line with quantum mechanics principles, an electron wave function 'bleeds' into a barrier of finite height, thus having a non-zero probability of electrons being in there, leading to the phenomenon of tunnelling [30].

On a device level, since HEMTs consist of semiconductor slabs, Ohmic and Schottky contacts, this simplifies using a band diagram to explain HEMTs pinching off at negative voltages and operating in a default-ON mode. Figure 2.25 is one such illustration. Under no bias at all, the depletion from the Schottky contact is sufficiently small so that the Fermi Level cross-over does not happen within the barrier layer, but instead the conduction band discontinuity between the barrier and channel layers crosses over the Schottky metal-pinned Fermi Level. Under significant reverse bias, however, the quasi-Fermi levels indicate that electrons no longer crowd in the channel-barrier interface.

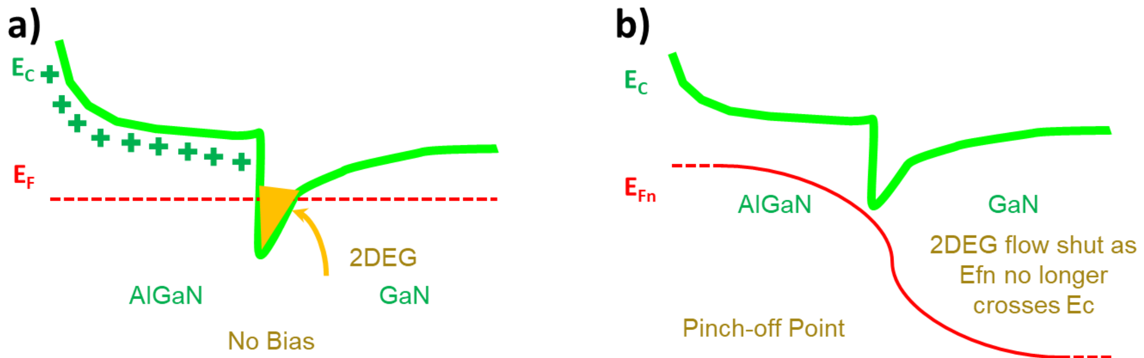

Figure 2.25: Illustration of HEMT conduction band **a)** under no bias and **b)** pinched-off at negative bias.

2.5: Conclusion

The various solid-state physics concepts relating to semiconductors have been explored, both generally and in specific relation to the III-N material family. The role that polarisation plays in the electrical characteristics of GaN and related compound semiconductors has been established, in that it generates a built-in electric field. Heterojunctions that make up HEMT and MQW LED devices have been explored, complete with their design philosophies and mechanics of operation. MQW structures enable multiple successive InGaN active regions in tandem with pn junction built-in potentials to generate visible light under forward bias, whilst ensuring that most photons leave the active regions since their energies will need to meet GaN bandgap for re-absorption. HEMTs employ electron confinement brought on by a combination of larger bandgap barriers and a main channel, surface states, and doping/polarisation to create a mostly-free sea of electrons which creates an on-by-default channel, and a Schottky contact to control this channel.

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Chapter 3 – Experimental Techniques

A number of advanced experimental techniques have been employed for the duration of the research project, for both device manufacturing and also their characterisation, as research demands compliant data and reliable devices to back up a hypothesis.

3.1: Fabrication and Other Device Processing

Once a sample wafer is grown, the defining features of a device need to be set through device processing in a way that will finalise the test structures. Here are a few of the methods used to manufacture these devices. Throughout the fabrication processes, it should be noted that nitrile gloves and tweezers are used for sample handling, especially for protection from dust. Acids require further layers of PPE to handle, including designated thick gloves, aprons, and specialist goggles.

3.1.1: UV Photolithography

Photolithography or other forms of lithography are necessary in order to set device sites, which, depending on the process number, allows developed photoresist to selectively permit or block certain sites from being affected during the process. UV photolithography has relatively higher throughput and lower complexity as compared to the more precise and maskless electron beam lithography (EBL) [1], so is the project’s lithography method of choice as the majority of the devices processed do not go below feature sizes of 1 µm. UV photolithography is undertaken in the dedicated ‘yellow room’ due to ambient short wavelength light sources potentially being able to prematurely make resists soluble, as they are sensitive to higher energy photons. [2]

Photoresist Coating Process via Spinner

Figure 3.1: Photoresist control unit on a chemical bench with resist phials, a timer, and a hotplate.

Figure 3.1 shows a photoresist spinner with its companion tools for photoresist coating of the sample after surface cleaning. Blue tack paper is first obtained to ensure that the sample is somewhat firmly adhered onto it before the resist coating process. The desired resist is then dripped onto the sample using the droppers. SPR350 (≈1.2 µm coating at 4000 rpm, easier to lift off and ideal for metallisation) and BPRS200 (2 µm coating at 4000 rpm, ideal for mesa etching) are the most commonly-used by the *GaN Centre*, and processes are usually set to be mainly reliant on positive photoresists – resists that, upon exposure and development, transfer the pattern on as process windows as the regions become more soluble. Negative photoresists, such as SU-8, are rarer and they leave their mirror image as process windows – exposure hardens them instead of softening [3-7] .

Next, the resist-coated sample is fixated on the chuck using the built-in vacuum pump by the tack paper end, using the switch as shown on Figure 3.2. The rate of spinning and any optional dwell times are set using the Spin Coater Model 4000, also on the same Figure, with instructions on how to alter the rate beside the device. The preferred spin rate is 4000 revolutions per minute, which ensures that the resist is spread as thinly and evenly as possible. Upon setting the spin conditions, the green button on the spinner (Figure 3.1) is pressed when ready. The process may either be manually terminated by pressing the red button, or awaited, which usually takes around 30 s to a minute. The tack paper is then removed, disposed of in the provided waste bin, and the sample is heated up on the hotplate at 100°C for 1 minute (with optional glass slides underneath) in a process of 'soft baking'. This helps the resist adhere to the sample better and form a more solidified layer [8].

Figure 3.2: Spinner revolution rate controls and vacuum pump switch.

If the photoresist seems to be fairly evenly coated and baked right, preferably without any air bubbles, then the sample is ready for the alignment and exposure process. If, however, it does not appear to be coated right, it could be removed on a solvents bench and coated again.

Photomasks and Mask Aligner

The next step in photolithography is to expose the photoresist to ultraviolet for a number of seconds specified for the photoresist and mask aligner combination. Before this step, though, the photomask needs to be cleaned with solvents, namely acetone (first, to remove residues of resist) and isopropyl alcohol (IPA, to clean up the mask generally and also wash away the acetone precursor), and doing it over a solvent waste container. The mask is then dried with an air gun. Cleansing the mask of residues and potential dust, even though they are kept in enclosed containers and a sterile environment afforded by the cleanroom, allows the features to be better transferred onto the sample.

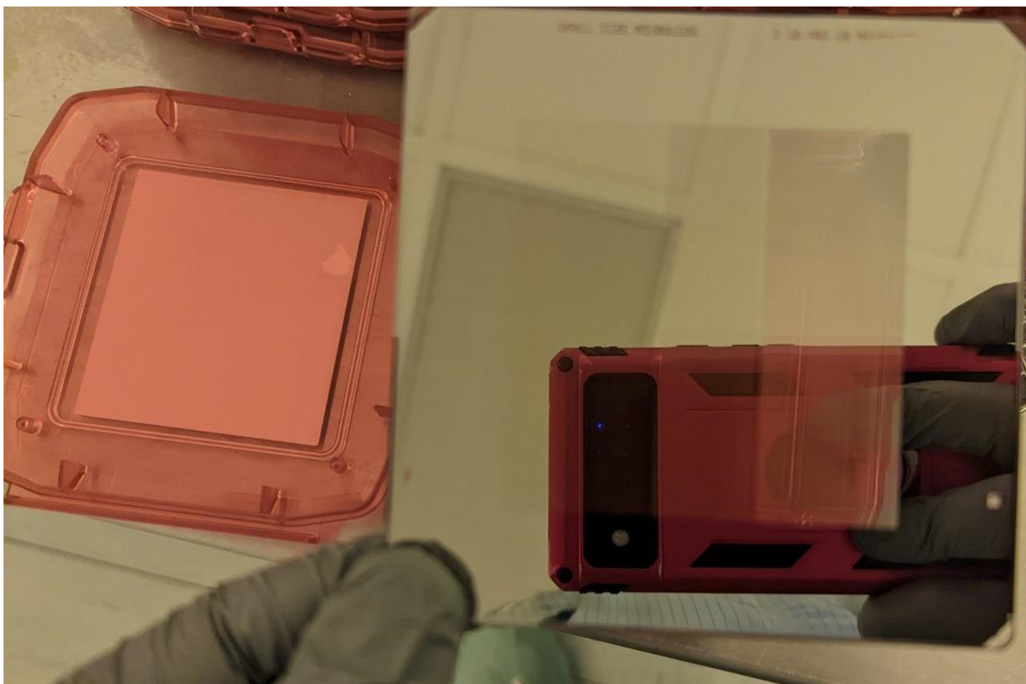

Figure 3.3: A chromium photomask that also reflects the smartphone that took the picture, and a mask case in the background. This is a ‘bright field’ variant, noticeable thanks to the mask tone itself and everything except the features being transparent in the active area. Care must be taken to not use camera flash while taking the picture, as it can potentially damage the mask.

The preferred material for photomasks is chromium, especially thanks to its reflective properties that allows it to be selective with light transfer upon exposure to light sources, as can be seen in Figure 3.3. Masks may have polarities that are either inverted or directly transferred, but out

of the ones employed within the scope of the project, it is mainly in mask tone that they differ from each other. As mentioned in the caption of Figure 3.3, ‘bright field’ masks exist, which are transparent in the active area and reflective in the areas where the device patterns are. This has uses in exposing everything except the pattern to UV, such as with device mesa etching, which requires the device sites to be elevated from the rest of the wafer to electrically isolate individual devices. ‘Dark field’ masks are the opposite; everything else is darkened and the mask has a notably darker colour tone, but the pattern itself is transparent. As a consequence, dark field masks are harder to align because only the pattern is see-through. Dark field masks have plenty of utility in, for example, Ohmic and Schottky contact deposition, because they ensure that only the metal pattern is transferred onto the photoresist. Ideally, the mask should have alignment and Vernier marks.

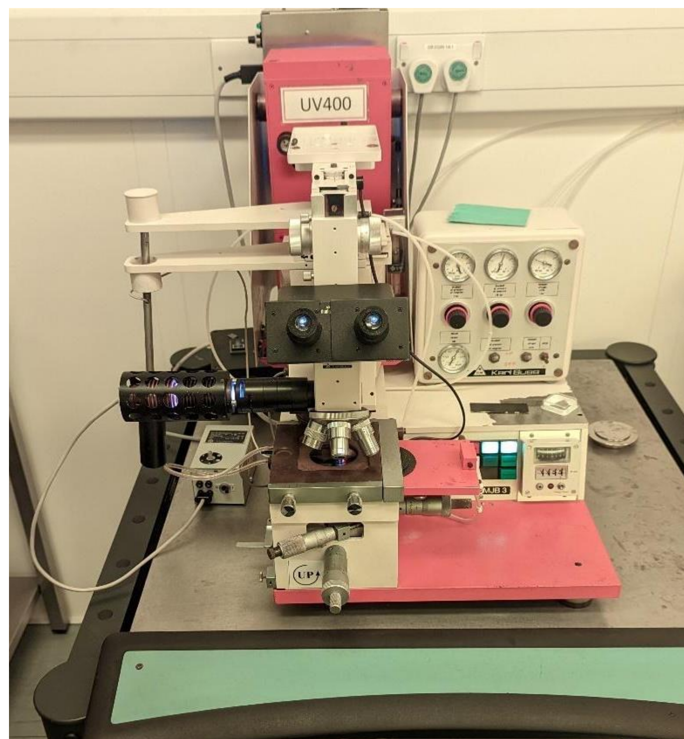

Figure 3.4: Karl Suss MJB3 mask aligner for ‘UV 400’; near-ultraviolet with visible bands.

Once the mask is ready, it may be mounted on the mask aligner shown in Figure 3.4 alongside the resist-coated sample, which has a designated stage that can be moved to coincide with the photomask pattern. The initial pattern may be cursorily set, but any subsequent marks need to be carefully aligned. A pump coolant system is in place for the microscope adjustment and also the UV power source. The mask needs to be mounted by using the built-in vacuum pump to ensure it remains in place during exposure; it is flipped to place on the mount as the top side of the mask needs to overlook the UV lamp. There is a slider for ‘separation’ and ‘contact’ positions for the sample stage, which represent the relative distancing between the mask and the sample, which is

initially positioned in the separation state, then gradually moved into the contact position. This is a potential source of mask contamination by resist, hence the cleaning step prior to processing. Ideally, there should still be a small separation at this stage, and the XYZ knobs as well as the sample pitch can be used to position the sample. UV exposure may commence.

Post-Exposure Development

Development is the final stage that solves away the soluble photoresist pattern, leaving behind process windows. MF26A is the preferred developer for the positive photoresists: it is employed as diluted 0.7 H_2O: 1 MF26A and undiluted MF26A for BPRS200 and SPR350 respectively. The exposed sample is dipped in the solution for 1 minute and 'stirred' around while gently grasped with a tweezer and dried with a filter paper and air gun. The end result may be seen under the microscope to ensure the resist pattern is transferred accurately. The end pattern and 'wave' structures may be used to gauge if the resist is overexposed or underexposed to UV.

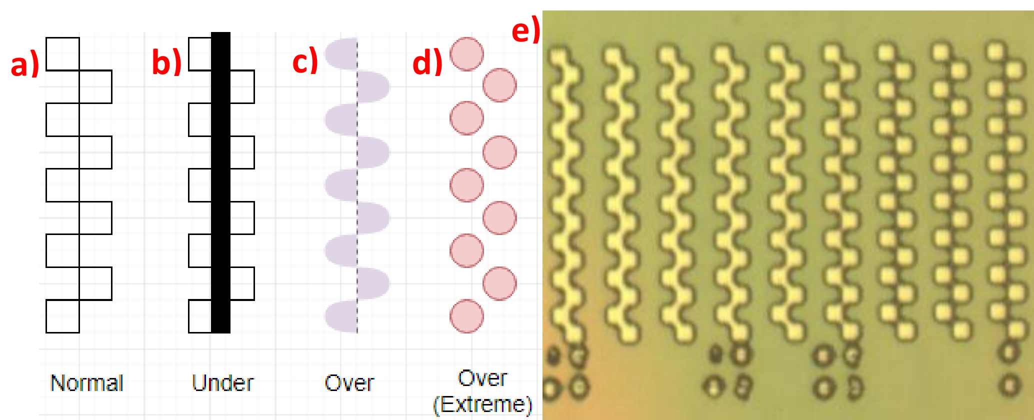

Figure 3.5: Illustration of expected exposure marks across an entire wave mini-structure with a) to d) being conceptually: **a)** Correct exposure length transferring pattern well; **b)** Underexposure with a thick middle line indicating not enough resist solubility; **c)** Mild overexposure making the resist too soluble; **d)** Excessive overexposure breaking pattern and **e)** Practical microscope image example: Slight overexposure showing mostly correct pattern transfer and occasional dotted patterns.

3.1.2: Dry Etching: ICP and RIE

There are a couple of dry etching techniques employed, as dry etching, unlike wet chemical etching, is not inherently isotropic (omnidirectional) and depending on the power conditions and the masking process, is ideal for selective etching of devices and determination of sharp device features. The high chemical stability of III-Nitrides as mentioned in Chapter 1 also demands physical etching.

Reactive Ion Etching (RIE)

Reactive Ion Etching is a dry etching method that relies on etchant gases in a chamber to achieve dry, highly directional etching, with a single parallel-electrode RF power generator that drives an ion bombardment plasma inside the etching chamber by operating at voltages that break down the said gases [9]. Commonly used gases include SF_6, CHF_3, O_2, and Ar.

The RIE setup used is a JLS Design Plasma Technology system, which has an enclosed glove box which in turn has the reaction chamber within and behaves as a secondary parallel-plate ground electrode. The set flow rates of each constituent gas of the etching process are controlled by inlet valves, and the appropriate RF power rating of each recipe is manually set.

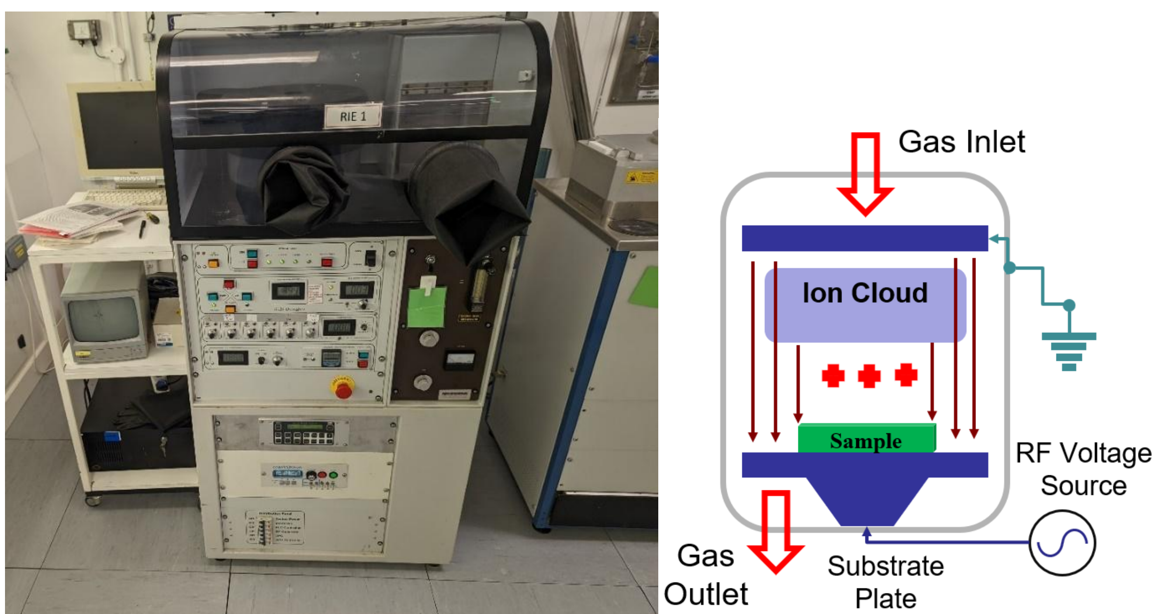

Figure 3.6: a) The RIE setup; **b)** An illustration of the mechanics of operation.

RIE is commonly used as a method to remove passivation layers as well, usually Si_3N_4 or SiO_2, in combinations of CHF_3/SF_6 and CHF_3/O_2 in flow rates of 30/10 and 35/5 respectively.

Inductively Coupled Plasma (ICP) Etching

ICP, or Inductively Coupled Plasma(-enhanced) Reactive Ion Etching (ICP-RIE), is a variant of RIE that uses an induction subsystem which forms the etchant gases into a reactive ion plasma, which gives the method its name. Then, a secondary parallel electrode voltage drives an electric field that directs the said plasma into an etchant beam. In semiconductor processing, ICP is used for selective etching alongside photolithography, or when an ICP-resistant mask layer is already in place. It is preferred to be used when a metal contact has not been deposited yet, as metal contacts may sputter in the ICP chamber and contaminate it. To that end, the RIE setup above is usually used.

An implication of this secondary electromagnetic field source is that higher plasma density with powerful and anisotropic (directional) ionic etching can be achieved as compared to RIE GaN, for example, uses either SF_6/N_2 [10], or a combination of Cl_2 and Ar at a 45/12 sccm flow rate ratio and 50 W etching power for an etch rate of ≈ 110 nm/min [6]. A 450 W ICP power rate is maintained for the plasma density, however. Setting the RF power to a high enough value to allow quick etching but low enough value for minimal ICP damages is of key importance. ICP is long-lauded as a method for keeping etchant ions from colliding with one another or neutral ions, even more so than RIE. [11-13]

The ICP setup used is an Oxford Instruments Plasmalab System 100. An on-site monitoring system with laser interferometry is used to control the process and monitor the etch rates. For example, with a 'standard' HEMT epi-wafer (20 nm barrier, 1 nm spacer, 25 nm HT-GaN), at least 50 nm of semiconductor should be etched to get down to the buffer, but to provide enhanced inter-device mesa isolation, deeper etching still may be performed subject to user's discretion.

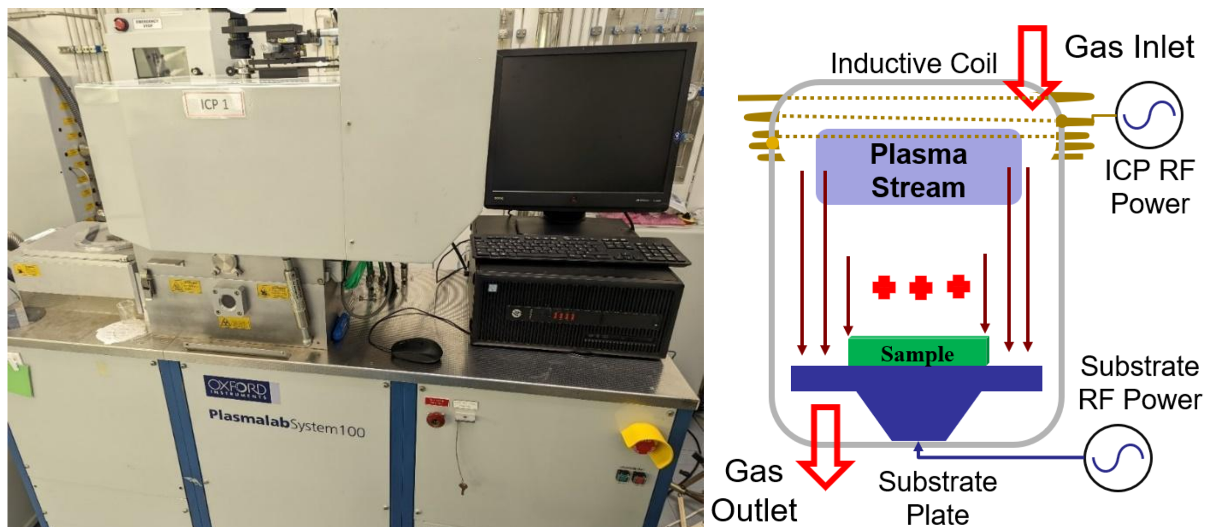

Figure 3.7: a) The ICP-RIE setup supplied by Oxford Instruments. **b)** Operation principles.

3.1.3: Semiconductor Film, Metal Contact, and Insulator Oxide Deposition

Plasma-Enhanced Chemical Vapour Deposition (PECVD)

PECVD is a valuable tool for deposition of overgrown layers through a solid mask window, but especially of dielectric materials, particularly SiO_2 and Si_3N_4. PECVD uses an RF signal large voltage-driven ion plasma to significantly lower the deposition temperature of the constituent gaseous ingredients, and a gas outlet to extract the by-products via an interconnected vent system. Similar in scope to ICP, it could be thought of as the reverse process. PECVD has the large advantage of requiring a far lower temperature (≈ 300°C) for good deposition rates as compared to

conventional CVD methods, and has the dual advantage of higher quality, faster deposited films with very little to no dependence on substrate and specific growth conditions [14].

Common precursor gases used are SiH_4 and N_2, while NH_3 and N_2O are reactant gases for Si_3N_4 and SiO_2 respectively. The idea behind CVD assembly is that precursor gases are inlet, adhere themselves onto the heated substrate and combine with the plasma-enhanced reactant gases, thus starting a chain reaction of epitaxial assembly, a precise layer-by-layer deposition process.

The PECVD apparatus provided to the researcher is a PlasmaTherm 790 Series system, remote controlled via a computer.

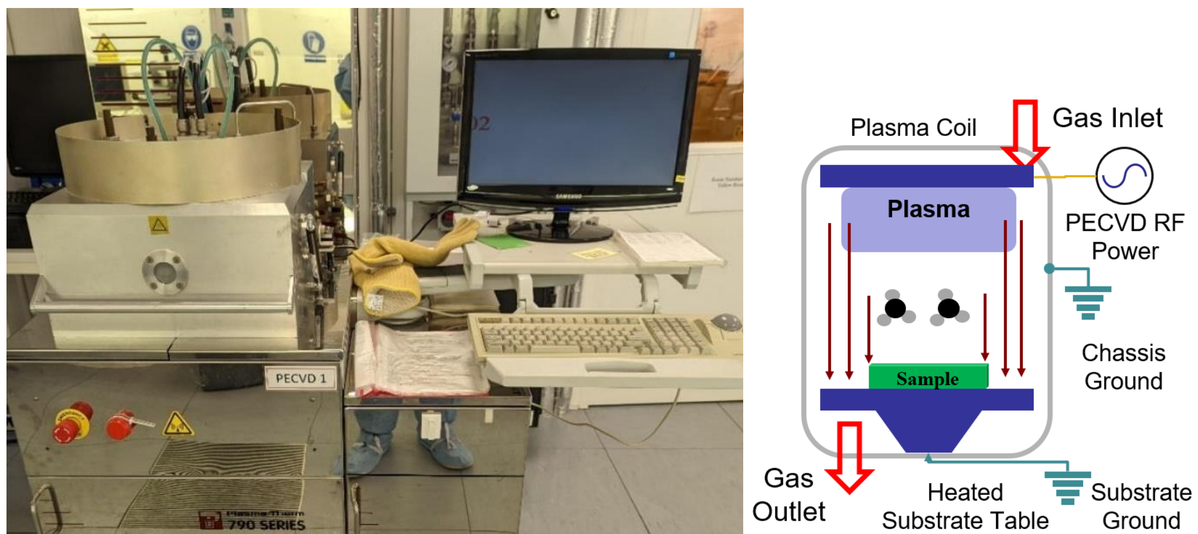

Figure 3.8: a) The PlasmaTherm PECVD setup used. **b)** Operation principles.

Physical Vapour Deposition

Metal filaments are subjected to resistive heating, through the use of tungsten coils to hold the metals. Tungsten can be subjected to the high currents (up to 40 A) passed through it which will melt the mounted metal filaments, with the metal itself being largely unaffected by the process. The evaporators are vacuumed, as the vacuum conditions allow lower temperature melting. It should also be noted that while the diffusion pump is on, the system should be filled with liquid nitrogen (LN_2) at least every 1.5 hours, as it relies on an oil hydraulics system for the ventilation valves that should never be left to overheat, lest apparatus failures occur.

Figure 3.9: A box of tungsten coils designated for different metal wires.

Samples are loaded by first letting the diffusion pump start up for at least 20 minutes, then turning the baffle valve off into backing position via the rotary pump and enabling air admission. It will reach atmospheric pressure in about a minute, at which point the user may carefully remove the bell jar and implosion guard. The sample(s) and coils with their constituent metals are put in place and the system re-vacuumed to less than 3×10^{-1} mbar on the Pirani gauge by turning off air admission and opening the roughing valve, then the backing valve again. An hour and a half of vacuuming should bring the pressure to less than 6×10^{-6} mbar. At this point, ensuring the LN_2 supply is adequate, the deposition may begin.

Figure 3.10: An Edwards E306A Thermal Evaporator and its bell jar, with a crystal monitor. A separate cylindrical implosion jar is also used.

The crystal monitor is used to gauge how many nanometres of a selected metal is deposited through the use of density data and acoustic impedance constants, which is how, for example, in Ti/Al/Ni/Au Ohmic contacts for example, precise thicknesses such as 20/120/20/80 nm are able to be given. Then a variac is used to pass varying amounts of current through the fixated coils by selecting the slot they are located in. Higher melting point metals such as Ti and Ni should be up top, kept further away from the sample. A shutter is used to control the flow of evaporated metals. A cooldown and unload procedure concludes the evaporation procedure.

3.1.4: Rapid Thermal Annealing (RTA), Resist Oxygen Ashing Process, and Miscellaneous Processing

Rapid Thermal Annealing (RTA)

Thermal annealing has been discussed earlier as a useful method of activating p-type Mg doping, for example for p-type contact activation for an LED as it enables breaking up of Mg-H complexes [15], and also as an activation method for Ti/Al/Ni/Au Ohmic contacts by enabling Ti_xN complexes to form as surface states for GaN/AlGaN [16], which give the negative or small Schottky barrier necessary. The RTA setup allows for settings of quick 30 s to 1 min activation times at 850°C at nitrogen ambient or other background gases, or of longer, low temperature activation.

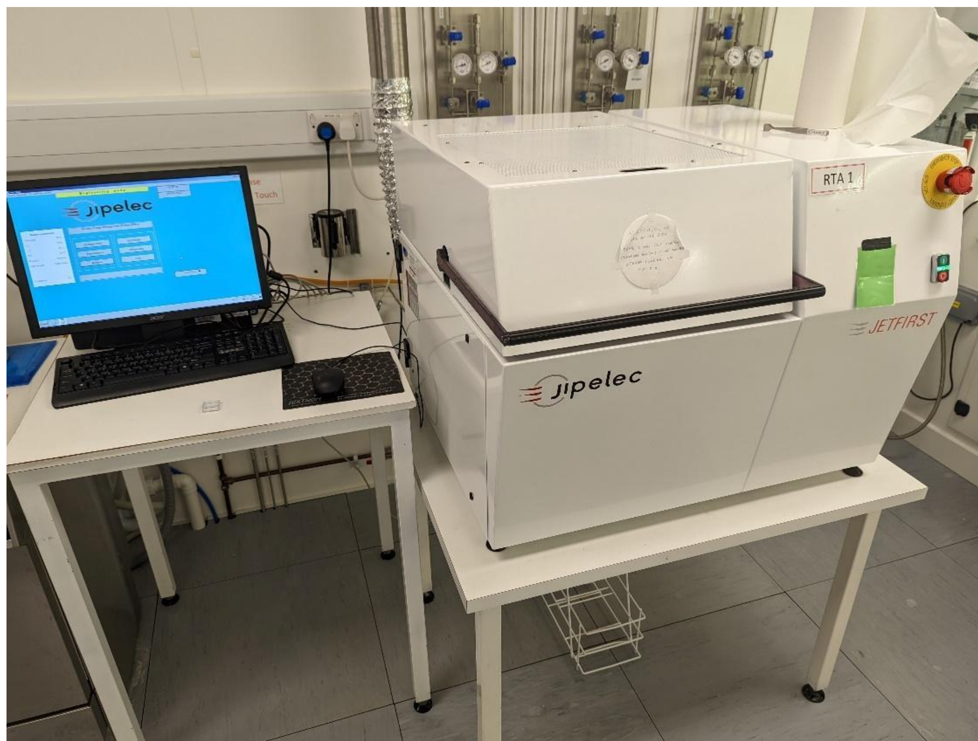

Figure 3.11: The Rapid Thermal Annealer in the Nanosciences cleanroom.

The Jipelec Jetfirst is set up by the technical team for quick use with a computer, where recipes can be loaded for different annealing conditions subject to the user's process requirements.

Resist Asher

The use of an oxygen plasma asher is useful for removing excess photoresist, 'smoothing out' of 'correctly' deposited photoresist and longer ashing processes can oftentimes even help remove overbaked resists. It is largely non-destructive to III-N semiconductor epi-wafers.

The resist asher used is a Polaron PT7150 RF plasma barrel etcher, with individual controls for the RF power, gas release valves and standby/vent buttons. The sample is loaded into the chamber with the help of glass slides and gas releases controlled. Care should be taken during operation to ensure the reflected power does not exceed 20 W. Application times could be as short as a few seconds for resist feature clean-up and up to several minutes for complete clean-up.

Figure 3.12: a) The resist asher. **b)** Microscope system to view samples

Chemical Processing in Brief

Chemical benches with fume cupboards are instrumental to sample surface cleaning, resist removal, development, and metal lift-off post-deposition. There are designated acid, solvent, and resist development chemical benches.

For example: surface cleaning may simply be done by dipping the sample in a solvent, but the preferred procedure is the use of n-butyl acetate placed on a hotplate, followed by ultrasonic

bath treatment in acetone and IPA to remove any of the residues of the two. Metal lift-off with properly coated resist is achieved by placing the sample in one of the solvents, usually acetone, and 'spraying' some of the solvent on the sample with a pipette, as metal that actually adheres to the semiconductor firmly remains in place. Acids such as HF are often used to remove passivation layers and for destructive etching when other methods fail, but the use of it is limited to a select group of authorised personnel because of its excessive reactivity. Aqua regia dissolves gold contacts.

Figure 3.13: A chemical bench for solvents also equipped with a hotplate.

3.2: Device Characterisation

There have been largely non-destructive methods that have been applied, as logistically the unfabricated wafer pieces involved may have to be used multiple times, as well as there being little benefit in using the more destructive characterisation methods.

3.2.1: Crystallographic Characterisation

X-ray Diffractometer (XRD)

X-ray diffractometry is an excellent way of obtaining crystallographic information about a sample without damaging it, such as crystal qualities along different axes and the implied different types of dislocation densities from Rocking Curves, getting the composition of a semiconductor alloy involved in the end form of a sample by taking the given curve spacing into account, and the implied strain information.

Figure 3.14: The Bruker D8 Discover XRD apparatus [17]. © 2022 Bruker.

The XRD equipment used for the measurements is a Bruker D8 Discover family system, with a computer for remote testing. It has a vacuum pump system to fixate the sample in place while rotating the sample along the azimuth angles, yaw (ϕ), roll (ψ) and pitch (ω) necessary for varying incident angle behaviour with (θ) as the ray path. The measurements entail using the angles of (ω) and (θ) as a stand-in for incidence and reflection deviation, and setting a sweep to pick up a beam.

It comes complete with its Diffraction Suite software package, including Commander and Leptos for instrument control, execution of sweep setups, real-time monitoring and transferring measurements into a spreadsheet processing software-editable format respectively, and its Wizard module can calculate and transfer to Commander ω/θ values for materials, like with GaN indices for (0001)/ '(002) GaN' [17].

3.2.2: Electrical Characterisation

Source Measure Unit (SMU) and Probe Station Setup

An SMU is instrumental to the electrical characterisation performed for research purposes as it provides much greater precision than a multimeter or a dedicated ammeter, and is less susceptible to fluctuations in output voltage than a regular wall-mounted power supply unit, and moreover, has the flexibility to be configured for both a current and a voltage source, and to measure any of the Ohmic quantities. In addition, it eliminates manual sweeps and data recording.

Figure 3.15: a) SMU front panel. **b)** Microscope stage with Karl Suss probe micropositioners.

The SMU used for I-V and resistance measurements is a Keithley 2612B device, complete with its companion program KickStart for remote testing and data logging. The program allows for setting of multiple parameters (start voltage, end voltage, step voltage, current limit, waveform delay, number of power line cycles (NPLC) per measurement etc) and sweep types (stepper for two voltage source sweeps with one being kept at a value while the other runs, useful for HEMT I-V curves while stepping V_{GS}; voltage sweep for one or two sources simultaneously, plain voltage bias, pulsed voltage), for each channel, with the option for measuring current, resistance, programmed or output voltage, timestamp, or trigger/output capacitance settings. KickStart allows these results to be output in either a comma-separated values or Excel sheet format.

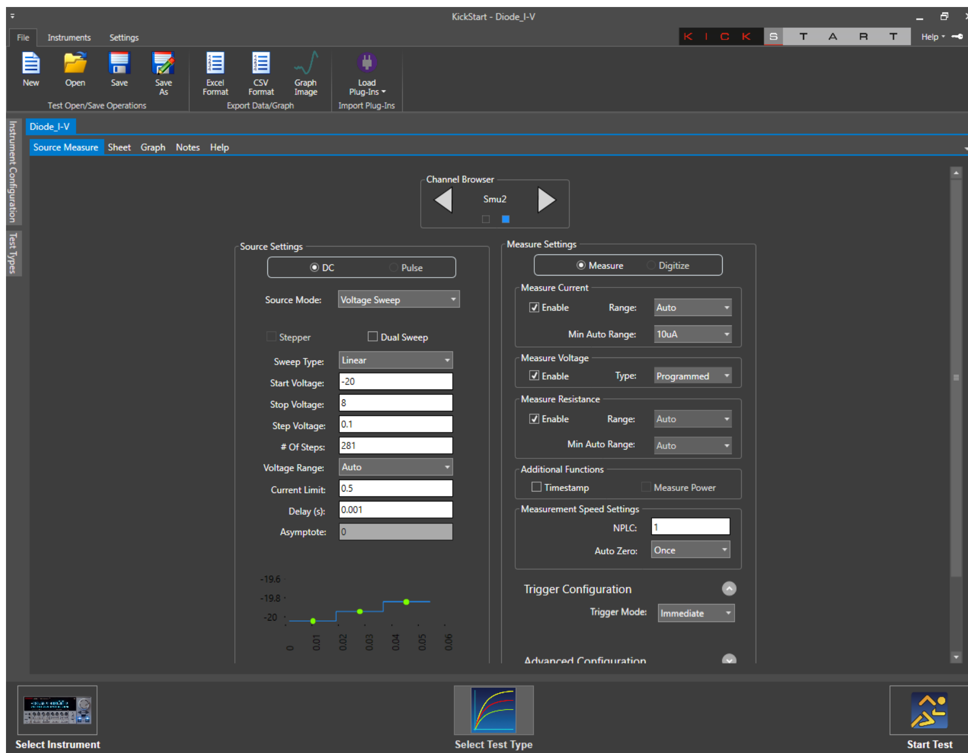

Figure 3.16: KickStart operation menu.

Inductance-Capacitance-Resistance (LCR) Meter

An LCR meter is necessary for capacitance-voltage measurements, which are critical to estimating doping concentrations and obtaining other critical information about a device, such as the negative capacitance characteristics seen with micro-LEDs. They may also be configured to measure, for example, impedance real/reactive components and their phase angle.

The LCR meter in question is a Keysight E4980A device, capable of obtaining measurements for applications of small signals between 20 Hz and 2 MHz, and also complete with a purely-DC output. However, since the 2612B is more accurate and precise for DC measurements, the E4980 is mainly used for AC small signals. Its parameters include parallel equivalent circuit-model capacitance (Cp), series model (Cs), series resistance (Rs) and many more.

Figure 3.17: The Keysight E4980 LCR meter main menu.

Doping estimations via C-V measurements are inexpensive compared to secondary ion mass spectroscopy to operate, as the main costs are from the setup of the equipment itself, and also non-destructive [18]. While especially with Schottky contacts, gate metal/depletion region charge trapping is likely to interfere with the results for both charge carrier density and implied dielectric constant calculations [19], thus making Hall Effect testing more accurate for high-doping or high charge carrier samples, such as the case with fully-polar unintentionally-doped structures, C-V measurements are more reliable with lower, nearly-intrinsic doping concentrations, since the absolute capacitance (subject to instrument precision and device innate noise) can still be integrated (Equation 5.1) to show the results, while Hall measurements are likely to be affected by innate carrier/magnetic/thermal noise, minority carriers and limited by the high resistivity of low-doped semiconductors, which is when the method should theoretically be the strongest but it does not translate into practice [20]. So, epitaxial structure and fabrication time permitting, both methods are used for charge carrier concentrations where appropriate.

Hall Effect Sensor Based on van der Pauw Principles

A Hall Effect sensor has been employed with a four-metal leaf arrangement in order to perform electromagnetic characterisation on semiconductor wafers, especially those with inherent polarisation or intentional doping. Hall Effect sensors are excellent for sheet carrier density, sheet resistivity, and electron mobility measurements, especially when the doping involved is substantial and not at nearly-unintentional or intrinsic levels, and may even be configured for hole mobility.

The sample to be tested on is mounted onto the supplied printed circuit boards (PCB), which are then loaded into the Ecopia MP55 0.56 T magnetic chamber which has a slider for N ⍰ S and S ⍰

N magnetic field directions and a small liquid nitrogen (LN_2) receiver compartment for 77 K measurements rather than 300 K room temperature measurements. Beside the equipment is a wire 'black box' for 4-pin measurements, with both the current and the voltage supply being given out via two Keithley 2400 series SMUs. Once the PCB has been mounted onto the socket, the measurements may be performed as instructed by the pre-made macro spreadsheet for data recording and transfer. As per van der Pauw principles, first, the horizontal measurements are performed, then the vertical ones, then cross-over magnetic field voltages give Hall coefficients.

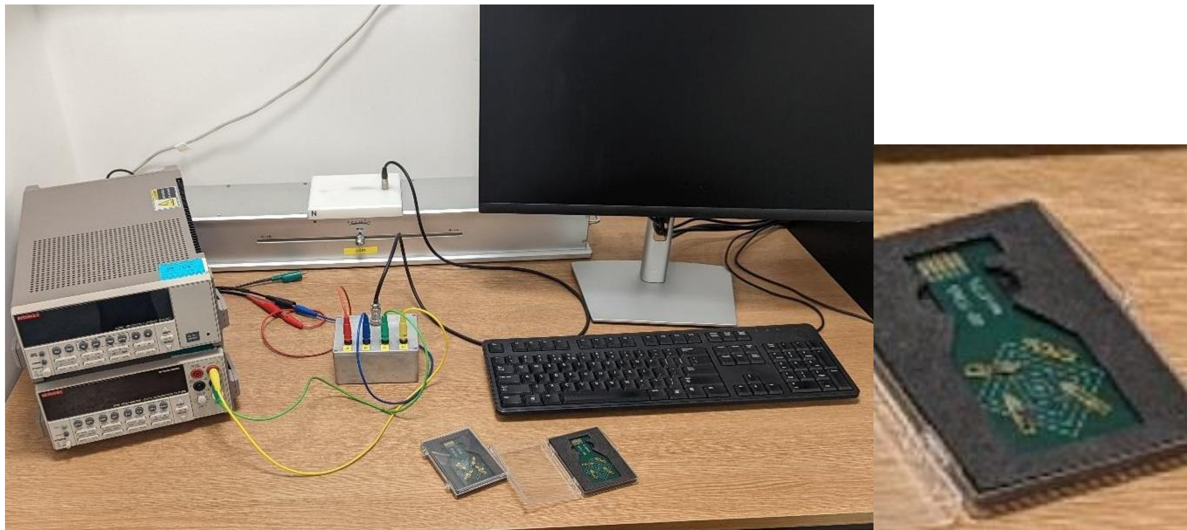

Figure 3.18: The Hall Effect setup with a computer, a 0.56 T magnetic chamber and SMUs with a zoomed-in view of one of the PCBs.

One note to add is that LN_2 is handled similarly to how it is with the thermal evaporators; using PPE, a thermal insulator container is used to decant the LN_2 from a de-pressurised dewar by carefully tipping it over, as the LN_2 is normally processed and stored in pressurised cooling systems and needs in turn to be poured into one for individual researcher use at atmospheric pressure; a step that is oftentimes performed by the technical team and supplied to the laboratories. Then a 77K rated funnel or a secondary thermal flask is used to decant this LN_2 again and pour it more precisely into the magnetic chamber receiver.

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Chapter 4 – Electrical characterisation of Micro-LEDs

A systematic study has been performed on three different µLED size templates based on InGaN/AlGaN/GaN p-n heterojunctions; with µLED sizes of 40, 5 and 3.6 µm respectively. Our application of the principles of direct epitaxial overgrowth through the use of MOVPE has presented itself with tangible benefits to micro-LED array performance, including a smooth negative capacitance curve expected of such devices instead of unusual capacitance performances, and a large reduction of size-dependent inefficiency presented by the aforementioned ICP etching sidewall damage issue, which has been the subject of discussion for many micro-LED studies prior to it. Electrical characterisation performed on the selectively grown µLEDs as well as conventionally-fabricated µLEDs reveals that the overgrown µLEDs suffer from smaller leakage per µLED, exhibiting leakage currents as low as 14.1 nA per LED at a bias of - 5 V. Moreover, the overgrown µLEDs exhibit much smaller and more consistent leakages than their mesa-etched counterparts. Operational voltage RC constants also greatly favour overgrown µLEDs over the conventionally fabricated mesa-etched µLEDs.

4.1: Introduction

Micro-light-emitting diodes (µLEDs), with a size of a few or tens of micrometres, are attracting extensive attention within optoelectronics research and industry, due to a wide array of applications, such as micro-displays and augmented reality and visual reality (AR and VR). [1 – 4] Current µLEDs are typically electrically driven by existing silicon-based complementary metal oxide semiconductor (CMOS) electronics. [5] Likewise, they also address maximum driving current density (in kA cm^{-2}) issues faced with conventional broad-area LEDs. [6]

It is expected that the usually quick response time of µLEDs (determined by the so-called RC constant of the junction capacitance of a µLED) is favourable to achieving a high modulation bandwidth for visible light communication (VLC), which, in turn, allows for physical end-to-end secure connection without resorting to encryption unlike radio frequency (RF) and microwave transmissions that may be intercepted. The theoretical cutoff frequency for a µLED used as a transmitter is dependent on the RC constant of its junction capacitance, which is defined as follows:

$$f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi R(A\varepsilon_0\varepsilon_r/L)};$$
$$\varepsilon_0 = 8.85 \times 10^{-12}\ \mathrm{F\,m^{-1}} \tag{4.1}$$

where ε_0 and ε_r are free space permittivity and relative permittivity of a semiconductor which is used to fabricated into a µLED, respectively; A is the area of a µLED; and L is the length of the junction

capacitance of the LED. A smaller RC leads to a higher frequency. Regular white LEDs coated with yellow phosphors are usually limited to a dozen Mbps, while it is expected that µLED can reach a GHz level.[7 – 11]

III-nitrides are excellent candidates for developing µLEDs as key components for microdisplays, due to their wide direct bandgap of 3.4 eV for GaN and tuneable emission wavelengths for visible light. Compared with LCDs and OLEDs, III-nitride based µLEDs benefit the display technology in many ways: better contrast ratio, wider operating temperature, higher brightness and stability, wider view angles, and better colour precision. [4] Moreover, III-nitrides permit high electrical breakdown fields, which can attain high driving current densities for µLEDs. [12 – 13] Due to high intrinsic electron mobility of around 1000 $cm^2V^1 s^1$ and high electron saturation velocity of $2.5 \times 10^7 ms^{-1}$ for GaN, further enhanced by AlGaN/GaN heterostructures, GaN is held in high regard in power electronics, and III-nitride based µLEDs allow for quick response time, high maximum current, and high-frequency operation thanks to this high intrinsic mobility, the latter of which is already a subject of interest for power devices with high electron mobility transistors (HEMTs) going up to 300GHz.[14 – 16]

So far, loads of the work on GaN-based µLEDs have been reported, but their fabrication is limited to conventional dry etching approaches using inductively coupled plasma (ICP) or reactive ion etching (RIE) tools. [17 – 24] However, dry-etching tends to generate severe damages on the devices, leading to a significant reduction in both optical and electrical. Furthermore, such damages become more severe with reducing the dimension of µLEDs, [17] which is why small µLEDs, in particular, with a size of µLEDs below ≤5 µm, exhibits extremely low performance. This can be attributed to Shockley–Read–Hall recombination, implying a drop in external quantum efficiency (EQE) as electron–hole pairs recombine in trapping sites and cause phonons. In turn, this can be explained by an increase in damaged zone proportion and surface states per unit. Such trapping sites enable tunnelling for recombination and leakage too, exacerbating the problems.[18, 19] So far, a few methods have been attempted for removing the sidewall damage induced by the dry-etching, such as neutral beam etching and KOH chemical treatment. [25, 26] Though they have demonstrated to be effective in mitigating the etching damage, the etching approach to fabrication of µLEDs still requires a sidewall passivation and isolation, which can bring about extra processing and performance issues as well. [20, 21]

Recently, we have developed a different approach to fabrication of InGaN/GaN multi-quantum wells (MQWs) µLEDs: a selective overgrowth on patterned templates instead of mesa-etching. The green µLEDs have demonstrated high external quantum efficiency and high

luminescence. [3, 25] We have also grown InGaN-based HEMT–µLEDs to take advantage of higher driving current densities expected of µLEDs for VLC. [7] In this work, current–voltage and capacitance–voltage characteristics have been investigated systematically on the overgrown µLEDs with different sizes, which have also been compared with those µLEDs fabricated by means of using a conventionally dry-etching approach.

4.2: Structure description of Micro-LED Arrays

Figure 4a is a schematic drawing, showing our approach to achieving InGaN/GaN MQW µLED arrays. First, a microhole array pattern is formed on a n-type GaN layer on a sapphire substrate with a silicon dioxide (SiO2) mask, which is called an "n-GaN template." To fabricate the n-GaN template, a 500 nm-thick AlN buffer layer is first grown on a c-plane (0001) sapphire substrate via metalorganic chemical vapor deposition (MOCVD), followed by a GaN layer and n-doped GaN layer. A 500 nm SiO2 film is deposited on the template using a standard plasma-enhanced chemical vapor deposition (PECVD) technique. Afterward, a standard photolithography and subsequent dry-etching techniques are used to selectively etch the dielectric layer down to the n-GaN surface, forming regularly arrayed microholes.

Next, a standard LED structure is grown on the n-GaN template by MOCVD, namely, a silicon-doped n-GaN layer with a dopant concentration of 5×10^{18} cm^{-3} is initially grown, followed by an InGaN based prelayer (5% indium content), five periods of InGaN/GaN MQWs with 2.5 nm InGaN quantum wells and 13.5 nm GaN barriers as an active region, then a 20 nm p-type $Al_{0.2}Ga_{0.8}N$ blocking layer, and finally a 170 nm p-type doped GaN layer. Due to the dielectric masks, the LED structure can be grown only within the microholes, naturally forming arrays of isolated µLEDs. It means that the dimension, the interpitch, the individual location, and the shape of µLEDs are fully controlled. It is worth mentioning that isolation of the sidewalls is not necessary during the fabrication processing. The benefits of this dielectric SiO_2 mask are twofold; not only eliminating the aforementioned necessity of mesa etching, but also providing insulation for each µLED. Figure 1b is a top-view scanning electron microscope (SEM) image of our overgrown µLED arrays.

For this kind of µLED array sample, all the µLEDs share a common n-type contact, and all the p-type contacts are left open which can be used in the future as indium bumps bonded to driving transistors based on a silicon CMOS IC for manufacturing a microdisplay. In this work, the arrayed µLEDs are fabricated into a 330 µm × 330 µm device with an area of around 0.1mm2. The indium tin oxide is deposited as a common p-type contact for all the µLED pixels in one device and rapidly thermally annealed at 600°C for 1 min. The n-type metal Ti/Al/Ni/Au is deposited as Ohmic n-contacts.

Each device also has an additional Ti/Au metal layer on top of both n-contact and p-contact as their actual electrodes. Thus, the µLEDs in one device are electronically connected in parallel.

Figure 4.1 a) shows the scheme and structure of the overgrown LEDs in question; Figure 4.1 b) is the SEM image of the 5 µm diameter, 3 µm inter-pitch variants; and their companion figures Figure 4.1 c) and d), identical to Figure 1.12 a) and b), shows how it is different from the traditional mesa-etching method.

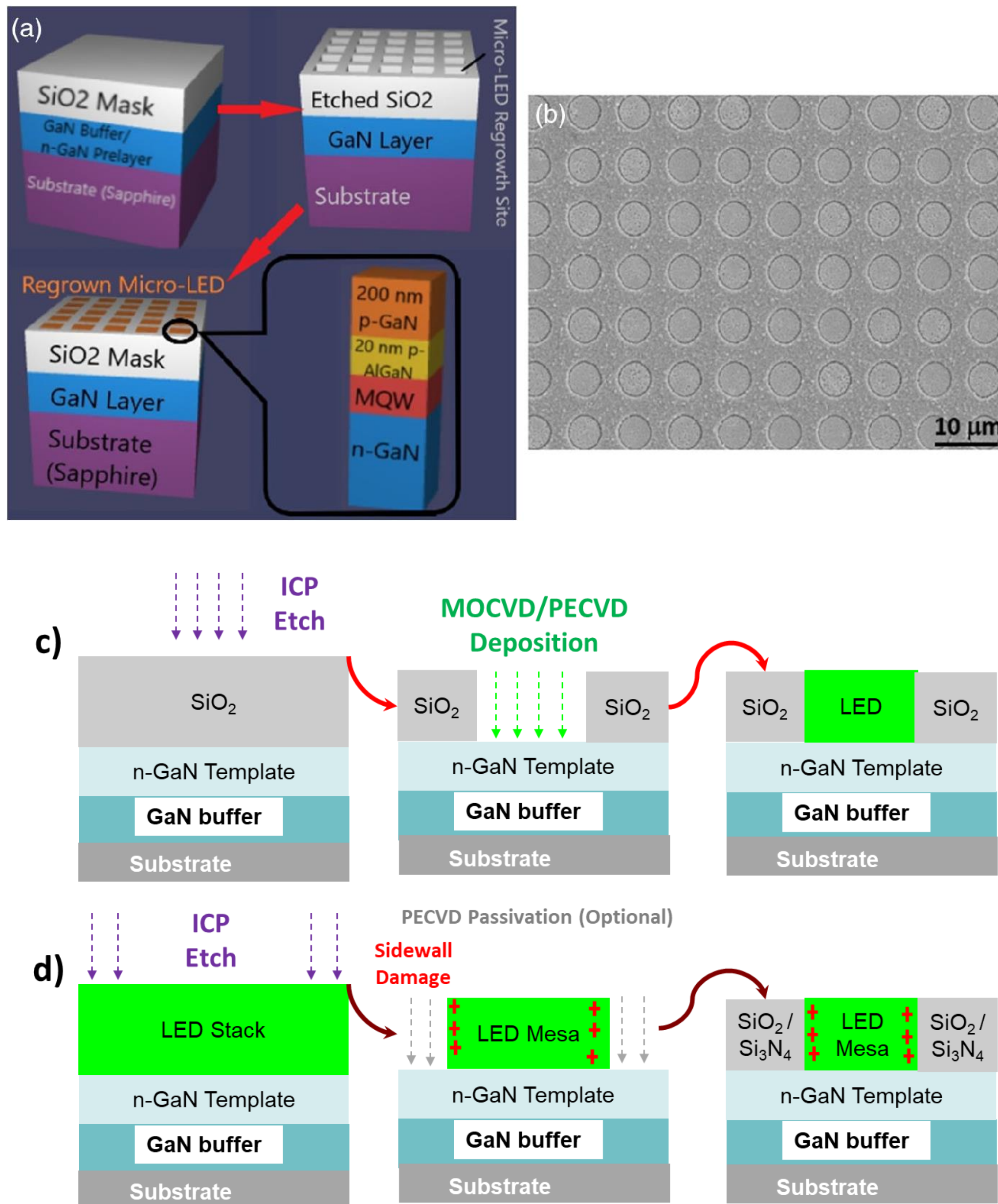

Figure 4.1: a) Scheme and structure of our overgrown LEDs; **b)** an SEM image of a 5 µm LED array sample; **c)** illustration of the overgrowth method; and **d)** the traditional mesa-etching method.

The overgrowth method uses an n-GaN template on which the aforementioned 500 nm thick layer of SiO_2 is deposited, and micro-patterns are etched on the SiO_2 mask, which provides a pattern for the LED structures to be grown, which was proposed with the intention of eliminating the sidewall damage directly etching to create an LED structure would. In contrast, the traditional fabrication method is done by having an LED structure grown as a full wafer, then etched out to create mesas of LEDs isolated from one another. Then, optionally, an extra layer of SiO_2 or Si_3N_4 is deposited as a passivation layer.

4.3: Micro-LED Characterisation

Voltage–current–resistance characteristics have been performed using a Keithley 2612B source meter unit (SMU), with a PC connection for the Tektronix-endorsed KickStart remote-testing and data extraction software package, and a probe station with an optical microscope. Current–voltage (I–V) characteristics are the most intuitive and down-to-integrated-circuit way of analysing devices. The devices were measured between -5 and 6 V. These were repeated for tens of devices throughout each sample to ensure consistency in results.

Capacitance–voltage (C–V) characteristics have been conducted by using a Keysight E4980A LCR (inductance–capacitance–resistance) meter, which has been calibrated for an open-circuit prior to measurements as a correction value. These were performed at 1 MHz which is deemed to be a high enough benchmark for small-signal frequency of operation to minimalize and normalize reactance (capacitive impedance) and determine the capacitance of the device accordingly. Capacitance data included here exclusively consists of the parallel equivalent circuit model (Cp), for the clear-cut reason of the devices themselves being in parallel. It is on a tuning scale of voltage bias from -5 to 6 V. The four or five smallest leakage arrays from each sample have been utilised as a baseline.

4.4: Results and Discussion

A set of epitaxy-overgrown µLED array samples with different sizes are used in this work, namely, a 3.6 µm diameter with an interpitch of 2 µm, a 5 µm diameter with a 3 µm interpitch, and a 40 µm diameter with a 10 µm interpitch, respectively. Figure 4.2 shows electroluminescence (EL) spectra of a 3.6 µm µLED array device at different current densities. The inset is a photo image of emitted µLEDs under 3 A cm^{-2} current density taken with 50 × magnification. It shows uniform green luminous intensities. Electrical properties have been investigated on the µLED array devices through I–V and C–V measurements and have also been compared with single µLEDs with a diameter of 10 or 40 µm, which have been fabricated by a conventional dry-etching approach.

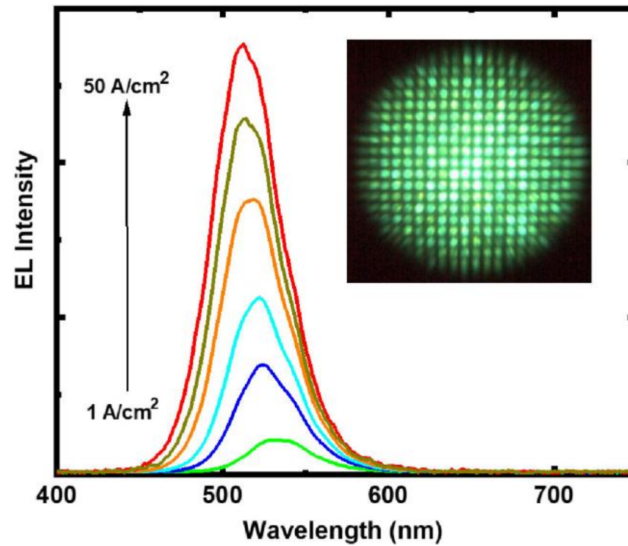

Figure 4.2: EL spectra of a 3.6 µm device. The inset is a photo image under 3 A cm^{-2} injection current density.

Figure 4.3a shows the typical forward I–V curves as a function of forward bias for the 3.6, 5, and 40 µm µLED array devices fabricated by our epitaxy overgrown approach. The 5 µm µLED array sample displays the lowest turn-on voltage and a high current value of 124.5 mA at 6 V, while the 3.6 µm µLED array sample has the highest turn-on voltage with a current of 33.8 mA at 6 V.

Figure 4.3b compares the reverse I–V curves of these epitaxy overgrown µLED arrays as a function of reverse bias. It shows that the total reverse current still favours the µLED arrays with a larger diameter. It indicates that the total leakage current increases with reducing µLED size. A typical I–V curves of the 10 µm µLED sample and 40 µm µLED sample fabricated by the conventional dry-etching method have also been presented in Figure 4.3c. To achieve accurate data and then draw a clear conclusion, we have conducted leakage current measurements on a few tens of µLED devices for both our epitaxy overgrown µLED arrays and the µLED samples fabricated by the conventional dry-etching method.

Table 1 is a summary of the leakage current characteristics for both our epitaxy overgrown µLEDs and the single µLEDs fabricated by the conventional dry-etching method, where the number of our epitaxy overgrown µLEDs in each device, the leakage current per LED, and the current densities have been listed. The ranges are a simple min–max analysis of the results observed.

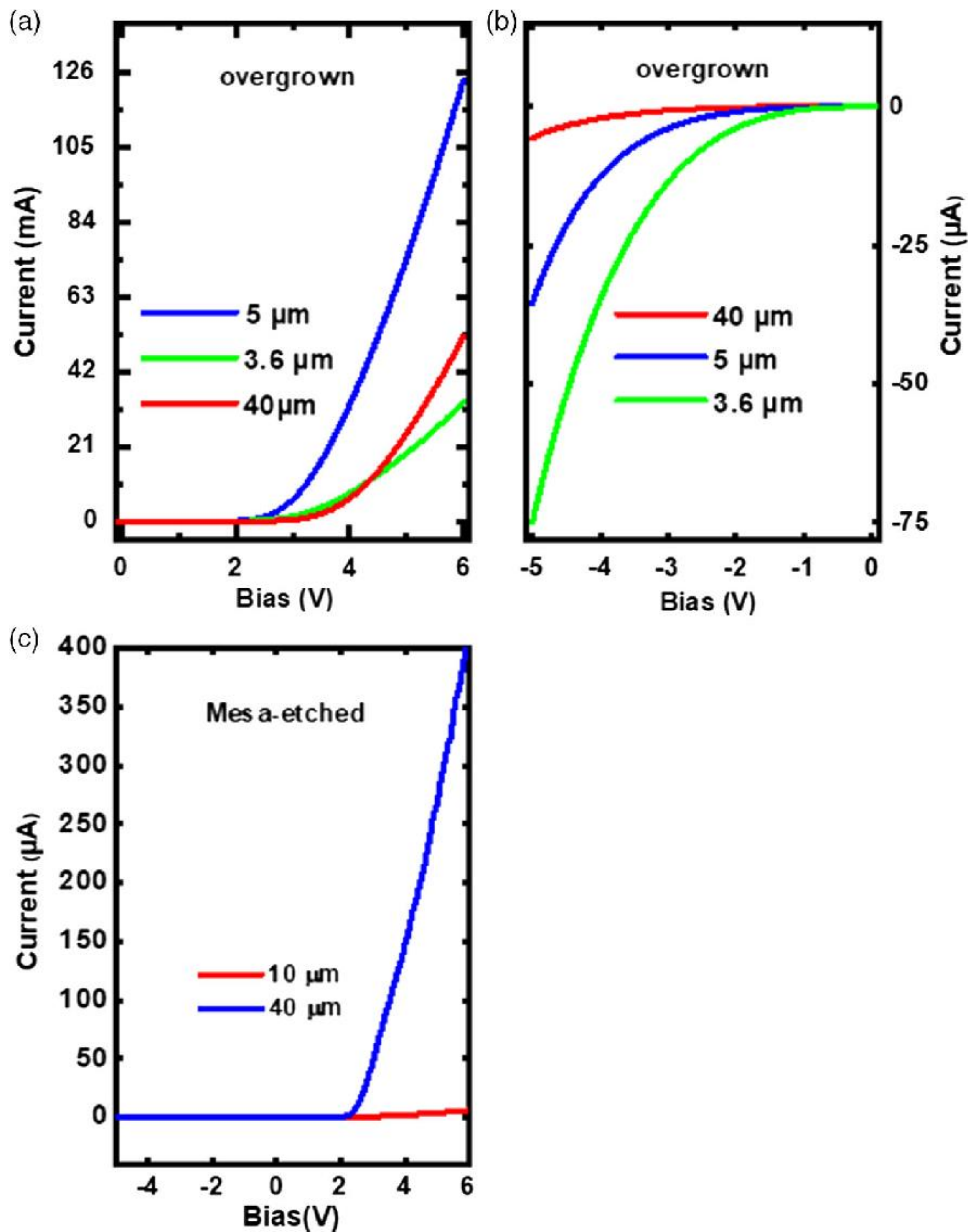

Figure 4.3: a) Forward I-V curves; **b)** leakage currents of the three µLED array sizes per LED and **c)** I-V curves of mesa-etched 10 and 40 µm LEDs.

A quick glance at the data about leakage current per µLED shows that our epitaxy overgrown µLEDs with a diameter of 3.6 and 5 µm performed similarly in terms of the ratio of forward to reverse current, but the 3.6 µm µLEDs show the best result in terms of leakage current per µLED under a reverse bias of 5 V. The overgrowth conditions as well as the device size may have contributed to this result. Importantly, our epitaxy overgrown µLEDs exhibit much lower leakage currents than those ones fabricated by the conventional dry-etching method. For example, the leakage current per µLED for our epitaxy overgrown 3.6 µm µLED reaches as low as 14.1 nA under a reverse bias of 5 V.

Moreover, the leakage current of our epitaxy overgrown µLEDs shows a smaller deviation than those ones fabricated by the conventional dry-etching method. It suggests one of two things; either the dry-etching-induced damage can be nonuniform within the sample, leading to substantially different leakage current within the same device group, or that the dry-etching processes induced difference in local defect density (from the centre part of each µLED to its edge part). Furthermore, it has been found that there is a moderate correlation between a decrease in µLED size and the leakage improvement for our epitaxy overgrown µLEDs. In contrast, those devices fabricated by the conventional dry-etching method suffer more from leakage as they get smaller, indicating the etching-induced damage becomes significantly severe with reducing the size of µLEDs as expected.

When the leakage current density is scrutinised, the leakage becomes more severe with decreasing the size of µLEDs. Clearly, when scaling down µLEDs, the perimeter to area ratio of a µLED increases, which leads to large surface recombination and increased current leakage. It is also noted that both the leakage current density and their dispersions are much smaller compared with the devices fabricated by the conventional dry-etching method. Moreover, when scaling down µLED, there is a significant increase in dispersion for the devices by the conventional dry-etching method, further confirming the severe issue of dry-etching on small µLEDs.

Device	No. of µLEDs per device	Leakage current per µLED at −5 V	Leakage current density (nA µm^{-2})
Overgrown 40 µm	36	159–850 nA	0.13–0.68
Overgrown 5 µm	1702	20–37 nA	1.04–1.88
Overgrown 3.6 µm	3472	14–17 nA	1.39–1.67
Convetional 10 µm	1	17 nA–38 µA	0.22–484
Convetional 40 µm	1	250 nA–400 µA	0.20–318

Table 4.1: A summary of leakage currents of our epitaxy-overgrown µLEDs and the µLEDs fabricated by the conventional dry etching method.

It is worth mentioning that ideally, the sidewalls of microLEDs are supposed to seamlessly contact with the sidewalls of the SiO2 masks. In this case, the leakage current is expected to be extremely small. To achieve this, the sidewalls of the SiO2 micro-masks need to be very straight, which depends on the thickness of SiO2 and ICP etching conditions. If the sidewalls of the SiO2 masks are slanted, tiny irregularities between microLEDs and SiO2 mask may be formed, forming a channel for current leakage. Nevertheless, the issue could be minimized by further optimizing the conditions of template fabrication.

Figure 4.4 shows the capacitance characteristics of the devices. To compare a single epitaxy overgrown µLED with a single µLED fabricated by the conventional dry-etching method, the total capacitances measured for the epitaxy overgrown µLED arrays were divided by the number of µLEDs within each array to obtain the capacitance for a single epitaxy overgrown µLED. This will provide a baseline to compare with a single µLED fabricated by the conventional dry-etching method, though contact resistivity and alternate current paths are likely to affect the end results in practice.

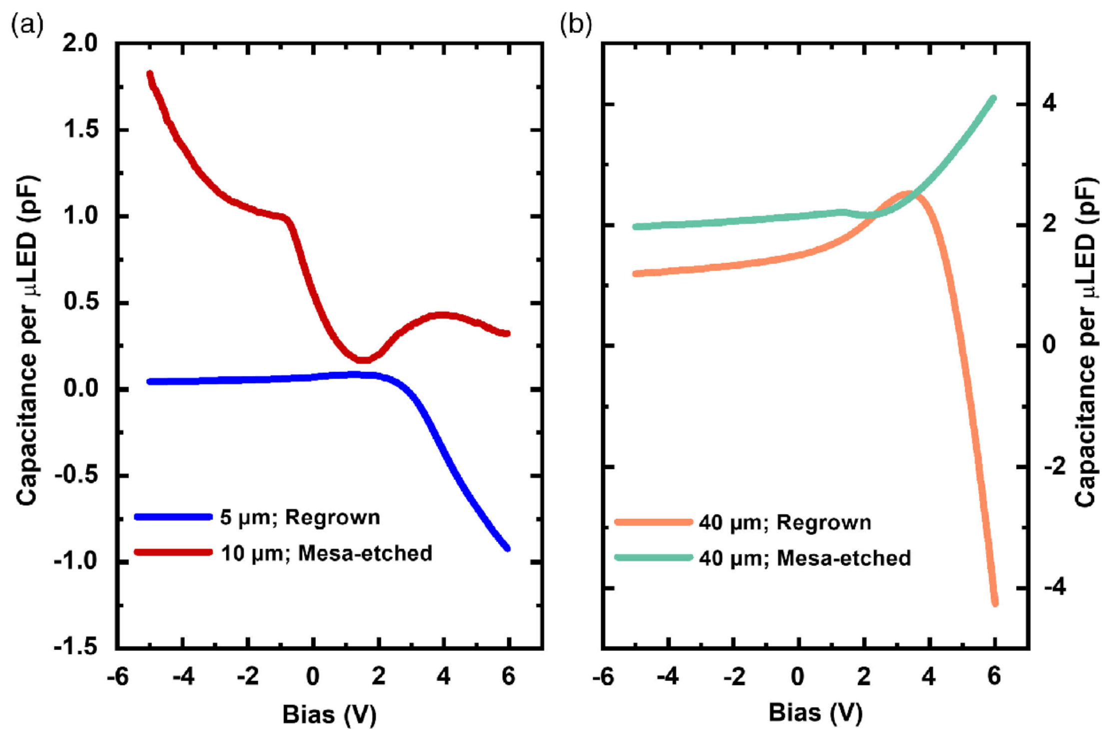

Figure 4.4: Capacitances gauged for a single device at 1 MHz. **a)** Overgrown 5 µm µLED versus Mesa-etched 10 µm µLED. **b)** Overgrown 40 µm µLED versus mesa-etched 40 µm µLED.

Figure 4.4a shows the typical C–V characteristics of our epitaxy overgrown 5 µm µLED, which is compared with the µLEDs with a diameter of 10 µm fabricated by the conventional dry-etching method (it is difficult to use a conventional dry etching method to fabricate µLEDs with a diameter of ≤ 10 µm). Purely from the perspective of the influence of size on capacitance with ignoring any other factors, the µLEDs with a diameter of 10 µm are supposed to exhibit 4 times capacitance as our epitaxy overgrown 5 µm µLED. However, the behaviour of the 10 µm µLED is completely different, and it never ends up going to the negative capacitance region with increasing bias.

This most likely can be attributed to the etching-induced damage being so significant at this µLED size that the sidewalls and/or trapping regions actively contribute to the charge–discharge cycles of the device. As a result, other factors such as surface induced damages instead of the size dominate

the capacitive reactance for the µLEDs with a diameter of 10 µm fabricated by the conventional dry-etching method.

To explain what this negative capacitance implies, it is imperative to understand LED junction capacitance variation by voltage. Traditionally, a pn-junction based LED will have its capacitance vary by a factor of the donor and acceptor concentrations, as shown in equation 4.2 [28]:

$$C_{dep} = {}^{\varepsilon A}\!/_{W} \;= {}^{A}\!\Big/_{(\sqrt{V_0 - V})} \sqrt{\left({}^{e\varepsilon_0\varepsilon_r(N_D N_A)}\!\Big/_{2(N_D + N_A)}\right)} \qquad (4.2)$$

Where C_{dep} is the depletion capacitance, ε the permittivity, A the active area of the device, W the depletion width, V0 the built-in voltage, V the applied voltage, e the electron charge, and Nd and Na the donor and acceptor concentrations respectively. This is however a time and frequency-independent variant of the dynamic, and to put this into an AC applied small signal perspective [29]:

$$C(\omega) = \frac{1}{\omega} Im\big(Y(\omega)\big)\; where\; Y(\omega) = \frac{\delta I(\omega)}{\delta V(\omega)} \qquad (4.3)$$

This forms the basis of using transient current-voltage relationships from complex parts of frequency-dependent measurements. A simple explanation is therefore that high-frequency capacitance can be thought of as a derivative of continuously increasing current density, and at a high enough injection current, this differential turns negative.

The NC effect is thought to be most pronounced at high injection currents and that there is an inductive effect taking place during electron-hole recombination, with presumably [30] referring to radiative recombination and that it is more likely to happen at the onset of LED emission. Therefore, the overgrown devices are more likely to display this effect, with them suppressing Shockley-Read-Hall recombination, since Auger is equally likely to happen to both.

We have further compared the C–V characteristic of our epitaxy overgrown µLEDs with a diameter of 40 µm and the µLEDs with a diameter of 40 µm fabricated by the conventional dry-etching method, which is shown in Figure 4.4b. Similar to Figure 4.4a, the 40 µm one fabricated by the conventional dry-etching method also suffers from parasitic capacitance characteristics under higher biases. Moreover, its starting positive capacitance is higher compared with the overgrown one. Rather than decreasing and flattening out in a curve, however, the µLEDs fabricated by the conventional dry-etching method keeps increasing in capacitance as the bias increases. In contrast, both the overgrown µLEDs in Figure 4.4a and b demonstrate the expected negative capacitance behaviour.

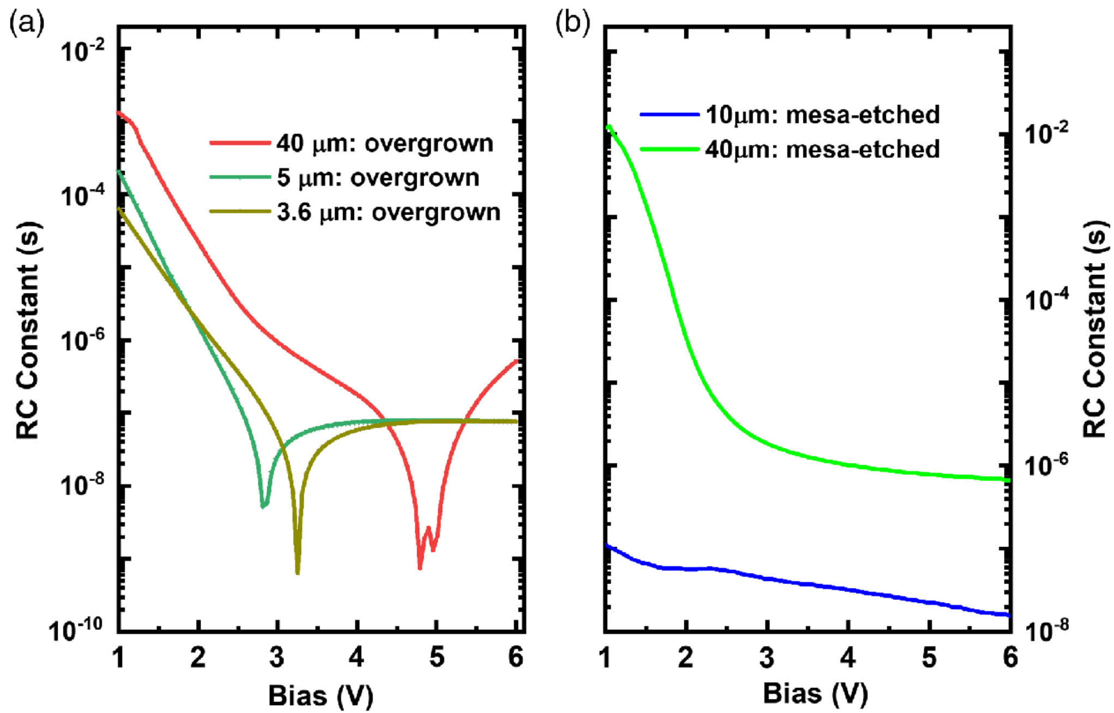

Figure 4.5: RC constants of **a)** overgrown μLEDs, and **b)** mesa-etched μLEDs.

Figure 4.5a shows the RC constants of our epitaxy overgrown μLEDs with different sizes as a function of bias, which have been measured by using the data multiplication of the resistance and the capacitance for each sample. The resistance curve is obtained by measuring the resistance using an SMU, which gets it dividing the voltage by the measured current. The LED resistance is also a voltage-dependent dynamic value like the junction capacitance, where it is $Vth/I_0(e^{eV/kT})$. The RC constants of our epitaxy overgrown μLEDs with smaller sizes reach their "bottom values" under high bias, indicating a quick transient response under high bias. Further increasing bias leads to their RC constants tending to be much lower across the board for all biases, down to the range of nanoseconds or even hundreds of picoseconds. For the 40 μm sample, except for its bottomed-out corresponding bias where it shows a pretty low RC, the RC constants in the main range are much higher than those of its 5 and 3.6 μm counterparts. Despite the fact that μLED arrays naturally have parasitic capacitance between devices, [6] the collective RC constant roughly equals the individual device because equal capacitances add and equal resistances divide in parallel. This means that the RC constants are mainly dominated by the size effect for our epitaxy overgrown μLEDs as expected. Normally, a wider device area should proportionally increase capacitance and decrease resistance, (for example, a 40 μm device should have 16 times the capacitance and 1/16 times the resistance compared to a 10 μm one) but due to the disproportionate decrease in capacitance per unit area in smaller LEDs, this is how there are discrepancies by size. Moreover, due to the implications of the NC effect mentioned, each size of LED hits their 'peak' RC at different values.

Figure 4.5b shows the RC constants of the µLEDs fabricated by the conventional etching method as a function bias. The 10 µm device consistently remains in the range from 10 to 100 ns. The response time of the 40 µm one maintains above µs under all the bias range. In contrast, Figure 4.5a shows that the smaller overgrown µLED devices allow for nanosecond response times. By combining with the reduced leakage characteristics, our epitaxy overgrown µLED devices place them in a good position for high-frequency switching applications.

4.5: Conclusion

The leakage and forward currents have been measured on our epitaxy-overgrown µLEDs with different sizes, showing a significant improvement in comparison with those µLEDs fabricated by the conventional dry-etching method. The influence of the µLED size on the leakage current has been systematically investigated. Due to the effective elimination of etching-induced damage by an overgrowth approach which is particularly important for smaller µLEDs, it reveals that our smaller overgrown µLEDs have much smaller leakage current than those µLEDs fabricated by the conventional dry-etching method in terms of either leakage current per µLED or leakage current density. Moreover, the µLEDs fabricated by the conventional dry-etching method displays a larger dispersion in leakage current, especially for those smaller µLEDs, which is attributed to high amounts of dry-etching-induced damages. Furthermore, the RC constants have also been found to be more favourable to the epitaxy overgrown devices. It is expected that our epitaxy overgrown µLEDs will bring about advantages of better pixel-level resolution, high efficiency, and energy efficiency to applications of micro-display, augmented/virtual reality setups, and VLC.

4.6: References

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Chapter 5 – Electrical and structural investigation of HEMTs grown in a 2D growth mode

An extensive study has been conducted on a series of AlGaN/GaN high electron mobility transistor (HEMT) samples, grown as (0001) 'c-plane' GaN, using metalorganic vapour phase epitaxy, to investigate the influence of growth modes for GaN buffer layers on device performance. The unintentional doping concentration and screw dislocation density are significantly lower in the samples grown with our special two-dimensional **(**2D) growth approach, compared to a widely-used two-step method combining the 2D and 3D growth. The GaN buffer layers grown by the 2D growth approach has achieved an unintentional doping density of 2×10^{14} cm^{-3}, two orders lower than 10^{16} cm^{-3} of the GaN samples grown using a conventional two-step method. High-frequency capacitance measurements show that the samples with lower unintentional doping densities have lower buffer leakage and higher breakdown limits. This series of samples have attained sub-nA/mm leakages, a high breakdown limit of 2.5 MV/cm, and a saturation current density of about 1.1 A/mm. It indicates that our special 2D growth approach can effectively lessen the unintentional doping in GaN buffer layers, leading to low buffer leakage and high breakdown limits of GaN/AlGaN HEMTs.

5.1: Introduction

GaN based band gap semiconductors are alluring for power electronics due to a number of major advantages in comparison with other III-V semiconductors,[1-13] such as the inherently high breakdown electric fields which are disputed to be anywhere between 3 and 3.7 MV/cm, the saturation carrier velocity of 2.5×10^{7} ms^{-1} and the intrinsic electron mobility around 900 – 1250 cm^{2} V^{-1} s^{-1} at room temperature which can be further be enhanced up to 2100 cm^{2} V^{-1} s^{-1} through the formation of an AlGaN/GaN heterostructure leading to high electron mobility transistors (HEMTs).

As a result, research into high electron mobility transistors (HEMT), from the very first inception in III-arsenide material system,[14,15] has been a cornerstone of III-nitride semiconductor material research for high-frequency, high power and high temperature applications.[16-22] In order to maximise the exploitation of the major advantages and maintain a performance faithful to the figure of merit of the material, it is necessary to minimise the buffer leakage of GaN-based HEMTs, one of the fundamental issues that prevent a HEMT structure from naturally excellent electronic performance. It is generally regarded that dislocations lead to formation of unintentional donor/acceptor traps, in particular the resultant deep level traps, [23, 24] providing an effective path for current leakage. [23, 25, 26] However, the relationship between the fundamental issue and a growth mode

is unclear, which is of paramount importance for further improving the electrical properties of the GaN buffer in AlGaN/GaN HEMTs.

It is well-known that a classic two-step growth approach has been widely used for GaN grown on sapphire by using metalorganic vapour phase epitaxy (MOVPE) techniques. This approach consists of the initial deposition of a thin GaN or AlN nucleation layer at a low temperature (LT) and the preparation of a thick GaN buffer layer at a high temperature (HT) prior to the growth of any further device structures. For the two-step growth method, small islands on a nanometre scale initially form as a result of a subsequent annealing process underwent on the LT nucleation layer, followed by a gradual coalescence process. Finally, a flat surface can be obtained. It means that the growth of GaN on sapphire initially follows a three-dimensional (3D) growth mode and then takes a two-dimensional (2D) growth mode. However, it is a great challenge to obtain a semi-insulating GaN buffer layer which is required for GaN electronics by using this two-step approach. [27-29] Very recently, we employed a high-temperature (HT) AlN buffer technique for the growth of an AlGaN/GaN HEMT structure on sapphire, [30-34] demonstrating an extremely low off-state buffer leakage current of down to 1 nA/mm at 1000 V. [35] Unlike the classic two-step growth method, our high-temperature AlN buffer technique leads to a 2D growth mode throughout the whole growth processes. Furthermore, our GaN on sapphire obtained by this 2D growth mode exhibits an extremely narrow full width at half maximum (FWHM) of on-axis X-ray diffraction (XRD) rocking curve along (0002) direction, [31] which implies an extremely low screw dislocation density.

An illustrative diagram is also necessary to discuss how the two methods compare. Figure 5.1 shows an overview of how the two methods are performed using MOCVD.

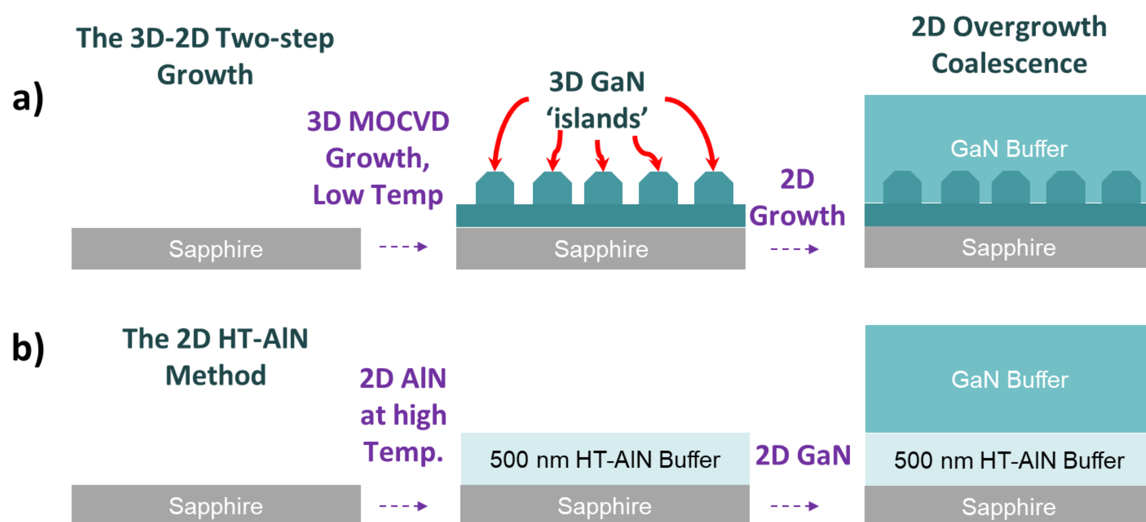

Figure 5.1: a) The two-step 3D/2D GaN buffer and **b)** The HT-AlN 2D method.

The two-step method first uses a lower V-III ratio at lower temperature to initiate 3D growth, which results in 3D 'islands' of GaN being formed on a total of 25 nm thick nucleation layer; this is then followed up by increasing the V-III ratio to follow up with a 2D growth coalescence into a full buffer layer. The HT-AlN method, in contrast, uses 2D growth throughout, with the AlN buffer being the nucleation layer and again a 2D overgrowth of GaN.

In this study, a systematic investigation has been carried out a series of HEMT structures grown by using our HT AlN buffer techniques, where the AlN buffer was prepared under different growth conditions. Detailed on-axis and off-axis XRD measurements have been performed on these samples to examine their screw dislocation densities, which has been found to be dependent on the growth conditions, in particular the V/III ratio during the AlN buffer growth. A capacitance-voltage (CV) technique, a powerful non-destructive tool which allows for working acceptably with low doping concentrations, has been employed to assess the unintentional doping densities in the GaN buffer layers in these samples.[36] A combination of both XRD and CV measurements has confirmed that the 2D growth approach leads to a significant reduction in screw dislocation density, which massively reduces the unintentional doping levels in the GaN buffers of our AlGaN/GaN HEMT structures by using the HT AlN buffer technique.

5.2: Sample description

In this work, four HEMT samples, which were all grown on c-plane (0001) sapphire substrates using MOVPE, have been studied, labelled Sample A to D. Figure 5.2a schematically illustrates a block diagram of the epitaxial structure for the four HEMT samples. It is worth highlighting that Sample A was grown by a modified two-step method, with a 25 nm GaN nucleation layer grown at 550°C, followed by a HT GaN buffer layer grown at a temperature a little bit lower than usual. The decreased growth temperature of the GaN buffer aims to form a semi-insulating GaN buffer layer by increasing carbon doping for compensation of the unintentional n-type doping. The other three samples, Sample B, C, and D, were all grown by our HT AlN buffer approach, which started with an AlN buffer layer grown at high temperature and followed by a HT GaN buffer layer. The subsequent structure after the 1.5 µm GaN buffer layer is identical for all samples, composed of a 1 nm AlN spacer layer and a 30 nm $Al_{0.2}Ga_{0.8}N$ layer, as demonstrated in Figure 5.2a.

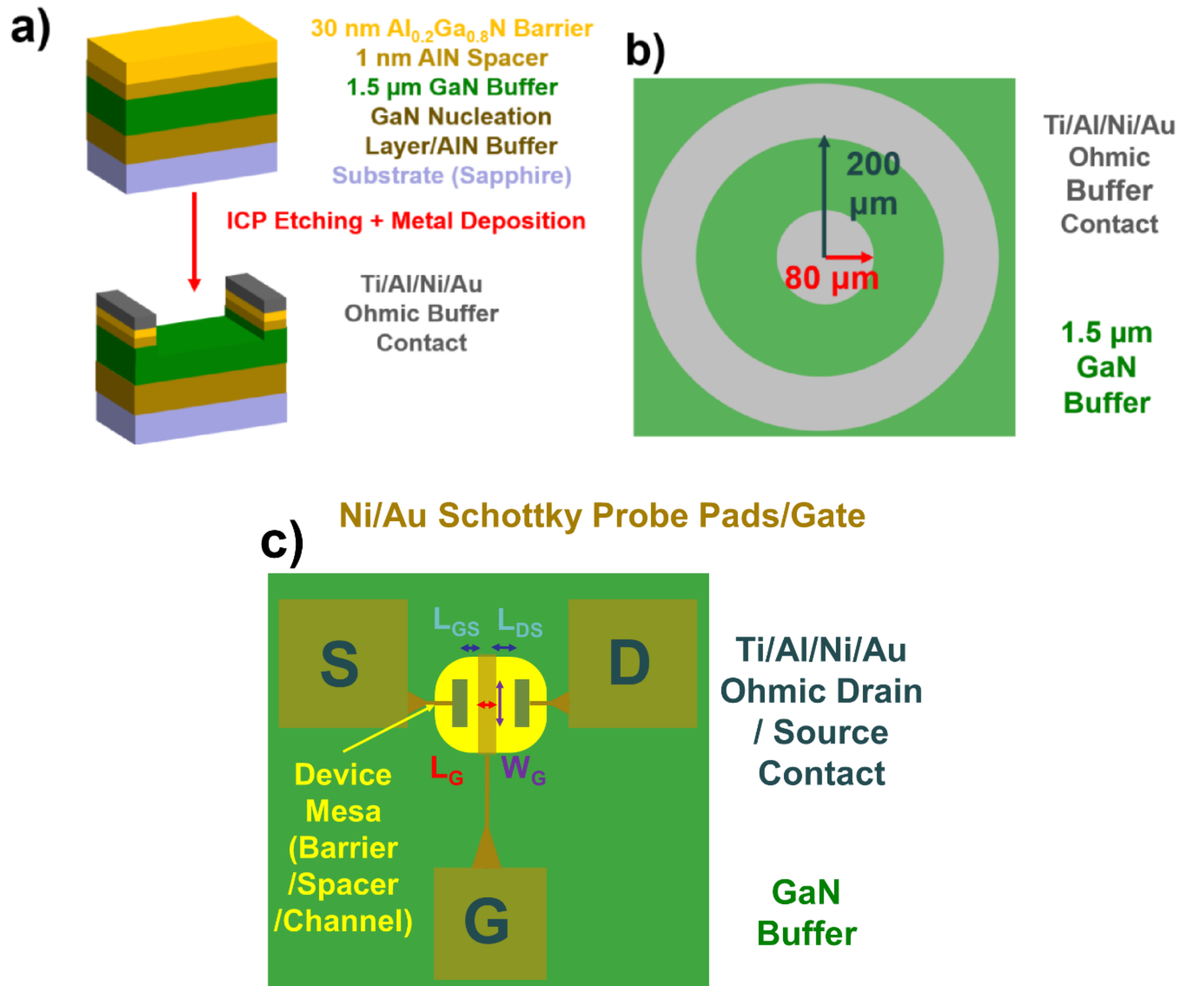

Figure 5.2: a) A block diagram of the device structure. **b)** A circular metallic deposition pattern normally used for Schottky Barrier Diodes deposited only as Ohmic metal on the buffer. **c)** A schematic configuration of the HEMT device.

5.3: Experimental

Table 5.1 shows layer-by-layer growth conditions of the individual samples as a function of temperature, pressure, and the flow rates of precursors. For both the AlN buffer layer and the GaN buffer layer, compared to Sample A, the V/III flow rate ratios of Sample B, C, and D were grown with a much higher V/III flow rate ratios to encourage the 2D growth.

Moreover, the GaN buffer was grown at a higher pressure of 225 Torr for Sample A and Sample B, but at a lower pressure of 175 Torr for Sample C and Sample D. In addition, only for Sample D, the GaN buffer layer was grown at a bit higher temperature. The growth conditions for the aforementioned HEMT structures, a thin GaN layer, an AlN spacer and an $Al_{0.2}Ga_{0.8}N$ layer subsequently grown, are all identical for the four samples.

Sample	Layer	Temperature [°C]	Pressure [Torr]	NH_3 Flow Rate [sccm]	TMGa Flow Rate [sccm]	TMAl Flow Rate [sccm]
A	*AlGaN Barrier*	1100	75	5480	12.5	30
	AlN Spacer	1100	75	5480		30
	1.5μm GaN Buffer	1100	225	5480	65	
	25nm LT GaN Nucleation Layer	550	65	1900	65	
B	*AlGaN Barrier*	1110	75	5480	12.5	30
	AlN Spacer	1110	75	5480		30
	1.5μm GaN Buffer	1110	225	5480	65	
	HT-AlN Buffer	1180	65	5480		180
C	*AlGaN Barrier*	1108	75	5480	12.5	30
	AlN Spacer	1108	75	5480		30
	1.5μm GaN Buffer	1108	175	5480	65	
	HT-AlN Buffer	1180	65	5480		180
D	*AlGaN Barrier*	1130	75	5480	12.5	30
	AlN Spacer	1130	75	5480		30
	1.5μm GaN Buffer	1130	175	5480	65	
	HT-AlN Buffer	1180	65	5480		180

Table 5.1: The growth parameters of the four samples.

After the growth, circular Ohmic contacts that are the same size and pattern as our Schottky Barrier Diodes are fabricated on the HEMT epi-wafers for investigation on unintentional doping in the GaN buffer layers, as shown in Figure 1b. First, UV photolithography and inductively coupled plasma (ICP) etching were used to expose the main GaN buffer layer all around the sample except the contact sites. Ti/Al/Ni/Au metals with thicknesses of 20/70/20/55 nm were deposited as the Ohmic contact using thermal evaporator. The contacts were then rapidly thermally annealed at 800°C for 30 s in N_2 ambient. Next, Si_3N_4 is deposited using plasma-enhanced chemical vapour deposition (PECVD) for passivation, with the intent of suppressing surface state conduction and parasitic leakage paths. This is important for the purpose of gauging the inherent leakage from the buffer layer. Finally, the Si_3N_4 on top of the contacts is removed by ICP etching for measurements.

Moreover, HEMT devices are also fabricated on the HEMT epi-wafers as shown in **Figure 5.2c**. The fabrication process is described as below: A 300 nm depth mesa is etched down to define the active region for the HEMT by ICP etching, then the metal stack of Ti/Al/Ni/Au (20/150/30/80 nm) is deposited and then annealed at 800°C for 30 s in N_2 ambient for 30 s in order to form Ohmic contacts for the source and drain of the HEMT. Finally, a Ni/Au (50/150 nm) alloy is deposited in order to form a Schottky gate for the HEMT.

5.4: Results and Discussion

In order to obtain the dislocation information, X-ray diffraction (XRD) measurements are performed on the four samples, using a Bruker X-ray diffractometer with a 1.54 Å Cu-Kα tube. Figure 5.3a to 5.3d record ω rocking curves of the four samples along the (002) lattice axis and along the (102) axis, which can reflect densities of screw and mixed dislocations in the epitaxial samples, respectively.

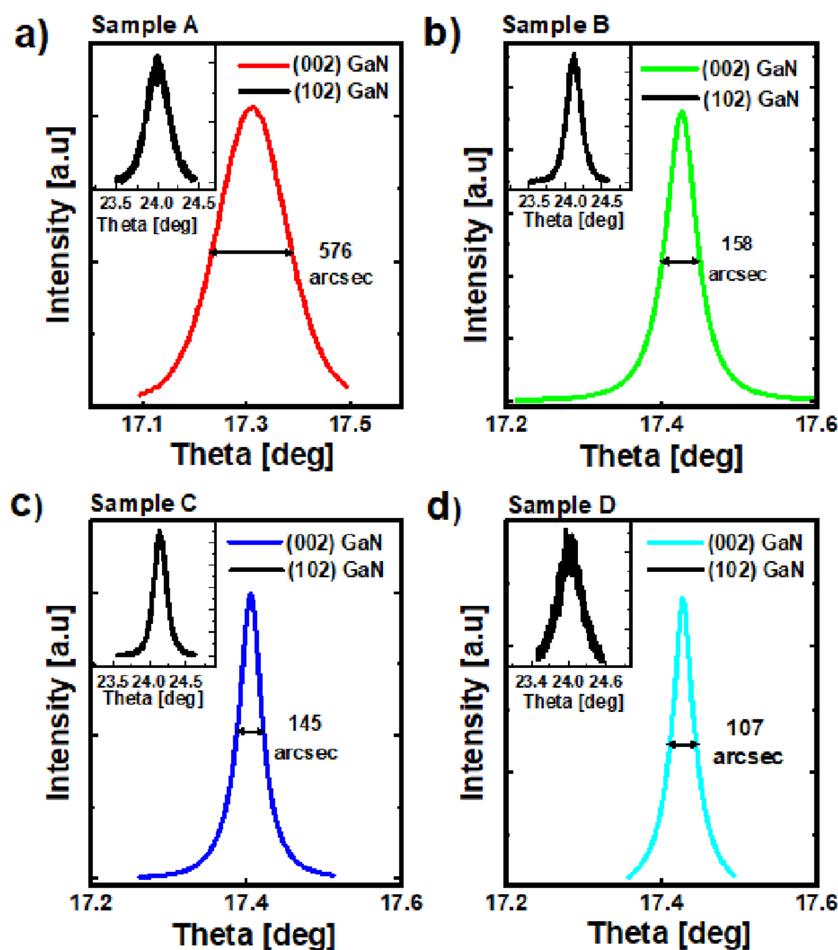

Figure 5.3: XRD measurements along the (002) axis and (102) axis for Sample A (a), Sample B (b), Sample C (c) and Sample D (d), respectively.

Equation 5.1, the Gay-Hirsch-Kelly Equation, originally used for metals, first modified by Dunn and Koch, is used to calculate the dislocation density from the width of each peak for each orientation for GaN XRD measurements, in full widths at half of maximum (FWHM) [37-39]. It is as follows [37]:

$$D_{screw} = \frac{\beta^2_{(0002)}}{4.35 b^2_{screw}} \quad D_{edge} = \frac{\beta^2_{(10\bar{1}2)} - \beta^2_{(0002)}}{4.35 b^2_{edge}} \tag{5.1}$$

As for an explanation of the terms, D_{screw} is the calculated screw dislocation from (002)/(0002) GaN and D_{Edge} is the calculated edge dislocation from the differential of (102)/(10-12) and (002) GaN. βc and βa are the peak widths for the c-axis (002) and a-axis (102), converted to radians from degrees by multiplying with 2π and dividing by 360. The b terms are the Burgers vectors – dislocation vectors that relate to the lattice constants of GaN – equal to 0.3189 nm for edge-type and 0.5185 nm for screw-type dislocations. Once the edge and screw components are calculated from (102) GaN scans, the results are added together to calculate mixed dislocations, whereas (002) GaN results are accepted to be the total screw dislocation density. [37-39]

Table 5.2 shows the corresponding FWHM and calculated dislocation densities. Compared to Sample A, the screw dislocation densities of Sample B, C and D are one order lower, which means that the screw dislocation density is decreased with the 2D growth being enhanced. The mixed dislocation density, however, does not follow a corresponding decrease and is a lot more complicated, suggesting that the edge dislocation density does not follow this trend. Given that the buffer leakage paths are mainly affected by screw dislocations, it implies that the 2D growth is effective in suppressing breakdown limits.

Sample	(002) GaN FWHM [°]	Screw Dislocation Density [cm^{-2}]	(102) GaN FWHM [°]	Mixed Dislocation Density [cm^{-2}]
A	0.1599	6.7×10^{8}	0.3005	8.6×10^{9}
B	0.0438	5.0×10^{7}	0.2363	5.3×10^{9}
C	0.0402	4.2×10^{7}	0.1948	3.6×10^{9}
D	0.0296	2.3×10^{7}	0.4429	1.9×10^{10}

Table 5.2: XRD measurement data of the four samples and their inferred dislocation densities.

The voltage-current (I-V) characteristics are measured on the four HEMT devices using a Keithley source measure unit, connected to a PC for remote testing and data extraction, and a probe station equipped with an optical microscope. The biases are from -20 V to 20 V. The measurements were conducted on a few devices for each sample to ensure consistency in results. Moreover, the transistor characteristics are measured through two sweeping voltages applied to the gate and drain, of -9 to 1 V and 0 to 10 V, respectively.

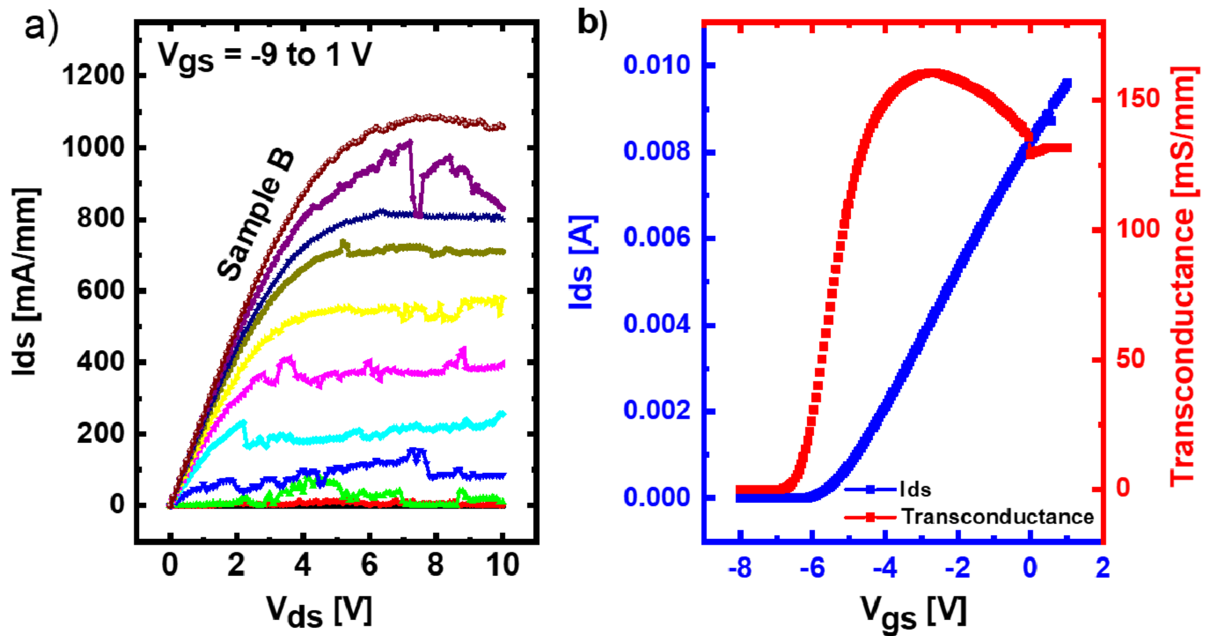

Figure 5.4: (a) I-V characteristics of Sample B. (b) Transconductance for a HEMT on Sample B.

Figure 5.4a displays an I-V plot of the device with the highest saturation current, i.e. Sample B. Figure 5.4b demonstrates its corresponding consistent transconductance curve. A high current rating of about 1.1 A/mm is obtained for Sample B. Though there is a report on higher current densities of 1.4 A/mm, it employed intentionally doped barriers and different substrates – SiC to be exact, which has a lower lattice mismatch with GaN than sapphire. [26] It is noted that the record I-V curve is not quite smooth, which could be related to donor traps. These charge traps emerge as ICP etching for isolation of the HEMT mesa, which is small, creates trapping sites, comparable to the LED sidewall damage mentioned in previous Chapters, which cause electrons to be trapped in them in charge/discharge cycles. Nevertheless, a high current density has been obtained in a HEMT device which is achieved through our special 2D growth and without an intentional doping. The only case where a > 2 A/mm current density has been observed on sapphire was with dedicated AlInN ternary alloy barriers which allow for gate modulation up to 2 V VGS with a Schottky contact, lattice matching for overgrowth on GaN and almost the full spontaneous polarisation of AlN for induction of 2DEG charges, and another with 1.43 A/mm where sub-1 µm gate length devices were able to be fabricated using EBL, thus leading to higher density, in addition to Ohmic contact area pre-treatment with $SiCl_4$ [40, 41]. The strength of our method, however, is the combination of increased breakdown limits with relatively high current density.

The capacitance characteristics are captured on the circular Ohmic structures by a Keysight E4980A LCR (inductance-capacitance-resistance) meter, which is calibrated for an open-circuit prior to measurements. These are performed at 1 MHz to ensure the frequency is large enough to both

reduce series reactances and improve reliability of the results for small-signal frequency of operation. Capacitance data included here is of the parallel equivalent circuit model. Voltage biases of -20 to 0 V have been chosen to roughly correspond to depletion voltage regimes. Equation 5.2 describes the capacitance integration method as follows [42]:

$$n(2D) = \int_{V_T}^{V} \frac{C\,dV}{(qA)} \tag{5.2}$$

Where C is the measured capacitance per point of the devices; V_T is the lower voltage threshold used to integrate the capacitance data; V is the upper limit (in our case, V = 0); q is the electron charge (1.6×10^{-19} C) and A is the active area of the device. Because we have no Schottky contacts, the inter-contact area is used instead. The end result as a 2D charge density can be extrapolated onto a 3D space to give the final result for the calculated unintentional doping concentration per unit volume rather than sheet area.

Figure 5.5a shows a collective of representative capacitances at reverse bias measured from -20 to 0 V for all the samples. Figure 5.5b displays unintentional doping concentrations which are obtained by integrating the resultant capacitances over the voltage range, using Equation 5.2 and extrapolated into a 3D charge density as described by raising the 2D result to the power of 1.5.

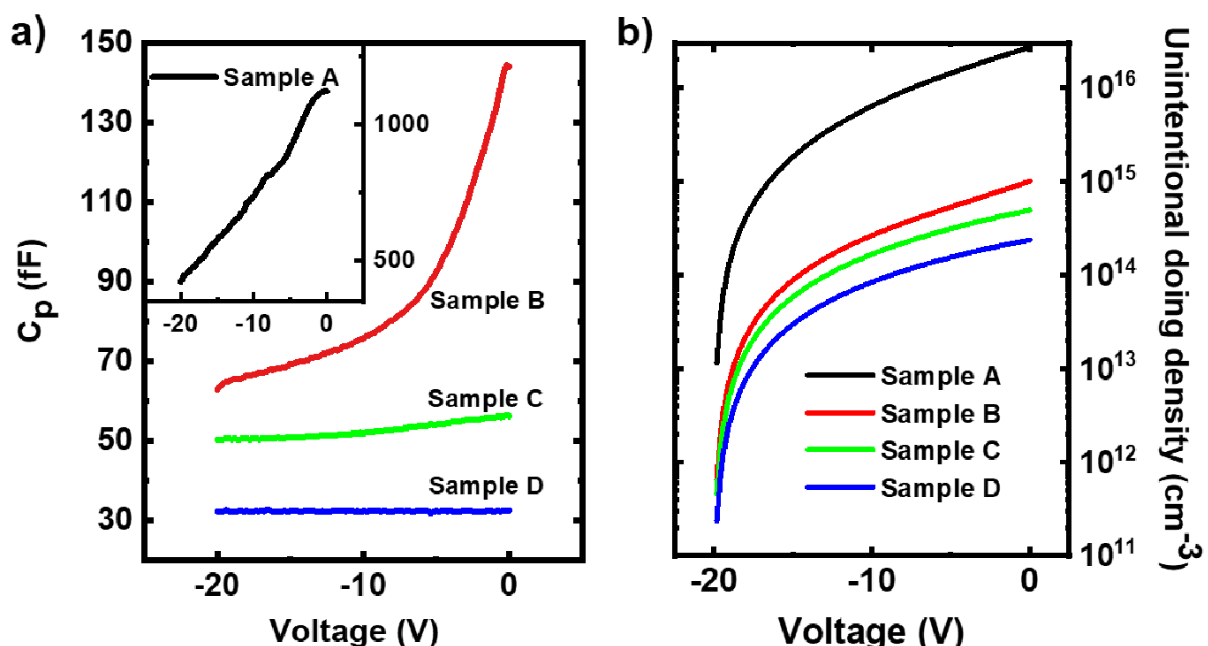

Figure 5.5: (a) Capacitance curves obtained for a Schottky Barrier Diode for all devices under negative bias. (b) The inferred unintentional doping curves for the four samples.

Sample A has the highest capacitance, as high as slightly above 1 pF, which corresponds to the highest unintentional doping density. In addition, its increase in capacitance over the given voltage range is also the most significant among these samples, which is an indicator of depletion regime for the unintentional doping. Compared to Sample A, other three samples successively show slower rise in capacitance with the voltage as well as lower starting capacitance. Sample B is on the higher end for starting capacitance and increase in capacitance from depletion region (-20 V) to equilibrium state (0 V bias) compared to Sample C, which shows a lower starting capacitance and a smaller rise when integrated, and Sample D as the lowest of both. Therefore, when the aforementioned capacitance curves are integrated, it is evident that Sample D has the lowest unintentional doping, Sample C higher still, Sample B higher than that and Sample A has the highest unintentional doping.

Though, when zoomed in, the capacitance increase for Sample D within this regime is overshadowed by the instrument's innate noise, the integration method is resilient enough to be able to still calculate the doping density with reasonable accuracy.

Given the samples' growth parameters, a lower buffer growth pressure (Samples C and D have buffers grown at 175 Torr as opposed to 225 for the others) and a higher buffer growth temperature (1130°C for Sample D, versus C, at 1108°C) seems to lead to lower unintentional doping in general. More growth is necessary to establish this hypothesis as a trend, however. It is clear that all of the 2D HT-AlN samples outperform the traditional 3D-2D two-step growth for obtaining a semi-insulating buffer, however.

Sample	D_{screw} [cm^{-2}]	Calculated $N_{unintentional}$ [cm^{-3}]	Buffer Leakage, 2 µm@20 V [pA]	HEMT Current Density, Lg = 10 µm [mA/mm]	Breakdown Limit of Buffer [MV/cm]
A	6.7×10^{8}	1.0×10^{16}	1136.4	1024	0.25
B	5.0×10^{7}	1.0×10^{15}	980.9	1086	0.6
C	4.2×10^{7}	5.0×10^{14}	615.0	920	1.9
D	2.3×10^{7}	2.0×10^{14}	41.7	582	2.5

Table 5.3: A summary of each sample's performances in five categories: screw dislocation density, calculated unintentional doping concentration, buffer leakage for a 2 µm spacing, maximum saturation current density for a full HEMT device, and breakdown limit of the sample.

Table 5.3 lists the measured performances of the four samples in terms five quantities: Overall calculated unintentional doping concentrations obtained from the contacts' capacitance characteristics; screw dislocation density; buffer leakage current at 20 V; breakdown field limits, [35] and forward saturation current density at V_{GS} = 1 V. It is found that the unintentional doping concentrations of Sample B, C and D are one order or even two orders lower than that of Sample A. It

indicates that the 2D growth efficiently reduces the unintentional doping, which can be further lessened by a lower pressure during the buffer growth. It results in a strong link between the screw dislocation density and the unintentional doping concentration, i.e., the screw dislocation density in the sample is always higher when the doping concentration is higher. It further confirms that screw dislocations lead to formation of unintentional donor/acceptor traps and can be significantly prevented by the 2D growth.

The breakdown measurements were performed on similar buffer Ohmic contact structures separated by 3 µm in a special high-voltage permitted laboratory with source measure units with sweeps up to 1000 V. Fluorinert, a trademarked mix of fluorocarbon compounds, has been used to prevent aerial breakdown above 300 V. The end result for the breakdown field was obtained by converting the applied voltage to the field strength and the current to mA/mm. The current densities for full HEMT devices were obtained by dividing the current by the gate length then converting to mA, thus also yielding a result in mA/mm.

Furthermore, as shown in Table 5.3, the samples with lower screw dislocation densities are found to have lower leakages and higher breakdown field limits, such as Sample B, Sample C and Sample D, due to lessened leakage paths and increase of channel off-resistance. Sample D, with the lowest screw dislocation density, has achieved a well-recorded breakdown characteristic of 2.5 MV/cm, exceeding the breakdown limits of even intentionally C-doped buffer structures, which are limited to 2 MV/cm due to deep acceptor traps and the impurities-introduced extra dislocations [35, 43]. In the case of auto C-doping, carbon acts as a deep acceptor for GaN, contributing extra holes at an energy level distant from the valence band of GaN. Therefore, any recombination of holes and electrons that happens during device operation will recombine at these new energy states, thus in effect reducing the effective bandgap of the GaN structure in question, partially negating the increased buffer resistivity from counter-acting the unintentional n-type doping. Meanwhile, impurities such as the aforementioned dopants reduce the breakdown limit due to worsening buffer quality by introducing defects.

However, it is worth mentioning that the samples with lower unintentional doping densities attain lower saturation currents, which is not good for device performance. Though Sample D is the best sample in terms of screw dislocation density, leakage, and breakdown limit, it is also the worst in terms of full device saturation current density. A modulation and delta doping has been reported to be used in c-plane GaN/AlGaN HEMTs to achieve extremely high current densities [26]. It is expected that the modulation doping can be employed to the growth of Sample D to induce both great on-state current densities and low off-state current densities with high breakdown voltage limits. Nevertheless,

in the absence of intentional doping, Sample C offers the best compromise of a good saturation current density and a good performance with high breakdown limit and low leakage.

5.5: Conclusion

We have performed a comprehensive study on GaN/AlGaN HEMTs grown with a special 2D-growth approach, and made a comparison with a two-step method with a combination of 2D and 3D growth. It is found that the unintentional doping concentrations and screw dislocation densities are significantly lower in the 2D-grown samples compared to the two-step growth method, achieving a very low unintentional doping density of 2×10^{14} cm^{-3} and a screw dislocation density of 2.3×10^{7} cm^{-2}. High-frequency capacitance measurements show that the samples grown with the 2D growth approach have much lower buffer leakage and higher breakdown limits, attaining a sub-nA/mm leakage, a high breakdown limit of 2.5 MV/cm, and a saturation current density of about 1.1 A/mm. It indicates that our special 2D-growth approach can effectively lessen the unintentional doping in the GaN buffer layers, leading to GaN/AlGaN HEMTs with low buffer leakage and high breakdown limits.

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Chapter 6 – Electrical investigation of non-polar HEMTs on r-plane sapphire

The non-polar planes of III-Nitride semiconductors are of particular intrigue due to their inherent suppression of QCSE (Quantum Confined Stark Effect), displaying much ambition for monolithic integration of photonics and power electronics, with the premise of eliminating green-yellow wavelength shift and not being constrained to spontaneous polarisation for inducing 2DEG, thus allowing for varying gate modulation. On sapphire, one reliable, lower cost and higher yield way compared to freestanding non-polar GaN substrates, to grow orientationally-consistent wafers, is by using a-plane (11-20) GaN growth on r-plane (10-12) sapphire. a-plane GaN is non-polar, meaning it has no inherent spontaneous polarisation (P_{SP}), unlike c-plane, which has the full value of P_{SP} for GaN and thus is considered polar. A set of such samples were grown using MOVPE (Metalorganic Vapour Phase Epitaxy). Our samples of interest grown in this way have crystal qualities at slightly greater than 1300 arcsec and electron mobilities between 7 and 76 $cm^2V^{-1}s^{-1}$ leading to current densities of 30 to 65 mA/mm for the successfully gate-modulated samples.

Experimentation with the application of quantum mechanics, bandgap engineering and different epitaxial parameters to confine and improve the mobility of 2DEG electrons in non-polar a-plane GaN/AlGaN HEMTs on r-plane sapphire, yields potential paths of improvement on the platform as well as tangible improvements that have already been recorded such as increased electron mobility of 76 cm^2 V^{-1} s^{-1}. While this planar combination is usually limited to an electron mobility of 46 cm^2 V^{-1} s^{-1} due to sample quality, our application of the principles of a quantum well as the main GaN channel has increased that all the way up to 76 cm^2 V^{-1} s^{-1} according to Hall Effect measurements. Our simulations, as well as measurements, also provide a guideline for optimising Al percentage, barrier thickness and general epitaxial structure for this type of HEMT to provide decent performance.

6.1: Introduction

High Electron Mobility Transistors (HEMT) have been a focal point of many works of research on Group III-Nitride (GaN/AlGaN/AlN/InGaN…) devices in the last couple of decades due to several qualities of the material set and heterojunctional transistor technology that lend themselves to effective usage with high-frequency and EM emission/power integrated systems. These include: A high breakdown electric field and saturation electron velocity owing to the material capabilities; better current density performance and mobility compared to their silicon-based peers (while intrinsic silicon has acceptable mobility, polycrystalline silicon growth and reliance on doping at all device layers both produce carrier scattering), versatility with power and EM applications, relatively low degree of breakdown condition power loss (indicative by its high Baliga figure of merit) and greater physical

resilience thanks to the material's Young's modulus [1 – 5]. Indeed, the use of AlGaN/GaN HEMT devices in a microwave frequency engineering context are prevalent, with one particular example demonstrating gain even up to 300 GHz. The increasingly widespread use of III-nitrides in visible light and power systems is also expected to spearhead further advances in the nascent Li-Fi technology, with already-existent communications modulation protocols under experimentation, unlike their more mature arsenide counterparts, which, while attractive for their exceptional mobility, only emit in the mid-infrared range. [6 – 8]

Most of existing examples of successful HEMT technology use the fully-polar c-plane of GaN, and the reasons are manifold: Growth is easier since the sapphire substrates used are already in this orientation by default as well as growth on similarly-hexagonal SiC; the spontaneous polarisation causes a built-in energy band bias that generates an innate build-up of charges, thus eliminating the need for doping; easy compensation of thermal expansion and a low lattice mismatch; acceptable performance through transfer onto a silicon substrate and so on. Ever increasingly, however, it is becoming evident that research into non-polar GaN is relevant because of spontaneous polarisation's effect on EM wave-related performance droop, especially for green light, which is a well-documented drawback caused by QCSE. [9 – 12] One such demonstration of why non-polar GaN helps suppress QCSE may be found in Chapter 2 as Figure 2.20.

GaN, but especially in the c-plane orientation or other fully polar planes, also struggles to achieve normally-off enhancement mode operation so transistors from it are often cleverly combined with existing normally off 'switches'; in the form of a silicon transistor driving the GaN-based HEMT, and from another power device standpoint, fully polar (Al)GaN is prone to a phenomenon called current collapse, courtesy of trapped charges in a small-signal AC field whose alternating flow is distorted by polarisation, negatively impacting AC saturation current. [9 – 12]

The obvious solution then, in the confines of stable Wurtzite GaN, is the use of semi- and non-polar III-Nitride planes for use in integration. Non-polar GaN/AlGaN HEMTs are in a relatively early stage of their development – the few select successful examples use off-cut freestanding m-plane (10-10) or freestanding a-plane GaN substrates as this yields the highest crystal quality possible. Current densities of up to 340 mA/mm on freestanding m-plane GaN substrates [13] have been previously attained. However, this is expensive and difficult to reproduce on a large scale, especially since the freestanding substrates themselves are expensive to produce even before considering overgrowth, so a less costly procedure involves the use of sawn-off sapphire substrates in the r-plane orientation with a-plane GaN overgrowth. This in contrast yields more of a biaxial orthorhombic strain and dislocation

problem, which may be remedied with multi-stage layer and temperature engineering, and certain device-level adjustments. [13 – 17]

This crystal quality-related drawback is the main reason why a-plane GaN on r-plane sapphire does not see much use in commercial applications and is relegated to mainly a research role. Firstly, electron mobilities rarely exceed 46 $cm^2\ V^{-1}\ s^{-1}$ for HEMTs. Secondly, unlike with fully-polar III-Nitride-based HEMTs, which have an almost constant sheet carrier density between several times 10^{12} to $2\times10^{13}\ cm^{-2}$, with non-polar HEMT structures, there is a trade-off between using high concentrations of modulation or delta doping for high sheet carrier density and charge carrier surplus scattering, which has a knock-on effect for electron mobility, so not over-doping or under-doping the HEMT layers is important [18]. This is due to a double effect of excessive dopants (mainly Si) causing parasitic 3D growth [19] and carrier-to-carrier scattering being significant, though carefully adjusting the silane or disilane flow rate can help with off-axis edge dislocations [20]. AlGaN Si dopant efficiency is higher than GaN for this plane, which is an advantage thanks to AlGaN being used as a barrier material [20, 21]. Labour-intensive patterned coalescent GaN overgrowth can achieve FWHM ratings of 250 arcsec, but is not practical on a large scale. [22, 23] Regardless, this makes a-plane GaN on r-plane sapphire promising for future non-polar HEMTs and integrated power/illumination devices.

Figure 6.2 is an illustration of the differences between modulation and delta doping simplified. Modulation doping has a moderate-to-thick barrier doped with donors for extra electron introduction into the transistor epitaxial structure, with the objective of separating the doped region from the actual channel. Delta doping has a very thin, almost infinitesimally small but ideally strongly doped barrier sandwiched in between two further barriers, named so because it closely resembles a Fermi-Dirac delta function.

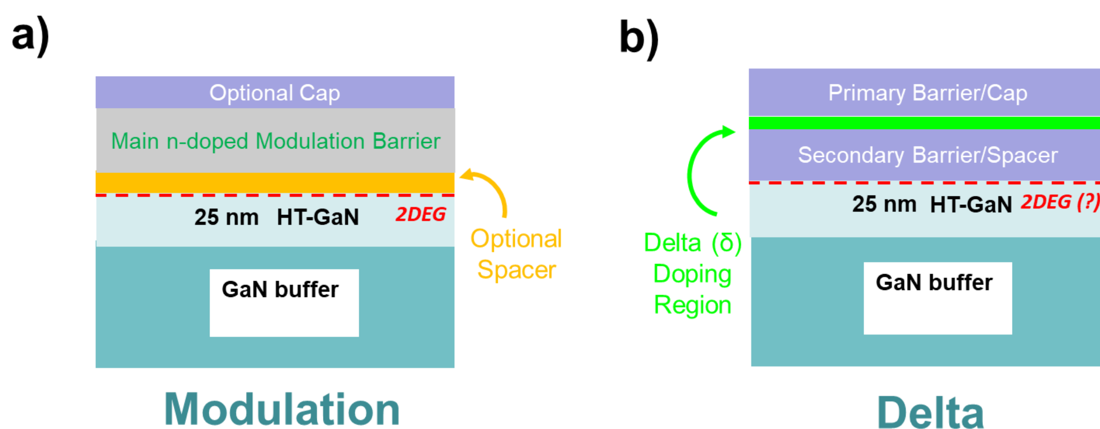


Figure 6.1: a) Modulation and **b)** Delta doping.

Thus, in this piece of work, we have conducted a comprehensive study of a range of different epitaxial growth templates and conditions using non-patterned a-plane GaN HEMTs on r-plane sapphire; from whose I-V and X-ray characterisation a set of conclusions about the current limitations of the aforementioned non-polar platform are to be reached.

6.2: Description of (11-20) Non-Polar GaN/AlGaN HEMT Templates

A range of samples, labelled Samples A-L, have been grown and characterised according to their electronic and other physical characteristics. All of the samples use a similar buffer growth system atop a nucleation layer of 300 nm AlN, but their follow-up layers, including actual buffer composition or single/dual layered growth, are different.

The growth process consists of a multi-stage MOVPE deposition on a sapphire substrate, sawn off to give an r-plane (1-102) termination and then growth of GaN is initialised on this end via the aforementioned AlN nucleation layer, giving the final buffer an a-plane (11-20) orientation. Afterwards, the successive layers are grown on this buffer across all of the templates, with disilane (Si_2H_6) flow for n-type doped layers, ($Ga(CH_3)_3$) in all cases and trimethylaluminium ($Al(CH_3)_3$) for AlN. Overgrown layers have a higher V-III ratio to encourage 2D growth on buffers. The full growth conditions and descriptions for each sample's course and aim of growth may be seen in Appendix B. Sample growth philosophies will still be given here, however, for the sake of cohesion within the Chapter.

The samples will be arranged in three sub-groups for the sake of organisation of results and discussion; the original set of modulation-doped samples with a doped AlGaN barrier, and GaN buffer overlaid directly on a HT-AlN buffer in a similar vein to Chapter 5; a series of samples with a secondary GaN buffer overgrown on a base of CMP-polished main buffer, whose composition will also be described, and a third set of newer-generation experimental samples with thick and thin barriers, and a quantum well channel. All samples apart from Sample K also have a HT-GaN layer that constitutes an AlGaN growth facilitator function, on top of usually being the channel layer itself.

6.2.1: Group 1: Classical Modulation Doped Samples, A to D

This group of samples consists of the original modulation doping ideas, as demonstrated in Figure 6.2a. All of these samples have a buffer thickness of 500 nm, with a V-III ratio that initially encourages 3D growth for the buffer, with remaining layers being grown in 2D.

Sample A is grown in a 'traditional' HEMT epitaxial layer stack fashion; a thin n-GaN cap, a doped barrier layer of AlGaN, and a 'high-temperature' thin layer of GaN for 2DEG build-up, to be induced by the barrier doping, atop a thick a-plane GaN buffer.

Sample B is a modulation-doped triple stack, consisting of a 10 nm doped layer of AlGaN sandwiched in between a thicker unintentionally-doped AlGaN cap and a thinner unintentionally-doped AlGaN 'spacer', intended to spatially separate the doped region from the GaN layer just atop an a-plane buffer. The principal idea behind this sample is that, in theory, by using a thicker cap, the backwards leakage towards the contact metals would be reduced; the spacer is kept a little thicker than usual with the aim of preventing surface state-related leakage and the barrier is kept reasonably thin to allow enough of a charge depletion into the HT-GaN layer, but also thin enough to allow for gate modulation.

Sample C is another of the modulation-doped samples, but with a much thinner cap and spacer intended to allow for better charge tunnelling from the central barrier into the HT-GaN layer while a thick barrier allows for a greater amount of charge accumulation within the barrier itself, to be depleted into it. The dopant flow rate (and therefore the doping concentration) and buffer/nucleation/substrate composition remains identical to the previous two samples.

Sample D is a hybrid modulation-doped sample not too dissimilar to Sample C, with the simple addition of a thin u-doped GaN cap to present smaller electro-potential barrier with especially Schottky contacts and u-doped GaN is still a good match for Ohmic contact metals, which in theory should improve the sample's gate modulatability and gate leakage.

Sample A	Sample B
	13 nm u-$Al_{0.3}Ga_{0.7}N$
2 nm n-GaN	10 nm n-$Al_{0.3}Ga_{0.7}N$
25 nm n-$Al_{0.3}Ga_{0.7}N$	3 nm u-$Al_{0.3}Ga_{0.7}N$
25 nm HT-GaN	25 nm HT-GaN
a-plane GaN buffer	a-plane GaN buffer
HT-AlN Nucleation Layer	HT-AlN Nucleation Layer
r-plane Sapphire	r-plane Sapphire

	2 nm u-GaN
2 nm u-$Al_{0.3}Ga_{0.7}N$	2 nm u-$Al_{0.3}Ga_{0.7}N$
22 nm n-$Al_{0.3}Ga_{0.7}N$	22 nm n-$Al_{0.3}Ga_{0.7}N$
1 nm u-$Al_{0.3}Ga_{0.7}N$	1 nm u-$Al_{0.3}Ga_{0.7}N$
25 nm HT-GaN	25 nm HT-GaN
a-plane GaN buffer	a-plane GaN buffer
HT-AlN Nucleation Layer	HT-AlN Nucleation Layer
r-plane Sapphire	r-plane Sapphire

Sample C **Sample D**

Figure 6.2a: Samples A to D in the 'Classical' category with their epitaxial structures.

6.2.2: Group 2: Secondary Buffer Samples, E to H

Figure 6.2b shows the collection of the second group of samples with secondary GaN buffers on top of a CMP polished primary a-plane GaN buffer, whose composition is identical to the previous samples. It is reckoned that the secondary GaN buffers would reduce buffer leakage.

Sample E is an iteration on Sample D with a different buffer composition in an attempt to tackle a buffer leakage issue that other non-polar HEMT samples of the same platform face. The secondary overgrown a-plane GaN buffer is also around 500 nm thick and its growth temperature is slightly raised to 1075°C. The secondary buffer is also 3D grown like the first, in an effort to help with its strain characteristics.

Sample F is one of a delta-doped nature. It is only 1 nm of AlGaN as a 'barrier', in between a thick unintentionally-doped AlGaN cap and a medium thickness AlGaN spacer separating it and a thin HT-GaN region. It too, has a dual-phase buffer. The overgrown buffer has slightly adjusted parameters across the board – a longer growth time at a slightly lower temperature and higher pressure, and with the V-III ratio of the aforementioned layer increased – with the hopes of more of a shift towards 2D growth flow rates but keeping a degree of 3D growth for strain adjustment. This secondary buffer is around 1.6 µm thick.

Following the same HEMT epitaxial stack formula as Sample C and the same buffers as sample F, but with a stronger doping in the AlGaN barrier and slightly adjusted cap and spacer thicknesses, Sample G is an attempt at addressing a concern with the previous samples; if their activated doping concentration was not high enough, and if the device current density could be improved still.

In consideration of the idea of an addition of a thin n-GaN cap above an epitaxial structure similar to Sample G, Sample H retains the dual-phase buffer template, but sporting a thicker HT-GaN layer like the earlier samples, also in an effort to find a solution to buffer leakage and HEMT drain leakage respectively. The doping concentration remains identical to G.

Sample E	Sample F
2 nm u-GaN	
2 nm u- $Al_{0.3}Ga_{0.7}N$	22 nm u-$Al_{0.3}Ga_{0.7}N$
22 nm n-$Al_{0.3}Ga_{0.7}N$	1 nm n-$Al_{0.3}Ga_{0.7}N$
1 nm u-$Al_{0.3}Ga_{0.7}N$	2.5 nm u-$Al_{0.3}Ga_{0.7}N$
25 nm HT-GaN	8 nm HT-GaN
Secondary GaN buffer	Overgrown GaN buffer
a-plane GaN buffer	a-plane GaN buffer
HT-AlN Nucleation Layer	HT-AlN Nucleation Layer
r-plane Sapphire	r-plane Sapphire

Sample E **Sample F**

Sample G	Sample H
	2 nm n-GaN
1.5 nm u-$Al_{0.3}Ga_{0.7}N$	1.5 nm u-$Al_{0.3}Ga_{0.7}N$
22 nm n+-$Al_{0.3}Ga_{0.7}N$	22 nm n+-$Al_{0.3}Ga_{0.7}N$
1.5 nm u-$Al_{0.3}Ga_{0.7}N$	1.5 nm u-$Al_{0.3}Ga_{0.7}N$
8 nm HT-GaN	25 nm HT-GaN
Overgrown GaN buffer	Overgrown GaN buffer
a-plane GaN buffer	a-plane GaN buffer
HT-AlN Nucleation Layer	HT-AlN Nucleation Layer
r-plane Sapphire	r-plane Sapphire

Sample G **Sample H**

Figure 6.2b: Samples E to H in the Secondary Buffer category.

6.2.3: Group 3: New Generation Samples, Thick Barrier/Cap and Quantum Well

Figure 6.2c shows a collection of the 'new generation' samples experimenting with higher doping concentrations (indicated by n+ and n++ respectively), thick barriers, a simulation-optimised thickness of 12 nm and a quantum well idea with 4 nm GaN in between the doped barrier and a secondary pre-buffer barrier. All of these revert back to the singular 500 nm 3D-grown a-plane GaN buffer at the higher pressure used for samples F to H, and a growth temperature tuned down to 1060°C.

Sample I, possessing a very thin cap and spacer surrounding a thick strongly-doped barrier, is also an effort to improve the current density of the devices grown on this set. The thick barrier is theoretically meant to present a greater amount of charges to the transistor channel. It was to be seen whether thick barriers at high doping concentrations mean that most of the charge may not be contained within the intended HT-GaN layer and instead will either leak from the channel or 'short

circuit' the drain and source contacts via the barrier itself, which also causes a lack of proper gate modulation of current.

Sample J is a sample of a cap/secondary top-level barrier composition that is a hybrid of the previous attempts – the thin n-GaN cap combined with a thicker AlGaN secondary barrier and a thin spacer encasing a moderately thick, but strongly doped, AlGaN primary barrier. This is the first of the series to have the primary barrier aluminium composition dropped to ≈ 25% from ≈ 30%.

Sample K is the quantum well GaN channel sample in question. Using the principle of Sample J but without the top-level GaN cap and in its stead comprising of a buffer barrier encircling a thin HT-GaN layer in between itself and the usual thin spacer, it was to be seen if a 4 nm HT-GaN layer essentially grown into a quantum well would have helped it in terms of 2DEG mobility as well as observing how that would affect the sheet carrier density overall. All AlGaN layers were kept at an alloy percentage of 25% Al.

Sample L is similar to Sample J, but with all AlGaN ratio being ≈ 25% and a 1 nm GaN cap that is unintentionally-doped. The lack of intentional doping was proposed to reduce source/drain leakage.

Sample I
1 nm u-$Al_{0.3}Ga_{0.7}N$
26 nm n+-$Al_{0.3}Ga_{0.7}N$
1 nm u-$Al_{0.3}Ga_{0.7}N$
25 nm HT-GaN
a-plane GaN buffer
HT-AlN Nucleation Layer
r-plane Sapphire

Sample J
1.5 nm n-GaN
15 nm u-$Al_{0.3}Ga_{0.7}N$
12 nm n++-$Al_{0.25}Ga_{0.75}N$
1 nm u-$Al_{0.25}Ga_{0.75}N$
25 nm HT-GaN
a-plane GaN buffer
HT-AlN Nucleation Layer
r-plane Sapphire

Sample K
15 nm u-$Al_{0.25}Ga_{0.75}N$
12 nm n++-$Al_{0.25}Ga_{0.75}N$
1 nm u-$Al_{0.25}Ga_{0.75}N$
4 nm HT-GaN
20 nm u-$Al_{0.25}Ga_{0.75}N$
a-plane GaN buffer
HT-AlN Nucleation Layer
r-plane Sapphire

Sample L
1 nm u-GaN
15 nm u- $Al_{0.25}Ga_{0.75}N$
12 nm n++-$Al_{0.25}Ga_{0.75}N$
1 nm u- $Al_{0.25}Ga_{0.75}N$
25 nm HT-GaN
a-plane GaN buffer
HT-AlN Nucleation Layer
r-plane Sapphire

Figure 6.2c: Samples I to L in the Experimental category.

6.3: Experimental and simulation methods

6.3.1: Fabrication of HEMTs, SBDs, TLM structures and Buffer Contacts

The fabrication of the HEMT devices takes place in a procedure as follows: Each device is isolated with the etching out of a deep mesa after a UV photolithography process to expose all of the buffer except the device area, and an etch depth of about 300 nm through selective epi removal is achieved with the use of ICP-RIE (Inductively Coupled Plasma Reactive Ion Etching). Once the device sites are determined, a second set of process windows are opened through photolithography for the source and drain metals on the device mesa. The process windows are then used to deposit Ti/Al/Ni/Au in a 20 nm/150 nm/50 nm/50 nm ratio in a vacuumed evaporator to form Ohmic contact metals for the drain and source. Once metal deposition takes place, the devices are rapidly thermally annealed (RTA) for optimal Ohmic contact formation, in N_2 ambient for 30 s and at 850 degrees Celsius. The process is repeated for the gate Schottky metal, Ni/Au, in a 50/150 nm ratio. The device is left to cool down before passivation with Si_3N_4 as a regrown layer via PECVD (Plasma-enhanced Chemical Vapour Deposition). Finally, the extraneous passivation layers on contact sites are removed.

Figure 6.3 shows the test structures used in this work, with top-down view of the TLM structure, a top-down and 3D cross-section view of the SBDs and a top down/3D cross-section view of the HEMTs used, as well as the Schottky pads used for buffer leakage testing.

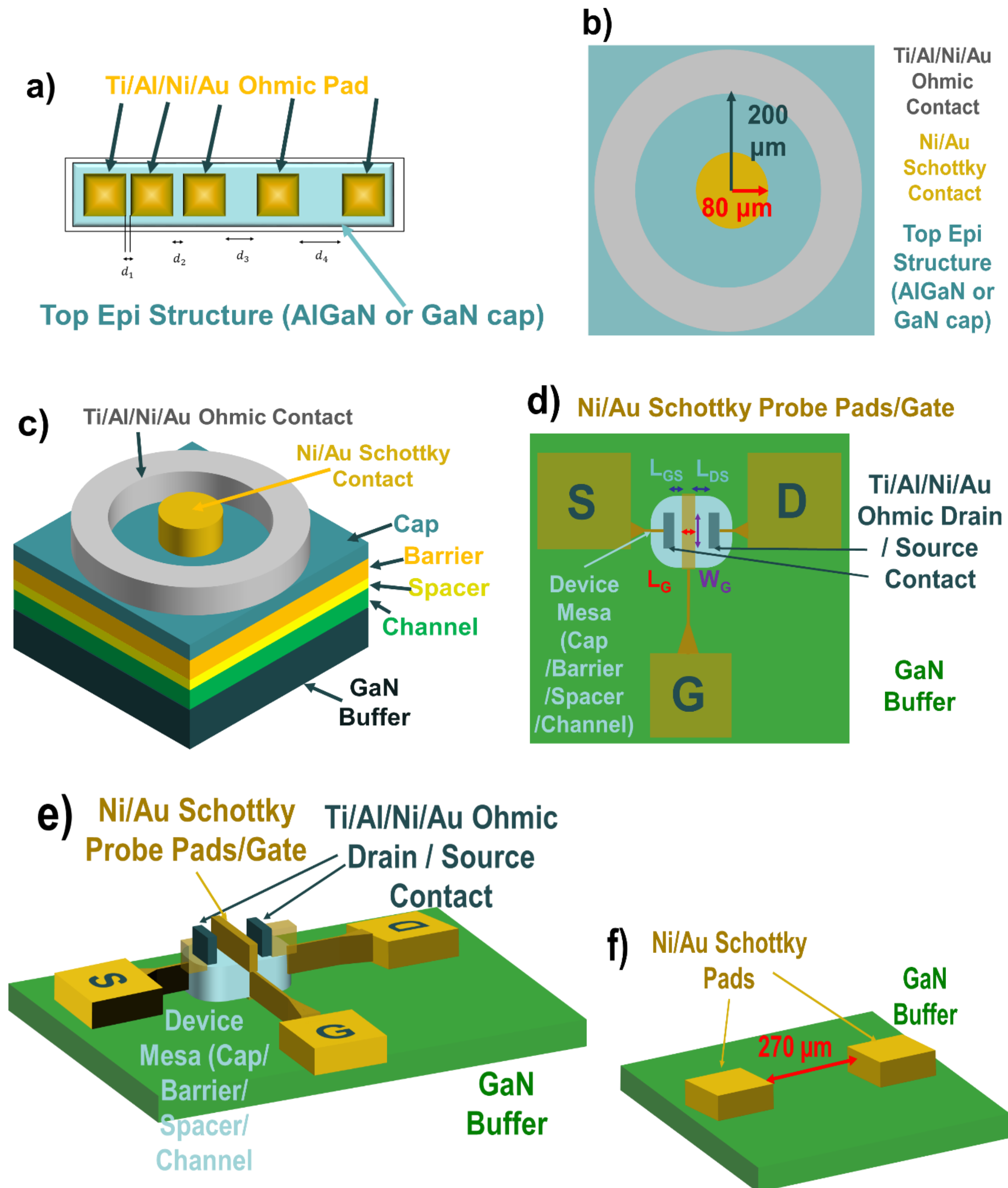


Figure 6.3: a) A top-down view of the TLM structure; **b)** A top-down view of the SBD; **c)** a 3D cross-section of the SBD with a genericised epitaxial structure; **d)** A top-down view of the HEMTs; **e)** a 3D cross-section of the HEMTs, genericised and **f)** a buffer contact structure.

The same process masks for the HEMT devices are also used to mesa isolate Schottky Barrier Diode (SBD) and Transmission Line Measurement (TLM) structures, and deposit both Schottky and Ohmic contacts on the SBD structures and only increasingly spaced Ohmic contacts to gauge Schottky and Ohmic contact effectiveness respectively, with identical metal and passivation thicknesses for each. The buffer leakage structures are simply deposited Ni/Au on two separate mesas.

6.3.2: 1D Schrödinger/Poisson Epitaxial Structure Solver

Special thanks to Michael Grundmann for the BandEng program [24] which has helped with theoretical 1D Schrödinger-Poisson solutions of epitaxial layers to help further our understanding of non-polar HEMT epitaxial stacks.

Generalised variations with Al percentage in the barrier, doping concentration for the GaN cap and the AlGaN barrier were performed using BandEng. The program is pre-equipped with a materials and simulations rules for GaN and AlGaN, which are loaded into the program and the individual layers defined in Ångströms. The simulation precision is 1 Å maximum and 10 Å (1 nm) default; however, 2.5 Å is chosen instead for a compromise between precision and fast simulations.

Sample A is used as a default structure due to resembling the 'traditional' c-plane HEMT structure the most but still having a GaN cap whose thickness is minimal. Even with this stated, the exact epitaxial structures under scrutiny using Sample A as the template will still be re-drawn for clarification purposes and the graphs for Poisson-corrected electron concentration graphs as well as the band diagrams will be re-drawn to clarify those as well.

The Schottky-Mott Rule is then used to set the contact height for metals. Normally, entering the simulation parameters as they are, will make the program assume a neutral contact (0 eV), but by using GaN's electron affinity, for example, on a Ni/Au Schottky contact, will yield 1.1 eV. A properly activated Ti/Al/Ni/Au with Ti_xN complexes (ϕ_m of 3.74 eV) in contrast will be -0.36 eV in theory and will be the adopted value (though practically it will have a small positive Schottky barrier) [25, 26].

6.4: Results and Discussion

6.4.1: Electrical Characterisation

6.4.1.1: Hall Effect Measurement Results

Table 6.1 shows the summary of Hall Effect measurements on the samples, split into Group 1, Group 2 and Group 3 as elaborated in 6.3.1. For the sake of keeping the table together, these will be clarified in text instead. As many samples as available wafer pieces were allowing were used in these tests. The Hall Effect setup comes pre-equipped with measurement and calculation tools based on van der Pauw principles to obtain sheet resistivity (R_{Sh}), sheet carrier density (n_{Sh}) and electron mobility at 300 K (μ_n).

Sample	R_{sh} [Ω/sq]	n_{Sh} [cm^{-2}]	μ_n, 300 K [$cm^2 V^{-1} s^{-1}$]
A (Grp 1)	5220	6.40×10^{13}	18.697
B (Grp 1)	2662.617	1.306×10^{14}	17.946
C (Grp 1)	757	1.921×10^{14}	42.941
G (Grp 2)	6739	1.501×10^{13}	34.272
H (Grp 2)	1007	1.587×10^{14}	39.061
I (Grp 3)	2784	1.39×10^{14}	16.150
J (Grp 3)	3348	1.98×10^{14}	9.401
K (Grp 3)	66210	1.234×10^{12}	76
L (Grp 3)	3470	2.31×10^{14}	7.774

Table 6.1: A summary of all the Hall characterisation of samples A, B, C and G to L. Hall measurements taken at 300 K.

Hall measurements on Ohmic clover leaf contacts were performed at 300 K and with a dual-mode (North (N) to South (S) and S to N) magnetic field of a magnitude of 0.556 T. The applied current is 0.1 mA for consistency, but it is more important to observe and interpret the resultant Hall voltages. Hall measurements cannot be taken at face value if the sample has leakage anywhere from the main layer where the device channel is located because charge carriers will move more omnidirectionally, but will nevertheless help in understanding the relationship between doping, sheet density and lateral mobility and how one type of doping scheme will influence the sheet density.

Despite increasing dopant flow rate over the previous samples, interestingly, the sheet density of Sample G remains lower than the rest and with a higher mobility. This could be its source-side leakage, because as to be seen in 6.4.1.4, it has a significant degree of Ohmic contact behaviour with V_{DS} even for voltages it is supposed to be pinched off by gate voltage, thus this being one theory for its lack of complete pinch-off, although there may also be dual barrier-channel conduction due to its thickness and doping concentration (bottom/trough of the AlGaN conduction band must be modestly above Fermi level to keep lack of barrier conduction [16]), or the Hall testing contact's relative position on the wafer (as sample quality varies with position on the wafer).

Sample C is the second best for mobility, whose sheet resistivity is nominally the best, and mobility is superior to most the other samples. However, as there is a clear lack of gate modulation as to be seen on Figure 6.3, the most likely explanation is that doping-induced excess electrons from the barrier never tunnel through to the other epitaxial layers. A thinner barrier in this arrangement may lead to gate modulation and good mobility. The best mobility, however, is demonstrated by Sample

K, at 76 $cm^2\ V^{-1}\ s^{-1}$, the experimental quantum well-style sample, at the expense of higher sheet resistivity. Sample L is over-doped and has an excessively thick AlGaN layer on top of the barrier, which is also reflected in its very low mobility, and having a GaN cap for this architecture is detrimental. The same is also true of Sample J. Sample I has a doped barrier that is too thick, so also has poor mobility and high sheet density.

6.4.1.2: Methodology and Summary of Other Electrical Measurements

The I-V measurements were performed using a probe and microscope bench interconnected with a Keithley 2612B source meter unit, to be able to get the statistics for each individual device. These are coded according to which row and column they occupy in reference to their device die (e.g.: R1C3 being row 1, column 3). The I-V curves cover gate-to-source voltages and drain-to-source voltages of -7 to 1 V and 0 to 10 V respectively. The full I-V curves show that only Samples A, D, E and G demonstrate some form of transistor-like behaviour and the others downwards gate-modulating, in a sense, but otherwise following a linear-like plot without any proper saturation.

Transconductance curves are obtained for Vds = 10 V and Vgs from -7 to 1 V as a measure of relative change in current per unit change in gate voltage and in HEMT devices, which should ideally resemble a bell curve or a similar shape. Right away, we can see that the samples A and E work well, as well as Sample I, if not ideally following this pattern. Sample D seems to transition up and down a lot by gate input but otherwise follow a similar pattern, and Sample G is where it is seen that there is a large negative Gm followed by a small positive peak, then to zero and back upwards, due to the sample's very large transistor-level leakage. The other samples show unstable increases, starting at large negative values too, alluding to their lack of proper gate modulation, and pinching off that can easily be their barriers short-circuiting, except Sample F with almost no current flow at all, due to its thin barrier and exceptionally thick cap.

Transmission Line Measurements are used as a way to determine the Ohmic contact performance of the samples, their usual current flow paths, contact and sheet resistivity and any glaring leakage characteristics. With the exceptions of Sample H, J and K and L on a very short path, all of them have linear TLM patterns, meaning most of their limiting factor must be coming from the epitaxial structure and the Schottky contacts, and thus their vertical, not lateral, electron movement that is the limiting factor. Sample H behaves in a pseudo-Schottky manner (could be a post-process effect or Fermi-pinning on the Ohmic contacts due to its GaN cap) and Samples J and K have large source-side leakages, J being on the larger side as similar to H it has a GaN cap. These results also suggest the possibility of over-doping.

To get a complete picture of transistor behaviour, individual Schottky contact testing is necessary, as the combination of Schottky and Ohmic regions of the channel make up complete transistor behaviour with depletion and accumulation regions. -20 V to 10 V are the voltages used for the devices as they cover the reverse and forward bias behaviour in standard operation. Sample A does well and so do Samples D, E and G, to an extent. D is the best thanks to the unintentionally-doped GaN cap. Given Sample G's otherwise well-conforming Schottky tests (apart from one cell) on top of its normal, linear Ohmic operation, its problem is further confirmed to be not down to the cap layer in isolation, nor the buffer.

Sample B does well in terms of device leakage performance, but its forward current does not increase exponentially as according to Shockley's Equation. Sample C, operates in both large reverse voltages in a roughly linear regime and exponentially in forward voltages, further contributing to the idea of its barrier short-circuiting. Sample F doesn't scale well with increased voltage and Sample H suffers a similar issue to that of Sample C, with the exception of its current not increasing with as large of an exponential factor as it due to its GaN cap on top of a secondary barrier.

Buffer leakages were also measured across two metal pads, using Schottky contacts, deposited via etching 300 nm down into the GaN buffer to measure the current flow at this level down the epitaxial structure. The pads are separated by 270 µm. The measurements are between 0 and 20 V due to equipment and safety limitations, and also because this covers the usual operational voltages of the devices.

Samples A, D, F and G have their leakages in the nano or even several hundred picoamp sort of range, yet again confirming that leakage in Sample G must come from the top-level epitaxial structure, likely the balance between the thick doped barrier and thin cap, and not the buffer nor contacts, making buffer leakage a non-issue. Sample E's leakage is significant, but not enough to influence the device operation as it is still in the microamps. Samples B, C and H do have strong leakage in the several hundred µA or even mA range however. Sample B and C's leakages cannot be explained by crystal quality alone due to similar FWHM values, as on Table 6.2, to Sample G. The dual buffer formula does seem to lead to significant improvements in leakage characteristics.

6.4.1.3: Group 1 Results

This section explores the detailed device characteristics of Group 1 to hopefully shed some light on the results for the samples within Group 1 and explain the performances of each device group in reference to their epitaxial structures.

HEMT Device I-V Curves

The I-V curves of Group 1 devices, as seen in Figure 6.4, can reveal some important results relating to the epitaxial structures of the Samples, and also in relation to their optimisation. Both Samples A and D have thin GaN caps, one n-doped and one u-doped, and both samples have 25 nm AlGaN layers in total, with all 25 nm of A being n-doped and 22 nm for Sample D being n-doped, with 2 nm as a pre-cap barrier and 1 nm spacer.

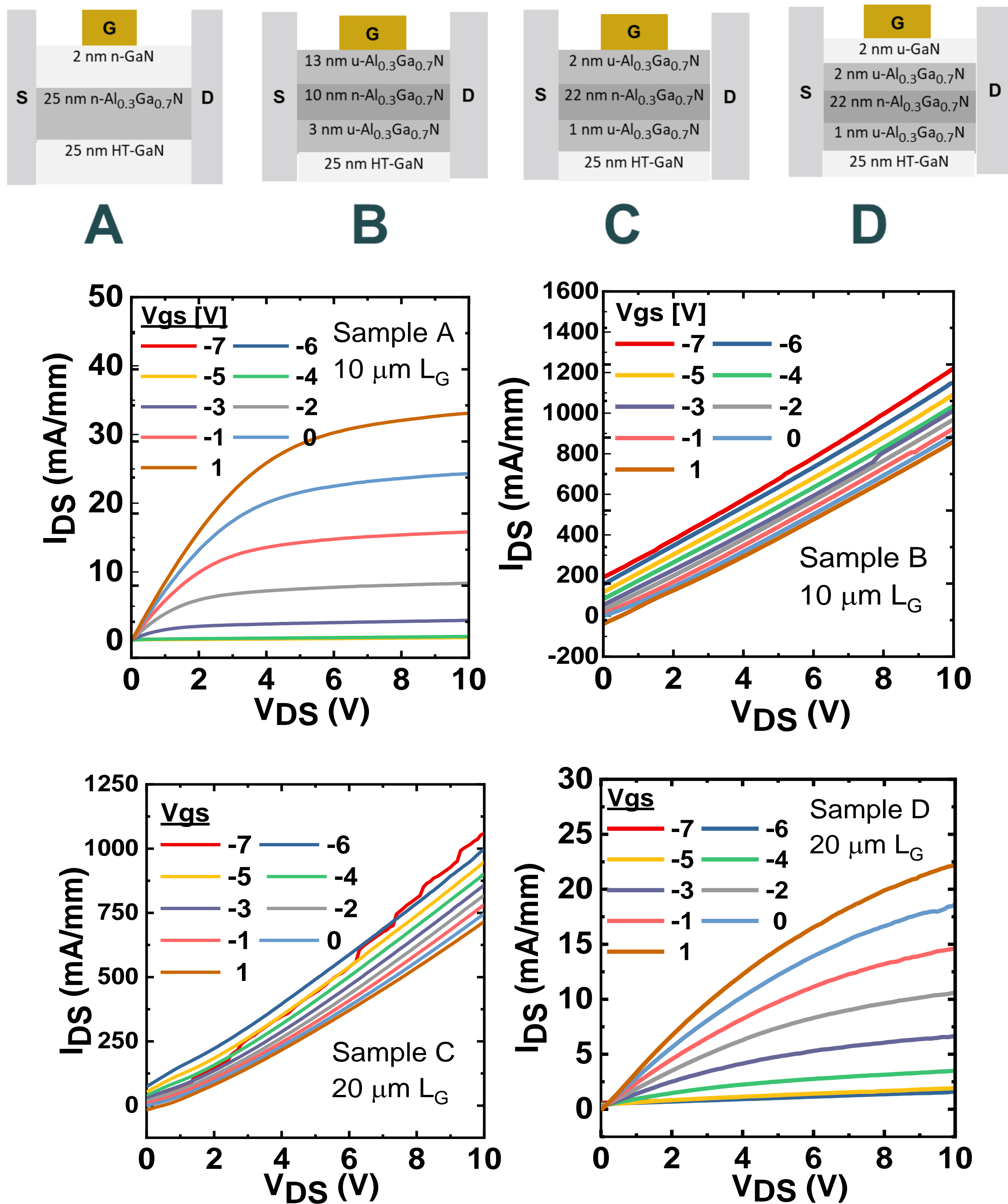


Figure 6.4 a) to h): The fabricated HEMT devices and the I-V curves of Samples A to D.

Samples B and C do not gate modulate at these test voltages in a manner expected of transistors, but rather purely Ohmic behaviour just translated downwards every unit of V_{GS}, likely alluding to their AlGaN caps, as a Schottky contact to AlGaN will have a higher barrier height. At this barrier thickness and doping, it is likely that charge depletion does make the band cross over the Fermi level ‘prematurely’ by barrier length, thus leading to barrier conduction. A thinner AlGaN barrier and cap may work.

HEMT Device Transconductances

Figure 6.5 is a collection of the transconductance measurement results of Group 1. It is quite clear from these results that Samples A and D get fairly close to the expected ‘bell’ shape for this curve, where they peak at a given V_{GS} point, for a fixed V_{DS}. Samples B and C have large negative transconductances that show unstable increases, alluding to not only improper gate modulation, but also significant barrier level conduction. Sample B’s 3 nm spacer and 13 nm barrier may be too thick.

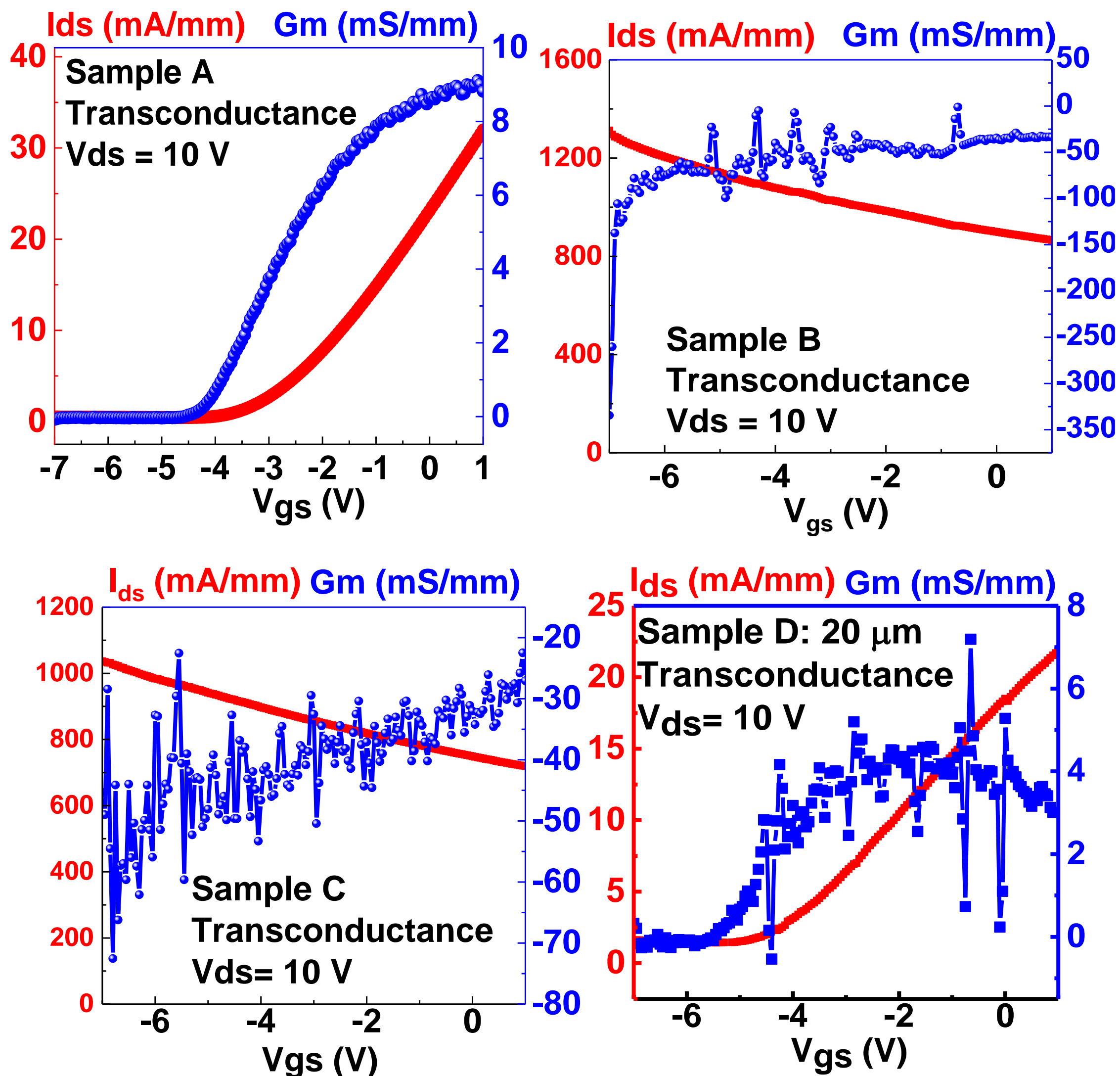
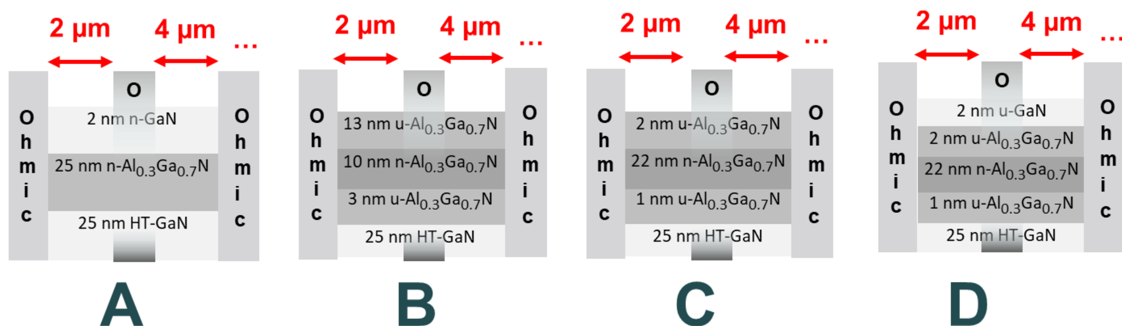


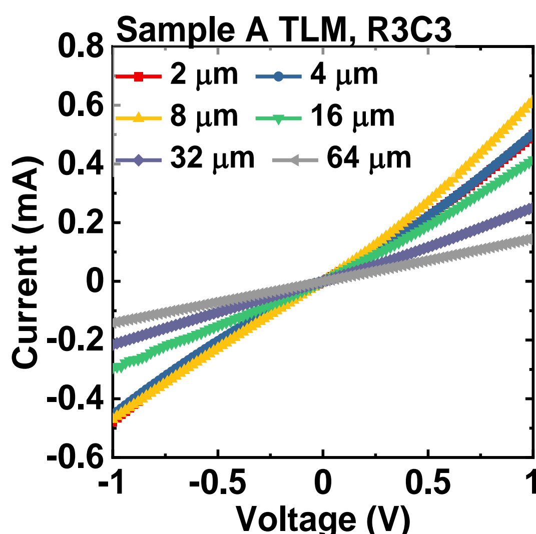
Figure 6.5: a) to d) Transconductance curves of samples A to D.

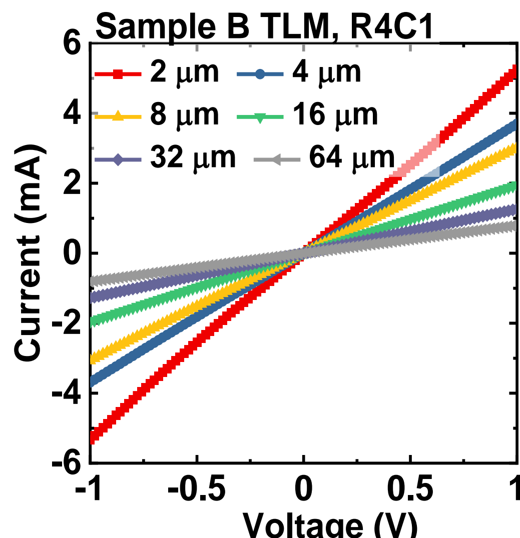
Moreover, it is evident that Sample C has significant barrier leakage from the oscillating increases in gm and decreasing Ids with increasing Vgs. The interesting part is Figure 6.6d, where the pattern resembles a more oscillating and translated version of Sample A's. Given its otherwise similar composition to Sample A, except replacing the n-GaN cap with a u-GaN one and instead of the entire barrier being doped, it has a 2 nm cap spacer and a 1 nm primary spacer, it is possible one of the two works against the Sample, but still displaying proper gate modulation.

TLM Device I-V Plots

The TLM data should show the purely Ohmic contact characteristics of each of the sample in this group. If increasing Ohmic distancing starts to lead to a less-than-linear result, then this indicates that the sheet charges may be improperly induced. Sample A works well as expected, but so does Sample B, meaning that the problem for Sample B is mainly the lack of proper Schottky gate modulation. Sample C is where the linearity starts to break and there is a very sharp increase in observed current from 4 to 2 μm spacing, and a moderately sharp increase from 8 to 4 μm. Since it behaves fairly normally as the distancing increases, this may be as a result of the contact resistivity between the contact and the semiconductor, rather than the sheet resistivity of the semiconductor itself. Sample D has a much less prominent version of this as according to the data.







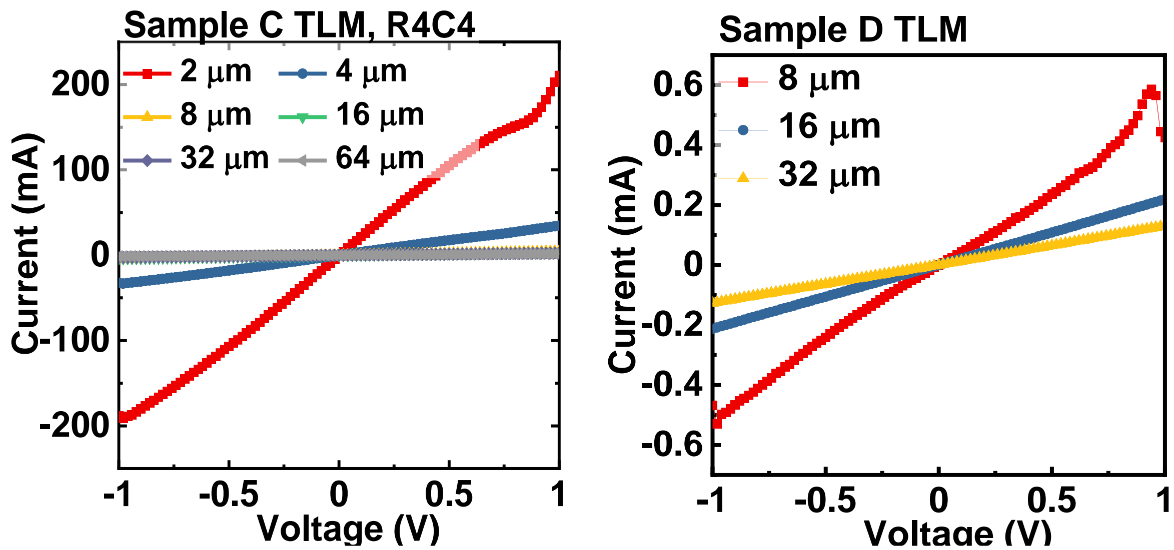
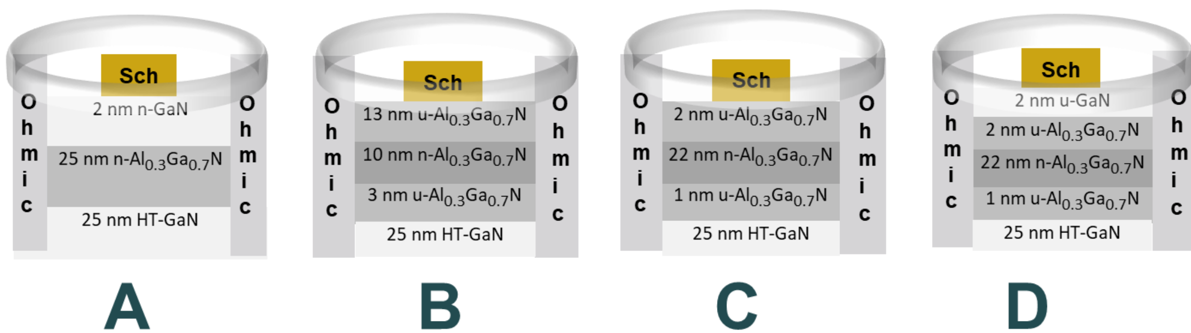


Figure 6.6 a) to h): The TLM structure cross-sections and TLM plots for Samples A to D.

SBD Device I-V Curves

Figure 6.7 shows the Schottky Barrier Diode test for the Samples A to D in order to show how the Schottky contact performs and to ascertain where the gate modulation problems arise from, sometimes from multiple locations on the wafer, using a row/column system based on the device die. Sample A performs well outside of the fourth row; it was therefore established that this part of the wafer was just leakier than general since transconductance measurements seem to imply that this sample does not suffer from major source leakage. Sample B also holds up, except that forward biases do not seem to generate an exponential increase in line with Shockley's Equation. Sample C is very leaky throughout, ≈ 30 mA for both large positive and negative biases, which partly explains its lack of gate modulation. Sample D behaves mostly as expected from a Schottky Barrier Diode, very similarly to 3/5 devices on Sample A.



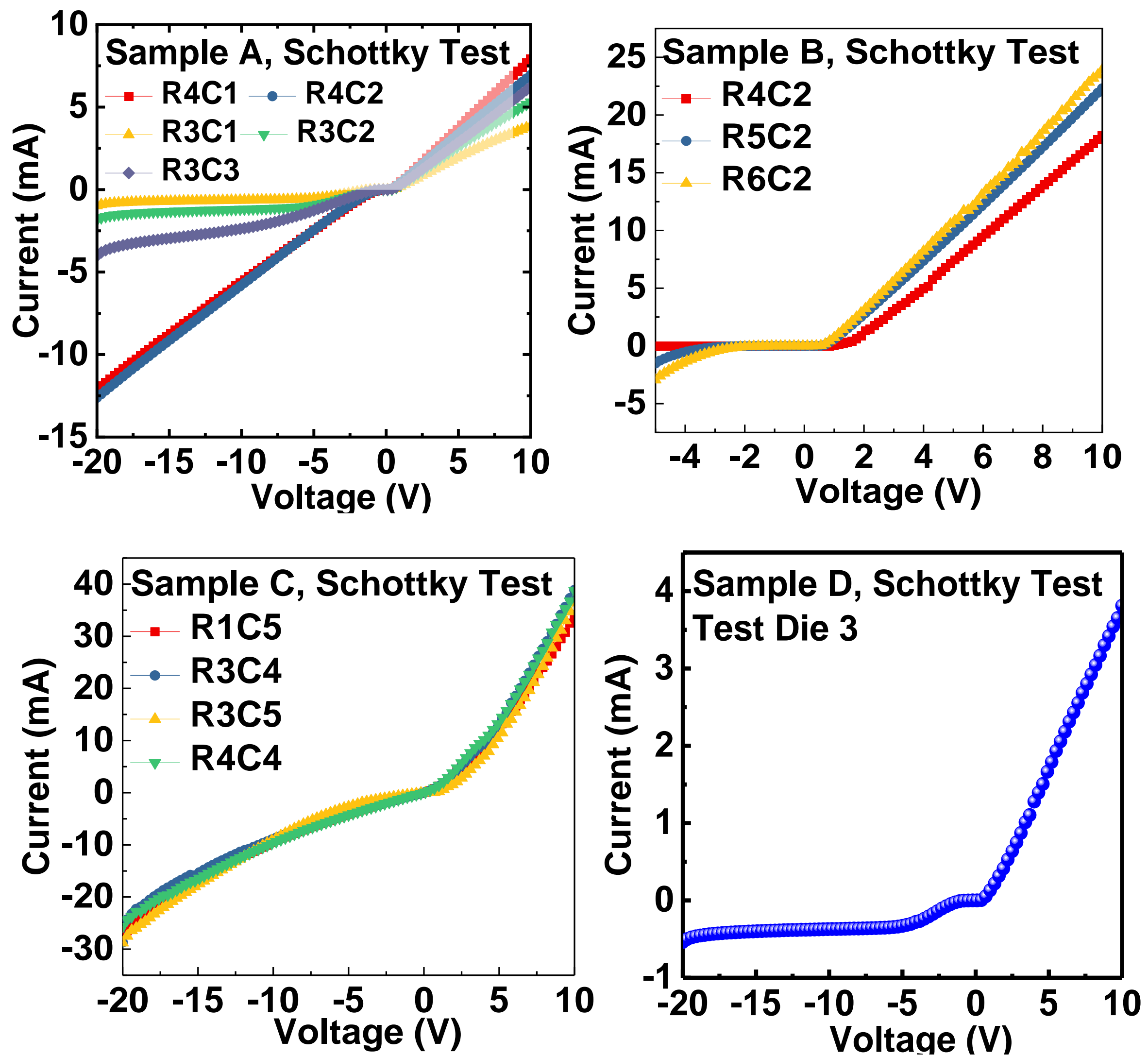


Figure 6.7 a) to h) Schottky Barrier Diodes and their I-V plots for Samples A to D.

Buffer Leakage Structure I-V Curves

Finally, for each group, the buffer leakage will be analysed, as this is one final part of the total device leakage that can skew the results of samples that would normally work well as HEMT devices, since, the Ohmic contacts are entrenched deep enough to extend to the buffer and also some of the channel charges may leak into the buffer. Samples A and D perform well, with leakages in the 10s of nA or even 100 pA range. Sample B is quite leaky, despite similar buffer formula to the samples in this group. Sample C is also leaky in the buffer, which may partially explain the different results observed with Sample G in Group 2, which in theory should behave similarly to these two.

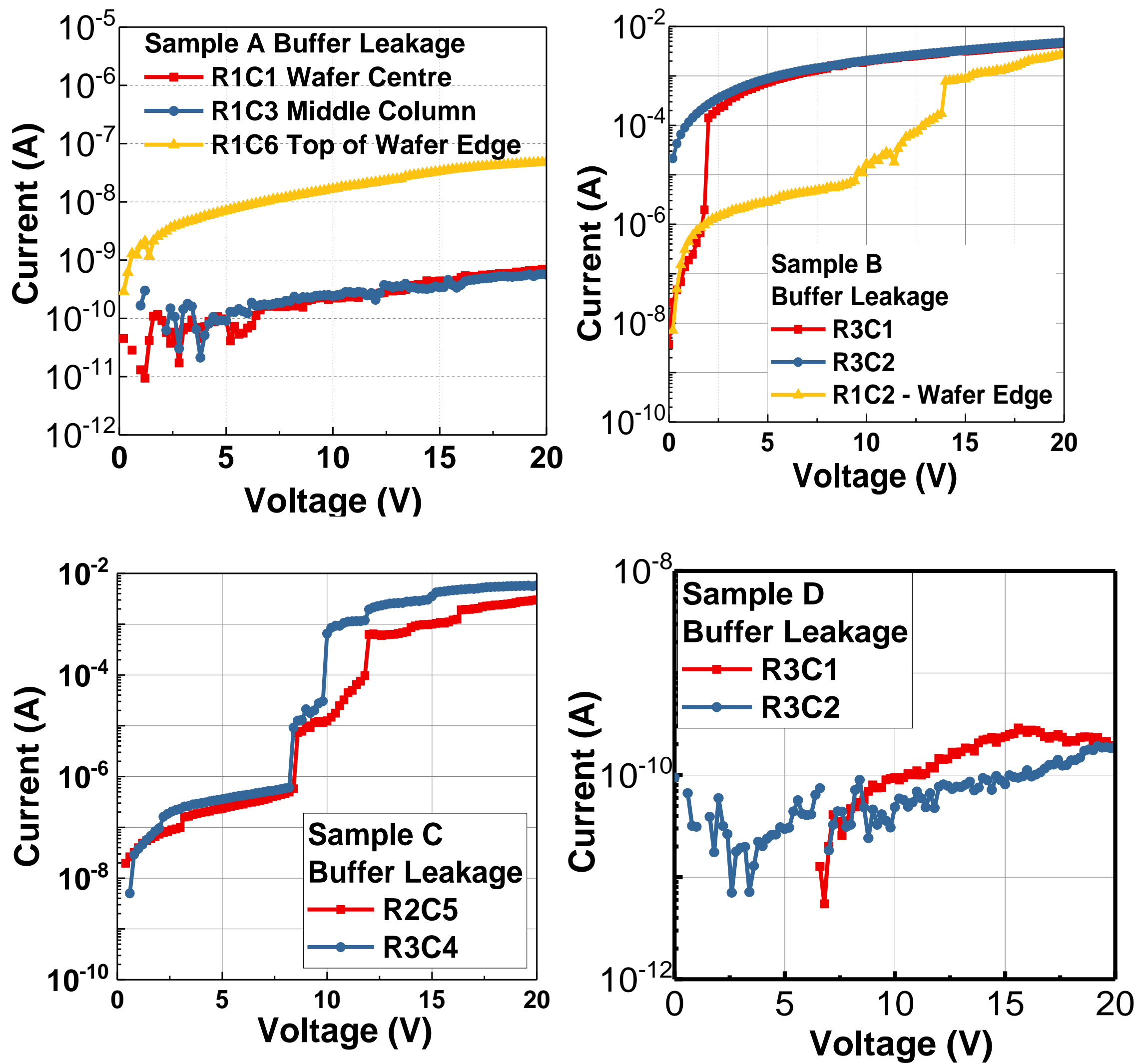


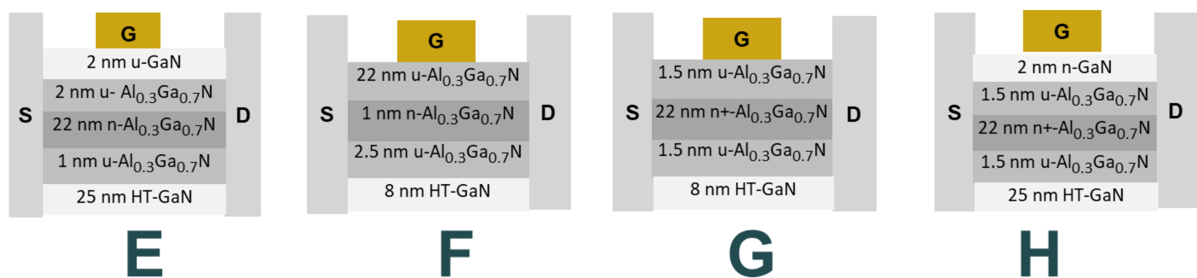
Figure 6.8 a) to d): Buffer leakage results for Group 1.

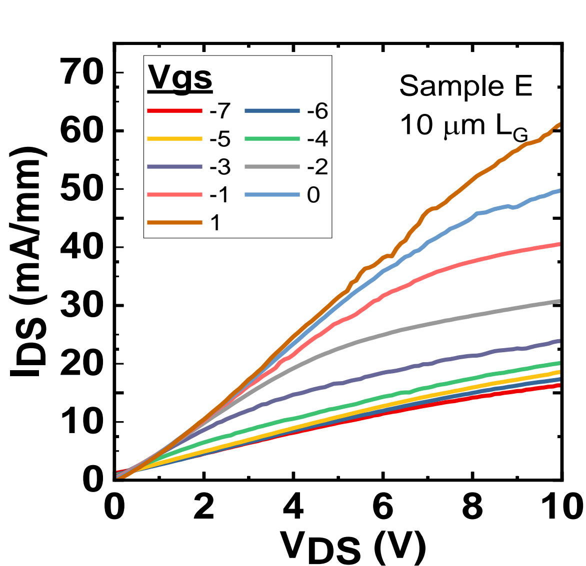
6.4.1.4: Group 2 Results

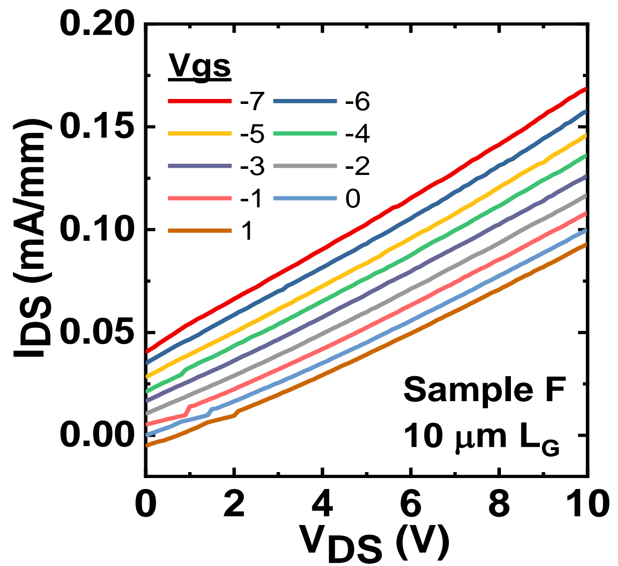
HEMT Device I-V Curves

In summary, samples E and G show clear gate modulation but not complete channel pinching off at the expected voltage ranges, whereas F and H do not show any transistor behaviour at all, instead just translated Ohmic contact behaviour. We believe, at least with the archetype of samples that principally demonstrate a linear I-V plot instead of the transistor behaviour, there are significant levels of barrier short-circuiting going on, so most of the free charge carriers flow through the presumed barrier, which is certainly not an impossibility if the activated doping concentration exceeds the order of a couple times 10^{19} per cm^3 as per 6.4.3 simulations; whereas delta doping as with Sample F simply does not work at the dopant flow rate for the sample, producing the worst result for both [lack of] gate modulation and current density. There is simply not enough charge depletion with such a thin barrier at moderate doping concentrations.

Sample G is a curious case as at the doping concentrations and given its doping scheme (with increased doping too), it should demonstrate similar behaviour to samples B, C, F and H. It is believed, given its relatively high two-dimensional leakage – both towards the source and the drain at certain gate voltage values – but otherwise decent transistor curve caused by a degree of pinch off, the reason that it gate-modulates is that the cap is thin enough and potentially high enough due to the Al composition, to present a high enough barrier of entry for electrons, which translates to a greater degree of electron confinement in the intended GaN channel layer – all other similar samples had either excessively thick caps or imbalance in spacers. Its thinner HT-GaN layer should not factor into the surface 2DEG density. Its complete set of results including buffer leakage should help shed some light on the difference it has with similar samples.







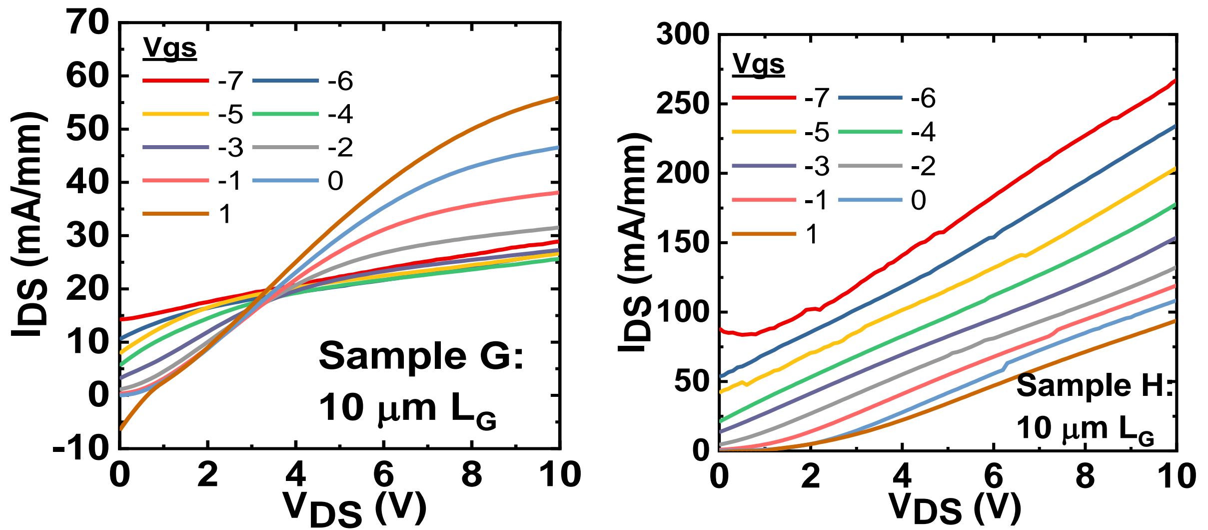


Figure 6.9 a) to h): Cross-sections and performances of Group 2 HEMTs.

HEMT Device Transconductances

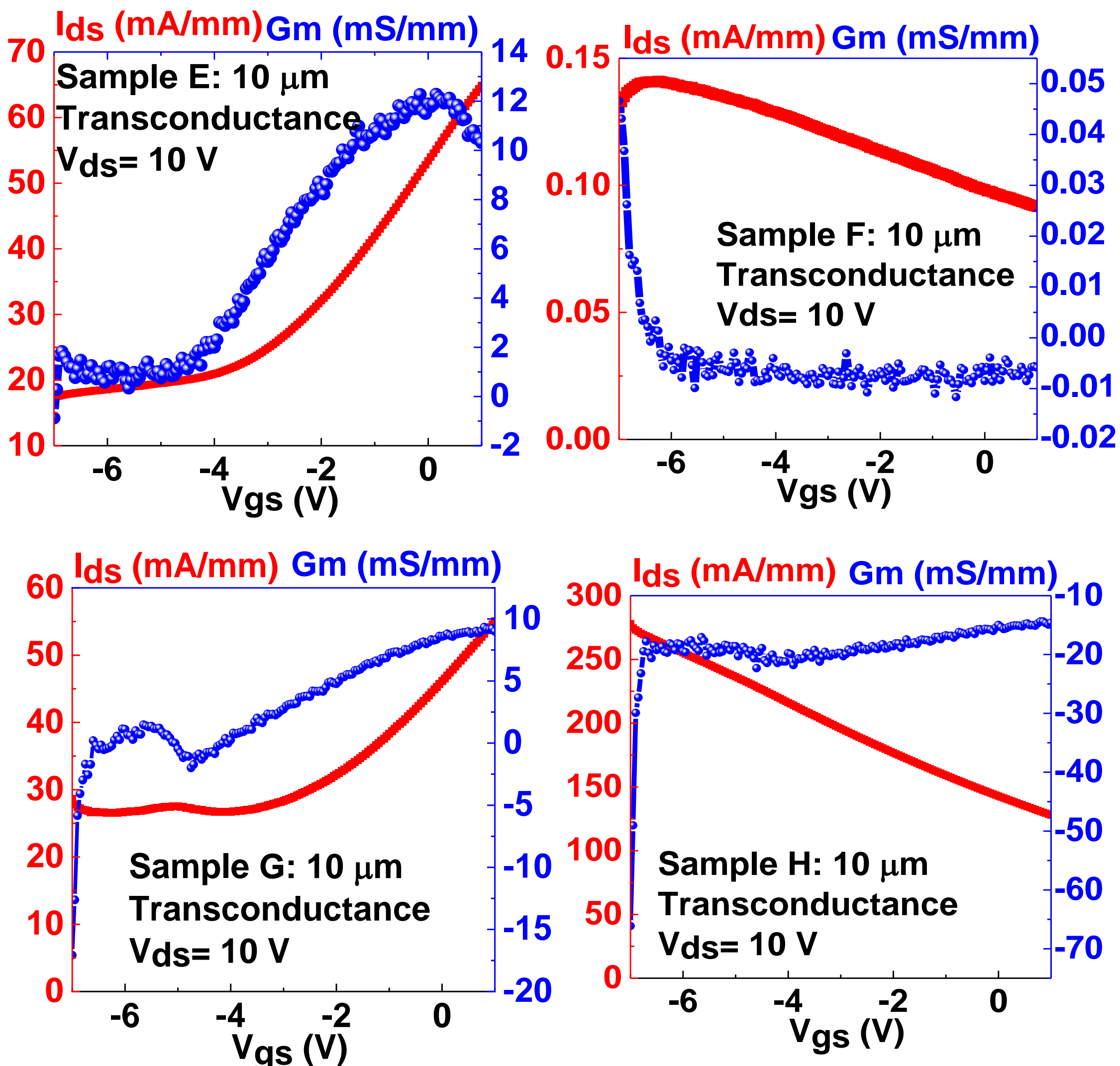


Figure 6.10 a) to d): HEMT Transconductance results for Group 2.

Figure 6.10 shows a collection of transconductance curves for Group 2. Sample E's gm curve is exactly as one would expect, with a slight caveat of a negative trough at Vgs = -7 V. Sample F shows almost exactly the opposite behaviour to a transistor in terms of its gm curve. Sample G is pretty much as expected up until -4 V, where it has a slight peak and then it decreases into the negatives. Sample H is negative throughout, akin to a smoother version of Sample B results. Therefore, one can ascertain that the likely reason for Sample E and G leakage is from either the barrier or parasitic charge leakage during gate voltage decreases towards the would-be pinch-off point instead of the intended 2DEG.

TLM Device I-V Plots

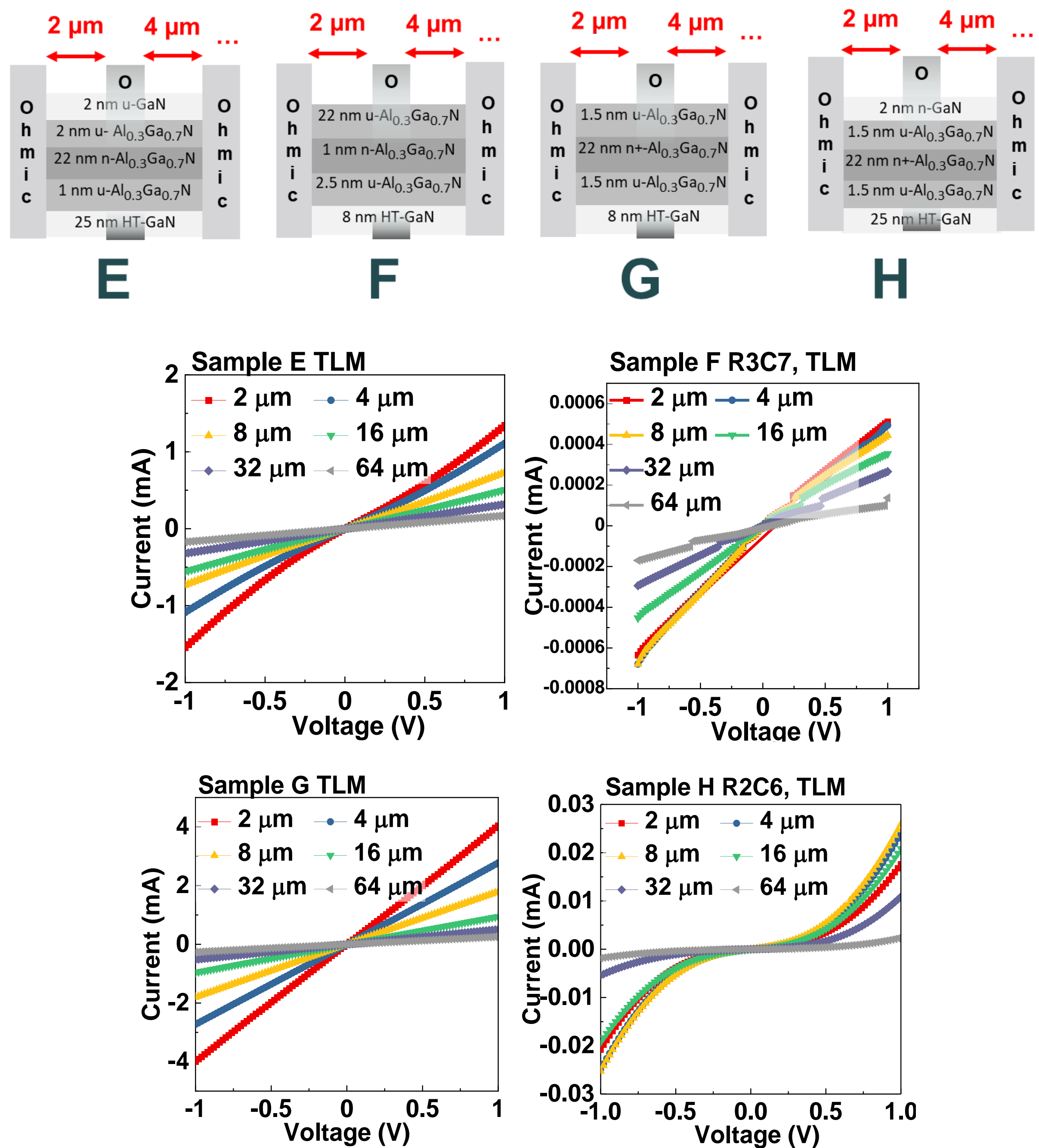


Figure 6.11 a) to h): TLM structure cross-section and results for Group 2.

Figure 6.11 shows a collection of TLM plots for Group 2. In general, this group maintains its linear Ohmic performance over the course of contacts spaced by a factor of 2. The only exception is Sample H, which tends towards a dual pseudo-Schottky conduction style the closer the contacts get. This cannot be explained by a small positive Schottky barrier when contacted by AlGaN either, because none of the other samples which have AlGaN show this behaviour. The likely reason may be buffer leakage, or conduction via the n-GaN cap and barrier with increased doping.

SBD Device I-V Curves

Figure 6.12 shows a collection of SBD plots and structures for Group 2.

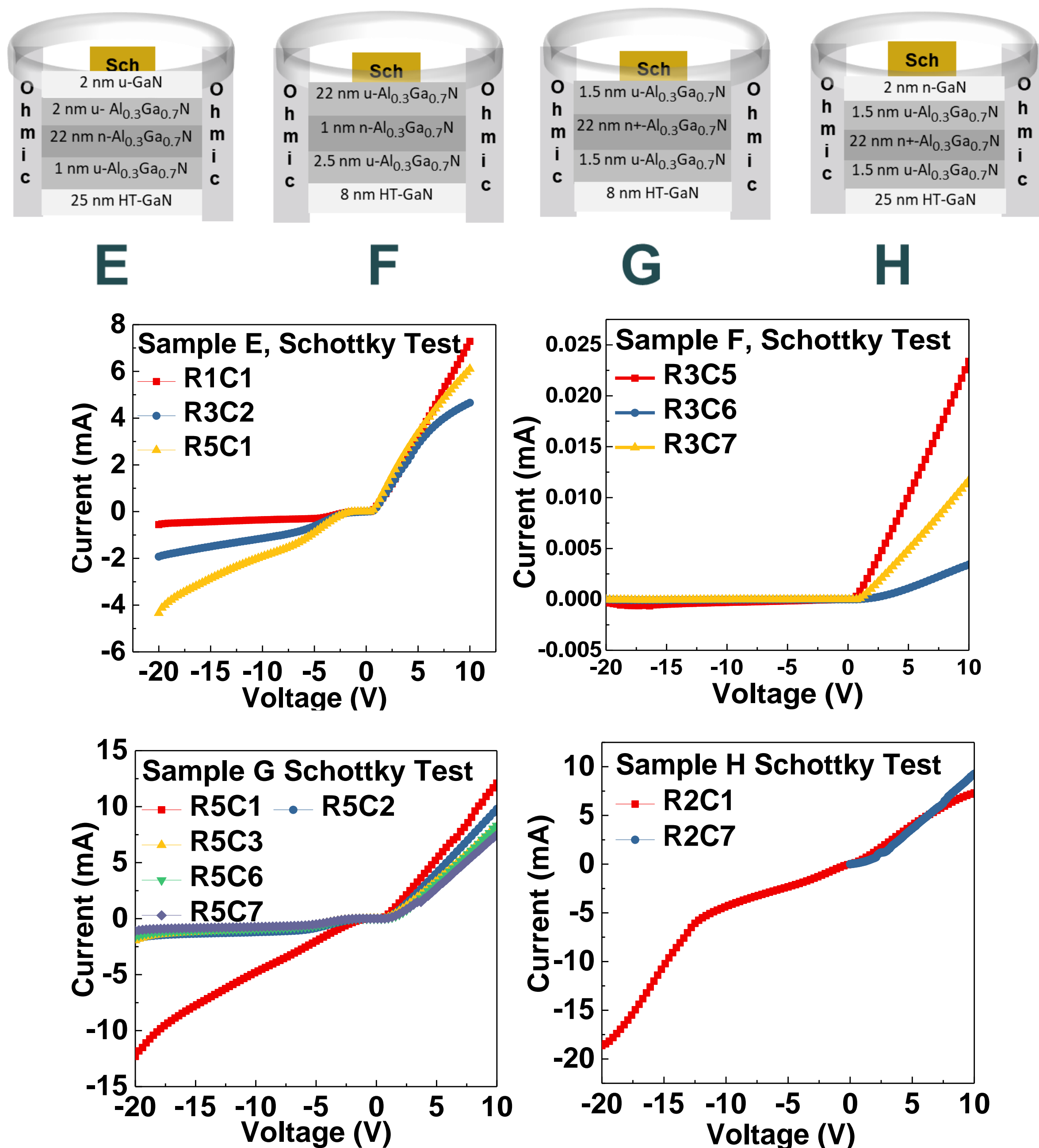


Figure 6.12 a) to h): SBD structure cross-sections and results for Group 2.

To begin, Sample F does show a pattern close to what is expected, but is far eclipsed in terms of current by the others. Sample E's results are fairly leaky both for positive and negative voltages applied, except the first row and column of the device dice where it is normal. Sample G's SBDs work as expected except the first column of the fifth row, as this must be a leakier part of the wafer compared to for example the centre. Sample H shows a fairly large leak at negative voltages.

Buffer Leakage Structure I-V Curves

Figure 6.13 shows buffer leakages for Group 2.

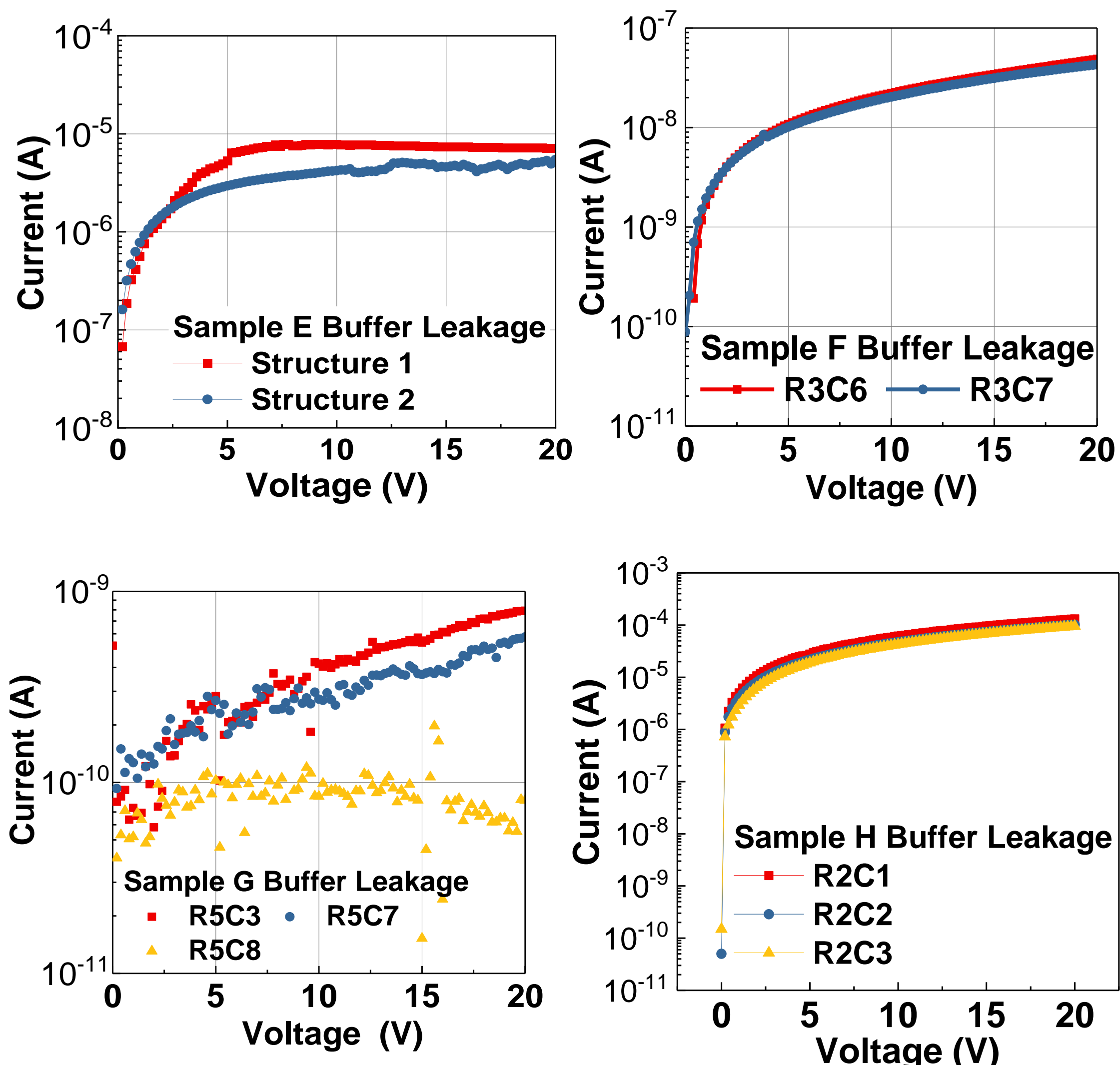


Figure 6.13: a) to d): Buffer leakage results for Group 2.

Compared to their Group 1 equivalents Sample B and C, Samples E and H show a remarkable 2 orders of magnitude improvement in their buffer leakage, but other than that, a clear pattern cannot be established. Samples F and G have their leakage in the several hundred pA or nA range. This alludes to the dual overgrown buffer template being effective at suppressing buffer leakage somewhat.

6.4.1.5: Group 3 Results

As a result of not having enough wafer pieces for Group 3 samples, very limited data is available for this set of samples. Regardless, the TLM and transconductance data here may prove useful.

HEMT Device Transconductances

Only Sample I was able to be fabricated in a full HEMT device, and its results may be seen on Figure 6.14. Otherwise similar to Sample G but with even further decreased cap and spacer thicknesses and a thicker barrier, it is clear that while it abides by the same transconductance behaviour and proper gate modulation, there is still some source leakage present, which has to be as a result of an overly thick barrier at negative Vgs which should lead to pinch-off conditions.

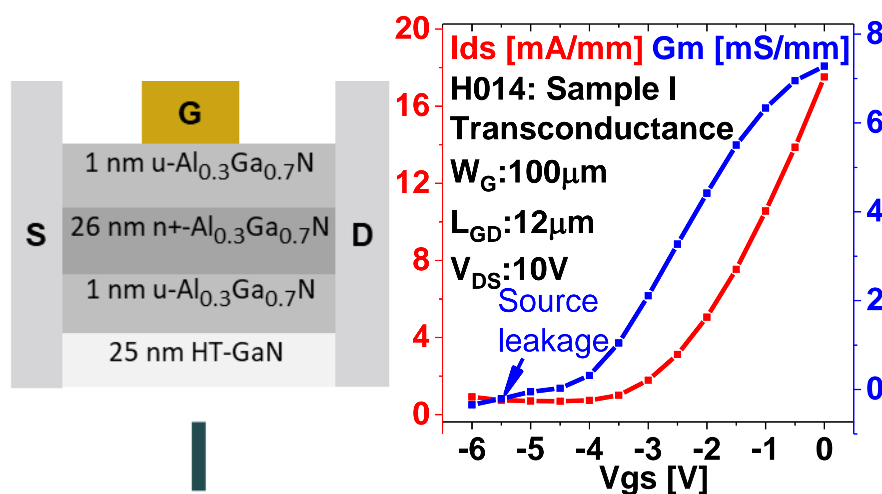
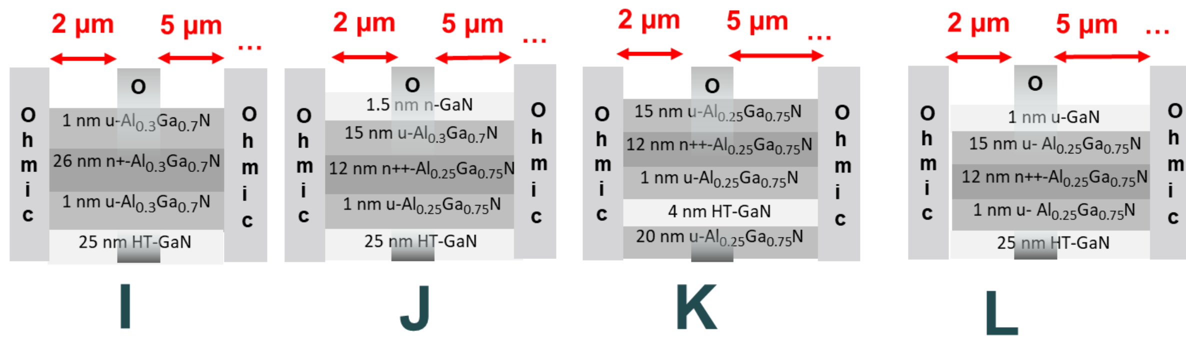
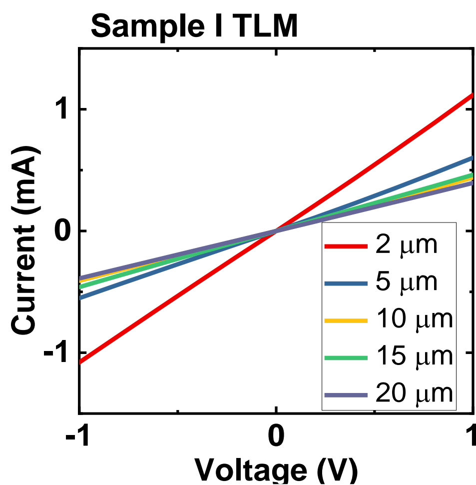


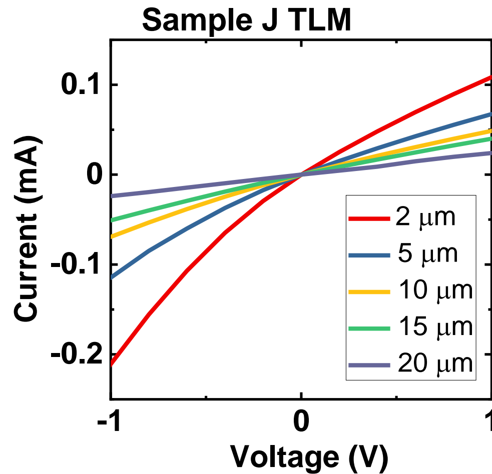
Figure 6.14: Transconductance results for Sample I with a fabricated device.

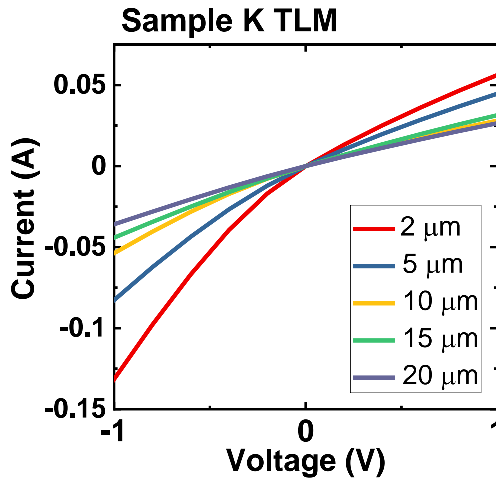
TLM Device I-V Plots

Figure 6.15 shows the TLM results for Group 3 and their cross-sectional diagrams. One minor difference is that the TLM spacing is slightly different, but their functionality should still be similar. Samples I and L (aside from a short contact spacing) do show the expected linear Ohmic behaviour across a different range of lengths. Samples J and K, however, have slightly parabolic Ohmic curves at shorter contact lengths, and Sample L also shows two asymmetric half-curves at 2 µm spacing. An explanation might be the decreased Al ratio and increased doping in these samples. The lack of buffer leakage data disallows us from putting that into context, however, and is still the most likely reason.









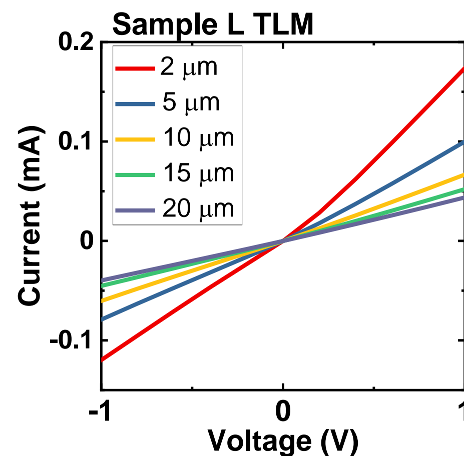


Figure 6.15 a) to h): TLM structure cross-sections and results for Group 3.

6.4.2: XRD Characterisation

The XRD characteristics of the non-polar HEMT samples were obtained through the use of a Bruker XRD setup (Chapter 3) emitting a 1.54 Å X-ray via a Cu-Kα tube. In order to obtain the measurements, an ω Rocking Curve and ω-2θ sweep was run for the samples. The counts from an ω sweep gives an indication of GaN refractivity over a range of azimuth sweep angles and a full width half of maximum (FWHM) value is calculated from this measurement using the two half-points on either side of the peak, then multiplied by 3600 to give the seconds-of-arc (arcsec) value – one in 60

of a minute of arc (MOA) which is in turn one in 60 of a degree, and this gives an indication of the sample quality.

ω-2θ peak values are the peaks of sweeps of the sample pitch and sample incident angle behaviour; this gives an indication of the sample composition. The first peak in an ω-2θ sweep is always the diffractometry result for GaN and the third is for pure AlN, with AlGaN alloys being in the middle.

DBD is what will be referred to as the Direct Bragg Difference; a full Wurtzite lattice of GaN and AlN will have their ω-2θ results be separated by a certain number of degrees, ≈ 0.75 normally, with around 28.75° being for full GaN and 29.5° for full AlN respectively in the a-plane orientation, but depending on the sample's quality and composition, the results may vary. For example, using these figures, a 0.375° difference indicates a 50% DBD or '50% Al ratio', whereas in reality the real Al composition is likely 27-30% with the extra strain from a-plane growth on r-plane sapphire actually skewing the results. Because accurately calculating the real Al% requires complex XRD triangulation methods and matrix maths [17], anecdotal data will be used to estimate the real Al composition of the AlGaN alloy.

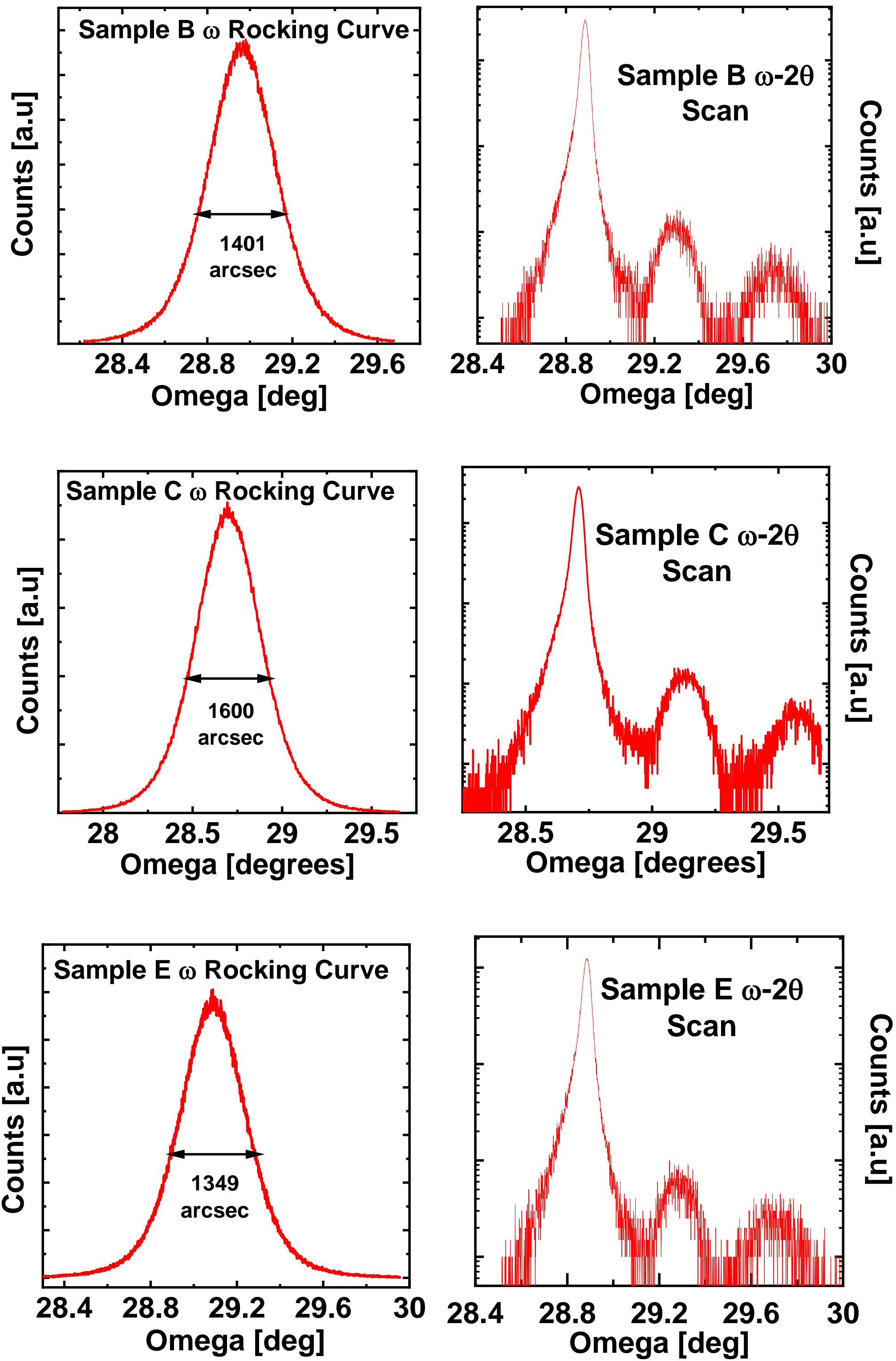
A collection of such results may be found on Table 6.2.

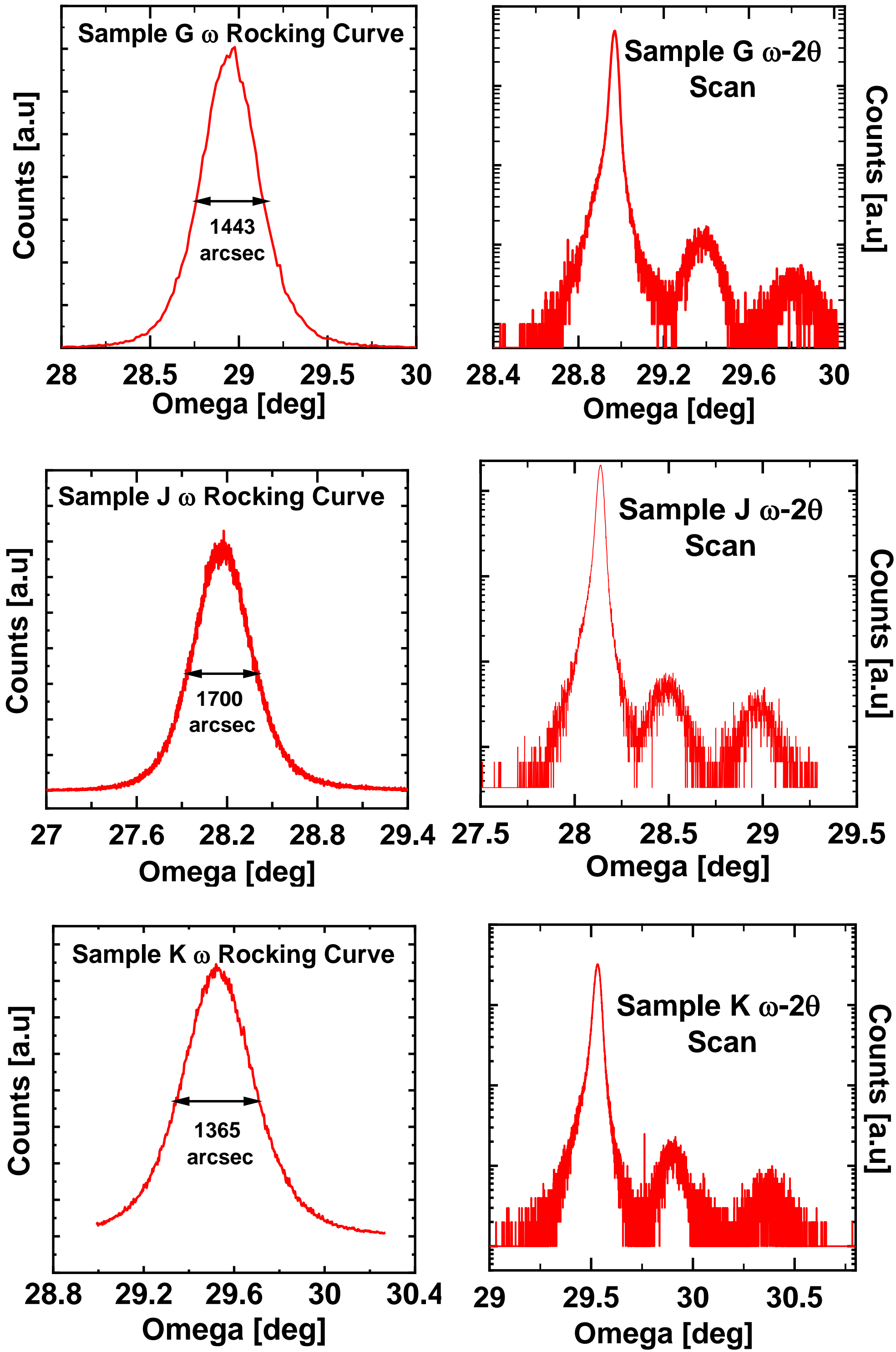
	B	**C**	**E**	**G**	**J**	**K**	**L**
FWHM [arcsec]	1401	1600	1349	1443	1700	1365	2364
ω-2θ Peak Positions	28.887° 29.292° 29.742°	28.709° 29.135° 29.571°	28.854° 29.285° 29.691°	28.968° 29.388° 29.813°	28.137° 28.493° 28.975°	29.531° 29.895° 30.369°	28.884° 29.254° 29.724°
DBD	54%	56%	57%	56%	47%	48%	47%

Table 6.2: A list of X-ray measurements across samples B, C, E, G, J, K and L. The peak ω-2θ are displayed here correct to 3 decimal places. DBD means direct Bragg diffraction peak difference percentage, which is used to interpret Al% in AlGaN alloys.

A few patterns can already be revealed; Samples with excessively high doping (such as Sample J and L), even though nowhere near the level of the volumetric density of III-N ionic pairs, tend to have greater dislocation densities, as evident by their higher FWHM, as the lower Al%, relatively similar growth temperature and pressure and similar V-III flow ratios should not make a large difference. Too many alternating barrier-well structures may also contribute to additional stress or strain which causes dislocations, as Samples B, C, E and G have nearly identical buffer statistics. Peak positions in an isolated, idealised position and the actual sample peak positions may also be slightly different

depending on the layers' composition in regard to thickness and impurities such as dopants. Sample K, in addition to its mobility, also has the second best buffer.




Sample G ω Rocking Curve
1443 arcsec
Counts [a.u]
28
28.5
29
29.5
30
Omega [deg]
Sample G ω-2θ Scan
Counts [a.u]
28.4
28.8
29.2
29.6
30
Omega [deg]
Sample J ω Rocking Curve
1700 arcsec
Counts [a.u]
27
27.6
28.2
28.8
29.4
Omega [deg]
Sample J ω-2θ Scan
Counts [a.u]
27.5
28
28.5
29
29.5
Omega [deg]
Sample K ω Rocking Curve
1365 arcsec
Counts [a.u]
28.8
29.2
29.6
30
30.4
Omega [deg]
Sample K ω-2θ Scan
Counts [a.u]
29
29.5
30
30.5
Omega [deg]

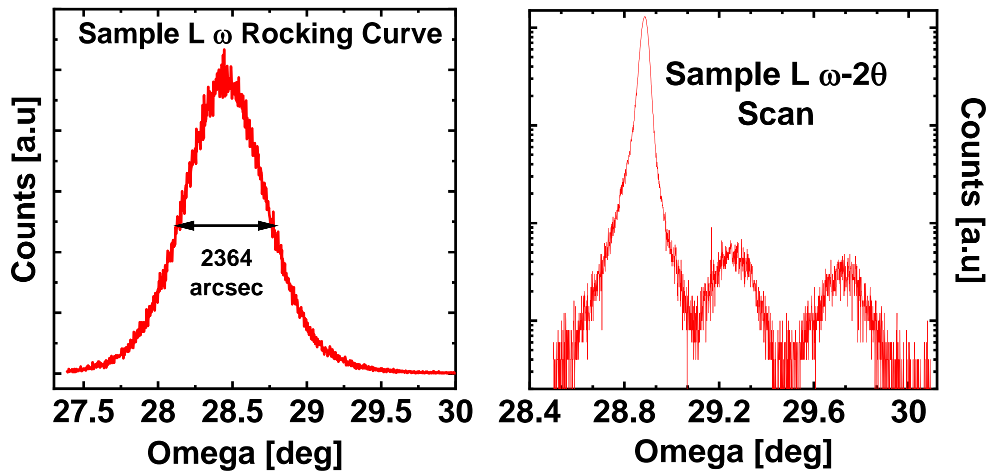


Figure 6.16 a) to q): A comprehensive list of all of the XRD curves.

The accuracy of the Al% interpretations through the use of direct Bragg Diffraction differences (through calculation of peak positions theoretically by using theoretical lattice constants) is highly dependent on sample quality, due to orthorhombic distortion of the unit Wurtzite cell and strain by layer transition between the higher part of the epitaxial structure and the r-plane sapphire buffer. This is in contrast to c-plane on c-plane sapphire samples whose Al composition can easily be interpreted directly. Anecdotally we have information corroborating to 49% DBD for an a-plane on r-plane sample of similar crystal quality and an actual 26% Al molar ratio; therefore, suggesting the possibility of Samples A to L having between 25% to 30% Al, and somewhat suggesting in turn that Al ratio for layers overgrown is roughly directly proportional to TMG flow rate at this regime, which may not be unreasonable to expect considering the Al site substitution at this range of molar ratios is favourable. [11, 21]

6.4.3: Schrödinger-Poisson Solutions

Here are a series of 1D epitaxial wavefunction-based electron concentration distributions for a variety of Al ratios for the barrier, doping concentrations for the barrier and also the cap, using Sample A as an archetype but using 12 nm as the barrier thickness. In 6.4.3.4, it will be explained why this barrier thickness has been chosen for the simulations for demonstration purposes. These will also be used to relate the results to the real fabricated structures presented to attempt to explain what is being meant in each case. In order to carry out the simulation, u-doping has been assumed to be 10^{14} cm^{-3} as a best-case scenario for demonstration, although 10^{16} is a more realistic figure. The barrier doping has been set at 10^{19} cm^{-3} for all cases other than 6.4.3.2, where variation by barrier doping is assessed.

The next series of figures is to visually demonstrate the differences barrier thickness, aluminium composition and doping concentration can make onto channel layer electron

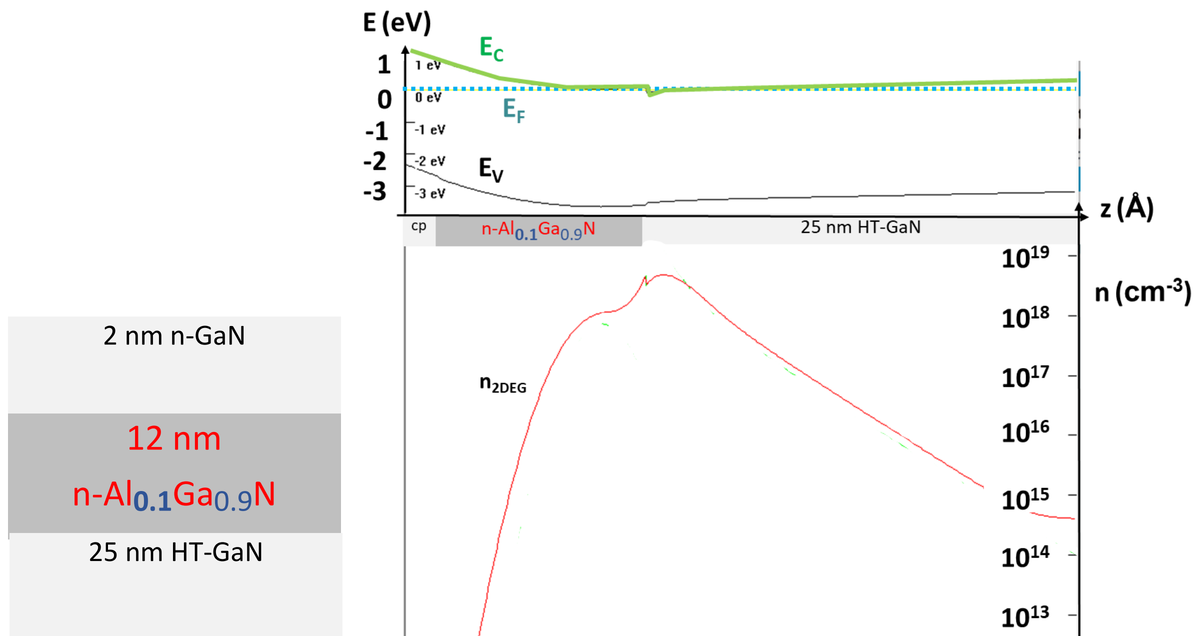
concentrations, through the use of 1D Schrödinger-Poisson solutions, in the hopes of establishing the basic relationships.

6.4.3.1: Variation by Al Ratio

Higher Al ratios, within practical limits, in the barrier naturally are favourable to induce a greater electric potential drop from the barrier to the channel layer, and also to contain the free charge carriers in their intended unintentionally doped GaN layer, largely thanks to AlGaN's higher bandgap than GaN. Figure 6.17 depicts a series of simulations with this in mind, done with a 12 nm barrier thickness doped at 10^{19} cm^{-3}, the 2 nm GaN cap being at 5×10^{19} cm^{-3} for the sake of argument. 40% Al performs the best for confinement, as expected, but 30% is very close to it in terms of electron concentration distribution. The Schottky barrier heights are the same due to the structure containing a GaN cap.

Figure 6.18 shows a 1D epitaxial wavefunction-based electron concentration distribution for sample A as an archetype at different Al concentrations. In order to carry out the simulation, u-doping has been assumed to be 10^{14} cm^{-3} as a best-case scenario for demonstration, although 10^{16} is a more realistic figure. The barrier doping has been set at 1×10^{19} cm^{-3} for demonstration purposes.

Figure 6.18 has been split into two parts, where a) and b) show 10% and 20% Al ratio respectively and c) and d) show a 30% and 40% ratio. In all cases, the conduction band and Fermi Level have been drawn over and magnified to clarify the plot; additional axes have been added in a larger font for readability. It is evident from this first group that at this level of doping, the conduction band donor-induced potential drop is comparable to the Schottky barrier height, thus indicating that in both cases there is significant dual barrier-channel conduction happening. Therefore, if 20% Al is to be used, the doping concentration needs to be tuned down in order to improve 2DEG confinement.



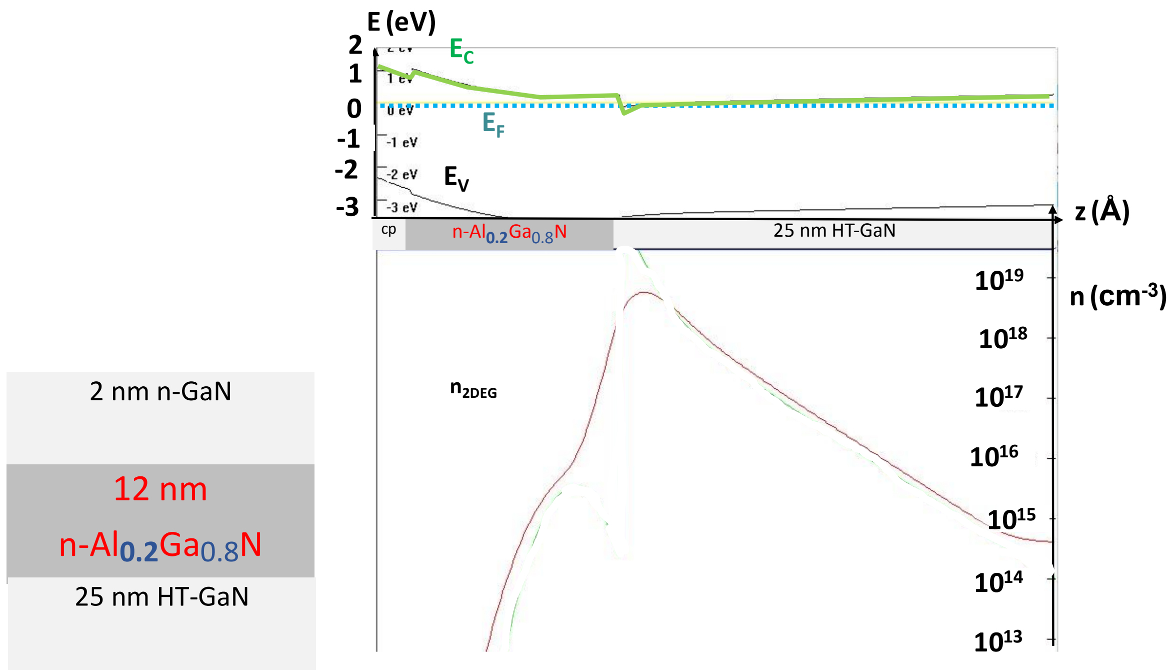


Figure 6.17 a) and b): Variation of electron concentration, in a logarithmic scale, with Al composition of the barrier (10% and 20%) with their epitaxial structure labelled.

Figure 6.17 c) and d) show when the Al concentration is at the estimated 30% and 40% respectively. In both of these cases at the given doping concentration and barrier thickness, the bottom of the barrier conduction band is a significant height away from the Fermi level, thus allowing for most of the charges to be confined in the 2DEG channel layer. This is good from a device perspective, since it means a successfully gate-modulated device that can be turned off at a negative voltage, and most of the conduction happening only in the channel layer. Therefore, in a 'traditional' epitaxial structure similar to Sample A, or similar GaN-cap gate-modulated samples like Sample D

and G, it shows that this Al ratio is effective. Given all of Group 1 and 2 samples use 30% as estimated, the real limiting factors is barrier thickness and doping concentration in 2DEG confinement.

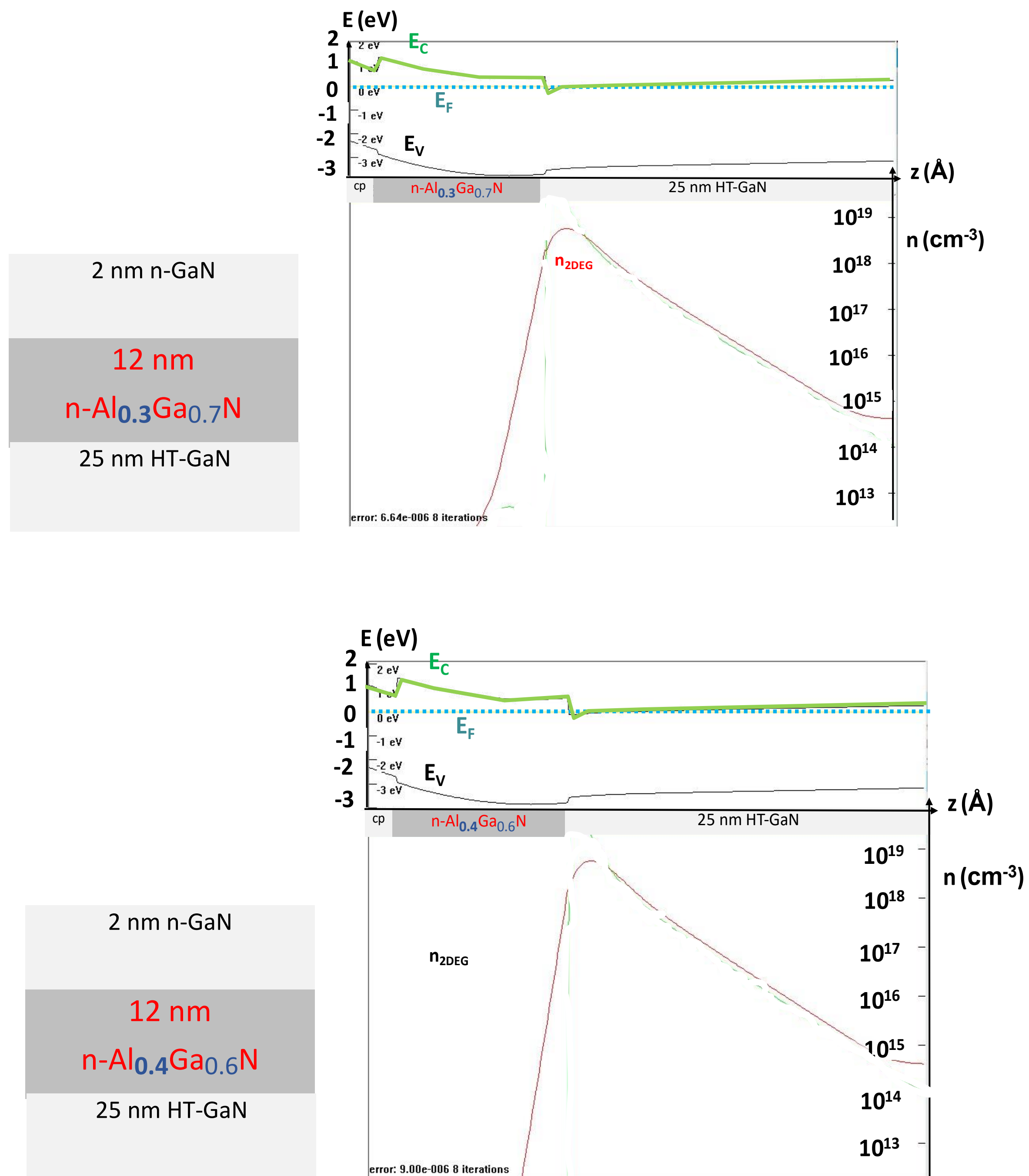


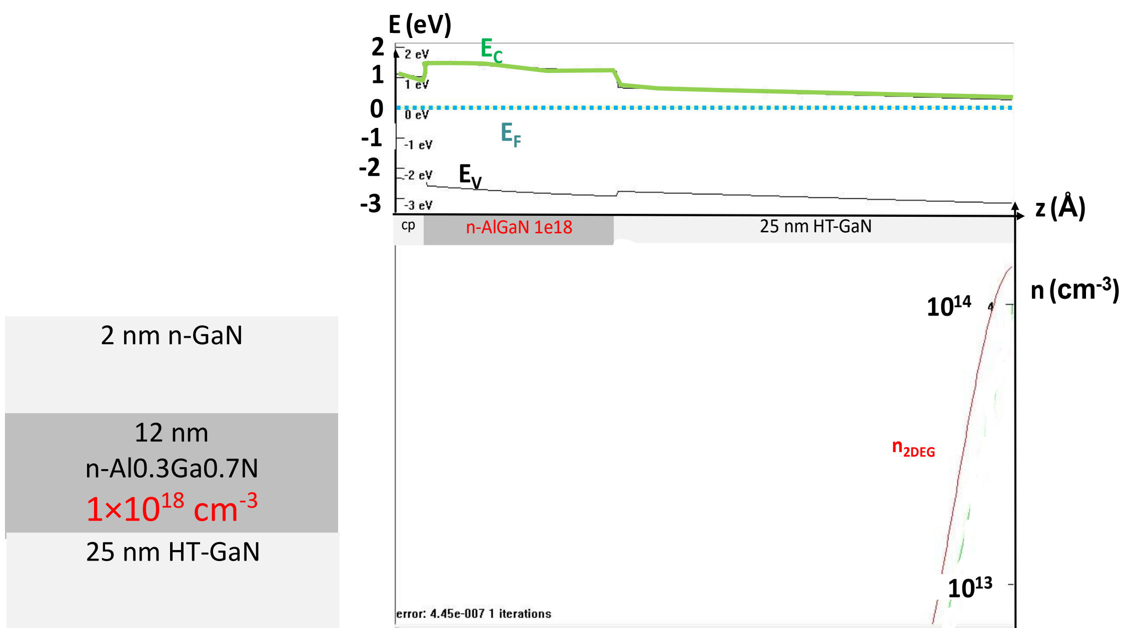
Figure 6.17 c) and d): Variation of electron concentration, in a logarithmic scale, with Al composition of the barrier (30% and 40%) with their epitaxial structure labelled.

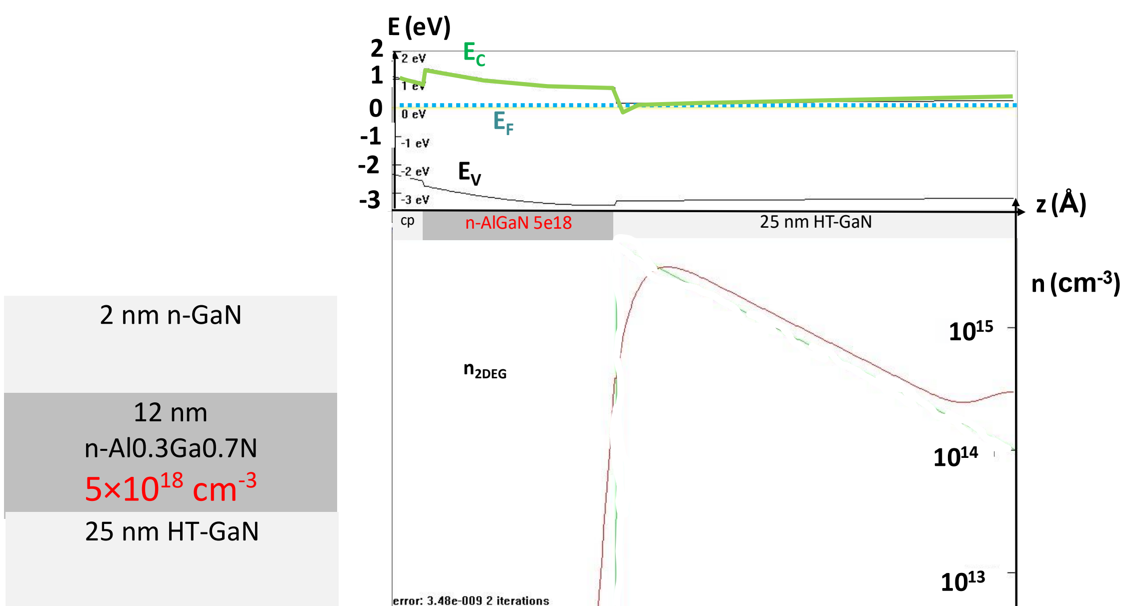
6.4.3.2: Variation by Doping Level For Barrier

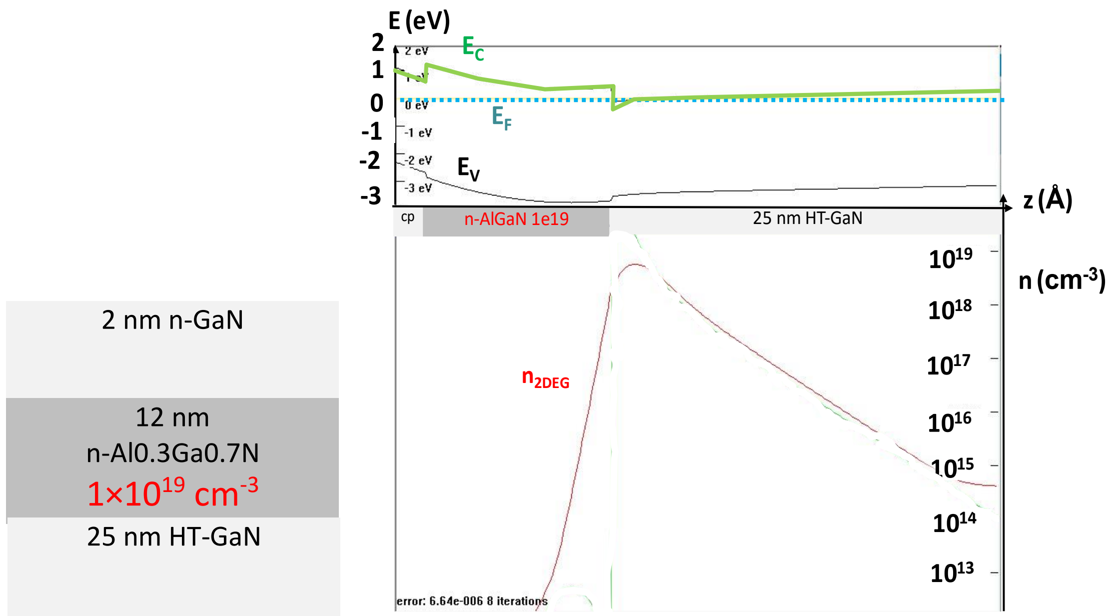
Next, higher barrier doping usually results in stronger band bending, as compliant with Poisson's theory that these surplus charges create a potential, and naturally more charge carriers to

be freed up, which can reasonably be expected to influence the channel's final number of carriers. Slightly saturated doping is preferred, but degenerate doping causes electrons to spill over into the barrier. Figure 6.18 shows one such hypothetical simulation. This is one of the reasons why modulation doping works with this combination but delta doping will have too little of a barrier area to cover.

Electron concentration is relatively insensitive to the doping of a GaN cap, as seen in Figure 6.19, unless it is extremely degenerate doping in which case that does generate a significant amount of charge depletion.







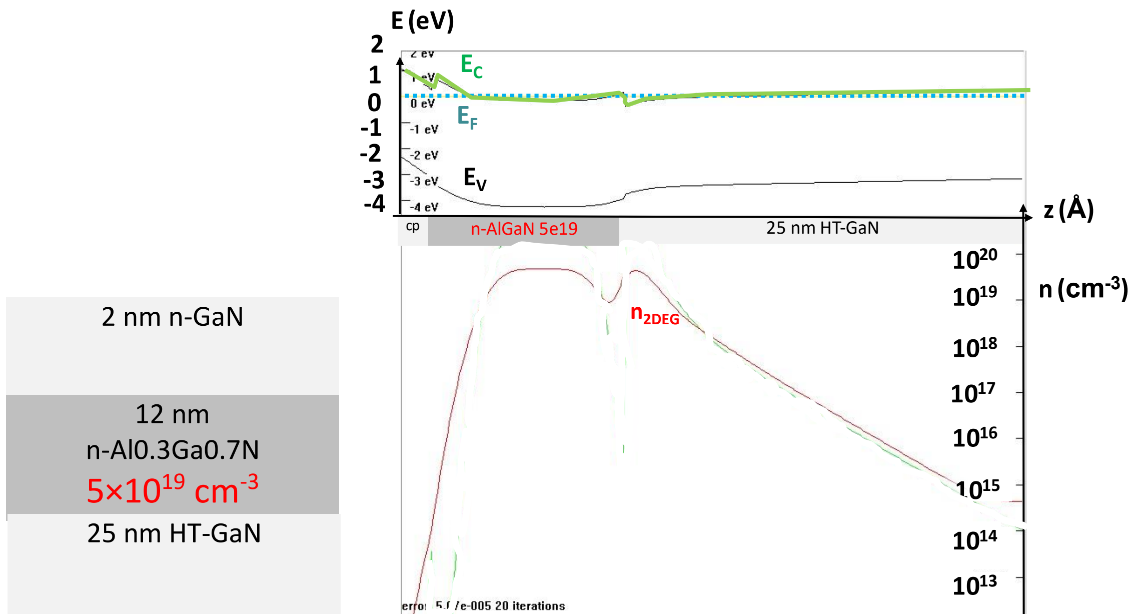
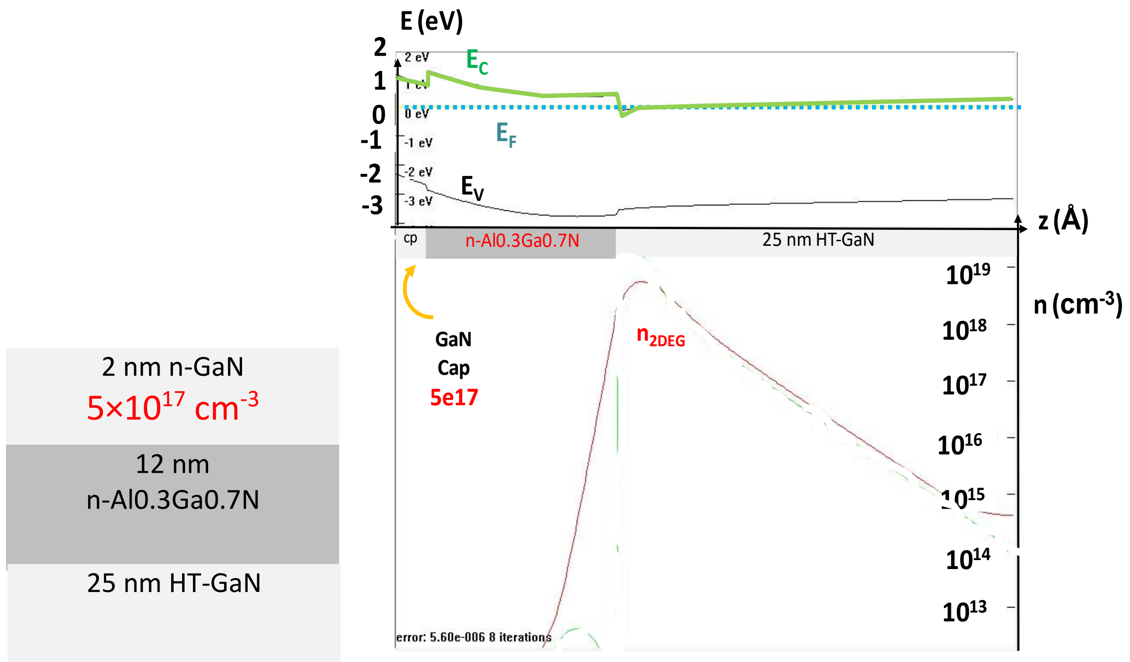


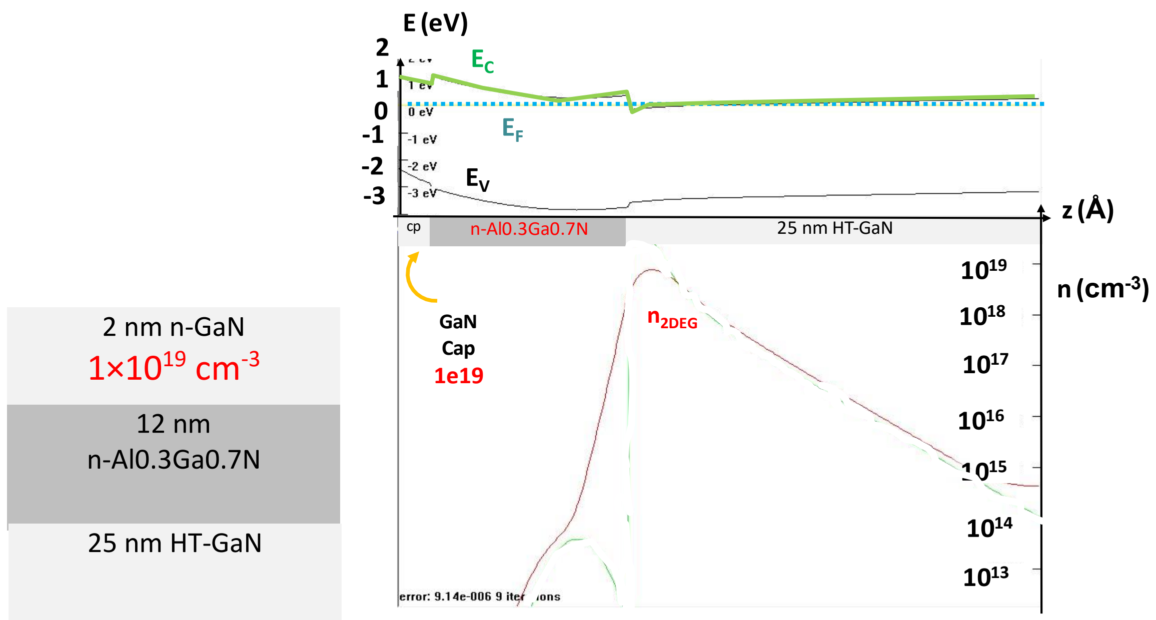
Figure 6.18 a) to d): AlGaN barrier doping changes affecting electron concentration in a logarithmic scale for a 12 nm barrier (1 $\times 10^{18}$, 5 $\times 10^{18}$, 1 $\times 10^{19}$ and 5 $\times 10^{19}$ cm^{-3}).

Sample K has also been assessed in this manner, as its novel hybrid heterostructure has been designed with taking advantage of the principles of quantum confinement in mind. As long as the Al percentage remains above 15, the 1D epitaxial solutions imply that the dual barrier approach greatly suppresses buffer leakage from the doping scheme so it is mainly the intrinsic buffer leakage from unintentional doping that remains on a device level affecting the final leakage value. In addition, the thin GaN layer is also excellent for maintaining a high concentration of electrons confined within the

channel as long as the doping does not exceed 1.5 x 10^{19} cm^{-3}, which also happens to be the upper limit of Si doping of GaN before significant 3D stacking faults are observed.

6.4.3.3: Variation by Doping Level for GaN Cap





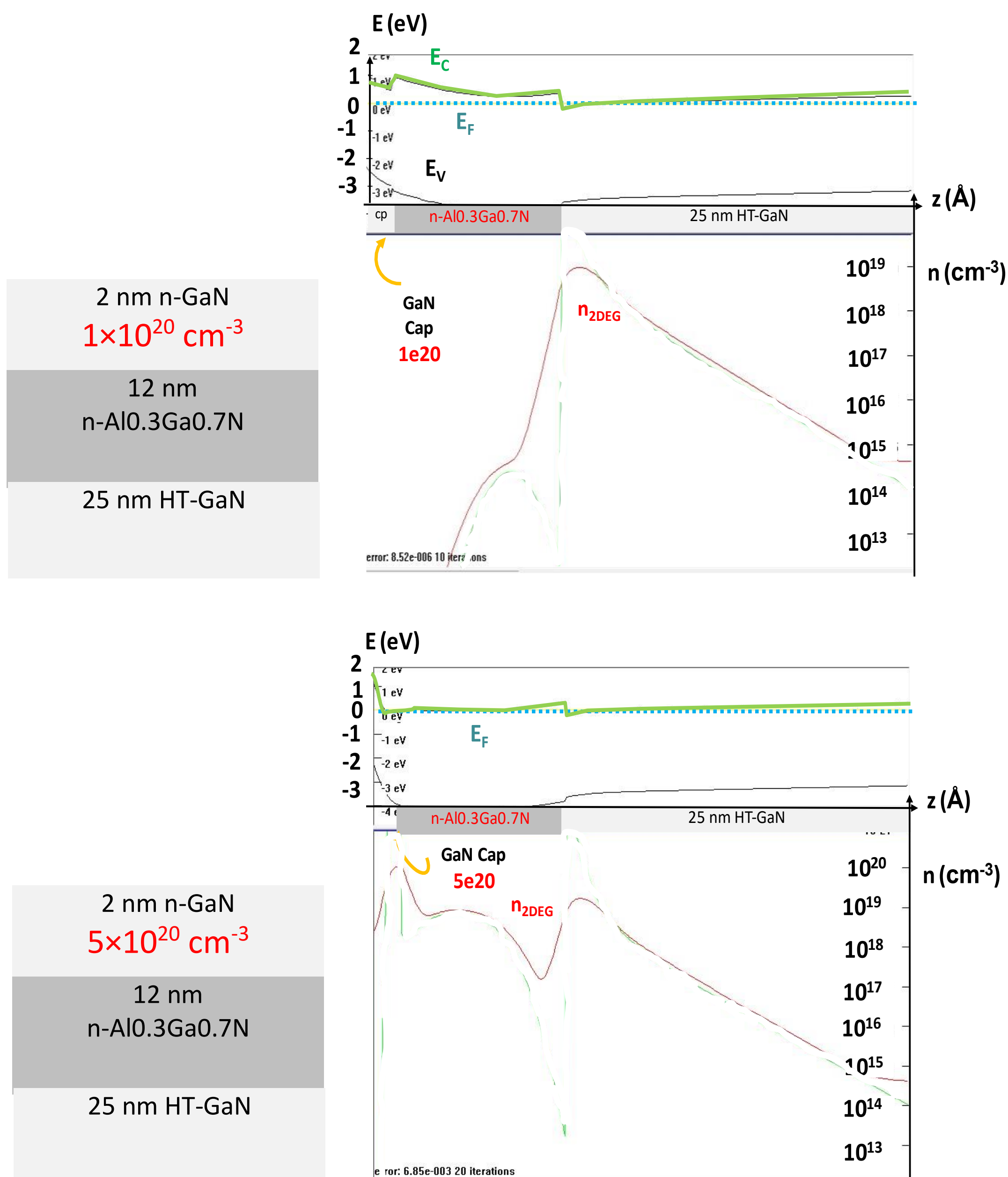


Figure 6.19: GaN cap doping changes affecting electron concentration in a logarithmic scale.

6.4.3.4: Example of a 25 nm Barrier Doped 1e19 for Dual Barrier-Channel Conduction Demonstration

Figure 6.20, it is hoped, will be able to establish what is meant by barriers being too thick and Fermi-level cross-over. So far, all of the simulated structures based on Sample A have been with 12 nm thick barriers. However, most of the real samples use 25 or 26 nm as the total AlGaN thickness. One such simulation comparing the two is being shown on the aforementioned Figure 6.20. 1×10^{19} cm^{-3} is used as the n-type doping in these simulations with a 30% Al ratio.

As a result of the dopant-induced charge depletion length being not larger than the top of the conduction band for AlGaN, the 12 nm barrier length maintains the bottom of the conduction

band higher than the Fermi level for a Schottky contact, and a large portion of the charges will crowd in the HT-GaN/AlGaN interface as the intended 2DEG region. However, with 25 nm, it can clearly be seen that the charge depletion makes the bottom of the conduction band cross over the Fermi level before the potential rises back to the band discontinuity level, and as a result, the middle of the barrier will have a significant charge carrier density. This demonstrates what is being meant by dual channel-barrier conduction.

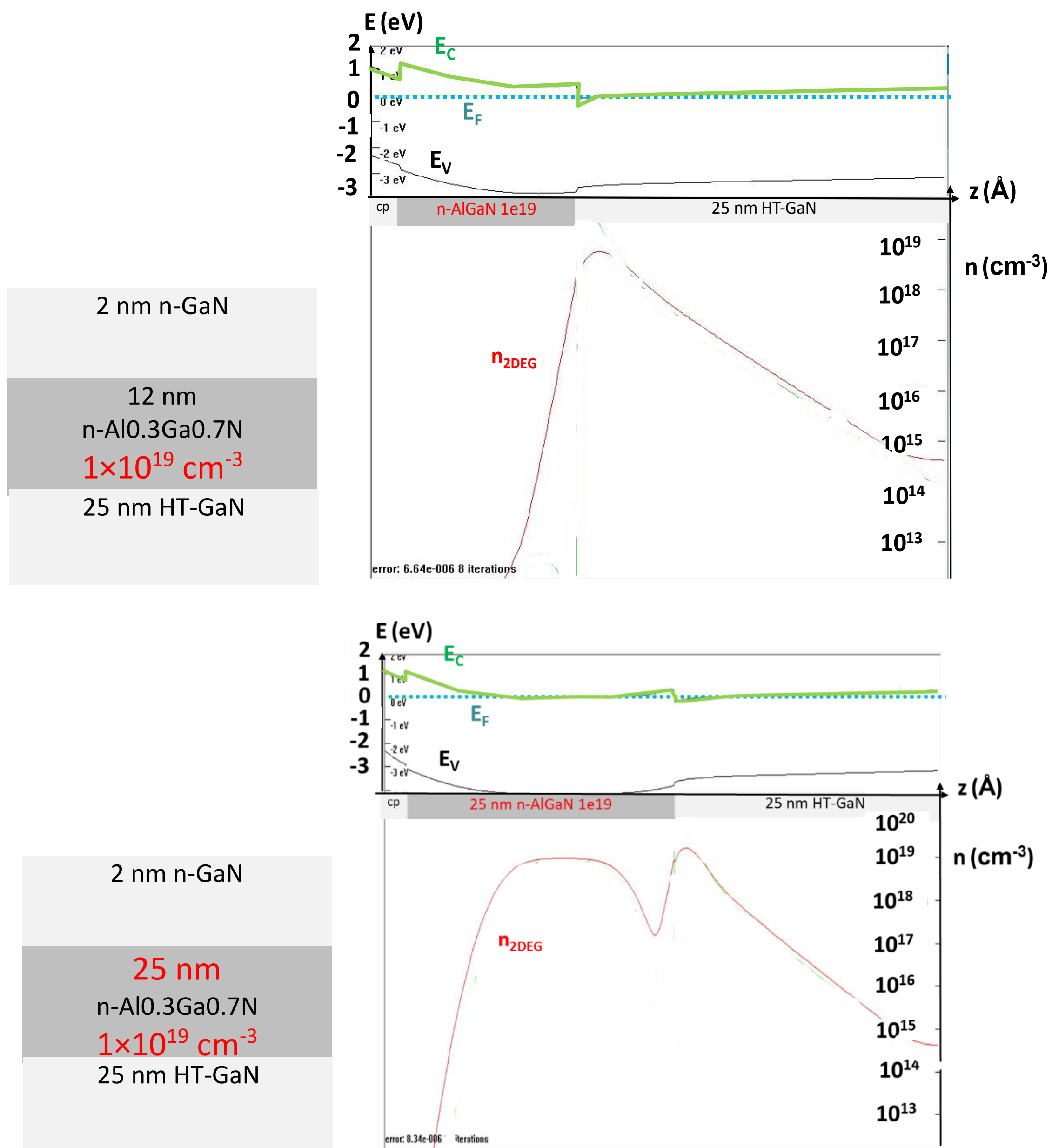


Figure 6.21: 12 vs 25 nm barrier at 1×10^{19} cm^{-3} doping.

6.5: Conclusion

A series of 12 non-polar GaN/AlGaN HEMT samples in three different categories, exploring the more traditional modulation doping schemes, a dual buffer composition and experimental epitaxial

structures respectively have been fabricated, along with a series of TLM, SBD and buffer leakage structures. An electron mobility of 76 $cm^2 V^{-1} s^{-1}$ has been reported for Sample K, which belongs to the third experimental category and uses a GaN quantum well, at the expense of high measured sheet resistivity, thus marking an improvement for a-plane GaN on r-plane sapphire, which seldom exceeds 46 $cm^2 V^{-1} s^{-1}$. The quantum well sample formula is therefore still an intriguing option for future designs. A maximum current density of 65 mA/mm has been obtained, displayed by Sample E. Some improvement is recorded in buffer leakage by the introduction of a secondary overgrown a-plane GaN buffer, sometimes by 2 orders of magnitude, but it may be worth using high-quality coalescent nano-patterned buffers instead.

Results across all of the non-polar samples suggest that at the thicknesses and dopant flow rates used, delta doping is ineffective and sandwich-barrier modulation doping runs the risk of barrier conduction. In practice, it is the GaN cap (A, D, E) or very thin AlGaN cap samples (G) that display any gate modulation. Simulations also support the hypothesis that excessively thick barriers and excessive doping causes a degree of barrier/channel dual conduction, which ultimately leads to source leakage and reduction in mobility/2DEG density compared to what the sample should allow.

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Chapter 7 – Conclusion and Future Work

7.1: Conclusion

The Thesis has focussed on three areas of research that have been the subject of intrigue in regard to III-Nitride power and optoelectronics.

Investigation into Improvements in InGaN/GaN Micro-LEDs Through Overgrowth

The leakage and forward currents have been measured on our epitaxy-overgrown µLEDs with different sizes, showing a significant improvement in comparison with those µLEDs fabricated by the conventional dry-etching method. The influence of the µLED size on the leakage current has been systematically investigated. Due to the effective elimination of etching-induced damage by an overgrowth approach which is particularly important for smaller µLEDs, it reveals that our smaller overgrown µLEDs have much smaller leakage current than those µLEDs fabricated by the conventional dry-etching method in terms of either leakage current per µLED or leakage current density. LED leakage currents as small as 14 nA have been able to be obtained using this series of overgrown devices as well as response times in the range of several ns. Moreover, the µLEDs fabricated by the conventional dry-etching method displays a larger dispersion in leakage current, especially for those smaller µLEDs, which is attributed to high amounts of dry-etching-induced damages. While it has been concluded that overgrown LEDs do actually have a size-dependent leakage magnification, it is inherently tied to the dimensions of the devices rather than parasitic trap-induced non-radiative recombinations. Furthermore, the RC constants have also been found to be more favourable to the epitaxy overgrown devices. It is expected that our epitaxy overgrown µLEDs will bring about advantages of better pixel-level resolution, high efficiency, and energy efficiency to applications of micro-display, augmented/virtual reality setups, and VLC. The application of the principles of overgrowth, therefore, has proven itself to be a reliable, efficient and self-passivating method of mass-production of µLED arrays with minimal damage and maximum leakage suppression, which will be doubly important at the chip level.

Investigation of Unintentionally-Doped GaN Buffers in High-Temperature AlN Nucleation Layer 2D Grown AlGaN/GaN HEMT Stacks

We have performed a comprehensive study on GaN/AlGaN HEMTs grown with a special 2D-growth approach, and made a comparison with a two-step method with a combination of 2D and 3D growth. It is found that the unintentional doping concentrations and screw dislocation densities are

significantly lower in the 2D-grown samples compared to the two-step growth method, achieving a very low unintentional doping density of 2×10^{14} cm^{-3} and a screw dislocation density of 2.3×10^{7} cm^{-2}. High-frequency capacitance measurements show that the samples grown with the 2D growth approach have much lower buffer leakage and higher breakdown limits, attaining a sub-nA/mm leakage, a high breakdown limit of 2.5 MV/cm, and a saturation current density of about 1.1 A/mm. It indicates that our special 2D-growth approach can effectively lessen the unintentional doping in the GaN buffer layers, leading to GaN/AlGaN HEMTs with low buffer leakage and high breakdown limits. Moreover, it appears that a higher AlN buffer temperature and lower pressure leads to fewer dislocations of a screw nature.

Epitaxial Analysis and Characterisation of Non-polar (11-20) 'a-plane' GaN/AlGaN HEMTs on 'r-plane' (10-12) Sapphire

A series of 12 non-polar GaN/AlGaN HEMT samples in three different categories, exploring the more traditional modulation doping schemes, a dual buffer composition and experimental epitaxial structures respectively have been fabricated, along with a series of TLM, SBD and buffer leakage structures. An electron mobility of 76 cm^{2} V^{-1} s^{-1} has been reported for Sample K, which belongs to the third experimental category and uses a GaN quantum well, at the expense of high measured sheet resistivity, thus marking an improvement for a-plane GaN on r-plane sapphire, which seldom exceeds 46 cm^{2} V^{-1} s^{-1}. The quantum well sample formula is therefore still an intriguing option for future designs. A maximum current density of 65 mA/mm has been obtained, displayed by Sample E. Some improvement is recorded in buffer leakage by the introduction of a secondary overgrown a-plane GaN buffer, sometimes by 2 orders of magnitude, but it may be worth using high-quality coalescent nano-patterned buffers instead.

Results across all of the non-polar samples suggest that at the thicknesses and dopant flow rates used, delta doping is ineffective and sandwich-barrier modulation doping runs the risk of barrier conduction. In practice, it is the GaN cap (A, D, E) or very thin AlGaN cap samples (G) that display any gate modulation. Simulations also support the hypothesis that excessively thick barriers and excessive doping causes a degree of barrier/channel dual conduction, which ultimately leads to source leakage and reduction in mobility/2DEG density compared to what the sample should allow.

Moreover, simulations have established that the optimal barrier thickness at the given dopant flow rates is likely to be between 12 and 25 nm, and that doping should not exceed 1×10^{19} cm^{-3} for 30% or less Al. The TMA flow rate is established to be proportional to the Al end ratio for a-plane.

7.2: Future Work

To follow up work undertaken in Chapter 4 with a statement that micro-LEDs have a further room for improvement. Fairly recently the GaN Centre has been undertaking further pursuits towards scaling down micro-LEDs even further, down to 2 µm diameter and a smaller inter-pitch, with 1.5 µm also being prototyped. In keeping with the Centre's close collaboration with industry, this will prove further useful for back panels for VR equipment, where small, densely packed RGB µLED clusters are desired for high pixel-level precision. Therefore the electronic implications this reduced size will bring about are a subject of debate. Moreover, schemes to improve Si_3N_4 etching profiles are also a subject of intrigue, which has a direct impact on the device performance.

As brought forward in Chapter 5, it was discussed that the lower screw dislocation, lower unintentional doping of Sample D owing to its high-temperature AlN buffer and prominent 2D growth mode combine together to give the best buffer leakage current performance. It is quite intriguing to find out whether high current density and low buffer leakage simultaneously may be achieved by introducing intentional barrier doping whilst still taking advantage of the high spontaneous polarisation from the AlN spacer layer. Moreover, a further increase in the 2D growth temperature and adjustment of the chamber pressure also remains a point of interest to see whether the idea presents diminishing returns or is unfeasible for further suppression of screw dislocations, with implications for strain and wafer bowing implications.

According to Chapter 6, while the presence of a GaN quantum well layout, as per Sample K's epitaxial structure, apparently presented great improvements to the electron mobility and electron confinement, whilst reducing the sheet density despite higher doping, and the stacking faults as apparent by its XRD characteristics owing to its different buffer growth scheme, the increase in measured sheet resistivity was also quite notable, which may actually be a reflection of the contact characteristics due to the Hall Effect samples. Still, it is a curious idea that may be improved upon to inject more electrons into the channel layer whilst blocking electrons from going deep into the buffer, provided that the buffer unintentional doping is kept at a low. Therefore, it seems prudent to experiment with higher intentional barrier doping and work with different cap layer thicknesses too. Moreover, growth without requiring multi-step nanorods that results in a good crystal quality will also remain a point of interest. It is highly possible that longer growth coalescence on its own may lead to better buffer characteristics.

Chapter 8 - Appendices

8.1: Appendix – Full Growth Parameters, Descriptions and Structures of the 12 Non-Polar (11-20) GaN/AlGaN HEMT Samples Used (Chapter 6)

Appendix B shows a series of samples, grown *in situ* within Nanosciences facilities, that have been used in the study as seen in Chapter 6. As their full growth parameters and growth philosophy would have been too long for the main chapter, the Author has opted to place these samples here.

Sample A

Sample A is grown in a 'traditional' HEMT epitaxial layer stack fashion; a GaN cap, a doped 'barrier' layer of AlGaN, and a 'high-temperature' thin layer of GaN for 2DEG build-up, to be induced by the barrier doping, atop a thick a-plane GaN buffer. The idea is for the doped layer to compensate for the lack of polarisation to induce charge carriers to the HT-GaN region whilst spatially separating the dopants from it as electrons have a tendency to scatter across impurities, thus in theory improving mobility. But above all, the main purpose of this HT-GaN layer is as an AlGaN growth facilitator. The n-GaN cap is supposed to be persistent enough to enable better, lower resistivity Ohmic contacts and also thin enough to not heavily influence Schottky gate behaviour. A short growth time and a lower V/III ratio has been used for the buffer for a relatively thin, partially-3D growth to offset the biaxial lattice mismatch. The buffer is 500 nm thick. The remaining layers are 2D-grown. The disilane flow rate for the cap and barrier layers is 5 standard cubic centimetres per minute.

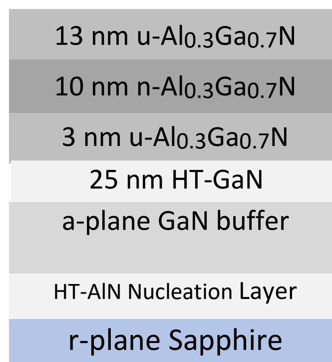
2 nm n-GaN
25 nm n-$Al_{0.3}Ga_{0.7}N$
25 nm HT-GaN
a-plane GaN buffer
HT-AlN Nucleation Layer
r-plane Sapphire

Layer	Time [s]	Pressure [Torr]	Temperature [°C]	TMG Flow Rate [sccm]	TMA Flow Rate [sccm]	NH_3 Flow Rate [sccm]	Si_2H_6 Flow Rate [sccm]
n-GaN	5	75	1160	12.5	---	5480	5
n-AlGaN	153	75	1160	12.5	30	5480	5
HT-GaN	150	75	1160	12.5	---	5480	---
Buffer	625	90	1060	47	---	1900	---

Figure 8.1: Structure of Sample A and **Table 8.1:** Full growth parameters.

Sample B

Sample B is a modulation-doped triple stack, consisting of a 10 nm doped layer of AlGaN sandwiched in between a thicker unintentionally-doped AlGaN cap and a thinner unintentionally-doped AlGaN 'spacer', intended to spatially separate the doped region from the GaN layer just atop an a-plane buffer. The principal idea behind this sample is that, in theory, by using a thicker cap, the backwards leakage towards the contact metals would be reduced; the spacer is kept a little thicker than usual with the aim of preventing surface state-related leakage and the barrier is kept reasonably thin to allow enough of a charge depletion into the HT-GaN layer, but also thin enough to allow for gate modulation.



Layer	Time [s]	Pressure [Torr]	Temperature [°C]	TMG Flow Rate [sccm]	TMA Flow Rate [sccm]	NH_3 Flow Rate [sccm]	Si_2H_6 Flow Rate [sccm]
u-AlGaN	73	75	1160	12.5	30	5480	---
n-AlGaN	61	75	1160	12.5	30	5480	5
u-AlGaN	18	75	1160	12.5	30	5480	---
HT-GaN	150	75	1160	12.5	---	5480	---
Buffer	625	90	1060	47	---	1900	---

Figure 8.2: Structure of Sample B and **Table 8.2:** Full growth parameters.

Sample C

Sample C is another of the modulation-doped samples, but with a much thinner cap and spacer intended to allow for better charge tunnelling from the central barrier into the HT-GaN layer while a thick barrier allows for a greater amount of charge accumulation within the barrier itself, to be depleted into it. The dopant flow rate (and therefore the doping concentration) and buffer/nucleation/substrate composition remains identical to the previous two samples.

2 nm u-$Al_{0.3}Ga_{0.7}N$
22 nm n-$Al_{0.3}Ga_{0.7}N$
1 nm u-$Al_{0.3}Ga_{0.7}N$
25 nm HT-GaN
a-plane GaN buffer
HT-AlN Nucleation Layer
r-plane Sapphire

Layer	Time [s]	Pressure [Torr]	Temperature [°C]	TMG Flow Rate [sccm]	TMA Flow Rate [sccm]	NH_3 Flow Rate [sccm]	Si_2H_6 Flow Rate [sccm]
u-AlGaN	12	75	1160	12.5	30	5480	---
n-AlGaN	134	75	1160	12.5	30	5480	5
u-AlGaN	6	75	1160	12.5	30	5480	---
HT-GaN	150	75	1160	12.5	---	5480	---
Buffer	625	90	1060	47	---	1900	---

Figure 8.3: Structure of Sample C and **Table 8.3:** Full growth parameters.

Sample D

Sample D is a hybrid modulation-doped sample not too dissimilar to Sample C, with the simple addition of a thin u-doped GaN cap to present smaller electro-potential barrier with especially Schottky contacts and u-doped GaN is still a good match for Ohmic contact metals, which in theory should improve the sample's gate modulatability and gate leakage.

2 nm u-GaN
2 nm u-$Al_{0.3}Ga_{0.7}N$
22 nm n-$Al_{0.3}Ga_{0.7}N$
1 nm u-$Al_{0.3}Ga_{0.7}N$
25 nm HT-GaN
a-plane GaN buffer
HT-AlN Nucleation Layer
r-plane Sapphire

Layer	Time [s]	Pressure [Torr]	Temperature [°C]	TMG Flow Rate [sccm]	TMA Flow Rate [sccm]	NH_3 Flow Rate [sccm]	Si_2H_6 Flow Rate [sccm]
u-GaN	5	75	1160	12.5	---	5480	---
u-AlGaN	12	75	1160	12.5	30	5480	---
n-AlGaN	134	75	1160	12.5	30	5480	5
u-AlGaN	6	75	1160	12.5	30	5480	---
HT-GaN	150	75	1160	12.5	---	5480	---
Buffer	625	90	1060	47	---	1900	---

Figure 8.4: Epitaxial Structure of Sample D and **Table 8.4:** Growth parameters of Sample D.

Sample E

2 nm u-GaN
2 nm u- $Al_{0.3}Ga_{0.7}N$
22 nm n-$Al_{0.3}Ga_{0.7}N$
1 nm u-$Al_{0.3}Ga_{0.7}N$
25 nm HT-GaN
Secondary GaN buffer
a-plane GaN buffer
HT-AlN Nucleation Layer
r-plane Sapphire

Layer	Time [s]	Pressure [Torr]	Temperature [°C]	TMG Flow Rate [sccm]	TMA Flow Rate [sccm]	NH_3 Flow Rate [sccm]	Si_2H_6 Flow Rate [sccm]
u-GaN	5	75	1160	12.5	---	5480	---
u-AlGaN	12	75	1160	12.5	30	5480	---
n-AlGaN	134	75	1160	12.5	30	5480	5
u-AlGaN	6	75	1160	12.5	30	5480	---
HT-GaN	150	75	1160	12.5	---	5480	---
Buffer	625	90	1075	47	---	1900	---

Figure 8.5: Epitaxial Structure of Sample E and **Table 8.5:** Growth parameters of Sample E.

Sample E is an iteration on Sample D with a different buffer composition in an attempt to tackle a buffer leakage issue that other non-polar HEMT samples of the same platform face – a dual buffer of one CMP (Chemical-Mechanical Polishing) processed a-plane GaN layer and a second overgrown a-plane GaN buffer, prior to the further growth of identical epitaxial top layers. For experimentation purposes, the utility of fully 3D overgrowth is tested with this sample in an effort to improve the sample's strain characteristics and potentially improve device current performance.

Sample F

22 nm u-$Al_{0.3}Ga_{0.7}N$
1 nm n-$Al_{0.3}Ga_{0.7}N$
2.5 nm u-$Al_{0.3}Ga_{0.7}N$
8 nm HT-GaN
Overgrown GaN buffer
a-plane GaN buffer
HT-AlN Nucleation Layer
r-plane Sapphire

Layer	Time [s]	Pressure [Torr]	Temperature [°C]	TMG Flow Rate [sccm]	TMA Flow Rate [sccm]	NH_3 Flow Rate [sccm]	Si_2H_6 Flow Rate [sccm]
u-AlGaN	131	75	1160	12.5	30	5480	---
n-AlGaN	6	75	1160	12.5	30	5480	5
u-AlGaN	15	75	1160	12.5	30	5480	---
HT-GaN	50	75	1160	12.5	---	5480	---
Buffer	2050	118	1140	40	---	2500	---

Figure 8.6: Epitaxial Structure of Sample F and **Table 8.6:** Growth Conditions of Sample F.

Sample F is one of a delta-doped nature. It is only 1 nm of AlGaN as a 'barrier', in between a thick unintentionally-doped AlGaN cap and a medium thickness AlGaN spacer separating it and a thin HT-GaN region. It too, has a dual-phase buffer. The regrown buffer has slightly adjusted parameters across the board – a longer growth time at a slightly lower temperature and higher pressure, and with the V-III ratio of the aforementioned layer increased – with the hopes of more of a shift towards 2D growth flow rates but keeping a degree of 3D growth for strain adjustment.

Sample G

1.5 nm u-$Al_{0.3}Ga_{0.7}N$

22 nm n+-$Al_{0.3}Ga_{0.7}N$

1.5 nm u-$Al_{0.3}Ga_{0.7}N$

8 nm HT-GaN

Overgrown GaN buffer

a-plane GaN buffer

HT-AlN Nucleation Layer

r-plane Sapphire

Layer	Time [s]	Pressure [Torr]	Temperature [°C]	TMG Flow Rate [sccm]	TMA Flow Rate [sccm]	NH_3 Flow Rate [sccm]	Si_2H_6 Flow Rate [sccm]
u-AlGaN	9	75	1160	12.5	30	5480	---
n-AlGaN	134	75	1160	12.5	30	5480	7
u-AlGaN	9	75	1160	12.5	30	5480	---
HT-GaN	50	75	1160	12.5	---	5480	---
Buffer	2050	118	1140	40	---	2500	---

Figure 8.7: Epitaxial Structure of Sample G and **Table 8.7:** Growth Conditions of Sample G.

Following the same HEMT epitaxial stack formula as Sample C and the same buffers as sample F, but with a stronger doping in the AlGaN barrier and slightly adjusted cap and spacer thicknesses, Sample G is an attempt at addressing a concern with the previous samples; if their activated doping concentration was not high enough, and if the device current density could be improved still. The silane flow rate was increased to 7.

Sample H

2 nm n-GaN

1.5 nm u-$Al_{0.3}Ga_{0.7}N$

22 nm n+-$Al_{0.3}Ga_{0.7}N$

1.5 nm u-$Al_{0.3}Ga_{0.7}N$

25 nm HT-GaN

Overgrown GaN buffer

a-plane GaN buffer

HT-AlN Nucleation Layer

r-plane Sapphire

Layer	Time [s]	Pressure [Torr]	Temperature [°C]	TMG Flow Rate [sccm]	TMA Flow Rate [sccm]	NH_3 Flow Rate [sccm]	Si_2H_6 Flow Rate [sccm]
u-GaN	5	75	1160	12.5	---	5480	---
u-AlGaN	9	75	1160	12.5	30	5480	---
n-AlGaN	134	75	1160	12.5	30	5480	7
u-AlGaN	9	75	1160	12.5	30	5480	---
HT-GaN	150	75	1160	12.5	---	5480	---
Buffer	2050	118	1140	40	---	2500	---

Figure 8.8: Epitaxial Structure of Sample H and **Table 8.8:** Growth Conditions of Sample H.

In consideration of the idea of an addition of a thin n-GaN cap above an epitaxial structure similar to Sample G, Sample H retains the dual-phase buffer template, but sporting a thicker HT-GaN layer like the earlier samples, also in an effort to find a solution to buffer leakage and HEMT drain leakage respectively. The doping concentration remains identical to the previous few.

Sample I

1 nm u-$Al_{0.3}Ga_{0.7}N$

26 nm n+-$Al_{0.3}Ga_{0.7}N$

1 nm u-$Al_{0.3}Ga_{0.7}N$

25 nm HT-GaN

a-plane GaN buffer

HT-AlN Nucleation Layer

r-plane Sapphire

Layer	Time [s]	Pressure [Torr]	Temperature [°C]	TMG Flow Rate [sccm]	TMA Flow Rate [sccm]	NH_3 Flow Rate [sccm]	Si_2H_6 Flow Rate [sccm]
u-AlGaN	5	75	1150	12.5	30	5480	---
n-AlGaN	155	75	1150	12.5	30	5480	7
u-AlGaN	6	75	1150	12.5	30	5480	---
HT-GaN	150	75	1150	12.5	---	5480	---
Buffer	650	118	1060	47	---	1900	---

Figure 8.9: Epitaxial Structure of Sample I and **Table 8.9:** Growth Conditions of Sample I.

Possessing a very thin cap and spacer surrounding a thick strongly-doped barrier with the 'standard single' buffer layout of slightly lower temperature and higher chamber pressure, this is also an effort to improve the current density and crystal quality of the devices grown on this set. The thick barrier is theoretically meant to present a greater amount of charges to the transistor channel while not allowing for much back tunnelling into the doped layer, if the doping concentration is kept at appropriate levels – usually thick barriers at high doping concentrations may mean that most of the charge may not be contained within the intended HT-GaN layer and instead will either leak from the channel or 'short circuit' the drain and source contacts via the barrier itself, which also causes a lack of proper gate modulation of current.

Sample J

1.5 nm n-GaN

15 nm u-$Al_{0.3}Ga_{0.75}N$

12 nm n++-$Al_{0.25}Ga_{0.75}N$

1 nm u-$Al_{0.25}Ga_{0.75}N$

25 nm HT-GaN

a-plane GaN buffer

HT-AlN Nucleation Layer

r-plane Sapphire

Layer	Time [s]	Pressure [Torr]	Temperature [°C]	TMG Flow Rate [sccm]	TMA Flow Rate [sccm]	NH_3 Flow Rate [sccm]	Si_2H_6 Flow Rate [sccm]
u-GaN	4	75	1150	12.5	---	5480	---
u-AlGaN	62	75	1150	12.5	30	5480	---
n++AlGaN	50	75	1150	12.5	25	5480	10
u-AlGaN	4	75	1150	12.5	25	5480	---
HT-GaN	150	75	1150	12.5	---	5480	---
Buffer	650	75	1060	47	---	1900	---

Figure 8.10: Epitaxial Structure of Sample J and **Table 8.10:** Growth Conditions of Sample J.

J is a sample of a cap/secondary top-level barrier composition that is a hybrid of the previous attempts – the thin n-GaN cap combined with a thicker AlGaN secondary barrier and a thin spacer encasing a moderately thick, but strongly doped, AlGaN primary barrier. This is the first of the series to have the primary barrier aluminium composition dropped to (according to measurements and anecdote) ≈ 25%, while the disilane flow rate was increased to 10 sccm.

Sample K

15 nm u-$Al_{0.25}Ga_{0.75}N$

12 nm n++-$Al_{0.25}Ga_{0.75}N$

1 nm u-$Al_{0.25}Ga_{0.75}N$

4 nm HT-GaN

20 nm u-$Al_{0.25}Ga_{0.75}N$

a-plane GaN buffer

HT-AlN Nucleation Layer

r-plane Sapphire

Layer	Time [s]	Pressure [Torr]	Temperature [°C]	TMG Flow Rate [sccm]	TMA Flow Rate [sccm]	NH_3 Flow Rate [sccm]	Si_2H_6 Flow Rate [sccm]
u-AlGaN	62	75	1150	12.5	25	5480	---
n++-AlGaN	50	75	1150	12.5	25	5480	10
u-AlGaN	4	75	1150	12.5	25	5480	---
HT-GaN	4	75	1150	12.5	---	5480	---
u-AlGaN	120	75	1150	12.5	25	5480	---
Buffer	650	75	1060	47	---	1900	---

Figure 8.11: Epitaxial Structure of Sample K and **Table 8.11:** Growth Conditions of Sample K.

Using the principle of Sample J but without the top-level GaN cap and in its stead comprising of a buffer barrier encircling a thin HT-GaN layer in between itself and the usual thin spacer, it was to be seen if a thin HT-GaN layer essentially grown into a quantum well would have helped it in terms of 2DEG mobility as well as observing how that would affect the sheet carrier density overall. All AlGaN layers were kept at an alloy percentage of 25% Al.

Sample L

1 nm u-GaN

15 nm u- $Al_{0.25}Ga_{0.75}N$

12 nm n++-$Al_{0.25}Ga_{0.75}N$

1 nm u- $Al_{0.25}Ga_{0.75}N$

25 nm HT-GaN

a-plane GaN buffer

HT-AlN Nucleation Layer

r-plane Sapphire

Layer	Time [s]	Pressure [Torr]	Temperature [°C]	TMG Flow Rate [sccm]	TMA Flow Rate [sccm]	NH_3 Flow Rate [sccm]	Si_2H_6 Flow Rate [sccm]
u-GaN	4	75	1100	12.5	---	5480	---
u-AlGaN	62	75	1100	12.5	25	5480	---
n++-AlGaN	50	75	1100	12.5	25	5480	10
u-AlGaN	4	75	1100	12.5	25	5480	---
HT-GaN	150	75	1100	12.5	---	5480	---
Buffer	650	75	1060	47	---	1900	---

Figure 8.12: Epitaxial Structure of Sample L and **Table 8.12:** Growth Conditions of Sample L.

The final one of the growth patterns present within the scope of growth, L sees a return to the cap-dual barrier-spacer template used in Sample J, except with an even thinner top-level GaN cap and all 25% Al. The silane flow rate remains identical to the latter two.