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**MOCVD Growth and characterisation of III-nitride semiconductor  
materials for monolithically integrated optoelectronics**

**Chenqi Zhu**

The University of Sheffield  
Department of Electronic and Electrical Engineering  
Centre for GaN Materials and Devices

Supervisor: Professor Tao Wang

May 2022



# Abstract

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There has been a significantly increasing interest in developing III-nitride semiconductor based micro-light-emitting diodes ( $\mu$ LEDs), the key components for future microdisplay systems such as augmented reality (AR), virtual reality (VR), helmet-mounted displays (HMD) and head-up displays (HUD), which require high brightness, high resolution, and high efficiency. An electronic component that is also an essential part for controlling individual  $\mu$ LEDs is also extremely important. However, the performance of  $\mu$ LEDs fabricated using conventional dry-etching methods is far from enough. The ability to monolithically integrate  $\mu$ LEDs and electronics such as high electron mobility transistors (HEMTs) on a single chip is also of great importance. In this thesis, the epitaxial integration of  $\mu$ LEDs and HEMTs has been demonstrated. Fundamental epitaxial work behind the technology has been conducted with a particular focus on GaN grown on a Si substrate.

The growth of GaN on (111) Si substrates is complicated due to a number of fundamental challenges, such as the large lattice mismatch between GaN and silicon and the large difference in the thermal expansion coefficient between GaN and silicon, both leading to a significant amount of tensile strain during the final cooling process, a major reason for wafer cracking. Furthermore, unlike GaN-on-sapphire, GaN-on-Si growth has issues with melt back etching. In this study, the entire process, including the growth mechanism, was investigated in detail. Several new methods were developed. Detailed measurements and analyses were performed to determine the optimal growth conditions. As a result, this study has led to achieving crack-free, high-quality GaN-on-Si crystals that exhibits good surface morphology.

Both electronics and photonics were grown and fabricated on high-quality GaN-on-Si. An AlGaN/GaN-based HEMT was grown on GaN-on-Si, where the influence of the strain status of the device on its performance was investigated. An InGaN/GaN multiple quantum well (MQWs) structure was grown on the GaN-on-Si, which exhibited major differences in terms of optical performance compared with InGaN MQWs grown on sapphire under identical conditions. The strain was found to play an important role in these differences.

This comparative study provides useful information regarding the growth of InGaN with high indium contents for visible LEDs with longer emission wavelengths.

This work also presents a selective epitaxial overgrowth method using pre-patterned micro array templates. The optimisation of this selective overgrowth method resulted in the demonstration of a monolithically integrating  $\mu$ LEDs and HEMTs device onto a single chip. Finally, a prototype of an  $8 \times 8$  microdisplay in which each  $\mu$ LED is controlled by an individual HEMT was demonstrated.

# Acknowledgements

Doing a PhD is never an easy task, especially with the pandemic and other unexpected accidents. However, with the encouragement and help from so many people, I am now grateful to reach my final stage of this journey. I would like to take this opportunity to show my deepest thanks for everything they have done.

I want to show my most sincere gratitude to my supervisor, Professor Tao Wang, who is full of wisdom as well as experience and always willing to share his intelligence to help me. As a very supportive supervisor, his enthusiasm towards both research and life did not only encourage me on my PhD study but also on many other corners in my life and helped to shape me a tougher and stronger personality. Once again, thank him so much for all his support over those years.

I am deeply indebted to Dr. Yuefei Cai, Dr. Xiang Yu and Dr. Yiping Gong, from whom I learnt the most about the experiment and manuscript writing. Thanks for their patience in helping me and showing me the proper attitude towards science and engineering. Following their example, I turned from a student to a researcher step by step.

I would also like to thank Dr Jie Bai, Dr Xiangyu He and Dr. Nicolas Poyiatzis for their assistance with the device fabrication and manuscript proofreading. Thanks for their valuable advice.

I am fortunate to work with Mr. Peng Feng, Mr. Xinchu Chen, Mr. Ce Xu, Ms. Rongzi Ni, Mr. Guillem Martínez de Arriba, Mr. Ye Tian, Mr. Peter Fletcher, Mr. Jack Haggar and Mr. Volkan Esendag. Thanks for all their ideas and suggestions.

I wish to send my thanks to the members who have left the group, which are Dr. Jiu Ling, Dr. Shuoheng Shen, Dr. Xuanming Zhao, Mr. Wei Zhong and Mr. Zhiheng Lin. And I also wish to thank our technician team and the department management team for their support and kind help.

Last but not least, I want to express my deepest, most genuine appreciation to my loved ones. Both my parents and my girlfriend have given me unconditional love and encouragement. They understood my frailty and helped me get through the toughest times

with the softest smiles but the strongest support. As always, I appreciate your endless love and my love for you is the same.

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# List of Publications

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- [1] **C Zhu**, C Xu, P Feng, X Chen, G M de Arriba, J Bai and T Wang, “A comparison study of InGaN/GaN multiple quantum wells grown on (111) silicon and (0001) sapphire substrates under identical conditions”, *Journal of Physics D: Applied Physics*, (Accepted)
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# Chapter 1 Introduction

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## 1.1 The History of III-Nitride Research

III-nitride has now been widely regarded as one of the most significant members of the third-generation semiconductor materials due to their supreme characteristics, such as their high breakdown voltage and their infrared-to-deep-ultraviolet bandgap. Thanks to those advantages, III-nitrides are continuing to draw great attention from both optoelectronic and electronic application areas. Topics around them, such as micro-LED, GaN-based radio-frequency chips and power devices, are most recently attracting enormous investment (both emotionally and economically) from the public, which will keep this hot spot popular for a long time among researchers.

The first GaN semiconductor was produced in 1932 by flowing ammonia gas over gallium metal at high temperatures around 900~1000°C, where GaN appeared in a form of dark grey GaN powders [1]. However, due to the high melting point (>1600°C) and dissociation pressure of GaN, the first single GaN crystal was not produced until 1969, when Maruska and Tietjen [2] deposited GaN on sapphire substrates using a technique known as hydride vapour phase epitaxy (HVPE). This process used ammonia as a nitrogen source and gallium monochloride (GaCl) as a gallium source, where the GaCl was initially synthesized by chemically reacting metallic gallium with chlorine. Only two years later, GaN and AlN were achieved using a metal-organic chemical vapour deposition (MOCVD) technique, in which trimethylgallium (TMG) and trimethylaluminum (TMA) were used as the sources of gallium and aluminium, respectively [3]. However, the single-crystal GaN produced by the techniques described above exhibited a very high density of dislocations and an extremely rough surface morphology because of the severe mismatch between the lattices of GaN and sapphire substrate.

There was a major technological breakthrough in 1986 when a ‘two-step’ GaN growth method was invented by Isamu Akasaki, Hiroshi Amano et al. , resulting in a major step forward in crystal quality and surface morphology [4]. This ‘two-step’ growth method

involved a thin, low-temperature AlN nucleation layer that is initially deposited on a sapphire substrate, followed by the growth of a thick GaN layer at a high temperature. Nakamura [5] simplified this technique by replacing the AlN nucleation layer with a thin, low-temperature GaN nucleation layer. This technique has since been widely utilized for GaN-on-sapphire growth.

Another major breakthrough in GaN-based optical devices occurred in 1989 when Amano et al. [6] achieved the first p-type GaN. This was accomplished by treating as-grown Mg-doped GaN under low-energy electron beam irradiation (LEEBI). Three years later, Nakamura [7] obtained a p-type GaN by simply using an annealing process at around 700°C under a nitrogen ambience. These advancements lead to the birth of the first bright indium gallium nitride/aluminium gallium nitride (InGaN/AlGaN) blue light-emitting diode (LED) reported by Nakamura et al. [8][9] in 1994, followed by the first white LED developed by combining an InGaN blue LED with yellow phosphor in 1995 [10].

Due to their wide bandgaps, III-nitride semiconductors have also attracted a significant amount of attention for their potential applications in power devices. Furthermore, the high electron mobility in the two-dimensional electron gases (2DEG) that naturally form at the interface of AlGaN and GaN in a GaN/AlGaN heterojunction allowed for the development of GaN-based high electron mobility transistors (HEMTs), where the first GaN MEMTs were reported in 1993 [11].

GaN-based photonics and electronic devices have since been used extensively in a variety of applications, including power electronics, radio frequency (RF) wireless communication, and solid-state lighting. Due to their high efficiency, extended durability, and low energy consumption, GaN/InGaN LEDs and LDs are excellent candidates for use in illuminating applications. In addition, GaN-based HEMTs are expected to have major advantages over their silicon-based counterparts, including high power conversion efficiencies, reduced switching losses, and rapid switching speeds.

## **1.2 State-of-the-art and Challenges of III-nitrides**

### **1.2.1 The Growth of GaN on Si**

Although there has been significant progress in the development of III-nitride semiconductors over the past few decades, there are still several major challenges that must

be overcome, such as how to integrate GaN with silicon. Specifically, how can high-quality, crack-free GaN-on-Si be obtained?

One of the fundamental problems is the occurrence of meltback etching between Ga atoms and Si substrates, which refers to the chemical reaction between the two materials at high temperatures [12]. To address this issue, a thick AlN buffer layer must first be grown to separate the Si substrate from the GaN layer subsequently grown. The crystal quality, strain status, and surface morphology of the following GaN layer are strongly influenced by the initial AlN layer growth, where growth conditions such as temperature, V/III ratio, thickness, nitridation, and TMA-preflow have been investigated [13]-[18].

Another major concern that occurs during the growth of GaN on a Si substrate is cracking, which can occur due to the large difference in the coefficient of thermal expansion between GaN and Si. There have been several proposed solutions to this issue, including the utilisation of insertion layers, epitaxial lateral overgrowth (ELO) techniques, carbon nano-tube masks, facet-initiated growth, and patterned substrates [19]-[25]. Among these methods, the utilisation of strain balance layers is an effective approach to compensate for the enormous thermal stress while also reducing the threading dislocation density. Specifically, it is an effective approach that employs a so-called graded AlGa<sub>x</sub>N buffer technique to grow crack-free GaN crystals on Si [26]. These graded buffer layers can be composed of a single AlGa<sub>x</sub>N layer or multiple AlGa<sub>x</sub>N layers with step-graded Al content and optimised Al compositions and thicknesses for each of the AlGa<sub>x</sub>N layers [27],[28]. AlN/GaN superlattices, composed of a low-temperature AlN layer and a thin SiN<sub>x</sub> layer, have also been attempted. It is worth highlighting that each of these solutions has its advantages and can be used in different scenarios [29],[30].

Wafer bowing is another significant challenge that prevents the growth of crack-free GaN on Si. It is particularly problematic in GaN crystals grown on Si substrates with large diameters. This issue is also catalysed by thermal stress, as the compressive stress induced by the strain balance layers to compensate for the tensile thermal stress can also generate large wafer curvatures in the opposite direction. Wafer bowing can be monitored by in-situ curvature monitoring systems [31]-[40]. With the help of these monitoring systems, the wafer curvature, lateral wafer temperature uniformity, and stress status can be

systematically studied by extracting data from the in-situ measurements using the Stoney formula [41].

### 1.2.2 Micro-light-emitting-diodes

A microdisplay is defined as a screen with a diagonal length of less than 25 mm. Microdisplays are expected to be widely used in next-generation display systems such as augmented reality (AR) and virtual reality (VR) systems, helmet-mounted displays (HMD), and head-up displays (HUD). Although organic light-emitting diodes (OLEDs) and liquid-crystal displays (LCD) can be used to manufacture microdisplays, micro-LEDs ( $\mu$ LEDs) overshadow their competitors because they are self-emissive devices with high brightness, tiny form factor, and can achieve higher resolutions. However,  $\mu$ LED technology is still under development, and many aspects require improvement [42]-[45]. For example, to achieve 4K resolution on a glasses-sized wearable AR display system, the luminating pixel size needs to be less than 10  $\mu$ m (or even 4  $\mu$ m), with respect to a sufficient pixel-to-pixel length for other process steps. Furthermore, for a better commercial application, this less-than-10- $\mu$ m space is expected to emit both red, blue and green light with an acceptable brightness.

The optical efficiency of  $\mu$ LEDs at such small sizes is the fundamental barrier (our own case see in the chapter below) to its widespread adoption. These efficiency issues arise in  $\mu$ LEDs due to epiwafer growth and the subsequent fabrication of the device. GaN grown on a sapphire substrate typically have a high density of defects due to the significant mismatch between the lattices of GaN and sapphire. This is even more severe for GaN grown on a Si substrate. During device fabrication, sidewall damage, which becomes particularly important when attempting to reduce the dimensions of the LED, can occur due to dry etching. A number of methods have been proposed to mitigate the damage, such as an annealing process after  $N_2$  plasma treatment, chemical etching processes, and silicon nitride ( $SiN_x$ ) or silicon dioxide ( $SiO_2$ ) passivation [46]-[48]. As shown in *Figure 1.1*, our team has recently developed a direct epitaxy approach based on the idea of selective growth that results in the natural formation of  $\mu$ LEDs in which dry-etching processes are not involved. Our technique eliminates damage caused by dry-etching [49]-[51].

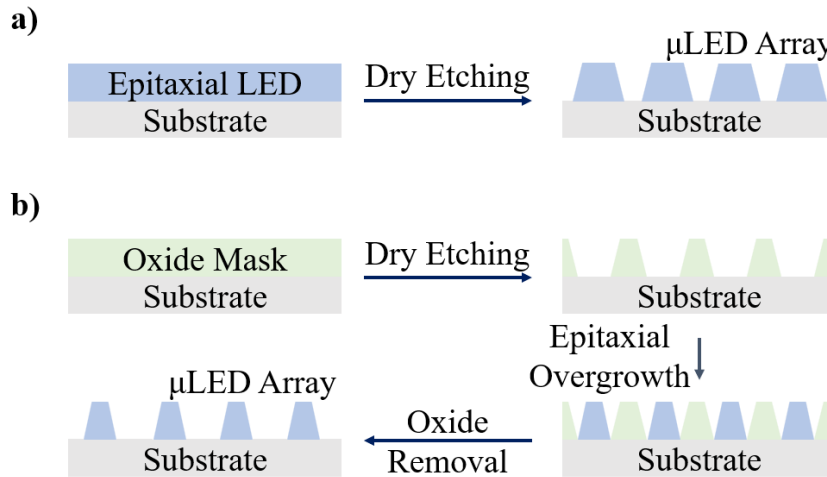


Figure 1.1 Process flow of a) conventional micro-LED array fabrication and b) Selective area overgrown micro-LED array.

The fabricated  $\mu$ LED pixels must then be individually electrically connected. One of the most popular methods is known as “pick-and-place”, which involves the transfer and alignment of millions of  $\mu$ LED pixels from a wafer to another substrate with a backplane, a process that requires extremely high precision. Therefore, this approach may not be suitable for mass production, especially when higher resolutions are required, which necessitates an even further reduction of the dimensions of  $\mu$ LEDs.[52]-[55] Another way to achieve this is flip-chip bonding, which involves heterogeneous integration via wafer bonding techniques [52],[56]-[62] and would still stick to the original substrate, which is abandoned in the “pick-and-place” method. However, in some cases, this approach has similar issues due to the precision required for alignment if the pixels need to be bonded on the electrical control circuit during this step and can lead to a further reduction in the optical performance of  $\mu$ LEDs [56]-[60],[63]-[65].

Furthermore,  $\mu$ LED display technologies face additional problems when it comes to enabling RGB full-colour displays, where the individual control of  $\mu$ LEDs in a fast and stable manner is required.

### 1.3 Motivation and Aims

GaN-based microdisplays currently face many challenges. However, our group believes that the monolithic on-chip epitaxy integration of  $\mu$ LEDs and high electron mobility transistors (HEMTs) that are capable of electrically controlling individual  $\mu$ LEDs could be

the most promising approach to manufacturing microdisplays. We have developed an epitaxial growth approach that involves the natural formation of  $\mu$ LEDs on a pre-patterned template in a process that does not involve dry-etching, hence avoiding any potential etching damage [49]-[51]. As a result, we have demonstrated ultra-compact LEDs, which can be found in Figure 1.2, with record external quantum efficiencies (EQE) of 9% at  $\sim 500$  nm [49],[50]. In addition, this project aims to investigate the growth methods used for the epitaxial integration of  $\mu$ LEDs and HEMTs, leading to the demonstration of an  $8 \times 8$  monolithically integrated  $\mu$ LEDs/HEMTs microdisplay on a single chip.

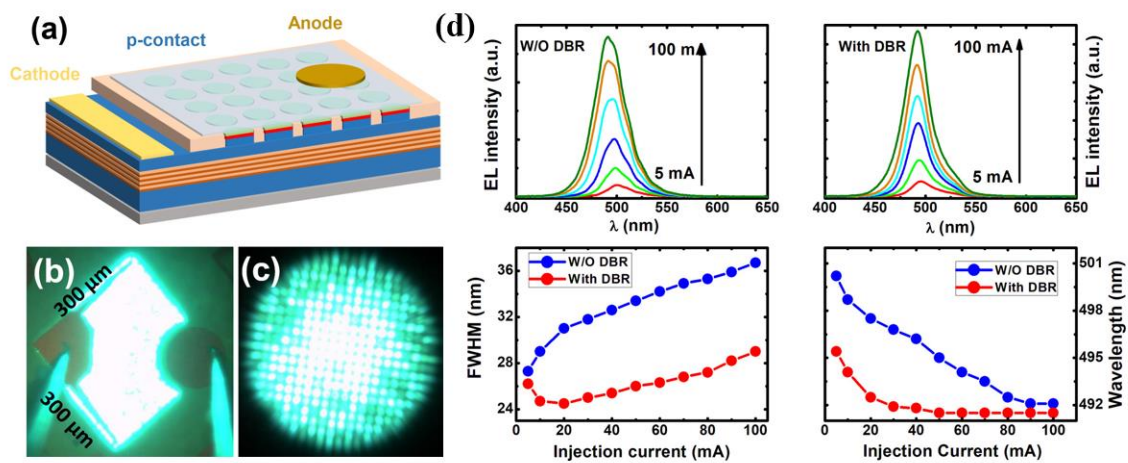


Figure 1.2 (a) Schematic drawing of our ultra-compact (a diameter of  $3.6 \mu\text{m}$  and an interpatch of  $2 \mu\text{m}$ )  $\mu$ LED arrays. (b) Emission microscopy images of our  $\mu$ LED arrays at an injection current density of  $15 \text{ A/cm}^2$  under a low magnification and (c) under a high magnification. (d) EL spectra of the  $\mu$ LED arrays without and with DBRs, both measured as a function of injection current at room temperature. The fwhm of EL spectra for both devices as a function of injection current. Emission peak wavelength of both devices as a function of injection current.

Another research objective was to apply this epitaxial integration method to a Si substrate to produce crack-free GaN-on-Si with high-quality crystals and good surface morphology. Furthermore, a detailed investigation into the growth of individual optical and electrical devices such as LEDs and HEMTs on Si substrates and their advanced characterisation is crucial.

## 1.4 Outlines

Chapter 1 provides a brief overview of the history of the development of III-nitride semiconductors, the challenges faced by GaN-on-Si growth, and the current state of microdisplay research. It also discusses the main motivations and aims of this investigation.



Chapter 2 briefly introduces the general background of III-nitride semiconductors, including their physical characteristics and fundamental principles, as well as the issues faced by III-nitride semiconductor devices. The problems associated with GaN-on-Si development are also discussed.

Chapter 3 presents the main experimental techniques employed in this project, including the initial epitaxy growth, material characterisation, and device fabrication. This involves techniques and instruments such as MOCVD (growth), XRD, SEM, Microscopy, AFM and PL (characterisation), PECVD, RIE, ICP and photolithography (device fabrication).

Chapter 4 primarily investigates each step of the growth of GaN on a Si substrate. This includes the treatment of the Si substrate surface, an investigation into vertical temperature uniformity, AlN growth, AlGaN growth, and GaN growth.

Chapter 5 focuses on the investigation of the growth of both GaN-based electronics and photonics on Si substrates. The performance and strain status of GaN/AlGaN HEMT structures and InGaN/GaN structures are also studied.

Chapter 6 demonstrate a prototype of an integrated device, namely,  $8 \times 8$  monolithically integrated  $\mu$ LEDs/HEMTs microdisplay on a single chip, which was achieved by our direct selective area overgrowth technology.

Chapter 7 provides a summary of the work and potential avenues for future research.

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# Chapter 2 Background

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## 2.1 Semiconductors

Materials are classified as either solids, liquids, gases, or plasmas. Solid materials can be further categorised as conductors, insulators, or semiconductors based on their electric conductivity. The conductivity of an insulator is typically very low, in the range of  $10^{-8}$ – $10^{-18}$  S/cm<sup>-1</sup> due to the absence of free electrons[1]. Similarly, the conductivity of conductors, such as metals, is very high due to a large number of free electrons and often falls between  $10^4$ – $10^6$  S/cm<sup>-1</sup>[1]. The conductivity of semiconductors falls between these values, and their conductivities can be tuned by an external process.

### 2.1.1 Band Structure

Due to their periodic structures, there are distinct energy levels in which electrons can exist in a semiconductor. Figure 2.1 describes how the terms ‘valence band’ and ‘conduction band’ refer to the highest occupied and the next unoccupied energy bands of a single crystalline solid at absolute zero, assuming no external processes, respectively, while the energy gap between them is referred to as a ‘forbidden gap’ or bandgap [2].

While the Fermi levels of insulators and semiconductors fall within their bandgaps, conductors have their Fermi levels covered by both their valence and conduction bands, allowing the electrons in a conductor to move freely. In addition, the Fermi level of an insulator is far from any current-carrying state, and its bandgap is so large that electrons in the valence band cannot be energised and driven into the conduction band through thermal energy or an external electric field. Consequently, electrons in the valence band are unable to move freely. In contrast, the Fermi levels of a semiconductor may be tuned by doping.

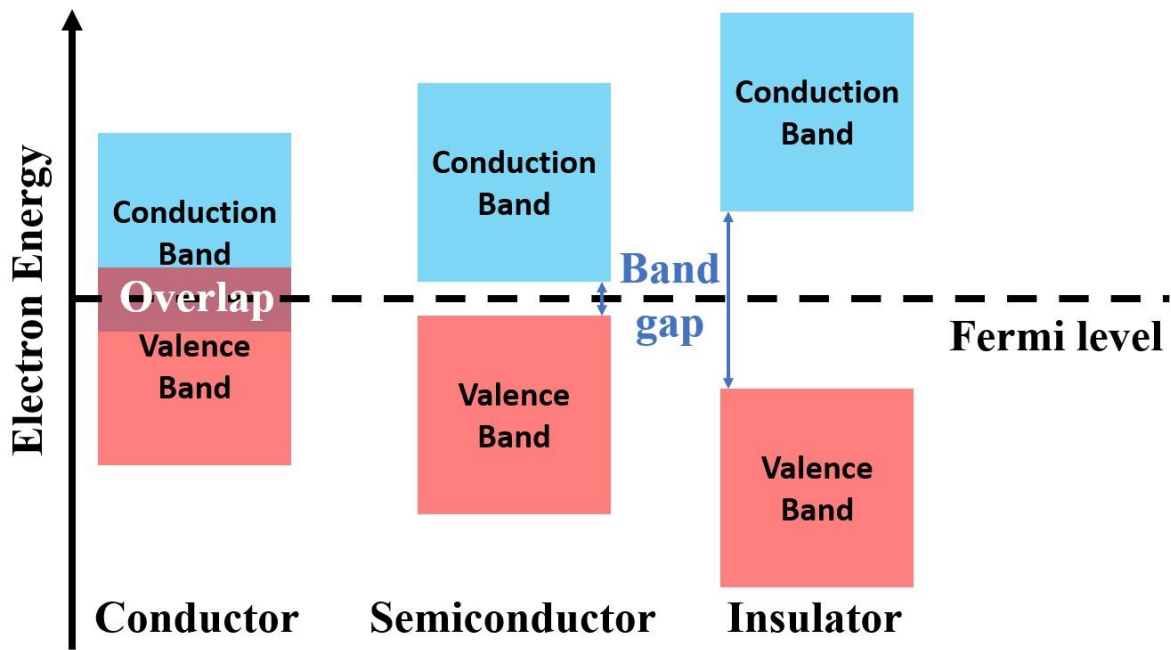


Figure 2.1 Diagram that describes the band structures of conductors, semiconductors, and insulators.

Figure 2.2 shows that there are two kinds of band structures exhibited by semiconductors: direct bandgap and indirect bandgap, which are defined by the alignment of a semiconductor's valence band maximum and conduction band minimum in a  $k$ -space or momentum space. A direct bandgap semiconductor exhibits the same values for the valence band maximum and conduction band minimum, while these values in indirect bandgap semiconductors have a different  $k$  value. The recombination between electrons and holes in a direct bandgap semiconductor is different from an indirect bandgap semiconductor, as carrier recombinations in indirect bandgap semiconductors require a third party to maintain the conservation of momentum [3].

Semiconductors can absorb light to create electrons and holes; this can also be accomplished using an injection process. Following the absorption of light, carrier recombination occurs, either through a radiative recombination process or a non-radiative recombination process. Figure 2.2 also demonstrates the recombination of electrons and holes in a direct bandgap and an indirect bandgap semiconductor. In the case of an indirect bandgap semiconductor, an additional phonon must be involved in the recombination process to preserve the conservation of energy-momentum ( $k$ ), significantly reducing the carrier recombination rate and thus its quantum efficiency, while the carrier recombination process in a direct bandgap semiconductor does not require the involvement of a third party.

Thus, direct semiconductors are commonly used in the fabrication of light-emitting diodes or laser diodes.

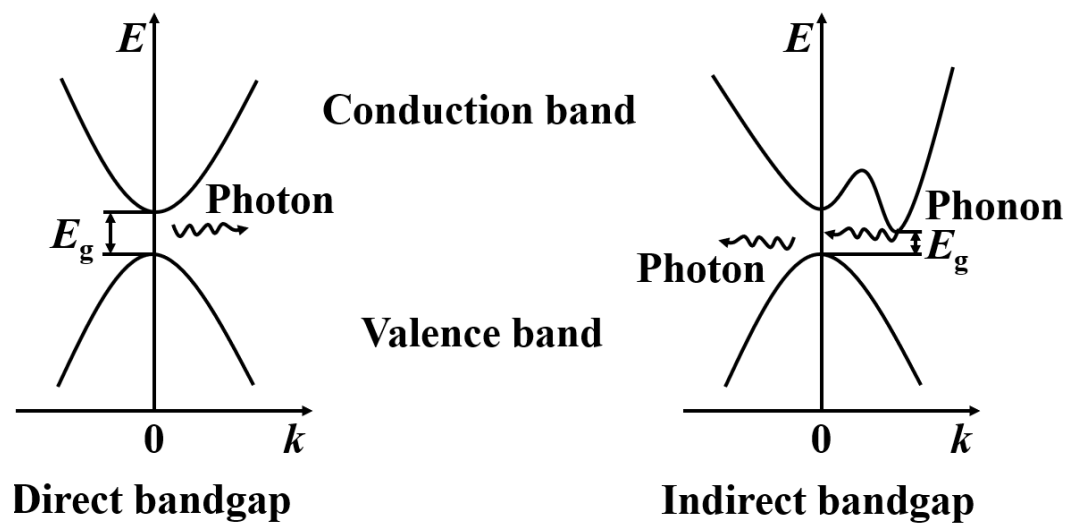


Figure 2.2 Schematic of a recombination process between electrons and holes in semiconductor: a direct bandgap; and an indirect bandgap

### 2.1.2 Doping

The electrical properties of a semiconductor can be modified through doping, which introduces impurities that generate more free carriers in the form of either electrons or holes. A doped semiconductor can be typically classified as either a p-type (acceptor) or an n-type (donor) semiconductor. Using III-nitride materials as an example, a small amount of Group II elements, such as magnesium (Mg), can be doped onto gallium nitride (GaN), causing the gallium (Ga) atoms to be replaced by Mg atoms, generating an extra energy level just above the valence band. This process causes Mg-doped GaN to become a p-type semiconductor. Similarly, by doping GaN with a small amount of group IV elements, such as silicon (Si), Ga atoms are substituted with Si atoms, forming an n-type semiconductor with a high concentration of free electrons at room temperature [4].

### 2.1.3 Recombination

When an electron is excited and moves from the valence band to the conduction band, it generates a hole in the valence band, forming an electron-hole pair (EHP). The excited electron will eventually return to the valence band, a process known as recombination. This recombination process can occur in one of three ways: Shockley-Read-Hall (SRH) recombination, radiative recombination, and Auger recombination.

Figure 2.3a illustrates the mechanisms behind the SRH recombination process [5],[6], in which the trap formed by the impurity or imperfections in the material is the main cause of recombination. The arrows in the figure indicate that these electrons can gradually revert to the valence band through the energy levels induced by those traps. Compared to the size of the bandgap, the energy involved in this kind of recombination is relatively small and thus multiple phonons are involved rather than a photon. This recombination process is dominant at low injection currents. Specifically, the rate of SRH recombination ( $R_{SRH}$ ) is dependent on the carrier concentration and trap density, and can be expressed as follows:

$$R_{SRH} = An \quad (2.1)$$

Where  $A$  denotes the coefficient of SRH recombination and  $n$  denotes the carrier concentration.

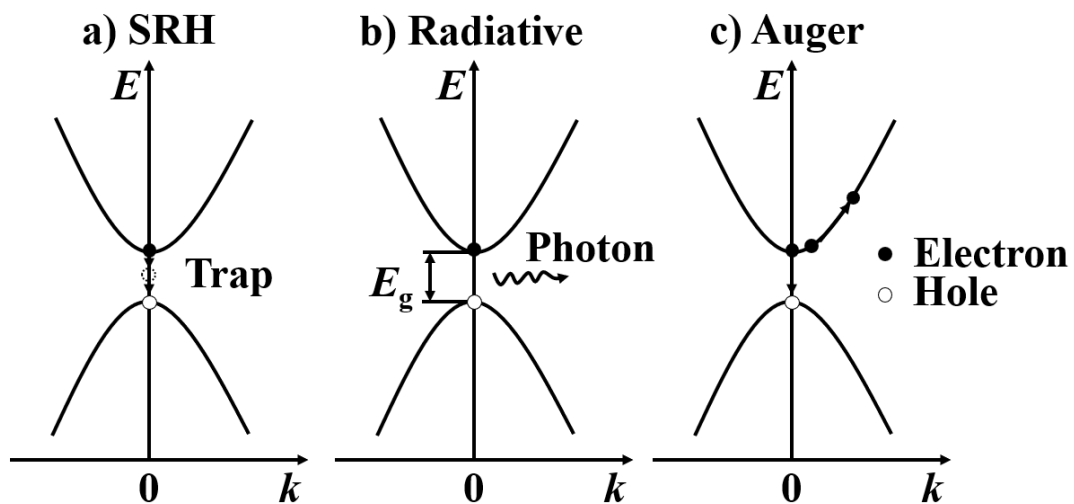


Figure 2.3 Three types of the recombination process: (a) SRH recombination, (b) Radiative recombination and (c) Auger recombination.

Figure 2.3b demonstrates the radiative recombination process, which leads to the generation of photons that we require. It is notable that Figure 2.3b only illustrates band-to-band recombination – radiative recombination can also take place through excitonic recombination and donor-acceptor recombination. In each of the radiative recombination processes, the excited electron returns to the valence band by emitting a photon. However, in band-to-band recombination, the energy of the emitted photon is determined by the bandgap between the conduction band and the valence band. In contrast, the energy of the emitted photon is decreased in excitonic or donor-acceptor recombination because of the

exciton binding energy or the activation energy of the specific dopants. Generally, a carrier recombination rate for radiative recombination can be expressed as follows:

$$R_{Rad} = Bn^2 \quad (2.2)$$

where  $B$  is the radiative recombination coefficient, which typically ranges between  $10^{-9}$ – $10^{-11}$   $\text{cm}^3/\text{s}$  for III-nitrides [7].

Finally, Figure 2.3c describes an Auger recombination process, where the energy obtained when an excited electron returns to the valence band results in the excitation of another electron (or hole) in the conduction band (valence band) to a higher energy state resulting in a hot electron (hole), rather than the generation of photons. This form of recombination is particularly noticeable at large injection currents and has been accepted as one of the main causes of efficiency droop.[8] Because the hot electron will ultimately lose energy via the emission of phonons (lattice vibration or heat), the Auger recombination process is non-radiative. The recombination rate of an Auger recombination process is expressed as follows:

$$R_{Aug} = Cn^3 \quad (2.3)$$

where  $C$  is the Auger coefficient of recombination.

Another important parameter for describing a carrier recombination process in a semiconductor is the carrier recombination lifetime. Carrier recombination lifetime is an important parameter in general illumination, display, and visible light communication (VLC) applications, where short recombination lifespans are desirable. Normally, the non-radiative recombination term is relative to temperature and defect density. The total recombination lifetime of a semiconductor material may be described in terms of both radiative ( $\tau_{rad}$ ) and non-radiative ( $\tau_{non-rad}$ ) lifetimes, as indicated in the following equation [9]:

$$\frac{1}{\tau} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{non-rad}} \quad (2.4)$$

## 2.2 III-Nitrides Semiconductors

Unlike Si or Ge semiconductors, which consist of single elements, compound semiconductors are formed by the combination of group III and V elements. One of the most compelling reasons to use compound semiconductors is the ability to tune their bandgaps by adjusting their alloy composition. For example, the bandgaps of GaN, indium nitride (InN), aluminium nitride (AlN), as well as their ternary or quaternary alloys, extent from the deep ultraviolet to the infrared spectral regions, covering the entire visible spectrum (Figure 2.4). These materials are also referred to as III-nitrides, and they all exhibit direct bandgap structures. Hence, they have significant advantages over conventional III-V semiconductors, potentially making III-nitrides one of the best choice for optoelectronic devices.

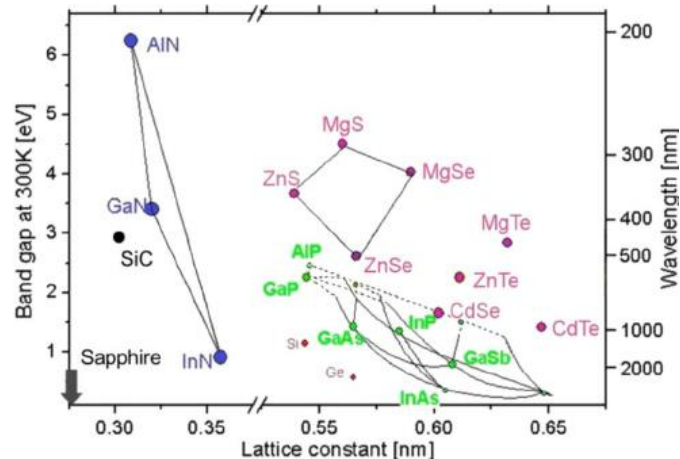


Figure 2.4 Bandgap at room temperature and emission wavelength as a function of the lattice constant of various compound semiconductors [10]. Reused with permission.

### 2.2.1 Crystal Structure

In general, III-nitride semiconductors can exhibit three distinct crystal structures: wurtzite, zincblende, and rock-salt [11]. GaN with a rock-salt structure can only exist at very high pressures, while GaN with a zincblende structure can be formed on a cubic substrate. This zincblende structure can potentially transform into a wurtzite structure, which is much more thermodynamically stable [12]. Thus, GaN with a wurtzite structure is the most useful class of III-nitride semiconductors [13],[14]. This dissertation will thus be exclusively dedicated to the research of wurtzite-structured III-nitride semiconductors.

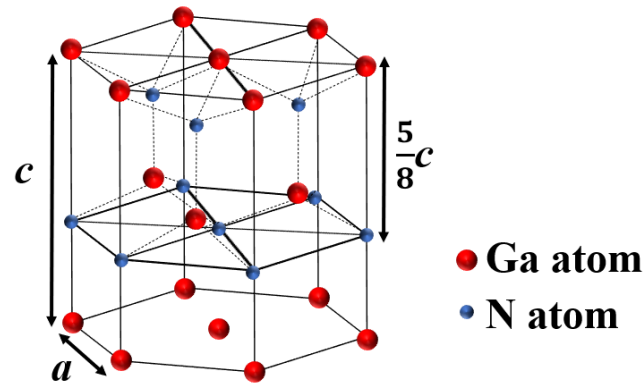


Figure 2.5 Schematics of III-nitride semiconductor (GaN) with the wurtzite crystal structure.

Figure 2.5 is a schematic representation of a wurtzite GaN, where the small blue dots represent nitrogen atoms, while the larger red dots represent Ga atoms. In this crystal structure, each nitrogen atom naturally bonds to four Ga atoms, represented by the dashed lines in the figure. This results in an ABABAB hexagonal-close-packed (HCP) configuration for the crystal. The two HCP sublattices of Ga and N have an interpenetrating offset that is equal to 5/8 of the height of the cell. In addition, the in-plane lattice constant ( $a$ ) and the out-of-plane lattice constant ( $c$ ) of a wurtzite structure – as labelled in Figure 2.5 – are used to describe the distance between two adjacent atoms within the same basal plane and the distance between two adjacent basal planes, respectively.

Table 2-1 Lattice constants of wurtzite III-nitrides.

	AlN	GaN	InN
In-plane lattice constant ( $a$ ) (Å)	3.111	3.189	3.533
Out-of-plane lattice constant ( $c$ ) (Å)	4.982	5.185	5.693

The lattice constants of the III-nitrides (GaN, AlN, and InN) are listed in Table 2-1 [15].



Bravais Miller indices  $(h, k, i, l)$  are used to describe the crystal lattice's plane and orientation [16]. The three vectors  $a_1, a_2$  and  $a_3$  (Figure 2.6) describe the orientations of the basal planes, which are represented by the indices  $(h, k, i)$ . Additionally, the index  $l$  denotes the intercept reciprocals along the  $c$  axis. In a wurtzite structure, the Miller and  $i$  indices are equal to  $-(h + k)$ ; thus, the Miller indices of a wurtzite structure are sometimes expressed as  $(h, k, l)$ .

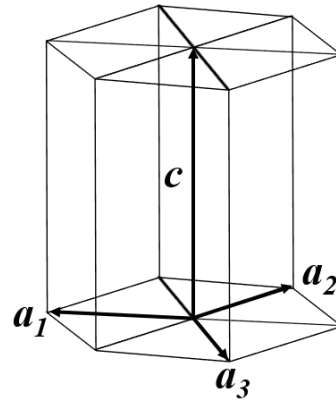


Figure 2.6 Bravais Miller indices in a wurtzite unit cell.

There are two distinct formations of GaN crystals, each with a different terminating atom on the surface: the formation that involves terminating gallium atoms is referred to as a Ga-polar (Miller index of  $(0001)$ ) structure, while the formation that involves terminating nitrogen atoms, is known as an N-polar (Miller index of  $(000\bar{1})$ ). Nitrogen atoms on the N-face surface can easily react, resulting in the decreased stability of N-face GaN. As a result, chemical etching processes may occur rapidly owing to surface defects or N-polar GaN, but intrinsic GaN with a Ga-polar structure are very chemically stable. In addition, the physical and chemical properties of these two polarities can vary significantly, altering the growth process and resulting in highly distinct optical and electrical capabilities.

### 2.2.2 Properties

The fundamental material parameters of GaN are compared to other semiconductor materials in Table 2-2 [17],[25]. In particular, electron mobility is one of the most important parameters for a semiconductor, which describes how rapidly electrons may move when an electric field is applied. This parameter is impacted by the quality of the crystal components, such as lattice vibrations, impurities, and defects. The electron mobility in freestanding GaN has been measured to be as high as  $1245 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  at room temperature [26]. In

addition, an epilayer of high-quality GaN generally has an electron mobility of around 1000  $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ . Table 2-2 also highlights that GaN has an extremely high breakdown voltage and great thermal conductivity compared to GaAs and Si, which are indicative of GaN's potential uses in the fabrication of high-power, high-frequency electronic devices.

Table 2-2 Electrical and thermal properties of semiconductor materials at 300K [17]-[25].

Material	Melting Point ( $^{\circ}\text{C}$ )	Thermal Conductivity ( $\text{W}\cdot\text{cm}^{-1}\text{K}^{-1}$ )	Electron Mobility ( $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ )	Breakdown Field ( $\text{kVcm}^{-1}$ )
GaN	2500	2.3	1245	5000
GaAs	1238	0.55	9400	400
InP	1062	0.68	4000	500
Si	1414	1.56	1400	300

In addition, the chemical stability of GaN is significantly greater than that of its competitors; this is due to its polarity and crystal purity. For example, Ga-polar GaN cannot be etched in the most common acidic and alkaline solutions [27], whereas N-polar GaN and surface defects on Ga-polar GaN may be etched by phosphoric acid ( $\text{H}_3\text{PO}_4$ ) and potassium hydroxide (KOH) [27].

### 2.2.3 Alloys and Tuneable Bandgaps

As mentioned above, the bandgap and lattice constants of III-nitride materials can be tuned by changing the composition of the semiconductor alloys. The lattice constants can be expressed as a linear relationship between the alloy compositions as defined by Vegard's law:

$$a_{A_xGa_{(1-x)}N} = xa_{AN} + (1-x)a_{GaN} \quad (2.5)$$

where  $a_{AN}$  denotes the lattice constant of the III-Nitride material (Al or In in most cases),  $a_{GaN}$  refers to the GaN lattice constant, and  $x$  refers to the mole fraction of the group III elements (Al or In).

Due to its close relationship with the lattice constants, the bandgap of a ternary alloy is highly dependent on the alloy composition, which can be described as an empirical equation as follows:

$$Eg_{A_xGa_{(1-x)}N} = xEg_{AN} + (1 - x)Eg_{GaN} - bx(1 - x) \quad (2.6)$$

where  $Eg_{AN}$  represents the bandgap of AlN or InN,  $Eg_{GaN}$  represents the bandgap of GaN, and  $B$  is a bowing factor that is associated with curvature and strain state.

The bandgaps and emission wavelengths of III-nitrides can be found in Table 2-3 [7]. Both Table 2-3 and Figure 2.4 show that InN has a small bandgap and that its ternary alloys with GaN can cover the entirety of the visible light spectrum (380–740 nm), while a ternary alloy consisting of AlN and GaN has the potential to be used in applications involving the deep ultraviolet (DUV) and ultraviolet (UV) spectra. Hence, the bandgap energies of III-nitride ternaries can be continuously tuned by varying their alloy compositions, which allows for these materials to cover a wavelength range from 6.2 eV (200 nm) to 0.78 eV (1590 nm), suggesting the high possibility for their use in light luminance applications ranging from the infrared to the ultraviolet, as well as for visible light communication.

*Table 2-3 Bandgaps and relative emission wavelength of III-nitrides materials.*

III-nitride Materials	Bandgap (eV)	Corresponding Wavelength (nm)
AlN	6.2	200
GaN	3.42	363
InN	0.78	1590

## 2.2.4 Internal Polarizations

III-nitride semiconductors and their heterojunctions exhibit intrinsic polarisation due to the asymmetry of their wurtzite structure, which determines the fundamental properties of III-nitride optoelectronics. In general, the dipole moments in semiconductors with a symmetric crystal structure can cancel each other out, causing the system to have a dipole moment of zero, macroscopically. Figure 2.5 shows that, due to the asymmetry of wurtzite GaN, these dipoles are not cancelled out, causing the net dipole moment to point in the [000-1]

direction, resulting in the spontaneous polarisation of the wurtzite GaN structure. As shown in Figure 2.7a, the value of the spontaneous polarisation of GaN, InN, and AlN can be calculated via Vegard's interpolation (Equation 2.7). In unstrained III-nitrides, the spontaneous polarisation was found to be -0.029, -0.032, and -0.081 C/m<sup>2</sup> in GaN, InN, and AlN, respectively [28].

$$P_{sp,A_xGa_{(1-x)}N} = xP_{sp,AN} + (1-x)P_{sp,GaN} \quad (2.7)$$

where  $P_{sp,AN}$  denotes the spontaneous polarisation of the III-nitride material (AlN or InN for most cases),  $P_{sp,GaN}$  denotes the spontaneous polarisation of the GaN, and  $x$  is the mole fraction of the group III elements (Al or In).

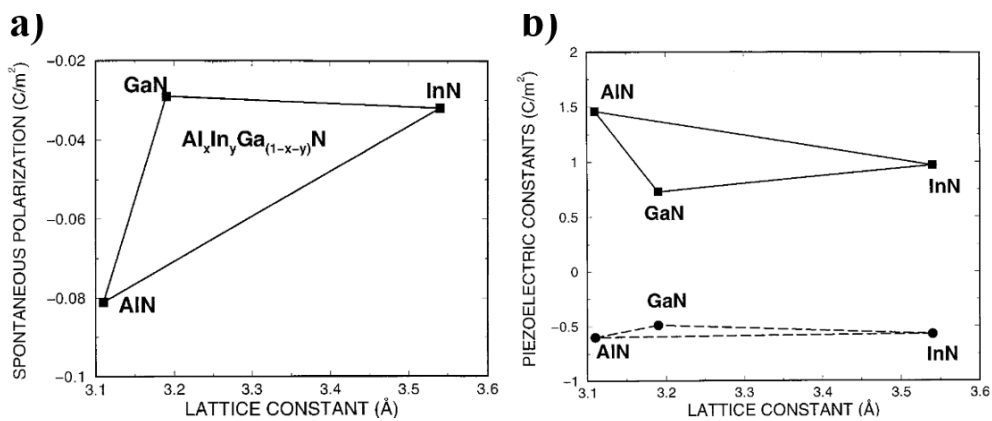


Figure 2.7(a) The spontaneous polarizations of III-nitrides as a function of the lattice constant, as well as the spontaneous polarizations of III-nitride alloys according to a Vegard-like rule. (b) The piezoelectric coupling constants of III-nitrides  $e_{31}$  (dash line) and  $e_{33}$  (solid line) as a function of lattice constants. According to a Vegard-like rule, triangles indicate III-nitride alloys [29]. Reused with permission.

Each of the above-mentioned spontaneous polarisations is calculated based on unstrained materials.

Under strained conditions, the group III and N atoms are displaced from their equilibrium positions, resulting in an extra polarisation field known as piezoelectric polarisation. This strain can be described as a combination of the isotropic in-plane strains  $\epsilon_{xx}$  and the out-of-plane strain  $\epsilon_{zz}$ , which can be determined by the strained in-plane and out-of-plane lattice constants  $a$  and  $c$  as well as their corresponding equilibrium lattice constants  $a_0$  and  $c_0$ . In particular, the relationship between the strain and the lattice constants can be expressed by the equation below:

$$\varepsilon_{xx} = \varepsilon_{yy} = \frac{(a - a_0)}{a_0} \quad (2.8)$$

$$\varepsilon_{zz} = \frac{(c - c_0)}{c_0} \quad (2.9)$$

The piezoelectric polarisation can then be calculated from the in-plane strains  $\varepsilon_{xx}$  and out-of-plane strain  $\varepsilon_{zz}$  using the following equation:

$$P_{pz} = e_{31}(\varepsilon_{xx} + \varepsilon_{yy}) + e_{33}\varepsilon_{zz} \quad (2.10)$$

where  $e_{31}$  and  $e_{33}$  are the piezoelectric constants (see Figure 2.7b) [28].

Thus, the total polarisation includes both spontaneous and piezoelectric polarisation, which can be expressed by the equation below:

$$P = P_{sp} + P_{pz} \quad (2.11)$$

Figure 2.7 shows the spontaneous polarisation and piezoelectric coefficients of III-nitrides and their alloys as a function of the lattice constant. The intrinsic spontaneous polarisation of heterostructures such as AlGa<sub>x</sub>N/GaN or InGa<sub>x</sub>N/GaN results in the formation of a self-built electric field. AlN exhibits a spontaneous polarisation coefficient that is approximately three times larger than that of GaN, while InN has a similar spontaneous polarization coefficient to GaN. However, the lattice mismatch between GaN and AlN is much smaller than the mismatch between GaN and InN.

Therefore, in an AlGa<sub>x</sub>N/GaN heterostructure, the spontaneous polarisation formed along [000-1] is dominant, while the piezoelectric polarisation, which also forms along [000-1], is fairly weak. Similarly, for an InGa<sub>x</sub>N/GaN heterostructure such as an InGa<sub>x</sub>N/GaN quantum well (QW), the piezoelectric polarisation dominates and is oriented in the opposite direction of the spontaneous polarisation.

The distribution of the spontaneous and piezoelectric polarisation in a c-plane InGa<sub>x</sub>N/GaN QW structure can be found in Figure 2.8a. Because the polarisation is oriented in the growth direction, the charges built at the interface between the GaN barrier and the InGa<sub>x</sub>N QW create an opposing electric field. As shown in Figure 2.8, this built-in electric field separates

the holes and electrons in opposing directions, causing the band structure to be deformed and consequently resulting in the separation of the wave functions of the electron and its hole. This electric field-induced phenomenon is referred to as the quantum-confined Stark effect (QCSE).

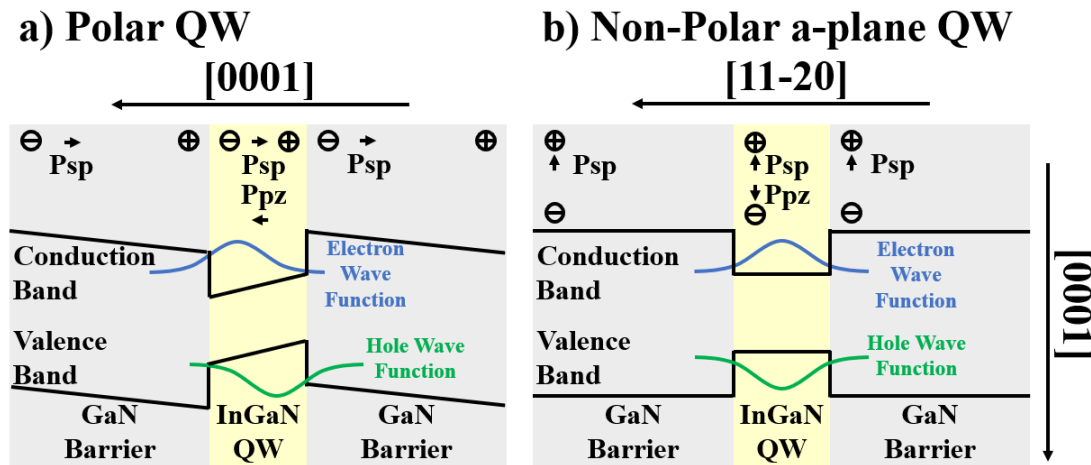


Figure 2.8 Schematic representation of the orientation of polarisation and the band structure of (a) a polar c-plane InGaN/GaN QW and (b) a non-polar a-plane InGaN/GaN QW.

The QCSE phenomenon strongly influences the performance of an III-nitride heterostructure in many ways. For example, the induced reduction of the integral wave function overlaps of electrons and holes leads to an increase in the radiative recombination lifetime, which can decrease the internal quantum efficiency (IQE) of InGaN/GaN-based visible emitters for general illumination while also limiting the maximum modulation bandwidth for VLC applications. In addition, the modification of their band diagram decreases the transition energy between the conduction band and valence band, resulting in a redshift in the emission wavelength. With increasing injection currents, a blueshift in the emission wavelength occurs due to a carrier-induced screening effect (Consider an electron flow in which every electron repels each other and therefore forms small regions around themselves due to the Coulomb's interaction. And those small regions, which can be regarded as "screening holes", will cancel the electric fields generated by those electrons.), generating a wavelength stability issue.

Furthermore, the QCSE phenomenon presents a great challenge for the growth of an InGaN/GaN QW structure for long emission wavelengths (such as green, yellow or even red), as it requires much higher In concentrations. InGaN/GaN QW structures with higher

In contents results in stronger built-in electric fields, leading to a further reduction in the wave function overlap between the holes and electrons and, consequently, even more severe QCSE. This is one of the greatest challenges for the development of long emission wavelength high-efficiency III-nitride LEDs.

### 2.2.5 Structure of an LED

Figure 2.9a presents a typical (and very conventional) LED structure with a simple p-n junction. The formation of a depletion region between the n-type and p-type sides results in the formation of a built-in electric field across the depletion region. In an open circuit, this built-in electric field tends to stop carrier diffusing carriers, eventually forming an equilibrium. This is shown in Figure 2.9b, which demonstrates the behaviour of electrons and holes in a zero-biased p-n junction using a band diagram.

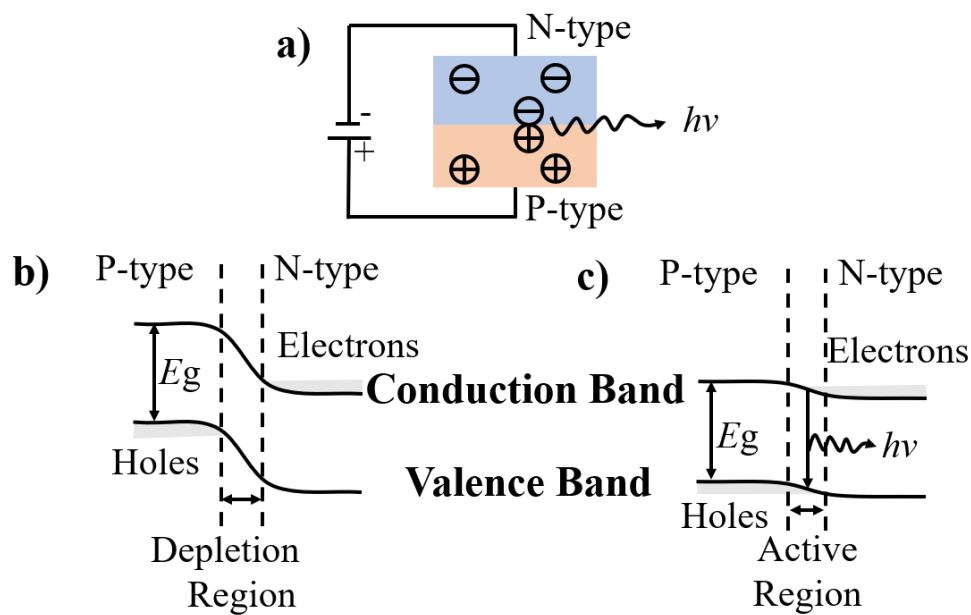


Figure 2.9 (a) Schematic of a forward-biased p-n junction. This figure also shows the energy band diagram of (b) a zero-biased p-n junction and (c) a forward-biased p-n junction.

Figure 2.9 shows a p-n junction under biased conditions, in which electrons and holes can continuously diffuse into the opposite area. In a forward-biased p-n junction LED, minority carriers, such as electrons, in the p-type region can radiatively recombine with majority carriers, such as holes, in the p-type region, resulting in the emission of photons.

### 2.2.6 High-Electron-Mobility Transistor (HEMT)

III-nitrides like GaN can also be used in power devices; their applications in this field have attracted an increasing amount of attention in recent decades [30]-[32]. Compared to Si, GaN has a wider bandgap, which means GaN-based power devices can reach much higher breakdown voltages than their Si-based counterparts.

As mentioned in Section 2.2.4, the asymmetry of the structure of wurtzite GaN allows for intrinsic polarisation [33]. Thus, modulation doping, which typically forms two-dimensional electron gases (2DEG) in AlGaAs/GaAs-based high electron mobility transistor structures, is no longer necessary in AlGaN/GaN-based power devices as 2DEG can simply be formed at the interface between the AlGaN and GaN in an AlGaN/GaN heterostructure due to intrinsic polarisation.

In addition, the 2DEG layer between AlGaN and GaN has a high sheet carrier density and electron mobility, and thus possesses lower on-state resistance compared to Si/SiC-based devices [33],[34].

The two fundamental parameters can be used to describe the major advantages of GaN-based power devices: Baliga's figures of merit (BFoM) and Johnson's figure of merit (JFoM). These values are presented in Table 2-4, where  $E_c$  denotes the critical electric field strength,  $v_{sat}$  denotes the saturation velocity,  $\epsilon$  represents the dielectric constant, and  $\mu$  is the electron mobility (for GaN, it describes the electron mobility in the 2DEG layer between AlGaN and GaN).

*Table 2-4 A comparison of FoM values for power device applications between Si, SiC, and GaN. The BFoM and JFoM methods are used to determine the low- and high-frequency performance of power devices, respectively.*

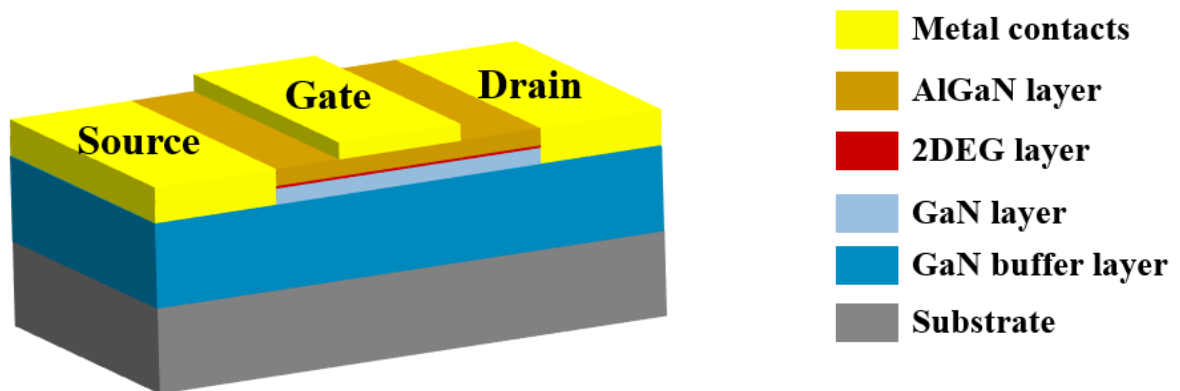
Figure of Merit	Si	4H-SiC	GaN
BFoM ( $\epsilon\mu E_c^3$ )	1	130	650
JFoM ( $E_c v_{sat}/2\pi$ )	1	180	760

The BFoM parameter is commonly used to assess the performance of power devices at low frequencies. This figure is a measure of the trade-off between on-state resistance and breakdown voltage [35]. As previously mentioned, GaN-based power devices can have



high breakdown voltages and low conduction losses due to their crystal properties. Hence, the BFoM of GaN is much higher than that of Si and SiC.

The JFoM is a measure of the performance of an electronic device when used for high-frequency power switching [36]. This is primarily controlled by the saturation velocity of the device material and the applied voltage. For an AlGaN/GaN heterostructure, the generated 2DEG layer greatly increases electron mobility, resulting in better performances at high frequencies than Si or SiC power devices.



*Figure 2.10 Structure of an AlGaN/GaN HEMT.*

The fundamental structure of a normally on AlGaN/GaN HEMT grown on a foreign substrate (usually c-plane sapphire or (111) Si) is illustrated in Figure 2.10. Typically, this structure is composed of a thick GaN buffer layer that separates an AlGaN/GaN heterostructure from the substrate. In most cases, this buffer layer needs to be at least semi-insulating to prevent the buffer from being ‘punched through’ in an off-state [37]. As explained previously, the channel in an AlGaN/GaN HEMT heterostructure is achieved by the 2DEG layer. In addition to the parts needed for the compound semiconductor, three metal contacts are required for a HEMT. Two ohmic contacts are required, one serving as a drain and the other as a source (represented by the yellow blocks in Figure 2.10). In addition, a gate contact or a Schottky contact is employed on top of the AlGaN layer surface and is located between the source and drain. Normally, these contacts are formed by depositing metal alloys onto the system, which are then subjected to an annealing process. Typically, a Ti/Al/Ni/Au alloy is used for the ohmic contact, while a Ni/Au alloy is used for the Schottky contact. Under zero bias, the current passes straight through the 2DEG layer from drain to source and, consequently, the device is ‘on’. However, when a bias is

applied to the gate, the electric field will deplete the 2DEG layer beneath the gate and eventually close off the channel. The minimum voltage that must be applied to the gate to switch the channel ‘off’ is known as the threshold voltage ( $V_{th}$ ). As mentioned previously, a normally on device generally does not meet energy consumption or safety requirements. Hence, research into normally off HEMTs is necessary.

The three main parameters used to fully describe the performance of a HEMT device are the breakdown voltage ( $V_{br}$ ), the on-state resistance ( $R_{on}$ ), and the drain current ( $I_{DS}$ ). Specifically,  $V_{br}$  is describing the highest off-state voltage that a transistor may reach before its breakdown. This breakdown might occur vertically or laterally, depending on the geometry of the device. The lateral breakdown is from the gate/source electrodes, while a vertical breakdown is in the buffer layers. Hence, the breakdown voltage can be increased in two ways: 1) by improving the buffer resistivity to increase both the vertical and lateral breakdown voltage; 2) by increasing the gate-drain spacing to improve the lateral breakdown voltage.

On-state resistance ( $R_{on}$ ) is another important parameter for qualifying HEMT performance. This parameter describes the conduction loss of a device due to ohmic contact resistance and 2DEG channel sheet resistance. As previously stated, the 2DEG channel sheet resistances is the main characteristic of  $R_{on}$ . Therefore, decreasing the gate-drain spacing can weaken  $R_{on}$  significantly; this involves a trade-off with the breakdown voltage, which is also influenced by gate-drain separation.  $R_{on}$  is often calculated from the linear part of the I-V characteristics of a device and is typically normalised to the gate width of a device for comparative purposes.

Finally, the drain current ( $I_{DS}$ ) is a critical parameter that affects the current rating of a device. When a bias is applied across the device, the  $I_{DS}$  can be determined by the sheet resistance of the 2DEG channel and the voltage applied. The drain current initially linearly increases as the applied voltage is increased – this occurs until the  $I_{DS}$  saturates. The value of the  $I_{DS}$  can be calculated using the equation below:

$$I_{DS} = n_s \times v_{eff} \times q \quad (2.12)$$

where  $n_s$  denotes the sheet charge density,  $q$  denotes the electronic charge, and  $v_{eff}$  refers to the effective electron velocity in the channel area. This equation shows that increasing

$n_s$  can be an effective way of improving  $I_{DS}$ . For a typical AlGaIn/GaN HEMT, the value of  $n_s$  can reach  $1 \times 10^{13} \text{cm}^{-3}$ , leading to high conductivities in the 2DEG channel. Like  $R_{on}$ ,  $I_{DS}$  is usually normalised to the gate width of the described transistor for comparisons with similar devices.

### **2.2.7 Challenges**

There have been major advancements in the development of III-nitride visible LED technologies in the last few decades, though these have been primarily restricted to III-nitride devices on c-plane substrates. This section describes the major obstacles and basic concerns regarding several fundamental issues in the growth of III-nitrides, such as crystal properties, epitaxial substrates, efficiency droop and the QCSE.

#### **Crystal Properties**

As mentioned in the section above, wurtzite GaN crystals have high melting points and dissociation pressures, and therefore cannot be effectively obtained by the commonly used Czochralski or Bridgman methods, in which single-crystal boules are normally extracted straight from the melt [38],[39]. Due to the lack of affordable substrates, less expensive foreign substrates such as sapphire, silicon, and silicon carbide are now commonly employed in III-nitrides for research and commercial purposes.

Heteroepitaxial growth with the presence of such large lattice mismatches results in a great degree of dislocation, posing major obstacles for optical and electrical applications, as these dislocations can function as non-radiative recombination centres or as paths for leakage currents. Typically, these dislocations can be around  $10^9$ – $10^{10} \text{cm}^{-2}$  for GaN-on-sapphire and are even larger for GaN-on-silicon.

As mentioned in Section 2.2.4, InGaIn/GaN QW structures, which are typically used as an emitting region for visible emitters, suffer from strong built-in electric fields. Furthermore, to achieve longer emission wavelengths such as green, yellow, or even red, higher In concentrations are necessary, leading to more severe piezoelectric polarisation, which further reduces optical quantum efficiency. This is referred to as the “green/yellow gap” [40].

#### **Epitaxial Substrates**

Among sapphire, silicon, and silicon carbide, the three major substrates used in the growth of GaN, SiC has the least lattice mismatch with GaN and AlN but is the most expensive. Sapphire is the most widely used substrate for the growth of III-nitrides semiconductors. Although Si is not the optimal substrate for the growth of III-nitrides, it is the ideal substrate for integrated circuits and has a mature production industry; hence, they are the least expensive and offer the most potential for future integration applications. Other substrates are also available for GaN growth but are much less competitive, such as zinc oxide (ZnO) [41] or diamond [42]; these substrates will not be discussed in this work.

The lattice mismatch between SiC and GaN is 3.5% [43]; hence, the growth of GaN crystals on SiC is preferable compared to other foreign substrates. However, there are two kinds of SiC, 4H-SiC and 6H-SiC, which exhibit different stacking sequences and thus leads to differences in the penetration of stacking faults that are generated during GaN growth. Furthermore, SiC is similar to GaN in that it has a high melting point and dissociation pressure, and thus its production incurs high costs. Consequently, the growth of GaN on SiC substrates is the most expensive of the three substrates.

Sapphire, a single-crystal aluminium oxide ( $\text{Al}_2\text{O}_3$ ), is the most widely used substrate for GaN growth. Sapphire has excellent thermal and chemical stability. Furthermore, the thermal expansion coefficients of GaN and sapphire are relatively similar. These physical properties make sapphire an ideal substrate for epitaxial growth. Furthermore, sapphire is transparent and is thus suitable for use in optical devices in both the UV and the visible spectral regions.

Not only is c-plane sapphire the most used substrate for polar GaN growth, but r-plane sapphire is the preferred substrate for non-polar a-plane GaN growth. However, the lattice mismatch between GaN and sapphire along the m-direction is 16 % compared to 1% along the c-direction [44].

Silicon technology is well developed and has been widely used in semiconductor devices and integrated circuits for decades. Si substrates are cheaper than other substrates. However, it is difficult to grow high-quality GaN crystals on silicon. Silicon has a cubic crystalline structure, in contrast to wurtzite GaN. The lattice mismatch between GaN and Si is 17% for the most commonly used components: (111) Silicon and c-plane GaN [45]. In addition, the coefficient of thermal expansion of Si is 54% smaller than that of GaN [46]; because

GaN must be grown at high temperatures, this results in a large amount of tensile stress when the GaN-on-Si wafer cools. Even if this tensile stress can be compensated for by the use of stress management buffer layers, severe wafer bowing generated by the stress can result in poor uniformity throughout the wafer, making further fabrication problematic; these issues are exacerbated for larger-scale substrates. The challenges of GaN-on-Si growth will be explained in further detail later in the thesis.

### **Efficiency Droop**

The term “efficiency droop” refers to the phenomena in which the efficiency of an LED initially increases with increasing injection current density (below  $10 \text{ A/cm}^2$ ) before quickly decreasing with increasing injection current density. Although the mechanisms that underlie efficiency droop on III-nitride LEDs are debated, both Auger recombination and electron leakage have been considered to be the most likely explanations. Carrier delocalisation, density-activated defect recombination (DADR), reduced current injection efficiency, and current crowding may also contribute to this problem.

### **Quantum Confined Stark Effect**

QCSE which significantly affect the optical performance of c-plane InGaN/GaN quantum wells based emitters is caused by the built-in electric field which leads to the separation of the wavefunction overlap of electrons and holes.

The QCSE causes many issues that degrade the optical performance of III-nitride emitters. For example, due to the modification of the band diagram, III-nitride emitters exhibit redshifts in their emission wavelength. The QCSE can be screened out by increasing the injection current – however, this leads to a blueshift in the emission wavelength and, consequently, an emission wavelength instability issue. Other consequences of the QCSE include an increased radiative recombination lifetime, which generally leads to a reduction in the IQE for general illumination applications and reduced modulation bandwidth in VLC applications. Therefore, the QCSE significantly constrains the development of InGaN/GaN QW structures for long emission wavelengths (such as green, yellow, or even red) because the InGaN QW layer requires much higher In concentrations. However, because the built-in electric field in InGaN/GaN QWs becomes stronger as the In content increases, this is

one of the most challenging obstacles to the development of a long emission wavelength GaN-based LED structure.

## 2.3 III-Nitrides on Silicon Substrates

### 2.3.1 Lattice Mismatches

III-nitrides with a wurtzite structure, such as GaN, AlN, or InN, have a hexagonal six-fold surface symmetry as shown in Figure 2.11c, while Si crystals have a cubic structure and thus a four-fold surface symmetry as shown in Figure 2.11a. A common problem is that GaN crystals with different orientations can appear simultaneously when GaN is grown on (001) silicon, leading to a rough surface.

Figure 2.11b shows that the (111) Si plane has a three-fold surface symmetry, which is more similar to the hexagonal six-fold surface symmetry exhibited by wurtzite GaN as shown in Figure 2.11d. Hence, the (111) crystal plane of Si may be compatible with wurtzite GaN, forming the basis of a mechanism for GaN-on-Si growth.

Furthermore, due to the roughly 17% lattice mismatch between GaN and Si, GaN crystals are subjected to significant tensile stress in GaN-on-Si systems, as can be determined by the following equation:

$$f_{GaN/Si} = \frac{a_{GaN} - \frac{\sqrt{2}}{2} a_{Si}}{\frac{\sqrt{2}}{2} a_{Si}} \quad (2.13)$$

where  $a_{Si}$  is the in-plane lattice constant of cubic Si and  $a_{GaN}$  is the in-plane lattice constant of wurtzite GaN.

### 2.3.2 Thermal Expansion Coefficient Mismatch

The difference in the thermal expansion coefficient between the GaN and Si represents another major issue for GaN-on-Si growth. There is a 54% difference in the thermal expansion coefficient between GaN and Si, which results in significant tensile stress as GaN-on-Si wafers are cooled following crystal growth at high temperatures. This generates enormous tensile stress, causing a severe wafer bowing issue and cracking issues. Even if this tensile stress can be compensated for through the use of stress management buffer

layers, wafer bowing is still a serious issue that results in nonuniformity across the entire wafer. This issue becomes more severe with increasing substrate diameters.

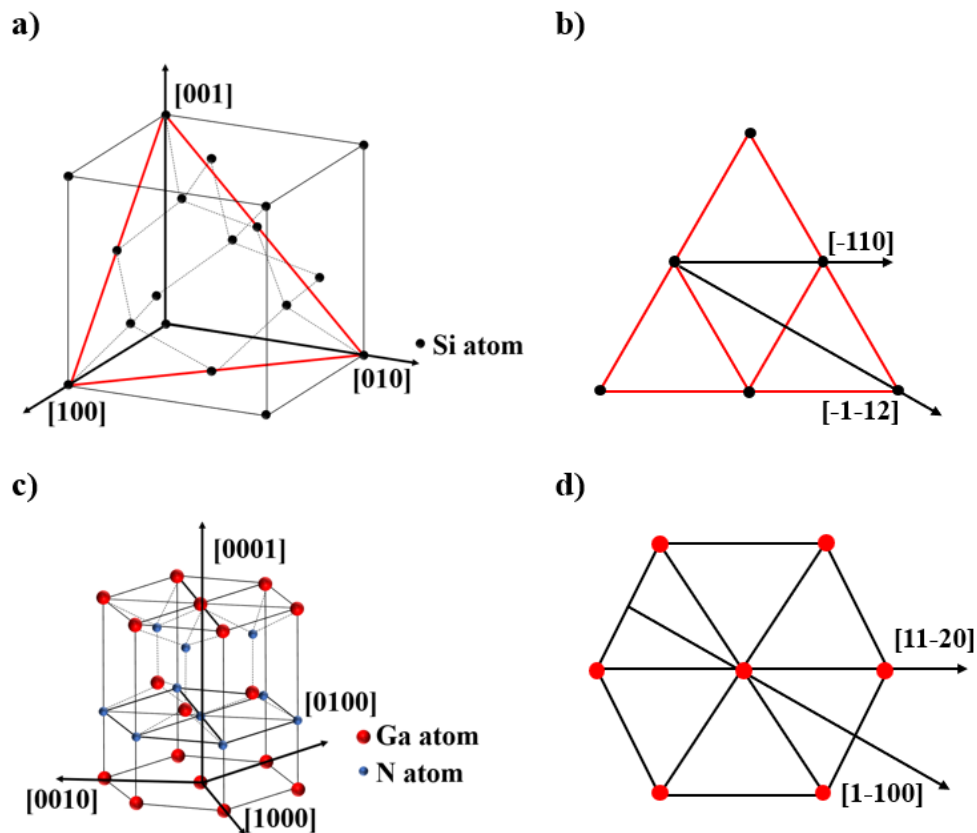


Figure 2.11 (a) Cubic Si crystal structure; (b) Si atoms on the (111) Si plane; (c) Wurtzite GaN crystal structure; (d) Gallium atoms on the (0001) GaN plane.

### 2.3.3 Meltback Etching

Unlike sapphire and SiC substrates, Si can chemically react with GaN to form a eutectic alloy at high temperatures, with growth generally starting at around 1000°C. Therefore, rough surfaces tend to be produced when GaN is directly deposited onto a Si substrate due to Ga meltback issues. To prevent this so-called ‘meltback etching’ effect, a thick AlN buffer layer must be grown between the GaN and the Si substrate. It is important to note that any areas with pits or increased roughness in the AlN buffer layer may result in localised meltback etching; hence, the thickness and surface roughness of the AlN buffer layer must be optimised. Meltback etching can be eliminated if the crystals are grown below 870°C. However, such low temperatures are not optimal for GaN growth as these conditions result in an extremely high density of crystal defects.

## 2.4 Monolithic Integration of HEMT and LED

In the previous sections, two major GaN based optoelectronic devices, HEMT and LED, are detailed introduced. Due to the superior performances of HEMT at high voltage, temperature and frequency, it is quite nature to try to drive an LED device with a homogeneous HEMT structure. However, many prior work has been done before this idea really comes true. Some groups tried to combine a metal–oxide–semiconductor field-effect transistor (MOSFET) with an LED [47][48], while some others tried to achieve light emitting field effect transistor (FET) on HEMT [49]. Since the late 2010s, many groups have started to report more reliable monolithic integration results for HEMT and LED. [50]-[54]

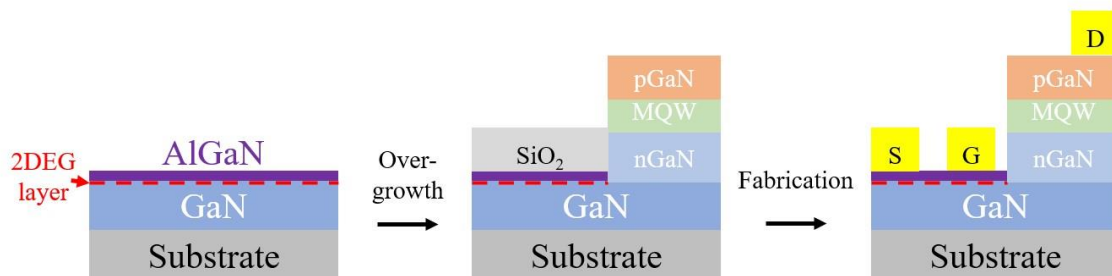


Figure 2.12 Typical fabrication process flow-chart of the monolithic integration of LED and HEMT

As shown in Figure 2.12, a typical fabrication process of the monolithic integration of LED and HEMT would start from the SiO<sub>2</sub> mask deposition on an AlGaN/GaN HEMT template. After patterning and etching this mask, the required LED growth window will be exposed for the next LED structure growth. Finally, the metal electrodes of this integrated device would be fabricated after the SiO<sub>2</sub> mask removal. In this structure, the drain of the HEMT structure will also act as the P-contact of the LED part. By this means, the LED and HEMT are connected metal-freely through the 2DEG layer of the HEMT structure and therefore lower energy loss and higher modulation frequency can be obtained.



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## Chapter 3 Experimental Techniques

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### 3.1 Metal-organic chemical vapour deposition (MOCVD)

#### 3.1.1 Introduction

Metal-organic chemical vapour deposition (MOCVD), also known as metal-organic vapour phase epitaxy (MOVPE), is one of the most commonly used epitaxial growth techniques for producing III-V (e.g. GaN, GaAs, or InP) semiconductor compounds for optoelectronic and electronic devices. All samples described in this thesis were grown using this technique.

Two MOVPE systems were used for the samples grown in this thesis. Both systems were equipped with a close-coupled showerhead (CCS), allowing for the group III precursor(s) and group V precursor(s) to be vertically injected separately into the growth chamber. The first instrument was manufactured by Thomas-Swan Scientific Ltd, which was acquired by AIXTRON Ltd. In this instrument, the showerhead is fixed on top of the growth chamber; however, the growth chamber can move vertically to allow for wafer loading and unloading. The second instrument was manufactured by AIXTRON Ltd. and features a growth chamber with a flip-top configuration. This allows the chamber to be opened by simply flipping the top.

In both systems, the distance between the showerhead and the susceptor which holds substrates for epitaxial growth is very short (approximately 11 mm), a design that minimises any potential parasitic reactions between the group III precursor(s) and group V precursors, particularly with regards to Al(Ga)N growth. Both instruments allow for 3×2-inch or 1×4-inch wafer systems, meaning that three 2-inch wafers or a single 4-inch wafer can be grown in each growth run. The susceptor uses a high rotation speed to ensure that the crystals grow uniformly [1]. The two instruments are similar, but the differences in chamber size and the specifications of the heating system lead to different growth conditions in each system.

### a) Aixtron Reactor



### b) Thomas-Swan Reactor

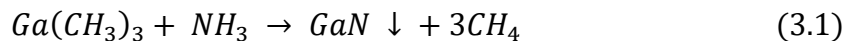


Figure 3.1 Photos of the MOCVD systems used in this thesis: (a) Aixtron 3×2” flip-top CCS reactor; (b) Thomas-Swan 3×2” vertical CCS reactor.

### 3.1.2 Growth Principles

Trimethylgallium (TMGa), trimethylaluminum (TMAI), and trimethylindium (TMIn) were chosen as the precursors for the group III elements gallium (Ga), aluminium (Al) and indium (In), while ammonia (NH<sub>3</sub>) was chosen as the group V element precursor. Magnesium (Mg) and disilane (Si<sub>2</sub>H<sub>6</sub>) are the typical precursors used for n-type and p-type doping, respectively.

The synthesis of a single GaN film on a substrate is the result of a series of chemical reactions between group III and group V precursors that takes place on the substrates as they are held in a susceptor at high temperatures. For example, the growth of GaN on either sapphire or Si substrates requires a mixture of NH<sub>3</sub> and vapourised TMGa as the reactants. Like gaseous NH<sub>3</sub>, the vapourised TMGa involved in the reaction must be carried from the bubbler by a carrier gas, which is usually either pure hydrogen (H<sub>2</sub>) or pure nitrogen (N<sub>2</sub>).



Growth processes are complicated and involve a series of gas-phase and surface reactions [2],[3]. Specific details can be found in Table 3-1.

An example of a gas-phase reaction is the formation of adducts by TMG and NH<sub>3</sub> in a gas-phase mixing process, which is then transported to a heating area. The reaction is very complicated and highly dependent on heating and mixing conditions. The consequence is the mixture of TMG with NH<sub>3</sub> increases the rate of CH<sub>4</sub> formation with a few amides, as the mixing process of TMG and NH<sub>3</sub> takes place at a low temperature (close to room

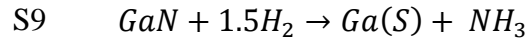
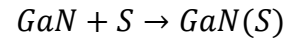
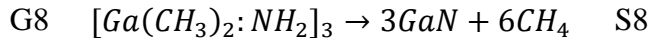


temperature) which will be then heated quickly [4]. Because the reaction occurs under low-pressure conditions, the effects of some of the complex parasitic reactions can be considered to be negligible [5].

Surface reactions take place at the surface of the substrate, and determine the growth rate of the crystals [3]. The relevant reaction equations can be found in Table 3-1, where  $S$  refers to a free surface site. Equations S5, S6, and S7 can be used to estimate the deposition rate of GaN, while S9 can be used to determine the effects caused by the use of  $H_2$  as a carrier gas, which can cause etching at high temperatures [5].

Table 3-1 Gas-phase and surface reactions involved in the growth of GaN by MOCVD.

Gas-phase reactions		Surface reactions	
No.	Reaction equation	No.	Reaction equation
G1	$Ga(CH_3)_3 \rightarrow Ga(CH_3)_2 + CH_3$	S1	$Ga(CH_3)_3 + S \rightarrow Ga(S) + 3CH_3$
G2	$Ga(CH_3)_2 \rightarrow GaCH_3 + CH_3$	S2	$Ga(CH_3)_2 + S \rightarrow Ga(S) + 2CH_3$
G3	$GaCH_3 \rightarrow Ga + CH_3$	S3	$GaCH_3 + S \rightarrow Ga(S) + CH_3$
G4	$Ga(CH_3)_3 + NH_3$ $\rightarrow Ga(CH_3)_3:NH_3$	S4	$Ga + S \rightarrow Ga(S)$
G5	$Ga(CH_3)_3:NH_3$ $\rightarrow Ga(CH_3)_3 + NH_3$	S5	$Ga(CH_3)_3:NH_3 + 2S$ $\rightarrow GaN + 3CH_4$
G6	$Ga(CH_3)_3:NH_3$ $\rightarrow Ga(CH_3)_2:NH_2$ $+ CH_4$	S6	$Ga(CH_3)_2:NH_2 + 2S$ $\rightarrow GaN + 2CH_4$
G7	$3[Ga(CH_3)_2:NH_2]$ $\rightarrow [Ga(CH_3)_2:NH_2]_3$	S7	$[Ga(CH_3)_2:NH_2]_3 + 6S$ $\rightarrow 3GaN + 6CH_4$



A summary of the standard steps in the MOCVD growth procedure is presented as follows (see also Figure 3.2):

1. The group III precursors (TMGa, TMAI or TMIIn) and group V precursor ( $\text{NH}_3$ ) are supplied to the substrate; the group III precursors are supplied using a carrier gas, typically either  $\text{H}_2$  or  $\text{N}_2$ .
2. The atoms or molecules diffuse from the gas phase onto the surface of the substrate.
3. The atoms or molecules are adsorbed onto the heated substrate/susceptor surface.
4. The atoms or molecules migrate to the crystallization zones. Normally, this step involves the transport of reactants from the susceptor to the substrate. However, in the case of selective area growth, this step also represents the transport of atoms and molecules from the mask area to the growth window area.
5. Surface reactions and the resultant decomposition of chemicals.
6. Desorption and decomposition of by-products followed by convection and diffusion back into the gas phase.
7. Extraction of the by-products and the carrier gas from the reacting area and the chamber.

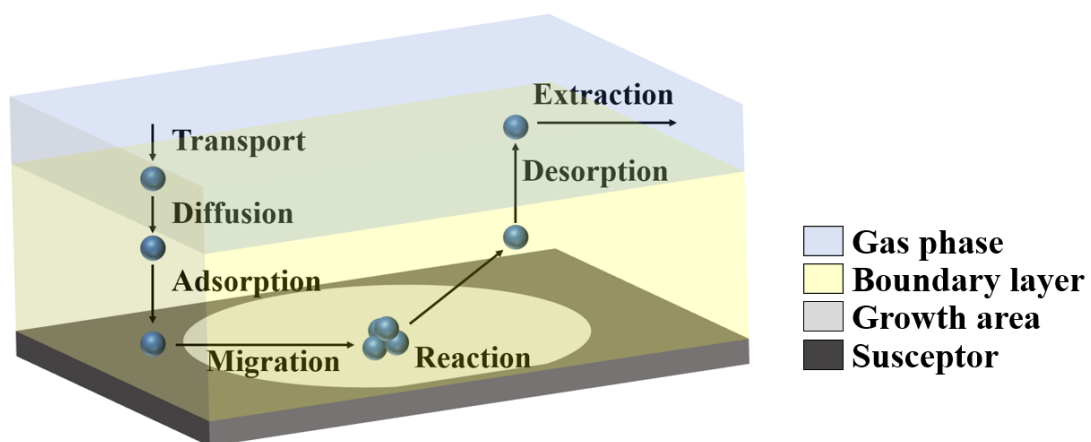


Figure 3.2 Standard reaction steps for an MOCVD growth process.

### 3.1.3 Gas System

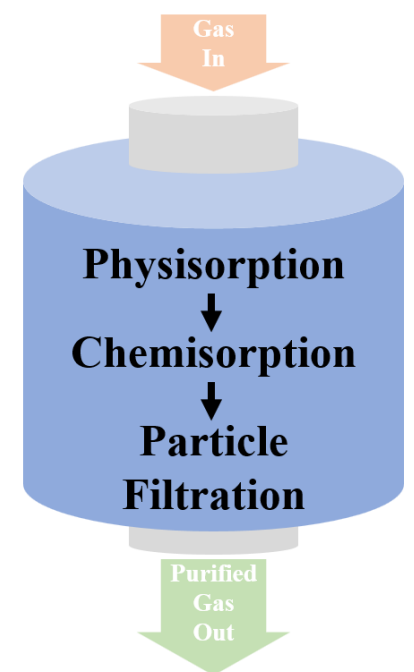


Figure 3.3 The schematic description of the In-line purifier.

#### Purifiers

Both the carrier gas (either  $H_2$  or  $N_2$ ) and the group V precursor ( $NH_3$ ) must pass through their corresponding purifiers before entering the MOCVD gas system. In-line purifiers are used for the purification of  $N_2$  and  $NH_3$ . Figure 3.3 shows that this type of purifier utilises physisorption, chemisorption, and particle filtration and does not require an additional heating or pressurising assembly. However, it can only remove some residual water ( $H_2O$ ), oxygen ( $O_2$ ), or carbon dioxide ( $CO_2$ ). For example, the unpurified  $NH_3$  source used in this thesis is white ammonia with a purity of 99.99999%.

A palladium membrane purifier is typically used for  $H_2$  purification. Figure 3.4 presents a photo and the schematic of the  $H_2$  purifier system used in this thesis. At palladium cell temperatures over  $300^\circ C$  (the standard working temperature of this system is  $400^\circ C$ ),  $H_2$  is the only gas that is small enough to diffuse through the palladium membrane. Hence, the palladium membrane purifier can produce  $H_2$  at a much higher purity than the in-line purifier.

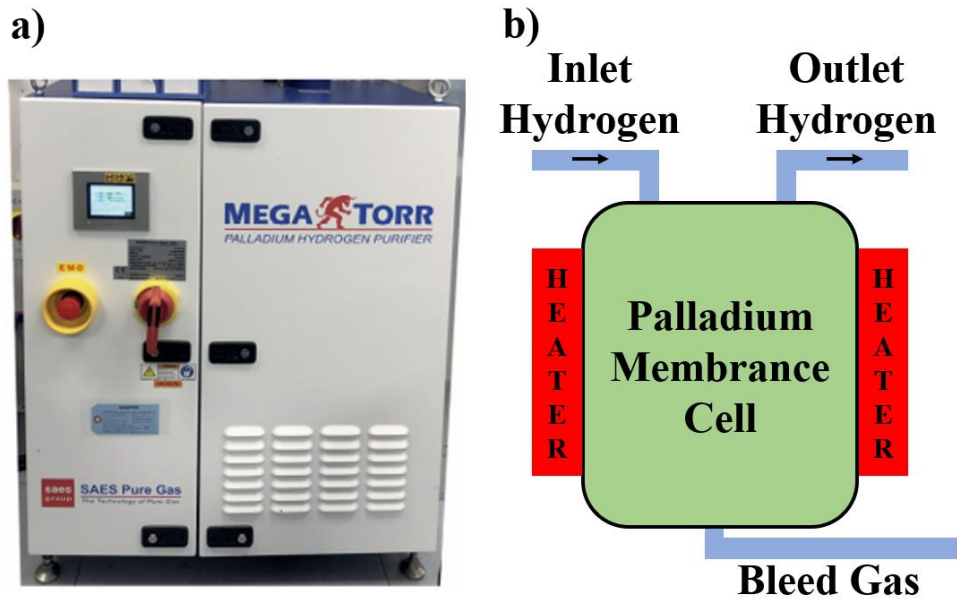


Figure 3.4 The (a) photo and (b) schematic of the hydrogen purifier.

### Gas delivery system

The gas delivery system includes the manual valves that are used to separate the MOCVD system and the purifiers. With the exception of these general inlet valves, most of the valves used in the gas delivery system are pneumatic valves that are driven by compressed air or pressurised  $N_2$ . These pneumatic valves are used to easily switch between the  $H_2$  and  $N_2$  carrier gases. Mass flow controllers (MFCs) are used to precisely control the mole flow rate of these gases.

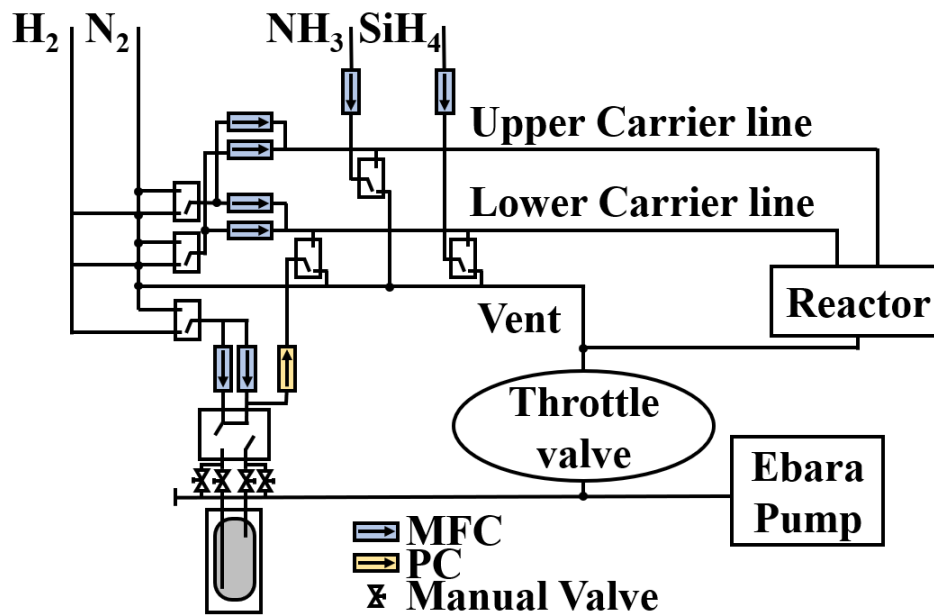


Figure 3.5 Schematic of the gas delivery system.

Figure 3.5 shows that, typically, two separate channels are used to supply the precursors to a growth chamber via a showerhead. This is because the group V precursor ( $\text{NH}_3$ ) and the group III precursors (e.g., TMGa, TMAI, TMIIn, etc.) must be supplied to the growth chamber separately. The upper carrier line is used to inject hydride gas, i.e., it carries the  $\text{NH}_3$  in a GaN MOCVD system, while the lower carrier line is used to carry group III precursors. The n-type and p-type doping sources ( $\text{Si}_2\text{H}_6$  and  $\text{Cp}_2\text{Mg}$ , respectively) are also injected through this channel.

The main pump connects the growth chamber and an exhaust system and is used to control the pressure in the growth chamber using a throat valve that is installed between the growth chamber and the main pump. The reactor pressure can then be directly controlled using the throat valve.

### 3.1.4 MO Source System

An MO source system, which supplies the precursors of the group V elements, is a key part of an MOCVD machine. Each MO source system usually consists of three main parts: the control unit, the gas system, and the source storage unit.

The source storage unit is more commonly known as a bubbler. Each bubbler is made of stainless steel and stores a specific MO source, which can be in the form of either a liquid or a solid. Each bubbler is mounted on a thermostatically controlled bath to maintain a

specific temperature that, in turn, determines the mole flow rate of the MO source. The water temperature of each bath must be constantly monitored. The bath temperature required for each MO source is different, depending on the equipment type and local environment. In this thesis, the TMG source stays at 0°C, the TMA stays at 18 or 21°C, and the TMA and the Cp<sub>2</sub>Mg stays at 30°C.

There are two main control units: valves and MFCs. The most important valve is the so-called 4/2-way valve, which allows the carrier gases to either flow through (when ‘Open’) or bypass (when ‘Closed’) a bubbler. Typically, four manual valves are used for maintenance purposes, such as to change bubblers. Three of these pneumatic valves are used to switch between the N<sub>2</sub> and H<sub>2</sub> carrier gases, while the last pneumatic valve is used to funnel the carrier gas between the reactor and the vent line.

Two primary gas systems are used to supply the gases with or without the standard gas, which is provided via an extra dilution line that is typically used for small flow rates. The left gas system in Figure 3.6 shows a standard gas system without the dilute line. It includes two input MFCs that control the carrier gases. It also includes a pressure controller that allows for control over the pressure in the bubbler, which also determines the flow rate of specific MO sources. The second double dilution gas system, which includes the additional dilute gas line, has an extra output MFC that allows for the precise tuning of small gas flow rates. With the extra output MFC, the actual injected gas flow ( $f$ ) can be further reduced and the actual amount of gas injected can be calculated using Equation (3.2), where  $f_{source}$  is the flowrate controlled by the bubbler input MFC,  $f_{dilute}$  represents the flowrate from the other input carrier gas line, and  $f_{inject}$  indicates the final flowrate of the mixture injected into the reactor, which is controlled by the MFC that controls the flow into either the reactor or vent line.

$$f = \frac{f_{source}}{f_{source} + f_{dilute}} \times f_{inject} \quad (3.2)$$

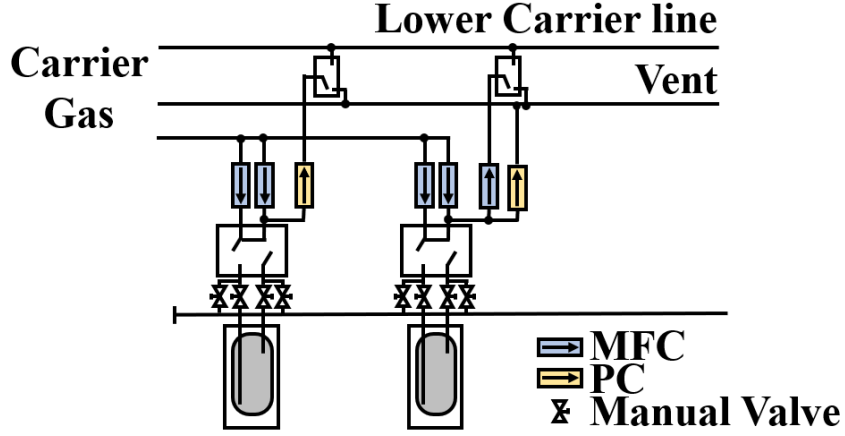


Figure 3.6 MO sources system schematics.

A mole flow rate has units of mol/min, and it controls the epitaxial growth rate as described by Equation (3.3)

$$n(MO) = \frac{f_{source} \times P_{partial}}{V_m \times (P_{source} - P_{partial})} \quad (3.3)$$

where  $f_{source}$  is the gas flow rate into the bubbler and can be controlled by a bubbler input MFC,  $P_{source}$  represents the partial pressure in the bubbler, which can be controlled by a pressure controller,  $V_m$  refers to the molar volume of the gas at 1 atmosphere and 0°C, which is 22,414 cm<sup>3</sup>/mole.  $P_{partial}$  is the partial pressure of the vapourised group III precursor in each bubbler (e.g., TMG, TMA, or TMI), which can be calculated using the following equation:

$$\log(P_{partial}) = B - \frac{A}{T} \quad (3.4)$$

where  $A$  and  $B$  are constants that are related to the nature of the MO source, and  $T$  is the temperature of the MO source in Kelvin, which is controlled and maintained by a thermal bath.

It should be noted that a different equation is required to calculate the partial pressure of Cp<sub>2</sub>Mg, which is different from the other trimethyl precursors:

$$\log(P_{partial}) = B - \frac{A}{T} - 2.18 \ln T \quad (3.5)$$

Table 3-2 shows the values of  $A$  and  $B$  for different MO sources.

Table 3-2 MO bubbler parameters [6]-[9].

Source	Chemical Formula	A	B	Bubbler Temperature (K)	Bubbler Pressure (torr)
TMG	$Ga(CH_3)_3$	1703	8.07	273	1300
TMA	$Al(CH_3)_3$	2134	8.22	291	1500
TMI	$In(CH_3)_3$	3014	10.52	303	1000
$Cp_2Mg$	$Mg(C_2H_5)_2$	4198	25.14	303	900

TMG and TMA, which were used in this project, are liquids at room temperature, while TMI and  $Cp_2Mg$  are solid sources. The gas lines between the bubbler outlet and the reactor are wrapped with heating tape to prevent the condensation of MO sources on the inner walls of the gas lines.

### 3.1.5 Close-Coupled Showerhead Reactor

Figure 3.7 presents a schematic illustration of a close-coupled showerhead system, and highlights the main components of the system, including a showerhead, double O-ring, susceptor (and its support), heater, thermocouple, quartz liner, and an exhaust port. The distance between the showerhead and a susceptor should be small enough to minimise any parasitic reactions. The typical distance between the bottom of the showerhead and the top surface of the susceptor is around 9–25mm (a distance of 11mm was used in both of the systems used in this thesis).



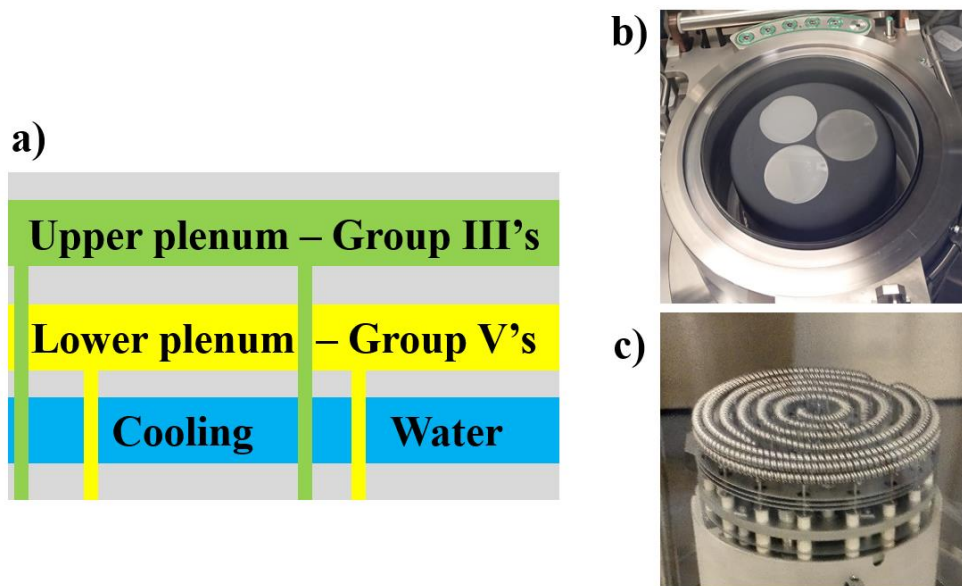


Figure 3.7 Close coupled showerhead reactor. (a) Schematic of the entire system. (b) Susceptor unit. (c) Heater.

The showerhead and the double O-ring are directly connected to the gas line system. The separated group V and group III gases are not mixed until they pass through the showerhead outlet due to the two-plenum design described in Figure 3.7(a). The water coolant used in the showerhead is controlled by an exclusive chiller that maintains a stable flow rate and a constant temperature. The double O-ring is used to seal the reactor as there is a gas line port that is connected to the main pump which can be used to pump down the pressure between the two O-rings to as low as 0 mbar.

A heater, a susceptor, and a thermocouple are included in the system. Figure 3.7(c) shows that the heater consists of three tungsten coils: the inner zone, A, the middle zone, B, and the outer zone, C. Each of these coils has its own power supply. By tuning the power output of the three coils, a uniform temperature distribution across zones A, B and C can be achieved. A thermocouple located beneath the susceptor is used to measure temperature data that is then fed to the temperature control circuit in the heater.

Beneath the susceptor is a quartz support that is used to rotate the susceptor at a speed of approximately 60 rad/s, which ensures a stable and uniform temperature across the surface of the susceptor's three 2-inch pockets.

The exhaust port is located at the very bottom of the reactor chamber. Any exhaust gases can be pumped through a flexible stainless-steel pipe that contains both a mesh filter and a

pall filter. These filters aim to remove any particulates that remain in the exhaust gases coming from the main pump.

### **3.1.6 In-situ Monitoring**

The in-situ monitoring system used in this project allows any research to monitor the growth of the crystals, including their surface morphology, wafer bowing, wafer curvature, and growth rate. The in-situ monitoring system includes an ARGUS system, an interferometer system, and a Laytec Epicurve TT system.

#### **ARGUS**

The ARGUS system dual-wavelength multiple-point pyrometric profiling system (for Aixtron MOCVD) and the Laytec Epicurve TT system (for Thomas Swan MOCVD) are used to separately monitor the temperature profile across the susceptor. This measurement uses the principles of black body radiation. A matrix of detectors located at the top of the showerhead measures the radiation from the susceptor surface that passes through the showerhead holes. The number of detectors in this matrix depends on the size of the reactor — in the 3 × 2-inch reactor used in this project, six detectors are distributed along the radius of the showerhead from the centre to its edges. As the susceptor rotates during the growing process, the detector matrix collects temperature data that is used to construct temperature profiles over time, radius, and angle through an appropriate analysis software.

#### **Interferometer**

An interferometer, also known as a reflectometer, is another necessary piece of equipment for in-situ measurement that is normally used to monitor layer thickness and surface morphology. By directing a laser onto the surface of a sample and collecting the reflected light, a reflection intensity curve that changes periodically over time can be obtained. The film thickness ( $d$ ) over one period can be calculated by the equation provided belowbelowbelow:

$$d = \frac{\lambda}{2n} \quad (3.6)$$

where  $\lambda$  is the wavelength of the laser and  $n$  is the refractive index of the grown material. Typically, a red laser with a wavelength of 635 nm is used. In this case, the thickness ( $d$ ) of one oscillation is approximately 133 nm for GaN and 144 nm for AlN.

The intensity of the reflected signal may also give an indication of surface roughness. For example, if the reflectivity intensity variation between the peaks and troughs across oscillations shrinks as time passes, this often means that the surface of the sample is becoming increasingly rough.

## Epicurve

Wafer bowing is another common issue during the growth of films on substrates with large lattice mismatches. In addition to the lattice mismatch, the differences in the thermal expansion coefficient between the crystals being grown and the substrate can also result in wafer bowing. Even within the same material, non-uniform temperature distributions along the thickness of a substrate in the vertical direction or across the substrate could lead to differential thermal expansion that leads to wafer bowing. Wafer bowing could, in turn, result in non-uniform temperature distributions, worsening the wafer bowing. This issue becomes much more severe for GaN-on-Si growth due to the large difference in thermal expansion coefficients between the two materials, especially in conjunction with their large lattice-mismatch compared to GaN-on-sapphire growth. Thus, an in-situ monitoring system capable of measuring curvature is a necessity in this field.

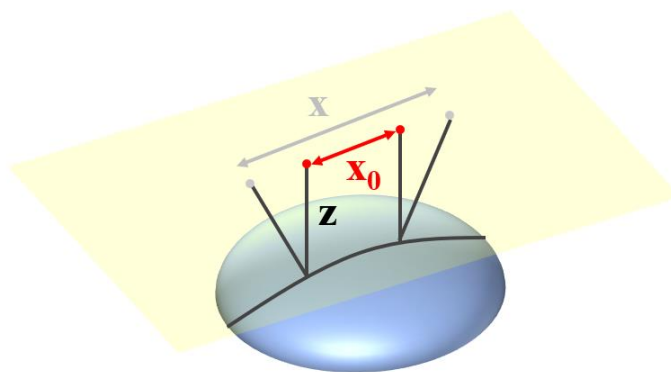


Figure 3.8 The working principle of the Epicurve.

Figure 3.8 demonstrates the use of two parallel 635 nm laser beams that are emitted from a curved optical head that is then directed onto the measured wafer through a viewport in the

showerhead. The reflected laser beams are then collected by a detector. In the case of wafer bowing, while the two incident laser beams are always in parallel, the two reflected laser beams may not be in parallel any longer; i.e., the separation of two reflected laser beams is not equal to the separation of the two incident laser beams. This difference in separation is dependent on the wafer curvature. In other words, a larger difference indicates a greater degree of wafer bowing. This can be determined quantitatively by the equation below:

$$\kappa = -\frac{1}{2Z} \frac{x - x_0}{x_0} \quad (3.7)$$

where  $Z$  is the height between the sample surface and the measurement plane,  $x_0$  is the distance between the two incident beams, and  $x$  is the distance between the two reflected beams. A positive value of  $\kappa$  indicates concave bowing, while negative values are indicative of convex bowing.

## 3.2 Characterisation Techniques

### 3.2.1 X-ray diffraction (XRD)

X-ray diffraction (XRD) is one of the most powerful material characterisation techniques and has been widely used to investigate the crystal quality, alloy composition, lattice parameters, layer thicknesses and the strain state of a structure.

Figure 3.9 presents a schematic illustration for Bragg's reflection law, which forms the physical foundation of XRD measurements. Similar to the interaction between light and a grating, constructive interference caused by the X-ray beam scattered by different atomic planes can be generated using a specific incident angle that meets Bragg's reflection law [10]. The incident angles can be determined using the equation below:

$$2d \sin \theta = n\lambda \quad (3.8)$$

where  $\lambda$  is the X-ray wavelength,  $n$  is the order of diffraction,  $d$  is the distance between 2 adjacent atomic planes of the measured sample, and  $\theta$  is the incident angle. This technique can be used to calculate the lattice constants of the measured sample from the incident angles.

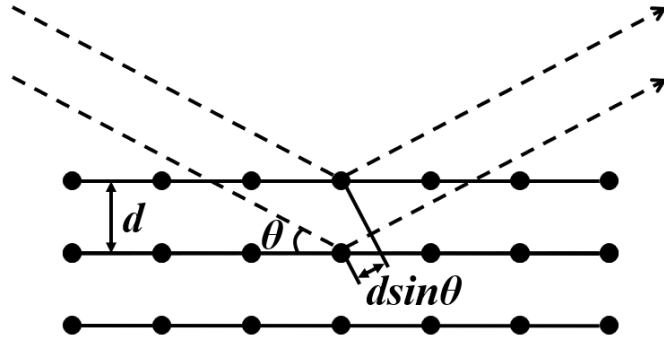


Figure 3.9 Schematic of X-ray diffraction and Bragg's law.

XRD was used to determine that all samples used in this work were III-nitrides with a hexagonal crystal structure. The theoretical interspacing of the measured atomic planes ( $h$ ,  $k$ ,  $l$ ) can be determined by their lattice constants  $a$  and  $c$  via the equation below.

$$\frac{1}{d_{hkl}^2} = \frac{4}{3} \cdot \frac{h^2 + k^2 + hk}{a^2} + \frac{l^2}{c^2} \quad (3.9)$$

#### Bruker X-ray diffractometer system

A Bruker D8 X-ray diffractometer system was used in this project. The system consists of an X-ray tube, primary optics, a sample stage, secondary optics, and a detector. The X-ray beams are generated in the X-ray tube at high voltages by bombarding a copper anode with electrons, which generates a Cu  $K\alpha$  X-ray with a wavelength of 1.5418 Å. The primary optics unit is used to collimate the generated X-rays, ensuring that the incident X-ray beams are symmetrical and easily focused. The incident X-ray beams are then emitted onto a sample that is held on the sample stage, which can be rotated in the Phi( $\varphi$ ), Psi( $\psi$ ) and Omega( $\omega$ ) directions as shown in Figure 3.10, allowing for measurements in different scattering modes. The X-ray beams that are scattered or reflected off the sample are collected by a secondary optics unit and recorded using a detector.

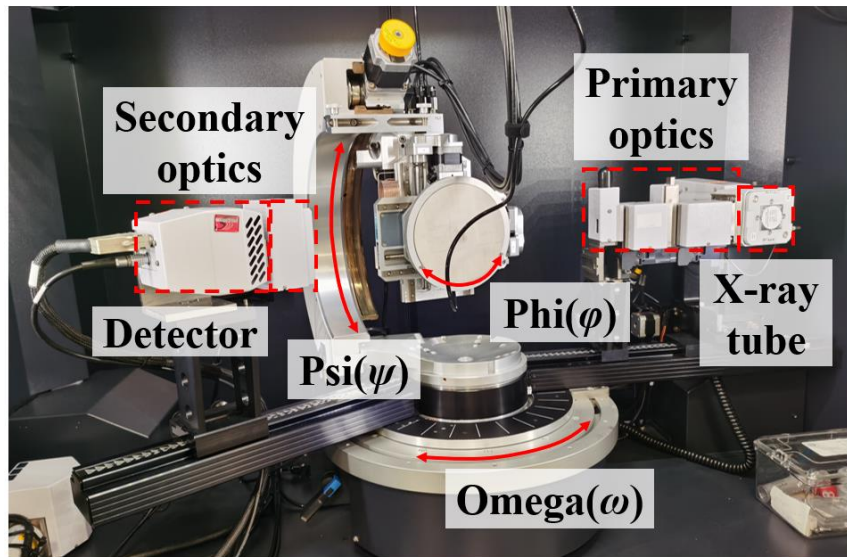


Figure 3.10 Schematic of the Bruker D8 X-ray diffractometer.

### Measurements in Different Scanning Modes

To understand the diffraction geometry of different XRD scan modes, we introduce an Ewald sphere constructed in reciprocal space, in which each crystal plane and their corresponding diffraction spots can be represented by reciprocal lattice points in a single figure [10]-[12].

Figure 3.11 shows an illustration of the Ewald sphere of c-plane GaN, where  $k_0$  and  $k_h$  represent an incident and a diffracted beam vector, respectively, and their length is  $1/\lambda$ . The scattering vector (labelled  $S$ ) represents  $k_0 - k_h$ , which points in the direction of the measured reciprocal lattice point. For example, in Figure 3.11, (0004) represents the measured plane, and the scattering vector points towards the point of this plane in reciprocal space, i.e., (0004).

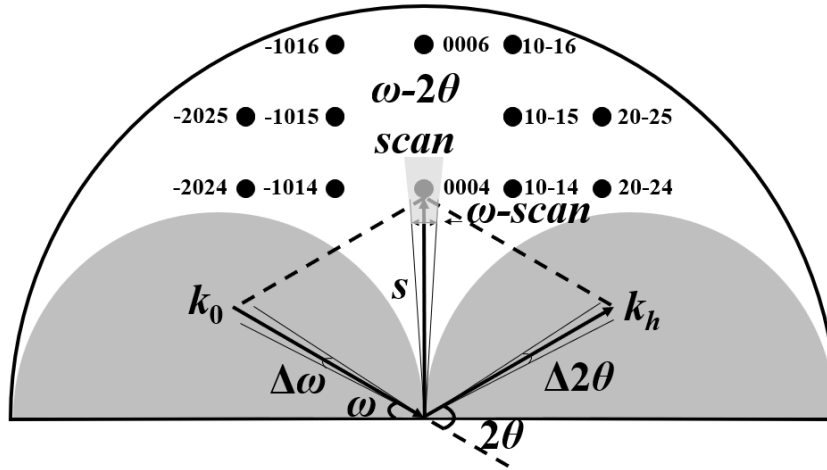


Figure 3.11 Example of the X-ray diffraction of a c-plane GaN film and its accessible areas in reciprocal space as described using an Ewald sphere.

Figure 3.11 also represents the reciprocal space where the incident or diffracted beam is sheltered by the sample itself in an asymmetric scan, indicated by the two grey semi-circular areas. Not all possible diffraction points are presented in the figure, but points that fall within the grey semicircles are inaccessible. However, by changing the measurement geometry, it is possible to access the sheltered area. Specifically, Figure 3.12 shows that, for symmetric geometries, where  $2\theta = 2\omega$  and no additional rotation or offset is needed, the crystal planes that are parallel to the surface of the sample can be measured. For crystal planes that are tilted by an angle  $\alpha$  relative to the sample surface (i.e., an asymmetric geometry), in which  $2\theta \neq 2\omega$ , an asymmetric scan is needed. To access the inaccessible area in the Ewald sphere, a skew-symmetric geometry is required, which involves rotating a sample by  $90^\circ$  in the  $\Phi$  direction and subsequently tilting the crystal plane by an angle  $\alpha$  such that the scan becomes a tilted version of a symmetric geometry (meaning that  $2\theta = 2\omega$  in the skew-symmetric geometry). Finally, in the most extreme cases, in which the incident or scattering angle is small, a grazing incidence diffraction (or in-plane scattering) geometry can be used.

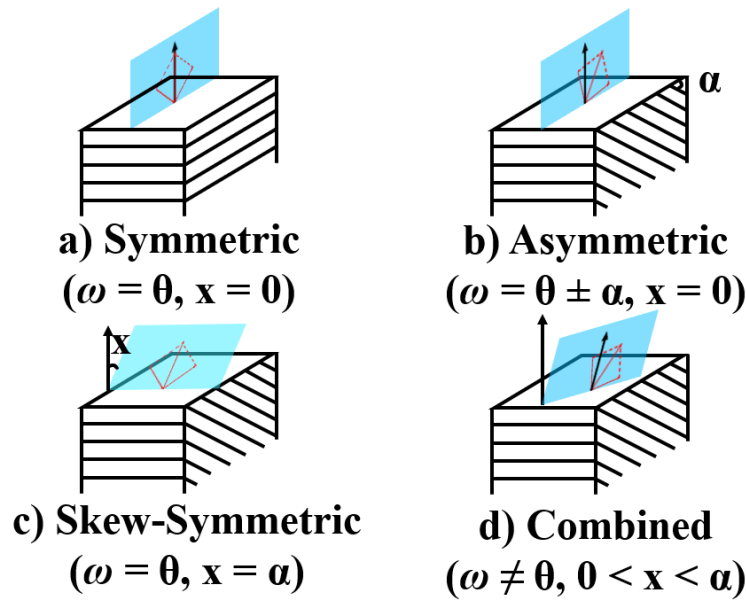


Figure 3.12 Schematic illustration of the diffraction geometries.

Based on these diffraction geometries, three types of scanning modes are used for measurements:  $\omega$ -scan,  $\omega$ - $2\theta$  scan, and  $2\theta$  scan. A  $\omega$ -scan measurement can be performed by keeping the source and detector fixed and rotating the sample around an axis. In other words, in the reciprocal space of the  $\omega$ -scan, the direction of the scattering vector  $S$  changes at a constant rate. Therefore, the  $\omega$ -scan measurement is often referred to as an X-ray rocking curve (XRC) measurement. A  $\omega$ -scan measurement is normally used to determine the dislocations, the surface mosaicity, and the wafer curvature of a sample. A  $\omega$ - $2\theta$  scan measurement can be conducted by ensuring that  $\Delta 2\theta$  remains equal to  $2\Delta\omega$  and causing the length of scattering vector  $S$  to change in a constant direction. This measurement allows for the identification of the orientations of crystal planes. Finally, in a  $2\theta$  scanning mode, the detector holds a fixed incident beam angle and makes an arc across the circumference of the Ewald sphere. This scan is useful to address diffraction spots as needed.

Reciprocal space mapping (RSM) measurements have been widely used in the study of strain distribution. RSM refers to a combination of a series of  $\omega$ - $2\theta$  scans with a continuously changing  $\omega$ -offset, meaning that the results of an RSM measurement can be used to project a 3D map of diffraction intensity onto a 2D region in reciprocal space. This makes RSM a powerful tool for studying the strain distribution within a crystal.



### 3.2.2 Nomarski Microscopy

Optical microscopy systems have been widely used in semiconductor industries and laboratories and are one of the most powerful tools for the quick examination of the surface morphology of a semiconductor. Nomarski microscopy, also known as differential interference contrast (DIC) microscopy, is an advanced optical microscopy system that was used in this work. In addition to the features available in standard microscopy systems, the DIC system uses optical interferometry effects to improve the quality of an optical image, especially for transparent materials such as GaN. Furthermore, the optical interferometry effects also allow for the extraction of additional information, such as differences in thickness and variables in the refraction index [13],[14]. Figure 3.13 describes the mechanisms behind this imaging system.

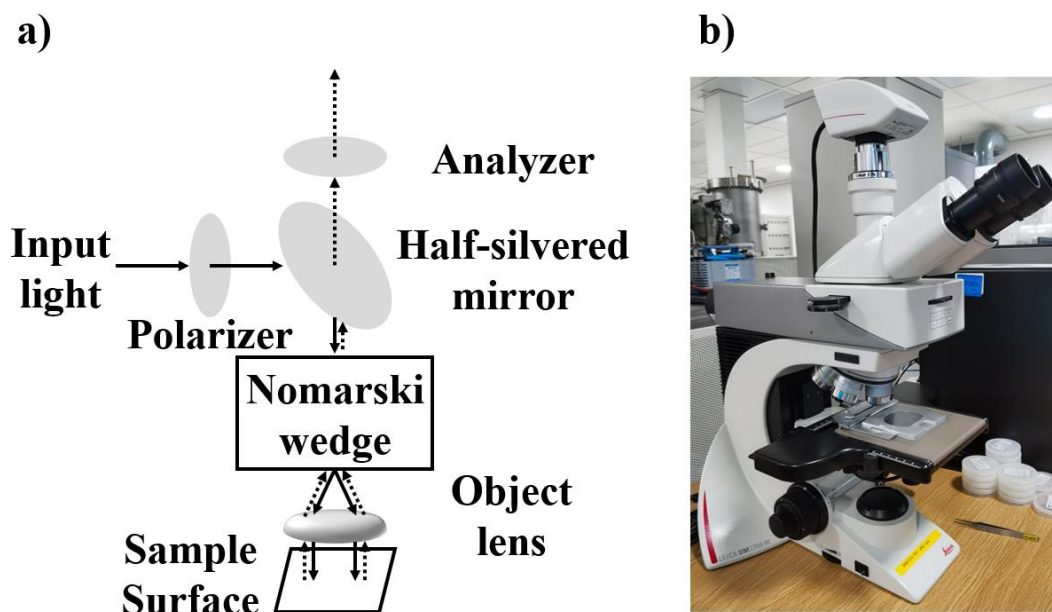


Figure 3.13 (a) A schematic illustration of a Nomarski microscope. (b) A photo of the Nomarski microscope used in this work.

Unpolarised light is first introduced into the system before being linearly polarised at  $45^\circ$ . After being reflected by a semi-transparent mirror onto a Wollaston prism, the polarised light is separated into two beams, which are then separately focused and projected onto a sample surface using a condenser. These two beams are identical except for their polarisation, and they take slightly different optical pathways due to the sample thickness and/or variations in the refractive index. These beams are then reflected into the Wollaston prism and recombined into a single ray of light with a linear polarisation of  $135^\circ$  at the analyser. The interference produced by the two beams can be visualised in the output image.

### 3.2.3 Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) is a high-resolution scanning probe microscopy technique that is often used to characterise the surface roughness of a material. Figure 3.14 presents a very basic illustration of the AFM mechanism, in which a cantilever is used to manipulate a nanoscale tip while being illuminated by a laser beam. During the scanning process, the nanoscale tip probes the point on the sample surface that corresponds to an individual pixel in the scanning region. Information about surface morphology is recorded for each pixel.

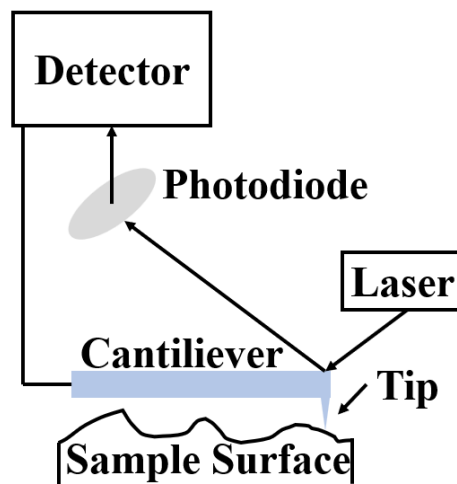


Figure 3.14 The schematic of the AFM.

Two operational modes are typically used. In the “contact mode”, a tip must touch the surface of a sample, which deforms the tip based on the roughness of the surface. The reflected laser experiences a phase change due to the deformation of the tip, which can be used to evaluate the surface morphology of the sample in the area being scanned. The deformation of the tip is driven by the atomic repulsive force between the tip and the sample atoms and is the basis for this operational mode. Although this operational mode allows for high resolutions, the atomic repulsive force typically falls within the range of  $10^{-6}$  to  $10^{-9}$  N, which could potentially damage some samples. The second mode is known as the “tapping mode”. In this mode, the tip is made to vibrate vertically at its resonance frequency. The Van der Waals interactions between the tip and the sample surface determine the amplitude of the tip oscillation during the scanning process, with the amplitude decreasing as the tip approaches the sample surface. The AFM image is thus obtained by measuring the force of the interactions between the tip and the sample.

### 3.2.4 Scanning Electron Microscopy (SEM)

Scanning electron microscopy (SEM) is generally used to examine the surface morphology or access cross-sectional information about a sample (including its microstructural information) at the sub-micrometre/nanometre scale. An SEM system uses an electron beam as the illumination source rather than visible light, resulting in far greater resolutions compared to optical microscopy systems.

Figure 3.15 presents a schematic illustration of the basic structure of an SEM system, which is primarily composed of an electron source, a series of magnetic condensers, a set of deflection coils, and a sample holder. Notable, an SEM system operates in a vacuum held at  $<5.5 \times 10^{-5}$  mBar. An electron beam is generated by a field emission gun and focused using a magnetic condenser lens. These ‘primary electrons’ are then shone onto the sample. The interactions of the primary electrons with the sample results in the formation of a suite of signals that contain information about the surface morphology and structure of the sample, which are collected using detectors.

The signals generated due to the interaction between the primary electrons and the sample can be classified into four broad categories: backscattered electrons (BSE), Secondary electrons (SE), X-ray emissions, and light emissions. Backscattered electrons are electrons that have been scattered by the sample due to elastic scattering. As they have a significant amount of energy and travel quickly in a straight line, the BSE detector is situated immediately above the sample. Due to the sensitivity of BSE to the atomic number of the sample, BSEs are commonly used to determine the chemical composition of a material. SEs are defined as electrons that are created as a result of primary electron radiation. Hence, SEs are very beneficial for deciphering information about the morphology and topography of the surface. Because SEs have low energy and thus move slowly, they are often captured using a positively charged SE detector. Primary electrons can also create electrons from the inner shell of atoms – the unoccupied states are quickly filled by electrons from the higher energy outer shell, generating X-ray emissions. Since each element has a distinct electron configuration that corresponds to a unique signature emission spectrum, energy-dispersive X-ray (EDX) analysis can be used to determine the elemental composition of a sample. Finally, light emissions are often referred to as cathodoluminescence (CL), which are extremely valuable for studying the optical characteristics of the sample at a nanometre scale. CL has much higher spatial resolutions compared to photoluminescence (PL).

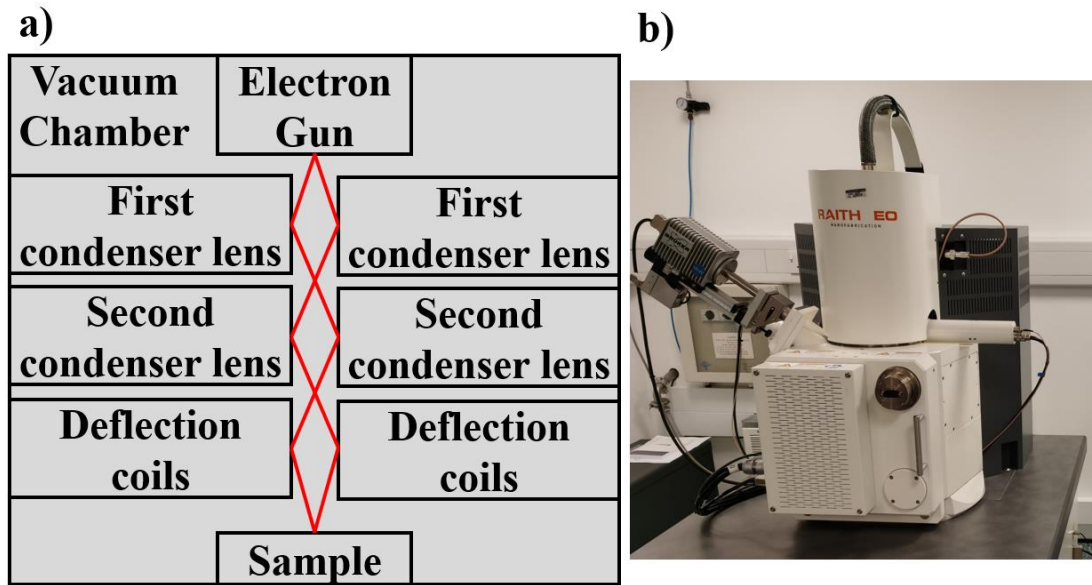


Figure 3.15 (a) Schematic structure of an SEM system and (b) the photo of the used SEM.

### 3.2.5 Photoluminescence (PL)

PL refers to the light emitted by a material after being optically excited. PL spectroscopy is a non-destructive, non-contact analytical method that is widely used to analyse the optical properties of materials. It is useful in investigating the optical performance of direct bandgap semiconductors [15].

The bandgap energy of a semiconductor as well as the compositions of its alloys can be investigated by PL. Other factors such as its strain, electric field, and compositional variation can also be studied. The crystal quality of a semiconductor can be estimated by evaluating the intensity and spectral linewidth of the PL, which is normally defined as the full width at half maximum (FWHM) [16].

A schematic illustration of the PL system used in this study is presented in Figure 3.16. For samples with high AlGa<sub>N</sub> contents, a doubled-frequency Argon ion laser (244 nm, Coherent) was employed as an excitation source, while GaN samples were excited by a He-Cd laser (325 nm, Kimmon). The beam was reflected using mirrors and then focussed using a lens onto a spot with a diameter of 200  $\mu\text{m}$  on the surface of the sample. The emissions are collected by a monochromator, and the PL was detected using a thermoelectrically cooled CCD detector.

Samples can be held in a helium-filled closed-circuit cryostat with a temperature range of 10–300K under vacuum to perform low-temperature measurements or temperature-dependent PL measurements. Neutral density attenuators are used to allow for excitation power-dependent PL measurements.

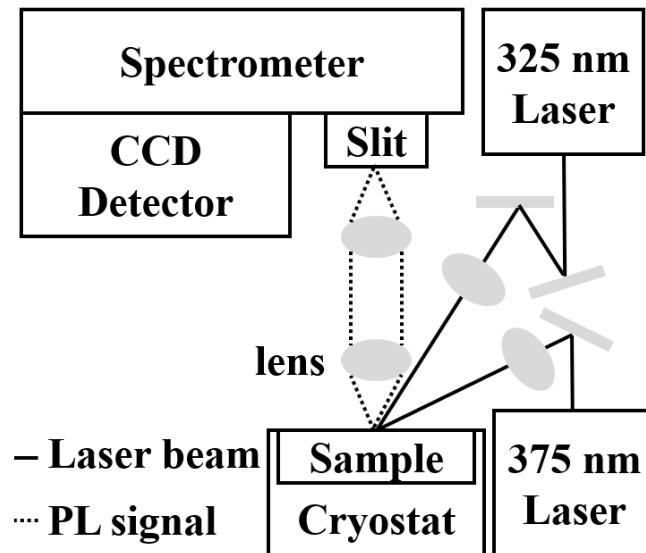


Figure 3.16 Schematic of a PL system.

### 3.3 Fabrication Techniques

#### 3.3.1 Sample Treatment

##### Basic Cleaning

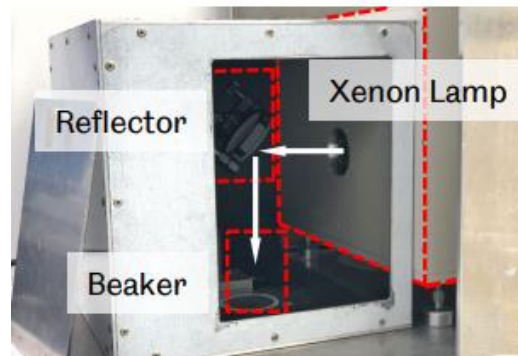
The surface treatment/cleaning of a template is essential for MOCVD overgrown growth on the template, especially for patterned templates. We developed a standard operating procedure as follows:

1. Immerse the wafer in solutions of n-butyl acetate, acetone, and isopropyl alcohol in an ultrasonic bath for 5 mins each.
2. Rinse the wafer with deionized water for 5 mins to remove any residual solvent.
3. Dry the wafer using a nitrogen gun and then baking it in an oven at 100°C.

For patterned templates, an extra procedure involving the use of potassium hydroxide (KOH) and hydrochloric acid (HCl) to remove any potential contamination due to the template fabrication process must be conducted. This procedure will be described in greater detail in the relevant sections.

## Photo-Enhanced Chemical Etching (PEC)

In this work, ultraviolet (UV) photo-enhanced chemical (PEC) etching was used to treat the overgrown patterned template before overgrowth.



*Figure 3.17 The custom-built PEC etching system used in this work.*

The custom-built PEC etching system used in this work is shown in Figure 3.17. A 1.5 W/cm<sup>2</sup> Xenon arc lamp rated at 450 watts was used to generate the UV light required. To properly etch the sample, the sample was immersed in an electrolytic solution containing 10% potassium hydroxide (KOH) and illuminated using an aluminium-coated UV reflector.

The mechanism behind PEC etching involves the generation of electron-hole pairs in GaN due to the UV photons from the Xenon lamp used to illuminate the sample, which is consumed during the dissolution of the semiconductor and the reduction of the oxidizing agent (KOH) in the electrolyte.

### 3.3.2 Thin-film Deposition

#### Plasma Enhanced Chemical Vapour Deposition (PECVD)

PECVD is a standard technique for depositing a dielectric film onto a substrate. In this work, PECVD was used to deposit silicon dioxide (SiO<sub>2</sub>) onto either a GaN template or a standard Si or sapphire substrate to fabricate a patterned template or substrate. Figure 3.18 presents a photograph of the PECVD system used in this study (Plasma-Therm model 790). Typically, SiH<sub>4</sub>, N<sub>2</sub>O, and N<sub>2</sub> are the standard gases used for the deposition of SiO<sub>2</sub> on the substrate at temperatures of 300°C.



Figure 3.18 A photo of the Plasma-Therm 790 series instrument used for PECVD.

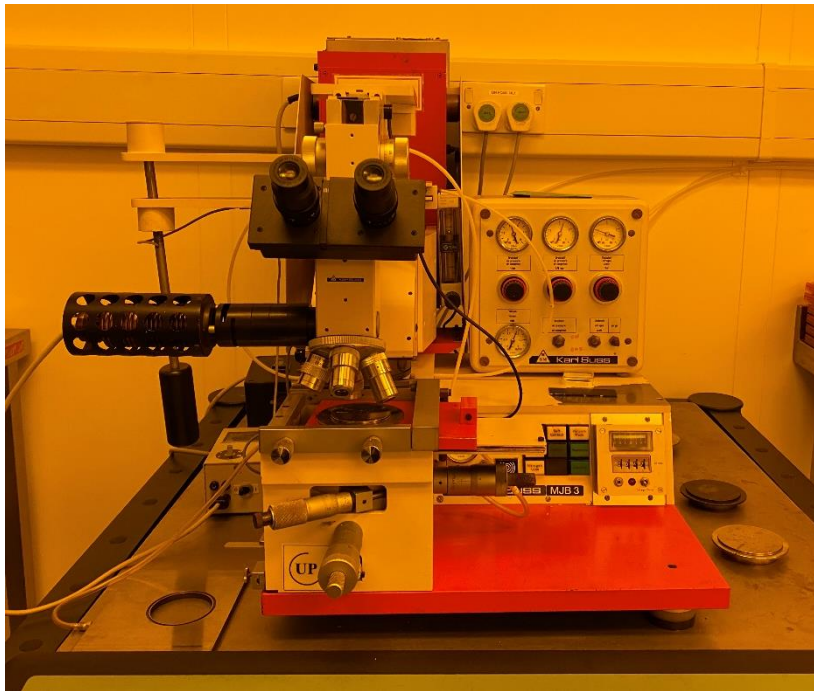
### 3.3.3 Photolithography



Figure 3.19 Spinner for photoresist deposition.

Photolithography refers to a common device fabrication or template patterning technique used to transfer a pattern from a mask to a substrate or a semiconductor wafer. The spinner is first used to deposit a photoresist layer. Figure 3.19 presents a photograph of the spinner used in this work. To obtain an even and uniform coating of photoresist, the wafer is spin-coated at a rotation speed exceeding 4000 rev/min lasting for around 30 seconds. This is followed by baking on a hot plate for 60 seconds at 100°C.

The next stage of the photolithography process involves the use of a mask as an aligner to transfer the pattern to the photoresist. In this work, both a Karl Suss MJB3 UV400 system with a wavelength of 350–450nm and a UV300 system with a wavelength of 250–350nm were employed for this task. The only difference between the two aligners is the wavelength of their UV light. The photograph of the UV400 mask aligner system is shown in Figure 3.20.



*Figure 3.20 Karl Suss MJB3 UV400 mask aligner.*

### **3.3.4 Dry Etching**

#### **Reactive-Ion Etching (RIE)**

Dry etching is a typical technique that is widely used in the semiconductor industry. In this work, a Plasma-Therm Shuttlelock series RIE system was used to fabricate dielectric mask-based patterned templates (Figure 3.21). Specifically, RIE was used to etch  $\text{SiN}_x$  or  $\text{SiO}_2$  to produce dielectric masks for further selective overgrowth.

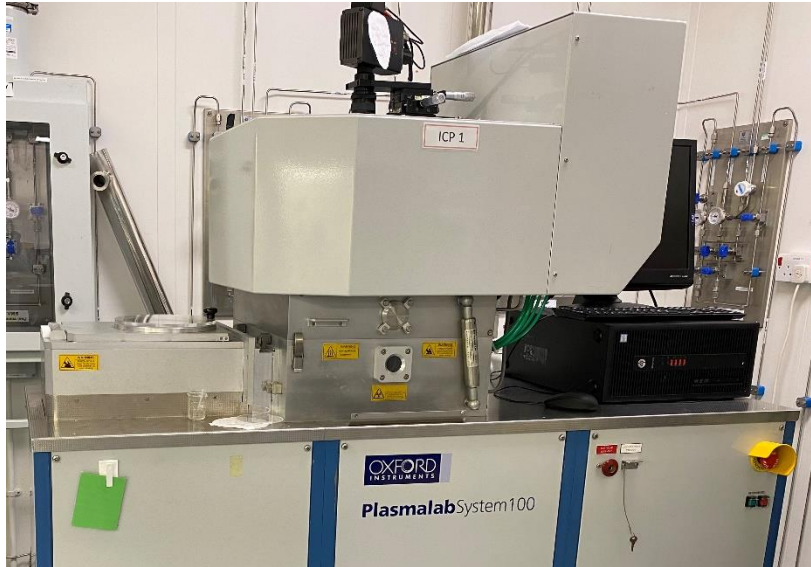




*Figure 3.21 Plasma-Therm Shuttlelock Series RIE.*

### **Inductively Coupled Plasma (ICP)**

ICP-RIE is one of the most powerful tools for dry-etching and is widely used in the semiconductor industry. Compared with RIE, where the plasma generated by the RF is delivered between two electrodes, the plasma generated by ICP passes through a stand-alone RF coil that generates a time-varying electromagnetic field in which the reactant gases are ionised by the inductive coupling as shown in Figure 3.22. In addition, a bottom electrode driven by RF is used to attract and accelerate the reactive ions toward the sample disc in the ICP system. Each of these systems offers independent controls for plasma density and vertical ion bombardment, providing more control over the etching process.



*Figure 3.22 Schematic illustration of ICP and the Plasmalab System 100 (Oxford Instruments) used in this study.*

Figure 3.22 also shows a photograph of the ICP system used in this work (Plasmalab System 100, Oxford Instruments). The etch depth and rate are monitored using an interferometry endpoint system. The working principle of this monitoring system is similar to that of the in-situ interferometry system used in MOCVD. A laser beam is incident on a sample surface and its reflected signals are collected. When a sample is etched, the reflected light exhibits periodic curves with increasing etching depth, such that etched depth can be determined by the period of the reflectance, refractive index, and the wavelength of the laser used. The etch rate can subsequently be calculated by dividing the depth by the etching time.

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# Chapter 4 Growth of GaN on (111) Silicon

## Substrates

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This chapter investigates the growth mechanism and the detailed growth procedures for gallium nitride (GaN) growth on silicon substrates, including Si substrate treatment, vertical wafer temperature uniformity, aluminium nitride (AlN) layer development, aluminium gallium nitride (AlGaN) layer growth, and gallium nitride (GaN) layer growth. All optimised circumstances for the aforementioned elements are summarised at the conclusion of each section. Their surface, in-situ curvature, and crystal quality are characterised using optical microscopy, scanning electron microscopy (SEM), the Laytec Epicurve, and the Bruker X-ray diffractometer (XRD), respectively. As a result, GaN on Si grown under the optimised conditions is prepared for the subsequent growth of device structures.

### 4.1 Introduction

It is preferable to use a homoepitaxial growth technique to obtain high-quality III-V compounds, whereas large lattice heteroepitaxy may result in lattice-mismatch induced strain, the most fundamental issue that can significantly alter a growth mode and thus the optical properties of III-V semiconductors. Heteroepitaxy has been extensively utilised to develop III-V compound semiconductors, resulting in significant success in the manufacture of high-performance III-V semiconductor optoelectronics in recent decades, most notably GaAs and InP based optoelectronics for telecom applications.[1]-[8] However, because of the lack of inexpensive native substrates, research on III-nitride semiconductors is mostly focused on lattice-mismatched heteroepitaxy. The two major substrates for heteroepitaxial development of III-nitride semiconductors are sapphire and silicon. The enormous lattice mismatch between sapphire or silicon and GaN leads to a great challenge in obtaining GaN with reasonably crystal quality which can meet the requirements of devices. A compressive strain occurs in GaN on sapphire owing to the substantial lattice mismatch of 16%, while tensile strain occurs in GaN on silicon due to the greater thermal expansion coefficient of GaN compared to Si (54%), as well as the large lattice mismatch between GaN and silicon (17%).[9]-[14] It is broadly accepted that a high growth

temperature of more than 1000 °C is essential for the growth of GaN on silicon or sapphire. Such a high growth temperature complicates the growth of GaN on silicon since the considerable thermal expansion coefficient between GaN and Si causes tensile strain and hence severe cracking problems in GaN on silicon.[9]-[14] Additionally, because of the well-known melt-back effect (i.e., gallium may chemically react with silicon at elevated temperatures),[11]-[14] the standard two-step growth process used to generate GaN on sapphire cannot be used to grow GaN on silicon. As a result, a separate technique is required for growing GaN on silicon, where it is necessary to prepare an initial AlN buffer and subsequently a strain engineering layer, further complicating the strain status of GaN on silicon.

Until now, a number of approaches have been proposed, such as AlN/GaN superlattice layers,[16][17]  $\text{Al}_x\text{Ga}_{1-x}\text{N}$ -based interlayers,[15],[18]-[20] patterned silicon substrate [21][22] and step-graded  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  strain-release layers.[23][26] The idea is to use the compressive strain that is built due to the GaN on these Al(Ga)N layers to compensate for the tensile strain between GaN and silicon generated during the post-growth cooling down process. Among these methods, the graded  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  method is very popular due to its easiness to achieve and analyse the strains in each layer. In detail, for the graded  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  buffer layers, a large number (>4) of  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  layers [27] and different Al compositions (from 0.75 to 0.25) have been reported.[28] However, the growth procedures are quite time-consuming, leading to a high manufacturing cost.[18] On the other side, due to the complex epi-structure design, the strain-released mechanism is still not explicitly explained yet.

This chapter discusses the GaN on Si growth process on each stage, including Si substrate preparation, vertical wafer temperature uniformity, AlN layer growth, AlGaN layer growth, and GaN layer growth. For the Si substrate treatment, optical microscopy images are taken to exam surface morphology after surface treatments. For the vertical wafer temperature uniformity, the in-situ curvature curves have been measured on 330  $\mu\text{m}$  thick Sapphire, 430  $\mu\text{m}$  thick Si and 1030  $\mu\text{m}$  thick, respectively, demonstrating their vertical temperature variation in each case. For the AlN growth, XRD rocking curve measurements and SEM measurements along with in-situ interferometer measurements have been carried out to identify the optimal AlN growth conditions. For the AlGaN growth, the wafer cracks have been studied by optical microscopy and the influence of the growth conditions on the

properties of AlGaN has been investigated. For the GaN growth, the growth conditions have been optimised in terms of surface morphology and crystal quality.

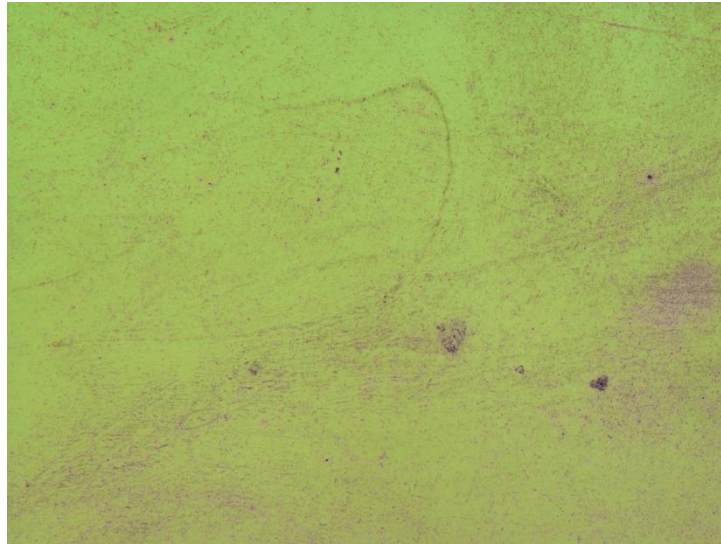
## **4.2 Experiments and Results discussion**

### **4.2.1 Silicon Substrate Treatment**

Once a silicon substrate is exposed to the air, a very thin oxidation layer will be formed on the surface of the silicon substrate. Two approaches have been used and have also been compared. The 1<sup>st</sup> one is due to chemical cleaning, which involves the utilisation of solvent cleaning, acid oxidation and final HF etching, while the other method is to use high-temperature annealing under a hydrogen ambience. Optical microscopy and SEM have been used to observe the treated (111) silicon surface.

The surface treatment of a silicon substrate has a significant influence on the growth and quality of GaN grown on silicon, as any contamination or oxide on the silicon substrate surface can lead to a significant change in growth pattern and thus have major impact of the crystal quality of GaN on silicon including defect density and surface morphology.

For example, Figure 4.1 shows the surface of an AlN sample grown on a (111) silicon substrate by MOCVD, which is a crucial step for growing GaN on a silicon substrate. Initially, prior to the growth, a silicon substrate is cleaned by using chemicals and then undergoes baking in an oven at a 100°C for 1 minute. After that, the silicon substrate is then stored in the glovebox of the MOCVD system overnight to eliminate any potential residual water and others, where the oxygen level inside the glovebox is around 10 ppm and the moisture level is lower than 0.5 ppm. Finally, the silicon substrate is loaded into the MOCVD growth chamber. Initially, the silicon substrate is annealed under 1280 °C in a hydrogen ambience for 600 seconds before any deposition. Even with so many step treatments, Figure 4.1 shows that there is a feature which looks like a watermark pattern under optical microscopy, which is often observed on the samples where the substrates undergo chemical surface treatments.



*Figure 4.1 Watermark on AlN surface after growing on chemical treated Si wafers*

The 2<sup>nd</sup> approach for surface treatment is to directly anneal it at a high temperature in a hydrogen ambience but without any chemical treatments, where hydrogen at a high temperature exhibit an etching function. In this case, this method can be applied only to epi-ready silicon substrates. Otherwise, if there are metal residuals or tiny or heavy oxides left on a silicon substrate surface, the silicon substrate is expected to suffer a very bad morphology after the high temperature annealing process. Figure 4.2 shows an extreme case, where a silicon substrate suffers a very bad surface morphology after being annealed at 1360 °C for 1 hour. It can be seen that its surface has been severely etched, featuring some large particles. In addition to that, as shown in Figure 4.2b, the evenly distributed trapezoidal pits also indicate that some reactions occurred between hydrogen and Si surface (or SiO<sub>x</sub> due to partially oxidized Si surface) under high-temperature annealing conditions.

Therefore, it is important to obtain a proper procedure for chemical cleaning treatment and optimise annealing process for the 2<sup>nd</sup> approach (e.g. temperature and duration time).



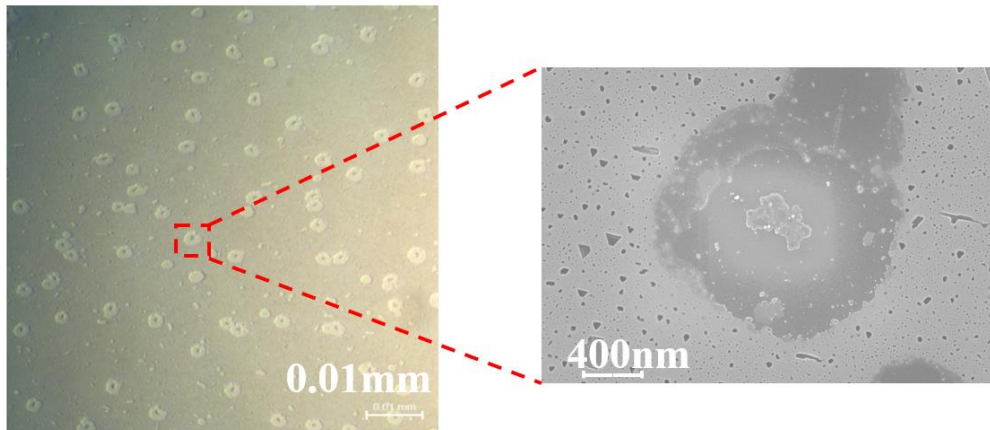


Figure 4.2 Extreme Example of a Si wafer without chemical cleaning after over-time and over-temperature annealing. Measured by a) Optical microscopy b) SEM

Below shows our typical procedure for the 1<sup>st</sup> approach for silicon substrate treatment prior to any Gan epitaxial growth on a silicon substrate:

1. Immerse a Si substrate in n-butyl acetate, then acetone, and finally isopropyl alcohol (IPA) using an ultrasonic bath each for 5 mins.
2. Rinse the Si substrate using deionized water (DI water) to remove any remaining solvent.
3. Immerse the Si substrate in a mixed solution with 98% concentrated sulfuric acid, hydrogen peroxide and DI water in a ratio of 1:1:2 for 5 mins.
4. Rinse the Si substrate using DI water to remove any residual chemicals.
5. Immerse the Si substrate in 40% Hydrofluoric acid (HF) for 5mins.
6. Rinse the Si substrate using DI water to remove any residual chemicals.
7. Blow and then dry the Si substrate using a dry nitrogen pistol and then bake it in an oven at 100 °C to remove absorbed moisture.

For comparison purpose, a set of samples consisting of 4 samples are prepared separately. Sample A and B have been treated using the above procedure chemicals before annealing and then growth while Sample C and D have not been yet. In each case, AlN growth was carried out under the same growth conditions. Additionally, the silicon substrates for Sample A and C were annealed at 1280 °C while those for Sample B and D were annealed at 1340 °C.

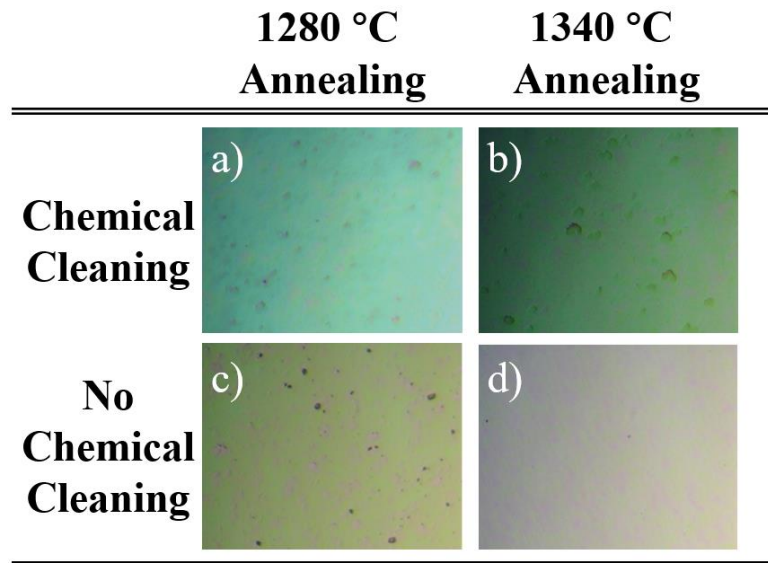


Figure 4.3 Optical Microscopy pictures of a) Sample A, b) Sample B, c) Sample C and d) Sample D

Figure 4.3. shows the optical microscopy images of Sample A, B, C and D, respectively. The silicon substrates used for the growth of Sample A and Sample C were annealed at 1280°C for 900 seconds. Among these two samples, Sample C shows dark spots whose density is higher than that of Sample A. This means that the chemical treatment is useful if the subsequent annealing temperature is low. Moreover, the images of Sample A and B as shown in Figure 4.3 indicate that a high-temperature annealing process can effectively remove any residual stains. Figure 4.3 shows that the stains left on the surface of Sample B can be easily observed, while such stains are not observed on Sample D. The stains are possibly replica due to any residuals after the chemical cleaning process. By comparing Sample A and Sample D (using Sample C as a reference), it can be concluded that the annealing temperature has a greater influence on the surface cleanness compared to the chemical treatment.

Two different approaches for silicon substrates surface treatment have been investigated and compared in this section. The direct high-temperature annealing method exhibits advantages over than the chemical cleaning method in terms of simplicity and performance. Therefore, the direct high-temperature annealing method at 1340 °C under hydrogen is chosen for silicon substrate surface treatment prior to epitaxial growth for this work. It is worth highlighting that this method also sensitively depends on the quality of silicon substrates.

#### 4.2.2 Investigation of vertical wafer temperature uniformity by in-situ curvature measurement

At a high temperature, the top surface and the bottom of a substrate generally exhibit different temperatures. This temperature variation may cause a wafer bowing, which can be observed by using an in-situ curvature detector system, Laytec Epicurve in our case. Furthermore, such a temperature variation also depends on a substrate used. This vertical temperature non-uniformity also causes a variation in the surface temperature across a substrate. In this section, a curvature measurement and temperature distribution across a 2” inch substrate have been carried out on a sapphire substrate with a thickness of 330  $\mu\text{m}$ , a Si substrate with a thickness of 430  $\mu\text{m}$  and a Si substrate with a thickness of 1030  $\mu\text{m}$ , respectively, in order to investigate the influence of the thickness of a substrate on wafer curvature and temperature distribution at a high temperature.

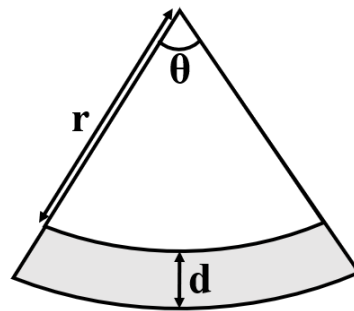


Figure 4.4 Drawing of wafer curvature

Figure 4.4 shows a schematic of wafer bowing at a high temperature, where  $d$  means the wafer thickness and  $r$  is the radius of the circle that fits the wafer surface at a measured point. The curvature value  $\kappa$  from the measurement can be determined by the equation below:

$$\kappa = \frac{1}{r} \quad (4.1)$$

The dimension of the wafer top surface and the bottom of a wafer can be expressed in an unit of arcsecond by the equations below:

$$L_{top} = \frac{\theta}{360} 2\pi r \quad (4.2)$$

$$L_{bot} = \frac{\theta}{360} 2\pi(r + d) \quad (4.3)$$

Where  $\theta$  is the angle labelled as shown in Figure 4.4. Furthermore, the bottom length can also be expressed as:

$$L_{bot} = L_{top}(1 + \alpha * \Delta T) \quad (4.4)$$

Where  $\alpha$  is the thermal expansion coefficient of the wafer and  $\Delta T$  is the temperature variation between the top and bottom of a wafer. The  $\Delta T$  can be obtained by combining equations (4.2), (4.3) and (4.4):

$$\frac{\frac{\theta}{360} 2\pi r}{\frac{\theta}{360} 2\pi(r + d)} = \frac{L_{top}}{L_{bot}} = \frac{L_{top}}{L_{top}(1 + \alpha * \Delta T)} = \frac{1}{1 + \alpha * \Delta T}$$

$$\therefore \kappa = \frac{1}{r} = \frac{\alpha * \Delta T}{d} \quad (4.5)$$

$$\Delta T = \frac{\kappa d}{\alpha} \quad (4.6)$$

Three 2" substrates as mentioned above (a sapphire substrate with a thickness of 330  $\mu\text{m}$ , a Si substrate with a thickness of 430  $\mu\text{m}$  and a Si substrate with a thickness of 1030  $\mu\text{m}$ ) have been used to investigate the wafer curvature issue. These 3 substrates are heated up in the same run until the temperature is stabilized at 1100  $^{\circ}\text{C}$ , 1120  $^{\circ}\text{C}$ , 1140  $^{\circ}\text{C}$ , 1160  $^{\circ}\text{C}$ , 1180  $^{\circ}\text{C}$  and 1200  $^{\circ}\text{C}$  under an  $\text{H}_2$  atmosphere. All the curvature values are measured by the Laytec Epicurve system.

Figure 4.5 shows the in-situ curvatures of the 3 substrates as a function of temperature ramping time which indicates a temperature variation as a function of time. The green curve corresponds to the 430  $\mu\text{m}$  Si wafer in the temperature range of 1100  $^{\circ}\text{C}$  ~ 1200  $^{\circ}\text{C}$ , showing that the curvature starts from 20  $\text{km}^{-1}$  at 1100  $^{\circ}\text{C}$  and gradually increases with increasing temperature and ends at 25  $\text{km}^{-1}$  at 1200  $^{\circ}\text{C}$ . According to Equation (4.6), the increase in curvature is due to an increase in the temperature variation  $\Delta T_A$  between the top and the bottom of the silicon substrate.

Considering that  $\alpha_{\text{Si}}$  of Si is  $4.3 \times 10^{-6} \text{ K}^{-1}$ , the calculated  $\Delta T_{\text{A}}$  is  $\sim 2 \text{ }^\circ\text{C(K)}$  at  $1100 \text{ }^\circ\text{C}$ , and  $\sim 2.5 \text{ }^\circ\text{C(K)}$  at  $1200 \text{ }^\circ\text{C}$ . For the Si wafer with a thickness of  $1030 \text{ }\mu\text{m}$  which is labelled as purple as shown in Figure 4.5, the curvature in the temperature range from  $1100 \text{ }^\circ\text{C} \sim 1200 \text{ }^\circ\text{C}$  is from  $25 \text{ km}^{-1}$  to  $30 \text{ km}^{-1}$ , this gives that  $\Delta T_{\text{B}}$  is  $\sim 6 \text{ }^\circ\text{C(K)}$  at  $1100 \text{ }^\circ\text{C}$  and  $\sim 7 \text{ }^\circ\text{C(K)}$  at  $1200 \text{ }^\circ\text{C}$ , respectively.

For the sapphire substrates with a thickness of  $330 \text{ }\mu\text{m}$  labelled as the black curve as shown in Figure 4.5, it shows the curvature change during the same temperature range as above, giving a curvature change from  $54 \text{ km}^{-1}$  to  $64 \text{ km}^{-1}$  in the temperature range from  $1100 \text{ }^\circ\text{C}$  to  $1200 \text{ }^\circ\text{C}$ . This value is much higher than that on the Si wafer but its  $\Delta T_{\text{C}}$  is from  $\sim 2 \text{ }^\circ\text{C(K)}$  to  $\sim 2.4 \text{ }^\circ\text{C(K)}$  using a thermal expansion coefficient  $\alpha_{\text{Sapphire}}$  of  $8.8 \times 10^{-6} \text{ K}^{-1}$ . This temperature variation  $\Delta T_{\text{C}}$  is quite close to  $\Delta T_{\text{A}}$ , while both are much smaller than  $\Delta T_{\text{B}}$ . This indicates that the vertical temperature uniformity is mainly related to the wafer thickness at high temperatures among those three kinds of substrates. These results might be because the variation of thermal conductivity between Si and Sapphire at such a high temperature is not significant enough to overcome the cooling effects caused by the surface gas flow, giving them very similar surface temperatures at the same wafer thickness.

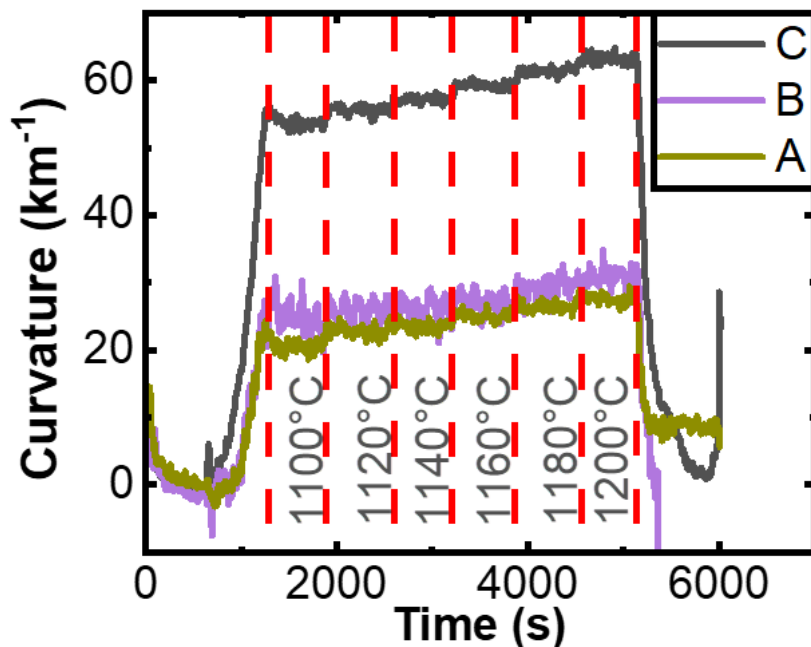


Figure 4.5 Wafer curvature at different temperatures for A  $430 \text{ }\mu\text{m}$  Si wafer, B  $1030 \text{ }\mu\text{m}$  Si wafer and C  $330 \mu\text{m}$  Sapphire wafer.

The vertical temperature uniformity caused by the wafer bowing at high temperatures has been investigated by performing in-situ curvature measurements on three different kinds of substrates: one 330 $\mu\text{m}$  Sapphire wafer, one 430 $\mu\text{m}$  Si wafer and one 1030 $\mu\text{m}$  Si wafer. Their vertical temperature variations have been measured by the in-situ curvature monitoring system Laytec Epicurve. Furthermore, the obtained results indicate that the vertical temperature uniformity of the wafer is mainly determined by thickness.

### **4.2.3 Growth of AlN on (111)Silicon**

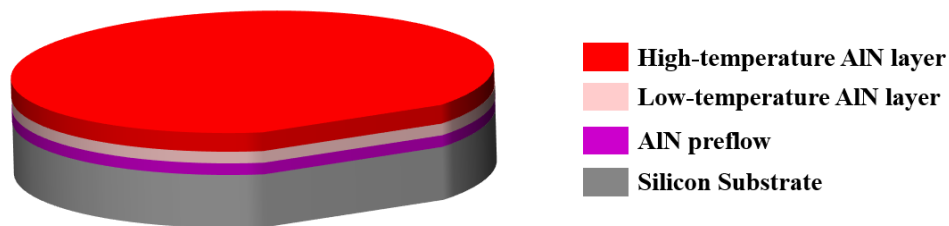
Si substrates have been used for optimising the growth of GaN on silicon substrates. AlN growth is the first step of the GaN-on-silicon growth process, where the crystal quality and surface roughness of the AlN layer play a critical role in determining the quality of subsequently grown layers. Therefore, it is important to optimise AlN growth conditions on Si. In this section, TMAI pre flow and AlN growth rates, the two key parameters, have been used to demonstrate that these two key elements play an important role in growing AlN with high quality.

Two major methods for an initial process are used before the growth of AlN on a silicon substrate:  $\text{NH}_3$  nitridation and TMA preflow. The former means that AlN is directly grown on silicon after silicon nitridation (i.e., initially flowing  $\text{NH}_3$  before flowing TMAI precursor and  $\text{NH}_3$ ), while the latter requires flowing TMAI preflow but without  $\text{NH}_3$  for a short time on a silicon substrate, giving a very thin Al metal film prior to the growth of AlN on the silicon substrate. Generally, the TMA preflow method leads to high crystal quality, while the  $\text{NH}_3$  nitridation approach gives good reproducibility but reduces crystal quality. In this work, the TMA preflow method was chosen to perform an AlN layer grown on Si. Based on this method, this section is investigating the influence of TMA preflow on the crystal of AlN.

As shown in Figure 4.6, AlN growth on a silicon substrate consists of 3 steps: TMAI preflow, a thin AlN layer prepared at a low-temperature growth and then at a high-temperature. In addition to that, all the samples used in this section are grown on 1030  $\mu\text{m}$  (111) Silicon substrates which undergo a high-temperature annealing process under a hydrogen ambience as mentioned in Section 4.2.1. After that, the growth temperature drops to 1150  $^\circ\text{C}$  for the TMA preflow to form a very thin Al film and then the low-temperature AlN growth. Specifically, the preflow and the low-temperature AlN growth are both

conducted by using a same TMAI flow rate of 20 sccm. After the TMAI preflow process, 300 sccm ammonia is then injected to the reactor chamber for the low-temperature AlN growth.

Subsequently, the growth temperature rises to 1300 °C for the high-temperature AlN growth. During the high-temperature AlN growth, different TMA and ammonia flowrates are used for different samples by changing the AlN growth rate and therefore investigate the influence of growth rate on the surface morphology.



*Figure 4.6 Structure of the AlN on Silicon.*

Figure 4.7a shows typical examples of the in-situ reflectance measurements during AlN preflow by using the in-situ monitoring system equipped with a 635nm laser. Please note that the normalised reflectance is shown in the figure, which is defined using the reflectance value just prior to the TMAI preflow as a baseline that is labelled as the black curve. It has been found that an insufficient preflow situation leads the reflectance to drop very slowly after the NH<sub>3</sub> is then injected into the reactor chamber, which means the growth rate of the subsequent low-temperature AlN growth layer is dramatically lower than in the proper preflow situation. The blue line shows a sharp increase in the reflectance, indicating an overpreflow for TMAI, while the red line shows the situation when the preflow is about enough. Too thick Al film as a result of the over-deposition generally leads to AlN with a low crystal quality. By carefully monitoring the reflectance of the initial TMAI preflow, we will be able to optimise the doses of TMAI preflow, where the optimised doses is that its normalized reflectance is around 1.01, meaning a very thin Al metal is a key factor for achieving high quality AlN.

According to Fresnel equations for normal incidence, the reflectance  $R$  can be calculated by the refractive index  $n_0$  of the medium where the light is coming from and the refractive index  $n_1$  of the reflected material following the equation below,

$$R = \frac{(n_0 - n_1)^2}{(n_0 + n_1)^2} \quad (4.7)$$

where  $n_0$  is the refractive index of the air or vacuum which is one,  $n_{Si}$  is the refractive index of Si which is 3.88, the reflectance before preflow  $R_{Si}$  can be estimated as 0.348. During the preflow, only TMA sources enter the reactor and only Al metal is deposited on the silicon. If an proper Al metal surface is fully covered the silicon substrate, its reflectance could rise to  $\sim 0.9$ , while the reflectivity in between is for a very thin Al film.

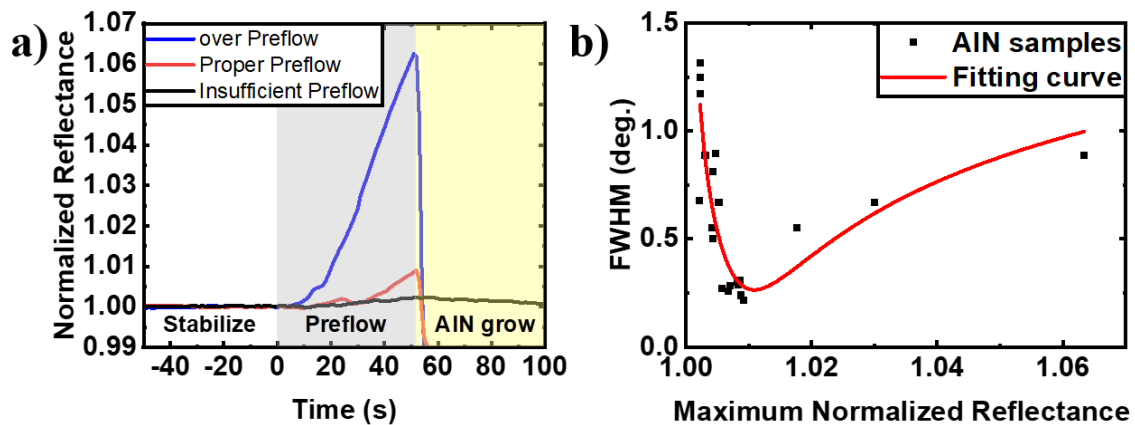


Figure 4.7 a) Example of AlN preflow reflectance during growth, the normalized reflectance value is the actual reflectance value divided by the initial reflectance when the preflow starts. b) Relation between the AlN crystal quality (determined by XRD curve FWHM) and the maximum normalized reflectance of Preflow.

Figure 4.7b demonstrates a relationship between AlN crystal quality (evaluated by using the FWHM of XRD rocking curve of AlN) and the normalized reflectance value (at the endpoint of the preflow). All the AlN crystal qualities are determined by the FWHM of the XRD rocking curves measured along the 002 direction. It is clear that the lowest FWHM of the XRD rocking curve is obtained when the maximum normalized reflectance is around 1.01, which means that only a very tiny amount of TMAI preflow is required for producing a high crystal quality AlN layer on Si. We have developed this simple and useful method to grow a high-quality AlN layer in a very reproducible manner.



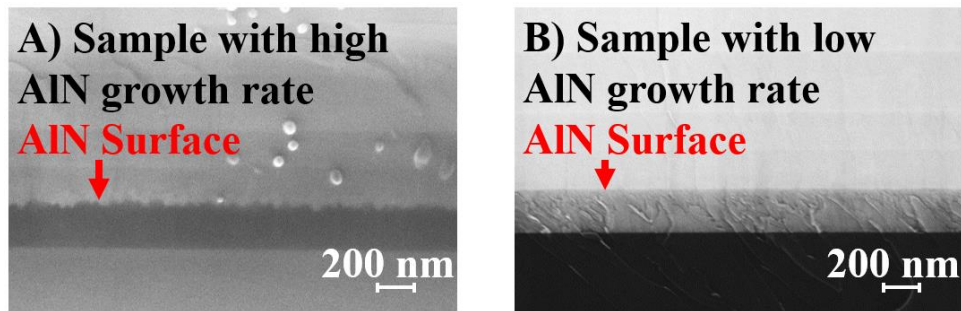


Figure 4.8 SEM pictures from a cross-section view of A) Sample with high AlN growth rate and B) Sample with low AlN growth rate.

Next, by decreasing the growth rate of high-temperature AlN growth, a flat surface can be achieved. Figure 4.8 shows the typical cross-section SEM pictures of two samples grown using different high-temperature AlN growth rates, where Figure 4.8a shows the sample grown at a TMA flow rate of 120 sccm and an ammonia flow rate of 500 sccm for 750 seconds while Figure 4.8b shows the sample prepared using a TMA flow rate of 30 sccm and an ammonia flow rate of 120 sccm during 2300 seconds. In both cases, the thicknesses of the AlN remains unchanged. From the SEM pictures, it is clear that the AlN surface grown at a high growth rate is much rougher than that at a low growth rate.

A study is conducted to investigate the influence of TMAI preflow and high-temperature AlN growth rates on the quality of AlN in terms of surface morphology and crystal quality. It is crucial to control a tiny amount of TMAI preflow in order to achieve high-quality AlN. In order to address a reproducibility issue, we have developed a simple method to monitor the amount of TMAI preflow by simply monitoring the reflectance. Moreover, the growth rate for subsequent high-temperature AlN has a major impact on the surface morphology and crystal quality of AlN. Our conclusion is that an atomically flat AlN surface can be obtained using a low growth rate.

#### 4.2.4 Optimisation of AlGaIn buffer growth

This section investigates the key factors which can affect the growth of AlGaIn buffer layers grown on AlN on silicon. The AlGaIn buffers leads the subsequently grown GaN to suffer from compressive strain which is used to compensate the tensile strain generated during the final cooling process. Therefore, it is necessary to carefully design AlGaIn buffer layers in terms of Al content and each AlGaIn layer thickness. This work is targeting cracking free GaN layers with a total thickness of 2.5  $\mu\text{m}$  (a 2.2  $\mu\text{m}$  GaN layer and a 300 nm n-GaN layer). Optical microscope has been used as a routine characterisation tool to examine under

surface morphology and cracking. Finally, the optimised growth conditions for the AlGaN buffer layer including thickness, Al content and NH<sub>3</sub> flow rate have been achieved.

AlGaN buffer layers typically consists of a number of AlGaN layers with graded Al content, where the growth conditions under investigation include thickness, Al content, and NH<sub>3</sub> flow rate.

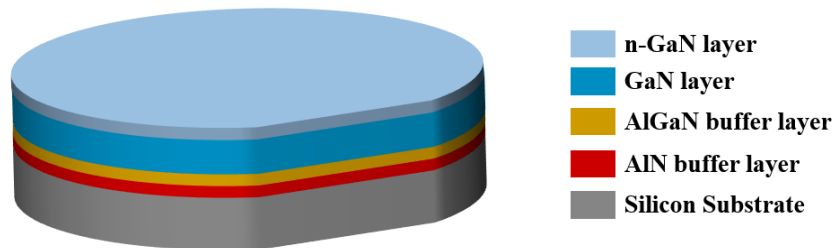


Figure 4.9 Structure of GaN on Si wafer with one AlGaN layer.

Three sets of samples, designated as Group A, Group B, and Group C, have been designed and then grown aiming to obtain the optimised conditions for the growth of AlGaN. In each case, a Si substrate was initially annealed at a high temperature under H<sub>2</sub> ambience for surface treatment as discussed above, followed by the TMA preflow process at 1150 °C and then the low-temperature AlN layer growth. Subsequently, a high-temperature AlN layer was deposited at 1350 °C at a low growth rate to perform a high-quality AlN layer with a smooth surface. After than an AlGaN buffer layer with different Al content in each case were grown. Figure 4.9 schematically shows the structure of these samples. Next, a single AlGaN layer with fixed Al content was grown under different conditions for optimisation purpose, where the Al content was determined by XRD measurements. Finally, a 2.2 μm GaN layer and a 300 nm n-GaN layer were grown.

Table 4-1 Growth conditions of AlGaN layer in different groups.

Sample Group	Sample Label	Thickness (nm)	Al Content (%)	NH <sub>3</sub> (sccm)
Group A	A1	646	27	1000
	A2	500	26	1000

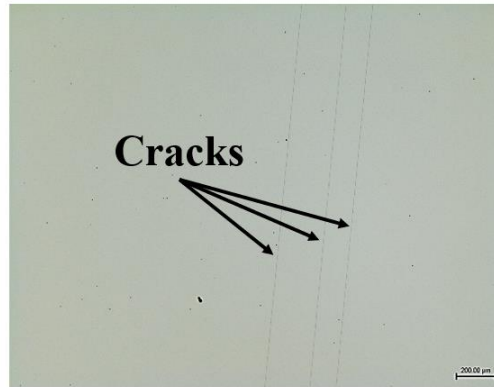
Group B	B1	646	29.2	1000
	B2	646	27	1000
	B3	646	26.2	1000
Group C	C1	646	26.5	2800
	C2	646	27	1400
	C3	646	26.5	1000
	C4	646	27	700

Table 4-1 lists the growth conditions of all the samples in the 3 groups. For the 1<sup>st</sup> group, Sample A1 has an AlGa<sub>0.2</sub>N layer of 646 nm while Sample A2 has a 500 nm AlGa<sub>0.2</sub>N. In both cases, the Al content is similar, and is about 26% or 27%. The AlGa<sub>0.2</sub>N thicknesses are controlled by tuning the growing time of AlGa<sub>0.2</sub>N. For the 2<sup>nd</sup> group which consists of three samples all with identical thickness but with different Al content, this offers an opportunity to investigate the influence of Al content, where Sample B1, B2 and B3 with Al content of 29.2, 27 and 26.2 are used, respectively. The Al content can be changed by tuning either TMAI or TMG source flow rate and the Al content is determined by carrying out XRD measurement in a  $\omega$ -2 $\theta$  scan mode. The third group which consists of 4 samples is designed to investigate the influence of the NH<sub>3</sub> flow rate on AlGa<sub>0.2</sub>N growth.

**a) Sample A1**



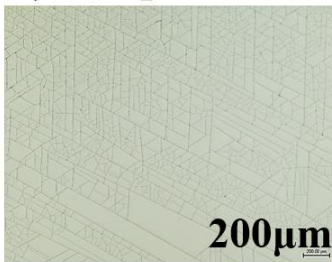
**b) Sample A2**



*Figure 4.10 Results of Group A. Among those samples, the sample with a thicker AlGa<sub>N</sub> layer does not have any cracks.*

Figure 4.10. shows the optical microscopy images of the samples in the 1<sup>st</sup> group (i.e., Group A), demonstrating that Sample A1 (shown in Figure 4.10a) has a crack-free surface, whereas Sample A2 has visible cracks. Since Samples A1 and A2 with different AlGa<sub>N</sub> thickness were grown under the same conditions, it is obvious that a thicker AlGa<sub>N</sub> helps reduce cracking.

**a) Sample B1**



**b) Sample B2**



**c) Sample B3**



*Figure 4.11 Results of Group B. Among those samples, Samples with a lower Al content AlGa<sub>N</sub> layer does not have any cracks. Besides, Samples with lower Al content AlGa<sub>N</sub> layers would have lower surface pits densities.*

Figure 4.11 shows the optical microscopy images of the samples in the 2<sup>nd</sup> group (i.e., the Group B). Severe cracking has been observed on Sample B1, while Sample B2 and Sample B3 don't. Moreover, Sample B1 shows a higher density of cracks than Sample A2. By carefully examining the surface, it has been observed that these samples in the 2<sup>nd</sup> group exhibit pits whose density decreases with decreasing Al content. This evidence suggests that the Al content of less than 29% help not only reduce cracking issue but also improve surface morphology.

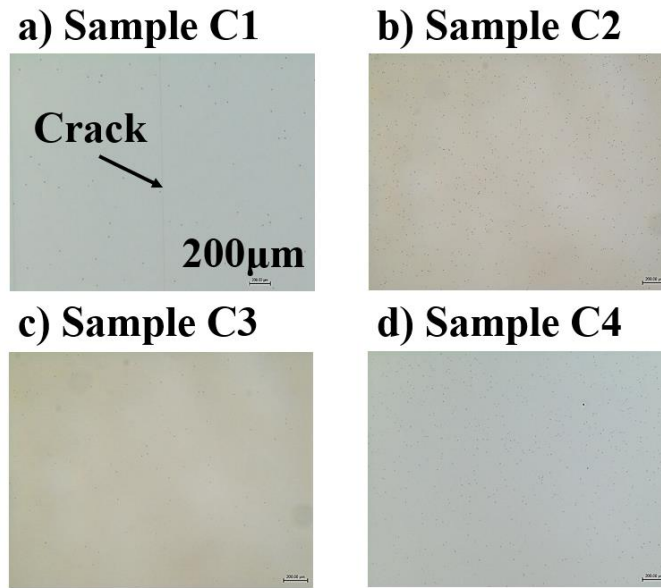


Figure 4.12 Results of Group C. Among those samples, Samples grown under lower  $\text{NH}_3$  flow rate does not have any cracks. Besides, Sample C3, which is grown under a medium  $\text{NH}_3$  flow rate, shows the lowest surface pits densities.

Figure 4.12 shows the optical microscopy images of the samples in the 3<sup>rd</sup> group (i.e., Group C). Among these 4 samples, only Sample C1 exhibits cracks. Furthermore, the surface pits density among the three cracking-free samples reduces dramatically, where Sample C3 shows the least pit density.

In this section, the influence of growth conditions such as thickness, Al content, and  $\text{NH}_3$  flow rate on surface morphology and cracking issues have been investigated. As a consequence, the cracking issue can be eliminated by optimising Al content and AlGa<sub>N</sub> thickness while the pit density is more sensitive to Al content and  $\text{NH}_3$  flow rate. Furthermore, the optimised growth conditions for obtaining a single cracking-free AlGa<sub>N</sub> layer are 27% Al content and a thickness of 646 nm grown under a ammonia flow rate of 1000 sccm.

#### 4.2.5 Optimization of GaN Growth

So far, the above optimisation of AlN growth and then AlGa<sub>N</sub> buffer layers growth aims to generate strain engineering to allow further GaN growth to obtain enough compressive strain which compensate tensile strain generated during the final cooling process. In this case, cracking-free GaN can be achieved. In the meantime, it is also necessary to ensure that reasonably good crystal quality can be obtained. In this section, we developed a 2-step method for GaN growth on AlGa<sub>N</sub>/AlN/Si. During the growth process, in situ reflectance

monitoring system has been used to monitor any surface change. A Bruker D8 X-ray diffractometer system has been used to perform XRD rocking curve measurements, where the FWHM of the XRD rocking curve has been used to evaluate crystal quality including the estimation of the dislocation density of the GaN. Optical microscopy measurements have been conducted to evaluate the surface morphology of the GaN. Finally, the optimized GaN growth conditions have been concluded.

Unlike the growth of GaN on Sapphire, an AlN/AlGaIn buffer layer is required prior to the growth of the GaN layer due to melting-back, and the large thermal expansion coefficient difference between GaN and Si. Additionally, the large lattice-mismatch between GaN layer and Si is very large which is comparable to that between GaN and Sapphire, resulting in a high defect density. This section aims to optimise the MOCVD conditions for subsequent GaN growth, leading cracking-free GaN with high crystal quality and atomically flat surface. Our procedure for GaN growth consists of two steps, aiming to initially perform a three dimensional mode and then a two-dimensional growth mode. This combined mode leads to enhance crystal quality which we have learned from GaN growth on sapphire. It means that an island-like GaN layer is initially obtained, followed by a coalescence process. This eventually results in a smooth surface and enhanced crystal quality.

A number of GaN samples were continuously grown on Al<sub>0.17</sub>GaN/Al<sub>0.35</sub>GaN/Si in order to identify the optimised growth conditions. All the Si treatment and AlN layer growth were carried out under the optimised conditions discussed in Section 4.2.4. The AlGaIn buffer layers consist of an initial Al<sub>0.35</sub>GaN layer deposited on the AlN layer with a thickness of ~260 nm and then another 440 nm Al<sub>0.17</sub>GaN layer. Afterwards, the 2-step GaN method was performed, where the 2 GaN layers grown by this method are labelled as GaN-1 layer and GaN-2 layer. The total thickness of these two layers is 1.5 μm including a 300 nm n-GaN layer.

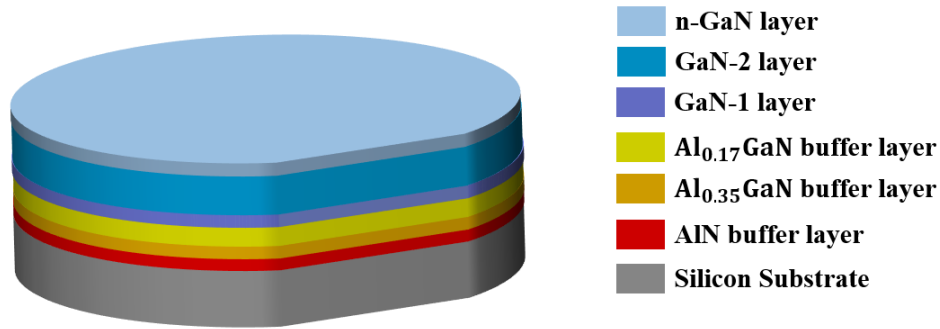


Figure 4.13 Structure of GaN on Si wafer with 2-step GaN layers.

The in-situ reflectance has been measured by using a 635 nm laser Interferometer system. A Bruker D8 X-ray diffractometer system has used for evaluating the crystal quality by performing XRD rocking curve measurements, where this FWHM of the XRD rocking curves can be used to estimate the dislocation density. Surface morphology was conducted by using a Nomarski optical microscopy system.

#### a) GaN Pause Mode

As explained in the introduction, the 2 step GaN growth method is aiming to form an island-like GaN layer in the first step, followed by a coalescence process to obtain a smooth surface in the 2<sup>nd</sup> step. However, due to a requirement in terms of the growth temperature limitation aiming to prevent cracking issue, it would be a challenge to carry out the coalescence process during the GaN-2 layer growth using a higher temperature as normally used in the case of sapphire substrate.

Therefore, a 'Pause mode' was during the GaN-2 layer growth, which is accomplished by stopping injecting the TMG source flow for a short period such as 120-second in a periodic manner while maintaining flowing NH<sub>3</sub> flow. This 'Pause mode' gives time to anneal the GaN facet during growth and therefore helps to form a better surface. Figure 4.14 and Figure 4.15 below show the in-situ reflectance and the optical microscopy images of the samples grown under the “pause” mode and normal continuous mode. The GaN-1 layer in both cases were grown under identical conditions: at 1215 °C with TMG/NH<sub>3</sub> flow rates of 49/3000 sccm for 700 seconds, which leads to a GaN-1 layer thickness of 325 nm. Except the “pause” The GaN-2 layer in both cases were also grown under the identical conditions at 1215 °C with TMG/NH<sub>3</sub> flow rates of 38/2100 sccm for 700 seconds, giving a thickness of 1230 nm for the GaN-2 layer.

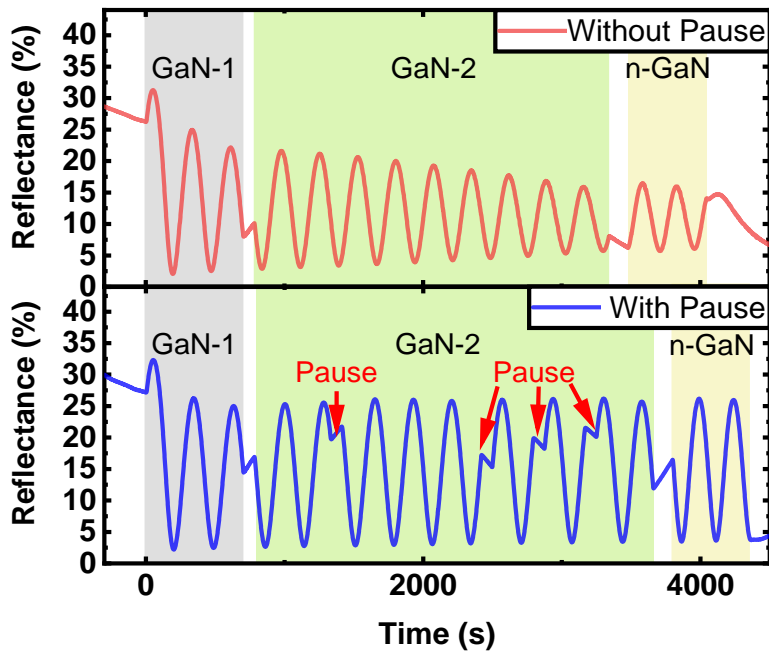


Figure 4.14 In-situ reflectance of Sample without and with Pause during GaN growth. The upper one is grown without Pause Mode while the lower one with. The one with a Pause mode has a higher reflectance at the end of GaN-2 growth step.

As shown by the red curve in Figure 4.14, the reflectance during GaN-2 growth of the sample without the ‘Pause’ mode keeps dropping, which indicates a degradation of the surface. This surface degradation ends up in a rough surface shown in Figure 4.15a with a large pit density on the surface. When the ‘Pause’ mode is applied, the trend of reflectance decreasing could be delayed and even reversed as shown by the blue curve in Figure 4.14. Consequently, a smooth GaN surface can be achieved as presented in Figure 4.15b.

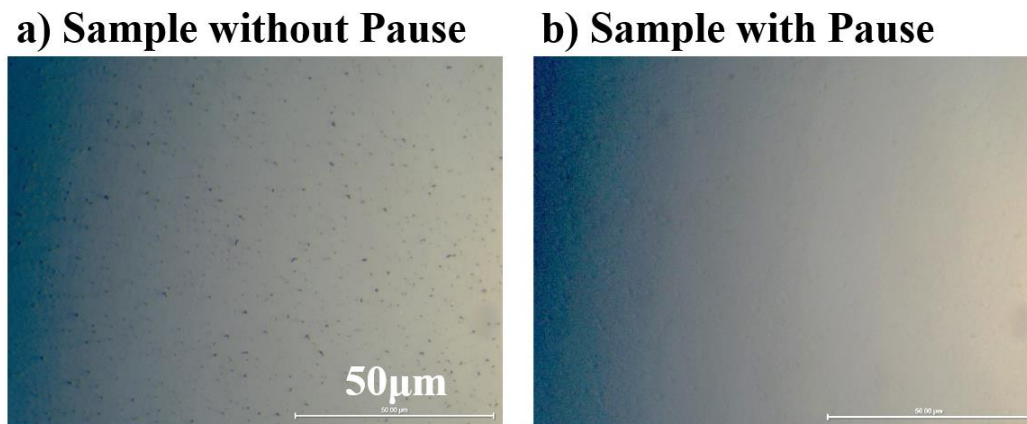


Figure 4.15 Optical microscope pictures of GaN surface on a) the Sample without Pause and b) the Sample with Pause. The one with Pause Mode has a much lower pits density.



b) GaN-1 layer thickness

Four samples were grown in the 'Pause' mode for the GaN-2 layer under the identical growth parameters as mentioned in the last section. For the GaN-1 growth for these four samples, the growth was carried out at 1210 °C and a TMG/NH<sub>3</sub> flow rate of 51/3000 sccm with a growth time of 700 s, 500 s, 400 s, and 300 s for each sample.

The crystal quality of the GaN layer is evaluated by estimating a screw dislocation density ( $D_{screw}$ ) and an edge dislocation density ( $D_{edge}$ ) by using FWHM of XRD rocking curves measured along the on-axis and the off-axis directions, which can be obtained by the using equations below:

$$D_{screw} = \frac{\beta_{(0002)}^2}{4.35b_{screw}^2} \quad (4.8)$$

$$D_{edge} = \frac{\beta_{(10\bar{1}2)}^2 - \beta_{(0002)}^2}{4.35b_{edge}^2} \quad (4.9)$$

where,  $\beta_{(0002)}$  and  $\beta_{(10\bar{1}2)}$  are the FWHM of symmetric (0002) and asymmetric (10 $\bar{1}2$ ) rocking curve scan, respectively. The Burgers vector for a screw-type dislocation and an edge-type dislocation are 0.5185 nm ( $b_{screw}$ ) and 0.3189 nm ( $b_{edge}$ ), respectively.

Table 4-2 Growth time variation and their crystal quality change.

Sample NO.	Growth Time (s)	GaN-1 Thickness (nm)	(002) GaN FWHM (deg)	Screw Dislocation density (cm <sup>-2</sup> )	(102) GaN FWHM (deg)	Edge Dislocation density (cm <sup>-2</sup> )
Sample 1	700	363	0.1063	2.94×10 <sup>8</sup>	0.1718	1.25×10 <sup>9</sup>
Sample 2	500	242	0.1095	3.12×10 <sup>8</sup>	0.1746	1.27×10 <sup>9</sup>
Sample 3	400	194	0.1383	4.98×10 <sup>8</sup>	0.2475	2.90×10 <sup>9</sup>

Sample 4	300	145	0.1509	$5.93 \times 10^8$	0.2852	$4.03 \times 10^9$
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As shown in the table above, it can be found that both the screw dislocation density and the edge dislocation density of GaN reduces with increasing GaN-1 layer thickness. For example, when the GaN-1 layer is over 240 nm, the final GaN screw density and the edge dislocation density are  $3 \times 10^8 \text{ m}^{-2}$  and  $1.25 \times 10^9 \text{ m}^{-2}$ , respectively, the best crystal quality among the 4 samples.

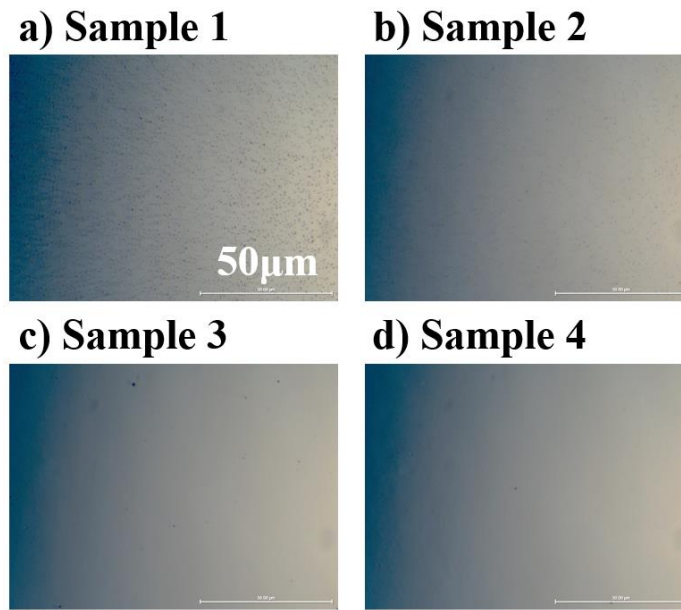


Figure 4.16 Optical images of a) Sample 1 for 700s GaN-1, b) Sample 2 for 500s GaN-1, c) Sample 3 for 400s GaN-1 and d) Sample 4 for 300s GaN-1. Among those samples, the pits density decrease with the decrease of the GaN-1 growth time.

However, it is worth highlighting that a thick GaN-1 layer generally leads to a degradation in surface morphology. As shown in Figure 4.16, the pit density increases with increasing GaN-1 thickness and becomes unacceptable when the GaN-1 thickness is over 200 nm.

By applying a 2-step GaN growth method, the crystal quality and the surface conditions of the GaN on the Si wafer can be improved. Furthermore, a ‘Pause’ mode for the GaN-2 layer growth and the GaN-1 layer thickness have been discussed in this section, further improving the crystal quality of GaN. As a consequence, the optimized GaN-1 layer should be around 200 nm and a ‘Pause’ mode is necessary for the GaN-2 layer growth.

### 4.3 Conclusions

GaN on Si growth is very complicated due to the large lattice-mismatch and the large thermal expansion coefficient difference between GaN and silicon in addition to melting back issue at a high temperature. A number of steps are required for GaN growth on silicon including silicon substrate preparation, AlN layer growth, AlGaIn buffer layer growth, and GaN layer growth, each of which has been investigated in detail and then optimised. A direct high-temperature annealing method without any prior chemical treatment has been chosen for Si surface treatment. The in-situ curvature measurements suggest the influence of substrate thickness on the vertical temperature uniformity is also important. Additionally, it is found that an AlN layer with both good crystal quality and smooth surface on a Si substrate can be achieved by properly controlling TMA-preflow and optimising a low high-temperature AlN growth rate. Furthermore, AlGaIn buffer growth conditions including thickness, Al content, and NH<sub>3</sub> flow rate have been identified to play a critical role in achieving a crack-free GaN-on-Si template. Finally, for the GaN growth, a two-step GaN growth method has been developed aiming to achieve GaN with both high crystal quality and smooth surface. However, the thickness of the first step GaN has a significant influence on the final GaN crystal quality and surface roughness, resulting in a trade-off between the GaN surface and the crystal quality. With the experiments above, optimized conditions for both surface treatment, AlN growth and AlGaIn growth can be obtained. As for the GaN layers for the subsequent work, the thickness of the first step GaN is controlled to be between 400nm and 500nm, trying to get the best GaN quality under an acceptable surface.

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# Chapter 5 Growth of GaN-Based Electrical and Optical devices on (111) Silicon

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After discussing how Gallium Nitride (GaN) is grown and optimised on Silicon (Si) wafers in the previous chapter, this chapter addresses the electrical and optical devices produced on such wafers and paves the path to transfer the epitaxially integrated micro light-emitting diode ( $\mu$ LED) and high electron mobility transistors (HEMTs) from sapphire to silicon substrate. All device structures are grown using metal-organic chemical vapour deposition (MOCVD), and their surface, in-situ curvature, emission wavelength, current-voltage (I-V) curve and crystal quality are measured using optical microscopy, scanning electron microscopy (SEM), the Laytec Epicurve, PL system, two-channel Keithley 2612B source meter (Cleveland, OH, USA) and the Bruker X-ray diffractometer (XRD), respectively. GaN-based HEMT and LED on Si substrate are discussed in separate two sections respectively. The growth and characteristics of those devices are demonstrated in this chapter.

## 5.1 Introduction

In the last decade, III-nitride devices have been widely used in many applications, such as general illumination [1], radio-frequency communication [2] and power conversion [3], etc. Especially for electronic applications, GaN high electron mobility transistors (HEMTs) are expected to demonstrate a number of major advantages, such as a fast switching speed, low switching loss and high power conversion efficiency in comparison with silicon-based counterparts.[4] Thus far, a number of substrates have been explored for the growth of GaN HEMTs, such as sapphire ( $\text{Al}_2\text{O}_3$ ), silicon, silicon carbon (SiC) and free-standing GaN, among which silicon substrates are becoming more attractive to the semiconductor industry due to the mature silicon technology, good thermal conductivity and scalability. However, there is a large lattice mismatch and a large thermal expansion coefficient (TEC) difference between GaN and silicon, typically causing extensive cracks in the post-growth cooling down process [5]-[9], and thus posing a great challenge for growing GaN HEMTs on silicon substrates.



A further device structure, InGaN/GaN multiple quantum wells (MQWs) normally acting as an active region (for achieving the display function) is then grown on the Si substrate. It has been understood that stress modifies the vapour-solid thermodynamic equilibrium, reducing the solid-phase epitaxial composition towards lattice-matched conditions and thus limiting indium incorporation into GaN.[10],[11] In other words, an indium incorporation rate into GaN depends on the strain status of the GaN underneath. Normally, tensile stress enhances an indium incorporation rate into GaN, facilitating higher indium content in GaN which is crucial for achieving III-nitride emitters with a long emission wavelength such as green or yellow. This will help to mitigate the well-known “green/yellow gap” issues. GaN on sapphire is subjected to compressive strain while GaN on silicon exhibits tensile strain. Therefore, it is expected that the InGaN MQWs grown on GaN-on-sapphire will be different from those grown on GaN-on-silicon even under identical growth conditions. Given that there is an increasing demand for developing microLED based microdisplays, where Si-CMOS is normally used as an electronic driver,[12]-[17] requires transferring the mature growth technologies from GaN-on-sapphire to GaN-on-Si for III-nitride emitters. However, so far, there is almost an absence in reporting a comparison study on the growth of InGaN MQWs on GaN-on-sapphire and GaN-on-silicon. This is the main purpose of our work presented in the later section of this chapter.

In this chapter, a very basic HEMT and an InGaN/GaN MQWs epi structure are grown. Both of them are achieved on a GaN buffer layer grown on Si substrate with an AlN and two graded composition  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  buffer layers in between. For the HEMT structure, its strain components are demonstrated by X-ray reciprocal space mapping (RSM) and the device performance is also exhibited. For the MQWs structure, a comparison group of a GaN on Sapphire template is prepared and used for the MQWs growth in the same run with the experiment group of GaN on Si template. Both samples have been subjected to photoluminescence (PL) and comprehensive x-ray diffraction (XRD) examinations, revealing a considerable variance in their structure and optical characteristics. Furthermore, in-situ monitoring curvature measurements have been conducted, demonstrating the stress status on both samples during growth.

## 5.2 Experiments and Results Discussion

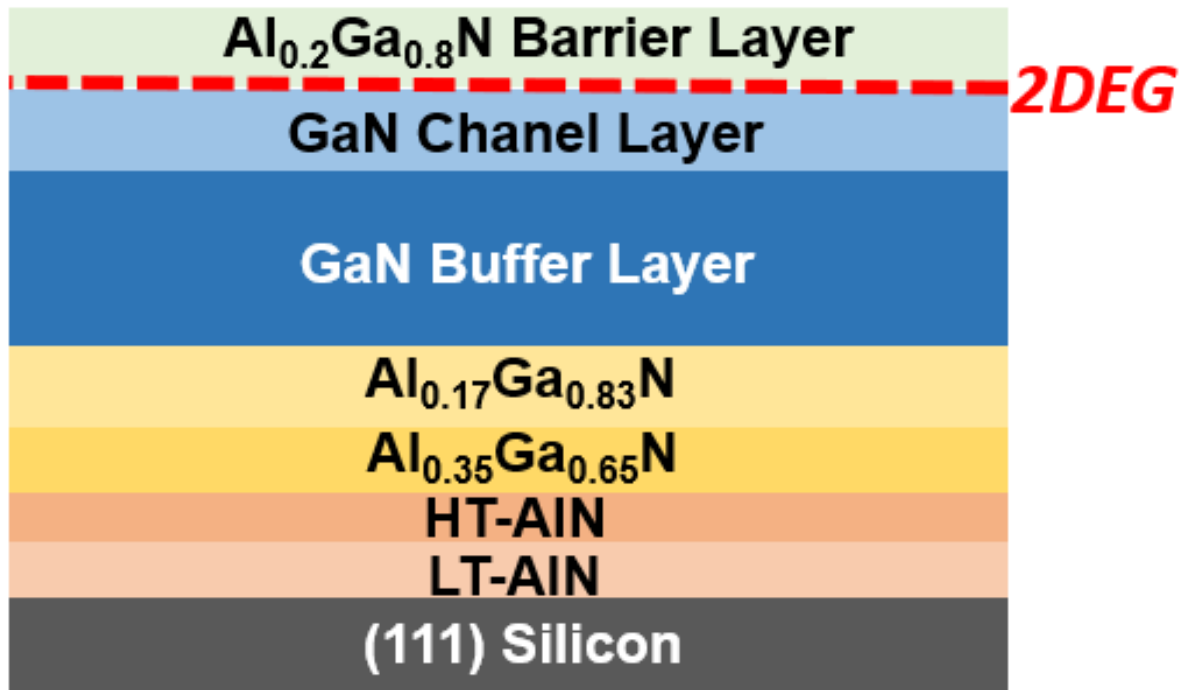
### 5.2.1 Strain Analysis of GaN HEMTs on (111) Silicon with Two Transitional $\text{Al}_x\text{Ga}_{1-x}\text{N}$ Layers

We have designed and then grown a simple structure for high electron mobility transistors (HEMTs) on silicon, where as usual two transitional layers of  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  ( $x = 0.35$ ,  $x = 0.17$ ) have been used in order to engineer the induced strain as a result of the large lattice mismatch and large thermal expansion coefficient difference between GaN and silicon. Detailed x-ray reciprocal space mapping (RSM) measurements have been taken in order to study the strain, along with cross-section scanning electron microscope (SEM) images and x-ray diffraction (XRD) curve measurements. It has been found that it is critical to achieve a crack-free GaN HEMT epi-wafer with high crystal quality by obtaining a high quality AlN buffer, and then tuning the proper thickness and aluminium composition of the two transitional  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  layers. Finally, HEMTs with high performance that are fabricated on the epi-wafer have been demonstrated to confirm the success of our strain engineering and above analysis.

In this section, we design a very simple HEMT epi-structure with one AlN buffer layer, only two graded transitional  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  layers and then a GaN/ $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$  heterostructure. This simple structure allows us to analyze the strain more clearly for the graded  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  transitional layers with different compositions and thicknesses. By measuring X-ray reciprocal space mapping (RSM), the strain components in our  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  layers can be obtained and then feed back into epi-wafer growth. Finally, the HEMTs with high performance have been demonstrated, verifying the quality of our GaN HEMT epi-wafers.

Figure 5.1 schematically displays the GaN HEMTs epi-structure used. First, a standard 2-inch (111) silicon wafer is loaded into a low-pressure metalorganic vapour-phase epitaxy (MOVPE) system (Aixtron, Herzogenrath, Germany) and subjected to a high temperature (1320 °C) annealing process under  $\text{H}_2$  ambiance to remove any contaminants and native oxides. Subsequently, the temperature is decreased to 1000 °C and a trimethylaluminium (TMA) pre-flow is conducted without any  $\text{NH}_3$  flowing for 40 s. A thin low-temperature AlN (LT-AlN) layer is then grown, followed by a high temperature AlN (HT-AlN) layer grown at 1297 °C. The thickness of the AlN layer is 260 nm in total. Next, two layers of  $\text{Al}_{0.35}\text{Ga}_{0.65}\text{N}$  and  $\text{Al}_{0.17}\text{Ga}_{0.83}\text{N}$  have been further grown as strain-compensation transitional

layers. After finishing the growth of the two  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  transitional layers, a  $1.2\ \mu\text{m}$  (0001) GaN layer was then grown, followed by a final  $25\ \text{nm}$   $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$  barrier layer. During the cooling down procedure,  $\text{N}_2$  and  $\text{NH}_3$  are used as cooling gases in order to eliminate any micro cracks generated on the final  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  layer which has been accepted as a result of  $\text{H}_2$  enhanced surface etching [18].



*Figure 5.1 Epi-structure designed for our GaN high electron mobility transistors (HEMTs) with two graded  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  strain-compensation transitional layers grown on (111) silicon.*

The whole wafer has been examined across two inches by optical microscopy, confirming that it is crack-free except for the edge region of the wafer, as shown in Figure 5.2c,d. Furthermore, cross-sectional scanning electron microscope (SEM, Raith, Dortmund, Germany) measurements have been taken as shown in Figure 5.2a,b, taken from the central part and the edge part, respectively, indicating that the thicknesses for the AlN buffer layer, the  $\text{Al}_{0.35}\text{Ga}_{0.65}\text{N}$  layer, the  $\text{Al}_{0.17}\text{Ga}_{0.83}\text{N}$  layer and the GaN layer are  $258\ \text{nm}$ ,  $180\ \text{nm}$ ,  $290\ \text{nm}$  and  $1.18\ \mu\text{m}$ , respectively.

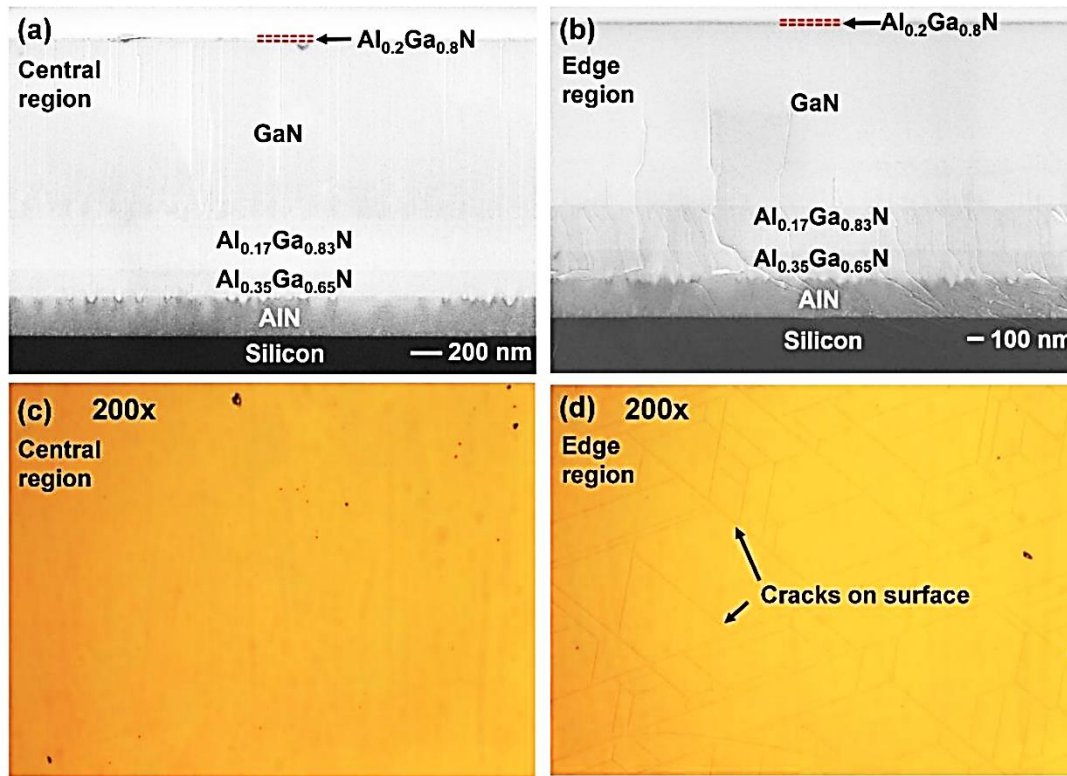


Figure 5.2 Cross-sectional SEM images of the epi-structure of GaN HEMT on silicon (a) in the central region and (b) in the edge region; Optical microscope images of the wafer surface (c) in the central region and (d) in the edge region.

By comparing Figure 5.2a,b, the AlN layer in the central part is flat and crack-free, which eventually leads to a crack-free region for the final device structure. In contrast, at the edge region, most cracks generated in the AlN layers merge into the second  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  layer, thus filtered by the  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  layers. However, there are still a few cracks penetrating the GaN layer which extend to the surface, as shown in Figure 5.2d. The differences of the crack densities in the AlN layers between the central and the edge regions may be caused by the differences in wafer bowing, which are measured to be 121  $\mu\text{m}$  and 63  $\mu\text{m}$  for the wafer centre and wafer edge, respectively. At the same time, we also note that our wafer centre bowing is comparable and even smaller than the reported 119  $\mu\text{m}$  in [19].

The crystal quality has been further characterized by X-ray diffraction (XRD, Bruker, Billerica, MA, USA) measurements as shown in Figure 5.3b-d, demonstrating that the full-width half-maximum (FWHM) values for the AlN and the GaN layers measured across the (002) reflection are  $0.3783^\circ$  and  $0.1348^\circ$ , respectively. The FWHM value for the GaN layer measured across the (102) GaN reflection is  $0.2533^\circ$ . Our (002) direction XRD result is better than the reported  $0.294^\circ$  and  $0.2^\circ$  in References [19][20], and close to the reported  $0.122^\circ$  and  $0.132^\circ$  in References [21][22]. Moreover, our (102) GaN direction XRD result

is also comparable to the reported  $0.24^\circ$  in Reference [20]. This represents that a high crystal quality has been achieved by our method, and also implies that it is crucial to obtain an AlN buffer with high quality, which is one of the factors leading to our high quality GaN grown on top.

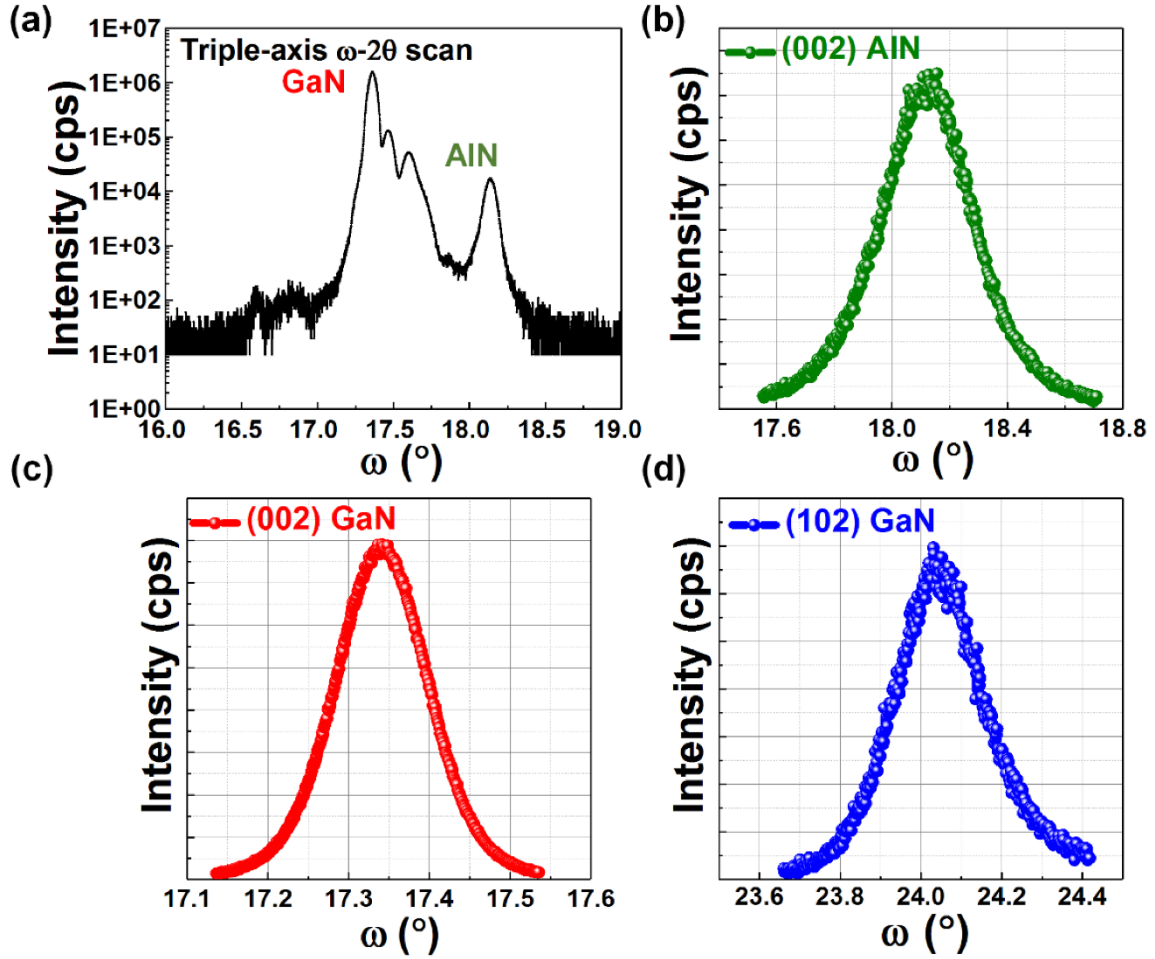


Figure 5.3 XRD results: (a)  $\omega$ - $2\theta$  scan aligned on AlN and XRD rocking curves of (b) (002) AlN, (c) (002) GaN and (d) (102) GaN.

According to Reference [23], the screw dislocation density ( $D_{screw}$ ) and edge dislocation density ( $D_{edge}$ ) in the GaN layer can be calculated by using the below equations:

$$D_{screw} = \frac{\beta_{(0002)}^2}{4.35b_{screw}^2} \quad (5.1)$$

$$D_{edge} = \frac{\beta_{(10\bar{1}2)}^2 - \beta_{(0002)}^2}{4.35b_{edge}^2} \quad (5.2)$$

where,  $\beta_{(0002)}$  and  $\beta_{(10\bar{1}2)}$  are the FWHM of symmetric (0002) and asymmetric (10 $\bar{1}2$ )  $\omega$  scan. Burgers vector lengths for screw-type and edge-type are 0.5185 nm ( $b_{screw}$ ) and 0.3189 nm ( $b_{edge}$ ), respectively.

Thus, we can get

$$D_{screw} = \frac{\beta_{(0002)}^2}{4.35(0.5185nm)^2} = 4.733 \times 10^8 cm^{-2}$$

$$D_{edge} = \frac{\beta_{(10\bar{1}2)}^2 - \beta_{(0002)}^2}{4.35(0.3189nm)^2} = 3.167 \times 10^9 cm^{-2}$$

With our growth method, the edge dislocation density is almost 7.3 times the screw dislocation density, thus edge dislocation dominates all the dislocations.

To further analyze the strain and Al composition effects on the strain compensation layers separately [24], reciprocal space mapping (RSM, Bruker, Billerica, MA, USA) measurements have been taken from the central part and the edge part along the [0002] and [112 $\bar{4}$ ] directions, which are shown in Figure 5.4. The golden dash line indicates the coordinates of GaN, Al<sub>x</sub>Ga<sub>1-x</sub>N and AlN layers in RSM maps. The solid white line shows the fully relaxed Al<sub>x</sub>Ga<sub>1-x</sub>N layers grown AlN. The green point with an Al content between 17% and 35% is the AlGa<sub>x</sub>N barrier of the HEMT structure. In Figure 5.4a,c, in the (0002) Bragg reflection plane, three epitaxial layers overlap with each other at Q<sub>x</sub> = 0, making it difficult to investigate the in-plane strain distribution of Al<sub>x</sub>Ga<sub>1-x</sub>N transitional layers. We rotated certain angles to the (112 $\bar{4}$ ) Bragg reflection plane to better analyze the in-plane strain, as shown in Figure 5.4b,d.

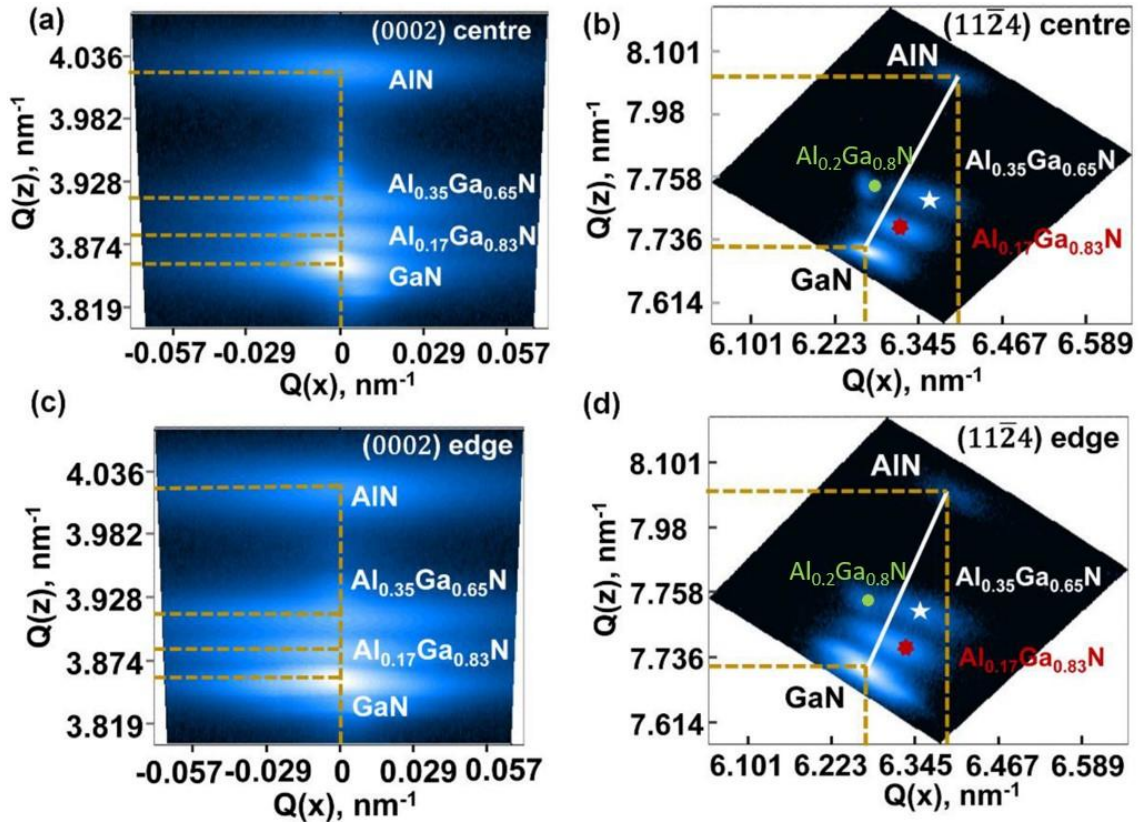


Figure 5.4 RSM results: (a) (0002) plane, (b)  $(11\bar{2}4)$  plane for central region, (c) (0002) plane and (d)  $(11\bar{2}4)$  plane for edge region.

Based on the RSM measurements, the compressive in-plane strain components accumulated in each  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  layer have been calculated according to the below equations:

$$a = \sqrt{\frac{4(h^2 + hk + k^2)}{3q_x^2}} \quad (5.3)$$

$$c = \frac{l}{q_z} \quad (5.4)$$

$$\tan[\alpha(x)] = \frac{q_x - q(x_0)}{q_z - q(z_0)} \quad (5.5)$$

$$\varepsilon_{zz} = -D(x)\varepsilon_{xx} \quad (5.6)$$

$$D(x) = 2 \frac{C_{13}(x)}{C_{33}(x)} \quad (5.7)$$

where  $(q_x, q_z)$  is the coordinates in the map, corresponding to the latticed constants (a,c); (h,k,l) is the Bragg reflection direction;  $(q(x_0), q(z_0))$  is the coordinates of the fully relaxed reciprocal lattice points (RLPs) with the same Al composition as the  $(q_x, q_z)$ ;  $\alpha(x)$  is the angle between the  $Q_z$  axis and the extended line interpolated from the two points described above;  $\varepsilon_{zz} = \frac{[c-c_0(x)]}{c_0}$ ,  $\varepsilon_{xx} = \frac{[a-a_0(x)]}{a_0}$  are in-plane and out-plane strain components, respectively, among which c and a are measured lattice parameters, where  $c_0$  and  $a_0$  are the relaxed parameters from Vegard's law;  $C_{i,j}(x)$  are the elastic constants.

For the GaN and AlN lattice constant,  $a_{GaN} = 3.189 \text{ \AA}$ ,  $c_{GaN} = 5.185 \text{ \AA}$ ,  $a_{AlN} = 3.112 \text{ \AA}$ ,  $c_{AlN} = 4.982 \text{ \AA}$  are used. For the elastic constants,  $C_{13} = 103 \text{ GPa}$ ,  $C_{33} = 405 \text{ GPa}$  for GaN [23] and  $C_{13} = 108 \text{ GPa}$ ,  $C_{33} = 373 \text{ GPa}$  for AlN [25] are used for calculation. We first calculate initial D(x) values for the first and second  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  layer, then use these initial D(x) values to obtain an initial  $\alpha(x)$  value and Al composition value. After several steps of iterative operations using the least-square method for error-minimization, we can finally get accurate values of the in-plane strain component  $\varepsilon_{xx}$ , as listed in Table 5-1.

*Table 5-1 Calculated in-plane strain components of the two strain-compensation  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  layers for both the wafer central and edge regions measured along with the  $[11\bar{2}4]$  direction.*

Location	1st layer $\text{Al}_{0.35}\text{Ga}_{0.65}\text{N}$	2nd layer $\text{Al}_{0.17}\text{Ga}_{0.83}\text{N}$
central	-0.00227	-0.00189
edge	-0.00174	-0.0011

From Table 5-1, we can see that the strain components in the wafer central region are larger than the ones in the wafer edge region. According to Reference [21], there are three strains causing the formation of the crack. Namely, the lattice-mismatched strain, the grain size growth strain (or dislocation relaxation-related strain) and the thermal expansion coefficient mismatched strain. The former two strains exist during the growth. The thermal strain occurs during the cooling down procedure. At the growth temperature, initial tensile strain accumulates during AlN growth. After  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  growth, the compressive strain accumulated. Finally, during the GaN growth, compressive strain increases at first and then decreases due to the dislocation relaxation. Given that the GaN thicknesses and dislocation



densities are almost the same for the wafer centre and edge, an equal amount of compressive strain accumulated in GaN layers and was consumed by dislocations during the growth procedure for the wafer centre and edge. However, cracks form only at the wafer edge after cooling down, so we can conclude that not enough initial compressive strain accumulated during the  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  transitional layers for the wafer edge leads to the cracks formed at the edge region when cooling down to room temperature.

To evaluate the whole HEMT epi quality, Hall measurements have also been conducted. The Ti/Al/Ti/Au (20/150/50/80 nm) alloys have been deposited as pads and thermally annealed in order to form Ohmic contacts. The Hall result shows that the carrier mobility of the two-dimensional electron gas (2DEG) is as high as  $1600 \text{ cm}^2 \text{ V}^{-1} \text{ S}^{-1}$ , which is less than, but still comparable to the reported  $2150 \text{ cm}^2 \text{ V}^{-1} \text{ S}^{-1}$  in Reference [21]. The high carrier mobility confirms the success of the strain compensation and a low dislocation density in the GaN channel layer, otherwise, carrier scattering is expected to lead to low mobility.

To further verify the epi quality, GaN HEMT devices are also fabricated on the HEMT epi-wafer. The fabrication process is described below: A 300 nm depth mesa is etched down to define the active region for the HEMT by inductively coupled plasma (ICP) etching, and then the metal stack of Ti/Al/Ti/Au (20/150/50/80 nm) is deposited and then annealed under an  $850 \text{ }^\circ\text{C}$   $\text{N}_2$  ambient atmosphere for 30 s in order to form Ohmic contacts for the source and drain of the HEMT. Finally, a Ni/Au (50/150 nm) layer is deposited in order to form a Schottky gate for the HEMT.

Figure 5.5a shows a schematic configuration of the HEMT device. Figure 5.5b shows a typical current-voltage (I-V) as a function of gate voltage, measured by a two-channel Keithley 2612B source meter (Cleveland, OH, USA). For the HEMT device with a gate length, gate-to-drain distance, gate-to-source distance and gate width of  $2 \text{ }\mu\text{m}$ ,  $15 \text{ }\mu\text{m}$ ,  $3 \text{ }\mu\text{m}$ , and  $120 \text{ }\mu\text{m}$ , respectively, it shows a maximum current density of  $290 \text{ mA/mm}$  at  $V_{\text{gs}} = 1 \text{ V}$  and  $V_{\text{ds}} = 8.8 \text{ V}$  and specific-on resistance of  $0.427 \text{ }\Omega\cdot\text{mm}^2$ , less than a half to the reported value of  $688 \text{ mA/mm}$  at  $V_{\text{ds}} = 9 \text{ V}$  in Reference [21], considering the large active area of our HEMT. These results indicate a high mobility and carrier density of the channel layers of our HEMT epi.

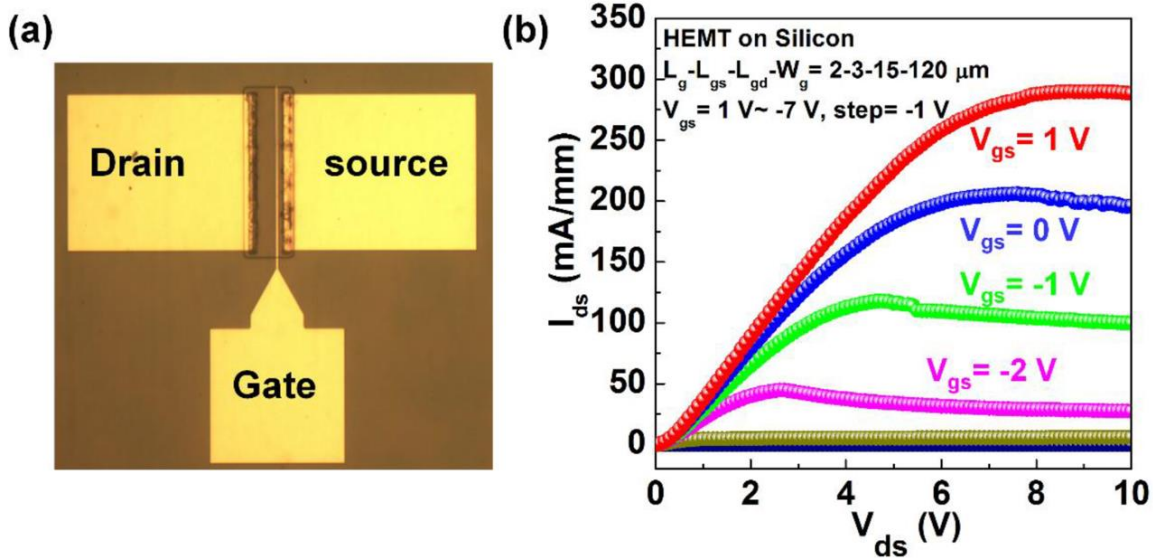


Figure 5.5 A schematic configuration of the HEMT device (a); current–voltage ( $I$ - $V$ ) as a function of gate voltage (b).

To conclude, we have achieved a crack-free GaN HEMT epi-wafer grown on silicon by properly tuning two  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  transitional layers. The compressive strain of GaN on the  $\text{Al}_{0.35}\text{Ga}_{0.65}\text{N}$  and  $\text{Al}_{0.17}\text{Ga}_{0.83}\text{N}$  layers on the AlN buffer is good enough to compensate for the tensile strain between GaN and silicon. As a result of a high crystal quality AlN buffer layer, high-quality GaN HEMTs on silicon with mobility of  $1600 \text{ cm}^2 \text{ V}^{-1} \text{ S}^{-1}$  and a current density of  $290 \text{ mA/mm}$  for  $120 \mu\text{m}$ -gate-length HEMTs have been achieved.

### 5.2.2 A comparison study of InGaN/GaN multiple quantum wells grown on (111) silicon and (0001) sapphire substrates under identical conditions

Given that there is a demand for developing III-nitride optoelectronics on silicon substrates, it is necessary to investigate the influence of different substrates on the growth and the optical properties of III-nitride optoelectronics such as InGaN based LEDs, for example, widely used sapphire substrates and silicon substrates. GaN-on-silicon suffers from tensile strain, while GaN-on-sapphire exhibits compressive strain. This paper presents a comparison study of InGaN/GaN MQWs grown on a GaN-on-silicon template and a GaN-on-sapphire template in the same growth run under identical conditions. It has been found that the strain status of the GaN underneath has a significant influence on the growth and the optical properties of InGaN/GaN MQWs. Photoluminescence measurements indicate the InGaN/GaN MQWs grown on the GaN-on-Si template exhibit significantly longer wavelength emission than those on the GaN-on-sapphire template. Detailed XRD measurements including reciprocal space mapping measurements confirm that both indium

content and growth rate in the InGaN MQWs on the GaN-on-Si template are enhanced due to the tensile strain of the GaN underneath compared with those on the GaN-on-sapphire template. A detailed study on strain evolution during the InGaN MQWs growth on both templates has been carried out. A qualitative study based on in-situ curvature measurements indicates that a strain change during the growth on the GaN-on-Si template is much more sensitive to a temperature change than that on the GaN-on-Si template. It is worth highlighting that the results provide useful guidance for optimising growth conditions for III-nitrides optoelectronics on silicon.

In this section, both standard GaN-on-sapphire templates and standard GaN-on-Si templates were initially prepared by an MOCVD technique. Both templates were then loaded into a multiple-wafer MOCVD chamber for further growth of InGaN/GaN MQWs simultaneously, meaning that the InGaN/GaN MQWs have been grown under identical conditions. An initial n-GaN layer was grown, followed by the growth of 30 pairs of In<sub>0.05</sub>Ga<sub>0.95</sub>N: 4.2 nm/GaN: 2.5 nm superlattice layers (SLs) as a pre-layer and then 5 periods of InGaN/GaN MQWs as an emitting region. Finally, a 20 nm p-AlGaN acting as an electron blocking layer (EBL) and then a 200nm p-GaN layer were grown. For simplicity, the sample grown on the GaN-on-Si template is denoted as Sample A, while the sample grown on the GaN-on-sapphire template is labelled as Sample B. In order to demonstrate reproducibility, such a comparative growth in the same growth run has been repeated by growing a second set of LEDs on a GaN-on-Si template and on a GaN-on-sapphire template, respectively.

Photoluminescence (PL) and detailed x-ray diffraction (XRD) measurements have been carried out on both samples, demonstrating a significant difference in both structure and optical properties. The InGaN/GaN MQWs on the GaN-on-sapphire exhibit an emission in the blue spectral region, while the InGaN/GaN MQWs on the GaN-on-silicon show a green emission. The detailed XRD measurements have confirmed that the indium content in the MQWs on the GaN-on-silicon is greater than its counterpart on the GaN-on-sapphire. It has also been found that the growth rate of the InGaN MQWs between the two samples is different.

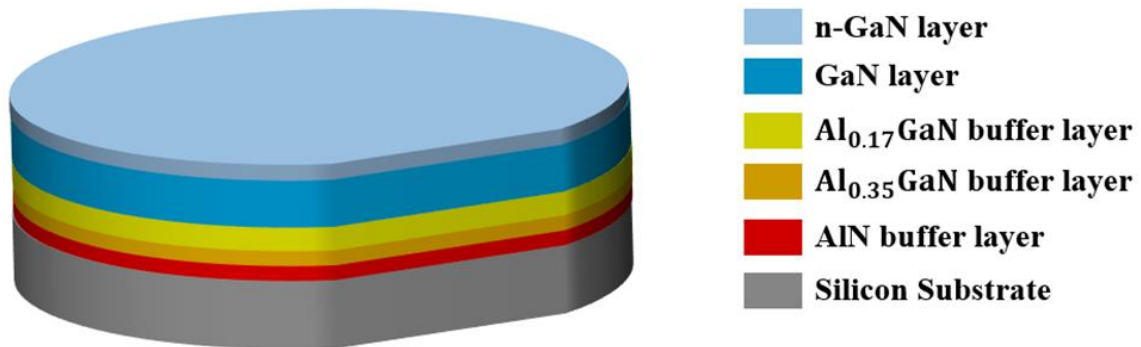
Meanwhile, in-situ monitoring curvature measurements have been conducted, demonstrating that the sample on the GaN-on-Si exhibits significant tensile stress that is

sensitive to a change in growth temperature, while the compressive stress that the sample on the GaN-on-sapphire exhibits is much less sensitive to a growth temperature variation. The stress for both samples has also been studied qualitatively. The results demonstrate that extra attention will have to be paid when the growth conditions which have been optimised for III-nitride optoelectronics on sapphire substrates are transferred to those on silicon substrates.

Two different kinds of GaN templates (i.e., GaN-on-sapphire templates and GaN-on-Si templates) have been prepared by a standard 3×2” closed-coupled showerhead flip-top MOCVD system. For GaN-on-sapphire templates, standard (0001) c-plane sapphire substrates were initially subjected to a high-temperature annealing process in H<sub>2</sub> ambience at 1150 °C, followed by the growth of a 25 nm thick low-temperature nucleation layer at 620°C. Subsequently, the growth temperature was decreased to 1120 °C to carry out the growth of a nominally undoped GaN layer with a thickness of approximately 1.5 μm and finally a 300 nm silicon doped n-GaN layer. The GaN-on-Si templates were grown by using a step-graded AlN/AlGaN buffer approach to overcome a cracking issue which typically takes place during the cooling process [15]-[17],[26]. Standard (111) silicon substrates were initially annealed at 1350°C for 10 minutes in a H<sub>2</sub> ambience to thermally remove any native oxides. Subsequently, the temperature was reduced to 1000 °C and a trimethylaluminum (TMA) pre-flow is then conducted without any NH<sub>3</sub> flowing for 40 s, followed by a thin low-temperature AlN (LT-AlN) layer and then a high-temperature AlN (HT-AlN) layer grown at 1290 °C. The total AlN thickness is around 200 nm. Afterwards, a 260 nm Al<sub>0.35</sub>Ga<sub>0.65</sub>N layer and then a 440 nm Al<sub>0.17</sub>Ga<sub>0.83</sub>N layer were grown as a step-graded AlGaN buffer, which aims to generate extra compressive strain to compensate for a tensile strain that takes place during the cooling process after the subsequent growth of a thick GaN layer. A 1.5 μm GaN layer and then a 300 nm silicon doped n-GaN were grown at 1120 °C. Figure 5.6 schematically illustrates these two kinds of GaN templates in detail.

Subsequently, the two templates were then reloaded into the multiple-wafer MOCVD chamber simultaneously for the further growth of a standard InGaN MQW LED structure in a same run under identical conditions. It is worth highlighting that the growth conditions which have been optimised for InGaN/GaN MQWs grown on sapphire but not on silicon have been chosen to use for such a comparative study.

### a) Template for Sample A



### b) Template for Sample B

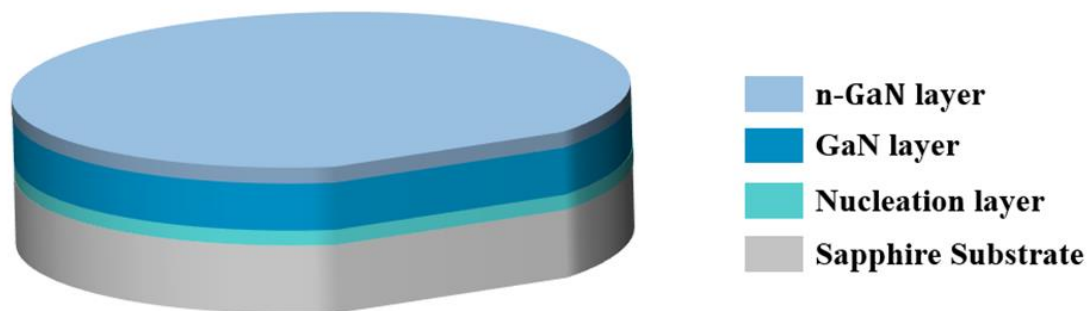


Figure 5.6 Schematic illustration of GaN-on-silicon template (a) and GaN-on-sapphire template (b)

PL measurements have been carried out using a 375 nm diode laser as an excitation source, which is directed by two aluminium mirrors with high reflectivity and then focused on a sample by an ultraviolet (UV) lens. The emission is introduced into a monochromator (Horiba SPEX 500 M) by a pair of lenses and then detected by a thermoelectrically cooled charge-coupled device (CCD) detector.

XRD measurements have been conducted by using a Bruker D8 X-ray diffractometer system, which is typically equipped with a copper (Cu) based anode generating the  $\text{Cu K}\alpha$  X-ray with a wavelength of 1.5418 Å. Along with a commercial Bruker RADS software for fitting and simulation, XRD measurements conducted in a  $\omega$ -2 $\theta$  scan mode have been used to determine indium content and layer thickness in the InGaN/GaN MQW region. Reciprocal space mapping (RSM) measurements have been carried out by performing an asymmetric scan along the (10-15) direction as usual.[12],[27]-[33]

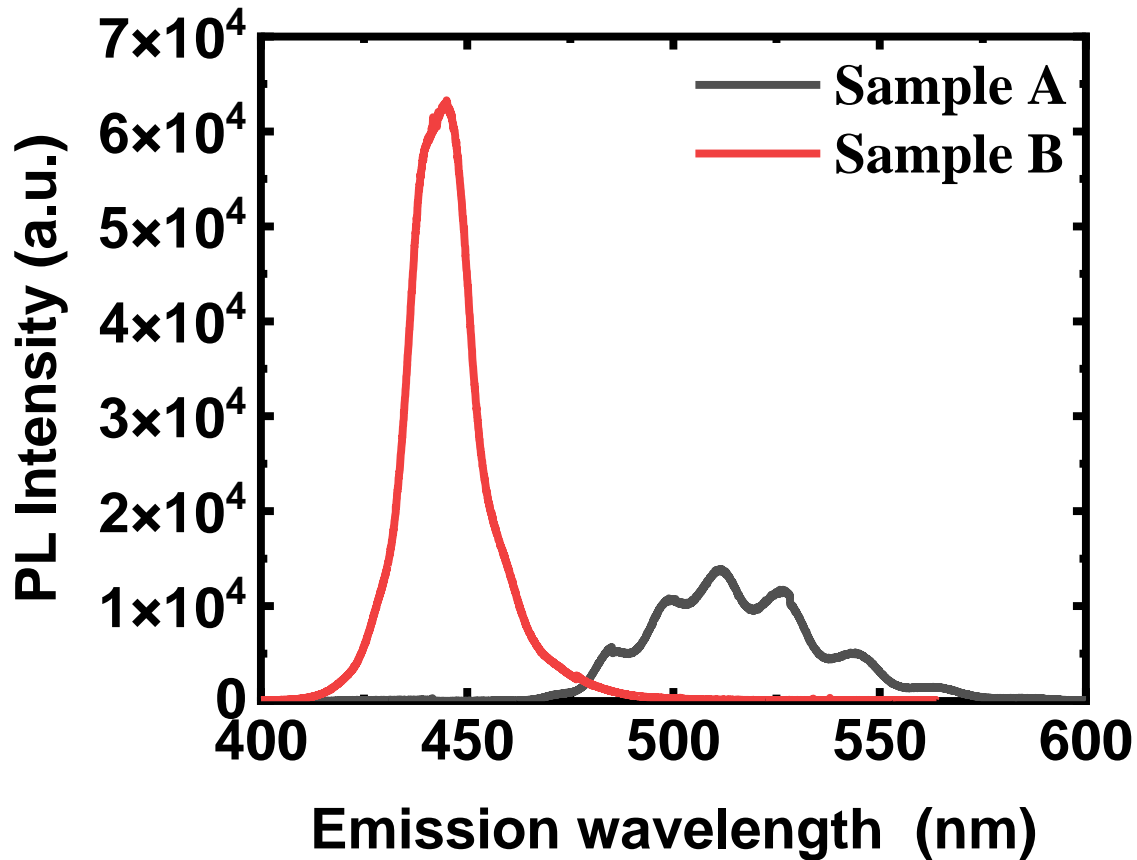


Figure 5.7 Photoluminescence spectra of Sample A and Sample B measured under identical conditions at room temperature

Figure 5.7 shows the PL spectra of both samples measured under identical conditions at room temperature, indicating that Sample B exhibits a strong emission at 444 nm, while a green emission peak centred at 512 nm has been observed for Sample A. Furthermore, the emission peak from sample B is much narrower than that from Sample A, while the emission intensity from sample A is weaker than that from Sample B. As mentioned above, the growth conditions which were chosen for the growth of Sample A and Sample B simultaneously are optimised for InGaN/GaN MQWs grown on sapphire but not for MQWs on silicon. Figure 5.7 clearly demonstrates that there exists a significant difference between Sample A and Sample B in terms of optical characterisation although their InGaN/GaN MQWs were grown in the same run under identical conditions. In order to make a further confirmation, PL measurements were performed on the second set of InGaN LEDs grown on a GaN-on-Si template and on a GaN-on-sapphire template, respectively, which also show very similar results, namely, the emission wavelength from the InGaN/GaN MQW

sample grown on the GaN-on-sapphire template is much shorter than that on the GaN-on-Si template.

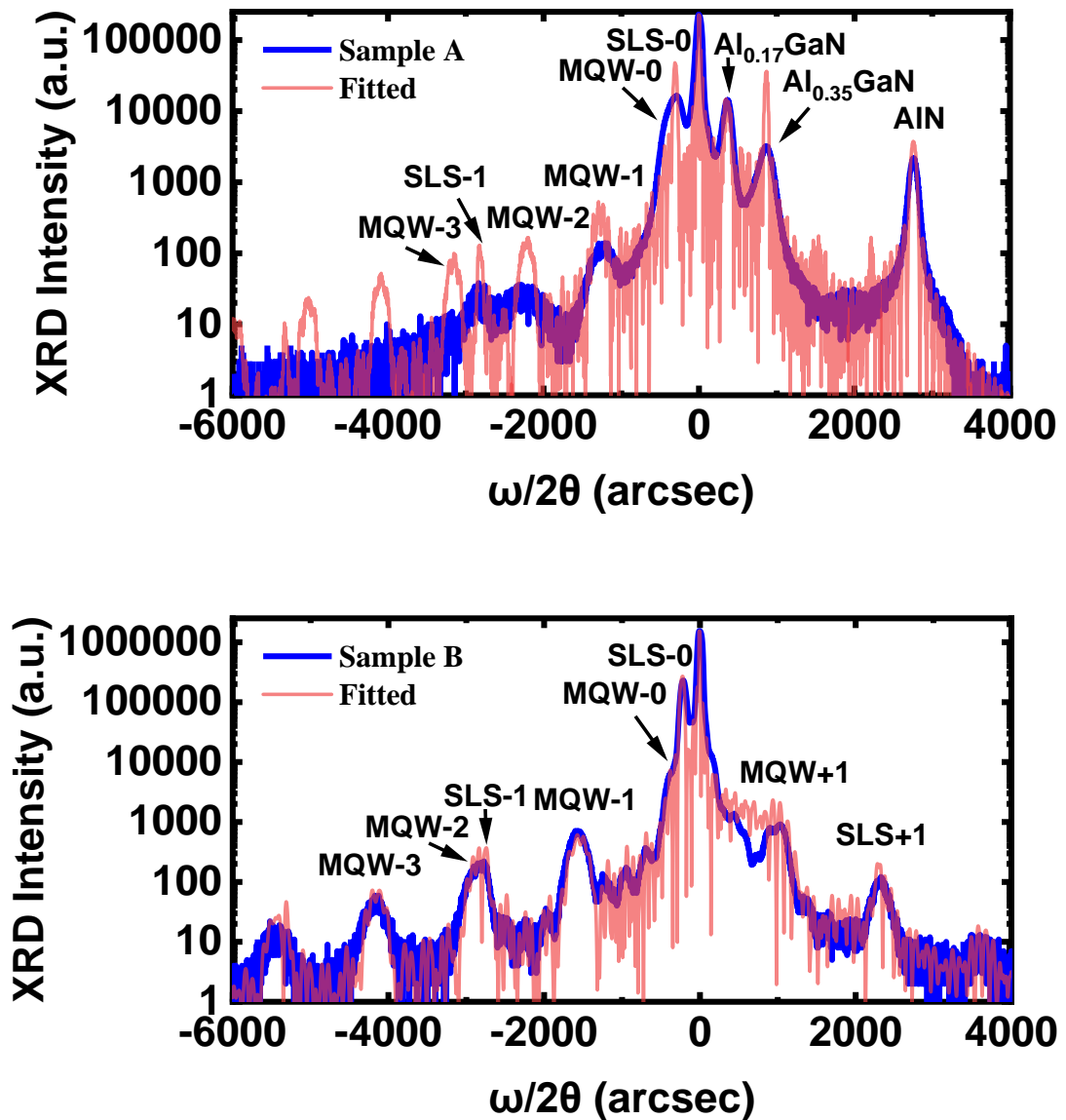


Figure 5.8 XRD spectra measured in a  $\omega$ - $2\theta$  scan mode for Sample A (a) and Sample B (b). In each case, the satellite peaks from the InGaN/GaN SLS as a standard pre-layer and the 5 periods of InGaN/GaN MQWs as an active region have been clearly observed and obtained by using the commercial Bruker RADS software, considering the PL results and the results from our RSM measurements shown in Figure 4.

Figure 5.8 presents the XRD spectra of both Sample A and Sample B measured in a  $\omega$ - $2\theta$  scan mode, where both the satellite peaks from the 30 pairs of the InGaN/GaN SLS as a standard pre-layer and the 5 periods of InGaN/GaN MQWs as an active region have been

clearly observed. These satellite peaks with different orders have also been marked. The indium composition, the InGaN quantum well thickness and the GaN barrier thickness of the InGaN/GaN MQWs in these two samples have been determined by combining the simulation results of the commercial Bruker RADS software and the PL results. Table 5-2 lists the indium content, the InGaN quantum well thickness and the GaN barrier thickness for both Sample A and Sample B. Sample B shows the InGaN quantum wells with 13% indium content and a thickness of 2.3 nm and the GaN barriers with a thickness of 10.5 nm, while the indium content, and the InGaN quantum well thickness and the GaN barrier thickness of Sample A are 21%, 2.6 nm and 15.1 nm, respectively. Similar results have been obtained for the second set of samples. These results mean that InGaN/GaN MQWs grown on a GaN-on-Si template exhibit higher indium content and a faster growth rate than that on a GaN-on-sapphire template. It has been reported that stress can change vapour-solid thermodynamic equilibrium, reducing the solid-phase epitaxial composition towards lattice-matched conditions and thus limiting indium incorporation into GaN [15]. The higher indium content for InGaN/GaN MQWs on the GaN-on-Si template indicates that the tensile strain of the GaN underneath helps enhance the indium incorporation rate into GaN and the growth rate, due to the changes in thermodynamic limitations caused by strain differences in the template layers.[33]

*Table 5-2 Indium content in the InGaN quantum well; InGaN quantum well (QW) thickness and GaN barrier thickness determined from the XRD results and the PL results*

<b>Sample No.</b>	<b>Emission wavelength (nm)</b>	<b>Indium Content (x)</b>	<b>InGaN well thickness (nm)</b>	<b>GaN barrier thickness (nm)</b>
Sample A	512	0.21	2.6	15.1
Sample B	444	0.13	2.3	10.5

Please note that a detailed RSM has also been performed along with the (10-15) orientation [12][34] on both samples to determine the strain of the InGaN/GaN MQWs in both cases, one of the important parameters for our simulation to accurately determine the indium content and the InGaN quantum well thickness. Figure 5.9 shows the RSM results of Sample A and Sample B measured in an asymmetric diffraction scan along with the (10-



15) orientation, demonstrating that the InGaN/GaN MQWs grown on the GaN-on-sapphire template are fully strained since all the satellite peaks from the InGaN/GaN MQW align with the vertical line which passes through the GaN peak, while it is not the case for Sample A. For the InGaN/GaN MQWs on the GaN-on-Si template (i.e., Sample A), a clear strain relaxation has been observed on the InGaN/GaN MQWs since the satellite peaks from the InGaN/GaN MQWs inclines towards the relaxing direction. Detailed relaxation can be calculated by using Equation 1 given below: [29],[30]

$$R = (a_{measured}^{InGaN} - a_{measured}^{GaN}) / (a_{reference}^{InGaN} - a_{reference}^{GaN}) \quad (5.8)$$

where  $a_{measured}^{InGaN}$  and  $a_{measured}^{GaN}$  are the measured in-plane lattice constants, respectively; and  $a_{reference}^{InGaN}$  and  $a_{reference}^{GaN}$  are the in-plane lattice constants in a fully relaxed situation, respectively.

Based on Equation (5.8) and the RSM results, 5% relaxation has been determined for Sample A and Figure 5.9 has been used for our XRD simulation/fitting discussed above.

The strain evolution of Sample A and Sample B during the growth process has been investigated by using a commercial Laytec EpiCurve TT system which is equipped with the MOCVD system. Two parallel laser beams with a wavelength of 635 nm are introduced into a measured wafer through the optical port of the MOCVD and are then reflected back through the optical port. The curvature of the wafer can be determined from the distance between the two reflected laser beams. Figure 5.10 shows the results of the in-situ curvature measurements during the growth of Sample A and Sample B. A positive value indicates that a wafer is in a concave shape, meaning that the wafer is under tensile stress, while a negative value represents a convex shape meaning that the wafer is under compressive stress.

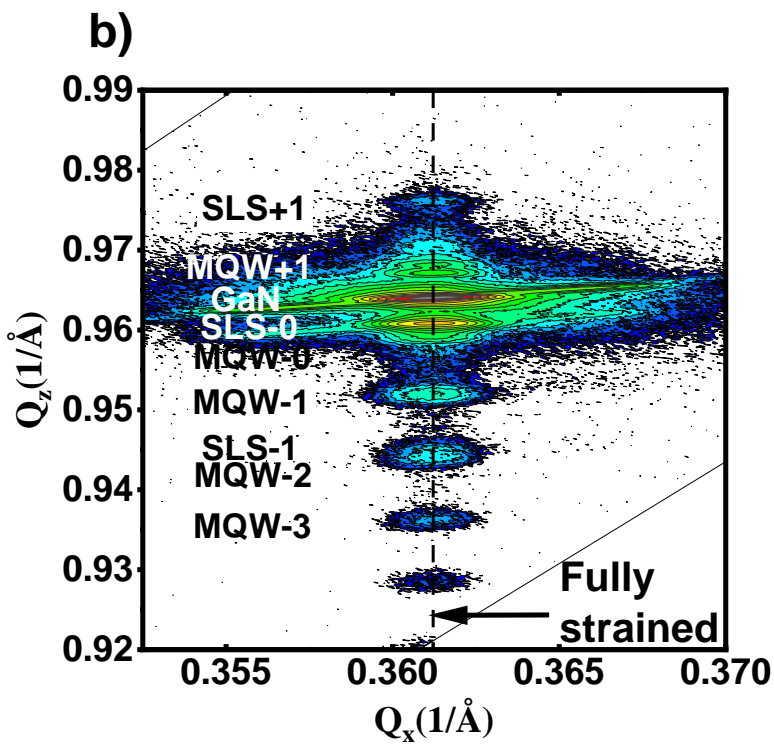
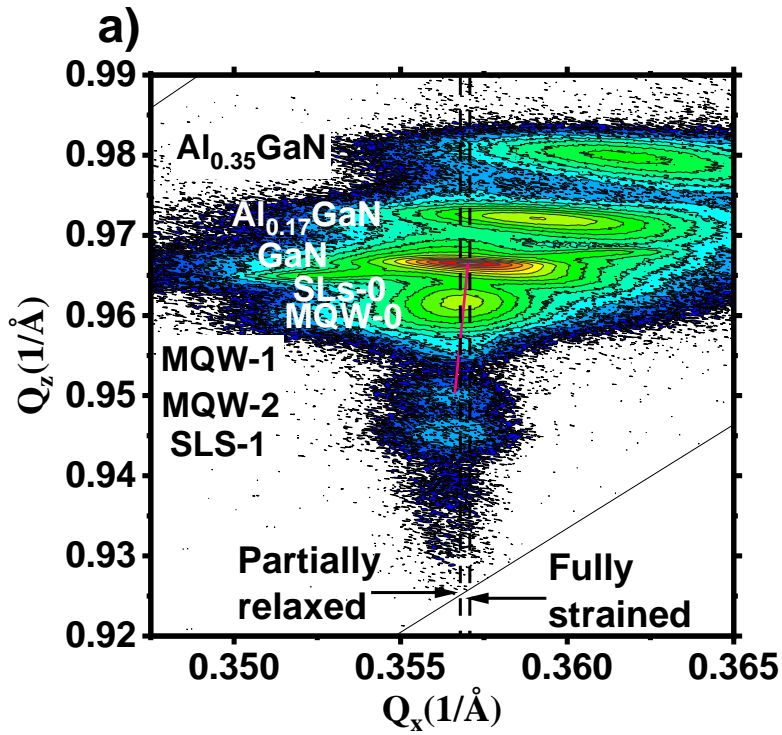


Figure 5.9 RSM measured along with the asymmetric (10–15) diffraction for Sample A (a) and Sample B (b).

Figure 5.10 shows that Sample A exhibits positive curvature values before and after the growth process, indicating that the GaN on the silicon substrate is under tensile stress at room temperature. In contrast, Sample B exhibits a little bit convex shape, which indicates that the GaN on the sapphire substrate is under compressive stress at room temperature. Furthermore, during the growth process of the InGaN/GaN MQW, Sample B is constantly under compressive stress, while Sample A experiences a variation in tensile stress which is due to a growth temperature change between the InGaN quantum wells and the GaN barriers. This means that the strain variation that occurred to Sample B is much less sensitive to a growth temperature change compared to Sample A.

The Stoney formula is given below [35],[36] is further used to estimate the stress (labelled as  $\sigma$ ) of the GaN on silicon or sapphire and the stress of Sample A and Sample B after the InGaN MQWs growth,

$$\sigma = \frac{\kappa E_s t_s^2}{6t_f(1 - \nu_s)} \quad (5.9)$$

where  $t_f$  and  $t_s$  represent the thickness of a film on a substrate and the thickness of the substrate, respectively;  $E_s$  and  $\nu_s$  are Young's modulus; and the Poisson's ratio, respectively. The thickness  $t_s$  of the silicon substrate and the sapphire substrates are 430  $\mu\text{m}$  and 330  $\mu\text{m}$ , respectively, which are about 100 times thicker than the epilayer thickness of either Sample A or Sample B. Based on Equation (5.9), the stress that the GaN layers of Sample A and Sample B suffer is -0.34 GPa and 0.35 GPa, respectively. Their stress during the growth of InGaN/GaN MQWs for Sample A and Sample B is -0.35 GPa and 0.17 GPa, respectively.

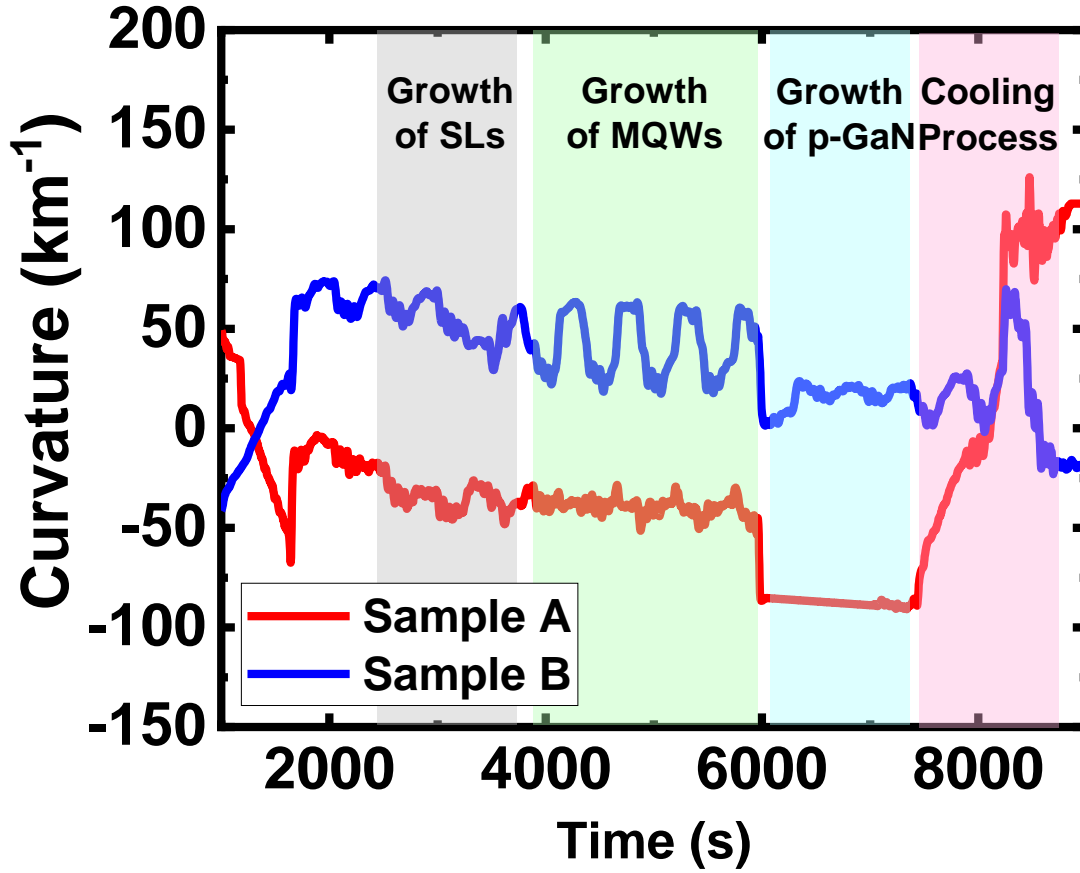


Figure 5.10 In-situ curvature measurements during the growth process for Sample A and Sample B.

The thermal stress (labelled as  $\sigma_{th}$ ), which are generated during a cooling process, can be estimated by Equation (5.10) provided below,[34],[37]

$$\sigma_{th} = \frac{E_{film}}{1 - \nu_{film}} (\alpha_1 - \alpha_2)(T_1 - T_2) \quad (5.10)$$

where  $T_1$  and  $T_2$  are the growth temperature and room temperature, respectively;  $\alpha_1$  and  $\alpha_2$  are the thermal expansion coefficients of the substrate and the epilayer, respectively.  $E_{film}$  and  $\nu_{film}$  are Young's modulus and the Poisson ratio of the epilayer, respectively. Based on Equation (5.10), the thermal stress of Sample A and Sample B is -0.78 GPa and 0.55 GPa, respectively, which are consistent with the stress obtained from the in-situ curvature measurements.

In summary, a systematic study on the influence of different substrates on the growth and the optical properties of InGaN/GaN MQWs has been carried out by simultaneously

growing InGaN/GaN MQWs on a GaN-on-Si template and a GaN-on-sapphire template in the same growth run. Our results demonstrate a major difference between them: the MQWs grown on the GaN-on-Si template show significantly longer wavelength emission than those on the GaN-on-sapphire template. Detailed XRD measurements confirm that the MQWs grown on the GaN-on-Si template exhibit an enhancement in both indium content and growth rate than those on the GaN-on-sapphire. These major differences can be attributed to the changes in thermodynamic limitations, caused by the tensile strain that the GaN-on-Si suffers. In-situ curvature measurements during the MQWs growth suggest that more attention will have to be paid to a temperature change during growth on the GaN-on-Si template than on the GaN-on-sapphire template, as the strain for the growth on the GaN-on-Si template is much more sensitive to a temperature change compared to the GaN-on-sapphire case.

### **5.3 Conclusion**

In this chapter, a GaN/AlGaN HEMT and an InGaN/GaN MQWs are grown on crack-free GaN-on-Si wafers. As a result of a high crystal quality AlN buffer layer, high-quality GaN HEMTs on silicon with mobility of  $1600 \text{ cm}^2 \text{ V}^{-1} \text{ S}^{-1}$  and a current density of  $290 \text{ mA/mm}$  for  $120 \text{ }\mu\text{m}$ -gate HEMTs have been achieved. As for the MQWs, a GaN-on-Si template and a GaN-on-sapphire substrate are prepared and grown in the same growth run. The growth and the optical properties differences between these substrates are investigated. Specifically, the emission wavelength of the MQWs grown on the GaN-on-Si template is significantly longer than that on the GaN-on-sapphire template and the detailed XRD measurements demonstrate an enhancement in indium content in the MQWs grown on the GaN-on-Si template. Moreover, the in-situ curvature measurements during growth indicate that the temperature effect on the strain during the growth of MQWs on GaN-on-Si is significantly more significant than that on GaN-on-sapphire.

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# Chapter 6 Growth of Integrated $\mu$ LEDs/HEMTs

## Microdisplay on a Single Chip

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In this chapter, a direct epitaxial approach is introduced, discussed and optimized to grow integrated micro-LEDs/HEMTs ( $\mu$ LEDs/HEMTs) Microdisplay on a single chip. The selective area overgrowth pattern of GaN is investigated and a selective area overgrown  $\mu$ LED is demonstrated in corresponding sections. After that, an integrated  $\mu$ LEDs/HEMTs microdisplay is achieved and its properties are exhibited at the end of this chapter. All selective area overgrown structures are grown by a metal-organic chemical vapour deposition (MOCVD), and their surface, emission wavelength, current-voltage ( $I$ - $V$ ) curve and crystal quality are measured using optical microscopy, scanning electron microscopy (SEM), electroluminescence (EL) system, two-channel Keithley 2612B source meter (Cleveland, OH, USA) and the Bruker X-ray diffractometer (XRD).

### 6.1 Introduction

A microdisplay, defined as an ultrasmall screen with a diagonal  $\leq 1$  inch, is the critical component of a wide variety of next-generation display systems, including augmented reality (AR)/virtual reality (VR) systems, helmet-mounted displays (HMD), and head-up displays (HUD), which are typically used in small spaces or in close proximity to the eye. As a consequence, high resolution, high brightness (in order to achieve an adequate ambient contrast ratio (ACR)), and a tiny form factor are necessary. However, owing to inherent constraints, contemporary liquid crystals on silicon or digital light processor-based projection microdisplays cannot achieve these criteria. In comparison, it is anticipated that a microdisplay based on III-nitride inorganic semiconductor micro-LED ( $\mu$ LED) technology would significantly overcome these constraints.

In comparison to an organic LED (OLED), an inorganic micro-LED has the potential to provide high brightness without sacrificing reliability or longevity.[1],[2] By and large, III-nitride LEDs outperform OLEDs in terms of illuminance and ACR.[1]-[4] Additionally, OLEDs must be strongly driven with a high injection current to provide a brightness many

times that is needed by the colour filter [4]. As a result, a micro-LED microdisplay is an optimal solution [4]-[12].

Essentially, a micro-LED based microdisplay is composed of  $\mu$ LED arrays and electronic components that electrically operate individual  $\mu$ LEDs. At the moment, two distinct technologies are employed to combine  $\mu$ LED arrays with electrical components. The first way is referred to as transfer printing, which is based on massive transfer technology, in which millions of  $\mu$ LEDs are moved from a wafer to a transistor backplane, requiring very high precision of roughly 1  $\mu$ m and substantial time. As a consequence of the poor yield [13]-[16], this technique is unfeasible for manufacturing a microdisplay, particularly for AR/VR applications. The second solution is based on flip-chip bonding, in which  $\mu$ LEDs and a CMOS (used to electrically control individual  $\mu$ LEDs) are manufactured separately and then heterogeneously wafer-bonded together [17]. However, it is worth noting that the second strategy faces two significant obstacles. The first difficulty arises from an assembly problem. Due to the fact that individually addressable  $\mu$ LEDs must be driven by CMOS circuits, a heterogeneous integration approach is used to combine  $\mu$ LEDs and electrically driving components [2],[8]-[13]. In this situation, there is still a concern with the precision of the alignment between the  $\mu$ LEDs and the CMOS, hence reducing the transfer yield and rising production costs. The second difficulty arises from a loss in the optical performance of  $\mu$ LEDs, which are manufactured using photolithography technology and subsequent dry-etching operations [2]-[11]. During such dry-etching and subsequent procedures, considerable damage is produced, resulting in a significant loss of the optical performance of  $\mu$ LEDs [18]-[19]. Additionally, by shrinking the size of  $\mu$ LEDs, the severity of the problem is increased [18]-[22]. Although an additional passivation step using an atomic layer deposition (ALD) technology is used [22],[23], optical performance is only partially recovered owing to permanent damage induced by dry-etching operations. As a result, this method of heterogeneous integration for the production of a microdisplay is far from perfect.

We think that epitaxial integration of  $\mu$ LEDs and high electron mobility transistors (HEMTs) may be the ultimate method for microdisplay fabrication. We recently established an epitaxial growth technique for the production of  $\mu$ LEDs on a pre-patterned template, in which no dry-etching procedures are used, hence avoiding any etching damage [24]-[26]. As a consequence, we have created ultracompact  $\mu$ LEDs with an unprecedented external quantum efficiency (EQE) [24],[25]. In this study, we suggest a paradigm in which,

rather than a single GaN template, a pre-patterned HEMT structure is employed as the template for growing  $\mu$ LEDs. This project intends to accomplish epitaxial integration of  $\mu$ LEDs and HEMTs for a microdisplay, therefore resolving all basic challenges that cannot be resolved using either "pick-and-place" or "flip-chip bonding technology." We have shown an  $8 \times 8$  micro-LED microdisplay in this study, where each  $\mu$ LED is electrically powered by a separate HEMT.

## **6.2 Experiment and Results discussion**

### **6.2.1 Growth of GaN on Selective area overgrowth pattern**

Effects of different growth conditions on the growth patterns during selective area overgrowth are investigated using the example of GaN overgrowth on  $\text{SiO}_2$  masked GaN templates in this work. Specifically, those conditions including growth window size, pressure, source flow rate and temperature are varied and their effects are investigated. Furthermore, the growth results are observed and compared by the Scanning electron microscopy (SEM) results. With the help of this investigation, proper basic growth conditions are determined for the further selective area overgrowth (SAG) of GaN-based devices.

In order to achieve an integrated  $\mu$ LEDs/HEMTs Microdisplay structure on a single chip by a direct epitaxial approach, selective area overgrowth would be a very important and fundamental step.

To properly investigate this issue, groups of GaN templates are prepared with the exact growth conditions and then fabricated with similar steps to achieve the required  $\text{SiO}_2$  masks respectively. Specifically, all the templates are grown by MOCVD and have a structure as shown in Figure 6.1a. On the top of the substrate, a 200nm-thick AlN buffer layer is grown at high temperature and then a step graded AlGaIn buffer layer is deposited with a thickness of 500nm. After that, a  $1 \mu\text{m}$  GaN layer is grown on top and waiting for the next fabrication and overgrowth.

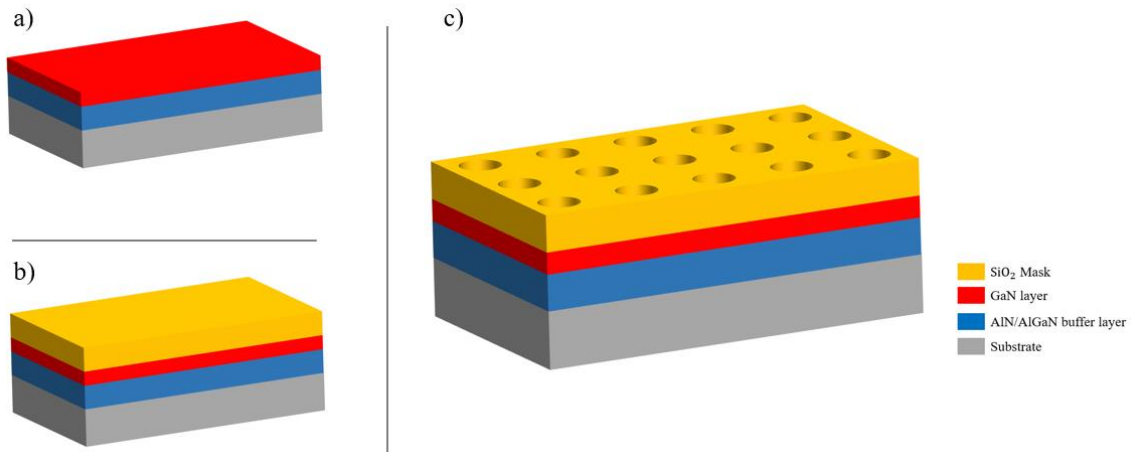


Figure 6.1 Structure of used templates a) MOCVD growth, b)  $\text{SiO}_2$  deposition and c) After Mask aligning and ICP etching.

Figure 6.1b shows the grown templates deposited with a  $\text{SiO}_2$  layer by PECVD. This  $\text{SiO}_2$  is 500nm thick and will then be patterned and then be etched by inductively coupled plasma(ICP). As shown in Figure 6.2, the used masks consist of 6 different patterns. For pattern A shown in Figure 6.2a, the growth window is a circle with a  $60\ \mu\text{m}$  diameter and the distance between 2 circles is  $20\ \mu\text{m}$ . And for pattern B in Figure 6.2b, the mask consists of  $40\text{-}\mu\text{m}$ -diameter circles with a  $20\text{-}\mu\text{m}$  distance. Furthermore, pattern C and pattern F share the same growth window shape and diameter of  $20\ \mu\text{m}$  but with different distances of  $20\ \mu\text{m}$  and  $10\ \mu\text{m}$  respectively in between. Additionally, this  $10\ \mu\text{m}$  distance is also used in patterns D and E but with different window diameters of  $5\ \mu\text{m}$  and  $10\ \mu\text{m}$  separately.

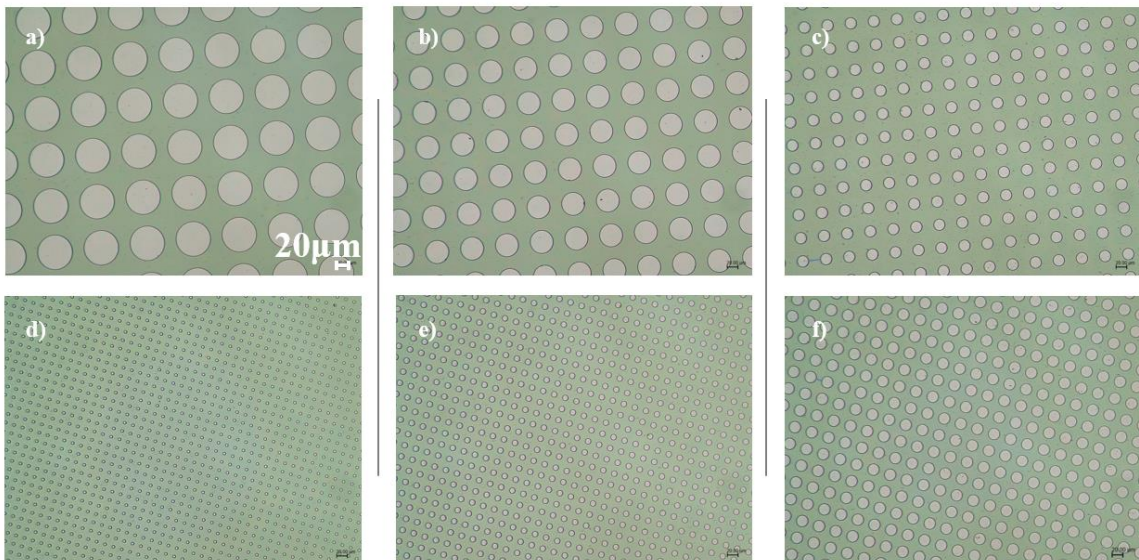


Figure 6.2 Optical Microscopy Pictures of different Masks :a)  $60\ \mu\text{m}$  pattern with  $20\ \mu\text{m}$  interpatch distance; b)  $40\ \mu\text{m}$  pattern with  $20\ \mu\text{m}$  interpatch distance; c)  $20\ \mu\text{m}$  pattern with  $20\ \mu\text{m}$  interpatch distance; d)  $5\ \mu\text{m}$  pattern with  $10\ \mu\text{m}$  interpatch distance; e)  $10\ \mu\text{m}$  pattern with  $10\ \mu\text{m}$  interpatch distance; f)  $20\ \mu\text{m}$  pattern with  $10\ \mu\text{m}$  interpatch distance.

After the template fabrication, there is still one more important step before overgrowth, which is template cleaning. These cleaning steps are similar to the steps mentioned in chapter 4.2.1 above. However, instead of using the Hydrofluoric acid (HF) for the Si cleaning, the Photo-Enhanced Chemical Etching (PEC) with Potassium hydroxide (KOH) is used here to clean the top GaN surface.

1. Immerse the template in n-butyl acetate, acetone, and isopropyl alcohol (IPA) using an ultrasonic bath for 5 mins each.
2. Rinse template under running deionized water (DI water) to eliminate any remaining solvent for 5 mins.
3. Immerse the template in 20% Potassium hydroxide (KOH), and then put the solution under a Xe lamp for 40 mins.
4. Rinse template under running deionized water (DI water) to eliminate any remaining solvent for 5 mins.
5. Immerse the template in 40% Hydrogen chloride (HCl) for 5 mins.
6. Rinse template under running deionized water (DI water) again to eliminate any remaining solvent for 5 mins.
7. To eliminate template stains, blow wafers with dry nitrogen and bake it at 100 °C for 5 minutes to remove absorbed moisture.

With all the steps above, the templates are well prepared for the upcoming overgrowth steps.

After cleaning these templates, the experimental overgrowth conditions can be divided into 5 groups and each of these groups serves as the experimental group itself and the control group for the next one at the same time. Consequently, with these results, we are able to draw various conclusions from 5 different aspects. All the growth conditions from these 5 groups can be found in Table 6-1 below. Meanwhile, in order to observe the growth modes of the templates, all the overgrown GaN layers are more than 1  $\mu\text{m}$  thick to ensure that they can escape from the  $\text{SiO}_2$  mask confinement.

Table 6-1 Overgrowth conditions of all different experiment groups.

<b>Sample Group</b>	<b>Pattern Type</b>	<b>Temperature (°C)</b>	<b>Pressure (mbar)</b>	<b>V/III sources flow rate (sccm)</b>
Group A	Pattern A/B/C	1280	233	2200/65
Group B	Pattern D/E/F	1280	233	2200/65
Group C	Pattern D/E/F	1280	400	2200/65
Group D	Pattern D/E/F	1280	400	1500/40
Group E	Pattern D/E/F	1180	400	1500/40

Specifically, as shown in Table 6-1 the 5 groups shown in Table 6-1, the comparison of Group A and Group B is talking about the influence of the growth pattern, while Group A and Group B are sharing the same growth conditions but using different growth patterns or templates masks. All those growth patterns mentioned in Table 6-1 can refer to Figure 6.2, e.g. pattern A refers to Figure 6.2a, pattern B refers to Figure 6.2b and so on.

In addition to that, the differences from Group B to Group E are focused on condition variance during growth. In particular, the growth conditions of Group C are based on those of Group B but with an increase in the growing pressure from 233 mbar to 400 mbar. Next, the difference between Group C and Group D is the V/III sources flow rate. It is notable that even though the flow rates of the V/III sources are dropped, their V/III ratio is keeping similar. Last but not the least, the growth temperature of Group E is much lower than that of Group D.

With the help of those 5 groups of different conditions and therefore 4 couples of result comparisons, Figure 6.3 ~ Figure 6.6 are demonstrated. Each of those figures shows a significant factor that can change the final shape of the overgrown GaN structure and further influence the device structure after. These factors can be concluded as growth pattern, growth pressure, sources flowrate and growth temperature.



a) Effect of growth pattern

Figure 6.3 depicts the SEM images of Group A and Group B's ultimate growth outcomes. As can be referred to in Figure 6.2, the shapes of all the growth patterns from A to F are all circles but with different diameters, which are 60  $\mu\text{m}$ , 40  $\mu\text{m}$ , 20  $\mu\text{m}$ , 5  $\mu\text{m}$ , 10  $\mu\text{m}$ , and 20  $\mu\text{m}$  respectively. Additionally, the distances between the two circles are also different for the 6 patterns. For Pattern A to C, this distance is 20  $\mu\text{m}$  while that of Pattern D to F is 10  $\mu\text{m}$ .

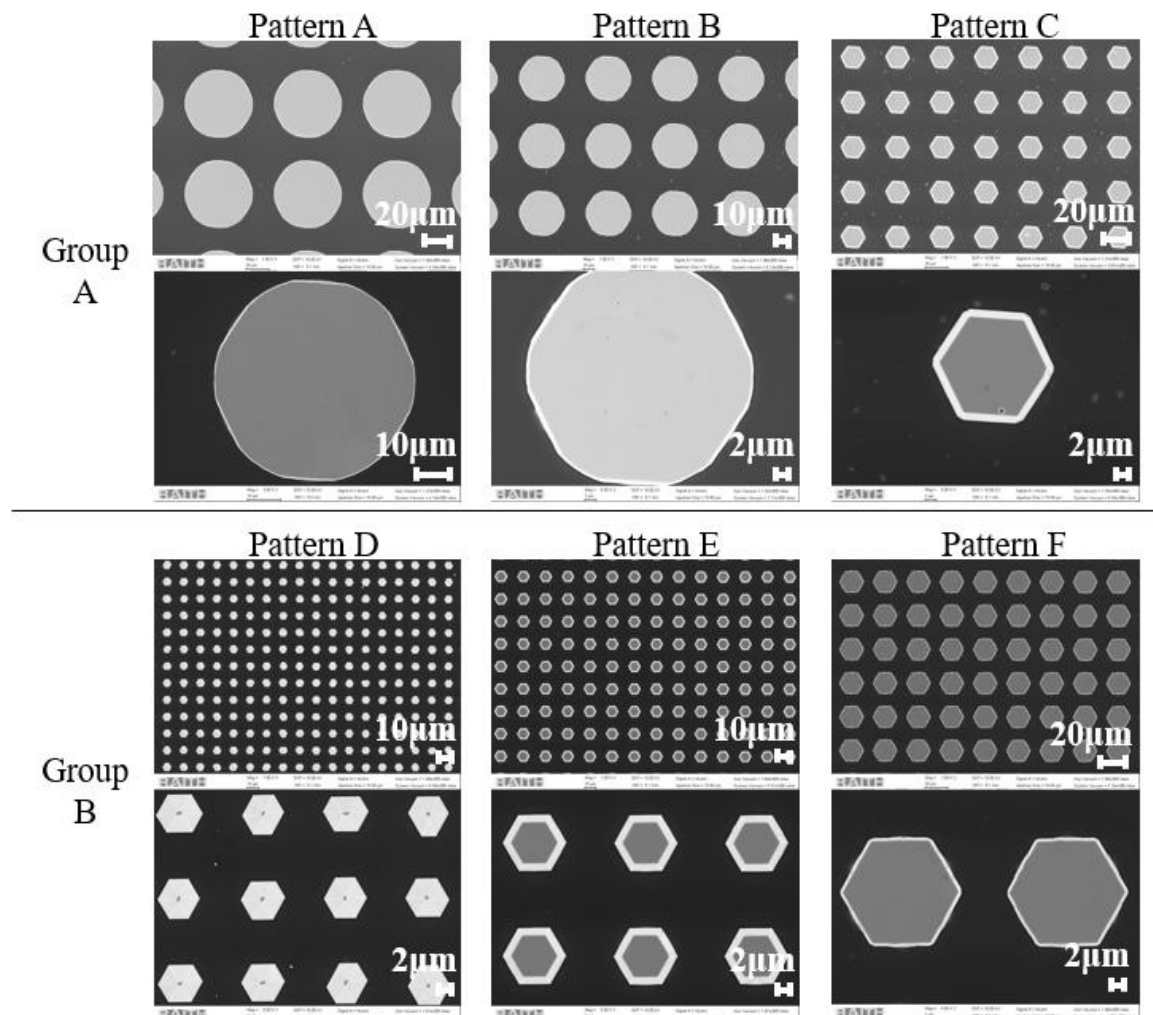


Figure 6.3 Top view SEM pictures of Sample Group A and B. They share identical growth conditions but with different pattern sizes and interpatch distances. Pattern A has a 60- $\mu\text{m}$  diameter with 20  $\mu\text{m}$  interpatch distance. Pattern B has a 40- $\mu\text{m}$  diameter with 20  $\mu\text{m}$  interpatch distance. Pattern C has a 20- $\mu\text{m}$  diameter with 20  $\mu\text{m}$  interpatch distance. Pattern D has a 5- $\mu\text{m}$  diameter with 10  $\mu\text{m}$  interpatch distance. Pattern E has a 10- $\mu\text{m}$  pattern with 10  $\mu\text{m}$  interpatch distance. Pattern F has a 20- $\mu\text{m}$  diameter with 10  $\mu\text{m}$  interpatch distance.

From the overgrown GaN shape of Pattern A to F, it can be found that once the growth window diameter is over 20  $\mu\text{m}$ , the overgrown GaN will be close to a cylinder. Additionally, when the window diameter is between 10  $\mu\text{m}$  to 20  $\mu\text{m}$ , the shape of GaN

will be a hexagonal prism. With the decrease in the window diameter, the area difference between the top surface and the bottom surface of this hexagonal prism is increasing. Furthermore, when the growth window downsizes to a 5  $\mu\text{m}$  diameter, the top surface of the hexagonal prism shrinks to a point and makes the final GaN shape a hexagonal pyramid. This cylinder to hexagonal prism to hexagonal pyramid transformation can be explained by a weakening in GaN lateral growth accompanying the growth window downsizing.

Apart from that, the form of the GaN in Pattern C is obviously different from that of Pattern F, which has the same window size but different window spacing. Specifically, the top surface/bottom surface area ratio of the GaN hexagonal prism in Pattern F is less than that of the GaN hexagonal prism in Pattern C, indicating that decreasing the window distance results in increased GaN lateral growth strength. This phenomenon is reasonable as the growth area/general area ratio can be increased by shortening the distance between the growth windows. Alternatively, as the Ga atoms have a longer diffusion distance on the  $\text{SiO}_2$  surface than on the GaN surface during growing, it is easier to find the pattern with a shorter window distance has better confinement of the free Ga atoms and therefore gets a stronger lateral growth.

Another critical comparison is between Patterns B and F, which both have the same growth area/general area ratio but vary in their GaN forms. That is, regardless of the growth area/general area ratio, the effect of the growth window size and distance may dominate the growth mode. In addition to that, another conclusion that can be drawn using Pattern C as a control group is that the effect of the growth window radius is greater than the influence of the growth window distance.

#### b) Effect of growth pressure

Patterns D, E, and notably F are chosen as the experimental patterns for the following growth groups based on the data above. The SEM images of Group B and Group C's overgrowth are shown in Figure 6.4. Group B has an overgrowth pressure of 233 mbar, whereas Group C has an overgrowth pressure of 400 mbar. As per the data, there is no statistically significant variation in the shape and size of GaN in Pattern D and E between Group B and Group C. However, in Pattern F, it is seen that the form of the GaN following overgrowth in Group C is more round than in Group B, despite the fact that the diameters of the overgrown GaN in both groups are similar. This would lead to a conclusion that the

influence of pressure change during growth is very small even in the 20  $\mu\text{m}$  diameter sized growth window and could even be neglectable for the smaller growth window.

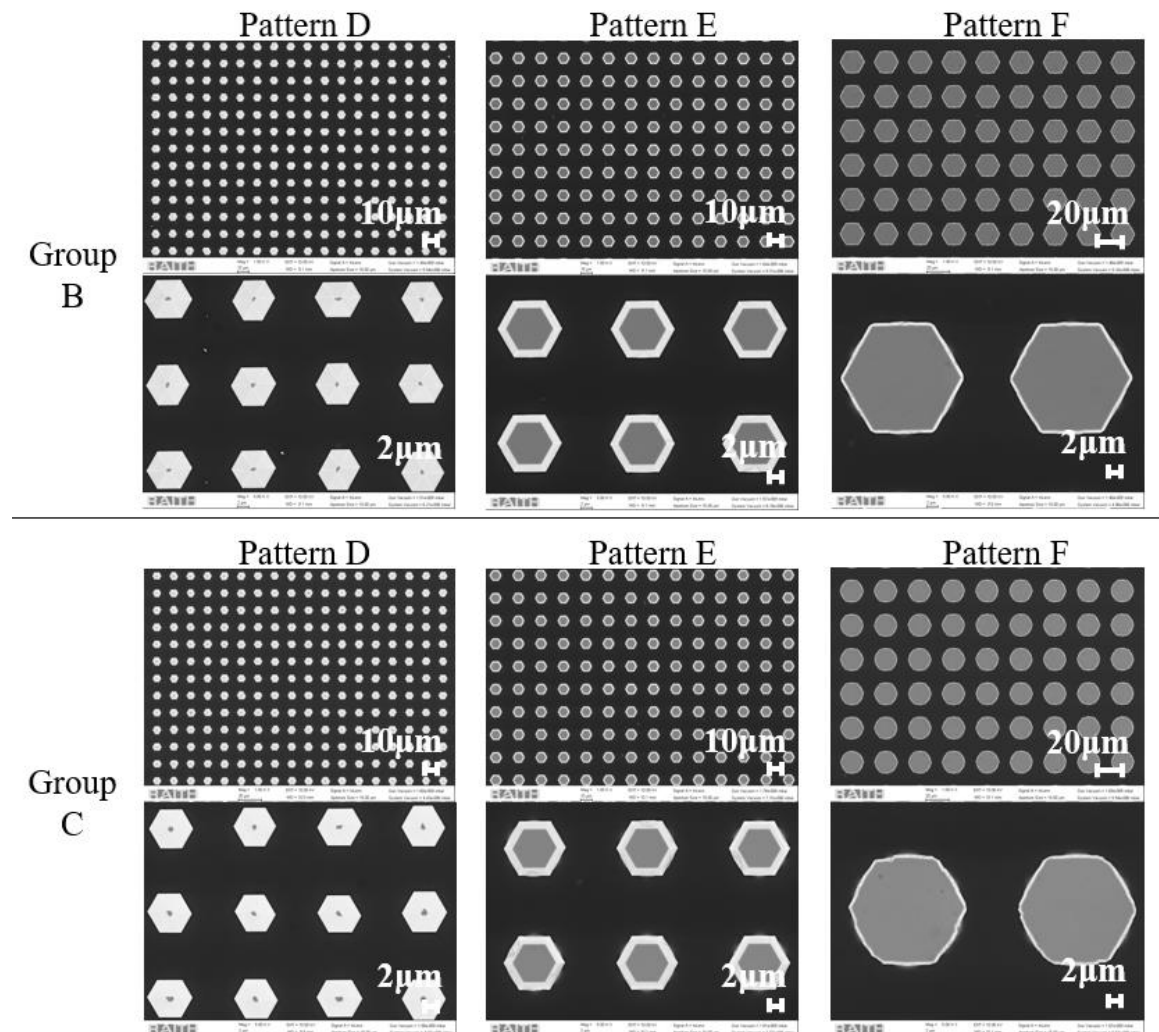


Figure 6.4 Top view SEM pictures of sample Group B and C. They share the identical growth area pattern and other growth conditions but Group B was grown under 233 mbar while Group C was grown under 400 mbar. Among those groups, Pattern D has a 5- $\mu\text{m}$  diameter with 10  $\mu\text{m}$  interpatch distance. Pattern E has a 10- $\mu\text{m}$  pattern with 10  $\mu\text{m}$  interpatch distance. Pattern F has a 20- $\mu\text{m}$  diameter with 10  $\mu\text{m}$  interpatch distance.

### c) Effect of sources flowrate

Based on the results above, the growth pressure is determined as 400 mbar for the remaining groups. Furthermore, the next change between Group C and Group D is about the V/III sources flow rates, which are dropped from 2200/65 sccm to 1500/40. The V/III ratio remains similar to eliminating its influence. It is notable that the sources flow rates and the ratio of V/III sources will influence the GaN growth not only in their shape but also in the crystal quality and so on. So this section here is a brief discussion about these conditions that need further optimisation for exact growth requirements. As shown in Figure 6.5, the

results indicate that although the overgrowth GaN diameters are decreased in all three patterns, the shape of the GaN changes significantly only in Patterns E and F. To be more precise, for pattern E, the GaN structure in Group D may retain the fundamental hexagonal prism shape but with a more thin and blurred border. However, in the case of pattern F, this border is too fractured to reveal the overgrowth GaN pillar's shape. This unexpected deformation of GaN at the pattern boundary could be because of a lack of sources at the very beginning of the overgrowth since all the overgrown GaN pillars are much higher than the SiO<sub>2</sub> mask and the lateral growth can not recover afterwards. However, the narrower boundary in Pattern E of Group D indicates this low-flow-rate growth could benefit the lateral growth during the later growing period.

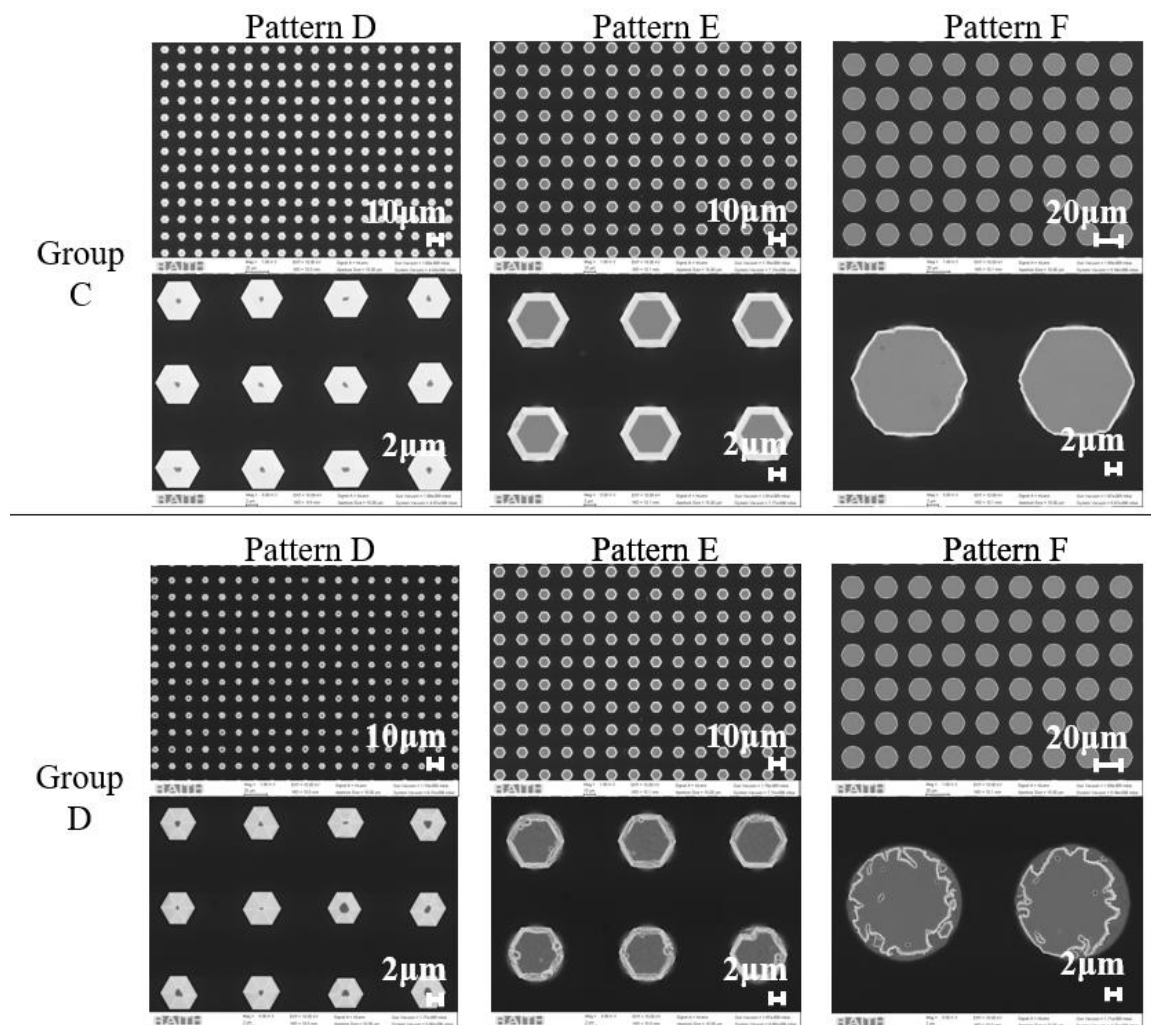


Figure 6.5 Top view SEM pictures of sample Group C and D. They share the identical growth area pattern and other growth conditions but Group C was grown with 2200 sccm NH<sub>3</sub> and 65 sccm TMGa while Group D was grown with 1500 sccm NH<sub>3</sub> and 40 sccm TMGa. Among those groups, Pattern D has a 5- $\mu\text{m}$  diameter with 10  $\mu\text{m}$  interpatch distance. Pattern E has a 10- $\mu\text{m}$  pattern with 10  $\mu\text{m}$  interpatch distance. Pattern F has a 20- $\mu\text{m}$  diameter with 10  $\mu\text{m}$  interpatch distance.

#### d) Effect of temperature

Last but not the least, Group D and Group E are grown to investigate the influence of growth temperature on the overgrown GaN shape. Most of the growth conditions in Group E are the same as those in Group D apart from the growth temperature (1280°C for Group D and 1180°C for Group E).

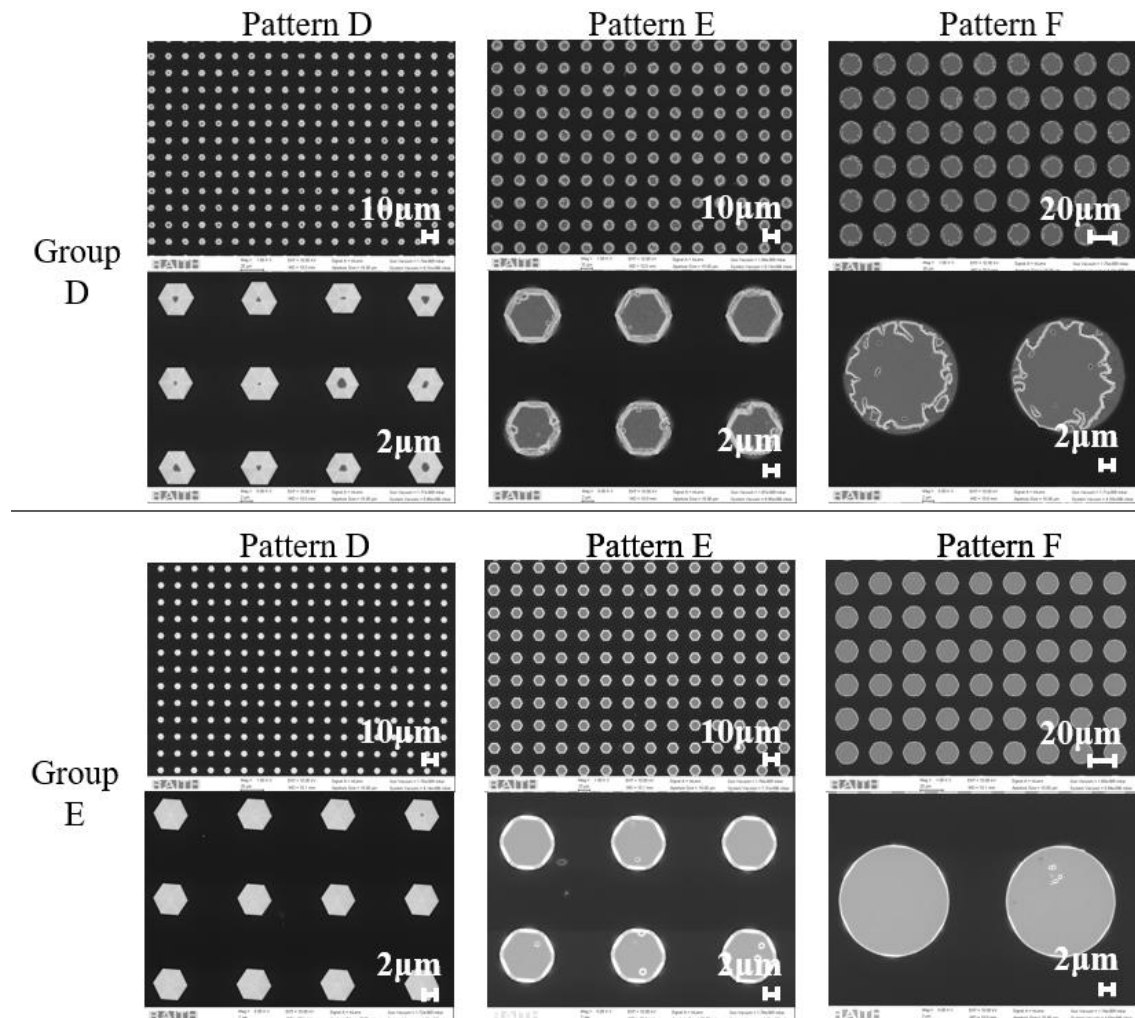


Figure 6.6 Top view SEM pictures of sample Group D and E. They share the identical growth area pattern and other growth conditions but Group D was grown under 1280 °C while Group C was grown under 1180 °C. Among those groups, Pattern D has a 5- $\mu\text{m}$  diameter with 10  $\mu\text{m}$  interpatch distance. Pattern E has a 10- $\mu\text{m}$  pattern with 10  $\mu\text{m}$  interpatch distance. Pattern F has a 20- $\mu\text{m}$  diameter with 10  $\mu\text{m}$  interpatch distance.

From Figure 6.6, it is obvious that the temperature causes a dramatic change in the grown GaN form. For the 20  $\mu\text{m}$  Pattern F, it can be found that the formation of grown GaN is an entire cylinder which is not seen in any of the other groups in this pattern before. Additionally, the diameter of the top surface on this GaN cylinder in Group E is larger than that in Group D and is almost equal to the longest hexagon diagonal of the bottom surface

on the hexagonal prism in Group B and C. Both the size and shape information of the overgrown GaN layer indicate that the lateral growth is enhanced during a lower temperature selective area overgrowth. This result also matches the fact that the lateral growth is also encouraged under low temperature in nanowire/nanostructure growth. However, it can also be found that there are some pits on the surface in Group E, which will normally be regarded as a signal for the weakening of the lateral growth. One of the most possible explanations is that the GaN selective area overgrowth using the SiO<sub>2</sub> mask is a complex process. This process is affected by the different diffusion rates of atoms on SiO<sub>2</sub> and GaN surfaces. For the results in Group E, on the one hand, the drop in temperature causes a weakening of the GaN lateral growth on the GaN surface and leads to the pits. But on the other hand, the weakening of Ga atoms diffusion on SiO<sub>2</sub> surface also weakens the reinforcement of the vertical GaN growth in the growth window. This explanation can also be applied to similar results in Pattern E.

However, there are some differences in Pattern D, where the overgrown GaN is forming a hexagonal pyramid instead of a hexagonal prism observed in other Groups with the same pattern. This transformation can be regarded as a weakening in the lateral growth, which is much more significant than the enhancement of the GaN vertical growth. Considering the Pattern D sample from other groups are forming a similar thick-boundary hexagonal prism, it is possible that the vertical growth is mainly influenced by the diffused Ga atoms from the SiO<sub>2</sub> surface dominates the overgrowth process in Pattern D. Additionally, as the growth area/total area ratio in Pattern D is very small, the changes in growth conditions can hardly influence the saturated Ga atoms from diffusion. Therefore, with the weakening of GaN lateral growth at a low growth temperature, the vertical growth further dominates the whole overgrowth process.

Four growth conditions are investigated to observe their influence during the selective area GaN overgrowth on patterned SiO<sub>2</sub> masks. The pattern size and growth window distance as well as the growth temperature are the key factors that determine the GaN overgrowth modes and growth rates in different degrees. Besides, growth pressure and V/III sources flow rates can also influence the final results but need to be optimised further for different growth requirements.

## 6.2.2 Growth of micro-LEDs on GaN

After the study of selective area GaN growth modes, the next step is to achieve steady and reproducible devices by the direct epitaxial approach. As the final design of the integrated micro-led/HEMT microdisplay is to grow the micro-LED structure on a prepared and patterned HEMT template, this work here is aiming to achieve micro-LEDs by a direct epitaxial approach.

Based on the previous selective area growth mode investigation in the section before, the overgrown GaN layer is designed to be oversized and much thicker than the SiO<sub>2</sub> masks. However, for the device structure overgrowth, it needs to be nearly the same height as the mask to meet the following fabrication requirements. Besides, unlike the GaN, the InGaN can be deposited on SiO<sub>2</sub>. Therefore its growth rate change would be quite different compared with that of GaN. Consequently, it is necessary to investigate the growth conditions of the InGaN/GaN micro-LED ( $\mu$ LED) structure for the selective area overgrowth.

Considering the fabrication requirements and the growth conditions investigated before, 20  $\mu$ m is chosen to be the growth window size here and Pattern F is finally determined as the  $\mu$ LED mask pattern. Moreover, compared to the overgrowth of planar LED structure, the cleaning treatment before the selective area overgrowth is the same as demonstrated in section 6.2.1.

After that, as shown in Figure 6.7, the prepared template with SiO<sub>2</sub> mask is sent to MOCVD for the  $\mu$ LED structure overgrowth. The whole overgrowth process starts in the hydrogen atmosphere and firstly with the deposition of an n-GaN layer. Then, the temperature decreases to 890 °C and the carrier gases are all switched to nitrogen to perform the 30 pairs of InGaN/GaN superlattice growth. Next, 5 pairs of InGaN QWs and GaN QBs are grown at 798 °C and 880 °C respectively. After the active region growth, the carrier gases are changed back to hydrogen and the temperature raises to 930 °C for the p-GaN growth.

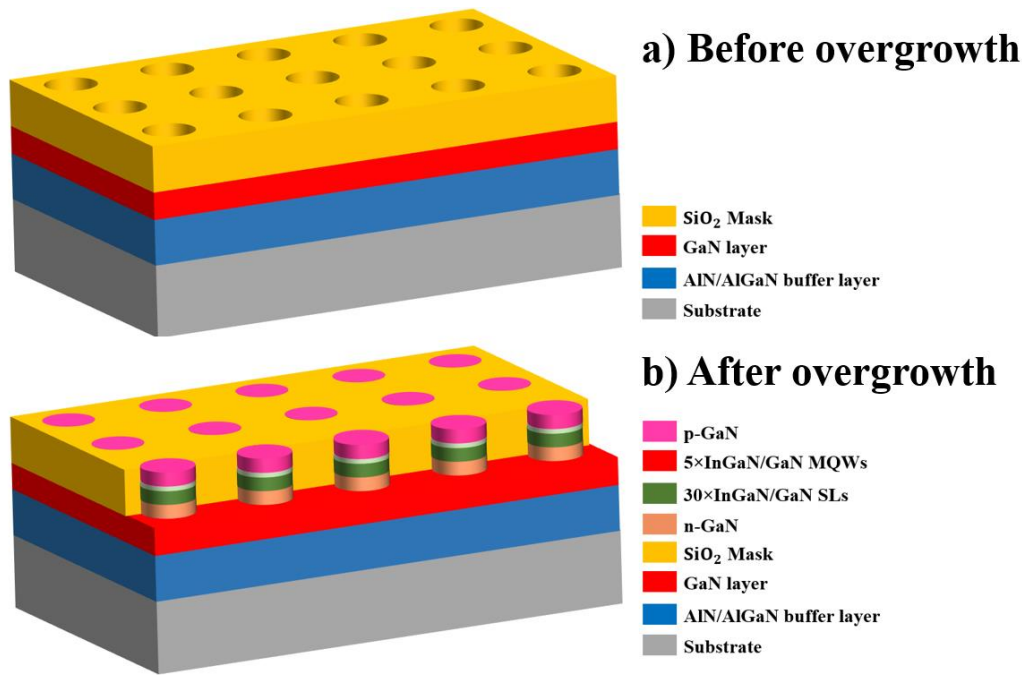


Figure 6.7 Structure of a) template before overgrowth, b) overgrown  $\mu$ LED

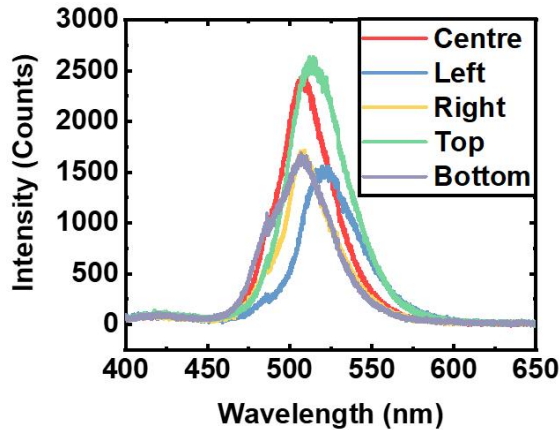
Figure 6.8a shows the PL measurement results of an overgrown 20  $\mu$ m-diameter  $\mu$ LED. Curves in different colours represent spectra from different areas of the whole wafer. The red shows the emission wavelength from the very centre of the wafer and its peak wavelength is 507 nm. Then, the purple one labelled as ‘bottom’ means it is taken from the area near the cut orientation of the wafer and the peak emission wavelength of it is 507nm as well. The top area, which locates in the area opposite to ‘bottom’ on the wafer, is marked in green and has a slightly longer peak wavelength of 512nm. As for the area ‘left’ and ‘right’, they are obtained by placing the sample face up in front of the observer, with the cut orientation close to the observer. Then, at this time, the left-hand side of the observer is the 'left' area, and the other side is the 'right' area. And their emission curves are marked as blue and yellow in the figure and get the peak wavelengths of 520nm and 507nm respectively.

Figure 6.8b shows an SEM picture taken from a 45° tilt Top view. It demonstrates a 20  $\mu$ m diameter overgrown  $\mu$ LED clearly. As can be seen in the figure, the height of the  $\mu$ LED is roughly the same as that of the area outside the growth zone. Besides, inside the growth window, no obvious edge effect, which means the boundary part of the growth area is dramatically higher than the centre, is detected. Therefore, this sample can be used for further device fabrication. However, the surface of the device is quite rough. This is because



of the unoptimized p-GaN growth condition. Decreasing the p-GaN growth rate would be benefit to overcome this issue.

### a) PL spectra of a 20 $\mu$ m diameter $\mu$ LED



### b) SEM picture from a 45° tilt Top view

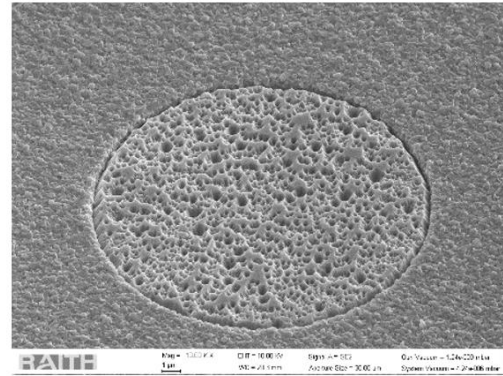


Figure 6.8 Results of a 20 $\mu$ m diameter  $\mu$ LED. a) PL spectra and b) SEM picture from a 45° tilt Top view. The bad surface condition is because of the p-GaN growth condition. Further optimization towards it is needed.

A 20 $\mu$ m diameter  $\mu$ LED structure is achieved by overgrowing corresponding structures on a patterned GaN template in this section. Besides, the PL emission spectra of it are measured and the emission wavelength of this sample is 507nm ~ 520nm depending on the different parts of the sample. Furthermore, the top surface morphology of this sample is observed by SEM to ensure the sample is ready for the next fabrication.

### 6.2.3 Growth of Integrated $\mu$ LEDs/HEMTs Microdisplay on a Single Chip

There is a growing need for creating a micro-LED ( $\mu$ LED) based microdisplay since it may be the only display system capable of meeting the criteria for augmented reality/virtual reality systems, helmet-mounted displays and head-up displays. However, a number of basic obstacles that no current technology is addressable must be addressed before such a microdisplay with satisfactory performance can be developed. The purpose of this study is to offer a novel integration idea based on an epitaxial technique for monolithically integrating  $\mu$ LEDs and high electron mobility transistors (HEMTs) on a single chip. This notion may be accomplished by using a selective epitaxial overgrowth technique on a predetermined HEMT template with micro-hole masks. Finally, the suggested epitaxial integration approach is shown by the creation of a prototype displaying an 8  $\times$  8 micro

LED microdisplay in which each  $\mu$ LED is electrically powered by a separate HEMT through the HEMT's gate bias.

Figure 6.9a shows a 3D layout for our  $8 \times 8$   $\mu$ LED microdisplay. Figure 6.9b illustrates the schematic of the cross section of a single  $\mu$ LED as a pixel, demonstrating each  $\mu$ LED which is selectively overgrown on a prepatterned HEMT template can be electrically driven by the circular gate of each HEMT surrounding a  $\mu$ LED, namely, all  $\mu$ LEDs are individually address-able via HEMTs.

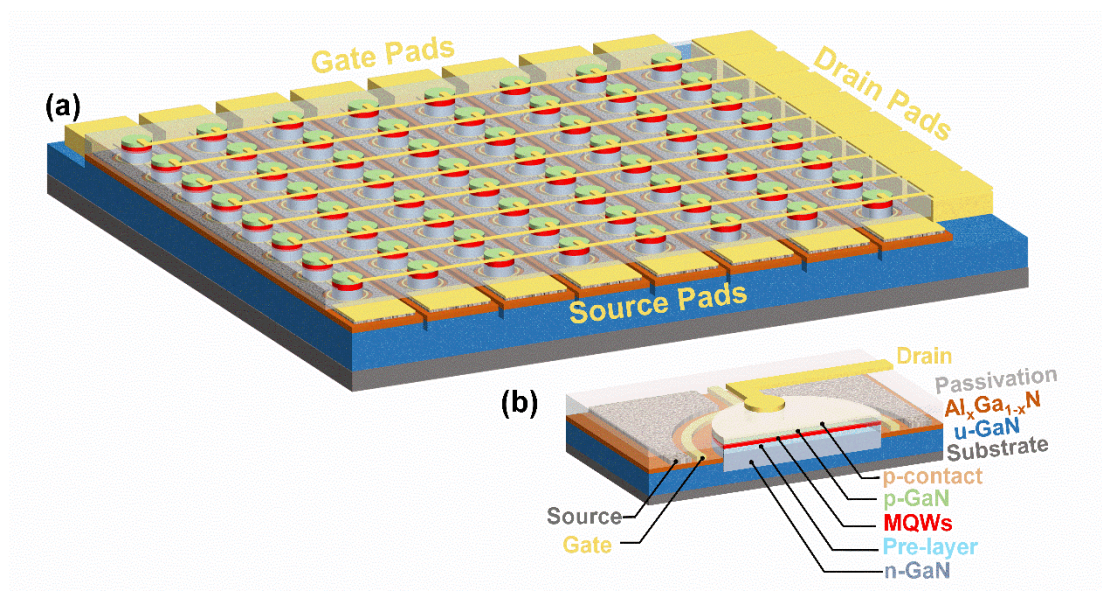


Figure 6.9 a) 3D layout of our  $8 \times 8$   $\mu$ LED microdisplays; b) schematic of the cross-section of a single  $\mu$ LED, demonstrating each  $\mu$ LED can be electrically driven by the circular gate of each HEMT surrounding a  $\mu$ LED.

In our previous work (i.e., not individually addressable  $\mu$ LEDs), a single n-GaN layer on sapphire was used as a template for the selective overgrowth of  $\mu$ LED arrays.[24],[25] In this work, an AlGaIn/GaN HEMT structure instead of a single n-GaN layer is used as a template to achieve a microdisplay via an epitaxial integration of  $\mu$ LEDs and HEMTs, where each  $\mu$ LED is individually driven by a HEMT. The HEMT template consists of a 25 nm  $\text{Al}_{0.20}\text{Ga}_{0.80}\text{N}$  barrier and a 1 nm AlN spacer in addition to a 1  $\mu\text{m}$  GaN buffer layer and a high temperature AlN buffer layer which is directly grown on c-plane sapphire. Using our high temperature AlN buffer approach, our HEMTs have demonstrated an extremely high breakdown field and an extremely low leakage current.[27] Such a HEMT structure can electrically drive

individual  $\mu$ LEDs without concerning about leakage current which may unintentionally turn on  $\mu$ LEDs which are supposed to be off. For the details of our HEMT structure, please refer to our paper recently published elsewhere.[27]

Subsequently, a  $\text{SiO}_2$  film with a thickness of 500 nm is deposited on the HEMT template by using a plasma-enhanced chemical vapor deposition (PECVD) technique. A photolithography technique and then drying etching processes are used to selectively etch the  $\text{SiO}_2$  mask and the AlGa $\text{N}$  (HEMT barrier) down to the surface of the HEMT template, forming regularly arrayed microholes with a diameter of 20  $\mu\text{m}$ . Next, a standard InGa $\text{N}$ -based LED structure with a thickness of 500nm, which is close to the  $\text{SiO}_2$  thickness, is selectively overgrown on the patterned template. With the same height of the  $\text{SiO}_2$  and the LED structure, the metal electrodes could be easily fabricated. The LED structure consists of a n-type Ga $\text{N}$  layer, an  $\text{In}_{0.05}\text{Ga}_{0.95}\text{N}$  prelayer, five-period InGa $\text{N}$ /Ga $\text{N}$  MQWs (InGa $\text{N}$  quantum well: 2.5 nm and Ga $\text{N}$  barrier: 13.5 nm) as an active region, and then a 20 nm p-type  $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$  as a blocking layer. Finally, a 150 nm p-type Ga $\text{N}$  is grown. Due to the dielectric mask, the LED growth is limited within the preformed  $\text{SiO}_2$  microholes, naturally forming regularly arrayed  $\mu$ LEDs. By this approach,  $\mu$ LEDs (including diameter, location, and shape) are fully determined by the  $\text{SiO}_2$  microhole masks, where the pitch size and the pitch-to-pitch spacing determine the resolution of the final microdisplay. In our case, the diameter of each  $\mu$ LED and the edge-to-edge spacing are 20  $\mu\text{m}$  and 25  $\mu\text{m}$ , respectively, leaving enough space for electronic part integration. It is worth highlighting that the size of  $\mu$ LEDs can be further reduced, leading to a further reduction in the gate-width of a transistor for current driving. A reduced pixel size and pixel-to-pixel distance may be helpful for further enhancing a resolution. By using this direct epitaxial approach, a high resolution with a 3.6  $\mu\text{m}$  pitch size and a 2  $\mu\text{m}$  edge-to-edge spacing have been achieved..[24],[25] This direct epitaxial approach also means that the formation of  $\mu$ LED arrays does not involve any  $\mu$ LED mesa etching processes. Please refer to Figure 6.10a–d for our detailed selective growth processes. By means of using the selective overgrowth approach on a prepatterned HEMT template,  $\mu$ LEDs and HEMTs are epitaxially integrated. The next step is due to integrated device fabrication. Figure 6.10e–l provides the schematic of our integrated device fabrication procedure. I have done all the epitaxy work during the whole process, while Dr. Yuefei Cai has performed all the fabrication and packaging work.

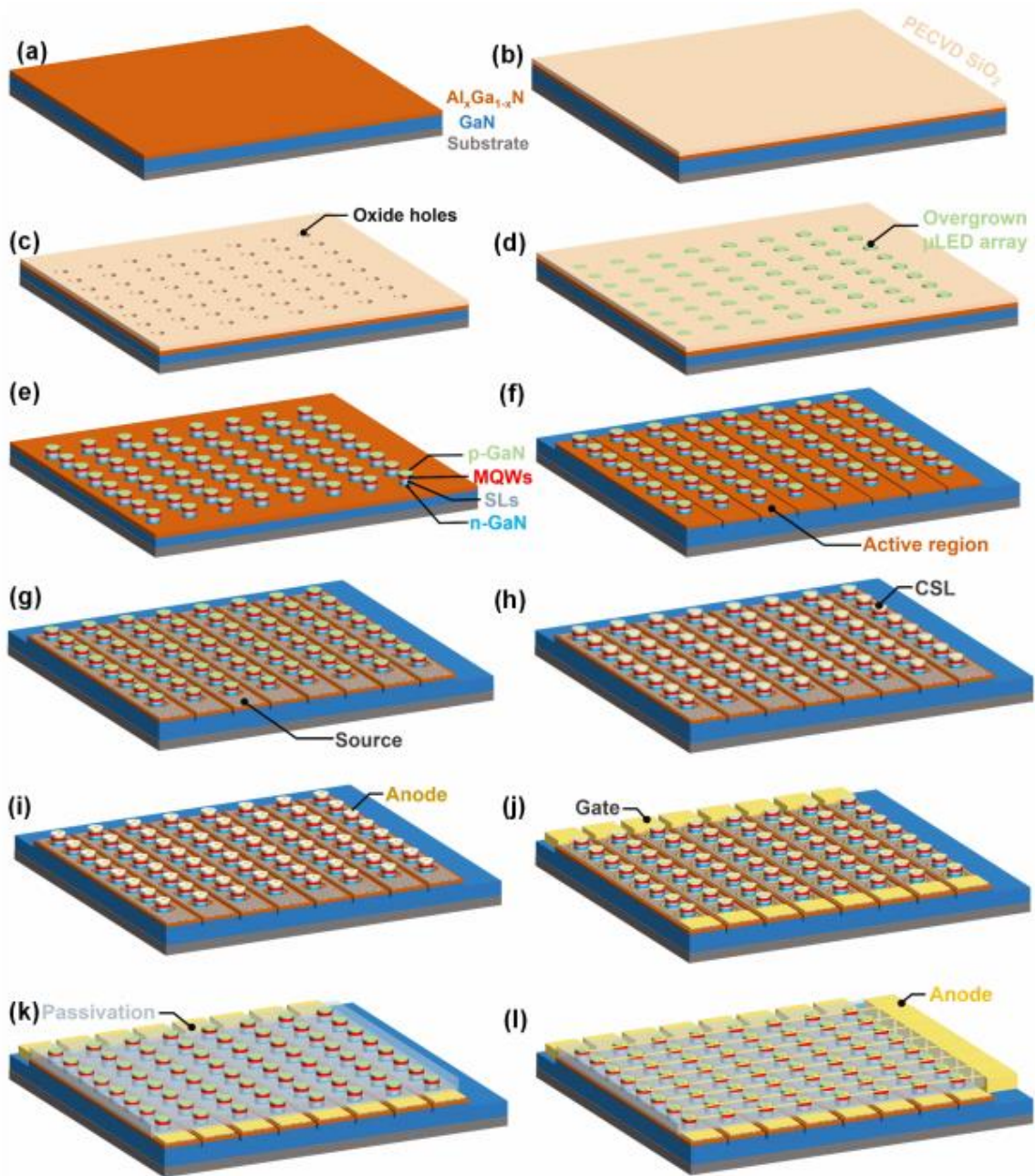


Figure 6.10 Fabrication process flow-chart of the integrated  $\mu$ LEDs/HEMTs microdisplay

Figure 6.9b illustrates each  $\mu$ LED which is surrounded by an individual HEMT, where a circular gate in each HEMT controls injection current into each  $\mu$ LED. Figure 1a indicates that all the circular gates in each column are eventually connected to a gate pad located on one side of the  $8 \times 8$   $\mu$ LED microdisplay, while all the semicircular sources (Ti/Al/Ni/Au metal stacks which undergo rapid thermal annealing (RTA)) represented by grey color in each column are connected to a source pad (Ti/Al/Ti/Au) on another side. All the p-contacts on top of each  $\mu$ LED in each row are connected to a drain pad (Ti/Al/Ti/Au). Between two neighboring columns, an isolation trench

with a width of 3  $\mu\text{m}$  and a depth of 300 nm is formed by etching down to the semi-insulating GaN buffer of the HEMT structure for an insulation purpose by an inductive-coupled plasma (ICP) technique.

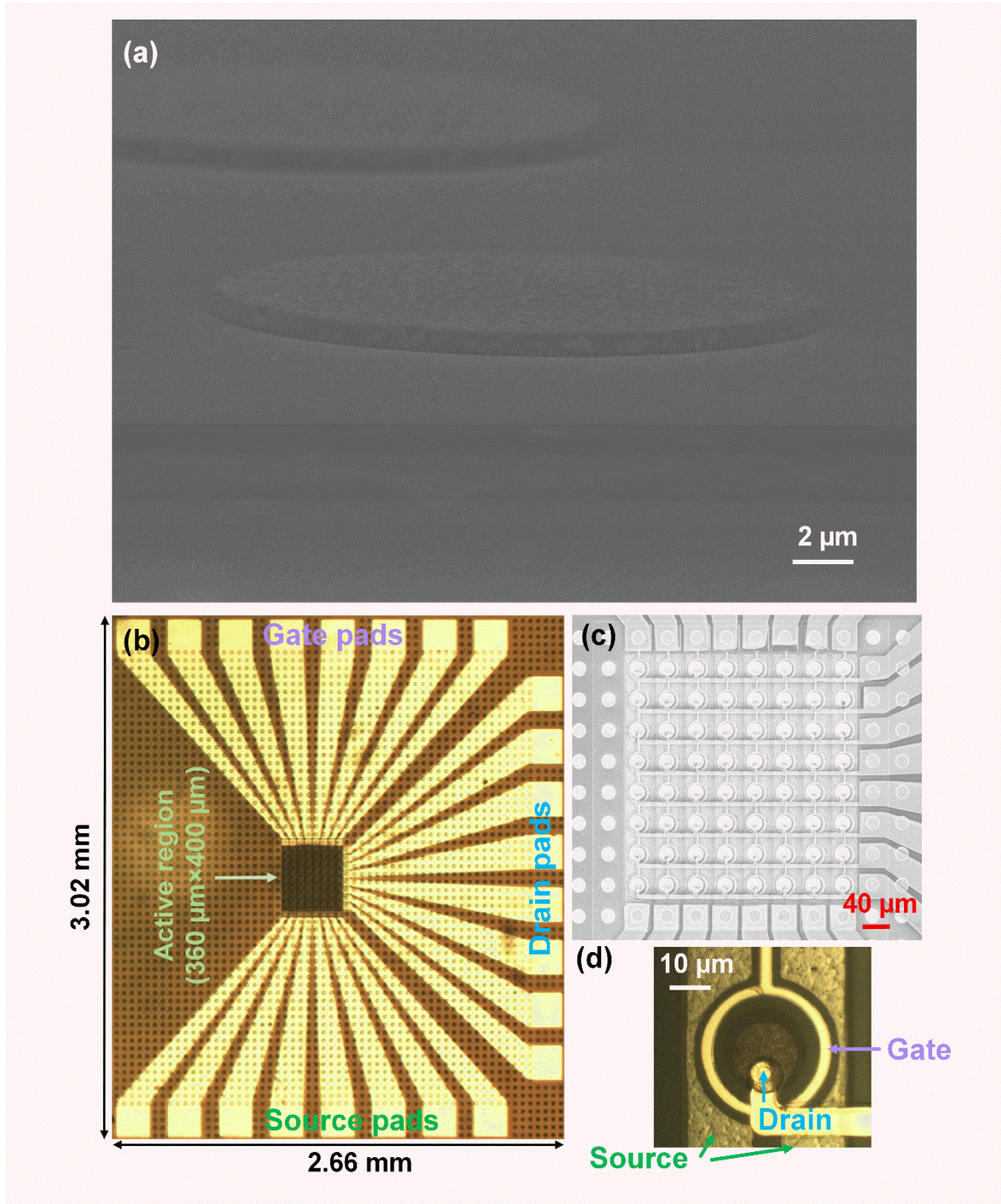


Figure 6.11 a) Tilted SEM image of our overgrown  $\mu\text{LEDs}$ ; b) optical microscopic image of our  $8 \times 8$  integrated  $\mu\text{LEDs/HEMTs}$  microdisplay; c) SEM image of the screen region of each microdisplay; d) a single  $\mu\text{LED/HEMT}$  integrated unit as a pixel, showing that each  $20 \mu\text{m}$   $\mu\text{LED}$  is surrounded by an individual HEMT (scale bar:  $10 \mu\text{m}$ ).

## Results

Figure 6.11a shows the tilted scanning electron microscopy (SEM) image of our single  $\mu$ LEDs after selective overgrowth and then oxide mask removal.

Figure 6.11b displays the optical microscopic image of our  $8 \times 8$  integrated  $\mu$ LEDs/HEMTs microdisplay, showing  $2.66 \text{ mm} \times 3.02 \text{ mm}$  in dimension for each microdisplay chip. The rectangular screen region with a size of  $360 \mu\text{m} \times 400 \mu\text{m}$  consists of  $8 \times 8$  integrated  $\mu$ LEDs/HEMTs.

Figure 6.11c shows the SEM image of the screen region of each microdisplay. Each drain pad which connects all the pixels in a same row is deposited on a  $2 \mu\text{m}$  SU8-2 passivation layer, while each source pad and each gate pad connecting all the pixels in a same column locate below the passivation layer. Such a design avoids the use of double or triple passivation layers, thus simplifying the fabrication process.

Figure 6.11d displays a typical single  $\mu$ LED/HEMT pixel, showing that each  $20 \mu\text{m}$   $\mu$ LED is surrounded by an individual HEMT. The drain of each  $\mu$ LED is located on the transparent p-type contact made of Ni/Au alloy which has undergone a thermal annealing process. In each HEMT, the gate length, the gate-to-source distance, and the gate width are  $2 \mu\text{m}$ ,  $2 \mu\text{m}$ , and  $88 \mu\text{m}$ , respectively.

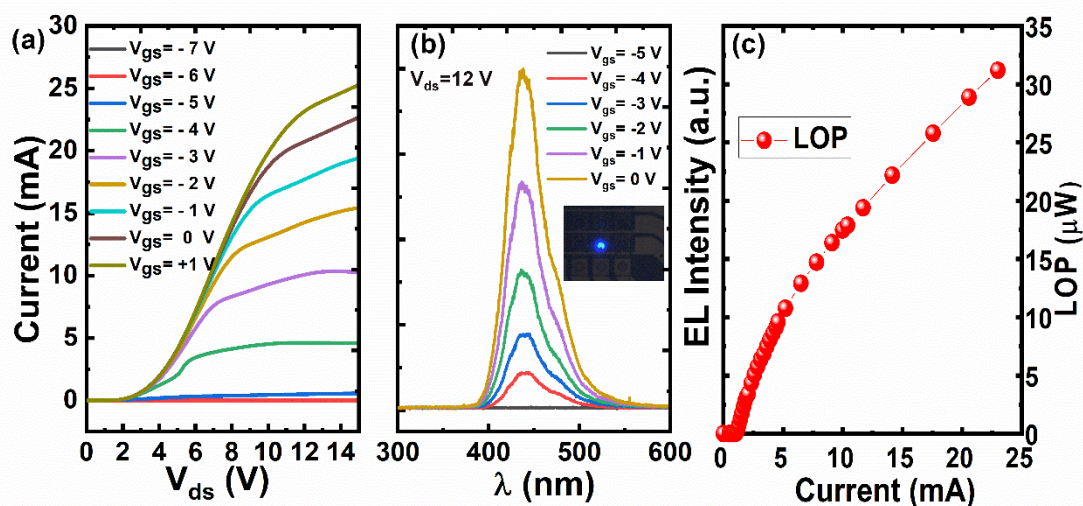


Figure 6.12 a) Typical  $I$ - $V$  characteristics of a single  $\mu$ LED/HEMT integrated unit; b) typical EL spectra of a single  $\mu$ LED driven by an individual HEMT as a function of gate bias; Inset: Typical EL image from a single  $\mu$ LED driven at a

*gate-source bias  $V_{gs} = 0$  V and a drain-source bias  $V_{ds} = 12$  V; c) LOP as a function of injection current for a single  $\mu$ LED/HEMT device.*

Figure 6.12a shows the typical current–voltage ( $I$ – $V$ ) characteristics of a single  $\mu$ LED/HEMT integrated unit, indicating a typical HEMT characteristic. Figure 6.12b exhibits the typical electroluminescence (EL) spectra of a single  $\mu$ LED driven by an individual HEMT as a function of gate bias, where inset provides an EL image from a single  $\mu$ LED driven at a gate–source bias  $V_{gs} = 0$  V and a drain–source bias  $V_{ds} = 12$  V as an example. Figure 6.12b shows that the EL intensity of a single  $\mu$ LED can be modulated by a gate bias from  $-5$  to  $0$  V. Figure 6.12c shows the light output power (LOP) of a single  $\mu$ LED measured as a function of injection current. The emission is collected by an objective lens ( $40\times$ ,  $0.75$  NA) and then detected by a power meter (Thorlabs PM100D).

Figure 6.13a shows an equivalent circuit for our  $8 \times 8$  integrated  $\mu$ LEDs/HEMTs microdisplay. Gate and source terminals in each column are introduced into G1-G8 and S1-S8, respectively. Drain terminals in each row are introduced into A1-A8. These terminals are eventually wire bonded into a  $2.6$  cm  $\times$   $3$  cm PCB as shown in Figure 6.13b, where all the source terminals on the PCB are converted into two pins, while the gate terminals and the drain terminals remain separated pins for an easy control purpose.

Figure 6.13c shows our electrically driving scheme for our  $8 \times 8$  integrated  $\mu$ LEDs/HEMTs microdisplay. As mentioned above, the turn-on voltage for a gate and the operation voltage for a drain are different from that used for a conventional seven-segment display (typically for driving standard LEDs). As a result, a standard Max7221 chip which is commercially available does not match our integrated microdisplay and thus cannot be adopted here.

To address this issue, a different design is required. In our design, source terminals are directly introduced to a  $+5$  V power supply (provided by Keithley 2400). In this case, we do not need to further convert a positive  $0$  to  $+5$  V SEG signal into a negative voltage which is used to switch on/off a HEMT. Since the source terminals are at  $+5$  V, the voltage drop from the gates to the sources can be tuned from  $-5$  to  $0$  V, which is good enough to use the gate to switch on/off a HEMT. To bypass the SEG current,  $20$  k $\Omega$  resistors are used between the SEG signals and ground prior to being introduced to the gate terminals.

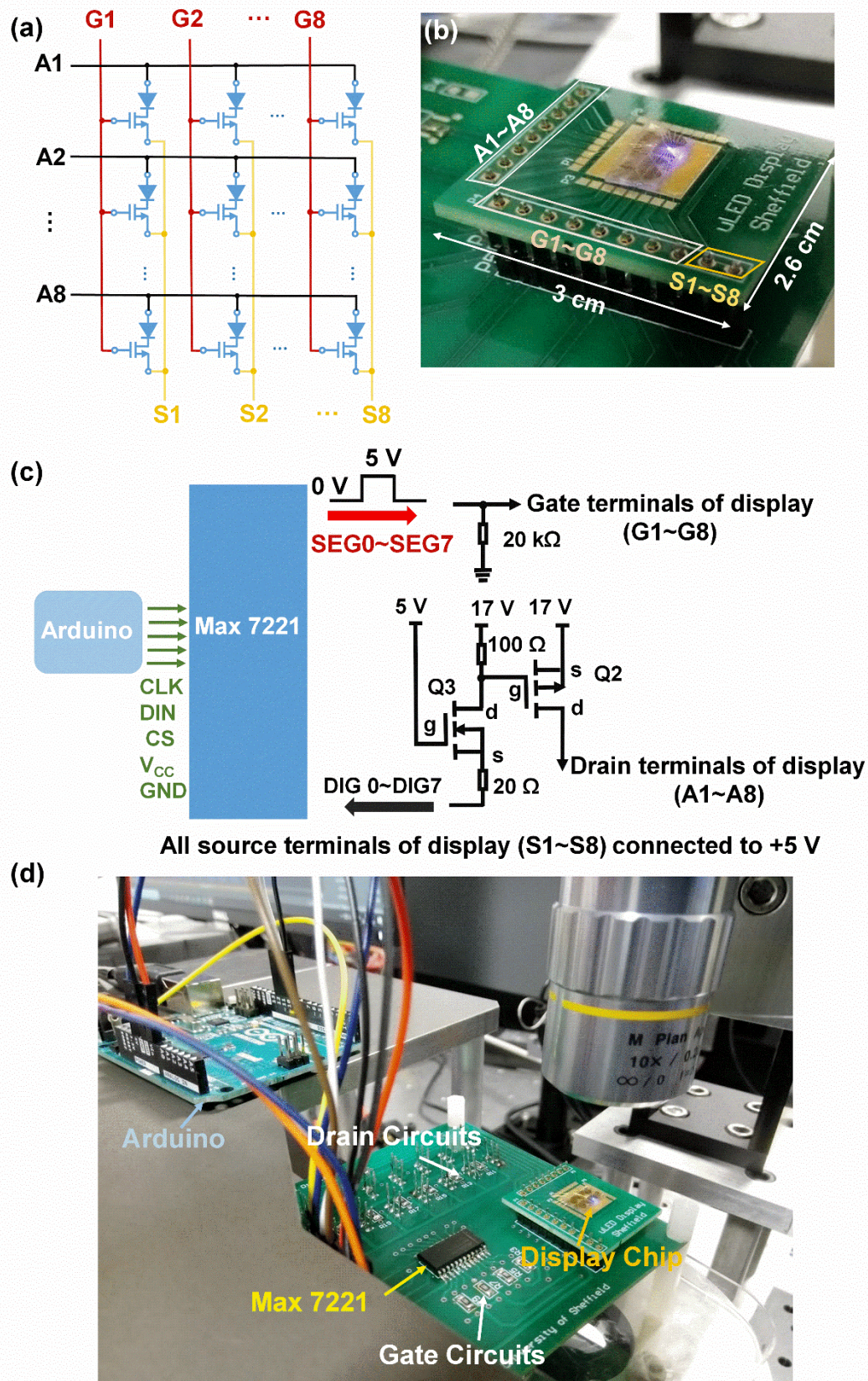


Figure 6.13 a) Equivalent circuit for our  $8 \times 8$  integrated  $\mu$ LEDs/HEMTs microdisplay; b) Our PCB where all the gate terminals, source terminals, and drain terminals are wire-bonded; c) our electrically driving scheme for our  $8 \times 8$  integrated  $\mu$ LEDs/HEMTs microdisplay; d) photo of our test setup and driving PCB.



For the drain terminals, an analog circuit as shown in Figure 6.13c is used to boost the DIG signal to a higher voltage level ( $>10$  V). To achieve such a function, the circuit suggested in Max 7221's application note [28] has been modified, where two MOSFETs have been adopted, namely, Q2 which is IRF9520 (p-channel) and Q3 which is IRF510 (n-channel). The drain terminals of Q2 are connected to the drain terminals. A CPU controlled Arduino board is used to provide clock (CLK), data (DIN), chip-selection (CS),  $V_{cc}$  (+5 V), and GND signal to the Max 7221 chip. Our test setup and driving PCB are displayed in Figure 6.13d.

Finally, our  $8 \times 8$  integrated  $\mu$ LEDs/HEMTs microdisplay has been demonstrated through a short video showing "I ♥ Sheffield" which can be found in the Supporting Information. The video has been recorded via a CCD camera mounted on a light collection system consisting of a  $10\times$  objective lens and a NAVITA 12 $\times$  Zoom Lens System as shown in Figure 6.14a.

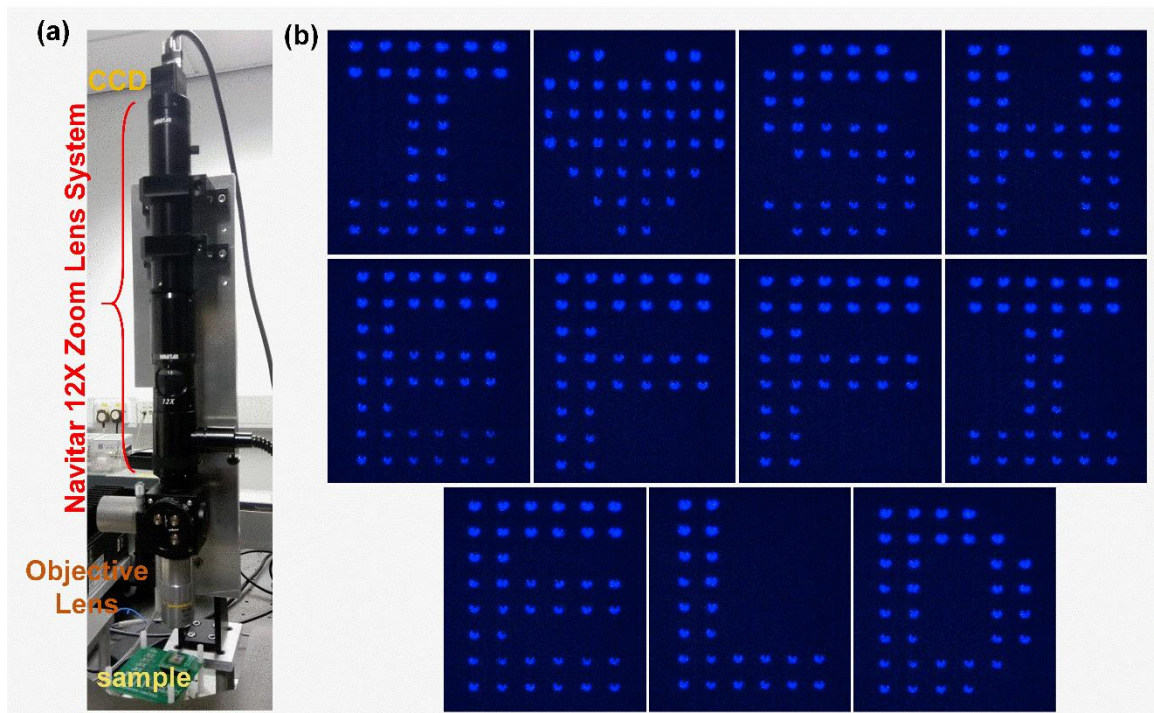


Figure 6.14 a) Optical image of our light collection system for recording a short video using our  $8 \times 8$  microdisplays; b) images ("I ♥ Sheffield") which are captured from the short video for a demo purpose.

Figure 6.14b shows the images which are captured from the short video for a demo purpose. The delay between each letter in the video is 1000 ms, which can be changed through the code in Arduino. By means of changing the duty cycle of the gate pulse, the EL intensity

of individual  $\mu$ LED pixel can be modified using a pulse-width-modulation (PWM) scheme [29] to obtain a high-contrast-ratio display.

It is worth highlighting that such each  $\mu$ LED/HEMT integrated unit can be controlled by both gate voltage and drain voltage. As a consequence, such an integrated unit can also play a visible light communication (VLC) role in addition to its microdisplaying function [30]-[32]. Except for this dual-functionality application, such an integrated device can also be adopted for much broader fields, such as display and flexible biomedical applications [33],[34], quantum dot colour-converting layers for a full colour display, etc [35],[36].

## Summary

In conclusion, we have developed an epitaxial approach to monolithically integrate  $\mu$ LEDs and HEMTs on a single chip by means of using a selective overgrowth method on a predefined HEMT template featuring  $\text{SiO}_2$  microhole masks. Our approach has eliminated all the fundamental issues which cannot be overcome in either “pick-and-place” approach or “flip-chip bonding” technology. Finally, we have translated the proposed epitaxial integration concept into a prototype, demonstrating an  $8 \times 8$  microLED microdisplay, where each  $\mu$ LED is electrically driven by an individual HEMT which surrounds its respective  $\mu$ LED via the gate bias of the HEMT.

## 6.3 Conclusion

Growth conditions of selective area overgrowth of GaN are investigated and then applied to perform an integration of  $\mu$ LEDs and HEMTs on a single chip. Specifically, the pattern size and growth window distance as well as the growth temperature, are found to be the most significant influencing factors for the GaN overgrowth. After that, a  $20\mu\text{m}$  diameter  $\mu$ LED is achieved with an emission wavelength of  $507\text{nm} \sim 520\text{nm}$ . Finally, monolithic integration of  $\mu$ LEDs and HEMTs on a single chip is achieved and an  $8 \times 8$  microLED microdisplay with each  $\mu$ LED electrically controlled by its own HEMT through the HEMT's gate bias is demonstrated.

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# Chapter 7 Conclusions and Future work

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## 7.1 Conclusions

In this thesis, the growth of GaN on (111) silicon was investigated in detail, resulting in the production of AlGaN/GaN HEMTs and InGaN/GaN MQWs prototypes. The monolithic epitaxial integration of  $\mu$ LED and HEMT has been demonstrated on pre-patterned GaN templates (albeit on sapphire substrates instead of silicon substrates), culminating in the prototype of an  $8 \times 8$  microLED microdisplay. These fundamental products have paved the way to achieving an epitaxially integrated microdisplay on Si substrates in the future.

### 7.1.1 Growth of GaN-based Material on (111) Silicon Substrate

An extensive investigation was conducted that encompassed the various stages of GaN - on-Si growth, such as the preparation of the silicon substrate, the optimised growth of aluminium nitride (AlN) layers, the optimised growth of aluminium gallium nitride (AlGaN) layers, and the optimised growth of gallium nitride (GaN) layers. A direct high-temperature annealing method (that did not require any chemical pre-treatment) was used to treat the Si surface. An in-situ measurement of the curvature revealed that the substrate thickness plays an important role in determining the non-uniformity of the vertical temperature distribution. A combination of a low high-temperature AlN growth rate and a very thin TMA-preflow was found to produce an AlN buffer layer with excellent crystal quality and a smooth surface on the Si substrate. The generation of a crack-free GaN-on-Si template is dependent on AlGaN growth parameters, including thickness, Al content, and  $\text{NH}_3$  flow rate. Finally, a two-step approach to GaN growth was developed, where the thickness of the GaN layer in the first step plays a critical role in determining the quality and surface morphology of the final GaN crystals.

### 7.1.2 Demonstration of Electronics and Photonics on (111)Silicon

Based on the aforementioned studies on the optimisation of GaN growth on (111) Si, we demonstrated the potential of GaN/AlGaN HEMTs and an InGaN/GaN MQW. As a result of a high crystal quality AlN buffer layer, GaN HEMTs with an electron mobility of  $1600 \text{ cm}^2 \text{ V}^{-1} \text{ S}^{-1}$  and a current density of  $290 \text{ mA/mm}$  for  $120 \text{ }\mu\text{m}$ -gate HEMTs on (111) silicon were produced. A detailed comparison study has been carried out on InGaN/GaN



MQWs grown on (111) silicon and sapphire under identical conditions. This study demonstrated that the tensile strain plays a very positive role in extending the LEDs to longer emission wavelengths. The InGaN MQW structure grown on a GaN-on-Si template exhibits a much longer emission wavelength than a comparable structure on a GaN-on-sapphire template, which was further confirmed by both XRD and PL measurements. This provides useful information regarding the development of longer emission wavelength LEDs, such as yellow or red LEDs, which have historically been a great obstacle in the field of III-nitride optoelectronics.

### **7.1.3 Demonstration of a Monolithically Integrated $\mu$ LEDs/HEMTs Microdisplay on a Single Chip**

A systematic study of selective epitaxial growth was carried out on micro-arrayed templates, in which the growth parameters were optimised. Unlike GaN growth on a planar substrate or template, selective epitaxial growth exhibited unique features, such as the occurrence of preferred growth, which makes it a challenge to obtain flat surfaces. Our optimised growth conditions allowed for the generation of flat surfaces in selectively overgrown samples. These developments were used to create a monolithically integrated  $\mu$ LED with a diameter of 20 $\mu$ m in the green spectral region and a HEMT on a single chip, culminating in an 8  $\times$  8  $\mu$ LED microdisplay with each LED controlled by an individual HEMT via a biased HEMT gate.

## **7.2 Future work**

Considering these valuable fundamental optimizations, it is possible to extend the epitaxial integration method to  $\mu$ LEDs and HEMTs on a (111) Si substrate. However, to ensure compatible device performance, it is necessary to further improve the crystal quality of the GaN layer grown on the Si substrate, which would reduce the dislocation density and allow for greater optical efficiencies.

In addition to improvements to the crystal quality, the applicability of the current GaN-on-Si growth methods to Si wafers of larger diameter is also important, as larger GaN-on-Si devices are in great demand, especially CMOS-compatible (100) silicon substrates.

As for the  $\mu$ LED applications, due to the tensile strain induced during the epi process, the GaN-on-Si template based  $\mu$ LEDs have a great potential in achieving better performance

at a longer emission wavelength (550nm~650nm) comparing to their competitors on GaN-on-Sapphire templates. Many relevant work have been done since the start of manuscript writing of this thesis but more work are still on going. Issues like the crystal quality and  $\mu$ LED luminance uniformity are still waiting to be solved.

Besides, so far our group has demonstrated ultra small and ultra compact green and red  $\mu$ LED arrays. Based on those structures and with the idea of adding top and bottom DBRs, green or even red vertical cavity surface emitting micro-laser array could be achieved. By the end of the manuscript writing of this thesis, most of the fundamental work of this idea has been achieved and some interesting results are collected. Hopefully we could make some exciting conclusions or demo some thrilling device in the near future.

Furthermore, there are still many obstacles that must be overcome in the field of microdisplay technology, such as the development of a full-colour RGB microdisplay on a single chip.