The University Of Sheffield.

Fabrication and Characterisation of Nitride DBRs and Nitride Membranes by Electrochemical Etching Techniques

Ye Tian

The University of Sheffield

Faculty of Engineer

Department of Electronic Electrical Engineering

Centre for GaN Materials and Devices

Supervisor: Professor Tao Wang

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Abstract

A Distributed Bragg Reflector (DBR) is an important component for semiconductor microcavities and optoelectronic devices, such as vertical cavity surface emitting lasers (VCSELs), resonant cavity light-emitting diodes (RCLEDs). In the past thirty years, epitaxially grown GaAs-based DBRs have made great achievements of the application of III-V VCSELs in communications and mobile applications. At the same time, III-nitrides have demonstrated excellent performance in solid-state lighting and advanced optoelectronic devices due to the wide bandgap and unique properties. In recent years, GaN-based semiconductors have made great progress in the application of blue VCSELs. However, the absence of high-performance DBRs is a challenge for developing higher-power GaN-based VCSELs.

Currently, the typical epitaxial GaN-based DBRs are limited by a long growth period, low optical performance, and poor quality of growth. Therefore, this project proposes a method to fabricate nanoporous (NP)/GaN-based DBR by electrochemical etching (EC), which are grown using metalorganic vapour-phase epitaxy (MOVPE). The heavily silicon doped GaN layer is transformed into an NP structure by selective etching, resulting in a higher refractive index contrast in each periodic layer. Moreover, a lateral etching method is proposed to further improve the EC etching of DBRs. This method can confine the etching in each sacrificial layer and make the etching aperture directions highly uniform. The corresponding characterizations have been carried out to explore the mechanisms of different etching methods, by optical microscopy, scanning electron microscopy (SEM) and reflectance measurements. It further confirms that the laterally etched NP GaN-based DBRs exhibit a higher reflectivity and wider stopband.

The GaN sacrificial layers required for the EC etching are typically heavily silicon doped ($>10^{19}cm^{-3}$), resulting in a rough surface and saturated conductivity. On the other hand, the heavily silicon doped AlGaN with a low Al content (≤5%) exhibits an atomically flat surface

and an enhanced electrical conductivity. Therefore, in this work, we introduced multiple pairs of heavily doped n^{++}-$Al_{0.01}Ga_{0.99}N$/GaN to replace the widely used multiple pairs of heavily doped n^{++}-GaN/GaN to fabricate lattice-matched NP DBRs by EC etching. Consequently, the epitaxially grown n^{++}-$Al_{0.01}Ga_{0.99}N$/GaN-based DBR demonstrates a smoother surface than the n^{++}-GaN/GaN-based DBR. Moreover, the NP-$Al_{0.01}Ga_{0.99}N$/GaN-based DBR exhibits higher reflectivity and wider stopband after lateral EC etching compared to the NP-GaN/GaN-based DBR. This method has been successfully applied to fabrication of high-performance DBR structures with the wavelength range from blue to deep yellow by modifying the epitaxial growth conditions.

Furthermore, it is found that a very thin Al-Si diffusion layer is formed at the interface between an AlN buffer layer and a silicon substrate when growing the low-temperature AlN buffer layer on the n-doped silicon substrate by MOVPE. The diffusion layer exhibits high conductivity and can be EC-etched and polished as a sacrificial layer. Therefore, this method is proposed for stripping large-area GaN membranes by EC etching. A sample with AlN/AlGaN/GaN layers is first epitaxially grown by MOVPE on an n-doped (111) silicon substrate, and then bonded upside-down to a new glass host substrate and EC etched. Finally, lift-off of a large size GaN-based membrane has been realized with an area of 2.625cm^2 and a crack-free and nanoscale smooth surface. Compared to other lift-off methods such as laser lift-off (LLO), chemical lift-off (CLO), and mechanical release techniques, this method does not involve bulky and expensive equipment, which can be used to fabricate high-performance III-nitride devices on the membrane at low cost in the future.

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List of publications

[1] **Y. Tian,** P. Feng, C. Zhu, X. Chen, C. Xu, V. Esendag, G. Martinez de Arriba, T. Wang, *"Nearly Lattice-Matched GaN Distributed Bragg Reflectors with Enhanced Performance."* Materials (Basel), 15(10): 3536, (2022)

[2] J. Bai, Y. Cai, P. Feng, P. Fletcher, C. Zhu, **Y. Tian,** T. Wang, *"Ultrasmall, Ultracompact and Ultrahigh Efficient InGaN Micro Light Emitting Diodes (μLEDs) with Narrow Spectral Line Width."* ACS Nano. *14* (6), 6906-6911, (2020)

[3] J. R. Pugh, E. G. H. Harbord, A. Sarua, P. Fletcher, **Y. Tian,** T. Wang, M. J. Cryan, *"A Tamm plasmon-porous GaN distributed Bragg reflector cavity."* Journal of Optics. 23 (3), 035003, (2021)

[4] P. Fletcher, G. Martinez de Arriba, **Y. Tian,** N. Poyiatzis, C. Zhu, P. Feng, J. Bai, T. Wang, "*Optical characterisation of InGaN-based microdisk arrays with nanoporous GaN/GaN DBRs"*, Phys. D: Appl. Phys. 55 464001, (2022).

[5] **Y. Tian**, P. Feng, Zhu. C, C. Xu, X. Chen, R. Ni, T. Wang, *"GaN membrane lift-off with electrochemical etching method",* (In preparation).

Contents

List of Acronyms

AFM atomic force microscopy

AlGaAs aluminum gallium arsenide

AlGaN aluminum gallium nitride

AlN aluminum nitride

BOE buffered oxide etch

CCS close-coupled showerhead

CdS cadmium sulfide

CLO chemical lift-off

CP_2MG bis(cyclopentadienyl)magnesium

CVD chemical vapour deposition

DBR distributed Bragg reflector

DLDs dark-line defects

EC electrochemical etching

EDX energy-dispersive X-ray spectroscopy

ELO epitaxial lift-off

FDTD finite-difference time-domain

Ga gallium

Ga_2O_3 gallium oxide

GaAs gallium arsenide

GaCl gallium monochloride

GaN gallium nitride

GaP gallium phosphide

Ge germanium

HF hydrofluoric

HMDS hexamethyldisilazane

HNO_3 nitric acid

HVPE hydride-vapour-phase epitaxy

ICP inductively coupled plasma

InGaAs indium gallium arsenide

InN indium nitride

InP indium phosphide

IPA isopropyl alcohol

KOH potassium hydroxide

LDs laser diodes

LEDs light emitting diodes

LEEBI low energy electron beam irradiation

LLO laser lift off

LT low temperature

MBE molecular beam epitaxy

Mg magnesium

MIS metal-insulator-semiconductor

MOCVD metal-organic chemical vapour deposition

MOVPE metal-organic vapour phase epitaxy

nBA n-butyl acetate

NH3 ammonia

NM nanomembrane

NP nanoporous

PEC photo-enhanced electrochemical etching

PECVD plasma enhanced chemical vapour deposition

PET polyethylene terephthalate

PML perfectly matched layers

Pt platinum

QW quantum well

RCLEDs resonate cavity light-emitting diodes

RF radiofrequency

RIE reactive ion etching

RTA rapid thermal annealing

SCR space charge region

SEM scanning electron microscopy

SHE standard hydrogen electrode

Si silicon

SiC silicon carbide

SiO_2 silicon dioxide

Ta_2O_5 tantalum pentoxide

TMAl trimethyaluminium

TMGa trimethylgallium

TMIn trimethylindium

UV ultraviolet

VCSELs vertical cavity surface emitting lasers

ZnS zinc Sulphide

ZnSe zinc selenide

Chapter 1: Introduction

1.1 Laser diode and VCSEL

1.1.1 History of the Laser diode

Laser, which is the abbreviation of **L**ight **A**mplification by **S**timulated **E**mission of **R**adiation, is one of the major inventions of humans after nuclear energy and the computer in the 20th century. It is a coherently enhanced beam of photons produced by stimulating atoms to cause electron transitions and release radiant energy [1]. Compared with other light sources, the laser has various unique characteristics, such as extremely small divergence, high power density, monochromaticity and good coherence. In 1960, Theodore Harold Maiman reported the first laser, which is a ruby laser [2]. Two years later, a gallium arsenide (GaAs) based laser was reported by Robert N.Hall, which created a precedent for the study of semiconductor lasers [3]. With the first development of semiconductor technology, efficient and durable semiconductor lasers have been realized [4-10]. Currently, the commonly used semiconductor laser diodes are mostly made of gallium arsenide (GaAs) [5-7], cadmium sulfide (CdS) [8], indium phosphide (InP) [9], zinc sulfide (ZnS) [10]. Compared to gas lasers or solid-state lasers, semiconductor laser diodes have the advantages of high efficiency, small size, low weight, and low price, which is now widely used in many applications, such as optical fibre communication, optical disc, laser printer, laser scanner, laser pointer and so on. With the growing demand in medical, industrial, commercial, and other fields, as well as the rapid development of laser technology, the laser technology market is expanding significantly. As shown in **Figure 1.1**, the laser technology market size will increase to $17.6 billion by 2025 [11].

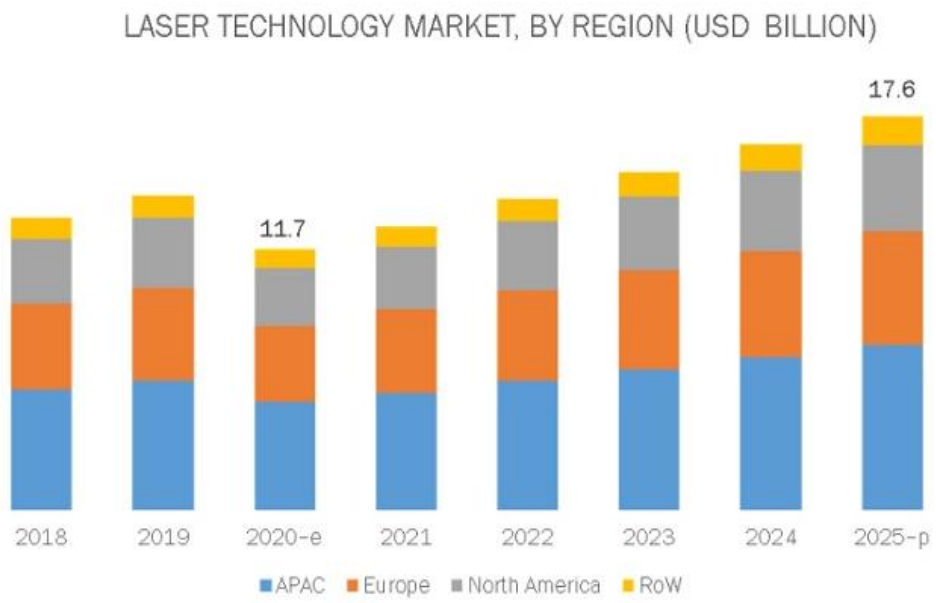

Figure 1.1: The laser technology market prediction by 2025 [11].

1.1.2 Vertical -Cavity Surface-Emitting Laser (VCSEL)

Vertical-Cavity Surface-Emitting Laser (VCSEL) is a type of semiconductor laser diode. Unlike the conventional edge-emitting semiconductor lasers, VCSEL emits the laser beam from the top surface. This type of laser was first proposed by Kenichi Iga in 1977 [12]. The resonator of the laser consists of two mirrors parallel to the wafer's surface. This double mirror structure forms a cavity. The active region usually consists of one or more quantum wells in the middle of the cavity and the generated photons are vertically confined in the cavity. The first VCSEL device was reported in 1979 by Haruhisa *et al* [13]. They fabricated an InGaAs/InP surface-emitting laser by liquid phase epitaxy (LPE) technique. This device was driven in pulsed mode at low temperature cooled by liquid nitrogen, it can emit a high-intensity light with a narrow spectrum and the threshold current is 800 mA. Professor Yasuharu Suematsu named it a surface-emitting laser, later called VCSEL to distinguish it from other surface-emitting lasers.

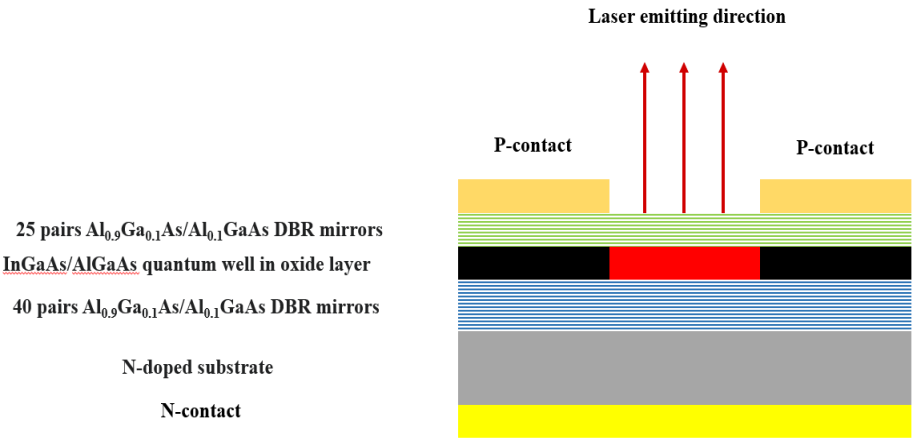

Figure 1.2: Schematic diagram of a GaAs based VCSEL.

The introduction of the quarter-wave mirror (which is also called the Bragg mirror) as a reflector can significantly improve the reflection of light at the interface. It is a dielectric mirror that consists of an alternating sequence of layers of two different materials. In 1986, the first VCSEL of GaAs/AlAs multilayer films was grown by metal-organic chemical vapour deposition (MOCVD) [14]. Until 1988, all VCSELs required a low temperature for operation. Fumio Koyama *et al.* first reported a continuous operation of the surface-emitting laser of a GaAs system at room temperature in 1988, which was a great breakthrough for the development of VCSEL [15]. This device has a threshold current of 23-30 mA, external differential quantum efficiency of about 10-20% and the laser output of about 1-2 mW. The structure of AlGaAs based distributed Bragg reflector (DBR) plays an essential role in the great success of GaAs based VCSELs. The alternating layer consists of two kinds of AlGaAs layers with different compositions. It can provide nearly 100% of reflectivity to confine the photons in the vertical direction. In addition, the lattice constant of the GaAs-AlGaAs does not change drastically with compositional changes that allow multiple lattice-matched epitaxial layers to be grown on GaAs substrates. Meanwhile, the AlGaAs DBR structure can also be used as a current path for p-type or n-type doping [16]. **Figure 1.2** presents a diagram of a simple VCSEL structure. InGaAs/AlGaAs quantum wells are grown between two $Al_{0.9}Ga_{0.1}As/Al_{0.1}Ga_{0.9}As$ DBR. These two DBR

mirrors are in different positions to form a total reflection mirror (99.9%) at the bottom and a partial reflection mirror on top. When a voltage is applied to the metal electrode of a GaAs laser diode, the quantum well will emit light with a specific wavelength which will be resonantly amplified by reflecting between two DBR mirrors subsequently. Since the partial reflection mirror is designed to transmit part of the laser, the high-energy laser will be emitted from the top surface of the device.

The structure of VCSEL is unique and has many excellent characteristics, such as (1) small size for ease of integration, (2) large output aperture, and high coupling efficiency with optical fibre, (3) small threshold current to reduce the power consumption, (4) higher inherent modulation bandwidth, (5) low test cost, etc. VCSEL has been widely used in data communication, optical sensor, face ID, laser printing, computer mouse and other fields [17]. With the promotion of data communication and mobile applications, the VCSEL market is expected to reach $3.3 billion in 2026 [18].

1.1.3 GaN based VCSEL

VCSEL technology was limited to red light and long-wavelength spectra for a long time. However, the development of VCSEL in the visible spectrum, especially in the short-wavelength range was relatively slow. The two main issues that hinder the development of short-wavelength VCSELs are as follow: First, the DBRs of the visible VCSEL require materials that have large refractive index difference and can be grown on the substrate directly. Moreover, the materials also need to enable the epitaxial growth of the short-wavelength active layer. In addition, it is challenging to grow an active gain layer with high optical quantum efficiency [19]. Consequently, until the early 1990s, there were only a few reports on short-wavelength VCSELs due to the lack of high-quality and low defect density direct-bandgap semiconductor materials with the emission wavelength in green, blue, and near-ultraviolet (near-UV).

Silicon carbide (SiC) and zinc selenide (ZnSe) are two materials which were used to fabricate short wave laser diodes (LDs) before the application of GaN. However, since

SiC has an indirect bandgap structure, the optical quantum efficiency of SiC-based LD is low. The highest reported optical quantum efficiency of a SiC-based LD is only about 0.03% [20]. Meanwhile, the motion of dislocation in the active region of ZnSe based optical devices creates the so-called dark-line defects (DLDs) which limit the lifetime of ZnSe based light emitting diodes (LEDs) or laser diodes [21].

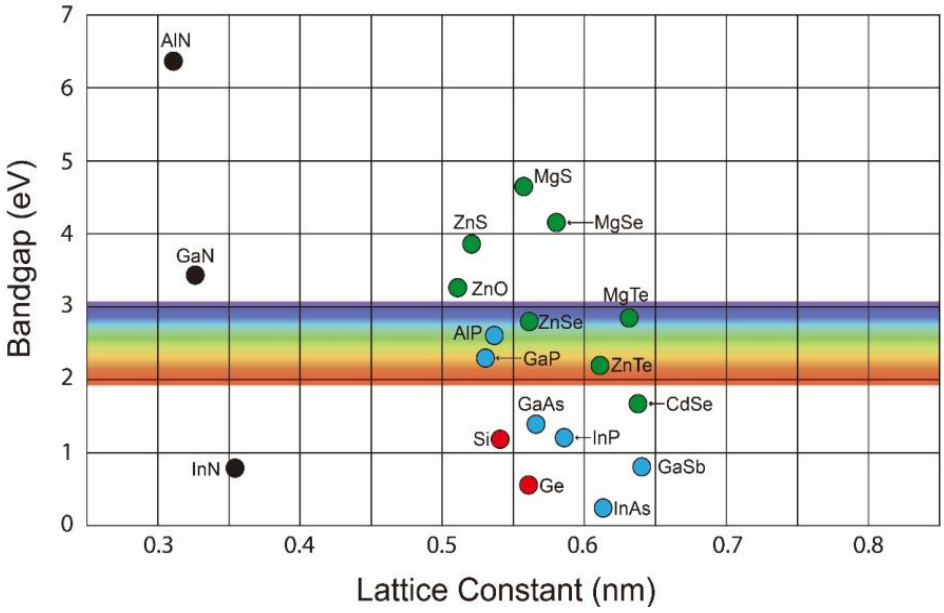

Figure 1.3: The bandgap energy and corresponding spectral wavelength of different materials at room temperature [22].

The family of III-nitride is made up of AlN, GaN, InN and their ternary or quaternary alloys. They are all direct bandgap semiconductor materials [23]. **Figure 1.3** shows the bandgap energy and corresponding spectral wavelength of different materials at room temperature. The bandgap of III-nitrides semiconductors and their ternary alloys covers from 0.7eV (InN) through 3.4eV (GaN) to 6.2eV (AlN) at room temperature. Thus, it is easy to get the entire spectrum by changing their alloy composition which is impossible for other materials like GaAs/GaP. In addition, III-nitride semiconductor materials show strong chemical, physical and thermal stability that enables III-nitride based devices to adapt to the harsh environment. Meanwhile, the III-nitride based devices present high breakdown voltage and high carrier drift saturation velocities.

Thanks to these advantages, the III-nitrides semiconductor is one of the ideal candidates for fabricating high-efficiency LDs.

Currently, the GaN-based VCSELs are still in the research stage. The main limitation of high-performance GaN-based VCSEL is the fabrication of GaN-based vertical cavities. By summarizing the previous work, the following three key factors are the research directions of GaN-based VCSELs [24].

1. DBR mirrors with high reflectivity.
2. Vertical structures in cavities.
3. Top DBR structure and optical confinements.

DBR mirrors with high reflectivity

Since the mirror is an important component that provides vertical confinement of photons, the mirrors in VCSEL are required to have extremely high reflectivity. Due to the limited amount of gain, the reflectivity of the mirrors needs to be higher than 99% to enable the laser operation. In addition, the narrower stopband of the DBR mirror is another concern. Since the refractive index difference of the periodic layers in III-nitride based DBRs is typically small, leading to a narrower stopband than arsenide, the stopband of DBRs needs to be tightly controlled within the laser wavelength [25]. At the same time, the low growth rate of III-nitride DBRs also limits its development [26]. This part will be discussed in detail in Chapter 5.

Vertical structure in cavities

The VCSEL structure consists of p-type space layer, n-type space layer, quantum wells and other intracavity layers. They are required to form a proper vertical structure in order to output the beam with a lower divergence angle. Thus, the design of cavity length, cavity mode wavelength and vertical position of antinodes and quantum wells

are essential. Unfortunately, it is still difficult to realize high quality epitaxial growth at a nanometer scale by MOCVD or vacuum deposition [27-33].

Top DBR structure and optical confinements

Most of the GaN-based VCSELs have a flat bottom mirror and there is no refractive index change in the lateral direction. Unlike the bottom DBR, the structures of the top DBR are in different shapes and categorize the propagation of laser. **Figure 1.4** is the schematic diagram of three different types that have been reported: concave [34, 35], convex [36] and flat [25, 37].

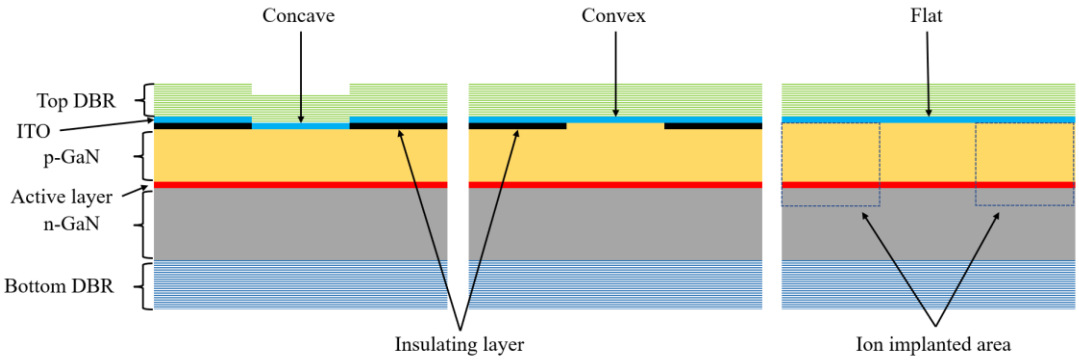

Figure 1.4: Schematic diagram of reported GaN based VCSELs with three different types of top DBR structure: concave, convex and flat configurations.

Concave top-side DBRs were used in the early stage of VCSELs. However, an anti-guiding cavity is formed in this structure and causes a significant diffraction loss [34, 35]. The GaN-based VCSELs with a flat configuration of the top-side DBR were obtained by aluminium-ion implanted apertures [37]. This type of DBR was reported to have a five-fold reduction than the concave structure in the threshold current of the device under pulsed injection. The convex structure of the GaN-based VCSELs was reported to enable the lowest threshold current and the highest output and efficiency [38-40]. However, the shrinkage in the aperture diameter causes scattering loss that decreases the threshold current density [28, 32, 36].

1.2 Distributed Bragg Reflector (DBR)

Distributed Bragg Reflector (DBR) is also known as a Bragg reflector or quarter-wave mirror. This is a simple one-dimensional photonic crystal with periodic structures. The periodic structures of the DBR consist of multiple layers with different refractive indexes to obtain an ideal reflectivity. The thickness of each layer generally needs to be equal to a quarter of the emission wavelength of the target light ($\lambda/4$), or more broadly, an odd multiple of a quarter wavelength. The light with a wavelength of λ will be strongly reflected due to the constructive interference caused by continuous reflections at each interface of the DBR.

Around 1940, G. L. Dimmick [41] and Mary Banning [42] proposed a multilayer Bragg mirror with alternating dielectric coatings. These dielectric coatings were soon used to fabricate high-quality cavities for early laser devices. With the development of epitaxial growth techniques such as Molecular Beam Epitaxy (MBE) and Metal-organic Chemical Vapor Deposition (MOCVD) in the 1970s, significant progress has been made in the precise growth of heterostructures. If the DBR structure layer can be grown together with devices such as LED devices, the fabrication process will be simplified. In 1982, Burnham *et al.* proposed the idea of introducing the DBR structure into LED devices to improve luminous efficiency [43]. In 1984, Thornton first reported the first high-quality DBR structure grown by MOCVD [44]. This is important for the subsequent fabrication of room-temperature continuous-wave operation of VCSELs in the infrared wavelength [45, 46]. Although the electrically-injected InGaN VCSELs have been reported since 2008 [47], the GaN-based VCSELs have not been commercialized until now. Nevertheless, it is recognized that the preparation of high-quality DBR mirrors, especially the DBR structure on the substrate side, is the critical part of GaN-based VCSEL technology. Unfortunately, it is still challenging to obtain a high-quality bottom DBR in GaN-based VCSELs. The design and fabrication of DBRs

are currently facing the challenges in materials, optical design and the influence of electrical and thermal conductivity.

1.2.1 DBR materials

The highly reflective DBRs of early VCSELs were achieved by depositing amorphous dielectric layers with oxide (SiO_2, HfO_2, and Ta_2O_5), nitrides (SiN_x) and fluorides (MgF_2) on the exposed active regions [48]. However, the DBR mirrors made by these materials have the disadvantages of a complex fabrication process, low quality, and high scattering losses in the dielectric layers. Moreover, these materials are usually insulating. Recently, the epitaxial growth III-nitride layers has been proposed for fabrication of high-reflective DBR structure. It can greatly simplify the manufacturing process of epitaxial DBRs. In addition, the epitaxial DBRs have better electrical conductivity and thermal conductivity which can improve the performance of VCSELs. However, there are four main challenges with the epitaxial growth of DBR mirrors. Firstly, when the DBR layers contain different elements (Al, Ga or In), the surface will become rough due to the difference in adatom diffusivity [49, 50]. Then, it is necessary to maintain the uniformity of compositions and thickness of each layer when employing ternary or quaternary alloys to manufacture the DBR structure [51-53]. In addition, the different growth conditions of the periodic structure will lead to a rough interface [54, 55]. Finally, the DBR's periodic structure with materials of different compositions will cause a large difference in lattice parameters between the constituent layers. So, a resulting tensile or compressive strain in the structure will lead to low quality of the epitaxial layers [56, 57].

1.2.2 Optical design of DBR

DBR mirrors exploit successive Fresnel reflection at normal incidence on the interface between alternating layers with different refractive indices, resulting in constructive interference of all reflection components and enhancing the accumulated reflections

(details in Chapter 2). Therefore, the shape of the reflection spectrum gradually tends to be a perfect rectangular spectral band and the reflection peak tends to 100% as the number of periodic increases [58]. For low-threshold VCSEL devices, it is very important to have a high reflectivity DBR (R>99.5%) in order to reduce the round-trip mirror loss. However, the refractive index difference between the layers of alternating material is usually tiny, requiring more pairs to obtain high reflectance. For example, $Al_{0.82}In_{0.18}N$/GaN DBR requires more than 40 pairs to get a peak reflectance higher than 99% [59]. This led to a significant extension of the DBR growth time introducing many undesired factors to the DBRs, such as surface roughness or thickness variation. On the other hand, the stopband of DBR must strictly correspond to the emitting wavelength of the active region. The reflection of DBR is more inclusive with a wider stopband. Therefore, the DBR structure with high reflectivity and wide stopband is very important for VCSEL.

1.2.3 The influence of electrical and thermal conductivity

Figure 1.5(a) is a schematic of a typical non-epitaxial DBR. As this type of DBR is usually fabricated by deposition of electrically insulating materials such as SiO_2/SiN_x, a particular lateral current injection scheme is required. However, this will increase the absorption loss of light. In addition, the thermal conductivity of the dielectric DBRs is usually very low (0.1~2W/mK), which causes the joule heat issue [60]. Compared with the non-epitaxial DBR, the epitaxial growth DBR has good electrical and thermal conductivity. Taking an AlGaAs/GaAs DBR as an example, its resistance can reach $10^{-3}\Omega$cm with a resistivity of 300W/mK [61, 62]. **Figure 1.5(b)** shows a schematic of VCSEL with epitaxial growth DBR structure. As shown, the current can be vertically injected into the gain region of the VCSEL. However, the stacking of alternating layers with different bandgaps in the DBR structure creates a potential barrier which inhibits carrier flow and increases the overall DBR resistance. Interfacial doping [63] and

interfacial alloy grading [64] are two solutions proposed for these issues, but these usually come with low reflectivity or thermal conductivity.

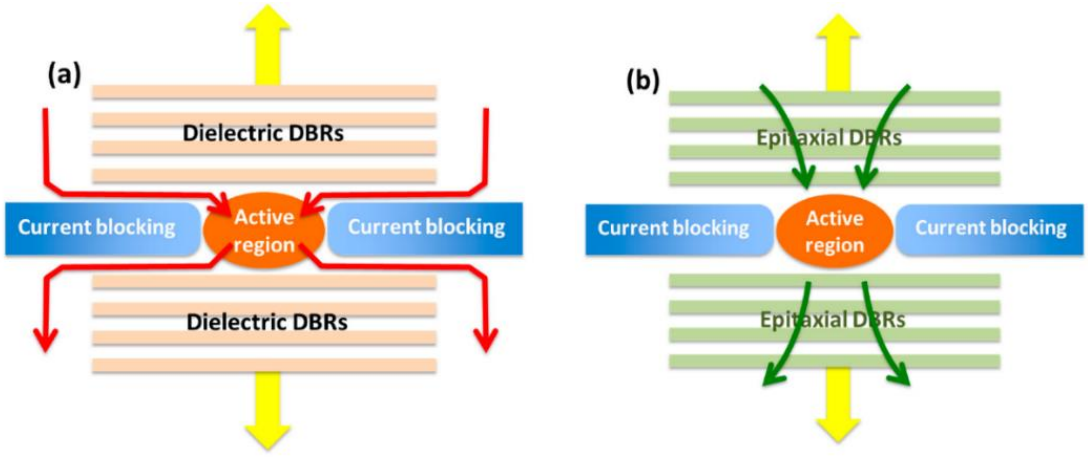

Figure 1.5. *Schematic illustration of VCSELs that employ (a) non-epitaxial DBRs (b) epitaxial DBRs. The red and green arrows represent the current injection pathways in these two different structures, respectively [58].*

1.3 III-nitrides material development

Among the III-nitride family, GaN plays an essential role in fabricating high-performance optoelectronic devices. Although Juza and Hahn first synthesized GaN in 1928 by using ammonia (NH_3) to pass through liquid gallium (Ga) at high temperature, this material is just GaN powder which can only be used to study the crystal structure of GaN [65]. The first single crystalline GaN film was reported by H.P Maruska and J.J. Tietjen in 1969 [66]. They flow ammonia gas to the gallium monochloride (GaCl) on a sapphire substrate at high temperatures. However, the GaN film grown by this method is inherently n-type doped with an electron concentration of 10^{19} cm^{-3} which may be attributed to a high density of nitrogen vacancies [67]. Germanium (Ge) were used for p-type GaN doping, but the uniformity is poor and has low reproducibility. In addition, the p-type GaN exhibited insulating or semi-insulating properties under such heavy doping concentrations. Therefore, the reported GaN-based LEDs were focused on metal-insulator-semiconductor (MIS) structure at that period [68, 69]. Until 1989, Amano *et al.* reported a conductive p-typed GaN with Mg-doped by low energy

electron beam irradiation (LEEBI) treatment [70]. Later in 1992, Nakamura *et al*. realized p-type GaN by thermally annealing Mg-doped GaN under nitrogen ambient [71]. The Mg-H complex formed during the MOCVD growth is broken under H_2 or NH_3 ambient and the free holes can be obtained [72, 73].

Improving the quality and morphology of GaN films is a great challenge for GaN-based devices. Due to the large lattice mismatch (16%) between GaN and sapphire substrate, the dislocation density of GaN films on sapphire is very high which hinders the development of GaN. Yoshida *et al.* introduced a two-step growth method in Molecular Beam Epitaxy (MBE) in 1983 [74]. This method grew an aluminium nitride (AlN) buffer layer before the GaN growth to reduce the lattice mismatch between GaN and sapphire. In 1986, Amano obtained a smooth morphology GaN film by applying a low temperature (LT) AlN buffer layer with a two-step growth method using MOCVD [75]. In 1991, Nakamura optimized the two-step growth by using LT GaN to replace the AlN buffer layer and achieved a GaN layer with high crystal quality [76]. Nowadays, the LT GaN or AlN buffer layer of the two-step growth method has already been widely employed for the high-quality GaN growth on sapphire.

Although there has been a tremendous development for III-nitride semiconductors and devices in the last 30 years which also led to the Noble Prize in Physics in 2014, the major achievement is still in the region of blue LEDs on conventional C-plane III-nitrides. The lack of an affordable substrate is a major obstacle to the future development of III-nitride devices.

Homoepitaxial growth on a bulk GaN substrate is the ideal substrate, especially for high brightness LEDs fabrication. The free-standing GaN substrates are typically grown via hydride-vapour-phase epitaxy (HVPE) and then been laser lift-off [77-79]. Due to the cost of this method being extremely high and limited size (typical $1*1cm^2$), the free-standing GaN substrates are only used for some regardless of cost purposes. The current economical method is the heteroepitaxial growth of III-nitrides on foreign substrates by

chemical reaction deposition methods (MOVPE and HVPE). Silicon carbide (SiC), sapphire and silicon substrates are wildly used for GaN heteroepitaxial growth. Compared with homoepitaxial growth, the heteroepitaxial growth of GaN on foreign substrate normally results in a high density of dislocations due to the large lattice mismatch between GaN and substrate materials. The dislocation density is typically on the order of 10^9 to 10^{10} cm^{-2} on sapphire and even worse on a silicon substrate.

Compared with sapphire and silicon substrates, SiC substrates have the highest thermal conductivity (4.9W/cm·K) with the smallest (3.5%) lattice mismatch [80]. So, the GaN grown on the SiC substrate exhibits the lowest dislocation density among all these three foreign substrates. It is especially suitable for the fabrication of high-power electronic devices [81]. However, the high price of SiC substrate makes it difficult for commercial application.

Sapphire substrate is much cheaper than SiC substrate and has highly stable chemical properties. In addition, the structure is hexagonal symmetry with a close matching thermal expansion coefficient that makes the sapphire substrate be the most popular substrate for III-nitride growth. However, the large lattice mismatch (16%) and low thermal conductivity (0.41 W/cmK) result in high dislocation density for the GaN growth on top [82]. Although the growth methods such as epitaxial lateral overgrowth (ELOG) are applied to improve the crystal quality of GaN, growth on sapphire still faces great challenges.

Silicon has an extremely mature technology after the development of nearly half a century as a traditional semiconductor material. The low cost and large substrate size available of silicon lead to a growing interest in the GaN growth on the silicon substrate. However, the (111) silicon has a 17% lattice mismatch with (0001) GaN and the thermal expansion difference is large as 115% [83]. A tensile stress produced during growth not only leads to high defect density but also makes the wafer bowing seriously and the epilayer cracking during the cooling-down process. Furthermore, silicon will also easily

react with gallium metal at high growth temperature and form a eutectic alloy [84]. This phenomenon will stop the growth of GaN. Therefore, the growth of GaN on Silicon still faces great challenges.

1.4 Nanomembrane lift off

The semiconductor nanomembrane can afford unique properties such as capacities for flexure [85,86], transparency [87-90], and strain-engineering from lattice mismatch [91-95], etc. The semiconductor nanomembranes are distinguished from bulk semiconductors most significantly by releasing them from their original substrate. The term nanomembrane here not only encompasses the films in nanoscale thickness but also continuous, self-supporting membranes that have properties independent of their supporting substrates. People have shown great interest in semiconductor nanomembrane and have applied these materials to many fields like heterogeneous integration and flexible electronic devices [86,96-98]. For heterogeneous integration, nanomembrane can be easily transferred to other substrates by trans-printing [96-98]. The flexible electronic devices on nanomembrane can conform to any shape and are bendable, twistable, and stretchable [86]. At present, various membrane materials have come out successively, such as silicon graphene [99], amorphous oxide [100], and III-V semiconductor materials [101, 102] etc. Among them, III-V nanomembrane has attracted much attention due to its huge market demand and maturity of technology for device fabrication.

The epitaxial lift-off (ELO) typically involves three steps: epitaxial growth of crystal structure on the original host substrate, separating with the original substrate, and transfer to a new carrier substrate. It is a recyclable way to reduce the costs by applying this non-destructive ELO process and reusing the original substrate. On the other hand, the light extraction of the LED devices will be improved effectively by removing the substrate [103]. Additionally, the device can be transferred to a new substrate with a better electrical or thermal conductivity. Meanwhile, flexible GaN electronic devices

are also a popular research topic. For example, Xin *et al.* exfoliated GaN-based HEMT from the original growth substrate by electrochemical selective etching on the n^+-GaN sacrificial layer and transferred the device to a polyethylene terephthalate (PET) flexible substrate [104]. The transferred membrane exhibited a decreased dislocation density and high saturation current of 105.67mA/mm under zero gate voltage. This HEMT also shows a low saturation current attenuation under the compressive state.

There are various methods to achieve ELO of GaN membrane. The laser lift-off (LLO) method uses a high-powered laser to vaporize the interface between GaN and sapphire [105]. It was widely used to separate GaN-based LED devices from sapphire substrate [106]. However, the LLO method involves bulky and expensive equipment which undoubtedly increases the cost. In addition, the laser used is typical with high power leading to a rough surface or breaking the membrane sometimes. Thus, this method cannot be commercialized due to the low yield and high cost.

In recent years, several groups reported that chemical lift-off of GaN membrane are achieved through a selective wet etching process [107-111]. The III-V semiconductor membrane structure is realized by applying a selective wet etching process such as chemical etching or electrochemical etching on the sacrificial layer, which will be broken to separate the membrane from the substrate. In contrast with other ELO methods, the selective wet etching process offers several advantages. Apart from ease of operation and low cost, this method enables the lift-off of devices on a membrane with large size [110, 111]. However, this method requires harsh acid treatment or high voltage. The electrochemical etching lift-off method even needs to introduce holes on the epitaxial wafer [111, 112]. Therefore, the challenge for the chemical lift-off method is to protect the effective area and keep the integrity of nanomembranes (NMs).

1.5 Motivation and Aims

It is accepted that the fabrication of DBR is a key component and bottleneck of semiconductor microcavities and VCSELs, especially for the bottom DBR on the substrate side. With the advance in epitaxial growth technologies for III-nitride semiconductors, the epitaxial growth of III-nitride based DBRs is replacing the dielectric DBRs. Since the air is the ultimate low-index media, the nanoporous based DBRs have attracted extensive attention recently. This type of DBRs can be simply fabricated by electrochemical etching and has higher optical performance. However, the mechanism of EC etching in DBR fabrication remains unclear. In addition, the development of nanoporous based DBR still needs to further improve the surface morphology and optical performance.

The semiconductor nanomembranes have various applications such as heterogeneous integration and flexible devices. Several techniques have exhibited capability for the membrane lift-off, for example, LLO, chemical lift-off, mechanical release, and electrochemical etching. However, the development of these techniques is limited to the involvement of expensive equipment or strong acid. Furthermore, the rough surface and small size are issues that need to be addressed for the development of III-nitride nanomembrane lift-off. Thus, it is significant importance to find a simple lift-off technique to peel off the III-nitride nanomembrane with high integrity, a smooth surface as well a large lift-off area.

The research presented in this PhD thesis aims to investigate the mechanism of electrochemical etching to fabricate nanoporous GaN-based DBRs and fabricate nanoporous GaN-based DBRs with better surface morphology and optical performance. The lateral electrochemical etching method and introduction of Al in n-type layers are two methods that are proposed to achieve the goals. In addition, the electrochemical etching method is also applied to the GaN on silicon sample to obtain a crack-free III-nitride membrane of large size.

1.6 Thesis Organization

This thesis consists of seven chapters as follows:

Chapter 1 gives a brief introduction, development, and challenges of III-nitride based DBRs, followed by current status of III-nitride membrane lift-off technologies. The motivation and aims of this project are also discussed.

Chapter 2 describes the background of semiconductors, in particular III-nitride semiconductors. Then, distributed Bragg reflectors are introduced. The fundamental mechanism of electrochemical etching and membrane is explored in detail.

Chapter 3 introduces the technical equipment employed to carry out the project, including sample growth, device fabrication and corresponding characterization.

Chapter 4 investigates the electrochemical etching results of GaN-based DBRs with different doping levels and bias voltages. In addition, a lateral electrochemical etching method is employed to improve the optical performance of DBR.

Chapter 5 investigates the effect on nanoporous GaN DBRs from adding a very small amount of aluminium in the heavily silicon doped GaN layer. This leads to better surface morphology and improve the optical performance of DBR.

Chapter 6 investigates lift-off of the III-nitride membrane by electrochemical etching. The detailed procedure of the membrane lift-off technique and the optical characterization of the membrane after lift-off are discussed in this chapter.

Chapter 7 provides a summary of this thesis and gives an outlook for the future plan.

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Chapter 2: Background

This chapter introduces the background of semiconductors, and development and challenges about III-nitride semiconductors. Specially, the distributed Bragg reflector is expounded in detail in terms of its theory and application. In addition, a conceptual study of electrochemical (EC) etching is presented at the end of this chapter.

2.1 Semiconductor

2.1.1 Semiconductor Theory

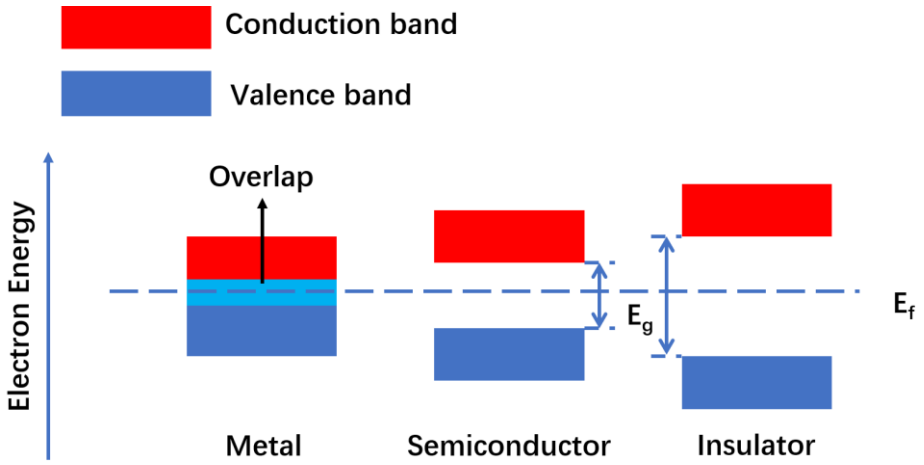

Figure 2.1: The bandgap structure of the metal, semiconductor and insulator. In the diagram, E_g is the bandgap energy, and E_f is the Fermi level.

In solid-state physics, the energy difference between the valence and conduction bands is the bandgap (E_g) of a solid-state material [1]. Solid-state materials are classified into three groups by their electrical conductivity, which are insulators, semiconductors, and conductors. **Figure 2.1** is a schematic of the band structure for these three different types of solid-state materials.

The electrons are difficult to be excited from the valence band to the conduction band for an insulator due to its large bandgap. Although the insulator will become a conductor when the external electric field is larger than a threshold, the electrons are

normally bound in the valence band and cannot move freely. So, the carrier concentration of the insulator is extremely low, and the electrical conductivity can be ignored. As for conductors, there is no bandgap between the valence band and conduction band. The overlap makes a part of electrons move freely, and then the current can flow at room temperature even without any further energy. The bandgap of semiconductors is between insulator and conductor. At room temperature, semiconductors have a larger conductivity compared to insulators. The thermal excitation allows many electrons to get enough energy to jump from the valence band to the conduction band and leave the same number of empty states in the valence band. These empty states are holes and also allow the electrons in the valence band to have the ability to move. When the electrons get energy equal to or larger than the material's bandgap, the semiconductor is conductive. In simple terms, the number of electron-hole pairs depends on the bandgap of the semiconductor. Therefore, a small bandgap leads to a high carrier density. Besides, the electrical properties of a semiconductor can also be changed by doping, light or electrical field. Thus, semiconductor materials are the most important materials for the application of amplification, switching and energy conversion.

2.1.2 Band structure of semiconductors

The semiconductor materials can be divided into direct bandgap semiconductors and indirect bandgap semiconductors [1]. **Figure 2.2** shows the band diagrams of a direct bandgap semiconductor and an indirect bandgap semiconductor. In a direct bandgap semiconductor (**Figure 2.2(a))**, the maximal energy state in the valence band is at the same crystal momentum (k-vector) with the minimal energy state in the conduction band. So, the electrons can recombine with the holes directly and emit photons without involving any third party to meet the conservation of the momentum for the transition. The recombination lifetime of direct bandgap material is relatively fast. As **Figure 2.2 (b)** shows, the maximal energy state in the valence band has a different k value with the minimal energy state in the conduction band of an indirect semiconductor.

Therefore, an extra momentum is required in the optical transition of electron-hole recombination to conserve momentum [2]. The involved phonon will convert into heat, leading to a longer recombination lifetime and reduced radiative recombination probability. The indirect bandgap materials hence have a lower optical efficiency than the direct bandgap materials. As a result of these considerations, the direct bandgap semiconductors such as gallium arsenide (GaAs) and gallium nitride (GaN) are more favourable for high-performance emitter fabrication than the indirect bandgap semiconductor like silicon (Si).

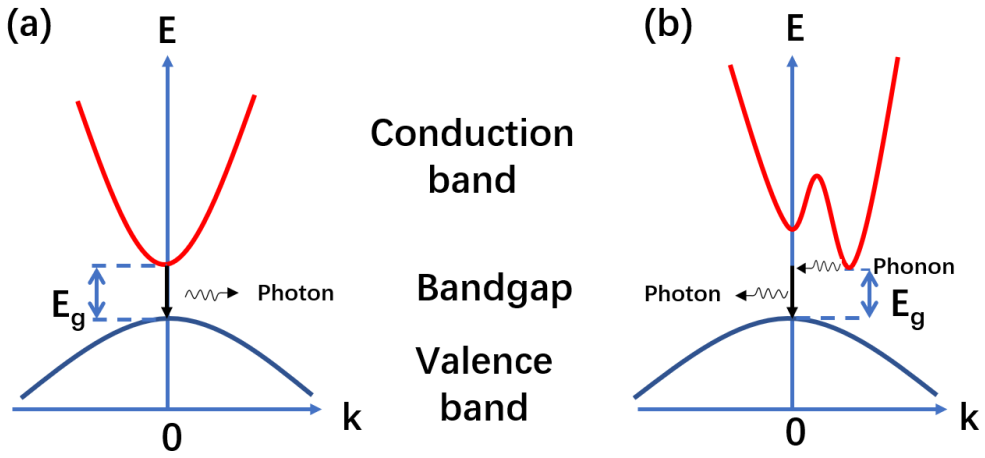

Figure 2.2: The band diagram of (a) direct bandgap and (b) indirect bandgap.

2.1.3 Doping

An intrinsic (pure) semiconductor is also called an undoped semiconductor or i-type semiconductor, which does not have any dopant species. So, the material properties determine the charge carriers in an intrinsic semiconductor and the electrical conductivity is caused by the defects or electron excitation. Doping introduces the impurities into an intrinsic semiconductor to change its electrical, optical, and structural properties. These introduced impurities generate additional free electrons or holes in the intrinsic semiconductor. The doped semiconductor can be divided into two types referring to the doping element. An n-type (donor) semiconductor has impurities that provide free electrons, and a p-type (acceptor) semiconductor is doped with impurities to provide free holes. For III-nitride materials, magnesium (Mg) is commonly used for

p-type doping where the Mg atoms will replace the gallium atoms and generate additional vacancies. On the other hand, Si atoms can occupy the substitutional position of Ga atoms and generate additional free electrons, leading to n-doped GaN.

2.2 III-nitride semiconductors

As mentioned in chapter 1, the research on III-nitride semiconductors and their alloys has become one of the most active scientific and technological development areas. It has unique properties like a wide bandgap, high saturated drift rate, high breakdown voltage, high thermal conductivity, and remarkable chemical and thermal stability, making the III-nitride semiconductors to satisfy the requirement of modern microelectronics and optoelectronics. This section will introduce the alterable bandgaps of III-nitrides and their crystal structures.

2.2.1 Crystal Structure

Unlike Si or germanium (Ge), compound semiconductors are composed of at least two elements, typically III and V group elements. III-nitride semiconductor family consists of gallium nitride (GaN), indium nitride (InN), aluminium nitride (AlN) and their alloys, such as AlGaN, InGaN and AlInGaN. The III-nitride semiconductor exhibits three different kinds of crystal structures depending on the atomic configuration: rock-salt, zinc-blende, and wurtzite [3]. The rock-salt type of III-nitride materials can only be formed under high pressures (for example: 52.2GPa for GaN [4]), but it is unstable under standardized ambient conditions [4]. It is worth noticing that the rock-salt type of III-nitrides cannot be obtained from the epitaxial growth method. The zinc-blended type of III-nitrides is in a metastable state. It can be grown on a cubic substrate such as Si, SiC, MgO, and GaAs [4-6]. However, the zinc-blend of III-nitrides has a trend of converting into the wurtzite structure as the latter is more thermodynamically stable.

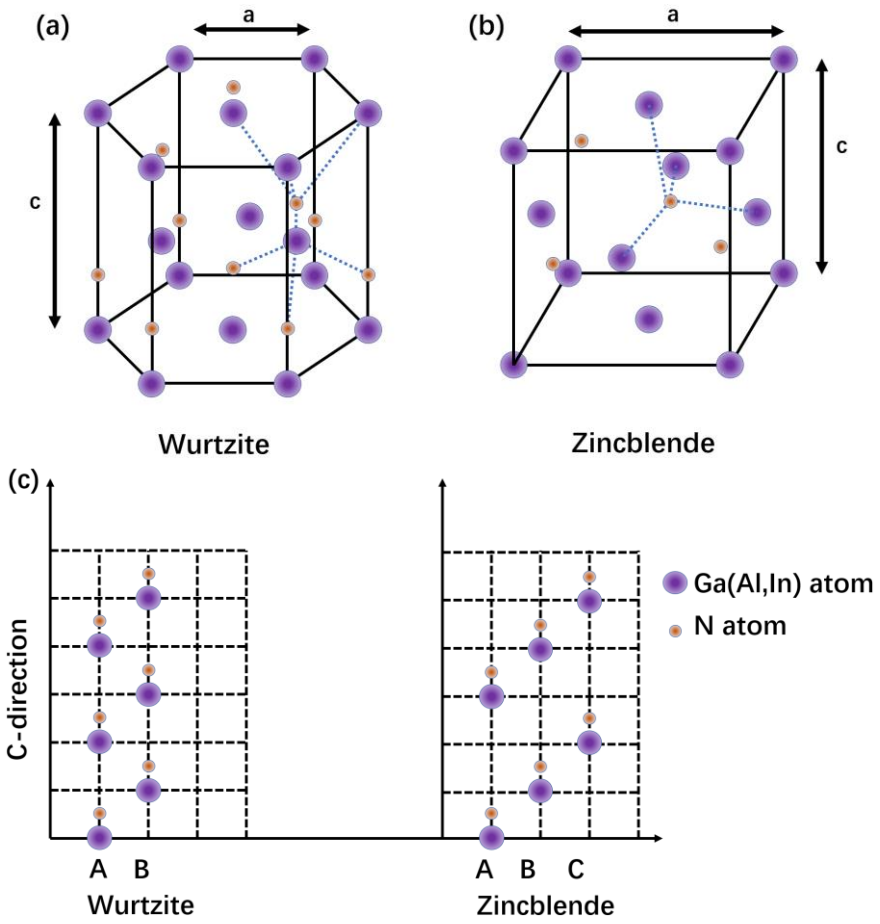

Figure 2.3: Schematic of III-nitride semiconductor with (a): wurtzite structure, (b): zinc blende structure and (c): corresponding stacking sequences.

Figure 2.3 (a) and **(b)** are atomic arrangements of III-nitrides with wurtzite and zinc-blend structures, respectively. Four N atoms in both structures surround each III-group atom (Ga, In, Al), and four III-group atoms also neighbour each N atom. However, the layer stacking sequences of these two structures are different. For the wurtzite structure, the stacking sequence along the c-direction (Vertical to the hexagonal basal plane) is in the order of AaBbAaBb. On the other hand, the atom stacking order in the zinc-blend structure is AaBbCcAaBbCc. These forms' capital and lowercase letters represent the III group element (Ga, In, Al) and nitrogen atom, respectively. The different letters (A, B and C) are the different atom positions. Each atom is surrounded by four adjacent atoms for both structures, but the difference is that the wurtzite structure is a hexagonal unit cell while the zinc-blende structure is a cubic unit cell. **Table 2.1** shows the lattice

constants of III-nitrides GaN, AlN and InN with wurtzite structures where ‘a’ represents the distance between two adjacent atoms on a basal plane and ‘c’ is the length of the unit cell [7, 8].

Table 2.1: lattice constants of GaN, AlN and InN

Material	Lattice constant ‘a’ (Å)	Lattice constant ‘c’ (Å)
GaN	3.189	5.185
AlN	3.112	4.982
InN	3.533	5.693

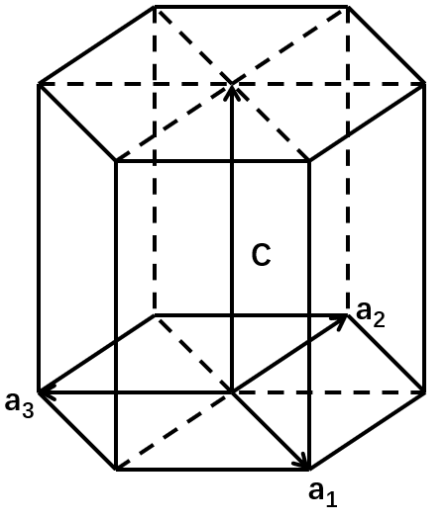

Figure 2.4: Bravais Miller indices in a wurtzite unit cell.

Miller indices (*h, k, i, l*) are introduced to describe the wurtzite structure's crystal planes and directions [9]. In **Figure 2.4**, the basal plane is divided into three equal areas. (a_1, a_2, a_3) are angled at 120 degrees to each other, and the indices (*h, k, l*) are the intercept reciprocals of them. *l* is the intercept reciprocals along the c axis. Because *i* is also equal to –(*h*+*k*) in the wurtzite structure, the hexagonal structure can also be denoted as (*h, k, l)*. Unlike the zinc-blend structure, the wurtzite structure is non-centrosymmetric, which

means it has two polar directions. C-plane (0001) represents the group III atoms on the outer surface plane. The Ga polar GaN typically exhibits a smooth surface, making it more practical for device fabrication. On the contrary, the -C-plane (000-1) is terminated with N atoms leading to a rough surface with hexagonal hillocks. The polarity of GaN means a lot of differences in chemical property, defect generation, impurity incorporation, etc.

2.2.2 Chemical and electrical properties of III-nitrides

The III-nitrides materials are now widely used in optoelectronics and power electronics due to their excellent chemical and thermal stability. **Table 2.2** lists some basic electrical and thermal properties of III-V group semiconductors.

Table 2.2: Semiconductor material properties at 300K [10-17].

Material	Electron Mobility ($cm^2V^{-1}s^{-1}$)	Electron Saturation Velocity (10^7s^{-1})	Breakdown Field ($kVcm^{-1}$)	Thermal Conductivity ($W{\cdot}cm^{-1}K^{-1}$)	Melting Point (˚C)
GaN	1245	2.5	5000	1.3	2500
GaAs	9400	2.0	400	0.55	1238
InP	4000	0.6	500	0.68	1062

The electron mobility characterizes how quickly carriers (electrons and holes) can move through a metal or semiconductor under an electric field. The scattering causes the electron mobility of semiconductors, such as phonons (lattice vibration), impurities and defects. Therefore, the higher scattering frequency in semiconductors leads to lower electron mobility. It's also one of good indicators of crystal quality. Since the substrate,

growth technique and growth condition influence the quality of GaN epilayer, the reported electron mobilities vary. Typically, the electron mobility of GaN epilayer is around 1000 $cm^2V^{-1}s^{-1}$. D. C. Look reported a freestanding GaN with the electron mobility of 1245 $cm^2V^{-1}s^{-1}$ which is the highest experimental data now [14]. Compared with GaAs and InP, GaN also shows its high electron saturation velocity and large breakdown voltage, making GaN-based devices a strong candidate for application prospects in semiconductors.

Meanwhile, GaN also exhibits high thermal conductivity and a high melting point. So GaN transistors can operate at higher temperatures. Furthermore, the chemical properties of GaN are strongly dependent on the polarity and crystal quality. For example, Ga-polar GaN exhibits high chemical stability that cannot be etched by the standard acidic or alkaline solutions [8]. On the contrary, N-polar GaN and the defects on Ga-polar GaN can be etched by various etchants such as phosphoric acid (H_3PO_4) and potassium hydroxide (KOH). In addition, n-type doped GaN can also be etched by EC etching. The EC etching is a common way to fabricate nanoporous structures and lift-off GaN nanomembrane. It is also the main method used in this thesis.

2.2.3 Alterable Bandgaps of III-Nitrides

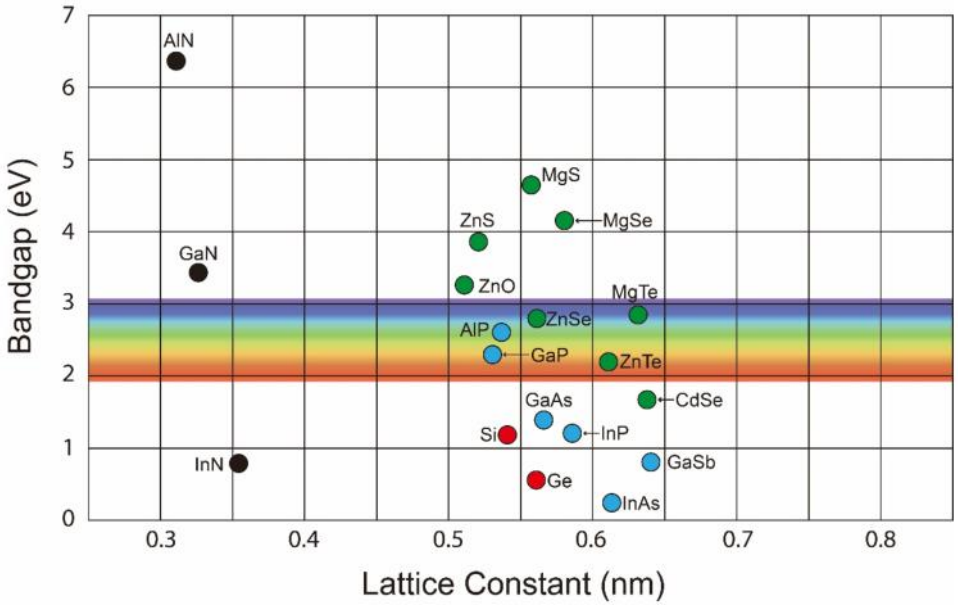

Figure 2.5: Bandgap of different materials VS lattice constant at room temperature [18].

Figure 2.5 shows the summary of important semiconductors in terms of energy bandgaps and lattice constants. It is worth noticing that the bandgap of III-nitride semiconductors (black spots) can cover a broad range spectrum from deep ultraviolet to infrared. The lattice constant of III-nitride alloys is in a linear relation with its alloy composition, which follows the Vegard's Law:

$$a_{A_xGa_{(1-x)}}N = xa_{AN} + (1-x)a_{GaN} \tag{2.1}$$

Here, a_{AN} represents the lattice constant of AlN or InN, a_{GaN} is GaN's lattice constant and x is the mole fraction of Al or In.

Similar to the lattice constants, the bandgap energy of ternary alloys is also related to the alloy composition. So, the emission wavelength of III-nitrides is alterable by modifying the proportion of Al, In and GaN in the ternary alloys. **Table 2.3** gives the bandgap and their corresponding wavelength of typical III-nitrides [19].

Table 2.3: Bandgap and emission wavelength of typical III-nitride materials.

Material	Bandgap (eV)	Wavelength (nm)
AlN	6.42	193
GaN	3.42	362
InN	0.78	1589

For the deep ultraviolet (DUV) to ultraviolet (UV) range, the emission wavelength can be adjusted by modifying the aluminium composition in AlGaN alloy. On the other hand, the InGaN alloy covers the near UV to infrared range by adjusting indium composition. In theory, the full spectrum of visible light (380-740 nm) is covered by InGaN. So, the III-nitride allays have good prospects for fabricating optoelectronic devices due to their tuneable wavelength and wide range spectrum.

2.2.4 Doping of GaN and its alloy

The un-doped GaN exhibits native N-type characteristics with a typical background carrier concentration of $10^{16}cm^{-3}$. Its dominant donor is considered to be nitrogen vacancy [20]. Si atoms can generate n-type doping by replacing the gallium site in the lattice and adding the required electrons [21]. The n-type doping of III-nitride semiconductor and its alloy (AlGaN, InGaN) is realized by controlling the flow rate of silane (SiH_4) or Disilane (Si_2H_6) during the MOCVD growth. Unlike the n-doped GaN, p-doped GaN has been difficult to achieve for a long time due to most potential acceptor materials being deep-level acceptors which hinders the growth of p-type materials [22]. The current mainstream dopant material is cyclopentadienyl magnesium (CP_2Mg) in order to replace the GaN site with divalent magnesium.

2.3 Distributed Bragg Reflector

2.3.1 Fresnel's Equation

Fresnel's equation is routinely used to design and fabricate optical coating of optoelectronics. It describes the light transmission and reflection when incident on the interface of two different media. The light will be partially reflected when it is incident on the surface of a material. The reflectance of the light is strongly dependent on the refractive index of two mediums which is shown in the following equation:

$$R = (\frac{n_1 - n_2}{n_1 + n_2})^2 \tag{2.2}$$

This equation is for the case of normal incidence where the incident angle is 0. R is the reflection coefficient n_1 and n_2 are the refractive indexes of two layers. Take Si as an example, the refractive index of Si is about 3.95 at 600nm. When a light incident from air to Si surface, R is around 0.355 which means 35.5% of light is reflected at the interface [23]. The reflection is called Fresnel reflection.

2.3.2 Photonic Crystal

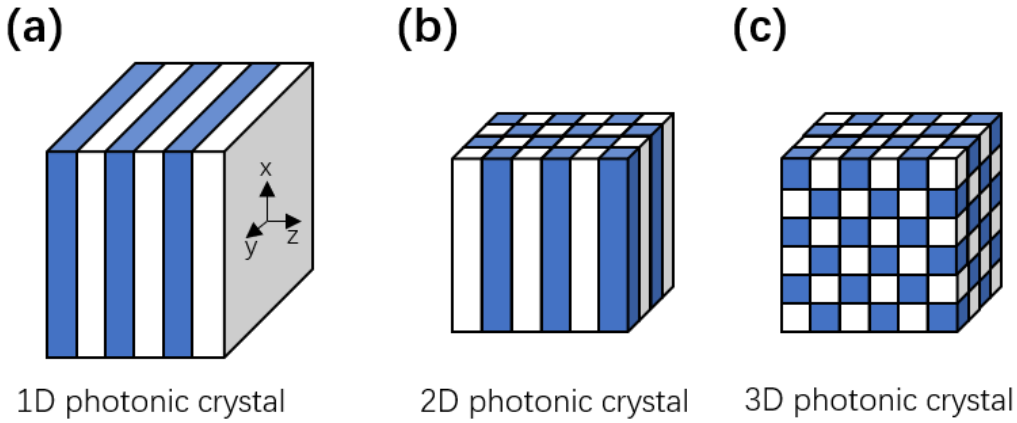

Figure:2.6: Photonic crystals in (a) 1D, (b) 2D, (c) 3D, D being the dimension.

Photonic crystals are special optical structures composed of dielectric, metal dielectrics and even superconductor microstructures or nanostructures. The natural world provides

a rich collection of examples, such as peacock features, fish scales or molluscs' eyes. In a photonic crystal, its optical structure's refractive index changes periodically and affects light propagation [24]. The most fundamental feature of photonic crystals is the photonic bandgap. This photonic bandgap means the waves within a certain wavelength are not possible to go through this periodic structure in the direction of refractive index variation. Conversely, a photonic crystal has a special band of frequencies that will reflect the light. This band is also called an optical bandgap or stopband. In theory, photonic crystals made of the non-absorbing dielectric can 100% reflect incident light in its designed wavelength [24]. So far, three different types of photonic crystal configurations have been proposed, namely one-dimension photonic crystal, two-dimension photonic crystal and three-dimension photonic crystal. **Figure 2.6** is the schematic diagram of 1-3D photonic crystals. 1D photonic crystals are the simplest structure that consists of periodic layers with alternating refractive index stacks. It can be fabricated by periodically depositing thin-film layers of different dielectric materials on a surface. Nowadays, 1D photonic crystal is widely used as dielectric mirrors or Bragg mirrors. 2D photonic crystals are reported to be produced by photolithography, self-assembly method or multiple-beam interference method [25]. It has been developed into hollow-core fibres or photonic crystal fibres, which have already been used in optical fibre communications, sensors, nonlinear devices, and other fields. However, 3D photonic crystals are still under study due to their difficulty in fabrication. In general, the research and fabrication of photonic crystals are extraordinary for optoelectronic semiconductor devices.

2.3.3 Distributed Bragg Reflector

A distributed Bragg reflector (DBR) is a simple example of a 1D photonic crystal. It consists of multiple thin layers of optical materials of alternating refractive indices, typically deposited on a substrate such as glass or silicon. **Figure 2.7** is a schematic illustration of the principle of the dielectric mirror. A layer with a high refractive index

(n_H) and a layer with low refractive index (n_L) form each cycle layer. The thickness of each layer is equal to $\lambda_{layer}/4n$, where λ_{layer} is the centre wavelength that the mirror is designed, and n is the refractive index of the layer. So, a DBR is also called a quarter-wave mirror [26]. By increasing the total number of n_H and n_L pairs of layers N, the reflectance also increases. The standard case is light incident onto the interface directly and will cause Fresnel Reflection at each interface.

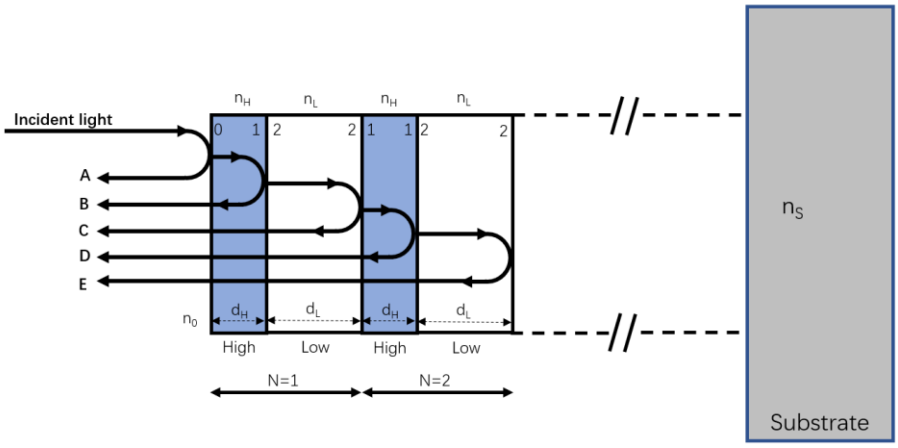

Figure 2.7: Schematic of the light propagation in distributed Bragg reflector.

The principle of the dielectric mirrors can be understood as **Figure 2.7** shows. The light in layer 1 is reflected at the 1-2 boundary, and the reflection coefficient r_{12} can be obtained from the Fresnel equations: $r_{12}=(n_H-n_L)/(n_H+n_L)$, which is positive due to that n_H is higher than n_L. The positive r_{12} indicates there is no phase change. When the light in layer 2 is reflected at the 2-1 boundary, the reflection coefficient is changed to $r_{21}=(n_L-n_H)/(n_H+n_L)$ and equal to $-r_{12}$. The difference between r_{12} and r_{21} indicates a π phase change. B and C in **Figure 2.7** are two reflected waves at two consecutive interfaces. Due to wave C travelling an additional two d_2 thickness which is equal to $2(\lambda_{layer}/4)$, that is π. Thus, the phase difference between B and C is 2π. Wave B and wave C interfere constructively. Therefore, it can be concluded that all waves reflected from the consecutive boundaries interfere constructively with each other. After several pairs (depending on the n_H/n_L) reflection, the reflected light intensity will be close to

100%. Due to the periodic variation of the refractive index in DBR, the reflectance is the same if the high and low layers are interchanged.

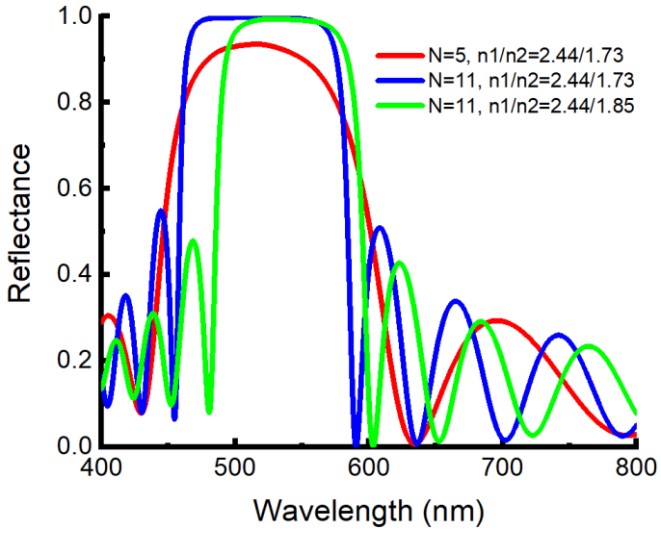

Figure 2.8: Simulation of the reflectance of three different DBR.

Figure 2.8 is simulated reflections of different DBR samples. The reflectance is almost 100% over a band of wavelength when DBR has a sufficient number of periodic layers. Conversely, this wavelength range within which there is very high reflection, is called reflectance bandwidth or stopband of the DBR samples. As the dielectric structure is a one-dimensional photonic crystal, the waves cannot propagate along the direction parallel to the surface [27]. The periodic structure can reflect light within the certain stopband. As **Figure 2.8** shows, two factors influence the shape of reflectance spectra. The number of periods layers N and the refractive index ratio of two different dielectric materials n_H/n_L. The maximum reflectance R for N pairs of layers in the air or free space is given by:

$$R = \left[\frac{n_H^{2N} - (\frac{n_0}{n_S}) n_L^{2N}}{n_H^{2N} + (\frac{n_0}{n_S}) n_L^{2N}}\right]^2 \tag{2.3}$$

Where n_0 is the refractive index of the incident material (usually air $n_0=1$) and n_s is the refractive index of the substrate. So, the reflectance R increases with the refractive

index ratio n_H/n_L; or put differently, the larger difference in the refractive index of two material results in more light reflected.

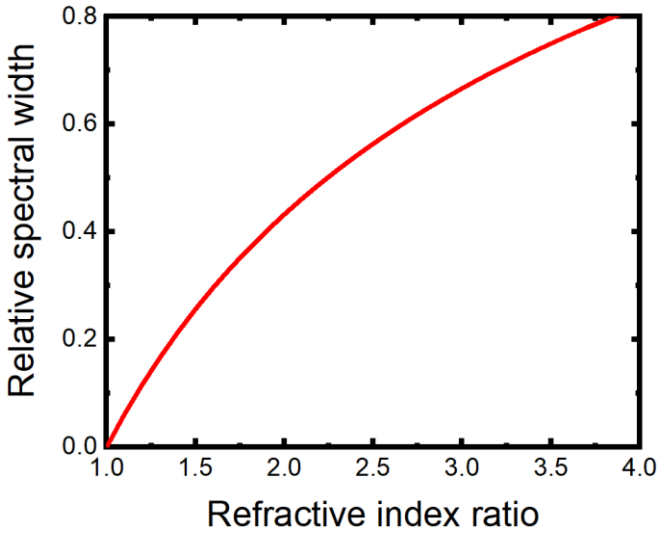

Figure 2.9: The relationship of reflective index ratio with relative spectral width

The relative spectral width $w = \Delta\lambda / \lambda_{layer}$ is given by:

$$\frac{\Delta\lambda}{\lambda_{\text{layer}}} = \frac{4}{\pi}\arcsin\left(\frac{n_H - n_L}{n_H + n_L}\right) \tag{2.4}$$

As **Figure 2.8** shows, the centre wavelength and stopband are different after the refractive index ratio changes. The relationship between relative spectral width and refractive index ratio can be more intuitively expressed as shown in **Figure 2.9**. For a DBR mirror with a large number of periodic layers, the bandwidth $\Delta\lambda$ of high reflectance zone for a DBR mirror increases with increasing refractive index ratio (n_H/n_L).

2.4 Electrochemistry

It is important to have a full understanding of electrochemistry for the DBR fabrication and nanomembrane lift-off. Electrochemistry is a branch of physical chemistry that focuses on the relationship between electric potential and chemical reactions. The basic principles of electrochemistry are oxidation and reduction. Since the 19th century,

electrochemistry has already been widely used in industry, such as battery technologies, electroplating, electropolishing etc [28]. Nowadays, as an important component of modern chemistry, the research and application of electrochemistry has made considerable progress. This part introduces the key principles and focus on the electrochemical etching of semiconductor.

2.4.1 Electrochemical Reaction and Potentials

The electrochemical reaction system consists of electrodes (electronic conductors) and electrolytes (ion conductors) [29]. The electrons and holes are the charge carriers between electrodes. While in the electrolyte, the charge is transferred to form ions. Therefore, the study of electrochemistry includes two aspects: the first is the electrochemical behaviour at the interface between the electrode and the electrolyte, and the other is the conductivity of the electrolyte, the ion transport properties and the balanced properties of the ions participating in the reaction [30]. Due to that the electrochemical reaction mainly occurs at the interface between the electrode and the electrolyte, and that the nature of the reaction on each electrode is different, it is therefore possible to construct a complete picture of the reaction in the entire system by studying the individual process.

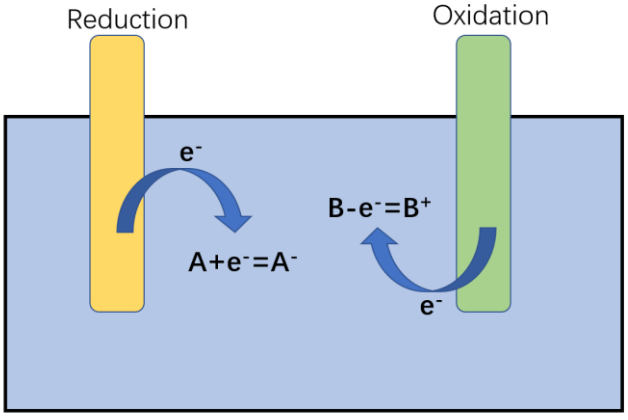

Figure 2.10: Schematic of reduction and oxidation reactions occurring at the electrode-electrolyte interface.

A standard cell system includes positive and negative electrodes and electrolyte solution. Due to the difference in the potential at the electrode-electrolyte interface, the two electrodes of the electrochemical reaction involve two half-reactions [30]. The standard hydrogen electrode (SHE) represents the potential difference required in the reaction, which is obtained by defining the standard electrode potential of hydrogen at any temperature as zero (E^0) and comparing any other electrode potential with the standard hydrogen electrode potential at the same temperature. As mentioned earlier, the electrochemical reaction involves two half-reactions: oxidation and reduction. Oxidation is the process of the reducing agent losing electrons and being oxidized, while the reduction is the process that the oxidant gains electrons and is reduced. **Figure 2.10** describes the oxidation and reduction reactions in electrochemistry. The charge of the system has not changed. In the process above, the electrode itself may dissolve or corrode which is the basic principle of achieving EC-etching. Since the electrochemical reaction is affected by the potential difference, the total potential of the cell can be obtained from two half-reactions [30]. **Figure 2.11** is an example of the Daniel cell. It is a typical electrochemical cell with two electrodes of zinc and copper, and the electrolyte containing both zinc and copper ions. The reactions are given as below [30]:

Overall: $Zn + Cu^{2+} \rightarrow Zn^{2+} + Cu \qquad E^0 = +0.34 - (-0.76) = 1.10V$

Left: $Zn \rightarrow Zn^{2+} + 2e^- \qquad E^0 = -0.76V$

Right: $Cu^{2+} + 2e^- \rightarrow Cu \qquad E^0 = +0.34V$

Equation 2.5: Illustration of simple electrochemical cell reaction with potentials.

Due to the two half-reactions will not occur independently of the other, a salt bridge or porous disc is required between them to allow ions to move freely. The total cell potential is the potential difference between the two involved reactions. So, determining the two half-equations is important for further analysing the cell potential of electrochemical reactions. In the left half-cell, an oxidation reaction occurs. The zinc

electrode is oxidized and generates two free electrons. This equation is in the potential of -0.76V. In the right half-cell, a reduction reaction occurs. The Cu^{2+} in the copper sulfate ($CuSO^4$) gets two electrons and is restored to copper. The potential in the right half-cell is 0.34V. Thus, the total potential is 1.10V and the electrons move from the zinc electrode to the copper electrode.

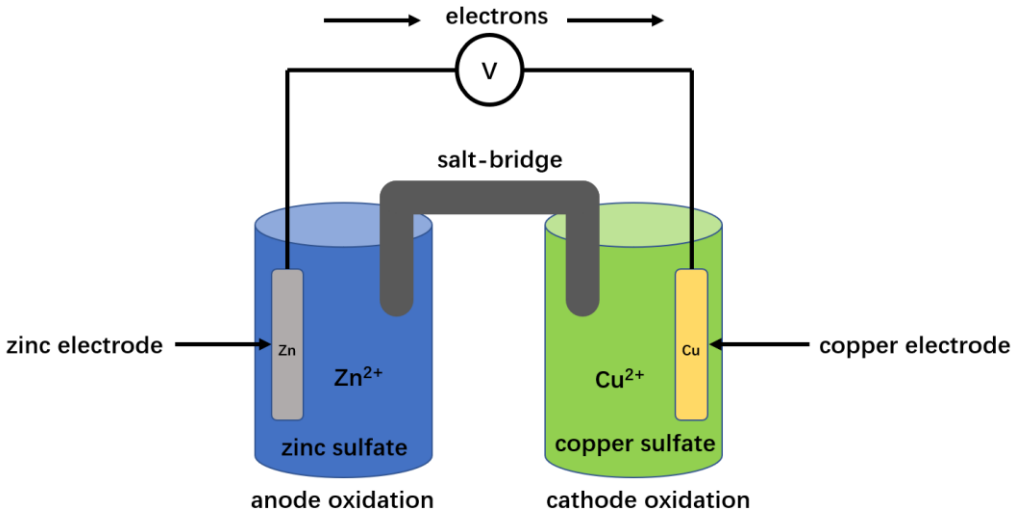

Figure 2.11: Schematic of a Daniel cell.

2.4.2 Semiconductor-Electrolyte Interface

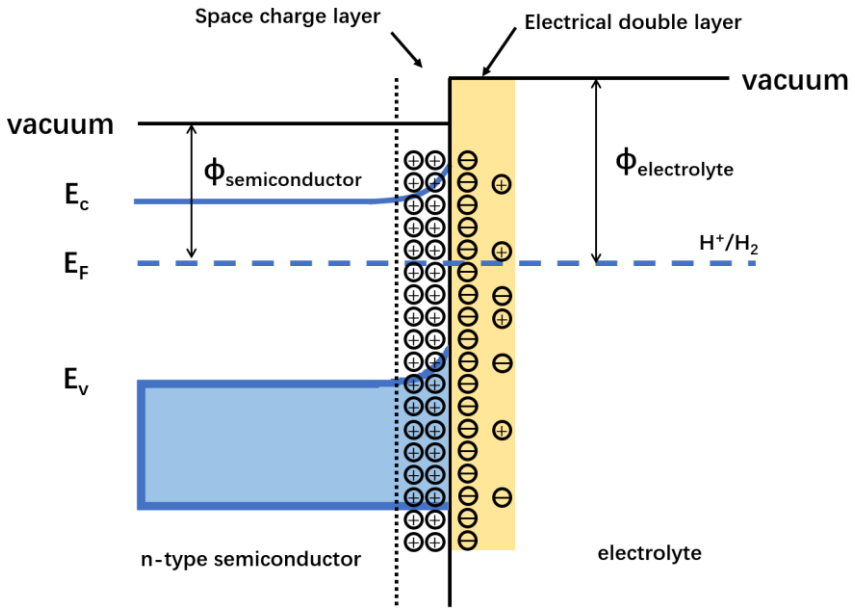

Figure 2.12: n-type semiconductor-electrolyte junction after contact.

Due to the different work functions of semiconductor and electrolyte, a carrier diffusion at the interface is formed once the semiconductor contacts with an electrolyte. Therefore, a built-in electric field is generated at the interface. The diffusion of the charge carrier stops when the Fermi energy level in the semiconductor is equal to the redox potential of the electrolyte. **Figure 2.12** shows the schematic of the interface between the n-type semiconductor and the electrolyte. An electrical double layer (also called the Helmholz layer) is formed at the side of the semiconductor to the electrolyte. The first layer consists of ions absorbed into the semiconductor by the chemical interactions, and the second layer is formed by the ions attracted via Coulomb force [31]. Meanwhile, a space charge layer is formed at the side of the semiconductor due to the built-in electric field. The band bending and charge transfer take place in this region. Similar to a P-N junction, the thickness of a space charge layer in this system depends on the doping level of the semiconductor, and the thickness of the electrical double layer depends on the concentration of ions in the electrolyte.

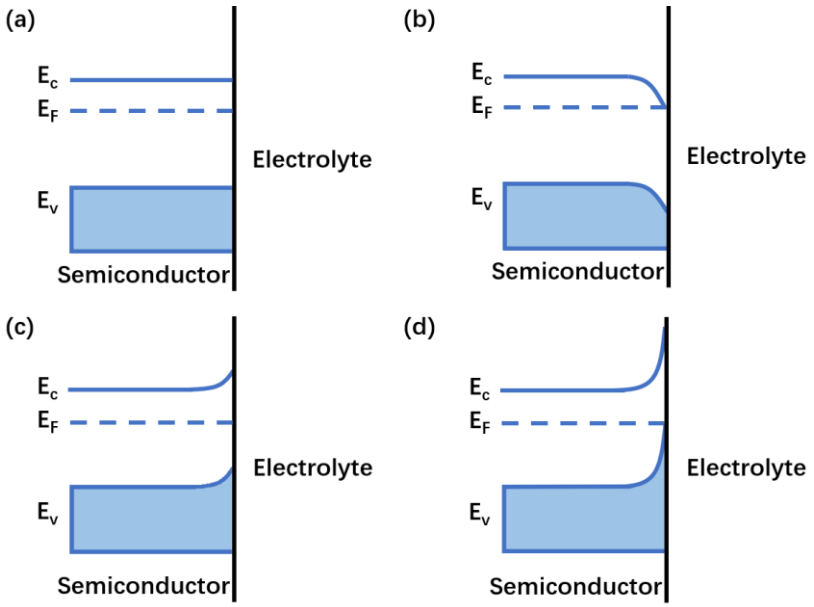

Figure 2.13：Band structure of n-type semiconductors in electrolyte (a) semiconductor Fermi level equal to the redox potential (b)semiconductor Fermi level smaller than redox potential (c) semiconductor Fermi level higher than redox potential (d) semiconductor Fermi level much higher than redox potential.

The doped semiconductors are usually used as electrodes for the electrochemical reactions, so the band bending depends on whether the semiconductor is n-type or p-type doped. The semiconductor and the electrolyte properties determine the change in the surface potential of the contact surface. Therefore, the doping level of the semiconductor and the ion concentration of the electrolyte affect the change in the surface potential. **Figure 2.13** shows the different situations of the interface between n-type semiconductor and electrolyte. **Figure 2.13(a)** represents a flat band potential (E_{fb}) which has equal redox potential and Fermi level of the semiconductor, so the energy band is not bent and there is no net charge transfer. In **Figure 2.13(b)**, the Fermi level of a semiconductor is lower than the redox potential due to the electron injection and forms an accumulation region, forcing the band to bend downward [30]. The accumulation region will cause an excess of the majority carriers at the interface, leading to a metallic-like behaviour. **Figure 2.13(c)** describes the formation of the depletion layer. In this situation, the Fermi level of the semiconductor is higher than the

redox potential of the electrolyte and the electrons flow into the electrolyte leaving a positive charge behind. A depletion region is formed on the surface of the semiconductor and forces the band to shift upward. Electronic transfer is restricted due to the lack of charge carriers. When applying a significant force to the system, the electrons can be extracted from the electrode's valence band to the conduction band and form an inversion layer (**Figure 2.13(d)**). The n-type semiconductor will be converted to p-type at the interface due to the excessive removal of electrons on the surface of the semiconductor [30]. Therefore, there must be enough carriers for effective charge transfer processes. Among them, the n-type electrode accumulates electrons to cause a reduction reaction, and the p-type electrode accumulates holes to cause an oxidation reaction. **Figure 2.13** describes the energy band relationship between the n-type semiconductor and the electrolyte interface, while the p-type semiconductor is the opposite.

2.4.3 Electrochemical etching of III-nitride

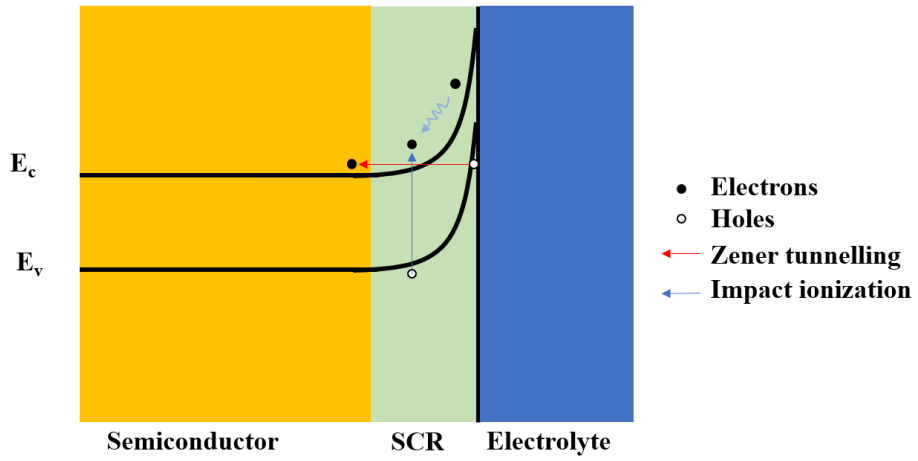

Figure 2.14: Energy band diagram of the GaN/electrolyte interface.

The introduction of semiconductor electrochemistry provides a basic understanding of the principle involved in EC etching. Due to that the nitride semiconductors exhibit strong chemical stability. It is hard to etch them via normal wet etching [32]. The Dry etching processes such as Reactive Ion Etching (RIE) can only be used for top-down etching [33]. Therefore, EC etching is a unique method that can fabricate a wider range

of possible morphologies. The application of EC etching on semiconductors is not new, which has been used to manufacture porous silicon since 1950 [34]. However, it had not received widespread attention until when Leigh Canham published a report on the luminescence of porous silicon fabrication in 1990 [35]. Different from silicon, nitrides are highly inert and the properties are much less affected by surface state [36, 37]. EC etching and photo-enhanced electrochemical (PEC) etching have already been developed as the main methods for manufacturing porous nitrides or polishing the nitrides [38-41].

EC etching Process.

A basic EC etching system set-up consists of the following units:

1. Sample, connected as an anode.
2. Inert electrode, as the cathode connection, usually platinum (Pt) pad.
3. Electrolyte, forming an ion transmission path between the electrodes.
4. Voltage source or current source.
5. In the case of PEC etching, A UV lamp is required to illuminate the sample.

The detailed introduction of the system will be described in Chapter 3. Different electrolytes, voltage, and doping levels will influence the nitride semiconductor in EC etching and produce different morphologies [42]. Based on the previous studies of qualitative and phenomenological aspects of etching, several theories have already been proposed. For example, the etching process for nanoporous or electropolishing can be described as a cyclic four-step process. (a) free charge carrier holes are generated on the interface of semiconductor and electrolyte, (b) hole assisted the oxidation, (c) oxidation products dissolve in the electrolyte, (d) transportation of the products and reactants [42]. Take the EC etching of GaN as an example, the oxidation process of GaN is an electrochemical reaction driven by holes. The function is shown as [43]:

$$2GaN + 6h^{+} \rightarrow 2Ga^{3+} + N_2 \uparrow \tag{2.6}$$

The Ga^{3+} ion in the reaction is movable in the electrolyte. This view is generally accepted as the mechanism of EC etching of nitrides in EC etching and PEC etching [44]. Some reports also conclude that Ga_2O_3 will be formed first and then react with the electrolyte, since the GaN surface will be oxidized and the oxide is not dissolved when pure water is used as the electrolyte [45]. However, for nitric acid and nitrate electrolytes, the gallium nitrate produced is soluble. It can be seen from this equation that free holes drive the etching process. In the case of PEC etching, the irradiated ultraviolet light will generate electron-hole pairs. These generated holes will be collected at the nitride/electrolyte interface by the applied electric field and an etching reaction occurs [46]. Unlike the PEC etching, the EC etching does not require any additional ultraviolet light. So, there are no photogenerated carriers in EC etching. Two other ways are applied to generate holes in n-type semiconductors: Zener tunnelling and impact ionization. The energy band diagram of the GaN/electrolyte interface is shown in **Figure 2.14**. The space charge region (SCR) is very thin when the doping level is high enough. The band bending caused by the negative potential applied at the electrolyte interface is large enough for the valence band at the interface to reach a higher energy level than the semiconductor's conduction band. Therefore, the electrons can tunnel from the valence band of the interface into the conduction band of the semiconductor and leave free holes. This phenomenon is Zener tunnelling. At a low doping level, the SCR is large. Therefore, the impact ionization occurs under a larger electric field. Unlike the Zener tunnelling, highly energetic electrons in the conduction band will collide with a valence band electron and generate an electron-hole pair by losing its kinetic energy [47]. The large SCR provides sufficient distance for the carriers to be accelerated by the electric field. Meanwhile, both the EC etching and PEC etching are conductivity-selective etching methods. There will be no electric field at the interface if the electrical conductivity of the semiconductor is insufficient. No holes will be injected into the surface and no etching occurs. Therefore, since an undoped layer can be used to stop the EC etching, it is useful for fabricating highly reflective distributed Bragg reflectors to alternately grow Si-doped/un-doped structures. Due to

the challenges of high conductivity and effective p-type nitride doping, nearly all the currently reported porous nitride materials are n-doped.

In electrochemical etching, the etching results depend on the doping level and bias voltage and can be summarised into three different types. With a low doping level or bias voltage, the GaN layer cannot be etched. Then, the porous shows the increasing doping level or bias voltage. The result of “polishing” means the sacrificial n-doped GaN layer is completely etched and no more n-doped GaN is left. The polishing result in this project means the DBR structure is removed since there is not enough support for the un-doped GaN layer.

2.5 Membrane lift-off

The development of electronic technology focuses on the miniaturization of circuitry to integrate more components and improve the performance of the devices [48, 49]. In addition to reducing the lateral dimensions, the membrane structures also provide a new perspective for this research. Compared with bulk materials, semiconductor nanomembranes have many advantages, including capacities for flexure [48, 50], transient construction with tuneable paths of degradation [51, 52], transparency [53, 55], strain engineering from lattice mismatch [46,60], transportable of the substrate, and tuneable bandgaps via quantum confinement effects [61-63]. These functionalities provide a pathway for the manufacture of next-generation electronic and optoelectronic devices. In recent years, various electronic materials have been fabricated in nanomembrane structures. Such as silicon [64-66], III-V group materials [67, 68], graphene [69, 70], and polymer [71]. Three different methods have already been applied for preparing the nanomembrane materials: direct growth, mechanical release, and chemical lift-off. However, the direct growth of 2D nanomembrane is subject to extremely high cost and immature technology. Mechanical and chemical exfoliations are currently common methods of nanomembrane fabrication [61, 63, 72-74]. Samples will be first grown by chemical methods, then connected to a supporting substrate, and

finally processed to a very low thickness by methods including etching, polishing or selective cutting [53, 75-77].

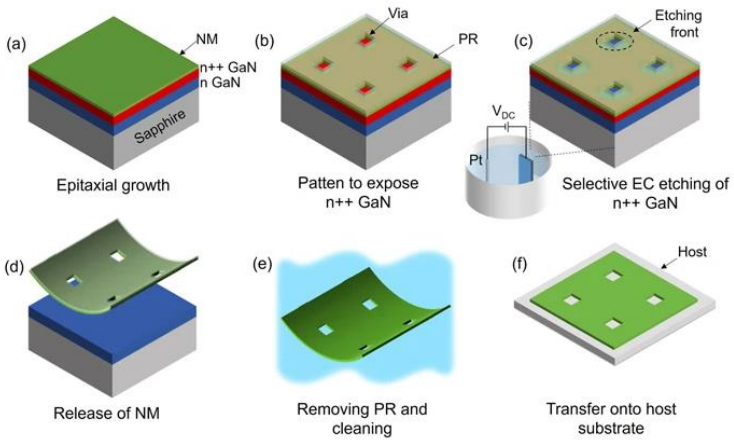

Figure 2.15: Schematic of the fabrication process of III-Nitride NM. (a) Epitaxial grow III-Nitride NM on heavily doped n^{++}GaN layer, (b) Dry etch window to expose n^{++} GaN sidewalls, (c) selective EC etching of n^{++}GaN layer, (d) separate NM from the epitaxial wafer, (e) remove photoresist and clean NM, (f) transfer NM onto a new host substrate. [78].

Wet etching is a typical chemical processing and has also been used to prepare nanomembrane materials in recent years. The separation of the nano-film and the substrate is achieved by removing the sacrificial layer [77, 79-89]. **Figure 2.15** is an example of the III-nitride nanomembrane fabrication process [78]. The required nanomembrane structure is epitaxially grown on a heavily doped n^{++}-GaN sacrificial layer by MOCVD. Then, a window is dry-etched to the low doped n-GaN current spreading layer to expose the sacrificial layer completely. After the EC etching fully polishes the sacrificial layer, the nanomembrane is separated from the original host substrate. Finally, the stripped nanomembrane is transferred to a new host substrate. Semiconductor nanomembrane has shown exciting potential in fabricating electronic and optoelectronic devices. Currently, the high-quality semiconductor nanomembrane materials have many successful application cases, such as the preparation of flexible,

wearable electronic devices, bioelectronics integration, spintronics and quantum devices, transparent optoelectronic devices, and nano-electronic devices.

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Chapter 3: Equipment

A series of technical equipment are employed to carry out the whole research project. These types of equipment include the steps of template fabrication, epitaxial growth, device fabrication and corresponding characterization. This chapter presents a detailed description of all the techniques for understanding the operation and functional perspective essentially.

3.1 Metal-Organic Chemical Vapour Deposition

Metal-Organic Chemical Vapour Deposition (MOCVD) is the main epitaxy equipment employed in this project to grow on (0001) sapphire substrate or silicon substrates. It is also called Metal-Organic Vapour Phase Epitaxy (MOVPE) or Organometallic Chemical Vapour Deposition (OMCVD) or Organometallic Vapour Phase Epitaxy (OMVPE). MOCVD is now widely supplicated for the semiconductors industry or research due to high-quality epitaxial layer growth and reproducibility. The thickness and composition of the epi-layer are controlled precisely is another advantage for MOCVD growth. There are three types of MOCVD systems which are commonly used for epitaxy growth: high-speed rotation vertical reactor [1], planetary rotation horizontal reactor [2], and close-coupled showerhead (CCS) reactor [3]. **Figure 3.1** are two MOCVD systems in our group. Aixtron 3×2” flip-top CCS system is used for the growth of GaN-based DBR structure and a Thomas-Swan 3×2” vertical CCS system is used for the growth of GaN-based template structure.

Figure 3.1: Images of MOCVDs (a): Aixtron 3×2" flip-top CCS reactor; (b): Thomas-Swan 3×2" vertical CCS reactor.

As **Figure 3.1(b)** shows, the MOCVD system consists of two control panels, gas delivery cabinet, metal-organic (MO)bubbler cabinet reactor cabinet, in-situ laser monitoring system, load lock chamber and electrical distribution part. Additionally, gas purifiers, two cooling water systems and exhaust systems are not shown in the picture. H_2 is purified by pathing through permeation of a heated palladium (Pd) membrane and N_2 is purified by chemical gettering to remove impurity (moisture, oxygen and CO_2) [4]. During the growth, the purified H_2 and N_2 are sent into the MOCVD system as the

carrier gases for metal-organic sources. Due to H_2 is much better purified, it is used for most of the growth. N_2 is only used for InGaN quantum well (QW) because InGaN incorporation is unfavourable at H_2 ambient.

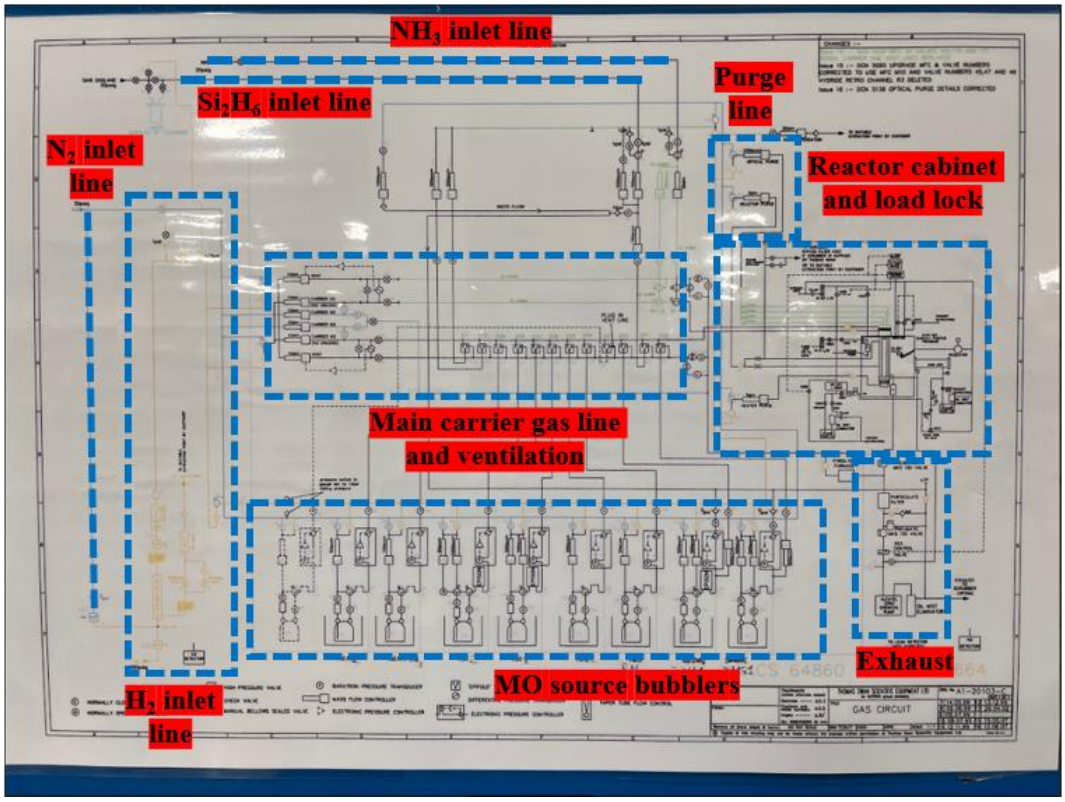

Figure 3.2. Schematic gas circuit of MOCVD gas delivery system.

Ammonia (NH_3), Trimethylgallium (TMGa), Trimethyaluminium (TMAl), and TrimethylIndium (TMIn) are the group V precursors for growing GaN epitaxial layers. In addition, dilute silane and bis(cyclopentadienyl)magnesium (Cp_2Mg) are employed as n-type dopant and p-type dopant respectively. These group V metal-organic sources are stored in the bubblers as **Figure 3.2**. During the growth, the carrier gas will flow from the bottom of the bubblers and bring the metal-organic source into the reactor. Ultra-pure NH_3 (99.99999%) and Si_2H_6 are supplied from the cylinders outside of the gas system. In our MOCVD system, there are 2 separate gas lines to carry group V precursor and group III precursors so that they can't react before entering the reactor. The metal-organic source and hydride precursors are then injected into the growth

chamber through a showerhead to avoid jetting or turbulence. In addition, this showerhead and the stainless-steel chamber are designed with a water-cooling system due to the high temperature during growth. The reactor is completely sealed with the outside by a double O-ring mechanism and makes sure there is not any gas leakage. A SiC-coated graphite susceptor is just below the showerhead for wafers loading. It has three 2-inch pockets that allow three samples to be grown with the same growth condition in a single run. The temperature system is constituted by three independent heating zone as **Figure 3.3**. By adjusting the power supply unit (PSU) on the heater, the temperature on the susceptor is achieved with very good uniformity. The growth pressure is controlled by a dry pump. There is an in-situ interferometry monitoring system on the top of the reactor that can monitor the real-time surface temperature and wafer curvature during the epitaxial growth.

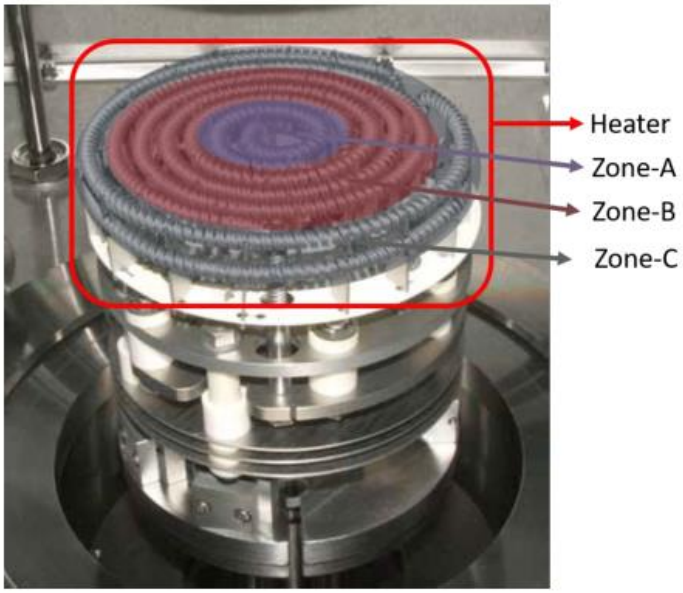

Figure 3.3: Image of heater (Modified from [5]).

3.2 Fabrication Technique

Sample Cleaning

A standard cleaning procedure is employed to remove any contaminants, residual dust, or particles on the surface of the sample before any further overgrowth and device fabrication. These standard cleaning steps include:

1) Solvent Cleaning: Immerse the sample in order of n-butyl acetate (nBA), Acetone, and Isopropyl alcohol (IPA). This step should take place in the ultrasonic bath.
2) Rinsing the sample with deionized water to remove the solvent residual.
3) Remove the water stains with the clean and dry nitrogen and bake the sample on the hot plate at 100℃ to de-moisturization completely.

3.3 Thin film deposition

3.3.1 Plasma Enhanced Chemical Vapour Deposition

Plasma Enhanced Chemical Vapour Deposition (PECVD) is one of the powerful equipment to deposit dielectric film such as SiO_2 or SiN with plasma. Compared with standard (CVD), the utilization of plasma in PECVD leads to lower operation temperature with high-quality dielectric film (standard CVD with 800℃). As shown in **Figure 3.4(a)**, the reactant gases are fed into the reaction chamber with two parallel electrodes during the deposition process. The grounded electrode is on the sample stage where the radio frequency (RF) energized electrode is on the top of the chamber. The reactant gases are excited into plasmas via capacitive coupling between these two electrodes. Meanwhile, the sample is heated to 300℃. The gas mixture which contains atoms, molecules, ions and radicals will form required dielectric films by chemical reactions.

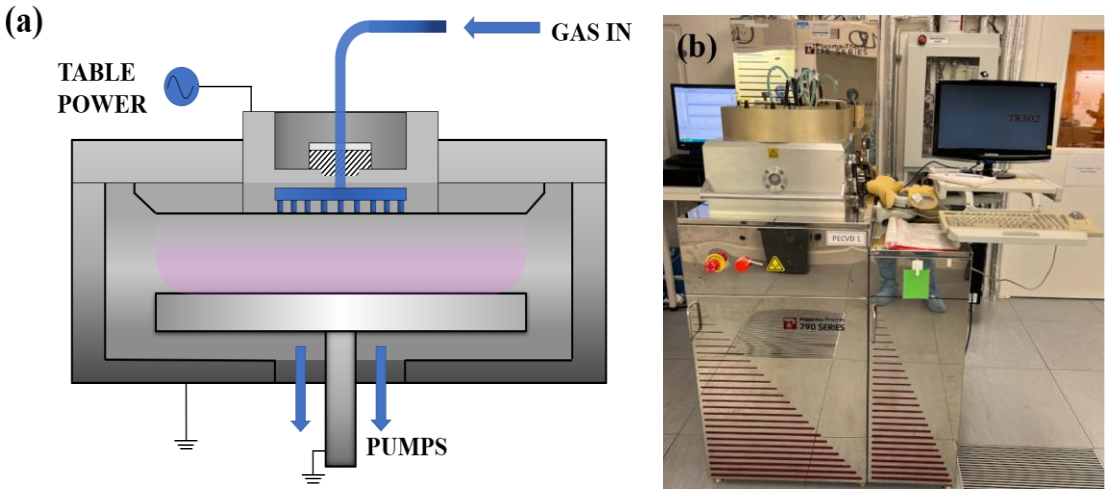

Figure 3.4: (a) schematic illustration of PECVD, and (b) the Plasma-Therm 790 PECVD system.

Our PECVD is Plasma-Therm 790 PECVD system (**Figure 3.4(b)**) which is employed to deposit the SiO_2 films on the sample. During the deposition process, the sample stage is heated up to 300℃ while the sidewall is 60℃. SiH_4, NH_3 and N_2 are the reactant gases and inject into the chamber with the flow rates of 160sccm, 900sccm and 240sccm respectively. Meanwhile, the pressure of the chamber is set as 900 mTorr and RF power is 25W. Under this condition, the deposition rate of SiO_2 is 40nm/min approximately. In this work, the thickness of the SiO_2 layer is required about 500nm for top surface protection.

3.3.2 Rapid Thermal Annealing (RTA)

The rapid thermal process is a semiconductor manufacturing process involving heating the sample to affect its electrical properties. The samples can be heated to a unique temperature that can activate dopants, change the film-to-film interface or drive dopants from one film into another. In this work, a Jipelec rapid thermal annealing system is used for Hall measurement Ohmic-contact fabrication. Halogen lamps are used to heat the sample to a high temperature and the heating process is monitored by a pyrometer and a thermocouple. The indium contact annealing for Hall measurement is under N2 ambient for the whole process. The temperature of the sample started at 200℃ and

increased to 420℃ in 30s. Then, the sample keeps at 420℃ for 30s. Once the annealing is completed, the sample will be cooled by nitrogen at a high flow rate. **Figure 3.5** is the RTA system used in this work.

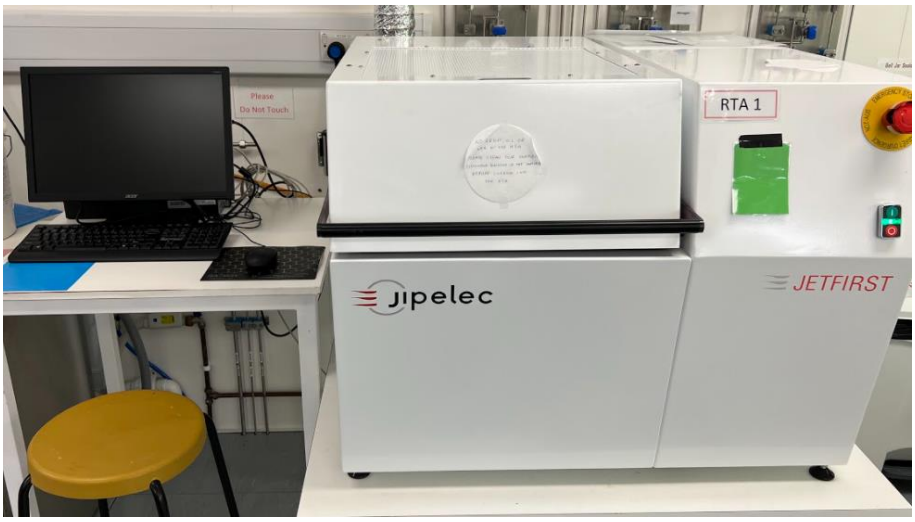

Figure 3.5: The Jipelec rapid thermal annealing system.

3.4 Photolithography

Photolithography is one of the typical techniques in semiconductor device fabrication. It transfers a pre-designed pattern from the photomask to the photosensitive medium on the sample surface by short-wavelength light (UV). This process must be carried out in a yellow room to filter the short-wavelength light and prevent the photoresist from reacting early. Photolithography can be divided into three main steps: photoresist coating, UV exposure and development.

3.4.1 Photoresist coating

The photoresist is a kind of light-sensitive material. It is mainly used in photolithography and photoengraving, which is a vital material in the modern electronics industry. **Figure 3.6** is the flow chart of photolithography. After the surface cleaning procedure, the sample is placed on a hot plate to evaporate the residual water. Then, spin a layer of photoresist evenly. It is necessary to apply a soft bake process after spin. This step helps evaporate the organic solvent in the photoresist and dry the

photoresist layer for the following exposure. Then, a patterned mask will be applied to the sample surface to block UV light and expose unmasked areas to UV light for UV exposure. The sample will leave a corresponding pattern after passing through the development step. There are two kinds of photoresists: positive photoresists and negative photoresists. The area of the positive photoresist (SPR350, BPRS200 and SPR220) exposed to UV light will be photolyzed, leaving a layer on where the mask is placed after development. A negative photoresist (SU-8) is the opposite. The photosensitive material polymerizes under UV light and the developer dissolves only the unexposed areas.

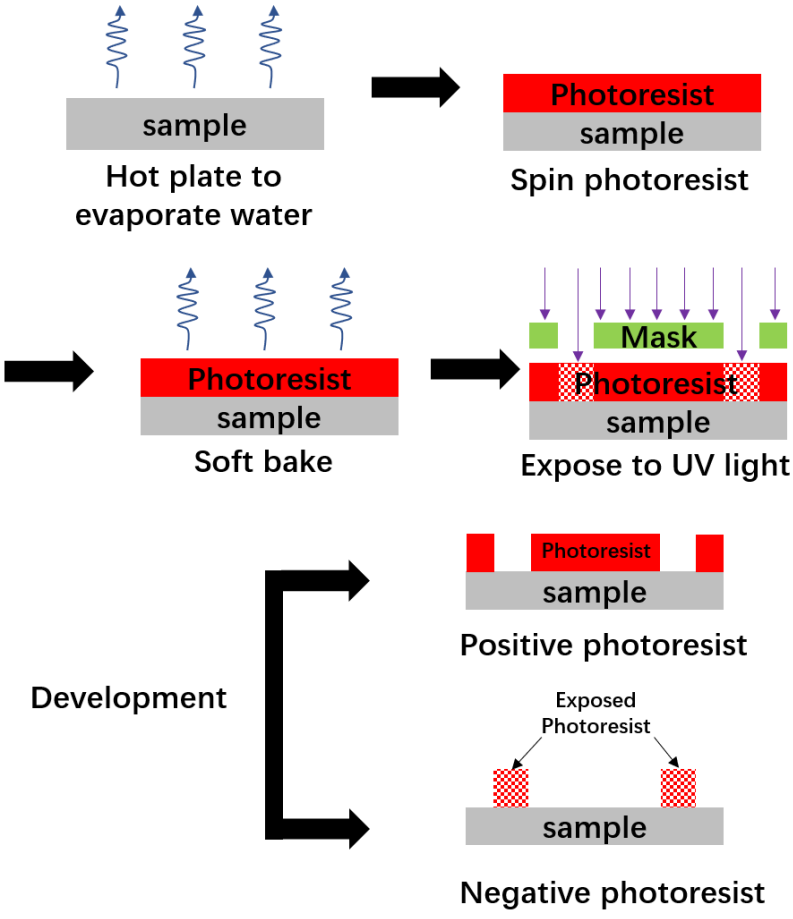

Figure 3.6: Photolithography flow chart.

In this work, a 500nm SiO_2 layer is deposited on the top of the DBR sample by PECVD. Then the sample is cleaned and baked with the steps stated in the sample clean section. Due to the reason that SiO_2 is naturally hydrophilic and absorbs water from ambient

humidity, there will be a water layer between the interface of the photoresist and SiO_2 when applying the photoresist directly. Such a water layer leads to undercutting or completely delamination of the photoresist pattern. **Figure 3.7** shows Hexamethyldisilazane (HMDS) which is introduced as an adhesion promoter. It will convert the hydrophilic state of SiO_2 to a hydrophobic surface and increase the adhesion during develop [6]. SPR-220 is the main photoresist in this work. By applying 4000 RPM for 30s with the Electronic Micro System Spin Coater Model 4000, it will form a 3.5μm uniform coating layer on the sample. Then, the coated sample needs to be soft baked with 100℃ to get solidified photoresist on the wafer surface.

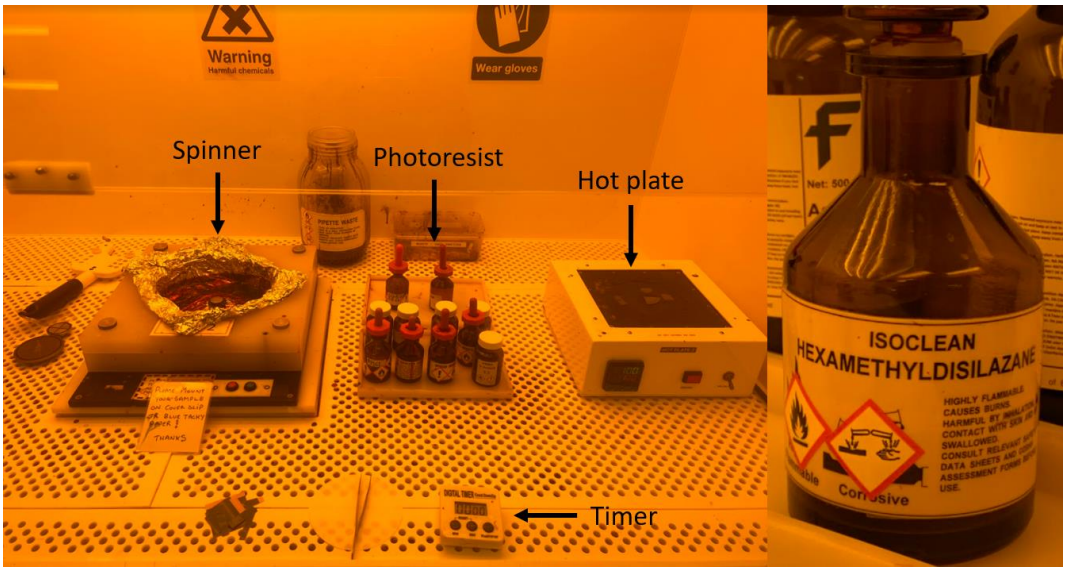

Figure 3.7: Electronic Micro Systems Spin Coater Model-4000 and inserted image is Hexamethyldisilazane (HMDS).

3.4.2 Wafer bonding with SU-8.

Su-8 is an epoxy-based negative photoresist whose name comes from the presence of eight epoxy groups. It can be made as a viscous polymer and the spin thickness ranges from below 1μm to above 300μm. Su-8 absorbs the light in the UV region, especially for i-line (365nm). It will polymerize at about 100℃ and be stable at up to 150℃. This kind of polymer has a high cross-linking density and high stability. Considering the

various advantages of SU-8, there have been many reports using this material as a wafer bonding material [7-10].

NANO^{TM} SU-8 2010 which is used in this work. It is the second generation of this series of products. The film thickness is in range of 10-20μm (depending on spin speed). For a typical SU-8 bonding procedure, it includes the following steps:

- Sample cleaning.
- Dehydration.
- Spin coating the SU-8 with 4000rpm for 30s.
- Soft bake: low temperature for 3min (65℃) and high temperature (95℃) for 5min. to evaporate solvent and densify the film.
- Exposure with UV light. Curing the SU-8.
- Post exposure bake to selectively cross-link the exposure portion.
- Hard bake 150℃ for 30min for further cross link the material.

3.4.3 Exposure

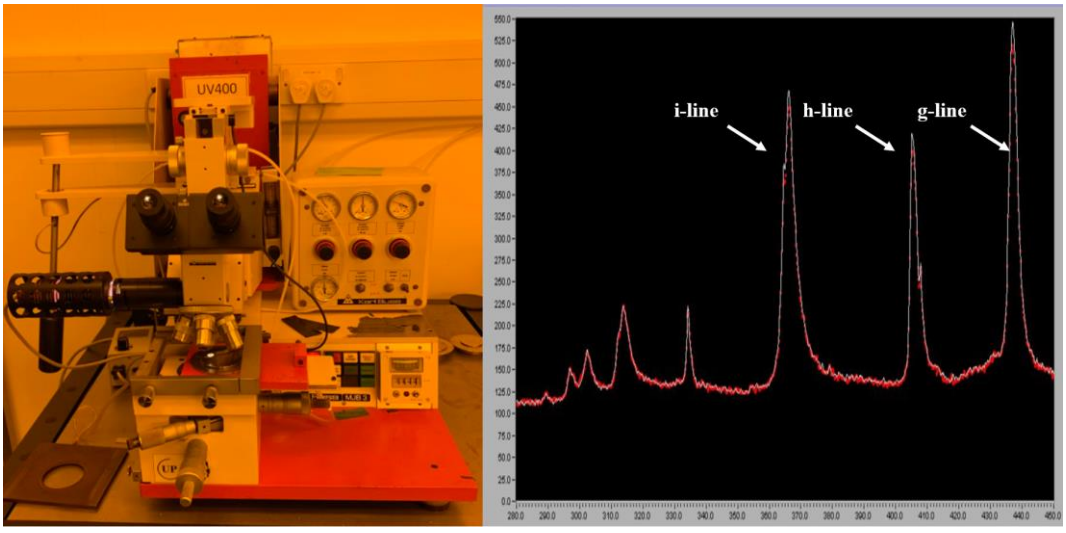

Figure 3.8: The Karl Suss MJB3 UV400 Mask Aligner in a yellow room and the UV lamp wavelength

Figure 3.8 is the Karl Suss MJB3 UV400 Mask Aligner which is employed to prime the patterned structure resist film. This aligner uses a UV lamp with 365nm, 405nm and

440nm wavelength light to illuminate the photomask with a resolution of 0.8μm under optimum conditions. The photomask is made of a quartz plate and coated with patterned chrome. The UV light from the mask aligner will be blocked with the pattern opaque region then the un-blocked light will change the properties of the photoresist. So, the pattern structure on the photomask is transferred to the photoresist film with a 1:1 ratio. The whole photolithography process is undertaken in a yellow room to filter the unwanted UV light which can make the photoresist pre-reaction.

3.4.4 Development

After exposure, the sample is developed in the develop solution to either remove the exposed or unexposed area which depends on the type of photoresist. MF-26A is the developer that applies to the SPR220 in this work. It is an aqueous solution of the metal ion free organic TetraMethyl Ammoniumhydroxide (THAH). The developer is diluted in DI water with a ratio of 2:1 to control the development rate and the developing time is 60s.

3.5 Etching

3.5.1 Dry etching: Inductively Coupled Plasma etching

Inductively Coupled Plasma Reactive-ion etching (ICP-RIE) is shown in **Figure 3.9,** which is a dry etching technique based on the use of an inductively coupled plasma source. An independent RF coil inside the system is applied to generate a time-varying electromagnetic field and the reactance gases are ionized by inductive coupling. Meanwhile, an additional RF power on the cathode can generate DC bias to attract and accelerate reactive ions to the wafer. Therefore, the plasma densities are very high with ICP-RIE and easier to control the etching condition with vertical ion bombardment. Another major advantage of ICP-RIE is the etch chamber separated with RF generated and has better selectivity.

Oxford Instruments Plasmalab System 100 is employed for GaN etching in this work. The frequency for RIE and ICP RF generators are all set as 13.56MHz. For typical GaN etching, the ICP power is 450W and RIE RF power is 80W. In addition, Cl_2/Ar gas mixture is the etchant gas [11]. An interferometry endpoint system is inside the ICP to monitor the etch depth and rate. It consists of a laser sensor to spot the sample surface and measure the intensity of the reflected laser. Due to the changing of the interference cycle, the periodic oscillation will change with the etching taking place. The typical etch rate of GaN is 120nm/min.

Figure 3.9. Image of an ICP system.

3.5.2 Electrochemical etching

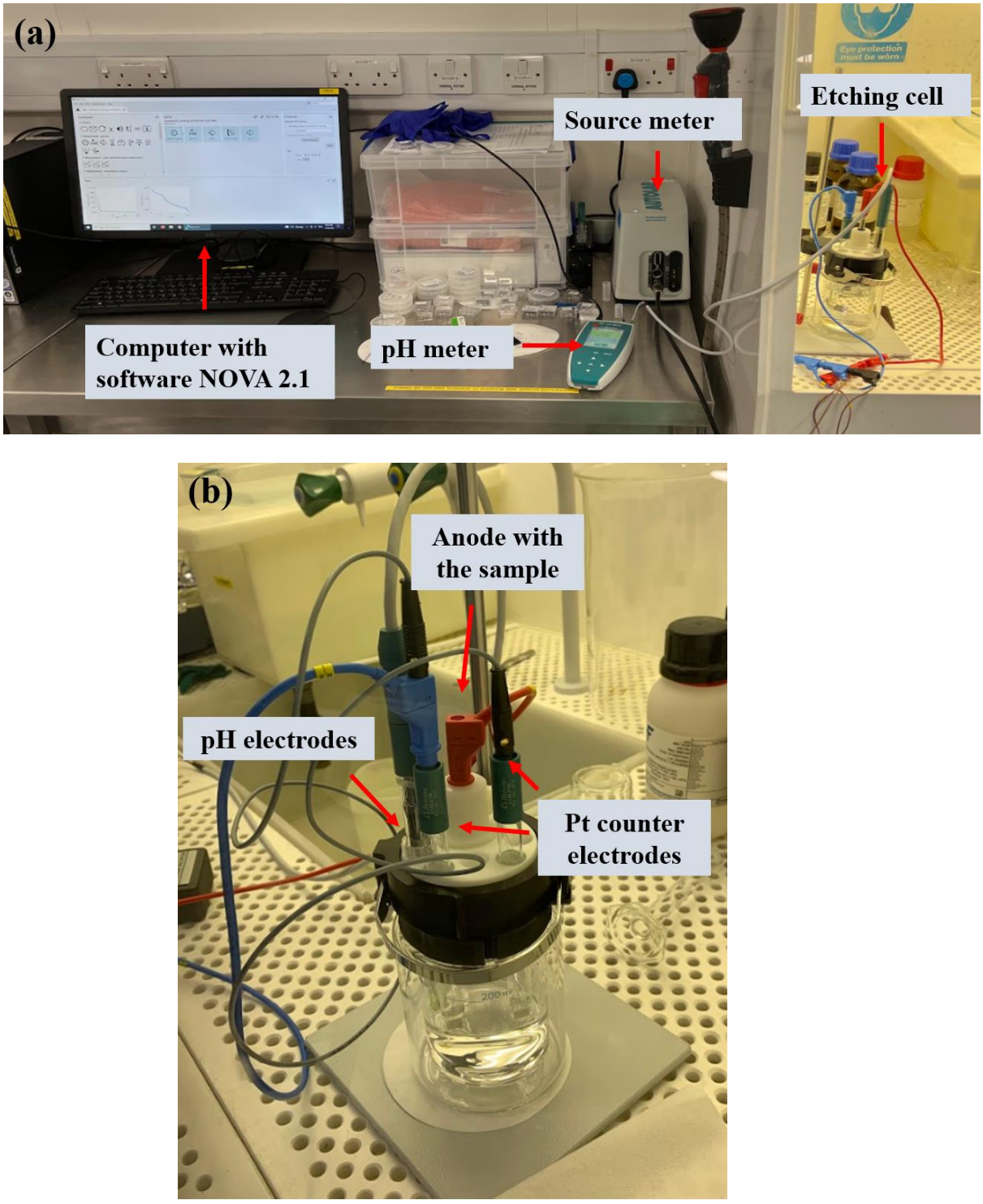

Figure 3.10: (a) Metrohm electrochemical etching system and (b) the etching cell with electrodes.

As described in chapter 2, a standard electrochemical etching system consists of electrodes, a counter electrode, a source meter, and an electrolyte. When they are all immersed in the electrolyte, electrical and chemical reactions will occur with a proper bias voltage. **Figure 3.10** shows the Metrohm electrochemical etching system in this work. This system consists of a metal electrode, a Pt counter electrode, an open beaker, a top safety case with a seal O-ring, a pH meter with a pH electrode, and a source meter controlled by computer software Nova 2.1. Firstly, the sample is scratched at the edge and makes an indium contact. Then, connect the indium with the metal electrode. As shown in **Figure 3.10(b),** the anode with the sample is connected through the large hole on the top case and controls the height with a small O-ring. Next, the Pt counter electrodes and pH electrode are put at the small holes and face. They are required to face the sample. Then, the sample electrode and Pt counter electrode are connected to the source meter which is used to control the bias and etching time. The pH meter connects with the pH electrode and monitors the pH value and the temperature. The electrolyte used in this work is nitric acid. The etching condition will be discussed in detail in Chapter 4.

The electrolyte used in EC etching is made of nitric acid with 70% weight percentage. For the concentration of the HNO_3 electrolyte used in EC etching, it is calculated with the following equation:

$$C_D \times V_D = C_{Acid} \times V_R \tag{3.1}$$

Where C_d is desired concentration, V_D is desired final volume, C_{Acid} is the concentration of HNO_3 (15.698M) and V_R is the volume required acid in this work.

3.5.3 HF treatment

Hydrofluoric (HF) acid is an aqueous solution of hydrogen fluoride. HF acid is a colourless and highly corrosive acid that can strongly corrode metals, glass and silicon-containing objects. Therefore, it is generally used for etching glass and silicon wafers.

However, HF is extremely toxic. The fluoride ions can enter the blood, tissue or even bone and combine with calcium and magnesium ions to cause permanent damage. Therefore, the use of HF acid requires special personal protective equipment (PPE). Once contact with skin, usually rinse with Hexafluorine and seek medical attention promptly.

In this work, 40% Buffered oxide etch (BOE) is employed to etch the SiO_2 layer or remove the oxide layer on the surface of the silicon substrate. BOE is a mixture of a buffering agent that consists of ammonium fluoride (NH_4F) and hydrofluoric acid (HF). BOE is easier to control the etching due to its low etching rate than concentrated HF. All samples were put into the 40% BOE for 5mins to remove the SiO_2 completely.

3.6 Characterization technique

3.6.1 Nomarski Microscopy

The Nomarski microscopy, also known as differential interference contrast (DIC) microscopy can enhance the contrast of unstained, transparent samples and magnify the image of a testing object. Nomarski microscopy uses the difference between two coherent lights to improve the contrast of the image and get invisible information. This system is easy to observe the difference in thickness or refractive index. Due to the III-nitrides and sapphire substrate being all transparent, Nomarski microscopy is especially suitable for the characterization of the GaN-based sample.

The basic structure and image of Nomarski Microscopy in our group are shown in **Figure 3.11**. An input unpolarized light is first polarized at 45° by a polarizer. Then, it is reflected by a semi-transparent mirror into a birefringent Wollaston prism and separated into two orthogonally polarized beams. These beams are with respect to each other and focused by a condenser to object onto a sample surface. Due to the two light beams being different in polarization, it is sensitive to the varied thickness or reflective index where the light path through different optical path lengths. The reflected lights

with different phases are back to Wollaston Prism and recombined together with a 135° polarizer. The interfering of these two coherent beams will form a different brightness during recombination and shows the detail of the sample (thickness or refractive index) [12].

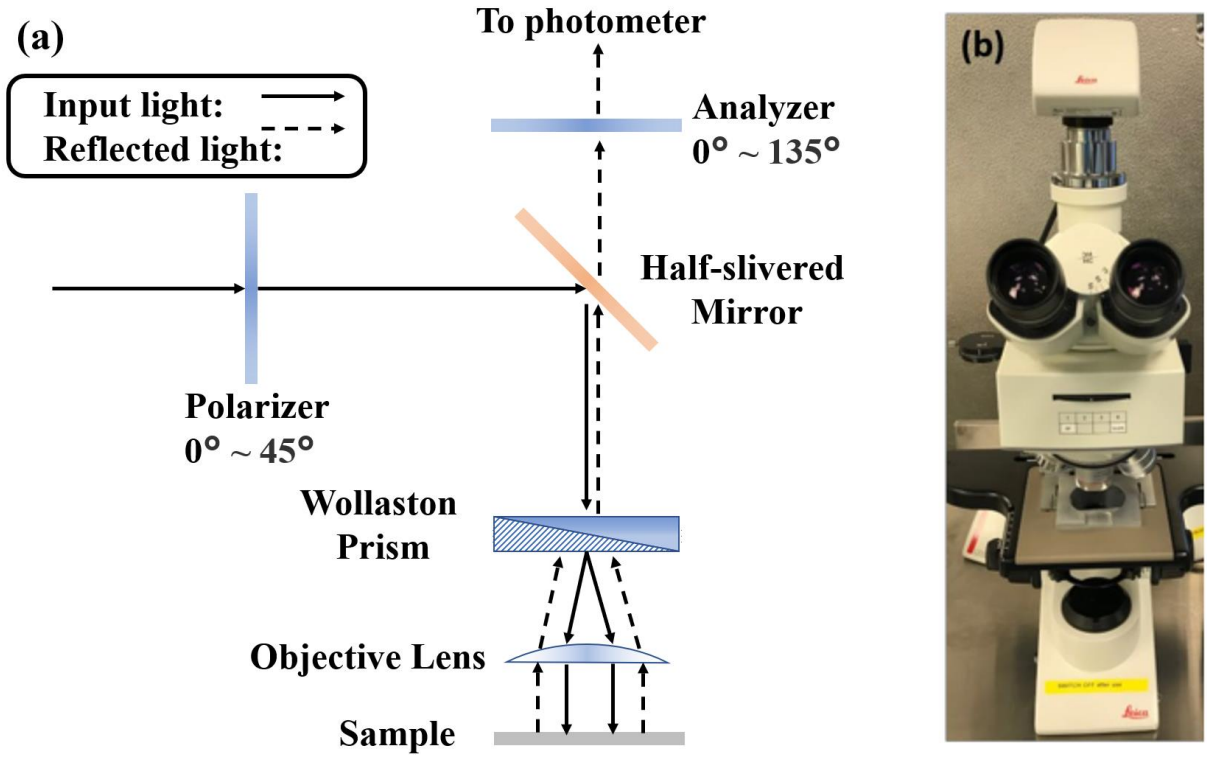

Figure 3.11: The (a): schematics of light route, (b): image of Leica DMC4500 microscope.

3.6.2 SEM

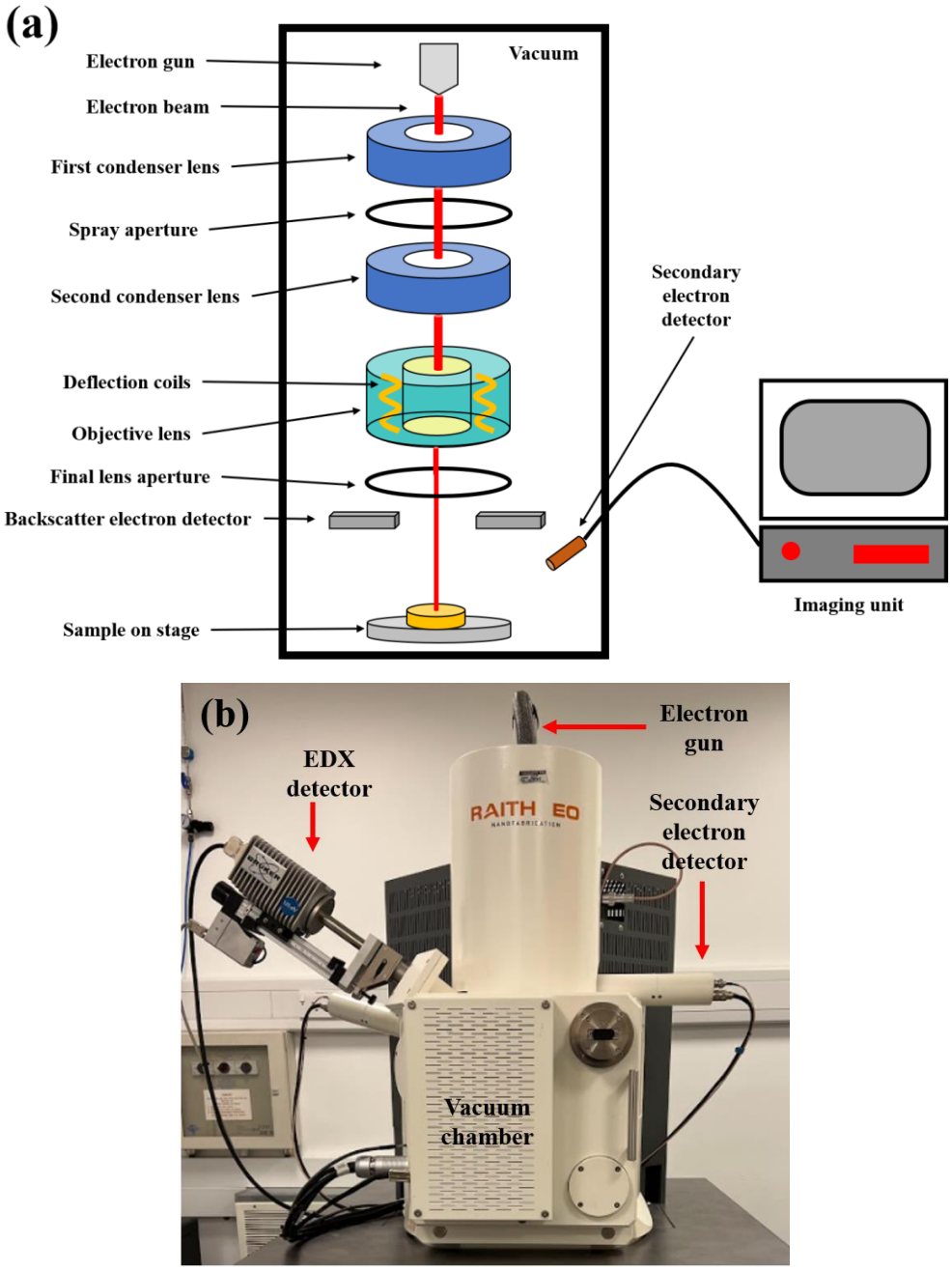

Figure 3.12: (a) Schematic diagram of a typical SEM and (b) Raith 150 EBL based SEM system.

Scanning electron microscopy (SEM) is an important tool to investigate the nanoscale structure in this work. Unlike the conventional optical microscope that uses a visible light source, SEM employs the electron beam as the illumination source. The much

shorter wavelengths of electrons can produce images with higher resolution. **Figure 3.12(a)** shows the schematic configuration of the SEM system. The whole system is operated under a high vacuum environment (typically under $5*10^{-5}$mbar) to avoid the oxidation of the beam system and also increase the mean free path of the electrons. A field emission gun (FEG) generates electrons with a high voltage of 30kV to accelerate the beam. The generated electron beam will then be collimated and focused on the surface of the sample after passing through a series of magnetic lenses. Meanwhile, there is a set of deflection coils in the system to control the beam position. The secondary electrons are collected by an appropriate detector and converted into electrical signals. **Figure 3.12(b)** is the Raith 150 electron-beam lithography (EBL) with reconfiguration employed as the SEM system in this work.

The electrons generated by the FEG are in terms of primary electrons. These electrons will lose energy when penetrating the surface of a sample and interact with the sample [13]. Then, the lost energy is converted into other forms of signals. There are four types of signals used in SEM to characterise the sample: backscattered electrons, secondary electrons, X-ray emission and light emission.

- Backscattered electrons (BSE) work like an asteroid that circles the earth and drifts back into space without hitting the earth. The negatively charged electrons won't be captured by the positive nucleus and reflected or "backscattered" out of the sample. These electrons have high energy and move fast in a straight line. Therefore, the detector is placed directly above the sample. Since the scattering of BSE is strongly determined by the size of the nucleus, the BSE is used to obtain high-resolution images of the different elements in a sample [14].
- Secondary electrons (SE) are generated as ionisation products from a sample surface. Since the energy of SE is very low (<50eV) and the electrons are highly localized impact, the SE can be used to realize a high-resolution scan. They are captured by a positively charged SE detector and used to characterise surface morphology and the topography of a sample.

- X-rays are generated by the interaction of incident electrons and the excited electrons of the outer shell. A unique signature emission spectrum of material is generated when the excited electrons return to the low energy state. So, the X-rays can be used to identify the elemental composition in the sample through energy-dispersive X-ray analysis.
- Light emission is also known as cathodoluminescence. It is caused by the excitation of atoms. It is used similar to photoluminescence but uses a high energy electron beam as the excitation source which has a high spatial resolution on a nanometre scale.

3.6.3 EDX measurement

Energy-dispersive X-ray spectroscopy (EDX, EDS, EDXS or XEDS), is used for the elemental analysis or chemical characterization of a sample. As a part of the SEM system (shown in **Figure 3.12b)**, it relies on the interaction of the sample and electrons. Once the electrons are focused on the sample surface, an inner shell electron may be excited and release the energy in the form of an X-ray. It will show a unique peak of the electromagnetic emission spectrum due to each element having a unique atomic structure [15]. The EDX measurement in this work is employed to further detect the chemical composition of the lift-off membrane.

3.6.4 Reflect system

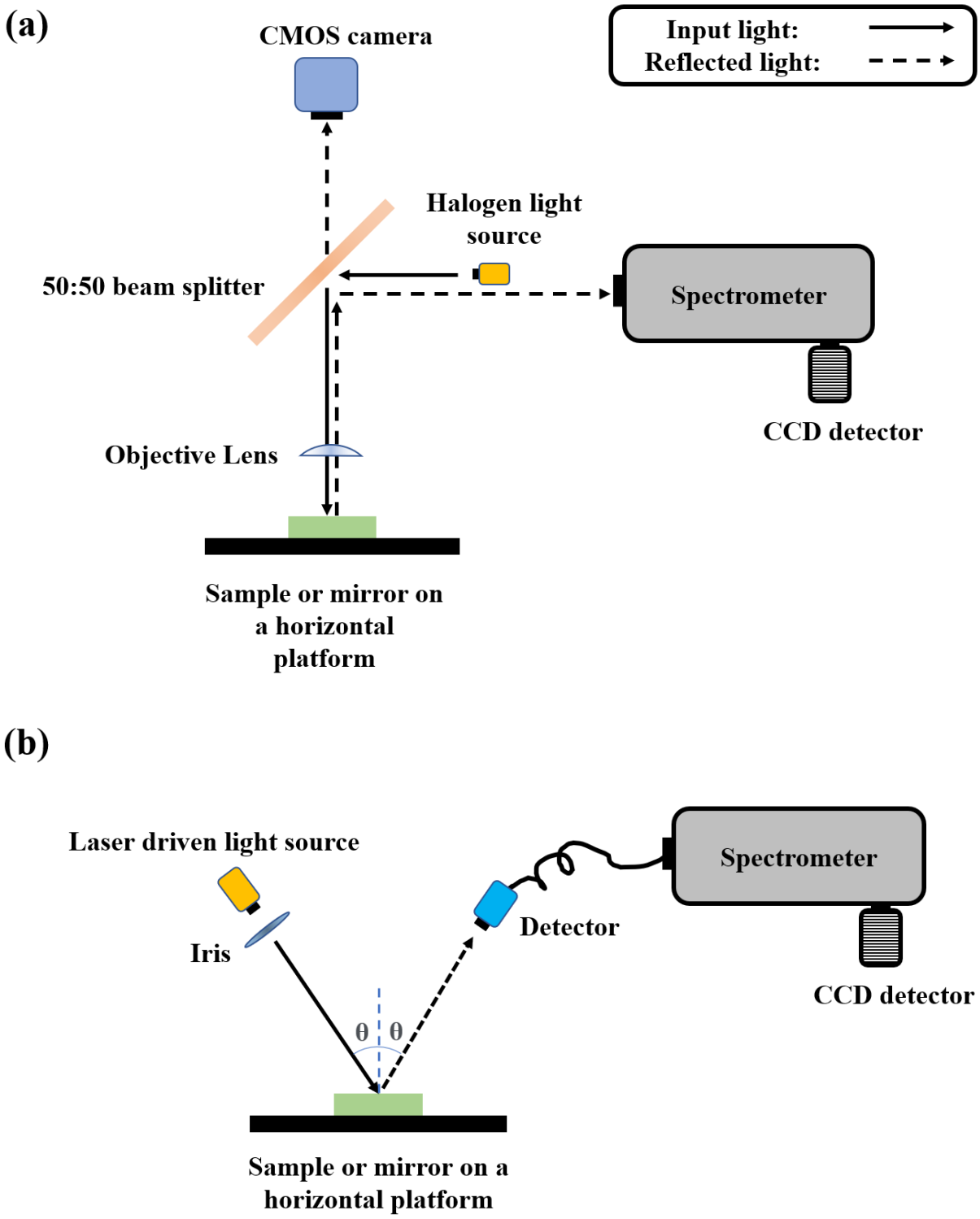

Figure 3.13: schematic image of (a) Direct reflectance measurement system (b) Angle dependent reflectance measurement system.

As mentioned earlier, reflectance is an important property of DBR devices. The ratio of the reflected wave to the incident wave power is the reflectance. There are two different types of reflectance measurement systems in this work: The direct Reflectance Measurement System and Angle Dependent Reflectance Measurement System. The Direct Reflectance Measurement System is shown in **Figure 3.13(a)**. A standard halogen lamp is employed as a light source, covering a wide range from ultraviolet to far-infrared (390nm-900nm). The light will irradiate on a commercially calibrated specular reflectance standard directly. This standard is provided by the STAN-SHH high reflectance mirror which has 85%-98% in the 250nm-2500nm range. The objective lens collects the reflected light and introduces it into a 50:50 beam splitter. 50% of light is used for the CMOS camera to identify the sample positions. The remaining half was collected by a shamrock 500i Czerny-turner spectrometer through a light collimator and finally detected by an air-cooled charge-coupled device (CCD). The Angle Dependent Reflectance Measurement System in this work is shown in **Figure 3.13(b).** Unlike the Direct Reflectance Measurement System, a laser light source and a monochromator are respectively fixed on two computer-controlled arms. This light source can provide a light beam in the wavelength range from 250nm to 2500nm. The light is then adjusted to a 1mm spot by the iris, irradiated on the mirror, and then collected by the spectrometer. Ultimately, like the Direct Reflectance Measurement System, an air-cooled charge-coupled device (CCD) detects reflected light. A spirit level calibrates the sample platforms of both systems. The reflectivity of the sample is measured with the function:

$$R = \frac{I_{sample}}{I_{mirror} \times R_{mirror}} \tag{3.2}$$

Where R is the reflectance of sample, I_{sample} and I_{mirror} is the detected intensity of sample or mirror at exact wavelength. R_{mirror} is the exact reflectance of mirror at a different wavelength.

3.6.5 AFM

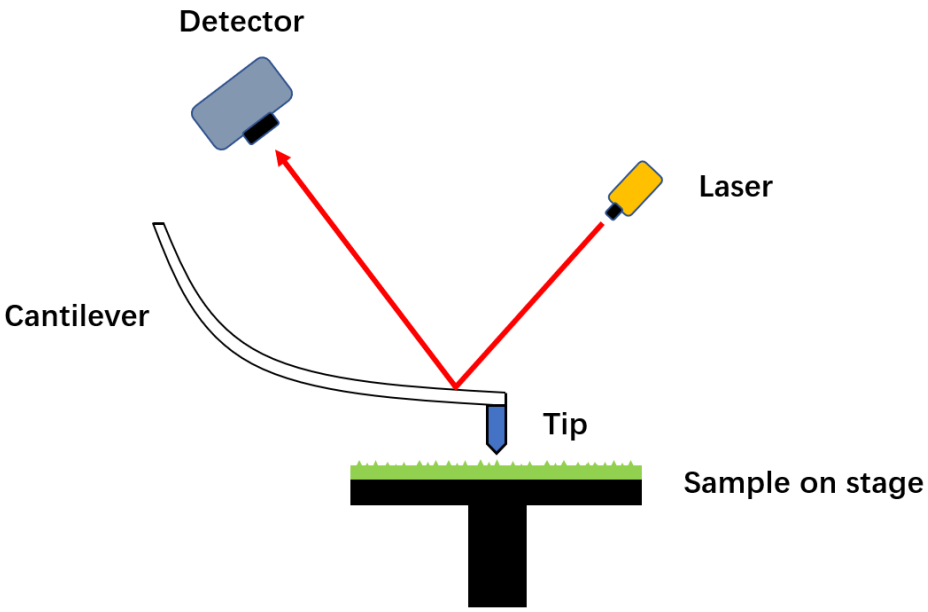

Figure 3.14: Schematic diagram of AFM.

Atomic force microscopy (AFM) is a kind of scanning probe microscopy with very high resolution. Unlike the two-dimensional images provided by SEM, AFM is able to do 3D surface scanning. **Figure 3.14** is a schematic diagram of an AFM. A minute tip is immobilized on a cantilever. The cantilever is extremely sensitive to forces and the tip is usually made of silicon. Since GaN is a very hard material and can damage the tip during scanning, a SiN coating is implemented for protection. When the tip scans the sample surface, the interaction between the sample and tip will deform the cantilever. A laser shines on the back of the cantilever and the detector detects the reflected laser spot to obtain the topography information of the sample surface. There are two detection modes: contact mode and tapping mode. The tip in contact mode is "dragged" on the sample surface and measured the surface directly. Tap mode can non-destructively assess the sample surface with more precision. The tip is periodically and briefly contacts the sample surface to reduce the lateral forces. By recording the phase of the cantilever's oscillation with respect to the driving signal, the tapping mode can provide information of surface roughness and average height.

3.6.6 Hall measurement

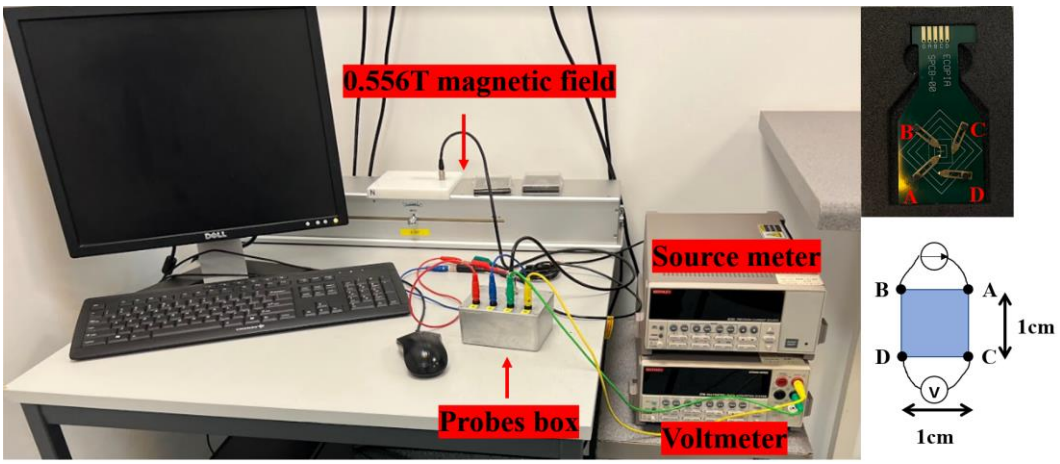

Figure 3.15: Hall measurement system. The top insert picture is the probe stage, and the bottom schematic is the resistance measurements from Van der Pauw connections between I_{AB} and V_{DC}.

The carrier concentration, resistivity and the electron mobility of the GaN-based sample were determined by using the Van der Pauw technique. It is also called Hall measurement which is shown in **Figure 3.15**. All samples were diced into squares with a side length of 1cm in order to follow a four-point probe symmetry. For DBR samples, a dry-etch process is required to remove the top un-doped GaN layer and fully expose the heavily silicon doped n-GaN. The sample surface was cleaned via a cleaning process to minimise any electrical resistance. An indium contact was applied on the edge of each corner. Then the samples were applied an RTA process to form an ohmic contact [16].

The test sample is placed onto a probe stage and four corners were connected to probes with labelled A, B, C and D. Two Keithley source meters are used as voltmeter and current source in this measurement. Then, sequentially measure the voltage in different directions at the same current and the data are simulated by LabVIEW. The Hall measurement is typically carried on with 0.1mA under room temperature (300K) where the magnetic field is 0.556T. Since the doping level of un-doped GaN is far less than

heavily n-doped GaN, the layer thickness of the DBR sample measurement only takes into account the total thickness of n-GaN.

Resistance Measurement Data (Zero Magnetic Field)

Vertical:							
I(AB)	*V(DC):*	17.610	mV	*R(AB,DC):*	1.761	W	
I(BA)	*V(CD):*	17.608	mV	*R(BA,CD):*	1.761	W	
I(CD)	*V(BA):*	17.604	mV	*R(CD,BA):*	1.760	W	*R (vertical):*
I(DC)	*V(AB):*	17.605	mV	*R(DC,AB):*	1.761	W	1.761 W
Horizontal:							
I(AD)	*V(BC):*	25.520	mV	*R(AD,BC):*	2.552	W	
I(DA)	*V(CB):*	25.520	mV	*R(DA,CB):*	2.552	W	
I(CB)	*V(DA):*	25.519	mV	*R(CB,DA):*	2.552	W	*R (horizontal):*
I(BC)	*V(AD):*	25.519	mV	*R(BC,AD):*	2.552	W	2.552 W

Table 3.1: An example of resistance measurement data with zero magnetic field.

A total of eight resistance measurements including vertical and horizontal directions are shown in **Table 3.1**. **Table 3.2** shows the different connections of Hall measurements under the influence of a magnetic field. In order to maintain accuracy, the samples were multi-measured with different areas of the wafer.

The data were then simulated via LabVIEW and output in **table 3.3**.

Hall Voltage Measurment Data

		Negative Field (S→N):		*Positive Field (N→S):*		*Difference (N→S) - (S→N)*	
I(AC)	*V(DB):*	-7.221	mV	-8.601	mV	-1.380	mV
I(CA)	*V(BD):*	-7.222	mV	-8.600	mV	-1.378	mV
I(BD)	*V(AC):*	8.611	mV	7.232	mV	-1.379	mV
I(DB)	*V(CA):*	8.603	mV	7.225	mV	-1.378	mV

Table 3.2: An example of Hall Voltage measurement.

Output Parameters		
Sheet Resistance:	9.658	W
Resistivity:	9.562E-04	W.cm
Conductivity:	1045.853	(W.cm)-1
Hall Voltage:	-0.689	mV
Sheet Density:	5.035E+15	cm-2
Bulk Density:	5.085E+19	cm-3
Hall Coefficient:	-1.227E-01	cm3C-1
Mobility:	128.377	cm2V-1s-1

Table 3.3: The output parameter of Hall measurement.

3.6.7 FDTD simulation

In this experiment, the sample was first designed by the Lumerical FDTD software, the finite-difference time-domain (FDTD) algorithm [17]. Since the Maxwell equations were proposed in 1873, they have been widely used to deepen understanding of electromagnetic phenomena. In 1966, K. S. Yee first introduced the numerical time-domain method to describe Maxwell's equations in his paper [18]. That makes the discretization of Maxwell's equations in the time and space dimensions can be solved by the FDTD. With the rapid development of computer processing power and algorithm optimization, the FDTD method has become one of the most accurate and efficient numerical simulation techniques for electromagnetic problems. This method can calculate the electromagnetic interactions accurately. Thus, it is commonly used to simulate propagation, reflection, scattering, diffraction and many other electromagnetic phenomena. Currently, there are more than ten kinds of different software for FDTD simulation. This software allows engineers to design arbitrary model geometries with no restriction on the material properties [19]. The simulation in this work was used to design the DBR structure as well as etching result analyses. The refractive index of GaN is 2.45 [20] and the effective refractive index is from the software analysis of the cross-sectional SEM images. The electric field in simulation is set as a plane wave source with an emission wavelength in the range of 400nm to 700nm which is placed

right above the DBR structure. The running time for the simulation is 1000fs and each wavelength has minimum of 22 mesh points. All structure is surrounded by perfectly matched layers (PML) boundary conditions.

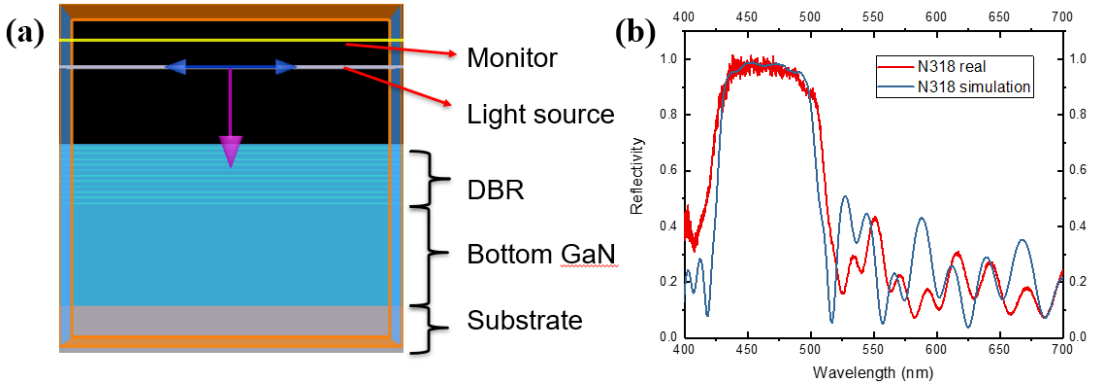

Figure 3.16: (a) Modelling of DBR structure by FDTD simulation. (b) Comparison of real measurement and simulation of example sample.

Figure 3.16a is the modelling of the DBR structure by FDTD simulation. In this model system, a whole DBR structure with a GaN buffer layer and substrate was placed at the bottom. The thickness of each layer is determined by the SEM measurement result. The refractive index of the sapphire substrate was set as 1.76 (Al_2O_3), and the GaN layers were set as 2.44 for 500nm. The etched porous GaN layer has a refractive index which depends on the porosity. Above the DBR, a planner light source is set to irradiate parallel light to the DBR surface directly, and the reflected light can be detected by the monitor behand the light. Meanwhile, the boundaries were set as perfectly matched layer (PML) boundaries. After the FDTD simulation, the simulation results are compared with the real measurements as **Figure 3.16b** shows. It is used to evaluate the etching as well as the adjustment of the subsequent growth conditions.

3.6.8 Accuracy and Error

In order to maintain the accuracy of the experiment equipment and the consistency of the measurement, a series of procedures were included to minimize the error of data.

The non-variable conditions of all experiments were kept the same. In MOCVD growth, the in-situ laser monitoring system can monitor and control the thickness of each layer. The thickness will be used as a benchmark for the subsequent SEM measurements. Since the possible system error in the SEM system, the thickness difference between SEM results and laser measurement results should be within a defined tolerance level (+-5nm). The software Image J was applied in the measurement of porous size in the SEM results. Consistency checks were carried out by the average value of different layers to ensure that all results were universal.

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Chapter 4: Fabrication and characterization of lattice matched DBRs

Chapter 4 presents a detailed study of the electrochemical (EC) etching mechanism on nanoporous (NP) GaN-based DBR fabrication. The first section will be focused on the conditions of EC etching of DBR. Three n-GaN/GaN DBR samples with different doping concentrations were grown by MOCVD and went through standard EC etching. By analyzing the etching under different applied bias voltages, it is proved that both the voltage of EC etching and the conductivity of the sample play crucial roles in the EC etching of GaN-based NP DBR devices. The sample etched with a low voltage exhibits a smooth surface but a low refractive index ratio between the n-GaN layer and GaN layer in each period which is not beneficial for high-performance DBR devices fabrication. On the other hand, a high applied bias can effectively increase the porosity of the n-GaN layer and get a large refractive index ratio. However, the overall DBR structure will be fragile with cracks, or the heavily n-doped GaN even be polished. A processing phase diagram of the EC etching is presented to summarize the etching results. The best conditions for DBR fabrication are used for the following experiments. In the second section, a lateral etching method is designed to enhance the DBR performance, which employs SiO_2 and photoresist as a protection layer. Therefore, the EC etching can only start in the dry-etched trenches and the etching direction is confined within each n-GaN layer. As a result, the porosity after etching is highly uniform. Compared with the normal etching method, the reflectance of DBRs after lateral etching is increased from 97.3% to 98.5% and the stopband width is increased from 104 nm to 144 nm. In addition, the mechanism of these two EC etching methods are also discussed.

4.1 Introduction

As a direct bandgap semiconductor material, gallium nitride (GaN) and its alloys are widely used in electronic and optoelectronics. Since the first commercial nitride light-emitting diodes (LEDs) were developed in the mid-1990s [1], the usage of this material has already been expanded to optoelectronic devices. Such as single-photon sources [2-4], laser diodes (LD) [5-8], vertical cavity surface emitting lasers (VCSEL) [9-13], solar cells [14-16], integrated photonic circuits [17-19], etc. Changing the composition ratio of different group III metals (In, Ga, Al) to form binary compounds with nitrogen can achieve a material system with band gaps spanning the entire visible spectrum. Distributed Bragg Reflectors (DBRs) are a kind of reflector that consists of multiple pairs of alternating layers with different refractive indexes. It is an important component of semiconductor photonic devices such as VCSELs and resonator cavity light-emitting diodes (RCLEDs). High-quality GaN-based DBRs are designed to improve light extraction efficiency in optoelectrical devices [20-22]. The typical III-nitride-based DBRs such as AlGaN/GaN DBR structures [23], AlN/GaN DBR structures [24], and AlInN/GaN DBR structures [21] are introduced as bottom DBRs for VCSEL fabrication which can be formed during the epitaxial growth. However, the difference in refractive index between alternating layers of the materials is usually small, which requires a lot of pairs to achieve high reflectivity. For example, $Al_{0.83}In_{0.17}N$/GaN DBR requires more than 40 pairs to achieve peak reflectivity higher than 99% [25]. On the other hand, applying EC etching on a highly n-doped layer to form a porous structure can easily obtain a large refractive index difference in the periodic layers. The NP DBR structures have a higher reflectivity and a wider reflective wavelength. Therefore, applying the NP DBR structure can further enhance the performance of optoelectronic devices.

Typically, nanoporous material is a porous structure with a 1-100 nanometers aperture. Compared with bulk semiconductor materials, porous semiconductors have received

extensive attention in the past decade due to their unique optical and physical properties. Tunable hole structures have been successfully fabricated on Si [26], GaAs [27-29], GaP [30] and InP [31, 32]. The research is mainly focused on changing the emission properties of porous semiconductors by controlling the pore size. For GaN, porous structures have great potential in water splitting [33], high-quality epitaxial structure re-growth [34] and membrane lift-off [35, 36]. However, GaN is extremely chemically inert and is fairly stable in standard wet etching. Meanwhile, dry etching methods can only be applied for the top-down etching, limiting the applications for creating new nanostructures. The success of electrochemical etching in preparing porous silicon has brought new ideas for the fabrication of porous GaN devices. In this method, heavily doped GaN is immersed in an acidic electrolyte and etched with a positive anodic bias. By controlling parameters during the etching process, the porosity of the porous structure can be changed to meet different requirements. The application of the NP DBR structure to optoelectronic devices has been reported massively. However, there are relatively few studies about improving the performance of DBRs. Meanwhile, the mechanism of EC etching in the DBR formation is rarely discussed. Moreover, current reports just simply use the EC etching on bulk n-GaN to fabricate NP GaN DBR. However, the effect of the undoped layer during the EC etching is still not well understood.

This chapter will demonstrate an n-GaN/GaN multilayer structure which went through the EC etching to be transformed into a nanoporous GaN/GaN DBR structure. Firstly, three DBR structures were grown with different n-GaN doping levels and were separately EC-etched with different bias voltages. This series of experiments aimed to investigate the parameters that affect the NP DBR fabrication. In addition, the best electrochemical etching condition was also found for further work. Then, a lateral electrochemical etching process was designed to control the etching direction. Unlike the normal electrochemical etching process, a 500nm SiO_2 layer and a thick photoresist were deposited on the top surface to stop the top-down etching. As a result, the

electrochemical etching can only start in the dry-etched window and etch in the 2D direction. This section discusses the detail of different etching methods for the first time and demonstrates realization of a 1mm laterally etched DBR structure with a high reflectance and a wider stopband, which has never been achieved before.

4.2 DBR etching conditions

4.2.1 Methods

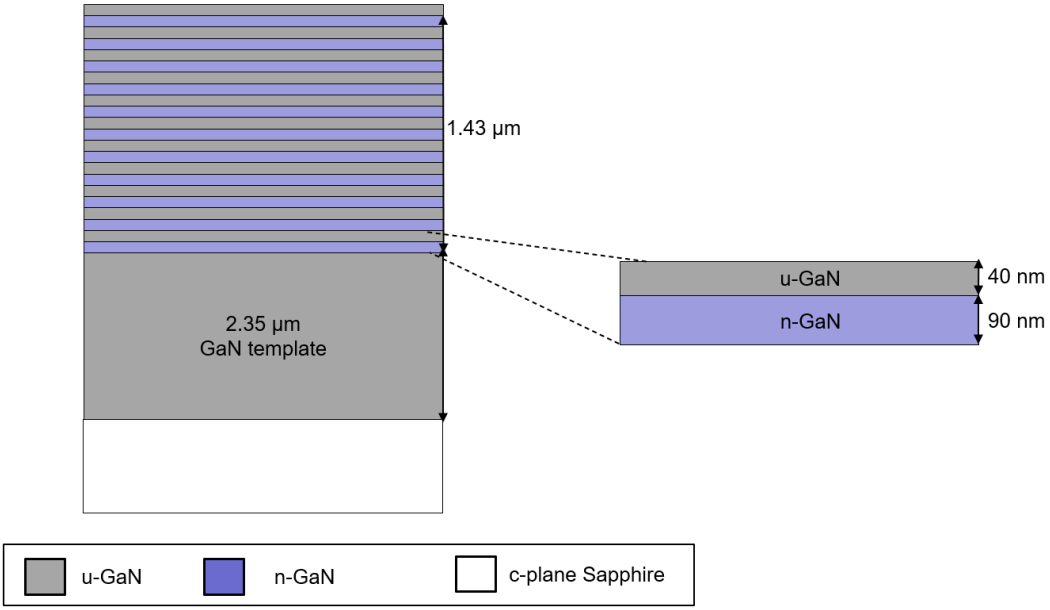

Figure 4.1: Schematic of DBR structure

All DBR samples in this work were grown on GaN templates with a standard two-step GaN growth on a 2-inch (0001) sapphire substrate by metal-organic vapour phase epitaxy (MOVPE). For the GaN template, a 25 nm low temperature (650°C) GaN nucleation layer was grown on a (0001) sapphire substrate under high pressure conditions (600mbar) after thermal substrate cleaning in a hydrogen ambient [37]. Then, a 1.6µm undoped GaN buffer layer was grown under high pressure (400mbar) at 1290°C. This high-pressure GaN buffer layer was aimed to produce an atomically flat surface as the two-dimensional growth dominates over the three-dimensional growth [37]. A 750nm undoped GaN layer was grown subsequently under low pressure (230

mbar). Finally, a DBR structure was grown on these templates. **Figure 4.1** shows the schematic of the DBR structure used in this work. There were 11 periods of the alternating n-GaN/GaN structure. For n-type GaN, the overall doping level was controlled by the silane flow rate as silicon is introduced as the dopant. The thickness of n-GaN was 90 nm and the undoped GaN was 40 nm in each period. In this work three samples are studied which have different n-GaN doping levels, as shown in **Table 4.1**.

Table 4.1: Sample with different doping level in this work.

Sample No:	Doping Level (cm^{-3}):
Sample A	$5*10^{18}$
Sample B	$1*10^{19}$
Sample C	$4*10^{19}$

Once the epi-wafers were ready, the samples were cleaved from the epi-wafer by a diamond scribing pen into rectangular ones with a size of 1cm×2cm. An indium contact was physically pressed at the edge of the short side and fixed the sample at the anode of the EC system. During the etching, all samples were immersed with the size of 1cm×1cm into the electrolyte. The electrolyte used in this work was 0.3M nitric acid (HNO_3), while the EC etching products (Ga^{3+}, NO_3^-) are soluble. All samples were EC etched for 30mins. As described in Chapter 2, the GaN will be oxidized by the injected holes under an anodic bias, and the product is chemically dissolved in an acidic electrolyte. In addition, due to the EC etching being a conductivity-selective etching method, only the n-type layers were etched. Therefore, the alternative layers with a different refractive index in the NP DBR structure were formed. In order to explore how the parameters affect the NP DBR etch results and to find the optimal etch conditions, all samples were EC etched with different applied voltages. Following the

EC etching, the NP DBR samples undergo several characterization steps including optical microscopy and scanning electron microscope (SEM) to evaluate the etching performance.

Table 4.2 list the etching conditions of the samples.

Table 4.2: Sample with different etching conditions in this work.

Bias: / Sample:	4V	5.5V	8.5V	10V
Sample A	-	-	-	A_1
Sample B	-	-	-	B_1
Sample C	C_1	C_2	C_3	C_4

4.2.2 Result and discussion

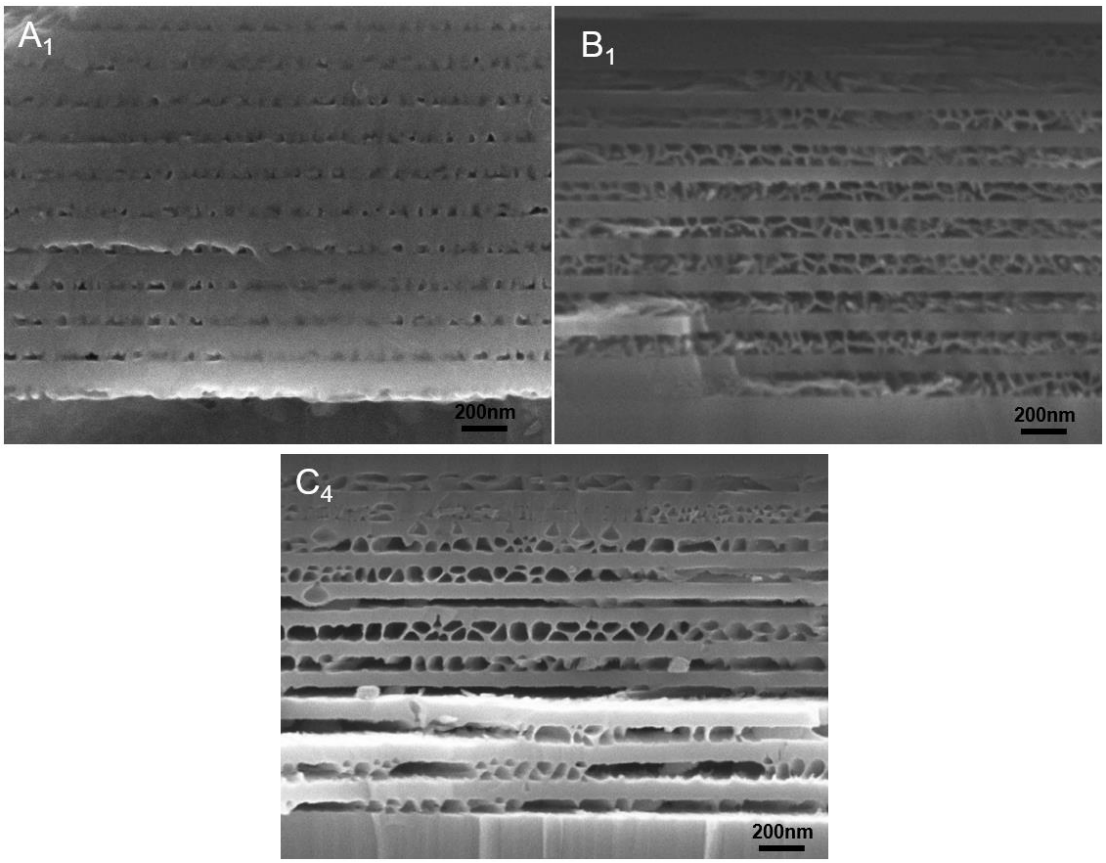

Figure 4.2: Cross-section SEM images of DBR etched according to sample A_1, B_1 and C_4 conditions in Figure 4.5.

The SEM images of samples A, B and C after the EC etching under 10V bias are shown in **Figure 4.2**. Sample A_1 has the lowest doping level, $N_D=5*10^{18}cm^{-3}$. The n-GaN layers in the DBR structure were etched into tiny pores of 15 nm. The thickness of the porous wall is 30 nm. The interface between the porous layer and the unetched layers was extremely unclear, which is harmful to the high-performance DBR structure fabrication. Sample B_1 ($N_d=1*10^{19}cm^{-3}$) exhibits a pore diameter of 50 nm after the EC etching at 10V. The porous wall thickness was decreased to 13nm. The doping level for sample C_4 is $4*10^{19}cm^{-3}$, and the DBR structure was polished after the EC etching at 10 V bias. Most of the DBR is etched completely and peeled off as **Figure 4.4** shows. The cross-section SEM of sample C_4 shows the remaining part. The n-GaN layers under this

EC etching condition were etched as 90 nm pores. In addition, the porous walls were very thin so that some pores merged. Thus, the whole structure was too fragile to support the top structure and n-GaN layers were polished. The SEM images of the DBR etching result further prove the EC etching of NP DBR is highly affected by the doping level of n-GaN layers.

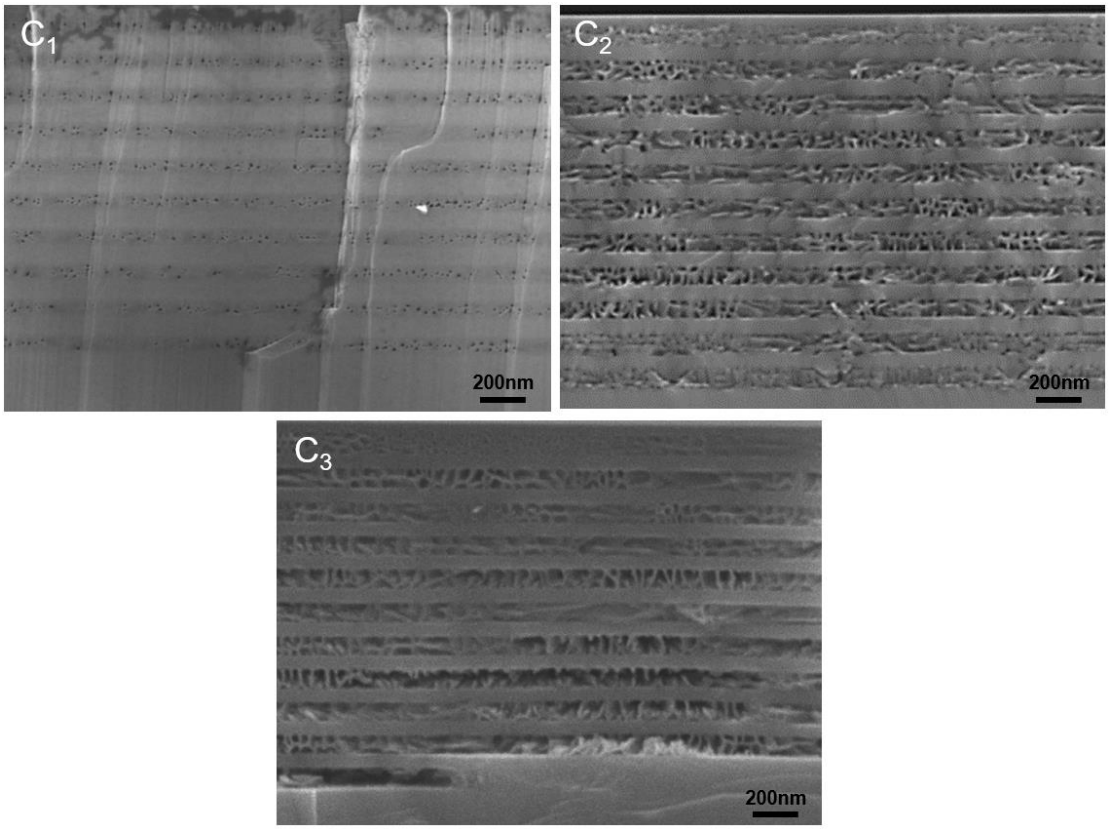

Figure 4.3: Cross-section SEM images of DBR etched according to sample C_1, C_2 and C_3 conditions in Figure 4.5.

Figure 4.3 shows the cross-section SEM images of DBRs etched with different applied biases. All these DBR structures were EC etched on sample C where $N_d=4*10^{19}cm^{-3}$. The applied bias of sample C_1 was 4V and the pores were 8 nm. In addition, only ten layers were etched. The refractive index ratio of the NP-GaN layer/undoped GaN (u-GaN) layer in each period is small due to the low porosity. Sample C_2 was etched with 5.5V bias voltage and the pore size was increased to 25 nm. However, it is difficult for the bottom two n-GaN layers to be etched into large pores. They were etched with 5nm

pores due to the difficulty in ion transport during the EC etching. Sample C_3 was etched with 8.5V and the pore size was further increased to 65 nm. It can be observed that some n-GaN layers were already polished. Although this etching condition has a larger porosity, it cannot be used for the DBR fabrication due to the cracks on the top surface which will be further discussed in **Figure 4.4.**

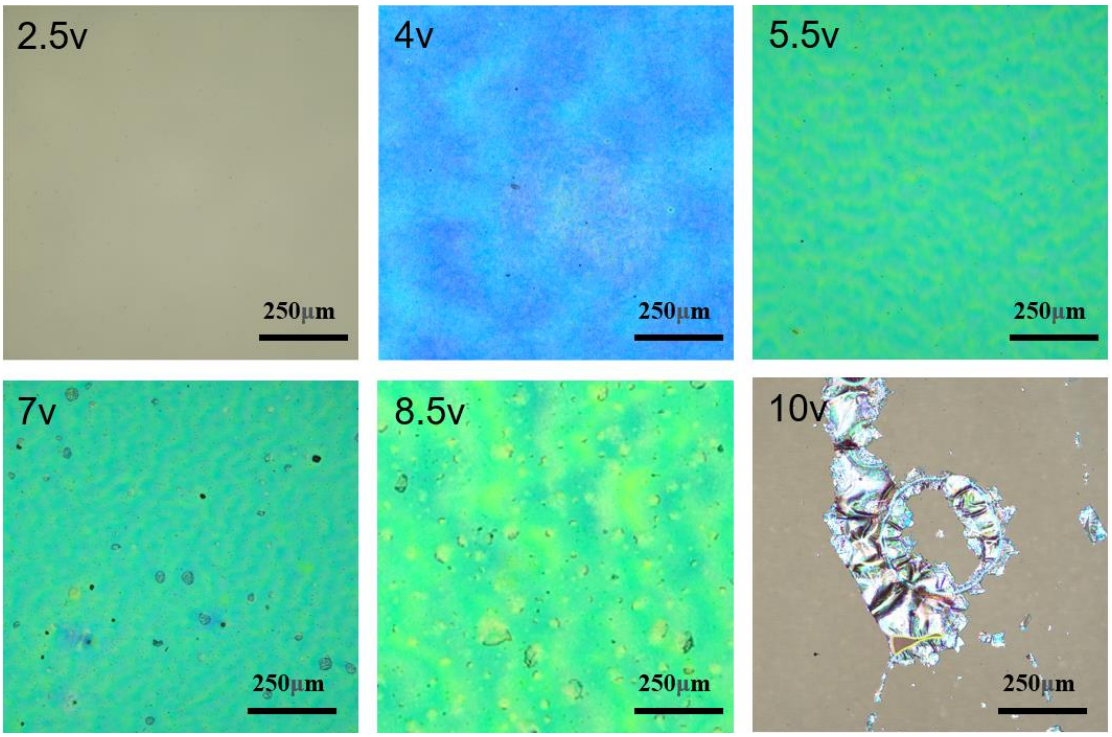

Figure 4.4: Plan-view optical microscope images of sample C after EC etching with applied bias from 2.5V to 10V.

The plan-view optical microscope images of sample C after EC etching with different bias voltages are shown in **Figure 4.4**. When the applied bias was low, no EC etching took place. The n-GaN layers remain intact and no colour changes after 30min EC etching. Unlike the 2V etching, the tiny pores inside the n-GaN layers show up after an EC etching under 4V bias (sample C_1 in **Figure 4.3**). The colour of the sample changes after the 4V etching. However, as discussed in Chapter 2, the small refractive index ratio in sample C_1 leads to the short reflect wavelength. Thus, the microscope image shows blue. According to equations 2.3 and 2.4, the lower refractive index ratio also

leads to a lower reflectance and a narrow stopband width of NP DBR. The etching condition of 5.5V bias voltage (Sample C_2) results in a smooth top surface after 30 min etching. As **Figure 4.3 (C_2)** shows, these appropriately sized nanopores not only have large porosity but are also strong enough to support the whole structure. The microscope images of samples etched in 7V and 8.5V show green colour but also cracks. It means that the higher voltage leads to large pores due to the EC etching of n-GaN being extremely sensitive to the bias change. Since the thickness of n-GaN layer limited the porous size, the colour of DBR after higher bias EC etching tends to have a longer wavelength but has not changed much from the etching above 5.5V. The top surface of 7V etching and 8.5V etching showed cracks or holes that were caused by the N_2 generated during the EC etching. The gas destroyed the porous wall and the top structure lost support. Further increasing the applied bias to 10V leads to the polish of n-GaN. Most of the DBR structure fell off as shown in the last image of **Figure 4.4**. Therefore, the DBR EC etching result is extremely sensitive to the applied bias change. The high-voltage EC etching would destroy the top structure and degrade the performance for the subsequent device fabrication.

By applying electrochemical (EC) etching on the n-GaN/GaN based DBR structure, the n-GaN layer can be either etched or polished. The porosity is highly dependent on the etching conditions. The most important parameters that influence the etching result are anodic bias voltage and the conductivity of the n-GaN layer [38-40]. **Figure 4.5** summarizes an EC etching phase diagram of GaN-based DBR with different doping levels and bias voltages. It can be divided into four regions: not etched, tiny porous, nanoporous and polished. There will be no chemical reactions when the applied bias is low or n-GaN has a low doping level. The DBR structure remains intact and no colour change after the EC etching. When the applied bias or the doping concentration was increased above a critical value, the injection of holes led to the oxidation of n-GaN. Meanwhile, the oxidization products were dissolved in the nitric based acid. The n-GaN layer shows a tiny porosity (<15nm) after etching. The reflected light of the DBR in

this region exhibits a short wavelength. At a higher applied bias or with a higher doping concentration, these tiny pores merged and formed large pores. The refractive index ratio in the NP GaN/u-GaN period became larger leading to a red-shift of the reflecting wavelength. Although increasing the applied bias voltage or doping concentration can further improve the porosity, the pore size is limited by the n-GaN thickness, where the reflecting light wavelength reaches the limitation of design. In addition, the fragile porous wall will cause less support for u-GaN layers and cracks will show up. The DBR will be polished eventually. The conditions for sample C_2 (N_D=4*$10^{19}$$cm^{-3}$, V=5.5V) have been chosen as the best EC etching conditions in future work as there were no cracks after etching and the porosity after etching was relatively large.

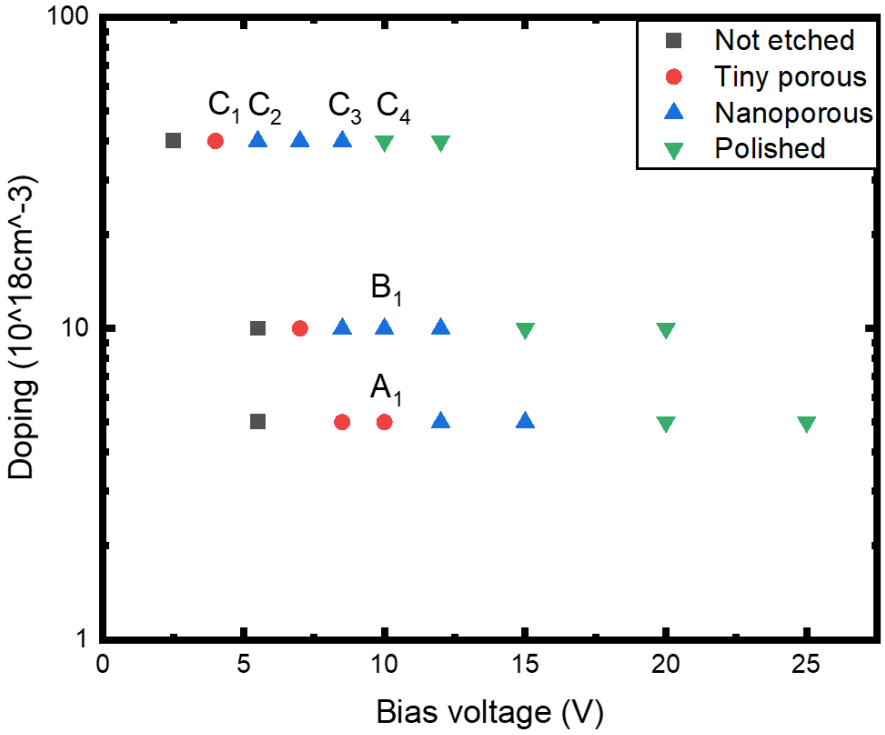

Figure 4.5: Processing phase diagram for EC etching.

4.3 Lateral Electrochemical Etching

4.3.1 Methods

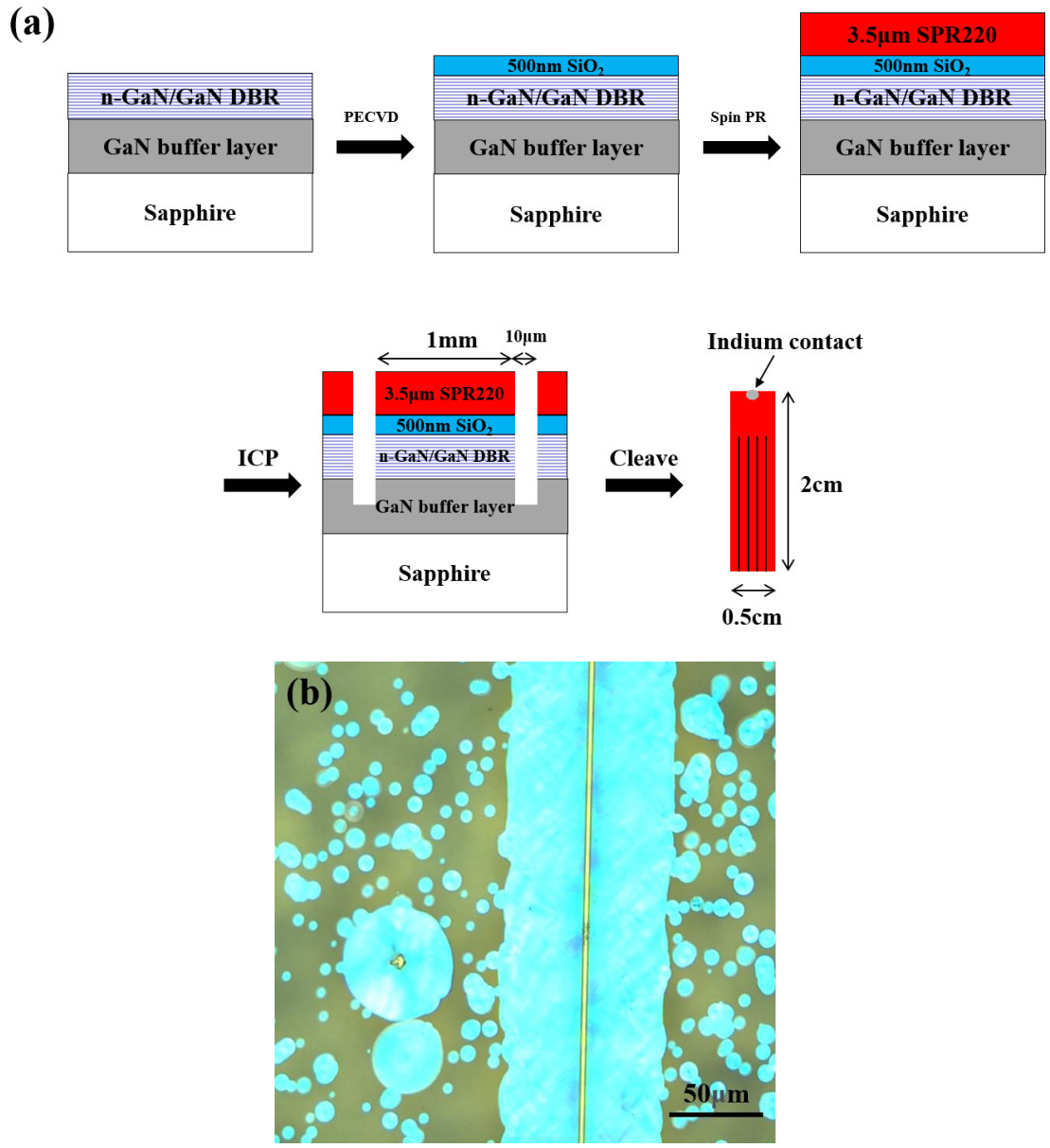

Figure 4.6: (a) Schematic for procedure of lateral etched sample preparation process. (b) Microscope result of unsuccessful lateral etched sample.

A standard n-GaN/GaN-based DBR was first grown on c-plane sapphire by a standard two-step GaN growth technology with MOCVD [41]. The thickness of the n-GaN layer was 90nm and the u-GaN thickness was 40nm. The doping level of n-GaN was

$4*10^{19}cm^{-3}$. Subsequently, the as-grown n-GaN/GaN based DBR wafer was cleaved into two parts using a diamond scribing pen. The two half-wafers were then cleaved into regular rectangle samples of 0.5cm*2cm, for a normal etching and a lateral etching, respectively. **Figure 4.6(a)** shows the schematic of the process for lateral etching. First, on one half wafers, a standard sample cleaning process was employed to remove contaminants, residual dust, and particles on the surface of the sample. Then, a 500 nm SiO_2 layer was then deposited on the top surface with the PECVD system. Next, stripes were patterned using a standard photolithography. After that, the half wafer was dry-etched into 2 μm deep trenches by an ICP etch system to expose the total n-GaN layers in the DBR structure. The distance between the two trenches was 1 mm and each trench was 10 μm wide, as shown in **Figure 4.6(a)**.

Due to that a thin photoresist layer (SPR350) will be consumed during the ICP etch and dissolved in a long wet-etching step, it is important to use a thicker photoresist. SPR220 is a thick photoresist used, which is thick enough to protect the surface from the following dry-etching and wet-etching. **Figure 4.6(b)** shows the microscope result of unsuccessful lateral etched with a thin photoresist. The etchant passed through the protective layer and reacted with the bottom DBR sample leading to many circular etching areas.

For the standard EC etching process, an indium contact was physically pressed at the edge of the short side and immersed into the electrolyte with the immerse size of 0.5cm*1cm. The etching conditions are identical for both samples, which are in a 0.3M nitric acid solution at a positive 5.5V external bias voltage for 4 hours to ensure all areas were etched. The current change was recorded to monitor the etching process. Following the EC etching, the laterally etched sample was then cleaned with solvents to remove the photoresist, and then remove the SiO_2 by HF treatment with 40% BOE for 5mins. All etched NP DBR samples were characterized by optical microscope, reflectivity measurement and scanning electron microscope to assess the quality of the NP DBR.

4.3.2 Result and discussion

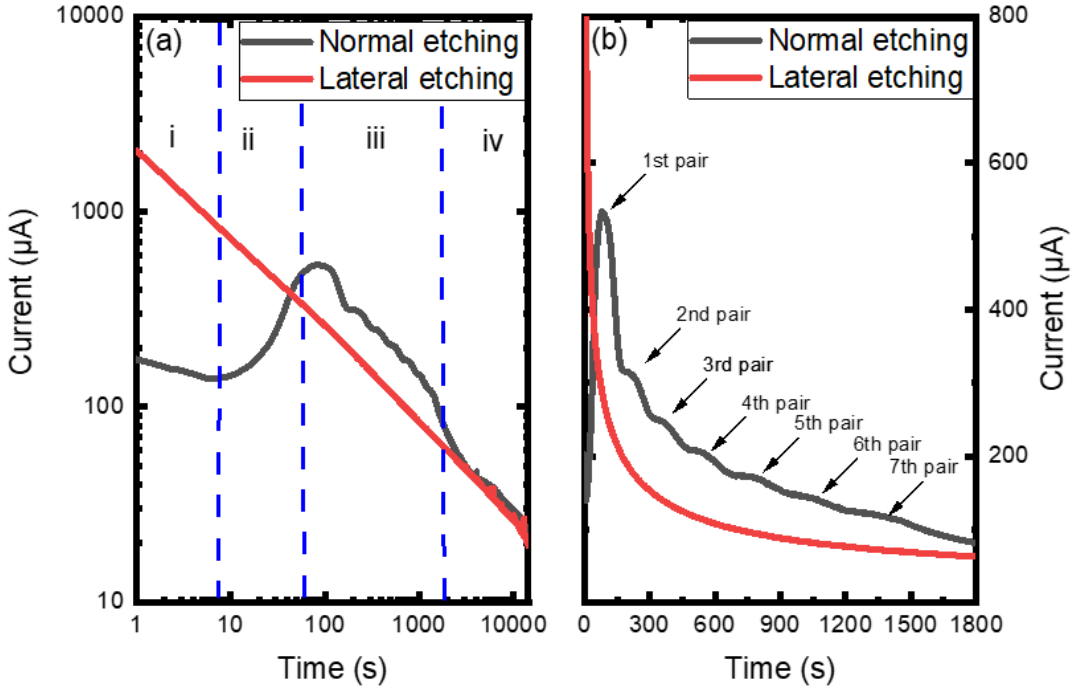

Figure 4.7: (a) The currents measurement as a function of EC etching time. (b) The current measurement detail for step iii of normal etching.

The current changes as a function of EC etching time with 5.5V are shown with the log-log plot in **Figure 4.7(a)**. The current change can exhibit the mechanisms of different etching methods. The normal etching method consists of four steps. In step 1, the etching only takes place at the edge of the sample where the n-GaN were exposed to the etchant. Thus, the current decreases at the first 10s. As there was no protection from the SiO_2 on the top surface, the defects on the top u-GaN layer were etched as tiny penetrating openings subsequently. The current increase in step 2 means the etchant reached the first underlying n-GaN layer and started to etch from these points. From this point, the nanopores spread in a radial form and formed a circle etching trace. Step 3 is from the 80s to the 1800s. In this step, the current shows oscillation characteristic that indicates the normal etching method is a top-down process. This step will be discussed in detail in **Figure 4.7(b)** later. Then, a significant current decrease, which

suggests the EC etching was completed, and the minimum current was obtained in step 4.

The current changing for the lateral etched DBR was shown as a nearly straight line in a log-log plot. Due to the surface of the sample was protected with 500nm SiO_2 and photoresist, the EC etching can only start with the exposed sidewalls. In addition, there were four ICP-etched trenches on the lateral etched sample. Therefore, the current for the lateral etching at the start was approximate 6 times higher than the current for normal etching. With the nanopores being etched deeper, the ion/mass transport becomes much more difficult in the high-aspect-ratio nanopores (length: diameter >10000:1). So, the slowing down of the dissolution rate of GaN oxide products leads to increasing of the overall resistance [42]. The etching rate decreases slowly throughout the remaining etching process.

The current measurements for step 3 of the normal etching are shown in detail in **Figure 4.7(b)**. As discussed before, the current for the normal etching shows clear oscillation characteristics in step 3, and there were altogether seven oscillations–that can be observed in **Figure 4.7(b)**, which correspond to each EC etching on every n-GaN layer. For each oscillation, the current increased when the etchant reached the n-GaN layer via penetrating openings on the u-GaN layer. After most of this n-GaN layer was etched, the current decreased quickly. Meanwhile, the defects on the next u-GaN layer were etched as new penetrating openings to the next n-GaN layer and made the etchant diffuse to a further layer. By repeating the above process, the normal etched method can etch the n-GaN as nanoporous from top to bottom layer by layer. However, with the layer increasing, it becomes more and more difficult for the etchant to diffuse into the bottom n-GaN layers, and the current reached minimum finally. It is worth noticing that the current of normal etching at step 3 is higher than that of lateral etching, due to that the normal etched sample had more etching points than the lateral etched sample and thereby much faster etching rate. As the top-down diffusion in the normal etching

stopped, the final currents for these two etching methods were nearly equal due to the only lateral etching left.

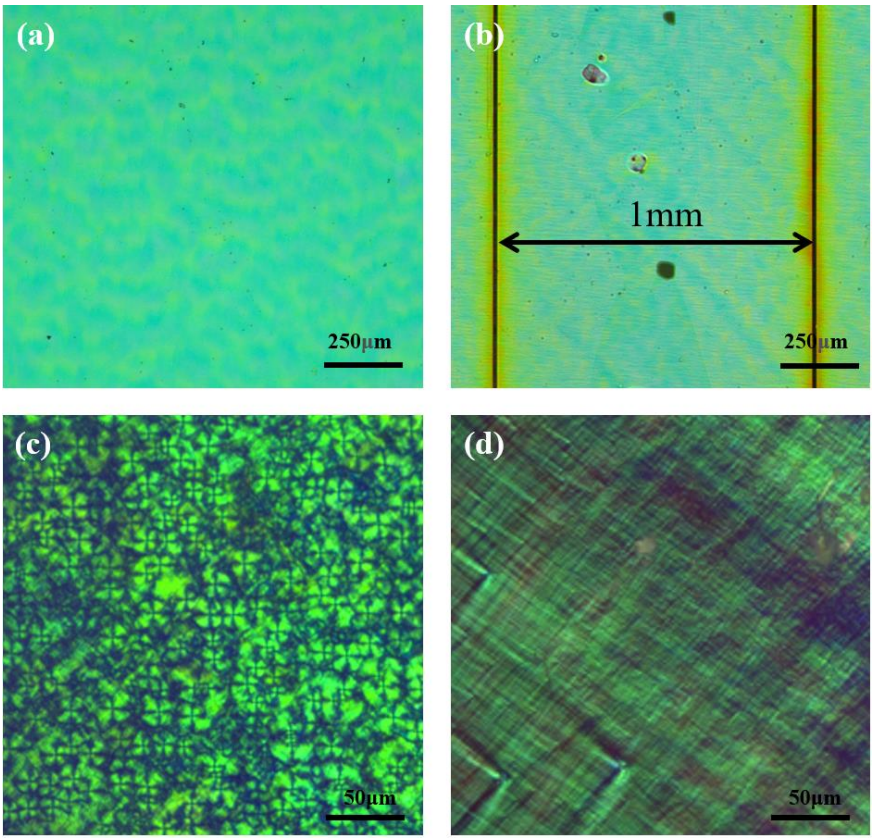

Figure 4.8: Plan-view optical microscope image of (a) normal etched sample without polarization. (b) lateral etched sample without polarization. (c) normal etched sample with 90 degree polarization. (d) lateral etched sample with 90 degree polarization.

Since the porous structure has anisotropic reflectivity, polarizing optical microscope is applied to figure out the etching direction of the porous of DBR samples after etching. **Figure 4.8(a)** and **(b)** show the plan-view optical microscope images without polarization of samples after normal etching and lateral etching, respectively. In both EC etching methods, all samples were green, indicates that the thickness ratios of the nanoporous layer/ unetched layer were the same. However, due to the light scattering near the trench, the DBR after etching in **Figure 4.8(b)** tends to be yellow near the dry-etched window. The distance between two ICP etched trenches was 1mm. The part

between the two trenches was etched smoothly. After applying 90-degree polarizing, the detailed etching trace of normal etching and lateral etching were shown in **Figure 4.8(c)** and **Figure 4.8(d)**. Since there was not any protection on the top surface for normal etching, the dislocations on the surface formed tiny pipes that connect the etchant and n-GaN layer. Then, the EC etching started with these points and left radiating pores, as shown in **Figure 4.8(c)**. The microscope image of lateral etching in **Figure 4.8(d)** is largely different. A uniform porous trace was observed. It is attributed that the top SiO_2 and photoresist prevent the etching from starting with the top surface which leads to a lateral etching at each n-GaN layer. Although some defects affected the etching, they did not form round etching traces in the normal etching. Thus, the top protection on the DBR sample is better for formation of a uniform nanoporous layer. The following SEM results show more detailed information.

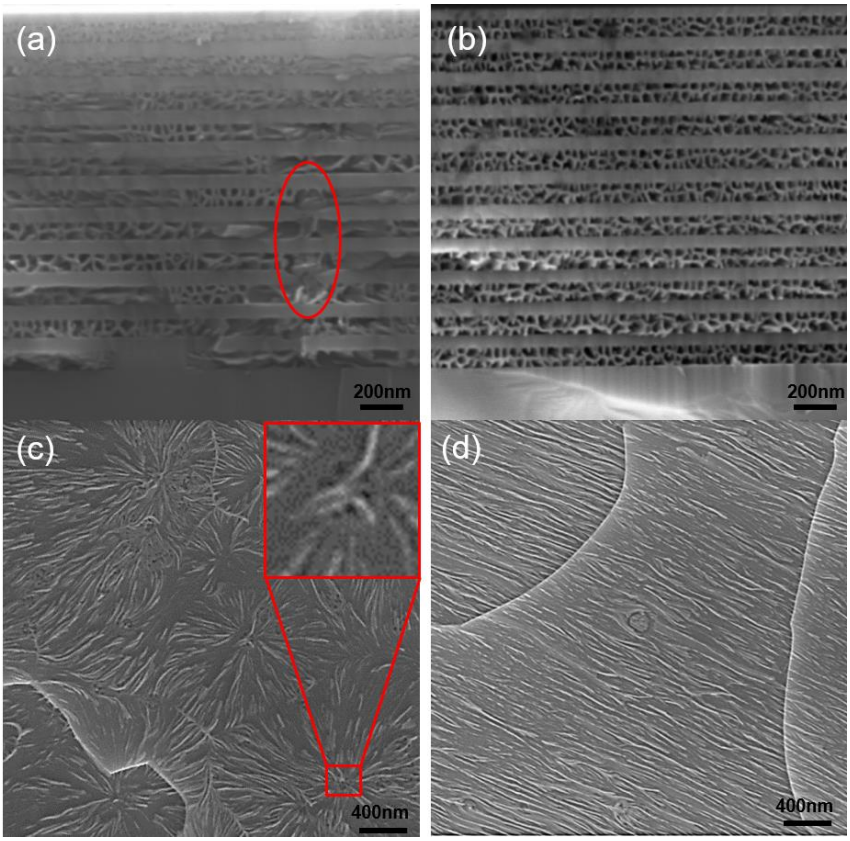

Figure 4.9: (a) cross-sectional view SEM result of normal etched sample. (b) cross-sectional view SEM result of lateral etched sample. (c) top-view SEM result of normal etched sample. The inset image is the zoom in of etched defect. (d) top-view SEM result of lateral etched sample.

After the EC etching, both samples were cleaved and checked with the cross-section view SEM observation. The cleaved face of the laterally etched sample was parallel to the trench. **Figure 4.9(a) and (b)** show the cross-section view SEM images of the normal etching and the lateral etching samples, respectively. In each case, the thickness of the nanoporous layer and un-etched layer in both samples after etching were 90 nm and 40 nm, which is similar to the thicknesses designed for the MOCVD growth. However, in **Figure 4.9(a),** the pores of the normal etching sample were disorganized. This is due to that the orientation of the nanopores are not completely perpendicular to the cleaved surface. Thus, some parts can be observed with complete holes and some parts seem not have been etched. In addition, only the top nine layers of n-GaN were

etched with large holes, while the bottom two layers were small porous. It can also be observed that the bottom layers at some parts of the n-GaN layers were not etched. These bottom unetched layers further proved that the etching for the GaN-based DBR without top protection advanced from top to bottom. The bottom n-GaN layers are difficult to be etched as the transport of ion/mass is harder at the bottom. The red circled part in **Figure 4.9(a)** shows some holes that penetrate the adjacent n-GaN layers. These holes were caused by the EC etching of defects that have an enhanced conductivity. Meanwhile, the ions and gas produced in EC etching can be transported to the electrolyte via these penetrated openings. In contrast, the porosity of the lateral etched sample in **Figure 4.9(b)** was much more uniform. The interfaces between the porous layer and unetched layer were etched very clear. Since the samples were dry-etched to open a window and expose all eleven n-GaN layers, the etching direction is extremely restricted inside each n-GaN layer. No penetrate holes were found after applying lateral EC etching on DBR samples, and all n-GaN layers were etched into large pores. The pores were perpendicular to the dry-etched trench and laterally etched towards the centre between two trenches. By image analysis of SEM results, the porosity of the normal etched sample is 50%, whereas the porosity of the lateral etched sample is increased to 61%. Although the average sizes of pores for both samples are nearly the same (25nm in average), the well-distributed holes inside the n-GaN layer will occupy as much space as possible, making the increment of porosity.

Subsequently, the top undoped layers of the samples were removed using the ICP etching for SEM top view observation. **Figure 4.9(c)** and **(d)** are the top view SEM results of the normal etched sample and lateral etched sample, respectively. In **Figure 4.9(c)**, the etching trace is in radial shape and spread like a circle. Since there was no top protection, the etchant first reacted with the defects on the undoped layer and formed tiny penetrating to the bottom layer. These openings are shown as the red circle part in **Figure 4.9(a)**. The under-layer etching can spread around this point. The observed openings also explain the ununiform display of some porous layers in **Figure**

4.8(c) and **4.9(a)**. The inset figure is one of the "etching centres". Some defects were already etched and left holes here. For the lateral etching process, the top surface was protected with SiO_2 and photoresist which eliminated the possibility of the spread of etchant from top to bottom. In addition, the current was confined in the n-GaN layer. Therefore, the etching can only start from the dry-etched window and extend in the same direction with the same rate. Although some etched defects can be observed, it does not affect the overall etch direction.

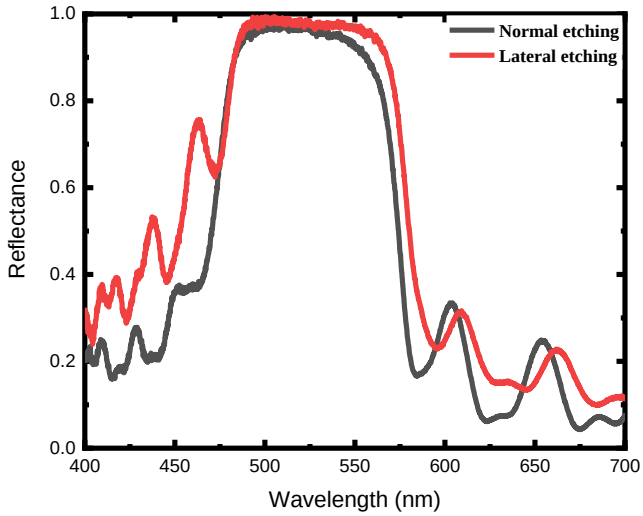

Figure 4.10: Direct reflectance spectra of DBR samples with different etching methods. The incident light is non-polarized light source.

Figure 4.10 presents the direct reflectance spectra of samples after normal etching and lateral etching. Both samples have shown very high reflectivity as DBR structures. The reflectance was 97.3% with 520 nm as a central wavelength and a stopband of 104 nm for the sample with normal etching. The central reflectance of the lateral etched sample was measured to be 98.5% at 525nm with a 124nm stopband. As discussed in SEM results, the porosity of the lateral etched DBR was higher than the normal etched DBR, leading to the larger refractive index ratio of the lateral etched sample. Therefore, the lateral etching method can significantly increase the optical performance of nanopores

based DBRs with not only a higher reflectance but also a wider stopband. A side peak is observed at 463 nm in the lateral etched sample reflectance spectra. This is due to the anisotropic refractive index of the laterally etched pores, which leads to the decreasing of reflectance at a short wavelength in 0 polarization degree [43].

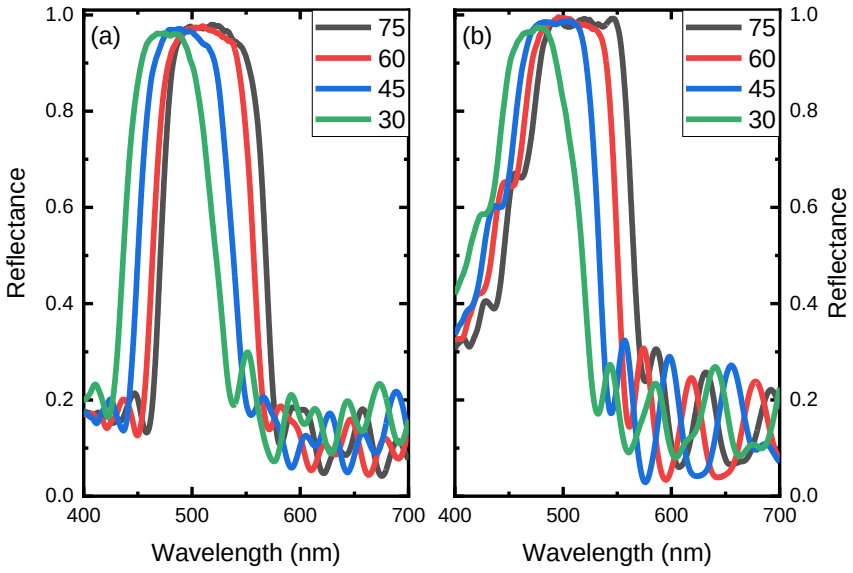

Figure 4.11: Angle-dependent reflectance spectral of (a) normal etched DBR sample (b) lateral etched sample at detection angle from 75° to 30°. The incident light is non-polarized light source.

The angle-dependent reflectance spectra of **(a)** normal etched DBR sample and **(b)** lateral etched sample at a light incident angle from 75° to 30° were shown in **Figure 4.11**. Due to the spot size of the incident light was 1mm which is exactly the same as the distance between two ICP-etched trenches, it was required to place the light spot inside the etching area and avoid the light scattering on the trenches. In **Figure 4.11(a)**, the central wavelength and the reflectance of the normal etched DBR sample were measured to be 514.6 nm/97% at 75° and 475.5 nm/96.2% at 30°, respectively. The stopband width shows a decreasing trend with decreasing the detection angle. It decreases from 94.6 nm at 75° to 87 nm at 30°. For the lateral etched DBR in **Figure 4.11(b)**, it is worth noticing that the side peak became weakened with increasing the

incident angle. The central wavelength and the reflectance were measured to be 519.2nm/98.3% at 75° and 472.4nm/97.2% at 30°. The stopband width was 120 nm at 75° and decreased to 106.9 nm at 30°. The relationship of Bragg spectral position (λ_B) against the incident light angle is explained with the following equation [44]:

$$\lambda_B = 2d\sqrt{n^2 - (\sin\theta)^2} \tag{4.1}$$

Where *d* is the thickness of total porous GaN/ undoped GaN pair, *n* is the average refractive index of each pair and θ is the incident light angle with respect to the sample surface.

4.4 Conclusion

To summarize, we have applied electrochemical etching to form NP GaN-based DBRs with high reflectivity. The influence of the voltage and the doping level of n-GaN in EC etching was summarized in **Figure 4.5** as a phase diagram. The higher applied bias or higher doping level would lead to a large porosity or even polished n-GaN layers. In addition, the oversized pores would cause cracks on the surface which are not beneficial for high reflectivity DBR fabrication. The DBR with N_D=4*$10^{19}$$cm^{-3}$ in n-GaN layers with an etching in 5.5V bias voltage was measured to be the best condition to form the DBR structure. Moreover, a lateral etching method was proposed to improve the optical performance of the DBR structure. The sample was protected with SiO_2 and photoresist during the EC etching to realize the lateral etching inside each n-GaN layer. The current measurements of the normal etching and the lateral etching have exhibited the mechanisms of these two methods. Meanwhile, the lateral etching shows uniform nanopores after EC etching, leading to a higher porosity. The direct reflectance of the lateral etched sample was 98.5% with 124 nm stopband width, which was better than the 97.3% with 104 nm stopband width of the normal etched sample. The enhancement can be attributed to the protection of the top surface as well as the well-organized porous structure in the DBR.

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Chapter 5: Fabrication and characterization of nearly lattice matched DBRs.

The heavily silicon doped GaN samples typically face the problems of rough surface and saturated conductivity. Recently, it has been reported that heavily silicon-doped n^{++}-AlGaN with ≤ 5% aluminum (Al) can maintain an atomically flat surface and exhibit enhanced conductivity. Therefore, we propose to introduce heavily silicon-doped n^{++}-$Al_{0.01}Ga_{0.99}N$ layers instead of the heavily silicon-doped n^{++}-GaN layers in the widely used multiple pairs of heavily silicon-doped n^{++}GaN/undoped-GaN structure for fabrication of a lattice-matched distributed Bragg reflector (DBR) by using an electrochemical (EC) etching technique. As the Al content is tiny, the lattice mismatch between n^{++}-$Al_{0.01}Ga_{0.99}N$ and undoped GaN can be safely ignored. The heavily silicon-doped layer can be converted into nanoporous (NP) layers after EC etching while the undoped GaN stays intact, which leads to a significant large refractive index ratio between the NP-layer and the undoped GaN, thus forming a DBR. In this work, an NP-$Al_{0.01}Ga_{0.99}N$/undoped GaN based DBR is achieved and exhibits a much smoother surface, an enhanced reflectivity and a wider stopband compared to the typical NP-GaN/undoped GaN-based DBR. Furthermore, a series of NP DBR structure with multiple pairs of n^{++}-$Al_{0.01}Ga_{0.99}N$/undoped GaN have been fabricated by controlling the thickness of multilayers during the MOCVD growth, which all demonstrate high performance with the reflectance wavelengths in the range from blue to dark yellow.

5.1 Introduction

A high-performance distributed Bragg reflector (DBR) requires a high reflectivity and a large stopband, which are both determined by the refractive index ratio between two alternating layers of each pair in the DBR structure. It means increasing the contrast in refractive index ratio between materials can simultaneously improve the reflectivity and stopband of DBRs. Since high-performance VCSELs are all achieved by epitaxial growth, the alternating layer materials need to be lattice-matched and have a sufficiently high refractive ratio in each pair. So far, epitaxially grown AlAs/GaAs based DBRs have achieved great success and have been widely used. Thanks to the large refractive index ratio (n_{AlAs} = 2.89 and n_{GaAs}=3.42) as well as the nearly lattice-matching between AlAs and GaAs, the GaAs-based VCSELs exhibit high performance [1, 2].

Different from the AlAs/GaAs based DBRs, achieving high-performance epitaxially grown Al(Ga)N/GaN based DBR remains a great challenge for III-nitride based optoelectronic devices[3-6]. Firstly, the large lattice-mismatch between AlN and GaN (2.4%) generates a high density of dislocations. In addition, it also causes a high tensile strain when Al(Ga)N is grown on GaN, which leads to to cracking issues. Secondly, the refractive index difference between GaN and AlN (~ 0.2) is so small as to require a large number of pairs in order for obtaining a reasonably high reflectivity. The small refractive ratio also means a narrow stopband. Furthermore, high-density dislocations, generated as a result of the large lattice-mismatch between AlN and GaN, naturally extend to any overlying structures, thus potentially causing a degradation in the optical performance of an active region grown on top of the DBR.

In principle, the AlN layers can be matched to GaN by doping an appropriate amount of In in AlN to form AlInGaN, such as $Al_{0.82}In_{0.18}N$ lattice matched with GaN [7]. However, maintaining the required alloy content for the high crystal quality AlInN throughout the whole process of the DBR growth is extremely difficult. Firstly, InN is required to grow at a low temperature (<700^0C), but AlN is normally grown at a high

temperature (>1100^{0}C). Moreover, a severe miscibility gap is caused by the large difference in interatomic spacing between AlN and InN (even larger than that between AlN and InN). This miscibility gap will generate indium segregation and non-uniformity [8, 9]. In addition, the refractive index difference between AlInN and GaN is even smaller than that between AlN and GaN [10]. Therefore, the typical AlInN/GaN based-DBRs usually require a vast number of alternating periods to achieve a high reflectivity which undoubtedly increases the growth time.

In chapter 4, we introduce lattice-matched NP DBR structures using multiple pairs of nanopores (NP) GaN and GaN. By applying the electrochemical (EC) etching, the heavily silicon doped GaN (i.e., n^{++}-GaN) is converted into NP-GaN which has a significantly lower refractive index than that of GaN [11-19]. It has been highlighted in previous work that EC etching technique sensitively depends on the conductivity of silicon doped GaN. Although the NP DBR structures with high reflectivity and wide stopbands have been obtained by improving the etching method, it is still a challenge to further improve the performance of large-area NP DBRs. So, it is necessary to grow n-GaN with a very high doping level. However, heavily doped n^{++}-GaN leads to surface roughness, the interface between n^{++}-GaN and undoped GaN during the epitaxial growth. These fundamental issues form the main obstacles to realising the high-performance DBRs with large area.

It was reported that the heavily silicon-doped AlGaN can not only maintain an atomically flat surface but also exhibits enhanced conductivity when the Al content is not higher than 5% [20-23]. In this chapter, we are proposing to flow a tiny amount of Al precursor during the growth of the heavily doped n^{++}-GaN. It will form heavily doped n^{++}-$Al_{0.01}Ga_{0.99}N$ layers instead of n^{++}-GaN layers in GaN based DBR. In addition, the lattice-mismatch between $Al_{0.01}Ga_{0.99}N$ and GaN is even smaller than that between AlAs and GaAs and can be safely ignored. As a result, our n^{++}-$Al_{0.01}Ga_{0.99}N$/u-GaN based NP DBR exhibits an atomically smooth surface. After EC etching, a sharp interface is shown between NP-$Al_{0.01}Ga_{0.99}N$ and undoped GaN. In addition, this leads

to enhanced performance in terms of reflectivity and stopband compared with the NP-GaN/undoped GaN counterpart. Under the identical bias used for the EC etching, the n^{++}-$Al_{0.01}Ga_{0.99}N$ shows an enhanced conductivity by a factor of 2.5 compared with the n^{++}-GaN.

5.2 Methods

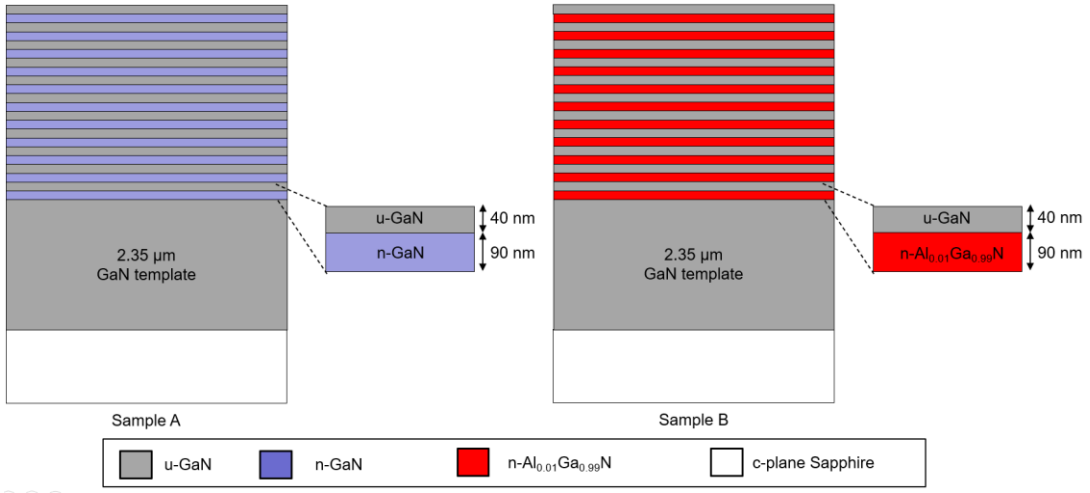

Figure 5.1: Schematic of DBR samples.

All epi-wafers used in this work were grown on 2-inch (0001) sapphire substrates by metal-organic vapour phase epitaxy (MOVPE) with a widely used two-step growth method. The initial GaN buffer growth is identical for all the epi-wafers: a 25nm low temperature (650°C) GaN nucleation layer was grown on a (0001) sapphire substrate after an initial annealing process under H_2 at a high temperature. Then, a 1.6µm undoped GaN buffer layer was grown under high pressure (400mbar) at 1290°C followed by a 750nm low pressure (230mbar) undoped GaN layer. The subsequent DBR structure growth for two kinds of samples was different, labelled as Sample A and Sample B, respectively. The schematic of DBR samples is shown in **Figure 5.1.** For Sample A, 11 periods of n^{++}-GaN/GaN alternating layers were grown as DBR structure where silane was used to supply silicon dopant. The n^{++}-GaN layer thickness was designed as 90 nm and the undoped GaN layer was 40 nm in each period. For sample

B, the DBR growth step was carried out under almost the same conditions as those for sample A and the only difference was that a small amount TMAl flow was introduced during the high doped GaN growth in each pair while the undoped GaN growth condition did not change. Therefore, a DBR structure of 11 pairs of alternating n^{++}-AlGaN layer (with a tiny amount of Al content) and undoped GaN layer are formed.

The Hall measurement was applied for measuring the doping level. First, a square shape of samples was cut out with an area of 2cm*2cm from each of the two wafers. Then, a dry-etching process was used for the samples by an Inductively Coupled Plasma (ICP) etching system to remove the top 40 nm undoped GaN layer. The indium contacts were made at the four corners of the square and were annealed by Rapid Thermal Annealing (RTA) system at 420°C to make sure the contact ohmic. The subsequent standard Hall measurements were performed for both sample A and sample B.

Bruker D8 X-ray diffractometer has been used to determine the Al content in n^{++}-AlGaN, which is 1%. This result is consistent with the Energy dispersive X-ray spectroscopy (EDX) measurement result. The EDX system is installed as a part of Raith 150 Scanning Electron Microscope (SEM) system. The surface morphology of samples was also examined by the SEM.

The lateral EC etching were carried out on both samples as introduced in chapter 4. A 500 nm SiO_2 film was first deposited on each epi-wafer by a standard PECVD technique. Then a thick photoresist was applied over the SiO_2 for the following ICP dry-etching process and EC etching process. These protection layers aim to prevent the EC etching along with a vertical direction potential via any defects such as either V-pits or screw dislocations. In order to enhance the EC etching, parallel trenches with a spacing of 1 mm were fabricated by a standard photolithography technique and the ICP dry-etching process. These trenches were etched through all the 11 pairs of alternating n^{++}-GaN (or n^{++}-$Al_{0.01}Ga_{0.99}N$) layers and undoped GaN layer to expose the high doped layers to the etchant during the EC etching. Finally, each epi-wafer was diced into a

number of samples with a rectangular shape of 1×2 cm^2. All the EC etchings were performed at room temperature using a Metrohm Autolab PGSTAT204 system as a potentiostat to record the etching data. EC etching was conducted in 0.3M nitric acid (HNO_3) solution under 5.5V bias voltage. The indium contact was physically pressed at the edge of the sample and connected to the anode probe. A platinum plate was used as a cathode. The injection current was well monitored during the whole EC etching process which continued for 3 hours. After the EC etching, the SiO_2 on the top surface was removed by a standard HF treatment with 40% buffered oxide etch (BOE) for the following direct reflectivity measurement.

Our simulation was carried out with Lumercial FDTD simulation software. The import data was based on the structural data obtained from the cross-sectional SEM images. The effective refractive index for GaN is 2.45 whereas the effective refractive indices for NP-$Al_{0.01}Ga_{0.99}N$ and NP-GaN are 1.52 and 1.76, respectively [24]. The electric field used in the simulation was a plane wave source with an emission wavelength from 400 nm to 700 nm. The source was placed above the DBR to directly irradiate the sample surface. A frequency-domain power monitor collected all reflect wavelengths. The simulation runed for 1000fs with a minimum of 22 mesh points per wavelength, where the boundary conditions were all set as perfectly matched layers (PML).

5.3 Results and discussion

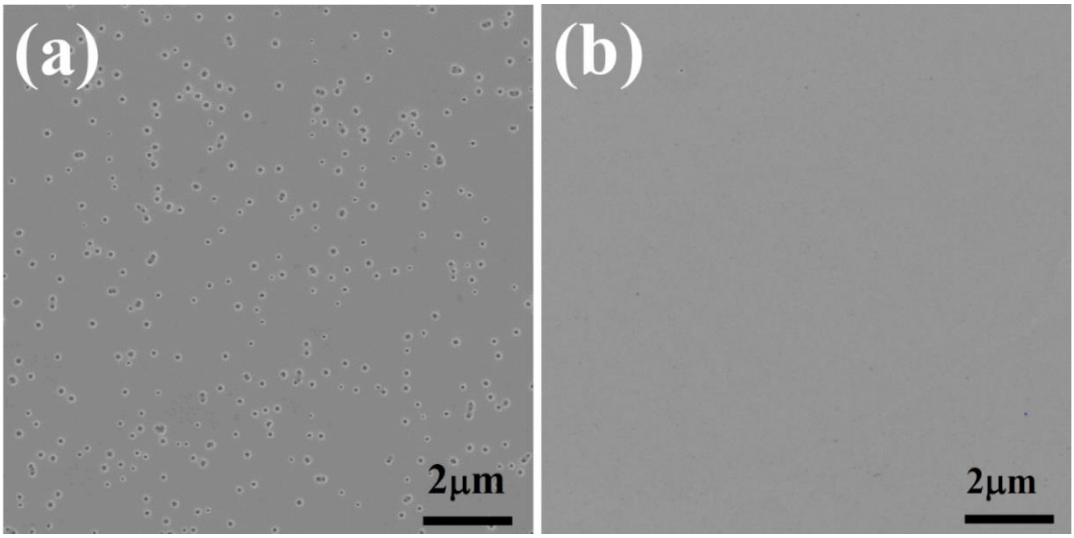

Figure 5.2: Plan-view SEM images of (a) sample A and (b) sample B prior to EC etching.

The plan-view SEM images of sample A and sample B prior to EC etching are shown in **Figure 5.2a** and **Figure 5.2b**, respectively. For sample A, **Figure 5.2a** displays many V-pits on the surface after MOCVD growth which were generated due to the heavy silicon-doping on GaN.[24-27] This also means that further increasing the silane (SiH_4 is a typical n-type dopant precursor) flow rate cannot increase the doping level, as high SiH_4 flow rate will deteriorate the surface completely. Indeed, the appearance of a high density of V-pits will no doubt degrade the performance of any device structure grown subsequently on its top. In remarkable contrast, sample B exhibits a very smooth surface, and no V-pits are observed in **Figure 5.2b**, although the SiH_4 flow rates for sample A and sample B were the same for n-doped layer growth. The results further confirm that the introduction of a small amount of Al precursor during the growth of heavily silicon-doped GaN (leading to the formation of n^{++}-$Al_{0.01}Ga_{0.99}N$ layers in the DBR structure) is beneficial to achieving a smooth, V-pits free surface. The doping concentration of the heavily silicon doped layers were measured by Hall measurement, where sample A

is $4*10^{19}cm^{-3}$ and sample B is $4.75*10^{19}cm^{-3}$. In addition, due to the low Al content, the lattice-mismatch between $Al_{0.01}Ga_{0.99}N$ and GaN in each pair can be safely ignored.

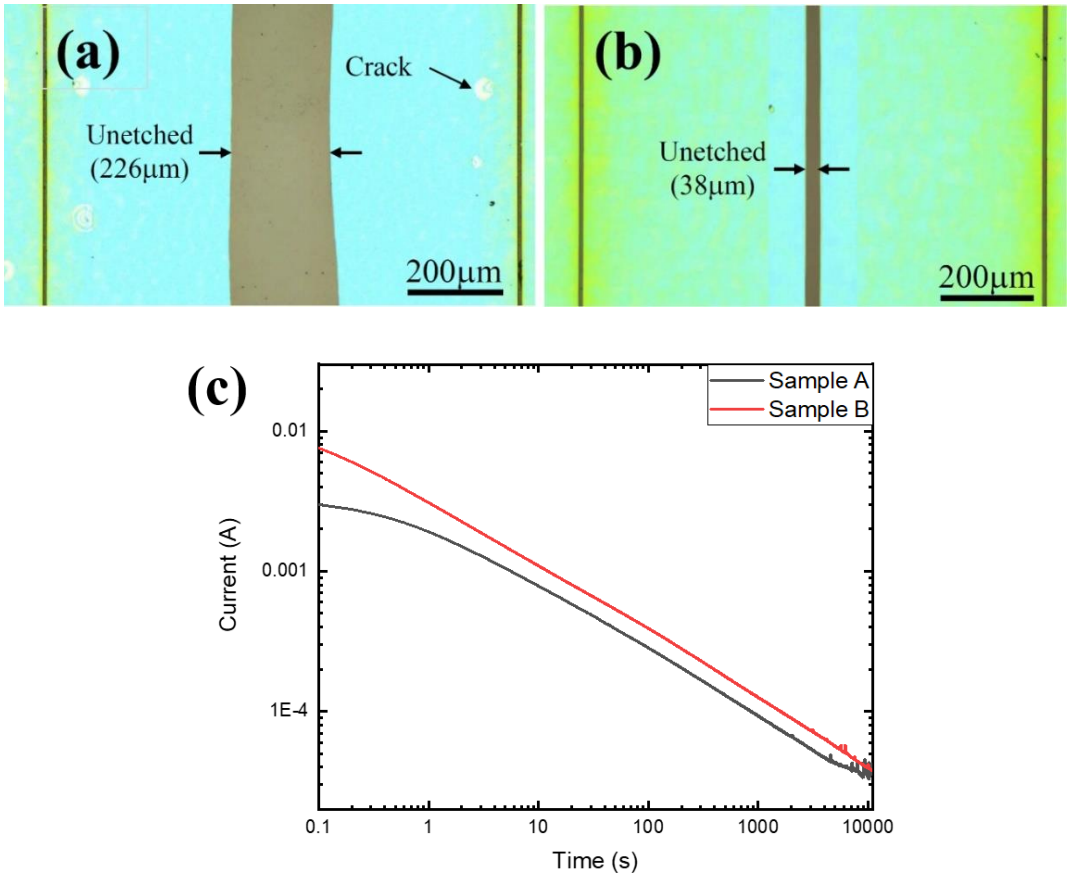

Figure 5.3: Plan-view optical microscopy images of (a) Sample A and (b) Sample B after EC etching (scale bar = 200 mm). The spacing between two neighbouring trenches is 1 mm. (c) The injection current of Sample A and Sample B in EC etching.

Figure 5.3 shows the plan-view optical microscopy images of sample A and sample B after 3 hours of EC etching under the same conditions, respectively. Due to the sample surface being covered with a protective layer of SiO_2 and photoresist, the EC etching starts from both sides of each trench, then spreads to the centre in a 2D direction. By carefully monitoring the injection current (shown in **Figure 5.3c**), the injection current for sample B is 2.5 times higher than that for sample A which proves that the conductivity of sample B is 2.5 times higher than that of sample A. In **Figure 5.3a**, the average unetched part in sample A was about 230 μm between two neighbouring

trenches. In contrast, sample B exhibits an unetched part with only a width of 38 μm on average. Once again, it has further confirmed that the EC etching was significantly enhanced by introducing 1% aluminium during the high silicon doped layers growth.

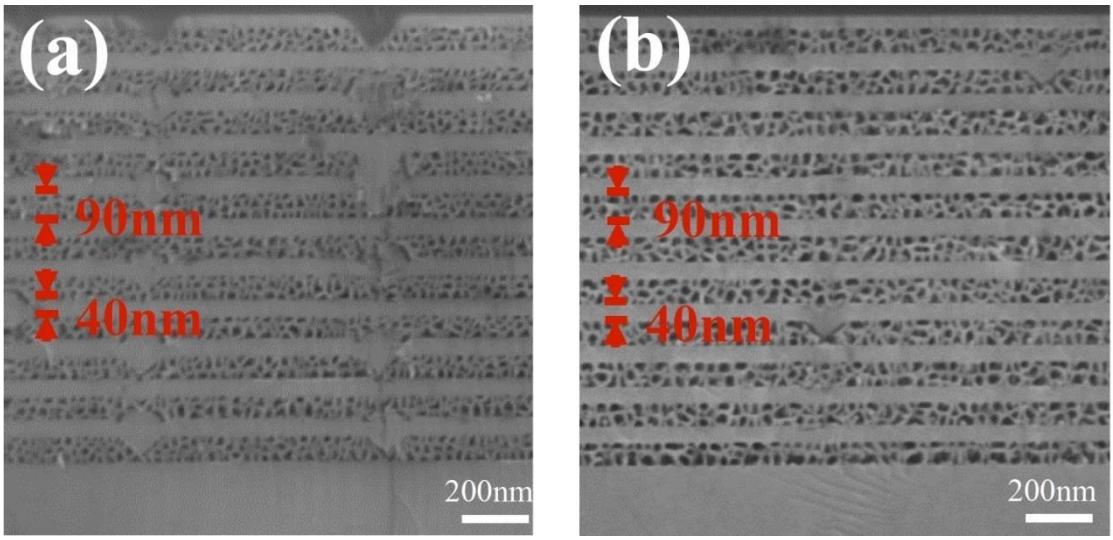

Figure 5.4: Cross-sectional SEM image of (a) Sample A and (b) Sample B after EC etching.

Figure 5.4 shows the cross-sectional SEM images of sample A and sample B after EC etching under the same conditions, respectively. In each case, all 11 layers of high silicon doped layers were transformed to nanopores in both sample A and sample B. However, by carefully examining **Figure 5.4**, it can be easily found that the average size of pores in sample A is smaller than that in sample B. By analysing the cross-sectional SEM images for both samples with software (ImageJ), the size of pores in sample A is 20 nm on average with a porosity of 58%. In addition, the V-pits were observed in sample A, leading to that some parts of the heavily doped GaN layers nearby cannot be converted into porous layers by EC-etching. Therefore, the interfaces between NP-GaN and undoped GaN were not etched sharply. In stark contrast to sample A, the introduction of 1% Al during the heavily doped GaN layers (i.e., sample B) growth leads to V-pits free structure. As a result, the NP-$Al_{0.01}Ga_{0.99}N$ were EC-etched to be nanoporous uniformly. Detailed image analysis indicates the size of porous of sample B was increased to 35nm and the porosity was increased to 71%. The larger

porosity implies that the effective refractive index ratio between the nanoporous layer and unetched layer for sample B is larger than in sample A. Furthermore, the interface between the NP-$Al_{0.01}Ga_{0.99}N$ layer and undoped GaN layer in each pair for sample B is much sharper than that in sample A.

The volume average theory (VAT) can be used for estimation of the effective index of the NP-(Al)GaN:

$$n_{por} = \left[(1-\varphi) n_{(Al)GaN}^2 + \varphi n_{air}^2 \right]^{1/2} \quad (5.1)$$

where $n_{por}, n_{(Al)GaN}, n_{air}$ and φ are the effective refractive index of the NP-(Al)GaN, the refractive index of intact GaN, the refractive index of air and porosity, respectively [23].

Substitute the porosity obtained from the software analysis to Equation 1, the effective index of NP-GaN for sample A was determined to be 1.76 and the effective refractive index of the NP-$Al_{0.01}Ga_{0.99}N$ for sample B is 1.52.

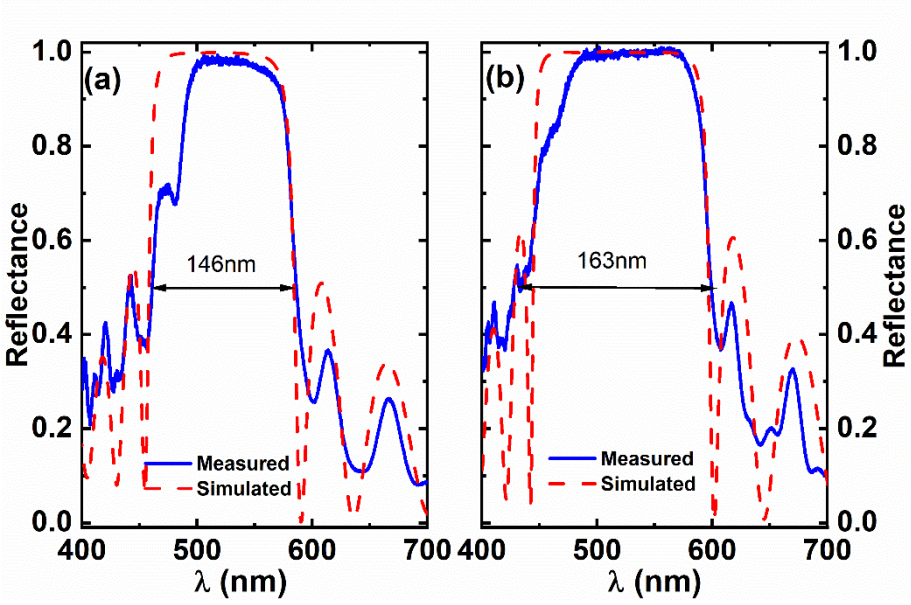

Figure 5.5: Reflectance spectra of (a) Sample A and (b) Sample B after EC etching, which have been converted to the NP DBR structures.

The reflectance spectra of sample A and sample B are shown in **Figure 5.5** as solid line, and both samples have been converted into NP DBR structures with high reflectivity. **Figure 5.5a** indicates the reflectivity of sample A is 98.5% at 529 nm as a central wavelength and the stopband width is 146 nm. The reflectivity of sample B in **Figure 5.5b** is 99.9% with a central wavelength at 525 nm and the stopband is increased to 163 nm. This result further confirms that an introduction of a tiny amount of aluminium in high doped layers growth could significantly improve the optical performance of the NP DBR after EC etching. The corresponding standard finite-difference time-domain (FDTD) simulated reflectance spectra are also presented in **Figure 5.5**. The effective refractive indices of the NP-GaN or the NP- $Al_{0.01}Ga_{0.99}N$ used are 1.76 or 1.52, respectively. These refractive indices were obtained from the cross-sectional SEM analysis. **Figure 5.5** shows that the simulated results (dash line) are in great agreement with the measured reflectance spectra (solid line). The difference between the simulation and real data might be due to the diffuse scattering from the non-uniformity of the pore size and the rough inner surface of the nanoporous layers. The deformation at the edge of the stopband is caused by the randomized phase of scattered light [25, 26].

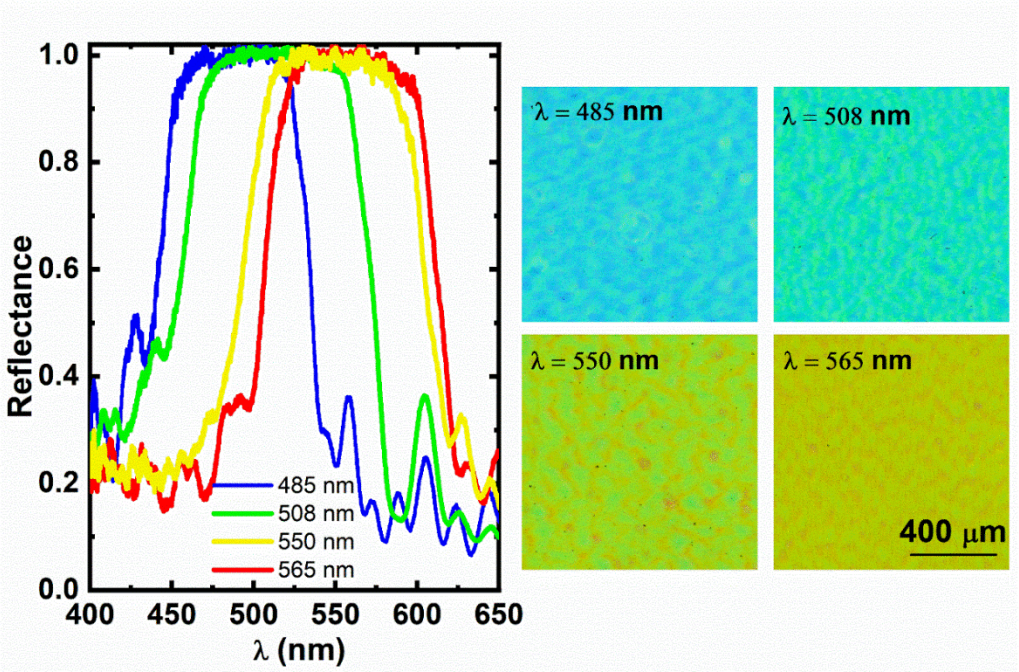

Figure 5.6: (a) Reflectance from four different kinds of $Al_{0.01}Ga_{0.99}N$/GaN NP DBR structures each with a central wavelength at 485 nm, 508 nm, 550 nm and 565 nm, respectively; (b) Optical images of these NP-$Al_{0.01}Ga_{0.99}N$/GaN DBR structures taken using a white light source (scale bar = 400 μm).

Based on the result of sample B, we systematically varied the parameters of the different layers in DBR growth to control the centre wavelength of the $Al_{0.01}Ga_{0.99}N$ /GaN NP DBR. First, we used the same growth condition but changed the growth time to adjust the thickness of the n-doped and the un-doped layers. Then, all samples were EC-etched with identical conditions. **Figure 5.6a** presents the reflectance spectra of a series of NP DBR mirrors with different central wavelengths at 485 nm, 508 nm 550 nm and 565 nm, respectively. As a result, these NP DBR mirrors show high reflectivity (>99%) and a wide stopband (>110nm). Due to only 1% aluminium being introduced during the growth of heavily doped layers, the lattice-mismatch is minimal, and these four structures can be easily prepared. **Figure 5.6b** shows the microscope images of these different $Al_{0.01}Ga_{0.99}N$/GaN NP DBR mirrors with a white lighting source. The colours

of these NP DBR structures are from blue through green/yellow to dark yellow which correspond to the~~ir~~ central wavelengths of the reflectance spectra.

5.4 Conclusion

In summary, it has been well-known that the rough surface and saturated conductivity are generally caused by the heavily silicon-doped GaN growth, which is required by high-performance NP DBR fabrication. Meanwhile, it is reported that the introduction of ≤ 5% aluminium for heavily silicon-doped AlGaN can maintain an atomically smooth surface and enhance conductivity. Considering the advantages of AlGaN with ≤ 5% aluminium, we propose replacing the heavily silicon-doped GaN layers in conventional GaN-based DBRs with heavily silicon-doped n^{++}-$Al_{0.01}Ga_{0.99}N$ layers by introducing 1% aluminium. In contrast to the traditional n^{++}-GaN/undoped GaN-based DBR, this n^{++}-$Al_{0.01}Ga_{0.99}N$/undoped GaN-based DBR has a V-pits free surface which is undoubtedly more beneficial to the growth of subsequent high-performance devices on its top. After the EC etching with identical conditions, these alternating layers can be converted into multiple pairs of NP-$Al_{0.01}Ga_{0.99}N$ layers/undoped GaN DBR and exhibit an enhancement in the refractive index of the NP-$Al_{0.01}Ga_{0.99}N$ layer and undoped GaN layer, leading to a NP DBR structure with an enhanced reflectivity and a wider stopband. In addition, since the Al concentration is extremely low, the lattice-mismatch between $Al_{0.01}Ga_{0.99}N$ and GaN can be safely ignored. The n^{++}-$Al_{0.01}Ga_{0.99}N$/undoped GaN multilayers also have a larger area of etched NP DBR after EC etching compared to the n^{++}-GaN/undoped GaN ones. Furthermore, a series of high-performance NP DBR structures have been fabricated based on this technique. These NP DBRs' colours are in the range from blue to dark yellow by controlling the thickness of multilayers during the MOCVD growth.

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Chapter 6: Fabrication and characterization of III-nitride membrane.

The large scale, crack-free III-nitride membrane lift-off has always been a great challenge for the development of future optical and electronic devices. These days, it is reported that the low-temperature (1000℃) AlN grown on an n-type silicon substrate via MOVPE can create a thin diffusion layer with high conductivity at the interface of AlN and silicon. Considering the previous research on electrochemical (EC) etching, this diffusion layer can be treated as a sacrificial layer in the etching and be polished. Therefore, we proposed to bond the AlN/GaN film grown epitaxially on an n-type silicon substrate to a new glass substrate first and then apply EC etching to realize the lift-off of the membrane structure with a large size. Due to that the n-type silicon substrate can also work as a current spreading layer, the voltage required in this EC etching is very low. As a result, the lift-off membrane is 2.625 cm^2 with a smooth and crack-free surface. This is the first time to realize peeling off such a large III-nitride membrane. Compared to other lift-off methods, our EC etching of GaN-on-silicon samples does not require expensive equipment or complex procedure but can guarantee a large smooth surface of the membrane structure. This method can be used to fabricate high-quality large-area GaN thin films at low cost, and also provides a new idea for the development of high-performance III-nitride devices on the membrane in the future.

6.1 Introduction

In recent years, semiconductor membrane structures have attracted much attention due to its promising prospects in hetero-integration and flexible electronics [1-4]. The hetero-integration mainly transfers the microstructures onto different host substrates

and makes bonding via techniques such as transfer-printing [1-3]. For flexible electronic devices, the purpose of research is to enable electronic products to have the ability to bend and stretch through membrane structures [4]. At present, there are a variety of materials have been prepared into membrane structures, including silicon [5-7], graphene [8-10], polymers [11-13], semiconductor materials [5, 14-17] and so on. Among them, the inorganic Si and III-V membranes are very attractive due to their compatibility with the growth process and excellent device performance. The preparation of membrane structures typically requires the polish of the sacrificial layer. For example, the silicon nanomembrane can be obtained by etching silicon on insulator (SOI) with HF acid [18], while the III-V semiconductor membranes are usually fabricated by selective etching [16-17].

III-nitrides are the most promising semiconductor materials with excellent features, including wide direct bandgap, high thermal stability, excellent electron velocity and excellent chemical and physical stability [19, 20]. Therefore, III-nitrides have been widely used in optoelectronic devices, high-frequency, and high-power devices. However, the research on III-nitride membranes is still under exploration. The extremely strong chemical inertness of III nitrides is an important factor limiting the development. Therefore, it is a great challenge to apply selective etching in the GaN membrane preparation.

Currently, various methods have been reported to achieve the aim of lifting-off III-nitrides membranes, including laser lift-off (LLO) [21, 22], chemical etching [23], electrochemical etching [16, 24], and mechanical lift-off on a suitable buffer layer [25, 26]. Wong *et al.* introduced LLO method to separate a GaN-based laser epilayer from a sapphire substrate and then transfer this epilayer to a new substrate [27]. They use a laser with high power to pass through the sapphire substrate and absorbed by the interfacial GaN. The photon absorption at the interface makes the bulk GaN decompose into metallic Ga and gaseous N_2 leading to the separation of GaN nanomembrane from the sapphire substrate. This nanomembrane can be easily transferred to a new substrate.

Other reports also demonstrated the laser lift-off technique to fabricate GaN-based LEDs and LDs on a stress-free GaN substrate [28]. However, the LLO technique requires expensive equipment, and the high energy laser will cause damage to the GaN layer. In addition, the uneven and whisker-like micro-pole formed on the lift-off membrane is another disadvantage that limits the development of the LLO technique.

As introduced in chapter 4, it is possible to completely polish the heavily doped GaN layer by conductivity selective electrochemical etching (EC). Chang *et al.* reported a strain balanced AlGaN/GaN/AlGaN nanomembrane HEMT [16]. They epitaxially grew a membrane structure on a heavily n-doped GaN layer. This n^{++}-GaN layer is used as a sacrificial layer which can be etched by selective EC etching. After releasing the nanomembrane, it is transferred onto a new host substrate. However, the membrane is easily damaged during the EC etching and transfer processes, leading to that the membrane size cannot be very large. Moreover, a high voltage is required during the EC etching to make sure that the sacrificial layer is completely polished. It will damage the electronic devices on the membrane.

Recently, nanoporous GaN has been presented to work as a special structure to slice and separate GaN device layers. Yerino et al. reported their achievement in the shape transformation of nanoporous GaN by annealing [29]. In their work, they grew a sample consisting of 2 μm thick n-GaN ($n=5*10^{18}$ cm^{-3}) on 2 μm undoped GaN by MOCVD. The sample was then etched with 0.3M oxalic acid under two different voltages to form the nanoporous structure. The layer on top has a 25% porosity, and 55% porosity at the bottom. Then, the sample was annealed at a high temperature (1000℃) with both N_2/NH_3 and H_2/NH_3 ambient. After 60 min annealing, the shape of the NP is significantly transformed due to the surface and gas phase diffusion. The layer with low porosity changed to a bulk structure, and the layer with high porosity changed to columnar voids with vertical sidewalls. This GaN-on-air structure is used for the following nanomembrane lift-off. The membrane can be peeled off by applying mechanical force. The difficulty in implementing this method is the decomposition of

GaN in annealing. This method requires precise control of temperature, pressure and gas flow during the annealing which undoubtedly reduces the repeatability.

It was reported that a diffusion layer is created at the AlN/Si interface after low-temperature AlN deposition on n-type silicon substrate by MOVPE [30, 31]. This layer has higher conductivity which can be used as the sacrificial layer for EC etching and realize the lift-off of III-nitride membranes. In this chapter, we are proposing to apply EC etching to GaN-on-silicon samples to realize lift-off of a large area of AlN/GaN membrane.

6.2 Methods

6.2.1 GaN on silicon growth

The samples used in this work were grown on n-type (111) silicon substrate with a standard GaN-on-silicon growth method by metal-organic vapour phase epitaxy (MOVPE). First, a TMAl pre-flow process was carried out at low pressure (86mbar) with low temperature (1145℃) after thermal substrate cleaning in a hydrogen ambient. Then, a 255 nm low temperature (1145℃) AlN buffer layer was grown underneath a high temperature (1300℃) AlN buffer layer. A 700nm AlGaN layer was grown subsequently under 100mbar with 1290℃. Finally, a 700 nm undoped GaN was grown on top of the sample. Hall measurement was taken to the silicon substrate. The conductivity is 0.864 $(W.cm)^{-1}$ and is n-type doped with $3.65*10^{15}cm^{-3}$. This n-type silicon substrate is necessary to form a diffusion layer of Si and Al at the interface between the silicon substrate and low-temperature AlN buffer layer. In addition, it can also be used as the current spreading layer in the EC etching to allow a smooth lift-off.

6.2.2 wafer bonding

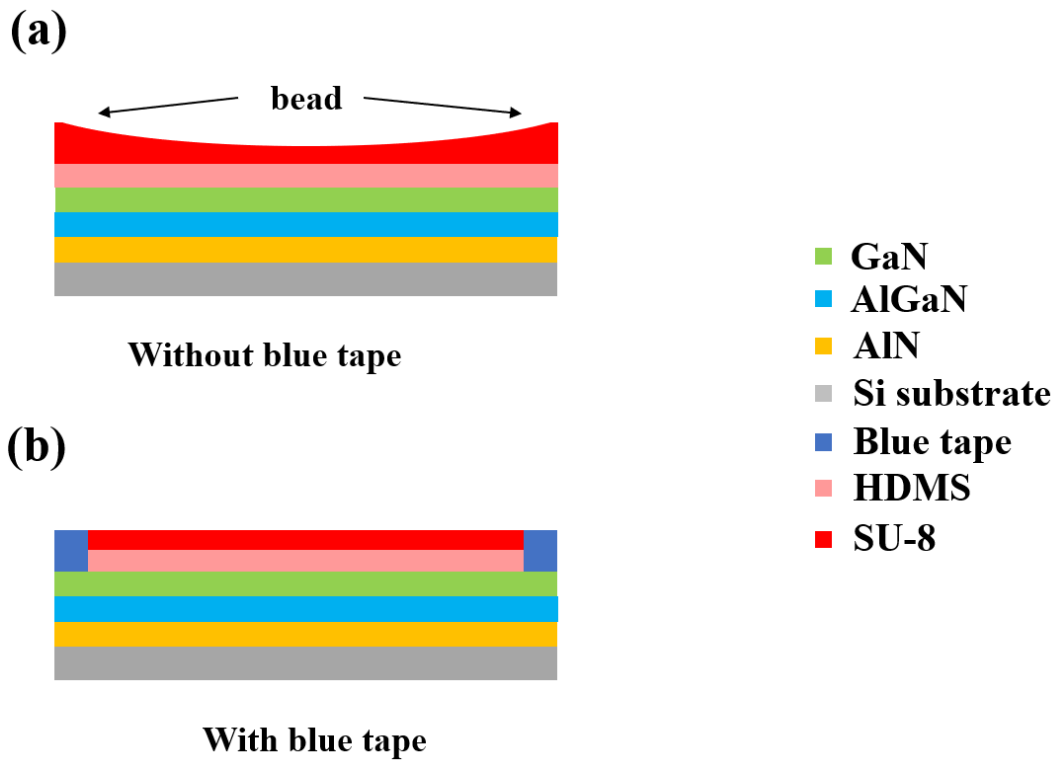

Figure 6.1: Schematic of photoresist spin (a) without and (b) with blue tap protection at the edge of the sample.

To transfer the polished membrane onto a new substrate, the sample needs to be first spin-coated with a kind of thick photoresist and bonded on the substrate. The classical spinning method cannot be applied directly in this work. Since the SU-8 photoresist used in this work is a very thick and sticky photoresist, it will cause a very strong spin-coat edge bead effect after spinning. As **Figure 6.1a** shows, a height difference between the centre of the sample and the edge was created, leading to many bubbles while bonding the SU-8 coated face to a new glass substrate. These bubbles are very deadly to the electrochemical lift-off because these areas have no support and cause cracks in the membrane. A simple solution is to use blue tapes to cover the edge before spinning and let it sit overnight after the spinning process. Then, the surface is sprayed with edge bead remover to prevent the surface from drying out. Finally, the blue tape is removed,

and the SU-8 spin-coat will have a flat surface like **Figure 6.1b**. In addition, the blue tape covered area can also be an open window for the etchant to contact with the sample.

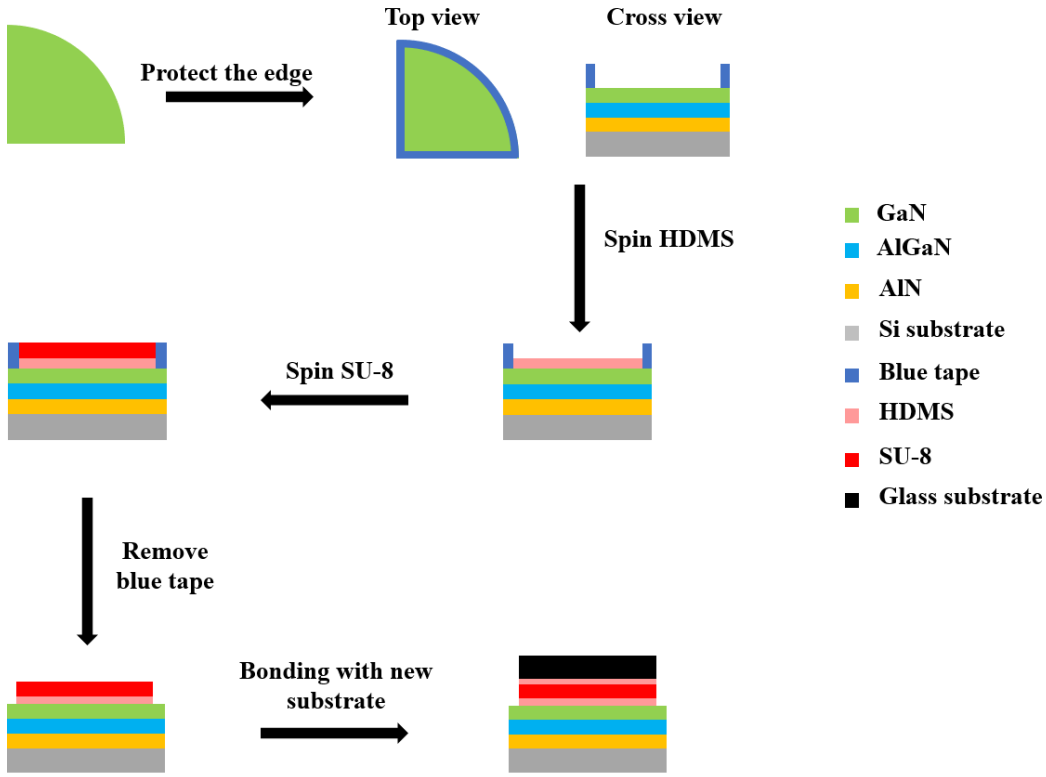

Figure 6.2: Schematic of substrate bonding process.

Figure 6.2 is a schematic of the new substrate bonding process. The wafer after epitaxial growth was cleaved into four equal pieces by a diamond scribing pen at the centre. Each of the cleaved samples was a quarter wafer with a 1-inch radius. The new glass substrate was carefully cleaved from a cover glass according to the shape of the GaN on silicon sample which is a trapezoid with a lower base of 2cm, upper base of 1.5 cm and height of 1.5cm (**Figure 6.6**). The next step is to clean the samples and new substrate in an ultrasonic bath of n-Butyl, acetone, isopropanol and finally rinse with DI water. Each step takes 2 minutes to remove the organic residual and dust completely. Then, blow the samples and new substrate with clean nitrogen to remove the water stains and bake at a hot plat for 1min with 100℃ to de-moisturization. Next, use blue tape to cover the edge of GaN-on-silicon sample with a width of 3 mm. Finally, the samples were spin-coated with photoresist SU-8 2010. The required thickness of the

SU-8 is 20 μm, which is achieved by the following steps: Firstly, spin a layer of hexamethyldisilazane (HMDS) on the sample surface with 4000 rpm for 30s. This layer can work as an adhesion promoter preventing photoresist from delamination. Then, distributed SU-8 across the whole surface by spinning at 500 rpm for 10s with an acceleration ramp of 100rpm/s, followed by a spinning cycle at 4000r pm for 30s with an acceleration ramp of 300 rpm. The slow acceleration ramp is helpful for the photoresist's spreading due to that SU-8 is very sticky. An edge bead removing process is required by leaving the sample overnight. The new glass substrate was spin-coated with HDMS at 4000 rpm for 30s. Then, remove the blue tape protections at the edge and bond to the new glass substrate from one side to the other. Finally, press the new substrate carefully and remove any bubbles inside the SU-8.

A soft bake process is required before an UV light exposure. The samples were first baked at 65℃ for 3min, then heated to 95℃ in 5mins and kept for 5 mins. It is required to apply pressure on the surface throughout the soft baking process to ensure a tight bonding between the sample and glass substrate. The exposure was performed on a *Karl Suss MJB3 UV400 Mask Aligner* with 120s. A long exposure time is required to ensure the long molecular chains in SU-8 are fully cross-linked. The post-exposure bake was 95℃ for 5mins, heated to 150℃ in 10mins and kept 30mins for hard bake. It is essential to increase the temperature with a very low warming up speed in the baking process, because the drastic change in temperature will lead to the breakage of the SU-8 bonding.

6.2.3 EC etching

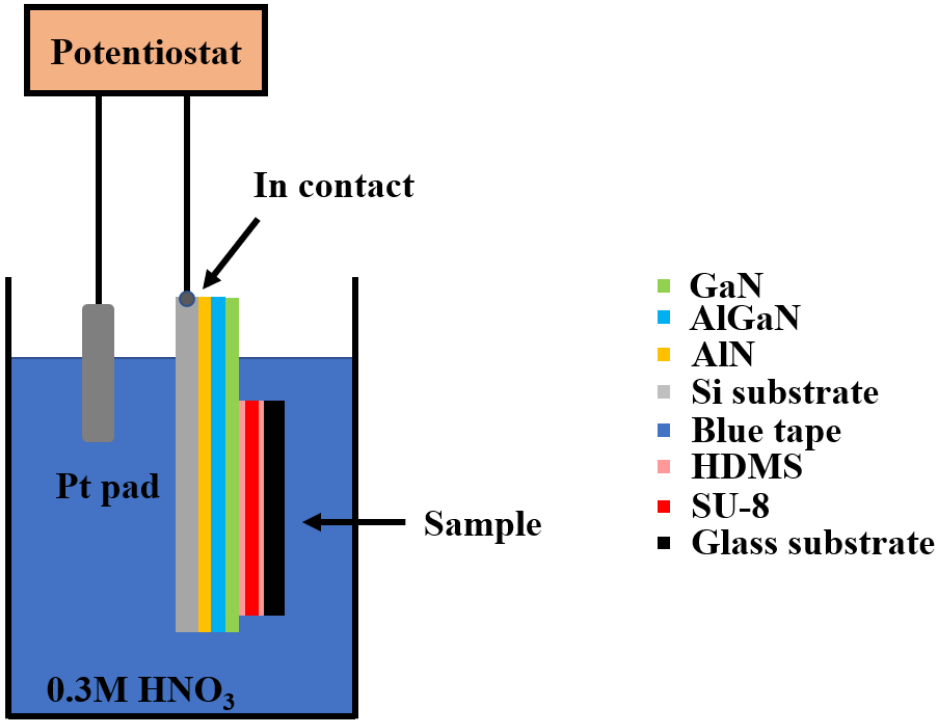

Figure 6.3: Schematic of EC etching for membrane lift-off.

Figure 6.3 is the schematic of EC etching of lift-off AlN/GaN membrane. A Metrohm Autolab PGSTAT204 SYSTEM was employed as a potentiostat to record the etching data. Since the silicon substrate is n-type doped, it can work as a current spreading layer and enhance the EC etching. An indium contact was physically pressed at the edge of the backside of silicon substrate and connected to the anode. Then the sample anode and Pt counter-electrode were immersed in 0.3M nitric acid solution. All samples were etched for 30min under different bias voltages. In order to lift off the membrane completely, the glass substrate covered area was required to be fully immersed in the etchant. Meanwhile, the metal electrode (connected to sample) cannot be in touch with the etchant to prevent water electrolysis rather than EC etching (shown in **Figure 6.3**). Therefore, the membrane will automatically peel off with the new glass substrate after etching. This membrane on glass substrate will then be clean with DI water and blew dry gently with nitrogen gas.

6.3 EC etching optimize

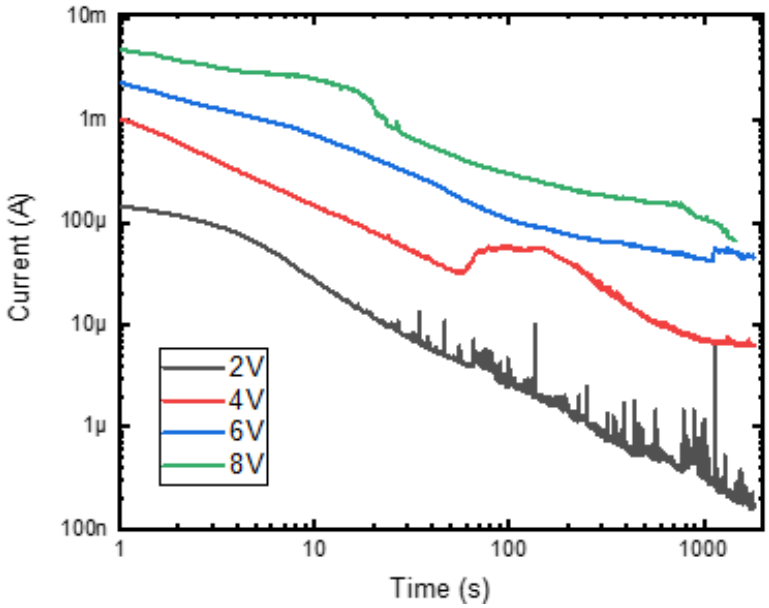

Figure 6.4: The injection current of samples etched with different bias voltage

In order to investigate the etching conditions of GaN membrane lift-off via EC etching, the samples were etched with 2V, 4V, 6V and 8V, respectively. The injection currents of samples etched with different bias voltages are shown in **Figure 6.4**. When the sample was etched with 2V, no change was observed after 30 minutes of etching. So, the injection current remains very low and even lower than the background noise. However, after being etched with 4V, the current shows a significant increase at 16s. This increase means the EC etching start. It will be discussed in detail with optical-microscope results later. In fact, the GaN-based membrane can be lifted-off from the silicon substrate only when the etching voltage is higher than 6V. It is also worth noticing that the etching time for 8V is 1440s when the membrane with the new glass substrate is lifted-off and detached from the silicon substrate.

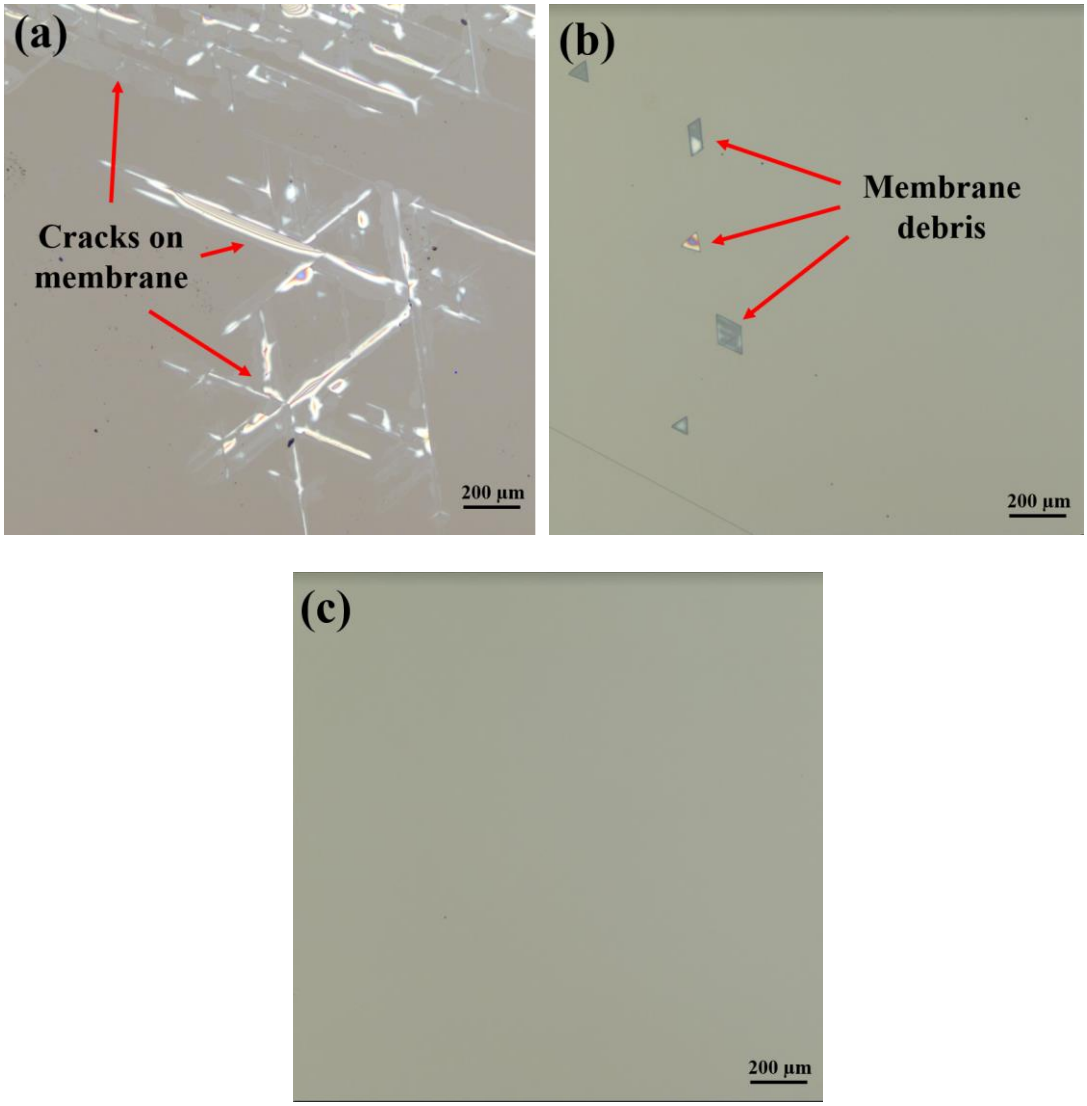

Figure 6.5: optical-microscope images for sample etched with (a) 4V, (b) 6V, and (c) 8V.

The optical-microscope images of samples after EC etching with 4V, 6V and 8V are shown in **Figure 6.5**, respectively. Since nothing changes on the surface of sample after 2V etching, the etching result is not shown. The membrane was not lifted-off with 4V bias etching (**Figure 6.5a**). Although some etching traces can be observed at the edge of the sample (not covered by SU-8 or glass substrate), the AlN/GaN membrane structure remains intact. The EC etching traces were distributed along cracks caused by the inevitable cracks at the edge of the sample during the epitaxial growth. When the etching breaks the membrane, the etchant can react with more sacrificial layer and the

current suddenly increases. However, 4V is too low for the membrane lift-off. For 6V bias voltage etching, the membrane can be lifted-off after 30mins etching. Unfortunately, the EC etching cannot polish the sacrificial layer completely. **Figure 6.5b** shows some III-nitride membrane debris remains on the silicon substrate after EC etching, which indicates that the membrane was already broken. In **Figure 6.5c**, the surface of silicon substrate is very smooth and has no residual AlN/GaN structure. Thanks to the higher bias voltage in EC etching, the membrane can be easily lifted off completely. Therefore, the 8V bias voltage in 0.3M HNO_3 solution with an etching time of 30mins is the best condition for the AlN/GaN membrane lift-off.

6.4 Membrane Characterization

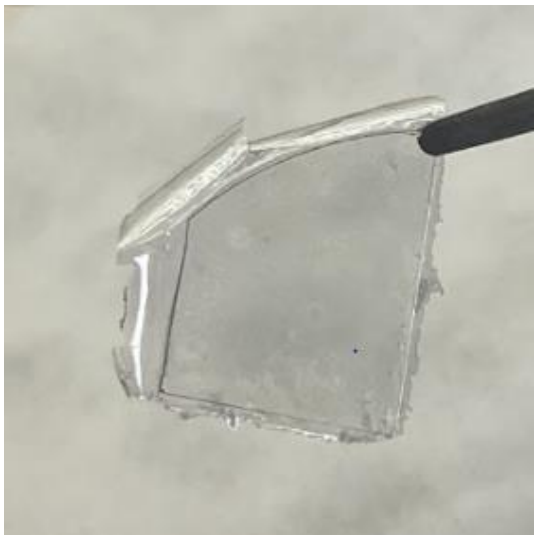

Figure 6.6: photoshoot of membrane on glass substrate.

Figure 6.6 shows the photo of the AlN/GaN membrane on the host glass substrate after etching. The new glass substrate is slightly smaller than the original sample, so the total lift-off shape is a trapezoid with a bottom base of 2 cm, a top base of 1.5 cm and a height of 1.5 cm. Therefore, the total lift-off area is 2.625 cm^2. It is worth highlighting that this is the largest lift-off GaN membrane without cracking reported so far [16, 32]. Since the surface of the sample was spun with SU-8 photoresist, the unbonded membrane curled by itself. It is caused by the release of the stress in the AlN/GaN

produced during the epitaxial growth. Actually, the lift-off membrane will break easily if without the support of a new glass substrate. The surface tension force of liquid is too strong to tear the membrane while taking it out of the etchant. Therefore, it is necessary to bond the sample with the glass substrate before EC etching. In this work, the AlN/GaN membrane structure, SU-8 photoresist and glass substrate are all transparent, which is a huge advantage for the development of future optoelectronic structures. It is also worth highlighting that the SU-8 photoresist and glass substrate can be replaced with any other bonding material or substrate, such as flexible substrate, conductive substrates, etc.

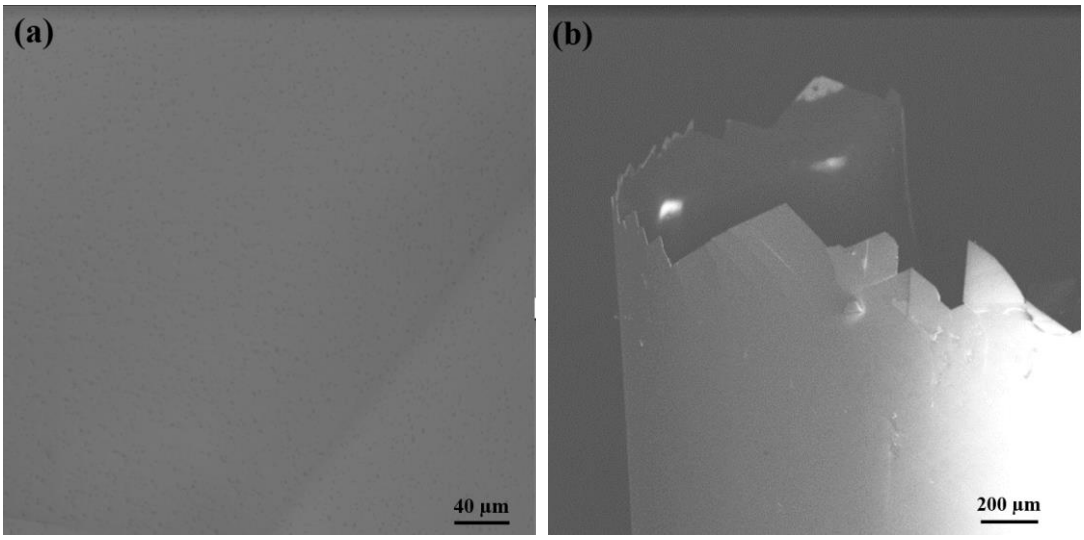

Figure 6.7: (a) Plan view SEM result of the centre of the lift off membrane. (b) SEM result of the edge of lift off membrane.

Figure 6.7a is the plan view SEM image of the centre of the lift-off membrane. Since the surface of the sample after epitaxial growth was bonded to the new glass substrate, the entire membrane structure was upside down. Thus, this is the N-polar face of the AlN layer. Meanwhile, some small pits can be observed on the surface. The EC etching is an isotropic etching method, which generated these pits at the interface between the low-temperature AlN buffer layer and the silicon substrate. Very importantly, the whole membrane surface was carefully inspected with SEM and no obvious cracks were found in such a large lift-off AlN/GaN membrane. Unlike the typical lift-off methods (LLO

or EC polish), the small lift-off membrane size always restricts the development of membrane application. The fragile membrane will easily break with the stress releasing or teared by the liquid surface tension when removed from the liquid. Thanks to our EC etching of GaN on silicon method which proposes bonding the membrane structure with the new host substrate before lift-off, it effectively avoids cracks caused by stress releasing and provide certain support for the membrane when taking out membrane from the acid solution. **Figure 6.7b** shows the SEM image of the edge of the AlN/GaN membrane. Without the support of the glass substrate, the AlN/GaN membrane bends towards the photoresist direction. Even so, the membrane did not crack at the curved arc, except that the edge of the sample is jagged and fractured.

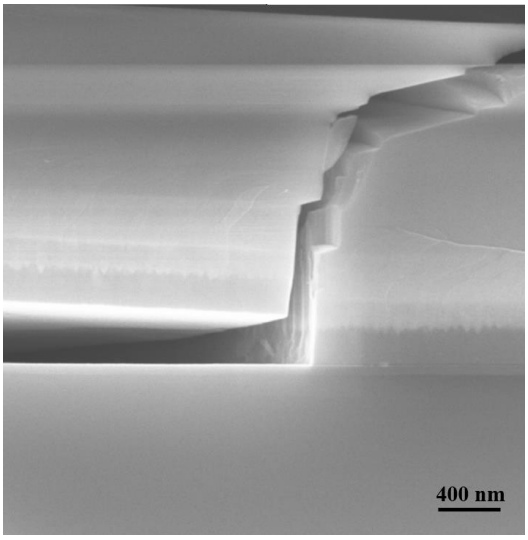

Figure 6.8: Cross-sectional view SEM image of the membrane structure separated with the silicon substrate.

The morphology of each layer after EC etching have been studied from the cross-sectional SEM observation. The cross-view image of the membrane structure and separated with the silicon substrate is shown in **Figure 6.8**. This image clearly shows the epitaxial growth structure layer by layer. From the bottom to top are the silicon substrate, the low-temperature AlN buffer layer, high-temperature AlN buffer layer, AlGaN layer and GaN layer, respectively. The left part is the lift-off membrane, and the right part is not etched. After 30 mins EC etching with 8V bias voltage, the epitaxial

growth structure was separated from the substrate at the interface between the low-temperature AlN buffer layer and the silicon substrate. It is believed that diffusion of the acceptor dopant (Al) caused by the process conditions (temperatures/pressure/gasses flow rate) has formed a metallurgical junction inside the n-type silicon substrate. As Chang *et al.* claimed recently, this diffusion of such species can be limited to a few tens of nanometres and significantly change the conductivity into the substrate [30]. Meanwhile, Micka *et al.* also reported that the low-temperature (~1000°C) AlN epitaxial growth on n-type silicon substrate by MOCVD would form a diffusion layer with an extremely high acceptor concentration (10^{18}cm^{-3}) [31]. Thus, it can be treated as the sacrificial layer in traditional EC etching and be polished to realise the lift-off of membrane structures. Like the EC etching in the previous chapter, the reaction function is shown as:

$$2AlN + 6h^{+} \rightarrow 2Al^{3+} + N_2 \uparrow \tag{6.1}$$

The Al^{3+} ion in the reaction is movable in the nitric acid. In addition, the n-type silicon substrate is a good current spreading layer that helps the EC etching maintain continuously. By using software (ImageJ) to analyse the thickness of each layer, the low-temperature AlN buffer layer after EC is 215 nm, whereas the epitaxial growth AlN thickness is 255 nm. So, a 40 nm high hole concentrated diffusion layer was formed in growth. Since the thickness of this layer is as low as the porous after EC etching, the whole diffusion layer was etched completely. Therefore, the very sharp interfaces between the membrane after lift-off and silicon substrate further indicates that this diffusion layer has a very high doping level.

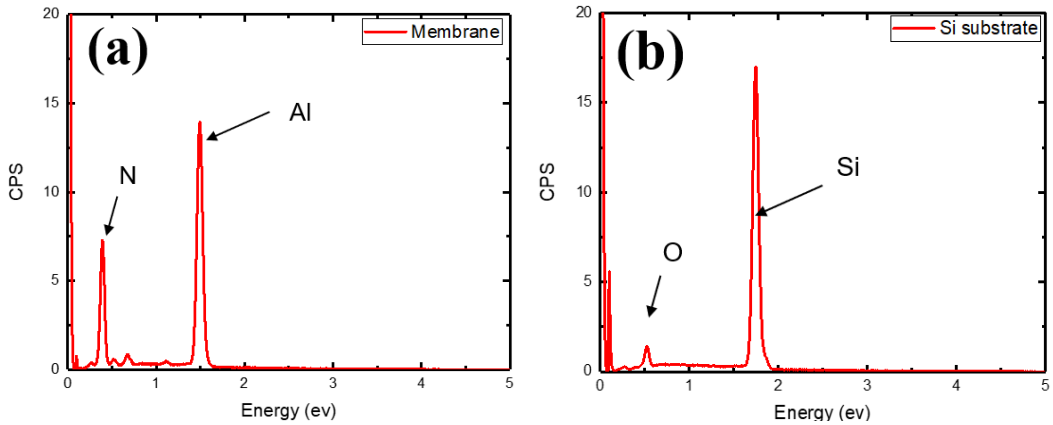

Figure 6.9: EDX mapping results for (a) lift-off membrane and (b) Si substrate after EC etching.

In order to further understand the EC etching for AlN/GaN membrane on silicon, the energy dispersive X-ray (EDX) mapping measurements have been carried out, as shown in **Figure 6.9a** and **Figure 6.9b** for membrane and silicon substrate after etching, respectively. In **Figure 6.9a**, the nitrogen peak is at 0.392 keV and the aluminium peak is at 1.486keV, which are the only two detected element. It indicates that the top layer is AlN. In **Figure 9b**, the silicon substrate after EC etching shows a high Si energy peak at 1.739 keV with a low oxygen energy peak at 0.525 keV. This double peak EDX result is ascribed that the silicon is easily oxidized and forms a thin oxide layer after lift-off. These EDX mapping measurement results also demonstrate that the EC etching occurred at the silicon substrate and AlN layer interface.

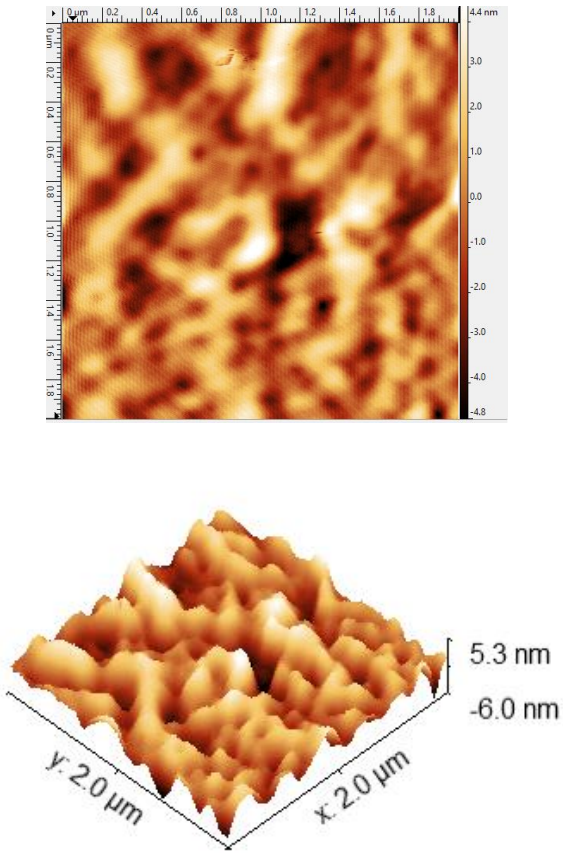

Figure 6.10: Two- and three-dimensional AFM image taken from centre of lift-off membrane.

In order to evaluate the possible etching damage on the surface of the lift-off membrane, atomic force microscopy (AFM) images were taken from the centre of the GaN membrane on the glass host substrate, which are shown in **Figure 6.10** as two-and three-dimensional AFM images. In these images, the brightest areas are the highest point of the membrane surface, and the dark regions indicate the valleys. No significant damage to the surface morphology was observed. The exposed N-polar low-temperature AlN buffer layer had a root-mean-square (RMS) roughness of 1.586 nm over a 2µm × 2 µm area. Since the EC etching is an isotropic etching method, some small hillocks were formed during the etching process. Therefore, the AFM image depicts a slightly rougher surface than the recent works exploring N-polar AlN for optoelectronics applications [33, 34].

6.5 Conclusion

High-quality III-nitride membranes have good development prospects. However, it is restricted by small size, high cost, and complex preparation process. Meanwhile, it is reported that a very thin diffusion layer can be formed beneath the AlN/Si interface when applying MOVPE to deposit low-temperature AlN film in a close coupled showerhead system. This diffusion layer has strong conductivity which can be used as the sacrificial layer in EC etching. Our group has proposed a simple EC etching method of GaN on silicon sample to realize the lift-off of the III-nitride membrane. This method applies SU-8 photoresist to bond the high-quality epitaxially grown GaN-on-silicon sample to a new glass substrate and peels off the membrane structure by low voltage electrochemical etching. It has been demonstrated that a large area (>2.5cm^2) and crack-free AlN/GaN membrane with a smooth surface is achieved using this method. These exciting results constitute a great progress in developing high-quality membrane devices at a low cost. In addition, the etching mechanism of the membrane lift-off is also discussed which further proves that a high conductivity diffusion layer can be formed at the interface of low-temperature AlN buffer layer and the n-type silicon substrate. Therefore, this method offers an affordable and simple way to realize lift-off III-nitride devices on membrane structures.

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Chapter 7: Conclusion and future work

In this thesis, a detailed investigation has been carried out on the mechanism of electrochemical (EC) etching and the application to the fabrication of nanoporous (NP) GaN based DBR structures. Two methods are proposed to enhance optical performance of the NP DBRs: one is the lateral etching method, and the other one is introducing a small amount of Al flow during epitaxial growth of heavily doped n-GaN. Detailed characterizations of structural and optical properties have validated that the two methods are feasible and beneficial to improving the reflectivity and stopband width. Furthermore, EC etching is also applied to lifting off the III-nitride membranes which leads to successful achieving a crack-free membrane with large size.

7.1 Summary of the results

7.1.1 Electro-chemical etching for nanoporous DBR fabrication

In this chapter, we applied EC etching to fabricate NP-GaN based DBR structures with high reflectivity. By changing the doping level of heavily doped n-GaN layer or the bias voltage of EC etching, the EC etching is demonstrated to be sensitive about conductivity. A higher bias voltage and a higher doping level led to a large porosity in the n^{++}-GaN layer or even polish of the n^{++}-GaN layer after EC etching. A processing phase diagram for EC etching is summarized for the guidance of the follow-up experiments, as shown in **Figure 4.3**. Furthermore, a lateral etching method is proposed to replace the normal etching to improve the optical performance of the NP-GaN based DBR structure. The SiO_2 and thick photoresist were used as protective layers during the EC etching. Then, the sample was dry-etched with trenches to fully expose the

highly doped n^{++}-GaN layer to achieve 2D lateral etching of each n^{++}-GaN layer. Through the measurements on the electric currents during the EC-etching and SEM observations, the mechanisms of both the normal etching and the lateral etching are explored. As a result, a more uniform nanoporous morphology is obtained after lateral etching, simultaneously leading to a higher porosity. In addition, the protective SiO_2 and thick photoresist on the top surface can also prevent the top undoped GaN layer from the damage caused during the EC etching. The direct reflectivity of the lateral etched DBR sample is 98.5% with a stopband width of 124 nm, which is better than the normal etched sample with a reflectivity of 97.3% and a stopband width of 104nm.

7.1.2 Nearly Lattice-matched GaN Distributed Bragg Reflectors with Enhanced Performance

Heavily silicon-doped GaN is necessary for the fabrication of high-performance nanoporous DBRs. However, it also results in a rough surface and saturated conductivity. Therefore, 1% aluminium is introduced in the epitaxial growth of the heavily doped GaN layer. Consequently, a heavily silicon doped n^{++}-$Al_{0.01}Ga_{0.99}N$ is formed to replace the heavily silicon doped n^{++}-GaN layer in each period of the traditional GaN-based DBR. This n^{++}-$Al_{0.01}Ga_{0.99}N$/undoped GaN-based DBR has a V-pit free surface, which is undoubtedly beneficial to the growth of subsequent high-performance devices on the top. After the EC etching under the same conditions, the n^{++}-$Al_{0.01}Ga_{0.99}N$/undoped GaN-based DBR is converted into an NP-DBR with a higher refractive index ratio. Compared with the NP-GaN/undoped GaN DBR (R=98.5%, stopband width = 146nm), the NP-$Al_{0.01}Ga_{0.99}N$/undoped GaN-based DBR has a higher reflectivity and a wider stopband (R=99.9%, stopband width = 163nm). At the same time, since only a very low concentration of Al flow is introduced during the growth, the lattice mismatch between the n^{++}-$Al_{0.01}Ga_{0.99}N$ layer and the undoped GaN layer can be safely ignored. After lateral EC etching, the n^{++}-$Al_{0.01}Ga_{0.99}N$/undoped GaN multilayers have larger etched DBR regions than the n^{++}-GaN/undoped GaN sample.

Finally, a series of high-performance DBR structures have been-fabricated based on the method. By controlling the multilayer thickness during MOCVD growth, these NP DBR structures demonstrate reflectance wavelengths with a long range from blue to deep yellow.

7.1.3 III-nitride membrane lift-off by electrochemical etching from GaN on silicon sample.

The GaN-on-silicon samples used for the present study were grown on n-type silicon substrates by metal organic chemical vapour deposition (MOCVD). A low temperature (1145℃) AlN was first deposited on an n-type silicon substrate, followed by a high temperature (1295℃) AlN layer. Then an AlGaN buffer layer was grown before the final undoped GaN layer. Next, the sample after epitaxial growth was bonded to a new glass host substrate with SU-8 and then went through the EC etching. A thin diffusion layer with high conductivity will be created at the interface of low-temperature AlN and the n-type silicon substrate. Consequently, this depletion layer can be polished by EC etching, and the GaN membrane can be lifted-off from the n-type silicon. The III-nitride membrane lifted off automatically when the EC etching is performed with 8V in 0.3M HNO_3 for 30mins. The lift-off membrane is 2.625cm^2, which has a smooth and crack-free surface. It is the first-time to report achieving a III-nitride membrane with such a large size.

7.2 Future work

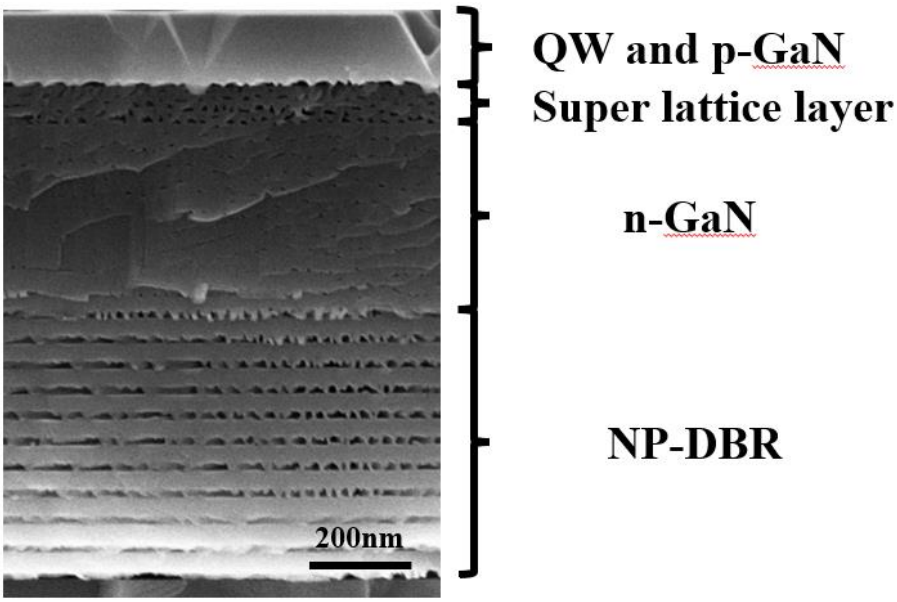

Figure 7.1: Cross-sectional SEM of a LED structure on DBR after EC etching.

So far, NP-DBR structures with high reflectivity and wide stopband width have been already fabricated by electrochemical etching. In addition, the DBRs with different reflection wavelengths can be obtained by changing the layer thickness of each period. It means that the NP-GaN based DBR can be employed in fabrication of optical-electronic devices. In recent years, many groups have demonstrated the application of high reflectivity NP-GaN DBR mirror, such as optically pumped VCSELs [1, 2], resonant-cavity LEDs (RC-LEDs) [3, 4] and enhanced micro-LED [5], etc. However, a great challenge of incorporating NP-DBR into practical devices is to avoid the unwanted etching of other doped regions in the device. **Figure 7.1** shows a cross-sectional SEM of a LED on DBR structure after EC etching. It is seen that the low doped n-GaN layer and the supper lattice layer between the DBR structure and quantum wells were etched and transformed to nanoporous structures. Even though the porous size is small, it affects the optical performance of the DBR as well as the electrical properties. Therefore, further optimization of etching methods and conditions to prevent the unwanted etching area is required for the development of NP-GaN based

DBRs. Future work should be focused on the relationship between low-doped n-GaN in LED structure and the heavily doped n-GaN in DBR structure. Investigation of the etching in the same etching condition and protecting the top LED structure are very important. Meanwhile, new masks in photolithography is also a possible method to control the heavily doped n-GaN. A dot matrix opening is one of the structures to enhance the EC etching for LED devices.

It has been verified that the surface morphology, reflectivity, and stopband width of NP-DBR can be effectively improved by introducing a small amount of Al during the epitaxial growth of heavily doped GaN layer and forming n^{++}-$Al_{0.01}Ga_{0.99}N$ instead. However, the effect of Al composition during the DBR growth on the performance of NP-DBR is not clear. A series of DBR samples with different Al contents in heavily silicon doped layers can be designed and etched by EC etching to further investigate the influence of Al composition on the NP-DBR optical performance.

Currently, our group has already lifted-off membrane structures with micro-LEDs successfully over the large size from GaN-on-silicon samples by EC etching methods. However, as the top surface of the sample was bonded to the new substrate, the entire micro-LED structure is turned upside down. It undoubtedly poses a new challenge to the device fabrication of micro-LEDs. On the other hand, the new substrate should not be limited to glass. It is expected that more substrates with flexible or conductive properties can be introduced to bring more applications to the membranes. Polymethylmethacrylate (PMMA) and Polydimethylsiloxane (PDMS) are two kinds of polymer organic compounds. Both materials have the characteristics of high transparency, low price, and ease of processing. Furthermore, they are now popular in the application of flexible devices substrate. The liquid PMMA and PDMS can easily spin on the surface of the sample and form a supporting layer. After baking, they can be plastic easily. There have been a number of reports about applying PMMA or PDMS as a substrate to fabricate flexible semiconductor devices.

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