The University Of Sheffield.

Fabrication and characterization of GaN-based lateral and vertical transistors for switching applications

by:

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A dissertation submitted in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy
In

Electronic and Electrical Engineering
The University of Sheffield

Supervisor: Dr. Kean Boon Lee
Oct 2022

In memory of Professor Peter A. Houston.

Abstract

GaN-based lateral and vertical structures are investigated to exploit the full potential of GaN-based electronics. Four distinctive structures – vertical V-groove semi-polar (11-22) GaN metal oxide semiconductor field effect transistor (VMOSFET), vertical semi-polar (11-22) GaN Fin field effect transistors (FinFETs), lateral p-channel Ga-polar (0001) GaN metal insulator field effect transistors (MISFETs) and lateral n-channel Ga-polar (0001) GaN MISFETs are studied. The design principle for these structures is presented, and real devices are fabricated and characterized.

In the semi-polar (11-22) VMOSFETs, the crystallographic wet etching approach was utilized to achieve the trench sidewall opening in a vertical architecture. The VMOSFETs exhibits a threshold voltage (V_{th}) of 9.49 V, a current ON/OFF ratio of 10^7, an ON-state resistance (R_{on}) of 8.0 mΩ.cm^2, an output current of 516 A/cm^2, and a breakdown voltage (V_{BD}) of 150 V. For the first time, the dry plasma etching free GaN vertical inversion channel is achieved. The inversion channel mobility is 21.3 cm^2/Vs.

Subsequently, the crystallographic wet etching approach was applied to obtain the sub-micro nano patterns for the semi-polar FinFETs fabrication. The devices operation principle and device parameters are evaluated by using technology computer aided design simulation. Several process modules are investigated and established. A smooth and uniform Fin sidewall is obtained, and the 2nd stage electron beam lithography is achieved. The fabrication process is integrated and FinFETs device is fabricated and characterized. A high leakage current is observed, and the possible leakage current paths is discussed.

In the lateral p-channel Ga-polar (0001) GaN transistor with metal-insulator-semiconductor structures, for the first time, the record low subthreshold value of 60 mV/decade is measured with very low metal-insulator-semiconductor interface trap density of ~ 10^{10} cm^{-2}eV^{-1}. An enhancement mode threshold voltage of -1.53, a high transconductance (g_m) of 1.0 mS/mm, a high current ON/OFF ratio of 10^7 and a small V_{th} hysteresis of < 120 mV are concurrently achieved. In the lateral n-channel Ga-polar (0001) GaN MISFETs, a self-terminated dry etching approach is utilized to selectively access the AlGaN/GaN heterostructures, which allow the fabrication of n-channel device. A high g_m of 100 mS/mm and high drain current of 800 mA/mm are achieved indicating the mitigated degradation of 2DEG channel.

Acknowledgement

I'd like to start by expressing my gratitude to Dr. Kean Boon Lee, my research supervisor, for his guidance, patience, and support over the duration of this project, whose teachings went much beyond in a PhD programme, and whose influence will last a lifetime.

I'd want to express my gratitude to my previous group members, Dr. Sheng Jiang, Dr. Joseph Pinchebeck, Prof. Peter A. Houston and Dr. Srikanth Reddy Devireddy for the illuminating conversations we've had and the invaluable insight and guidance they've provided me with regards to GaN device fabrication, characterization, and beyond. I would like to thank my current group member, Upeksha M De Silva for your encouragement.

The love and support of my family is invaluable to me, and I'd want to express my gratitude to them.

Publications

Journal Paper:

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Y. Yin and K. B. Lee, “P-channel and N-channel Metal Insulator Semiconductor Field Effect Transistor on p-GaN/i-GaN/i-AlGaN/i-GaN Hetero-structure,” in 2022 International Workshop on Nitride Semiconductors, Berlin, Germany, Oct 2022. (Oral presentation)

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Award:

2022 UKNC Phil Dawson travel award

Table of Contents

1.Introduction

Since the vast majority of the energy used today still comes from nonrenewable sources, ensuring a steady supply of energy for people everywhere is a pressing concern for all societies. Improving power converter efficiency is the primary means through which power consumption can be decreased in the field of power electronics. Although power electronics are now ubiquitous in everything from a country's infrastructure to people's daily lives, they nevertheless suffer from significant energy loss during the conversion process. As a result, preserving the nonrenewable energy source could be greatly aided by even a modest improvement in power conversion. Silicon-based power devices, including insulated gate bipolar transistors (IGBTs) and metal oxide semiconductor field effect transistors (MOSFETs), are widely employed in today's power electronic systems but are beginning to reach their theoretical limits. For this reason, III-V semiconductors like gallium nitride (GaN) have been looked to as a more promising option for satisfying the ever-increasing demands of high power, high voltage, and high-frequency applications.

1.1 Overview

Transistor developments and implementations have had far-reaching effects on today society ever since the Germanium point-contact/bipolar junction transistor (BJT) and the Silicon (Si) metal-oxide-semiconductor field effect transistor (MOSFET) were invented and realised on 1947 [1]. Nowadays, the materials of GaN play an unprecedented role to challenge the conventional Si electronics in the semiconductor industry due to its unique material properties, enabling its exceptional promise in the field of power electronics and optical electronics. Baliga's Figure of Merit (BFOM) [2] shows that its wide band gap, high breakdown field (E_{br}), and high saturation velocity (V_{sat}) make it superior to conventional Si transistors for use in

power electronics. It is common practise to utilise BFOM, as demonstrated by Eq.(1-1), as a benchmark, shown in Table 1-1, for assessing the potential of power devices.

$$\text{BFOM}= \frac{4\,V_{bd}{}^2}{R_{on.}} = \mu E_{crit}{}^3 \varepsilon \qquad (1\text{-}1)$$

Table 1-1. materials properties comparison of Si, GaAs, GaN and SiC [3], [25], [26]

	Si	GaAs	GaN	SiC
E_g (eV)	1.1	1.43	3.4	3.3
E_{br} (MV/cm)	0.3	0.4	3.3	3.0
$V_{n,\,sat}$ (cm/s)	1×10^7	1×10^7	2.5×10^7	2×10^7
μ_n (cm^2/Vs)	1350	8500	1000 (bulk) 2000 (2DEG)	650
$V_{p,\,sat}$ (cm/s)	0.7×10^7	0.9×10^7	0.9×10^7	1.3×10^7
μ_p (cm^2/Vs)	<450	<400	<50	<100
BFOM	1	17	827	330

Where E_g is energy bandgap, E_{br} is the breakdown electric field, $V_{n,\,sat}$ is the saturation velocity of electrons, μ_n is the electron mobility, $V_{p,\,sat}$ is the saturation velocity of holes, μ_p is the hole mobility and BFOM is calculated based on the Eq. 1-1 using electron mobility.

GaN material is also capable to achieve heterostructure field effect transistors (HFETs) [4], [5] due to the spontaneous and piezoelectric polarisation [6] in wurtzite structure, resulting in the presence of 2-dimensional hole gas (2DHG) [7], [8] and the two-dimensional electron gas (2DEG) [9], [10] at the GaN/AlGaN/GaN heterointerface. These features enable GaN HFETs to concurrently achieve high carrier concentrations and high carrier mobility, which conventional Si or SiC transistors cannot achieve since intentional impurity-doping is required.

In addition to its usefulness in electronics, GaN also has a significant impact on optics. GaN blue light LEDs have made it possible to create a white light that uses far less energy than traditional light bulbs [11]. Furthermore, the III-nitride and its alloys feature a direct band gap (E_g) covering the whole spectrum from near-infrared to ultraviolet, as shown in Fig. 1-1.

Ultimately, with the future development of GaN related material systems, monolithic integration of GaN-based electronics and optoelectronics can provide compact size, cost-effective, and energy-efficient next-generation system on chips solutions [12].

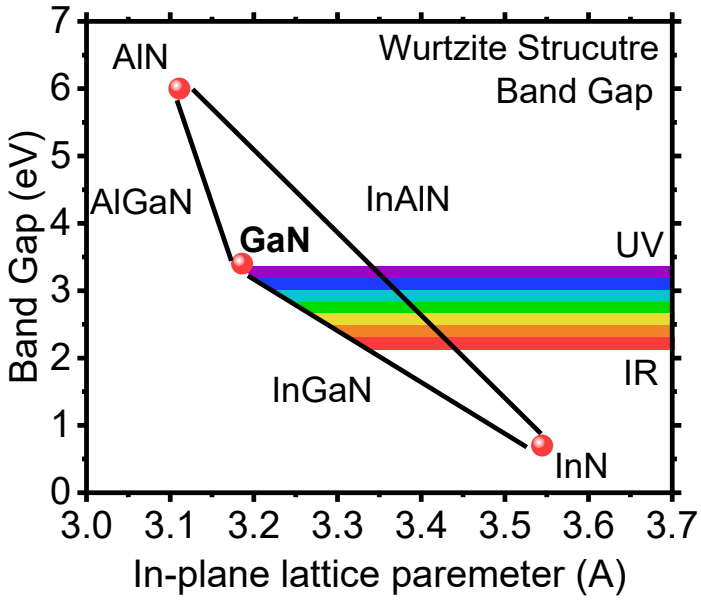
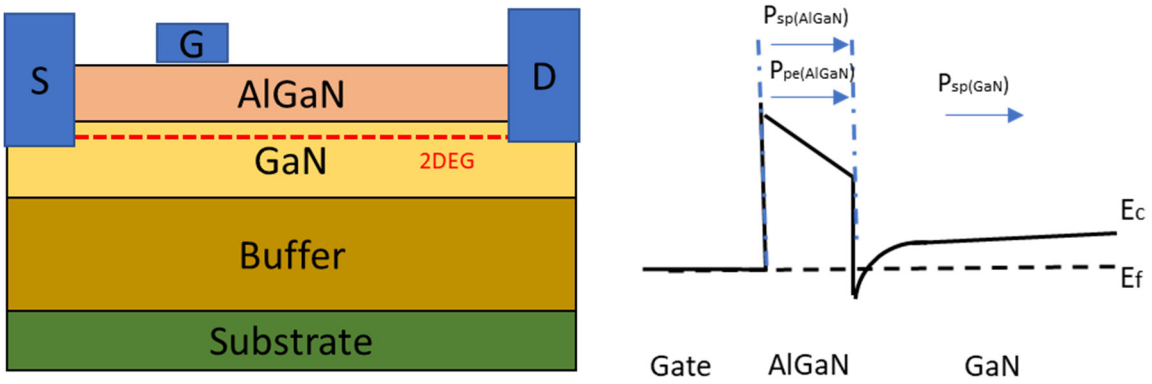


Figure 1-1. Band gap versus lattice parameter plot of III-nitride materials

1.2 Challenges in GaN Electronics

GaN has unique features, but there are still challenges that must be overcome before we can push it to its theoretical limits. It is desirable in power electronics for transistors to operate in enhancement mode (E-mode) to safeguard the entire system from damage or to reduce the severity of damage caused by faults. However, the conventional GaN High Mobility Transistors (HEMTs) is a depletion-mode (D-mode) device, illustrated in Fig. 1-2, [13], [14] due to the presence of 2DEG induced by polarisations. Therefore, GaN HEMTs have been extensively studied in the past decades for achieving high performance enhancement mode (E-mode) operation. Processing techniques such as gate-recessing [15], fluorine treatment [16], and pGaN gate [17] have been extensively studied and make it possible for E-mode operation

and now there are commercial lateral GaN devices available on the market for 650V applications. However, when the breakdown voltage of a device is required to further increase, the source to drain distance has to increase simultaneously for avoiding the electric field from reaching the material's critical breakdown value. Inevitably, the device footprints and R_{on} are increasing at the same time due to this issue and fewer devices may be manufactured on a given-sized epitaxy wafer. The large areas of a device also increase the parasitic elements in an integrated circuit, which further reducing the conversion efficacy and the switching speed in a system.



(a) Basic structure of GaN lateral HEMT (b) Band diagram

Figure 1-2. Concept of GaN-based High Electron Mobility Transistor (HEMT).

As a result, vertical structures, as shown in Fig.1-3, have been offered as an alternative to GaN lateral devices due to their many benefits: First, increasing the thickness of the drift region on the epitaxy level can lead to higher V_{BD} without increasing the area size of the devices themselves [18]. Second, redistributing the surface's peak electrical field into the bulk region reduces surface trapping-related effects, leading to improved reliability [19]. Third, more evenly distributed current allows for greater current capacity [18]. Despite the promising advantageous from the vertical transistors, the vertical current flow nature requires a vertical conduction trench sidewall for modulation the current. The demonstrated vertical Transistor so

far relied on the complicated vacuum system to optimize the plasma dry etching conditions and or channel regrowth to mitigate the dry etching induced crystal defects, which increase the complexity of device fabrication.

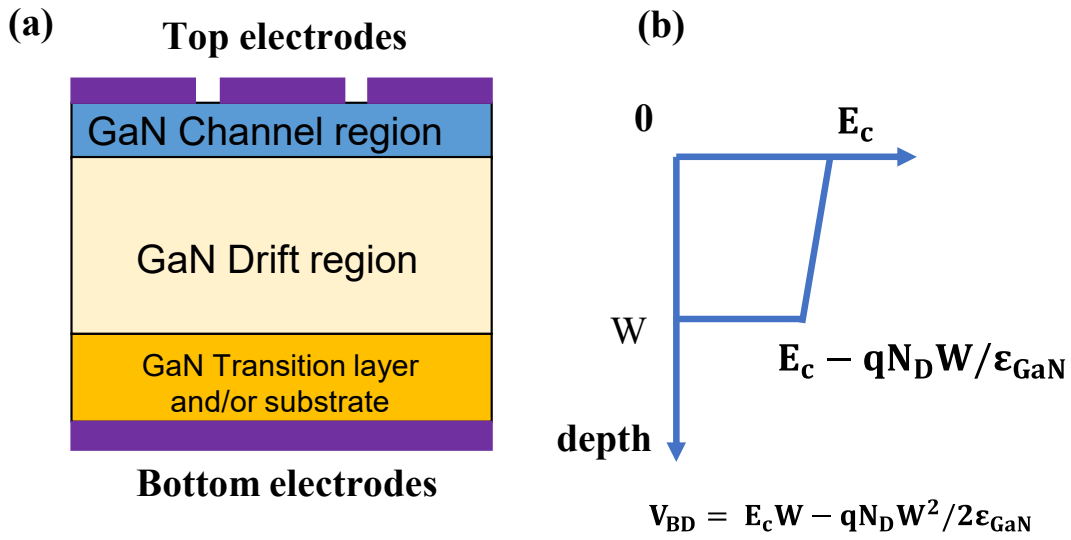


Figure 1-3. (a) an illustrated diagram of the vertical GaN devices (b) electric field profile in the drift region and the mathematical expression for the theoretical value of V_{BD}, where E_c is the electrical field of GaN. W and N_D are the thickness and donor concentration of the drift region.

In another aspect, to take full advantage of GaN electronics, monolithic integration of the gate driver with power switches and/or LED array [12], [20], as shown in Fig. 1-4., is desired to eliminate the parasitic elements in the integrated circuits. The gate driver circuit typically consists of Silicon complementary n-channel and p-channel transistors [21]. Despite the commercial availability of n-channel E-mode GaN HEMTs device, there is no production at the present for its GaN p-channel part because of low hole mobility of ~ 10 - 15 cm^2/Vs [22], upper limit of hole density < 10^{18} cm^{-3} in bulk pGaN [23] and the difficulty of achieving good p-type ohmic contact [24], resulting in the slow development of a p-channel GaN transistor with E-mode operation [21].

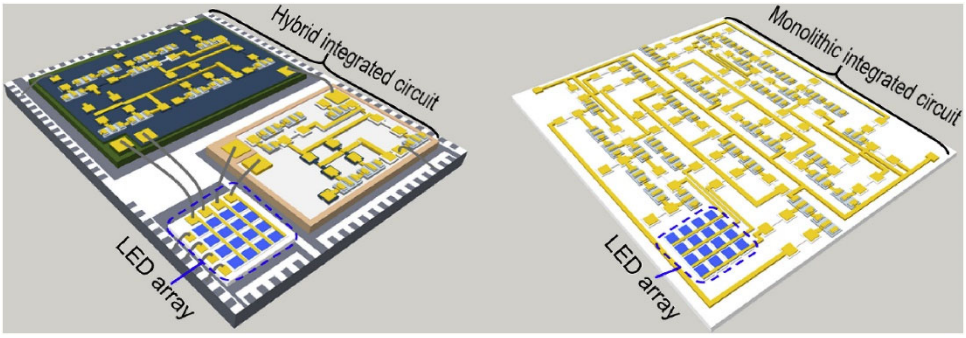


Figure 1-4. The monolithic GaN ICs, reproduced from [12], with permission from the publisher.

As such, novel device concepts and fabrication methods were presented in this project to produce high-performance GaN-based transistors which could be deployed/integrated in many of the above applications.

1.3 Scope and Outline of Thesis

In this report, the novel device fabrication techniques, and novel device epitaxy structure towards achieving energy efficient GaN n-channel and p-channel electronics is proposed and investigated.

For the n-channel GaN transistors, it was focus on the vertical device structure and propose an unconventional trench formation method for the device fabrication on a semi-polar (11-22) GaN platform. The method benefits from the sidewall formation without the need for a complex vacuum system and without the worry of Cl-induced contaminations. For the p-channel transistors, an epitaxy structure by accommodating the Mg back-diffusion was used on the Ga-polar (0001) GaN-on-Si platform. The structure benefits from the graded Mg profile to mitigate the impurity doping scattering's impacts on the 2DHG channel and the back barrier AlGaN providing better confinement of the 2DHG.

This report covers the device design, simulation, fabrication, and characterization of a wide range of advanced GaN transistors: n-channel vertical V-groove semi-polar (11-22) GaN MOSFETs, n-channel vertical semi-polar (11-22) GaN FinFETs, p-channel lateral Ga-polar

(0001) GaN transistor and lateral n-channel Ga-polar (0001) GaN transistor. This thesis consists of 5 chapters:

Chapter 1 provides a brief introduction of the potential and challenges of GaN electronics. The motivation and thesis structure are presented.

Chapter 2 summarizes the background for the development of GaN transistors family. The fundamentals of lateral and vertical n-channel GaN transistors are discussed. Followed by the rationale and development of p-channel GaN transistors.

Chapter 3 describes the design, fabrication, and characterization of semi-polar (11-22) GaN V-groove MOSFETs. It starts by introducing a crystallographic wet etching trench opening method on the semi-polar (11-22) GaN, followed by the detailed fabrication process. Finally, the electrical characteristics of quasi-vertical semi-polar (11-22) GaN transistors are discussed.

Chapter 4 starts with a design and simulation of the vertical semi-polar (11-22) GaN FinFETs, on a semi-polar (11-22) GaN platform. Multiple process modules such as the Fin formation at sub-micro size using crystallographic wet etching, photoresist-planarization, selectively gate metal wet etching and double-stage electron beam lithography alignment are investigated. Individual Fabrication process is integrated for the FinFETs fabrication and the FinFETs' electrical characterization are measured.

Chapter 5 is devoted to the lateral p-channel GaN transistors on the Ga-polar (0001) GaN-on-Si platform for complementary metal-oxide-semiconductor technology. An overview of the wafer structure is firstly provided. An enhancement of p-channel GaN transistors is fabricated and characterized. In addition, the counterpart n-channel GaN is also investigated.

In Chapter 6, a conclusion is given by summarising the findings of the report along with a discussion on future work.

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2. Background Theory

In this chapter, a summary and background theory of the GaN transistors family including both n-channel and p-channel GaN transistors are presented. The related device fabrication concept and its advantages and challenges are discussed, starting from the basics of 2-dimensional electron gas (2DEG) formation and the development of achieving lateral enhancement-mode (E-mode) GaN transistors operation, followed by the vertical transistor GaN transistor device concept and its development. Finally, the origin of 2-dimensional hole gas (2DHG) and the development of lateral E-mode p-channel GaN transistor for the GaN complementary metal-oxide-semiconductor (CMOS) technology were presented.

2.1 Development of Lateral n-Channel GaN Transistors

2.1.1 Basics of AlGaN/GaN Heterostructure Field Effect Transistors

Unlike GaAs high electron mobility transistors (HEMTs), the GaN HEMT is a device based on the presence of the 2DEG in abrupt AlGaN/GaN heterostructure without the need for modulation doping. The presence of 2DEG is the result of the spontaneous polarization (P_{SP}) of wurtzite GaN and the piezoelectric polarization (P_{PE}) of the AlGaN layer tensile strain [1], [2], as shown in Fig 2-1.

The polarization and piezoelectric polarization induced sheet charge density $|\sigma(x)|$ due to abrupt divergence in the AlGaN/GaN heterointerface is calculated by the Eq. (2-1) below as the function of the Al mole fraction x:

$$\begin{aligned} |\sigma(x)| &= |P_{PE}(Al_xGa_{1-x}N) + P_{SP}(Al_xGa_{1-x}N) - P_{SP}(GaN)| \\ &= \left| 2\frac{a(0)-a(x)}{a(x)}\left\{e_{31}(x) - e_{33}(x)\frac{C_{13}(x)}{C_{33}(x)}\right\} + P_{SP}(x) - P_{SP}(0)\right| \end{aligned} \quad (2\text{-}1)$$

Where: $a(0)$ and $a(x)$ are the lattice constants of strained and relaxed materials, e_{ij} are piezoelectric coefficients, C_{ij} are stiffness constants, P_{SP} is the spontaneous polarization along the c-axis of the wurtzite structure

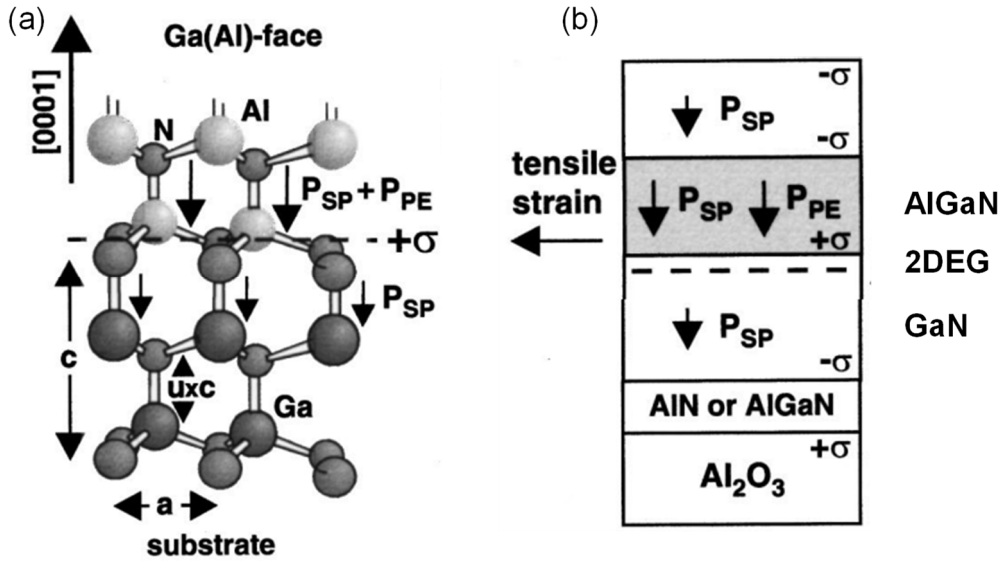


Figure 2-1. (a) Wurtzite Ga(Al)N crystal structure and (b) spontaneous and piezoelectric polarization induced 2DEG at AlGaN heterostructure, reproduced from [2], with permission from the publisher.

Inherently, the AlGaN/GaN HEMT is a "normally-on" device, due to the presence of a high density of the 2DEG at the AlGaN/GaN interface. This leads to the complexity of gate drive circuits and poses a fault tolerance concern [3]. Enormous efforts have been made to achieve "normally-off" operations.

2.1.2 Enhancement Mode (E-mode) GaN HEMTs for Power Switches.

Fig. 2-2 shows a schematic diagram of a standard gate recessing GaN HEMTs. It was firstly reported in 1996 [4] as a straightforward method to achieve E-mode GaN HEMTs operation because the reduction of AlGaN barrier thickness (dAlGaN) resulted in a decrease of the 2DEG

carrier concentration [5] and hence 2DEG is lifted above the Fermi Level corresponding a positive shift of threshold voltage (Vth). Vth of ~0.5V can be achieved on a barrier recessed Schottky gate structure without a gate dielectric [6] and >4 V with metal-oxide-semiconductor (MOS) gate structure [7]. To reduce the AlGaN barrier thickness under the gate, wet etching of GaN is not possible due to the chemical stability of c-plane GaN [8]. Hence, this technology typically requires a reactive ion etching (RIE) or inductively coupled plasma (ICP) etching method to etch the AlGaN barrier. However, this method requires precise control of the recessing depth and the dry etching approach typically introduces damage to the etched surface resulting in degradation of mobility and reliability issues of device operation. Nowadays, a combination of dry etching, wet treatment, and channel regrowth [9] were typically adopted for mitigating the plasma damage on the gate recessed GaN HEMTs.

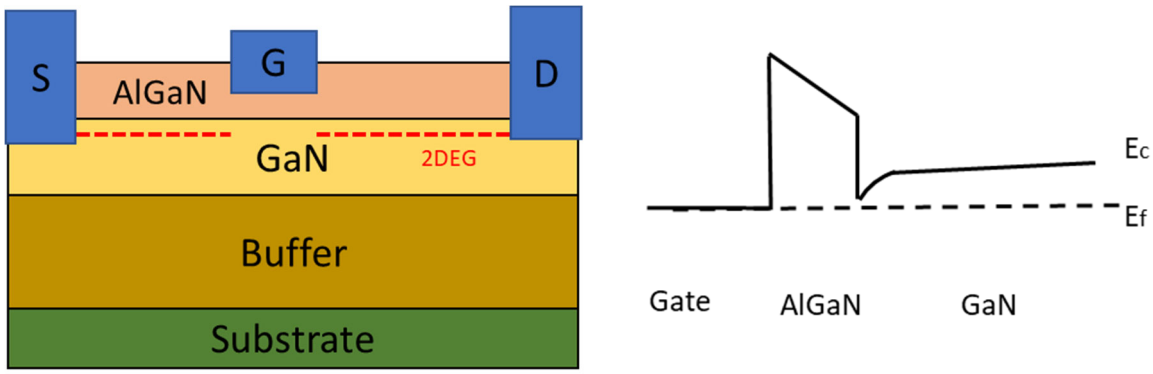


Figure 2-2. (a) A basic structure of gate recessed GaN HEMTs. (b) an illustrated conduction band diagram along the gate.

Alternatively, E-mode operation in the n-channel AlGaN/GaN HEMTs can be achieved by a fluorine (F) plasma treatment/ion implantation under the gate and were first introduced in 2005 [10]. This technology utilises the electronegativity of fluorine ions to modulation the Vth. The presence of F- ion in the AlGaN/GaN heterostructures resulting a certain amount of immobile negative charges and hence leading the upward bending of conduction band [11]. It can

electrostatically modulate the 2DEG in the channel and be able to achieve E-mode modulation. In this context, the F plasma process conditions are critical to the device performance since the F concentration in the AlGaN/GaN heterostructures is directly related to compensation of 2DEG. An insufficient processing time/condition leads to D-mode operation while a prolonged processing time will result in the degradation of mobility. With optimized process condition, the mobility degradation can be controlled to be around 10-20% [12]. Finally, a point of concern for this technology is the stability of F ion in the AlGaN barrier. Under high electric field and long-time gate stress, a negative Vth shift would typically occur [13] due to the effect of F ions impact ionisation [14].

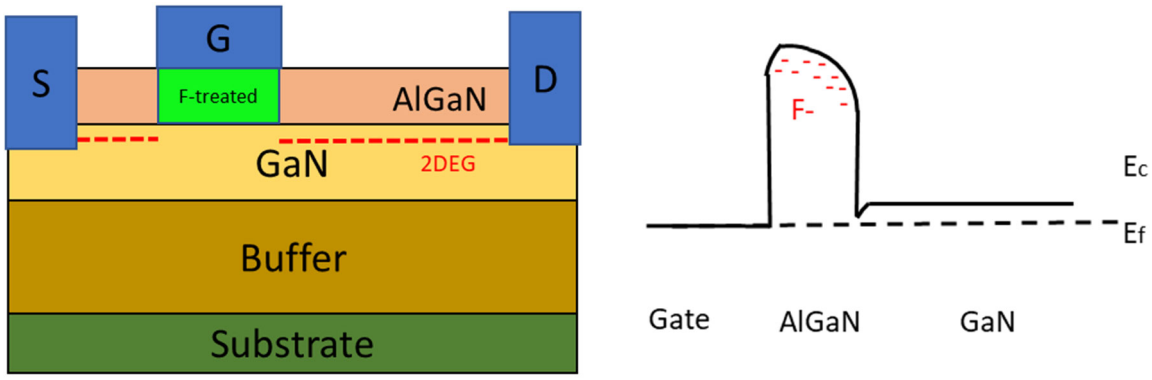


Figure 2-3. (a) A basic structure of a fluorine treated GaN HEMTs. (b) an illustrated conduction band diagram along the gate.

An approach to achieve E-mode operation while mitigate the plasma etching/treatment's impacts under the gated region is the p-GaN technology. In this technique, a p-GaN layer is grown on the AlGaN/GaN structure and the top p-GaN layer is etched away during the device fabrication except in the gated region. Due to the presence of the p-GaN, the conduction band of the AlGaN/GaN is lifted above the Fermi level and hence E-mode operation is achieved. The challenges in this technology are: 1) control of doping in the p-GaN layer to counterbalance the 2DEG to achieve precise V_{th} control, 2) high gate current issue due to the forward-biased

p-n junction of the p-GaN/AlGaN at a positive gate bias, and 3) plasma damage induced surface states on the etch AlGaN surface which leads to dynamic on-resistance issues during the switching operations [15].

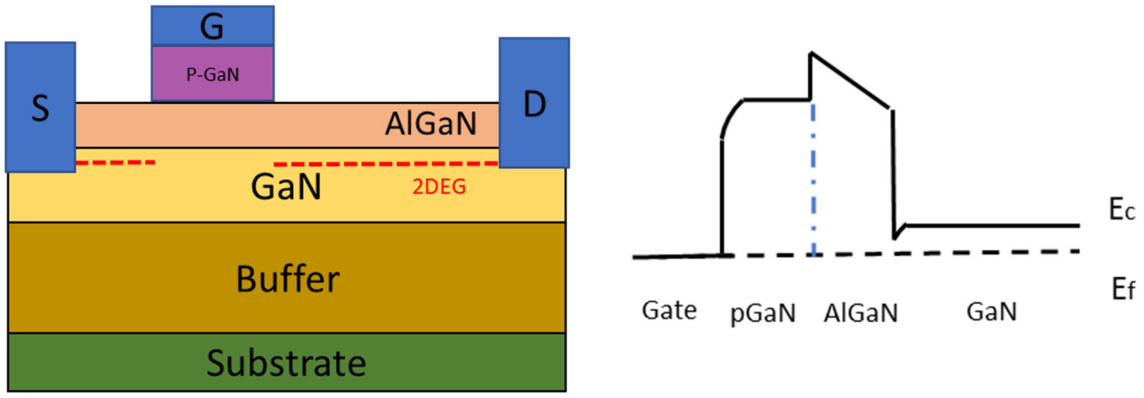


Figure 2-4. (a) A basic structure of a p-GaN gate GaN HEMT. (b) The conduction band diagram along the gate of the p-GaN gate GaN HEMT.

2.2 Vertical GaN Transistors

Various GaN-based power transistor with vertical topologies have been proposed and demonstrated in the past two decades. It can be predominantly classified into four devices structures, as shown in Fig. 2-5: (1) current aperture vertical electron transistors (CAVETs), (2) trench metal-oxide-semiconductor field-effect transistors (3) vertical fin field-effect transistors and (4) junction field-effect transistors (JFETs). Currently, all these vertical structures are based on the c-plane (0001) GaN orientation.

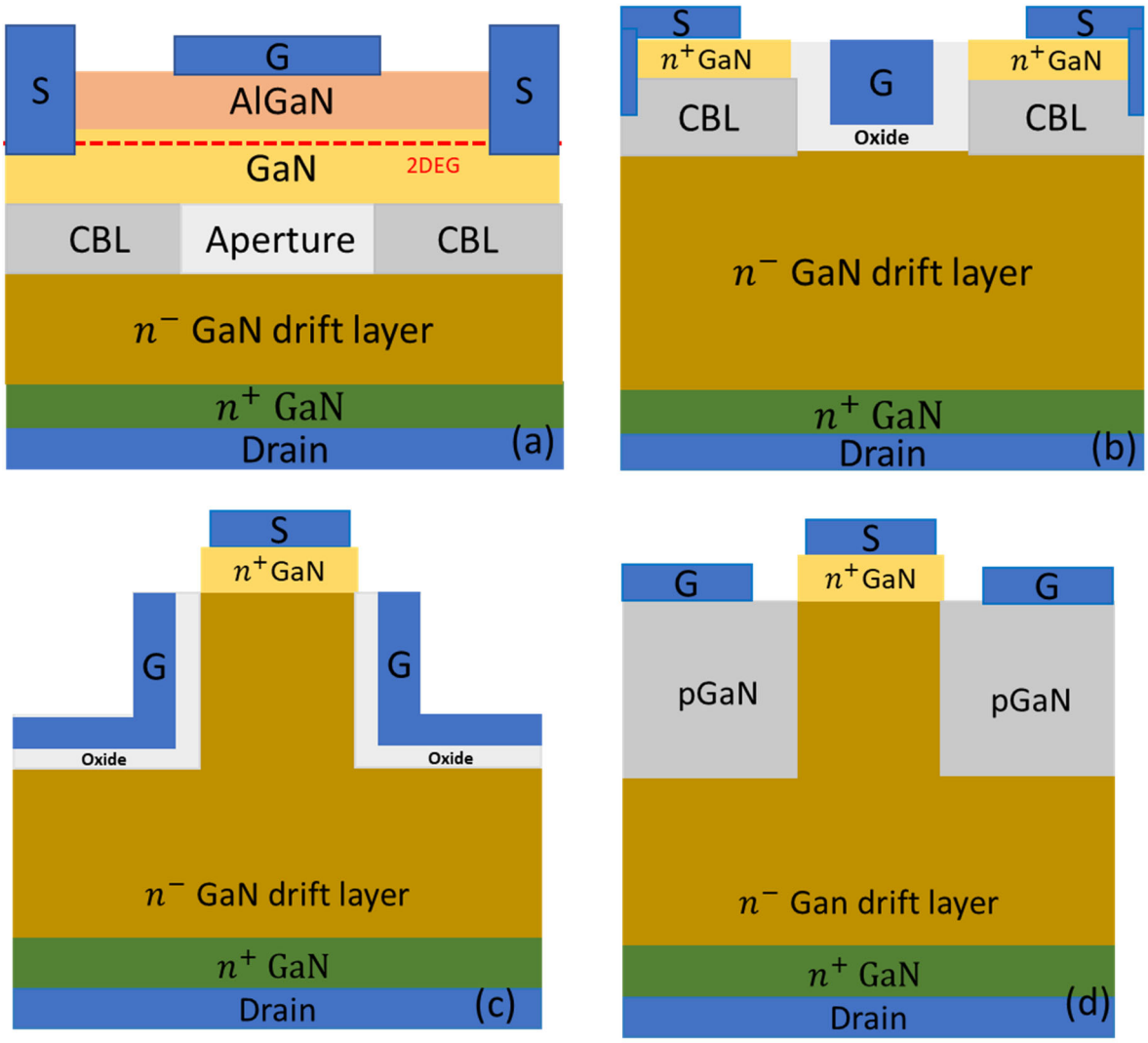


Figure 2-5. Reported GaN-based vertical transistors: (a) CAVET, (b) Trench MOSFET, (c) Fin FET and (d) JFET

2.2.1 Current Aperture Vertical Electron Transistors (CAVET)

The concept of current aperture vertical electron transistors (CAVET), as shown in the Fig. 2-5 (a), can be traced back to 2004 [16], [17]. It is effectively a modified version of lateral AlGaN/GaN HEMTs. The epitaxial structure consists of a p^+-GaN current blocking layer (CBL), n^--GaN drift layer and n^+-GaN layer for the drain ohmic contacts. The structure is then plasma-etched to form an aperture on the p^+-GaN CBL. n^--GaN is then re-grown on the structure to fill the etched aperture and finally capped with an AlGaN layer to form an

AlGaN/GaN heterostructure on the top of the structure. This type of device utilises the advantage of highly conductive AlGaN/GaN 2DEG channel while achieve an improved electric field distribution than that of the lateral structure.

In the ON-State, the electrons first flow through lateral direction from the source on the 2DEG and then through the aperture of the CBL vertically in the center and collected by the bottom drain contact. In the OFF-state, the 2DEG is depleted by a negative gate bias and therefore no electrons will pass through the aperture. In addition, the p-n junction formed by p-type CBL and n-type drift layer blocks the off-state voltage. It is found that the overlap between the gate and the CBL as well as the p-n junction in the center have a significant impact on its performance [17], [18], [19]. A resistive aperture would lead to poor saturation drain current and high R_{on}. A conductive aperture would increase the leakage current and reduce V_{bd}. A CAVE is a normally-on device due to the presence of 2DEG [18], [20]. The normally-off operation can be achieved using were reported with Si_3N_4/AlGaN/GaN gate structure with a breakdown voltage of 225V, limited by the gate dielectric breakdown. More recently, a high performance E-mode CAVET with V_{BD} >1.5kV and R_{on} < 2.2 mΩcm^2 was reported using a p-GaN gate structure [21], [22].

2.2.2 Trench Metal-Oxide-Semiconductor Field-Effect Transistors

The trench MOSFET has been explored extensively on the Si or SiC platforms for power switching applications [23]. The GaN-based trench MOSFETs were first demonstrated in 2007 [7]. Thereafter, a variety of trench MOSFET structures have been proposed and studied. Its simplest concept is illustrated in Fig. 2-5 (b). The operation principle of the trench MOSFETs is as follow: an inversion channel is formed in the p-GaN/dielectric interface on the channel sidewall when a positive voltage above the threshold voltage (V_{th}) is applied. The electrons

flow vertically from the source terminal along the vertical sidewall channel, spread into the drift region and collected by the bottom drain contact.

Unlike the AlGaN/GaN 2DEG channel based transistors, the trench MOSFET with the inversion channel is a normally-off device, which is preferred in the power electronics system for safety reasons. However, this type of structure suffers from the low electron mobility and trapping effect in the MOS-channel.

The trench MOSFETs also require a buried p-type GaN layer to serve as the current blocking layer. However, the buried p-type GaN layer is likely to be passivated during the hydrogen (H)-rich metalorganic chemical vapour deposition growth a capping layer due to the formation of magnesium(Mg)-H complex [24],[25],[26],[27]. The activation of the p-GaN layer is challenging due to the buried nature in comparison with the exposed p-GaN layer. This is because the built-in electric field in the n-p junction between the top n-GaN layer and the p-GaN layer prevents the hydrogen in the buried layer from moving towards the top surface [28] and hydrogen has lower diffusivity in the n-type GaN [27], [29]. The insufficient activation of the p-type GaN would cause a premature punch-through breakdown in the power devices [28], [30].

2.2.3 Vertical Fin Field-Effect Transistors

To avoid the issue originates from the p-GaN, vertical GaN fin power FET is proposed [31]. This structure, as shown in Fig. 2-6 (c), can significantly simplify the wafer structure since the p-GaN layer growth is not required. The large-area FinFET device [32] achieved an 1.2 kV, 5A rating and R_{on} of 2.1 mΩcm^2 with competitive switching performance against the commercial 1.2 kV devices.

In this structure, assuming an ideal MOS interface with a fixed interface charge and no fermi level pinning effect taken place, the Vth can be tailored by modifying the work function difference between gate metals and GaN [31], and the fin channel is theoretically able to pinch-off without applying a negative gate bias. With the increasing of V_{gs} (positive), the depletion width decreases, and a channel is formed. The E-mode operation of this structure requires the fin width control and a low doping concentration in the drift layer. When the fin width reducing to 200-500 nm, the channel can be fully depleted without negative bias. The current rating of this transistor can be increased by increasing the number of fins as well as channel length [32]. However, in this structure, the good depletion requires either small (<200nm) fin widths or lower doping concentration in the drift region. By lowering down the fin width, the gate conformity is becoming difficult. The lower n^- GaN drift doping is difficult to achieve as well due to carbon incorporation. Even if low doping concentration is achieved, it requires more Fins channel to achieve high current rating which would increase the contact resistance of the transistors.

2.2.4 Vertical Channel Junction Field-Effect transistors

As described in the vertical fin FET topology described above, a MOS structure is required for the gate structure. However, the GaN-based devices are still lack of an effective approach to achieve a robust MOS gate technology [33]. On the other hand, the cv-JFETs is advantageous for mitigating MOS gate reliability problems and the excellent electrical performance has been demonstrated in the SiC JFETs [34], [35]. Fig. 2-5 (d) shows the vertical JFET structure. The JFET device structure is similar to that of the fin FETs except the vertical channel is pinched off by the depletion region during OFF-state created by the p-GaN/n-GaN/p-GaN junctions. In the ON-state, a positive gate bias is applied to the p-GaN region with respect to the source which reduces the depletion width of the p-n junction. This enables the electrons to flow from

the source to the drain terminal. The fin width, the doping concentration in the fin as well as in the p-GaN are critical in order to achieve E-mode in the JFETs.

Despite the earlier proposal and simulation study of GaN vc-JFET in [36], [33], the vc-JETs has only been experimentally verified in 2018 [37] by an selectively regrowth approach. Although this technology is demonstrated relatively late comparing with other vertical GaN transistors, a 1.2kV class vc-JFETs with fast switching performance, avalanche capability, high temperature stability [38], [39], [40], and >10 μs short circuit robustness at 800V [41] are demonstrated recently by NexGen Power Systems Inc. on GaN substrates. The down-side of this device topology is that the p-GaN re-growth between the etched fins is required and a very good re-growth interface between the p-GaN and n-GaN is needed for a good electrical performance. In addition, a high gate positive bias will lead to a high gate current in the JFETs, as a result of the forward-bias of the p-n junction.

2.3 The Lateral p-Channel GaN-based Heterostructure Field-Effect Transistor

2.3.1 Introduction

Despite the promising characteristics from the n-channel lateral or vertical GaN transistors, the end systems using GaN devices are commonly limited by the parasitic elements in the integrating circuits (ICs) [42]. The silicon complementary metal-oxide-semiconductor (CMOS) based technology is used for complex logic control. Fig. 2-6 shows a typical CMOS structure and its transfer characteristics. Both of the p-channel and n-channel MOSFETs are E-mode and their drains are connected to serve as the output node. When the input voltage is lower than the V_{th} of n-channel transistor and higher than the V_{th} of p-channel transistor, the n-channel transistor is in OFF-State and the p-channel transistor is in ON-State, with the output node charging to V_{dd} and achieving logic “1”. When the input voltage is higher than V_{th} of n-channel

transistor and lower than the V_{th} of p-channel transistor, the n-channel transistor is in ON-state and the p-channel is in OFF-state, with the output node discharging to ground and achieving logic "0". It is of importance to achieve a match Vth for both n-channel and p-channel transistor for achieving the low power consumption and noise immunity of CMOS.

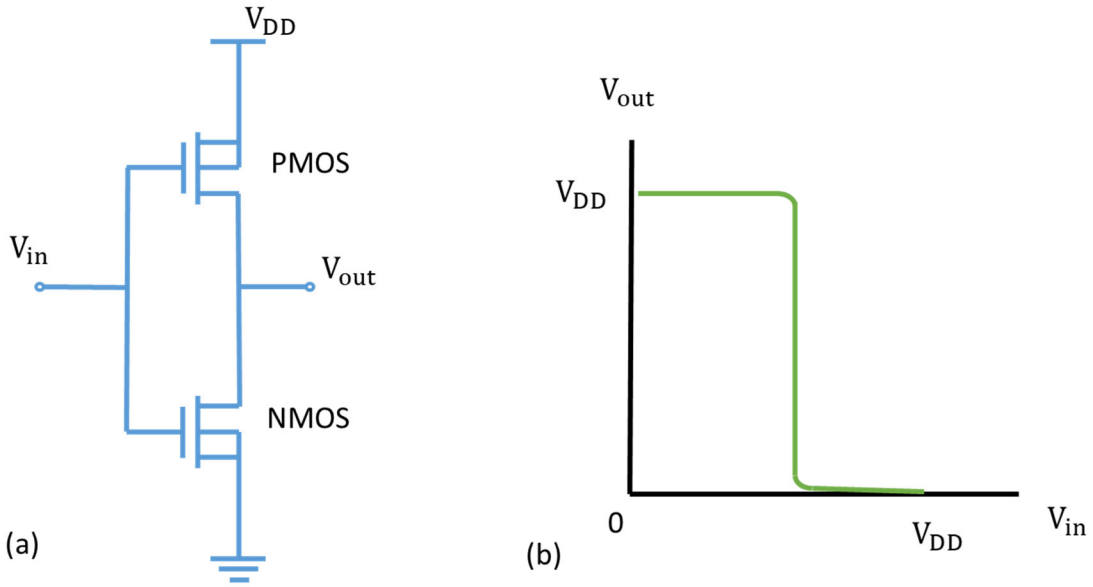


Figure 2-6. (a) The CMOS inverter (b)Transfer characteristics of a COMOS inverter.

For achieve the full potential of the high speed and high-efficiency GaN ICs, there is a great interest of monolithic implementation GaN CMOS on the epitaxy level [43]. The development of the state-of-art E-mode p-channel GaN transistors is summarized in the next subsection.

2.3.2 Development of E-mode p-Channel GaN HFETs for Complementary Integrations

As shown in Fig. 2-7, the PSP and PPE will not only lead to the formation of 2DEG at AlGaN/GaN heterojunction, but also result in the formation of 2DHG at the GaN/AlGaN heterojunction. The study of 2-Dimensional Hole Gas (2DHG) at GaN/AlGaN heterojunction can be tracked back to 1999 [44] and the 2DHG gate modulation at 20K are experimentally

verified in 2004 [45]. However, the developments of high-performance E-mode p-channel transistors are not well established as this technology is limited by: (1) low hole concentration due to the large Mg dopant activation energy of 125 -215 meV [46] and the formation of Mg-H complexes during MOCVD growth [27], (2) difficulty of achieving good p-type ohmic contact [47], (3) low hole mobility of pGaN [48] and (4) the presence of 2DHG resulting the normally-on operation behaviour of p-channel transistors.

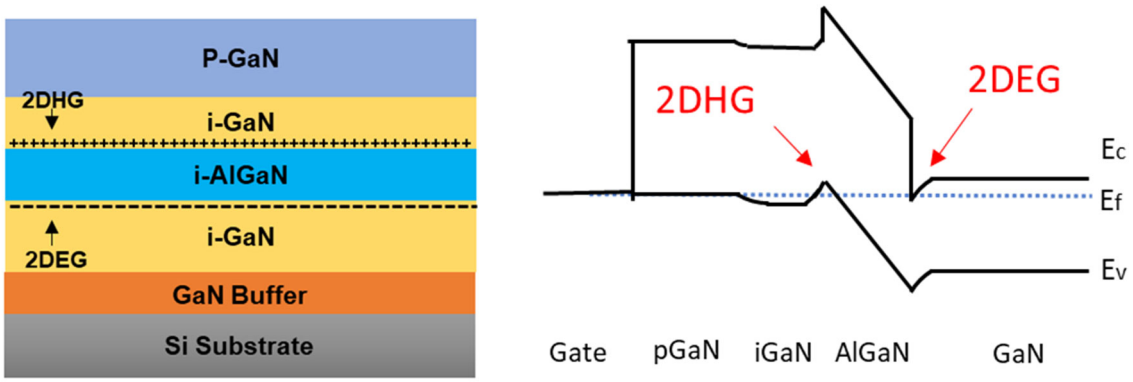


Figure 2-7. (a) A basic structure of GaN/AlGaN/GaN heterojunction structure. (b) an illustrated band diagram.

In the past, the p-channel GaN transistors have been explored by different research groups based on the InGaN/GaN [45], GaN/AlInGaN [49], GaN/AlN [50] and GaN/AlGaN [51] induced 2DHG. On these structures, it has higher polarization difference than that standard AlGaN/GaN structures which can induce more hole, which is advantageous to improve the output current density [50]. Among these hetero-structures, the first E-mode p-channel transistors were demonstrated in 2013 [49] and first complementary GaN device demonstration in 2014 by RWTH Aachen University [52]. In their demonstrations [49], [52], [53], gate-recessing were used to obtain E-mode operations and devices were featured with Schottky gate, which limiting the gate voltage operating range to a maximum ± 2 V. A steep subthreshold slope of 60 mV/dec and maximum drain current of ~ -0.1mA/mm at V_{ds} = - 0.1 V were

demonstrated [52]. They also have observed the highest hole mobility of 43 cm^2/vs and a moderate 2DHG density of 1.3 $\times 10^{12}$ cm^{-2} for the D-mode operations [53].

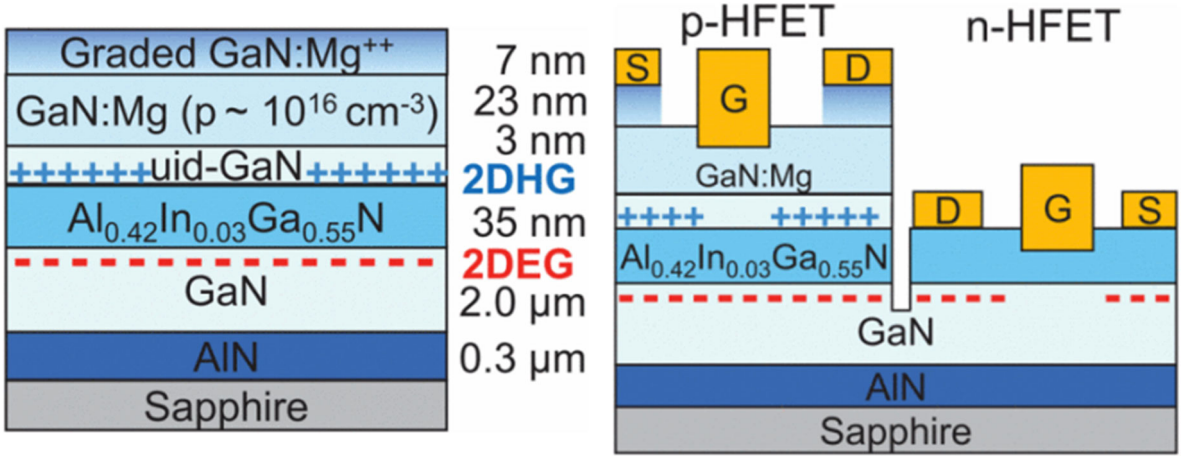


Figure 2-8. (a) wafer epitaxy structure (b) device structures of p-channel and n-channel HFETs, reproduced from [52], with permission from the publisher.

More recently, the GaN/AlGaN/GaN platform, as shown in Fig. 2-8, has seen a significant attention for the development of the enhancement mode p-channel GaN HFETs [54], [55], [56] due to the commercial availability, easy integration with the n-channel transistors without the need of additional re-growth [54], [57] and offer a scalable technology up to 300 mm Si substrates [58], [59].

The development of the E-mode p-channel GaN transistors were not as well established as E-mode n-channel GaN transistors. There have been mainly two technologies established to achieve E-mode p-channel GaN: (1) gate-recessing and (2) plasma treatment. The direct gate-recessing method suffers the same difficulty as the similar situation faced by the n-channel transistors such as difficulty of precise etch depth control and the dry etching introduced surface contaminations/damage. On the other hand, plasma treatment seems to mitigate the dry etching induced damages on the 2DHG. O_2 plasma treatment in combination with gate-recessing were explored by HKUST [60], [61], [57] with promising performance. However, the device suffers significant V_{th} instability due to the presence of Mg-Ga-O traps [62], [63].

Technique such as SiN_x/in-situ-GaO_xN_{1-x} gate structures were introduced to improve the gate reliability issue [64]. H_2 plasma treatment were also reported to passivate p-GaN and achieve E-mode operation. However, the reported device shows a low drain current of < -0.1 mA/mm at V_{ds}=-5V [65], which is about 10 time smaller compare with other reported E-mode devices [54], [60]. Further optimisation of H_2 plasma treatment approach is still needed.

2.4 Metal-Oxide-Field Effect Transistor (MOSFET) Fundamentals

As this thesis cover a wide range of novel n-channel and p-channel transistors, the basic characteristics of four types of typical MOSFET is provided in this subsection.

2.4.1 Four Types of MOSFET

Fig. 2-9 provides a summary for four standard MOSFETs' operation principles. The device typical cross section, output and transfer characteristics are illustrated. For a n-channel transistor, the majority carrier of current flow is electron, if a positive gate bias required to applied for the channel inversion, then the device is called enhancement-mode (normally-off) MOSFET. If a negative gate bias is required to deplete the carriers in the channel, then the device is called depletion-mode (normally-on) MOSFET. P-channel MOSFETs function in the same way as n-channel MOSFETs, but the polarities of the currents flowing through them are reversed. A negative gate voltage is used to enhance the channel for an enhancement-mode p-channel MOSFET and a positive gate voltage is required to deplete the channel for a depletion-mode p-channel MOSFET.

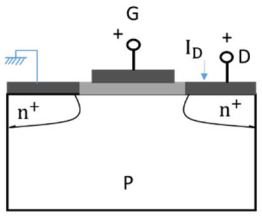
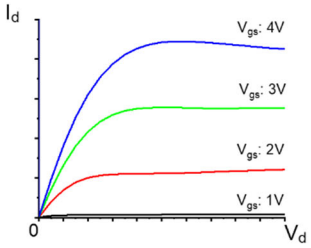
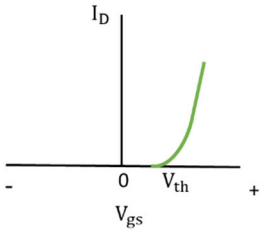
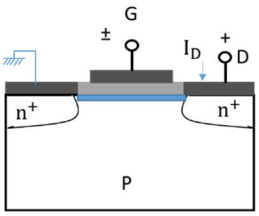
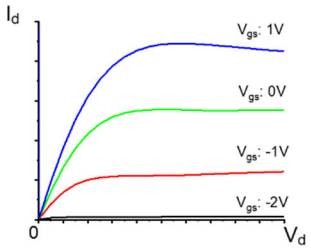
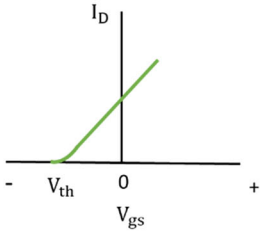
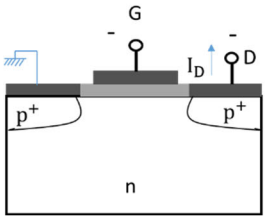
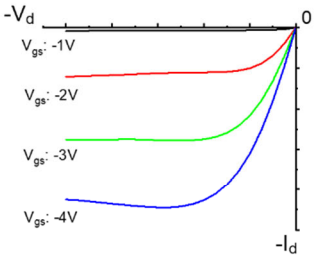
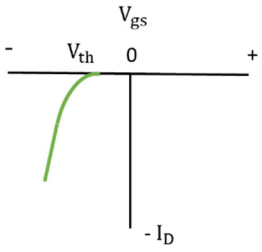
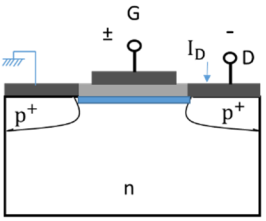
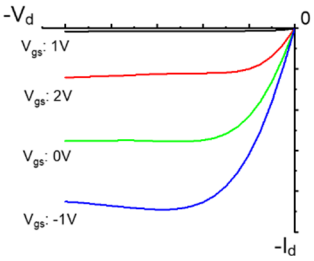
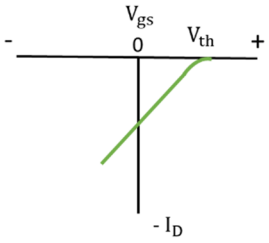
Type	Cross section	Output characteristics	Transfer Characteristics
n-channel Enhancement (Normally OFF)			
n-channel Depletion (Normally ON)			
p-channel Enhancement (Normally OFF)			
p-channel Depletion (Normally ON)			

Figure 2-9. Different types of MOSFET.

2.4.2 Performance Parameters

In this section, the typical parameters of an enhancement-mode n-channel MOSFET are presented. These extractions of these characteristics are readily applicable to p-channel devices with changing polarity.

2.4.2.1 Threshold voltage

The threshold voltage, V_{th}, is the minimal gate electrode bias necessary to sufficiently invert the MOS structure so that a conducting channel between the source and drain regions is produced. The ideal V_{th} physical model for a n-channel enhancement mode Si MOSFET device can be expressed by Eq. (2-2) and (2-3) and the corresponding ideal band structure is illustrated in Fig. 2-10.

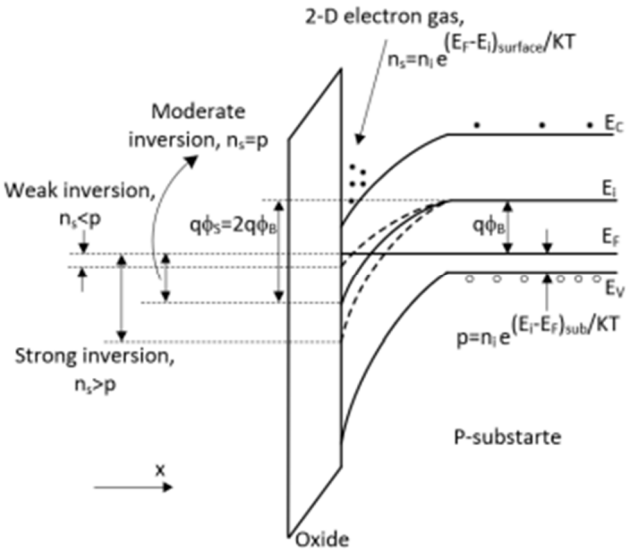


Figure 2-10. Typical energy band diagram of an n-channel enhancement-mode MOSFET, reproduced from [66], under Creative Commons CC BY 3.0 license.

$$V_{th} = V_{FB} + 2\Psi_B + \frac{\sqrt{2\varepsilon_s q N_A (2\Psi_B + V_{BS})}}{C_O} \tag{2-2}$$

Where V_{FB} is the flat-band voltage shift induced by the fixed-oxide charge and the metal-semiconductor work function difference, $2\ \Psi_B$ is the electrostatics potential reaching the strong inversion, N_A is the acceptor concentration on the p-substrate. V_{BS} is the reverse substrate-source bias. C_O is gate capacitance per unit area.

The V_{FB} can be expressed as :

$$V_{FB} = \phi_{ms} - \frac{(Q_f + Q_m + Q_{ot})}{C_o} \tag{2-3}$$

Where ϕ_{ms} is the metal-semiconductor work function difference, Q_f is the fixed oxide charge, Q_m is the mobile ionic charge, Q_{ot} is the oxide-trapped charged and C_o is oxide capacitance per unit area.

From the Eq. 2-2, it can see that for tailoring the V_{th} of the MOS transistor, the most widely used strategic is to modify the carrier concentration in the bulk, the use of novel gate oxide materials and the metal-semiconductor work function difference. A wide range of techniques as described in the section 2.1-2.3 is to engineer these parameters and to achieve enhancement mode operation of lateral and vertical GaN transistors.

In practice, V_{th} normally defines in two ways from the experimental measured I_d-V_g characteristics. This first way of defining V_{th} is to obtain the peak transconductance (g_m) value from the $\partial I_D/\partial V_G$ at small V_D (typical < 1V), and use the value of peak g_m and V_g for the liner interpolation to obtain the correspond V_{th}, as shown in Fig. 2-11 (a). The second way is to plot the measured I_d-V_g characteristics in the log-scale and specified a fixed value (i.e ~ μA) , as shown in Fig. 2-11 (b). The corresponding V_g is then defined as the V_{th} for the transistor.

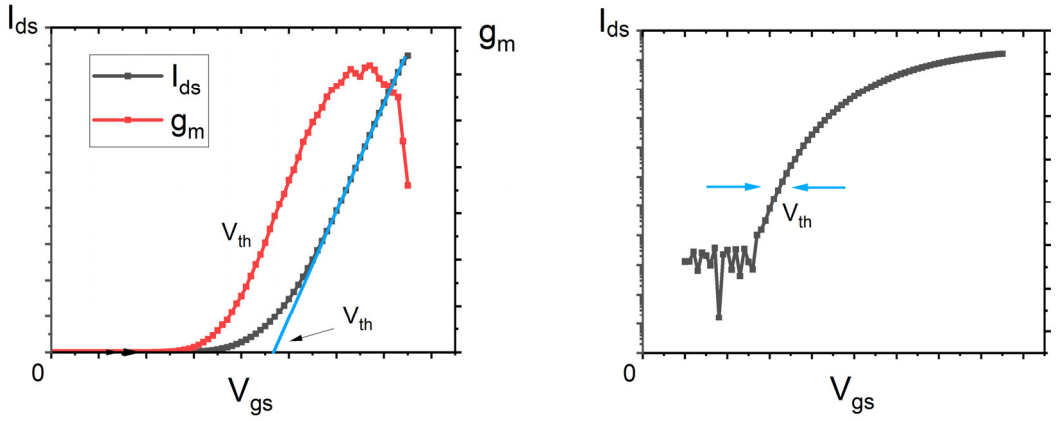


Figure 2-11. Typical gate transfer characteristics (a) in the linear-scale (b) in the log-scale.

2.4.2.2 Transconductance

The transconductance (g_m) represents the effectiveness of the gate control on the current flow between the drain to source electrode and mathematically calculated by the derivative of I_d divided by the derivative of V_g at the fixed drain voltage (V_D). The Eq. (2-4) is also widely used to extract the channel mobility μ_n [67]. A large transconducatnce value is desirable for a transistor.

$$g_m \cong \frac{\partial I_D}{\partial V_G}\Big|_{V_{D=constant}} \cong \frac{Z}{L}\mu_n C_o(V_G - V_T - V_D) \cong \frac{Z}{L}\mu_n C_o V_D \quad (2\text{-}4)$$

2.4.2.3 Output current voltage characteristics

The drain current flow through the channel of a transistor can be estimated by the Eq. (2-5).

$$I_{ds} = q n_s \nu_{eff} \quad (2\text{-}5)$$

where ns is the sheet density, q is the electronic charge and ν_{eff} the effective electron velocity.

When the transistor is operated at the region with small drain to source bias ($V_{ds}=V_{gs}-V_{th}$), the I_{DS} increase linearly with the applied voltage. Thus, the transistor acts as a resistor. This region is typically called linear region or ohmic region. The ON-state resistance (R_{on}) of a transistor is typically extracted from this region from the ohms' law.

For a long channel (channel length > few microns) ideal field effect transistor, with the further increasing of drain to source bias ($V_{ds}> V_{gs}-V_{th}$), the thickness of the inversion layer at the drain-side reduced and the number of electrons reduce at the drain side of the channel. The channel pinch-off. Beyond this pinch-off point, the drain current will not keep rinsing as in the linear region. This region is called the pinch-off saturation. For a short channel (channel length < sub-micron) field effect transistor, the drift velocities of carrier initially appear as linear relationship. With the increased of the electrical field, it departs from the linear relationship and saturate at sufficiently large electrical fields. Even low voltage can result in the high field

saturation along the channel for short channel devices compared to the long channel devices [68].

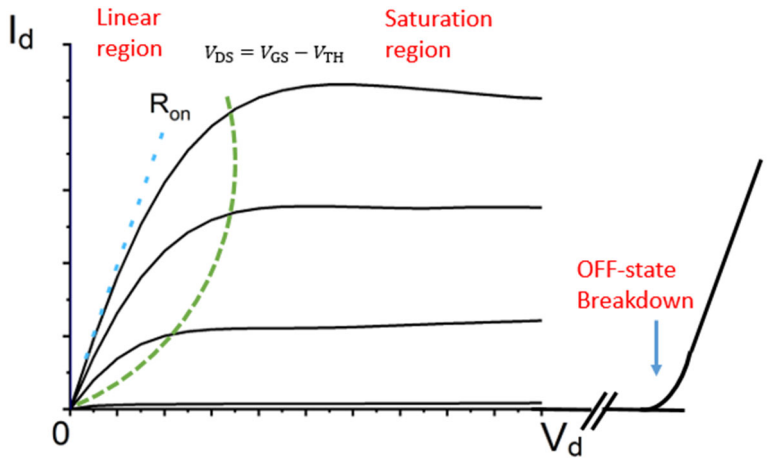


Figure 2-12. Typical transistors output current-voltage characteristics.

The breakdown voltage (V_{bd}) of a transistor represents the maximum voltages that a transistor can handle for its 3-terminals at its OFF-states. It occurs with further increasing of applied drain bias and the electrical potential reaching the material critical electric field. The V_{bd} can be enhanced by the increasing the gate to drain separation with the expense of increasing R_{on}. The field plate is the most common strategy to modulate the electric field in the OFF-state for a transistor to redistribute the peak electric field and improve the V_{bd}.

2.5 Sentaurus Technology Computer Aided Design

Synopsys Corporation's Sentaurus Technology Computer-Aided Design (TCAD) serves as the simulation tool that is being applied to this particular project. It is able to solve fundamental physical partial differential equations, which allows for numerical prediction of the electrical characteristics of semiconductor devices. Fig. 2-13 illustrates the workflow for the simulation procedure.

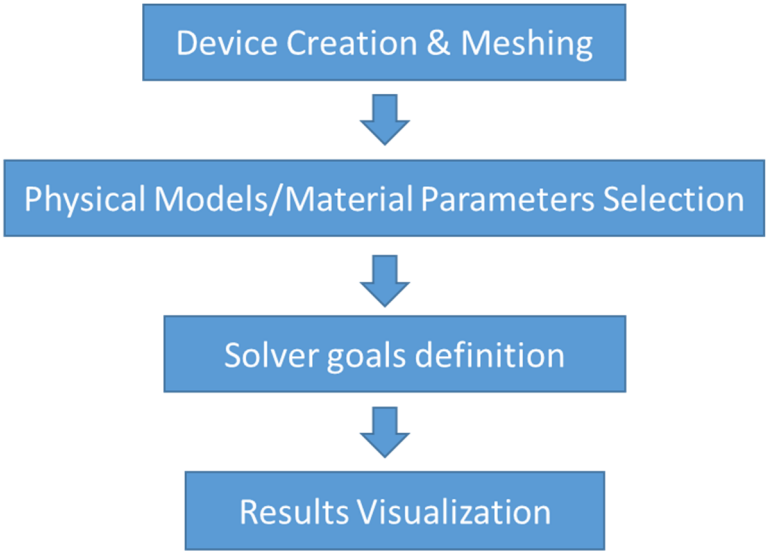


Figure 2-13. Process flow of Sentaurus TCAD device simulation.

The Sentaurus Structure/Mesh program is initially utilized for the purpose of generating a user-defined structure. The Sentaurus Device is then used to simulate the electrical characteristics and define the physical properties. Simulation is carried out by resolving Poisson's equation in conjunction with the two-dimensional (2D) drift-diffusion carrier transport equations and the current continuity equations. The current densities for electronics and holes are calculated by the equation below:

$$\vec{J}_n = \mu_n(n\nabla E_c - 1.5nkT\,\nabla \ln m_n) + D_n(\nabla n - n\nabla \ln \gamma_n) \quad (2\text{-}6)$$

$$\vec{J}_p = \mu_p(p\nabla E_c - 1.5pkT\,\nabla \ln m_p) + D_p(\nabla p - p\nabla \ln \gamma_p) \quad (2\text{-}7)$$

Where:

- $\vec{J}_n$ and $\vec{J}_p$ are the electron and hole current density.
- n and p are the electron and hole density.
- μ_n and μ_p are the electron density and hole density.
- m_n and m_p are the electron and hole effective mass.
- D_n and D_p are the diffusivities of electrons and holes.
- E_c and E_v are the conduction and valence band energy level.
- K is the Boltzmann constant.

- T is the temperature in Kelvin.
- γ_n and γ_p =1 for Boltzmann statistics.

The solutions of the above equations are stored in the vector datasets and can be inspected by the Sentaurus Visualizer/Inspect tool. Sentaurus workbench is used to drive a variety of simulation and visualization tools.

2.6 References

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3. Fabrication and Characterization of Semi-Polar (11-22) GaN Vertical V-groove MOSFETs

3.1 Introduction

To modulate the vertical current flow, GaN vertical transistors require a vertical conduction channel. Until now, plasma-dry etching techniques were the only demonstrated method for vertical trench formation due to the chemical inert properties of c-plane (0001) GaN. It has been reported that the etching plasma conditions [1], etching hard mask materials [2], and the choice of carrier wafer [3] would strongly affect the etched surface morphology. On the etched surface of GaN, ion bombardment can leave crystal defects and dry-etching by-product contaminations. As a result, wet etching post-treatment and/or additional channel regrowth were widely used to mitigate the effects of physical bombardment on the dry-etched GaN surface. However, these techniques increase fabrication complexity and required additional vacuum system for the optimization on the dry-etch or the channel regrowth. Therefore, fabrication of the vertical transistors without the plasma etching is highly desirable.

Monolithic integration of GaN LEDs with vertical GaN transistors has been proposed and demonstrated in the recent years on the c-plane (0001) GaN direction to achieve the ultra-compact displays applications[4], [5], [6], [7]. However, the c-plane GaN LEDs suffer from the quantum-confined stark effect (QCSE) and the difficulty of indium content incorporation for shorter emission wavelength such as green and red [8]. On the other hand, semi-polar (11-22) LEDs have been shown to suppress the QCSE effect and have a higher indium incorporation efficiency compared to c-plane (0001) GaN [9]. However, there are limited studies reported on the semi-polar (11-22) GaN transistor to date.

This chapter proposes and explores a novel crystallographic hydroxide-based wet etching technique for vertical trench channel formation on the semi-polar (11-22) GaN vertical V-

groove MOSFETs. This method differs from the conventional vertical trench formation technique on the c-plane (0001) GaN direction which relies on dry-plasma etching technique. A study on the hydroxide-based wet-etching on the semi-polar (11-22) GaN to form the vertical trench sidewalls for channel conduction in the V-groove MOSFETs was performed initially. The first experimental demonstration of the semi-polar GaN V-groove MOSFET with a vertical channel formation without the use of dry-plasma GaN etching at semi-polar (11-22) GaN platform is presented. Simulations including device level technology computer aided design (TCAD) and SPICE were performed to understand the performance of the fabricated V-groove MOSFETs.

The photolithography mask layout design, device fabrication, device electrical characterization of the semi-polar (11-22) GaN Vertical V-groove MOSFET, and the investigation of the wet etching by the scanning electron microscopy (SEM) images were conducted using the EEE facility, at the University of Sheffield. The epitaxy wafer of the semi-polar GaN sample was grown on a 2-inch m-plane sapphire substrate, by the University of Cambridge. The cross-sectional scanning transmission electron microscopy (STEM) images of the 3-terminal Vertical V-groove MOSFETs were captured by Dr. Colm O'Regan from the Sorby Centre for Electron Microscopy, the University of Sheffield.

3.2 Wet Etching of GaN

3.2.1 GaN Crystal Structure and Wet Etching Mechanism

The most well-studied GaN crystal structure is the wurtzite structure with the lattice constant values of a= 3.189 A and c= 5.185 A, the Ga and N are in mirror symmetry along (0001) direction (c-axis) as an ABABAB sequence. Fig. 3-1 depicts the typical crystallographic planes in the wurtzite structure.

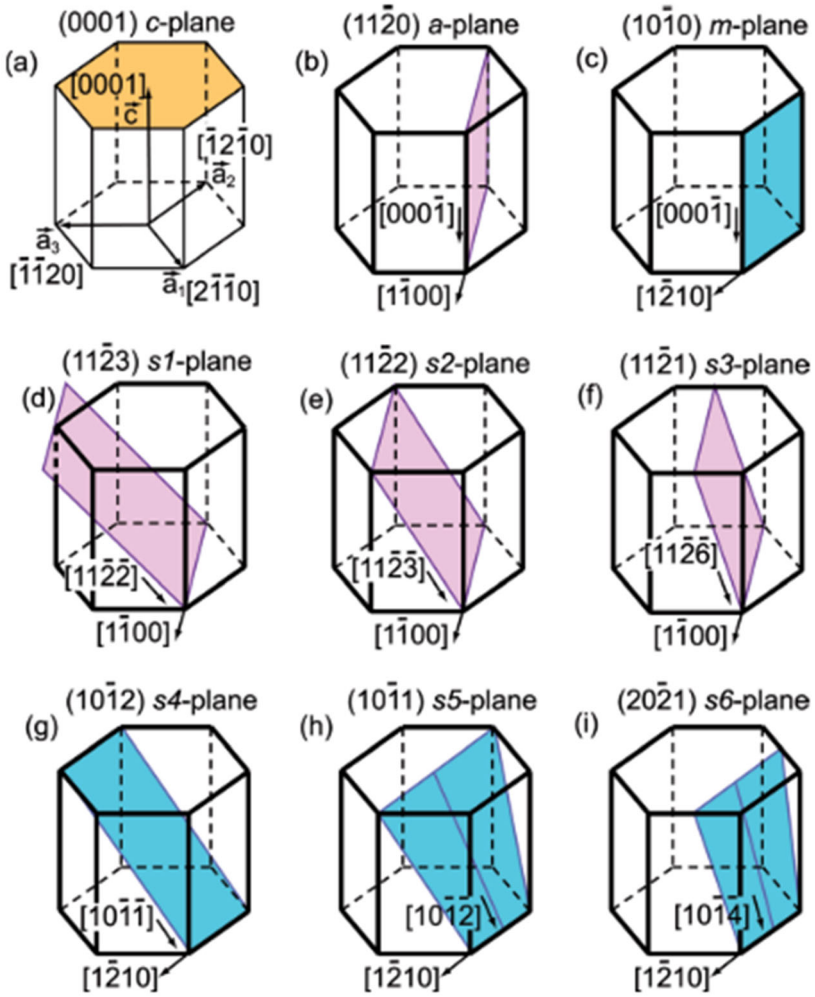

Figure 3-1. Schematics of typical crystallographic planes in the GaN wurtzite structure, reproduced from [10], with the permission from the publisher.

The anisotropic wet etching of semiconductors is widely used in the silicon industry to obtain the specific crystal plane orientations [11], [12], [13], [14] because the etching rate of different crystal planes is different, and consequently different planes are revealed. However, the wet etching of GaN is not as simple as silicon wet etching. Since the majority of GaN devices are grown on the (0001) c-plane direction, the earlier reports focused on the Ga-face c-plane polar (0001) GaN wet etching [15], [16], [17]. The wet etching of the GaN using potassium hydroxide (KOH) can be expressed in Eq. (3-1) and it involves the oxidation of GaN and dissolution of Ga_2O_3 [17], as shown in Fig. 3-2. In the c-plane GaN etching, hydroxide ions (OH^-) first attacks Ga atoms. The GaN then gets oxidized and dissolved to expose the N

atom. However, the N atom with three dangling bonds is repellent to the incoming OH^-, which leads to the difficulty of the further underlying Ga oxidation and the etch stops. Thus, the c-plane GaN is highly inert to the wet etchant with a very low etch rate of < 0.001 μm/min reported [15].

$$2GaN + 3\,H_2O \xrightarrow{KOH} Ga_2O_3 + NH_3 \qquad (3\text{-}1)$$

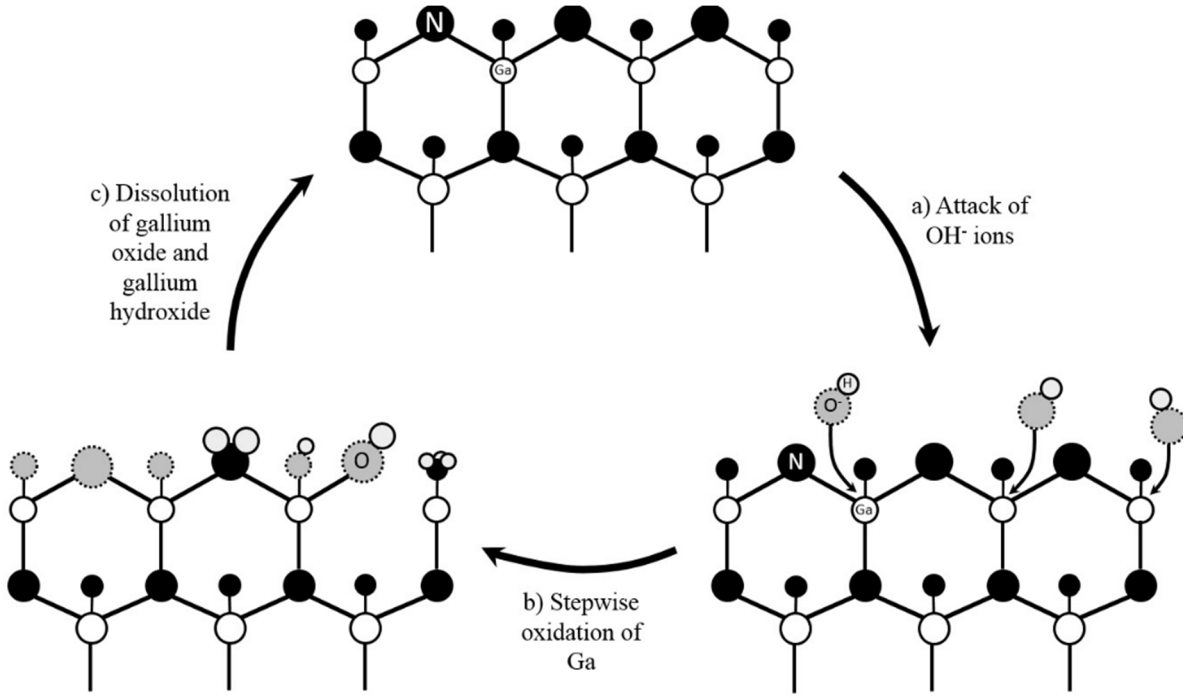

Figure 3-2. Wet etching cycle of GaN, reproduced from [17], with the permission from the publisher.

On the other hand, in the semi-polar GaN such as (11-22) GaN, the N-dangling bond is reduced compared to the c-plane, allowing the Ga to be more easily attached by the hydroxide-based wet etchant and thus the bulk GaN to be more easily etched. [18], [19]. In the growth direction of [11-22], the (0001) c-plane and (11-20) a-plane are inside the bulk semi-polar (11-22) GaN, as shown in Fig. 3-3. It has been reported that the c-plane and a-plane has the highest difficulty degree of etching compared to the other GaN planes [20]. These properties provide a path for

the crystallographic etching of semi-polar GaN for the vertical trench formation to selectively reveal the c- and a- planes GaN.

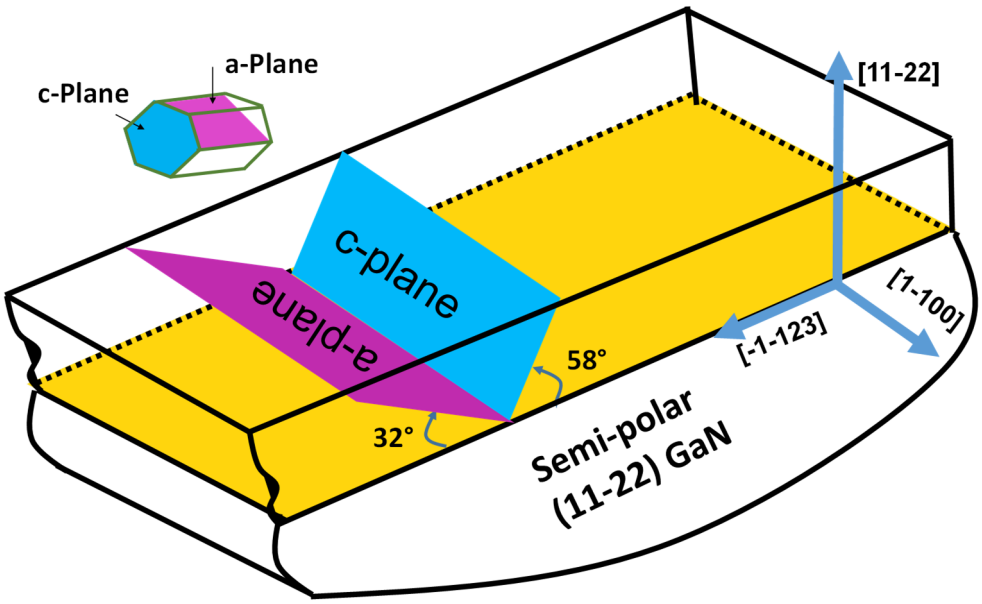

Figure 3-3. Schematics of semi-polar (11-22) GaN layer with highlighted c-plane and a-plane inside the bulk semi-polar (11-22) GaN.

3.2.2 Crystallographic Wet Etching of Semi-Polar (11-22) GaN

The semi-polar (11-22) GaN sample in this study was grown on m-plane sapphire substrate by metal organic chemical vapour deposition (MOCVD). The wafer epitaxy structures, were: 0.25 μm n^+-GaN (Si: ~ 5×10^{18} cm^{-3}), 0.5 μm p^+-GaN (Mg: ~ 1×10^{19} cm^{-3}), 3.0 μm n^--GaN (Si: ~ 5×10^{17} cm^{-3}), and 0.5 μm n^+-GaN (Si: ~ 5×10^{18} cm^{-3}), shown in Fig 3-4 (a). The top n^+-GaN and bottom n^+-GaN are for the drain and source ohmic contact. The p^+-GaN is to serve as the current blocking layer as well as to form the inversion MOS channel for the ON-state, and the n^--GaN drift layer is to sustain OFF-state high electrical field. The SiN_x was deposited by inductively couple plasma chemical vapour deposition (ICPCVD) and the wet etching trench opening windows was patterned by optical photolithography. The opening windows are aligned

to [1-100] and [-1-123] orientations, as shown in Fig. 3-4 (b) in order to reveal c-plane and a-plane on the sidewalls of the trench after the wet-etching process. Subsequently, the SiN_x were etched away by reactive ion etching (RIE).

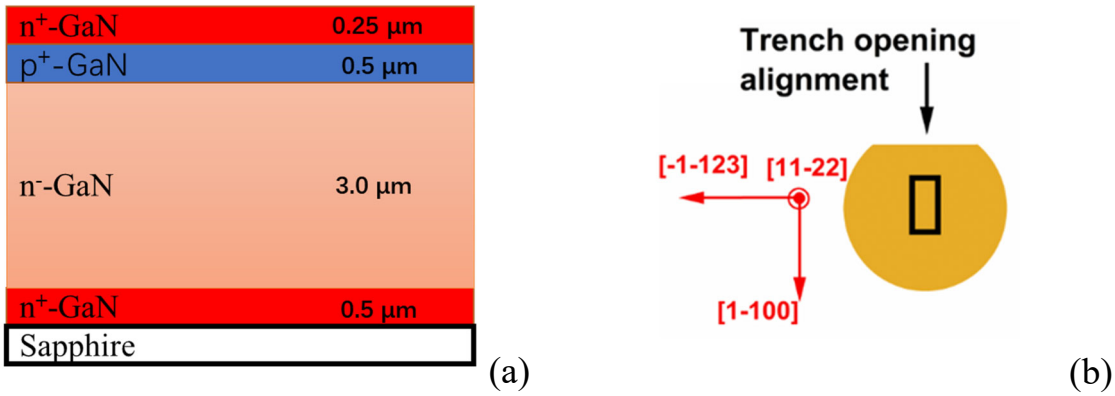

Figure 3-4. (a) Wafer epitaxy structure and (b) Wet etching trench opening alignment.

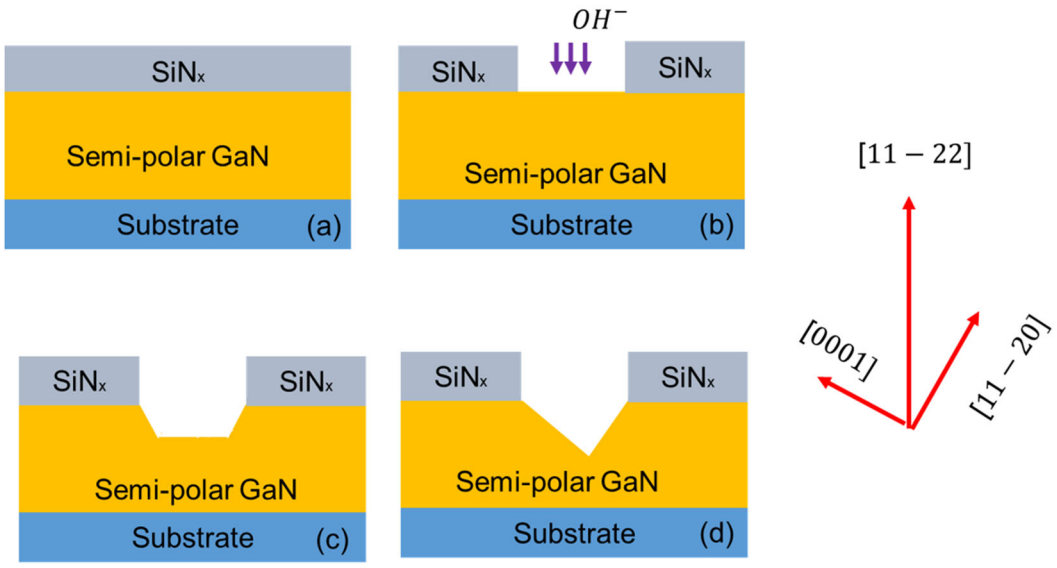

Figure 3-5. Cross-sectional schematics of step-by-step semi-polar (11-22) GaN etching process.

In this study, 30 M KOH solution at ~ 95 ℃ was used for etching the (11-22) GaN sample. 30 M KOH was selected for the wet etching because this is the highest achievable concentration in the aqueous solution. The etching mechanism of semi-polar GaN is illustrated in the Fig. 3-5. At the beginning of the etching process, the OH^- ions from KOH react with the surface GaN atoms of the exposed (11-22) GaN (the area without the SiN_x hard mask) and the surface of the GaN is

etched along the - [11-22] direction from the top [18] , as illustrated in Fig. 3-5 (b). As the etching continues, lateral etch on GaN toward the sidewall of the trench will commence until the chemically stable planes with a slower etch rate than that of the (11-22) plane such as c-plane and a-plane [20] are revealed at the sidewalls as shown in Fig. 3-5 (c) and (d).

From the etching trials, the etch rate of semi-polar (11-22) n-GaN and p-GaN was estimated to be ~ 98 nm/min and ~13 nm/min, respectively. The slower etch rate of the p-GaN compared to the n-GaN is due to the strong repulsion of OH- due to the p-type doping [21].

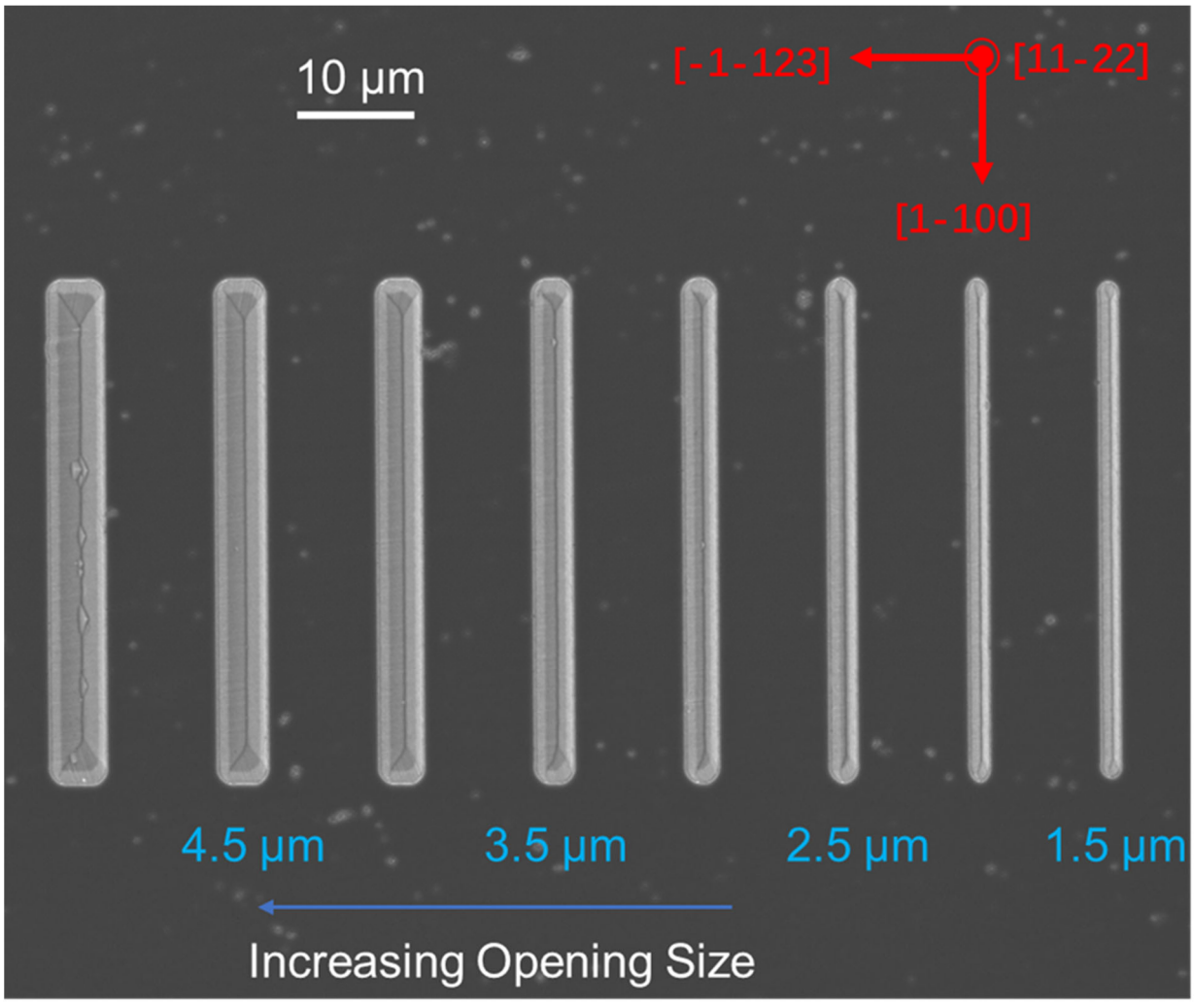

Figure 3-6. SEM image of wet-etched trenches with differenct trench opening sizes on the semi-polar (11-22) GaN.

The SEM image of the wet etched trenches with different trench opening sizes (trench width: 50 µm and trench length: 1.5 µm to 5.5 µm) is illustrated in the Fig. 3-6. The total etching time was ~ 85 minutes. For the small opening (<4.5 µm), V-groove structure was fully revealed. For the larger opening such as 5 µm trench length, trigonal prism cells with two m-plane and c-plane are also observed in the bottom of the trench.

Fig. 3-7 shows a typical SEM image of partially etched V-groove trench with illustrated different GaN planes. A tilted SEM image is shown in Fig. 3-8, confirmed the double m-plane angle of 120° in a GaN wurtzite crystal structure. The double m-planes and a-planes are having the same direction along [11-20] orientation in the GaN wurtzite crystal structure. These double m-planes disappear with increase of etching time, resulting the a-plane (11-20) sidewall formation. The observed results are consistent with the increasing theoretical predicted difficulty of crystal facet etching of (i.e. c-plane > a-plane > m-plane) [20]. A smooth V-groove sidewalls are revealed with a sufficiently long etching time as shown in Fig. 3-9.

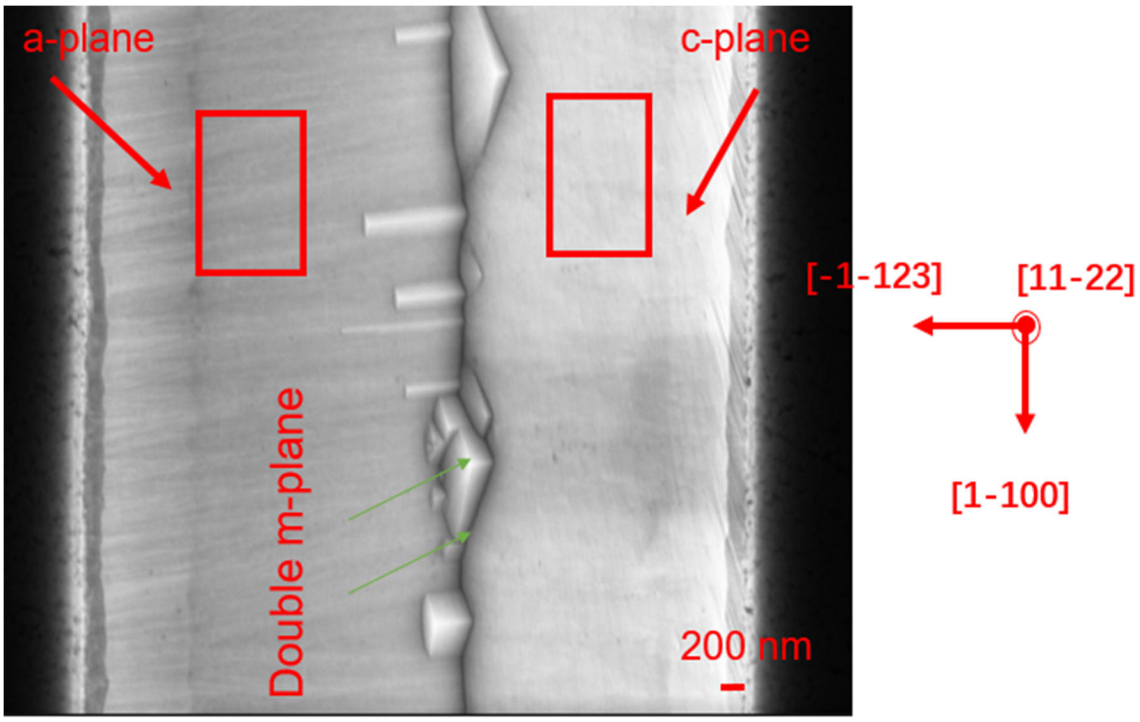

Figure 3-7. Partially wet-etched V-groove trench.

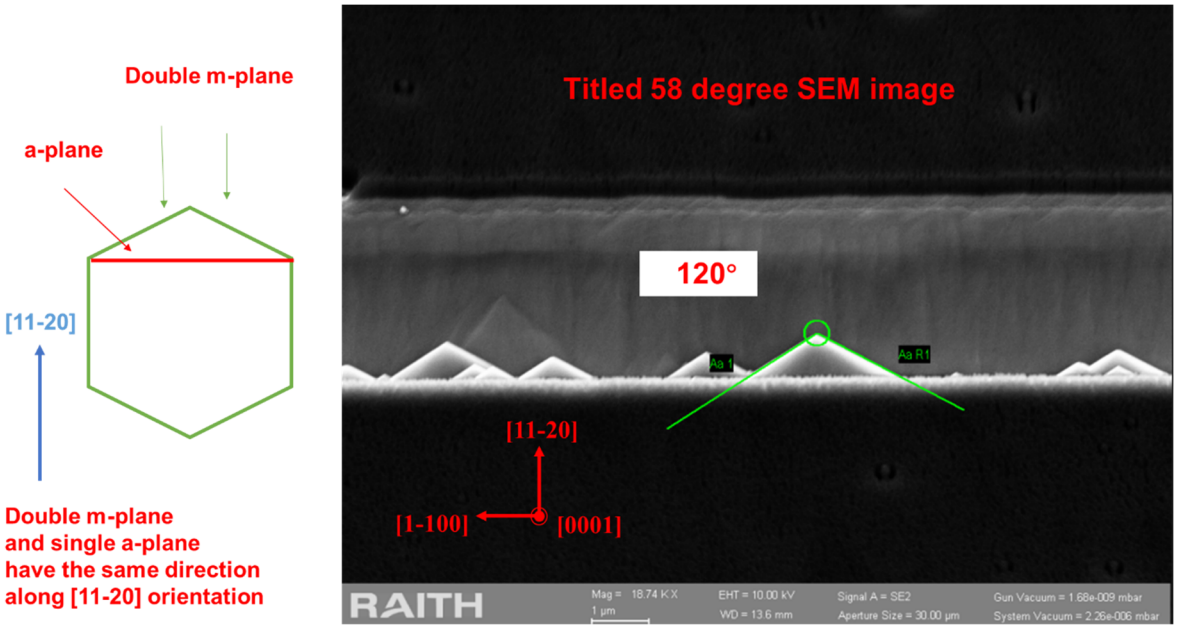

Figure 3-8. SEM image taken with the sample titled at angle of 58°.

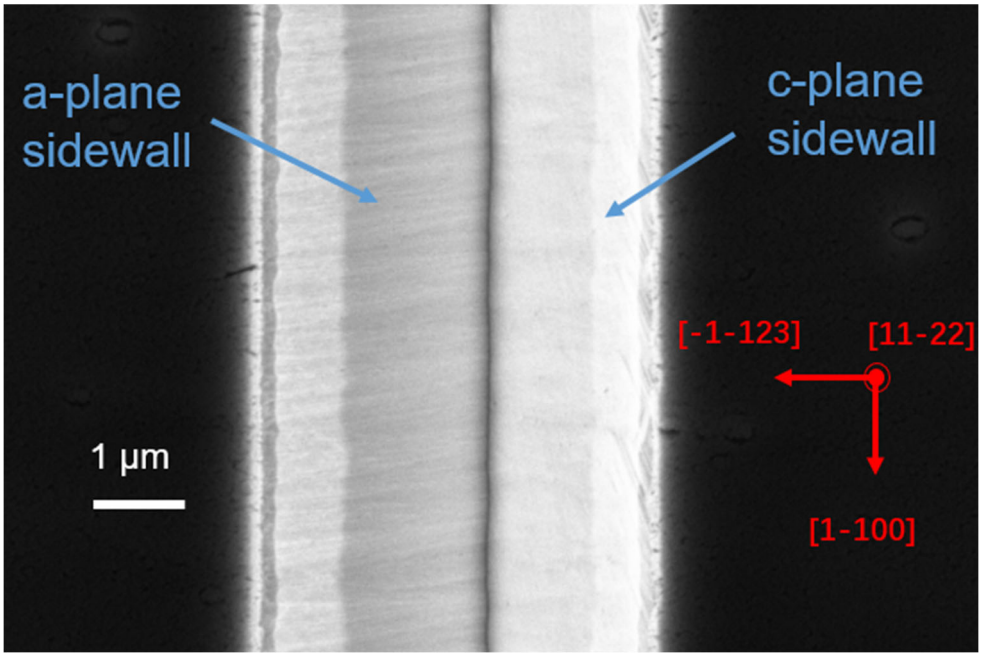

Figure 3-9. Fully etching V-groove trench.

3.3.3 The choice of Trench Opening Size (trench length)

In order to achieve an optimum electrical performance of the trench MOSFETs, the trench depth is critical. To ensure current flow between the source and drain terminals at ON-state via the gate-modulated MOS-channel, the trench should be etched beyond the p-type GaN electron blocking layer into the n^--GaN drift region. For the trench formation using the conventional dry plasma-etching techniques in the polar GaN, the desired trench depth can be adjusted by tailoring the plasma etching conditions, such as plasma etching power and time.

For achieving a higher current density with a specific opening trench, the smaller trench opening length is preferred. In the case of crystallographic wet etching trench opening technique in the semi-polar GaN, the depth of the trench is linked to the length of the trench opening. This is due to the sloped-nature and plane orientations of the trench sidewalls. As discussed in Section 3.2.2, once the apex is formed at the bottom at the trench, the vertical etching of the trench will slow and stop due to the presence of the slow etch rate of the c-plane and a-plane GaN.

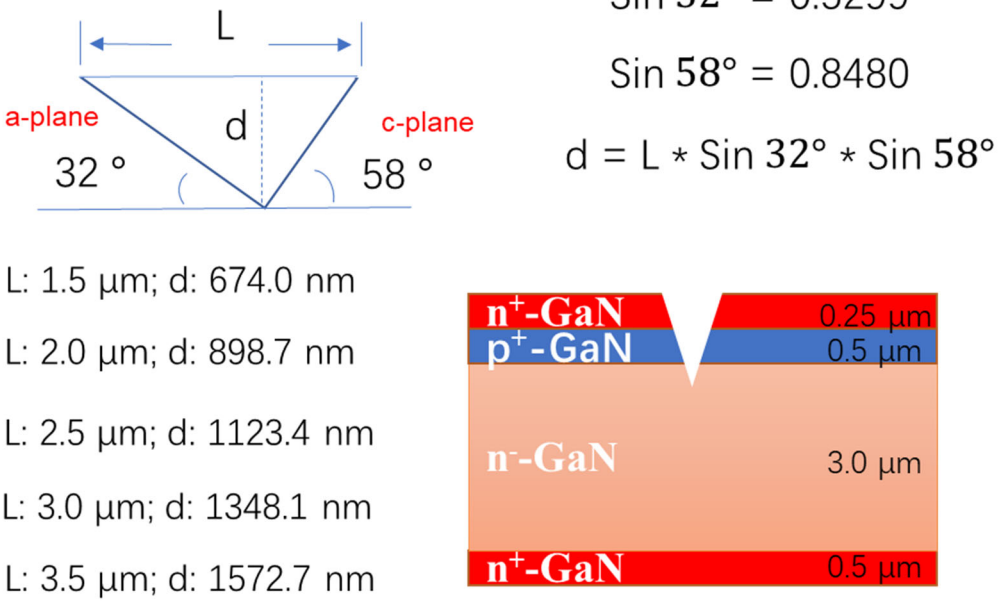

Figure 3-10. Wet-etch trench depth (d) estimations with varying trench opening (L).

In this work, the total thickness of the n^+-GaN and the buried p^+-GaN layers was ~750 nm. Using the theoretical slope angle of the c-plane and a-plane with respect to the (11-22) GaN, the trench depth with varying trench opening length was calculated as shown in Fig. 3-10. It is found that an opening length of 1.5 µm is not enough to penetrate the pGaN region. A widen length is required in order to fully recess the p-GaN layer in the trench region. 2 µm is theoretically sufficient to penetrate the drift region. However, a slightly wider opening length of 2.5 µm is suggested to considering the possible Mg-back diffusion effect into the drift region.

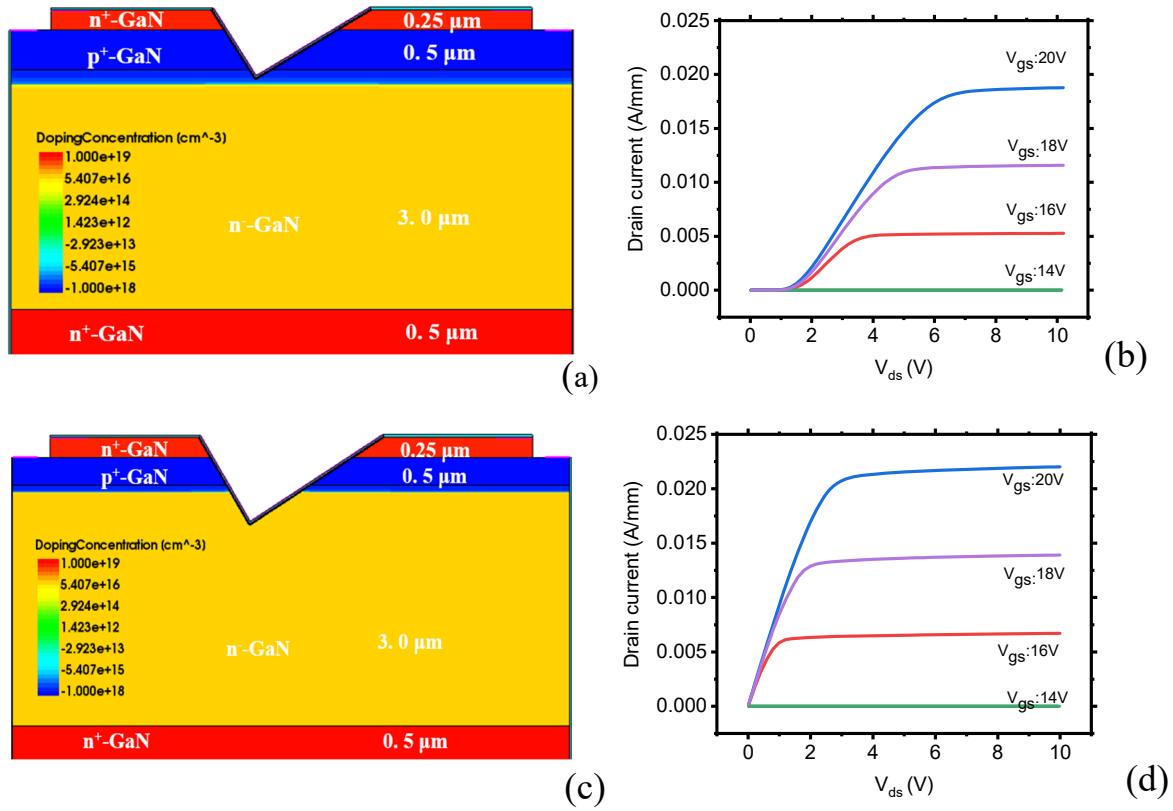

Figure 3-11 (a) TCAD simulated V-groove MOSFET with a 2.0 µm trench length device and (b) the corresponding simulated I-V characteristics. (c) TCAD simulated V-groove MOSFET with a 2.5 µm trench length device and (d) the corresponding simulated I-V characteristics. Note: the simulation is for the investigation of effect of the trench depth on the MOSFET output characteristics only, the simulated channel mobility and bulk mobility parameters are not optimized.

Fig. 3-11 (a) and (b) show the Sentaurus TCAD simulated Vertical V-groove semi-polar GaN MOSFETs with graded 200 nm Mg-back diffusion profile. It is noted that a non-linear off-set is observed in the simulated ON-state output characteristics of the MOSFETs with the p-GaN layer is not fully recessed. The observed off-set in the output characteristics is due to a barrier existing in the vertical channel for the electrons in the p-GaN layer, additional drain voltage is required to overcome this barrier. On the other hand, the off-set in the simulated ON-state output characteristics is not observed for the MOSFET with the fully recessed p-GaN layer as illustrated in Fig. 3.11 (c) and (d).

A wider L, on the other hand, will cause the bottom of V-groove to be too close to the bottom n^+-GaN as the trench depth increases. This will lead to a reduced effective distance between the bottom of the V-groove and the drain of the MOSFETs on the bottom n^+-GaN layer, resulting an increased electric field crowding at the transistor's OFF-state and hence it is not in favor for the breakdown of the MOSFETs at off-state. In this project, a trench length of 2.5 μm is recommended for the fabrication of a 3-terminal device for the specific wafer structure of n^+-GaN/p^+-GaN/n^--GaN/n^+-GaN (0.25 μm/0.5 μm/3.0 μm/0.5 μm) shown in Fig 3-10.

3.3 Fabrication of Semi-polar GaN V-groove MOSFETs

3.3.1 Three-terminal V-groove MOSFET Device Fabrications

Following the establishment of the wet-etching process, 3-terminal V-groove MOSFETs are fabricated. Fig 3-12. depicts the device fabrication process flow. Firstly, SiN_x were deposited on the sample as a hard mask using ICPCVD. Wet-etching windows which aligned to [1-100] and [-1-123] orientations as shown in Fig 3-4. were opened on the SiN_x hard mask using ICP.

Here, a trench opening length of 2.5 μm is used for the fabrication of the V-groove MOSFETs to ensure the p-GaN layer is fully wet-etched as discussed in Section 3.3.1.

For the V-groove trench formation, the crystallographic wet etching method described in section 3.2. (Fig. 3-12. b) is used and the total wet etching time was ~ 50 minutes. After the wet-etch process, the samples were treated in 40% hydrofluoric acid for 15 minutes to remove the remaining SiN_x hard mask. The sample was then transferred to plasma enhanced chemical vapour deposition (PECVD) chamber for the 60 nm gate dielectric SiO_2 deposition at 300 °C.

Following that, inductively couple plasma etchings were performed to access the top n^+-GaN to remove the SiO_2 on the contact region. Further dry-etching steps using inductively couple plasma etching technique were performed to access to the buried p^+-GaN layer with an etch depth of ~300 nm and to the bottom n^+-GaN layer with an etch depth of ~3000 nm. The sample was then annealed in N_2 at 500 ℃ to recover the plasma induced damage as well as in attempt to activate the p^+-GaN layer. The thermal annealing budget was constrained by the gate dielectric deposition temperature. Thermal evaporation was used to deposit the n-type ohmic metal stacks of Ti/Al/Ni/Au (20 nm/ 120 nm/ 20 nm/40 nm) on both top and bottom n^+-GaN. Pd/Ni/Au (20 nm/ 20 nm/ 200 nm) metal stacks were also deposited using thermal evaporation on the p^+-GaN surface. Following the metal depositions, the sample was annealed in N_2 for 10 minutes at 400 ℃ to form the ohmic contacts on the n^+-GaN and p^+-GaN. After the annealing step, Ni/Au (20 nm/200 nm) gate metal stacks were deposited.

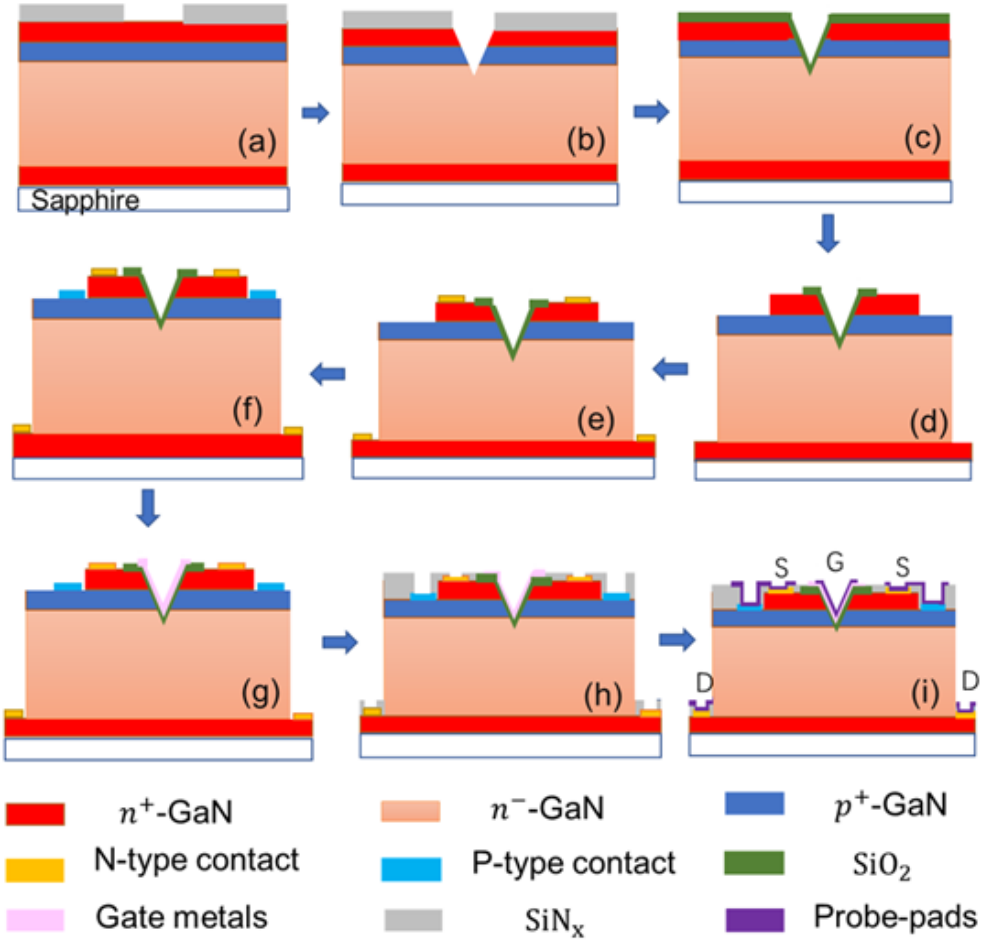

Figure 3-12. Fabrication sequence of the semi-polar V-groove MOSFET.

A 300 nm bi-layer SiN_x was subsequently deposited using the ICPCVD and PECVD to serve as passivation layer. Finally, via opening on the SiN_x passivation was performed using RIE to access the contacts and the probe pad metal of Ni/Au (20 nm/ 200 nm) was deposited to complete the device fabrication. The detailed step-by-step process traveller is also provided in the Appendix A. Fig 3-13 depicts the schematic diagram and top view SEM image for the fabricated V-groove MOSFET in this study.

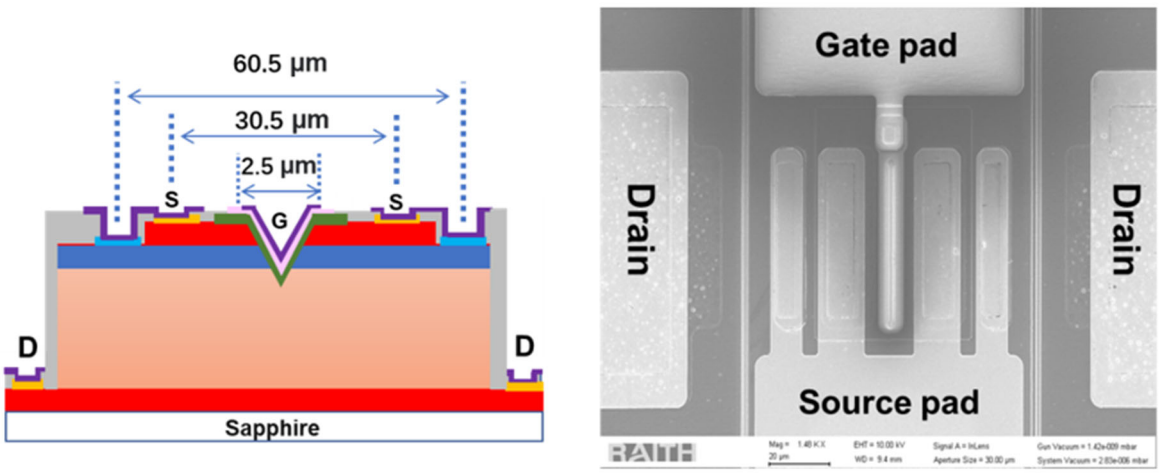

Figure 3-13. Device schematic and top-view SEM image.

3.3.2 Structural Analysis

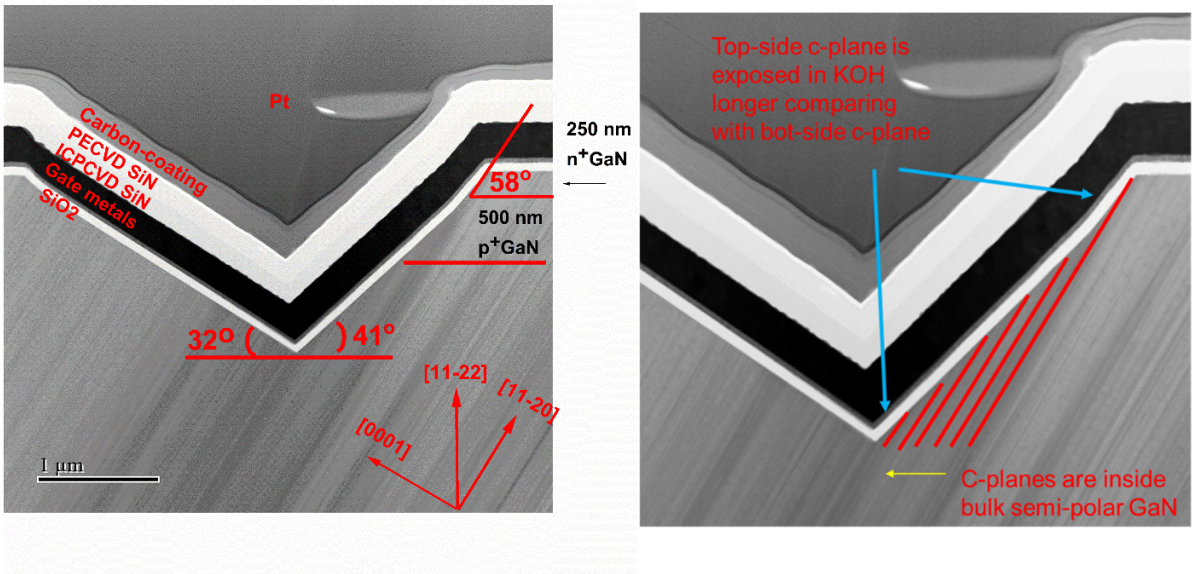

Figure 3-14. Cross-sectional scanning transmission electron microscopy (STEM) image of the wet-etched trench of the V-groove MOSFET.

Fig. 3-14 shows a cross-sectional STEM image of the wet-etched trench of the V-groove MOSFET. A sharp interface is observed between the SiO_2 gate dielectric and the wet-etched GaN sidewalls. An angle of 32° was measured on the left side of the V-groove trench,

corresponding to [11-20] a-plane direction. An angle of 58° was measured on the top n^+-GaN layer on the right side of the V-groove trench and deviated to 41° toward the bottom of the trench.

The difference in the sidewall slope is primarily due to the bottom GaN sidewall's shorter exposure time to KOH solution than that of the top GaN layer. The top n-type GaN layer was exposed to KOH first, and it was fully etched along -[11-22] within three minutes at a ~98 nm/min etch rate. Once the top n^+-GaN has been fully etched, the p^+-GaN is exposed to KOH and the p-type GaN etching process begins. As discussed in Section 3.2.2., the etch rate of the p^+-GaN layer is 13 nm/min, which is significantly slower than that of the n-GaN layer due to accumulation of electrons at the p^+-GaN surface caused by surface band bending [21]. In order to fully etch the 500 nm p^+-GaN layer, an etching time of ~40 minutes are required. A further 8 minutes etching time was used to etch 800 nm of the bottom n-GaN drift layer along -[11-22].

In comparison to the top n^+-GaN sidewall, which was exposed to KOH for >40 minutes, the bottom GaN sidewall was only exposed to KOH for 8 minutes, which was insufficient to fully reveal the c-plane with a slope angle of 58°. The c-planes are inside the bulk semi-polar GaN, as shown in Fig. 3-14 (b). A longer etching time is required to allow lateral etching of the sidewall c-planes to reveal the single c-plane with angle of 58° in order to achieve the same sidewall slope for the bottom n^--GaN. This can be achieved with a thicker SiN_x hard mask for the longer wet etching on the GaN layers.

In addition, using a higher molar concentration of hydroxide-based solution (60 M NaOH at 95 °C), a single 58° slope along the $n^+/p^+/n^-$ GaN sidewall was observed in the preliminary

studies. This is due to higher concentrations of OH- allowing for a faster etch rate along the sidewall direction in the p^+-GaN and bottom n^--GaN layers.

3.4 Device Electrical Characterizations

3.4.1 Ohmic Contact Characterizations

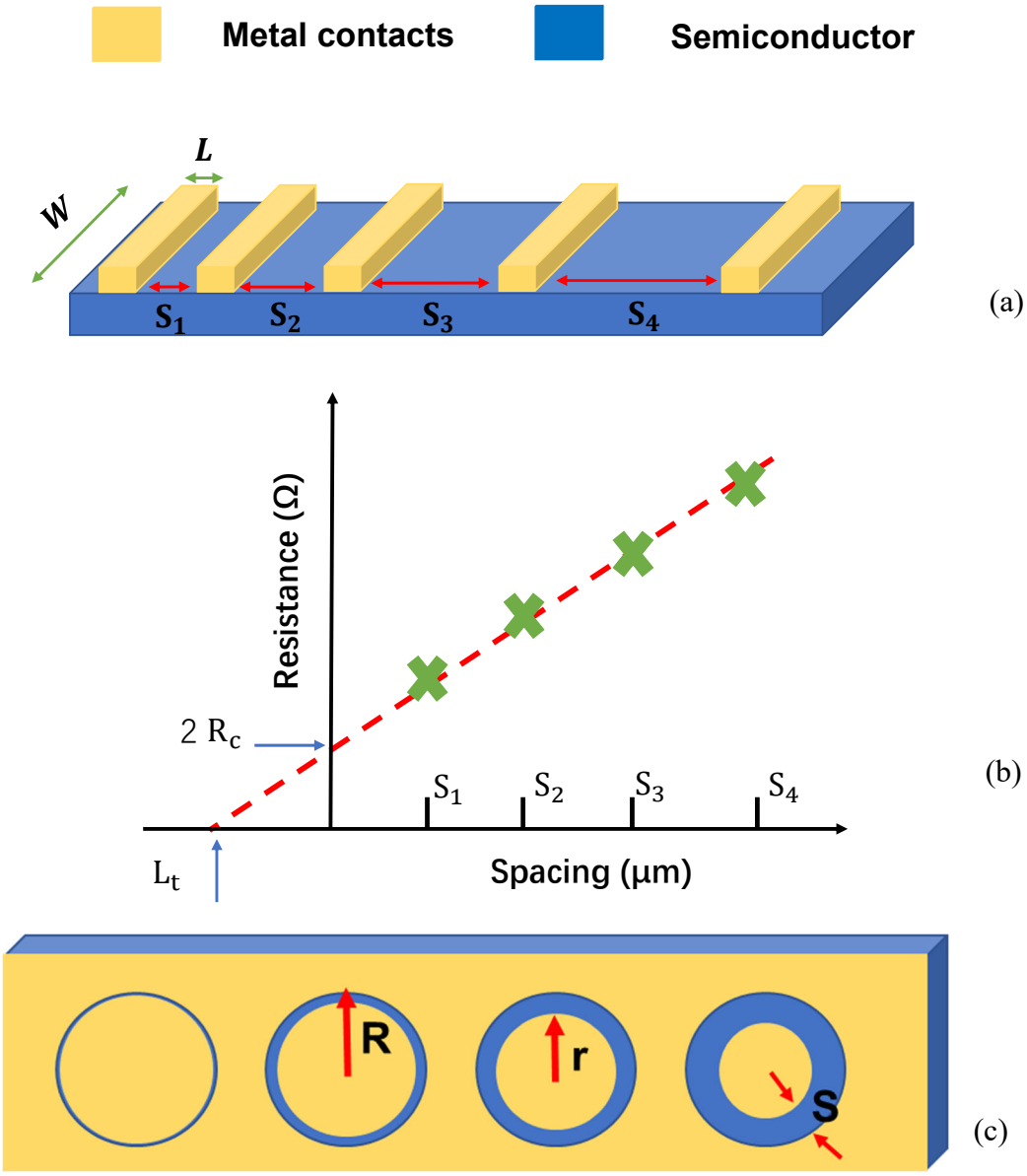

Figure 3-15. (a) linear TLM pattern (b) linear relationship between measured resistance and gap spacing and (c) circular TLM pattern.

The first step of device characterization was to extract the sheet resistance (R_{sh}) and contact resistance (R_c) of the GaN layers by using linear transmission line method (LTLM) or circular transmission line method (CTLM) structures. The typical LTLM contact pads have a length (L) of 100 μm and a width (W) of 125 μm, with different gap spacing ranging from 2 μm to 25 μm, as shown in Fig. 3-15. (a). Fig. 3-15. (b) depicts the relationship between the total resistance (R_T) and the gap spacing (S) with the following relationships:

$$\text{Slope} = R_{sh}/\text{W} \tag{3-2}$$

$$R_{sh} = \text{Slope} \times \text{W} \ [\Omega/\text{sq}] \tag{3-3}$$

$$\text{Contact resistivity, } \boldsymbol{\rho}_c = R_{sh} \times L_t^2 \tag{3-4}$$

The R_{sh} can be extracted from Eq. 3-2 and R_c can be obtained by the half of y-axis intercept. The LTLM will be used for lateral device in chapter 5.

CTLM is used in this section to characterise the top n^+-GaN layer, the buried p^+-GaN layer, the n^--GaN drift layer and the bottom n^+-GaN layer. This method shares the same principle of LTLM, but R_T and S are not a linear relationship and R_T and S can be determined by fitting the values of R_{sh} and L_T using the Eq. below:[22]

$$\mathrm{R}_T = \frac{\mathrm{R}_{sh}}{2\pi}\left[\ln\frac{\mathrm{R}_0}{\mathrm{R}_0 - \mathrm{S}} + \mathrm{L}_T\left(\frac{1}{\mathrm{R}_0 - \mathrm{S}} + \frac{1}{\mathrm{R}_0}\right)\right] \tag{3-5}$$

where R_T is the total resistance, R_0 is the radius (100 μm) of the outer circular contact, S is the gap spacing from 10 μm to 35 μm and R_{sh} is the sheet resistance. R_c is calculated from the half of y-axis intercept multiply by $W_c=2\pi R_0$ with the unit of Ω.mm. Fig. 3-16 and 3-17 shows the measured CTLM characteristics of top n^+-GaN and bot n^+-GaN. The non-ideal IV relationship was due to the low thermal annealing temperature of 400 ℃. The extracted sheet resistance, R_{sh}

of the top n^+-GaN and bottom n^+-GaN layers were between ~116 Ω/sq and ~141 Ω/sq, respectively as shown in Figs. 3-16 and 3-17. The extracted contact resistance, R_c of the ohmic contacts for the top n^+-GaN and bottom n^+-GaN layers was ~5.7 Ω.mm and ~5.1 Ω.mm, respectively. Both R_{sh} and R_c for n-type ohmic contacts are extracted at 0.1 V.

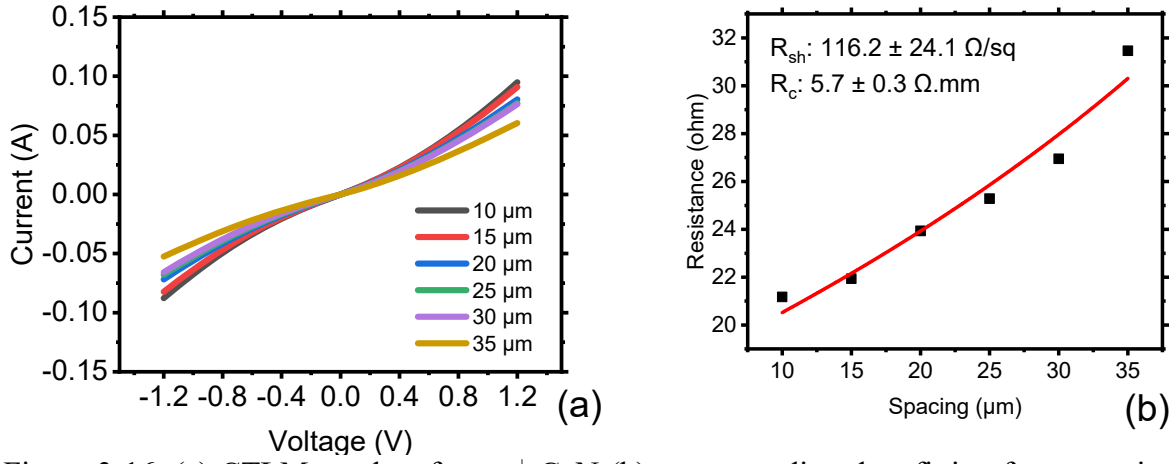

Figure 3-16. (a) CTLM results of top n^+-GaN (b) corresponding data fitting for extraction R_{sh} and R_c.

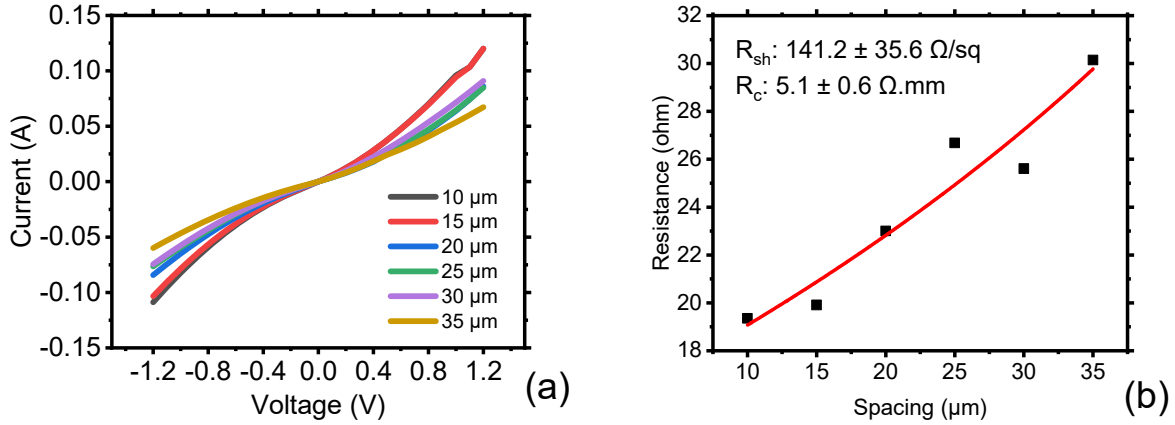

Figure 3-17. (a) CTLM results of bot n^+-GaN (b) corresponding data fitting for extraction R_{sh} and R_c.

For the buried p^+-GaN, a rectifying behaviour was observed, Fig. 3-18. The R_{sh} and R_c were ~1.7×10^6 Ω/sq and ~1.6×10^4 Ω.mm, extracted at 10 V. For the optimisation of the p^+-GaN contacts, other metallisation schemes such as Ni/Au (20 nm/ 20 nm) and Pd/Ni/Au (20 nm/20 nm/20 nm), as shown Fig. 3-19, were also carried out in the testing trials. The trial samples

were annealing at 800 °C for 20 minutes in attempt to increase the Mg-acceptor activations in the buried p^+-GaN. An improved current level of about one order of magnitude was observed. However, the rectifying behaviour of the p^+-GaN contacts does not change. It is believed that the difficulty in obtaining p-type ohmic contacts were primarily due to the low hole concentration in the buried p-type layer as a result of insufficient Mg activation. In addition, plasma induced damage during the dry etching step to access the buried p^+-GaN layer, resulting in introduction of the N-vacancy to compensate Mg acceptors may also contribute to the difficulty in achieving good p-type ohmic contacts. Adapting Mg-post diffusion technique [23] and introducing a KOH wet-etching approach to access the buried p^+-GaN may bring more insights on the improvement of the p-type ohmic contacts.

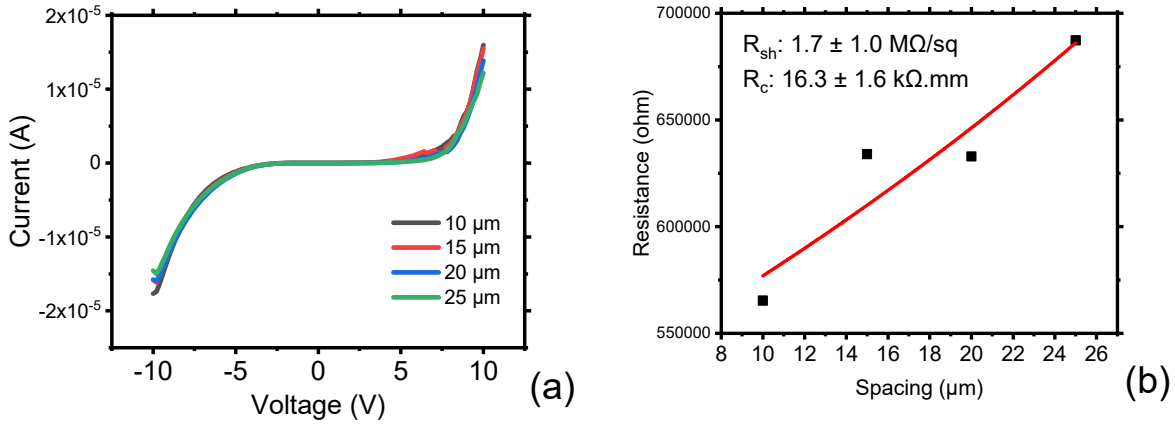

Figure 3-18. (a) CTLM results of buried p^+-GaN (b) corresponding data fitting for extraction R_{sh} and R_c.

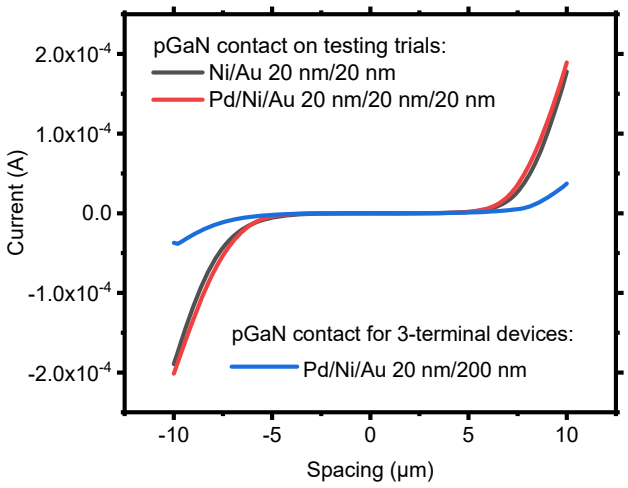

Figure 3.19. p-type ohmic contact characteristics with different metallisation schemes.

3.4.2 Three-terminal V-groove MOSFET Output Characteristics

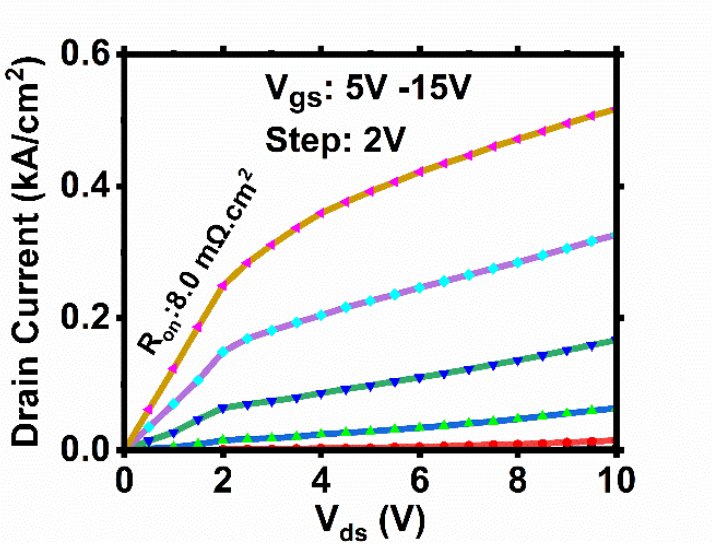

Figure 3.20. The output characteristics of the V-groove MOSFET with a 2.5 μm trench length opening.

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Fig. 3.20 demonstrates the output characteristics of the 3-terminal V-groove GaN MOSFETs. The current was normalized to the active area of 5.5 μm * 53 μm = 291.5 μm^2, taking account the current spreading of 3 μm drift region thickness. This method is widely used and reported in [24], [25], [26], [27], [28] on the quasi-vertical GaN MOSFETs. The MOSFET exhibits an output

current density of 516 A/cm^2 at V_{ds} =10 V and V_{gs} =15 V. The on-state resistance (R_{on}) extracted from the linear region of the output characteristics was 8.0 mΩ.cm^2. At a higher drain bias, it was observed that the drain current does not saturate with increasing of the drain bias. This may indicate a low hole concentration in the buried p^+-GaN layer due to a low activation efficiency of Mg p-type dopant. In the future, optimisation techniques such as improving Mg activation of the p^+-GaN, introducing a thicker p^+-GaN layers, or lowering the n^--GaN drift region n-type doping concentration could be used [7].

Fig. 3-21 shows the demonstrates the output characteristics of the 3-terminal V-groove GaN MOSFET with a smaller trench length opening (1.5 µm). A non-linear behavior in the output characteristics is observed at V_{ds} below 1V. This in prediction with the TCAD simulated results described in Section 3.3.1 with the small trench length.

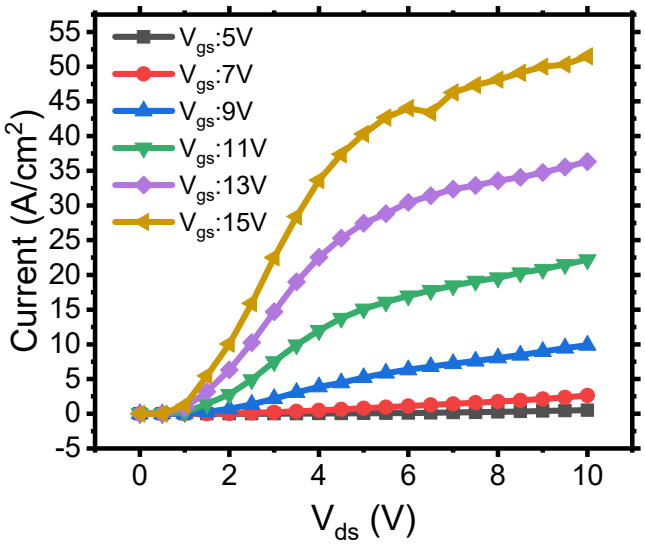

Figure 3-21. The output characteristics of the 3-terminal V-groove MOSFET with a 1.5 µm trench length opening.

3.4.3 Three-terminal Device Transfer Characteristics

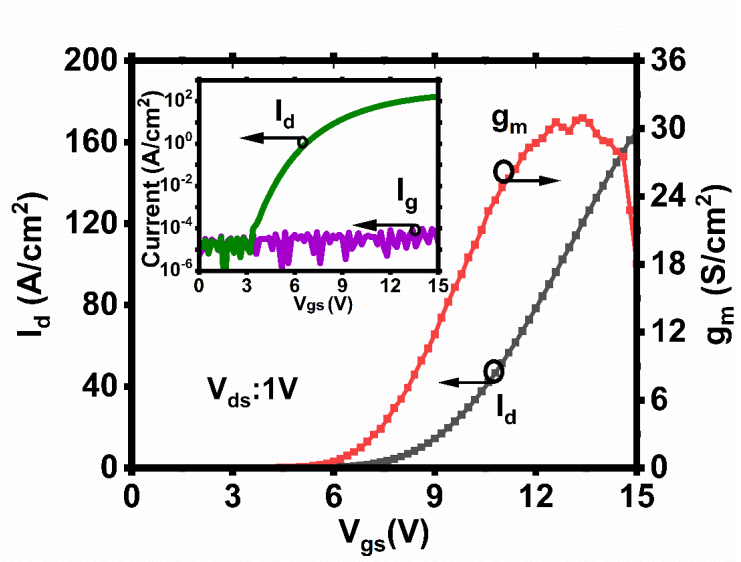

Figure 3-22. The gate transfer characteristics of the V-groove MOSFET.

Fig. 3-22 depicts the gate transfer characteristics in both the linear and log scales of the V-groove MOSFET at V_{ds} = 1 V. A threshold voltage of 9.49 V was extracted using the linear interpolation method from the peak transconductance (g_m) of 30.9 S/cm^2. The channel mobility of the MOSFET was extracted using Eq. 3-6 [29], [30],

$$I_{ds} = \frac{V_{ds}}{\frac{1}{\frac{W}{L} C_{ox}\mu_{CH}(V_{gs} - I_{ds}R_{GS} - V_{th})} + R_{other}} \quad (3\text{-}6)$$

where W is the gate width, L is the channel length, C_{ox} is the gate capacitance per unit area, μ_{CH} is channel mobility, I_{DS} is the drain current, R_{GS} is the gate to source resistance (source contact resistance + top n$^+$-GaN resistance), V_{th} is the threshold voltage and R_{other} is the series resistance that is independent of V_g (i.e. not modulated by gate) and composes of the source contact resistance, top n$^+$-GaN layer resistance, n$^-$-GaN drift layer resistance, bottom n$^+$-GaN layer resistance and drain contact resistance.

In the VMOSFET: R_{GS} = 0.2 mΩ.cm^2, estimated from the CTLM results, R_{other} = 2.6 mΩ.cm^2, extracted using the method described in [29], C_{ox} = 3.9 × 8.854 × 10^{-14} / 60 (nm) = 5.75x10^{-8}

(F/cm^2), L is defined by the effective channel length which takes into account the sidewall slope, ½ (0.5 µm/sin 32° + 0.5 µm/sin 41°) = 0.852 µm, where 0.5 µm is p^+-GaN thickness, W = 50 µm × 2 = 100 µm and V_{th} is defined from the linear-interpolation from the gate transfer characteristics, = 9.49 V.

The calculated channel mobility was 21.3 cm^2/Vs at V_{gs}=15 V and V_{ds} =1 V. A comparison of extracted mobility in this work with others' reported inversion channel is illustrated in the Table 3-1. It is observed that the extracted mobility of 21.3 cm^2/Vs in this work were comparable with reported mobility of 20 - 30 cm^2/Vs at a similar Mg doping level (1×10^{19} cm^{-3}) in the p-GaN layer. A further enhancement of the channel mobility can be optimised by the AlGaN /GaN channel re-growth with a two-dimensional electron gas channel on the trench sidewall [31].

Table 3-1. Vertical GaN Trench MOSFET Channel Mobility Comparison

Affiliation	Substrate	Mg doping (cm^{-3})	Mobility (cm^2/Vs)
ROHM [30]	GaN	4×10^{19}	131
UCSB [24]	Sapphire	3×10^{19}	7 - 10
UCSB [32]	Sapphire	3×10^{19}	5 - 10
EPFL [33]	Silicon	4×10^{19}	17.8
EPFL [26]	Silicon	2×10^{19}	21 - 41
HKUST [34]	Sapphire	3×10^{19}	4.7
HKUST [34]	Sapphire	1.2×10^{19}	25.2
HKUST [25]	Sapphire	1.2×10^{19}	30 - 57
This work	Sapphire	1.2×10^{19}	21.3

In addition to the mobility extraction by using Eq. 3-6, Level 3 MOSFET model from SPICE simulator is also used to extract the mobility, taking the body effect into account. The Level 3

model [35] can be expressed by Eq. 3-7. Using the methods described in [35], the values for theses fitting parameters are extracted and illustrated in Fig. 3-23. The fitted curve shows a matched gate transfer characteristic.

$$I_D = \frac{\boldsymbol{KP}}{1 + \boldsymbol{Theta}\,(\mathrm{Vgs} - \mathrm{Vto})} \frac{\mathrm{W}}{\mathrm{L}} (V_{GS} - V_{to})(V_{DS} - R_S I_D - R_d I_D) - \left[1 + \frac{\boldsymbol{Gamma}}{2\sqrt{\boldsymbol{Phi}}}\right] \left(\frac{(V_{DS} - R_S I_D - R_d I_D)^2}{2}\right) \quad (3\text{-}7)$$

where KP is transconductance parameter, Theta is the mobility modulation constant that models the effect of V_{gs} on the mobility [49], R_s is source resistance, R_d is drain resistance, Gamma is the body-effect parameter, phi is the surface potential in strong inversion, Vto is the threshold voltage, W and L are the channel length and width, respectively.

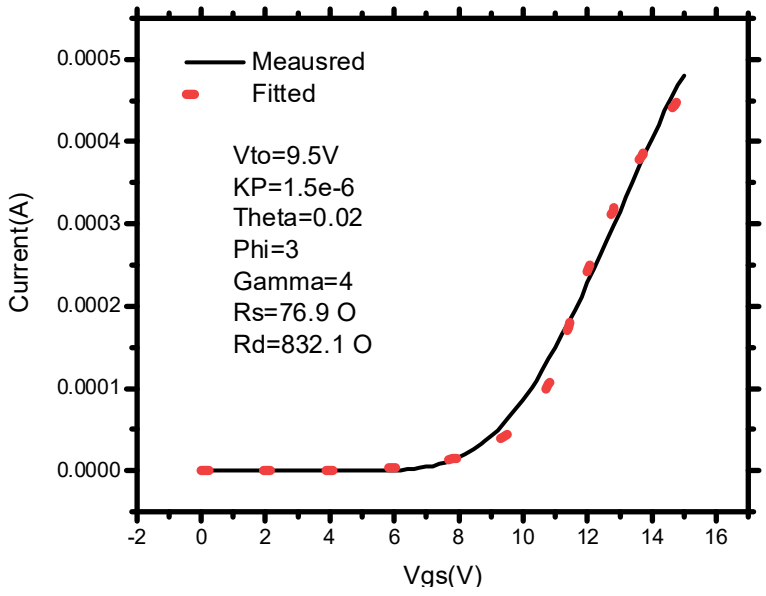

Figure 3-23. Simulated gate transfer characteristics using Level 3 MOSFET model in the LTSPICE.

Figure 3-23. shows the simulated gate transfer using Level 3 MOSFET model in the LTSPICE simulation program. Based on the simulated KP value, the mobility of ~23 cm^2/Vs at Vgs=15V is calculated, which is consistent with the mobility value extracted using Eq (3-6).

The body effect in the MOSFETs can be described using the gamma parameter from the Level 3 MOSFET model and is given by:

$$Gamma = \frac{\sqrt{2q\varepsilon N_A}}{C_{ox}} \quad (3\text{-}8)$$

where q is electric charge, ε is permittivity in GaN, N_A is the carrier concentration in the channel and C_{ox} is the gate capacitance per unit area. Based on the simulated gamma parameter of $4V^{-1}$ and from Eq. 3-8, the hole concentration in the p-GaN layer was estimated to be ~$2x10^{17}$ cm^{-3}, which corresponds to a 2% ionisation and activation ratio with the Mg doping concentration of $1x10^{19}$ cm^{-3}. The 2% ionised Mg acceptors are close to the typical reported ionised acceptors of 1-10 % ratio at the room temperature [36], [37], [38].

3.4.4 Three-terminal Device Breakdown Characteristics

The OFF-state output characteristics at V_{gs} = 0 V of fabricated VMOSFET were demonstrated in the Fig. 3-24 with a gate hard breakdown voltage at ~ 150 V. The gate breakdown is the result of the V-groove sharp corner electric field crowding at the trench bottom [39]. The introduction of a thick bottom dielectric at the trench bottom [25] and the trench filling regrowth technique [40] are promising methods to flatten the sharp corner that have been suggested in the literature. These methods could be used in future VMOSFET improvements.

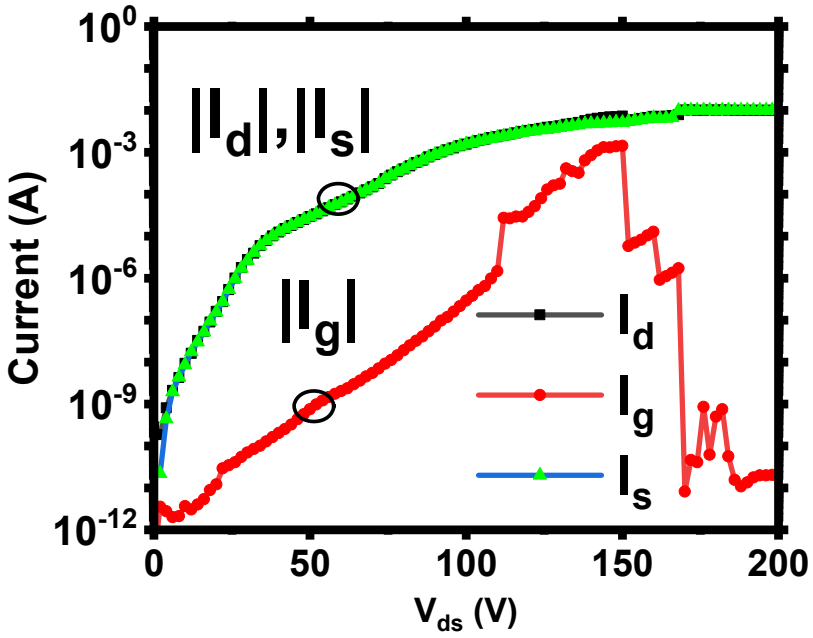

Figure 3-24. The off-state characteristics of the 3-terminal V-groove MOSFET at V_{gs}= 0 V.

On the other hand, it is noted that the off-state drain to source leakage current of the MOSFET is higher than the gate leakage current. The possible explanations for the observed high drain to source leakage current are as follow: 1) dry-etched mesa sidewall induced leakage current, which is related to the device fabrication, 2) lack of gate control on the MOS channel at high drain bias, i.e. drain-induced barrier lowering effect and 3) bulk semi-polar GaN leakage via the buried p^+-GaN current blocking layer.

In order to understand the origin of the high drain-to source leakage current, two-terminal circular p^+-GaN / n^--GaN / n^+-GaN diode structures with varying diameter from 100 µm to 250 µm were also fabricated. Fig. 3-25 shows the 2-terminal I-V characteristics of the circular p^+-GaN / n^--GaN / n^+-GaN diodes. It is noted that current of the diode structure (without the MOS channel) exhibits the similar behaviour as the high off-state drain to source leakage current in the MOSFET. In addition, the current from the diode structure is found to scale with the diode area. This implies that, rather than the dry-etched mesa sidewall induced leakage current and

the leakage via the MOS-channel, the leakage current flows through the bulk semi-polar GaN was dominant in the device leakage current [41].

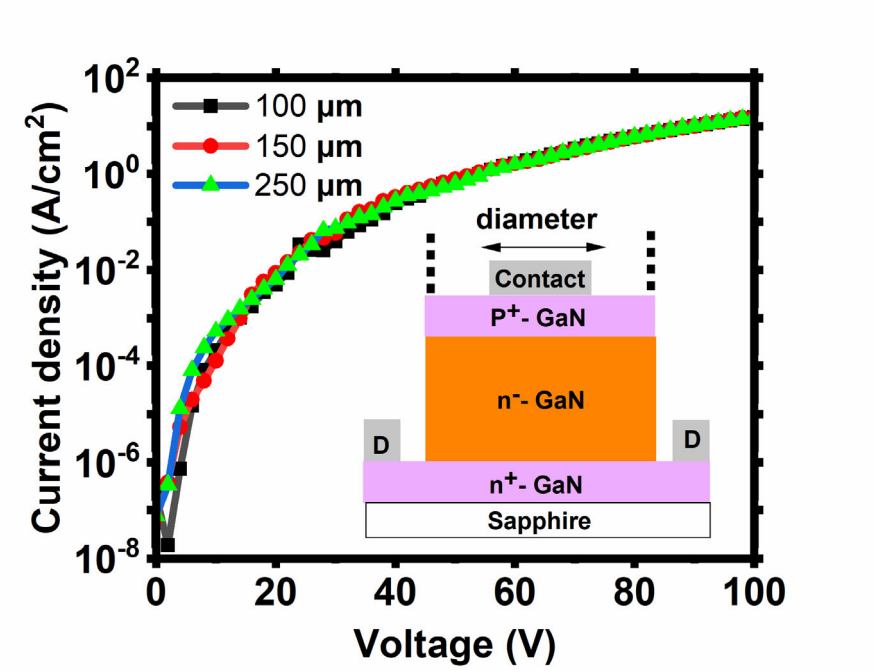

Figure 3-25. I-V characteristics of the circular p^+-GaN/n^--GaN/n^+-GaN diodes.

High temperature p^+-GaN activation temperature at 800 °C for 20 minutes in N_2 environment was conducted to investigate the effect of annealing temperature on the leakage current in the p^+-GaN / n^--GaN / n^+-GaN diode structures as described in [30]. In this work, no discernible effect of improving leakage current was observed. In the contrary, leakage current was rising fast compared to the lower temperatures annealing, as shown in Fig. 3-26. This is maybe the result of the high temperatures annealing deforming the crystal structure and increasing the trap states with the bulk GaN [42], [43]. The direct growth of semi-polar GaN on foreign sapphire substrates were typically have a high dislocation density of $>10^{10}$ cm^{-2} [44], [45], which is significantly higher than that of GaN on GaN substrate with dislocation of $< 10^6$ cm^{-2} [46], [47]. Further advancements on the semi-polar GaN material growth methods or use semi-polar GaN substrates [48] together with the optimisations of the p-GaN activations in the future were needed to improve the overall semi-polar GaN device performance.

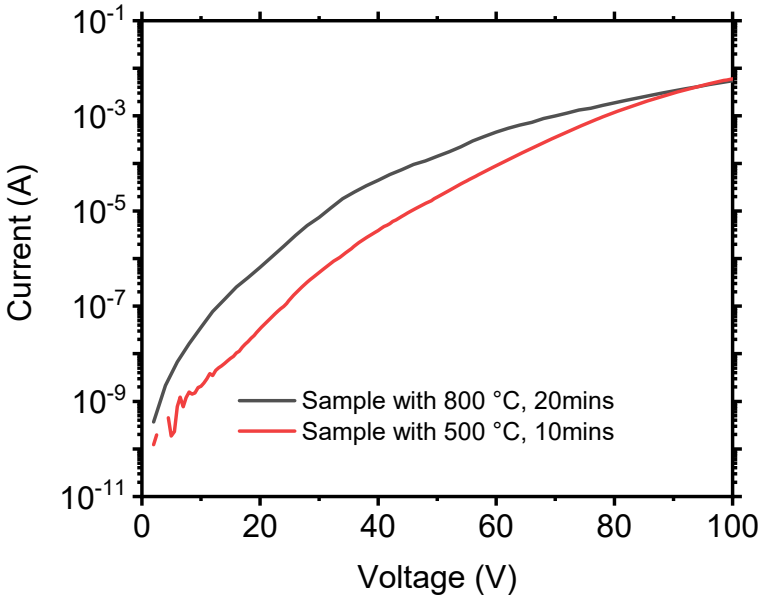

Figure 3-26: The leakage current of the circular p^+-GaN / n^--GaN / n^+-GaN diode structure with different activation annealing temperatures and times.

3.5 Summary

3.5.1 Conclusion

In this chapter, a summary of GaN crystal structure and the hydroxide-based wet etching mechanism is given. An experimental investigation of a crystallographic hydroxide-based wet etching technique was accomplished on the semi-polar (11-22) GaN-on-sapphire substrate. The design consideration for the V-groove trench metal-oxide-semiconductor field effect transistor (MOSFET) is offered. Fabrication process for the 3-terminal MOS devices is established. The gate modulation in the vertical channel device architecture is experimentally realized on the vertical GaN architectures for the first time without the use of the traditional dry plasma etching process to generate the GaN trench channel.

The 3-terminal VMOSFET operates at a positive threshold voltage of 9.6 V with an ON-state resistance of 8.0 Ωm.cm^2, and a maximum output current density of 516 A/cm^2. The channel mobility is extracted with a value of 21.3 cm2/Vs, in consistence with other's reported values. The VMOSFET's breakdown voltage is 150 V, limited by the gate breakdown. The punch through current was observed because of semi-polar bulk GaN leakage current. The wet-etch trench opening technique demonstrates the promise of the plasma etch-free trench formation method on GaN-based electronic devices and is compatible with optoelectronics on a semi-polar GaN platform.

3.5.2 Future works

Due to the intrinsic nature of crystallographic wet etching, when the trench opening windows aligned to the specific orientation of [1-100] and [-1-123] described earlier in this chapter, the crystal planes formed at the vertical sidewalls are different. The extracted ON-state characteristics is a combination result of two different inversion MOS sidewall, which could have very different properties. It could be one of the sidewalls have superior channel mobility, but another sidewall was significantly worse. Or the interface trap mechanism and/or interface properties are very different. Connecting only one side of the source may be a useful tactic for investigating the single sidewall MOS interface, as shown in Fig. 3-27. By just connecting one side of the source and drain, the conduction channel will be dominated at one side trench sidewall when the gate bias is applied, making it possible to investigate the various properties of the specific crystal planar MOS interface.

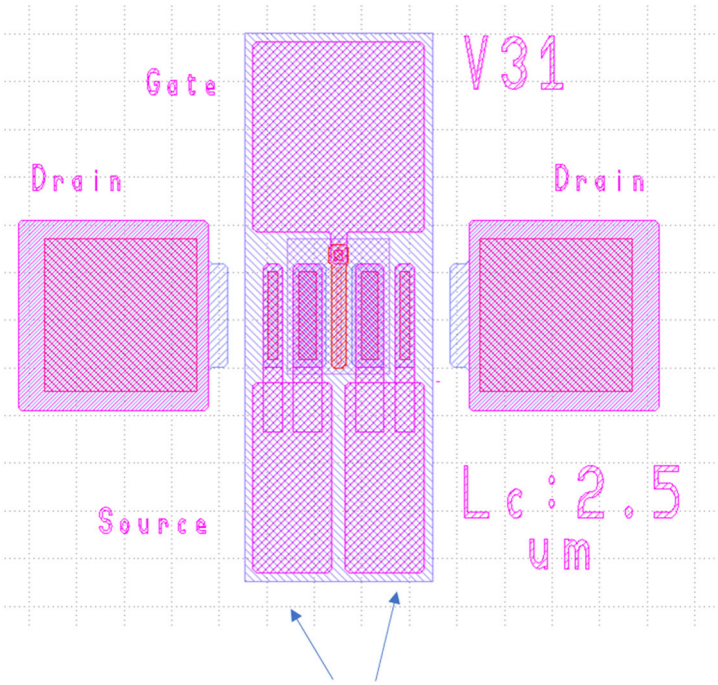

Figure 3-27. An illustrated photolithographic mask with separated source terminal probe pads.

On the other hand, it would be of interest to explore the V-groove trench formation when aligned to different orientations, as shown in Fig. 3-28. With the changing of wet-etching opening, the V-groove trench formations would have different mechanisms and provide further insight into the crystallographic wet-etching V-groove sidewalls, which have not been studies in this work. The photolithography masks have already been designed and manufactured and available at the EEE cleanroom, awaiting the exploration of these properties.

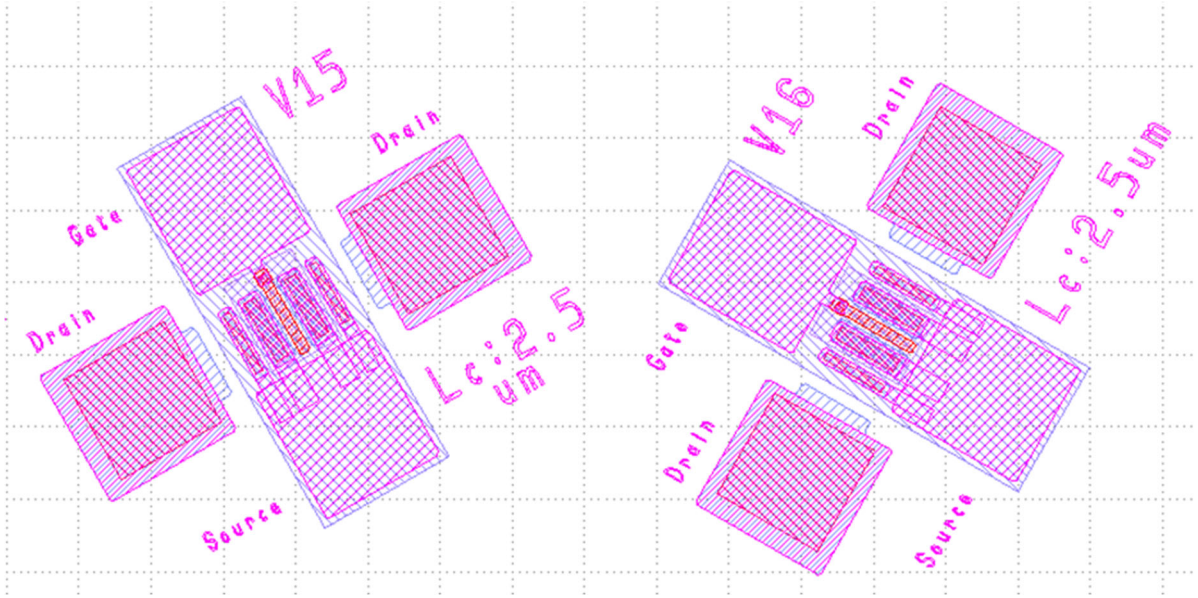

Figure 3-28. An illustrated photolithographic mask with different wet-etching opening orientations.

For the optimization of the OFF-state, it would be suggested to grow the semi-polar (11-22) GaN on the bulk semi-polar substrate to excluding the impacts of defects induced leakage current. Starting by the activation temperature's impacts on the p-type semi-polar GaN p-n junction characteristics followed by the optimization of 3-terminal devices. The trench filling [40] or hick bottom gate dielectric [25] should be adapted to mitigate the V-groove bottom electric field crowding and enhance the OFF-state breakdown characteristics.

3.5 References

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4. Modelling, Fabrication, and Analysis of Vertical Semi-polar (11-22) GaN FinFETs

4.1 Introduction

Vertical Fin field effect transistors (FinFETs) are very attractive for power switching applications with many merits such as a high breakdown voltage, a low on-state resistance, and low switching losses [1]. It features sub-μm Fins with all-around gate stacks to modulate the vertical channel current without the need of p-GaN layer to serve as a current-blocking layer, [2] [3], [4].

In chapter 3, the vertical V-groove semi-polar GaN MOSFETs have been fabricated and demonstrated using the wet crystallographic etching trench opening method at the relatively large size in the range of ~ μm. In this chapter, the study focuses on applying the crystallographic hydroxide-based wet etching technique for semi-polar (11-22) GaN V-groove FinFETs with sub-micron Fin sizes. In the reported Fin arrays formation for the FinFETs on polar (0001) GaN structure, the precise control on the optimization of plasma dry etching uniformity is important.

On the other hand, the novel wet etching method on the semi-polar GaN enables the Fin to be formed without the needs of the dry plasma etching. The wet-etch technique induces no dry plasma etching surface defects on the Fin sidewalls and results in a high uniformity vertical sidewall morphology which are critical for the electrical performances of the FinFETs.

In this chapter, device design consideration and electrical performance of the semi-polar (11-22) GaN FinFETs are simulated using Sentaurus TCAD at first. The development of the device fabrication process is performed and device characterization results on the fabricated FinFETs are presented. The device fabrication including electron beam lithography, electrical

characterization of the semi-polar (11-22) GaN Vertical FinFETs, and the investigation of the wet etching Fin arrays by the scanning electron microscopy (SEM) images were conducted at the Electronic and Electrical Engineering Department, University of Sheffield. The semi-polar (11-22) GaN epitaxy wafers were provided by University of Cambridge.

4.2 Simulation and Modeling

4.2.1 Device Structure

The schematic of device structure of the GaN FinFETs is shown in Fig. 4-1. The device features an n^+-GaN/ n^--GaN/ n^+-GaN epitaxy structure. The base simulated parameters are a 0.5 μm bottom n^+-GaN (Si: ~ 5×10^{18} cm^{-3}) for drain ohmic contact, lightly doped 3 μm n^+-GaN (Si: ~ 1×10^{15} cm^{-3}) to serve as the drift region and a 50 nm top n^+-GaN (Si: ~ 5×10^{18} cm^{-3}) for the source ohmic contact. The bulk semi-polar GaN mobility was set as 99 cm^2/Vs, corresponds to the reported semi-polar GaN on m-sapphire mobility of 99.3 cm^2/Vs [5]. The channel mobility at the gate-insulator-semiconductor interface was ~ 12 cm^2/Vs, closed to reported Fin channel mobility of ~ 14 cm^2/Vs [6]. A 20 nm SiN_x was used as the gate dielectric. The interface density between gate dielectric and GaN sidewall was set as 2×10^{12} $cm^{-2}eV^{-1}$, which is the reported interfacial trap density in the GaN FinFETs [7], [8]. The gate metal work function was 5.15 eV [9], which corresponds to the Ni gate metal. The Fin sidewall angles were set as 32°and 58° angle offset, which correspond to the theoretical a-plane and c-plane GaN sidewalls angle offset, respectively that inside the (11-22) bulk GaN, which is described in the chapter 3.

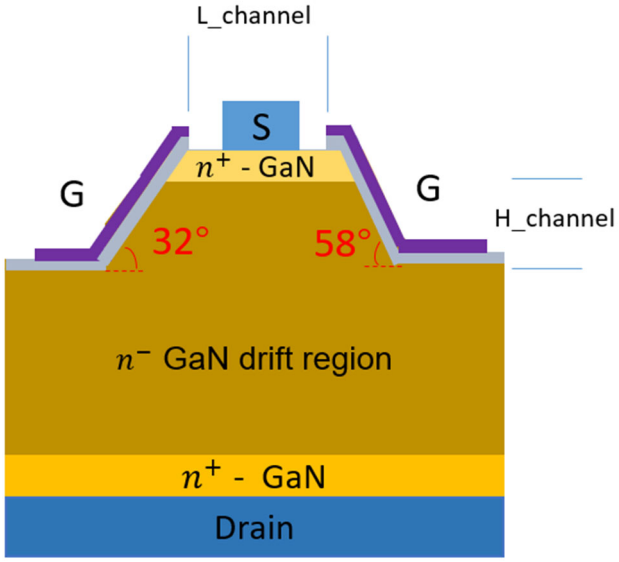

Figure 4-1. Schematic diagram of a semi-polar (11-22) GaN FinFETs.

4.2.2 Operation Principle and Design Parameters

The section describes a basic operation principle and provides initial understand of the semi-polar (11-22) GaN FinFETs. Devices structure was simulated using Sentaurus TCAD with 2 dimensional (2D) drift-diffusion carrier transport models. Fig 4-2 shows the simulated cross sectional electron profile at OFF-state (V_{gs}=0 V) and the corresponding band diagrams along the gate. The electrons are depleted from the Fin sidewalls due to the work function difference between the gate metals and GaN and the conduction band of GaN bending up.

When a sufficiently high positive gate voltage (V_{gs}= +3 V) is applied, conduction band bends down and the electrons starts to accumulate at the gate dielectric/GaN interface and leads to sidewall channel conduction in the FinFETs as illustrated in Fig. 4-3 (a) and (b).

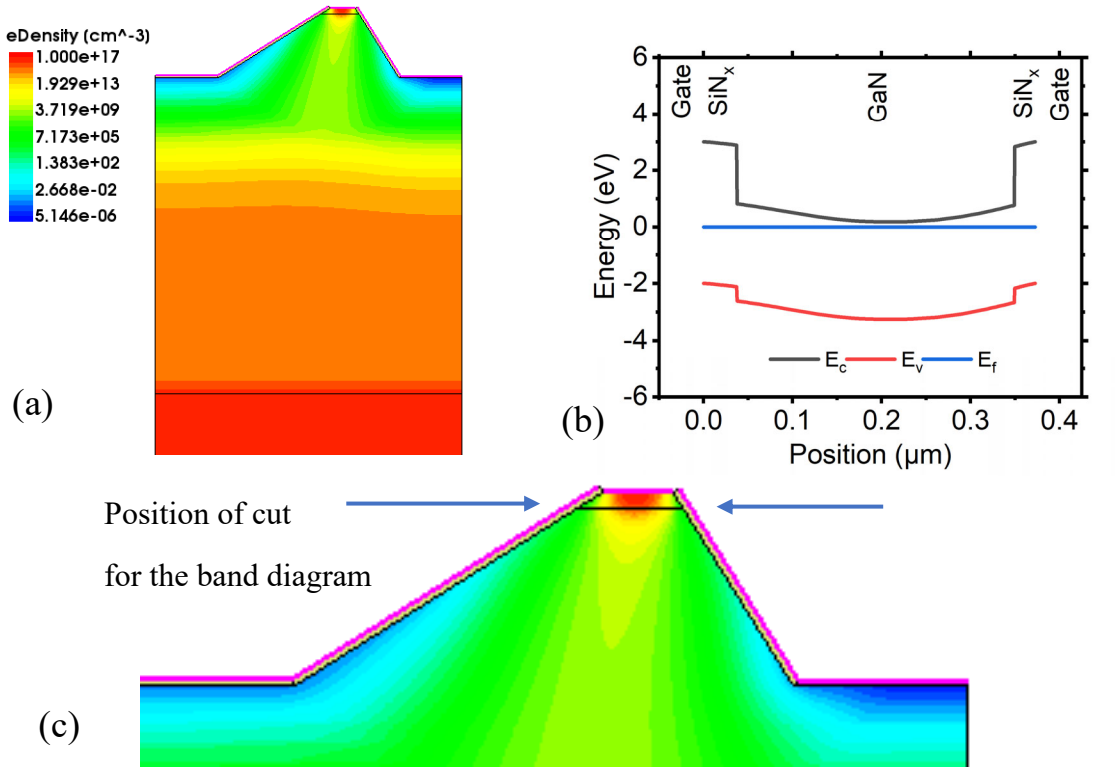

Figure 4-2. (a) Simulated electron profile at OFF-state (V_{gs} = 0 V) (b) corresponding band diagram for FinFETs.

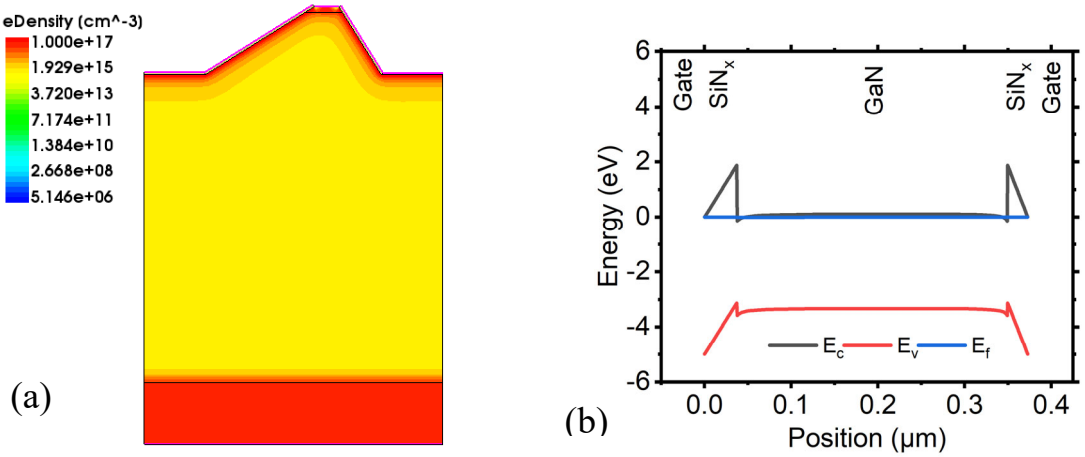

Figure 4-3. (a) Simulated electron profile at ON-state (V_{gs} = 3 V) and (b) corresponding band diagram for FinFETs at the gate region.

Fig. 4-4 shows the simulated gate transfer characteristics for FinFETs with different Fin length (L_channel) in the linear and log scales. The Fin length (L_channel) was defined as the top n^+-GaN lateral length and the Fin height (H_channel) was defined from the top n^--GaN which is 700 nm, as shown in Fig. 4-1. The channel width (W_channel) is set as 1000 μm in the simulations. For the larger L_channel (>200 nm), the threshold voltage (V_{th}), defined at 1 nA,

of the FinFETs shifts negatively. This is because the wider channel results in the difficulty in the gate modulation in the center region of the Fin and a more negative gate voltage is required to fully deplete the channel. Therefore, reducing the L_channel at sub-micron size < 300 nm is important to achieve the enhancement mode operations in the semi-polar GaN FinFETs.

Fig. 4-5 (a) shows the simulated gate transfer characteristics of the FinFETs with varying the Si doping concentration of the n^--GaN drift layer from $1x10^{15}$ to $1x10^{17}$ cm^{-3}, L_channel of 200 nm and H_channel of 700 nm was used. A higher Si doping concentration is found to shift V_{th} towards more negative. Fig 4-5 (b) shows the influence of the gate dielectric thickness on V_{th} of the FinFETs. A thinner gate dielectric thickness shifts V_{th} more positively. A low doping concentration in the n^--GaN drift layer together a thin gate dielectric thickness is required to achieve enhancement mode operation.

The simulated output I-V characteristics of the FinFETs with a 200 nm Fin length, 700 nm Fin height, and n^--GaN drift region doping of 1×10^{15} cm^{-3} are shown in Fig. 4-6. An output drain current (I_d) density of ~ 280 A/cm^2 for V_{gs}=2 V at V_{ds} =10 V and an ON-state resistance (R_{on}) of 4 mΩ.cm^2 was extracted. The current was normalized to L_channel (200 nm) * W_channel (1000 μm). For a higher current density, a higher drift region doping concentration may be used. However, the higher doping concentration leads to the shift of V_{th} toward negative. It is a trade-off between the ON-state and OFF-state performances. On the other hand, to improve the output current is to increase the bulk mobility and the channel mobility. However, the channel mobility or the bulk mobility is inherently limited by the current development of semi-polar GaN bulk material quality and metal-insulator-semiconductor (MIS) interface quality.

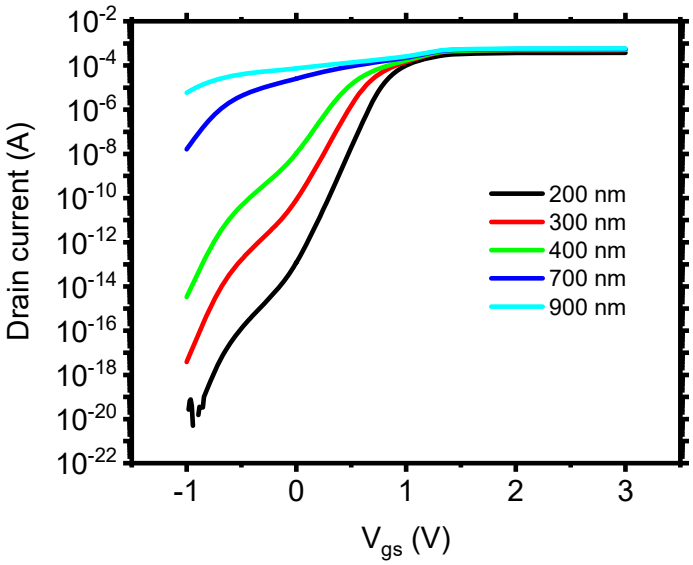

Figure 4-4. Simulated gate transfer characteristics of FinFETs with varying Fin length in the log scale.

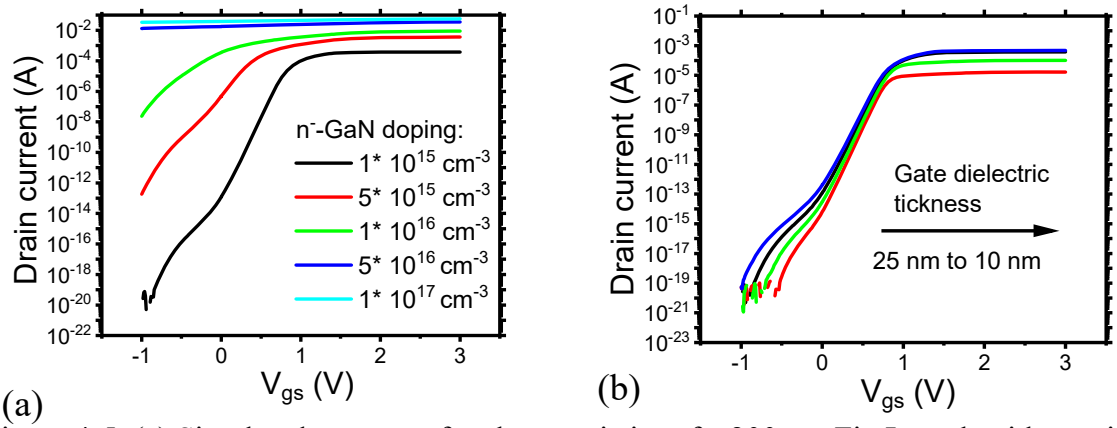

Figure 4-5. (a) Simulated gate transfer characteristics of a 200 nm Fin Length with varying n^--GaN Si doping concentration and (b) Simulated gate transfer characteristics of a 200 nm Fin length with varying SiN_x gate dielectric thickness.

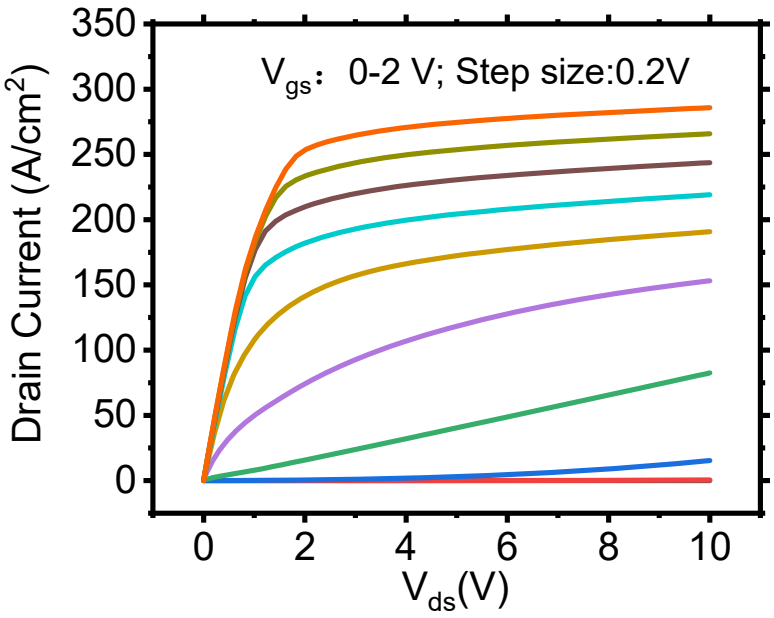

Figure 4-6. Simulated I-V characteristics of the FinFETs with 200 nm L_channel and 700 nm H_channel.

4.3 Semi-polar (11-22) GaN FinFETs Device Fabrication Process

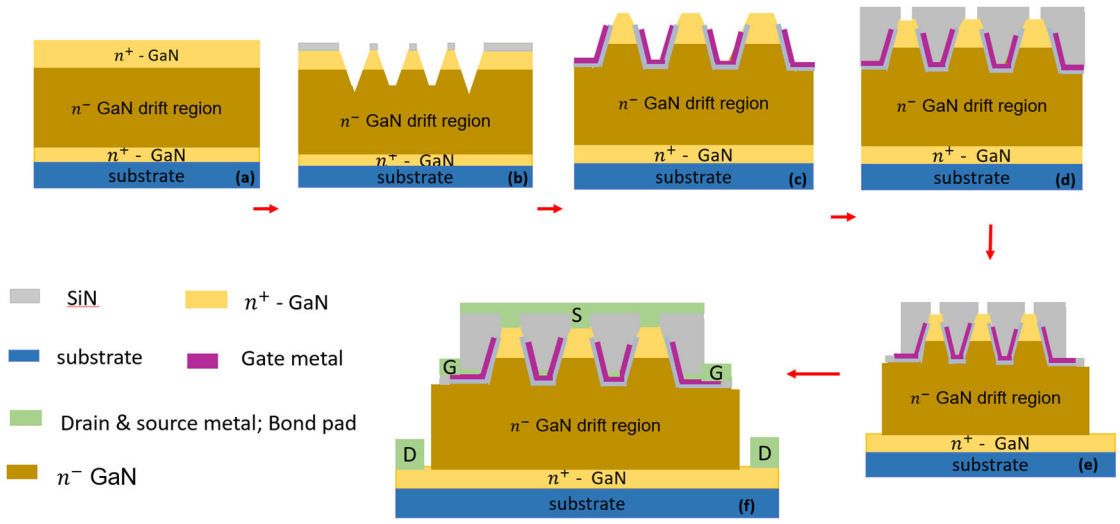

Figure 4-7. Overview of vertical V-groove semi-polar GaN FinFETs fabrication flow.

The semi-polar (11-22) GaN sample in this study was grown on m-plane sapphire substrate by metal organic chemical vapour deposition (MOCVD). The wafer epitaxy structure as follow: 0.2 μm n^+-GaN (Si: ~ 5×10^{18} cm^{-3}), 3.0 μm n^--GaN (semi-insulating), and 0.5 μm n^+-GaN (Si: ~ 5×10^{18} cm^{-3}) as shown in Fig. 4-7 (a).

Fig. 4-7 give an overview of vertical semi-polar GaN FinFETs fabrication process for this study. First, the Fin formation on the epitaxy structure was performed using potassium hydroxide (KOH) solution as shown in Fig. 4-7 (b). As the Fin length is sub-μm, electron beam lithography (EBL) was used to define the Fin patterns in the study. The details of Fin formations and the EBL process are described in Section 4.3.1.

Once the Fins were formed, the next step is the gate dielectric and gate metal deposition as shown in Fig. 4-7 (c). To achieve an all-around MIS gate structure for the FinFETs, a photoresist planarization method was employed in this study. The details of the planarization process and the MIS gate formation are described in Sections 4.3.2 and 4.3.3.

Finally, device mesa isolation was performed using inductively couple plasma (ICP) etching. The device fabrication was completed with the metal deposition of the probe pads for gate, source and drain electrodes. The fin length of the FinFETs in this study is varied between 100 to 900 nm. The fin height and the fin width of the FinFETs is 700 nm and 100 μm, respectively. The SEM image of the fabricated FinFETs is shown in Fig. 4-8. The detailed step-by-step process traveller is also provided in the Appendix A.

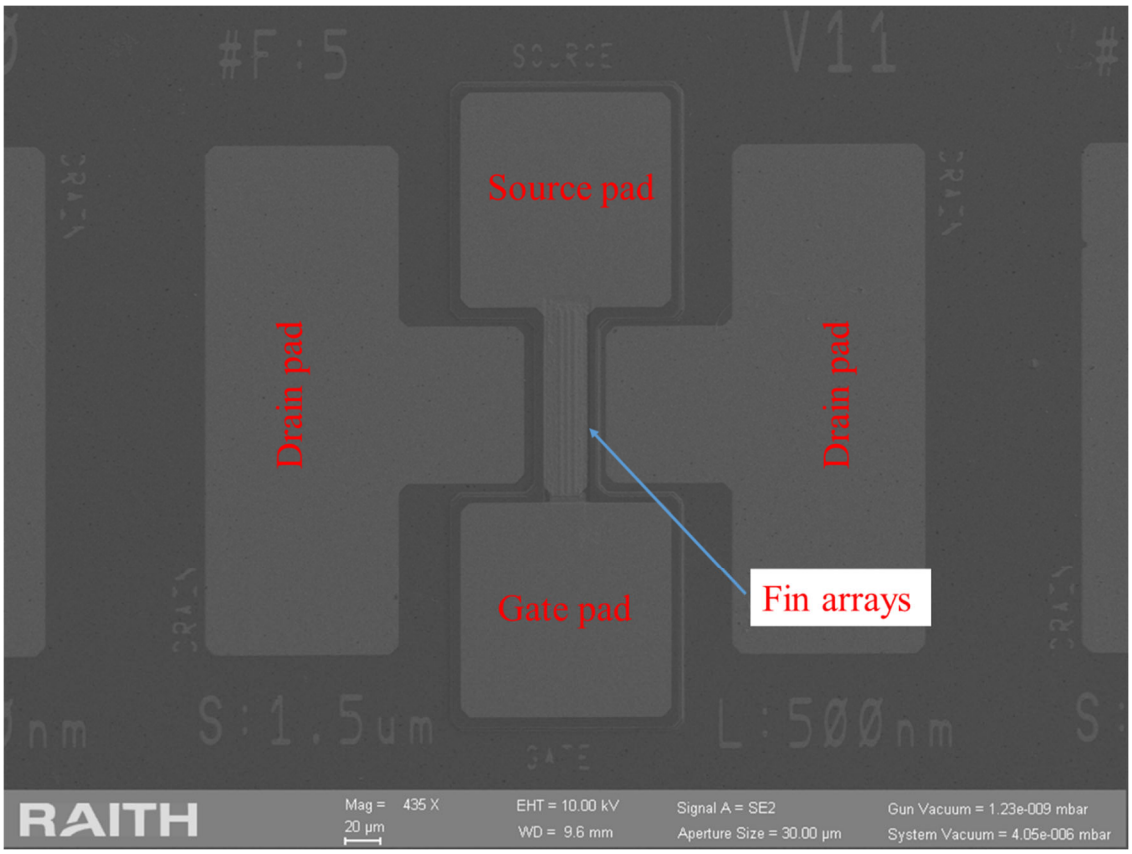

Figure 4-8. SEM image of the fabricated semi-polar GaN FinFETs.

4.3.1 Fin Formation Using the Crystallographic Wet Etching

Fig. 4-9 shows the process flow for the Fin formation step. Metal alignment marks were firstly patterned using the optical lithography and deposited on the sample to allow the Fin to align to the [-1-123] and [1-100] direction the same as described in Chapter 3. A ~ 100 nm of SiN_x was deposited using ICPCVD as a hard mask for the wet-etch step for the Fin. EBL was then used to define the Fin patterns on the SiN_x hard mask as shown in Fig. 4-9 (b). Unlike the V-groove fabrication for the V-groove MOSFETs outlined in Chapter 3 which uses the photoresist SPR350 with a typical thickness of ~ 1200 nm for optical lithography, the EBL resist used was the AR-P-6200 (CSAR62) with a thickness of ~ 400 nm. However, it was found that the

thickness of the EBL resist was not sufficient to sustain the aggressive dry-etch of the SiN_x hard mask using reactive ion etching (RIE) and the SiN_x was partially etched.

To ensure the SiN_x hard mask for the wet-etch step remains in-tact after the RIE step, a Ni/Au (20 nm/ 20 nm) metal was used as a hard mask for etching the SiN_x instead. The patterns of the metal hard mask were defined using the EBL as shown in Fig. 4-10 (a). For the EBL, the electron beam dosage becomes important. A standard 100 μC/cm^2 at 50 kV was initially used for the exposure. However, the dosage was not sufficient and led to underexposed which causes the metals are not adhered to the SiN_x, as shown in Fig. 4-10 (b). The problem was solved by increasing the electron beam dosage to 160 μC/cm^2 at 50 kV. Fig. 4-10 (c) illustrates the optical image of the EBL defined metal hard mask on SiN_x. The actual defined pattern sizes after the EBL exposure and resist development are less than < ~10 % deviation from the designed sizes.

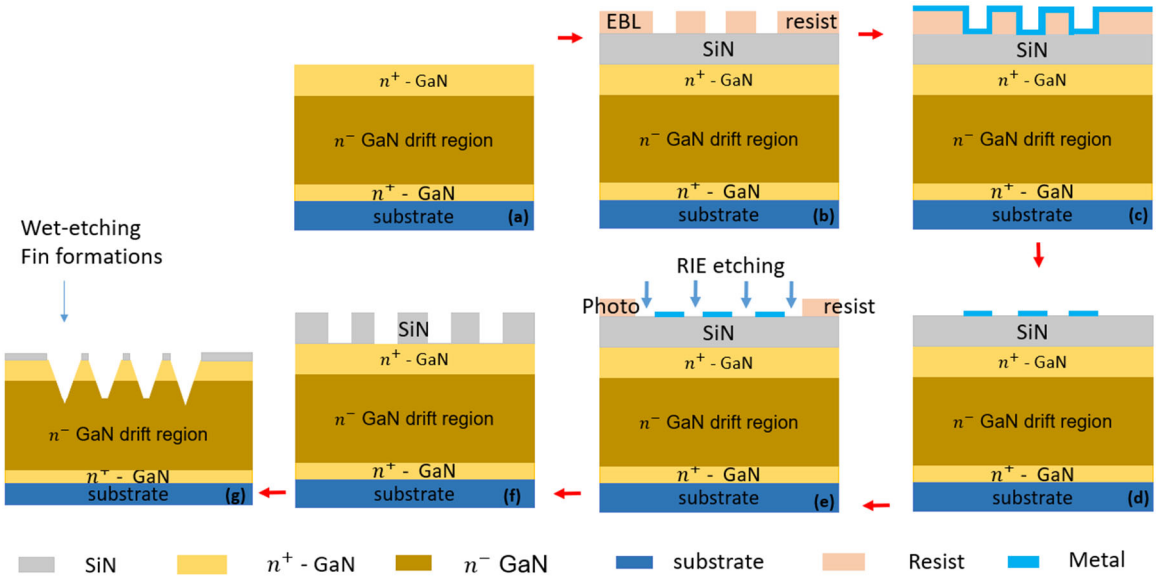

Figure 4-9. The process flow of the Fin array formation using KOH wet etching method.

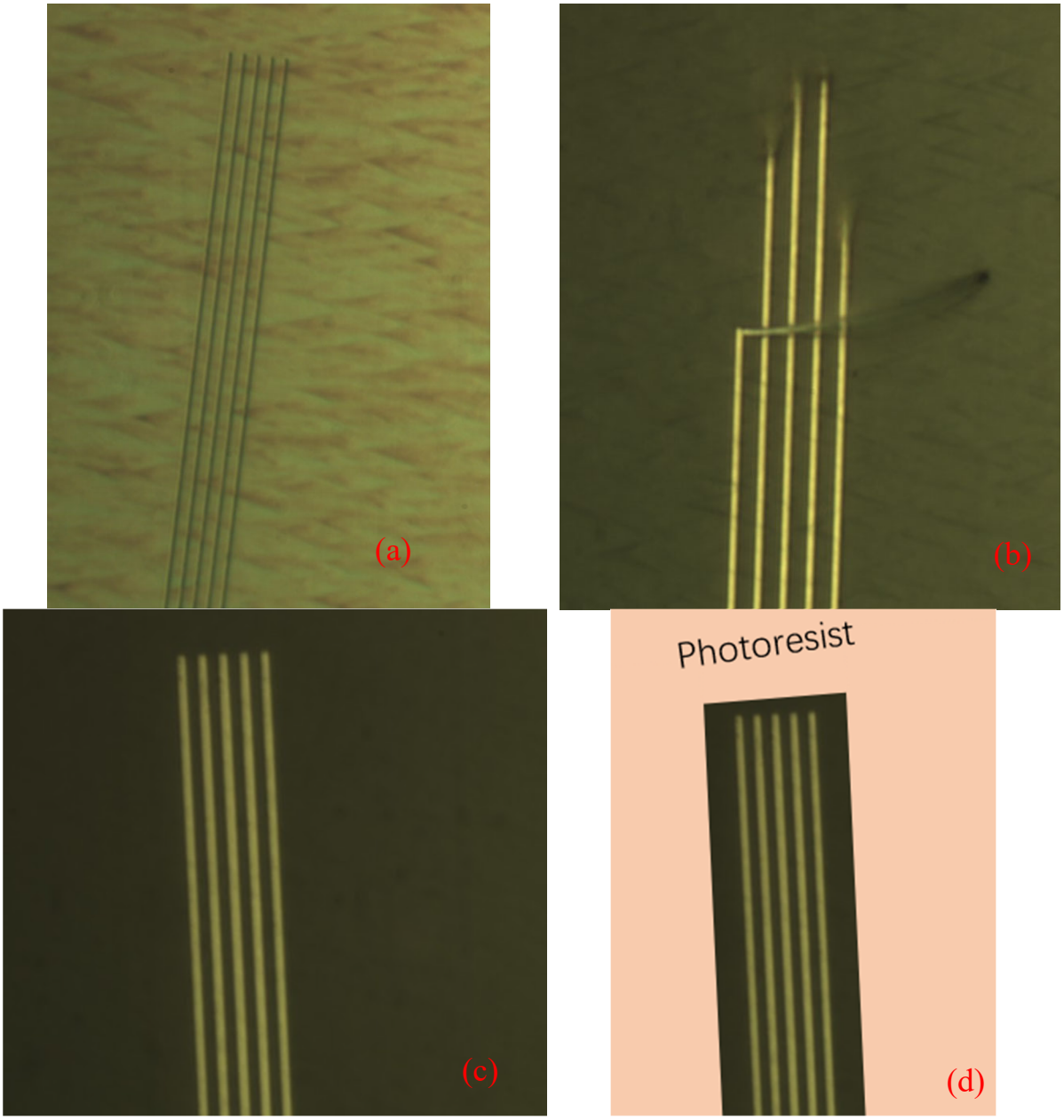

Figure 4-10. (a) an optical image of Fin array pattern defined by the electron beam lithography. (b) problematic hard mask metal lift-off. (c) a successful hard mask metal lift-off and (d) Fin arrays boundary defined by optical photolithography.

Upon successfully obtaining the desired Fin patterns on the metal hard mask, additional SPR350 photoresist was spin-coated and UV-exposed to define the boundary of each Fin arrays as shown in Fig. 4-9 (e) and Fig. 4-10 (d). The SiN_x inside the boundary was etched using the RIE to form the wet-etching windows, ready for the KOH wet-etching to form the vertical V-groove trench sidewall on semi-polar GaN, as shown in Fig. 4-9 (f). The sample was then wet-etched at the same condition as described in the Chapter 3 to establish the Fin arrays. The

remaining Ni/Au hard mask for the Fin formation was etched away by the aqua regia. Fig. 4-11 and Fig. 4-12 show the SEM image of Fin arrays with a Fin length of 200 nm and 500 nm, respectively.

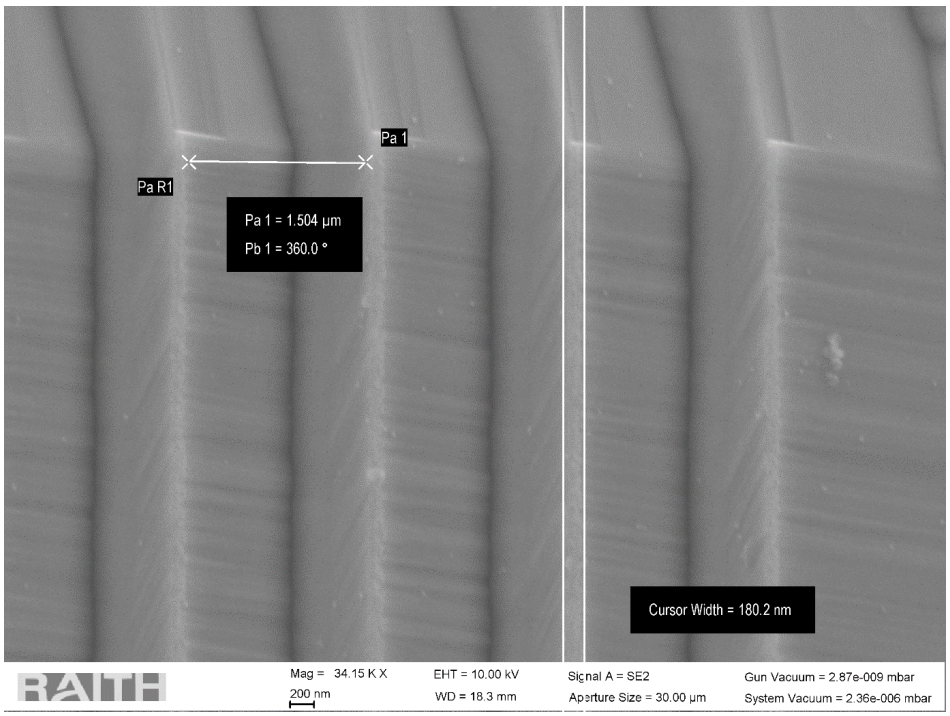

Figure 4-11. Fin arrays with size < 200 nm.

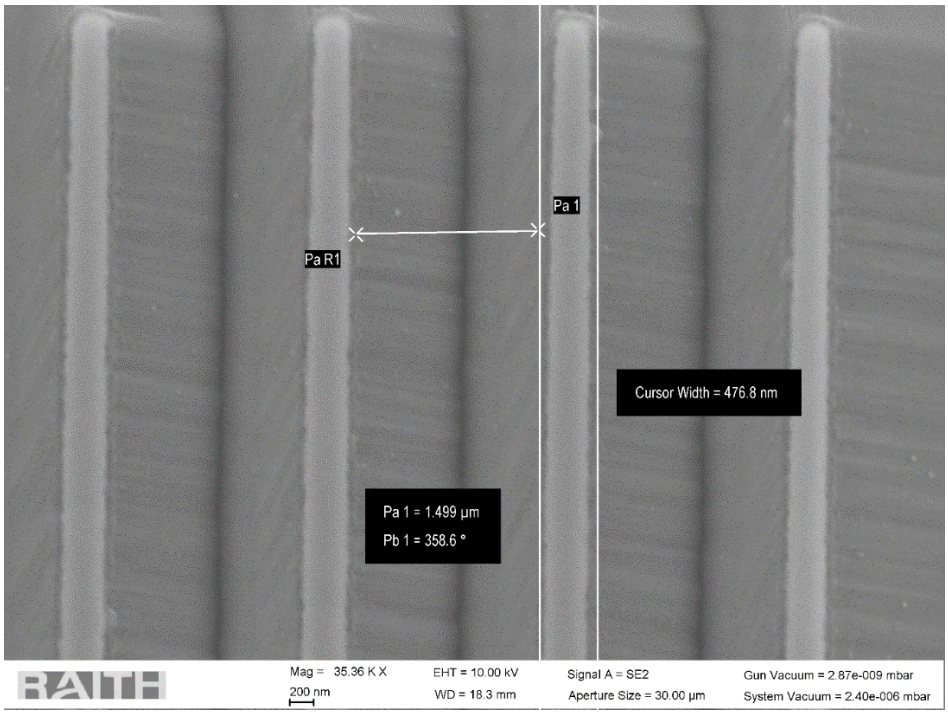

Figure 4-12. Fin arrays with size < 500 nm.

4.3.2 Photoresist Planarization

Once the Fins were formed, the next step is to obtain the gate dielectric and gate metal deposition on the Fin sidewall as shown in Fig. 4-7 (c). To ensure an all-around gate are achieved for the FinFETs, depositions of the gate dielectric and metals were required. However, in order to access the source contacts on the top of the Fin, the gate dielectric and metals on the top of the Fin were needed to be etched away while the sidewall gate dielectric and metals are protected.

As the Fin are with sub-μm length, the size and the alignments of the etch windows on the top of the Fin are critical. The EBL could be used to define the etch window. However, the issue become whether the EBL resist is be able to sustain both aggressive etching of the gate dielectric and gate metals. To overcome this, a photoresist planarization method was employed in this study to remove the gate dielectric and metals on the top of the Fin. The details of the planarization process are described in Section 4.3.2.

The photoresist planarization is based on the idea [10], [11], [12], [13] that when the photoresist thickness (T1) and the vertical thickness of the Fin arrays (T2) are well adjusted, ie. $T_1 >> T_2$ as shown in Fig. 4-13. The narrow Fin array bottom would be filled in the photoresist and the top of the Fin is thinner compared to the bottom of the Fin, resulting in a "planarization" on the sample surface. Upon the sample surface being planarized, the O_2 plasma was used to etch back the photoresist to reveal the top of the Fins while the bottom of the Fin remains protected by the photoresist, as shown in Fig. 4-13 (d).

To validate this concept, the planarization process was performed on a SiN_x test structure first. The test structure consists of a 700 nm SiN_x deposited using ICPCVD on Si and Fin patterns was defined by the EBL with the steps described in Section 4.3.1. The SiN_x was etched using

the RIE to form Fin arrays (the SiN_x Fin arrays which mimic the GaN FinFETs have the same height as the channel height in the GaN FinFETs). Afterwards, BPRS 200 photoresist with a thickness of ~ 2.7 μm, which is much thicker than the 700 nm SiN_x, was spin-coated on the sample. The SEM image of the planarized photoresist on the SiN_x test structure was demonstrated in the Fig. 4-14. In addition, a surface profilometer was used to scan the top of the planarized Fin arrays. The measured vertical thickness value is ~ 86 nm, as shown in Fig. 4-15, indicating a planarized surface.

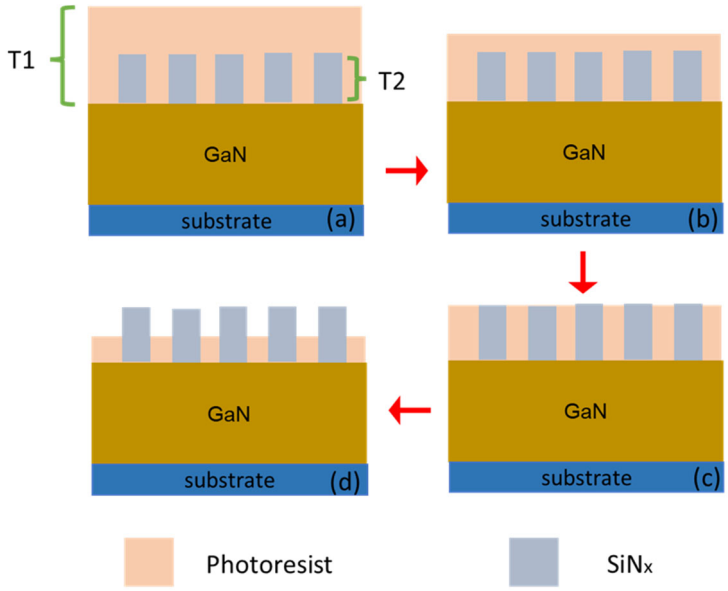

Figure 4-13. Photoresist planarization process.

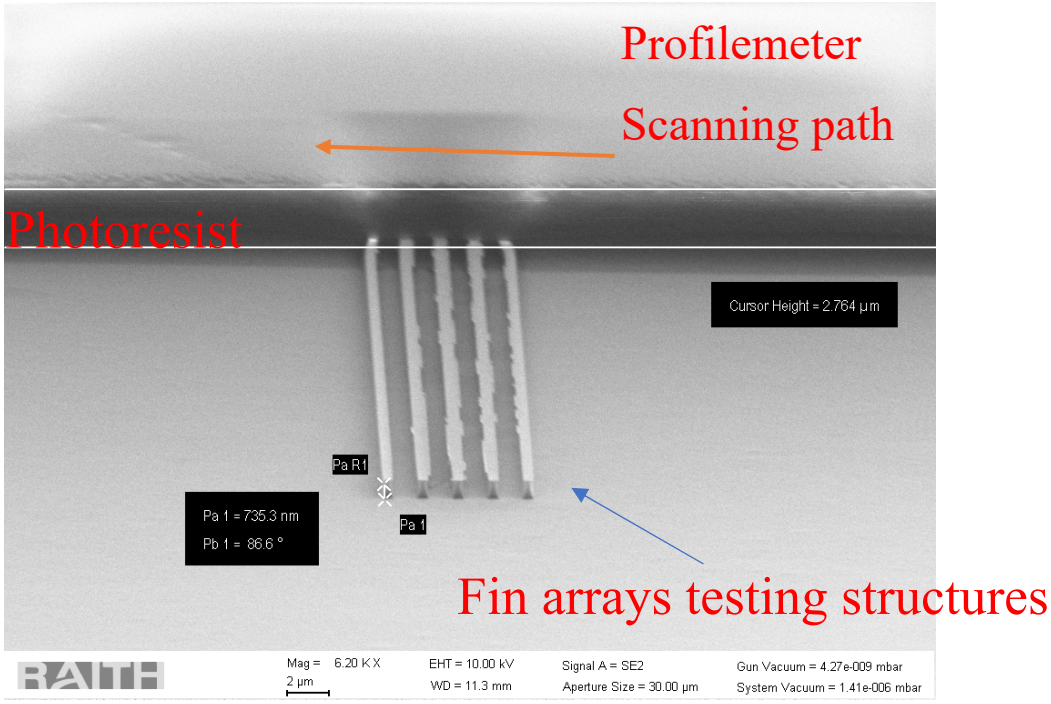

Figure 4-14. Cross sectional SEM image of planarisation testing strucutre.

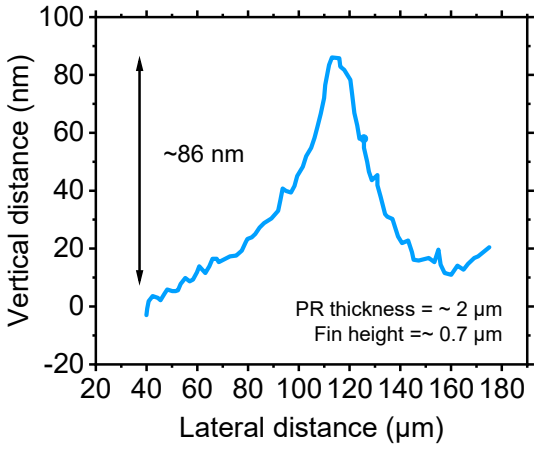

Figure 4-15. The surface profile of planarized structure measured using the surface profilometer.

The oxygen plasma etch back process, with a photoresist etch rate of 100 nm/min, was then used to etch the photoresist on the top of the Fin. The time required to revealing the top of the Fin can be estimated by: (T1-T2) / 100 nm/min. Therefore, a 20-min etch is required to reveal the top of the Fin with a height of 700 nm (T2). Fig 4-16 (a) shows the surface profile of the

planarized structure after 10 mins of oxygen plasma etching. The measured vertical thickness remains largely unchanged, which shows that the top of the Fin has not yet been revealed. However, the vertical thickness increases to 280 nm were measured after a further 12 mins of the etching. This corresponds to 280 nm of Fin height (measured from the top) is revealed. The SEM image of the Fin structure with the revealed Fin top is shown in Fig. 4-17.

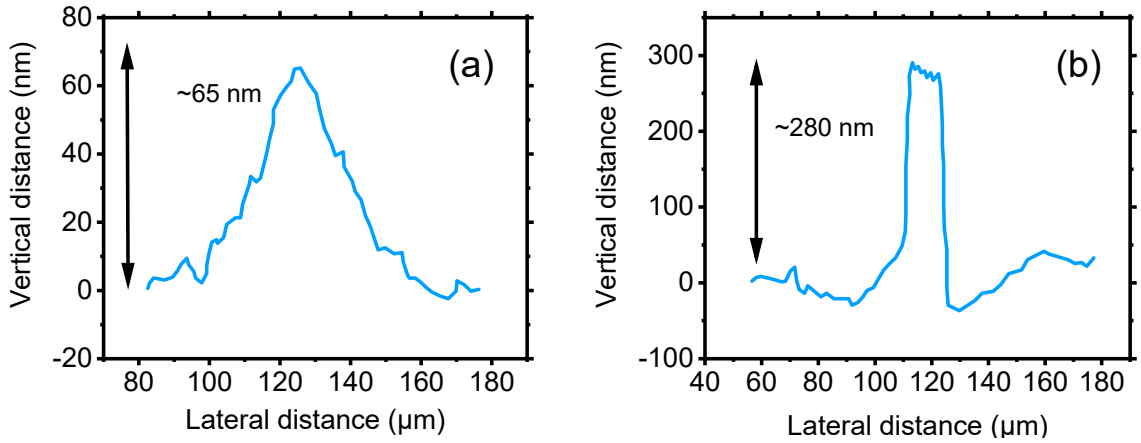

Figure 4-16. Oxygen plasma etch back process (a) top Fin not fully revealed and (b) top Fin fully revealed.

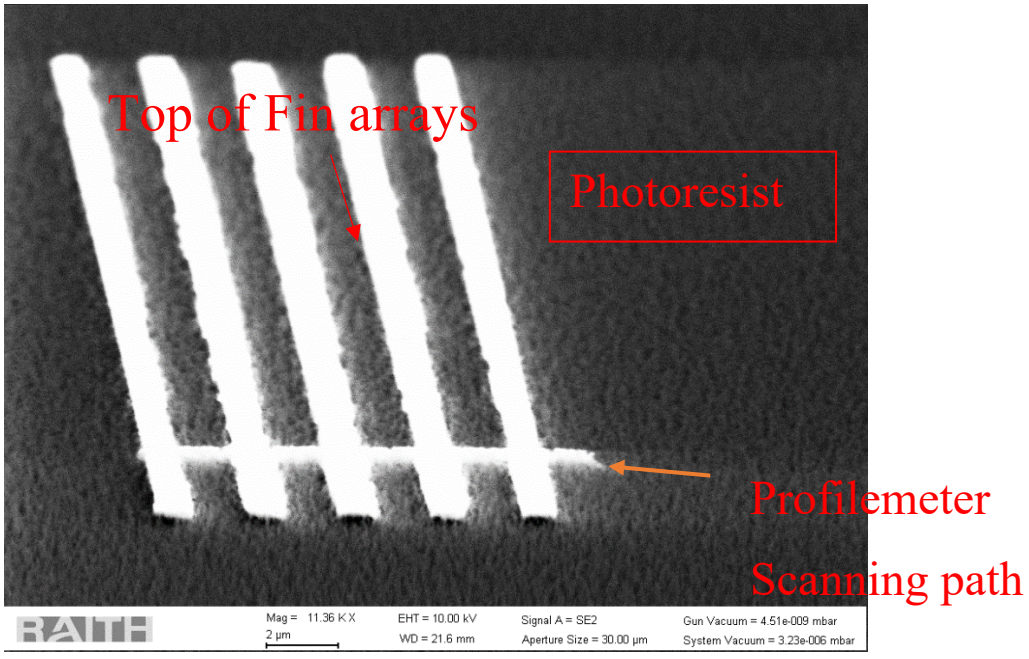

Figure 4-17. SEM image of oxygen plasma etch back of the SiN_x Fin arrays with the top of the Fin is revealed.

4.3.3 Gate Formation and Top Gate Metal Etching

After the validation of photoresist planarization and oxygen plasma etch back process on the trial dummy sample, this process was applied to the wet-etched GaN Fin arrays established in the Section 4.3.1. However, in the GaN FinFETs, the Fin arrays are within the boundary as shown Fig. 4-18 (a). In order to achieve a good planarization effect, the fin arrays must be the highest structure on the sample. An ICP etching step was introduced to etch the remaining SiN_x layer and 700 nm of the GaN (i.e. 200 nm of top n_ GaN and 500 nm of n-GaN drift layer), which is outside the active Fin arrays area, as shown in Fig. 4-18 (b) and (c).

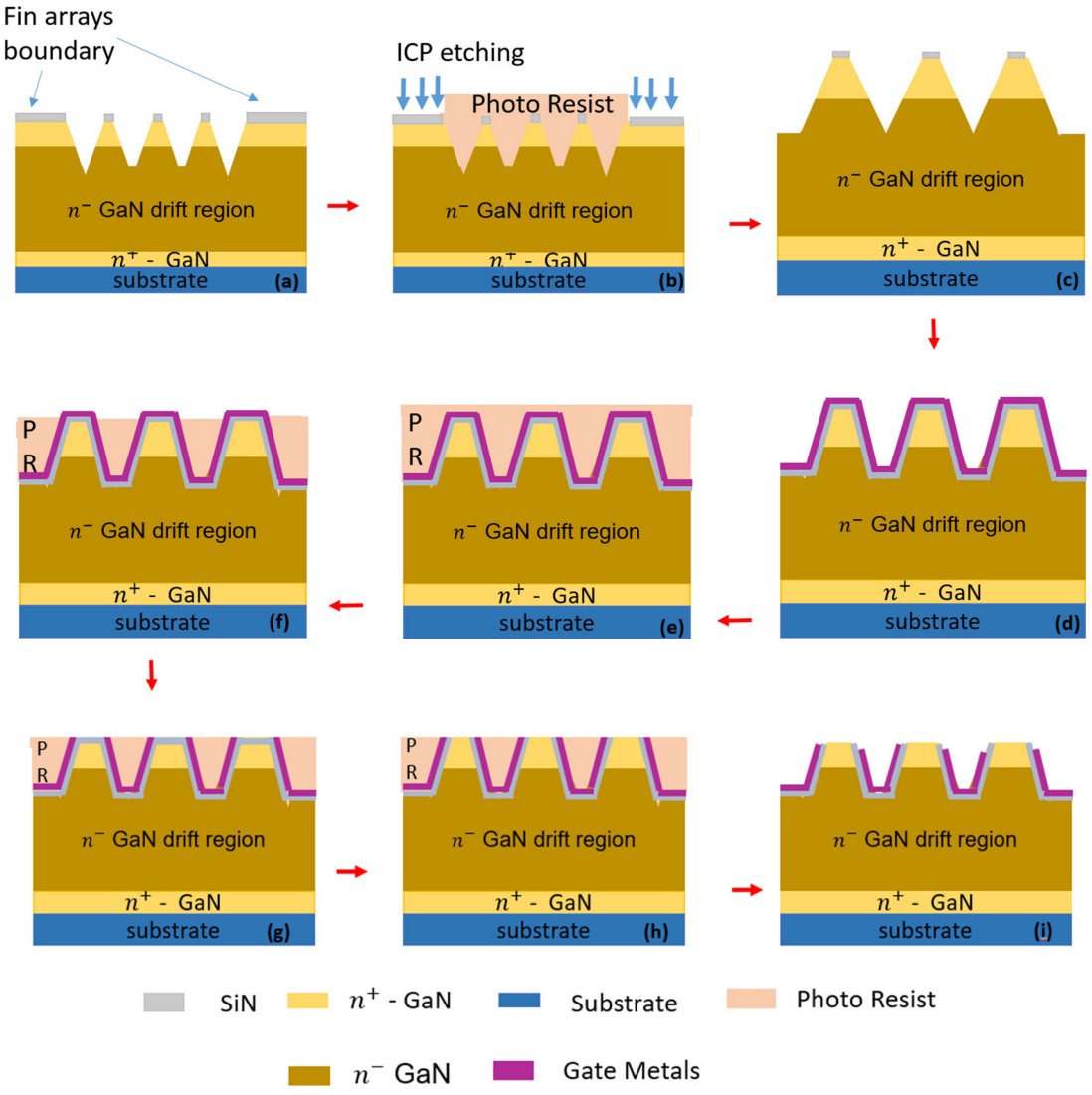

Figure 4-18. Process flow for the MIS gate formation and the photoresist planarization.

The Fin sidewall gate structure was the formed by a 20 nm SiN_x deposition using plasma enhance chemical vapour deposition (PECVD) and followed by gate metal Ni/Au (20 nm/ 200 nm) deposition, illustrated in Fig. 4-18 (d). Photoresist planarization and oxygen plasma etch back process described in Section 4.3.2 was used to expose the top of the Fins (Fig. 4-18 (e) and Fig. 4-18 (f)). Fig. 4-19 illustrates the SEM image of the GaN Fin array with the top gate metals revealed. The sample was then dipped in the aqua regia, the mixture of HNO_3 and HCl with the ratio of 1:3, for 10 s to remove the revealed gate metals. Fig. 4-20 shows the SEM image of the top gate metals have been removed successfully. Next, the sample was transferred to RIE chamber to etch the top SiN_x with an etching time of 30 s. Finally, the photoresist is removed by soaking the sample in photoresist stripper (EKC830) for 10 mins at 100 ℃, illustrated in 4-18 (i).

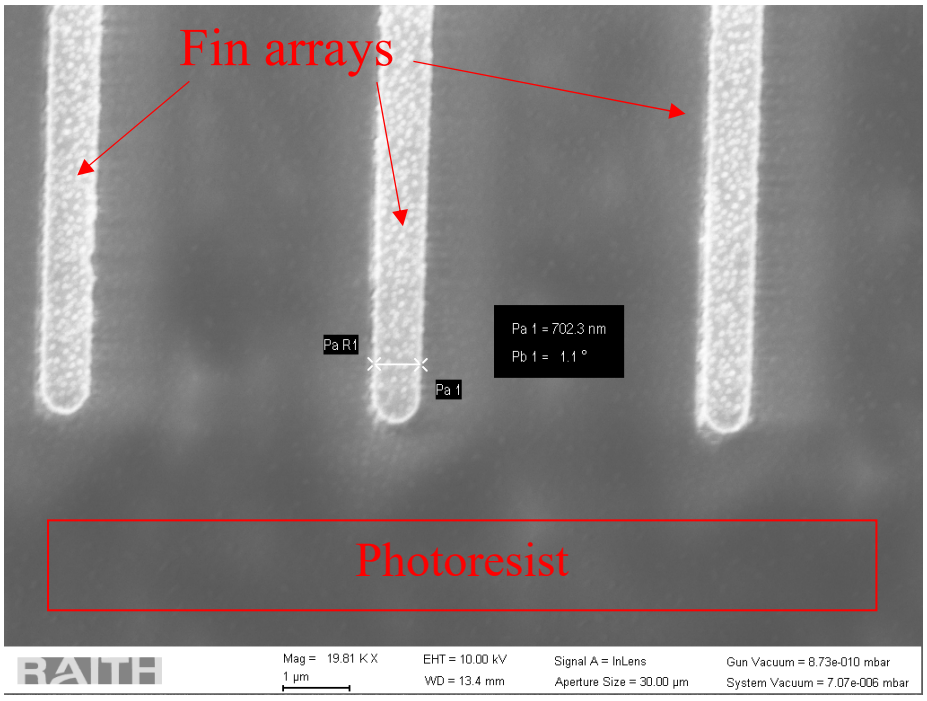

Figure 4-19. Photoresist planarization and oxygen plasma etch back process to reveal to top of the Fin with gate metals

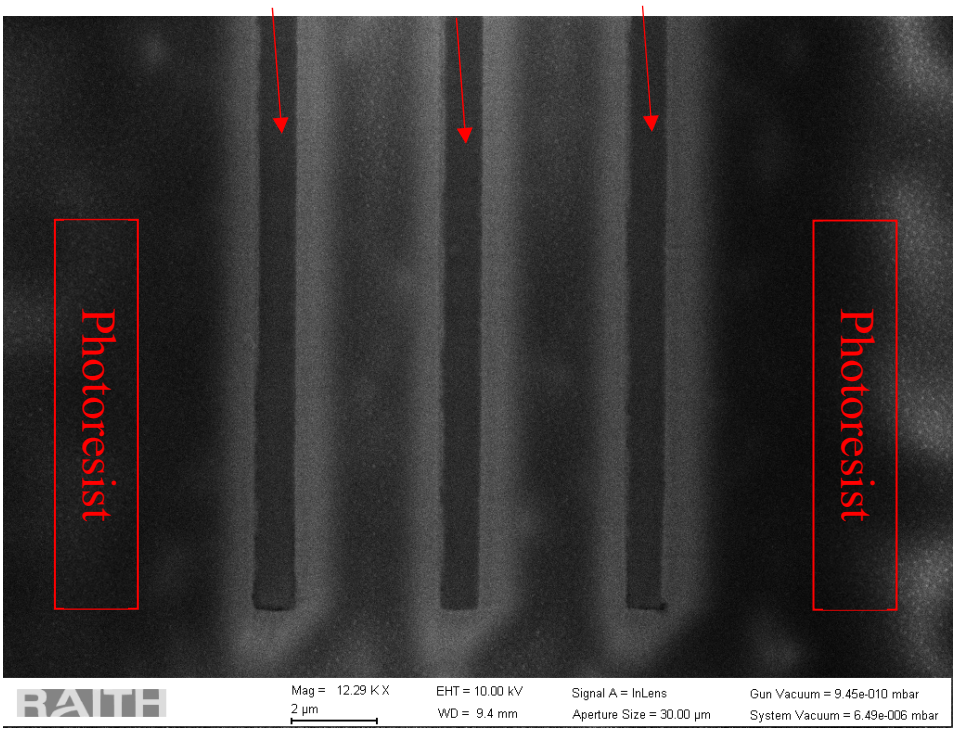

Figure 4-20. The top gate metals are removed using aqua regia while the bottom of the Fin is protected by photoresist.

4.3.4 Via Opening and Contact Formation

After establishing the removal of gate metals process, an additional ~ 80 nm SiN_x was deposited using PECVD to serve as an insulating layer between the gate and source metals (Fig 4-21 (a)). A further EBL step was used to define the etch via openings on the top of the Fin for the source contacts (Fig 4-21 (b)). In this process, the smaller the Fin patterns defined in the first stage EBL, the smaller tolerance of alignment errors in the second stage EBL. Fig 4-22 shows the defined source via-opening windows showing the mis-aligned and aligned patterns. The SiN_x was then etched using RIE to create the via-opening windows (Fig 4-21 (c)). The SEM image of the etched SiN_x opening on the top of a Fin is shown in Fig. 4-23.

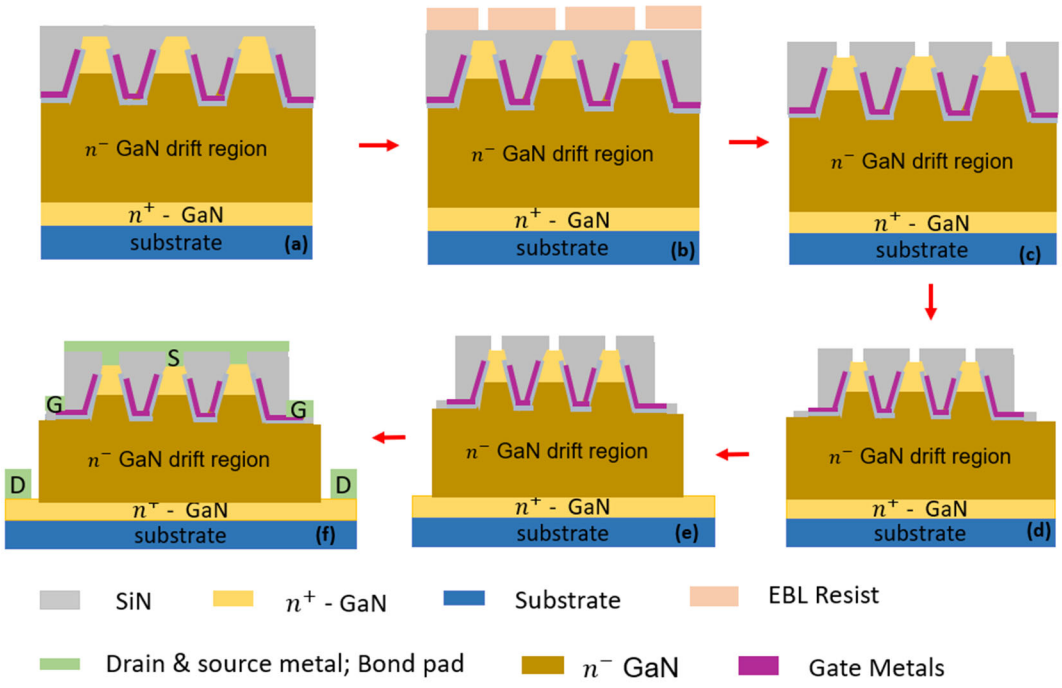

Figure 4-21. Fabrication process for the Via-opening and contact formation.

Via-opening by the 2nd stage EBL alignment

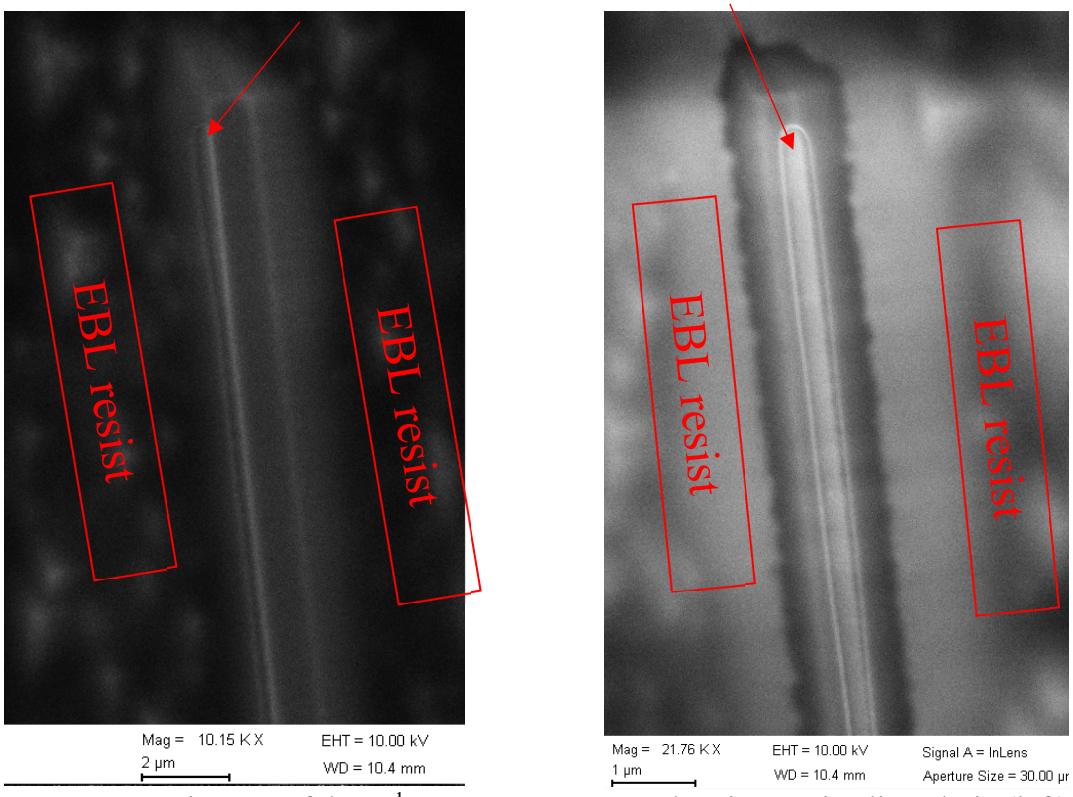

Figure 4-22. SEM images of the 2nd stage EBL patterns showing a mis-aligned Fin (left) and an aligned Fin (right).

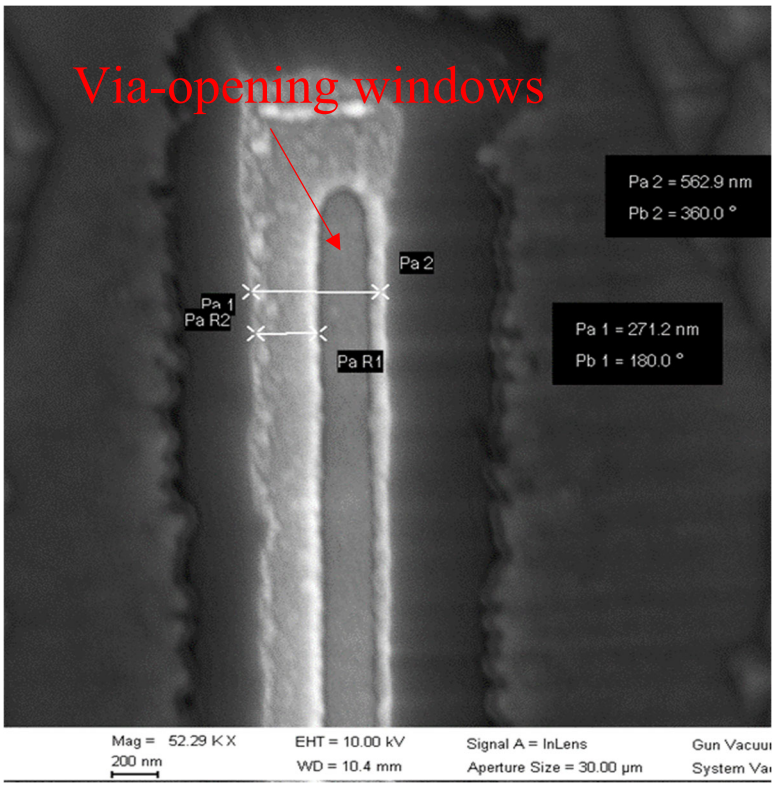

Figure 4-23. The via-opening windows showing the opened via on the top of nGaN.

4.4 FinFETs Electrical Characterizations

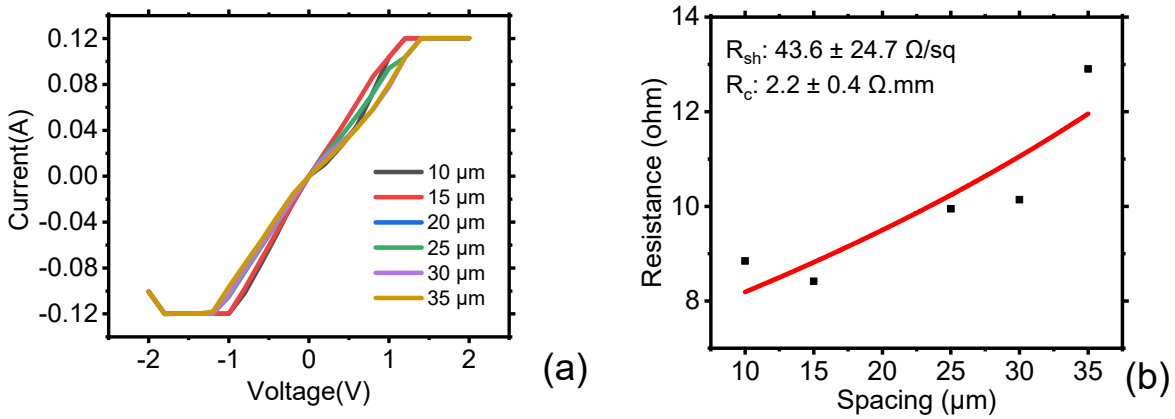

Figure 4-24. (a) CTLM results of top n^+-GaN (b) corresponding data fitting for extraction R_{sh} and R_c.

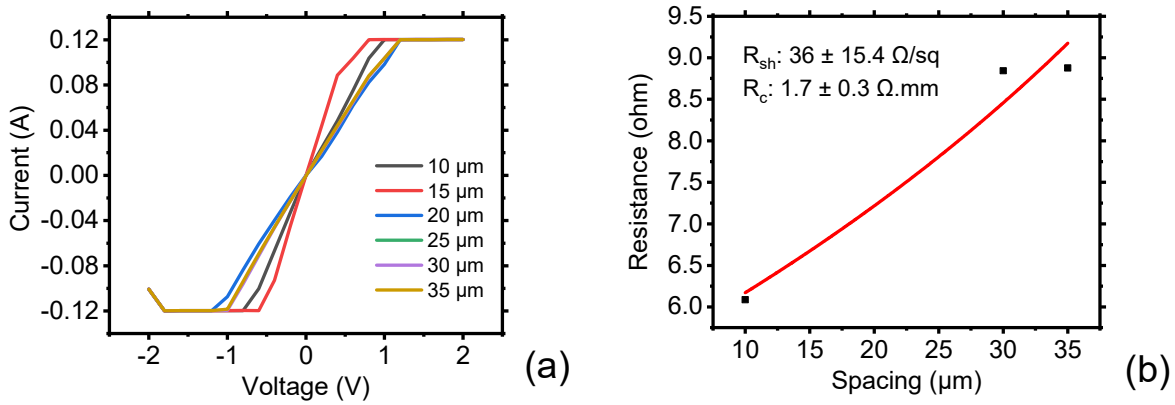

Figure 4-25. (a) CTLM results of bot n^+-GaN (b) corresponding data fitting for extraction R_{sh} and R_c.

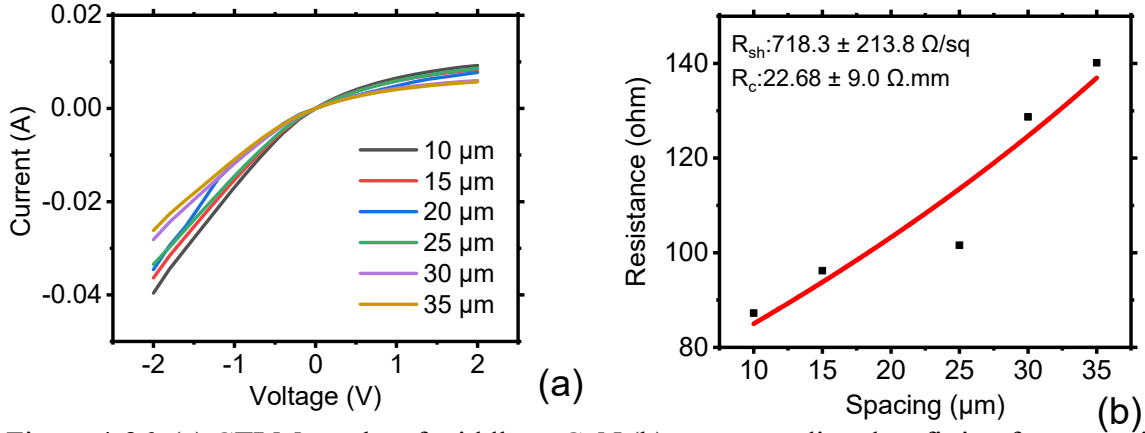

Figure 4-26. (a) CTLM results of middle n^--GaN (b) corresponding data fitting for extraction R_{sh} and R_c.

The sheet resistance and contact resistance of top and bottom n^+-GaN are shown in Fig. 4-24 and Fig. 4-25. Despite the fact that the sample was not subject to the high temperature annealing after ohmic metal deposition, the top n^+-GaN and bottom n^+-GaN were highly conductive. The extracted R_{sh} was 36.0~43.6 Ω/sq and R_c was 1.7 ~ 2.2 Ω.mm. On the other hand, the n^--GaN drift layer was not conductive as the top or bottom n^+-GaN. The extracted R_{sh} and R_c, was 718.3 Ω/sq and 22.68 Ω.mm. All the R_{sh} and R_c are extracted at 0.2 V.

The FinFETs gate transfer characteristics was performed. No gate modulation was observed from the FinFETs. In order to understand the origins of the lack of gate modulation, the drain bias of the FinFETs is kept at 0 V to investigate the gate-to-source leakage. It was found that

at very small gate bias < 0.3 V, the gate-to-source leakage current increased dramatically. The high leakage current at the small drain and gate biases have prevented the FinFETs from showing the gate modulations.

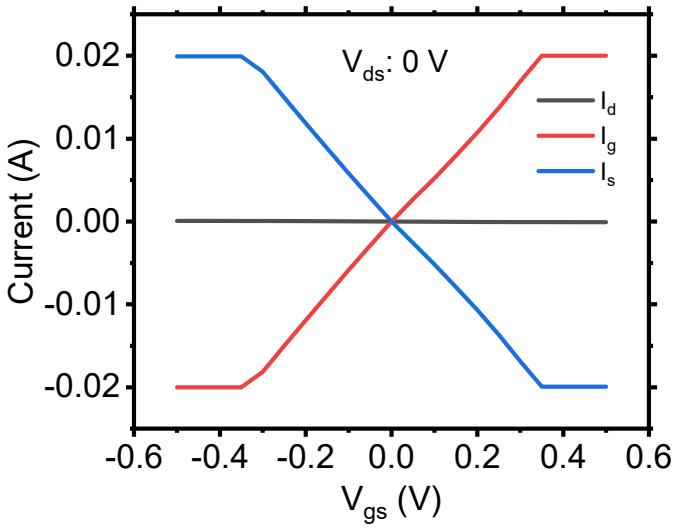

Figure 4-27. Gate transfer characteristics at V_{ds}= 0 V

In the vertical FinFETs in this study, the gate-to-source current blocking capability is determined by the SiN_x insulator deposited by PECVD prior the source metals depositions. The metal-insulator-metal (MIM) between the source and gate metals [14] testing structure as shown in Fig 4-28 (a), which was fabricated on the same sample as the FinFETs, was tested to voltage/current blocking capability of the SiN_x insulator. The measured results at different locations of sample indicate that the majority of MIM structures show a leaky behavior, as shown in Fig. 4-28. < 30% of the MIM structure show the desired voltage blocking capability with a low leakage current (< nA). These results indicate that the gate-to-source leakage observed in the gate transfer characteristics could be the results of uniform/failure of SiN_x insulator deposition. The proposed leakage current path in the fabricated FinFETs is illustrated in Fig. 29 (a).

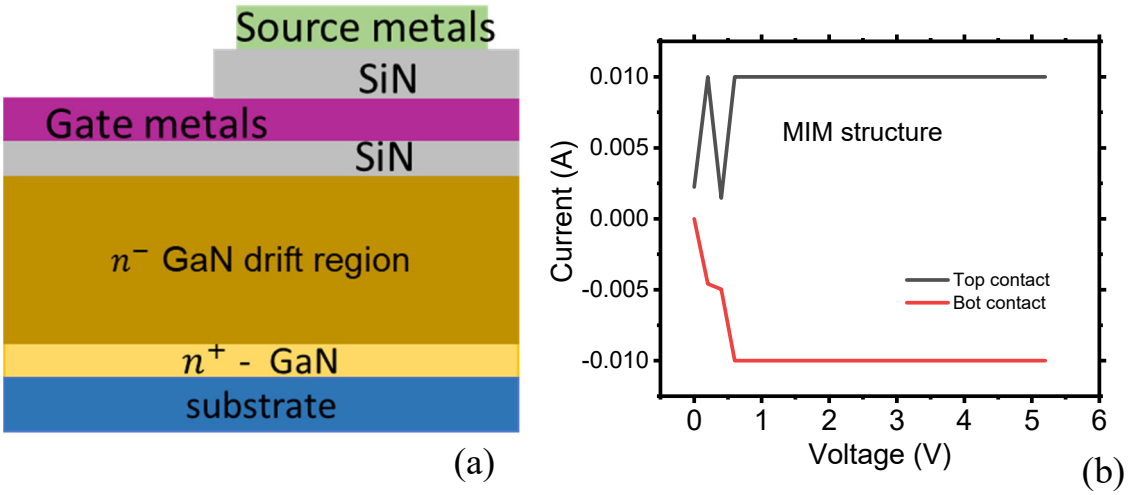

Figure 4-28. Metal-insulator-metal structure measurement results

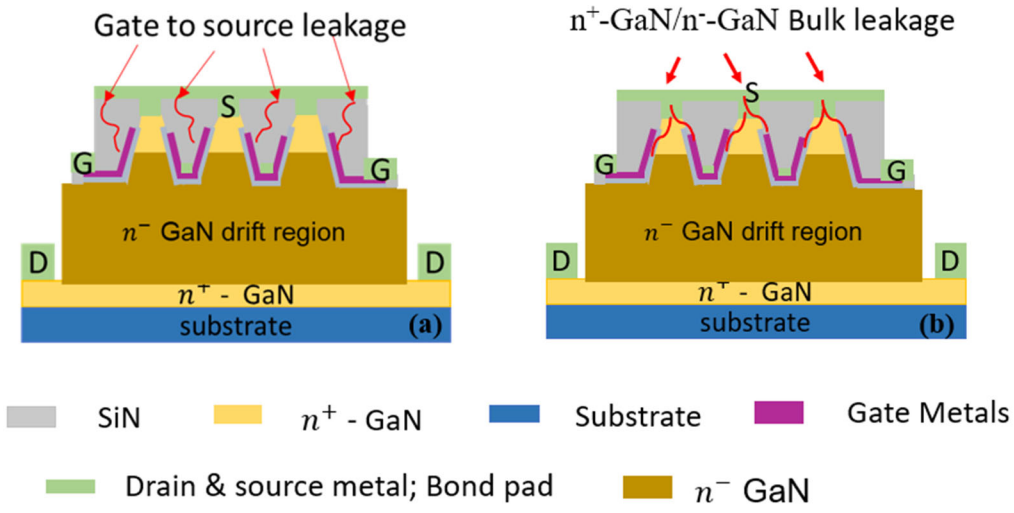

Figure 4-29. Possible leakage current path in the fabricated FinFETs (a) leaking through the SiN_x passivation (b) leaking through the n^+-GaN/n^--GaN.

On the other hand, another possible mechanism could be the uniform/failure of SiN_x gate dielectric. The dielectric is much thinner compared to the passivation. The coverage on the FinFETs sidewall was not uniform resulting the direct gate metal contact with n^+-GaN/n^--GaN. As measured from the CTLM results on the n^--GaN, it also much more conducive compared to the desired semi-insulating properties. If the gate dielectric failure on the n^+-GaN/n^--GaN region, the current leaks through the bulk GaN, as shown in Fig. 4-29 (b).

4.5 Summary

4.5.1 Conclusion

As a promising vertical device structure, as well as a building block of other novel architecture, semi-polar (11-22) GaN FinFETs is explored in the chapter. Wet crystallography etching approach was investigated to create a sub-micron Fin arrays with feature-sizes down to 200 nm that is highly-uniform and without the need of the conventional dry plasma etching of GaN. Sentaurus TCAD's 2D drift-diffusion model is used to investigate the FinFET electrical properties. The modelling shows that the narrow fin size of < 200 nm is required in order to achieve an enhancement mode operation. The doping concentration of the n-$^{-}$GaN drift region, and the thickness of the gate dielectric also play an important role in achieving a positive threshold voltage.

In order to fabricate the FinFETs, multiple process modules are proposed and investigated. The electron beam lithography process for sub-micron fin sizes was optimised. The semi-polar GaN fin arrays formation was accomplished using the hydroxide-based wet crystallography etching approach. A photoresist planarization technique was used to achieve the all-around gate structure in the FinFETs. FinFETs device fabrications included integrating each individual process module. Electrical characterisations were performed on the fabricated FinFETs. However, no gate modulation was achieved, and a high gate-to-source leakage current was measured. The electrical measurements on metal-insulator-metal test structure reveal a poor voltage blocking capability on the SiN_x insulator between the gate and source metals. The possible leakage current paths are illustrated. Nonetheless, this research lays the groundwork for future advancements in the crystallographic wet etching approach to realise the FinFETs on the sub-micron scale and highlight the potential of nanostructures patterning by wet etching approach.

4.5.2 Recommendations for Future works

4.5.2.1 process optimisation for the vertical semi-polar (11-22) FinFETs

In the fabricated semi-polar (11-22) FinFETs, a source to gate leakage current and non-uniform electrical characteristics of metal-insulator-metal structure was observed. This step represents the most challenging step in the whole fabrication process. As insulator between the gate and source electrode is necessary and cannot be avoid. In the future fabrication approach, the deposited insulator should have the high uniformity and high electrical insulating properties. Optimisation on the FinFETs sidewall coverage would be necessary. The ICPCVD deposition methods could be tried. On the other hand, for the purpose of insulating between the different electrodes. The photoresist itself could be used as an insulating layer, which has demonstrated in the vertical nanowire GaN transistors [18]. This concept can also be used in the vertical semi-polar (11-22) FiNFETs fabrications and with no need of worrying the quality of deposited thin films.

4.5.2.1 Transistor operation on the lateral FinFETs

The innovative fabrication procedures in this work might make it challenging to fabricate vertical semi-polar (11-22) FinFETs. On the other hand, it would be much easier to fabricate the lateral FinFETs based on this novel crystallographic wet etching approach. Fig. 4-31 demonstrated the achieved < 100 nm top Fin features, and Fig. 4-32 shows a proposed lateral semi-polar (11-22) GaN FinFETs, with the future designed of epitaxy wafer nGaN/pGaN thickness and doping control. The enhancement operation is easily to achieved. Fig. 4-33 demonstrated a proof-of-concept lateral devices on the large scale with V-groove opening of

1.5 μm. The gate modulation is achieved with I_{ON}/I_{OFF} ratio $>10^8$ and maximum drain current of 15 mA/mm.

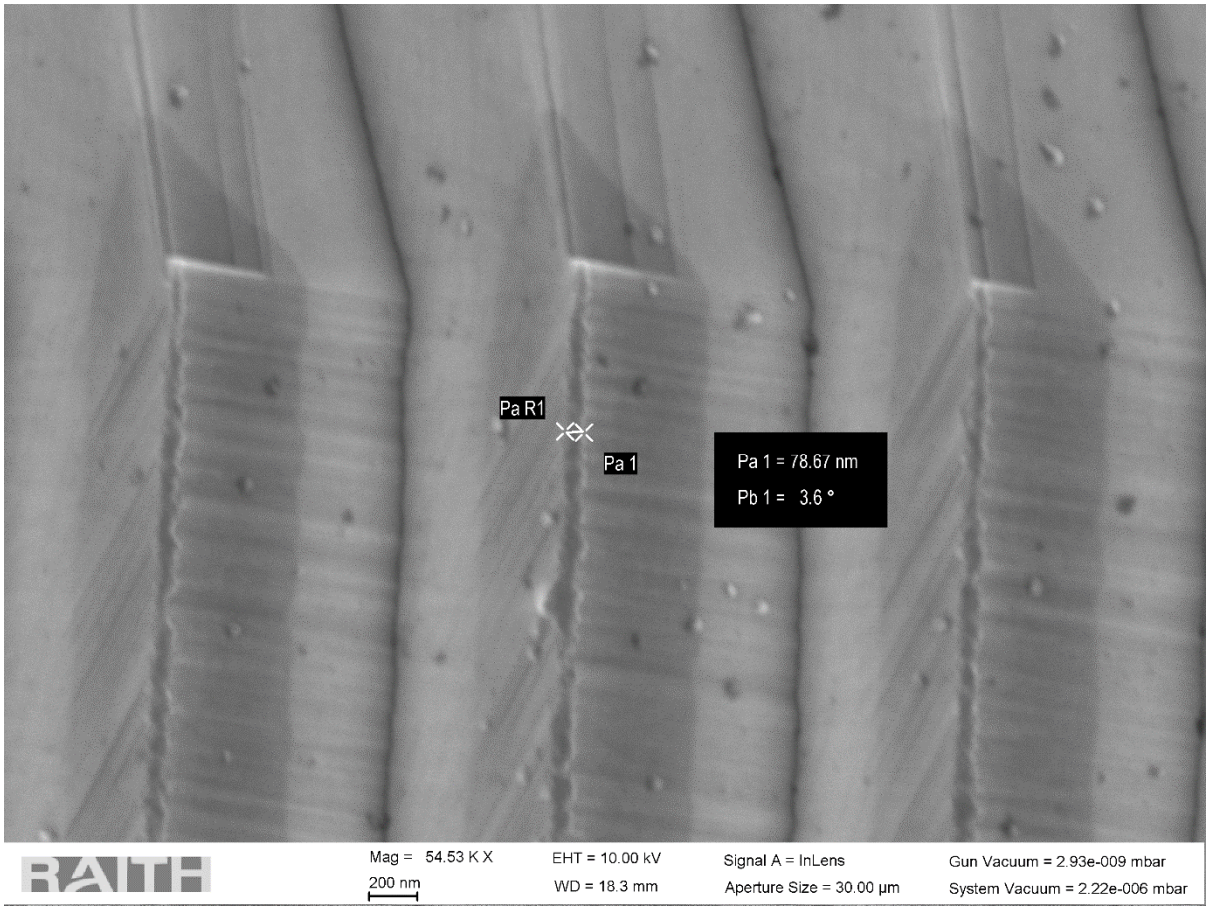

Figure 4-30. 100 nm Fin arrays with size < 100 nm.

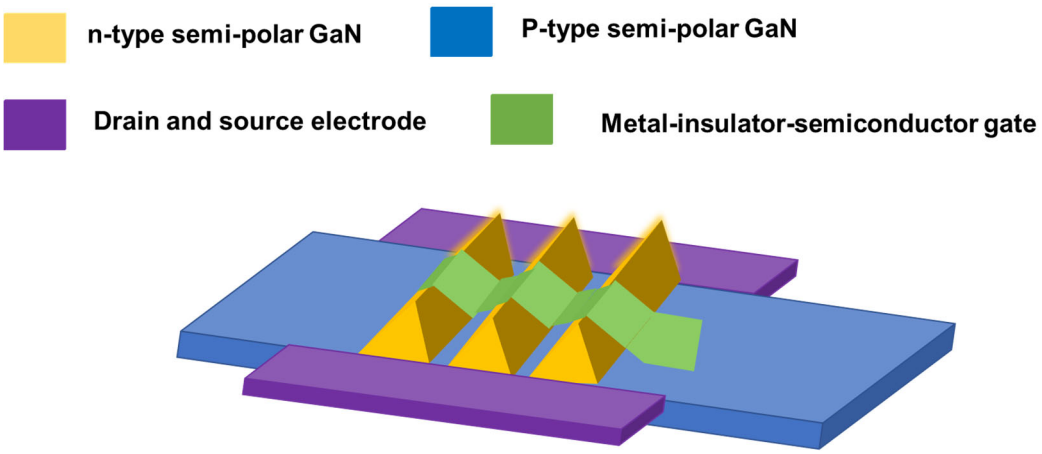

Figure 4-31. Example of lateral nanowire semi-polar GaN transistor with multiple V-groove.

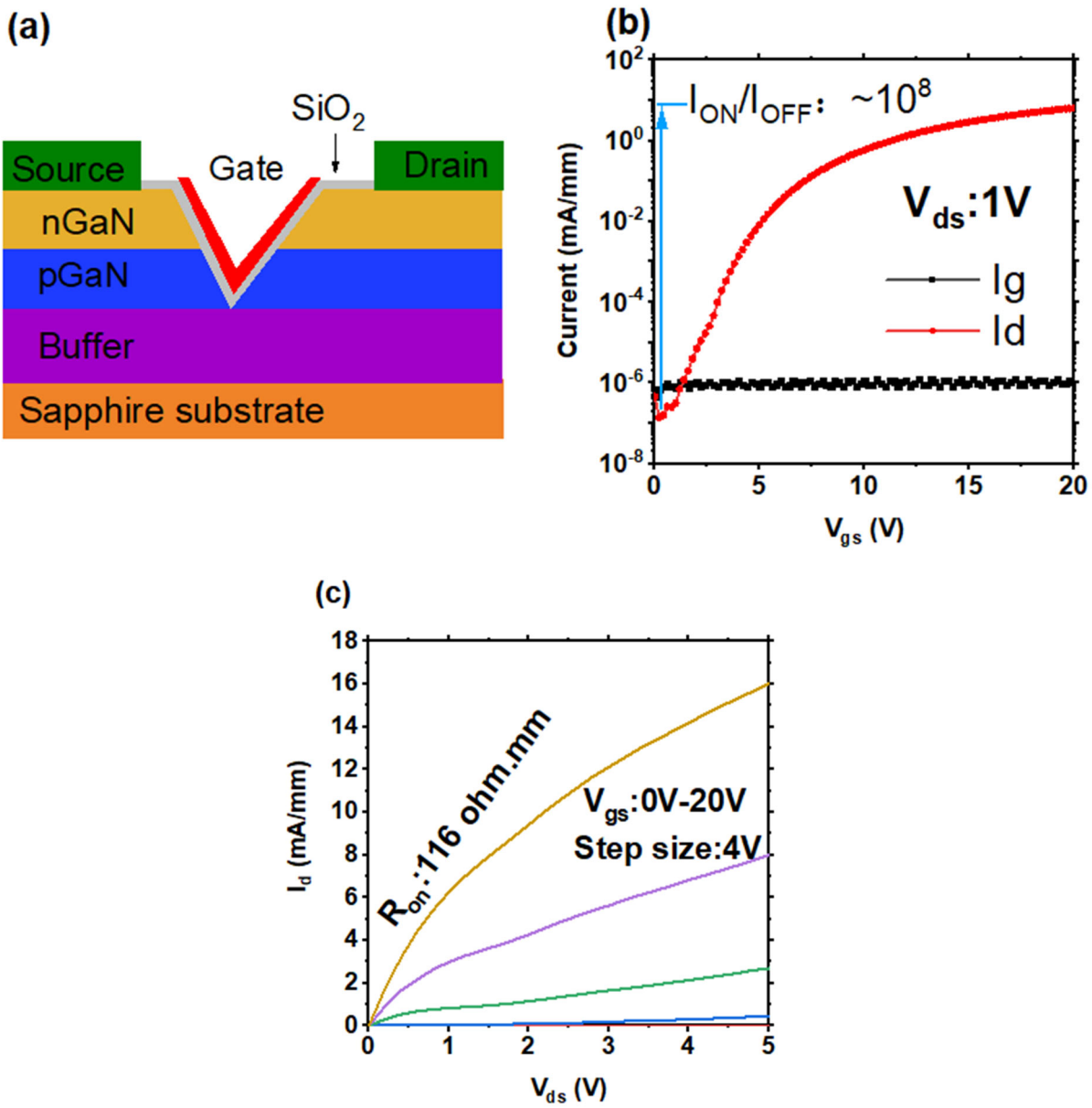

Figure 4-32. Primary results of lateral semi-polar GaN transistor with single V-groove (a) device structure (b) gate transfer characteristics and (c) output characteristics.

4.5.2.2 Application beyond the transistor.

Despite the crystallographic wet etching in this project was utilized to create conduction sidewall for the transistor operations. However, this wet etching technique can be applied to other applications that beyond the transistor. Fig.4-33 shows an example of wet etching window with self-limited etched profile. Currently, the project has only explored the trench opening on the mask geometries of rectangular shape, as shown in Fig. 4-34 (a). There are a

wide range of wet etching windows such as circular and hexagonal shapes are awaiting to explored. Also, it is noted in this work, semi-polar (11-22) GaN is used. However, this does not prevent to explored others semi-polar or non-polar GaN orientations.

On the modern selective area epitaxy methods [15] of III-V nanostructure arrays such as, quantum dot [16] or nanowire photonic crystals [17], typically, a plasma-dry etching of growth temple was used and followed by the subsequent selectively regrowth. Despite the dry-etching recipe may claim to be non-destructive to the substrate, the dry-etching by-products as well as other contaminations form un-cleaned etching chamber would leave on the surface, which affects the subsequent selectively epitaxy. In the crystallographic wet-etching approach, the nano patterns are solely defined by the wet-etching and the depths/angle is predictable defined by the nature of wet-etching windows opening orientations and the polarity of GaN, which allow the highly uniformity and fully controllable. The nanostructures arrays, once obtained by the pure wet-etching approach, it can be directly used for the subsequent selectively epitaxy, which significantly revolutionized the conventional nanostructures patterns process techniques.

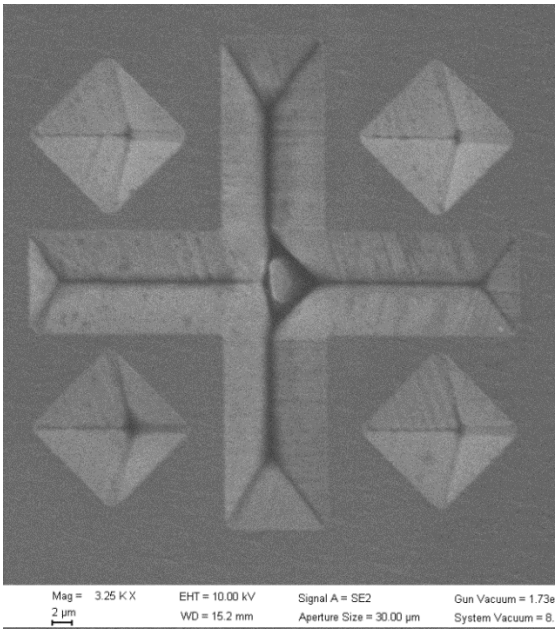

Figure 4-33. Anisotropic wet etching windows.

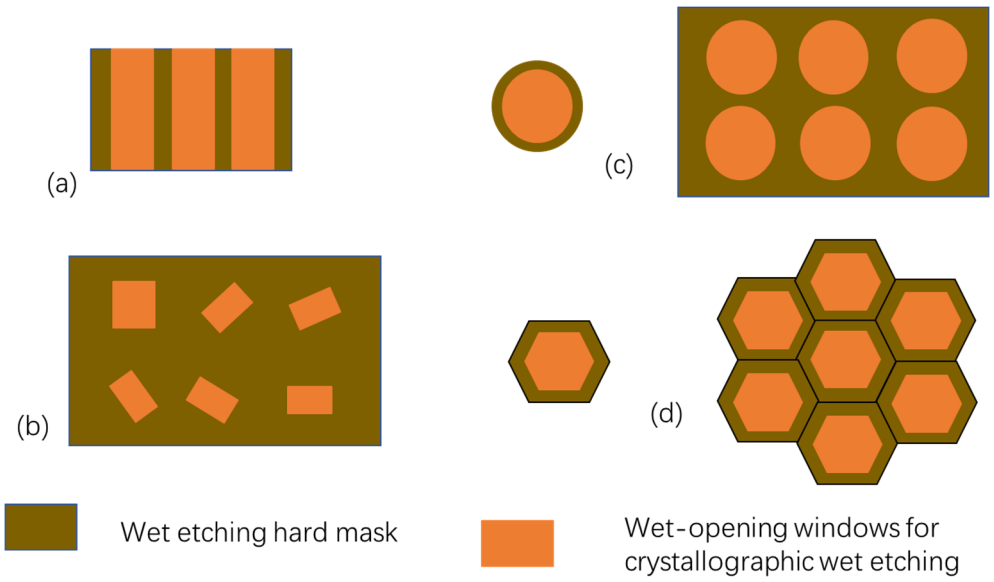

Figure 4-34. Different wet etching mask geometrics (a) rectangular shapes (b) rectangular shapes (c) circular shapes (d) hexagonal shapes.

4.7 References

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5. Fabrication and Characterization of Lateral p-channel and n-Channel GaN Transistors

5.1 Introduction

Despite the promising results on the development of lateral and vertical n-channel GaN transistors, the full potential of the high-efficiency GaN integrated circuits (ICs) is not yet achieved [1]. One of the reasons is lack of monolithic GaN complementary technology [2],[3]. For example, in a typical half-bridge converter circuit that consists of a high-side and a low-side n-channel GaN transistors, the external gate drivers that made of Si-based electronics are used [4]. The combination of the external Si-based electronics with the GaN electronics increases the system complexity as well as increases the parasitic elements in the circuitry, in which limiting the overall performance of the power electronic systems [5].

For that reason, implementation of GaN complementary metal-oxide-semiconductor (CMOS) circuitry is highly desired for the logic controls [6], [7]. To achieve this, an enhancement-mode (E-mode) p-channel GaN transistors are needed in addition to the well-established E-mode n-channel GaN transistors. However, the development of *p*-channel GaN transistors, in the past, has been hindered by: (1) low carrier concentration due to the high magnesium (Mg) acceptor activation energy of 200 meV [8] and the formation of Mg-H complexes [9], [10], (2) low hole mobility of p-type GaN [11] with typical value of < 50 $cm^2/V.s$ [12], and (3) lack of appropriate metals or conducting oxides having a larger work function than that of p-type GaN [13], [3] to reduce the Schottky barrier height [13], [14].

This chapter investigates lateral p-channel and n-channel GaN transistors on an p-GaN/UID-GaN/UID-AlGaN/UID-GaN-on-Si platform for GaN complimentary technology, illustrated in Fig. 5-1. Wafer epitaxy structures, p-type ohmic contact optimization, fabrication and

characterization of the p-channel and n-channel GaN transistors are discussed in the rest of the section.

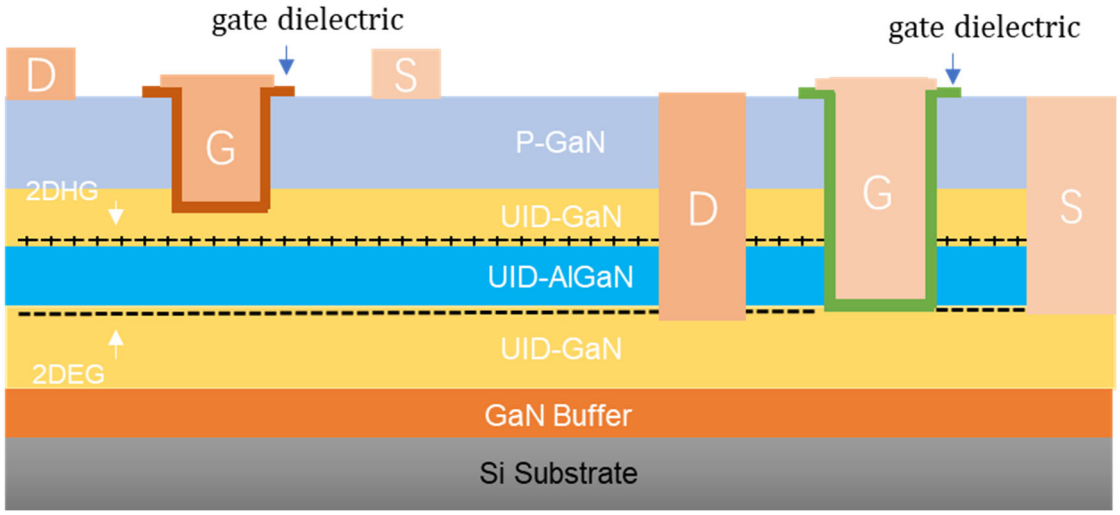

Figure 5-1. Lateral p-channel and n-channel GaN metal-insulator-field effect transistors on p-GaN/UID-GaN/UID-AlGaN/UID-GaN hetero-structures.

5.2 E-mode p-channel Metal-Insulator-Semiconductor Field-Effect Transistors (MISFETs) Fabrication

5.2.1 Epitaxial Layers

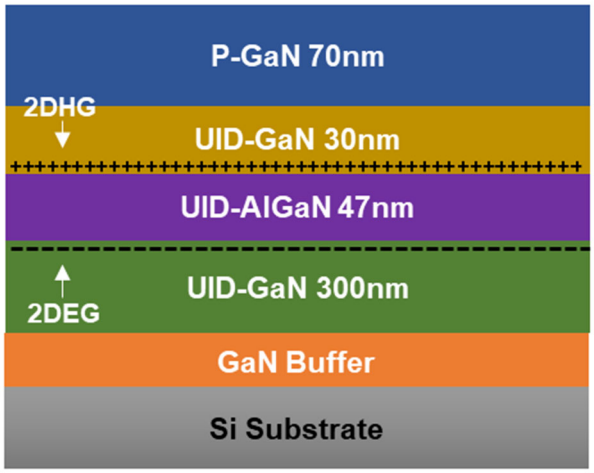

Figure 5-2: Schematic of the wafer used to fabricate the p-channel devices.

The wafer structure is shown in Fig. 5-2. It was grown by Nippon Telegraph and Telephone Advanced Technology Corporation (NTT-AT) on the 3-inch Si (111) substrate using metal-

organic chemical vapor deposition techniques (MOCVD). The GaN is growth on the Ga-polar (0001) direction and the detailed epitaxial structure is as follows: 70 nm p-GaN (Mg: 6×10^{19} cm^{-3}), 30 nm un-intentionally doped (UID)-GaN, 47 nm UID-$Al_{0.23}Ga_{0.77}N$, 300 nm UID-GaN, and 3.9 µm carbon-doped strain relief buffer layer. The purpose of the 70 nm heavily doped p-GaN layer is to facilitate the formation of p-type ohmic contacts and the 30 nm UID-GaN is to accommodate the back-diffusion/inter-diffusion effect [15], [16], [17] of Mg during the growth process and to reduce the doping impurity scattering's impact on the 2-dimensional hole gas (2DHG) channel. The secondary ion mass spectrometry measurements (performed by the wafer supplier) suggest a gradually reduced Mg profile with an Mg dopant level of $< 2 \times10^{17}$ cm^{-3} in the UID GaN layer 5 nm from the GaN/AlGaN interface. The 47 nm UID-$Al_{0.23}Ga_{0.77}N$ is to induce the 2DHG and 2-dimensional electron gas (2DEG) at the GaN/AlGaN and AlGaN/GaN interfaces, respectively.

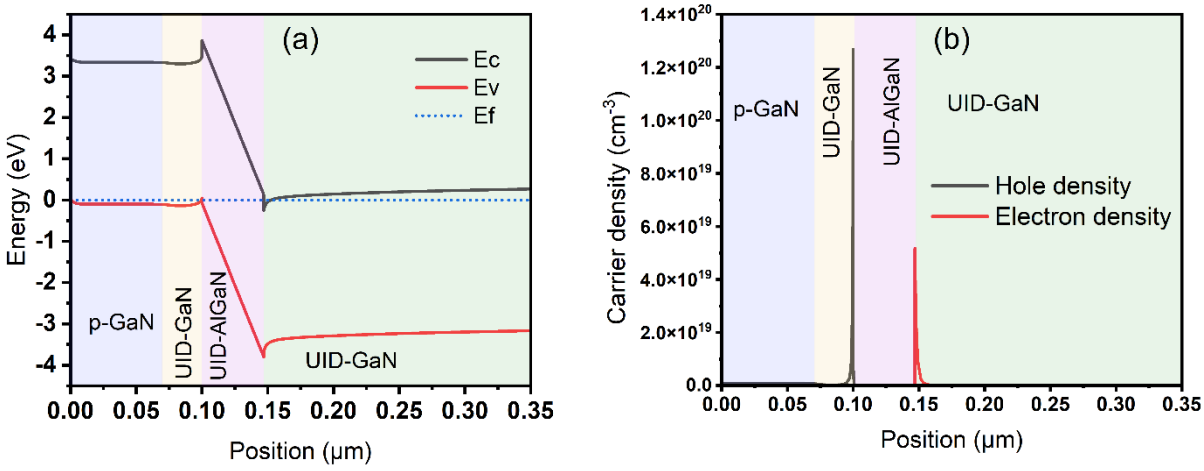

Figure 5-3: (a) Simulated band diagram of the epitaxial structure and (b) Simulated carrier density.

The technology computer-aided design (TCAD) simulated band diagram of epitaxial structure is demonstrated in Fig. 5-3 (a) with the formation of 2DHG and 2DEG is observed at GaN/AlGaN interface and AlGaN/GaN interface. Fig. 5-3 (b) shows the simulated hole and electron density at the heterojunction interface. The 2DHG and 2DEG sheet density from the simulation was ~ 3.5×10^{13} cm^{-2} and ~ 2.5×10^{13} cm^{-2}, respectively.

5.2.2 P-type Ohmic Contact Optimization

For the fabrication of p-channel transistors, a p-type GaN ohmic contact is needed for the source and drain contacts. In this project, two types of metal scheme were tried to establish the ohmic contacts for the p-type GaN, namely Ni/Au metals scheme and Pd/Ni/Au scheme. For the Ni/Au metals scheme, the Ni/Au (20 nm/20 nm) were deposited on the p-type GaN of the epitaxy wafer described in Section 5.2.1. Prior to the metal deposition, a 25s O_2 plasma step to remove the residual photoresist and 1 min HCl:H_20 (1:1) wet treatment to remove the surface oxide were performed. The sample was then annealed at 535 ℃ in N_2:O_2 (4:1) environment for 5 mins to form the NiO_x [18]. In this approach, a large work function conducting p-type NiO_x semiconductor was formed, resulting the reduced barrier height to the p-GaN and subsequently established the ohmic contacts to the p-GaN. In order to characterize the p-type ohmic contact, linear transmission line method (LTLM) as described in Section 3.4.1 was used. The current-voltage characteristics of the p-type contacts measured from the LTLM are demonstrated in the Fig.5-4 (a). The p-type contacts show an ohmic behavior. A contact resistance (R_c) of 104.8 Ω.mm and sheet resistance of 69 kΩ/sq were extracted from the LTLM.

In the full transistor fabrication process integration, plasma-based surface passivation and via-opening are typically required. However, the effect of the plasma-processing on the p-type ohmic contacts is not well reported. To study the effect of the plasma deposition and the plasma etching on the p-type GaN ohmic contacts, a 100 nm of SiN_x was deposited using deposited using plasma enhanced chemical vapor deposition (PECVD) after the Ni/Au ohmic contact formation. Via-opening were defined using photolithography and etching using reactive ion etching (RIE) to access the p-type contacts in the LLTM.

The deterioration in the p-type ohmic contacts electrical characteristics was observed after the passivation and plasma etching steps. Unlike the ohmic behavior observed in the LTLM I-V

characteristics before the passivation and plasma etching steps, a rectifying behavior was observed in the I-V characteristics after the plasma steps as shown in Fig. 5-4 (b). The degradation observed in the I-V characteristics suggests that the plasma steps introduce plasma damage to the p-type contacts.

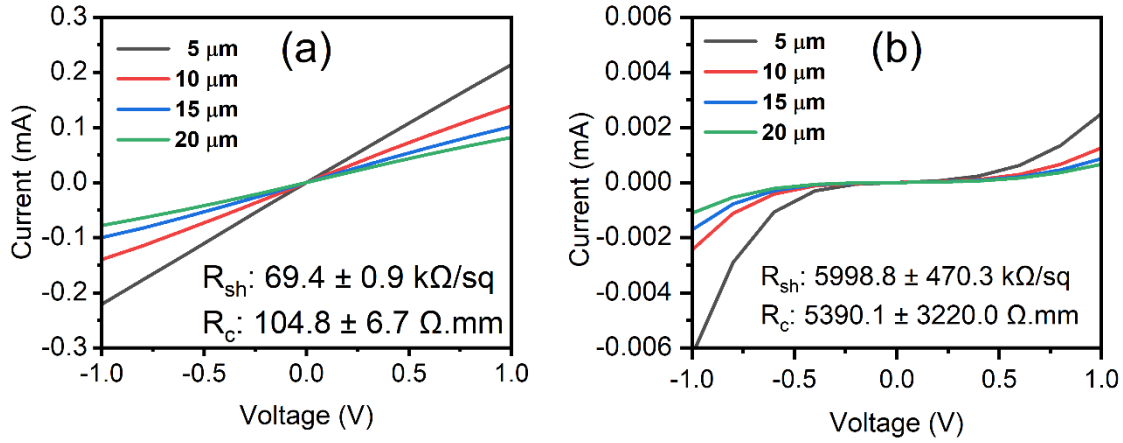

Figure 5-4. The LTLM I-V characteristics of Ni/Au (20 nm/ 20 nm) p-type ohmic contacts after thermal annealing (a) before and (b) after SiNx passivation and via-opening plasma etching.

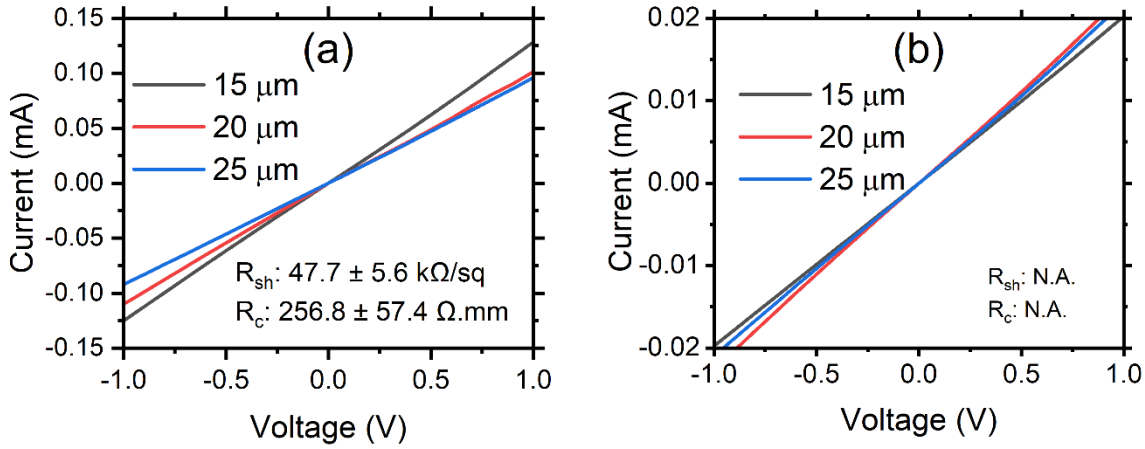

Figure 5-5. The LTLM I-V characteristics of the Pd/Ni/Au (20 nm/ 40nm/ 180 nm) p-type ohmic contacts after thermal annealing (a) before and (b) after SiNx passivation and via-opening plasma etching.

Other metal scheme (Pd/Ni/Au) was also investigated for the p-type contacts on the p-GaN layer. Metal stack of Pd/Ni/Au (20 nm/ 20 nm/ 180 nm) was deposited on the p-GaN surface and annealed at 400 °C for 5 mins in the N_2 environment. The electrical characteristics of the

LTLM structure with the Pd/Ni/Au ohmic metal scheme was shown in Fig. 5-5 (a). An ohmic behavior was also observed from the LTLM structure with the Pd/Ni/Au metal scheme. The extracted R_c and sheet resistance are 256.8 Ω.mm and 47.7 kΩ/sq, respectively. After the SiN_x passivation and the plasma etching steps, a reduction in the current was also observed from the I-V characteristics of the LTLM, as shown in Fig. 5-5 (a). In addition, it is noted that the current does not scale with the gap spacing of the LTLM structure. These show that the plasma steps affect the Pd/Ni/Au metal scheme, similar to that of the Ni/Au ohmic metal scheme.

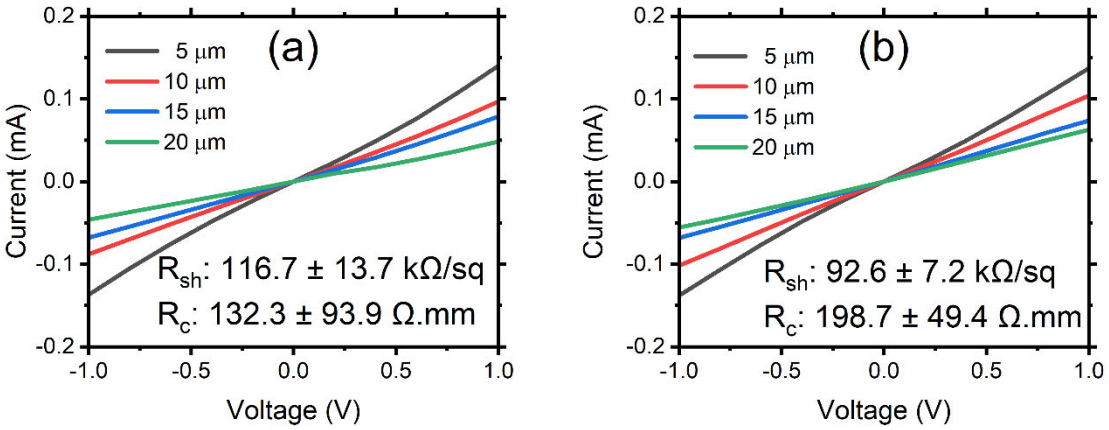

Figure 5-6. The LTLM I-V characteristics of the Ni/Au (20 nm/ 20 nm) p-type ohmic contacts with a Ni/Au protection layer (a) before and (b) after SiNx passivation and via-opening plasma etching.

To reduce the effect of the plasma steps on the p-type ohmic contacts, an additional metal stack of Ni/Au (20 nm/200 nm) to serve as a contact protection layer is introduced to the Ni/Au (20 nm/ 40 nm) p-type ohmic contacts prior to the SiN_x passivation deposition and the via-opening plasma etching steps. Fig. 5-6 compares the I-V characteristics of the LTLM structure with the contact protection layer before and after the plasma steps. It is found that the currents measured from the LTLM before and after the plasma steps are largely unchanged. These results indicate the effectiveness of the contact protection layer for reducing the plasma damage induced by the passivation and via-opening plasma etching.

Upon successfully establishment of the p-type ohmic contact scheme, a four-point Van-der-Pauw Hall measurements were conducted based on the Ni/Au ohmic metal with the additional Ni/Au (20 nm/ 200 nm) protection layer. The Hall measurements reveal a hole mobility of 6.0 cm^2/Vs, a hole sheet density of 2.7×10^{13} cm^{-2} and R_{sh} of 41.9 kΩ/sq. The extracted hole sheet density value was closely in agreement with the simulated value of ~ 3.5×10^{13} cm^{-2} described in the section 3.2.1. The extracted mobility value of 6.0 cm^2/Vs is also comparable with reported value in the literature, which is typically ranging from 7 cm^2/Vs to 11 cm^2/Vs based on the GaN/AlGaN structures [19], [20], [21]. The extracted R_{sh} of 41.9 kΩ/sq from hall measurements is consistent with the range of R_{sh} values extracted from LTLM structure. Note that the variation of the R_{sh} in the LTM is likely due to the uniformity of the wafer.

5.2.3 E-mode p-channel Device Fabrication Process Flow

The p-channel device fabrication process is illustrated in Fig. 5-7. First, the sample of approximately 2 cm × 2 cm size was cleaved from the 3-inch wafer described in Section 5.2.1 and followed by 3-step solvent clean process using n-butyl acetate, acetone and isopropyl alcohol (IPA), respectively.

The sample was spin-coated with photoresist (SPR350) and mesa pattern was defined by the standard optical photolithography process. The sample was then etched by a ~500 nm depth using inductively coupled plasma etching with the gas mixture of $SiCl_4/Ar/Cl_2$ to achieve mesa isolations. The sample was soaked in EKC830 photoresist stripper at 90 ℃ for 10 mins after the etching to remove the remaining photoresist.

The ohmic contact patterns for drain and source terminals were then defined by photolithography. A 25s O_2 plasma de-scum to remove any residual photoresist and 1 min $HCl:H_20$ (1:1) wet treatment to remove the surface oxide were performed before the deposition

of Ni/Au (20/20 nm) metal stack. The p-type ohmic contacts were established by thermal annealing at 535 ℃ in N_2:O_2 (4:1) environment for 5 mins. An additional Ni/Au (20/200 nm) layer was deposited on the ohmic contacts to serve as a contact protection layer to mitigate the plasma damage issue on the p-type contacts as discussed in Section 5.2.2.

After the p-type ohmic contact formation, a 100 nm SiN_x was deposited using PECVD to serve as the passivation layer. Next, gate window opening patterns were defined by photolithograph and the SiN_x was etched away using inductively coupled plasma (ICP) etching with CHF_3/O_2 gas mixture. The top 70 nm of p-GaN layer plus 15 nm of the UID GaN was recessed (total recess depth is 85 nm) on the gate window opening using ICP with a Cl_2/SF_6 gas mixture, as shown in Fig. 5-8 (a). The sample was then cleaned using photoresist stripper (EKC830) and solvents. Subsequently, the sample was dipped in HCl solution for 1 min to remove the residual ICP induced contaminations and surface oxides. A nominal 15 nm SiO_2 was then deposited to serve as a gate dielectric using PECVD. Ni/Au (20 nm/200 nm) metal stacks were then deposited as the gate metal stack.

The device fabrication was completed by the via-opening etching using RIE to access the drain, gate and source electrodes and probe-pad metal Ni/Au (20 nm/200 nm) deposition. The p-channel transistors in this study features a 50 µm gate width, 1.5 µm gate length and a 3 µm of drain to source separation. The SEM image of the fabricated p-channel transistor in this work is illustrated in Fig. 5-8. A detailed fabrication process traveller is provided in the Appendix A.

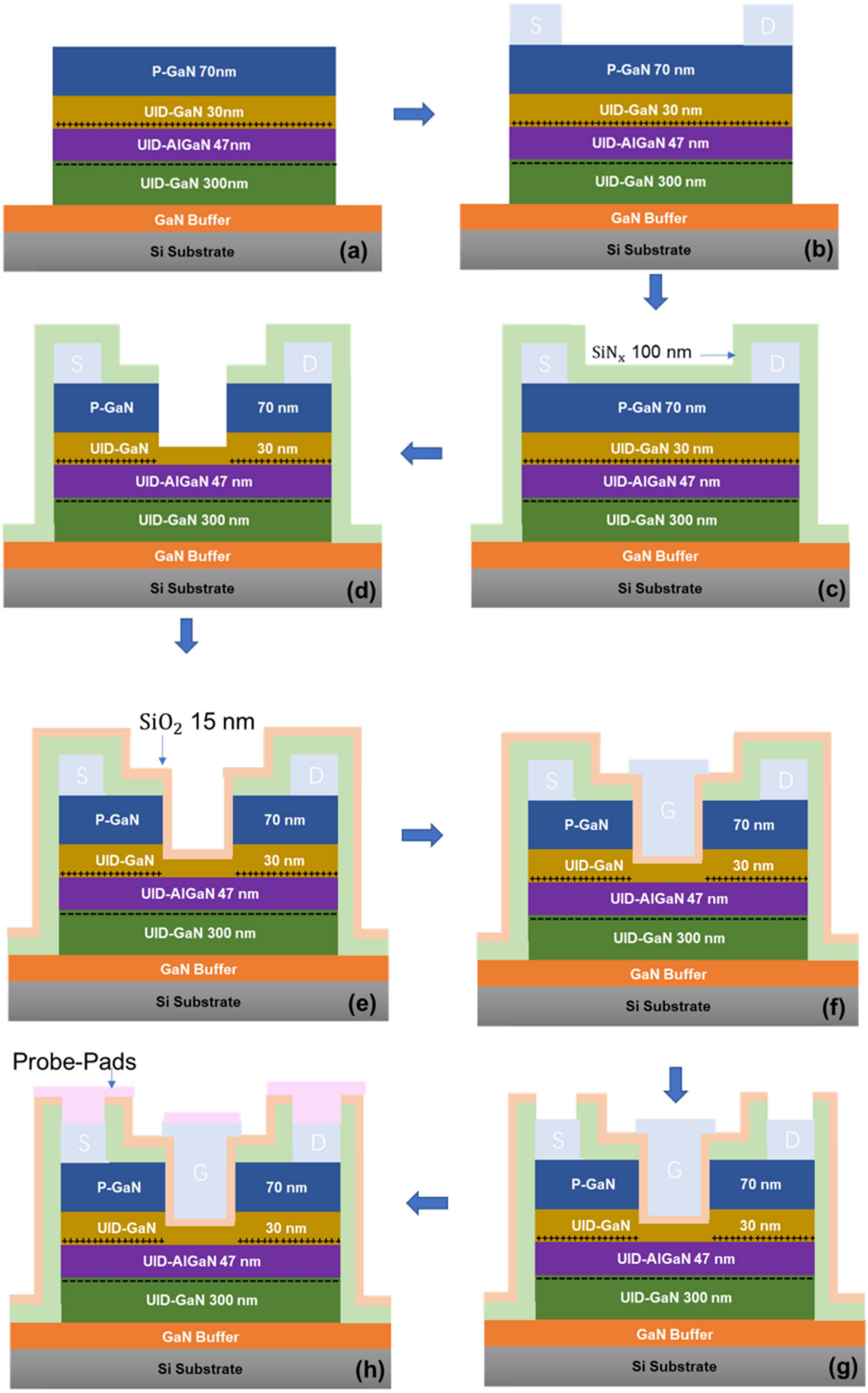

Figure 5-7. Device fabrication flow. (a) mesa isolation (b) p-type ohmic contact formation (c) SiN passivation deposition (d) Gate recessing (e) Gate dielectric deposition (f) Gate metal deposition (g) Via window opening (h) bond pad depositon.

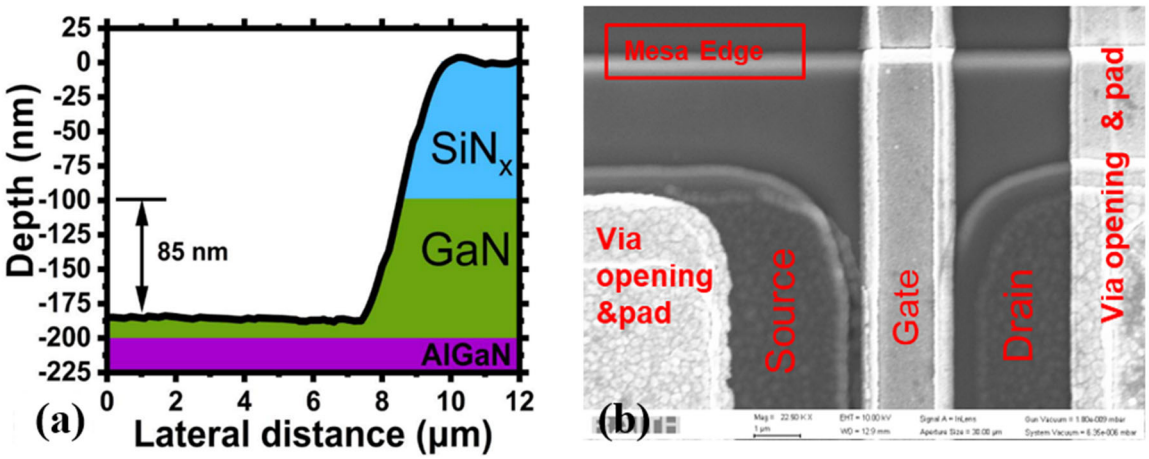

Figure 5-8. a SEM image of the p-channel transistor.

5.3 E-mode P-channel MISFETs Characterization

5.3.1 P-channel GaN MISFETs Gate Transfer Characterization

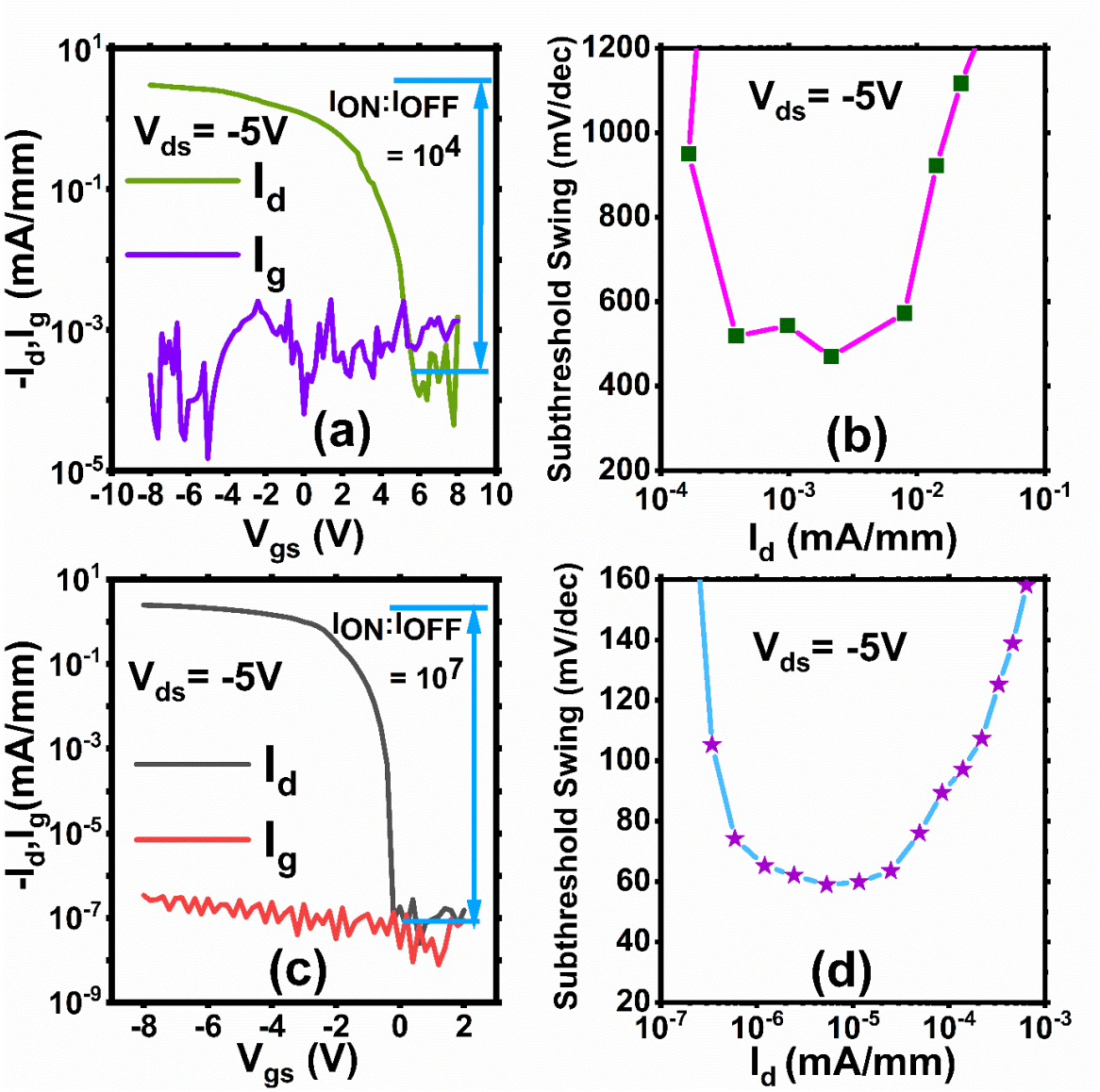

Figure. 5-9. (a) The gate transfer characteristics and (b) the corresponding subthreshold swing versus drain current plot for the p-channel MISFET without the HCl pre-treatment before the SiO_2 gate dielectric deposition. (c) The gate transfer characteristics and (d) the corresponding subthreshold swing vs drain current plot for the p-channel MISFET with the HCl pre-treatment before the SiO_2 gate dielectric deposition.

Fig. 5-9 depicts the gate transfer characteristics in log-scale of the fabricated p-channel MISFETs comparing the impacts of the HCl pre-treatment before the deposition of the SiO_2 gate dielectric. For the MISFETs without the HCl pre-treatment, a depletion mode operation is observed with a positive threshold voltage (V_{th}) of ~ +4 V, the minimum subthreshold swing (SS) was ~460 mV/dec and a high off-state leakage current with I_{ON}/I_{OFF} ratio of 10^4.

On the other hand, for the p-channel MISFET with the HCl pre-treatment, an improved I_{ON}/I_{OFF} = 10^7 and SS value of 60 mV/dec was measured. This is the first time that the room temperature theoretically limits SS value of 60 mV/dec is obtained for the GaN-based p-channel GaN transistors with metal-insulator-semiconductor gate structure. This is also the first reported HCl pre-treatment method that was used as the gate dielectric pre-treatment for the fabrications of 3-terminal p-channel GaN transistors.

It has been reported that Mg surface accumulation on GaN can easily lead to the surface oxides and a Mg-Ga-O interfacial layer [22], [23], both of which negatively impact device performance by creating a poor interface between the gate dielectric and the GaN surface. The HCl pre-treatment is efficient in eliminating ICP-induced residual contaminations [24] and the GaO and MgO surface oxides [25], [23]. As a result of the HCl pre-treatment, the SiO_2/GaN interface in the MISFET in this study is of good interface quality, resulting in a low SS of 60 mV/dec.

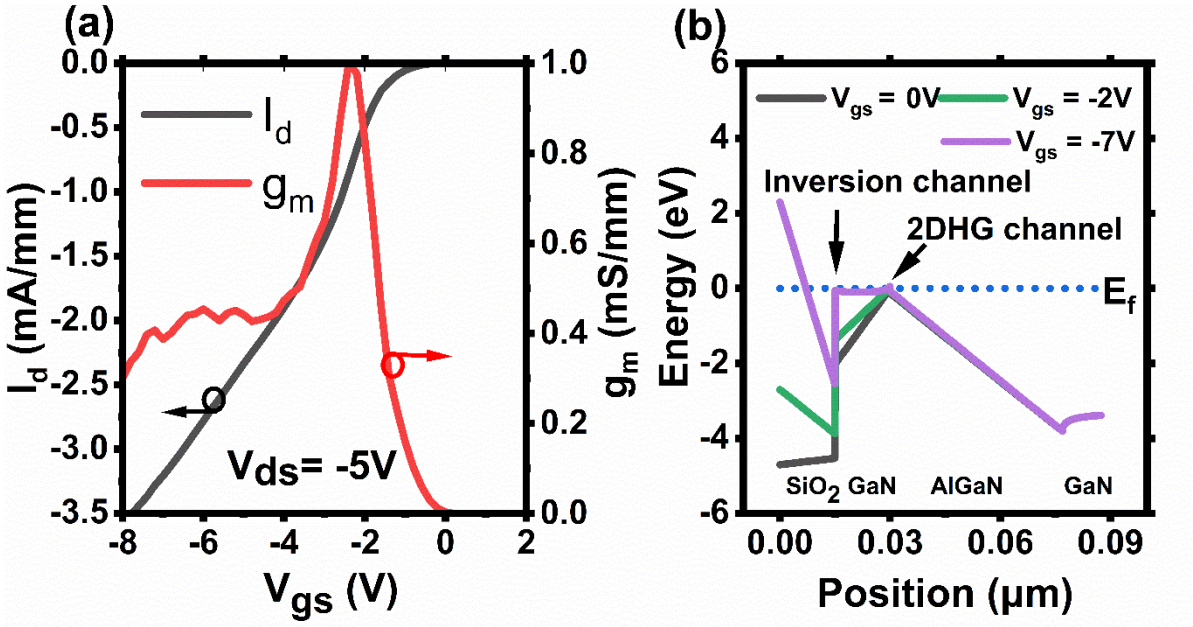

Figure 5-10. (a) Gate transfer characteristics of the fabricated p-channel MISFET in the linear-scale. (b) Simulated valence band diagram of the p-channel MISFET with varying V_{gs} using Sentaurus TCAD.

Fig. 5-10 (a) demonstrates the linear-scale gate transfer characteristics of the p-channel MISFET with the HCl pre-treatment at V_{ds} = -5 V. An enhancement operation with V_{th} of -1.53 V is extracted using the linear-interpolation method from the peak transconductance (g_m) of 1.0 mS/mm. With the further increase of V_{gs}, a second peak of g_m was observed. The similar dual g_m peak characteristics were observed in the GaN n-channel and p-channel devices previously, indicating a dual-channel modulation [26], [27].

Here, Sentaurus TCAD is used to establish the channel modulation mechanism in the p-channel MISFET. The simulated valence band diagram with varying gate bias is illustrated in the Fig. 5-10 (b). At the V_{gs} = 0V, the valence band was below the Fermi level and no channel is formed with an enhancement mode operation was achieved. With the increase of V_{gs} (negative), the 2DHG located at the GaN/AlGaN interface was formed and lead to channel conduction. The occurrence of the first g_m peak at V_{gs} ~2.5V is associated with the 2DHG channel. With the further increase of V_{gs} (negative), the valence band at the SiO_2/GaN interface will rise above the Fermi level and a MIS inversion channel is formed. The second peak g_m observed in the gate transfer characteristics of the p-channel MISFET is caused by the MIS inversion channel.

5.3.2 Muti-sweep Gate Transfer Characteristics

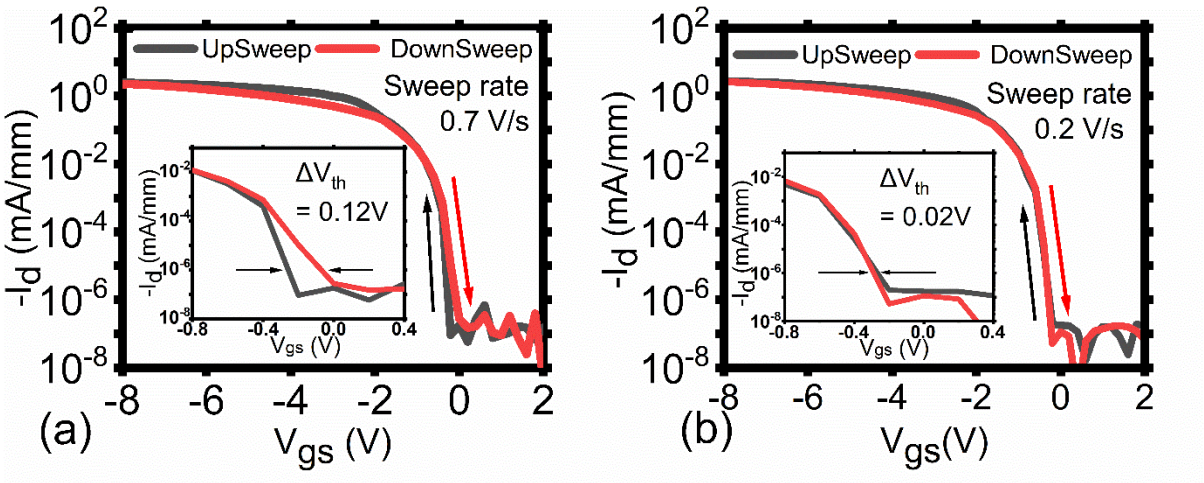

Figure 5-11. Bi-directional gate sweep transfer characteristics of the p-channel transistor.

Fig. 5-11 shows the bi-directional gate sweep transfer characteristics of the MISFET from +2V to −8 V (up-sweep) and from −8V to + 2 V (down-sweep). There is no intentional delay introduced between the up and down sweep measurements. For the sweep rate of 0.7 V/s, the transistor exhibits a positive | V_{th} | shift of 120 mV (at I_d = −1 nA/mm) at in the down-sweep compared to the up-sweep measurement. The corresponding SS for the up and down sweeps is 60 mV/dec and 107 mV/dec, respectively. The | V_{th} | shift is further reduced to 20 mV (at I_d =−1 nA/mm) when sweep at 0.2 V/s and the SS was maintained as 60 mV/dec for the up and down sweep, indicating that de-trapping of traps is a fast process. The observed V_{th} hysteresis is significantly lower than other's demonstrated GaN p-channel transistor, a hysteresis of more than | 2 V | has been reported [28], [29].

The interfacial trap density (D_{it}) of the MIS structure can be extracted from the SS by using the method from [30], [31]:

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{SS}{T} * \frac{q}{\ln(10)k} - 1\right) \quad (3\text{-}1)$$

where SS is subthreshold swing of 60 mV/decade, $C_{ox}$is gate capacitance per unit area, q is electron charge, k is Boltzmann constant and T is temperature in Kelvin.

The extracted D_{it} of the p-channel MISFET using Eq. 3-1 is 1.5×10^{10} $cm^{-2}eV^{-1}$. The typical reported MIS GaN interface trap density was in the range of $10^{12} - 10^{13}$ $cm^{-2}eV^{-1}$ [34]. The low D_{it} value at the range of 10^{10} $cm^{-2}eV^{-1}$ observed here enables the near-ideal SS in the p-channel MISFET in this study. The low D_{it} value at the range of 10^{10} $cm^{-2}eV^{-1}$ has also been reported for GaN n-channel Nanowire devices [30] using the same Eq. 3-1. It is noted that the extremely low MIS GaN D_{it} of below 10^{10} $cm^{-2}eV^{-1}$ has been achieved [60], which is an optimised PECVD deposited SiO_2 process and HCl were also used for pre-deposition treatment.

Apart from the evaluation of using Eq. 3-1, a CV measurement extraction method was also performed in this work and described in the section 5.3.3.

Fig. 5-12 demonstrates the continuous multiple-sweep gate transfer characteristics of the p-channel MISFET with a sweep rate of 0.2 V/s. The MISFET was continuously switching from the OFF-state to the ON-state with increasing negative gate bias. There is no intentional delay introduced during the multiple sweep. The maximum observed V_{th} shift at 1 nA/mm was 95 mV, indicating that very small charge trapping is induced by the repeated sweeps, highlighting the highly reliable gate modulations in the p-channel MISFET.

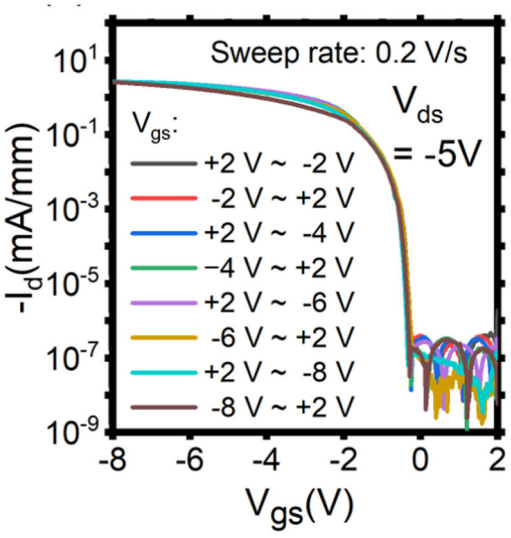

Figure 5-12. Continuous multiple-sweep gate transfer characteristics of the fabricated p-channel MISFET in the linear-scale.

5.3.3 Capacitance-Voltage (C-V) Characteristics

To further evaluate D_{it} for the MIS interface in the p-channel MISFET, multiple frequency capacitance-voltage measurements was also performed on the FATFETs with a gated area of 160 µm × 100 µm (gate width × gate length). The large gate area of FATFETs ensure that the measured capacitance is dominated by the intrinsic gate-to-channel capacitance. The capacitance of the FATFETs was measured using HP 4284 LCR meter. The oscillation level

of the AC signals was set to 50 mV and the oscillation frequency was varied from 100 kHz to 1 kHz. The DC bias was swept from 3 V to -8V at the dark room conditions.

Figure 5-13. shows the C-V measurement results of the FATFETs. A 5% dispersion/decade was observed, indicating a low interface trap density [32]. By using the Castagne-Vapaille method [33], [34], D_{it} can be calculated as below:

$$D_{it} = \frac{C_{ox}}{q}\left(\frac{C_{tot}^{lf}}{C_{ox} - C_{tot}^{lf}} - \frac{C_{tot}^{hf}}{C_{ox} - C_{tot}^{hf}}\right) \tag{3-2}$$

where D_{it} is the interface trap state density, q is electron charge, C_{ox} is gate capacitance per unit area, C_{tot}^{lf} is the total capacitance at low frequency and C_{tot}^{hf} is the total capacitance at high frequency.

The extracted D_{it} was $6.4\times10^{10}\text{cm}^{-2}\text{eV}^{-1}$ for the C-V measurements on the FATFETs. The extracted D_{it} from Eq. 3-1 and Eq. 3-2 is very close and in the range of $\sim10^{10}\text{cm}^{-2}\text{eV}^{-1}$.

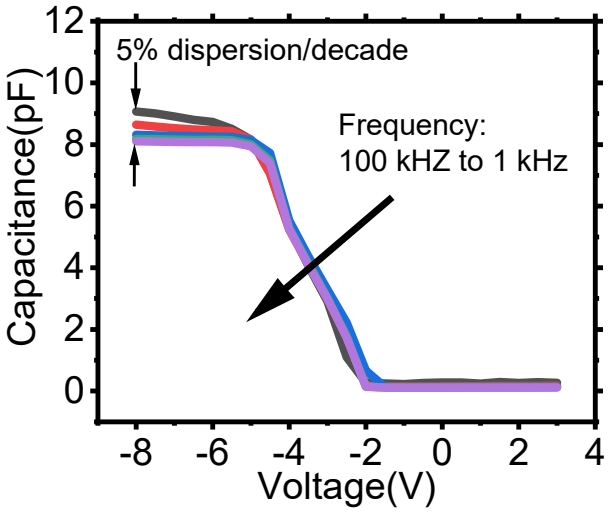

Figure 5-13. Multiple frequency capacitance-voltage measurements on the the p-channel FATFETs.

5.3.4 E-mode p-channel GaN MISFETs Output Characteristics

Fig. 5-14 demonstrates the output characteristics of the fabricated p-channel MISFET. The MISFET exhibits an output current of -4.1 mA/mm and an effective ON-state resistance of 1.0

kΩ.mm at V_{ds} = -2.5V and V_{gs} = -10V. A small non-linearity in the I-V characteristics was observed at the lower V_{ds} region. The non-linear behavior is observed at the lower V_{ds} region, the similar characteristic is widely observed in others GaN p-channel devices [35], [36], [37], [38], [39], [40], attributable to the difficulty in achieving a good p-type ohmic contacts [41].

In the p-channel MISFET in this study, the presence of the non-linear region at low V_{ds}, indicates a barrier existing on the path of the current flow during ON-state. It could be originated from the p-type contact on the Au/Ni/Au/Ni/pGaN hetero-structure or the middle of pGaN/ i-GaN heterostructure. A selectively-area p-type doping [42] or Mg post diffusion method [43] on the specific p-type contact area could be used to reduce the Schottky barrier height and improve the output characteristics of the p-channel MISFET.

Fig. 5-14 (b) shows the OFF-state characteristics at V_{gs} = 0 V. It is observed that the gate leakage current begins to rise as V_{ds} increases above -15V. This is likely due to presence of the high electric field at the gate edge which induces leakage through the gate dielectric. Above -18 V, a rapid rise in the source leakage current is observed due to the ineffectiveness of the gate to pinch-off the channel as a result of the high gate leakage current (> 1 μA/mm).

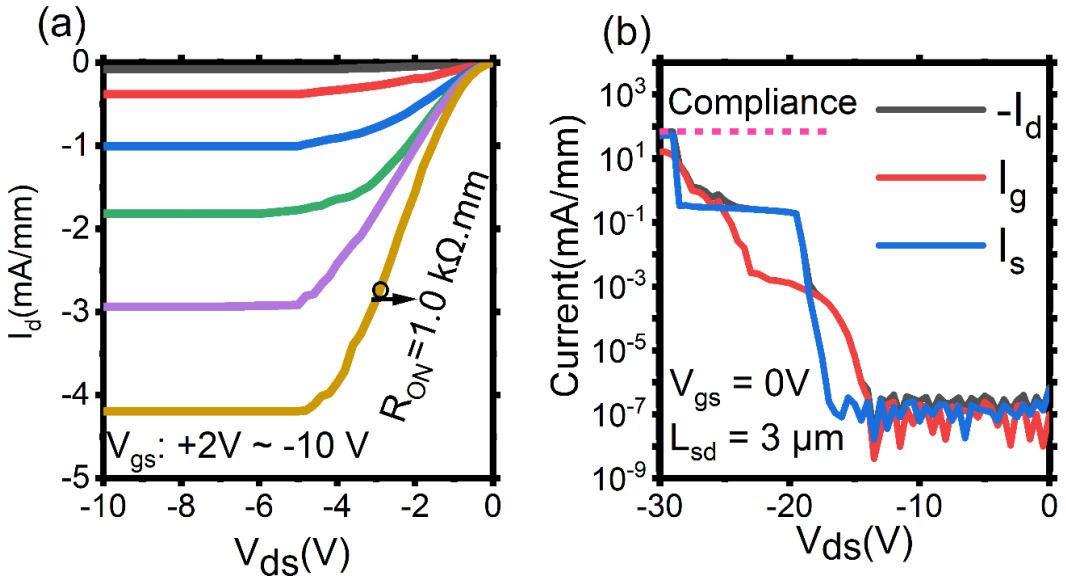

Figure 5-14. (a) Output characteristics and (b) OFF-state characteristics of the of the fabricated p-channel MISFET.

5.4 E-mode p-channel GaN Transistor Benchmark

Table 5-1. benchmarks the E-mode p-channel device in this study with other's reported E-mode p channel devices, comparing the key device parameter at V_{ds} = -5 V. The p-channel MISFET reported here represents an excellent combination of the lowest SS, high I_{ON}/I_{OFF} ratio, a high I_{ON}, and a high g_m.

Table 5-1. Benchmark of E-mode p-channel GaN transistors

Affiliations	V_{th}[a] (V)	I_{on}[b] (mA/mm)	g_m[c] (mS/mm)	I_{ON}/I_{OFF}[d]	SS[e] (mV/dec)
HRL[2]	-0.36 (V_{ds}: -0.1 V)	-1.65	N.A.	10^6 (V_{ds}: -0.1 V)	304 (V_{ds}: -0.1 V)
RWTH [12]	-0.5	-1.8	0.46	10^8	75
Cornell [44]	1.32	-9	1.5	10^4	1027
HKUST [20]	-1.7	-3.38	0.75	10^7	230
MIT [45]	0.8 (V_{ds}: -1 V)	-12	N.A.	10^5 (V_{ds}: -1 V)	800 (V_{ds}: -1 V)
AZU [46]	-0.4	-0.1	0.22	10^7	123
MIT [47]	5.5 (V_{ds}: -2 V)	-80	14 (V_{ds}: -4 V)	10^7 (V_{ds}: -2 V)	150
XD [48]	6	-8.5	1.3	10^8	130
CAS [29]	-2 (V_{ds}: -1V)	-5.1	N.A.	10^6	N.A.
This work	-0.73	-4.1	1.0	10^7	60

[a] defined at I_d = -10 μA/mm and V_{ds} = -5 V, [b,c,d,e] defined at V_{ds} = -5 V, except where otherwise stated in the brackets.

5.5 D-mode n-channel MISFETs Fabrication and Characterization

For the CMOS complementary integration, an n-channel transistor is also required. For achieving E-mode n-channel in p-GaN/UID-GaN/UID-$Al_{0.23}Ga_{0.77}N$/UID-GaN (70 nm/ 30 nm/ 47 nm/300 nm) hetero-structures: (1) gate-recessing on the gated region is needed to lift the

2DEG from the fermi level. (2) plasma etching to remove p-GaN/UID-GaN is also required to allow n-type ohmic contact formation with 2DEG on the contact region. In this study, an AlGaN self-stop etching is proposed to remove the top p-GaN/UID-GaN layer, which provides minimized damage to the UID-$Al_{0.23}Ga_{0.77}N$/UID-GaN heterostructure that induces 2DEG. The E-mode operation can be achieved with additional low power plasma partially gate-recessing [49] on the AlGaN and/or F^- implantation treatment [50]. In the next subsection, the feasibility of a self-terminated etching approach was investigated.

5.5.1 D-mode n-channel MISFETs Device Fabrication Process Flow

The n-channel device fabrication process is illustrated in Fig. 5-16. The epi-wafer used for the n-channel is the same as the p-channel MISFET as described in Section 5.2.1. First, a sample of ~ 2 cm × 2 cm size was cleaved from the 3-inch wafer and followed by a 3-step solvent cleaning process using n-butyl acetate, acetone and isopropyl alcohol, respectively.

In order to access the 2DEG channel for the n-channel, the top p-GaN and UID-GaN layers are required to be etched. The top p-GaN and UID-GaN layers was etched using ICP with a SF_6/Cl_2 gas mixture. The ICP power was 350 W, RF power was 80 W and the chamber pressure of 50 mTorr. Unlike the ICP etch recipe used for etching GaN in the p-channel MISFET described in Section 5.2.3, SF_6 gas is used together with Cl_2. The inclusion of SF_6 reduces the etch rate of AlGaN due to the development of non-volatile AlF_3 residues on the AlGaN surface [51], [52], [53]. The leads to a high etch selectivity between the GaN and AlGaN. This is critical for achieving the n-channel transistors as the 2DEG channel (carrier density) depends on the AlGaN barrier layer thickness. Fig. 5-15 shows the end-point detection using laser interferometer for the top GaN layers etching with an etch-stop at the AlGaN barrier layer.

The sample was then cleaned using the HCl solution and followed by 3-step solvent cleaning process. The sample was then spin-coated with photoresist and mesa pattern was defined by

photolithography. Mesa isolation was then achieved by etching using ICP with a gas mixture of $SiCl_4/Ar/Cl_2$. The etch depth was ~500 nm. Followed by this, the remaining photoresist was removed using EKC830 photoresist stripper 90 ℃ and the sample was subsequently cleaning using the 3-step solvent cleaning process.

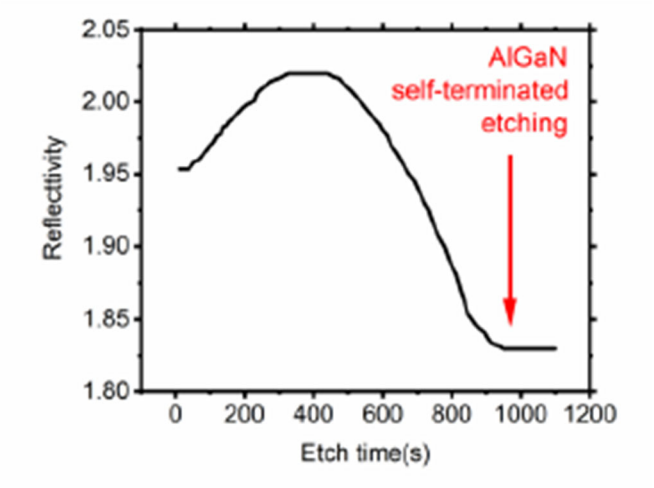

Figure 5-15. End-point detection using laser interferometer for the

The sample was then coated with photoresist and ohmic contact pattern was defined by photolithography, following by 25s O_2 plasma to remove the residual photoresist contaminations and 1 min (HCl: H_2O) wet etching to remove the surface oxide. Metal stacks of Ti/Al/Ni/Au (20/120/20/40 nm) was deposited. The n-type ohmic contacts for the source and drain were established by the metal lift-off and a thermal annealing at 800 ℃ in N_2 environment for 1 min.

After the ohmic contact formation, a nominal 20 nm SiN_x was deposited using PECVD to serve as a gate dielectric. Ni/Au (20 nm/200 nm) metal stacks were deposited as the gate metals. Next, a 100 nm SiN_x was deposited as the passivation layer. The device fabrication was then completed by the via-opening on the SiN_x passivation to access the gate, drain and source electrodes and the probe-pad metal Ni/Au (20 nm/200 nm) deposition. The process flow of the n-channel MISFETs is illustrated in Fig. 3-16. The n-channel MISFET in this study features a

50 µm gate width, 1.5 µm gate width and 7.5 µm drain to source separation. The SEM image of the fabricated n-channel MISFET in this work is shown in Fig. 5-17.

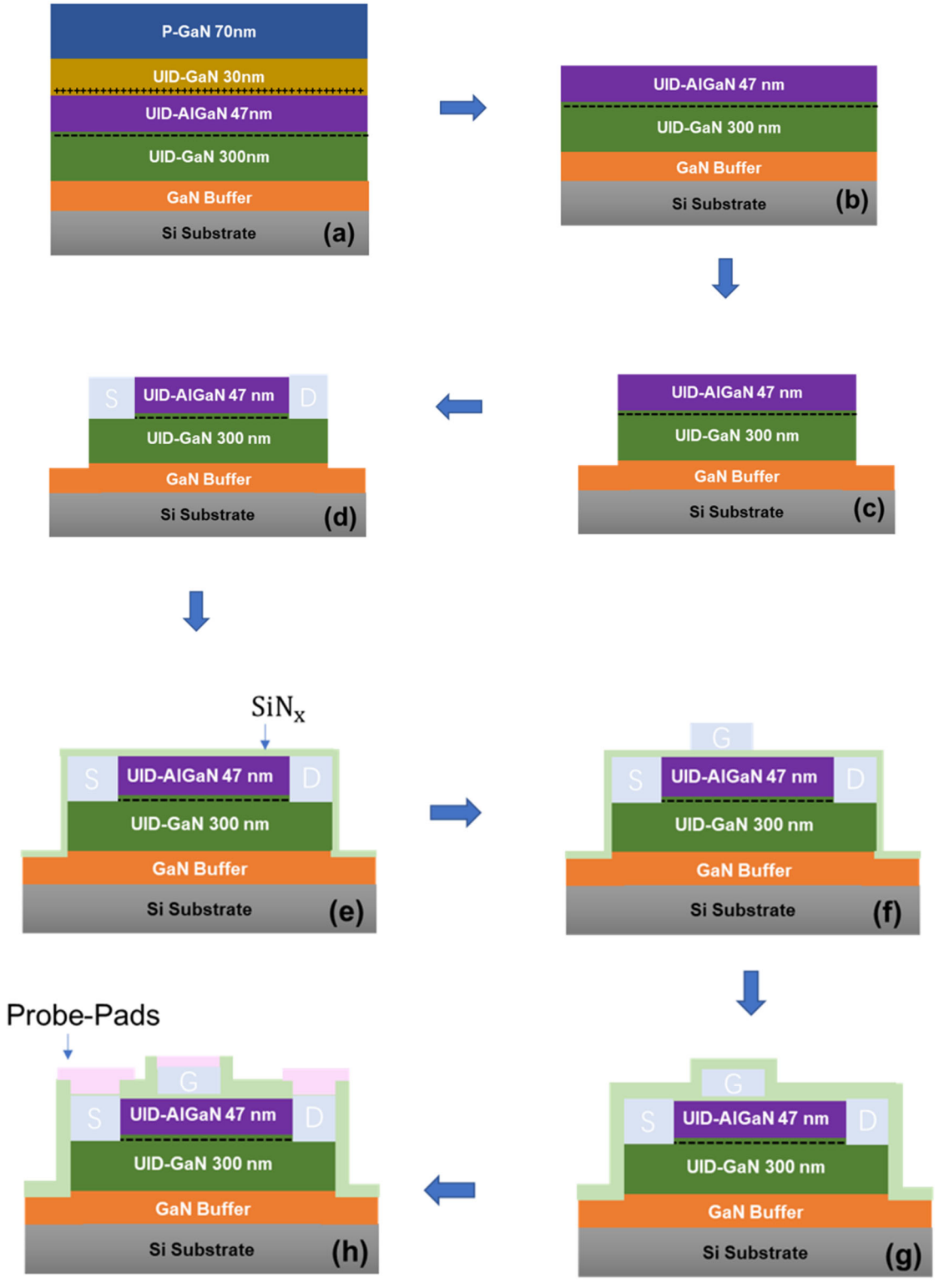

Figure 5-16. D-mode n-channel MISFET fabrication process flow.

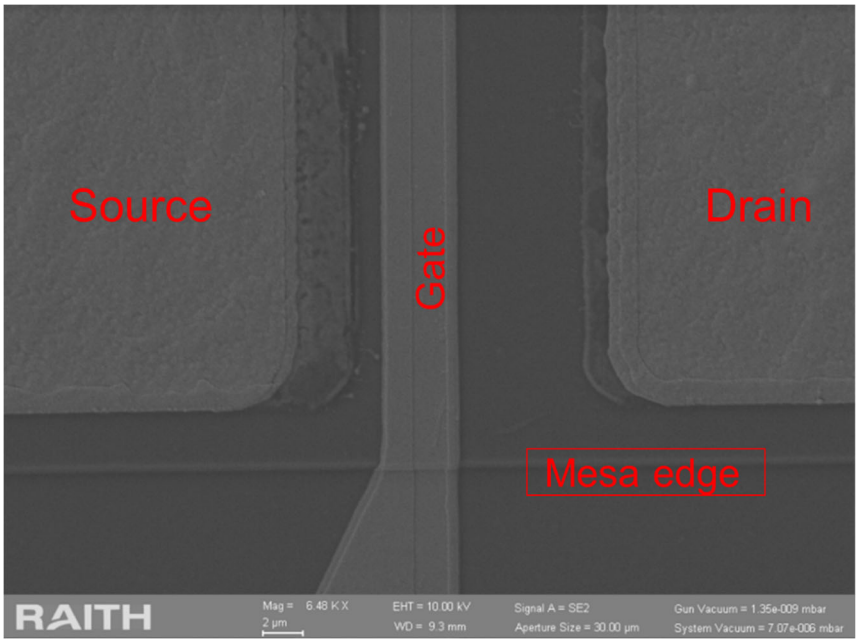

Figure 5-17. SEM image of fabricated n-channel MISFET.

5.5.2 D-mode n-channel MISFETs Characterization

Fig. 5-18 shows the measured C-V and I-V characteristics on the n-channel FATFETs (Wg:160 µm × Lg: 100 µm). Using the Eq. 3-3 and Eq. 3-4, the extracted 2DEG density from the C-V is ~ 1.0×10^{13} cm^{-2} and 2DEG mobility is 1509.8 $cm^2/(V.s)$. The high density and mobility of 2DEG are concurrently achieved, indicating the mitigated plasma damages on the 2DEG using the self-terminated AlGaN etching approach.

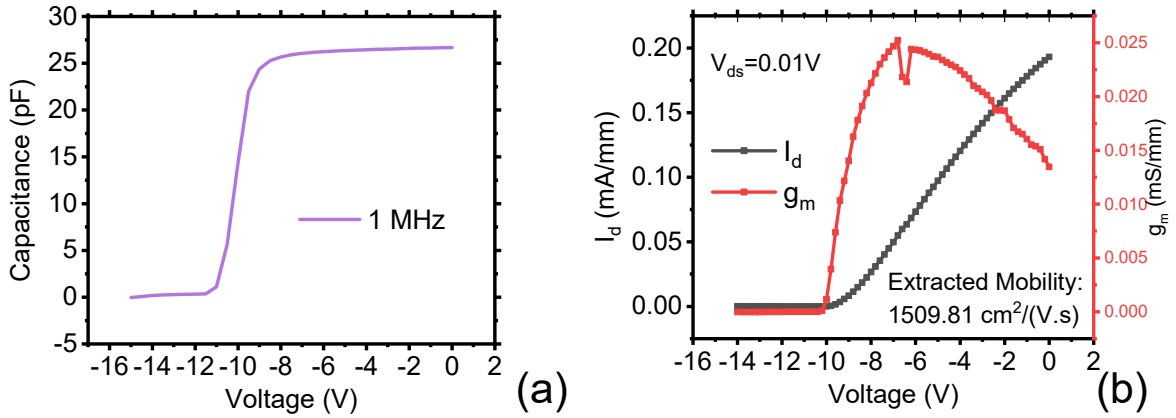

Figure 5-18. the n-channl FATFETs' (a) capacitance-voltage characteristics (b) current-voltage characteristics.

$$n_s(V_g) = \int_{-\infty}^{V_g} C \cdot dV_g \quad (3\text{-}3)$$

where V_g is the gate voltage, n_s is the sheet charge density of the 2DEG and C is the capacitance measured from C-V measurement.

$$\mu_{FE} = (\frac{L}{W})\frac{g_m}{C_o V_{ds}} \quad (3\text{-}4)$$

where μ_{FE} is the field effect mobility, W is the gate width, L is the gate length. C_o is the gate capacitance per unit area and V_{ds} is the drain-source voltage.

Fig. 5-19 (a) shows the n-type ohmic contact LTLM electrical characteristics on the AlGaN self-stop etching surface. The extracted R_{sh} of 345 Ω/sq and R_c of 1.15 Ω.mm are comparable to other's reported as-growth AlGaN/GaN structures [54], [55] with the typical value of ~ 300 to 400 Ω/sq for R_{sh} and ~ 1 Ω.mm.

Fig. 5-19 (b) shows the gate transfer characteristics of the n-channel MISFET with a peak transconductance g_m of ~ 100 mS/mm and V_{th} of -11V. A I_{ON}/I_{OFF} ratio of ~ 10^5 and SS value of 270 mV/dec are obtained from the MISFETs as shown in Fig 5-19 (c). These values are the typical reported values for AlGaN/GaN HEMTs [31] without the SiN_x pre-deposition wet etching treatment.

Fig. 5-19 (d) shows the output characteristics of the n-channel MISFET with an output current I_d of ~ 800 mA/mm and the R_{ON} of 3.8 Ω.mm. The g_m, I_d and R_{ON} are similar to the typical as-grown D-mode n-channel GaN HEMTs characteristics [56]. These results demonstrate the feasibility of self-terminated AlGaN selective etching approach to access the 2DEG located at the UID-AlGaN/UID-GaN hetero-interface without the deterioration on the 2DEG electrical characteristics in the p-GaN/UID-GaN/UID-AlGaN/UID-GaN hetero-structure wafer.

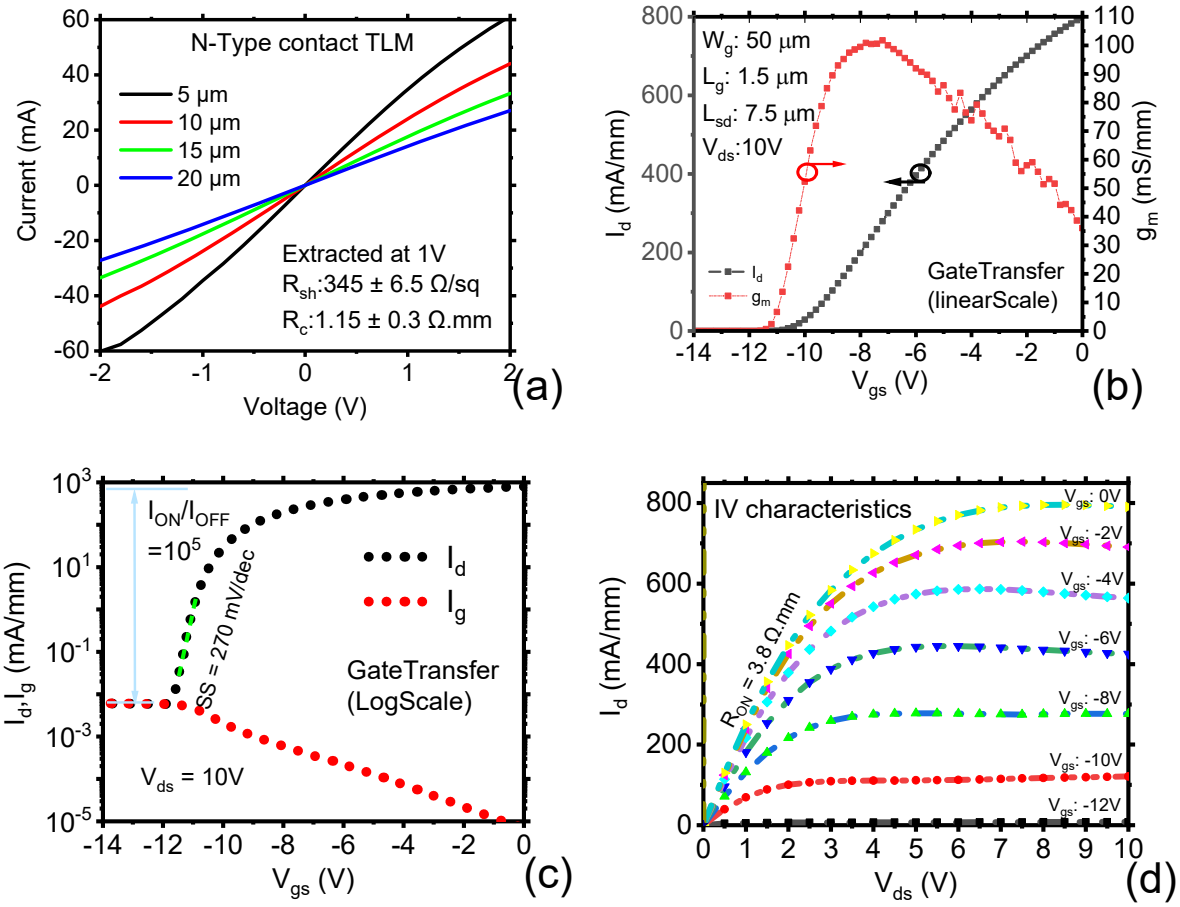

Figure 5-19. (a) The I-V characteristics of LTLM structure with Ti/Al/Ni/Au (20 nm /120 nm /20 nm /40 nm) n-type ohmic contacts after 1 min thermal annealing at 800 °C, (b) 3-terminal gate transfer characteristics of n-channel MISFET in the linear-scale, (c) 3-terminal gate transfer characteristics of n-channel MISFET in the log-scale and (d) 3-terminal output characteristics of the n-channel MISFET.

5.6 Summary

5.6.1 Conclusion

In this chapter, the lateral p-channel and n-channel GaN MISFETs were fabricated on GaN-on-Si platform. The band structure is simulated which showing the locations of 2DHG and 2DEG. The simulated 2DHG and 2DEG density values are in consistent with the measured 2DHG and 2DEG density values in the range of ~ 3.5×10^{13} cm^{-2} and ~ 1.0×10^{13} cm^{-2}. For the p-channel GaN transistor, an enhancement mode operation GaN transistor is achieved with the negative V_{th} of -1.53. The theoretical room temperature limits of 60 mV/dec subthreshold

swing value is measured, attributing to the good control of Mg back-diffusion to GaN/AlGaN interface and 2DHG confinement by back barrier AlGaN in the p-GaN/UID-GaN/UID-AlGaN/UID-GaN epitaxy structure in conjunction with the good metal-insulator-semiconductor interface with very low interface density in the range of $\sim 10^{10}\mathrm{cm}^{-2}\mathrm{eV}^{-1}$. The combination of high g_m of 1.0 mS/mm and high I_{ON}/I_{OFF} ratio of > 10^7 and a maximum drain current of -4.1 mA/mm and the very small V_{th} hysteresis of < 120 mV is achieved, which is very competitive compared to the others' reported structures.

For the n-channel GaN transistor, the investigation is conducted to accessing the n-channel region by a self-terminated dry-plasma etching approach. The depletion-mode device exhibits a V_{th} of -11 V and a high g_m of 100.0 mS/mm and high maximum drain current of 800 mA/mm, indicating the mitigated 2DEG degradation by this approach. With further developments, such technique can be integrated into the fabrication of enhancement-mode n-channel GaN transistors.

The findings in this chapter, taken as a whole, provide the foundation for developing high speed and high efficiency GaN integrated circuits in the future.

5.6.2 Future work

Despite the achieving subthreshold swing (SS) value of 60 mV/decade in the p-channel GaN transistor, for a further study on the improvement of SS and to achieve sub-60 mV/decade SS is suggested by using the ferroelectric gate dielectric materials such as ZrHfO [57] and HfO_2 [58]. The ferroelectric materials have already widely used in the modern Si CMOS technology [59] , such as Intel® Core™ 2 Extreme and Xeon® processors, to extend Moore's law. However, no study on the p-channel GaN transistor at presence. To boosting the current density, novel structures such as FinFETs or nanowire could be used. For the improvement on the OFF-

state characteristics, the field-plates structure which is widely used in the n-channel GaN transistors can be easily integrated into the p-channel device fabrication flow.

For the n-channel transistors, the fabrication optimization on the gate-recessing/ by Cl-based and/or F implantation treatments could be incorporated into the device fabrications and achieve enhancement-mode operation. Together with the overall process integration and to achieve GaN complementary integrated circuits.

5.7 References

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6. Summary

6.1 Conclusions

Due to the inherent material properties, III-nitride materials have great potentials in the field of RF, power, logic, light-emitting diodes (LEDs), and laser diodes (LDs) applications. In the ecosystem of III-nitride devices, it provides a path for monolithic integration with electronics and optical devices at the epitaxy wafer level, which other conventional semiconductor materials, such as silicon, cannot accomplish. As of now, the primary focus of GaN electronics device development is on the standalone lateral HEMTs. For greater area efficiency, vertical structures and/or monolithic integration with LEDs are preferable for higher energy efficiency and ultra-compact applications [1], [2].

The thesis presented the device design, device modeling, device fabrication, and structural and electrical characterizations on both vertical and lateral GaN transistors. Below is a summary of the transistor architectures studied in this project.

6.1.1 Vertical V-groove Semi-polar (11-22) GaN MOSFETs

The thesis presented an experimental study of the crystallographic hydroxide-based wet etching approach on the semi-polar (11-22) GaN on the m-plane sapphire substrate. Based on the formation of V-groove structures, the design consideration for the V-groove trench metal-oxide-semiconductor field effect transistor (MOSFET) fabrication was provided. For the first time, the gate modulation in the vertical channel device architecture is experimentally achieved in the GaN platform without the need for the conventional dry plasma etching technique to form the trench channel.

The 3-terminal V-groove trench MOSFET exhibits an enhancement mode operation with a positive threshold voltage (V_{th}) of 9.6 V. An on-state resistance (R_{on}) of 8 mΩ.cm^2 is achieved from the V-groove trench MOSFET which is at the same order of magnitude as typical GaN-on-foreign substrate vertical devices [3], [4]. The measured MOS inversion channel mobility was ~ 21 cm^2/Vs, in good agreement with others' reported mobility value with a similar p-GaN doping concentration level [3]. The output drain current of the MOSFET was ~ 516 A/cm^2, it can be improved by optimization of the device mask layout design for the channel conduction such as using a large area hexagon/circular layout [5]. The p-type hole concentration was evaluated by the MOSFET level 3 equation with an estimated hole concentration of ~ 1× 10^{17} cm^{-3} with an activation ratio of 2 % magnesium (Mg) activation. This value is consistent with the typically reported activation ratio (1 % - 10 %) of Mg in the p-GaN layer at room temperature [6], [7].

In the OFF-state of the V-groove MOSFET, a gate breakdown was observed at 150 V. The gate breakdown is attributable to the electrical field crowding effect at the V-groove bottom. This effect could be mitigated by trench-filling methods in order to improve the breakdown characteristics. In addition, a high leakage current from drain-to-source terminals was also observed. This is likely due to the insufficient activation of the p-GaN current blocking layer and/or the presence of a high dislocation density (10^{12} cm^{-3}) in GaN grown on the sapphire substrate. The good material quality of the semi-polar GaN is needed in the future. Nonetheless, the results presented in this thesis highlight the potential of the semi-polar GaN materials for electronic applications as well as the dry plasma etch-free vertical trench formation technique for the vertical GaN transistors.

6.1.2 Vertical Semi-polar (11-22) GaN FinFETs

Upon the demonstration of V-groove trenches using the wet-etching technique on the semi-polar (11-22) GaN, the work was further extended to apply the wet-etching technique for FinFETs with sub-micron size fin size. The vertical FinFETs design utilizes a fin structure with all-around-gate structures to modulate channel current flowing from the top (source) of the Fin downward to the drain terminal at the bottom. The FinFETs characteristics and design were initially explored using Sentaurus TCAD 2D drift-diffusion model. In the modelling study, it is found that the sub-micron fin size such as 200 nm is required to achieve a robust normally-off operation with a low off-state leakage current at the range of nA. This is due to the sloped nature of the fin sidewall achieved using the wet etch technique on semi-polar GaN. Furthermore, it was found that parameters such as the doping concentration of the n-type drift layer, the fin height, the gate dielectric thickness, and the gate metals affect the threshold voltage of the FinFETs.

The fabrication process modules for the FinFETs with an all-around-gate structure on the semi-polar (11-22) GaN were developed. The selection of hard mask materials for defining narrow fin was investigated. A smooth fin sidewall with a fin length of 200 nm was achieved using the hydroxide based wet etching and electron beam lithography. A method of using a photoresist planarization-assisted method to achieve a self-aligned process for the top gate metal etching was performed.

However, no gate modulations were achieved on the fabricated FinFETs. The current-voltage measurements on a metal-insulator-metal structure indicates that the high leakage current via the gate dielectric is the main reason for the lack of gate modulation in the fabricated FinFET. Nonetheless, this study provides useful insights and the foundation for the future development of crystallographic wet etching approach to achieve FinFET structure. With further developments, such crystallographic wet etching technique can be designed and incorporated

to the dry plasmas etched free nanostructure patterning and selectively epitaxy growth applications on a semi-polar/non-polar GaN platform.

6.1.3 Lateral p-channel and n-channel Ga-Polar (0001) GaN MISFETs

Despite the promising results on the development of the n-channel GaN transistors, the full benefits of GaN electronic circuits and systems have not yet fully realised due to the lack of p-channel GaN transistors for complementary circuits. This thesis investigates the fabrication and characterisation of the lateral p-channel and n-channel GaN metal-insulator-semiconductor field effect transistors (MISFETs) on a p-GaN/GaN/AlGaN/GaN epitaxy on Si substrate platform for complementary integrations.

The enhancement mode p-channel MISFETs with a record low subthreshold swing of 60 mV/dec, a high I_{ON}/I_{OFF} ratio > 10^7, a high g_m of 1.0 mS/mm and a small V_{th} shift of (up to 120 mV) were experimentally demonstrated. The interfacial trap between the SiO_2 gate dielectric and GaN was studied. A trap density in the range of ~ 10^{10} $cm^{-2}eV^{-1}$ was extracted, which is significantly lower than the other reported trap values of 10^{12} to 10^{13} $cm^{-2}eV^{-1}$ [8]. The low interfacial trap density is attributable to low plasma power gate-recessing etching and gate dielectric deposition HCl pre-treatment. The low trap density, coupled with a good control of Mg back-diffusion to GaN/AlGaN interface and 2DHG confinement by back barrier AlGaN in the p-GaN/UID-GaN/UID-AlGaN/UID-GaN epitaxy structure are the main reason for the record low subthreshold swing.

In addition, a dual-peak in the transconductance of the p-channel MISFET was observed. The origins of the dual-peak transconductance were studied using Sentaurus T-CAD. It was found that the presence of the 2DHG channel at the GaN/AlGaN hetero-interface and the inversion

channel at the MIS interface is the reason for the two transconductance peaks. This is the first time the dual-channel conduction mechanism is reported in the p-channel GaN-based transistors. The

For the n-channel MISFET fabrication, an etch-stop at AlGaN etching approach was developed to access the AlGaN/GaN hetero for the 2DEG n-channel on the p-GaN/GaN/AlGaN/GaN wafer. The measured 2DEG density and mobility of the AlGaN/GaN hetero-structures is ~1.0 $\times$ 10^{13} cm^{-2} and 1509.8 $cm^2/(V.s)$, respectively. The n-channel MISFETs with an depletion mode operation exhibit a high output current of 800 mA/mm, a high transconductance of 100 mS/mm, and a small Ron of 3.8 Ω.mm, which is comparable with standard as-grown AlGaN/GaN HEMTs [9]. With further development, such techniques can be integrated into future E-mode n-channel device fabrications without the damage of 2DEG on the ohmic contact region. For the gated region, additional gate-recessing by Cl-based ICP etching and/or F implantation treatments could be incorporated into the device fabrications.

The findings from this study on the fabrication and characterization of lateral p-channel and n-channel devices on a p-GaN/GaN/AlGaN/GaN-on-Si substrate lay the groundwork for realizing high-speed, high-efficiency GaN integrated complementary circuits.

6.2 Recommendations for Future Research and Development

In this section, recommendations for future GaN devices research and development are provided.

6.2.1 Vertical p-channel GaN Devices

Upon now, from the lateral device architecture point of view, the n-channel and p-channel GaN devices has been reported worldwide by different research group with novel device structures and processing techniques. The promising performance of vertical n-channel GaN device architecture is also evident by CAVETs, trench MOSFET, FinFETs and junction field effect structures. The discussion of vertical p-channel GaN is absent. From the demonstrated lateral GaN p-channel transistors so far, the expected 2DHG mobility (typically 10 cm^2/Vs) is still significantly lower than that of Si devices. In fact, Intel has demonstrated n-channel GaN transistor integration with p-channel Si transistors by 3D layer transfer [10]. The hole mobility and hole concentration of Si was achievable at 450 cm^2/Vs and 10^{21} cm^{-3} [10], which is significantly superior to GaN hole mobility and hole concentration.

To improve the p-channel GaN devices output current density and breakdown characteristics, new devices concept is needed, one of which could be the vertical p-channel GaN devices by optimized device layout to boost the overall output current density. The vertical p-channel Trench MOSFETs based on wide bandgap semiconductor materials has been demonstrated on diamond [11], which provide high breakdown voltage of 580 V and specific on-resistance of 23 $m\Omega cm^2$. With the development of the GaN material growth maturity and advanced process techniques of GaN in the next few years, it would be expected to see that one would demonstrate the gate modulation behaviour of vertical p-channel GaN devices.

To pave the road on the research and development of vertical p-channel GaN devices in the ecosystem of GaN electronics. This thesis proposed the study of vertical p-channel GaN devices. An example of monolithic integration of vertical GaN electronics is illustrated in Fig. 6-1. By tailoring the growth epitaxy structure and the selectively GaN etching, the individual vertical n-channel and p-channel GaN transistors can be implemented and monolithically integrated with the high voltage vertical GaN transistors. Herein, the trench MOSFET gate is for illustrated purposes only. The trench size can be scaled down to sub-micron and for

achieving FinFETs or additional p-type GaN regrowth to achieve Fin JFETs. Furthermore, the c-plane side wall on the V-groove can also be utilized to growth GaN/AlGaN/GaN channel with the 2DEG and 2DHG sidewall channel. The SiN_x/SiO_2 hard masks for the V-groove wet etching process naturally serves as hard masks for selectively regrowth process as well, which simplify fabrication process. For the p-type ohmic contact, Mg-post diffusion, selectively ion implantations and p-type regrowth could be adapted for recover the plasma damaged p-GaN surface.

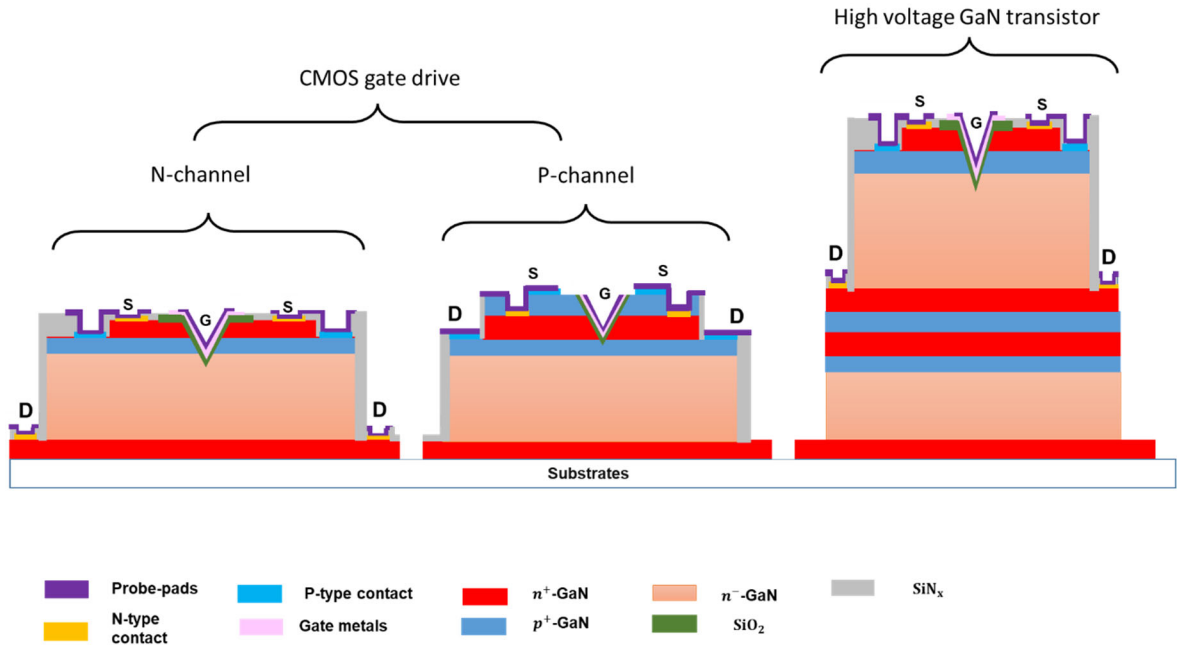

Figure 6-1. An example of monolithic vertical GaN integrated electronics.

On the other hand, the vertical p-channel transistor can also be implemented on the c-plane direction, which features the similar advantages mentioned above, excepting the gate trench formation would require the approach of dry plasma etching and wet treatment to recover the plasma induced damages on the surface.

Furthermore, regardless of growth direction. The implementation of high voltage p-channel GaN devices can be used in the half bridge power converter to replace the high-side n-channel devices, which simplify the gate driver circuits [12].

In conclusion, there is no discussion/demonstration on the vertical p-channel GaN devices to date. The exploration of vertical p-channel GaN devices would open a door on the full realization of GaN electronics ecosystem and exciting research opportunities in this very dynamic research field await.

6.3 References

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Appendix A: Fabrication Process Traveller

Section 1: VMOSFET fabrication process

VMOSFET traveller

Cleave and Clean				
	n-Butyl	Ultrasonic		10 min
	Acetone	Ultrasonic		10 min
	IPA	Ultrasonic		10 min
	N_2 dry			
Inspect	Optical microscope			
SiN_x deposition				>300 nm
	ICPCVD	Clean and condition		
	Recipe: SiN 300C SiO_2 grid 8			
Clean				
	n-Butyl	Ultrasonic		5 min
	Acetone	Ultrasonic		5 min
	IPA	Ultrasonic		5 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min
Photoresist Spin				
	SPR 350	Spin	4000 rpm	30 sec
	Hot plate bake		100 ℃	1 min
Exposure				
	Mask:	**NPIN1-Layer1**		
	UV300			10.8 s
Develop				
	MF26A			60 sec
	DI water			10 sec
Inspect	Optical microscope			
Etch				
	ICP	Clean and condition		
	Recipe: SiN-2			~15 min
Photoresist Strip				
	EKC 830		100 ℃	10 min
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
KOH wet etching				

	DI water (10 mL)	Pre-heat	95 ℃	5 min
	KOH (15 g)	Dissolved in water	95 ℃	10 min
	GaN etching		95 ℃	~ 50 min
Inspect	Optical microscope			
	SEM			
SiNx Strip	HF 40 %			10 - 15 min
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Gate Dielectric				
	PECVD	Clean and condition		
	Recipe: SiO_2-1			~ 60 nm
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min
Photoresist Spin				
	SPR 350	Spin	4000 rpm	30 sec
	Hot plate bake		100 ℃	1 min
Exposure				
	Mask:	**NPIN1-Layer2**		
	UV300			10.8 s
Develop				
	MF26A			60 sec
	DI water	rising		10 sec
Inspect	Optical microscope			
SiO_2 etch				
	ICP	Clean and condition		
	Recipe: SiO_2-1			~ 15 min
GaN etch	ICP			
	Recipe: GaN-4			~ 5 min
Photoresist Strip				
	EKC 830		100 ℃	10 min
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min
Photoresist Spin				
	SPR 220	Spin	4000 rpm	30 sec
	Hot plate bake		100 ℃	3 min
Exposure				
	Mask:	**NPIN1-Layer3**		
	UV300			50 s
Develop				
	MF26A			60 sec
	DI water	rising		10 sec
Inspect	Optical microscope			
GaN etch	ICP			

	Recipe: GaN-1			~ 20 min
Photoresist Strip				
	EKC 830		100 ℃	10 min
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Annealing				
	Jipelec			
	Recipe: Eng-1	N_2	500 ℃	10 min
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min
Photoresist Spin				
	PMGI	Spin	4000 rpm	30 sec
	Hot plate bake		180 ℃	5 min
	SPR350	Spin	4000 rpm	30 sec
	Hot plate bake		100 ℃	1 min
Exposure				
	Mask:	**NPIN1-Layer4**		
	UV300			50 s
SiO_2 etch				
	ICP	Clean and condition		
	Recipe: SiO_2-1			~ 15 min
Metal Deposition				
	HCl treatment			1 min
	Thermal evaporator	Ti/Al/Ni/Au		
Liftoff				
	EKC830			Overnight
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min
Photoresist Spin				
	PMGI	Spin	8000 rpm	30 sec
	Hot plate bake		180 ℃	5 min
	SPR350	Spin	8000 rpm	30 sec
	Hot plate bake		100 ℃	1 min
Exposure				
	Mask:	**NPIN1-Layer5**		
	UV300			11 s
Metal Deposition				
	HCl treatment			1 min
	Thermal evaporator	Pd/Ni/Au		
Liftoff				
	EKC830			Overnight
Clean				
	n-Butyl	Soak		1 min

	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Annealing				
	Jipelec	N_2		
	Recipe: Eng-1		400 ℃	10 min
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min
Photoresist Spin				
	PMGI	Spin	8000 rpm	30 sec
	Hot plate bake		180 ℃	5 min
	SPR350	Spin	8000 rpm	30 sec
	Hot plate bake		100 ℃	1 min
Exposure				
	Mask:	**NPIN1-Layer6**		
	UV300			11 s
Metal Deposition				
	HCl treatment			1 min
	Thermal evaporator	Ni/Au		
Liftoff				
	EKC830			Overnight
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Passivation				
	ICPCVD	Clean and condition		
	Recipe: SiN 300C SiO_2 grid 8			~ 150 nm
	PECVD	Clean and condition		
	Recipe: SiN -5			~ 150 nm
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min
Photoresist Spin				
	PMGI	Spin	4000 rpm	30 sec
	Hot plate bake		180 ℃	5 min
	SPR350	Spin	4000 rpm	30 sec
	Hot plate bake		100 ℃	1 min
Exposure				
	Mask:	**NPIN1-Layer7**		
	UV300			11 s
Via-opening etch				
	RIE	Clean and condition		
	Recipe: SiN_x			8 min
Photoresist Strip				

	EKC 830		100 ℃	10 min
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min
Photoresist Spin				
	PMGI	Spin	8000 rpm	30 sec
	Hot plate bake		180 ℃	5 min
	SPR350	Spin	8000 rpm	30 sec
	Hot plate bake		100 ℃	1 min
Exposure				
	Mask:	**NPIN1-Layer8**		
	UV300			11 s
Metal Deposition				
	HCl treatment			1 min
	Thermal evaporator	Ni/Au		
Liftoff				
	EKC830			Overnight
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
	SEM			

Section 2: FinFETs fabrication process

FinFETs traveller

Cleave and Clean				
	n-Butyl	Ultrasonic		10 min
	Acetone	Ultrasonic		10 min
	IPA	Ultrasonic		10 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min
Photoresist Spin				
	PMGI	Spin	8000 rpm	30 sec
	Hot plate bake		180 ℃	5 min
	SPR 350	Spin	8000 rpm	30 sec
	Hot plate bake		100 ℃	1 min
Exposure				
	Mask: **NIN1-Layer1 (EBL alignment mark)**			
	UV300			10.8 s
Develop				
	MF26A			60 sec
	DI water			10 sec
Inspect	Optical microscope			
Metal Deposition				
	Thermal evaporator	Ti/Al/Ni/Au		
Liftoff				
	EKC830			Overnight
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
SiN_x deposition				100 nm
	ICPCVD	Clean and condition		
	Recipe: SiN 300C SiO_2 grid 8			
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min
Resist Spin				
	CSAR62	Spin	4000 rpm	30 sec
	Hot plate bake		180 ℃	3 min
	Electra92	Spin	4000 rpm	30 sec
	Hot plate bake		100 ℃	1 min
Exposure (EBL)				
	Mask: **NIN1-Layer2 Fin arrays pattern**			
	Ratih voyager			160 μC/cm^2
Develop				
	DI water			60 sec

	Xylene			60 sec
	IPA			10 sec
	IPA			10 sec
Inspect	Optical microscope			
	SEM			
Metal Deposition				
	Thermal evaporator	Ni/Au		
Liftoff				
	EKC830			Overnight
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
	SEM			
Dehydration	Hot plate bake		100 ℃	1 min
Photoresist Spin				
	SPR 350	Spin	8000 rpm	30 sec
	Hot plate bake		100 ℃	1 min
Exposure				
	Mask: **NIN1-Layer3** **(SiN etching windows/ Fin boundary)**			
	UV300			10.8 s
Develop				
	MF26A			60 sec
	DI water			10 sec
Inspect	Optical microscope			
SiN etching				
	RIE	Clean and condition		
	Recipe: SiN			8 min
Photoresist Strip				
	EKC 830		100 ℃	10 min
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
	SEM			
KOH wet etching				
	DI water (10 mL)	Pre-heat	95 ℃	5 min
	KOH (15 g)	Dissolved in water	95 ℃	10 min
	GaN etching		95 ℃	~ 7 - 10 min
Inspect	Optical microscope			
	SEM			
Metal Strip				
	Aqua regia			1 min
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min
Photoresist Spin				
	PMGI	Spin	4000 rpm	30 sec

	Hot plate bake		180 ℃	5 min
	SPR 350	Spin	4000 rpm	30 sec
	Hot plate bake		100 ℃	1 min
Exposure				
	Mask: **NIN1-Layer4 (SiN_x+nGaN etching)**			
	UV300			10.8 s
Develop				
	MF26A			60 sec
	DI water			10 sec
Inspect	Optical microscope			
SiN_x etch	ICP			
	Recipe: SiN-2			~ 15 min
GaN etch	ICP			
	Recipe: GaN-4			~ 5 min
Photoresist Strip				
	EKC 830		100 ℃	10 min
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Gate Dielectric				
	PECVD	Clean and condition		
	Recipe: SiN-5			~20 nm
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min
Photoresist Spin				
	PMGI	Spin	4000 rpm	30 sec
	Hot plate bake		180 ℃	5 min
	SPR 350	Spin	8000 rpm	30 sec
	Hot plate bake		100 ℃	1 min
Exposure				
	Mask:	**NIN1-Layer5 (Gate metals)**		
	UV300			10.8 s
Develop				
	MF26A			60 sec
	DI water			10 sec
Inspect	Optical microscope			
Metal Deposition				
	Thermal evaporator	Ni/Au		
Liftoff				
	EKC830			Overnight
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min

Photoresist Spin				
	BPRS200	Spin	4000 rpm	30 sec
	Hot plate bake		100 ℃	2 min
Photoresist planarization				
	RIE	Clean and condition		
	Recipe: O_2 ashing			~22 min
Inspect	Optical microscope			
	Surface profilemeter			
	SEM			
Gate metal etching				
	Aqua regia			8-10 sec
Inspect	Optical microscope			
	SEM			
SiN etching				
	RIE	Clean and condition		
	Recipe: SiN			30 sec
Photoresist Strip				
	EKC 830		100 ℃	10 min
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
	SEM			
Passivation				
	PECVD	Clean and condition		
	Recipe: SiN -5			80 nm
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min
Resist Spin				
	CSAR62	Spin	4000 rpm	30 sec
	Hot plate bake		180 ℃	3 min
	Electra92	Spin	4000 rpm	30 sec
	Hot plate bake		100 ℃	1 min
Exposure (EBL)				
	Mask:	**NIN1-Layer6 (2^{nd} stage EBL)**		
	Ratih voyager			160 μC/cm^2
Develop				
	DI water			60 sec
	Xylene			60 sec
	IPA			10 sec
	IPA			10 sec
Inspect	Optical microscope			
	SEM			
SiN etching				
	RIE	Clean and condition		
	Recipe: SiN			~ 1.5 min
Photoresist Strip				
	EKC 830		100 ℃	10 min

Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min
Photoresist Spin				
	PMGI	Spin	4000 rpm	30 sec
	Hot plate bake		180 ℃	5 min
	SPR 350	Spin	4000 rpm	30 sec
	Hot plate bake		100 ℃	1 min
Exposure				
	Mask:	**NIN1-Layer7 (SiN_x etch)**		
	UV300			10.8 s
Develop				
	MF26A			60 sec
	DI water			10 sec
Inspect	Optical microscope			
SiN_x etch	RIE			
	Recipe: SiN-2			~ 5 min
Photoresist Strip				
	EKC 830		100 ℃	10 min
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min
Photoresist Spin				
	SPR 220	Spin	4000 rpm	30 sec
	Hot plate bake		100 ℃	3 min
Exposure				
	Mask:	**NIN1-Layer8 (GaN mesa etch)**		
	UV300			~ 50 s
Develop				
	MF26A			60 sec
	DI water			10 sec
Inspect	Optical microscope			
SiN_x etch	ICP			
	Recipe: GaN-1			~ 20 min
Photoresist Strip				
	EKC 830		100 ℃	10 min
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min
Photoresist Spin				
	PMGI	Spin	8000 rpm	30 sec
	Hot plate bake		180 ℃	5 min
	SPR 350	Spin	8000 rpm	30 sec
	Hot plate bake		100 ℃	1 min

Exposure				
	Mask: **NIN1-Layer 9 (probe-pads)**			
	UV300			10.8 s
Develop				
	MF26A			60 sec
	DI water			10 sec
Inspect	Optical microscope			
Metal Deposition				
	Thermal evaporator	Ti/Al/Ni/Au		
Liftoff				
	EKC830			Overnight
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
	SEM			

Section 3. p-channel MISFETS fabrication process

Cleave and Clean				
	n-Butyl	Ultrasonic		10 min
	Acetone	Ultrasonic		10 min
	IPA	Ultrasonic		10 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min
Photoresist Spin				
	SPR 350	Spin	4000 rpm	30 sec
	Hot plate bake		100 ℃	1 min
Exposure				
	Mask:	**ET1-rapid1 (mesa)**		
	UV300			10.8 s
Develop				
	MF26A			60 sec
	DI water	rising		10 sec
Inspect	Optical microscope			
GaN etch	ICP	Clean and condition		
	Recipe: GaN-4			~ 8 min
Photoresist Strip				
	EKC 830		100 ℃	10 min
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min
Photoresist Spin				
	PMGI	Spin	4000 rpm	30 sec
	Hot plate bake		180 ℃	5 min
	SPR 350	Spin	4000 rpm	30 sec
	Hot plate bake		100 ℃	1 min
Exposure				
	Mask:	**ET1-rapid1**		

		(ohmic)		
	UV300			11 s
Develop				
	MF26A			60 sec
	DI water	rising		10 sec
Inspect	Optical microscope			
Metal Deposition				
	O_2 treatment			25s
	HCl:H_2O treatment			1 min
	Thermal evaporator	Ni/Au (20/ 20 nm)		
Liftoff				
	EKC830			Overnight
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Annealing				
	Jipelec			
	Recipe: Eng-1	N_2:O_2 (4:1)	535 ℃	5 min
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min
Photoresist Spin				
	PMGI	Spin	8000 rpm	30 sec
	Hot plate bake		180 ℃	5 min
	SPR350	Spin	8000 rpm	30 sec
	Hot plate bake		100 ℃	1 min
Exposure				
	Mask:	**ET1-rapid1 (ohmic)**		
	UV300			11 s
Metal Deposition				
	Thermal evaporator	Ni/Au (20/ 200 nm)		
Liftoff				
	EKC830			Overnight
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Passivation				
	PECVD	Clean and condition		
	Recipe: SiN -5			100 nm
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			

Dehydration	Hot plate bake		100 ℃	1 min
Resist Spin				
	PMGI	Spin	4000 rpm	30 sec
	Hot plate bake		180 ℃	5 min
	SPR 350	Spin	4000 rpm	30 sec
	Hot plate bake		100 ℃	1 min
Exposure (EBL)				
	Mask:	**ET1-rapid1 (gate foot)**		
	UV300			11 s
Develop				
	MF26A			60 sec
	DI water			10 sec
Inspect	Optical microscope			
SiN_x etch	ICP	Clean and condition		
	Recipe: SiN-2	CHF_3/O_2		100 nm
GaN etch	ICP			
	Recipe: Eng-1	Cl_2/SF_6		75 nm
Photoresist Strip				
	EKC830		90 ℃	10 min
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Gate Dielectric				
	HCl treatment			1 min
	PECVD	Clean and condition		
	Recipe: SiO_2-1			~ 15 nm
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 ℃	1 min
Photoresist Spin				
	PMGI	Spin	4000 rpm	30 sec
	Hot plate bake		180 ℃	5 min
	SPR 350	Spin	4000 rpm	30 sec
	Hot plate bake		100 ℃	1 min
Exposure				
	Mask:	**ET1-rapid1 (gate metals)**		
	UV300			11 s
Develop				
	MF26A			60 sec
	DI water	rising		10 sec
Inspect	Optical microscope			
Metal Deposition				
	Thermal evaporator	Ni/Au		
Liftoff				
	EKC830			Overnight
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min

	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 °C	1 min
Photoresist Spin				
	PMGI	Spin	4000 rpm	30 sec
	Hot plate bake		180 °C	5 min
	SPR 350	Spin	4000 rpm	30 sec
	Hot plate bake		100 °C	1 min
Exposure				
	Mask:	**ET1-rapid1 (Via-opening)**		
	UV300			11 s
Develop				
	MF26A			60 sec
	DI water	rising		10 sec
Inspect	Optical microscope			
SiNx etch	RIE			
	Recipe: SiN			100 nm
Photoresist Strip				
	EKC830		90 °C	10 min
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			
Dehydration	Hot plate bake		100 °C	1 min
Photoresist Spin				
	PMGI	Spin	4000 rpm	30 sec
	Hot plate bake		180 °C	5 min
	SPR 350	Spin	4000 rpm	30 sec
	Hot plate bake		100 °C	1 min
Exposure				
	Mask:	**ET1-rapid1 (pads)**		
	UV300			11 s
Develop				
	MF26A			60 sec
	DI water	rising		10 sec
Inspect	Optical microscope			
Metal Deposition				
	Thermal evaporator	Ni/Au		
Liftoff				
	EKC830			Overnight
Clean				
	n-Butyl	Soak		1 min
	Acetone	Soak		1 min
	IPA	Soak		1 min
	N_2 dry			
Inspect	Optical microscope			

For the n-channel GaN transistor, the fabricate process is very similar to the p-channel and not separately produced.