

# **The University of Sheffield**



## **Novel Pulse Width Modulation and Control Strategies for Open Winding Permanent Magnet Synchronous Machines**

**Lei Xu**

A thesis submitted for the degree of Doctor of Philosophy

Department of Electronic and Electrical Engineering

The University of Sheffield

Mappin Building, Sheffield, S1 3JD, UK

**July 2022**

# ABSTRACT

Open winding permanent magnet synchronous machines (OW-PMSMs) can combine the synergies of high efficiency, torque density, and power density in PMSMs and high voltage utilization, fault tolerant capability, and flexible control freedom in OW inverter topologies. Pulse width modulation (PWM) can affect the control performance of an OW-PMSM drive in many aspects including current harmonics, common mode voltage (CMV), modulation region, and switching frequency. In this thesis, new and novel PWM and control strategies are proposed and investigated for both isolated and common DC-bus OW-PMSM drives.

Firstly, the isolated DC-bus OW-PMSM drives have larger voltage utilization, more output voltage levels, and lower control complexity compared with other OW topologies, i.e. common DC-bus and floating capacitor topologies. Sinusoidal PWMs (SPWMs) have the advantages of easy implementation and less computation burden compared with space vector PWMs (SVPWMs), and are preferable for the isolated DC-bus OW drives due to abundantly available switching states. SPWM strategies with zero sequence voltage (ZSV) injection and unbalanced voltage distribution are proposed to reduce current harmonics and switching frequency for the isolated DC-bus OW drives with symmetrical and arbitrary DC-bus voltage ratios. Moreover, balanced and unbalanced voltage distributions of SPWM can cause different inverter nonlinearity characteristics and are utilized for the inverter nonlinearity compensation.

Secondly, the common DC-bus OW-PMSM drives have lower cost, high fault tolerant capability, and better controllability of zero sequence current (ZSC) compared with other OW inverter topologies. The ZSC control is necessary but limits the utilization of vectors in the common DC-bus OW topology, so that SVPWMs are preferable for the switching pattern optimization due to visible voltage vectors, vector durations, and vector action sequences compared with SPWMs. With switching pattern optimization for SVPWM, ZSC is controlled under different objectives, i.e. low current harmonics, CMV variation elimination, and maximum operation range. Specifically, current harmonics can be reduced by the vector action sequence optimization. The voltage vectors with the same CMV are selected for CMV elimination, and further selected with different ZSVs for ZSC control to achieve the control of CMV and ZSC simultaneously. The operation range of an OW-PMSM can be extended by the optimal selection of the voltage vectors with non-null ZSV and the largest magnitude for the ZSC control.

# ACKNOWLEDGEMENTS

First and foremost, I would like to express my sincere gratitude to my supervisor, Professor Z. Q. Zhu, for giving me the chance to study in this interesting field. His professional technical guidance, support, and encouragement during my Ph.D. study are very valuable and impressive.

I would like to thank my sponsoring company Midea Welling Motor Technology (Shanghai) Co., Ltd for the financial support to boost my career. My special thanks give to Dr Liming Gong for his introduction and encouragement. Thanks are also given to my colleagues, Dr Chao Wang and Mr Xiangnan Qin, for their technical support and discussions.

I would like to express my thanks to all my fellow colleagues of the Electrical Machines and Drives Group at The University of Sheffield for their help and knowledgeable discussions, particularly, Dr Ximeng Wu, Dr Dawei Liang, Dr Bo Shuang, Dr Yang Xiao, Dr Tianyi Liu, Dr Bo Shao, and Mr Luocheng Yan.

Finally, great thanks to my parents and my wife for their endless love, support, and encouragement throughout my Ph.D. study.

# CONTENTS

<b>ABSTRACT.....</b>	<b>1</b>
<b>ACKNOWLEDGEMENTS .....</b>	<b>2</b>
<b>CONTENTS.....</b>	<b>3</b>
<b>NOMENCLATURES.....</b>	<b>6</b>
<b>LIST OF ABBREVIATIONS.....</b>	<b>9</b>
<b>CHAPTER 1 GENERAL INTRODUCTION .....</b>	<b>11</b>
1.1 Introduction.....	11
1.2 Topologies and Model of PMSM.....	12
1.3 Topologies of DTL-VSIs .....	14
1.4 Isolated DC-bus Dual Inverters .....	19
1.4.1 PWM strategies.....	20
1.4.2 CMV control .....	33
1.4.3 Over charge of capacitors .....	35
1.4.4 Fault tolerant control.....	36
1.5 Common DC-bus Dual Inverters .....	38
1.5.1 PWM and ZSC control strategies .....	41
1.5.2 CMV control .....	48
1.5.3 Flux weakening.....	51
1.5.4 Sensorless strategy based on ZSV .....	52
1.5.5 Fault tolerant control.....	54
1.6 Floating Capacitor Dual Inverters.....	59
1.6.1 PWM strategies and floating capacitor voltage control.....	59
1.6.2 Fault tolerant control.....	65
1.7 Performance Comparison for Three Types of Dual Inverters .....	66
1.8 Scope and Contributions of the Thesis .....	70
1.8.1 Motivation.....	70
1.8.2 Outline .....	72
1.8.3 Contributions .....	73
<b>CHAPTER 2 LOW SWITCHING FREQUENCY SPWM STRATEGIES FOR OPEN WINDING MACHINE WITH LOW CURRENT HARMONICS.....</b>	<b>75</b>
2.1 Introduction.....	76
2.2 Dual Two-level Inverters and Conventional SPWM Strategy .....	77



2.3 Proposed SVPWM Strategies .....	80
2.3.1 PWM strategy implementation .....	80
2.3.2 Comparative performance analysis .....	83
2.4 Simulation and Experiment Results .....	89
2.4.1 Simulation validation .....	89
2.4.2 Experimental validation .....	100
2.5 Summary .....	106
<b>CHAPTER 3 A GENERALIZED SINUSOIDAL PWM STRATEGY FOR OPEN WINDING MACHINE WITH LOW CURRENT HARMONICS .....</b>	<b>107</b>
3.1 Introduction .....	107
3.2 Proposed PWM Strategy .....	108
3.2.1 Zero sequence voltage injection .....	110
3.2.2 Voltage distribution method .....	113
3.2.3 Current ripple prediction .....	116
3.2.4 Capacitor overcharge issue in dual inverters .....	120
3.2.5 Switching commutation issue in dual inverters .....	121
3.3 Experiment Results .....	123
3.4 Summary .....	136
<b>CHAPTER 4 INVERTER NONLINEARITY COMPENSATION FOR OPEN WINDING MACHINE WITH DUAL SWITCHING MODES .....</b>	<b>137</b>
4.1 Introduction .....	138
4.2 Analysis of Nonlinearity of Dual OW Inverters .....	139
4.2.1 SPWM strategy with balanced and unbalanced switching modes for dual OW inverters .....	139
4.2.2 Analysis of inverter nonlinearity in balanced and unbalanced switching modes .....	142
4.3 Proposed Inverter Nonlinearity Compensation Strategy .....	149
4.4 Experiment Results .....	154
4.5 Summary .....	164
<b>CHAPTER 5 A NOVEL SVPWM FOR COMMON DC-BUS OPEN WINDING MACHINE WITH LOW CURRENT HARMONIC .....</b>	<b>165</b>
5.1 Introduction .....	166
5.2 Dual Two-level Inverters fed OW Machine .....	166
5.2.1 Conventional SVPWM strategy and issues .....	166
5.2.2 Current harmonic analysis method for PWM strategy .....	171
5.3 Proposed SVPWM Strategy .....	174
5.3.1 Symmetrical vector sequence .....	174

5.3.2 Asymmetric vector sequence .....	178
5.3.3 Zero sequence current control.....	183
5.4 Experiment Results .....	185
5.5 Summary .....	192
<b>CHAPTER 6 ZERO SEQUENCE CURRENT SUPPRESSION STRATEGY FOR OPEN WINDING PMSM DRIVES WITH CONSTANT COMMON MODE VOLTAGE .....</b>	<b>194</b>
6.1 Introduction.....	194
6.2 Dual Inverters and Conventional PWM Strategies .....	195
6.2.1 Common mode voltage and zero sequence voltage in dual inverters.....	195
6.2.2 Conventional CMV elimination PWM strategy .....	197
6.3 Proposed SVPWM Strategy.....	198
6.3.1 Switching combination groups in space vector plane of dual inverters.....	198
6.3.2 Proposed SVPWM strategy .....	201
6.4 Experiment Results .....	210
6.5 Summary .....	222
<b>CHAPTER 7 A NOVEL SVPWM FOR OPEN WINDING PMSM WITH EXTENDED OPERATION RANGE .....</b>	<b>223</b>
7.1 Introduction.....	224
7.2 Modulation Region in Conventional SVPWM Strategy.....	224
7.3 Proposed SVPWM Strategy.....	227
7.4 Experiment Results .....	238
7.5 Summary .....	251
<b>CHAPTER 8 GENERAL CONCLUSION AND FUTURE WORK .....</b>	<b>252</b>
8.1 PWM and Control Strategies for Isolated DC-bus OW-PMSM Drive .....	253
8.2 PWM and Control Strategies for Common DC-bus OW-PMSM Drive.....	256
8.3 Future Work .....	259
<b>REFERENCES.....</b>	<b>261</b>
<b>APPENDIX A THREE-LEG CLAMPING SVPWM STRATEGY .....</b>	<b>271</b>
<b>APPENDIX B PUBLICATIONS .....</b>	<b>278</b>

# NOMENCLATURES

Symbol	Meaning	Unit
$B$	Friction coefficient	Nm/(rad/s)
$f_{PWM}$	Frequency of PWM carrier signal	Hz
$i_0^*$	Reference zero sequence current	A
$i_d^*$	Reference $d$ -axis current	A
$i_q^*$	Reference $q$ -axis current	A
$i_0$	Zero sequence current	A
$i_a, i_b, i_c$	Phase A, B, C currents	A
$i_d$	$d$ -axis current	A
$i_q$	$q$ -axis current	A
$J$	Rotational inertia	Kg·m <sup>2</sup>
$L_d$	$d$ -axis inductance	H
$L_q$	$q$ -axis inductance	H
$p$	Number of pole pairs	/
$R_s$	Phase resistance	Ω
$T_e$	Electromagnetic torque	Nm
$T_l$	Load torque	Nm
$T_{mnZ}$	Duration of vectors with non-null zero sequence voltage	s
$t_{off}$	Turn-off time of switching device	s
$t_{on}$	Turn-on time of switching device	s

$T_{PWM}$	Duration of a PWM cycle	s
$T_r$	Redistribution time of zero vectors	s
$V_0^*$	Reference zero sequence voltage	V
$V_A^*, V_B^*, V_C^*$	Reference voltages for OW drive in three phases	V
$V_{A_z}^*, V_{B_z}^*, V_{C_z}^*$	Reference voltages for OW drive in three phases after zero sequence voltage injection	V
$V_{A1}^*, V_{B1}^*, V_{C1}^*$	Reference voltages for Inverter I in three phases	V
$V_{A2}^*, V_{B2}^*, V_{C2}^*$	Reference voltages for Inverter II in three phases	V
$V_d^*$	$d$ -axis reference voltage	V
$V_q^*$	$q$ -axis reference voltage	V
$V_\alpha^*$	$\alpha$ -axis reference voltage	V
$V_\beta^*$	$\beta$ -axis reference voltage	V
$V_A, V_B, V_C$	Phase A, B, C voltages	V
$V_{A'O}, V_{B'O}, V_{C'O}$	Phase A, B, C pole voltages of Inverter II (Common DC-bus topology)	V
$V_{A'O'}, V_{B'O'}, V_{C'O'}$	Phase A, B, C pole voltages of Inverter II (Isolated DC-bus topology)	V
$V_{AO}, V_{BO}, V_{CO}$	Phase A, B, C pole voltages of Inverter I	V
$V_c$	Voltage of floating capacitor	V
$V_{CMV}$	Common mode voltage of OW drive	V
$V_{CMV1}$	Common mode voltage of Inverter I	V
$V_{CMV2}$	Common mode voltage of Inverter II	V
$V_d$	Diode forward voltage	V

$V_{dc}$	DC-bus voltage	V
$V_{dc1}$	DC-bus voltage of Inverter I	V
$V_{dc2}$	DC-bus voltage of Inverter II	V
$V_{ref}$	Magnitude of reference voltage vector of OW drive	V
$V_{ref\alpha1}$	$\alpha$ -axis reference voltage of Inverter I	V
$V_{ref\alpha2}$	$\alpha$ -axis reference voltage of Inverter II	V
$V_{ref\beta1}$	$\beta$ -axis reference voltage of Inverter I	V
$V_{ref\beta2}$	$\beta$ -axis reference voltage of Inverter II	V
$V_s$	Collector-emitter saturation voltage	V
$V_z$	Injected zero sequence voltage for SPWM	V
$V_{ZSV}$	Zero sequence voltage of OW drive	V
$\theta$	Electrical angular rotor position	rad
$\psi_m$	Permanent magnet flux-linkage	Wb
$\omega_e^*$	Reference electrical angular speed	rad/s
$\omega_e$	Electrical angular speed	rad/s
$\omega_m$	Mechanical angular speed	rad/s

# LIST OF ABBREVIATIONS

BEMF	Back electromotive force
BPF	Band pass filter
CMV	Common mode voltage
CMVE-PWM	Common mode voltage elimination pulse width modulation
DC	Direct current
DTL-VSIs	Dual two-level voltage source inverters
IGBT	Insulated-gate bipolar transistor
IPMSM	Interior permanent magnet synchronous machine
MI	Modulation index
OW	Open winding
PM	Permanent magnet
PMSM	Permanent magnet synchronous machine
PWM	Pulse width modulation
RMS	Root mean square
SHCPWM	Sub-hexagonal centre pulse width modulation
SPMSM	Surface mounted permanent magnet synchronous machine
SPWM	Sinusoidal pulse width modulation
SVPWM	Space vector pulse width modulation
THD	Total harmonic distortion
TLC-SVPWM	Three-leg clamping space vector pulse width modulation

VSI	Voltage source inverter
ZSC	Zero sequence current
ZSV	Zero sequence voltage
PI	Proportional integral
MOSFET	Metal-oxide-semiconductor field-effect transistor
PR	Proportional resonant
POD-PWM	Phase opposition deposition pulse width modulation

# CHAPTER 1 GENERAL INTRODUCTION

## 1.1 Introduction

Permanent magnet synchronous machines (PMSMs) have been widely used in electric vehicles, aerospace, and industry applications due to excellent performance, such as high efficiency, torque density, and power density [ZHU07] [ELR14]. Generally, a PMSM is driven by a voltage source inverter (VSI), which has the merits of good voltage profiles, fast response, and easy implementation for variable frequency drives [KAZ98] [BAI04]. However, the maximum speed and power of a PMSM fed by a conventional two-level inverter are limited due to the increase of back electromotive force (BEMF) with the speed rise and the limited DC-bus voltage utilization. Moreover, the conventional three phase two-level inverter has the drawback of low fault tolerant capability. The open winding (OW) inverter topology can improve the DC-bus voltage utilization and increase the speed range. Meanwhile, the OW drive also has the merits of flexible control freedom, fault tolerant capability, and multilevel output voltages [KIM04] [KIA17] [ZHA18a] [ZHU19]. Compared with a two-level VSI, a multilevel VSI can reduce the total harmonic distortion of output voltages, and generate higher voltages while utilizing low voltage rating switching devices. Compared with conventional multilevel inverters, such as cascaded H-bridge, flying capacitor, and diode-clamped inverters, OW dual inverters have obvious advantages, such as fewer switching devices, fault tolerant capability, and more redundant switching states [HUA22]. An OW-PMSM fed by dual two-level voltage source inverters (DTL-VSIs) can simply be obtained by disconnecting the stator winding neutral point without changing any of the machine structure, and two standard two-level inverters are connected to two sides of three phase windings. Hence, the OW-PMSM can combine the synergies of the PMSM and the OW inverter topology, and has drawn much attention by researchers for many applications, such as electric vehicles and aerospace [WEL03] [HUA21].

Pulse width modulation (PWM) strategies have a great influence on the performance of VSIs. Many sinusoidal PWM (SPWM) [SEK13] [PIR17] and space vector PWM (SVPWM) [SRI13] [AGH19] strategies are reported for an OW drive fed by dual inverters. SPWMs design switching patterns from a macro perspective, while SVPWMs design switching patterns from a micro perspective. Compared with SVPWMs, SPWM strategies have the advantage of easy implementation due to the absence of the sector selection and vector duration calculation. On



the other hand, voltage vectors, vector durations, and vector action sequences are clearly shown in SVPWMs, making it more convenient for switching pattern optimization. Due to the error between the reference voltage and the instantaneous output voltage with the PWM control, current harmonics are generated in three phase currents. The PWM induced current harmonics should be considered in the OW drive. Moreover, PWM strategies can also affect some other control performances in the OW drive, such as common mode voltage (CMV), modulation region, switching frequency. An OW drive fed by dual inverters has abundant switching states, so that there is more freedom to design PWM strategies to improve control performances.

In this thesis, the PWM and control strategies of OW-PMSMs fed by DTL-VSIs are investigated in terms of current harmonics, CMV, modulation region for performance improvement.

## 1.2 Topologies and Model of PMSM

PMSMs have various geometry structures with different characteristics and can be used for different applications. Generally, according to stator winding configurations, PMSMs can be categorized into fractional-slot and integral-slot machines, which usually adopt non-overlapping concentrated (tooth-coil) and overlapping concentrated or distributed winding configurations, respectively, to achieve high winding factor. Fig. 1.1 shows the non-overlapping and overlapping winding configurations. Compared to overlapping windings, non-overlapping concentrated windings have advantages of lower copper loss and less total machine mass due to short end-windings, leading to the increase of torque density and efficiency. However, due to less stator magneto-motive harmonic components in integral-slot machines, the overlapping windings, particularly overlapping distributed windings, can reduce permanent magnet (PM) eddy current losses, iron losses, acoustic noise and vibration compared with the non-overlapping concentrated windings.

On the other hand, according to the rotor structure, there are two types of radial field PMSMs, i.e. surface mounted PMSM (SPMSM) and interior PMSM (IPMSM) [HEN10] [WAN19]. Fig. 1.2 shows typical rotor structures of radial field PMSMs. For the SPMSM, the PMs are mounted on the rotor's surface as shown in Fig. 1.2 (a), and the SPMSM is widely used in servo systems because of its low torque ripple and small inductance, making it ideal for the fast current regulation. The interior PMs can be magnetized radially or circumferentially in an IPMSM as shown in Fig. 1.2 (b) and (c), respectively. Different effective air gaps in  $d$ - and  $q$ -

axes of the IPMSM cause different  $d$ - and  $q$ -axis inductances, and generating the saliency of the IPMSM, which can be utilized for the reluctance torque generation. As a result, with the same torque, the consumption of PMs in an IPMSM is less than that in a SPMSM. Moreover, compared with SPMSMs, IPMSMs are more suitable for flux weakening operations due to larger  $d$ -axis inductance and buried magnets which can effectively avoid demagnetization. Consequently, IPMSMs are widely used in home appliances and electric vehicle applications.

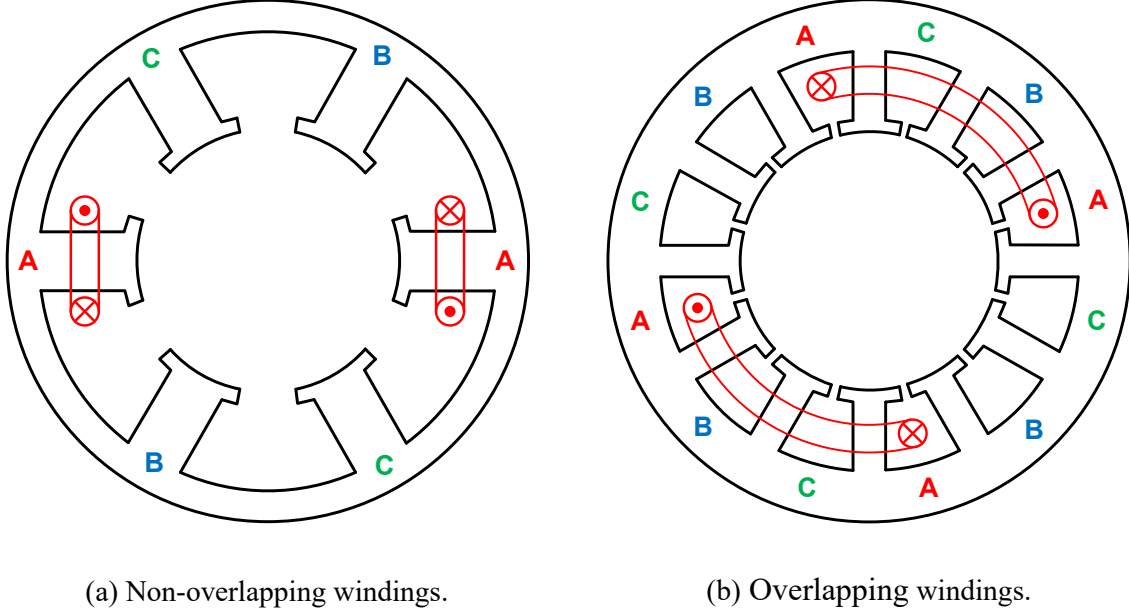


Fig. 1.1 Winding configurations of PMSM.

$D$ - and  $q$ -axis voltages of a PMSM can be expressed as

$$\begin{aligned} u_d &= R_s i_d + L_d \frac{di_d}{dt} - \omega_e L_q i_q \\ u_q &= R_s i_q + L_q \frac{di_q}{dt} + \omega_e (L_d i_d + \psi_m) \end{aligned} \quad (1.1)$$

where  $R_s$  is the phase resistance,  $L_d$  and  $L_q$  are the  $d$ - and  $q$ -axis inductances, respectively,  $i_d$  and  $i_q$  are the  $d$ - and  $q$ -axis currents, respectively,  $\omega_e$  is the electrical angular speed,  $\psi_m$  is the permanent magnet flux-linkage.

The torque of a PMSM can be expressed as

$$T_e = \frac{3}{2} p \left[ \psi_m i_q + (L_d - L_q) i_d i_q \right] \quad (1.2)$$

where  $p$  is the number of pole pairs. Both permanent magnet torque and reluctance torque can

contribute to the torque of an IPMSM. However, in a SPMSM, there is no reluctance torque due to negligible saliency.

The mechanical motion equation of a PMSM can be expressed as

$$T_e = J \frac{d\omega_m}{dt} + B\omega_m + T_l \quad (1.3)$$

where  $J$  is the rotational inertia,  $B$  is the resistance coefficient,  $\omega_m$  is the mechanical speed of rotor,  $T_l$  is the load torque.

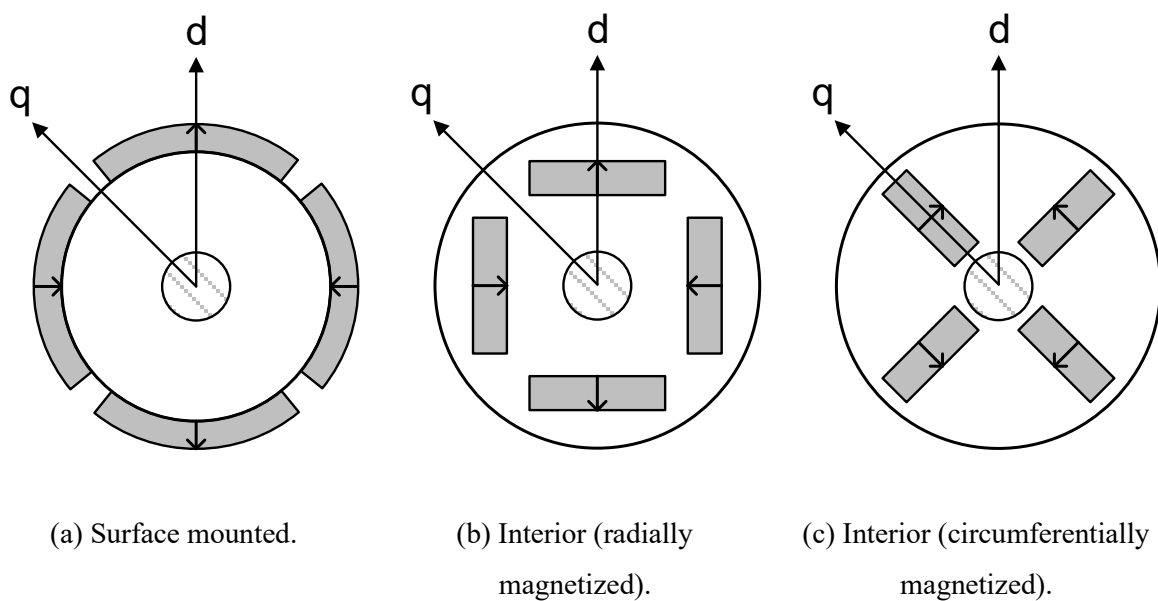


Fig. 1.2 Typical PMSM rotor structures.

### 1.3 Topologies of DTL-VSIs

The topologies of DTL-VSIs can be categorized into three types, i.e. isolated DC-bus, common DC-bus, and floating capacitor as shown in Fig. 1.3, according to voltage sources of two inverters [MOH03] [WEL03] [KOM04]. Compared with the conventional three phase electrical machine with Y- or delta-connections, the OW three phase machine disconnects the three-phase windings, and the two terminals of open windings are connected to two inverters. If two isolated voltage sources are used for two inverters, the DTL-VSIs are configured as the isolated DC-bus topology as shown in Fig. 1.4 (a). If the two inverters are supplied with the same voltage source, then the DTL-VSIs are configured as the common DC-bus topology as shown in Fig. 1.4 (b). If the two inverters are supplied with a voltage source and a floating

capacitor, then the DTL-VSIs are configured as the floating capacitor topology as shown in Fig. 1.4 (c). Although the three topologies all have an OW machine fed by two inverters, they have quite different control requirements and performances, which will be described and compared in detail in Sections 1.4-1.7.

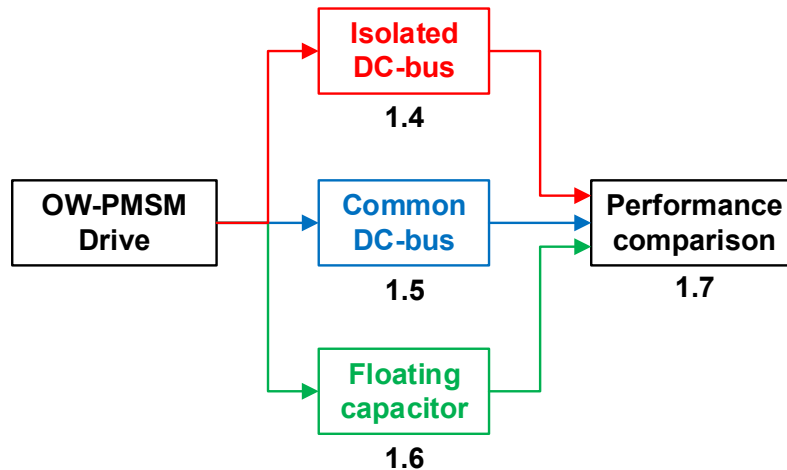
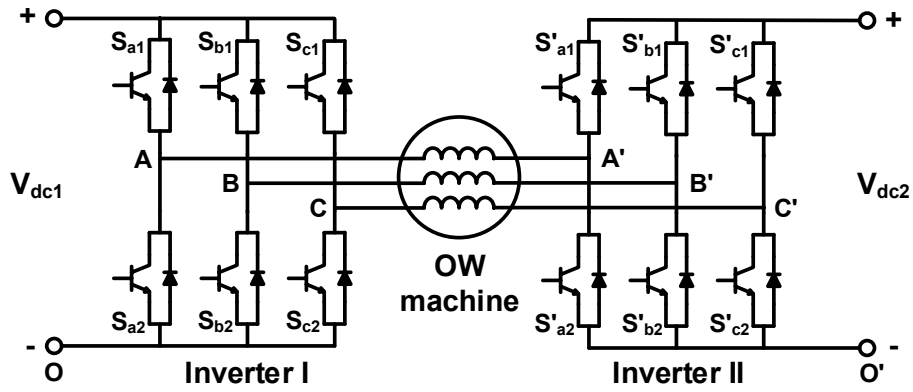
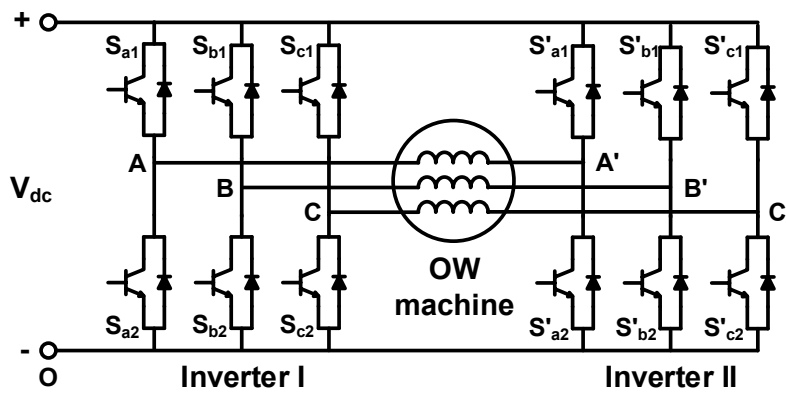


Fig. 1.3 Three type topologies of OW-PMSM drive.

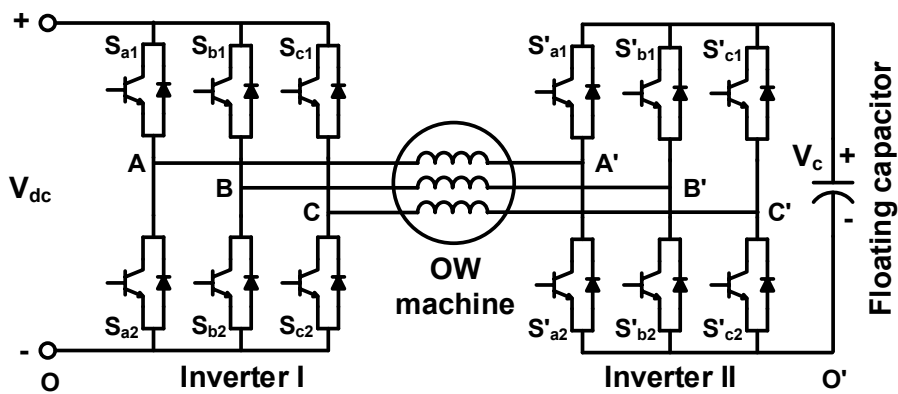
DTL-VSIs can increase the hexagonal modulation region compared with a two-level inverter, and the hexagonal modulation region is determined by DC-bus voltages of two inverters. Taking the DC-bus voltage ratio of 1:1 as an example, the space vector planes of two two-level inverters are shown in Fig. 1.5, and there are 6 effective voltage vectors and 2 zero voltage vectors with the same location, consequently 7 vector locations in total. The space vector plane of DTL-VSIs with a 1:1 DC-bus voltage ratio is shown in Fig. 1.6. There are 64 switching combinations corresponding to 64 basic vectors and 19 vector locations, which are much more than these in a two-level inverter. As a result, there are more redundant vectors that can be used to design PWM strategies, and thus, it has the potential to improve the performance of the control system. Each two-level inverter has 8 switching states corresponding to 8 voltage vectors, and the combinations of two switching states from two inverters are switching combinations for the OW drive. For example, Inverter I switching state is 1 (100) when the states of three up switching devices are “on”, “off” and “off”, and the switching state of Inverter II is 4' (011). These individual states of the two inverters together form the switching combination ‘14’ for the OW drive, which is located at ‘G’ in the space vector plane as shown in Fig. 1.6.



(a) Isolated DC-bus.



(b) Common DC-bus.



(c) Floating capacitor.

Fig. 1.4 Three topologies of DTL-VSIs.

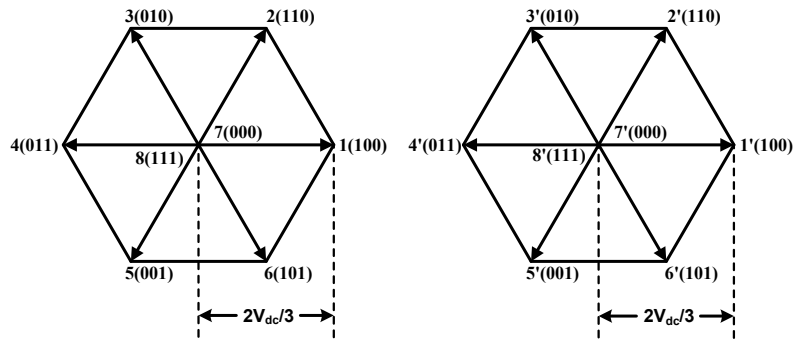


Fig. 1.5 Voltage vectors for Inverter I and Inverter II with 1:1 DC-bus voltage ratio.

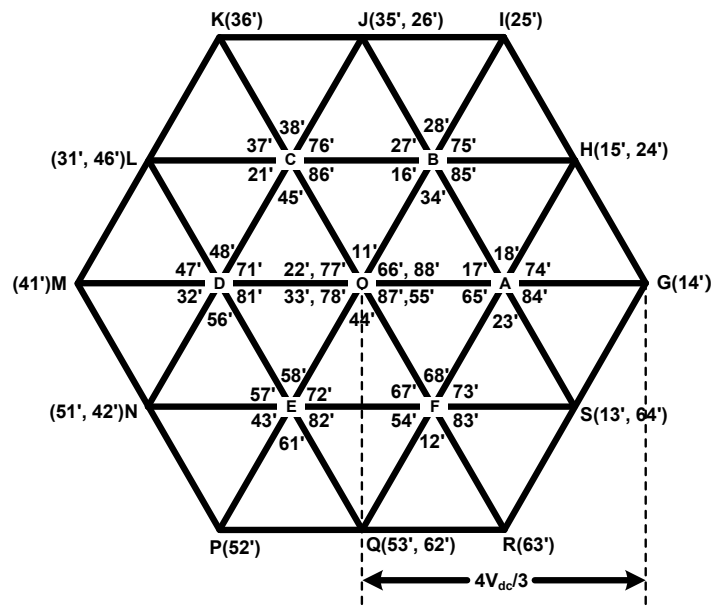


Fig. 1.6 Voltage vectors for OW drive.

For the common DC-bus topology, the DC-bus voltage ratio of two inverters is always 1:1. However, the DC-bus voltage ratios of isolated and floating capacitor topologies can be variable. Fig. 1.7 shows the locations of the vector 34' in the space vector planes with DC-bus voltage ratios of 1:2 and 2:1. The magnitudes of vector 3 and vector 4' change with the ratio between the two DC-bus voltages, so the synthesized vector 34' has different locations in the two space vector planes of DTL-VSIs as shown in Fig. 1.7. Fig. 1.8 shows space vector planes of DTL-VSIs with unequal DC-bus voltage ratios. It can be observed that locations of switching combinations are different with different voltage ratios. DTL-VSIs can generate three-level voltages when the voltage ratio is 1:1, and four-level voltages when the voltage ratio is 1:2 or 2:1. If the voltage ratio is 1:3 or 3:1, DTL-VSIs cannot generate typical three or four-level voltages.

DTL-VSIs can increase the hexagonal modulation region compared with a two-level inverter,

so that the DC-bus voltage utilization can be increased, but the increments are different for different topologies. For the isolated DC-bus topology, the whole hexagonal modulation region can be utilized without any restrictions. However, due to the control of zero sequence current (ZSC) in the common DC-bus topology and the control of capacitor voltage in the floating capacitor topology, the whole hexagonal modulation region cannot be fully utilized. Moreover, the modulation region also has a close relationship with the two DC-bus voltages in isolated and floating capacitor topologies.

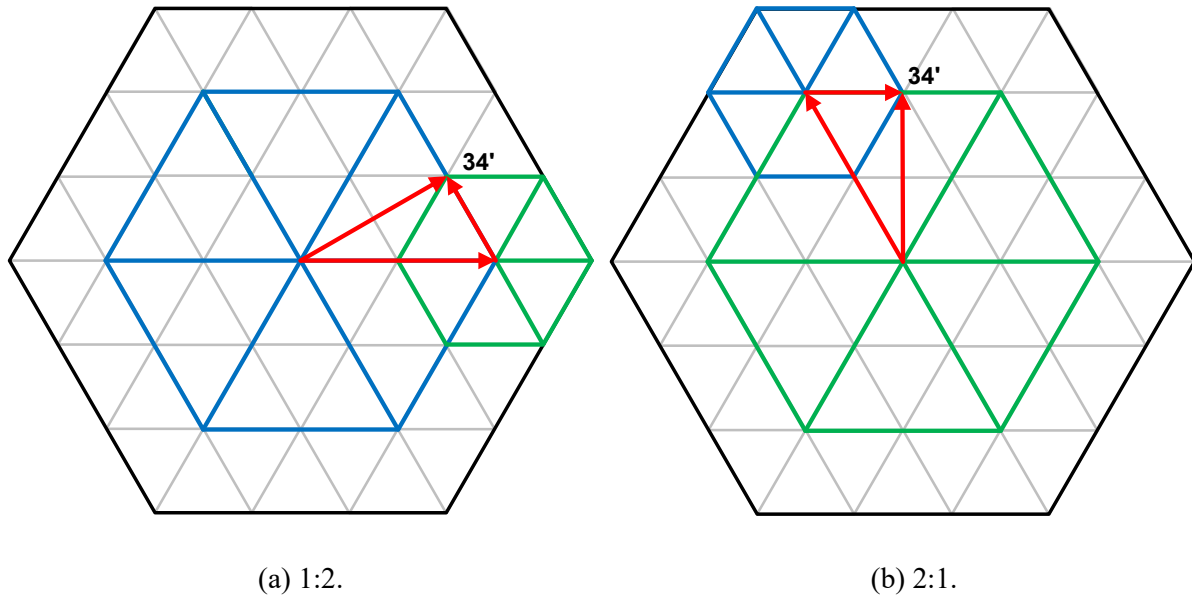
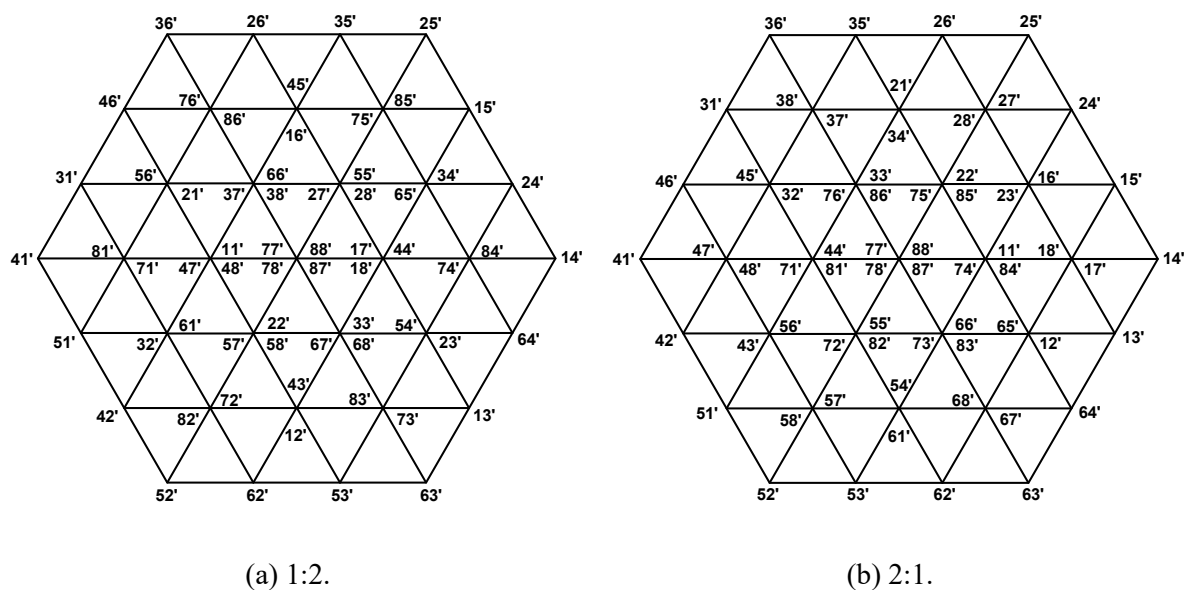


Fig. 1.7 Locations of vector  $34'$  in the space vector planes of DTL-VSIs with 1:2 and 2:1 DC-bus voltage ratios.



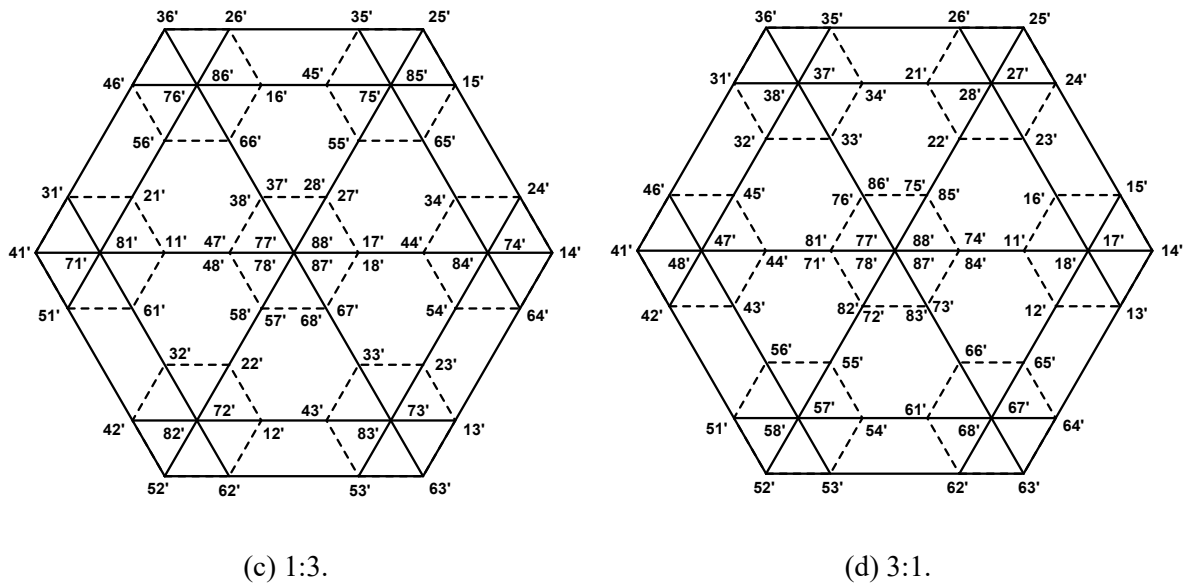


Fig. 1.8 Space planes for DTL-VSIs with different DC-bus voltage ratios.

### 1.4 Isolated DC-bus Dual Inverters

An OW machine fed by isolated DC-bus DTL-VSIs with DC-bus voltages of  $V_{dc1}$  and  $V_{dc2}$  is shown in Fig. 1.4 (a), where O and O' are two isolated grounds for Inverters I and II. The isolated DC-bus dual inverters have the advantages of multilevel output voltages, larger voltage utilization, and lower control complexity, compared with other two OW topologies. However, the isolation between two inverters can increase the cost. In this section, the control strategies of OW machines fed by isolated DC-bus dual inverters will be described in terms of PWM strategies, CMV control, over charge of capacitors, and fault tolerant control as shown in Fig. 1.9.

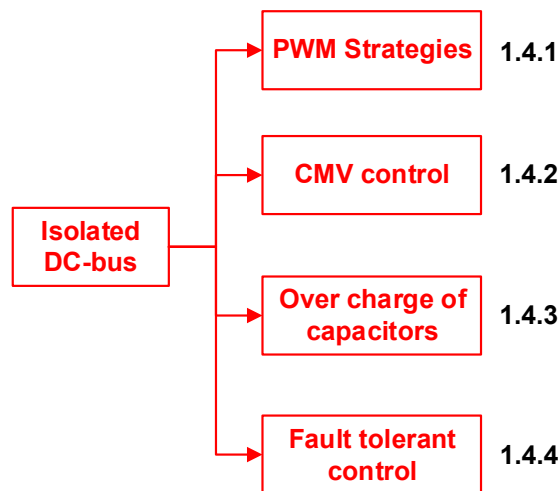


Fig. 1.9 Control strategies of OW machines fed by isolated DC-bus dual inverters.



Three phase voltages of an OW machine fed by isolated DC-bus dual inverters can be given by

$$\begin{cases} V_A = V_{AO} - V_{A'O'} + V_{OO'} \\ V_B = V_{BO} - V_{B'O'} + V_{OO'} \\ V_C = V_{CO} - V_{C'O'} + V_{OO'} \end{cases} \quad (1.4)$$

where  $V_{AO}$ ,  $V_{BO}$ , and  $V_{CO}$  are the pole voltages of Inverter I, while  $V_{A'O'}$ ,  $V_{B'O'}$ , and  $V_{C'O'}$  are the pole voltages of Inverter II,  $V_{OO'}$  is the zero sequence voltage (ZSV) across the points O and O',  $V_A$ ,  $V_B$ , and  $V_C$  are the three phase voltages of the OW machine.

The voltage vectors of Inverters I and II are

$$\begin{aligned} \mathbf{V}_{s1} &= \frac{2}{3} \left( V_{AO} e^{j0} + V_{BO} e^{j2\pi/3} + V_{CO} e^{-j2\pi/3} \right) \\ \mathbf{V}_{s2} &= \frac{2}{3} \left( V_{A'O'} e^{j0} + V_{B'O'} e^{j2\pi/3} + V_{C'O'} e^{-j2\pi/3} \right) \end{aligned} \quad (1.5)$$

The synthesis voltage vector of the OW machine fed by dual inverters can be given by

$$\mathbf{V}_s = \frac{2}{3} \left( V_A e^{j0} + V_B e^{j2\pi/3} + V_C e^{-j2\pi/3} \right). \quad (1.6)$$

According to (1.4) -(1.6), the synthesis voltage vector of dual inverters can be expressed as the difference between voltage vectors of Inverters I and II.

$$\mathbf{V}_s = \mathbf{V}_{s1} - \mathbf{V}_{s2}. \quad (1.7)$$

### 1.4.1 PWM strategies

For an OW machine fed by isolated DC-bus dual inverters with different DC-bus voltage ratios, the space vector planes are different, so that different PWM strategies are needed for different types of voltage ratio as shown in Fig. 1.10. For the fixed DC-bus voltage ratio, the symmetrical voltage ratio, i.e. 1:1, is the most popular one, while the asymmetric voltage ratio, such as 2:1, can increase the quality of voltage profiles. Many PWM strategies are proposed for the symmetrical DC-bus voltage ratio [SHI01] [SRI13] [SRI08] [SEK13] and asymmetric DC-bus voltage ratio [RED11] [RED18]. However, these PWM strategies can only be used for the fixed DC-bus voltage ratios, and are not suitable for the arbitrary DC-bus voltage ratio. A generalized PWM should be used for the arbitrary DC-bus voltage ratio [CHE17] [HUA19b].

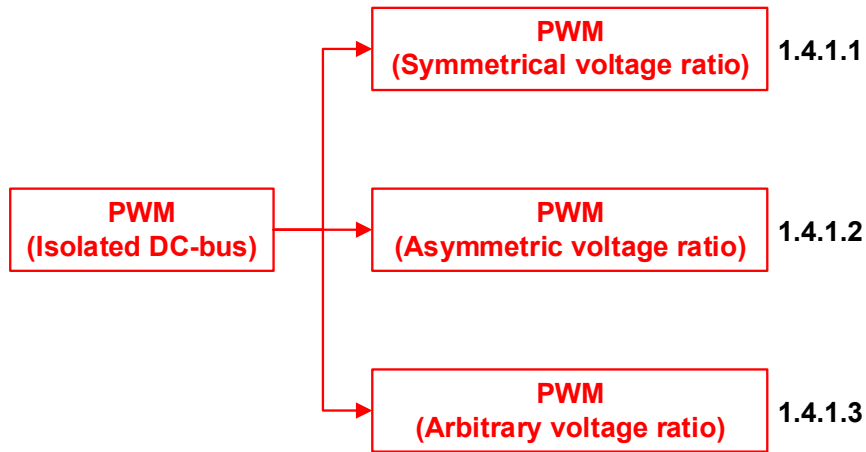


Fig. 1.10 PWM of isolated DC-bus OW drive with different types of DC-bus voltage ratio.

#### 1.4.1.1. Symmetrical DC-bus voltage ratio

For an isolated DC-bus OW drive with the symmetrical DC-bus voltage ratio, the two inverters have the same DC-bus voltage, and the OW drive can output three-level voltages. Fig. 1.11 shows some popular PWM strategies for isolated DC-bus dual inverters with the symmetrical voltage ratio, i.e. conventional SVPWM, sub-hexagonal centred PWM (SHCPWM), alternate SHCPWM, and they will be reviewed in this section.

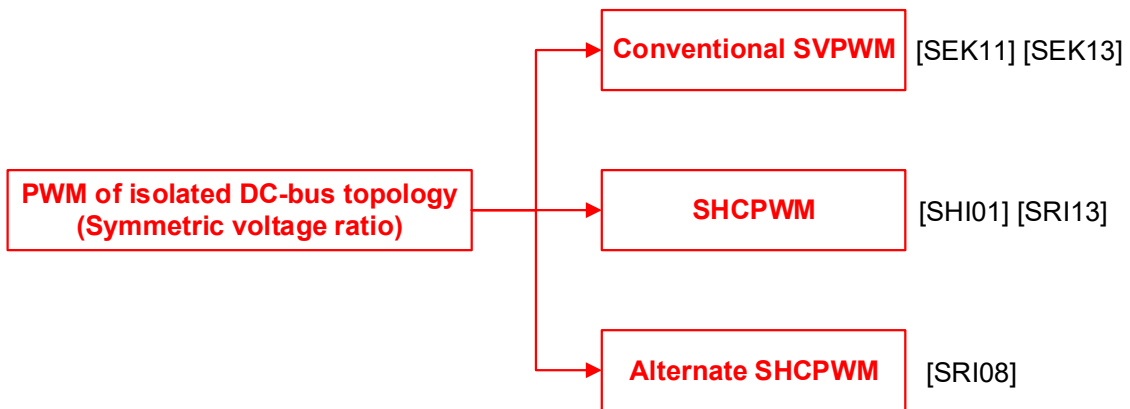


Fig. 1.11 Some popular PWM strategies for the isolated DC-bus OW drive with symmetrical DC-bus voltage ratio.

According to (1.7), the reference voltage vector for an OW drive can be decomposed into two reference voltage vectors for two inverters. In the conventional SVPWM strategy [SEK11], the reference voltage vector for dual inverters in Fig. 1.12 can be decomposed to two reference voltage vectors for two inverters with the same magnitude and opposite directions as shown in Fig. 1.13.

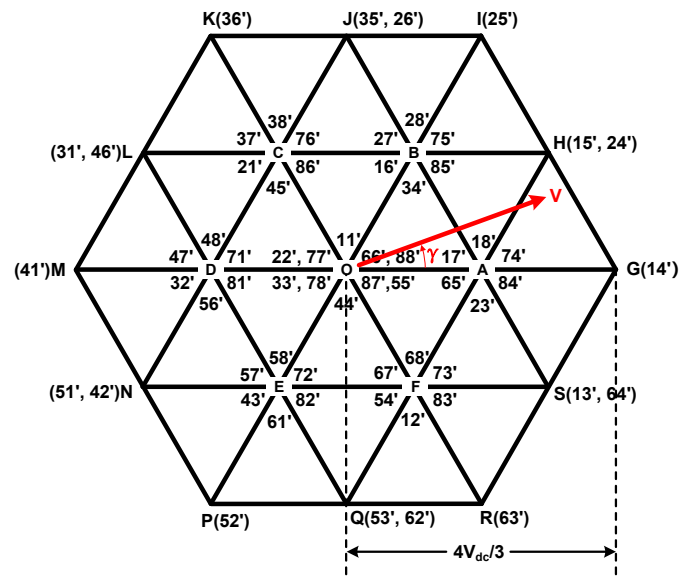


Fig. 1.12 Reference voltage vector in the space vector plane of DTL-VSIs.

The SVPWM strategy is widely used in the electrical machine drive fed by a two-level inverter due to the metres of high voltage utilization and low current/voltage harmonics, and can clearly show voltage vectors, vector durations, and vector action sequences. By applying two SVPWM strategies with the reference voltages for two two-level inverters, the conventional SVPWM strategy for the isolated DC-bus OW drive can be realized. PWM waveforms of the conventional SVPWM strategy for the isolated DC-bus OW drive are shown in Fig. 1.14. It can be observed that zero vectors are always used, even when the reference voltage vector is outside the small hexagon. As a result, the conventional SVPWM strategy does not have the optimal selection of basic voltage vectors.

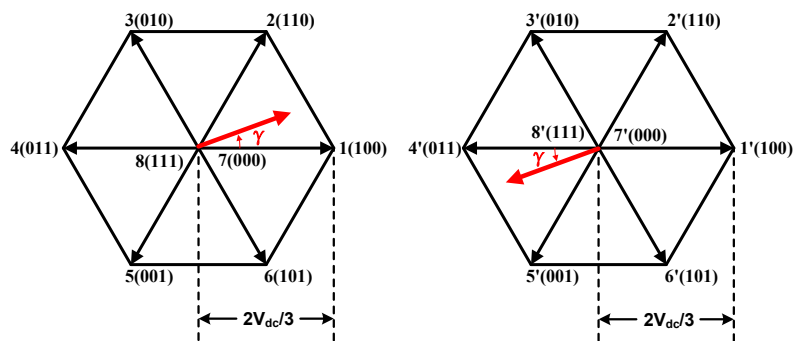


Fig. 1.13 Reference voltage vector for two two-level inverters.

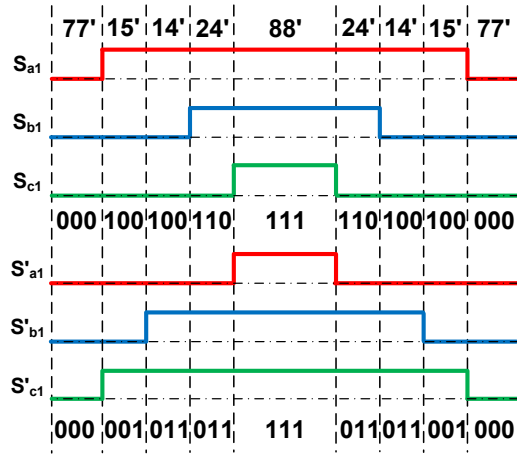


Fig. 1.14 PWM waveforms of conventional SVPWM for isolated DC-bus OW drive.

Compared with SVPWM strategies, SPWM strategies have the advantage of easy implementation due to the absence of sector and vector duration calculations. The conventional SVPWM can be realized by SPWM, and the two inverters are controlled independently [SEK13]. Each individual inverter is controlled by SPWM strategy as shown in Fig. 1.15, which can simply transform reference voltages of each inverter to duty cycles. To improve the voltage utilization of SPWM strategy, two ZSVs need to be injected to reference voltages of two inverters, respectively. The reference voltage of the OW drive in each phase is distributed to reference voltages of two inverters with the same magnitude but opposite signs in the conventional SPWM strategy. This SPWM strategy has the same performance as the SVPWM strategy, such as maximum modulation region and current harmonics, but the implementation is much easier.

The SHCPWM strategy can achieve the optimal selection of voltage vectors, and the reference voltage vector of the OW drive can always be synthesized by three nearest basic vectors [SHI01] [SRI13]. Moreover, the switching actions in a PWM cycle can be reduced by half compared with the conventional SVPWM strategy. The space vector plane of dual inverters can be divided into 6 sectors as shown in Fig. 1.16. Each sector can be regarded as parts of a small hexagon, and there are six small hexagons corresponding to six sectors with six centres, i.e. A, B, C, D, E, F. With the decomposition of the reference voltage vector for the OW drive, a two-level inverter can be always kept in an effective voltage vector state in a PWM cycle, while the other two-level inverter can generate voltages with SVPWM. Taking the sector 1 as an example, the reference voltage vector  $\vec{OV}$  is decomposed into two parts,  $\vec{OA}$  and  $\vec{AV}$  in Fig. 1.16, which are generated by two individual inverters. For instance,  $\vec{OA}$  is the output voltage vector of

Inverter I which is clamped on 1 (100) state. At the same time,  $\overline{AV}$  is realized by Inverter II with the principle of SVPWM strategy. Alternatively,  $\overline{OA}$  can be generated by Inverter II which is clamped on 4 (011) state, and  $\overline{AV}$  is the output voltage vector of Inverter I. With the clamping of Inverter I or Inverter II, reference voltage vectors for two two-level inverters and PWM waveforms of the OW drive are shown in Fig. 1.17 (a) and (b), respectively.

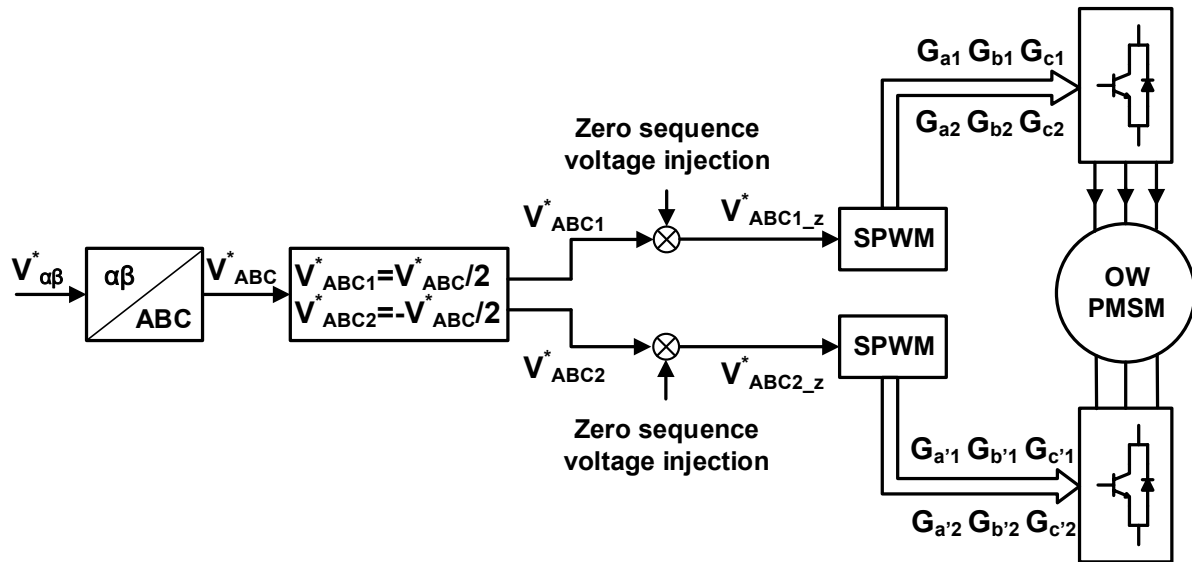


Fig. 1.15 Control diagram of SPWM for isolated DC-bus dual inverters.

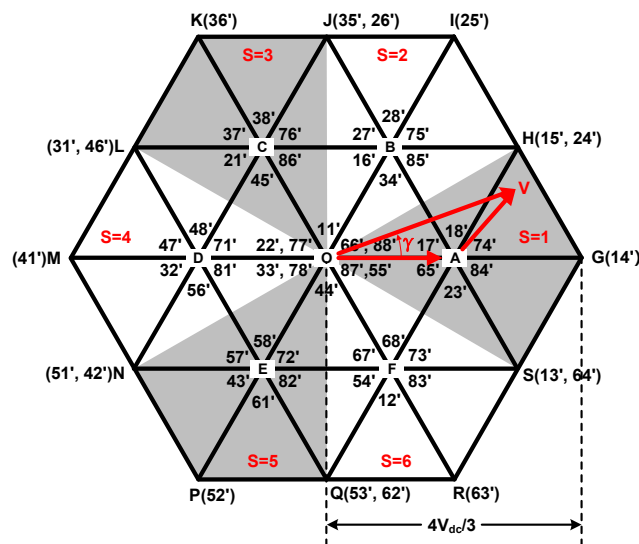
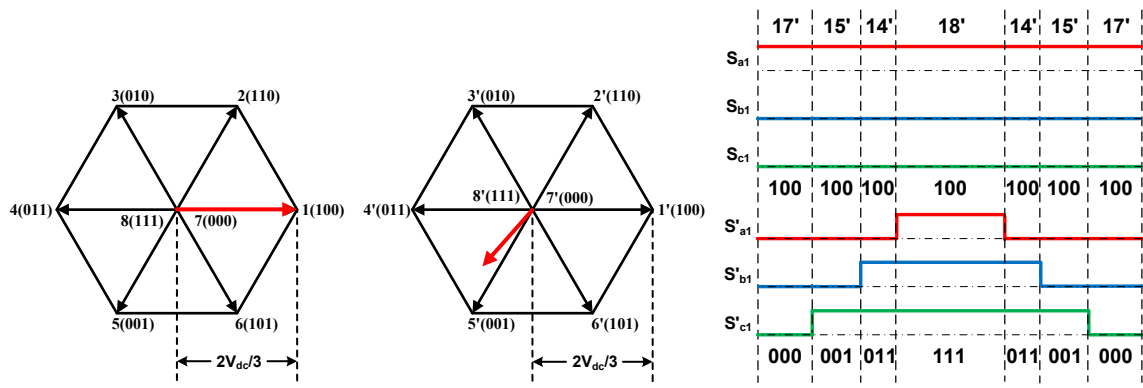
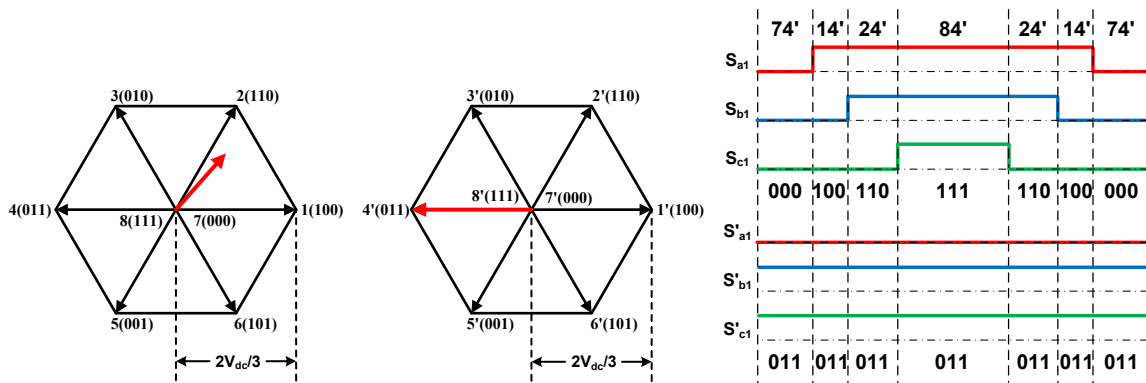


Fig. 1.16 Sector division and decomposition of reference voltage vector for OW drive in the SHCPWM.



(a) Inverter I clamped.



(b) Inverter II clamped.

Fig. 1.17 Reference voltage vectors for two two-level inverters and PWM waveforms of OW drive.

If one inverter is clamped all the time and the other one is always switched, then the temperature rises of two inverters will be different. To balance the operation of two inverters, the alternate SHCPWMs are introduced, in which two inverters are clamped alternately [SRI08]. Considering the clamping states of two inverters, there are four SHCPWMs. In SHCPWM1 strategy, Inverter II is clamped all the time, while Inverter I is always switched in SHCPWM2 strategy. Inverters I and II are clamped alternately in SHCPWM3 and SHCPWM4 strategies. In SHCPWM3 strategy, Inverter I is switched in sectors 1, 3, and 5, and clamped in sectors 2, 4, and 6, while Inverter II is switched in sectors 2, 4, and 6, and clamped in sectors 1, 3, and 5. In SHCPWM4 strategy the switching states of two inverters are exchanged compared with SHCPWM3 strategy, i.e. Inverter I is switched in sectors 2, 4, and 6 and clamped in sectors 1, 3, and 5, while Inverter II is switched in sectors 1, 3, and 5 and clamped in sectors 2, 4, and 6.

When one inverter is clamped, the reference voltage vector of the switched inverter should be acquired to realize SVPWM strategy. From (1.7), the reference voltage of the switched inverter can be calculated.

If Inverter I is clamped, the reference voltage vector of Inverter II is

$$\mathbf{V}_{s2} = \mathbf{V}_{s1} - \mathbf{V}_s. \quad (1.8)$$

If Inverter II is clamped, the reference voltage vector of Inverter I is

$$\mathbf{V}_{s1} = \mathbf{V}_s + \mathbf{V}_{s2}. \quad (1.9)$$

Taking SHCPWM4 as an example, the reference voltages of two inverters in  $\alpha$ - and  $\beta$ -axes are shown in Table 1.1. The reference voltages of the switched inverter in other SHCPWM strategies can be calculated similarly.

In SHCPWM strategies, due to the change of clamping state for two inverters in different sectors, switching commutations can be generated during the sector change. The commutations should be considered since it can affect the switching loss of dual inverters especially in the high frequency operation. To analyse the number of commutations of these four SHCPWM strategies, the PWM waveforms of sectors 1 and 2 are illustrated. Fig. 1.18 shows the PWM waveforms of SHCPWM1 strategy in sectors 1 and 2. It can be observed that one commutation accrues at the switch  $S'_{b1}$ . Fig. 1.19 shows the PWM waveforms of SHCPWM2 strategy in sector 1 and sector 2. There is also only one commutation during sector change, but it happens at the switch  $S_{b1}$ . As the initial switching state of the switched inverter is always 7 (000), so that the commutation will never accrues in the switched inverter for SHCPWM1 and SHCPWM2 strategies. On the other hand, Fig. 1.18 and Fig. 1.19 show that the commutation always happens in the clamped inverter in SHCPWM1 and SHCPWM2 strategies.

The PWM waveforms of SHCPWM strategies with alternate inverter clamping (SHCPWM3 and SHCPWM4) are shown in Fig. 1.20 and Fig. 1.21, and the numbers of commutations are four and two during sector change, respectively. Although SHCPWM3 and SHCPWM4 strategies can solve the problem of unbalanced operation in two inverters, they also induce the increase of commutations during sector change.

Table 1.1 Reference Voltages of Two Individual Inverters in SHCPWM4 Strategy

Sector	Inverter I	Inverter II
1	$V_{ref\alpha 1} = 2V_{dc}/3$ $V_{ref\beta 1} = 0$	$V_{ref\alpha 2} = -V_{ref\alpha} + V_{dc}/3$ $V_{ref\beta 2} = -V_{ref\beta}$
2	$V_{ref\alpha 1} = V_{ref\alpha} - V_{dc}/3$ $V_{ref\beta 1} = V_{ref\beta} - \sqrt{3}V_{dc}/3$	$V_{ref\alpha 2} = -V_{dc}/3$ $V_{ref\beta 2} = -\sqrt{3}V_{dc}/3$
3	$V_{ref\alpha 1} = -V_{dc}/3$ $V_{ref\beta 1} = \sqrt{3}V_{dc}/3$	$V_{ref\alpha 2} = -V_{ref\alpha} - V_{dc}/3$ $V_{ref\beta 2} = -V_{ref\beta} + \sqrt{3}V_{dc}/3$
4	$V_{ref\alpha 1} = V_{ref\alpha} + 2V_{dc}/3$ $V_{ref\beta 1} = V_{ref\beta}$	$V_{ref\alpha 2} = 2V_{dc}/3$ $V_{ref\beta 2} = 0$
5	$V_{ref\alpha 1} = -V_{dc}/3$ $V_{ref\beta 1} = -\sqrt{3}V_{dc}/3$	$V_{ref\alpha 2} = -V_{ref\alpha} - V_{dc}/3$ $V_{ref\beta 2} = -V_{ref\beta} - \sqrt{3}V_{dc}/3$
6	$V_{ref\alpha 1} = V_{ref\alpha} - V_{dc}/3$ $V_{ref\beta 1} = V_{ref\beta} + \sqrt{3}V_{dc}/3$	$V_{ref\alpha 2} = -V_{dc}/3$ $V_{ref\beta 2} = \sqrt{3}V_{dc}/3$

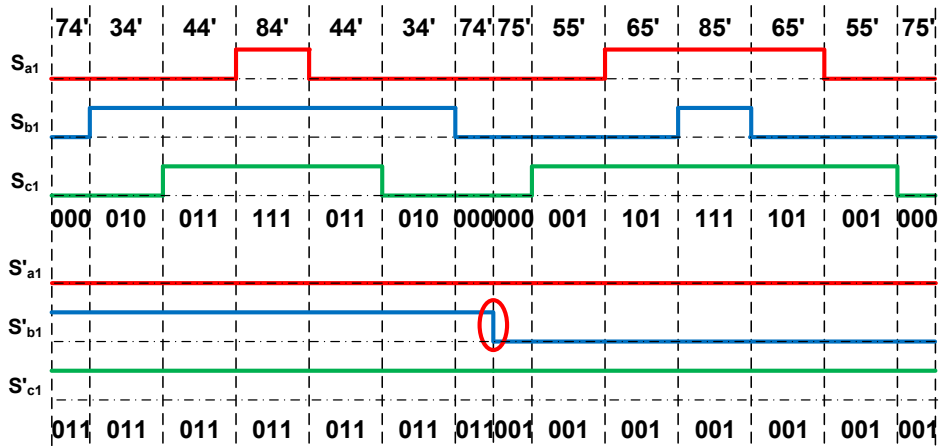


Fig. 1.18 SHCPWM1 waveforms in sectors 1 and 2.



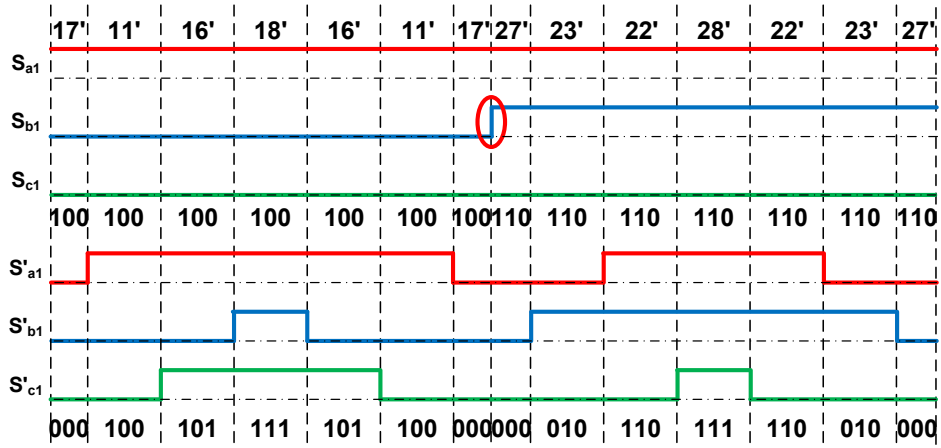


Fig. 1.19 SHCPWM2 waveforms in sectors 1 and 2.

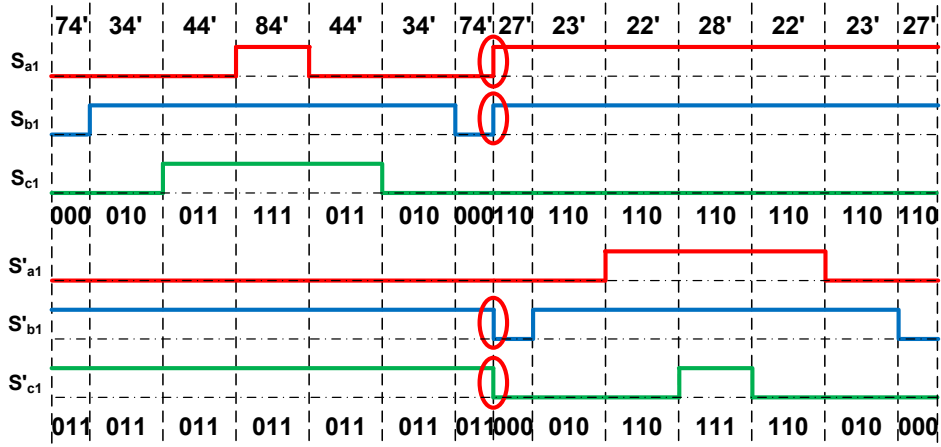


Fig. 1.20 SHCPWM3 waveforms in sectors 1 and 2.

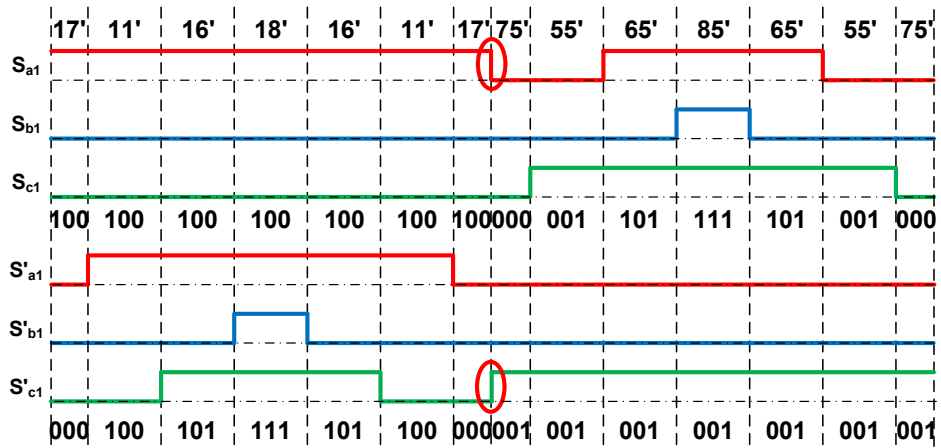


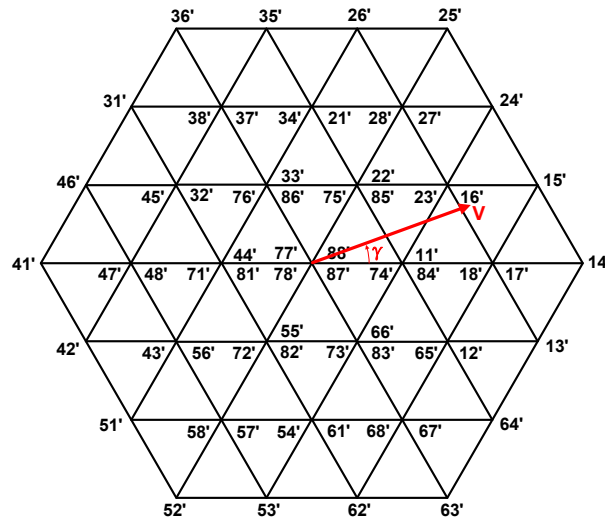
Fig. 1.21 SHCPWM4 waveforms in sectors 1 and 2.

### 1.4.1.2. Asymmetric DC-bus voltage ratio

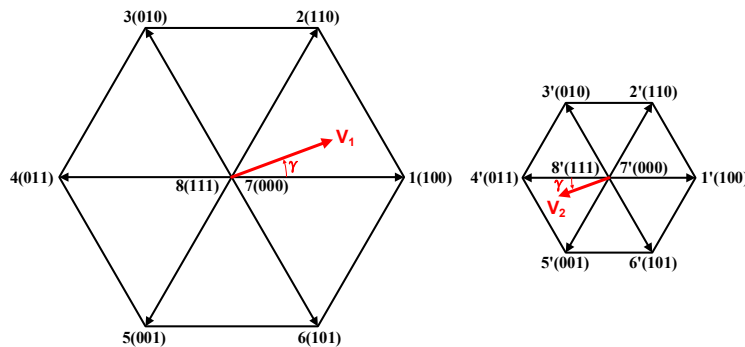
Compared with three-level output voltages of isolated DC-bus dual inverters with a 1:1 DC-bus voltage ratio, dual inverters with a 2:1 voltage ratio can generate four-level voltages. The SVPWM for dual inverters with a 2:1 voltage ratio is proposed in [RED11], the reference voltage vector of the OW drive is decomposed into two vectors for two inverters with the opposite directions and a magnitude ratio of 2:1 as shown in Fig. 1.22.

$$\begin{aligned} \mathbf{V}_{s1} &= 2\mathbf{V}_s / 3 \\ \mathbf{V}_{s2} &= -\mathbf{V}_s / 3 \end{aligned} \quad (1.10)$$

where  $\mathbf{V}_s$  is the voltage vector for the OW drive,  $\mathbf{V}_{s1}$  and  $\mathbf{V}_{s2}$  are the voltage vectors for Inverters I and II, respectively.



(a) Voltage vector of OW drive.



(b) Voltage vectors of two inverters.

Fig. 1.22 Decomposition of voltage vectors.

Fig. 1.23 shows PWM waveforms of isolated DC-bus dual inverters with a 2:1 DC-bus voltage ratio in sector 1. The SVPWM can also be realized by SPWM with easy implementation in [RED18].

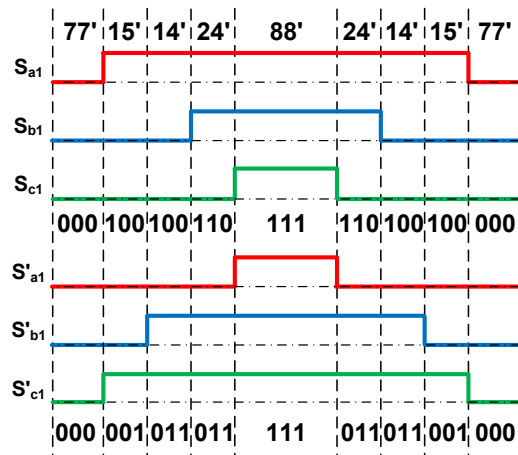


Fig. 1.23 PWM waveforms of isolated DC-bus OW drive with 2:1 DC-bus voltage ratio.

#### 1.4.1.3. Arbitrary DC-bus voltage ratios

A generalized PWM strategy is proposed for an OW machine fed by isolated DC-bus dual inverters with arbitrary DC-bus voltage ratio between two voltage supplies in [CHE17]. The space vector plane of dual inverters is divided into six sectors, and each sector is further divided into three regions as shown in Fig. 1.24.

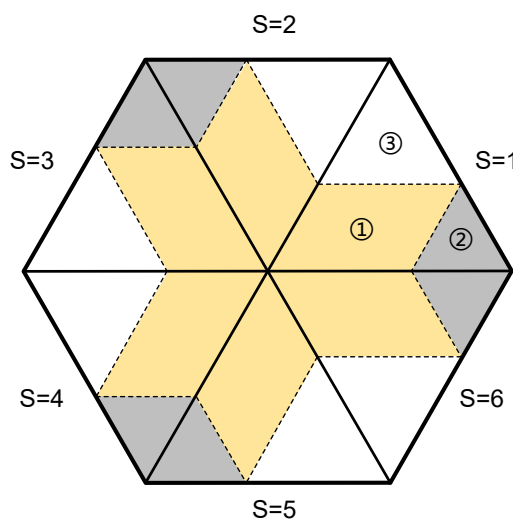


Fig. 1.24 Sector division of the SVPWM in [CHE17].

When the reference voltage vector is located in three different regions in sector 1, the reference voltage vector of the OW drive can be decomposed into basic vectors of two inverters as shown

in Fig. 1.25.  $\mathbf{V}_{1x}$  and  $\mathbf{V}_{1y}$  are two basic vectors of Inverter I, while  $\mathbf{V}_{2x}$  and  $\mathbf{V}_{2y}$  are two basic vectors of Inverter II. The syntheses of  $\mathbf{V}_{1x}$  and  $\mathbf{V}_{2x}$ ,  $\mathbf{V}_{1y}$  and  $\mathbf{V}_{2y}$  are  $\mathbf{V}_x$  and  $\mathbf{V}_y$ , respectively.

$$\begin{aligned} \mathbf{V}_x &= \mathbf{V}_{1x} + \mathbf{V}_{2x} \\ \mathbf{V}_y &= \mathbf{V}_{1y} + \mathbf{V}_{2y} \end{aligned} \quad (1.11)$$

The durations of  $\mathbf{V}_x$  and  $\mathbf{V}_y$  can be calculated as

$$\begin{aligned} t_x &= \frac{\sqrt{3}V_{ref}}{V_{dc1}} T_{PWM} \sin\left(\frac{\pi}{3} - \theta\right) = t_{1x} + t_{2x} / k \\ t_y &= \frac{\sqrt{3}V_{ref}}{V_{dc2}} T_{PWM} \sin\theta = kt_{1y} + t_{2y} \end{aligned} \quad (1.12)$$

where  $V_{ref}$  is the magnitude of the reference voltage vector,  $T_{PWM}$  is the duration of a PWM cycle.  $t_{1x}$ ,  $t_{2x}$ ,  $t_{1y}$  and  $t_{2y}$  are the durations of basic vectors  $\mathbf{V}_{1x}$ ,  $\mathbf{V}_{2x}$ ,  $\mathbf{V}_{1y}$ , and  $\mathbf{V}_{2y}$ ,  $k=V_{dc1}/V_{dc2}$ .

Durations of basic voltage vectors for Inverters I and II in three different regions are shown in Table 1.2. PWM waveforms in three different regions in sector 1 are shown in Fig. 1.25. It can be seen that only two of six legs in the dual inverters are switched and the other legs are clamped in a PWM cycle. As a result, the switching actions in a PWM cycle can be reduced by 2/3 compared with the conventional SVPWM for isolated DC-bus dual inverters.

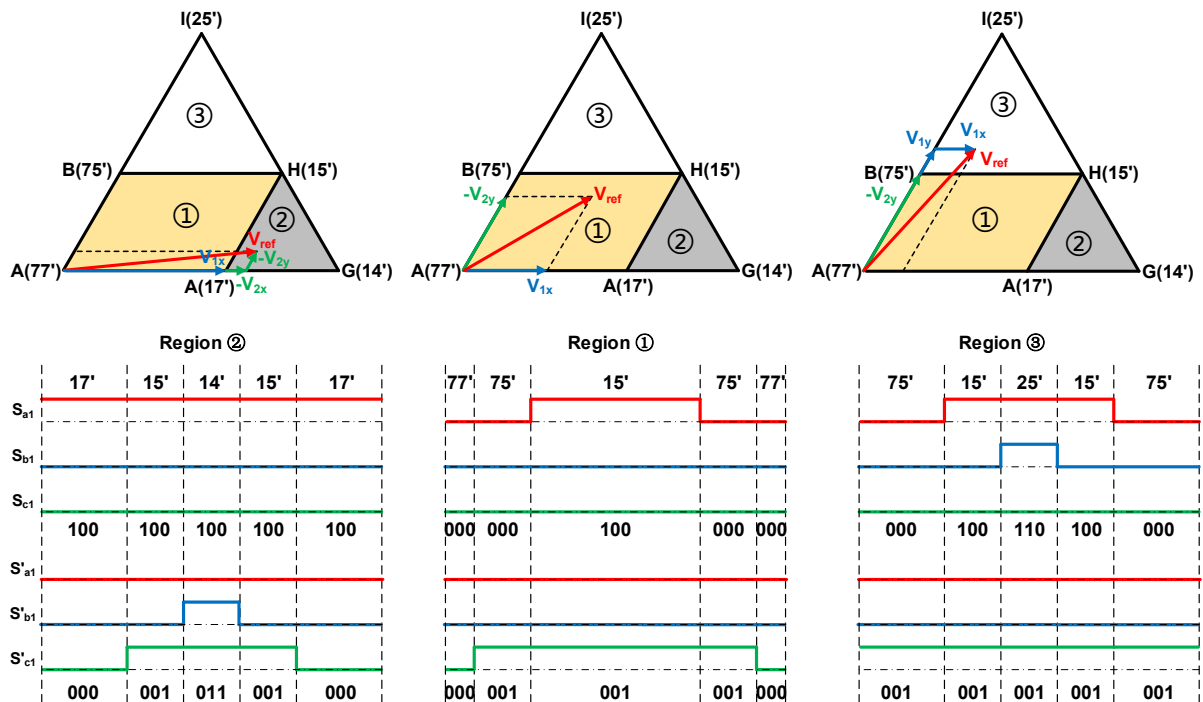


Fig. 1.25 Voltage vectors and PWM waveforms of the PWM in sector 1 [CHE17].

The PWM strategy in [CHE17] is optimized with low current harmonics in low modulation regions in [HUA19b]. A 180-degree phase shift of the carrier signal is applied for Inverter II in region 1 in [HUA19b] and the PWM waveforms in three different regions in sector 1 are shown in Fig. 1.26.

For the PWM strategy in [CHE17], there is no switching commutation in low modulation regions, where the reference voltage vector is located in region 1. However, two commutations exist during the region change in high modulation regions. As a result, there are 12 commutations in an electrical cycle in high modulation regions. For the modified PWM strategy in [HUA19b], there are 6 commutations in an electrical cycle in low modulation regions, and 12 commutations in an electrical cycle in high modulation regions.

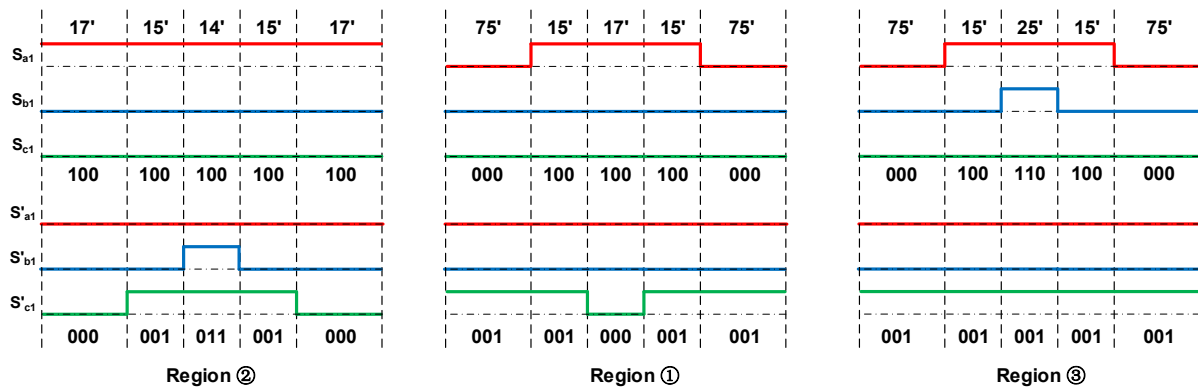


Fig. 1.26 PWM waveforms of the modified PWM in sector 1 [HUA19b].

Table 1.2 Durations of Voltage Vectors for Two Inverters

Regions Vectors	Region 1 ( $t_x \leq T_{PWM}, t_y \leq T_{PWM}$ )	Region 2 ( $t_x > T_{PWM}, t_y \leq T_{PWM}$ )	Region 3 ( $t_x \leq T_{PWM}, t_y > T_{PWM}$ )
Inverter I $V_{1x}$	$t_{1x} = t_x$	$t_{1x} = T_{PWM}$	$t_{1x} = t_x$
Inverter I $V_{1y}$	$t_{1y} = 0$	$t_{1y} = 0$	$t_{1y} = (t_y - T_{PWM})/k$
Inverter II $V_{2x}$	$t_{2x} = 0$	$t_{2x} = k(t_x - T_{PWM})$	$t_{2x} = 0$
Inverter II $V_{2y}$	$t_{2y} = t_y$	$t_{2y} = t_y$	$t_{2y} = T_{PWM}$

## 1.4.2 CMV control

The variation of CMV can cause the shaft voltage variation, and thus generate bearing current in an OW-PMSM fed by isolated DC-bus DTL-VSIs, which may cause the failure of bearings [KAL15]. As a result, the variation of CMV should be reduced to cope with the negative effects.

CMVs of Inverters I and II are

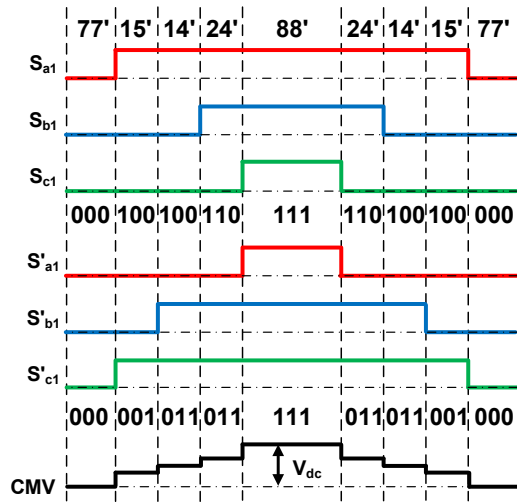
$$\begin{aligned} V_{CMV1} &= (V_{AO} + V_{BO} + V_{CO})/3 \\ V_{CMV2} &= (V_{A'O'} + V_{B'O'} + V_{C'O'})/3 \end{aligned} \quad (1.13)$$

where  $V_{CMV1}$  and  $V_{CMV2}$  are the CMVs of two two-level inverters, respectively.  $V_{AO}$ ,  $V_{BO}$ ,  $V_{CO}$  are the three pole voltages of Inverter I, and  $V_{A'O'}$ ,  $V_{B'O'}$ ,  $V_{C'O'}$  are the three pole voltages of Inverter II.

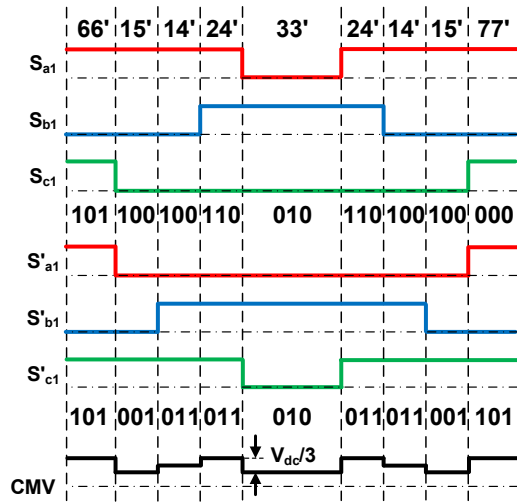
CMV of the OW drive can be expressed as the average of CMVs in two two-level inverters.

$$V_{CMV} = \frac{V_{CMV1} + V_{CMV2}}{2} = \frac{V_{AO} + V_{BO} + V_{CO} + V_{A'O'} + V_{B'O'} + V_{C'O'}}{6}. \quad (1.14)$$

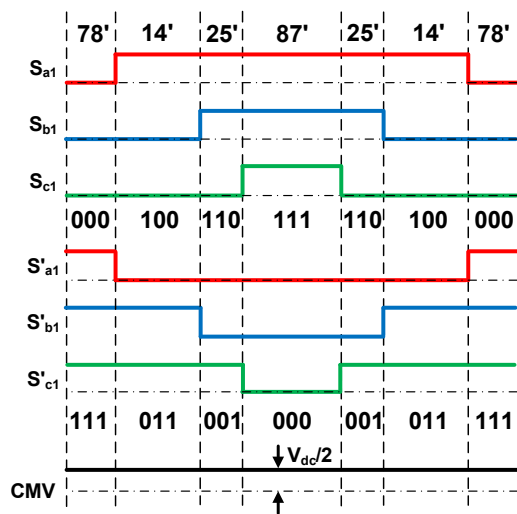
PWM waveforms and CMV of the conventional SVPWM in a PWM cycle are shown in Fig. 1.27 (a). It can be seen that there is a large variation of CMV from 0 to  $V_{dc}$ , which may cause large bearing current. In a two-level inverter, zero vectors can be replaced by two effective vectors with the opposite directions to reduce the variation of CMV. To solve the CMV issue in DTL-VSIs, the CMV variation reduction method of a two-level inverter is applied to the two inverters of the OW drive [KAL13], and PWM waveforms and CMV are shown in Fig. 1.27 (b). It can be seen that the variation of CMV can be reduced to  $V_{dc}/3$ . The phase opposition deposition PWM (POD-PWM) strategy is well known as the advantage of CMV variation elimination in the multilevel inverter [LOH03]. [KAL15] proposed a POD-PWM to eliminate the variation of CMV of an OW drive, two legs of each H-bridge in dual inverters have the same modulation single but the opposite phases of carrier signals. As a result, the PWM waveforms of two legs of each H-bridge are opposite, and the average pole voltage of the two legs is always  $V_{dc}/2$ , so that the CMV of the OW drive can be kept at  $V_{dc}/2$ . Put it another way, it can be seen from Fig. 1.27 (c) that all switching combinations have the same CMV of  $V_{dc}/2$ , so that the CMV can always be kept the same.



(a) Conventional SVPWM.



(b) PWM in [KAL13].



(c) PWM in [KAL15].

Fig. 1.27 PWM waveforms and CMVs with different PWM.

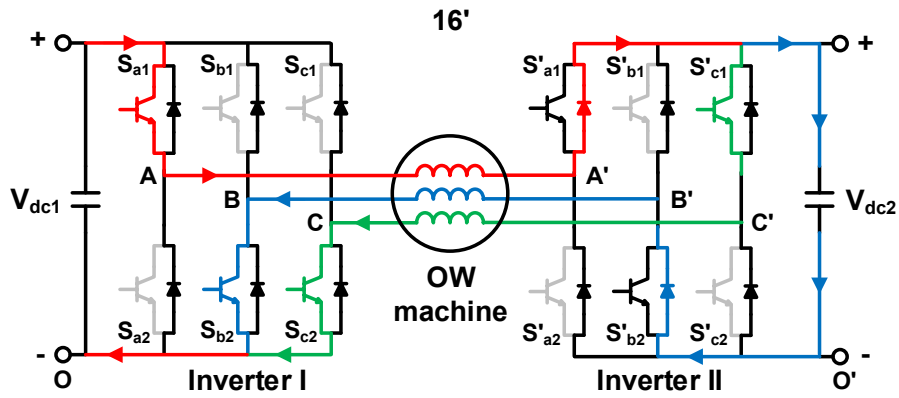
All existing CMV control methods are for the OW drive with a symmetrical DC-bus voltage ratio. For the asymmetric DC-bus voltage ratio, the different DC-bus voltages of two inverters make the control of CMV more complicated.

### 1.4.3 Over charge of capacitors

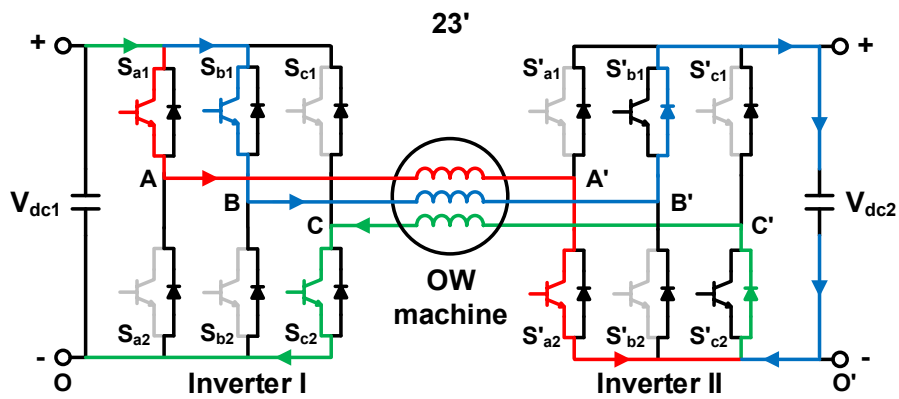
Although an asymmetric dual inverter configuration enables the possibility to improve output quality (e.g. four-level in the DC-bus voltage ratio of 1:2 or 2:1), it increases the risk of overcharging the capacitor in the low-voltage side with unidirectional voltage sources. This situation can eliminate the desired DC-bus voltage ratio and may cause safety issues of the capacitor in the low-voltage side [HUA22]. The overcharge issue can be solved by bidirectional voltage sources for dual inverters [DAR17], which can increase the hardware complexity and cost of system. For a unidirectional voltage source, including uncontrolled rectifier, current can only flow out of the positive terminal, but cannot flow into the positive terminal. In an OW machine fed by isolated DC-bus DTL-VSIs, the two inverters control the same three phase windings, and they also need to provide a current path for each other. The current path may be blocked in an inverter under a certain switching state and current directions. Consequently, the current may flow into the capacitor in dual inverters with unidirectional voltage sources, and cause the charge of the capacitor.

The overcharge issue for an OW machine fed by isolated DC-bus dual inverters with a 2:1 DC-bus voltage ratio is firstly reported in [SOM02b] and studied in [RED11]. Fig. 1.28 shows current flows in dual inverters with two switching combinations 16' and 23', and the overcharge of the capacitor in Inverter II can be seen. To avoid the charge of the capacitor in Inverter II in [RED11], the angle between the voltage vectors of Inverters I and II should be less than 90 degrees. However, the three-phase current directions of the OW drive in [RED11] are assumed to be always the same as the three-phase voltage directions of Inverter I. For example, Inverter I is in the state of vector 1 (100), so that three-phase currents are assumed to be positive, negative, and negative, respectively. The directions of currents and voltages may be different in an OW drive, so that the conclusion in [RED11] is not accurate. This problem is solved in [HUA19c], and an active modulation scheme for avoiding overcharging in dual inverters with asymmetric voltage sources is proposed, which chooses the switching state according to phase current directions.





(a) Switching combination 16'.

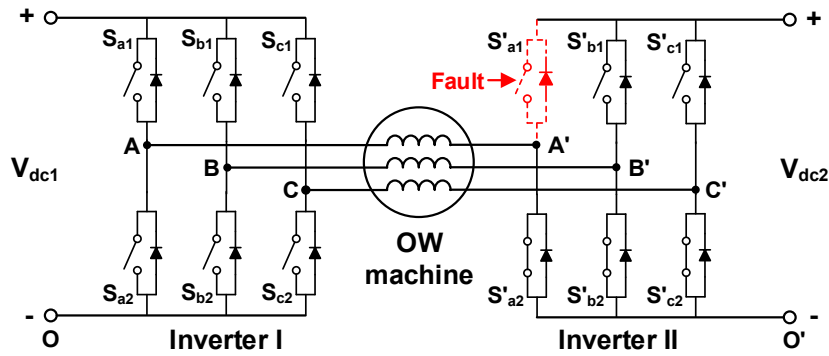


(b) Switching combination 23'.

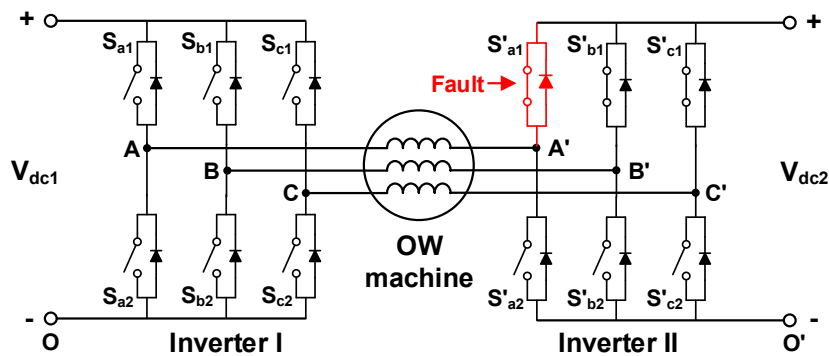
Fig. 1.28 Current flows in dual inverters with two switching combinations 16' and 23' [RED11].

### 1.4.4 Fault tolerant control

Compared with a two-level inverter, the isolated DC-bus OW dual inverters have fault tolerant capability. By creating an artificial neutral, an OW machine fed by isolated DC-bus dual inverters can be operated under a reduced power capability, when a short- or open-circuit fault of switch/diode occurs [WAN11]. As the DTL-VSIs have two independent DC voltage sources, an artificial neutral can be created by turning on all three up or low switching devices of a two-level inverter, and the OW drive becomes a Y-connection three-phase machine fed by the other two-level inverter. For example, if  $S'_{a1}$  has an open-circuit fault, then the three low switching devices, i.e.  $S'_{a2}$ ,  $S'_{b2}$ ,  $S'_{c2}$  are all turned on to short-circuit the three phase windings to the negative DC-bus of Inverter II as shown in Fig. 1.29 (a). On the other hand, if  $S'_{a1}$  is in a short-circuit fault, then the other two up switching devices, i.e.  $S'_{b1}$ ,  $S'_{c1}$  are turned on to short-circuit the three phase windings to the positive DC-bus of Inverter II as shown in Fig. 1.29 (b).



(a) Open-circuit fault.



(b) Short-circuit fault.

Fig. 1.29 Artificial neutral of OW machine fed by isolated DC-bus DTL-VSIs.

Fault tolerant capability of an OW machine fed by isolated DC-bus DTL-VSIs can be further improved by the modification of the inverter topology [ZHA18b]. The leg with the fault switch/diode can be cut off, and the corresponding phase winding is connected to the neutral point of the voltage source to achieve the fault tolerant operation as shown in Fig. 1.30. Compared with the fault tolerant method in [WAN11], the modulation region can be enlarged in the fault tolerant operation in [ZHA18b].

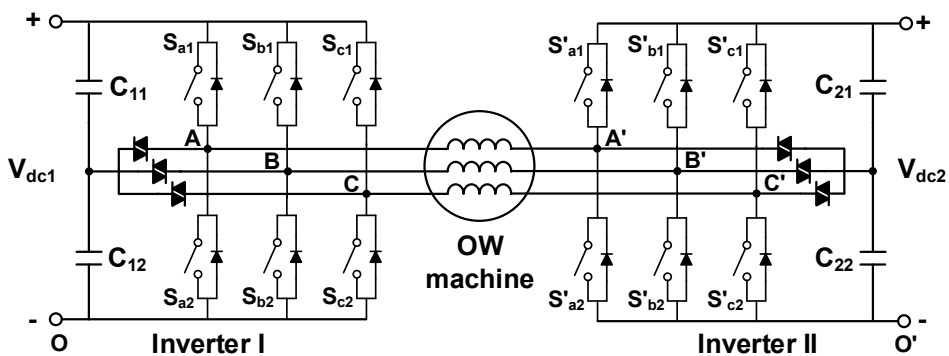


Fig. 1.30 Modified dual inverter topology in [ZHA18b].

## 1.5 Common DC-bus Dual Inverters

In this section, the control strategies of OW machines fed by common DC-bus dual inverters will be described in terms of PWM strategies and ZSC control, CMV control, flux weakening, sensorless, and fault tolerant control, as shown in Fig. 1.31.

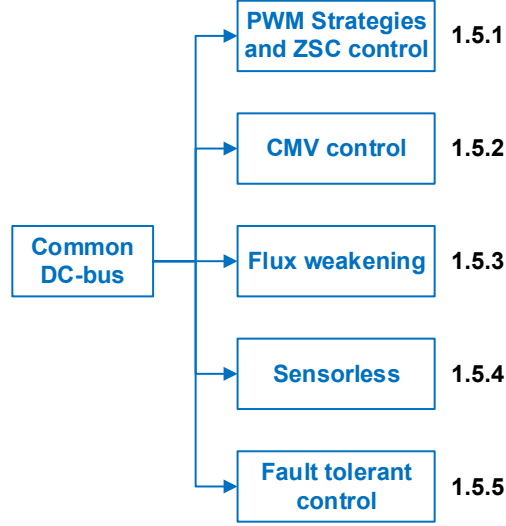


Fig. 1.31 Control strategies of OW machines fed by common DC-bus dual inverters.

An OW machine fed by DTL-VSIs with a common-DC bus is shown in Fig. 1.4 (b). Compared with isolated DC-bus and floating capacitor topologies, the common DC-bus topology has the advantages of controllable ZSC, better fault tolerant capability, and lower cost. However, it has drawbacks of smaller maximum modulation region, more control complexity, and lower level of output voltages compared with the isolated DC-bus topology.

The two inverters have the same ground in the common DC-bus topology, which is different from isolated and floating capacitor topologies, so that the voltage model of an OW machine fed by common DC-bus DTL-VSIs is also different. Three phase voltages of a three phase OW machine fed by common DC-bus DTL-VSIs are given by

$$\begin{cases} V_A = V_{AO} - V_{A'O} \\ V_B = V_{BO} - V_{B'O} \\ V_C = V_{CO} - V_{C'O} \end{cases} \quad (1.15)$$

where  $V_{AO}$ ,  $V_{BO}$ , and  $V_{CO}$  are the pole voltages of Inverter I, while  $V_{A'O}$ ,  $V_{B'O}$ , and  $V_{C'O}$  are the pole voltages of Inverter II,  $V_A$ ,  $V_B$ , and  $V_C$  are the three phase voltages of the OW machine.

The voltage vectors in Inverter I and Inverter II are

$$\begin{aligned} \mathbf{V}_{s1} &= \frac{2}{3} \left( V_{AO} e^{j0} + V_{BO} e^{j2\pi/3} + V_{CO} e^{-j2\pi/3} \right) \\ \mathbf{V}_{s2} &= \frac{2}{3} \left( V_{A'O} e^{j0} + V_{B'O} e^{j2\pi/3} + V_{C'O} e^{-j2\pi/3} \right) \end{aligned} \quad (1.16)$$

The voltage vector of the OW machine fed by common DC-bus dual inverters can be given by

$$\mathbf{V}_s = \frac{2}{3} \left( V_C e^{j0} + V_B e^{j2\pi/3} + V_C e^{-j2\pi/3} \right). \quad (1.17)$$

According to (1.15) - (1.17), the voltage vector of the common DC-bus OW drive can be expressed as the difference between voltage vectors in Inverters I and II.

$$\mathbf{V}_s = \mathbf{V}_{s1} - \mathbf{V}_{s2}. \quad (1.18)$$

The voltage vector equations of an OW machine fed by isolated and common DC-bus DTL-VSIs are the same in (1.7) and (1.18). The reason is that the voltage vector is on the  $\alpha\beta$ -plane, which is independent with the zero sequence axis, so that ZSV cannot be reflected on the voltage vector. ZSV cannot generate ZSC in the isolated DC-bus topology, but can generate ZSC in the common DC-bus topology due to the existence of zero sequence circuit.

ZSV of the OW drive is the difference between CMVs of two two-level inverters, and can be expressed as

$$V_{zsv} = \frac{V_{AO} + V_{BO} + V_{CO}}{3} - \frac{V_{A'O} + V_{B'O} + V_{C'O}}{3}. \quad (1.19)$$

ZSVs of all switching combinations in an OW drive can be calculated as shown in Table 1.3. The ZSV signs of switching combinations are shown in different colours in Fig. 1.32. ‘‘Red’’ represents that the switching combination has a positive ZSV, ‘‘green’’ represents that the ZSV of the switching combination is negative, and the switching combination in ‘‘black’’ colour has null ZSV.

A switching combination can generate a ZSV in zero sequence axis in Table 1.3 and a basic voltage vector in  $\alpha\beta$ -plane in Fig. 1.32, and the zero sequence axis is independent of the  $\alpha\beta$ -plane. As a result, a basic voltage vector in  $\alpha\beta$ -plane is corresponding to a ZSV. For example, switching combination 17' can generate a ZSV of  $V_{dc}/3$  and a basic vector 17', which is

identical to the vector  $\vec{OA}$  in  $\alpha\beta$ -plane. Consequently, the basic vector  $17'$  is with a positive ZSV of  $V_{dc}/3$ .

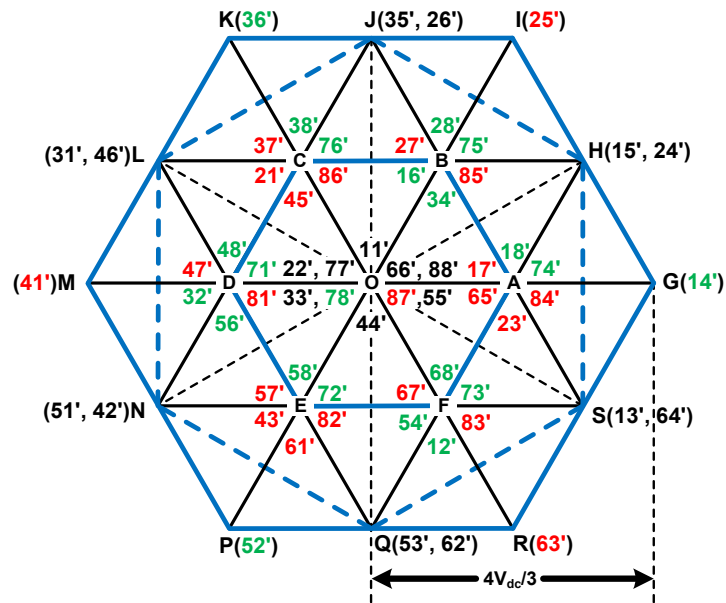


Fig. 1.32 Space vector plane of common DC-bus OW drive.

Table 1.3 ZSVs of Switching Combinations in OW Drive

ZSV	Switching combinations
$V_{dc}$	87'
$2V_{dc}/3$	27', 47', 67', 81', 83', 85'
$V_{dc}/3$	17', 37', 57', 82', 84', 86', 21', 23', 25', 41', 43', 45', 61', 63', 65'
0	13', 15', 35', 31', 51', 53', 24', 26', 42', 46', 62', 64', 11', 22', 33', 44', 55', 66', 77', 88'
$-V_{dc}/3$	71', 73', 75', 28', 48', 68', 12', 32', 52', 14', 34', 54', 16', 36', 56'
$-2V_{dc}/3$	72', 74', 76', 18', 38', 58'
$-V_{dc}$	78'

### 1.5.1 PWM and ZSC control strategies

ZSC is caused by ZSV in an OW-PMSM fed by common DC-bus DTL-VSIs, and should be controlled due to the negative effects, such as extra loss and torque ripples. The ZSC control is not considered in PWM strategies of isolated DC-bus dual inverters, so that these PWM strategies cannot be used in the common DC-bus topology. Fig. 1.33 shows PWM and ZSC control strategies of common DC-bus OW drive.

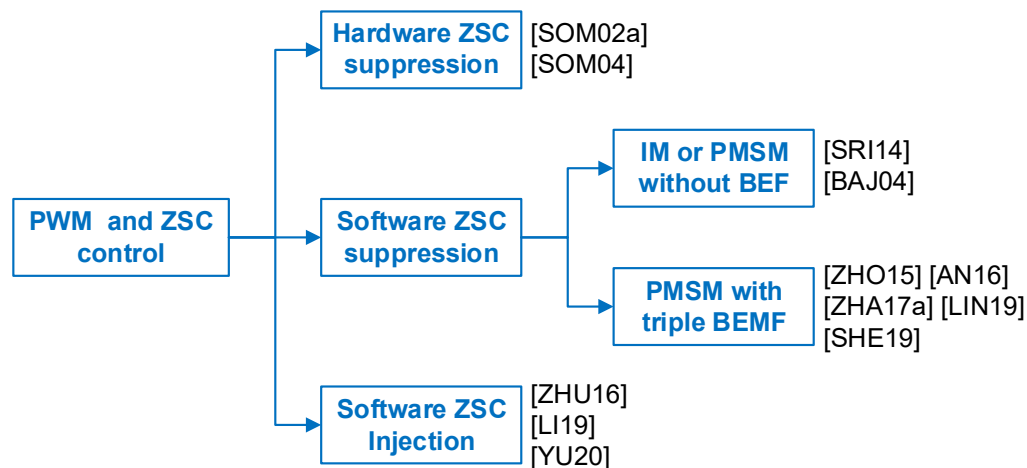


Fig. 1.33 PWM and ZSC control strategies of common DC-bus dual inverters.

Many ZSC control strategies have been proposed for the common DC-bus OW drive. [SOM02a] and [SOM04] proposed hardware solutions to address the ZSC issues and auxiliary switches are needed as shown in Fig. 1.34, but these solutions can increase system complexity and cost. Consequently, software solutions are preferable for the ZSC control.

ZSV of dual inverters can be generated by PWM, inverter nonlinearity, triplen BEMF harmonics, zero sequence coupling voltages [ZHA17a], among which only PWM can generate a controllable ZSV to achieve ZSC control. As a result, a proper designed PWM is needed in software solutions to build a clear relationship between ZSV and modulation parameters.

In an OW induction machine or an OW-PMSM without triplen BEMF harmonics, only the ZSV from PWM is often considered and ZSVs from other sources can be neglected. If only the switching combinations with null ZSV are used to eliminate the ZSV from PWM at any instant, ZSC can be suppressed. In [SRI14], odd or even switching states of each two-level inverter are exclusively used, and all switching combinations of DTL-VSIs have null ZSV, so that the ZSV from PWM can be eliminated. Fig. 1.35 shows PWM waveforms and ZSV of the PWM in [SRI14]. It can be seen that one inverter is clamped while the other inverter is switched, and

ZSV can be always zero.

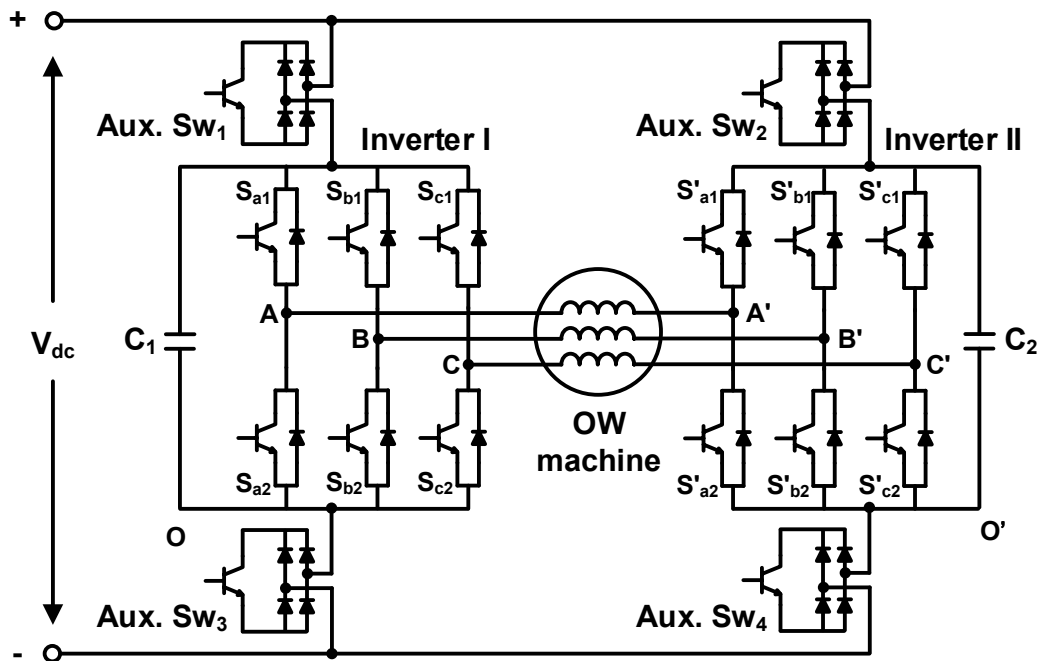
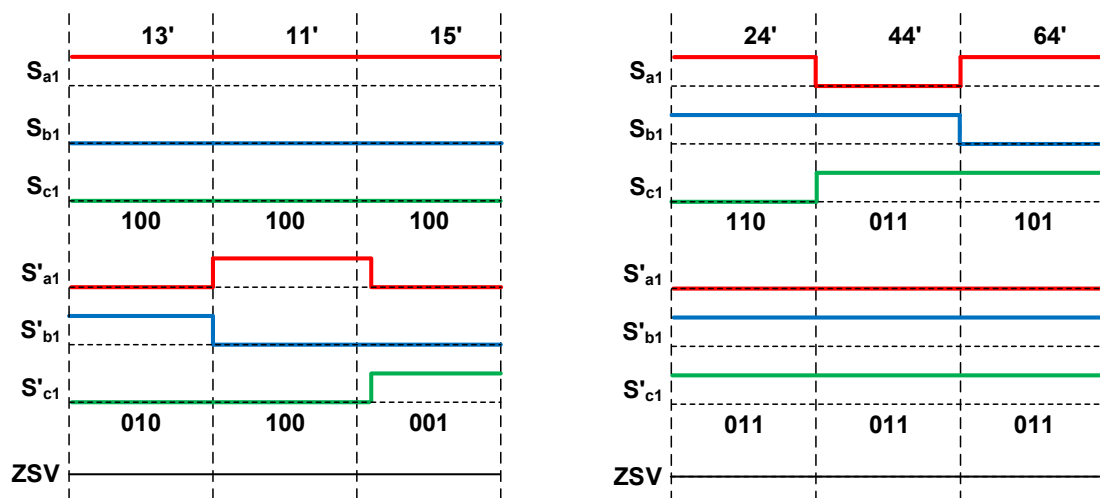


Fig. 1.34 Topology of dual inverters with auxiliary switches.



(a) Odd switching combinations.

(b) Even switching combinations.

Fig. 1.35 PWM waveforms and vectors of PWM strategy in [SIR14].

In [BAI04], all switching combinations with null ZSV can be achieved by the decomposition of the reference voltage vector of the OW drive into two reference vectors of two two-level inverters, and they have the same magnitude and a 120 electrical degree angle with each other. Fig. 1.36 shows the vector decomposition, PWM waveforms and ZSV of the PWM strategy in [BAI04].

The above mentioned PWM strategies can only be used in an OW induction machine or an OW-PMSM without triplen BEMF harmonics, but cannot be used in an OW-PMSM with triplen BEMF harmonics, since large ZSC can be generated by the ZSV from triplen BEMF harmonics. Moreover, ZSVs generated by inverter nonlinearity and coupling voltages in zero sequence are ignored in these above mentioned PWM strategies. Among four sources of ZSV, inverter nonlinearity is the inverter inherent characteristic, while the triplen BEMF harmonics and coupling ZSVs are the inherent characteristics of the OW-PMSM. As a result, ZSVs from the above mentioned three ZSV sources are uncontrollable in the OW drive. However, the ZSV from PWM is controllable in the OW drive. Thus, the basic principle of the ZSC suppression is that the controllable ZSV from PWM counteracts with ZSVs from the other three sources and switching combinations with positive or negative ZSVs in DTL-VSIs should be used to generate the controllable ZSV.

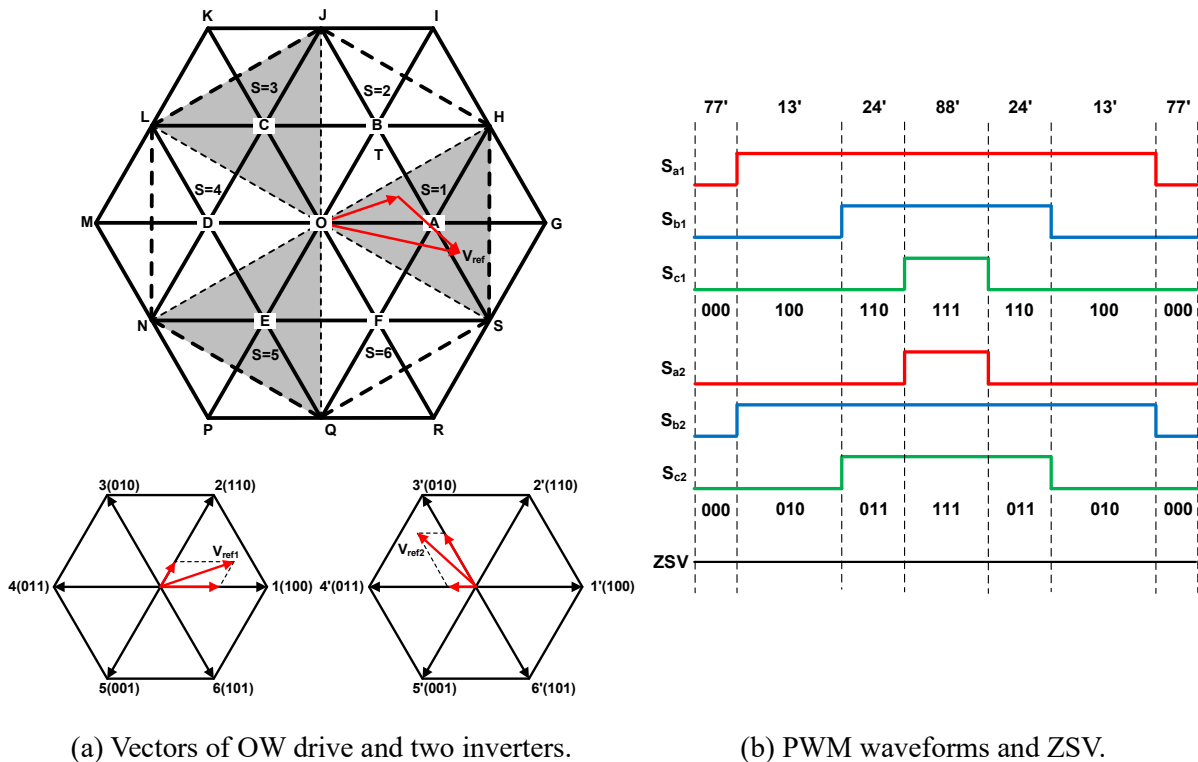


Fig. 1.36 Vector decomposition, PWM waveforms and ZSV of PWM strategy in [BAI04].

[ZHO15] proposed a zero vector redistribution PWM strategy with the ZSC closed-loop control in Fig. 1.37, and a proportional resonant (PR) controller is used to avoid the static error in a proportional integral (PI) controller for ZSC control. The controllable ZSV from PWM can be generated by regulating the durations of zero vector 7(000) and 8(111) in two two-level inverters to suppress ZSC. The reference voltage vector of the OW drive is decomposed into



two voltage vectors for two inverters with the same magnitude and opposite directions as shown in Fig. 1.38 (a). Fig. 1.38 (b) shows the PWM waveforms and ZSV of the PWM strategy in [ZHO15]. With the regulation of zero vector durations in two inverters, a controllable ZSV can be generated by PWM. However, it can be seen that switching combinations with both positive and negative ZSVs are used at the same time, and thus there is a relatively large variation of ZSV, which will cause large ZSC harmonics.

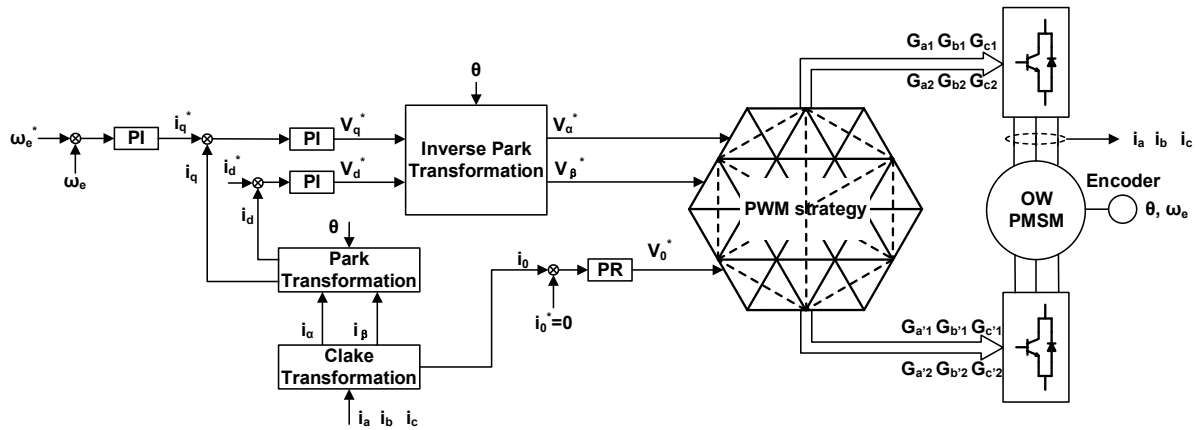
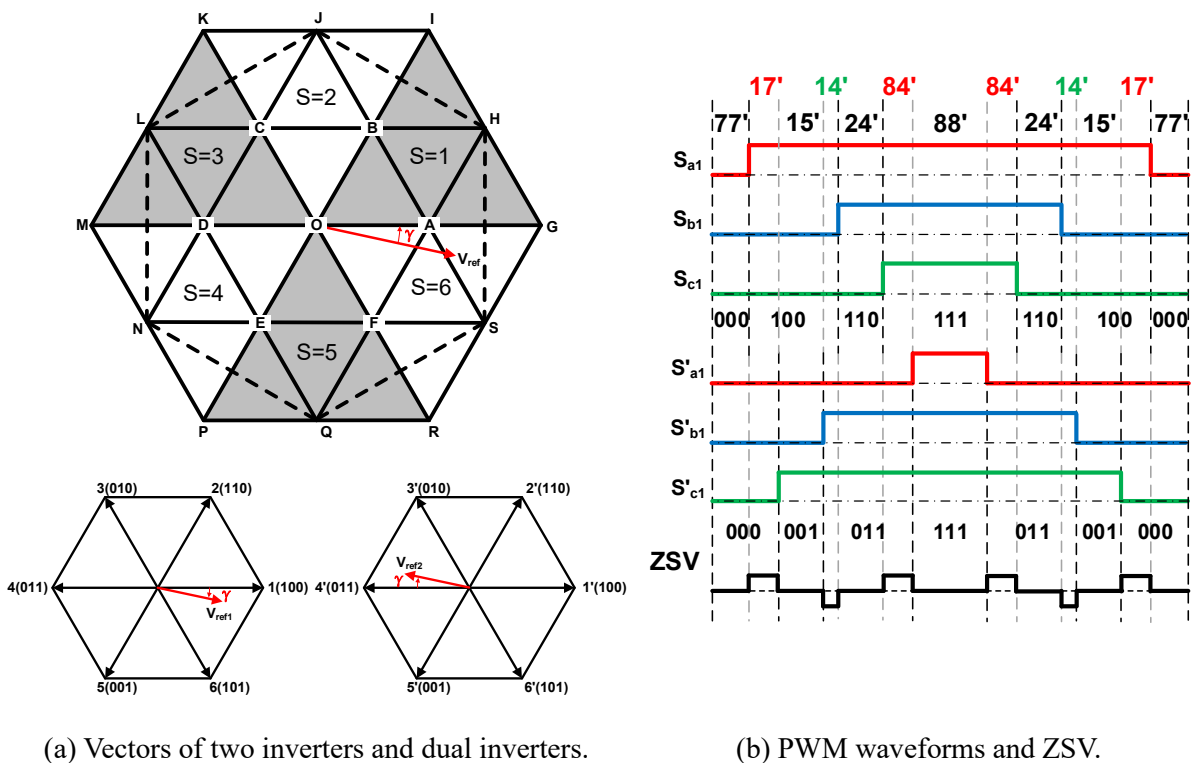


Fig. 1.37 Control diagram of PWM strategy in [ZHO15] with ZSC close loop controller.



(a) Vectors of two inverters and dual inverters.

(b) PWM waveforms and ZSV.

Fig. 1.38 Vector decomposition, PWM waveforms, and ZSV of PWM strategy in [ZHO15].

[AN16] analysed the effect of dead time on the ZSC control, and an SVPWM strategy with the ZSC closed-loop control is proposed. Fig. 1.39 shows the PWM waveforms and ZSV with the PWM strategy in [AN16], one inverter is clamped while the other inverter is switched. The controllable ZSV from PWM can be generated by regulating the duration of zero vectors in the switched inverter. However, this method also uses both positive and negative switching combinations at the same time, which can generate a large variation of ZSV in a PWM cycle as shown in Fig. 1.39 and thus a large ZSC harmonics.

[ZHA17a] use a similar PWM strategy as [BAI04] and the same vector decomposition as shown in Fig. 1.36 (a). To suppress the ZSC in the OW-PMSM drive, a similar zero vector redistribution method as [ZHO15] is used. Fig. 1.40 shows PWM waveforms and ZSV of the PWM strategy in [ZHA17a] with positive and negative reference ZSV  $V_o^*$ . It can be seen that only positive ZSV switching combinations are used with positive  $V_o^*$ , and only negative ZSV switching combinations are used with negative  $V_o^*$ . As a result, ZSC harmonics can be reduced compared with these in [ZHO15] and [AN16].

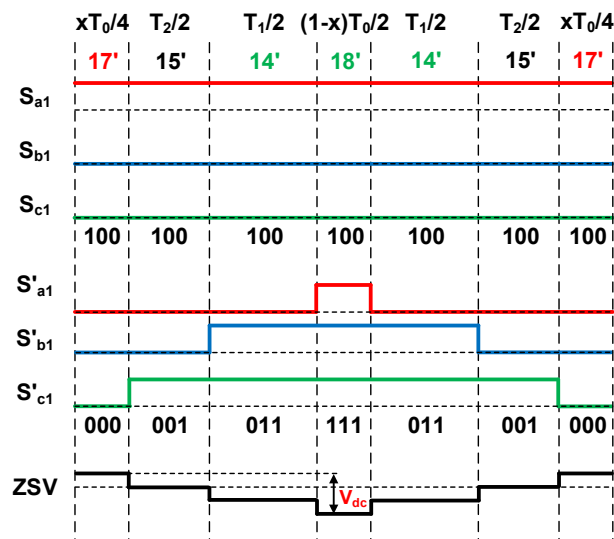


Fig. 1.39 PWM waveforms and vectors of PWM strategy in [AN16].

Different PWM methods are used under positive and negative ZSCs in [LIN19], and the selection of switching combinations are shown in Fig. 1.41. A hysteresis controller is applied for ZSC suppression, which can cause large current harmonics. Moreover, the modulation region will be much less than the middle hexagon.

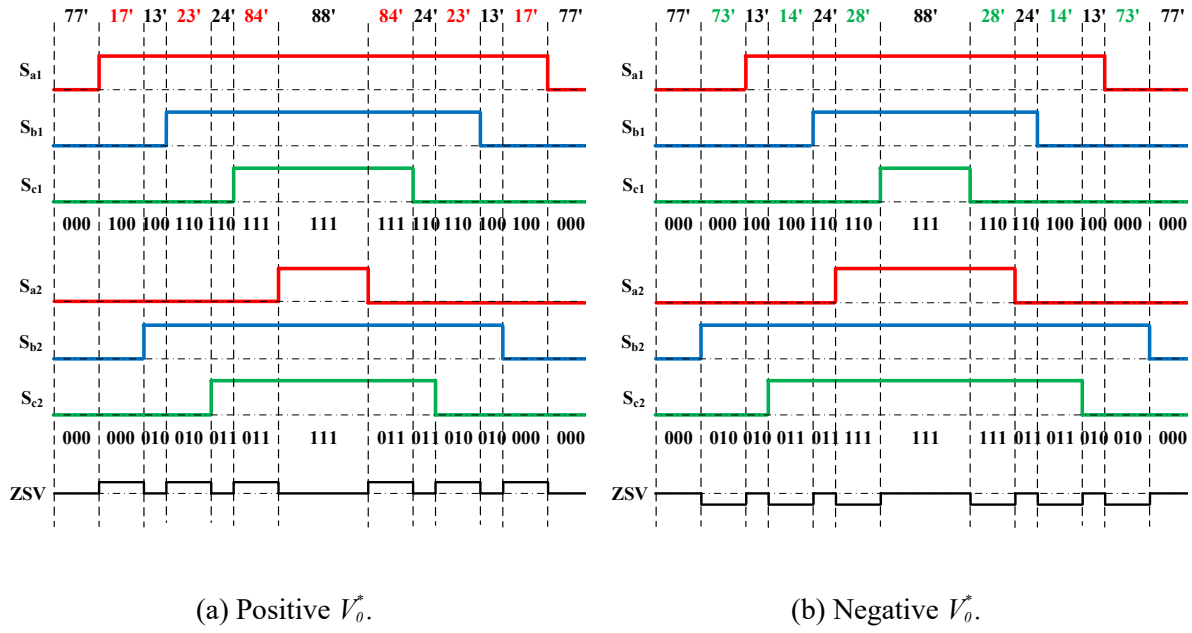


Fig. 1.40 PWM waveforms and vectors of PWM strategy in [ZHA17a].

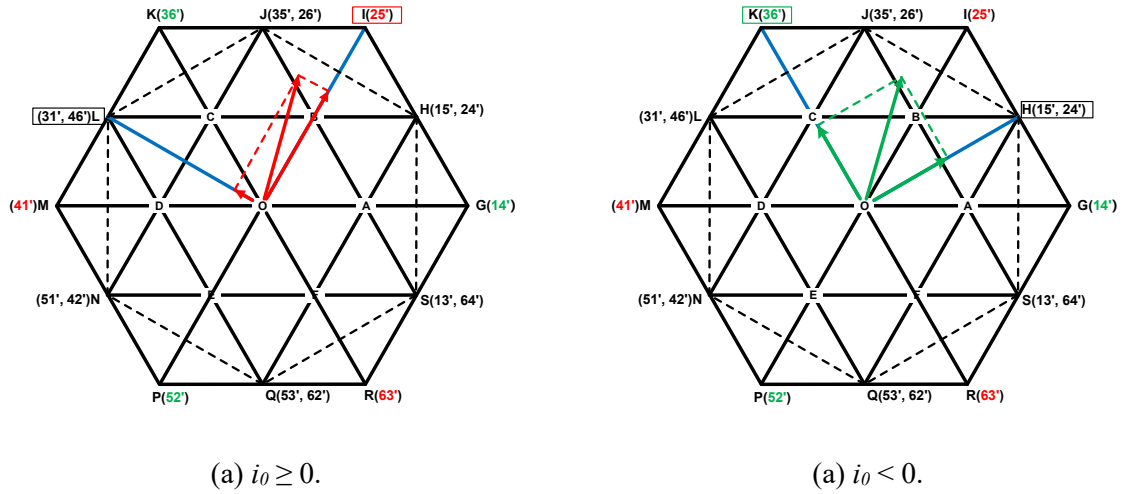


Fig. 1.41 Selection of switching combinations of the PWM strategy in [LIN19].

[SHE19] proposed a SPWM with a phase shift to achieve an asymmetric vector sequence as shown in Fig. 1.42. PWM induced current harmonics can be reduced in high modulation regions, and thus, machine vibration and acoustic noise can be suppressed. A similar PWM waveform regulation method as [ZHO15] and [ZHA17a] is used for ZSC suppression. However, the asymmetric vector sequence can cause low-order phase current harmonics.

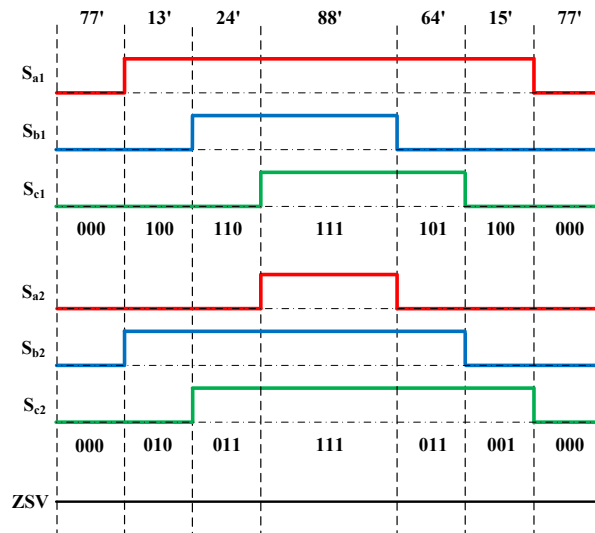


Fig. 1.42 PWM waveforms and vectors of PWM strategy in [SHE19].

In an OW three-phase machine drive, common DC-bus dual inverters can be regarded as three H-bridges inverters, and each phase is controlled by a H-bridge as shown in Fig. 1.43. As a result, three phase currents can be controlled independently, and DC-biased sinusoidal currents can be used in the integrated field and armature current control for some specific machine drive, such as variable flux reluctance machine [ZHU16], vernier machine [LI19], switched reluctance machine [YU20]. Fig. 1.44 shows the DC-biased sinusoidal phase current, which is achieved by the ZSC injection to phase currents. Different from the above mentioned ZSC suppression in an OW drive, where the reference ZSC is set to zero, the reference ZSC is set to a DC-biased value of  $I_{dc}$  in the DC-biased current control.

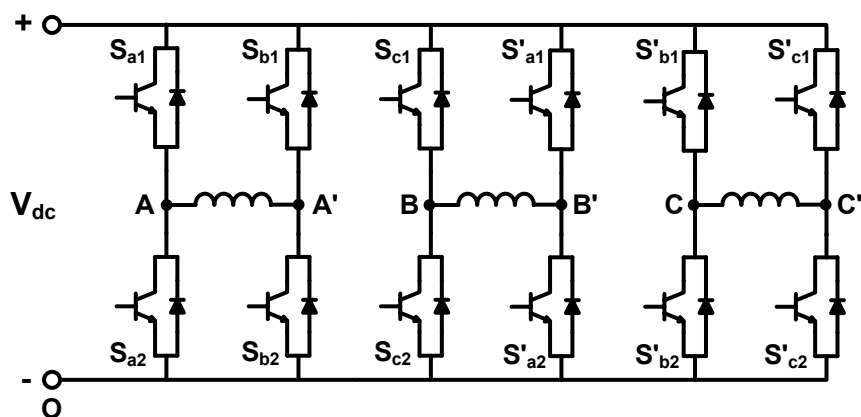


Fig. 1.43 Three H-bridges in the common DC-bus dual inverters.

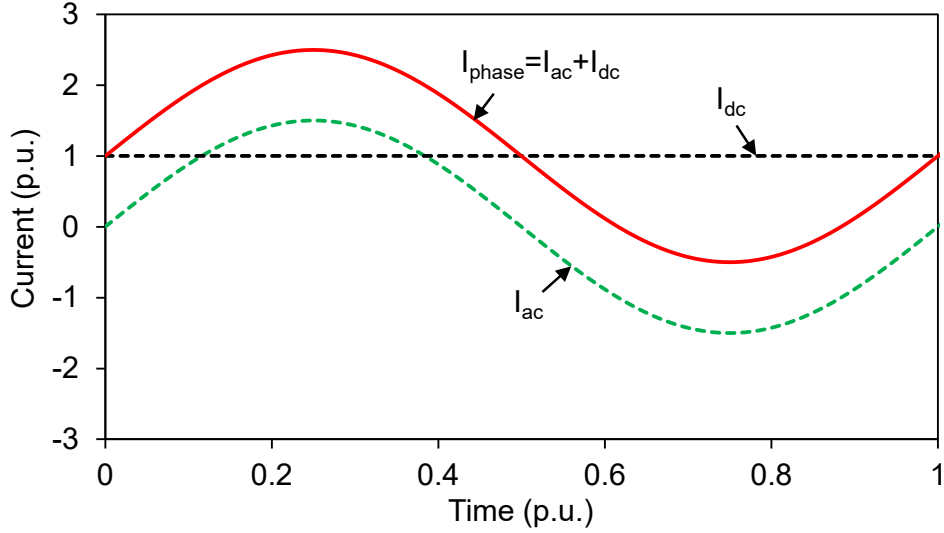


Fig. 1.44 Phase current of DC-biased current control.

### 1.5.2 CMV control

CMV variation can cause shaft voltage variation, and thus generate bearing current, which may cause the failure of bearings. CMV of a common DC-bus OW drive can be expressed as the average of CMVs in two two-level inverters.

$$V_{CMV} = \frac{V_{CMV1} + V_{CMV2}}{2} = \frac{V_{AO} + V_{BO} + V_{CO} + V_{A'O} + V_{B'O} + V_{C'O}}{6}. \quad (1.20)$$

Different from the CMV control in the isolated DC-bus OW drive, the CMV control in the common DC-bus OW drive should also consider the ZSC control at the same time.

For the SVPWM strategy of common DC-bus dual inverters in [ZHA17b], there is a large variation of CMV regardless of positive or negative reference ZSV  $V_o^*$  as shown in Fig. 1.45. To reduce the negative effect of CMV, the variation of CMV should be suppressed. In an OW machine fed by dual inverters, the variation of CMV can be eliminated utilizing redundant voltage vectors.

In [BAR15], only odd switching states 1(100), 3(010), 5(001) or even switching states 2(110), 4(011), 6(101) are used in each two-level inverter to eliminate the variation of CMV. If only odd switching states are applied, the switching combinations of the OW drive are 11', 13', 15', 31', 33', 35', 51', 53, 55', which have the same CMV, i.e.  $V_{dc}/3$ . On the other hand, if only even switching states are applied, the switching combinations in the OW drive are 22', 24', 26', 42', 44', 46', 62', 64, 66', whose CMV are all  $2V_{dc}/3$ . PWM waveforms of this PWM

strategy in sector 1 are shown in Fig. 1.46. The odd switching combinations are exclusively used in Fig. 1.46 (a). It can be seen that Inverter I is clamped, and the CMV is kept on  $V_{dc}/3$ . The even switching combinations are exclusively used in Fig. 1.46 (b). It can be seen that Inverter II is clamped, and the CMV is a constant value of  $2V_{dc}/3$ .

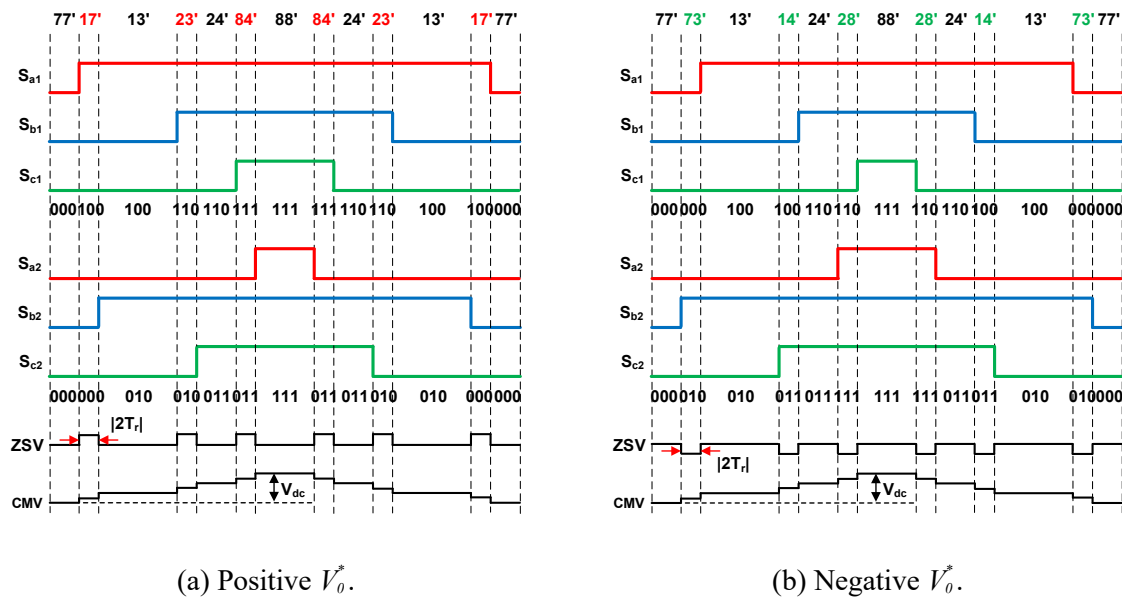


Fig. 1.45 PWM waveforms, switching combinations, ZSV, and CMV of the conventional SVPWM with ZSC control.

ZSV caused by the PWM in [BAR15] is always zero as shown in Fig. 1.46, so that this method can only be used in an OW induction machine or an OW-PMSM machine without triplen BEMF harmonics to eliminate CMV variation and suppress ZSC. However, some other sources, such as the triplen BEMF harmonics in PMSM, inverter nonlinearity, and zero sequence component of coupling voltages, can also generate ZSVs. As a result, this PWM strategy cannot generate a controllable ZSV to counteract with ZSVs caused by other sources, so that ZSC is uncontrollable, and large ZSC is generated in an OW-PMSM drive with triplen BEMF harmonics.

A POD-PWM strategy is proposed in [HU21] for a common DC-bus OW-PMSM drive to eliminate CMV variation and suppress ZSC simultaneously. There is 180-degree phase difference between two carrier signals of Inverters I and II, and two legs of each H-bridge have completely opposite signals as shown in Fig. 1.47. Consequently, according to (1.20), the CMV of the OW drive can always be kept on the constant value  $V_{dc}/2$ . Fig. 1.47 shows the switching combinations of the PWM strategy in [HU21]. According to Table 1.3, all switching

combinations have the same CMV of  $V_{dc}/2$ . On the other hand, the control of ZSC is necessary in an OW-PMSM fed by common DC-bus dual inverters. The PWM strategy in [HU21] can generate a controllable ZSV by regulating the durations of two zero vectors  $78'$  and  $87'$ , whose ZSVs are  $-V_{dc}$  and  $V_{dc}$ , respectively. With the controllable ZSV from PWM, ZSVs from other sources can be counteracted and thus the ZSC can be suppressed. However, this PWM strategy uses both positive and negative ZSV switching combinations at the same time for the ZSC control, and cause a large variation of ZSV from  $-V_{dc}$  to  $V_{dc}$  as shown in Fig. 1.47, so that large current harmonics in zero sequence are induced.

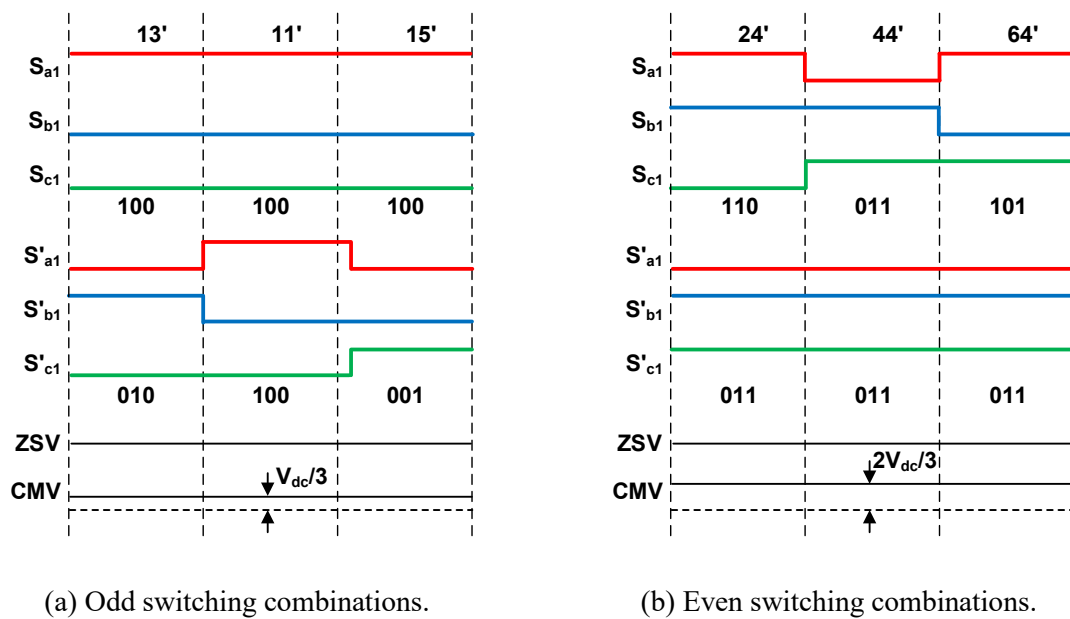


Fig. 1.46 PWM waveforms, ZSV, and CMV of PWM strategy in [BAR15].

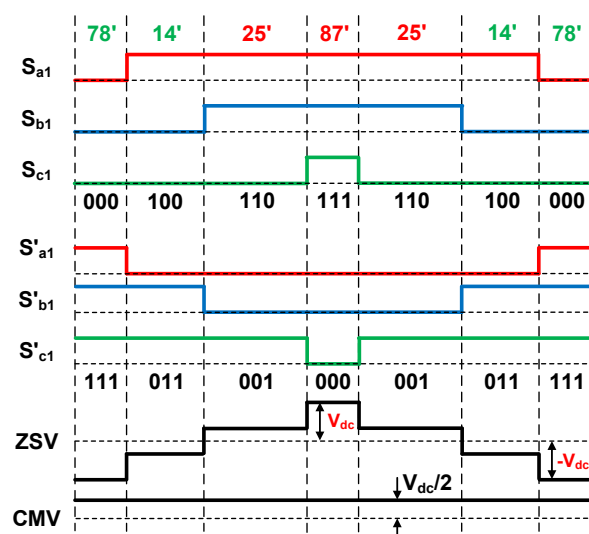


Fig. 1.47 PWM waveforms, ZSV, and CMV of PWM strategy in [HU21].

### 1.5.3 Flux weakening

The speed range of an OW-PMSM is limited due to the limited DC-bus voltage and the increase of BEMF with the speed rise. To extend the operation range, the flux weakening control should be considered. A feedback flux weakening strategy is applied to the OW-PMSM drive in [SAN13] as shown in Fig. 1.48. Three phase currents can be controlled independently in an OW machine fed by common DC-bus dual inverters, so that the control strategy should handle not only  $dq$ -axis currents but also ZSC.  $D$ -axis flux weakening current can be expressed as  $i_d^* = \lambda \int (V_{dc} - \sqrt{(V_d^*)^2 + (V_q^*)^2}) dt$ , where  $V_d^*$  and  $V_q^*$  are the outputs of  $dq$ -axis current PI controllers,  $\lambda$  is the integral coefficient, and  $V_{dc}$  is the DC-bus voltage. The control strategy in [SAN13] can maintain the close-loop control of ZSC and avoid the voltage saturation of dual inverters. However, the OW-PMSM can only operate in the linear modulation region.

In [SAN14], a flux weakening strategy for the OW-PMSM drive is proposed considering magnitudes and phase angles of voltage harmonic components as shown in Fig. 1.49, which can increase the voltage utilization compared with the method in [SAN13]. A lookup table is set to acquire the magnitudes and phase angles of voltage harmonic components. However, this method strongly depends on parameters of the OW-PMSM. Moreover, only the linear modulation region is considered in [SAN14], and ZSC is out of control in the over modulation region.

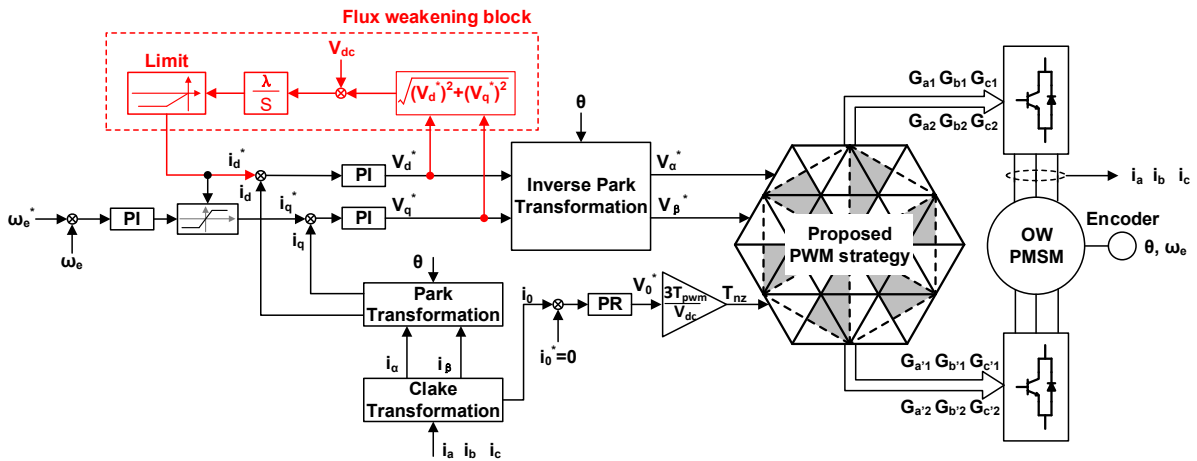


Fig. 1.48 Control diagram of OW-PMSM in [SAN13].



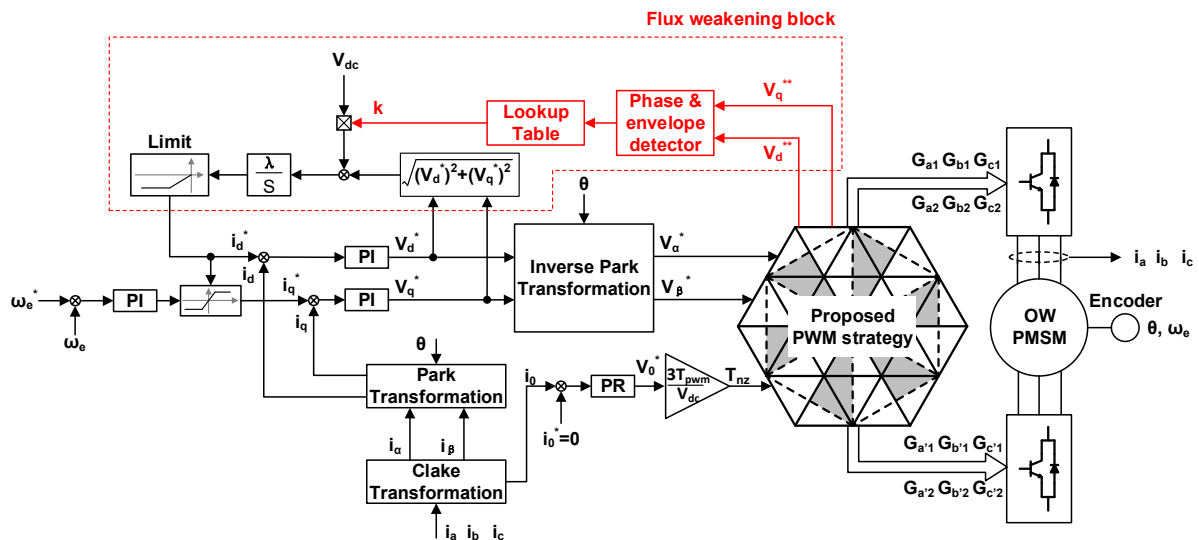


Fig. 1.49 Control diagram of OW-PMSM in [SAN14].

### 1.5.4 Sensorless strategy based on ZSV

Accurate rotor position is needed in the high-performance PMSM drive, and a position sensor is often used. However, in some special applications, the position sensor can cause some issues, such as reliability and higher cost, and the sensorless control is preferable. Generally, sensorless methods can be categorized into BEMF-based and rotor saliency-based methods, which are suitable for high and low speed operations, respectively. The third BEMF harmonic-based method is a special kind of BEMF-based method, and rotor position information is extracted from the third BEMF harmonic. A virtual neutral point needs to be constructed for detecting the third BEMF harmonic in the traditional PMSM, which will increase the cost and complexity of system. However, ZSC can flow through the OW-PMSM fed by common DC-bus dual inverters, and the third BEMF harmonic can be easily detected. Fig. 1.50 shows sensorless methods for OW-PMSM fed by common DC-bus dual inverters.

[ZHA16] proposed a zero sequence model-based sensorless method for an OW-PMSM fed by common DC-bus dual inverters, and the third BEMF harmonic can be reconstructed by the zero sequence model and ZSC. However, this method can cause large ZSC and torque ripples. [NIA19a] also utilizes ZSC to detect the third BEMF harmonic, and a torque control in  $q$ -axis is used to suppress torque ripples, but ZSC still cannot be eliminated, which will cause extra loss. [ZHA17b] proposed a zero sequence controller-based sensorless method. ZSC can be suppressed by the zero sequence controller in [ZHA17b], and the output of the zero sequence controller is used for the third BEMF harmonic extraction and the rotor position estimation.

The method in [ZHA17b] has the advantage of no requirement for machine parameters, such as  $dq0$ -axis inductances, the winding resistance, and PM flux linkage. [LIU21] proposed a zero sequence model-based sensorless method with enhanced robustness, and a general-integral state observer is used for the ZSC control and the third BEMF harmonic estimation. Figs. 1.51 (a) and (b) show the control diagrams of an OW-PMSM fed by common DC-bus dual inverters with two sensorless methods, i.e., zero sequence model-based and zero sequence controller-based, respectively.

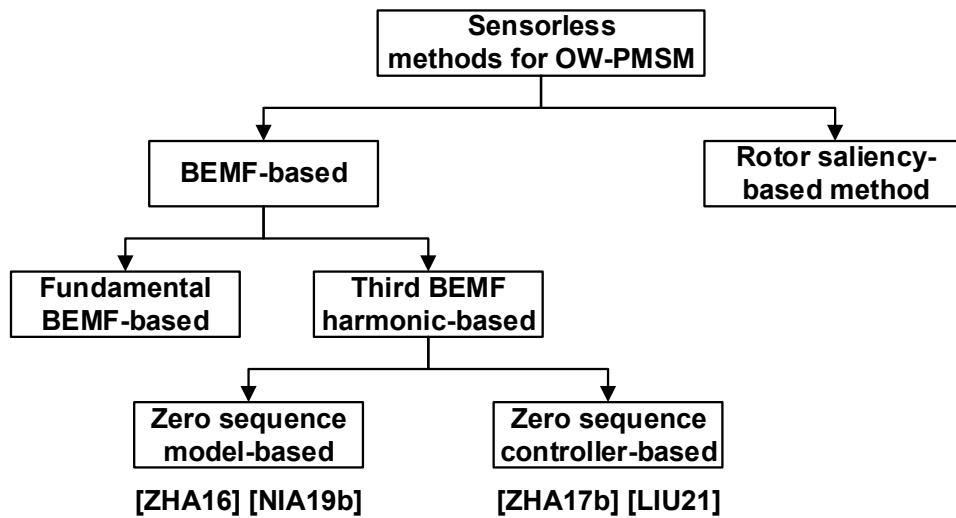
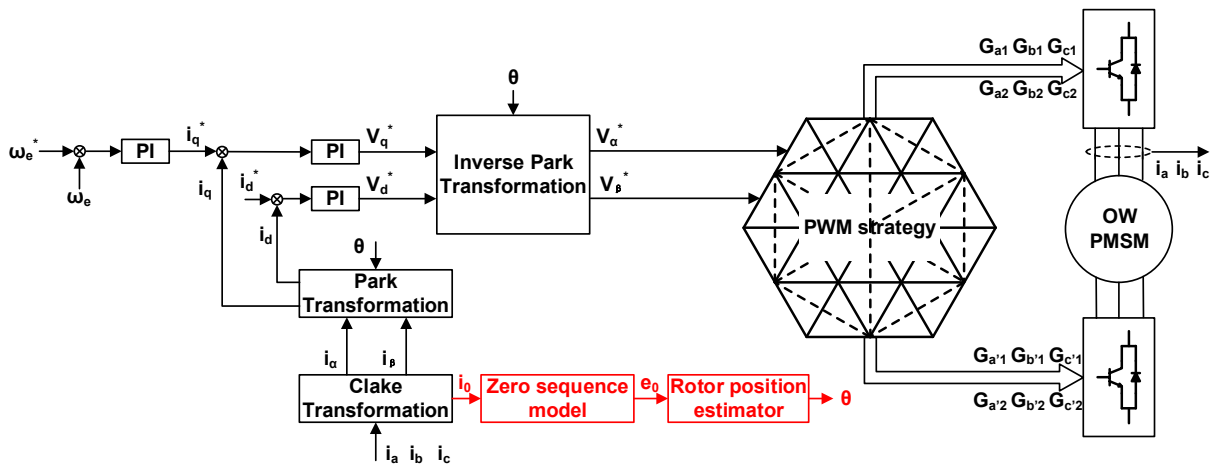
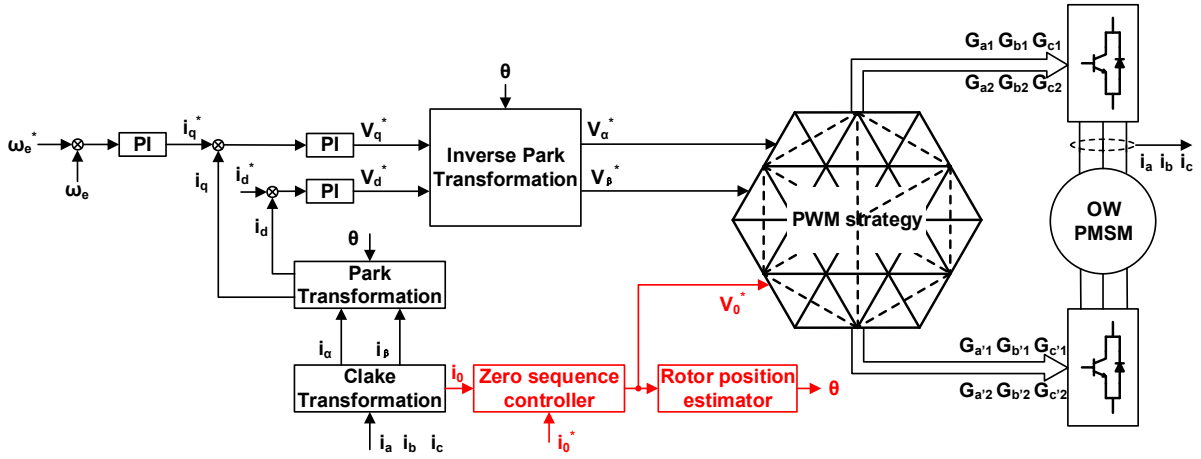


Fig. 1.50 Sensorless methods for OW-PMSM fed by common DC-bus dual inverters.



(a) Zero sequence model-based sensorless.



(b) Zero sequence controller-based sensorless.

Fig. 1.51 Control diagram of OW-PMSM fed by common DC-bus dual inverters with sensorless control.

### 1.5.5 Fault tolerant control

For an OW-PMSM fed by common DC-bus DTL-VSIs, each phase can be regarded to be controlled independently by an H-bridge inverter. When an H-bridge inverter or a phase winding has an open- or short-circuit fault in an OW-PMSM fed by common DC-bus DTL-VSIs, the H-bridge with the fault phase can be cut off and no current will flow into this phase, and the other two H-bridges can still be used to drive the machine [AN14]. For example, the winding or the H-bridge inverter in phase A has a fault, and the H-bridge with phase A winding can be cut off from control system as shown in Fig. 1.52. There are 16 switching combinations for the two H-bridge configurations when phase A is fault, and the corresponding vectors are shown in Table 1.4. Among these vectors,  $\mathbf{V}_0$  is the zero vector, while effective vectors  $\mathbf{V}_1$ - $\mathbf{V}_6$  have the same magnitude of  $V_{dc}$ , and  $\mathbf{V}_7$  and  $\mathbf{V}_8$  have the magnitude of  $\sqrt{3}V_{dc}$ .  $\mathbf{V}_0$  -  $\mathbf{V}_6$  can generate the space vector plane for the two H-bridge configurations as shown in Fig. 1.53, while  $\mathbf{V}_7$  and  $\mathbf{V}_8$  are not used due to the different magnitude. The reference voltage vector can be synthesized by two adjacent effective vectors and a zero vector in the space vector plane according to SVPWM principle. Fig. 1.54 shows three phase currents and ZSC in the normal operation with three H-bridge configurations and the fault tolerant operation with two H-bridge configurations.

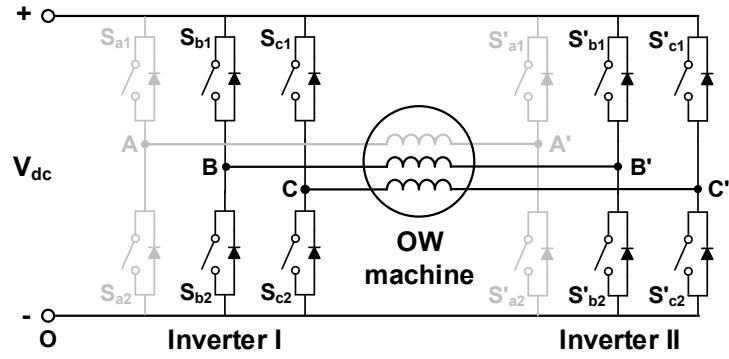


Fig. 1.52 Two H-bridge configurations for OW machine under fault tolerant control.

Table 1.4 Switching Combinations of Two H-bridge Configurations

Vectors	$V_0$	$V_1$	$V_2$	$V_3$	$V_4$	$V_5$	$V_6$	$V_7$	$V_8$
$S_{b1}S'_{b1}S_{c1}S'_{c1}$	0000,0011, 1100,1111	0101	0001, 1101	1000, 1011	1010	0010, 1110	0100, 0111	1001	0110

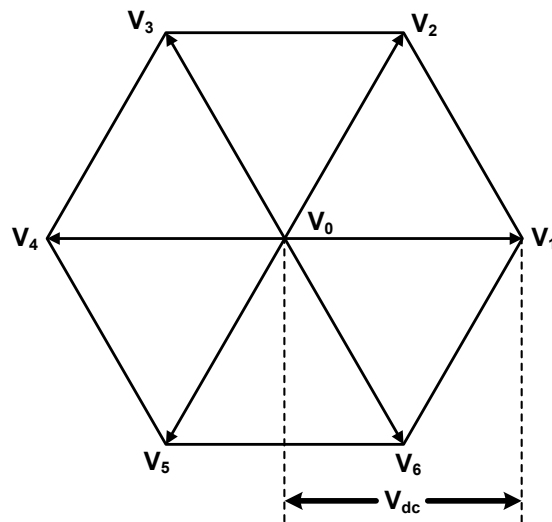
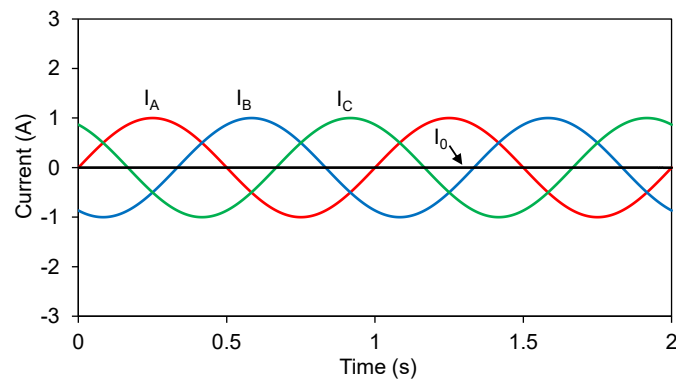
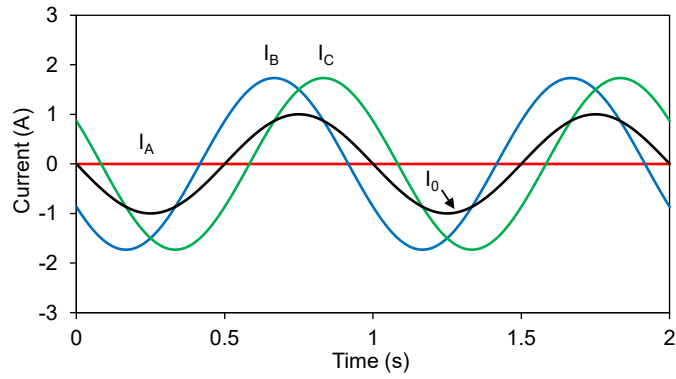


Fig. 1.53 Voltage vector in the space vector plane.



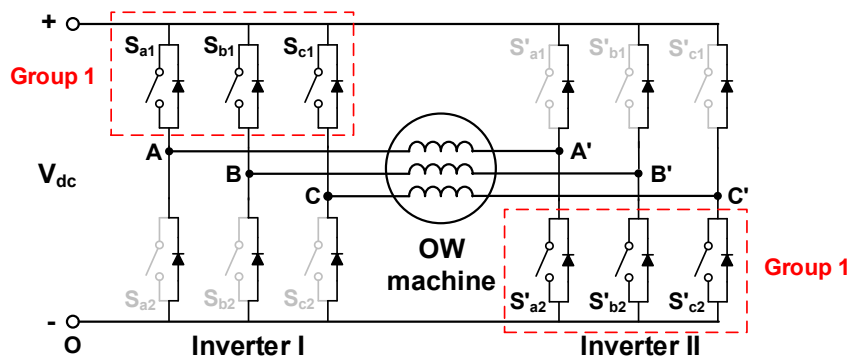
(a) Normal operation.



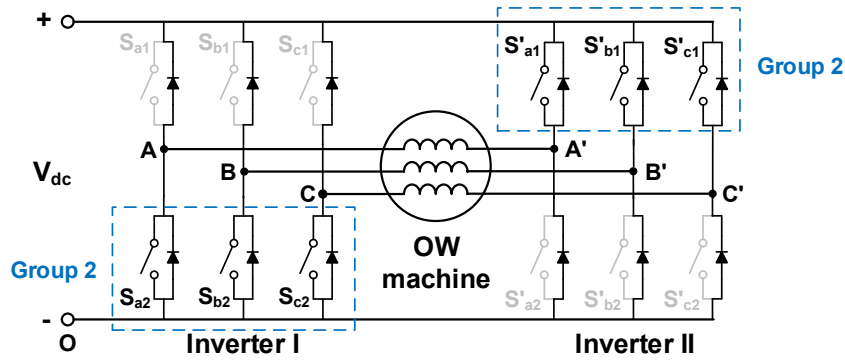
(b) Fault tolerant operation.

Fig. 1.54 Three phase currents and ZSC in [AN14].

For the open-circuit fault of switches/diodes, the dual inverters can be reconfigured as shown in Fig. 1.55 [RES12]. Three lower switches in Inverter I are cut off, while three upper switches in Inverter II are cut off as shown in Fig. 1.55 (a), and only six switches of group 1 are used. Consequently, the utilizing of switches can be reduced by half and the control of the OW machine can still be maintained, but this configuration can reduce the modulation region and induce ZSC. Three phase currents and ZSC are shown in Fig. 1.56 (a), and three phase currents are always positive. On the contrast, only six switches of group 2 are used in Fig. 1.55 (b), if switches/diodes in group 1 have an open-circuit fault. Three phase currents and ZSC are shown in Fig. 1.56 (b), and three phase currents are always negative. [YU19] use the similar method for the fault tolerant control of an OW vernier reluctance machine, and the DC-biased ZSC can be used for field excitation.

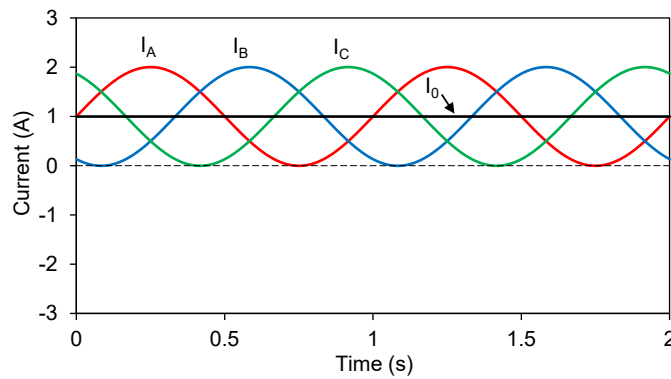


(a) Group 1.

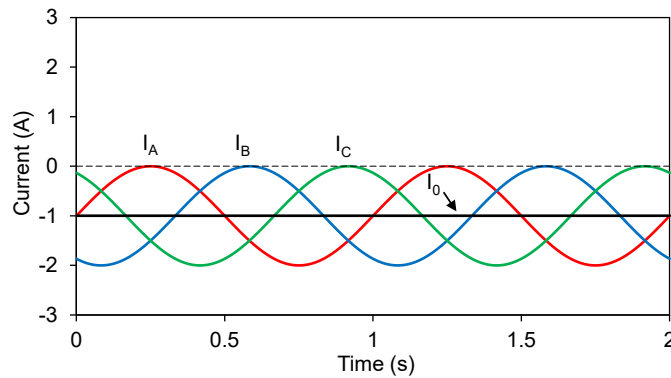


(b) Group 2.

Fig. 1.55 Dual inverters with six switches in [RES12].



(a) Positive three phase currents.



(b) Negative three phase currents.

Fig. 1.56 Three phase currents and ZSC in [RES12].

[ZHU19] proposed a fault tolerant control for an OW-PMSM based on ZSC injection, when freewheel diodes have an open circuit fault in either inverter. For example,  $S_{a1}$  or  $S'_{a2}$  have an open-circuit diode fault as shown in Fig. 1.57, so that there is no flowing path for negative phase A current, but positive phase A current can still flow. As a result, a ZSC, which equals zero when  $\alpha$ -axis current is positive and is  $(I_b + I_c)/3$  when  $\alpha$ -axis current is negative, is injected

to three phase currents as shown in Fig. 1.58. Table 1.5 gives a comparison between three fault tolerant strategies for an OW machine fed by common DC-bus dual inverters. The method in [AN14] can handle both open- and short-circuit fault of switches/diodes and windings, while the method in [ZHU19] has the smallest root mean square (RMS) value of ZSC.

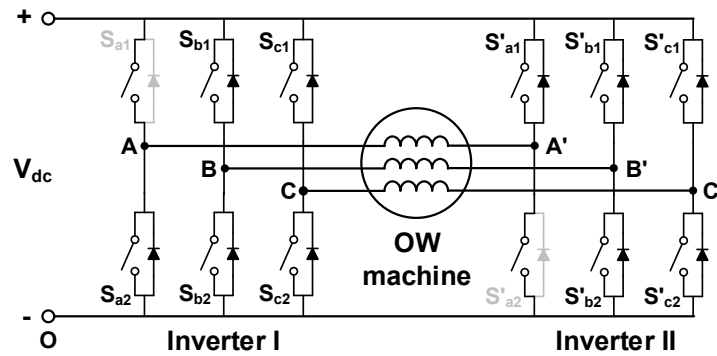


Fig. 1.57 OW machine fed by common DC-bus dual inverters with open circuit diode fault of  $S_{a1}$  and  $S'_{a2}$ .

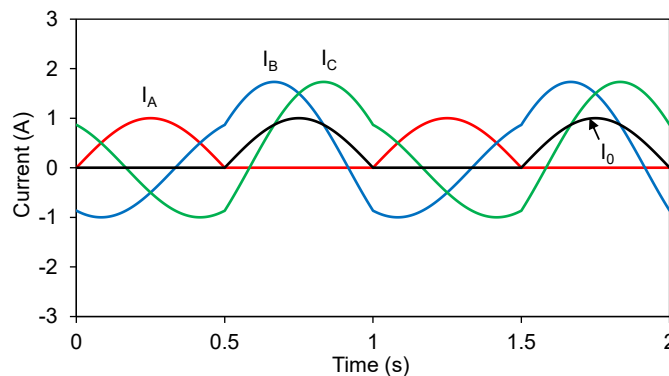


Fig. 1.58 Three phase currents and ZSC with ZSC injection in [ZHU19].

Table 1.5 Comparison of Fault Tolerant Control for OW Machine Fed by Common DC-bus Dual Inverters

Fault tolerant methods	Fault type	RMS value of ZSC
Method in [AN14]	Switch/diode short/open-circuit Winding short/open-circuit	middle
Method in [RES12] [YU19]	Switch/diode open-circuit	large
Method in [ZHU19]	Diode open-circuit	small

## 1.6 Floating Capacitor Dual Inverters

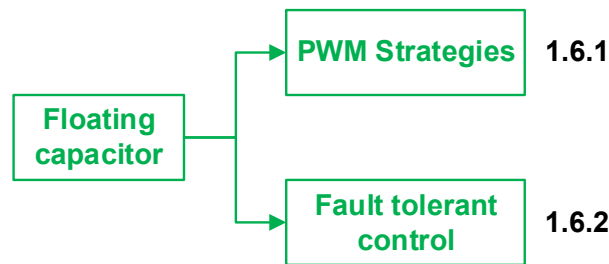


Fig. 1.59 PWM of floating capacitor dual inverters.

For the floating capacitor dual inverters in Fig. 1.2 (c), one inverter is fed by a voltage source, while the other inverter is fed by a floating capacitor, which is not powered by any voltage source. Similar with the isolated DC-bus topology, the floating capacitor topology can also block the flowing path of ZSC, which exists in the common DC-bus topology. Compared with isolated and common DC-bus topologies, the floating capacitor topology shows relatively limited fault tolerant capability [MAJ21], and only faults of switches/diodes on the inverter fed by the floating capacitor can be resolved. The floating capacitor topology can be regarded as a special isolated DC-bus topology, and one of two voltage sources is replaced by a floating capacitor, so that they have similar voltage models.

In an OW machine fed by floating capacitor dual inverters, the voltage ratio between the voltage source and the floating capacitor can be controlled, and the ratio can affect the voltage utilization and output voltage quality of the OW machine. With a suitable DC-bus voltage ratio, the levels of output voltages can be increased for the performance improvement [PER13] [MAJ21] [CHO16]. For example, with a DC-bus voltage ratio of 2:1, three-level output voltages can be generated. Consequently, for floating capacitor OW drive, the main challenge is to control the floating capacitor voltage to a desired value.

### 1.6.1 PWM strategies and floating capacitor voltage control

Switching combinations in floating capacitor dual inverters can affect the charging/discharging state of the floating capacitor, so that a proper selection of switching combinations can regulate the floating capacitor voltage. In [HUA19a], a capacitor voltage control method is proposed for floating capacitor dual inverters with a 2:1 DC-bus voltage ratio, and Inverter II is fed by the floating capacitor. Voltage vectors are categorized into three types as shown in Fig. 1.60 according to the charging/discharging state of the floating capacitor. Type I vectors can achieve



both charging/discharging of the floating capacitor, and type II vectors have neither charging/discharging state, and type III vector can only discharge the floating capacitor. Types I and II vectors are all within the Inverter I hexagon in Fig. 1.60, while type III vectors are all outside of the Inverter I hexagon.

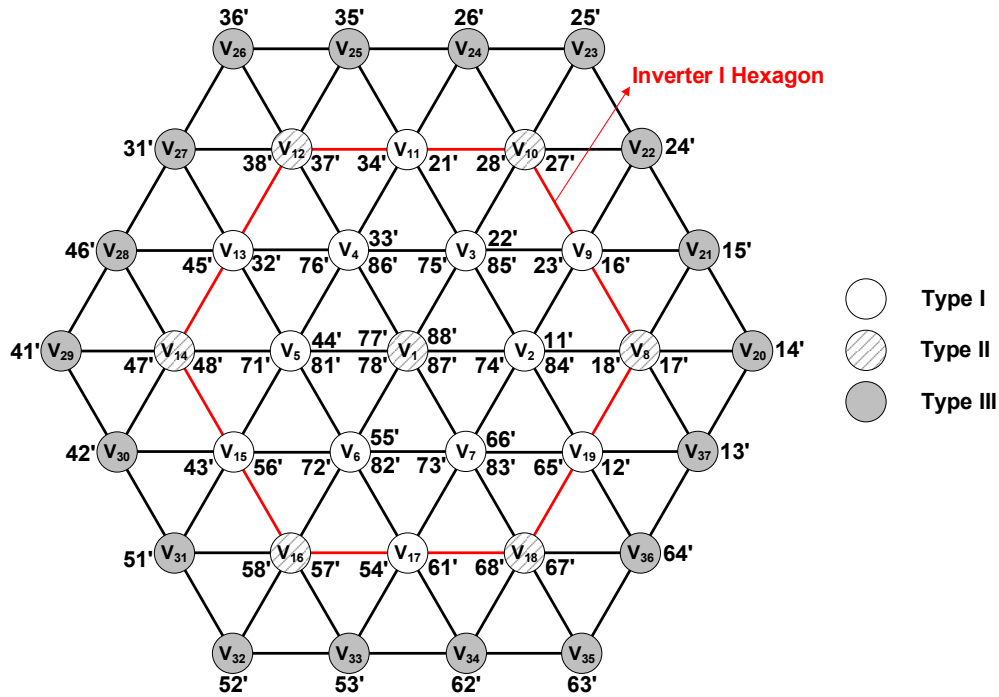


Fig. 1.60 Types of voltage vectors for floating capacitor dual inverters with DC-bus voltage ratio 2:1.

Fig. 1.61 shows the sector 1 of the space vector plane, and a sector is divided into 9 regions. To maintain the capacitor voltage to a desired value, type I vectors must be used, as only type I vectors can charge the floating capacitor. For the regions 1-4 in Fig. 1.61, type I vectors can be used while type III vectors do not need to be used, so that the voltage of the floating capacitor can be fully controlled. For the regions 5-9, type III vectors need to be used, so that the voltage of the floating capacitor may be out of control. Especially for the regions 5 and 9, only types II and III vectors can be used, so that the discharge of the floating capacitor will occur and the voltage of the floating capacitor will be reduced. For regions 6-8, all three types of vectors should be used, and the voltage of the floating capacitor can be controlled when the duration of the type I vector larger than the duration of the type III vector. Consequently, the floating capacitor voltage can only be controlled in parts of regions 6-8. With the capacitor voltage control method in [HUA19a], the voltage utilization can be increased by approximately 10% compared with a two-level inverter. However, the voltage utilization of floating capacitor dual inverters is still much lower than that of isolated and common DC-bus dual inverters.

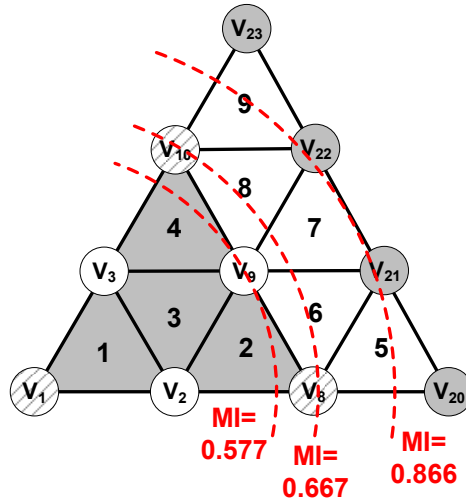
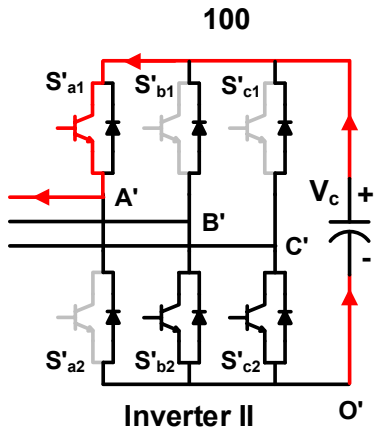
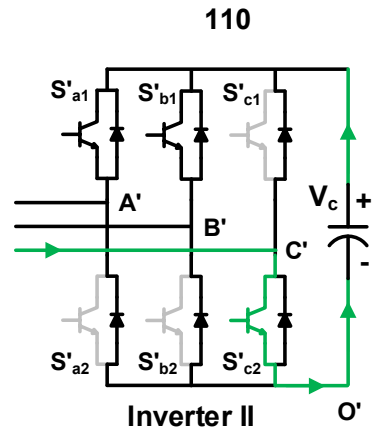


Fig. 1.61 Space vector plane of sector 1.

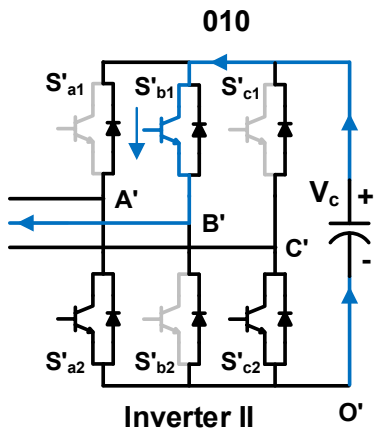
The charging/discharging state of vectors in [HUA19a] is acquired under the assumption that the signs of three-phase voltages are the same as these of three-phase currents in dual inverters. However, this may not be accurate in actual operation conditions of an OW machine drive. The control of the capacitor voltage in the floating capacitor dual inverters is improved in [HUA21], and the directions of currents are considered. Assuming Inverter I is fed by a voltage source, while Inverter II is fed by a floating capacitor as shown in Fig. 1.2 (c). The switching state of Inverter II and current directions can result in different charging/discharging state of the floating capacitor. Due to the existence of diodes in an inverter, there is always a flowing path for charging the capacitor regardless the switching state of Inverter II and current directions. However, the discharging of the capacitor needs certain switching states and current directions, and occurs only when there is a discharging path. Figs.1.62 (a)-(f) show the discharging path for six effective vectors in Inverter II. For example, in Fig. 1.62 (a), the switching state is 100 in Inverter II, and the discharge of capacitor only occurs when phase A current is negative. On the contrast, the charge of capacitor occurs when phase A current is positive. Figs.1.62 (g) and (h) show the switching states of 000 and 111, respectively, in Inverter II, and only the three phase current directions with (+--) are shown in the figures. However, three phase currents with any direction can flow through Inverter II and do not cause the charging/discharging of the capacitor. Table 1.6 shows the relationship between switching states, current directions and charging/discharging states of the floating capacitor. In [HUA21], the appropriate switching combinations are chosen according to Table 1.6 to charge or discharge the floating capacitor, and the capacitor voltage can be controlled at a desired value. Compared with the method in [HUA19a], the method in [HUA21] has a more accurate control of capacitor voltage by considering current directions.



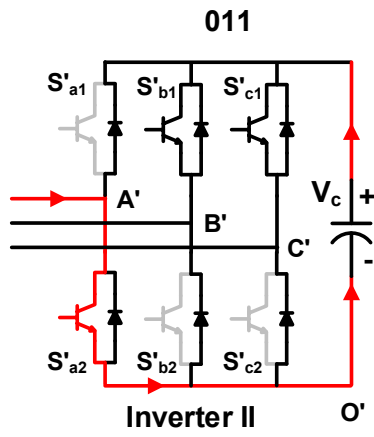
(a) 1' (100).



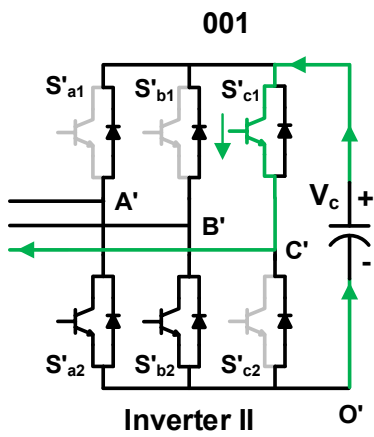
(b) 2' (110).



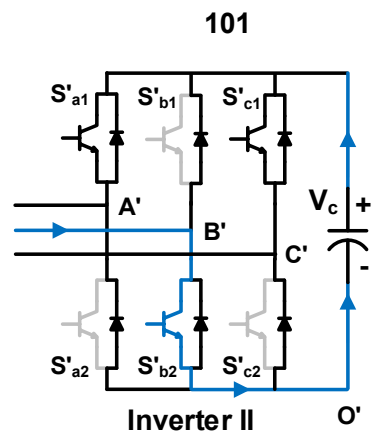
(c) 3' (010).



(d) 4' (011).



(e) 5' (001).



(f) 6' (101).

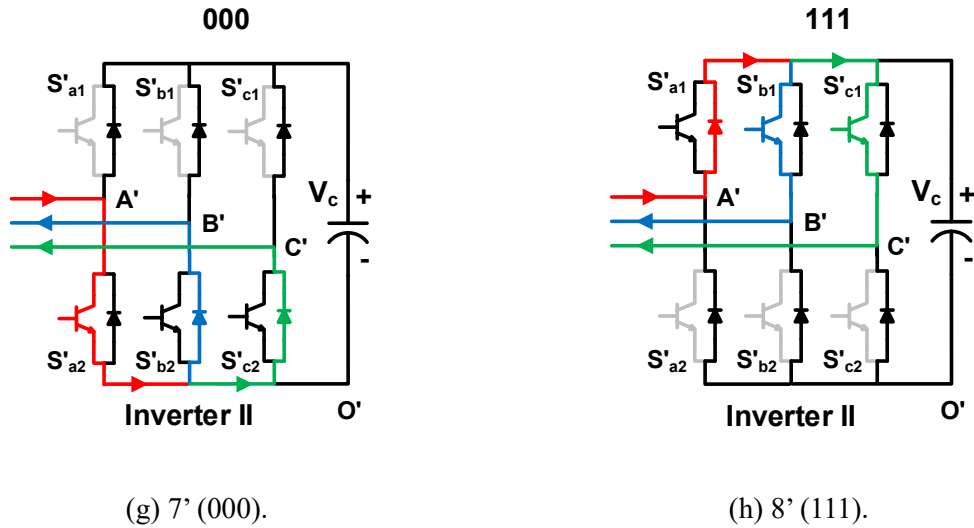


Fig. 1.62 Discharge path of vectors in Inverter II.

Table 1.6 Relationship between Switching States, Current Directions and Charging/Discharging States of Floating Capacitor

Switching state Charging /Discharging state	100	110	010	011	001	101	000/111
Charging	$+i_a$	$-i_c$	$+i_b$	$-i_a$	$+i_c$	$-i_b$	N/A
Discharging	$-i_a$	$+i_c$	$-i_b$	$+i_a$	$-i_c$	$+i_b$	N/A

The charging/discharging issue of the capacitor can also be analysed in the viewpoint of voltage and current vectors. According to Table 1.6, the current vector  $\mathbf{I}$  that discharging the capacitor should be in shaded regions in Fig. 1.63 for different effective vectors in Inverter II. It needs to note that the current vector directions are opposite with respect to two inverters, so that the current vector  $\mathbf{I}$  in Fig. 1.63 of Inverter II is opposite with the current vector of Inverter I and also the current vector of the OW machine. It can be seen that the angle between the basic voltage vector and current vector should be less than 90 degrees to discharge the capacitor. On the contrast, the charging of the capacitor accrues when the angle between the current and voltage vectors is greater than 90 degrees. This can also be explained by the power flowing between the floating capacitor and the electrical machine. If the angle between voltage and current vectors is less than 90 degrees, the power of Inverter II is positive, which means that power flows out of the Inverter II to the OW machine, so that the discharging of the capacitor

occurs. On the other hand, if the angle between the voltage and current vectors is greater than 90 degrees, the power of Inverter II is negative, which means power flows into Inverter II from the OW machine, so that the charging of the capacitor occurs.

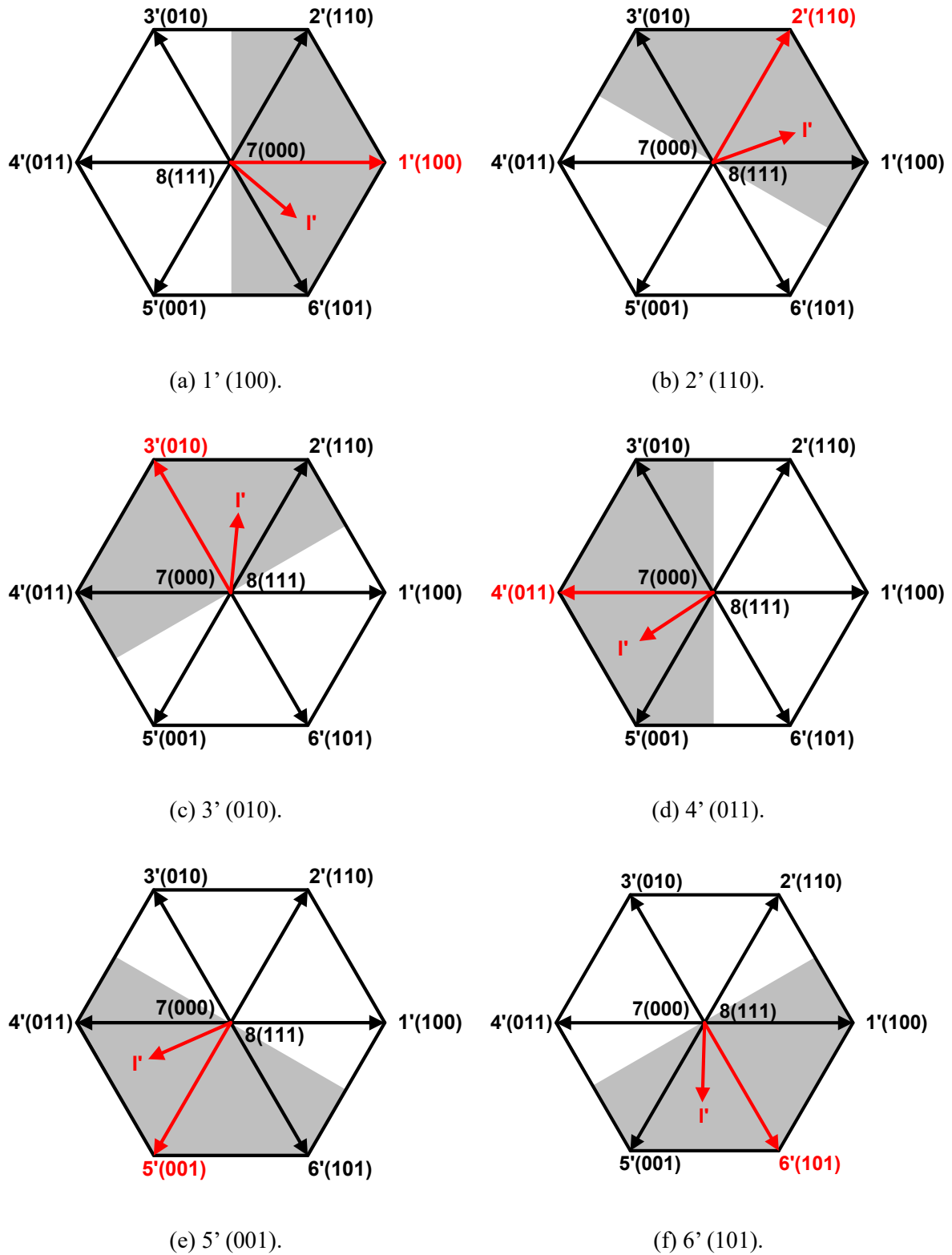
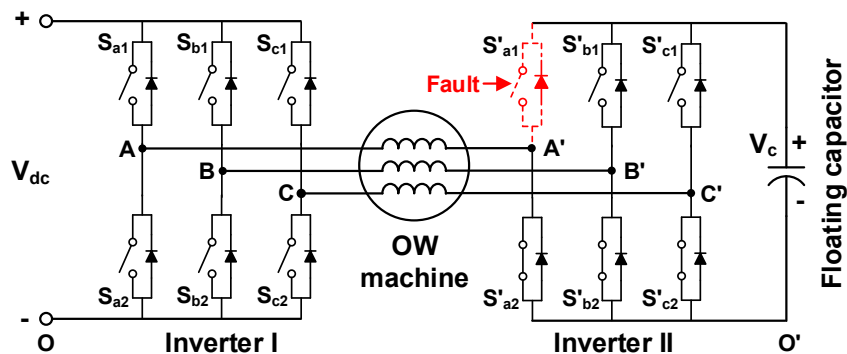


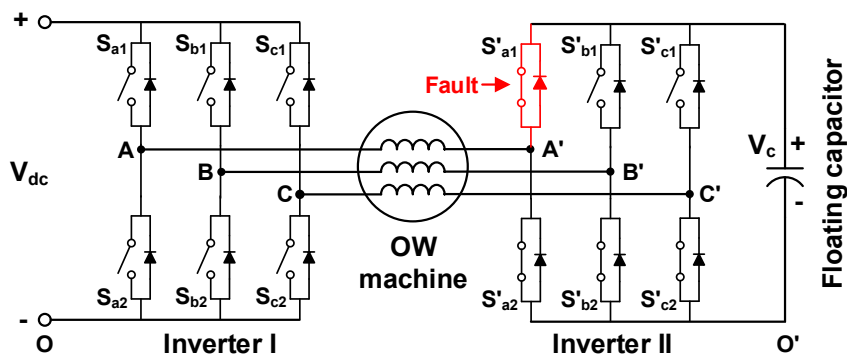
Fig. 1.63 Regions of current vector for discharging the capacitor.

## 1.6.2 Fault tolerant control

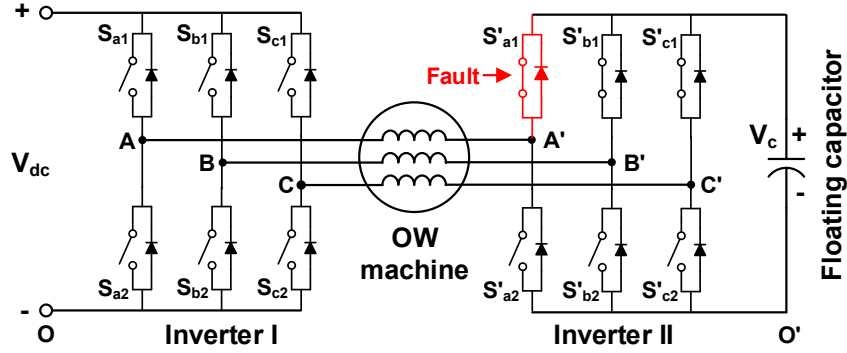
In an OW machine fed by floating capacitor DTL-VSIs, when a short- or open-circuit fault occurs in Inverter II which is fed by the floating capacitor, an artificial neutral can be created by turning on three low/up switches in Inverter II to achieve the fault tolerant operation [MAJ21]. For the open-circuit fault, the floating capacitor topology has the same fault tolerant action as the isolated DC-bus topology as shown in Fig. 1.64 (a) and Fig. 1.29 (a). For the short-circuit fault, the floating capacitor topology can create an artificial neutral by turning on either three up or low switches in Inverter II in Figs. 1.64 (b) and (c). However, to avoid a short circuit of the voltage source in the isolated DC-bus topology, only the three switches which are opposite to the short-circuit fault switch are turned on in Fig. 1.29 (b). In the isolated DC-bus topology, the short- or open-circuit fault can be resolved in both Inverters I and II, but only Inverter II short- or open-circuit fault can be resolved in the floating capacitor topology. As a result, the floating capacitor topology has a limited fault tolerant capability.



(a) Open-circuit fault (turn-on of three low switches).



(b) Short-circuit fault (turn-on of three low switches).



(c) Short-circuit fault (turn-on of three up switches).

Fig. 1.64 Artificial neutral of OW machine fed by floating capacitor DTL-VSIs.

## 1.7 Performance Comparison for Three Types of Dual Inverters

Fig. 1.65 shows PWM and control strategies of an OW-PMSM drive fed by three types of DTL-VSIs, i.e. isolated DC-bus, common DC-bus, and floating capacitor topologies, which have been reviewed in Sections 1.4-1.6. Compared with a two-level inverter, all three OW topologies have the advantage of larger voltage utilization and fault tolerant capability. However, among these three OW topologies, they have their own advantages and disadvantages. In this section, the three OW topologies will be compared in terms of cost, maximum linear modulation region, level of output voltages, existence of zero sequence circuit, control complexity, and fault tolerant capability.

- The isolated DC-bus dual inverters normally need a bulky transformer to achieve the isolation between two inverters, which can increase the weight and volume of the control system. However, the isolation can be easily achieved in the electric vehicle application by separated batteries. The floating capacitor topology needs a large capacitor to maintain a stable voltage for Inverter II. As a result, the common DC-bus topology has the lowest cost, as only one voltage source is needed.
- With the same DC-bus voltage  $V_{dc}$  for three types of DTL-VSIs, the isolated DC-bus topology has the largest linear modulation region, and the maximum modulation index (MI = reference voltage/ $V_{dc}$ ) is  $\frac{2}{\sqrt{3}}V_{dc}$ . The maximum modulation indices for the common DC-bus and floating capacitor topologies are  $V_{dc}$  and  $\frac{2}{3}V_{dc}$ , respectively.

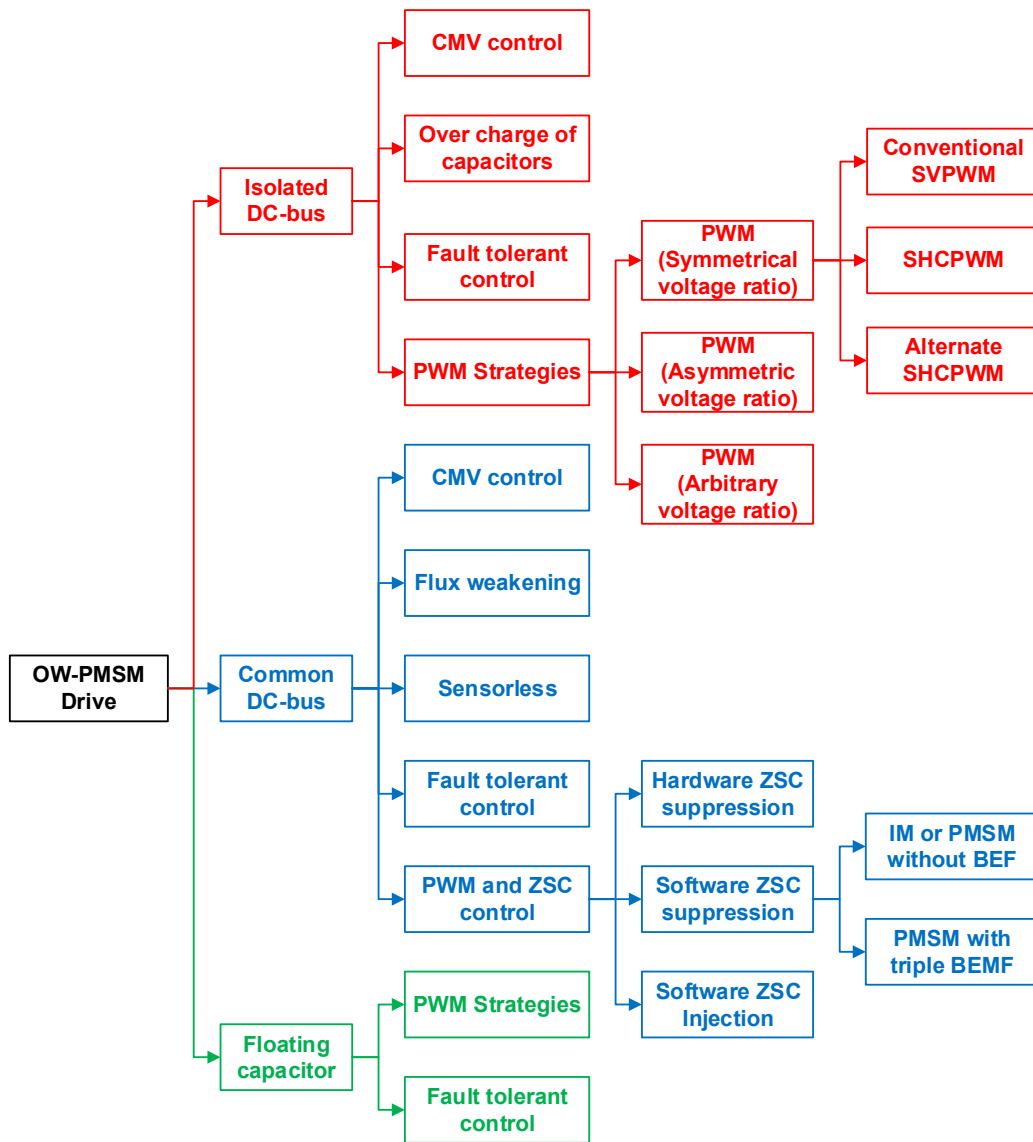


Fig. 1.65 PWM and control strategies of three types of OW-PMSM drive.

- The isolated DC-bus topology can output four-level voltages when the voltage ratio between two voltage sources is 1:2 or 2:1. The floating capacitor topology can output three-level voltages when the voltage ratio between the voltage source and the floating capacitor is 2:1. The common DC-bus topology can only generate two-level output voltages.
- Zero sequence circuit is blocked in the isolated DC-bus and floating capacitor topologies. However, ZSC can flow through the zero sequence circuit in an OW machine fed by common DC-bus dual inverters, which not only can be used for the fault tolerant control, but also can be used for the ZSC injection control for some special machine drives, such



as variable flux reluctance machine [ZHU16], vernier machine [LI19], switched reluctance machine [YU20].

- Due to the existence of zero sequence circuit in the common DC-bus topology, the control of ZSC is necessary, and the control of capacitor voltage is needed in the floating capacitor topology. On the contrast, there is no extra control requirement in the isolated DC-bus topology.
- Among the three types of DTL-VSIs, the common DC-bus topology has the highest level of fault tolerant capability, as short/open-circuit fault of both switches/diodes and windings can be resolved. The isolated DC-bus topology can solve the short/open-circuit fault of switches/diodes in two inverters, while the floating capacitor topology can only solve the short/open-circuit fault of switches/diodes in the inverter fed by the floating capacitor.

Table 1.7 gives a comprehensive comparison between the three types of DTL-VSIs, and a graphical assessment is given in Fig. 1.66. It can be seen that the isolated DC-bus topology has advantages in the larger maximum linear modulation region, higher level of output voltages, and lower control complexity, while the common DC-bus topology has advantages in lower cost, existence of zero sequence circuit, and higher fault tolerant capability. However, the floating capacitor topology shows no outstanding point compared with the other two topologies. In this thesis, PWM and control strategies for the isolated DC-bus and common DC-bus topologies are studied.

Table 1.7 Comparison of Three Types of DTL-VSIs

Topologies	Cost	Maximum linear modulation region	Level of output voltages	Zero sequence circuit	Control complexity	Fault tolerant capability
Isolated DC-bus topology	High	$MI \leq \frac{2}{\sqrt{3}} V_{dc}$ ( $V_{dc1} = V_{dc2} = V_{dc}$ )	Four ( $V_{dc1} = 2V_{dc2} = V_{dc}$ )	No	Low	Middle (Short/open-circuit fault of switch/diode)
Common DC-bus topology	Low	$MI \leq V_{dc}$	Two	Yes	High (ZSC control)	High (Short/open-circuit fault of switch/diode or winding)
Floating capacitor topology	Middle	$MI \leq \frac{2}{3} V_{dc}$	Three	No	High (Capacitor voltage control)	Low (Short/open-circuit fault of switch/diode in Inverter II)

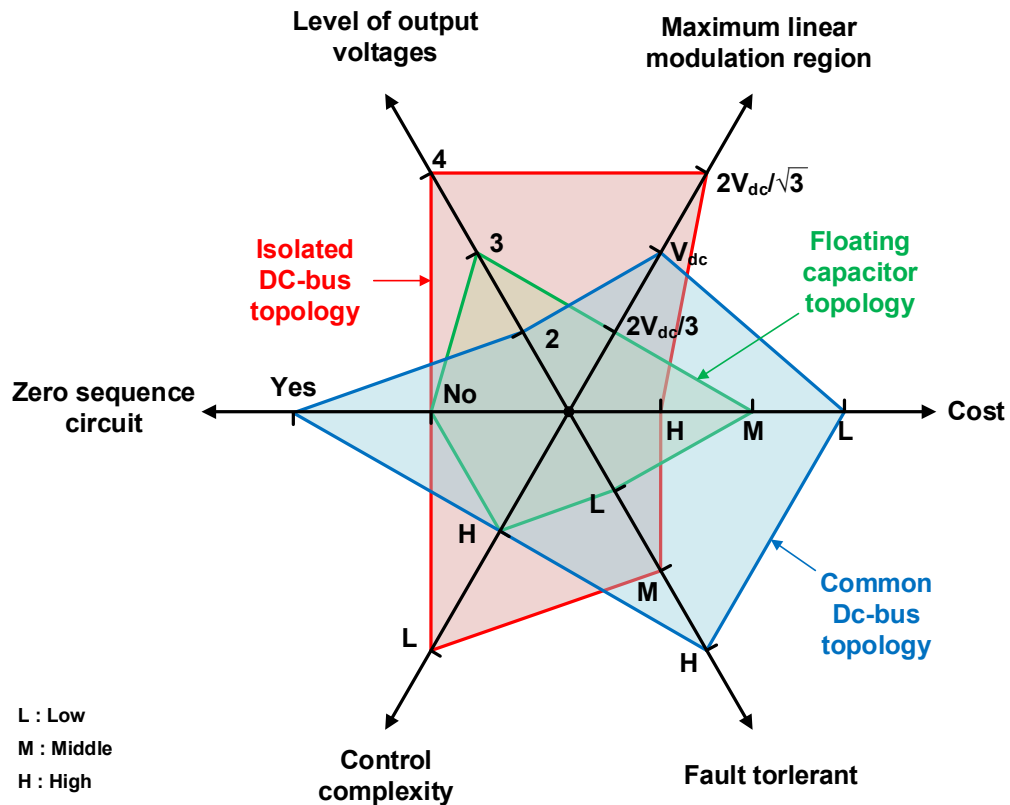


Fig. 1.66 Overall assessment of three types of DTL-VSIs.

## 1.8 Scope and Contributions of the Thesis

### 1.8.1 Motivation

From the above reviews, the trends of the OW-PMSM drive fed by DTL-VSIs can be summarized as follows:

- SHCPWM can achieve the optimal selection of basic vectors for an isolated DC-bus OW drive with 1:1 DC-bus voltage ratio, and the reference voltage vector can always be synthesized by three nearest basic vectors [SHI01]. However, SHCPWM can cause the unbalanced operation of two inverters. The alternate SHCPWM can achieve the balanced operation [SRI08], but generates more switching commutations.
- SPWM have the advantage of easy implementation, and is more preferable for the isolated DC-bus OW-PMSM drive [SEK13]. However, the existing SPWMs show larger current harmonics compared with SHCPWM.
- An OW-PMSM fed by isolated DC-bus dual inverters can output three-level voltages with a 1:1 DC-bus voltage ratio and four-level voltages with a 1:2 or 2:1 DC-bus voltage ratio.

Generalized SVPWM for the OW-PMSM drive with arbitrary DC-bus voltage ratios has wider applicability [HUA19b], but cannot select the optimal switching pattern for low current harmonics.

- (d) The ZSC control is necessary in the common DC-bus OW-PMSM drive, and a controllable ZSV should be generated by PWM to counteract with ZSVs from other sources to suppress ZSC [ZHA17a]. High frequency current harmonics can be reduced by the asymmetric vector sequence for the common DC-bus OW-PMSM drive [SHE19], but low frequency harmonics are induced.
- (e) POD-PWM can eliminate the variation of CMV for both the isolated DC-bus OW drive [KAL15] and common DC-bus OW drive [HU21], but also can induce large current harmonics.
- (f) Voltage saturation can be avoided by the voltage limitation in the flux weakening control of the common DC-bus OW-PMSM drive considering voltages in both zero sequence axis and  $dq$ -axis [SAN14]. However, the ZSC control can only be achieved in linear modulation regions.
- (g) The control of capacitor voltage can be achieved in the floating capacitor dual inverters by the selection of switching combinations considering both the voltage and current directions [HUA21]. A similar method can be used to solve the capacitor overcharge issue in the isolated DC-bus topology [HUA19c].

The researches in this thesis focus on PWM strategies for both isolated and common DC-bus OW-PMSM drive for performance improvement, such as low current harmonics, inverter nonlinearity compensation, CMV variation elimination, and operation range enhancement.

For an OW-PMSM fed by isolated DC-bus DTL-VSIs, the research scope includes

- 1) Low switching frequency SPWM with low current harmonics (1:1 DC-bus voltage ratio);
- 2) Low switching frequency generalized SPWM with low current harmonics (arbitrary DC-bus voltage ratio);
- 3) Inverter nonlinearity compensation with dual switching modes.

For an OW-PMSM fed by common DC-bus DTL-VSIs, the research scope includes

- 1) Vector action sequence optimization for low current harmonics;
- 2) CMV variation elimination SVPWM with low current harmonics;
- 3) SVPWM with operation range enhancement.

## 1.8.2 Outline

The outline of research in this thesis is organized as shown in Fig. 1.67.

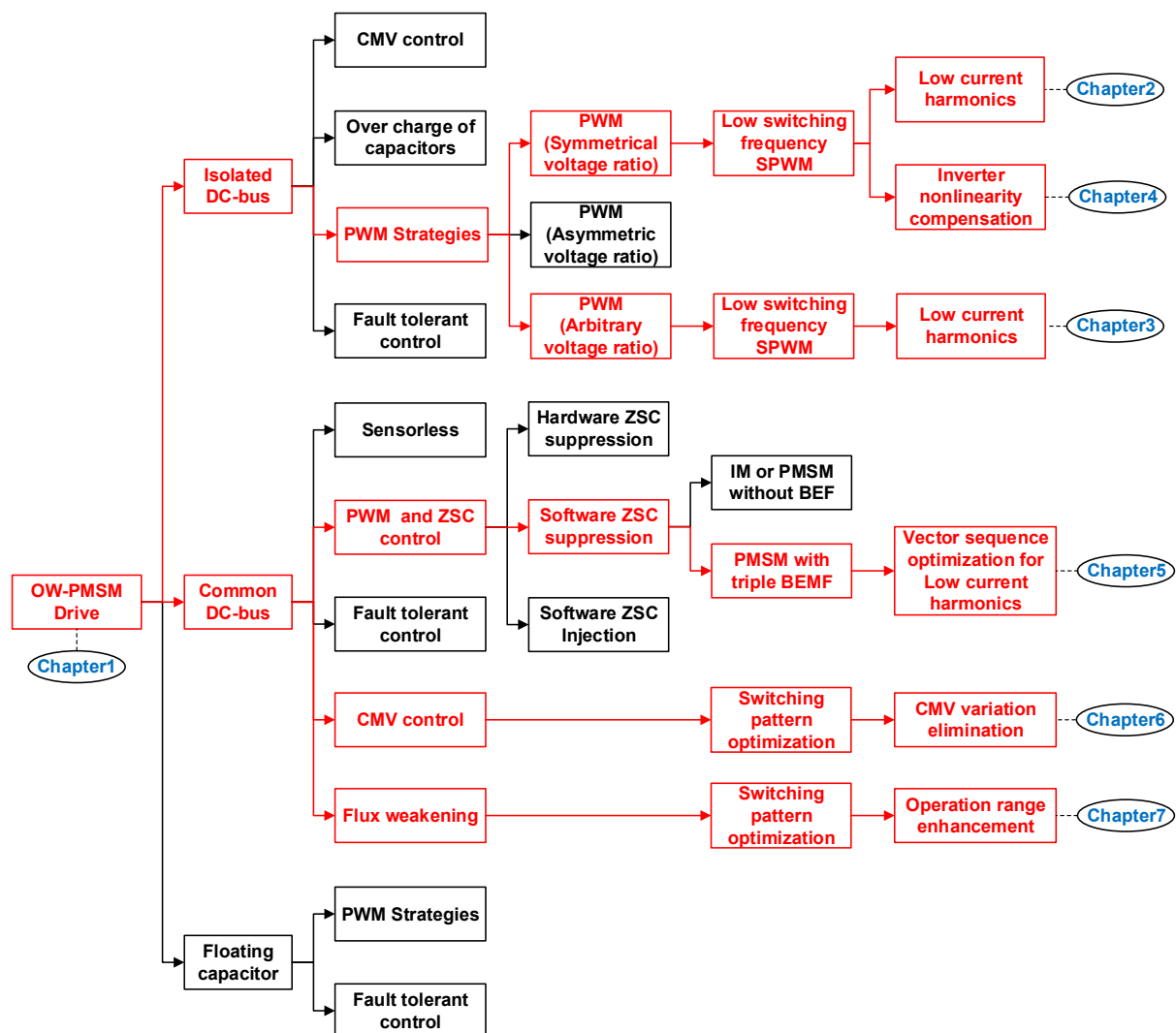


Fig. 1.67 Outline of research in the thesis.

PWM and control strategies of the isolated DC-bus OW drive are studied in Chapters 2-4. SPWM with ZSV injection and voltage distribution is proposed in Chapter 2 with low switching frequency and low current harmonics for DTL-VSIs with 1:1 DC-bus voltage ratio. For an OW machine fed by DTL-VSIs with arbitrary DC-bus voltage ratios, the optimal ZSV

injection and voltage distribution of SPWM are used for the current harmonic reduction in Chapter 3. Balanced and unbalanced voltage distribution methods can cause different inverter nonlinearity characteristics and are utilized for the inverter nonlinearity compensation in Chapter 4.

PWM and control strategies of the common DC-bus OW drive are studied in Chapters 5-7. They have the common point of the ZSC control, and different control objects are achieved by the selection of optimal switching patterns of dual inverters. The optimal vector action sequence is analysed and used for the current harmonic reduction in Chapter 5. Chapter 6 focuses on the CMV variation elimination with the merits of low switching frequency and low current harmonics. The modulation region of the OW drive is analysed and the switching combinations with non-null ZSV on the large hexagon are used for the ZSC control to extend the operation range in Chapter 7.

### 1.8.3 Contributions

The major contributions of this thesis are as follows:

1. Two novel SPWM strategies with a simple implementation are proposed for an OW drive fed by isolated DC-bus DTL-VSIs with a 1:1 DC-bus voltage ratio to reduce switching frequency and current harmonics. (**Chapter 2**)
2. A generalized SPWM with the optimal combinations of the ZSV injection and voltage distribution is proposed with low current harmonics for an OW drive fed by isolated DC-bus DTL-VSIs with arbitrary DC-bus voltage ratios. (**Chapter 3**)
3. A novel inverter nonlinearity compensation method is proposed for an OW drive fed by isolated DC-bus DTL-VSIs based on the mode-switching between balanced and unbalanced switching modes, and can overcome the issues in conventional methods, such as the need of accurate rotor position and pre-set compensation voltage curves, mixed voltage distortions caused by inverter nonlinearity and back EMF harmonics, and slow convergence speed. (**Chapter 4**)
4. A novel SVPWM strategy for an OW drive fed by common DC-bus DTL-VSIs is proposed with the optimal selection of effective and zero voltage vector action sequences to reduce current harmonics. (**Chapter 5**)

5. A novel SVPWM strategy is proposed for both the CMV variation elimination and ZSC suppression in a common DC-bus OW drive with low current harmonics and switching frequency. (**Chapter 6**)
6. A novel SVPWM is proposed to achieve the ZSC control and extend the operation range by considering voltages in zero sequence axis and voltage vectors in  $\alpha\beta$ -plane, both of which are mapped by switching combinations in an OW drive. (**Chapter 7**)

# **CHAPTER 2 LOW SWITCHING FREQUENCY SPWM STRATEGIES FOR OPEN WINDING MACHINE WITH LOW CURRENT HARMONICS**

In this chapter, two novel SPWM strategies with simple implementation are proposed for an OW machine fed by isolated DC-bus dual two-level three-phase inverters to reduce switching frequency and current harmonics. The proposed strategies utilize zero sequence voltage injection and unbalanced reference voltage distribution to generate discontinuous PWM with low current harmonics and less switching actions. Two different zero sequence voltages are introduced in this chapter corresponding to two proposed PWM strategies with different switching actions in a PWM cycle. The novelty of this chapter is low current harmonics and less switching actions in a PWM cycle compared with the conventional SPWM strategy. Moreover, compared with the SHCPWM strategy, the proposed SPWM strategies have advantages of easy implementation and half switching commutations with the same current harmonic characteristics. The superiority of the proposed SPWM strategies is validated by simulation and experiment results.

This chapter is based on the papers published in:

L. Xu and Z. Q. Zhu, “Low switching frequency SPWM strategies for open-winding machine with low current harmonics,” 2021 IEEE International Electric Machines & Drives Conference (IEMDC), 2021, pp. 1-7.

L. Xu, Z. Q. Zhu and L. Yan, “Low switching frequency SPWM strategies for open-winding machine with low current harmonics,” *IEEE Transactions on Industry Applications*, vol. 58, no. 2, pp. 2042-2054, Mar.-Apr. 2022.



## 2.1 Introduction

In a PWM-controlled inverter, the reference voltage vector is synthesized by several basic voltage vectors in an average sense. On the one hand, due to the limitation of switching frequency, the error between the reference voltage vector and the instantaneous actual output voltage vector will generate current harmonics in phase currents [SEK13], which can cause extra loss in electrical machine and should be considered when choosing a PWM strategy for the inverter. On the other hand, the PWM frequency affects the magnitudes of current harmonics as well as the loss of the inverter. In addition to the effect on harmonic characteristics and loss of the OW inverter, PWM strategies can also affect the voltage utilization of the inverter when shunt sensing technology is applied [ZHA17c] [CHO13], in which two or three shunts on the lower arms are used and phase currents can be sampled during the zero vector. In this chapter, current harmonics, switching loss and voltage utilizations are studied for PWM strategies of dual two-level inverters.

PWM strategies have great influence on the performance of VSIs. Many continuous and discontinuous, sinusoidal and space vector PWM strategies are reported [SEK13] [SRI13]. Compared with the SVPWM strategy, the implementation of a SPWM strategy is easier, since the calculation of sectors and vector duration can be avoided. However, a ZSV should be injected to reference voltages to achieve the same voltage utilization and harmonic characteristics as the SVPWM strategy [ZHO02]. As a result, the SPWM strategy with zero sequence voltage injection has the same performance as the SVPWM strategy, and reduces the implementation complexity. A discontinuous SPWM strategy is proposed in [SEK13] for an OW induction machine fed by dual two-level inverters, and the two inverters are controlled independently. Two ZSVs are injected to the reference voltages of two inverters, respectively, and the switching actions can be reduced by 1/3 in a PWM cycle. However, high current ripples are generated as improper selection of vectors. In this chapter, two novel SPWM strategies are proposed here with easier implementation, and only a ZSV needs to be injected to the reference voltage of dual inverters. Moreover, only parts of switches of dual inverters are switched in a PWM cycle utilizing an unbalanced voltage distribution method. As a result, with the same PWM frequency, the average switching frequency of proposed PWM strategies can be reduced, compared with the conventional SPWM strategy. Two different ZSVs are used in this chapter, and the switching actions in a PWM cycle can be reduced by half and two third, respectively. Besides, in the proposed PWM strategies, the reference voltage vector can always be

synthesized by three nearest voltage vectors of dual inverters, and thus the overall current ripples can be reduced, compared with that in the conventional SVPWM strategy.

## 2.2 Dual Two-level Inverters and Conventional SPWM Strategy

An OW machine fed by isolated DC-bus dual two-level three-phase inverters is shown in Fig. 2.1. Three phase windings are unconnected compared with a conventional Y-connection machine, and two two-level inverters are connected to the two terminals of phase windings. Fig. 2.2 shows the space vector plane and sectors of dual two-level inverters with the same DC-bus voltages.

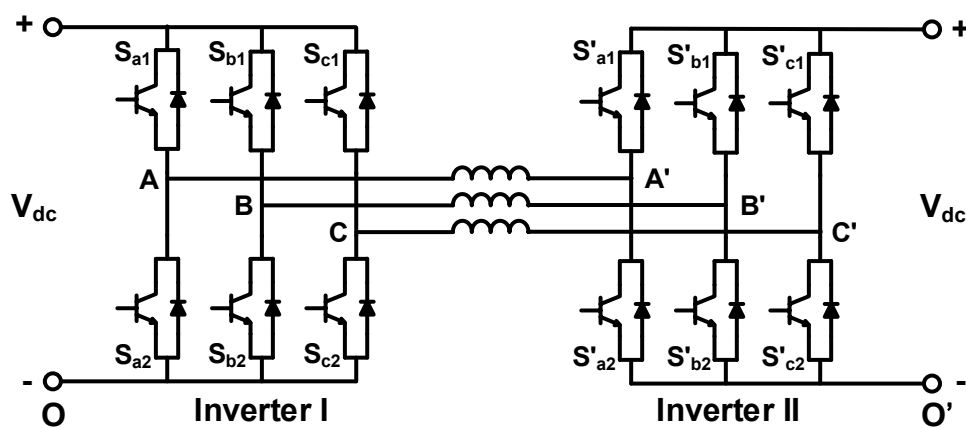


Fig. 2.1 Topologies of isolated DC-bus dual two-level inverters.

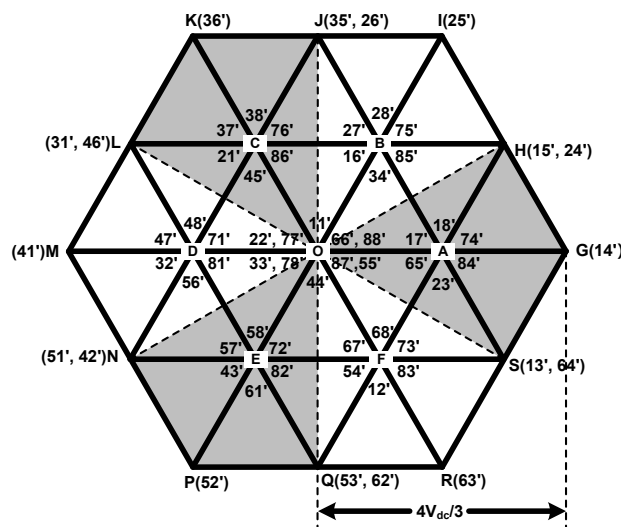


Fig. 2.2 Space plane for dual two-level inverters.

There are 64 switching combinations and 19 voltage locations, which are much more than those in the two-level inverter. As a result, there are more redundant vectors that can be used to

design PWM strategies, and thus it has the potential to improve the performance of the control system. The switching combinations of dual inverters are the combinations of switching states of each inverter. For example, Inverter I switching state is 1 (100) when the states of three upper switching devices are “on”, “off” and “off”, and the switching state of Inverter II is 4' (011). These individual states of the two inverters together form the switching combination ‘14’ for the OW machine drive, which is located at ‘G’ in the space vector plane.

The relationship between the reference voltages of dual inverters and two individual inverters can be expressed as

$$\mathbf{V}_s = \mathbf{V}_{s1} - \mathbf{V}_{s2} \quad (2.1)$$

where  $\mathbf{V}_s$  is the reference voltage vector for dual inverters,  $\mathbf{V}_{s1}$  and  $\mathbf{V}_{s2}$  are the reference voltage vectors for two inverters, respectively.

The control diagram of the conventional SPWM strategy with ZSV injection is shown in Fig. 2.3. Each individual inverter is controlled by SPWM strategy, which can simply transform reference voltages of each inverter to duty cycles.

The voltage distribution module in Fig. 2.3 determines reference voltages for two inverters. In the conventional SPWM strategy, the reference voltage vectors of two inverters have the same magnitudes and opposite directions, and the relationship between the two reference voltages of two inverters and the reference voltage of dual inverters are given by

$$\begin{cases} V_{n1}^* = V_n^* / 2 \\ V_{n2}^* = -V_n^* / 2 \end{cases} \quad (n = A, B, C) \quad (2.2)$$

where  $V_n^*$  is the reference voltage for dual inverters in arbitrary phase,  $V_{n1}^*$  and  $V_{n2}^*$  are the reference voltages for two inverters in arbitrary phase, respectively.

To improve the voltage utilization of SPWM strategy for two two-level inverters, two ZSVs need to be injected to reference voltages of two inverters, respectively, which can equalize the durations of two zero vectors and achieve the same voltage utilization as SVPWM [ZHO02]. The ZSVs for two inverters can be expressed as

$$\begin{aligned} V_{z1} &= \left[ V_{dc} - \max(V_{a1}^*, V_{b1}^*, V_{c1}^*) - \min(V_{a1}^*, V_{b1}^*, V_{c1}^*) \right] / 2 \\ V_{z2} &= \left[ V_{dc} - \max(V_{a2}^*, V_{b2}^*, V_{c2}^*) - \min(V_{a2}^*, V_{b2}^*, V_{c2}^*) \right] / 2 \end{aligned} \quad (2.3)$$

The reference voltages for two inverters after the injection of the ZSV can be expressed as

$$\begin{aligned} V_{n1\_z}^* &= V_{n1}^* + V_{z1} \\ V_{n2\_z}^* &= V_{n2}^* + V_{z2} \end{aligned} \quad (2.4)$$

It can be observed that the reference voltage of dual inverters in each phase is distributed equally to two inverters in the conventional SPWM strategy. This PWM strategy has the same performance as the SVPWM strategy, such as maximum modulation region and current harmonics, but its implementation is much easier. The PWM waveforms of the conventional SPWM strategy with ZSV injection are shown in Fig. 2.4. With the unipolar SPWM, reference voltages in (2.4) can be converted to duty cycles for two inverters by

$$\begin{aligned} Duty_{n1\_z} &= \frac{V_{n1\_z}^*}{V_{dc}} \\ Duty_{n2\_z} &= \frac{V_{n2\_z}^*}{V_{dc}} \end{aligned} \quad (2.5)$$

With the injection of ZSVs for two two-level inverters, the durations of two zero vectors are the same in Fig. 2.4, i.e.  $T_7=T_8$  in Inverter I and  $T_7'=T_8'$  in Inverter II. All switches in the dual inverters are switched in the conventional SPWM strategy. Compared with a two-level inverter, although the dual inverters have the advantages such as high voltage utilization and fault tolerant abilities, it can cause more switching loss due to the switching action of all switches in two inverters.

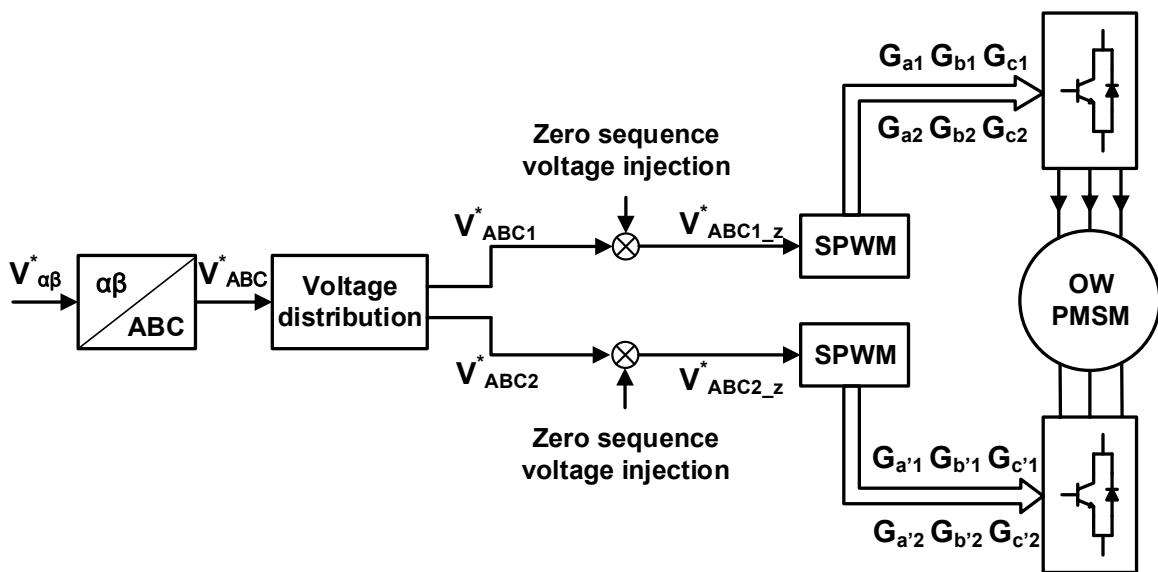


Fig. 2.3 Control diagram of conventional SPWM with ZSV injection.

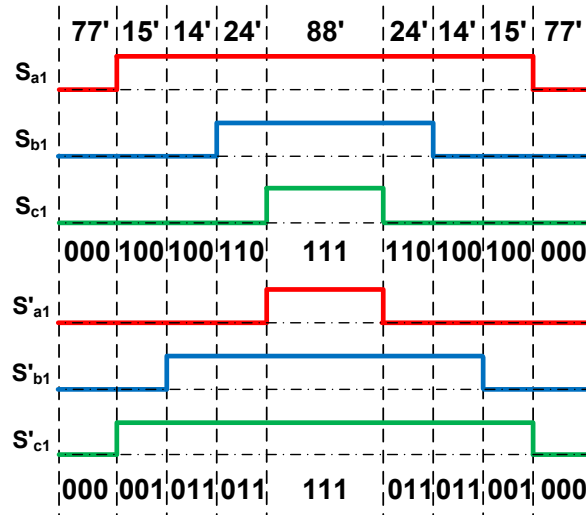


Fig. 2.4 PWM waveforms of conventional SPWM with ZSV injection.

In this chapter, two novel SPWM strategies are proposed for isolated DC-bus dual two-level inverters to reduce switching frequency and current harmonics.

## 2.3 Proposed SVPWM Strategies

### 2.3.1 PWM strategy implementation

In the conventional SPWM strategy for dual inverters, two inverters are regarded as independent control targets, and the SPWM strategy with ZSV injection of the conventional two-level inverter is applied to each individual inverter. However, in the proposed SPWM strategies the dual two-level inverters are regarded as only one whole control target. The control diagram of proposed SPWM strategies is similar as that of conventional SPWM strategy as shown in Fig. 2.5, but the injection of one ZSV is applied to the reference voltage of dual inverters rather than the injection of two ZSVs for two inverters in the conventional SPWM strategy. Moreover, the implementations of ZSV injection and voltage distribution modules are different. Two different ZSVs will be introduced in this chapter to improve the voltage utilization, and two SPWM strategies are proposed with different reduced switching actions in a PWM cycle for an OW machine fed by dual inverters.

The first new ZSV can be expressed as

$$V'_z = [V_{dc} - V_{\max} - V_{\min}] / 2. \quad (2.6)$$

The second new ZSV can be expressed as

$$V'_z = \begin{cases} -V_{\min} & V_{\min} + V_{\max} \leq V_{dc} \\ V_{dc} - V_{\max} & V_{\min} + V_{\max} > V_{dc} \end{cases} \quad (2.7)$$

where  $V_{\min} = \min(V_A^*, V_B^*, V_C^*)$ ,  $V_{\max} = \max(V_A^*, V_B^*, V_C^*)$ .

To calculate  $V_{\min}$  and  $V_{\max}$ , three new voltages are introduced as

$$V_n^{*'} = \begin{cases} V_n^* & \text{if } V_n^* \geq 0 \\ V_{dc} + V_n^* & \text{if } V_n^* < 0 \end{cases} \quad (n = A, B, C) \quad (2.8)$$

where  $V_n^*$  is the reference voltage of dual inverters in arbitrary phases,  $V_{dc}$  is the DC-bus voltage.

Proposed SPWM1 and SPWM2 strategies are generated by the injection of two new ZSVs, respectively. After the injection of new ZSV, the three phase reference voltages of dual inverters are

$$V_{n\_z}^* = V_n^* + V'_z. \quad (2.9)$$

To reduce the switching frequency, a new unbalanced voltage distribution method is proposed as

$$\begin{cases} \begin{cases} V_{n1}^* = V_{n\_z}^* \\ V_{n2}^* = 0 \end{cases} & \text{if } V_{n\_z}^* > 0 \\ \begin{cases} V_{n1}^* = 0 \\ V_{n2}^* = -V_{n\_z}^* \end{cases} & \text{if } V_{n\_z}^* < 0 \end{cases}. \quad (2.10)$$

Duty cycles can also be calculated by (2.5) with the unipolar SPWM. It needs to note that SPWM1 and SPWM2 strategies have the same unbalanced voltage distribution method, and the only difference is the injection of ZSV. The PWM waveforms of the two proposed SPWM strategies in a PWM cycle are shown in Figs. 2.6 (a) and (b), respectively. It is worth noting that the phases of carrier signals for two inverters are opposite in the proposed SPWM strategies, while they are the same in the conventional SPWM strategy. As a result, the PWM waveforms are high-level centred in Inverter I and low-level centred in Inverter II. The proposed SPWM can also be implemented with SVPWM principle in Appendix A, and the effect of opposite-phase carriers is analysed in detail. In Fig. 2.6 (a), the switches at three of six legs are switched,

and other switches are clamped in the proposed SPWM1, so that the switching actions is half of that in the conventional SPWM. For the proposed SPWM2 in Fig. 2.6 (b), only the switches at two of six legs are switched, and the switching actions is one third of that in the conventional SPWM. Moreover, switching combinations used in the proposed SPWM strategies are also shown in Fig. 2.6, and there are seven segments and five segments in a PWM cycle in the proposed SPWM1 and SPWM2, respectively.

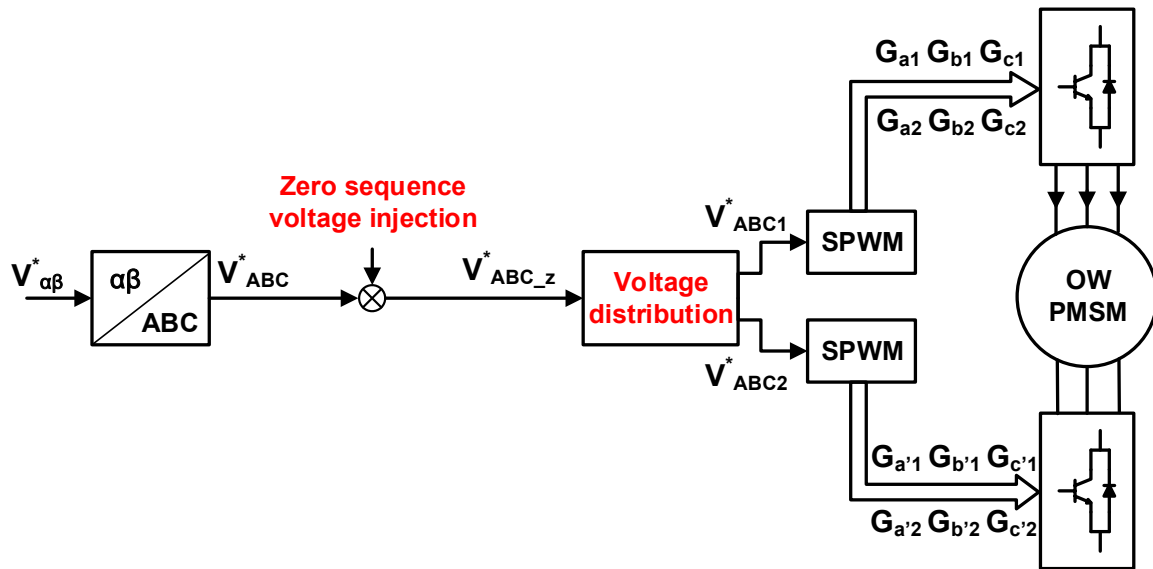


Fig. 2.5 Control diagram of the proposed SPWM with ZSV injection.

In the two proposed SPWM strategies, not all six legs of dual inverters are switched in a PWM cycle, and only half and one third of the six legs are switched. The injection of ZSV can change the duty cycle of switched legs and distribute the duration of the vector, which is located at the central of a sector. For example, the central vector is located at point A in sector 1 of the space plane.  $T_A$  is the duration of the central vector at point A, and Table 2.1 shows the distribution of  $T_A$  to the durations of  $V_{17'}$  and  $V_{75'}$  with different ZSVs. It needs to note that both switching combinations  $V_{17'}$  and  $V_{75'}$  are located at point A in the space plane. The first ZSV in Table 2.1 can generate the average distribution of the central vector, while the second and third ZSVs can generate 5-segment PWMs with less switching actions. The first ZSV is used in the proposed SPWM1, while the second and third ZSVs are used in the proposed SPWM2. A general expression of ZSVs is shown in the last row of Table 2.1, in which  $x$  represents the inequality of central vector distribution. For the first ZSV,  $x$  is 0.5, while  $x$  is 0 and 1 for the second and third ZSVs, respectively. Compared with the first three ZSVs, the other ZSVs generate 7-segment PWMs and cause an unequal distribution of the central vector, which can induce larger current harmonics. Similar result can be seen from [SRI13]. Different  $x$  values

are analysed in [SRI13], and the current ripple is the lowest when  $x$  is 0.5, which corresponds to the first ZSV in Table 2.1. Consequently, other ZSVs show no advantage in current harmonics and switching loss, and only the three ZSVs are used in this chapter.

Table 2.1 ZSVs and Duration of Central Vectors in Sector 1

ZSVs	Duration of $V_{17'}$	Duration of $V_{75'}$
$(V_{dc}-V_{max}-V_{min})/2$	$T_A/2$	$T_A/2$
$-V_{min}$	$T_A$	0
$V_{dc}-V_{max}$	0	$T_A$
$x(V_{dc}-V_{max}+V_{min})-V_{min}$	$(1-x)T_A/2$	$xT_A/2$

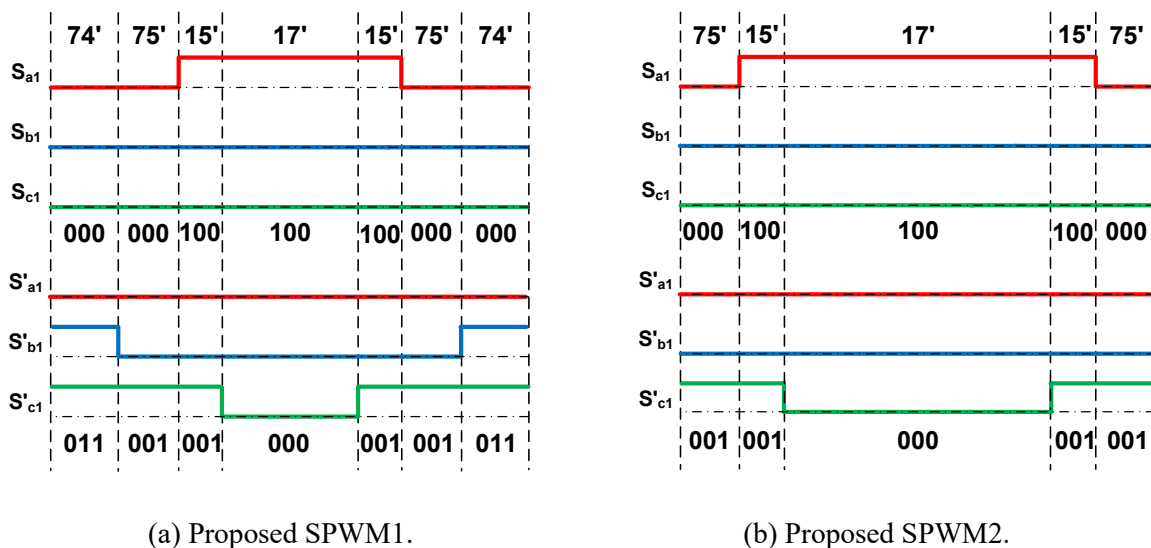


Fig. 2.6 PWM waveforms of proposed SPWMs with ZSV injection.

### 2.3.2 Comparative performance analysis

Figure 2.7 shows the vectors that are used in the conventional and proposed SPWM strategies corresponding to the PWM waveforms in Fig. 2.4 and Fig. 2.6, respectively. In the view point of space vectors, the reference voltage vector is always synthesized by three nearest vectors of dual inverters in the proposed SPWM strategies. However, this cannot be guaranteed in the conventional SPWM strategy, and zero vector is always used while effective vectors in the small hexagon (ABCDEF) are not used. As a result, the selection of vectors in the proposed



SPWM strategies is better than that in the conventional SPWM strategy, and the current ripples are lower in the proposed SPWM strategy. The selection of basic vectors of the proposed SPWM1 and SPWM2 is the same, and the difference is the use of switching combinations. Taking Fig. 2.6 as an example, both switching combinations 74' and 17' are used in the proposed SPWM1, while only switching combination 17' is used in SPWM2, and they are located at the same location A in the space vector plane of dual two-level inverters.

In [SEK13], the conventional SPWM is improved with different ZSV injections, and four legs are switched while the other two legs are clamped. This SPWM strategy only can provide two third switching actions in a PWM cycle, compared with the half and two third switching actions in the proposed SPWM strategies. PWM waveforms and the vector utilization in the space vector plane for this SPWM in sector 1 with different modulation indices ( $MI = \text{reference voltage}/V_{dc}$ ) are shown in Fig. 2.8. The switching actions can be reduced by 1/3 in a PWM cycle compared with the conventional SVPWM, since one leg is clamped in each inverter. It can be observed that the reference voltage vector is synthesized by three nearest vectors of the dual inverters when the modulation index is 0.4. However, this SPWM strategy cannot keep the optimal selection of vectors in high modulation regions as shown in Fig. 2.8 (b) and (c). Compared with Fig. 2.7 (b), the reference voltage vector is always synthesized by three nearest vectors of the dual inverters in the proposed SPWM strategies. As a result, the proposed SPWM strategies have lower current harmonics in high modulation regions.

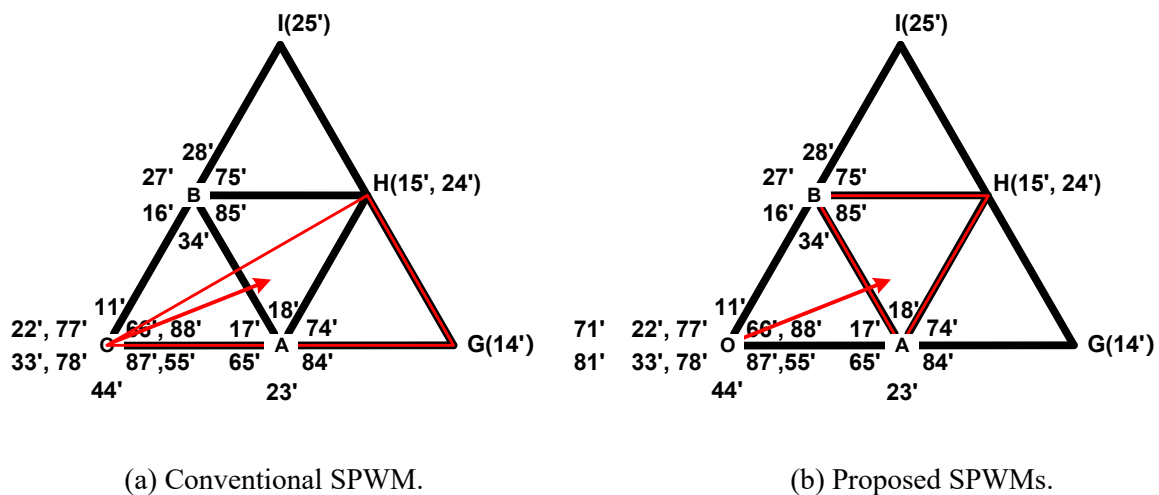
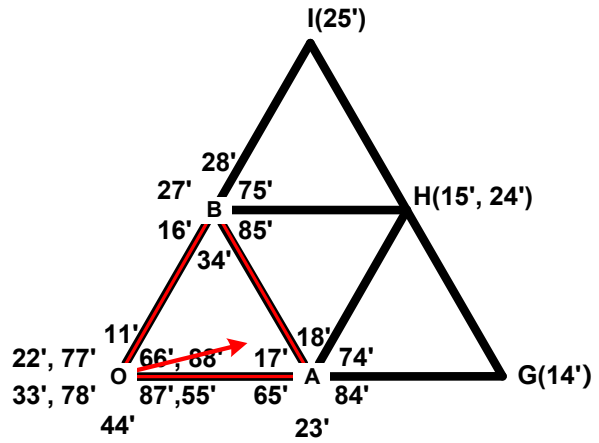
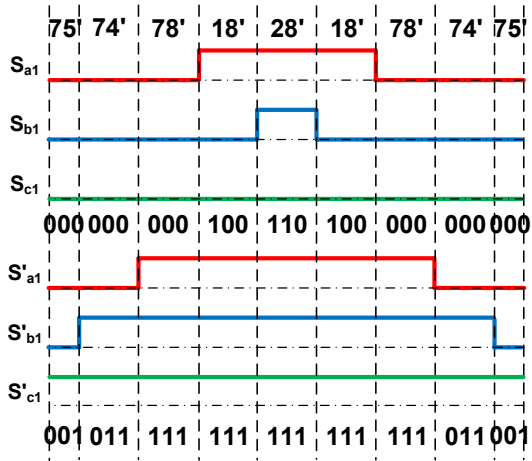
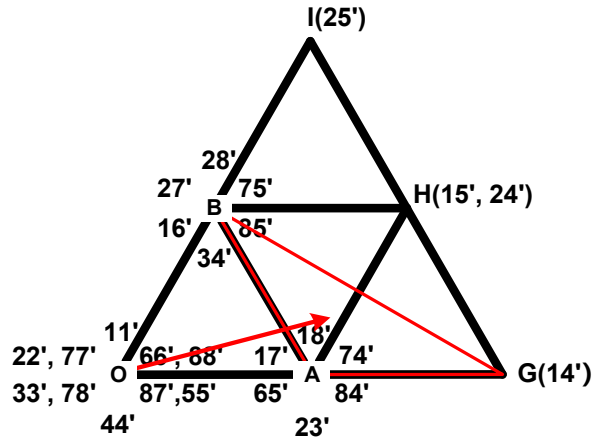
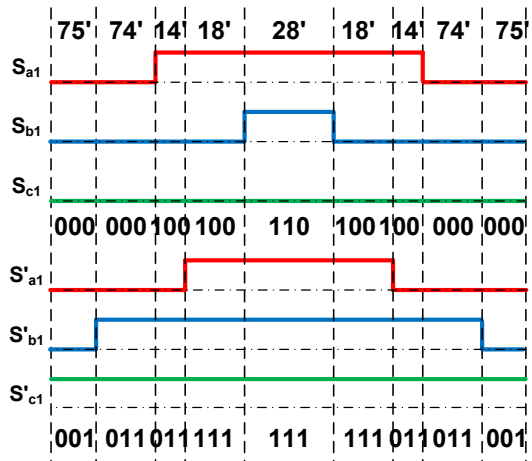


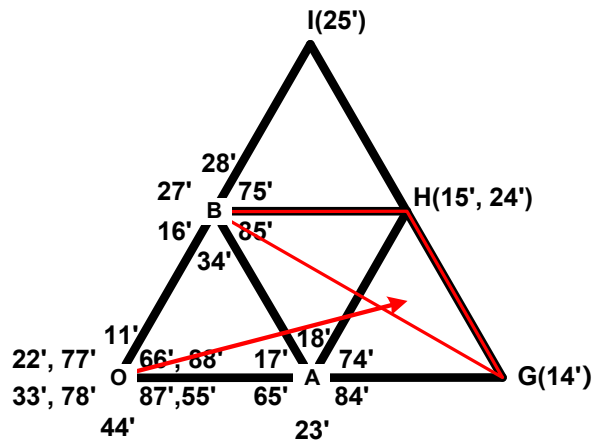
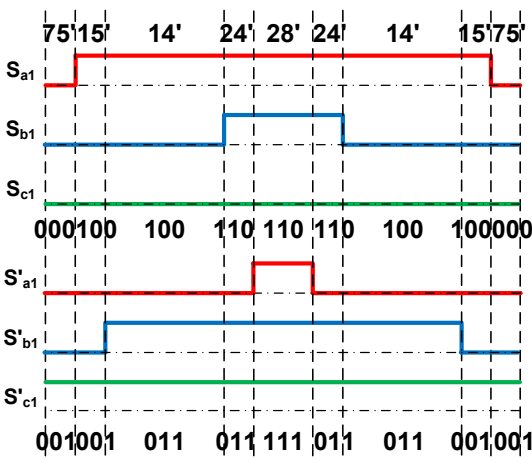
Fig. 2.7 Vectors in the conventional and proposed SPWM strategies.



(a) MI=0.4.



(b) MI=0.7.



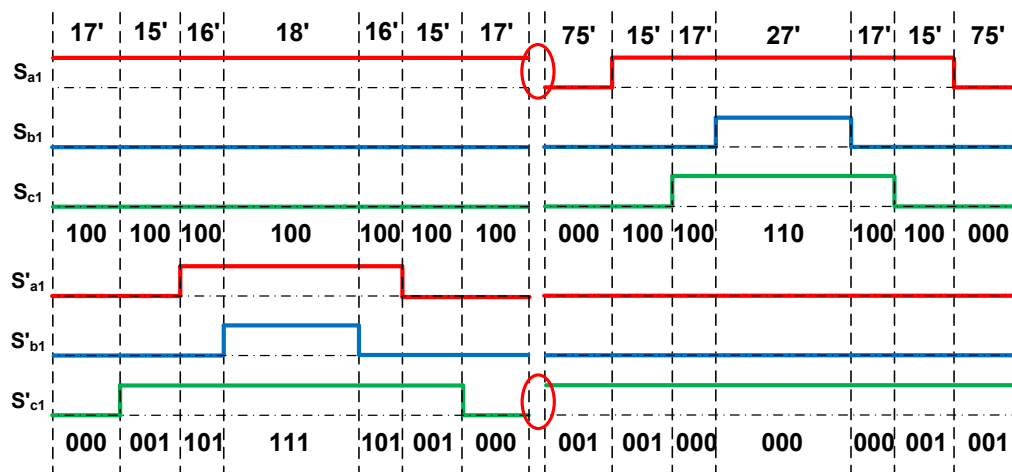
(c) MI=1.

Fig. 2.8 PWM waveforms and vectors for the SPWM of [SEK13] in sector 1.

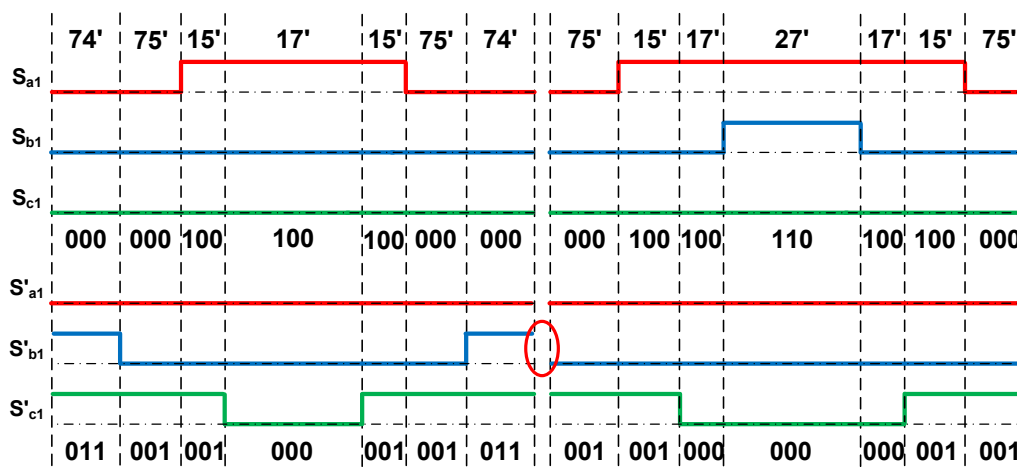
In the SHCPWM strategy, one inverter is clamped and the other inverter is switched to generate the desired voltage vector [SRI13]. The proposed SPWM1 strategy has the same switching actions and the same utilization of vectors but different switching combinations compared to the SHCPWM strategy. Consequently, they have the same harmonic characteristics. However, there are some advantages of the proposed SPWM1 strategy compared with the SHCPWM strategy. First, the implementation of the proposed SPWM1 strategy is much easier, since the calculation of sectors and reference voltage vectors can be avoided compared with the SHCPWM strategy. The advantage of easy implementation in SPWM strategy is more obvious with the increase of inverter voltage levels, as the increase of voltage vectors in a multilevel inverter [IQB09] [POU12]. The OW machine fed by isolated DC-bus dual two-level inverters can be equivalent to a three-level inverter, and there are 64 switching combinations in the space vector plane. Consequently, SPWM strategy can significantly reduce the memory and computation burden of a digital processor. Moreover, due to different clamping states in different sectors in the SHCPWM strategy, extra switching actions are generated during the sector change, which is designated as switching commutations in this chapter. The SHCPWM strategy in [SRI13] reduces switching commutations from 24 in [SOM08b] to 12 in an electrical cycle, and switching commutations can be further reduced to 6 in this chapter. Less switching commutations can reduce the switching loss especially when the ratio between PWM and electrical fundamental frequencies is low. PWM waveforms in sectors 1 and 2 of the SHCPWM strategy are shown in Fig. 2.9 (a). There are two switching commutations during sector change, and will be a total of 12 switching commutations in an electrical cycle. PWM waveforms in sectors 1 and 2 of the proposed SPWM1 strategy are shown in Fig. 2.9 (b). There is only one switching commutation during sector change, and thus are overall 6 switching commutations in an electrical cycle. As a result, the proposed SPWM1 strategy can reduce switching commutations by half compared with the SHCPWM strategy.

Pulse width modulation can generate current harmonics due to the error voltages between the instantaneous output voltage and the reference voltage. A current harmonic analysis method based on switching states of the OW inverter is proposed in [SEK13] and the transient actual output voltages are acquired according to switching states. The error between the actual output and reference voltages is used to calculate current ripples. The method in [SEK13] is used to analyse current harmonics of the proposed SPWM, conventional SPWM, SPWM in [SEK13], and SHCPWM strategies with different modulation indices. It needs to note that switching actions in a PWM cycle are different for these PWM strategies. As a result, these PWM

strategies should be compared with the same switching loss and different PWM frequencies. The current ripples in  $\alpha\beta$ -axis in each segment can be calculated according to the method in [SEK13], and then current ripple trajectories in  $\alpha\beta$  plane can be depicted. Taking the reference voltage vector in sector 1 as an example, the locations of reference voltage vectors and current ripple trajectories in  $\alpha\beta$  plane are shown in Fig. 2.10. It can be observed that the proposed SPWM1 and SPWM2 have low current ripples in whole modulation regions. Besides, since the two proposed SPWM strategies use the same basic vectors, SPWM1 and SPWM2 have similar current ripples in low and high modulation regions. However, SPWM1 has slightly lower current ripples in middle modulation regions. The SHCPWM strategy has the same current ripple trajectory as the proposed SPWM1. For the SPWM in [SEK13], it has similar current harmonics with the proposed SPWM strategies in low modulation regions, but has large current ripples in high modulation regions.

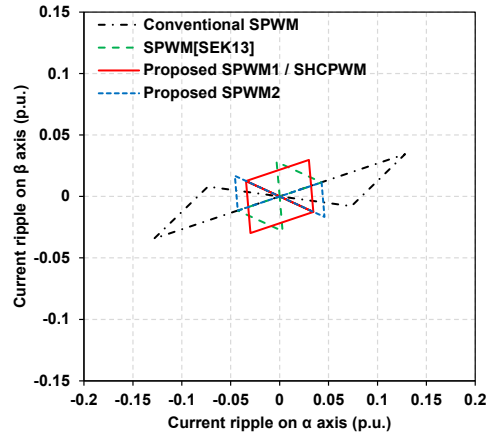
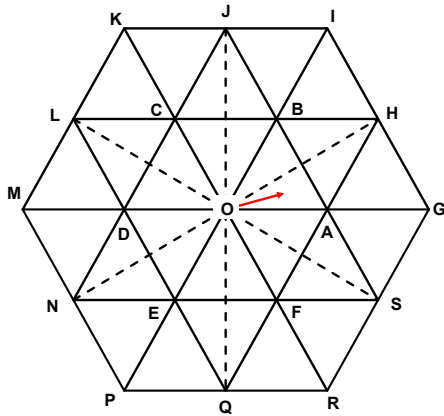


(a) SHCPWM strategy.

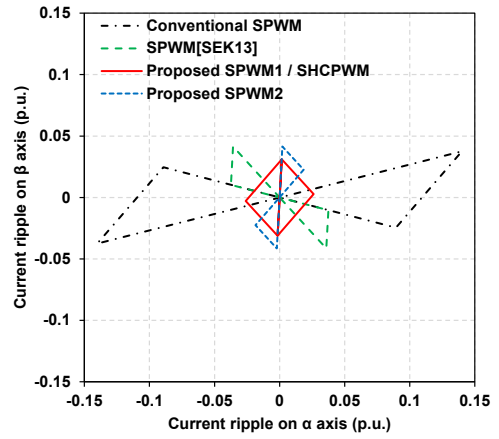
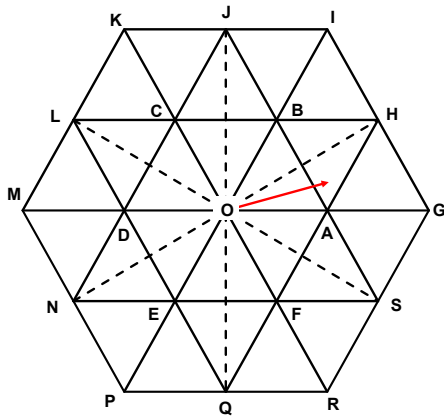


(b) proposed SPWM1 strategy.

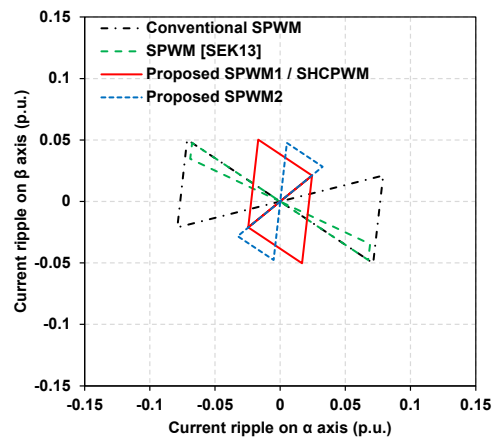
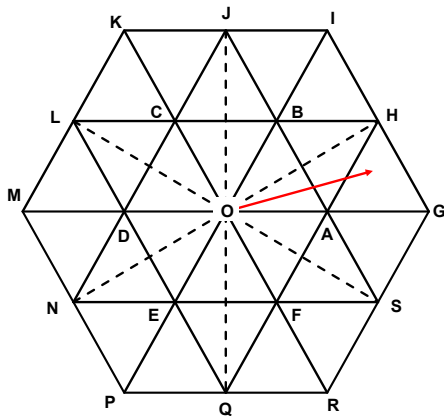
Fig. 2.9 PWM waveforms in sectors 1 and 2.



(a)  $MI=0.4, \theta = 15^\circ$ .



(b)  $MI=0.7, \theta = 15^\circ$ .



(c)  $MI=1.0, \theta = 15^\circ$ .

Fig. 2.10 Current ripple trajectories of proposed SPWM1, SPWM2, conventional SPWM, SPWM in [SEK13] and SHCPWM in  $\alpha\beta$  plane.

## 2.4 Simulation and Experiment Results

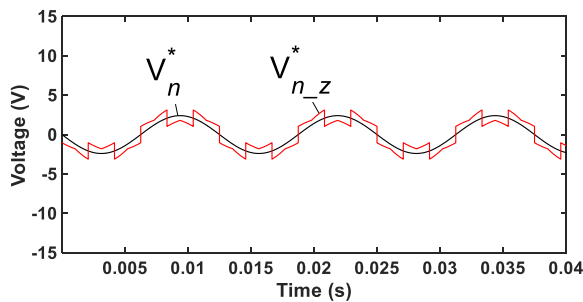
### 2.4.1 Simulation validation

The simulation model is built to control an OW PMSM in MATLAB/Simulink, and its parameters are shown in Table 2.2. The OW machine is driven by an isolated DC-bus dual two-level three-phase inverters. The DC-bus voltage is 12V.

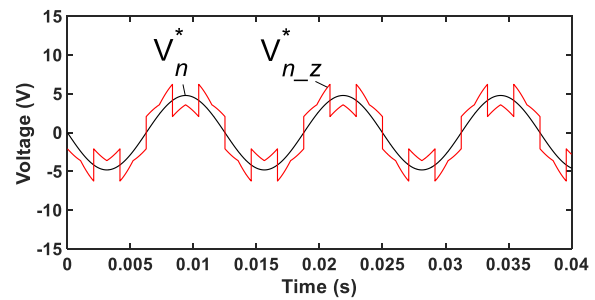
Table 2.2 Parameters of OW-PMSM

Pole pairs	5
Resistance( $\Omega$ )	0.8
No-load PM flux linkage (mWb)	12
$d$ - and $q$ -axis inductances (mH)	4
Rated current (A)	6
Rated voltage (V)	12
Rated power (W)	88.5

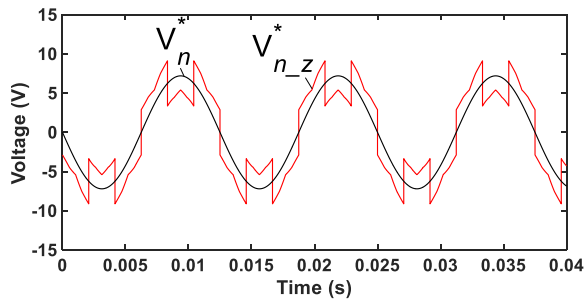
Figures 2.11 and 2.12 show the reference voltages of dual inverters before and after the new ZSV injection in different modulation indices for the proposed SPWM1 and SPWM2 strategies, respectively. The electrical frequency is 80Hz. It can be observed that the magnitude of reference voltages after the ZSV injection is  $V_{dc}$  when the modulation index reaches 1.15 in both proposed SPWM1 and SPWM2 strategies. As a result, the proposed SPWM strategies can achieve the same maximum voltage utilization as the conventional SVPWM strategy, but the implementation is much easier as neither sectors nor vector action time durations need to be calculated.



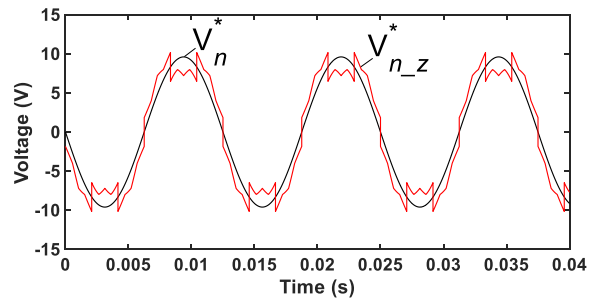
(a) MI = 0.2.



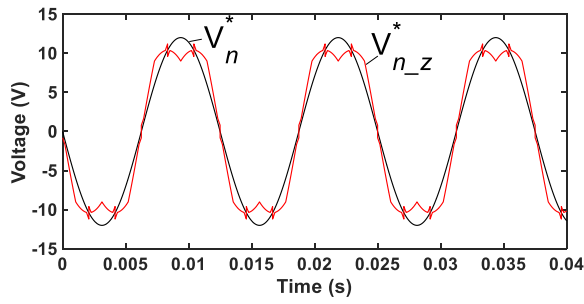
(b) MI = 0.4.



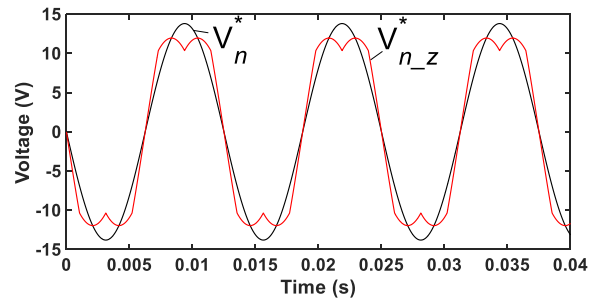
(c) MI = 0.6.



(d) MI = 0.8.

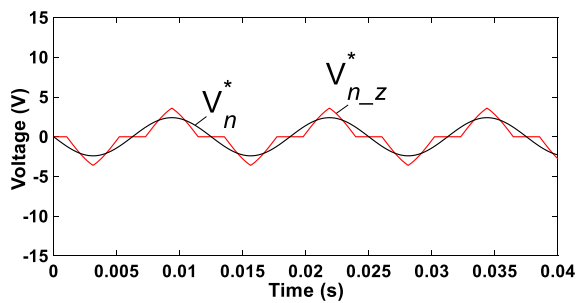


(e) MI = 1.0.

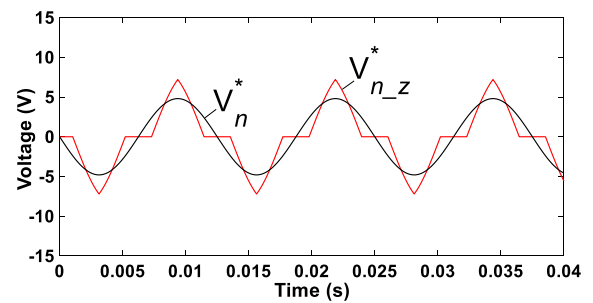


(f) MI = 1.15.

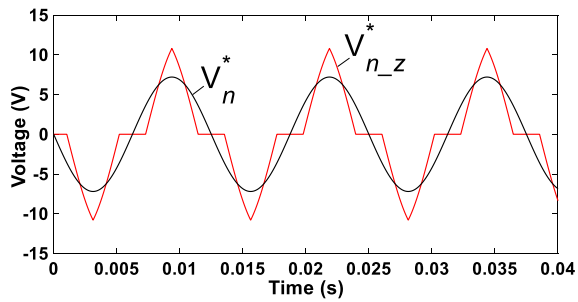
Fig. 2.11 Reference voltages of dual inverters before and after the new ZSV injection with different modulation indices in the proposed SPWM1.



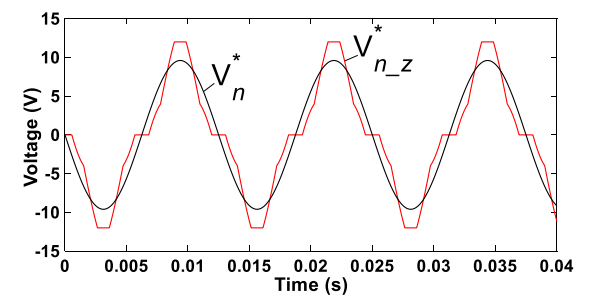
(a) MI = 0.2.



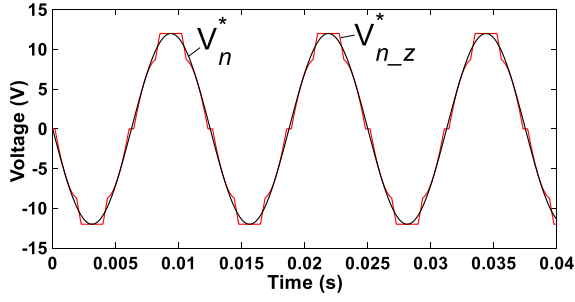
(b) MI = 0.4.



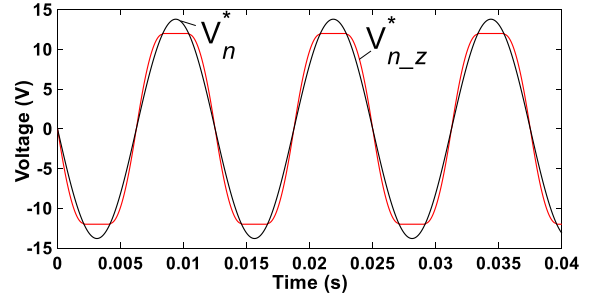
(c) MI = 0.6.



(d) MI = 0.8.



(e) MI = 1.0.



(f) MI = 1.15.

Fig. 2.12 Reference voltages of dual inverters before and after the new ZSV injection with different modulation indices in the proposed SPWM2.

PWM waveforms and three phase voltages of the conventional and proposed SPWM strategies are shown in Fig. 2.13. It can be observed that the conventional SPWM strategy is a continuous PWM strategy, while the proposed SPWM strategies are discontinuous PWM strategies. Compared with the conventional SPWM strategy, only half switches are switched and other switches are clamped over every 60 electrical degrees in the SPWM1 strategy. In the conventional and proposed SPWM1 strategies, outlines of PWM waveforms are the same in low and high modulation regions, but they are different in the proposed SPWM2 strategy. However, two of six switches are switched and other switches are clamped over every 60 electrical degrees in SPWM2 in whole modulation regions. Moreover, the operation of two inverters is balanced in both proposed SPWM strategies. From three phase voltages in Fig. 2.13, the proposed SPWMs have less harmonics compared with the conventional SPWM.

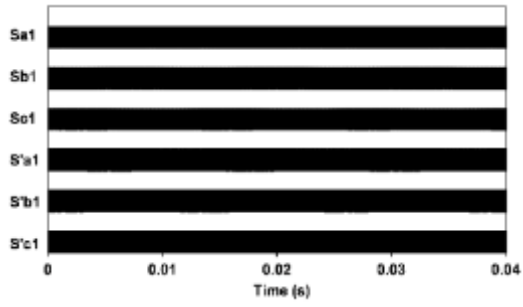
It should be noted that the relationships between the PWM frequency and switching frequency are different in continuous and discontinuous PWM strategies. The PWM frequency is the frequency of carrier signal, while the switching frequency is determined by actions of switching devices and should be evaluated within an electrical cycle in average sense in discontinuous PWM strategies. As a result, the average switching frequencies of the proposed SPWM strategies are less than that of the conventional SPWM strategy, when the three SPWM strategies have the same PWM frequency.

To evaluate the influence of PWM strategy on current harmonics, the total harmonics of phase currents are defined as

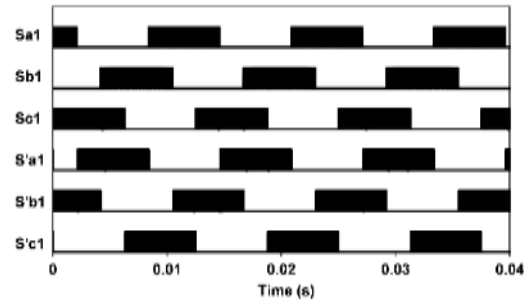
$$\text{Total harmonics} = \sqrt{\sum_{n=1,2,3,\dots}^{\infty} (I_n)^2} \quad (2.11)$$

where  $I_n$  is the magnitudes of current harmonics at the multiples of PWM frequency.

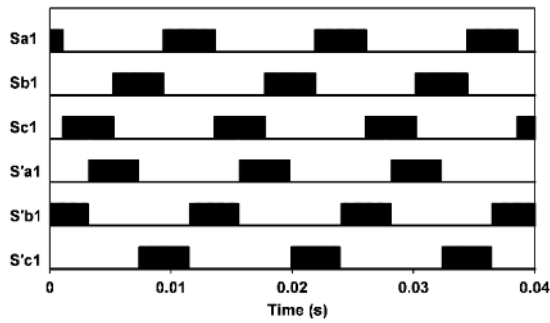




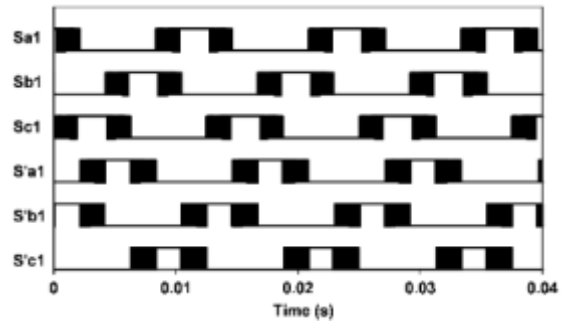
(a) Conventional SPWM.



(b) Proposed SPWM1.



(c) Proposed SPWM2 (MI = 0.4).



(d) Proposed SPWM2 (MI = 1.15).

Fig. 2.13 PWM waveforms and three phase voltages.

Simulated three phase currents and spectra of the conventional SPWM strategy with different modulation indices are shown in Figs. 2.14 (a), (b), (c), while Figs. 2.15 (a), (b), (c) and Figs. 2.16 (a), (b), (c) show simulated three phase currents and spectra of proposed SPWM1 and SPWM2 strategies with different modulation indices. Simulated total current harmonics of the conventional and proposed SPWM strategies with different PWM frequencies are shown in

Fig. 2.17. Due to the different switching actions in a PWM cycle for the three PWM strategies, the switching loss will be different if they have the same PWM frequency. To compare the proposed and conventional SPWM strategies with the same average switching frequency and switching loss, their PWM frequencies should be set differently. The PWM frequencies are 5kHz, 10kHz and 15kHz for the conventional SPWM, proposed SPWM1 and SPWM2, respectively. For the conventional SPWM, the voltage vectors on the small hexagon are not used, so that the maximum current harmonics appear at the modulation index of 0.6 in Fig. 2.17 when the reference voltage vector is close to the small hexagon. Compared with the conventional SPWM, both the proposed SPWM1 and SPWM2 strategies have much lower current harmonics over whole modulation regions. Further, the proposed SPWM1 strategy has similar total current harmonics as the proposed SPWM2 strategy in low and high modulation regions, and has lower current ripples in middle modulation regions. Simulated results are consistent with the results of current ripple trajectory analysis in Section 2.3.

The proposed SPWM1 and SPWM2 are also compared with the conventional SPWM with the same PWM frequency ( $f_{PWM} = 10\text{kHz}$ ) in Fig. 2.17. It can be observed that current harmonics of the proposed SPWM1 strategy are lower in most modulation regions, although they are similar in low modulation region and slightly higher in high modulation region, compared with those of the conventional SPWM strategy. The proposed SPWM2 strategy generates higher current harmonics in low and high modulation regions, and lower current harmonics in middle modulation region, compared with the conventional SPWM strategy. Besides, current harmonics of the proposed SPWM1 strategy are lower than those of the proposed SPWM2 strategy over whole modulation regions. However, it needs to note that the average switching frequency and switching loss for the three SPWM strategies are different. The proposed SPWM1 and SPWM2 strategies have only half and one third average switching frequency and switching loss, respectively, compared with the conventional SPWM strategy.

According to the switching loss analysis method in [JIA13], an electrical cycle is divided into  $N$  ( $N = \text{PWM frequency} / \text{electrical frequency}$ ) PWM cycles, and the total switching losses are the sum of the switching losses in all these PWM cycles. The switching loss of three phase dual two-level OW inverters in the  $k^{\text{th}}$  PWM cycle in one electrical cycle is proportional to the phase current  $|i_n(k)|$ . Assuming the unit switching loss of the switching leg is  $e_{\text{unit}}$  in a PWM cycle, which means the switching loss with unity output current for the leg. The unit switching loss of dual inverters  $e_{\text{inv}}$  varies according to the PWM strategies of the dual inverters, and can be expressed as

$$e_{inv} = \begin{cases} 6e_{unit} & \text{Conventional SPWM} \\ 3e_{unit} & \text{Proposed SPWM1} \\ 2e_{unit} & \text{Proposed SPWM2} \end{cases} \quad (2.12)$$

Assuming there are  $N$  PWM cycles in an electrical cycle when the PWM frequency is 10kHz. Consequently, when the PWM frequency is 5kHz and 15kHz, there are  $N/2$  and  $3N/2$  PWM cycles in an electrical cycle, respectively.

For the proposed SPWM1 strategy with 10kHz PWM frequency, half switches in the dual inverters are switched, and the switching loss can be expressed as

$$E_{sw\_SPWM1\_10kHz} = \sum_{k=1}^N |i_n(k)| e_{inv} = 3 \sum_{k=1}^N |i_n(k)| e_{unit} \quad (2.13)$$

For the conventional SPWM strategy with 5kHz or 10kHz PWM frequency, the switching loss can be expressed as

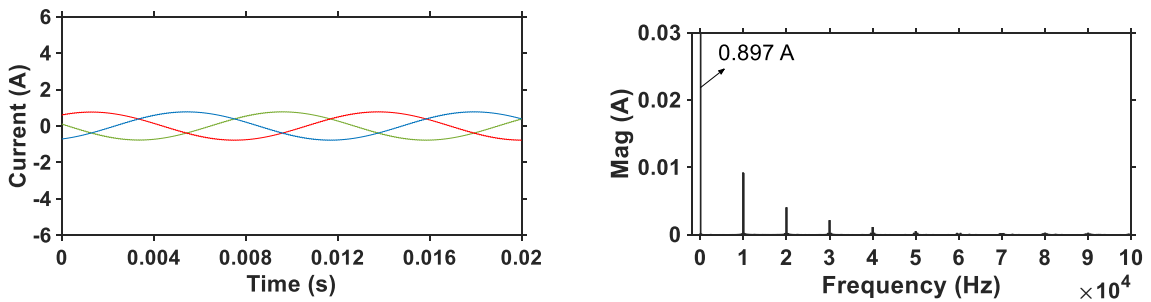
$$E_{sw\_CSPWM\_5kHz} = \sum_{k=1}^{N/2} |i_n(k)| 6e_{unit} = 3 \sum_{k=1}^N |i_n(k)| e_{unit} \quad (2.14)$$

$$E_{sw\_CSPWM\_10kHz} = 6 \sum_{k=1}^N |i_n(k)| e_{unit}$$

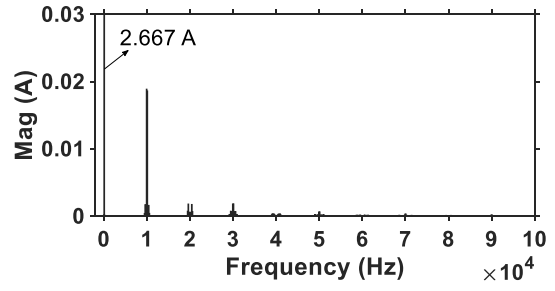
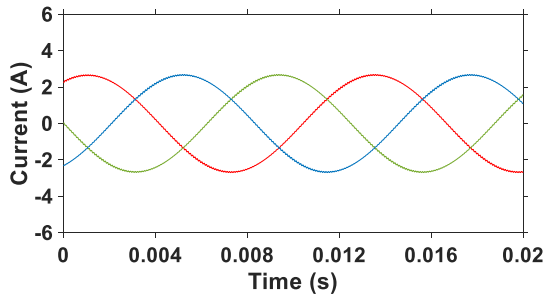
For the proposed SPWM2 strategy with 15kHz or 10kHz PWM frequency, the switching loss can be expressed as

$$E_{sw\_SPWM2\_15kHz} = \sum_{k=1}^{3N/2} |i_n(k)| 2e_{unit} = 3 \sum_{k=1}^N |i_n(k)| e_{unit} \quad (2.15)$$

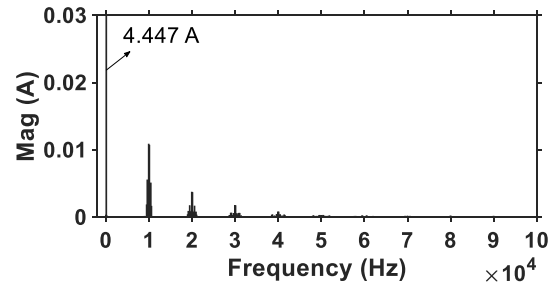
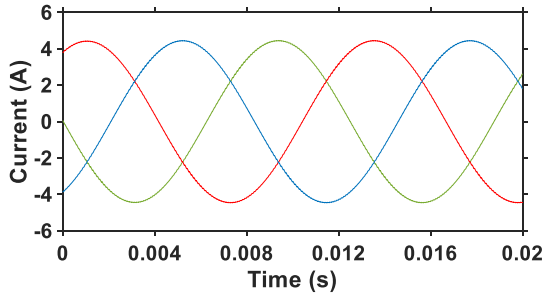
$$E_{sw\_SPWM2\_10kHz} = 2 \sum_{k=1}^N |i_n(k)| e_{unit}$$



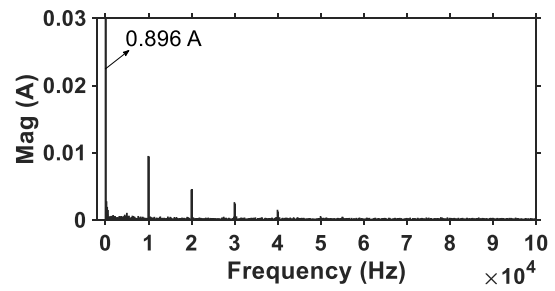
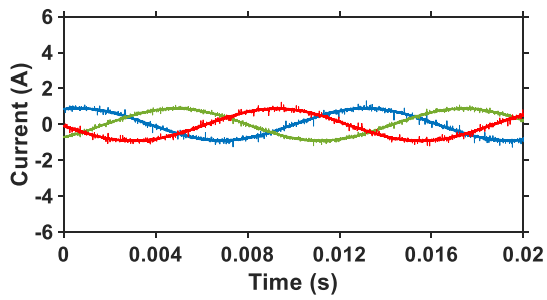
(a) MI=0.2 (simulated).



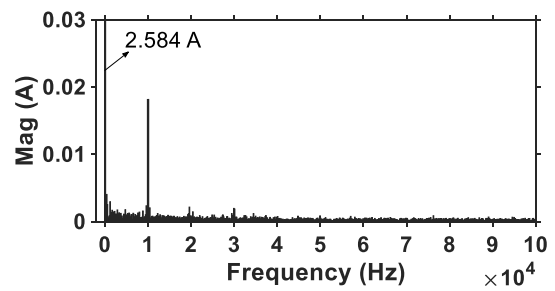
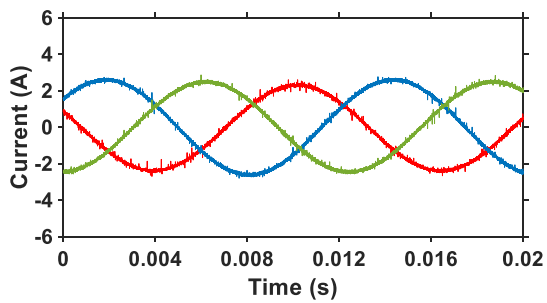
(b) MI=0.6(simulated).



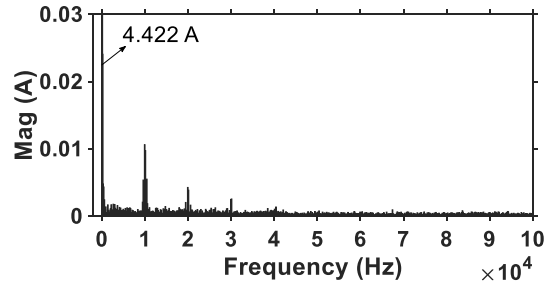
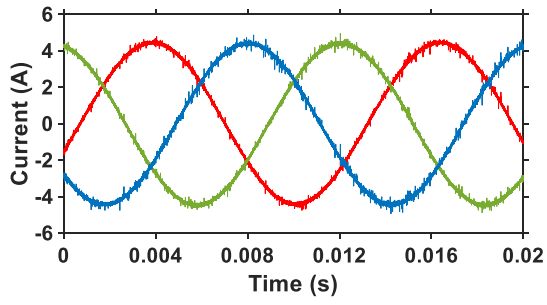
(c) MI=1.0 (simulated).



(d) MI=0.2(measured).

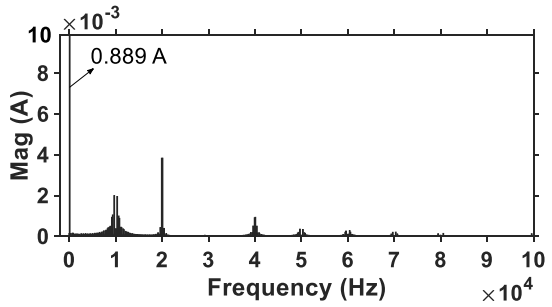
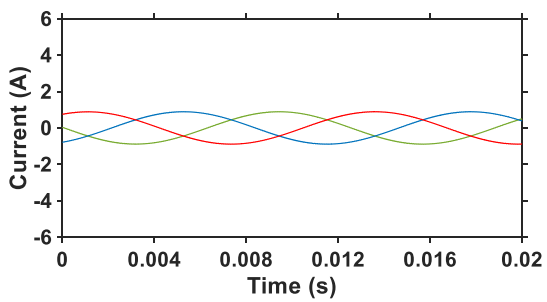


(e) MI=0.6(measured).

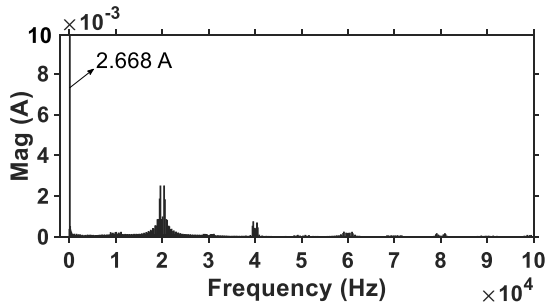
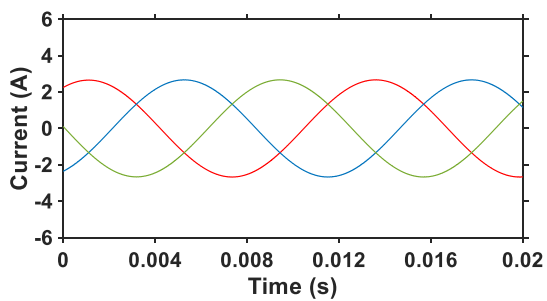


(f) MI=1.0 (measured).

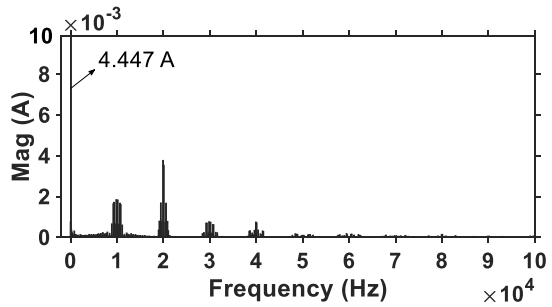
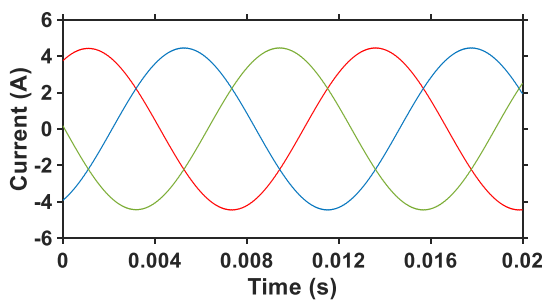
Fig. 2.14 Waveforms and spectra of phase current with different modulation indices in the conventional SPWM strategy ( $f_{PWM} = 5\text{kHz}$ ).



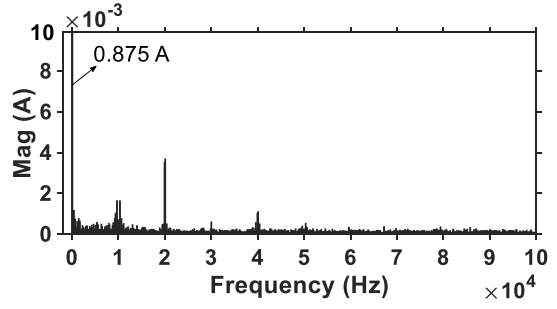
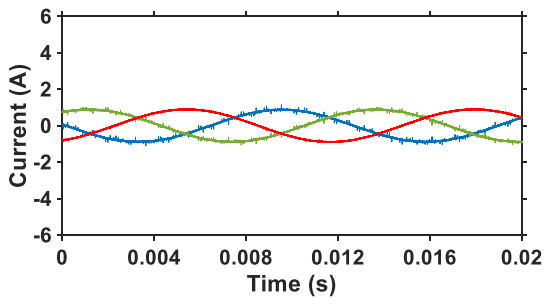
(a) MI=0.2 (simulated).



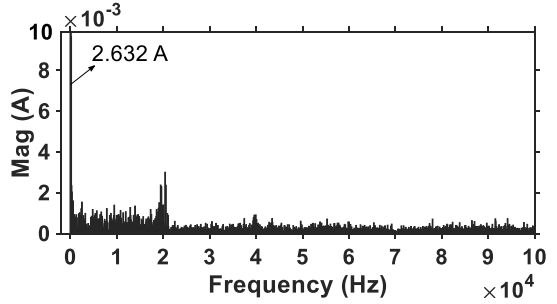
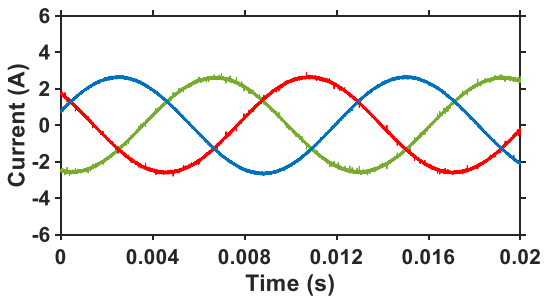
(b) MI=0.6(simulated).



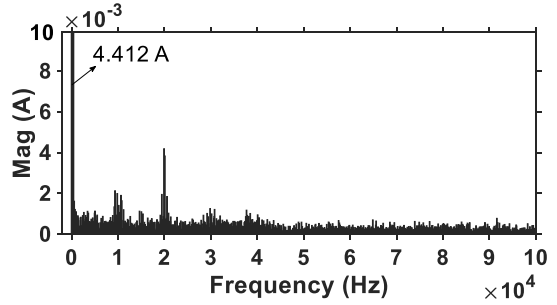
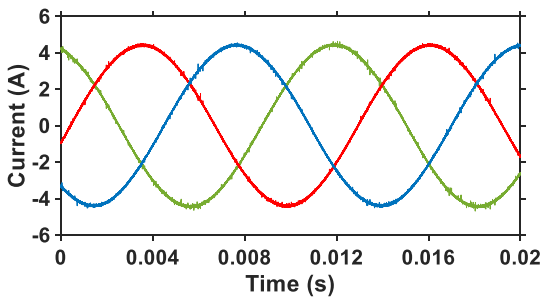
(c) MI=1.0 (simulated).



(d) MI=0.2(measured).

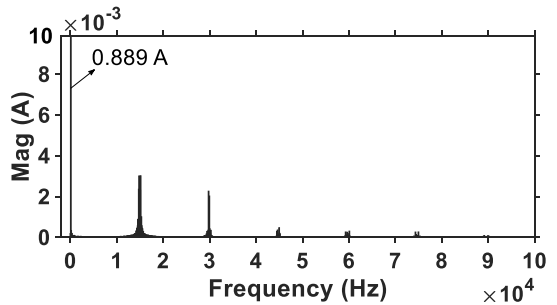
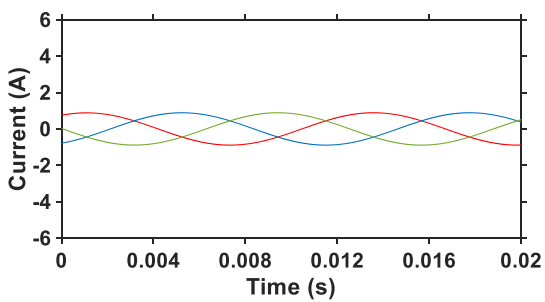


(e) MI=0.6(measured).

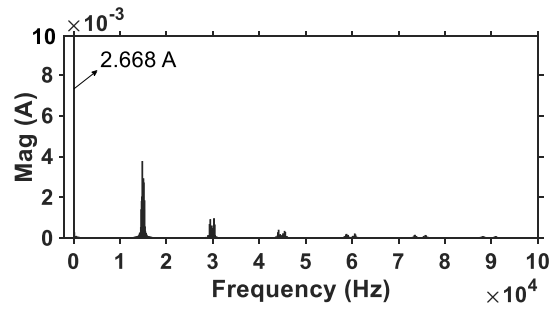
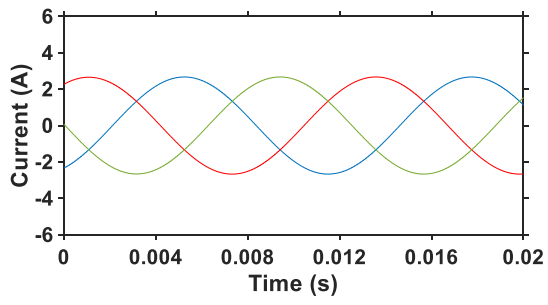


(f) MI=1.0 (measured).

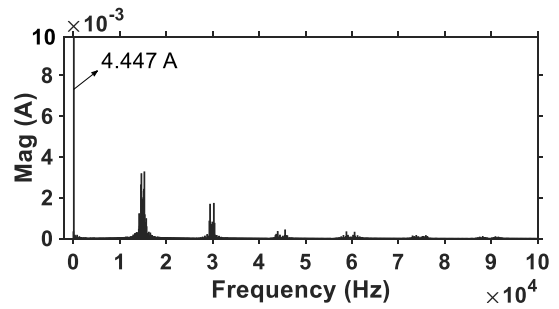
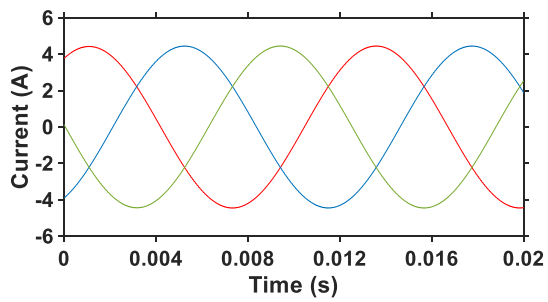
Fig. 2.15 Waveforms and spectra of phase current with different modulation indices in the proposed SPWM1 strategy ( $f_{PWM} = 10\text{kHz}$ ).



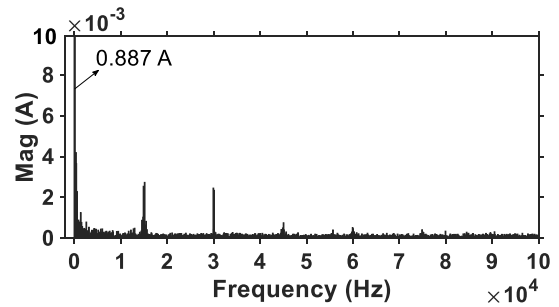
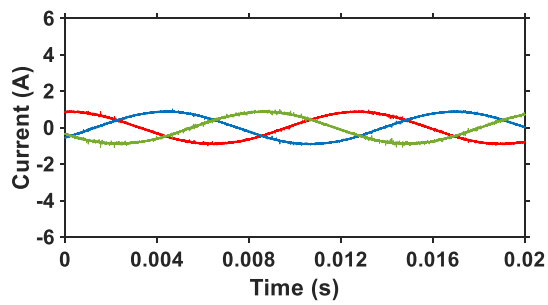
(a) MI=0.2 (simulated).



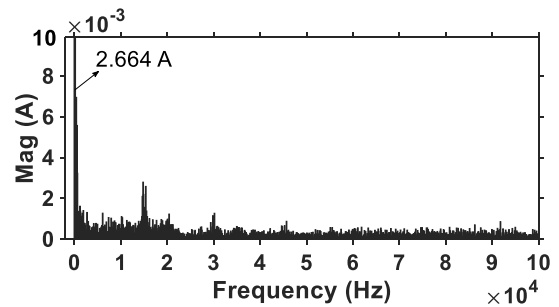
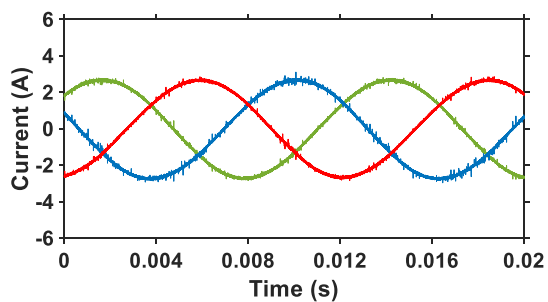
(b) MI=0.6(simulated).



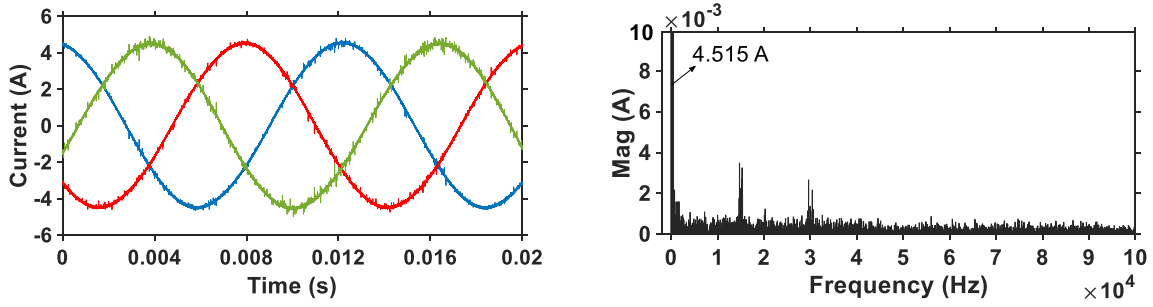
(c) MI=1.0 (simulated).



(d) MI=0.2(measured).



(e) MI=0.6(measured).



(f) MI=1.0 (measured).

Fig. 2.16 Waveforms and spectra of phase current with different modulation indices in the proposed SPWM2 strategy ( $f_{PWM} = 15\text{kHz}$ ).

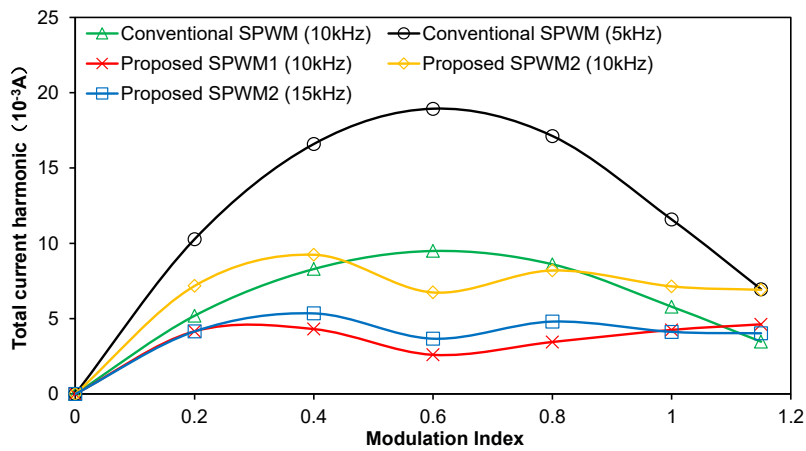


Fig. 2.17 Simulated total current harmonics of proposed SPWM1 ( $f_{PWM} = 10\text{kHz}$ ), SPWM2 ( $f_{PWM} = 10\text{kHz}$ ,  $15\text{kHz}$ ) and conventional SPWM ( $f_{PWM} = 10\text{kHz}$ ,  $5\text{kHz}$ ) strategies.

Shunt sensing technology is widely used in many applications due to its good performance in cost-effectiveness and system integration [ZHA17c] [CHO13]. Generally, two or three shunts on the lower arms are used for the sensing technology, and phase currents should be sampled during zero vector. As a result, the duration of zero vector should be longer enough for current sampling, and the voltage utilization is limited. In [ZHA17c], a constant time  $T_{\min}$  is defined to represent the minimum pulse width required for reliable current detection, and the maximum modulation region of a Y-connection three phase machine fed by a two-level inverter is analysed. To increase the voltage utilization, a 5-segment PWM strategy is often used as the larger modulation region, compared with a 7-segment PWM strategy [CHO13]. The shunt sensing technology can also be used in the OW machine drive. Fig. 2.18 show the modulation regions of OW machine fed by dual two-level inverters when the conventional SPWM and two proposed SPWM strategies are applied, while the PWM cycle is  $100\mu\text{s}$  and the constant time  $T_{\min}$  is  $4\mu\text{s}$ . It can be observed that both proposed SPWM strategies have larger voltage utilization, compared with the conventional SPWM strategy. The proposed SPWM2 strategy



is a 5-segment PWM strategy, and the advantage of 5-segment PWM of a two-level inverter also exists in an OW machine fed by dual two-level inverters. Although the proposed SPWM2 strategy shows almost no advantage in current harmonics compared with the proposed SPWM1 strategy, the proposed SPWM2 strategy has larger voltage utilization.

This shunt sensing technology can be applied for the SPWM strategy in [SEK13], which has the same voltage utilization as the proposed SPWM1, but has lower voltage utilization compared with the proposed SPWM2. On the other hand, for the SHCPWM strategy with the alternating clamping of two inverters, the shunt sensing technology cannot be applied since there is no zero vector in one inverter during clamping state.

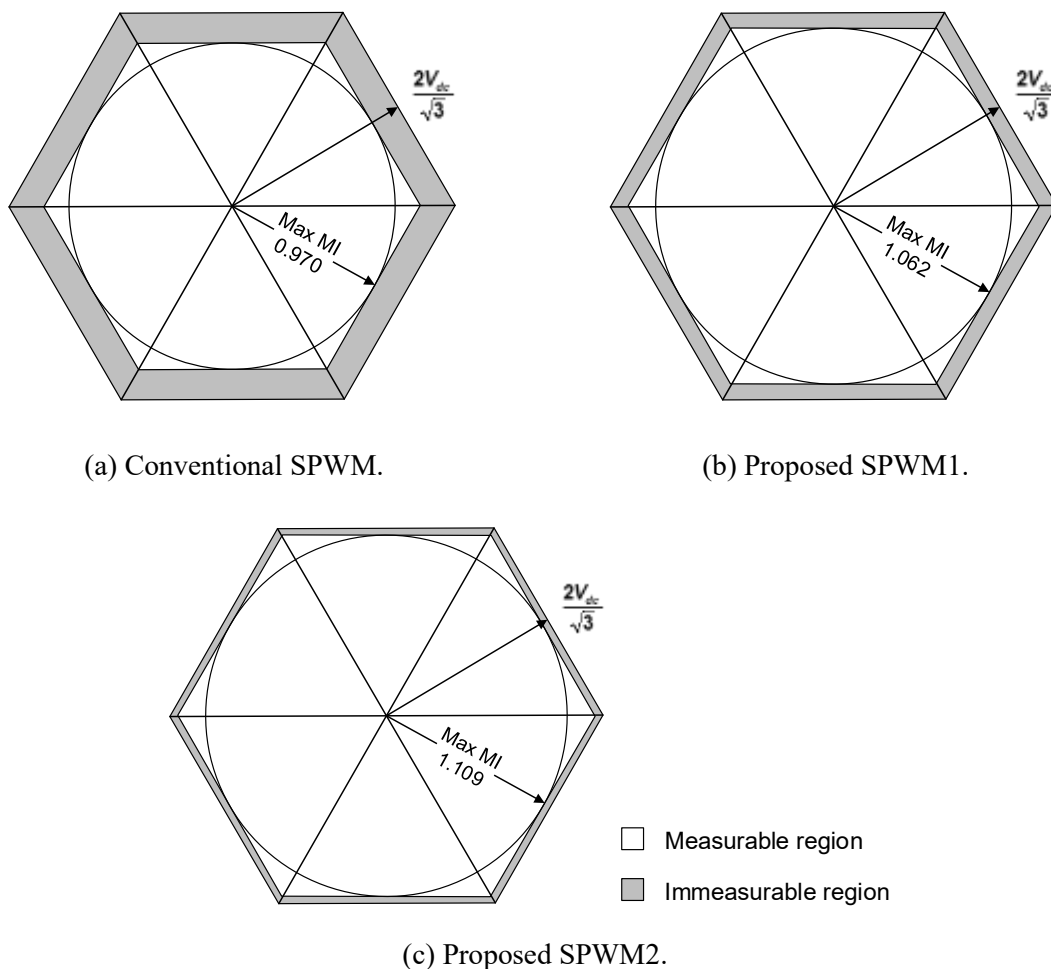


Fig. 2.18 Modulation region ( $T_{PWM} = 100\mu s$ ,  $T_{min} = 4\mu s$ ).

## 2.4.2 Experimental validation

The proposed SPWM strategies are validated in an OW-PMSM and implemented using an STM32F303 based MCU control board. The power switches of the inverter are IRFH7440 MOSFET. The parameters of the prototype machine are shown in Table 2.2. The OW machine

is driven by dual two-level inverters with two isolated DC-sources. The dead-time is set to  $2\mu\text{s}$ . The DC-bus voltage is 12V. Fig. 2.19 shows the experiment platform including an MCU control board, dual two-level inverters, an OW-PMSM, a load machine, and a position sensor.

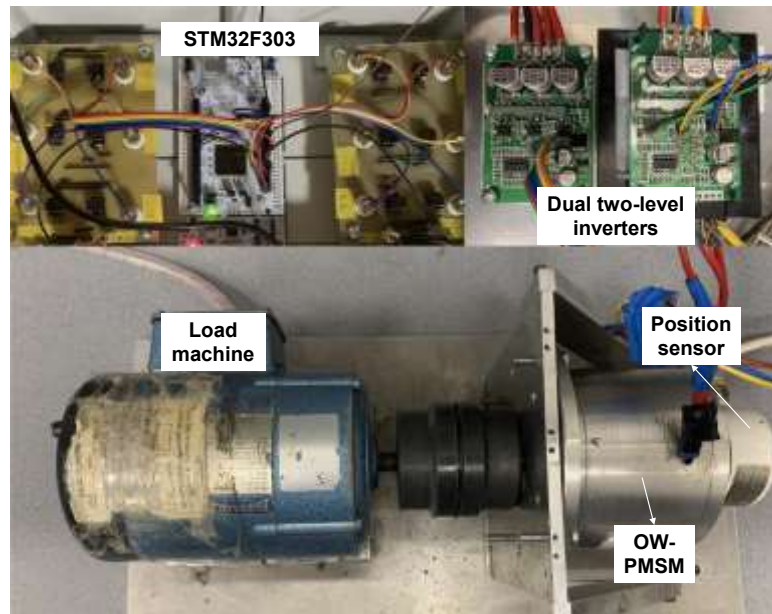


Fig. 2.19 Experiment platform.

Measured three phase currents, which are sampled by a high-resolution oscilloscope, and spectra of the conventional SPWM strategy with different modulation indices are shown in Figs. 2.14 (d), (e), (f), while Figs. 2.15 (d), (e), (f) and Figs. 2.16 (d), (e), (f) show measured three phase currents and spectra of the proposed SPWM1 and SPWM2 strategies with different modulation indices, respectively. Although extra harmonics exist in the measured spectra, the harmonics at multiples of the PWM frequency are similar to simulated results. Measured total current harmonics of the conventional and proposed SPWM strategies with different PWM frequencies are compared in different modulation indices in Fig. 2.20, and they are consistent with simulated results in Fig. 2.17.

With the same switching loss, both proposed SPWM1 and SPWM2 strategies show much better harmonic characteristics compared with the conventional SPWM strategy. The proposed SPWM1 strategy shows slightly lower current harmonics in the middle modulation region, and slightly higher current harmonics in the high modulation region, compared with the proposed SPWM2 strategy. With the same switching loss, the maximum total current harmonic magnitudes are  $18.47e^{-3}\text{A}$ ,  $4.51e^{-3}\text{A}$ , and  $5.22e^{-3}\text{A}$  for the conventional SPWM, proposed SPWM1 and SPWM2, respectively. Figure. 2.20 also compares the total current harmonics of the three SPWM strategies with the same PWM frequency. The proposed SPWM1 strategy has

lower harmonic characteristics and only half switching loss, compared with the conventional SPWM strategy. The proposed SPWM2 strategy has similar harmonic characteristics and one third switching loss, compared with the conventional SPWM strategy. With the same PWM frequency, the maximum total current harmonic magnitudes are  $9.46e^{-3}A$ ,  $4.51e^{-3}A$ , and  $7.59e^{-3}A$  for the conventional SPWM, proposed SPWM1 and SPWM2, respectively.

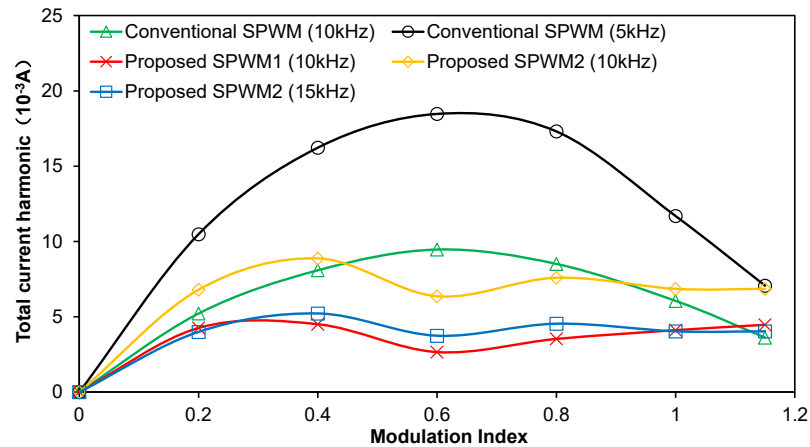


Fig. 2.20 Measured total current harmonics of proposed SPWM1 ( $f_{PWM} = 10kHz$ ), SPWM2 ( $f_{PWM} = 10kHz, 15kHz$ ) and conventional SPWM ( $f_{PWM} = 10kHz, 5kHz$ ) strategies.

The total current harmonics of the proposed SPWM1, SPWM2, SPWM in [SEK13] and SHCPWM strategies are compared in Fig. 2.21. The proposed SPWM1 strategy has the similar harmonic characteristics with the SHCPWM strategy. The SPWM in [SEK13] has similar current harmonics as the proposed SPWM2 strategy in low modulation regions, but has much larger current harmonics in high modulation regions. Results in Fig. 2.21 are consistent with the current ripple trajectory analysis in Fig. 2.10.

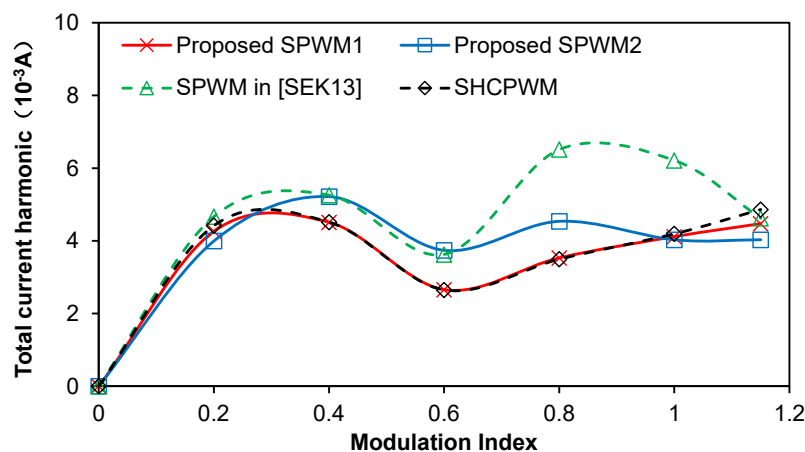


Fig. 2.21 Measured total current harmonics of proposed SPWM1 ( $f_{PWM} = 10kHz$ ), SPWM2 ( $f_{PWM} = 15kHz$ ), SPWM in [SEK13] ( $f_{PWM} = 7.5kHz$ ) and SHCPWM ( $f_{PWM} = 10kHz$ ) strategies.

A comprehensive comparison of conventional and proposed PWM strategies is shown in Table 2.3 and Table 2.4. The proposed SPWM strategies have low current harmonics and less switching actions in a PWM cycle compared with the SPWM in [SEK13] and conventional SPWM strategy. Moreover, compared with the SHCPWM strategy in [SRI13], the proposed SPWM strategies have advantages of easy implementation and less switching commutations with the same current harmonic characteristics.

Simulated and measured total current harmonics of the proposed SPWM strategies with different modulation indices are compared in Fig. 2.22, and they are almost identical. Due to the limitation of PWM duty cycles for current sampling in many applications, the proposed SPWM2 strategy has larger voltage utilization, compared with the proposed SPWM1 strategy, although the proposed SPWM2 strategy has higher current harmonics in the middle modulation region. As a result, the proposed SPWM2 strategy is more suitable for the high modulation region operation, while the proposed SPWM1 strategy is more suitable for the low and middle modulation region operation.

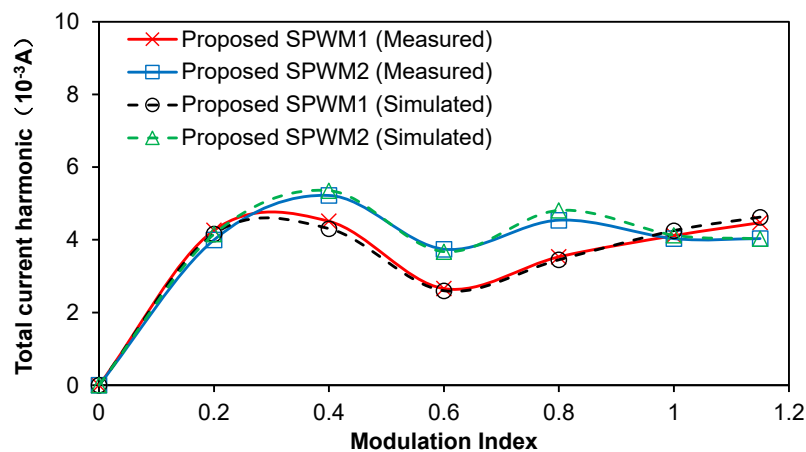


Fig. 2.22 Simulated and measured total current harmonics of proposed SPWM1 ( $f_{PWM} = 10\text{kHz}$ ) and SPWM2 ( $f_{PWM} = 15\text{kHz}$ ) strategies.

Table 2.3 Comparison of Conventional and Proposed PWMs with the Same Switching Loss

PWM strategy	PWM frequency (Hz)	Switching loss (p.u.*)	Switching commutations (in an electrical cycle)	Maximum harmonic magnitude ( $10^{-3}A$ )	Sector and vector duration calculation
Conventional SPWM	5k	1	0	18.47	No
SPWM in [SEK13]	7.5k	1	0	6.51	No
SHCPWM in [SRI13]	10k	1	12	4.51	Yes
Proposed SPWM1	10k	1	6	4.51	No
Proposed SPWM2	15k	1	6	5.22	No

Table 2.4 Comparison of Conventional and Proposed PWMs with the Same PWM Frequency

PWM strategy	PWM frequency (Hz)	Switching loss (p.u.)	Switching commutations (in an electrical cycle)	Maximum harmonic magnitude ( $10^{-3}A$ )	Sector and vector duration calculation
Conventional SPWM	10k	2	0	9.46	No
SPWM in [SEK13]	10k	4/3	0	4.88	No
SHCPWM in [SRI13]	10k	1	12	4.51	Yes
Proposed SPWM1	10k	1	6	4.51	No
Proposed SPWM2	10k	2/3	6	7.59	No

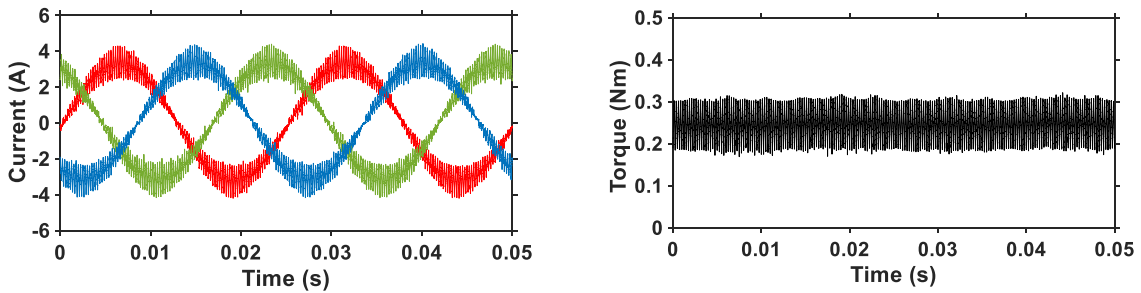
\*  $I_{pu}$  is the switching loss in (2.13)

The magnitudes of current harmonics caused by PWM strategies are affected by DC-bus voltage, electrical machine inductance, and PWM frequency. As a result, the high frequency current harmonics of the proposed SPWM strategy will be more obvious in high DC-bus voltage, smaller electrical machine inductance, and low PWM frequency applications. To evaluate the effect of PWM strategies on machine performance, new experiment parameters are shown in the Table 2.5.

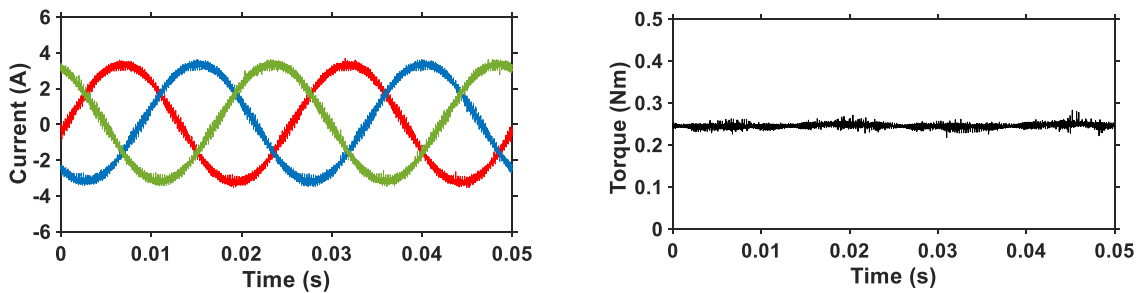
Table 2.5 Experiment Parameters

Pole pairs	10
Resistance( $\Omega$ )	1.2
No-load PM flux linkage (mWb)	10
$d$ - and $q$ -axis inductances (mH)	1.7
DC-bus voltage (V)	30
PWM frequency	2kHz (Conventional SPWM) 4kHz (Proposed SPWM1) 6kHz (Proposed SPWM2)

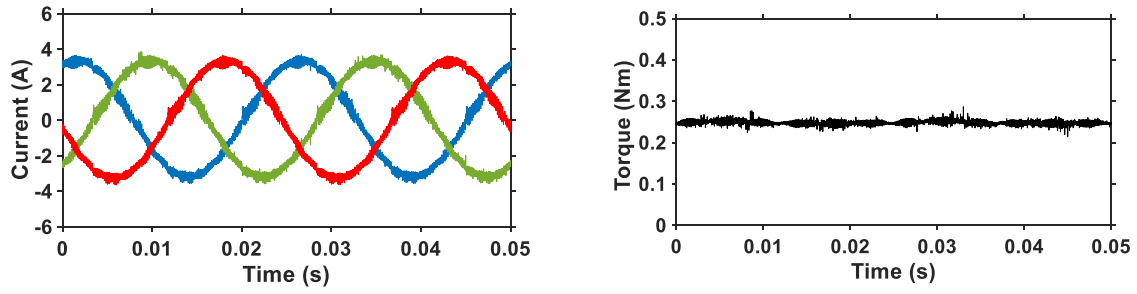
Torque of electrical machine can be estimated from the measured currents and machine parameters. Fig. 2.23 shows three phase currents and the estimated torque of three different SPWM strategies with the same switching loss, and the modulation index is approximately 0.6. It can be observed that the torque ripple can be significantly reduced in the two proposed SPWM strategies, compared with the conventional SPWM strategy.



(a) Conventional SPWM ( $T_{PWM} = 2\text{kHz}$ ).



(b) Proposed SPWM1 ( $T_{PWM} = 4\text{kHz}$ ).



(c) Proposed SPWM2 ( $T_{PWM} = 6\text{kHz}$ ).

Fig. 2.23 Three phase currents and estimated torque ( $V_{dc} = 30\text{V}$ ,  $L_d=L_q=1.7\text{mH}$ ).

## 2.5 Summary

In this chapter, two novel SPWM strategies are proposed with low switching frequency and low current harmonics for an OW machine fed by isolated DC-bus dual two-level inverters. Compared with the conventional continuous SPWM strategy, the proposed SPWM strategies are discontinuous PWM strategies. With the injection of two different ZSVs, the switching actions can be reduced by half and two third in a PWM cycle, respectively, compared with the conventional SPWM strategy. Moreover, in the proposed SPWM strategies, the reference voltage vector is always synthesized by three nearest vectors of dual inverters, and thus current harmonics can be reduced. With the same switching loss, the maximum total current harmonic magnitude of harmonic currents can be reduced over two third in the proposed SPWM strategies, compared with that in the conventional SPWM strategy. Compared with SHCPWM strategy, the proposed SPWM shows advantages of easy implementation and half switching commutation, without the degradation of current harmonic characteristics. Simulation and experiment results verify the performance of the proposed PWM strategies.

In this chapter, PWM strategies in isolated DC-bus dual two-level inverters with two identical DC-bus voltages are investigated, and the two voltage sources can also be configured with different voltages. In the next chapter, PWM strategies in isolated DC-bus dual two-level inverters with arbitrary DC-bus voltages will be investigated, and the current ripple prediction model will be combined with SPWM strategies to achieve the optimal current harmonic characteristic.

# **CHAPTER 3 A GENERALIZED SINUSOIDAL PWM STRATEGY FOR OPEN WINDING MACHINE WITH LOW CURRENT HARMONICS**

In Chapter 2, SPWM strategies with ZSV injection and voltage distribution are proposed to reduce switching frequency and PWM induced current harmonics for the isolated DC-bus OW drive with a 1:1 DC-bus voltage ratio. For an OW machine drive fed by two isolated voltage sources with arbitrary DC-bus voltage ratios, this chapter proposed a generalized OW sinusoidal pulse width modulation (OW-SPWM) with the optimal combination of ZSV injection and voltage distribution between two inverters. A current ripple prediction model of OW machine drive is developed and the PWM induced current ripples are predicted in each control cycle and subsequently used for determining the optimal combination of ZSV injection and voltage distribution methods. The proposed OW-SPWM can solve the conflict between the generalized modulation strategy and the optimal current harmonic characteristic in an OW drive with arbitrary DC-bus voltage ratios. It shows that for all DC-bus voltage ratios in dual inverters, the proposed OW-SPWM can generate significantly lower current harmonics than the conventional generalized space vector PWM, as confirmed by experiments.

This chapter has been submitted to IEEE Transactions on Energy Conversion and is currently under review.

## **3.1 Introduction**

Due to the error between the reference voltage and the instantaneous output voltage in the PWM control, current ripples are generated in three phase currents. The PWM strategy has a great influence on the performance of a voltage source inverter, and many existing PWM strategies for an OW machine fed by isolated DC-bus dual inverters have been described in Section 1.4.1. The PWM strategies for a fixed DC-bus voltage ratio are not suitable for the isolated DC-bus dual inverters with two variable DC-bus voltages. It is difficult to maintain a fixed DC-bus voltage ratio in many applications, such as batteries or AC voltage sources with



rectifiers. A generalized SVPWM strategy with a variable DC-bus voltage ratio is proposed in [CHE17] and optimized in [HUA19b] with low current harmonics in low modulation regions. However, there are abundant switching patterns for dual inverters with the same reference voltages, but these PWM strategies cannot choose the optimal switching pattern and thus the current harmonics could not be minimized.

SPWMs are proposed for an OW machine fed by dual inverters in Chapter 2, and reference voltages can be converted into switching signals with ZSV injection and voltage distribution methods. Compared with SVPWMs, SPWM strategies have the advantage of easy implementation due to the absence of sector selection and vector duration calculation. On the other hand, voltage vectors, vector durations, and vector action sequences are clearly shown in SVPWMs. However, the ratio between two DC-bus voltages of dual inverters is often not constant in some applications, such as electric vehicles [HUA19b]. Since the space vector plane changes with DC-bus voltage ratios, it is difficult to design a generalized SVPWM with the optimal current harmonic characteristic. This chapter will propose an OW-SPWM with the optimal combination of ZSV injection and voltage distribution between two inverters with arbitrary DC-bus voltage ratios for minimum current harmonics.

PWM induced phase current ripples [JIA14],  $dq$ -axis current ripples [YAN15], and DC-bus current ripples [LI18] can be predicted. In [YE20], the current ripples are reduced by optimizing the switching sequence of dual three-phase inverters via the prediction of current harmonics. In OW dual inverters, there are many switching patterns, which can be utilized for reducing current harmonics. In this chapter, various OW-SPWM switching patterns can be achieved by different combinations of ZSV injection and voltage distribution methods. Furthermore, current harmonic characteristics for different OW-SPWM switching patterns are predicted and the optimal switching pattern is selected for reducing current harmonics. The main contribution of this chapter is that the proposed OW-SPWM can solve the conflict between the generalized modulation strategy and the optimal current harmonic characteristic in an OW drive with arbitrary DC-bus voltage ratios.

### **3.2 Proposed PWM Strategy**

The control diagram of an OW machine drive with the proposed OW-SPWM strategy is shown in Fig. 3.1. Various switching patterns with different vectors and vector sequences in a PWM cycle are achieved by the proposed OW-SPWMs with different ZSV injection and voltage

distribution methods. A ZSV is injected into three phase reference voltages of dual inverters to increase the voltage utilization and reduce switching frequency. The voltage distribution module is used to distribute the reference voltages of dual inverters to each two-level inverter. All available ZSV injection and voltage distribution methods are enumerated, and the corresponding switching patterns are evaluated by the current ripple prediction model in the proposed OW-SPWM strategy. The optimal ZSV injection and voltage distribution methods can be acquired for the optimal switching pattern with the lowest high-frequency current harmonics. The proposed OW-SPWM is based on the 5-segment SPWM, which has the advantages of fewer switching actions in a PWM cycle and easy implementation. Typical 5-segment SPWM waveforms are shown in Fig. 3.2.

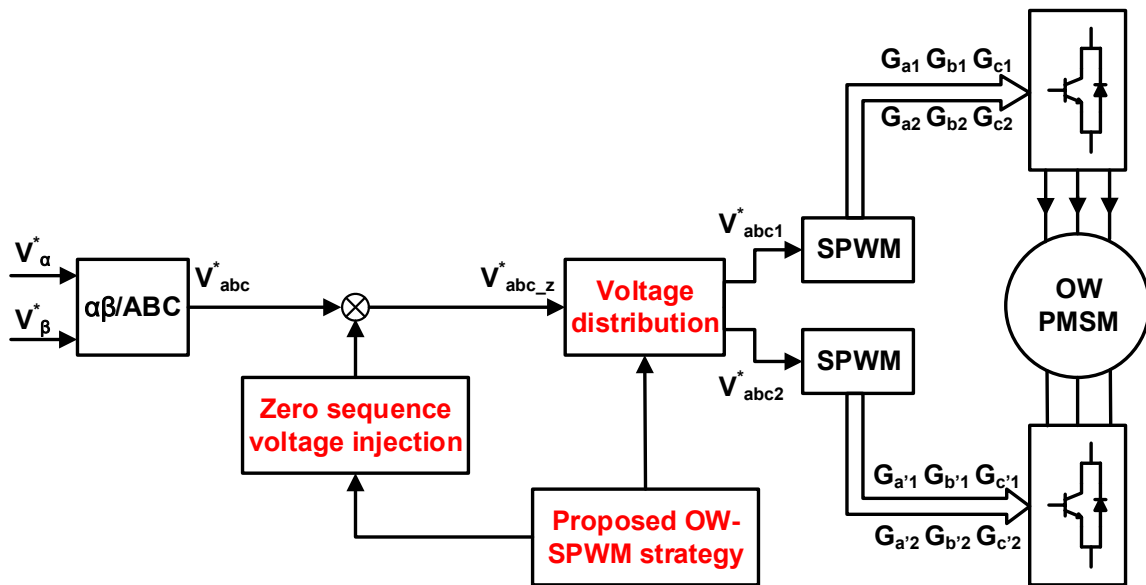


Fig. 3.1 Control diagram of an OW machine drive with the proposed OW-SPWM strategy.

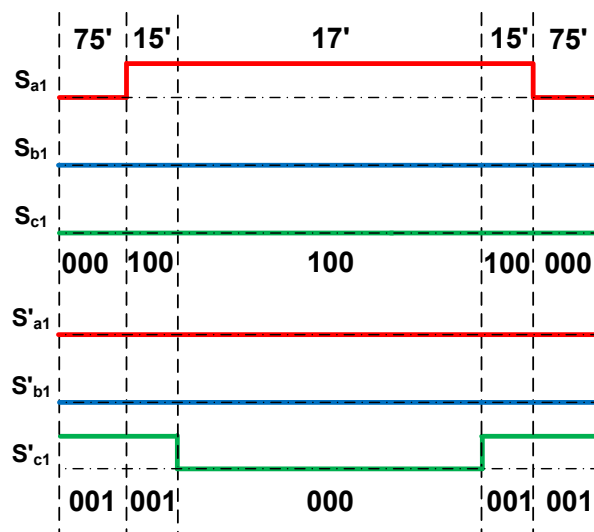


Fig. 3.2 Waveforms of a 5-segment SPWM.

### 3.2.1 Zero sequence voltage injection

In a dual two-level inverter fed OW machine, each phase is controlled by an H-bridge inverter. In a 5-segment PWM strategy, only two of six legs are switched, while the other legs are clamped. As a result, one of three H-bridges is clamped, so that the phase has a constant voltage in a PWM cycle, and the constant voltage can be  $V_{dc1}$ ,  $V_{dc1}-V_{dc2}$ , 0, or  $-V_{dc2}$  corresponding to four clamping states of the H-bridge. To achieve these constant voltages in a phase, ZSVs should be injected to reference voltages. When the maximum phase voltage is a constant value after the injection of a ZSV, the constant voltage cannot be  $-V_{dc2}$ , as the two other phase voltages exceed the limits of  $-V_{dc2}$  to  $V_{dc1}$ . Consequently, the constant value for the maximum phase voltage can be  $V_{dc1}$ ,  $V_{dc1}-V_{dc2}$  or 0. Similarly, the constant value for the middle phase voltage can be  $V_{dc1}-V_{dc2}$  or 0, and the constant value for the minimum phase voltage can be  $V_{dc1}-V_{dc2}$ , 0, or  $-V_{dc2}$ . In total, there are eight different ZSVs can be injected to reference voltages as shown in Table 3.1.  $V_{max}$ ,  $V_{mid}$ , and  $V_{min}$  are the maximum, middle, and minimum values of three phase reference voltages before the ZSV injection. After the ZSV injection, maximum, middle, and minimum values become  $V'_{max}$ ,  $V'_{mid}$ , and  $V'_{min}$ .

Taking  $V_{dc1} = 32\text{V}$ ,  $V_{dc2} = 16\text{V}$  as an example, the reference voltages before and after different ZSV injections in phase A are shown in Fig. 3.3 and Fig. 3.4, when the modulation indices (MI = reference voltage\*2/( $V_{dc1}+V_{dc2}$ )) are 0.2 and 1.15, respectively. It needs to note that reference voltages should be between  $-V_{dc2}$  and  $V_{dc1}$  after the injection of ZSV. It can be observed that all ZSV injections are available when the modulation index is 0.2, but only the first and second ZSV injections are always available when the modulation index is 1.15. As a result, if reference voltages after a ZSV injection exceed the range between  $-V_{dc2}$  and  $V_{dc1}$ , the ZSV injection method will be excluded from the enumeration in the proposed OW-SPWM.

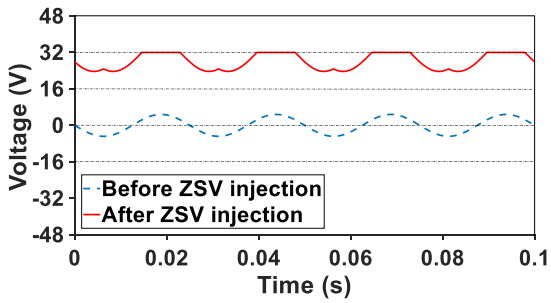
With the ZSV injection, the reference voltage in an arbitrary phase can be expressed as

$$V_{nz}^* = V_n^* + V_z \quad (n = A, B, C) \quad (3.1)$$

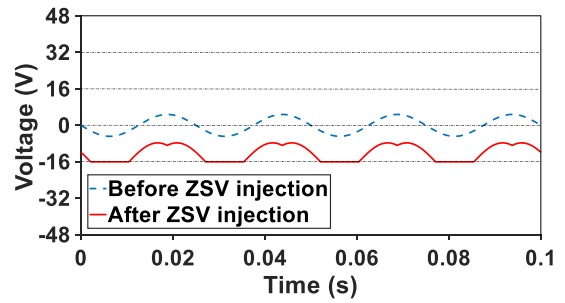
where  $V_z$  is the injected ZSV,  $V_n^*$  is the reference voltage before the ZSV injection,  $V_{nz}^*$  is the reference voltage after the ZSV injection.

Table 3.1 Zero Sequence Voltages

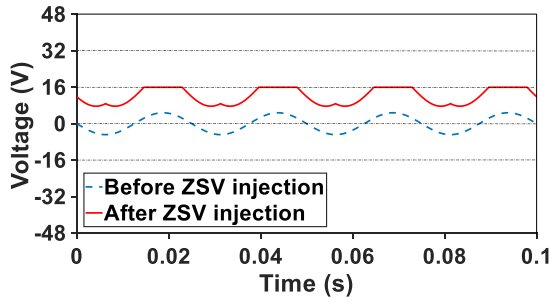
Ref. voltage ZSV	$V'_{max}$	$V'_{mid}$	$V'_{min}$
$V_{z1} = V_{dc1} - V_{max}$	$V_{dc1}$	$V_{mid} + V_{dc1} - V_{max}$	$V_{min} + V_{dc1} - V_{max}$
$V_{z2} = -V_{dc2} - V_{min}$	$V_{max} - V_{dc2} - V_{min}$	$V_{mid} - V_{dc2} - V_{min}$	$-V_{dc2}$
$V_{z3} = V_{dc1} - V_{dc2} - V_{max}$	$V_{dc1} - V_{dc2}$	$V_{mid} + V_{dc1} - V_{dc2} - V_{max}$	$V_{min} + V_{dc1} - V_{dc2} - V_{max}$
$V_{z4} = V_{dc1} - V_{dc2} - V_{mid}$	$V_{max} + V_{dc1} - V_{dc2} - V_{mid}$	$V_{dc1} - V_{dc2}$	$V_{min} + V_{dc1} - V_{dc2} - V_{mid}$
$V_{z5} = V_{dc1} - V_{dc2} - V_{min}$	$V_{max} + V_{dc1} - V_{dc2} - V_{min}$	$V_{mid} + V_{dc1} - V_{dc2} - V_{min}$	$V_{dc1} - V_{dc2}$
$V_{z6} = -V_{max}$	0	$V_{mid} - V_{max}$	$V_{min} - V_{max}$
$V_{z7} = -V_{mid}$	$V_{max} - V_{mid}$	0	$V_{min} - V_{mid}$
$V_{z8} = -V_{min}$	$V_{max} - V_{min}$	$V_{mid} - V_{min}$	0



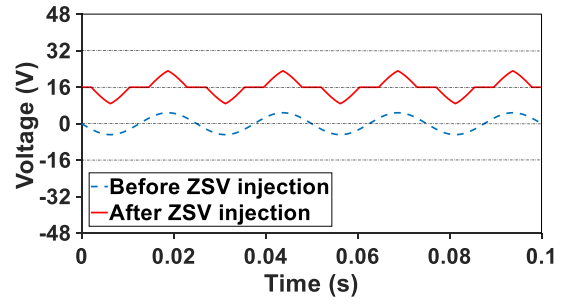
(a)  $V_{z1} = V_{dc1} - V_{max}$ .



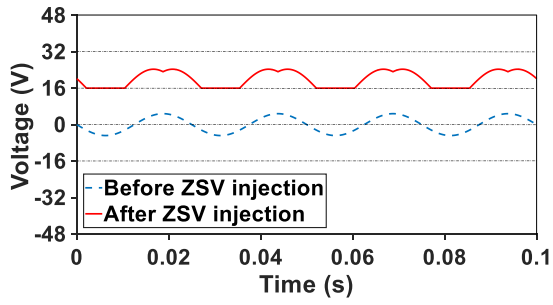
(b)  $V_{z2} = -V_{dc2} - V_{min}$ .



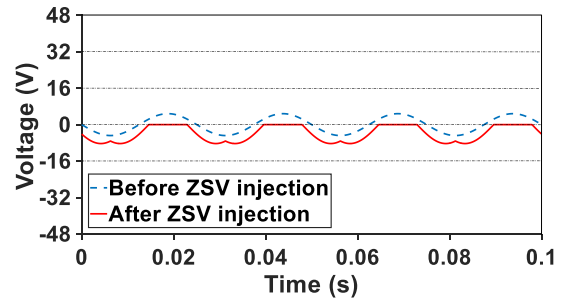
$$(c) V_{z3} = V_{dc1} - V_{dc2} - V_{max}.$$



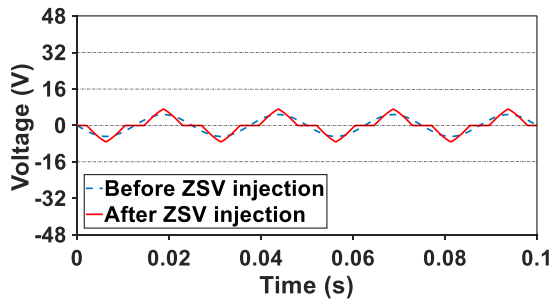
$$(d) V_{z4} = V_{dc1} - V_{dc2} - V_{mid}.$$



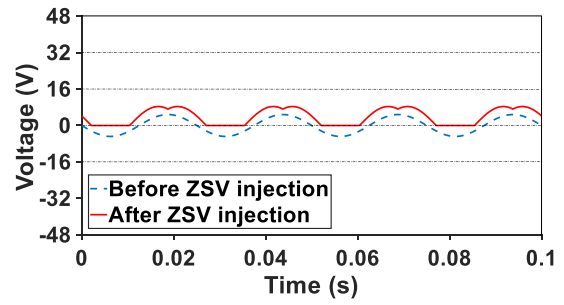
$$(e) V_{z5} = V_{dc1} - V_{dc2} - V_{min}.$$



$$(f) V_{z6} = -V_{max}.$$

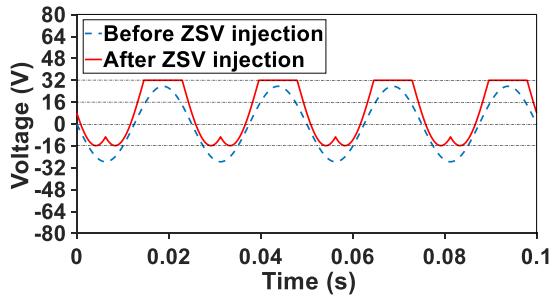


$$(g) V_{z7} = -V_{mid}.$$

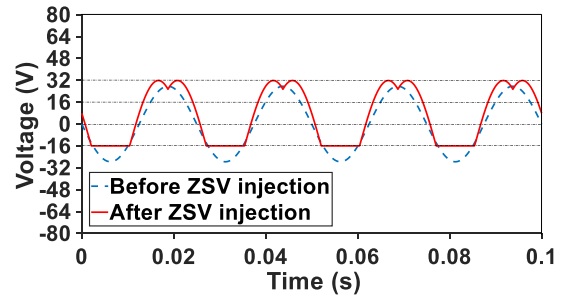


$$(h) V_{z8} = -V_{min}.$$

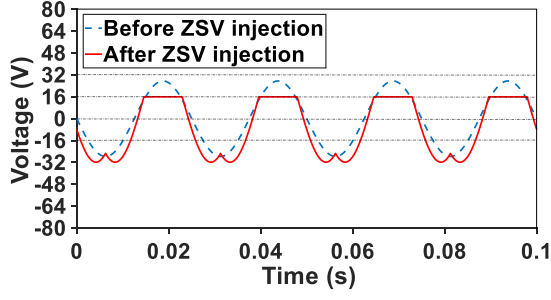
Fig. 3.3 Reference voltages before and after ZSV injection (MI = 0.2).



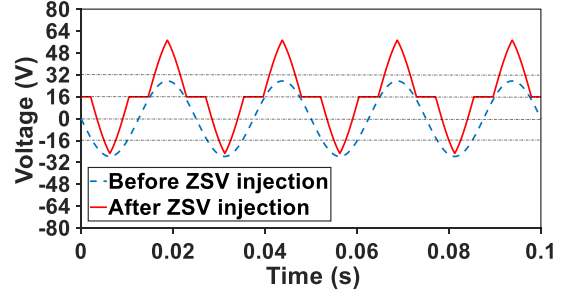
$$(a) V_{z1} = V_{dc1} - V_{max}.$$



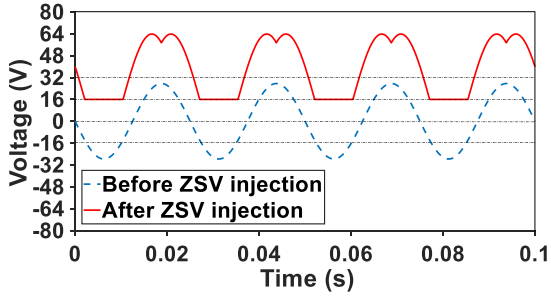
$$(b) V_{z2} = -V_{dc2} - V_{min}.$$



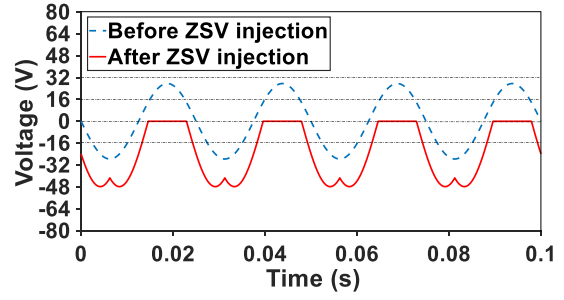
$$(c) V_{z3} = V_{dc1} - V_{dc2} - V_{max}.$$



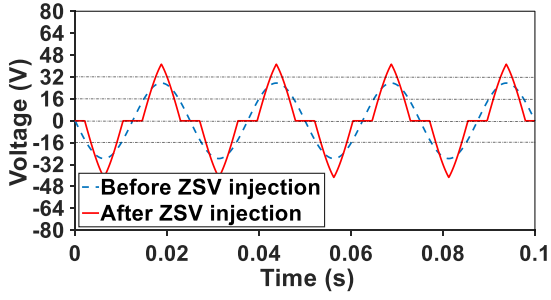
$$(d) V_{z4} = V_{dc1} - V_{dc2} - V_{mid}.$$



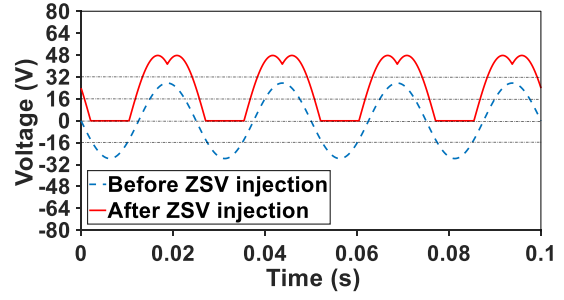
$$(e) V_{z5} = V_{dc1} - V_{dc2} - V_{min}.$$



$$(f) V_{z6} = -V_{max}.$$



$$(g) V_{z7} = -V_{mid}.$$



$$(h) V_{z8} = -V_{min}.$$

Fig. 3.4 Reference voltages before and after ZSV injection (MI = 1.15).

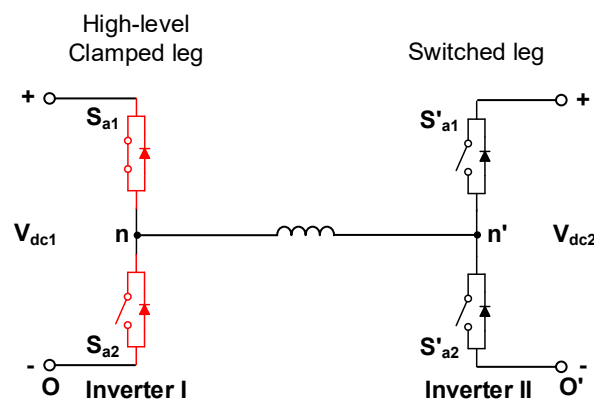
### 3.2.2 Voltage distribution method

In a 5-segment PWM strategy, only two of six legs are switched, while the other legs are clamped in three H-bridges of dual inverters. It needs to note that one leg is switched in an H-bridge at most, so that there are two switched H-bridges and a clamped H-bridge. One leg is switched and the other leg is clamped in the two switched H-bridges, while two legs are all clamped in the clamped H-bridge.

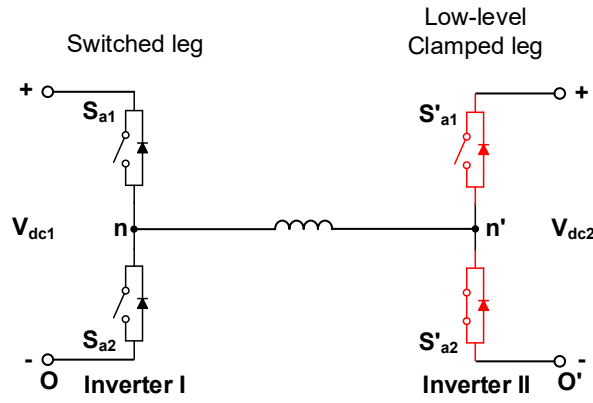
With the clamping of one of two legs, with or without carrier signal 180-degree phase shift, there are four different voltage distribution methods in the switched H-bridge as shown in Table

3.2. Taking the positive reference voltage as an example, firstly, the H-bridge leg in Inverter I cannot be clamped in low-level state, since the H-bridge can only generate a negative phase voltage in this case. Consequently, there are three clamping states, i.e. the H-bridge leg in Inverter I high-level clamping, in Inverter II low-level clamping, and in Inverter II high-level clamping as shown in Fig. 3.5. For Inverter II low-level clamping, with or without carrier signal 180-degree phase shift of Inverter I, voltage distribution methods are 1 and 2, respectively. For Inverters I and II high-level clamping, voltage distribution methods are 3 and 4, respectively. It needs to note that carrier signal 180-degree phase shift cannot be used since initial switching states in a PWM cycle for two legs of H-bridges cannot be both high-level, when considering the switching commutation issues which will be discussed in detail in Section 3.2.5. For the negative reference voltage, four voltage distribution methods can be acquired similarly.  $V_{no}$  and  $V_{n'o'}$  are the pole voltages of two legs in an H-bridge,  $V_n$  is the actual phase voltage ( $n = A, B, C$ ) in Table 3.2. In a 5-segment PWM strategy, one phase is clamped and two phases are switched, so that there are 16 voltage distribution methods for the two switched phases in dual inverters. Methods 1 and 2 are unconditional voltage distribution methods, while Methods 3 and 4 are conditional voltage distribution methods. Method 3 can only be used under the condition  $V_{nz}^* \geq V_{dc1} - V_{dc2}$ , and Method 4 can only be used under the condition  $V_n^* < V_{dc1} - V_{dc2}$ . If Method 3 or 4 cannot meet their application conditions, the voltage distribution method will be excluded from the enumeration in the proposed OW-SPWM.

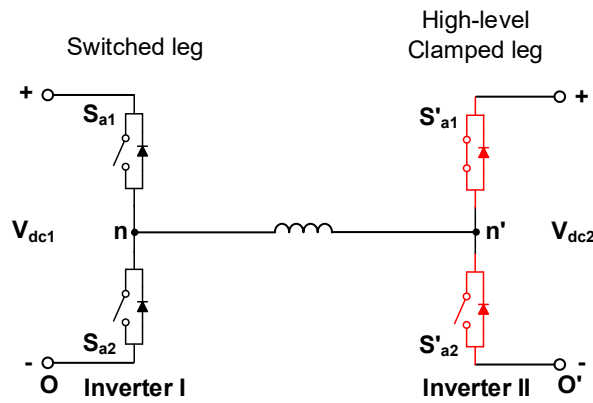
Various switching patterns in the proposed OW-SPWM are achieved by different ZSV injection and voltage distribution methods. ZSV injection methods determine which H-bridge is clamped and the clamping state, while voltage distribution methods determine the switching states of two switched H-bridges.



(a) The H-bridge leg in Inverter I high-level clamping.



(b) The H-bridge leg in Inverter II low-level clamping.



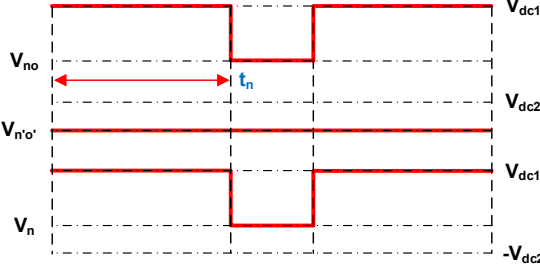
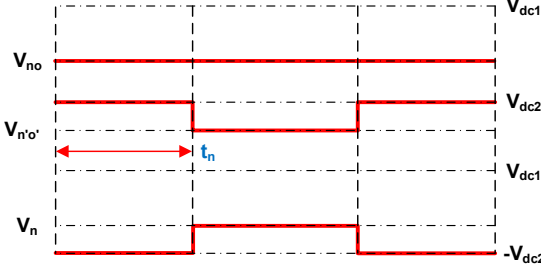
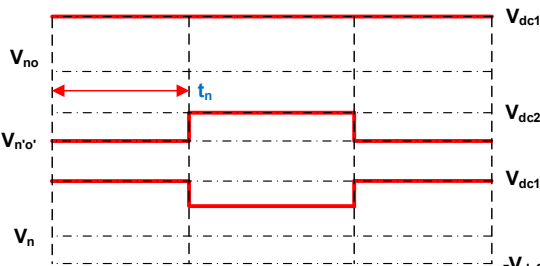

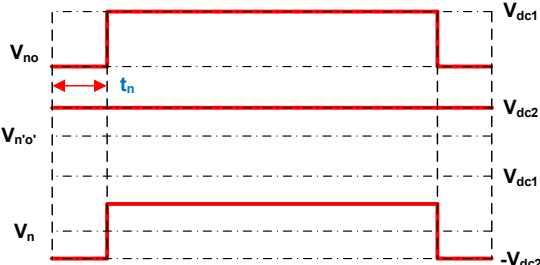
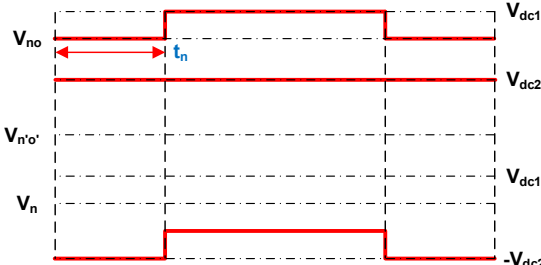
(c) The H-bridge leg in Inverter II high-level clamping.

Fig. 3.5 Clamping states of two legs in the switched H-bridge with the positive reference voltage.

Table 3.2 Voltage Distribution Methods, Turn-on Time, and Error Voltages

	$V_{nz}^* \geq 0$	$V_{nz}^* < 0$
1	$t_n = (T_{PWM} - T_{PWM} * V_{nz}^* / V_{dc1}) / 2$ $V_{en} = \begin{cases} -V_{nz}^* & \text{if } t < t_n \parallel t \geq (T_{PWM} - t_n) \\ V_{dc1} - V_{nz}^* & \text{if } t_n \leq t < (T_{PWM} - t_n) \end{cases}$	$t_n = (T_{PWM} + T_{PWM} * V_{nz}^* / V_{dc2}) / 2$ $V_{en} = \begin{cases} -V_{nz}^* & \text{if } t < t_n \parallel t \geq (T_{PWM} - t_n) \\ -V_{dc2} - V_{nz}^* & \text{if } t_n \leq t < (T_{PWM} - t_n) \end{cases}$



2	 $t_n = (T_{PWM} * V_{nz}^* / V_{dc1}) / 2$ $V_{en} = \begin{cases} V_{dc1} - V_{nz}^* & \text{if } t < t_n \parallel t \geq (T_{PWM} - t_n) \\ -V_{nz}^* & \text{if } t_n \leq t < (T_{PWM} - t_n) \end{cases}$	 $t_n = (-T_{PWM} * V_{nz}^* / V_{dc2}) / 2$ $V_{en} = \begin{cases} -V_{dc2} - V_{nz}^* & \text{if } t < t_n \parallel t \geq (T_{PWM} - t_n) \\ -V_{nz}^* & \text{if } t_n \leq t < (T_{PWM} - t_n) \end{cases}$
3	 $t_n = (T_{PWM} - T_{PWM} * (V_{dc1} - V_{nz}^*) / V_{dc2}) / 2$ $V_{en} = \begin{cases} V_{dc1} - V_{nz}^* & \text{if } t < t_n \parallel t \geq (T_{PWM} - t_n) \\ V_{dc1} - V_{dc2} - V_{nz}^* & \text{if } t_n \leq t < (T_{PWM} - t_n) \end{cases}$	 $t_n = (T_{PWM} - T_{PWM} * (V_{dc1} - V_{nz}^*) / V_{dc2}) / 2$ $V_{en} = \begin{cases} V_{dc1} - V_{nz}^* & \text{if } t < t_n \parallel t \geq (T_{PWM} - t_n) \\ V_{dc1} - V_{dc2} - V_{nz}^* & \text{if } t_n \leq t < (T_{PWM} - t_n) \end{cases}$
4	 $t_n = (T_{PWM} - T_{PWM} * (V_{nz}^* + V_{dc2}) / V_{dc1}) / 2$ $V_{en} = \begin{cases} -V_{dc2} - V_{nz}^* & \text{if } t < t_n \parallel t \geq (T_{PWM} - t_n) \\ V_{dc1} - V_{dc2} - V_{nz}^* & \text{if } t_n \leq t < (T_{PWM} - t_n) \end{cases}$	 $t_n = (T_{PWM} - T_{PWM} * (V_{nz}^* + V_{dc2}) / V_{dc1}) / 2$ $V_{en} = \begin{cases} -V_{dc2} - V_{nz}^* & \text{if } t < t_n \parallel t \geq (T_{PWM} - t_n) \\ V_{dc1} - V_{dc2} - V_{nz}^* & \text{if } t_n \leq t < (T_{PWM} - t_n) \end{cases}$

### 3.2.3 Current ripple prediction

The relationship between an arbitrary phase reference voltage after the ZSV injection and the pole voltages can be expressed as

$$V_{nz}^* = \frac{1}{T_{PWM}} \int_0^{T_{PWM}} (V_{nO} - V_{n'O'}) \cdot dt \quad (3.2)$$

The error voltage between the reference and actual output voltages can cause ripples in phase currents. The error voltage in an arbitrary phase can be expressed as

$$V_{en} = (V_{nO} - V_{n'O'}) - V_{nz}^* \quad (3.3)$$

Turn-on time  $t_n$  and error voltages  $V_{en}$  between reference and actual output voltages with different voltage distribution methods in a switched phase can be calculated in Table 3.2.

According to turn-on time and error voltages of switched phases, the vector, duration, and error voltages in each segment of the 5-segment PWM strategy can be acquired in Table 3.3. It needs to note that error voltages in the clamped phase are always zero.

Table 3.3 Vectors, Duration and Error Voltages of 5-segment PWM

Segment	1	2	3	4	5
Vector	<b>V1</b>	<b>V2</b>	<b>V3</b>	<b>V2</b>	<b>V1</b>
Duration	$t_1$	$t_2$	$t_3$	$t_4$	$t_5$
Three phase error voltages	$V_{eA1}$ $V_{eB1}$ $V_{eC1}$	$V_{eA2}$ $V_{eB2}$ $V_{eC2}$	$V_{eA3}$ $V_{eB3}$ $V_{eC3}$	$V_{eA4}$ $V_{eB4}$ $V_{eC4}$	$V_{eA5}$ $V_{eB5}$ $V_{eC5}$

Taking the PWM waveforms in Fig. 3.2 as an example, the durations and three phase error voltages for 5 segments are shown in Table 3.4.

Error voltages in  $dq$ -axes can be calculated from  $abc$ -axes by Park transformation.

$$\begin{bmatrix} V_{edj} \\ V_{eqj} \end{bmatrix} = \mathbf{T}_{dq}(\theta) \cdot \begin{bmatrix} V_{eAj} \\ V_{eBj} \\ V_{eCj} \end{bmatrix} \quad (3.4)$$

$$\mathbf{T}_{dq}(\theta) = \frac{2}{3} \begin{bmatrix} \cos \theta & \cos(\theta - 120^\circ) & \cos(\theta + 120^\circ) \\ -\sin \theta & -\sin(\theta - 120^\circ) & -\sin(\theta + 120^\circ) \end{bmatrix}$$

where  $j$  represents the segment 1~5.

Table 3.4 Durations and Three Phase Error Voltages for 5 Segments

$t_1 = t_A$	$t_2 = t_C - t_A$	$t_3 = T_{PWM} - 2t_C$	$t_4 = t_C - t_A$	$t_5 = t_A$
$V_{eA1} = -V_{AZ}^*$	$V_{eA2} = V_{dc1} - V_{AZ}^*$	$V_{eA3} = V_{dc1} - V_{AZ}^*$	$V_{eA4} = V_{dc1} - V_{AZ}^*$	$V_{eA5} = -V_{AZ}^*$
$V_{eB1} = 0$	$V_{eB2} = 0$	$V_{eB3} = 0$	$V_{eB4} = 0$	$V_{eB5} = 0$
$V_{eC1} = -V_{dc2} - V_{CZ}^*$	$V_{eC2} = -V_{dc2} - V_{CZ}^*$	$V_{eC3} = -V_{CZ}^*$	$V_{eC4} = -V_{dc2} - V_{CZ}^*$	$V_{eC5} = -V_{dc2} - V_{CZ}^*$

The three phase error voltages contain the zero sequence component, which cannot generate current in the isolated DC-bus dual inverters due to the block of the zero sequence circuit. With Park transformation, error voltages in  $dq$ -axes can be calculated, and the zero sequence component can be separated simultaneously.

By ignoring resistance voltage drops, the relationship between the error voltage and the current variation in a segment can be expressed as

$$i_{varj} = \int \frac{V_{exj}}{L_x} dt \quad (3.5)$$

where “ $x$ ” represents  $d$  or  $q$ ,  $L_x$  is the  $d$  or  $q$ -axis inductance.

With the error voltages in  $dq$ -axes, the ripple currents at the end of each segment can be calculated by

$$\begin{aligned} i_{x1} &= \frac{V_{ex1}t_1}{L_x} & i_{x2} &= i_{x1} + \frac{V_{ex2}t_2}{L_x} & i_{x3} &= i_{x2} + \frac{V_{ex3}t_3}{L_x} \\ i_{x4} &= i_{x3} + \frac{V_{ex4}t_4}{L_x} & i_{x5} &= i_{x4} + \frac{V_{ex5}t_5}{L_x} \end{aligned} \quad (3.6)$$

The trajectories of current ripples in  $dq$ -axes corresponding to PWM waveforms in Fig. 3.2 can be depicted in Fig. 3.6 with the DC-bus voltage ratio of 1:1.

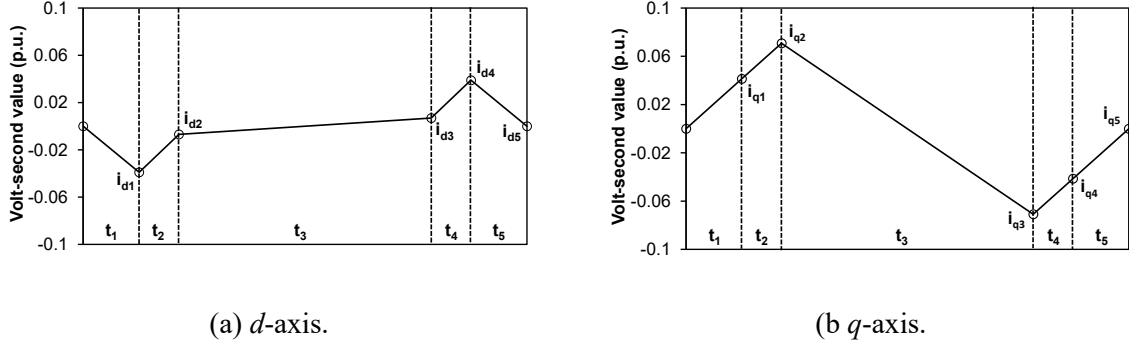


Fig. 3.6 Current ripple trajectories in  $d$  and  $q$ -axis.

The root-mean-square (rms) value in  $dq$ -axes of ripple currents in the next PWM cycle can be predicted as

$$\Delta i_{x(rms)} = \sqrt{\frac{1}{3T_s} \sum_{j=1}^5 t_j (i_{xj-1}^2 + i_{xj} i_{xj-1} + i_{xj}^2)}. \quad (3.7)$$

In order to suppress high-frequency current ripples, a cost function is designed to evaluate the total rms value of  $d$  and  $q$ -axis current ripples. The cost function is designed as

$$g = \sqrt{\Delta i_{d(rms)}^2 + \Delta i_{q(rms)}^2}. \quad (3.8)$$

The control diagram of the proposed OW-SPWM strategy is shown in Fig. 3.7. Various OW-SPWM switching patterns can be realized by different combinations of ZSV injection and voltage distribution methods. There are 8 ZSV injection methods and 16 voltage distribution methods, so that there are 128 candidate combinations of ZSV injection and voltage distribution methods. The one that has the minimum cost value is selected as the optimal combination of ZSV injection and voltage distribution methods, and will be applied in the next PWM cycle. It needs to note that there are some restrictions of ZSV injection and voltage distribution methods. The reference voltages after a ZSV injection should be between  $-V_{dc2}$  and  $V_{dc1}$  as described in Section 3.2.1, while the voltage distribution method 3 can only be used under the condition  $V_n^* \geq V_{dc1} - V_{dc2}$ , and the voltage distribution method 4 can only be used under the condition  $V_n^* < V_{dc1} - V_{dc2}$  as described in Section 3.2.2. With these restrictions, the candidates for the prediction model are less than 128.

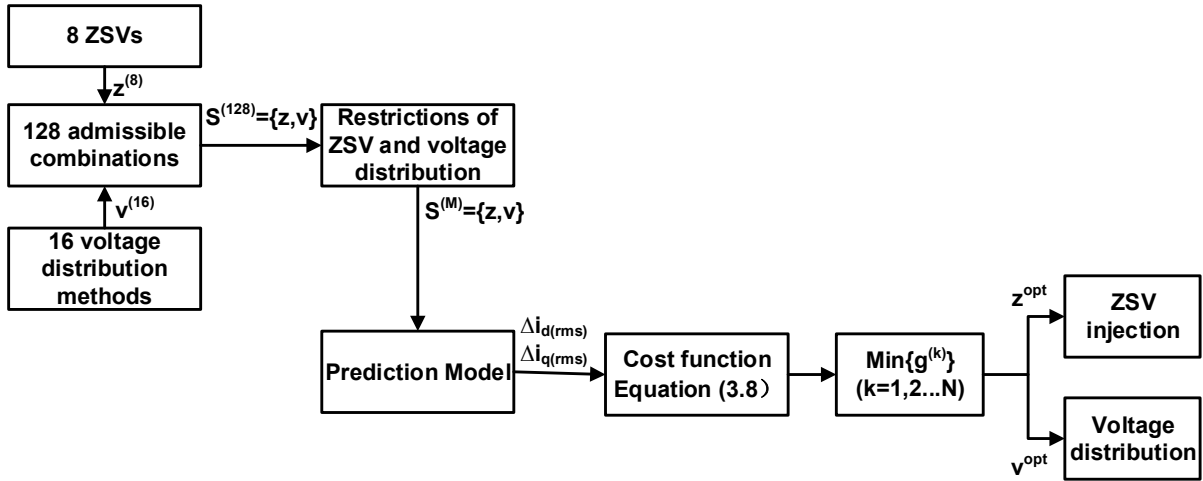


Fig. 3.7 Control diagram of proposed OW-SPWM.

### 3.2.4 Capacitor overcharge issue in dual inverters

For a unidirectional voltage source, including uncontrolled rectifier, current only can flow out of the positive pole, but cannot flow into the positive pole. Although an asymmetric dual inverter configuration enables the possibility to improve output quality (e.g. four-level in DC-bus voltage ratio 1:2 or 2:1), it increases the risk of overcharging the capacitor on the low-voltage side with unidirectional voltage sources. This situation can eliminate the desired DC-bus voltage ratio and may cause safety issues of the capacitor on the low-voltage side [HUA22]. In an OW machine fed by isolated DC-bus DTL-VSIs, the two inverters control the same three phase windings, and they also need to provide the current flow path for each other. The flow path may be blocked in an inverter under a certain switching state and current directions. Consequently, the current may flow into the capacitor in dual inverters with unidirectional voltage sources, and cause the charge of the capacitor. The overcharging issue at the DC-bus voltage ratio 2:1 is studied in [RED11], and the vector of Inverter II which subtends an acute angle with the vector of Inverter I should be avoided, as they can cause the charge of the capacitor in Inverter II. The current vector direction in [RED11] is assumed to be always the same as the voltage vector of Inverter I. For example, Inverter I is in the state of vector 1 (100), so that three-phase currents are assumed to be positive, negative, and negative, respectively. However, the directions of current and voltage vectors are often different, so the conclusion in [RED11] is not accurate. A simplified method is proposed in this chapter to accurately avoid the overcharge of capacitors.

To analyse the charge of the capacitor, both current and voltage vector directions are used in

this chapter. To simplify the capacitor overcharge issue in dual inverters, this problem can be analysed in a two-level inverter firstly, and then in dual inverters. The charge of the capacitor occurs when the angle formed by the voltage and current vectors is an obtuse angle in a two-level inverter, and this conclusion can be explained by the flowing of power between the inverter and the machine. If the angle between the output voltage and current vectors is an acute angle in an inverter, the power is positive, which means the power flows out from the inverter to the machine. On the other hand, if the angle is an obtuse angle, the power is negative, and the power flows out from the machine to the inverter, which can cause the charge of the capacitor. This conclusion can also be applied to two inverters in an OW drive, and it needs to note that the directions of current vectors are opposite with respect to two inverters. To avoid the overcharge of capacitors in dual inverters, the angle between voltage and current vectors in each two-level inverter should be less than 90 degrees, which should be applied as restrictions in the proposed OW-SPWM. For current vectors in Fig. 3.8 in the space vector planes of two inverters, the voltage vectors that can avoid the charge of capacitors are in grey regions.

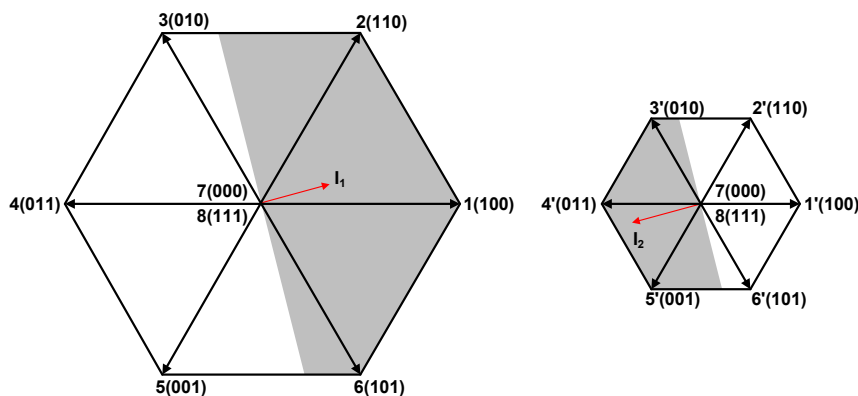


Fig. 3.8 Current vectors and voltage vectors in Inverters I and II.

### 3.2.5 Switching commutation issue in dual inverters

Switching actions are turn on/off times of switching devices within a PWM cycle, while switching commutations are turn-on/-off times of switching devices at the beginning or end of a PWM cycle. The proposed OW-SPWM can cause switching commutations due to the applying of different voltage distribution methods in Table 3.2. Switching commutations can increase the switching loss, and should be considered in the proposed OW-SPWM.

In the 5-segment PWM of the proposed OW-SPWM, the first and last vectors in a PWM cycle are the same, and designated as the commutation vector in this chapter. Switching

commutations are caused by different commutation vectors in two adjacent PWM cycles. To reduce switching commutations, a restriction of commutation vectors is added to the proposed OW-SPWM in Table 3.5. It can be observed that initial switching states in a PWM cycle for two legs of H-bridges cannot be both positive, which has been considered in the selection of voltage distribution methods in Section 3.2.2. Taking voltages of capacitors and switching commutations into account, the control diagram of the proposed OW-SPWM is improved as shown in Fig. 3.9. Together with the restriction of ZSV injection and voltage distribution methods in Section 3.2.1 and 3.2.2, the control of capacitor voltage and switching commutations can further reduce the number of candidates that is sent into the prediction model. As a result, the actual candidates are much less than 128, so that the computation burden is reduced.

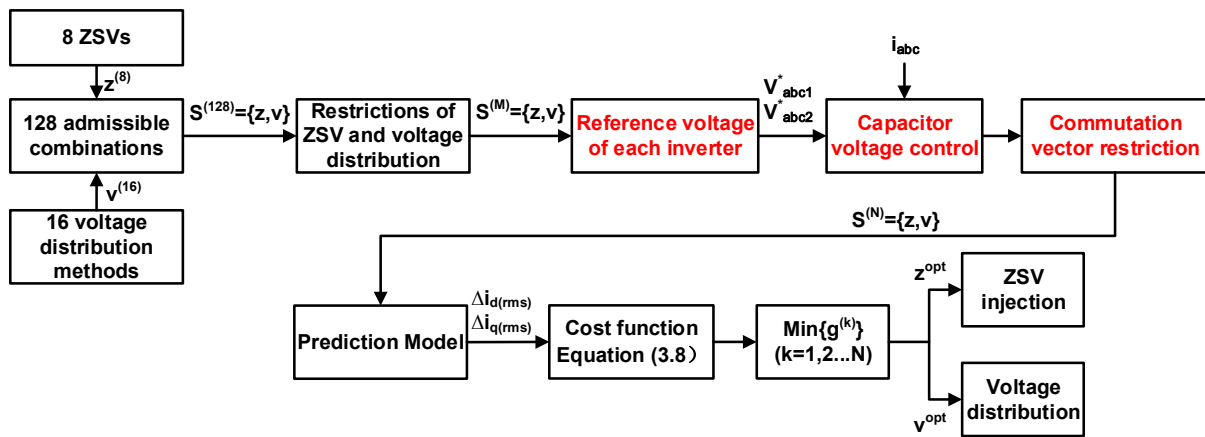


Fig. 3.9 Control diagram of the proposed OW-SPWM strategy with capacitor voltage and switching commutation control.

Table 3.5 Restriction of Commutation Vectors

Sectors	1	2	3	4	5	6
Commutation vectors ( $V_{dc1} < V_{dc2}$ )	74'	77' or 75'	76'	77' or 71'	72'	77' or 73'
Commutation vectors ( $V_{dc1} \geq V_{dc2}$ )	77' or 17'	27'	77' or 37'	47'	77' or 57'	67'

### 3.3 Experiment Results

The proposed OW-SPWM strategy is validated on an OW-PMSM fed by isolated DC-bus DTL-VSIs. The magnitudes of current harmonics caused by PWM strategies are affected by DC-bus voltage, electrical machine inductance, and PWM frequency. For the convenience of comparison of current harmonics, a relatively high DC-bus voltage, smaller electrical machine inductance, and low PWM frequency is needed. The PWM frequency, current loop frequency, and sampling frequency are set as 2kHz in the experiments. The parameters of the tested OW-PMSM are listed in Table 3.6. The DC-bus voltages of two inverters with different DC-bus voltage ratios are shown in Table 3.7, and the sum of two DC-bus voltages is always the same to keep the same maximum output voltages of dual inverters in different DC-bus voltage ratios. The dead-time is set to 2 $\mu$ s. Fig. 3.10 shows the experiment platform including a dSPACE, dual two-level inverters, an OW-PMSM, a load machine, and a position sensor.

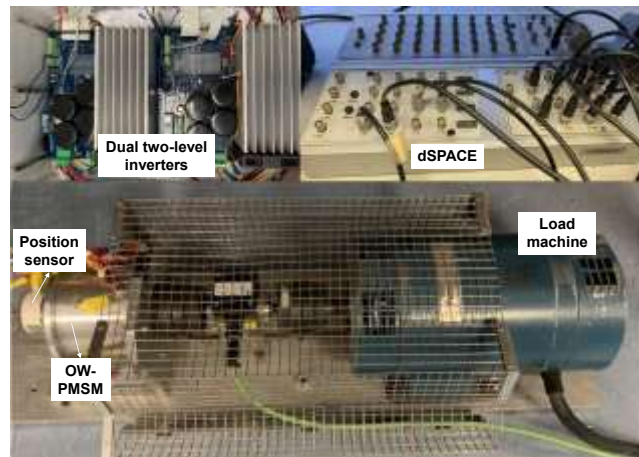


Fig. 3.10 Experiment platform.

The total harmonics of phase currents can be used to evaluate the influence of a PWM strategy on current harmonics, and can be defined as

$$\text{Total harmonics} = \sqrt{\sum_{n=1,2,3,\dots}^{\infty} (I_n)^2} \quad (3.9)$$

where  $I_n$  is the magnitude of the harmonic current at the  $n$  times of PWM frequency.



Table 3.6 Parameters of Tested OW-PMSM

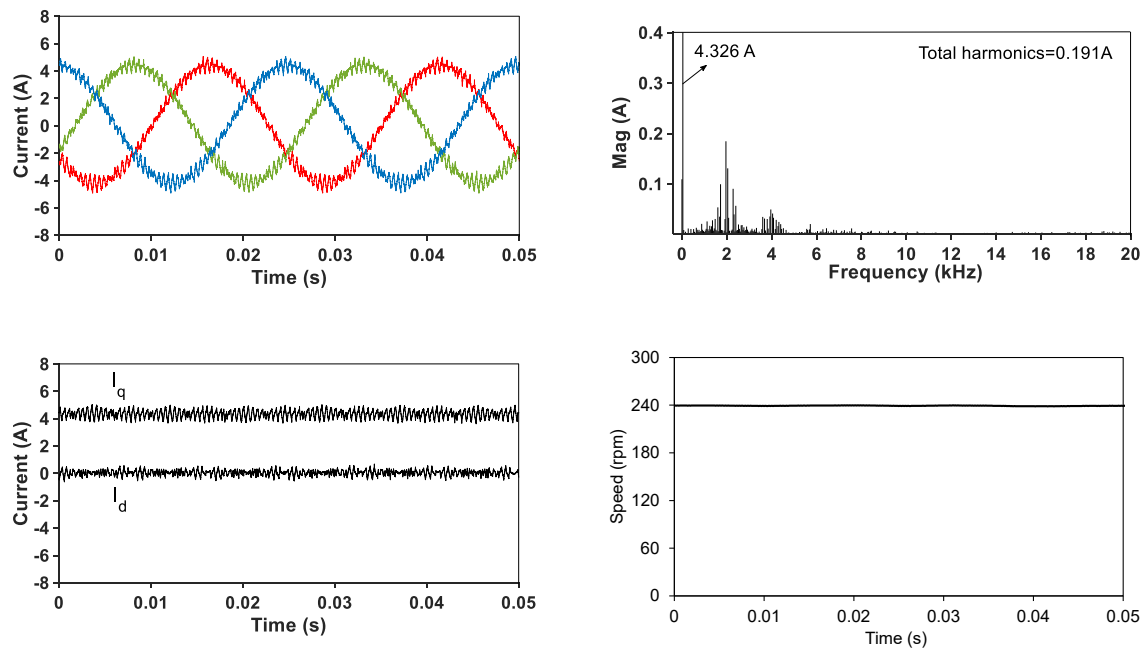
Pole pairs	10
Resistance( $\Omega$ )	1.2
PM flux linkage (mWb)	10
$d$ -axis inductances (mH)	1.7
$q$ -axis inductances (mH)	1.7
Rated current (A)	6
Rated torque (Nm)	0.9

Table 3.7 DC-bus Voltages of Two Inverters with Different Voltage Ratios

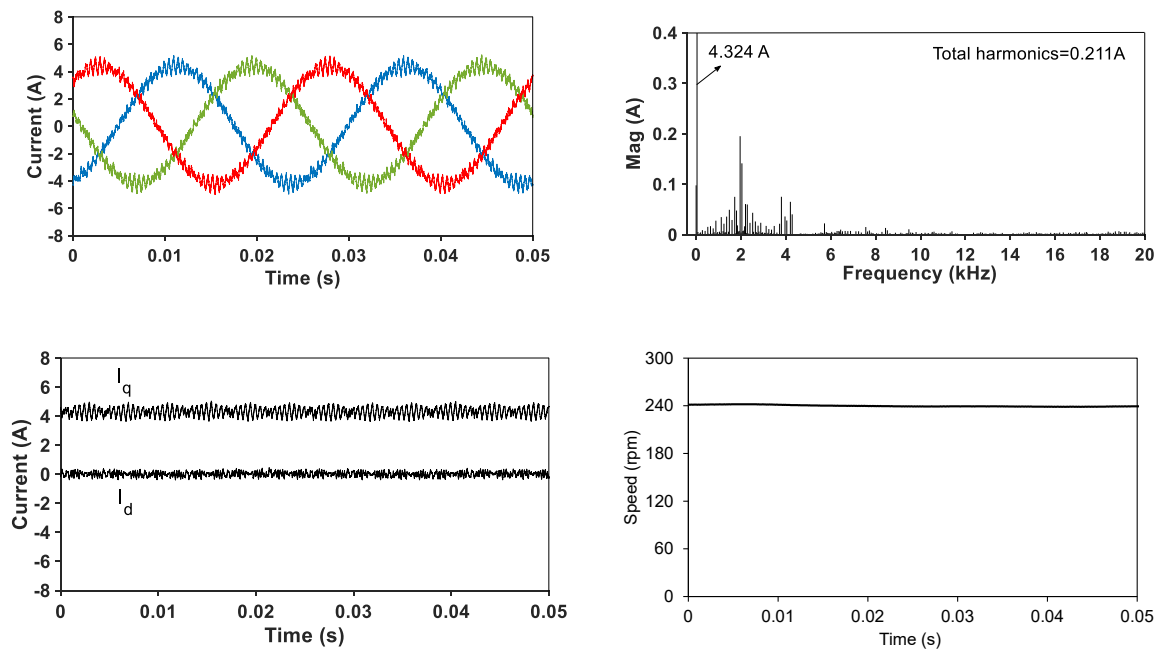
DC-bus voltage ratios	$V_{dc1}$ (V)	$V_{dc2}$ (V)
1:1	24	24
2:1	32	16
1:2	16	32
3:1	36	12
1:3	36	12

Current harmonics of the proposed OW-SPWM strategy and the conventional SVPWM strategy in [HUA19b] are compared with different DC-bus voltage ratios in this chapter. These two PWM strategies have the same switching actions in a PWM cycle, i.e. two legs are switched, and the other legs are clamped, and the similar switching commutations. As a result, these two PWM strategies can be compared with the same PWM frequency and switching loss. Figs. 3.11-3.15 compare measured three phase currents, phase current spectra,  $dq$ -axis current, and speed between the proposed OW-SPWM and the conventional SVPWM with 5 different DC-bus voltage ratios. The speed is 240rpm and the modulation index is about 1.0. It can be

observed that the proposed OW-SPWM can generate lower phase current ripples and  $q$ -axis current ripples for all DC-bus voltage ratios.



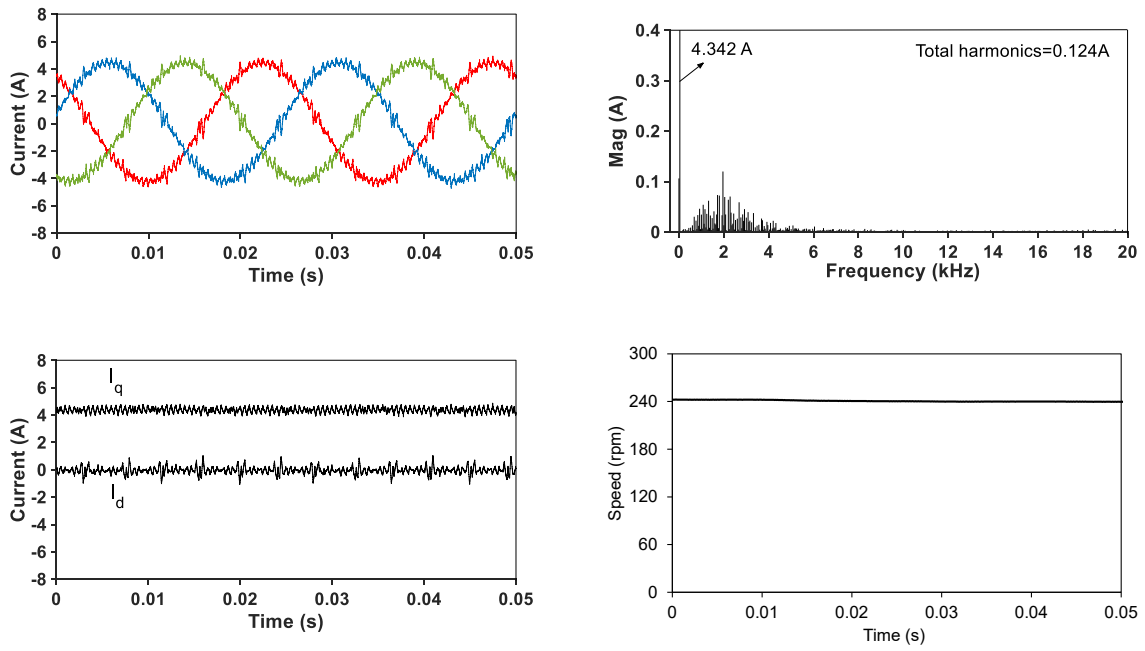
(a) Proposed OW-SPWM.



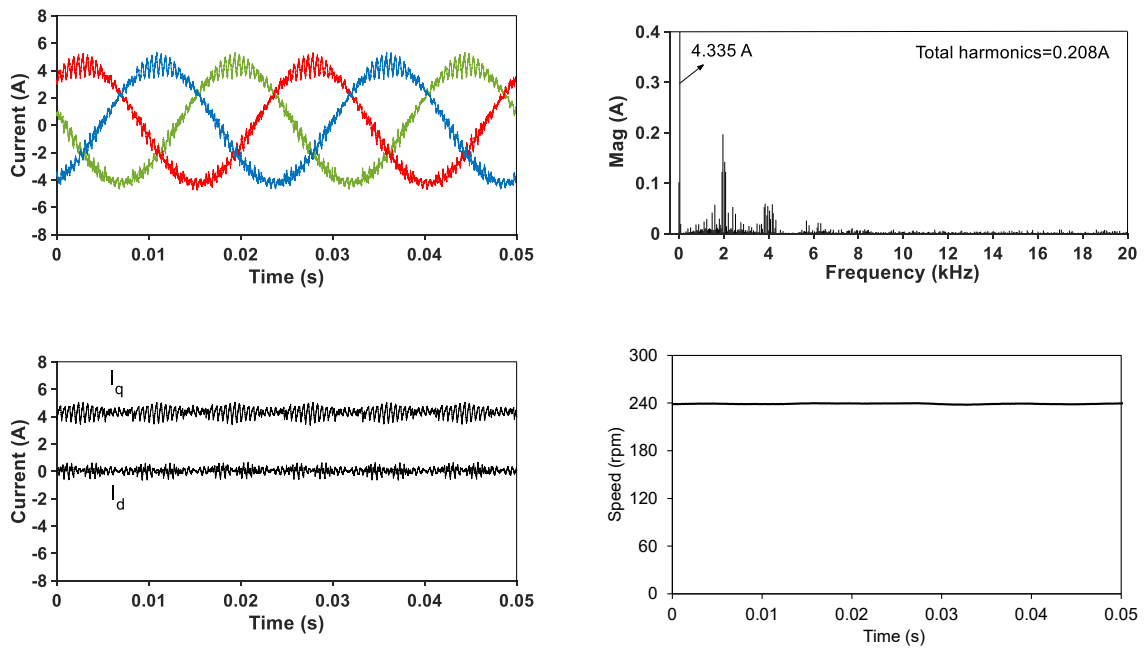
(b) Conventional SVPWM.

Fig. 3.11 Measured waveforms, spectra of phase current,  $dq$ -axis current, and speed with proposed OW-SPWM and conventional SVPWM under DC-bus voltage ratio of 1:1 (speed = 240rpm, MI =

1.0).

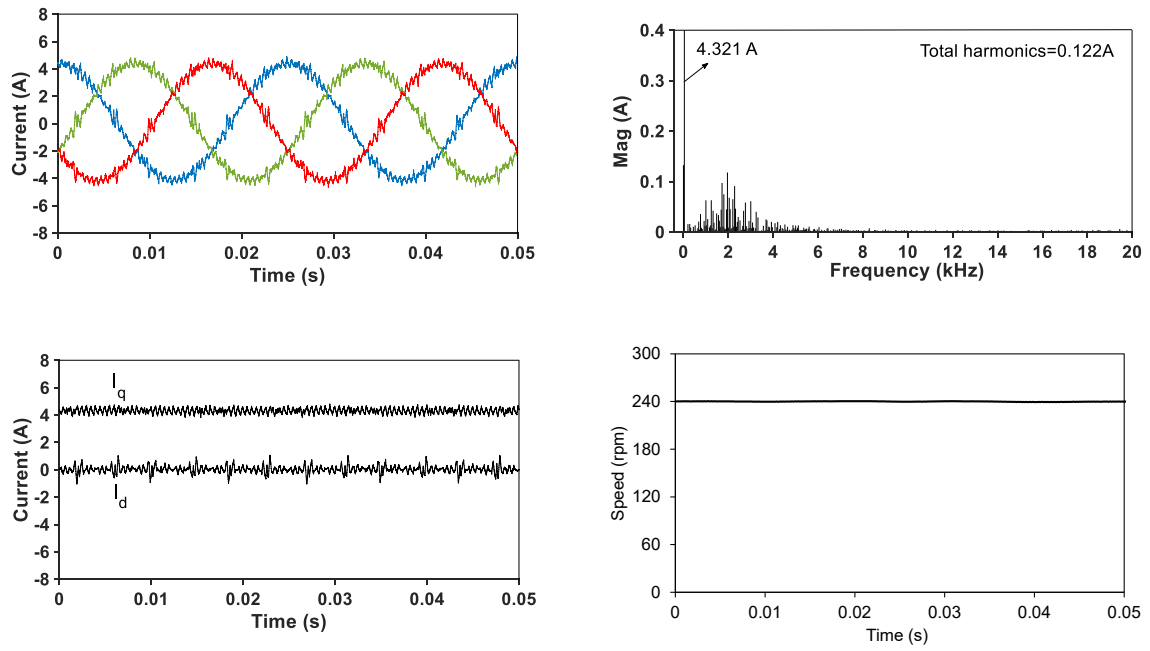


(a) Proposed OW-SPWM.

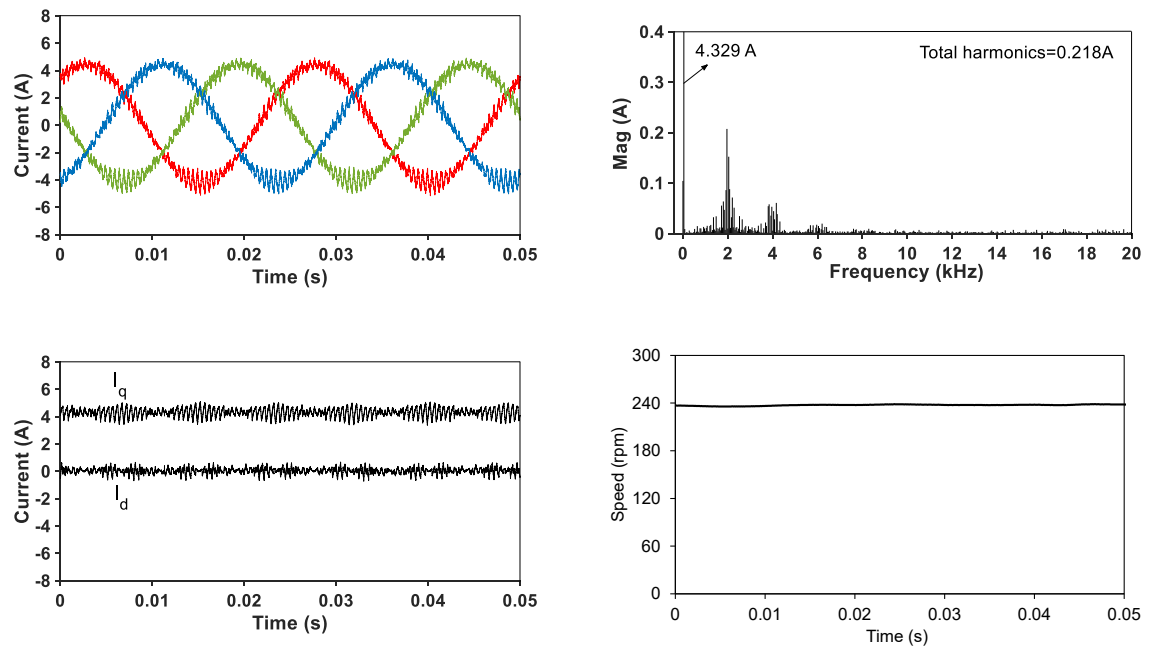


(b) Conventional SVPWM.

Fig. 3.12 Measured waveforms, spectra of phase current,  $dq$ -axis current, and speed with proposed OW-SPWM and conventional SVPWM under DC-bus voltage ratio of 1:2 (speed = 240rpm, MI = 1.0).

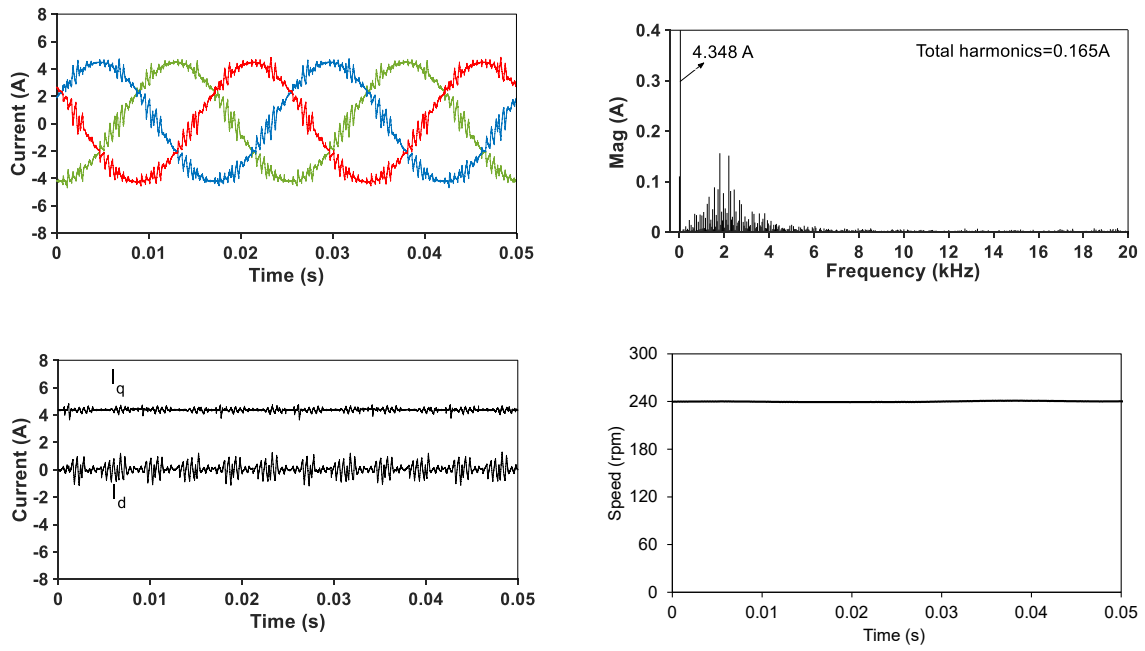


(a) Proposed OW-SPWM.

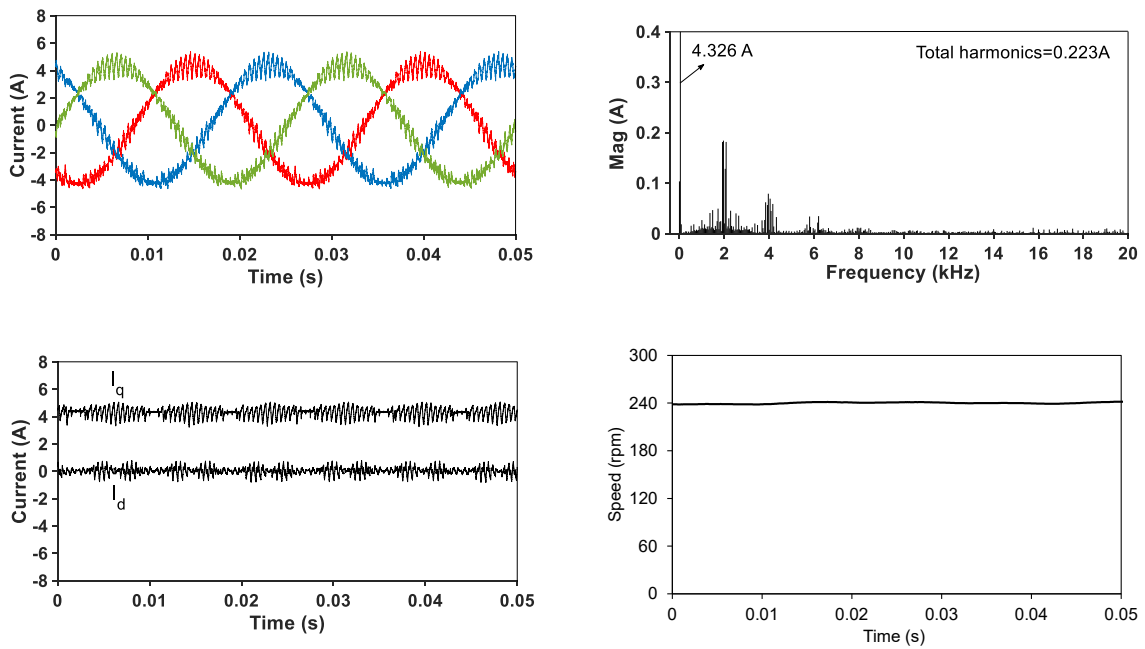


(b) Conventional SVPWM.

Fig. 3.13 Measured waveforms, spectra of phase current,  $dq$ -axis current, and speed with proposed OW-SPWM and conventional SVPWM under DC-bus voltage ratio of 2:1 (speed = 240rpm, MI = 1.0).

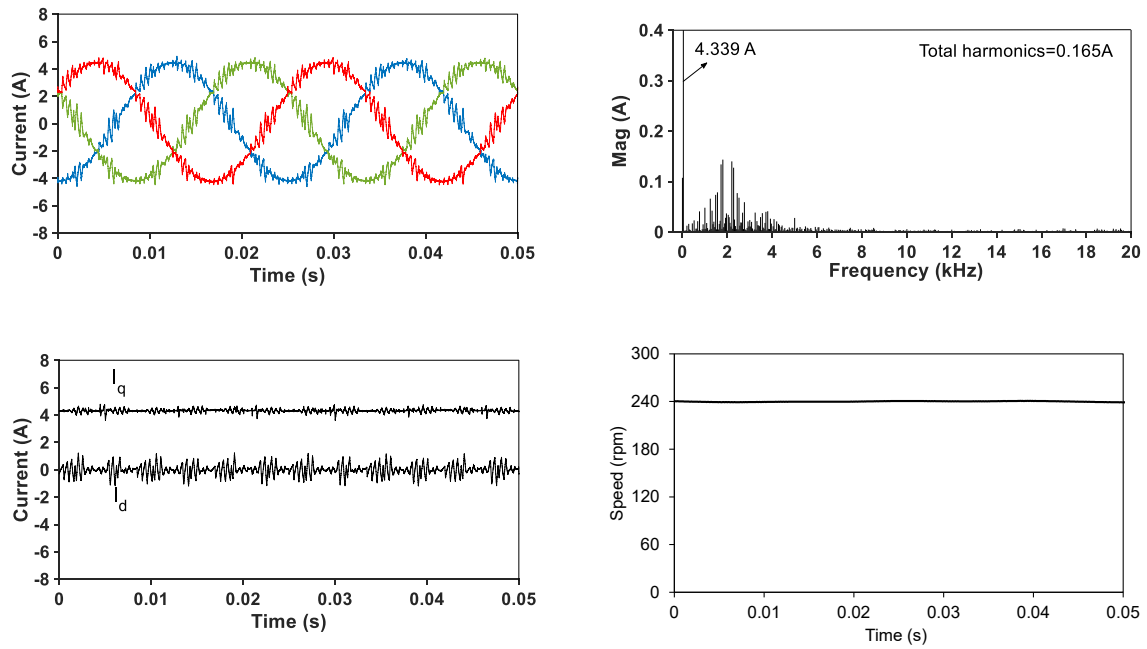


(a) Proposed OW-SPWM.

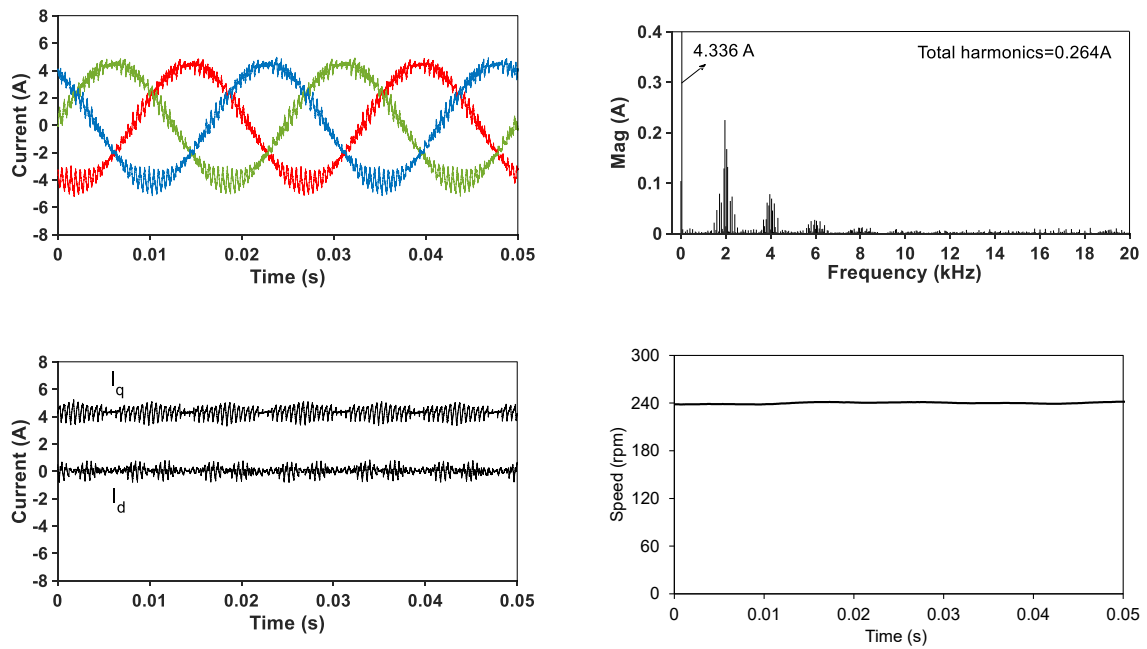


(b) Conventional SVPWM.

Fig. 3.14 Measured waveforms, spectra of phase current,  $dq$ -axis current, and speed with proposed OW-SPWM and conventional SVPWM under DC-bus voltage ratio of 1:3 (speed = 240rpm, MI = 1.0).



(a) Proposed OW-SPWM.



(b) Conventional SVPWM.

Fig. 3.15 Measured waveforms, spectra of phase current,  $dq$ -axis current, and speed with proposed OW-SPWM and conventional SVPWM under DC-bus voltage ratio of 3:1 (speed = 240rpm, MI = 1.0).

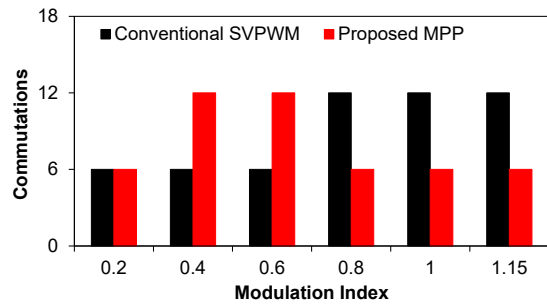
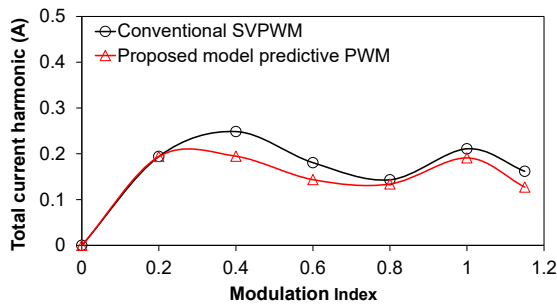
There are 128 candidate combinations of ZSV injection and voltage distribution methods in the proposed OW-SPWM in Fig. 3.9, but the final candidates for the prediction model are

reduced due to the restrictions of ZSV injection, voltage distribution, capacitor voltage, and switching commutation control. Table 3.8 shows the measured numbers of candidates for the prediction model of proposed OW-SPWM with different voltage ratios. As a result, the actual candidates are no more than 6 and much less than 128, so that the proposed OW-SPWM has a low computation burden. The numbers of candidates change with operations conditions, including DC-bus voltage ratio, modulation index, and electrical angle. Although only a few candidates are evaluated by the prediction model each time, all 128 candidates are needed to cover all operation conditions.

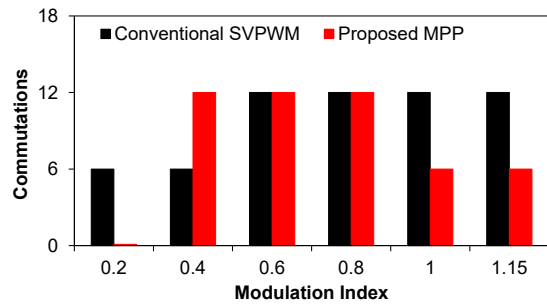
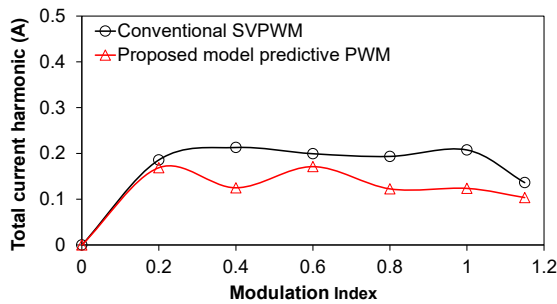
Fig. 3.16 shows the total current harmonics and switching commutations in an electrical cycle of the proposed OW-SPWM and the conventional SVPWM with different DC-bus voltage ratios. It can be seen that the proposed OW-SPWM and the conventional SVPWM have similar switching commutations. Due to the same switching actions in a PWM cycle in these two PWM strategies, so that they can be compared with the same switching loss. The proposed OW-SPWM shows lower current harmonics compared with the conventional SVPWM, and the better performance is more obvious in unequal DC-bus voltage ratios. Figs. 3.14 (a) and (b) compare the total current harmonics under different DC-bus voltage ratios with the proposed OW-SPWM and the conventional SVPWM, respectively. The current harmonics are different for DC-bus voltage ratios 1:2 and 2:1, 1:3 and 3:1 in the conventional SVPWM, since the vector selection and vector action sequence do not change with voltage ratios. However, considering the symmetrical structure of two inverters in an OW drive, DC-bus voltage ratios 1:2 and 2:1, 1:3, and 3:1 should have the similar current harmonic characteristic. This problem can be solved in the proposed OW-SPWM as shown in Fig. 3.17 (b). Figs. 3.18 and 3.19 compare voltages of capacitors with and without the capacitor voltage control, which is the 90-degree restriction of the angle between voltage and current vectors in each two-level inverter. The overcharge of the capacitor in Inverter I can be seen from the measured results in Fig. 3.18 without the capacitor voltage control, when the modulation index is 0.6 and the DC-bus voltage ratio is 1:2 (16V:32V). In Fig. 3.18 (b), the angle between voltage and current vectors can be larger than 90 degrees in Inverter I. Consequently, the DC-bus voltage of Inverter I will increase and become larger than 16V in Fig. 3.18 (c). With the control of capacitor voltages, the angle between voltage and current vectors in both inverters can be limited to 90 degrees as shown in Fig. 3.19 (b), and the DC-bus voltage of Inverter I can be maintained on 16V in Fig. 3.19 (c).

Table 3.8 Measured number of candidates for prediction model

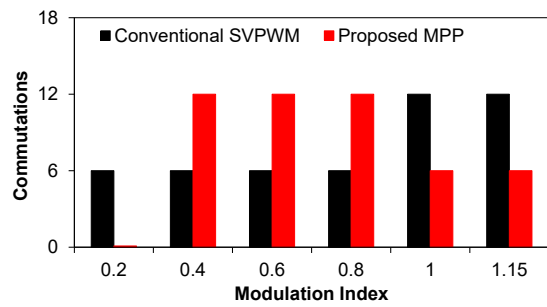
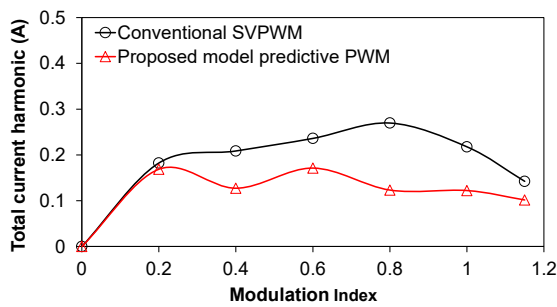
MI \ Voltage ratios	0.2	0.4	0.6	0.8	1	1.15
1:1	3~6	3~6	2~6	1~4	1~4	1~4
2:1	5~6	4~6	2~5	1~5	1~4	1~4
1:2	5~6	4~6	2~5	1~5	1~4	1~4
3:1	4~6	3~5	2~5	2~5	1~4	1~4
1:3	4~6	3~5	2~5	2~5	1~4	1~4



(a) 1:1.

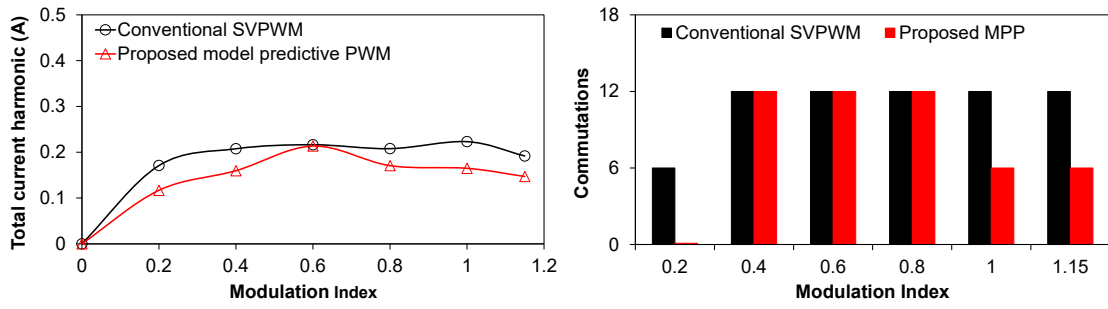


(b) 1:2.

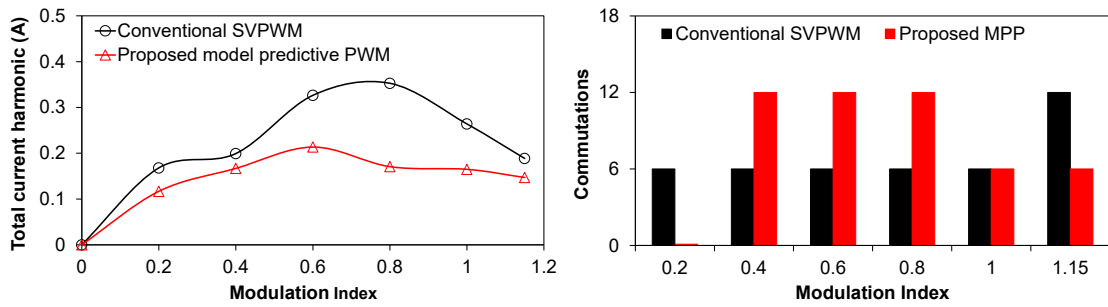


(c) 2:1.



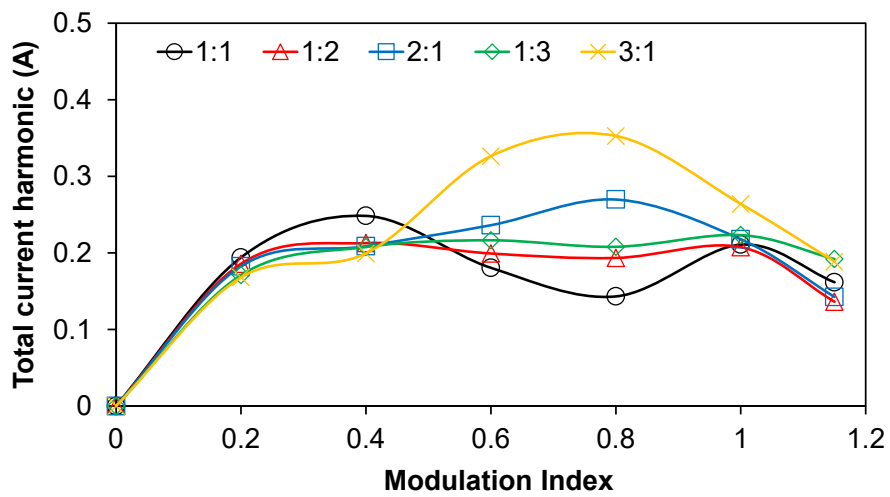


(d) 1:3.

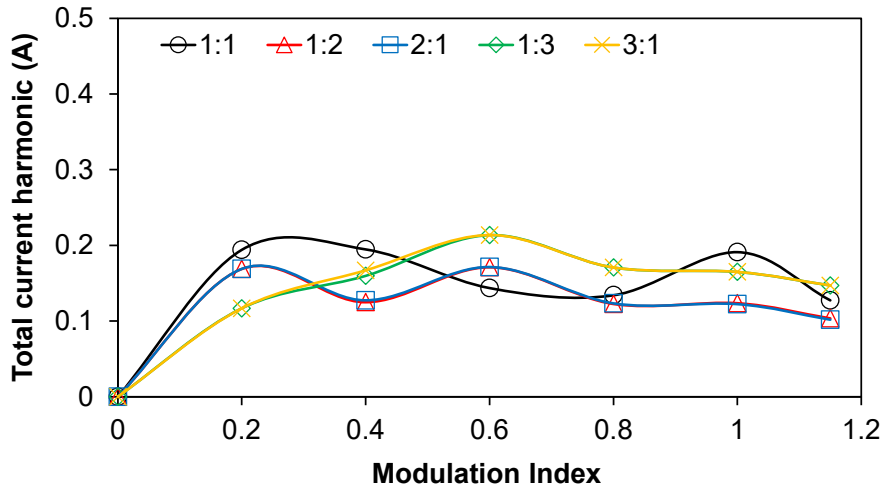


(e) 3:1.

Fig. 3.16 Total current harmonics and switching commutations of the proposed OW-SPWM and conventional SVPWM with different DC-bus voltage ratios.

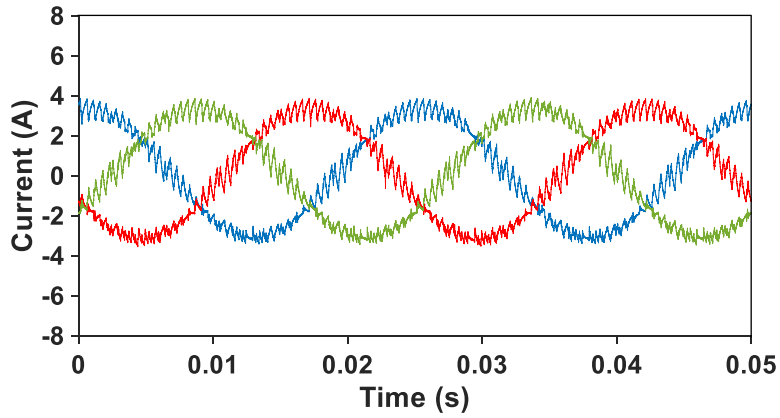


(a) Conventional SVPWM.

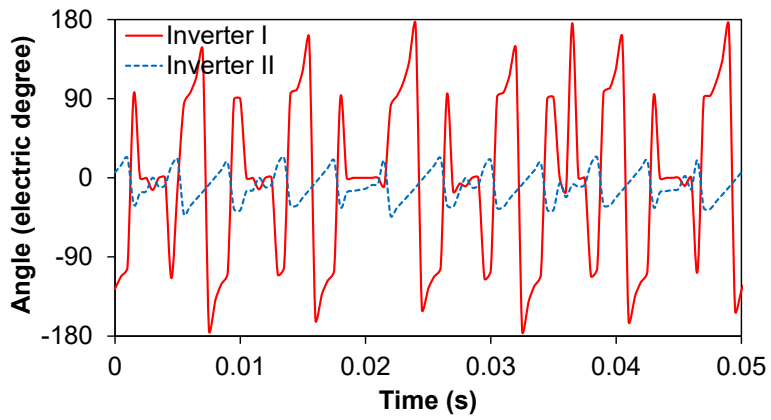


(b) Proposed OW-SPWM.

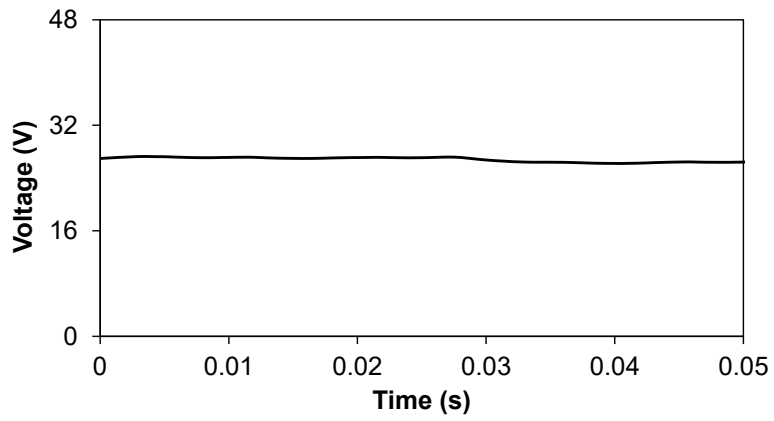
Fig. 3.17 Total current harmonics of the proposed OW-SPWM and conventional SVPWM with different DC-bus voltage ratios.



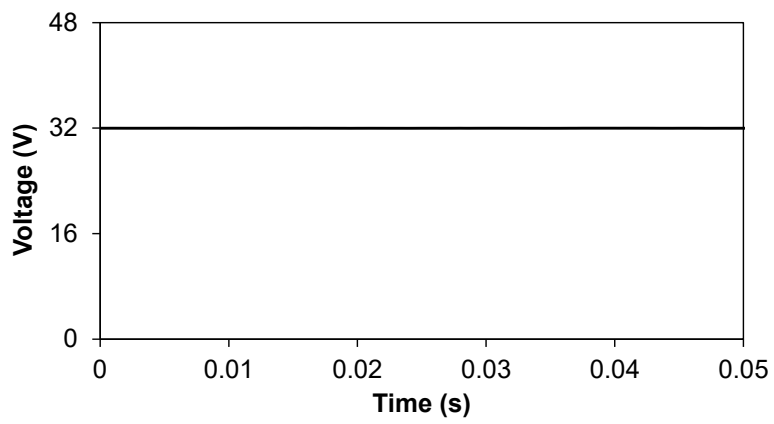
(a) Three phase currents.



(b) Angle between voltage and current vectors.

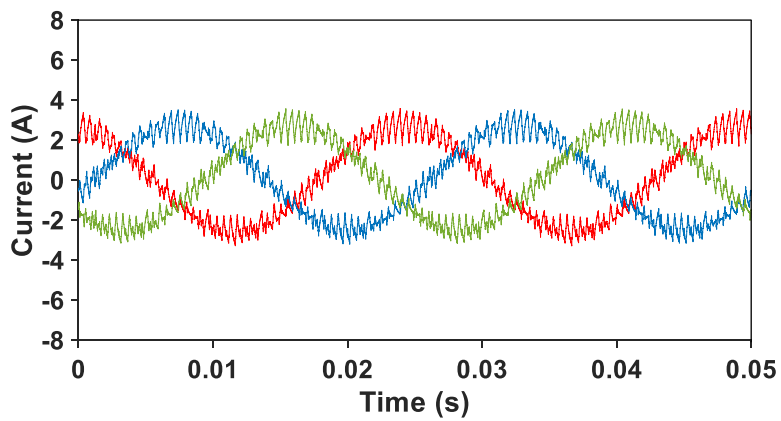


(c) DC-bus voltage of Inverter I.

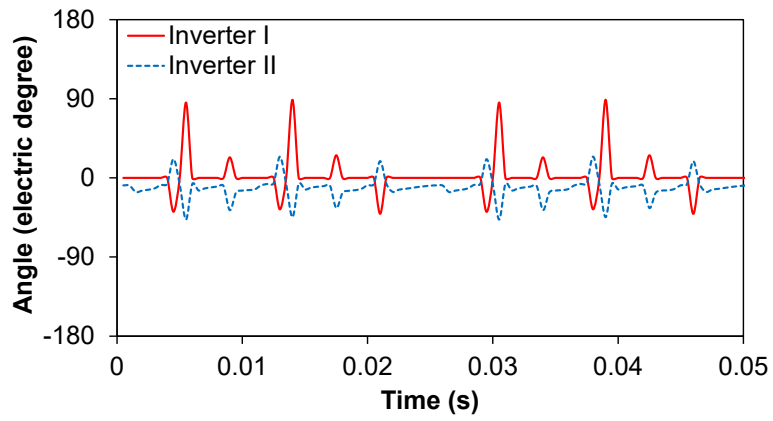


(d) DC-bus voltage of Inverter II.

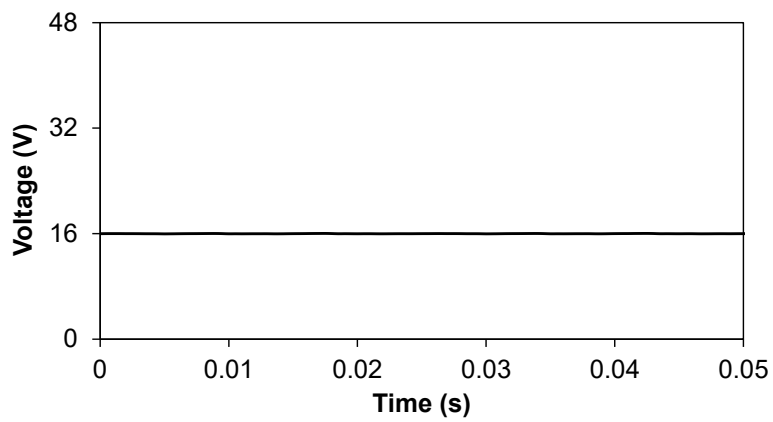
Fig. 3.18 Measured result of the proposed OW-SPWM strategy without capacitor voltage control (DC-bus voltage ratio 1:2, MI = 0.6).



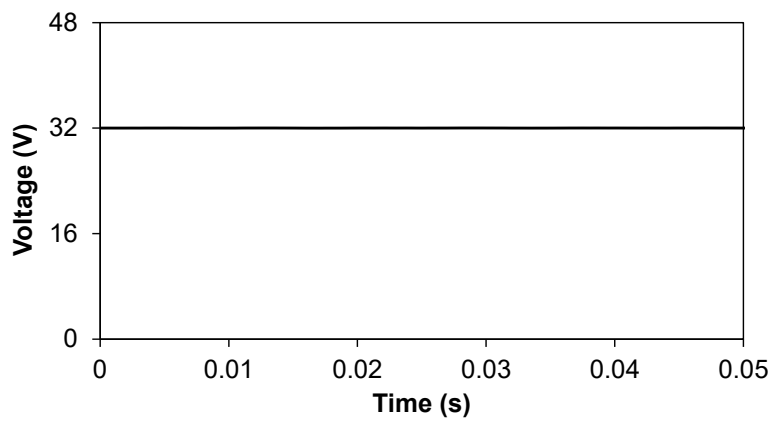
(a) Three phase currents.



(b) Angle between voltage and current vectors.



(c) DC-bus voltage of Inverter I.



(d) DC-bus voltage of Inverter II.

Fig. 3.19 Measured result of the proposed OW-SPWM strategy with capacitor voltage control (DC-bus voltage ratio 1:2, MI = 0.6).

### 3.4 Summary

In this chapter, a generalized OW-SPWM is proposed for an OW machine fed by isolated DC-bus DTL-VSIs with arbitrary DC-bus voltage ratios for current harmonic minimization. With the current ripple prediction model for the OW machine fed by DTL-VSIs, the optimal combination of ZSV injection and voltage distribution methods can be selected to achieve the optimal switching pattern for the next PWM cycle to improve the current harmonic characteristic. Compared with the conventional generalized SVPWM strategy for arbitrary DC-bus voltage ratios, the proposed generalized OW-SPWM shows better current harmonic characteristics in all DC-bus voltage ratios, and the better performance is more obvious in unequal DC-bus voltage ratios. The issue of different harmonic characteristics between DC-bus voltage ratios 1:2 and 2:1, 1:3 and 3:1 in the conventional method is solved in the proposed method. Moreover, in the proposed OW-SPWM, the switching commutation control can guarantee a similar switching loss with the conventional SVPWM, and a simplified capacitor voltage control method is used to avoid the overcharge of capacitors. The superior performance of the proposed OW-SPWM is verified experimentally.

SPWM strategies with ZSV injection and voltage distribution are used in Chapters 2 and 3 for the current harmonic reduction in the isolated DC-bus OW drive with symmetrical and arbitrary DC-bus voltage ratios, respectively, and the unbalanced voltage distribution is used to reduce switching actions in a PWM cycle. In the next chapter, both balanced and unbalanced voltage distributions are used, the different voltage distortion from inverter nonlinearity in the two voltage distributions are analysed and utilized for the inverter nonlinearity compensation.

# **CHAPTER 4 INVERTER NONLINEARITY COMPENSATION FOR OPEN WINDING MACHINE WITH DUAL SWITCHING MODES**

Both balanced and unbalanced switching modes can be used in dual two-level inverters with isolated DC-bus, and SPWM strategies with the unbalanced switching mode are used in Chapters 2 and 3 for the current harmonic reduction with identical and arbitrary voltage ratios, respectively. Both balanced and unbalanced switching modes will be used in this chapter, and a novel inverter nonlinearity compensation method is proposed for OW machines fed by isolated DC-bus dual two-level 3-phase inverters based on the dual switching modes. Inverter nonlinearity of dual inverters is analysed in both balanced and unbalanced switching modes for the first time, and the different voltage distortions are utilized for a close loop inverter nonlinearity compensation by alternately applying the two switching modes. The proposed strategy needs no offline measurement for the parameters of dual inverters and the electrical machine, and can also deal with the variation of inverter parameters in different operation conditions. Further, the proposed strategy can overcome issues in conventional current harmonic-based methods, such as the need of accurate rotor position and preset compensation voltage curves. Experimental results verify the performance of the proposed inverter nonlinearity compensation method.

This chapter is based on the paper published in:

L. Xu and Z. Q. Zhu, "Inverter nonlinearity compensation for open-winding machine with dual switching modes," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2022.3164851.

## 4.1 Introduction

PWM inverters are widely used in PMSM drives due to excellent performance, such as fast response and low harmonics. To prevent the shoot-through in the DC-bus due to simultaneous conduction of two switches in one inverter leg, dead times should be inserted into the two gate drive signals. As a result, before the turn-on of one switch, the other switch in the same leg should be turned off in advance. Dead times will cause errors between the real output voltages and the reference voltages in an inverter. Besides, turn-on and turn-off times of inverter switches can also affect the errors. It needs to note that the average contribution of time delays caused by the effect of inverter parasitic capacitances can be included in turn-on/off times. Furthermore, the voltage drops of switching devices and freewheel diodes can also affect output voltages of an inverter. These physical parameters of an inverter are difficult to be measured accurately since they can vary with operation conditions, such as phase currents, DC-bus voltage, and temperature [KIM06].

The distortion of inverter output voltages will cause current harmonics, torque ripples, extra losses, and thus degrade the control performance of electrical machines. Moreover, in the sensorless control and motor parameter estimation, reference voltages are often used as output voltages, so that it is essential to acquire errors between the two voltages. To deal with this problem, many approaches have been proposed to compensate for error voltages caused by inverter nonlinearity [PEL10] [SUK91] [WAN18]. Among them, early approaches are based on the offline compensation. In [PEL10], a look-up table that contains inverter nonlinearity characteristics is set up to compensate for voltage distortions. However, offline measurements are time consuming and difficult to deal with the variation of inverter parameters. Consequently, online compensation strategies are developed to address these problems [CHO96] [KIM06] [PAR12] [PAR14] [ZHA04]. The distortion voltage in  $q$ -axis is calculated to suppress harmonics caused by inverter nonlinearity in [CHO96], but this method needs to sample currents in two different steady states, which limits the operation condition. Furthermore, the inverter nonlinearity caused by parasitic capacitances is not considered. The model reference adaptive system is utilized to generate compensation voltages in [KIM06]. However, the accurate model of an electrical machine is difficult to acquire, as its parameters vary with operation conditions. The 6<sup>th</sup> harmonics in  $dq$ -axes are extracted to generate compensation voltages in [ZHA04] [PAR12] [PAR14] [LIU14]. In these current harmonic-based methods, preset compensation voltage curves, which are similar to an S curve, are needed, which limits

the performance of the compensation. Moreover, these current harmonic-based methods have disadvantages such as the need of accurate rotor position and the convergence of compensation voltages is affected by the electrical frequency. Besides, the 6<sup>th</sup> harmonics in  $dq$ -axes are assumed to be only generated by inverter nonlinearity, which is inaccurate in the control of PMSMs with non-ideal back EMF. In [LEE21], a switching between continuous and discontinuous PWM strategies is utilized for inverter nonlinearity compensation. However, the low switching frequency will cause a low response. Moreover, pre-set compensation voltage curves and accurate position are still needed.

The effects of inverter nonlinearity on output voltages are analysed and many compensation methods are proposed for a two-level inverter, but researches are rare on OW machines fed by dual two-level inverters. The two different switching modes of dual inverters can be used in the SPWM strategies and compared in Chapter 2. The two switching modes can generate different actions of switching devices, and the effects of inverter nonlinearity on phase voltages are different. In this chapter, the effects of inverter nonlinearity on phase voltages in isolated DC-bus dual two-level 3-phase OW inverters are analysed and compared when the two switching modes are applied. Furthermore, the difference between the inverter nonlinearity effects on phase voltages of the two switching modes is utilized to compensate for the inverter nonlinearity.

## **4.2 Analysis of Nonlinearity of Dual OW Inverters**

In this section, the voltage model of dual OW inverters is described firstly. Then, two switching modes of SPWM strategy for dual OW inverters are described. Finally, the inverter nonlinearity of dual OW inverters in the two switching modes is analysed and compared.

### **4.2.1 SPWM strategy with balanced and unbalanced switching modes for dual OW inverters**

Many PWM strategies have been proposed by researchers with balanced [SOM08a] [SEK11] [SEK13] and unbalanced [SRI13] [SOM08b] [SRI15] [SEK18] switching modes for dual OW inverters. In Chapter 2, the balanced and unbalanced switching modes are compared and used in the conventional and proposed SPWMs, respectively. For the three H-bridges in an OW drive, two legs of each H-bridge are switched in the balanced switching mode, while one leg is switched and the other leg is clamped in the unbalanced switching mode. However, the



different effects of inverter nonlinearity on phase voltages are not studied for the two switching modes. In this chapter, the inverter nonlinearity will be analysed and compared for the two switching modes, and the difference will be utilized for the inverter nonlinearity compensation. The SPWM strategy with balanced and unbalanced switching modes is used in this chapter for the inverter nonlinearity compensation.

The control diagram of the SPWM strategy for dual OW inverters is shown in Fig. 4.1. A ZSV is injected to three phase reference voltages of dual OW inverters to increase the voltage utilization. The ZSV can be expressed as

$$V_z = \left[ -\max(V_A^*, V_B^*, V_C^*) - \min(V_A^*, V_B^*, V_C^*) \right] / 2 \quad (4.1)$$

where  $V_A^*$ ,  $V_B^*$ , and  $V_C^*$  are the reference voltages in three phases.

The switching mode module is used to distribute the reference voltages of dual OW inverters to each two-level inverter. In the SPWM strategy with the balanced switching mode, the relationship between the reference voltages of dual OW inverters and each two-level inverter can be expressed as

$$\begin{cases} V_{n1}^* = V_{n\_z}^* / 2 + V_{dc} / 2 \\ V_{n2}^* = -V_{n\_z}^* / 2 + V_{dc} / 2 \end{cases} \quad (n = A, B, C) \quad (4.2)$$

where  $V_{n\_z}^*$  is the reference voltage for dual OW inverters after the injection of the ZSV in an arbitrary phase,  $V_{n1}^*$  and  $V_{n2}^*$  are the reference voltages for two two-level inverters, respectively.

On the other hand, in the unbalanced switching mode, the reference voltages for two inverters in an arbitrary phase can be described as

$$\begin{cases} \begin{cases} V_{n1}^* = V_{n\_z}^* \\ V_{n2}^* = 0 \end{cases} & \text{if } V_{n\_z}^* > 0 \\ \begin{cases} V_{n1}^* = 0 \\ V_{n2}^* = -V_{n\_z}^* \end{cases} & \text{if } V_{n\_z}^* < 0 \end{cases} \quad (4.3)$$

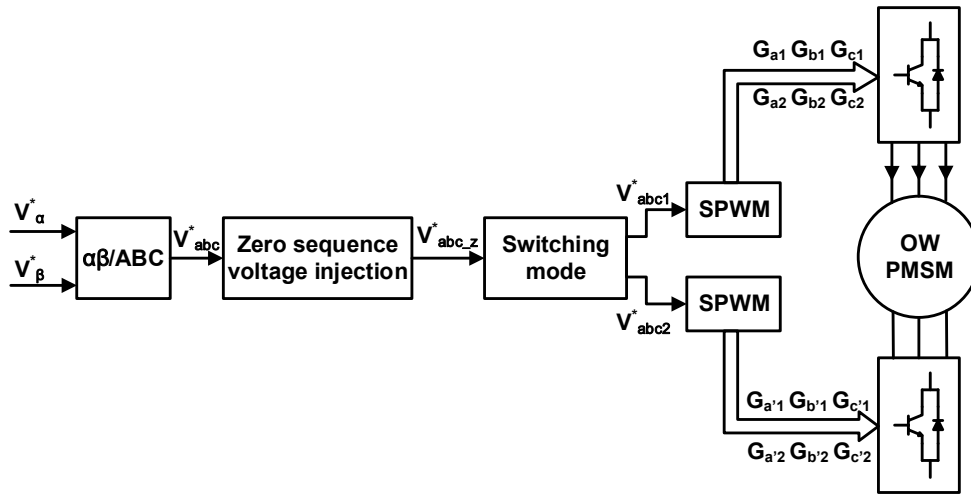
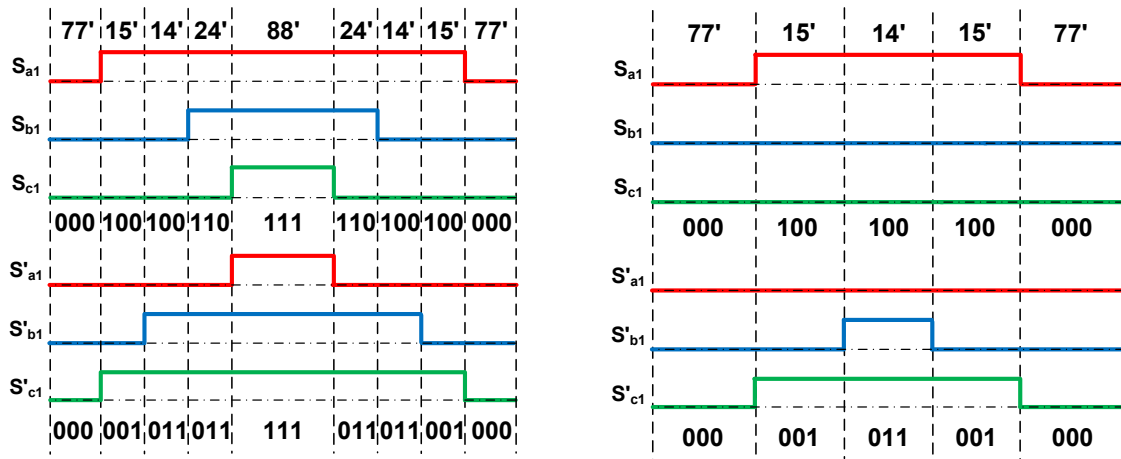


Fig. 4.1 Control diagram of SPWM strategy for dual OW inverters.

The PWM waveforms of the SPWM strategy with the balanced and unbalanced switching modes are compared in Figs. 4.2 (a) and (b). In the balanced switching mode, all switches are switched, and the SPWM strategy has the same performance as the conventional SVPWM strategy, such as the maximum modulation region and current harmonics, but the implementation is much easier, as neither the sectors nor the durations of vectors need to be calculated. In the SPWM strategy with the unbalanced switching mode, for any phase, only one of two H-bridge legs is switched, while the other leg is clamped.



(a) Balanced switching mode.

(b) Unbalanced switching mode.

Fig. 4.2 PWM waveforms of SPWM strategy.

## 4.2.2 Analysis of inverter nonlinearity in balanced and unbalanced switching modes

PWM signals can affect the switching actions of the dual OW inverters, and then the nonlinear effects of the inverters on phase voltages. Each phase of an OW machine and dual inverters can be regarded as a H-bridge, and each H-bridge can be controlled in two different switching modes, e.g. balanced and unbalanced switching modes. In the balanced mode, two legs of a H-bridge are all switched, while only one of the two legs are switched in the unbalanced mode. The nonlinear effects on the output voltages of dual OW inverters will be analysed when the balanced and unbalanced switching modes are applied, respectively.

Figs. 4.3 (a) and (b) show phase A current direction, the ideal pole voltage, actual pole voltage, and phase A actual output voltage in dual OW inverters when the balanced switching mode is applied while  $i_a > 0$ . In Inverter I, phase A current flows through  $S_{a1}$  during on period (solid arrow in Inverter I), while it flows through  $D_{a2}$  during off period and dead time (dotted arrow in Inverter I). As a result, the pole voltage of Inverter I  $V_{AO}$  in dead time is the same as that in off period while  $i_a > 0$ . It needs to note that that the directions of currents are opposite with respect to Inverters I and II. As a result, phase A current flows through  $D'_{a1}$  during on period and dead time (solid arrow in Inverter II), while it flows through  $S'_{a2}$  during off period (dotted arrow in Inverter II). Consequently, the pole voltage of Inverter II  $V_{A'O'}$  in dead time is the same as that in on period while  $i_a > 0$ .  $V_{AO}^{dt}$  and  $V_{A'O'}^{dt}$  are the pole voltages of two inverters respectively when considering the effect of dead time. It can be observed that  $V_{AO}^{dt}$  is zero during dead time, while  $V_{A'O'}^{dt}$  is  $V_{dc}$  during dead time. The different pole voltages during dead time is caused by different current directions with respect to two legs of the H-bridge. In Fig. 4.3,  $t_{on}$  and  $t_{off}$  are turn-on and turn-off times of switching devices, which includes turn-on/off delays and the average contribution of time delays caused by the effect of inverter parasitic capacitances. Due to the difference between turn-on time and turn-off time of switching devices, the pole voltages of two inverters become  $V_{AO}^{dt+tsw}$  and  $V_{A'O'}^{dt+tsw}$ , respectively. In addition, the pole voltages of two inverters are  $V_{AO}^{dt+tsw+on}$  and  $V_{A'O'}^{dt+tsw+on}$  when on-state voltages of switching devices and diodes are considered.

According to (1.4), the ideal phase A voltage  $V_{AA'}^{ideal}$  is

$$V_{AA'}^{ideal} = V_{AO}^{ideal} - V_{A'O'}^{ideal} + V_{OO'} \quad (4.4)$$

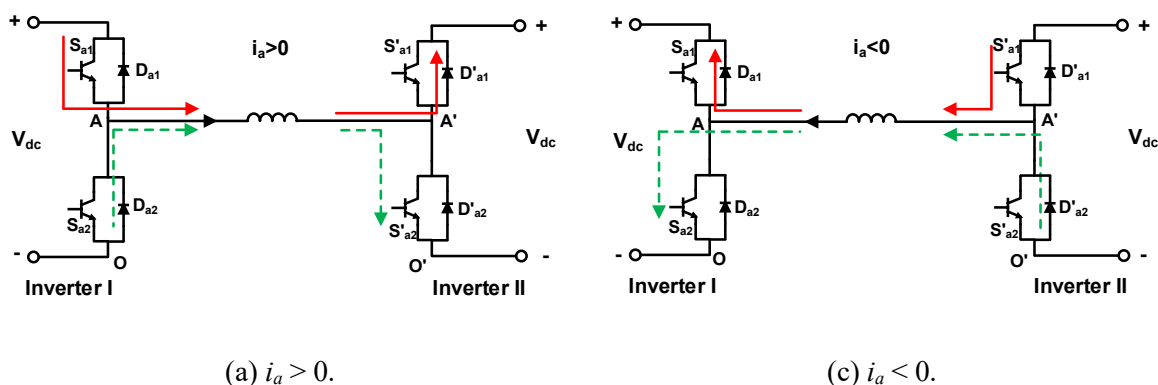
The actual phase A voltage  $V_{AA'}^{dt+tsw+on}$  is acquired as

$$V_{AA'}^{dt+tsw+on} = V_{AO}^{dt+tsw+on} - V_{A'O'}^{dt+tsw+on} + V_{OO'}. \quad (4.5)$$

As a result, the difference between ideal and actual phase voltages is

$$\begin{aligned} \Delta V_{AA'} &= V_{AA'}^{ideal} - V_{AA'}^{dt+tsw+on} \\ &= (V_{AO}^{ideal} - V_{AO}^{dt+tsw+on}) - (V_{A'O'}^{ideal} - V_{A'O'}^{dt+tsw+on}). \end{aligned} \quad (4.6)$$

The ideal and actual phase voltages, and their difference are shown in Fig. 4.3 (b) when the balanced switching mode is applied while  $i_a > 0$ . During  $i_a < 0$ , the flowing path of phase A current in dual OW inverters is shown in Fig. 4.3 (c) when the balanced switching mode is applied. Compared with Fig. 4.3 (a), the direction of current in the H-bridge inverter is opposite. As a result, the paths of currents in the two legs are exchanged when  $i_a < 0$  compared with those in  $i_a > 0$ . The ideal and actual phase voltages, and their difference can also be calculated according to (4.9) - (4.11), and are shown in Fig. 4.3 (d). It can be observed that the average error voltage in a PWM cycle between the ideal and actual phase voltages has the same sign as the phase current, and its magnitude changes according to the error between turn-on and -off times of switching devices. It is known that the magnitude of phase currents can affect the turn-on/off times of switching devices due to the effect of parasitic capacitances.



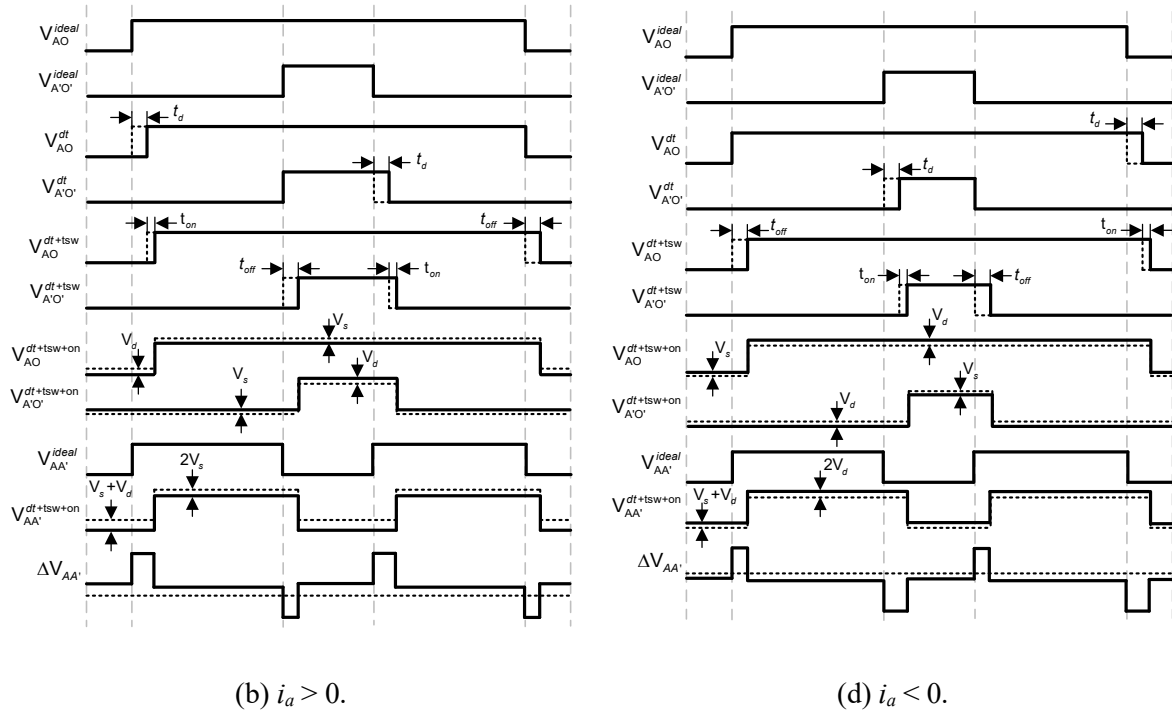
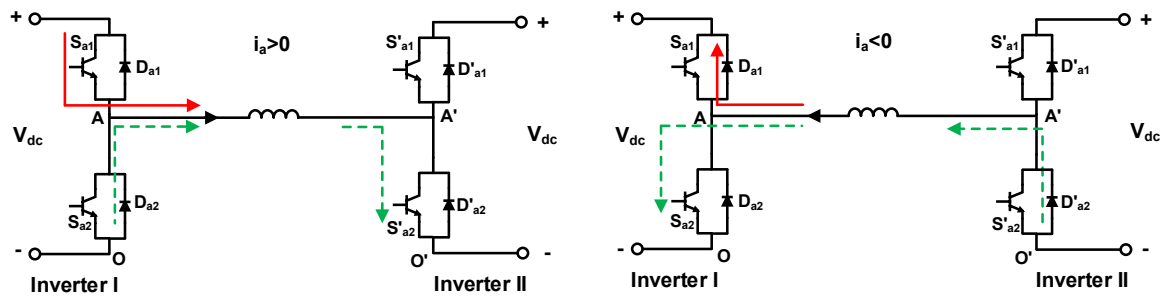


Fig. 4.3 Phase A current in dual OW inverters and output voltage in balanced switching mode.

In the unbalanced switching mode, only switches in one of two legs of an H-bridge are switched, while switches in the other leg are clamped. It needs to note that the switched leg in the unbalanced switching mode has the same nonlinearity character as that in the balanced switching mode. However, the switches in the clamped leg have no switching action, so that there is no dead time and turn-on/off times. Assuming the leg in Inverter II is clamped on low level, Fig. 4.4 (a) shows the path of phase A current in the dual OW inverters with the unbalanced switching mode when  $i_a > 0$ . As the clamping state is low, phase A current flows through  $S'_{a2}$  in the whole PWM cycle when  $i_a > 0$ . At the same time, the leg in Inverter I works the same as that in the balanced switching mode. If the unbalanced switching mode is applied, the ideal phase voltage, the actual phase voltage and their difference are shown in Fig. 4.4 (b) when  $i_a > 0$ . Figs. 4.4 (c) and (d) show the phase A current in an H-bridge inverter and output voltages when  $i_a < 0$ , respectively. Phase A current flows through  $D'_{a2}$  in the whole PWM cycle, while the leg in Inverter I works the same as that in the balanced switching mode.

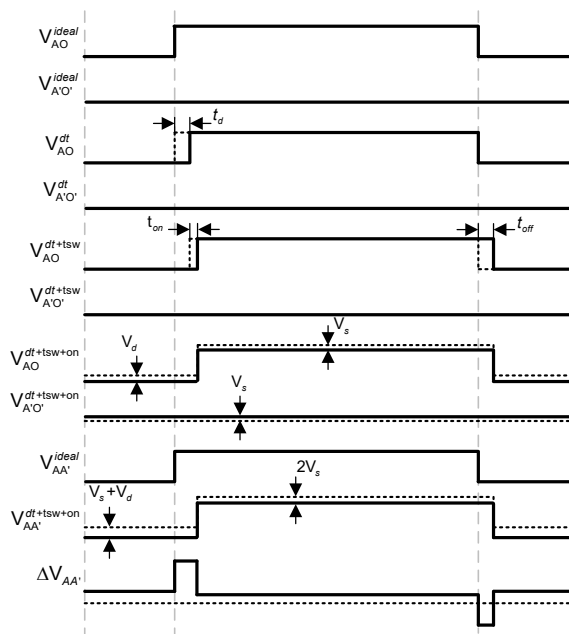
Due to the switching of the two H-bridge legs in the balanced switching mode, the dead time and turn-on/off times cause voltage distortions in the pole voltages of two legs. In the unbalance switching mode, only one of the two H-bridge legs is switched, and thus, there is no dead time and turn-on/off times in the clamped leg, and the dead time and turn-on/off times only cause voltage distortion in the pole voltage of the switched leg. As a result, according to phase

voltages in (1.4), the distortions of phase voltages are different in the balanced and unbalanced switching modes and will be analysed in detail as follows.

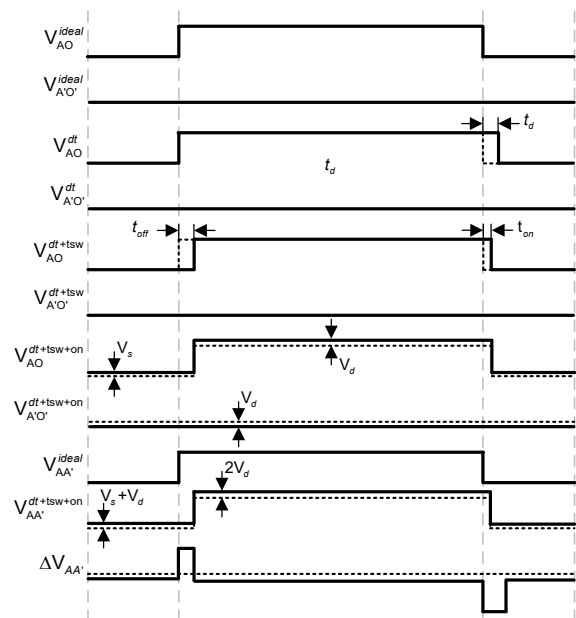


(a) Phase A current in dual OW inverters ( $i_a > 0$ ).

(c) Phase A current in dual OW inverters ( $i_a < 0$ ).



(b) Output voltage ( $i_a > 0$ ).



(d) Output voltage ( $i_a < 0$ ).

Fig. 4.4 Phase A current in dual OW inverters and output voltage in unbalanced switching mode.

The error voltages caused by inverter nonlinearity in two inverters can be expressed as

$$\begin{aligned} V_{e1} &= V_{d1} + V_{sw1} + V_{on1} \\ V_{e2} &= V_{d2} + V_{sw2} + V_{on2} \end{aligned} \quad (4.7)$$

where  $V_{d1}$  and  $V_{d2}$ ,  $V_{sw1}$  and  $V_{sw2}$ ,  $V_{on1}$  and  $V_{on2}$  are the error voltages caused by dead time, turn-on and turn-off times, on-state voltages of Inverters I and II, respectively.

Thus, the error voltage in the dual OW inverters is

$$V_e = V_{e1} - V_{e2} = (V_{d1} - V_{d2}) + (V_{sw} - V_{sw2}) + (V_{on1} - V_{on2}). \quad (4.8)$$

For the balanced switching mode, these voltages can be expressed as

$$V_{d1} - V_{d2} = \frac{2t_d}{T_s} V_{dc} \text{sign}(i_n) \quad (4.9)$$

$$V_{sw1} - V_{sw2} = \frac{2(t_{on} - t_{off})}{T_s} V_{dc} \text{sign}(i_n) \quad (4.10)$$

$$V_{on1} - V_{on2} = (V_s + V_d) \text{sign}(i_n) + \frac{T_{nOon} - T_{n'O'on} - 2\Delta T \text{sign}(i_n)}{T_s} (V_s - V_d) \quad (4.11)$$

$$V_{ne\_b} = \left[ \frac{2(V_{dc} + V_d - V_s) \Delta T}{T_s} + (V_s + V_d) \right] \text{sign}(i_n) + (V_s - V_d) \frac{T_{nOon} - T_{n'O'on}}{T_s} \quad (4.12)$$

where  $t_d$  is the dead time,  $t_{on}$  and  $t_{off}$  are the turn-on and turn-off times of switching devices,  $T_{nOon}$  and  $T_{n'O'on}$  are the ideal on state times of upper switches in two legs of an arbitrary phase respectively,  $\Delta T = t_d + t_{on} - t_{off}$ ,  $T_s$  is the duration of a PWM cycle,  $i_n$  is the current of an arbitrary phase,  $V_s$  and  $V_d$  are the voltage drops of switches and diodes, respectively.

The voltage drops of active switches and diodes can be expressed as [PEL10]

$$\begin{aligned} V_s &= V_{s0} + r_s |i_n| \\ V_d &= V_{d0} + r_d |i_n| \end{aligned} \quad (4.13)$$

where  $V_{s0}$  and  $V_{d0}$  are the threshold voltages of the active switches and diodes respectively,  $r_s$  and  $r_d$  are the ON-state slope resistances of switches and diodes respectively.

The ON-state slope resistances can be assumed as a part of the resistance of electrical machine. Besides,  $V_s - V_d$  is neglected due to the low magnitude. The error voltage in an arbitrary phase can be rewritten as

$$V_{ne\_b} \approx \left[ \frac{2(V_{dc} + V_d - V_s) \Delta T}{T_s} + (V_{s0} + V_{d0}) \right] \cdot \text{sign}(i_n). \quad (4.14)$$

On the other hand, for the unbalanced switching mode, these voltages can be expressed as

$$V_{d1} - V_{d2} = \frac{t_d}{T_s} V_{dc} \text{sign}(i_n) \quad (4.15)$$

$$V_{sw1} - V_{sw2} = \frac{t_{on} - t_{off}}{T_s} V_{dc} \text{sign}(i_n) \quad (4.16)$$

$$V_{on1} - V_{on2} = (V_s + V_d) \text{sign}(i_n) + \frac{T_{nOon} - T_{n'O'on} - \Delta T \text{sign}(i_n)}{T_s} (V_s - V_d) \quad (4.17)$$

$$\begin{aligned} V_{ne\_ub} &= \left[ \frac{(V_{dc} + V_d - V_s) \Delta T}{T_s} + (V_s + V_d) \right] \text{sign}(i_n) + (V_s - V_d) \frac{T_{nOon} - T_{n'O'on}}{T_s} \\ &\approx \left[ \frac{(V_{dc} + V_d - V_s) \Delta T}{T_s} + (V_{s0} + V_{d0}) \right] \text{sign}(i_n) \end{aligned} \quad (4.18)$$

It needs to note that  $T_{nOon} - T_{n'O'on}$  will be the same for the two switching modes given the same reference voltage.

$$T_{nOon} - T_{n'O'on} = \frac{V_n^*}{V_{dc}} T_s \quad (4.19)$$

where  $V_n^*$  is the reference voltage for dual OW inverters in an arbitrary phase.

The difference between the error voltages with balanced and unbalanced switching modes in an arbitrary phase is

$$V_{nd} = V_{ne\_b} - V_{ne\_ub} = \frac{(V_{dc} + V_d - V_s) \Delta T}{T_s} \bullet \text{sign}(i_n). \quad (4.20)$$

As the threshold voltages are constant values in the error voltages and can be compensated separately, the two error voltages in (4.14) and (4.18) can be divided into nonlinearity and linearity components as

$$V_{ne\_b}^1 = \frac{2(V_{dc} + V_d - V_s) \Delta T}{T_s} \bullet \text{sign}(i_n) \quad V_{ne\_b}^2 = (V_{s0} + V_{d0}) \bullet \text{sign}(i_n) \quad (4.21)$$

$$V_{ne\_ub}^1 = \frac{(V_{dc} + V_d - V_s) \Delta T}{T_s} \bullet \text{sign}(i_n) \quad V_{ne\_ub}^2 = (V_{s0} + V_{d0}) \bullet \text{sign}(i_n) \quad (4.22)$$



where  $V_{ne\_b}^1$  and  $V_{ne\_ub}^1$  are the nonlinearity components of error voltages in the balanced and unbalanced modes, respectively.  $V_{ne\_b}^2$  and  $V_{ne\_ub}^2$  are the linearity components of error voltages in the balanced and unbalanced modes, respectively.

It can be observed that the linearity components of the two error voltages are the same, while the nonlinearity component in the balanced mode is twice of that in the unbalanced mode. The nonlinearity and linearity components will be compensated separately in the proposed strategy. The equivalent compensation time for the nonlinearity component is  $T_c$ , and then (4.20), (4.21) and (4.22) can be rewritten as

$$V_{ne\_b}^{1'} = \frac{2(V_{dc} + V_d - V_s)(\Delta T - T_c)}{T_s} \cdot \text{sign}(i_n) \quad (4.23)$$

$$V_{ne\_ub}^{1'} = \frac{(V_{dc} + V_d - V_s)(\Delta T - T_c)}{T_s} \cdot \text{sign}(i_n) \quad (4.24)$$

$$V_{nd}' = \frac{(V_{dc} + V_d - V_s)(\Delta T - T_c)}{T_s} \cdot \text{sign}(i_n). \quad (4.25)$$

The linearity component can be compensated simply, but the nonlinearity component is difficult to be compensated since it varies according to operation conditions. According to (4.23) and (4.24), the nonlinearity component  $V_{ne\_b}^{1'}$  in the balanced mode is twice of  $V_{ne\_ub}^{1'}$  in the unbalanced mode. As a result, the difference between two error voltages of balanced and unbalanced switching modes  $V_{nd}'$  in (4.25) equals the nonlinearity component  $V_{ne\_ub}^{1'}$  in the unbalanced mode, and is half of the nonlinearity component  $V_{ne\_b}^{1'}$  in the balanced mode. The relationship between  $V_{ne\_b}^{1'}$ ,  $V_{ne\_ub}^{1'}$ , and  $V_{nd}'$  can be expressed as

$$\begin{aligned} V_{ne\_b}^{1'} &= 2V_{nd}' \\ V_{ne\_ub}^{1'} &= V_{nd}' \end{aligned} \quad (4.26)$$

Consequently, the nonlinearity component of error voltages in dual inverters can be compensated by the difference between the error voltages in balanced and unbalanced switching modes. The nonlinearity component is difficult to be calculated directly, but can be accurately acquired from the difference between two error voltages of balanced and unbalanced switching modes.

If the compensation is perfect,  $T_c$  is equal to  $\Delta T$  ; If the inverter nonlinearity is undercompensated, then  $T_c$  is smaller than  $\Delta T$  ; If the inverter nonlinearity is overcompensated, then  $T_c$  is larger than  $\Delta T$  . According to (4.25), the voltage differences  $V'_{nd}$  between two switching modes is zero when a full compensation is achieved, while it has the same sign as the phase current for the under compensation and the opposite sign for the over compensation. As a result, the voltage differences  $V'_{nd}$  can reflect the accuracy of compensation voltages for inverter nonlinearity. It is worth noting that in the conventional current harmonics based online inverter nonlinearity compensation methods, current harmonics in  $dq$ -axes cannot distinguish the over and under compensation. Therefore, in this chapter, a novel online inverter nonlinearity compensation strategy will be proposed based on the alternately applying balanced and unbalanced switching modes in dual two-level OW inverters.

### 4.3 Proposed Inverter Nonlinearity Compensation Strategy

A high frequency switching technique between the balanced and unbalanced switching modes for the SPWM strategy is proposed in this section to extract inverter nonlinearity characteristics and subsequently utilized for the inverter nonlinearity compensation in an OW machine fed by dual two-level three phase inverters. This switching frequency between the balanced and unbalanced switching modes is designated as the mode-switching frequency to avoid potential confusion with the PWM switching frequency. If the inverter nonlinearity is undercompensated or overcompensated, ripples will appear in phase voltages due to the difference between the error voltages caused by inverter nonlinearity in the balanced and unbalanced switching modes, with the frequency of ripple voltages being the mode-switching frequency. On the other hand, if inverter nonlinearity is compensated completely, the abovementioned ripple voltages will disappear.

With the current closed-loop control, the reference voltages are the outputs of current PI regulators. Ripple voltages can be reflected in the reference voltages, and thus, the high frequency ripple voltages can be extracted from the reference voltages to regulate the compensation voltages for inverter nonlinearity. The mode-switching frequency between balanced and unbalanced switching modes needs to be set much higher than the electrical frequency, so that reference voltages can be regarded as the same for both the balanced and unbalanced switching modes. If the mode-switching frequency is close to the electrical frequency, the compensation performance will be degraded. On the other hand, the mode-

switching cycle must be an even multiple of the PWM cycle. As a result, an appropriate mode-switching frequency should be chosen. In this chapter, the PWM frequency is 10kHz, and the mode-switching frequency is set as 1kHz.

The control diagram of the proposed inverter nonlinearity compensation strategy is shown in Fig. 4.5. A mode-switching signal at the above selected frequency is used to determine the balanced or unbalanced switching mode. The balanced or unbalance switching mode module distributes the reference voltages of dual inverters to the reference voltages of each two-level inverter according to the mode-switching signal. The inverter nonlinearity compensation module extracts ripple voltages from the reference voltages according to the mode-switching signal, and generates the inverter nonlinearity compensation voltages. Fig. 4.6 shows the details of the inverter nonlinearity compensation module. To extract voltage ripples caused by the mode-switching between the balanced and unbalanced switching modes, a band pass filter (BPF) is used.  $V_{bpf}^*$  is the high frequency reference voltage signal after the BPF. Figs. 4.7 (a) and (b) show the mode-switching signal and the high frequency reference voltage signal after the BPF with over inverter nonlinearity compensation when  $i_a > 0$  and  $i_a < 0$ , respectively. Fig. 4.8 and Fig. 4.9 show the mode-switching signal and the high frequency reference voltage signal after the BPF with full and under compensation, respectively. When the unbalanced switching mode is applied, the mode-switching signal is 1, while it is -1 when the balanced switching mode is applied. It can be observed that voltage ripples have the same frequency as the mode-switching signal.

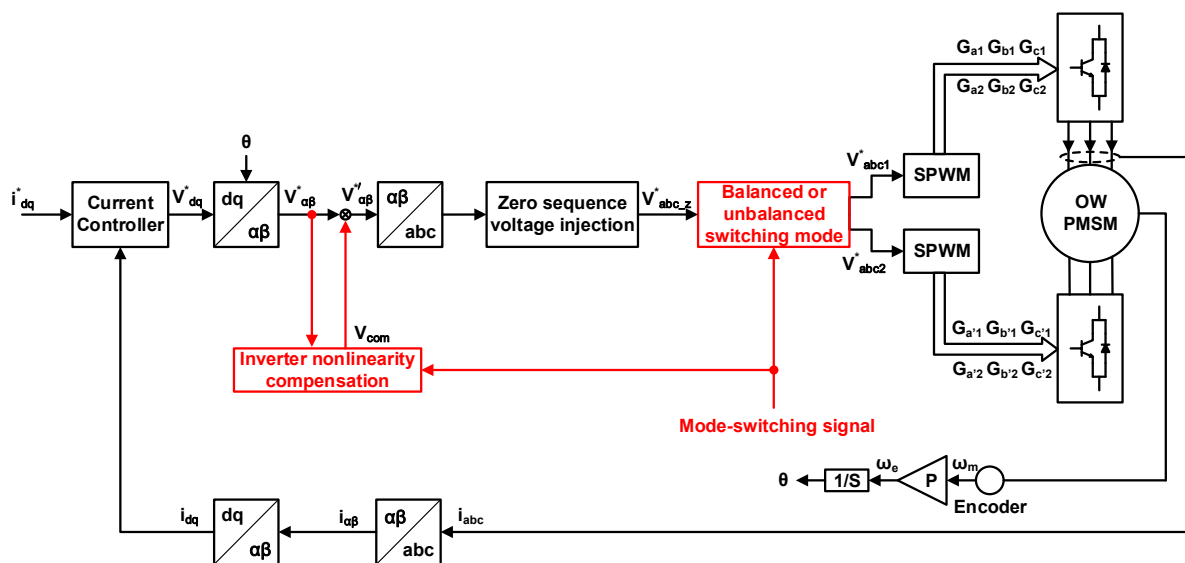


Fig. 4.5 Control diagram of OW drive based on proposed inverter nonlinearity compensation strategy.

In Figs. 4.7-9, the extremum values of the ripple voltage in the duration of two switching modes are used to calculate the fluctuation as

$$V_{nfluc} = V_{nex\_b} - V_{nex\_ub} \quad (4.27)$$

where  $V_{nfluc}$  is the fluctuation of the ripple voltage in an arbitrary phase,  $V_{nex\_ub}$  and  $V_{nex\_b}$  are the extremum values of the ripple voltage with unbalanced and balanced switching modes in an arbitrary phase, respectively.

It needs to note that the extremum value of the unbalanced switching mode appears at the first sample cycle of the balanced switching mode, as the one step delay in the discrete control system, and vice versa. The extremum values are highlighted in Figs. 4.7-9. Equation (4.27) is the algorithm of the fluctuation calculation module in Fig. 4.6. Reference voltage ripples are caused by the different voltage distortions between the two switching modes, and thus  $V_{nfluc}$  can be used to regulate three-phase compensation voltages for inverter nonlinearity. The fluctuation signal  $V_{nfluc}$  will be sent into a PI regulator, and its output is the voltage difference between the two switching modes, and can also be expressed as

$$V_{nd}' = \left( K_p + \frac{K_i}{s} \right) \bullet V_{nfluc} \quad (4.28)$$

where  $K_p$  and  $K_i$  are the proportional and integral gains of the PI regulator.

According to (4.26), the nonlinearity component of compensation voltages in the two switching modes can be expressed as

$$V_{ne\_b}' = 2 \left( K_p + \frac{K_i}{s} \right) \bullet V_{nfluc} \quad (4.29)$$

$$V_{ne\_ub}' = \left( K_p + \frac{K_i}{s} \right) \bullet V_{nfluc} \quad (4.30)$$

According to (4.21) and (4.22), the compensation voltages in two switching modes consist of nonlinearity and linearity components in Fig. 4.6. The linearity components are threshold voltages multiplying with the sign of phase currents, and are the same for two switching modes. The nonlinearity components can be acquired from the outputs of PI regulators in (4.29) and

(4.30), and a double gain is needed for the balanced switching mode. The voltage selection module selects the compensation voltages for two switching modes. Finally, three-phase compensation voltages should be transformed to  $\alpha\beta$ -axes.

Distortion voltages are the error voltages between the actual output voltages and the reference voltages before compensation. From (4.23) and (4.24), it can be observed that nonlinearity distortion voltages are zero when a full compensation is applied, while they have the same sign with phase currents in the under-compensation and the opposite sign in the over compensation. For the convergence of the close loop compensation, the sign of the PI regulator input  $V_{nfluc}$  should always be the same as the sign of the distortion voltage. According to Figs. 4.7-9, the signs of the PI regulator input and the distortion voltage which needs to be compensated are shown in Table 4.1. It can be observed that the signs of the PI regulator input and the distortion voltage are always the same. As a result, the outputs of the PI regulator can always reduce the absolute value of distortion voltages, so that the close loop inverter nonlinearity compensation can converge precisely.

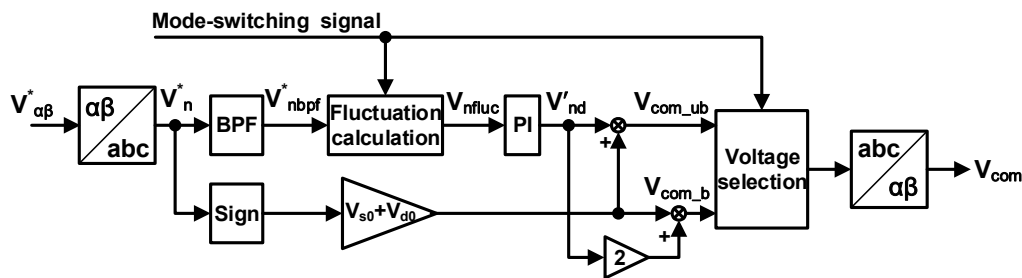


Fig. 4.6 Control diagram of inverter nonlinearity compensation module.

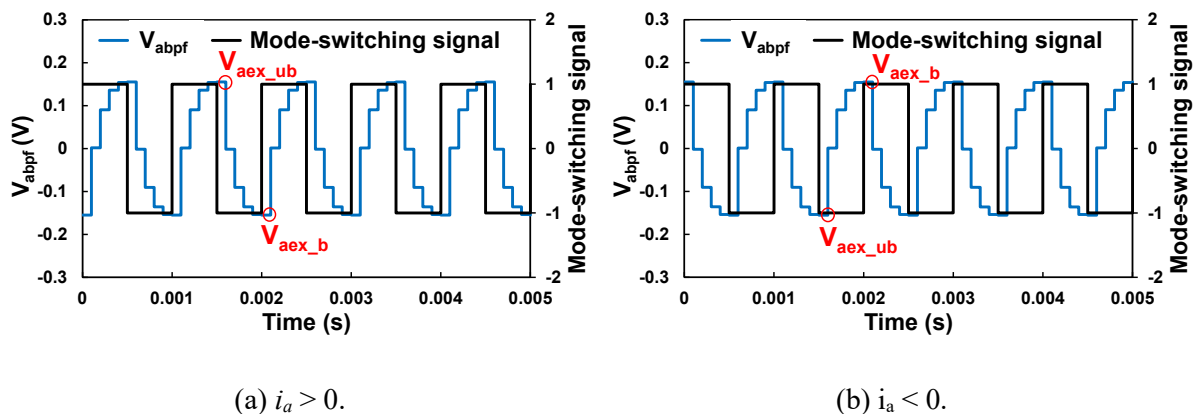


Fig. 4.7 Bandpass filtered phase A reference voltage and mode-switching signal with over compensation.

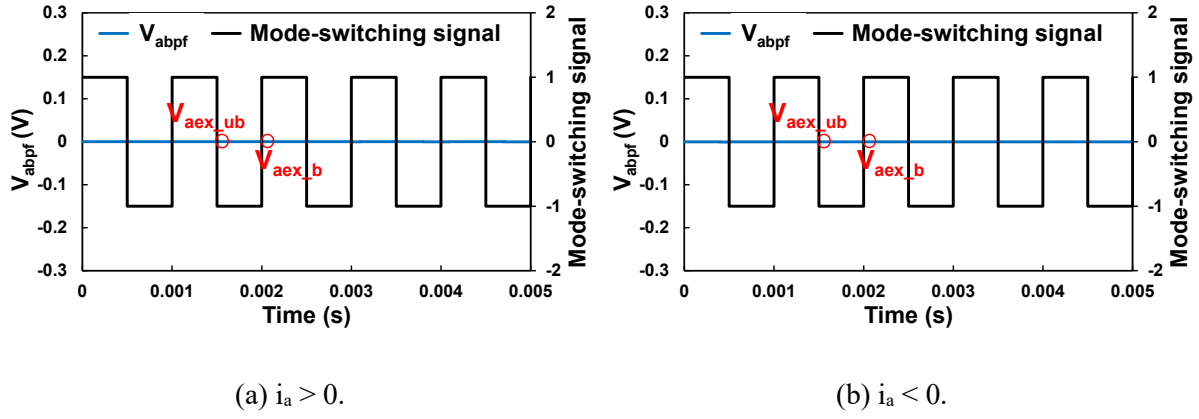


Fig. 4.8 Bandpass filtered phase A reference voltage and mode-switching signal with full compensation.

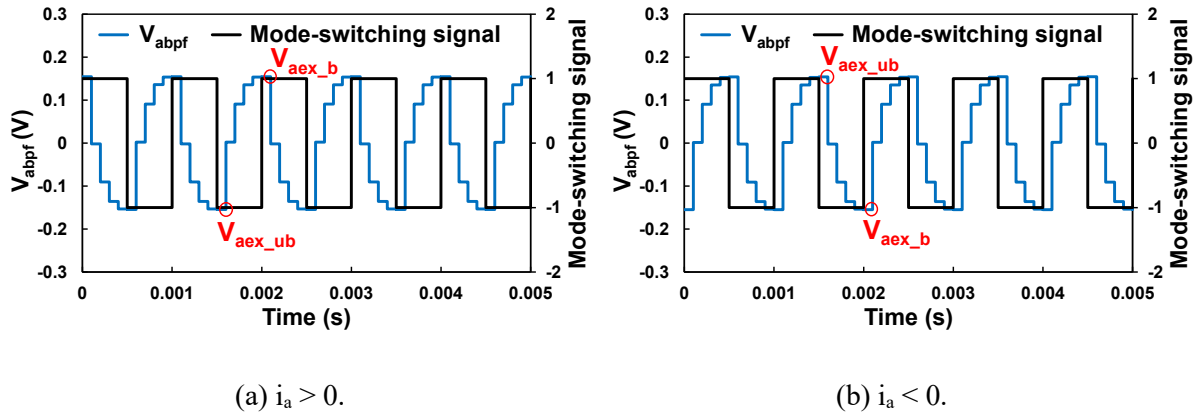


Fig. 4.9 Bandpass filtered phase A reference voltage and mode-switching signal with under compensation.

Inverter nonlinearity can cause current harmonics, among which the main components are the 5<sup>th</sup> and 7<sup>th</sup> harmonics in phase currents or the 6<sup>th</sup> harmonic in  $dq$ -axis currents. In the conventional current harmonic-based online compensation strategies, the magnitude of the 6<sup>th</sup> harmonic in  $d$ -axis current is extracted to regulate the amplitude of preset compensation voltage curves [PAR12] [PAR14] [ZHA04] [LIU14]. As the 6<sup>th</sup> harmonic cannot generate full compensation curves, but can only regulate a parameter of preset curves, the compensation performance and robustness of parameter variation are limited by the preset curves. Moreover, since both inverter nonlinearity and nonideal back EMF can cause the 6<sup>th</sup> harmonic in  $dq$ -axis currents, it is impossible to separate them in conventional current harmonic-based online compensation strategies. Furthermore, the frequency of the 6<sup>th</sup> harmonic is determined by the electrical frequency, and thus the convergence of compensation voltages is also affected by the electrical frequency, which may cause low response in the low electrical frequency operation.

Finally, the accurate rotor position is needed in conventional methods, which can degrade the compensation performance in the sensorless control.

Table 4.1 Sign of PI Regulator Input and Distortion Voltage

Compensation state	Direction of phase current	Input of PI regulator $V_{nfluc} = V_{nex\_b} - V_{nex\_ub}$	Distortion voltage
Over	$i_n > 0$	Negative	Negative
	$i_n < 0$	Positive	Positive
Under	$i_n > 0$	Positive	Positive
	$i_n < 0$	Negative	Negative

To solve issues in conventional inverter nonlinearity compensation methods, a novel compensation strategy is proposed in this chapter. Different voltage distortions from inverter nonlinearity between two switching modes of SPWM strategy are utilized to generate inverter nonlinearity compensation voltages without preset compensation voltage curves. Furthermore, as the turn-on/off times depend on phase currents and temperature, it changes according to the operation condition. The performance of the proposed inverter nonlinearity compensation is inherently reflected in the fluctuation of reference voltages at the designed mode-switching frequency. Consequently, the change of operation condition has no influence on the proposed compensation strategy. Besides, the high frequency reference voltage ripples are only caused by the under or over inverter nonlinearity compensation, and are not affected by non-ideal back EMF, as the variation of back EMF can be ignored in the high mode-switching frequency. Moreover, the proposed inverter nonlinearity compensation method is applied in the stationary coordinate system and has no need of the accurate rotor position.

#### 4.4 Experiment Results

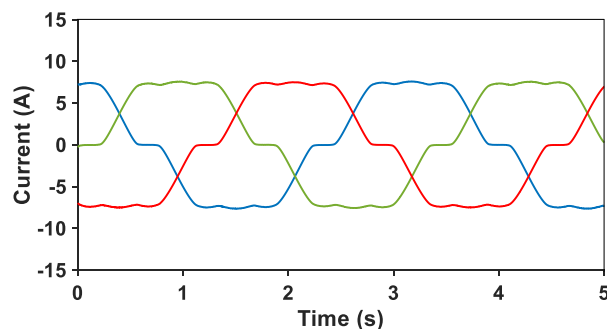
The proposed inverter nonlinearity compensation strategy with dual switching modes is validated in an OW-PWSM. The parameters of the prototype machine are shown in Table 3.6. The OW machine is driven by dual two-level inverters with two isolated DC power supplies. The PWM frequency, current loop frequency and the sampling frequency are 10kHz, and the

dead-time is set to  $2\mu\text{s}$ . The DC-bus voltage is 30V. Fig. 3.9 shows the experiment platform including a dSPACE, dual two-level inverters, an OW-PMSM, a load machine and an encoder for rotor position sensing. The parameters of the IGBT(STGIPS20C60) are shown in Table 4.2.

Table 4.2 Parameters of IGBT

Symbol	Parameter	Value
$V_s$	Collector-emitter saturation voltage (V)	1.6
$V_d$	Diode forward voltage (V)	1.9
$T_{on}$	Turn-on time (ns)	390
$T_{off}$	Turn-off time (ns)	970

Two different switching modes, i.e. balanced and unbalanced modes, are used in an OW driver to generate different PWM patterns in this chapter. Different switching actions in a PWM cycle in two switching modes cause different inverter nonlinearity, and current harmonics will be compared experimentally. The prototype OW machine fed by isolated DC-bus dual two-level inverters is controlled with the SPWM strategy shown in Fig. 4.1. Measured three phase current waveforms and spectra of balanced and unbalanced switching modes without inverter nonlinearity compensation are shown in Fig. 4.10 and Fig. 4.11, respectively. Since inverter nonlinearity is affected by the current magnitude, balanced and unbalanced switching modes are compared with the same phase current magnitude 7.5A. It can be observed that three phase currents are distorted and large 5<sup>th</sup> and 7<sup>th</sup> harmonics exist in phase current in both switching modes. However, the magnitudes of current harmonics in the balanced switching mode are larger than those in the unbalanced switching mode, since the effects of inverter nonlinearity on phase voltages in the balanced switching mode are larger than that in the unbalanced switching mode.





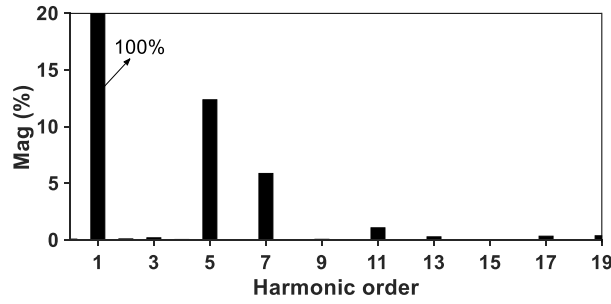


Fig. 4.10 Three phase current waveforms and spectra of balanced switching mode without inverter nonlinearity compensation.

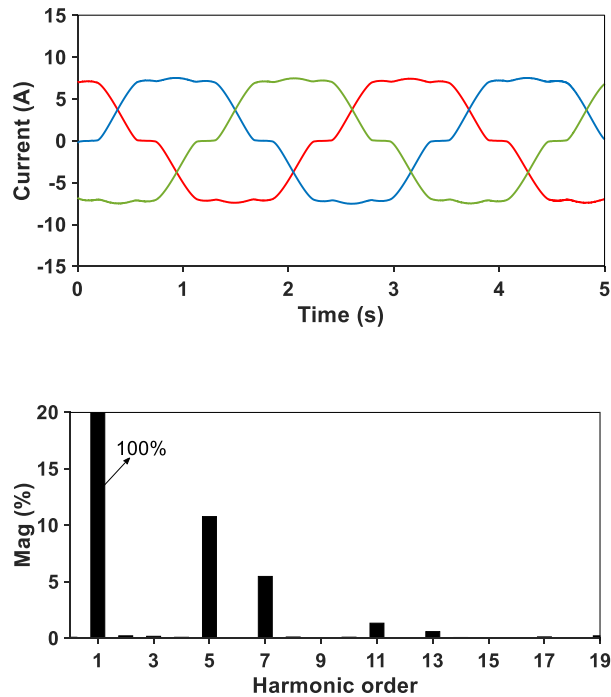
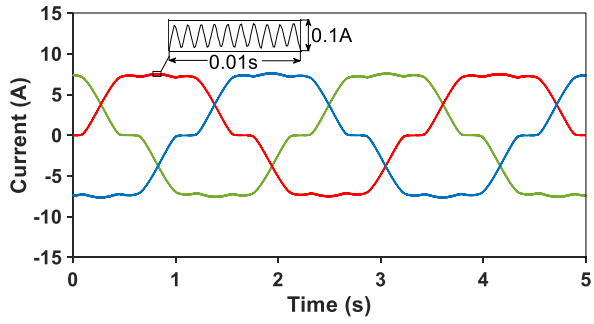


Fig. 4.11 Three phase current waveforms and spectra of unbalanced switching mode without inverter nonlinearity compensation.

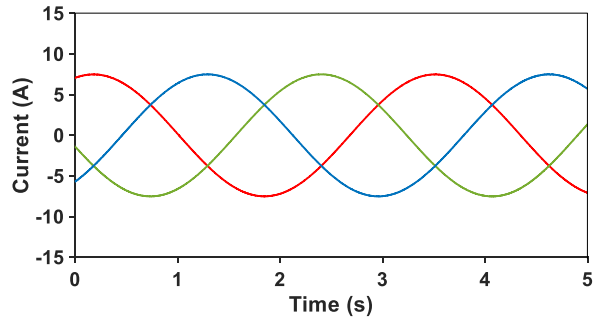
If the balanced and unbalanced switching modes are applied alternately and the inverter nonlinearity is not compensated correctly, an extra harmonic whose frequency is identical with the mode-switching frequency will be introduced. The mode-switching frequency between balanced and unbalanced switching modes is 1kHz in the experiment. To make a fair comparison with a single balanced or unbalanced mode, the magnitude of phase currents is 7.5A when the mode-switching is applied, which is the same as that in Figs. 4.10 and 4.11. When balanced and unbalanced switching modes are applied alternately, Fig. 4.12 (a) shows the measured three phase currents, while Figs. 4.12 (b) and (c) show current spectra without inverter nonlinearity compensation in low- and high-frequency regions, respectively. It can be

observed that there are the 5<sup>th</sup>, 7<sup>th</sup> and 1kHz harmonics in the current spectrum, and the magnitudes of the 5<sup>th</sup> and 7<sup>th</sup> harmonics are larger than those in the balanced mode but smaller than those in the unbalance mode. With the current closed-loop control, ripple voltages can be reflected in the  $dq$ -axis reference voltages that are the outputs of current PI regulators. After the inverse Park transformation, reference voltages are converted to  $\alpha\beta$ -axes from  $dq$ -axes. Fig. 4.13 (a) shows the ripple voltages in  $\alpha\beta$ -axis reference voltages with current closed-loop control, but without the inverter nonlinearity compensation. It can be seen that 1kHz ripple voltages exist in reference voltages. According to (4.32), fluctuation values of ripple voltages in three phases can be calculated, as shown in Fig. 4.13 (b).

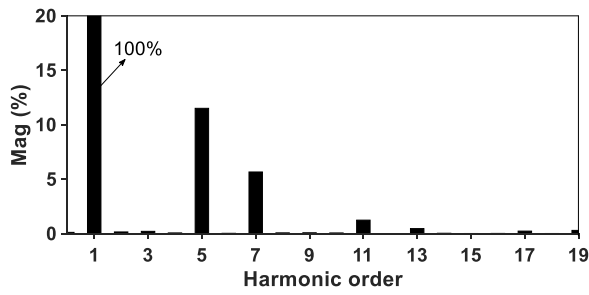
The above-mentioned 1kHz ripple in phase currents or reference voltages is caused by the different inverter nonlinearity characteristic in two switching modes, when the inverter nonlinearity is undercompensated or overcompensated. With complete compensation of inverter nonlinearity, the difference between the error voltages in balanced and unbalanced switching modes is zero, and the ripple is eliminated. With the proposed online inverter nonlinearity compensation method, the OW machine fed by isolated DC-bus dual two-level inverters is controlled as shown in Fig. 4.5. The balanced and unbalanced modes are applied alternately, and different inverter nonlinearities in the two switching modes are utilized for inverter nonlinearity compensation. To make a fair comparison, phase currents are also controlled in the magnitude 7.5A. When the proposed inverter nonlinearity compensation is applied, Fig. 4.12 (d) shows the measured three phase currents, and Figs. 4.12 (e) and (f) show current spectra in low- and high-frequency regions, respectively. It can be observed that the 1kHz harmonic in phase current is eliminated. At the same time, the 5<sup>th</sup> and 7<sup>th</sup> harmonics in phase current which are caused by inverter nonlinearity are also eliminated by the proposed control strategy. Figs. 4.13 (c) and (d) show  $\alpha\beta$ -axis reference voltages before compensation and three phase fluctuation values, respectively, with both current closed-loop control and the proposed inverter nonlinearity compensation. It can be observed that ripple voltages are eliminated in reference voltages before compensation. As a result, with the proposed inverter nonlinearity compensation, there is no ripple in both phase currents and reference voltages before compensation, although two different switching modes are applied alternately.



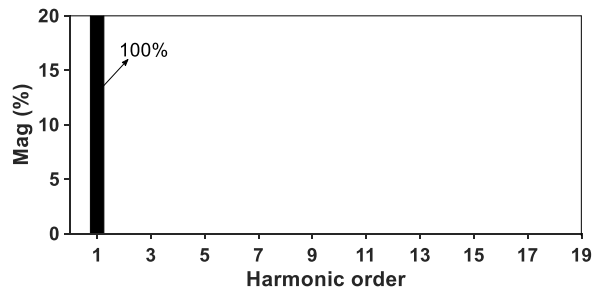
(a) Three phase current without compensation.



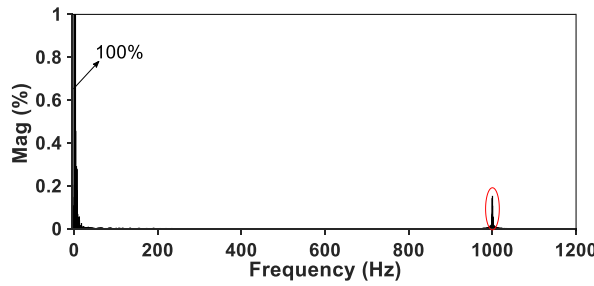
(d) Three phase current with compensation.



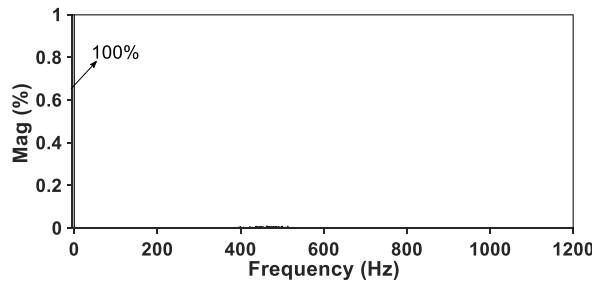
(b) Spectra in low frequency regions without compensation.



(e) Spectra in low frequency regions with compensation.

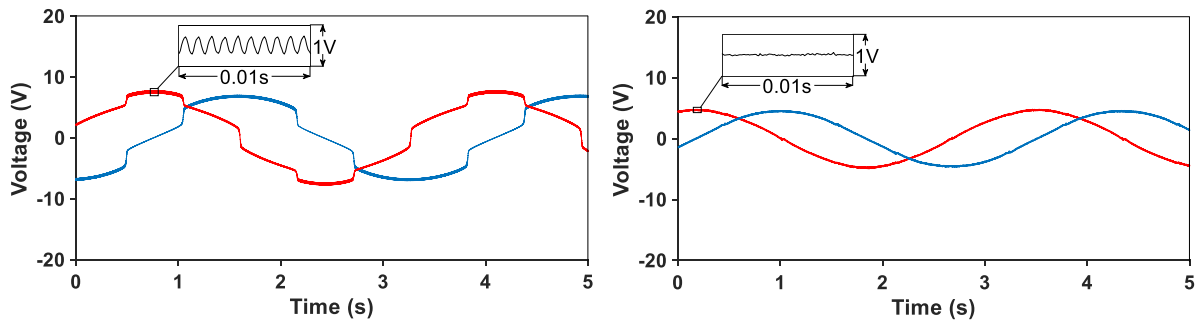


(c) Spectra in high frequency regions without compensation.



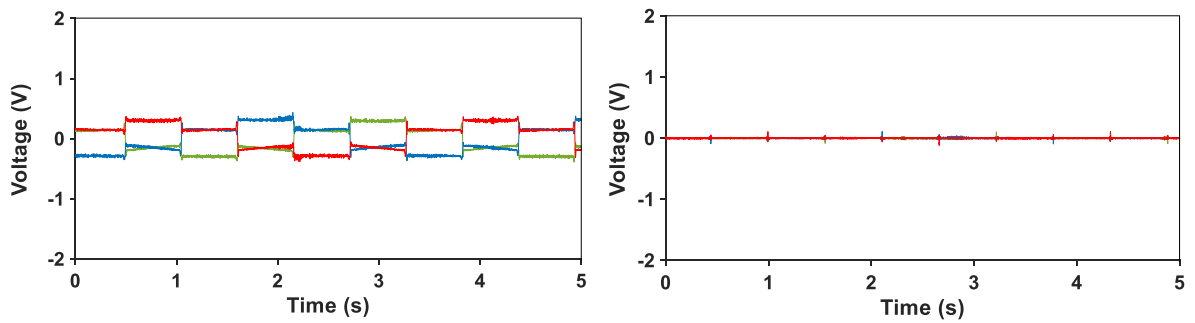
(f) Spectra in high frequency regions with compensation.

Fig. 4.12 Three phase current waveforms and spectra with the mode-switching.



(a)  $\alpha\beta$ -axis reference voltages without compensation.

(c)  $\alpha\beta$ -axis reference voltages before compensation.

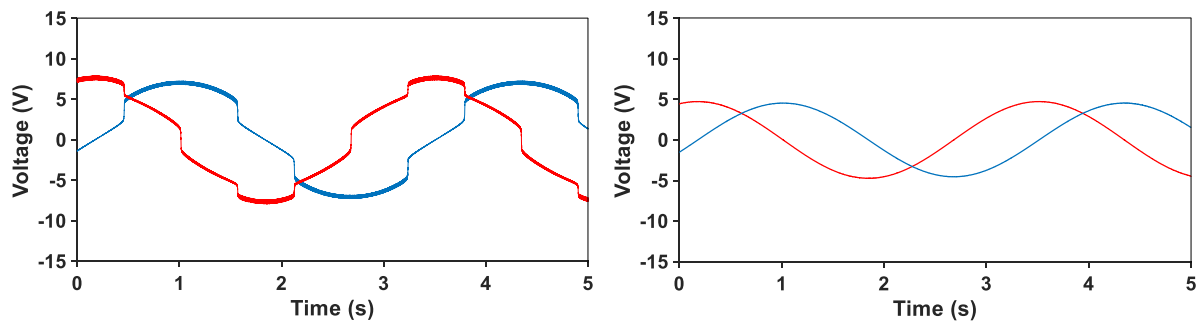


(b) Three phase fluctuation values without compensation.

(d) Three phase fluctuation values with compensation.

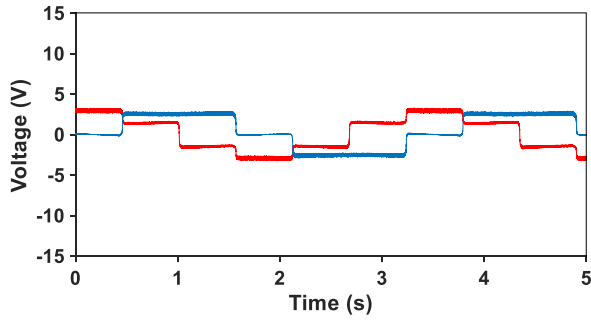
Fig. 4.13 Ripple voltages in reference voltages with current close loop.

Figs. 4.14 (a) and (b) show the reference voltages in  $\alpha\beta$ -axes after the proposed inverter nonlinearity compensation and actual output voltage, respectively. With correct compensation voltages, which is shown in Fig. 4.14 (c), the reference voltages before compensation are sinusoidal waves, as shown in Fig. 4.13 (c). Error voltages between the actual output voltages and the reference voltages before compensation are shown in Fig. 4.14 (d), and voltage errors can always keep low. As a result, the proposed inverter nonlinearity compensation method can correctly generate compensation voltages.

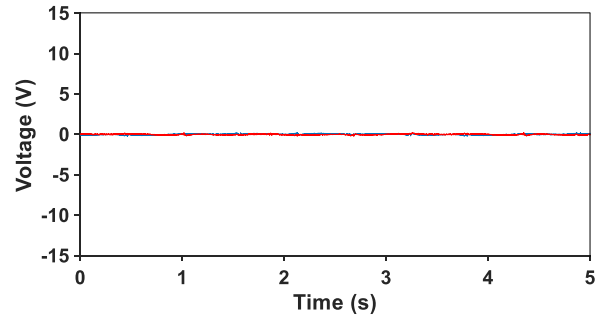


(a) Reference voltages after compensation.

(b) Actual output voltage.



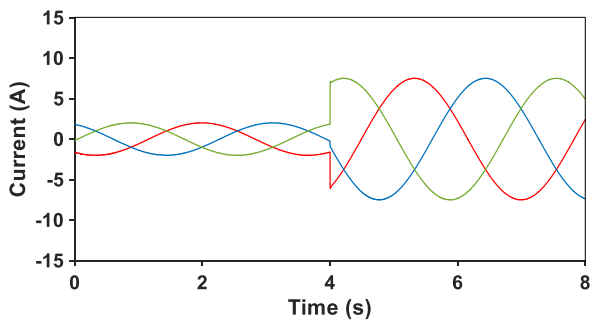
(c) Compensation voltages.



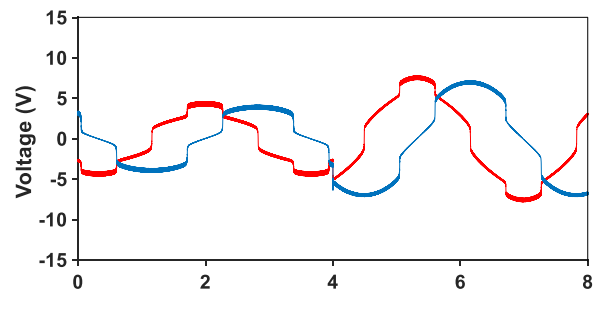
(d) Error voltages.

Fig. 4.14 Reference voltages, compensation voltages, actual output voltage and error voltages of the proposed strategy in  $\alpha\beta$ -axes (0.3Hz electrical frequency, 1kHz mode-switching frequency).

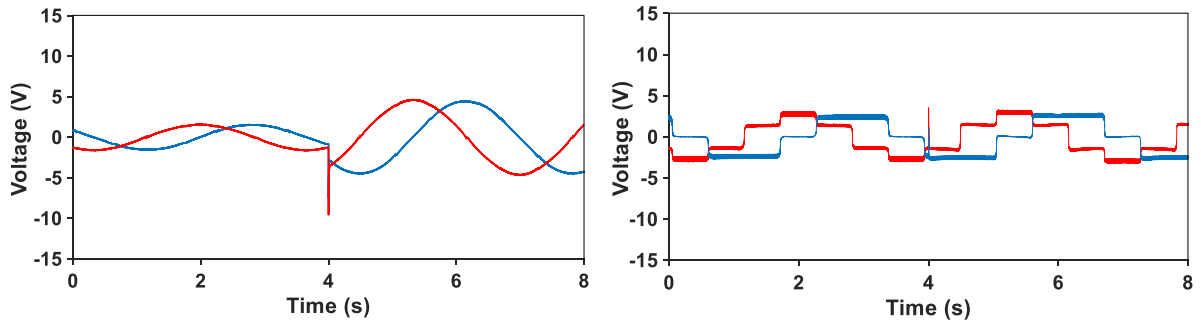
Fig. 4.15 (a) shows three phase currents of the proposed inverter nonlinearity compensation method with a current step from 2A to 7.5 A. The reference voltages after and before the proposed inverter nonlinearity compensation are shown in Fig. 4.15 (b) and (c), respectively. Figs. 4.15 (d) and (e) show compensation voltages and actual output voltage with a current step, respectively. Fig. 4.15 (f) shows error voltages between the actual output voltages and reference voltages before compensation. It can be observed that there is a short transient process, and the response of the proposed inverter nonlinearity compensation is fast. By applying the conventional current harmonic-based inverter nonlinearity compensation, three phase currents are shown in Fig. 4.16 (a) with a current step from 2A to 7.5 A. Fig. 4.16 (b) show  $\alpha\beta$ -axis error voltages between the actual output voltages and the reference voltages before compensation in the conventional method. It can be seen that error voltages are relatively high just after the current step, and become lower after several electrical cycles. Current spectra in regions I and II in Fig. 4.16 (a) are compared in Figs. 4.16 (c) and (d). It can be seen that current harmonics in region I are higher than those in region II. As a result, the conventional method needs several electrical cycles to converge, and the proposed inverter nonlinearity compensation method has faster response than the conventional method.



(a) Three phase currents.

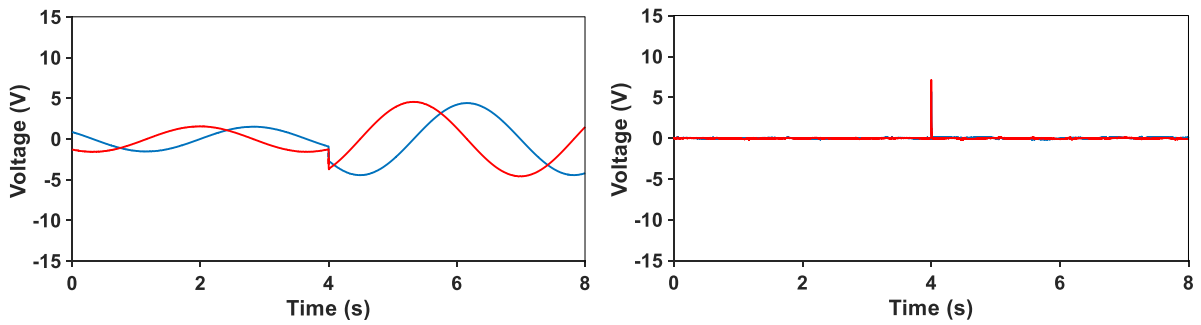


(b) Reference voltages after compensation.



(c) Reference voltages before compensation.

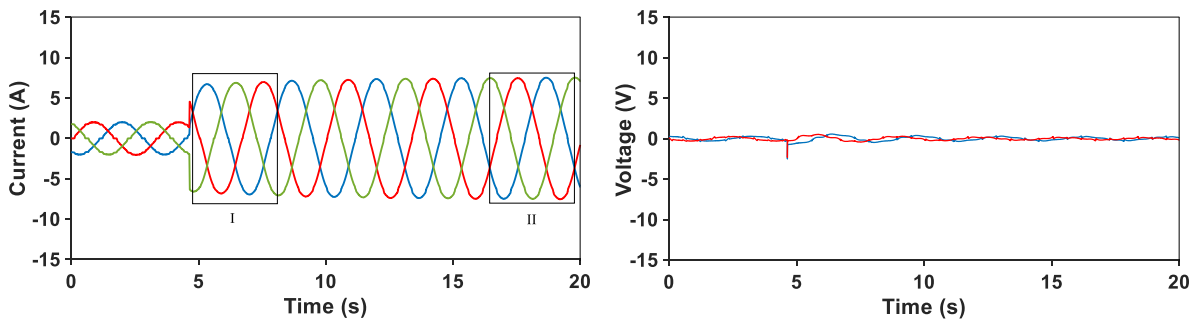
(d) Compensation voltages.



(e) Actual output voltage.

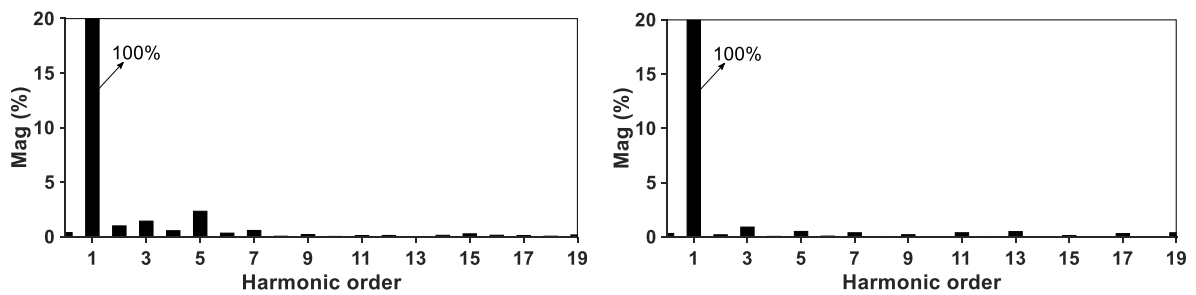
(f) Error voltages.

Fig. 4.15 Proposed inverter nonlinearity compensation with a current step.



(a) Three phase currents.

(b) Error voltages.

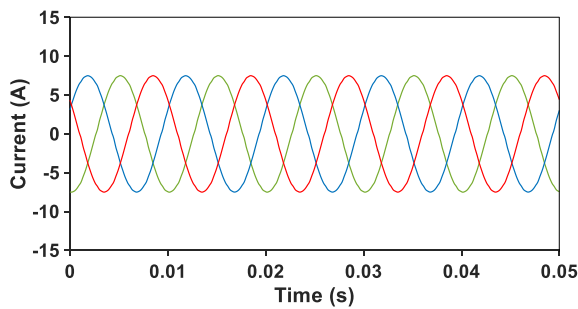


(c) Current spectra in region I.

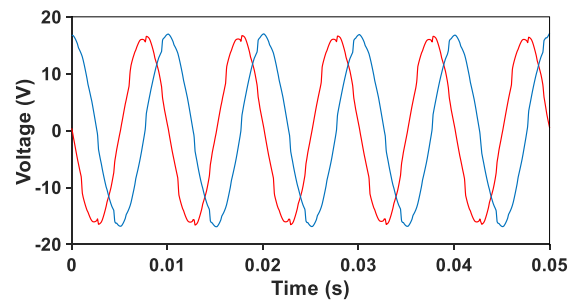
(d) Current spectra in region II.

Fig. 4.16 Conventional inverter nonlinearity compensation method based on current harmonics with a current step.

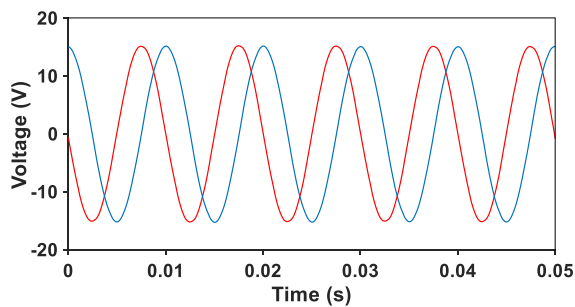
In previous experimental results, the electrical frequency is 0.3 Hz, and the mode switching frequency is 1kHz. To investigate the feasibility of the proposed inverter nonlinearity compensation method, control performances with different speed and mode switching frequency are compared experimentally. In the proposed method, two switching modes are applied alternately at a high mode-switching frequency, and the reference voltages are regarded as the same for the two switching modes. With the increase of electrical frequency, the ratio between the mode-switching frequency and the electrical frequency is reduced, so that the reference voltages in two switching modes cannot be regarded as the same, and then the compensation performance is degraded. Fig. 4.17 shows three phase currents, reference voltages after and before compensation, compensation voltages, actual output voltages and error voltages with 600rpm (100Hz electrical frequency) and mode-switching frequency 1kHz. With the reduction of mode-switching frequency, the compensation performance can be degraded, and even cannot generate stable compensation voltages. Besides, the ratio between the PWM frequency and mode-switching frequency should be an even number, and the largest ratio is 18 when the electrical frequency is 100Hz. Consequently, with 100Hz electrical frequency, the lowest mode-switching frequency is 555.6Hz ( $=10\text{kHz}/18$ ) in the experiment conditions of this chapter, and experimental results are shown in Fig. 4.18. It can be seen that with the reduction of mode-switching frequency, the error voltages will increase. At a result, a large ratio between the mode-switching frequency and the electrical frequency is needed for a better compensation performance.



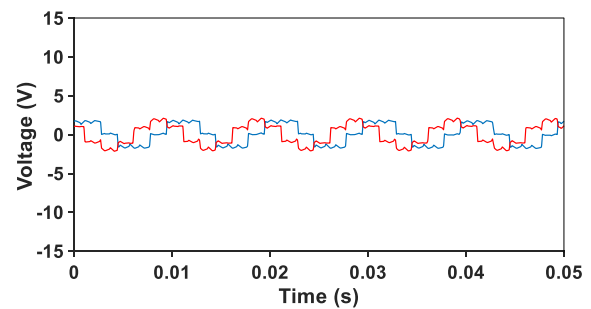
(a) Three phase currents.



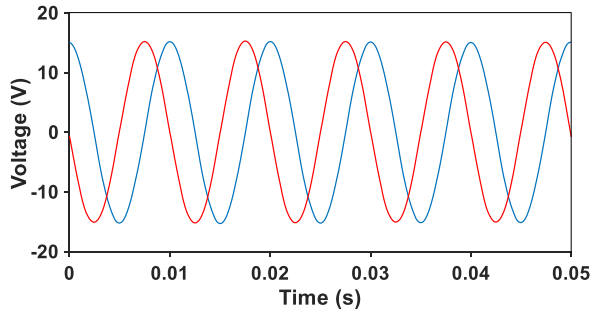
(b) Reference voltages after compensation.



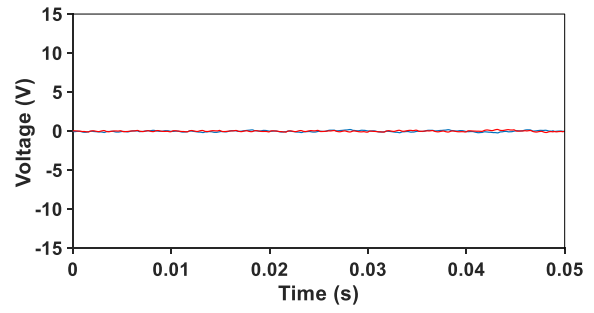
(c) Reference voltages before compensation.



(d) Compensation voltages.

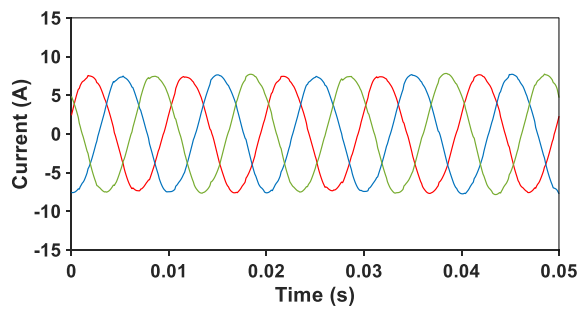


(e) Actual output voltage.

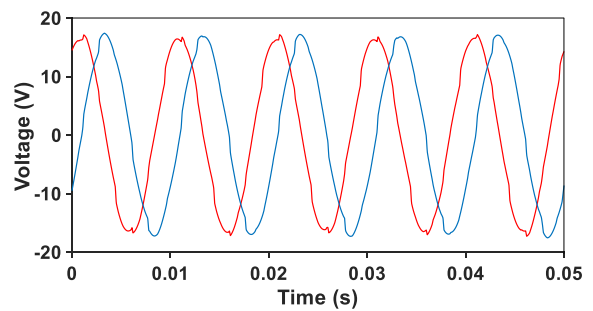


(f) Error voltages.

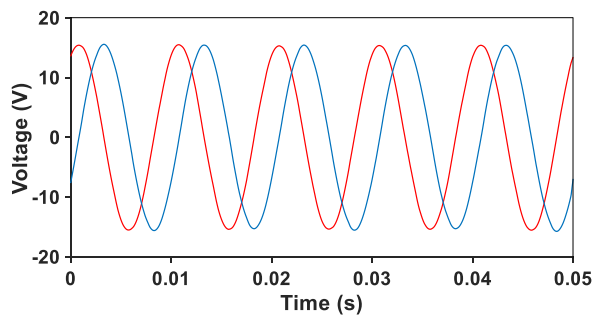
Fig. 4.17 Proposed inverter nonlinearity compensation (100Hz electrical frequency, 1kHz mode-switching frequency).



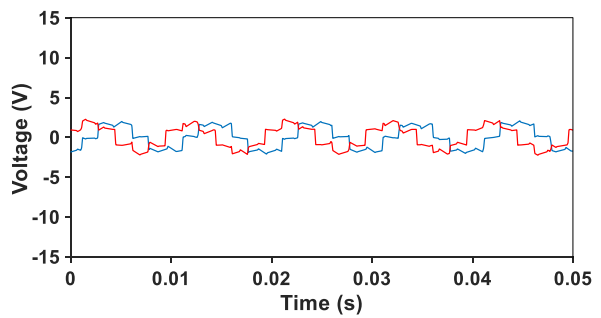
(a) Three phase currents.



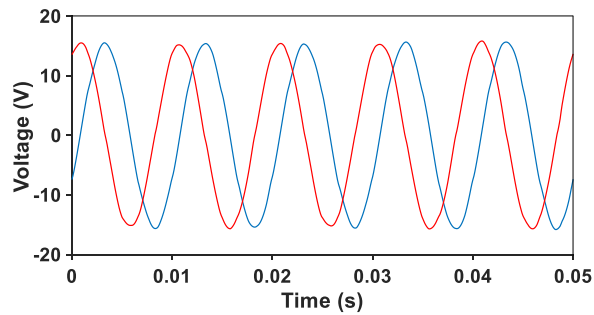
(b) Reference voltages after compensation.



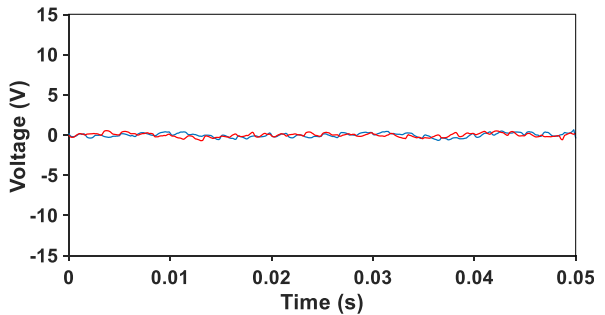
(c) Reference voltages before compensation.



(d) Compensation voltages.



(e) Actual output voltage.



(f) Error voltages.

Fig. 4.18 Proposed inverter nonlinearity compensation (100Hz electrical frequency, 555.6Hz mode-switching frequency).



## 4.5 Summary

In this chapter, a novel inverter nonlinearity compensation strategy is proposed for an OW machine fed by isolated DC-bus dual two-level inverters. The SPWM strategy with balanced and unbalanced switching modes is applied, and the inverter nonlinearity effects on output voltages of dual OW inverters are analysed. The two switching modes are applied alternately at a preset mode-switching frequency, and a close compensation loop is designed to generate compensation voltages utilizing the different voltage distortions in the two switching modes. The proposed inverter nonlinearity compensation method needs no offline measurement for the parameters of the dual OW inverters and the electrical machine, and can also deal with the variation of inverter parameters in different operation conditions. The proposed strategy can also overcome the issues in conventional current harmonic-based methods, such as the need of accurate rotor position and preset compensation voltage curves, as well as mixed voltage distortions caused by inverter nonlinearity and back EMF harmonics. Experiment results have validated the performance of the proposed inverter nonlinearity compensation strategy.

There is more control freedom in an OW machine fed by dual inverters compared with a conventional machine fed by a two-level inverter. For the isolated DC-bus dual inverters, balanced and unbalanced switching modes can be used, and the unbalanced mode is utilized for current harmonic reduction in Chapters 2 and 3, while the mode-switching between balanced and unbalanced modes is used for the inverter nonlinearity compensation in Chapter 4. For the common DC-bus topology, ZSC can flow through the zero sequence circuit, and ZSC can be controlled utilizing the abundant switching combinations of dual inverters. In the next chapter, PWM and control strategies of an OW-PMSM fed by common DC-bus dual two-level inverters are studied for control performance improvements.

# **CHAPTER 5 A NOVEL SVPWM FOR COMMON DC-BUS OPEN WINDING MACHINE WITH LOW CURRENT HARMONIC**

In the previous three chapters, PWM and control strategies of isolated DC-bus dual two-level three phase inverters are investigated. Compared with the isolated DC-bus topology, the common DC-bus topology has the advantage of low cost and the controllability of ZSC, although it has the disadvantage of a smaller modulation region. From this chapter, PWM and control strategies of common DC-bus dual two-level three phase inverters will be studied. In this chapter, a novel SVPWM strategy for OW machines fed by common DC-bus dual two-level three phase inverters is proposed to reduce current harmonics. In the proposed SVPWM strategy for an OW machine, each of six sectors in the space vector plane is further divided into three sub-sectors, in which the optimal effective and zero voltage vector action sequences are found to be different. Consequently, different effective and zero voltage vector action sequences are employed in three sub-sectors. Besides, the symmetrical and asymmetric vector sequences for the conventional and proposed SVPWMs are compared. With the asymmetric vector sequence, low-order current harmonics are induced in the conventional SVPWM, which will be solved by the proposed SVPWM. Compared with the conventional SVPWM strategy with symmetrical and asymmetric sequences for OW machines, the proposed SVPWM strategy produces similar current harmonics in low modulation regions but generates much lower current harmonics in high modulation regions without increasing switching frequency

This chapter is based on the paper published in:

L. Xu and Z. Q. Zhu, "A novel SVPWM strategy for open-winding machine with low current ripples," 2021 IEEE International Electric Machines & Drives Conference (IEMDC), 2021, pp. 1-7.

## 5.1 Introduction

When a PWM strategy is applied to an inverter, there always exist instantaneous errors between the reference voltage vector and the output voltage vectors, resulting in current harmonics [SRI13] [SEK13]. Two analysis methods of current harmonics which are caused by PWM strategy in an OW machine fed by dual two-level inverters, i.e. error voltage vector trajectory method and switching state method, are introduced in [SRI13]. The impact of effective time placement of two inverters on current harmonics is analysed in [SEK13], and it shows that current harmonics can be affected by the action time of the zero vector. In [ZHA17a], an SVPWM strategy with the signal rotation is used in the common DC-bus OW PMSM drive, and ZSC can be controlled by the steerable ZSV. The conventional SVPWM strategy in [ZHA17a] will be compared with the proposed SVPWM strategy. In [SHE19], a phase shift SPWM is proposed for common DC-bus dual inverters, and the asymmetric vector sequence can reduce high-frequency current harmonics. In this chapter, a novel SVPWM strategy for the common DC bus topology is proposed to reduce current harmonics, and each sector is divided into three sub-sectors. The vector action sequences for zero and effective vectors in each sub-sector are analysed in this chapter. It is found that the optimal effective and zero voltage vector action sequences are different and can be employed to significantly reduce current harmonics in high modulation regions. In addition, low-order harmonics introduced by the asymmetric vector sequence are analysed and can be eliminated by the proposed SVPWM. The proposed SVPWM strategies with an asymmetric vector sequence can further reduce current harmonics.

## 5.2 Dual Two-level Inverters fed OW Machine

### 5.2.1 Conventional SVPWM strategy and issues

In an OW induction machine or an OW-PMSM without triplen BEMF harmonics, only the ZSV from PWM is often considered and ZSVs from other sources can be neglected. In this situation, the conventional SVPWM strategy only uses the switching combinations with null ZSV to eliminate ZSV from PWM at any instant and thus suppress ZSC. Fig. 5.1 shows the sector division in the space vector plane of dual two-level inverters with the conventional SVPWM strategy, and the middle hexagon, i.e. HJLNQS, is the theoretical maximum modulation region. For the reference voltage in sector 1 in Fig. 5.1, Fig. 5.2 shows PWM waveforms, switching combinations, and ZSV with the conventional SVPWM strategy in a PWM cycle. Two zero vectors  $77'$  and  $88'$  which are located at the O point, and two effective

vectors 13' and 24' which are located on the middle hexagon, are used to synthesize the reference voltage vector. According to Table 1.3, all four corresponding switching combinations in Fig. 5.2 have null ZSV so that ZSV in a whole PWM cycle can be kept zero at any instant. In sector 1, two effective vectors 1 (100) and 2 (110) are used in the Inverter I while vectors 3' (100) and vectors 4' (110) are used in the Inverter II. Moreover, the duration of vectors 1 is the same as that of vectors 3', while the duration of vectors 2 is the same as that of vectors 4'. Since the 120 degrees between vectors 1 and 3', 2 and 4', the reference voltage vector for the Inverter II can be acquired from a 120-degree rotation of the reference voltage vector for the Inverter I.

For the conventional 7-segment SVPWM strategy in Fig. 5.2, the vector action sequence and durations of these vectors are shown in Table 5.1, where  $\mathbf{V0}$  is the zero voltage vector at the O point,  $\mathbf{V1}$  and  $\mathbf{V2}$  are the two effective voltage vectors on the middle hexagon, and  $T0$ ,  $T1$ , and  $T2$  are the durations of  $\mathbf{V0}$ ,  $\mathbf{V1}$ , and  $\mathbf{V2}$ , respectively. It can be observed that the vector sequence is symmetrical. Besides, the zero vector has three segments, while two effective vectors only have two segments, respectively, which may result in high current harmonics as they are affected by the action sequence of zero and effective vectors and the location of the reference voltage vector. Therefore, the conventional SVPWM strategy needs to be improved to reduce current harmonics by optimizing the vector action sequence and the implementation region.

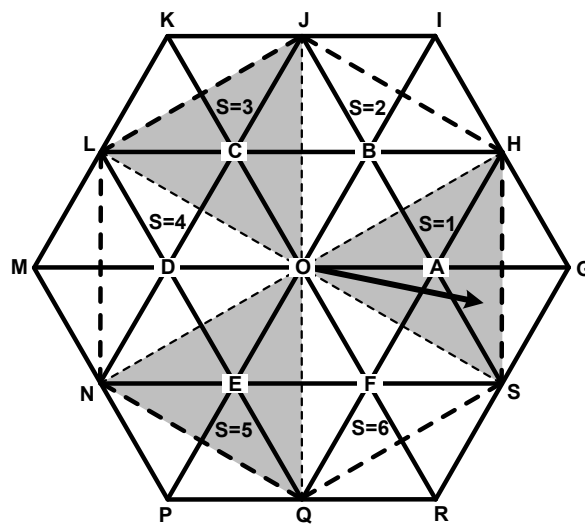


Fig. 5.1 Sectors of the conventional SVPWM strategy.

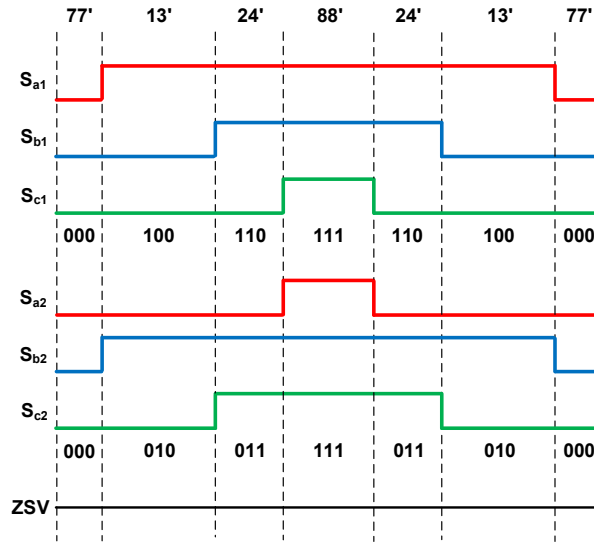


Fig. 5.2 PWM waveforms of the conventional SVPWM strategy in sector 1.

Table 5.1 Vector Sequence and Durations of the Conventional SVPWM Strategy

Segments	1	2	3	4	5	6	7
Vectors	<b>V0</b>	<b>V1</b>	<b>V2</b>	<b>V0</b>	<b>V2</b>	<b>V1</b>	<b>V0</b>
Duration	T0/4	T1/2	T2/2	T0/2	T2/2	T1/2	T0/4

In the conventional SVPWM strategy of common DC-bus dual two-level inverters, the SVPWM strategy of a two-level inverter is applied to Inverters I and II with different reference voltage vectors, which have the same magnitude and 120 electrical degree angle between each other as shown in Fig. 5.3. The two reference voltage vectors for two inverters are from the decomposition of the reference voltage vector for dual two-level inverters as shown in Fig. 5.4. The relationship between the reference voltage vector for dual two-level inverters and the two reference voltage vectors for two inverters can be expressed as

$$\begin{aligned} \mathbf{V}_{ref1} &= \frac{1}{\sqrt{3}} e^{j\frac{\pi}{6}} \mathbf{V}_{ref} \\ \mathbf{V}_{ref2} &= \frac{1}{\sqrt{3}} e^{j\frac{5\pi}{6}} \mathbf{V}_{ref} \end{aligned} \quad (5.1)$$

where  $\mathbf{V}_{ref1}$  and  $\mathbf{V}_{ref2}$  are the reference voltages for Inverters I and II, respectively, and  $\mathbf{V}_{ref}$  is the reference voltage for dual two-level inverters.

In addition to the PWM, ZSV can also be generated by some other sources, such as inverter nonlinearity, the triplen harmonics of BEMF, and cross coupling voltages in the zero sequence

in an OW-PMSM control system. Among these sources, only PWM can generate a controllable ZSV, which can counteract ZSVs from the other three sources to achieve the ZSC suppression. Fig. 5.5 shows the control diagram of the conventional SVPWM, and a close loop is used for ZSC control.

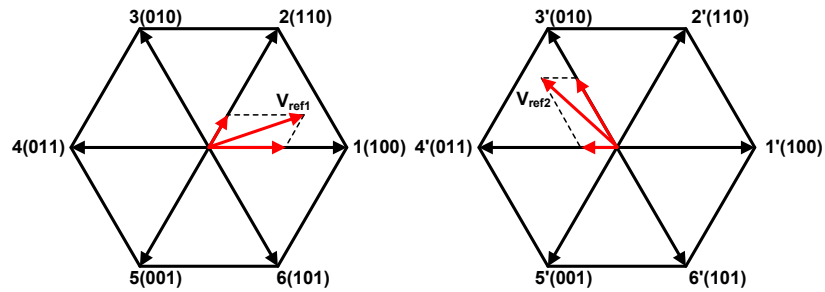


Fig. 5.3 Reference voltage vector of each inverter.

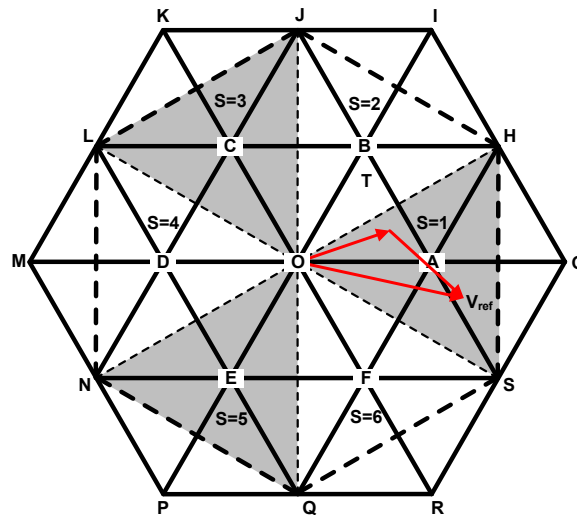


Fig. 5.4 Reference voltage vector of dual inverters.

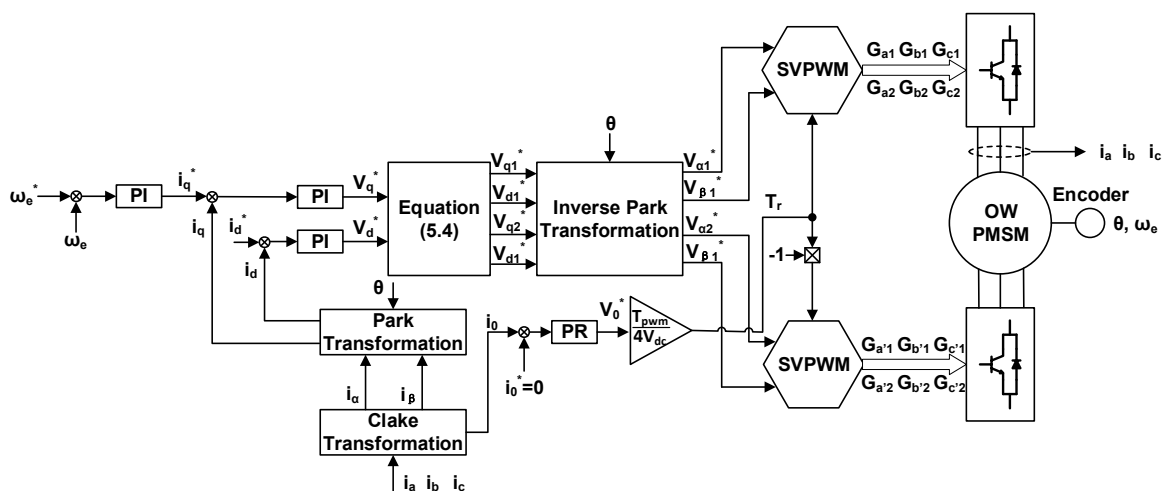


Fig. 5.5 Control block diagram of the conventional SVPWM strategy.

Since the frequency of the ZSC varies with the fundamental frequency according to operation conditions, a PR controller is used to avoid the static error in a proportional integral controller [ZHA17a] [KPU15].

The open-loop transfer function of the PR controller can be expressed as

$$C(s) = K_{P,PR} + \frac{2K_{I,PR}s}{s^2 + \omega_0^2} \quad (5.2)$$

where  $K_{P,PR}$  and  $K_{I,PR}$  are the proportional and integral coefficients, respectively. Apart from PWM, the main component of ZSV sources is the third BEMF harmonic in an OW-PMSM drive, so that  $\omega_0$  is set as the triple of electrical frequency of OW-PMSM, i.e.  $\omega_0=3\omega_e$ .

For the ZSC closed-loop control,  $K_{P,PR}$  and  $K_{I,PR}$  can be designed according to [KPU15] as

$$\begin{aligned} K_{P,PR} &= L_0 \omega_c \\ K_{I,PR} &= R \omega_c \end{aligned} \quad (5.3)$$

where  $L_0$  is the zero sequence inductance,  $R$  is the phase resistance, and  $\omega_c$  is the cut-off frequency of the PR controller, which is set as 1000Hz in this chapter.

The proportional resonant controller generates the redistribution time  $T_r$  of zero vectors for the conventional SVPWM strategy, and the input of the controller is the difference between the ZSC reference and the feedback. Three phase duty cycles will be increased by  $2T_r/T_{pwm}$  in Inverter I and decreased by  $2T_r/T_{pwm}$  in Inverter II regardless of the sign of  $T_r$  ( $T_{pwm}$  is the PWM cycle). With the change of three phase duty cycles, durations of zero vectors are redistributed in two inverters. Before the redistribution of zero vectors, only the switching combinations with null ZSV are used as shown in Fig. 5.2. After the redistribution, PWM waveforms are shown in Fig. 5.6, and non-null ZSV switching combinations are introduced to generate ZSV, which can counteract the ZSVs caused by other sources, such as the triplen BEMF harmonics, inverter nonlinearity, and zero sequence component of coupling voltages.

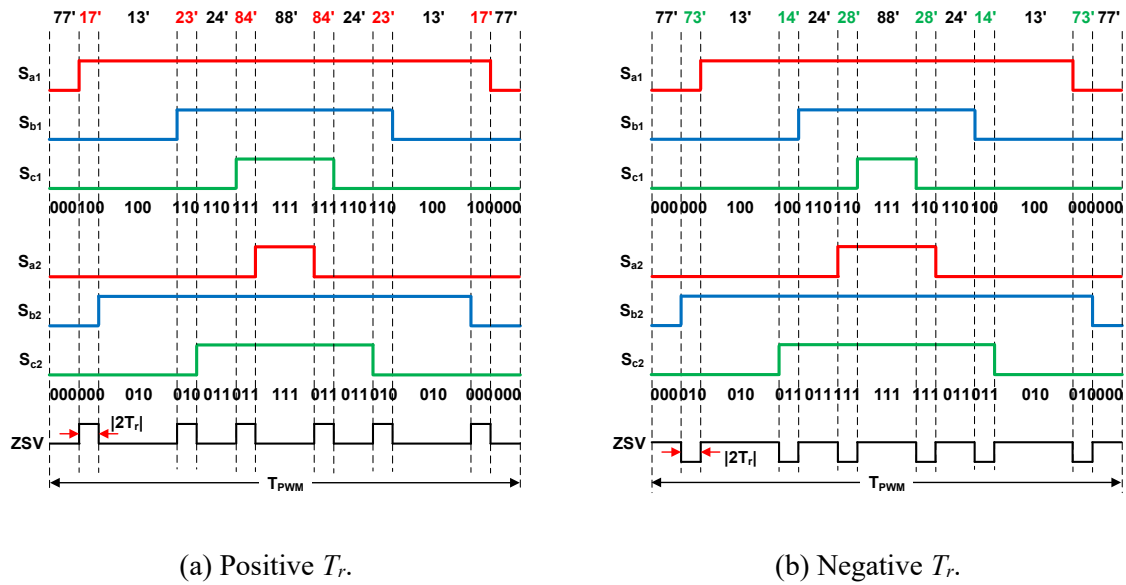


Fig. 5.6 PWM waveforms of the conventional SVPWM with ZSC control.

Due to the redistribution of zero vectors, three phase duty cycles will be increased by  $2T_r/T_{pwm}$  in Inverter I and decreased by  $2T_r/T_{pwm}$  in Inverter II, so that ZSV of Inverter I will increase by  $2T_rV_{dc}/T_{pwm}$ , while ZSV reduces by  $2T_rV_{dc}/T_{pwm}$  in Inverter II. As a result, ZSV generated by PWM is  $4T_rV_{dc}/T_{pwm}$  in the dual inverters, which should equal the reference ZSV. As a result, the relationship between  $T_r$  and the reference ZSV  $V_0^*$  can be expressed as

$$T_r = \frac{T_{PWM}V_0^*}{4V_{dc}}. \quad (5.4)$$

It can be seen that ZSV from PWM is determined by  $T_r$ , and thus can be controlled by the zero sequence close loop. With the controllable ZSV from PWM, the conventional SVPWM strategy can suppress ZSC.

### 5.2.2 Current harmonic analysis method for PWM strategy

It is known that there always exists an error between the reference voltage vector and the instantaneous output voltage vector, and this error will generate ripples in three phase currents. Some current harmonic analysis methods had been proposed for OW machines [SRI13] [SEK13], and they can be simplified in this chapter. The reference voltage vector and three error voltage vectors are shown in Fig. 5.7 when the reference voltage vector is located in the triangle OSH of the space vector plane. Those error voltage vectors can be expressed as



$$\begin{aligned}
\mathbf{V}_{VO} &= -\mathbf{V}_{OV} \\
\mathbf{V}_{VS} &= \mathbf{V}_{OS} - \mathbf{V}_{OV} \\
\mathbf{V}_{VH} &= \mathbf{V}_{OH} - \mathbf{V}_{OV}
\end{aligned} \tag{5.5}$$

where  $\mathbf{V}_{OV}$  is the reference voltage vector,  $\mathbf{V}_{OS}$  and  $\mathbf{V}_{OH}$  are the effective voltage vectors of dual inverters.

Taking the conventional SVPWM in Fig. 5.2 as an example, when the reference voltage vector is located in the triangle OSH. Considering the stator circuit as a simplified inductor circuit with inductance  $L_s$ , the relationship between the error voltage and ripple current in each segment can be expressed as

$$i_{rip} = \int \frac{V_{error}}{L_s} dt. \tag{5.6}$$

For the trajectories of current ripples in the  $\alpha\beta$  plane in Fig. 5.8 or  $\alpha$  and  $\beta$ -axes in Fig. 5.9, the terminal values of each segment can be calculated by

$$\begin{aligned}
i_{1x} &= \frac{V_{VOx}T_0}{4L_s} & i_{2x} &= i_{1x} + \frac{V_{VSx}T_{OS}}{2L_s} & i_{3x} &= i_{2x} + \frac{V_{VHx}T_{OH}}{2L_s} \\
i_{4x} &= i_{3x} + \frac{V_{VOx}T_0}{2L_s} & i_{5x} &= i_{4x} + \frac{V_{VHx}T_{OH}}{2L_s} \\
i_{6x} &= i_{5x} + \frac{V_{VAx}T_{OS}}{2L_s} & i_{7x} &= i_{6x} + \frac{V_{VOx}T_0}{4L_s}
\end{aligned} \tag{5.7}$$

where 1~7 represents 7 segments in Table 5.1, “x” represents  $\alpha$  and  $\beta$ ,  $T_0$ ,  $T_{OS}$ , and  $T_{OH}$  are the durations of zero vectors,  $\mathbf{V}_{OS}$ , and  $\mathbf{V}_{OH}$ .

The current ripple trajectory in the  $\alpha\beta$  plane can be used to evaluate harmonic characteristics of the proposed and conventional SVPWM strategies with symmetrical and asymmetric vector sequences in this chapter. The farther the trajectory is from the zero point, the larger the current ripples.

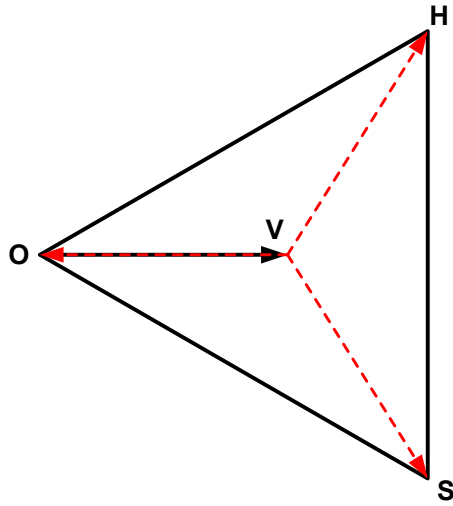


Fig. 5.7. Reference voltage vector and error vectors.

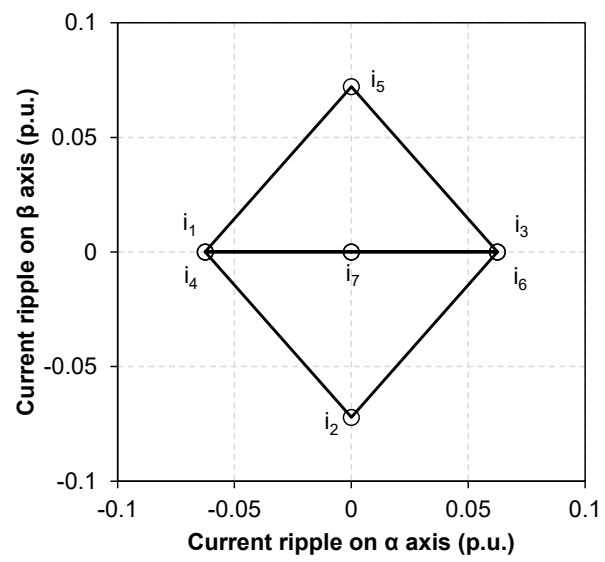
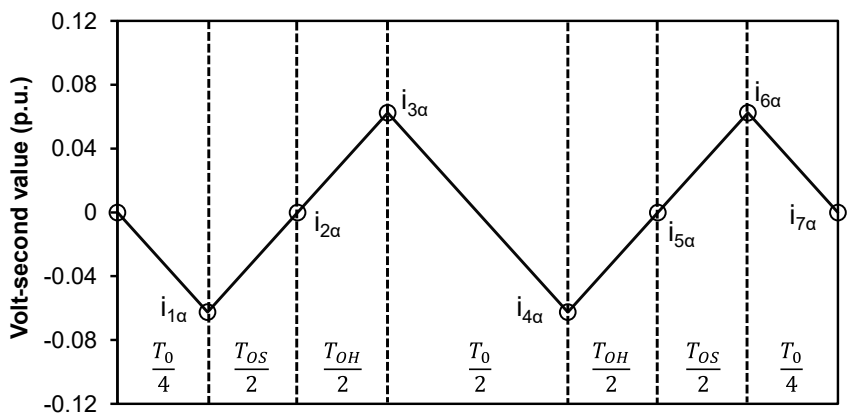
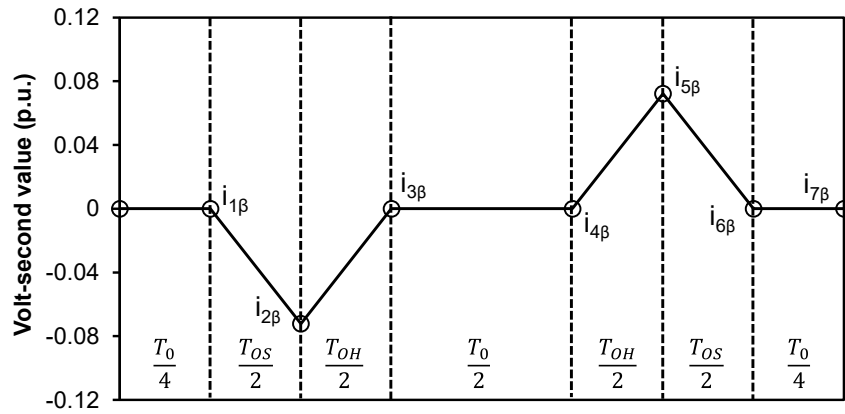


Fig. 5.8 Current ripple trajectory in  $\alpha\beta$  plane.



(a)  $\alpha$ -axis.



(b)  $\beta$ -axis.

Fig. 5.9 Current ripple trajectories in  $\alpha$  and  $\beta$ -axis.

### 5.3 Proposed SVPWM Strategy

#### 5.3.1 Symmetrical vector sequence

In the proposed SVPWM strategy, the whole modulation region is divided into six sectors and each sector is further divided into three sub-sectors in Fig. 5.10. Further, in addition to the voltage vector action sequence in the conventional SVPWM strategy, two new voltage vector action sequences are introduced, in which two effective vectors have three segments, respectively, while the zero vector only has two segments. The vector action sequences and durations of voltage vectors in different sub-sectors are shown in Table 5.2, and the three vector sequences are all symmetrical.

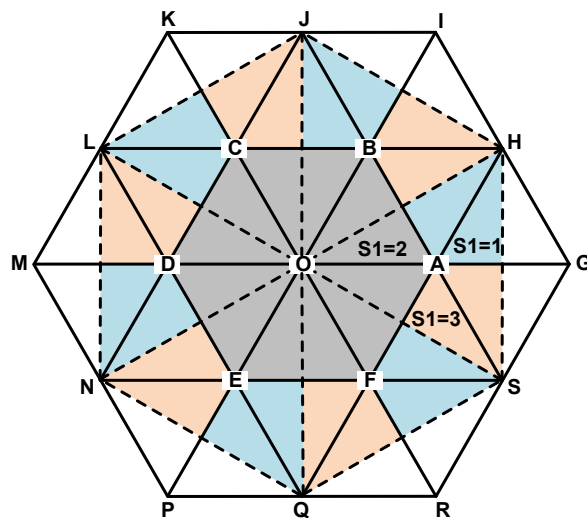


Fig. 5.10 Sectors and sub-sectors of the proposed PWM strategy.

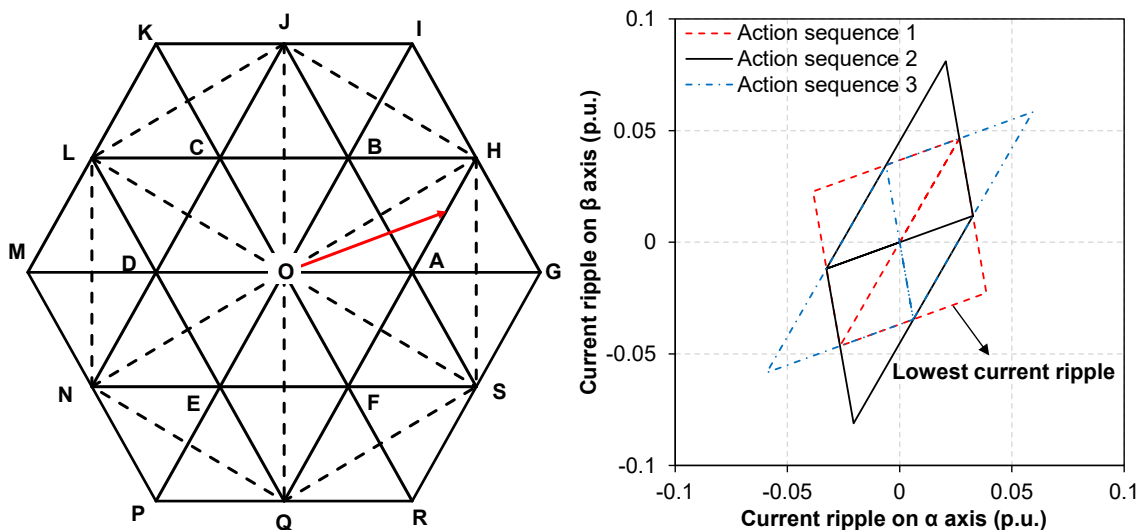
Table 5.2 Symmetrical Vector Sequence and Durations of the Proposed SVPWM Strategy

Vector action sequence 1 (Sub-sector 1)	Vector	<b>V2</b>	<b>V1</b>	<b>V0</b>	<b>V2</b>	<b>V0</b>	<b>V1</b>	<b>V2</b>
	Duration	T2/4	T1/2	T0/2	T2/2	T0/2	T1/2	T2/4
Vector action sequence 2 (Sub-sector 2)	Vector	<b>V0</b>	<b>V1</b>	<b>V2</b>	<b>V0</b>	<b>V2</b>	<b>V1</b>	<b>V0</b>
	Duration	T0/4	T1/2	T2/2	T0/2	T2/2	T1/2	T0/4
Vector action sequence 3 (Sub-sector 3)	Vector	<b>V1</b>	<b>V2</b>	<b>V0</b>	<b>V1</b>	<b>V0</b>	<b>V2</b>	<b>V1</b>
	Duration	T1/4	T2/2	T0/2	T1/2	T0/2	T2/2	T1/4

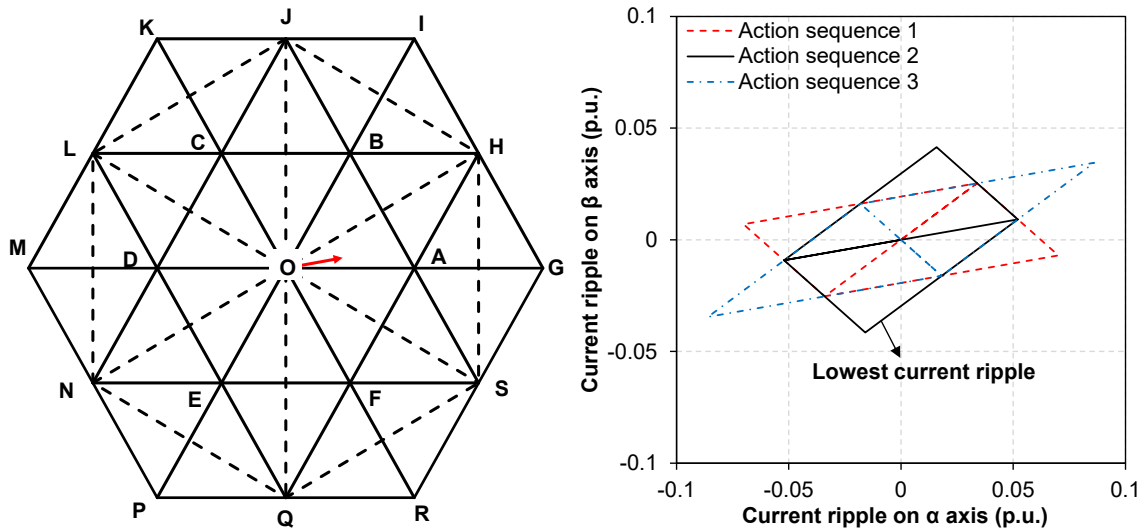
The current harmonic analysis method in 5.2.2 is used to analyse current ripples for three vector action sequences with different modulation indices ( $MI = \text{reference voltage}/V_{dc}$ ) and electrical angles ( $\theta$ ), and the locations of reference voltage vectors and current ripple trajectories in the  $\alpha\beta$  plane are shown in Fig. 5.11. Fig. 5.11 (a) shows that the vector action sequence 1 has the lowest current ripples when the reference voltage vector is located in sub-sector 1. When the reference voltage vector is in sub-sectors 2 and 3, the optimal vector action sequences are 2 and 3, respectively, as shown in Fig. 5.11 (b) and (c). As a result, in three sub-sectors, the optimal effective and zero voltage vector action sequences are found to be different. The voltage vector, which is the nearest one to the reference voltage vector, has a larger effect on current harmonics compared with the other two vectors. If this vector has three segments in a 7-segment vector action sequence, current harmonics will be the lowest. As a result, a sector can be equally divided into three sub-sectors, and each of them is close to a vertex of the sector. Further, if the voltage vector close to a sub-sector has three segments in a vector action sequence, then this sequence is optimal for this sub-sector. Consequently, different effective and zero voltage vector action sequences can be employed in three sub-sectors to reduce current ripples. In the proposed SVPWM strategy, two new voltage vector action sequences are used in sub-sectors 1 and 3, respectively, while the conventional voltage vector action sequence is applied in sub-sector 2.

Taking sector 1 as an example,  $\overrightarrow{OS}$  is vector **V1** and  $\overrightarrow{OH}$  is vector **V2** as shown in Fig. 1.32. It can be observed that there are ten switching combinations at the O point that can be used for the zero vector and two switching combinations on the middle hexagon for an effective vector

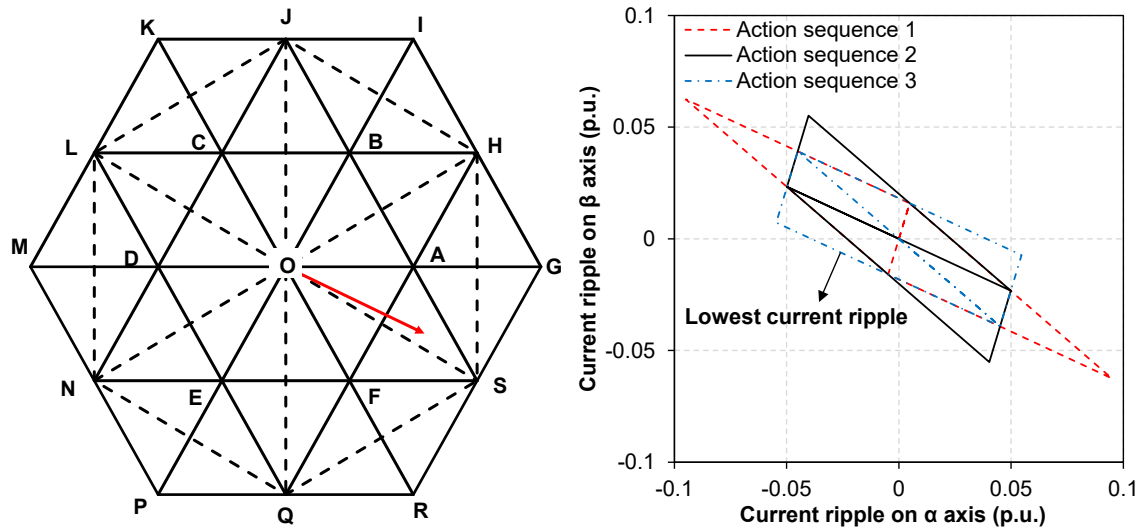
to design a PWM strategy. According to the vector action sequence in each sub-sector in sector 1 of the proposed SVPWM strategy in Table 5.2, it can be observed that the zero vector  $\mathbf{V}_0$  has three segments in sub-sector 2, which is the same as that in the conventional SVPWM strategy. On the other hand, vector  $\mathbf{V}_2$  ( $15^\circ, 24^\circ$ ) has three segments in the sub-sector 1, so that vector  $\mathbf{V}_2$  replaces the position of the zero vector  $\mathbf{V}_0$  in the conventional SVPWM strategy (vector action sequence 2). Besides, vector  $\mathbf{V}_1$  ( $13^\circ, 64^\circ$ ) has three segments in sub-sector 3. To maintain the PWM switching frequency the same as the conventional SVPWM strategy, the action times of a switching device should be less than twice in a PWM cycle, which means it only has one switching on and one switching off. As a result, switching combinations of zero vectors, such as 11', 22' ...66', which are not used in the conventional SVPWM strategy are applied in the sub-sectors 1 and 3 to comply with the principle of twice switching times in one PWM cycle for a switching device. Switching combinations 22' and 44' are used in sub-sector1 while switching combinations 44' and 66' are used in sub-sector3. PWM waveforms and switching combinations of the proposed SVPWM strategy with symmetrical vector sequence in each sub-sectors of sector 1 are shown in Fig. 5.12 (a), (b) and (c), respectively. It can be observed that ZSV can maintain zero in all three sub-sectors in the proposed SVPWM strategy. Due to the different initial switching states in different sub-sectors, the proposed SVPWM will cause extra switching commutations during the sector change. However, when the ratio between the PWM carrier frequency and the electrical frequency is high, the extra switching commutations can be neglected compared with high-frequency switching actions, and the proposed SVPWM can be compared with the conventional SVPWM with similar switching loss.



(a)  $MI=0.9, \theta = 20^\circ$ .

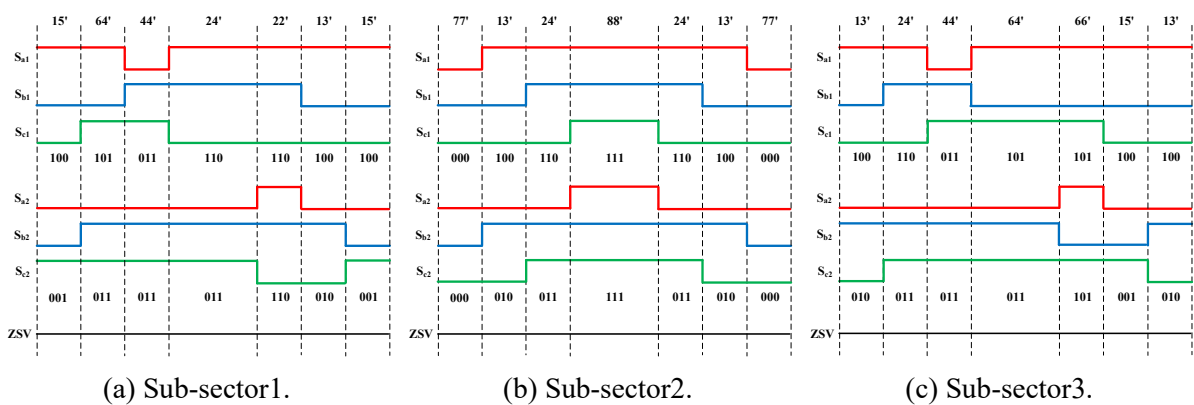


(b)  $MI=0.3, \theta = 10^\circ$ .



(c)  $MI=0.8, \theta = -25^\circ$ .

Fig. 5.11 Current ripple trajectories of proposed SVPWM strategy with symmetrical vector sequence.



(a) Sub-sector 1.

(b) Sub-sector 2.

(c) Sub-sector 3.

Fig. 5.12 PWM waveforms of proposed SVPWM strategy with symmetrical vector sequence in sector 1.

### 5.3.2 Asymmetric vector sequence

In the conventional SVPWM strategy, the vector action sequence is centrosymmetric as shown in Table 5.1. The asymmetric vector sequence of the conventional SVPWM strategy is shown in Table 5.3, in which vectors in the fifth and sixth segments are exchanged, compared with the symmetrical vector sequence. Fig. 5.13 shows the location of the reference voltage vector in the space vector plane and the current ripple trajectories of the conventional SVPWM strategies with symmetrical and asymmetric vector sequences. It can be observed that the trajectory of the symmetrical vector sequence SVPWM strategy is a quadrangle, but it becomes a triangle when the asymmetric vector sequence SVPWM strategy is applied. Consequently, the trajectory of the asymmetric vector sequence SVPWM strategy is halved compared with the symmetrical vector sequence SVPWM strategy. As a result, the current harmonic characteristics of the conventional SVPWM strategy can be improved by applying the asymmetric vector sequence.

Table 5.3 Asymmetric Vector Sequence and Durations of the Conventional SVPWM Strategy

Segments	1	2	3	4	5	6	7
Vectors	<b>V0</b>	<b>V1</b>	<b>V2</b>	<b>V0</b>	<b>V1</b>	<b>V2</b>	<b>V0</b>
Duration	T0/4	T1/2	T2/2	T0/2	T1/2	T2/2	T0/4

In the proposed SVPWM strategy, three vector action sequences are applied in the different regions of a sector to reduce current harmonics. However, all three vector action sequences are symmetrical. The asymmetric vector sequence can also be applied to the proposed SVPWM strategies. Table 5.4 shows the three asymmetric sequences. Figs. 5.14-16 (a) show the locations of reference voltage vectors and current ripple trajectories in the  $\alpha\beta$  plane when the proposed asymmetric vector sequence SVPWM strategy is applied. It can be observed that the asymmetric sequence can further reduce current ripples.

Figs. 5.14-16 (b), (c) (d) show current ripple trajectories in the  $\alpha$ - and  $\beta$ -axes of three action sequences with different locations of reference voltage vectors. For the conventional SVPWM with the asymmetric sequence, i.e. asymmetric sequence 2 in Table 5.4, current ripple trajectories in B and C axes have a large DC bias in large modulation regions in Fig. 5.14 (c) and Fig. 5.16 (c), respectively, which can cause an error between the sample current and the

actual average current in a sample cycle, and thus generate low-order harmonics in phase currents. For the proposed SVPWM with the asymmetric sequence, different action sequences are used in each sub-sector, and the DC bias of current ripple can be reduced as shown in Fig. 5.14 (b), Fig. 5.15 (c), and Fig. 5.16 (d). As a result, the low-order harmonic issues in the conventional SVPWM with the asymmetric sequence can be solved in the proposed SVPWM.

PWM waveforms and switching combinations of the proposed PWM strategy with an asymmetric vector sequence are shown in Fig. 5.17. It can be observed that ZSV can still maintain zero in all three sub-sectors.

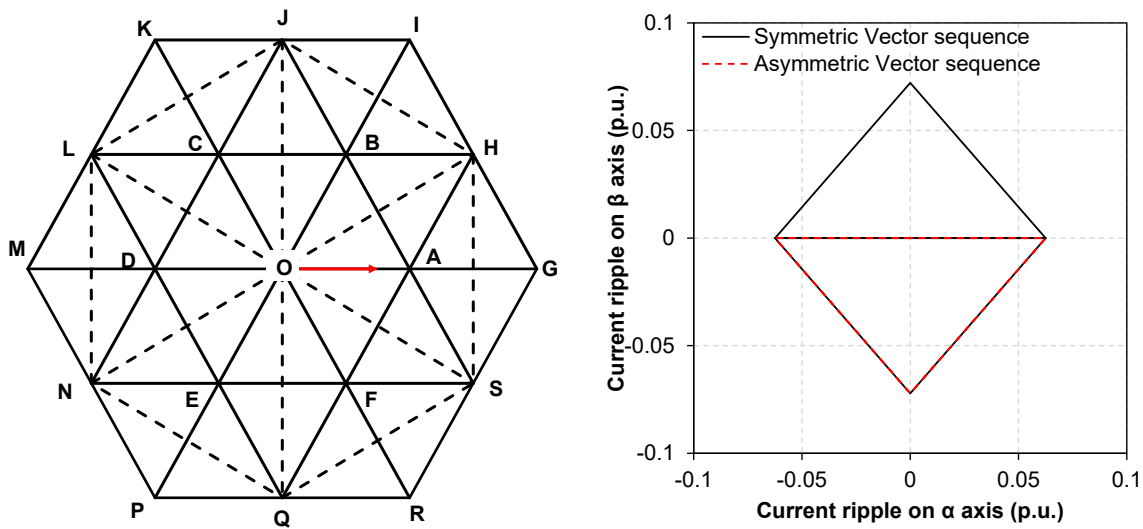
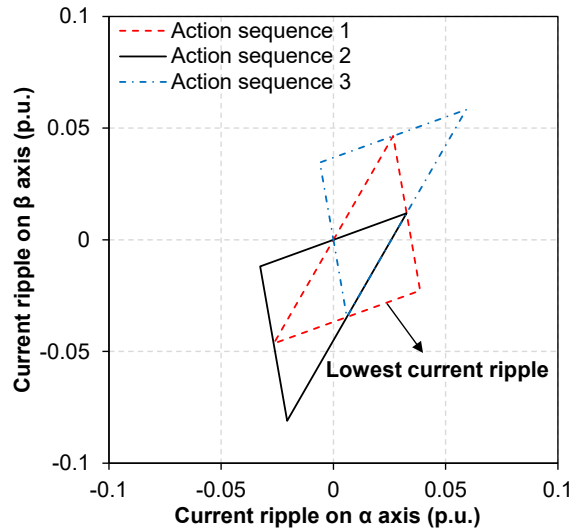
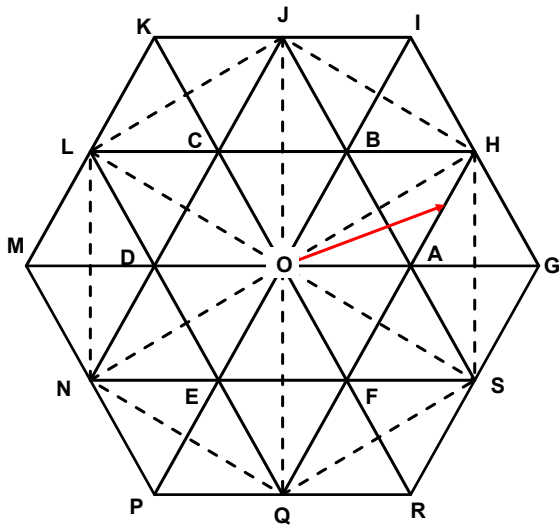


Fig. 5.13 Reference voltage vector and current ripple trajectories of conventional SVPWM strategies with symmetrical and asymmetric vector sequences.

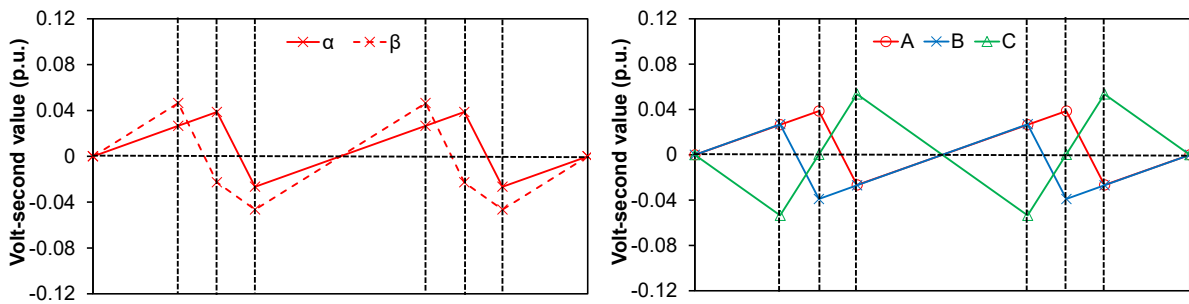
Table 5.4 Asymmetric Vector Sequence and Duration of Proposed SVPWM Strategy

Vector action sequence 1 (Sub-sector 1)	Vector	<b>V2</b>	<b>V1</b>	<b>V0</b>	<b>V2</b>	<b>V1</b>	<b>V0</b>	<b>V2</b>
	Duration	T2/4	T1/2	T0/2	T2/2	T1/2	T0/2	T2/4
Vector action sequence 2 (Sub-sector 2)	Vector	<b>V0</b>	<b>V1</b>	<b>V2</b>	<b>V0</b>	<b>V1</b>	<b>V2</b>	<b>V0</b>
	Duration	T0/4	T1/2	T2/2	T0/2	T1/2	T2/2	T0/4
Vector action sequence 3 (Sub-sector 3)	Vector	<b>V1</b>	<b>V2</b>	<b>V0</b>	<b>V1</b>	<b>V2</b>	<b>V0</b>	<b>V1</b>
	Duration	T1/4	T2/2	T0/2	T1/2	T2/2	T0/2	T1/4

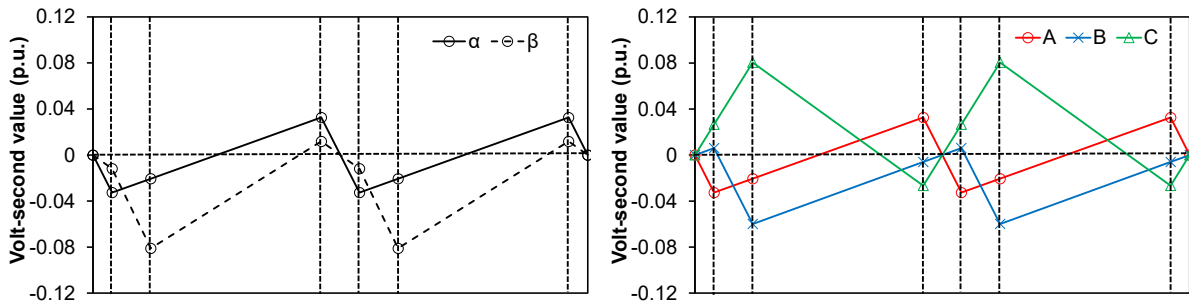




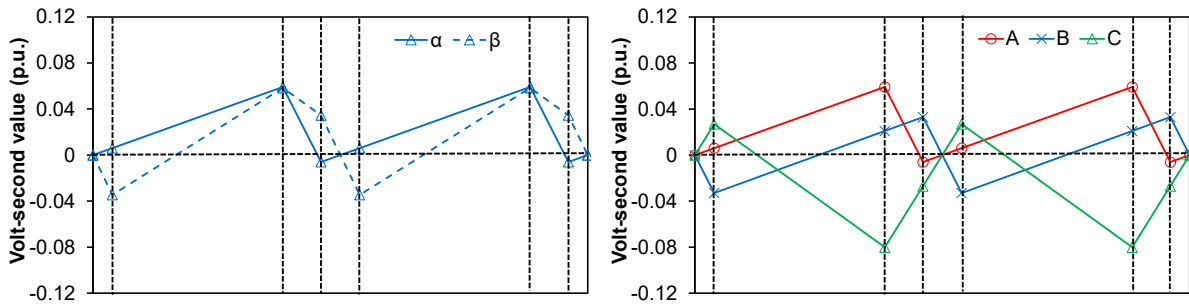
(a) Reference voltage vector and current ripple trajectories of three action sequences in the  $\alpha\beta$  plane.



(b) Current ripple trajectories in  $\alpha\beta$ -axes and ABC-axes (action sequence 1).

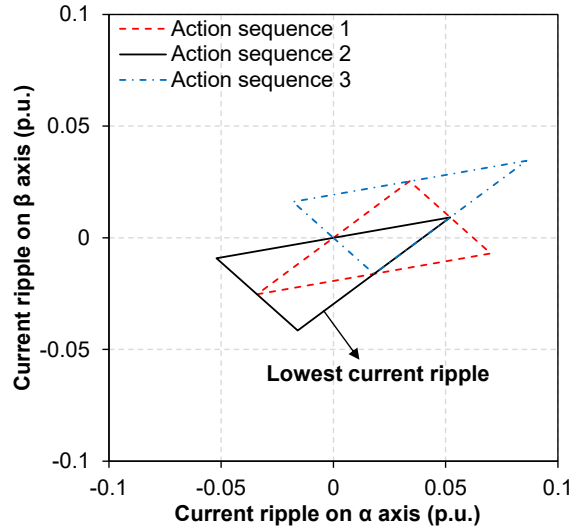
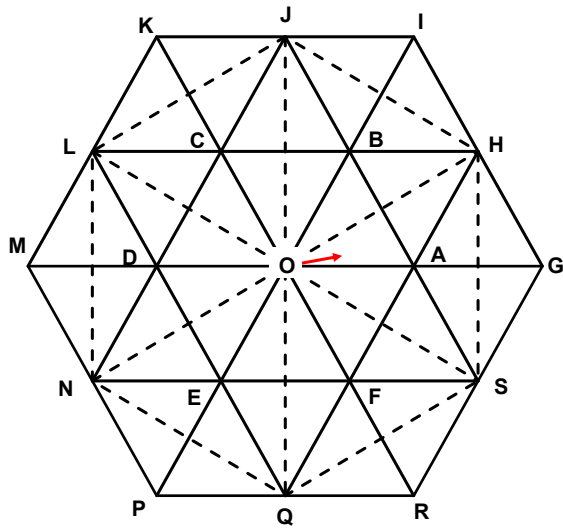


(c) Current ripple trajectories in  $\alpha\beta$ -axes and ABC-axes (action sequence 2).

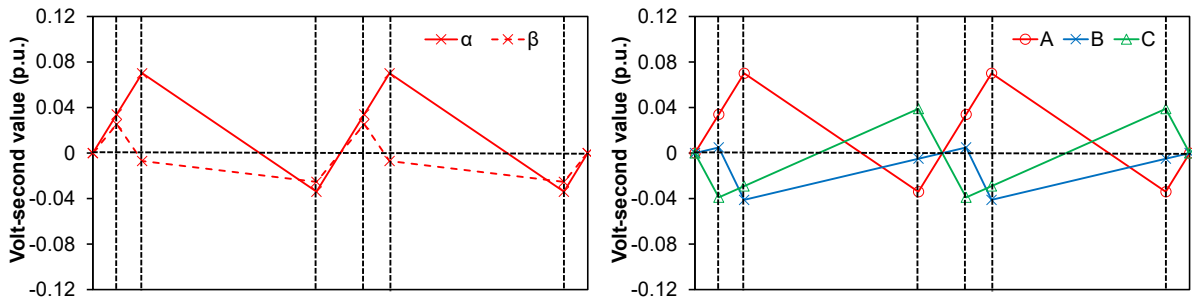


(d) Current ripple trajectories in  $\alpha\beta$ -axes and ABC-axes (action sequence 3).

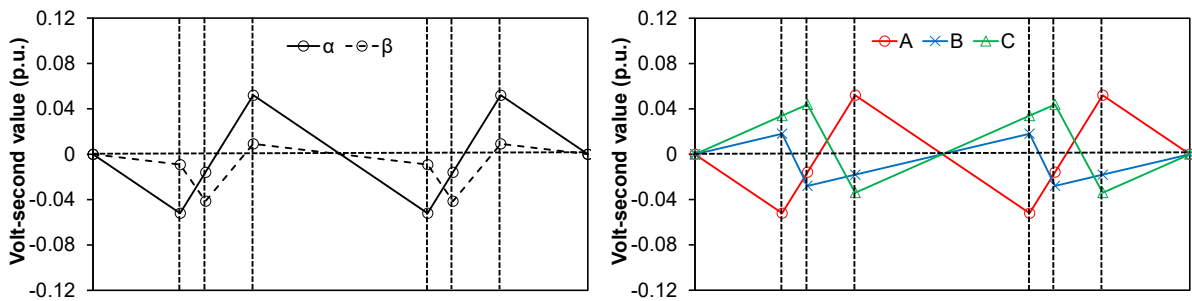
Fig. 5.14 Reference voltage vector and Current ripple trajectories ( $MI=0.9, \theta = 20^\circ$ ).



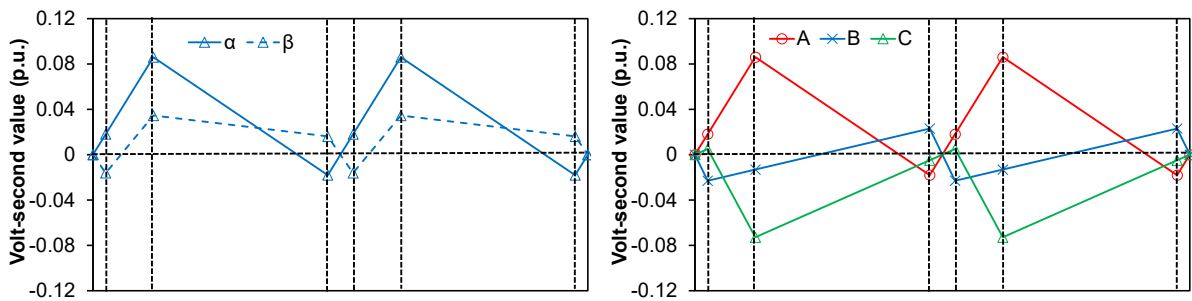
(a) Reference voltage vector and Current ripple trajectories of three action sequences in the  $\alpha\beta$  plane.



(b) Current ripple trajectories in  $\alpha\beta$ -axes (action sequence 1).

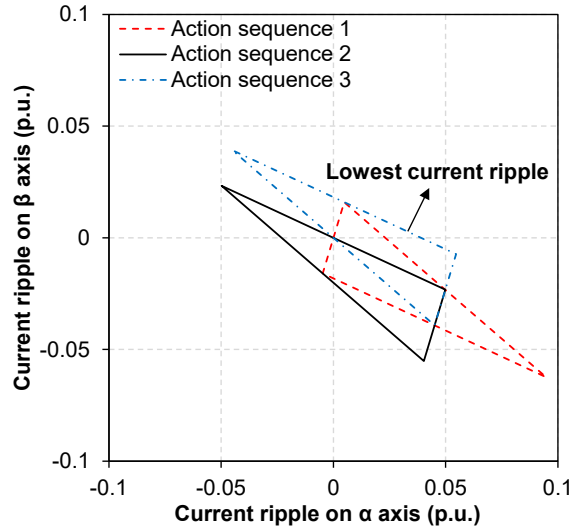
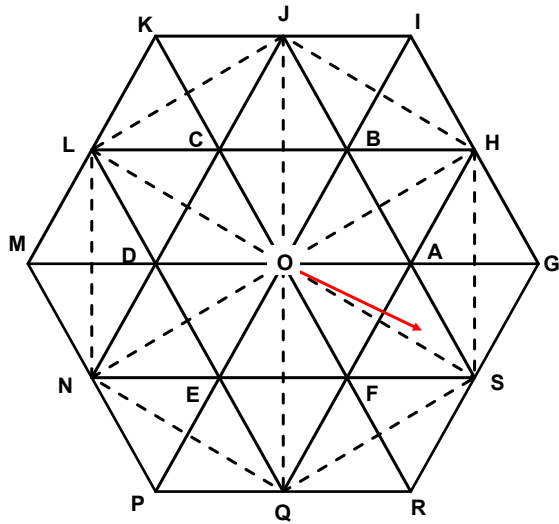


(c) Current ripple trajectories in  $\alpha\beta$ -axes (action sequence 2).

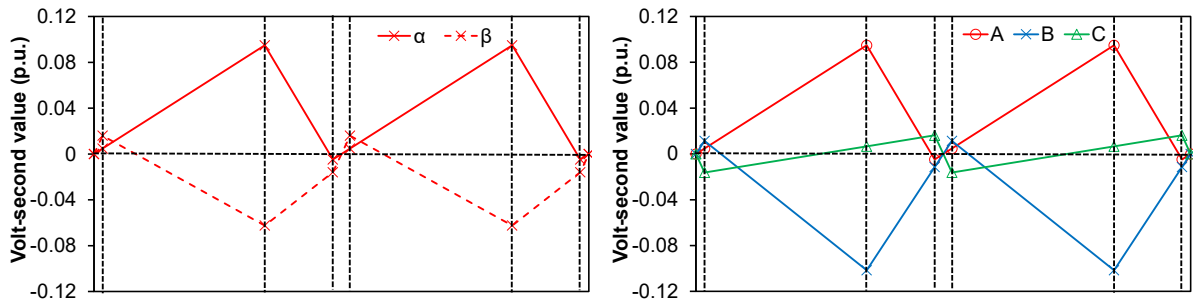


(d) Current ripple trajectories in  $\alpha\beta$ -axes (action sequence 3).

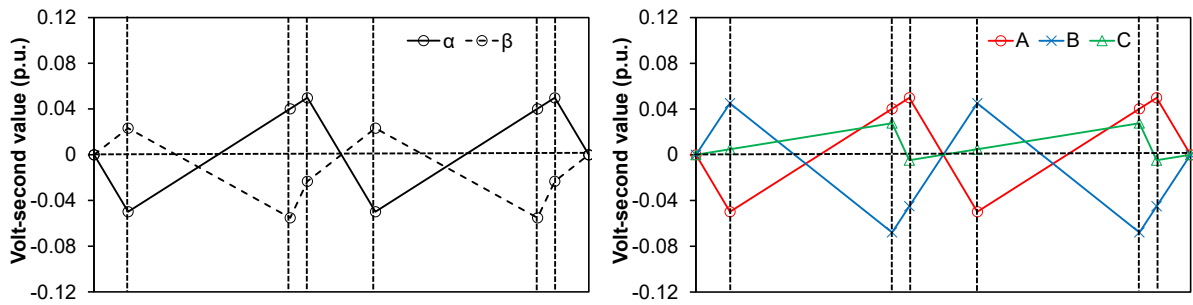
Fig. 5.15 Reference voltage vector and Current ripple trajectories ( $MI=0.3, \theta = 10^\circ$ ).



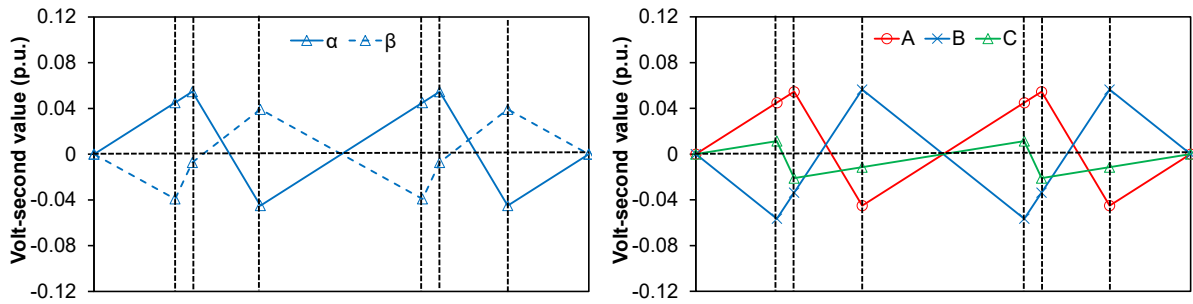
(a) Reference voltage vector and Current ripple trajectories of three action sequences in the  $\alpha\beta$  plane.



(b) Current ripple trajectories in  $\alpha\beta$ -axes (action sequence 1).



(c) Current ripple trajectories in  $\alpha\beta$ -axes (action sequence 2).



(d) Current ripple trajectories in  $\alpha\beta$ -axes (action sequence 3).

Fig. 5.16 Reference voltage vector and Current ripple trajectories (MI=0.8,  $\theta = -25^\circ$ ).

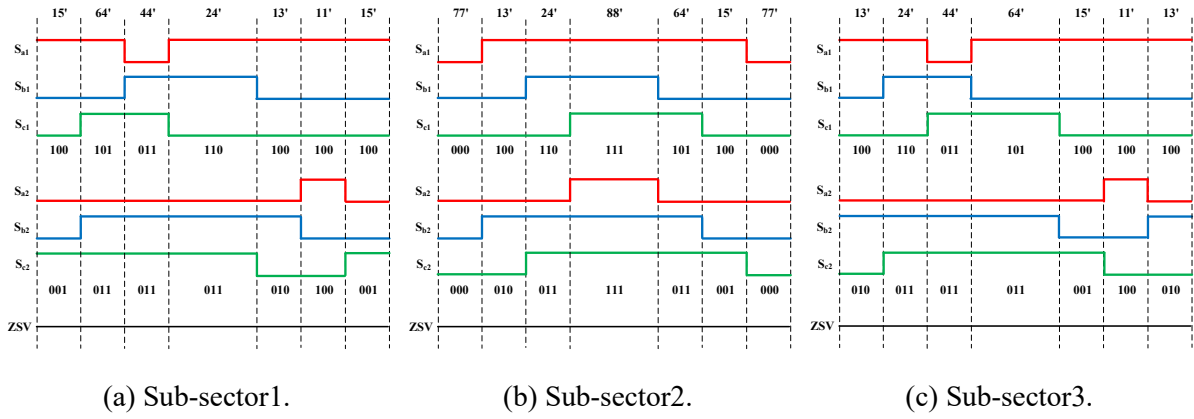


Fig. 5.17 PWM waveforms of proposed SVPWM strategy with the asymmetric vector sequence in sector 1.

### 5.3.3 Zero sequence current control

In addition to the PWM, ZSV can also be generated by some other sources, such as back-EMF harmonics, inverter nonlinearity, and cross coupling voltage in the zero sequence of the OW control system. Many ZSC control methods have been studied by researchers [BAI04] [SOM04] [SOM08a] [AN16] [LIN19]. However, they are not suitable for the proposed SVPWM strategy due to asymmetric PWM waveforms. Therefore, a more generalized ZSC control method is proposed in this chapter. To eliminate ZSV, a ZSV control loop is constructed as shown in Fig. 5.18. A redistribution time  $T_z$  is used to adjust the PWM waveforms of two inverters. Consequently, an adjustable ZSV component can be generated by PWM to counteract the ZSV components that are caused by other sources. If  $T_z$  is positive, the turn-on time will be left-shifted by  $T_z/2$  and the turn-off time will be right-shifted by  $T_z/2$  in Inverter I, while the turn-on time will be right-shifted by  $T_z/2$  and the turn-off time will be left-shifted by  $T_z/2$  in Inverter II. If the redistribution time  $T_z$  is negative, the shift directions of turn-on and turn-off times are opposite for two inverters. The PWM waveforms of the proposed PWM strategy with the asymmetric vector sequence in three sub-sectors in sector 1 are shown in Fig. 5.19 and Fig. 5.20 when  $T_z$  is positive and negative, respectively. When  $T_z$  is positive, there are six positive pulses whose ZSV is  $V_{dc} / 3$ . When  $T_z$  is negative, there are six negative pulses whose ZSV is  $-V_{dc} / 3$ .

The relationship between  $T_z$  and ZSV generated by PWM can be expressed as

$$V_0 = \frac{6T_z}{T_{PWM}} \frac{V_{dc}}{3} = \frac{2T_z}{T_{PWM}} V_{dc} \quad (5.8)$$

where  $T_{PWM}$  is the time of a PWM cycle,  $V_{dc}$  is the voltage of DC-bus.

The error between the reference and feedback of ZSC is sent into a proportional resonant controller, and its output is the reference ZSV  $V_0^*$ . The redistribution time  $T_z$  can be calculated by

$$T_z = \frac{V_0^* T_{PWM}}{2V_{dc}} \quad (5.9)$$

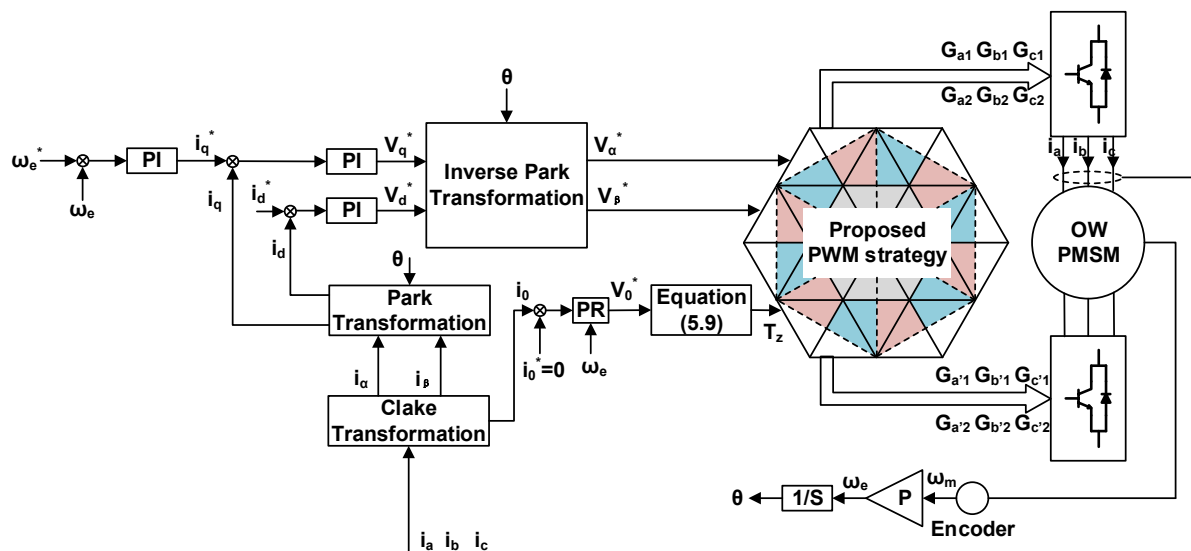


Fig. 5.18 Control block diagram of the proposed SVPWM strategy.

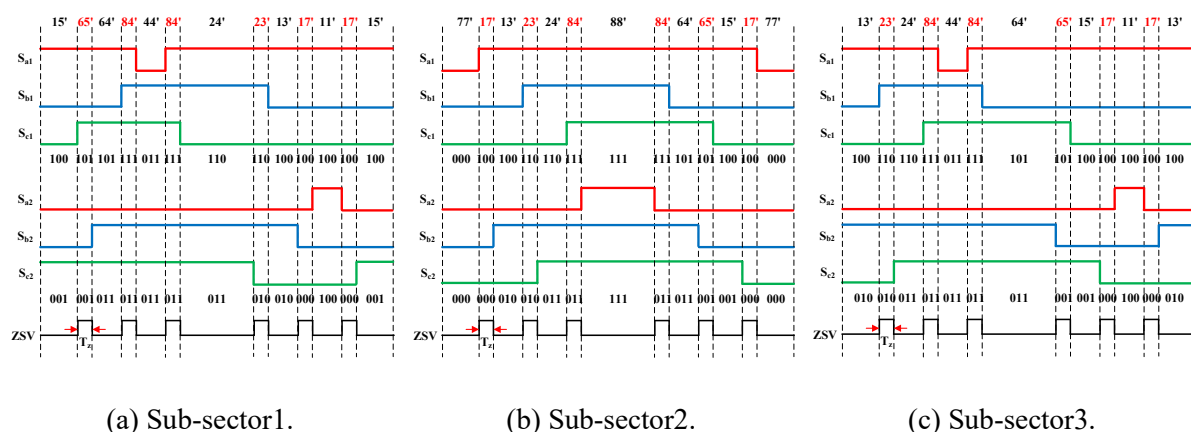


Fig. 5.19 PWM waveforms of the proposed SVPWM strategy (asymmetric vector sequence) in sector 1 when  $T_z$  is positive.

For the control block diagram of the conventional SVPWM in Fig. 5.5, two inverters are controlled independently and two reference voltages are needed for two inverters. For the control block diagram of the proposed SVPWM in Fig. 5.18, the OW inverter is regarded as

one control target and only the reference voltages for the OW inverter are needed. Moreover, the relationships between the reference ZSV and the time shift are different in (5.4) and (5.9).

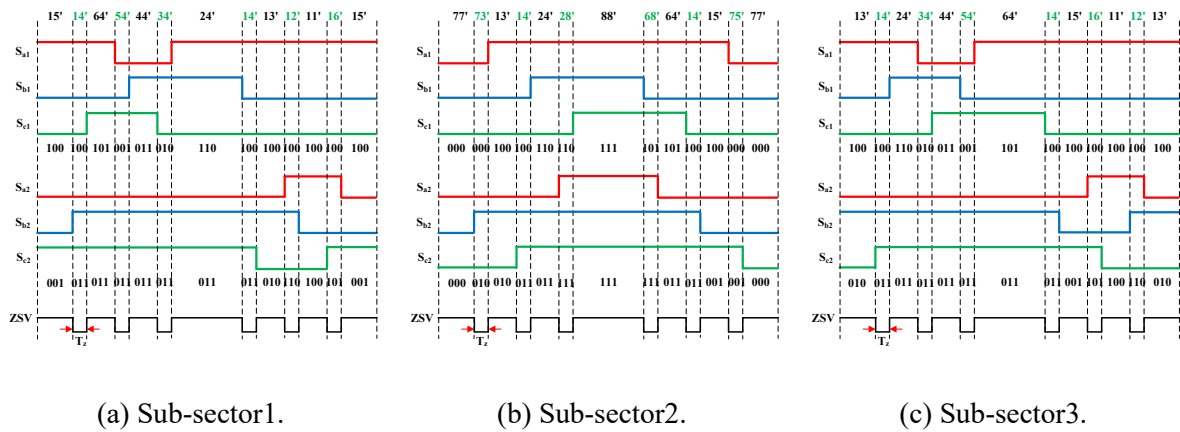
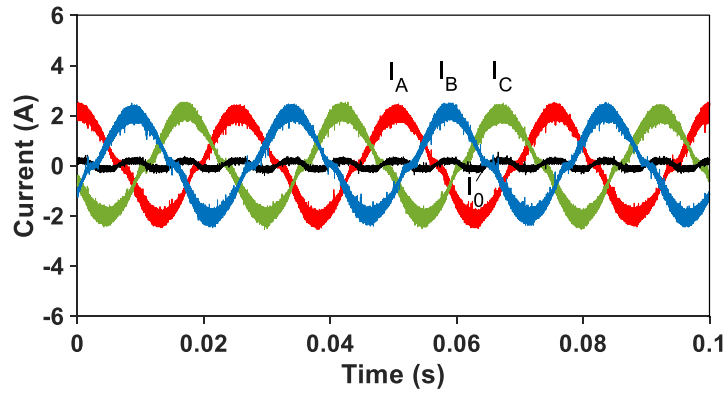


Fig. 5.20 PWM waveforms of the proposed SVPWM strategy (asymmetric vector sequence) in sector 1 when  $T_z$  is negative.

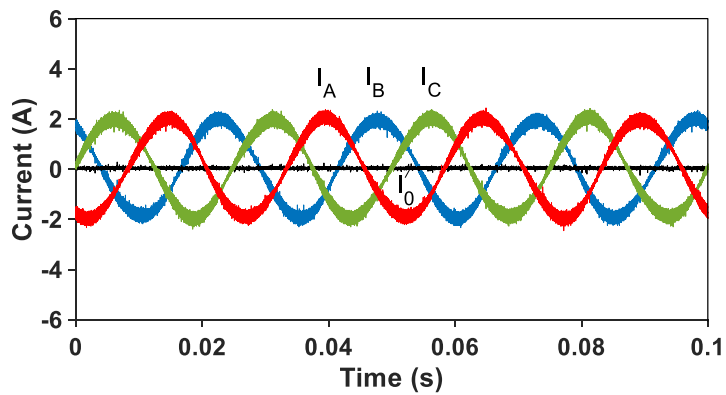
## 5.4 Experiment Results

The conventional and proposed SVPWM strategies for an OW-PMSM driven by dual two-level inverters with a common DC-bus are validated experimentally. The parameters of the OW-PMSM are listed in Table 3.6. The PWM carrier frequency and sampling frequency are 5kHz, and the dead-time is set to 2 $\mu$ s. The DC-bus voltage is 30V. The pictures of the experiment platform are shown in Fig. 3.9.

Fig. 5.21 (a) and (b) shows the measured three phase currents and ZSC with and without the zero sequence control, respectively. There is a large ZSC when the zero sequence control is not applied. Although the ZSV caused by the SVPWM strategy is zero, the ZSV can also be generated by other factors as mentioned earlier. After the zero-sequence control, ZSC can be controlled to zero. As a result, the proposed zero sequence control is effective for the proposed SVPWM strategy.



(a) Without ZSC control.



(b) With ZSC control.

Fig. 5.21 Three phase currents and ZSC of the proposed method.

The measured three phase currents, high-frequency, and low-frequency spectra of the conventional and proposed SVPWM strategies with symmetrical and asymmetric vector sequences at different modulation indices are compared in Figs. 5.22 - 27. With the change of the modulation index, the reference voltage vector will scan different regions in the space vector plane of dual two-level inverters. For example, when the modulation index is lower than  $1/\sqrt{3}$ , the reference voltage vector is always located in sub-sector 2 of each sector. As a result, the vectors and their sequence are the same for the conventional and proposed SVPWM strategies. In Fig. 5.22, the modulation index is 0.4, and the conventional and proposed SVPWM strategies with the symmetrical vector sequence have the same current spectra. When the modulation index is larger than  $1/\sqrt{3}$ , the reference voltage vector will go through sub-sectors 1 and 3, and two new vector sequences are used in the proposed SVPWM strategy. In Fig. 5.23 and Fig. 5.24, the modulation indices are 0.6 and 0.8 respectively, and the current

harmonics of the proposed SVPWM strategy are lower than those of the conventional SVPWM strategy. Comparing the spectra of symmetrical and asymmetric vector sequences in Figs. 5.22 - 27, it can be observed that harmonics with odd multiples of PWM carrier frequency are eliminated from the spectra of the asymmetric vector sequence, and the harmonics with even multiples of PWM carrier frequency are almost the same for both vector sequences. The reason is that the current ripple trajectory in the first half PWM cycle is the same as that in the second half PWM cycle with applying the asymmetric vector sequence, as shown in Fig. 5.13, but they are different in the symmetrical vector sequence in Fig. 5.11. As a result, the asymmetric vector sequence can reduce high-frequency current harmonics by eliminating the harmonics with odd multiples of PWM carrier frequency. However, due to the difference between sampled and actual currents caused by the DC-biased current trajectories in the conventional SVPWM with an asymmetric vector sequence, low-order harmonics are introduced in phase currents as shown in Figs. 5.25 – 27 (a). Low-order harmonics can be reduced by the proposed SVPWM with an asymmetric vector sequence, and maintain the reduction of high-frequency harmonics as shown in Figs. 5.25 – 27(b).

The measured total magnitudes of harmonic currents of the conventional and proposed SVPWM strategies with different modulation indices are compared in Fig. 5.28. It needs to note that the maximum modulation index cannot reach 1.0 and is about 0.96 due to the control of ZSC. As shown in Fig. 5.28, when the symmetrical vector sequence is used in both conventional and proposed PWM strategies, the current harmonics of the proposed SVPWM strategy are the same as these of the conventional SVPWM strategy when the modulation index is lower than  $1/\sqrt{3}$ . If the modulation index is higher than  $1/\sqrt{3}$ , the current harmonics of the proposed SVPWM strategy are lower than these of the conventional SVPWM strategy. The reason is that vectors and their action sequences of the proposed SVPWM strategy are the same as these of the conventional SVPWM strategy when the modulation index is lower than  $1/\sqrt{3}$ , and vectors and their action sequences are optimized in the proposed SVPWM strategy when the modulation index is higher than  $1/\sqrt{3}$ . The conventional SVPWM with an asymmetric vector sequence can reduce high-frequency harmonics compared with the symmetrical vector sequence conventional SVPWM, but also induce low-order harmonics, and the total harmonics are similar to those of the conventional SVPWM. When the asymmetric vector sequence is applied, the current harmonics of the proposed SVPWM strategy can be reduced in the middle



and high modulation regions. Overall, the proposed SVPWM strategy with an asymmetric vector sequence has the best current harmonic characteristic.

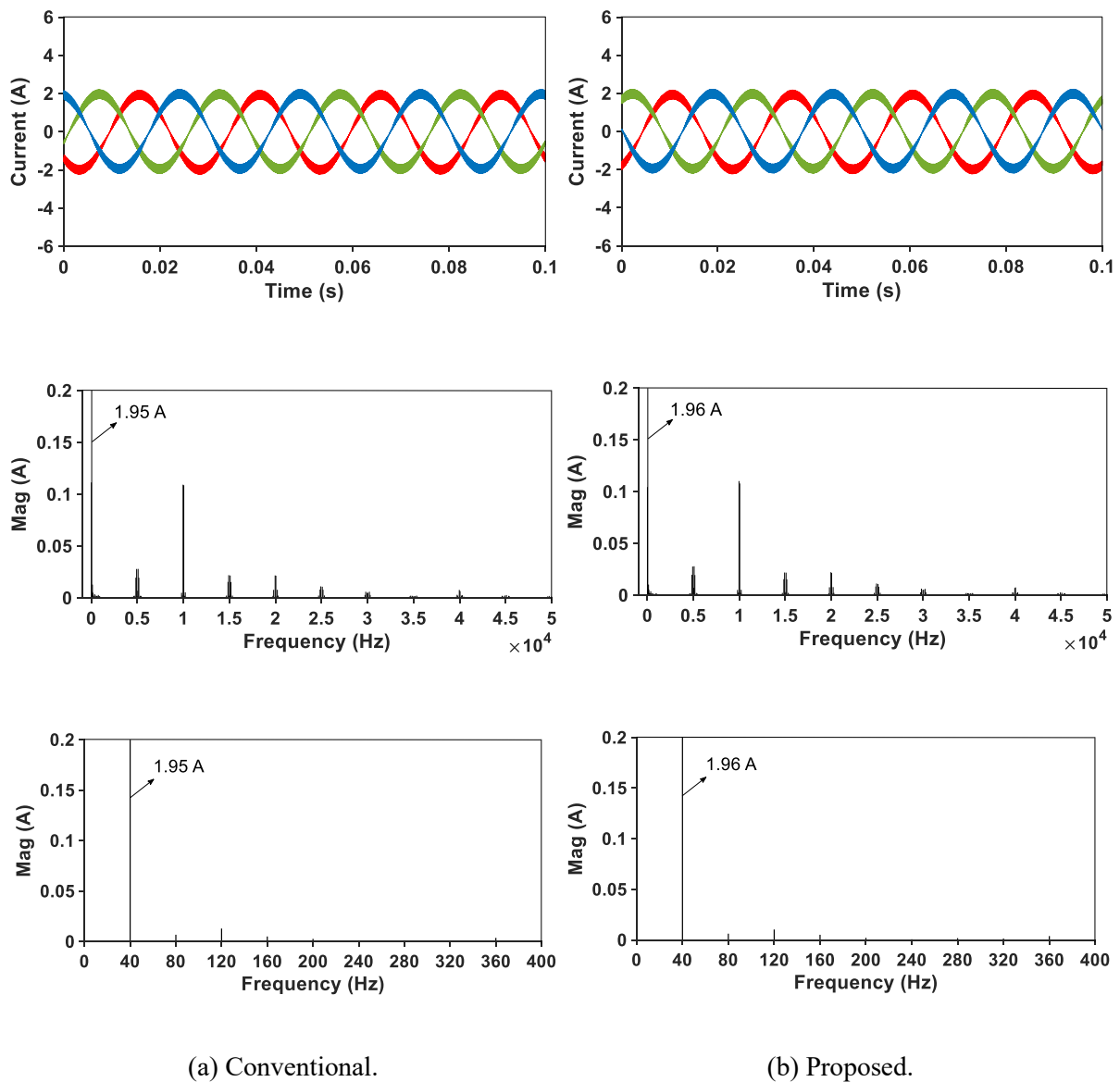
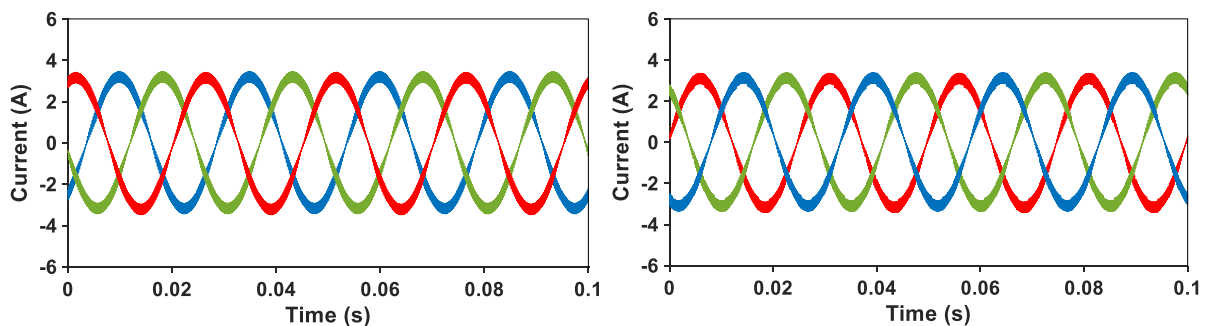


Fig. 5.22 Measured waveforms and spectra of phase current in conventional and proposed SVPWM strategies with the symmetrical vector sequence (MI=0.4).



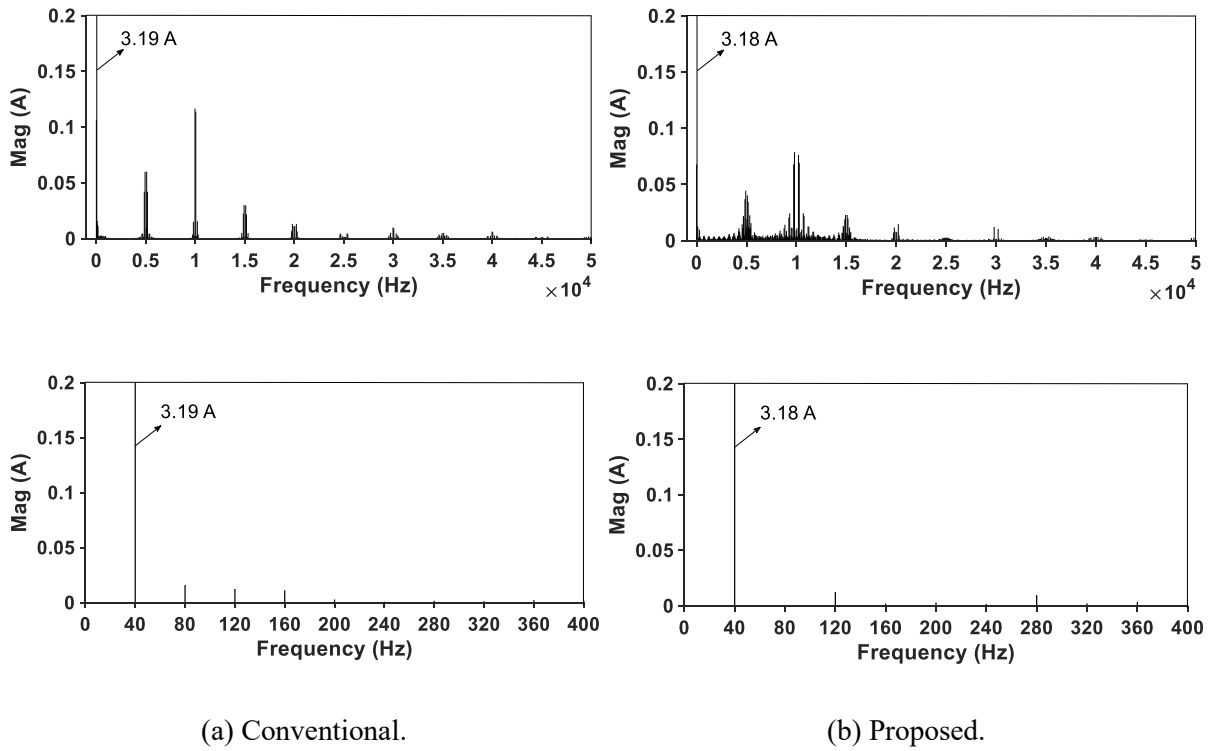
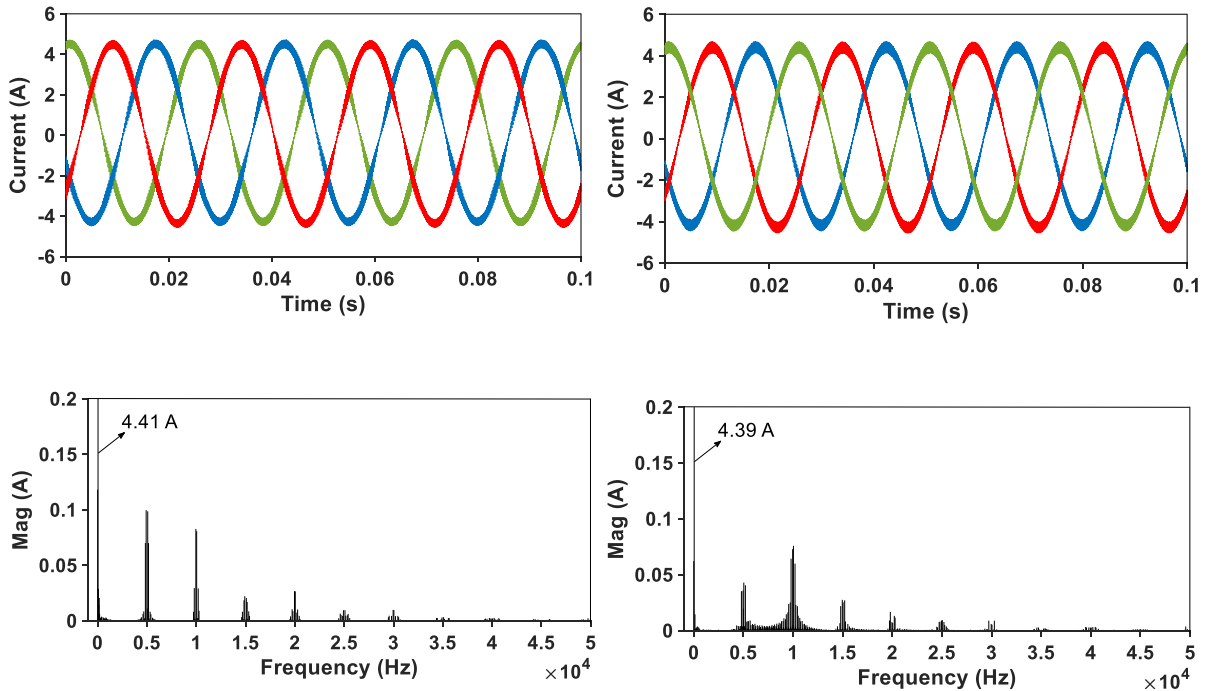
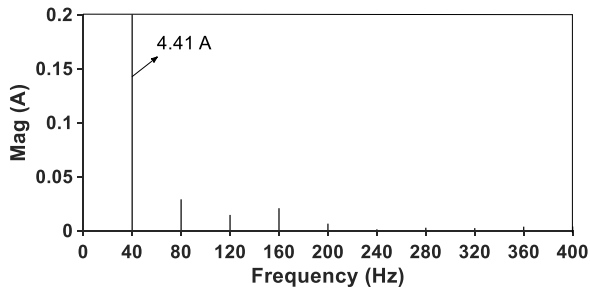
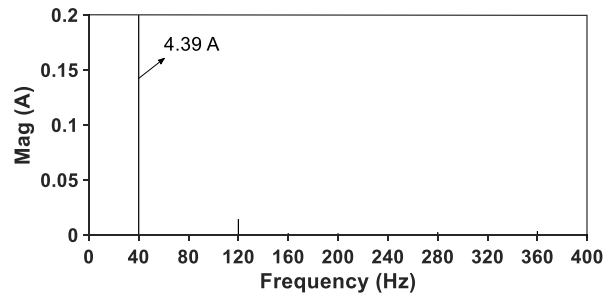


Fig. 5.23 Measured waveforms and spectra of phase current in conventional and proposed SVPWM strategies with the symmetrical vector sequence (MI=0.6).



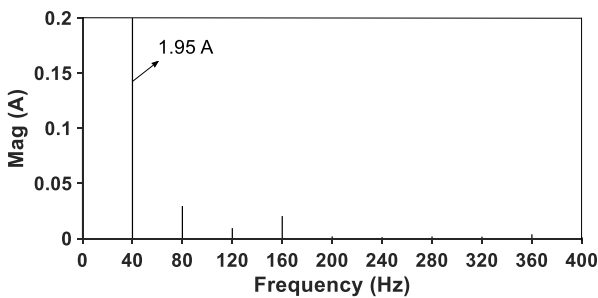
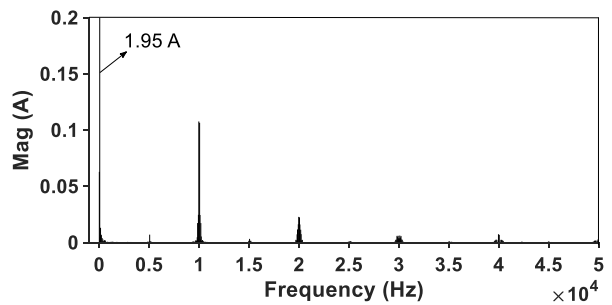
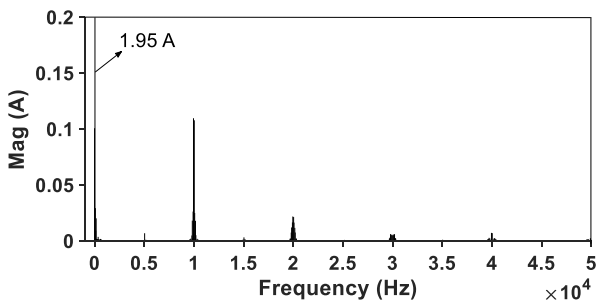
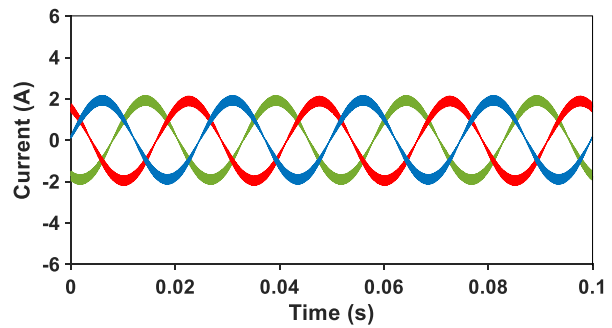
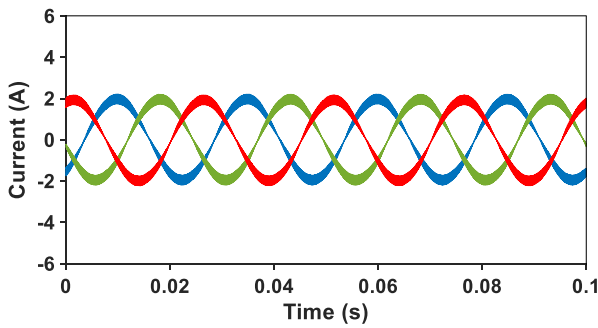


(a) Conventional.

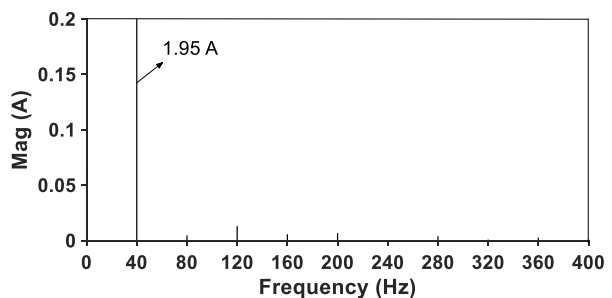


(b) Proposed.

Fig. 5.24 Measured waveforms and spectra of phase current in conventional and proposed SVPWM strategies with the symmetrical vector sequence (MI=0.8).



(a) Conventional.



(b) Proposed.

Fig. 5.25 Measured waveforms and spectra of phase current in conventional and proposed SVPWM strategies with the asymmetric vector sequence (MI=0.4).

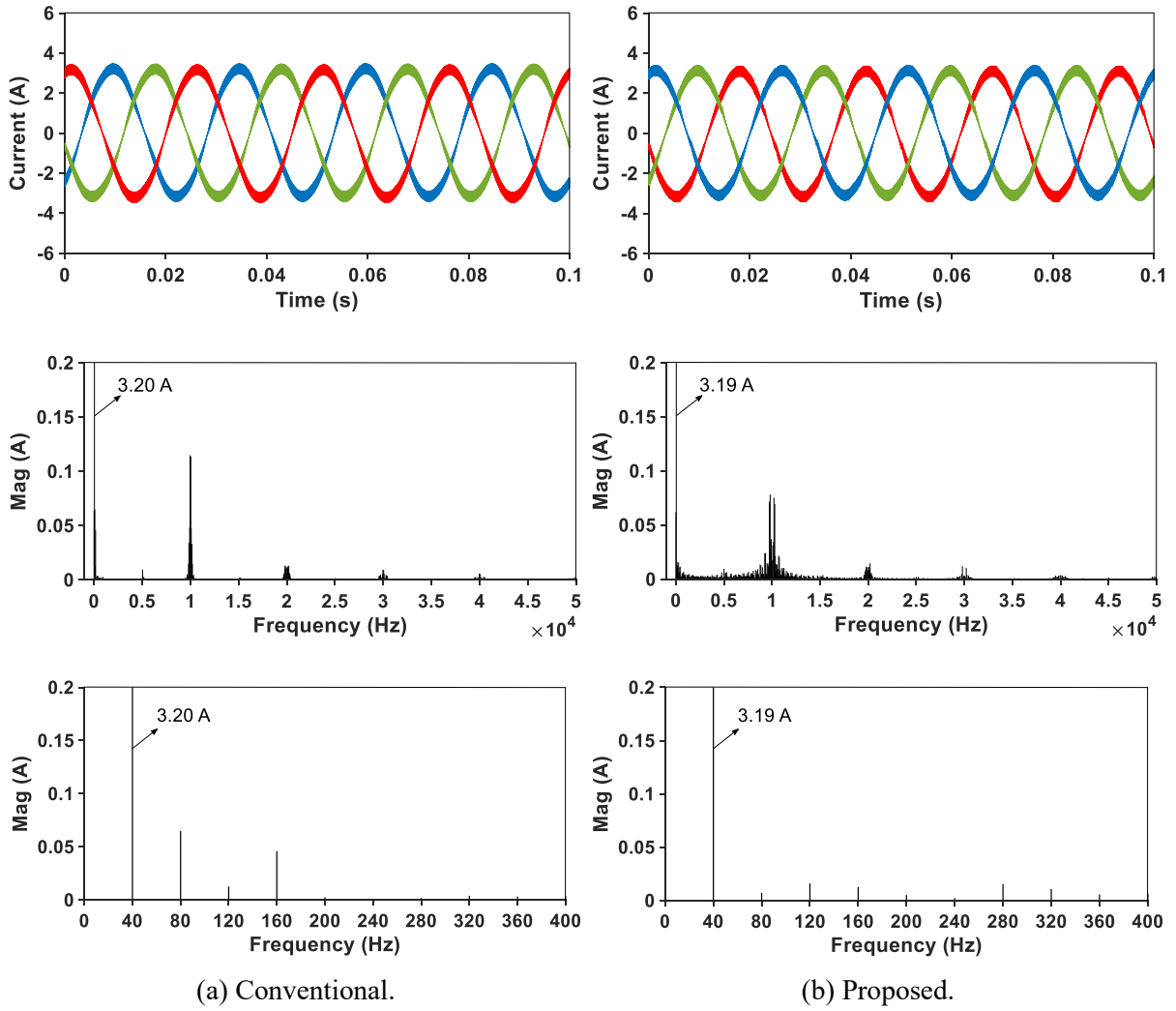
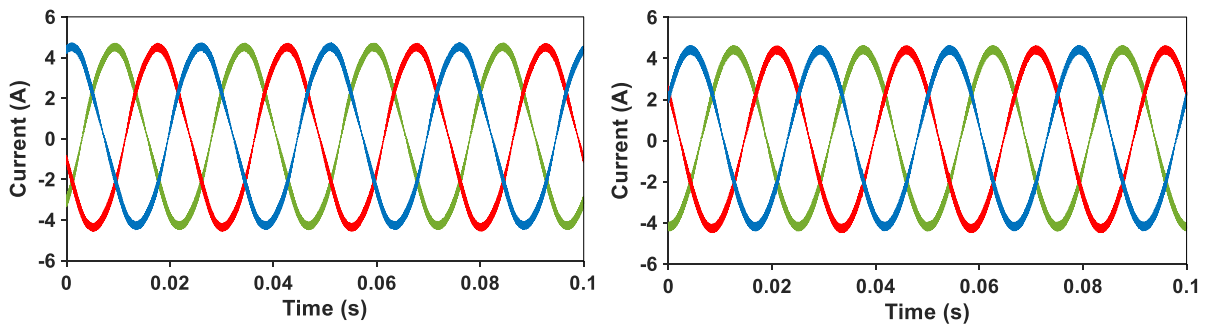


Fig. 5.26 Measured waveforms and spectra of phase current in conventional and proposed SVPWM strategies with the asymmetric vector sequence (MI=0.6).



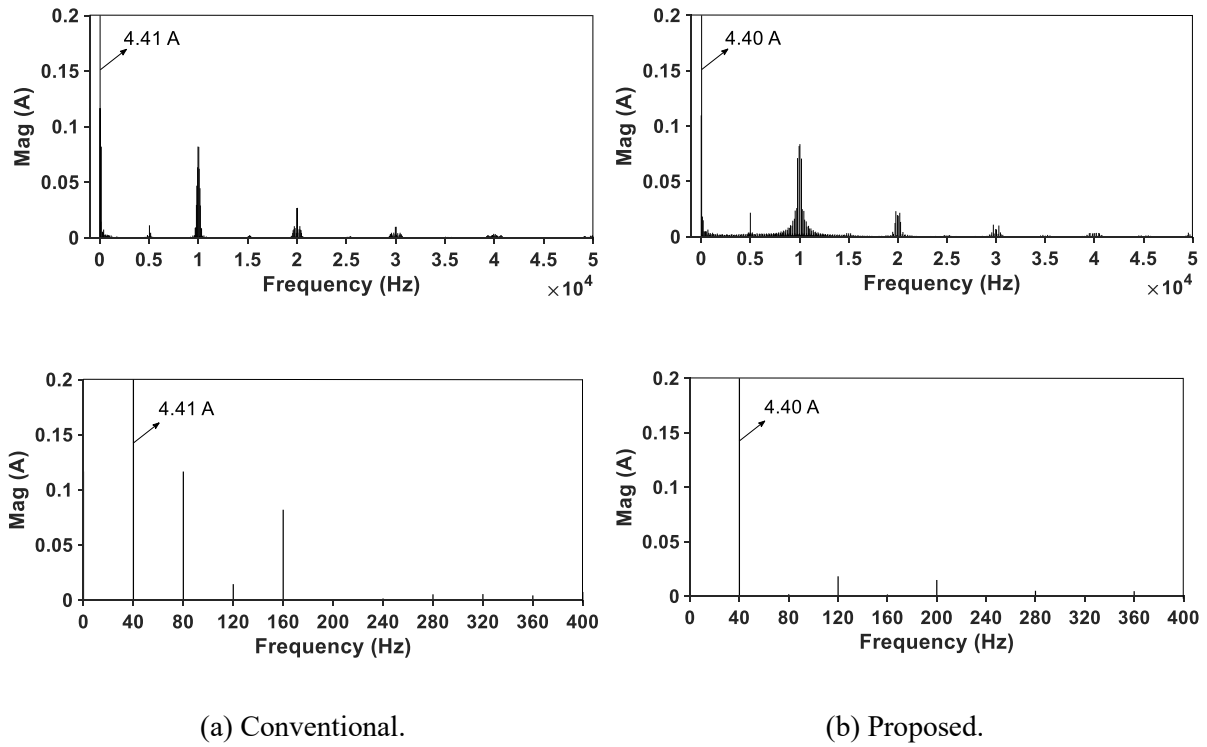


Fig. 5.27 Measured waveforms and spectra of phase current in conventional and proposed SVPWM strategies with the asymmetric vector sequence (MI=0.8).

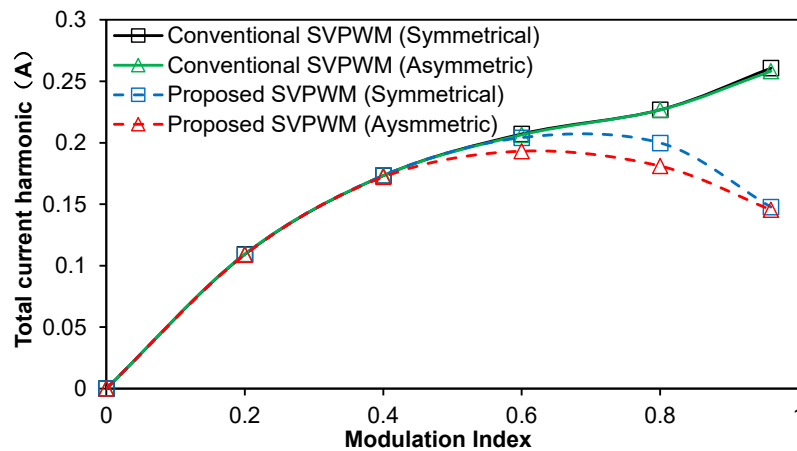


Fig. 5.28 Comparison of the measured total current harmonic magnitudes of conventional and proposed SVPWM strategies.

## 5.5 Summary

In this chapter, a novel SVPWM strategy for an OW machine fed by common DC-bus dual two-level three phase inverters is proposed, in which each sector is divided into three sub-sectors in the space vector plane, and three vector action sequences for zero and effective vectors in each sub-sector are analysed. It is found that the optimal effective and zero voltage

vector action sequences are different and can be employed to significantly reduce current harmonics in high modulation regions without increasing switching frequency. Besides, the asymmetric vector action sequence is analysed in this chapter, which can generate low-order harmonics in phase currents with the conventional SVPWM, and this issue can be solved by the proposed SVPWM. Experiment results have validated the superiority of the proposed SVPWM strategy. Furthermore, the zero sequence control of the proposed SVPWM strategy is introduced to suppress ZSC in this chapter. In the next chapter, common mode voltage issues in the common DC-bus dual two-level inverters are investigated, and the ZSC suppression and the common mode voltage variation elimination can be achieved simultaneously.

# CHAPTER 6 ZERO SEQUENCE CURRENT SUPPRESSION STRATEGY FOR OPEN WINDING PMSM DRIVES WITH CONSTANT COMMON MODE VOLTAGE

In Chapter 5, the effects of vector action sequences on the current harmonics are studied, and the ZSC control is designed for the novel SVPWM strategy. In this chapter, both ZSC and CMV control of common DC-bus dual two-level inverters will be investigated. ZSV can cause circulating current, while the variation of CMV can cause bearing current in an OW-PMSM fed by common DC-bus dual two-level inverters. In this chapter, a novel SVPWM strategy is proposed for both the CMV variation elimination and low/high-frequency ZSC suppression by the optimal selection of switching combinations. The conventional CMV control can usually limit the utilization of switching combinations and may induce large high-frequency ZSC harmonics. The proposed SVPWM can minimize the effect of the CMV control on the ZSC control. Moreover, the proposed SVPWM can achieve ZSC suppression in both linear and over modulation regions with constant CMV. Compared with the conventional CMV elimination PWM, the proposed SVPWM shows advantages in low switching frequency, low ZSC harmonics, and controlled ZSC in the over modulation region as verified by experiment.

This chapter has been submitted to *IEEE Journal of Emerging and Selected Topics in Power Electronics* and is currently under review.

## 6.1 Introduction

In an OW-PMSM fed by dual two-level inverters, ZSV and CMV are different, although they are equal to each other in a two-level inverter fed three phase machine [KAL15]. ZSV can be caused by PWM, inverter nonlinearity, the triplen BEMF harmonics of PMSM and coupling voltages in zero sequence [ZHA17a]. In the common DC-bus OW drive, ZSV can generate zero sequence circulation current through the zero sequence circuit, and thus extra loss and torque ripples can be induced. As a result, the control of ZSC is necessary in a common DC-

bus OW-PMSM drive. On the other hand, CMV variation can cause shaft voltage variation, and thus generate bearing current, which can cause the failure of bearings [KAL15]. Both ZSC and CMV should be controlled in a common DC-bus OW-PMSM drive. At present, abundant literatures have been published to report and solve the ZSC problem in an OW drive with common DC-bus dual two-level inverters [SOM02] [SOM04] [SRI14] [ZHO15] [ZHA17a], which have been introduced in Section 1.5.1.

In a voltage source inverter, fast switching devices are used and operated at a high-frequency. This can acquire good output voltage profiles, but also cause a high-frequency variation of CMV, which will cause the bearing current problem. The problem should also be considered in an OW machine drive. The abundant switching combinations in dual inverters provide the possibility to eliminate the variation of CMV. The difference between ZSV and CMV in an OW machine fed by dual inverters is described in [KAL15], and hybrid PWMs are designed to reduce CMV in the magnitude and the number of levels for isolated DC-bus OW drive. However, this method can only be used in the dual inverters with isolated DC-bus, since the PWM can generate uncontrollable ZSVs, and thus cause large ZSC in the common DC-bus topology. In [SRI10] and [BAR15], switching combinations with the same CMV are used in the common DC-bus dual inverters, and CMV can always maintain constant. Nevertheless, ZSV of these switching combinations is always zero, so that they cannot generate controllable ZSVs, and thus large ZSC will be generated by other sources except from PWM. Both of the ZSC and CMV control are considered in the CMV elimination PWM (CMVE-PWM) in [HU21]. However, large high-frequency ZSC harmonics are generated and ZSC suppression cannot be achieved in the over modulation region, and these problems will be addressed by the proposed SVPWM in this chapter.

## 6.2 Dual Inverters and Conventional PWM Strategies

### 6.2.1 Common mode voltage and zero sequence voltage in dual inverters

CMV and ZSV are the same in a two-level inverter. In Inverters I and II, they can be expressed as

$$\begin{aligned} V_{CMV1} = V_{ZSV1} &= \frac{V_{AO} + V_{BO} + V_{CO}}{3} \\ V_{CMV2} = V_{ZSV2} &= \frac{V_{A'O} + V_{B'O} + V_{C'O}}{3} \end{aligned} \quad (6.1)$$



where  $V_{CMV1}$  and  $V_{CMV2}$  are the common mode voltages of two two-level inverters, respectively.  $V_{ZSV1}$  and  $V_{ZSV2}$  are the ZSVs of two two-level inverters, respectively.  $V_{AO}$ ,  $V_{BO}$ ,  $V_{CO}$  are the three pole voltages of Inverter I, and  $V_{A'O}$ ,  $V_{B'O}$ ,  $V_{C'O}$  are the three pole voltages of Inverter II.

On the other hand, CMV and ZSV are different in dual two-level inverters. The variation of CMV can generate the bearing current, and the CMV of dual inverters  $V_{CMV}$  can be expressed as the average of CMVs in two two-level inverters.

$$V_{CMV} = \frac{V_{CMV1} + V_{CMV2}}{2} = \frac{V_{AO} + V_{BO} + V_{CO} + V_{A'O} + V_{B'O} + V_{C'O}}{6}. \quad (6.2)$$

All switching combinations in dual two-level inverters can be categorized by CMV in Table 6.1.

Table 6.1 CMVs of Switching combinations in Dual Inverters

CMV	Switching combinations
0	77'
$V_{dc}/6$	17', 71', 37', 73', 57', 75'
$V_{dc}/3$	11', 33', 55', 13', 15', 35', 31', 51', 53', 27', 47', 67', 72', 74', 76'
$V_{dc}/2$	78', 87', 21', 23', 25', 41', 43', 45', 61', 63', 65', 12', 14', 16', 32', 34', 36', 52', 54', 56'
$2V_{dc}/3$	22', 44', 66', 24', 26', 42', 46', 62', 64', 18', 38', 58', 81', 83', 85'
$5V_{dc}/6$	28', 48', 68', 82', 84', 86'
$V_{dc}$	88'

ZSV can cause the zero sequence circulation current in the common DC-bus OW topology. It can be expressed as the difference between CMVs of Inverters I and II.

$$V_{ZSV} = V_{CMV1} - V_{CMV2} = \frac{V_{AO} + V_{BO} + V_{CO} - V_{A'O} - V_{B'O} - V_{C'O}}{3}. \quad (6.3)$$

Switching combinations can also be categorized by ZSV as shown in Table 1.3. The ZSVs of switching combinations in dual inverters are highlighted in different colors in Fig. 1.32. Black represents the null ZSV of switching combinations. Red represents the positive ZSV of switching combinations, while green represents the negative ZSV. To control ZSC, PWM should generate a controllable ZSV to counteract with ZSVs from other sources. Making a full use of these switching combinations with null and non-null ZSVs, ZSC can be controlled.

### 6.2.2 Conventional CMV elimination PWM strategy

In an OW-PMSM fed by dual two-level inverters with a common DC-bus, ZSVs can be generated by PWM, the triplen BEMF harmonics, inverter nonlinearity, and zero sequence component of coupling voltages [ZHA17a]. Due to the existence of zero sequence circuit in common DC-bus dual two-level inverters, ZSC will be introduced by ZSV, and cause extra cost and torque ripples in the OW-PMSM. Consequently, the suppression of ZSC is necessary. CMV in dual inverters also needs to be controlled due to the negative effects of bearing currents.

A CMVE-PWM strategy is proposed in [HU21] for an OW-PMSM drive with both the ZSC suppression and CMV variation elimination. The carrier signals of Inverters I and II have a 180-degree phase difference, and two legs of each H-bridge have completely opposite drive signals as shown in Fig. 6.1. Consequently, according to (6.2), the CMV can always be kept on the constant value of  $V_{dc}/2$ . In the view point of switching combinations' CMV, it can be seen that all switching combinations in Fig. 6.1 have the same CMV of  $V_{dc}/2$  according to Table 6.1. In an OW-PMSM fed by common DC-bus dual inverters, the control of ZSC is necessary. The PWM strategy in [HU21] can redistribute the zero vectors  $78^\circ$  and  $87^\circ$ , whose ZSV are  $-V_{dc}$  and  $V_{dc}$ , respectively, to maintain the average ZSV in a PWM cycle equals the reference ZSV, and thus low-frequency ZSC can be suppressed. However, this PWM strategy has a drawback of the large variation of ZSV from  $-V_{dc}$  to  $V_{dc}$  as shown in Fig. 6.1, which can cause large high-frequency ZSC harmonics.

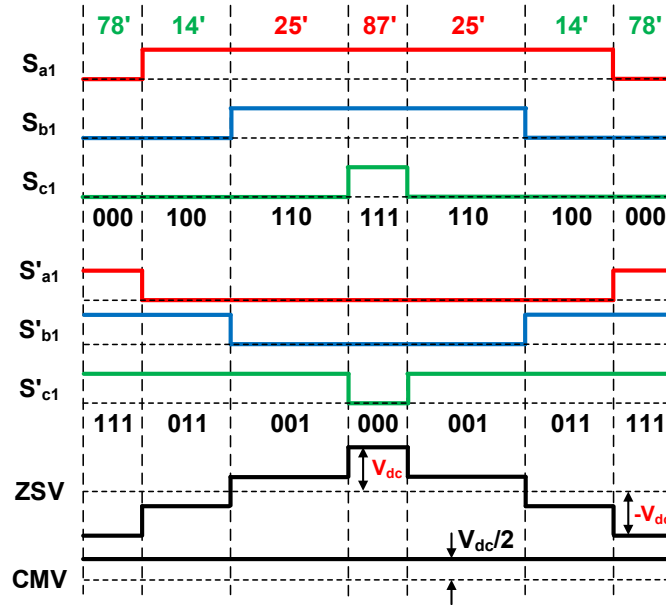


Fig. 6.1 PWM waveforms, ZSV and CMV of PWM strategy in [HU21].

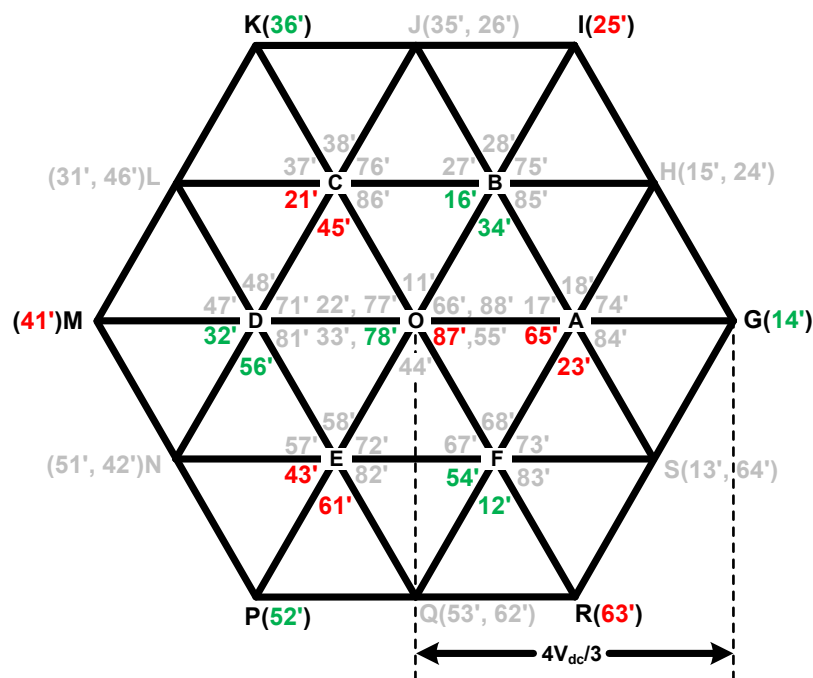
In [HU21], both positive and negative ZSVs are generated at the same time by PWM in Fig. 6.1, so that large ZSC harmonics are generated. Although the conventional CMVE-PWM can eliminate the variation of CMV, it also degraded the current harmonic characteristic. The problem will be solved in the proposed SVPWM, and the ZSV from PWM can only be positive or negative in a PWM cycle, and has the same sign with the reference ZSV. Moreover, the conventional CMVE-PWM cannot achieve ZSC suppression in the over modulation operation, since only switching combinations with non-null ZSV are used and ZSV changes with durations of switching combinations in the over modulation region. In this chapter, a novel SVPWM strategy is proposed for an OW-PMSM drive with a common DC-bus to achieve the CMV variation elimination and low/high-frequency ZSC harmonic suppression simultaneously in both linear and over modulation regions.

### 6.3 Proposed SVPWM Strategy

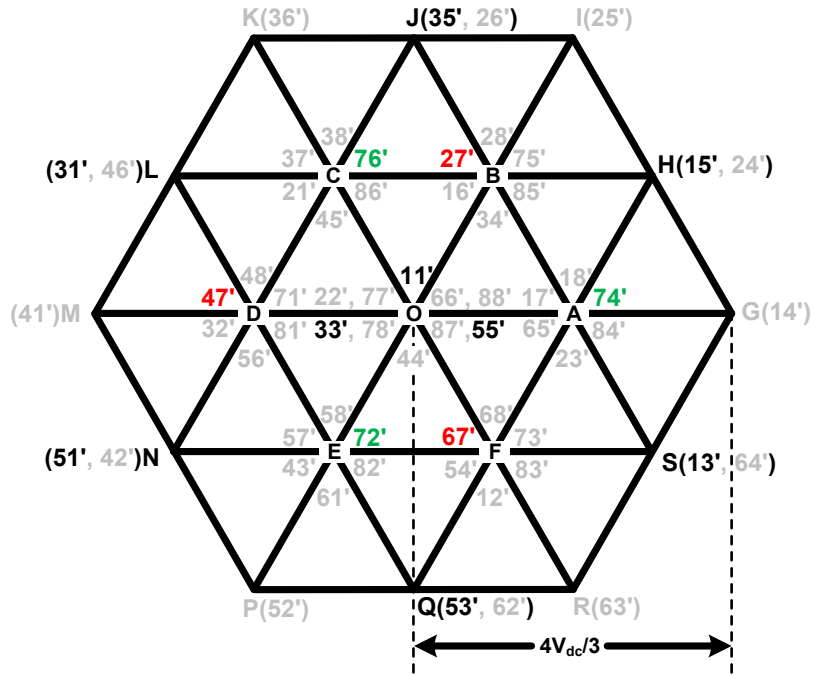
#### 6.3.1 Switching combination groups in space vector plane of dual inverters

In order to eliminate the variation of CMV, switching combinations with the same CMV are used to design the proposed SVPWM strategy in this chapter. All switching combinations in dual inverters are categorized into seven groups by their CMVs as shown in Table 6.1, and only the middle three groups of switching combinations can be used for the PWM strategy design, as they contain both zero vectors and effective vectors. The groups of switching combinations whose CMVs are  $V_{dc}/2$ ,  $V_{dc}/3$ , and  $2V_{dc}/3$  are highlighted in the space vector plane in Fig. 6.2 (a), (b), and (c), respectively. Exclusively using the switching combinations that have the same CMV can eliminate the variation of CMV, so that there are three candidates

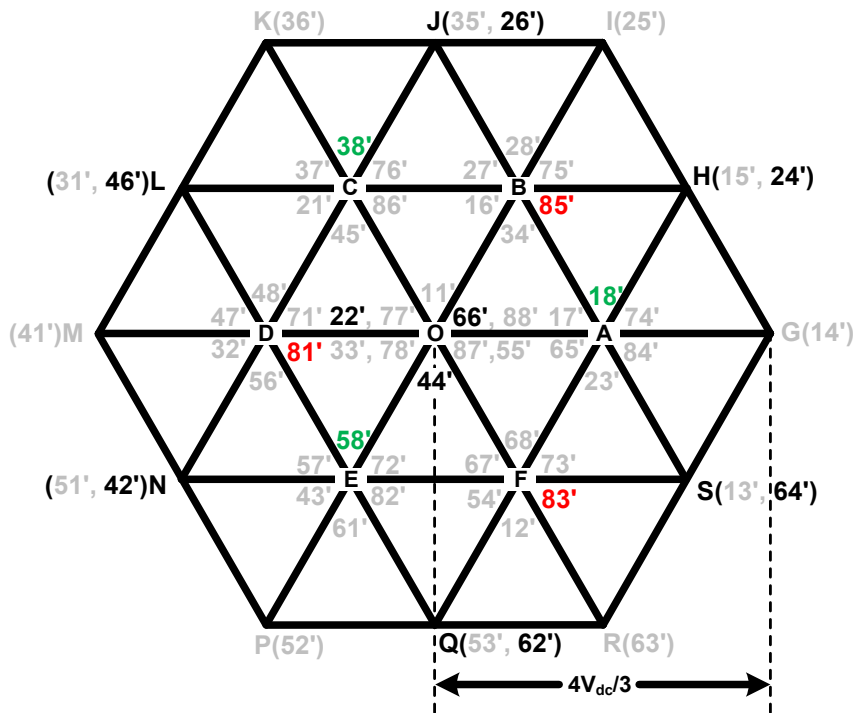
of switching combination groups for the PWM design. Switching combinations can also be categorized by their ZSVs in Table 1.3, and highlighted in different colors in Fig. 6.2, i.e. positive ZSV (red), negative ZSV (green), and null ZSV (black). The switching combinations in Fig. 6.2 (a) have positive or negative ZSVs, but have no null ZSV, so that they are not suitable for the ZSC control in the OW drive with a common DC-bus, and can induce large high-frequency ZSC harmonics. However, this group of switching combinations is the best choice for the isolated DC-bus topology, since it can reach the whole modulation region within the large hexagon in the space vector plane. If switching combinations in Fig. 6.2 (b) or (c) are used, the modulation region is the same as that in the conventional modulation method for the OW drive with a common DC-bus, and is limited within the middle hexagon. However, switching combinations in Fig. 6.2 (b) or (c) have all three types of ZSVs. As a result, these two groups of switching combinations are not suitable for the isolated DC-bus dual inverters as the smaller modulation region, but they are more suitable for the common DC-bus dual inverters in this chapter. To control zero sequence current in the common DC-bus OW machine, PWM should generate a controllable ZSV which can counteract with ZSVs formed by other sources. The controllable ZSV from PWM can be achieved by making use of both non-null ZSV switching combinations on the small hexagon and null ZSV switching combinations on the middle hexagon in Fig. 6.2 (b) or (c). Bearing in mind that switching combinations in Fig. 6.2 (b) or (c) have the same CMV, the two groups of switching combinations can be used to design the PWM strategy for both the CMV variation elimination and the ZSC control. The detailed implementation of the proposed SVPWM strategy will be described in Section 6.3.2.



(a)  $V_{dc}/2$ .



(b)  $V_{dc}/3$ .



(c)  $2V_{dc}/3$ .

Fig. 6.2 Switching combinations with the same CMV.

### 6.3.2 Proposed SVPWM strategy

The design of the proposed SVPWM strategy will be introduced in detail using the group of switching combinations with  $V_{dc}/3$  CMV in Fig. 6.2 (b), and the group of switching combinations with  $2V_{dc}/3$  CMV in Fig. 6.2 (c) can also be used in a similar way. The space vector plane is divided into 12 sectors as shown in Fig. 6.3. The control diagram of the OW drive with the proposed SVPWM strategy is shown in Fig. 6.4. In the proposed SVPWM, switching combinations have the same CMV of  $V_{dc}/3$ , so that the elimination of the CMV variation can be guaranteed inherently. Consequently, the key in the proposed SVPWM strategy is the control of ZSC, which should be achieved under the restriction of utilizing the group of switching combinations in Fig. 6.2 (b). A current close loop is applied for the control of ZSC in Fig. 6.4. The proportional resonant controller generates the reference ZSV, and the input of the controller is the difference between the ZSC reference and the feedback. To suppress ZSC, the reference ZSC is set to zero in the control block diagram. To control the overall ZSV to zero, the ZSV from PWM should equal the reference ZSV by making a full use of positive, negative, and null ZSV switching combinations in Fig. 6.2 (b). Null ZSV switching combinations are always used, while the selection of non-null ZSV switching combinations is determined by the sign of the reference ZSV. Moreover, the duration  $T_{mz}$  for non-null ZSV switching combinations is determined by the magnitude of the reference ZSV.

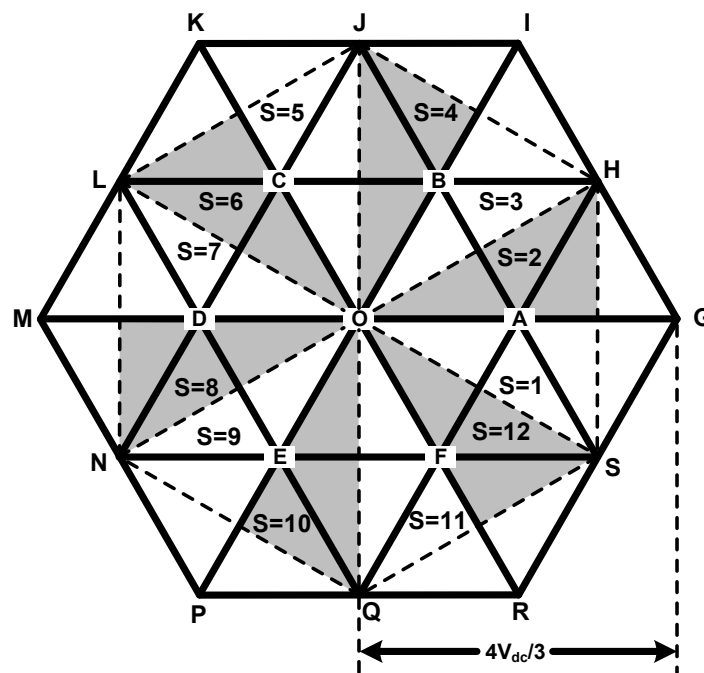


Fig. 6.3 Sectors of the proposed SVPWM strategy.

Fig. 6.5 and Fig. 6.6 show the switching combinations, voltage vectors, and PWM waveforms when the reference ZSV is positive and negative, respectively, in the proposed SVPWM strategy in sector 1. If the reference ZSV is positive, the reference voltage vector will be divided into two components, which are marked in red and blue in Fig. 6.5 (a). The two vectors are in the same direction but have different magnitudes. The blue vector is synthesized by two basic vectors with null ZSV, i.e. 15' and 13', while the red vector is synthesized by basic vectors 27' and 67'. As the corresponding switching combinations 27' and 67' have positive ZSV, they can be used to generate ZSV to counteract with the negative ZSVs caused by other sources. It can be observed that two pulses of ZSV appear as shown in Fig. 6.5 (b), and their amplitudes are  $2V_{dc}/3$ . The duration sum of two non-null ZSV switching combinations, i.e. 27' and 67', equals  $T_{nnZ}$ , and thus  $T_{nnZ} = T_{27'} + T_{67'}$ . The relationship between  $T_{nnZ}$  and the reference ZSV  $V_0^*$  can be expressed as

$$T_{nnZ} = \frac{3T_{PWM} |V_0^*|}{2V_{dc}}. \quad (6.4)$$

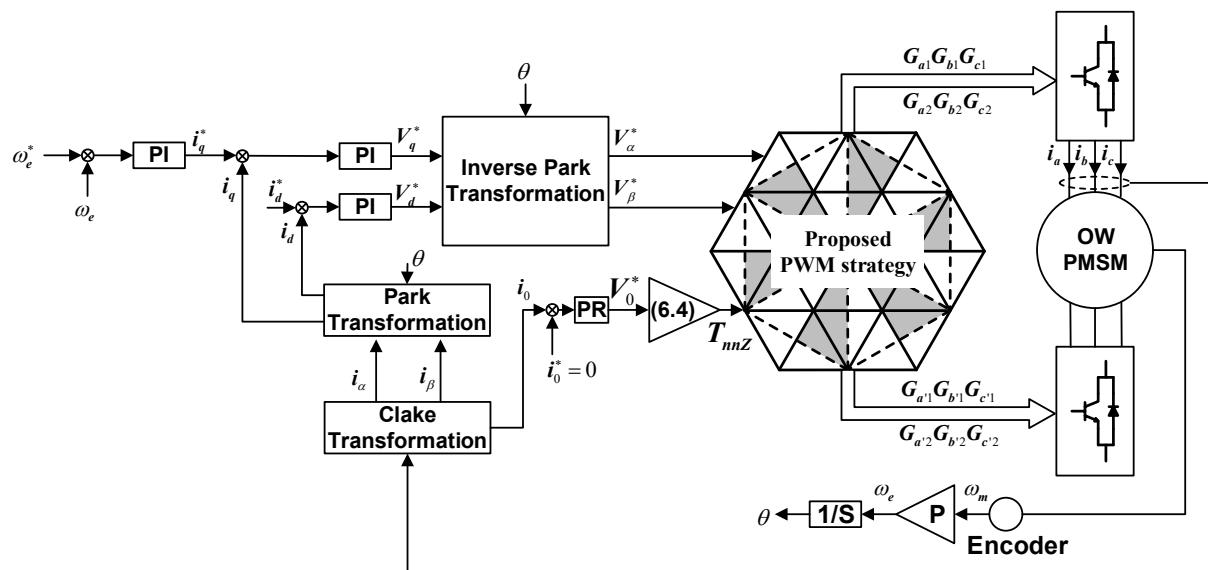


Fig. 6.4 Control diagram of the OW drive with the proposed SVPWM strategy.

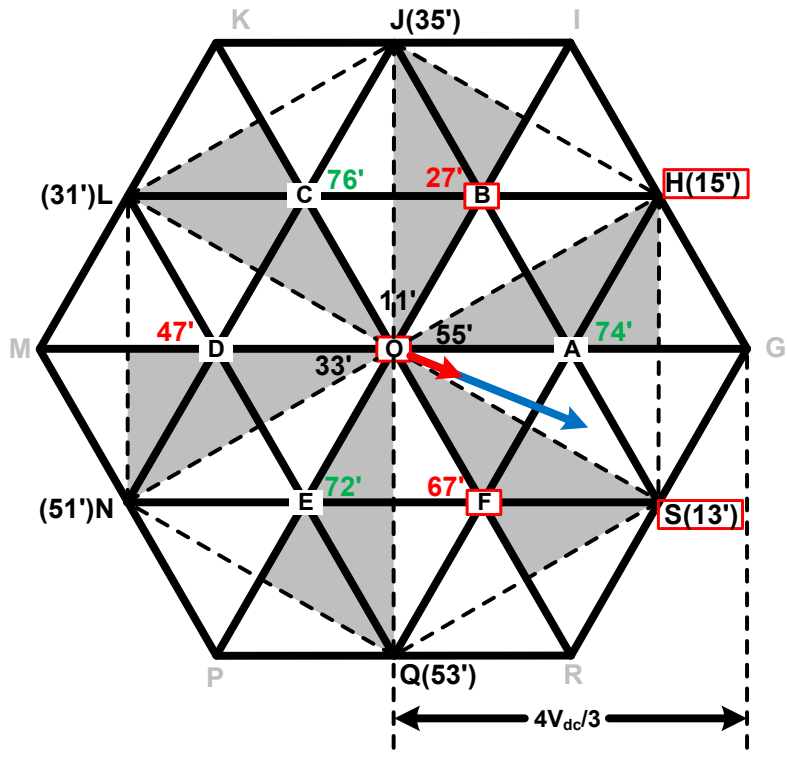
With the control of the durations for the non-null ZSV switching combinations, the ZSVs generated by 27' and 67' equals the reference ZSV  $V_0^*$ , when  $V_0^*$  is positive.

On the other hand, if the reference ZSV is negative, the reference voltage vector can also be divided into two components, which are marked in green and blue in Fig. 6.6 (a). The blue vector is synthesized by two basic vectors with null ZSV, i.e. 15' and 13', which is the same

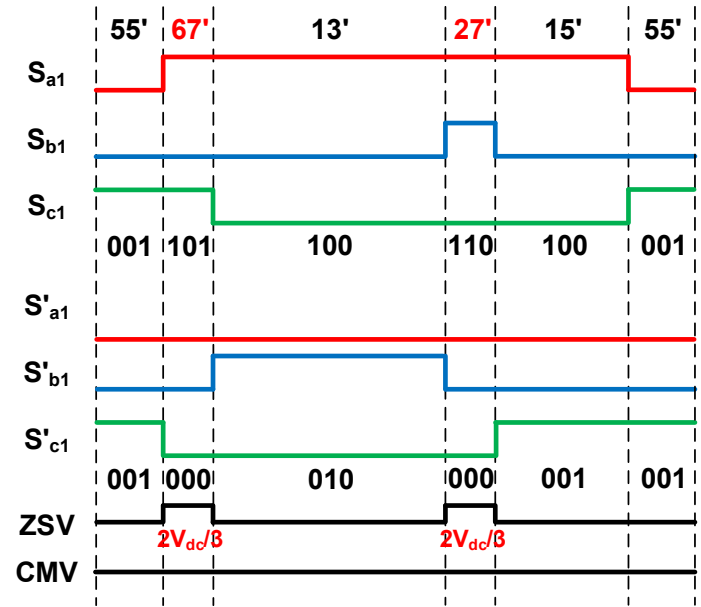
as that in Fig. 6.5 (a), while the green vector is synthesized by basic vectors 72' and 74'. The corresponding switching combinations 72' and 74' can generate negative ZSVs to counteract with the positive ZSVs caused by other sources. It can be observed that two pulses of ZSVs appear in Fig. 6.6 (b), and their amplitudes are  $-2V_{dc}/3$ . As the sum of the durations of vectors 72' and 74' is  $T_{nnZ}$ , the relationship between  $T_{nnZ}$  and the reference ZSV  $V_o^*$  can also be expressed as (6.4).

In sector 2, if the reference ZSV is positive, the location and decomposition of the reference voltage vector are shown in Fig. 6.7 (a). The switching combinations and their action sequence in Fig. 6.7 (b) are the same as those in sector 1 in Fig. 6.5 (b). However, switching combinations and their action sequence are different in sectors 1 and 2 when the reference ZSV is negative as shown in Fig. 6.6 (b) and Fig. 6.8 (b). Two non-null ZSV switching combinations change from 72', 74' to 74', 76'. The reason is that the direction of the reference voltage vector must be within the 120 degree angle between the two vectors  $\overline{OA}$  and  $\overline{OC}$  with non-null ZSV, which are corresponding to two non-null ZSV switching combinations, i.e. 74' and 76' in Fig. 6.8 (a). It can be observed that there are three positive ZSV switching combinations, i.e. 27', 47' and 67', forming three vectors  $\overline{OB}$ ,  $\overline{OD}$  and  $\overline{OF}$  with positive ZSV. Similarly,  $\overline{OA}$ ,  $\overline{OC}$  and  $\overline{OE}$  are three vectors with negative ZSV corresponding to the negative ZSV switching combinations. The angles among the three vectors with positive or negative ZSV are all 120 degrees, and thus four sectors within the 120 degree angle will use the same two non-null ZSV switching combinations to control ZSC. For example, if the reference ZSV is positive, non-null ZSV switching combinations, i.e. 27' and 67' are used in sectors 12, 1, 2, and 3. On the other hand, six basic vectors with null ZSV are formed by null ZSV switching combinations on the middle hexagon. The angle between two adjacent basic vectors with null ZSV is 60 degrees, and the corresponding null ZSV switching combinations should be used when the reference voltage vector is within the 60 degree angle. For example, null ZSV switching combinations, i.e. 13' and 15' are used in sectors 1 and 2. According to the above mentioned principles for the selection of null and non-null ZSV switching combinations, the switching combinations and their action sequences in other sectors can be acquired similarly. To design the proposed SVPWM strategy, the durations of null and non-null ZSV switching combinations should be calculated.



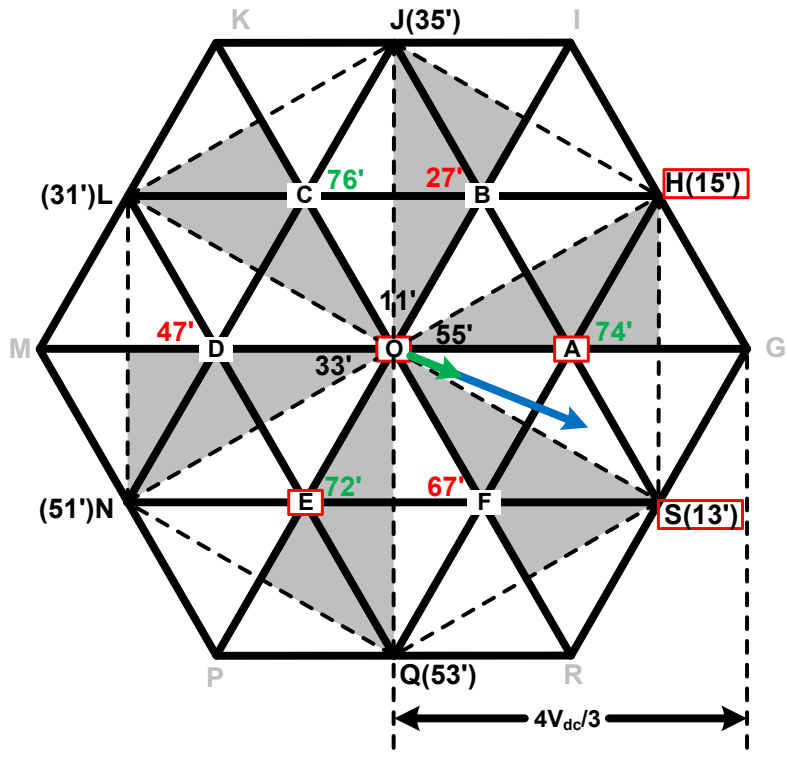


(a) Voltage vectors.

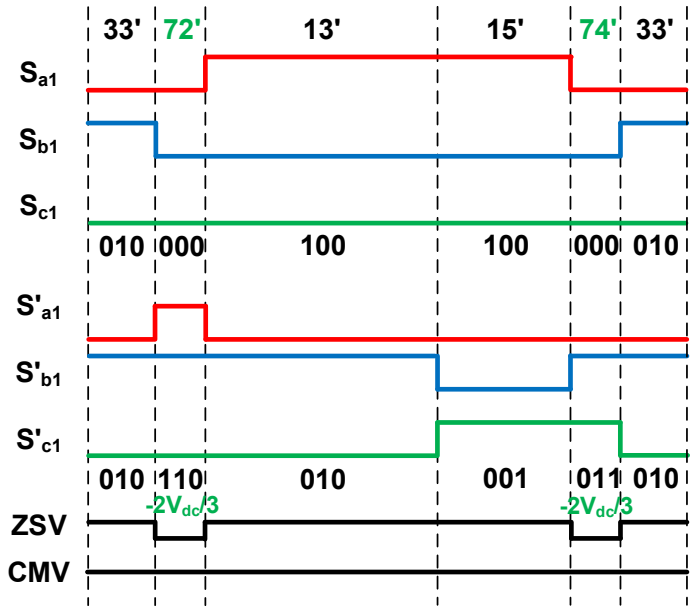


(b) PWM waveforms.

Fig. 6.5 Voltage vectors, switching combinations, and PWM waveforms in sector 1 with the proposed SVPWM strategy ( $V_o^* > 0$ ).

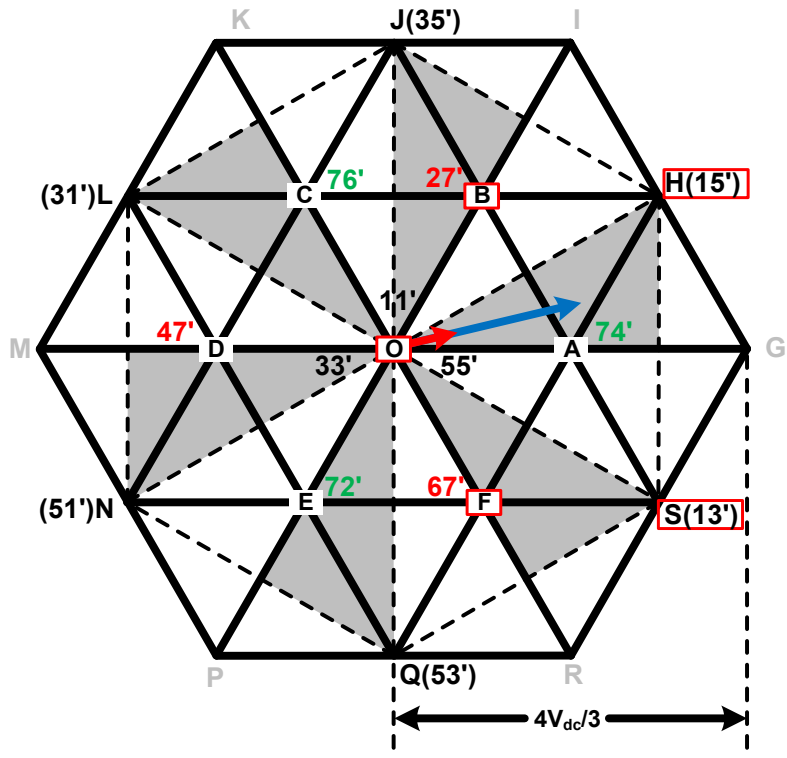


(a) Voltage vectors.

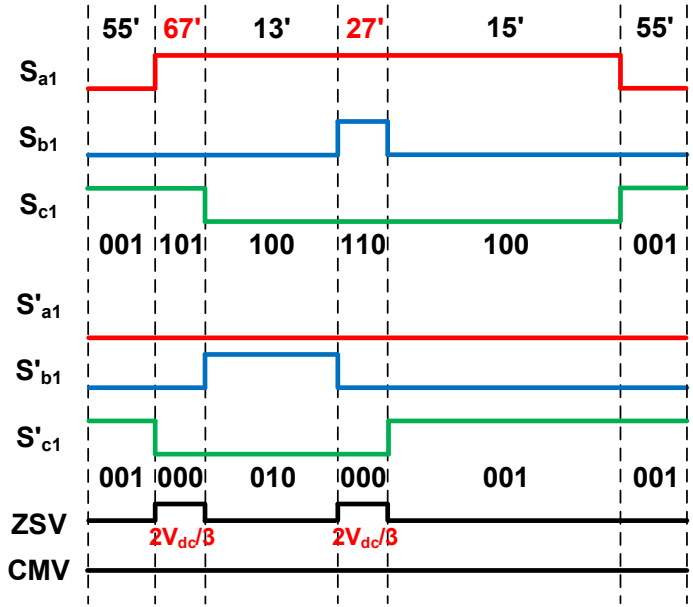


(b) PWM waveforms.

Fig. 6.6 Voltage vectors, switching combinations, and PWM waveforms in sector 1 with the proposed SVPWM strategy ( $V_0^* < 0$ ).

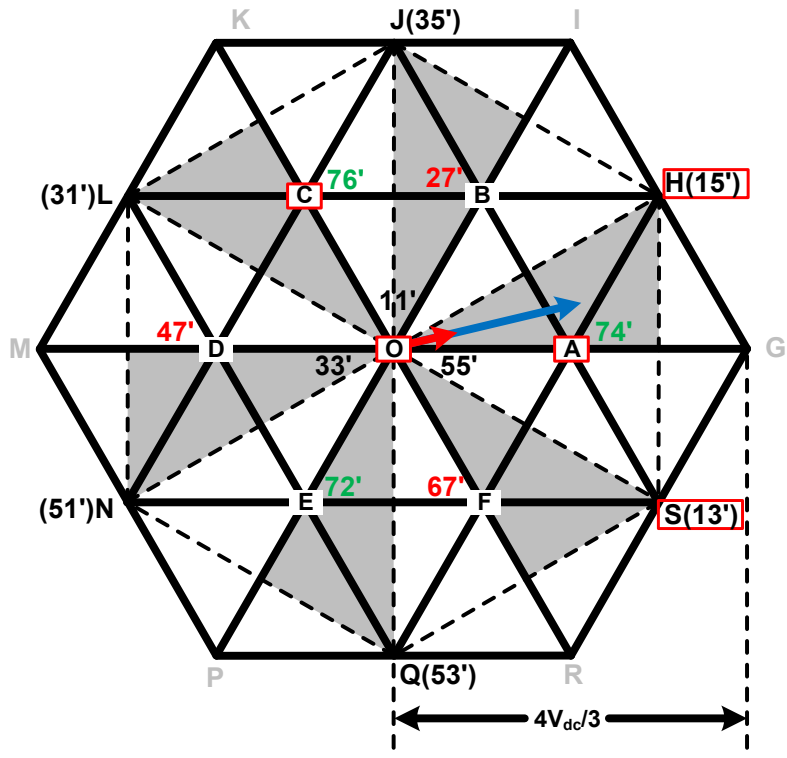


(a) Voltage vectors.

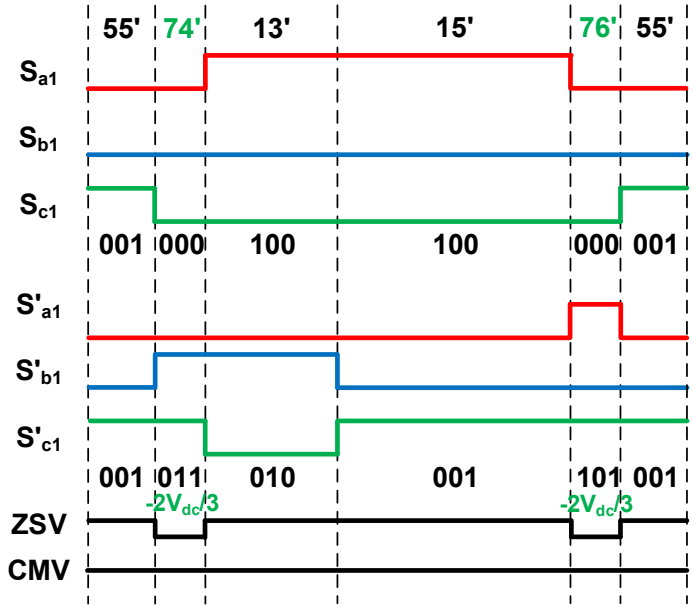


(b) PWM waveforms.

Fig. 6.7 Voltage vectors, switching combinations, and PWM waveforms in sector 2 with the proposed SVPWM strategy ( $V_o^* > 0$ ).



(a) Voltage vectors.



(b) PWM waveforms.

Fig. 6.8 Voltage vectors, switching combinations, and PWM waveforms in sector 2 with the proposed SVPWM strategy ( $V_0^* < 0$ ).

Four effective vectors and a zero vector are used in the proposed SVPWM. Two effective vectors ( $V_1, V_2$ ) are on the middle hexagon, which correspond to null ZSV switching

combinations. The other two effective vectors ( $\mathbf{V}_3, \mathbf{V}_4$ ) are on the small hexagon, which correspond to non-null ZSV switching combinations. To realize this PWM strategy, the durations of two non-null ZSV vectors ( $\mathbf{V}_3, \mathbf{V}_4$ )  $T_3$  and  $T_4$  need to be calculated firstly. The relationship between  $T_{nnZ}$  and the durations of two non-null ZSV vectors can be expressed as

$$T_{nnZ} = T_3 + T_4. \quad (6.5)$$

Assuming  $\mathbf{V}_3$  leads  $\mathbf{V}_4$ , Table 6.2 shows the angle  $\varphi$  between  $\mathbf{V}_3$  and  $\alpha$ -axis in different sectors. The angle between the reference voltage vector and the  $\alpha$ -axis is  $\gamma$ , so that the angle between the reference voltage vector and  $\mathbf{V}_3$  is  $\gamma - \varphi$ .  $T_3$  and  $T_4$  can be calculated as below

$$\begin{aligned} T_3 &= \frac{\sin(120 - \gamma + \varphi) T_{nnZ}}{\sin(\gamma - \varphi) + \sin(120 - \gamma + \varphi)} \\ T_4 &= \frac{\sin(\gamma - \varphi) T_{nnZ}}{\sin(\gamma - \varphi) + \sin(120 - \gamma + \varphi)}. \end{aligned} \quad (6.6)$$

Table 6.2 Angle Between  $\mathbf{V}_3$  and  $\alpha$  axis

Sector	$\varphi (V_0^* \geq 0)$	$\varphi (V_0^* < 0)$
1	$-\pi/3$	$-2\pi/3$
2		0
3	$-\pi/3$	0
4	$\pi/3$	
5	$\pi/3$	0
6		$2\pi/3$
7	$\pi/3$	$2\pi/3$
8	$\pi$	
9	$\pi$	$2\pi/3$
10		$-2\pi/3$
11	$\pi$	$-2\pi/3$
12	$-\pi/3$	

$\alpha$  and  $\beta$  axis components of the voltage vector that is synthesized by vectors  $\mathbf{V}_3$  and  $\mathbf{V}_4$  are

$$\begin{aligned} V_{mz\alpha} &= \frac{T_4 V_{dc} \cos\theta}{\sqrt{3} T_{PWM} \sin(\gamma-\varphi)} \\ V_{mz\beta} &= \frac{T_4 V_{dc} \sin\theta}{\sqrt{3} T_{PWM} \sin(\gamma-\varphi)} \end{aligned} \quad (6.7)$$

$\alpha$  and  $\beta$  axis components of the voltage vector that is synthesized by vectors  $\mathbf{V}_1$  and  $\mathbf{V}_2$  are

$$\begin{aligned} V_{nz\alpha} &= V_{\alpha}^* - V_{mz\alpha} \\ V_{nz\beta} &= V_{\beta}^* - V_{mz\beta} \end{aligned} \quad (6.8)$$

where  $V_{\alpha}^*$  and  $V_{\beta}^*$  are the  $\alpha$  and  $\beta$  axis reference voltages for dual inverters.

The durations  $T_1$  and  $T_2$  of two effective vectors ( $\mathbf{V}_1$ ,  $\mathbf{V}_2$ ) with null ZSV can be calculated by the SVPWM principle with  $\alpha$  and  $\beta$  axis reference voltages  $V_{nz\alpha}$  and  $V_{nz\beta}$ . As a result, durations of the four effective vectors as well as a zero vector can be acquired. With durations of four effective vectors  $\mathbf{V}_1$ ,  $\mathbf{V}_2$ ,  $\mathbf{V}_3$ , and  $\mathbf{V}_4$ , the duration of the zero vector can be calculated as  $T_0 = T_{PWM} - (T_1 + T_2 + T_3 + T_4)$ , so that durations of all basic vectors can be acquired. When  $T_{PWM} < (T_1 + T_2 + T_3 + T_4)$ , the OW drive enters the over modulation region. To maintain the controllability of ZSC,  $T_3$  and  $T_4$  should remain unchanged, and the modified durations  $T'_1$  and  $T'_2$  for the two basic vectors  $\mathbf{V}_1$  and  $\mathbf{V}_2$  with null ZSV can be expressed as

$$\begin{aligned} T'_1 &= \frac{T_1}{T_1 + T_2} (T_{PWM} - T_3 - T_4) \\ T'_2 &= \frac{T_2}{T_1 + T_2} (T_{PWM} - T_3 - T_4) \end{aligned} \quad (6.9)$$

From the PWM waveforms of the proposed SVPWM in Figs. 6.5-6.8, it can be seen that 5 legs of dual inverters are switched and a leg is clamped. On the other hand, the proposed SVPWM can cause extra switching commutations during the sector change due to the different initial switching combinations of different sectors. However, due to the large ratio between the carrier and electrical frequencies, the extra switching commutations are neglectable. For the PWM waveforms of the conventional CMVE-PWM in Fig. 6.1, all six legs are switched, so that the switching frequency can be reduced by 1/6 in the proposed SVPWM.

The control diagram of the proposed SVPWM strategy is shown in Fig. 6.9. The proposed SVPWM strategy uses the group of switching combinations whose CMV is  $V_{dc}/3$  for both the

CMV variation elimination and ZSC suppression, and the group of switching combinations with  $2V_{dc}/3$  CMV can also be used in the similar way.

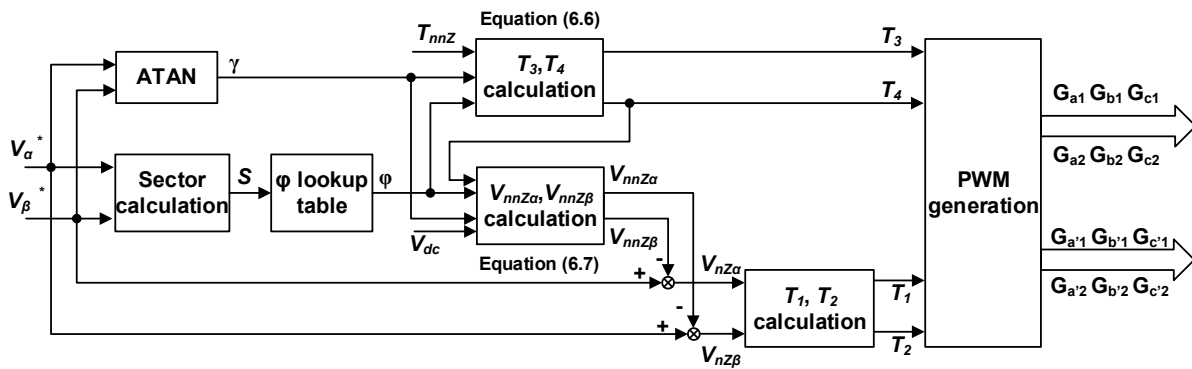


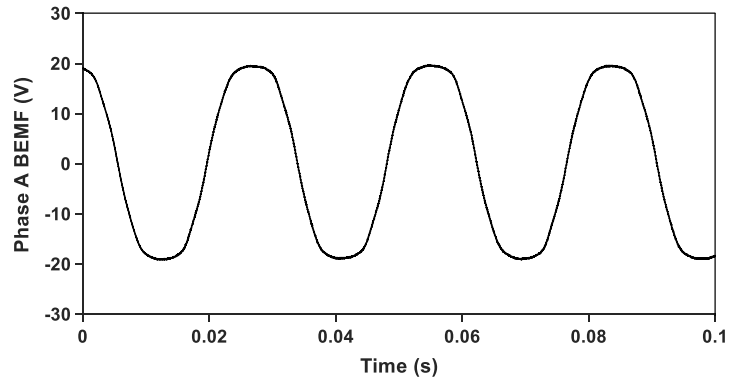
Fig. 6.9 Control diagram of the proposed SVPWM strategy.

## 6.4 Experiment Results

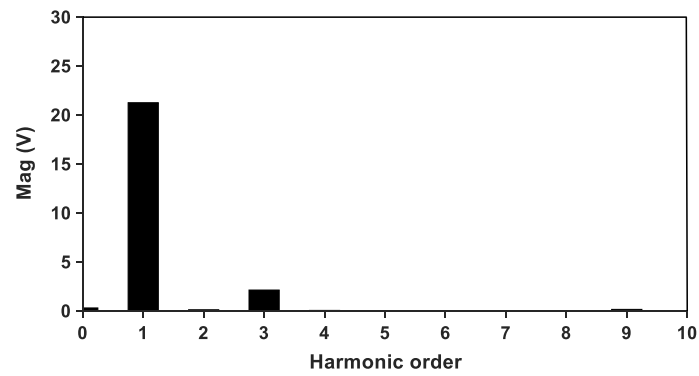
The experimental validation of the proposed SVPWM strategy is implemented for an OW-PMSM, and the parameters are listed in Table 6.3. Fig. 6.10 shows the phase BEMF waveform and spectrum of the prototype OW-PMSM at 420 rpm, and the percentage of the third harmonic is about 10%. The large component of the third BEMF harmonic can cause large ZSV, which should be counteracted by ZSV from PWM to suppress ZSC. The experimental platform of the OW-PMSM fed by dual inverters is based on a dSPACE in Fig. 6.11, and a wound field excited DC machine is used as the load machine. The DC-bus voltage is 30V. The interrupt frequency and the PWM frequency are 10kHz.

Table 6.3 Parameters of OW-PMSM

Resistance	0.9 $\Omega$
$d$ -axis inductances	5 mH
$q$ -axis inductances	5 mH
PM flux linkage	96.4 mWb
Pole pairs	5
Rated current	6 A
Rated torque	4.3 Nm



(a) Waveform.



(b) Spectrum.

Fig. 6.10 Measured phase BEMF waveform and spectrum of the prototype OW-PMSM, 420 rpm.

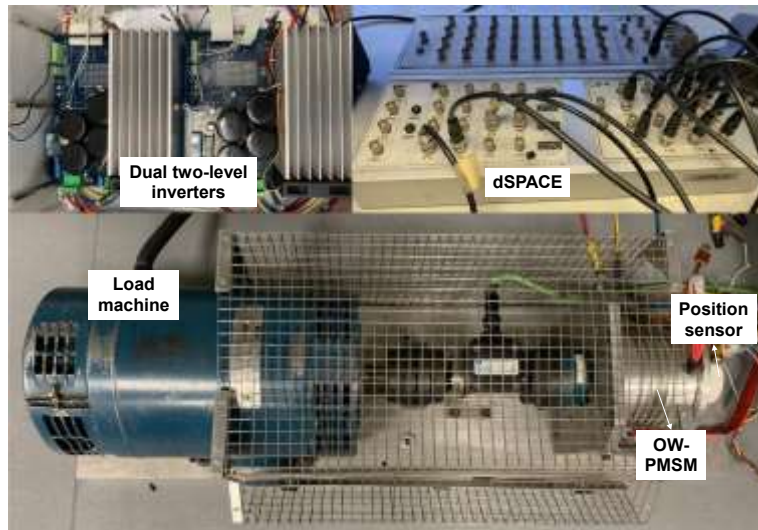


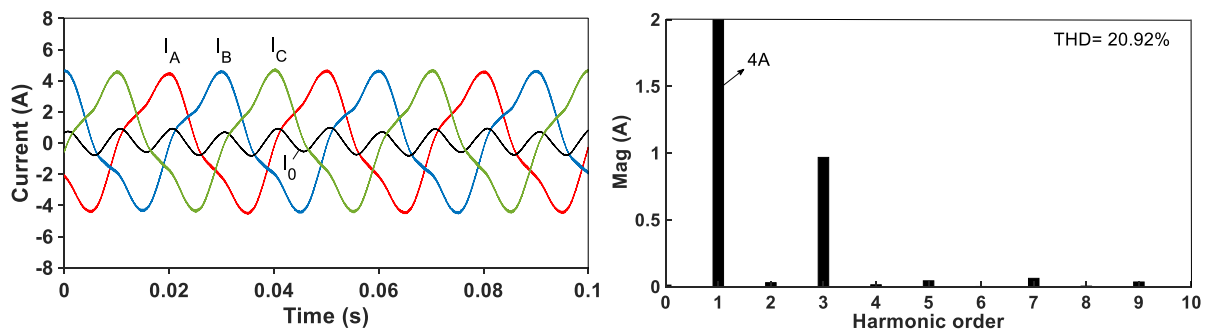
Fig. 6.11 Experiment platform.

The OW-PMSM is controlled in both the linear modulation region (Speed=400rpm, torque=2.9Nm) and over modulation region (Speed=600rpm, torque=2.9Nm) with the



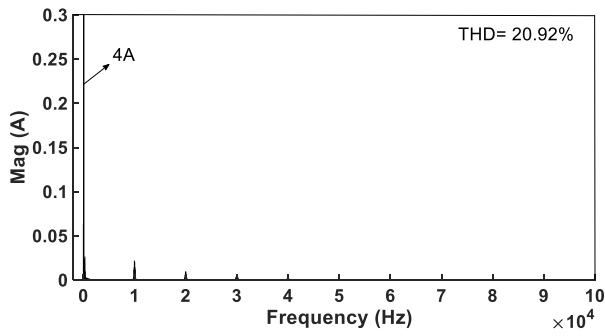
proposed SVPWM and conventional CMVE-PWM strategies. However, ZSC is out of control with the conventional CMVE-PWM strategy in the over modulation region as verified by following experiments. The CMV elimination and ZSC control performances of the proposed SVPWM and conventional CMVE-PWM strategies will be described and compared.

Fig. 6.12 shows the measured ZSC, three phase currents, spectrum of phase A current,  $dq$ -axis currents, and rotor speed of the proposed SVPWM without the ZSC close loop control. The OW-PMSM is controlled in the linear modulation region with the speed of 400rpm, and  $dq$ -axis currents are 0 and 4A, respectively. It can be seen that there is a large ZSC whose frequency is triple of electrical frequency in Figs. 6.12 (a) and (b). Figs. 6.12 (b) and (c) show phase A current spectra in low and high-frequency regions, respectively. A large third harmonic can be seen in Fig. 6.12 (b), but the high-frequency harmonics are relatively low in Fig. 6.12 (c). CMVs of Inverters I and II, ZSV, and CMV of the OW drive with the proposed SVPWM strategy without the ZSC control are shown in Fig. 6.13. Fig. 6.13 (b) is the magnified view of the highlighted region in Fig. 6.13 (a). CMV1 and CMV2 are CMVs of Inverters I and II, and they are maintained at a constant value  $V_{dc}/3$ . CMV of the OW drive is the average of CMV1 and CMV2, and is also maintained at the constant value  $V_{dc}/3$  in Fig. 6.13. ZSV of the OW drive is the difference between CMV1 and CMV2, and is maintained at the constant value 0. Although the PWM induced ZSV is 0, other ZSV sources can still generate ZSVs in the OW-PMSM drive. As a result, a large ZSC is generated without the ZSC close loop control.

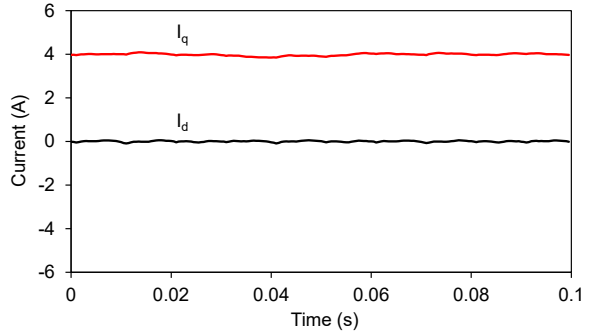


(a) Three phase currents and ZSC.

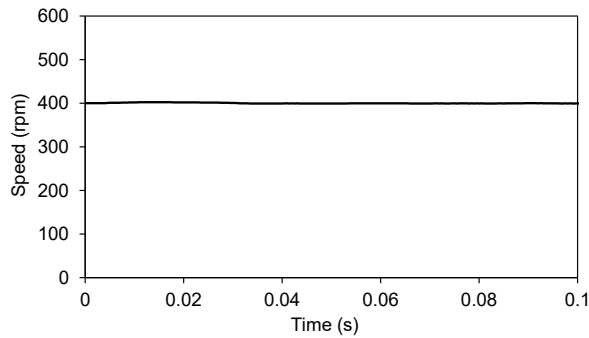
(b) Phase A current spectrum (low-frequency region).



(c) Phase A current spectrum (high-frequency region).

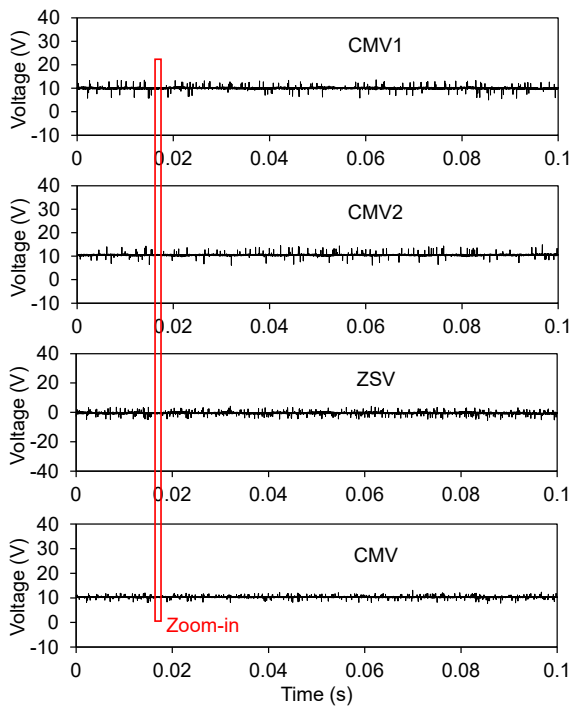


(d)  $Dq$ -axis currents.

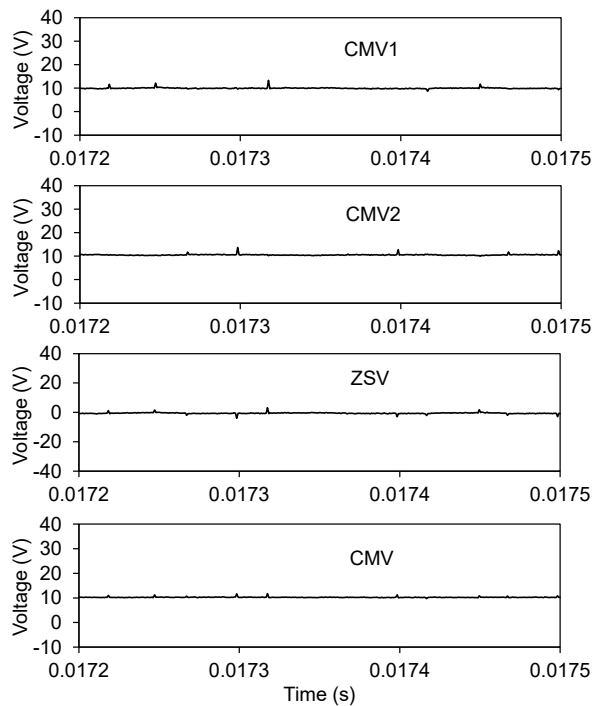


(e) Speed of OW-PMSM.

Fig. 6.12 ZSC, three phase currents, phase A current spectrum,  $dq$ -axis currents, and speed of the proposed SVPWM strategy without ZSC control.



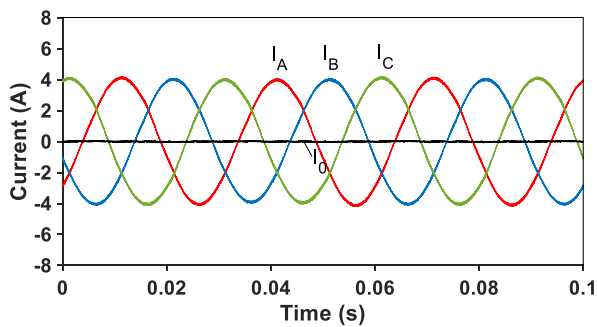
(a) CMVs and ZSVs.



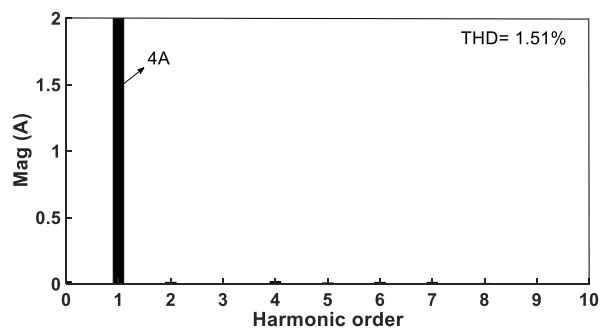
(b) CMVs and ZSVs in the Zoom-in region.

Fig. 6.13 CMVs and ZSVs of the proposed SVPWM strategy without ZSC control.

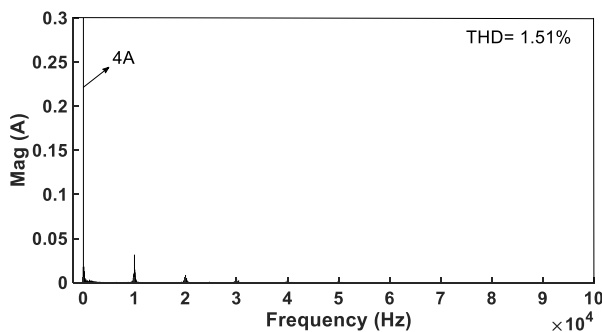
Fig. 6.14 shows the control performance of the proposed SVPWM strategy in the linear modulation region (Speed=400 rpm, torque=2.9Nm) with the ZSC close loop control. ZSC can be controlled to zero in Fig. 6.14 (a), and the third harmonic is eliminated in Fig. 6.14 (b). Compared with Fig. 6.13, the phase current THD is reduced from 20.92% to 1.51%. CMVs of Inverters I and II, ZSV, and CMV of the OW drive in the proposed SVPWM strategy are shown in Fig. 6.15. CMV is kept on a constant value of  $V_{dc}/3$ , as all the switching combinations have the same CMV, i.e.  $V_{dc}/3$ , in the proposed SVPWM strategy. Consequently, the proposed SVPWM strategy can eliminate CMV variation and control ZSC simultaneously. In dual inverters, ZSV can be generated by PWM, the triplen BEMF harmonics, inverter nonlinearity, and zero sequence component of coupling voltages, among which only PWM can generate a controllable ZSV. In the proposed SVPWM strategy, ZSC can be suppressed to zero, which indicates that the whole ZSV is controlled to zero, so that PWM in dual inverters can generate a controllable ZSV to counteract with ZSVs caused by other sources. Due to the main component of other ZSV sources is the third BEMF harmonic, the frequency of ZSV from PWM in Fig. 6.15 (a) is also triple of the electrical frequency.



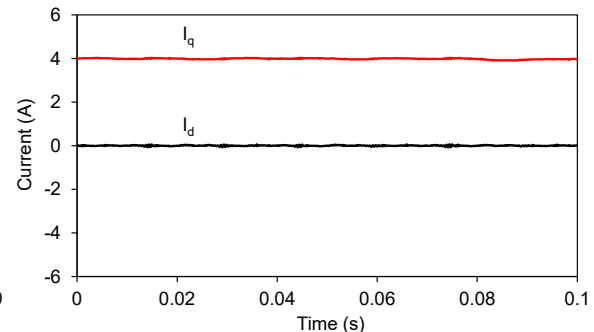
(a) Three phase currents and ZSC.



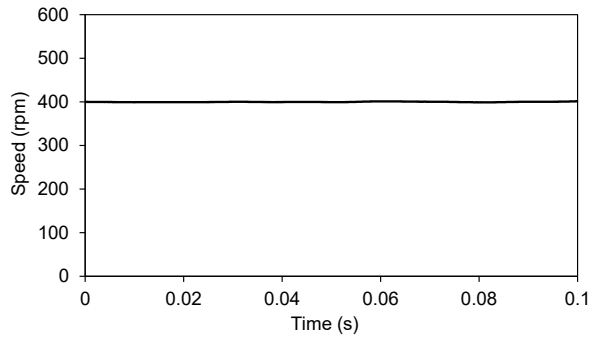
(b) Phase A current spectrum (low-frequency region).



(c) Phase A current spectrum (high-frequency region).

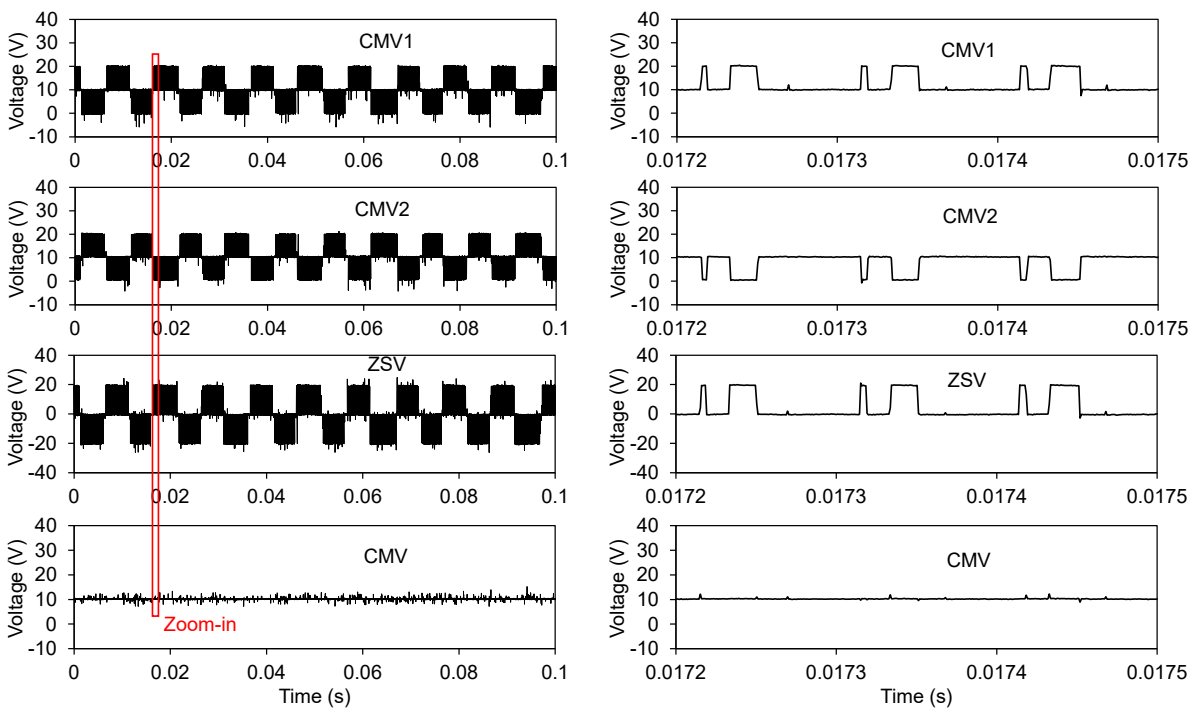


(d)  $Dq$ -axis currents.



(e) Speed of OW-PMSM.

Fig. 6.14 ZSC, three phase currents, phase A current spectrum,  $dq$ -axis currents, and speed of the proposed SVPWM strategy with ZSC control.



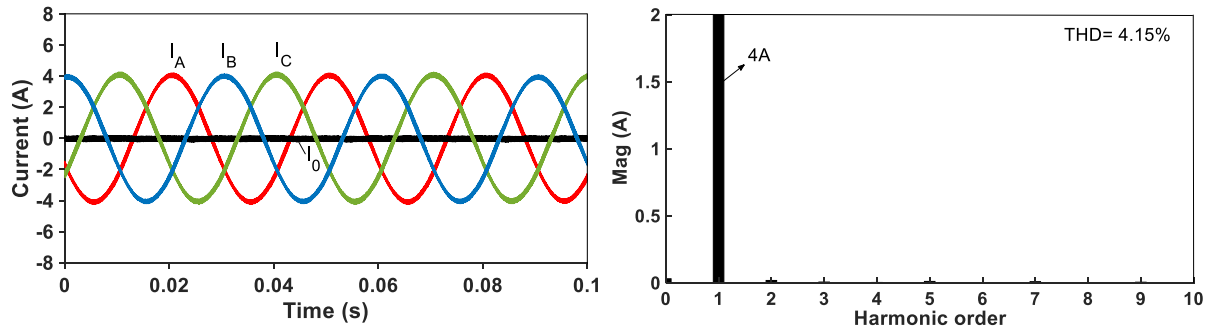
(a) CMVs and ZSVs.

(b) CMVs and ZSVs in the Zoom-in region.

Fig. 6.15 CMVs and ZSVs of the proposed SVPWM strategy with ZSC control.

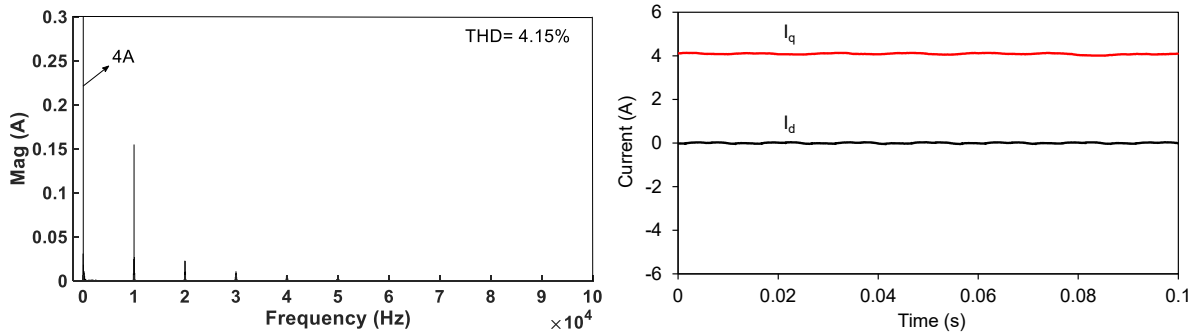
Fig. 6.16 shows the control performance of the conventional CMVE-PWM strategy in the linear modulation region (Speed=400rpm, torque=2.9Nm) with the ZSC close loop control. Although low-frequency ZSC can be suppressed as shown in Fig. 6.16 (b), high-frequency ZSC harmonics in Fig. 6.16 (c) are much larger compared with these of the proposed SVPWM in Fig. 6.14 (c). The larger high-frequency ZSC harmonics of the conventional CMVE-PWM can also be visible when comparing ZSC and three phase currents in Fig. 6.14 (a) and Fig. 6.16 (a). CMVs of Inverters I and II, ZSV, and CMV of the OW drive in the conventional CMVE-PWM strategy are shown in Fig. 6.17. Although there is a large variation of CMVs in Inverters I and

II, they have the opposite phase, and their average value, i.e. CMV of the OW drive, can be maintained at a constant value  $V_{dc}/2$ . However, there is a large variation of ZSV from  $-V_{dc}$  to  $V_{dc}$  with the conventional CMVE-PWM strategy in Fig. 6.17 (b), which is the reason of large high-frequency ZSC harmonics. Bearing in mind that the switching frequency for the proposed SVPWM is  $5/6$  of that for the conventional CMVE-PWM strategy. As a result, the proposed SVPWM can reduce both the switching frequency and high-frequency ZSC harmonics, and the THD of phase current can be reduced from 4.15% to 1.51%.



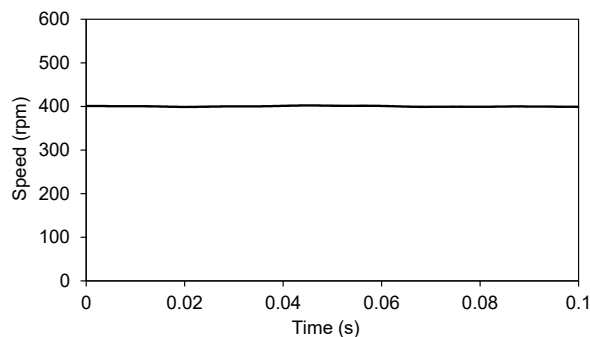
(a) Three phase currents and ZSC.

(b) Phase A current spectrum (low-frequency region).



(c) Phase A current spectrum (high-frequency region).

(d)  $Dq$ -axis currents.



(e) Speed of OW-PMSM.

Fig. 6.16 ZSC, three phase currents, phase A current spectrum,  $dq$ -axis currents, and speed of the CMVE-PWM strategy in [HU21].

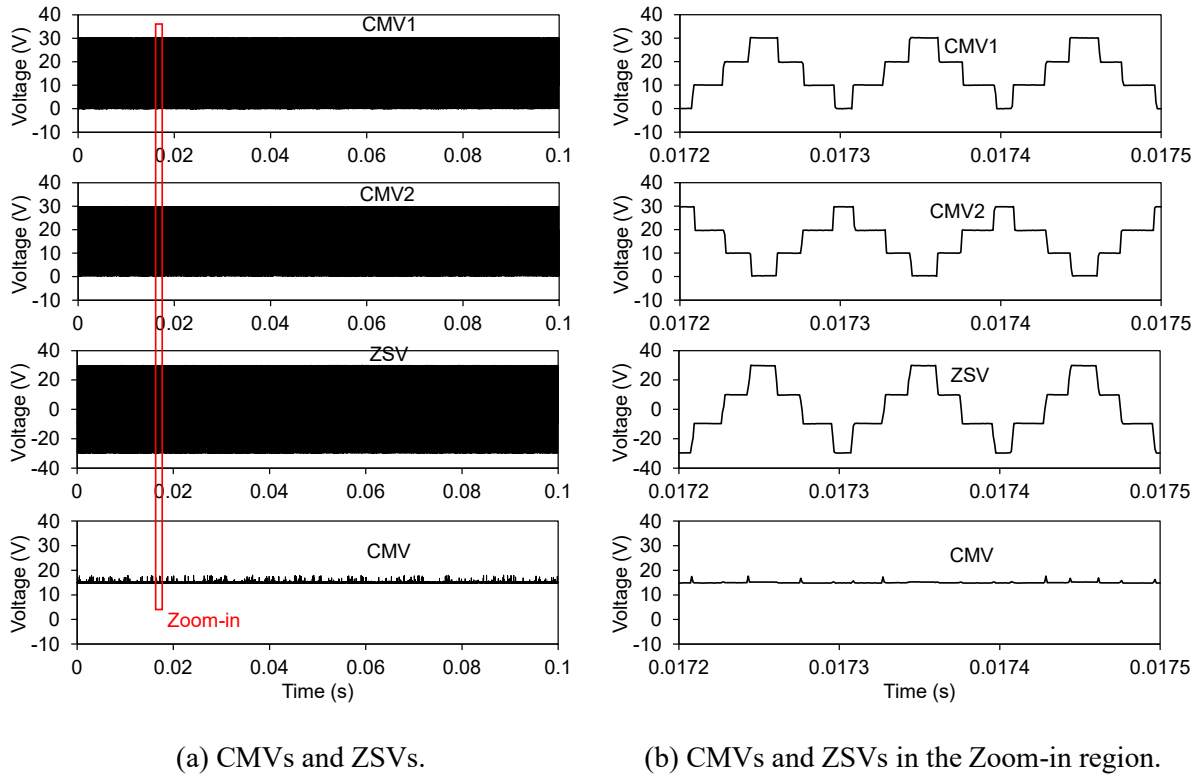
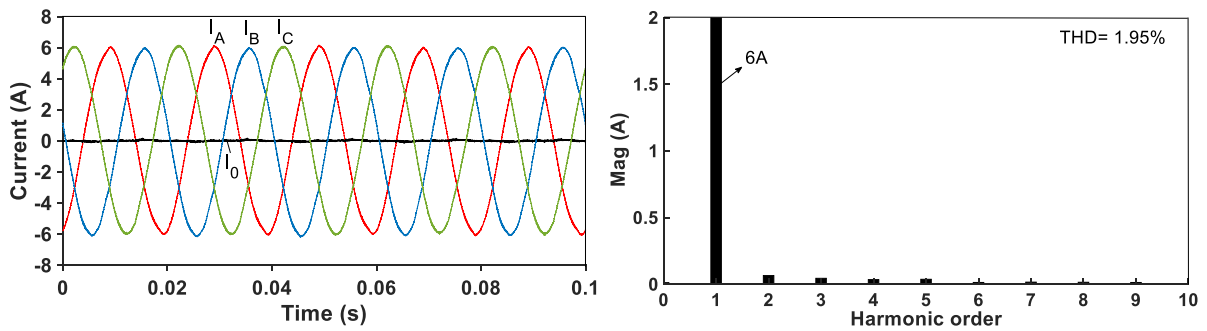


Fig. 6.17 CMVs and ZSVs of the conventional CMVE-PWM strategy in [HU21].

Figs. 6.18 and 6.19 compare the control performance of the proposed SVPWM and conventional CMVE-PWM strategies in the over modulation region with the speed of 600rpm and torque of 2.9Nm. The conventional CMVE-PWM strategy cannot achieve ZSC control in the over modulation region, and large low/high-frequency ZSC harmonics can be seen from Figs. 6.19 (b) and (c). On the contrast, the proposed SVPWM can achieve the ZSC control in the over modulation region, and ZSC can be suppressed in both low and high frequencies as shown in Figs. 6.18 (b) and (c), and the THD of phase current can be reduced from 18.02% to 1.95%.  $Dq$ -axis currents are -4.3A and 4A respectively, and the conventional CMVE-PWM strategy has large  $dq$ -axis current ripples due to the uncontrollable ZSC. Overall, compared with the conventional CMVE-PWM strategy, the proposed SVPWM strategy has the advantage of low switching frequency, low ZSC harmonics, and controlled ZSC in the over modulation region.

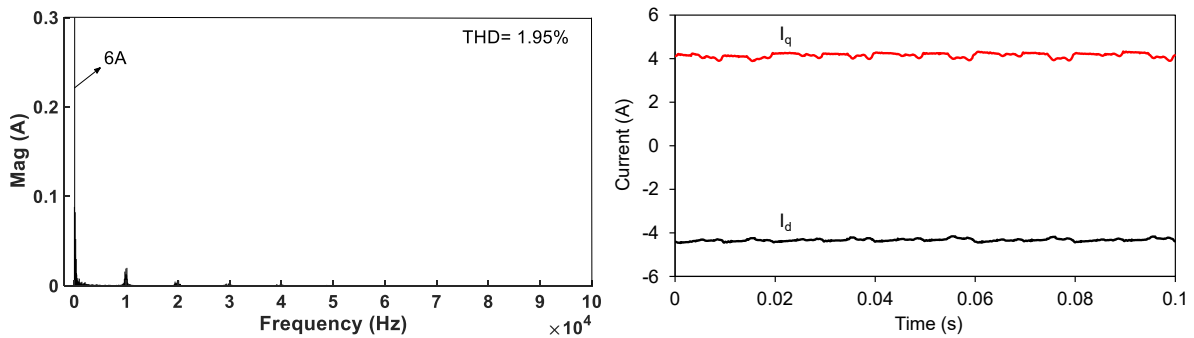
To evaluate the dynamic performance of the proposed SVPWM strategy, close loop controllers are designed with current inner loop and speed outer loop. The output of current controller is the reference voltages for the proposed SVPWM strategy. Fig. 6.20 shows the transient phase A current,  $dq$ -axis currents, reference and measured speeds with a speed step from 200 to 400

rpm. Fig. 6.21 shows the transient phase A current,  $dq$ -axis currents, reference and measured speeds under a load step from no-load to 2.9Nm.



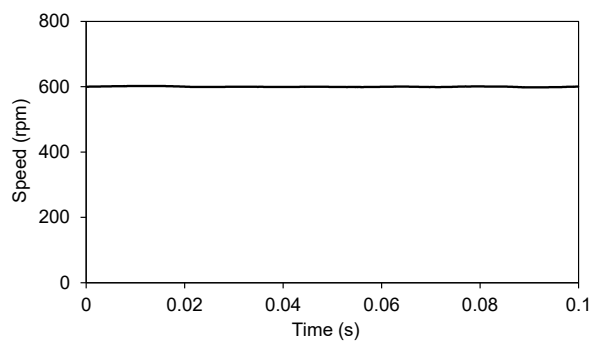
(a) Three phase currents and ZSC.

(b) Phase A current spectrum (low-frequency region).



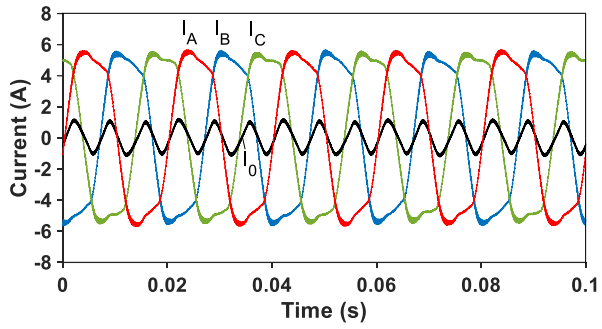
(c) Phase A current spectrum (high-frequency region).

(d)  $Dq$ -axis currents.

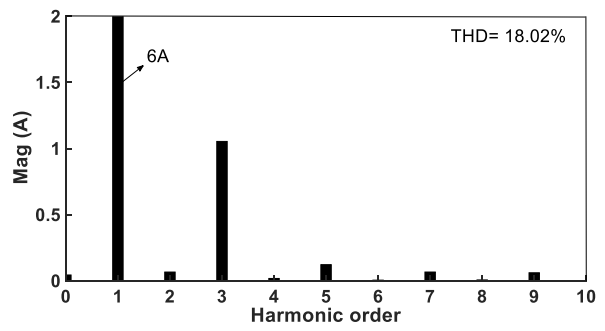


(e) Speed of OW-PMSM.

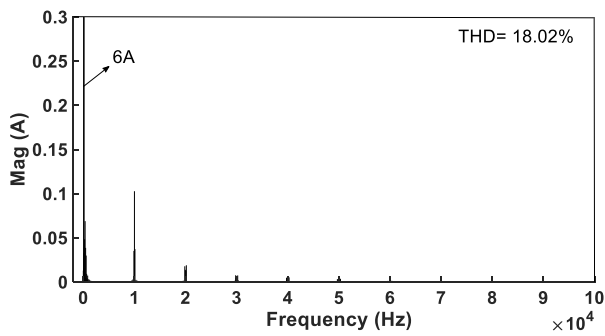
Fig. 6.18 ZSC, three phase currents, phase A current spectrum,  $dq$ -axis currents, and speed of the proposed SVPWM strategy in over modulation region with ZSC control.



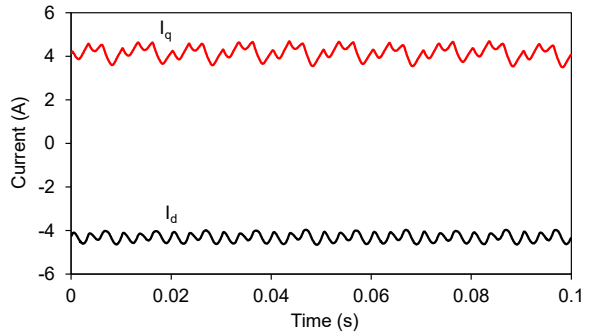
(a) Three phase currents and ZSC.



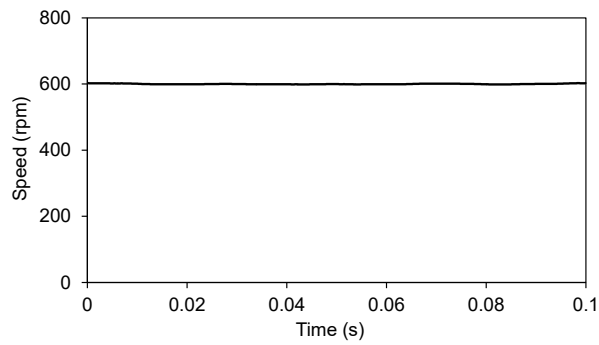
(b) Phase A current spectrum (low-frequency region).



(c) Phase A current spectrum (high-frequency region).



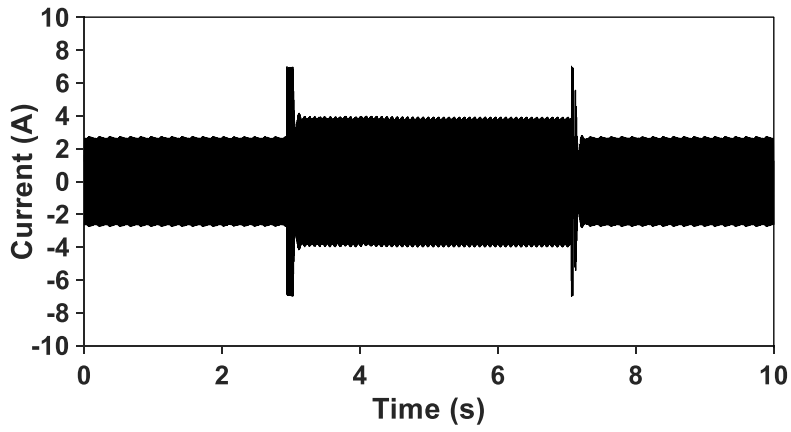
(d)  $Dq$ -axis currents.



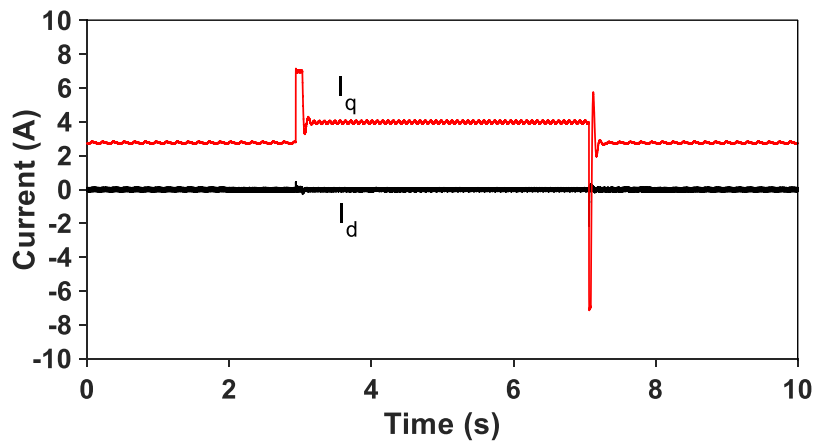
(e) Speed of OW-PMSM.

Fig. 6.19 ZSC, three phase currents, phase A current spectrum,  $dq$ -axis currents, and speed of the CMVE-PWM strategy in [HU21] in over modulation region.

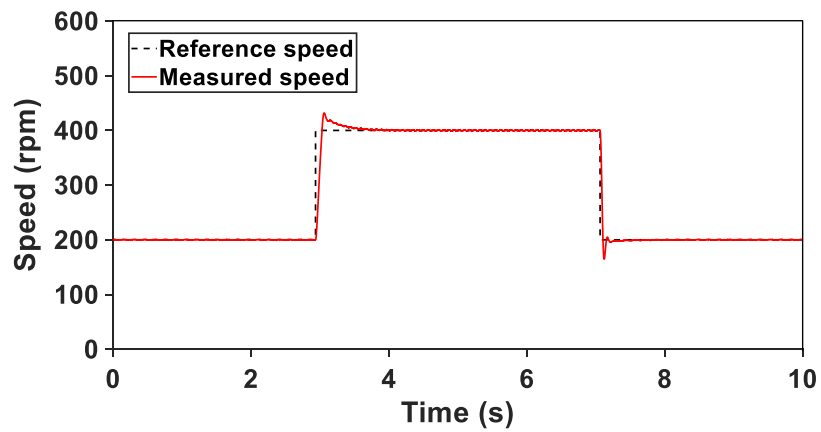




(a) Phase A current.

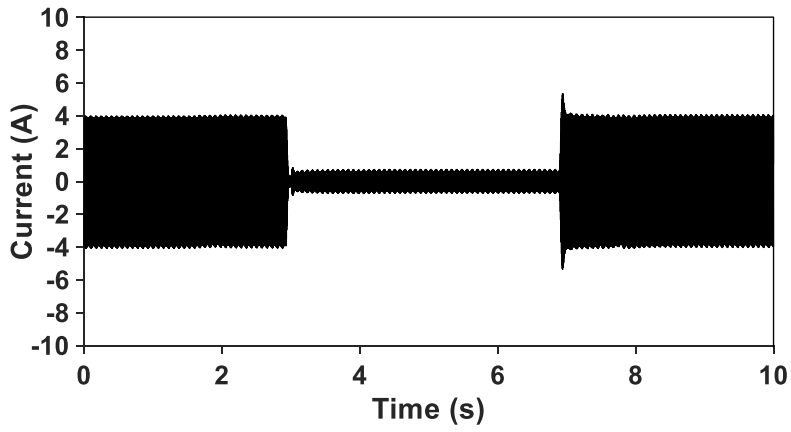


(b)  $Dq$ -axis currents.

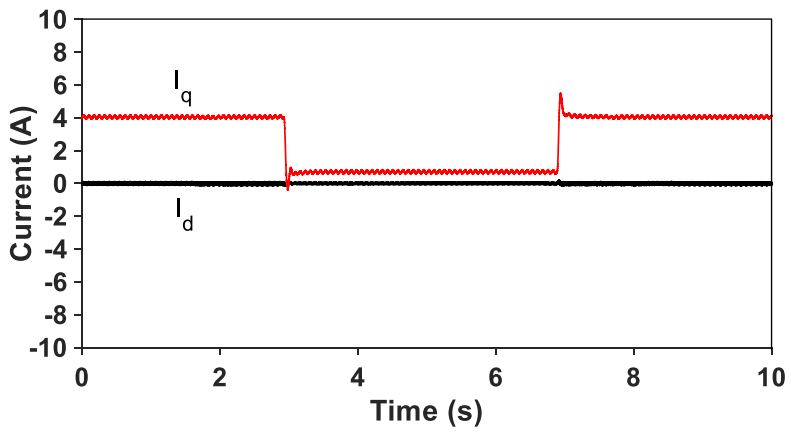


(c) Reference and measured speed.

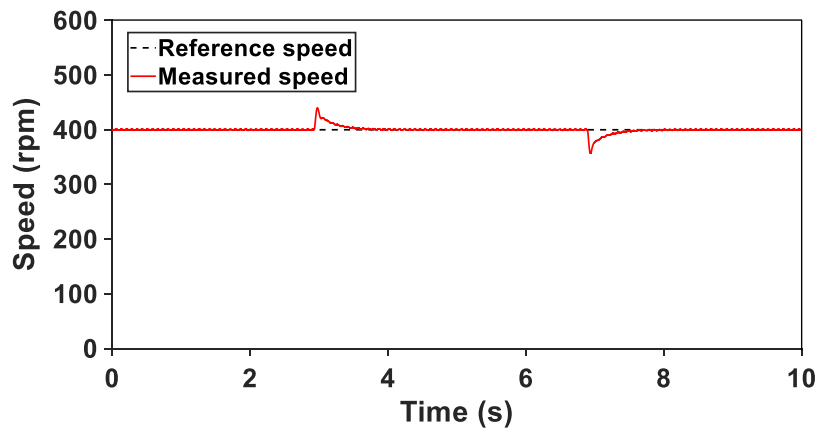
Fig. 6.20 Control performance of speed step from 200 rpm to 400 rpm.



(a) Phase A current.



(b) *Dq*-axis currents.



(c) Reference and measured speed.

Fig. 6.21 Control performance of torque step from no-load to 2.9 Nm.

## 6.5 Summary

This Chapter has proposed an SVPWM strategy for an OW-PMSM fed by dual two-level inverters with a common DC-bus to eliminate CMV variation and suppress low/high-frequency ZSC simultaneously by the optimal selection of switching combinations. Switching combinations in the dual inverters are categorized into groups according to their CMVs, and the group with  $V_{dc}/3$  CMV is used to design the proposed SVPWM strategy for CMV variation elimination as well as the control of ZSC. The proposed SVPWM can minimize the effect of the CMV control on the ZSC control, as the CMV control can limit the utilizing of switching combinations and may induce large high-frequency ZSC harmonics. Compared with the conventional CMVE-PWM, the proposed SVPWM can reduce the switching frequency by 1/6, and significantly reduce high-frequency ZSC harmonics. Moreover, the proposed SVPWM can solve the problem of uncontrolled ZSC with the conventional CMVE-PWM in the over modulation region, and current harmonics can be reduced in both low- and high-frequencies. Experiment results validate the performance of the CMV variation elimination and ZSC suppression in the proposed SVPWM strategy. In the next chapter, the effects of the ZSC control on the modulation region will be studied, and a novel SVPWM is proposed utilizing the switching combinations with non-null ZSV on the large hexagon for ZSC control to increase the operation range of the OW machine.

# CHAPTER 7 A NOVEL SVPWM FOR OPEN WINDING PMSM WITH EXTENDED OPERATION RANGE

In Chapters 5 and 6, PWM strategies of common DC-bus dual two-level inverters are investigated for the current harmonic reduction and CMV variation elimination, and they have the commonality of ZSC control. In this chapter, the effects of ZSC control on the modulation region will be investigated. A novel SVPWM with ZSC control strategy is proposed to extend the operation range for an OW-PMSM in this chapter. The proposed SVPWM can achieve the ZSC control and extend the operation range by considering voltages in zero sequence axis and voltage vectors in  $\alpha\beta$ -plane, both of which are mapped by switching combinations in an OW drive. The effect of switching combinations with non-null ZSV on the modulation region of a common-DC bus OW-PMSM is investigated for the first time. The proposed SVPWM has the optimal selection of switching combinations on the large hexagon rather than on the small hexagon in the conventional SVPWM for ZSC control, and still maintains the controllability of ZSC in the over modulation region. Compared with the conventional SVPWM strategy, the operation range of the OW-PMSM can be extended over 10% with the proposed SVPWM strategy. The performances of the conventional and the proposed SVPWMs are compared experimentally.

This chapter is based on the paper published in:

L. Xu and Z. Q. Zhu, "A novel SVPWM for open winding permanent magnet synchronous machine with extended operation range," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2022, doi: 10.1109/JESTPE.2022.3200346.

## 7.1 Introduction

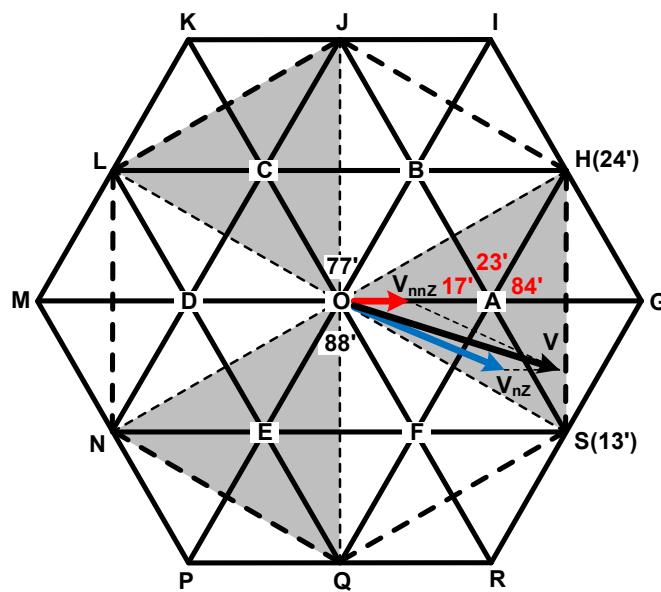
ZSC is caused by ZSV in an OW-PMSM fed by common DC-bus DTL-VSIs, and should be controlled due to the negative effects, and many ZSC control strategies have been proposed [BAI04] [AN16] [LIN19] [HU19]. The effect of ZSV on the linear modulation region is analysed in [HU19]. However, [HU19] only gives the maximum linear modulation range for ZSV. These methods cannot maintain the ability of the ZSC control in the over modulation region. An SVPWM strategy is proposed in [ZHA17a], and a controllable ZSV can be generated by PWM with zero vector redistributions to control ZSC. Moreover, the over modulation operation can be achieved. The effect of switching combinations with non-null ZSV on the modulation region of a common-DC bus OW-PMSM is investigated for the first time in this chapter. It was found in [ZHA17a] that the basic voltage vectors in  $\alpha\beta$ -plane mapped by switching combinations with non-null ZSV have a small magnitude. Consequently, the maximum modulation region is reduced.

The contributions of this chapter are that the ZSC control and the extended operation range can be achieved in the proposed SVPWM by considering voltages in zero sequence axis and voltage vectors in  $\alpha\beta$ -plane, both of which are mapped by switching combinations in an OW drive. By exclusively utilizing the optimal switching combinations on the large hexagon for the ZSC control, the corresponding basic voltage vectors in  $\alpha\beta$ -plane have the maximum magnitude, so that the modulation region of DTL-VSIs can be enlarged. A ZSC closed-loop is designed to control the durations of the basic vectors with non-null ZSV on the large hexagon, which will be used together with the other two basic vectors with null ZSV on the middle hexagon to synthesize the reference voltage vector. The control of ZSC can be achieved in both linear and over modulation regions in this chapter and the operation range of the OW-PMSM can be extended compared with the conventional SVPWM in [ZHA17a], as extensively verified by experiments.

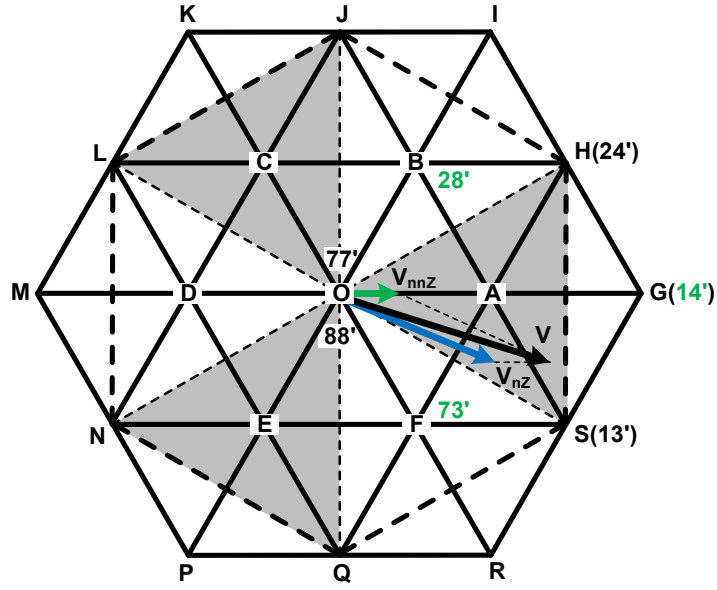
## 7.2 Modulation Region in Conventional SVPWM Strategy

The conventional SVPWM has been described in detail in Section 5.2.1. From (5.7), ZSV from PWM is proportional to  $T_r$  in the conventional SVPWM, and is controlled to the desired value by the ZSC closed-loop. As a result, ZSC can be suppressed since ZSVs from other sources can be counteracted by the controllable ZSV from PWM. It can be seen from Figs. 5.7 (a) and (b), there are three types of switching combinations with null, positive, and negative ZSVs.

When the reference ZSV is positive, switching combinations with null and positive ZSVs are used, while switching combinations with null and negative ZSVs are used when the reference ZSV is negative. The locations of these null and non-null ZSV switching combinations are shown in Figs. 7.1 (a) and (b) with positive and negative  $T_r$ , respectively. The null ZSV switching combinations are the same for both positive and negative  $T_r$ , but the locations of non-null ZSV switching combinations are different. When  $T_r$  is positive, three positive ZSV switching combinations are all located at A point in the space vector plane of DTL-VSIs. However, when  $T_r$  is negative, three negative ZSV switching combinations are located at B, F, and G, respectively. All basic vectors with non-null ZSV have the same duration  $|4T_r|$  in Fig. 5.7, so that the vector  $\overrightarrow{OV_{nnZ}}$  synthesized by all basic vectors with non-null ZSV has the same magnitude for positive and negative  $T_r$ . Consequently, the resultant magnitude of these basic vectors with non-null ZSV is  $2V_{dc}/3$ , which is the same as the magnitude of basic vectors on the small hexagon. Due to the small resultant magnitude of basic vectors with non-null ZSV, the maximum modulation region will be reduced.



(a) Positive  $T_r$ .



(b) Negative  $T_r$ .

Fig. 7.1 Switching combinations and voltage vectors in sector 1.

The vector  $\overrightarrow{OV_{nZ}}$  in Fig. 7.1 is synthesized by basic vectors 13' and 24' with null ZSV, and the synthesis of  $\overrightarrow{OV_{nZZ}}$  and  $\overrightarrow{OV_{nZ}}$  is the vector  $\overrightarrow{OV}$ , which is the final output voltage vector. It needs to note that the redistribution of zero vectors can change ZSV in DTL-VSIs, but  $\alpha\beta$ -axis voltages keep unchanged. However, a minimum duration  $|2T_r|$  for both zero vectors 77' and 88' is needed for the redistribution. Due to the same duration for two zero vectors 77' and 88' in the conventional SVPWM, the duration of zero vectors before redistribution can be expressed as

$$T_{77'} = T_{88'} \geq |2T_r|. \quad (7.1)$$

The duration of effective vectors 13' and 24' before the redistribution in sector 1 can be expressed as

$$T_{13'} + T_{24'} \leq T_{PWM} - |4T_r|. \quad (7.2)$$

Due to the reserved duration for zero vectors, the maximum magnitude of output voltage vector will be reduced. Assuming the angle of the  $\overrightarrow{OV}$  is  $\varphi$  with respect to  $\overrightarrow{OA}$  in sector 1, magnitude of  $\overrightarrow{OV}$  can be expressed as

$$|\overrightarrow{OV}| \leq \frac{V_{dc}}{\cos \varphi} \frac{T_{PWM} - |4T_r|}{T_{PWM}}. \quad (7.3)$$

According to (5.7), (7.3) can be rewritten as

$$|\overline{OV}| \leq \frac{V_{dc}}{\cos \varphi} - \frac{|V_o^*|}{\cos \varphi}. \quad (7.4)$$

$\varphi$  varies between  $-\pi/6$  to  $\pi/6$  radians, and can be expressed as

$$\varphi = \begin{cases} \gamma & -\frac{\pi}{6} \leq \gamma < \frac{\pi}{6} \\ \gamma - \frac{\pi}{3} & \frac{\pi}{6} \leq \gamma < \frac{\pi}{2} \\ \gamma - \frac{2\pi}{3} & \frac{\pi}{2} \leq \gamma < \frac{5\pi}{6} \\ \gamma - \pi & \frac{5\pi}{6} \leq \gamma < \frac{7\pi}{6} \\ \gamma - \frac{4\pi}{3} & \frac{7\pi}{6} \leq \gamma < \frac{3\pi}{2} \\ \gamma - \frac{5\pi}{3} & \frac{3\pi}{2} \leq \gamma < \frac{11\pi}{6} \end{cases} \quad (7.5)$$

where  $\gamma$  is the angle between the reference voltage vector  $\overline{OV}$  and  $\alpha$ -axis.

For the other sectors, similar results can be acquired as (7.4). If the magnitude of  $\overline{OV}$  is  $V_{dc}/\cos\varphi$ , the vector can reach the boundary of the middle hexagon. However, the maximum magnitude will be reduced by  $|V_o^*|/\cos\varphi$  due to the redistribution of zero vectors for the ZSC control. Due to the use of non-null ZSV switching combinations for the ZSC control in the conventional SVPWM, the maximum output voltage will be reduced, and the modulation region will be smaller than the middle hexagon.

### 7.3 Proposed SVPWM Strategy

The reduction of the modulation region of an OW-PMSM in the conventional SVPWM strategy can be overcome by the optimal selection of non-null ZSV switching combinations. In this chapter, only the non-null ZSV switching combinations on the large hexagon are used for the ZSC control in an OW-PMSM drive, and thus, the modulation region can be enlarged compared with the conventional SVPWM. Different from six sectors in the conventional SVPWM strategy, the space vector plane of DTL-VSIs in Fig. 7.2 is divided into 12 sectors in the proposed SVPWM strategy. Fig. 7.3 shows the control diagram of the OW drive with the proposed SVPWM strategy including the ZSC closed-loop control. The ZSC control will be realized under the restriction of using the non-null ZSV switching combinations on the large hexagon in the proposed SVPWM strategy.



To control ZSC, a ZSC closed-loop is set in Fig. 7.3. The input of the PR controller is the error between the reference and feedback of ZSC, and the output is the reference ZSV  $V_0^*$ . The ZSC reference is set to zero to suppress ZSC in Fig. 7.3. Utilizing positive, negative, and null ZSV switching combinations, the ZSV from PWM can equal the reference ZSV to control the whole ZSV to zero. At the same time, PWM of DTL-VSIs can generate  $\alpha\beta$ -axis voltages according to the reference voltages. Basic vectors with null ZSV are always used, corresponding to the zero vector at O point, and effective vectors on the middle hexagon. For the selected switching combinations with non-null ZSVs on the large hexagon, their ZSVs should have the same sign as the reference ZSV. Moreover, the total duration  $T_{nz}$  for the switching combinations with non-null ZSV can be calculated according to the magnitude of the reference ZSV.

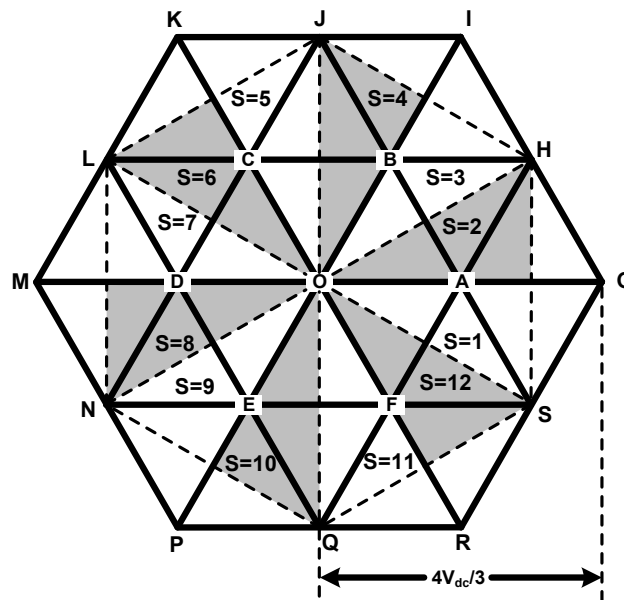


Fig. 7.2 Sectors of the proposed PWM strategy.

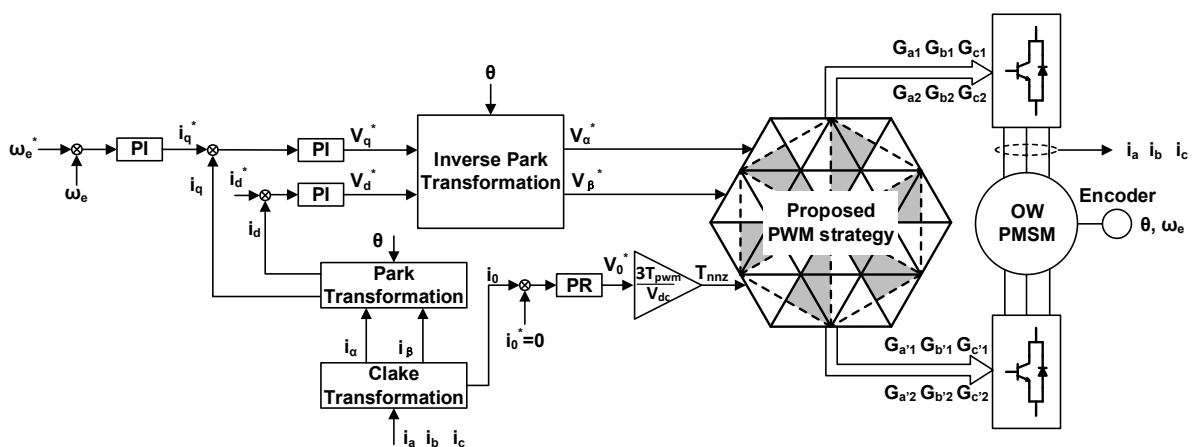


Fig. 7.3 Control diagram of the OW drive with the proposed PWM strategy.

Fig. 7.4 (a) shows the decomposition of the reference voltage vector, the selection of switching combinations and PWM waveforms in sector 1 with the proposed PWM strategy, when the reference ZSV is positive. The reference voltage vector  $\overrightarrow{OV}$  in Fig. 7.4 (a) is decomposed into two vectors with the same direction, i.e.  $\overrightarrow{OV_{nZ}}$  and  $\overrightarrow{OV_{nnZ}}$ .  $\overrightarrow{OV_{nZ}}$  is synthesized by two basic vectors on the middle hexagon, i.e. 13' and 15', and the corresponding switching combinations have null ZSV.  $\overrightarrow{OV_{nnZ}}$  is synthesized by two basic vectors on the large hexagon, i.e. 63' and 25', and the corresponding switching combinations have a ZSV of  $V_{dc}/3$ . With the positive ZSV, negative ZSVs caused by other sources can be counteracted to achieve the ZSC suppression. The PWM waveforms and ZSV in a PWM cycle in sector 1 with the proposed SVPWM strategy are also shown in Fig. 7.4 (a), when the reference ZSV is positive. It can be seen that there are two positive pulses of ZSV with the magnitude of  $V_{dc}/3$ . The total duration of two switching combinations 63' and 25' with non-null ZSV is  $T_{nnZ}$ , i.e.  $T_{nnZ} = T_{63'} + T_{25'}$ . To generate the reference ZSV  $V_0^*$ , The total duration  $T_{nnZ}$  of two non-null ZSV switching combinations can be expressed as

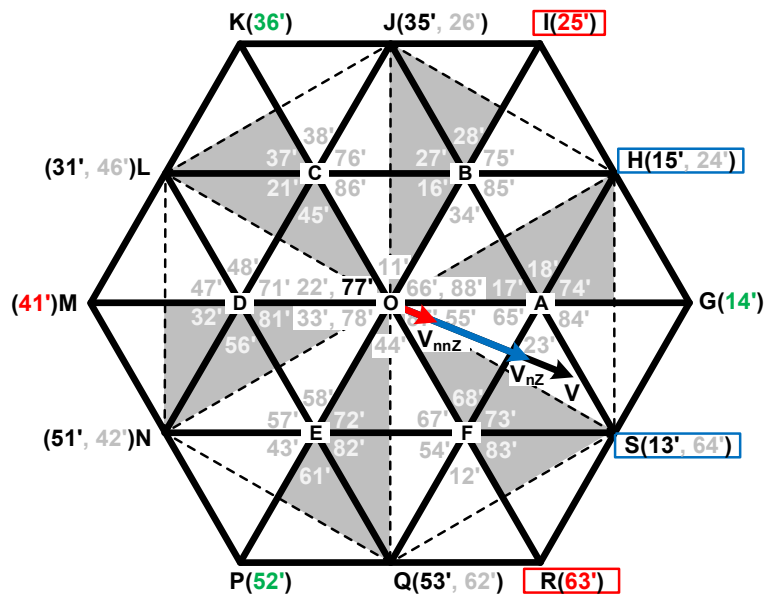
$$T_{nnZ} = \frac{3T_{PWM} |V_0^*|}{V_{dc}}. \quad (7.6)$$

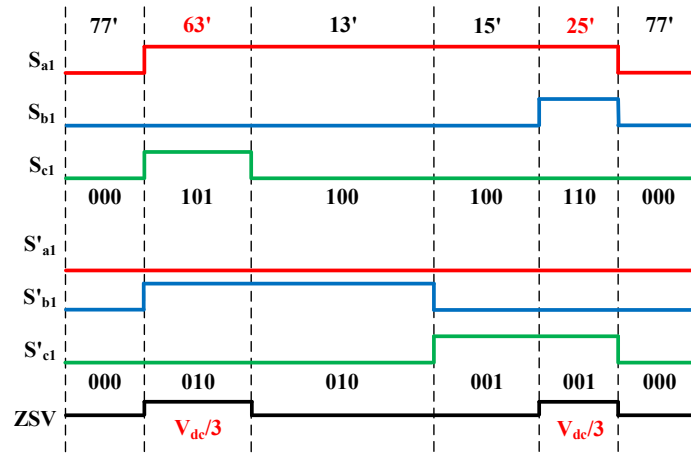
In sector I, two non-null ZSV switching combinations 63' and 25' can generate positive ZSV according to the reference ZSV  $V_0^*$ , with the control of the duration  $T_{nnZ}$ .

Fig. 7.4 (b) shows the reference voltage vector, switching combinations, and PWM waveforms in sector 1 with the proposed PWM strategy, when the reference ZSV is negative. The reference voltage vector  $\overrightarrow{OV}$  can also be decomposed into two components with the same direction, i.e.  $\overrightarrow{OV_{nZ}}$  and  $\overrightarrow{OV_{nnZ}}$ . Similar with the positive reference ZSV,  $\overrightarrow{OV_{nZ}}$  is synthesized by two basic vectors with null ZSV on the middle hexagon, i.e. 13' and 15'. However, different switching combinations are used for the vector  $\overrightarrow{OV_{nnZ}}$ , which is synthesized by two basic vectors with negative ZSV on the large hexagon, i.e. 52' and 14'. With the negative ZSV from PWM, positive ZSVs from other sources can be counteracted to achieve the ZSC suppression. From ZSV in Fig. 7.4 (b), it can be seen that two negative pulses with the magnitude of  $-V_{dc}/3$  appear. The total duration of two negative ZSV switching combinations 52' and 14' is  $T_{nnZ}$ , which can also be expressed as (7.6).

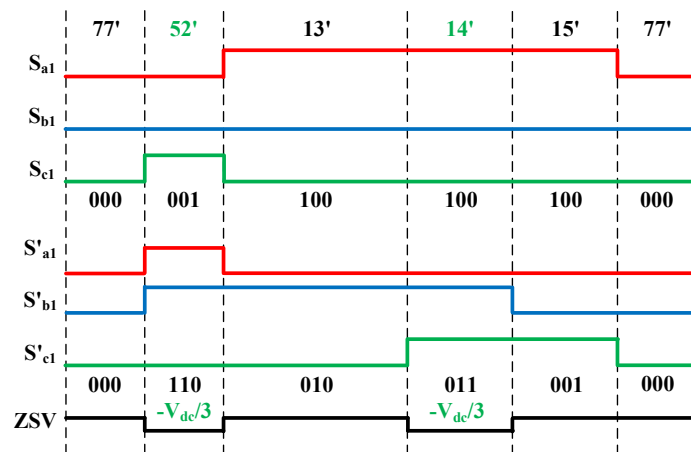
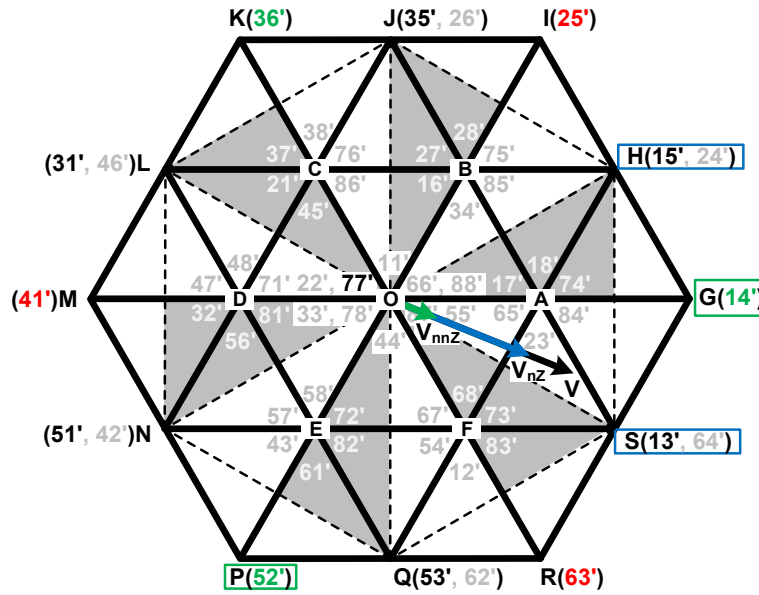
Figs. 7.5 (a) and (b) show the reference voltage vector, switching combinations, and PWM waveforms in sector 2 with the proposed PWM strategy, when the refernece ZSV is positive

and negative, respectively. With a positive reference ZSV, the selection of null and positive ZSV switching combinations is the same for sectors 1 and 2 as shown in Fig. 7.4 (a) and Fig. 7.5 (a). With a negative reference ZSV in sector 2 in Fig. 7.5 (b), the use of null ZSV switching combinations keeps the same, but the selection of negative ZSV switching combinations is different from these in sector 1 in Fig. 7.4 (b), and 52' and 14' in sector 1 become 14' and 36' in sector 2. The six basic vectors on the large hexagon can be categorized into two groups, i.e. 25', 41', 63' with positive ZSV and 14', 36', 52' with negative ZSV. In Fig. 7.5 (b), the voltage vector  $\overrightarrow{OV_{nnZ}}$  is synthesized by two of three basic vectors with negative ZSV on the large hexagon, and the vector  $\overrightarrow{OV_{nnZ}}$  should be located between the two selected basic vectors with negative ZSV, and they have a 120-degree angle between each other. As a result, basic vectors 14' and 36' are selected, and the corresponding switching combinations 14' and 36' are used in sector 2 to generate negative ZSV. Due to four sectors, i.e. 120 degrees, between any two basic vectors with positive or negative ZSV on the large hexagon, the corresponding two switching combinations with non-null ZSV are used to control ZSC in the four sectors. For example, with the negative reference ZSV, two negative ZSV switching combinations, i.e. 14' and 36', are used to generate a controllable ZSV in sectors 2, 3, 4, and 5.





(a)  $V_0^* \geq 0$ .

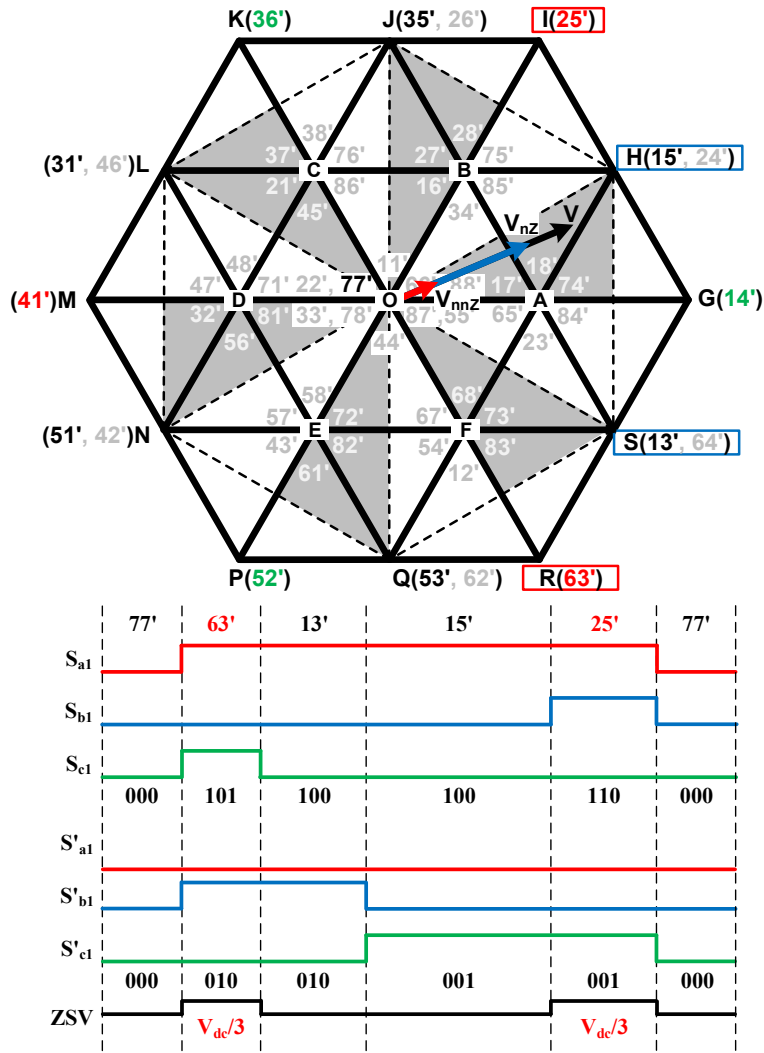


(b)  $V_0^* < 0$ .

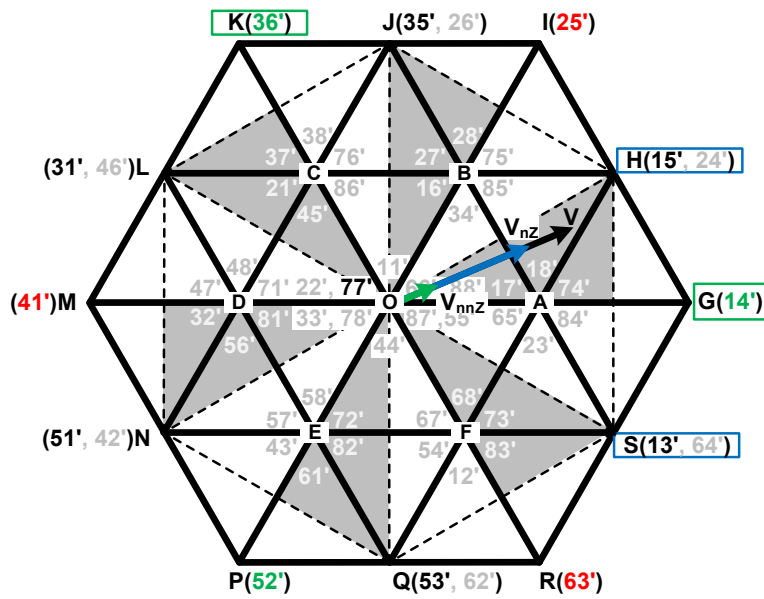
Fig. 7.4 Decomposition of the reference voltage vector, selection of switching combinations and PWM waveforms with the proposed SVPWM (Sector 1).

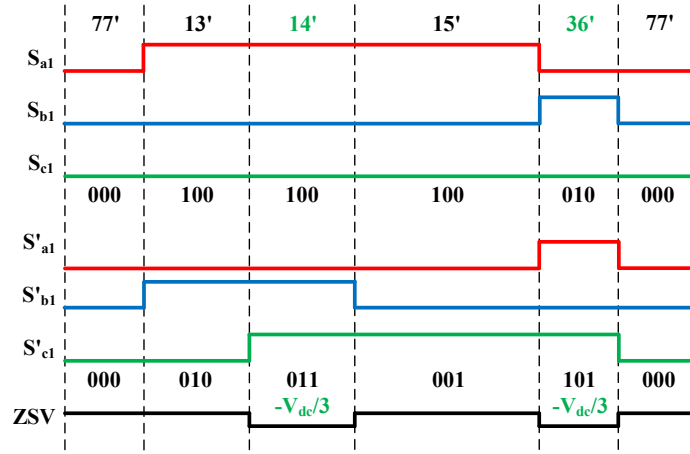
Basic vectors with non-null ZSV can synthesize the vector  $\overrightarrow{OV_{nnZ}}$ , which is not sufficient for the reference voltage vector  $\overrightarrow{OV}$ . As a result, the vector  $\overrightarrow{OV_{nz}}$  which is synthesized by basic vectors with null ZSV is used to supplement and achieve the required reference voltage vector  $\overrightarrow{OV}$ . Switching combinations (13', 15', 35', 31', 51', 53') with null ZSV correspond to six basic vectors with null ZSV on the middle hexagon. When the reference voltage vector is located within the 60 degree angle between two adjacent basic vectors with null ZSV, the corresponding switching combinations with null ZSV are used. For example, sectors 1 and 2 use the same switching combinations with null ZSV on the middle hexagon, i.e. 13' and 15'. According to the selection principles of switching combinations with null and non-null ZSVs in sectors 1 and 2 mentioned above, the selection of switching combinations can be achieved similarly in other sectors. Moreover, the durations for switching combinations with null and non-null ZSVs should be calculated to implement the proposed SVPWM strategy.

In the proposed SVPWM strategy, four effective vectors and a zero vector 77' at O point, are used. Among these four effective vectors, two basic vectors ( $V_{nz1}$ ,  $V_{nz2}$ ) with null ZSV are on the middle hexagon corresponding to null ZSV switching combinations, while the other basic two vectors ( $V_{nnz1}$ ,  $V_{nnz2}$ ) with non-null ZSV are on the large hexagon corresponding to non-null ZSV switching combinations. To achieve the ZSC control, the durations  $T_{nnz1}$  and  $T_{nnz2}$  for  $V_{nnz1}$  and  $V_{nnz2}$  should be calculated firstly. The sum of the durations  $T_{nnz1}$  and  $T_{nnz2}$  is the total duration  $T_{nnz}$ , i.e.  $T_{nnz} = T_{nnz1} + T_{nnz2}$ . Figs. 7.6 (a) and (b) show the three voltage vectors on the large hexagon with positive and negative ZSVs, respectively. Assuming  $V_{nnz1}$  leads  $V_{nnz2}$ , with angle  $\gamma$  for the reference voltage vector in Fig. 7.6,  $\lambda$  is the angle between  $V_{nnz1}$  and the reference voltage vector.



(a)  $V_o^* \geq 0$ .





(b)  $V_0^* < 0$ .

Fig. 7.5 Decomposition of the reference voltage vector, selection of switching combinations and PWM waveforms with the proposed SVPWM (Sector 2).

The relationship between  $\lambda$ ,  $\gamma$ , and the sign of  $V_0^*$  can be expressed as

$$\lambda = \begin{cases} \begin{cases} \gamma + \frac{\pi}{3} & -\frac{\pi}{3} \leq \gamma < \frac{\pi}{3} \\ \gamma - \frac{\pi}{3} & \frac{\pi}{3} \leq \gamma < \pi \end{cases} & \text{when } V_0^* \geq 0 \\ \begin{cases} \gamma - \pi & \pi \leq \gamma < \frac{5\pi}{3} \\ \gamma & 0 \leq \gamma < \frac{2\pi}{3} \\ \gamma - \frac{2\pi}{3} & \frac{2\pi}{3} \leq \gamma < \frac{4\pi}{3} \\ \gamma - \frac{4\pi}{3} & \frac{4\pi}{3} \leq \gamma < 2\pi \end{cases} & \text{when } V_0^* < 0 \end{cases} \quad (7.7)$$

Figs. 7.6 (a) and (b) also show the angle  $\lambda$  when the reference voltage vector  $\vec{OV}$  is in sector 2 with positive and negative  $V_0^*$ , respectively.  $T_{nnZ1}$  and  $T_{nnZ2}$  can be calculated as

$$\begin{aligned} T_{nnZ1} &= \frac{\sin(2\pi/3 - \lambda) T_{nnZ}}{\sin\lambda + \sin(2\pi/3 - \lambda)} \\ T_{nnZ2} &= \frac{\sin\lambda T_{nnZ}}{\sin\lambda + \sin(2\pi/3 - \lambda)} \end{aligned} \quad (7.8)$$

$\alpha$  and  $\beta$  axis voltages of  $\vec{OV}_{nnZ}$  which is synthesized by  $V_{nnZ1}$  and  $V_{nnZ2}$  can be expressed as

$$\begin{aligned}
V_{mz\alpha} &= \frac{2T_{mz1}V_{dc}\cos\gamma}{\sqrt{3}T_{PWM}\sin(2\pi/3-\lambda)} \\
V_{mz\beta} &= \frac{2T_{mz1}V_{dc}\sin\gamma}{\sqrt{3}T_{PWM}\sin(2\pi/3-\lambda)}
\end{aligned}
\tag{7.9}$$

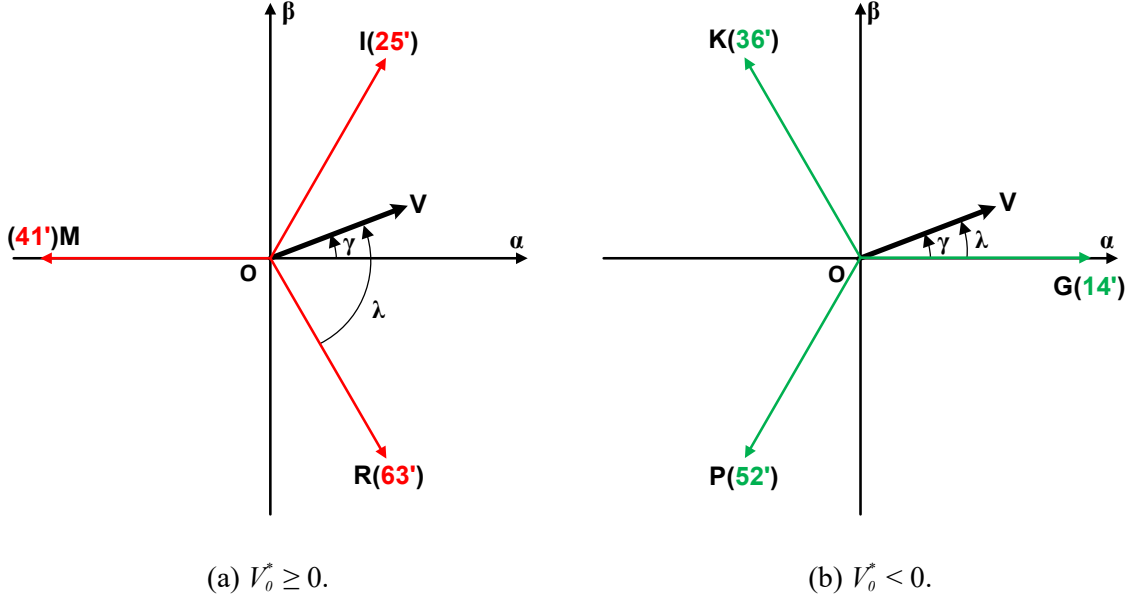


Fig. 7.6 Angle  $\delta$  between  $V_{nz1}$  and  $\alpha$ -axis.

Since  $V_{nnz1}$  and  $V_{nnz2}$  only can synthesize a part of the reference voltage vector, the vector  $\overline{OV_{nz}}$  is synthesized by two basic vectors  $V_{nz1}$ , and  $V_{nz2}$  with null ZSV as a supplement.  $\alpha$  and  $\beta$  axis voltages of the vector  $\overline{OV_{nz}}$  can be calculated as

$$\begin{aligned}
V_{nz\alpha} &= V_{\alpha}^* - V_{mz\alpha} \\
V_{nz\beta} &= V_{\beta}^* - V_{mz\beta}
\end{aligned}
\tag{7.10}$$

where  $V_{\alpha}^*$  and  $V_{\beta}^*$  are the reference voltages in  $\alpha$  and  $\beta$  axes for DTL-VSIs.

With reference voltages  $V_{nz\alpha}$  and  $V_{nz\beta}$  in  $\alpha$  and  $\beta$  axes, durations  $T_{nz1}$  and  $T_{nz2}$  for  $V_{nz1}$  and  $V_{nz2}$  can be calculated according to SVPWM. With durations of four effective vectors  $V_{nz1}$ ,  $V_{nz2}$ ,  $V_{nnz1}$ , and  $V_{nnz2}$ , the duration of the zero vector can be calculated as  $T_0 = T_{PWM} - (T_{nnz1} + T_{nnz2} + T_{nz1} + T_{nz2})$ , so that durations of all basic vectors can be acquired. When  $T_{PWM} < (T_{nnz1} + T_{nnz2} + T_{nz1} + T_{nz2})$ , the DTL-VSIs enter the over modulation region. To maintain the controllability of ZSC,  $T_{nnz1}$  and  $T_{nnz2}$  should remain unchanged, and the modified durations  $T'_{nz1}$  and  $T'_{nz2}$  for the two basic vectors  $V_{nz1}$  and  $V_{nz2}$  with null ZSV can be expressed as



$$\begin{aligned}
T'_{nZ1} &= \frac{T_{nZ1}}{T_{nZ1} + T_{nZ2}} (T_{PWM} - T_{nnZ1} - T_{nnZ2}) \\
T'_{nZ2} &= \frac{T_{nZ2}}{T_{nZ1} + T_{nZ2}} (T_{PWM} - T_{nnZ1} - T_{nnZ2})
\end{aligned} \tag{7.11}$$

Fig. 7.7 shows the control diagram of the proposed SVPWM strategy. The relationship between  $T'_{nZ1}$ ,  $T'_{nZ2}$ , and  $T_{nnZ}$  can be expressed as

$$T'_{nZ1} + T'_{nZ2} = T_{PWM} - T_{nnZ} . \tag{7.12}$$

The magnitude of  $\overrightarrow{OV_{nZ}}$  can be expressed as

$$|\overrightarrow{OV_{nZ}}| \leq \frac{V_{dc}}{\cos \varphi} \frac{T_{PWM} - T_{nnZ}}{T_{PWM}} . \tag{7.13}$$

According to (7.8), the magnitude of voltage vector  $\overrightarrow{OV_{nnZ}}$  that is synthesized by basic vectors with non-null ZSV can be expressed as

$$|\overrightarrow{OV_{nnZ}}| = \frac{2T_{nnZ}V_{dc}}{\sqrt{3}T_{PWM}(\sin\lambda + \sin(2\pi/3 - \lambda))} . \tag{7.14}$$

As  $\overrightarrow{OV_{nZ}}$  and  $\overrightarrow{OV_{nnZ}}$  are with the same direction, the magnitude of  $\overrightarrow{OV}$  can be calculated according to (7.6), (7.13), and (7.14).

$$|\overrightarrow{OV}| \leq \frac{V_{dc}}{\cos \varphi} - \frac{3|V_o^*|}{\cos \varphi} + \frac{6|V_o^*|}{\sqrt{3}(\sin\lambda + \sin(2\pi/3 - \lambda))} . \tag{7.15}$$

The difference between the maximum magnitudes of  $\overrightarrow{OV}$  in the proposed and conventional SVPWMs in (7.15) and (7.4) is

$$\left( \underbrace{\frac{6}{\sqrt{3}(\sin\lambda + \sin(2\pi/3 - \lambda))} - \frac{2}{\cos \varphi}}_g \right) |V_o^*| . \tag{7.16}$$

According to (7.5) and (7.7),  $\varphi$  depends on  $\gamma$ , while  $\lambda$  depends on  $\gamma$  and the sign of  $V_o^*$ . As a result,  $g$  depends on  $\gamma$  and the sign of  $V_o^*$ , and can be expressed as

$$g = f(\gamma, \text{sign}(V_o^*)) . \tag{7.17}$$

The coefficient  $g$  can reflect the increment of output voltages in the proposed SVPWM compared with the conventional SVPWM. The coefficient  $g$  in an electrical cycle with positive and negative  $V_0^*$  is depicted in Fig. 7.8, and varies between 0 and 2. Consequently, the proposed SVPWM has larger maximum output voltages and modulation region compared with those in the conventional SVPWM.

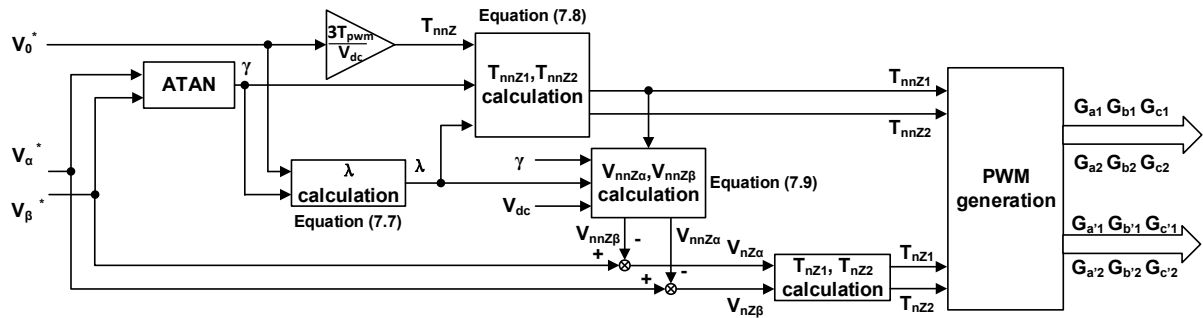


Fig. 7.7 Control diagram of the proposed SVPWM strategy.

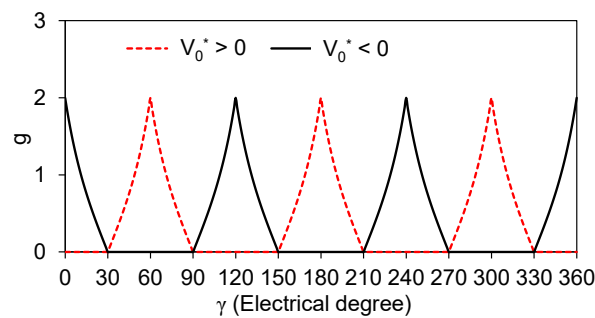


Fig. 7.8 Coefficient  $g$  in an electrical cycle with positive and negative  $V_0^*$ .

Apart from PWM, the main component of ZSV sources is the third BEMF harmonic in an OW-PMSM drive, so that the reference ZSV  $V_0^*$  is an alternating voltage with the triple of fundamental electrical frequency. Figs. 7.9 (a) and (b) show the reference ZSV  $V_0^*$  and  $g$  with respect to  $\gamma$ , when the angle between the reference voltage vector and  $q$ -axis is 0 and 15 electrical degrees, respectively. There is a phase shift of  $V_0^*$  in Figs. 7.9 (a) and (b). As a result,  $g$  is affected by the angle between the reference voltage vector and  $q$ -axis. In Fig. 7.9 (a),  $g$  is zero only when  $\gamma$  equals  $30+60k$  electrical degrees ( $k = 0-5$ ). In Fig. 7.9 (b),  $g$  is zero when  $\gamma$  is between  $30+60k$  and  $45+60k$  electrical degrees. With the increase of the angle between the reference voltage vector and  $q$ -axis, the average value of  $g$  will decrease. In an OW-PMSM drive, the  $q$ -axis voltage is dominated due to the BEMF. As a result, a large  $g$  exists by applying the proposed SVPWM, and the modulation region can be enlarged compared with the conventional SVPWM.

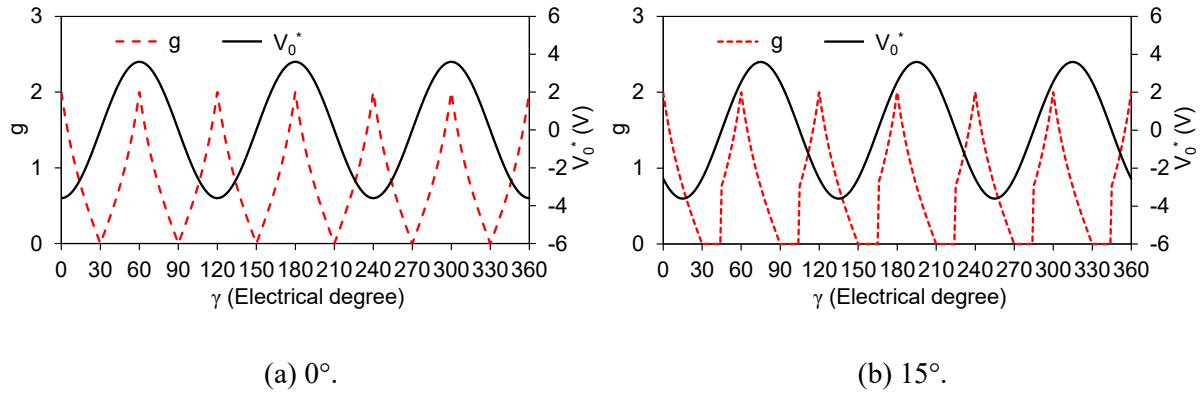


Fig. 7.9 Coefficient  $g$  and reference ZSV in an electrical cycle with different angle between the reference voltage vector and  $q$ -axis.

## 7.4 Experiment Results

The conventional and proposed SVPWM strategies are experimentally validated and compared in a common DC-bus DTL-VSIs-fed OW-PMSM in this chapter. Parameters of the tested OW-PMSM are shown in Table 6.3. The measured phase A BEMF and the spectrum analysis of the OW-PMSM at 420rpm are shown in Fig. 6.11. There is a large component of the third harmonic, approximately 10% of the fundamental component. The interrupt frequency and the PWM frequency are 10kHz. The DC-bus voltage of the common DC-bus DTL-VSIs is 36V. The experimental platform is shown in Fig. 6.12, including DTL-VSIs, a dSPACE, an OW-PMSM, a position sensor, and a load machine.

The OW-PMSM fed by common DC-bus dual two-level inverters is controlled with the proposed and conventional SVPWM strategies as shown in Fig. 5.6 and Fig. 7.3, respectively. To compare the maximum operation ranges of the conventional and proposed SVPWM strategies, the ZSC control in the OW-PMSM drive can be maintained in the over modulation region, and the flux weakening control is used. In this section, the superiority of the proposed SVPWM will be verified experimentally.

Fig. 7.10 shows three phase currents, ZSC, and phase A current spectrum before the ZSC control at 400rpm and the maximum torque of 4.3 Nm with the proposed SVPWM strategy. Since the main component of other ZSV sources is the third BEMF harmonic, ZSC is induced with triple of fundamental electrical frequency as shown in Fig. 7.10 (b). After the ZSC control, ZSC can be suppressed as shown in Figs. 7.15 (a) and (b).

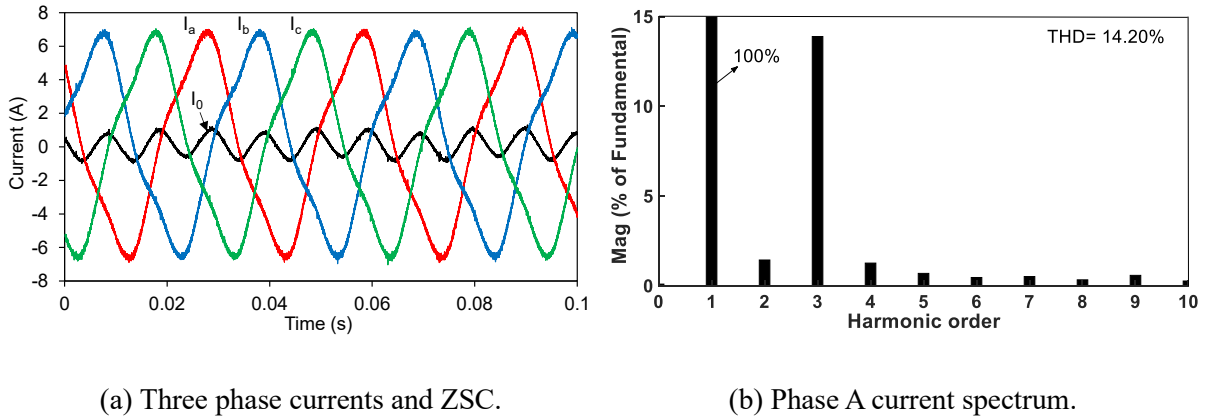
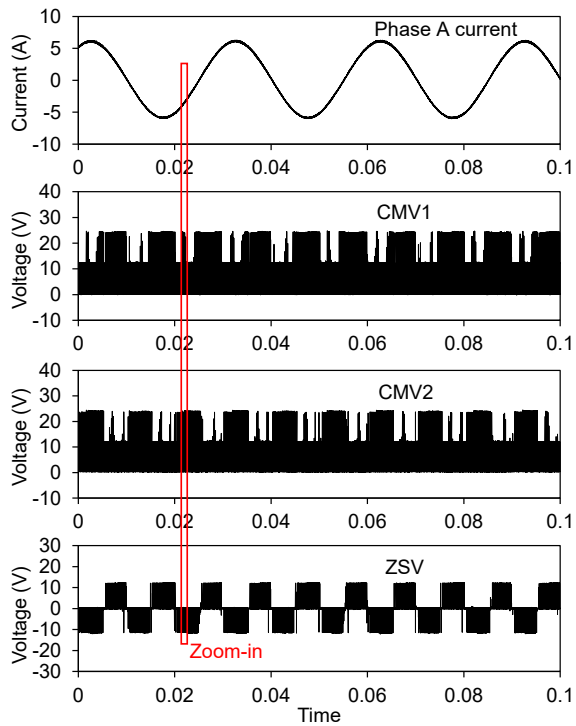


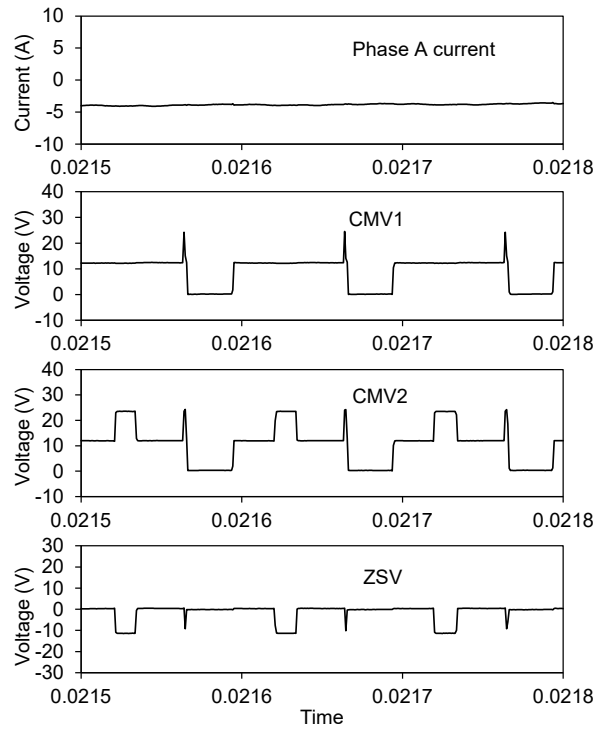
Fig. 7.10 Three phase currents, ZSC, and phase A current spectrum of the proposed SVPWM before the ZSC control (Torque = 4.3 Nm, Speed = 400 rpm).

Figs. 7.11 and 7.12 show the phase A current, CMVs of two inverters, and ZSV of the DTL-VSIs with the proposed SVPWM in linear modulation region (torque = 4.3 Nm, speed = 400 rpm) and over modulation region (torque = 0.35 Nm, speed = 1125 rpm), respectively. ZSV of the DTL-VSIs is the difference between CMVs of two inverters. The frequency of ZSV from PWM in Figs. 7.11 (a) and 7.12 (a) is triple of the electrical frequency, since the main component of other ZSV sources is the third BEMF harmonic. Figs. 7.11 (b) and 7.12 (b) are magnified views of the highlighted regions in Figs. 7.11 (a) and 7.12 (a), respectively. It can be seen that with the proposed ZSC control, two pulse of ZSV can be generated by PWM to counteract with ZSVs from other sources, which is consistent with theoretic analysis in Section 7.3.

Fig. 7.13 show the acceleration performance of OW-PMSM with the proposed SVPWM. The speed accelerates from 0 to 1125rpm with an acceleration of 400rpm/s as shown in Fig. 7.13 (a). Fig. 7.13 (b) shows three phase currents during the acceleration, and ZSC can be suppressed in the whole process. Fig. 7.13 (c) shows  $dq$ -axis currents during the acceleration, and the OW-PMSM enters flux weakening control regions with the speed rise.

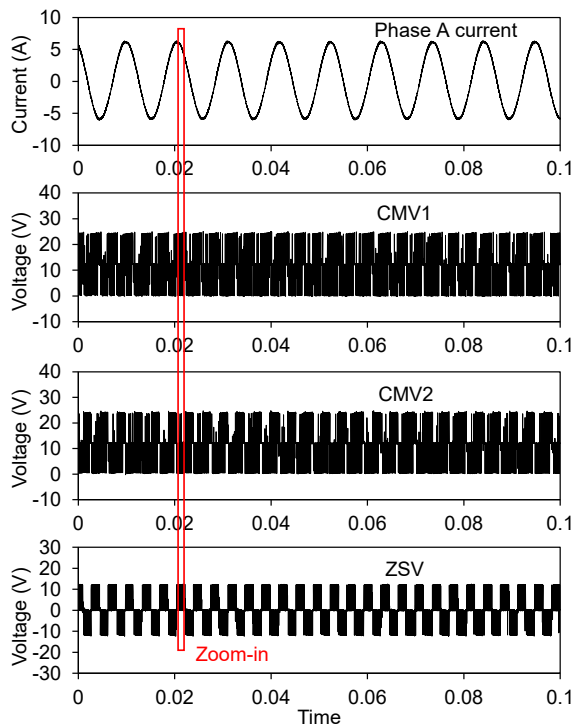


(a)  $I_a$ , CMVs, and ZSV.

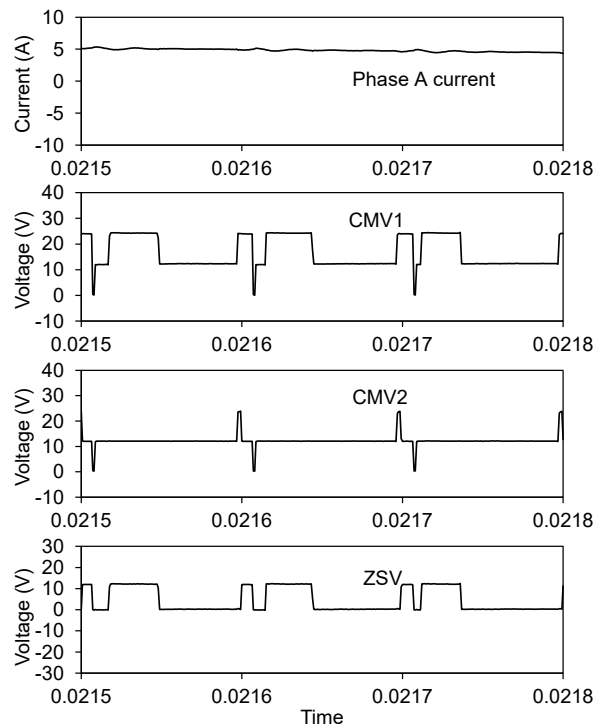


(b)  $I_a$ , CMVs, and ZSV in the Zoom-in region.

Fig. 7.11 Phase A current, CMVs of two inverters, and ZSV of DTL-VSIs with the proposed SVPWM. (Torque = 4.3 Nm, Speed = 400 rpm).

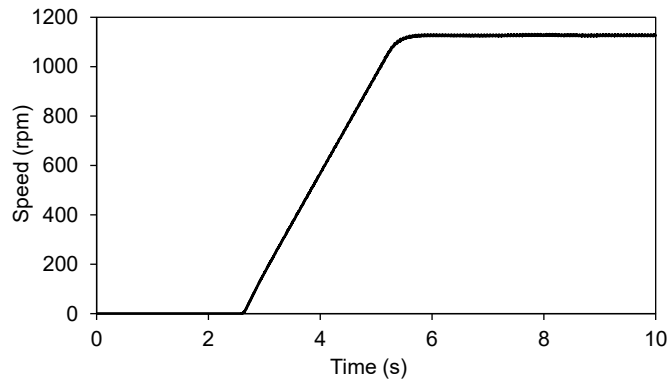


(a)  $I_a$ , CMVs, and ZSV.

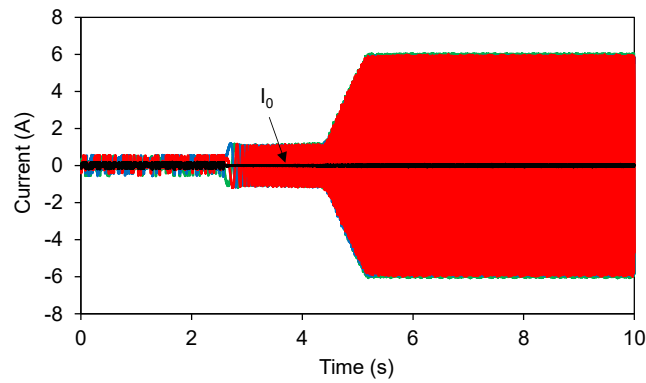


(b)  $I_a$ , CMVs, and ZSV in the Zoom-in region.

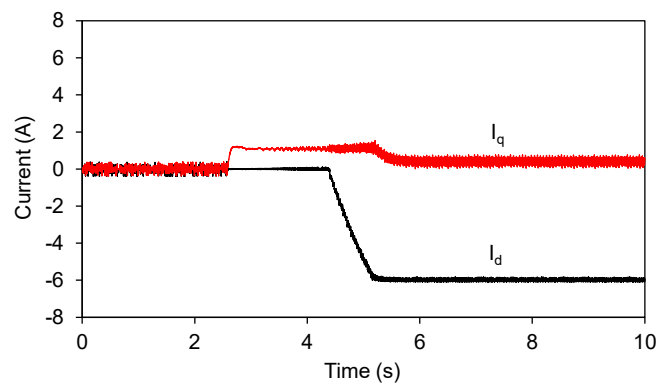
Fig. 7.12 Phase A current, CMVs of two inverters, and ZSV of DTL-VSIs with the proposed SVPWM (Torque = 0.35 Nm, Speed = 1125 rpm).



(a) Speed.



(b) Three phase currents and ZSC.

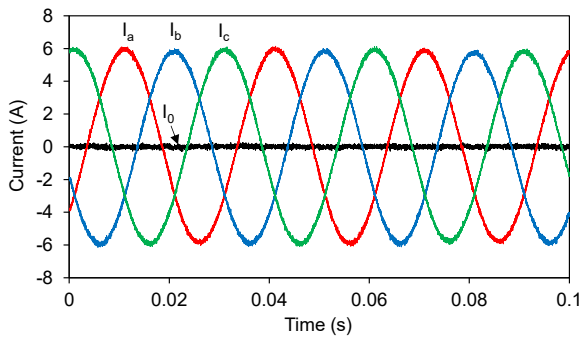


(c) *Dq*-axis currents.

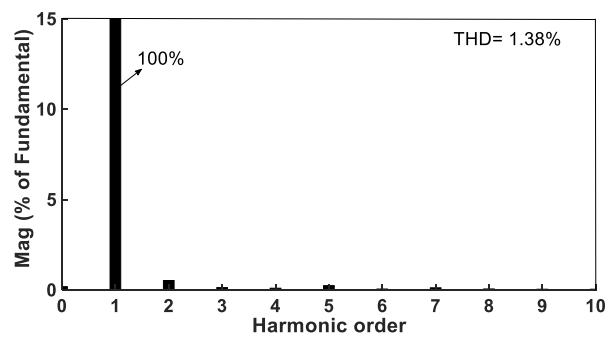
Fig. 7.13 Acceleration of OW-PMSM with the propose SVPWM (400rpm/s).

Figs. 7.14 and 7.15 compare three phase currents, phase A current spectrum, ZSC, *dq*-axis currents, speed, and  $\alpha$  and  $\beta$  axis voltages of the OW-PMSM at 400rpm and the maximum torque 4.3 Nm with the conventional and proposed SVPWM strategies, respectively. As the OW-PMSM is operated in the linear modulation region, the conventional and proposed SVPWM strategies have almost the same control performance. *D*-axis current of OW-PMSM

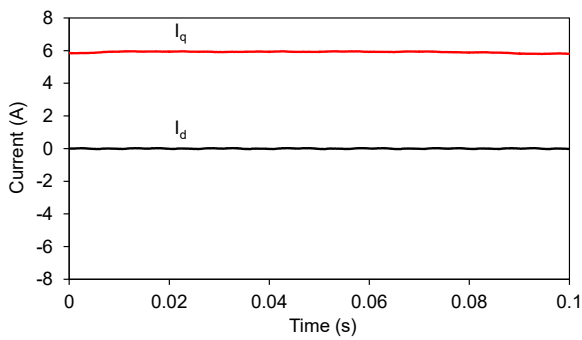
is zero, while  $q$ -axis current is 6A. ZSC can be suppressed by both the conventional and proposed SVPWM strategies.



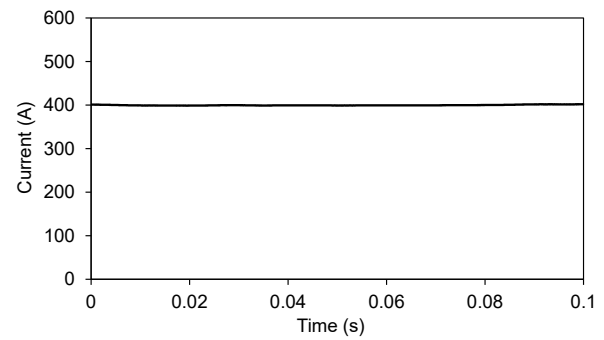
(a) Three phase currents and zero sequence current.



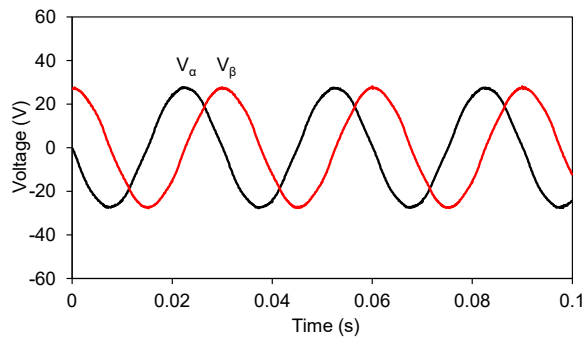
(b) Phase A current spectrum.



(c)  $D$  and  $q$  axis currents.

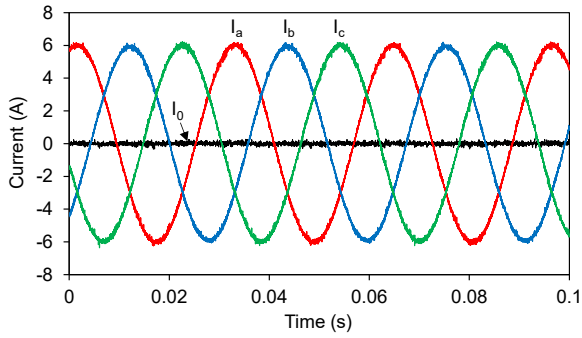


(d) Speed.

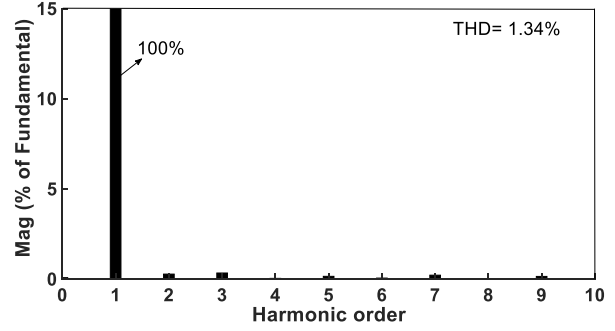


(e)  $\alpha$  and  $\beta$  axis voltages.

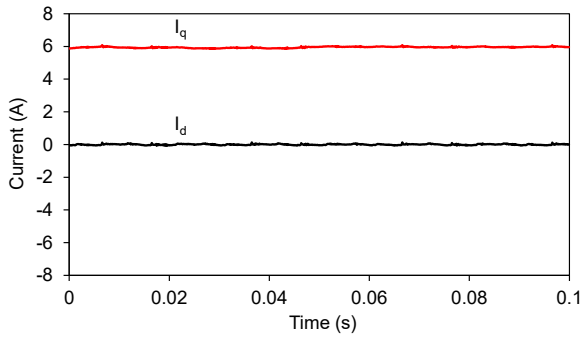
Fig. 7.14 Control performance of the OW-PMSM with conventional SVPWM (Torque = 4.3 Nm, Speed = 400 rpm).



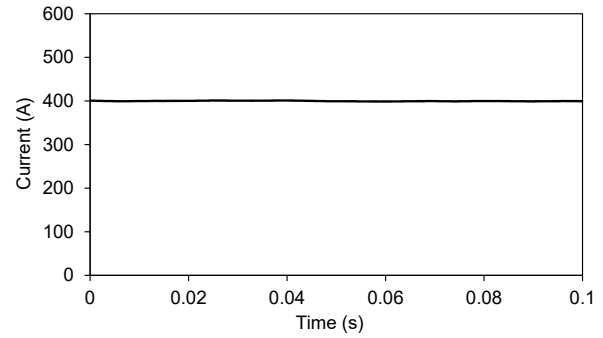
(a) Three phase currents and zero sequence current.



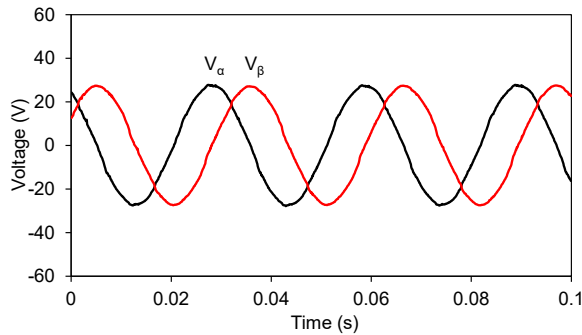
(b) Phase A current spectrum.



(c)  $D$  and  $q$  axis currents.



(d) Speed.



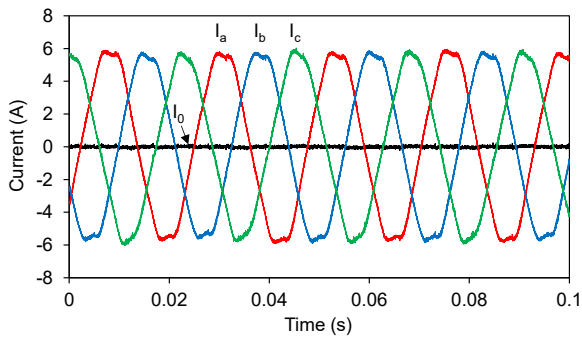
(e)  $\alpha$  and  $\beta$  axis voltages.

Fig. 7.15 Control performance of the OW-PMSM with proposed SVPWM (Torque = 4.3 Nm, Speed = 400 rpm).

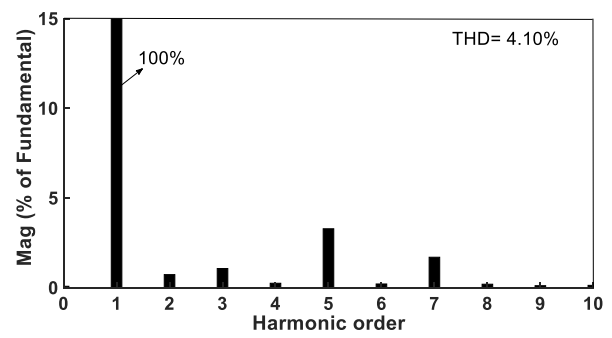
To illustrate the maximum speed of the OW-PMSM with maximum torque under the constant torque region, Fig. 7.16 and Fig. 7.17 compare the control performance of the conventional and proposed SVPWMs, respectively, in the over modulation region with the maximum torque of 4.3 Nm.  $Dq$ -axis currents for two SVPWMs are the same, i.e.  $i_d = 0$ ,  $i_q = 6$ A. ZSC can be controlled to zero for both the conventional and proposed SVPWM strategies. However, due to the larger modulation region of the proposed SVPWM, the speed of the proposed SVPWM



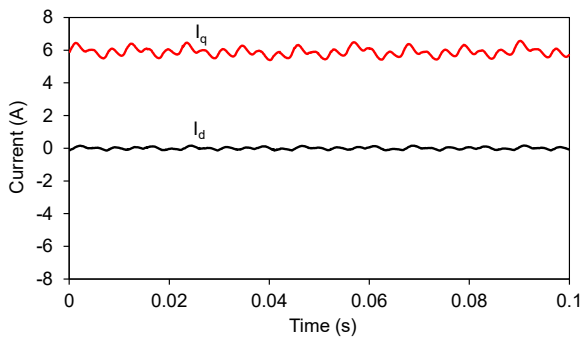
(590 rpm) is larger than the speed of the conventional SVPWM (535 rpm), as shown in Fig. 7.16 (d) and Fig. 7.17 (d).



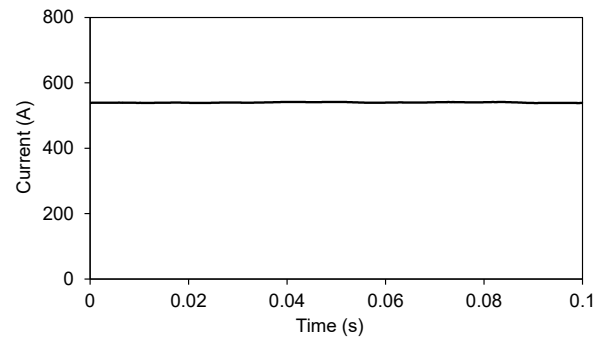
(a) Three phase currents and zero sequence current.



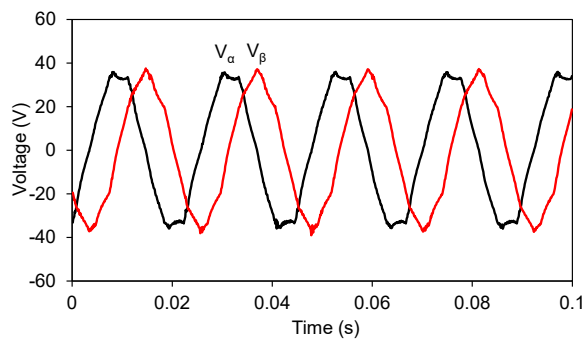
(b) Phase A current spectrum.



(c)  $D$  and  $q$  axis currents.

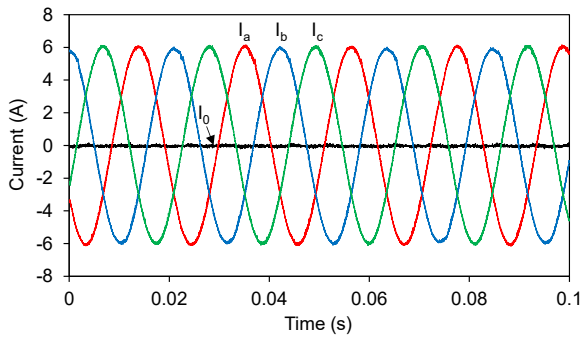


(d) Speed.

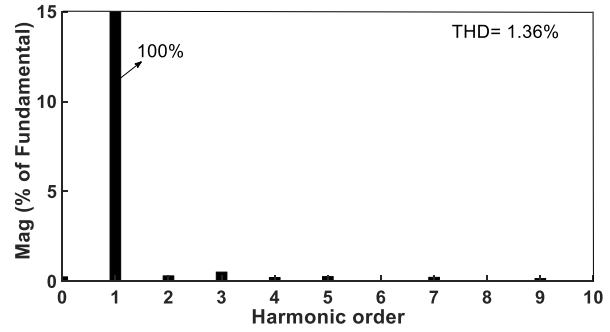


(e)  $\alpha$  and  $\beta$  axis voltages.

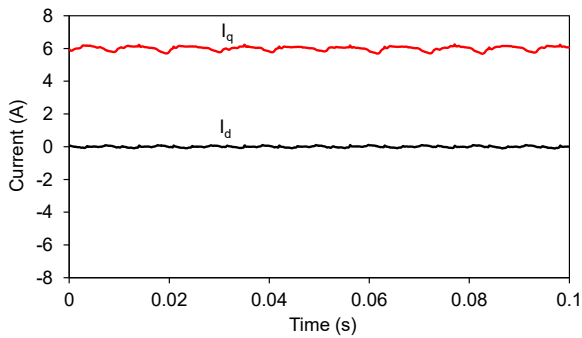
Fig. 7.16 Control performance of the OW-PMSM with conventional SVPWM (Torque = 4.3 Nm, Speed = 535 rpm).



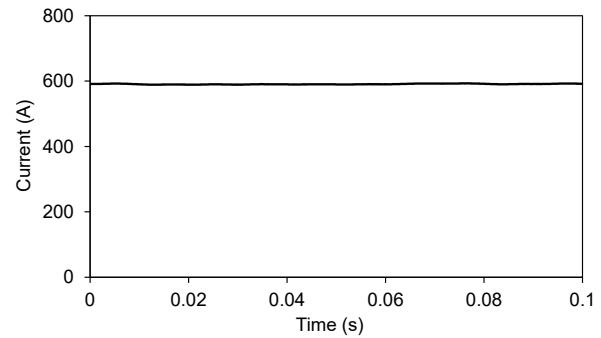
(a) Three phase currents and zero sequence current.



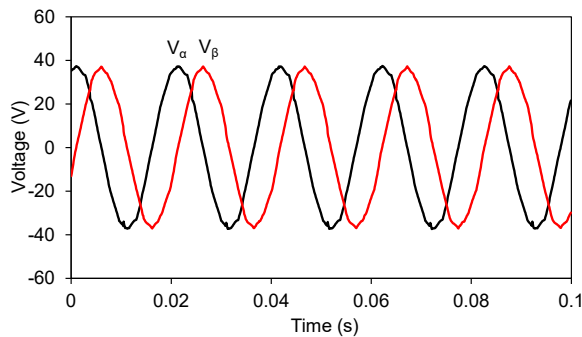
(b) Phase A current spectrum.



(c)  $D$  and  $q$  axis currents.



(d) Speed.

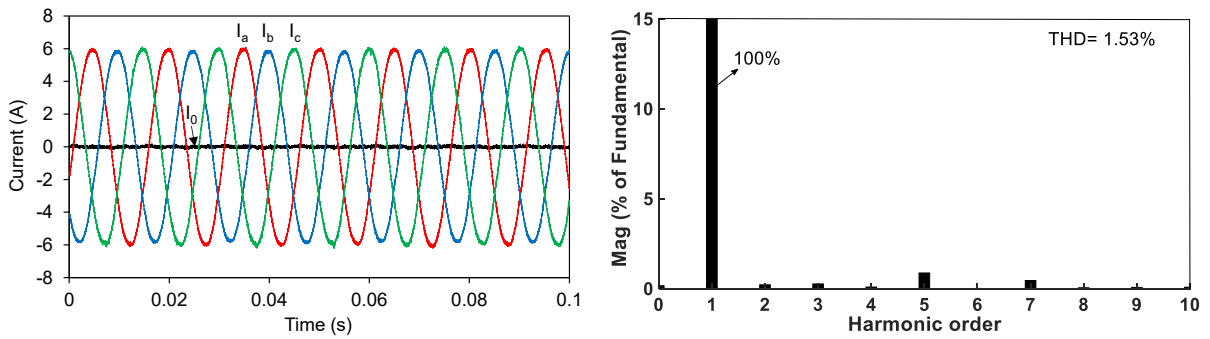


(e)  $\alpha$  and  $\beta$  axis voltages.

Fig. 7.17 Control performance of the OW-PMSM in 590rpm with proposed SVPWM (Torque = 4.3 Nm, Speed = 590 rpm).

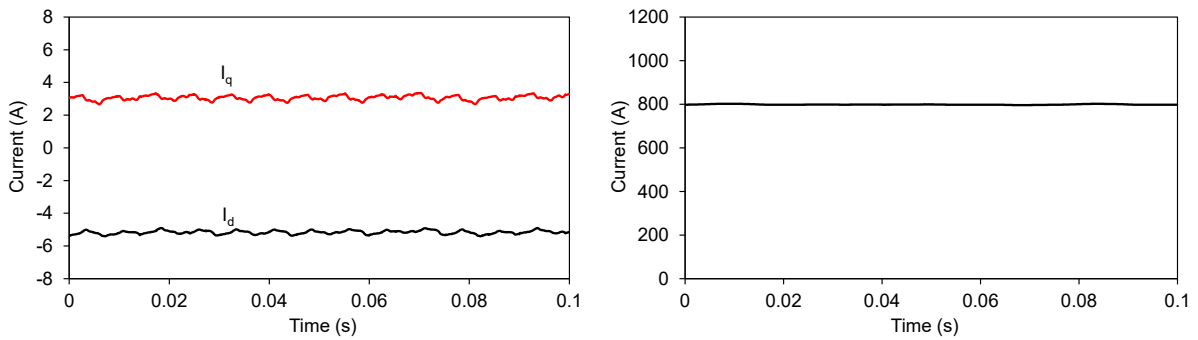
Figs. 7.18 and 7.19 compare the control performance with the conventional and proposed SVPWMs, respectively, in over modulation region with the speed of 800 rpm. Both the conventional and proposed SVPWM strategies can achieve the ZSC suppression. The OW-PMSM is operated in flux-weakening region, and less flux-weakening current is needed in the proposed SVPWM, since the modulation region is enlarged when compared to the conventional SVPWM.  $D$ -axis current is -5.2 A in the conventional SVPWM, and it becomes -4.5 A in the

proposed SVPWM. As a result, in the proposed SVPWM, there is more current margin for  $q$ -axis current, which increases from 3 A to 3.85 A. Consequently, the proposed SVPWM can generate larger torque of 2.8 Nm, compared with 2.2 Nm in the conventional SVPWM.



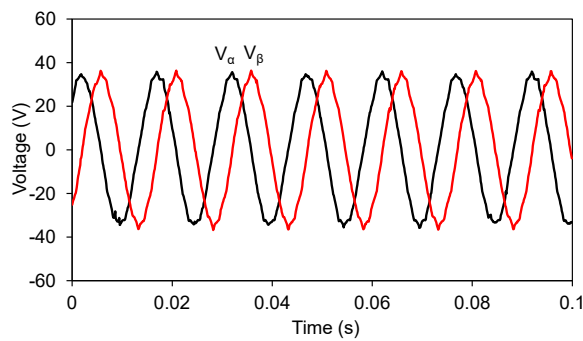
(a) Three phase currents and zero sequence current.

(b) Phase A current spectrum.



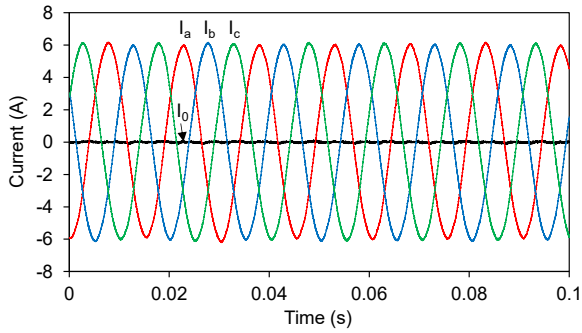
(c)  $D$  and  $q$  axis currents.

(d) Speed.

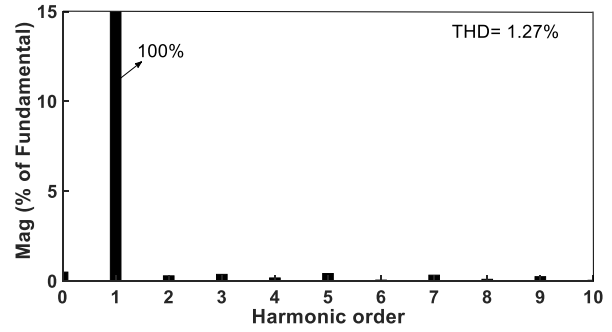


(e)  $\alpha$  and  $\beta$  axis voltages.

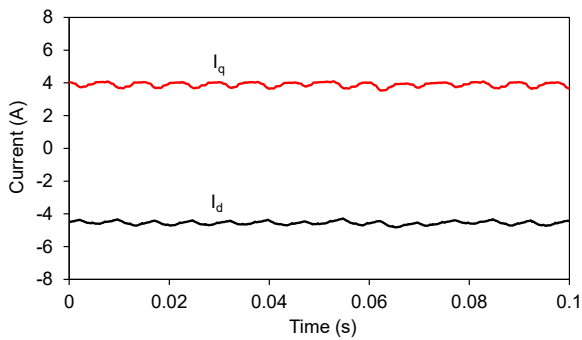
Fig. 7.18 Control performance of the OW-PMSM with conventional SVPWM (Torque = 2.2 Nm, Speed = 800 rpm).



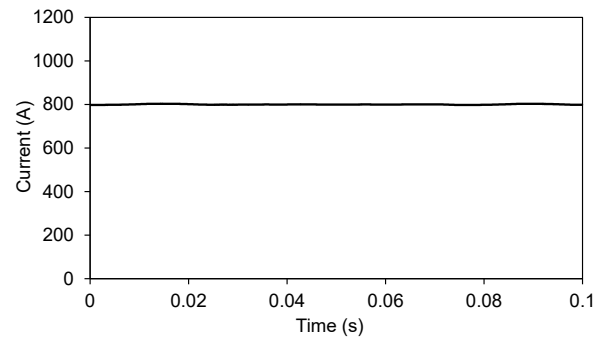
(a) Three phase currents and zero sequence current.



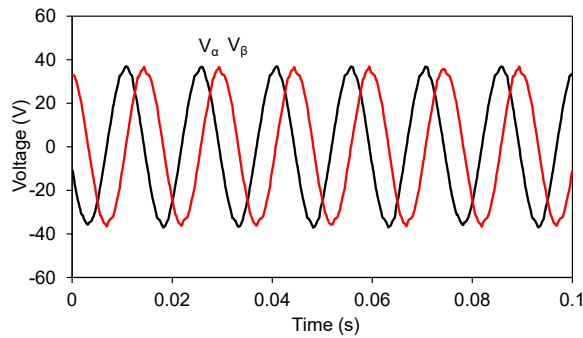
(b) Phase A current spectrum.



(c) D and q axis currents.



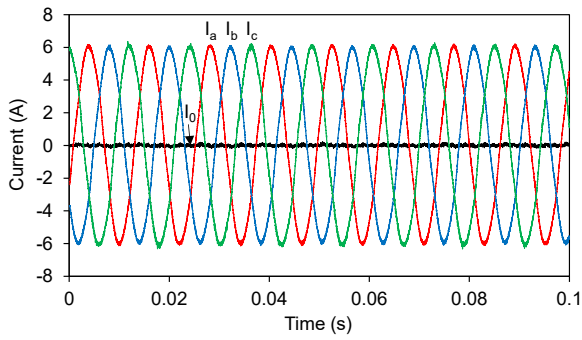
(d) Speed.



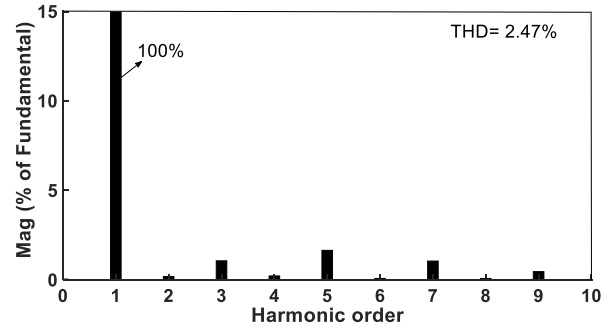
(e)  $\alpha$  and  $\beta$  axis voltages.

Fig. 7.19 Control performance of the OW-PMSM with proposed SVPWM (Torque = 2.8 Nm Speed = 800 rpm).

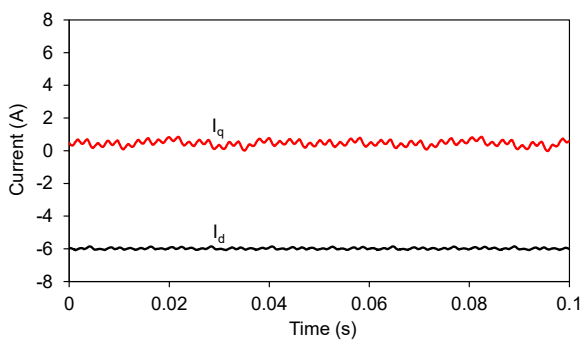
Figs. 7.20 and 7.21 compare the control performance of the conventional and proposed SVPWMs, respectively, in over modulation region with the torque 0.35 Nm. ZSC can be suppressed by both the conventional and proposed SVPWMs. Due to the larger modulation region of the proposed SVPWM, the speed of the proposed SVPWM (1125 rpm) is larger than the speed of the conventional SVPWM (998 rpm) as shown in Fig. 7.20 (d) and Fig. 7.21 (d).



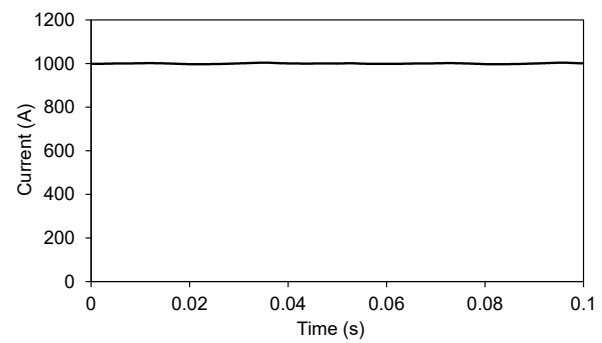
(a) Three phase currents and zero sequence current.



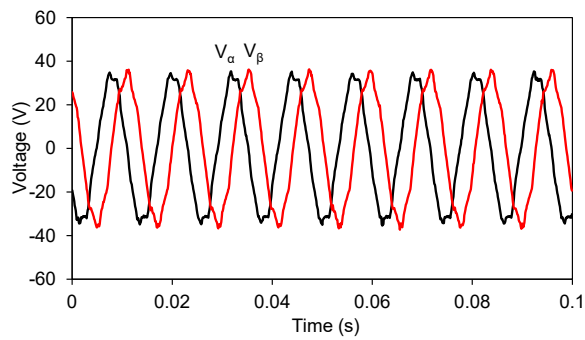
(b) Phase A current spectrum.



(c) D and q axis currents.

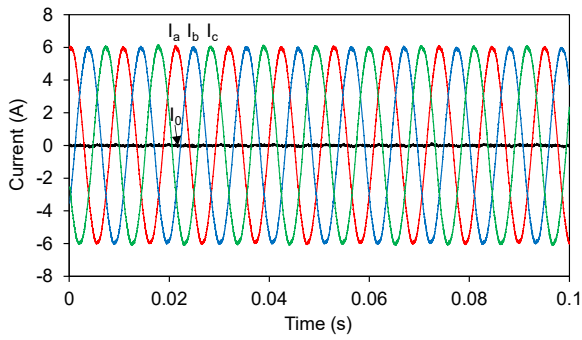


(d) Speed.

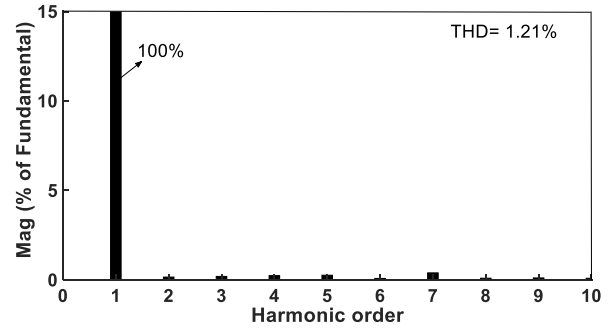


(e)  $\alpha$  and  $\beta$  axis voltages.

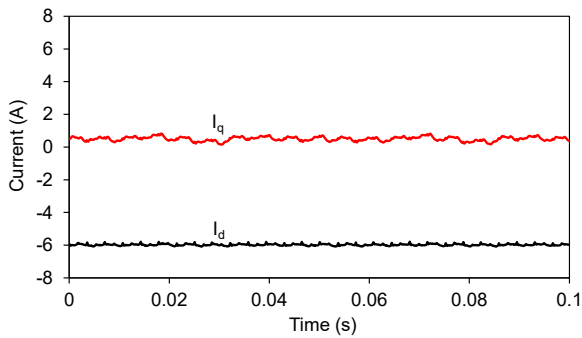
Fig. 7.20 Control performance of the OW-PMSM with conventional SVPWM (Torque = 0.35 Nm, Speed = 998 rpm).



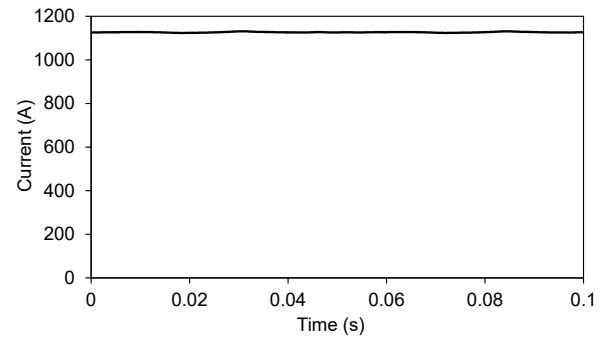
(a) Three phase currents and zero sequence current.



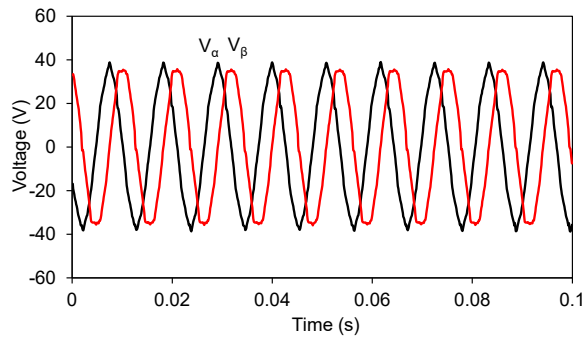
(b) Phase A current spectrum.



(c) D and q axis currents.



(d) Speed.



(e)  $\alpha$  and  $\beta$  axis voltages.

Fig. 7.21 Control performance of the OW-PMSM with proposed SVPWM (Torque = 0.35 Nm, Speed = 1125 rpm).

With the  $\alpha$  and  $\beta$  axis voltages after the over modulation in Fig. 7.14-7.21 (e), voltage trajectories in  $\alpha\beta$ -plane of the proposed and conventional SVPWM strategies are depicted in Fig. 7.22. The middle hexagon of DTL-VSIs is also shown in Fig. 7.22 as a reference, and voltage trajectories of the conventional SVPWM are always within the middle hexagon, but voltage trajectories of the proposed SVPWM strategy can be extended out of the middle hexagon in some operation points. The voltage trajectories of the conventional and proposed

SVPWM strategies are overlapped in the linear modulation region in Fig. 7.22 (a). However, in the over modulation region in Figs. 22 (b)-(d), the proposed SVPWM has larger maximum modulation region than that of the conventional SVPWM. Moreover, with the increase of speed, the difference between the two voltage trajectories become larger.

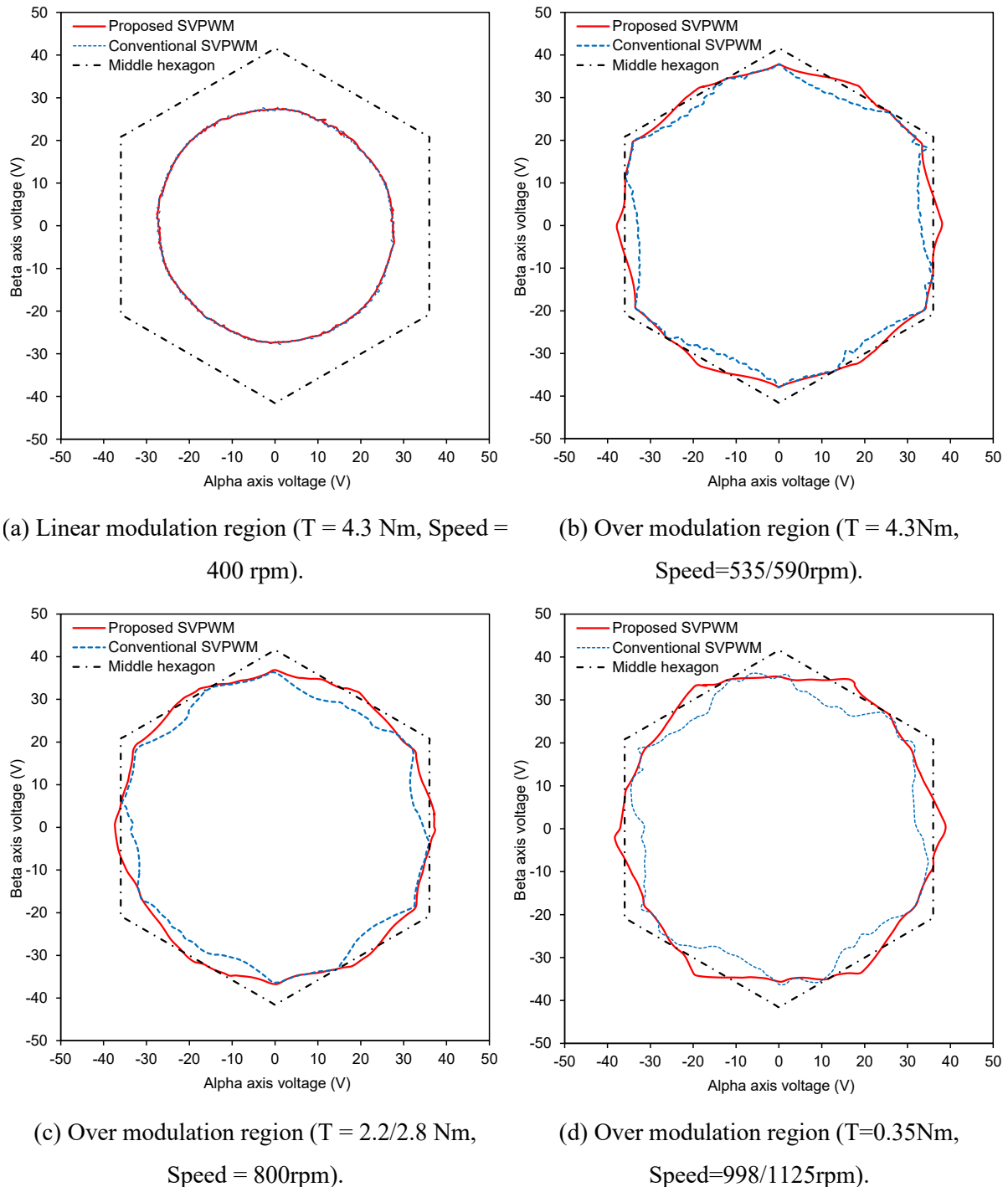


Fig. 7.22 Voltage trajectories in  $\alpha\beta$ -plane of proposed and conventional SVPWM strategies.

The conventional and proposed SVPWMs have similar current harmonics in the linear modulation region as shown in Fig. 7.14 (b) and Fig. 7.15 (b). However, due to the different

voltage trajectories of the proposed and conventional SVPWMs in the over modulation region in Figs. 22 (b)-(d), the current harmonics of the proposed SVPWM in Fig. 7.17 (b), Fig. 7.19 (b), and Fig. 7.21(b) are lower than that of the conventional SVPWM in Fig. 7.16(b), Fig. 7.18(b), and Fig. 7.20 (b).

Fig. 7.23 shows the torque-speed curves of the OW-PMSM with the conventional and proposed SVPWM strategies. The maximum speed of constant torque region is increased from 535rpm in the conventional SVPWM to 590 rpm in the proposed SVPWM, and the maximum speed of the flux weakening region is increased from 998rpm to 1125rpm. As a result, with the same torque, the proposed SVPWM can increase the speed of the OW-PMSM by over 10% compared with the conventional SVPWM.

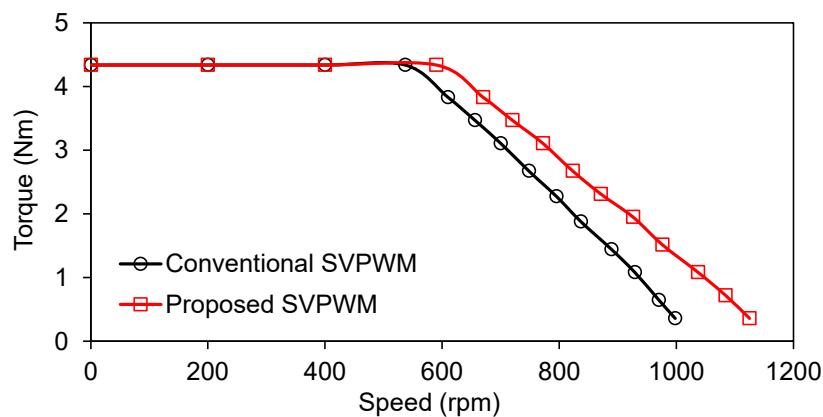


Fig. 7.23 Torque-speed curves of the OW-PMSM with conventional and proposed SVPWM strategies.

## 7.5 Summary

In this chapter, a novel SVPWM with ZSC control strategy is proposed to increase the operation range of a three phase OW-PMSM fed by common DC-bus DTL-VSIs. The proposed SVPWM has an optimal selection of switching combinations on the large hexagon, rather than on the small hexagon in the conventional SVPWM, for ZSC control to enlarge the maximum modulation region. The proposed SVPWM has a similar control performance as the conventional SVPWM in the linear modulation region, but has a larger torque with the same speed or a higher speed with the same torque in the over modulation region. Thus, the proposed SVPWM has a larger operation range compared with the conventional SVPWM, and the superiority of the proposed method increases with the speed rise. The proposed and conventional SVPWMs are compared experimentally in both linear and over modulation regions, and the operation range of the OW-PMSM can be extended over 10% by the proposed SVPWM.



# CHAPTER 8 GENERAL CONCLUSION AND FUTURE WORK

In this thesis, new and novel PWM and control strategies are proposed and investigated for reducing current harmonics, compensating inverter nonlinearity, eliminating CMV variation, and maximising operation range in both isolated and common DC-bus OW-PMSM drives.

In the isolated DC-bus OW drive, many control performances that are related to PWM should be considered, such as

- ✓ Current harmonics
- ✓ Capacitor overcharging issues
- ✓ CMV variation control
- ✓ Fault tolerant control

The isolated DC-bus OW drive has the advantages of multilevel output voltages, larger voltage utilization, and lower control complexity, compared with other OW topologies, i.e. common DC-bus and floating capacitor topologies. Due to abundantly available vectors in the isolated DC-bus topology, SPWMs with easy implementation and low computation burden are preferable compared with SVPWMs, and are used in Chapters 2-4.

In the common DC-bus OW drive, PWM can affect many control performances, such as

- ✓ ZSC control
- ✓ Current harmonics
- ✓ Flux weakening control
- ✓ Sensorless control
- ✓ CMV variation control
- ✓ Fault tolerant control

The common DC-bus OW drive has the advantages of controllable ZSC, better fault tolerant

capability, and lower cost compared with other OW topologies. The ZSC control is necessary and limits the utilization of vectors in the common DC-bus topology, so that SVPWMs are preferable for the switching pattern optimization due to visible voltage vectors, vector durations, and vector action sequences compared with SPWMs, and are used in Chapters 5-7.

## 8.1 PWM and Control Strategies for Isolated DC-bus OW-PMSM Drive

Fig. 8.1 shows the summary of PWM and control strategies for the isolated DC-bus OW-PMSM drive in Chapters 2-4.

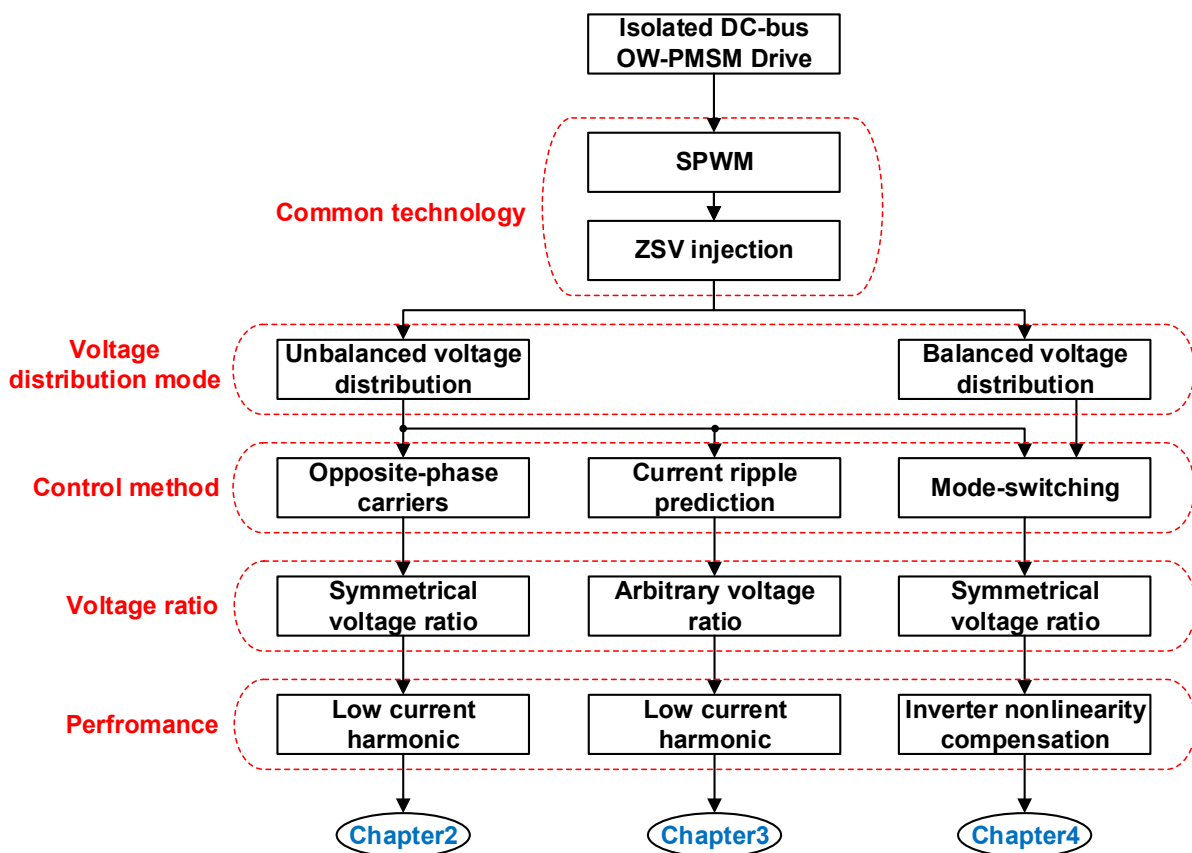


Fig. 8.1 PWM and control strategies for the isolated DC-bus OW-PMSM drive.

All three chapters are based on SPWM strategies with ZSV injection. The high control freedom of SPWM strategies can be utilized for current harmonic reduction, by opposite-phase carriers, switching pattern enumeration, and mode-switching of voltage distributions. The unbalanced voltage distribution is used in Chapters 2 and 3 to reduce the switching frequency and PWM induced current harmonics. The different inverter nonlinearity characteristics of balanced and unbalanced voltage distributions are utilized for the inverter nonlinearity compensation in Chapter 4.

## 1. SPWM strategy for symmetrical DC-bus voltage ratio

Chapter 2 proposed SPWM strategies with ZSV injection, unbalanced voltage distribution, and opposite-phase carriers to reduce switching frequency and PWM induced current harmonics for the isolated DC-bus OW drive with a symmetrical DC-bus voltage ratio. Two different ZSVs are introduced in Chapter 2 corresponding to two proposed SPWM strategies with different numbers of switching actions in a PWM cycle. Table 8.1 shows the comparison of conventional and proposed PWMs with the same switching loss.

Table 8.1 Comparison of Conventional and Proposed PWMs with the Same Switching Loss

PWM strategy	Switching actions in a PWM cycle	Switching actions during sector change in an electrical cycle	Current harmonics	Sector and vector duration calculation
SPWM [SEK11]	12	0	Large	No
SPWM [SEK13]	8	0	Medium	No
SHCPWM [SRI13]	6	12	Low	Yes
Proposed SPWM1 (Chapter 2)	6	6	Low	No
Proposed SPWM2 (Chapter 2)	4	6	Low	No

Current harmonics and the number of switching actions in a PWM cycle can be reduced in the proposed SPWM strategies, compared with those in the conventional SPWM strategies. Compared with the SHCPWM strategy, the proposed SPWM strategies show advantages of easy implementation and half switching actions during sector change, without the deterioration of current harmonics. The proposed SPWM strategies can combine the synergies of easy implementation in conventional SPWM strategies and low current harmonics in SHCPWM strategies, while maintain other good control performances, such as balanced operation of two inverters, less switching actions in a PWM cycle and during sector change.

## 2. SPWM strategy for arbitrary DC-bus voltage ratio

For an isolated DC-bus OW drive with an arbitrary DC-bus voltage ratio, the generalized PWM strategy has the advantage of wider applicability. However, since the space vector plane changes with DC-bus voltage ratios, current harmonics could not be minimized in conventional methods with the non-optimal selection of switching combinations. Chapter 3 proposed a generalized SPWM strategy with the optimal combination of ZSV injection and unbalanced voltage distribution between two inverters. A current ripple prediction model of the OW drive is developed to predict the PWM induced current ripples in each control cycle, which are subsequently used for determining the optimal combination of ZSV injection and voltage distribution. The proposed SPWM can solve the conflict between the generalized modulation strategy and the minimum current harmonics in an OW drive with arbitrary DC-bus voltage ratios. Compared with the conventional generalized SVPWM strategy [HUA19b] under the same switching loss, the proposed SPWM has lower current harmonics in all DC-bus voltage ratios, and the better performance is more obvious in unequal DC-bus voltage ratios. For DC-bus voltage ratios of 1:2 and 2:1, 1:3 and 3:1, the proposed method has the same current harmonics due to the symmetrical structure of two inverters in an OW drive, and solves the issue of different harmonic characteristics in the conventional method. Moreover, the overcharge of capacitors can be avoided by a simplified capacitor voltage control method.

## 3. Inverter nonlinearity compensation

A novel inverter nonlinearity compensation method is proposed in Chapter 4 for an isolated DC-bus OW drive with a symmetrical DC-bus voltage ratio based on balanced and unbalanced voltage distributions. Inverter nonlinearity of dual two-level OW inverters is analysed in both balanced and unbalanced voltage distributions for the first time, and the different voltage distortions are utilized for a close loop inverter nonlinearity compensation by alternately applying the two voltage distributions. Thus, inverter nonlinearity induced harmonics can be reduced and accurate compensation voltages can be acquired. Table 8.2 shows the comparison of offline, current harmonic-based and proposed inverter nonlinearity compensation methods. The proposed inverter nonlinearity compensation method needs no offline measurement for the parameters of the dual OW inverters, and can maintain a high compensation accuracy with the variation of inverter parameters in different operation conditions. As a result, the proposed method shows higher robustness compared with off-line methods. Moreover, the proposed method can overcome the issues in current harmonic-based methods, such as the need of

accurate rotor position and pre-set compensation voltage curves, slow convergence speed, as well as compensation accuracy affected by non-ideal BEMF harmonics.

Table 8.2 Comparison of Inverter Nonlinearity Compensation Methods

Methods	Convergence speed	Robustness	Affected by BEMF harmonics	Need of pre-set curves	Need of accurate rotor position
Offline	High	Low	No	Yes	No
Current harmonic-based	Low	Medium	Yes	Yes	Yes
Proposed (Chapter 4)	High	High	No	No	No

## 8.2 PWM and Control Strategies for Common DC-bus OW-PMSM Drive

Fig. 8.2 summarises the PWM and control strategies for the common DC-bus OW-PMSM drive in Chapters 5-7. The ZSC control can limit the available switching combinations and their durations in the common DC-bus OW-PMSM drive. The available switching combinations depend on the sign of the reference ZSV, and durations of switching combinations are determined by not only the reference voltage vector in the  $\alpha\beta$  space vector plane but also the reference ZSV in the zero sequence axis. The proposed three methods in Chapters 5, 6, and 7, respectively, are all based on switching pattern optimization of SVPWM for ZSC control under different objectives, i.e. low current harmonics, CMV variation elimination, and maximum operation range.

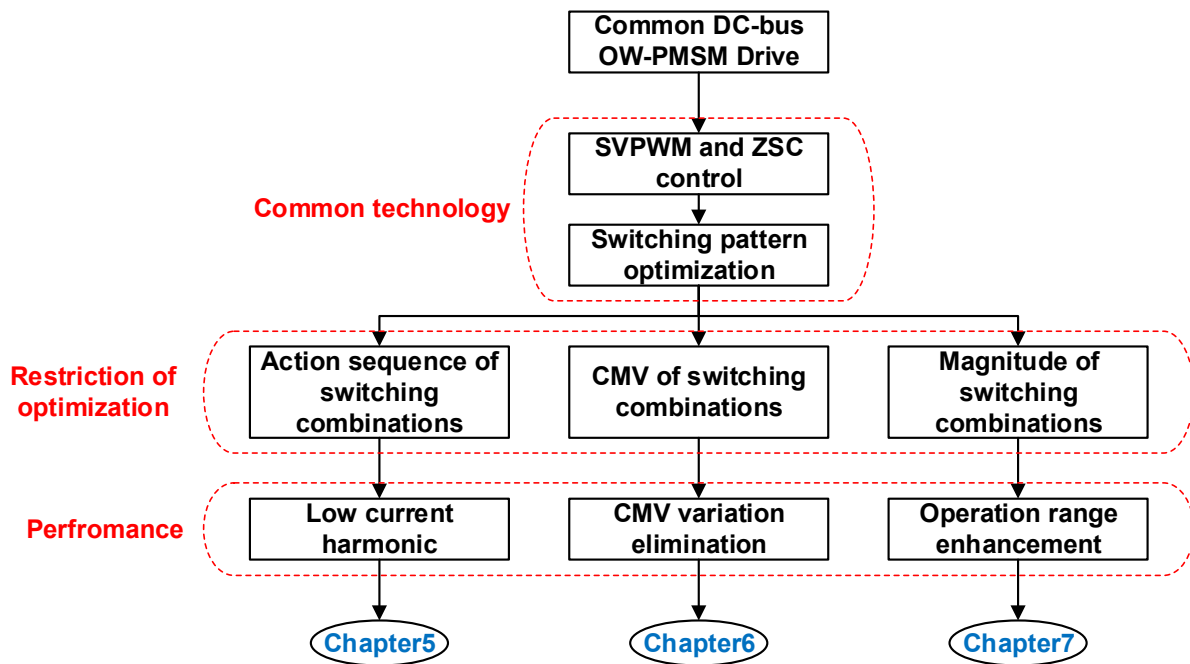


Fig. 8.2 PWM and control strategies for the common DC-bus OW-PMSM drive.

### 1. Action sequence optimization of switching combinations

For a common DC-bus OW drive, the switching pattern optimization in Chapter 5 aims to optimize the switching combinations and their action sequence for both the ZSC suppression and current harmonic reduction. A novel SVPWM strategy is proposed, and each of six sectors is further divided into three sub-sectors in the space vector plane, in which the optimal switching combinations and their action sequence are found to be different. Consequently, different switching combinations and their action sequences are employed in three sub-sectors to significantly reduce current harmonics. Furthermore, a closed-loop ZSC control of the proposed SVPWM strategy is introduced to suppress ZSC. Table 8.3 shows the comparison of the proposed and existing PWM and ZSC control methods. Compared with hardware methods, the proposed SVPWM with a software ZSC control method has the advantage of low cost and can generate a controllable ZSV for the ZSC control of an OW-PMSM with triplen BEMF harmonics. Compared with conventional PWM strategies with the symmetrical action sequence of switching combinations, the proposed SVPWM shows low current harmonics in the high-frequency region. Moreover, the proposed SVPWM can eliminate the low-frequency current harmonics induced by the conventional SVPWM with the asymmetric action sequence of switching combinations.

Table 8.3 Comparison of PWM and ZSC control methods

ZSC suppression methods		Action sequence of switching combinations	Current harmonics		Applicable for OW-PMSM with triplen BEMF harmonics
			Low-frequency	High-frequency	
Hardware	[SOM02]	Symmetrical	Low	Low	No
	[SOM04]				
Software	[SRI14]		Low	Large	No
	[BAI04]		Low	Medium	No
	[ZHO15]		Low	Large	Yes
	[AN16]				
	[LIN19]		Low	Large	Yes
	[ZHA17a]		Low	Medium	Yes
	[SHE19]	Asymmetric	Large	Low	Yes
Proposed SVPWM (Chapter 5)	Action sequence optimization	Low	Low	Yes	

## 2. CMV variation elimination

To eliminate the negative effect of CMV and reduce ZSC harmonics in an OW-PMSM drive, the switching pattern optimization should be applied for both the ZSC suppression and CMV variation elimination. Chapter 6 proposed a novel SVPWM strategy utilizing switching combinations with the same CMV for eliminating CMV variation, and then switching combinations are further selected with different ZSVs for ZSC control. Switching

combinations in the dual inverters are categorized into groups according to their CMVs, and the group with  $V_{dc}/3$  CMV can be used for CMV variation elimination. Then, switching combinations are further selected from the group according to their ZSVs and the reference ZSV for the control of ZSC in the proposed SVPWM strategy. Thus, the control of CMV and ZSC can be achieved simultaneously. The conventional CMV control can usually limit the utilization of switching combinations and may induce large high-frequency ZSC harmonics, while the proposed SVPWM can minimize the effect of the CMV control on the ZSC control. Compared with the conventional CMVE-PWM [HU21], the proposed SVPWM can reduce the switching loss by 1/6, and significantly reduce high-frequency ZSC harmonics. Moreover, in the over modulation region, the proposed SVPWM can reduce both low and high-frequency ZSC harmonics and solve the problem of uncontrolled ZSC in the conventional CMVE-PWM.

### 3. Operation range enhancement

To extend the operation range of a common DC-bus OW-PMSM drive, the switching pattern optimization should be applied for both suppressing ZSC and maximizing the modulation region. The proposed SVPWM in Chapter 7 can achieve the ZSC control and extend the operation range by considering voltages in zero sequence axis and voltage vectors in  $\alpha\beta$ -plane, both of which are mapped by switching combinations in an OW drive. To suppress ZSC in an OW-PMSM fed by common DC-bus dual inverters, switching combinations with non-null ZSV should be used for generating a controllable ZSV to counteract with other ZSVs. The effect of switching combinations with non-null ZSV on the modulation region of a common-DC bus OW-PMSM drive is investigated for the first time. The proposed SVPWM has the optimal selection of non-null ZSV switching combinations on the large hexagon in the space vector plane, compared with the conventional SVPWM [ZHA17a] which uses the non-null ZSV switching combinations on the small hexagon. The proposed SVPWM has a similar control performance as the conventional SVPWM in the linear modulation region, but has a higher speed with the same torque or a larger torque with the same speed in the over modulation region. The proposed SVPWM can extend the operation range over 10% compared with the conventional SVPWM, and the superiority of the proposed method increases with the speed rise.

## 8.3 Future Work

For an isolated DC-bus OW drive with an arbitrary DC-bus voltage ratio, the combination of



ZSV injection and voltage distribution in SPWM can be optimized for various control performance improvement. In this thesis, only the PWM induced current harmonics are considered in Chapter 3, and other control performances such as CMV variation reduction and DC-bus current ripple suppression can be studied in the future. Moreover, the multi-objective optimization can also be achieved by introducing weighting factors in the cost function.

The inverter nonlinearity effect on output voltages can be affected by PWM strategies of an inverter. The different voltage distortions of two voltage distribution modes are utilized in Chapter 4 for the inverter nonlinearity compensation. This concept can be expanded to other electrical machine drive topologies, such as the conventional three phase machine fed by a two-level or multilevel inverter and the dual three phase machine fed by two inverters.

SVPWM strategies are used in this thesis for the common DC-bus topology due to the visible vectors, vector sequences, and vector durations, which are convenient for the switching pattern optimization. In Chapters 5-7, switching pattern optimizations are used to improve control performances including current harmonic reduction, CMV variation elimination, and operation range enhancement. Other control performances such as DC-bus current ripple suppression and current harmonic reduction in low carrier ratio operation can be studied in the future.

The research in this thesis is about the isolated and common DC-bus OW topologies, but some of the research results can be applied to the floating capacitor topology, such as SPWM with easy implementation, PWM induced current harmonic reduction, switching pattern optimization, and CMV control.

## REFERENCES

- [AGH19] A. Aghazadeh, M. Jafari, N. Khodabakhshi-Javinani, H. Nafisi, and H. Jabbari Namvar, "Introduction and advantage of space opposite vectors modulation utilized in dual two-level inverters with isolated DC sources," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 10, pp. 7581-7592, Oct. 2019.
- [AN14] Q. An, M. H. Duan, L. Sun, and G. L. Wang, "SVPWM strategy of post-fault reconfigured dual inverter in open-end winding motor drive systems," *Electronics Letters*, vol. 50, no. 17, pp. 1238-1240, Aug. 2014.
- [AN16] Q. An, J. Liu, Z. Peng, L. Sun, and L. Sun, "Dual-space vector control of open-end winding permanent magnet synchronous motor drive fed by dual inverter," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8329-8342, Dec. 2016.
- [BAI04] M. R. Baiju, K. K. Mohaoatra, R. S. Kanchan, and K. Gopakumar, "A dual two-level inverter scheme with common mode voltage elimination for an induction motor drive," *IEEE Transactions on Power Electronics*, vol. 19, no. 3, pp. 794-805, May 2004.
- [BAR15] R. Baranwal, K. Basu, and N. Mohan, "Carrier-based implementation of SVPWM for dual two-level VSI and dual matrix converter with zero common-mode voltage," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1471-1487, Mar. 2015.
- [CHE17] M. Chen and D. Sun, "A unified space vector pulse width modulation for dual two-level inverter system," *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 889-893, Feb. 2017.
- [CHO13] B. Cho, J. Ha, and S. Sul, "Analysis of the phase current measurement boundary of three shunt sensing PWM inverters and an expansion method", *Journal of Power Electronics*, vol. 13, no. 2, pp. 232-242, Mar. 2013.
- [CHO16] S. Chowdhury, P. W. Wheeler, C. Patel, and C. Gerada, "A multilevel converter with a floating bridge for open-end winding motor drive applications," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 9, pp. 5366-5375, Sept. 2016.

- [CHO96] J.W. Choi and S.K. Sul, "Inverter output voltage synthesis using novel dead time compensation," *IEEE Transactions on Power Electronics*, vol. 11, no. 2, pp. 221-227, Mar. 1996.
- [DAR17] M. Darijevic, M. Jones, O. Dordevic, and E. Levi, "Decoupled PWM control of a dual-inverter four-level five-phase drive," *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 3719-3730, May 2017.
- [ELR14] A. M. EL-Refaie, J.P. Alexander, S. Galioto, P.B. Reddy, K. Huh, P. de Bock, and X. Shen, "Advanced high-power-density interior permanent magnet motor for traction applications," *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3235-3248, Sep./Oct. 2014.
- [HEN10] J. R. Hendershort Jr. and T. J. E. Miller, *Design of Brushless PermanentMagnet Machines*. Venice, FL: Motor Design Books, 2010, pp. 693-694.
- [HU19] W. Hu, H. Nian, and D. Sun, "Zero-sequence current suppression strategy with reduced switching frequency for open-end winding PMSM drives with common DC bus," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 10, pp. 7613-7623, Oct. 2019.
- [HU20] W. Hu, C. Ruan, H. Nian, and D. Sun, "An improved modulation technique with minimum switching actions within one PWM cycle for open-end winding PMSM system with isolated DC bus," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 5, pp. 4259-4264, May 2020.
- [HU21] W. Hu, C. Ruan, H. Nian, and D. Sun, "Zero-sequence current suppression strategy with common-mode voltage control for open-end winding PMSM drives with common DC bus," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 6, pp. 4691-4702, Jun. 2021.
- [HUA19a] Z. Huang, T. Yang, P. Giangrande, S. Chowdhury, M. Galea, and P. Wheeler, "An active modulation scheme to boost voltage utilization of the dual converter with a floating bridge," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 7, pp. 5623-5633, Jul. 2019.
- [HUA19b] Z. Huang, T. Yang, P. Giangrande, P. Wheeler, and M. Galea, "An enhanced unified space vector modulation technique for dual converters with isolated voltage supplies," *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, Lisbon, Portugal, 2019, pp. 3511-3516.

- [HUA19c] Z. Huang, T. Yang, P. Giangrande, P. Wheeler, and M. Galea, "An active modulation scheme for avoiding overcharging in the dual converter with isolated asymmetric supplies," 2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), 2019, pp. 1-9.
- [HUA21] Z. Huang, T. Yang, P. Giangrande, S. Chowdhury, M. Galea, and P. Wheeler, "Enhanced performance of dual inverter with a floating capacitor for motor drive applications," *IEEE Transactions on Power Electronics*, vol. 36, no. 6, pp. 6903-6916, Jun. 2021.
- [HUA22] Z. Huang, T. Yang, P. Giangrande, M. Galea, and P. Wheeler, "Technical review of dual inverter topologies for more electric aircraft applications," *IEEE Transactions on Transportation Electrification*, vol. 8, no. 2, pp. 1966-1980, Jun. 2022.
- [IQB09] A. Iqbal and S. Moinuddin, "Comprehensive relationship between carrier-based PWM and space vector PWM in a five-phase VSI," *IEEE Transactions on Power Electronics*, vol. 24, no. 10, pp. 2379-2390, Oct. 2009.
- [JIA13] D. Jiang and F. Wang, "Variable switching frequency PWM for three-phase converters based on current ripple prediction," *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 4951-4961, Nov. 2013.
- [JIA14] D. Jiang and F. Wang, "Current-ripple prediction for three-phase PWM converters," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 1, pp. 531-538, Jan.-Feb. 2014.
- [KAL15] J. Kalaiselvi and S. Srinivas, "Bearing currents and shaft voltage reduction in dual-inverter-fed open-end winding induction motor with reduced CMV PWM methods," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 144-152, Jan. 2015.
- [KAZ98] M. P. Kazmierkowski and L. Malesani, "Current control techniques for three-phase voltage-source PWM converters: a survey," *IEEE Transactions on Industrial Electronics*, vol. 45, no. 5, pp. 691-703, Oct. 1998.
- [KIA17] A. D. Kiadehi, K. E. K. Drissi, and C. Pasquier, "Voltage THD reduction for dual-inverter fed open-end load with isolated DC sources," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 3, pp. 2102-2111, Mar. 2017.
- [KIM04] J. Kim, J. Jung, and K. Nam, "Dual-inverter control strategy for high-speed operation of EV induction motors," *IEEE Transactions on Industrial Electronics*, vol. 51, no. 2, pp. 312-320, Apr. 2004.

- [KIM06] H.W. Kim, M.Y. Youn, K.Y. Cho, and H.S. Kim, "Nonlinearity estimation and compensation of PWM VSI for PMSM under resistance and flux linkage uncertainty," *IEEE Transactions on Control Systems Technology*, vol. 14, no. 4, pp. 589-601, Jul. 2006.
- [KUP15] A. Kuperman, "Proportional-resonant current controllers design based on desired transient performance," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5341-5345, Oct. 2015.
- [LEE21] J. H. Lee and S. K. Sul, "Inverter nonlinearity compensation through dead time effect estimation," *IEEE Transactions on Power Electronics*, vol. 36, no. 9, pp. 10684-10694, Sept. 2021.
- [LI18] Q. Li and D. Jiang, "Variable switching frequency PWM strategy of two-level rectifier for DC-link voltage ripple control," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 7193-7202, Aug. 2018.
- [LI19] A. Li, Z. Gao, D. Jiang, W. Kong, and R. Qu, "Drive system with asymmetrical power electronics devices for novel reluctance machines with dc-biased sinusoidal current," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 4, pp. 2303-2313, Dec. 2019.
- [LIN19] X. Lin, W. Huang, and L. Wang, "SVPWM strategy based on the hysteresis controller of zero-sequence current for three-phase open-end winding PMSM," *IEEE Transactions on Power Electronics*, vol. 34, no. 4, pp. 3474-3486, Apr. 2019.
- [LIU14] K. Liu and Z. Q. Zhu, "Online estimation of the rotor flux linkage and voltage-source inverter nonlinearity in permanent magnet synchronous machine drives," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 418-427, Jan. 2014.
- [LIU21] C. Liu and J. Shang, "Sensorless drive strategy of open-end winding PMSM With zero-sequence current suppression," *IEEE Transactions on Energy Conversion*, vol. 36, no. 4, pp. 2987-2997.
- [LOH03] Poh Chiang Loh, D. G. Holmes, Y. Fukuta, and T. A. Lipo, "Reduced common-mode modulation strategies for cascaded multilevel inverters," *IEEE Transactions on Industry Applications*, vol. 39, no. 5, pp. 1386-1395, Sept.-Oct. 2003.
- [MAJ21] M. Ghosh Majumder, R. R. K. Gopakumar, L. Umanand, K. Al-Haddad, and W. Jarzyna, "A fault-tolerant five-level inverter topology with reduced

- component count for OEIM drives,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 1, pp. 961-969, Feb. 2021.
- [MOH03] K. K. Mohapatra, K. Gopakumar, V. T. Somasekhar, and L. Umanand, “A harmonic elimination and suppression scheme for an open-end winding induction motor drive,” *IEEE Transactions on Industrial Electronics*, vol. 50, no. 6, pp. 1187-1198, Dec. 2003.
- [NIA19] H. Nian and W. Hu, “A sensorless drive strategy for open-end winding PMSM with common DC voltage based on lower switching frequency,” *IEEE Transactions on Energy Conversion*, vol. 34, no. 3, pp. 1553-1562, Sept. 2019.
- [PAR12] Y. Park and S. Sul, “A novel method utilizing trapezoidal voltage to compensate for inverter nonlinearity,” *IEEE Transactions on Power Electronics*, vol. 27, no. 12, pp. 4837-4846, Dec. 2012.
- [PAR14] D. Park and K. Kim, “Parameter-Independent Online Compensation Scheme for Dead Time and Inverter Nonlinearity in IPMSM Drive Through Waveform Analysis,” *IEEE Transactions on Industrial Electronics*, vol. 61, no. 2, pp. 701-707, Feb. 2014.
- [PEL10] G. Pellegrino, R. I. Bojoi, P. Guglielmi, and F. Cupertino, “Accurate inverter error compensation and related self-commissioning scheme in sensorless induction motor drives,” *IEEE Transactions on Industry Applications*, vol. 46, no. 5, pp. 1970-1978, Sept.-Oct. 2010.
- [PER13] J. Pereda and J. Dixon, “Cascaded multilevel converters: optimal asymmetries and floating capacitor control,” *IEEE Transactions on Industrial Electronics*, vol. 60, no. 11, pp. 4784-4793, Nov. 2013.
- [PIR17] V. F. Pires, D. Foito, and J. F. Silva, “Fault-tolerant multilevel topology based on three-phase H-bridge inverters for open-end winding induction motor drives,” *IEEE Transactions on Energy Conversion*, vol. 32, no. 3, pp. 895-902, Sept. 2017.
- [POU12] J. Pou, J. Zaragoza, S. Ceballos, M. Saedifard, and D. Boroyevich, “A carrier-based PWM strategy with zero-sequence voltage injection for a three-level neutral-point-clamped converter,” *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 642-651, Feb. 2012.
- [RED11] B. Venugopal Reddy, V. T. Somasekhar, and Y. Kalyan, “Decoupled space-vector PWM strategies for a four-level asymmetrical open-end winding

- induction motor drive with waveform symmetries,” *IEEE Transactions on Industrial Electronics*, vol. 58, no. 11, pp. 5130-5141, Nov. 2011.
- [RED18] M. H. V. Reddy, T. B. Reddy, B. R. Reddy, and M. S. Kalavathi, “Discontinuous PWM Technique for the Asymmetrical Dual Inverter Configuration to Eliminate the Overcharging of DC-Link Capacitor,” *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 156-166, Jan. 2018.
- [RES12] J. A. Restrepo, A. Berzoy, A. E. Ginart, J. M. Aller, R. G. Harley, and T. G. Habetler, “Switching strategies for fault tolerant operation of single DC-link dual converters,” *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 509-518, Feb. 2012.
- [SAN13] A. P. Sandulescu, F. Meinguet, X. Kestelyn, E. Semail, and A. Bruyere, “Flux-weakening operation of open-end winding drive integrating a cost-effective high-power charger,” *IET Electrical Systems in Transportation*, vol. 3, no. 1, pp. 10–21, Mar. 2013.
- [SAN14] P. Sandulescu, F. Meinguet, X. Kestelyn, E. Semail, and A. Bruyère, “Control strategies for open-end winding drives operating in the flux-weakening region,” *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4829-4842, Sept. 2014.
- [SEK11] K. R. Sekhar and S. Srinivas, “Current ripple analysis in a decoupled SVPWM controlled dual two-level inverter fed open-end winding induction motor drive,” 2011 2nd Power Electronics, Drive Systems and Technologies Conference, Tehran, 2011, pp. 373-378.
- [SEK13] K. R. Sekhar and S. Srinivas, “Discontinuous decoupled pwms for reduced current ripple in a dual two-level inverter fed open-end winding induction motor drive,” *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2493-2502, May 2013.
- [SEK18] K. R. Sekhar and S. Srinivas, “Torque ripple reduction PWMs for a single DC source powered dual-inverter fed open-end winding induction motor drive,” *IET Power Electronics*, vol. 11, no. 1, pp. 43-51, Jan. 2018.
- [SHE19] Z. Shen, D. Jiang, L. Zhu, Y. Xu, T. Zou, Z. Liu, and R. Qu, “A novel zero-sequence current elimination PWM scheme for an open-winding PMSM with common dc bus,” *IEEE Transactions on Power Electronics*, vol. 34, no. 12, pp. 12476-12490, Dec. 2019.

- [SHI01] E. G. Shivakumar, K. Gopakumar, S. K. Sinha, A. Pittet, and V. T. Ranganathan, "Space vector PWM control of dual inverter fed open-end winding induction motor drive," *Proc. IEEE Annu. Appl. Powe. Electron. Conf. Expos.*, 2001, pp. 399-405.
- [SOM02a] V. T. Somasekhar, K. Gopakumar, A. Pittet, and V. T. Ranganathan, "PWM inverter switching strategy for a dual two-level inverter fed open-end winding induction motor drive with a switched neutral," *IEE Proceedings-Electric Power Applications*, vol. 149, no. 2, pp. 152-160, Mar. 2002.
- [SOM02b] V. Somasekhar, E. Shivakumar, K. Gopakumar, and A. Pittet, "Multi level voltage space phasor generation for an open-end winding induction motor drive using a dual inverter scheme with asymmetrical DClink voltages," *EPE Journal*, vol. 12, no. 3, pp. 59-77, 2002.
- [SOM04] V. T. Somasekhar, K. Gopakumar, and M. R. Baiju, "Dual two-level inverter scheme for an open-end winding induction motor drive with a single DC power supply and improved DC bus utilisation," *IEE Proceedings - Electric Power Applications*, vol. 151, no. 2, pp. 230-238, Mar. 2004.
- [SOM08a] V. T. Somasekhar, S. Srinivas, and K. K. Kumar, "Effect of zero-vector placement in a dual-inverter fed open-end winding induction-motor drive with a decoupled space-vector PWM strategy," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 6, pp. 2497-2505, Oct. 2008.
- [SOM08b] V.T. Somasekhar, S. Srinivas, and K.K. Kumar, "Effect of zero-vector placement in a dual-inverter fed open-end winding induction motor drive with alternate sub-hexagonal center PWM switching scheme," *IEEE Transactions on Power Electronics*, vol. 23, no.3, pp. 1584-1591, 2008.
- [SOM13] A. Somani, R. K. Gupta, K. K. Mohapatra, and N. Mohan, "On the causes of circulating currents in PWM drives with open-end winding AC machines," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 9, pp. 3670-3678, Sept. 2013.
- [SRI08] S. Srinivas and V. T. Somasekhar, "Space-vector-based PWM switching strategies for a three-level dual-inverter-fed open-end winding induction motor drive and their comparative evaluation," *IET Proc. Electric Power Applications*, vol. 2, no. 1, pp. 19-31, Jan. 2008.
- [SRI10] P. Srinivasan, B. Venugopal Reddy, and V. T. Somasekhar, "PWM switching strategy for the elimination of common mode voltage of a two-level inverter



- drive with an open-end winding induction motor configuration,” 2010 Joint International Conference on Power Electronics, Drives and Energy Systems & 2010 Power India, New Delhi, 2010, pp. 1-6.
- [SRI13] S. Srinivas and K. Ramachandra Sekhar, “Theoretical and experimental analysis for current in a dual-inverter-fed open-end winding induction motor drive with reduced switching PWM,” *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 4318-4328, Oct. 2013.
- [SRI14] S. Srinivas and J. Kalaiselvi, “Pulse width modulation schemes enabling single DC power source driven dual two-level voltage source inverter with single voltage source inverter switching,” *IET Power Electronics*, vol. 7, no. 5, pp. 1181-1191, May 2014.
- [SRI15] P. Srinivasan, B. L. Narasimharaju, and N. V. Srikanth, “Space-vector pulse width modulation scheme for open-end winding induction motor drive configuration,” *IET Power Electronics*, vol. 8, no. 7, pp. 1083-1094, Jul. 2015.
- [SUK91] T. Sukegawa, K. Kamiyama, K. Mizuno, T. Matsui, and T. Okuyama, “Fully digital, vector-controlled PWM VSI-fed AC drives with an inverter dead-time compensation strategy,” *IEEE Transactions on Industry Applications*, vol. 27, no. 3, pp. 552-559, May.-Jun. 1991.
- [WAN11] Y. Wang, t. A. Lipo and D. Pan, “Robust operation of double-output AC machine drive,” 8th international conference on power electronics - ecce asia, Jeju, 2011, pp. 140-144.
- [WAN18] Y. Wang, W. Xie, X. Wang, and D. Gerling, “A precise voltage distortion compensation strategy for voltage source inverters,” *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 59-66, Jan. 2018.
- [WAN19] Chao Wang, “Novel flux-weakening control of permanent magnet synchronous machines with particular reference to stability issues”, PhD Thesis, Department of Electronic and Electrical Engineering, University of Sheffield, 2019.
- [WEL03] B. A. Welchko and J. M. Nagashima, “The influence of topology selection on the design of EV/HEV propulsion systems,” *IEEE Power Electronics Letters*, vol. 1, no. 2, pp. 36-40, Jun. 2003.
- [WEL03] B. A. Welchko and J. M. Nagashima, “The influence of topology selection on the design of EV/HEV propulsion systems,” *IEEE Transactions on Power Electronics Letters*, vol. 1, no. 2, pp. 36-40, Jun. 2003

- [YAN15] F. Yang, A. R. Taylor, H. Bai, B. Cheng, and A. A. Khan, "Using d–q transformation to vary the switching frequency for interior permanent magnet synchronous motor drive systems," *IEEE Transactions on Transportation Electrification*, vol. 1, no. 3, pp. 277-286, Oct. 2015.
- [YE20] D. Ye, D. Jiang, and J. Chen, "Variable switching sequence PWM strategy of dual three-phase machine drive for high-frequency current harmonic suppression," *IEEE Transactions on Power Electronics*, vol. 35, no. 5, pp. 4984-4995, May 2020.
- [YU19] Z. Yu, W. Kong, D. Jiang, R. Qu, D. Li, S. Jia, J. Sun, and C. Gan, "Fault-tolerant control strategy of the open-winding inverter for dc-biased vernier reluctance machines," *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1658-1671, Feb. 2019.
- [YU20] Z. Yu, C. Gan, Y. Chen, and R. Qu, "DC-biased sinusoidal current excited switched reluctance motor drives based on flux modulation principle," *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 10614-10628, Oct. 2020.
- [ZHA04] H. Zhao, Q. M. J. Wu, and A. Kawamura, "An accurate approach of nonlinearity compensation for VSI inverter output voltage," *IEEE Transactions on Power Electronics*, vol. 19, no. 4, pp. 1029-1035, Jul. 2004.
- [ZHA16] H. Zhan, Z. Q. Zhu, M. Odavic, and Y. Li, "A novel zero sequence model based sensorless method for open-winding PMSM with common DC bus," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 6777-6789, Dec. 2016.
- [ZHA17a] H. Zhan, Z. Q. Zhu, and M. Odavic, "Analysis and suppression of zero sequence circulating current in open winding permanent magnet synchronous machine drives with common DC bus," *IEEE Transactions on Industry Applications*, vol. 53, no. 4, pp. 3609-3620, Mar. 2017.
- [ZHA17b] H. Zhan, Z. Q. Zhu, and M. Odavic, "Nonparametric sensorless drive method for open-winding PMSM based on zero-sequence back EMF with circulating current suppression," *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 3808-3817, May 2017.
- [ZHA17c] Z. Zhang, D. Leggate, and T. Matsuo, "Industrial inverter current sensing with three shunt resistors: limitations and solutions," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4577-4586, Jun. 2017.

- [ZHA18a] W. Zhao, Z. Chen, D. Xu, J. Ji, and P. Zhao, "Unity power factor fault-tolerant control of linear permanent-magnet vernier motor fed by a floating bridge multilevel inverter with switch fault," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 11, pp. 9113-9123, Nov. 2018.
- [ZHA18b] W. Zhao, B. Wu, Q. Chen, and J. Zhu, "Fault-tolerant direct thrust force control for a dual inverter fed open-end winding linear vernier permanent-magnet motor using improved SVPWM," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 9, pp. 7458-7467, Sept. 2018.
- [ZHO02] K. Zhou and D. Wang, "Relationship between space-vector modulation and three-phase carrier-based PWM: a comprehensive analysis," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 1, pp. 186-196, Feb. 2002.
- [ZHO15] Y. Zhou and H. Nian, "Zero-sequence current suppression strategy of open-winding PMSG system with common DC bus based on zero vector redistribution," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 6, pp. 3399-3408, Jun. 2015.
- [ZHU07] Z. Q. Zhu and D. Howe, "Electrical machines and drives for electric, hybrid, and fuel cell vehicles," *Proceedings of the IEEE*, vol. 95, no. 4, pp. 746-765, Apr. 2007.
- [ZHU16] Z.Q. Zhu, B. Lee, and X. Liu, "Integrated field and armature current control strategy for variable flux reluctance machine using open winding," *IEEE Transactions on Industry Applications*, vol. 52, no. 2, pp. 1519-1529, Mar./Apr. 2016.
- [ZHU19] B. Zhu, C. Tan, M. Farshadnia, and J. E. Fletcher, "Postfault zero-sequence current injection for open-circuit diode/switch failure in open-end winding PMSM machines," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 7, pp. 5124-5132, Jul. 2019.

# APPENDIX A THREE-LEG CLAMPING

## SVPWM STRATEGY

Novel SPWM strategies are proposed for the isolated DC-bus OW drive in Chapter 2. Compared with SHCPWM, the proposed SPWMs have the advantages of easy implementation and less switching commutations during sector change. To analyse the proposed SPWMs in the viewpoint of space vectors, the corresponding three-leg clamping SVPWM (TLC-SVPWM) strategy is described in this appendix. TLC-SVPWM has the same switching pattern as the proposed SPWM1 in Chapter 2, but the implementation is much more complex.

The TLC-SVPWM strategy can be derived from SHCPWM strategies, which have been described in Section 1.4.1.1. Taking SHCPWM1 strategy in sector 1 as an example, in which Inverter I is switched, and Inverter II is clamped. The pole voltages of Inverters I and II can be expressed as

$$\begin{aligned} V_{AO} &= \text{duty}_A * V_{dc} & V_{A'O'} &= 0 \\ V_{BO} &= \text{duty}_B * V_{dc} & V_{B'O'} &= V_{dc} \\ V_{CO} &= \text{duty}_C * V_{dc} & V_{C'O'} &= V_{dc} \end{aligned} \quad (\text{A.1})$$

From (1.4) and (A.1), the phase voltages of OW machine are

$$\begin{aligned} V_{AA'} &= V_{AO} - V_{A'O'} + V_{OO'} = \text{duty}_A * V_{dc} + V_{OO'} \\ V_{BB'} &= V_{BO} - V_{B'O'} + V_{OO'} = \text{duty}_B * V_{dc} - V_{dc} + V_{OO'} \\ V_{CC'} &= V_{CO} - V_{C'O'} + V_{OO'} = \text{duty}_C * V_{dc} - V_{dc} + V_{OO'} \end{aligned} \quad (\text{A.2})$$

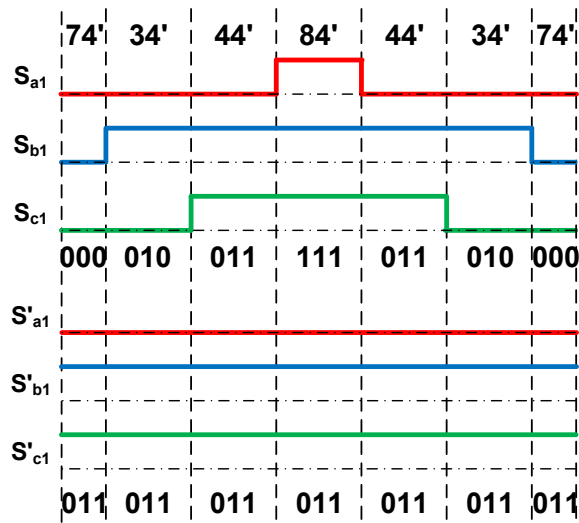
In Fig. A.1 (a), S<sub>b1</sub> and S<sub>c1</sub> are clamped at high voltage level, which means the upper switches should be kept in “on” state and the lower switches are in “off” state. The switching states of switches S<sub>b1</sub> and S<sub>c1</sub>, S<sub>b1</sub> and S<sub>c1</sub> are exchanged in TLC-SVPWM strategy. As a result, S<sub>b1</sub> and S<sub>c1</sub> will be clamped, while S<sub>b1</sub> and S<sub>c1</sub> are switched. To maintain three phase voltages of the OW machine the same as before, three phase voltages can be rewritten as

$$\begin{aligned} V_{AA'} &= \text{duty}_A * V_{dc} - 0 + V_{OO'} \\ V_{BB'} &= 0 - (1 - \text{duty}_B) * V_{dc} + V_{OO'} \\ V_{CC'} &= 0 - (1 - \text{duty}_C) * V_{dc} + V_{OO'} \end{aligned} \quad (\text{A.3})$$

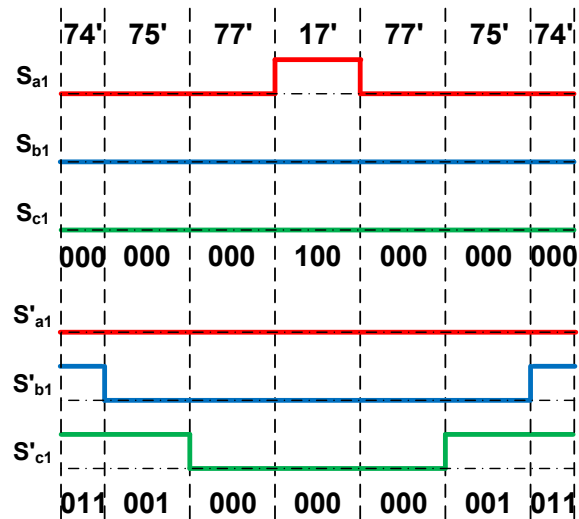
Then, the pole voltages of Inverters I and II can be expressed as

$$\begin{aligned}
V_{AO} &= \text{duty}_A * V_{dc} & V_{A'O'} &= 0 \\
V_{BO} &= 0 & V_{B'O'} &= (1 - \text{duty}_B) * V_{dc} \\
V_{CO} &= 0 & V_{C'O'} &= (1 - \text{duty}_C) * V_{dc}
\end{aligned} \tag{A.4}$$

From (A.4), the PWM waveforms of the proposed TLC-SVPWM strategy can be illustrated, as shown in Fig. A.1 (b). Compared with the PWM waveforms of SHCPWM1 strategy in Fig. A.1 (a), the single inverter clamping is changed to three-leg clamping in the proposed PWM strategy. As a result, the proposed SVPWM strategy is named as three-leg clamping SVPWM strategy in this appendix.



(a) SHCPWM1.



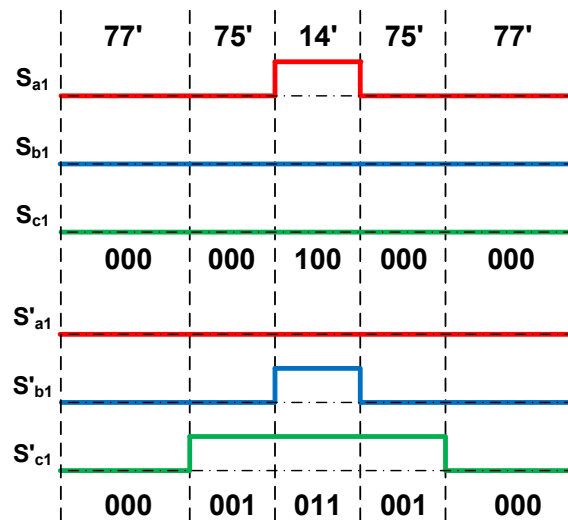
(b) Proposed TLC-SVPWM.

Fig. A.1 PWM waveforms of SHCPWM1 and proposed TLC-SVPWM.

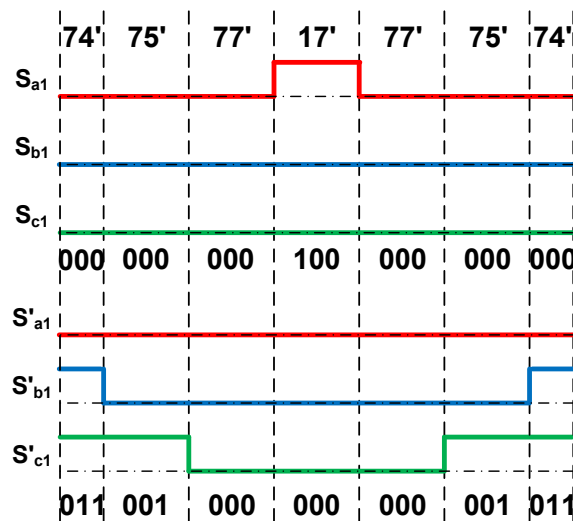
After the exchange of switching states,  $S_{b1}$  and  $S_{c1}$  are clamped on low-level state, and the states of  $S'_{b1}$  and  $S'_{c1}$  become switched, but the switching mode is changed from high level centred to low level centred. As a result, there are opposite-phase carriers in Inverters I and II. The proposed TLC-SVPWM strategy is derived from SHCPWM1 with the exchange of switching states and opposite-phase carriers in Inverters I and II. To evaluate the effect of opposite-phase carriers, the PWM waveforms with and without opposite-phase carriers in sector 1 are shown in Fig. A.2. The reference voltage vector and basic voltage vectors are shown in Fig. A.3. It can be observed that the use of basic voltage vectors is not optimal without opposite-phase carriers, and three nearest basic voltage vectors are used when opposite-phase carriers are applied.

Before and after the exchange of switching states of switches  $S_{b1}$  and  $S'_{b1}$ ,  $S_{c1}$  and  $S'_{c1}$ , the vectors and their action sequences are listed in Table A.1. It can be observed that the two PWM strategies use the same voltage vectors (at the same location in the space vector plane) and the same voltage vector action sequence, and consequently, the current harmonics caused by the two PWM strategies are the same. Moreover, the first and last switching combinations are not changed in TLC-SVPWM and SHCPWM1, so that the number of switching commutations during sector change will be the same as before. As a result, SHCPWM1 and SHCPWM2 strategies can be modified to TLC-SVPWM strategy, keeping the same low commutation times. The exchange of switching states for SHCPWM3 and SHCPWM4 strategies is not described here due to their more commutations. Fig. A.4 shows the exchange of switching states for SHCPWM2. Compared with Fig. A.2 (b), Fig. A.4 (b) has different switching mode. The switching mode of  $S_{a1}$  is changed from high level centred to low level centred, while  $S'_{b1}$  and  $S'_{c1}$  are changed from low level centred to high level centred. However, Fig. A.4 (b) and Fig. A.2 (b) have the same voltage vectors and clamping states. As a result, they are the same PWM strategy.

The TLC-SVPWM in other sectors can be acquired by the same method. PWM waveforms in sectors 1 and 2 of TLC-SVPWM strategy are shown in Fig. A.5. There is only one commutation during sector change. The state of switches in each sector is listed in Table A.2. All switches will be clamped in three sectors and switched in other three sectors through a whole electrical cycle, so that the operation of two inverters is balanced.



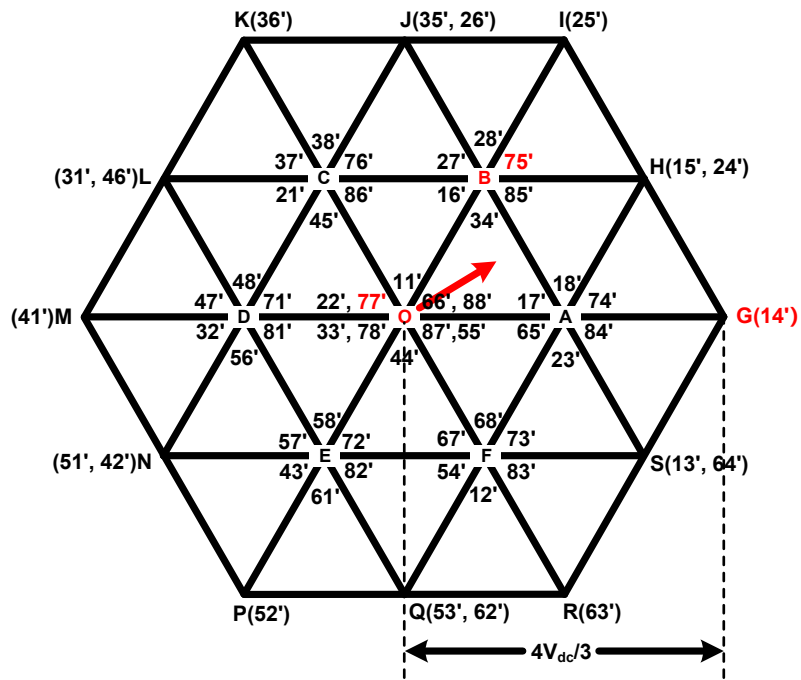
(a) Without opposite-phase carriers.



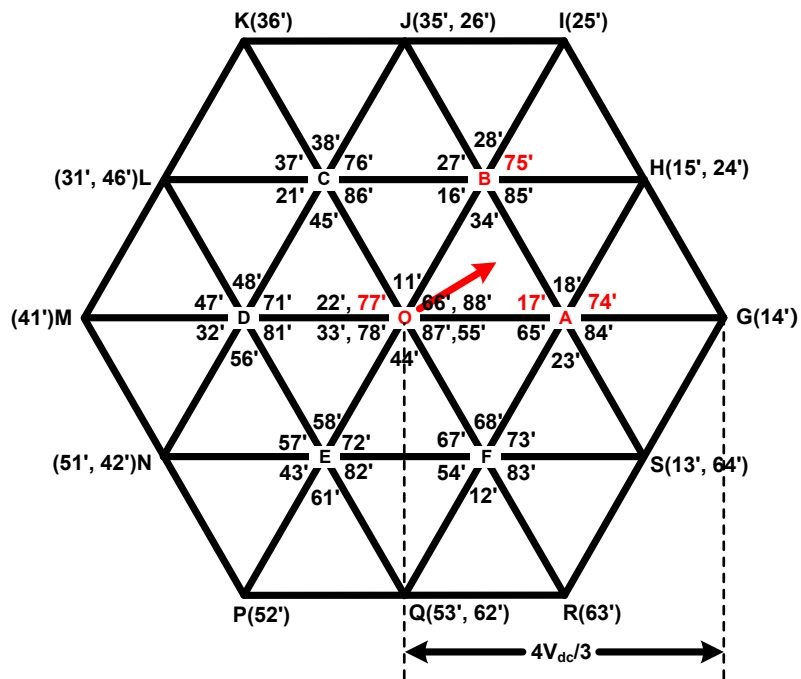
(b) With opposite-phase carriers.

Fig. A.2 PWM waveforms with and without opposite-phase carriers.

The proposed TLC-SVPWM strategy is actually modified from SHCPWM strategy. If an upper switch is clamped in high-level state, then this switch will be changed from clamping mode to switching mode (low level centred), and the duty cycle is complementary to that of the counterpart upper switch in another inverter. At the same time, the counterpart upper switch in another inverter will be changed from switching mode to clamping mode, and is clamped on low-level state. The proposed TLC-SVPWM strategy has the same current harmonics as the SHCPWMs, but can achieve the balanced operation of two inverters compared with SHCPWMs 1 and 2, and reduce switching commutations compared with SHCPWMs 3 and 4. As a result, The proposed TLC-SVPWM strategy can combine the synergies of SHCPWMs.



(a) Without opposite-phase carriers.



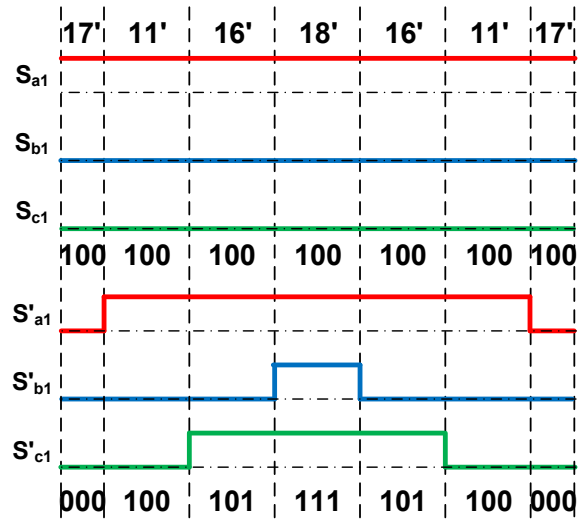
(b) With opposite-phase carriers.

Fig. A.3 Voltage vectors with and without opposite-phase carriers.

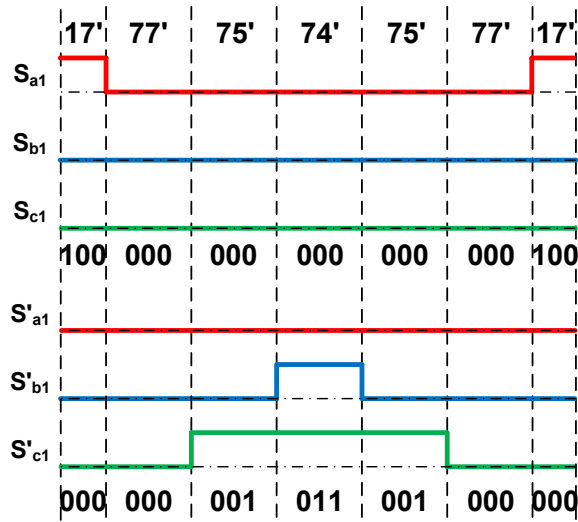
Table A.1 Vectors and Their Action Sequence of SHCPWM1 and TLC-SVPWM Strategy in Sector 1



SHCPWM1	74' (A)	34' (B)	44' (O)	84' (A)	44' (O)	34' (B)	74' (A)
TLC-SVPWM	74' (A)	75' (B)	77' (O)	17' (A)	77' (O)	75' (B)	74' (A)



(a) SHCPWM2.



(b) Proposed TLC-SVPWM.

Fig. A.4 PWM waveforms of SHCPWM2 and proposed TLC-SVPWM strategy.

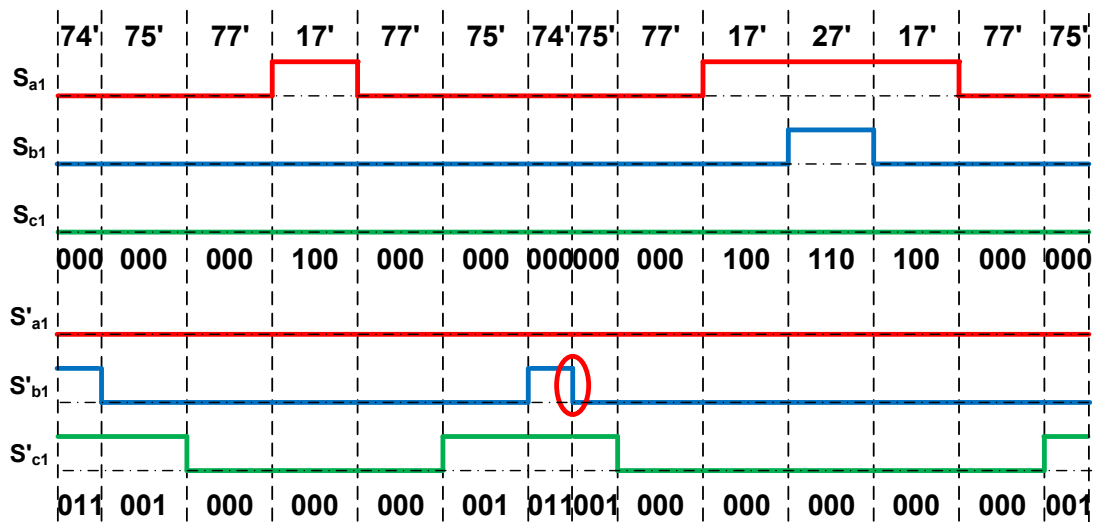


Fig. A.5 Proposed TLC-SVPWM waveforms in sectors 1 and 2.

Table A.2 States of Switches in Each Sector of Proposed TLC-SVPWM Strategy

Sector	1	2	3	4	5	6
$S_{a1}$	S	S	C	C	C	S
$S_{b1}$	C	S	S	S	C	C
$S_{c1}$	C	C	C	S	S	S
$S'_{a1}$	C	C	S	S	S	C
$S'_{b1}$	S	C	C	C	S	S
$S'_{c1}$	S	S	S	C	C	C

Note: C: Clamped S: Switched

The TLC-SVPWM has the same switching pattern as the proposed SPWM1 in Chapter 2. The three-leg clamping is achieved by the unbalanced voltage distribution in the proposed SPWM1, and the ZSV injection in the proposed SPWM1 can equalize durations of the two central vectors, which are located at six subcentres A-F in the space vector plane, in a PWM cycle. The proposed SPWM2 can also correspond to a 5-segment SVPWM similarly. However, the proposed SPWMs in Chapter 2 can reduce implementation complexity and computation burden compared with these SVPWMs.

# APPENDIX B PUBLICATIONS

## Journal Papers

- [1] L. Xu, Z. Q. Zhu, and L. Yan, "Low switching frequency SPWM strategies for open-winding machine with low current harmonics," *IEEE Transactions on Industry Applications*, vol. 58, no. 2, pp. 2042-2054, Mar.-Apr. 2022.
- [2] L. Xu and Z. Q. Zhu, "Inverter nonlinearity compensation for open-winding machine with dual switching modes," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2022.3164851.
- [3] L. Xu and Z. Q. Zhu, "A novel SVPWM for open winding permanent magnet synchronous machine with extended operation range," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2022, doi: 10.1109/JESTPE.2022.3200346.
- [4] X. Y. Sun, Z. Q. Zhu and L. Xu, "Analysis of excitation winding induced emf in non-overlapped stator wound field synchronous machines," *IEEE Transactions on Energy Conversion*, vol. 37, no. 1, pp. 685-695, Mar. 2022.

## Journal Papers under Review

- [1] L. Xu, Z. Q. Zhu, X. Wu, and L. Yan, "A generalized sinusoidal PWM strategy for open winding machine with low current harmonics", *IEEE Transactions on Energy Conversion*. under review.
- [2] L. Xu and Z. Q. Zhu, "Novel SVPWM for open winding PMSM drives with simultaneous common mode voltage control and full frequency zero sequence current suppression," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, under review.

## Conference Papers

- [1] L. Xu and Z. Q. Zhu, "A low switching frequency SPWM strategy for open-winding machine with low current harmonics," 2021 IEEE International Electric Machines & Drives Conference (IEMDC), 2021, pp. 1-7.
- [2] L. Xu and Z. Q. Zhu, "A novel SVPWM strategy for open-winding machine with low current ripples," 2021 IEEE International Electric Machines & Drives Conference (IEMDC), 2021, pp. 1-7.