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Design, control and modelling of piezoelectric transformer-based resonant power supplies

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Summary

This thesis proposes new techniques to improve the performance of the piezoelectric transformer (PT)-based resonant power supplies. The work is motivated by the increasing demands of smaller and higher energy density electronic circuits. The emergence of PTs provide a great opportunity to replace reactive components completely. This thesis provides improvements in this area.

The state of the art of PT-based techniques are reviewed, in terms of piezoelectric material, modelling and analysis. In addition, novel techniques for design, control and voltage regulation of PT-based converters are demonstrated. New analytical modelling methods for predicting the circuit behaviour of a PT-based converter are also described. The design challenges and research gaps form the basis of this thesis. The resonant current estimation techniques are provided initially, to reconstruct resonant and detect zero crossings. Three different implementations are proposed and validated by both simulation and experimental results. These current estimation techniques are applied throughout the thesis to provide zero voltage switching (ZVS) information for the control circuit. Following the current estimation techniques, nine novel controllers based on the phase-locked loop (PLL) are demonstrated, to lock onto the phase and frequency of the resonant current and generate adequate deadtime thereby ensuring ZVS. A comparative analysis of nine variants of PLL controllers are provided in terms of noise immunity and lock-on period. These control techniques are further extended to achieve an output voltage regulation. A 30V input 5V output PT-based converter is implemented. Finally, a novel converter modelling technique with a new control approach are proposed, with simultaneous ZVS and output regulation. Detailed models are provided for the proposed technique which accurately predict circuit behaviour. An implementation which provides a regulated 5V output voltage with 10V-60V input, by varying the deadtime interval, is reported.

Publications

1. Z. Yang, J. Forrester, J. N. Davidson, M. P. Foster and D. A. Stone, "Resonant current estimation and phase-locked loop feedback design for piezoelectric transformer-based power supplies", *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 10 466-10 476, 2020.

2. Z. Yang, J. Forrester, J. N. Davidson, M. P. Foster and D. A. Stone, "Output voltage regulation for piezoelectric transformer-based resonant power supplies using phase-locked loop", The 10th International Conference on Power Electronics, Machines and Drives (PEMD 2020), pp. 455-460, 2021.

Manuscripts in progress

3. Z. Yang, J. Forrester, J. N. Davidson, M. P. Foster and D. A. Stone," Resonant current estimation and voltage regulation for piezoelectric transformer-based power supply", to be published in the 11th International Conference on Power Electronics, Machines and Drives (PEMD 2022).

4. Z. Yang, J. Forrester, J. N. Davidson, M. P. Foster and D. A. Stone, " Cyclic mode analysis of H-bridge-driven inductorless piezoelectric transformers for simultaneous voltage regulation and zero-voltage switching ", to be submitted to *IEEE Transactions on Power Electronics*.

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Nomenclature

Symbol	Meaning
v_{in}	PT input voltage
v_{out}	PT output voltage
i_m	mechanical equivalent
R_m	Mechanical loss resistance
C_m	Series resonant capacitor
L_m	Series resonant inductor
n_1	electrical-to-mechanical transformation ratio
n_2	mechanical-to-electrical transformation ratio
L_1	Equivalent series inductor
R_1	Equivalent loss resistance
C_1	Equivalent series capacitor
i_{L1}	resonant current
i'_{L1}	current flow at the PT output section
N	Equivalent number of turns ratio for a piezoelectric ideal transformer

C_{in}	PT input capacitor
C_{out}	PT output capacitor
$v_{C\text{in}}$	PT input capacitance voltage
$v_{C\text{out}}$	PT output capacitance voltage
Q	Quality factor
R_L	Load resistor
v_L	Actual load voltage
$v_{\text{L}}^{'}$	Ideal load voltage
$v_{L,\text{RMS}}$	Root mean square value of the load voltage
v_{gs}	Gate-source voltage
v_{g}	Gate signal generated by the controller before applied to the gate driver
ω_0	Series resonant frequency
$x(t)$	State vector at time t
$x(t_i^+)$	Discontinuity in the state-variables at $t=t_{i+1}$

x_i	Vector to represent discontinuity in v_{Cin} due to MOSFETs switching
K	Vector to correct the values of the state variables at the switching instant
$\boldsymbol{A_i}$	Dynamical matrix for i^{th} mode of operation
$\boldsymbol{B_i}$	Input vector for i^{th} mode of operation
d_i	Duty cycle
m	operating modes
$\boldsymbol{\Phi_i}$	Augmented matrix for i^{th} mode of operation
$\boldsymbol{\Gamma_i}$	Argument input matrix for i^{th} mode of operation
φ	Resonant current phase angle
t_d	Half-bridge PT-based converter deadtime in time
δ	Half-bridge PT-based converter deadtime in radians
v_{ec}	Estimated current using voltage differentiator
v_{zc}	Modified estimated current

v_{d}	Estimated current using anti-parallel diodes
v_{lock}	VCO output signal
v_{lock}'	VCO output signal after frequency division
C_{t}	Timing capacitor of CD4046
I_{piezo}	PT equivalent current source
v_{burst}	Burst-mode control signal
K_{ZVS}	Zero voltage switching factor
Δt_i	Deadtime period of mode *i*
f_{s}	Switching frequency
f_{n}	Normalised switching frequency
v_{gain}	Normalised voltage gain

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Chapter I

Introduction

This chapter gives an outline of the work which contributes to this thesis. It includes the motivation for this research, issues of converter topology, control and modelling, and design challenges of modern power electronics. Finally, the thesis structure and main contribution of each chapter are presented.

1.1 Background

Power electronics is experiencing significant changes in the way energy is generated. The development of semiconductor technologies and advanced software making power electronic critical to the success of electricity networks in a foreseeable future. It is the centre of energy conversion, power devices and power system control.

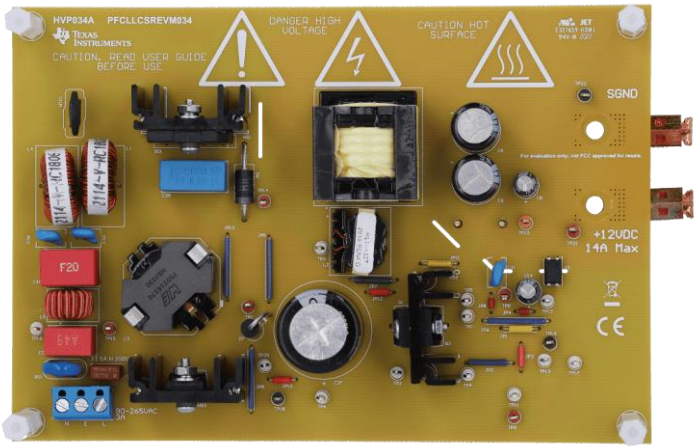
The ultimate potential of power electronics is growingly recognised by industrial and academic experts. It is a critical enabling technology and the heart of radical innovation in aircraft [1.1], renewable energy [1.2], automotive [1.3], robotics [1.4] and aerospace [1.5]. The development of power electronics provides a great opportunity to replace existing technologies due to the improvements in reliability, size, efficiency, cost and functionality, and allows the integration of various energy resources within an industrial facility.

Power electronics has functional impacts on industries and is buoyed by development in multiple technology areas, including new devices [1.6], new materials [1.7], new topologies [1.8], and new modelling techniques [1.9]. Over the past few years, piezoelectric transformers (PTs) have raised great research

interest for power electronic applications, owing to the emergence of advanced materials and novel applications. This field aims to enhance the design and modelling of PTs as well as improving the modelling, design and control of PT-based switch mode power supplies (SMPS). This thesis proposes a further study in this field.

1.2 Motivation

1.2.1 Trends in PT design and relevant techniques



(a)

(b)

(c)

Fig. 1.1: (a) AC/DC SMPS for power factor correction [1.10], (b) isolated flyback AC/AC inverter [1.11] and (c) PT-based DC/AC inverter [1.12].

PTs are a good alternatives to conventional magnetic transformers owing to the advantages including low electromagnetic interference (EMI), high power density (>40W/cm^3), high efficiency (compared to magnetic transformers, up to 98% [1.13]), reduced weight and simpler manufacturing process [1.14]–[1.17]. They transfer energy between input and output sections using mechanical vibrations. PTs are generally constructed from hard piezoelectric materials such as lead-zirconate titanate (PZT) and exhibit high quality (Q) factor and low loss. Fig. 1.1 (a) shows a typical LCC resonant converter for power factor correction from Texas Instruments. Even though the circuit is not optimised for energy density, it can be seen clearly that a conventional converter's size is significant with large of the capacitors, inductors and transformers. Fig. 1.1(b) and (c) show a conventional SMPS and a PT-based SMPS, respectively. It is clear that limited space available and PTs have higher density. As the trend in electronic equipment is moving towards lighter, smaller and cheaper, the emergence of PTs makes it possible that the reactive components of SMPSs can be completely replaced.

Many piezoelectric devices are constructed from PZT since it allows the material properties to be easily controlled and designed for a specific application [1.18]. The PZT composition that lies on what materials scientists call the *morphotropic phase boundary* (MPB) is normally used as it maximises the coupling coefficients and piezoelectric. However, at the MPB there are 14 possible poling directions due to coexistence of the rhombohedral and tetragonal polymorphs [1.19], and this draws a new challenge for the piezoelectric materials. These issues are the subject of research by prominent materials scientists [1.20]-[1.22]. For our purposes, it is enough to know that PZT is diverse in its poling and can be challenging in its manufacture.

PTs have been extensively commercialised in step-up applications such as cellular mobile phone battery chargers [1.23], LED lighting [1.24] and plasma

generators [1.25], since simple converter topologies and control methods are required. However, for step-down applications, the control circuit is more complex as load and line regulation are often required in addition to high efficiency operation. Additionally, voltage gain variation and resonant frequency drift should be considered since they are temperature and load dependent. This poses a new design challenge and research into voltage regulation, zero-voltage switching (ZVS) and control circuit are ongoing [1.26]–[1.28]

Due to complex piezoelectric materials, variation of PT voltage gain and resonant frequency drift, there is a vital area of research and a strong impetus to develop modelling, design and control of PT-based SMPS, which will be addressed in this thesis.

1.2.2 EPSRC project−FPeT

An EPSRC-sponsored research project, *FPeT*, was proposed and funded to undertake research on PT based resonant power supplies. The overall objective is to produce a framework for designing piezoelectric transformers, using a mixture of analytical tools, lumped-parameter models and finite element analysis. The research encompasses all aspects of piezoelectric transformer design and application. By combining normally separate disciplines, it is possible to simultaneously develop new electrical applications and new materials. The work presented in this thesis complements (and has been partially supported by) this project.

1.3 Novelty

The novelty of the work described in this thesis centres on the design a phase-locked loop (PLL) control system for PT-based inductorless half-bridge resonant converter. Nine variants of a PLL controller are accomplished by different resonant current estimation technique and gate signal generators. This technique

is further extended to achieve output voltage regulation. To regulate the output voltage under ZVS operation, an analytical model is proposed for a PT-based inductorless H-bridge converter, to predict the circuit behaviour, and to analysis ZVS profile and output voltage regulation characteristics. A new control approach for this H-bridge converter is also designed and implemented.

The main contributions presented in this thesis cover the following areas:-

1. **Resonant current estimation and PLL feedback design for PT-based half-bridge converter**

   The resonant current is internal to the PT and cannot be measured directly. This is a common scenario for a PT-based converter. New techniques for estimating the resonant current to identify effective signs for ZVS are presented in ***Chapter III*** while approaches to allow the lock-on to effective signs by PLL controller and generation of in-phase gate signals by steering logics are presented in ***Chapter IV***. For a typical PT-based converter, the proposed approach shows a fast system initialisation time, high tolerance to system noise, reduced lock-on period and low power loss compared with a traditional PT-based control method.

2. **Output voltage regulation of half-bridge inductorless PT-based inductorless converter**

   Based on the proposed PLL controller and gate signal generators, the PT-based converter is further extended to achieve output voltage regulation. The burst-mode hysteresis control is applied and improved due to non-instant stop behaviour of the PT-based circuit and presented in ***Chapter V***.

3. **Output voltage regulation of H-bridge inductorless PT-based converter with simultaneous parameter control**

To allow a wide input voltage or large load variation, an H-bridge PT-based inductorless converter is proposed. The new idea is to control the output voltage by varying the deadtime period and MOSFETs conduction time. Based on a PLL, the control system is further developed and accomplished by a mixed analogue-digital circuit, to generate in-phase gate signals. This new control method enables simultaneous parameter control for the proposed H-bridge configuration to achieve output regulation.

4. **Development of cyclic-mode analysis for PT-based inductorless H-bridge converter**

   The new technique of cyclic modelling is applied to an H-bridge PT-based inductorless converter to generate ZVS loci and voltage regulation characteristics. By using cyclic-mode analysis, a model is derived to predict the state-variable values of the circuit for a given operating condition. Subsequently, the proposed model is used to demonstrate the operation in ZVS region and it provides estimates for the required deadtime period, load and operating frequency along the ZVS boundary. The output voltage-regulation profile is then indicated by the model and regions where voltage regulation can be continuously achieved while still obtaining ZVS are demonstrated.

1.4 Thesis structure

The thesis is organised into seven chapters with interconnections. The publications correspond to each chapter is given in section 1.3. A full list of referenced papers and chapter summary can be found at the last section of each chapter. A brief introduction of each chapter is given below.

Chapter I demonstrates the general background and motivation of the thesis and the importance of modern power electronics. The thesis structure is provided with brief description of each chapter.

Chapter II reviews the state-of-the-art work reported in the literature. The first part is the previous research on PTs regarding types of PTs, materials of PTs, emerging technologies, PTs modelling techniques and different applications. Then, different topologies driving PTs are reviewed. Additionally, potential control techniques, current estimation approaches and output voltage regulation methods for PT-based converter are discussed. Finally, the design challenges and research gaps posed by PTs are identified, which will be addressed in later chapters.

Chapter III introduces the novel methods for estimating resonant current for PT-based converter. Two types of current estimators with two different locations for current estimation are proposed. Additionally, the chapter establishes the experimental setup used in this thesis to estimate the resonant current, indicate zero-voltage switching (ZVS) and provide feedback signal for the control circuit.

Chapter IV presents a novel control technique associated with phase-locked loops (PLL) for fast resonance tracking. By using the synchronisation function of a PLL, different types of pulse-width modulation (PWM) signals can be generated, and three different approaches to provide in-phase gate drive signals with required deadtime are proposed. Additionally, comparison between different combinations of current estimators and gate signal generators are demonstrated in terms of lock-on period, fact-tracking ability and noise immunity.

Chapter V demonstrates an output voltage regulation method based on burst-mode control for PT-based inductorless converter using the current estimation method indicated in ***Chapter III*** and ZVS PLL controller presented in ***Chapter***

IV. By setting up a hysteresis window with voltage regulation limit, the circuit operates in burst mode and the burst signal is used to control the MOSFETs on/off periods thereby meet the regulation requirement.

Chapter VI introduces a novel method to simultaneously achieve output voltage regulation and ZVS, and a new analytical approach to model the resonant circuit. A cyclic-mode analysis is performed to estimate the state-variable values of the circuit for a given operating condition. The ZVS region is then generated and ZVS loci are provided for variable deadtime period, operating frequency and load. Subsequently, the output voltage-regulation profile is indicated by the model and the regions where voltage regulation is continuously achievable while maintaining ZVS are presented. In addition, ***Chapter VI*** further improves the ZVS PLL control technique presented in ***Chapter IV***. It modifies the control technique with a mixed analogue-digital circuit, which is modified to suit an H-bridge PT-based inductorless converter. The deadtime period and MOSFET conduction time can be controlled independently with the circuit still achieving ZVS. The technique enables simultaneous parameter control for an H-bridge configuration and is used to validate the analytical model presented in this chapter.

Chapter VII summarises the work and highlight the improvement to the field of power electronics. It recommends the future work which could be undertaken following the work from this thesis.

1.5 References

[1.1] B. Rahrovi and M. Ehsani, "A Review of the More Electric Aircraft Power Electronics," *2019 IEEE Texas Power and Energy Conference (TPEC)*, 2019, pp. 1-6.

[1.2] J. Sun *et al.*, "Renewable energy transmission by HVDC across the

continent: system challenges and opportunities," *CSEE Journal of Power and Energy Systems*, vol. 3, pp. 353-364, 2017.

[1.3] D. Bilyi and D. Gerling, "Modeling of automotive power network for analysis of power electronics and losses calculation and verification by measurements on claw-pole alternator," *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, 2016, pp. 3599-3605.

[1.4] M. Lok, X. Zhang, E. F. Helbling, R. Wood, D. Brooks and G. Wei, "A power electronics unit to drive piezoelectric actuators for flying microrobots," *2015 IEEE Custom Integrated Circuits Conference (CICC)*, 2015, pp. 1-4.

[1.5] U. Nasir *et al*., "A SiC based 2-Level Power Converter for Shape-and-Space-Restricted Aerospace Applications," *2019 IEEE 13th International Conference on Power Electronics and Drive Systems (PEDS)*, 2019, pp. 1-7.

[1.6] K. Ino, M. Miura, Y. Nakano, M. Aketa and N. Kawamoto, "SiC Power Device Evolution Opening a New Era in Power Electronics," *2019 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, 2019, pp. 1-3,

[1.7] G. Hao *et al*., "Study on Improving the Short-Time Overcurrent Capability of Press- pack IGBTs Using Phase Change Materials," *2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia)*, 2020, pp. 2173-2177.

[1.8] M. Petersen and F. W. Fuchs, "Investigation on power electronics

topologies for inductive power transfer (IPT) systems in high power low voltage applications," *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, 2015, pp. 1-10

[1.9] C. Shah et al., "Review of Dynamic and Transient Modeling of Power Electronic Converters for Converter Dominated Power Systems," *IEEE Access*, vol. 9, pp. 82094-82117, 2021.

[1.10] Texas Instruments, “PFCLLCSREVM034,” USA, 2021.

[1.11] Power integrations, “RDR-839,” 2019.

[1.12] LCDIS, embedded & display solutions, “CCFL LED backlights with piezo inverter,” France, 2021.

[1.13] E. L. Horsley, M. P. Foster and D. A. Stone, "State-of-the-art Piezoelectric Transformer technology," *2007 European Conference on Power Electronics and Applications*, 2007, pp. 1-10.

[1.14] V. C. Alfredo, “50 years of piezoelectric transformers. Trends in the technology,” *Materials research society symposium proceedings*, vol. 785, 2003, pp.33-44.

[1.15] J. Díaz, F. Nuno, M. J. Prieto, J. A. Martín-Ramos, and P. J. Villegas Saiz, “Closing a second feedback loop in a DC-DC converter based on a piezoelectric transformer,” *IEEE transactions on power electronics*, vol. 22, pp. 2195-2201, 2007.

[1.16] E. M. Baker, Weixing Huang, D. Y. Chen and F. C. Lee, "Radial mode piezoelectric transformer design for fluorescent lamp ballast applications," *IEEE Transactions on Power Electronics*, vol. 20, pp. 1213-1220, 2005.

[1.17] S. Ben-Yaakov and S. Lineykin, "Maximum power tracking of piezoelectric transformer HV converters under load variations," *IEEE Transactions on Power Electronics*, vol. 21, pp. 73-78, 2006.

[1.18] R. C. Buchanan, R. W. Schwartz, J. Ballato, and G. H. Haertling, Ceramic materials for electronics, (chapter 4), 3rd ed: Marcel Dekker Inc., 2004.

[1.19] R. E. Newnham, "Molecular Mechanisms in Smart Materials," *MRS Bulletin*, vol. 22, pp. 20-34,1997.

[1.20] D. W. Wang, H. Fayaz, K. Amir, F. Antonio, T. Ye, Q. L. Zhao, and I. M. Reaney. "Composition and temperature dependence of structure and piezoelectricity in (1− x)(K1− yNay) NbO3-x (Bi1/2Na1/2) ZrO3 lead-free ceramics." *Journal of the American Ceramic Society*, no. 2, pp. 627-637, 2017.

[1.21] A. Khesro, D. Wang, F. Hussain, R. Muhammad, G. Wang, A. Feteira, and I. M. Reaney, "Temperature dependent piezoelectric properties of lead-free (1-x) K0. 6Na0. 4NbO3–xBiFeO3 ceramics." *Frontiers in Materials*, no. *7*, pp.140, 2020.

[1.22] C. A. Randall, R. Eitel, B. Jones, T. R. Shrout, D. I. Woodward, and I. M. Reaney. "Investigation of a high T c piezoelectric system:(1− x) Bi (Mg 1/2 Ti 1/2) O 3–(x) PbTiO 3." *Journal of applied physics*, no. 7. pp. 3633-3639, 2004

[1.23] J. Navas, T. Bove, J. A. Cobos, F. Nuno and K. Brebol, "Miniaturised battery charger using piezoelectric transformers," *16th Annual IEEE Applied Power Electronics Conference and Exposition*, 2001, pp. 492-496.

[1.24] M. S. Roedgaard, M. Weirich, and M. A. E. Andersen, “Forward conduction mode controlled piezoelectric transformer-based PFC LED drive,” *IEEE transactions on power electronics*, vol. 28, pp. 4841–4849, 2013.

[1.25] B. T. Hutsel, S. D. Kovaleski and J. W. Kwon, "Optimization of Piezoelectric Resonance Effect in a Piezoelectric Transformer Plasma Source," *IEEE Transactions on Plasma Science*, vol. 41, pp. 305-311, 2013.

[1.26] A. J. Gilbert, C. M. Bingham, D. A. Stone and M. P. Foster, "Self-Oscillating Control Methods for the LCC Current-Output Resonant Converter," *IEEE Transactions on Power Electronics*, vol. 23, pp. 1973-1986, 2008.

[1.27] M. P. Foster, J. N. Davidson, D. A. Stone, and R. Yappa, “A PLL controller for achieving zero voltage switching (ZVS) in inductorless half-bridge drive piezoelectric transformer resonant power supplies.” *The Journal of Engineering*, pp.3639-3642, 2019.

[1.28] Y. P. Liu, D. Vasic, F. Costa and D. Schwander, "Improvement of burst-mode controlled piezoelectric transformers," *15th International Power Electronics and Motion Control Conference (EPE/PEMC*), 2012, pp. DS2c.7-1-DS2c.7-6.

Chapter II

Literature review

This Chapter presents a review of the state-of-the-art techniques in PT design, PT-based power converter design, voltage regulation, control, modelling and their applications. This Chapter provides the reader with the basic knowledge required to understand the improvements in the current research field, some of which is proposed in following chapters covering PT-based converter design, control, output regulation and circuit modelling.

2.1 Introduction

In Chapter I, it was shown that the trend in electronic equipment is for lighter, smaller and cheaper products and the emergence of PTs makes it possible that the reactive components of SMPSs can be completely replaced only if proper modelling and control strategies are employed for ZVS operation and voltage regulation. Following the background, motivation, novelty and thesis structure described in Chapter I, a literature review for current research field will be presented in this chapter.

Piezoelectric devices are normally constructed from high quality factor piezoelectric materials, and transfer energy using electro-mechanical properties of the material at its mechanical (vibration) resonance. Different types of piezoelectric devices have emerged, with different modelling techniques for accurately predicting piezoelectric device behaviour. A discussion of piezoelectric effect, devices, material and modelling is therefore described in section 2.2.

Since PT-based SMPSs exhibit great advantages over conventional magnetic ones, different driving techniques are employed to reduce switching loss, ensure soft switching, maximum PT output power and achieve output voltage regulation. A discussion of PT-based converter topologies is therefore presented in section 2.3.

To track resonant frequency and maintain a desirable voltage gain of a PT, great effort should be given to the control circuitry since PT parameters are temperature and load dependent. As voltage regulation is normally required for converters, different techniques have been employed to form a second feedback control to achieve high efficiency operation as well as output voltage regulation. A discussion of state-of-the-art control techniques is therefore described in section 2.4.

Unlike conventional resonant converters, PT-based converters find it difficult to achieve ZVS due to the limited resonant current which much charge a large input capacitance, giving rise to the necessary deadtime period. Thus, it is important to understand and be able to predict the circuit behaviour and ZVS characteristics of a given PT for practical applications. A discussion of PT-based converter modelling techniques reported in literature is therefore demonstrated in section 2.5.

Finally, the design challenges and research opportunities are identified and highlighted in section 2.6, which will be addressed in subsequent chapters.

2.2 Piezoelectric devices

2.2.1 Piezoelectric effect

The piezoelectric effect is the ability of piezoelectric materials to provide an electric charge when mechanical stress is applied. This effect is reversible since

it generally exhibits a direct piezoelectric effect (a charge is produced when mechanical stress is applied) and a converse piezoelectric effect (a strain is developed when applying an electric field), as shown in Fig. 2.1.

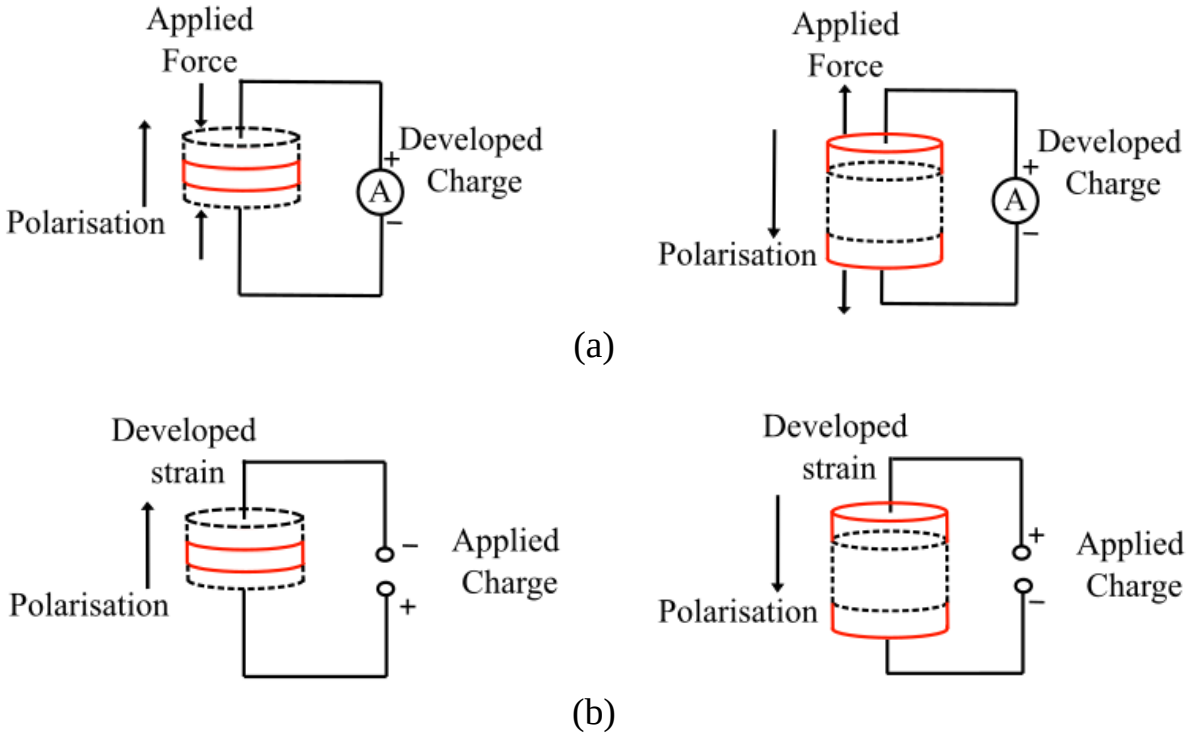


Fig. 2.1: (a) Direct and (b) converse piezoelectric effect.

As can be seen from Fig. 2.1(a), when a mechanical strain is applied, positive and negative charge centres of the piezoelectric material shifts, resulting in an outer electrical field and current flow through the ammeter (A). The dashed line shows the original thickness of the device which is reduced (red lines) under strain. Conversely, in Fig. 2.1(b), the external electrical field leads to a contraction or expansion of the piezoelectric material (once again demonstrated by the dashed and red lines), depending on the charge direction. PTs use both direct and converse piezoelectric effect to transfer energy electromechanically from input to output terminals.

2.2.2 Piezoelectric material

Piezoelectric materials are generally classified as ceramic, crystalline and polymeric [2.1]. Although the large electromechanical coupling factors of crystal materials make them attractive for the construction of PTs, polycrystalline ceramics are generally the material of choice for most PTs. Commonly used piezoelectric ceramics include barium titanate, lead zirconate titanate (PZT) and lead titanate, among which PZT ceramics are most popular since they exhibit low curie temperature, high sensitivity and high coupling coefficients [2.1]. In addition, by incorporating modifiers and dopants, the material properties can be tailored through customisation of PZT chemical composition [2.1].

PZT generally exhibits different types of polymorphs. To improve dielectric and piezoelectric properties, a certain range of composition have been investigated and the PZT ceramics composition lying on the morphotropic phase boundary (MPB) region or near this region is usually considered. Since rhombohedral and tetragonal structures coexistence at MPB, a number of PZT material variants occurs with different poling directions, and make it possible to achieve a specific crystal structure and a desired piezoelectric response. PZT ceramics at MPB with modified composition have been employed in various applications, such as piezoelectric transducer [2.2] and sensor [2.3]. In [2.4], for example, a specific composition for PZT ceramic at MPB was presented with sintering temperature at 1250°C. The Nb dopant improved the dielectric constant (1500 at 1kHz), loss factor (0.02) and electromechanical coupling coefficient (0.591) of the PZT material, and a piezoelectric sensor was fabricated with enhanced device property.

2.2.3 Piezoelectric transformer

Different types of PT have been commercialised currently and they are classified based on their vibration mode: thickness mode, radial mode, thickness-shear mode, and longitudinal mode. The mode is defined as the natural frequency at

which a PT resonates. In general, the piezoelectric transformer converts energy stored in electrical charge into mechanical energy (stored in stress) and the reconverts this energy back to an electrical charge. The simplest concept of a PT can be thought of as a piezoelectric actuator mechanically attached to a piezoelectric transducer. A desired voltage conversion can be achieved for a specific application if a PT is properly designed.

2.2.3.1 Thickness mode PTs

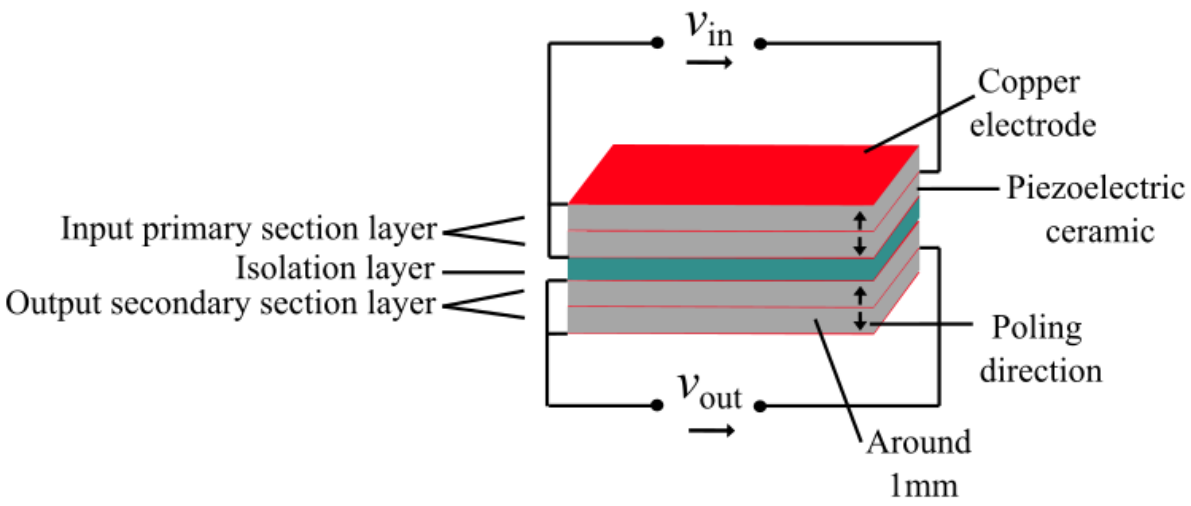


Fig. 2.2: Thickness mode PT [2.5][2.6].

Thickness mode PTs generally exhibit the lowest thickness dimension compared with other types of PTs in terms of length, width and radius. For a thickness mode PT, the poling direction is in parallel with the applied electric filed, and input and output sections are constructed one after the other making a stack. A typical thickness mode PT design is shown in Fig. 2.2 as proposed in [2.5][2.6], which includes two layers for each input and output section, with an insulation layer in between thereby providing an isolated output voltage. The dimensions of width and length of this type of PT is normally much larger than the thickness, resulting in a large output capacitance and high resonant frequency [2.7] and therefore a low output impedance, which is suitable for low voltage applications [2.7]. The

thickness of each layer is usually around 1mm [2.8].The voltage transfer ratio of a thickness mode PT is proportional to the ratio of a single input layer thickness to a single output layer thickness [2.8]. The electromechanical coupling factor of thickness mode PTs are higher than other types of PTs [2.8], which is desirable for high power density operation [2.9].

However, thickness mode PTs exhibit fundamental problems. Since the thickness is much smaller than the width and length, the resonant frequency of thickness vibration mode is high compared to the width and length vibration mode resonant frequencies, due to the high transverse mode coupling factor of the PZT material [2.5]. In other words, unwanted spurious (not designed for) vibration modes could occur near the thickness vibration mode, causing undesirable fluctuations in the impedance frequency response [2.5]. Furthermore, spurious vibration modes reduce PT efficiency, maximum power density and attenuate the desired thickness vibration mode [2.10].

To reduce disturbance from spurious vibration mode, it is possible to change the PT geometry such that length and width is smaller than thickness, as proposed in [2.5][2.6], since the lowest resonance is determined by the largest dimension of the PT [2.8]. However, this would in turn shift the resonant frequency into a lower region, result in low power density and smaller output capacitance. In [2.5], suppressing the high order modes was presented by using the barium to ensure the electromechanical coupling factors of spurious vibration modes are small. In [2.10], a ring shape thickness mode PT was proposed to ensure the high order modes away from the thickness mode, by modifying the ratio of inner and outer radius. The PT achieved an overall efficiency of 98% at 330kHz with a power density of 50 W/cm^3. Although the frequency response of the ring shape thickness vibration mode PT was significantly improved compared with [2.6], the ring shape created difficulties for mounting.

2.2.3.2 Radial mode PTs

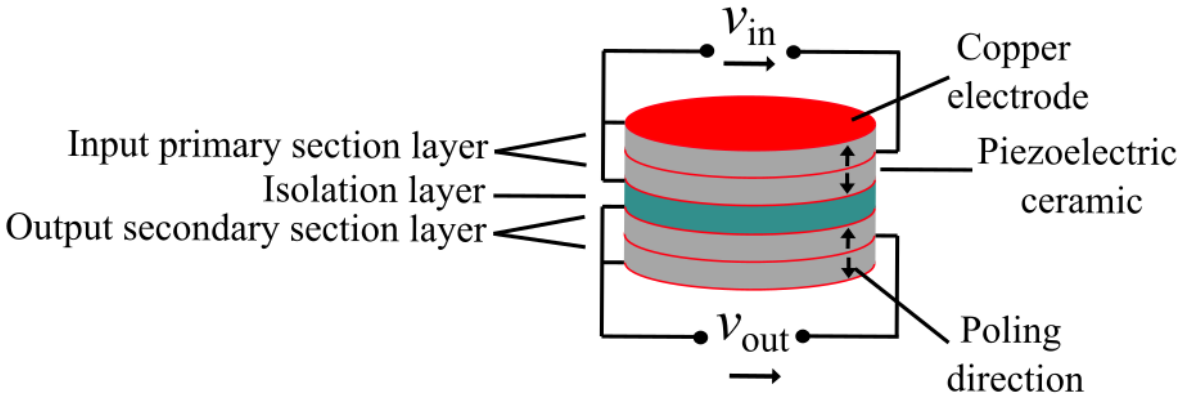


Fig. 2.3: Radial mode PT [2.7].

A typical radial mode PT consists of several individual piezoelectric discs, with an isolation layer in between, as shown in Fig. 2.3. To achieve a desired transformer characteristic, the number of layers for primary and secondary section can be adjusted. By exciting the primary section of the PT, the radial strains are generated from the device thereby producing an output voltage at its secondary section. The power rating for the radial mode PTs reaches up to 40W/cm^3 [2.11], with a typical power of 100W-200W [2.12], at 50-300kHz resonant frequency range [2.13], while the traditional transformers are used at power levels of 50W-1000W [2.14].

To maximise the PT performance that only radial vibration mode occurs, it is desirable to used disc shape for each layer, since the distances from centre to edge of each layer are the same. In [2.14], the performance of square and disc shaped layer were compared, and it was shown that square shape exhibited a decreased electromechanical coupling factor (hence a reduced energy conversion between electrical and mechanical energy). This is mainly because the distances from centre to edge of a square shaped layer are not equal, and additional vibration modes are introduced [2.15].

2.2.3.3 Thickness-shear mode PTs

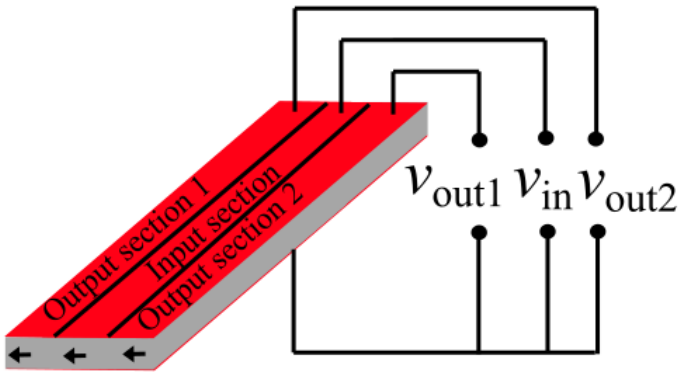


Fig. 2.4: Thickness-shear vibration mode PT [2.8].

Compared with other types of PTs, the poling direction of thickness-shear vibration mode PT is orthogonal to the applied and generated electric field. By exciting at the PT input section, a shear strain of the device is generated thereby producing a voltage at the PT output section. The power density of the thickness-shear vibration mode PT is normally high since most PZT material exhibits a large shear mode electromechanical coupling factor [2.7].

To obtain a multi-output PT, multiple transducer regions can be applied to a single device when the PT is constructed [2.16]. In [2.16], a thickness-shear vibration mode PT with multiple outputs was presented. A total output power of 170W was achieved with 17.7W/cm^3 power density at 90% efficiency. However, research on this type of PT is less developed since the lumped equivalent circuit which models the multiplayer input and output sections, and corresponding electrical voltage and current refers to vibration velocity are still being studied. Furthermore, this type of PT exhibits the same problem as the thickness vibration mode PT, that higher order spurious mode occurs in the vicinity of the desired vibration mode [2.16].

2.2.3.4 Longitudinal mode PTs (Rosen type transformer)

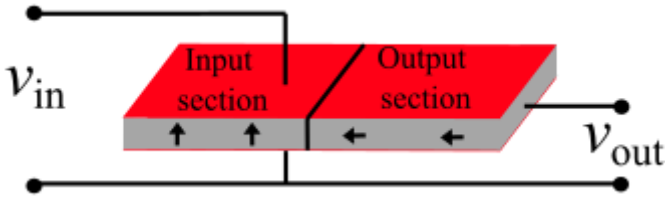


Fig. 2.5: Single layer longitudinal mode PT [2.7].

The Rosen-type PT shown in Fig. 2.5 consists of a single layer rectangular piezoelectric material. As can be seen, the input section of the piezoelectric ceramic is poled in thickness direction while the output section is poled in length direction. For this PT the input and output section possess a common electrode across the bottom of the device. When applying an AC voltage to the thickness poled input section, a corresponding longitudinal vibration at the same frequency occurs (i.e. converse piezoelectric effect). The vibration is mechanically coupled throughout the entire piezoelectric ceramic and a potential difference at the longitudinal poled output section is generated (direct piezoelectric effect). Therefore, the input section exhibits a piezoelectric actuator behaviour and output section experiences a piezoelectric transducer behaviour. For a given input voltage, if this type of PT operates at resonance, the vibration amplitude and corresponding strains can be maximised [2.8].

Rosen-type PTs are commonly used in step-up application due to its high output impedance and high output gain nature [2.17]–[2.19]. For the single-layer Rosen-type PT, as shown in Fig. 2.5, the transformation ratio is proportional to the ratio of length to thickness of the PT [2.15]. Higher transformation ratios can be achieved if the multi-layer piezoelectric ceramic is used. Rosen-type PTs have been extensively used in low current and high voltage applications, such as field emission displays [2.20] and LCD backlighting [2.21]. In [2.12], an output power of 5-8W was achieved for a Rosen-type PT with 5-10W/cm^3 power density. The

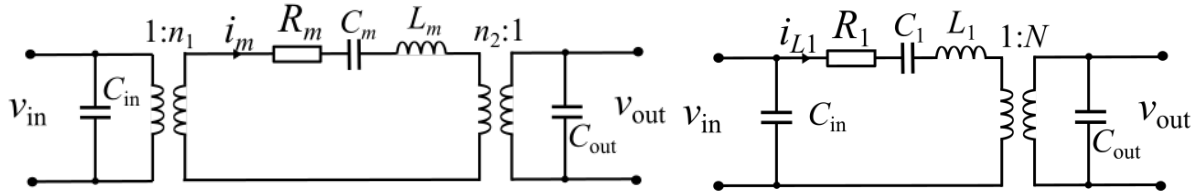
Rosen-type PTs generally exhibit low power density since the coupling factors corresponds to the input region is transverse coupling factor, which is the lowest coupling factor in most PZT materials [2.8].

2.2.4 Simulation, modelling and analysis of PTs

Equivalent circuit models are extensively used to describe the electrical characteristics of a PT. Several modelling and simulation techniques have been performed to optimise the PT design, such as lumped equivalent circuit model [2.22], analytical continuum model [2.23] and finite element analysis (FEA).

2.2.4.1 Ideal equivalent circuit

Mason equivalent circuit is the most commonly used equivalent circuit model. It is an ideal model that describes a PT operating at resonance, with no other vibration mode introduced and with the material dielectric losses neglected.



(a) (b)

Fig. 2.6: (a) Full lumped and (b) simplified equivalent circuit model.

A typical full lumped equivalent circuit model is shown in Fig. 2.6 (a) and a simplified model is given in Fig. 2.6 (b). The equivalent model shown in Fig. 2.6 can be used to model all types of PTs. In Fig. 2.6(a), the input and output electrode capacitances are modelled by C_{in} and C_{out}, they range up to a few nano-farads due to PT geometry limit. R_m corresponds to the mechanical loss, L_m (around 100mH), C_m (around 100pF) represent the resonant characteristics, n_1 and n_2 represent electrical-to-mechanical and mechanical-to-electrical transformation ratio of a PT. i_m is the excited mechanical current and it is equivalent to the device vibration

velocity [2.8]. Referring the mechanical equivalent components across the ideal transformer n_1 allows the mechanical branch shown in Fig. 2.6(a) to be simplified to the equivalent circuit given in Fig. 2.6 (b), where

$$R_1 = \frac{R_m}{n_1^2} \tag{2.1}$$

$$L_1 = \frac{L_m}{n_1^2} \tag{2.2}$$

$$C_1 = C_{\mathrm{m}} n_1^2 \tag{2.3}$$

$$N = \frac{n_1}{n_2} \tag{2.4}$$

With the equivalent circuit models, the electrical characteristics of a PT can be represented as a function of temperature, material parameters, load condition and device dimensions. Furthermore, this is also the initial state from which to design a good PT-based converter.

2.2.4.2 Lumped parameter model

Since PTs can operate in different vibration modes at different frequencies, undesired spurious modes could interfere with the optimum vibration mode thereby reducing the PT efficiency [2.8]. Therefore, it is important to accurately model the spurious vibration modes.

In [2.24], an extended lumped parameter model was presented. Multiple RLC branches were introduced to model main resonant vibration mode and other spurious vibration modes. Each vibration mode was modelled by the corresponding RLC network while only the main vibration mode turns ratio was used. This approach was further developed in [2.15], as shown in Fig. 2.8, where

different turns ratio values were used to model the spurious vibration modes and modelling accuracy was improved.

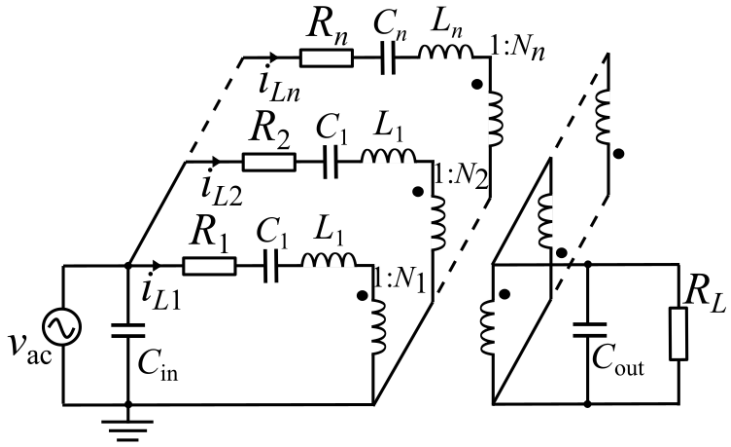


Fig. 2.7: Extended equivalent circuit model [15].

In [2.25], the lumped parameter model was developed for a galvanically isolated ring-dot PT. A ring-dot PT is typically poled in in thickness direction, and exhibits a hole at the centre to improve the heat radiation since the highest temperature occurs in this area during device operation. The ‘gap’ section that occurs between the input dot and output ring electrodes was modelled. Subsequently, the model was further developed for a non-ideal case that the ‘gap’ region is made from a polled material. The results showed good agreement with simulation and experimental measurements.

2.2.4.3 Simulation

Compared with analytical solutions for piezoelectric device modelling, finite element analysis (FEA) using numerical methods provides an effective way of evaluating and validating PT designs. Several software packages existing including Ansys, PZFlex and COMSOL. FEA with COMSOL offers several advantages for PT design, such as the ability to achieve accurate electromechanical coupling assessment [2.26], structure and circuit simulation [2.26], complex topological structure [2.27] and piezoelectric structure vibration

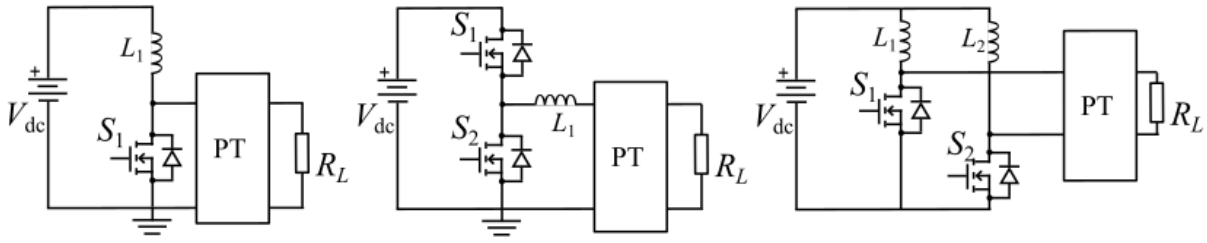
simulation [2.28]. It brings the opportunity to validate the analytical model and optimise device geometry and material properties.

2.3 PT-based converter

PTs exhibit a narrow bandwidth (within 50kHz) by virtue of their high *Q*-factor and, therefore, it is necessary for a converter to operate close to the PTs resonant frequency to ensure high efficiency operation [2.8]. In general, a PT normally operates slightly above its resonance, where it experiences inductive behaviour, since the efficiency of a PT can be maximised when it is driven by a frequency higher than the resonant frequency [2.8][2.9]. Therefore, the converter topology should be carefully selected to ensure an optimal operating frequency.

2.3.1 Inductor driven topologies

Generally, a PT can be driven by a square wave or a sine wave. It has been reported that a sine wave input would reduce the energy circulating through the PT input capacitance thereby reducing switching loss due to capacitive turn-on of PT input capacitance, and achieving zero-voltage switching (ZVS) [2.12]. However, additional reactive components are required in order to provide a sinusoidal drive waveform (typically an inductor).



(a) (b) (c)

Fig. 2.8: PT driving circuit topologies: (a) class-E, (b) half-bridge and (c) push-pull.

The most commonly used topologies reported in the literature to drive PTs include class-E, half-bridge and push-pull, as shown in Fig. 2.8(a), (b) and (c), respectively.

For step-down applications, half-bridge and class-E are extensively used and are desirable for high and low power levels, respectively [2.29]. Both configurations are compared in [2.29], and it is shown that half-bridge configuration performs better in high efficiency. Due to band-pass-filter nature and high-quality factor of a PT, an excitation of a square waveform at PT input results in a sinusoidal waveform output at its fundamental component. Therefore, additional losses in the PT occurs due to the harmonics of the square waveform, thereby reducing the maximum power density [2.9].

For step-up applications, push-pull configuration are widely used due to the simple control circuit requirement and high step-up ratio [2.9] [2.12]. In [2.30], an energy conversion with 70% efficiency was achieved by using an amplitude modulation via push-pull topology. Compared with the half-bridge square wave excitation, the loss within the PT is reduced since reduced harmonics from the input voltage are introduced.

2.3.2 Inductorless driven topology

To ensure ZVS operation, it has been reported that additional components can be used. This is often done by placing a series inductor at the PT input section using a half-bridge configuration, in order to provide extra resonant current to sufficiently charge the PT input capacitor during the deadtime. The presence of the input inductor means the PT input capacitor is not instantaneously discharged by the switching of the half-bridge MOSFETs. However, as mentioned previously, this requires an additional component and so would remove one of the possible advantages for using a PT in the first place.

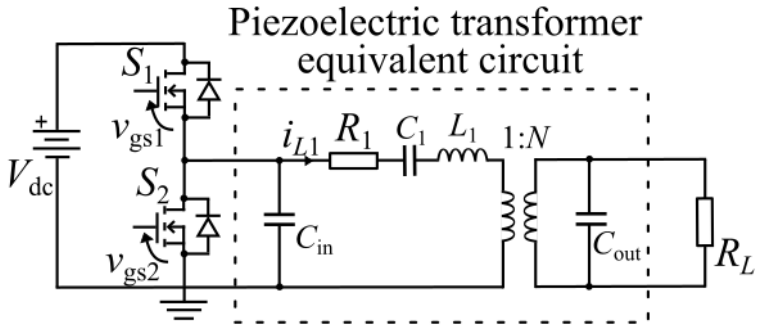


Fig. 2.9: The half-bridge inductorless driven PT-based converter.

A typical half-bridge inductorless driven PT-based converter is shown in Fig. 2.9. Here, a significant deadtime exists between the between the turn-off of S_2 and turn-on of S_1 to allow C_{in} to be naturally charged by the resonant current i_{L1} from 0 V to V_{dc} to achieve zero voltage switching (ZVS). In [2.31], both DC and AC analysis for achieving ZVS has been reported for an inductorless configuration using numerical optimisation techniques. Five rectifier configurations were performed and it was shown that ZVS ability was largely dependent on the load, PT capacitor ratio and deadtime conditions. A comparison between inductor and inductorless operation has been presented in [2.32]. Compared with inductorless configuration, the inductor topology refers to a PT-based SMPS with an additional series inductor placed between the PT input section and the half-bridge. It was indicated that applying a series/parallel inductor would significantly enhance the ZVS performance, and relaxing the requirements of load, PT design, range of input voltage and deadtime. The inductorless configuration can be used only if the PT is designed with a carefully chosen input-to-output capacitor ratio [2.33] (i.e. $C_{\text{in}}/(N^2C_{\text{out}})$) and a precise control is employed to track resonant frequency, since resonant frequency is both load and temperature dependent [2.8]. A comparison of the PT-based SMPS configurations reported in literature are shown in Table 2.1,

Table 2.1: Comparison of different topologies of PT-based converter

Topology	Push-pull		Class-E	Half-bridge		Half-bridge inductorless	
Reference	[2.34]	[2.30]	[2.29]	[2.35]	[2.36]	[2.37]	[2.38]
Efficiency[%]	86	70	70.5	82.4	83.5	86	90
Power[W]	/	2	3.6	3.6	/	6.5	32

2.4 Control strategy

To ensure high efficiency operation of PT-based converter, a PT should be driven slightly above the resonance where it exhibits an inductive behaviour. However, the operation band is reduced to a narrow range due to its high-quality factor. Furthermore, with inductorless configuration, the soft-switching ability is further reduced due the necessity of charging C_{in} between the supply rails during the deadtime. Any resonant frequency drift would significantly reduce the PT efficiency. Thus, the control circuit should provide both an adequate deadtime and precise tracking of resonant frequency to account temperature and load variations [2.39].

2.4.1 Purpose of control

The control techniques of PT-based SMPS reported in literature mainly focus on two purposes: maximum efficiency [2.40][2.41] and maximum output power [2.18][2.42].

To achieve maximum efficiency operation of a PT-based converter, the energy transferred from a PT should be maximised, and this can be obtained by operating the circuit at the matched load. The matched load condition is the worst case for achieving ZVS since it provides the lowest resonant current (i.e. highest

efficiency point) to charge PT input capacitance. The match load can be defined as [2.8]:

$$R_L = \frac{1}{\omega_0 C_{\text{out}}} \tag{2.5}$$

where ω_0 is the series resonant frequency and C_{out} is the PT output capacitance.

The matched load condition is considered the worst case for achieving ZVS because, for a fixed deadtime, it takes the longest period to charge the input capacitance. Thus, if ZVS can be obtained at matched load condition, it is achievable for all load conditions [2.33]. In addition, sufficient deadtime should be provided by the control circuit in order to ensure that PT input capacitance can be fully charged to the DC rail thereby achieving ZVS. In general, optimum operating point for ZVS operation can be detected by measuring the phase difference between the PT input voltage and resonant current [2.41][2.43] or PT input and output voltage [2.12], thereby adjusting the operating frequency through a control circuit with time delay compensation, to ensure ZVS at matched load condition with an adequate deadtime.

The maximum output power tracking normally aims for load and line regulation, the frequency at which maximum voltage gain (or maximum output voltage) occurs should be locked by the control circuit. The operating point where maximum voltage gain occurs can be indicated by measuring the phase difference between the PT input and output voltage [2.18] or output voltage and output current [2.12]. Subsequently, the operating frequency of the PT-based converter is controlled such that it varies accordingly with respect to input voltage or load variation. In [2.18], a deviation of the optimum frequency was proposed and it was highlighted that maximum voltage gain can be achieved when the PT was

operated close to its primary resonant frequency and phase different between PT input voltage and resonant current was zero.

2.4.2 Control techniques

Piezoelectric transformers should be carefully controlled in order to achieve a desired output power and efficiency, since 1) resonant frequency shifts due to load and temperature variation [2.44], 2) voltage gain changes with respect to temperature [2.39], operating frequency [2.7] and load [2.18]. Several techniques have been employed to control the PT-based converter to address these issues.

2.4.2.1 Phase-locked loop control

The phase-locked loop (PLL) is a control system that compares an input signal with an internally generated oscillator signal and it provides this signal as an output which is related in some manner to the phase- and frequency-of the input signal, as shown in Fig. 2.10. It typically consists of a phase comparator, a low-pass filter and a voltage-controlled oscillator.

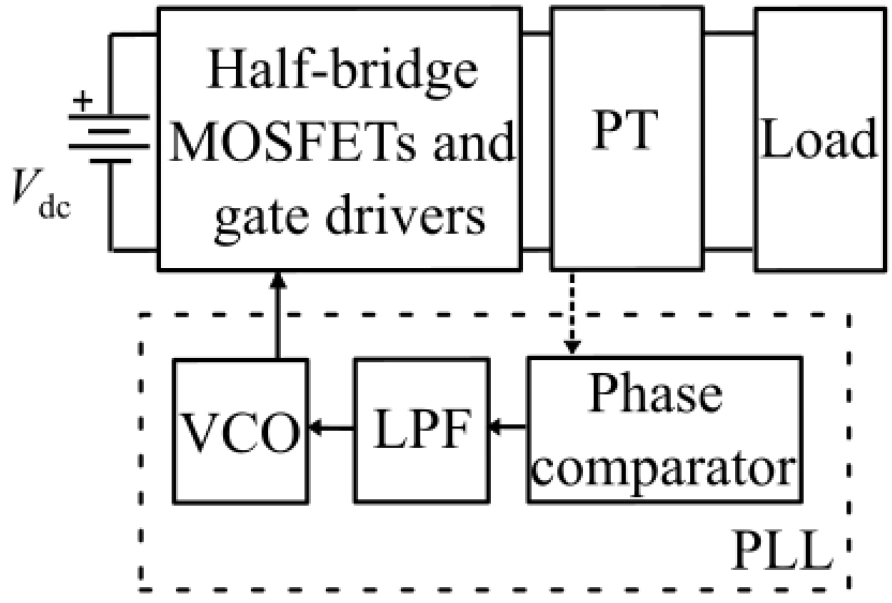


Fig. 2.10: A PLL controller for PT-based converter.

By measuring the phase difference, such as the phase lag between PT input and output voltage [2.9] or the PT input voltage and resonant current [2.13], the PLL is able to synchronise both phase and frequency of the input signals, thereby locking on to the resonant frequency and thus able to adjust the operating frequency according to load and temperature variation. The ability of the PLL to lock on to phase and frequency, irrespective of circuit conditions [2.45] and fast tracking response [2.13] makes the PLL control highly desirable for a PT-based converter.

In [2.46], ZVS was satisfied over 120V-230V input voltage and a 92% total efficiency with 5.7W output power was achieved by using a PLL. In [2.13], different variants of PLL implementation were proposed. ZVS was achieved at matched load condition and all the implementations indicate fast tracking performance (5-6 resonant periods) for PT start-up. By using the fast tracking behaviour of a PLL, this technique is further improved to form a burst-mode operation [2.47]. Since the MOSFETs operates on/off during burst-mode operation, a short start-up time would ensure ZVS is achieved more quickly during voltage regulation process thereby reducing the switching loss.

A detailed description of a novel PLL ZVS controller is provided in Chapter IV.

2.4.2.2 Self-oscillating control

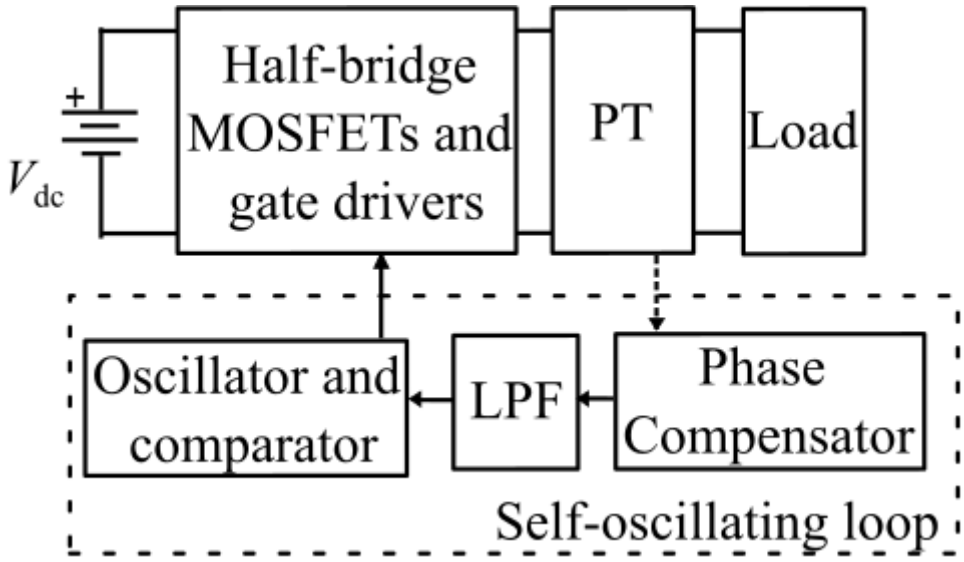


Fig. 2.11: Block diagram of self-oscillating control.

Since a phase shift is introduced by the PT owing to its band-pass filter behaviour, the self-oscillating control method is typically implemented by adjusting total phase shift to follow the resonant frequency, as shown in Fig. 2.11. The idea of this phase shift compensation is to track the resonant frequency change in a PT with cycle-by-cycle adjustments. An integer multiple of 2π is required for the entire control loop according to Barkhausen criterion, forming a self-induced oscillation, to ensure resonant current and PT input voltage are in-phase.

In [2.9], two self-oscillating controllers were presented with phase reference signal taken from resonant current and load voltage, respectively. The time delay introduced by each individual component within the feedback loop were considered. Subsequently, together with the phase delay introduced by the PT, a low-pass filter (LPF) was implemented in the feedback loop with a certain phase lag such that the total phase shift is 2π. This approach is further improved in [2.43], that a digital delay circuit was implemented such that its output is proportional to the phase delay of PT input voltage and resonant current. Therefore, the control circuit is able to self-adjust the entire phase shift of the

feedback loop, thereby ensuring the operating frequency follows the resonant frequency.

However, to control a PT-based converter, the self-oscillating control technique exhibits several drawbacks. When the resonant frequency changes, multi-period lock-in delays can be introduced, which is not desirable for fast tracking. In addition, this approach requires a self-induced oscillation to excite the PT vibration near the resonant frequency during system initialisation. Since the controller must operate as an oscillator and, during start-up, operating away from the PT's resonant frequency would significantly reduce the efficiency of the PT [2.8].

2.4.3 Output voltage regulation

In addition to high efficiency operation, a PT-based converter is often required to provide output voltage regulation under large load and input voltage variations, and this is normally accomplished by a second feedback loop. Careful design consideration should be taken since voltage gain are load, temperature and frequency dependent [2.7].

2.4.3.1 Pulse-width and pulse-frequency modulation

Pulse-width modulation (PWM) and pulse-frequency modulation (PFM) are commonly used control methods for PT-based converter. For PWM, the gate-drive signals are adjusted by the controller with asymmetric duty cycle according to the regulation requirement. In terms of PFM, by comparing the phase error signal (proportional to phase difference between input and output voltage) and output voltage, a reference signal is generated to control the voltage-controlled oscillator, thereby regulating the output voltage through operating frequency change.

For step-up applications, PFM is often used as it simply tracks the desired frequency to maximise the output voltage, and power transferred to the load is maximised when PT voltage gain reaches its maximum [2.18]. For step-down converters, since the line and load regulation are normally required with high efficiency operation, both PFM and PWM have been used extensively [2.48]–[2.50]. In [2.48], a PWM controller was employed and the output regulation was achieve by fixing the switching frequency with a asymmetric duty cycle. An 80% efficiency was achieved with 20V output over 100V-250V input. In [2.49], to regulate the output at 20V, the operating frequency was shifted away from the resonant frequency to cover 360V-420V input voltage variation, and 81% efficiency was achieved.

However, to control a PT-based converter, both PWM and PFM exhibit fundamental issues. For PWM, since resonant frequency drifts due to load and temperature variation, a fixed operating frequency during output regulation would significantly reduce the PT efficiency as it operates away from the primary resonant frequency. In terms of PFM, to maintain a constant output voltage, the operating frequency is significantly shifted away from the resonant frequency in order to compensate load and input voltage variation, resulting in a reduced PT efficiency.

2.4.3.2 Burst-mode control

To regulate the output voltage of a PT-based converter, a burst-mode control technique has been reported in [2.47][2.51]. The energy is transferred in modulated bursts according to the regulation requirement. A burst signal is generated by comparing the output voltage to voltage regulation limit, thereby controlling the on/off periods of the MOSFET switches. A typical burst-mode operation is shown in Fig. 2.12.

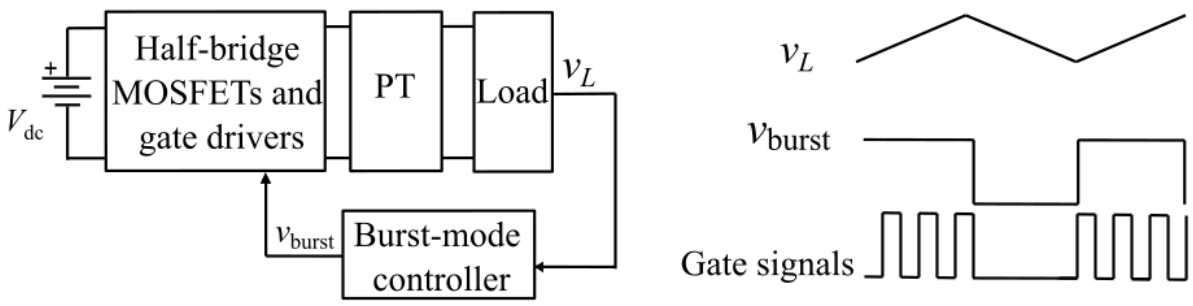


Fig. 2.12: Burst mode operation.

As an alternative to regulate output voltage, the burst-mode control modulation has been shown to provide superior performance when compared with PFM and PWM since it provides a higher efficiency and lower harmonics [2.52][2.53]. In [2.52], the burst-mode controller was implement separately from the ZVS controller. A LPF was used before and after the hysteresis comparator to smooth the input reference signal and to delay the burst signal before it being applied to the gate driver (to prevent driver turning on and off at the same switching cycle). The output voltage was regulated at 45V with a load variation of 250kΩ-900kΩ. In [2.3], a 15V output regulation was achieved for load range from 1-10W with 80% efficiency. The dynamic response of the filter capacitor was analysed, and it was indicated that the hysteresis window (i.e. burst signal frequency) should be adjusted to compensate resonant frequency variation and components tolerances within a low system noise level.

However, unlike traditional converters, a PT-based converter under burst-model operation exhibits several problems: 1) since the resonant frequency changes due to load and temperature variation during regulation process, the hysteresis window should be adjusted accordingly to obtain a desired burst signal frequency [2.3], thereby satisfying regulation requirements; 2) since PT resonance cannot start and stop instantly due to its mechanical vibration nature, switching transition times are introduced at the PT start-up and stop, resulting in time delay and non-

linear voltage regulation [2.54]. Therefore, it is necessary to reduce the start-up and stop transition time in order to improve the regulation accuracy.

2.4.4 Resonant current estimation

A practical issue encountered in PT-based converters is that the resonant current is internal to a PT and cannot be measured directly. Figure 2.8 shows an inductorless half-bridge driving the Mason equivalent circuit of a PT. The current i_{L1} is equivalent to the vibration velocity and circulates within the PT and, therefore, it is not easily measurable. It is important to estimate the resonant current since effective signs (e.g. zero-crossings) from resonant current can be used to indicate ZVS thereby providing a reference signal for the control circuit. Several techniques have been presented in the literature.

2.4.4.1 Estimation through voltage differentiation

This current estimation technique was first proposed in [2.9] and has been used in [2.41][2.43][2.13][2.47]. The idea of this type of current estimator is to reconstruct resonant current using the PT input capacitor current $i_{C\text{in}}$ and PT input current i_{in}, as shown in Fig. 2.13. The PT input current is sensed by measuring the voltage across R_{B} and a scaled version of PT input capacitor current is sensed by measuring the voltage across R_{A}. Therefore, the resonant current can be regenerated through the combined current signals with proper selection of sensing resistors.

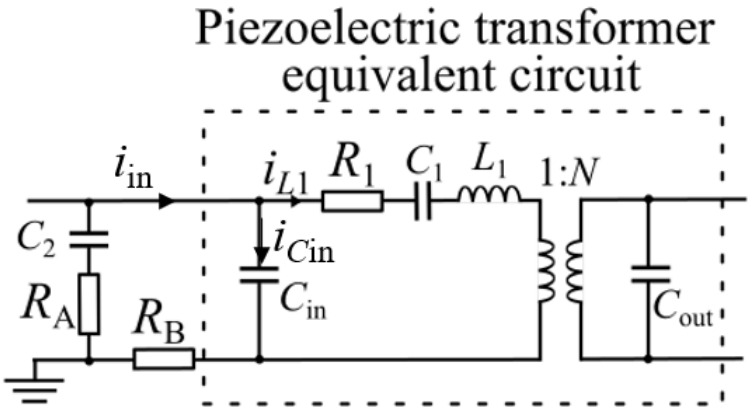


Fig. 2.13: Resonant current estimation with voltage differentiator.

However, to ensure a high efficiency operation, a PT usually operates at a matched load condition which gives the lowest resonant current (around 100mA-200mA), the sensed signals are therefore sensitive to system noise and may cause inaccurate current estimation [2.43]. Furthermore, since this estimation technique is implemented at the input section of the PT, the sensed current signals is also affected by the MOSFETs switching event, which again leads to inaccuracy of current estimation [2.13].

2.4.4.2 Anti-parallel diode

Compared with voltage differentiator current estimator, a simpler estimation technique was proposed in [2.18][2.42], which consists of anti-parallel diodes. Therefore, instead of reconstructing resonant current, the effective signs of resonant current, such as zero-crossings and phase, are used as ZVS indicators.

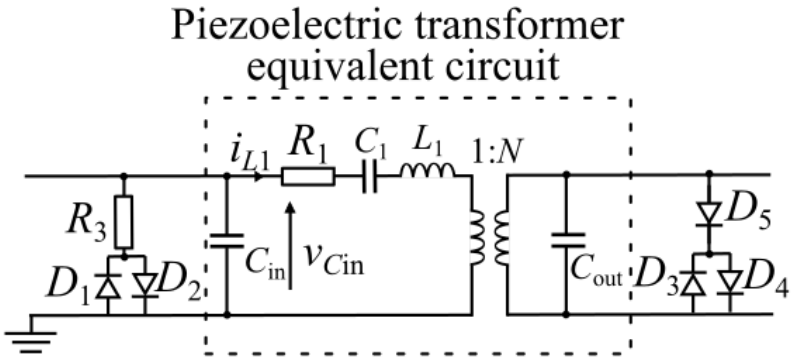


Fig. 2.14: Resonant current estimation with anti-parallel diodes from [18].

In [2.18], the anti-parallel diodes were implemented at both input and output section of a PT, as shown in Fig. 2.14. At PT output section, since the diode D_5 switches off when resonant current i_{L1} changes the polarity, the instant of direction reversal can be used to indicate the phase of resonant current. At PT input section, the anti-parallel diodes are implemented to detect the phase of PT input voltage $v_{C\text{in}}$. Subsequently, the phase difference between $v_{C\text{in}}$ and i_{L1} can be measured and ZVS is achieved when they are in phase.

However, the cross talk between primary and secondary side significantly reduces the system robustness to noise and causes inaccurate phase detection from the phase comparator. Moreover, an extra compensation circuit (e.g. LPF and bias network) should be employed due to the phase shift caused by the parasitic capacitances of the diodes.

2.5 Converter modelling

Before experimental implementation of the circuit, it is important to predict the circuit behaviour using analytical expressions and compared with simulation results. Several converter techniques have been proposed in the literature to improve the accuracy of the circuit prediction and provide fast circuit analysis.

2.5.1 Cyclic modelling

The cyclic modelling is a time-domain modelling technique which is described as an extended Floquet-based method [2.55], by determining steady-state values of the state variables. It is an alternative to integration-based [2.33] methods and the state-space averaging technique [2.56] often used to model the periodical switching networks. For a typical periodically switched system, the state-vector at the start and the end of the switching period should be equal, thus

$$x(t)=x(t+gT) \tag{2.6}$$

where T is the switching period of a single cycle and g is an integer corresponding to a whole number of cycles.

In general, a periodical switching network can be considered as a non-linear state-variable model that is derived from the circuit parameters. Subsequently, depending on the conduction status of the MOSFET switches, the circuit is divided into m operating modes. Hence, the non-linear state-variable model can be decomposed into a piecewise linear model according to the mode of operating. The state-variables x of each operating mode is found by

$$\dot{x} = \boldsymbol{A_i} x + \boldsymbol{B_i} \tag{2.7}$$

where $x(t)$ is the state vector, i is the mode index, $\boldsymbol{A_i}$ and $\boldsymbol{B_i}$ are the dynamical matrix and the input vector, respectively.

Therefore, for $t_{i-1} \leq t \leq t_{i,}$ the state vector $x(t)$ at $t=t_i$ can be solved from the state vector value at t_{i-1} by evaluating the evolution of the state vector

$$\begin{aligned} x(t_i) &= e^{\boldsymbol{A_i}(t_i - t_{i-1})} x(t_{i-1}) + \int_{t_{i-1}}^{t_i} e^{\boldsymbol{A_i}(t-\tau)} \boldsymbol{B_i} d\tau \\ &= e^{\boldsymbol{A_i} d_i T} x(t_{i-1}) + \boldsymbol{A_i^{-1}} (e^{A_i d_i T} - I) B_i \\ &= \Phi_{\boldsymbol{i}} x(t_{i-1}) + \boldsymbol{\Gamma_i} \end{aligned} \tag{2.8}$$

where I is the identity matrix, $\boldsymbol{\Phi_i} = \boldsymbol{\Phi}(t_{i,} t_{i-1}) = e^{A_i d_i T}$, $\boldsymbol{\Gamma_i} = \boldsymbol{A_i^{-1}}(e^{A_i d_i T} - \boldsymbol{I})\boldsymbol{B_i}$, $d_i = (t_{i,} - t_{i-1})/T$ is the duty cycle for the i^{th} mode and the period $T=1/f$.

Subsequently, for a periodic system with m operating modes, the state-vector of mode 1, 2 and m is given by

$$x(t_1) = \Phi_1 x(t_0) + \Gamma_1 \tag{2.9}$$

$$\begin{aligned} x(t_2) &= \Phi_2 x(t_1) + \Gamma_2 \\ &= \Phi_2(\Phi_1 x(t_0) + \Gamma_1) + \Gamma_2 \\ &= \Phi_2\Phi_1 x(t_0) + \Phi_2\Gamma_1 + \Gamma_2 \end{aligned} \tag{2.10}$$

$$\begin{aligned} x(t_m) &= \Phi_m x(t_{m-1}) + \Gamma_m \\ &= \Phi_m(\Phi_{m-1} x(t_{m-2}) + \Gamma_{m-1}) + \Gamma_m \\ &= \Phi_m\Phi_{m-1}\cdots\Phi_1 x(t_0) + \Phi_m\Phi_{m-1}\cdots\Phi_2\Gamma_1 + \\ &\quad \Phi_m\Phi_{m-1}\cdots\Phi_3\Gamma_2 + \cdots + \Phi_m\Gamma_{m-1} + \Gamma_m \end{aligned} \tag{2.11}$$

Therefore, by using the periodical nature of the system, $x(t_m)=-x(t_0)$, the initial condition of the system can be found by

$$\begin{aligned} x(t_0) = [-I - \Phi_m\Phi_{m-1}\cdots\Phi_1]^{-1}[&\Phi_m\Phi_{m-1}\cdots\Phi_2\Gamma_1 \\ &+ \Phi_m\Phi_{m-1}\cdots\Phi_3\Gamma_2 + \cdots + \Phi_m\Gamma_{m-1} + \Gamma_m] \end{aligned} \tag{2.12}$$

Finally, with the circuit operating modes and time duration of each mode, the state-variables at a given time of operation can be evaluated using equation (2.7), (2.11) and (2.12).

This technique was used in [2.57] to estimate the ZVS ability of a half-bridge driven inductorless PT inverter and in Chapter VI of this this thesis it is applied to analyse a novel simultaneous ZVS-output voltage regulation control method in an H-bridge-driven inductorless converter.

2.5.2 Describing function

Unlike cyclic modelling which estimates the switching behaviour of the circuit based on the circuit operating mode and time duration, the describing function is a frequency-domain modelling technique that describes the switching characteristics with analytical expressions. It has been extensively used in PT-based converters [2.33] as well as other types of resonant [2.58]–[2.60]

In [2.33], a describing function was used to indicate ZVS characteristics of a PT-based converter. The resonant current and PT input voltage were provided initially as a function of key circuit parameters (e.g. switching frequency, PT input capacitance, phase angle) and converted into ZVS metric using the Euler equation. Subsequently, with fundamental component extraction and energy balance approach, the ZVS metric was further update with desired circuit parameters (e.g. input-to-output capacitance ratio, load, operating frequency and deadtime). Finally, the ZVS characteristics and optimum operating regions were indicated regarding switching frequency and load. A critical criterion was established to provide a guideline for PT and converter design in order to achieve ZVS.

Compared with cyclic modelling approach that provides a numerical solution to analysis circuit under ZVS, the describing function technique offers a quantitative measurement of the PT-based converter's ability to achieve ZVS and a better understanding of fundamental mechanisms involved.

2.6 New challenges and contribution

PTs transfer energy using electromechanical coupling from input to output section. It brings a great advantage to achieve high electrical efficiency (compared with conventional LCLC family) and high temperature operation (compared with traditional transformers). As such it is a multidisciplinary research field which involving specialisms in electronics, mechanics and materials.

2.6.1 Challenges for PT design

To maximise the PT performance in terms of coupling and piezoelectric coefficients, a PZT material with different poling directions at MPB should be optimised. In addition, the impact of spurious vibration should be reduced, such

as changing the dimensions and geometry of the piezoelectric device [2.61] and ensuring spurious modes have negligible effect on the main vibration mode [2.25]. However, this is an area which should be addressed by materials scientists.

2.6.2 Challenges for PT-based converter control

To maximise the efficiency and output power of a PT-based converter, optimum frequency should be continuously tracked since resonant frequency drifts due to load temperature variation. Moreover, ZVS region is further reduced when an inductorless configuration is applied. All of these impose strict requirements on the control circuit design. In terms of output voltage regulation, conventional PWM and PFM control cannot be applied for a PT-based converter and burst-mode control still needs to be improved to compensate start-up and stop transition due to the non-instant stop behaviour of a PT caused by the device vibration. In addition, to provide feedback reference for achieving ZVS, resonant current should be estimated since it is internal to a PT and cannot be measured directly. Additional efforts should be applied to improve system robustness to noise thereby preventing inaccurate current estimation.

2.6.3 Challenges for PT-based converter modelling

To ensure ZVS operation for a PT-based resonant converter, the circuit operating conditions should be carefully examined by analytical models, especially for an inductorless configuration, since deadtime period and resonant current are limited and input-to-output capacitance ratio is critical [2.33]. In addition, to guarantee ZVS is continuously achievable when regulating the output voltage, mathematical models are necessary to evaluate the operating region over which the frequency, load and deadtime are considered. This in turn poses a challenge for the control circuit design for achieving simultaneous ZVS and voltage regulation.

2.6.4 Opportunities and contribution

This thesis addresses some of these aforementioned challenges in the following way:

- The research provides a resonant-frequency tracking zero-voltage switching controller for inductorless half-bridge-driven PT power supplies by using a PLL ZVS controller (Chapter IV) to synchronise to estimated resonant currents (Chapter III)
- Output voltage regulation is provided by incorporating the PLL ZVS controller within a burst mode hysteresis control loop (Chapter V)
- Simultaneous ZVS and output regulation is achieved through a novel inductorless H-bridge drive (Chapter VI) which provides a 3-level (V_{dc}, 0V, $-V_{dc}$) input voltage to the PT where the 0V level provides the output voltage regulation and a PLL is employed for resonant frequency tracking and ZVS control.

2.7 Chapter conclusions

In this Chapter, a literature review is presented in fundamental topics regarding the proposed research. The latest PT material and device modelling methods are described in detail, and available techniques for PT-based converter design, control and modelling are evaluated.

Although the inductorless half-bridge topology is the best candidate for step-down and high-power applications, the ZVS control techniques together with resonant current estimation methods, however, still need great efforts to be developed in order to achieve ZVS (demonstrated in Chapter III and Chapter IV). Methods of output regulation are reported, and practical issues due to PT vibration should be compensated to obtain an accurate voltage regulation

(proposed in Chapter V). Techniques to model PT-based converters, which are required for predicting ZVS and voltage regulation region, are reported. It is highlighted that simultaneous ZVS and output regulation should be achieved continuously over the applicable of operating conditions, and complex control circuitry is required since circuit parameters should be controlled simultaneously (e.g. deadtime, load and frequency) (proposed in Chapter VI).

2.8 References

[2.1] H. Liu, J. Zhong, C. Lee, S. W. Lee, and L. Lin, “A comprehensive review on piezoelectric energy harvesting technology: Materials, mechanisms, and applications,” *Appl. Phys. Rev.*, vol. 5, no. 4, 2018.

[2.2] Vasic, Dejan, and François Costa. " . Vasic and F. Costa, "Energy recovery DC/AC converter for piezoelectric transformer," *2014 16th European Conference on Power Electronics and Applications*, 2014, pp. 1-10,

[2.3] Y. Liu, D. Vasic, F. Costa and D. Schwander, "Piezoelectric 10W DC/DC converter for space applications," *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, 2011, pp. 1-7.

[2.4] Chu, Sheng-Yuan, Te-Yi Chen, I-Ta Tsai, and Walter Water. "Doping effects of Nb additives on the piezoelectric and dielectric properties of PZT ceramics and its application on SAW device." *Sensors and Actuators A: Physical* 113, no. 2, pp:198-203. 2004.

[2.5] O. Ohnishi, H. Kishie, A. Iwamoto, Y. Sasaki, T. Zaitsu and T. Inoue, "Piezoelectric ceramic transformer operating in thickness extensional vibration mode for power supply," *IEEE 1992 Ultrasonics Symposium Proceedings*, 1992, pp. 483-488 vol.1.

[2.6] T. Zaitsu, T. Inoue, O. Ohnishi and A. Iwamoto, "2 MHz power converter with piezoelectric ceramic transformer," *14th International Telecommunications Energy Conference - INTELEC '92*, 1992, pp. 430-437.

[2.7] E. L. Horsley, M. P. Foster and D. A. Stone, "State-of-the-art Piezoelectric Transformer technology," *2007 European Conference on Power Electronics and Applications*, 2007, pp. 1-10,

[2.8] E. L. Horsley, Modelling and analysis of radial mode piezoelectric transformers and inductor-less resonant power converters, Ph.D thesis, University of Sheffield, 2011.

[2.9] M. S. Rodgaard, "Piezoelectric transformer based power converters design and control." Ph.D thesis, Technical University of Denmark, 2012.

[2.10] K. Brebol, "Piezoelectric transformer," *U.S. Patent 6,707,235,*2004.

[2.11] A. V. Carazo, "Piezoelectric transformers: An historical review," *Actuators*, vol. 5, no. 2, pp. 12. Multidisciplinary Digital Publishing Institute, 2016.

[2.12] V. C. Alfredo, "50 years of piezoelectric transformers. Trends in the technology," in *Proc. Symp. D Mater. Devices Smart Syst.*, vol. 785, 2003, pp.33-44.

[2.13] Z. Yang, J. Forrester, J. N. Davidson, M. P. Foster, and D. A. Stone, "Resonant current estimation and phase-locked loop feedback design for piezoelectric transformer-based power supplies," *IEEE Trans. Power Electron.*, pp. 1–1, 2020.

[2.14] Texas Instrument,"Power transformer design", 2020.

[2.15] P. Laoratanakul and K. Uchino, "Designing a radial mode laminated piezoelectric transformer for high power applications," *14th IEEE International Symposium on Applications of Ferroelectrics, 2004. ISAF-04. 2004*, 2004, pp. 229-232.

[2.16] R. L. Lin, Piezoelectric transformer characterization and application of electronic ballast. Ph.D thesis, Virginia Polytechnic Institute and State University, 2001.

[2.17] J. Du, J. Hu, and K. J. Tseng, “High-power, multioutput piezoelectric transformers operating at the thickness-shear vibration mode,” *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 51, no. 5, pp. 502–509, 2004.

[2.18] D. Guyomar, C. Magnet, E. Lefeuvre, and C. Richard, “Power capability enhancement of a piezoelectric transformer,” *Smart Mater. Struct.*, 2006.

[2.19] S. Ben-Yaakov and S. Lineykin, “Maximum power tracking of piezoelectric transformer HV converters under load variations,” *IEEE Trans. Power Electron.*, 2006.

[2.20] I Kartashev, I., T. Vontz, and H. Florian. "Regimes of piezoelectric transformer operation." *Measurement Science and Technology* 17, no. 8. pp:2150, 2006.

[2.21] A. P. Rane and T. N. Date, "Design and simulation of piezoelectric transformer based LED driver," *2016 International Conference on Global Trends in Signal Processing, Information Computing and Communication (ICGTSPICC)*, 2016, pp. 660-662.

[2.22] Y. C. Wang *et al*., "Theory and experiment of high voltage step-up ratio disk type piezoelectric transformer for LCD-TV," *IEEE International*

Conference on Mechatronics, 2005. ICM '05., 2005, pp. 284-287.

[2.23] E. L. Horsley, A. V. Carazo, M. P. Foster and D. A. Stone, "A Lumped Equivalent Circuit Model for the Radial Mode Piezoelectric Transformer," *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, 2009, pp. 1747-1753.

[2.24] Pulpan, P., J. Erhart, and O. Štípek. "Analytical modeling of piezoelectric transformers." *Ferroelectrics,* 2007, no. 1, pp:204-215,2007.

[2.25] C. Y. Lin, Design and analysis of piezoelectric transformer converters, Ph.D thesis, Virginia Polytechnic Institute and State University, 1997.

[2.26] J. Forrester, J. N. Davidson, M. P. Foster and D. A. Stone, "Influence of Spurious Modes on the Efficiency of Piezoelectric Transformers: A Sensitivity Analysis," in *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 617-629, 2021,

[2.27] Y. W. Yang, *et al* "Vibration-based energy harvesting with a clamped piezoelectric circular diaphragm: analysis and identification of optimal structural parameters." *Smart Materials and Structures* 26, no. 4, 2017.

[2.28] D. Bath and A. Salehian, “A novel 3D folded zigzag piezoelectric energy harvester; Modeling and experiments,” *Smart Mater. Struct.*, vol. 28, no. 2, 2019.

[2.29] R. Dauksevicius, A. Kleiva, and V. Grigaliunas, “Analysis of magnetic plucking dynamics in a frequency up-converting piezoelectric energy harvester,” *Smart Mater. Struct.*, vol. 27, no. 8, 2018.

[2.30] F. E. Bisogno *et al.,* "Comparison of resonant topologies for step-down

applications using piezoelectric transformers," *2004 IEEE 35th Annual Power Electronics Specialists Conference*, 2004, pp. 2662-2667, vol.4.

[2.31] H. Schwarzmann, T. Erlbacher, A. J. Bauer, H. Ryssel and L. Frey, "Amplitude Modulated Resonant Push-Pull Driver for Piezoelectric Transformers in Switching Power Applications," *2012 7th International Conference on Integrated Power Electronics Systems (CIPS)*, 2012, pp. 1-5.

[2.32] E. L. Horsley, A. V. Carazo, N. Nguyen-Quang, M. P. Foster and D. A. Stone, "Analysis of Inductorless Zero-Voltage-Switching Piezoelectric Transformer-Based Converters," in *IEEE Transactions on Power Electronics*, vol. 27, no. 5, pp. 2471-2483, 2012.

[2.33] M. Sanz, P. Alou, R. Prieto, J. A. Cobos and J. Uceda, "Comparison of different alternatives to drive piezoelectric transformers," *APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition*, 2002, pp. 358-364 vol.1.

[2.34] M. P. Foster, J. N. Davidson, E. L. Horsley, and D. A. Stone, “Critical Design Criterion for Achieving Zero Voltage Switching in Inductorless Half-Bridge-Driven Piezoelectric-Transformer-Based Power Supplies,” *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 5057–5066, 2016.

[2.35] M. Shoyama, K. Horikoshi, T. Ninomiya, T. Zaitsu, and Y. Sasaki, “Steady-State Characteristics of the Push-Pull Piezoelectric Inverter.” *IEICE transactions on communications* , 1999, no. 8, pp:1318-1325.

[2.36] M. Sanz, P. Alou, R. Prieto, J. A. Cobos and J. Uceda, "Comparison of different alternatives to drive piezoelectric transformers," *APEC.*

Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition, 2002, pp. 358-364 vol.1.

[2.37] Sungjin Choi, Taeil Kim and B. H. Cho, "Design of half-bridge piezo-transformer converters in the AC adapter applications," *Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, 2005. APEC 2005.*, 2005, pp. 244-248 Vol. 1.

[2.38] R. L. Lin, F. C. Lee, E. M. Baker and D. Y. Chen, "Inductor-less piezoelectric transformer electronic ballast for linear fluorescent lamp," *APEC 2001. Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition* , 2001, pp. 664-669 vol.2,

[2.39] M. S. Roedgaard, M. Weirich and M. A. E. Andersen, "Forward Conduction Mode Controlled Piezoelectric Transformer-Based PFC LED Drive," in *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4841-4849, 2013.

[2.40] G. Ivensky, I. Zafrany and S. Ben-Yaakov, "Generic operational characteristics of piezoelectric transformers," *IEEE Transactions on Power Electronics*, vol. 17, no. 6, pp. 1049-1057, 2002,

[2.41] S. Nakashima, T. Ninomiya, H. Ogasawara and H. Kakehashi, "Piezoelectric-transformer inverter with maximum-efficiency tracking and dimming control," *APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition*, 2002, pp. 918-923 vol.2.

[2.42] M. Ekhtiari, T. Andersen, Z. Zhang and M. A. E. Andersen, "Digitized self-oscillating loop for piezoelectric transformer-based power converters," *2016 IEEE Applied Power Electronics Conference and*

Exposition (APEC), 2016, pp. 1430-1436.

[2.43] E. Minazara, D. Vasic and F. Costa, "Comparing piezoelectric transformer working with PLL and with nonlinear load approaches in DC-DC converter," *2007 European Conference on Power Electronics and Applications*, 2007.

[2.44] M. Ekhtiari, T. Zsurzsan, M. A. E. Andersen and Z. Zhang, "Optimum Phase Shift in the Self-Oscillating Loop for Piezoelectric-Transformer-Based Power Converters," in *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 8101-8109, 2018.

[2.45] M. Ekhtiari, Z. Zhang and M. A. E. Andersen, "State-of-the-art piezoelectric transformer-based switch mode power supplies," *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, 2014, pp. 5072-5078.

[2.46] M. P. Foster, J. N. Davidson, D. A. Stone, and R. Yappa, "A PLL controller for achieving zero voltage switching (ZVS) in inductorless half-bridge drive piezoelectric transformer resonant power supplies." *The Journal of Engineering*, no. 17, pp: 3639-3642, 2019.

[2.47] E. M. Baker, Weixing Huang, D. Y. Chen and F. C. Lee, "Radial mode piezoelectric transformer design for fluorescent lamp ballast applications," in *IEEE Transactions on Power Electronics*, vol. 20, no. 5, pp. 1213-1220, Sept. 2005.

[2.48] Z. Yang, J. N. Davidson, and M. P. Foster, "Output voltage regulation for piezoelectric transformer-based resonant power supplies using phase-locked loop," PEMD 2020, 2020, pp. 455–460.

[2.49] Myounghwan Ryu, Sungjin Choi, Sangmin Lee and B. H. Cho, "A new piezoelectric transformer driving topology for universal input AC/DC adapter using a constant frequency PWM control," *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC '06.*, 2006, pp. 4.

[2.50] S. Choi, M. Ryu, S. Lee and B. H. Cho, "Adaptive frequency control strategy for piezoelectric transformer in AC/DC adapter applications using phase detector," *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC '06.*, 2006, pp. 4.

[2.51] S. Hamamura, T. Ninomiya, M. Yamamoto and M. Katsuno, "Combined PWM and PFM control for universal line voltage of a piezoelectric transformer off-line converter," in *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 270-277, 2003.

[2.52] D. Vasic, Y. Liu, F. Costa and D. Schwander, "Piezoelectric transformer-based DC/DC converter with improved burst-mode control," *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 140-146.

[2.53] S. Chen and C. Chen, "ZVS Considerations for a Phase-Lock Control DC/DC Converter with Piezoelectric Transformer," *IECON 2006 - 32nd Annual Conference on IEEE Industrial Electronics*, 2006, pp. 2244-2248.

[2.54] Y. P. Liu, D. Vasic, F. Costa, W. J. Wu, and C. K. Lee, “Design of fixed frequency controlled radial-mode stacked disk-type piezoelectric transformers for DC/DC converter applications,” *Smart Mater. Struct.*, vol. 18, no. 8, 2009.

[2.55] D. Vasic, Y. P. Liu, D. Schwander, F. Costa, and W. J. Wu, “Improvement

of burst-mode control of piezoelectric transformer based DC/DC converter," *Smart Mater. Struct.*, vol. 22, no. 5, 2013.

[2.56] H. R. Visser and P. P. J. van den Bosch, "Modelling of periodically switching networks," *PESC '91 Record 22nd Annual IEEE Power Electronics Specialists Conference*, 1991, pp. 67-73,

[2.57] M. P. Foster, H. I. Sewell, C. M. Bingham, D. A. Stone, D. Hente, and D. Howe, "Cyclic-averaging for high-speed analysis of resonant converters," *IEEE Trans. Power Electron.*, vol. 18, no. 4, pp. 985–993, 2003.

[2.58] M. P. Foster, E. L. Horsley, and D. A. Stone. "Predicting the zero-voltage switching profiles of half-bridge driven inductor-less piezoelectric transformer-based inverters." *IET Power Electronics*, no. 7, pp: 1068-1073, 2012.

[2.59] M. P. Foster, C. R. Gould, A. J. Gilbert, D. A. Stone, and C. M. Bingham, "Analysis of CLL voltage-output resonant converters using describing functions," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1772–1781, 2008.

[2.60] H. I. Sewell, D. A. Stone and C. M. Bingham, "A describing function for resonantly commutated H-bridge inverters," in *IEEE Transactions on Power Electronics*, vol. 19, no. 4, pp. 1010-1021, 2004.

[2.61] M. P. Foster, H. I. Sewell, C. M. Bingham, D. A. Stone, and D. Howe, "Methodologies for the design of LCC voltage-output resonant converters," *IEE Proc. Electr. Power Appl.*, vol. 153, no. 4, pp. 559–567, 2006.

[2.62] R. Prieto, M. Sanz, J. A. Cobos, P. Alou, O. Garcia and J. Uceda, "Design considerations of multi-layer piezoelectric transformers," *APEC 2001*.

Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2001,vol. 2, pp. 1258-1263.

Chapter III

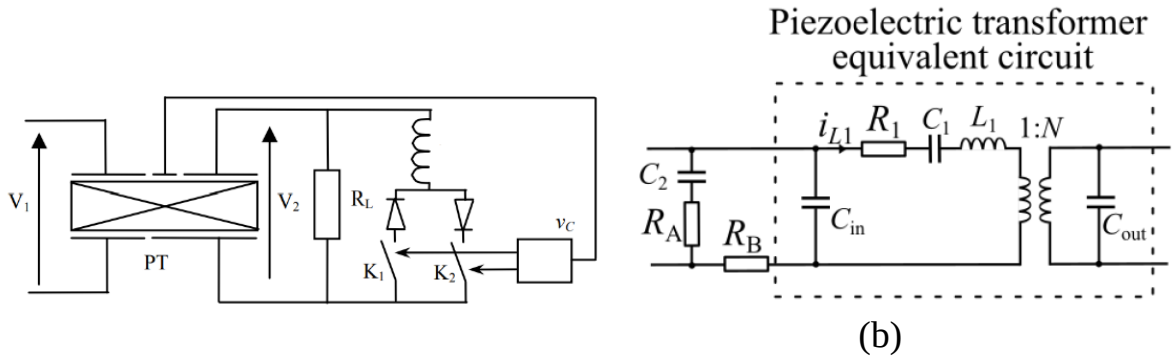
Resonant current estimation

In this chapter, three techniques are proposed for estimating the resonant current of a piezoelectric transformer. These approaches are described in detail so they may be used in the later chapters without full explanation. Initially, the basic operating principle of a PT-based inductorless half-bridge converter is presented. The typical mode of operation is indicated with ZVS and non-ZVS condition being demonstrated. Subsequently, input section current estimation is described with two types of estimating approaches. By reconstructing the resonant current and detecting zero crossings of the resonant current, synchronisation necessary for achieving ZVS are indicated and thus the feedback signal with ZVS information is provided for the control circuit. Analytical expressions are derived for estimated signals for each mode of operation. Output section current estimation is then described using concepts similar to the estimation techniques presented for input section. Finally, simulated results show good indication for estimating the resonant current and detecting the zero crossings.

3.1 Introduction

Since the resonant current is internal to a PT and cannot be measured directly, several techniques have been reported in literature to reconstruct the resonant current and detect the zero crossing points. In [3.2], an anti-parallel diode approach is presented at the secondary-side to indicate zero crossings of the resonant current, as shown in Fig. 3.1(a). A parallel inductor is employed to compensate the reactive current of the PT output capacitance while two switches are used to synchronising resonant current and secondary voltage. However, these mitigating steps increase the circuit size, increase cost and diminish the benefits

of using a PT. Hence, approaches which take feedback from the primary side have emerged as presented in [3.3]. Current and voltages from the Mason equivalent circuit model are estimated by sensing PT input current PT input capacitor current, as shown in Fig. 3.1(b), and the converter is switched when estimated reference signal passes through its zero-crossings or peaks. However, the resonant current of a PT-based converter is relatively small (less than 500 mA), the estimated current is highly sensitive to the system noise and MOSFET switching events [3.1].



(b)

Fig. 3.1: Resonant current methods reported in (a) [3.2] and (b) [3.3].

Therefore, in this chapter, techniques which provide good current estimation, improved robustness to noise and easy implementation are presented. Two different approaches are proposed to estimate the resonant current for a PT-based inductorless half-bridge converter. These approaches are initially employed at primary-side and further improved by implementing at the secondary-side to avoid MOSFET switching events thereby improving overall noise performance.

3.2 Operation of PT-based inductorless half-bridge resonant converter

PTs generally have high Q-factor band-pass filter-like characteristics when they operate close to their primary resonant frequency. There are typically several other modes but, for a well-designed PT operated close to its primary vibration

mode, these can be neglected. Their mechanical resonance and piezoelectric effect can be modelled by the simplified Mason-equivalent circuit as shown in Fig. 3.2. The gate drive signals are represented as v_{gs1} and v_{gs2}. i'_{L1} is the current flow at the PT output section and is related to the resonant current i_{L1} through the ideal transformer which has a ratio 1:*N*. An adequate deadtime is required to provide sufficient input capacitor charging time [3.1]. Insufficient deadtime results in the input capacitance voltage v_{Cin} failing to reach the DC input voltage V_{dc} before S_1 is turned on thereby generating switching losses [3.1].

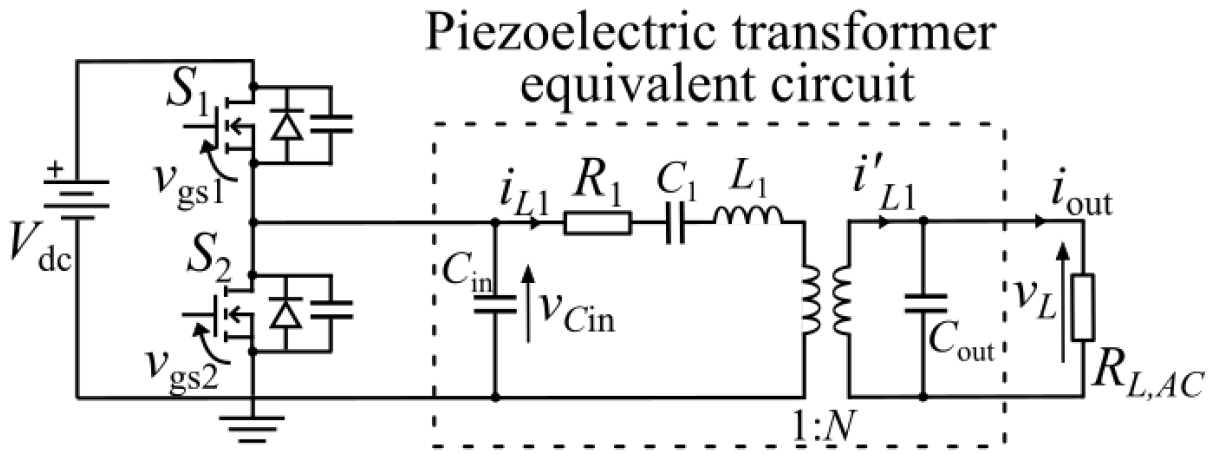


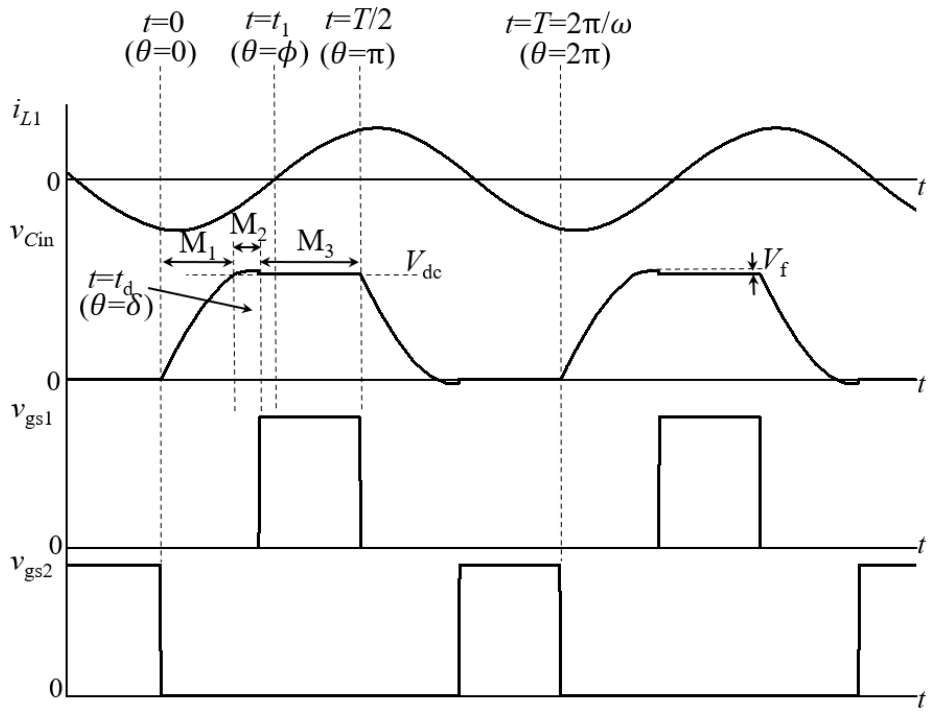
Fig. 3.2: PT-based inductorless half-bridge resonant converter with Mason equivalent circuit.

The typical operation for inductorless PT-based resonant converters exhibits one of following three modes during a half-cycle period.

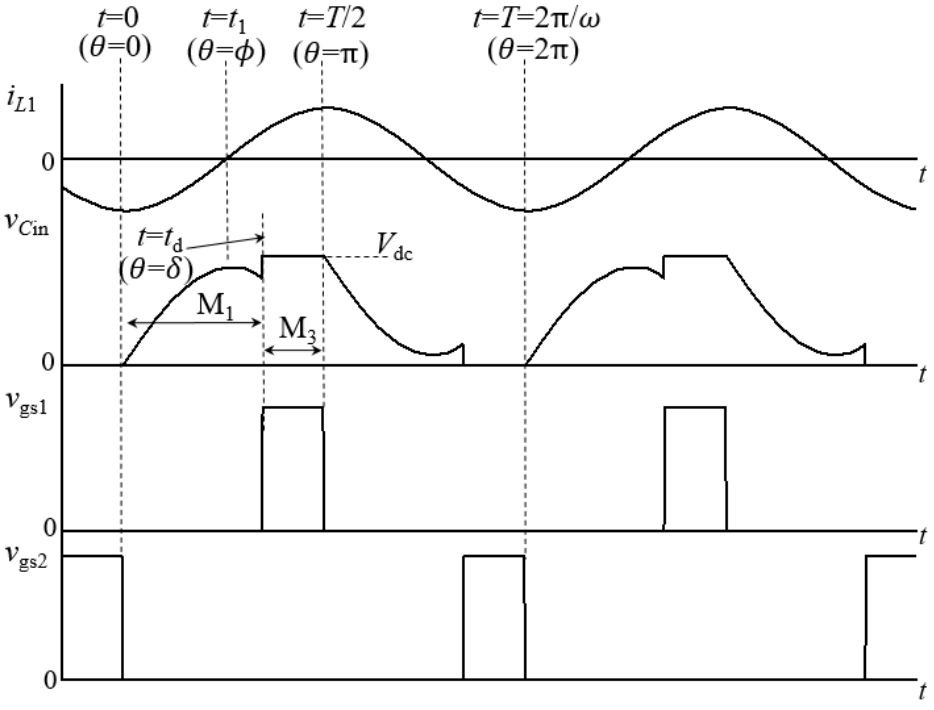
M1: S_1 and S_2 are off. PT input capacitance voltage v_{Cin} is charged (or discharged) towards the DC input voltage V_{dc} (or 0) by inductor current i_{L1}. This is the deadtime period.

M2: v_{Cin} has exceeded V_{dc} (or fallen below 0) and the body diode of S_1 (or S_2) is conducting, causing v_{Cin} to be V_{f} above V_{dc} (or V_{f} below 0), where V_{f} is the forward voltage drop of the MOSFET body diode.

M3: S_1 (or S_2) is on and v_{Cin} is maintained at V_{dc} (or 0).



(a)



(b)

Fig. 3.3: Switching waveforms of the inductorless half-bridge PT-based converter at (a) ZVS achieved and (b) ZVS not achieved.

The switching waveforms of a PT-based converter are shown in Fig. 3.3 under two different scenarios: ZVS achieved and ZVS not achieved. The high quality of the resonant tank allows one to assume i_{L1} is sinusoidal. Periods t_d (or δ radians) and t_1 (or ϕ radians) refer to the deadtime and phase delay between PT input capacitance voltage and resonant current, respectively. Voltages v_{gs1} and v_{gs2} correspond to half-bridge MOSFET gate drive signals.

In Fig. 3.3(a), ZVS is achieved following the mode sequence $M_1 \rightarrow M_2 \rightarrow M_3$. During the deadtime $0<t\leq t_d$, the PT input voltage v_{Cin} exceeds V_{dc}, inducing the conduction of the body diode of S_1 until S_1 is turned on at $t=t_d$ which is the positive going zero-crossing point of i_{L1}. Since the MOSFETs support bidirectional current flow, the reverse resonant current flows through S_1 during $t_d \leq t < t_1$. In contrast, the non-ZVS condition is shown in Fig. 3.3(b) with corresponding switching waveforms. Here, v_{Cin} does not reach V_{dc} during the deadtime and power dissipation occurs due to the near-instantaneous discharge of v_{Cin} as S_1 turns on.

A low input-to-output capacitance ratio ensures that the resonant current is able to charge or discharge the input capacitor quickly between the DC rails. This reduces the deadtime requirement. To guarantee ZVS for a PT-based inductorless topology, the design criterion developed in [3.4] is used in this work. The input-to-output capacitance ratio is set met $C_{\text{in}}/N^2C_{\text{out}} < 2/\pi$ with $\pi/2$ deadtime at matched load condition. The input capacitance voltage v_{Cin} is hence maximised at the end of the deadtime interval. In order for the ZVS criterion to be satisfied at the limit of the capacitor ratio, the resonant current must be in phase with the MOSFET gate drive signal thereby ensuring that deadtime starts at the negative peak of the resonant current. By starting the charge at the peak of the current waveform, the charge transfer is at its maximum. Operating with a matched load results in the lowest resonant current value because it corresponds to the highest

efficiency point as described in [3.5]. An unfortunate consequence of operating with a matched load is that it takes longer to charge the input capacitor during the deadtime period [3.4]. Therefore, if ZVS can be achieved at the matched load, then ZVS is achievable for all load conditions [3.4]. The matched load is given as

$$R_{L,AC} = \frac{1}{\omega_0 C_{\text{out}}} \tag{3.13}$$

Where ω_0 is the series resonant frequency.

3.3 Input side resonant current estimation

In this section, two current estimation techniques are described for connection at the primary side of the PT. Current estimator 1 has been previously described in [3.6], but it needs careful differential amplification and requires additional resistance. Subsequently, a new technique current estimator 2 is proposed, based on similar concepts but eliminates the need resistors and does not need a differential amplifier.

3.3.1 Current estimator 1: Voltage differentiator (CE1)

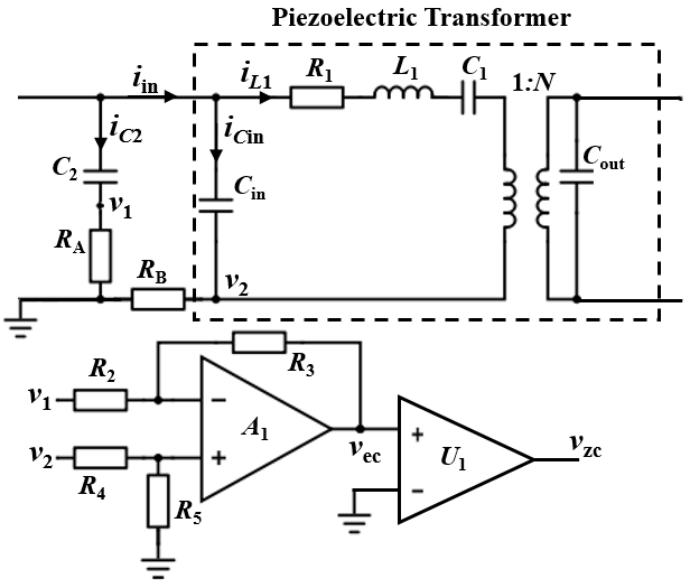


Fig. 3.4: Current estimator 1.

Current estimator 1, shown in Fig. 3.4, differentiates the PT input voltage $v_{C\text{in}}$ to estimate the capacitor current $i_{C\text{in}}$ during deadtime. C_2 and R_A form an approximate differentiator if $R_\text{A}C_2 \ll T$, where T is the switching period. The mid-point voltage v_1 provides a derivative signal of the PT input voltage $v_{C\text{in}}$. During the deadtime, the capacitor currents for C_in and C_2 can be found (assuming $R_\text{A}C_2 \ll T$ and $R_\text{B}C_\text{in} \ll T$) from

$$i_{C\text{in}} = C_\text{in}\frac{\mathrm{d}v_{C\text{in}}}{\mathrm{d}t} \tag{3.14}$$

$$i_{C2} = C_2\frac{\mathrm{d}v_{C\text{in}}}{\mathrm{d}t} \tag{3.15}$$

$$v_1 = i_{C2}R_\text{A} \tag{3.16}$$

Solving equation (3.14) to (3.16) results in

$$v_1 = \frac{R_\text{A}C_2}{C_\text{in}}i_{C\text{in}} \tag{3.17}$$

which shows that v_1 is a scaled version of the PT input capacitor current $i_{C\text{in}}$.

The PT input current i_in is detected by the sensing resistor R_B. Since

$$i_\text{in} = i_{C\text{in}} + i_{L1} \tag{3.18}$$

$$v_2 = (i_{L1} + i_{C\text{in}})R_B \tag{3.19}$$

Substituting equation (3.16) into (3.18) and rearranging provides the equation (3.19) for the resonant current

$$i_{L1} = \frac{v_2}{R_B} - \frac{v_1 C_\text{in}}{R_A C_2} \tag{3.20}$$

The resonant current, i_{L1}, can be estimated using a differential amplifier. R_2, R_3, R_4 and R_5 set the gain as

$$v_{\mathrm{ec}} = v_2 \frac{R_5/(R_4 + R_5)}{R_2/(R_2 + R_3)} - v_1 \frac{R_3}{R_2} \tag{3.21}$$

Comparing equation (3.20) and (3.21), it can be seen that with careful selection of component values, $v_{\mathrm{ec}} \propto i_{L1}$.

It should be noted that the total effective capacitance at the PT input is increased since C_2 is introduced, thereby ZVS is harder to achieve. Therefore, C_2 should be much smaller than C_{in} in order to minimise its effect on PT performance and the ZVS capability [3.7] (e.g. a factor of ten times smaller).

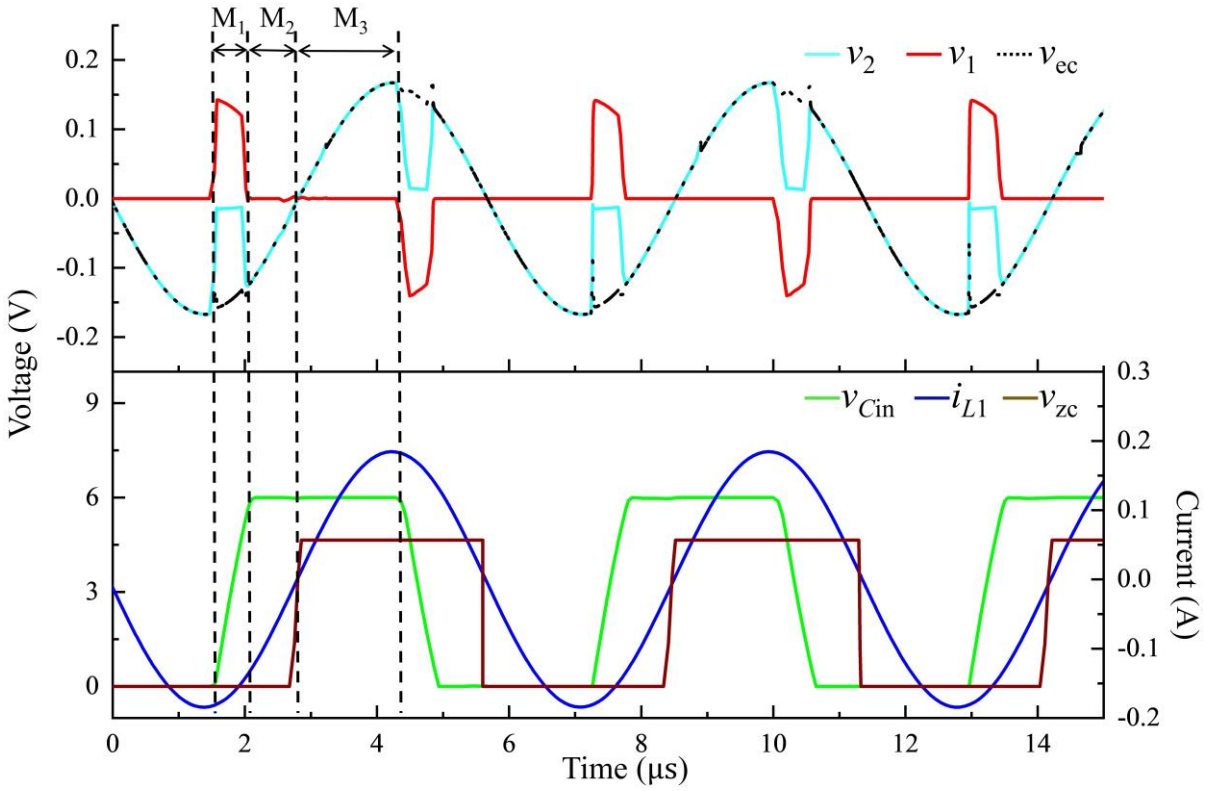


Fig. 3.5: Switching waveforms of current estimator 1.

The operating waveforms of current estimator 1 under ZVS are shown in Fig. 3.5. During M_1, the PT input current i_{in} and its scaled representation v_2 remain almost

zero since the PT input capacitor C_{in} is being charged towards V_{dc}. The current through C_{in} and its scaled version v_1 increase accordingly. Once the PT input capacitor has been fully charged, i_{in} is dominated by resonant current i_{L1} which flows in the reverse direction and the body diode of the MOSFET conducts during M_2. During M_3, v_{Cin} is maintained constant at V_{dc}, therefore its derivative signal v_1 is zero. Voltages v_1 and v_2 are combined to reconstruct the estimated resonant current v_{ec} as shown in Fig. 3.5. A sign-detecting comparator U_1 provides feedback v_{zc} for the controller.

3.3.2 Current estimator 2: Anti-parallel diode sign detector (CE2)

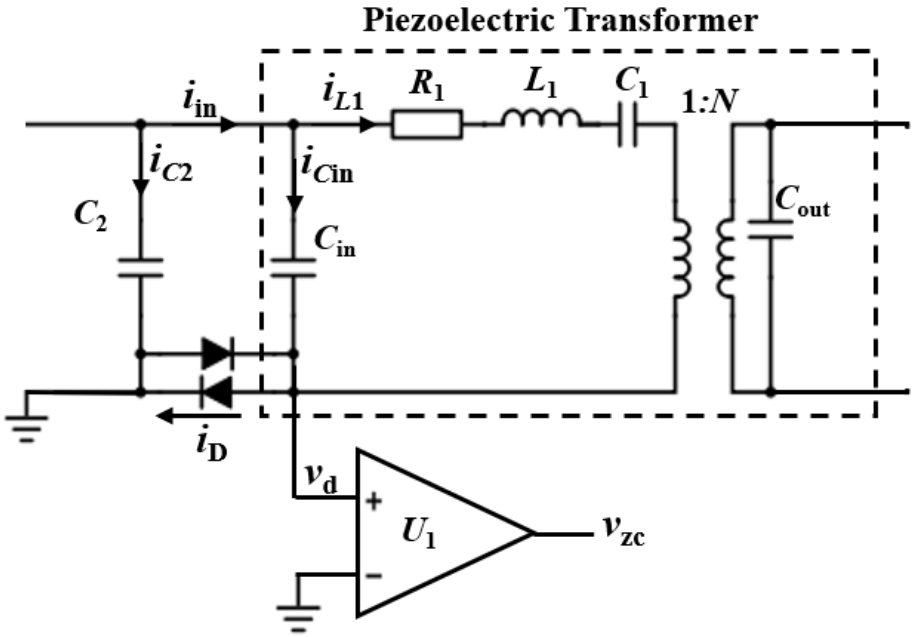


Fig. 3.6: Current estimator 2.

Current estimator 2, shown in Fig. 3.6, consists of two anti-parallel diodes coupled to the input section of the PT. These diodes are used to detect the zero-crossing of the resonant current. Each diode current is described by the Shockley equation

$$i_D = I_s\left(\exp\left(\frac{qv_d}{nkT_a}\right) - 1\right) \tag{3.22}$$

where v_d is the voltage across the diode, T_a is absolute temperature, k is Boltzmann's constant, n is the emission coefficient, q is the electronic charge and I_s is the reverse saturation current. Employing equation (3.22) to the anti-parallel diodes configuration results in (neglecting the "-1" term)

$$i_{\mathrm{d}} = 2I_{\mathrm{s}} \sinh\left(\frac{qv_d}{nkT_a}\right) \tag{3.23}$$

A silicon fast switching diode 1N4148 is employed in this design for easy sign detection of the input current. The reverse-recovery time of 1N4148 is 4ns which is negligible in comparison to the 6μs switching period. There is negligible change in the conducting diode's forward voltage when the current is above 10mA. Since this is much less than the typical current (above 50mA), we can safely assume the forward voltage is constant and merely changes sign with current. Similar to current estimator 1, a capacitor C_2 is connected in parallel to PT input to as shown in Fig. 3.6 and it is chosen to be much smaller than C_{in} (e.g. ten times smaller) in order to minimise its effect on ZVS capability [7]. Note that no series resistor is required.

The anti-parallel diode current and PT input capacitor current are given as

$$i_{\mathrm{d}} = i_{C\mathrm{in}} + i_{L1} \tag{3.24}$$

$$i_{C\mathrm{in}} = -\begin{cases} i_{L1} + i_{C2}, & \mathrm{M1} \\ 0, & \mathrm{M2, M3} \end{cases} \tag{3.25}$$

therefore

$$\frac{d}{dt} v_{C\mathrm{in}} = \frac{i_{C2}}{C_2} = \frac{i_{C\mathrm{in}}}{C_{\mathrm{in}}} \tag{3.26}$$

Solving (3.24)-(3.26),

$$i_{\mathrm{d}} = i_{L1} \cdot \begin{cases} 1 + \dfrac{C_2}{C_{\mathrm{in}}}, & \mathrm{M1} \\ 1, & \mathrm{M2, M3} \end{cases} \tag{3.27}$$

Therefore, i_{d} and i_{L1} share the same polarity under all modes.

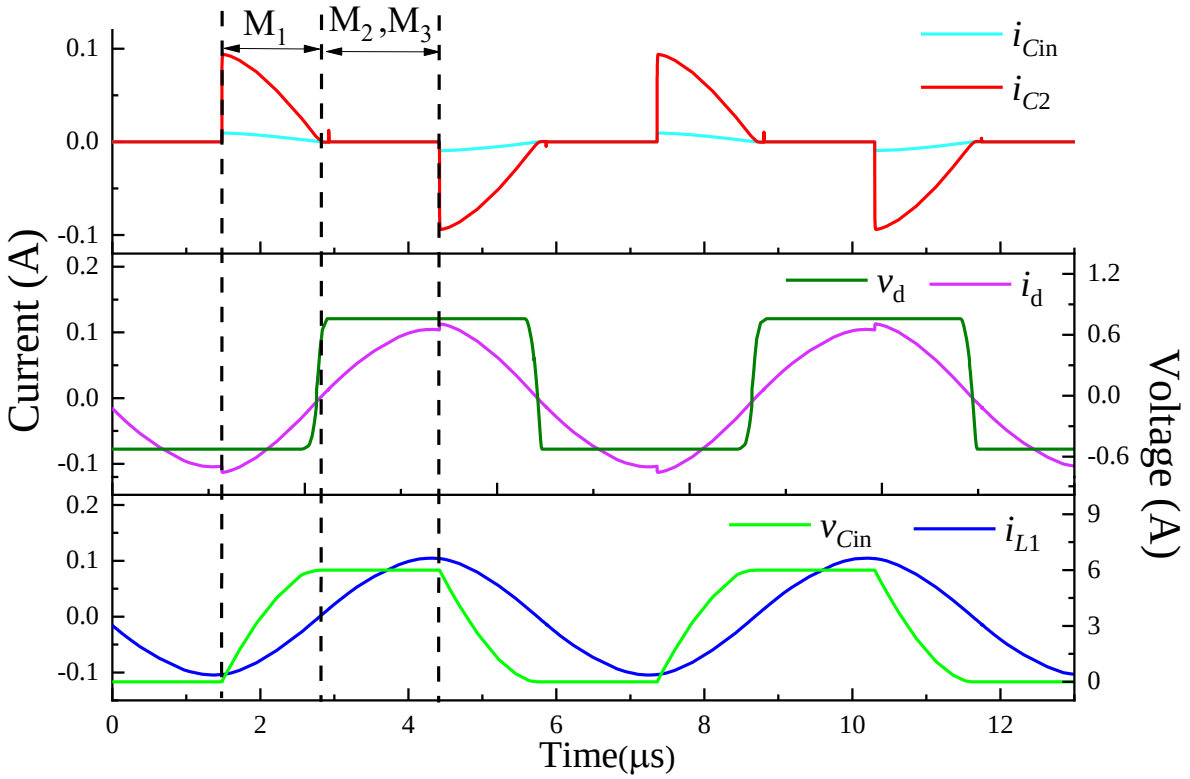


Fig. 3.7: Switching waveforms of current estimator 2.

Circuit operating waveforms of current estimator 2 are shown in Fig. 3.7. During M_1, current is flowing out of the resonant circuit and so both C_2 and C_{in} are charged positively towards V_{dc} and the capacitor current i_{C2} is proportional to $i_{C\mathrm{in}}$. Both i_{C2} and $i_{C\mathrm{in}}$ remain zero once the total PT output capacitance is fully charged to V_{dc}. In Fig. 3.7, i_{d} is contributed by i_{C2} and $i_{C\mathrm{in}}$ during M_1 and, for the component values in Fig. 3.6, it is 1.1 times larger than resonant current i_{L1} as given in equation (3.27) (since C_2 is set to be 10 times smaller than C_{in}). During M_2 and M_3, i_{d} is dominated by i_{L1} since C_2 and C_{in} are fully charged. As shown in Fig. 3.7, i_{d} and i_{L1} share the same zero-crossing points under all modes. Since the effective

signs of i_d can be indicated by anti-parallel diode voltage v_d, v_d represents the sign (i_{L1}) and so can be used by the controller. A comparator U_1 is used to modify v_d and provide the resonant current zero-crossing feedback signal v_{zc} for the ZVS PLL controller.

3.4 Output side resonant current estimation

3.4.1 Current estimator 3: Voltage differentiator (CE3)

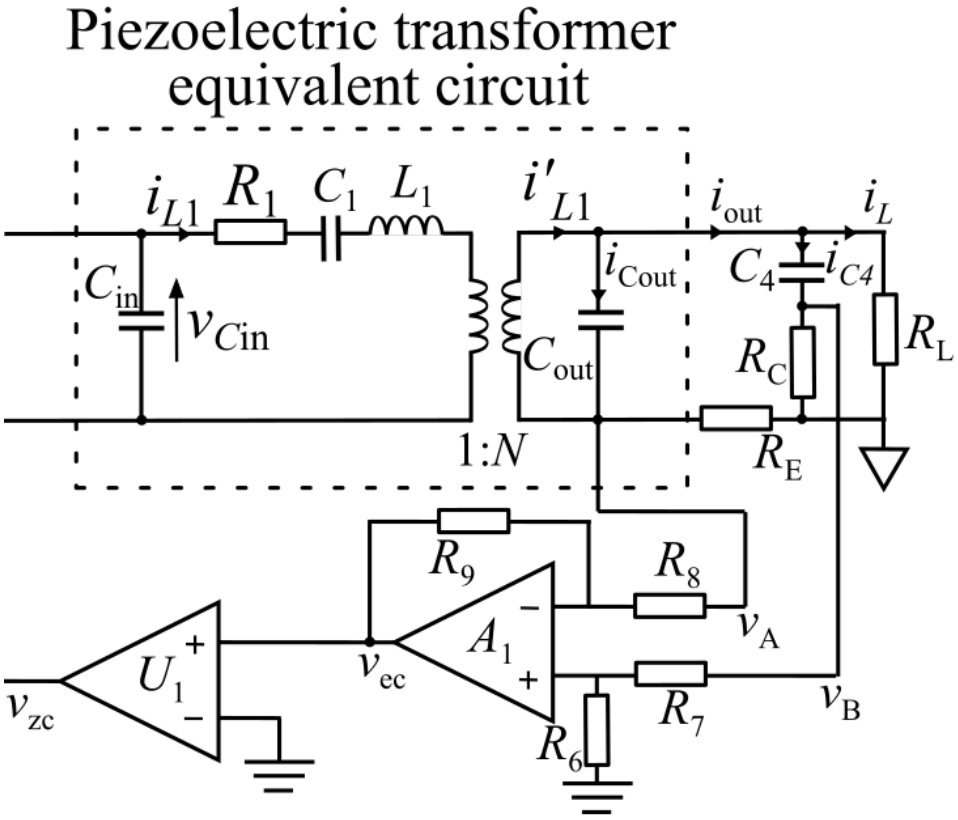


Fig. 3.8: Current estimator 3.

The current estimator 3 is developed at the secondary side to reconstruct resonant current, using a similar approach from current estimator 2, as shown in Fig. 3.8. Since i'_{L1} is a scaled version of the resonant current i_{L1}, they exhibit the same polarity and, therefore, i'_{L1} can be estimated by combining measurements of v_A and v_B. The two reference signals are combined using a differential amplifier A_1, to provide the current estimate signal v_{ec}. Comparator U_1 detects the zero-crossing of current estimate which is then provided to the control circuit as voltage v_{zc} for

simultaneous phase and frequency locking. As can be seen from Fig. 3.8, R_C senses the PT output capacitor current while R_E senses the PT output current. Therefore, a scaled version of $i_{C\text{out}}$ and i_{out} can be generated (if $R_C C_4 << T$ and $R_E C_{\text{out}} << T$, where T is the switching period) to reconstruct the resonant current i_{L1}.

$$i_{C\text{out}} = i'_{L1} - i_{C4} - i_L \tag{3.28}$$

$$\frac{\mathrm{d}v_{C\text{out}}}{\mathrm{d}t} = \frac{i_{C\text{out}}}{C_{\text{out}}} = \frac{i_{C4}}{C_4} \tag{3.29}$$

Rearranging equation (3.29) results in

$$i_{C4} = \frac{C_4}{C_{\text{out}}} i_{C\text{out}} \tag{3.30}$$

$$i_{C\text{out}} = \frac{C_{\text{out}}}{C_4} i_{C4} \tag{3.31}$$

Substituting equation (3.31) into equation (3.28) and solving for i_{C4}

$$i_{C4} = \frac{(i'_{L1} - i_L)C_4}{C_{\text{out}} + C_4} \tag{3.32}$$

The voltage across R_E and R_C can be found by

$$v_{R_E} = (i_{C4} + i_L)R_E \tag{3.33}$$

$$v_{R_C} = i_{C4} R_C \tag{3.34}$$

Substituting equation (3.32) into equation(3.30) and (3.31)

$$v_{R_E} = \frac{(C_4 i'_{L1} + i_L C_{\text{out}})R_E}{C_{\text{out}} + C_4} \tag{3.35}$$

$$v_{R_{\mathrm{C}}} = \frac{(i'_{L1} - i_L)C_4 R_C}{C_{\mathrm{out}} + C_4} \tag{3.36}$$

Adding voltage $v_{R_{\mathrm{E}}}$ and $v_{R_{\mathrm{C}}}$ together from equation (3.33) and (3.34)

$$v_{\mathrm{add}} = v_{R_{\mathrm{C}}} + v_{R_{\mathrm{E}}} = (R_{\mathrm{C}} + R_{\mathrm{E}})i_{C4} + R_{\mathrm{E}} i_L \tag{3.37}$$

If R_C/R_E is made the same as C_{out}/C_4, then equation (3.37) is rearranged as

$$v_{\mathrm{add}} = \frac{[(i_{C4} + i_L)C_4 + i_{C4}C_{\mathrm{out}}]R_{\mathrm{E}}}{C_4} \tag{3.38}$$

Substituting equation (3.28) and (3.30) into (3.38) and rearranging for v_{add}

$$\begin{aligned} v_{\mathrm{add}} &= R_{\mathrm{E}}(i_{C\mathrm{out}} + i_{C4} + i_L) \\ &= R_{\mathrm{E}} i'_{L1} \end{aligned} \tag{3.39}$$

From equation (3.39), it is indicated that $v_{\mathrm{add}} \propto i'_{L1}$ .Therefore, the resonant current can be estimated using a differential amplifier and $v_{\mathrm{ec}} \propto i_{L1}$.

Fig. 3.9 shows the SPICE simulation waveforms of current estimator under ZVS. v_A and v_B are combined to reconstruct the estimated current v_{ec}, and are used to generate the feedback signal v_{ZC} for the control circuit. As can be seen, v_{ec} is proportional to i_{L1}, and they share the same zero-crossings.

Although the finding presented in this chapter have only been validated by simulation results, Chapter IV will present a phase-locked loop controller using the current estimators presented in this chapter which will be validated by the experimental results. These results will also validate the operation of these current estimators.

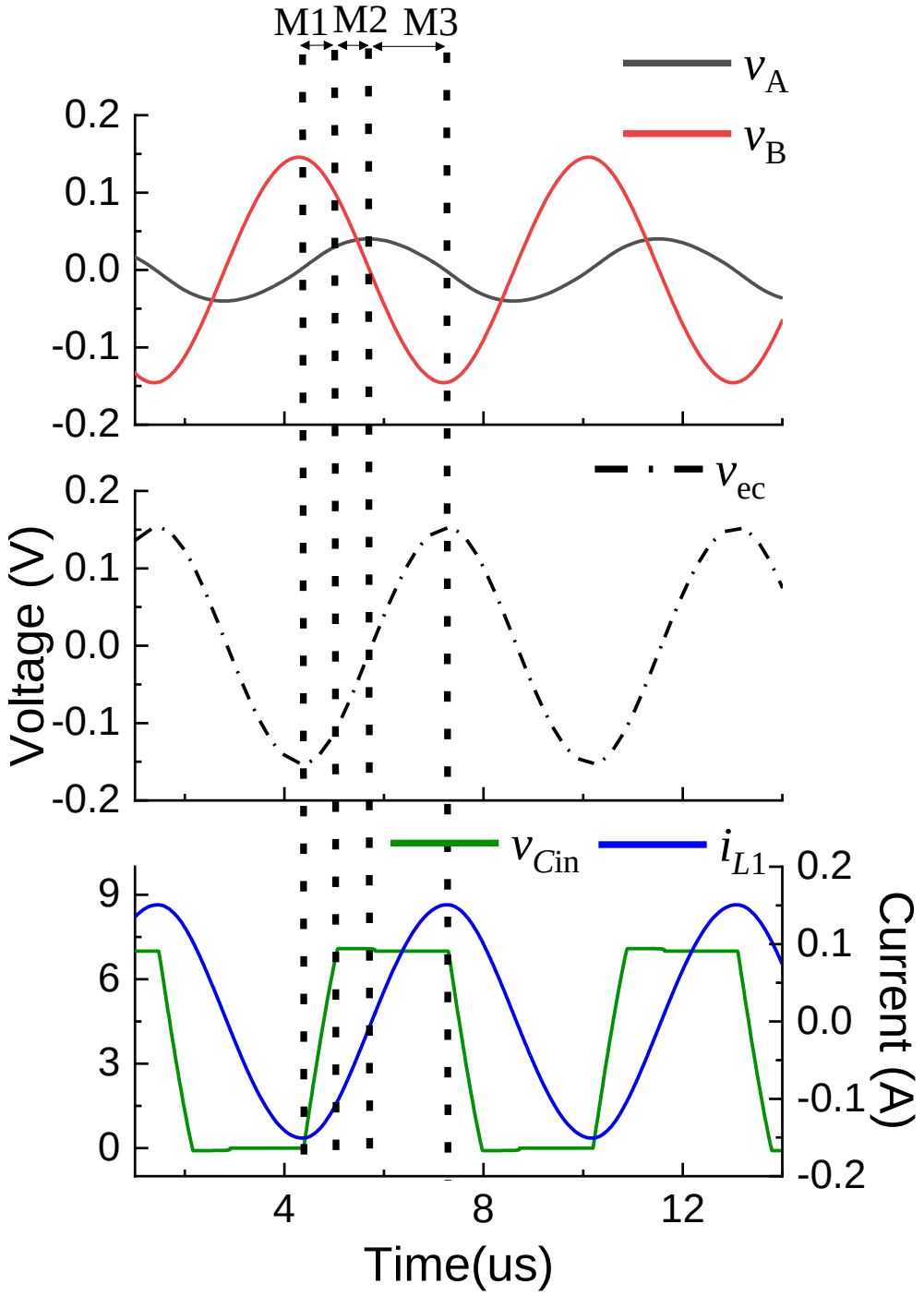


Fig. 3.9: Switching waveforms of current estimator 3.

3.5 Chapter conclusions

In this chapter, techniques used to estimate resonant current and indicate zero-crossings for ZVS has been presented. Initially, the operating principle of PT-based inductorless half-bridge resonant converter is described with ZVS and non-

ZVS condition. Subsequently, primary side current estimation is demonstrated. By regenerating PT input current and PT input capacitor current, the resonant current is reconstructed through a voltage differentiator. Additionally, an anti-parallel diode current estimator with zero crossings detection is described. The resulting estimations are modified before applied to the control circuit. To improve system noise performance and avoid interference from MOSFET switching events, the voltage differentiator approach is further developed at the secondary side to rebuild resonant current, by reproducing PT output capacitor current and PT output current. All these estimation techniques, which shows good correlations that indicate zero crossings compared to the actual resonant current, can be used for the control circuit to lock-on to the resonant current and provide in-phase gate signals with adequate deadtime.

3.6 References

[3.1] Z. Yang, J. Forrester, J. N. Davidson, M. P. Foster and D. A. Stone, "Resonant current estimation and phase-locked loop feedback design for piezoelectric transformer-based power supplies", *IEEE Transactions on Power Electronics*, vol. 35, pp. 10 466-10 476, 2020.

[3.2] E. Minazara, D. Vasic and F. Costa, "Comparing piezoelectric transformer working with PLL and with nonlinear load approaches in DC-DC converter," *2007 European Conference on Power Electronics and Applications*, 2007.

[3.3] M. Ekhtiari, T. Zsurzsan, M. A. E. Andersen and Z. Zhang, "Optimum Phase Shift in the Self-Oscillating Loop for Piezoelectric-Transformer-Based Power Converters," *IEEE Transactions on Power Electronics*, vol. 33, pp. 8101-8109, 2018.

[3.4] M. P. Foster, J. N. Davidson, E. L. Horsley and D. A. Stone, "Critical Design Criterion for Achieving Zero Voltage Switching in Inductorless Half-Bridge-Driven Piezoelectric-Transformer-Based Power Supplies," *IEEE Transactions on Power Electronics*, vol. 31, pp. 5057-5066, 2016.

[3.5] V. C. Alfredo, “50 years of piezoelectric transformers. Trends in the technology,” *Materials research society symposium proceedings*, vol. 785, 2003, pp.33-44

[3.6] M. Ekhtiari, T. Andersen, Z. Zhang and M. A. E. Andersen, "Digitized self-oscillating loop for piezoelectric transformer-based power converters," *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 1430-1436.

[3.7] M. S. Rødgaard, "Piezoelectric transformer based power converters design and control," Ph.D dissertation, Department of Electronic Engineering, Technical university of Denmark, Kongens Lyngby, Denmark, 2012.

Chapter IV

Phase-locked loop control design

In this Chapter, a new technique, which locks onto the switching waveforms using an analogue phase-locked loop (PLL) to ensure ZVS operation, is described in detail and compared with prior art. The proposed PLL control technique enables fast tracking of resonant frequency, compensation of resonant frequency drift, improved robustness to noise and ZVS for inductorless configuration at the matched load condition. By taking the reference signals generated from current estimators presented in Chapter III, the PLL synchronises both phase and frequency of the resonant current, and generate the in-phase gate drive signals with adequate deadtime. Three PLL controllers are developed– a phase locked PWM which employs the timing capacitor of PLL, a time delay circuit which shapes the PLL output through a RC network, and a frequency divider which halves the PLL output frequency. To validate the proposed ZVS PLL controller, a prototype converter is implemented with a ring-dot radial mode PT. Experimental validation show successful ZVS operation of all PLL controllers together with the current estimators presented in Chapter III. The comparison of lock-on time and start-up period are also reported, and nine permutations of current estimation and feedback are concluded for application-specific usage.

4.1 Introduction

Following the development of resonant current estimation techniques in Chapter III, Chapter IV presents a PLL control system which employs the current estimator for achieving ZVS of a PT-based converter.

Several circuit topologies have been investigated to drive PTs, as described in Chapter II, including push-pull [4.1], class-E [4.2] and half-bridge [4.3]. For step-down applications, although the inductorless half-bridge configuration shows the best performance in terms of size and cost, as it eliminates the need for any magnetic components at the expense of increased deadtime and difficulty of control [4.4][4.5], the operating frequency is reduced to a narrow band slightly above resonance, where the PT exhibits inductive behaviour. Therefore, a control circuit which enables precise tracking of resonant frequency is required.

The control strategies for PT-based converters reported in the literature include pulse-width modulation (PWM) [4.6], pulse-frequency modulation (PFM) [4.7], pulse-density modulation [4.8] and phase-locked loop (PLL) [4.9]. In [4.10], a combination of PWM and PFM is used for line and load regulation of an AC/DC converter. The circuit in [4.10] employed PWM at a fixed switching frequency for low output voltages and employed PFM at a fixed duty ratio for high output voltage. For PT-based inductorless configurations, an input matching network has been introduced in [4.8][4.11] while a self-oscillating control system is implemented in [4.12] to achieve ZVS. In [4.8], pulse-density modulation is employed to regulate the output voltage, with an input matching network implemented to reduce switching harmonics. A multi-loop control strategy is used to modify the number of on/off cycles, switching frequency, burst-mode period and deadtime which can be dynamically adjusted. However, each of these control methods reported in the literature experiences one or more of the following drawbacks:-

1) Resonant frequency drift of the PT is uncompensated. The resonant frequency varies with load and temperature [4.13][4.14]. As the efficiency of a PT is maximised when it is operated close to its resonant frequency, any uncompensated change in resonant frequency can decrease efficiency.

Therefore, a highly sensitive adjustable control strategy is required to maintain high-efficiency operation, such as phase-locked loop control [4.15], adaptive phase control [4.9] or self-oscillating control [4.16].

2) High efficiency of both PT and resonant converter is hard to achieve for the inductorless topology. This is because reduced resonant current flows during the deadtime [4.17]. In [4.8] and [4.11], an input matching network is introduced for ZVS optimization. However, total efficiency is decreased since part of the energy is consumed by the matching network. Moreover, the PT's driving waveform generated by the matching network is not ideal and hence other higher-order harmonics are introduced and cannot be ignored in practice.

To address these problems, a self-oscillating phase-shift compensation approach was introduced in [4.16][4.18]. Current peaks [4.18] and zero-crossing points [4.16] of the resonant current are sensed and used for switch timing. The principle of phase compensation is to track the resonant frequency change in a PT with cycle-by-cycle adjustments where the phase around the loop is adjusted to be an integer multiple of 2π to meet the Barkhausen criterion [4.19] for sustained oscillation. A self-induced oscillation is used to excite the PT vibration near the resonant frequency during system start-up. However, this approach suffers from two problems:-

1) Since the controller must operate as an oscillator and, during start-up, operates with a frequency lower than the PT's resonant frequency, the efficiency of the PT is reduced due to below resonance operation.

2) When the resonant frequency changes, multi-period lock-in delays can be introduced, which is not desirable for fast tracking. Additionally, soft

switching is not preserved during lock-in delay as the driver has not reached steady state.

In this Chapter, a comparative analysis of nine variants of a phase-locked loop (PLL) controller is presented which overcomes these problems. Together with the current estimators presented in Chapter III, three gate-signal generators are proposed and evaluated to mitigate issues of resonant frequency drift, ZVS for the inductorless half-bridge configuration, extra circuity and time required for self-excitation of the resonant current, and to expedite circuit start-up. The designs lock on to the resonant frequency, ensuring $\pi/2$ radians deadtime necessary for meeting the critical criterion in [4.17] and therefore achieving ZVS for all resistive loads. The controller's ability to lock on to phase and frequency, irrespective of operating conditions and temperature, makes PLL control highly desirable in this application.

4.2 Operation of the ZVS PLL control system

The proposed ZVS control system consists of a resonant current estimation circuit (described in Chapter III) and PLL controller, as shown in Fig. 4.1. A resonant current estimator is employed to reconstruct the Mason-equivalent circuit resonant current by its zero crossings using signal v_{zc} which is applied as an input signal to the PLL controller. Although two signals are shown for v_{zc}, only one of those signals will be used depending on whether primary-side or secondary-side resonant current estimation is being used. The PLL controller is implemented by a CMOS CD4046 (using the type II phase detector) to lock on to the phase and frequency of the resonant current and provide correctly synchronised gate signals via steering logic to achieve ZVS.

The CD4046 consists of the phase comparator and a voltage-controlled oscillator (VCO) which are connected to each other by an external low-pass filter (LPF).

The phase comparator output of the CD4046 (the phase error) is integrated by the low-pass filter and therefore ensures, once the PLL has locked on, that the phase error is zero. The LPF operating within a feedback loop performs this integration and also reduces phase noise to produce a stable voltage for the VCO. The PLL's output frequency is therefore adjusted until the output is locked in phase and frequency to the resonant current, and ZVS will therefore be achieved if the critical design criterion is met [4.17]. Signal v_{lock} is the VCO output and v_{lock}' corresponds to the phase comparator II input, v_{lock} equals to v_{lock}' if no frequency division is employed in the feedback loop (as will be discussed later). v_{pc} and v_{vco} are type II phase comparator output and VCO input, respectively. The circuit operating waveforms have been described in Fig. 3.2 in Chapter III.

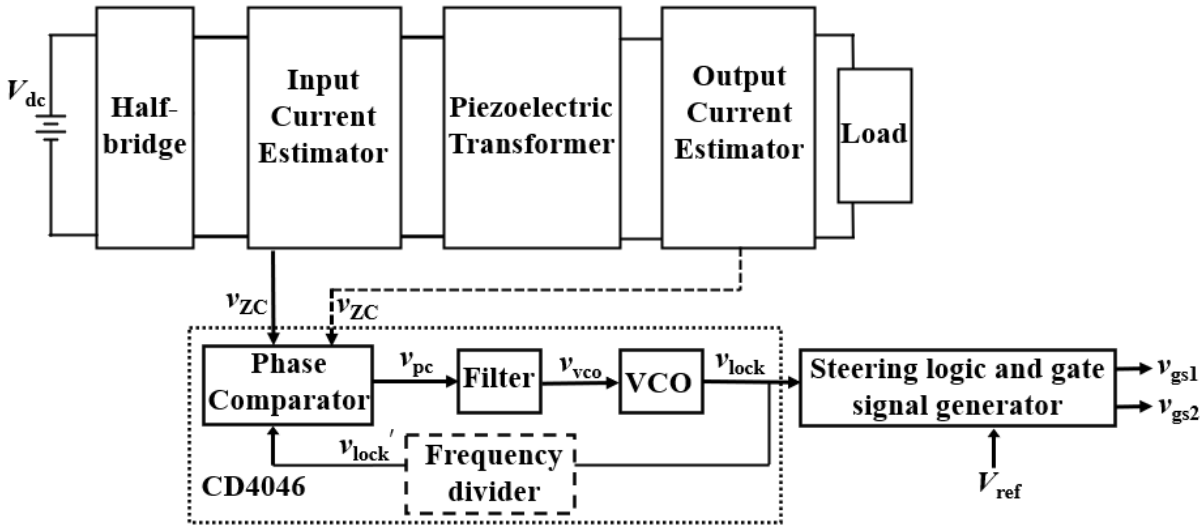


Fig. 4.1: Block diagram of the ZVS PLL control system.

4.3 Operation of CD4046 PLL

4.3.1 General description

The ZVS PLL controller is based on the CMOS CD4046 IC and utilises phase comparator II as a phase frequency detector (PFD) to achieve a signal v_{lock} which is locked in both frequency and phase to the input signal v_{zc}. A circuit block diagram adapted from the datasheet [4.19] is shown in Fig. 4.2 with annotations

shown in blue to allow them to be easily identified. As mentioned, this work will focus on the zero-phase-difference phase comparator (phase comparator II) and the Zener diode presented on pin 15 for supply voltage regulation. External resistor R_{t1} and capacitor C_t determine the frequency range of VCO while R_{t2} enables the frequency offset of VCO. Voltages v_{ct1} and v_{ct2} correspond to the voltage on each side of C_t.

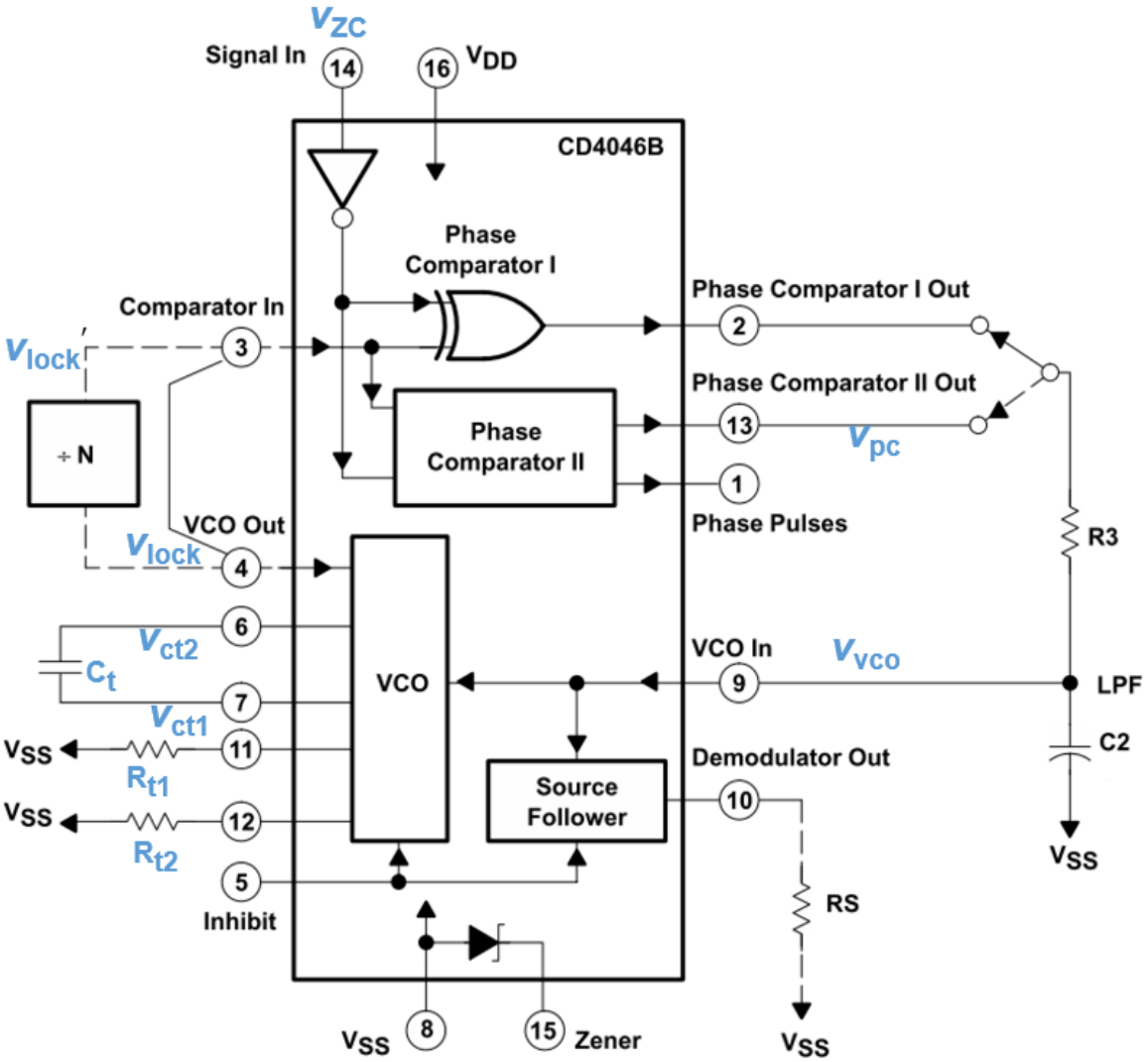


Fig. 4.2: The circuit block diagram of CD4046 [4.20].

The phase comparator II synchronises the frequency and phase of the input signal presented at pin 14, v_{zc}, by generating a phase error at pin 13, v_{pc}. When the phase error is zero when PLL is locked on. The external LPF reduces phase noise,

integrates the phase error, attenuates the high-frequency AC components and generates a stable voltage for VCO [4.20], v_{VCO}.

Previous literature on PT-based controller design introduces self-induced oscillation to initialise the PT-based converter, which results in additional circuity and time required for self-excitation of the resonant current [4.16][4.21]. This can be eliminated if the VCO range covers only the possible operating frequencies. At the system start-up, when no input signal has been applied to the PLL, the error voltage at the output of the phase comparator is zero. The VCO therefore initially operates at its minimum frequency, which is set close to expected resonant frequency thereby reducing the time required for self-excitation of the resonant current [4.16][4.21] and ensure a fast system start-up.

4.3.2 Phase synchronisation

The phase comparator II of CD4046 used in this work is a positive edge-controlled phase frequency detector. The PFD is triggered only by the positive signal transitions and therefore the duty cycles of signal input, v_{zc}, (pin 14) and the VCO input, v_{lock}, (pin 3) are not important. As shown in Fig. 4.3(a), the phase comparator II comprises a phase detector which consists of flip-flops, gates and a low-pass filter charge-pump which behaves like an up-down counter. The phase detector generates gating signals to trigger charge-pump switches. The charge-pump is implemented using a p-MOS and a n-MOS, and they are controlled such that the current flow into and out of LPF is dynamically adjusted according to the phase and frequency difference.

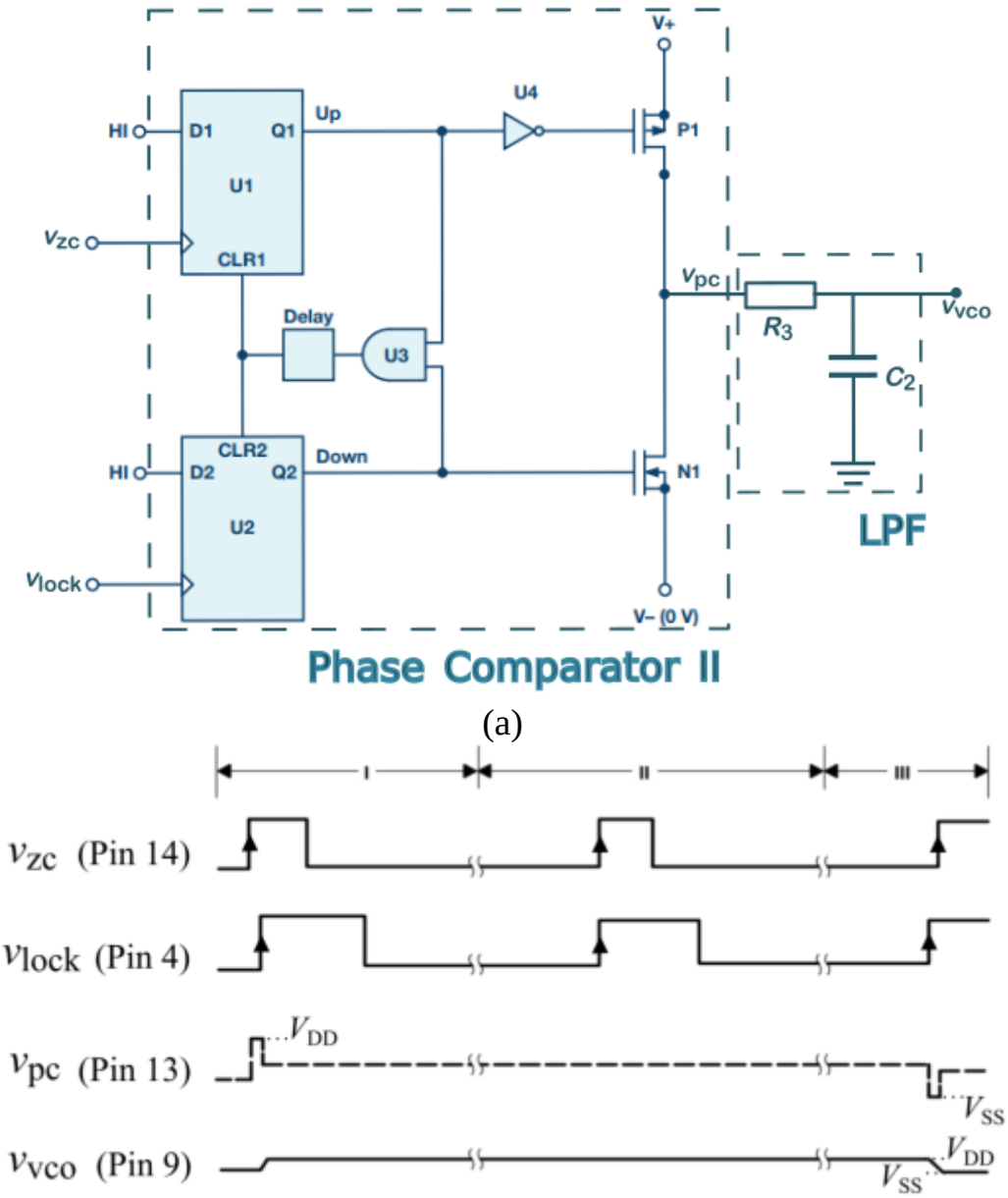


Fig. 4.3: (a) Block diagram and (b) switching waveforms of the PLL using phase comparator II [4.20].

The typical switching waveforms of the phase comparator II is shown in Fig. 4.3(b). It is classified into three sections (I, II and III), which corresponds to when VCO input lags the signal input, high-impedance state and signal input lags the VCO. Phase comparator II typically exhibit one or more of following operations:

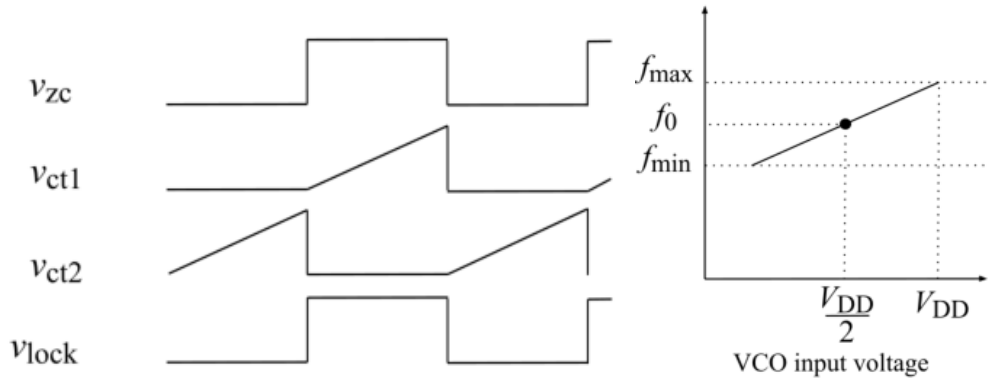
1) The signal input v_{zc} and comparator input v_{lock} are not frequency matched: if the frequency of v_{zc} is higher than the VCO, the n-MOS is off and p-MOS is on and this charges the capacitor of the LPF such that the VCO input v_{vco} increases thereby increasing the VCO operating frequency. Conversely, if the frequency of v_{zc} is lower than the VCO, the p-MOS is off and n-MOS is on so as to discharge the capacitor of the LPF and reducing the VCO input voltage, thereby decreasing the VCO operating frequency.

2) The signal input and VCO are frequency-matched but not phase-matched: if the VCO lags v_{zc} in phase then the n-MOS is off and p-MOS is pulsed on. A positive pulse is generated which width is proportional to the phase difference and the phase error is reduced. Conversely, if the VCO output exhibits a phase lead, then the p-MOS is off and n-MOS is pulsed on for the time corresponding to the phase difference.

3) Both signals are phase and frequency matched: the output of the phase comparator is in a high-impedance state since both n-MOS and p-MOS devices are off and so the LPF maintains a constant voltage.

4.3.3 Voltage-controlled oscillator (VCO)

Within the operating frequency range, the VCO is a linear, time-invariant system. The control voltage v_{vco} (VCO input) at pin 9 determines the charge/discharge currents that flow through the external timing capacitor C_t shown in Fig. 4.2, thereby control the time required to charge/discharge the capacitor to a pre-determined threshold value internal to the IC. Therefore, VCO output frequency is determined by the control voltage v_{vco} and exhibits 50% duty ratio.



(a) (b)

Fig. 4.4: VCO characteristics: (a) timing capacitor voltage in locked condition and (b) relationship between VCO input voltage and operating frequency range.

The switching waveforms of VCO correspond to timing capacitor in the locked condition and VCO operating range with respect to VCO input voltage are shown in Fig. 4.4(a) and Fig. 4.4(b), respectively. The voltage on each side of C_t is shown as v_{ct1} and v_{ct2} while f_{max}, f_{min}, and f_0, correspond to maximum, minimum and centre operating frequency of VCO. The VCO input voltage controls a current mirror that supplies C_t and this in turn controls the time for $v_{ct1/2}$ to charge from 0V to the threshold voltage thus producing the sawtooth type waveforms for $v_{ct1/2}$ that are phase and frequency locked to v_{zc}. The VCO characteristics are user-adjustable by external components R_{t1}, R_{t2} and C_1. The component selection for a typical operating condition can be found in the datasheet [4.20]. To ensure a proper VCO operation, the component values may still need to be tuned by experiment [4.22].

4.4 Gate signal generator

4.4.1 Phase locked PWM

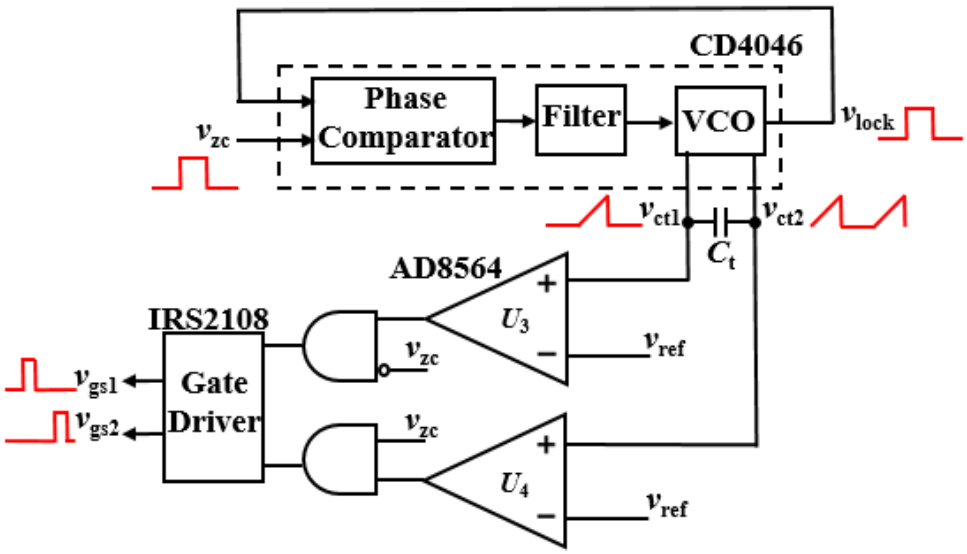


Fig. 4.5: Block diagram of PLL controller with phase-locked PWM

The PLL controller with phase-locked PWM (shown in Fig. 4.5) is implemented by employing the CD4046's timing capacitor voltage (seen as two sawtooth waveforms with 180° phase shift) as a reference signal to produce gate drive signals. The VCO has a 50% duty cycle and operates by charging the external timing capacitor, C_t, via a current source controlled by the VCO input signal. One side of C_t is held at ground while the other side is charged by the current source, producing a ramp (sawtooth) waveform phase locked to the PLL input signal v_{zc}. Once C_t charges to half of the internal logic voltage, the charged side is pulled to ground, and the other side is discharged through an internal resistor. A new half cycle begins. v_{ct1} and v_{ct2} act as the carrier signals for the phase offset comparator U_3 and U_4 [4.15], which compare the capacitor voltages to reference voltage, v_{ref}. v_{ref} is carefully specified to ensure the correct dead-time is achieved. Subsequently, through the combinational logic, the phase and frequency-locked MOSFET gate drive signals synchronised to i_{L1} are generated, featuring the requisite $\pi/2$ deadtime interval.

4.4.2 RC time delay

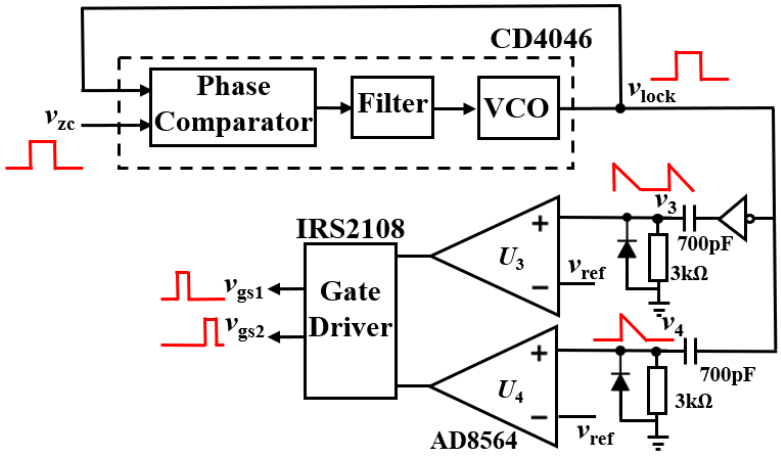


Fig. 4.6: Block diagram of PLL controller with RC time delay.

Fig. 4.6 shows an alternative implementation where the controller essentially forms an RC delay circuit by taking the VCO output v_{lock} as a reference. Once the PLL locks onto the resonant current i_{L1}, the VCO output v_{lock} follows the phase and frequency of i_{L1}. In Fig. 4.6, v_{lock} and its inverted version are shaped through identical RC delay circuits to trigger the gates following the correct delay. The circuit and reference voltage, v_{ref}, are arranged to provide $\pi/2$ deadtime, ensuring the high-side switch turns on at zero phase and maintains π radians delay between the two switches.

4.4.3 Frequency divider

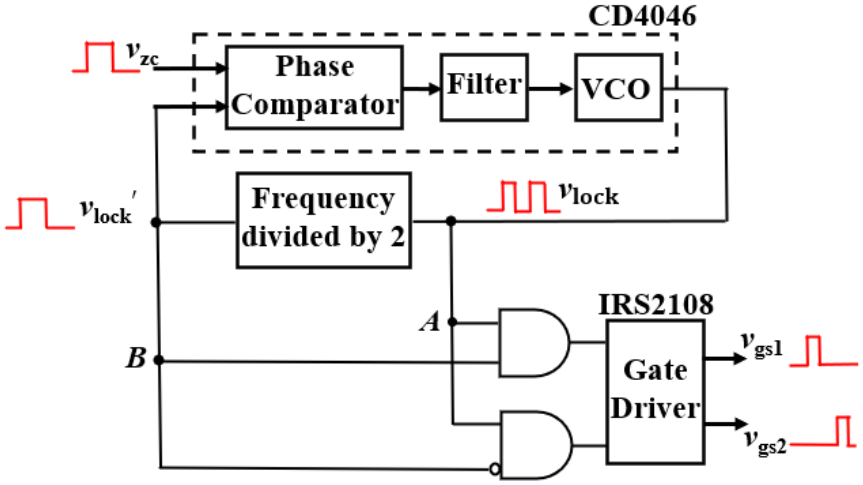


Fig. 4.7: Block diagram of PLL controller with frequency divider.

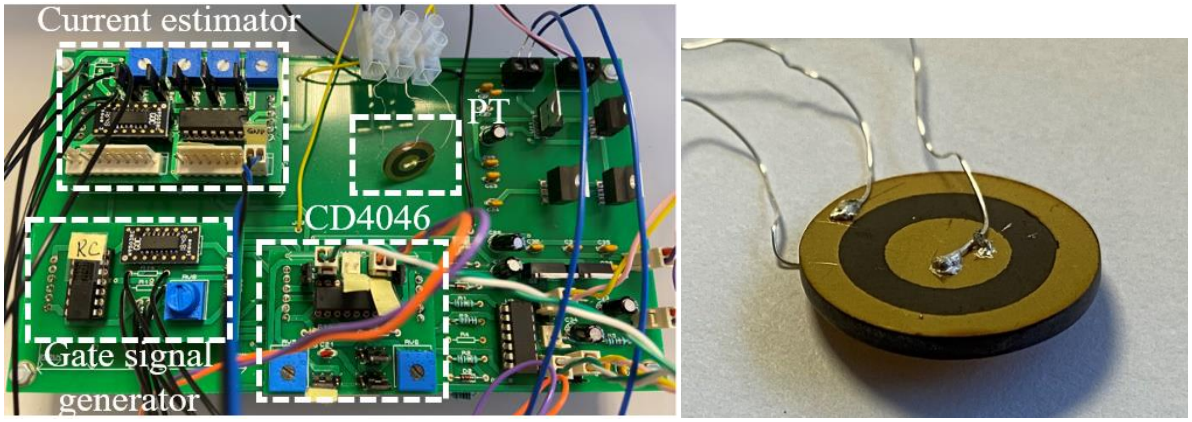
Fig. 4.7 shows an alternative approach where the PLL controller is implemented by employing a frequency divider to the feedback path between the VCO output and the phase comparator input v_{zc}. A D-type flip flop is used for the frequency divider. The incoming signal (v_{lock}) acts as a clock for the D-type flip flop and the D input is then clocked through the output. The VCO operates at twice the switching frequency, and its output frequency is halved and used to drive the half-bridge. With frequency divider input v_{lock} (or A) and its output v_{lock}' (or B), the corresponding in-phase gate drive signals with $\pi/2$ phase shift are generated through combinational logic, according to these Boolean equations:-

$$v_{gs1} = A \cdot B \tag{4.1}$$

$$v_{gs2} = A \cdot \bar{B} \tag{4.2}$$

4.5 Experimental validation

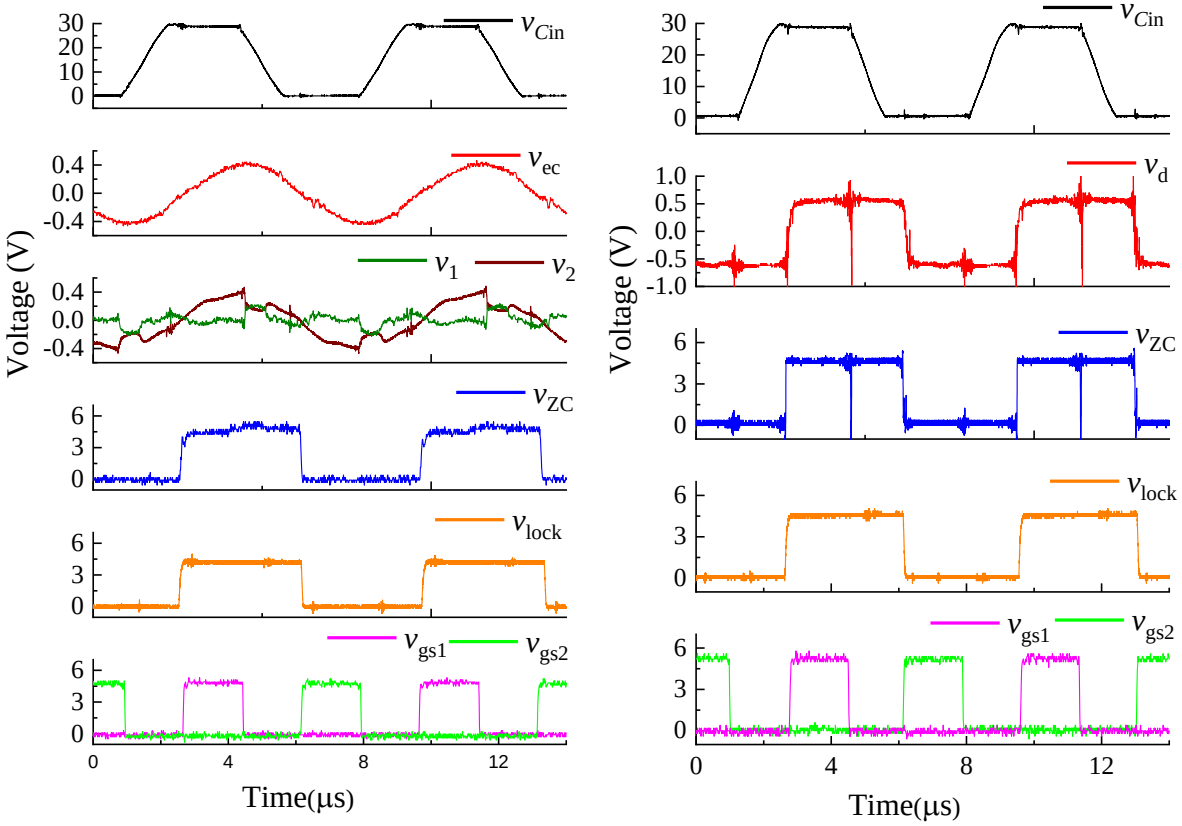
To provide validation of the proposed control methods and the current estimators presented in Chapter III, a prototype converter is implemented, as shown in Fig. 4.8(a). A radial mode PT presented in [4.23][4.24], as shown in Fig. 4.8(b), with the following extracted equivalent circuit component values at the matched load condition is used: C_{in}=0.43nF, C_{out}=1.14nF, L_1=17.2mH, C_1=77.8pF, R_1=12.4Ω, N=0.94, Q=1190.



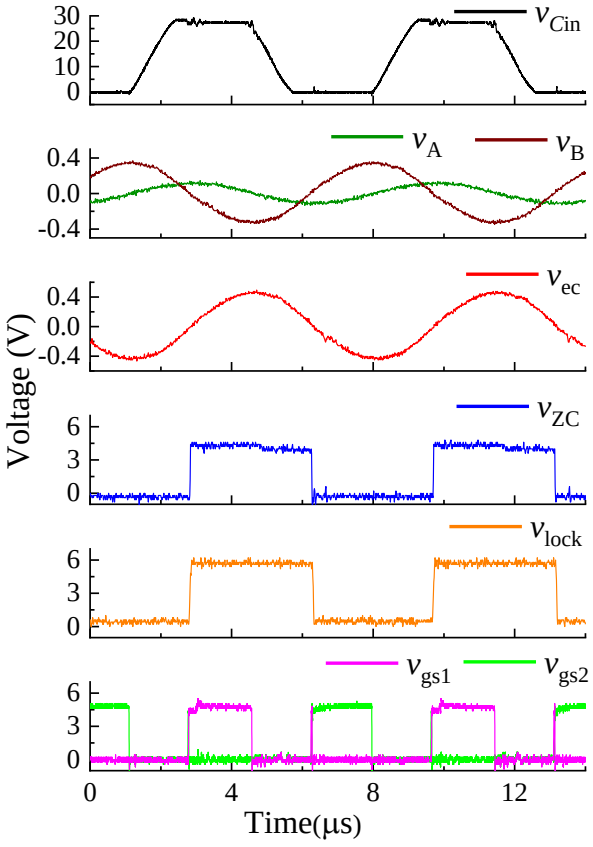
(a) (b)

Fig. 4.8: (a) Prototype half-bridge inductorless PT-based converter and (b) the ring-dot radial mode piezoelectric transformer under test.

A DC supply voltage of 30V is used for the power stage. Since the ideal operating frequency of the PT is temperature- and load-dependent, as well as being subject to manufacturing tolerances, suitable limits to the operating frequency range (typically ±5% of PT's resonant frequency) must be applied using the PLL [4.16]. The experimental measurements are shown in Fig. 4.9, with all combination of gate signal generators associated with current estimators (CE1-CE3) presented in Chapter III. The experimental waveforms are shown in Fig. 4.9 split across three pages with the phase locked PWM on the first page [parts (a)-(c)], The RC time delay approach shown on the second page [parts (d)-(f)] and the frequency divider approach on the third page [parts (g)-(i)]. Each page contains three plots – working left to right and top to bottom each plot is current estimator 1 (CE1), CE2 and CE3. Each plot shows v_{Cin}, the estimated current v_{ec} and v_d, and associated waveforms (i.e. v_1, $v_{2,}$ v_A, $v_{B,}$), current zero crossing signal v_{zc}, VCO output v_{lock} and the gate signals $v_{gs1,2}$. v_{ec} and v_d are the reconstructed current using voltage differentiator approach and voltage across the diode using anti-parallel diodes approach described in Chapter III, they are all considered as the zero-crossing references to the comparator and modified to v_{zc} before applied to PLL controller.


Voltage (V)
Time(μs)
v_{Cin}
v_{ec}
v_1
v_2
v_{ZC}
v_{lock}
v_{gs1}
v_{gs2}
v_d

(a) (b)


Voltage (V)
Time(μs)
v_{Cin}
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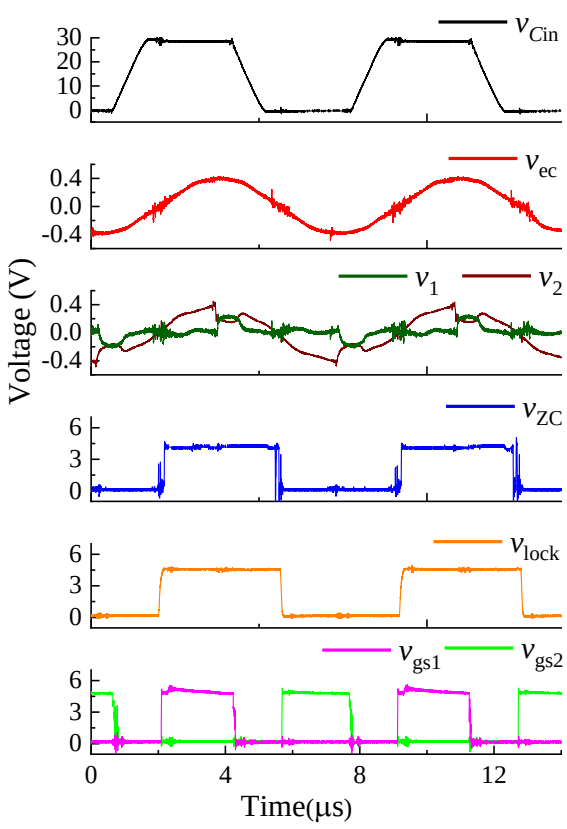
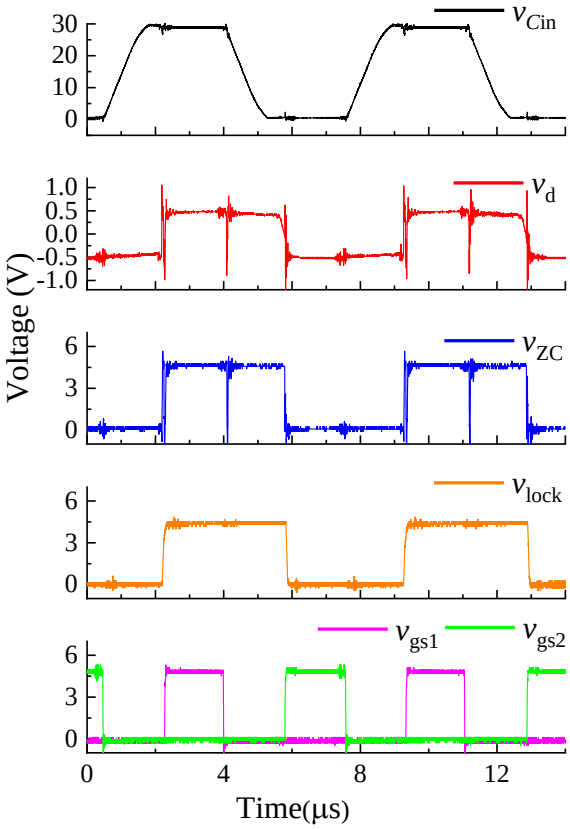
v_B
v_{ec}
v_{ZC}
v_{lock}
v_{gs1}
v_{gs2}

(c)


v_{Cin}
v_{ec}
v_1
v_2
v_{ZC}
v_{lock}
v_{gs1}
v_{gs2}
Voltage (V)
Time(μs)

(d)


v_{Cin}
v_d
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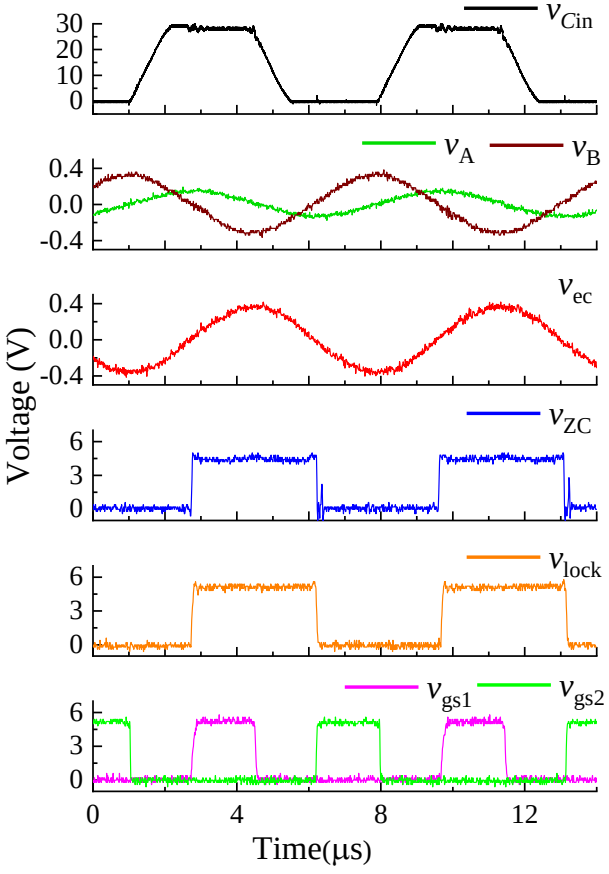
v_{lock}
v_{gs1}
v_{gs2}
Voltage (V)
Time(μs)

(e)


v_{Cin}
v_A
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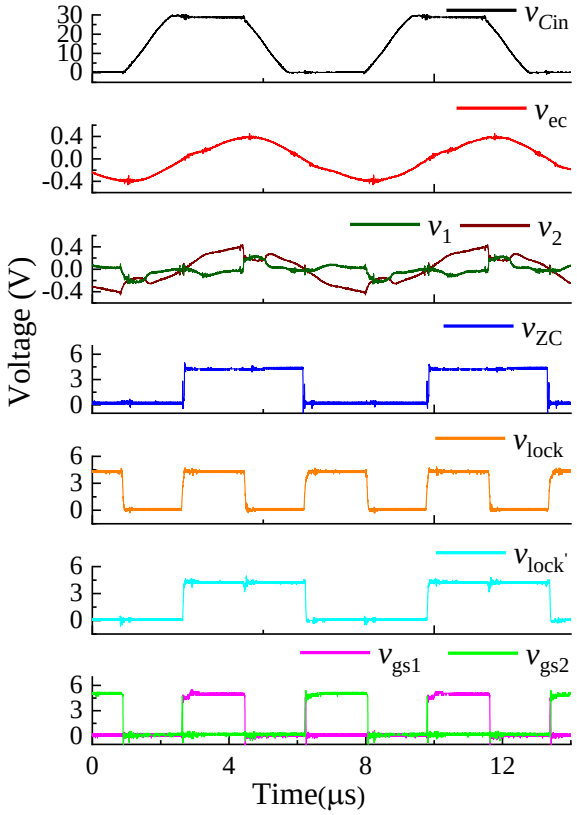
v_{lock}
v_{gs1}
v_{gs2}
Voltage (V)
Time(μs)

(f)


Voltage (V)
Time(μs)
v_{Cin}
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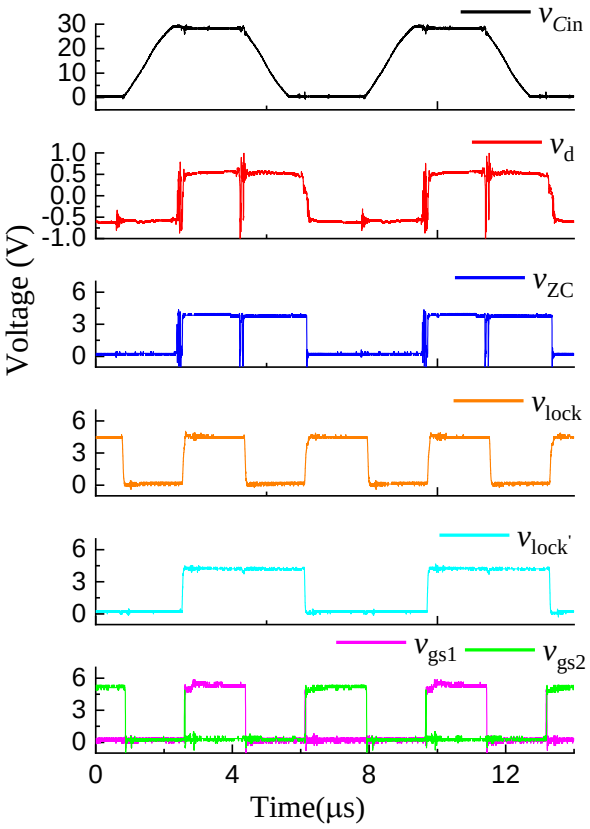
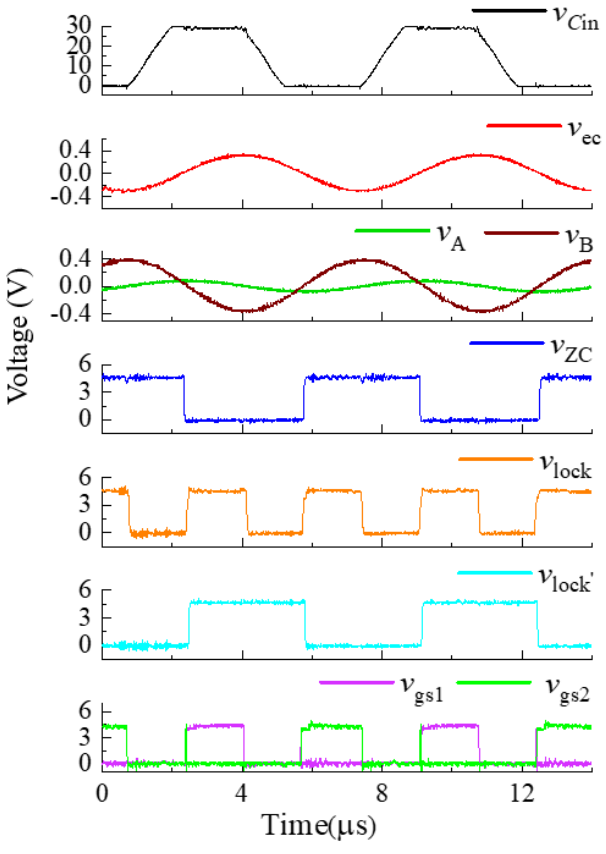
v_1
v_2
v_{ZC}
v_{lock}
v_{lock}'
v_{gs1}
v_{gs2}

(g)


Voltage (V)
Time(μs)
v_{Cin}
v_d
v_{ZC}
v_{lock}
v_{lock}'
v_{gs1}
v_{gs2}

(h)


Voltage (V)
Time(μs)
v_{Cin}
v_{ec}
v_A
v_B
v_{ZC}
v_{lock}
v_{lock}'
v_{gs1}
v_{gs2}

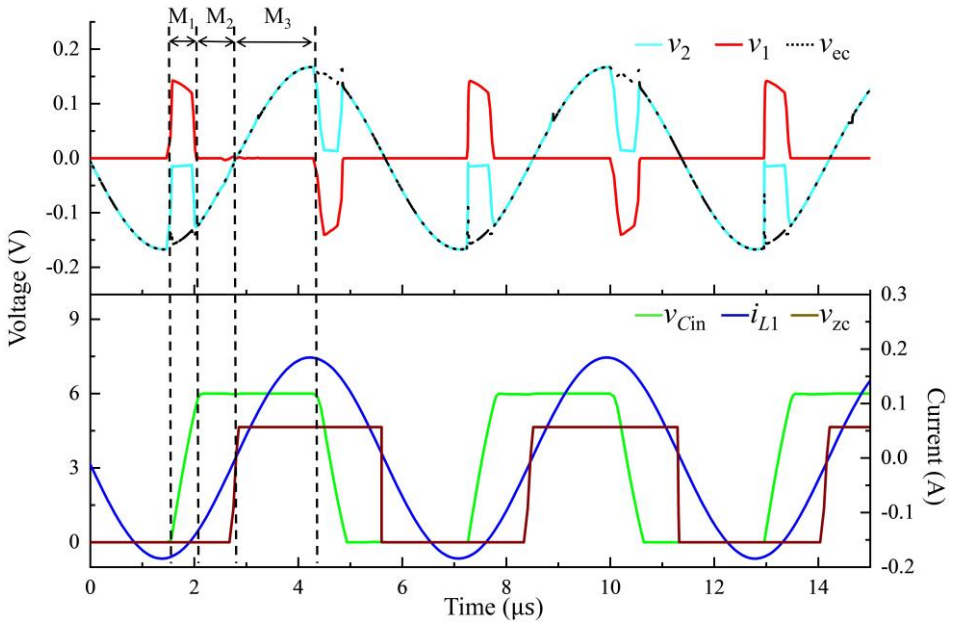
(i)

Fig. 4.9: Experimental results of the proposed control methods. Phase-locked PWM controller with (a) CE1, (b) CE2 and (c) CE3. RC time delay controller with (d) CE1, (e) CE2, and (f) CE3. Frequency divider controller with (g) CE1, (h) CE2 and (i) CE3.

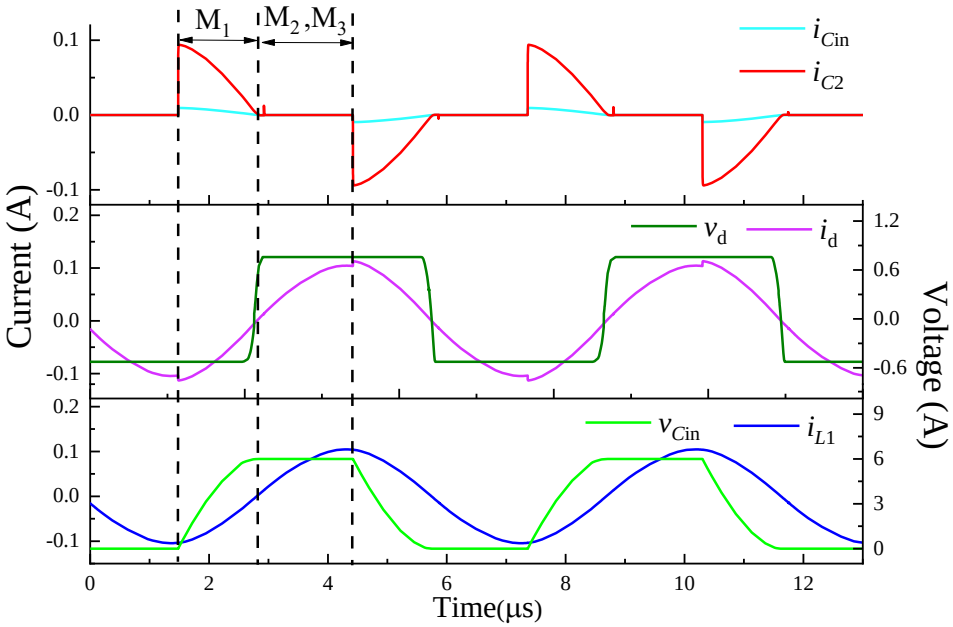
For all cases, the PLL's internal low-pass filter, which has a corner frequency of 400kHz, is used to compensate the loop and to minimise phase error. For the phase-locked PWM (Fig. 4.9(a)-(c)) and the RC time delay (Fig. 4.9(d)-(f)) steering logic implementations, the VCO is restricted to operate between 135kHz and 145kHz by a C_t=410pF timing capacitor, R_{t1}=50kΩ timing resistor and a R_{t2}=200kΩ frequency offset resistor. It thereby ensures adequate lock and capture range while still accommodating component tolerances. For the frequency divider implementation (Fig. 4.9 (g)-(i)), the VCO is set up to cover a lock and capture range of 270-290kHz (i.e. covering twice the resonant frequency) by a C_{t1}=220pF timing capacitor, R_{t1}=90kΩ timing resistor and R_{t2}=500kΩ frequency offset resistor. As shown in Fig. 4.9, for all cases, the two inputs of the phase comparator II, v_{zc} and v_{lock} (or v_{lock}'), have identical phase and frequency, indicating the PLL-locked condition. The zero-crossing points of the resonant current are clearly shown by the rising and falling edge of v_{zc}. Subsequently, gate signals v_{gs1} and v_{gs2} are generated through the appropriate steering logic and driver circuits.

All results show ZVS is achieved (indicated by the v_{Cin} rise completing during the deadtime). As these experiments were performed for the matched load, which is the worst-case condition, they demonstrate the ZVS-capability of the implementations for all loads. This is to be expected as the radial mode PT was designed to meet the critical criterion (see [4.30]). In each case, v_{zc}, the detected current phase, has clean edges which align to the detected current and the gate signals. Although the noise is not negligible, the results show good agreement with the simulation results (shown in Fig. 4.10), confirming the accuracy of the

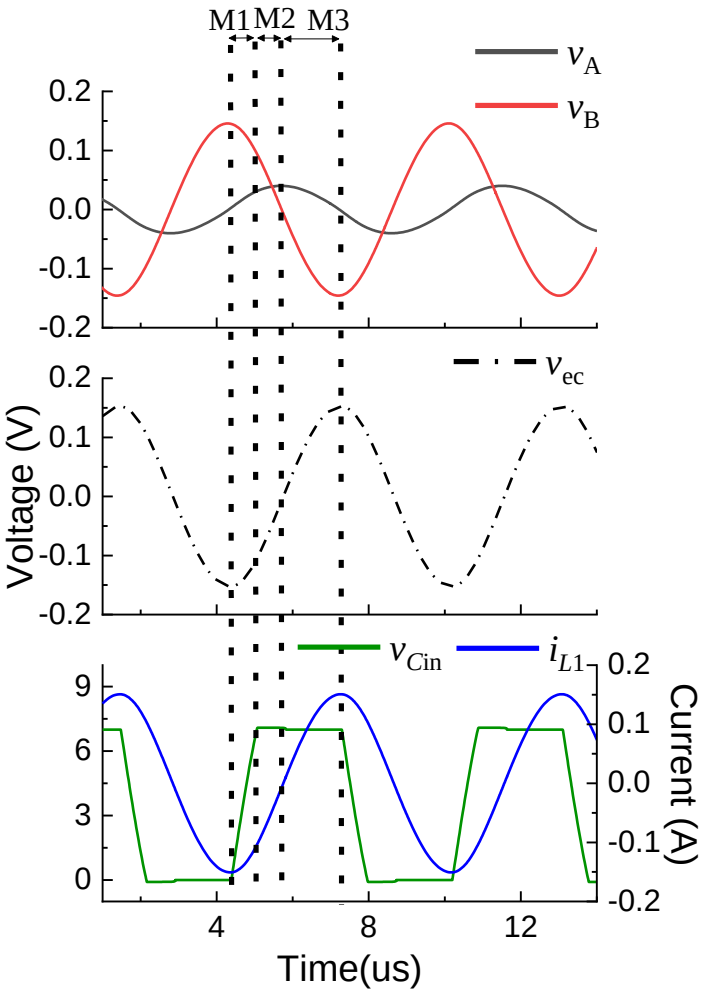
simulation and therefore provide experimental validation for the current estimators described previously.



(a)



(b)



(c)

Fig. 4.10: Switching waveforms from SPICE simulation. (a) Current estimator 1, (b) current estimator 2 and (c) current estimator 3.

4.6 Recommendations

The performance, complexity and versatility of the controller depends on the particular implementations of the steering logic (which produces the gate signals and phase feedback) and the resonant current estimator. In this section, a number of options are provided for nine implementations. Each is present and analysed individually, and the final complete implementations are compared. Both simulation and experimental results are provided to demonstrate the versatility of

the proposed control systems. A matched load is applied in this work since it indicates the most challenging operating condition for achieving ZVS [4.14]. If ZVS is achieved at the matched load, ZVS operation is possible at any load.

4.6.1 Noise immunity

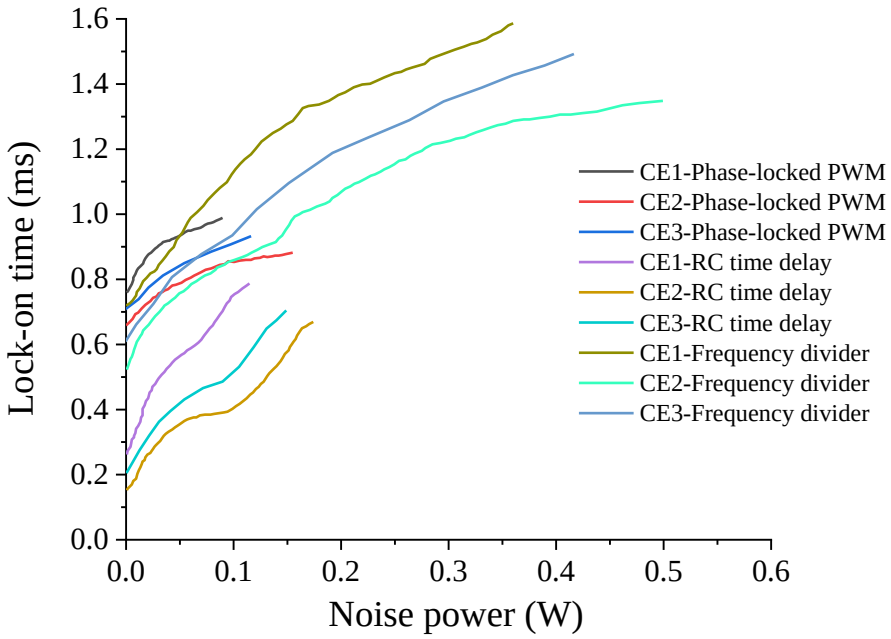


Fig. 4.11: Lock-on time comparison of the proposed PLL controllers associated with CE1 to CE4 under noise condition.

To indicate the resonant-frequency tracking performance of all nine methods, white noise of varying power is applied to the comparator input of the PLL in simulation and the time taken for the ZVS to achieve lock-on is measured. The simulation conditions are the same as experimental test, while the noise power is measured with respect to 1Ω, as shown in Fig. 4.12. The results are given in Fig. 4.11. The right hand side of each plot indicates where the ability to achieve lock-on was lost due to the adverse effects of noise. As can be seen, CE2 (anti-parallel diode current estimator) shows the best noise tolerance among all current estimators regardless of PLL controller type. The frequency divider controller with CE2 gives the best result overall and is able to handle up to 0.5W noise

power. In terms of the lock-on time, at a given noise power level, CE2 shows the shortest lock-on time among all the current estimators for all three gate-signal generators.

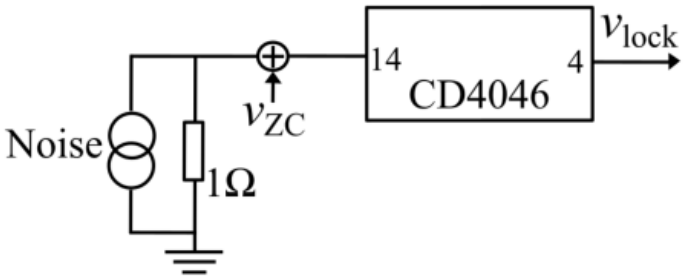


Fig. 4.12: The block diagram of the system noise test.

The controller noise immunity is significantly improved by the frequency divider approach. This can be explained that as the noise power level increases, the VCO will be affected and this appears as phase noise on the output of the VCO. In general, phase noise can be generated by PLL itself (e.g. phase detector dominates the noise source within the loop bandwidth while VCO is the dominant noise source outside the loop bandwidth), frequency divider and the resonant circuit [4.25]. Phase noise from frequency division is negligible when division ratio is small (i.e. 2 or 3), and it is insignificant when PLL operates at low frequencies. Therefore, the overall PLL noise performance is mainly determined by the resonant circuit [4.26]. The noise reduction for a given frequency division is $20\log_{10}n$, where n is the division ratio [4.25]. Hence, a frequency divide-by-two results in an improvement of 6dB (or $20\log_{10}2$) for phase noise correlated to the carrier frequency (VCO centre frequency), and 3dB (or $10\log_{10}2$) improvement for the uncorrelated phase noise [4.26], making a practical and effective way to reduce phase noise of the PLL.

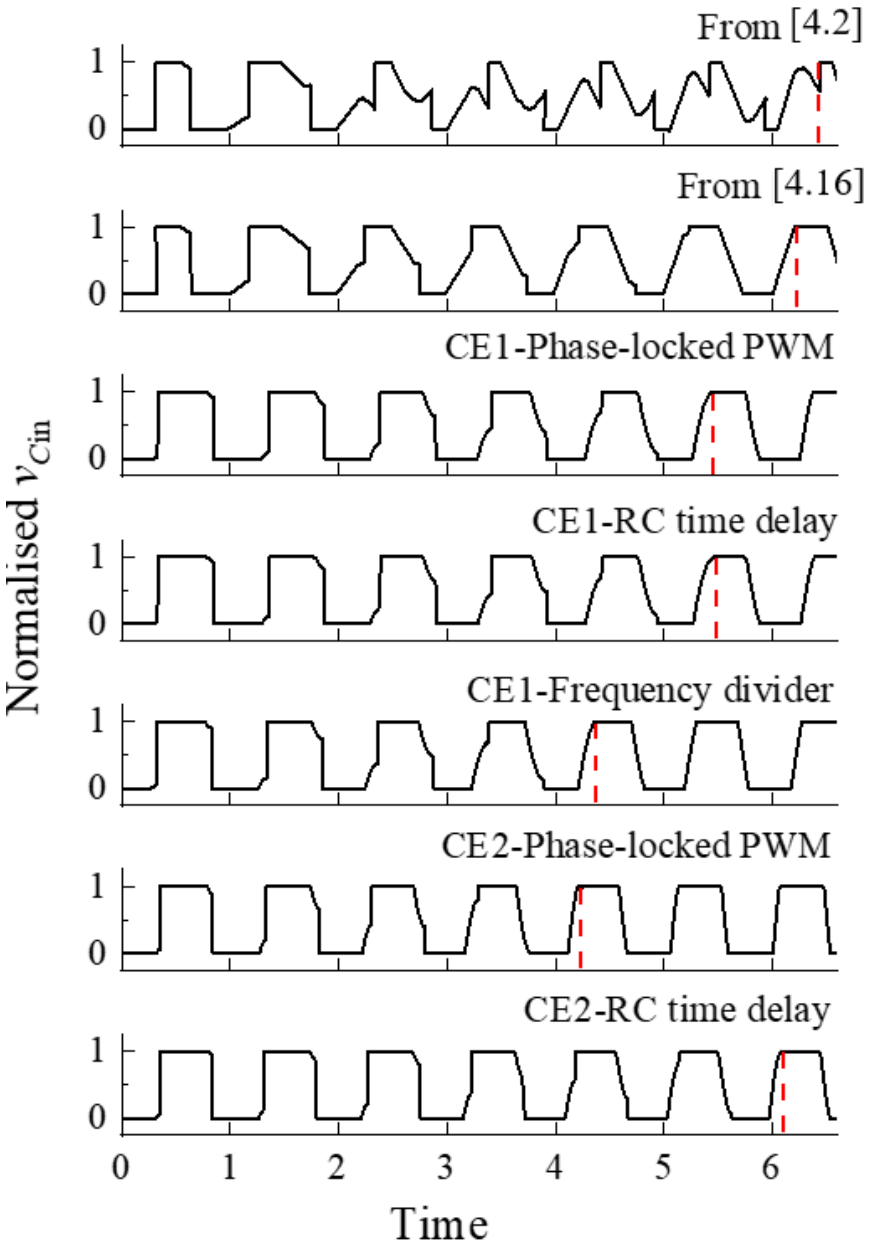
4.6.2 Start-up period

The start-up period of the proposed control methods associated with different current estimation methods are compared with previous art and shown in Fig.

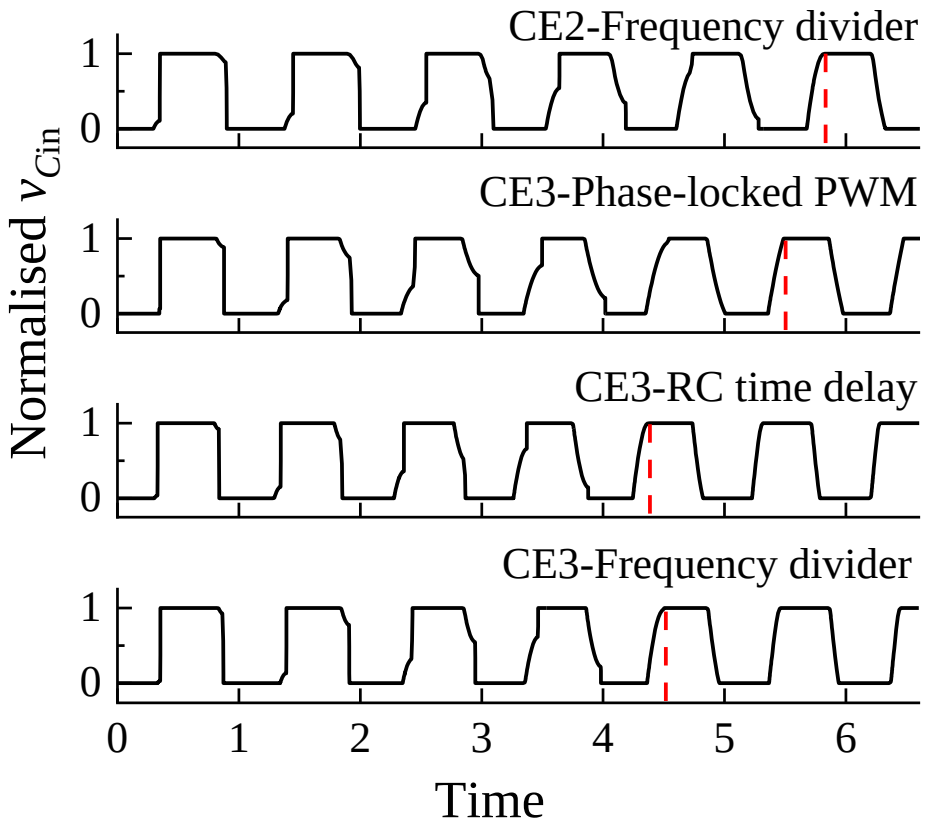
4.13. In this simulation test, each method is implemented in SPICE without adding noise. To ensure a fair comparison, the time scale is presented in terms of switching period, and v_{Cin} is normalised to unity.

Fig. 4.13, the top plot shows the start-up period of a fixed deadtime control presented in [4.2]. Seven cycles are required for the switching voltage to reach the positive rail during a single deadtime whereafter the system reaches steady state. The second plot from top shows a dynamically-adjusted control design presented in [4.27] with seven cycles required to reach V_{dc} in a single deadtime.

All the proposed control approaches shown in Fig. 4.13 demonstrate improved performance in terms of reaching the steady state with a reduced lock-on period. The best approach, CE2 with phase-locked PWM, requires only five cycles to enable the PT input voltage to meet the positive DC rail. For [4.2] and [4.27], the optimum deadtime is detected in each resonant cycle and a total feedback loop phase angle of integer multiple of is satisfied, therefore dynamic phase compensation is necessary every time the resonant frequency changes which is not desirable for fast-tracking.


From [4.2]
From [4.16]
CE1-Phase-locked PWM
CE1-RC time delay
CE1-Frequency divider
CE2-Phase-locked PWM
CE2-RC time delay
Normalised v_{Cin}
1
0
0
1
2
3
4
5
6
Time

(a)



(b)

Fig. 4.13: Comparison of start-up period. (a) top to bottom: previous art from [4.2] and [4.27], CE1 associated with phase-locked PWM, RC time delay and frequency divider, respectively. CE2 with phase-locked PWM and RC time delay. (b) top to bottom: CE2 employed with Frequency divider. CE3 implemented with phase-locked PWM, RC time delay and frequency divider, respectively.

The methods proposed in this thesis show the best performance since, during the system start-up, the VCO initially works at its minimum frequency, which is set to be near the resonant frequency. Thus, the PT should be excited and operated in the resonant modes more quickly. For a practical implementation of the PT-based converter control, when changes in optimum operating frequency caused by load and temperature variation are considered, the proposed methods are more advantageous since the PLL controller is able to lock on to the optimum frequency irrespective of operating conditions and temperature effects. Fewer

lock-on periods enable fast tracking of the optimum frequency thereby improving the overall system efficiency.

In terms of flexible control of deadtime, the phase-locked PWM and RC time delay approaches also perform better than the frequency divider approach. This is highly desirable when output voltage regulation is required for a practical implementation of a PT-based power supply. Approaches for regulating output voltage reported in the literature include: employing a hysteresis controller [4.28]; operating frequency modulation (thereby changing the reactance of the resonant tank) [4.29]; and adjusting the deadtime [4.3][4.27] (hence the duty cycle).

Reference [4.30] indicates that it is difficult to regulate the output voltage while achieving ZVS with deadtime control and frequency control simultaneously. The proposed phase-locked PWM and RC time delay approaches show potential advantages for a simple and flexible deadtime control to regulate the output since the deadtime interval can be controlled both symmetrically and asymmetrically by adjusting the reference voltages.

4.6.3 Overall performance

The overall performance of all control nine approaches is summarised in Table 4.1. The choice of control approach must be taken holistically, bearing in mind need for flexibility, noise immunity, system complexity and tracking speed.

Although the control circuit presented in this thesis was designed for PT-based inductorless resonant converters, the findings are likely to be generally applicable to other resonant converters [4.15][4.31][4.32] because this approach provides precise phase detection, wide frequency-locking range, adjustable deadtime, small time delay and ease of implementation.

Table 4.1: Summary of different control approaches

	Phase-locked PWM			RC time delay			Frequency divider		
	CE1	CE2	CE3	CE1	CE2	CE3	CE1	CE2	CE3
A*	Symmetrical and adjustable deadtime			Symmetrical, asymmetrical adjustable deadtime			Fixed deadtime		
B*	6	5	5	6	7	6	6	5	5
C*	10			10			40		
D*	0.09	0.15	0.11	0.11	0.17	0.15	0.36	0.5	0.41
E*	140	125	132	111	94	100	225	191	212

A*: Flexibility, B*: Start-up period (cycles), C*: VCO range (kHz)
D*: Maximum circuit noise tolerance (W), E*: Number of lock-on cycles at maximum noise level

4.7 Chapter conclusions

A PLL-based control system for achieving ZVS operation in a PT-based resonant power supply is presented in this chapter. The cooperation between current estimation circuits described in Chapter III and PLL controller feedback design were described in detail. By measuring the zero-crossing points of the estimated current, the switching waveforms are locked on to the resonant current while simultaneously ensuring $\pi/2$ radians dead time and hence achieving zero-voltage switching for all loads. The control system is implemented using different current estimation circuits with steering logic and gate signal generators based on CD4046 PLL. A ring-dot radial mode PT with a matched resistive load is used

and both simulation and experimental results demonstrate successful ZVS operation. Nine implementations are presented and evaluated, each with its own advantages in terms of flexibility, circuit noise condition, power consumption and lock-on time. The phase-locked PWM with CE2 approach shows excellent start-up performance with only five cycles required to achieve steady state. This ensures a fast-tracking of resonant frequency change. Frequency divider control performs better at circuit noise immunity and has potential advantages for high frequency operation. In addition, CE2 experiences shorter lock-on time under noise conditions and has higher circuit noise tolerance.

4.8 References

[4.1] V. C. Alfredo, “50 years of piezoelectric transformers. Trends in the technology,” in *Proc. Symp. D Mater. Devices Smart Syst.,* vol. 785, 2003, pp.33-44.

[4.2] M. S. Rødgaard, "Piezoelectric transformer based power converters design and control," Ph.D dissertation, Dept. Elect. Eng., Tech. Univ. Denmark, Kongens Lyngby, Denmark, 2012.

[4.3] M. S. Roedgaard, M. Weirich and M. A. E. Andersen, "Forward Conduction Mode Controlled Piezoelectric Transformer-Based PFC LED Drive," in *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4841-4849, 2013.

[4.4] K. S. Meyer, M. A. E. Andersen, and F. Jensen, “Parameterized analysis of zero voltage switching in resonant converters for optimal electrode layout of Piezoelectric Transformers,” *IEEE Annual Power Electronics Specialists Conference*, 2008, pp. 2543–2548.

[4.5] M. Khanna, R. Burgos, Q. Wang, K. D. T. Ngo, and A. V. Carazo, "New Tunable Piezoelectric Transformers and Their Application in DC-DC Converters," *IEEE Trans. Power Electron.,* vol. 32, no. 12, pp. 8974–8978, 2017.

[4.6] M. Ryu, S. Choi, S. Lee, and B. H. Cho, "A New Piezoelectric Transformer Driving Topology for Universal Input AC/DC Adapter using a Constant Frequency PWM Control." in *Proc. 21st Annu. IEEE Appl. Power Electron. Conf. Expo.,* Dallas, TX, USA, 2006, pp. 4-10.

[4.7] S. Choi, M. Ryu, S. Lee, and B. H. Cho, "Adaptive Frequency Control Strategy for Piezoelectric Transformer in AC/DC Adapter Applications using Phase-Detector," in *Proc. 21th Annu. IEEE Appl. Power Electron. Conf. Expo.,* Dallas, TX, USA, 2006, pp. 1296–1299.

[4.8] J. Diaz, M. J. Prieto, F. Nuño, J. A. Martín-Ramos, and J. A. Martínez, "Driving piezoelectric-Transformer-based DC/DC converters using pulse density modulation," *IEEE Energy Conversion Congress and Exposition,* 2017, pp. 5698–5703.

[4.9] S. T. Yun, J. M. Sim, J. H. Park, S. J. Choi, and B. H. Cho, "Adaptive phase control method for load variation of resonant converter with Piezoelectric Transformer," in *Proc. 7th Int. Conf. Power Electron. Drive Syst.,* Bangkok, Thailand, 2007, pp. 164–168.

[4.10] S. Hamamuraa, D. Kurose, T. Ninomiya, and M. Yamamoto, "New Control Method of Piezoelectric Transformer Converter by PWM and PFM for Wide Range of Input Voltage." in *Proc. 7th Int. Power Electron. Cong.,* Acapulco, Mexico, 2000, pp. 3-8.

[4.11] B. Ju, W. Shao, D. Huang, Y. Ye, and Z. Feng, “A topology for inductorless actuation of piezoelectric transformer with special driving waveform,” *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1346–1354, 2017.

[4.12] M. Ekhtiari, T. Andersen, M. A. E. Andersen, and Z. Zhang, “Dynamic Optimum Dead Time in Piezoelectric Transformer-Based Switch-Mode Power Supplies,” *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 783-793, 2017.

[4.13] G. Ivensky, I. Zafrany, and S. Ben-Yaakov, “Generic operational characteristics of piezoelectric transformers,” *IEEE Trans. Power Electron.*, vol. 17, no. 6, pp. 1049–1057, 2002.

[4.14] C.Y. Lin, “Design and Analysis of Piezoelectric Transformer Converters,” Ph.D dissertation, Dept. Elect. Eng., Virgin. Poly. Inst. State Univ., Blacksburg, Virginia, USA, 1997.

[4.15] A. J. Gilbert, M. P. Foster, D. A. Stone, and C. M. Bingham, “Phase Locked Loop (PLL) based self-oscillating controller for LCC resonant converters.” in *Proc. 4th IET Int. Conf. Power Electron., Mach. Drives,* York, UK, 2008, pp. 446-450.

[4.16] M. Ekhtiari, T. G. Zsurzsan, M. A. E. Andersen, and Z. Zhang, “Optimum Phase Shift in the Self-Oscillating Loop for Piezoelectric-Transformer-Based Power Converters,” in *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 8101–8109, 2018.

[4.17] M. P. Foster, J. N. Davidson, E. L. Horsley, and D. A. Stone, “Critical Design Criterion for Achieving Zero Voltage Switching in Inductorless

Half-Bridge-Driven Piezoelectric-Transformer-Based Power Supplies," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 5057–5066, 2016.

[4.18] M. S. Rødgaard, "Bi-directional piezoelectric transformer based converter for high-voltage capacitive applications," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2015, pp. 1993–1998.

[4.19] F. He, R. Ribas, C. Lahuec, and M. Jézéquel, "Discussion on the general oscillation startup condition and the Barkhausen criterion," *Analog Integrated Circuits and Signal Processing*, 2009, no. 2, pp: 215-221.

[4.20] D. K. Morgan, "CD4046B Phase-Locked Loop: A Versatile Building Block for Micropower Digital and Analog Applications,"*Application Report SCHA002A, Texas Instruments*, 2003.

[4.21] M. Ekhtiari, T. Andersen, Z. Zhang, and M. A. E. Andersen, "Digitized self-oscillating loop for piezoelectric transformer-based power converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Long Beach, CA, USA, 2016, pp. 1430-1436.

[4.22] Z. Yang, J. Forrester, J. N. Davidson, M. P. Foster, and D. A. Stone, "Resonant current estimation and phase-locked loop feedback design for piezoelectric transformer-based power supplies," *IEEE Trans. Power Electron.*, pp. 1–1, 2020.

[4.23] J. Forrester, *effect of spurious resonant modes on the operaiton of radial mode piezoelectric transformer*. .

[4.24] J. Forrester, J. Davidson, M. Foster, and D. Stone, "*Equivalent Circuit Parameter Extraction Methods for Piezoelectric Transformers*."

International Exhibition and Conference for Power Electronics, 2018, pp. 1-8.

[4.25] R. E. Best, "*Phase-locked loops: design, simulation, and applications*." McGraw-Hill Education, 2007.

[4.26] D. Banerjee, "PLL Performance, Simulation, and Design," 4th edition, *Sirirajmedj Com*, 2006

[4.27] M. Ekhtiari, T. Andersen, M. A. E. Andersen, and Z. Zhang, "Dynamic Optimum Dead Time in Piezoelectric Transformer-Based Switch-Mode Power Supplies," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 783-793, 2017.

[4.28] J. Díaz, F. Nuno, M. J. Prieto, J. A. Martín-Ramos, and P. J. Villegas Saiz, "Closing a second feedback loop in a DC-DC converter based on a piezoelectric transformer," *IEEE Trans. Power Electron*., vol. 22, no. 6, pp. 2195-2201, 2007.

[4.29] T. Zaitsu, T. Shigehisa, T. Inoue, M. Shoyama, and T. Ninomiya, "Piezoelectric Transformer Converter with Frequency Control." in *Proc. 17th Int. Telecom. Energy. Conf.,* The Hague, Netherlands, 2002, pp. 175-180.

[4.30] M. Radecker, F. Bisogno, and M. Herfurth, "Control circuit for a switch unit of a clocked power supply circuit, and resonance converter." U. S. Patent US7,746,671. Jun. 29, 2010.

[4.31] M. P. Foster, H. I. Sewell, C. M. Bingham, D. A. Stone, and D. Howe, "Methodologies for the design of LCC voltage-output resonant converters," *IEE Proc. Electr. Power Appl.*, vol. 153, no. 4, pp. 559–567, 2006.

[4.32] R. L. Lin, and W. C. Ju, “LLC DC/DC Resonant Converter with PLL Control Scheme,”in *22nd Annu. IEEE appl. Power electron. Conf. Expo.*, Anaheim, CA, USA, 2007.

Chapter V

Hysteresis control for output voltage regulation

This Chapter presents a technique to regulate the output voltage of a half-bridge inductorless PT-based resonant converter. The current estimation and PLL control techniques, demonstrated in Chapter III and Chapter IV, are used to achieve ZVS and form part of the feedback loop for voltage regulation. A burst-mode hysteresis control, which modifies the on/off periods of the MOSFETs, is employed to provide output voltage regulation of the DC/DC converter. The mechanical vibration initialisation and non-instant stop behaviour of a PT, which causes inaccuracy of voltage regulation, has been analysed. The prototype converter implemented in Chapter IV is further extended with a second feedback loop to achieve voltage regulation. Both experimental and simulation results demonstrate the operation of the system, and an output voltage at the matched load condition has been achieved. The fast system start-up by using a PLL controller which demonstrated in Chapter IV is also validated by the experimental results. The output characteristics of regulation limit, load and line regulation are described in detail.

5.1 Introduction

Following the resonant current estimation techniques described in Chapter III, and ZVS-achieving PLL control techniques demonstrated in Chapter IV, this chapter employs these techniques and extends the operation of the converter based on the circuit presented Chapter IV, to provide output voltage regulation using a burst-mode hysteresis controller.

To regulate the output voltage, burst-mode modulation has been shown to provide superior performance when compared with pulse-frequency modulation (PFM) and pulse width modulation (PWM) since it provides a higher efficiency and lower harmonics [5.1][5.2]. However, traditional burst-mode modulation uses a fixed switching frequency, and this is not desirable for PT-based converter since: 1) load variation is limited due to the narrow control bandwidth; 2) the resonant frequency of the PT will shift due to variations in temperature and load; and 3) a time delay is introduced during the start-up and stop periods as a result of the mechanical vibration of the PT, leading to inaccuracy of voltage regulation. Therefore, additional compensation is required regulate output voltage and maximise overall efficiency of a PT-based converter.

In this chapter, a phase-locked loop (PLL) controller and burst mode controller with a secondary-side resonant current estimator (CE3) is presented, to regulate the output voltage while maintaining ZVS operation. By estimating the resonant using only secondary side measurements interference from the MOSFET switching events are avoided improving robustness to noise. The PLL locks onto the estimated resonant current providing a synchronised square wave from which the MOSFET gate signals are derived. Adherence to the critical criterion described in [5.3] ensures that a particular design can achieve ZVS [5.3]. The output voltage is regulated through a burst mode controller by adjusting the on/off periods of the switches. The proposed control system is implemented and experimentally validated using a ring dot radial mode PT.

5.2 Operation of the proposed control system

The proposed control system includes a resonant current estimator, a burst-mode output voltage controller and a PLL ZVS controller, as shown in Fig. 5.1. Since the resonant current is internal to the PT and cannot be measured directly, a resonant current estimator is employed after the PT output section, using CE3 to

reconstruct i_{L1} for the PLL controller. Therefore, the resonant current is locked on to by the PLL controller and in-phase gate drive signals are generated through steering logic. Subsequently, the secondary-side voltage is rectified to form a DC output voltage which is regulated through burst-mode modulation. Finally, the on/off periods of the MOSFETs are dynamically adjusted from the burst-mode signal generated by a hysteresis window with voltage regulation limit.

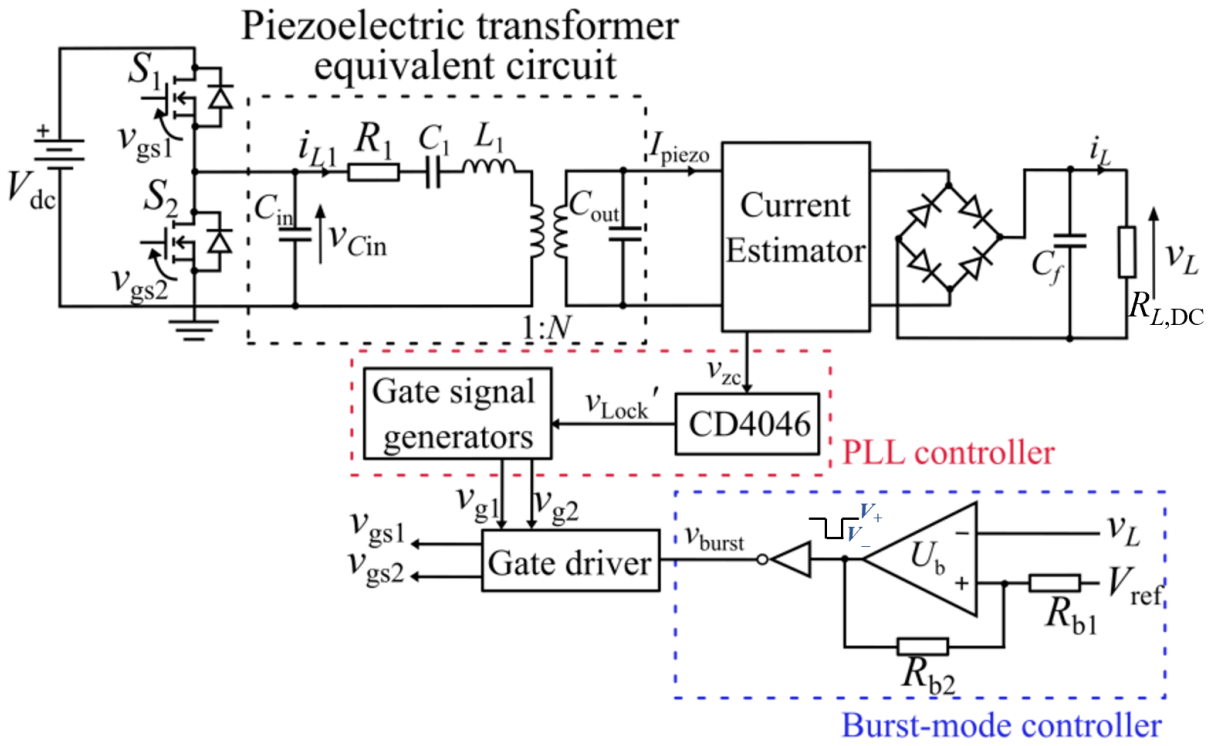


Fig. 5.1: Circuit block diagram of the proposed burst-mode hysteresis control.

The basic circuit operation and switching waveforms of an inductorless half-bridge PT-based converter has been described in Chapter III. The current estimator and PLL controller have been demonstrated in Chapter III and Chapter IV respectively, and therefore the detailed analysis of both is not included in this Chapter.

5.3 Burst-model control

5.3.1 Resonant behaviour of a PT

To regulate the output voltage, the power supply operates in burst mode by controlling the on/off periods of MOSFETs according to regulation requirement. A typical PT response in burst-mode modulation is shown in Fig. 5.2. As can be seen, there are two transition periods when PT operates in burst-mode. The start-up transition time is introduced since the PT should be excited to initiate mechanical vibration until it operates in resonant mode. This start-up period is largely dependent on the control circuit as explained in Chapter IV. For the PT stop period, however, the mechanical vibration cannot stop instantly due to its high quality factor (i.e. energy stored mechanically must first be released). The start-up and stop transitions are highlighted in blue and red, respectively. Only a single gate signal is shown for the sake of clarity.

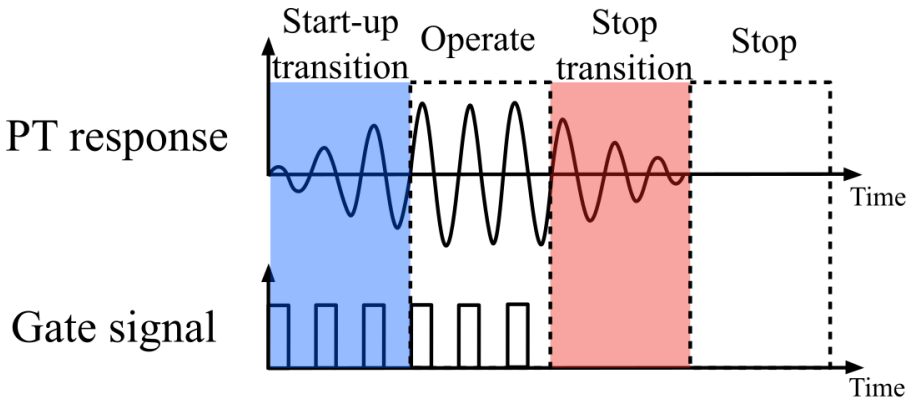


Fig. 5.2: PT response and gate signals during burst-mode operation

5.3.2 Hysteresis controller and temporal behaviour

The output voltage, v_L, and the burst-mode (hysteresis controller) voltage, v_{burst}, are shown in Fig. 5.3. Signal v_{burst} modulates the gate signals at a low-frequency controlling the flow of energy to the load, by enabling the gate driver when it is low and disable the gate driver when it is high. As can be seen, v_L travels between

a lower value, $v_{L(min)}$, and an upper value, $v_{L(max)}$, in response to the application of the burst-mode control pulse, v_{burst}. The burst-mode control pulse is obtained from a Schmitt trigger that compares the output voltage to an upper threshold value and a lower threshold value, the different between the threshold values being designated as $\Delta v_L'$. As can be seen the actual output voltage extends beyond the upper threshold limit due to finite time taken for energy stored within the PT to be delivered to the load, leading to a maximum value for the output voltage, $v_{L(max)}$. The output voltage also extends below the lower threshold level due to the finite time taken for the PT to start-up, leading to the minimum output voltage, $v_{L(min)}$. The difference between the upper and lower output voltage values is the output ripple voltage due to the burst-mode controller, $\Delta v_L = v_{L(max)} - v_{L(min)}$. The switching transitions described in Fig. 5.2 are also highlighted in red and blue. Since the direction of travel for v_L does not change the instant it crosses the upper/lower threshold levels the delays can result in inaccurate voltage regulation unless they are accounted for.

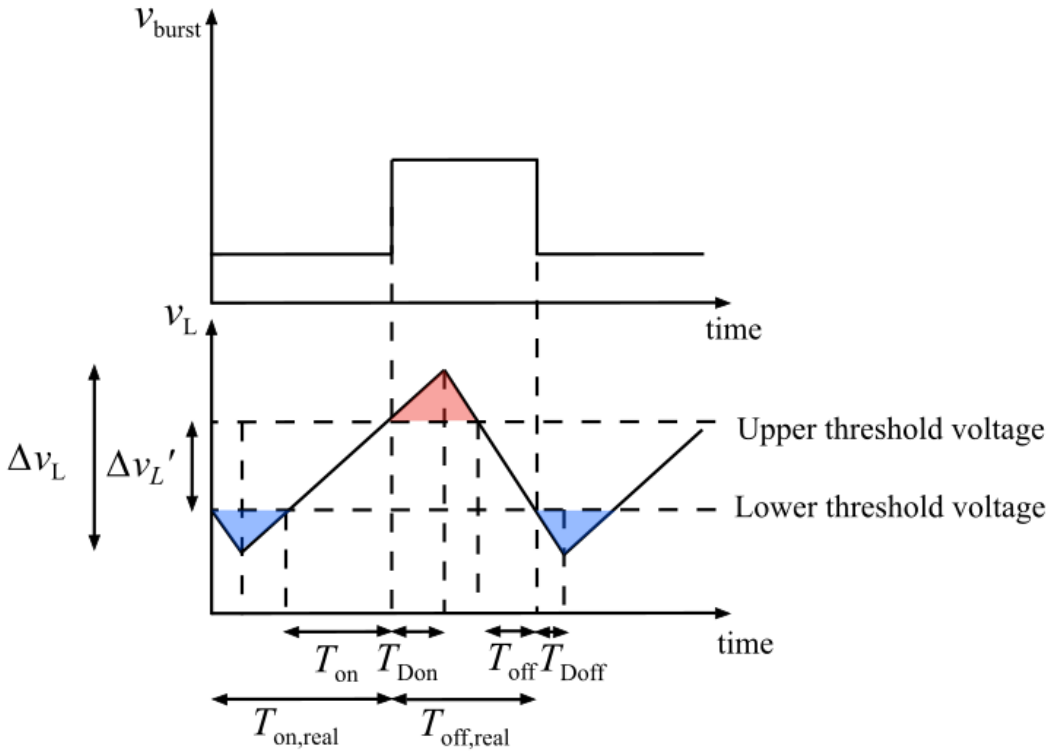


Fig. 5.3: Time delay due to PT response under burst-mode operation.

For the ideal case where the delay is zero, the on time (T_{on}) and off time (T_{off}) of burst-mode operation is given by

$$T_{\text{on}} = \frac{C_f \Delta v_{\text{L}}'}{I_{\text{piezo}} - I_{\text{L}}} \tag{5.1}$$

$$T_{\text{off}} = \frac{C_f \Delta v_{\text{L}}'}{I_{\text{L}}} \tag{5.2}$$

where I_{L} is the load current, C_f is the filter capacitor, I_{piezo} is the PT equivalent current source and $\Delta v_{\text{L}}'$ is the voltage ripple without time delay for an ideal case. If the PT operates continuously without burst mode modulation, then I_{piezo} equals I_{L}. When switching transition occurs, as shown in Fig. 5.3, the actual (measurable) voltage ripple Δv_{L} can be given as

$$\Delta v_{\text{L}} = \Delta v_{\text{L}}' \left(1 + \frac{T_{\text{Don}}}{T_{\text{off}}} + \frac{T_{\text{Doff}}}{T_{\text{on}}}\right) \tag{5.3}$$

where T_{Don} and T_{Doff} correspond to the time delay for the output voltage v_{L} reaching the maximum and minimum output voltage levels, respectively.

From equation (5.1) to (5.3), the real-world on-time ($T_{\text{on,real}}$) and real-world off-time ($T_{\text{off,real}}$) incorporating the effects of the time delays can be found

$$T_{\text{on,real}} = \frac{C_f \Delta v_{\text{L}}}{I_{\text{piezo}} - I_{\text{L}}} \tag{5.4}$$

$$T_{\text{off,real}} = \frac{C_f \Delta v_{\text{L}}}{I_{\text{L}}} \tag{5.5}$$

Therefore, the burst-mode frequency f_{burst} with transition time delay is given as

$$f_{\text{burst}} = \frac{(I_{\text{piezo}} - I_L)I_{\text{L}}}{C_f \Delta v_L I_{\text{piezo}}} \tag{5.6}$$

As can be seen from equation (5.6), for a given PT and filter capacitor, the voltage ripple Δv_{L} is inversely proportional to f_{burst}. Therefore, the burst frequency should be increased if a smaller Δv_L is required or a large value for C_f must be used.

5.3.3 Burst-mode operation for a PT-based converter

The burst-mode control signal v_{burst} is accomplished by comparing the output voltage (v_{L}) with a reference voltage (V_{Ref}) via a hysteresis window, as shown in Fig. 5.1. Thus, the PT drive stops when v_{L} meets the upper limit and it starts to operate again at the lower boundary. As can be seen, a Schmitt trigger comparator U_{b} is used to implement the hysteresis window, and the window size is determined by R_{b1} and R_{b2} while the reference signal V_{ref} sets the centre of the window. The burst mode signal is inverted before applied to the gate driver since IR2110 is enabled when v_{burst} is low and vice versa. The burst mode signal v_{burst} controls the gate signals v_{g1} and v_{g2} from PLL controller via the gate driver thereby modifies the on/off periods of the MOSFETs. The upper and lower threshold voltage of the hysteresis window (V_{TH} and V_{TL}) are found by

$$V_{\text{TH}} = V_{\text{ref}} \frac{R_{\text{b2}}}{R_{\text{b1}} + R_{\text{b2}}} + V_{+} \frac{R_{\text{b1}}}{R_{\text{b1}} + R_{\text{b2}}} \tag{5.7}$$

$$V_{\text{TL}} = V_{\text{ref}} \frac{R_{\text{b2}}}{R_{\text{b1}} + R_{\text{b2}}} + V_{-} \frac{R_{\text{b1}}}{R_{\text{b1}} + R_{\text{b2}}} \tag{5.8}$$

Where V_{+} and V_{-} are positive and negative output voltage of the comparator.

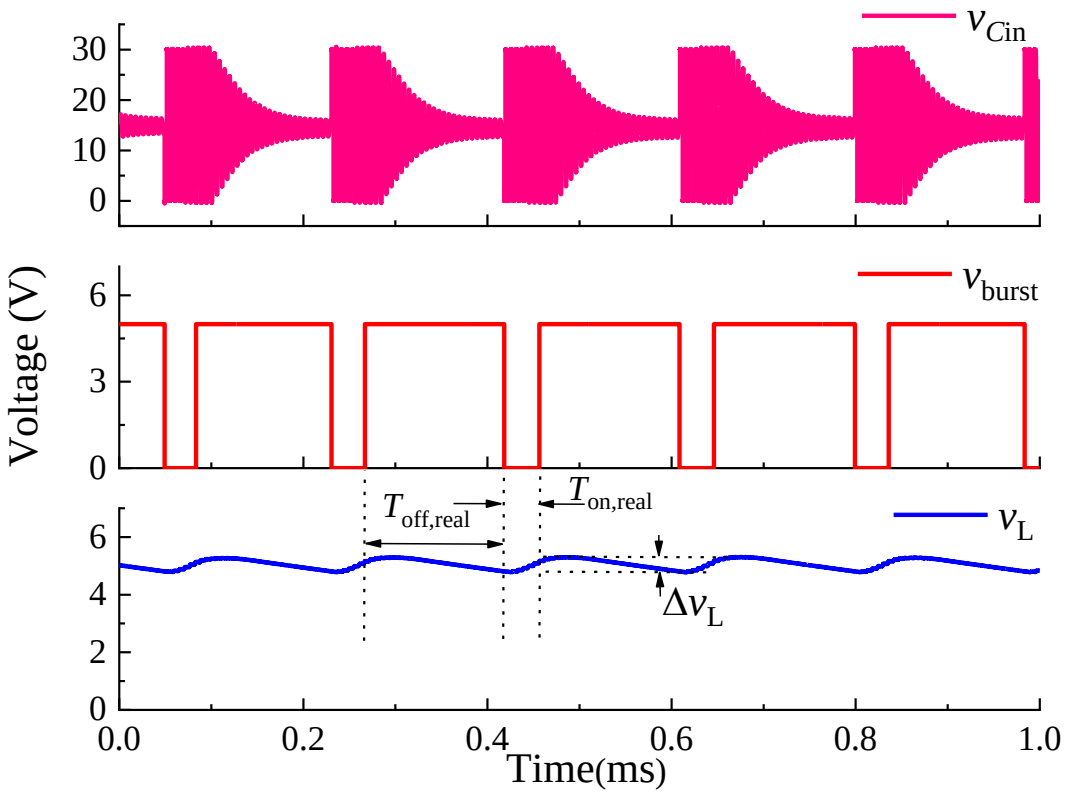


Fig. 5.4: Operating waveforms of the burst-mode control.

Fig. 5.4 shows the typical waveforms of the resonant converter under burst-mode operation. During burst mode operation, the piezoelectric transformer is considered to be a current source I_{piezo} that charges the filter capacitor C_f until v_L reaches the upper regulation limit and the load discharges C_f until v_L reaches the lower boundary. As can be seen from Fig. 5.4, the voltage ripple Δv_{L} is controlled by the on/off periods of the switches via the burst-mode signal v_{burst}. The start-up and stop transition of the PT switching waveform cause output voltage v_{L} to overshoot as described in Fig. 5.3.

5.4 Experimental results

To validate the proposed control method, the prototype half-bridge PT-based resonant converter implemented in Chapter IV with frequency divider PLL controller associated with current estimator 3 (CE3) is used. A ring-dot radial-mode PT with a natural frequency of 145.2 kHz is used for the test, with the

following extracted equivalent circuit component values: C_{in}=0.43nF, C_{out}=1.14nF, L_1=17.2mH, C_1=77.8pF, R_1=12.Ω, N=0.94, Q=1190 (the PT is same as the one used in Chapter IV). The burst-mode control signal v_{burst} is connected to the shutdown pin of the IR2110 gate driver IC to achieve burst-mode control.

5.4.1 ZVS performance

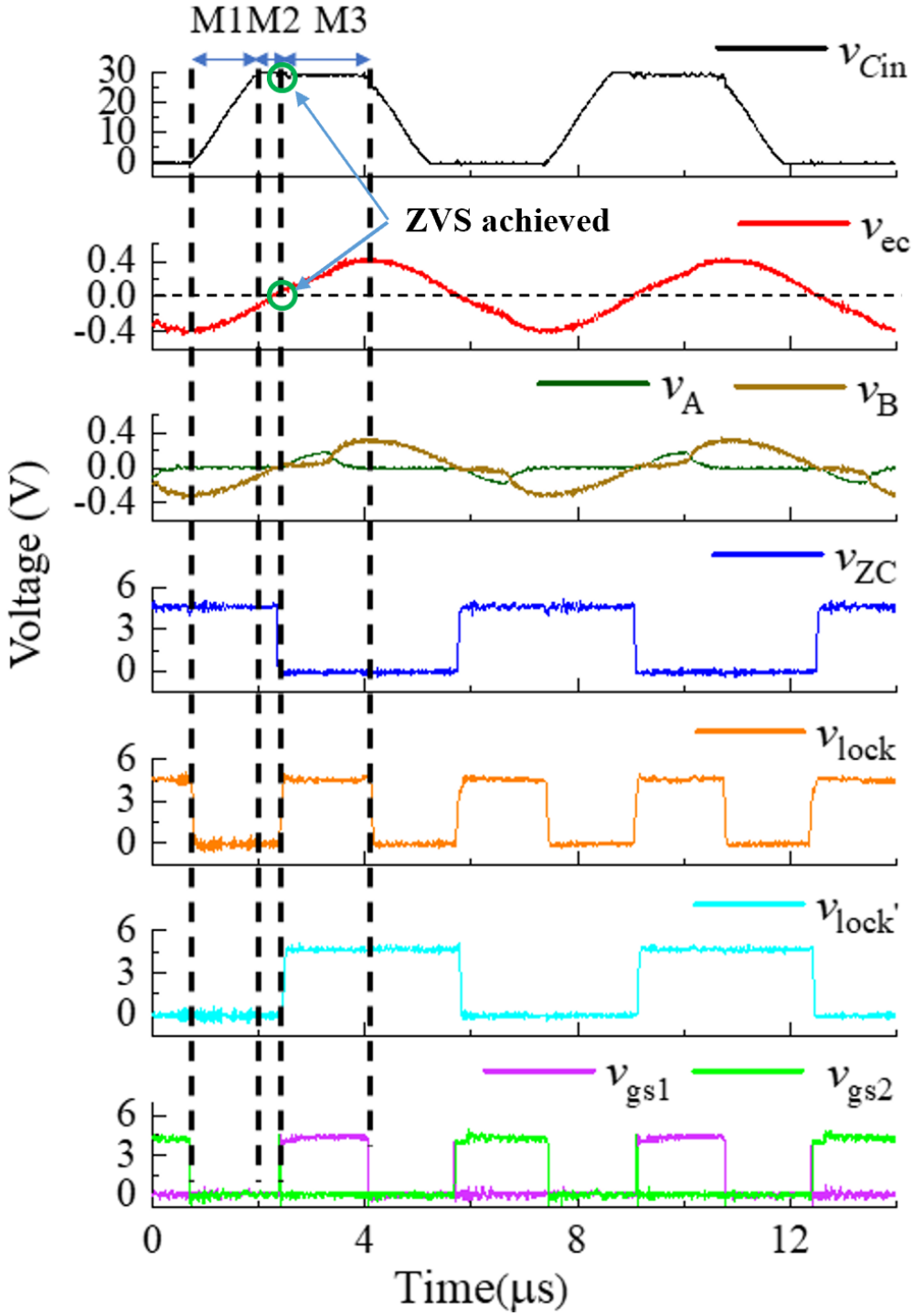


Fig. 5.5: Experimental results of the proposed control method for ZVS operation.

The experimental waveforms of the proposed control circuit for ZVS operation are shown in Fig. 5.5. The key observations from this experiment will be repeated here to act a springboard for the subsequent discussions. To ensure adequate lock range with acceptable component tolerance, the PLL is restricted to operate between 270 kHz to 290 kHz (i.e. in the range of twice the resonant frequency of the PT). An 820 Ω load (corresponds to 1 kΩ matched load at PT output) is used to validate the proposed controller, since this is the worst case operating condition for achieving ZVS.

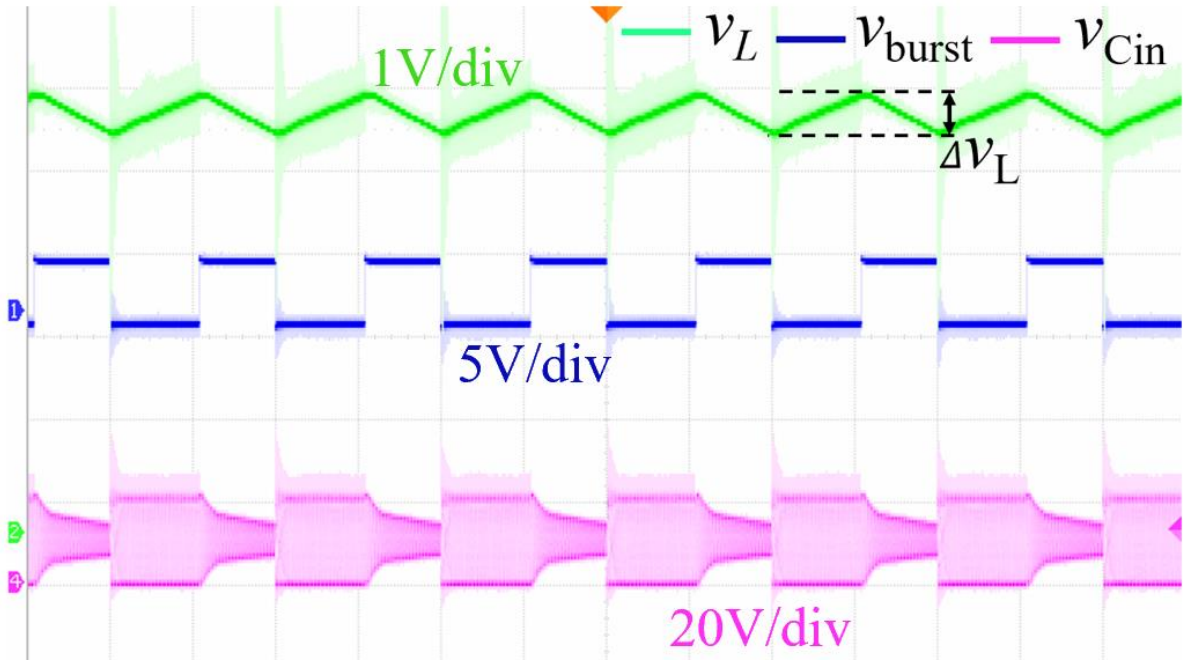
During M1 and M2, the bridge rectifier is conducting and so the PT output is clamped to the load voltage v_L and, therefore, $i_{C\mathrm{out}}$ and its derivative signal v_{A} are zero, while PT output current i_{out} and its scaled version v_{B} is dominated by the resonant current. In M3, C_{out} is being charged, and so $i_{C\mathrm{out}}$ and its scaled version v_{A} increase accordingly. v_{A} and v_{B} are combined to reconstruct the estimated current v_{ec}, and are used to generate the feedback signal v_{ZC} for the control circuit.

As can be seen from Fig. 5.5, the phase comparator input signals v_{zc} and v_{lock} are frequency- and phase-matched, demonstrating a PLL locked-on condition. The resonant current is estimated, reconstructed as v_{ec} and applied to a zero-crossing detector to generate v_{zc}, clearly indicating the zero crossings for ZVS operation. The gate drive signals are generated through steering logic with $\pi/2$ deadtime and align with the feedback signal v_{zc}. ZVS is clearly achievable since $v_{C\mathrm{in}}$ reaches V_{dc} during the deadtime period.

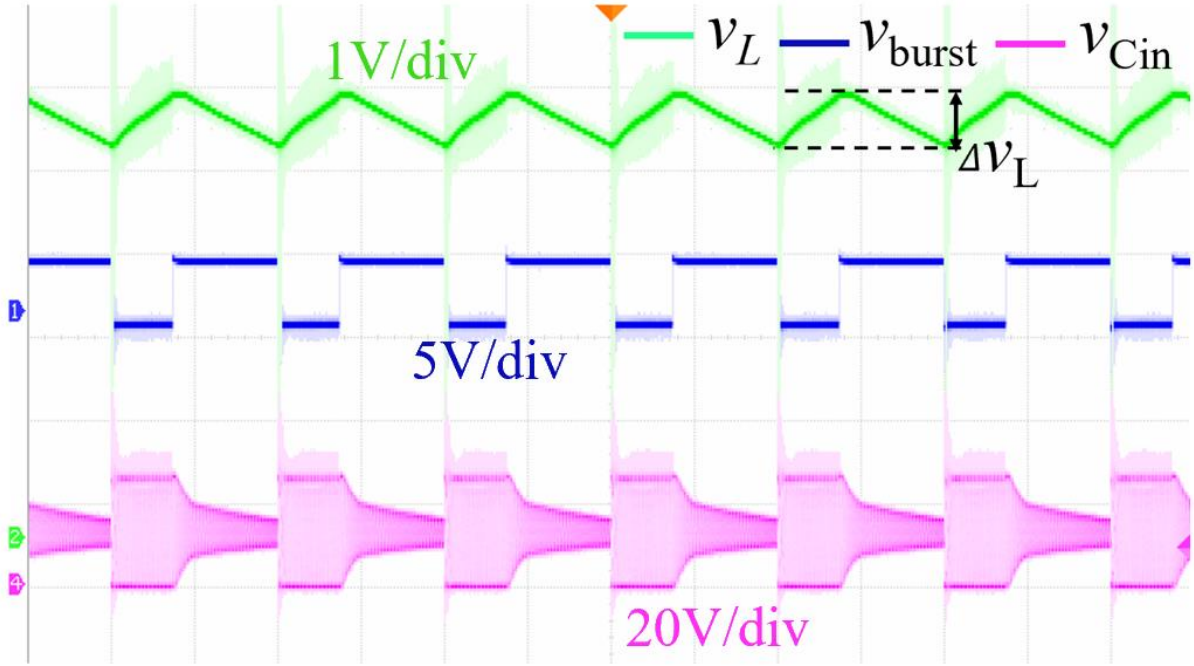
5.4.2 Voltage regulation performance

Fig. 5.6 shows the 5V output voltage regulation at 4.6 kΩ load under different operating conditions. A 1 kHz burst signal is set by the hysteresis window with different duty cycles to achieve 5V output. As can be seen, the proposed converter

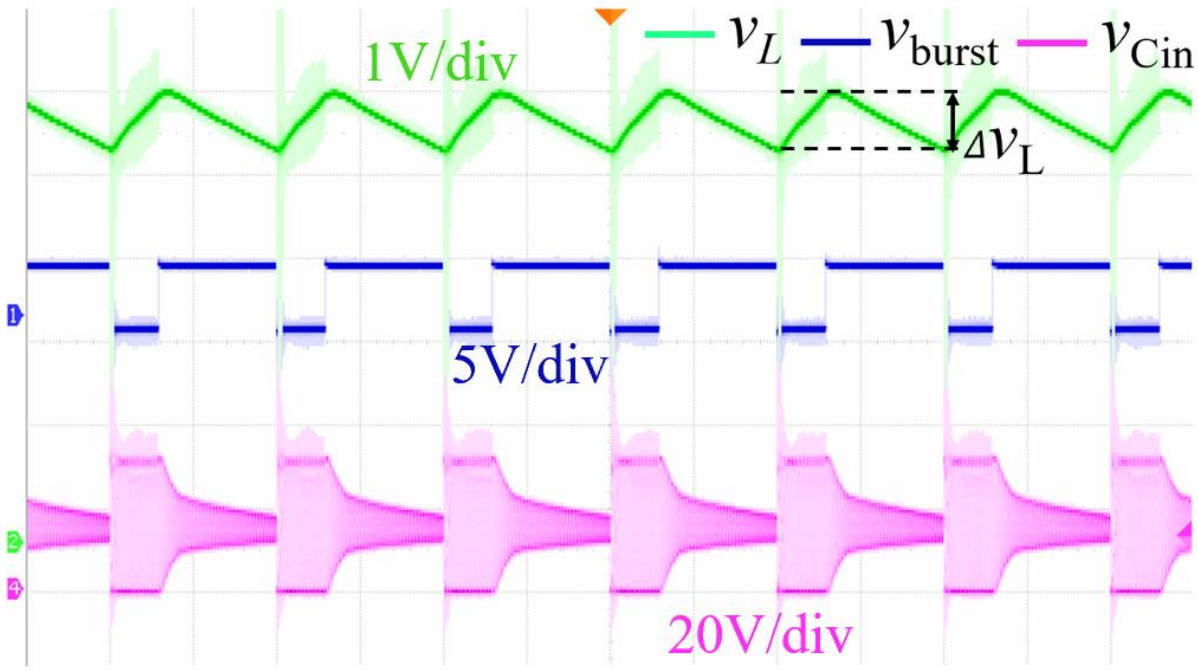
successfully regulates the output voltage at 5V with a 33.3% variation of the input voltage. It is shown that at a given burst frequency, the duty cycle is proportional to the output voltage ripple. Similarly, for a given duty cycle, the burst frequency is inversely proportional to the output voltage ripple, as indicated in equation (5.6). Voltage regulation specifications are summarised in Table 5.1.



(a)



(b)



(c)

Fig. 5.6: Voltage regulation performance of the prototype PT-based converter. v_L is regulation at 5V with a 1kHz burst signal. (a) 20V input with 0.46 duty cycle, (b) 25V input with 0.63 duty cycle and (c) 30V input with 0.71 duty cycle (PT input capacitance voltage v_{Cin} 20V/div, burst signal v_{burst} 5V/div and output voltage v_L 1V/div, 500μs/div).

Table 5.1: Voltage regulation specifications

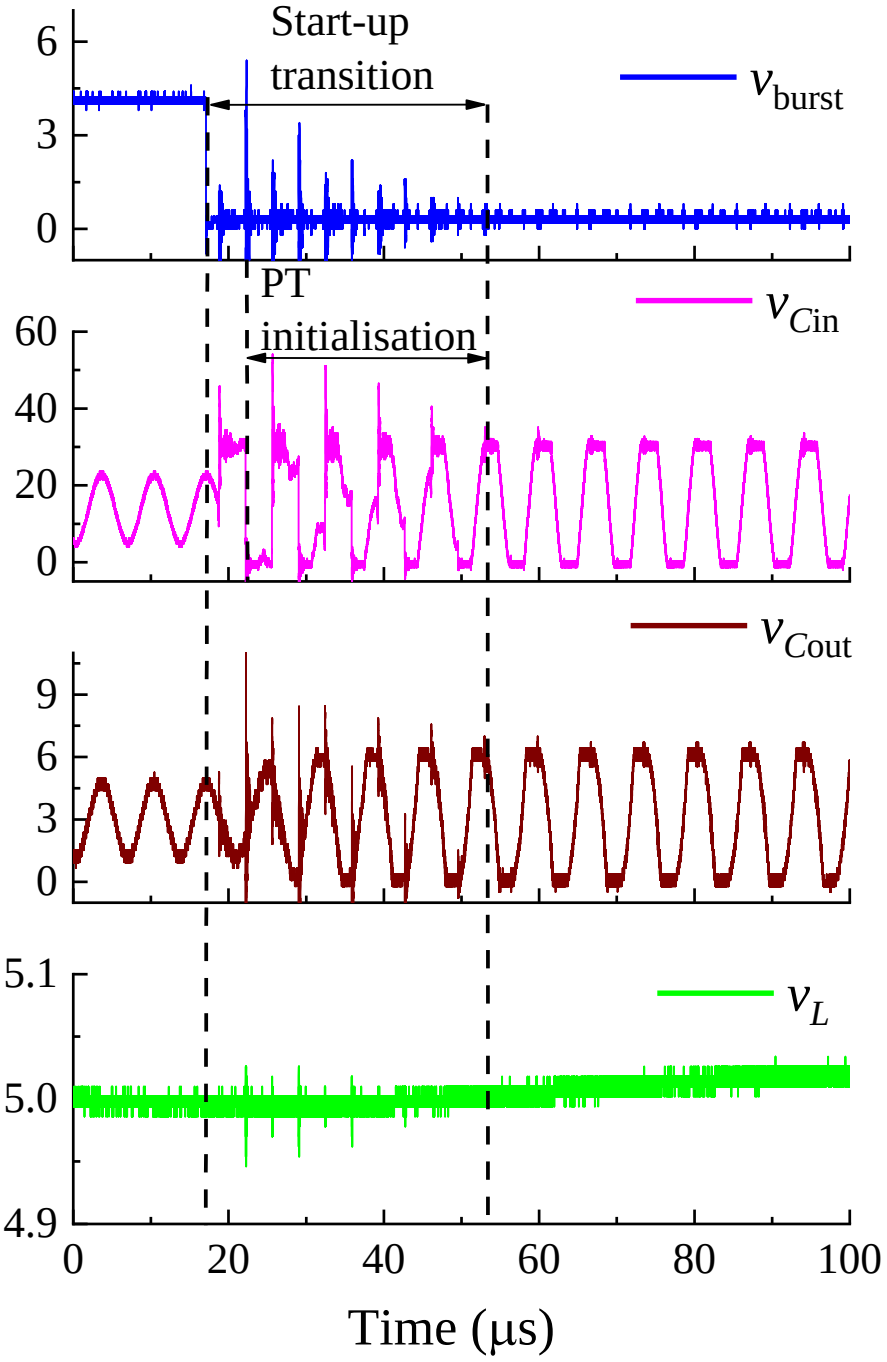
Output voltage v_L	Input voltage V_{dc}	Burst frequency f_{burst}	Duty cycle	Voltage ripple Δv_L
5V	20V	1kHz	0.66	500mV
5V	25V	1kHz	0.73	700mV
5V	30V	1kHz	0.77	750mV

5.4.3 Start-up and stop transition

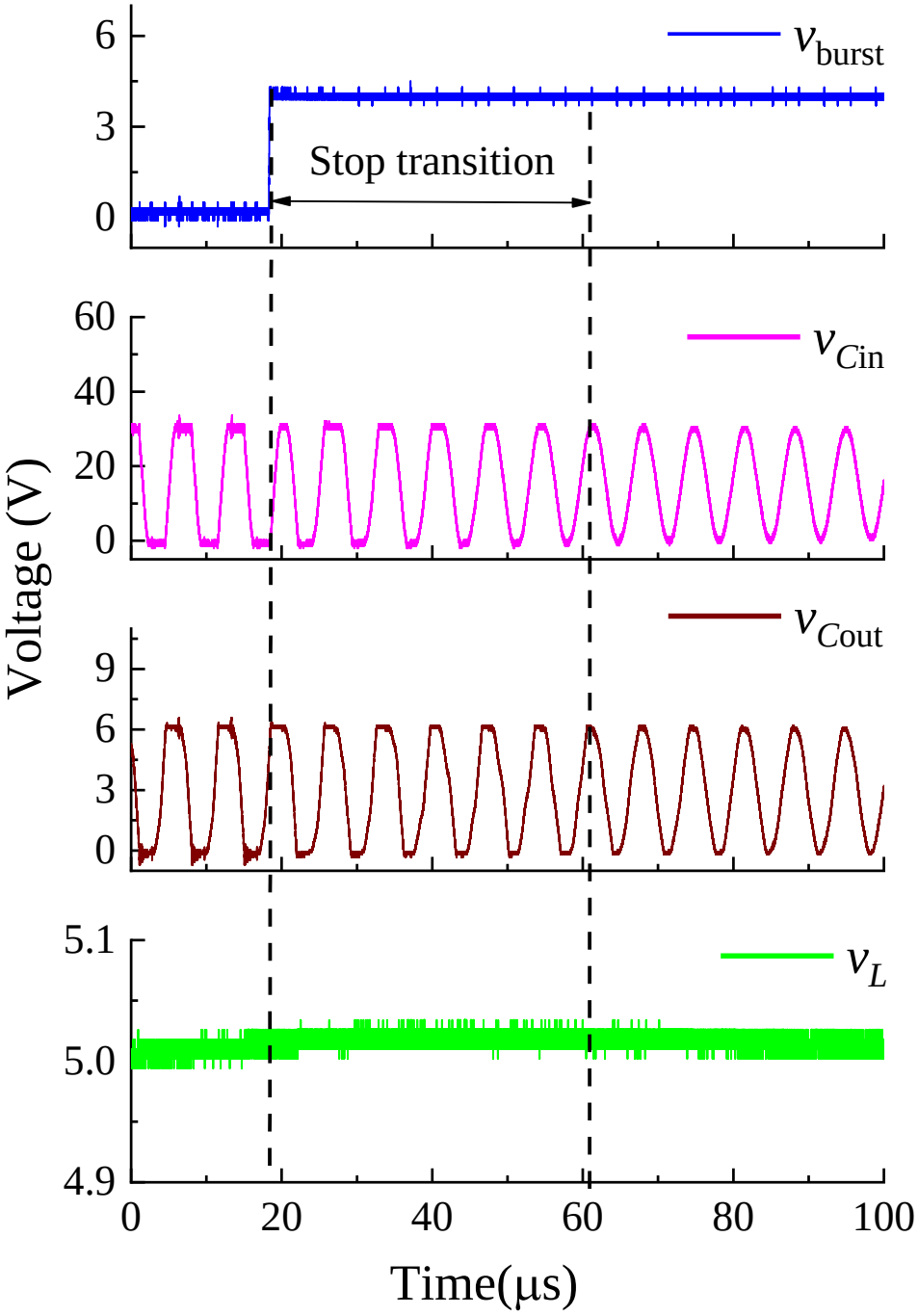
The start-up and stop transitions due to mechanical vibration of the PT are shown in Fig. 5.7(a) and (b). The start-up transition is measured between the burst signal switching instant and v_{Cin} reaches steady state. The stop transition is measured between the instant that the PT stops providing energy to the load and v_{burst} switching instant. The hysteresis window is implemented in such a way as to provide a 3kHz burst signal with 0.5 duty cycle. As can be seen, the transition time for PT requires 36us to start and 61us to stop, these correspond to 5.1 and 8.7 PT (i.e. high frequency) resonant periods, respectively.

In Fig. 5.7(a), a time delay is introduced between beginning of start-up transition and PT initialisation (i.e. a complete switching period for v_{Cin} to reach V_{dc} from 0V), this is because the burst enable signal of v_{burst} occurs during the deadtime, and v_{Cin} is not fully charged to V_{dc} before MOSFET turned on due to insufficient deadtime. Therefore, PT requires a further cycle to start charging v_{Cin} from 0V at the beginning of $\pi/2$ deadtime. The PT initialisation time shown in Fig. 5.7(a) is five switching cycles, using CE3 with frequency divider. This indeed validates the simulation results for the same approach shown in Fig. 4.12(b) of Chapter IV.

In Fig. 5.7(b), the PT output capacitance voltage, v_{Cout}, is not clamped by the rectifier after the stop transition, and secondary voltage is not high enough to turn on the rectifier and therefore it is no longer providing energy to the load.


Start-up
transition
v_{burst}
PT
initialisation
v_{Cin}
v_{Cout}
v_L
6
3
0
60
40
20
0
9
6
3
0
5.1
5.0
4.9
0
20
40
60
80
100
Time (μs)

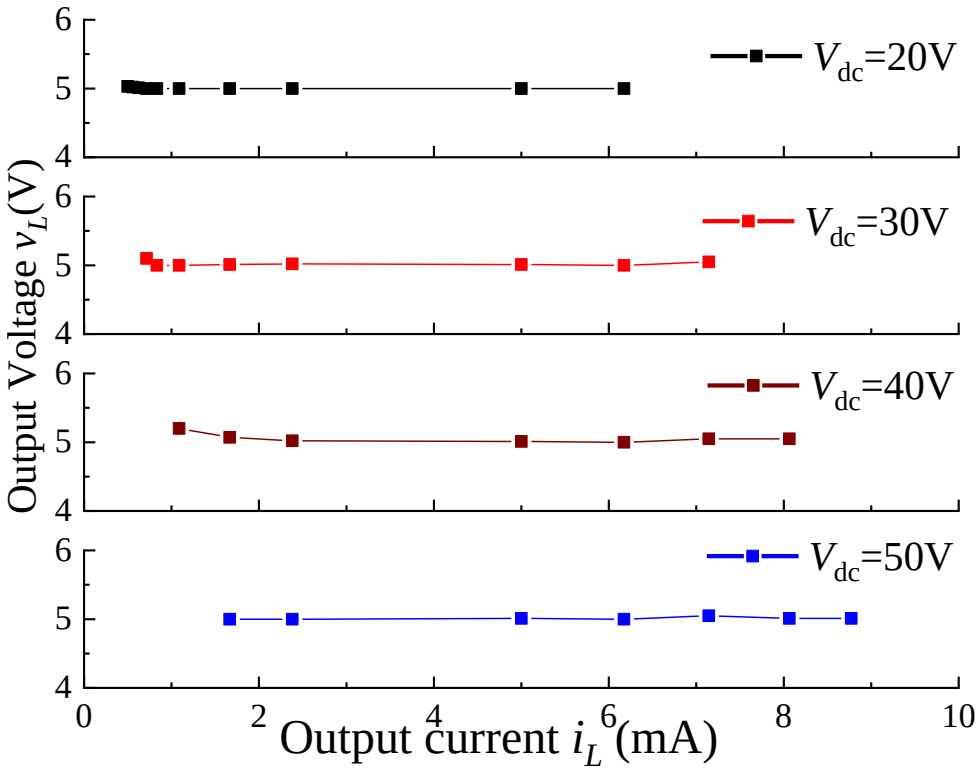
(a)



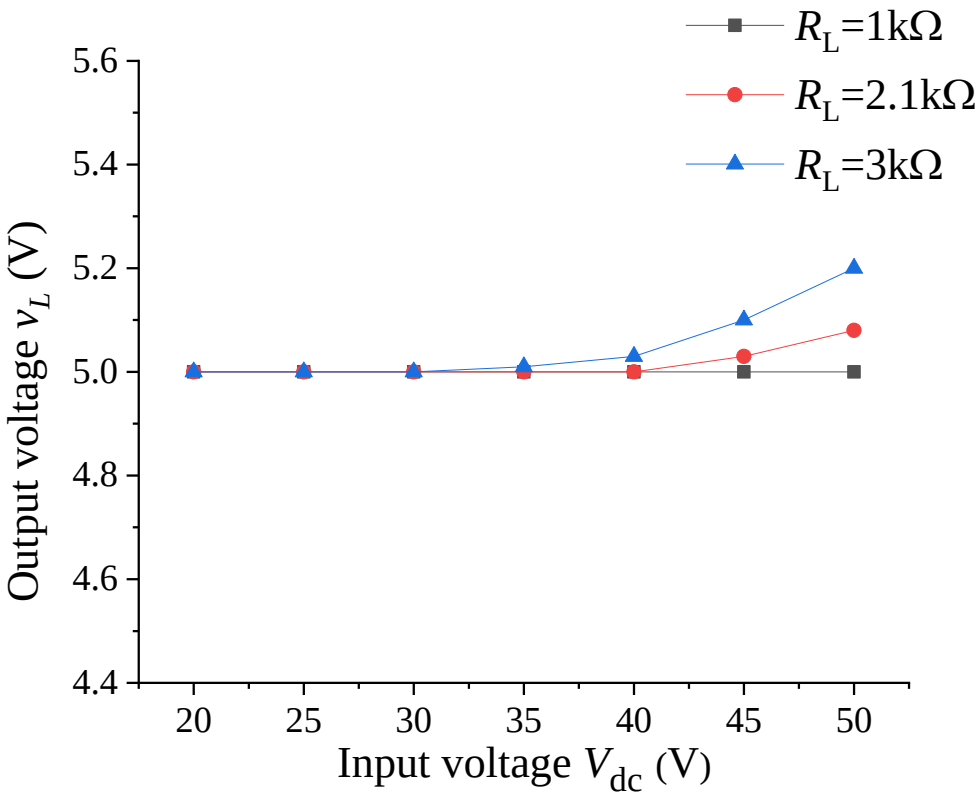
(b)

Fig. 5.7: Experimental measurements of the PT (a) start-up and (b) stop transitions (f_{burst}=1kHz, 0.5 duty cycle).

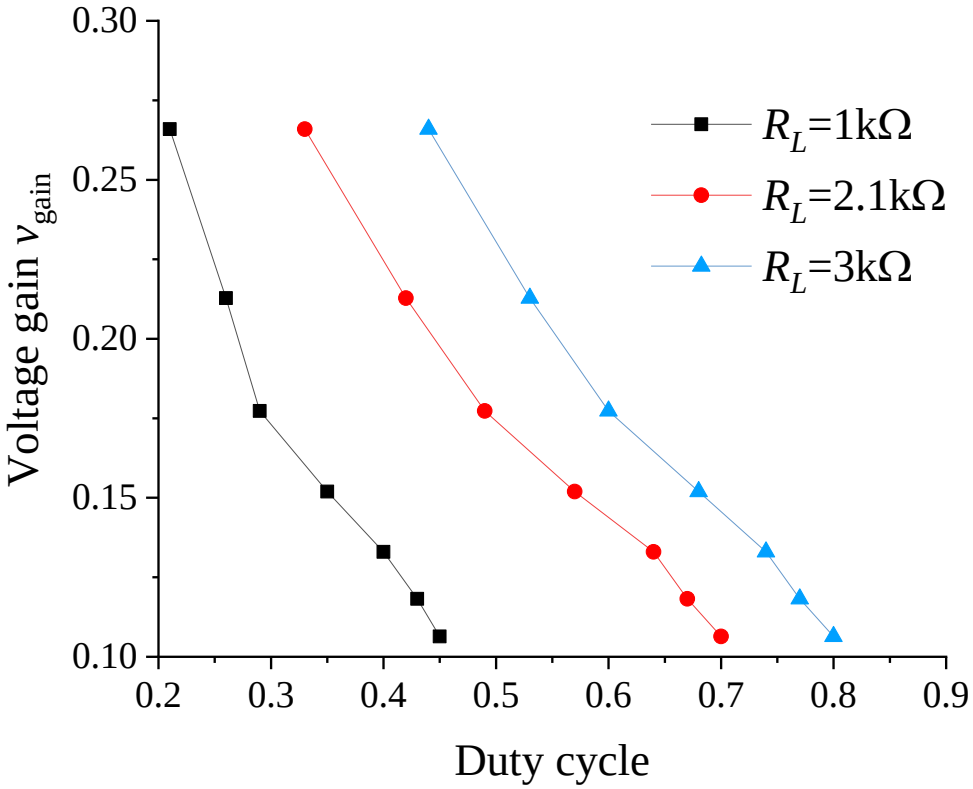
5.4.4 Voltage regulation characteristics



(a)



(b)



(c)

Fig. 5.8: Output characteristics of (a) load regulation, (b) line regulation and (c) regulation limit regarding duty cycle.

To further demonstrate the output voltage regulation ability of the proposed PT-based converter, the hysteresis window (Δv_L) is dynamically adjusted with variable resistors regarding load and input voltage variation, to maintain a constant output voltage. The output characteristics regarding load, line regulation and regulation limit are shown in Fig. 5.8(a), (b) and (c), respectively.

Fig. 5.8(a) shows different input voltages for load regulation, it can be seen that the output voltage remains at 5V from 1.7mA to 6.3mA load current for all cases. The regulation range varies from 20V to 50V input since the 5V output cannot be regulated at either light and heavy load conditions. The line regulation characteristics is shown in Fig. 5.8(b). As can be seen, at R_L=1kΩ, the output

voltage is able to maintain at 5V from 20V to 50V input. The input voltage regulation range is reduced for R_L=2.1kΩ and R_L=3kΩ, indicating 20V-40V and 20V-30V, respectively. In Fig. 5.8(c), a burst frequency of 1kHz is used with different duty cycles to regulate output at 5V. The output voltage is normalised and given as voltage gain $v_{gain}=v_L/\underline{N}V_{dc}$. When input voltage increases, duty cycle should be increased accordingly to maintain a constant output voltage, since MOSFETs conduction period needs be reduced in order to reduce the output voltage to meet the required level.

Although the voltage regulation has been achieved for an inductorless PT-based converter and ZVS is satisfied when v_{Cin} reaches steady-state during burst-on period, the regulation range of the proposed converter is limited and circuit behaviour is not predictable in terms of circuit parameters (i.e. deadtime and load). Therefore, a modelling technique is proposed in next chapter to predict the circuit behaviour, ensuring simultaneous ZVS and voltage regulation, and a new control method by varying deadtime is described to obtain a large regulation range.

5.5 Chapter conclusions

Output voltage regulation and ZVS operation of a PT-based inductorless half-bridge converter is presented in this Chapter. A ring dot radial mode PT is used verify the proposed control circuit at matched load condition. A secondary-side resonant current estimation using voltage differentiator has been demonstrated to accurately reconstruct an unmeasurable signal and ZVS is achieved by using a PLL to lock onto this signal. The fast lock-on behaviour of the PLL enables a quick start-up of the PT to reach ZVS. A 5V output regulation has been accomplished by burst mode control through a hysteresis window. The output voltage is restricted by the window size and the gate signals are modulated by the corresponding burst signal via PLL controller and logic circuit. Therefore, the MOSFETs are periodically switched on/off to satisfy regulation requirements.

Output regulation characteristics in terms of regulation limit, load and line regulation are demonstrated.

5.6 References

[5.1] Y. C. Wang, J. J. He, Y. P. Liu, Y. P. Wu, C. K. Lee, and Y. T. Huang, "Theory and experiment of high voltage step-up ratio disk type piezoelectric transformer for LCD-TV," in *Proc. IEEE Int. Conf. Mech*, Taiwan, 2005, pp. 284-287.

[5.2] M. S. Roedgaard, M. Weirich, and M. A. E. Andersen, "Forward conduction mode controlled piezoelectric transformer-based PFC LED drive," *IEEE Trans. Power Electron.,* vol. 28, no. 10, pp. 4841-4849, 2013.

[5.3] M. P. Foster, J. N. Davidson, E. L. Horsley, and D. A. Stone, "Critical Design Criterion for Achieving Zero Voltage Switching in Inductorless Half-Bridge-Driven Piezoelectric-Transformer-Based Power Supplies," *IEEE Trans. Power Electron.,* vol. 31, no. 7, pp. 5057–5066, 2016.

Chapter VI

Cyclic modelling of H-bridge PT-based converter

This Chapter describes a novel methodology for predicting the ability of an inductorless piezoelectric transformer (PT)-based H-bridge converter to simultaneously achieve zero-voltage switching and output regulation. A new idea for output voltage regulation by controlling deadtime interval is presented. A non-linear state-variable model is derived first and decomposed into a piecewise linear model based on the circuit operating mode. Then, cyclic-mode analysis is employed to model the periodically switching network to determine the steady-state (cyclic-mode) values of the circuit for a given operation condition. Subsequently, the proposed model is used to demonstrate the operation in ZVS region and it provides estimates for the required deadtime period, load and operating frequency along the ZVS boundary. The output voltage regulation profile is then indicated by the model and regions where voltage regulation can be continuously achieved while still obtaining ZVS are demonstrated. Both simulation and experimental results are presented to verify the model. Finally, the output regulation ability is described with respect to deadtime and load condition at different switching frequencies, and practical design consideration regarding PT design, ZVS and voltage regulation are demonstrated.

6.1 Introduction

Chapter V presented an approach to regulate the output voltage of a PT-based converter by burst-mode control. Voltage regulation also can be achieved using other approaches such as deadtime control [6.1]. For traditional resonant converters, the deadtime period is small proportion to the switching period due to the large resonant current circulating and so the amplitude of the resonant current

can be assumed to be constant to simplify the circuit analysis [6.2]. However, for a PT-based converter, this assumption is not valid due to limited availability of resonant current and the large input capacitance of the PT. Therefore, the deadtime period consumes a large proportion of the switching period – often the switches are only on for half the resonant period. Thus, the assumption of constant resonant current during the deadtime interval cannot be applied to a PT-based converter.

Several authors have developed analytical models to indicate ZVS characteristics in order to maximize the efficiency of a PT-based converter at different operating conditions. In [6.3], the ZVS behaviour of an inductorless PT-based converter is analysed. However, ZVS ability is conservatively estimated due assumptions regarding the shape of the PT input capacitance voltage waveform and its phase relationship to the resonant current. In addition, the application of this analysis is limited since it is not optimal to vary the deadtime period alone because a control parameter since ZVS is also dependent on switching frequency and load condition.

In [6.4], the ZVS ability is represented as a function of input-to-output capacitance ratio by parametric sweep of the equivalent circuit parameters. Although good correlation is indicated by this approach, the ZVS predictions are less accurate as the parameter sweep is dependent on a curve fit obtained from a specific PT characterization. In [6.5], a state-variable model is employed to describe the circuit operating conditions of a PT-based converter. A fundamental-mode approximation (FMA) is used to describe the nonlinear behaviour of the bridge rectifier and load. A numerical method is employed to indicate the ZVS region as a function of duty cycle and switching frequency. Although these methods are presented with improved accuracy, it is difficult to implement the methods in practice due to the lack of both normalised parameter analysis and a design example.

In [6.6], a piecewise linear state-variable model is presented with improved accuracy for predicting ZVS. The ZVS ability of an inductorless PT-based converter is assessed through the cyclic-mode analysis. The ZVS profile is generated as a function of deadtime, switching frequency and load. The ZVS boundary has been highlighted for different PTs and the appropriateness of PTs for different applications are assessed. In [6.7], an analytical model of the inductorless half-bridge driven PT is derived using a describing function approach. The design criteria to guarantee ZVS is explored and the difficulty associated with multiple parameter control for ZVS operation is highlighted.

However, all of the methods previously described exhibits one or more of following problems: 1) they do not adequately describe how to obtain continuously achievable ZVS, especially if ZVS region is discontinuous at the matched load condition. 2) simultaneous voltage regulation and ZVS is hard to achieve and is still a topic of open research.

In this Chapter, a novel inductorless H-bridge-driven PT-based power supply is proposed that can simultaneously achieve ZVS and output regulation through the introduction of a zero-voltage level during the deadtime interval. A piecewise linear state-variable model is presented, which provides predictions of switching waveforms from which cyclic mode analysis is used to provide predictions of ZVS profile, ZVS boundary and output voltage characteristics. The output regulation with continuously achievable ZVS is obtained by controlling the duration of the zero-voltage level during the deadtime interval via a H-bridge topology. Both simulation and experimental results are provided to validate the proposed model.

6.2 Operation of inductorless H-bridge PT-based resonant converter

When a PT operates near resonance, it generally exhibits a high quality factor and its electrical behaviour can be modelled by the Mason equivalent circuit, as shown by the dashed box in Fig. 6.1. Sufficient dead-time intervals are applied between the rising gate signals of each MOSFET to prevent shoot-through and to achieve ZVS by allowing sufficient time for the resonant current i_{L1} to charge C_{in} from $-V_{\text{dc}}$ to $+V_{\text{dc}}$ (and vice versa). Output voltage regulation is afforded by adjusting the duration of the zero voltage interval labelled as Δt_2 in Fig. 6.2.

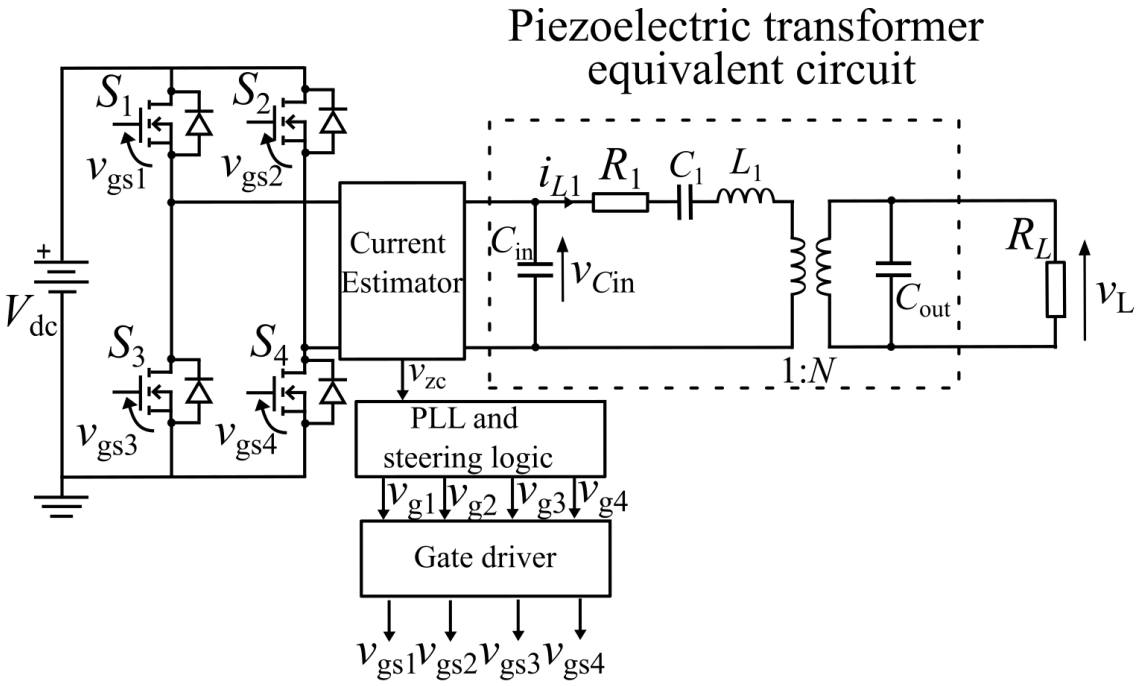


Fig. 6.1: Inductorless driven PT-based H-bridge converter

Fig. 6.2 shows the steady-state switching waveforms for the converter shown in Fig. 6.1 when operating under the ZVS condition, where v_{Cin} and i_{L1} are the input capacitor voltage and resonant current, respectively. The resonant current is assumed to be sinusoidal due to the high Q-factor of the PT and its magnitude is shown as I_{L1}. Signals v_{g1}, v_{g2}, v_{g3}, v_{g4} correspond to the reference gate signals and

are shown emerging from the PLL and steering logic block that will be described in more detail Chapter VII, while v_{gs1}, v_{gs2}, v_{gs3}, v_{gs4} are the actual (measured) gate-to-source signals of H-bridge from the gate driver. For the purpose of simplifying the analysis for ZVS operation it is assumed that the circuit exactly achieves ZVS and so can be described entirely by the mode sequence M1→M2→M3→M4 due to the half-cycle symmetry exhibited by the circuit operation. The first mode (M1) starts at time $t=t_0$ and the transition from mode i to mode i+1 occurs at time t_i. For example, considering mode 1 (M1), it starts at $t=t_0$ and ends at $t=t_1$. The transition times are labelled above the v_{Cin} waveform in Fig. 6.2 The mode time durations, Δt_1, Δt_2, Δt_3 and Δt_4 (where $\Delta t_i = t_i - t_{i-1}$) refer to the deadtime during M1; the conduction time of S_3 & S_4 during M2 when v_{Cin}=0; the deadtime during M3; and the conduction time of S_1 & S_4 during M4 to maintain V_{dc} (or S_2 & S_3 conduction period in M4 to maintain $-V_{dc}$ for the second half-cycle), respectively. As can be seen, ZVS is achievable if $v_{Cin}(t_3) \geq V_{dc}$.

During a half-cycle period, the H-bridge PT-based resonant converter shown Fig. 6.1 exhibits one of the following four modes of operation, depending on the conduction status of the switches.

M1 - $t \in [t_0, t_1]$: Prior to time t_0, MOSFETs S_2 & S_3 are on so $v_{Cin}(t_0)=-V_{dc}$. At $t=t_0$, all MOSFETs are turned off and so the resonant current, i_{L1}, circulates through C_{in}, thus v_{Cin} is being charged from -V_{dc} and heading in a positive direction towards 0V.

M2 - $t \in [t_1, t_2]$: At $t=t_1$, S_3 & S_4 are turned on to set v_{Cin}=0 and so i_{L1} flows through S_3 & S_4.

M3 - $t \in [t_2, t_3]$: At $t=t_2$ all MOSFETs are turned off and i_{L1} once again circulates through C_{in} charging it in a positive direction towards +V_{dc}.

M4 - $t \in [t_3, t_4]$: At $t=t_3$, $v_{Cin}(t_3)=V_{dc}$ and so S_1 & S_4 are turned on thereby achieving zero voltage switching (ZVS). Zero derivative voltage switching

(ZDVS) can be achieved if v_{Cin} hits V_{dc} at the start of this mode, thus $dv_{Cin}(t_3)/dt \propto i_{L1}(t_3) = 0$.

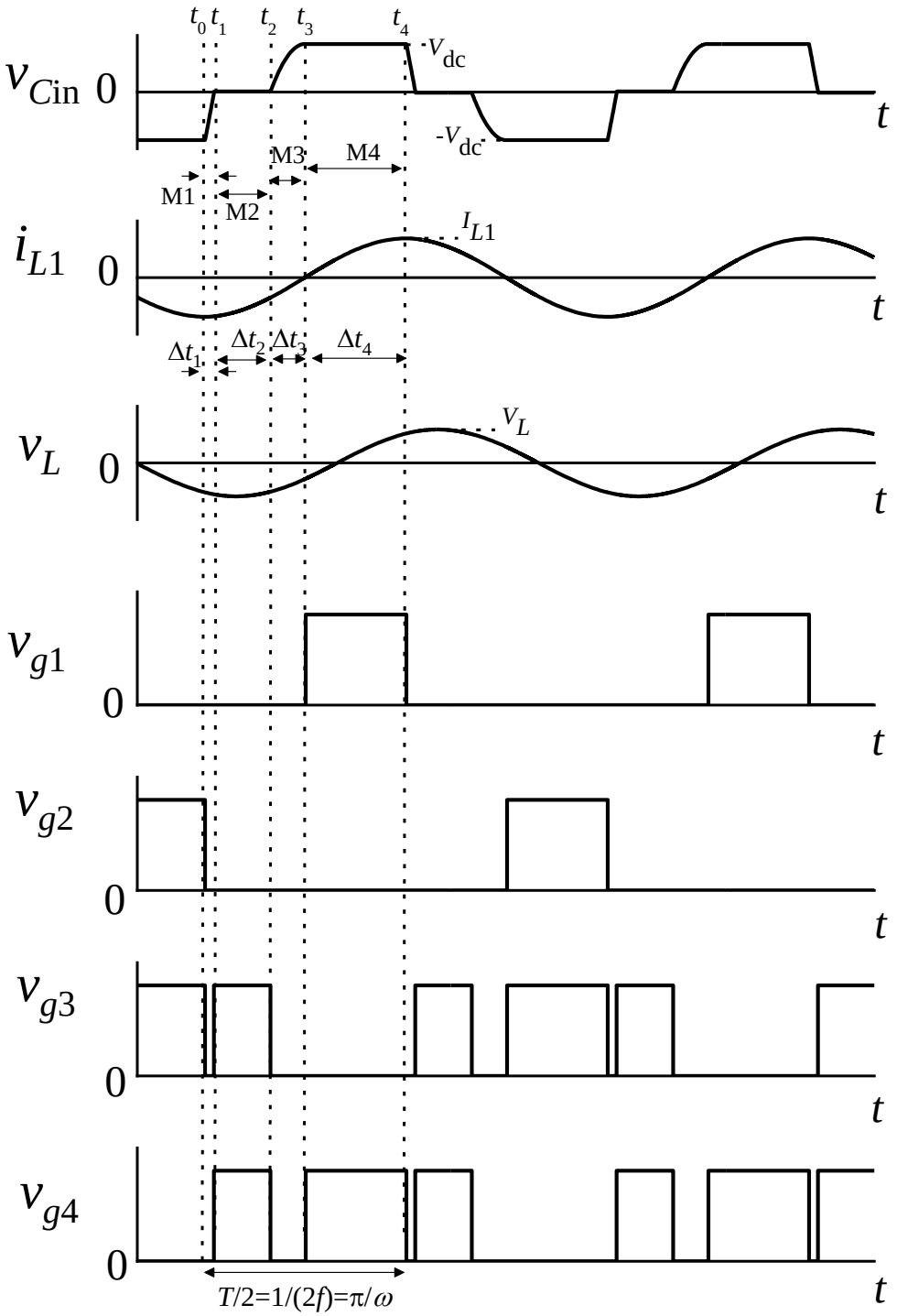


Fig. 6.2: Switching waveforms of the inductorless H-bridge PT-based converter.

Since the resonant current is internal to the PT and cannot be measured directly, a PLL controller with the current estimation technique presented in Chapter III and IV are employed to achieve synchronisation of the gate signals to the resonant current. The resonant current is estimated and the zero crossings are detected to giving signal v_{zc} as shown in Fig. 6.1. The deadtime intervals and the in-phase gate drive signals are generated via a PLL and the steering logic.

To ensure ZVS operation for an inductorless PT-based configuration, the critical criterion described in [6.7] is adapted. For a half-bridge it was shown that ZVS can be achieved for all load conditions if the input-to-output capacitance ratio meets $C_{in}/N^2C_{out} \leq 2/\pi$ with $\pi/2$ deadtime. When ZVS criteria is met, the resonant current i_{L1} should be in-phase with the gate signals, thereby guaranteeing the deadtime (or M1) begins at the negative peak of i_{L1} since this is where the quickest charging of C_{in} happens. This ensures the PT input voltage v_{Cin} is maximised by the end of the deadtime period. In this Chapter, the output voltage is regulated by controlling Δt_2, and Δt_3 is controlled to ensure the total deadtime ($\Delta t_1 + \Delta t_2 + \Delta t_3$) is $1/(4f)$.

Since the operation of the circuit is divided into four modes (see the input capacitor voltage v_{Cin} in Fig. 6.2), then four piecewise state-variable models are required to describe the evolution of the state trajectories during a half-cycle period. Adopting the technique described in [6.6] allows the system initial condition to be obtained by the cyclic-mode analysis, from which the state-variable values at any time during a cyclic-mode can be determined.

6.3 State-variable model analysis

6.3.1 Model derivation

In this section a non-linear state-variable model is derived from the differential equations for the inductor current and capacitor voltages. This model is then

decomposed into a piecewise linear model based on the operating modes previously described.

The inductor current is found from

$$i_{L1}^{\bullet} = \frac{v_{L1}}{L_1} = \frac{v_{C\text{in}} - i_{L1}R_1 - v_{C1}}{L_1} - \frac{v_{C\text{out}}}{NL_1} \tag{6.1}$$

The primary side capacitor voltage during M1-M4 is given by

$$v_{C1}^{\bullet} = \frac{i_{L1}}{C_1} \tag{6.2}$$

$$v_{C\text{in}}^{\bullet} = \begin{cases} -\dfrac{i_{L1}}{C_{\text{in}}} & t_0 \le t < t_1 \\ 0 & t_1 \le t < t_2 \\ -\dfrac{i_{L1}}{C_{\text{in}}} & t_2 \le t < t_3 \\ 0 & t_3 \le t < t_4 \end{cases} \tag{6.3}$$

With the initial conditions: $v_{C\text{in}}(t_0)=-V_{\text{dc}}$, $v_{C\text{in}}(t_1)=0$, $v_{C\text{in}}(t_2)=0$, $v_{C\text{in}}(t_3)=V_{\text{dc}}$ and it is assumed that the circuit is operated in an appropriate manner to guarantee these conditions can be achieved.

The PT output capacitor voltage $v_{C\text{out}}$ is given by

$$v_{C\text{out}}^{\bullet} = \frac{i_{L1}}{NC_{\text{out}}} - \frac{v_{C\text{out}}}{R_L C_{\text{out}}} \tag{6.4}$$

Combining equations (6.1)-(6.4) provides the complete state-variable model and coupling equations

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{v}_{C1} \\ \dot{v}_{C\text{in}} \\ \dot{v}_{C\text{out}} \end{bmatrix} = \begin{bmatrix} -\frac{R_1}{L_1} & -\frac{1}{L_1} & h_2(t)\frac{1}{L_1} & -\frac{1}{NL_1} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ -h_2(t)\frac{1}{C_{\text{in}}} & 0 & 0 & 0 \\ \frac{1}{NC_{\text{out}}} & 0 & 0 & -\frac{1}{R_L C_{\text{out}}} \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \\ v_{C\text{in}} \\ v_{C\text{out}} \end{bmatrix} + \begin{bmatrix} h_1(t)\frac{V_{\text{dc}}}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{6.5}$$

where $h_1(t)$ and $h_2(t)$ are switching functions defined as

$$h_1(t) = \begin{cases} 0 & t_0 \le t < t_1 \\ 0 & t_1 \le t < t_2 \\ 0 & t_2 \le t < t_3 \\ 1 & t_3 \le t < t_4 \end{cases}, \qquad h_2(t) = \begin{cases} 1 & t_0 \le t < t_1 \\ 0 & t_1 \le t < t_2 \\ 1 & t_2 \le t < t_3 \\ 0 & t_3 \le t < t_4 \end{cases} \tag{6.6}$$

The load voltage v_L=v_{Cout}.

6.3.2 State-variable analysis of operating modes

For M1, the state-variable model is obtained from equation (6.4) and (6.6).

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{v}_{C1} \\ \dot{v}_{C\text{in}} \\ \dot{v}_{C\text{out}} \end{bmatrix} = \begin{bmatrix} -\frac{R_1}{L_1} & -\frac{1}{L_1} & \frac{1}{L_1} & -\frac{1}{NL_1} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ -\frac{1}{C_{\text{in}}} & 0 & 0 & 0 \\ \frac{1}{NC_{\text{out}}} & 0 & 0 & -\frac{1}{R_L C_{\text{out}}} \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \\ v_{C\text{in}} \\ v_{C\text{out}} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$
$$= \boldsymbol{A_1} \begin{bmatrix} i_{L1} \\ v_{C1} \\ v_{C\text{in}} \\ v_{C\text{out}} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \boldsymbol{A_1} \begin{bmatrix} i_{L1} \\ v_{C1} \\ v_{C\text{in}} \\ v_{C\text{out}} \end{bmatrix} + \boldsymbol{B_1} \tag{6.7}$$

Equation (6.7) can be represented as $\dot{x} = \boldsymbol{A_1}x + \boldsymbol{B_1}$ where $x = [i_{L1} \quad v_{C1} \quad v_{C\text{in}} \quad v_{C\text{out}}]^T$

In M2, $v_{C\text{in}}$ is maintained at zero such that $\dot{v_{C\text{in}}} = 0$. Hence, M2 can be described as

$$\begin{bmatrix} \dot{i_{L1}} \\ \dot{v_{C1}} \\ \dot{v_{C\text{in}}} \\ \dot{v_{C\text{out}}} \end{bmatrix} = \begin{bmatrix} -\frac{R_1}{L_1} & -\frac{1}{L_1} & 0 & -\frac{1}{NL_1} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{NC_{\text{out}}} & 0 & 0 & -\frac{1}{R_L C_{\text{out}}} \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \\ v_{C\text{in}} \\ v_{C\text{out}} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$
$$= \boldsymbol{A_2} \begin{bmatrix} i_{L1} \\ v_{C1} \\ v_{C\text{in}} \\ v_{C\text{out}} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \boldsymbol{A_2}x + \boldsymbol{B_2} \tag{6.8}$$

Due to symmetric behaviour of the system, the model matrices for M3 are equivalent to M1, i.e. $\boldsymbol{A_3}$=$\boldsymbol{A_1}$, $\boldsymbol{B_3}$=$\boldsymbol{B_1}$.

For M4, $v_{C\text{in}}$ is maintained at V_{dc} hence $\dot{v_{C\text{in}}} = 0$.

$$\begin{bmatrix} \dot{i_{L1}} \\ \dot{v_{C1}} \\ \dot{v_{C\text{in}}} \\ \dot{v_{C\text{out}}} \end{bmatrix} = \begin{bmatrix} -\frac{R_1}{L_1} & -\frac{1}{L_1} & 0 & -\frac{1}{NL_1} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{NC_{\text{out}}} & 0 & 0 & -\frac{1}{R_L C_{\text{out}}} \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \\ v_{C\text{in}} \\ v_{C\text{out}} \end{bmatrix} + \begin{bmatrix} \frac{V_{\text{dc}}}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$= \boldsymbol{A_4}\begin{bmatrix} i_{L1} \\ v_{C1} \\ v_{C\text{in}} \\ v_{C\text{out}} \end{bmatrix} + \begin{bmatrix} \frac{V_{\text{dc}}}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} = \boldsymbol{A_4}x + \boldsymbol{B_4} \tag{6.9}$$

Finally, from the state-variable descriptions of each mode, and the time interval of each mode, the converter operation in a cyclic mode can be determined.

6.4 Modelling cyclic mode behaviour

The proposed cyclic modelling is described as an extended Floquet-based method [6.8], by determining steady-state values of state-variables. It is an alternative to integration-based [6.7] methods and the state-space averaging technique [6.9] often used to model the periodically switching networks.

During a single switching cycle in steady-state, the circuit operation is decomposed in to several operating modes (M1→M4, from t=t_0 to t=t_4), depending on the switch state, as shown by the waveforms given in Fig. 6.2. Therefore, the system in each mode can be described by the piecewise linear equation

$$\dot{x(t)} = \boldsymbol{A_i}x(t) + \boldsymbol{B_i} \tag{6.10}$$

Where $x(t)$ is the state vector, i is the mode index, A_i and B_i are the dynamical matrix and the input vector, respectively. Therefore, for $t_{i\text{-}1} \leq t \leq t_i$, the evolution of the state vector is given as

$$x(t) = e^{\boldsymbol{A_i}(t-t_{i-1})}x(t_{i-1}) + \int_{t_{i-1}}^{t} e^{\boldsymbol{A_i}(t-\tau)}\boldsymbol{B_i}d\tau \tag{6.11}$$

Assuming the input voltage is constant for the duration of a mode, the state vector $x(t)$ at $t=t_i$ can be solved from the state vector value at t_{i-1} using,

$$\begin{aligned} x(t_i) &= e^{\boldsymbol{A_i}(t_i - t_{i-1})} x(t_{i-1}) + \int_{t_{i-1}}^{t_i} e^{\boldsymbol{A_i}(t-\tau)} \boldsymbol{B_i} d\tau \\ &= e^{\boldsymbol{A_i} d_i T} x(t_{i-1}) + \boldsymbol{A_i^{-1}} (e^{\boldsymbol{A_i} d_i T} - I) \boldsymbol{B_i} \\ &= \Phi_{\boldsymbol{i}} x(t_{i-1}) + \boldsymbol{\Gamma_i} \end{aligned} \tag{6.12}$$

where I is the identity matrix, $\boldsymbol{\Phi_i} = \boldsymbol{\Phi}(t_i, t_{i-1}) = e^{\boldsymbol{A_i} d_i T}$, $\boldsymbol{\Gamma_i} = \boldsymbol{A_i^{-1}} (e^{\boldsymbol{A_i} d_i T} - I) \boldsymbol{B_i}$ and d_i is the duty cycle for the i^{th} mode.

Therefore, the complete cyclic-mode of the system can be determined from equation (2.8) once the initial circuit condition $x(t_0)$ has been found, which has the form

$$x(t_0) = [i_{L1}(t_0) \quad v_{C1}(t_0) \quad v_{C\text{in}}(t_0) \quad v_{C\text{out}}(t_0)]^T \tag{6.13}$$

The values of the state-variables at the end of M1 are found from

$$x(t_1) = \Phi_{\mathbf{1}} x(t_0) + \boldsymbol{\Gamma_1} \tag{6.14}$$

Similarly, at the end of mode 2, the state is given by

$$x(t_2) = \Phi_{\mathbf{2}} x(t_1^+) + \boldsymbol{\Gamma_2} \tag{6.15}$$

where $x(t_1^+)$ indicates the possible discontinuity in the state-variables at $t=t_2$ caused by turning-on of S_3 & S_4 to clamp $v_{C\text{in}} = 0\text{V}$,

$$x(t_1^+) = [i_{L1}(t_1) \quad v_{C1}(t_1) \quad 0 \quad v_{C\text{out}}(t_1)]^T \tag{6.16}$$

From equation (6.15) and (6.16), a new matrix *K* can be introduced to correct the values of the state variables at the switching instant and with an additional vector x_2 to represent the discontinuity in v_{Cin} due to MOSFETs switching. Therefore, equation (6.15) can be modified as

$$x(t_2) = \Phi_{\mathbf{2}}[\boldsymbol{K}x(t_1) + \boldsymbol{x_2}] + \boldsymbol{\Gamma_2} \tag{6.17}$$

$$\text{where} \quad \boldsymbol{K} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}, \ \boldsymbol{x_2} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{6.18}$$

In a similar manner, the solution of the state vector for M3 and M4 can be given by

$$x(t_3) = \Phi_{\mathbf{3}}\boldsymbol{K}\Phi_{\mathbf{2}}\boldsymbol{K}\Phi_{\mathbf{1}}x(t_0) + \Phi_{\mathbf{3}}\boldsymbol{K}\Phi_{\mathbf{2}}\boldsymbol{K}\boldsymbol{\Gamma_1} + \Phi_{\mathbf{3}}\boldsymbol{K}\boldsymbol{\Gamma_2} + \boldsymbol{\Gamma_3} \tag{6.19}$$

$$\begin{aligned} x(t_4) = \ & \Phi_4\boldsymbol{K}\Phi_{\mathbf{3}}\boldsymbol{K}\Phi_{\mathbf{2}}\boldsymbol{K}\Phi_{\mathbf{1}}x(t_0) + \ \Phi_{\mathbf{4}}\boldsymbol{K}\Phi_{\mathbf{3}}\boldsymbol{K}\Phi_{\mathbf{2}}\boldsymbol{K}\boldsymbol{\Gamma_1} \\ & + \Phi_{\mathbf{4}}\boldsymbol{K}\Phi_{\mathbf{3}}\boldsymbol{K}\boldsymbol{\Gamma_2} + \Phi_{\mathbf{4}}\boldsymbol{K}\boldsymbol{\Gamma_3} + \Phi_{\mathbf{4}}\boldsymbol{x_4} + \boldsymbol{\Gamma_4} \end{aligned} \tag{6.20}$$

$$\text{where } \boldsymbol{x_4} = \begin{bmatrix} 0 \\ 0 \\ V_{\text{dc}} \\ 0 \end{bmatrix} \tag{6.21}$$

By using the odd-symmetry behaviour of the converter during a half-cycle $x(t_4) = -x(t_0)$, the initial condition of the cyclic mode can be given by

$$x(t_0) = [-\boldsymbol{I} - \Phi_4\boldsymbol{K}\Phi_3\boldsymbol{K}\Phi_2\boldsymbol{K}\Phi_1]^{-1}[\,\Phi_4\boldsymbol{K}\Phi_3\boldsymbol{K}\Phi_2\boldsymbol{K}\boldsymbol{\Gamma_1} + \Phi_4\boldsymbol{K}\Phi_3\boldsymbol{K}\boldsymbol{\Gamma_2} + \Phi_4\boldsymbol{K}\boldsymbol{\Gamma_3} + \Phi_4\boldsymbol{x_4} + \boldsymbol{\Gamma_4}] \quad (6.22)$$

The value of PT input capacitor voltage v_{Cin} at $t=t_3$ in M3 can be found by substituting equation (6.22) into equation (6.19) to give

$$v_{Cin}(t_3) = [0\ \ 0\ \ 1\ \ 0][\Phi_3\boldsymbol{K}\Phi_2\boldsymbol{K}\Phi_1 x(t_0) + \Phi_3\boldsymbol{K}\Phi_2\boldsymbol{K}\boldsymbol{\Gamma_1} + \Phi_3\boldsymbol{K}\boldsymbol{\Gamma_2} + \boldsymbol{\Gamma_3}] \quad (6.23)$$

The deadtime value $\Delta t_1 = t_1 - t_0$ can be found from M1 in equation (6.14) when v_{Cin} is charged from $-V_{dc}$ to 0V, which is given by

$$v_{Cin}(t_1) = 0 = [0\ \ 0\ \ 1\ \ 0][\Phi_1 x(t_0) + \boldsymbol{\Gamma_1}] \quad (6.24)$$

The output voltage v_L is equal to the PT output capacitance voltage v_{Cout} therefore

$$v_L(t) = v_{Cout}(t) = [0\ \ 0\ \ 0\ \ 1]x(t) \quad (6.25)$$

In general, the ZVS condition is satisfied if the input capacitor voltage can be charged to (or above) the DC input voltage, that is $v_{Cin}(t_3) \geq V_{dc}$.

6.5 Model verification

6.5.1 Charge equivalence for ZVS

For a given PT, ZVS performance can be evaluated by comparing the value of $v_{Cin}(t_3)$ to V_{dc}. In general, ZVS can be achieved if v_{Cin} is fully charged to (or above) V_{dc} during M3, that is $v_{Cin}(t_3) \geq V_{dc}$. Fig. 6.3 shows the different waveforms shapes of PT input capacitance voltage under ZVS condition and how K_{ZVS} is evaluated. The dashed line is the proposed cyclic mode while solid line

corresponds to the practical condition when the body diode of the MOSFET conducts when v_{Cin} exceeds V_{dc}. The amount of charge for v_{Cin} can be found from the resonant current during this deadtime period, indicated by the blue shaded area in Fig. 6.3. Hence, the charge during MOSFET body diode condition period d_1 and the charge transferred during M3 when $v_{Cin}>0$ can be found by

$$Q_{d1} \approx \frac{d_1 h_1}{2} \tag{6.26}$$

$$Q_{d2} \approx \frac{d_2 h_2}{2} \tag{6.27}$$

where $d_2 = t_3 - t_2 = \Delta t_3$. Therefore, ZVS factor K_{ZVS} can be defined as

$$K_{\mathrm{ZVS}} = \frac{Q_{d2}}{C_{\mathrm{in}} V_{\mathrm{dc}}} \approx \frac{d_2 h_2}{2 C_{\mathrm{in}} V_{\mathrm{dc}}} = \frac{v_{C\mathrm{in}}\left(\theta = \frac{\pi}{2}\right)}{V_{\mathrm{dc}}} \tag{6.28}$$

where $C_{\mathrm{in}} V_{\mathrm{dc}}$ is the charge stored on C_{in} at V_{dc} and $v_{C\mathrm{in}}\left(\theta = \frac{\pi}{2}\right)$ is the extrapolated final value for v_{Cin} if the body diode of the MOSFET was not allowed to conduct for the condition when $v_{Cin}>V_{dc}$, shown as a dotted line in Fig. 6.3.

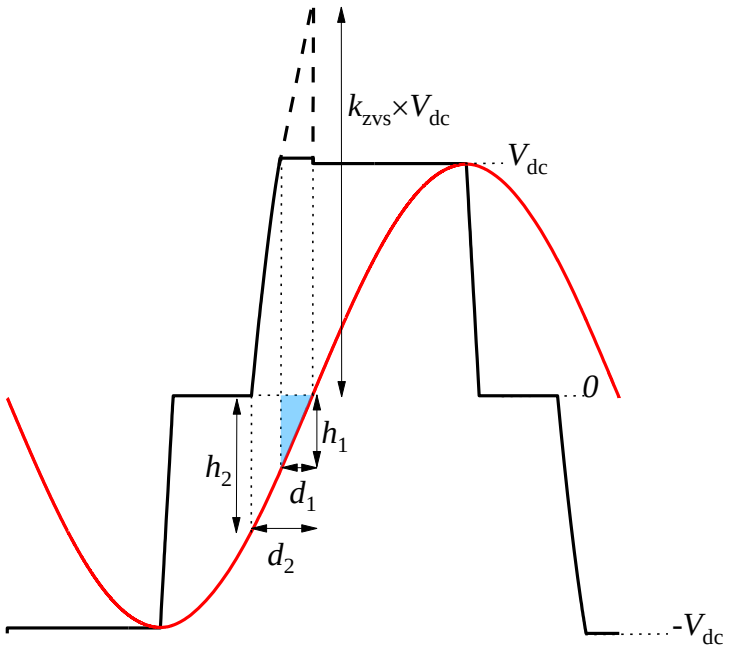


Fig. 6.3: Cyclic model and practical case of v_{Cin} under ZVS operation.

The circuit is simulated with the same PT parameters used in previous chapters (C_1=77.8pF, L_1=17.2mH, R_1=12.5Ω, Q=1190, C_{out}=1.14nF, C_{in}=0.43nF and N=0.94). For practical design considerations, the input capacitor value of the PT is modified by the H-bridge MOSFETs parasitic output capacitance (around 100pF), therefore, a value of 0.53nF was used for C_{in} to compensate for this additional capacitance.

In Fig. 6.4, the amount of charge during d_2 is evaluated for both cyclic mode and practical case and represented as K_{ZVS} using equation (6.28). As can be seen, the amount of charge for both cases are almost identical with nearly the same ZVS factor, thereby providing evidence that the proposed cyclic mode is able to accurately predict ZVS ability of a PT-based converter compared with practical case.

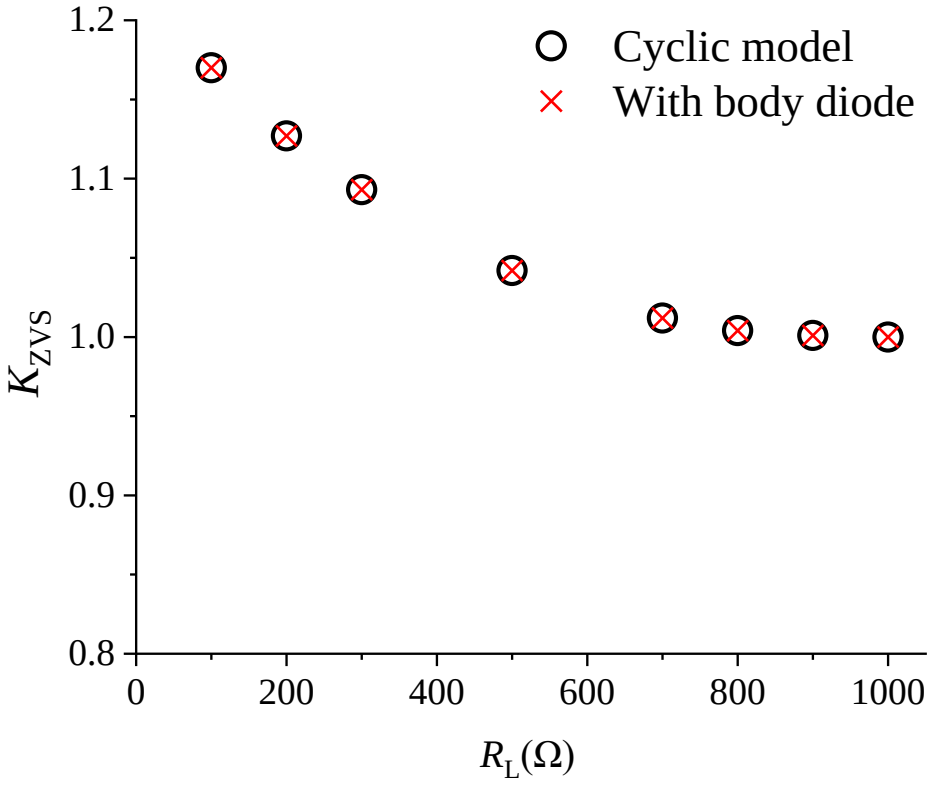
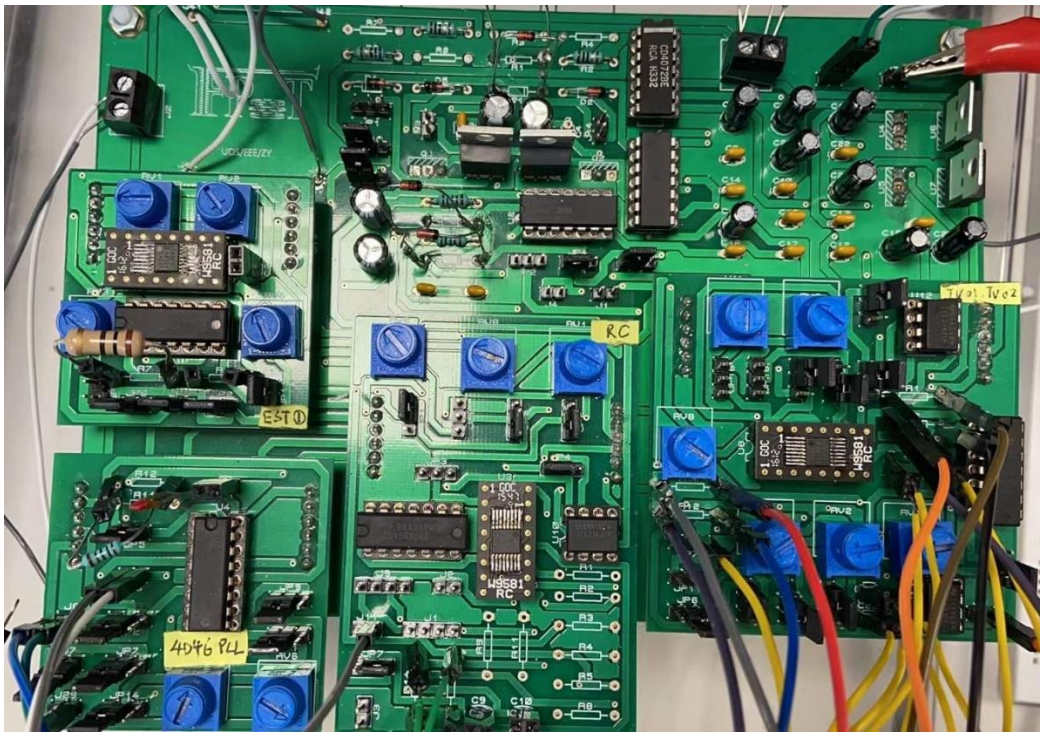
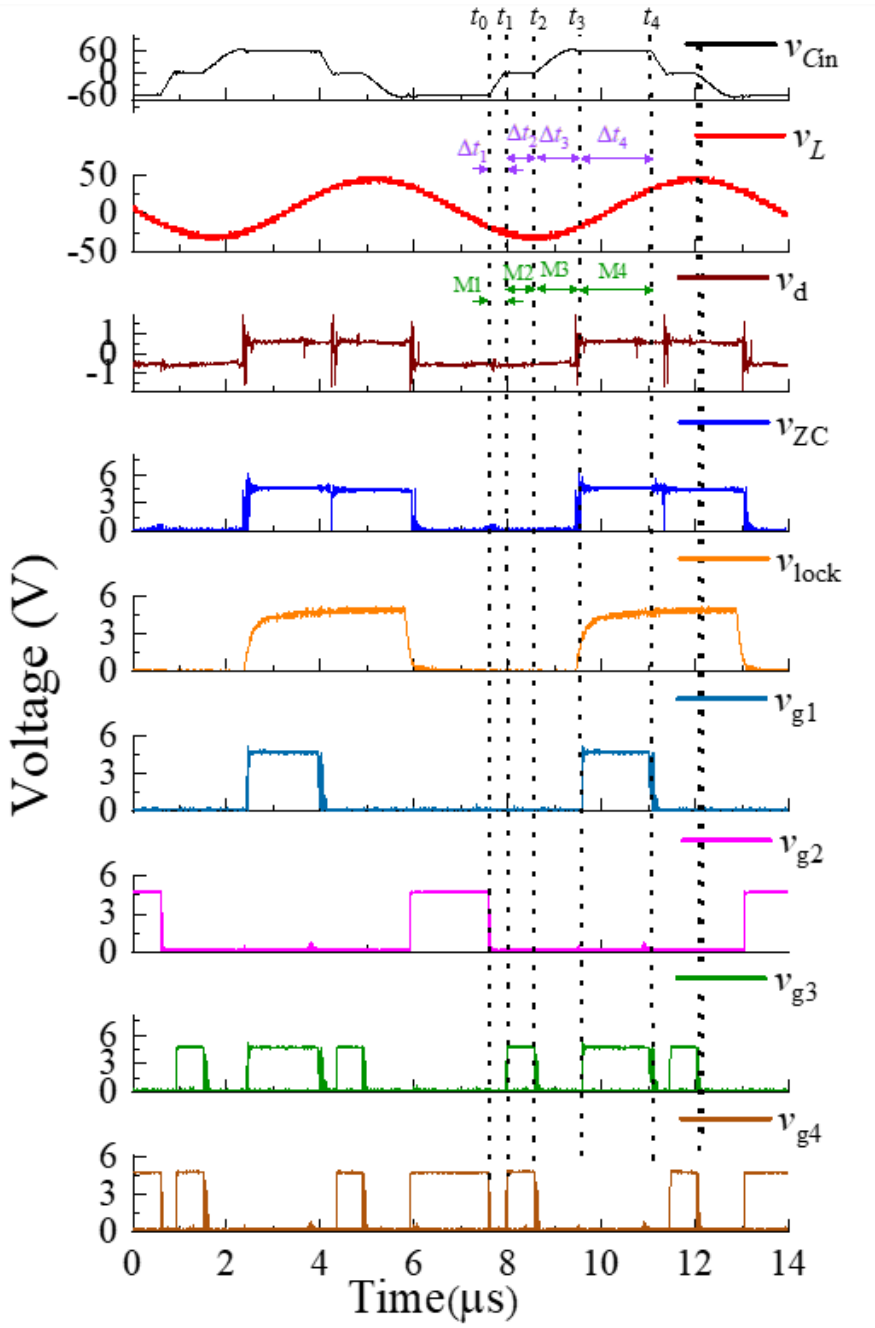


Fig. 6.4: ZVS factor comparison of cyclic model and practical case during d_2.

6.5.2 Experimental results



(a)



(b)

Fig. 6.5: (a) Prototype inductorless H-bridge PT-based converter and (b) experimental measurements.

To verify the proposed cyclic modelling and to predict the steady-state output voltage of a converter, a prototype converter based on the critical criteria [6.7] with the same ring-dot radial-mode PT (C_1=77.8pF, L_1=17.2mH, R_1=12.5Ω, Q=1190, C_{out}=1.14nF, C_{in}=0.43nF and N=0.94) presented in Chapter IV is

employed, as shown in Fig. 6.5(a). A matched load of 1kΩ is used at the PT output. The anti-parallel diode current estimator (CE2) with RC time delay PLL controller developed in Chapter IV is further extended to control the H-bridge converter since it offers asymmetrical deadtime control and each deadtime interval can be adjusted individually.

Fig. 6.5(b) shows the switching waveforms of the H-bridge converter. v_{d} is the estimated resonant current using CE2 and v_{ZC} is the PLL input reference signal. The time duration of Δt_1 from $-V_{\mathrm{dc}}$ to 0V in M1 can be found from equation (6.24) while the time period Δt_3 for M3 for just achieving ZVS can be found from equation (6.23) by setting $v_{\mathrm{Cin}}(t_3)$=V_{dc}. Subsequently, the time interval for M2 can be evaluated accordingly since the total deadtime period $\Delta t_1 + \Delta t_2 + \Delta t_3 = 1/(4f_s)$ [6.7]. The load voltage v_L is measured at a root-mean-square (RMS) value of 26.3V. The circuit operating conditions are summarized in Table 6.1.

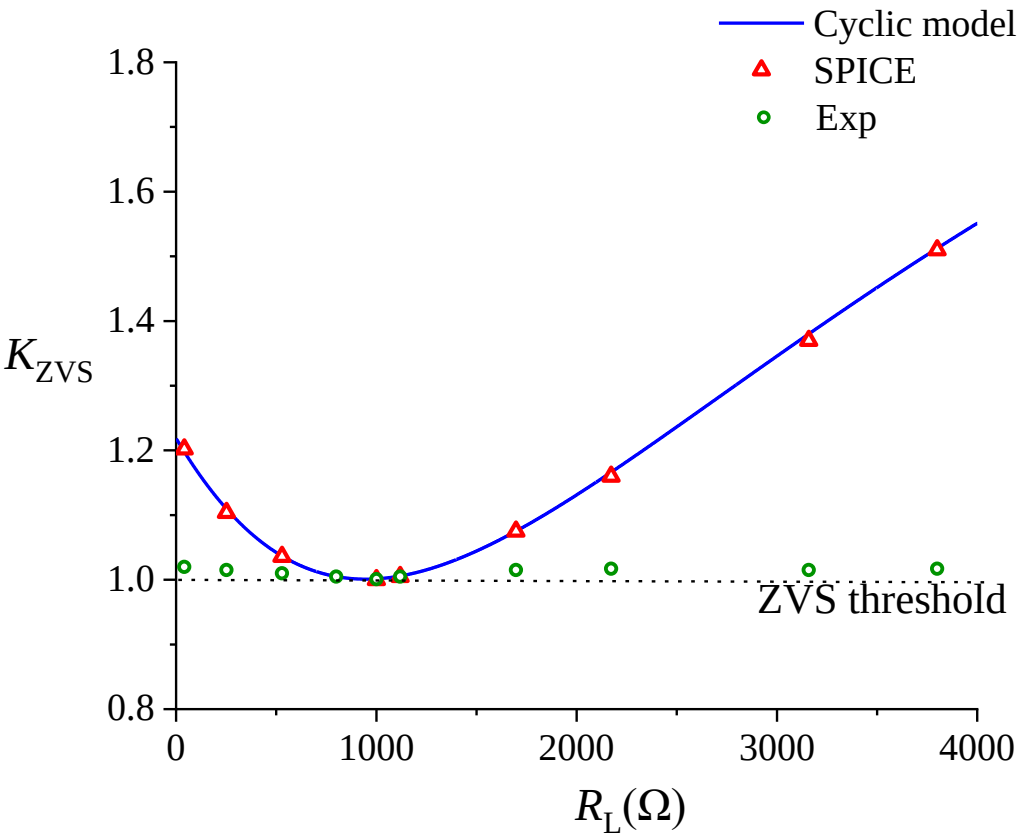
Table 6.1: Circuit operating conditions

V_{dc}	switching frequency, f_{s}	Δt_1	Δt_2	Δt_3	load	$v_{L,\mathrm{RMS}}$
60V	145.3kHz	0.36μs	0.46μs	0.9μs	1kΩ	26.3V

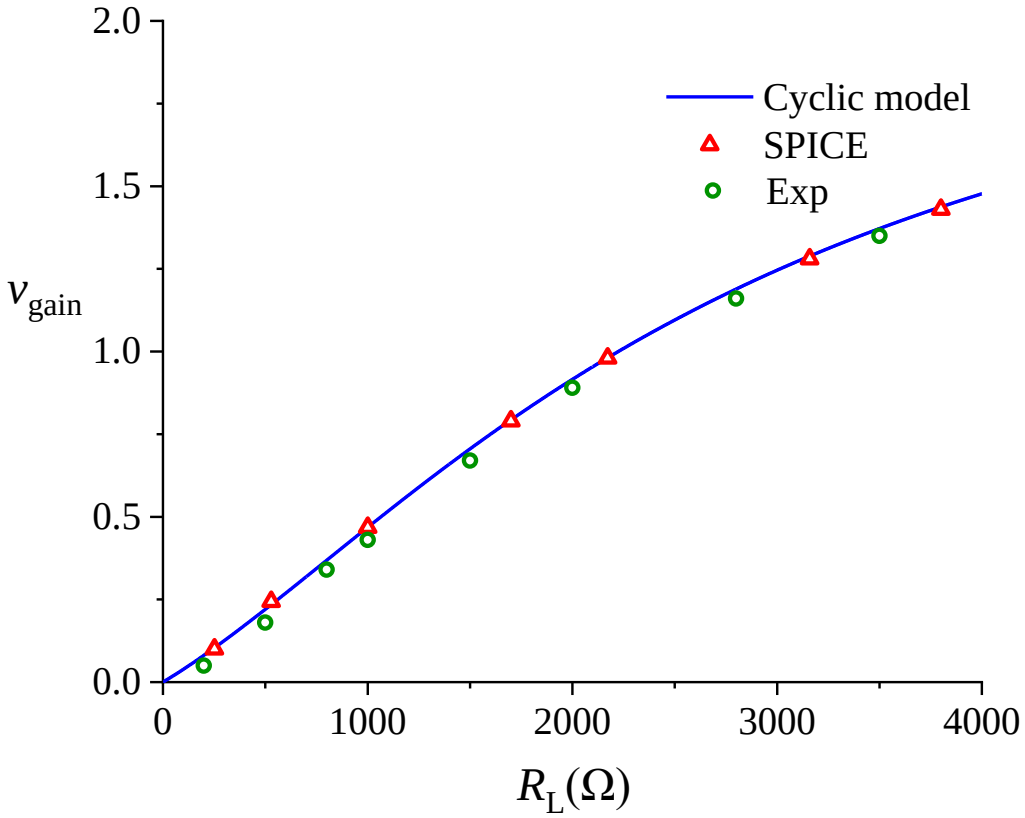
As can be seen from Fig. 6.5, the zero crossings of resonant current are clearly indicated by the reference signal v_{ZC}, and ZVS is achievable as v_{Cin} reaches V_{dc} during the deadtime, that is $v_{\mathrm{Cin}}(t_3) \geq V_{\mathrm{dc}}$. ZVDS is also obtained since the estimated current $i_{L1}(t_3) \propto \frac{\mathrm{d}v_{\mathrm{Cin}}(t_3)}{\mathrm{d}t} = 0$. This is to be expected since the radial-mode PT was design to meet the critical criterion described in [6.7].

In Fig. 6.6, the ZVS and output performance are illustrated as a function of load resistor R_L with the same circuit conditions and time intervals as given in Table 6.1. Equation (6.23) can be used to evaluate ZVS performance of a given PT, and

this is demonstrated in Fig. 6.6(a) where the ZVS factor K_{ZVS} is compared with SPICE simulation and experimental measurements. As can be seen from Fig. 6.6(a), the input capacitor voltage v_{Cin} is normalized and represented as K_{ZVS} = $v_{Cin}(t_3)$ /(V_{dc}). It is shown that the proposed cyclic model correlates well with the SPICE and experimental results. For this particular circuit operating condition, ZVS is clearly achievable for all load resistor values, while the worst case occurs at the matched load condition (1kΩ) where K_{ZVS}=1, which corresponds to the v_{Cin} shown in Fig. 6.5(b). The experimental measurements of K_{ZVS} are all slightly above the ZVS threshold since the body diode of the MOSFETs conducts, and this is equivalent to the proposed model, as explained in section 6.5.1. The RMS value of output voltage $v_{L,RMS}$ is normalised and given as the voltage gain v_{gain}= $v_{L,RMS}/\underline{N}V_{dc}$. As can be seen, the cyclic model matches well with the simulation and experimental results.



(a)



(b)

Fig. 6.6: Model validation: (a) ZVS and (b) voltage gain of the H-bridge converter.

6.6 ZVS and output voltage characteristics

6.6.1 Δt_1 sensitivity analysis

The ZVS performance can be assessed quantitatively with equation (6.23) by comparing $v_{Cin}(t_3)$ to V_{dc}, and this is done by controlling Δt_2. Since the range of Δt_2 variation is determined by Δt_1, the sensitivity of Δt_1 in terms of key circuit parameters should be evaluated initially. In general, the value for Δt_1 during M1 can be found from equation (6.24).

In Fig. 6.7, the deadtime Δt_1 is normalized to the switching period $T=1/f_s$ and plotted against ZVS factor K_{ZVS} and voltage gain v_{gain} with the same circuit parameters as used in previous section. As can be seen, both K_{ZVS} and v_{gain} exhibit

negligible change. Therefore, it can be assumed that sensitivity of K_{ZVS} and v_{gain} to Δt_1 is low for modest changes in timing.

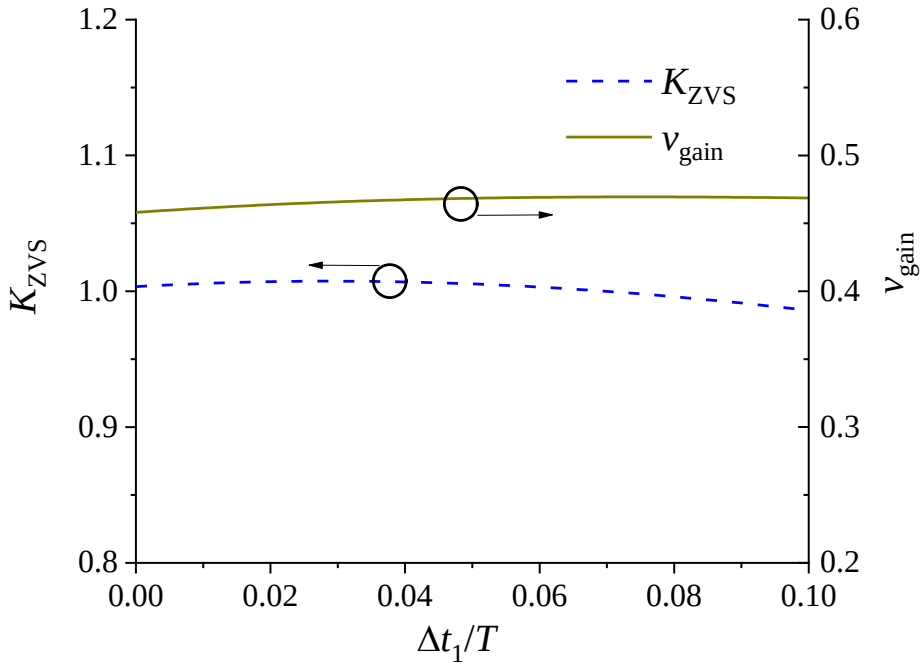


Fig. 6.7: Δt_1 sensitivity analysis for ZVS factor and voltage gain.

6.6.2 ZVS and output profile

The 3D plot shown in Fig. 6.8 illustrates the K_{ZVS} dependence on both load R_L and normalised operating frequency ($f_n = f_s / f_0$) with the same fixed deadtime intervals employed to generate Fig. 6.3 (parameters are summarised in Table 6.1). The K_{ZVS} curve in Fig. 6.6(a) is also indicated in Fig. 6.8 for the same parameter range. As can be seen, the ring-dot PT exhibits two distinct regions where ZVS is achievable for the inductorless H-bridge configuration as indicated by the shaded areas. These two regions are located at high and low loads respectively and are barely connected at the matched load. Careful design of the PT could ensure ZVS region can be maintained without disconnection for large load variations, and it brings the opportunity for output regulation since it is possible

to simultaneously control the deadtime, frequency and load to achieve ZVS continuously.

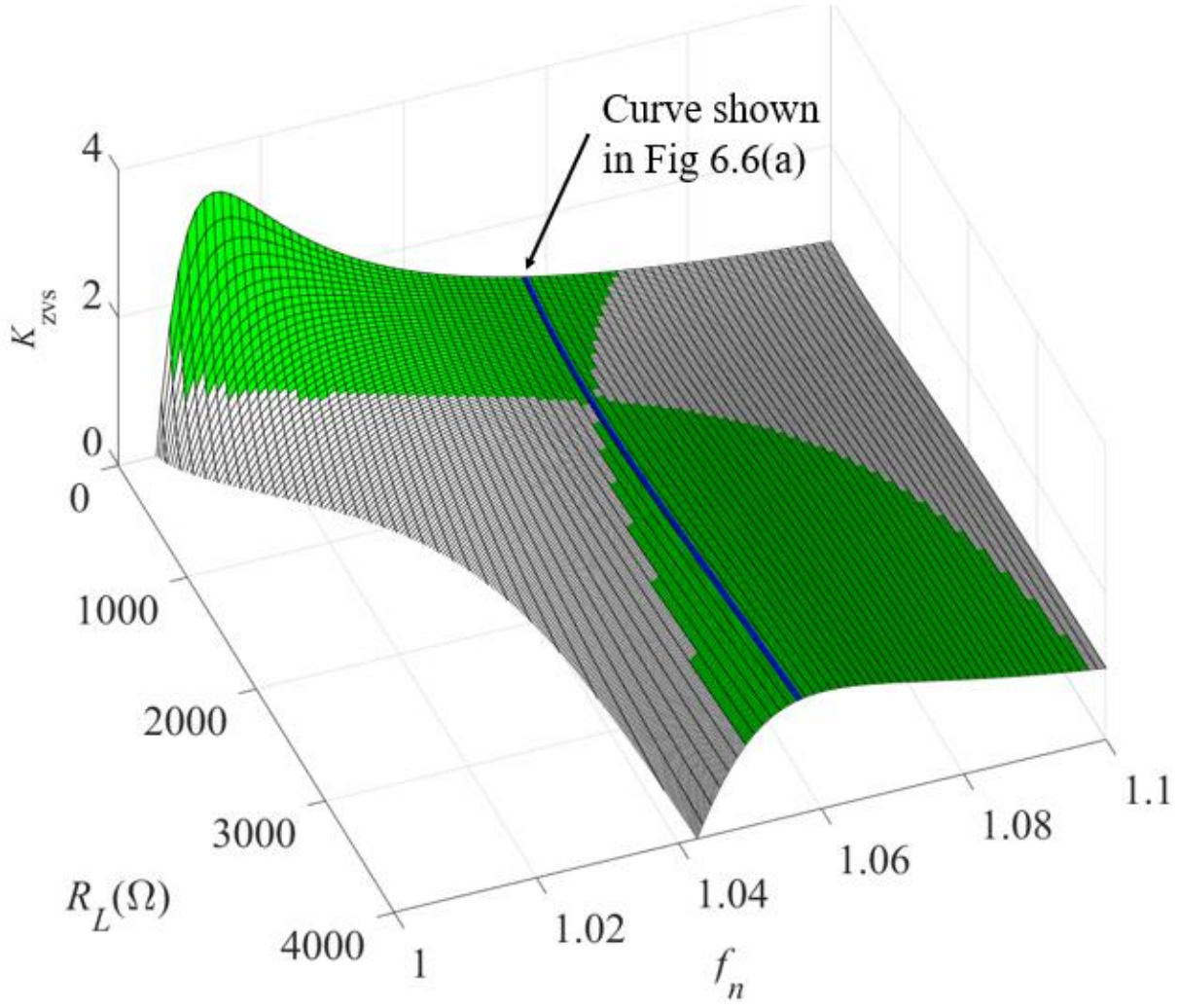
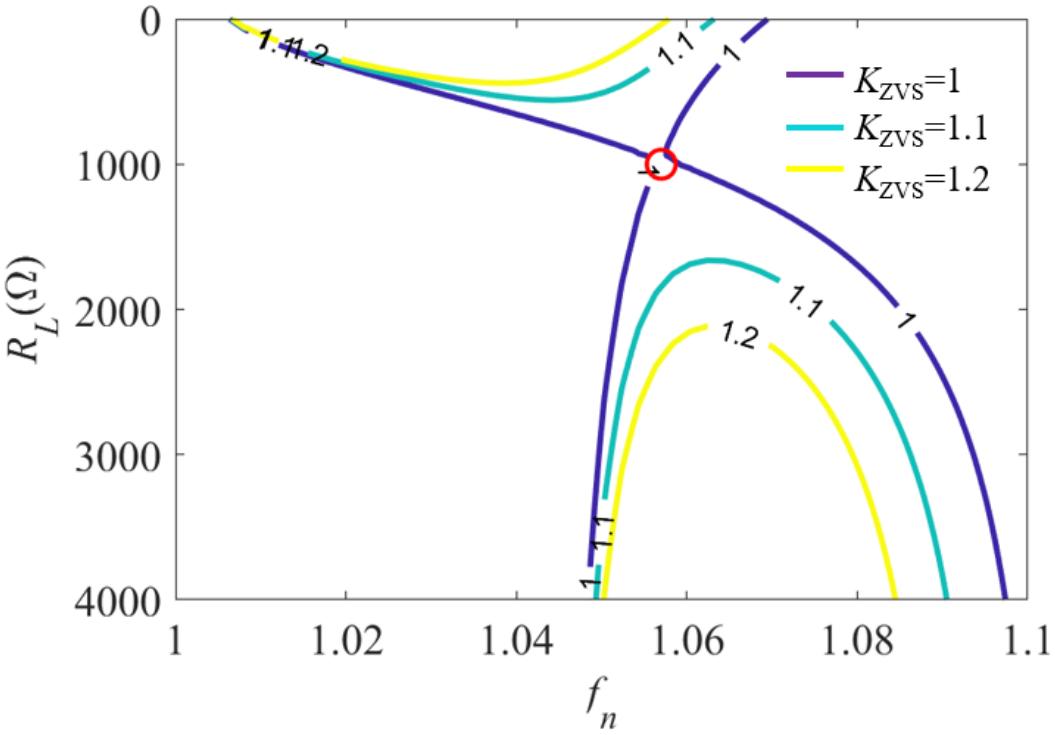


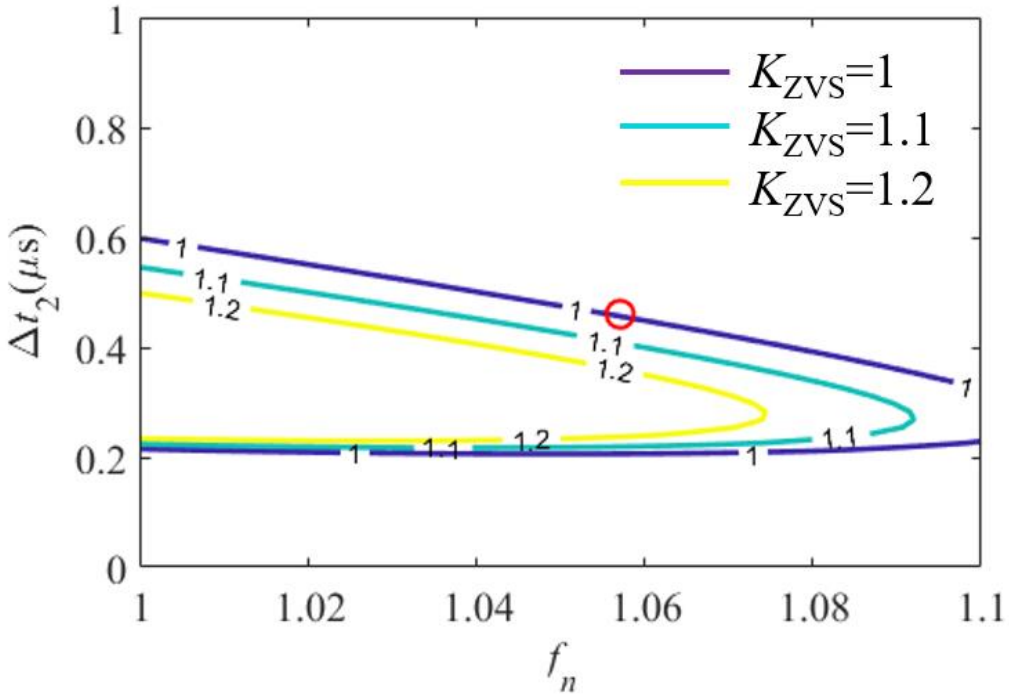
Fig. 6.8: ZVS characteristics for the radial-mode PT (shaded region is where $K_{ZVS} \geq 1$)

Expanding on the ZVS characteristics shown in Fig. 6.8, Fig. 6.9 demonstrates the relationship between (a) the load and normalised frequency and (b) the time interval Δt_2 and normalised frequency for different K_{ZVS} conditions. The contour of K_{ZVS} =1 is equivalent to walking along the boundary of the shaded area in Fig. 6.8. The circuit operating condition listed in Table 6.1 is also indicated as a red circle in both Fig. 6.9(a) and (b). In Fig. 6.9(a), ZVS is achievable at the matched

load condition. To maintain ZVS, both switching frequency and Δt_2 should be varied simultaneously and a maximum of 0.39μs variation for Δt_2 is required (i.e. K_{ZVS}=1), as shown in Fig. 6.9 (b).



(a)



(b)

Fig. 6.9: Contour plot of operating loci for the radial-model PT. (a) normalized frequency with load loci and (b) normalized frequency with time interval Δt_2 loci.

Fig. 6.10 shows the normalised output voltage gain characteristic with changes in both the operating frequency and the load for the same parameter range and circuit conditions with respect to Fig. 6.8. The voltage gain response corresponding to the conditions used to generate the Fig. 6.6(b) are indicated by the blue curve. As can be seen, the region of maximum achievable voltage gain is not completely covered by the ZVS area. The voltage gain increases with increasing load resistance, and for each load, the peak voltage gain occurs near f_n around 1.043 (shown as a red curve in Fig. 6.10). This indeed indicates the optimal frequency for Δt_2 variation in order to obtain the maximum voltage gain for regulation.

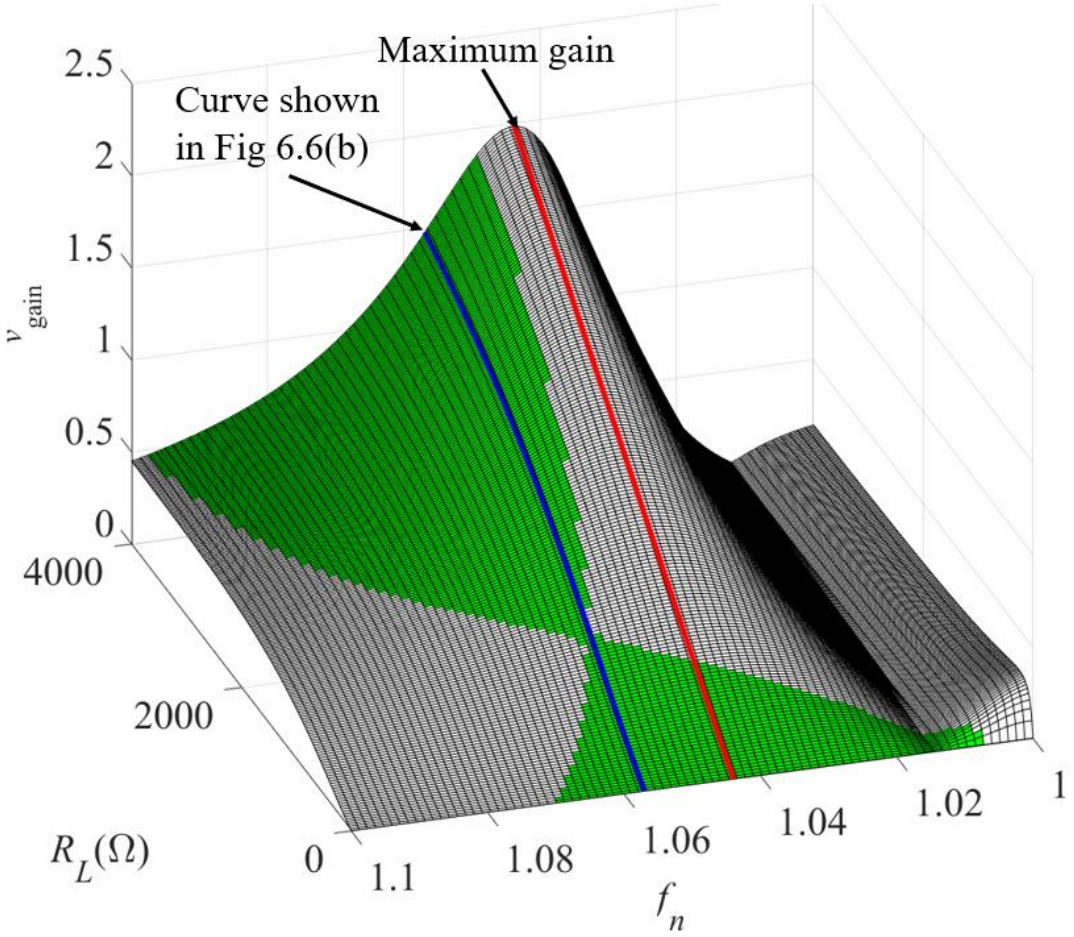
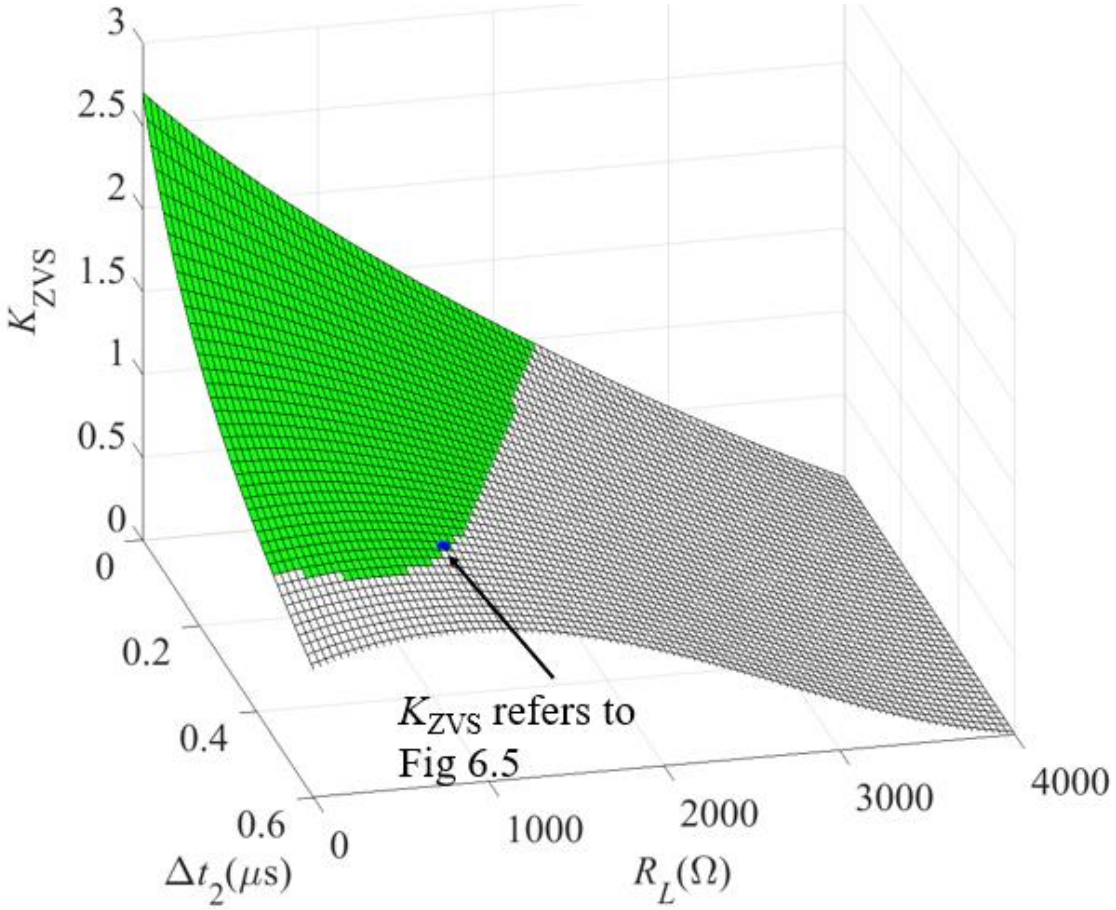


Fig. 6.10: Voltage gain profile of the radial-mode PT (shaded regions are where $K_{ZVS} \geq 1$)

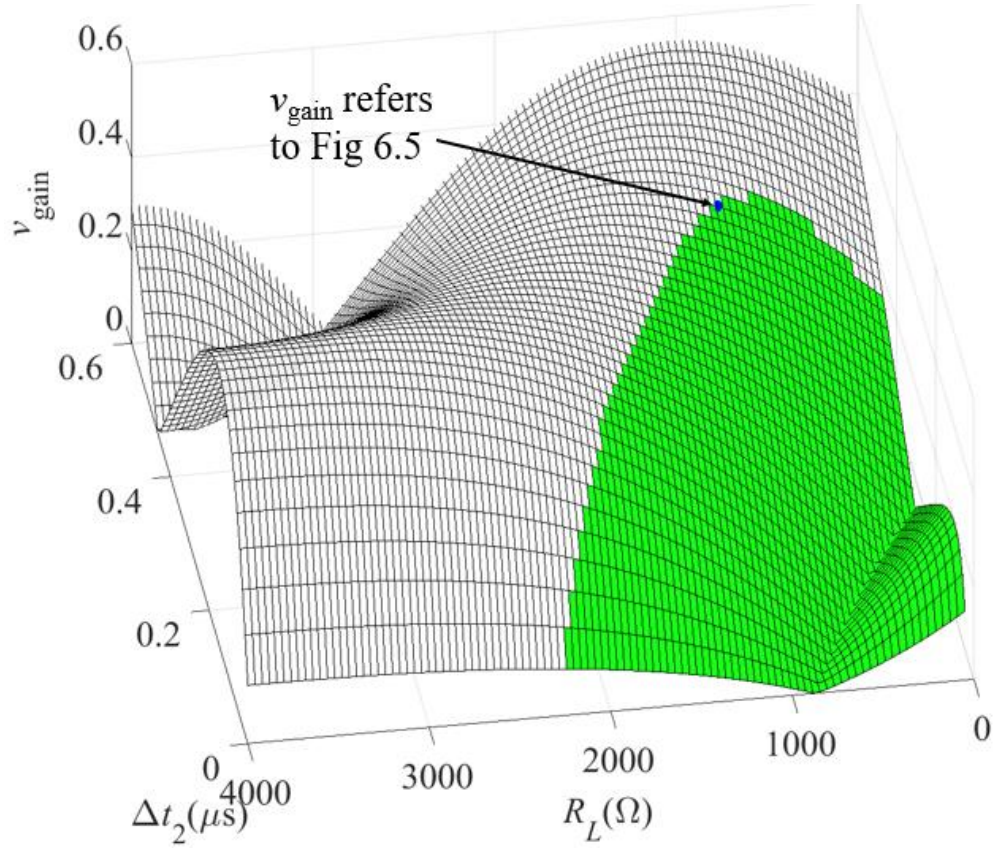
6.7 Simultaneous voltage regulation and ZVS

6.7.1 Output regulation ability

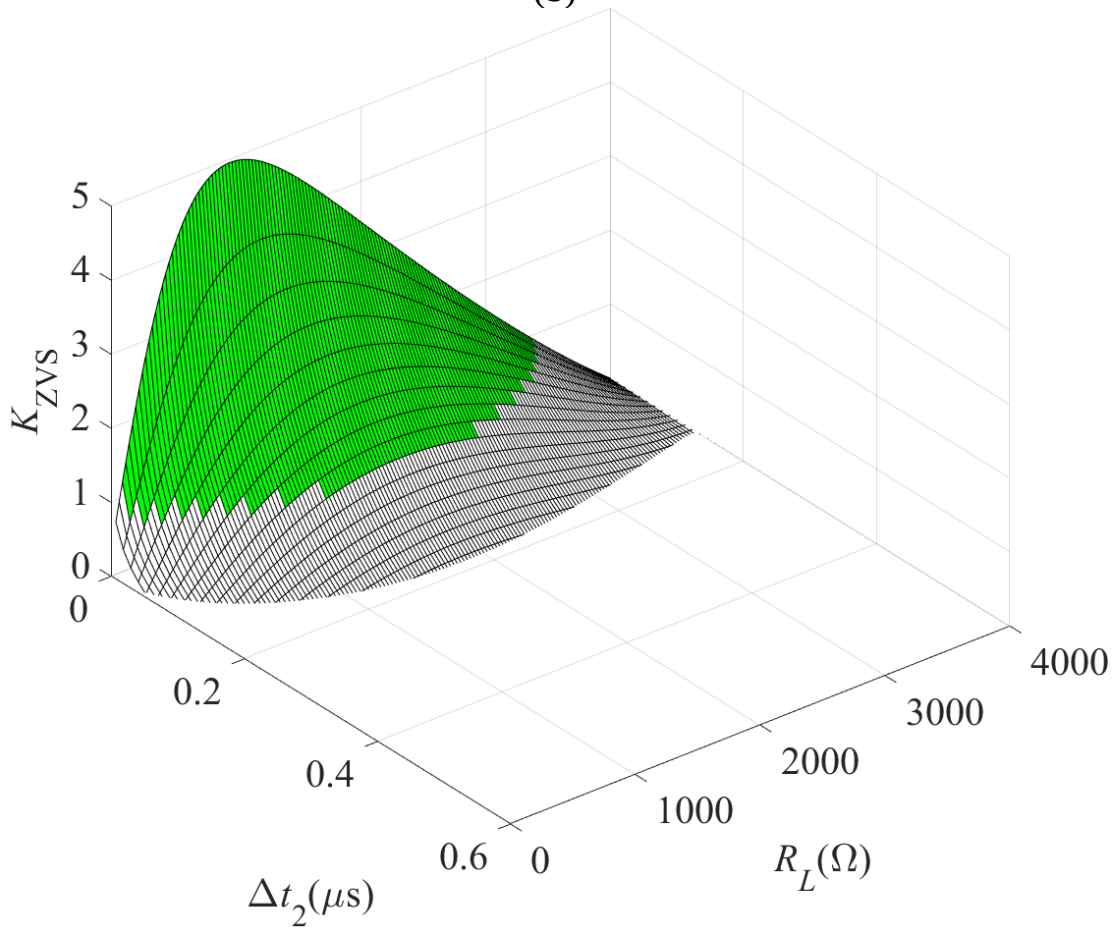
Although the highest efficiency can be achieved when the PT operates at the matched load condition, this could be difficult to achieve ZVS for inductorless driven PT in practice [6.10]. Moreover, it is difficult to regulate the output voltage while still achieving ZVS, since simultaneous parameter control should be employed and the ZVS region of should be continuously connected during voltage regulation, as highlighted in [6.6][6.7][6.11]. Therefore, an analysis for achieving simultaneous ZVS and output voltage regulation is presented in this section based on the previous cyclic-mode analysis.



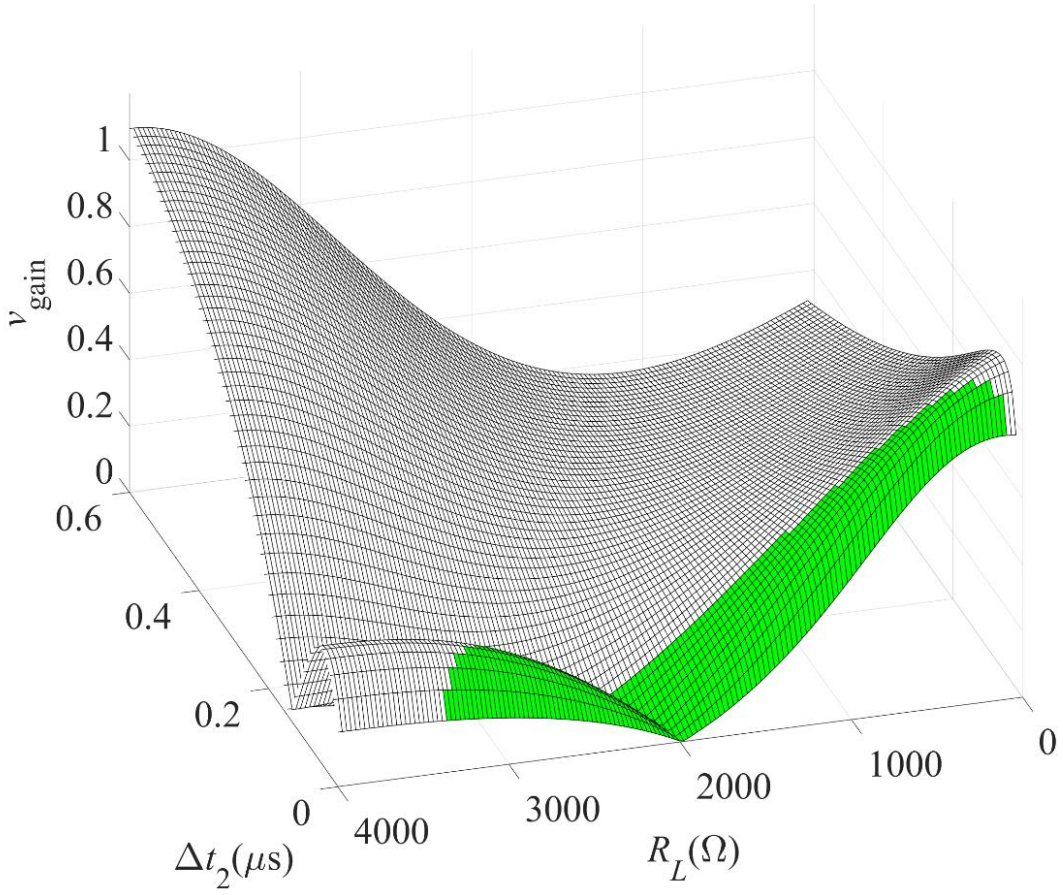
(a)


v_{gain} refers to Fig 6.5
v_{gain}
0.6
0.4
0.2
0
0.6
0.4
0.2
0
$\Delta t_2(\mu s)$
4000
3000
2000
1000
0
$R_L(\Omega)$

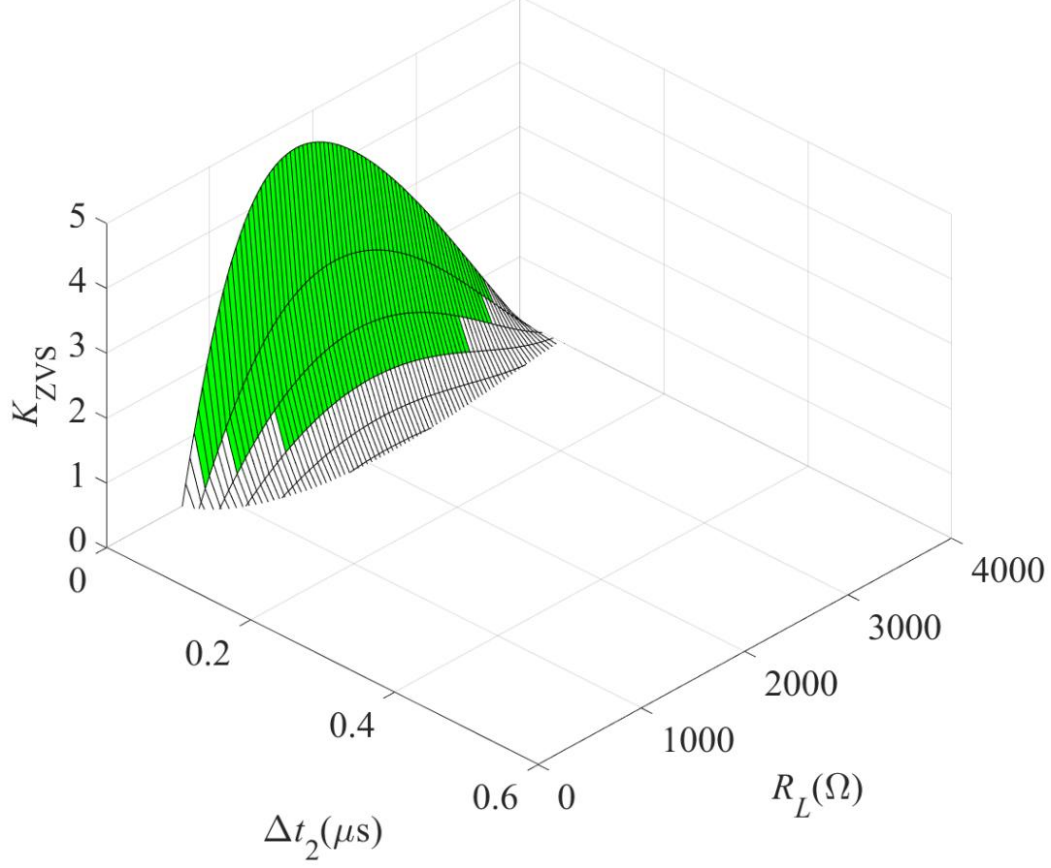
(b)


K_{ZVS}
5
4
3
2
1
0
0
0.2
0.4
0.6
$\Delta t_2(\mu s)$
0
1000
2000
3000
4000
$R_L(\Omega)$

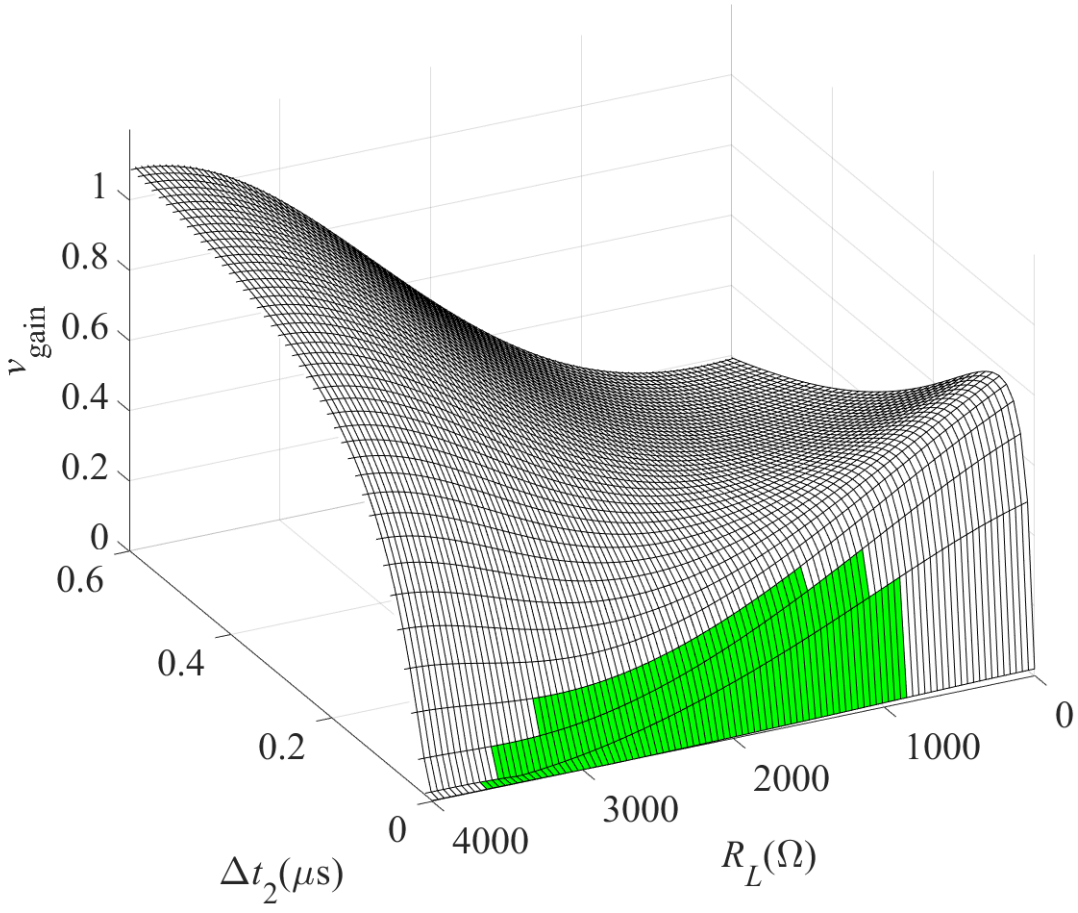
(c)


v_{gain}
1
0.8
0.6
0.4
0.2
0
0.6
0.4
0.2
0
$\Delta t_2(\mu s)$
4000
3000
2000
1000
0
$R_L(\Omega)$

(d)


K_{ZVS}
5
4
3
2
1
0
0
0.2
0.4
0.6
$\Delta t_2(\mu s)$
0
1000
2000
3000
4000
$R_L(\Omega)$

(e)



(f)

Fig. 6.11: ZVS profile at operating frequency of (a) f_n=1.057, (c) f_n=1.043, (e) f_n=1.01, and their corresponding normalized gain performance at (b) f_n=1.057, (d) f_n=1.043, (f) f_n=1.01 (shaded region is where $K_{ZVS}\geq 1$).

Fig. 6.11 highlights the K_{ZVS} and voltage-gain dependence on both the time interval Δt_2 and the load. To demonstrate the ZVS and output voltage regulation ability, the analysis is performed with the same circuit parameters as used in the previous section. By way of example, the operating locus for condition of f_n=1.057f_0 is illustrated in Fig. 6.9. The duration required for Δt_1 can be calculated from equation (6.24), for f_n=1.057f_0, f_n=1.043f_0 and f_n=1.01f_0, the Δt_1 values are determined as 0.36μs, 0.356μs and 0.351μs, respectively. The experimental results of v_{Cin} and v_{gain} correspond to Fig. 6.5 are also shown in Fig. 6.11 (a) and (b), indicated by blue circles, which are located at the boundary of the ZVS area (K_{ZVS}=1 at the matched load). As can be seen, at the matched load condition, ZVS

is no longer achievable when Δt_2 increases. This is to be expected as interval Δt_3 would be reduced accordingly to ensure total deadtime ($\Delta t_1 + \Delta t_2 + \Delta t_3$) is 1/(4$f$) based on the design criterion [6.7], and consequently, input capacitor voltage v_{Cin} cannot reach V_{dc} since Δt_3 is too small. In Fig. 6.11(a) and (b), although ZVS can be continuously obtained over a wide range of operating conditions, the corresponding normalised voltage gain under ZVS region is relatively low (i.e. 0.45 maximum).

Although the ZVS region is reduced at 1.043f_0 compared with 1.057f_0, shown in Fig. 6.11(c), the corresponding voltage gain shown in Fig. 6.11(d) indicates a wide range of operation for output regulation with a maximum voltage gain of 0.9 at the 198Ω load with 33.3ns Δt_2. By comparison, in Fig. 6.11(b) and Fig. 6.11(f), the maximum achievable voltage gains are reduced to 0.45 and 0.42, respectively. Therefore, careful consideration should be taken for output voltage regulation in order to achieve both high voltage gain and ZVS simultaneously.

6.8 Practical design considerations and discussion

Although the cyclic model presented in this paper mainly focuses on resistive load, other types of load and output configurations are also applicable. In general, maximum power can be delivered to the load when the voltage gain of a PT is maximised. From the circuit design perspective regarding output rectifier, it has been reported that, for a given PT, the AC output configuration gives a larger maximum PT output power compared to the DC output configuration [6.12]. From the PT design perspective, since optimum operating frequency is changed from achieving highest efficiency to obtaining maximum voltage gain, the PT is not necessarily designed to achieve ZVS at the matched load condition (see Fig. 6.10, the maximum voltage gain occurs at f_n=1.043 while the highest efficiency at matched load condition is at f_n=1.057). As a result, this would in turn reduce

the PT dimension requirements (e.g. stacked disc-type PT), since the matched load indicates highest efficiency point that requires smallest mechanical current. If operating at matched load is no longer required, the critical criterion (i.e. the capacitor ratio, C_{n}) can be relaxed. For example, for a ring-dot PT, this might mean less electrode area on the output section. Relaxing the criterion reduces the mechanical current and improves the voltage gain [6.10].

The thermal condition should also be considered since the piezoelectric properties (e.g. dielectric, elastic and piezoelectric constants [6.13]) vary with temperature, which could limit the regulation ability. All these effects can change the frequency response of a PT by shifting the resonant frequency and decreasing the voltage gain. In particular, the quality factor can be significantly reduced when a PT operates at high power levels due to vibration velocity [6.14] and heating [6.15]. The reduction of quality factor is associated with an increase of the damping resistor R_1, which further decreases the voltage gain. To investigate the ZVS and output voltage performance of a PT for a temperature-dependent parameter variation, extreme value analysis should be used, and both extreme (e.g. no load/full load condition, zero and maximum Δt_2 time interval, extreme operating temperature) and expected circuit condition should be evaluated.

In general, for a given PT, with specified output voltage requirement, load and input range, the design process of achieving output voltage regulation under ZVS using the proposed model is summarized as follows:

1) Generate K_{ZVS} and v_{gain} profile to find the optimum operating frequency which gives the maximum voltage gain.

2) Set up the optimum operating frequency and replot the K_{ZVS} and v_{gain} figures with respect to the deadtime interval Δt_2.

3) Finally, vary Δt_2, input voltage and load to see if this PT is able to meet voltage regulation requirement under ZVS using inductorless H-bridge configuration.

To summarise, with the ring-dot radial-mode PT employed in this work, the inductorless H-bridge converter is able to provide a 5V $v_{L,\mathrm{RMS}}$ from 10V to 60V input, by varying the deadtime interval Δt_2 . Moreover, ZVS is continuously achievable during the voltage regulation process as expected. By employing the proposed cyclic model, circuit behaviour is predictable, the ZVS boundary and voltage gain as a function of circuit parameters (i.e. switching frequency and deadtime) are clearly demonstrated, and can be used to find the operating frequency for achieving maximum voltage gain. Subsequently, by controlling the time interval Δt_2 and input voltage at the optimum frequency, the output voltage regulation can be realised with continuously achievable ZVS.

6.9 Chapter conclusions

A methodology for predicting the ZVS and output voltage capabilities of an inductorless driven PT-based converter is presented. Through the cyclic-mode analysis, an analytical model of the PT under ZVS operation is derived. Measurements taken from a radial-mode PT is used to validate the proposed model. Subsequently, the model is employed to show the ZVS profile, ZVS boundary and requirement for continuously achieving ZVS. By using a H-bridge configuration, the output can be controlled by varying the deadtime period. Furthermore, the optimum operating frequency for maximum voltage gain is demonstrated under continuous ZVS region. The output voltage characteristics of the radial-mode PT is generated at different frequencies, highlighting the importance of PT selection in order to obtain maximum achievable voltage gain meanwhile still achieving ZVS. Since the ZVS and output regulation ability is dependent on input capacitance, deadtime period, resonant current and operating

frequency, the proposed model can be used to assess the appropriateness of the PT for a given application.

6.10 References

[6.1] M. S. Roedgaard, M. Weirich, and M. A. E. Andersen, “Forward conduction mode controlled piezoelectric transformer-based PFC LED drive,” *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4841–4849, 2013.

[6.2] J. Díaz, F. Nuno, M. J. Prieto, J. A. Martín-Ramos, and P. J. Villegas Saiz, “Closing a second feedback loop in a DC-DC converter based on a piezoelectric transformer,” *IEEE Trans. Power Electron*., vol. 22, no. 6, pp. 2195-2201, 2007.

[6.3] E. M. Baker, W. Huang, D. Y. Chen, and F. C. Lee, “Radial mode piezoelectric transformer design for fluorescent lamp ballast applications,” *IEEE Trans. Power Electron.*, vol. 20, no. 5, pp. 1213- 1220, 2005.

[6.4] S. Ben-Yaakov and S. Lineykin, “Maximum power tracking of piezoelectric transformer HV converters under load variations,” *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 73-78, 2006.

[6.5] F. E. Bisogno *et al*., "Comparison of resonant topologies for step-down applications using piezoelectric transformers," *2004 IEEE 35th Annual Power Electronics Specialists Conference*, pp. 2662-2667, vol.4, 2004.

[6.6] M. P. Foster, E. L. Horsley, and D. A. Stone, “Predicting the zero-voltage switching profiles of half-bridge driven inductor-less piezoelectric transformer-based inverters,” *IET Power Electron.*, vol. 5, pp. 1068–1073, 2012.

[6.7] M. P. Foster, J. N. Davidson, E. L. Horsley, and D. A. Stone, “Critical Design Criterion for Achieving Zero Voltage Switching in Inductorless Half-Bridge-Driven Piezoelectric-Transformer-Based Power Supplies,” *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 5057–5066, 2016.

[6.8] H. R. Visser and P. P. J. Van den Bosch, “Modelling of periodically switching networks,” *IEEE Power Electronics Specialists Conference*, 1991, pp. 67–73.

[6.9] M. P. Foster, H. I. Sewell, C. M. Bingham, D. A. Stone, D. Hente, and D. Howe, “Cyclic-averaging for high-speed analysis of resonant converters,” *IEEE Trans. Power Electron.*, vol. 18, no. 4, pp. 985–993, 2003.

[6.10] E. L. Horsley, Modelling and analysis of radial mode piezoelectric transformers and inductor-less resonant power converters, Ph.D thesis, University of Sheffield, 2011.

[6.11] Z. Yang, J. Forrester, J. N. Davidson, M. P. Foster, and D. A. Stone, “Resonant current estimation and phase-locked loop feedback design for piezoelectric transformer-based power supplies,” *IEEE Trans. Power Electron.*, pp. 1–1, 2020.

[6.12] E. L. Horsley, A. V. Carazo, N. Nguyen-Quang, M. P. Foster, and D. A. Stone, “Analysis of inductorless zero-voltage-switching piezoelectric transformer-based converters,” *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2471–2483, 2012.

[6.13] H. W. Joo, C. H. Lee, J. S. Rho, and H. K. Jung, “Analysis of temperature rise for piezoelectric transformer using finite-element method,” *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 53, no. 8, pp. 1449–1457, 2006.

[6.14] M. Umeda, K. Nakamura, and S. Ueha, “Effects of vibration stress and temperature on the characteristics of piezoelectric ceramics under high vibration amplitude levels measured by electrical transient responses,” *Japanese J. Appl. Physics, Part 1 Regul. Pap. Short Notes Rev. Pap.*, vol. 38, no. 9 B, pp. 5581–5585, 1999.

[6.15] M. Umeda, S. Takahashi, Y. Sasaki, K. Nakamura, and S. Ueha, “Vibration stress and temperature dependence of piezoelectric resonators with lead-zirconate-titanate ceramics,” *Electron. Commun. Japan, Part II Electron.* vol. 83, no. 9, pp. 1–7, 2000.

Chapter VII

Conclusion

This Chapter summarises and discusses the work presented in the thesis. The main contributions from each Chapters are reported. The future work, which further expands the research that has been presented in this thesis, is demonstrated.

7.1 Discussion

This thesis proposes several techniques to improve PT-based converter design, including resonant current estimation, resonant frequency control, output voltage regulation and predicting circuit behaviour using analytical model.

In Chapter I, the motivation of this work, the impetus for higher energy density power electronic circuits, is discussed. To achieve high-efficiency and high-power operation, the PT-based power converter design is identified as one vital area of research. Therefore, this thesis focuses on PT-based resonant converter design, and provides a contribution to the state-of-the-art, as described below.

To familiarise the reader with the fundamental knowledge and latest research of the field, a literature review is provided in Chapter II. Commonly used piezoelectric devices, materials and modelling techniques are described. Four types of piezoelectric transformers are presented utilising different vibration modes, including thickness mode PTs, radial mode PTs, thickness-shear mode PTs and longitudinal mode PTs. Various converter topologies are reported, such as class-E, push-pull and half-bridge. Despite the requirement of precise control for achieving ZVS, the inductorless configuration is still the best candidate for PT-based resonant converters due to its reduced component count. Different

control techniques are discussed according to the purpose of control. It is indicated that the PLL is the best option for PT-based converters since it works correctly irrespective of operating conditions and provides fast resonant frequency tracking. Various techniques for output voltage regulation are reported and it is highlighted that additional efforts can be made to improve regulation accuracy due to PT vibration. To provide feedback reference signals for a control circuit, resonant current estimation is required and several approaches are reviewed. Methods for modelling the PT-based converter are described and cyclic modelling is described in detail. Finally, the design challenges and research gaps were identified, some of which have been addressed by the research presented in this thesis.

Chapter III described the techniques used for resonant current estimation in the subsequent chapters. The operating principle of PT-based inductorless half-bridge resonant converter is provided with ZVS and non-ZVS condition initially. Three variants of current estimators with mathematical analysis are described in detail, including two estimators at input section and one estimator at output section. By reconstructing the resonant current and detecting the zero crossings of the resonant current, the synchronisation edges necessary for achieving ZVS are indicated and thus a feedback signal with ZVS information is provided for the control circuit. Compared with the primary-side implementation approaches, the secondary-side implementation indicates improved robustness to noise. All these approaches are employed throughout the thesis as a way for detecting the zero-crossing edges of the resonant current necessary for synchronisation and for achieving ZVS.

A novel technique to lock onto the phase and frequency of resonant current was described in Chapter IV. The technique involved an analogue PLL that compensates resonant frequency drift and provides fast tracking. By using the

reference signals from current estimators presented in Chapter III, the PLL is able to synchronise to both the phase and the frequency of the resonant current, and generate the in-phase gate drive signals with adequate deadtime. Three types of gate signal generators have been proposed: a phase locked PWM which employs the voltage of the timing capacitor of PLL, a time-delay circuit which shapes the PLL output through a RC network, and a frequency divider which halves the PLL output frequency. A comparative analysis of nine variants of PLL controllers and current estimators are analysed in terms of noise immunity and lock-on period. The techniques were verified on a prototype inductorless PT-based converter and results show significant improvement on existing fast resonance tracking.

Chapter V used the current estimation methods presented in Chapter III, and PLL control techniques presented in Chapter IV, to regulate the output voltage of an inductorless PT-based converter. A burst-mode hysteresis control, which modifies the on/off periods of the MOSFETs by using a hysteresis window with regulation limit, was employed to provide output voltage regulation of the DC/DC converter. The mechanical vibration initialisation and non-instant stop behaviour of a PT, which causes inaccuracy of voltage regulation, has been analysed. Experimental measurement validates the proposed design, and it is indicated that the fast lock-on behaviour of the PLL enables a quick start-up of the PT to reach ZVS. In addition, the output characteristics of regulation limit, load and line regulation are described in detail.

A novel modelling technique which predicts the ability of an inductorless PT-based H-bridge converters to simultaneously achieve ZVS and output regulation, was presented in Chapter VI. A new idea of output voltage regulation by controlling deadtime interval was presented. The operating mode of the proposed H-bridge circuit is analysed initially. A non-linear state-variable model was derived and then decomposed into a piecewise linear model based on the circuit

operating mode. Subsequently, cyclic-mode analysis was employed to model the periodically switching network to determine the steady-state values of the circuit for a given operation condition. With the proposed cyclic mode, ZVS and voltage gain characteristics were presented in terms of deadtime period, load and operating frequency. The model was employed to provide a voltage gain profile indicating regions where output voltage regulation can be continuously achieved while still obtaining ZVS. The ZVS boundary and optimum operating frequency for maximum voltage gain are highlighted. Both simulation and experimental results validated the proposed modelling methods. Finally, the output regulation ability was described with respect to deadtime and load condition at different switching frequencies, and practical design consideration regarding PT design, ZVS and voltage regulation are demonstrated.

7.2 Thesis conclusions

This thesis develops the control and modelling techniques to improve the performance of a PT-based resonant converter. It subsequently proposes several approaches which provides these developments. Novel current estimation techniques are described for indicating ZVS while new gate signal generators are demonstrated for providing an adequate deadtime. These facilitates the novel PLL control techniques with nine variants for achieving ZVS of an inductorless PT-based converter. To predict circuit behaviour and achieving simultaneous ZVS and voltage regulation, a new analytical model is developed, with a novel idea for achieving voltage regulation by varying deadtime period. Both simulation and experimental results validate the proposed design.

Bringing all together, the techniques presented in this thesis will allow the engineers to develop PT-based resonant power supplies with improved ZVS and voltage regulation performance. These improvements are accomplished by the enhanced PLL controllers and modelling technique as a result of this work.

The research proposed in this work has been published in conference and journal papers, with two more papers in preparation, indicating the relevance of the research to the PT-based SMPSs.

7.3 Future work

Although the work presented in this thesis offers development for the state-of-the-art, further improvements on this work are possible. Potential areas for further development are summarised in following subsections.

7.3.1 ZVS for H-bridge MOSFETs capacitance

Chapter VI describes a control technique for achieving simultaneous ZVS and voltage regulation by varying the deadtime period in which the PT is held at 0V. Although ZVS is achievable for C_{in}, it is not achievable for MOSFET capacitance.

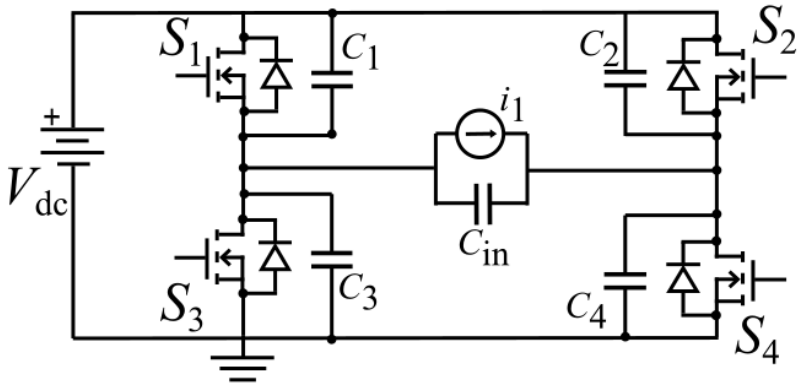


Fig. 7.1: H-bridge PT-based converter.

As shown in Fig. 7.1. C_1-C_4 are the MOSFET capacitors and C_{in} is the PT input capacitor. PT is represented as an equivalent current source i_1. During deadtime period the resonant current circulates in the resonant tank and charges the MOSFET capacitors. The voltage across C_{in} is in the range $-V_{dc}$ to V_{dc}, and while it is charging, the voltage of each bridge is also charging. At the start of the deadtime, the left bridge (i.e. C_1 and C_3) is at 0V and the right bridge (i.e. C_3 and C_4) is at V_{dc}. At the end of the deadtime, the left bridge is at V_{dc} while right bridge

is at 0V. When C_{in} is 0V, the voltage across the left bridge is equivalent to the right bridge. Therefore, at this point, if two MOSFETs are turned on, the energy in the MOSFET output capacitor is discharged and results in switching losses.

Therefore, a new control could be implemented such that the right hand bridge leg is turned off and output voltage of the right hand bridge is allowed to change from V_{dc} to 0V under the control of the resonant current. Then the low-side MOSFET are turned on to obtain the 0V deadtime period. The left-hand bridge leg is operated in a similar manner where it is turned off and its output voltage is charged to V_{dc}. Therefore, the switching loss can be eliminated in the MOSFETs.

7.3.2 Describing function

In Chapter VI, an analytical model which employs cyclic mode analysis is presented to predict ZVS and output characteristics, in terms of the key circuit parameters. For the resonant circuits where a non-linear load (i.e. LEDs and rectifier) is used, it is suggested that a describing function can be used to approximate the load. Furthermore, compared with cyclic modelling method, which is a numerical solution for circuit analysis, the describing function technique offers a quantitative measurement of the PT-based converter's ability to achieve ZVS and a better understanding of fundamental mechanisms involved. A critical design criterion might be developed to provide a guideline for the converter and the PT design, for achieving simultaneous ZVS and output regulation.