INSULATED GATE BIPOLAR TRANSISTOR'S AGEING AND ITS IMPACTS ON THE ELECTROMAGNETIC CONDUCTED EMISSIONS

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To my wife Corinne and my daughter Marta,

For their patience, reassurance, and love.

Abstract

Insulated Gate Bipolar Transistors (IGBTs) have become key electronic components in many applications, including life critical or mission critical products. The understanding of the failing mechanisms and the reliability aspects of the IGBT have become important to semiconductor manufacturers and application engineers, to provide reliable solutions especially in enhanced lifetime (thirty to forty years) applications. Since the IGBT is employed at elevated power scenarios, its sub-structures can be prone to multiple failure mechanisms which can lead to the general IGBT failure. The IGBT's failure mechanisms can be mainly divided into two categories: die-related failure mechanisms and package-related failure mechanisms. These will contribute to gate oxide degradation, bond-wire lift-off, bond-wire cracks, bond-wire ruptures, solder delamination, solder cracking, and the degradation of the metallization layers. The presented work tried to address the current gap in knowledge, by studying the relationship between specific degradation within the IGBT (primarily the degradation of the die-attach layer and the gate's oxide contamination), the static and dynamic operation of the IGBT, and hence the consequential influence this degradation has, on the EM conducted disturbances. For this purpose, accelerated ageing was conducted on commercially available 600V, 16A IGBTs. This was achieved through the development of a power cycling accelerated ageing system (PCAS), which subjects the IGBT to thermo-electrical overstress. The degree of the inflicted degradation was analysed through X-Ray inspection. Moreover, the static electrical parameters of tested IGBTs, were characterized before, during and after accelerated ageing, noting significant changes.

Consecutively the switching transients of the aged IGBTs were studied, by developing a Double-Pulse characterization system. This evidenced that the employed accelerated ageing, contributed to significant slow-down of the IGBT's turn-off transients, while producing minimal changes in the IGBT's turn-on transients. This led to the modelling of the IGBT's switching transients' evolution with ageing, effectively evidencing that the die-attach degradation together with the monitored contamination of the gate's oxide, were contributing to a more pronounced turn-off "tail current", and changes in the IGBT's parasitic elements predominantly the Miller capacitance. Finally, an EM conducted emissions experimental setup was developed, where it was determined that there is a direct correlation between the inflicted degradation, the switching transients, predominantly the collector current (I_C) turn-off transient, and the measured decrease in the EM conducted disturbances.

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Declaration

I declare that this thesis is a presentation of original work, and I am the sole author. This work has not previously been presented for an award at this, or any other, University. All sources are acknowledged as References.

Chapter 1 Introduction

1.1 Research Background

Today power electronics play a significant role in the operation and performance of ships, aircraft, electric or hybrid electric vehicles, utility interfaces, renewable energy sources, power transmission and many other industrial applications. These power-electronics based systems, utilize power semiconductor devices (PSDs) for power loads activation and control. Degradation or failure of these devices can reduce system efficiency or may lead to system failure, which can yield to monetary losses, mission abandonment, or life-threatening accidents. Hence, the reliability of power-electronic systems and more specifically the reliability of PSDs, has become crucial and has recently drawn more attention and more research. In this regard, Yang et al. [14], conducted an industrial survey related to the reliability of power electronic converters, where 31% of those interviewed classified PSDs as the "most fragile component". In another study [10], it was reported that PSD related failures, constitute 38% of the failures happening within Variable Speed Drives (VSDs), while according to Wolfgang [8], 34% of power-electronic systems' failures are attributed to failures occurring within PSDs.

Insulated Gate Bipolar Transistors (IGBTs) are PSDs which combine the low-on-state capabilities of a Bipolar Junction Transistor (BJT) (at increased breakdown voltage levels), with the facilitated input voltage control of a MOSFET. These characteristics, in conjunction with the enhanced switching capabilities, promoted the employment of the IGBT, in various power electronic systems, thus becoming one of the most widely used PSDs. This is evidenced in the same study conducted by Yang et al. [10], where it was reported by those interviewed, that the IGBT is the most utilized PSD in industrial applications. During their lifetime, PSDs and hence IGBTs, can be influenced by many degradation and failure mechanisms, which can be divided into two categories: semiconductor (die) related failures and package related failures. These can be triggered by various causes, such as harsh environmental conditions, electrical overstresses, chemical contamination, electromagnetic (EM) radiation, cosmic rays, or through regular usage leading to device's ageing. The construction of an IGBT involves multiple chemical, electrical, and mechanical processes and hence the employment of various materials. Thus, the IGBT's sub-structures can be prone to multiple failure mechanisms which

can lead to the general IGBT failure. Ciappa [73], provided an important study in relation to IGBT failures namely, bond wire fatigue, substrate cracking, interconnections corrosion and solder voiding. Another important study in this regard, was the one conducted by Busca et al. [74]. This study analyzed IGBT failing mechanisms associated with bond wire lift-off, solder voiding and bond wire cracking due to non-uniform thermal expansion coefficients.

1.2 Research Scope

A failure precursor is an event (or series of events) that is indicative of a looming failure. The identification of failure precursors and the monitoring of their extent of deviation, from the expected normal operation, can contribute to establish the health state of a device or a system, and hence determine lifetime parameters such as the Remaining Useful Life (RUL) or the Mean Time to Failure (MTTF). Failure precursor parameters can be identified by performing Failure Modes and Effects Analysis (FMEA). Moreover, PSDs' manufacturers and systems' engineers, perform accelerated ageing procedures, hence inflicting controlled degradation that is normally inflicted over a prolonged period. Throughout accelerated ageing procedures, the device or system, is characterized to identify those parameters that are manifesting a departure, from the normal operation. Eventually these parameters are utilized to diagnose degradation, by implementing prognostic algorithms, with the aim of predicting when the device or system will no longer perform its intended functionality, hence issuing important alerts and preventing catastrophic failures.

There are different studies in literature, which deal with different IGBT's failure precursors, where the latter include both mechanical and electrical parameters. Yang et al. [75], conducted a study which delved in diagnosis and prognosis methods to determine the health state of the IGBT. Patil et al. [81] conducted a thorough FMEA of IGBT related failures, correlating failures mechanisms, to failure causes, modes, and failure area within the IGBT, while identifying corresponding failure precursors. A more complete and updated review of the IGBT failure mechanisms was conducted by Abuelnaga et al. [67]. This study short listed the different failure mecahnisms and analysis, and different test setups to perform accelerated controlled degradation. Moreover, it reviewed the different diagnostic IGBT parameters indicating failure, and the corresponding lifetime modelling found in literature to determine the IGBT's health state.

Consulted literature showed that even though there are different studies which deal with the identification of IGBT's failure precursors and the corresponding prognostic techniques, there are limited studies where a particular degradation or failure mechanism is thoroughly studied vis-à-vis the changes experienced by the different IGBT's parameters, hence establishing the physical electronic changes happening within the IGBT, and eventually correlating the impacts of the manifested degradation with the IGBT's operation.

This particularly pertains to the field of EM compatibility and interference (EMC/EMI), which is a fundamental aspect in any electronic system design, especially in power electronics. In this regard, an interesting research pursuit was identified to systematically investigate the impacts on the EM disturbances generated by power electronic systems, when utilizing an aged IGBT. An equally interesting research pursuit was to establish, if the measured EM emissions of a power electronic system, can be exploited to establish the degradation state of any employed IGBT/s within that system. Both approaches rely on establishing a reliable and measurable correlation between the specific IGBT degradation mechanism and the EM conducted disturbances. Limited studies were encountered in literature which tried to establish this relationship, with three studies trying to establish a correlation between the IGBT degradation and EM conducted emissions [166-168], and two studies addressing this problem but from a radiated near-field point of view [179-180]. In relation to the EM conducted emissions studies, a thorough analysis will be conducted in Chapter 2, establishing that the results provided are inconclusive and hence a clear ascertainment of the correlation between the IGBT degradation and the EM conducted disturbances, could not be established.

1.3 Main Research Question and Addressed Research Paths

The presented work tried to address the current gap in knowledge, by studying the relationship between specific degradation within the IGBT (primarily the degradation of the die-attach layer and to a lesser extent contamination of the gate's dielectric oxide), the static and dynamic operation of the IGBT, and hence the consequential influence this degradation has, on the EM conducted disturbances. Thus, the presented research work attempted to address the following research paths:

1. Establish the most adequate accelerated ageing strategy, to produce specific IGBT degradation mechanisms reliably and controllably (in this case die-attach degradation

and gate's dielectric oxide contamination, which is the introduction of charge carriers within the dielectric structure).

2. Investigate the influence of the inflicted controlled degradation on the IGBT's static parameters
3. Investigate the influence of the inflicted controlled degradation on the IGBT's dynamic parameters and on the IGBT's switching transients, due to the importance of the latter on the EM conducted disturbances.
4. Investigate the influence of the inflicted controlled degradation on the physical electronics of the IGBT, hence attempting to explain the fundamental physical reasons why changes are manifesting in the IGBT's static and switching parameters and hence in the switching transients.
5. Investigate the impacts on the EM conducted disturbances of a power electronic circuit, which utilizes an IGBT that manifests the described specific degradation produced by the implemented accelerated ageing procedure.
6. Investigate if the EM conducted emissions of a power electronic circuit can be utilized, to provide insight on the degradation severity of the IGBT's metallization layer (more specifically the IGBT's die-attach)

1.4 Research Objectives and Methodology

The following list provides the main research objectives. Moreover, it provides a brief description of the methodology utilized to attain each objective.

1. Identify established failure mechanisms, failure causes and failure locations occurring within the IGBT. This objective was achieved by going through a detailed literature review and conducting a thorough FMEA analysis in this regard.

2. Identify the state-of-the-art IGBT's accelerated ageing systems and understand thoroughly the corresponding accelerated ageing strategy and procedure. This was achieved by conducting a detailed literature review of such systems and by performing a comparative analysis of the capabilities of each system.

3. Identify established IGBT's failure precursors, and understanding the limitations of their use within prognostics, while providing an insight on implemented lifetime modelling and prognostic techniques. This was achieved by conducting a detailed

literature in this regard, understanding the limitations of the identified failure precursors and the methods how these can be effectively implemented within a prognostic technique to determine the health state of the IGBT.

4. Develop an accelerated ageing technique to inflict controlled degradation within the IGBT's metallization layer, primarily the die-attach. This was achieved by developing a Power Cycling Ageing System (PCAS), implementing an accelerated ageing strategy of the constant case-temperature peak-to-peak fluctuation ($T_{C\_PK\text{-}PK}$) type, where the IGBT's case temperature (T_C) and consequentially the junction temperature (T_J) was elevated well beyond the maximum junction temperature (T_{J_MAX}) and maintained oscillating around a pre-established elevated case temperature (T_C) until the IGBT latches-up.

5. Conduct a mechanical analysis of the integrity of the IGBT's die-attach. This was achieved by conducting a detailed X-Ray analysis of the die-attach, hence determining the inflicted amount of voiding, and melting, within this metallization layer before, during, and after the implemented accelerated ageing strategy.

6. Determine the IGBT's static parameters changes, manifesting due to the implemented accelerated ageing strategy, while isolating as much as possible the influence of external elements such as environmental conditions. This was achieved by designing and developing an IGBT's static parameters characterization system.

7. Determine the IGBT's switching parameters and the corresponding switching transients' changes, manifesting due to the implemented accelerated ageing strategy. Again, the influence of external sources such as the environmental conditions, needs to be minimized when conducting these measurements. This was achieved by designing and developing an IGBT's Switching Transients' Characterization System (STCS), based on the Double-Pulse technique.

8. Provide an insight on the influence of the physical electronics and parasitic elements of the IGBT on the switching transients, when the IGBT is new. This understanding is to be extended to include the changes in the switching transients due to inflicted

degradation. This was achieved by reviewing different IGBT switching transients' models. The conducted analysis primarily focused on two models, the Jin et al. [215] model, which describes the IGBT's switching transients through piecewise linear equations, derived from the analysis of an equivalent IGBT switching circuit, and the Rajapaske et al. [213] model, which describes the IGBT's switching transients through piecewise non-linear equations, obtained through the transients' characteristic variation with time, for the different turn-on and turn-off phases. Both models were rederived and compared to the measured IGBT switching transients, which provided an insight on the influence of the physical electronics and parasitic elements on the characteristics of these transients when the IGBT is in a healthy state. Moreover, these models were modified by either introducing variations in the model's parasitic elements' values or providing new model equations, to account for the measured switching transients' changes due to the implemented accelerated ageing.

9. The final objective was to determine if the inflicted controlled IGBT's degradation, was influencing the EM conducted disturbances of a power electronic system utilizing this IGBT, while ensuring that the obtained measurements are minimally influenced by external sources such as environmental conditions. This assures a reliable and confident correlation between the IGBT's inflicted degradation, and the EM conducted emissions, and hence the feasibility of utilizing the latter as a failure precursor. This was achieved by designing and developing an EM conducted emissions measurement setup which was based on the Double Pulse STCS system.

1.5 Research Main Findings

This research established that the implemented accelerated ageing strategy, which inflicted a controlled degradation of the die-attach and contamination of the gate's dielectric oxide, influenced a progressive change in various IGBT's static and switching parameters. Moreover, this research established that the implemented ageing strategy was significantly slowing the IGBT switching performance. An interesting outcome was, that this switching slowdown was to a certain extent exclusively manifesting during the IGBT's turn-off, with the turn-on being minimally impacted. The switching transients' modelling established that this lengthier turn-off was primarily manifesting in the collector-current (I_C) transient, which predominantly manifested an intensified and prolonged presence of the "tail current", where the latter occurs only during the collector current (I_C) turn-off. This phenomenon was attributed to an increase

in the IGBT's junction temperature (T_J) even though the case temperature (T_C) was maintained at room temperature. This was a direct consequence of a degraded die-attach which hindered the heat flow from the junction to the case. Moreover, the experienced increase in the IGBT's junction temperature (T_J) and the gate's oxide contamination, impacted the parasitic Miller capacitance (C_{CG}), contributing to an extended Miller Plateau[1] during turn-off which impacted further the IGBT's turn-off slowdown.

Finally, the performed EM conducted emissions measurements, showed that, an IGBT manifesting a predominant degradation in the die-attach, leading to worsened heat dissipation capabilities, with the contribution of the gate oxide contamination, yield to a decrease in the EM conducted disturbances of a power electronic system employing such IGBT, when compared to the EM conducted disturbances of the same system when employing the same IGBT, but in a healthy state. This confirmed that there is a reliable correlation between the inflicted degradation produced by the implemented accelerated ageing strategy and the EM conducted emissions, and hence the latter can be employed within prognostic techniques to determine the degradation severity of the IGBT.

1.6 Research Outline

- This chapter proceeds by providing a general introduction to PSDs, and some general information about specific PSDs whose structure is in some way related to the structure of the IGBT, while providing some generic information about the IGBT itself.

- Chapter 2 provides a detailed literature review in relation to the IGBTs' failure mechanisms, including the physics of failure, degradation characterization, accelerated ageing, ageing prognostics, and RUL estimation techniques. Moreover, this chapter provides a detailed FMEA of the IGBT's failure mechanisms, failure causes and failure locations.

- Chapter 3 provides the details of the developed IGBT's PCAS. It reports the identified requirements for the proposed system as well as the corresponding design and implementation details of the required hardware and software.

[1] *Miller Plateau is the gate-emitter voltage (V_{GE}) during commutation, when the gate-emitter voltage rate of change (dV_{GE}/dt) is at a minimum.*

Successively, this chapter provides the details of the implemented IGBT accelerated ageing procedure, highlighting the corresponding operational procedure and results. Eventually it goes through the mechanical characterization of the inflicted IGBT degradation, through the analysis of the conducted X-Ray inspection. This leads to the characterization of the IGBT and IGBT's internal diode's, static electrical parameters, and their evolution with the inflicted degradation. This is conducted by describing the design and implementation of the static electrical parameters' characterization testbed, including both hardware and software. Finally, the corresponding characterization results are presented and discussed.

- Chapter 4 reports the design and development of the IGBT's STCS, based on the Double-Pulse technique. It provides the details of the STCS's developed software and hardware, along with the integration of commercial instrumentation, to measure the IGBT's and internal IGBT diode's switching transients, and hence the corresponding switching parameters. Finally, the measured changes manifested by these parameters and the switching transients, are presented, and discussed, in relation to the inflicted degradation.

- Chapter 5 presents the analysis and corresponding modelling of the IGBT's switching transients when new, by principally considering two models: a piece-wise linear model, and a piece-wise non-linear model. A thorough analysis accompanied by the complete derivation of all the mathematical functions utilized by each model, are presented here. Successively, the comparison of the modelled switching transients and the measured transients is provided. Moreover, this chapter presents the introduced changes in the models' parameters and the introduced mathematical functions, to include the measured ageing effects. Again, a comparison is provided between the IGBT's modelled aged transients and measured aged transients. The dependency of the switching transients (when new and aged), on the physical electronics as well as on the various factors such as switching voltage, switching current, reverse recovery of the freewheeling diode, stray inductance and parasitic capacitances are extensively discussed in this chapter.

- Chapter 6 presents the details of the experimental setup and procedure to measure the EM Conducted emissions, by taking into consideration the available standards and measurement practices. It provides the details of the measurement procedure which

involved the acquisition of both the IGBT's individual signals' frequency domain spectra, and the EM conducted emissions for the CISPR16-1-1 A and B bands. The comparative analysis of the individual signals' frequency domain and the EM conducted emissions, is provided here. Finally, this chapter provides a detailed analysis of the spectral results obtained, and hence the correlation between the spectral changes happening exclusively to the IGBT and the changes of the measured EM conducted disturbances, providing insights of how the EM conducted emissions were impacted by the IGBT's degradation, and if the measured changes in the EM conducted disturbances can be utilized to determine the health state of the IGBT.

- Chapter 7 presents the conclusions of this work and the corresponding contributions to knowledge. Moreover, it provides a way forward, where further research work can be conducted in relation to the research work presented here.

1.7 Introduction to Power Semiconductor Devices (PSDs)

The PSD is a semiconductor device mainly used as a switch or rectifier in power electronics applications. Even though there are applications which utilize the linear operation of PSDs, most PSDs are usually employed in "commutation mode" that is either on or off and hence throughout the years their design was mainly optimized for this usage. The first power semiconductor device was the Hall's power diode introduced in 1952. It had a current handling and breakdown voltage capabilities of 35A and 200V respectively and utilized germanium as semiconductor material [15]. Thyristors began to appear in the late 1950s. These devices increased the breakdown voltage and carrying current capabilities over the power diode. Their biggest limitation was in switching circuits, due to "latch-on" of the thyristor once in the conducting state. This offered a major limitation, since thyristors could not be switched off by external control, but rather had to be switched off passively by disconnecting power. Gate turn-off thyristors (GTO) introduced in the 1960s, overcame this limitation, since turn on and turn off was controlled by an applied signal. The first power Bipolar Junction Transistor (BJT) was introduced in the late 1960s. Due to the advancement of metal oxide semiconductor field effect transistor (MOSFET) technology utilized in integrated circuits, a 400V/25A power MOSFET was introduced in the 1970s by International Rectifier [15]. Power MOSFETs can be employed at switching frequencies which are higher than the BJTs but are inferior in terms of power handling capabilities. The hybrid of the power BJT and the power MOSFET was introduced in the 1980s and came to be known as the IGBT.

1.7.1 Power Devices Classification

Power devices can be classified into different categories. The most obvious classification is based on the terminals of the device (if the device is a two or three terminal device). In a two-terminal device, such as a power diode, the state of the device depends on the applied power (forward or reversed biased). In a three-terminal device the state does not depend only on the applied power but also on the applied control signal.

Another classification which has direct impact on the device performance, is if the device is a majority or a minority carrier device. A majority carrier device utilizes charge carriers of one type only (either holes or electrons) Typical examples of such devices include Schottky diodes and MOSFETs. A minority carrier device utilizes both majority and minority carriers (both holes and electrons) [1]. Typical examples of such devices include the IGBT, BJT and Thyristors. A majority carrier device has faster switched capabilities, while minority carrier devices have better on-state capabilities (lower collector-emitter on-state voltage (V_{CE_ON}) in case of BJTs and IGBTs and lower on-state drain to source resistance (R_{DS_ON}) for FET devices). The majority/minority carrier PSD classification can be extended to four technological categories: Bipolar, MOS, MOS-Bipolar and Junction Control as illustrated in Figure 1.1.

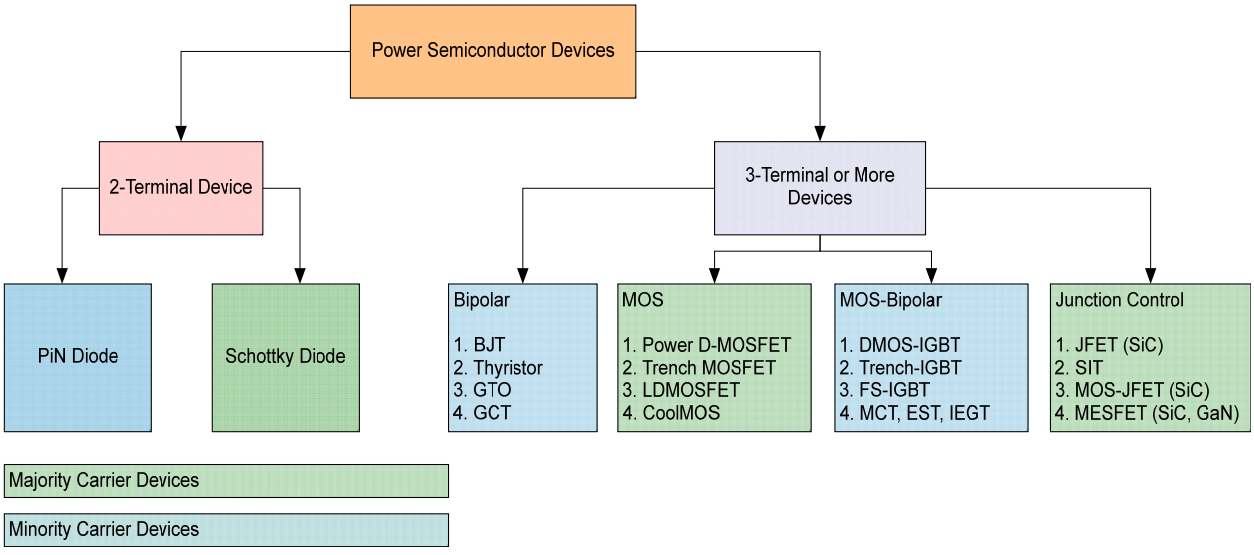


Figure 1.1 - Classification of Power Semiconductor Devices

1.8 Thyristors

Thyristors, or silicon-controlled rectifiers (SCRs) have been the industry's bulk power conversion and control device. The area of power electronics has been developed mainly due the introduction of this device [1]. The generic thyristor device includes within its family the following set of devices: the SCR, the triode for alternating current (TRIAC), Gate Turn-Off Thyristor (GTO), Integrated Gate Commuted Thyristor (IGCT) and MOS-controlled thyristor MCT. Thyristors are utilized in a variety of applications, including power-switching circuits, replacements to relays, inverter devices, motor speed control devices, phase-control circuits, light dimming circuits etc. Traditionally, thyristors could only be switched off through the removal or reversal of current, making their application limited especially in direct current (DC) circuits. Newer generation thyristors provide a gate signal from which the device can be turned on or off. The GTO is this kind of device. Unlike the BJT, the thyristor is not a proportional device and can only be switched fully on or off, making this device unsuitable for power amplification but useful only as a switch.

1.8.1 Thyristors Physical Structure & Operation

The thyristor is a three terminal, four layered, semiconductor device. The physical structure consists of four alternating N-type and P-type material. The main power terminals are the anode and cathode, with a control terminal called the gate. Figure 1.2 illustrates the layout structure and equivalent circuit of the thyristor. The operation of the thyristor can be modelled as two coupled PNP and NPN bipolar transistor, causing a self-latching action.

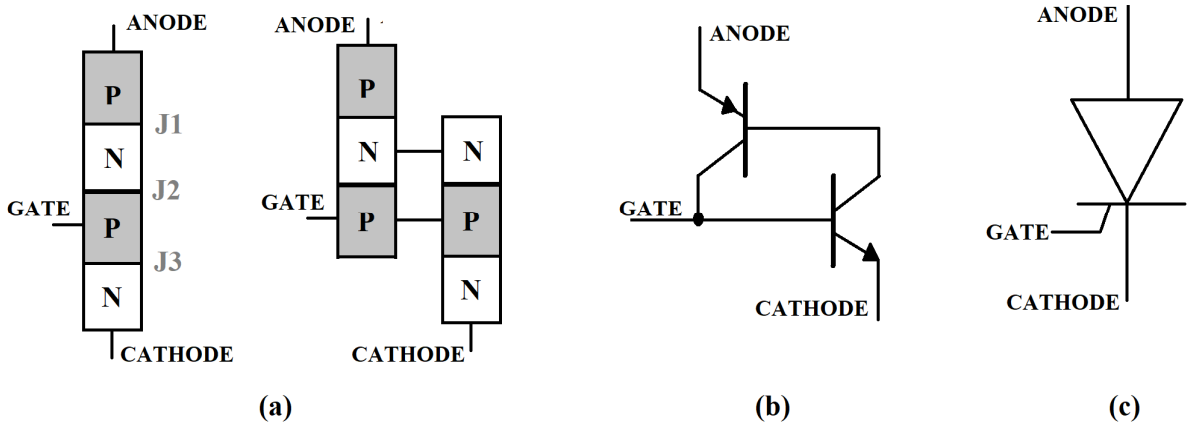


Figure 1.2 - Thyristor's Layout Structure and Equivalent Circuit (a) layout structure (b) equivalent circuit (c) symbol

Thyristors have three states of operation:

1. *Reverse Blocking* – The anode is at a lower potential than the cathode
2. *Forward Blocking* – The anode is at a higher potential than the cathode, but the gate terminal has not been triggered.
3. *Forward Conducting* – The device is triggered in conduction through the gate and will remain conducting until the forward current is dropped below a threshold current value known as the "holding current".

As illustrated in Figure 1.2, the thyristor has three p-n junctions. When the anode is at a higher potential than the cathode and no potential at the gate, then J1and J3 are forward biased, but J2 is reversed biased. If a positive voltage in relation to the cathode is applied at the gate, J2 will be reversed biased, and the thyristor will start to conduct. It is important to note that the thyristor can be made to conduct in another manner, by increasing the potential on the anode beyond the breakdown voltage of junction J2 which is effectively the breakdown voltage of the thyristor (V_{BO}). In this scenario J2 will go into avalanche breakdown and the thyristor will start to conduct. Through the gate voltage, the breakdown of J2 occurs at a lower anode-cathode voltage (V_{AK}) enabling the thyristor to be switched in the conduction state quicker. Once avalanche breakdown has been triggered the thyristor will continue to conduct independently from the gate voltage and can only be stopped either by removing the anode-cathode forward voltage or by decreasing the forward current below the holding current of the device. Hence the gate control signal of a thyristor is a power pulse mainly characterized by the gate trigger voltage (V_{GT}) and gate trigger current (I_{GT}). Furthermore, the gate is characterized by the minimum gate charge (Q_G) required to trigger the thyristor into conduction. Hence Q_G effectively translates in the specification of the pulse width required to trigger the thyristor [3].

Once a thyristor has been switched on by applying a gate pulse, the device will remain latched on and does not require the gate signal to remain on, providing that the anode current has exceeded the latching current (I_L). The device will remain in the on-state until the forward current drops below the holding current (I_H). The thyristor can be switched off, if the anode is set at lower potential than the cathode, a method known a natural or line commutation. Another switch-off technique involves the utilization of a second thyristor discharging a capacitor in the cathode of the first thyristor, a method called forced commutation.

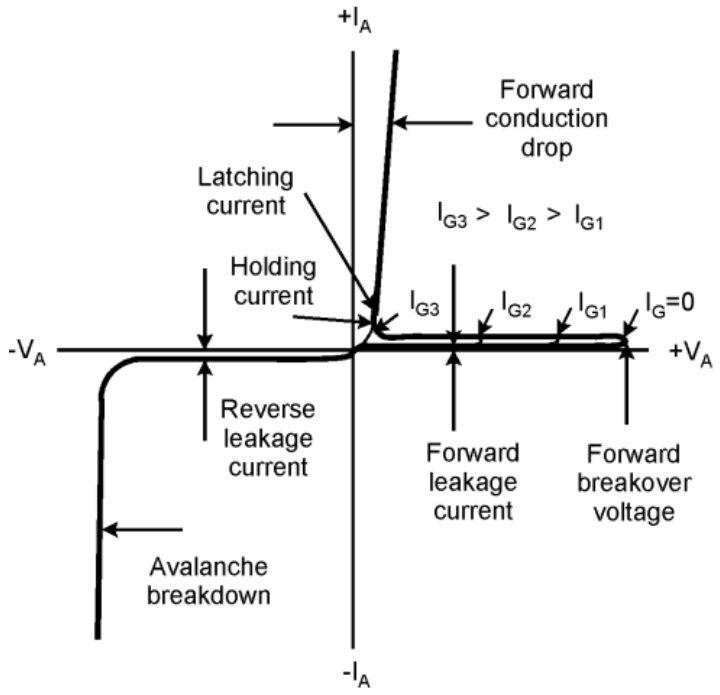


Figure 1.3 – Thyristor's Volt-Ampere Characteristics [1]

Thyristors require a minimum time-delay before the anode can again be positively biased after switch-off. If the anode is to be positively biased within this time, the free charge carriers (holes/electrons) which have not yet recombined, will cause the thyristor to self-trigger. This delay is referred as the commutation turn off time (t_Q). Hence improving the switching speed of a thyristor inherently involves accelerating the charge recombination process after switch-off. Hence fast thyristors utilize the diffusion of heavy metal ions materials such as gold or platinum which serve as charge combination centers. Other recent techniques involve ion implantation technique or electro irradiation technique [3]. These latter techniques provide better doping control and can be introduced at a later stage in silicon fabrication.

1.8.2 Thyristor Failure Modes

Like other PSDs, thyristor manufacturers specify a safe operating area, confined by acceptable voltage levels, current levels, and operating temperature. The maximum permissible gate power is also specified (P_G), and it is defined as the maximum permissible energy contained within the gate trigger pulse. Furthermore, thyristors have specific failure modes [2]:

- *dI/dt Failure* - This is related to the rate of increase of on-state current after the thyristor has been triggered. If this rate of increase is greater than the supported current spreading speed of the active conduction area, the device will be damaged

- *Spurious Switching dV/dt* – This is the spurious switch-on of the thyristor without any gate trigger, caused by a high rate of increase of the anode-to-cathode voltage.
- *Forced Commutation Failure* – During forced commutation reverse current is driven through the cathode to switch-off the thyristor. This reverse recovery current can cause a high-voltage drop in the cathode region, exceeding the reverse breakdown voltage of the gate-cathode diode junction.

1.9 Power BJT

The Power BJT was the first power semiconductor device to allow full control on the turn-on and turn-off operations, simplifying the design of power electronic systems which utilized thyristors. Other power transistors followed many of which are superior compared to the BJT, eventually leading to their complete replacement. However, the BJT was the first device closely to approximate an ideal fully controlled switch. Other power transistors have characteristics which are like the characteristics of the BJT (even though the physical electronic characteristics might be different). The power BJT is a minority carrier, current controlled device, however the operating characteristics differ significantly from its low power counterpart. This is mainly due to the large blocking voltage and high current carrying requirements during the "OFF" and "ON" states respectively.

1.9.1 Power BJT's Physical Structure

Power BJTs have vertically oriented alternating layers of n and p-type semiconductor materials as illustrated in Figure 1.4. Vertical structure is a preferred construction technique since it maximizes the cross-sectional area through which current can flow, especially during turn-on operations, hence minimizing the on-state resistance and consequent power-loss. The emitter doping density is much higher than the base, moreover the thickness of the base is made as small as possible. These two techniques ensure a large enough forward current gain (β), consequently reducing as much as possible the base drive current. To sustain large voltage stand-offs a lightly doped collector-drift region is introduced in between the moderately doped base region and the heavily doped collector region. The same technique is utilized in power diodes. The purpose of the collector-drift region is to absorb the depletion layer of the reversed biased collector-base (C-B) junction during Cutoff or turn-off operation.

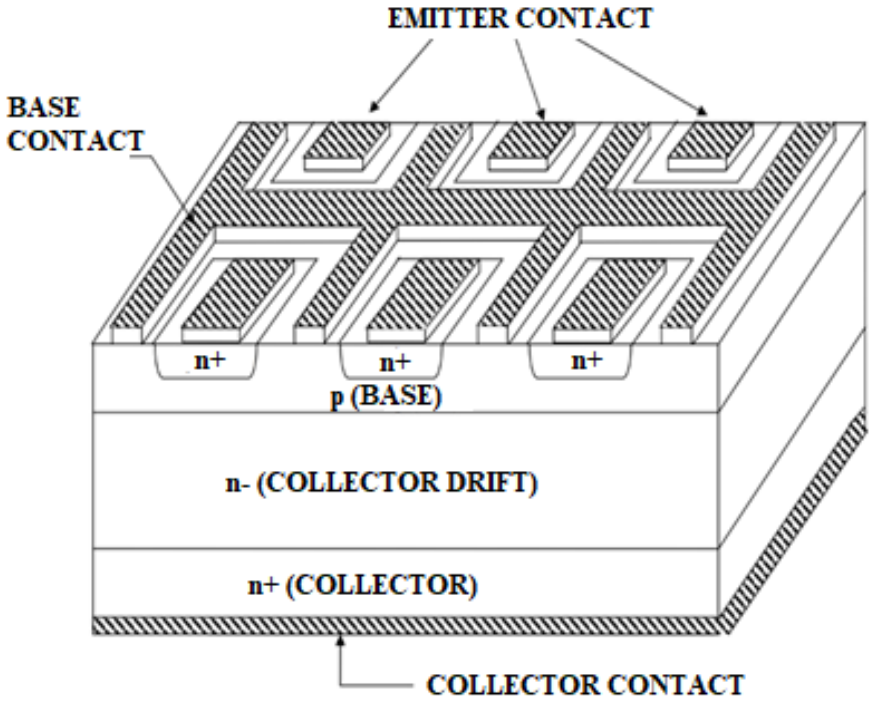


Figure 1.4 - Vertical Power BJT Structure [10]

The thickness of n-drift region determines the reverse breakdown voltage of the collector-base junction and hence determines the primary breakdown limit. Since this region is lightly doped it will add significant ohmic resistance when the collector-base junction is forward biased during turn-on or Saturation mode. Since the base region is moderately doped compared to the heavily doped collector region, the depletion region penetrates considerably into the base. Hence the base of the power BJT cannot be made as small as a low power transistor. The larger base has an adverse effect on the forward current gain (β) of a power BJT which typically varies between 5 to 20. Power BJTs have their emitters and bases interleaved as fingers. This is necessary to prevent current crowding which is a precursor to second breakdown. Furthermore, multiple emitter structure reduces parasitic ohmic resistance in the base's current path [3].

1.9.2 Power BJT Characteristics

A BJT transistor is formed by adding a 2nd p- or n- region to a p-n junction diode. A BJT has 2 junctions, the collector-base junction, and the base-emitter junction. Figure 1.5 illustrates the V-I characteristics of a power BJT. Like a small signal BJT, it exhibits the "Cut-Off", "Active" and "Saturation Region" of operation in its output characteristics. However, it exhibits an additional intermediary operating region known as the "Quasi-Saturation" region. This is a consequence of the lightly doped collector drift region where the collector-base junction

supports a higher reverse bias as described earlier. Moreover, Figure 1.5 illustrates the operational constraints of a power BJT namely the "Total Power Dissipation Limit" or "Maximum Junction Temperature Limit", the "Primary Breakdown Limit", the "Secondary Breakdown Limit" and the "Maximum Current Limit", constituting the limits of the safe operating area (SOA).

A breakdown voltage is defined as the absolute maximum voltage between two terminals with the third terminal open, shorted, or biased in either forward or reverse directions. At breakdown the voltage remains relatively constant, while the current rises rapidly. Power BJT manufacturers quote the following breakdown voltages:

- **BV_{EBO}** : The maximum voltage between the emitter terminal and the base terminal with the collector terminal open circuited.
- **BV_{CBO}** : The maximum voltage between the collector terminal and the base terminal with the emitter terminal open circuited.
- **BV_{CEO}** : The maximum voltage between the collector terminal and the emitter terminal with the base terminal open circuited.
- **BV_{SUS}** is the limit for primary breakdown and is the maximum collector-emitter voltage that can be sustained across the transistor when it is carrying high collector current. BV_{SUS} is lower than **BV_{CEO}** and **BV_{CBO}** both of which measure the transistor's voltage standoff capability when the base current is zero or below zero.

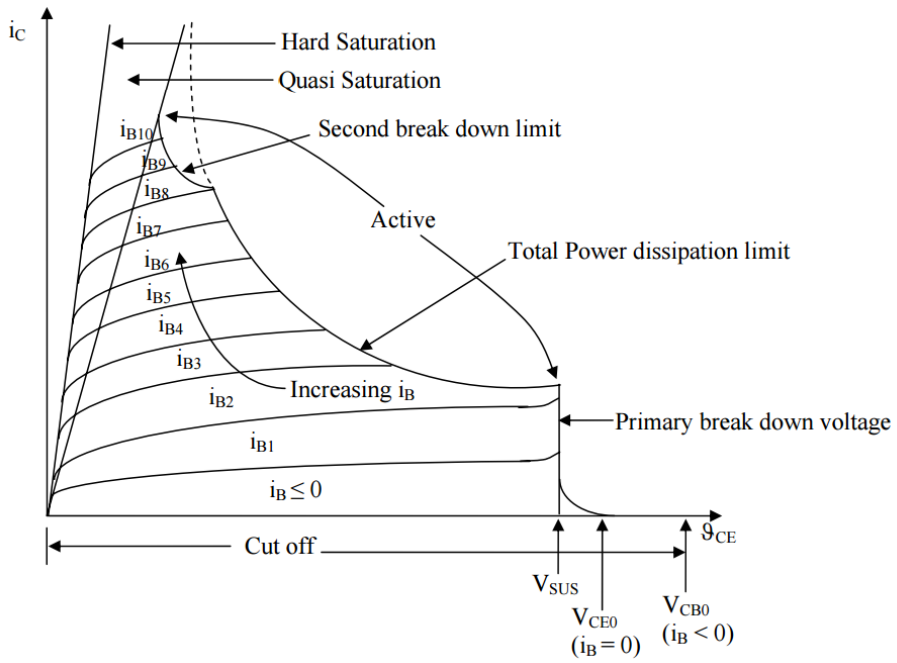


Figure 1.5 - Output V-I Characteristics of a Power BJT [11]

Increasing the voltage above the maximum rated collector-emitter voltage ($V_{CE(SUS)}$) the operation initially remains correct. The effect is that it will increase the reverse voltage on the collector-base junction and thus increasing the width of the depletion region of this junction. This will result in a decrease of the effective base width. This will impact the BJT's reverse saturation current (I_S) which will manifest an increase, contributing to an increase in the the collector current (I_C) too. This will influence an increase in the forward current gain (β). This is called the Early Effect [1]. If the collector-emitter voltage (V_{CE}) is increased further, above the maximum rated collector-emitter voltage ($V_{CE(SUS)}$), the base width can be reduced to zero and Punch-Through occurs. Even before Punch-Through occurs, an avalanche breakdown may occur due to the high electrical field. When this occurs, primary breakdown is said to have occurred. The avalanche breakdown occurs due to the collector-base junction being reversed biased and experiencing large electric fields. The breakdown of the collector-base junction is not destructive if the power dissipation in the device is kept within safe limits. The emitter-base junction can also experience breakdown in an avalanche manner, if reversed based and experiencing large electric fields. The emitter-base junction breaks at a voltage (BV_{EBO}) much smaller than BV_{CBO}. This breakdown is destructive in the sense that the forward current gain (β) of the transistor is permanently reduced.

Another breakdown mechanism of a power BJT is the secondary breakdown. It appears on the output characteristics of the power BJT as a precipitous drop in the collector-emitter voltage (V_{CE}) at large collector currents (I_C). As the collector voltage (V_C) drops, there will be a significant increase in the collector current (I_C) and hence a substantial increase in power dissipation. The problem arises since the power dissipation is not uniformly spread over the entire volume of the device but concentrated in highly localized regions. This is because the diffusion process does not produce a clean out, homogenous junction. This leads to the formation of hot spots which can eventually melt and recrystallize the silicon, resulting in the device's destruction.

Hence the power BJT can be viewed as sectioned parallel BJTs, depending on the local widths of the base. The BJT section with the smallest base, has the largest forward current gain (β) and hence takes the most collector-current (I_C), leading to the largest power dissipation and hence largest heat generation. The forward current gain (β) is proportional to temperature, which in-turn increases the collector-current (I_C) further. If uncontrolled, this will lead to

thermal runaway and device destruction. The secondary breakdown limit on the SOA, is junction temperature (T_J) and hence case temperature (T_C) dependent, and must be derated accordingly for operational case temperatures (T_C), higher than the rated case temperature (T_{C_RATED})

Power BJTs have two other operational limits. One of the limits is the "Maximum Allowable Current Limit" (I_{CMAX}). If this current is exceeded on a continuous basis (continuous current) it can lead to the melting and eventual rupture of the bonding-wires that bond the BJT's semiconductor to the package. The "Maximum Power Dissipation Limit", is the locus of points on the output V-I characteristics for which the product $V_{CE}I_C$, corresponds to the maximum power dissipation (P_{DMAX}). This limit is directly influenced by the maximum junction temperature (T_{JMAX}) which must not be exceeded for reliable operation. The BJT's case-temperature (T_C) is linked to the junction temperature (T_J) via the junction-to-case thermal impedance (θ_{JC}). Hence power BJTs' manufacturers specify a maximum power dissipation at a rated case temperature (T_{C_RATED}). For case temperatures (T_C) greater than the rated case temperature (T_{C_RATED}), power derating curves must be used to achieve the allowable value of maximum power dissipation (P_{DMAX}), hence obtaining a lower "Maximum Power Dissipation" boundary on the SOA. It is important to note that this power operating point can be allowed to move for some time outside the "Maximum Power Dissipation Limit", but the average power dissipation must not exceed this boundary [1].

1.10 Power MOSFETs

Power MOSFETs were first developed in the 1970s [15] and soon replaced Power BJTs. Unlike BJTs which are current controlled, these devices are voltage controlled and hence require a less complicated gate drive circuit. Research and development in MOSFETs led to improvements in the performance of Power MOSFETs. Today it is possible to fabricate MOSFETs with breakdown voltages as high as 600V and ON-State-Resistance (R_{DS_ON}) of 80mΩ [1]. Reduced switching and conduction losses and improved voltage stand-off capabilities led to the improved performance of power electronic circuits such as switch-mode power supplies. Power MOSFETs today are commonly utilized for high switching frequency application (up to a few MHz) and stand-off voltages less than 200V. Power MOSFETs do not suffer from secondary breakdown like power BJTs. On the other side power MOSFETs suffer from electrostatic discharge (ESD) hazards and are more likely to be permanently damaged under short-circuit fault conditions.

1.10.1 Depletion vs Enhancement Type MOSFETs

MOSFET devices can be divided into two main types: depletion MOSFETs and enhancement MOSFETs. An n-channel depletion-type MOSFET structure is shown in Figure 1.6(a). The depletion MOSFET is formed with a p-type silicon substrate, two heavily doped n-type silicon structures and a diffused channel in between. The gate is isolated from the n-channel by a thin oxide layer. The substrate section is generally connected to the source. The gate to source voltage (V_{GS}) can be either positive or negative. A negative gate to source voltage (V_{GS}) will cause some of the electrons in the n-channel sections to be repelled and hence a depletion region will be formed. This will cause the n-channel to narrow and hence causing the resistance between the drain to source to increase. If the gate to source voltage (V_{GS}) is driven more negative, the channel will become completely depleted offering a large value of resistance, hence allowing no current to flow from drain to source. The value of the gate to source voltage (V_{GS}) which leads to the complete depletion of the channel is referred as the pinch-off voltage (V_P). If the gate to source voltage (V_{GS}) is driven positive, the channel becomes wider hence allowing more current to flow from drain to source [1]. For an n-channel enhancement MOSFET, there is no physical n-type section acting as channel, as illustrated in Figure 1.6(b). When the gate to source voltage (V_{GS}) is driven positive, the induced voltage will attract electrons from the p-substrate. The attracted electrons will accumulate under the oxide. When the gate to source voltage (V_{GS}) exceeds the threshold voltage (V_{THRES}), enough electrons will accumulate under the oxide section that permits the creation of a virtual n-channel hence permitting conduction from drain to source. Hence a depletion MOSFET at V_{GS} = 0V will remain on, whilst the enhancement MOSFET will be off when V_{GS} = 0V. When considering this fact and the fact that the main power application of MOSFETs is that of a switch, power MOSFETs are mainly of, the enhancement type [1].

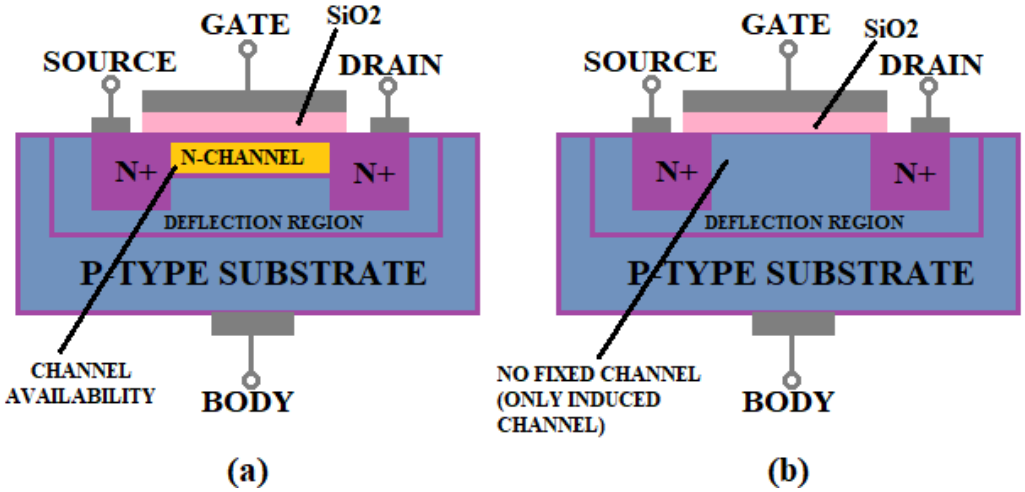


Figure 1.6 - N-Channel (a) depletion MOSFET (b) enhancement MOSFET

1.10.2 Power MOSFETS Physical Structure & Operation

The most common power MOSFET structure, is the Vertical Diffused MOS (VDMOS also known as Double-Diffused MOS DMOS) shown in Figure 1.7. It highlights the vertical structure of the device leading to a predominant vertical current when the device is in the on-state. The VDMOS structure requires the manufacturing of P-wells (P+ sections). These wells are obtained by a diffusion process. The process involves a double diffusion technique to get both P^+ and N^+ regions. This explains the double-diffused terminology. Figure 1.7 illustrates a plain VDMOS cell. The actual size of these cells varies from micrometers to tens of micrometers depending on the power application. A power MOSFET will have thousands of these cells. In a VDMOS structure the breakdown voltage is a function of the doping level and the thickness of N^- substrate layer. The maximum conduction current depends upon the channel dimensions. This enables the device two simultaneously block high voltages and sustain large currents within a compact silicon volume, hence optimizing the device for switching [1]. Sufficient positive drive of the gate to source voltage (V_{GS}) will attract electrons from the N+ layer to the P+ layer, hence opening a channel close the gate. This will allow current to flow from the drain to the source. It is important to note that there is a dielectric layer (silicon oxide SiO) between the gate metal and the N+ and P+ junction. The highly doped N+ layer close to the drain acts as a buffer below the N- drift layer. This buffer will prevent the depletion layer from reaching the drain metal and minimizes the forward voltage drop during the on-state. This buffer layer makes the device asymmetric.

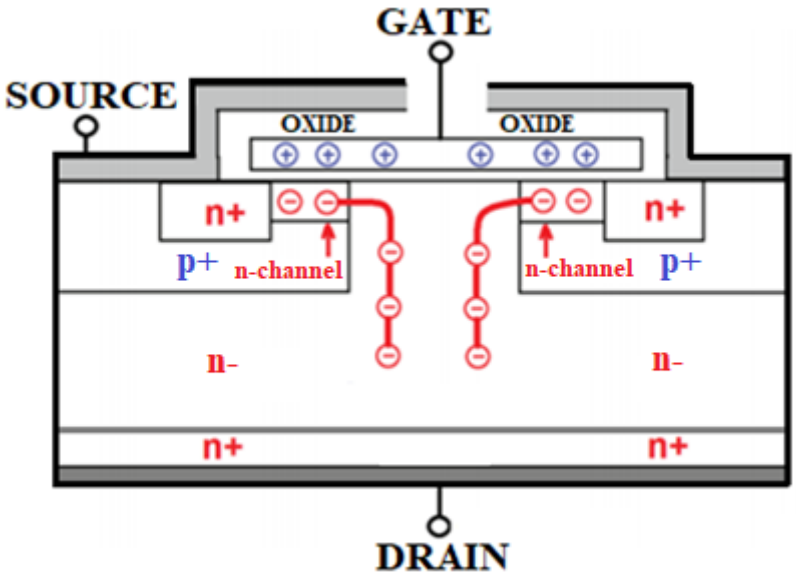


Figure 1.7 - VDMOS Cell Structure

As illustrated in Figure 1.7, in the off-state, the P+ diffusion region, N- drift region and the N+ substrate, form a structure equivalent to a PN-diode. This structure is highly non-symmetric. And hence when reversed-biased, the depletion region extends mainly in the lightly doped N- layer. As in the case of the power BJT structure, it is the N- layer that must withstand the off-state blocking voltage. During the ON-state, the N-layer has no use. Moreover, since it is lightly doped, it is resistive and acts as the main contributor to the ON-state drain to source resistance (R_{DS_ON}). Hence the thickness and the doping level parameters of the N-layer, control the contrasting R_{DS_ON} and breakdown voltage parameters. Hence power MOSFET design, is a compromise between low R_{DS_ON} contributing to low ON-state losses and high breakdown voltage contributing to better voltage stand-off capabilities [1-2].

Figure 1.7 shows that there is an intrinsic power BJT structure within the structure of the power MOSFET. The metal attached to the source terminal shorts both the N+ and P+ wells close to the source. The power MOSFET source requires only a connection to the N+ well. But if this was the case the P+ well would be left floating. This means that the intrinsic BJT has an unconnected base. Under the conditions of high drain current and some drain to source voltage, this parasitic BJT may be triggered leaving the power MOSFET without control. This failure condition is normally referred to as “latch-up” or “loss of gate control” [1]. The shorting of the P+ well to the N- source is effectively shorting the base of the parasitic BJT to its emitter, hence preventing from the parasitic BJT to be triggered. Furthermore, it creates a diode structure between the drain (cathode) and the source (anode). This diode structure is known as the bulk diode. It can be utilized as a freewheeling diode when switching inductive loads. This diode structure can handle high forward currents but has the disadvantage of large forward voltage drop.

Like other power semiconductor devices, the power MOSFET has parasitic capacitance between its terminals. Hence the main capacitance within the power MOSFET structure is the gate-to-source capacitance (C_{GS}), gate-to-drain “Miller” capacitance (C_{GD}) and drain-to-source capacitance (C_{DS}). In datasheets, these parasitic capacitances are indirectly referred by the following equivalent capacitances; C_{ISS} (input capacitance, measured with drain and source terminal shorted), C_{OSS} (output capacitance, measured with the gate and source shorted), and C_{RSS} (reverse transfer capacitance, source connected to ground) [1],[2].

$$C_{ISS} = C_{GS} + C_{GD} \quad (1.1)$$

$$C_{OSS} = C_{GD} + C_{DS} \quad (1.2)$$

$$C_{RSS} = C_{GD} \quad (1.3)$$

- *Gate to Source Capacitance (C_{GS}):* As illustrated in Figure 1.8, C_{GS} is made up of the parallel connection of C_{OXN+}, C_{OXP+} and C_{OXM}. The source N+ and P+ regions are highly doped and hence these two capacitances are considered to remain relatively constant. C_{OXM} represents the capacitance between the gate (polysilicon) and the source electrode metal, hence it is also assumed as constant. Therefore, C_{GS} value is assumed as constant and independent of the transistor's operational state.

- *Gate to Drain Capacitance (C_{GD}):* The C_{GD} capacitance is made up of the series combination of two capacitances, the first is the capacitance between the gate metal electrode, the gate oxide, and the top of N- layer. This capacitance, referred to as C_{OXD}, has a relatively constant value. The second capacitance is due to the extension of the depletion region. This occurs when the device is in the off state. Variation in the depletion region size contributes to a variable capacitance. Since this extension of the depletion region depends on the drain-to-source voltage (V_{DS}), as this latter voltage increases, this capacitance decreases.

- *Drain to Source Capacitance (C_{DS}):* Since the source metal is shorted and overlaps the P+ wells, then the source and drain terminals are separated by a PN junction. Hence C_{DS} is this PN junction capacitance. This capacitance is a non-linear capacitance.

The power MOSFETs silicon die must be connected to the external circuitry. This is achieved through wire bonding. Any wire bonding has parasitic inductances. These parasitic inductances have important effects on the device's switching speed. Any inductance will try to maintain the current constant and produce overvoltage during changes in current such as during device's switching. Hence these parasitic inductances increase switching losses. Each terminal has an associated terminal inductance [1], [2]:

- **Gate Inductance:** The gate inductance is not predominant since the gate's rate of change of current is low. It is important to note though that the gate inductance and the input capacitance of the device can produce oscillations. Devices' manufacturers tend to minimize as much as possible the gate inductance to prevent these oscillations which will result to high switching losses and device destruction.
- **Drain Inductance:** The drain inductance tends to minimize the drain voltage when the MOSFET is switched on, hence switch on losses are reduced. On the other-hand during switch off this inductance contributes to overvoltage and hence to switch-off losses.
- **Source Inductance:** The source inductance has similar effects as the drain inductance but with the added scenario that the source is both common to the input as well as the output. Hence the source inductance produces a feedback effect, making the switching last longer, thus increasing switching losses.
    - At the beginning of a fast switch-on, due to the source inductance, the voltage at the silicon die source will follow the gate voltage, hence the internal gate-to-source voltage (V_{GS}) will be maintained low thus delaying the device turn-on.
    - At the beginning of a switch-off, the voltage at the silicon die source goes negative with respect to the source lead. This leads for the internal V_{GS} to increase and hence keeping the device on, thus delaying switch-off.

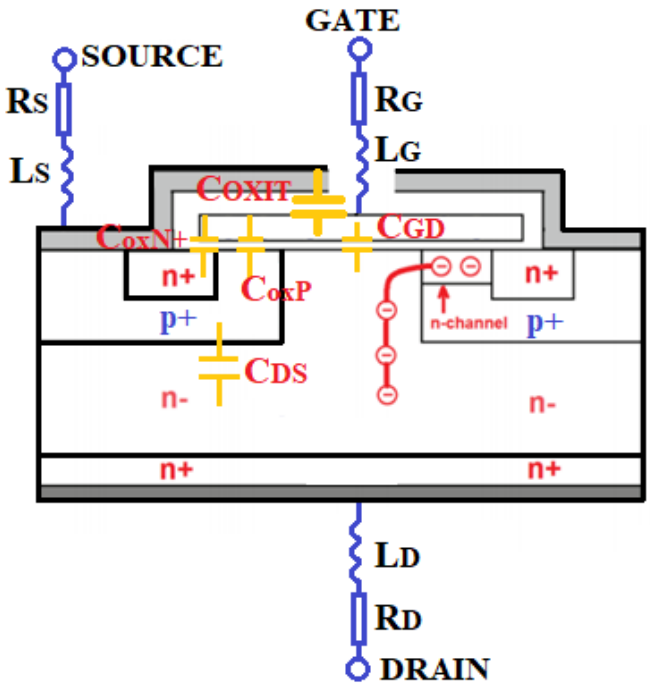


Figure 1.8 – Power MOSFET Parasitic Inductances and Capacitances [2].

1.11 Insulated Gate Bipolar Transistor (IGBTs)

The IGBT is a three-terminal power semiconductor device, utilized mainly as an electronic switch combining high efficiency and fast switching. The IGBT was introduced in the early 1980s [15], becoming a successful PSD because of its superior characteristics over other PSDs. Prior to the introduction of IGBTs, power BJTs and power FETs were mainly utilized in low to medium power and high-frequency applications, where thyristors' speed was inadequate. Power BJTs have good on-state capabilities, hence low on-state losses. On the other hand, since power BJTs are minority carrier devices, their switching capabilities are limited due to the long turn-on and especially turn-off, contributing to switching losses. Moreover, they are current controlled devices with a small forward current gain (β) due to a large base width (to optimize voltage blocking capabilities) hence leading to complex base drives. Power MOSFETs are voltage-controlled devices, having an insulated gate, which leads to a small gate current and simple gate drive requirement. Power MOSFETs are majority carrier devices with high switching capabilities and hence low switching losses. As the voltage stand-off rating of the device increases, the utilization of power MOSFETs will be limited by the on-state resistance (R_{DS_ON}). The unipolar characteristics of power MOSFETs, limit conduction when the voltage rating of the device is increased above 200V. Hence, the on-state resistance (R_{DS_ON}) increases with increasing standoff-voltage rating of the device. Furthermore, the increase in voltage rating will contribute to increase the recovery time of the body diode, leading to increased switching losses. Thus, a power device with insulated gate input and optimized on-state capability is obviously advantageous. Hence, the combined physics of a power MOSFET and power BJT, integrated in the same semiconductor region provides an improved on-state characteristics, switching characteristics and enhanced safe-operating area, simultaneously [3].

IGBTs are replacing MOSFETs in high voltage applications due to improved conduction losses, on-state voltage (V_{CE_ON}) comparable to that of power BJTs, and enhanced switching speeds. It is important to point out, that even though the turn-on speed of an IGBT is significantly improved, generally it is still lower than that of a power MOSFET [4]. Furthermore, the turn-off speed is significantly lower than that of a power MOSFET due to the residual current characteristic (tail current), like that of a thyristor. They can operate at frequencies up to hundreds of kHz, generally less than 200 kHz. IGBTs require less silicon area, compared to a similar characteristic power MOSFET, making them more cost effective [16].

1.11.1 IGBT Physical Structure and Operation

An IGBT cell structure is constructed very similar to that of a vertical double diffused power MOSFET (DMOS). The main difference is that the N+ drain region is replaced by the P+ collector layer as illustrated in Figure 1.9. This modification forms a vertical PNP bipolar junction transistor. This additional P+ region will form the cascaded connection of the surface power MOSFET and the underlying BJT. This P+ region forms a PN junction with the N- drift region. Conduction modulation occurs by injecting minority carriers into the drift region. This leads to a larger current density than the power MOSFET, while the forward voltage drop is reduced [16]. Hence the P+ substrate, the N- drift layer and the P+ emitter make up a BJT structure within the IGBT. This BJT structure has a wide base and hence a small current gain (β). The operation of the IGBT can be explained as a BJT with its base controlled by the current applied, through the voltage control signal, applied to the MOS gate. Taking the emitter to be grounded, applying a negative voltage to the collector, the PN junction between the P+ substrate and N- drift region is reverse biased which prevents any current flow, and hence the device is in the reverse blocking mode. If the gate terminal is kept at ground, but a positive potential is applied to the collector, the PN junction between the P+ substrate and N-drift region will remain reversed biased, this is called forward blocking mode. When a positive voltage is applied to the gate and exceeds the threshold voltage (V_{THRES}), this inverts the region under the gate, forming an n-channel, providing a path for electrons to flow into the N- drift region. The PN junction between the P+ substrate and N- drift region is hence forward biased, and holes are injected into the drift region. Electrons and holes recombine maintaining space-charge neutrality, while the remaining electrons flow to the emitter, having a net vertical current flow between the emitter and collector [1].

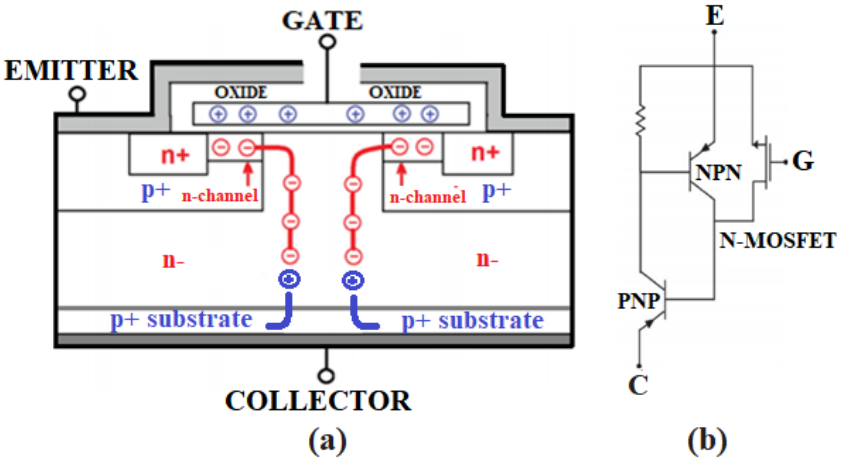


Figure 1.9 - IGBT (a) Cell Structure (b) Equivalent Circuit [1]

As the current density increases, the injected carrier density exceeds the low doping of the base region and becomes much larger than the background doping. This contributes to the decrease in the resistance of the drift region. This highlights the fact that the IGBT has a much greater current density than a power MOSFET with reduced forward voltage drop, hence explaining why IGBTs require less silicon footprint than a power MOSFET with similar electrical characteristics. It is important to note that the base-collector junction of the PNP BJT cannot be forward biased. This means that this PNP BJT cannot be driven into saturation state. But when the gate voltage increases channel pinch-off occurs. The pinch-off condition limits the electron current and consecutively the holes injected from the P+ layer. Hence, it is through channel pinching that current is limited in the intrinsic PNP BJT, hence going into pseudo current saturation. The IGBT is switched off, when the gate is shorted to the emitter to remove the MOS channel charge and hence the base current of the PNP transistor. The collector current is reduced because the electron current from the channel is removed. The excess carriers in the N- drift region decay by electron-hole recombination, which causes a gradual collector current decay. Like other minority carrier devices there is a compromise between the on-state losses and faster switching speeds. In punch-through (PT) IGBT structures, the switching transition time is reduced by the introduction of a heavily doped N+ layer in the drift region next to the collector. Due to the larger doping, the injection efficiency of the collector as well as the minority carrier lifetime is reduced. This enhances the removal of holes from the drift region and therefore increases the turn-off speed. Non-Punch Through (NPT) IGBTs do not have high doped N regions next to the collector, resulting in a longer minority carrier lifetime. Moreover, to prevent punch-through, NPT IGBTs utilize a thicker N-drift layer [18].

Chapter 2 Literature Review of IGBT Degradation and Failure Mechanisms

This chapter discusses the failure mechanisms and reliability testing of IGBTs at both chip and package level. IGBTs have become key electronic components in many applications, including life critical or mission critical products. Over the past decades IGBTs have become central in power electronic systems mainly power electronic converters, in applications such as energy, space and transport, all of which present challenging and severe operational conditions. Hence the understanding of the failing mechanisms and the reliability aspects of IGBTs have become important to semiconductor manufacturers as well as to application electronic engineers to provide reliable solutions, especially in enhanced lifetime (thirty to forty years) applications. Thus, this chapter goes through a broad review of the major IGBTs' failure mechanisms, including the physics of failure, degradation characterization, accelerated ageing, ageing prognostics, and remaining useful lifetime (RUL) estimation techniques.

2.1 Semiconductor Physics of Failure

Physics of Failure (PoF) is a scientific discipline which establishes the source of failure in electrical, electronic, and electromechanical items, which includes fatigue, fracture, wear, and corrosion. PoF items can consist of components, sub-systems, modules, or entire equipment [18]. According to White et al. [20], PoF procedure can be generally divided in the following steps:

1. Isolate failure modes which can be catalyzed chemically, thermally, electrically, structurally, or physically.
2. Isolate the failure locations in each component.
3. Subject each component to accelerated ageing and stress testing, to determine experimentally the main source of failure.
4. Since multiple failure modes might contribute to the general failure of the component, determine a list of failure modes based on their share of contribution to the general failure.
5. Model the dominant failure modes.

6. Obtain statistical significance (statistical distribution) to results obtained from accelerated stress testing.
7. Obtain an equation for the predominant failure modes mean time-to-failure (MTTF).

Semiconductor per se, suffer from two main deterioration mechanisms which are electro-migration (EM) and gate-oxide (GO) degradation. Gate oxide degradation is also referred as time dependent dielectric breakdown (TDDB) and hot carrier (HC) effects. Hot carrier effects include mechanisms such as hot carrier injection (HCI) and negative bias temperature instability (NBTI) [20].

2.1.1 Electro Migration (EM)

Electromigration (EM) consists of the displacement of atoms due to the flow of current within a material. It is characterized by the movement of atoms, due to heat, triggered by high current density [21]. This process leads to both conductor atomic vacancies[1] and atomic deposits[2]. The expansion of vacancies can eventually cause the electrical conductivity to deteriorate, leading to open circuits, while the expansion of deposits can enhance electrical conductivity, leading to short circuits. In semiconductor stack-ups there are embedded interconnects in interlayer dielectric materials. These connections provide the path for electrical signals between layers (equivalent to vias in Printed Circuit Boards, PCBs). Traditionally, the utilized interconnections' material is Aluminum (Al), even though lately other materials such as sandwiched Ti/Al-Cu/TiN metal layers have been employed [19]. Copper (Cu), Silver (Ag), Gold (Au) and other new dielectric materials have been utilized to improve resistance-capacitance delay and the interconnection resistance reliability [19].

EM is the dominating failure mechanism of interconnections [20]. EM has been thoroughly studied for many years, but there are still many aspects of EM which are not properly understood. The main issues relate to the fact that EM is not easy to isolate experimentally and moreover there are many factors which contribute to EM, including material structure and texture, interface structure, physics of voids and their growth, as well as thermal and current density dependencies [20]. Research shows that temperature and current density are the main contributors to EM degradation [22].

[1] *Atomic Vacancy is a type of point defect where an atom is missing from one of the lattice sites.*

[2] *Atomic Deposit is the pile up of conductor atoms that drift toward other nearby conductors, creating an unintended electrical connection known also as a hillock.*

Black [23], developed an empirical equation which relates the MTTF of a metal to the temperature and current density:

$$MTTF = \frac{A}{j^n} e^{\frac{Q}{kT}} \tag{2.1}$$

where A is a material and process-related constant,
j is the current density,
n is a model parameter,
Q is the activation energy[1],
k is the Boltzmann's constant
and T is the absolute temperature in Kelvin.

The above equation provides an abstract model, describing the relationship of the failure rate to temperature. The Black model's values are obtained through experimental data taken at elevated temperature and electrical stress levels in short periods of time (High Temperature Operating Life, HTOL tests).

Hence the parameters A, n and Q are found by adopting the Black model to the specific experimental data. Thus, the main scope of the model is to map the experimental data obtained during accelerated elevated temperature and electrical stress tests and translating to expected failure rates under normal operating conditions.

2.1.1 Basic Physics of Electro Migration

A detailed review of the research conducted in EM especially in the failure processes can be found in [24] and summarized in Figure 2.1. As electronics miniaturization is ever increasing, device density is increasing, hence interconnects are consequently miniaturized further, reducing in height and cross-section. This leads to enhanced current densities in the order of hundreds of Amperes/cm^2. This effect is also present in power devices where miniaturization issues are less predominant but the currents available are much larger than in small signal devices. At these elevated current densities, the momentum, between the electrons and the metal atoms will become significant.

[1]*Minimum energy that must be available for a chemical reaction to occur.*

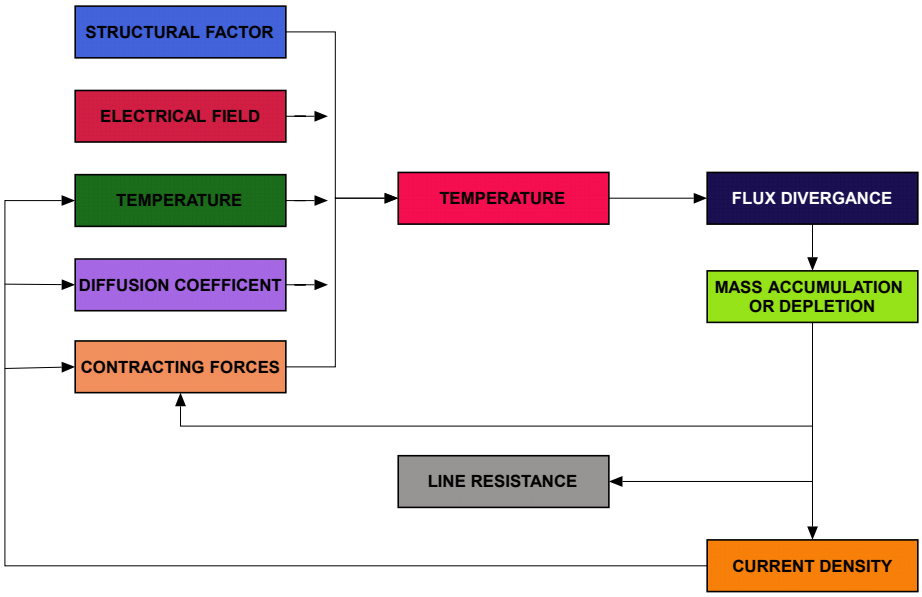


Figure 2.1 - Electromigration Failure Mechanisms [24]

This phenomenon referred as electron-wind force [24], will trigger the transport of the metal material along the direction of the electron movement. The metal atoms are energy activated by the electron-wind, which are in-turn influenced by the same electric-field dictating the electron flow. This electric-field will cause the positive ionization of the activated metal atoms, which will counteract the movement of the electron-wind. The resultant of the ionized metal atoms and the electron-wind will determine the net direction of the material mass transfer. As already discussed, this transport of material will manifest itself into either atomic vacancy referred also as voids, or atomic deposits which are also referred as material hillocks [25]. The voids will contribute to the decrease of the cross-sectional area of the conductor and hence increase the local resistance and current density at this point. Both will in turn contribute to the build-up of "hot spots", enhancing further the EM effects, leading to thermal runaway and failure.

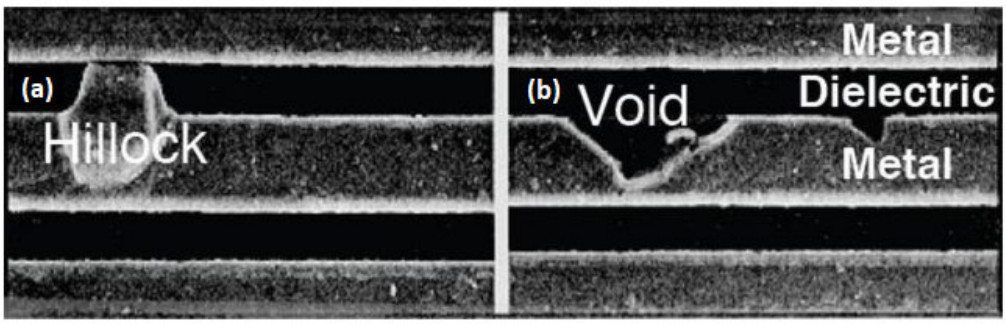


Figure 2.2 – Microscope imagery demonstrating the development of (a) Hillock and (b) Void through electromigration, within an interconnect of an ASIC [28].

The transport of electrons through a metal is represented through Bloch Wave, which is a wave function of a particle in a periodical-repetitive environment. A typical example of Bloch Waves are electrons moving in a semiconductor, hence referred as Bloch Electrons. Bloch Waves bring about the concept of electronic bands and hence explain the formation of the valence band and conduction band in a semiconductor [25], [37]. According to Cho et al. [26], Bloch Electrons can transfer energy through the interaction with structure defects such as Grain Boundaries. Single crystals with continuous atomic lattice and orientation form a grain. Neighboring grains with different orientations are separated by an immaterial surface referred to as a Grain Boundary. This is illustrated in Figure 2.3. When an electron interacts with a Grain Boundary, the electron is scattered by an ion, hence the electron's momentum is reversed. This causes a change in momentum and in the transport direction, creating the ion current divergence necessary to form a void. Similarly, ion pile-up can manifest in areas where the grain sizes increase in the direction of the electron flow. Hence densely grained areas will channel ions out more effectively than sparsely grained areas. Therefore, the actual microstructure of the metal, such as the grain density, grain boundaries and crystallite texture play a significant role in the EM process. Other important factors contributing to EM include electric field, current density, and temperature [27].

2.1.2 Electro Migration Statistical Modelling

Modelling EM accurately needs to consider all these factors. Hence statistical models based on empirical data are utilized to help understand EM mechanisms. The most common statistical distribution which characterizes EM related failures is the lognormal failure distribution as described by Equation 2.2,

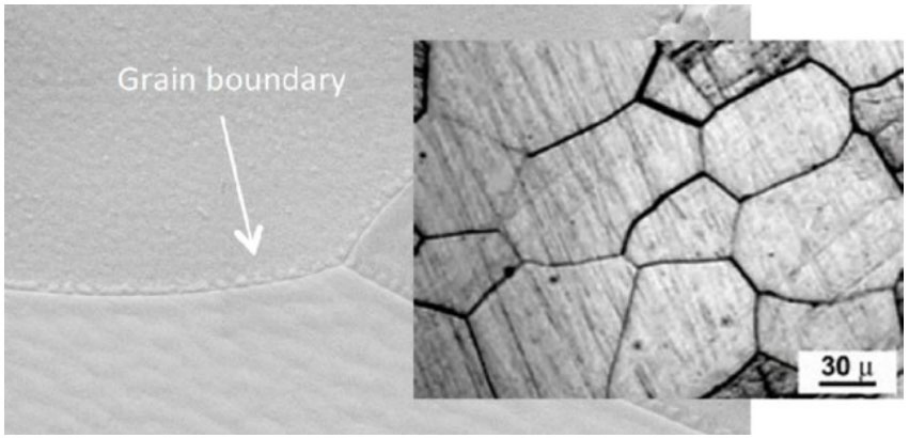


Figure 2.3 – Grains and corresponding Grain Boundaries of a metal surface [32].

$$f(t) = \frac{1}{\sigma t\sqrt{2\pi}} e^{\left\{-\frac{1}{2}\left(\frac{\ln(t)-\ln(MTTF)}{\sigma}\right)^2\right\}} \quad (2.2)$$

where t is time,

MTTF is the median time to failure,

σ is the lognormal standard deviation,

The MTTF is normally obtained through the Black model. The value of the lognormal standard deviation, σ, was related in literature to various factors contributing to EM. Cho et al. [26], related σ to the ratio between the grain boundary thickness and grain size, hence the material structure. Oates [27] related σ to the current density while Hinode et al. [29] provided a general range for σ between 0.28 to 1.4. Different studies [30], [31] and [33], utilized the lognormal failure distribution to model EM failure. Other studies utilized other statistical modelling, primarily the Weibull Distribution [34], [35]. The lognormal and the Weibull statistical modelling are reliably utilized when EM failure is due to a predominant physical phenomenon. When multiple simultaneous physical modes are contributing to EM, a bimodal lognormal distribution modelling was utilized [36].

2.2 Hot Carrier Degradation

Hot carrier degradation (HCD) is considered another important failure method in relation to solid-state devices. This phenomenon has a direct impact on the device's lifetime. Semiconductor charge carriers (holes/electrons) are continuously absorbing and emitting phonons, which are quanta of energy associated with the natural vibration waves of the crystal lattice. When the charge carriers are in thermal equilibrium, the net energy gained vis-à-vis the phonons' absorption and emissions process, is practically zero. At room temperature, the kinetic energy of electrons is marginally larger than the higher energy level of the conduction band, by a divergence of kT_{RM} (where k is the Boltzman Constant and T_{RM} is the room temperature). Similarly, at room temperature, holes manifest a kinetic energy which is marginally less than the edge of the valence band, again with a divergence of kT_{RM} [20]. When the electric field is small, the velocity of the charge carriers due to the field is small and therefore the contribution of kinetic energy gained by the charge carriers due to the field is marginal. Hence, at small electric fields, the energy divergence is only due to the ambient

temperature which at room temperature is provided by kT_{RM}, which is small (≈ 25meV) when compared to the energy levels at the edges of the conduction and the valence bands. On the other side, at high electric fields (≈1MV/m), accelerated charge carriers gain more energy than they lose, and hence the net kinetic energy gained kT_{EHEF} (where T_{EHEF} is the effective temperature at high electric field) is much larger than kT_{RM} and does not remain negligible when compared to the energy levels of the edges of the conduction and valence bands. Hence, the kinetic energy level for an electron accelerated due to high electric field, is $E_{CB} + kT_{EHEF}$ (where E_{CB} is the energy level at the edge of the conduction band) [20]. This translates to a very large Fermi-Dirac effective temperature (>10k Kelvin) and hence corresponding carriers at this energy level, are considered "hot carriers" occupying the top of the Fermi-Dirac distribution [37]. Thus, the term "hot carrier" does not refer to the actual physical temperature of the semiconductor (even though a higher semiconductor temperature will increase the population of hot carriers) but rather referring to the Fermi-Dirac effective temperature.

Instead of recombining or conducting, "hot carriers" have the necessary energy levels to escape the semiconductor material. A direct consequence is enhanced leakage current. "Hot Carriers" can be generated when a semiconductor is exposed to electromagnetic radiation (i.e. Visible Light, X-Rays etc). In this case electromagnetic energy can possibly excite the electrons out of the valence band triggering recombination. If the electron receives sufficient energy to surpass the conduction band, it effectively becomes a "hot electron" with a mobility that enables it to effectively leave the semiconductor and move to another material [37].

2.2.1 Hot Carrier Injection Mechanisms

Hot carrier injection (HCI) is a phenomenon in semiconductor where a charge carrier will gain sufficient energy to break an interface state overcoming the potential barrier. This has important implications specially to gate activated devices such as MOSFETs and to IGBTs since intrinsically these devices are MOSFET driven. When the gate voltage is equal or smaller to the output drain-to-source voltage (V_{DS}), the channel formation is more mature near the source than the drain. This implies that the channel current will generate a larger potential difference near the drain due to a larger channel resistance on this side. Hence, at this physical point, the electric field can be so large, that charge carriers can attain sufficient energy and become "hot carriers". The majority of these "hot carriers" will flow towards the drain hence generating a rise in the drain current (I_D). On the other side, some of the "hot carriers" will gain enough energy such that via a small gate current (I_G), they will be able to surpass the Silicon-

Silicon Dioxide (Si-SiO_2) interface, ending up in the gate oxide. This HCI process can permanently change the switching characteristics of the device [39]. Takeda et al. [38] classified hot carrier injection into three mechanisms known as; Channel Hot Electron (CHE) injection, Drain Avalanche Hot Carrier (DAHC) injection and Secondary Generated Hot Electron (SGHE) injection. CHE injection in mainly caused by "hot electrons" escaping from the channel into the oxide, causing oxide degradation. This phenomenon can happen even at low temperatures. DAHC injection can manifest in both charge carriers and hence can produce harsher degradations than CHE. SHCE injection is predominant in thinner oxide semiconductor devices and is mainly related to minority carriers.

2.2.2 Channel Hot Electron (CHE) Injection

Figure 2.4 illustrates CHE injection process, which manifest in n-MOSFETs when the gate voltage (V_G) and the drain to source voltage (V_{DS}) are similar. Correspondingly, Figure 2.5 illustrates the gate current vs gate voltage characteristics (I_G vs V_G), which includes the CHE injection phenomenon. One can notice that this plot is characterized by an initial gate current (I_G) increase. This effect is attributed to CHE and essentially depends on two reasons. First, when the channel is forming, the inversion charge in the channel is enhanced. This increases the availability of electrons present in the channel and hence increases the possibility that electrons are injected and trapped in the oxide. Secondly, the injected oxide electrons, will be prevented from drifting back to the channel due to the vertical electric field in the oxide. However, if the gate voltage is large enough, the channel is thoroughly formed, which reduces the channel's electric field, hence reducing the possibility of generating "hot electrons" [40].

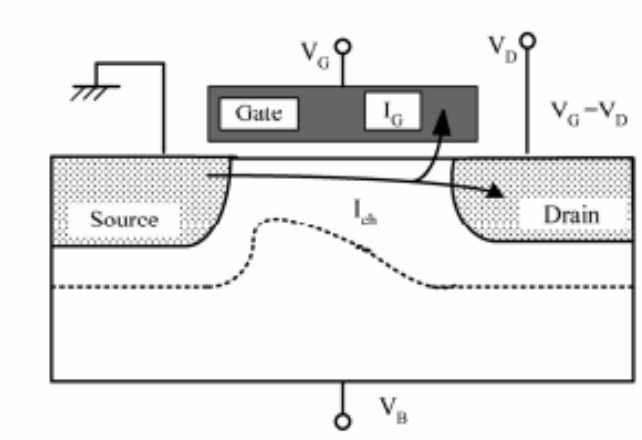


Figure 2.4 - N-MOSFET CHE Injection manifesting @ $V_G \approx V_D$ [40]

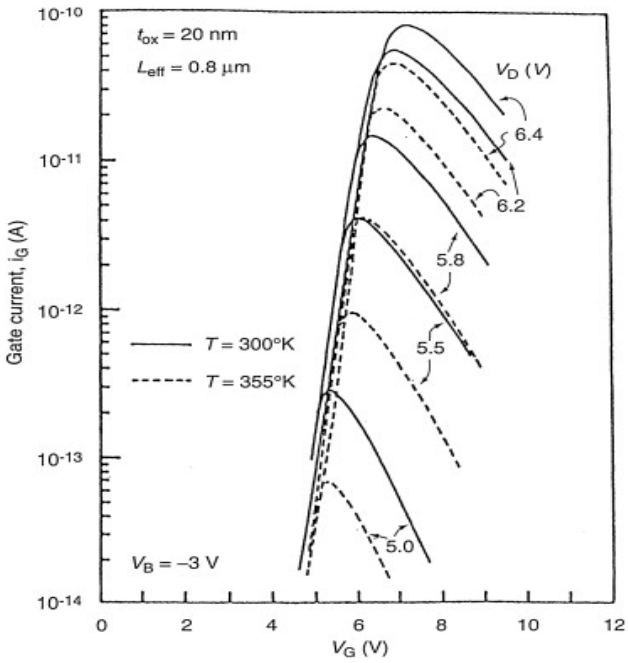


Figure 2.5 – I_G vs V_G characteristics manifesting CHE Injection [40]

Thus, gate current (I_G) manifests a peak when the gate voltage (V_G) is approximately equal to V_{DS}. Takeda et al. [38] reported that this is the best condition for CHE injection to take place. CHE electrons are injected since they would have gained sufficient energy to overcome the Si−SiO2 interface barrier but without experiencing any energy losses due to collisions in the channel. Therefore, CHE injected electrons are also referred to as “lucky electrons” [40]. Consequently, the gate current (I_G) is considered the predominant source of electron trapping within gate oxides.

2.2.3 Drain Avalanche Hot Carrier (DAHC) Injection

DAHC injection manifests in MOSFETs when the drain voltage (V_D) is greater than the gate voltage (V_G), as illustrated in Figure 2.6. This injection mechanism depends on energetic charge carriers, that knock a bound electron from its bound state (within the valence band) and push it to a state available for conduction (within the conduction band) generating an electron-hole pair. This process is known as impact ionization. If this occurs in a region of high electric field it can lead to avalanche breakdown. These secondary charge carriers liberated through impact ionization can become hot, injecting in the oxide, and causing degradation. Hence DAHC is characterized by the simultaneous injection of both hot holes and electrons within the oxide as well as across the drain junction just underneath the substrate surface [40].

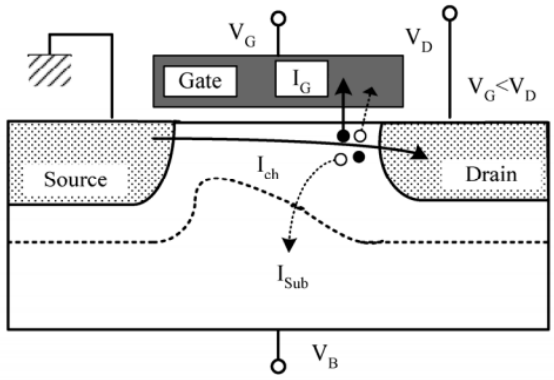


Figure 2.6 – Drain Avalanche Hot Carrier Injection [40]

2.2.4 Secondary Generated Hot Electron (SGHE) Injection

SGHE is mainly attributed to two secondary "hot electrons" generation mechanisms, as illustrated in Figure 2.7. The first mechanism is the generation of secondary "hot electrons", generated deeper in the silicon (Si) substrate due to impact ionization by hot holes caused by high substrate bias voltages [40]. The second mechanism is the generation of secondary "hot electrons", caused by a photon-strike [38]. Takeda et al. [38] showed that SGHE injection mechanism is more likely to happen from photo-induced secondary generation rather than through secondary impact ionization in the deep substrate.

2.2.5 Hot Carrier Injection Reliability Implications

Modern power semiconductor devices are required to operate at faster commutation speeds (MHz), with reduced switching losses and enhanced power conversion efficiency. This was achieved by scaling down power devices to smaller sub-micron dimensions.

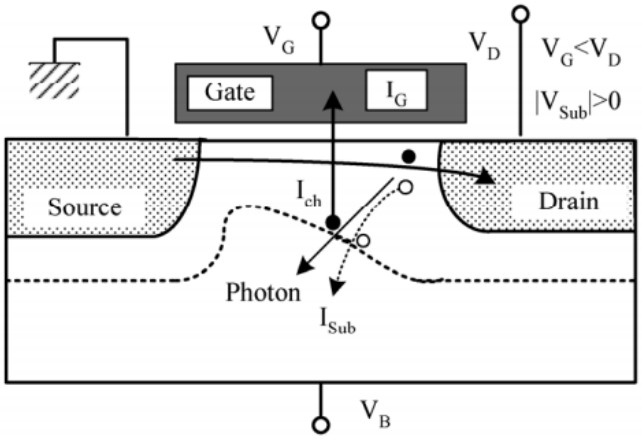


Figure 2.7 - Secondary Generated Hot Electron (SGHE) Injection [40]

On the other side drive voltages have not scaled down due to different reasons which include noise margin, non-scalable threshold voltages and parasitic capacitances with the most influential parasitic capacitance being the Miller capacitance. The result of this scaling has led to the saturation of majority and minority carrier velocities due to internal soaring electric fields. This situation presents a fertile environment for the generation of "hot carriers" and hence manifestation of HCI effects, presenting substantial reliability issues. For this purpose, different HCI reliability models were developed. These include the "Lucky Electron Model" originated by Shockley, applied by Verwey et al. [41] and verified by Ning et al. [42]. Other models include empirical models such as the Power Law Model proposed by Takeda et al. [43] and statistical based models as proposed by Hu [44].

2.3 Time Dependent Dielectric Breakdown (TDDB)

TDDB is related to the physical degradation of the silicon dioxide (SiO_2) dielectric material. This is the insulating layer commonly utilized between the gate terminal and the conducting channel of a gated transistor. TDDB leads to the actual physical breakdown of this insulating layer because of long-time application at low electric fields unlike the immediate breakdown when a large electric field is applied. Due to its good insulating properties (high bandgap) and the ability to scale down the manufacturing, SiO_2 has been widely utilized for dielectric purposes and one of the main contributors for the MOS proliferation [45].

The physical degradation mechanism related to TDDB is still an open discussion. The understanding is, that it is a consequence of the applied field across the dielectric and the tunneling of electrons. This creates defects in the oxide film. The accumulation of defects over time reaches a point when eventually a loss in the dielectric properties is triggered. This will result in the localized rise in temperature, leading to hot spots, which will lead to a permanent damage within the oxide. TDDB can have multiple root causes and to date it is still not fully understood. This section discusses the two principal root causes which are, entrapped charge within SiO_2 and Tunneling Current [45], [46].

2.3.1 Entrapped Charges in SiO_2 and corresponding Interface

Even though SiO_2 has very good insulative properties, it is not flawless and has the tendency to produce oxide vacancies. Dangling bonds refer to those atoms which possess too few bonding partners and hence possess unpaired electrons. Silicon-based materials may have dangling bonds on their atoms which can affect the band gap energies of the material. A

common site where dangling bonds are produced is at Si-SiO_2 interface. The formation of dangling bonds can be subdued through hydrogen passivation, hence stabilizing silicon atoms from chemical reactions [47]. Both oxide vacancies and dangling bonds are considered good locations where charges are trapped. Hence oxide can manifest defects due to four categories of charge carriers as illustrated in Figure 2.8. These include inherent charges trapped within inside vacancies of the oxide, charges trapped near the Si-SiO_2 interface, fixed oxide charges induced during the fabrication process, and sodium/potassium related mobile ionic charge. These charges can be excited and hence can make the transition from the silicon oxide interface to the surface state, altering the electrical and switching characteristics of the gated device [40].

2.3.2 Current Tunneling and TDDB

Tunneling is a quantum-mechanical phenomenon, where an electron due to the wave-particle duality, can propagate through an insulating layer, under the influence of an electric field. Tunneling can happen if occupied energy states and unoccupied energy states exist on each side of the insulating layer, the insulation layer is thin enough for the applied electric field and that momentum is always conserved [48]. Current tunneling, is mainly divided into three main processes; Fowler-Nordheim (F-N) Tunneling, Direct Tunneling and Trap Assisted Tunneling.

F-N tunneling is related to the process where electrons penetrate the oxide and become available at the oxide's conduction band. This is done under the influence of a high electric field. It is characterized by a triangular shape barrier, with tunneling only occurring through a localized part of the oxide. After tunneling through the triangular barrier occurs, the rest of the oxide will not impede the flow of current. This tunneling process is an important mechanism for thin oxide barriers [48].

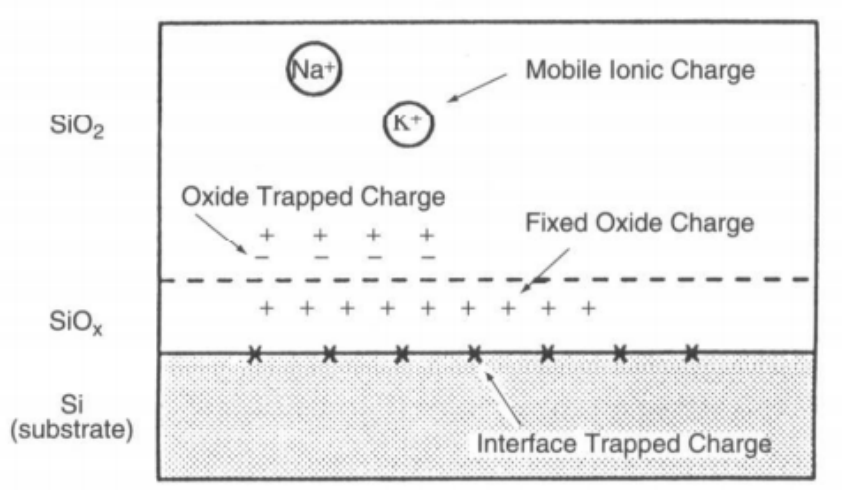


Figure 2.8 - Charges within SiO2 and Si-SiO2 interface [40]

Direct tunneling is the predominant current tunneling mechanism in oxide layers smaller than 5nm, even though at these thicknesses there are other quantum effects which are not negligible. In Direct Tunneling conditions, the electron tunnels through the whole barrier unlike in F-N tunneling, where this effect is localized [48]. There is no trivial dependence of the tunneling current density and field strength, but it is the dominant mechanism for thin SiO_2 layers [49].

Trap-assisted tunneling happens since traps effectively subdivide the barrier into shorter sections, with the field exciting the trapped charge carriers. Trapped-assisted tunneling is dependent on the traps' density as well as the electric field [50]. Other sources can contribute to tunneling current such as the gate-drain and gate-source overlap in MOS devices. Electron hopping is another mechanism which contributes to current tunneling. It is mainly due to thermally excited electrons which gain the ability to "jump" the interface [20].

2.4 Negative Bias Temperature Instability

Negative Bias Temperature Instability (NBTI) is another failure mechanism which predominantly occurs in MOSFETs' gates and hence intrinsically in IGBTs too. The main indicator of NBTI is an increase in the threshold voltage and a decrease in the output current, consequently a decrease in the transconductance. P-Channel devices are the most susceptible to such a phenomenon because they are always operated with a negative gate to source/emitter voltage. None the less, n-channel devices can also suffer from such a phenomenon since there are scenarios where the gate to source/collector voltage is negatively biased mainly to dictate a forced or deep device's cutoff.

An increase in temperature makes this phenomenon more severe. Temperature stress under constant (DC) negative gate to source/emitter bias, causes the generation of traps at the interface between the gate oxide and the silicon substrate. The degradation of device's performance, due to the shift in the threshold voltage, is one of the predominant reliability issues, especially when considering that NBTI worsens exponentially with time. Deal et al. [51] was one of the first to study this phenomenon naming it "Drift VI". Goetzberger et al. [52] showed how surface state changed, when placing MOSFETs under negative gate bias and temperature overstress. Jeppson et al. [58] was one of the first to propose a physical model, explaining the growth of interface traps when the device was subjected to negative gate to source bias. NBTI analysis became more important in recent years, since NBTI effects increase, with decreasing oxide thickness.

2.4.1 NBTI Physics

As described earlier silicon dioxide (SiO_2) is mainly utilized as the dielectric material within the gate of gated devices. Even though SiO_2 has very good insulative properties, it is never charge-carrier free and hence parasitic charges exist within this material. These charges can be categorized into four types, as described in section 2.3.1. The threshold voltage (V_{THRES}) of a gated device is reached when the surface of the substrate is driven into weak inversion, that is the voltage at the gate is such to just form a channel. The threshold voltage (V_{THRES}) is given by Equation 2.3, [56].

$$V_{THRES} = V_{FB} - 2\phi_F - \frac{|Q_F|}{C_{ox}} \tag{2.3}$$

Where V_{THRES} is the Threshold Voltage,

V_{FB} is the Flat Band Voltage,

$|Q_F|$ is the depletion layer charge provided by Equation 2.4.

Φ_F is the bulk surface potential which is provided by Equation 2.5.

$$|Q_F| = \sqrt{4q\varepsilon_s N_a \phi_F} \tag{2.4}$$

Where q is the electronic charge,

ε_s is the absolute permittivity of the semiconductor,

N_a is the substrate doping (carrier density after doping),

C_{ox} is the oxide capacitance per unit area,

$$\phi_F = V_t ln \frac{N_a}{n_i} \tag{2.5}$$

Where V_t is the thermal voltage provided by $\frac{kT}{q}$, where k is the Boltzman Constant and T is temperature and q is the electronic charge.

n_i is the intrinsic carrier density of the semiconductor (carrier density of semiconductor which has not been doped. This parameter is temperature dependent).

The flat band voltage (V_{FB}) of a MOS structure is the difference between the gate metal work function (ϕ_M) and the semiconductor work function (ϕ_S). The work function is the voltage required to extract an electron from the Fermi energy level to the vacuum level. The

semiconductor work function (ϕ_S) is affected by the presence of charge within the oxide and charge at the oxide-semiconductor interface as described by Equation 2.6, [56].

$$V_{FB} = \Phi_{MS} - \frac{Q_f}{C_{OX}} - \frac{Q_{it}}{C_{OX}} \tag{2.6}$$

Where V_{FB} is the Flat Band Voltage,

ϕ_{MS} is the metal work function (potential),

Q_f is the fixed charge due to oxide traps,

Q_{it} is the charge due to interface traps,

C_{OX} is the is the oxide capacitance per unit area.

Equation 2.6 shows that the Flat Band voltage (V_{FB}) and hence the threshold voltage (V_{THRES}) can be altered either by Q_f or Q_{it}. In literature, one can find different explanations for the root cause of NBTI, the predominant explanation is based on the charge states of the interface traps Q_{it} and the oxide traps Q_f. Oxide traps are positively charged by hole trapping in both the n and p-channel devices. Hence the contribution of the oxide traps in relation to the shift of the threshold voltage for both the n and p-channel devices is affected approximately in the same manner. On the other side, charge state at the interface, depends on the Fermi-level. The Fermi-level for a p-channel device just biased into inversion is below the middle energy level. This means that that the acceptor trap levels are empty, and the donor traps levels are partially filled. Hence the net charge resulting for the p-channel at the interface is positive and hence adds to the positive charge produced by oxide traps [53], [54], [56].

On the other-hand for n-channel devices, the Fermi-level at the interface is located above the middle energy level. This implies that the donor trap levels are filled, and the acceptor levels are partially filled. The result is that, for an n-channel device, a negative charge is due to interface traps, which tends to cancel with the oxide traps positive charge. Hence in p-channel devices, both the interface traps and oxide traps contribute to the threshold voltage shift. In n-channel devices the shift introduced by the oxide tends to be counterbalanced by the interface traps. Therefore, the threshold voltage shifts in n-channel devices are less evident. This is evidenced by the studies conducted by Huard et al. [53], which confronted bias temperature instability of p-channel and n-channel MOSFETs with positive and negative voltage stress. As illustrated in Figure 2.9 the highest degradation is evidenced in p-channel MOSFETs.

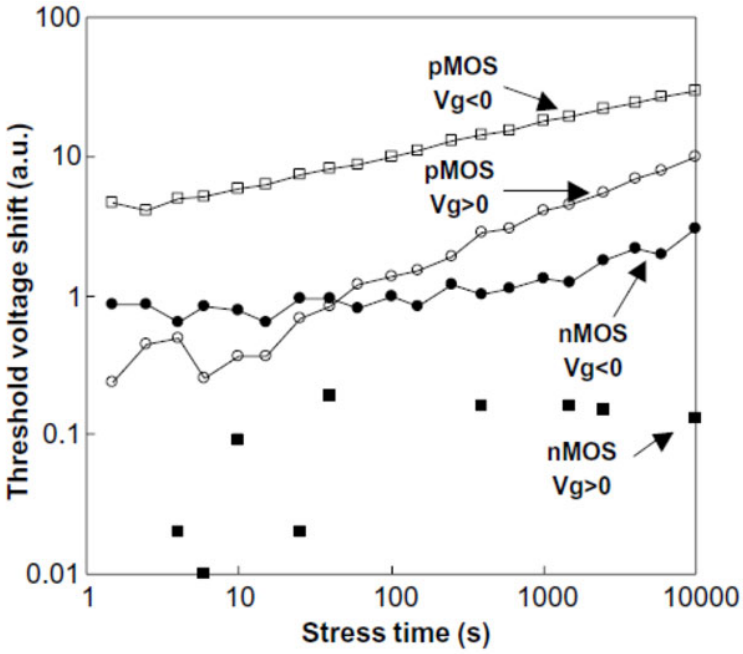


Figure 2.9 - Effects of NBTI for p- and n-channel MOS structures [53]

Tsetseris et al. [60] provided another reason for NBTI differences in p-channel and n-channel devices, by highlighting the importance of atomic hydrogen (H^+), which is found in the substrate dopants of both p and n-channel devices, which are phosphorus (P) and boron (B) respectively. This study highlights how H^+ can weaken and break Silicon-Hydrogen (Si-H) bonds at the interface. The energy required to dissociate Si-H bonds is normally very high. These bonds are only weakened in the depletion region. When a p-channel device is subjected to NBT stress, a depletion region is formed in the substrate. Here hydrogen atoms can be dissociated leading to a degradation at the interface. For positive stress, no depletion region is formed and hence no hydrogen is available via dissociation, thus the level of degradation is minimal. As already described n-channel MOSFETs' substrate is doped by boron, and activation energy required to dissociate hydrogen from boron is much higher than that of phosphorus even in the depletion regions. This makes n-channel MOSFETs less prone to NBTI irrespective if the stress voltage is positive or negative.

2.5 IGBT Structure and Manufacturing

There are different stages which characterize the lifecycle of an IGBT. It starts with construction and qualification at the solid-state manufacturer plant. It proceeds through the storage and transport, until it reaches the application industry plant where it is mounted within the desired circuitry, at this stage, circuit qualification is conducted. The finalized circuit is shipped to the intended customer, for commissioning and utilization. Throughout the above

stages, events such as mechanical shocks, thermal shocks, vibration, incorrect handling, Electrostatic Discharge (ESD), and incorrect assembly (soldering/mounting) may occur. All the above events may cause reliability issues which can eventually lead to IGBT failure. During operation, IGBTs can be subjected to a variety of strains, ranging from thermal/environmental overstress, overvoltage, and overload scenarios. Again, these events can deteriorate or sometimes destroy these devices. Even sustainable electrical or environmental conditions might lead to IGBT failure mainly due to long-term degradation and device ageing. Hence this section will focus on the construction of an IGBT, focusing on those aspects which might be affected or are susceptible to events during its life cycle which might lead to an early end-of-life.

2.5.1 IGBT Cell Structures

An IGBT die, consists of multiple IGBT cells connected in parallel, to provide the required on-state and off-state capabilities. IGBT cells are mainly classified into three categories: Punch Through (PT), Non-Punch Through (NPT) and Field Stop (FS). These are illustrated in Figure 2.10. The NPT cell structure permits forward and reverse blocking voltage utilizing a symmetric structure. Since for this structure hole doping is uniformly distributed over the drift region, holes flow due to a drift mechanism rather than a diffusion mechanism. Hence this structure is ideal for AC applications where the IGBT must withstand significant voltages in both polarities. On the other-hand PT and FS cell structures permit only forward blocking voltage capability by utilizing an asymmetric structure, through the introduction of an n-type buffer layer. The main purpose of this layer is to make available electrons for recombination, hence obtaining a faster switching. Conversely, it reduces the width of the N^- drift region, hence diminishing the stand-off capability. Therefore, these latter structures are intended for DC operations, where the device does not necessitate high reverse breakdown voltage [5], [61], [62]. Another IGBT cell classification is related to the gate configuration. Output current flow control can be obtained through either a planar gate Diffused Metal Oxide Semiconductor structure (D-MOS) or through a gate structure which is U-Shaped (U-MOS) which is more commonly known as Trench-Gate MOS technology [5]. In the planar gate configuration, the gate is fabricated on top of the IGBT hence forming a horizontal input MOSFET structure. In the second gate configuration, the gate is “trenched” in the P-body of the IGBT cell hence forming a vertical input MOSFET structure. This is illustrated in Figure 2.11. The trench gate IGBT cell, improves the on-state capabilities of the device (smaller V_{CE_SAT}) without compromising the off-state capabilities (breakdown voltage, V_{CE_MAX}).

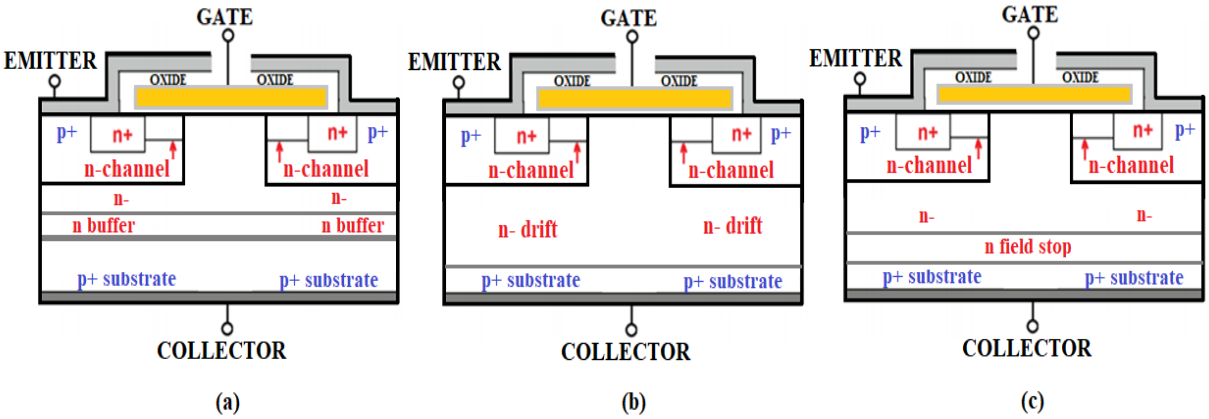


Figure 2.10 - IGBT Cell Structure (a) PT IGBT (b) NPT IGBT (c) Field Stop [61]

The trench gate architecture aims to maximize the verticality aspect of the design by conducting the current vertically rather than laterally hence achieving high on-state drive current with minimal on-state losses. This is accomplished by forming an accumulation layer along the sides of the trenches, connecting the N^+ source to the N^- drain region of the input MOSFET structure. This enhances the conductivity of the formed channel, hence improving the electron injection in the drift region. Furthermore, the trench-gate technology, has an added benefit of requiring fewer IGBT cells for a particular application, since the required active area will be less for the same off-state capabilities of a planar gate IGBT. Other IGBT cell technology such as the Lateral-MOS IGBT are employed, with more recent cell advancements including the Super-Junction Trench IGBT [5], [61], [62].

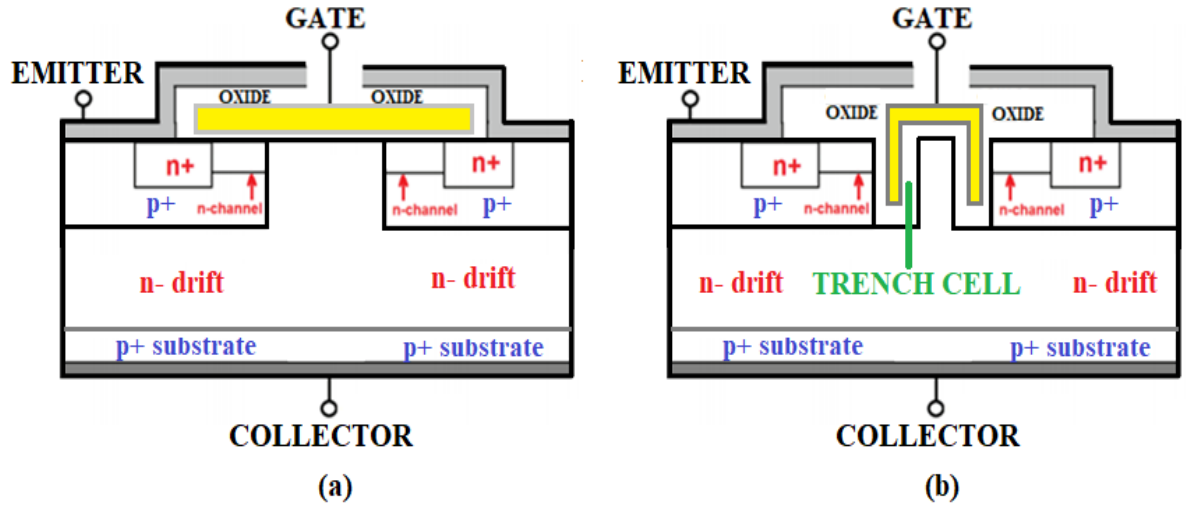


Figure 2.11 - IGBT Cells Categorized by Gate Structure (a) Planar (b) Trench

2.5.2 IGBT Cell Manufacturing Process Flow

This section will discuss the general procedure undertaken to fabricate an IGBT cell. The discussion will focus on the fabrication of Trench-IGBT technology as this is the predominant design. The following are the general steps undertaken [64]:

1. The growth of the epi layer of the drift region over a low resistivity silicon substrate layer for the collector.
2. The p-type doping for the body implant over the substrate.
3. The n-type doping for the emitter implant over body region.
4. Trench formation. This is commonly conducted by reactive ion beam etching where reactive plasma is used to remove wafer materials.
5. Gate definition. This is conducted by first oxidizing the silicon of the channel, forming an insulating layer of silicon dioxide (SiO_2) through Tetraethoxysilane (TEOS) $Si(OC_2H_5)_4$ etching and deposition. A conductive gate material (commonly a highly doped silicon) is deposited. This is achieved through the etching and deposition of polysilicon utilized as the conducting gate material.
6. TEOS etching and deposition for emitter metal isolation.
7. Source metal deposition. This is conducted through sputter coating which is a process utilized to cover a material with a thin layer of metal.
8. Finally, nitriding is conducted, a heat-treating process which diffuses nitrogen to obtain a hardened surface.

Figure 2.12 illustrates the various processes for a trench NPT and PT IGBT cell structure. As explained the process of manufacturing a trench IGBT involves multiple stages, each stage involving several processes and steps. The two most important and difficult processes are lithography[1] and the trench etching process which are most likely to cause defects. A little deviation in these processes could lead to device performance degradation and impact the fabrication process yield. Lithographic limitations in relation to power MOSFET manufacturing were studied by Goarin et al. [65]. In this study scaling down of the trench and the contact width was experimentally analyzed and was achieved through Deep Ultraviolet (DUV) lithography. Figure 2.13 illustrates a cross-sectional scanning electron microscope SEM image, highlighting the trench technology explained above [64].

[1]The process of transferring patterns to thin layer of radiation-sensitive material covering the semiconductor wafer.

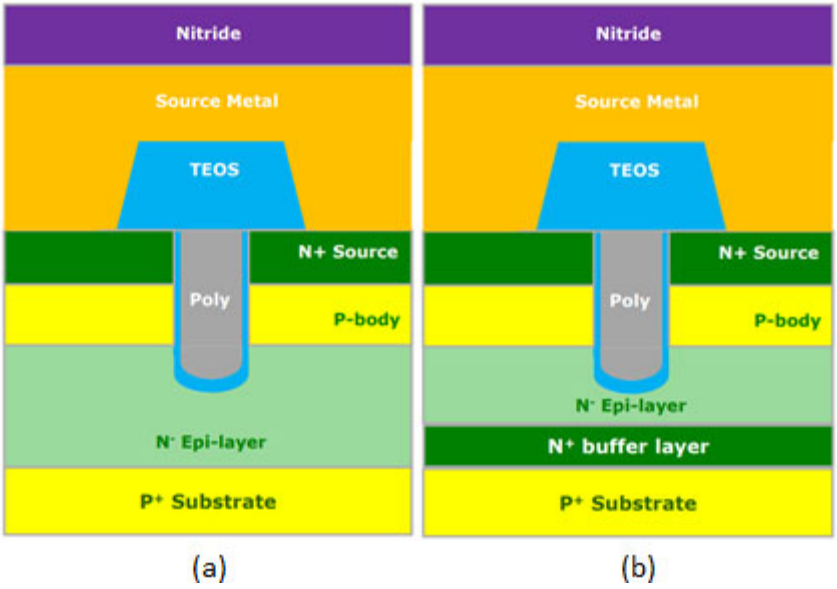


Figure 2.12 - (a) NPT IGBT Cell Structure (b) PT IGBT Cell Structure [65]

Enhancing the on-state performance, depends on the current density of the channel. This predominantly depends on the self-alignment fabrication processes. Without self-aligned fabrication processes the tolerances between different steps would become a major problem and cause limitations. Efforts to improve the trench power fabrication technique mainly focus on trench etching technology and self-alignment process technology.

Manufacturers strive to improve the on-state capabilities of IGBTs. One of the most important parameters related to the on-state capabilities and losses of IGBTs is the on-state collector-to-emitter saturation voltage (V_{CE_SAT}). However, there is a tradeoff between the on-state capability and the breakdown stand-off voltage. The larger the stand-off voltage the higher the on-state voltage (V_{CE_SAT}) gets. Hence for transistors with breakdown voltage exceeding the 400V, the diminishing of the on-state voltage will become a problem. For this purpose, the super-junction (SJ) structure is an innovative design which solves this problem and hence obtain large breakdown voltages and a low on-state voltage [66]. The SJ design was originally utilized in power MOSFETs to improve the stand-off capabilities without compromising the on-state resistance (R_{DS_ON}). This technology was mainly embraced by Infeneon Technologies with their CoolMOS technology and Renesas Electronics with super-junction MOSFETs [65]. A super-junction structure utilizes multiple p-pillars and n-pillars in the drift region. The technology is based on charge compensation techniques whereby excessive charge in the n-pillar is counterbalanced by the p-pillar. The epitaxial growth process is conducted in various steps, hence increasing gradually the total implanted layer thickness until the required voltage withstand, is achieved.

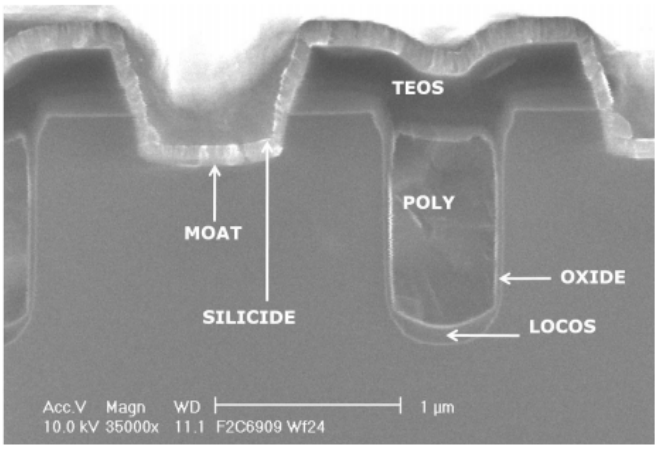


Figure 2.13 – Scanning Electron Microscope Imagery of Trench-Gate Technology [64]

This complication, drives the device's fabrication costs high, leading to limited productivity and proliferation of this technology. On the other-side, Bauer et al. [66] reported that such SJ IGBTs surpass by a very significant margin their SJ MOSFET counterparts in terms of power-handling capability and on-state and turnoff losses.

2.5.3 IGBT Die Design and Fabrication

An IGBT die consists of multiple cells. The number of cells determine the on-state current density of the IGBT. The IGBT design is required to have the highest on-state current density possible, as this minimizes the die size required for a particular application. The maximum current density of the IGBT is limited by its maximum junction temperature (T_{J_MAX}), which must not be exceeded to ensure long-term reliability. All the above incur on the active area of the IGBT structure which can be determined by Equation 2.7.

$$A_{ACTIVE} = \frac{I_L}{J_{ON}} \tag{2.7}$$

Where A_{ACTIVE} is the active area, I_L is the application maximum load current and J_{ON} is the current density. Hence the active area determines the area within which the cells will be placed. IGBT cells will be integrated in parallel throughout the active area separated one from another by the cell pitch. It must be ensured during manufacturing that throughout the length of the active area, the lithography does not produce any short circuits between the gate and source. Furthermore, the dielectric between the polysilicon gate and the source metallization must be free of insulative defects over the entire active area. Figure 2.14 illustrates how the polysilicon gate is laid out, focusing on one edge of the die's active area.

The polysilicon gate is characterized by polysilicon windows, which do not extend till the edge of the active area to allow horizontal polysilicon formation to connect all the vertical gate regions of all cells. This ensures that the gate signal is distributed across the entire active area [5].

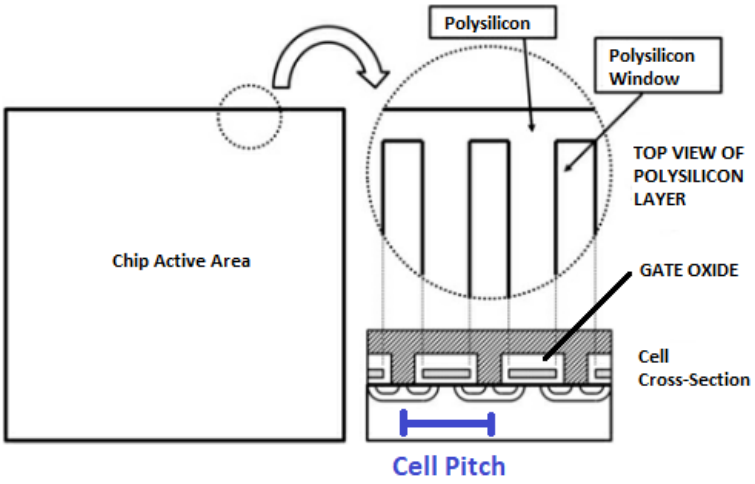


Figure 2.14 – IGBT Die Active Area [5]

Due to the vertical structure of the IGBT, a gate connection pad is included at the top of the IGBT structure in conjunction with the emitter connection pad. These are in-turn wire bonded to the package leads. Generally, gate connection pads are configured in three possible design configurations. The first configuration involves a gate pad being located at a corner of the die. In the second configuration the gate pad is located at the center of the die. In the third configuration the gate pad is located at an edge of the die. These configurations are illustrated in Figure 2.15. The placement of the gate connection pad is important, as it can affect the switching capabilities of the IGBT, since the neighboring active area cells will react to the gate signal prior to faraway sections.

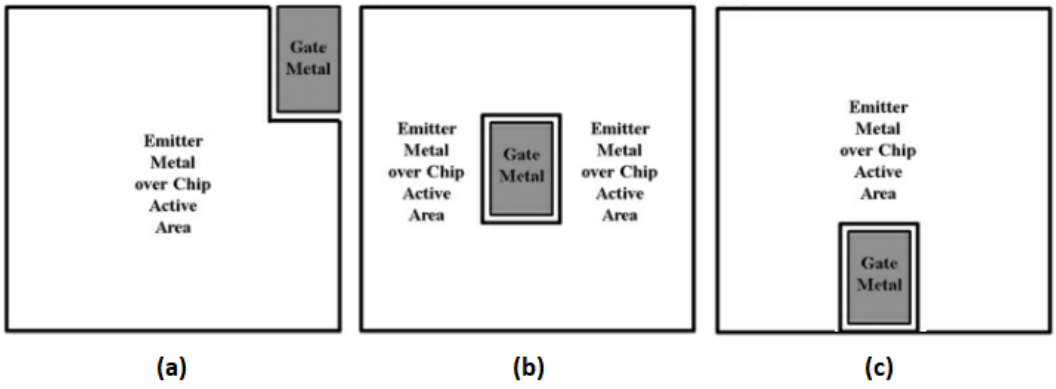


Figure 2.15 – Gate Metallization Configurations (a) Corner (b) Centre (c) Edge [5]

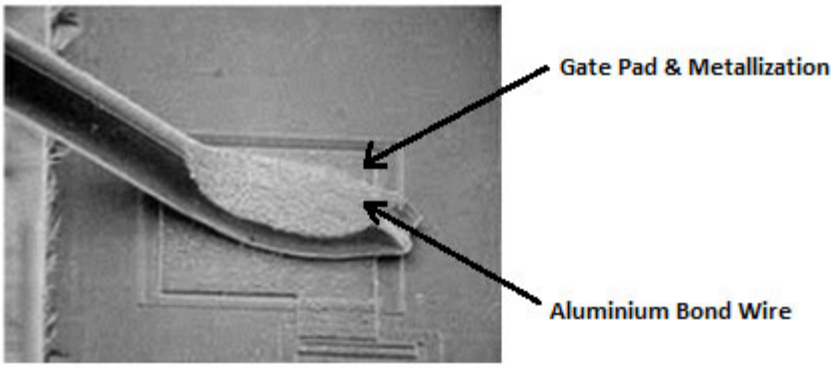


Figure 2.16 – Gate Pad & Metallization and corresponding Al Bond Wire [5]

Figure 2.16 illustrates zoomed imagery of a gate pad and corresponding metallization connected to the gate bond wire. The gate bonding pad size depends on the cross-sectional area of the bonding wire. For example, for aluminum alloy bonding, the gate pad width is commonly taken twice the diameter of the bond wire, while the length is taken three times as much [5].

The emitter is commonly connected to the package lead through the utilization of several bonding wires, which are allocated throughout the active area of the die. Hence, the emitter metallization design considers a matrix formation throughout the active area, as illustrated in Figure 2.17. This ensures a more homogenous current distribution throughout the emitter metallization and through the different bonding wires, hence avoiding emitter current build-up and the formation of "hot spots" [5], [6].

On the other side of the vertical IGBT structure, the collector metallization has several functions. Firstly, it is utilized as an electrical connection between the collector and the package lead. Secondly, it channels the thermal flow from the die to the package. Thirdly, it serves as an adhesive between the die and the solder layer. Moreover, other layers are deposited on the collector metallization, protecting against contamination through particle diffusion or oxidization [65].

IGBT chip size is defined through dicing which is performed by saw blades. Dicing has the tendency to damage the silicon and hence it is required to split up the junctions of the active area of the IGBT from the borders of the chip. Hence edge terminations are required between the IGBT's active area and the dicing lanes.

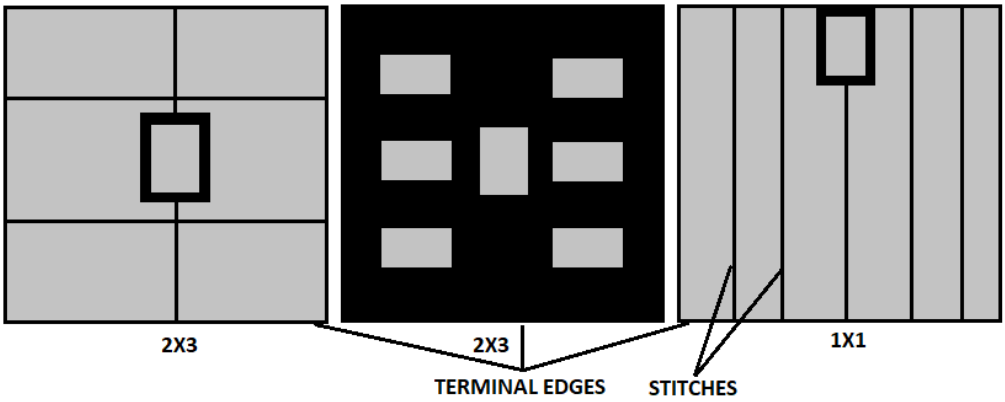


Figure 2.17 - Emitter metallization matrix designs [65]

Edge terminations design has an impact on the stand-off capability of the IGBT. They are commonly constructed using processes employed to create the IGBT cells themselves. Hence P^+ region employed within the IGBT cell structures is commonly utilized to make the edge terminations, through the utilization of floating field rings and field plates as illustrated in Figure 2.18. Since IGBTs are mainly intended for operations with high breakdown voltages, several floating field rings and field plates are utilized, with the employment of these structure increasing with increasing breakdown voltage capability [5], [6].

2.5.4 IGBT Packaging and Modules

The IGBT's package plays a very important part in the correct operation and reliability of the device, as it serves as the boundary between the raw semiconductor and the external circuitry. The device package plays a critical role in the actual determination of the device's limits and hence has a direct impact on the safe operating area (SOA) of the IGBT. The IGBT packaging provides; the electrical interconnections for one or multiple IGBT chips, the path for heat extraction from the IGBT chip to the environment, segregation of the high voltages from crucial low voltage parts, and mechanical sturdiness to the device.

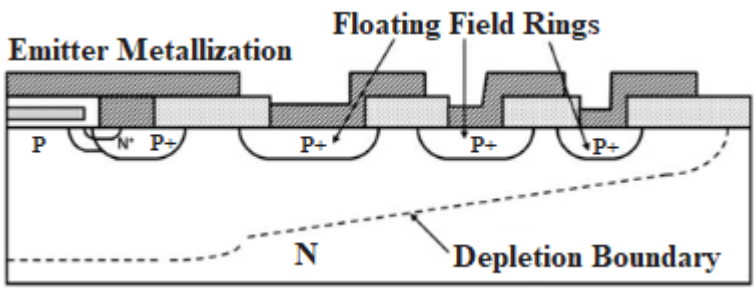


Figure 2.18 – Side View of Planar Gate IGBT Edge Termination Design [5]

IGBTs are generally packaged either as discrete power devices or as multi-chip power modules. In the latter, several IGBTs' and free-wheeling diodes' dies, are integrated in the same device forming power electronic building blocks such as half bridges, full bridges, hex bridges, choppers etc.

The following is a list of sub-components and processes commonly utilized in IGBT packages, which is illustrated in Figure 2.19:

- Die-Attach – It involves the placement of the semiconductor die (during fabrication process it is managed on a wafer frame) on a metal substrate. The attachment is conducted through the utilization of either epoxy, solder or eutectic[1] process. The die-attach has three main purposes within an IGBT package: It fixes the semiconductor die, hence providing mechanical assembly; It provides an electrical connection to the die bottom; It channels heat away from the die. Materials commonly utilized for die-attach are PbSnAg alloy based. Lately other materials which are lead free such as $Sn_{96.5}Ag_{3.5}$ were introduced for power devices [68], [69].
- Top-Die Interconnections - They provide electrical connection to the top IGBT contacts namely, the gate pad and emitter pads. Commonly, Aluminium (Al) wire bonding is utilized for these interconnections, even though contacts such as metal bumps or pressure-type contacts have been employed [5], [68].
- Thermally Conductive & Electrically Insulative Substrate – This layer provides the required support, for the die, die attach, interconnections, and terminals. The substrate must be electrically insulative as it provides electrical isolation between sub-module terminals. Furthermore, it must be thermally conductive as it must provide a path for heat to be extracted from the die. The most common solution for high power devices is a structure consisting of a ceramic substrate sandwiched between two copper (Cu) layers. Aluminium Oxide (Al_2O_3), Aluminum Nitride (AlN), Silicon-Nitride (Si_3N_4), Berillyium-Oxide (BeO) are common ceramic materials utilized for this purpose. This substrate technology is referred as Direct Copper Bonding (DCB). For medium power devices the substrate structure will consist of a ceramic-filled polymer (commonly epoxy) sandwiched between two Aluminium (Al) layers. This substrate technique is referred as Insulated Metal Substrate (IMS) [65], [68].

[1]Eutetic is a solder alloy that melts at a single temperature, lower than the melting point of its constituents.

- Encapsulant – This is commonly conformal coating and is utilized to protect the die and ancillary components from environmental contamination, while providing a mechanical protection. Thermoplastic materials such as epoxies and silicones are utilized for this purpose [68].
- Base Plate – The main purpose of the base plate is to distribute heat through conduction to the external passive or active heat sink. Moreover, the base plate provides mechanical support to the device. Copper (Cu) plates coated with Nickel (Ni) are typically utilized for this purpose. Other composite materials have been also employed such as Copper (Cu) plates reinforced with diamond and Aluminium (Al) plates reinforced with Silicon-Carbide (SiC). Composites provide the advantage of tweaking and providing similar thermal coefficient and thermal expansion coefficient of the base plate in relation to the silicon and substrate. [68], [70].
- Pins & Terminals – They provide the electrical connections from the IGBT to the external circuitry. Copper (Cu) is the material commonly used for pins and terminals. Solutions utilizing press pack Molybdenum (Mo) plates or spring-loaded pins, have been employed as well. [68], [71].
- Cover or Case – This is the plastic structure which houses and protects the entire device.

Going through two practical examples of IGBT packages. The first example is the packaging of a discrete IGBT in a TO-220 package, where the semiconductor device is soldered via the die-attach to a copper flange acting as substrate, collector terminal and baseplate. The source and gate terminals are connected from the copper leads to the top mounted die aluminium gate and source pads via aluminium wire bonding. Apart from the base plate, everything is encapsulated with ceramic filled epoxy, providing electrical insulation, environmental protection, and mechanical support.

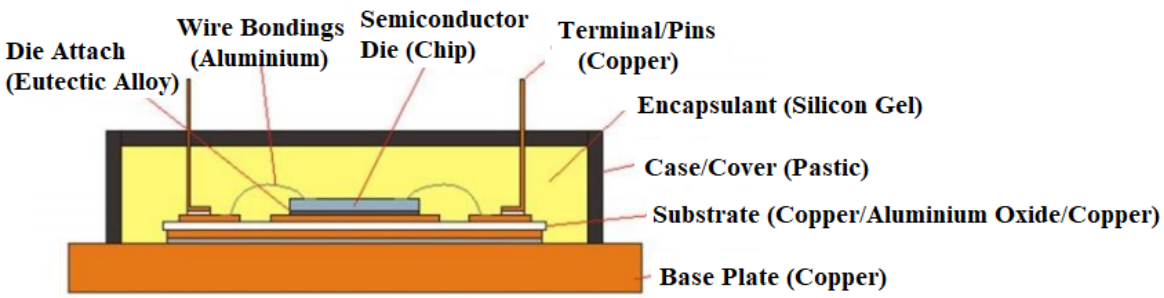


Figure 2.19 - Generic IGBT Package Structure [68]

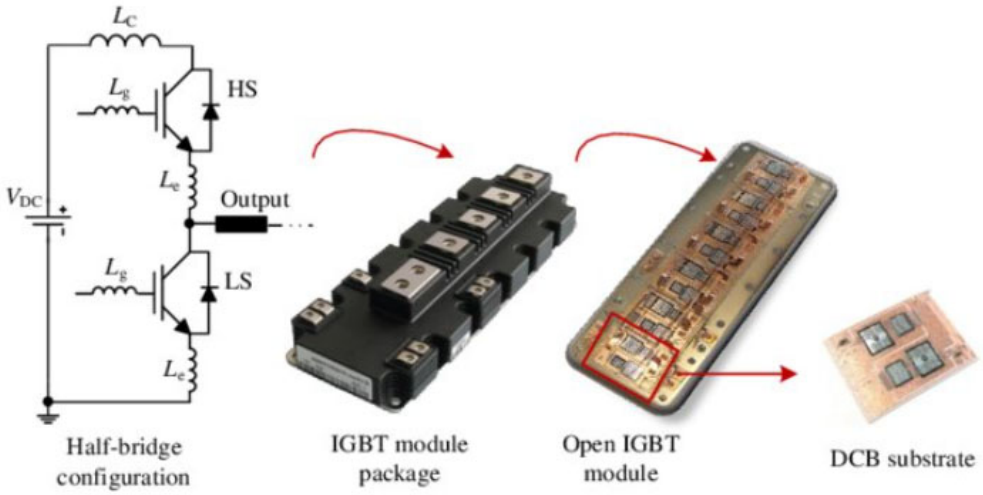


Figure 2.20 – 1.7kV/1kA Half-Bridge IGBT Module and corresponding DCB [72]

In the case of IGBT modules, with multiple semiconductors dies (IGBT chips and free-wheeling diodes chips), these are connected via wire -bonding. In this scenario a DCB substrate is utilized for both the IGBT and the free-wheeling diodes[1] providing the necessary electrical insulation, good thermal conductivity, and mechanical sturdiness. Eutectic soldering alloy is utilized as a die attach between the semiconductor and the DCB [65], [68] and [72]. Figure 2.20 illustrates a 1.7kV/1kA IGBT module with an internal half bridge configuration highlighting an IGBT module on the corresponding DCB.

2.6 Literature Reporting IGBT Failure Mechanisms, Effects and Analysis

As discussed so far, the construction of an IGBT, ranges from the raw semiconductor up to the package construction. It involves multiple chemical, electrical, and mechanical processes and hence the employment of various materials. Even though at face value an IGBT can appear as a simple electronic structure, the fact that it is employed at elevated power scenarios, the listed sub-structures can be prone to multiple failure mechanisms which can lead to the general IGBT failure. Hence this section will go through the reported IGBT failure mechanisms found in literature, discussing further the corresponding effects and analysis. Different literature goes through the topic of IGBT failure, failure diagnostics and prognostics [67], [73-81]. Ciappa [73], provided a thorough overview of IGBT wear out failures namely, bond wire fatigue, substrate cracking, interconnections corrosion and solder voiding. Here, the discussion focused on the IGBT latch-up and bond-wire lift-off mechanisms.

[1]*Free-wheeling diode is connected across an inductive load, to eliminate the sudden voltage transient seen across the load, when the load current is abruptly reduced or interrupted.*

Marginal discussion was included to more single event catastrophic failure mechanisms. Another IGBT failure mechanisms review was conducted by Busca et al. [74]. This study reviewed IGBT failing mechanism associated with bond wire lift-off, solder voiding and fatigue, bond wire cracking due to non-uniform thermal expansion coefficients and failures induced due to cosmic rays[1]. Moreover, this study reviewed IGBT failing modes mainly associated with IGBT modules such as fretting, corrosion, spring fatigue and relaxation, and failure of press-pack. Another similar review was conducted by Yang et al. [75], delving also in diagnosis and prognosis methods to determine the health state of the IGBT. Patil et al. [81] conducted a thorough Failure Mode Effect and Analysis (FMEA) of IGBT related failures, correlating failures mechanisms, to failure causes, modes, and failure area within the IGBT. Flicker et al. [76] provided a detailed review of all the wear out failure mechanisms, as well as catastrophic short circuit failures. On the other side marginal second breakdown and open-circuit failures were covered in this study. Wu. et al. [80] provided a detailed review of all the major types of IGBT failures addressing predominantly the catastrophic failures triggered due to overstress, including second breakdown and open circuit failures. Moreover, this study discussed the design of fault tolerant power electronic converters, utilizing IGBTs. A more complete and updated review of IGBT failure mechanisms was conducted by Abuelnaga et al. [67]. This study short listed the different failure mecahnisms and analysis, and different test setups to perform accelerated degradation. Finally, it reviewed the different diagnostic IGBT parameters indicating failure, and the corresponding lifetime modelling found in literature to determine the IGBT health state. Generally, the trend through the above literature is to divide these IGBT failures into two main categories; failures which are related to the IGBT die, and failures which are related to the IGBT package.

2.6.1 IGBT Die Related Failure Mechanisms, Effect and Analysis

IGBT die failure mechanisms manifest mainly due to two failure scenarios. The first failure scenario is mainly due to the different PoF wear-out phenomena (namely electro-migration and hot carrier degradation) described in Section 3.1 and Section 3.2, respectively. This failure is mainly induced through accumulated degradation over time. The second failure scenario is mainly due to electrical, thermal, or electromagnetic overstress. These are single event scenarios which lead to more abrupt and catastrophic failures. Hence the first scenario is more progressive and mainly related to degradation hence tending to alter IGBT characteristics

[1]*Cosmic Rays are atomic fragments that irradiate Earth from the sun and outside of the solar system. They travel at nearly the speed of light and have been blamed of inflicting damage to electronics.*

and performance prior to failure. While the second scenario is more catastrophic predominantly leading to abrupt failure.

2.6.2 IGBT Die Catastrophic Overstress Failure Mechanisms

IGBTs electrical overstress, is mainly related to over-voltage or overload events. Over-voltage scenarios can be input related, that is an overvoltage at the gate, hence deteriorating or breaking down the gate dielectric. Moreover, it can be an output overvoltage that is exceeding the allowable maximum collector to emitter voltage (V_{CE_MAX}). Overload scenarios is related to an excessive collector current (I_C). Thermal overstress is related to the fact that the IGBT's junction temperature exceeds the maximum allowable junction temperature (T_{J_MAX}) hence exceeding the maximum allowable power dissipation (P_{D_MAX}). Electromagnetic overstress is related to the scenario where the device is radiated with electromagnetic energy leading to device characteristics change and eventually burnout. Cosmic-rays radiation is an example of such electromagnetic overstress.

Overvoltage scenarios at the gate lead to input gate capacitance dielectric deterioration which if severe it can lead to gate dielectric breakdown. This leads to the complete loss of gate control and hence control on the IGBT switching and therefore it can manifest as either an open or short circuit fault depending on the operation. Gate dielectric breakdown can predominantly manifest during inductive switching due to excessive dV/dt [82]. Overvoltage scenarios at the output of the IGBT can lead to the device primary breakdown. Initially if the overvoltage is less severe it will manifest itself with an increased forward trans-conductance (g_m) of the device, as for the same gate drive there will be an increased manifestation of collector current (I_C). This is due to the Early Effect of the IGBT's output BJT structure. Moreover, this will also deteriorate the blocking voltage capability of the device. If the output overvoltage is more severe, it can lead to avalanche breakdown, which if uncontrolled, it will lead to device's punch-through, manifesting in an IGBT short circuit [83].

Latch-up is a failure mechanism where the output collector current can no longer be dictated by the gate voltage (V_G). This happens when the parasitic thyristor structure of the IGBT is triggered. IGBT latch-up can be divided into two categories static latch-up and dynamic latch-up. Static latch-up manifests during high continuous collector current (I_C). This causes enough voltage drop across the parasitic drift region resistance (R_{DRIFT}) to trigger the IGBT's parasitic thyristor structure. Dynamic latch-up occurs during the IGBT turn-off when the parasitic thyristor structure is triggered through the collector junction capacitance (C_J) displacement

current. This is mainly caused during two possible scenarios. The first scenario is when the gate voltage (V_G) decreases rapidly. This induces enough displacement current in the gate oxide which flows though the parasitic drift region resistance (R_{DRIFT}), developing enough potential difference to trigger the parasitic thyristor. The second scenario is caused by high off-state voltage which due to large output voltage rate of change (dV_{CE}/dt), enough current is again induced to flow through the parasitic drift region resistance (R_{DRIFT}). All the above three circumstances can lead to latch-up, hence losing the ability to switch the device off, and is generalized by a low-ohmic short-circuit of collector, emitter, and base, causing thermal runaway and device destruction [5], [73], [84-86]. It is important to highlight that newer generation IGBTs namely the Trench Field Stop technology offers enhanced immunity to latch-up failure [87].

Secondary Breakdown is a breakdown mechanism which mainly manifests in power BJTs and hence inherently in IGBTs too. It is mainly related to the combined conditions of high collector current (I_C) and collector-emitter voltage (V_{CE}), where the current tends to concentrate in localized spots. This leads to localized heating (hotspots), which eventually progresses to a short between the collector and emitter, leading to device destruction. During secondary breakdown, the collector-base junction space-charge density of the output BJT increases. This decreases the breakdown voltage stand-off capability of the IGBT, increasing further the current density. This progresses until at localized areas, the high current density is so large that the local temperature increase, due to self-heating, leading to a short circuit and hence to the abrupt collapse of the collector-emitter voltage (V_{CE}) [80]. This IGBT failure mechanism has been modelled and measured by Shen et al. [88]. During on-state, IGBTs can experience instantaneous short circuits especially during high power dissipation. This circumstance is referred as Energy Shock (ES) [80] which leads to high junction temperatures. Even though ES can drive the junction temperature (T_J) above the maximum junction temperature (T_{J_MAX}), this will not destroy the device. The IGBT will fail, if the junction temperature (T_J) reaches the temperature when the semiconductor on either side of the junction becomes intrinsic by temperature. This happens when the intrinsic carrier concentration (n_i) is equal or greater than the majority carrier concentration for either the N or P side of the junction. Hence, the higher the doping level, the higher the temperature at which this condition occurs (for silicon with majority carrier concentration (N_M) of $1x10^{15}cm^{-3}$ the temperature at which the semiconductor becomes intrinsic (T_i) is around 260˚C, but for $N_M = 1x10^{19}cm^{-3}$, $T_i \approx 1325°C$ [256]). This occurs since at these elevated temperatures all silicon impurities will become ionized.

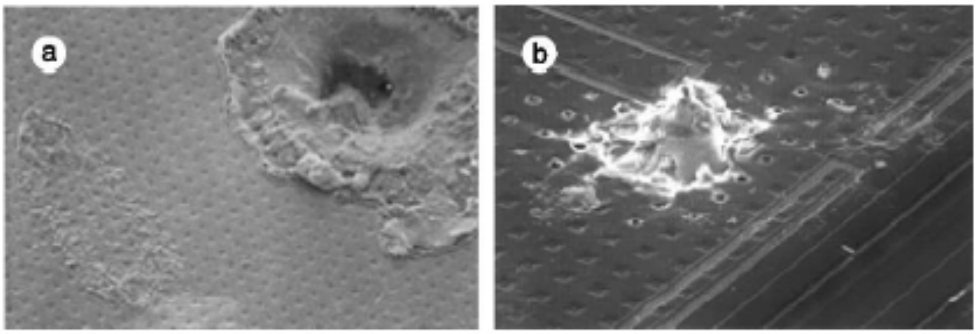


Figure 2.21 - Scanning Electron Microscope (SEM) Imagery of IGBT (a) Melted Pit due to Latch-up with Bond-Wire Lift Off (50 × Magnification) (b) Melted Pit due to Latch-up but affecting less dies than in (a) (90 × Magnification) [73]

In this scenario, there will be an exponential increase of electrons jumping from the valence band to the conduction band resulting in an exponential increase in the conductivity leading to thermal runaway. If the junction temperature is increased further the IGBT cell will be irreversibly damaged [80]. Hence this indicates that short circuit ES scenarios do not imply immediate IGBT destruction. In fact, Lefebvre et al. [89], proposed the concept of Critical Energy (CE). This study showed that an IGBT can survive thousands of short circuits but with short circuit energy, controlled below the CE value. On the other hand, if the short circuit energy content is substantially above the CE value, the IGBT will fail after the first short circuit. Furthermore, this study showed that IGBTs were able to switch-off after a short circuit, if the short circuit energy was below the CE value, but immediately failing the off commutation, if the short circuit energy was higher than the CE value. Determining the exact value of the CE is non-trivial and varies according to the device's characteristic capabilities. In literature it was mainly approximated through experimentation [90]. Overload scenarios will mainly manifest in bond-wire lift off, bond wire cracks and bond wire ruptures. Bond-wire lift-off is the detachment of the bonding wire from the corresponding IGBT die pad. Bond-wire cracks is the formation of cracks and hence the increased resistance of the bonding wire. It predominantly manifests in the vicinity of the die terminal, especially at the wire-bond heel (heel cracks) and at the wire bond edge (edge cracks). Bond wire rupture is the sudden breaking of the bond-wire, referring mainly to a break along the length of the bond-wire. All the above bond wire failure mechanisms, manifest predominantly but not exclusively due to thermally induced stress (in the case of overload, heat generated due to high current flow) arising from the mismatch in the coefficients of thermal expansion of the materials employed, leading to an increased wire resistance eventually open circuiting the IGBT [73], [91 - 92]. Figures 2.22 and 2.23 are respectively evidencing bond wire lift off and bond wire cracks scenarios.

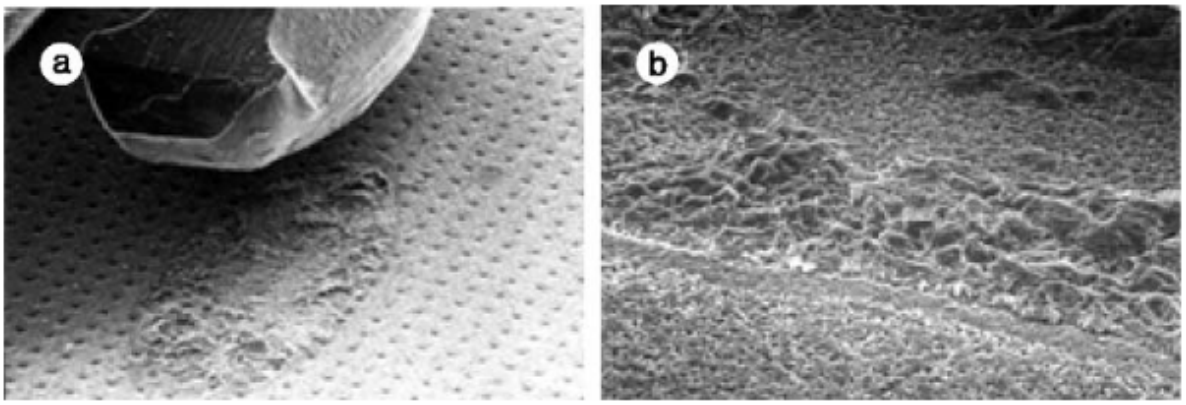


Figure 2.22 – Scanning Electron Microscope (SEM) Imagery of (a) Al Bond-Wire Lift-Off (40 × Magnification) (b) Al Bond-Wire Footprint after Lift-Off (100 × Magnification) [73]

Electrostatic Discharge (ESD) can also contribute to IGBT's catastrophic overstress. In general, ESD is particularly hazardous to gated devices as it can partially puncture the dielectric oxide. Due to the IGBT's large input capacitance, it can absorb more charge before reaching gate-breakdown voltage. Hence, ESD in IGBT, does not necessarily lead to immediate failure, but it can be enough to trigger early-life failure. On the other side, if through ESD, gate-breakdown is reached there is enough energy stored in the input capacitance, which can perforate the gate oxide. ESD gate failure has been reported in literature especially when no ESD protection was provided with the gate drive circuit [93].

External radiation can affect both BJTs and MOS devices and hence IGBTs too, and therefore can lead to device destruction. IGBT Single Event Burnouts (SEB) due to cosmic rays' heavy ions, was reported by Busca et al. [74] and Nishida et al. [94]. Through reactions between high energy neutrons and silicon atomic nuclei, IGBTs suffered significant characteristics alterations leading to device destruction.

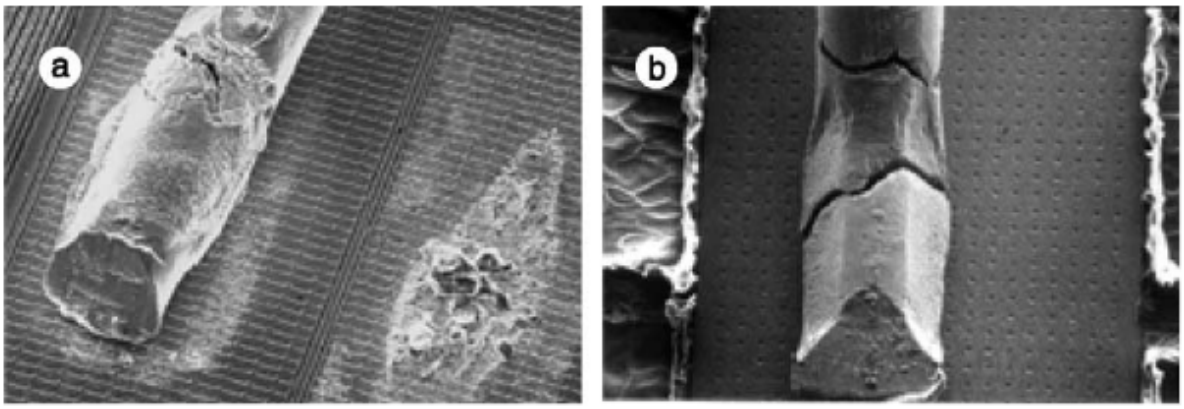


Figure 2.23 - Scanning Electron Microscope (SEM) Imagery of Bond Wire (a) Heel Cracks (25 × Magnification) (b) Heel Cracks & Edge Cracks (25 × Magnification) [73]

2.6.3 IGBT Die PoF Wear-out Mechanisms

As already discussed, IGBT die PoF wear-out failure mechanisms are mainly related to the progressive degradation of the IGBT's sub-components, and hence manifests with the progressive IGBT's characteristic alterations prior to failure. The physics related to these phenomena has been already described in Sections 2.1 and 2.2. In relation to IGBT die, PoF wear-out failures can be mainly categorized into Hot Carrier (HC) effects and electromigration (EM) effects.

HC degradation mainly manifests in IGBTs either through HCI or through TDDB effects. These are due to ionic contamination and mainly manifests in IGBTs as electric field distortion, through the accumulation of ionic contaminants in the passivation of the high-field region. Moreover, it manifests also as defects within the gate oxide. During enhanced temperature applications hot carriers are injected within the gate oxide ending up as trapped charge, degrading the insulative properties of the dielectric. In IGBTs, HC effects are nearly never catastrophic, mainly due to the large thickness of the oxide. Its main effect is mainly related to altering the IGBT performance by changing parameters such as the threshold voltage (V_{THRES}), forward transconductance (gm), leakage and saturation current and on-state saturation voltage (V_{CE}_sat). Hence HCI degrades the performance of the device as the above parameters contribute to the device's continuous and switching losses as well as the switching speed [75],[81], [95].

Another IGBT PoF wear-out mechanism is EM. This causes atomic migration and is mainly related to the metallization of the IGBT. This phenomenon is nearly never catastrophic due to the relatively large metallization areas, but it tends to affect the long-term reliability of the IGBT. In relation to IGBTs, EM mainly manifests due to the high currents involved, and contributes to the migration of the die pads metallization and within the aluminium bond wires. This was mainly observed during repetitive short-circuit and high temperature tests leading to a decrease in the conductivity [96]. Moreover, IGBTs operated under high voltage, high temperature and in humid environments tend to manifest atomic migration at the die passivation layer and die pads structures. This contributed to an increase in leakage currents and gradual loss of blocking capability [97-98].

2.6.4 IGBT Package Related Failure Mechanisms, Effects and Analysis

IGBT package related failure mechanisms are mainly due to thermal overstress, thermal shocks, thermal runaways, mechanical shocks, thermo-mechanical fatigue, thermo-mechanical creep, corrosion, and humidity. These will contribute to bond-wire lift-off, bond-wire cracks, bond-wire ruptures, solder delamination, solder cracking, and degradation of the die metallization [73-77]. Bond-wire lift-off failures are caused at the wire-die interface during temperature swings and happens due to the different thermal expansion coefficients of aluminium (Al) and silicon (Si). Hence, strain difference in the two materials causes stress at the materials interface resulting in the production of cracks at this point. The crack severity and propagation, depend on the temperature and thermal cycling. Cracks propagation will eventually lead to lift-off. [73], [77]. This is considered a major package failure mechanism and is illustrated in Figure 2.22. Scanning electron microscopy (SEM) is utilized to detect such failure mechanism even though other tests such as the measurement of the on-state collector-emitter saturation voltage (V_{CE_SAT}) has been utilized for this purpose [102]. Depending on the severity of the thermal cycling swing, strain at the interface, and the temperature itself, the failure can progress up to the rupture and melting of the bond wires. A secondary scenario related to bond-wires lift-off can be the induction of currents in closely spaced bond-wires. This leads to the uneven distribution of current between the different dies which can progress to bond-wire lift-off. This latter effect was observed by Xing et al. [101].

Another package related failure is solder fatigue, solder cracking and solder voids. These occur at the solder alloy between the IGBT die and substrate and between the substrate and the base plate. Again, this failure arises due to a difference in the thermal expansion coefficients of the different materials involved. The most critical interface is considered the solder alloy between the ceramic substrate and the base plate especially for copper base plates [73]. This is mainly because it is this location that presents the largest difference in the thermal expansion coefficient. Due to IGBT heating, different strain levels will develop at the materials interface, causing a net strain and subsequently stress. The resulting stress at the solder interfaces contributes to solder fatigue and hence to the manifestation of solder cracks and solder voids. These will be responsible for the enhanced thermal resistance of the die-attach, since there will be smaller solder area for heat to be removed by conduction, contributing to localized die heating. This is illustrated in Figure 2.24, showing X-Ray imagery of degraded die-attaches of IGBT dies, and corresponding free-wheeling diode dies.

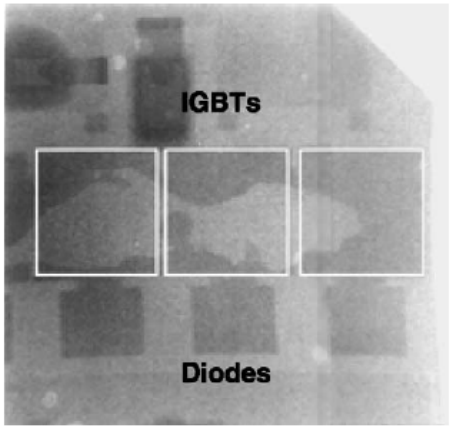


Figure 2.24 - X-Ray Imagery evidencing IGBT dies and corresponding free-wheeling diode dies, die-attach voiding and melting [73].

This process enhances the average temperature of the die which in-turn will contribute to further die-attach voiding and melting, leading to die failure. [73], [99-100]. Since IGBTs are vertical devices, the die-attach has the combined role of removing heat from the die and connecting the die electrically. Hence, from a diagnostic point of view, the most difficult die-attach cracks and voids are those which deteriorate heat flow to the heat sink but without noticeably degrading the current distribution and flow in the semiconductor. These situations are mainly manifested when cracks and voids develop at the edge of the die-attach [73]. Moreover, solder fatigue, cracks and voiding facilitate thermal runaway. This leads to the melting of the package interconnects, the further proliferation of cracks and voids at the solder layers, as well as die-metallization degradation [75].

In relation to the die-metallization degradation, again, this happens due to the difference in the thermal expansion coefficients of the stiff silicon die and the thin aluminium metallization layer leading to aluminium reconstruction. This occurs predominantly during power/thermal cycling, where periodic compressive stresses and tensorial stresses will contribute to the exceeding of the elastic limit of the aluminium metallization layer. The level of degradation is directly dependent on the rate of change of temperature, which for typical IGBT applications it will correspond to thermal transients' time constants in the range of milliseconds to tens of milliseconds. This leads to aluminium grain boundary cavitation hence aiding the proliferation of aluminium crack growth, as well as grain extrusion, leading to an uneven aluminium metallization layer topography. These processes aid to the thermal and predominantly electrical degradation of the IGBT's metallization layers as well as enhances EM effects [73]. This is illustrated in Figure 2.25, highlighting aluminium metallization topographic extrusion and the proliferation of voids at the larger grains, after the IGBT was subjected to power cycling.

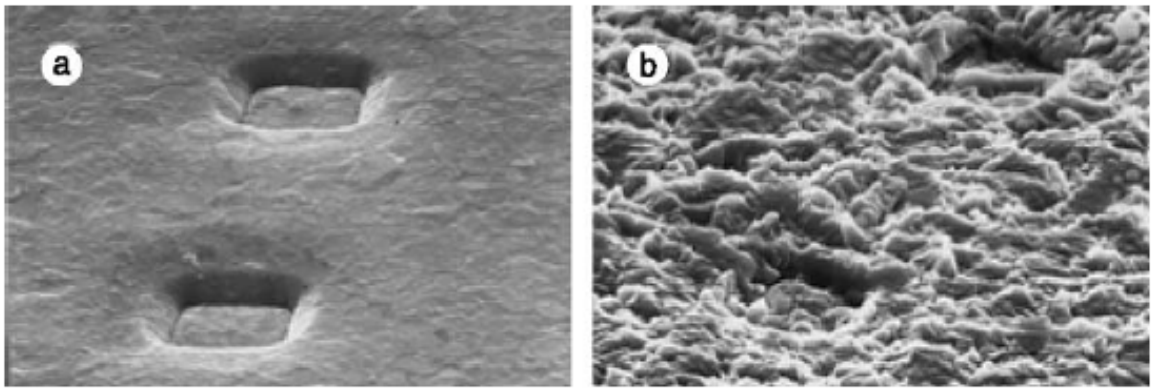


Figure 2.25 - Scanning Electron Microscope (SEM) Imagery of Emitter Metallization of IGBT (a) Before Power Cycling (1000 × Magnification) (b) After Power Cycling with temperature between 85 ˚C and 125 ˚C highlighting Grain Extrusion (1000 × Magnification) [73]

Corrosion is another failure mechanism, mainly affecting the aluminium bond wires. Aluminium corrosion occurs when it is exposed to oxygen. In this circumstance, the aluminium grows a thin layer of Aluminium Oxide (AlO) which coats the metal. It has been identified that galvanic corrosion mechanisms such as bimetallic corrosion, pitting corrosion, stress corrosion and dealloying are the predominant mechanisms which affect the different metallic structures of an IGBT [73]. The catalyst to such corrosion is still not fully understood as there can be multiple simultaneous sources, even though thermo-mechanical stresses has been strongly correlated to bond-wire corrosion [77]. Corrosive chemicals within the industrial application can also contribute to the deterioration of bond-wires. Moreover, high levels of humidity tend to degrade the Silicon-gel which the bonding wires are embedded in [103]. The degradation of the Silicon-gel and the Silicon-gel itself have been considered possible corrosion sources. In general, aluminium corrosion leads to bond-wire connection degradation, deteriorating the bond conductivity, and may lead to bond-wire rupture. This is illustrated in Figure 2.26.

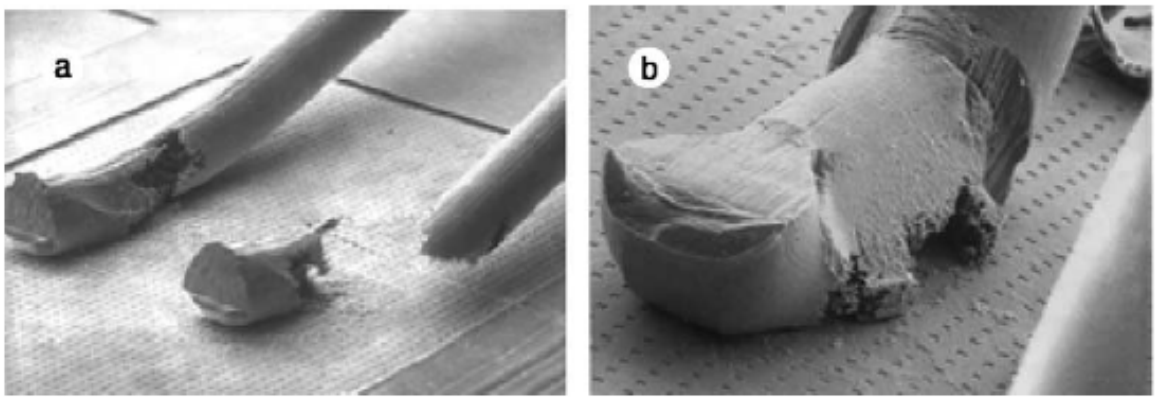


Figure 2.26 - Scanning Electron Microscope (SEM) Imagery of (a) Ruptured Emitter Bond due to Stress Corrosion (30 × Magnification) (b) Emitter Bond Corrosion (80 × Magnification) [73].

2.6.5 IGBT Application Related Failure Mechanisms, Effects and Analysis

Apart from the failures related to the inherent solid-state and package structures, IGBTs can be subjected to failure mechanisms which are triggered by the application or field where the device is employed, manifesting in failures which have been described in subsections 2.6.1 to 2.6.5. Application failures can be triggered due to electrical, mechanical, thermal, and chemical faults. Collector-Emitter (V_{CE}) overvoltage can be due to errors in measurement signals and control signals. Furthermore, it can be due to coupled surges. High overvoltage transients can be caused by high rate of change of falling collector current (I_C) through the application circuitry stray inductances [103]. This can destroy the IGBT especially during repetitive transients. Such overvoltage transients might damage one or few IGBT dies leading to high localized temperatures, as the neighboring dies will have to carry the current of the destroyed cells. This can lead to the overall failure of the IGBT. The gate too can be subjected to application related fault scenarios such as gate surges, gate driver failures, and gate signal instability especially during short circuits [80]. IGBT overload scenarios can happen too due to external faults, such as improper gate firing as well as unexpected dynamic low load events. Application related thermal faults play a significant role in compromising the integrity of IGBTs. These mainly manifest during elevated operational temperatures, thermal shocks or during power cycling leading to thermal cycling. These events may not immediately destroy the IGBT but tend to impact the long-term reliability of the device. The thermal issues can be due to a variety of root causes such as improper heat sink design, improper active cooling, insufficient gate voltage hence not properly switching on and off the IGBT contributing to elevated static-losses, and improper switching speeds leading to elevated dynamic losses [67], [104].

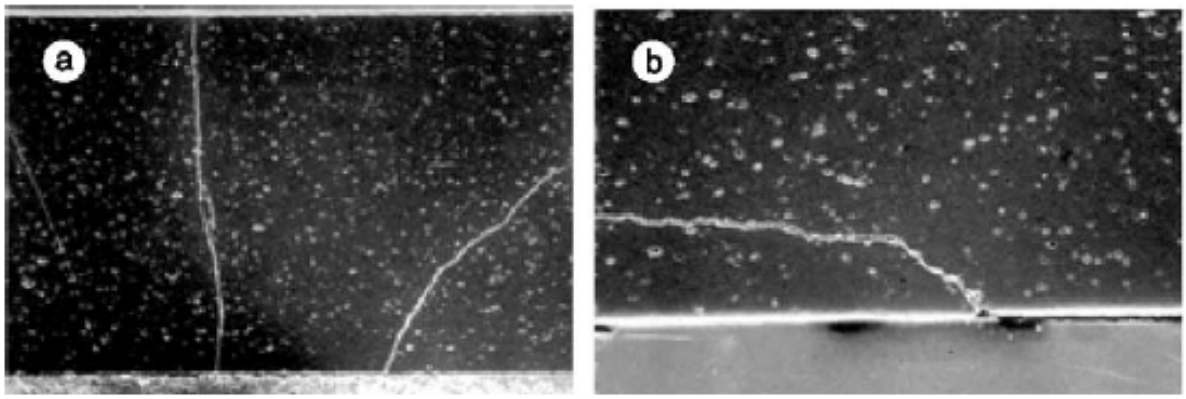


Figure 2.27 - Scanning Electron Microscope (SEM) Imagery of Al_2O_3 ceramic layer (a) Vertical Crack (400 × Magnification) (b) Horizontal Crack (600 × Magnification), due to Bending [73].

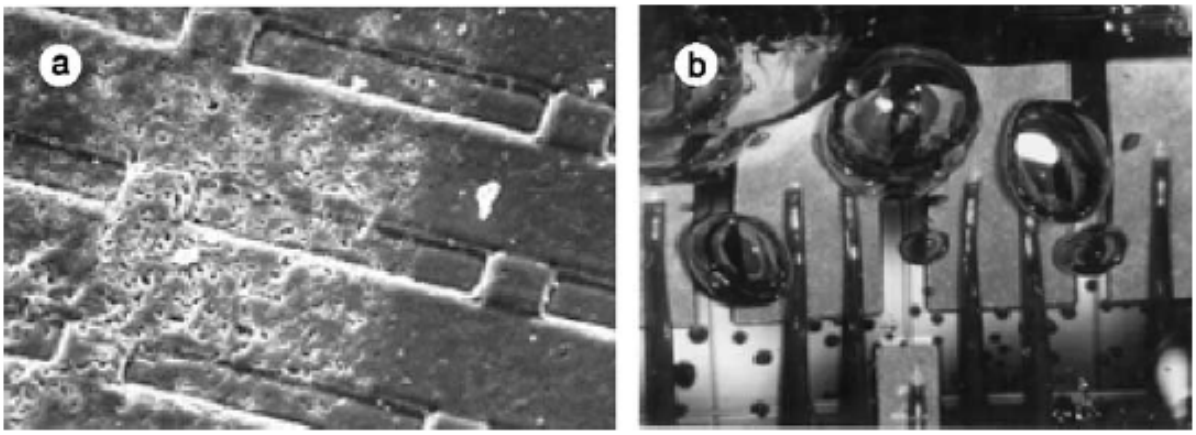


Figure 2.28 – (a) Scanning Electron Microscope (SEM) Imagery Emitter corrosion (160 × Magnification) (b) Optical imagery infiltrated gas in Si-Gel (8 × Magnification) [73].

In relation to mechanical stress, application vibrations and bending may contribute to the cut-off of bond-wires as well as cracks in the ceramic layer [73]. This is illustrated in Figure 2.27. Chemical and environmental corrosion contribute too to application related failures. Build-up of salts and other deposits of conductive chemicals at the IGBT terminals and or at the gate driver can cause insulation breakdowns, flashovers, short-circuits, and improper switching of the gate. Moreover, humidity can aid external particles to infiltrate the IGBT, which can deteriorate the internal wire-bonding and the Si-gel [73], [105].

2.6.6 Combining IGBT Failure Mechanisms

During operation, IGBTs will rarely manifest a single failure mechanism, but rather tend to manifest multiple failure mechanism. Simultaneous failures will aid each other in the overall degradation of the IGBT. The following are examples of combined failure mechanisms, effects, and analysis.

The first example highlights the failures interaction between the solder alloy degradation and bond-wire degradation. When both failures are present, they will aid each other in accelerating the overall failure of the IGBT. When the solder layer integrity is compromised, the overall die temperature and die temperature variation will increase. In this manner, it will also accelerate the degradation of the bond-wires. The two failures will keep alimenting each other, until there is the overall destruction of the IGBT. Held et al. [105], showed that bond-wire lift-off will start later when it is only due to bond-wire degradation, rather than the combined solder layer and bond wire degradation.

Another example of the effects of combined failures, considers the combination of metallization degradation and bond-wire degradation. Die metallization deterioration will decrease the conductivity of the metallization layer. This leads to an increase in the on-state collector emitter saturation voltage (V_{CE_SAT}). This will enhance the on-state power losses which in turn will increase the die temperature and die temperature fluctuations, eventually deteriorating the bond-wire, where this latter effect will aliment a further increase in die temperature and die temperature variations, deteriorating further the metallization layers. This leads to a vicious, runaway failure process. Hence the combination of bond wire degradation, solder degradation and metallization degradation will lead eventually to more severe scenarios.

A third example of combined failure effects involves the combination of bond-wire lift-off, bond-wire cracks, and corrosion, which increases the current density in the remaining non-degraded wire-bonds. This enhanced current density will increase the EM effects, which will lead to a decrease in the conductivity of the remaining bond-wires. This will in-turn increase the bond-wire temperature eventually leading to bond wires melt down or rupture. Moreover, the above may lead to localized temperature rise in the bond-wire pads, which will in-turn can cause localized melt-down and voiding in the metallization near the bond-wire pads of the remaining bond-wires [107-109]. Tables 2-1, 2-2 and 2-3 provides a detailed FMEA summary of all the different IGBT failures categorized and explained according to the different sub-sections within Section 2.6.

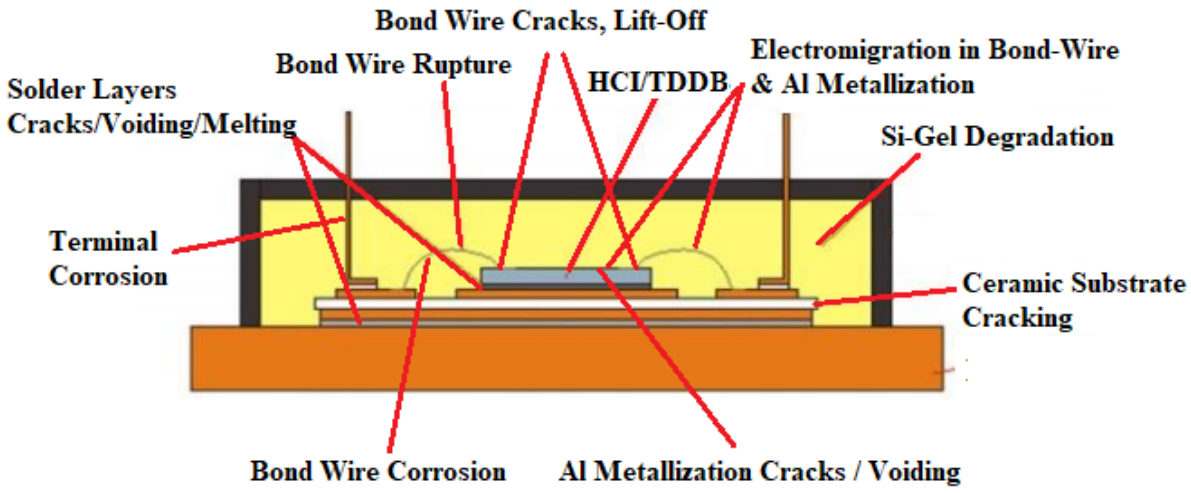


Figure 2.29 – IGBT Failure Mechanisms and Corresponding Locations

Failure Mechanism	Failure Cause	Failure Manifestation	Failure Location
Gate Overvoltage **[80], [82]**	Gate Drive Failure Inductive Switching Gate Protection Failure	Predominantly Open Circuit Failure. Possible Short Circuit Failure that can lead to Thermal Runaway. Gate Oxide Degradation. Gate Oxide Breakdown.	Gate Oxide
High Voltage Breakdown **[67], [80], [83]**	Inductive Switching. Measurement Error in V_{CE}. Gate Drive Control Error.	During turn-off: VCE collapses and IC rises after voltage spike. During turn-on: peak I_C results in destruction. Increased Transconductance (g_m) Early Effect. Decreased Blocking Voltage Capability. Primary Avalanche Breakdown (Short Circuit Failure). Thermal Runaway: Overheating of peripheral cells, spreads to the whole die.	Periphery of the Die Area, eventually effecting the entire die area.
Latch-Up **[67], [73], 76], [84-86]**	Activation of Parasitic Thyristor. High Collector Current (Static Latchup). High (dV_G/dt) during turn-off. High (dVce/dt) during turn-off.	Loss of Gate Control Device remains conducting current. Thermal Runaway: General overheating of die cells.	Entire Die Active Area Solder Layers (Die-Attach) Al Metallization
Secondary Breakdown **[67], [80], [88]**	Local thermal breakdown due to high currents Uneven distribution of high collector current High Collector-Emitter (V_{CE})	Decreased Blocking Voltage Capability. Short Circuit. High Local Temperature - Hot Spots. Thermal Runaway: Overheating of peripheral cells, spreads to the whole die.	Emitter Area
Energy Shocks **[80], [89-90]**	Short Circuits below the IGBT Critical Energy Level Short Circuits above the IGBT Critical Energy Level	Degradation of Die Al Metallization (Voids, Cracks) Thermal Runaway after successfully turned-off: General overheating of die cells. Bond Wires Lift-Off, Bond Wires Cracks, Bond Wires Rupture	Emitter Area Al Metallization Bond Wires Solder Layers (Die-Attach)
Overload **[67], [73-76], [80], [89-90]**	Improper Gate Activation Collector-Emitter Overvoltage (Primary Breakdown) Latch-up Secondary Breakdown Dynamic Low Load Events (Energy Shocks)	Decreased Blocking Voltage Capability. Thermal Runaway: General overheating of die cells. Solder Layers Voiding and Melting Bond Wires Rupture and Melting	Entire Die Active Area Al Metallization Bond Wires Solder Layers (Die-Attach)

Table 2-1 – IGBT Failure Mode, Effect and Analysis Table 1

Failure Mechanism	Failure Cause	Failure Manifestation	Failure Location
ESD **[93]**	Static Build-Up Electrical Charge, Discharging on IGBT Low Humidity Levels	Gate Oxide Degradation Gate Oxide Breakdown leading to Gate Oxide Perforation Open Circuit	Gate Oxide
External Radiation **[67], [74], [94]**	Exposure to Electromagnetic energy Exposure to Cosmic Rays	Gate Oxide Degradation Short Circuit, Burnout (Short Circuit when device is supporting full line voltage)	Gate Oxide Solder Layers Die Active Area Bond Wire
Hot Carrier Injection (HCI) **[67], [75], [81], [95]**	Elevated Gate Voltage High On-State Current Elevated Die Temperature	Change in Threshold Voltage (V_{THRES}) Change in Forward transconductance (g_m) Switching Characteristics Change Gate Oxide Degradation Electric Field Distortion (Loss of Voltage Blocking Capability)	Gate Oxide Die Active Area
Time Dependent Dielectric Breakdown (TDDB) **[67], [75], [81], [95]**	Elevated Gate Voltage High On-State Current Elevated Die Temperature	Change in Threshold Voltage (V_{THRES}) Change in Forward transconductance (g_m) Switching Characteristics Change Gate Oxide Degradation Electric Field Distortion (Loss of Voltage Blocking Capability)	Gate Oxide Die Active Area
Electromigration **[67], [73], [97-98]**	High On-State Current High Off-State Voltage High Humidity	Increase in resistance of Al Die-Metallization Increase in resistance of Bond Wire. Increased Leakage Currents. Loss of Voltage Blocking Capability.	Die-Pads Al Metallization Bond Wire
Bond-Wire Degradation **[73-77], [91-92], [101-102], [107-109]**	Elevated Temperature Rate of Change of Temperature Difference in Thermal Expansion Coefficients of Al & Si Power Cycling High-On State Current / Short Circuits Electromigration Induced Current in Closely Spaced Bond-Wires Corrosion	Bond-Wire Lift Off Bond-Wire Cracks Bond-Wire Rupture Increase of On-State Voltage (V_{CE_SAT}) Increase of On-State Losses Increase of Switching Losses Open Circuit	Bond-Wire Interface at the Bond-Wire and Silicon

Table 2-2 - IGBT Failure Mode, Effect and Analysis Table 2

Failure Mechanism	Failure Cause	Failure Manifestation	Failure Location
Solder Layers Degradation **[73-76], [81], [99-100]**	Elevated Temperature Rate of Change of Temperature Difference in Thermal Exp. Coeff. of Solder Alloy & Si Difference in Thermal Exp. Coeff. of Solder Alloy & Ceramic Substrate &Base Plate Power Cycling High-On State Current / Short Circuits Induced Current in Closely Spaced Bond-Wires Corrosion	Solder Fatigue Solder Crack Solder Void Die-Attach Voiding Die-Attach Melting Enhanced Die Temperature Enhanced Die-Attach Resistance	Solder Layer and Silicon Die (Die-Attach) Interface Ceramic Substrate and Base Plate
Die-Metallization Degradation **[73-76]**	Elevated Temperature Temperature Swings Difference in Thermal Expansion Coefficients of Al Metallization & Silicon Power Cycling Corrosion	Al metallization crack growths Al metallization extrusion Electromigration Enhanced Al metallization resistance Increase in the on-state voltage (V_{CE_SAT}) Enhanced on-state power loss. Enhanced Die-Temperature	Al metallization layers
Corrosion **[73-76], [103]**	Oxidation Thermo-mechanical stresses Corrosive chemical within the application Infiltrated gases Salts deposits Humidity	Bond-Wire Cracks Bond-Wire Rupture Al metallization cracks growths Open Circuit Enhanced Al metallization resistance Si-Gel degradation Enhanced Die-Temperature Insulation-Breakdown/Flashovers/Short Circuits	Bond-Wire Al metallization layers Silicon-Gel
Mechanical Overstress **[67], [73-76]**	Vibrations Bending Thermal Shocks	Bond-wires lift-off, cracks & ruptures / Open Circuit Ceramic substrate cracks Enhanced Die Temperature	Bond-Wire Ceramic Substrate
Silicon-Gel Degradation **[73], [105]**	Humidity Corrosion	Decreased Ingress Protection Bond-Wire Degradation Al Metallization Degradation	Silicon-Gel

Table 2-3 - IGBT Failure Mode, Effect and Analysis Table 3

2.7 IGBT Reliability and Accelerated Ageing Testing

The electronics industry is governed by reliability tests issued by different regulating bodies. These standards demand for industrial tests to be conducted on semiconductor components to ensure quality, reliability as well as to trigger early lifetime failing devices. Specific industries have specific standards, ranging from general, industrial, military, aerospace, and space grade tests. Some of these standard bodies include the Joint Electronic Device Engineering Council (JEDEC), International Electrotechnical Commission (IEC), Automotive Electronics Council (AEC), US Department of Defense Military Standard (MIL), with standards such as JEDEC JESD-22, IEC 60749-34, AEC-Q100, MIL-STD-750, amongst others. Such bodies regulate standards for device reliability testing and all commercially available devices must pass these tests to be utilized in a specific industrial sector hence guaranteeing a level of quality and reliability in the application. The main scope of these tests is to determine the long-term reliability aspects of the semiconductor device. Hence, IGBTs as other PSDs, are subjected to accelerated ageing testing to achieve the same degradation effects, obtained through the employment of the device for many years, but in a shorter period, within a laboratory setting. This is conducted by aggravating the test conditions, hence stressing the device, and speeding the normal ageing process. Aggravated test conditions during accelerated ageing include temperature, humidity, vibration, pressure, electrical overstress, light etc. The technique has been widely used in industry to determine the lifespan or shelf life of a product, especially for new products which have not gone through their useful lifetime. Furthermore, accelerated ageing test procedures help to determine the failure mechanisms of a product, determine the precursor indicators of failure, and help model the device life expectancy. Some of these reliability tests conducted for IGBTs include, High Temperature Gate Bias (HTGB), High Temperature Storage Life (HTSL), Temperature Humidity Bias Stress (THBS), Unbiased High Humidity Accelerated Stress Tests (UHAST), Temperature Cycling (TMCL), and Thermal Fatigue (TF) also known as Power Cycling (PC) [3],[13].

2.7.1 IGBT High Temperature Gate Bias (HTGB) Test

HTGB is a test designed to assess the quality and reliability of the gate oxide. It is conducted at the maximum DC gate voltage (stated in datasheet), while the device is at an elevated junction temperature (T_J). The main aim of this test is to assess the level of gate degradation triggered by the oxide defects (charge traps) and ionic contaminants (trapped charge) in the oxide. This test is conducted by applying the DC voltage (100% of rated V_{GE}) between the gate

and emitter while the collector is shorted with the emitter (V_{CE} = 0V). The test temperature is set at the maximum junction temperature (T_{J_MAX}). The device is subjected to these conditions for 1000 hours. Main parameters which are monitored are the gate-emitter threshold voltage (V_{THRES}) and gate current (I_G). Parameters must not shift by not more than twenty percent (20%) when compared to new [13], [110-111].

2.7.2 IGBT High Temperature Storage Life (HTSL) Test

The HTSL test is utilized to establish the capability of the device to counteract high temperatures. The main aim of this test is to assess the integrity of the package. Even though the device, is not normally exposed to these high temperatures during applications, this test is mainly utilized to accelerate failure modes that would pop-up during long storage periods. The test is conducted by placing the IGBT in a temperature chamber at an elevated ambient temperature (for plastic packages the ambient temperature T_A is set to 150°C). Test qualification requires 1000 hours under the above test conditions after which the IGBT should remain operational [13], [110-111].

2.7.3 IGBT Low Temperature Storage Life (LTSL) Test

LTSL test is utilized to determine the capability of the IGBT to withstand low temperatures. This test is mainly utilized to trigger mechanical failures of the device's package, as low temperatures seldomly affect the semiconductor part of the IGBT. Even though the IGBT during normal operation is rarely exposed to such low temperatures, this test is mainly required to expedite the long-term storage related failure mechanisms. During the test, the IGBT is placed in a thermal chamber set at an ambient temperature (T_A) of -65°C. Test qualification requires 1000 hours under the above test conditions after which the IGBT should remain operational [13], [110-111].

2.7.4 IGBT Temperature Humidity Bias Stress (THBS) Test

The THBS test is utilized to determine the capability of the different IGBT sub-components to withstand high temperatures and high humidity levels during prolonged operation. In section 2.6, it has been described the corrosive implications of humidity, especially through passivation materials and surface corrosion, predominantly in plastic packaged devices. This test highlights also if there are any ionic contaminants. These contaminants will diffuse especially under the influence of high temperature and high electric fields, shifting locally the threshold voltage (V_{THRES}). Devices that fail under HTRB, evidence sub-threshold conduction. During this test,

the IGBT collector-emitter voltage (V_{CE}) is set between 80% to 100%. The gate is shorted to the emitter (V_{GE} = 0V), while the ambient temperature is set at 85°C and the relative humidity is set at 85%. Test qualification requires 1000 hours under the above test conditions after which the IGBT should remain operational and the threshold voltage (V_{THRES}), breakdown voltage (V_{CE_MAX}) and collector-emitter leakage current ($I_{LEAKAGE}$) must not shift by not more than twenty percent (20%) when compared to new [13], [110-111].

2.7.5 IGBT Unbiased High Humidity Accelerated Stress Test (UHAST)

The main aim of the UHAST test is to assess the ability of the IGBT to withstand moisture. The IGBT is subjected to steam at high pressure levels. The device is placed in a thermal chamber above a tray containing deionized water (preventing water condensation to cluster on the IGBT). Compared to THBS, this test will cause more damage to the IGBT, due to the high level of moisture as it helps accelerate the corrosive effects of the water vapor. Furthermore, this test will cause significant damage to the insulation as well. The thermal chamber ambient temperature is set to 130°C, with pressure at 15PSI and relative humidity of 100%. The test is conducted for seventy-two hours after which threshold voltage (V_{THRES}). breakdown voltage (V_{CE_MAX}) and collector-emitter leakage current ($I_{LEAKAGE}$) must not shift by not more than twenty percent (20%) when compared to new [13], [110-111].

2.7.6 IGBT Steady State Operation (SSO) Test

SSO test is utilized to determine the reliable operation of the IGBT during normal continuous operational conditions. Multiple electrical parameters of the IGBT are monitored during this test including the threshold voltage (V_{THRES}), on-state voltage (V_{CE_SAT}), junction to case thermal resistance (θ_{JC}), collector to emitter leakage current ($I_{LEAKAGE}$). The test is conducted by setting the gate-emitter voltage (V_{GE}), typically greater than 10V, the junction temperature (T_J) at 100°C and ambient temperature (T_A) at 25°C. Test qualification requires 1000 hours under the above test conditions after which the above IGBT electrical parameters should be below the maximum values as specified by the manufacturer in the device's datasheet [13], [110-111].

2.7.7 IGBT Thermal Cycling (TC) Test

TC test is utilized to determine the capability of the IGBT to withstand thermal shocks in air, and hence determine the corresponding effects on the IGBT's sub-components, when exposed to extreme high and low temperatures. Test is conducted by utilizing two thermal chambers,

one set at a constant and evenly distributed high temperature and the other set at a constant evenly distributed low temperature. IGBTs are cycled from one chamber to the other, where each cycle consists of leaving the IGBT for a minimum of fifteen minutes in the hot chamber and immediately transiting the device to the cold chamber for another fifteen minutes. This enhances the effects, already discussed in Section 2.6, of thermal expansion coefficient mismatch, of the different IGBT's sub-components. Typical temperature utilized for the hot chamber is 150°C, while the typical temperature utilized for the cold chamber is -65°C. The device is exposed to numerous cycles, where the number of cycles depends on the level of degradation to be inflicted to the IGBT. Generally, ten cycles inflict enough degradation to assess the quality and reliability of the IGBT. After TC testing, the IGBT should remain operational with electrical parameters threshold voltage (V_{THRES}), breakdown voltage (V_{CE_MAX}), and collector-emitter leakage current ($I_{LEAKAGE}$) must not shift by not more than twenty percent (20%) when compared to new [13], [110-111].

2.7.8 IGBT Single-Shot Unclamped Inductive Switching (UIS) Test

In most power electronics applications, PSDs are protected by free-wheeling diodes to clamp reverse voltages and protect against any off-state conduction, especially during inductive switching. Switching an inductive load without free-wheeling diodes is referred as Unclamped Inductive Switching (UIS). There are some applications, where IGBTs can be forced to conduct during the off state through avalanche mode, and hence the device must be able to dissipate all the energy stored in the inductor during the switching process. A case in point is the fly-back converter circuit. The most common failure mode triggered by UIS is latch-up through the triggering of the parasitic thyristor leading to thermal runaway [117]. Equation 2.8 shows the dependencies of the maximum avalanche energy that can be sustained by an IGBT as seen in [116, Eq. 6]. It shows the dependence of avalanche energy on the avalanche duration through the size of the inductance.

$$E_{AS} = \frac{1}{2} L I_O{}^2 \left(\frac{V_{BR\_EFF}}{V_{BR\_EFF} - V_{DD}} \right) \tag{2.8}$$

Where E_{AS} is the energy in avalanche, L is the inductance, I_O is the output current, V_{DD} is the supply voltage, and V_{BR_EFF} is the avalanche breakdown voltage. Avalanche stress testing is conducted utilizing the test circuit shown in Figure 2.30. The DUT is utilized to charge the inductor and then the inductor dissipates the energy into the DUT after it is switched-off. The peak avalanche current depends on the inductor charging duration.

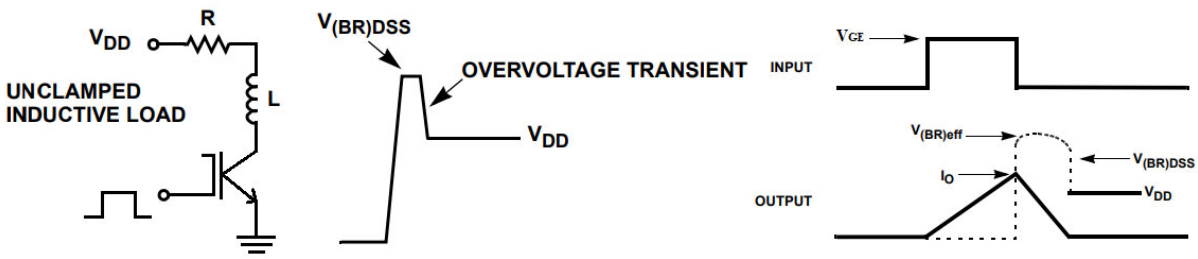


Figure 2.30 - Unclamped Inductive Switching Test Circuit [116]

Manufacturers in the respective datasheets provide the maximum avalanche current as a function of avalanche duration and temperature. Maximum avalanche current reduces with both temperature and avalanche duration [116]. The test is conducted by applying a single pulse gate signal. As the IGBT switches on, the output current (I_O) rises, up till the desired test current. At this point the gate drive is removed, abruptly turning-off the IGBT. Due to the inductor load, the current cannot change immediately, and hence the inductor over-voltage drives the IGBT into collector-emitter avalanche. Mainly there are two modes of avalanche failures, known as low current-long duration (LCLD) and high current-short duration (HCSD). LCLD avalanche failure are predominantly considered to be triggered by high temperature. HCSD avalanche failure modes are mainly triggered by the triggering of the parasitic thyristor. Hence this test aims to assess the ability of the device to withstand inductively induced overvoltage. This test specifies the Maximum Energy in Avalanche for single pulse operation (E_{AS}), Avalanche Current for single pulse operation (I_{AS}), and Maximum Energy in Avalanche versus starting junction temperature [116-117], [121].

2.7.9 IGBT Repetitive Unclamped Inductive Switching (RUS) Test

As discussed, IGBTs can be destroyed by UIS by the triggering of the parasitic thyristor (latch-up) and temperature constraints. Some applications require IGBTs to conduct in avalanche for millions of times over the device's lifetime. Latch-up and temperature constraints are not the only failure mechanisms that can be triggered by repetitive avalanche cycling. Hot carrier injection (HCI) process through impact ionization during avalanche conduction, injects hot carriers into the oxide layer, hence diminishing the insulation capabilities of the oxide layer. Therefore, another common failure is the shift in the threshold voltage with increased avalanche cycling. Repetitive avalanche also effects the aluminum emitter metallization. Due to avalanche, continuous temperature excursions are present, causing the continuous expansion and contraction of the IGBT's sub-components, hence causing degradation in the emitter metallization, voiding of the solder layers, and weaking of the wire bonds. This basically

increases the on-state collector to emitter voltage (V_{CE_SAT}) due to increased resistance of the source metallization and weakening of the wire-bonds contacts. Hence the RUS test, aims to assess the capability of the IGBT to withstand avalanche repetitively. IGBT manufacturers hence specify a parameter called Avalanche Energy under Repetitive Pulse (E_{RAS}) [88]. The same UIS test setup, utilized for single-shot operation is used here, with the difference of utilizing a pulse-train at the gate input with a corresponding frequency (f) and duty cycle (δ), hence making the Avalanche Energy under Repetitive Pulse (E_{RAS}) dependent on these parameters. Table 2-4 summarizes the above reliability tests and corresponding test conditions [116-117], [121].

IGBT Reliability Test	Test Conditions	Monitored Parameters & Compliancy
High Temperature Gate Bias (HTGB)	V_{GE} rated at 100% of datasheet rating, V_{CE} = 0V, $T_{TEST} = T_{J\_MAX}$. Test Duration = 1000 hours.	V_{THRES} & I_G within 20% as new.
High Temperature Storage Life (HTSL)	Unbiased, T_{TEST} = 150°C. Test Duration = 1000 hours.	Operational after test.
Low Temperature Storage Life (LTSL)	Unbiased, T_{TEST} = -65°C. Test Duration = 1000 hours.	Operational after test.
Temperature Humidity Bias Stress (THBS)	V_{GE} =0V, V_{CE} rated at 80% to 100% of datasheet rating, T_{TEST} = 85°C, Relative Humidity = 85%. Test Duration = 1000 hours.	V_{THRES} & V_{CE_MAX} & $I_{LEAKAGE}$ within 20% as new.
Unbiased High Humidity Accelerated Stress Test (UHAST)	Unbiased, V_{CE} rated at 80% to 100% of datasheet rating, T_{TEST} = 130°C, Pressure = 15PSI, Relative Humidity = 100%, Test Duration = 72 hours.	V_{THRES} & V_{CE_MAX} & $I_{LEAKAGE}$ within 20% as new.
Steady State Operation (SSO) Test	V_{GE} =10V, V_{CE} rated at 80% to 100% of datasheet rating, $T_{JUNCTION}$ = 100°C, T_{TEST} = 25°C, Relative Humidity = 85%, Test Duration = 1000 hours.	V_{THRES} & V_{CE_MAX} & $I_{LEAKAGE}$ & θ_{JC}, IGBT electrical parameters should be within the maximum values as specified by the manufacturer's datasheet
Thermal Cycling (TC) Test	Thermal Shocks, $T_{HOT\_CHAMBER}$ = 150°C, $T_{COLD\_CHAMBER}$ = -65°C, Test Duration = Maximum 10 Cycles, Cycle Duration = 15 minutes per cycle hot / 15 minutes per cycle cold.	V_{THRES} & V_{CE_MAX} & $I_{LEAKAGE}$ within 20% as new.
Single-Shot Unclamped Inductive Switching (UIS) Test	Depends on the IGBT power capability: Maximum Energy in Avalanche for Single Pulse Operation (E_{AS}), Avalanche Current for Single Pulse Operation (I_{AS}).	V_{THRES} & V_{CE_MAX} & $I_{LEAKAGE}$ & Forward Transconductance (g_m) & θ_{JC}. Switching Parameters: Rise Time, Fall Time, On-Time, Off-Time.
Repetitive Unclamped Inductive Switching (RUS) Test	Depends on the IGBT power capability: Maximum Energy in Avalanche for Repetitive Pulse Operation (E_{AS}), Avalanche Current for Repetitive Pulse Operation (I_{AS}) , Repetitive Pulse Frequency, Repetitive Pulse Duration.	V_{THRES} & V_{CE_MAX} & $I_{LEAKAGE}$ & Forward Transconductance (g_m) & θ_{JC} & V_{CE_SAT}. Switching Parameters: Rise Time, Fall Time, On-Time, Off-Time.

Table 2-4 – IGBT Industrial Reliability Tests & Corresponding Test Conditions

2.8 IGBT Power Cycling

Power Cycling testing is utilized to determine the reliability and integrity of the IGBT's die and package. The power cycling test aims to catalyze failure mechanism in bond wires, solder layers (die-attach), die metallization, ceramic substrate, and mechanical assembly. This is conducted by heating the device, through self-heating by dissipating power in the device and cooling the device, through self-cooling, through the removal of power from the IGBT. Power cycling is considered one of the best ways to accelerate the degradation of the IGBT as it significantly emulates the real application and utilization. In general, there is no standard testing methodology for power cycling testing, even though there are commonalities in the power cycling methodologies and systems found in literature. During power cycling testing, degradation is detected, by monitoring the IGBT's electrical and thermal parameters. Moreover, power cycling testing is utilized to conduct lifetime modelling of the IGBT.

2.8.1 Power Cycling Ageing Systems (PCAS)

PCAS are laboratory setups utilized to expedite IGBT ageing in a controlled way while acquiring and monitoring the IGBT's electrical and thermal parameters to be utilized for diagnostic and prognostic purposes. As already explained, there is no standard methodology which governs IGBT power cycling, even though they can be mainly categorized into two main types that is: DC PCAS and AC PCAS [118-124].

In DC PCAS, the IGBT is injected DC current. Since the IGBT has some on-state resistance, it will generate conduction losses, which in-turn generates thermal flux in the IGBT. The IGBT current is switched periodically between the full-injected DC current and zero. This is achieved by keeping the gate voltage constant and the injected current is switched periodically by controlling the power supply. In this way the device is self-heated when current is injected and self-cooled when the current is removed. The duration and amplitude of the current pulse are customized according to the desired temperature stress. In AC PCAS, the IGBT is switched periodically, by applying a periodic signal to the gate (commonly pulse width modulation PWM) and switching a high voltage at the output. In this scenario heat is generated in the IGBT not only through on-state conduction losses but also through switching losses. AC PCAS commonly employ an inductive load, conducting a sinusoidal current with constant magnitude during on-period and no-current during the off-period [123]. AC PCAS has the considerable advantage of generating thermal flux in the IGBT with better correlation to the thermal flux generated during IGBT normal application. This is since AC PCAS employs both conduction

and switching losses unlike in DC PCAS which employs on-state losses only and no high DC-Link voltage is utilized. Furthermore, in AC PCAS the IGBT integrated free-wheeling diode losses also contribute to the heat generation, unlike in DC PCAS where only the IGBT conduction losses are involved in the heat generation which requires high current pulses. This impacts the heat distribution within the IGBT package, as in DC PCAS the heat distribution is somewhat focused on the IGBT die, unlike in AC PCAS where the heat distribution is more even. On the other side the implementation of DC PCAS is simpler. More importantly, DC PCAS monitoring, and acquisition of the electrical and thermal parameters required for diagnostics purposes, are easier and more reliably implemented and acquired [67].

2.8.2 DC PCAS Procedures

As already discussed, in DC PCAS, current is injected periodically through the IGBT, to self-heat the device through the on-state resistance. Different DC PCAS procedures were found in literature which can be categorized as; constant heating time procedure, constant case-temperature peak-to-peak fluctuation ($T_{C\_PK\text{-}PK}$) procedure, constant power flow procedure, and constant junction temperature peak-to-peak fluctuation ($T_{J\_PK\text{-}PK}$) procedure. The main differentiator between the listed DC PCAS procedures is the ability to arrest the degree of degradation, hence obtaining a more controlled ageing. The constant heating time procedure is the severest but most realistic DC PCAS. As in a real application, this procedure does not provide any mechanism to arrest degradation during accelerated ageing. This has the advantage of providing a more realistic approach, but with an enhanced risk for the procedure to go out of control. The other three DC PCAS procedures provides better degradation control mechanisms. The least effective degradation control is the constant case-temperature peak-to-peak fluctuation ($T_{C\_PK\text{-}PK}$) procedure. During this procedure, the device is heated to a predefined case temperature (T_C). At this point the IGBT is periodically switched such that the case temperature (T_C) is allowed a degree of fluctuation. This procedure allows the device to marginally cool down the DUT during accelerated ageing, obtaining a lower average junction temperature (T_{J_AVR}) and hence arresting the rate of degradation. The constant power flow procedure provides an enhanced mechanism to control the level of degradation. This is achieved by controlling the power dissipation in the IGBT's junction, which compensates for the enhanced junction power dissipation during accelerated ageing, due to the increase in the junction temperature (T_J). The most efficient way to control the degree of degradation is to conduct an ageing procedure like the constant case temperature procedure, but instead fixing the junction temperature fluctuation ($T_{J\_PK\text{-}PK}$). This technique proves to be the most difficult

to implement as it requires access to reliable junction temperature measurement or reliable junction temperature estimation through thermal modelling or derived from other dependent IGBT electrical parameters such as the on-state saturation voltage (V_{CE_SAT}) [125-126]. Figure 2.31 illustrates the comparison of the listed IGBT DC PCAS procedures, as conducted by Schuler et al. [125]. It provides the plots of the junction temperature (T_J) and number of DC PCAS cycles, up till IGBT failure. This shows that the constant heating time procedure triggered the earliest end-of-life, with junction temperature (T_J) in the vicinity of 360°C. It was observed that the main source of failure was emitter die metallization melting. The second procedure to trigger failure was the constant case temperature fluctuation procedure (T_{C_PK-PK}), with a corresponding maximum junction temperature in the vicinity of 340°C. In this scenario extensive emitter metallization melting and die-attach melting, caused IGBT failure. The constant power loss procedure produced the third longest DC PCAS. The junction temperature (T_J) never surpassed the 180°C, and hence in this case emitter die metallization and die-attach melting were not observed. In this scenario failure was triggered by bond wire lift-off. Finally, the constant junction temperature fluctuation (T_{J_PK-PK}) was the longest DC PCAS, mainly since this ageing control strategy effectively limited the maximum junction temperature (T_J) to just above the specified IGBT maximum junction temperature (T_{J_MAX}). This latter procedure proved to obtain a longer and better controlled ageing procedure but fails to include relevant degradation in the device due to reduced overstress by maintaining the maximum junction temperature (T_{J_MAX}) as controlled as possible, hence avoiding thermal runaways.

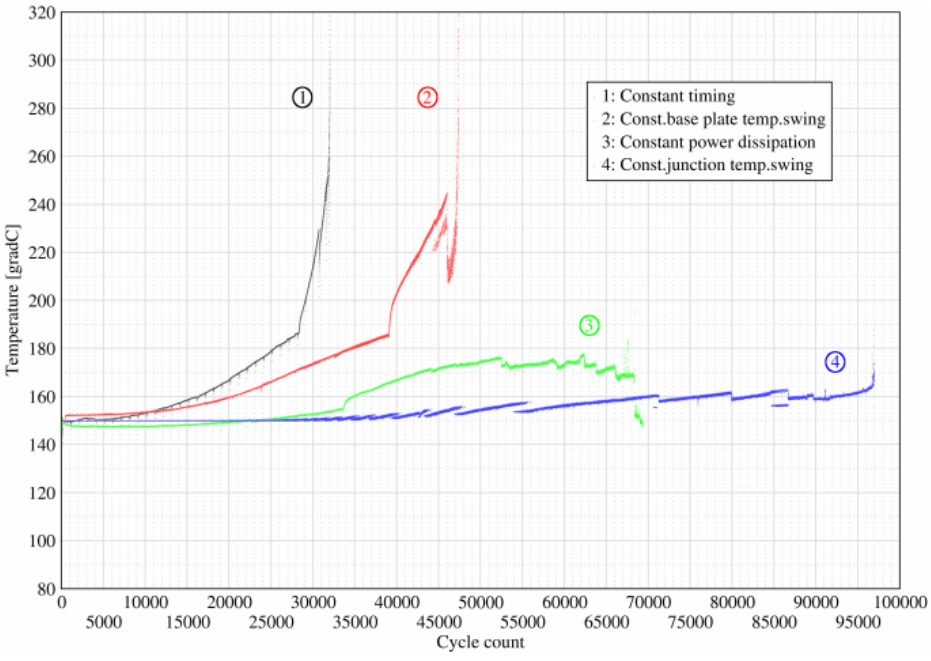


Figure 2.31 – Comparison of different DC PCAS procedures T_J vs Age Cycles [125]

Hence, Schuler et al. [125], concluded that to emulate real field failing scenarios and real field ageing, only the first two strategies are to be considered, as the last two strategies are inherently compensating for the stress to obtain a better age procedure control. Hence the most suitable DC PCAS procedure is considered the constant case-temperature peak-to-peak fluctuation ($T_{C\_PK\text{-}PK}$) as it provides the best compromise between stress level, accelerated ageing control, best real-field degradation representation and data reliability to conduct lifetime estimations.

Several DC PCAS accelerated ageing strategies were found in literature which in-large fit the four DC PCAS strategies mentioned earlier. Khong et al. [127] utilized a combined electro-thermal accelerated ageing procedure, electrically pulsating and keeping power MOSFETs and IGBTs under elevated controlled temperature. This accelerated ageing technique was utilized to emulate electro-thermal fatigue experienced by automotive electronic components. Ageing was performed with current pulses of 120A and duty cycle between 5% and 10% at an environment temperature close to the devices' maximum junction temperature (T_{J_MAX}). This study concluded that the induced stresses led to an increase in the on-state resistance and hence an increase in the on-state power losses. Furthermore, this was shown to be the consequence of die-attach de-lamination and bond wire cracking of the emitter terminal. Another study was conducted by Dupont et al. [128]. In this study, the main accelerating ageing agents were again temperature and electrical overstress. Devices were subjected to high environmental temperatures as well as pulsed currents of 150A and duty cycles of 30%. This study showed an increase in the off-state leakage current. This was mainly evident during tests where the device's junction temperature was left to considerably depart from the maximum junction temperature (T_{J_MAX}). Furthermore, a high on-state resistance was also observed which again was found to be the consequence of bond-wire cracking.

Smet et al. [138], conducted accelerated ageing of IGBT modules, utilizing a DC PCAS. In this study the case temperature (T_C) obtained through the baseplate temperature was set to an offset value in the range of 60°C to 90°C, while allowing for wide case temperature swings in the range of 60°C to 100°C, obtained through the control of the collector current pulse amplitude and duration, hence obtaining five different DC PCAS ageing strategies. Acoustic scanning and SEM imaging evidenced degradation due to bond-wire cracking, and solder alloy cracking between the ceramic substrate and base plate. Amoiridis et al. [139] utilized a DC PCAS to conduct accelerated wear-out tests for high power IGBT modules. Its operation principle is based on the case-temperature peak-to-peak fluctuation strategy. Through the injection of high DC current pulses, the die is heated up actively during the on-time while is let to cool down

during the off-time. Thus, case temperature swings were achieved due to losses in the active area of the IGBT. This system was reported to trigger failures such as solder fatigue and bond wires lift-off. An improved version of the DC PCAS is the DC PCAS with DUT in saturation mode [140-143]. In this scenario the DUT is operated in saturation mode to act like a constant current source. The required collector current (I_C) is obtained through the adjustment of the applied gate-emitter voltage (V_{GE}), in conjunction with the minimum collector voltage (V_C). This configuration removes the dependence of the collector current (I_C) from the collector voltage (V_C), even if the latter is above the required minimum for a given gate-emitter voltage (V_{GE}). Hence this configuration ensures more reliable power losses in the DUT.

Reviewed literature highlights the fact that accelerated ageing mechanisms of gate-controlled power devices utilize thermal and electrical overstress as the prevalent accelerated ageing agents. NASA's Ames Research Centre, Intelligent System division has been conducting accelerated ageing and prognostics of gated power transistors for the past years evidencing their findings in relation to precursor of failure parameters, prognostics techniques and health management systems in various literature [131-136]. Throughout these studies accelerated ageing methodology of gated power devices has remained relatively the same and is mainly based on the approach of thermo-electrical overstress. The aim was to age packaged power MOSFETs and IGBTs with current capabilities of up to 50A and blocking voltage capabilities of up to 800V. The accelerated ageing applied, consisted of DC power cycling, hence accelerating the degradation by thermal overstress through pulsating current in the DUT, but without the use of an external heat-sink, leading the device to self-heat. The strategy was that of self-inflicting damage. The failure scenarios intended to be triggered were mainly latch-up, thermal runaway and failure to turn-on due to gate control loss. Throughout the ageing procedure, the DUT's case temperature (T_C) was measured and controlled, while allowing for a specified case temperature (T_C) fluctuation.

Within these studies two different accelerated ageing procedures were conducted. The first method involved the DC power cycling of the DUT, with a constant temperature load profile. This was mainly done to determine the failure mode of the devices when operated in extreme temperature well beyond the safe operating area limits. During this procedure, the DUT's temperature was maintained swinging at 230˚C throughout the entire duration of the ageing procedure.

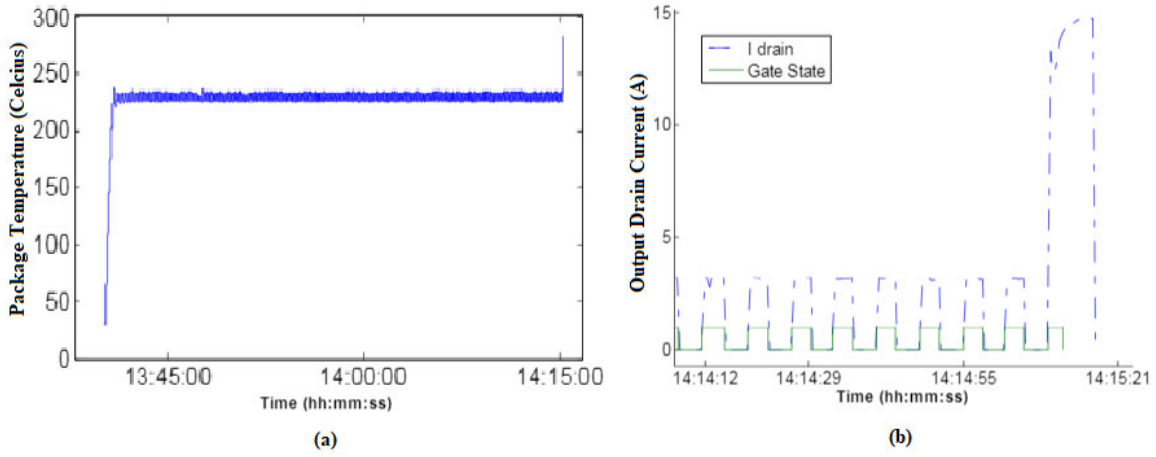


Figure 2.32 - Method 1 Accelerated Ageing Procedure highlighting the onset of thermal runaway (a) thermal profile (b) Gate State and Output Current [135]

Figure 2.32 illustrate the package temperature with power cycling time plot at the on-set of thermal-runaway, and the corresponding output current and gate voltage plot. It highlights the end of profile output current increase, corresponding to a rapid temperature increase which led to thermal runaway. This study shows that thermal runaway happened when the device latched-up. The accelerated ageing procedure would stop when this scenario is reached. The second accelerated ageing procedure employed, utilized a stepped temperature load profile. The stepped profile was used to enable a better understanding of the device degradation even within the safe operating area operation. Figure 2.33 illustrates the stepped temperature profile. Device failure occurred on average after three temperature load profiles with a profile duration of about an hour. The failure encountered was the DUT's inability to switch effectively due to an increased on-state resistance, leading to a drop in the output current. Failure generally occurred during the cool down period from 200˚C to 100˚C.

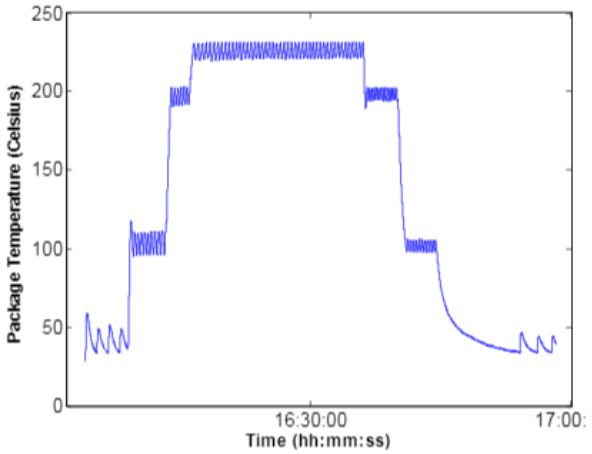


Figure 2.33 – Method 2 Accelerated Ageing Procedure, stepped temperature load profile [135]

In [136], the same research group modified the accelerated ageing procedure by modifying the power cycling procedure. Instead of utilizing lower power cycling levels but without the use of a heat sink, a larger output power was utilized in conjunction with a thermal block. The main aim was to obtain electrical overstress by exceeding the rated output voltage and output current of the DUT but without inflicting severe thermal stress as in the previous methodologies. This was obtained through the utilization of a thermal block to redirect the device's heat to the environment. This was conducted to inflict device degradation but without producing changes in the package that can be produced by the thermal overstress. This tended to avoid package related failure mechanisms.

2.8.3 Junction Temperature Measurement and Estimation

One of the most important aspects of power cycling, is the ability to detect and determine the IGBT's junction temperature (T_J). The specified maximum junction temperature (T_{J_MAX}), should be the highest attainable junction temperature (T_J) and this is directly related to the maximum allowable power dissipation (P_{D_MAX}) that ensures reliable IGBT operation. Commonly, during power cycling procedures, the maximum junction temperature (T_{J_MAX}) is reached and even surpassed. Moreover, the case temperature (T_C) is another critical parameter, especially for controlling the accelerated ageing procedure and to estimate the junction to case thermal resistance (θ_{JC}). Normally this is obtained through the utilization of thermocouples or resistance thermometers.

The ability to determine reliably the IGBT's junction temperature (T_J) is important as it is one of the most important controlling parameters during such procedures. Several techniques were employed in literature which are mainly categorized as either, junction temperature detection (JTD) techniques or temperature sensitive electrical parameters (TSEP) techniques. JTD techniques employ the utilization of thermal/IR cameras or integrated temperature sensors at IGBT die level [144-145]. On the other side TSEPs techniques do not employ any specialized sensors or transducers, but rather extract junction temperature (T_J) information from the IGBT electrical parameters which are affected by the junction temperature (T_J). Such parameters include: the on-state collector-emitter saturation voltage (V_{CE_SAT}), the threshold voltage (V_{THRES}) and the gate current (I_G) [146-147]. Out of the three listed parameters the collector-emitter saturation voltage (V_{CE_SAT}) is the most susceptible to variations in the junction temperature (T_J) and it is the least problematic to be measured, especially during normal operation [148-149].

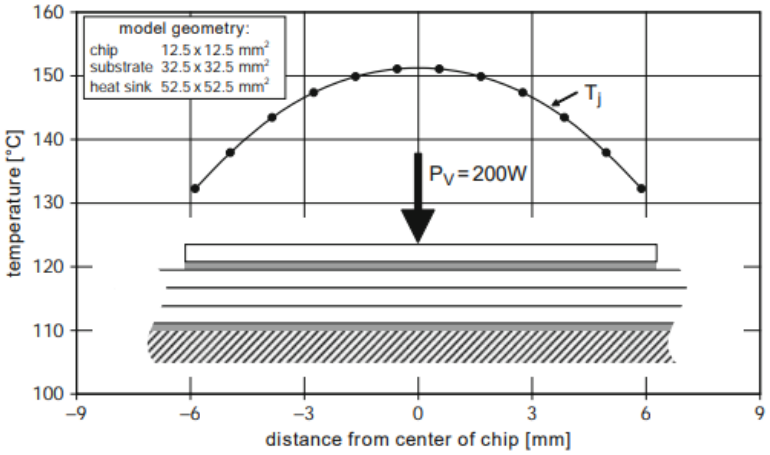


Figure 2.34 – Thermal Simulation of Silicon Die and Corresponding Layers [13]

Figure 2.34 illustrates the modelled temperature distribution of an IGBT die when subjected to a homogenously generated power dissipation of 200W [13]. This plot reveals that the temperature distribution is not homogenous over the entire region of the die, with the central region being approximately 20°C higher than the die's periphery. This indicates that JTD techniques which utilize integrated die temperature sensors, are predominantly affected by the sensor positioning and might not provide insight on the actual die's maximum temperature or average temperature. TSEP techniques, predominantly the collector-emitter saturation voltage (V_{CE_SAT}) technique usually provide the averaged die's temperature. This is commonly referred as the virtual junction temperature (T_{J_VIR}).

The forward voltage-drop (V_F) of a pn-junction diode biased through a very small forward current (I_F), is predominantly dependent on temperature and follows an inversely proportional relationship as illustrated in Figure 2.35. Hence if the forward current (I_F) is small enough, the measurement of the forward voltage (V_F) can be related to the diode's junction temperature. The magnitude of the forward sensing current (I_F) depends on the device's structure and size, but it must be small enough such that the temperature rise due to the sense current is ignored. Typical current densities which are smaller than 100mA/cm^2 are considered [13]. Together with the calibration of the diode's forward voltage (V_F) when biased with small forward current (I_F), at different ambient temperatures, this method provides a convenient way of determining the virtual junction temperature (T_{J_VIR}). This technique can be extended to IGBTs and is directly related to collector-emitter saturation voltage (V_{CE_SAT}), as in this scenario the junction is forward biased, but utilizing small collector current (I_C) acting as the sensing current. The obtained virtual junction temperature (T_{J_VIR}) is not the maximum junction temperature as the central part of the die is still considerably higher especially for large dies and elevated currents.

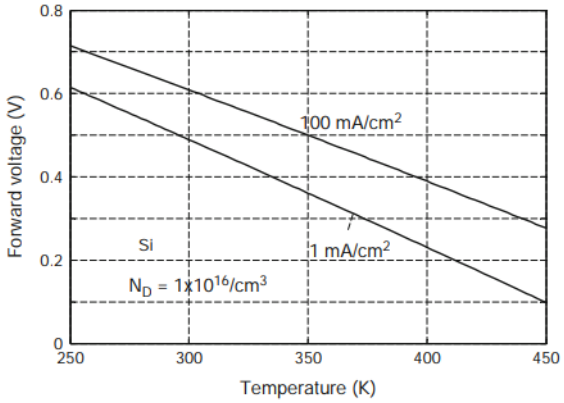


Figure 2.35 – PN-Junction Forward Voltage (V_F) Dependence on Temperature at Constant Current Density [13]

During calibration, the IGBT is kept in a thermal chamber under controlled ambient temperature and the collector-emitter saturation voltage (V_{CE_SAT}) is determined at different ambient temperatures. Through this method the linear relationship between the collector-emitter saturation voltage (V_{CE_SAT}) and temperature, as depicted in Figure 2.35, is obtained. During accelerated ageing, the collector-emitter saturation voltage (V_{CE_SAT}), is measured multiple times. Before conducting this measurement, the main conduction collector current is bypassed from the IGBT, with the IGBT conducting only the small sensing measurement current. As illustrated in Figure 2.36, the first collector-emitter saturation voltage (V_{CE_SAT}) measurement is conducted as soon as the main conducting collector current is bypassed. This measurement will determine the maximum virtual junction temperature ($T_{J\_VIR\_MAX}$), as at this point the junction will be at the beginning of the cooling cycle that is at its maximum temperature. A second collector-emitter saturation voltage (V_{CE_SAT}) measurement is taken prior to re-establishing the main conduction collector current. This measurement will determine the minimum virtual junction temperature ($T_{J\_VIR\_MIN}$). Through these two measurements the virtual junction temperature fluctuation ($T_{J\_VIR\_PK\text{-}PK}$) can be established [92],[150].

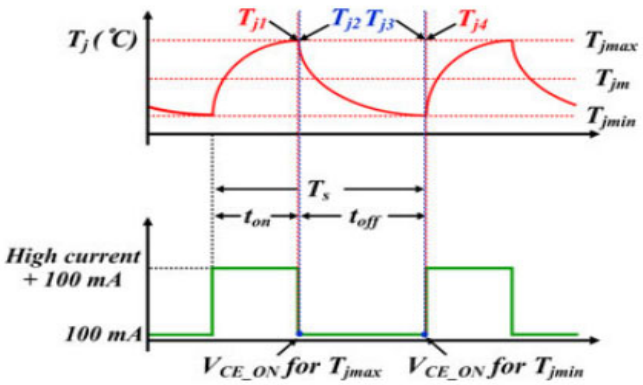


Figure 2.36 – V_{CE_SAT} measurement sequence during power cycling [92].

2.8.4 Other Accelerated Ageing Procedures

Apart from power cycling, other studies utilized other techniques to accelerate the age of power semiconductor devices. In [124] and [129] accelerated ageing was conducted by subjecting power MOSFETs to elevated environmental temperature only, but for extended periods of time. This is essentially a reliability test, like THBS, described in section 2.7, evidencing fault mechanisms such as TDDB. Stojandinovic et al. [151] performed power MOSFET ageing by conducting high gate bias stress (HGBS). It was observed that with gate voltages ranging from 88V to 94V and both the drain and source grounded for a test duration of 2 hours, the threshold voltage of the device was decreased. In another study [122], power MOSFETs were aged through the exposition of low and high radiation dosage rate, ranging from 1krad(Si)/day to 3.3krad(Si)/day and time varying gate bias. The main result was a decrease in the threshold voltage. This technique heavily relies on the DUT's positioning and the radiation distribution uniformity, to obtain consistent and reliable experimental results. Hayes et al. [137], artificially aged power MOSFETs by subjecting them to a series of electrostatic discharges. It was argued that this kind of accelerated ageing is advantageous since it really replicates a real-world degradation scenario (ESD) which can degrade or even destroy the power MOSFET. Accelerated ageing was conducted by tweaking the discharge method, the discharge voltage, and the number of discharge events obtaining a controlled manner of effectively degrading the device but without destroying it. An ESD simulator/gun was utilized with the gun's contact tip placed at the center of the TO-220 epoxy package. Four 20kV pulses were applied to the device, described as enough to degrade the transistor but without destroying it. It is important to point out that this procedure might lead to experimental inconsistences as the position of the ESD gun's tip will play a crucial role in the level of device degradation and hence in the repeatability of the results.

2.9 IGBT Precursors to Failure

Prognostics is an engineering field aimed to determine the time at which a device or system will not perform as intended and will be likely to fail. This time prediction gives what is known as the Remaining Useful Life (RUL). This concept is utilized in safety critical and mission critical systems to either fail safely or survive the failure hence managing the health of the system. Prognostics is mainly based on the analysis of the different failure modes of a system, the detection of the early signs of wear or aging commonly referred to as precursors to failure and the implementation of some form of action to mitigate that failure. A precursor to failure

is an indicator that reveals that a device or a system is likely to go through malfunction. This indicator can be a single parameter, multiple parameters, a single event, or a series of events. Through the monitoring of failure precursors, failure predictions can be conducted by correlating these parameters to an expected normal. This in turn will be useful to provide systems warnings or better understanding how to enhance reliability. This section will discuss the condition monitoring parameters of IGBTs as reported in literature, when conducting accelerated ageing.

2.9.1 IGBT Collector-Emitter Saturation Voltage (V_{CE_SAT})

The collector-emitter saturation voltage (V_{CE_SAT}) (referred also as the on-state voltage V_{CE_ON}), has been extensively employed as a condition monitoring parameter during IGBT degradation. Patil et al. [81], has conducted accelerated ageing on IGBTs by utilizing DC power cycling, hence elevating the IGBT's temperature way beyond the maximum junction temperature (T_{J_MAX}), until latch-up occurs. This technique has been thoroughly described in Section 2.8.2. For this study, the collector-emitter saturation voltage (V_{CE_SAT}) was measured before and after accelerated ageing at room temperature. Results evidenced that there was a decrease, in the range of 8% to 25% of the healthy state value. This study concluded that this decrease was mainly caused by a degradation in the die-attach. In another study Smet et al. [138], conducted DC power cycling on IGBT modules with the main intention to trigger wire-bonding degradation. This accelerated ageing strategy utilized three different case temperature fluctuations settings ($T_{C\_PK\text{-}PK}$) namely: 60°C-120°C, 90°C-150°C and 60°C-140°C.

This study evidenced an increase in the collector-emitter saturation voltage (V_{CE_SAT}). It was concluded that this increase was due to cracking in the bond-wire and degradation in the bond-pads metallization. Moreover, the implemented prognostic technique signaled a failure once the collector-emitter saturation voltage (V_{CE_SAT}) deviated by 3% from the nominal value. Even though the utilization of the collector-emitter saturation voltage (V_{CE_SAT}) as a degradation monitoring parameter at laboratory level can be relatively easy to implement, its employment in the field is not trivial. This parameter's change due to degradation can be susceptible to noise or switching interference and hence signal integrity problems in the field might be significant. Hence noise errors in the range of 1% maybe substantial, especially when considering that studies evidenced collector-emitter saturation voltage (V_{CE_SAT}) changes of 3% as a device failing condition. Hence when employing this parameter, the measurement accuracy will impact the reliability of the prognostic technique.

In-situ measurements of the collector-emitter saturation voltage (V_{CE_SAT}), for IGBTs employed in an automotive application [151], managed to obtain measurement accuracies within 0.1%. In section 3.8.3, it was described that the collector-emitter saturation voltage (V_{CE_SAT}) is dependent on the collector-current (I_C) as well as the junction temperature (T_J) and hence for reliable degradation monitoring this parameter must be isolated from these parameters. Through temperature calibration and look-up tables this isolation was implemented by Xiong et al. [152].

It is important to note that reviewed literature provided contrasting trends of the collector-emitter saturation voltage (V_{CE_SAT}), with studies reporting an increase [138],[151], while other studies reporting a decrease [81],[152]. This can be explained since the change in the collector-emitter saturation voltage (V_{CE_SAT}) depends on the mode of failure. A decrease is mainly contributed by a die-attach degradation, which will enhance the junction temperature (T_J), which will contribute to an enhanced charge carrier population and hence a decrease in the voltage-drop at the junction. This will lead to a decrease in the collector-emitter saturation voltage (V_{CE_SAT}). On the other-side if the failure mechanism is a bond-wire degradation, there will be an increase in the resistance of the wire bonds, this will lead to an increase in the voltage drop across the wire bonds and hence an increase in the collector-emitter saturation voltage (V_{CE_SAT}). Hence this indicates that for IGBT condition monitoring the collector-emitter saturation voltage (V_{CE_SAT}) on its own, might not be reliable enough.

2.9.2 IGBT Gate Threshold Voltage (V_{GE_THRES})

In the study of Patil et al. [81], the IGBTs' gate threshold voltage (V_{GE_THRES}) increased after conducting power cycling, with an average increase of 11%. This study argued that this increase was due to injected and trapped electrons in the gate dielectric, reflecting in an increase of the gate threshold voltage (V_{GE_THRES}). The same trend and conclusion were reported in [153] and [155], when IGBT modules were subjected to power cycling. Tounsi et al. [154], again subjected IGBT modules to accelerated ageing. Here, marginal changes were observed in the gate threshold voltage (V_{GE_THRES}). It was argued that when considering other literature, which reported an increase, the marginal increase was attributed to the good quality of the gate oxide of the tested IGBT modules. The above studies were all under laboratory settings. The employment of the gate threshold voltage (V_{GE_THRES}) for condition monitoring of IGBTs in the field is quite restricted, since obtaining the measurement of this parameter, suspends the IGBTs application operation and requires the use of an additional variable gate signal [121].

2.9.3 IGBT Temperature Precursor Parameters

In section 3.8.3, it was described how the low-current measurement technique of the collector-emitter saturation voltage (V_{CE_SAT}), can lead to the estimation of the virtual junction temperature (T_J). Moreover, this parameter is also utilized for degradation monitoring. In this case the collector-emitter saturation voltage (V_{CE_SAT}) measurement is conducted under the full application collector current (I_C) and maximum junction temperature (T_{J_MAX}). This measurement technique ensures the inclusion of bond-wire degradation and die-metallization degradation. Moreover, this measurement technique includes the effect of junction temperature (T_J) increase due to degradation and ageing on the bond-wire and die metallization. In relation to Figure 2.36, the collector-emitter saturation voltage (V_{CE_SAT}) is measured prior to switching to the low-current measurement technique. Furthermore, at this instant, through the measurement of this parameter and the IGBT's collector current (I_C), the power dissipation (P_D) at this instant can be computed. This latter parameter in conjunction with the junction temperature (T_J) and the case temperature (T_C), can provide an estimation of the junction to case thermal resistance (θ_{JC}). Hence keeping track of the variation of this thermal resistance, with ageing has been utilized in literature [156-159], as it provides insightful information on the degradation of the IGBT. Poppe et al. [159], utilized a measurement technique known as package thermal structure function. The technique entails that after N power cycles, the power cycling procedure is stopped. At this point a calibrated current is injected in the IGBT to heat the junction, after which it is left to cool down. Through this procedure the junction's transient temperature is measured obtaining the corresponding thermal impedance (thermal capacitance C_{JC} and thermal resistance θ_{JC}). Through this method the structure function is obtained. The structure function is the graphical representation of the Cauer Thermal Model network of the impedance of the junction-to-ambient heat-flow path.

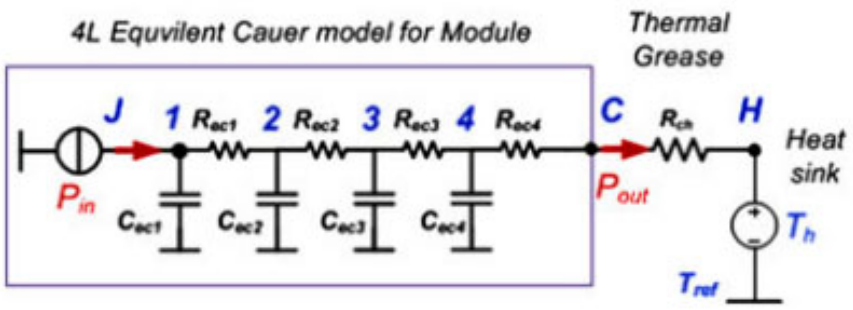


Figure 2.37 – IGBT module Equivalent 4L Cauer Thermal Network describing Thermal Flow from Junction Node to Sink Node [160].

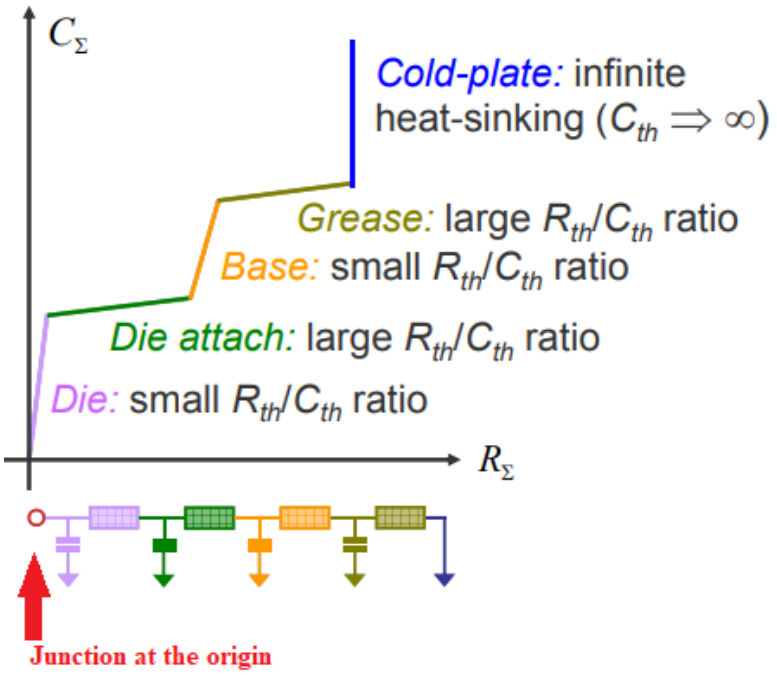


Figure 2.38 – Caeur Thermal Impedance Model Structure Function [159]

The Cauer Thermal Model element block represents the heat transfer through an individual layer of a semiconductor module. The Cauer thermal model represents the multiple layers that constitute the packaging of a semiconductor. This is illustrated in Figure 2.37. The shape of the structure function provides the properties of the junction-to-ambient heat-flow path. It illustrates the way heat flows through a package. This is illustrated in Figure 2.38. Through the Structure Function thermal resistances and thermal capacitances of the different materials and structures within a PSD can be determined. Furthermore, through the structure function, if a material is known, the volume can be identified.

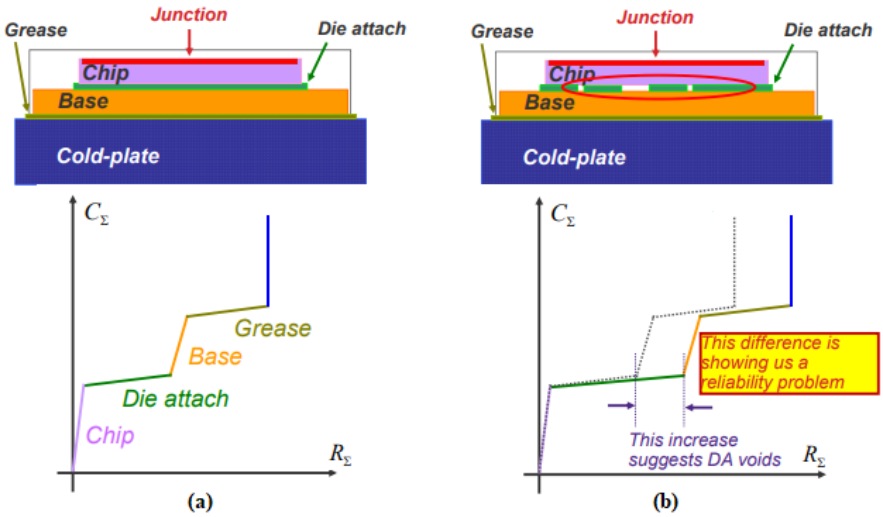


Figure 2.39 – Thermal Impedance Structure Function (a) Healthy (b) Degraded Die-Attach [159]

Figure 2.39 illustrates the variation of the thermal impedance structure function of a healthy device and a device with a degraded die-attach. Through the structure function the condition monitoring can be obtained, with the added benefit of localizing the degradation. Hence, structural or material property degradation changes can be clearly identified by the cumulative thermal impedance structure function. At laboratory level, this technique is very effective. On the other hand, since this technique requires specialized equipment to characterize (Thermal Transient Tester i.e. MENTOR MicRed T3Ster), and it suspends the IGBTs operation, its employment in the field is very limited.

2.9.4 IGBT Transient Time-Domain and Frequency Domain Precursors

IGBTs are mainly utilized in commutation mode. Through the monitoring of the switching performance of the IGBT, degradation can be detected. Switching time-based techniques, monitors the changes in the switching waveforms of the IGBT. Moreover, frequency-based techniques monitor changes in the IGBT's signals' spectrum. IGBT's signals employed in literature for this purpose, include; the gate-emitter voltage (V_{GE}), the collector-emitter voltage (V_{CE}), the gate current (I_G), and the collector current (I_C), including both turn-on and turn-off waveforms. The gate-emitter voltage (V_{GE}) and gate current (I_G) were utilized in [161-163], to identify bond-wire and die emitter metallization degradation in IGBT modules. In [162], the gate current peak, during both turn-on and turn-off decreased, when the IGBT module experienced bond-wire degradation and die emitter metallization degradation. The bigger change was manifested during turn-on with a minor change measured during turn-off. This latter distinction between the turn-on and turn-off was attributed to the Miller capacitance (C_{GC}) which is minimally affected by emitter bond wire degradation, which predominantly dictates the turn-off switching performance of the IGBT. Contrary to what happens during turn-on, where the switching performance of the IGBT is predominantly dictated by the charging of the input gate-emitter capacitance (C_{GE}). This is illustrated in Figure 2.40.

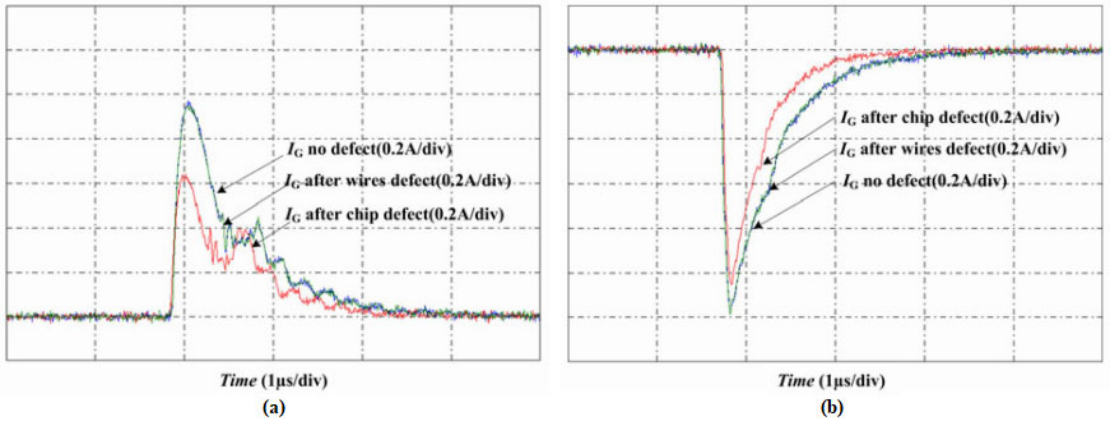


Figure 2.40 - IGBT Gate Current Waveforms due to different degradation (a) Turn-On (b) Turn-Off

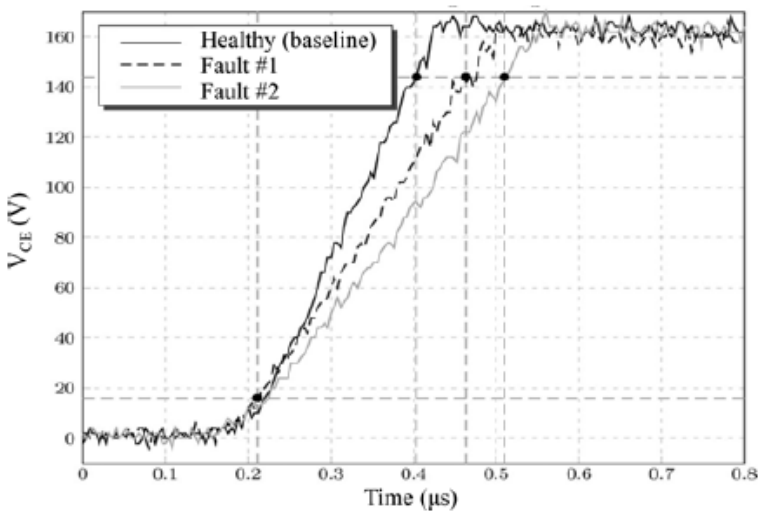


Figure 2.41 – Collector-Emitter Voltage (V_{CE}) waveforms during Turn-Off [161]

In [161], the gate-emitter voltage (V_{GE}) waveform changes were utilized to monitor IGBT degradation. This study determined that IGBT bond-wire degradation, contributed to a faster rise of the gate-emitter voltage (V_{GE}). The IGBT's turn-off collector-emitter voltage (V_{CE}), was utilized by Brown et al. [164], to determine condition monitoring. In this study, the IGBT turn-off time, (time between 10% and 90% of V_{CE}), was utilized as a precursor to failure. Here, it was determined that the turn-off time increased with IGBT's die-attach degradation, effectively slowing down the turn-off of the IGBT. This is illustrated in Figure 2.41.

During switching, ringing can occur on the on-state to off-state transition and vice-versa. The ringing in the IGBT switching waveform occurs due to resistive, inductive, and capacitive (RLC) network in the current loop. As IGBTs age, degradation of the RLC network, mainly constituted of parasitic devices, will influence the ringing waveform. Ginart et al. [133] and Brown et al. [164], studied online ringing as a diagnostic technique, to detect degradation in IGBTs. In these studies, the devices were power cycled utilizing the same strategy as proposed by Patil et al. [81]. The ringing was evaluated on a power drive (hex-inverter) test bed with a three-phase induction motor as load. New IGBTs and Aged IGBTs collector-emitter voltage (V_{CE}) ringing characteristics, were compared. Figure 2.42 illustrates these changes.

These studies evidenced a substantial decrease in the IGBTs' ringing once aged. This was mainly caused by a decrease in the rate of change of the collector-emitter voltage (V_{CE}), as evidenced in Figure 2.41.

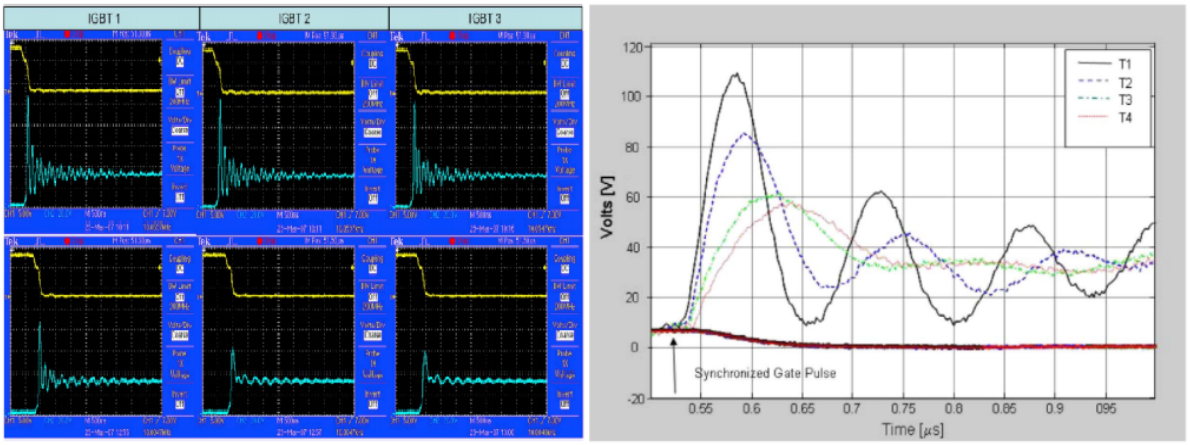


Figure 2.42 - (a) Ringing of (top) New and (bottom) Aged IGBTs (b) Ringing of IGBT when new (T1) and as degradation progresses with power cycling (T2-T3) [133]

Furthermore, this study conducted a Fast Fourier Transform (FFT) analysis on the collector-emitter voltage (V_{CE}) waveforms, to analyze exclusively the spectral changes of the ringing frequencies components with age degradation. Figure 2.43 illustrates this analysis, highlighting an enhanced attenuation of the ringing frequency components with the ageing. Moreover, the study concluded that there was no major change in the actual ringing frequencies. Hayes et al. [137], conducted a Laplacian analysis between new and aged power MOSFETs looking at the poles and zeros shifting of the drain-source voltage (V_{DS}), when subjecting these devices to an ESD based ageing strategy, described in Section 2.8.4. The study showed that after degradation the poles shifted to the left indicating an increase in the output voltage damping but with no significant change in the ringing frequencies.

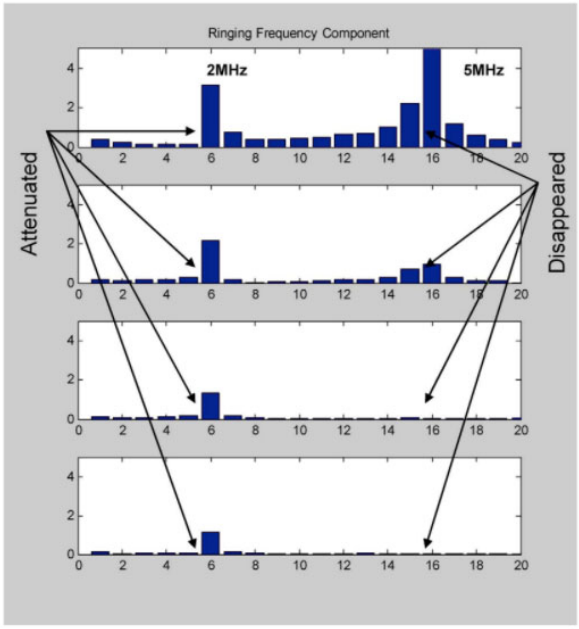


Figure 2.43 – IGBT's Ringing Frequencies Components in relation to ageing progress (top to bottom)

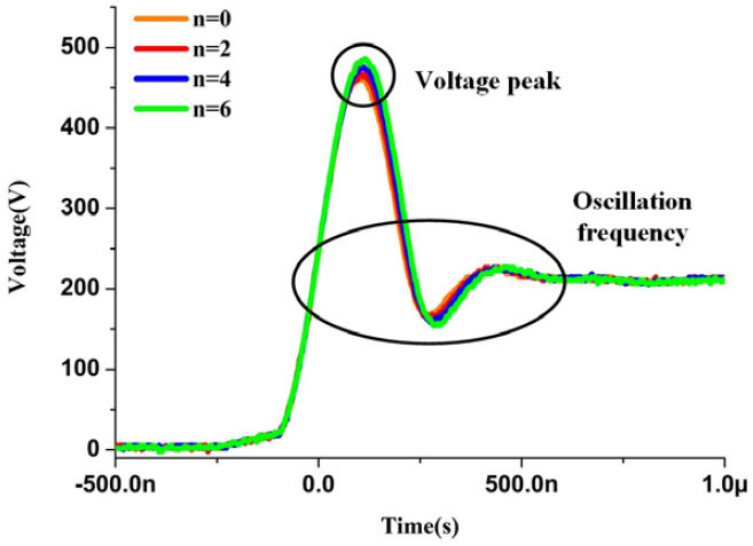


Figure 2.44 – IGBT Module V_{CE} ringing overshoot vs n (number of broken bond wires) [169]

In another study Jing. et al. [169], studied the IGBT modules' collector-emitter voltage (V_{CE}) ringing characteristics in relation to bond wire failure, by monitoring the ringing overshoot and frequency components, predominantly during turn-off. Bond wire degradation was emulated by cutting some of the modules' emitter-metallization bond wires. This study showed that by cutting four bond wires there was a ringing overshoot increase of 5%, when compared to a healthy IGBT module. This is illustrated in Figure 2.44. Moreover, this study characterized the ringing overshoot characteristics in relation to the IGBTs' junction temperature. It showed that the ringing overshoot linearly decreased with the junction temperature (T_J), with minimal changes in the frequency components of the ringing waveform. Hence this study concurs with the studies produced by Ginart et al. [133] and Brown et al. [164], which showed a decrease in the overshoot of the collector-emitter voltage (V_{CE}) due to die-attach degradation which causes an increase in the IGBT's junction temperature (T_J). This is illustrated in Figure 2.45.

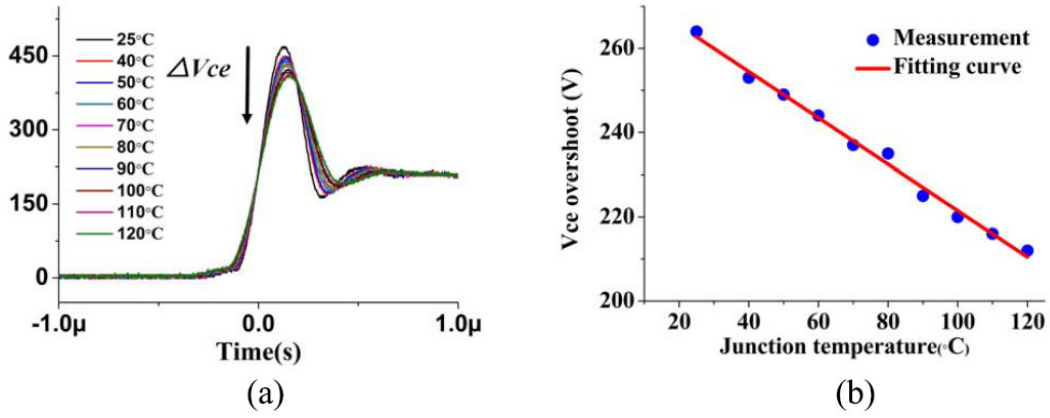


Figure 2.45 – IGBT Module V_{CE} ringing overshoot vs T_J (a) Waveform (b) Fitted Curve [169]

2.9.5 IGBT Conducted and Radiated EMI as a Degradation Precursor

In the previous section, multiple studies have been presented which utilized the IGBT's switching waveforms, highlighting their evolution with ageing, and their implementation as failure precursors. The changes in the IGBT transients due to degradation problems, have an impact on the EM emissions. The relationship between the ageing and degradation of electronic components and the corresponding conducted and radiated EMI, has recently become a major research interest [170-179]. In relation to switching devices, several authors have studied the corresponding EMI disturbances due to device degradation. Beliad et al. [172] studied the EMI ageing effects of RF power MOSFETs. Accelerated ageing, due to electrical overstress, was utilized in this study. It was concluded that ageing produced an increase in the conducted EMI, for frequencies up to 20MHz. It was noticed though, that there were no influences on the spectrum peaks' frequency components. Tlig et al. [174] studied EMI ageing effects in relation to RF L-DMOS devices. Douzi et al. [175] simulated the correlation between conducted EMI and ageing, in relation to a SiC power MOSFETs, while Pu. et al. [178], conducted an experimental study in this regard. Montanari et al. [170] studied these effects in relation to power MOSFETs.

Literature review evidenced that there are few studies, which address the relationship between the conducted EMI and the IGBT device ageing [166-168]. In the study conducted by Tlig. et al. [167], IGBTs were subjected to accelerated ageing consisting of high current, pulsating at a high switching frequency (≈ 50kHz). It was argued that this technique subjected the IGBT to a high junction temperature (T_J). Marginal details, apart from the ones listed above, were provided, in relation to the employed accelerated ageing. This study evidenced an increase in the on-time and off-time of the transient waveforms with device's ageing, effectively slowing down the switching ability of the tested IGBTs.

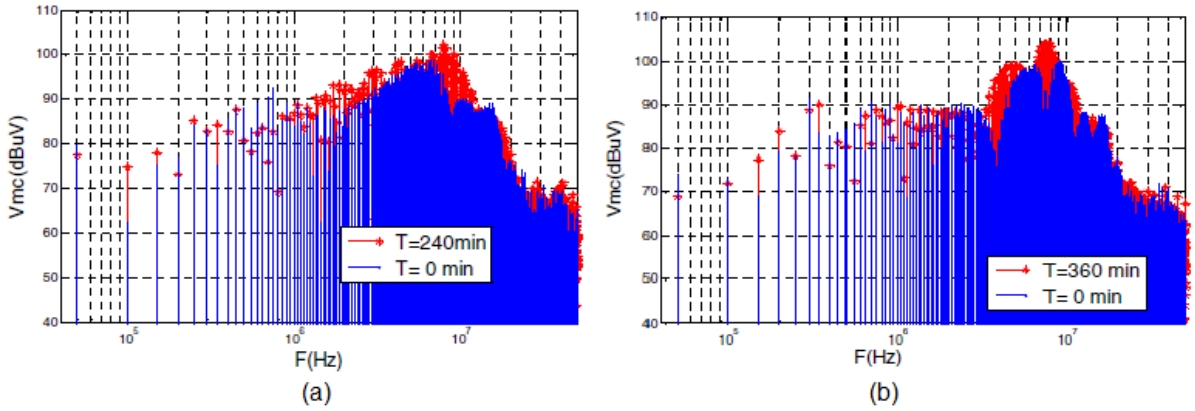


Figure 2.46 – IGBT Conducted Emissions, Ageing Time (a) 240 minutes (b) 360 minutes [167]

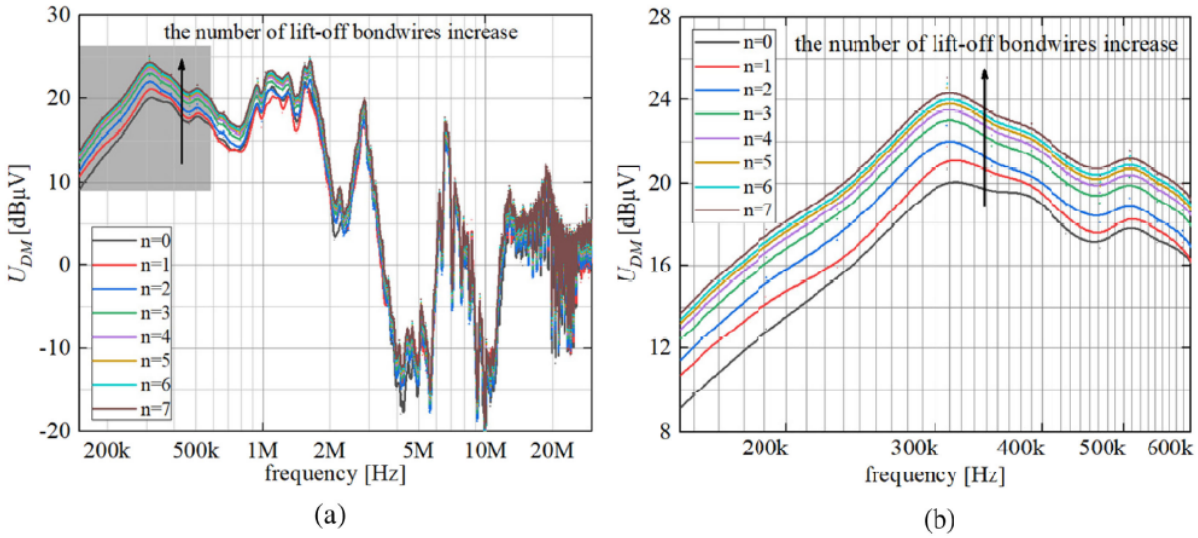


Figure 2.47 – Relationship between the number (n) of lifted-off bond-wires and Conducted EMI (a) Full Frequency Band (c) Low Frequency Band [168]

In relation to the conducted EMI, this study evidenced an increase in the disturbance level, throughout the entire test spectrum (up to 100MHz), with the increase becoming more pronounced as the accelerated ageing time increases. This is illustrated in Figure 2.46. It is important to highlight, that during this study, different devices of the same IGBT make, were subjected to different accelerated ageing periods. Hence the evidenced correlation between enhanced conducted EMI disturbances and accelerated ageing time does not exclude IGBT samples variation. In another study Chu et al. [168], studied the effects of bond-wire lift-off in relation to the conducted EMI of an IGBT module. In this study the IGBT module was utilized within a buck converter circuit. Bond-wires lift-off was emulated through the cutting of bond-wires. This study showed that the larger the number of bond-wires lifted-off, the larger the conducted disturbance, predominantly in the lower frequencies, (150kHz-600kHz).

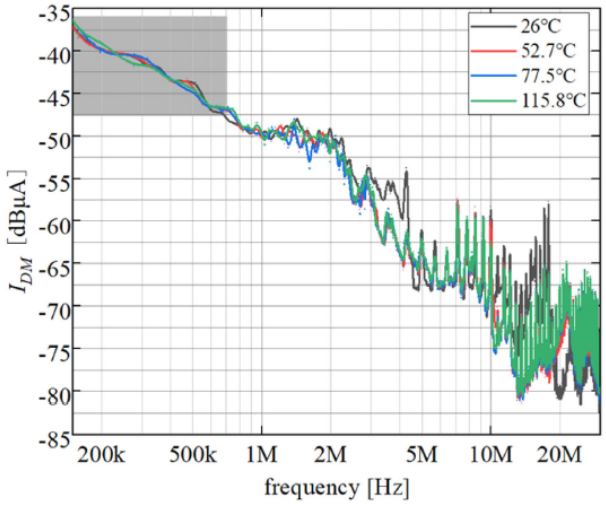


Figure 2.48 – Relationship between Conducted EMI and Junction Temperature (T_J) [168]

On the other side this study concluded, that in the higher spectrum range, this correlation is not that evident, and other elements such as the degradation of the IGBT's parasitic devices might impact more the conducted EMI. This is illustrated in Figure 2.47. Moreover, this study investigated the relationship between the junction temperature (T_J) and the conducted EMI. Again, it showed that there is marginal correlation between the two, and hence it was deemed inconclusive. This is illustrated in Figure 2.48. In another study Feng et al. [166] simulated the ageing effects of an IGBT module in relation to the conducted EMI, focusing on the influences of the IGBT's parasitic capacitances on the conducted disturbances. This was obtained by changing the IGBT's parasitic devices values, namely increase the gate-collector capacitance (C_{GC}) and gate-emitter capacitance (C_{GE}) by 20%, hence emulating ageing degradation. The simulated circuit under test was a traction inverter. Results showed an increase in the spectrum amplitude in the frequency range between 10kHz to 3MHz and a significant increase (≈11dB) in the frequency range from 0.08GHz to 2.7GHz, for conducted common mode voltage. In relation to the differential mode conducted voltage there was an increase of 10dB in the frequency spectrum between 200kHz to 400kHz and from 600kHz to 2MHz. It is important to highlight, that the above, where the only three studies found in literature, which utilized conducted EMI for IGBT condition monitoring. All of them reported enhanced conducted EMI, but this is considered far from conclusive, since in [167] and [168], where actual measurements were conducted, different degradation strategies were employed, hence addressing different IGBT failure modes. Moreover in [168], even though an increase was reported, it could only assert this outcome for lower frequency band of the conducted EMI spectrum, with the correlation for the rest of the spectrum being inconclusive. In relation to the last study, the aim was to assess how changes in the parasitic devices of the IGBT could influence conducted EMI. Even though IGBTs' parasitic capacitance degradation was reported in literature, it is trivial to assess this situation vis-à-vis a real degradation scenario in isolation. Hence this shows, that in this regard there is ample research work to be conducted, which is the main scope of the work presented in this research.

In relation to radiated EMI, only two recent studies were encountered in literature, both by Biswas et al. [179-180]. These studies utilized the radiated EM signature to monitor the health state of IGBTs. In [179], the IGBT was modelled as a magnetic dipole emanating a corresponding magnetic field. The near field magnetic interference was captured by a near-field coil. The health state of the IGBT was based on the picked-up interference signal.

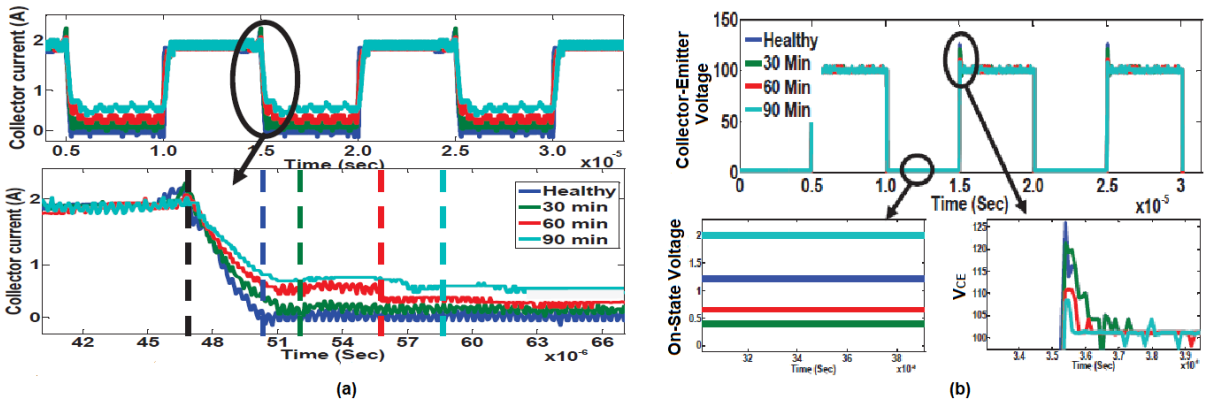


Figure 2.49 – (a) Collector Current (b) Collector-Emitter Voltage Evolution with Ageing [179]

In this study IGBTs' accelerated ageing was conducted through power cycling, operating the devices beyond the recommended SOA and beyond the maximum junction temperature (T_{J_MAX}). This study evidenced that there was an increase in the IGBT's turn-off time predominantly due to an increase in the tail current with IGBT ageing. This effect was concurrently evidenced by this research and will be presented in Chapter 5. The slower collector-current turn-off contributed to a smaller corresponding collector-emitter voltage (V_{CE}) peak and ringing. This is shown in Figure 2.49. Since the slower IGBT turn-off was catalyzed by the slower collector-current transition, this influenced the near magnetic-field interference and hence picked up by the near-field magnetic coil. The corresponding spectrum evidenced that there was a general decrease in the picked-up interference especially at two prominent peaks of the power spectrum 2.4MHz and 7.2MHz, which the author is correlating to the current fall time. This is shown in Figure 2.50.

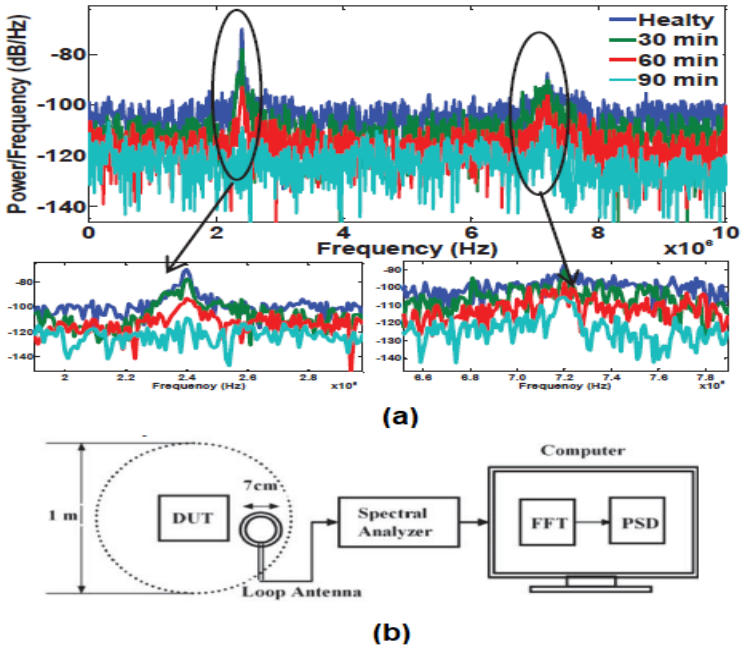


Figure 2.50 – (a) EMR power spectrum evolution with ageing (b) EMR Detection Setup [179].

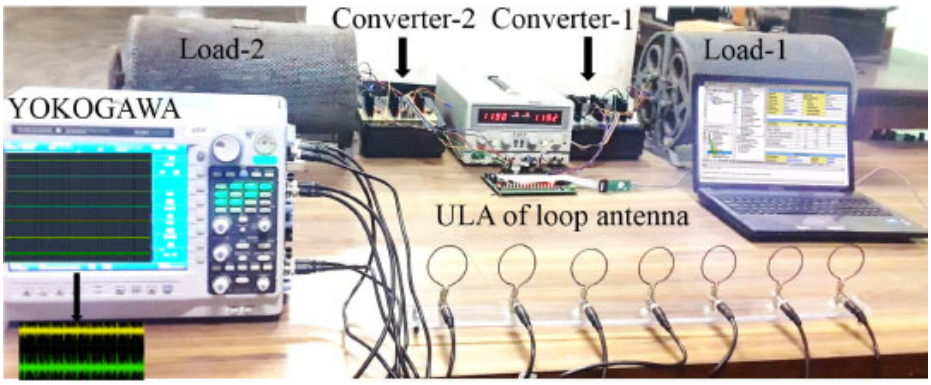


Figure 2.51 – Experimental Setup utilizing a linear array of near-field magnetic probes [180].

In [180], the same author utilized the technique described above to assess the health state of multiple IGBT based power electronic converters when operating simultaneously. This was obtained by utilizing a linear array of near-field magnetic probes. Through the combination of the Estimation of Signal Parameters via Rotational Invariance (ESPRIT) technique and the Multiple Signal Classification (MUSIC) algorithm, the localization of the faulty IGBT was determined. The setup utilized is illustrated in Figure 2.51. The salient advantage of utilizing the IGBT's near-field radiated interference as a precursor to failure, is the non-invasive measurement procedure. However, the disadvantage of this technique, is the fact that in a real application, the near-field radiated signal can be easily affected by external interference, which will influence and hence not guaranteeing the measurement reliability. Compared with radiated interference, the advantage of conducted interference, is that it propagates on the wires and hence it is less prone to external interference. In relation to the technique described in [180], it relies on complex mathematical and signal processing, and hence it might be non-trivial to implement and integrate.

2.9.6 Other IGBT Condition Monitoring Techniques

In the previous sections we have investigated different techniques to determine the health state of the IGBT. They rely on the measurement of either an electrical parameter, transient parameter, or EM emissions signature. In a real power electronic application, the measurement deviation from the nominal healthy state, might be non-trivial to execute, as the hardware and software techniques required to conduct such measurement, might impart on the operational characteristics of the IGBT. Hence other solutions were utilized to minimize the interference of the condition monitoring techniques with the operation of the IGBT. One technique was to integrate a sensor within the power device [181-182]. Another technique utilized Time-Domain Reflectometry (TDR) [183].

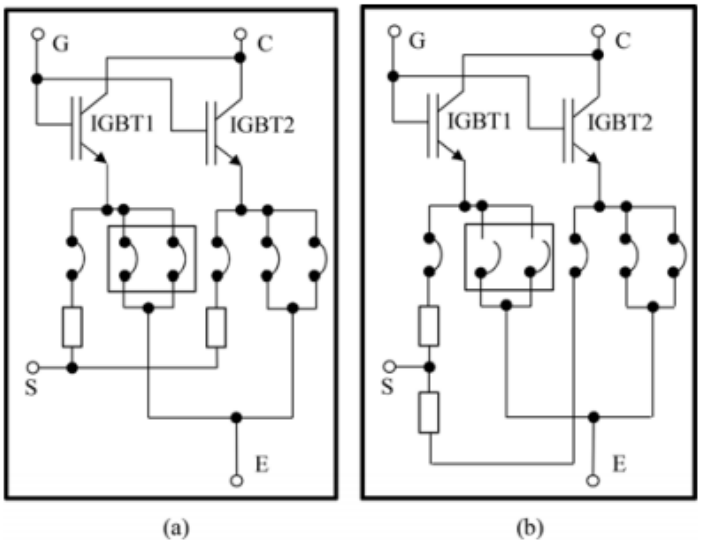


Figure 2.52 – Diagram depicting IGBT Module including sensor integration and redundant emitter bond wires (a) healthy bond wire and (b) emitter bond wires lifted off [181].

Lehmann et al. [181], integrated a sensor within the IGBT module to detect bond wires liftoff. Extra bond wires were connected to the die emitter metallization. These extra bond wires were utilized for measurement only. Failure was detected when the resistance between the emitter terminal and the integrated sensor, departed from the healthy nominal value. This technique proved to be effective and accurately detected bond-wire liftoff. On the other side it entailed a modification of the IGBT module and the implementation of the monitoring circuit. A similar technique was utilized by Ji et al. [181].

Nasrin et al. [183] utilized TDR technique to identify degradation in the power devices namely Power MOSFETs, when utilized within power electronic converters. In this study power MOSFETs were aged using a combination of power and thermal stress. TDR was applied, to identify the damaged power MOSFETs and was conducted while the power converter was in operation. Power MOSFET condition monitoring was achieved, based on the degradation variation of the on-state resistance (R_{DS_ON}). In this study, an impedance matrix was utilized, to identify the location of failure within a single-phase ac-ac converter across different test points. Different TDR impedance responses were recorded across the matrix for a healthy converter state. A reverse matrix impedance mapping has been used to isolate the fault, when compared to healthy responses. This technique is effective but must be carefully implemented since it depends on the power converter circuit's impedance, resistance variations during probing and EMI.

2.10 IGBT Remaining Useful Lifetime (RUL) Modelling

IGBT's precursors to failure are mainly utilized as diagnostics to assess the degree of degradation of the device. Obtaining these distinctive symptoms of degradation are important. On the other side, obtaining the diagnosis only, without further action will not suffice the main purpose of preventing catastrophic failure. Through prognostics techniques IGBT health prediction can be estimated, and the Remaining Useful Life (RUL) can be approximated. Even though the main purpose of this research is to relate to IGBT diagnostic measurements, this section will go through a high-level description of RUL techniques found in literature. Essentially this section will go through two IGBT prognostic techniques namely, Model-Based Prognostic Techniques and Data-Driven Prognostic Techniques.

2.10.1 IGBT Model-Based RUL

Model-based RUL techniques rely on Physics of Failure (PoF) models, obtaining the relationship between different parameters such as device's material properties (i.e. stress or strain) and device's lifetime. The main aim of RUL modelling is to estimate the reliability during product development. An example of RUL modelling is Fatigue modelling, which is mainly designed to forecast the number of cycles before failure under repetitive cycling. In relation to IGBTs this technique is utilized to predict the life expectancy of the IGBT for different failure modes through different failure mechanisms related to different sub-sections of the IGBT.

Fatigue is a failure mechanism which triggers failure modes mainly in bond-wires through bond-wire cracks and lift-off. The main cyclic stressor for this failure mechanism is the peak-to-peak temperature fluctuation. Fatigue RUL models are mainly categorized into four categories: Stress-Based Models, Strain-Based Models, Energy-Based Models and Damage-Based Models [121]. The Damage-Based model has been employed by Sasaki et al. [184] to predict the bond-wires lifetime of an IGBT module. The Coffin-Manson Strain-Based model (Coffin-Manson Equation) [185], as described in Equation 2.9, has been extensively utilized in relation to bond-wire failure under thermo-mechanical fatigue [186-187].

$$\boldsymbol{CTF = a(\Delta T)^{-n}} \tag{2.9}$$

where CTF is the cycle to failure, the model constants a and n are empirical parameters which depend on the IGBT design and ΔT is the peak-to-peak junction temperature.

Another failure mechanism related to IGBTs is surface fatigue, mainly manifesting in the emitter metallization layer. The main cyclic stressor for this failure mechanisms is the peak-to-peak junction temperature fluctuation and mean junction temperature. Empirical models have been provided in [188], in relation to this failure mode. Solder joint fatigue is another failure mechanism which occurs as failure mode within the IGBT's die-attach and terminal leads and manifests as solder-voids, solder-cracks and delamination. The main cyclic stressor for this failure mechanism is the peak-to-peak junction temperature fluctuation and the mean junction temperature. Coffin-Manson models [188] and empirical Norris-Landzberg equation [189] has been employed for the RUL of this kind of failure mechanism. In relation to IGBT modules ceramic fatigue can occur within the DCB substrate mostly manifesting as cracks. The main cyclic stressor for this failure mechanism is vibration and mechanical forces. Empirical models in relation to this failure mode have been provided in [188]. Another failure mechanism is electromigration (described in section 3.1.1), which can contribute to void formations in bond-wires and metallization layers. The main cyclic stressor for this failure mechanisms is current density and elevated junction temperature. It was already discussed that empirical equations such as Black's law, has been utilized to model the RUL for this type of failure.

2.10.2 IGBT Model Based RUL at Product Development Stage

The above RUL models are catering for a particular failure mechanism in isolation and are not taking into consideration the combination of failure mechanisms. Hence RUL models must take into consideration the interaction of different failure mechanisms. Moreover, as package technologies evolve, the introduced effects must be included. IGBT manufacturers derive new RUL models which include the introduced packaging advancements. Held et al. [190], derived one of the initial RUL empirical models where the main model variables were the peak-to-peak temperature fluctuation (ΔT_J) and mean junction temperature (T_{J_MEAN}). The main failure mode included in this empirical model, was bond-wire lift-off. Equation 2.10 describes this empirical RUL model, which was mainly intended for 90's package technology, and utilizing aluminium-oxide (Al_2O_3), for substrates.

$$CTF = K\Delta T_J^{\alpha} e^{\frac{E_{ACT}}{kT_{Jmean}}} \tag{2.10}$$

where CTF is the Cycles-To-Failure, K is an empirical model constant, to be adjusted for best match of model with experimental test data, ΔT_J is the peak-to-peak junction temperature

fluctuation, k is the Boltzman's constant $1.38x10^{-23}JK^{-1}$, T_{JMEAN} is the mean junction temperature in Kelvin, E_{ACT} is the activation energy 0.618eV and $\alpha = -5.039$ a model constant.

A similar RUL model in relation to bond-wire failure, was later developed by Bayerer et al. [191], which included the latest IGBT design advancements at the day of publishing. The main model variables included the peak-to-peak temperature fluctuation (ΔT_J) and minimum junction temperature (T_{J_MIN}), the heating time (t_{on}) (which is the current load pulse duration), the current carrying capability of each bond-wire (I), voltage capability of the IGBT (V) and the bond wires' diameter (D). This RUL model predominantly relates the IGBT life with the influence of bond wires thickness, the amount of bond wires per die and the die thicknesses. Bayerer et al. [191], argued that the IGBT's bond wires life does not depend solely on the peak-to-peak junction temperature (ΔT_J) variation and the mean junction temperature (T_{J_MEAN}), but depends as well on the stress distribution and geometrical design criteria. Like the RUL model provided by Held et al. [190], this model caters for package technologies which utilizes aluminium-oxide (Al_2O_3), for substrates but reflecting 2000's technology. This model is not adequate for IGBTs constructed with Aluminium-Nitride (AlN) and Aluminium-Silicon-Carbide (AlSiC) substrates. Equation 2.11 describes this empirical RUL model.

$$CTF = K\Delta T_J^{\beta 1} e^{\frac{\beta_2}{T_{JMEAN}}} t_{on}^{\beta_3} I^{\beta_4} V^{\beta_5} D^{\beta_6} \tag{2.11}$$

where CTF is the Cycles-To-Failure, K is an empirical model constant, to be adjusted for best match of model with experimental test data, $\beta_1 = -4.416$, $\beta_2 = 1285$, $\beta_3 = -0.463$, $\beta_4 = -0.716$, $\beta_5 = -0.716$, $\beta_6 = -0.5$ while the other parameters were described earlier on.

Another more recent IGBT empirical RUL model is the one proposed by Scheuermann et al. [192], including in the model a solder-free, sintering-based IGBT module technology. The main model variables included are the peak-to-peak junction temperature fluctuation (ΔT_J), the mean junction temperature (T_{J_MEAN}) and the heating time (t_{on}) which is the current load pulse duration. The Al bond wire aspect ratio was included in this model, as in previous studies it was observed that by increasing the height of the bond wire loops, bond wire lifetime was enhanced. Furthermore, a de-rating factor was included in this model to include also the free-wheeling diode effects. The model was built after 97 experiments collected over five years [193]. The main scope of this RUL model again was to determine IGBT lifetime in relation to bond-wire failure and is described in Equation 2.12.

$$CTF = K.\Delta T_J^{\alpha}.(ar)^{\beta 1 \Delta T_J + \beta_0}.\left\{\frac{C+t_{on}^{\gamma}}{C+1}\right\}.e^{\frac{E_a}{k_B T_{JMEAN}}}.f_{DIODE} \quad (2.12)$$

where CTF is the Cycles-To-Failure, K is an empirical model constant, to be adjusted for best match to experimental test data, β_0 = 1.942, β_1 = -9.012x10^{-3}, C = 1.434, γ = -1.208, E_a = 0.06606eV, f_{Diode} = 0.6204, α = -4.923, while the other parameters were described earlier on.

Parameters such as the Cycles-To-Failure (CTF), the junction temperature fluctuation (ΔT_J) and the mean junction temperature (T_{JMEAN}), were all in some way considered and logged during the different IGBT's accelerated ageing procedures conducted throughout this work, as described in Chapter 3, Section 3.3.4 for the studied IGBT with a TO-220 package. The different empirical model constants need to be re-adjusted to reflect this kind of package and to best match the obtained experimental data.

2.10.3 IGBT Model-Based RUL Applied in the Field

All the above RUL models are based on cycles which are identical. This is valid for experimental conditions but not in real-life applications, where lifetime stressors might not be cyclic, and cycles are not identical. In relation to the above RUL models, this will entail junction temperature (T_J) profiles which are not cyclic and hence complex.

Hence during real lifetime estimation, the stressor's complex load profile must be converted to simple identical cycles. In literature this conversion is achieved through the Rain-flow Counting Algorithm (RCA) [194-195], with the main scope of reducing varying stressor data into equivalent simple stressor cycles. Hence when IGBTs are subjected to electro-thermal stress, model-based lifetime estimation is achieved by generally conducting the following:

- Electrical load data and thermal data such as the ambient temperature (T_A) are to be defined, to be included within the estimation process. These are important, to calculate the corresponding IGBT losses and junction temperature (T_J) profile determination, like the procedure described in Section 2.8.3.
- The junction temperature profile (T_J) which commonly is complex, is inputted to the RCA to obtain equivalent simplified junction temperature (T_J) cycles.
- At this point the empirical RUL models as proposed by Held et al. [190], Bayerer et al. [191] or Scheuermann et al. [192], are utilized to estimate the CTF.
- The obtained CTF is in terms of the peak-to-peak junction temperature (ΔT_J) cycles, and hence must be translated to actual significant lifetime. This is commonly achieved

through the utilization of damage models. One of the simplest and extensively utilized damage models, especially for IGBTs, is the Miner's Cumulative Damage model equation [196-197]. This is described in Equation 2.13.

Miner's cumulative damage equation states that if there are k different stress level magnitudes, in the range of S_i ($1 \leq I \leq k$), each contributing $n_i(S_i)$ cycles, then if $N_i(S_i)$ is the number of cycles to failure, for a constant stress, the corresponding damage fraction C is given by [198]:

$$\sum_{i=1}^{k} \frac{n_i}{N_i} = C \tag{2.13}$$

If the damage fraction reaches the value of 1, failure occurs. Miner's equation provides the proportion of life consumed at each stress cycle. This equation assumes that the damage is the same across all the stress cycles, hence assuming, that the damage level accumulates linearly. This is not always the case, as non-linear relationship between cycles and damage can exist, especially when considering multiple degradation sources. Hence alternative damage models were employed in literature including the Double Linear Damage Rule [199], the Non-Linear Damage Rule [200] and Crack Growth Rule [201]. Having said that, the Miner's Linear Damage model in conjunction with the RCA is a popular lifetime estimation technique for IGBTs. This technique is not taking into consideration other ancillary degradation sources apart from those contributing to the stress cycles. Typical ancillary degradation sources can include humidity, corrosion, and cosmic ray radiation. These contribute to shorter lifetimes than the model's estimate.

The RUL models described above, most of them rely on cycles defined by the peak-to-peak change in the junction (ΔT_J) temperature and the mean junction temperature (T_{J_MEAN}). It has been already discussed that these stressor parameters, trigger both failure mode in the bond-wires as well as in the solder/metallization layers. Hence it is of interest, that even RUL prediction, discriminates between the two failure modes. An interesting study was conducted by Morozumi et al. [202] in this regard. This study evidenced the differentiator between the IGBT bond-wires and solder layers degradation. The first interesting result was the fact that IGBT packages which utilised lead (Pb) based solder layers experienced a lower cycles lifetime when compared to lead (Pb) free solder layers. This was true over the entire range of the tested peak-to-peak junction temperature (ΔT_J). Another interesting result was that when lead (Pb) based IGBT packages were tested at high mean junction temperature (T_{J_MEAN}) and hence low

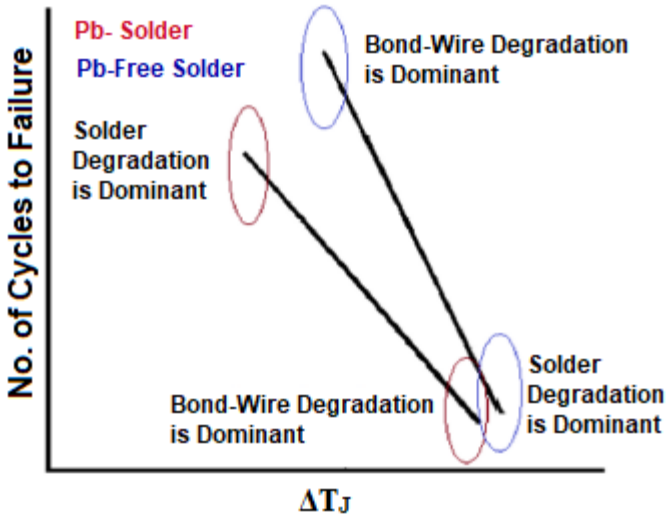


Figure 2.53 – Relationship Thermal cycles and (Pb) Solder and (Pb)-Free Solder IGBTs [202]

peak-to-peak junction temperature (ΔT_J), the solder layer degradation was the predominant failure mode. On the other side when the mean junction temperature (T_{J_MEAN}) was kept relatively low, hence with enhanced peak-to-peak junction temperature (ΔT_J), the predominant failure mode was bond-wire degradation. This behavior was inverted for lead (Pb) free solder layers packages. This is illustrated in Figure 2.53. Morozumi et al. [202] related this behavior to the material properties of leaded (Pb) solder and lead (Pb) free solder, as leaded (Pb) solder degradation occurs due to a permanent distortion that occurs when this material is subjected to tensile and compressive stress due to thermal cycling. On the other side lead (Pb) free solder degradation occurs predominantly due to grain formation and growth. This explains the degradation variation between these two materials. In another study Junghaenel et al. [203] managed to isolate the relationship of the collector-emitter saturation voltage (V_{CE_SAT}) and junction temperature (T_J) versus power cycles vis-a-vis solder-layer degradation and bond-wire degradation.

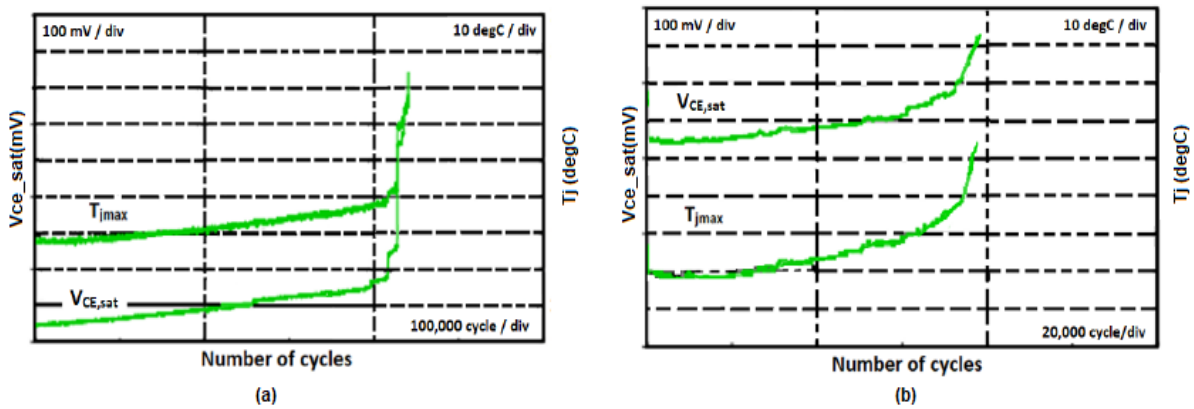


Figure 2.54 – V_{CE_SAT} & T_J relationships with cycles (a) Bond Wire (b) Solder Degradation [202]

This study showed that both failure modes manifested an increase in the corresponding collector-emitter saturation voltage (V_{CE_SAT}) and junction temperature (T_J). The main differentiator was that in the case of bond-wire degradation the increase was sudden, while for the solder degradation the increase was slower. Moreover, solder failure manifested earlier than bond-wire failure. This is illustrated in Figure 2.54.

2.10.4 Data Driven Prognostic Techniques

Fundamentally, RUL-model based prognostic techniques make use of data such as material characteristics, electrical load data, ambient temperature (T_A), stress distribution, geometrical design criteria, peak-to-peak junction temperature (ΔT_J) and mean junction temperature (T_{J_MEAN}), to approximate the lifetime of the IGBT. Hence, model-based RULs, require IGBT characteristic knowledge during a failure mechanism. Data driven prognostic techniques, essentially do not require IGBT characteristic knowledge, but rather health monitoring is based on past performance data without relying on any lifetime model equation. In this case lifetime is estimated utilizing statistics, probability theory and machine learning techniques. Hence data-driven RUL prognostics, iteratively determines and updates the time-to-failure probability distribution. This technique has been utilized in [204], to determine the health state of IGBTs. In this study the Mahalanobis Distance (MD) based probabilistic threshold technique was used to detect anomalies in the measurement of the collector-emitter saturation voltage (V_{CE_SAT}). The change in the collector-emitter saturation voltage (V_{CE_SAT}), which corresponded to a failure, was taken to be of 20%, from the measured value when the IGBT was new. Moreover, particle filters were applied to predict the time to failure. It was reported that from the anomaly detection, the implemented particle-filter technique managed to predict the IGBT remaining lifetime within an error of 20%. This was achieved during experimental conditions, and hence further work is required to conduct RUL predictions based on this technique, when IGBTs are utilized in the field.

In another study by Liu. et al. [205], a Novel Volterra k-Nearest Neighbor Optimally Pruned Extreme (VKOPP) machine learning model was utilized to determine the time-to-failure of IGBTs. In this study, IGBT degradation data of collector-emitter saturation voltage (V_{CE_SAT}) and collector-emitter current (I_{CE}) was utilized for the machine-learning technique training. Here, seven prediction models were compared to analyze the best prediction technique, with the proposed VKOPP technique obtaining the prediction with least error. Furthermore, it was argued that the implemented machine learning algorithm requires a small number of training

cycles. On the other hand, the computational intensity of the implemented technique is still considered an issue. In a recent study Ge. et al. [206], implemented a data-driven IGBT RUL technique based on the degradation changes of the transient signal of the collector-emitter voltage (V_{CE}). The log-log ratio of the collector-emitter voltage (V_{CE}) was reputed a better statistical feature to evidence the degradation degree of the IGBT. Moreover, a Kalman filter was utilized to eliminate noise in the data, after which a DeepAR Recurrent Neural Network (RNN) was used to predict the RUL of IGBTs. This technique was compared with an Auto Regressive Integrated Moving Average (ARIMA) and Single Exponential Smoothing (SES) methods, with the implemented DeepAR technique producing the best prediction result. Moreover, this study modified the IGBT Hefner model [207], to simulate transient IGBT waveform, to include the degradation effects. This involved solely a change in the threshold voltage (V_{THRES}), arguing that this only change triggered the corresponding changes in the collector-emitter voltage (V_{CE}) transient. The validity of this observation will be thoroughly discussed in Chapter 3.

As discussed in Chapter 3, the presented work showed measurable changes in relation to the implemented accelerated ageing, with repeatable trends in different IGBT's parameters such as the threshold voltage (V_{THRES}), collector-emitter on-state voltage (V_{CE_ON}), forward transconductance (g_{fe}) and the internal free-wheeling diode forward voltage (V_{FD}). The above listed data driven techniques can be based on the changes experienced by the above parameters to obtain lifetime estimations of the IGBT, with the threshold voltage (V_{THRES}) providing a better correlation in relation to the health-state of the gate, the collector-emitter on-state voltage (V_{CE_ON}) in relation to the health-state of the IGBT's die-attach and the internal free-wheeling diode forward voltage (V_{FD}) in relation to the health-state of the internal free-wheeling diode's die-attach.

2.10.5 Applicability of IGBT RUL Estimation

State of the art IGBT RUL estimation, being model-based or data-driven, still demands for further research in relation to their applicability in various real-field scenarios. Reviewed literature, as evidenced in section 2.6.6, highlighted IGBT field failures due to bond-wire fatigue, solder layers fatigue, ESD, cosmic-rays, latch-up and ceramic substrate fracture. When considering this spectrum of failure mechanisms, state-of-art RUL techniques only address a portion and hence further research is required to address the other failure mechanisms.

Moreover, in field-applications, IGBTs are subjected to varying operating conditions such as switching frequency, duty cycle, load, and environmental conditions. For example, a varying ambient temperature (T_A), incurs on the collector-emitter saturation voltage (V_{CE_SAT}) and hence it will affect the outcome of the RUL estimation if not considered. The presented IGBT RUL studies were conducted under controlled experimental conditions and hence their performance may differ under operational-field conditions. Hence further research is required to come up with IGBT RUL techniques that can include field-operation, discriminate between different failure mechanisms, and more importantly are based on precursor parameters which are not affected by multiple failure mechanisms, especially competing failure mechanisms. A case in point is the collector-emitter saturation voltage (V_{CE_SAT}) as explained in 2.10.3.

2.11 Conclusions

This chapter presented a thorough literature review in relation to IGBTs' failure mechanisms and the corresponding effects. The main PoF mechanisms related to semiconductor devices were presented in this chapter. In relation to IGBTs the predominant PoF mechanisms were identified to be Electromigration (EM) and Hot Carrier (HC) effects, where EM mainly affects the IGBT's bond-wires and metallization layers, while HC mainly affects the gate's dielectric oxide. Moreover, a detailed explanation of the IGBTs' structure and corresponding manufacturing process at both die and package levels was presented. Consecutively, the multiple IGBT's die, and package related failure mechanisms were shortlisted and explained. In addition, a detailed IGBT FMEA was conducted, based on the failure mechanisms encountered in literature. Successively, the IGBTs' reliability tests performed in industry were reviewed, leading to a detailed description of the IGBT's accelerated ageing and power cycling methodologies encountered in literature. At this point a detailed discussion of the different IGBT's precursors to failure, as identified in literature, was conducted. It was established that the IGBT's precursor techniques, which employ conducted EM emissions, were minimally investigated, in literature, hence providing a gap in knowledge and hence room for further study Finally, different prognostic techniques developed to predict and estimate the lifetime of IGBTs were analyzed and discussed.

Chapter 3 IGBT Accelerated Ageing & Characterization System

This chapter provides the details of the developed IGBT's Power Cycling Ageing System (PCAS). Initially, the identified system's requirements to achieve the required IGBT degradation, are reported. This leads to a detailed description of the design and development of the required PCAS's hardware and software. Eventually, this chapter provides the details of the implemented IGBT accelerated ageing procedure, highlighting the corresponding operational process and performance results. This is followed by the IGBT's mechanical characterization (conducted through X-Ray inspection), to confirm and evaluate the type and severity of the inflicted degradation. This leads to the characterization of the IGBT's static electrical parameters which is achieved through the development of the static electrical parameters' characterization testbed, hence providing a wide description of the hardware and software, design, and development, of this testbed. Finally, the obtained static electrical parameters characterization results are presented and discussed.

3.1 Aim of the Proposed Accelerated Ageing System

The main aim of this part of this research is to provide an understanding of the changes in the IGBTs' electrical parameters, when subjected to power cycling accelerated ageing. The correlation of the measured changes to the inflicted degradation, can be utilized within prognostic techniques to determine the health state of the device. As described in section 2.8.2, the main catalysts to perform accelerated ageing, as reviewed in literature, are elevated junction temperature (T_J) and peak-to-peak change in the junction temperature (ΔT_J). Hence, the main idea is to utilize these catalysts within a DC PCAS architecture to age discrete IGBT transistors.

3.2 Accelerated Ageing System Requirements

This section describes the identified DC PCAS architecture's system requirements for the research framework proposed. Table 3-1 provides the details of the identified requirements for the different subsystems including the IGBT activation, temperature measurement, node voltages and current measurement, and power handling capabilities.

Req. No.	Requirement Description
1	The DC PCAS is intended to accommodate PT IGBT transistors.
2	IGBT Transistors to be chosen for this study will have to be commercially available.
3	The DC PCAS will be based on reviewed thermo-electric overstress approach. This approach will enable correlation to the results presented in reviewed literature as well as an indirect verification and validation of the ageing procedure.
4	The DC PCAS must be able to record electrical, mechanical, environmental, transient, and spectral parameters, to control the ageing and preform the characterization of the ageing effects.
5	The DC PCAS must be designed flexible enough, such that it can allow additional instrumentation and control systems if required.
6	The DC PCAS must be designed to perform ageing autonomously, while limiting the human intervention to configure and start the ageing procedure.
7	The DC PCAS must provide a user interface for the user to configure and initiate the ageing procedure, as well as monitor the different parameters during the ageing process.
8	The DC PCAS must allow for both elevated junction temperature (T_J) and peak-to-peak change in the junction temperature (ΔT_J) as the accelerated ageing catalysts.
9	The DC PCAS must have the capability to accurately measure and log the IGBT's case temperature (T_C).
10	The DC PCAS must have a gate drive voltage capability which exceeds 20V, to induce gate overstress.
11	The DC PCAS must have a gate drive slew rate capability of at least 1V/ns, due to typical IGBT discrete transistors' fall times and rise times in the range of tens to hundreds of nanoseconds.
12	The DC PCAS must have a gate drive, capable of driving a maximum gate input capacitance of 10nF.
13	The DC PCAS must have a gate circuitry capability which enables and disables with electrical isolation the gate signal from the IGBT.
14	The DC PCAS must cater for IGBT discrete transistors with a maximum continuous collector current carrying capability of 20A and DC blocking voltage capability of 800V.
15	The DC PCAS must provide a DC power supply that is capable of a current capability in relation to the capability of the IGBT discrete transistors that is 20A. Furthermore, any utilized loads and custom designed PCBs must be capable of withstanding this load current.
16	The DC PCAS must provide a maximum power supply DC voltage capability of 50V. This voltage reflects the fact that the DC PCAS architecture does not require a high voltage DC link.
17	The DC PCAS must measure and log the gate-emitter node voltage (V_{GE}) and the collector-emitter node voltage (V_{CE}). Moreover, the DC PCAS must measure and log the gate current (I_G) and collector current (I_C). Furthermore, the DC PCAS should be flexible enough to allow the inclusion for the acquisition of the high-speed transient signals of the above node voltages and currents.

Table 3-1 - Proposed DC PCAS Requirements

3.3 Implemented PCAS Design

Figure 3.1 illustrates the proposed DC PCAS high-level architecture, based on the PCAS system proposed by Sonnenfeld et al. [132], utilizing a thermo-electric overstress approach, where the device will experience power pulses without the use of a heat sink to cause self-heating. The implemented DC PCAS is of the constant case-temperature peak-to-peak fluctuation ($T_{C\_PK\text{-}PK}$) procedure type, as it provides the best compromise between stress level, accelerated ageing control, best real field-degradation representation, and data reliability to conduct lifetime estimations. The system was designed to autonomously monitor and control the device temperature while recording electrical and environmental parameters. It consists of three main sections: the commercial instrumentation, the custom-built hardware and custom-built software.

3.3.1 PCAS Commercial Instrumentation

The commercial instrumentation includes a Tektronix MDO4104B-3 Mixed Domain Oscilloscope, which consists of a hybrid oscilloscope with specifications of 1GHz bandwidth and sampling of 5 GS/s scope and a 3GHz bandwidth spectrum analyzer.

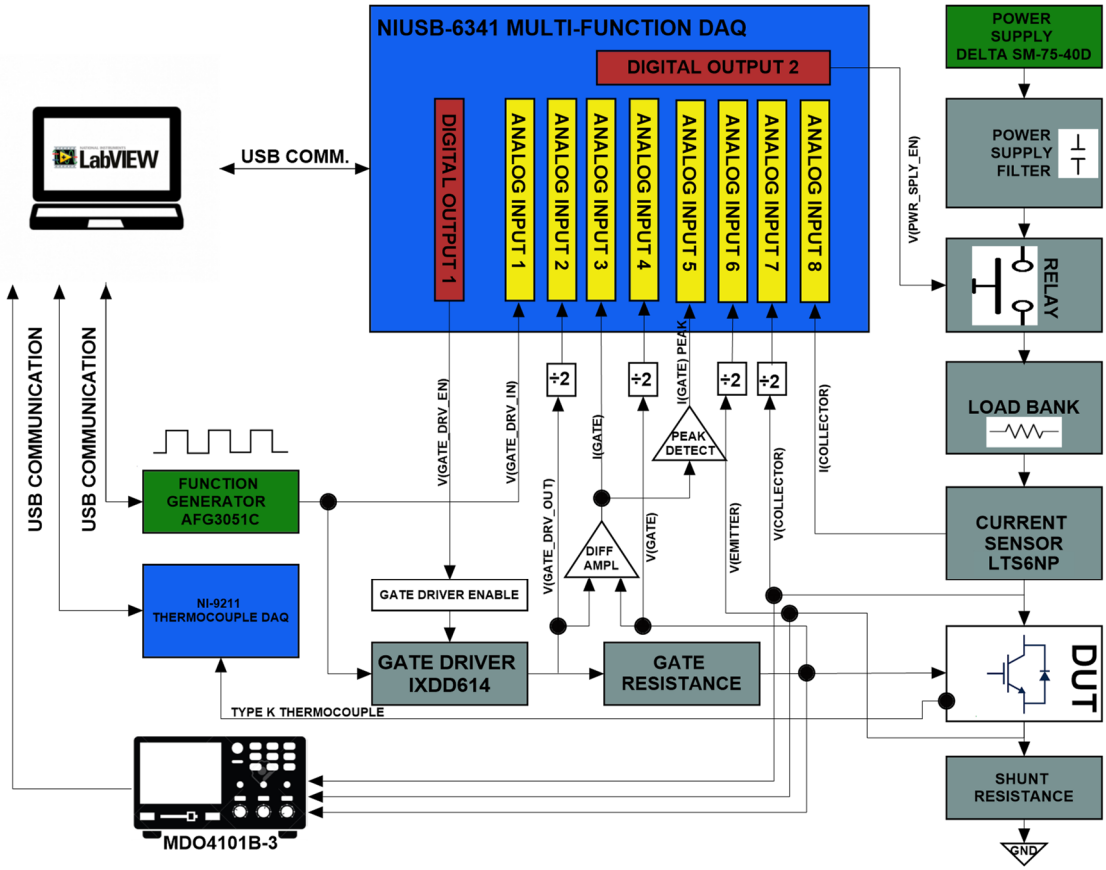


Figure 3.1 - Overview of the Accelerated Ageing & Characterization System

The main purpose of the oscilloscope is to capture high-speed transient signals and store them. Furthermore, it can be interfaced with the PC via Universal Serial Bus (USB) or Ethernet with supported drivers for the National Instruments (NI) Labview programming environment, for the remote configuration of the oscilloscope and the retrieval of the captured high-speed data. The Tektronix AFG3051C programmable arbitrary function generator was utilized to generate the gate signal. It provides a USB interface for controlling the gate signal via the PC. Three different power supplies were utilized, the first power supply is the DELTA SM 70-45 D which is a 70V, 45A power supply, solely utilized as the power source for the power pulses through the DUT. Two other power supplies, DELTA ES030-5 30V, 5A, were utilized for powering the signal conditioning and acquisition electronics within the custom-built hardware. Two National Instruments (NI) DAQ systems were utilized. The NI DAQ, NI-9211 4-channel temperature module, with a sampling rate of 14S/s for temperature data acquisition. The module includes anti-aliasing filters and capable of detecting open-thermocouple scenarios and cold-junction compensation for higher accuracy. This module was mainly utilized to measure the case temperature (T_C) of the Device Under Test (DUT). The second DAQ is the NI-USB-6341, which is a multi-function DAQ with 16 analogue inputs with capabilities of 500kS/s, 2 analogue outputs with 900kS/s and 24 digital input/output ports. This DAQ, was utilized for the acquisition of the DUT's electrical signals during the accelerated ageing procedure. Moreover, this DAQ was utilized to control the ageing process via the switching of the two digital outputs, which control the activation of the gate drive signal from the DUT, and the activation of the power supply current route through the DUT.

3.3.2 PCAS Custom-Built Hardware

Figures 3.2 and 3.3 illustrate the schematics for the IGBT PCAS circuit board. The board can be divided into three sections: IGBT control section, signal conditioning section. and power section. Figure 3.2 illustrates the circuit for the DUT's control and power sections. The IGBT circuit is set in a common-emitter configuration. The circuit consists of an IXYS IXDD614 high-speed gate driver (DRV1). This gate driver is a 14A sink/source gate driver hence capable of driving large input capacitances. Furthermore, it can operate with a maximum input voltage of 35V DC, generating a corresponding gate drive high-side signal, up to this voltage level, hence exceeding the 20V DC IGBT's discrete transistor gate voltage general limit, thus causing gate overstress if required. Furthermore, this driver can generate a low-side signal, down to -5V DC, if hard cut-off is required. Moreover, it can produce rise times and fall times less than 30ns. The IXDD614 has also an integrated "Enable" functionality which enables or disables

the driver's output signal. This feature was utilized by the temperature controller to control the DUT's case temperature (T_C), intended to be activated via one of the NIUSB-6341 DAQ digital output ports, through the intermediary activation of a low-power MOSFET (Q2). The gate was furthermore protected with clamping zener diodes (Z1 and Z2) to protect against undesired gate over and under-voltages.

The switching behavior of the DUT is controlled by the charging/discharging of the gate input capacitance. This capacitance charging is controlled by the gate resistance R_G (R7). Hence R_G dictates the dynamic performance of the gated transistor, by influencing the switching time and switching losses, dictating what time is needed to charge and discharge the gate by limiting the magnitude of the gate current pulses during turn-on and turn-off. Reducing the gate resistance, the turn-on and turn-off time will be shorter, and the switching losses will be reduced. On the other hand, the reduction of the gate resistance, increases the dI/dt effects due to stray inductances in the circuit, which can produce voltage spikes on the IGBT. So even though the gate resistance R_G should be ideally zero, the gate resistance prevents unnecessary ringing. In this case a 5Ω gate resistance was utilized. Moreover, a 2.2kΩ pull down resistor (R8) was added to the gate, to avoid a floating gate terminal once the gate drive is disabled.

On the output side of the DUT, an LTS-6NP Hall-effect current transducer (SNS1) was utilized. This transducer is capable of measuring DC, AC, and pulsed currents with a bandwidth up to 100kHz. The selected sensor has continuous current measurement capability of up to +/-40A. The device provides a corresponding output voltage varying from 0V to 5V corresponding to the -/+40A current range, with 2.5V corresponds to 0A. Furthermore, in series with the IGBT's collector, a high-power connector was utilized to connect the load (CON3). Another connector was utilized in series with the emitter to possibly connect a shunt resistance for transient collector current monitoring (CON4).

Moreover, a NEC/TOKIN EM1-2U1S 54A normally closed power relay (RLY1) was utilized in series with the load. The scope of this protection relay is to control the switch-on/off, of the DUT's output power when the IGBT goes into latch-up and could not be switched-off via the gate. This avoids severe thermal runaway and DUT's destruction.

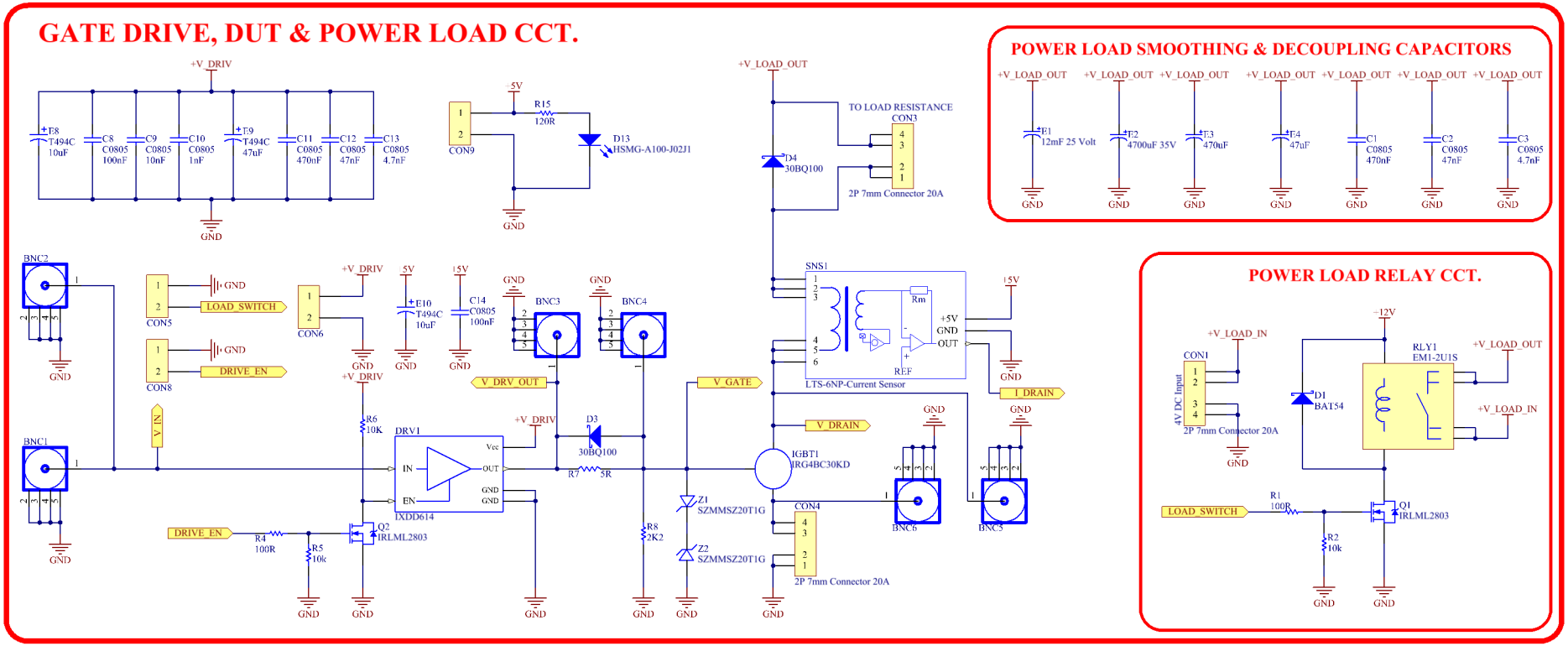


Figure 3.2 - IGBT DC PCAS Custom-Built Hardware, Control and Power Circuit Section.

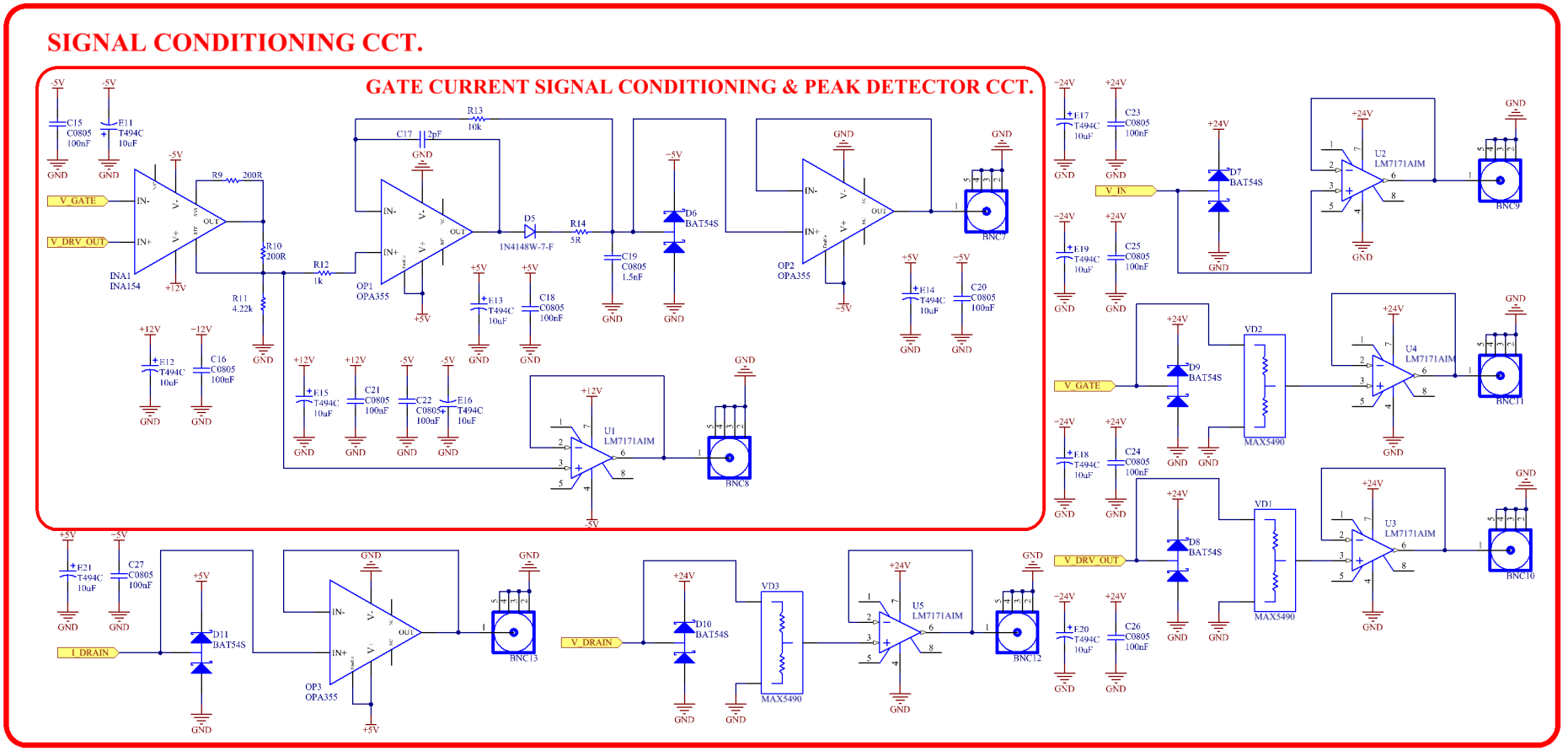


Figure 3.3 - IGBT DC PCAS Custom-Built Hardware Signal Conditioning Circuit

This relay was designed to be controlled via the NIUSB-6341 DAQ digital output port, through an intermediary low power MOSFET (Q1). Four bulk capacitors (E1-E4) were connected in parallel with the DUT's output power supply, to lower the transient impedance, and mitigate cable inductance effects. Figure 3.3 illustrates the signal conditioning section. Node voltages including the gate voltage (V_G), gate driver output (V_{DRIVE}), emitter voltage (V_E), and collector voltage (V_C), were all precisely divided by two, in hardware, through the individual utilization of MAX5490, a 100kΩ precision-matched resistor divider (VD1-VD3). This was conducted since the voltage range of these signals can exceed the analog input voltage limit of the NIUSB-6341 DAQ. Eventually these signals were over and under voltage protected (D8-D10), buffered (U3-U5), and supplied via BNC connectors (BNC10-BNC12) and RG-58 coaxial cables to the NIUSB-6341 DAQ. Moreover, the function generator output signal (V_{IN}) and transduced collector current (I_C) signal, were over and under voltage protected (D7 and D11), buffered (U4 and OP3), and supplied via BNC connectors (BNC9 and BNC13) and RG-58 coaxial cables to the NIUSB-6341 DAQ. The gate current was also captured by obtaining the potential difference across the gate resistance (R7). An INA154 instrumentation amplifier (INA1) was utilized to amplify this voltage difference. Furthermore, a fast peak detector (OP1) was designed to obtain the peak gate current, as this can provide useful information on the gate degradation. BNC connectors were added at important nodes such as the function generator voltage (V_{IN}), output gate drive (V_{DRV}), gate voltage (V_G), emitter voltage (V_E) and collector

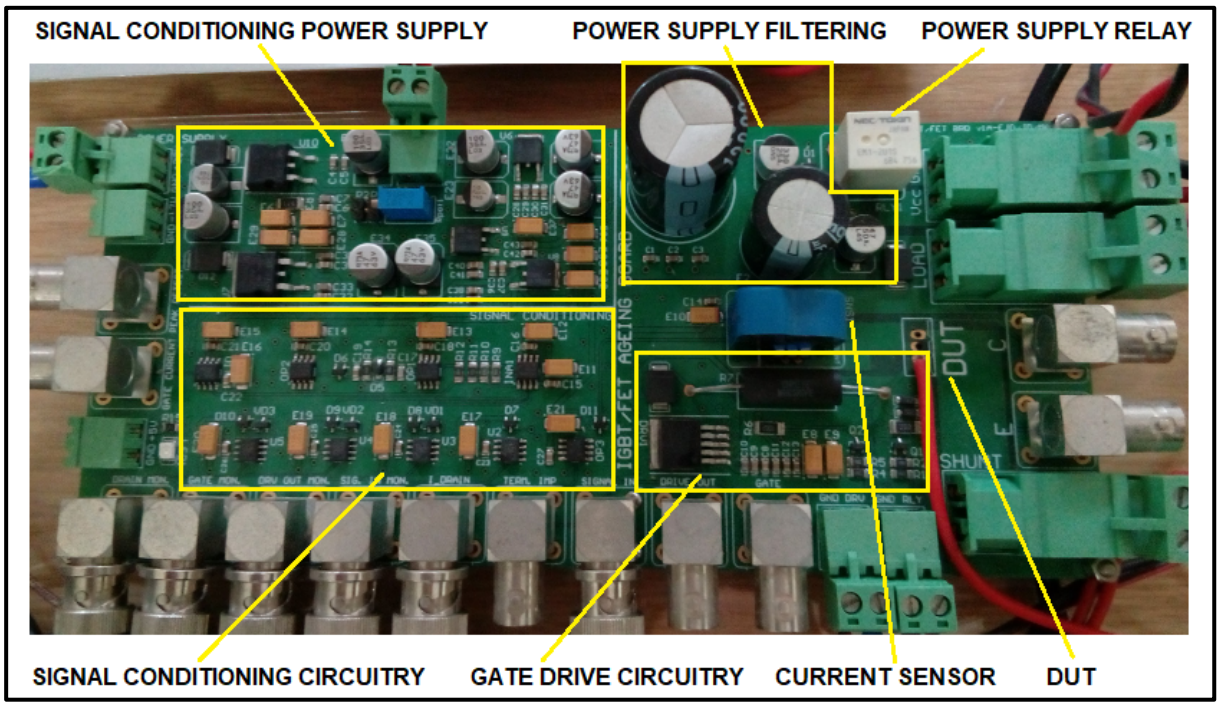


Figure 3.4 - IGBT DC PCAS Custom-Built Hardware PCB

voltage (V_C), (BNC2-BNC6) to provide a direct connection to the oscilloscope inputs to acquire the transient information, if required, during the ageing process. Furthermore, linear power regulation circuits were included to power the signal conditioning circuits, with the required power bus voltages. The circuit was implemented on a four-layer PCB with dedicated power bus, ground, analog signals, and power section layers. This PCB is shown in Figure 3.4.

3.3.3 IGBT DC PCAS Software

Software was developed within National Instruments (NI) Labview environment to control the IGBT ageing process and acquire, electrical and thermal parameters during ageing. The software is interfacing the PC with the function generator, to set the gate driver input signal function, frequency, amplitude, and DC offset. Moreover, this software is interfacing the PC with the NI-9211 thermocouple DAQ and the NI-USB-6341 multifunction DAQ. Finally, this software is interfacing the PC with the mixed domain oscilloscope (MDO4104-B), hence setting the instrument's vertical amplitude, scale and position, horizontal time, scale and position, sampling rate, and triggering mode. This enables the acquisition of a complete cycle of the gate voltage (V_G) and collector-emitter voltage (V_{CE}). The oscilloscope acquisition was triggered twice during each age iteration that is at the beginning of the age iteration at an IGBT's case temperature (T_C) of 25°C and when the IGBT's case temperature (T_C) reaches 150°C, which is the tested IGBT's maximum junction temperature (T_{J_MAX}). It is important to highlight the fact that the IGBT's junction temperature (T_J) will be somewhat higher than the maximum junction temperature (T_{J_MAX}) of 150°C, when the IGBT's case temperature (T_C) is at this temperature.

Apart from the acquisition and logging of the electrical and thermal parameters, the developed software is also responsible for the IGBT's autonomous ageing control. Within the developed Graphical User Interface (GUI) three parameters are to be specified by the user, which are the Thermal Runaway Temperature, Average Case Temperature Set Point, and the Case Temperature peak-to-peak fluctuation ($T_{C\_PK\text{-}PK}$) set around the Average Case Temperature Set Point (described within the GUI as the Hysteresis Band). The software was programmed to autonomously maintain the IGBT's average case temperature (T_{C_AVR}) to the value specified by the Average Case Temperature Set Point parameter within the specified Hysteresis Band. The developed software provides the flexibility of conducting accelerated ageing procedures with elevated average case temperature (T_{C_AVR}) and hence elevated average junction temperature (T_{J_AVR}), higher than the maximum junction temperature (T_{JMAX}), but with a

corresponding peak-to-peak case temperature ($T_{C\_PK\text{-}PK}$) fluctuation and hence peak-to-peak junction temperature ($T_{J\_PK\text{-}PK}$) fluctuation which is relatively small. This tends to trigger metallization and solder layers degradation. Moreover, the developed software provides the flexibility of conducting accelerated ageing procedures where the average case temperature (T_{C_AVR}) and hence the average junction temperature (T_{J_AVR}) is maintained at a value smaller than the maximum junction temperature (T_{JMAX}), but with large peak-to-peak case temperature ($T_{C\_PK\text{-}PK}$) fluctuation and hence large peak-to-peak junction temperature ($T_{J\_PK\text{-}PK}$) fluctuation. This tends to predominantly trigger bond-wire degradation. It is important to highlight the fact that throughout this study, IGBTs were aged according to the first described accelerated ageing procedure, with the intent of inflicting metallization and solder layers degradation.

Enabling the gate driver output, the DUT starts to dissipate power (predominantly due to on-state losses), causing it to directly heat up, since no external heat-sink is utilized. When the upper temperature value of the hysteresis band is reached the gate driver output is disabled, leaving the device to cool, until the lower temperature of the hysteresis band. At this point the gate driver output is enabled again. This procedure continues until the IGBT latches-up. At that point, it will be useless to disable the gate driver output because the IGBT would in any case remain conducting and therefore heating up. Therefore, whenever the IGBT goes into latch-up and hence thermal runaway, the IGBT's case temperature (T_C) will exceed the upper hysteresis limit, until it reaches the set Thermal Runaway temperature value. At this point the power relay will be energized to open, breaking the power supply path, hence preventing the IGBT from heating further leading to device's destruction. At this point the device is left to passively cool, hence ending the ageing procedure once the device reaches 25ºC. This procedure is repeated three times for each IGBT, for a full age procedure to be completed. In some cases, further age iterations were conducted, to examine severe IGBT ageing and degradation. Moreover, the software was provided with the functionality of manual overrides, overriding the autonomous procedure in case the accelerated ageing procedure goes out-of-control. The second version of this software included a stepped temperature accelerated ageing profile. This was conducted since when the IGBT was let to heat immediately to the Average Case Temperature Set Point, rather than taking a more gradual stepped approach, it was noticed that the above-described accelerated ageing procedure tended to go out-of-control, experiencing immediate device's destruction. This modification increased the rate of successful completion of the three age iterations. Figure 3.5 provides the DC PCAS software GUI, while Figure 3.6 provides the corresponding flowchart.

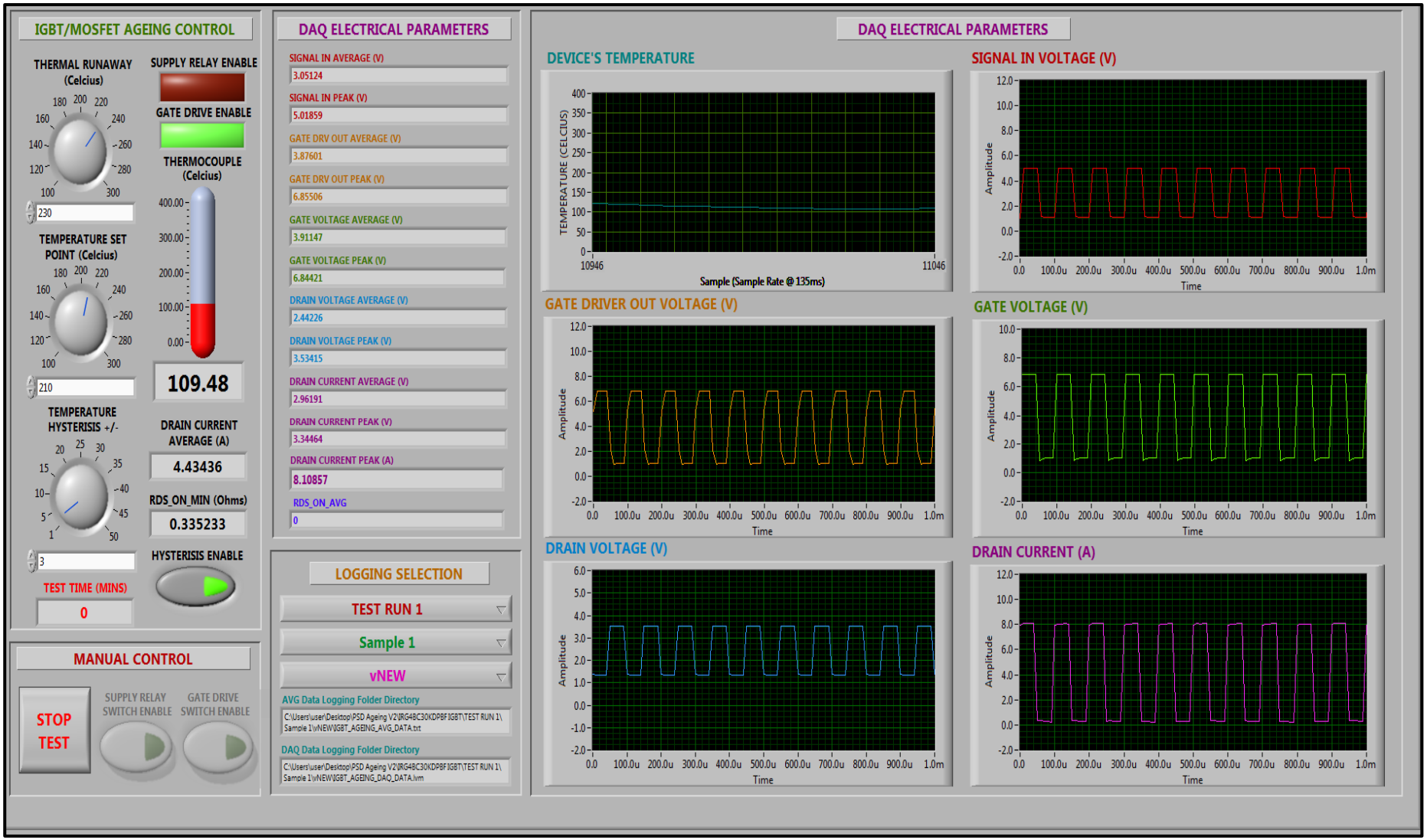


Figure 3.5 - Developed IGBT DC PCAS Software GUI

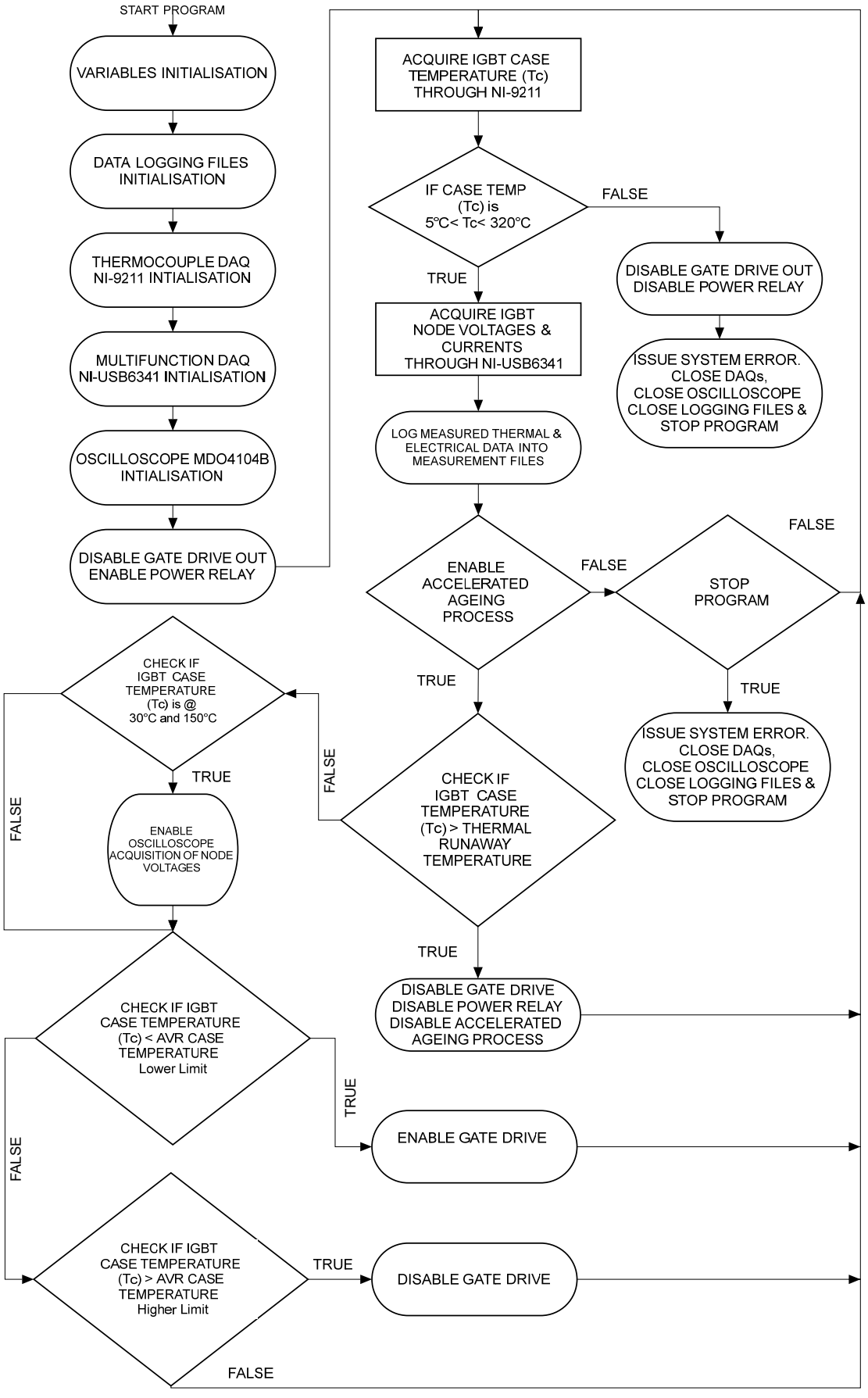


Figure 3.6 – Developed IGBT DC PCAS Software Flowchart

3.3.4 IGBT Accelerated Ageing Experimental Procedure

Figure 3.7 illustrates the PT IGBT cell structure utilized during this study, which is constructed similarly to a vertical diffused power MOSFET. The main difference is the inclusion of the P+ collector layer. This modification forms a vertical PNP BJT. The additional P+ region will form, the cascaded connection of the surface power MOSFET and the underlying BJT. This P+ region forms a PN junction with the N- drift region. Conduction modulation occurs by injecting minority carriers in the drift region. This leads to a larger current density than the power MOSFET, while the forward voltage drop is reduced. Once the IGBT is switched off, the excess carriers in the N- drift region decay by electron-hole recombination, which causes a gradual collector current decay.

The four-layer NPNP structure of the IGBT forms a parasitic thyristor structure. Turn-on of this thyristor is undesirable, as it will lead to the loss of gate control. Ideally, once minority carriers are injected into the drift region, they should flow to the emitter region directly. The electrons' charge in the formed MOSFET n-channel, attracts most holes. This attraction causes a lateral "holes current" through the p-type region. This current, flowing through the p-type region, develops a corresponding voltage drop across the p-type region spreading resistance. If this voltage drop is large enough, it can forward bias the base-emitter junction of the parasitic NPN transistor. This will trigger the parasitic thyristor structure hence latching up the IGBT.

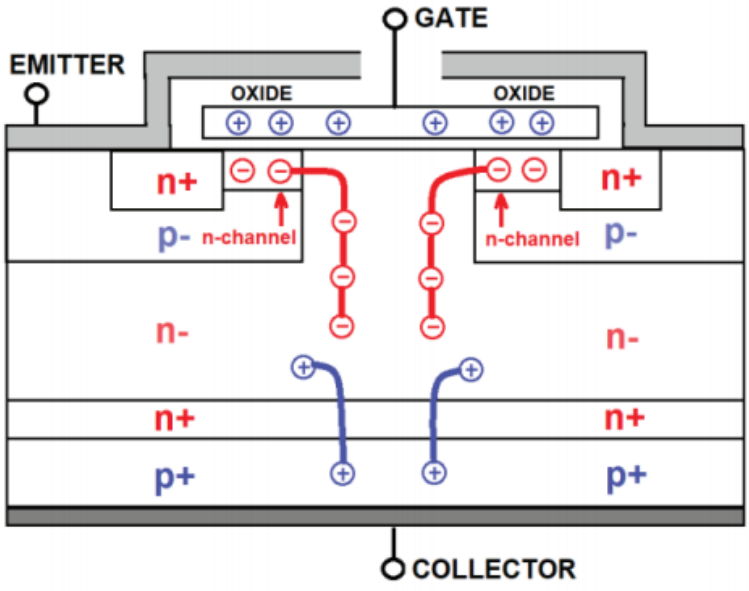


Figure 3.7 – Utilized PT IGBTs' Cell Structure

Accelerated ageing was conducted on the International Rectifier IRG4BC30KDPBF 600V 16A IGBT [209]. It is an International Rectifier generation 4 IGBT with a co-packaged HEXFRED^{TM} ultrafast soft recovery diode. The corresponding IGBT package utilized for this study was the TO-220 package. This IGBT was utilized since it has been employed extensively in research conducted by the NASA's Ames Research Centre, Intelligent Systems Division, in relation to IGBT prognostics techniques and health management systems evidencing their findings in various literature [131-136]. Hence results obtained, could be compared with the results obtained by these studies, hence validating the employed ageing procedure.

As discussed in section 3.3.2 the IGBT ageing test circuit was set in a common-emitter configuration. The corresponding output stage supply voltage ($+V_{LOAD\_OUT}$) was set to 7V DC. This reflects the characteristic of the DC PCAS that is of not employing a large output DC Link voltage. Two series 0.25Ω 1% 25W resistors were utilized as load. The gate input signal was set to a 10kHz square wave with a 50% duty cycle and a corresponding 12V peak-to-peak amplitude. With the above electrical conditions, and with a typical collector-emitter on-state voltage (V_{CE_ON}) in the range of 2.4V [209], the IGBT experiences a corresponding mean collector current (I_{C_MEAN}) of 4.6A and peak collector current (I_{C_PEAK}) of 9.2A. No heat-sink was attached with the IGBT, such that the on-state losses cause the IGBT to self-heat until latch-up occurs. It is important to highlight that the IGBT latch-up triggered through this accelerated ageing procedure is of the static type. The IGBT's temperature was obtained through the utilization of a type-K thermocouple. Different IGBT's locations were considered to attach the thermocouple. The intrinsic TO-220 heat sink was initially considered, essentially obtaining the IGBT's case temperature (T_C). This method required electrical isolation as the heat-sink itself presented a short to the thermocouple metals. Since this measurement was so crucial to the accelerated ageing procedure, it was desired that the IGBT's temperature measurement is as intimate as possible to the die's junction temperature. Hence it was decided to drill a 1.1mm hole in the IGBT's package epoxy on the front side. The depth of the hole was conducted and guided through X-Ray inspection, such that it is enough to surpass the IGBT's package epoxy and the thermocouple is just above the IGBT's die but without touching it and hence affecting critical parts of the IGBT. After some experimentation, a jig was built to penetrate the different IGBT samples with the same depth and at the same position. Through this method the thermocouple had a tight fit within the drilled hole (width of the thermocouple is 1mm). This is illustrated in Figure 3.8.

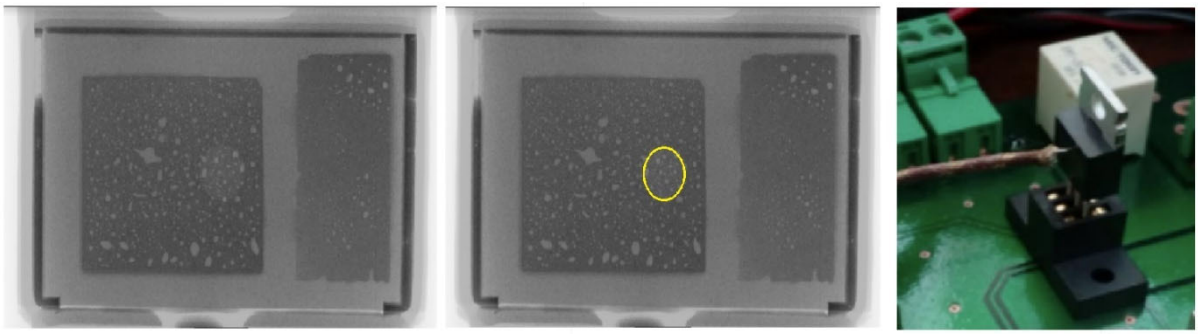


Figure 3.8 – (a) X-Ray Image of New IGBT including drilled hole shade (b) X-Ray Image of New IGBT with evidenced drilled hole (c) Thermocouple attachment with IGBT.

As discussed earlier the implemented accelerated ageing procedure involved heating up the IGBT through self-heating, until a specified elevated average case temperature (T_{C_AV}) is reached, at which point the IGBT case temperature (T_C) is left to oscillate within a small peak-to-peak case temperature ($T_{C\_PK\text{-}PK}$) fluctuation and hence relating to a peak-to-peak junction temperature ($T_{J\_PK\text{-}PK}$) fluctuation. In the initial conducted accelerated ageing tests, the average case temperature (T_{C_AV}) about which the case temperature (T_C) had to be maintained oscillating, was set to 160˚C, that is just above the maximum junction temperature of 150˚C. With this setting, tests took hours without triggering IGBTs' latch-up, proving a very slow ageing procedure which could not be qualified as an accelerated procedure. Eventually the average case temperature (T_{C_AV}) set point was raised in the range of 230˚C, with an oscillation band of +/-3˚C and a thermal runaway setting at which point the power within the IGBT was suspended, was set 20˚C higher than the specified average case temperature (T_{C_AV}). These settings for the tested IGBT proved to trigger latch-ups within a reasonable amount of time. One must mention that the set +/-3˚C case temperature (T_C) oscillation, translated to an oscillation of +/-6 ˚C. Two accelerated ageing approaches were undertaken. The first approach was to immediately self-heat the IGBT from room temperature up till the specified elevated average case temperature (T_{C_AV}). Even though this procedure was implemented, and successfully managed to age the IGBTs in this manner, it produced ageing inconsistency and reliability issues. Multiple scenarios were encountered where once the IGBT's case temperature (T_C) reaches the specified average case temperature (T_{C_AV}), the IGBT immediately goes into latch-up, triggering immediately thermal runaway, hence allowing no time during which the IGBT's case temperature (T_C) is left in controlled fluctuation ($T_{C\_PK\text{-}PK}$) phase. This is considered an essential phase of the implemented ageing procedure. Moreover, this ageing strategy sometimes triggered immediate IGBT failure. The corresponding IGBT's

case temperature (T_C), gate voltage (V_G) and average collector current (I_C) for this kind of accelerated ageing procedure is shown in Figure 3.10, evidencing at the end of the procedure, the loss of gate control, abrupt increase in collector current (I_C) and consequently the corresponding rise in the IGBT's case temperature (T_C).

A second accelerated ageing approach was implemented, where the IGBT case temperature (T_C) was raised till the specified average case temperature (T_{C_AV}) through intermediary case temperature (T_C) stages. During each stage, the IGBT's case temperature (T_C) is nominally left in controlled case temperature fluctuation ($T_{C\_PK\text{-}PK}$) mode, for 10 minutes. If during this time the monitored average current goes beyond 4.9A, then this time is extended to 20 minutes as there was a greater probability that the IGBT will encounter latch-up at this average case temperature (T_{C_AV}). If during this time the IGBT did not encounter latch-up, the IGBT's case temperature was let to increase by 10°C, to the next intermediary average case temperature (T_{C_AV}) stage and again left in controlled case temperature fluctuation ($T_{C\_PK\text{-}PK}$) mode for 10 minutes. This procedure continues until the IGBT's average case temperature was at 230°C, at which point the intermediary average case temperature (T_{C_AV}) will be only allowed to increase by 5°C instead of 10°C. This implemented accelerated ageing procedure, is shown in Figure 3.10. This technique ensured more accelerated ageing consistency and a higher success rate for the different IGBT samples to go through the pre-established three age iterations (ageing iteration is the accelerated ageing test procedure which will trigger an IGBT's latch-up at which point power is interrupted from the IGBT and left to cool down to room temperature (25°C)). Each device was subjected to at least three accelerated ageing iterations. An increase in the collector current (I_C) was noticed throughout the progression of each age iteration. This is mainly due to the negative linear temperature coefficient of the IGBTs' collector-emitter on-state voltage (V_{CE_ON}) for collector current (I_C) of less than 10A as evidenced in Figure 5 of the IGBT's datasheet [209]. Since IGBTs are minority carrier devices, they suffer from "residual current" or "tail-current" during turn-off, namely since the recombination process requires a substantial amount of time. It was noticed that during the ageing procedure this "residual current" increases in magnitude and time, before decaying completely. This phenomenon will be described in more detail in Chapter 4. Hence, there will come a point where this "residual current" is large enough indicating the on-set of IGBT's latch-up. This is indicated through the observation of the minimum current of the average collector current (I_C) plot, of both Figure 3.10 and Figure 3.11, indicating a corresponding increase. At this point, latch-up is triggered, leading to a sudden increase in the IGBT's collector current (I_C), potentially increasing up to

the continuous conditions, leading to an abrupt increase in the IGBT's case temperature (T_C), which if uncontrolled leads to thermal runaway and device's destruction. To determine the changes in the static electrical parameters with ageing a test campaign of twenty-one IRG4BC30KDPBF IGBTs was conducted, taken from three different manufacturing batches. Only 13 IGBTs survived the full accelerated ageing procedure (three age iterations) and remained operational. It is important to point out that the accelerated ageing methodology utilized in this test campaign for which results will be presented, involved the second described strategy. Tables 3-2, 3-3 and 3-4 describe; the overall time to failure of each age iteration (OTTF), the corresponding average IGBTs' case temperature ($T_{C\_AV\_FAIL}$) at which latch-up was encountered, the corresponding final time to failure (FTTF), and the final cycles to failure (FCTF), at the failing average IGBT's case temperature ($T_{C\_AV\_FAIL}$). A cycle refers to a complete IGBT's case temperature oscillation about the average case temperature (T_{C_AV}). Figure 3.9 illustrates the significance of the above parameters. From these tables one can notice that there was a general increase in the mean of all the different parameters, over the three age iterations (Age Iteration A to Age Iteration C). One can observe an increase in the mean OTTF, with 60.92 minutes for Age Iteration A, 73.32 minutes for Age Iteration B and 80.64 minutes for Age Iteration C. The mean failing average case temperature ($T_{C\_AV\_FAIL}$) increased too, with 227.69°C for Age Iteration A, 235.38°C for Age Iteration B and 237.92°C for Age Iteration C. Even the mean FTTF and FCF experienced a corresponding increase with 668.92s and 16 cycles for Age Iteration A, 676.62s and 16.92 cycles for Age Iteration B, and 785.23s and 18.23 cycles for Age Iteration C. The standard deviations for all the above parameters are also presented for each age iteration.

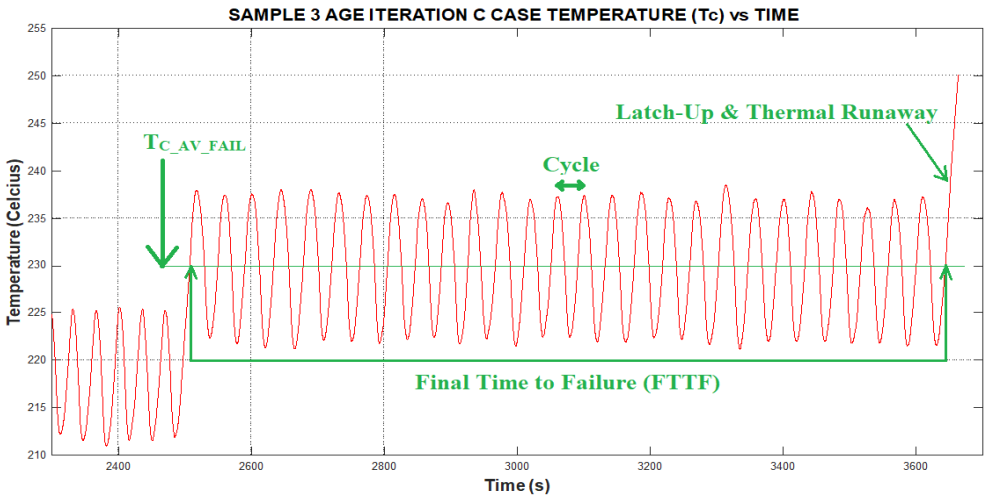


Figure 3.9 – IGBT Case Temperature (T_C) Plot, highlighting relevant failing parameters.

AGE ITERATION A						
IGBT SAMPLE	IGBT BATCH	Overall Time To Failure (OTTF) (mins)	Average Case Temperature at Fail ($T_{C\_AV\_FAIL}$) (°C)	Final Cycles To Failure (FCTF)	Final Time To Failure (s)	Mean Cycle Time @ Failure (MCTF)
IGBT 1	BATCH 1	62.12	240	15	669	44.60
IGBT 2	BATCH 2	53.71	230	21	804	38.29
IGBT 3	BATCH 1	58.97	210	19	700	36.84
IGBT 4	BATCH 3	52.83	230	13	517	39.77
IGBT 5	BATCH 2	51.73	220	24	933	38.88
IGBT 6	BATCH 2	58.86	210	15	781	52.07
IGBT 7	BATCH 1	65.48	230	18	737	40.94
IGBT 8	BATCH 3	80.82	245	9	477	53.00
IGBT 9	BATCH 1	74.47	235	15	641	42.73
IGBT 10	BATCH 3	61.13	230	12	488	40.67
IGBT 11	BATCH 3	63.32	230	13	520	40.00
IGBT 12	BATCH 2	47.34	220	17	715	42.06
IGBT 13	BATCH 1	61.22	230	17	714	42.00
MEAN		**60.92**	**227.69**	**16.00**	**668.92**	**42.78**
STANDARD DEVIATION (δ)		**9.14**	**10.33**	**3.98**	**137.21**	**5.59**

Table 3-2 – IGBTs' Age Iteration A Failure Parameters.

AGE ITERATION B						
IGBT SAMPLE	IGBT BATCH	Overall Time To Failure (OTTF) (mins)	Average Case Temperature at Fail ($T_{C\_AV\_FAIL}$) (°C)	Final Cycles To Failure (FCTF)	Final Time To Failure (s)	Mean Cycle Time @ Failure (MCTF)
IGBT 1	BATCH 1	61	240	15	645	43.00
IGBT 2	BATCH 2	53.15	230	18	654	36.33
IGBT 3	BATCH 1	62.37	235	12	634	52.83
IGBT 4	BATCH 3	82.28	235	15	643	42.87
IGBT 5	BATCH 2	82.95	235	11	526	47.82
IGBT 6	BATCH 2	93.25	240	19	690	36.32
IGBT 7	BATCH 1	73.1	235	15	554	36.93
IGBT 8	BATCH 3	76	240	8	441	55.13
IGBT 9	BATCH 1	89.45	240	23	810	35.22
IGBT 10	BATCH 3	51.15	220	15	600	40.00
IGBT 11	BATCH 3	83.45	235	22	778	35.36
IGBT 12	BATCH 2	61.5	235	24	947	39.46
IGBT 13	BATCH 1	83.47	240	23	874	38.00
MEAN		**73.32**	**235.38**	**16.92**	**676.62**	**41.48**
STANDARD DEVIATION (δ)		**14.00**	**5.58**	**5.07**	**142.56**	**6.64**

Table 3-3 - IGBTs' Age Iteration B Failure Parameters.

AGE ITERATION C						
IGBT SAMPLE	IGBT BATCH	Overall Time To Failure (OTTF) (mins)	Average Case Temperature at Fail ($T_{C\_AV\_FAIL}$) (°C)	Final Cycles To Failure (FCTF)	Final Time To Failure (s)	Mean Cycle Time @ Failure (MCTF) (s)
IGBT 1	BATCH 1	70.65	235	10	463	46.30
IGBT 2	BATCH 2	61.28	230	15	672	44.80
IGBT 3	BATCH 1	60.72	230	27	1136	42.07
IGBT 4	BATCH 3	88.75	240	19	694	36.53
IGBT 5	BATCH 2	92.32	238	13	612	47.08
IGBT 6	BATCH 2	91.87	245	12	594	49.50
IGBT 7	BATCH 1	72.53	230	13	658	50.62
IGBT 8	BATCH 3	90.12	240	30	1424	47.47
IGBT 9	BATCH 1	110.57	245	16	720	45.00
IGBT 10	BATCH 3	81.08	235	11	576	52.36
IGBT 11	BATCH 3	83.45	240	22	810	36.82
IGBT 12	BATCH 2	61.5	240	26	975	37.50
IGBT 13	BATCH 1	83.47	245	23	874	38.00
MEAN		**80.64**	**237.92**	**18.23**	**785.23**	**44.16**
STANDARD DEVIATION (δ)		**14.81**	**5.57**	**6.72**	**263.21**	**5.49**

Table 3-4 - IGBTs' Age Iteration C Failure Parameters.

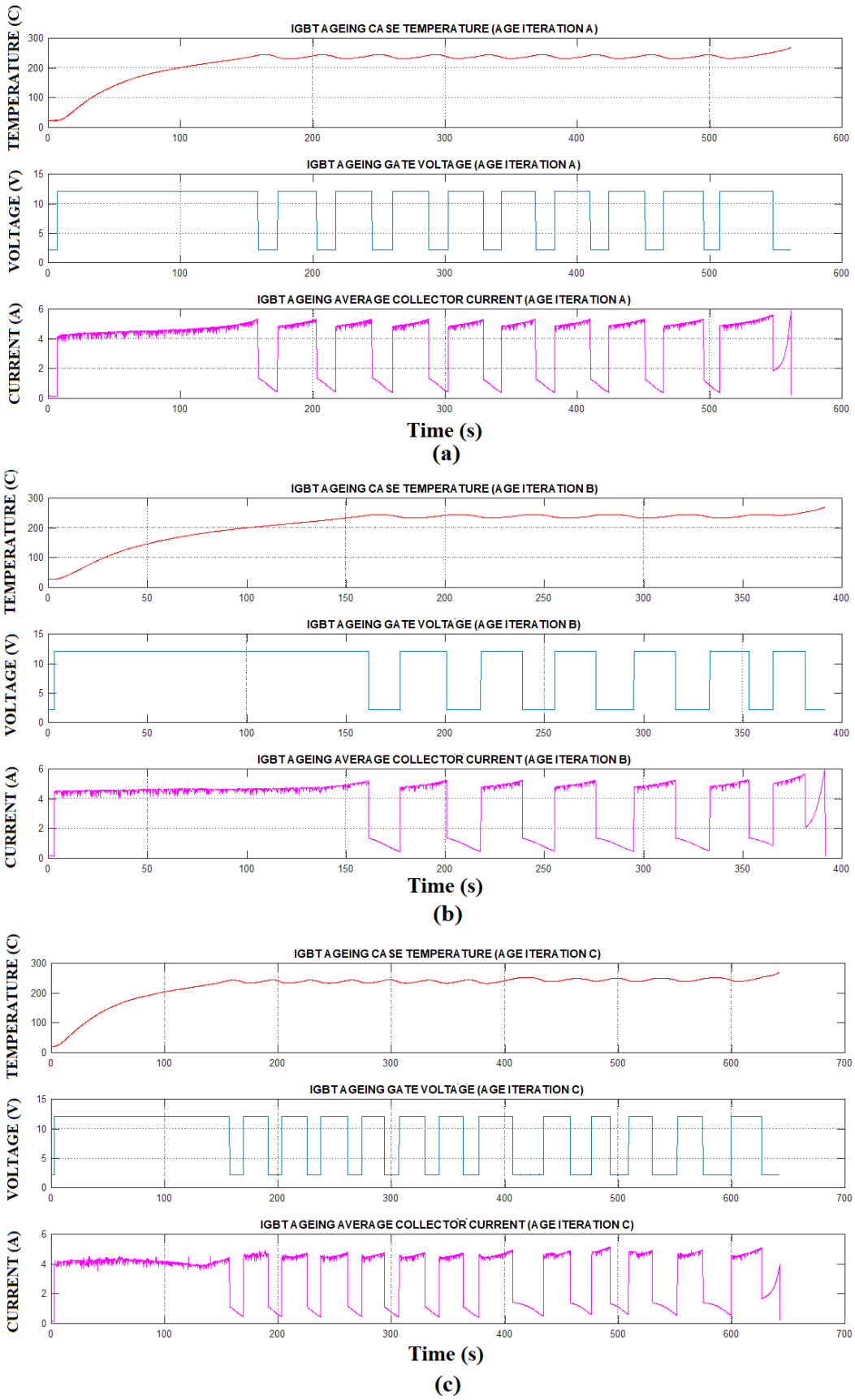


Figure 3.10 – IGBT Sample 9 DC PCAS Case Temperature (T_C), Gate Voltage (V_G) & Collector Current (I_C) (a) Age Iteration A (b) Age Iteration B (c) Age Iteration C

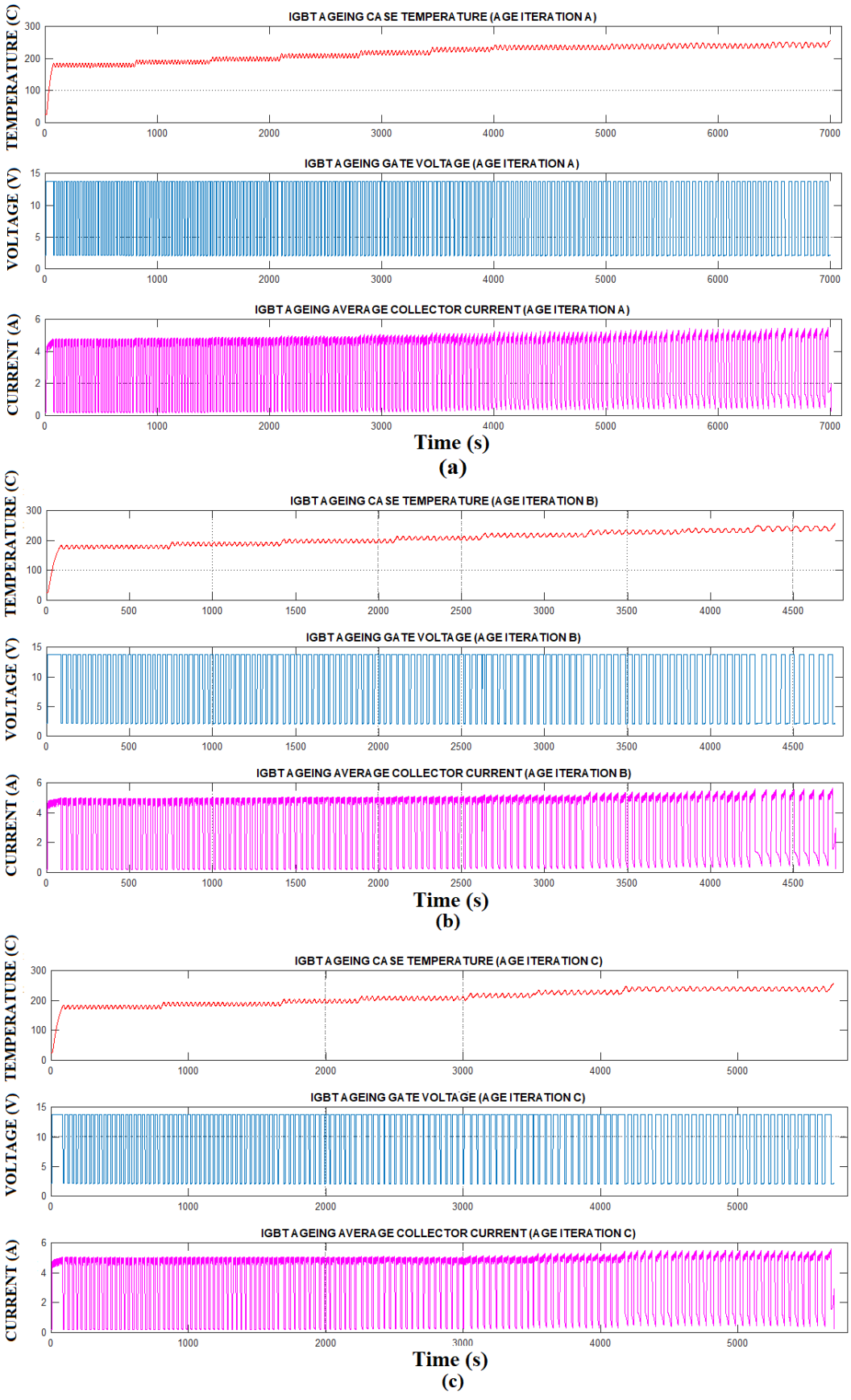


Figure 3.11 - IGBT Sample 8 DC PCAS Case Temperature (T_C), Gate Voltage (V_G) & Collector Current (I_C) (a) Age Iteration A (b) Age Iteration B (c) Age Iteration C

3.3.5 IGBT Ageing Mechanical (X-Ray) Characterization

X-Ray analysis was conducted to determine the effects produced by the implemented accelerated ageing strategy on the IGBT mechanical package. This was undertaken through the utilization of the NORDSON DAGE Jade X-Ray machine. Figure 3.12 (a) illustrates the X-Ray image of a new IRG4BC30KDPBF IGBT highlighting the "co-pack" package, with an integrated free-wheeling diode on the right (small area) and IGBT structure on the left (large area). These two areas characterize the die-attach of both devices. Silicon (Si) is invisible to X-Rays and hence reflections are produced by the die-attach layer. The die-attach layer has two main purposes: mechanical adhesion of the die to the substrate and dissipation of heat generated in the die [141]. In power devices heat densities are high, so conventional die-attach adhesives are not suitable. In this case high-melting solder alloys are used. Hence the solder alloy must cover as much as possible the surface between the lead-frame and the die, with a minimal void presence. Typically, for high power applications, the maximum void rate permitted is 10% [141]. As illustrated in Figure 3.12(a), the dark areas within the two structures indicate good die-attach adhesion, while the bright areas indicate voids. It is evident that even when the IGBT is new, there is a certain degree of voiding both in the IGBT die-attach and the internal diode die-attach. Tables 3-5 and 3-6 show the die-attach evolution with the implemented accelerated ageing procedure, evidencing an increased void presence in both die-attaches, as illustrated further in Figure 3.12(b).

An opensource software IMAGEJ was utilized to extract the degree of voiding in both die-attaches. This was conducted by isolating from the different new and aged X-Ray images, each respective die-attach area. Each extracted image was subjected to contrast enhancement, to evidence better the lightly grayed areas over the darker areas, hence pronouncing the voids further. Eventually an image processing thresholding technique was applied, translating the extracted images into binary black and white images. The black area represents the healthy die-attach while the white areas represent the die-attach voids.

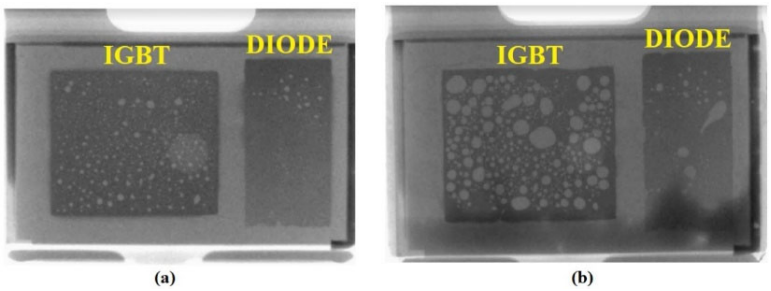


Figure 3.12 – X-Ray Image of the IGBT & Internal Diode Die-Attaches (a) New (b) Aged.

AGE PHASE	DIE-ATTACH PERCENTAGE VOIDING			
	IGBT		INTERNAL DIODE	
	MEAN VOID (%)	σ (%)	MEAN VOID (%)	σ (%)
NEW	3.638	2.566	1.292	0.258
AGE ITER A	27.175	7.157	12.823	5.435
AGE ITER B	32.804	7.916	14.724	6.450
AGE ITER C	37.587	5.309	16.878	7.863

Table 3-5 – Mean Percentage Voiding and corresponding Standard Deviation for all 13 IGBTs

Through the count of the white pixels over the black pixels, the percentage die-attach voiding could be computed. The resultant threshold images for the IGBT and the internal diode are illustrated in Tables 3-7 & 3-8 and Table 3-9 respectively. It is important to highlight, that obtained X-Ray images contained noise sources, namely minimal contrast in the original X-Ray image, X-Ray shadows created by melted solder and the thermocouple drilled hole. This might have introduced errors during the computation of the percentage voiding. For this purpose, each extracted image was individually processed to keep errors due to these noise artefacts to a minimum. All aged IGBTs experienced an increase in the corresponding die-attach voiding and melting, even though there were variations. Figure 3.13 provides the individual percentage voiding for each sample for both the IGBT and internal diode die-attaches. Table 3-5 provides the mean percentage voiding and corresponding standard deviation (σ) for all 13 samples. One can notice that the first age iteration, produced the largest void degradation with a mean void degradation of 27.18% and 12.82% for the IGBT die and internal diode die, respectively. Moreover, one can notice that the mean percentage voiding degradation of the IGBT die-attach was more severe than that of the internal diode with a mean final percentage voiding of 37.59% for the IGBT die-attach and 16.88% for the internal diode die-attach. This is a characteristic of the DC PCAS ageing strategy which utilizes a small DC voltage link and not utilizing an inductive load, hence not involving the internal free-wheeling diode during accelerated ageing commutation. Hence the internal diode's inflicted degradation was through a secondary effect, that is, through the heat generated within the package by the IGBT. The fact that the die-attaches are experiencing voiding, it will have an impact on the ability to dissipate the heat from the devices' junction to the environment. This means that for the same electrical conditions, the devices will experience an increase in the junction temperature (T_J). This will affect the IGBT's electrical and switching parameters which are temperature dependent as will be described later.

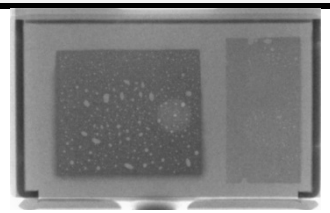
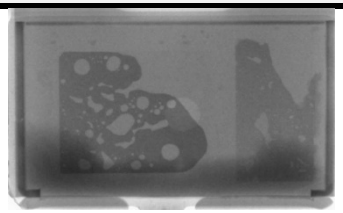
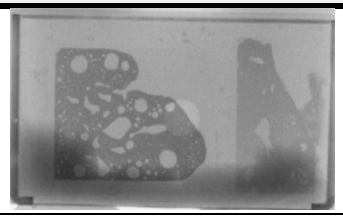
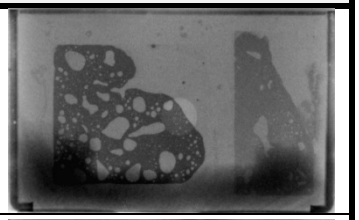
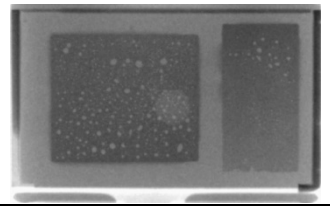
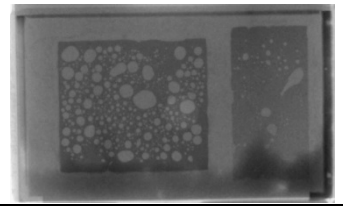
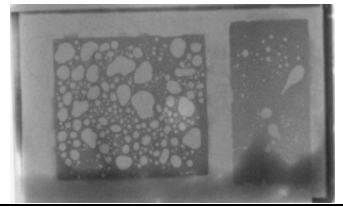
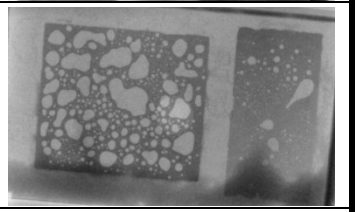
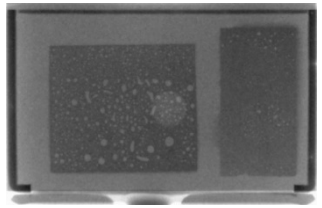
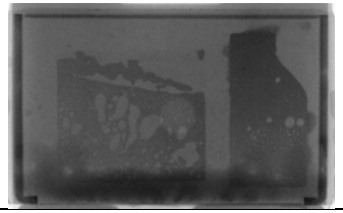
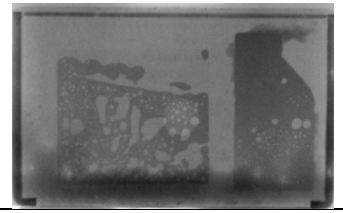
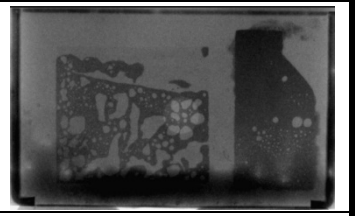
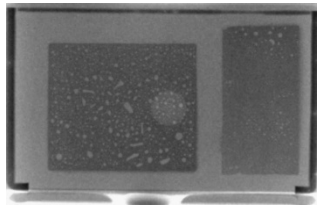
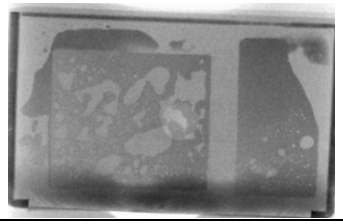
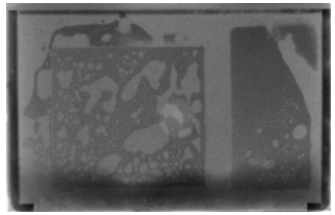
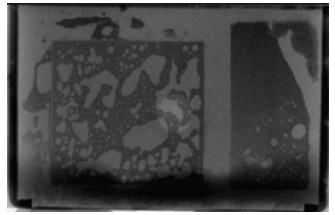
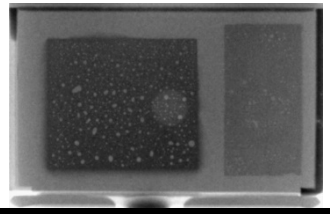
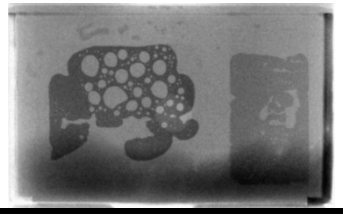
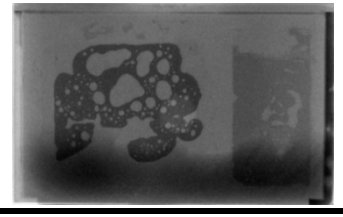
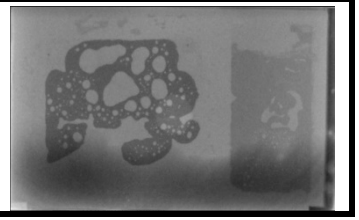
IGBT SAMPLE	NEW	AGE ITERATION A	AGE ITERATION B	AGE ITERATION C
IGBT 1				
IGBT 2				
IGBT 3				
IGBT 4				
IGBT 5				

Table 3-6 – X-Ray Imagery of IGBT & Internal Diode Die-Attach Degradation with Ageing (IGBT 1-5, New to Age Iteration C)

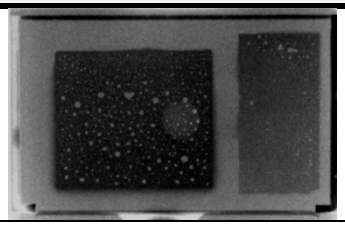
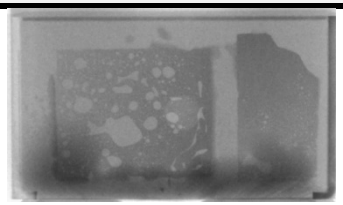
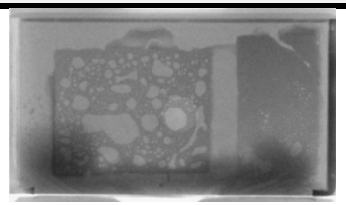
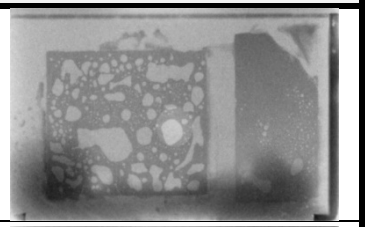
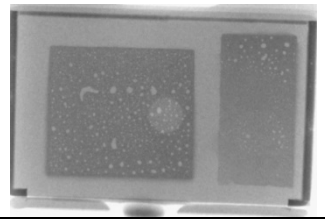
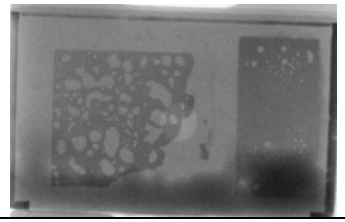
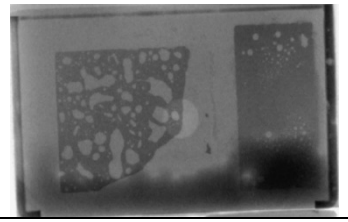
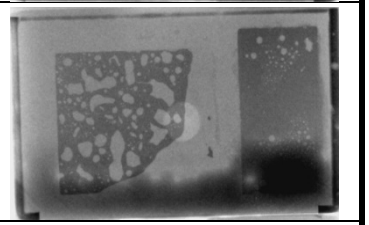
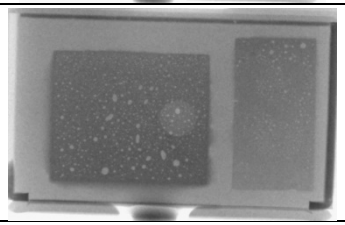
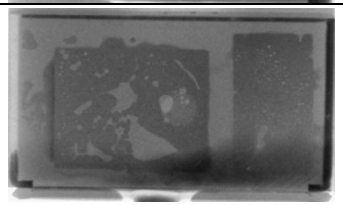
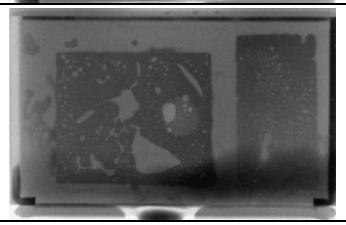
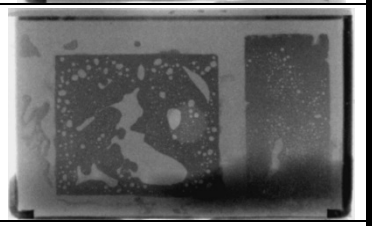
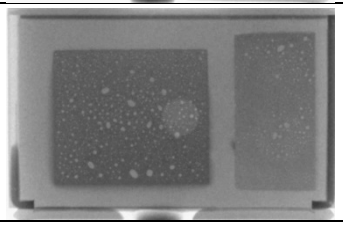
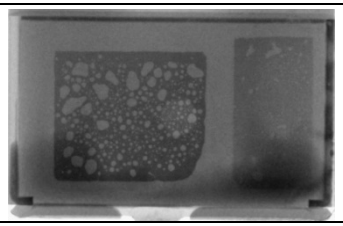
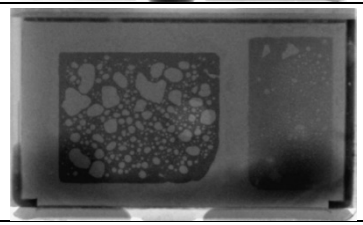
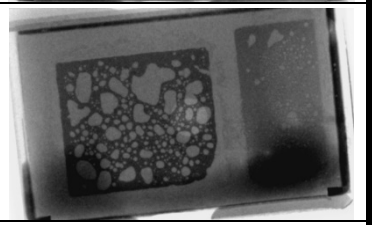
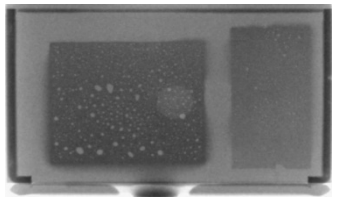
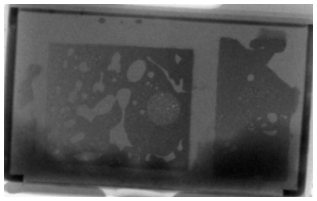
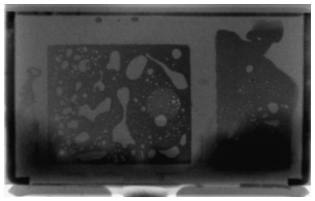
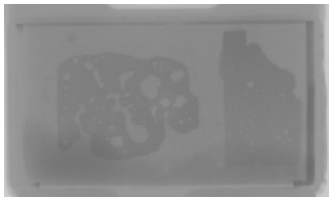
IGBT SAMPLE	NEW	AGE ITERATION A	AGE ITERATION B	AGE ITERATION C
IGBT 6				
IGBT 7				
IGBT 8				
IGBT 9				
IGBT 10				

Table 3-7 - X-Ray Imagery of IGBT & Internal Diode Die-Attach Degradation with Ageing (IGBT 6-10, New to Age Iteration C)

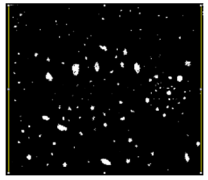
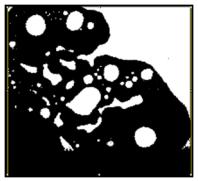
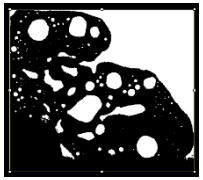
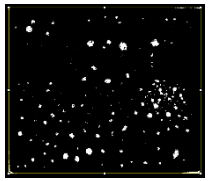
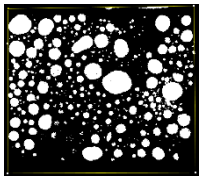
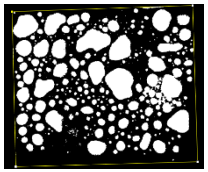
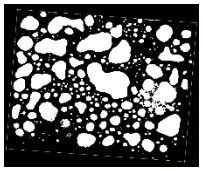
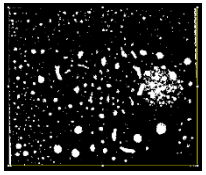
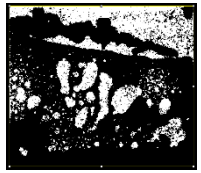
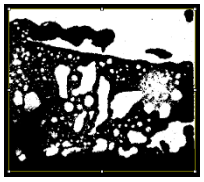
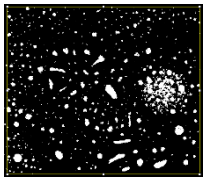
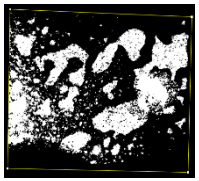
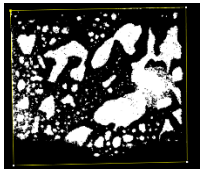
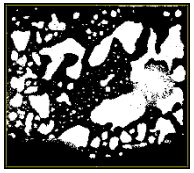
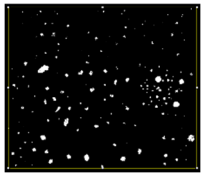
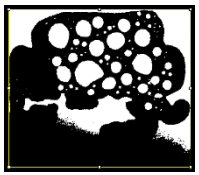
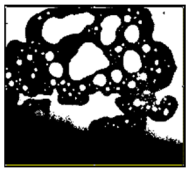
IGBT SAMPLE	NEW	AGE ITERATION A	AGE ITERATION B	AGE ITERATION C
IGBT 1				
IGBT 2				
IGBT 3				
IGBT 4				
IGBT 5				

Table 3-8 - X-Ray Imagery of IGBT Die-Attach Threshold Image with Ageing (IGBT 1-5, New to Age Iteration C)

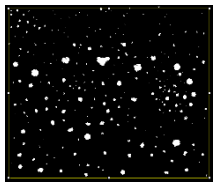
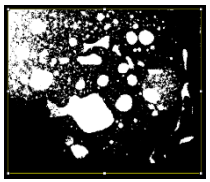
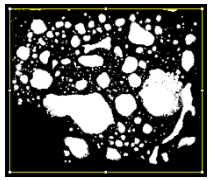
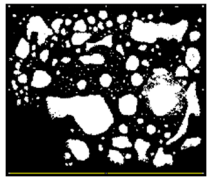
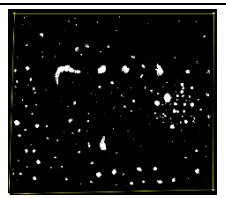
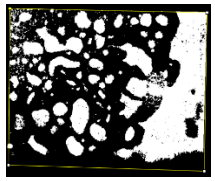
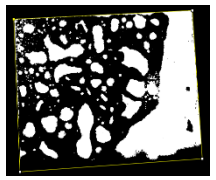
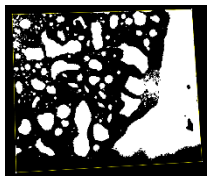
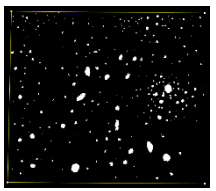
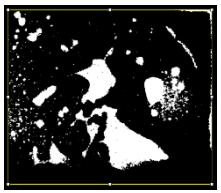
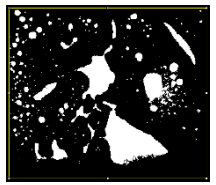
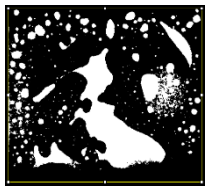
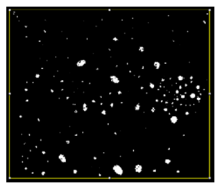
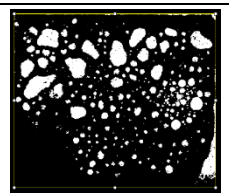
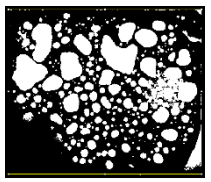
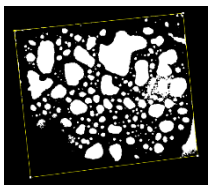
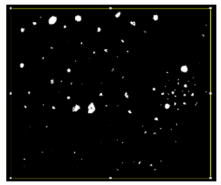
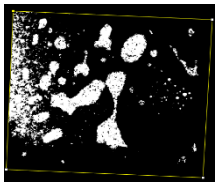
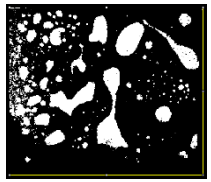
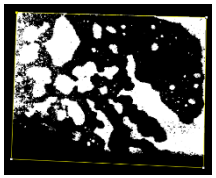
IGBT SAMPLE	NEW	AGE ITERATION A	AGE ITERATION B	AGE ITERATION C
IGBT 6				
IGBT 7				
IGBT 8				
IGBT 9				
IGBT 10				

Table 3-9 - X-Ray Imagery of IGBT Die-Attach Threshold Image with Ageing (IGBT 6-10, New to Age Iteration C)

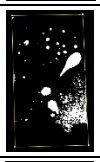
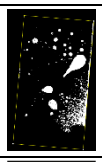
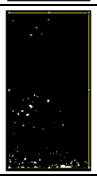
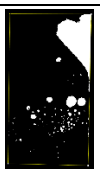
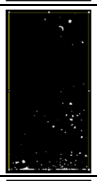
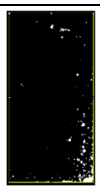
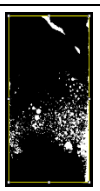
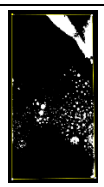
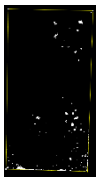
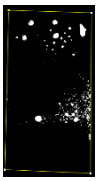
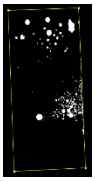
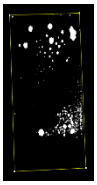
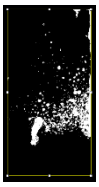
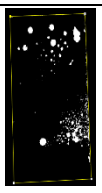
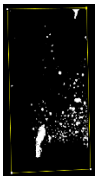
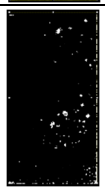
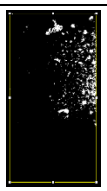
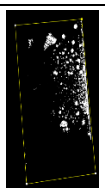
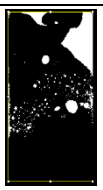
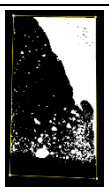
IGBT SAMPLE	NEW	AGE ITR A	AGE ITR B	AGE ITR C
IGBT 1				
IGBT 2				
IGBT 3				
IGBT 4				
IGBT 5				
IGBT 6				
IGBT 7				
IGBT 8				
IGBT 9				
IGBT 10				

Table 3-10 - X-Ray Diode Die-Attach Threshold Image (IGBT 1-10, New to Age Iteration C)

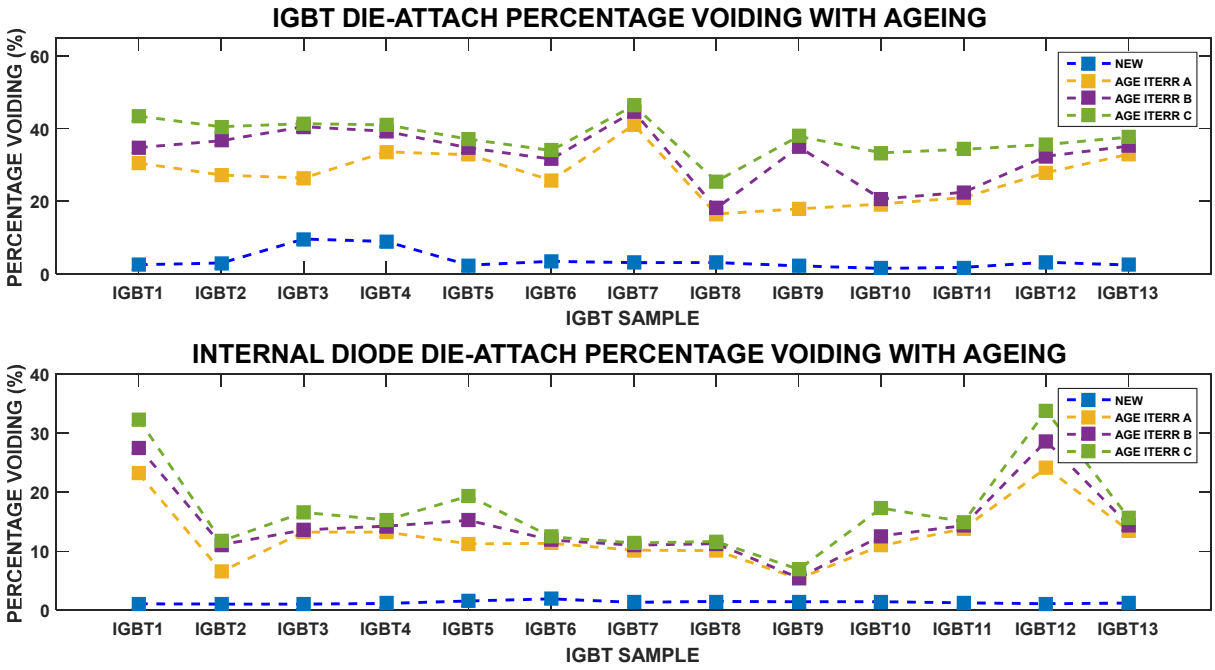


Figure 3.13 – IGBT & Internal Diode Die-Attaches' Voiding Evolution with Ageing

3.4 IGBT's Static Electrical Parameters Characterization Setup

Further to the electrical and thermal characterization parameters acquired and logged during ageing, other commercial hardware was utilized, and custom-built software was developed to measure the IGBT's electrical parameters and hence the corresponding ageing effects. Two source meter units (SMU) were utilized, the Keithley 2400 and the Keithley 2461. The Keithley 2400 is a four-quadrant source meter which can source voltage from 5µV to 210V; measure voltage from 1µV to 211V; can source current from 50pA to 1.05A and measure current from 10pA to 1.055A with maximum source power of 22W. The Keithley 2461 is a four-quadrant power source meter with a pulsed capability of 10A 100V and with voltage and current measurement resolution of 5µV and 50pA, respectively. The SMUs Keithley 2400 and Keithley 2461, were interfaced with the PC via RS232 and USB respectively, to configure and acquire measurement data. Furthermore, a thermoelectric cooler (Peltier Element) in conjunction with a thermoelectric controller (which was implemented within another SMU Keithley 2400) were utilized, to control and set the IGBT's case temperature (T_C) to 25˚C. This ensured that the electrical characterization measurements were isolated from ambient temperature changes. An electrical characterization test configuration circuit board was developed specifically to automate the shorting of the different IGBT pins during the different characterization tests and was controlled via NIUSB6341 DAQ.

3.4.1 IGBT Threshold Voltage & Leakage Current Characterization Hardware & Software Setup

The threshold voltage (V_{THRES}) is the minimum gate-to-emitter voltage (V_{GE}) required to create a conducting path between the collector and the emitter terminals. The threshold voltage (V_{THRES}) measurement was conducted by shorting the gate to the collector, while a gate-to-emitter voltage (V_{GE}) was applied, and the collector current (I_C) was simultaneously measured. As the gate to emitter voltage (V_{GE}) was increased, the threshold voltage was defined as the gate to emitter voltage (V_{GE}) at which the collector current (I_C) is at 250μA. The hardware was setup as illustrated in Figure 3.14(a), utilizing a single source meter unit (SMU 2400), forcing the gate-to-emitter voltage (V_{GE}) while sensing and measuring the collector current (I_C). Moreover, the IGBT case temperature (T_C) was maintained at 25˚C to isolate the measurement from ambient temperature (T_A) changes.

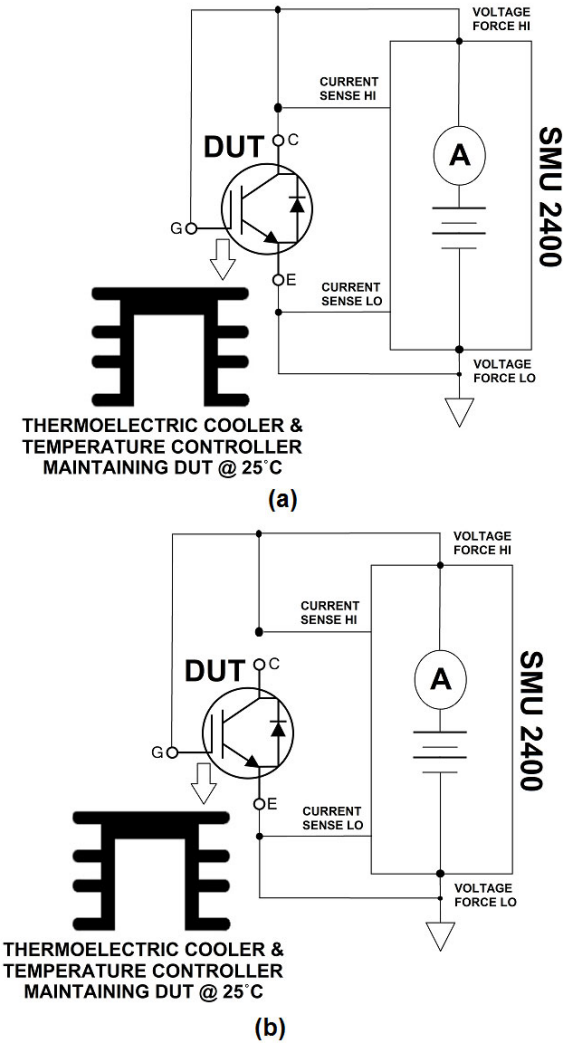


Figure 3.14 – IGBT (a) Threshold Voltage (V_{THRES}) (b) Leakage Current, Characterization Setup

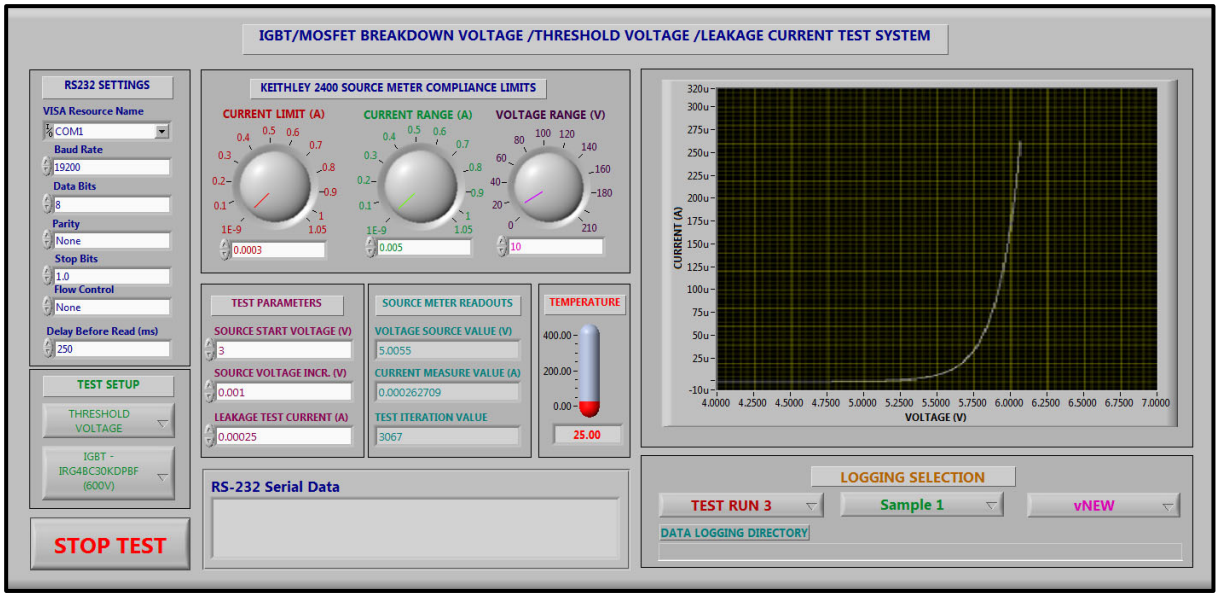


Figure 3.15 - IGBT Threshold Voltage and Leakage Current Measurement Software GUI

Figure 3.14(b) illustrates the hardware setup configuration for the gate-emitter leakage current (I_{GE_LEAK}) measurements. The leakage current (I_{GE_LEAK}) was determined by isolating the collector terminal and applying a gate to emitter voltage (V_{GE}) of 20V DC. The corresponding measured gate-to-emitter current (I_{GE}) is the leakage current. The measurement hardware, utilized a single source meter unit (SMU 2400), forcing the gate-to-emitter voltage (V_{GE}) to the above voltage, while sensing and measuring the gate-emitter current (I_{GE_LEAK}). Moreover, the IGBT case temperature was maintained at 25˚C to isolate this measurement from ambient temperature (T_A) changes.

Customized software was developed to autonomously conduct these measurements. Figure 3.15 illustrates the GUI of the developed software, which was developed within National Instruments (NI) Labview. This software was developed to be able, to conduct Breakdown Voltage measurement test, Threshold Voltage measurement test and Leakage Current measurement test. The Breakdown Voltage measurement configuration, even though implemented, was not employed for the IGBTs characterization, as none of the available SMUs had the output voltage capability to exceed the 600V breakdown voltage of the characterized IRG4BC30KDPBF IGBTs. This software, remotely configures and acquires data from the Keithley SMU2400 according to the different tests. For the threshold voltage test the SMU2400 output voltage is initialized at 3V DC and incremented by 1mV, until the measured current reaches 250µA. For the leakage current test, the output voltage is set to 20V DC while measuring the corresponding output current. This is conducted ten times and the mean leakage current is computed. Figure 3.16 provides the flowchart corresponding to this software.

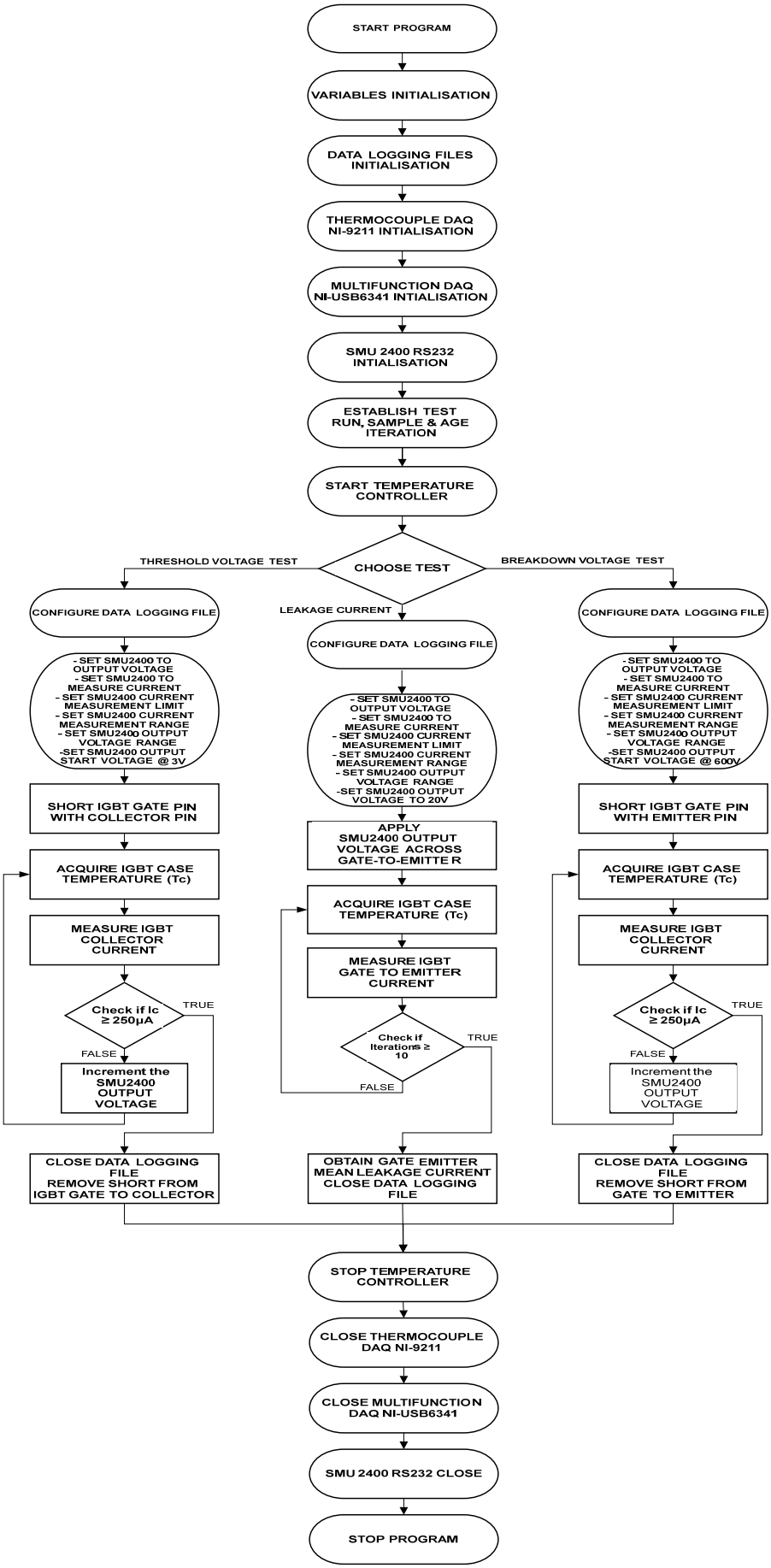


Figure 3.16 - IGBT Threshold Voltage and Leakage Current Measurement Software Flowchart

3.4.2 IGBT On-State Voltage (V_{CE_ON}), On-State Resistance and Output Characteristics Characterization Setup

When the IGBT is on, the collector-emitter voltage (V_{CE}) changes in accordance with the collector current (I_C), gate voltage (V_G) and the junction temperature (T_J). The collector-emitter on-state voltage (V_{CE_ON}) or collector-emitter saturation voltage (V_{CE_SAT}), represents the collector-emitter voltage (V_{CE}) when the IGBT is in hard saturation, and is important, as it directly impacts the power dissipation during the on-state. The smaller the collector-emitter on-state voltage (V_{CE_ON}) the smaller the on-state power dissipation.

Hence the IGBT should have the smallest collector-emitter on-state voltage (V_{CE_ON}) possible. As discussed in Section 2.9.1, the measurement of the collector-emitter on-state voltage (V_{CE_ON}) can provide direct information on the IGBT's junction temperature (T_J), due to its direct dependency on this latter parameter. Since it has been already established that the implemented accelerated ageing procedure was degrading the IGBT's internal die-attach, hence hindering the thermal path from the junction to the ambient, the collector-emitter on-state voltage was determined during the accelerated ageing procedure, at different IGBT's case temperature (T_C). This was conducted during the initial accelerated ageing procedure case temperature (T_C) ramp-up, with measurements focusing on the first 150°C, since this corresponds to the device's maximum junction temperature (T_{J_MAX}). Hence by conducting different measurements of the collector-emitter on-state voltage (V_{CE_ON}) at different case temperature (T_C), the collector-emitter on state voltage temperature coefficient ($\Delta V_{CE\_ON}/\Delta T_C$) was obtained for the different age iterations, for the different IGBT samples. The obtained results will be presented and discussed in Section 3.5.

Due to the dependence of the collector-emitter on-state voltage (V_{CE_ON}) on junction temperature (T_J) and collector current (I_C), it was of interest to characterize the changes in this parameter due to the ageing only. This was conducted by isolating the collector-emitter on-state voltage (V_{CE_ON}) measurements from any changes by retaining the aforementioned parameters as constant as possible. Hence the collector-emitter on-state voltage (V_{CE_ON}) and the corresponding on-state resistance (R_{CE_ON}) were characterized by pulsating a calibrated current pulse through the collector, while keeping the IGBT case temperature (T_C) constant at room temperature (25°C), measuring the corresponding IGBT's collector-emitter voltage (V_{CE}).

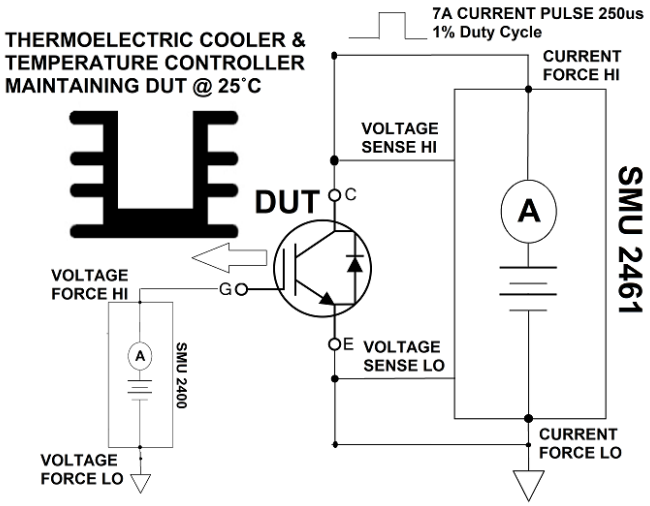


Figure 3.17 – IGBT Collector-Emitter On-State Voltage (V_{CE_ON}) characterization setup.

This measurement was implemented by setting the power source meter unit, Keithley SMU2461 to source a current pulse of amplitude 7A (SMU's maximum), pulse duration of 250μs and 1% duty cycle, through the IGBT's collector while measuring the corresponding collector-emitter voltage (V_{CE}) pulse. Simultaneously SMU2400 was set to provide the gate-to-emitter voltage, which was set to output a voltage of 15V DC, to ensure that the IGBT is in hard saturation. Even though the on-state resistance is not a standard term associated with IGBTs but rather with power MOSFETs, the corresponding IGBT's effective on-state resistance was computed by dividing the measured collector-emitter voltage (V_{CE}) during the flat section of the pulse with the corresponding flat section of the issued calibrated 7A current pulse. A current pulse with a small pulse duration and duty cycle was utilized to ensure further that the IGBT did not self-heat during this measurement. Furthermore, high current testing would produce voltage drops along the leads, hence Four Wire/Kelvin measurement technique was utilized to ensure a more precise measurement. The utilized characterization setup is illustrated in Figure 3.17.

Customized software was developed to autonomously conduct these measurements. Figure 3.20 illustrates the GUI of the developed software, which was developed within National Instruments (NI) Labview. This software, remotely configures and controls the temperature controller, while acquiring the IGBT's case temperature (T_C) through the NI-9211 DAQ, as well as configuring the SMU2400, to output the required IGBT's gate DC voltage. Moreover, this software, remotely configures the power source meter unit SMU2461 to issue the required collector current (I_C) pulse, while measuring and acquiring the corresponding collector-emitter voltage (V_{CE}) pulse. Figure 3.18 provides the flowchart corresponding to this software.

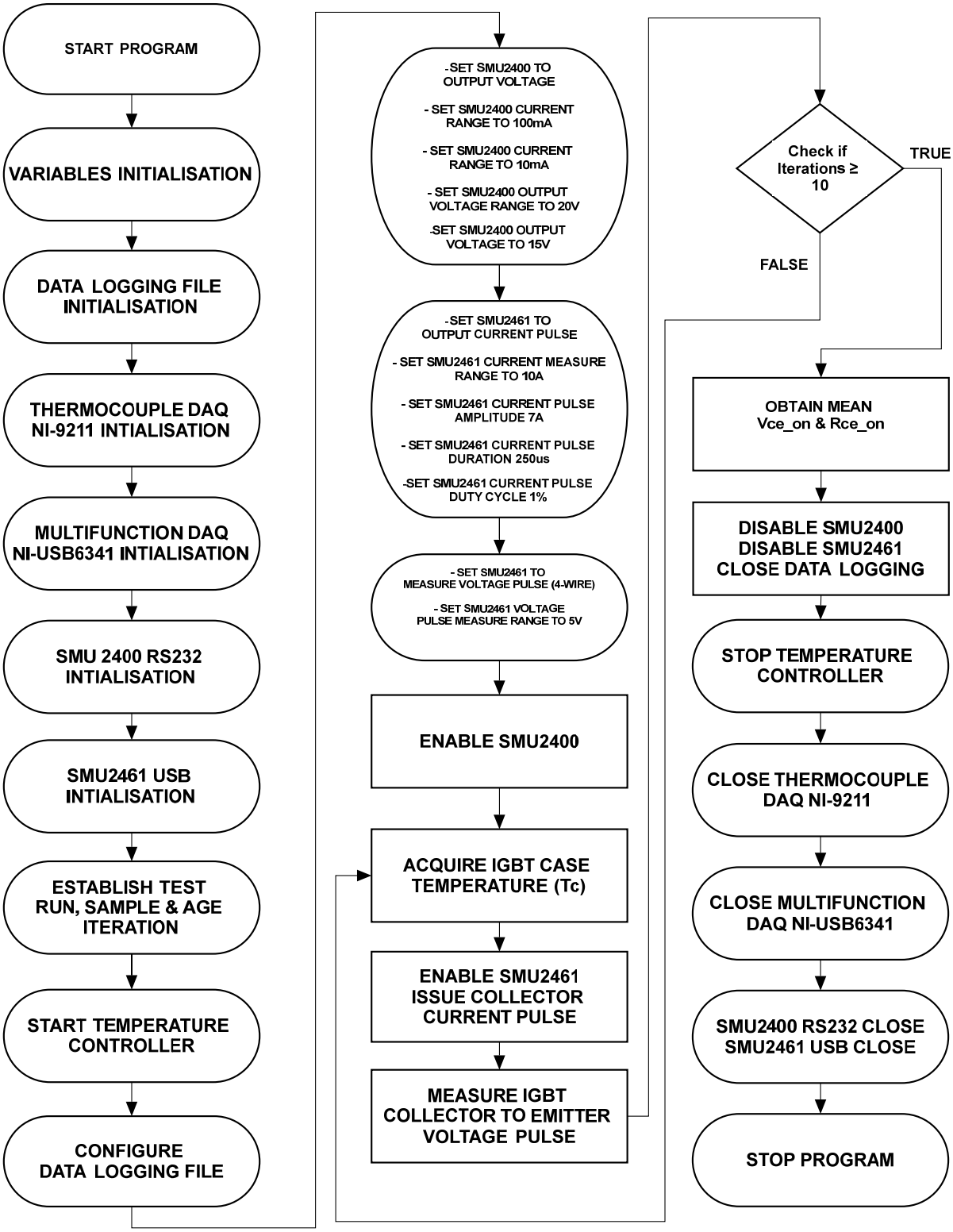


Figure 3.18 – IGBT ON-State Voltage and ON-State Resistance Measurement Software Flowchart

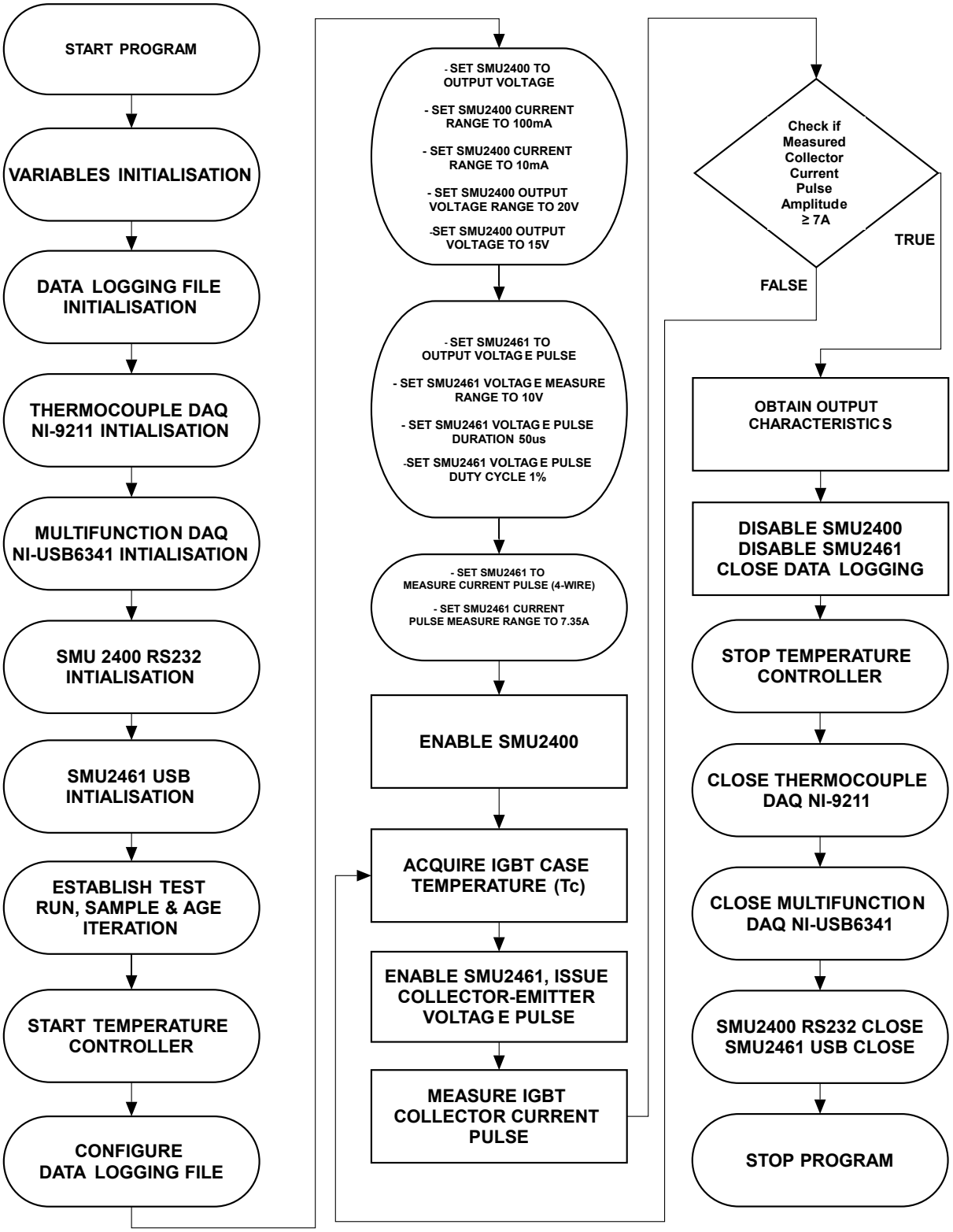


Figure 3.19 - IGBT Output Characteristics Measurement Software Flowchart

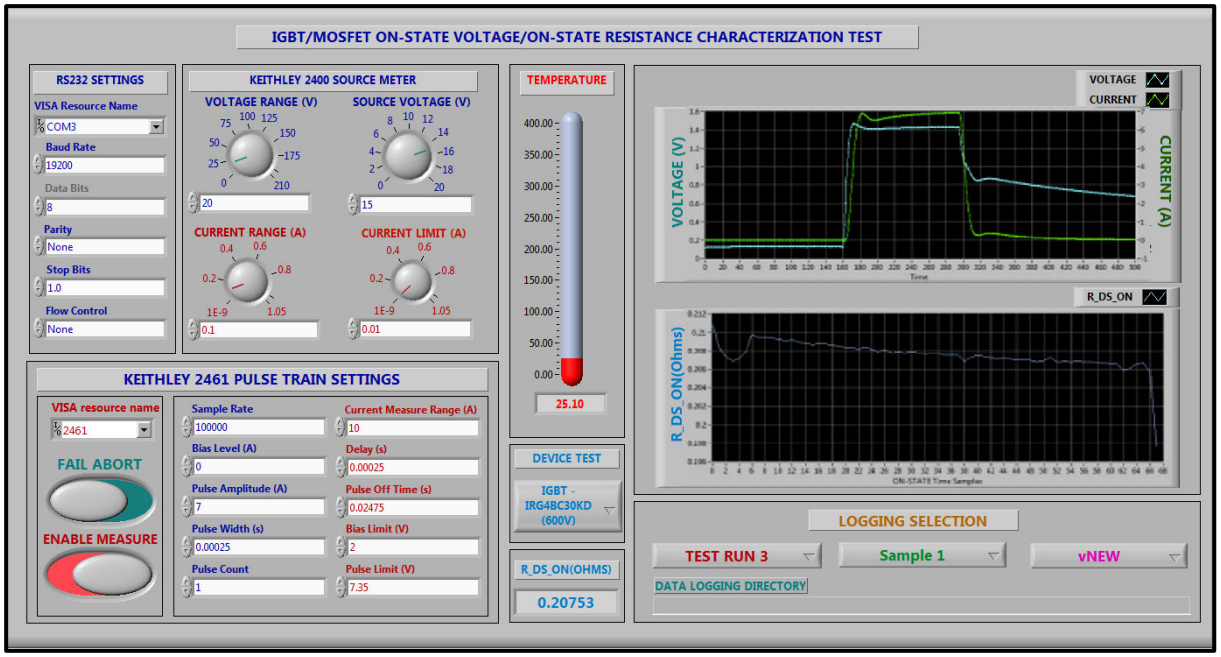


Figure 3.20 - IGBT Collector-Emitter On-State Voltage (V_{CE_ON}) Measurement Software GUI

The output characteristics provides the relationship between the collector-emitter voltage (V_{CE}) and the collector current (I_C) at a constant gate-to-emitter voltage (V_{GE}) and constant junction temperature (T_J), nominally at 25ºC since these characteristics are dependent on the junction temperature (T_J). To further evidence and substantiate changes due to the implemented accelerated ageing procedure in the output stage of the IGBT, the output characteristics were measured. These were obtained by setting the power source meter SMU2461 to generate voltage pulses across the collector and emitter, with duration of 50µs and duty cycle of 1% and measuring the corresponding collector current (I_C) pulse. The collector-emitter voltage (V_{CE}) pulses were configured to start at an amplitude of 1V and increased until the measured collector current pulse reaches 7A (which is the maximum current pulse amplitude that can be provided by the SMU2461). During this procedure, the gate to emitter voltage (V_{GE}) was set to a constant voltage of 15V DC by the SMU2400. Once again voltage pulses with low pulse duration and duty cycle were utilized to ensure further that the IGBT did not self-heat during the measurement, while the temperature controller was again employed to maintain the IGBT's case temperature (T_C) at room temperature (25°C). Moreover, Four Wire / Kelvin measurement technique was again utilized to ensure characterization measurement precision. The utilized characterization setup is illustrated in Figure 3.21. The software developed for the collector-emitter on-state voltage (V_{CE_ON}) measurement, was modified to accommodate this measurement. It retained the functionality of remotely configuring and controlling the

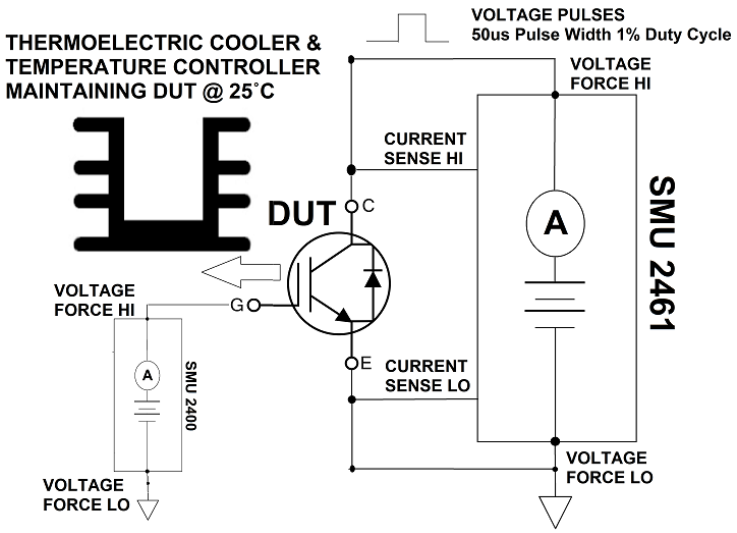


Figure 3.21 - IGBT Output Characteristics characterization setup

temperature controller, while acquiring the IGBT's case temperature (T_C) through the NI-9211 DAQ, as well as configuring the SMU2400, to output the required IGBT's gate DC voltage. On the other side this software, was modified to iteratively configure the power source meter unit SMU2461 to issue the required collector-emitter voltage (V_{CE}) pulses at different amplitudes, while measuring and acquiring the corresponding collector current (I_C) pulses. Figure 3.19 provides the flowchart of the output characteristics software.

3.4.3 IGBT Transfer Characteristics and Forward Transconductance Characterization Setup

The transfer characteristics relates the output collector current (I_C) of the IGBT to the input gate-emitter voltage (V_{GE}). Hence this relationship shows how the output collector current (I_C) increases with the gate-emitter voltage (V_{GE}), with a collector-emitter voltage (V_{CE}) that ensures the IGBT away from full enhancement, hence ensuring independence of this relationship to the latter parameter. The slope of the linear part of this relationship is the forward transconductance (g_{fe}) of the IGBT. Figure 3.22 illustrates the transfer characteristics and forward transconductance (g_{fe}) characterization setup. The measurement was conducted by setting the power source meter SMU2461 to pulsate a voltage pulse across the collector and emitter, of constant amplitude 15V, pulse duration of 50µs and 1% duty cycle, while concurrently measuring the corresponding collector current (I_C) pulse. For each collector-emitter voltage (V_{CE}) pulse, the gate-emitter voltage (V_{GE}) is varied through the SMU2400, until the measured collector current pulse, reaches 7A (which is the maximum current pulse amplitude that can be provided by the SMU2461). Once again voltage pulses with low pulse duration and duty cycle were utilized to ensure that the IGBT did not self-heat during the

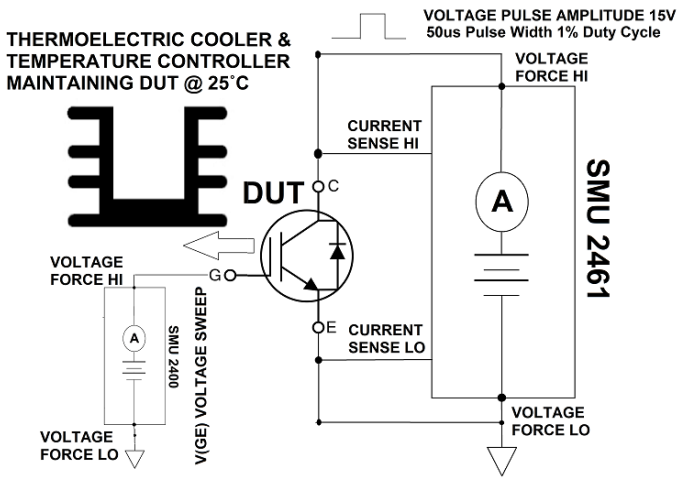


Figure 3.22 - Transfer Characteristics and Forward Transconductance (g_{fe}) characterization setup

measurement, while maintaining the IGBT's case temperature (T_C) at room temperature (25°C). Moreover, Four Wire / Kelvin measurement was employed to ensure measurement precision. Figure 3.23 illustrates the GUI of the software developed for this measurement. This software, remotely configures and controls the temperature controller, while acquiring the IGBT's case temperature (T_C) through the NI-9211 DAQ, as well as configuring the SMU2400, to iteratively vary the required IGBT's gate DC voltage while simultaneously configuring the power source meter unit SMU2461 to issue the required collector-emitter voltage (V_{CE}) pulse, while measuring and acquiring the corresponding collector current (I_C) pulse.

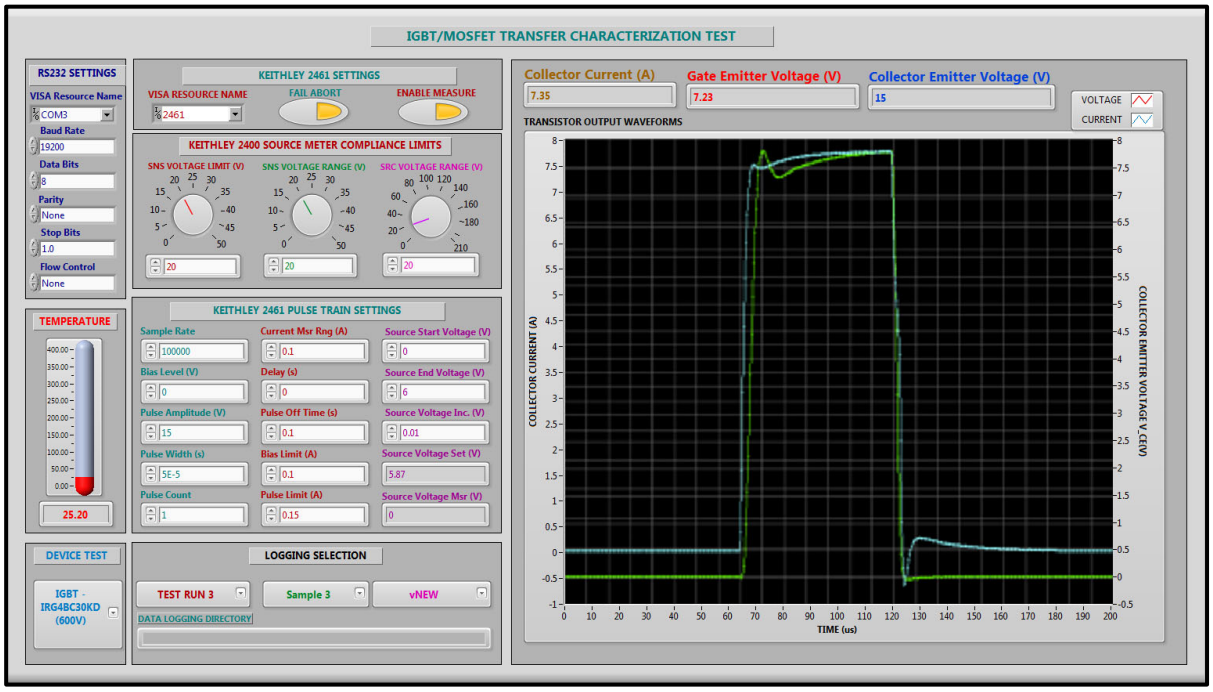


Figure 3.23 – Transfer Characteristics and Forward Transconductance (g_{fe}) Software GUI

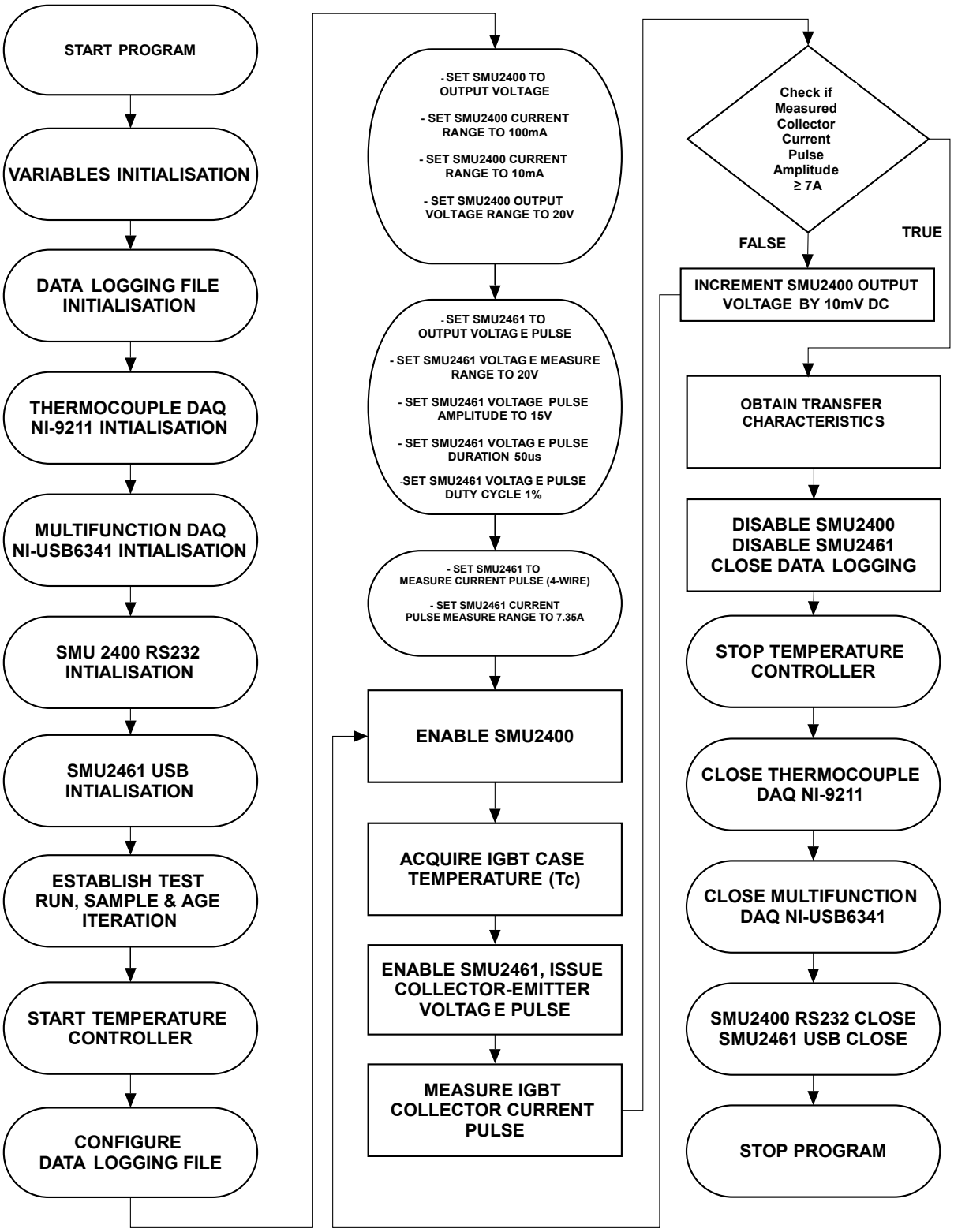


Figure 3.24 - Transfer Characteristics and Forward Transconductance (g_{fe}) Software Flowchart

3.4.4 IGBT Internal Diode Forward Voltage Drop (V_{FM}) Characterization Setup

This test was developed to characterize the forward voltage drop (V_{FM}) of the internal IGBT free-wheeling diode. The forward voltage drop across a diode's PN-junction is predominantly dependent on the diode's junction temperature (T_{JD}) and the forward conduction current (I_{FD}). This measurement was conducted by shorting the IGBT's gate and emitter and setting the power source meter SMU2461 to pulsate current pulses of pulse width 250µs and 1% duty cycle, through the emitter. The corresponding emitter-to-collector $V_{(EC)}$ voltage was measured, which effectively corresponds to the internal diode forward voltage drop (V_{FM}). The emitter current pulse amplitude was varied between 1A and 7A.

This measurement technique provided the Forward Voltage Drop (V_{FD}) vs the Instantaneous Forward Current (I_{FD}). Due to the dependencies of this parameter on the parameters highlighted earlier, calibrated current pulses with low pulse duration and duty cycle were utilized to ensure that the IGBT was not subjected to self-heating during measurement. This was enforced further by maintaining the IGBT's case temperature (T_C) at room temperature (25°C). Moreover, Four Wire / Kelvin measurement technique was again utilized to ensure measurement precision. The utilized characterization setup is illustrated in the Figure 3.25. Again, dedicated software was developed within National Instrument (NI) Labview to autonomously conduct this measurement. This software, remotely configures and controls the temperature controller, while acquiring the IGBT's case temperature (T_C) through the NI-9211 DAQ, configuring the power source meter unit SMU2461 to issue the required forward current (I_{FM}) pulses, while measuring and acquiring the corresponding forward voltage (V_{FM}) pulses. The flow chart for this software is illustrated in Figure 3.26.

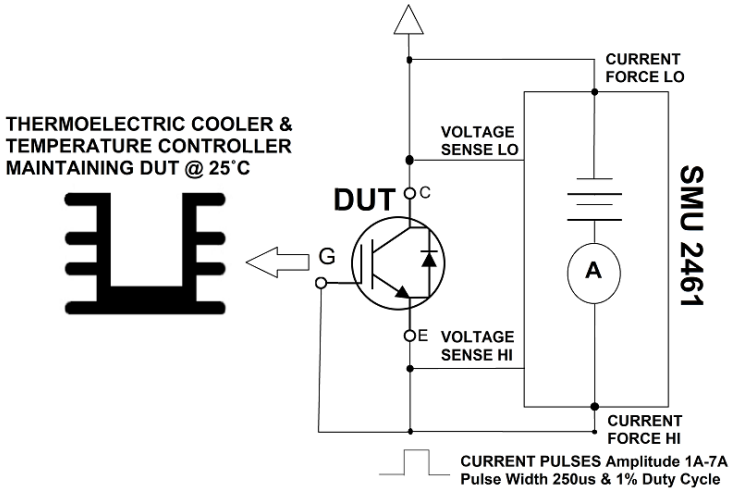


Figure 3.25 – Internal IGBT Diode's Forward Voltage (V_{FD}) characterization setup.

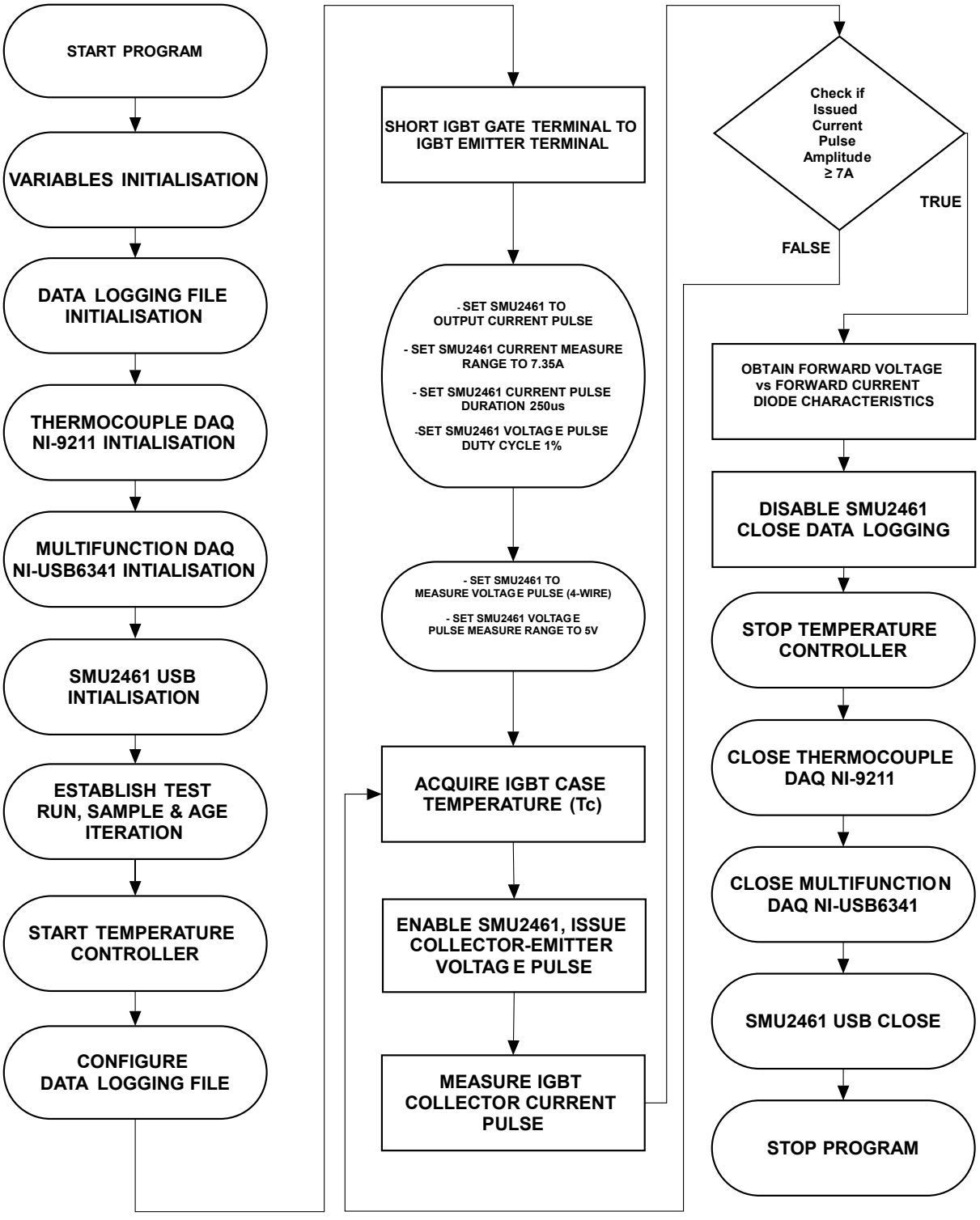


Figure 3.26 - Internal IGBT Diode's Forward Voltage (V_{FD}) software flowchart.

3.5 IGBT's Static Electrical Parameters Characterization Results

This section presents the results obtained from each of the measurements listed in section 3.4. Furthermore, an analysis and discussion of the obtained results vis-à-vis the implemented accelerated ageing procedure is conducted in this section.

3.5.1 IGBT Threshold Voltage & Leakage Current Characterization Results

Figure 3.27 illustrates the relationship between the gate-emitter voltage (V_{GE}) and the collector current (I_C), evolution with the implemented accelerated ageing strategy, for the IGBT Sample 1, measured as described in Section 3.4.1, to obtain the gate-emitter threshold voltage (V_{GE_THRES}). This plot indicates that there was an increase in the gate-emitter threshold voltage (V_{GE_THRES}). It was observed that all the tested IGBTs exhibited an increase in the gate-emitter threshold voltage (V_{GE_THRES}) as evidenced in Figure 3.28. Table 3-11 provides the average gate-emitter threshold voltage (V_{GE_THRES}) and corresponding standard deviation (σ) of the characterized 13 IGBTs, when the IGBTs were new and after each age iteration.

AGE PHASE	IGBT THRESHOLD VOLTAGE (V_{GE_THRES})	
	THRESHOLD VOLTAGE MEAN (V)	STANDARD DEVIATION σ (V)
NEW	5.359	0.0828
AGE ITERATION A	5.828	0.1328
AGE ITERATION B	5.951	0.0415
AGE ITERATION C	6.005	0.0315

Table 3-11 – IGBTs Average Threshold Voltage & Standard Deviation (σ) with Ageing

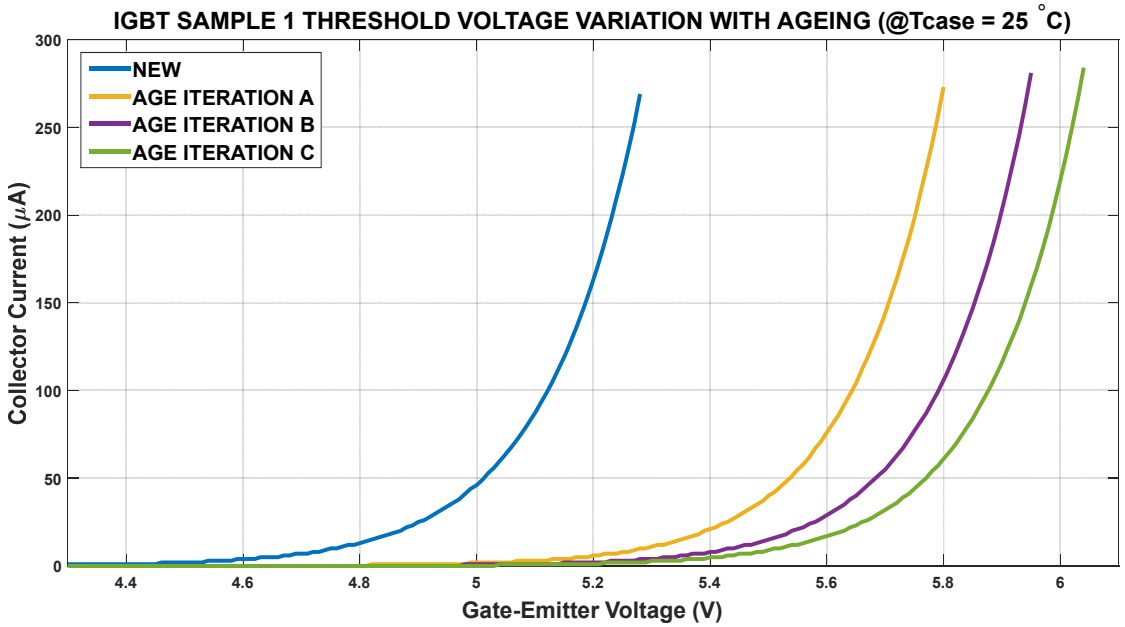


Figure 3.27 – IGBT Sample 1 Threshold Voltage Gate-Emitter Voltage (V_{GE}) vs Collector Current (I_C)

AGE PHASES COMPARISON	IGBT THRESHOLD VOLTAGE (V_{GE_THRES})	
	PERCENTAGE VARIATION (%)	STANDARD DEVIATION σ (%)
AGE A WITH NEW	8.780	2.9688
AGE B WITH NEW	11.238	1.9629
AGE C WITH NEW	12.084	1.8292

Table 3-12 – IGBTs Average Threshold Voltage & σ, Percentage Variation Compared to New

Table 3-12 provides the corresponding average percentage variation of the gate-emitter threshold voltage (V_{GE_THRES}), at each age iteration, when compared to new. After three age iterations, the average IGBT threshold voltage was 6.005V with a corresponding percentage increase of 12.084%. IGBT Sample 1 and IGBT Sample 8 manifested the largest threshold voltage increase of 14.231%. The tested IRG4BC30KDPBF IGBT model has a negative gate-emitter threshold voltage, junction temperature co-efficient ($\Delta V_{GE\_TH}/\Delta T_J$) typically of -12mV/˚C (Table 5 of datasheet) [209]. When considering the die-attach degradation, for constant electrical and environmental conditions, the junction temperature (T_J) would experience an increase. Hence theoretically the gate-emitter threshold voltage (V_{GE_THRES}) should experience a decrease. When considering the measurement procedure undertaken (utilizing very small collector current, smaller than 250μA) and the fact that the IGBT's case temperature (T_C) was maintained at a constant temperature (25°C), than the measured changes in the gate-emitter threshold voltage (V_{GE_THRES}) were considered relatively independent of the junction temperature (T_J). Hence, the measured changes were mainly due to trapped charge in the gate oxide leading to gate oxide degradation, agreeing with the observations obtained by Patil et al. [134].

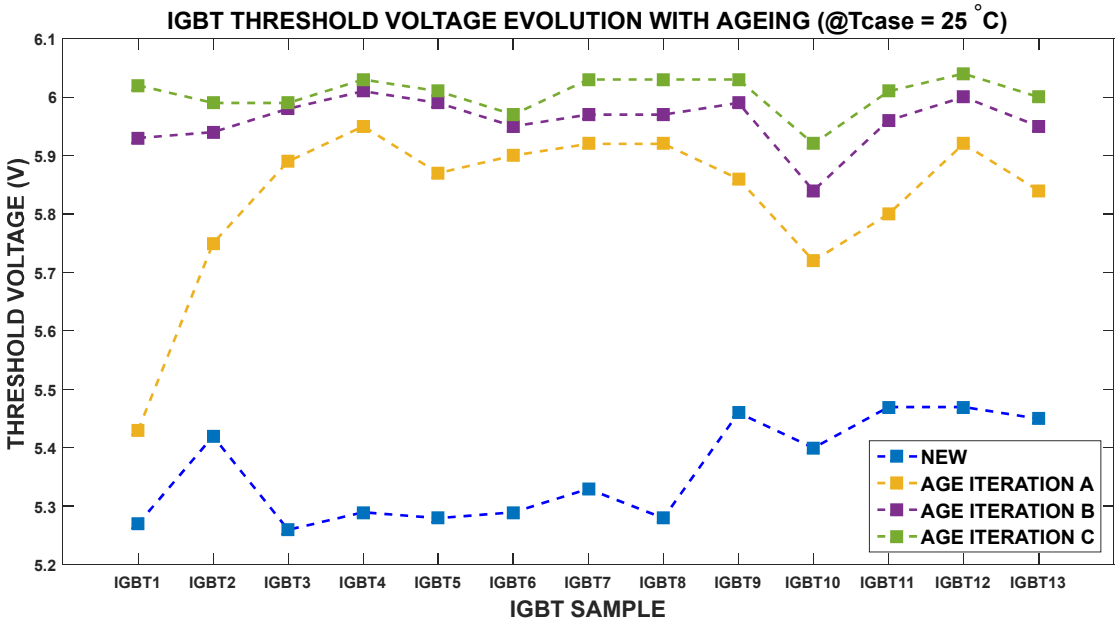


Figure 3.28 - IGBTs Gate-Emitter Threshold Voltage (V_{GE_TH}) Evolution with Accelerated Ageing

AGE PHASE	IGBT GATE-EMITTER LEAKAGE CURRENT (I_{GES})	
	LEAKAGE CURRENT MEAN (nA)	STANDARD DEVIATION σ (nA)
NEW	91.4	3.61
AGE ITERATION A	109.5	4.14
AGE ITERATION B	116.1	2.11
AGE ITERATION C	116.8	2.36

Table 3-13 - IGBTs Average Gate-Emitter Leakage Current & Standard Deviation (σ) with Ageing

Since the shift in the gate-emitter threshold voltage (V_{GE_THRES}) is positive, it corresponds to an oxide degradation due to trapped electrons within the gate oxide. Through capacitance-voltage (C-V) measurement Patil et al. [134], showed that when the gate's dielectric oxide degradation is due to trapped electrons it will contribute to an increase in the gate-emitter threshold voltage (V_{GE_THRES}). On the other side if the trapped charges were holes, the gate-emitter threshold voltage (V_{GE_THRES}) will experience a decrease. Hence the implemented accelerated ageing is not only producing degradation in the die-attach but additionally producing HCI effects, leading to gate-oxide degradation. In this scenario HCI was mainly triggered due to the elevated temperatures during the accelerated ageing procedures. The degradation of the IGBTs' gate-oxide was moreover substantiated by the enhanced gate-emitter leakage current (I_{GES}) vis-à-vis ageing. Table 3-13 provides the average gate-emitter leakage current (I_{GES}) when new and after every age iteration, and the corresponding standard deviation (σ). After three age iterations, the average IGBT gate-emitter leakage current (I_{GES}) was 116.8nA with a corresponding percentage increase of 27.978% when compared to new.

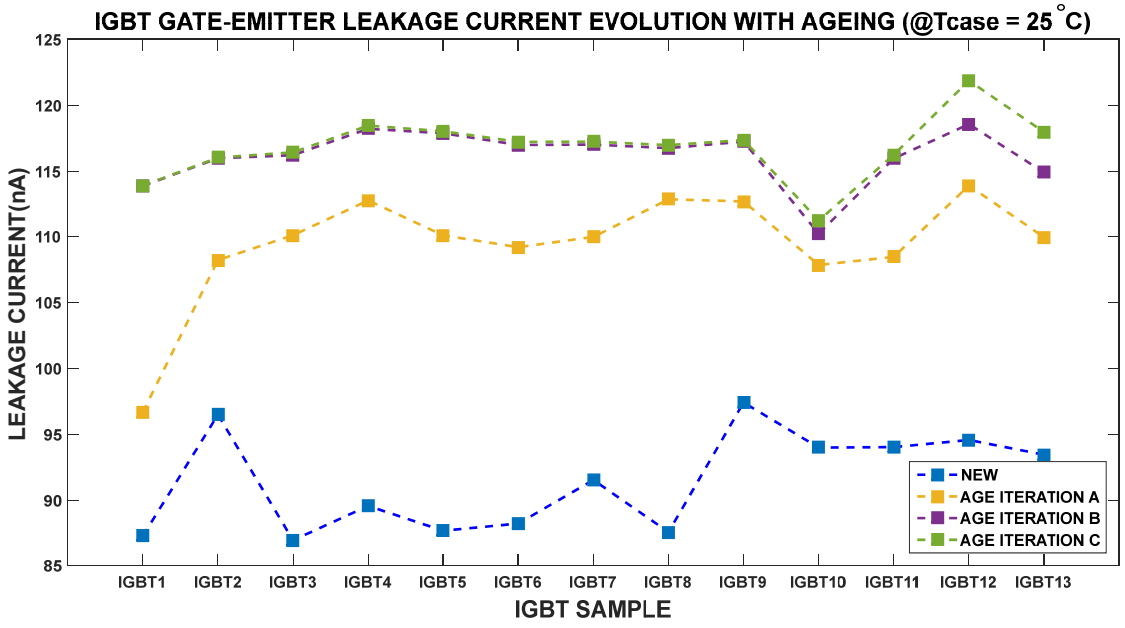


Figure 3.29 - IGBTs Gate-Emitter Leakage Current (I_{GES}) Evolution with Accelerated Ageing

AGE PHASES COMPARISON	IGBT GATE-EMITTER LEAKAGE CURRENT (I_{GES})	
	PERCENTAGE VARIATION (%)	STANDARD DEVIATION σ (%)
AGE A WITH NEW	19.844	5.706
AGE B WITH NEW	27.225	5.724
AGE C WITH NEW	27.978	5.485

Table 3-14 - IGBTs Average Leakage Current & σ Percentage Variation Compared to New

This is indicated in Table 3-14 which provides the corresponding average percentage variation of the gate-emitter leakage current (I_{GES}), at each age iteration, when compared to new. The gate-emitter leakage current (I_{GES}) is essentially the leakage current of the input capacitance of the IGBT. Essentially this leakage current depends on the applied voltage across the gate-emitter, temperature, and dielectric oxide health state [208]. The applied gate-emitter voltage was set to a calibrated constant value (+20V DC), while the temperature was minimized by the measurement technique itself since it involves no collector current (I_C), and the case temperature (T_C) was maintained to 25°C. Hence one can state that the observed gate-emitter leakage current (I_{GES}) increase, was predominantly due to the dielectric oxide degradation. One needs to mention that analogous to the changes observed in the die-attach voiding, both the gate-emitter threshold voltage (V_{GE_THRES}) and the gate-emitter leakage current (I_{CES}) experienced largest changes in the first age iteration, as evidenced again in Figure 3.29.

3.5.2 IGBT On-State Voltage (V_{CE_ON}), On-State Resistance and Output Characteristics Characterization Results

As described earlier, the IGBT's on-state voltage (V_{CE_ON}) is intimately dependent on the junction temperature (T_J). As described in section 3.4.2 three measurements were conducted in this regard. The first measurement was the measurement of the collector-emitter on-state voltage (V_{CE_ON}) during the initial heating stage of each accelerated ageing iteration. The second measurement was the measurement of the collector-emitter on-state voltage (V_{CE_ON}) at a case temperature (T_C) of 25°C, with a short current pulse duration, to avoid self-heating while ensuring that the device is in hard-saturation. The third measurement was the measurement of the output characteristics of the IGBT.

In relation to the first measurement technique, five different collector-emitter on-state voltage (V_{CE_ON}) measurements were conducted at five distinct case temperatures (T_C), namely (50°C, 75°C, 100°C, 125°C and 150°C). Figure 3.30 illustrates the measured collector-emitter on-state voltage (V_{CE_ON}) at the pre-stablished five case temperatures (T_C), for each age iteration.

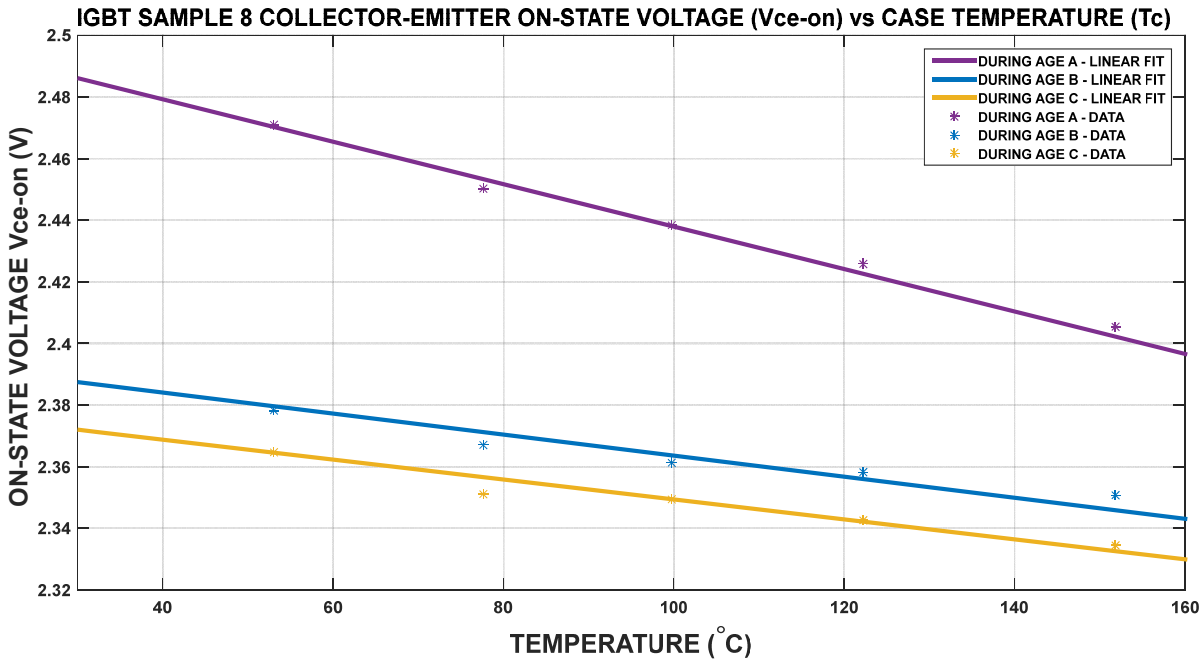


Figure 3.30 – IGBT Sample 3 Collector-Emitter On-State Voltage (V_{CE}) vs Case Temperature (T_C)

Figure 3.30 illustrates the collector-emitter on-state voltage (V_{CE_ON}), negative temperature coefficient as highlighted by the fitted linear relationship and further substantiated by the negative coefficient of the on-state voltage with the junction temperature (T_J) of the tested IGBTs' datasheet [209]. Moreover, this figure evidences the ageing evolution of this relationship. It highlights a negative offset in the collector-emitter on-state saturation voltage (V_{CE_ON}). Tables 3-15, 3-16 and 3-17 tabulate the measurements of the collector-emitter voltage (V_{CE_ON}) at case temperatures (T_C) of 50°C, 100°C and 150°C, respectively. As evidenced in these tables, there was a permanent decrease in this parameter between the different age iterations, with the tested average on-state voltage (V_{CE_ON}) decreasing from 2.464V during Age Iteration A to 2.424V during Age Iteration B and to 2.382V during Age Iteration C at a case temperature of 50°C. Further average decreases were monitored at the two other case temperatures (T_C) of 100°C and 150°C.

Since these measurements were conducted at the same case temperatures (T_C), this leads to the understanding, that the monitored collector-emitter on-state voltage (V_{CE_ON}) decrease, at the same electrical conditions, was due to an enhanced junction temperature (T_J) which was being influenced by an increase in the junction to case thermal resistance (θ_{JC}) due to the degraded die attach. Moreover, Table 3-18 is evidencing an increase with degradation, in the tested collector-emitter on-state voltage and case temperature coefficient ($\Delta V_{CE\_ON} / \Delta T_C$).

IGBT SAMPLE	Collector-Emitter On-State Saturation Voltage (Vce_on) Measurement @ 50°C					
	T(case) Measurement @ 50°C (°C) Age Iteration A	T(case) Measurement @ 50°C (°C) Age Iteration B	T(case) Measurement @ 50°C (°C) Age Iteration C	Vce_on @ 50°C (V) Age Iteration A	Vce_on @ 50°C (V) Age Iteration B	Vce_on @ 50°C (V) Age Iteration C
IGBT 1	50.03	49.89	50.08	2.497	2.407	2.388
IGBT 2	49.83	49.92	50.07	2.458	2.412	2.387
IGBT 3	50.25	50.05	50.16	2.455	2.449	2.420
IGBT 4	50.21	50.23	50.03	2.436	2.443	2.402
IGBT 5	50.23	50.26	49.90	2.461	2.437	2.347
IGBT 6	50.11	50.26	50.20	2.427	2.384	2.361
IGBT 7	49.90	50.22	49.79	2.529	2.485	2.395
IGBT 8	50.18	49.99	49.94	2.477	2.390	2.371
IGBT 9	49.77	49.93	50.17	2.482	2.414	2.383
IGBT 10	49.94	50.09	50.03	2.457	2.419	2.391
IGBT 11	49.90	50.25	50.14	2.439	2.418	2.375
IGBT 12	50.02	50.15	50.25	2.463	2.428	2.363
IGBT 13	50.25	50.23	50.17	2.453	2.421	2.378
MEAN	**50.04**	**50.11**	**50.07**	**2.464**	**2.424**	**2.382**
STD DEV (δ)	**0.19**	**0.14**	**0.13**	**0.027**	**0.026**	**0.019**

Table 3-15 – IGBTs' Collector-Emitter On-State Voltage (V_{CE_ON}) Ageing Evolution @50°C

IGBT SAMPLE	Collector-Emitter On-State Saturation Voltage (Vce_on) Measurement @ 100°C					
	T(case) Measurement @ 100°C (°C) Age Iteration A	T(case) Measurement @ 100°C (°C) Age Iteration B	T(case) Measurement @ 100°C (°C) Age Iteration C	Vce_on @ 100°C (V) Age Iteration A	Vce_on @ 100°C (V) Age Iteration B	Vce_on @ 100°C (V) Age Iteration C
IGBT 1	100.05	100.11	99.79	2.434	2.399	2.373
IGBT 2	99.91	100.21	100.16	2.436	2.402	2.372
IGBT 3	100.10	100.21	99.94	2.427	2.422	2.377
IGBT 4	100.14	100.14	100.00	2.416	2.430	2.376
IGBT 5	100.07	99.82	99.98	2.430	2.395	2.339
IGBT 6	100.12	99.94	100.01	2.407	2.382	2.356
IGBT 7	100.10	100.00	99.94	2.446	2.429	2.378
IGBT 8	99.77	99.83	100.00	2.439	2.363	2.352
IGBT 9	100.01	99.78	100.06	2.446	2.386	2.375
IGBT 10	99.94	100.06	99.96	2.440	2.408	2.385
IGBT 11	99.99	99.97	100.17	2.414	2.401	2.348
IGBT 12	100.10	100.15	100.15	2.433	2.368	2.354
IGBT 13	100.15	100.13	100.18	2.426	2.394	2.342
MEAN	**100.01**	**100.03**	**100.03**	**2.430**	**2.398**	**2.364**
STD DEV (δ)	**0.12**	**0.15**	**0.11**	**0.012**	**0.021**	**0.015**

Table 3-16 - IGBTs' Collector-Emitter On-State Voltage (V_{CE_ON}) Ageing Evolution @100°C

IGBT SAMPLE	Collector-Emitter On-State Saturation Voltage (Vce_on) Measurement @ 150°C					
	T(case) Measurement @ 150°C (°C) Age Iteration A	T(case) Measurement @ 150°C (°C) Age Iteration B	T(case) Measurement @ 150°C (°C) Age Iteration C	Vce_on @ 150°C (V) Age Iteration A	Vce_on @ 150°C (V) Age Iteration B	Vce_on @ 150°C (V) Age Iteration C
IGBT 1	149.98	150.11	150.00	2.408	2.370	2.358
IGBT 2	149.86	150.05	149.94	2.410	2.382	2.345
IGBT 3	150.09	149.99	149.99	2.386	2.379	2.358
IGBT 4	149.90	150.14	149.99	2.393	2.407	2.355
IGBT 5	149.96	150.05	149.95	2.403	2.377	2.323
IGBT 6	149.99	149.98	150.07	2.383	2.365	2.348
IGBT 7	150.10	149.88	149.99	2.418	2.404	2.361
IGBT 8	150.03	149.91	149.97	2.415	2.352	2.346
IGBT 9	150.08	149.99	149.93	2.400	2.374	2.363
IGBT 10	150.08	149.96	150.10	2.404	2.390	2.371
IGBT 11	150.02	150.20	150.05	2.388	2.379	2.346
IGBT 12	149.95	149.94	150.05	2.392	2.352	2.346
IGBT 13	150.10	149.98	150.10	2.381	2.375	2.332
MEAN	**150.01**	**150.01**	**150.01**	**2.399**	**2.377**	**2.350**
STD DEV (δ)	**0.09**	**0.09**	**0.06**	**0.012**	**0.017**	**0.013**

Table 3-17 - IGBTs' Collector-Emitter On-State Voltage (V_{CE_ON}) Ageing Evolution @150°C

AGE PHASE	IGBTs AVERAGE COLLECTOR-EMITTER ON-STATE VOLTAGE CASE TEMPERATURE COEFFICIENT ($\Delta V_{CE\_ON} / \Delta T_C$)	
	TEMPERATURE COEFFICIENT (mV/°C)	STANDARD DEVIATION σ (mV/°C)
DURING AGE A	-0.657	0.197
DURING AGE B	-0.464	0.193
DURING AGE C	-0.315	0.143

Table 3-18 – IGBTs Average Collector-Emitter On-State Voltage Case Temperature Coefficient ($\Delta V_{CE\_ON} / \Delta T_C$) Evolution with Ageing.

The collector-emitter on-state voltage (V_{CE_ON}) was moreover measured as indicated in section 3.4.2, when the IGBT was new and after each ageing iteration, at an IGBTs' case temperature (T_C) of 25˚C. Figure 3.31 shows the IGBTs' on-state resistance evolution with the implemented accelerated ageing. One can observe a decrease in the effective on-state resistance for all tested IGBTs. Since the collector current pulse amplitude was set to a calibrated constant (7A), this directly indicates that it is effectively the on-state voltage (V_{CE_ON}) which has decreased. As indicated in Table 3-20, after three age iterations, the average effective on-state resistance percentage decrease, over that of a new device, was of 22.3% with a maximum percentage decrease of 27.7%. Hence the die-attach degradation is impacting the on-state performance, by causing an increase in the junction-to-case (θ_{JC}) thermal resistance, hence increasing the IGBT's junction temperature, yielding to an increase in the charge-carrier concentration in the drift region, which contributes to an overall decrease of the effective on-state resistance of the IGBT. Again, it is important to point out that all tested IGBTs experienced the largest decrease in the on-state resistance, after the first age iteration, as evidenced in Figure 3.31.

AGE PHASE	IGBTs AVERAGE ON-STATE RESISTANCE (Ω)	
	ON-STATE RESISTANCE (Ω)	STANDARD DEVIATION σ (Ω)
NEW	0.291	0.0153
AGE ITERATION A	0.243	0.0128
AGE ITERATION B	0.234	0.0125
AGE ITERATION C	0.226	0.0086

Table 3-19 – IGBTs Average On-State Resistance Evolution with Ageing.

AGE PHASES COMPARISON	IGBT AVERAGE ON-STATE RESISTANCE PERCENTAGE VARIATION	
	PERCENTAGE VARIATION (%)	STANDARD DEVIATION σ (%)
AGE A WITH NEW	-16.42	3.816
AGE B WITH NEW	-19.51	4.797
AGE C WITH NEW	-22.31	3.666

Table 3-20 – IGBTs Average On-State Resistance & σ, Percentage Variation Compared to New.

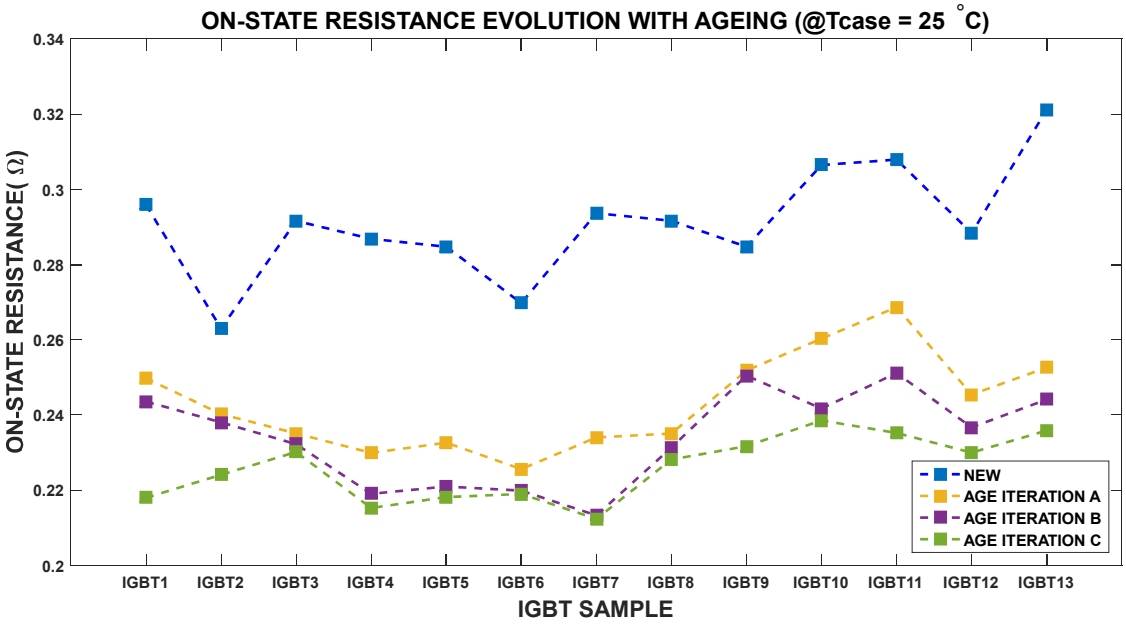


Figure 3.31 - IGBTs On-State Resistance Evolution with Accelerated Ageing

Furthermore, the relationship between the collector-emitter voltage (V_{CE}) and the collector current (I_C), that is the output characteristics of every tested IGBT, were determined before and after each age iteration, at a devices' case temperature (T_C) of 25°C. Figure 3.32 shows the output characteristics variation of IGBT10 for the first 7A of collector current (I_C). One can observe that for the same value of the collector-emitter voltage (V_{CE}), the corresponding collector current (I_C) has increased with each age iteration. This indicates that the effective resistance of the device has decreased. It is important to highlight the fact that each tested IGBT exhibited similar changes in their respective output characteristics, again with the largest changes manifesting after the first age iteration.

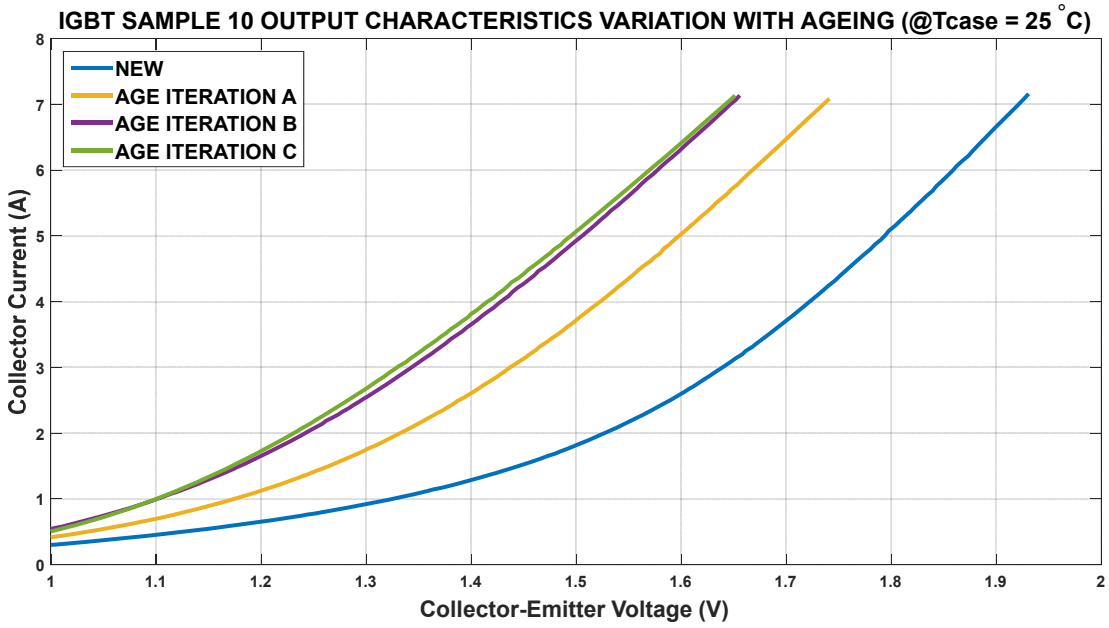


Figure 3.32 - IGBT Sample 10 Output Characteristics Evolution with Accelerated Ageing

3.5.3 IGBT Transfer Characteristics and Forward Transconductance Characterization Results

Figure 3.33 shows the transfer characteristics relationship (gate-emitter voltage (V_{GE}) vs collector current (I_C)) of IGBT Sample 11, for the first 7A of collector current (I_C). The transfer characteristics were determined for every tested IGBT when new and after each age iteration, at an IGBT's case temperature (T_C) of 25˚C. After the IGBT was subjected to the implemented accelerated ageing, one can observe that for the same gate-to-emitter voltage (V_{GE}) the corresponding collector current (I_C) has decreased. This trend progresses for each age iteration. All the other tested IGBTs experienced similar changes in the transfer characteristics. This indicates a decrease in the forward transconductance (g_{fe}) of the device. Figure 3.34 shows the variation of the transconductance (g_{fe}), with the implemented accelerated ageing, for the tested IGBTs.

AGE PHASE	IGBTs AVERAGE FORWARD TRANSCONDUCTANCE	
	FORWARD TRANSCONDUCTANCE (g_{fe}) (S)	STANDARD DEVIATION σ (S)
NEW	6.198	0.256
AGE ITERATION A	5.671	0.261
AGE ITERATION B	5.378	0.283
AGE ITERATION C	5.269	0.284

Table 3-21 – IGBTs Average Forward Transconductance Evolution with Ageing.

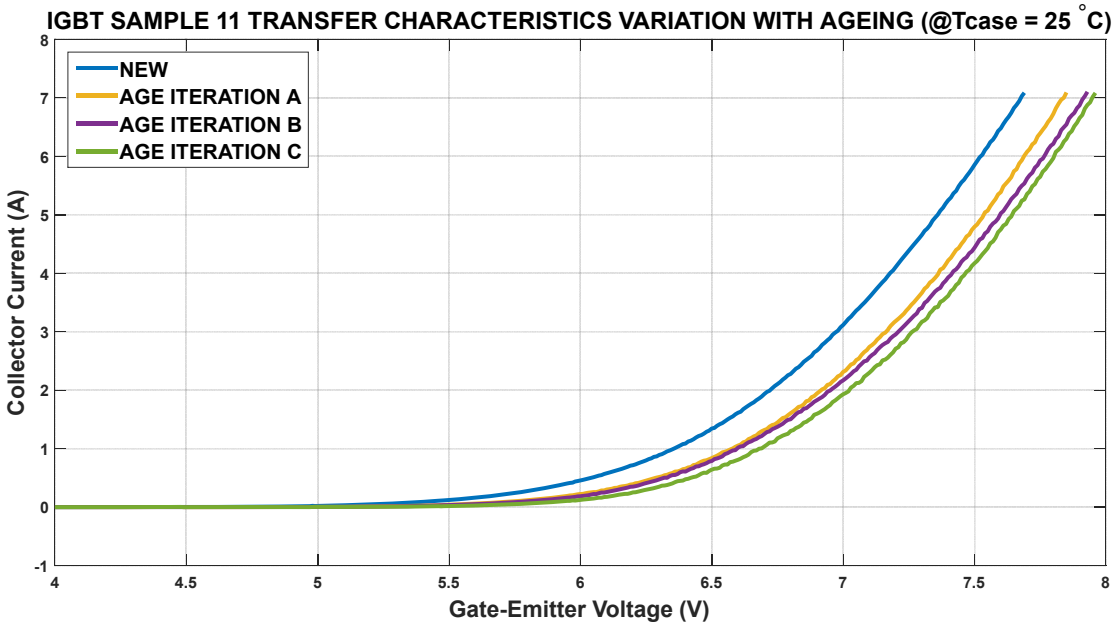


Figure 3.33 - IGBT Sample 11 Transfer Characteristics Evolution with Accelerated Ageing.

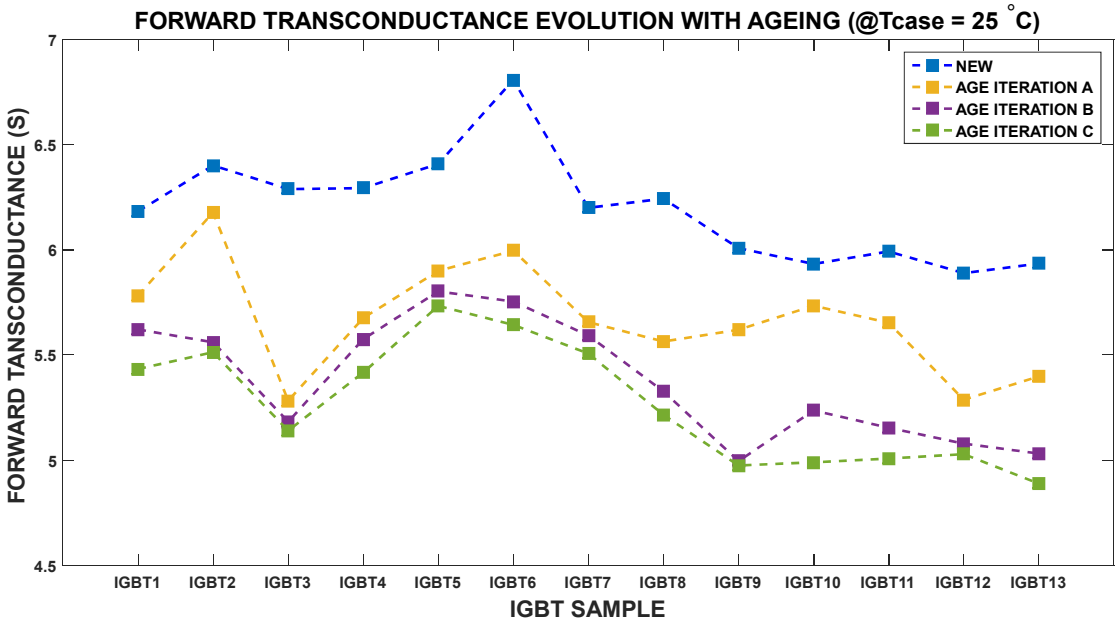


Figure 3.34 - IGBTs Forward Transconductance (g_{fe}) Evolution with Accelerated Ageing

The forward transconductance (g_{fe}) was determined by calculating the slope of the linear region of the transfer characteristics. Table 3-21 tabulates the IGBTs' average forward transconductance (g_{fe}) evolution with the implemented accelerate ageing procedure and corresponding standard deviation (σ). One can observe that tested IGBTs experienced a decrease in the forward transconductance (g_{fe}) with every age iteration. This result is in accordance with the observed gate threshold voltage (V_{GE_THRES}) increase with accelerated ageing, which is inversely related with the forward transconductance (g_{fe}). As indicated in Table 3-22, after three age iterations, the average forward transconductance percentage decrease over that of a new device, was of 15% with a maximum percentage decrease of 18.25% experienced by IGBT Sample 3.

AGE PHASES COMPARISON	IGBTs AVERAGE TRNASCONDUCTANCE PERCENTAGE VARIATION	
	PERCENTAGE VARIATION (%)	STANDARD DEVIATION σ (%)
AGE A WITH NEW	-8.455	3.496
AGE B WITH NEW	-13.234	2.778
AGE C WITH NEW	-15.006	2.532

Table 3-22 – IGBTs Average Transconductance (g_{fe}) & σ, Percentage Variation Compared to New.

3.5.4 IGBT Internal Diode Forward Voltage Drop Characterization Results

Figure 3.35 shows the internal diode forward characteristics of IGBT Sample 3, hence the relationship between the diode's forward current (I_{FM}) and the forward voltage (V_{FM}), up to 7A of forward current (I_{FM}). This relationship was determined for every tested IGBT, when new and after each accelerated ageing iteration.

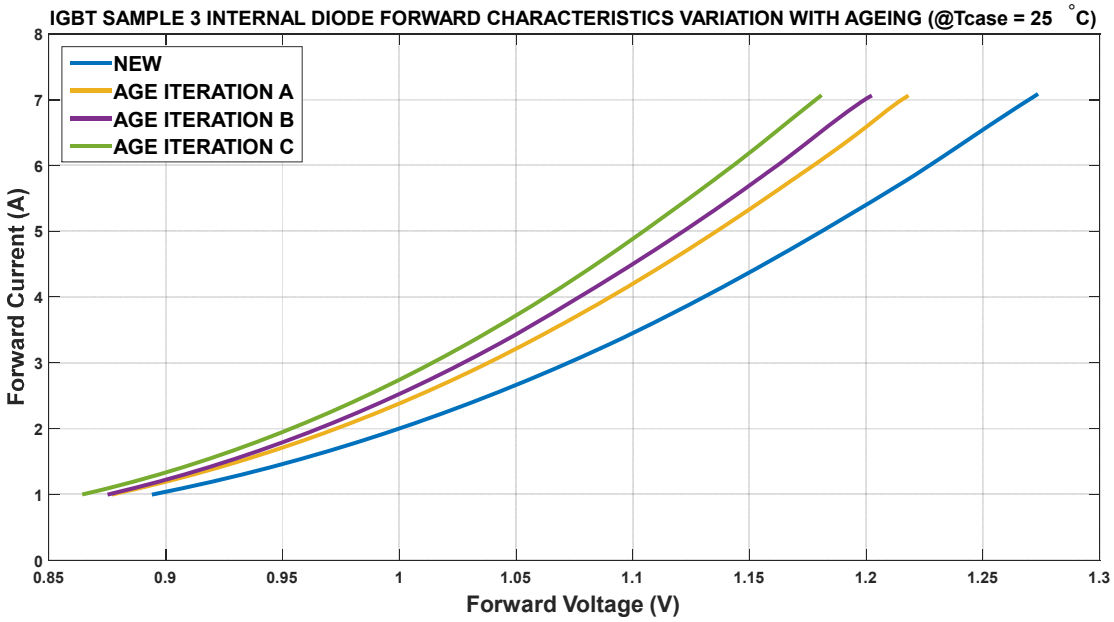


Figure 3.35 - IGBT Sample 3 Internal Diode Forward Characteristics Evolution with Accelerated Ageing.

The IGBTs' temperature was set during measurement, to 25°C. After the IGBT was subjected to the implemented accelerated ageing, one can observe that for the same forward current (I_{FM}), the corresponding internal diode's forward voltage (V_{FM}) has decreased. This trend progresses for each age iteration. All the other tested IGBTs experienced similar changes in the internal diodes' forward characteristics. Figure 3.36 shows the internal diode (V_{FM}) variation of the tested IGBTs with each age iteration, which was determined at a forward current (I_{FM}) of 5A. Table 3-23 tabulates the IGBTs' average internal diode forward voltage (V_{FD}) evolution with the implemented accelerate ageing procedure and corresponding standard deviation (σ). One can observe that the tested IGBTs internal diode experienced a decrease in the forward voltage (V_{FM}) with every age iteration. This result is in accordance with the results observed in the collector-emitter on-state voltage (V_{CE_ON}) and effective on-state resistance. The degraded internal diode die-attach contributed to an enhanced diode's junction temperature (T_{J_DIODE}), thus contributing to an increase in the charge-carrier concentration.

AGE PHASE	IGBTs AVERAGE INTERNAL DIODE FORWARD VOLTAGE	
	DIODE FORWARD VOLTAGE (V_{FM}) (V)	STANDARD DEVIATION σ (V)
NEW	1.1795	0.0079
AGE ITERATION A	1.1401	0.0298
AGE ITERATION B	1.1298	0.0327
AGE ITERATION C	1.1143	0.0332

Table 3-23 – IGBTs Average Internal Diode Forward Voltage Evolution with Ageing.

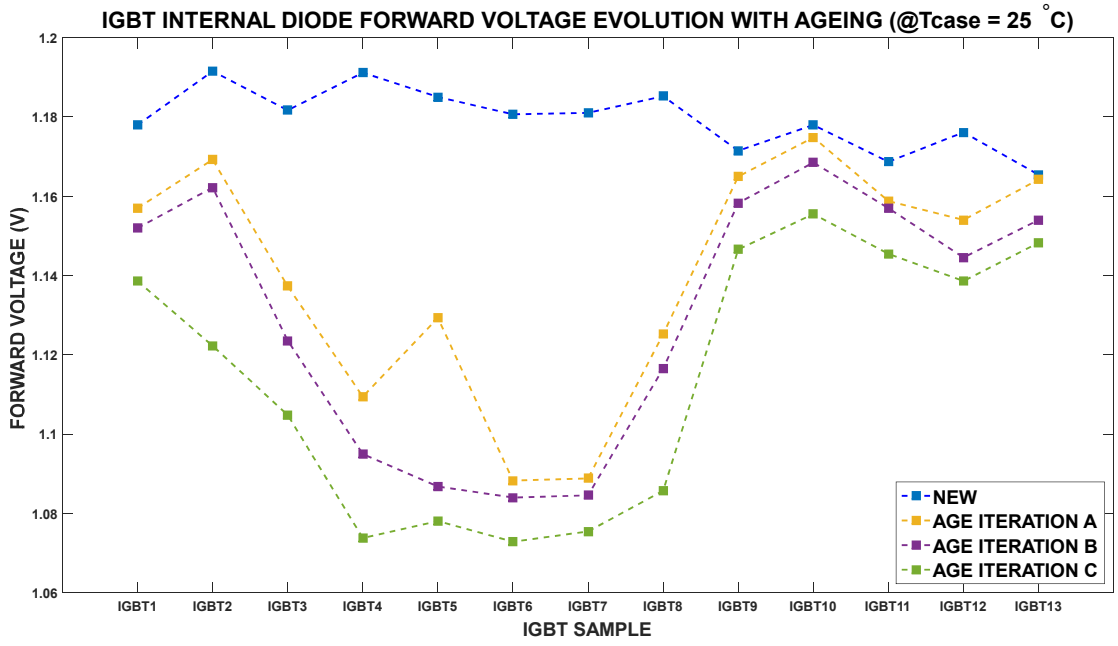


Figure 3.36 - IGBTs' Internal Diode Forward Voltage (V_{FM}) Evolution with Accelerated Ageing

Since the results shown in Figure 3.36 and Table 3-23 were conducted at a calibrated 5A amplitude short duration current pulse, and the case temperature (T_C) was maintained constant at 25˚C, the measured decrease in the diode's forward voltage (V_{FM}) was predominantly due to the degraded diode's die-attach, leading to an increase in the diode's junction temperature and hence the availability of charge carriers, hence obtaining a smaller forward voltage drop (V_F). As indicated in Table 3-24, after three age iterations, the average IGBTs internal diode's forward voltage percentage decrease was of 5.5% with a maximum percentage decrease of 9.9% for IGBT4. Again, it was the first accelerated age iteration which produced the largest average changes in the IGBTs' internal diode forward voltage (V_{FM}).

AGE PHASES COMPARISON	IGBTs AVERAGE INTERNAL DIODE FORWARD VOLTAGE	
	PERCENTAGE VARIATION (%)	STANDARD DEVIATION σ (%)
AGE A WITH NEW	3.331	2.858
AGE B WITH NEW	4.206	3.126
AGE C WITH NEW	5.513	3.275

Table 3-24 – IGBTs Average Transconductance (g_{fe}) & σ, Percentage Variation Compared to New

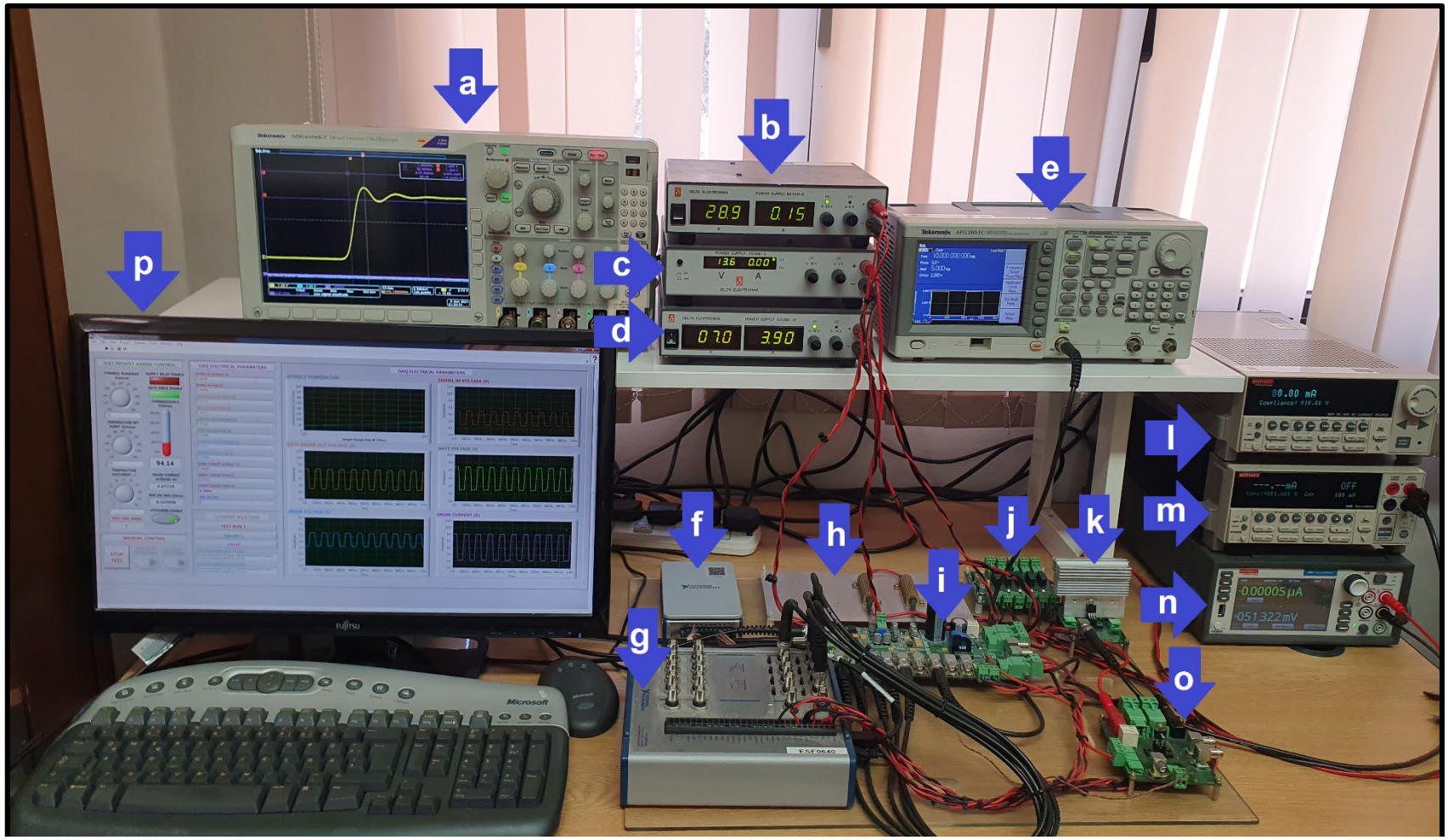


Figure 3.37 – IGBT DC PCAS & Characterization System (a) MDO4104-B Oscilloscope (b) Signal Conditioning Power Supply 1 (c) Signal Conditioning Power Supply 2 (d) Main Power Supply DELTA SM-75-40D (e) Programmable Function Generator Tektronix AFG3051C (f) Thermocouple DAQ NI-9211 (g) NI-USB-6341 Multi-Function DAQ (h) Load Bank (i) IGBT DC PCAS Custom-Built Hardware (j) Relay-Board Custom-Built Hardware (k) Thermoelectric Cooling/Heating Element (l) Thermoelectric Element Control Source Meter Unit (SMU) (m) Characterization Source Meter Unit Keithley SMU2400 (n) Characterization Power Source Meter Unit Keithley SMU2461 (o) Characterization Breakout Board (p) DAQ & Control PC

3.6 Conclusions

The concurrent presentation of the above IGBT's static parameters evolution with the progression of the die-attach degradation, substantiated with X-Ray analysis and hence die-attach voiding progression, is considered a meaningful contribution to knowledge. The characterization of aged IGBTs, showed that the implemented DC PCAS accelerated ageing strategy produced damage mechanisms within the IGBTs' structure, which consequently altered the corresponding static electrical parameters.

X-Ray imagery evidenced that the die-attach suffered the intended degradation during ageing, due to an increased presence of voids. This manifested in both the IGBTs' die-attach as well as the internal diodes' die-attach, even though the degree of voiding was more extensive in the IGBTs' die-attach. This impacted the IGBTs' output characteristics, mainly a decrease in the collector-emitter on-state voltage (V_{CE_ON}) and hence a decrease in the effective on-state resistance. X-Ray imagery evidenced that it was the first age iteration which produced the largest change in voiding. The same can be said for the effective on-state resistance, where it was the first age iteration which produced the largest changes, while consecutive age iterations produce changes of a lesser degree. This trend was present in all tested IGBTs and the corresponding tested electrical parameters. The die-attach plays a fundamental role in the heat dissipation of the device, with the monitored degradation contributing to a deteriorated heat path between the junction to the case of the IGBT. This impacted the IGBT's junction (closest to the collector) to experience higher temperatures when compared to new, hence leading to a higher concentration of charge carriers in the drift region, which led to the decrease of the effective on-state resistance. This same analysis can be extended to the internal free-wheeling diode's die-attach, with the resulting degradation impacting the diodes' forward voltage drop (V_{FM}), leading to a decrease. Furthermore, the utilized ageing strategy produced gate dielectric degradation, predominantly through HCI. This is evidenced by the increase in the gate threshold voltage and decrease in the forward transconductance (g_{fe}). Both, Saha et al. [131] and Patil et al. [134], after conducting IGBT's accelerated ageing, determined, through capacitance-voltage (C-V) measurement, that an increase in the gate's threshold voltage (V_{THRES}), is a result of gate's dielectric oxide degradation due to trapped electrons. This shows that the implemented IGBT accelerated ageing strategy, contributed to a degradation mechanism in both the input (the gate), and the output (collector junction) of the IGBT.

Chapter 4 Switching Parameters Characterization of Aged IGBTs

This chapter reports the monitored changes in the switching parameters of tested IGBTs when subjected to the implemented DC PCAS accelerated ageing strategy. These changes are indicative that the device is at the onset of failure and hence can be utilized within prognostic techniques to determine the health state of the device. Hence this chapter presents the details of the IGBTs' switching transients' evolution with ageing.

4.1 Aim of the Proposed IGBT Switching Parameters Characterization System

The main aim of this part of this research was to provide an understanding in relation to the manifested changes of the IGBT's switching parameters (commonly found within the manufacturer's datasheet) when the IGBT is subjected to power cycling and accelerated ageing. These changes are indicative of failure, while shedding light on the effects power cycling and accelerated ageing has on the EMI of a power electronic circuit when employing an aged IGBT. This comes from the fact that the EMI of a power electronic circuit is heavily influenced by the switching performance of the utilized power device/s. Hence, for this purpose an IGBT Switching Parameter Characterization System (SPCS) was designed, developed, and utilized to provide visibility on the evolution of these switching parameters with the implemented accelerated ageing procedure.

4.2 SPCS Requirements

This section describes the identified IGBT SPCS requirements. Table 4-1 provides the details of the identified requirements for the different subsystems including the IGBT activation, temperature measurement, node voltages and current transients' measurement, timing measurement and power handling capabilities.

Req. No.	Requirement Description
1	The SPCS is intended to accommodate IGBT discrete transistors.
2	IGBT discrete transistors are to be commercially available.
3	The SPCS will utilize the Double Pulse technique, which is a standard technique utilized by PSDs' manufacturers to determine the switching performance of the device.
4	The SPCS must be able to record switching parameters, switching transient, corresponding spectral parameters, and temperature.
5	The SPCS switching parameters should include: the turn-off delay time, fall time, energy loss during fall time, rate of change of collector voltage, turn-on delay time, rise time, energy loss during rise time, rate of change of collector current rise, reverse recovery time, peak reverse recovery current and energy loss during reverse recovery.
6	The SPCS must be designed to perform IGBTs' switching parameters characterization autonomously.
7	The SPCS must provide a user interface for the user to configure and initiate IGBTs' switching parameters characterization tests as well as to monitor the characterization results.
8	The SPCS must allow measurements for applications with DC Link Voltages of up to 650V and Peak Pulsating Current up to 50A. These requirements reflect the stand-off and on-state capabilities of the IGBT studied within this research.
9	The SPCS must have the capability to accurately control and measure the IGBT's case temperature (T_C).
10	The SPCS must have a gate drive voltage capability of up to 20V.
11	The SPCS must have a gate drive slew rate capability of at least 1V/ns, due to typical IGBT discrete transistors' fall times and rise times in the tens to hundreds of nanoseconds range.
12	The SPCS must have a gate drive capability of driving maximum gate input capacitance of 10nF.
13	The SPCS must provide electrical isolation between the gate drive voltage and the gate control voltage.
14	The SPCS must include a power source able of providing the required DC Link voltage and should have output voltage slew rate control.
15	The SPCS must include a programmable function generator able of generating the required input Double Pulse sequence.
16	The SPCS must provide capabilities of measuring: gate voltage (V_G) with voltage measurement capabilities of 50V and able to measure gate transients down to 10ns, collector voltage (V_C) with voltage measurement capabilities of 650V and able to measure collector voltage transients down to 10ns, collector current (I_C) with current measurement capabilities of 50A and able to measure collector current transients down to 10ns.
17	The SPCS must include an inductive load with voltage and current capabilities as listed in requirement 8. The inductive load is the standard load utilized by the Double Pulse technique

Table 4-1 - IGBT Switching Parameters Characterization System (SPCS) requirements.

4.3 Double-Pulse Test Procedure

In most applications, power semiconductor devices (PSDs) are utilized in commutation mode as switches. Hence IGBT manufacturers provide corresponding switching parameters which are fundamental in determining the performance of the device when employed as a switch. For this purpose, IGBTs' datasheets generally quote switching parameters such as Turn-On Delay Time, Rise-Time, Turn-Off Delay Time, Fall-Time, Turn-On Switching Loss, Turn-Off Switching Loss, Total Switching Loss, Diode Reverse Recovery Time and, Peak Reverse Recovery Current. Generally, to determine these parameters, the Double Pulse Test is utilized [209]. The outcomes of this test are typically in the form of transient waveforms captured via an oscilloscope. This test is commonly done with the IGBT connected in common-emitter configuration, switching a clamped inductive load. IGBT Double-Pulse testing, commonly involves the utilization of a half-bridge configuration with two identical IGBTs. The lower IGBT acts as the switch while the upper IGBT through the utilization of the internal diode acts as the clamping free-wheeling diode [210]. This configuration allows the combined switching characterization of the IGBT as well as the internal diode with the same test circuit. This is illustrated in Figure 4.1(a). The test gate waveform consists of two pulses (hence Double Pulse) with a repetition of rate of 1 to 2Hz which avoids the device from heating up. The first pulse is the longer pulse and is used to build-up the current in the inductor according to Equation 4.1:

$$V_{IND} = L\frac{\Delta I_{IND}}{\Delta t} \tag{4.1}$$

where V_{IND} is the voltage across the inductor (V)

L is the load inductance (H)

dI_{IND}/dt is the rate of change of the inductor current (A/s)

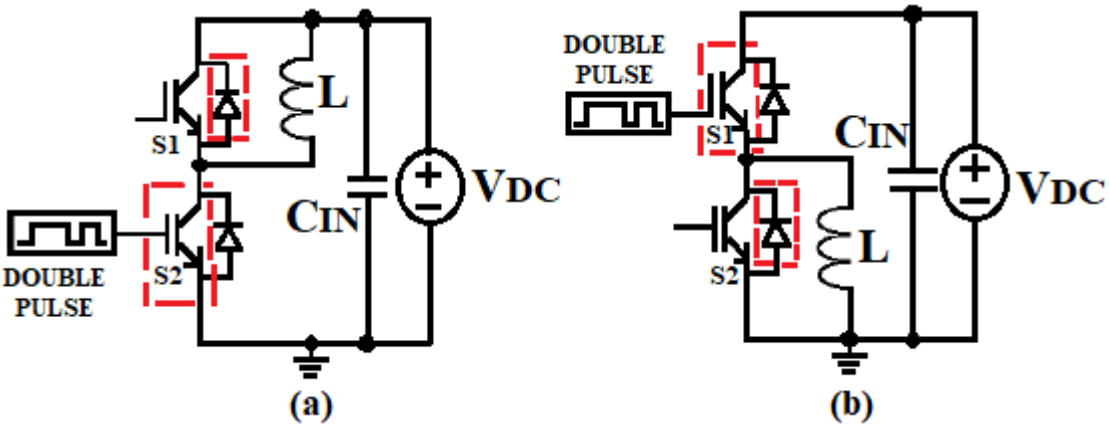


Figure 4.1 - Double Pulse Test Circuit in Half-Bridge Configuration (a) Configured for Characterization of IGBT of S2 (b) Configured for characterization of internal diode of S2.

Figure 4.2 illustrates the Double Pulse Test waveforms. The first pulse's width (T_1) corresponds to the charging time of the inductor, that is the term (Δt) in Equation 4.1. The first pulse (T_1) is adjusted, such that in conjunction with the load inductance (L) and the voltage across the load inductor (V_{IND}), the desired IGBT's test collector current (I_C) is obtained.

Referring to the circuit in Figure 4.1(a), at the end of the first pulse, the desired test current has build-up in the load inductor. At this point, the gate-emitter voltage (V_{GE}) is turned-off, and the inductor current commutates from $IGBT_{S2}$ to the internal free-wheeling diode of $IGBT_{S1}$. This point is the first transition of interest as it is used to measure the Turn-Off characteristics of $IGBT_{S2}$. This is followed by a short delay (T_2), set long enough for the currents and voltages to settle. During this delay the free-wheeling diode maintains circulating the inductor current, hence retaining the same test current for the Turn-On characterization.

This delay is in-turn followed by a second narrow pulse T_3, during which the retained test current is commuted from the internal free-wheeling diode of $IGBT_{S1}$ to $IGBT_{S2}$. At the beginning of this pulse the Turn-On characteristics are measured. During T_3, the current in $IGBT_{S2}$ continues to increase, exceeding the rated test current. Since the salient part of the pulse T_3 is at the beginning, this second pulse is made as short as possible. Hence the parts of interest in the Double Pulse Test waveforms are at the end of the first pulse and at the beginning of the second pulse corresponding to the Turn-Off and Turn-On characteristics respectively. Figure 4.1(a) illustrates how through a half-bridge configuration the Turn-On and Turn-Off characterization of $IGBT_{S2}$ can be obtained.

Apart from the Turn-On and Turn-Off parameters, IGBT switching parameters include the commutation capabilities of the internal free-wheeling diode namely the Peak Reverse Recovery Current and the Reverse Recovery Time. For this purpose, the half-bridge configuration illustrated in Figure 4.1 is configured such that the Double Pulse is issued to the gate of $IGBT_{S1}$, while the internal diode of $IGBT_{S2}$ is utilized as the free-wheeling diode. This configuration is illustrated in Figure 4.1(b) showing how the reverse recovery characteristics of the internal diode of $IGBT_{S2}$ can be determined by a marginal change in the test circuit. Hence, the two half-bridge configurations in Figure 4.1 illustrate how the switching transients and hence the switching parameters of $IGBT_{S2}$ for both the IGBT and the internal free-wheeling diode can be measured and obtained.

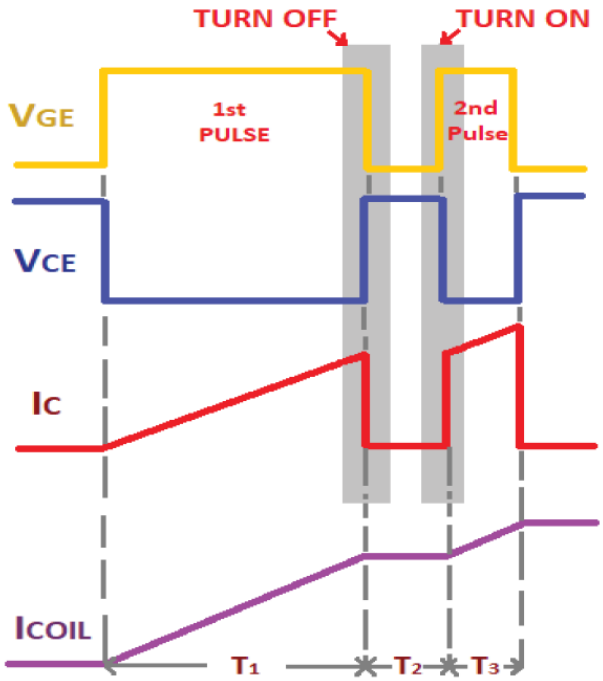


Figure 4.2 – Double Pulse Technique Test Waveforms

4.4 Implemented IGBT Switching Parameters Characterization System (SPCS)

In relation to the IGBT switching parameters characterization, the main transients of interest during this test are, the gate voltage transient (V_G), the collector voltage transient (V_C), and the collector current transient (I_C), during both Turn-On and Turn-Off. Moreover, for the internal diode commutation characterization, the main transients of interest are the internal diode's forward current transient (I_F) and forward voltage transient (V_F). Figure 4.3 illustrates the system architecture of the implemented IGBT Switching Parameters Characterization System (SPCS). The system consists of commercial instrumentation, as well as custom-built software and hardware.

4.4.1 SPCS Commercial Instrumentation

The commercial instrumentation includes a Tektronix MDO4104B-3 Mixed Domain Oscilloscope, with specifications of 1GHz bandwidth and sampling of 5 GS/s combined with a 3GHz bandwidth spectrum analyzer. It was utilized to capture the three required IGBT signals; the gate voltage (V_G), the collector voltage (V_C), and the collector current (I_C). Since the collector voltage (V_C) node was exposed to the DC link voltage, a Tektronix TPP0850 800MHz 1.8pF/40MΩ 1000V passive high voltage probe was utilized to capture the collector voltage (V_C) transients.

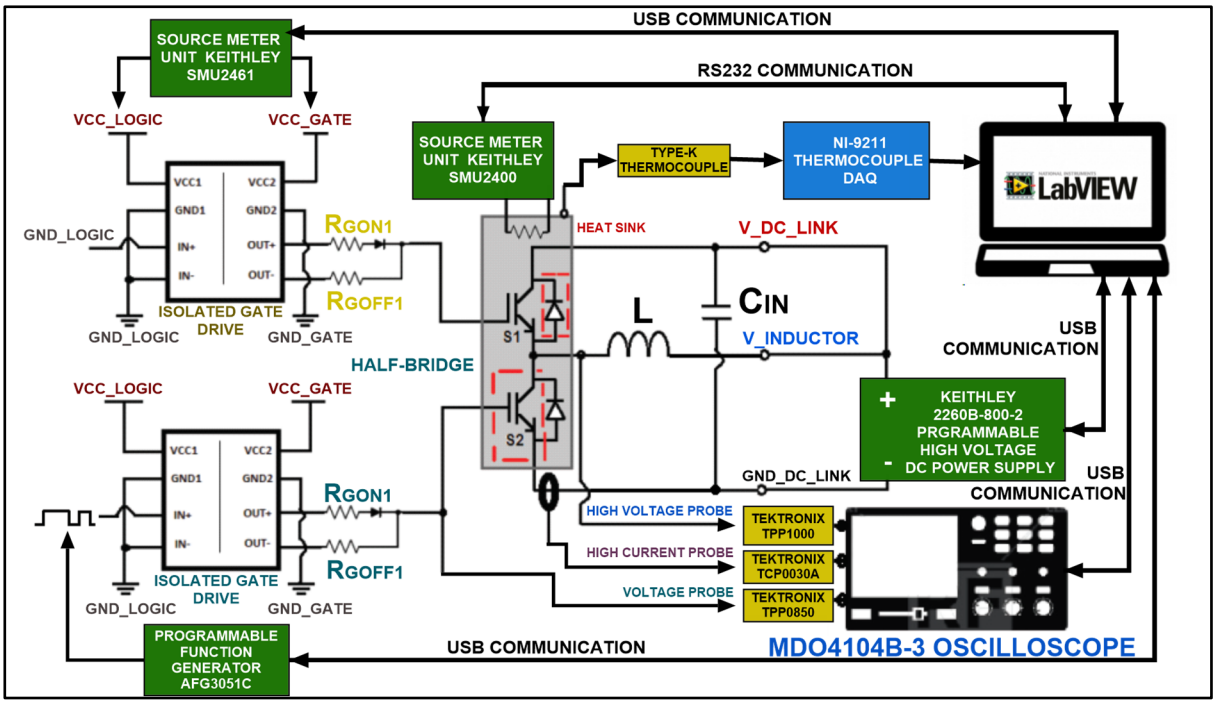


Figure 4.3 – Switching Parameters Characterization System Architecture

A Tektronix TCP0030A AC/DC 120MHz 30A RMS current probe, was utilized to measure the collector current (I_C) transients. Moreover, this current probe permits low current measurements down to 1mA. Finally, a Tektronix TPP1000 1GHz 300V 3.9pF/10MΩ passive voltage probe was utilized to measure the gate voltage (V_G) transients. The oscilloscope was interfaced with the test PC via USB.

The Keithley 2260B-800-2 programmable 800V 2.88A 720W, DC power supply was utilized to source the high DC link voltage. One of the salient benefits of this high voltage DC power supply, was that it enables the control of the voltage and current rise time and fall time, with capabilities of output voltage slew rate range of 0.1V/s to 1600V/s and current slew-rate range of 0.001A/s to 216A/s. This prevents from potentially dangerous in-rush currents from flowing to low impedance loads such as the DC link decoupling capacitors. This power supply was programmed and interfaced via USB with the test PC.

A second auxiliary low voltage DC source was utilized to power the logic circuitry and the gate drive voltage (V_G). Due to the importance on the precision and repeatability of this DC source a Keithley SMU2461 was utilized to power the logic circuitry and gate drive section. This too was interfaced via USB to the test PC.

A Tektronix AFG3015C programmable function generator was utilized to define and issue the double pulse test waveform. A programmable function generator was required since the generation of an arbitrary waveform was necessary due to the independence of the different Double Pulse waveform phases (T_1, T_2, and T_3) from each other. Finally, a Keithley 2400 SMU was utilized to source current through a power resistor, attached with the half-bridge heat sink to control the IGBTs case temperature (T_C). This SMU was configured and controlled from the test PC via RS232.

4.4.2 SPCS Custom Hardware

Custom hardware was utilized for the Double Pulse half-bridge configuration illustrated in Figure 4.1. This was based on the Double Pulse testbed described in [210]. The hardware consists of two different sections, namely the gate drive section (illustrated in Figure 4.4) and the Half-Bridge power circuit (illustrated in Figure 4.5). Double Pulse testing is nominally conducted at a DC link voltage set to eighty per cent (80%) of the breakdown voltage (V_{CEO}) of the device under test, which for power devices this involves the utilization of high DC voltages. Hence one of the important aspects of this hardware is galvanic electrical isolation between the low-power gate drive logic input stage and the high-power half-bridge stage. For this purpose, two Infineon Technologies 1EDI60I12AF (IC1 and IC2, Figure 4.4) single channel isolated IGBT gate drivers were utilized for each IGBT of the half-bridge configuration. This IGBT gate driver has an isolation of 1200V between the input and the output through a galvanically isolated internal coreless transformer technology. Moreover, it provides separate source and sink pins on the output stage, hence providing customized switching control through distinct gate resistances for turn-on and turn-off. To ensure galvanic isolation both the input and output gate driver circuits' power supplies should also be galvanically isolated. The input power supply was obtained from the DC auxiliary power supply (AUX, Figure 4.4), sourced by the Keithley SMU2461 source meter unit. This auxiliary DC voltage was fed to an LM7805 +5V DC voltage regulator, to supply the input logic stage of the two gate drivers.

The output gate drivers' power supply voltages should reflect the low-side and high-side operational voltages of the IGBT gate, to ensure that the IGBTs were driven in hard cut-off and hard saturation. To ensure galvanic isolation from the gate drivers' logic input stage power source (both gate drive power supplies were to be sourced by the auxiliary supply), a Vacuumschmelze T60403-D4615-X054 (TR1) gate drive pulse transformer was employed.

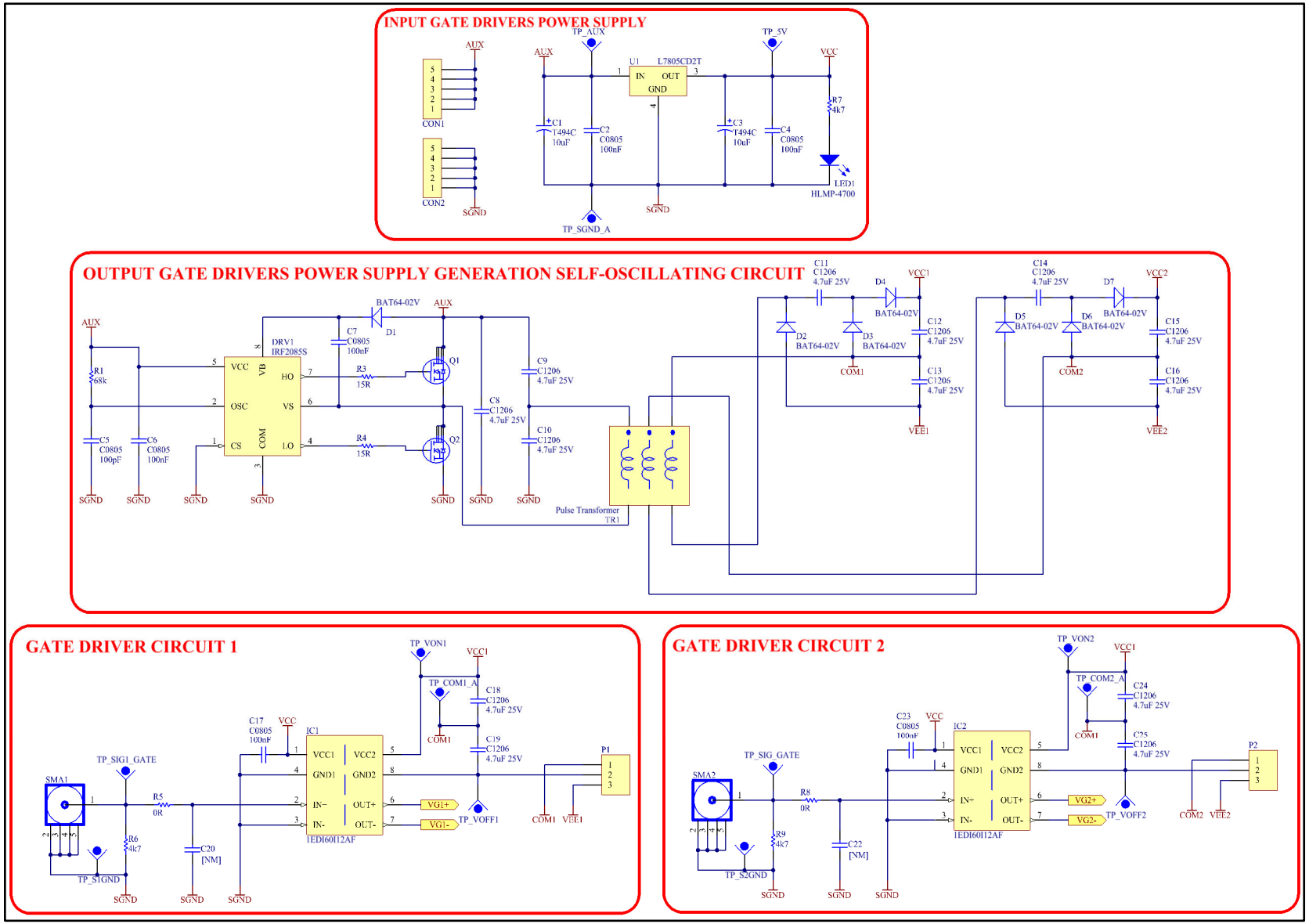


Figure 4.4 - SPCS Custom Hardware Gate Drive Circuit [210].

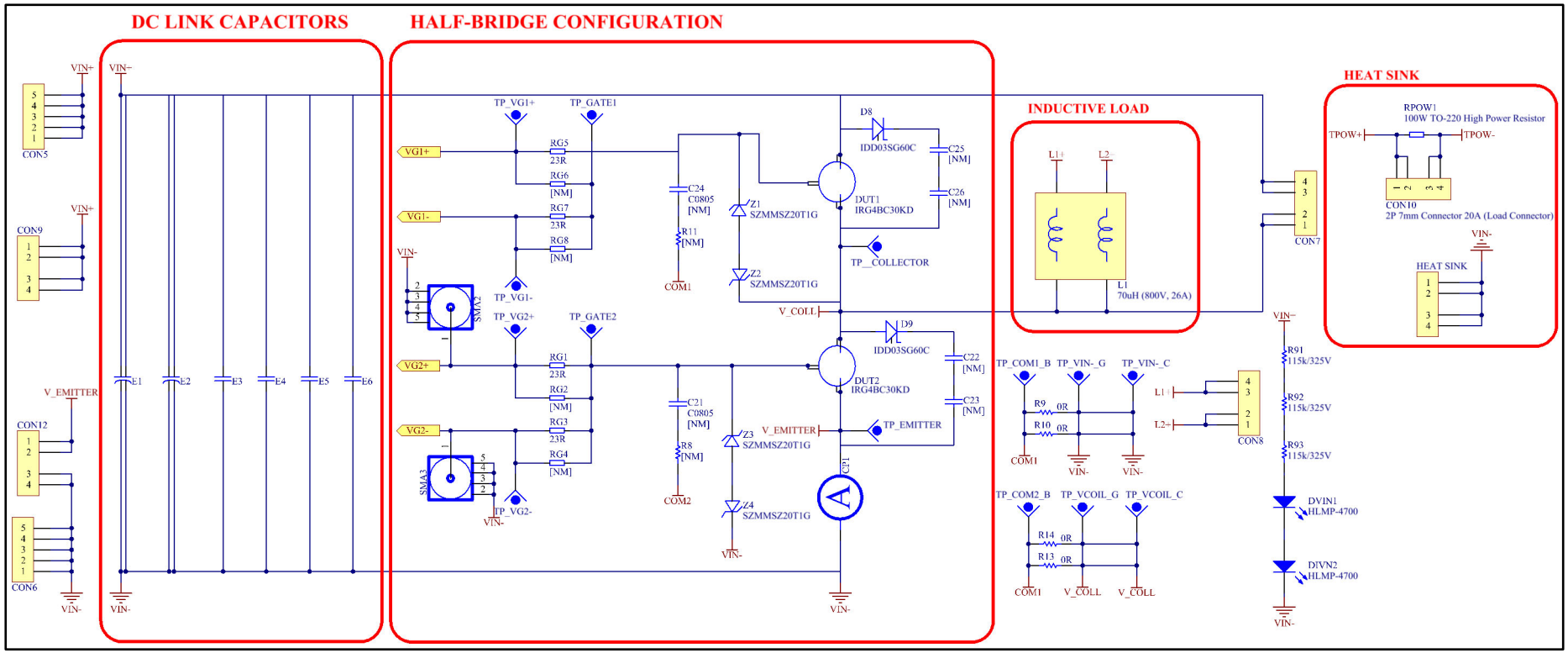


Figure 4.5 - SPCS Custom Hardware Half-Bridge Power Circuit [210].

This transformer has two secondaries with step-up ratios of 1:1.2 and 1:1.2. The primary of this transformer was driven by an Infineon Technologies AUIR2085S (DRV1, Figure 4.4), a high-speed self-oscillating 50% duty cycle half-bridge driver. In conjunction with bootstrapping circuit (D1 and C7) and push-pull MOSFET stage (Q1 and Q2), this self-oscillating half bridge driver swung the primary of the pulse transformer between the auxiliary supply voltage (AUX, Figure 4.4) and the negation of this supply voltage. On the secondaries this oscillating voltage was filtered and rectified generating the required high-side, common and low-side gate voltages, for each of the two gate drivers. SMA connectors (SMA1 and SMA2, Figure 4.4), were utilized to input the Double Pulse waveforms from the programmable function generator. The power section mainly consists of: the half-bridge configuration IGBTs, the corresponding passive gate drive components, the load inductor (L_1, Figure 4.5) and the DC link capacitors. Metal Electrode Leadless Face (MELF) resistors were utilized for each of the IGBT drivers R_{G_ON} and R_{G_OFF} resistors, due to the high accuracy and long-term stability of this resistor technology. TO-220 test socket pins were utilized for the two IGBTs. Even though test socket introduced some lead inductance during the switching parameters characterization, it facilitated the testing procedure of multiple IGBT samples. It is important to mention that the test socket pins employed, were of the soldered type (not spring loaded) to minimize the pins' lead inductance. A 66μH, 800V, 26A custom high current choke was utilized as load inductance. Two EPCOS B32778G 60μF 800V polypropylene DC Link capacitors (E1 and E2 in Figure 4.5) were utilized for the input capacitance (C_{IN} in Figure 4.1). These capacitors have good over-voltage capabilities and low losses with high current capability. These were placed across the DC Link voltage (V_{IN+}-V_{IN-} in Figure 4.5) supplied from the Keithley 2260B-800-2 high voltage power supply, to minimize the effects of voltage variations as the load changes. Furthermore, these capacitors provided a low impedance path for transient currents generated by power switching, while mitigating cables' inductance effects. Moreover, four EPCOS B32652 100nF 1kV polypropylene capacitors (E3 to E6 reference Figure 4.5) were connected across the DC link voltage (V_{IN+}-V_{IN-}) in parallel with (E1 and E2), to provide further high frequency decoupling. The IGBT half-bridge configuration was attached to a heat sink. The main purpose of the heat sink was not to dissipate heat from the half-bridge IGBTs (Double Pulse waveform employed short pulse durations and were repeated every 0.1ms with a duty cycle of 6%) but primarily to dictate the case temperature (T_C) of the IGBTs during testing. For this purpose, the heat sink was attached with an Arcol AP101 100mΩ 100W TO-247 power resistor. This power resistor was energized via constant current through the SMU2400 source meter unit to heat up the heat-sink to a pre-determined

case temperature (T_C). The heat sink temperature and hence the IGBTs' case temperature (T_C) was measured via a Type-K thermocouple, in conjunction with the NI-9211 Thermocouple DAQ. Both this latter DAQ and the SMU2400 were interfaced with the test PC, via USB and RS-232 respectively, with the test PC controlling the IGBTs case temperature (T_C) by enabling and disabling the SMU2400. The circuit was implemented on a four-layer PCB, where the main design criteria for the PCB layout was to ensure galvanic electrical isolation between the input and the output of the gate drivers, galvanic electrical isolation between the low-voltage levels and the high-voltage levels, segregation between the low power electronics and the high-power electronics, and low parasitic inductance on the high-power loop.

4.4.3 SPCS Custom-Built Software

Figure 4.7 illustrates the GUI of the software developed within NI Labview environment, to control the Double Pulse test procedure and acquire the IGBTs' switching waveforms. This software interfaces the test PC with; the programmable function generator via USB, the NI-9211 thermocouple DAQ acquiring the IGBTs case temperature (T_C) via USB, the SMU2400 to set the IGBTs case temperature (T_C) via RS232, the SMU2461 to define the auxiliary gate drive input voltage via USB, the 2260B-800-2 high voltage power supply via USB and the MD04104B-3 mixed domain oscilloscope via USB. The developed software initiates by requesting the user to input: the Double-Pulse phase timings (T_1, T_2 and T_3), choosing the IGBT's switching phase of interest (Turn-On, Turn-Off, and Reverse Recovery), and choosing

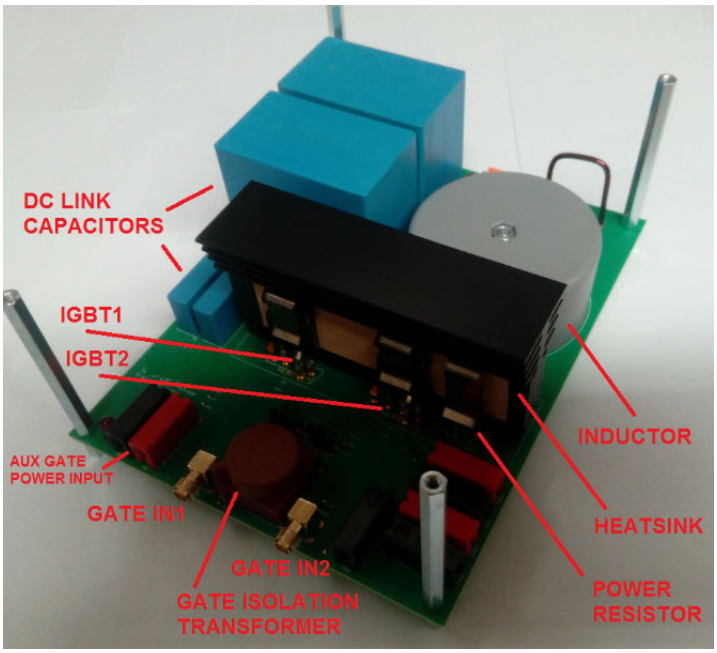


Figure 4.6 – SPCS Custom Hardware Mounted PCB

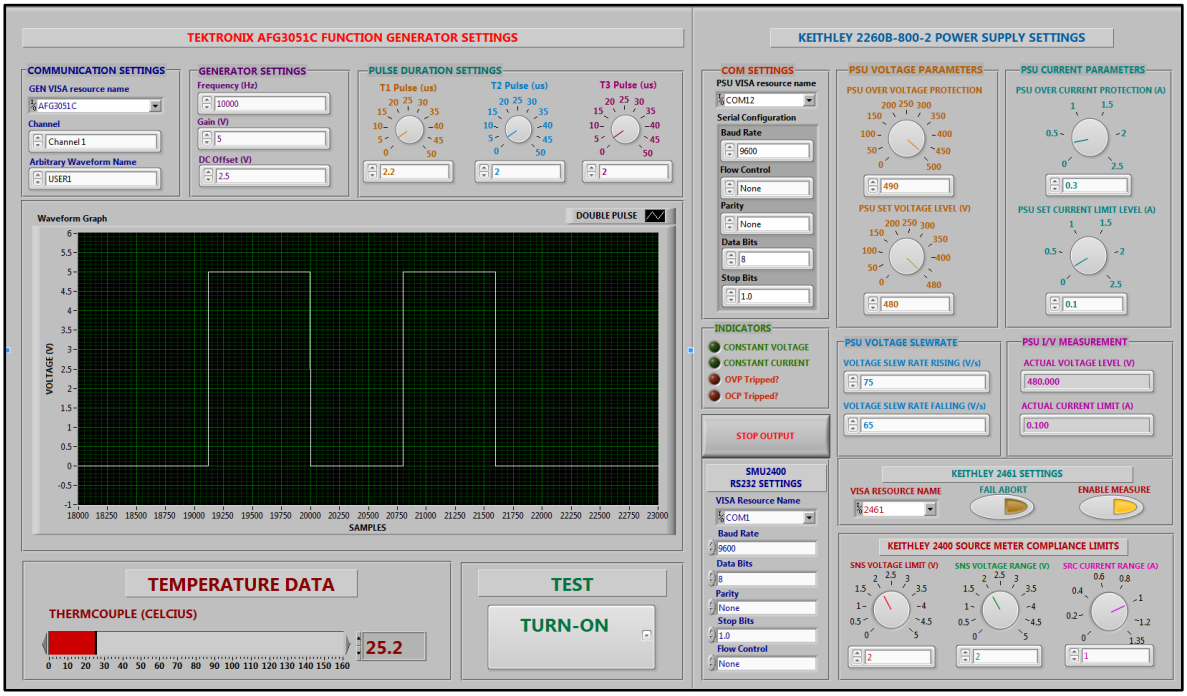


Figure 4.7 - SPCS Double-Pulse Test Custom Built Software GUI

mainly the test voltage, the output voltage slew-rate increase, the output voltage slew-rate decrease and the power supply protection parameters. The developed software progresses by initializing the function generator, the high voltage power supply, and the oscilloscope to the inputted and preset parameters. Three oscilloscope setups were programmed and saved within the instrument's memory reflecting the different oscilloscope settings (Y-Scale, Y-Position, X-Scale, X-Position, Triggering Mode and Level etc) based on the user's test selection (i.e. Turn-On, Turn-Off and Reverse Recovery). The SMU2461 is initialized to output DC voltage set at 13.531V, since this voltage reflects the input pulse transformer exact step-up ratio (i.e. 1:1.108) to produce a gate drivers output voltage of exactly 15V. Finally, the SMU2400 is initialized to output constant current while the NI-9211 thermocouple DAQ is initialized to measure IGBTs' case temperature (T_C). A trivial temperature controller algorithm was implemented on the test PC, with the aim to maintain the heat sink and hence the IGBTs' case temperature (T_C) to a constant value. The heat sink temperature was determined via a Type K thermocouple which was acquired via the test PC through the NI-9211 Thermocouple DAQ. The SMU2400 is enabled until the IGBTs' case temperature (T_C) reaches and is maintained at the required measurement temperature of 25°C. The developed program is maintained controlling and measuring the IGBTs case temperature (T_C) for a predefined time delay (20 seconds) to ensure that the case temperature (T_C) has stabilized. Eventually, all the other commercial instrumentation are successively enabled, each time the software requesting authorization

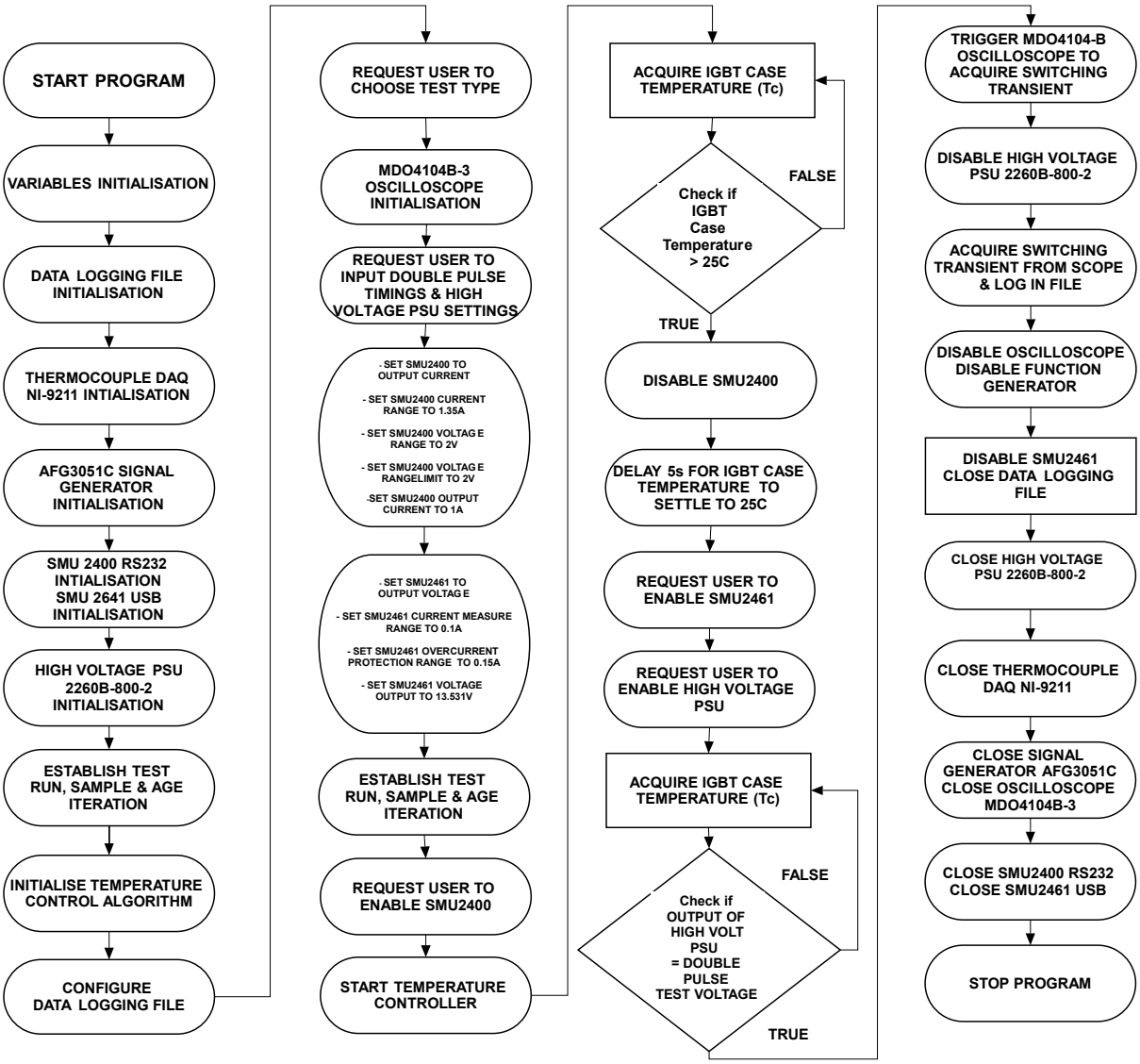


Figure 4.8 - SPCS Double-Pulse Test Custom Built Software Flowchart

from the user to enable the instrument. This procedure was included to allow the user to monitor the initialization of each instrument, hence providing instances to stop the test procedure if erroneous instrument initialization or hardware problems are encountered. The last commercial instrument to be enabled is the high voltage power supply. At this point the high voltage power supply starts increasing the output voltage according to the output voltage slew-rate increase parameter. As the output voltage reaches the Double Pulse test voltage, the oscilloscope is triggered to acquire the chosen phase of the IGBT's switching waveforms. The waveforms retrieved by the oscilloscope are acquired by the test PC and logged in a corresponding test file. The output voltage of the high voltage power supply is decreased to 0V, at which point all the test instrumentation are disabled and corresponding communication is closed. The flow chart for this software is illustrated in Figure 4.8.

4.4.4 IGBT Switching Parameters Characterization Experimental Procedure

The DC PCAS system described in Chapter 3, was utilized to conduct IGBT accelerated ageing. The second accelerated ageing procedure described in section 3.3.4, was employed during the switching parameters characterization. The same IGBT (IRG4BC30KDPBF) utilized during the static parameters' characterization, was utilized for the switching parameters characterization. In relation to Figure 4.1, the DUT was $IGBT_{S2}$.

$IGBT_{S1}$ was the same kind of IGBT but was not subjected to any accelerated ageing. Both devices were attached to a heat sink with an attached power resistor, which was energized via the SMU2400 through constant current, to control the heatsink temperature and hence the IGBTs case temperature (T_C). Generally, IGBTs' datasheets quote switching characterization at 25°C and 150°C. This study presents the switching characterization of new and aged IGBTs at 25°C only, to avoid secondary thermal effects. To obtain the Turn-On and Turn-Off switching transients of new and aged IGBTs, the SPCS circuit was configured as shown in Figure 4.1(a), with the double pulse issued to $IGBT_{S2}$, while $IGBT_{S1}$ acting as the freewheeling diode.

The test conditions were set as highlighted in the IGBT's datasheet. The gate-emitter on-state voltage (V_{GE_ON}) was set to 15V while the gate-emitter off-state voltage (V_{GE_OFF}) was set to 0V. The DC link voltage (V_{DC}) was set to 480V DC, reflecting eighty per cent of the 600V DC primary breakdown voltage (V_{CEO}) of the characterized IGBT. The test collector current (I_C) was set to 16A. The on-state gate resistance $R_{G(ON)}$ was set to 33Ω, and the off-state gate resistance $R_{G(OFF)}$ was set to 10Ω. The above test conditions and load inductor (L) of 66µH, resulted in the double pulse timings of T_1 = 2.2µs, T_2 = 2µs and T_3 = 2µs.

The reverse recovery characterization of the internal diode of $IGBT_{S2}$, was conducted by setting the SPCS custom circuit, according to the circuit illustrated in Figure 4.1(b). The reverse recovery test conditions are set as highlighted in the device datasheet with a reverse voltage (V_R) of 200V DC and forward current (I_F) of 12A. During IGBTs' switching parameters characterization, the threshold voltage (V_{THRES}), the forward transconductance (g_{fe}), and the effective on-state resistance were measured at 25°C, according to the procedure described in Section 3.4.

These measurements served as an indicator to ensure the same level of degradation as obtained during the static parameters' characterization. Switching characterization was conducted when the device was new and after each accelerated age iteration, ensuring each time that the device case temperature (T_C) cooled and stabilized at 25°C. This procedure was repeated for the pre-established three age iterations, reflecting a complete ageing procedure.

It is important to highlight that the main difficulty encountered with the above switching parameters characterization procedure, was that the IGBTs were to be characterized at the above switching test conditions (as quoted in datasheet, 480V DC, 16A) [209], even when the IGBTs were at a degraded stage after accelerated ageing. This impacted on the IGBT population which managed to successfully survive the three accelerated age iterations and consecutively characterized at the above test conditions. For this purpose, it was considered prudent to characterize the IGBTs at a more moderate switching test condition (i.e. 200V DC, 6.67A). A test campaign of twelve IRG4BC30KDPBF IGBTs taken from three different batches was conducted, with the outcome of ten IGBTs surviving the pre-established three accelerated age iterations and successfully completing the switching parameters characterization at 200V DC.

Another test campaign of ten IRG4BC30KDPBF IGBTs taken from two different batches was conducted, with the outcome of five IGBTs managing to survive the pre-established three accelerated age iterations procedure and successfully completing the switching parameters characterization at 480V DC. It is important to highlight that the above difference in this test procedure was only applied for the Turn-On and Turn-Off characterization, as the same test conditions (i.e. 200V, 12A) were retained for the internal diode reverse recovery characterization.

4.5 IGBT Accelerated Ageing Switching Parameters Characterization Results

This section will discuss the switching parameters evolution with the implemented accelerated ageing strategy. Results are mainly categorized into three sections namely Turn-Off, Turn-On and the reverse recovery results.

4.5.1 Turn-Off Delay Time (t_{D_OFF}), Fall-Time (t_F), Turn-On Switching Loss (E_{OFF}) and Collector-Emitter Voltage Rate of Change during Turn-Off (dV_{CE}/dt_{OFF})

The Turn-Off Delay Time (t_{D_OFF}) is the time difference between the points where the gate-emitter voltage (V_{GE}) is at 90% of $V_{GE\_NOMINAL}$ (i.e. 13.5V) and the collector-emitter voltage (V_{CE}) is at 10% of V_{DC} (i.e. 48V for the test with V_{DC} 480V and 20V for the test with V_{DC} 200V). During this time the IGBT's internal surface power MOSFET structure, channel, is removed and further supply of charge carriers from the emitter is cut. The Fall Time (t_F) is the time difference between the points where the collector current I_C is at 90% of $I_{C\_NOMINAL}$ (i.e. 14.4A for the test with V_{DC} 480V and 6A for the test with V_{DC} 200V) and 5% of $I_{C\_NOMINAL}$ (i.e. 0.8A for the test with V_{DC} 480V and 0.333A for the test with V_{DC} 200V). The Fall Time (t_F) includes the current tail period which stands for the time taken to recombine the excess charges stored in N- drift region. The Turn-Off Switching Loss (E_{OFF}) is the amount of total energy lost during turn-off under inductive load. It is the integral, of the power loss waveform (P_{OFF}) for the time interval when the collector-emitter voltage (V_{CE}) begins to rise at 10% V_{DC} (i.e. 48V for the test with V_{DC} 480V and 20V for the test with V_{DC} 200V) to the point where the collector current (I_C) falls to 5% of $I_{C\_NOMINAL}$ (i.e. 0.8A for the test with V_{DC} 480V and 0.333A for the test with V_{DC} 200V). Figure 4.9 shows the turn-off transients of IGBT Sample 14, conducted at a V_{DC} of 480V and test collector current (I_C) of 16A. It highlights the turn-off waveforms when new and after each age iteration. It is important to point out that each tested IGBT exhibited similar changes in their respective turn-off waveforms.

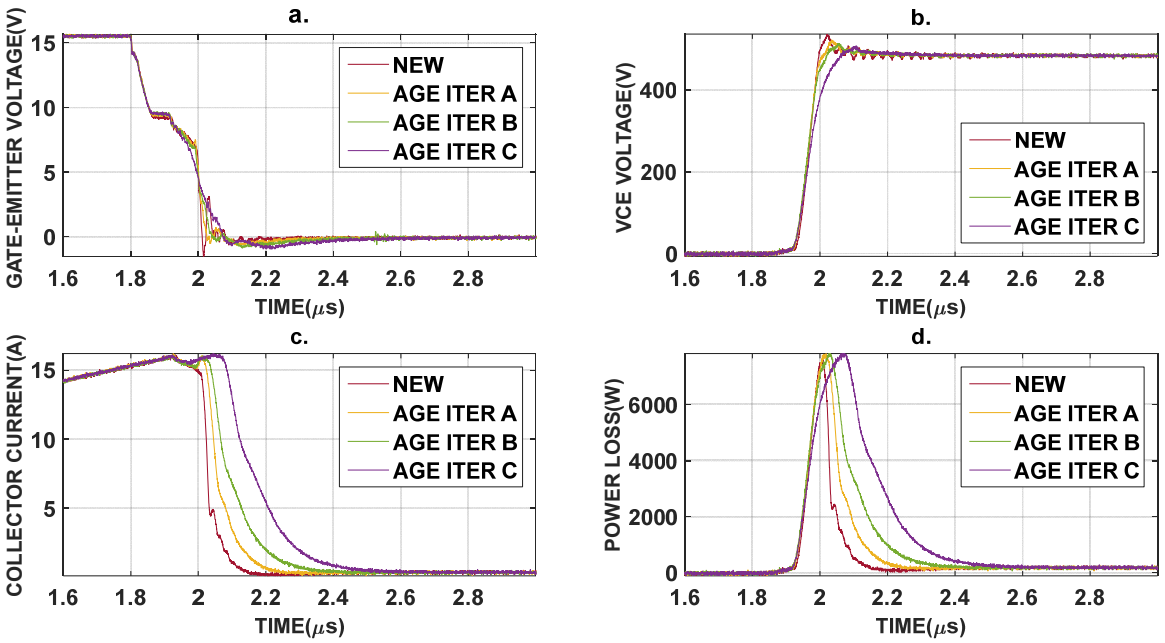


Figure 4.9 - Turn-Off Transients Comparison NEW vs AGED (3 Age Iterations) IGBT Sample 14 with V_{DC} 480V and Case Temperature (T_C) 25°C; (a) Gate-Emitter Voltage (V_{GE}) (b) Collector-Emitter Voltage (V_{CE}) (c) Collector Current (I_C) (d) Power Loss during Turn-Off (P_{OFF})

Figures 4.10 to 4.13 illustrate the turn-off switching parameters evolution, with the implemented accelerated ageing strategy, for each tested IGBT (for the test with V_{DC} at 200V), namely the turn-off delay time (t_{D_OFF}), fall time (t_F), the rate of change of the collector-emitter voltage (dV_{CE}/dt), and the energy loss (E_{OFF}) respectively. Correspondingly, Figures 4.14 to 4.17 illustrate the turn-off switching parameters evolution, but for the IGBTs tested with V_{DC} at 480V. Table 4-2 provides the averages of the turn-off parameters and corresponding standard deviation (σ), when new and after each age iteration. Table 4-3 provides the average percentage variation and corresponding standard deviation (σ), between each age iteration and new. These two tables provide the results for the IGBTs tested with V_{DC} at 200V. Similarly, Table 4-4 and Table 4-5 provide the results for the IGBTs tested with V_{DC} at 480V.

After ageing, tested IGBTs manifested an increase in the fall time of the gate-emitter voltage (V_{GE}) and an increase in the rise time of the collector-emitter voltage (V_{CE}). This led to a significant decrease in the collector-emitter voltage rate of change (dV_{CE}/dt_{OFF}). Moreover, a significant increase in the collector current (I_C) Fall Time (t_F) was observed, with an average percentage increase, after three age iterations, of 300.74% and 267.31%, for the 200V and 480V V_{DC} tests, respectively. This was characterized by an enhanced tail current amplitude and a prolonged tail current duration. Consequently, a longer turn-off power pulse was manifested leading to a significant increase in the energy losses during turn-off (E_{OFF}), with an average percentage increase, after three age iterations, of 416.83% and 269.60%, for the 200V and 480V V_{DC} tests, respectively.

AGE PHASE	IGBTs AVERAGE TURN-OFF PARAMETERS @ V_{DC} 200V							
	TURNOFF TIME (ns)	TURNOFF σ (ns)	FALL TIME (ns)	FALL TIME σ (ns)	TURNOFF SWITCHING LOSS (mJ)	SWITCHING LOSS σ (mJ)	dV_{CE}/dt (V/ns)	σ (V/ns)
NEW	109.32	0.7554	90.16	3.0416	0.03016	0.00071	8.4041	0.43896
AGE A	106.04	1.2285	218.64	52.6021	0.07498	0.02607	6.1318	1.27023
AGE B	105.23	1.3351	309.81	48.2421	0.11897	0.02554	4.1497	0.77867
AGE C	104.64	1.3125	361.04	32.3521	0.15593	0.02053	3.0021	0.47197

Table 4-2 - IGBTs Turn-Off Parameters Average & Standard Deviation Test @ V_{DC} 200V

AGE PHASES COMPARISON	IGBTs AVERAGE PERCENTAGE VARIATION TURN-OFF PARAMETERS @ V_{DC} 200V							
	TURN OFF TIME (%)	σ (%)	FALL TIME (%)	σ (%)	TURN OFF SWITCHING LOSS (%)	σ (%)	dV_{CE}/dt (%)	σ (%)
AGE A WITH NEW	-3.00	1.29	142.74	57.49	148.26	83.72	-27.14	13.80
AGE B WITH NEW	-3.74	1.28	243.68	52.53	294.17	82.10	-50.47	9.68
AGE C WITH NEW	-4.28	1.34	300.74	37.38	416.83	65.15	-64.19	5.87

Table 4-3 - IGBTs Turn-Off Parameters Average & Std. Dev. Percentage Variation @ V_{DC} 200V

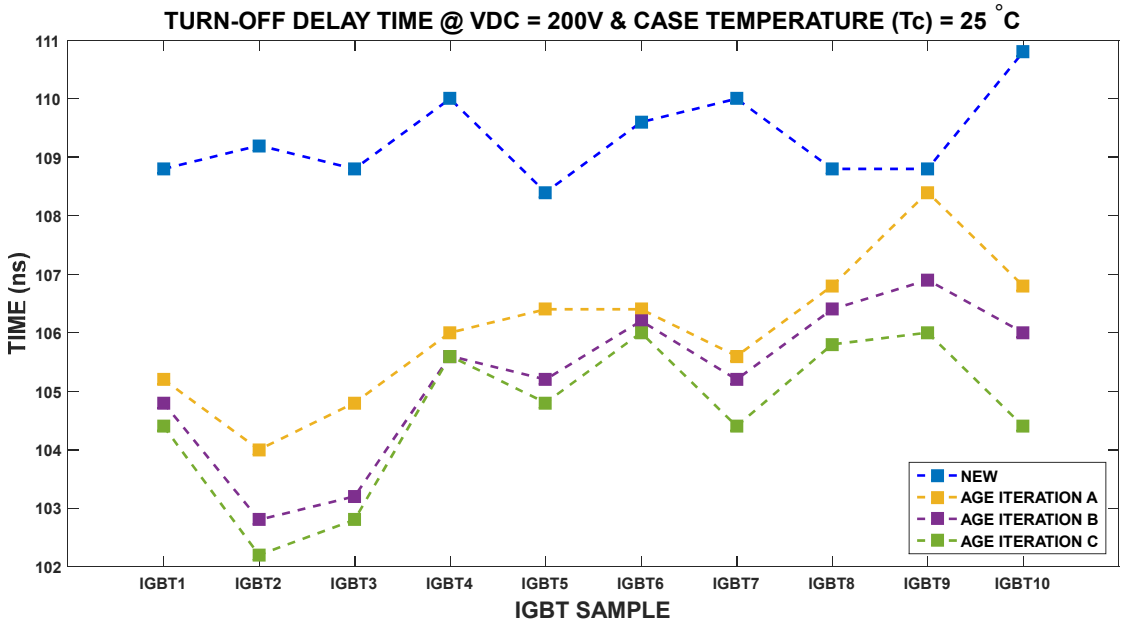


Figure 4.10 – IGBTs' Turn-Off Delay Time with Ageing, at V_{DC} 200V.

The collector-emitter voltage rate of change (dV_{CE}/dt_{OFF}) manifested a decrease, with a corresponding percentage decrease, after three age iterations, of 64.19% and 57.07%, for the 200V and 480V V_{DC} tests, respectively. This contributed to a significant decrease in ringing and overshoot in the collector-emitter voltage (V_{CE}). Marginal changes in the Turn-Off Delay Time (t_{D_OFF}) were observed, with an average percentage decrease, after three age iterations, of 4.28% and 3.57%, for the 200V and 480V V_{DC} tests, respectively.

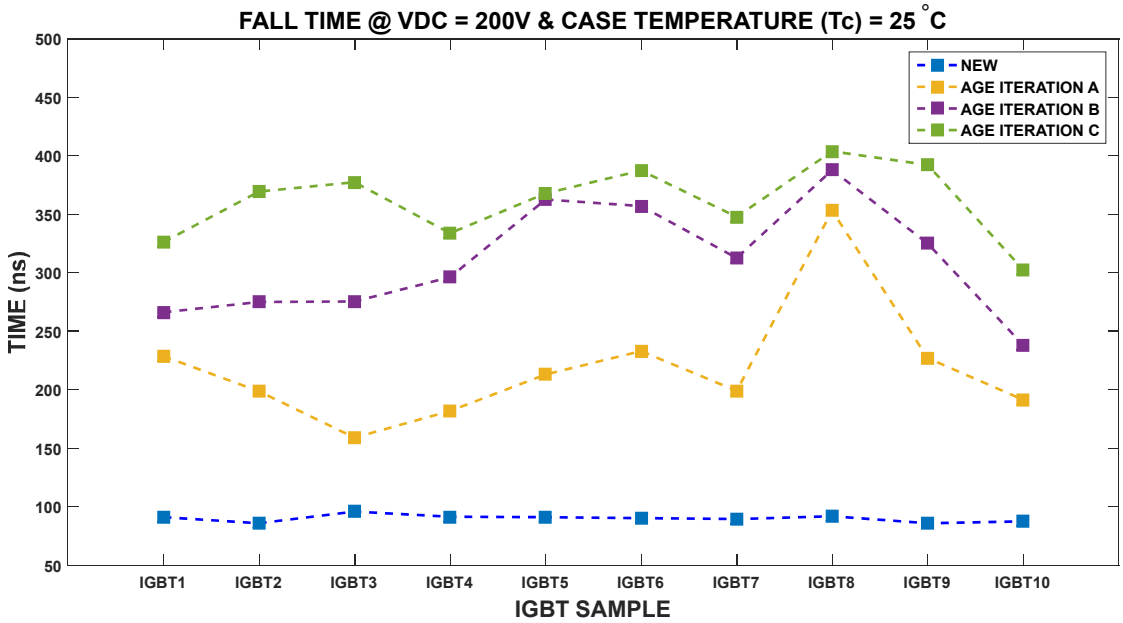


Figure 4.11 – IGBTs' Fall Time with Ageing, test at V_{DC} 200V.

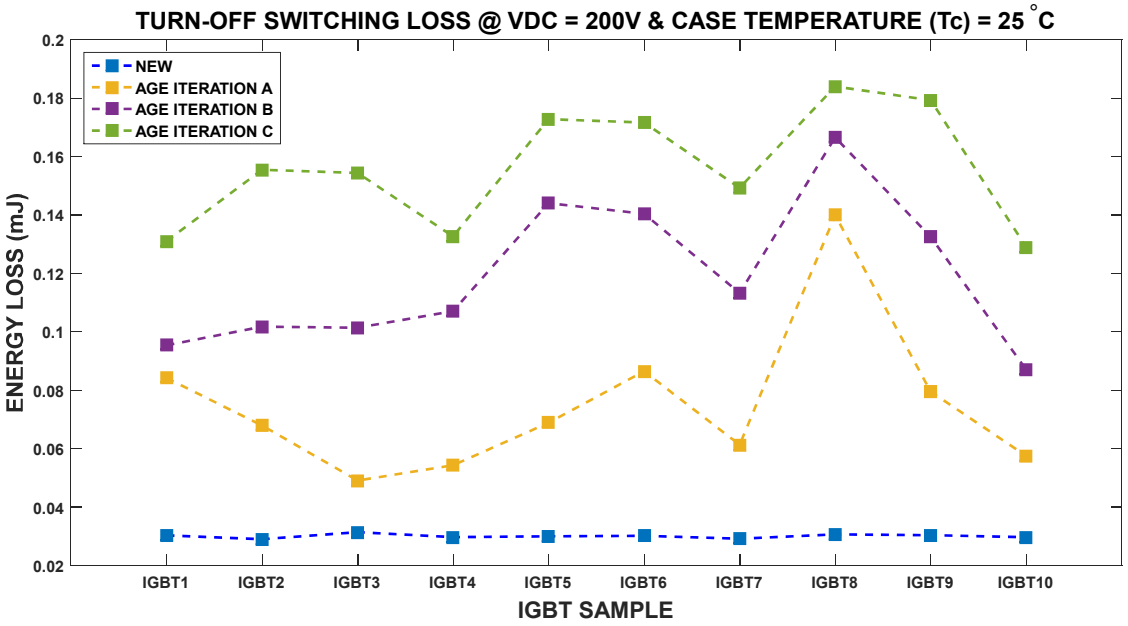


Figure 4.12 – IGBTs' Turn-Off Switching Loss with Ageing, test at V_{DC} 200V.

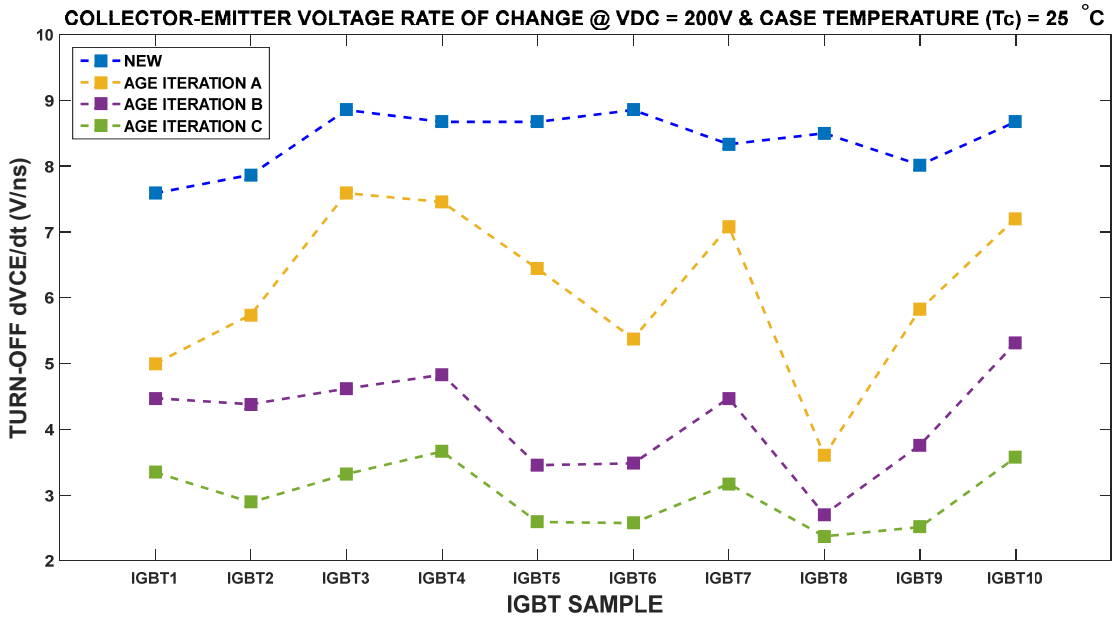


Figure 4.13 – Turn-Off Collector-Emitter Voltage Rate of Change (dV_{CE}/dt) at V_{DC} 200V.

AGE PHASE	IGBTs AVERAGE TURN-OFF PARAMETERS @ V_{DC} 480V							
	TURNOFF DELAY TIME (ns)	σ (ns)	FALL TIME (ns)	σ (ns)	TURNOFF SWITCHING LOSS (mJ)	σ (mJ)	dV_{CE}/dt (V/ns)	σ (V/ns)
NEW	126.22	1.924	95.34	3.557	0.5645	0.0215	7.472	0.1954
AGE A	123.60	2.059	220.8	70.478	1.2631	0.4677	5.284	1.8669
AGE B	127.06	5.344	287.06	72.832	1.6519	0.5877	4.397	1.9622
AGE C	127.08	5.885	348.42	55.006	2.0796	0.5022	3.199	1.2599

Table 4-4 - IGBTs Turn-Off Parameters Average & Standard Deviation Test @ V_{DC} 480V

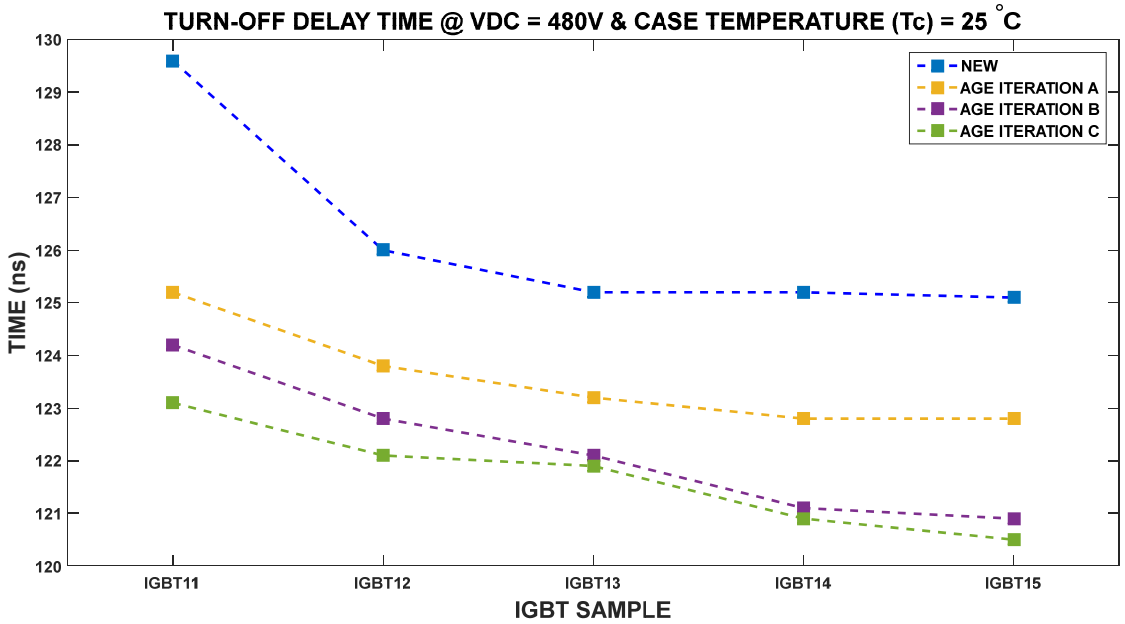


Figure 4.14 – IGBTs' Turn-Off Delay Time with Ageing, at V_{DC} 480V.

AGE PHASES COMPARISON	IGBTs AVERAGE PERCENTAGE VARIATION TURN-OFF PARAMETERS @ V_{DC} 480V							
	TURN OFF DELAY TIME (%)	σ (%)	FALL TIME (%)	σ (%)	TURN OFF SWITCHING LOSS (%)	σ (%)	dV_{CE}/dt (%)	σ (%)
AGE A WITH NEW	-2.10	0.73	133.76	80.71	124.24	82.63	-29.24	25.35
AGE B WITH NEW	-3.16	0.69	202.72	82.39	193.04	103.12	-40.99	26.92
AGE C WITH NEW	-3.57	0.90	267.31	68.97	269.60	93.20	-57.07	17.38

Table 4-5 - IGBTs Turn-Off Parameters Average & Std. Dev. Percentage Variation @ V_{DC} 480V

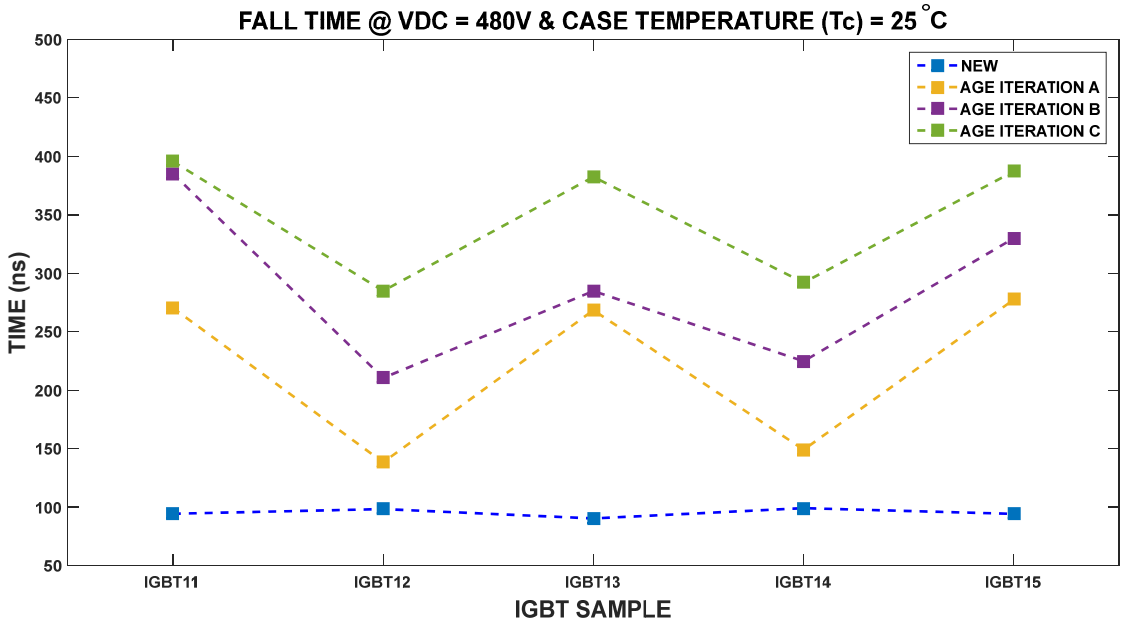


Figure 4.15 – IGBTs' Fall Time with Ageing, test at VDC 480V.

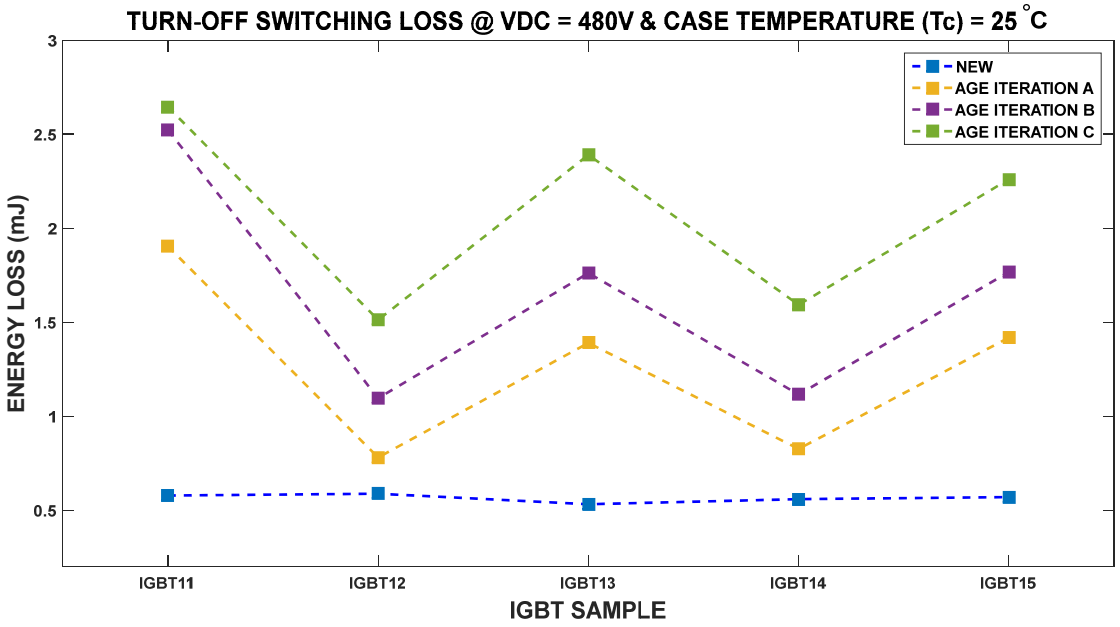


Figure 4.16 – IGBTs' Turn-Off Switching Loss with Ageing, test at V_{DC} 480V.

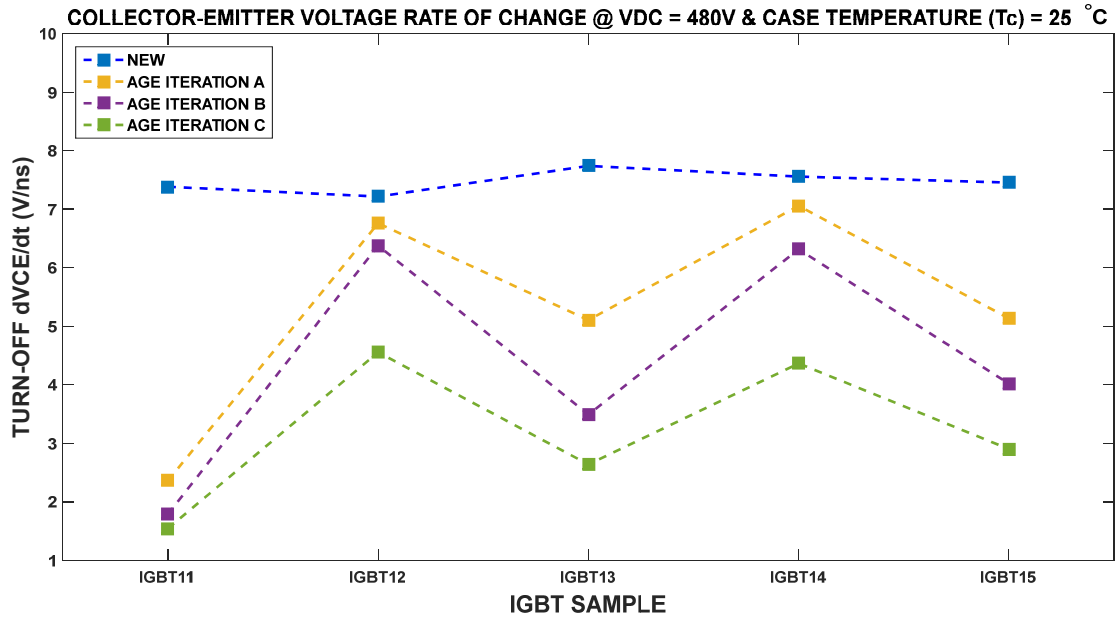


Figure 4.17 – Turn-Off Collector-Emitter Voltage Rate of Change (dV_{CE}/dt_{OFF}) at V_{DC} 480V.

4.5.2 Turn-On Delay Time (t_{D_ON}), Rise-Time (t_R), Turn-On Switching Loss (E_{ON}) and Collector Current Rate of Change during Turn-On (dI_C/dt_{ON})

The Turn-On Delay Time (t_{D_ON}) is the time difference between the points where the gate-emitter voltage (V_{GE}) is at 10% of $V_{GE\_NOMINAL}$ (i.e. 1.5V) and the collector current (I_C) is at 10% of $I_{C\_NOMINAL}$ (i.e. 1.6A for the test with V_{DC} 480V and 0.66A for the test with V_{DC} 200V). During this time, the IGBT's internal surface MOSFET channel, is formed defining the charging speed of the gate. The Rise Time (t_R) is the time difference between the points where

the collector current (I_C) is at 10% of $I_{C\_NOMINAL}$ (i.e. 1.6A for the test with V_{DC} 480V and 0.66A for the test with V_{DC} 200V) and 90% of $I_{C\_NOMINAL}$ (i.e. 14.4A for the test with V_{DC} 480V and 5.94A for the test with V_{DC} 200V). The Rise Time (t_R) is influenced predominantly by the gate characteristics. The Turn-Off Switching Loss (E_{ON}) is the amount of total energy lost during turn-on, under inductive load. It also includes the loss from the diode reverse recovery which is manifested as an overshoot in the collector current (I_C) turn-on waveform. The Turn-On Switching Loss (E_{ON}) is the integral of the power loss waveform (P_{ON}) from the point where the collector current (I_C) begins to flow at 10% $I_{C\_NOMINAL}$ (i.e. 1.6A for the test with V_{DC} 480V and 0.66A for the test with V_{DC} 200V) to the point where the collector-emitter voltage falls to 5% of $V_{CE\_NOMINAL}$ (i.e. 24V for the test with V_{DC} 480V and 10V for the test with V_{DC} 200V). Figure 4.18 shows the turn-on waveforms of IGBT Sample 14 when new and after three age iterations. It is important to highlight the fact that each tested IGBT exhibited similar changes in their respective turn-off waveforms. Figures 4.19 to 4.22 illustrate the turn-on switching parameters evolution, with the implemented accelerated ageing strategy, for each tested IGBT (for the test with V_{DC} at 200V), namely the turn-on delay time (t_{D_ON}), rise time (t_R), the rate of change of the collector current (dI_C/dt_{ON}), and the energy loss (E_{ON}) respectively. Correspondingly, Figures 4.23 to 4.26 illustrate the turn-on switching parameters evolution, for the IGBTs tested with V_{DC} at 480V.

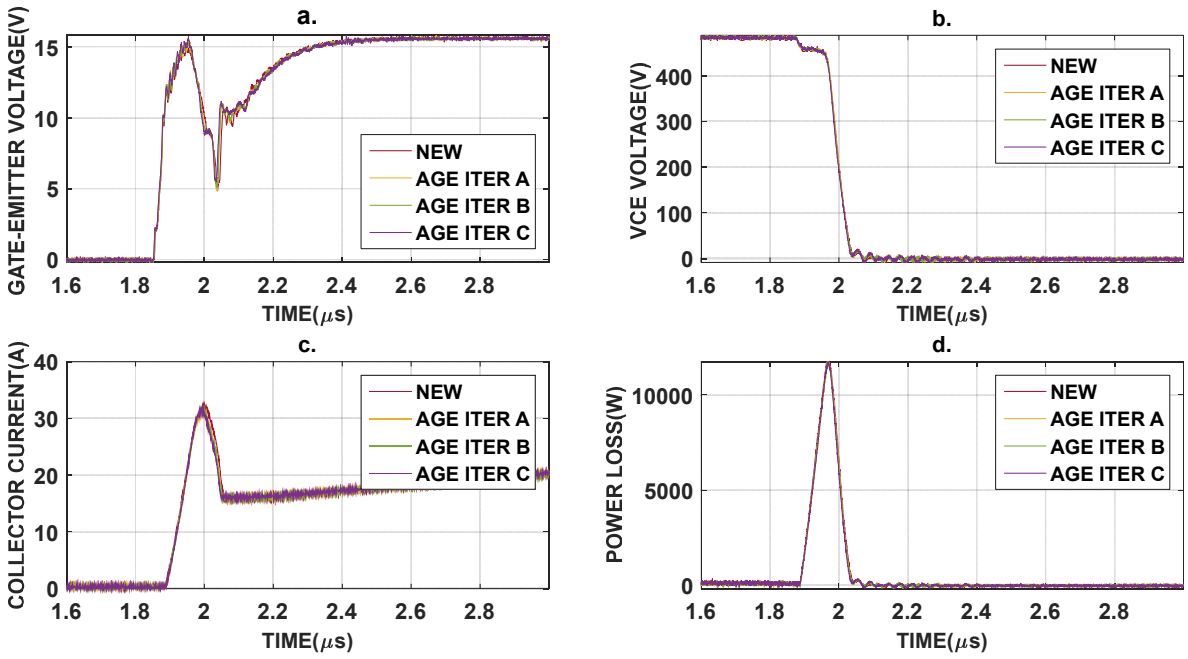


Figure 4.18 - Turn-On Transients Comparison NEW vs AGED (3 Age Iterations) IGBT14 with V_{DC} 480V and Case Temperature (T_C) 25°C; (a) Gate-Emitter Voltage (V_{GE}) (b) Collector-Emitter Voltage (V_{CE}) (c) Collector Current (I_C) (d) Power Loss during Turn-Off (P_{ON}).

AGE PHASE	IGBTs AVERAGE TURN-ON PARAMETERS @ V_{DC} 200V							
	TURNON TIME (ns)	TURNON σ (ns)	RISE TIME (ns)	RISE TIME σ (ns)	TURNON SWITCHING LOSS (mJ)	SWITCHING LOSS σ (mJ)	dI_C/dt_{ON} (A/ns)	σ (A/ns)
NEW	30.92	0.5350	10.60	0.5497	0.0342	0.0007	0.3915	0.0207
AGE A	31.71	0.4533	11.19	0.4725	0.0348	0.0007	0.3706	0.0157
AGE B	32.22	0.3327	11.55	0.4223	0.0353	0.0007	0.3589	0.0132
AGE C	32.66	0.3777	11.84	0.3134	0.0357	0.0008	0.3499	0.0092

Table 4-6 - IGBTs Turn-On Parameters Average & Standard Deviation Test @ V_{DC} 200V

Table 4-6 provides the average turn-on parameters and corresponding standard deviation (σ), when new and after each age iteration. Table 4-7 provides the average percentage variation and corresponding standard deviation (σ), between each age iteration and new. These two tables provide the results for the IGBTs tested with V_{DC} at 200V. Similarly, Table 4-8 and Table 4-9 provide the results for the IGBTs tested with V_{DC} at 480V. After ageing, tested IGBTs manifested marginal change in the rise-time of the gate-emitter voltage (V_{GE}). Correspondingly a marginal increase in the Turn-On Delay Time (t_{D_ON}) was observed, with an average percentage increase, after three age iterations, of 5.646% and 5.269%, for the 200V and 480V V_{DC} tests, respectively. The collector current (I_C) rise-time (t_R) manifested a marginal increase when compared to the more severe changes in the fall-time (t_F), observed in the turn-off transients, with an average percentage increase, after three age iterations, of 11.963% and 5.223%, for the 200V and 480V V_{DC} tests, respectively.

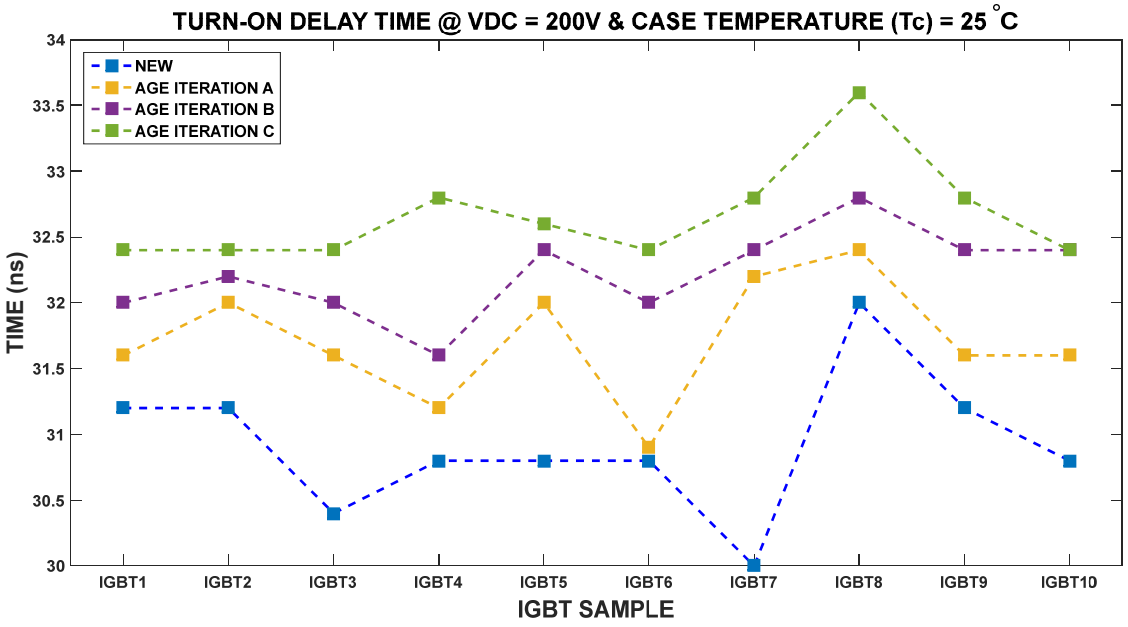


Figure 4.19 – IGBTs' Turn-On Delay Time with Ageing, at V_{DC} 200V.

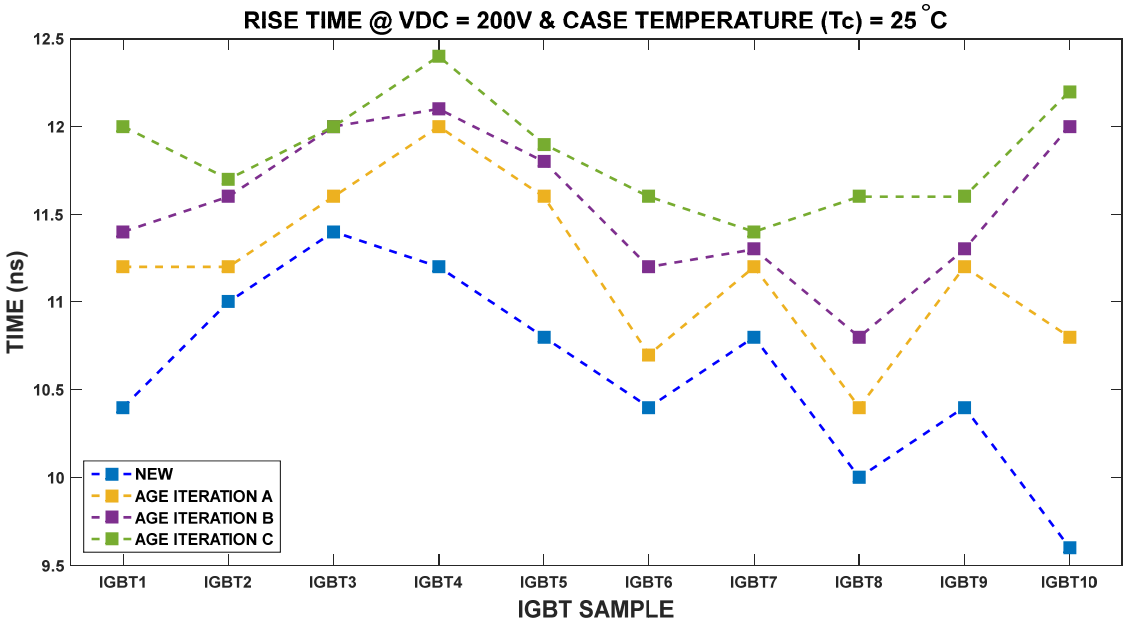


Figure 4.20 – IGBTs' Rise-Time with Ageing, at V_{DC} 200V.

AGE PHASES COMPARISON	IGBTs AVERAGE PERCENTAGE VARIATION TURN-OFF PARAMETERS @ V_{DC} 200V							
	TURN ON TIME (%)	σ (%)	RISE TIME (%)	σ (%)	TURN ON SWITCHING LOSS (%)	σ (%)	dI_C/dt_{ON} (%)	σ (%)
AGE A WITH NEW	2.5776	2.0565	5.6596	3.2342	1.5932	1.1072	-5.2691	3.0081
AGE B WITH NEW	4.2262	1.7283	9.1604	5.8270	3.3400	1.5115	-8.1797	4.4181
AGE C WITH NEW	5.6460	1.5098	11.9627	6.4894	4.4820	1.6708	-10.4295	4.9000

Table 4-7 - IGBTs Turn-On Parameters Average & Std. Dev. Percentage Variation @ V_{DC} 200V

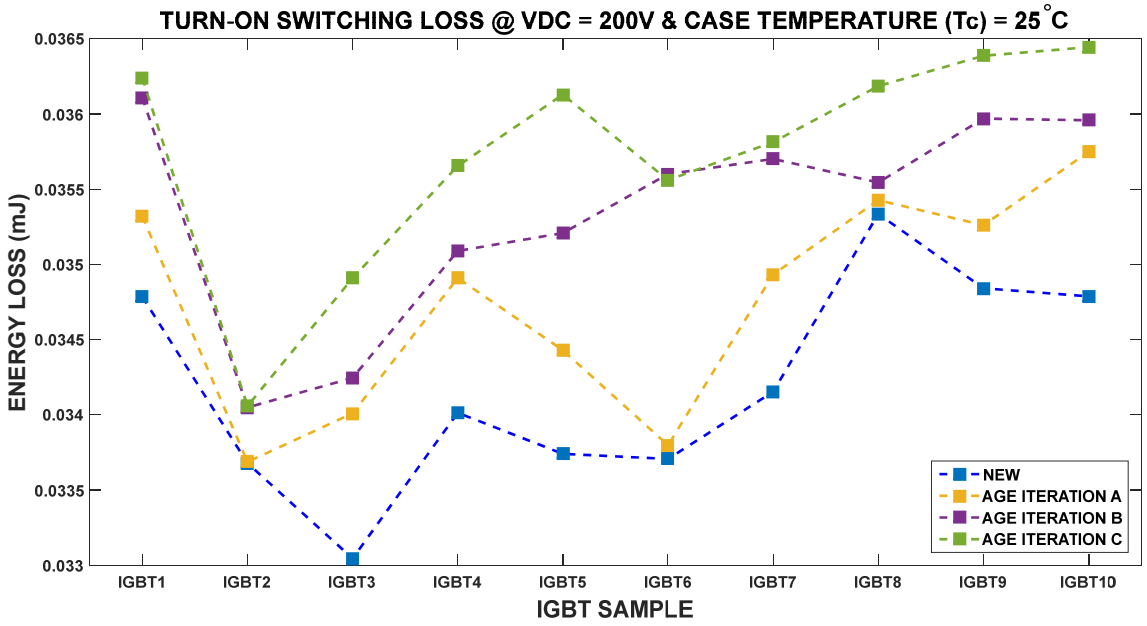


Figure 4.21 – IGBTs' Turn-On Switching Loss with Ageing, test at V_{DC} 200V.

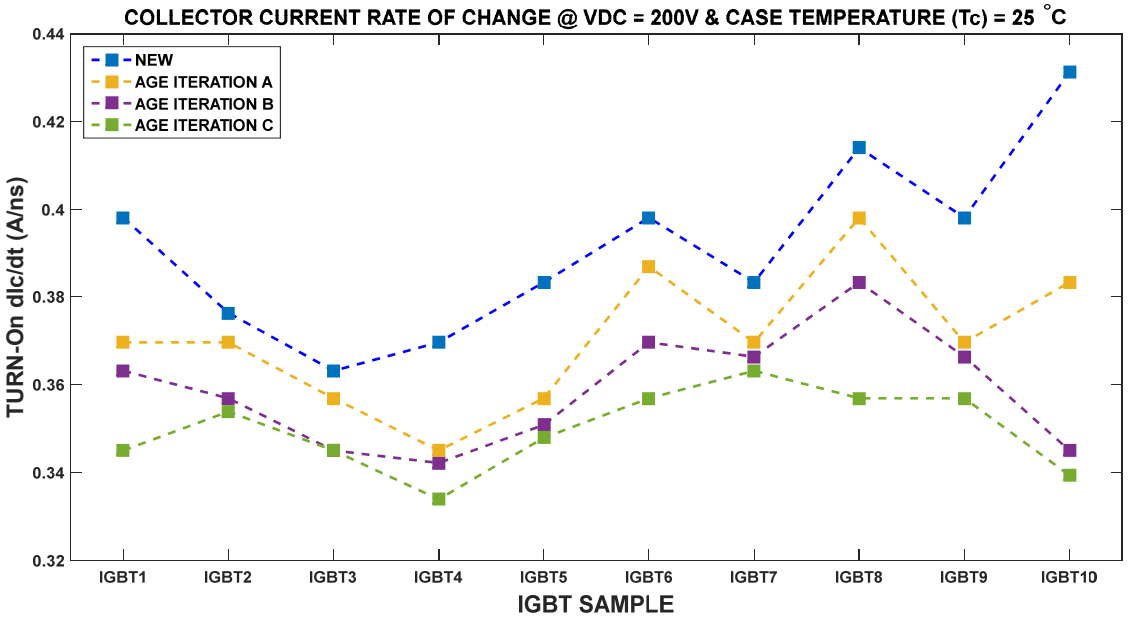


Figure 4.22 – IGBTs' Turn-On Collector Current Rate of Change (dI_C/dt_{ON}) at V_{DC} 200V.

The marginal increase in the turn-on, rise time (t_R), lead to a marginal decrease in the rate of rise of collector current (dI_c/dt_{ON}) with a 10.429% and 5.396%, for the 200V and 480V V_{DC} tests, respectively. The minor decrease observed in the rate of rise of collector current (dI_c/dt_{ON}), contributed to minor reduction in the peak collector current (I_C) overshoot. This is understandable as this overshoot is dependent on the rate of rise of collector current (dI_c/dt_{ON}), contributing to the reverse recovery current of the internal diode of $IGBT_{S1}$ (refer Figure 4.1), which during the different samples characterization, the same new IGBT was retained. Due to the above, there was a minimal increase in turn-on power pulse duration leading to a marginal increase in the energy losses during turn-on (E_{ON}), with a 4.482% and 3.807%, for the 200V and 480V V_{DC} tests, respectively. Hence the utilized accelerated ageing strategy produced marginal changes in the IGBTs turn-on waveforms and parameters, when compared to the more drastic changes observed during the turn-off transients.

AGE PHASE	IGBTs AVERAGE TURN-ON PARAMETERS @ V_{DC} 480V							
	TURNON TIME (ns)	TURNON σ (ns)	RISE TIME (ns)	RISE TIME σ (ns)	TURNON SWITCHING LOSS (mJ)	SWITCHING LOSS σ (mJ)	dI_C/dt_{ON} (A/ns)	σ (A/ns)
NEW	35.36	0.456	38.16	0.607	0.8750	0.0230	0.3355	0.005
AGE A	37.04	1.043	39.52	0.593	0.8951	0.0224	0.3239	0.005
AGE B	37.52	0.756	40.18	0.390	0.9011	0.0241	0.3184	0.003
AGE C	37.78	0.920	40.34	0.351	0.9082	0.0273	0.3173	0.003

Table 4-8 - IGBTs Turn-On Parameters Average & Standard Deviation Test @ V_{DC} 480V

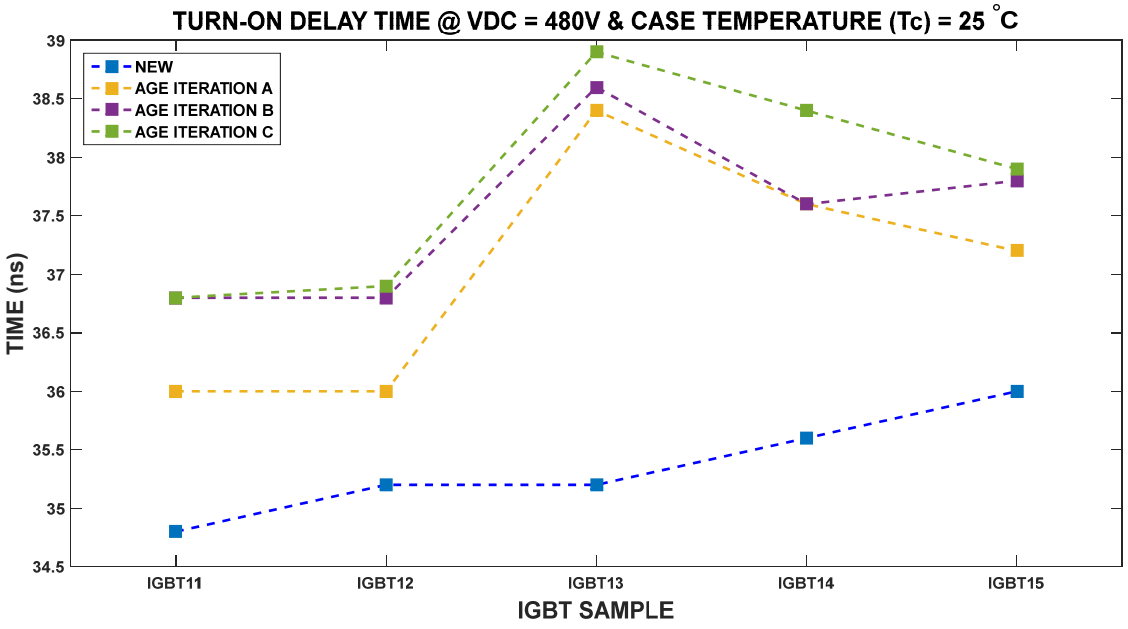


Figure 4.23 – IGBTs' Turn-On Delay Time with Ageing, at V_{DC} 480V.

AGE PHASES COMPARISON	IGBTs AVERAGE PERCENTAGE VARIATION TURN-OFF PARAMETERS @ V_{DC} 480V							
	TURN ON TIME (%)	σ (%)	RISE TIME (%)	σ (%)	TURN ON SWITCHING LOSS (%)	σ (%)	dI_C/dt_{ON} (%)	σ (%)
AGE A WITH NEW	4.7526	2.7127	3.5796	1.9311	2.3092	1.6856	-3.4291	1.7965
AGE B WITH NEW	4.9902	1.7441	5.0067	2.2666	3.0048	2.1544	-5.0651	2.2290
AGE C WITH NEW	5.2693	2.2986	5.2232	2.9490	3.8069	2.2266	-5.3960	2.1179

Table 4-9 – IGBTs Turn-On Parameters Average & Std. Dev. Percentage Variation @ V_{DC} 480V

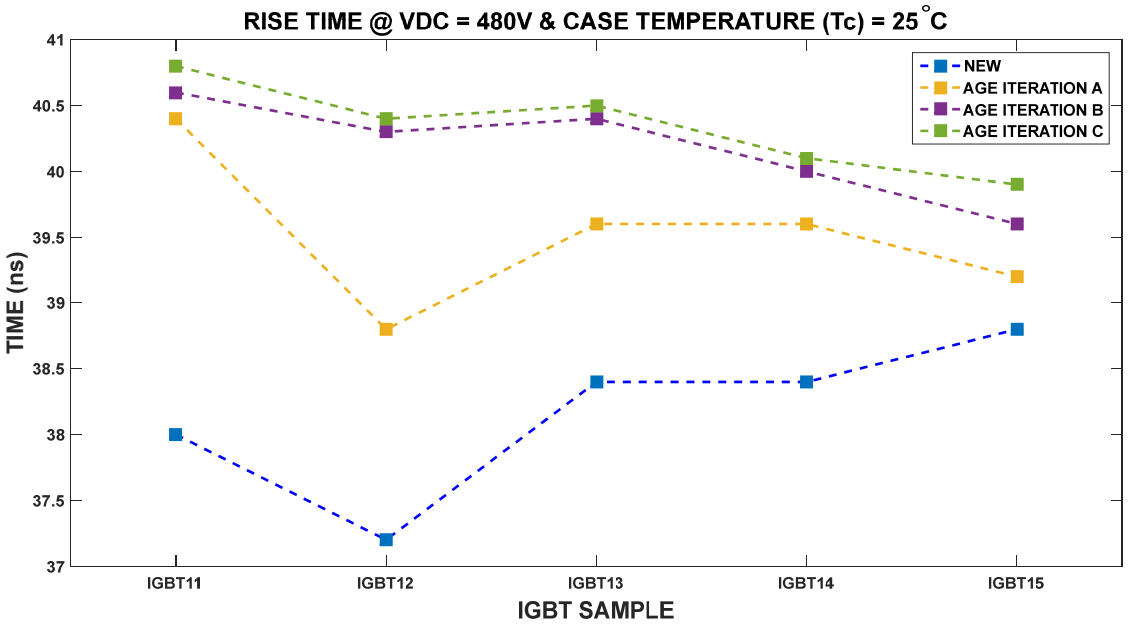


Figure 4.24 – IGBTs' Rise-Time with Ageing, at V_{DC} 480V.

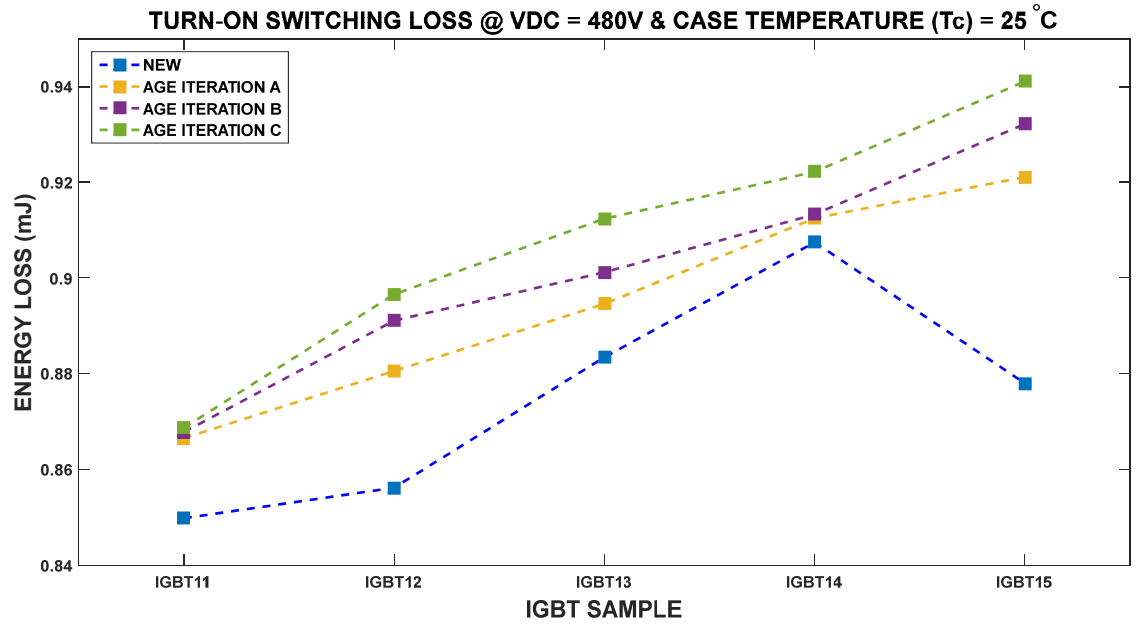


Figure 4.25 - IGBTs' Turn-On Switching Loss with Ageing, test at V_{DC} 480V.

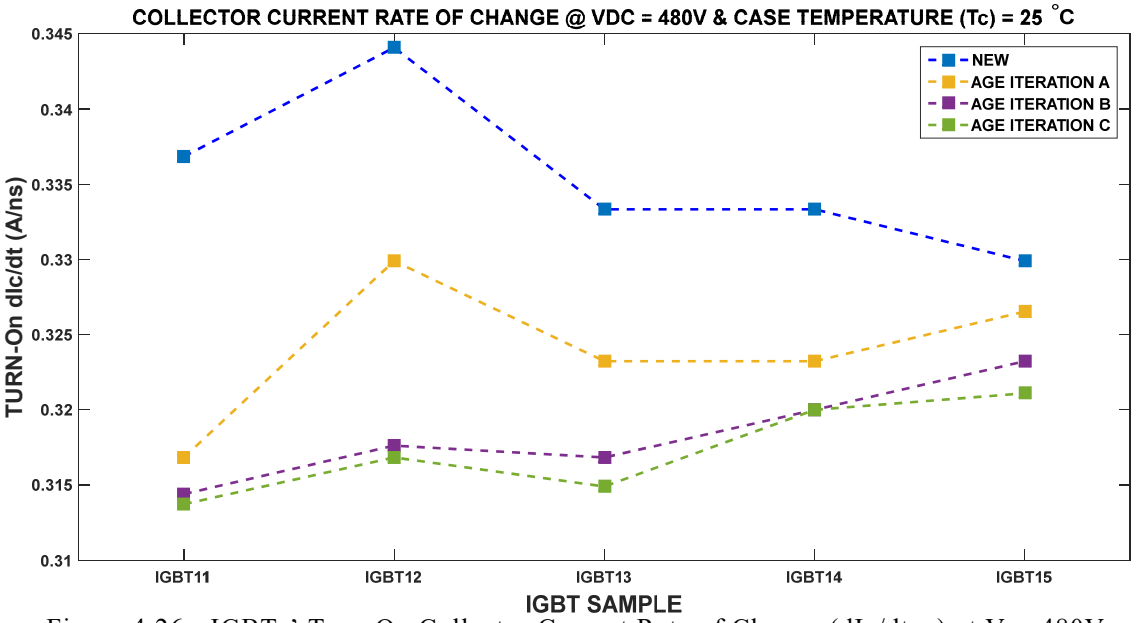


Figure 4.26 - IGBTs' Turn-On Collector Current Rate of Change (dI_C/dt_{ON}) at V_{DC} 480V.

4.5.3 IGBT's Internal Diode Reverse Recovery Time (t_{RR}), Internal Diode Peak Reverse Recovery Current (I_{PRR})

When a diode is suddenly switched from a forward conduction state to a blocking state, an initial current flow will happen in the reverse direction. This happens because the diode requires a finite amount of time before the excess minority carriers in the P and N region recombine. This time is known as Reverse Recovery Time (t_{RR}). Since the IGBT has an internal free-wheeling diode, it also experiences reverse recovery current (I_{RR}). Generally, this internal free-wheeling diode is slow and hence it has a long reverse recovery time (t_{RR}) and large peak reverse recovery current (I_{PRR}).

When the utilized double pulse test circuit was configured as shown in Figure 4.1(a), for turn-on and turn-off characterization, reverse recovery current will manifest during the turn-on transition. When $IGBT_{S2}$ is switched off, the internal free-wheeling diode of $IGBT_{S1}$ is circulating the inductor current, hence it is forward biased. On turn-on, $IGBT_{S2}$ is switched on, and the inductor current starts to flow through it. But since the internal free-wheeling diode of $IGBT_{S1}$ requires the reverse recovery time (t_{RR}) to go into reverse blocking mode, $IGBT_{S2}$ will experience the combined inductor current and the reverse recovery current. This will manifest itself as an overshoot in the collector current (I_C) of $IGBT_{S2}$. This is shown in Figure 4.18(c). During reverse recovery characterization, the DUT was set to be $IGBT_{S2}$. Hence the circuit was configured as shown in Figure 4.1 (b). With this configuration, reverse recovery changes in the internal free-wheeling diode of the aged IGBTs could be determined. Figure 4.27 shows the recovery waveforms of the internal diode of IGBT Sample 12 and the corresponding power loss during reverse recovery, conducted when the IGBT was new and after each age iteration. The test reverse voltage (V_R) was set to 200V DC, corresponding to the final reverse voltage depicted in Figure 4.27(a), while the test forward current (I_F) was set to 12A which is the starting current depicted in Figure 4.27(b).

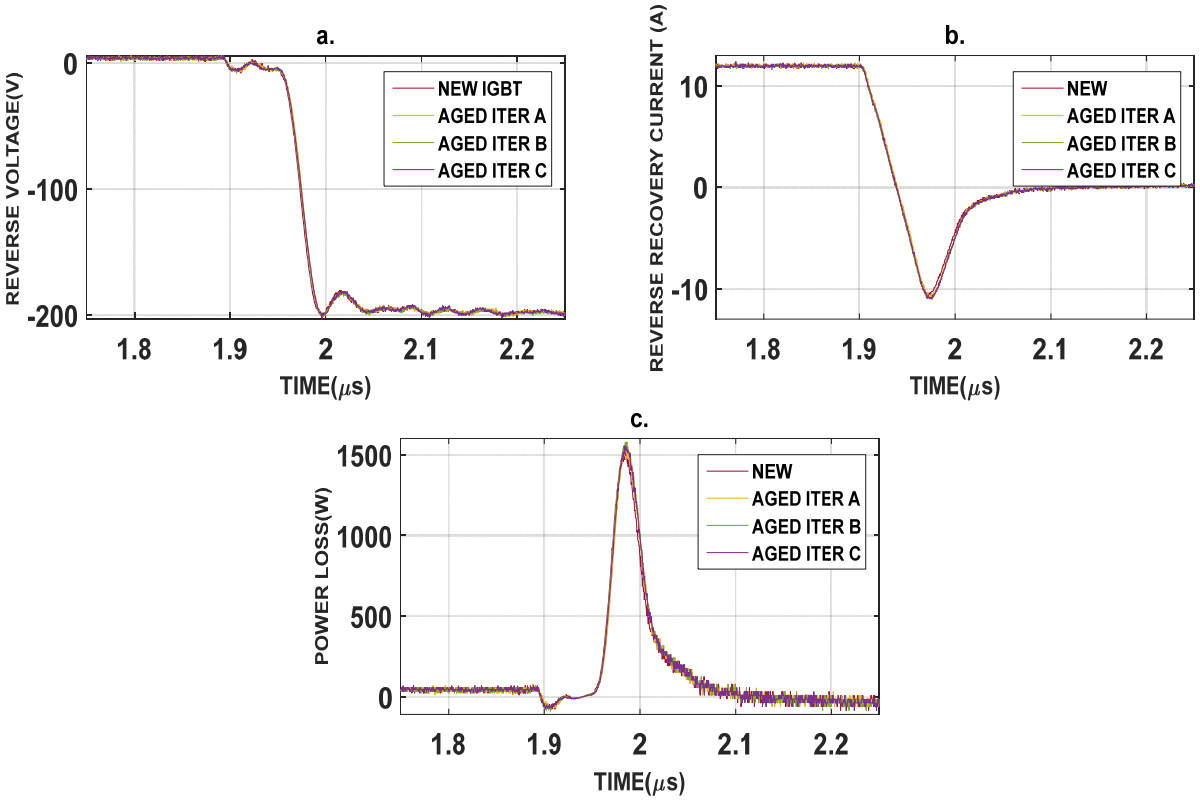


Figure 4.27 – Reverse Recovery Transients Comparison NEW vs AGED (3 Age Iterations) IGBT Sample 12 with V_{RR} 200V, Forward Current (I_F) 12A and Case Temperature (T_C) 25°C; (a) Reverse Voltage (V_{RR}) (b) Reverse Recovery Current (I_{RR}) (c) Power Loss during Reverse Recovery (P_{RR}).

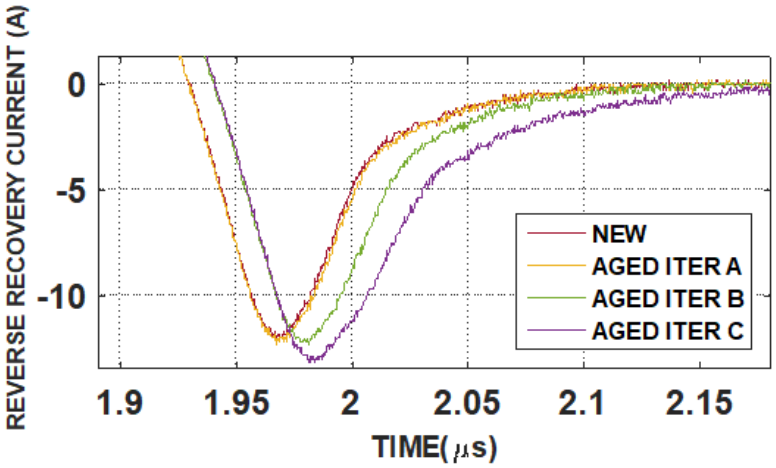


Figure 4.28 - Reverse Recovery Current (I_{RR}) Transient Comparison NEW vs AGED (3 Age Iterations) IGBT Sample 11 zoomed-in to highlight the evolution of the peak reverse recovery current (I_{PRR}) evolution with ageing.

In relation to the reverse recovery current (I_{RR}), the reverse recovery time (t_{RR}) is defined as the time between the free-wheeling diode's current zero-crossing to when the current returns within 10% of the peak reverse recovery current (I_{PRR}), where this latter parameter corresponds to the minimum current of the reverse recovery current plot depicted in Figure 4.27(b). Figures 4.29 to 4.31 show the changes in the reverse recovery parameters of tested IGBTs, before and after each accelerated ageing iteration. Figure 4.29 shows that after ageing, there was a general increase in the Reverse Recovery Time (t_{RR}).

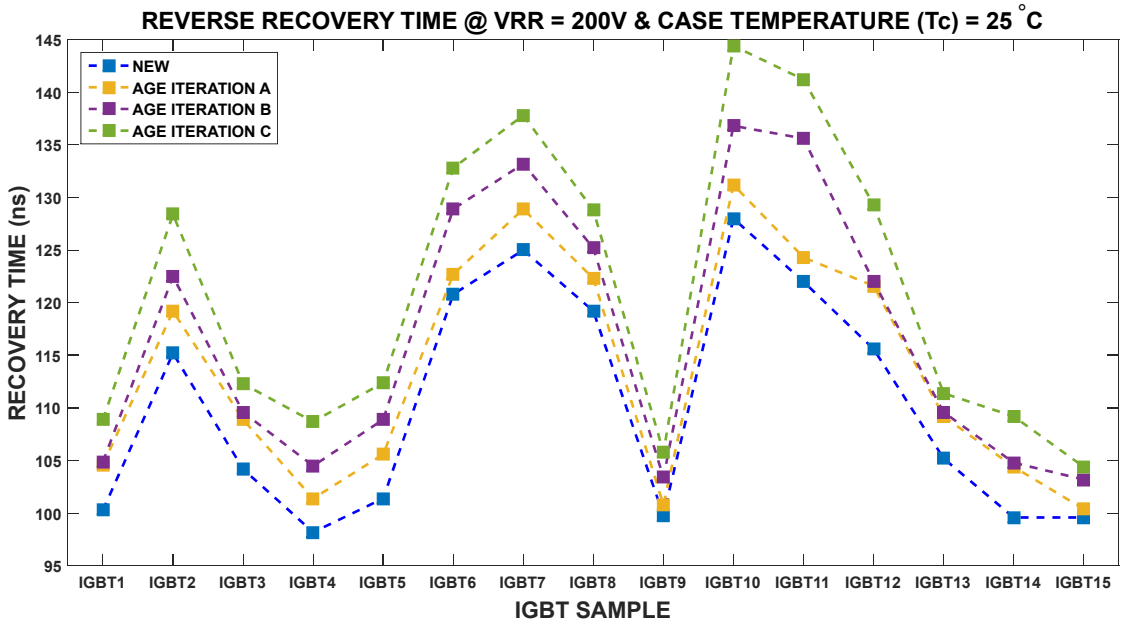


Figure 4.29 - IGBTs' Internal Diode Reverse Recovery Time (t_{RR}) evolution with Ageing, with Reverse Voltage (V_{RR}) 200V, Forward Current (I_F) 12A and Case Temperature (T_C) 25°C

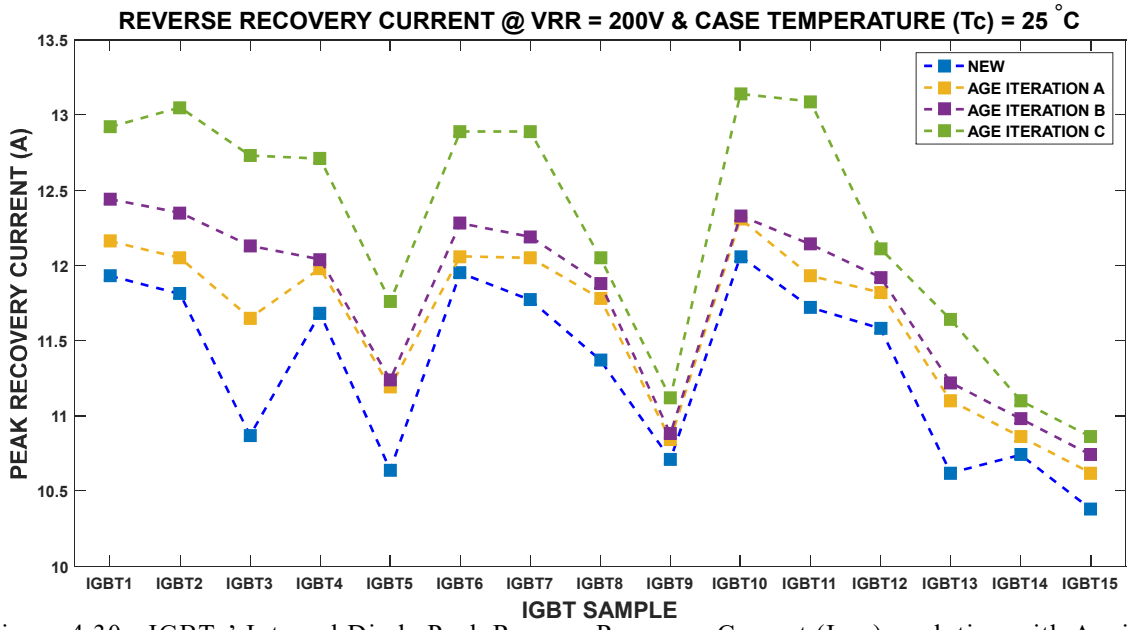


Figure 4.30 - IGBTs' Internal Diode Peak Reverse Recovery Current (I_{PRR}) evolution with Ageing, with Reverse Voltage (V_{RR}) 200V, Forward Current (I_F) 12A and Case Temperature (T_C) 25°C

The same trend was noticed in the Peak Reverse Recovery Current (I_{PRR}) as evidenced in Figure 4.30. Since these two parameters vary significantly with temperature, characterization was conducted with the DUT case temperature (T_C) set at 25°C. Table 4-10 provides the average reverse recovery parameters and corresponding standard deviation (σ), when new and after each age iteration. Table 4-11 provides the average percentage variation and corresponding standard deviation (σ), between each age iteration and new. After ageing, tested IGBTs manifested an increase in the reverse recovery time, with an average percentage increase, after three age iterations, of 9.623%. The peak reverse recovery current (I_{PRR}) manifested an increase too, with an average percentage increase, after three age iterations, of 8.35%. The increase in these two parameters led to an increase in the energy loss during reverse recovery, with an average percentage increase after three age iterations, of 10.55%.

AGE PHASE	IGBTs AVERAGE REVERSE RECOVERY PARAMETERS @ V_{RR} 200V					
	Reverse Recovery Time (ns)	Reverse Recovery σ (ns)	Peak Reverse Recovery Current (A)	Peak Reverse Recovery σ (A)	Energy Loss Recovery (mJ)	Energy Loss Recovery σ (mJ)
NEW	110.27	10.81	11.32	0.589	0.0654	0.00963
AGE A	113.71	10.92	11.63	0.552	0.0673	0.00958
AGE B	116.87	12.72	11.78	0.596	0.0693	0.00962
AGE C	121.05	14.01	12.27	0.805	0.0722	0.01049

Table 4-10 - IGBTs Reverse Recovery Parameters Average & Standard Deviation Test @ V_{RR} 200V.

AGE PHASES COMPARISON	IGBTs AVERAGE PERCENTAGE VARIATION REVERSE RECOVERY PARAMETERS @ V_{RR} 200V					
	Reverse Recovery Time (%)	Reverse Recovery σ (%)	Peak Recovery Current (%)	Peak Reverse Recovery σ (%)	Energy Loss Recovery (%)	Energy Loss Recovery σ (%)
AGE A WITH NEW	3.1311	1.3770	2.7253	1.7125	3.0235	2.3131
AGE B WITH NEW	5.8933	1.8762	4.1116	2.3857	6.0972	2.1452
AGE C WITH NEW	9.6226	2.8788	8.3498	3.5875	10.551	5.2991

Table 4-11 - Reverse Recovery Parameters Avg. & Std. Dev. Percentage Variation @ V_{RR} 200V.

The reverse recovery time (t_{RR}), and the peak reverse recovery current (I_{PRR}), are both dependent on the rate of fall of the diode's Forward Current (dI_F/dt). This is the rate of current drop from the initial diode's forward current until it reaches the Peak Reverse Recovery Current (I_{PRR}). The rate of fall of forward current (dI_F/dt) is not predominantly dependent on the diode per se but is mainly dependent on the reverse voltage and the circuit's stray inductances [1],[4]. Hence, for the same diode, same reverse voltage, but smaller stray inductances, the rate of fall of recovery will be higher. For the tested IGBTs, the reverse recovery time (t_{RR}) is inversely proportional with rate of fall of forward current (dI_F/dt). On the other hand, the Peak Reverse Recovery Current (I_{PRR}) is proportional with the Rate of Fall of Forward Current (dI_F/dt). This will be explained in further detail in Chapter 5. During characterization both the reverse test voltage as well as the circuit (hence the stray inductances, excluding some variation in the soldering/connection inductance), were kept constant utilizing rigorously same hardware and test procedure, to ensure that characterization results of the Reverse Recovery Time (t_{RR}) and Peak Reverse Recovery Current (I_{RR}) are as independent from this parameter.

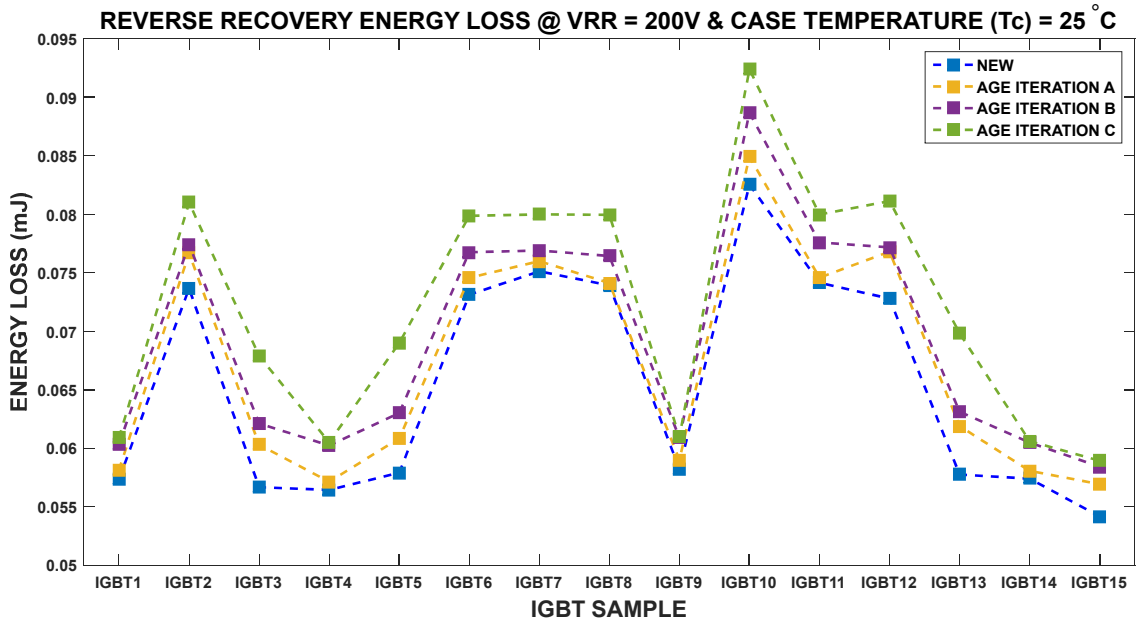


Figure 4.31 - IGBTs' Internal Diode Energy Loss during Reverse Recovery (E_{RR}) with Ageing, with Reverse Voltage (V_{RR}) 200V, Forward Current (I_F) 12A and Case Temperature (T_C) 25°C.

AGE PHASE	IGBTs AVERAGE REVERSE RECOVERY dI_F/dt @ V_{RR} 200V & I_F 12A	
	RATE OF FALL FORWARD CURRENT(A/µs)	STANDARD DEVIATION σ (A/µs)
NEW	323.54	0.9929
AGE ITERATION A	324.67	1.4781
AGE ITERATION B	326.49	1.3902
AGE ITERATION C	326.71	1.4318

Table 4-12 - IGBTs Average Rate of Fall of Current (dI_F/dt) & σ Evolution with Ageing

All tested IGBTs' rate of fall of forward current (dI_F/dt) was measured before and after each age iteration. The resultant average parameters and corresponding standard deviation (σ) are tabulated in Table 4-12. The corresponding percentage variation and corresponding standard deviation (σ) between each age iteration and new are tabulated in Table 4-13. After ageing, tested IGBTs manifested a marginal increase in the reverse recovery rate of fall of forward current (dI_F/dt), with an average percentage increase, after three age iterations, of 1.084%. This indicates that the rate of fall of current remained relatively constant and the changes observed are within possible measurement errors.

This means that the observed increases in the reverse recovery time (t_{RR}) and peak reverse recovery current (I_{PRR}) are relatively independent of the rate of fall of forward current (dI_F/dt). Hence, the changes are mainly contributed by the die-attach degradation of the internal free-wheeling diode section, which effects the thermal impedance of the diode's PN junction, which leads to a higher charge carrier concentration when the diode is forward biased. This increases the minority carriers' concentration and hence presence lifetime during reverse-biasing, thus explaining the increase in the Peak Reverse Recovery Current (I_{PRR}) and the Reverse Recovery Time (t_{RR}).

AGE PHASES COMPARISON	IGBTs AVERAGE PERCENTAGE VARIATION dI_F/dt @ V_{RR} 200V & I_F 12A	
	PERCENTAGE VARIATION (%)	STANDARD DEVIATION σ (%)
AGE A WITH NEW	0.3475	0.3645
AGE B WITH NEW	1.0027	0.5923
AGE C WITH NEW	1.0841	0.3186

Table 4-13 - IGBTs Average Rate of Fall of Current (dI_F/dt) & σ, Percentage Variation with Ageing

4.6 IGBTs Switching Parameters Ageing Evolution for a different IGBT Model.

The above results showed that the implemented accelerated ageing drastically altered the turn-off transient of the tested IGBTs and hence the corresponding turn-off parameters. On the other side the turn-on transient and the corresponding turn-on parameters were minimally impacted when compared to the turn-off. Hence it was decided to confirm that the monitored changes are not exclusive to the utilized IGBT model but manifest too in another IGBT model. For this purpose, the same accelerated ageing procedure and switching parameters characterization were utilized with an IGBT with similar capabilities, as the one tested and characterized above, but from a different manufacturer. Hence the STGP19NC60KD, TO-220, 600V, 20A CO-PACK, IGBT from ST Microelectronics was utilized for this purpose. A test-run of eight IGBTs was conducted with five IGBTs surviving the full pre-established three age iterations.

4.6.1 Turn-Off Delay Time (t_{D_OFF}), Fall-Time (t_F), Turn-On Switching Loss (E_{OFF}) and Collector-Emitter Voltage Rate of Change during Turn-Off (dV_{CE}/dt_{OFF})

Figure 4.32 shows the turn-off transients of IGBT Sample 1 of this test run, conducted at a V_{DC} of 480V and test collector current (I_C) of 16A. It highlights the turn-off waveforms when new and after each age iteration. It is important to point out that each tested IGBT exhibited similar changes in their respective turn-off waveforms. Table 4-14 provides the averages of the,

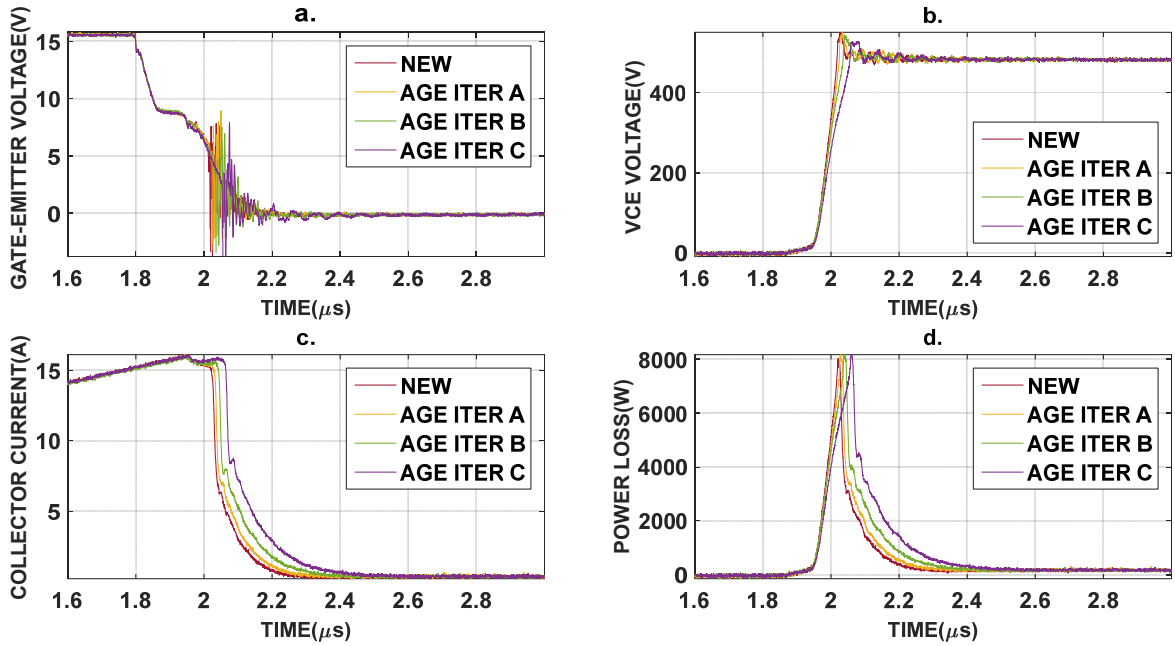


Figure 4.32 - Turn-Off Transients Comparison NEW vs AGED (3 Age Iterations) IGBT STGP19NC60KD Sample 1 with V_{DC} 480V and Case Temperature (T_C) 25°C; (a) Gate-Emitter Voltage (V_{GE}) (b) Collector-Emitter Voltage (V_{CE}) (c) Collector Current (I_C) (d) Power Loss during Turn-Off (P_{OFF}).

AGE PHASE	IGBTs AVERAGE TURN-OFF PARAMETERS @ V_{DC} 200V							
	TURNOFF TIME (ns)	TURNOFF σ (ns)	FALL TIME (ns)	FALL TIME σ (ns)	TURNOFF SWITCHING LOSS (mJ)	SWITCHING LOSS σ (mJ)	dV_{CE}/dt (V/ns)	σ (V/ns)
NEW	146.53	2.203	154.67	5.312	0.5547	0.02875	7.2114	0.35103
AGE A	150.13	2.411	214.11	12.477	0.7239	0.07519	6.2038	0.30393
AGE B	156.27	1.617	263.07	11.209	0.9176	0.10145	5.0574	0.49650
AGE C	167.81	5.556	284.21	33.093	1.0739	0.12694	4.1968	0.43869

Table 4-14 - IGBTs STGP19NC60KD Turn-Off Parameters Average & Std. Dev. Test @ V_{DC} 480V.

turn-off parameters and corresponding standard deviation (σ), when new and after each age iteration. Table 4-15 provides the average percentage variation and corresponding standard deviation (σ), between each age iteration and new. After ageing, tested IGBTs again manifested an increase in the fall time of the gate-emitter voltage (V_{GE}) and an increase in the rise time of the collector-emitter voltage (V_{CE}). This led to a significant decrease in the collector-emitter voltage rate of change (dV_{CE}/dt_{OFF}), with an average percentage decrease after three age iterations of 40.21%, contributing to a decrease in ringing and overshoot in the collector-emitter voltage (V_{CE}). Moreover, a significant increase in the collector current (I_C) Fall Time (t_F) was observed, with an average percentage increase, after three age iterations, of 82.85%.

Again, this transient was characterized by an enhanced tail current amplitude and a prolonged tail current duration. Consequently, a longer turn-off power pulse was manifested leading to a significant increase in the energy losses during turn-off (E_{OFF}), with an average percentage increase, after three age iterations, of 90.59%. When compared to the IRG4BC30KD International Rectifier IGBT, the ST IGBT manifested similar trends for the collector current (I_C) Fall Time (t_F), collector-emitter voltage rate of change (dV_{CE}/dt_{OFF}), and energy loss during turn-off (E_{OFF}), but which were not as significant, even though still considered considerable. The comparison of the two IGBTs' parameters is provided in Table 4-16. A discussion of the physical reasons contributing to the more moderate variations manifested in the ST IGBT when compared to the IR IGBT, is conducted in Chapter 5.

AGE PHASES COMPARISON	IGBTs AVERAGE PERCENTAGE VARIATION TURN-OFF PARAMETERS @ V_{DC} 480V							
	TURN OFF DELAY TIME (%)	σ (%)	FALL TIME (%)	σ (%)	TURN OFF SWITCHING LOSS (%)	σ (%)	dV_{CE}/dt (%)	σ (%)
AGE A WITH NEW	2.489	3.181	38.383	7.315	31.149	19.769	-13.716	8.098
AGE B WITH NEW	6.647	0.516	70.332	11.943	66.335	26.334	-29.540	10.359
AGE C WITH NEW	13.633	9.233	82.846	28.789	90.594	32.490	-40.213	8.402

Table 4-15 - IGBTs STGP19NC60KD Turn-Off Parameters Average & Std. Dev. Percentage Variation @ V_{DC} 480V.

AGE PHASES COMPARISON	IGBTs AVERAGE PERCENTAGE VARIATION TURN-OFF PARAMETERS @ V_{DC} 480V							
	IRG4BC30KD				STGP19NC60KD			
	TURN OFF DELAY TIME (%)	FALL TIME (%)	TURN OFF LOSS (%)	dV_{CE}/dt (%)	TURN OFF DELAY TIME (%)	FALL TIME (%)	TURN OFF LOSS (%)	dV_{CE}/dt (%)
AGE A WITH NEW	-2.10	133.76	124.24	-29.24	2.489	38.383	31.149	-13.716
AGE B WITH NEW	-3.16	202.72	193.04	-40.99	6.647	70.332	66.335	-29.540
AGE C WITH NEW	-3.57	267.31	269.60	-57.07	13.633	82.846	90.594	-40.213

Table 4-16 - IGBTs IRG4BC30KD vs STGP19NC60KD Turn-Off Parameters Evolution with Ageing @ V_{DC} 480V.

4.6.2 Turn-On Delay Time (t_{D_ON}), Rise-Time (t_R), Turn-On Switching Loss (E_{ON}) and Collector Current Rate of Change during Turn-On (dI_C/dt_{ON})

The turn-on transients of IGBT Sample 1 of this test run, conducted at a V_{DC} of 480V and test collector current (I_C) of 16A are shown in Figure 4.33. It highlights the turn-on waveforms when new and after each age iteration. It is important to point out that each tested IGBT exhibited similar turn-on waveform transients. Table 4-17 provides the averages of the turn-on parameters and corresponding standard deviation (σ), when new and after each age iteration. Table 4-18 provides the average percentage variation and corresponding standard deviation (σ), between each age iteration and new. After ageing, tested IGBTs again manifested similar transients to the one manifested by the IRG4BC30KD International Rectifier IGBT, obtaining minimal changes during the turn-on phase as evidenced in Figure 4.33.

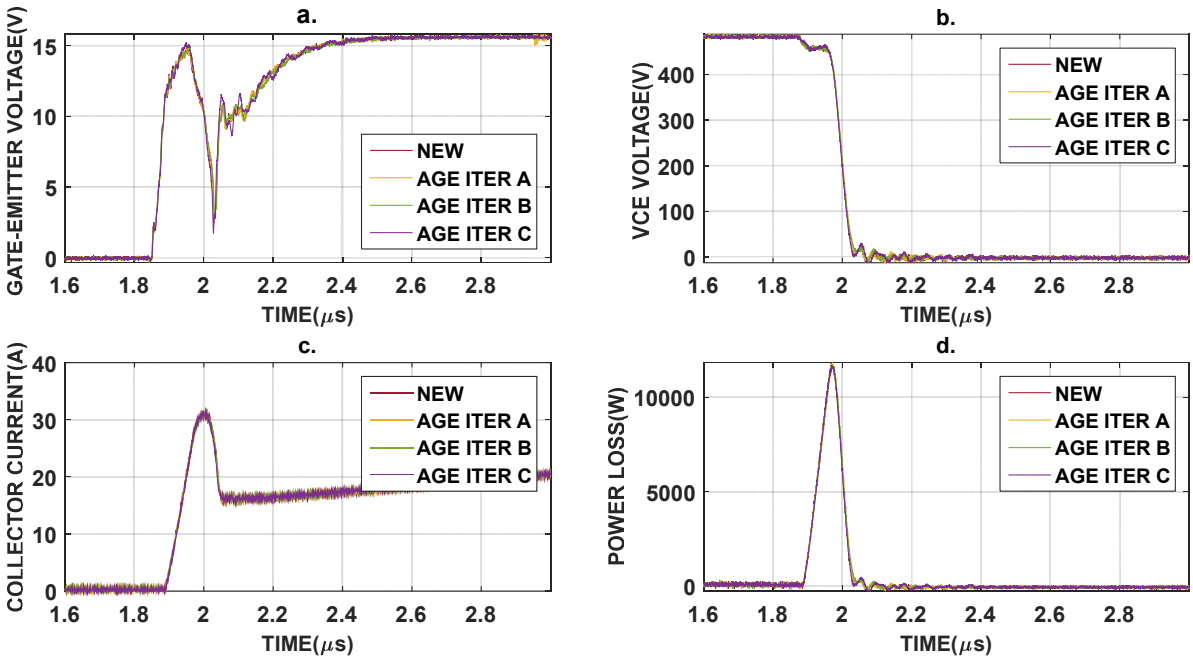


Figure 4.33 - Turn-On Transients Comparison NEW vs AGED (3 Age Iterations) IGBT STGP19NC60KD Sample 1 with V_{DC} 480V and Case Temperature (T_C) 25°C; (a) Gate-Emitter Voltage (V_{GE}) (b) Collector-Emitter Voltage (V_{CE}) (c) Collector Current (I_C) (d) Power Loss during Turn-Off (P_{ON}).

AGE PHASE	IGBTs AVERAGE TURN-ON PARAMETERS @ V_{DC} 480V							
	TURNON TIME (ns)	TURNON σ (ns)	RISE TIME (ns)	RISE TIME σ (ns)	TURNON SWITCHING LOSS (mJ)	SWITCHING LOSS σ (mJ)	dI_C/dt_{ON} (A/ns)	σ (A/ns)
NEW	39.87	0.462	39.20	0.400	0.8539	0.0147	0.3238	0.0025
AGE A	40.00	0.400	39.60	0.566	0.8726	0.0180	0.3233	0.0046
AGE B	40.93	0.231	39.73	0.611	0.8811	0.0208	0.3195	0.0033
AGE C	41.00	0.283	40.00	0.800	0.8996	0.0326	0.3174	0.0033

Table 4-17 – IGBTs STGP19NC60KD Turn-On Average & Standard Deviation Test @ V_{DC} 480V

After ageing, tested IGBTs manifested marginal change in the rise-time of the gate-emitter voltage (V_{GE}). Correspondingly a marginal increase in the Turn-On Delay Time (t_{D_ON}) was observed, with an average percentage increase, after three age iterations, of 2.843%. Again, the collector current (I_C) rise-time (t_R) manifested a marginal increase when compared to the more severe changes in the fall-time (t_F), observed in the turn-off transients, with an average percentage increase, after three age iterations, of 2.041%.

The marginal increase in the turn-on, rise time (t_R), led to a marginal decrease in the rate of rise of collector current (dI_c/dt_{ON}) with an average percentage decrease, after three age iterations, 1.989%. Due to the above, there was a minimal increase in turn-on power pulse duration leading to a marginal increase in the energy losses during turn-on (E_{ON}), with an average percentage increase, after three age iterations, of 5.352%. The comparison of the two IGBTs' parameters is provided in Table 4-19, highlighting the same trends in the measured changes, as well as the fact that the measured changes are considered marginal when compared to the more drastic changes experienced during turn-off.

AGE PHASES COMPARISON	IGBTs AVERAGE PERCENTAGE VARIATION TURN-ON PARAMETERS @ V_{DC} 480V							
	TURN ON DELAY TIME (%)	σ (%)	RISE TIME (%)	σ (%)	TURN ON SWITCHING LOSS (%)	σ (%)	dI_C/dt_{ON} (%)	σ (%)
AGE A WITH NEW	0.334	0.081	1.020	0.572	2.192	1.449	-0.166	0.1571
AGE B WITH NEW	2.676	0.606	1.361	0.889	3.192	2.101	-1.336	0.2604
AGE C WITH NEW	2.843	0.681	2.041	1.153	5.352	2.374	-1.989	0.2853

Table 4-18 - IGBTs STGP19NC60KD Turn-On Average & Standard. Deviation Percentage Variation @ V_{DC} 480V.

AGE PHASES COMPARISON	IGBTs AVERAGE PERCENTAGE VARIATION TURN-ON PARAMETERS @ V_{DC} 480V							
	IRG4BC30KD				STGP19NC60KD			
	TURN ON DELAY TIME (%)	RISE TIME (%)	TURN ON LOSS (%)	dI_C/dt_{ON} (%)	TURN ON DELAY TIME (%)	RISE TIME (%)	TURN ON LOSS (%)	dI_C/dt_{ON} (%)
AGE A WITH NEW	4.7526	3.5796	2.3092	-3.4291	0.334	1.020	2.192	-0.166
AGE B WITH NEW	4.9902	5.0067	3.0048	-5.0651	2.676	1.361	3.192	-1.336
AGE C WITH NEW	5.2693	5.2232	3.8069	-5.3960	2.843	2.041	5.352	-1.989

Table 4-19 - IGBTs IRG4BC30KD vs STGP19NC60KD Turn-On Evolution with Ageing @ V_{DC} 480V.

4.6.3 IGBT's Internal Diode Reverse Recovery Time (t_{RR}), Internal Diode Peak Reverse Recovery Current (I_{PRR})

Figure 4.34 shows the recovery waveforms of the internal diode of IGBT Sample 3 of this test run, and the corresponding power loss during reverse recovery, conducted when the IGBT was new and after each age iteration. The test reverse voltage (V_R) was set to 200V DC, while the forward current (I_F) was set to 12A, the same conditions as the test run for the International Rectifier IGBTs. It is important to point out that each tested IGBT exhibited similar recovery transients. Table 4-20 provides the average reverse recovery parameters and corresponding standard deviation (σ), when new and after each age iteration. Table 4-21 provides the average percentage variation and corresponding standard deviation (σ), between each age iteration and new. Again, an increase in the reverse recovery time was observed with an average percentage increase, after three age iterations, of 6.701%. The same trend was noticed in the Peak Reverse Recovery Current (I_{PRR}) with an average percentage increase, after three age iterations of 2.895%. Since these two parameters vary significantly with temperature and the rate of fall of forward current (dI_F/dt), characterization was conducted with the DUT case temperature (T_C) set at 25°C, while the rate of fall of forward current (dI_F/dt) was measured when new and after each age iteration, ensuring that this parameter remained relatively constant.

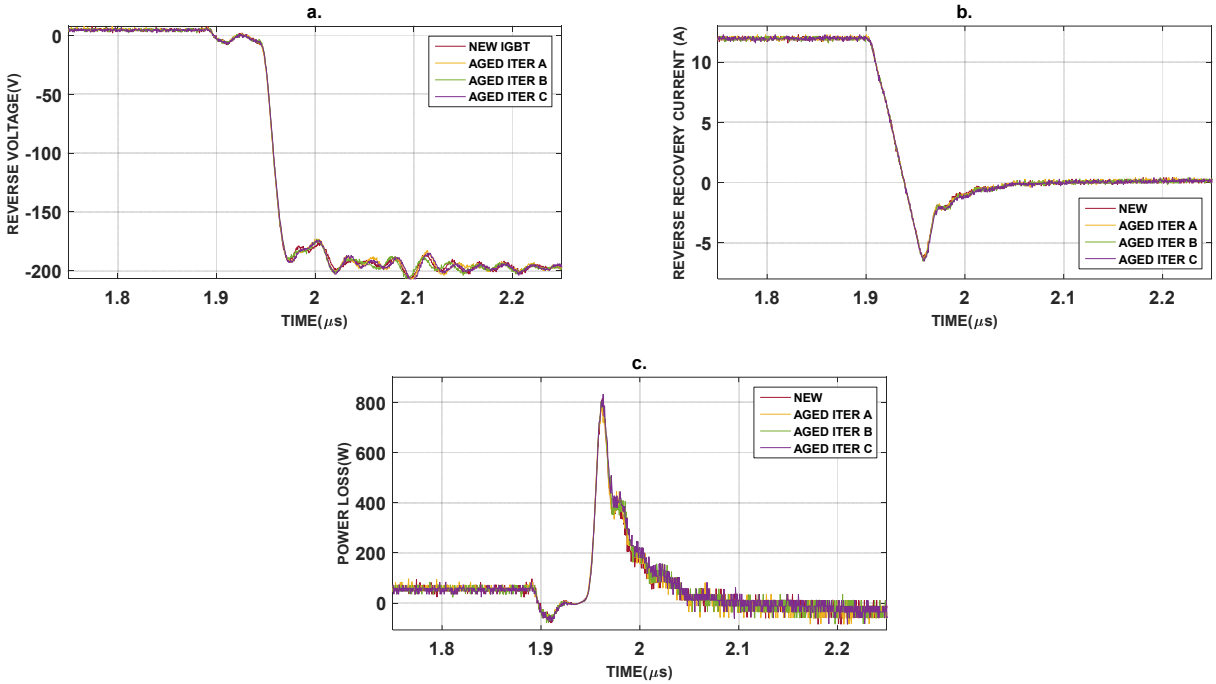


Figure 4.34 - Reverse Recovery Transients Comparison NEW vs AGED (3 Age Iterations) IGBT Sample 3 STGP19NC60KD with V_{RR} 200V, Forward Current (I_F) 12A and Case Temperature (T_C) 25°C; (a) Reverse Voltage (V_{RR}) (b) Reverse Recovery Current (I_{RR}) (c) Power Loss during Reverse Recovery (P_{RR}).

AGE PHASE	IGBTs AVERAGE REVERSE RECOVERY PARAMETERS @ V_{RR} 200V					
	Reverse Recovery Time (ns)	Reverse Recovery σ (ns)	Peak Reverse Recovery Current (A)	Peak Reverse Recovery σ (A)	Energy Loss Recovery (mJ)	Energy Loss Recovery σ (mJ)
NEW	88.8	1.697	6.18	0.1697	0.02170	0.00255
AGE A	91.4	5.374	6.24	0.0848	0.02210	0.00209
AGE B	93.6	6.223	6.3	0.3394	0.02242	0.00289
AGE C	94.8	6.788	6.36	0.2546	0.02271	0.00347

Table 4-20 - IGBTs STGP19NC60KD Reverse Recovery Parameters Average & Standard Deviation Test @ V_{RR} 200V.

Hence the average value of the rate of fall of forward current (dI_F/dt), was determined to be 328.36A/μs with a corresponding standard deviation (σ) of 4.209A/μs. This was obtained from all tested IGBT samples and corresponding age iteration measurements. The increase in reverse recovery time (t_{RR}) and the peak reverse recovery current (I_{PRR}) led to an increase in the energy loss during reverse recovery, with an average percentage increase after three age iterations, of 4.402%. The comparison of the two IGBTs' recovery parameters is provided in Table 4-22, highlighting the same trends in the measured changes between the two IGBTs, with the International Rectifier IGBT recovery parameters experiencing larger changes.

AGE PHASES COMPARISON	IGBTs AVERAGE PERCENTAGE VARIATION REVERSE RECOVERY PARAMETERS @ V_{RR} 200V					
	Reverse Recovery Time (%)	Reverse Recovery σ (%)	Peak Recovery Current (%)	Peak Reverse Recovery σ (%)	Energy Loss Recovery (%)	Energy Loss Recovery σ (%)
AGE A WITH NEW	2.924	0.207	0.971	0.095	1.803	0.062
AGE B WITH NEW	5.336	1.618	1.943	0.529	3.243	1.189
AGE C WITH NEW	6.701	2.929	2.895	1.293	4.402	2.338

Table 4-21 - IGBTs STGP19NC60KD Reverse Recovery Parameters Avg. & Std. Dev. Percentage Variation @ V_{RR} 200V.

AGE PHASES COMPARISON	IGBTs AVERAGE PERCENTAGE VARIATION REVERSE RECOVERY PARAMETERS @ V_{RR} 200V					
	IRG4BC30KD			STGP19NC60KD		
	Reverse Recovery Time (%)	Peak Recovery Current (%)	Energy Loss Recovery (%)	Reverse Recovery Time (%)	Peak Recovery Current (%)	Energy Loss Recovery (%)
AGE A WITH NEW	3.131	2.725	3.024	2.924	0.971	1.803
AGE B WITH NEW	5.893	4.112	6.097	5.336	1.943	3.243
AGE C WITH NEW	9.623	8.349	10.551	6.701	2.895	4.402

Table 4-22 - IGBTs IRG4BC30KD vs STGP19NC60KD Recovery Parameters Evolution with Ageing @ V_{RR} 200V.

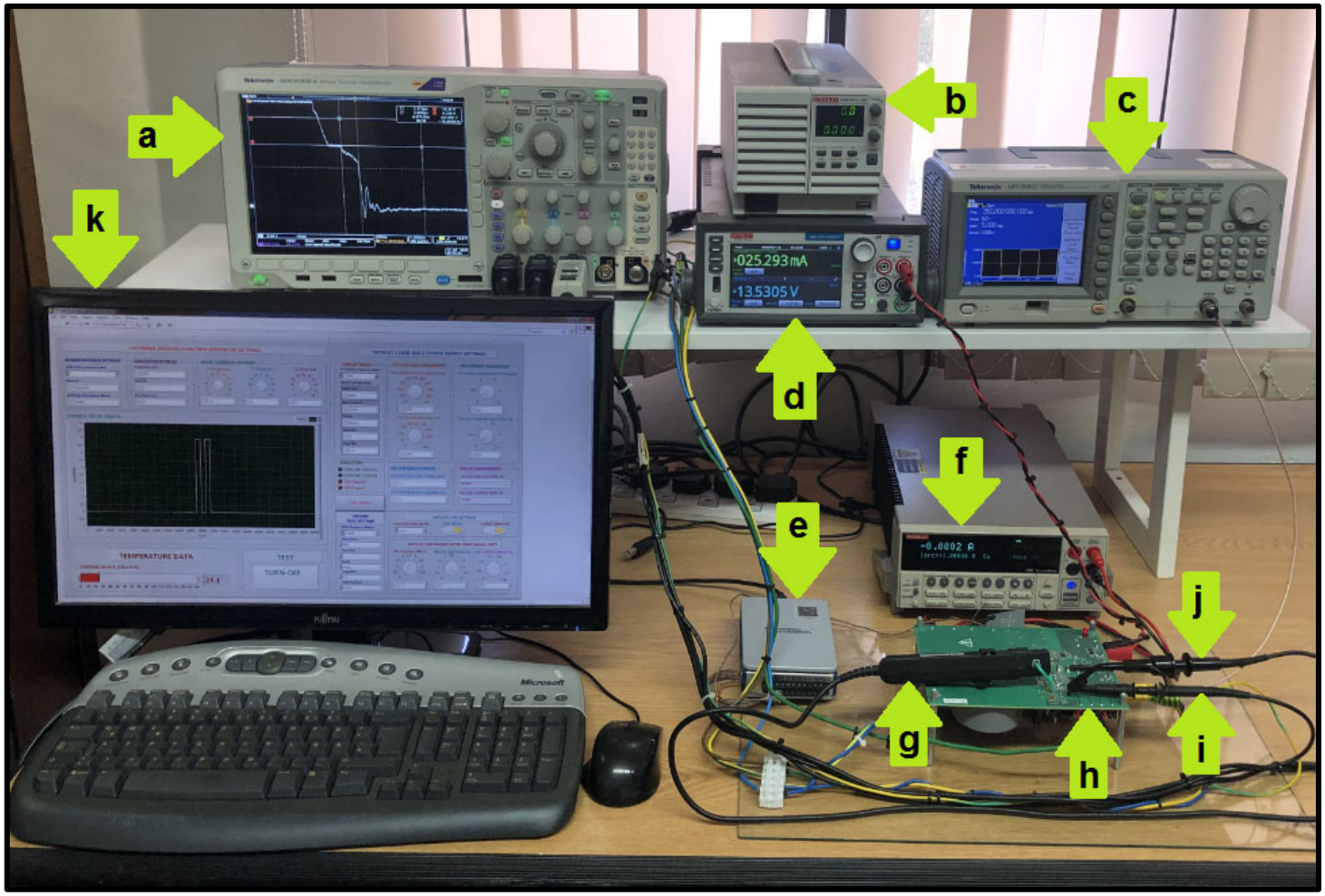


Figure 4.35 - IGBT Double Pulse Switching Parameters Characterization System (a) Tektronix MDO4104-B Oscilloscope (b) Keithley 2260B-800-2 Programmable High Voltage Power Supply (c) Programmable Function Generator Tektronix AFG3051C (d) Power Source Meter Unit Keithley SMU2461 set as Low Voltage Auxilliary Power Supply (e) National Instruments Thermocouple DAQ NI-9211 (f) Tektronix Source Meter Unit SMU2400 (g) Tektronix TCP0030A AC/DC 120MHz 30A RMS current probe (h) Switching Parameters Characterization Double Pulse Hardware (i) Tektronix TPP1000 1GHz 300V 3.9pF/10MΩ (j) Tektronix TPP0850 800MHz 1.8pF/40MΩ 1000V passive high voltage probe (k) DAQ & Control

4.7 Conclusions

This chapter presented the methodology to determine the switching parameters and switching transients' evolution caused by the implemented accelerated ageing strategy. As evidenced earlier, this ageing strategy produced significant degradation in the IGBTs' die-attach as well HCI effects, which impacted the gate's dielectric integrity. The degradation of the die-attach will decrease the devices' thermal capabilities as it impacts the devices' thermal impedance of the PN junction closest to the collector. This means that after ageing this junction will experience higher temperatures, leading to a higher concentration of charge carriers. This leads to an increase in the minority carriers' lifetime during turn-off, resulting in an increased and prolonged tail current, manifesting itself in a significant decrease of the turn-off IGBT commutation speed. This directly impacted the dV_{CE}/dt capabilities during turn-off, which resulted in smaller high frequency current passing through the reverse transfer (Miller) capacitance (C_{REV}) of the IGBT. Since before and after ageing the gate resistances were not changed, it is the smaller high frequency Miller current, which is causing a decrease in ringing in the gate-emitter voltage (V_{GE}) during turn-off, consequently dampening the ringing in the collector-emitter voltage (V_{CE}). In Chapter 3, the die-attach degradation of the internal free-wheeling diode section, was also observed. This in-turn effects the thermal impedance of the diode's PN junction, which leads to a higher charge carrier concentration when the diode is forward biased. This increases the minority carriers' presence and lifetime during reverse-biasing hence leading to an increase in the peak reverse recovery current (I_{PRR}) and the reverse recovery time (t_{RR}).

The salient result obtained throughout this chapter was the drastic influence of the turn-off transient when compared to the impacts of the turn-on transient, on the general IGBT's switching slow-down and consequently enhanced switching energy loss, as the implemented ageing progresses. It was verified that this trend was consistent across IGBTs produced by different semiconductor manufacturers. Hence, the degradation mechanisms monitored and described in Chapter 3 are predominantly impinging on the turn-off transient of the IGBT, with the turn-on transient remaining relatively unchanged. This differentiation between the two transients is related to the dominance between the intrinsic MOSFET structure and BJT structure during the switching transients as well as the evolution of the parasitic IGBT structures with the implemented accelerated ageing strategy. Thorough understanding of this result entails the modelling of the IGBT's switching transients with ageing, which is the work to follow in Chapter 5.

Chapter 5 Modelling Switching Transients of Aged IGBTs

Tools which facilitate a realistic estimation of the IGBT's switching transients, are becoming important for electronic engineers, to optimize the product design both from an electromagnetic as well as thermal management point of views. For applications which are critical, such estimations are becoming important, not only when the IGBT is new, but also when the IGBT has experienced ageing and degradation, hence ensuring design reliability under the widest range of operational scenarios. An Electromagnetic Transient Program (ETP) is a software which provides the simulation and analysis of power systems' transients. Applications include transient analysis of systems such as AC power systems, power electronics, high-voltage DC (HVDC) transmission, flexible AC transmission systems (FACTS), distribution systems, and complex power-electronic controllers. Examples of such ETP software are the ETAP eMT^{TM} [211] and EMTP-RV [212]. Most ETP software, model power semiconductor devices as on-off switches or two state resistances. This simple representation is sufficiently accurate to simulate the system-level electrical behavior of power electronic circuits. However, the accurate estimation of the switching losses and electromagnetic transient representation, requires the consideration of the physics of the switching process. This is more important if the ageing effects on the corresponding switching transients are to be considered.

This chapter presents the analysis and corresponding modelling of the IGBT's switching transients. The analysis primarily focuses on two transients' models, the Jin et al. [215] model, which describes the IGBT's switching transients through piecewise linear equations, derived from the analysis of an equivalent IGBT switching circuit, and the Rajapaske et al. [213] model, which describes the IGBT's switching transients through piecewise non-linear equations, obtained through the transients' characteristic variation with time, for the different turn-on and turn-off phases. Both models were rederived (as this was marginally provided) and compared to the measured IGBT switching transients, providing an insight on the influence of the physical electronics and parasitic elements on the characteristics of these transients when the IGBT is in a healthy state. Moreover, these models were modified by either introducing variations to the model elements' values, or providing new model equations, to account for the measured switching transients' changes due to the implemented accelerated ageing.

5.1 IGBT's Switching Transients General Analysis

IGBTs are power switches which combine the physics of a MOSFETs and power BJT. As explained in Section 3.3.4, when compared to power MOSFETs, the IGBT has an extra P+ layer. The base current of the BJT is via the MOSFET, which is in-turn controlled by the MOSFET's gate voltage. By imposing the gate voltage, a channel is formed to provide the base current of the intrinsic BJT thereby turning-on the IGBT. Otherwise, a negative voltage on the gate, eliminates the channel thereby turning-off the IGBT. Different from the power MOSFET, the existence of the PNP BJT results in a time delay to recombine the carriers even after the channel diminishes, creating the "tailing current". Moreover, the parasitic elements of the IGBT greatly impact the IGBT's switching process. In relation to the turn-on procedure this can be generally divided into four stages [3]:

Stage 1 – Figure 5.1 illustrates the equivalent circuit of the IGBT during the turn-on first stage. During this stage, the gate-drive voltage (V_G) starts to increase. The IGBT remains off until the gate-emitter voltage (V_{GE}) rises to the threshold voltage V_{TH}. The collector-emitter voltage (V_{CE}) and the collector current (I_C) remain unchanged. The gate-voltage-controlled current source shown in the equivalent model is equal to zero when $V_{GE} < V_{TH}$.

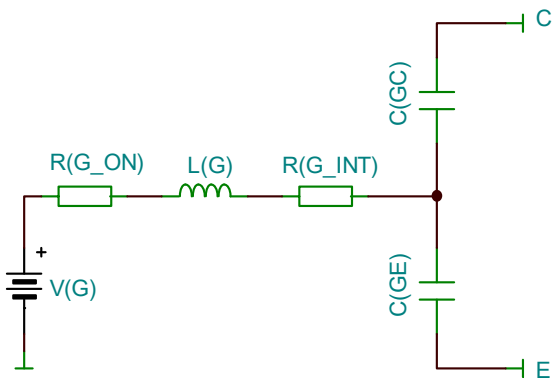


Figure 5.1 – IGBT Stage 1 Turn-On Equivalent Circuit.

Stage 2 – Figure 5.2 illustrates the equivalent circuit of the IGBT during the turn-on second stage. During this stage, the gate continues being charged. The collector current (I_C) starts to rise with the increasing gate-emitter voltage (V_{GE}). The collector-emitter voltage (V_{CE}) drops towards the gate-emitter voltage (V_{GE}). The output gate-voltage-controlled current source representing the collector current (I_C) is equal to $g_m(V_{GE} - V_{TH})$ when the device is in the active region.

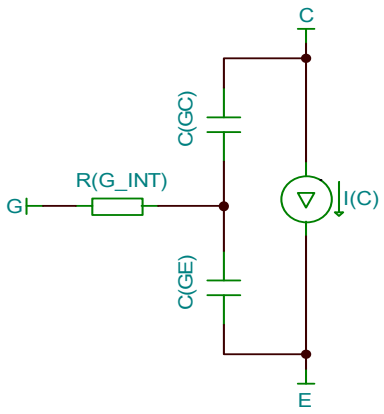


Figure 5.2 - IGBT Stage 2 Turn-On Equivalent Circuit.

Stage 3 – Figure 5.3 illustrates the equivalent circuit of the IGBT during the turn-on third stage. During this stage, the collector-emitter voltage (V_{CE}) drops further close to the on-state saturation voltage (V_{CE_SAT}). At this stage, due to the Miller effect, the input gate voltage is constant, set at the Miller plateau. Hence the gate-emitter voltage is constant during this state (since the emitter voltage is constant too), which means that the parasitic input gate-emitter capacitance (C_{GE}) appears as high impedance, leading nearly all the input gate current (I_G) to flow through the Miller capacitance (C_{CG}).

Stage 4 – Figure 5.4 illustrates the equivalent circuit of the IGBT during the turn-on fourth stage. The collector-emitter voltage (V_{CE}) has dropped to the on-state saturation voltage and remains constant, and the Miller effect disappears. The gate-drive current (I_G) keeps charging the gate. The intrinsic MOSFET structure enters the ohmic region when the gate-emitter voltage is greater than the collector-emitter voltage ($V_{GE} > V_{CE}$).

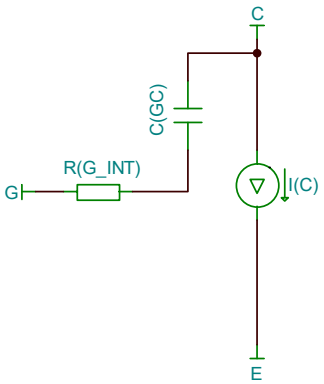


Figure 5.3 - IGBT Stage 3 Turn-On Equivalent Circuit.

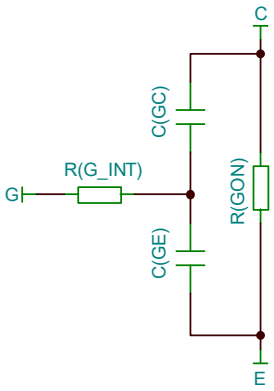


Figure 5.4 – IGBT Stage 4 Turn-On Equivalent Circuit.

In all the above four stages, the gate voltage (V_G) is the state variable, where the gate-drive current (I_G) charges the input capacitance ($C_{IES} = C_{GE} + C_{GC}$), through the gate-drive resistance (R_G) and gate-drive loop inductance (L_G). The IGBT turn-on switching is largely due to majority current, mainly determined by the MOSFET structure of the IGBT. MOSFETs are intrinsically faster than bipolar devices, since they have no excess minority carriers that must be moved in and out, when the device turns-on or off. The IGBT suffers from this effect mainly during turn-off. Other charges which must be moved are those on the stray capacitances as illustrated in Figure 5.1. The collector to emitter capacitance (C_{CE}) is not included in the equivalent model, as this does not affect the switching transients. This capacitance is important and must be considered when designing snubbers [3], which is beyond the scope of this analysis.

Another important consideration is that the parasitic gate to emitter capacitance (C_{GE}) and the gate to collector capacitance (C_{GC}), are not constant but vary according to the voltage across them. This is since these capacitances are in part contributed by the IGBT's depletion layers whose structure is voltage dependent [3]. For example, the gate-emitter capacitance is the combination of the capacitance of the depletion layer that forms the silicon - silicon dioxide interface (Si-SiO_2) in series with the electrostatic capacitance of the oxide layer. Due to this voltage dependence, it is the collector-gate capacitance (C_{CG}) which experiences the most significant changes as the experienced voltage across it is much larger than the voltage across the gate-emitter capacitance (C_{GE}). Hence, IGBT switching transient analysis, considers the collector-gate capacitance (C_{CG}) as voltage dependant. Other approaches [4], consider two discrete values for this capacitance (C_{CG1} and C_{CG2}).

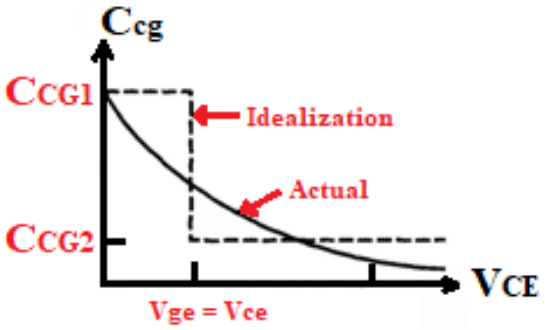


Figure 5.5 – IGBT's Intrinsic Collector-Gate Capacitance (C_{CG}) variation with the Collector-Emitter Voltage (V_{CE}) [11].

The collector-gate capacitance C_{CG1} represents the collector-gate capacitance (C_{CG}), when the intrinsic IGBT's MOSFET enters the ohmic region hence corresponding to a low collector-gate voltage (V_{CG}) and low collector-emitter voltage (V_{CE}). On the other side, when the collector-gate voltage (V_{CG}) is substantial and the output stage of the IGBT is not in the ohmic region, C_{CG2} is used. This corresponds to when the gate-emitter voltage is smaller than the collector-emitter voltage ($V_{GE} < V_{CE}$) [11]. This is illustrated in Figure 5.5.

5.1.1 IGBT General Turn-On Behaviour

During the turn-on delay-time $t_{d(on)}$, the gate-emitter voltage (V_{GE}) rises from zero to the threshold voltage (V_{TH}). The turn-on transient period is characterized by the initial rise of the collector current (I_C) during $t_{rise(on)}$. Once the gate-emitter voltage (V_{GE}) reaches the IGBT threshold voltage (V_{TH}), the collector-current (I_C) starts to rise. The rate of change of the collector current rise (dI_C/dt) is dependent on the rate of change of the gate voltage rise (dV_G/dt). The IGBT's turn-on switching transient is very similar to that of a power MOSFET.

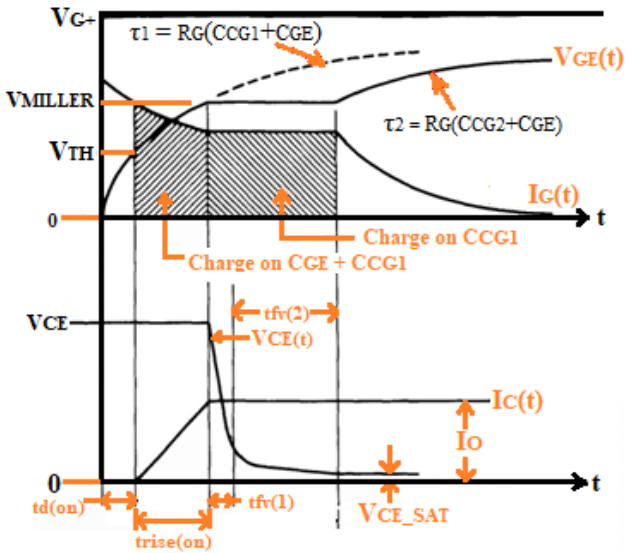


Figure 5.6 – Generic IGBT Turn-On V_{CE} and I_C [11].

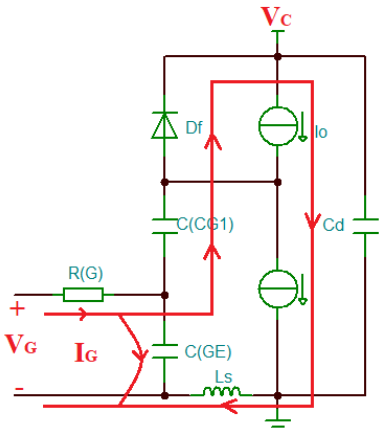


Figure 5.7 – IGBT Turn-On Transient Equivalent Circuit during $t_{RISE(ON)}$ [11].

The rise of the gate voltage (V_G) in this region, is exponential and has a corresponding time constant which is dependent on the input capacitance ($C_{ies} = C_{GE} + C_{CG}$), the stray inductance (L_S), the IGBT's transconductance (g_m), and the gate resistance (R_G). Figure 5.7 shows the equivalent circuit for the IGBT common-emitter configuration with clamped inductive load, which follows this phase of the turn-on transient, as discussed in the description above. The collector-emitter voltage (V_{CE}) remains unchanged, if the diode current (I_D) is smaller than the output current (I_O). The time required for the diode current (I_D) to build from zero to I_O corresponds to the current rise time $t_{rise(on)}$. Once, the IGBT is carrying the full load current (I_O), but is still in the active region, the gate-emitter voltage (V_{GE}) becomes temporarily clamped at a constant voltage known as the Miller Plateau. At this point the entire gate current flows through the collector-gate capacitance (C_{CG}), with the equivalent circuit shown in Figure 5.8. This is since the rate of rise of the gate-emitter voltage (dV_{GE}/dt) is zero and hence the gate-emitter capacitance (C_{GE}) is high impedance. The decrease in the collector-emitter voltage (V_{CE}) occurs in two distinct time intervals $tfv_{(1)}$ and $tfv_{(2)}$[11].

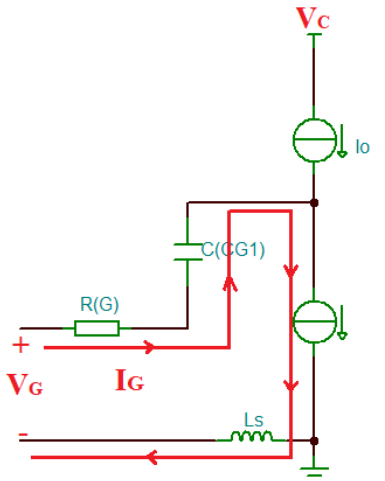


Figure 5.8 - IGBT Turn-On Transient Equivalent Circuit during the Miller Plateau [11].

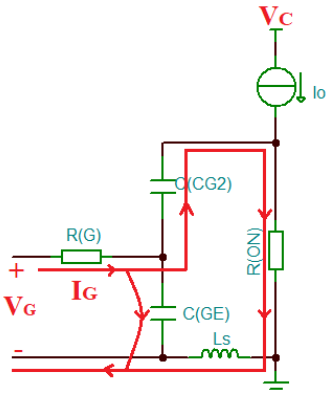


Figure 5.9 - IGBT Turn-On Transient Equivalent Circuit during and beyond tfv2 [11].

The first-time interval corresponds to when the device is still in the active region and the collector-gate capacitance (C_{CG}) is represented by C_{CG2}. The second time interval corresponds to the completion of the transient in the ohmic region where the equivalent circuit is the one shown in Figure 5.9. The free-wheeling diode (D_F) is not ideal, and hence has a corresponding reverse-recovery current. This changes the ideal turn-on switching waveforms shown in Figure 5.6. During the current rise time the collector current (I_C) goes beyond the output current (I_O) due to the addition of the reverse recovery current ($I_O + I_{RR}$). This causes the gate-emitter voltage (V_{GE}) to rise beyond the Miller voltage (V_{MILLER}). When the diode goes into hard reverse biasing, there is a rapid decrease of the gate-emitter voltage (V_{GE}) back to the Miller voltage (V_{MILLER}). This rapid decrease provides an additional current in the collector-gate capacitance (C_{CG}) in addition to the input gate current (I_G). This additional current causes the collector-gate voltage (V_{CG}) and in-turn the collector-emitter voltage (V_{CE}), to decrease very rapidly during the recovery interval. Once the reverse-recovery interval is over, the collector current (I_C) is back to the output current (I_O) and the rest of the transient proceeds as in the ideal diode scenario [11]. This is illustrated in Figure 5.10.

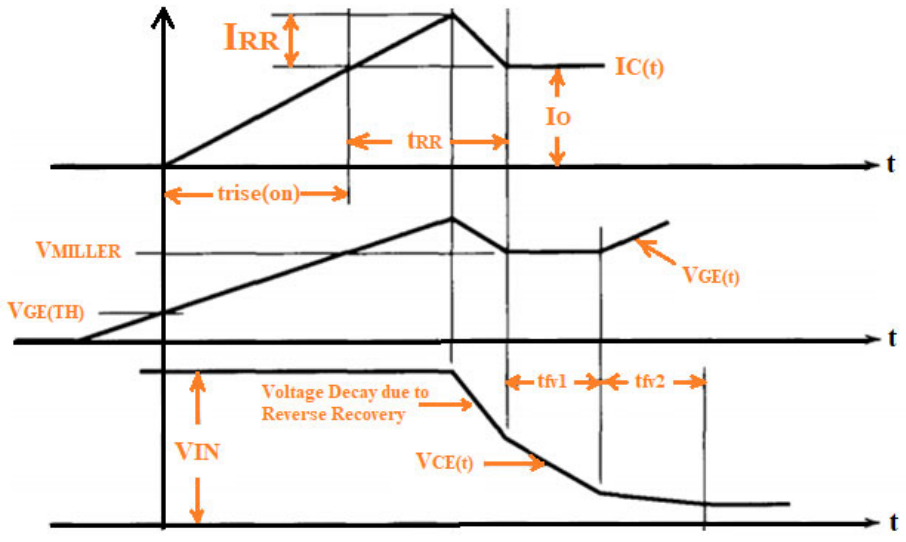


Figure 5.10 – Generic IGBT Turn-On Transient Waveforms including Reverse Recovery [11]

5.1.2 IGBT General Turn-Off Behavior

The IGBT turn-off transient involves the inverse procedure of the turn-on transient. The same approach can be utilized to obtain the turn-off voltage and current waveforms. According to Mohan [11], the intrinsic IGBT's MOSFET parasitic capacitances are relatively independent of the IGBT's junction temperature (T_J), hence the switching power losses in the intrinsic MOSFET are to a certain extent independent of junction temperature (T_J). However, the IGBT's on-state resistance is dependent on the junction temperature (T_J) and thus the on-state power loss, does depend on the junction temperature (T_J). In relation to the turn-off behavior, the turn-off delay time ($t_{d(off)}$), and the voltage rise time during turn-off are governed by the IGBT's intrinsic MOSFET. The major difference between the generic IGBT turn-off transients and that of a power MOSFET, is in the collector current (I_C) transient. This latter transient is generally characterized by two, time intervals, one due to the intrinsic MOSFET structure and another one due to the intrinsic BJT section. The turn-off current is characterized by an initial rapid drop due to the turn-off of the intrinsic MOSFET. The second interval is characterized by a "tail current" due to the stored charge in the N^- drift region which is a characteristic of a BJT structure. This is since, the MOSFET section of the IGBT is switched-off and there is no reverse voltage applied to the IGBT that could generate a negative collector current, hence preventing from removing the stored charge [1]. This is illustrated in Figure 5.11.

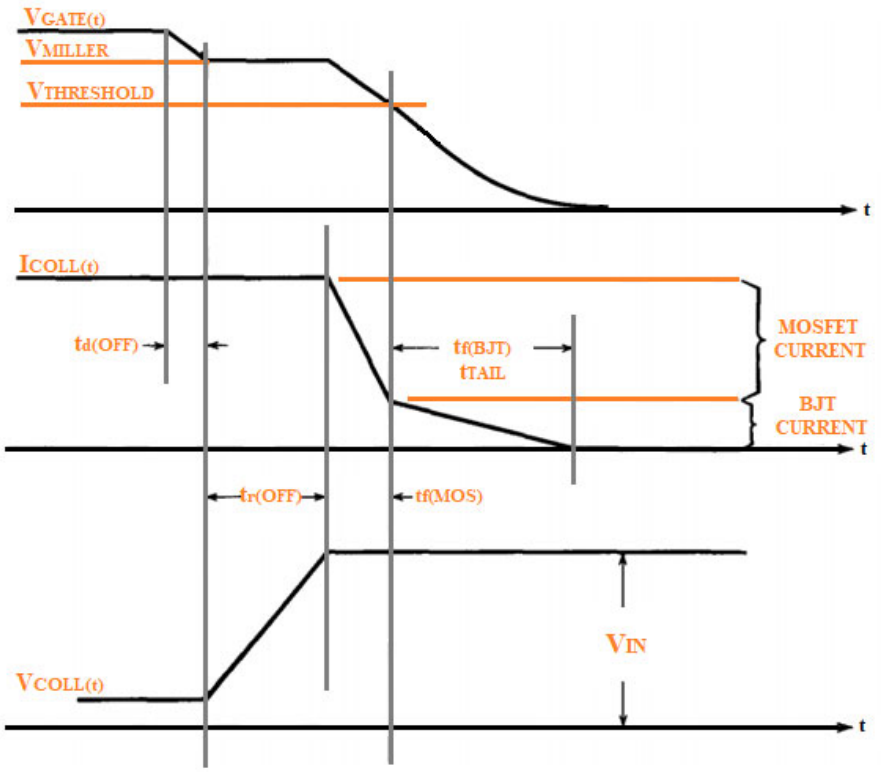


Figure 5.11 – Generic IGBT Turn-Off Transient Waveforms [11]

The only method of removing the excess charge carriers is through recombination. It is desirable to have the availability of excess charge carriers in this region, such that, the on-state collector-emitter voltage (V_{CE_ON}) is kept to a minimum. On the other side, the larger the availability of charge carriers the longer the duration of the "tail current", which in-turn effects the switching power dissipation. The presence of the charge carriers in the N^- drift is significantly affected by the IGBT's junction temperature (T_J), where the higher the value of the latter, the higher the presence of free-charge carriers, the longer the duration of the "tail current" [5].

5.2 IGBT Switching Transients Linear Piecewise Modelling

Figures 5.12 and 5.20 depict the reference IGBT turn-on and turn-off transients, when the IGBT is employed within a common-emitter circuit, with a clamped inductive load. These reference waveforms are to be utilized to obtain the corresponding turn-on and turn-off transients' model equations for each transient phase. The first approach was partially based on the approach, presented by Jin et al. [215], where each waveform transient phase was described through linear equations, based on the equivalent circuit provided in Figure 5.13, hence obtaining a set of linear equations for each waveform. This will be conducted for both the collector-emitter voltage (V_{CE}) transient, and the collector current (I_C) transient, for both turn-on and turn-off.

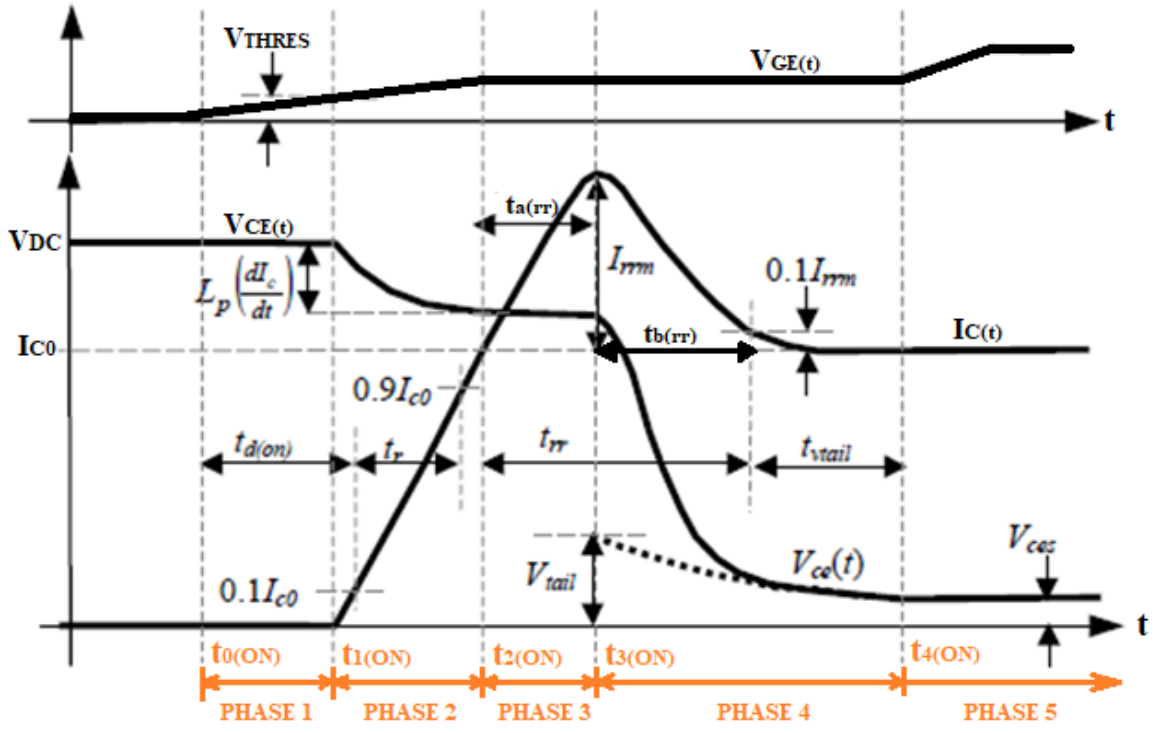


Figure 5.12 – IGBT Turn-On Transient Reference Waveforms for Piecewise Linear and Non-Linear Modelling [213].

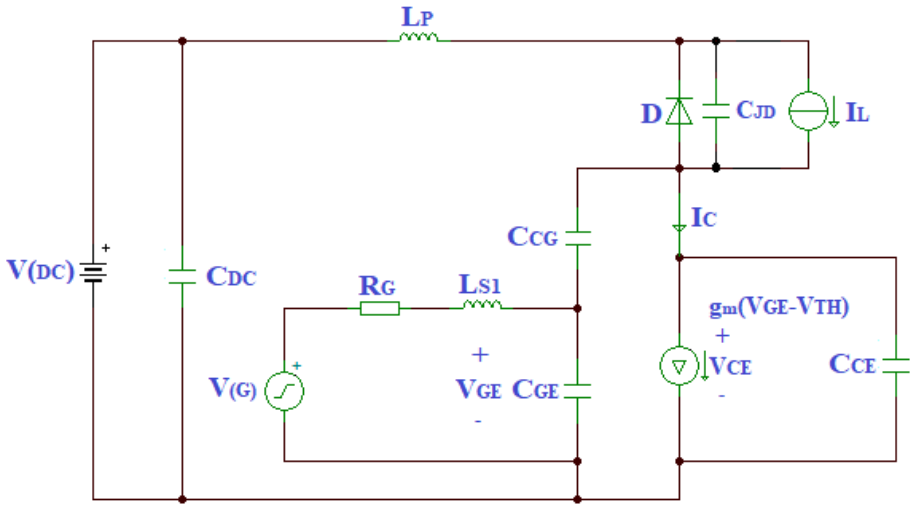


Figure 5.13 – IGBT Behavioral Circuit for Piecewise Linear Modelling [215]

5.2.1 IGBT Piecewise Linear Model for Turn-On Transients during Phase 1

In IGBT datasheets, the turn-on behaviour is characterized by the turn-on delay time ($t_{d(ON)}$), the rise time (t_r) and the turn-on energy (E_{ON}). The utilized equivalent circuit to obtain the turn-on piecewise linear equations is illustrated in Figure 5.14. In relation to Figure 5.12, the turn-on gate pulse is applied at $t_{0(ON)}$ resulting in the gradual rise of the gate-emitter voltage (V_{GE}). This is due to the charging of the IGBT's input capacitance (C_{IES}), where the latter is the summation of the gate-emitter capacitance (C_{GE}) and the collector-gate capacitance (C_{CG}) as provided by Equation 5.1. As indicated in Section 5.1, both these capacitances are voltage dependent, where the collector-gate capacitance (C_{CG}) experiences the largest change due to the large dynamic change of the collector-gate voltage (V_{CG}). During this phase, the IGBT's collector-emitter voltage (V_{CE}) and the collector current (I_C) remains relatively unchanged, hence represented in the piecewise linear model, by a constant voltage V_{DC} (in the case of the IGBT's Double Pulse test procedure utilized in Chapter 4, V_{DC} was set to 480V DC), and a collector current (I_C) set at 0A.

$$C_{IES} = C_{GE} + C_{CG} \tag{5.1}$$

5.2.2 IGBT Piecewise Linear Model for Turn-On Transients during Phase 2

Phase 2 starts at time $t_{1(ON)}$, when the gate-emitter voltage (V_{GE}) reaches the threshold voltage (V_{THRES}). At this point the collector current (I_C), starts to rise almost linearly, with the load current transferring from the free-wheeling diode to the IGBT. During this phase the collector-emitter voltage (V_{CE}), experiences a drop. This drop is mainly due to the rate of change of the collector current (dI_C/dt) through the parasitic inductance (L_P).

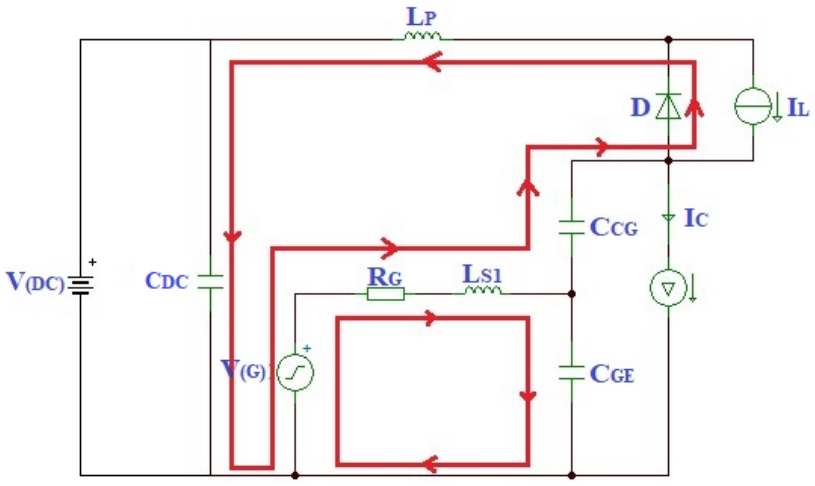


Figure 5.14 – IGBT Equivalent Circuit during Turn-On Transients [215].

The rate of change of the collector current (dI_C/dt) during this phase, is primarily dependent on the rate of change of the gate-emitter voltage (dV_{GE}/dt) and the IGBT forward transconductance (g_m). The rate of rise of the gate-emitter voltage (dV_{GE}/dt), in this region is almost linear, even though essentially it is a steep exponential increase with a time constant dependant on the input capacitance (C_{IES}) and stray gate inductance (L_{S1}) [214].

Hence the model equations for the constant rate of change of current (dI_C/dt) between $t_{1(ON)}$ and $t_{2(ON)}$ and correspondingly the constant dV_{CE}/dt during this period, as illustrated in Figure 5.15, were obtained as follows. The forward transconductance (g_m) is the ratio of the collector current (I_C) and the input voltage (V_G) as shown in Equation 5.2.

$$g_m = \frac{I_C}{V_G} \tag{5.2}$$

Hence from the above, the rate of change of rise of collector current (dI_C/dt) is given by Equation 5.3:

$$\frac{dI_C}{dt} = \frac{dV_G}{dt} g_m \tag{5.3}$$

The rate of change of the gate voltage (dV_G/dt) is provided by Equation 5.4:

$$\frac{dV_G}{dt} = \frac{\Delta V_G}{\text{Time Constant}} = \frac{\Delta V_G}{\text{Time Constant due to } R_G C_{ies} + \text{Time Constant due to } g_m L_{S1}} \tag{5.4}$$

Hence the rate of rise of the collector current (dI_C/dt) using Equation 5.4 is provided by Equation 5.5.

$$\left.\frac{dI_C}{dt}\right|_{t_{1on}<t<t_{2on}} = \frac{g_m(V_{G+} - V_{TH})}{(R_G C_{ies} + g_m L_{S1})} \tag{5.5}$$

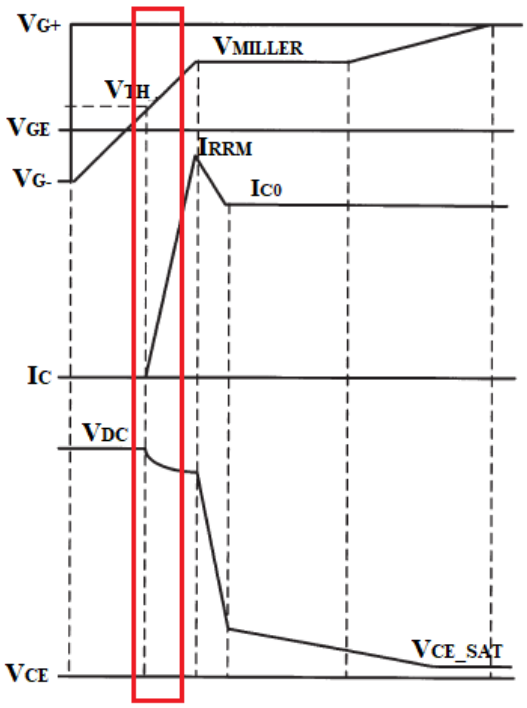


Figure 5.15 - IGBT Piecewise Linear Model Phase 2 Turn-On Waveforms (t_{1ON}–t_{2ON}) [215].

Consequently, the rise in collector current (I_C) between $t_{1(on)}$ and $t_{2(on)}$ causes a counteracting fall in the collector-emitter voltage (V_{CE}) transient in the primary stray inductance (L_P). The decrease in the collector voltage (V_{CE}) can be obtained by Equation 5.6, yielding to the rate of fall of the collector-emitter voltage (dV_{CE}/dt) during this period, provided by Equation 5.7:

$$\Delta V_{CE} = -L_P \frac{dI_C}{dt}\Big|_{t_{1on}<t<t_{2on}} \tag{5.6}$$

$$\frac{dV_{CE}}{dt}\Big|_{t_{1on}<t<t_{2on}} = -L_P \frac{\frac{dI_C}{dt}|_{t_{1on}<t<t_{2on}}}{(t_{2on}-t_{1on})} \tag{5.7}$$

5.2.3 IGBT Piecewise Linear Model Turn-On Transients during Phase 3

During Phase 3, the collector current (I_C) experiences a current overshoot due to the inability of the free-wheeling diode to immediately go into reverse blocking mode, hence continuing to conduct the reverse recovery current (I_{RR}). The rate of rise of the collector current (dI_C/dt), during the initial phase of the reverse recovery, hence Phase 3, is governed by the rate of rise of the collector current (dI_C/dt) during Phase 2, as described by Equation 5.5. The collector current (I_C) rises until the peak reverse recovery (I_{RRM}) of the free-wheeling diode (D) is reached. Consequently, during Phase 3, the collector-emitter voltage (V_{CE}) continues to experience a decay, as the one described during Phase 2 and is represented by Equation 5.7. The above is illustrated in Figure 5.16.

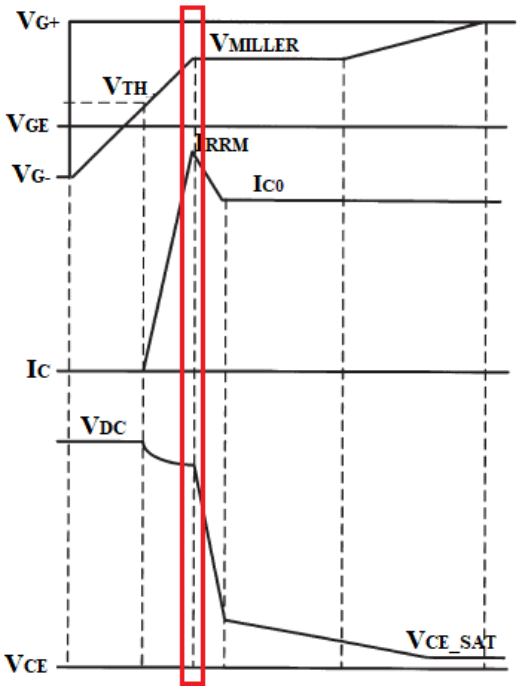


Figure 5.16 - IGBT Piecewise Linear Model Phase 3 Turn-On Waveforms (t_{2ON}–t_{3ON}) [215].

During Phase 2, the free-wheeling diode is in conduction and hence there is a minority charge carriers' surplus, in each layer of the diode (holes in the N-layer and electrons in the P-layer). At turn-off this surplus of charge carriers will not extinguish immediately, hence keeping the diode to conduct for the reverse recovery time (t_{RR}). The collector current (I_C) continues to rise with the same rate of change experienced during Phase 2. The reverse recovery time (t_{RR}) depends on the forward current flowing through the diode at the turn-off instant (I_{C0}), the reverse voltage that is applied (V_R), the rate of change of the forward current (dI_F/dt) and the diode's junction temperature (T_{JD}) [215]. In relation to Figure 5.12:

$$t_{RR} = t_{a(RR)} + t_{b(RR)} \tag{5.8}$$

t_{RR} is the reverse recovery time of the freewheeling diode, $t_{a(RR)}$ is the initial phase of the reverse recovery current until the peak reverse recovery current (I_{RRM}) is reached and reflects the time required by the free-wheeling diode to remove the charge from the depletion region, $t_{b(RR)}$ is the second phase of the reverse recovery current and reflects the time required for charge to be removed from the diode's semiconductor region. Hence the peak reverse recovery current (I_{RRM}) is provided by Equation 5.9.

$$I_{RRM} = t_{a(rr)} \frac{dI_C}{dt}\Big|_{t_{2on}<t<t_{3on}} = t_{a(rr)} \frac{dI_C}{dt}\Big|_{t_{1on}<t<t_{2on}} \tag{5.9}$$

A power diode's softness or 'snappiness' factor (S) is defined as the ratio of the $t_{b(RR)}$ to $t_{a(RR)}$ provided by Equation 5.10:

$$S = \frac{t_{b(rr)}}{t_{a(rr)}} \tag{5.10}$$

Hence substituting Equation 5.10 into Equation 5.9, yields to Equation 5.11:

$$I_{RRM} = \frac{t_{RR}}{(S+1)} \frac{dI_C}{dt}\Big|_{t_{1on}<t<t_{2on}} \tag{5.11}$$

The reverse recovery charge (Q_{RR}) is the amount of charge that flow through the diode when the diode changes state from forward conducting to reverse blocking. This is provided by the area enclosed by the collector-current (I_C) during reverse recovery and is approximated by Equation 5.12:

$$Q_{RR} \approx \frac{1}{2} I_{RRM} t_{rr} \tag{5.12}$$

Hence combining Equations 5.11 and 5.12, yields to Equation 5.13:

$$Q_{RR} = \frac{{t_{rr}}^2}{2(S+1)} \frac{dI_C}{dt}\Big|_{t_{1on}<t<t_{2on}} \tag{5.13}$$

Rearranging Equation 5.13 yields to Equation 5.14 [11]:

$$t_{RR} = \sqrt{\frac{2Q_{RR}(S+1)}{\frac{dI_C}{dt}\Big|_{t_{1on}<t<t_{2on}}}} \tag{5.14}$$

Combining Equation 5.14 and Equation 5.11, yields to Equation 5.15 [11]:

$$I_{RRM} = \sqrt{\frac{2Q_{RR}\frac{dI_C}{dt}\Big|_{t_{1on}<t<t_{2on}}}{(S+1)}} \tag{5.15}$$

According to Mohan et al. [11], the reverse recovery charge (Q_{RR}) is part of the total forward charge (Q_F). The latter is the charge stored within the diode when it is forward biased. This charge is removed during reverse recovery, by the reverse current. The charge stored during forward biasing is predominantly stored within the drift region especially in power diodes and is dependent on the diode's forward current (I_F). This dependence is related to the physical characteristics within the diode. According to Al-Naseem et al. [219] at low diode's forward current (I_F), Shockley-recombination dominates the diode's behavior, and hence the

dependence of the stored charge (Q_F) on the forward current (I_F) can be approximated as linear ($Q_F \propto I_F$). At intermediate diode's forward current (I_F), it depends mainly on injection efficiency of majority carriers and hence the forward charge (Q_F) is better approximated by a forward current (I_F) square root dependence ($Q_F \propto \sqrt{I_F}$). For large forward current (I_F), Auger recombination becomes the predominant process. This leads to a cube root dependence of the forward charge (Q_F) on the forward current (I_F) ($Q_F \propto \sqrt[3]{I_F}$). This is illustrated in Figure 5.17. Hence for small forward current (I_F), the forward charge (Q_F) is proportional to the forward current (I_F) as provided in 5.15 [11].

$$Q_F \propto I_F \tag{5.15}$$

But for intermediate forward current (I_F) values, a better relationship considers the fact, that injection efficiency usually dominates over the normal operating range of a power diode, and hence is provided by 5.16 [219].

$$Q_F \propto \sqrt{I_F} \tag{5.16}$$

The relationship between the forward charge (Q_F) and the recovery charge (Q_{RR}), depends on the diode's forward current rate of change (dI_F/dt). The higher the latter parameter (tending towards an infinite forward current change), the closer the reverse recovery charge (Q_{RR}) is to the forward charge (Q_F) [11]. Hence for large forward current rate of change (dI_F/dt) one can assume that:

$$Q_F \approx Q_{RR} \tag{5.17}$$

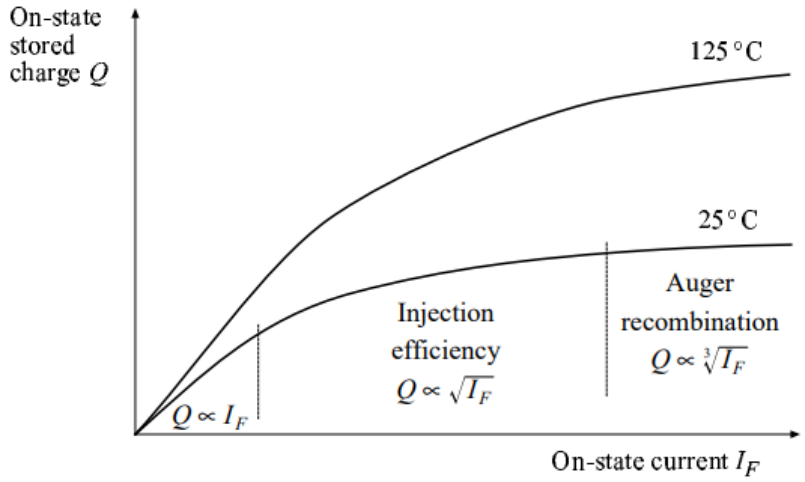


Figure 5.17 - Theoretical relationship of diode stored charge with on-state current, and corresponding dominant physical mechanism [219]

Hence for small forward current (I_F), the maximum reverse recovery time (t_{RR}) and maximum peak reverse recovery current (I_{RRM}) that can be attained, can be approximated by Equations 5.18 and 5.19 respectively.

$$t_{RR} = \sqrt{\frac{2\tau I_{C0}(S+1)}{\left.\frac{dI_C}{dt}\right|_{t_{1on}<t<t_{2on}}}} \tag{5.18}$$

$$I_{RR} = \sqrt{\frac{2\tau I_{C0}\left.\frac{dI_C}{dt}\right|_{t_{1on}<t<t_{2on}}}{(S+1)}} \tag{5.19}$$

Moreover, for intermediate diode's forward current (I_F), the maximum reverse recovery time (t_{RR}) and maximum peak reverse recovery current (I_{RRM}) that can be attained can be approximated by Equations 5.20 and 5.21 respectively.

$$t_{RR} = \sqrt{\frac{2\tau\sqrt{I_{C0}}(S+1)}{\left.\frac{dI_C}{dt}\right|_{t_{1on}<t<t_{2on}}}} \tag{5.20}$$

$$I_{RRM} = \sqrt{\frac{2\tau\sqrt{I_{C0}}\left.\frac{dI_C}{dt}\right|_{t_{1on}<t<t_{2on}}}{(S+1)}} \tag{5.21}$$

Equations 5.20 and 5.21 are evidencing a weak dependence of the reverse recovery time (t_{RR}) and the peak reverse recovery current (I_{RRM}) on the forward current for intermediate diode's forward current (I_F), with ($t_{RR} \propto \sqrt[4]{I_F}$) and ($I_{RRM} \propto \sqrt[4]{I_F}$). This relationship tends to get weaker for large values of diode's forward current (I_F). Hence for intermediate and large diode's forward current, both the reverse recovery time and the peak reverse recovery current can be modelled relatively accurate independent of the diode's forward current (I_F). On the other side the forward charge (Q_F) and hence the reverse recovery charge (Q_{RR}), has a direct dependence on the minority carrier lifetime (τ) under all diode's forward current (I_F) circumstances. Equation 5.22 describes the dependence of the minority carrier lifetime (τ), on the diode's parameters as proposed by Mohan et al. [11].

$$\tau = \frac{W_D^2}{(kT/q)\{\mu_n+\mu_p\}} \tag{5.22}$$

where W_D is the drift region width (m), k is the Boltzman constant 1.380649×10^{-23} J·K^{-1}, T is the temperature (K), q is the electronic charge $1.602\text{x}10^{-19}$C, μ_n is the electron mobility (m^2/Vs),

and μ_p is the hole mobility (m^2/Vs). These last two parameters, at room temperature and in moderately doped silicon (less than $10^{15}cm^{-3}$), have a typical value of 1500 cm^2/V-s and 500 cm^2/V-s respectively. Carriers' mobilities decrease with increasing temperature (T). In the above equation the drift region width (W_D), must be large enough to house the depletion region at its maximum expansion that is at the diode's breakdown voltage (BV_{BD}). This means that the drift region width (W_D) must be large enough and maximally equal to the width of the depletion region during breakdown $W(BV_{BD})$, where this latter parameter is provided by Equation 5.23 [11].

$$W(BV_{BD}) = \frac{2BV_{BD}}{E_{BD}} \tag{5.23}$$

where BV_{BD} is the diode's breakdown voltage and E_{BD} is the electric field across the depletion region during breakdown. This latter parameter for power diodes is generally in the order of 200 kV/cm to 300kV/cm [11]. This translates to a corresponding depletion region width during breakdown $W(BV_{BD})$ of $0.67x10^5 BV_{BD}$ to $1x10^5 BV_{BD}$. Hence the minority carrier lifetime (τ) provided by Equation 5.22 yields to Equation 5.24:

$$\tau = \frac{4\left(\frac{BV_{BD}}{E_{BD}}\right)^2}{(kT/q)\{\mu_n+\mu_p\}} \tag{5.24}$$

The above equation shows the predominant dependence of the minority carrier lifetime (τ) on the diode's breakdown voltage (BV_{BD}). The characterized internal IGBT free-wheeling diode is of the HEXFRED^{TM} diode technology. This technology is described as ultra-fast and ultra-soft, with a characteristic small peak reverse recovery current (I_{RRM}). Ultra-fast refers to the small reverse recovery time (t_{RR}). Ultra-soft means that the $t_{b(RR)}$ section of the reverse recovery is equal or greater than the $t_{a(RR)}$ section. This avoids the tendency to "snap-off" (the abrupt finish of the reverse recovery), during the $t_{b(RR)}$ portion of recovery, which leads to less oscillations after recovery and less EMI [209].

5.2.4 IGBT Piecewise Linear Modelling for Turn-On Transients during Phase 4

IGBT turn-on Phase 4, commences with the commutation of the diode, as the peak reverse recovery current (I_{RRM}) is reached, at $t_{3(ON)}$. This leads to a decay in the collector current (I_C), until the nominal output collector current ($I_{C0} \equiv I_L$) is reached. This is depicted in Figure 5.17. As the diode current falls, part of its stored charge is removed due to recombination. The amount of the charge removed, is a function of the free-wheeling diode's forward current rate

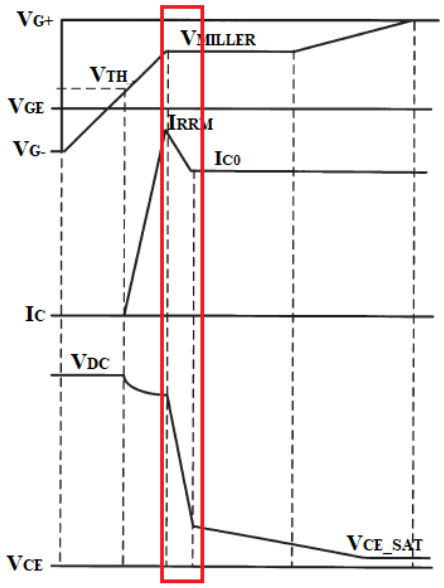


Figure 5.18 - IGBT Piecewise Linear Model Phase 4 Turn-On Waveforms (t_{3ON}–t_{4ON}) [215].

of change (dI_F/dt). The rate of decrease of the collector current (dI_C/dt) during this phase can be expressed linearly by Equation 5.25.

$$\left.\frac{dI_C}{dt}\right|_{t_{3(on)}<t<t_{4(on)}} = -\frac{I_{RR}}{t_{4(on)}-t_{3(on)}} \tag{5.25}$$

During this phase, the gate-emitter voltage (V_{GE}) is at the Miller voltage (V_{MILLER}), with the gate current predominantly flowing through the collector-gate capacitor (C_{CG}). Hence, the fall experienced in the collector-emitter voltage (V_{CE}), between $t_{3(ON)}$ and $t_{4(ON)}$, depends on the voltage rate of change across the collector-emitter capacitor (C_{CG}). Hence, the corresponding collector-emitter voltage rate of drop during Phase 4, can be approximated by considering the rate of change of the collector-gate capacitance voltage (dV_{Ccg}/dt). This is expressed in Equation 5.26.

$$\left.\frac{dV_{CE}}{dt}\right|_{t_{3(on)}<t<t_{4(on)}} = \frac{dV_{Ccg}}{dt} \tag{5.26}$$

The current through the collector-gate capacitance (C_{CG}), is given by Equation 5.27:

$$I_{Ccg} = C_{cg}\frac{dV_{Ccg}}{dt} \tag{5.27}$$

But the current through the collector-gate capacitance (C_{CG}) is made up of two components, the first component is due to the gate current (I_G), while the second component is due to the reverse–recovery current of the free-wheeling diode (D). During the reverse-recovery initial

stage (Phase 3), the gate-emitter capacitance (C_{GE}) is not high impedance as in the ideal free-wheeling diode case but continues to provide a low impedance path for the gate current (I_G), thus continuing to charge, as explained in Section 5.1.1. Hence, during this phase (Phase 4), the extra charge provided during the initial reverse recovery stage (Phase 3,) on the gate-emitter capacitance (C_{GE}) adds up to the gate current (I_G), through the available current path that is the gate-collector capacitance (C_{CG}). Thus, the gate current (I_G) can be provided by Equation 5.28, where V_{G+} is the maximum gate drive voltage, R_G is the gate resistance, and V_{GEIo} is the gate-emitter voltage at the end of the gate-emitter voltage (V_{GE}) spike due to reverse-recovery hence the Miller Voltage (V_{MILLER})

$$I_{Ccg\_due\_to\_gate\_current\_part} = \frac{V_{g+} - V_{GEIo}}{R_G} \tag{5.28}$$

$$\text{But } V_{GEIo} = V_{TH} + \frac{I_{C0}}{g_m} \tag{5.29}$$

where I_{C0} output collector current, g_m is the forward transconductance, and V_{TH} is the gate threshold voltage.

$$\text{Hence, } I_{Ccg\_due\_to\_gate\_current\_part} = \frac{V_{g+} - V_{th} - \frac{I_{C0}}{g_m}}{R_G} \tag{5.30}$$

The reverse recovery current contribution is based on the current provided by the gate-emitter capacitance (C_{GE}). This occurs, since during reverse recovery the gate-emitter voltage (V_{GE}) is not constant as in the ideal diode case when the gate-emitter voltage (V_{GE}) reaches the Miller voltage (V_{MILLER}) and remains constant but continues to rise with the same rate of change during Phase 2, ($dV_{GE}/dt_{(t1(ON)<t<t2(ON))}$), provided by Equation 5.31.

$$\left.\frac{dV_{GE}}{dt}\right|_{t_{1(on)}<t<t_{2(on)}} = \left.\frac{dI_C}{dt}\right|_{t_{1(on)}<t<t_{2(on)}} \Big/ g_m \tag{5.31}$$

Hence, the second component of the current through the collector-gate capacitance (C_{CG}) is provided by Equation 5.32.

$$I_{Ccg\_due\_to\_reverse\_recovery\_current\_part} = \frac{C_{ge}}{g_m}\left.\frac{dI_C}{dt}\right|_{t_{1(on)}<t<t_{2(on)}} \tag{5.32}$$

Thus, the current in the collector-gate capacitance (I_{Ccg}) is the summation of Equation 5.30 and Equation 5.32, provided by Equation 5.34.

$$I_{Ccg} = I_{Ccg\_due\_to\_gate\_current\_part} + I_{Ccg\_due\_to\_reverse\_recovery\_current\_part} \quad (5.33)$$

$$I_{Ccg} = \frac{V_{g+} - V_{th} - \frac{I_{C0}}{g_m}}{R_G} + \frac{C_{ge}}{g_m}\frac{dI_C}{dt}\Big|_{t_{1(on)}<t<t_{2(on)}} \quad (5.34)$$

Hence utilizing Equation 5.34 into Equation 5.27, the rate of change of the collector-emitter voltage rate of fall during Phase 4, ($dV_{CE}/dt_{(t3(ON)\,-\,t4(ON))}$), can be obtained, and is provided by Equation 5.35.

$$\frac{dV_{CE}}{dt}\Big|_{t_{3(on)}<t<t_{4(on)}} = \frac{-1}{C_{cg}}\left\{\frac{V_{g+} - V_{th} - I_{L/g_m}}{R_G} + \frac{C_{ge}}{g_m}\frac{dI_C}{dt}\Big|_{t_{1(on)}<t<t_{2(on)}}\right\} \quad (5.35)$$

Once the contribution of the gate-emitter capacitance (C_{GE}) due to reverse recovery seizes, the collector-gate capacitance (C_{CG}) continues to draw the gate current (I_G), during the collector-emitter voltage (V_{CE}) fall, experienced during Phase 4. This leads to the situation where the input gate current (I_G) does not contribute to charge the input gate capacitance (C_{IES}) further, thus holding the gate-emitter voltage (V_{GE}) at a flat level, called the Miller plateau. The duration of this plateau depends on the gate current (I_G) contributing to the rate of fall of the collector - emitter voltage (dV_{GE}/dt) during Phase 4, hence the rate of fall of the collector-gate capacitance (dV_{Ccg}/dt), as described by Equation 5.35, thus the discharge of the collector-gate capacitance (C_{CG}). An extended Miller plateau leads to a longer collector-emitter voltage (V_{CE}) fall, which increases the turn-on switching power dissipation [215]. Equation 5.20 is only providing a simplified behavioural linear equation describing Phase 4 and is not including the tailing effect of the collector-emitter voltage (V_{CE}), which requires a non-linear approach [213], [216].

5.2.5 IGBT Piecewise Linear Model Turn-On Transients during Phase 5

After the Miller-plateau region, the gate-emitter voltage (V_{GE}) continues to increase to its final on-state voltage (V_{G+}). During this phase, the collector-emitter voltage (V_{GE}),

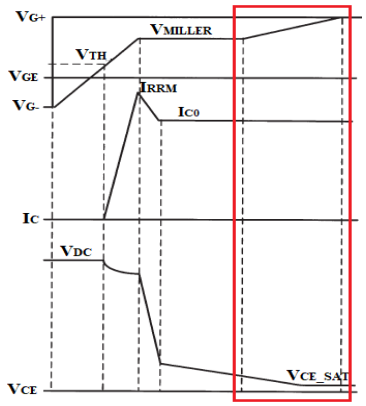


Figure 5.19 - IGBT Piecewise Linear Model Phase 4 Turn-On Waveforms (t_{4ON} onwards) [215].

reaches the collector-emitter on-state saturation voltage (V_{CE_SAT}), hence obtaining an output stage that can be represented with an on-state resistance as illustrated in Figure 5.9. Moreover, the collector current (I_C) would have already reached and stabilized at the output load current (I_{C0}).

5.2.6 IGBT Piecewise Linear Model Turn-Off Transients during Phase 1

The IGBT's turn-off reference transients are shown in Figure 5.20. The turn-off transients are generally characterized in the devices' datasheets by the turn-off delay time ($t_{d(off)}$), fall time (t_{fall}), and turn-off energy (E_{off}). Prior to starting the turn-off procedure, the gate terminal of the IGBT is at the maximum positive gate drive voltage (V_{G+}), the collector-emitter voltage (V_{CE}) is at the collector-emitter on-state saturation voltage (V_{CE_SAT}), the collector current (I_C) is equal to the set load current (I_{C0}) and the voltage across the free-wheeling diode junction capacitance (C_{JD}) is approximately equal to V_{CC}. The equivalent circuit to obtain turn-off transients linear equations [215], is illustrated in Figure 5.21. During Phase 1 ($t_{0(off)}$-$t_{1(off)}$), since the collector-gate capacitance (C_{CG}), is a non-linear capacitor and varies as a function of the collector-emitter voltage (V_{CE}), the collector voltage (V_C) rises slowly, because of the large input capacitance (C_{IES}), due to the large collector-gate capacitance (C_{CG}) at low collector-emitter voltage (V_{CE}). This is illustrated in Figure 5.5.

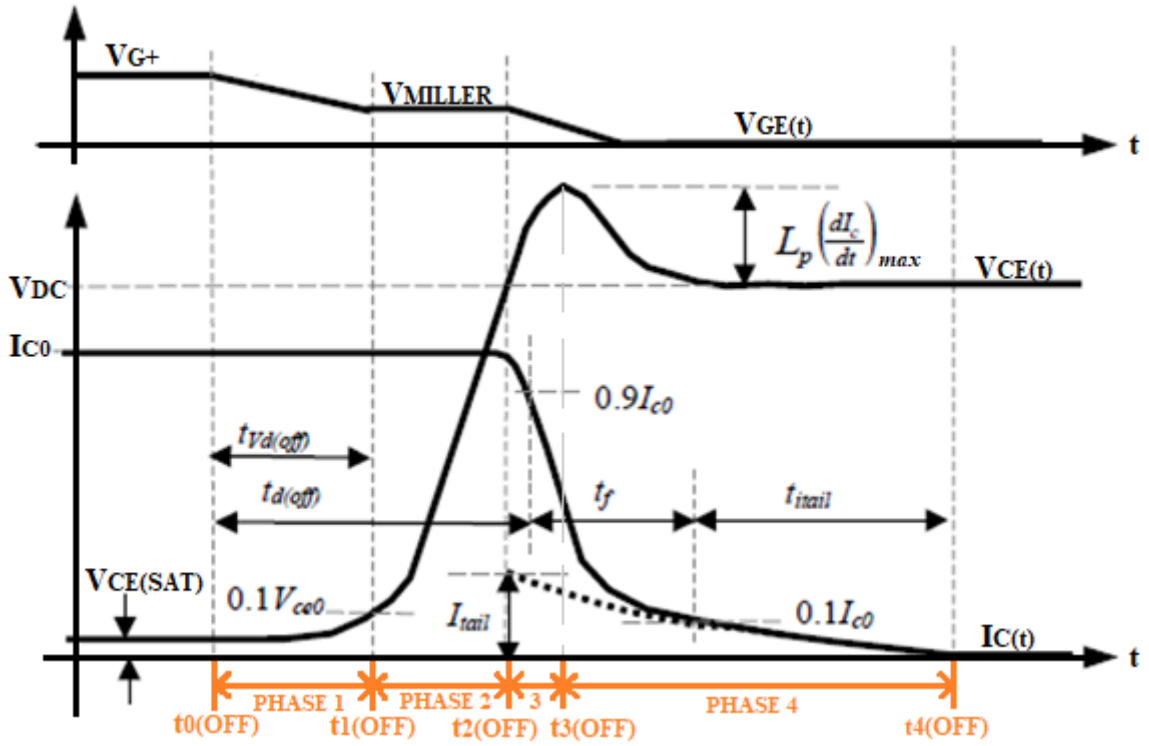


Figure 5.20 - IGBT Turn-Off Transient Reference Waveforms for Piecewise Linear and Non-Linear Modelling [213].

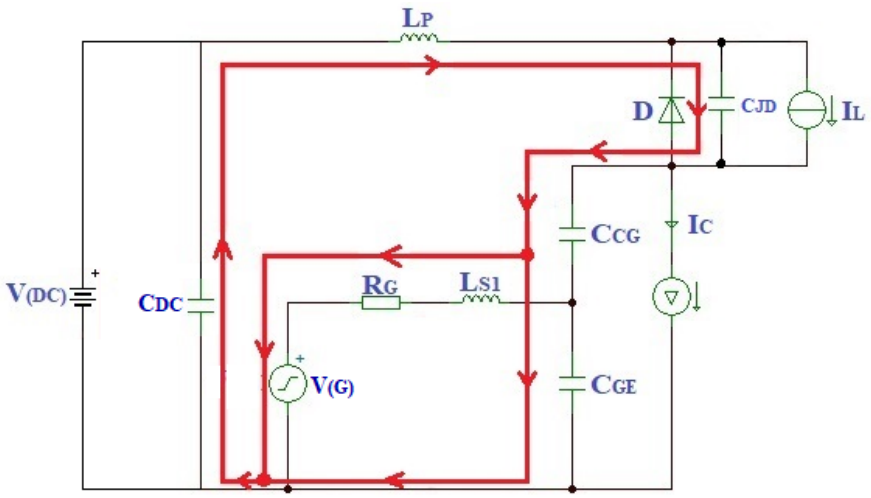


Figure 5.21 - IGBT Equivalent Circuit during Turn-Off Transients [215].

The IGBT's gate terminal during this phase starts to decrease from the maximum gate voltage (V_{G+}). The negative gate drive causes the input gate capacitance (C_{IES}) and hence the gate-emitter capacitance (C_{GE}) and the gate-collector capacitance (C_{CG}), to discharge through the gate resistance (R_G). This discharge causes the gate voltage (V_G) to drop progressively until the Miller plateau is reached, which occurs at $t_{1(off)}$ at the end of Phase 1.

During this phase the rate of rise of the collector-emitter voltage (dV_{CE}/dt) is essentially governed by the discharging of the collector-gate capacitance (C_{CG}) hence is equivalent to the collector-gate capacitance voltage rate of change (dV_{Ccg}/dt) which is provided by Equation 5.39 [217]. It is important to point out that during this phase the collector-emitter capacitance (C_{CG}) is C_{CG1}, as indicated in Figure 5.5.

$$I_{Ccg} = \frac{V_{GEIo} - V_{G-}}{R_G} \tag{5.36}$$

$$\text{But } V_{GEIo} = V_{TH} + \frac{I_{C0}}{g_m} \tag{5.37}$$

$$\left.\frac{dV_{CE}}{dt}\right|_{t_{0(off)}<t<t_{1(off)}} = \left.\frac{dV_{Ccg}}{dt}\right|_{t_{0(off)}<t<t_{1(off)}} = \frac{I_{Ccg}}{C_{cg}} \tag{5.38}$$

$$\left.\frac{dV_{CE}}{dt}\right|_{t_{0(off)}<t<t_{1(off)}} = \frac{V_{TH} + {}^{I_{C0}}/_{g_m} - V_{G-}}{R_g C_{cg}} \tag{5.39}$$

During this phase, since the collector-emitter voltage rate of change (dV_{CE}/dt) is relatively small, the collector-current (I_C) remains relatively unchanged and hence relatively equal to the output collector current (I_{C0}).

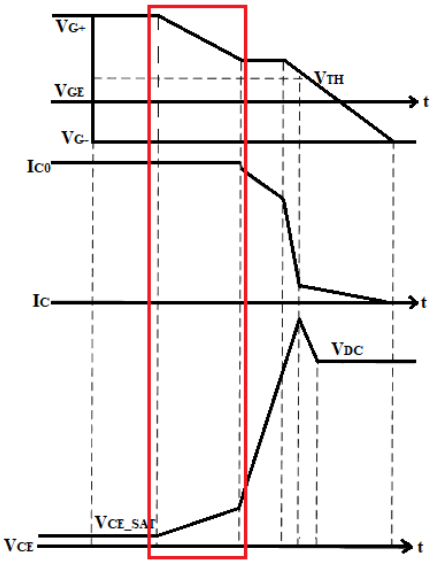


Figure 5.22 - IGBT Piecewise Linear Model Phase 1 Turn-Off Waveforms ($t_{0(ON)} - t_{1(ON)}$) [215].

5.2.7 IGBT Piecewise Linear Model Turn-Off Transients during Phase 2

During Phase 2, the collector-emitter voltage (V_{CE}), rises rapidly, after the slow initial rise experienced during Phase 1. Due to the substantial rise of the collector-emitter voltage (dV_{CE}/dt), the collector-gate capacitance (C_{CG}), decreases to a steady value corresponding to C_{CG2} as illustrated in Figure 5.5. During this phase, the gate voltage (V_G) tries to continue to decrease but is sustained by the discharge of the collector-gate capacitance (C_{CG}), hence resulting in a net constant gate voltage (V_G), the Miller plateau. The collector-emitter voltage rate of rise (dV_{CE}/dt) is essentially governed by the discharging of the collector-gate capacitance (C_{CG}) as in Phase 1, but with a lower collector-gate capacitance (C_{CG2}) hence a larger collector-emitter voltage rate of rise (dV_{CE}/dt) provided in Equation 5.40 [217].

$$\left.\frac{dV_{CE}}{dt}\right|_{t_{1(off)}<t<t_{2(off)}} = \frac{V_{TH}+{}^{I_{C0}}/_{g_m}-V_{G-}}{R_g C_{cg}} \tag{5.40}$$

During Phase 2, the collector-current (I_C), experiences a small decay. This is due the diode's junction capacitance (C_{JD}), which discharges during this phase, and is dependent on the collector-emitter voltage rise (dV_{CE}/dt), which is substantial during this phase producing a noticeable decay in the collector current (I_C) which is provided by Equation 5.42 [213].

$$\Delta I_C = -C_{JD}\left.\frac{dV_{CE}}{dt}\right|_{t_{1(off)}<t<t_{2(off)}} \tag{5.41}$$

$$\left.\frac{dI_C}{dt}\right|_{t_{1(off)}<t<t_{2(off)}} = -\frac{C_{JD}\left.\frac{dV_{CE}}{dt}\right|_{t_{1(off)}<t<t_{2(off)}}}{t_{2(off)}-t_{1(off)}} \tag{5.42}$$

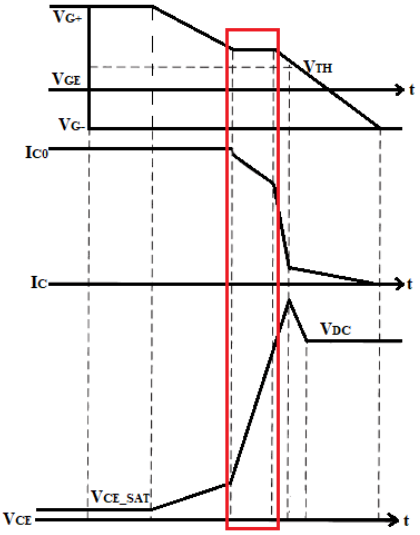


Figure 5.23 - IGBT Piecewise Linear Model Phase 2 Turn-Off Waveforms ($t_{1(ON)} - t_{2(ON)}$) [215].

5.2.8 IGBT Piecewise Linear Model Turn-Off Transients during Phase 3

Once the collector-emitter voltage (V_{GE}) reaches the collector-emitter output voltage (V_{DC}), the load current (I_L) transfers from the IGBT to the free-wheeling diode (D) when the latter is forward biased. Hence, due to this current transfer, the collector current (I_C) experiences a rapid decrease. This occurs simultaneously when the Miller plateau seizes to occur, and the gate voltage (V_G) continues to decrease. The collector current rate of decrease (dI_C/dt) depends on the rate of decrease of the gate-emitter voltage (dV_{GE}/dt) [217]:

$$g_m = \frac{I_C}{V_G} \quad \text{hence:} \left.\frac{dI_C}{dt}\right|_{t_{2(off)}<t<t_{3(off)}} = g_m \left.\frac{dV_G}{dt}\right|_{t_{2(off)}<t<t_{3(off)}} \tag{5.43}$$

$$\text{but} \left.\frac{dV_G}{dt}\right|_{t_{2(off)}<t<t_{3(off)}} = \frac{\Delta V_G}{\text{Time Constant}} = \frac{(V_{g-} - V_{TH}) - \frac{I_L}{g_m}}{Time\ Constant\ R_G C_{ies} + Time\ Constant\ g_m L_{S1}} \tag{5.44}$$

$$\text{Hence} \left.\frac{dI_C}{dt}\right|_{t_{2(off)}<t<t_{3(off)}} = \frac{g_{m(}V_{g-} - V_{TH}) - I_L}{R_G C_{ies} + g_m L_{S1}} \tag{5.45}$$

The collector current rate of decrease (dI_C/dt) causes an overshoot in the collector-emitter voltage (V_{CE}) due to the stray inductance L_p. Hence, the corresponding rate of increase of the collector-emitter voltage (dV_{CE}/dt), during this phase, is provided by Equation 5.47. Hence this phase characterizes the switch-off phase controlled by the IGBT's intrinsic MOSFET.

$$\Delta V_{CE} = L_p \left.\frac{dI_C}{dt}\right|_{t_{2(off)}<t<t_{3(off)}} \tag{5.46}$$

$$\text{Where} \left.\frac{dV_{CE}}{dt}\right|_{t_{2(off)}<t<t_{3(off)}} = -\frac{L_p \left.\frac{dI_C}{dt}\right|_{t_{2(off)}<t<t_{3(off)}}}{t_{3(off)} - t_{2(off)}} \tag{5.47}$$

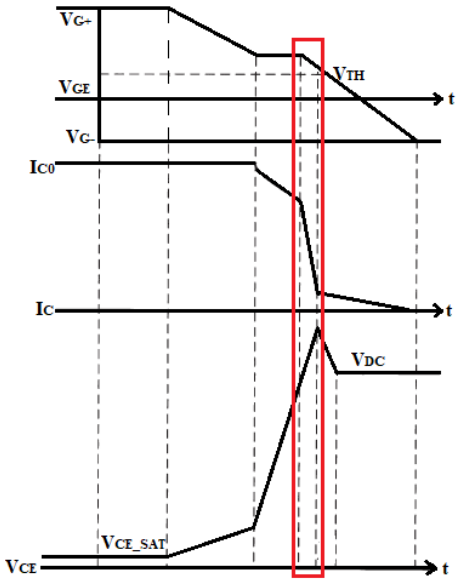


Figure 5.24 - IGBT Piecewise Linear Model Phase 3 Turn-Off Waveforms ($t_{2(ON)} - t_{3(ON)}$) [215].

5.2.9 IGBT Model Turn-Off Transients during Phase 4

Phase 4 highlights the salient turn-off difference, between that of a power MOSFET and that of an IGBT. When the gate-emitter voltage (V_{GE}) drops below the gate-emitter threshold voltage (V_{TH}), the collector current (I_C) does not extinguish immediately, instead it decays gradually, hence characterised by a "tail current". The extent and length of the "tail current" is determined by the IGBT's manufacturing technology as its presence is greatly influenced by the doping level of the N^- drift region and operational conditions as this is significantly influenced by the IGBT's junction temperature (T_J). The "tail current" is problematic to model through a linear equation and is commonly modelled in literature as an exponential decay, as described by Equation 5.48 [218].

$$I_C(t) = \alpha I_{C0} e^{-\frac{(t-t_O)}{\tau}} \tag{5.48}$$

Here α is the amplification coefficient of the BJT, I_{C0} is the IGBT on-state current, t_0 is the starting instant of the "tail current", and τ is the time constant of the "tail current". The amplification coefficient is dependent on the junction temperature (T_J), having a positive temperature coefficient. This means that if the junction temperature (T_J) increases, the initial collector current (I_C) at which the "tail" transient waveform starts, increases, as well as affecting the corresponding time constant τ. During this phase, the collector-emitter voltage (V_{CE}) is at the collector-emitter output voltage (V_{DC}). Tables 5-1 and 5-2 provide a summary of the Turn-On and Turn-Off transients linear model equations, except for the tail current, where an exponential model equation was proposed.

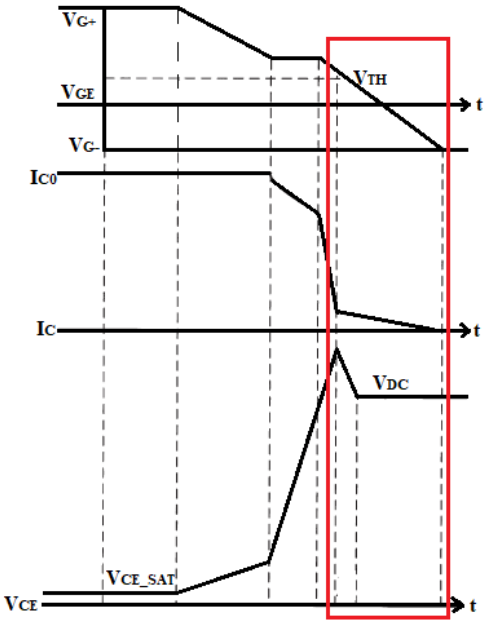


Figure 5.25 - IGBT Piecewise Linear Model Phase 2 Turn-Off Waveforms ($t_{3(ON)} - t_{4(ON)}$) [215].

Transient Phase	IGBT Turn-On Transient Linear Model Equations	
	V_{CE} Transient	I_C Transient
Phase 1	$V_{CE} = V_{DC}$	$I_C = 0A$
Phase 2	$\frac{dV_{CE}}{dt}(\text{Phase 2}) = -L_P \frac{\frac{dI_C}{dt}(Phase\ 2)}{(t_{2on} - t_{1on})}$	$\frac{dI_C}{dt}(\text{Phase 2}) = \frac{g_m(V_{G+} - V_{TH})}{(R_G C_{ies} + g_m L_{S1})}$
Phase 3	$\frac{dV_{CE}}{dt}(\text{Phase 3}) = -L_P \frac{\frac{dI_C}{dt}(Phase\ 2)}{(t_{2on} - t_{1on})}$	$\frac{dI_C}{dt}(\text{Phase 3}) = \frac{g_m(V_{G+} - V_{TH})}{(R_G C_{ies} + g_m L_{S1})}$ $I_{RRM} = t_{a(rr)} \frac{dI_C}{dt}_{t_{1on}-t_{2on}}$ $t_{RR} = \sqrt{\frac{2Q_{RR}(S+1)}{\frac{dI_C}{dt}_{t_{1on}-t_{2on}}}}$ $I_{RRM} = \sqrt{2Q_{RR} \frac{dI_C}{dt}_{t_{1on}-t_{2on}} (S+1)}$
Phase 4	$\frac{dV_{CE}}{dt}(Phase\ 4) = \frac{-1}{C_{cg}}\{\frac{V_{g+} - V_{th} - I_{\frac{L}{g_m}}}{R_G} + \frac{C_{ge}}{g_m}\frac{dI_C}{dt}(Phase\ 2)\}$	$\frac{dI_C}{dt}(Phase\ 4) = -\frac{I_{RR}}{t_{4(on)} - t_{3(on)}}$
Phase 5	$V_{CE} = V_{CE\_SAT}$	$I_C = I_{C0}$

Table 5-1 – IGBT Turn-On Transient Linear Model Equations Summary

Transient Phase	IGBT Turn-Off Transient Linear Model Equations	
	V_{CE} Transient	I_C Transient
Phase 1	$\frac{dV_{CE}}{dt}(Phase\ 1) = \frac{V_{TH} + {I_{C0}}/{g_m} - V_{G-}}{R_g C_{cg2}}$	$I_C = I_{C0}$
Phase 2	$\frac{dV_{CE}}{dt}(Phase\ 2) = \frac{V_{TH} + {I_{C0}}/{g_m} - V_{G-}}{R_g C_{cg1}}$	$\frac{dI_C}{dt}(Phase\ 2) = -\frac{C_{JD}\frac{dV_{CE}}{dt}(Phase\ 2)}{t_{2(off)} - t_{1(off)}}$
Phase 3	$\frac{dV_{CE}}{dt}(\text{Phase 3}) = -\frac{L_p\frac{dI_C}{dt}(t_{2(off)} - t_{3(off)})}{t_{3(off)} - t_{2(off)}}$	$\frac{dI_c}{dt}(Phase\ 3) = \frac{g_{m(}V_{g-} - V_{TH}) - I_L}{R_G C_{ies} + g_m L_{S1}}$
Phase 4	$V_{CE} = V_{DC}$	$I_C(t) = \alpha I_{C0} e^{-\frac{(t-t_o)}{\tau}}$

Table 5-2 - IGBT Turn-On Transient Linear Model Equations Summary

5.2.10 IGBT Piecewise Linear Model Parameters Extraction and Results

The above piecewise linear IGBT transients' model equations were implemented within MATLAB and superimposed on the measured transients. The different parameters utilized in the above equations, were mainly extracted either through the manufacturers' datasheets or through experimental measurements. The parasitic capacitors were the most challenging to determine as their values are dependent on the collector-emitter voltage (V_{CE}) as evidenced by Figure 7 of the manufacturer's datasheet [209]. This is especially valid for the collector-gate capacitor (C_{CG}), where distinct optimized values were employed for Turn-On and Turn-Off transient phases, with a corresponding low or high collector-emitter voltage (V_{CE}). Since these values were obtained from the IRG4BC30KDPBF IGBT manufacturer's datasheet, they were optimized to better reflect the measured transients, within the variability range provided by the datasheet. The junction capacitance of the free-wheeling diode (C_{JD}) was obtained through the parasitic output capacitance (C_{OES}), of the utilized IGBT since the internal diode of this same IGBT was employed for this purpose. The output capacitance of the IGBT (C_{OES}) is given by Equation 5.49, where C_{CE} is the collector-emitter capacitance and C_{CG} is the collector-gate Miller capacitance.

$$C_{OES} = C_{CE} + C_{CG} \tag{5.49}$$

The output capacitance (C_{OES}) is essentially determined by shorting the emitter terminal with the gate terminal, which is essentially the connection of the IGBT when utilized as a diode. Hence the IGBT's diode junction capacitance (C_{JD}) is equal to the collector emitter capacitance (C_{CE}) which can be obtained through Equation 5.50.

$$C_{JD} = C_{OES} - C_{CG} \tag{5.50}$$

The main stray inductance L_P was modelled through the series combination of the parasitic collector inductance (L_C), the parasitic emitter inductance (L_E), the combined stray inductance of the decoupling DC link capacitors (C_{IN}), and the DC Voltage PCB power plane and ground plane loop inductance of the implemented Double Pulse test circuit, as provided by Equation 5.51.

$$L_p = L_C + L_E + L_{DC\_BUS} + L_{Cin} \tag{5.51}$$

The IRG4BC30KDPBF IGBT's stray inductances were obtained from the manufacturer datasheet. Since only the emitter stray inductance was quoted (7.5nH), the collector as well as the gate stray inductances were assumed to be the same value, and ought to be in the order of magnitude of the emitter inductance (L_E), to reflect the measured transients. The equivalent series inductance (ESL) of the decoupling DC capacitances were obtained from the capacitors' manufacturer datasheet. For the EPCOS B32778G 60µF 800V DC link capacitors, the ESL at 1MHz (the maximum frequency ESL data available) is 15.6nH, while that for the EPCOS B32652 100nF 1kV polypropylene capacitors at 1MHz is 15.9nH. Hence the combined shunt stray inductance for the DC link capacitors (L_{Cin}) is 2.63nH. The power planes loop inductance, which was the most predominant of the three, was measured via the Keysight E4990A impedance-network analyser, measured at a frequency of 100MHz, since typical measured rise times and fall times are in the 10ns range. The combined plane inductance was determined to be 82.56nH. This resulted in a combined primary stray inductance (L_P) of 100.2nH. It is important to point out that this combined primary stray inductance value is not exact especially when considering that it was computed with some assumed inductances values and at some unknown and different measurement frequency. The scope was to provide an indicative value where the primary stray inductance (L_P) lies. The combined input gate stray inductance (L_{S1}) was modelled as the series combination of the output parasitic inductance of the gate driver output (L_{DRV_OUT}) and the parasitic IGBT gate inductance (L_G) and emitter inductance (L_E). The driver output was specified by the manufacturer (upon request as was not available in datasheet), to have a typical value of 3.5nH. This resulted in a combined input gate stray inductance (L_{S1}) to 18.5nH. Again, this is an inexact value and had to be optimized to a model value in the range of 10nH to 26.4nH to reflect the measured data as discussed in Section 5.4.3.

$$L_{S1} = L_{DRV\_OUT} + L_G + L_E \tag{5.52}$$

The threshold voltage (V_{TH}) and the forward transconductance (g_m), were obtained experimentally as described in Chapter 3 and verified with the quoted general values for the IGBT's manufacturer datasheet. Table 5-3 provides the values of the required model parameters and corresponding extraction description. Measured values are for IGBT Sample 14 when new, quoted in Chapter 4, which will be utilized as the reference sample, throughout the transient modelling analysis including ageing effects, conducted throughout this chapter, unless stated otherwise. The corresponding start and end time values of each turn-on and turn-off phase, were obtained from the measured transients through the Double Pulse test procedure, described in Chapter 5. These are tabulated in Table 5-4. Figures 5.26 and 5.27 illustrate the superimposed model equations on the measured transients of IGBT Sample 14. The reverse recovery time (t_{RR}), first phase of reverse recovery time ($t_{a(RR)}$), second phase of reverse recovery time ($t_{b(RR)}$), the peak reverse recovery current (I_{RRM}) were obtained and verified experimentally from the measured transients through the Double Pulse test procedure, described in Chapter 4.

IGBT PIECEWISE LINEAR MODEL PARAMETERS			
Parameter	**Symbol**	**Value**	**Extraction Description**
Threshold Voltage	V_{TH}	5.3185V	Measured experimentally & datasheet
Forward Transconductance	g_m	6.105S	Measured experimentally & datasheet
Collector-Gate Capacitance @ Low V_{CE}	C_{CG1}	2.6nF	Manufacturer datasheet
Collector-Gate Capacitance @ High V_{CE}	C_{CG2}	31.5pF	Manufacturer datasheet
Gate-Emitter Capacitance @ High V_{CE}	C_{GE}	900pF	Manufacturer datasheet
Diode Junction Capacitance	C_{JD}	160pF	Manufacturer datasheet
Gate Inductance	L_G	7.5nH	Assumed
Collector Inductance	L_C	7.5nH	Assumed
Emitter Inductance	L_E	7.5nH	Manufacturer datasheet
DC Link Capacitance Stray Inductance	L_{Cdc}	2.63nH	Manufacturer datasheet
DC PCB Power Bus Inductance	L_{DC_BUS}	82.56nH	Measured @100MHz
Gate Driver Output Stray Inductance	L_{DRV_OUT}	3.5nH	Manufacturer
Primary Stray Inductance	L_P	100.2nH	Approximated (Measured & datasheets)
Secondary Stray Inductance	L_{S1}	26.4nH	Approximated (Manufacturer datasheets)
Low Side Gate Voltage	V_{G-}	0V	Test Condition and measured
High Side Gate Voltage	V_{G+}	15V	Test Condition and measured
Gate Resistance Off	$R_{G(OFF)}$	10.2Ω	Test Condition and measured
Gate Resistance On	$R_{G(ON)}$	33.2Ω	Test Condition and measured
DC Link Voltage	V_{DC}	480V	Test Condition and measured
Collector-Emitter On-State Saturation Voltage	V_{CE_SAT}	2.21V	Measured experimentally & datasheet
On-State Load Current	I_{C0}	16A	Test Condition and measured
Amplification Coefficient of parasitic IGBT's BJT	α	0.385	Based on transient measurement
Start of tail current	t_0	2.028μs	Based on transient measurement
Collector-Current tail time constant	τ_{TAIL}	0.048μs	Based on transient measurement

Table 5-3 - IGBT Piecewise Linear Model Parameters (Measured values for IGBT Sample 14 NEW)

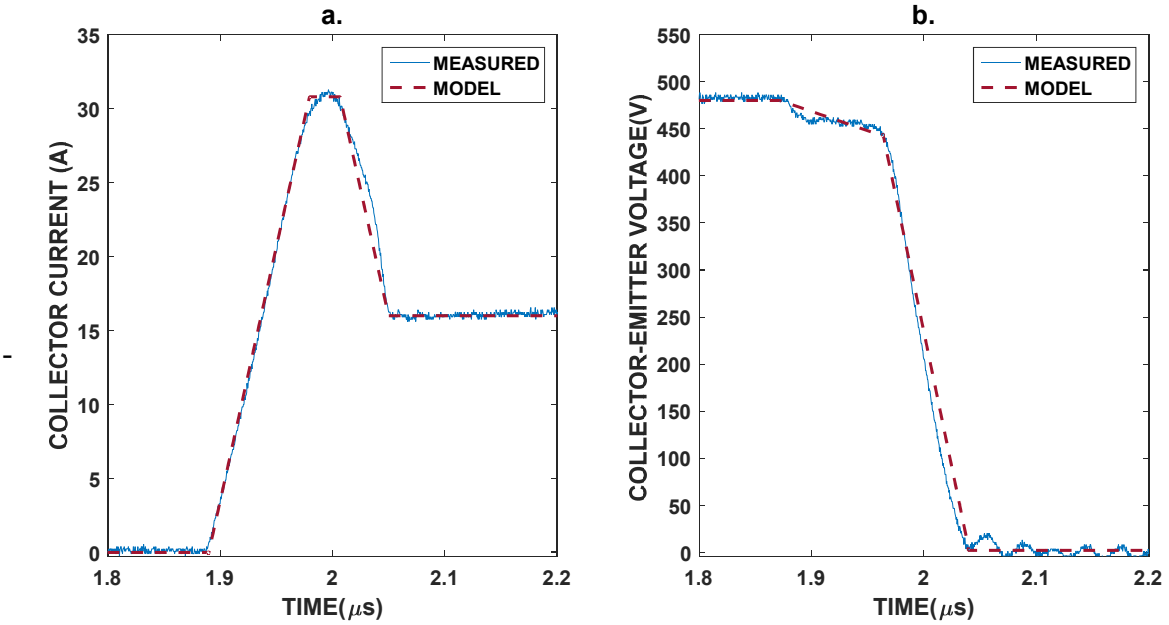


Figure 5.26 – IGBT Turn-On Piecewise Linear Model for IGBT Sample 14 (vNEW) (a) Collector Current (I_C) Transient (b) Collector-Emitter Voltage (V_{CE}) Transient

Table 5-4 tabulates the measured time parameters for the turn-on and turn-off transients as per Figure 5.12 and Figure 5.20, focussing on the phases which manifest the measured transient in a nearly linear manner. The tabulated results evidence that the measured and modelled collector-emitter voltage rate of change (dV_{CE}/dt) and collector current rate of change (dI_C/dt) correlate relatively well. The main discrepancies manifest in the turn-on collector-emitter voltage rate of change (dV_{CE}/dt) Phase 2 and Phase 3. This is since, these phases have been modelled through an overall single linear equation, while the actual transient measurement manifest through two distinct nearly linear stages

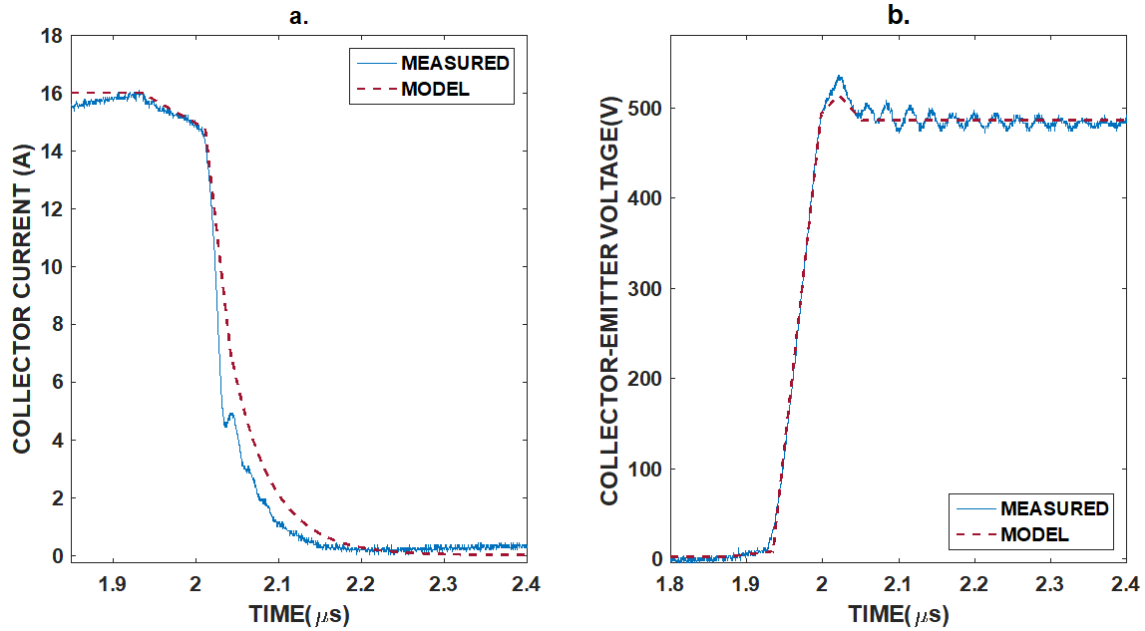


Figure 5.27 - IGBT Turn-Off Piecewise Linear Model for IGBT Sample 14 (vNEW) (a) Collector Current (I_C) Transient (b) Collector-Emitter Voltage (V_{CE}) Transient

TRANSIENT STAGE	TIME PARAMETER	COLLECTOR CURRENT (I_C) TRANSIENT	COLLECTOR-EMITTER VOLTAGE (V_{CE}) TRANSIENT
TURN-ON	$t_{0(ON)}$	1.600µs	1.600µs
	$t_{1(ON)}$	1.890µs	1.872µs
	$t_{2(ON)}$	1.980µs	1.964µs
	$t_{3(ON)}$	2.007µs	2.007µs
	$t_{4(ON)}$	2.040µs	2.040µs
TURN-OFF	$t_{0(OFF)}$	1.874µs	1.874µs
	$t_{1(OFF)}$	1.936µs	1.935µs
	$t_{2(OFF)}$	2.012µs	1.999µs
	$t_{3(OFF)}$	2.028µs	2.022µs
	$t_{4(OFF)}$	2.150µs	2.152µs

Table 5-4 – Measured Time Parameters for IGBT Sample 14 (vNEW) Turn-On and Turn-Off Transients with reference to Figure 5.12 and Figure 5.19 respectively.

TRANSIENT STAGE	TIME PARAMETER	COLLECTOR CURRENT RATE OF CHANGE (dI_C/dt) MEASURED (A/µs)	COLLECTOR CURRENT RATE OF CHANGE (dI_C/dt) MODEL (A/µs)
TURN-ON	Phase 2	333.87	343.93
	Phase 3	333.87	343.93
	Phase 4	-443.32	-325.31
TURN-OFF	Phase 2	-16.77	-16.11
	Phase 3	-472.58	-254.33

Table 5-5 – Collector Current Rate of Change (dI_C/dt) for IGBT Sample 14 Measured vs Model.

TRANSIENT STAGE	TIME PARAMETER	COLLECTOR-EMITTER VOLTAGE RATE OF CHANGE (dV_{CE}/dt) MEASURED (V/µs)	COLLECTOR-EMITTER VOLTAGE RATE OF CHANGE (dV_{CE}/dt) MODEL (V/µs)
TURN-ON	Phase 2	-1350.11	-411.23
	Phase 3	-260.86	-411.23
	Phase 4	-6796.47	-5774.3
TURN-OFF	Phase 1	88.19	92.79
	Phase 2	7885.71	7652.20
	Phase 3	1826.44	2083.00
	Phase 4	-1766.33	-2083.00

Table 5-6 – Collector-Emitter Voltage Rate of Change (dV_{CE}/dt) for IGBT Sample 14 Measured vs Model.

Table 5-7 shows the measured and calculated values of the different reverse recovery parameters. The reverse recovery charge (Q_{RR}) was modelled via the approximation provided by Equation 5.12, utilizing the measured reverse recovery time (t_{RR}) and the measured peak reverse recovery current (I_{RRM}). The measured reverse recovery charge (Q_{RR}) was obtained by integrating the area under the turn-on collector current (I_C) overshoot which corresponds to the reverse recovery transient phase. This highlights the proximity of the model and the measured values. The model value of the peak reverse recovery current (I_{RRM}) was obtained by utilizing Equation 5.15 with the model value of the reverse recovery charge (Q_{RR}), the modelled turn-on collector current rate of change (dI_C/dt) during Phase 2 (listed in Table 5-5), the measured first phase of the reverse recovery time ($t_{a(RR)}$) with a corresponding value of 58ns, and the measured second phase of the reverse recovery current ($t_{b(RR)}$) with a corresponding value of 60ns. The last two parameters were utilized to quantify the internal IGBT diode's softness factor (S) which was determined to be 1.034. The same procedure was conducted to obtain the reverse recovery time (t_{RR}) but utilizing Equation 5.14. Again, tabulated results show the proximity of the measured and the model parameters values. To determine the peak reverse recovery current (I_{RRM}), Jin et al. [215], proposed a model equation on the lines of Equation 5.19, including the dependence of this latter parameter on the diode's forward current (I_F). The proposed model equation did not include the diode's softness factor (S) and included the minority carrier lifetime (τ) parameter but providing minimal information how this parameter was determined.

Thus the minority carrier lifetime (τ) was approximated using Equation 5.24, with temperature (T) at 298.15K (25°C) reflecting the IGBT's case temperature (T_C) during measurement, electronic charge (q) at 1.602×10^{-19}C, Boltzmann Constant (k) at 1.381×10^{-23} m^2 kg s^{-2} K^{-1}, the typical electric field across the depletion region at break down voltage (E_{BD}) at 20MV/m, and the typical carriers' mobility ($\mu_n+\mu_p$) at $0.2 m^2$/V-s. This translates to a minority carrier lifetime (τ) approximation to $1.946 \times 10^{-12}(BV_{BD})^2$.

REVERSE RECOVERY PARAMETERS DESCRIPTION	SYMBOL	MEASURED	MODEL
Reverse Recovery Time	t_{RR}	118ns	104.07ns
Peak Reverse Recovery Current	$I_{(RMM)}$	15.52A	17.59A
Reverse Recovery Current Charge	Q_{RR}	1141.6nC	915.68nC

Table 5-7 – Reverse Recovery Parameters for IGBT Sample 14 Measured vs Model.

The utilized collector-emitter IGBT breakdown voltage (BV_{CE0}) quoted in the corresponding datasheet [209], is at 600V DC. The same value was assumed in this analysis, for the internal IGBT diode's breakdown voltage since it is internally connected in parallel to the IGBT structure. Table 5-8 tabulates the resultant values of the peak reverse recovery current (I_{RRM}) and the reverse recovery time (t_{RR}), for the different model equations derived in section 5.2.3, with different diode's reverse recovery charge (Q_{RR}) dependence on the forward current ($I_F \equiv I_{C0}$). The utilized diode forward current (I_F) is the output collector current (I_{C0}) as set during the Double Pulse test procedure, that is 16A. The turn-on Phase 2 collector current rate of change (dI_C/dt) was taken as the one determined by the implemented linear piecewise model as quoted in Table 5-5, that is 343.93A/μs. The softness factor (S) was taken as 1.034, as determined earlier.

The results in Table 5-8 indicate that for the internal IGBT diode, as the dependence on the diode's forward current ($I_F \equiv I_{C0}$) diminishes, the peak reverse recovery current (I_{RRM}) and reverse recovery time (t_{RR}) get closer to the measured parameters. When the diode forward current ($I_F \equiv I_{C0}$) was omitted from the model equations as indicated by Al-Naseem et al. [219], the resultant values of the peak reverse recovery current (I_{RRM}) and reverse recovery time (t_{RR}) are relatively congruent to the corresponding measured values as tabulated in Table 5-9. This analysis indicates that for the tested internal IGBT diode, the weaker the dependence of the reverse recovery charge (Q_{RR}) on the diode's forward current ($I_F \equiv I_{C0}$), the more consistent the model equations to the actual measurements are.

This latter diode's reverse recovery analysis and the utilized model equations are approximate estimates in several respects. They are based on an approximate analysis of an abrupt junction diode. Secondly, in the above analysis the drift region width was taken to be the minimum allowable to accommodate the worst-case width of the depletion region during the reverse breakdown voltage (BV_{BD}). If the drift region width is larger, it will make the estimates larger by the same amount. Third, this latter analysis was based on the approximation that the reverse recovery charge (Q_{RR}) and the forward charge (Q_F) are equal. This approximation is true for extensive values of the forward current rate of change (dI_F/dt). Thus, the above reverse recovery estimates are subject to inaccuracies, but are reliable in indicating general trends.

Relationship Q_{RR} with I_F	I_{RRM} Model Equation	I_{RRM} (A) Approx.	t_{RR} Model Equation	t_{RR} (ns) Approx.
$Q_{RR} \propto I_F$	$I_{RRM} = \sqrt{\frac{2\tau I_{C0} \left.\frac{dI_C}{dt}\right\|_{t_{1on}<t<t_{2on}}}{(S+1)}}$	61.57	$t_{RR} = \sqrt{\frac{2\tau I_{C0}(S+1)}{\left.\frac{dI_C}{dt}\right\|_{t_{1on}<t<t_{2on}}}}$	364.10
$Q_{RR} \propto \sqrt{I_F}$	$I_{RRM} = \sqrt{\frac{2\tau \sqrt{I_{C0}} \left.\frac{dI_C}{dt}\right\|_{t_{1on}<t<t_{2on}}}{(S+1)}}$	30.78	$t_{RR} = \sqrt{\frac{2\tau \sqrt{I_{C0}}(S+1)}{\left.\frac{dI_C}{dt}\right\|_{t_{1on}<t<t_{2on}}}}$	182.05
$Q_{RR} \propto \sqrt[3]{I_F}$	$I_{RRM} = \sqrt{\frac{2\tau \sqrt[3]{I_{C0}} \left.\frac{dI_C}{dt}\right\|_{t_{1on}<t<t_{2on}}}{(S+1)}}$	24.43	$t_{RR} = \sqrt{\frac{2\tau \sqrt[3]{I_{C0}}(S+1)}{\left.\frac{dI_C}{dt}\right\|_{t_{1on}<t<t_{2on}}}}$	144.49
Q_{RR} not dependant on I_F	$I_{RRM} = \sqrt{\frac{2\tau \left.\frac{dI_C}{dt}\right\|_{t_{1on}<t<t_{2on}}}{(S+1)}}$	15.39	$t_{RR} = \sqrt{\frac{2\tau(S+1)}{\left.\frac{dI_C}{dt}\right\|_{t_{1on}<t<t_{2on}}}}$	91.02

Table 5-8 - Reverse Recovery Current Modelling Dependence on the Forward Current

5.2.11 Limitations of the IGBT Linear Piecewise Model

The above IGBT linear piecewise model provides a simplified behavioral model of the turn-on and turn-off waveforms of the IGBT. In relation to the transients' phases described earlier, the linear piecewise model provides a relatively accurate approximation of the IGBT turn-on and turn-off transients when new, during the following phases:

- Turn-On Transient
    - Collector Current (I_C) Phase 1
    - Collector Current (I_C) Phase 2
    - Collector Current (I_C) Phase 5
    - Collector-Emitter Voltage (V_{CE}) Phase 1
    - Collector-Emitter Voltage (V_{CE}) Phase 2
    - Collector-Emitter Voltage (V_{CE}) Phase 5
- Turn-Off Transient
    - Collector Current (I_C) Phase 1
    - Collector Current (I_C) Phase 2
    - Collector Current (I_C) Phase 3
    - Collector-Emitter Voltage (V_{CE}) Phase 1
    - Collector-Emitter Voltage (V_{CE}) Phase 2

Other phases can be marginally modelled through linear equations. These include:

- The reverse recovery current transient during the turn-on collector current (I_C) (Phase 3 and Phase 4), cannot be modelled appropriately just through linear equations, leading to a truncation of the linear piecewise model, as clearly indicated in Figure 5.26,
- The drop in the turn-on collector-emitter voltage (V_{CE}) due to the stray inductance (L_P) (Phase 2 and Phase 3) can be marginally modelled through linear equations as it follows a non-linear decay.

- The fast drop in the turn-on collector-emitter voltage (V_{CE}) Phase 4, even though predominantly linear, it starts to include non-linearities towards the end of the decay.
- The voltage overshoot in the turn-off collector-emitter voltage (V_{CE}) Phase 3 and Phase 4, due to the stray inductance (L_P), can be marginally modelled through linear equations.
- The turn-off collector current (I_C) "tail current", is unfeasible to model linearly, being the most distinctive non-linear stage.

5.3 IGBT Switching Transients Non-Linear Modelling

This section will present the non-linear model equations representing the different IGBT switching transient phases, when the IGBT is new. The approach is based on the method presented by Rajapakse et al. [213] and will be discussed and compared in relation to the measured IGBT transients, obtained during the Double-Pulse test procedure as described in Chapter 5. Figure 5.12 and 5.20 will be again utilized as the reference turn-on and turn-off figures during this discussion. The approach is analogous to the approach taken for the linear piecewise modelling, that is providing model equations for each phase of the turn-on and turn-off transient collector current (I_C) and collector-emitter voltage (V_{CE}) but taking into consideration the different transients' non-linearities. It is important to highlight that the non-linear transient modelling is based on modelling the shape of the different waveforms from a transient analysis point of view rather than from an equivalent circuit analysis point of view, with the aim of providing a better representation of the IGBT's switching transients that can be integrated in ETP software.

5.3.1 IGBT Non-Linear Model for Turn-On Transients during Phase 1

In relation to Figure 5.12, during Phase 1, the collector-current (I_C) is at 0A while the collector-emitter voltage (V_{CE}), is at the output DC link voltage (V_{DC}).

$$V_{CE}|_{t0<t<t1} = V_{DC} \tag{5.53}$$

$$I_C|_{t0<t<t1} = 0 \tag{5.54}$$

5.3.2 IGBT Non-Linear Model for Turn-On Transients during Phase 2

During the turn-on transient Phase 2, the collector current (I_C) and collector-emitter voltage (V_{CE}) are modelled with an exponential increase and decay respectively. Equation 5.55 describes the corresponding exponential increase for the collector current (I_C) during this phase.

$$I_C(t) = I_{2(on)}(1 - e^{-\alpha_{2(on)}(t-t_{1(on)})}) \quad (5.55)$$

The steep increase of the collector current (I_C) during this phase, makes the exponential increase to reflect an almost linear growth. Hence the parameter $I_{2(on)}$, was approximated to be hundred times the output collector current (I_{C0}) as described by Equation 5.56, to reflect this steep increase.

$$I_{2(on)} \approx 100(I_{c0}) \quad (5.56)$$

The parameter $\alpha_{2(on)}$ is related to the IGBT's rise time (t_r), that is the time between when the collector current (I_C)is at 10% to 90% of the final on-state output collector current (I_{C0}). Due to this phase's linearity, the rise time (t_r) reflects 80% of the time duration of Phase 2, where Phase 2 reflects the time required for the collector current (I_C) to rise from 0A to the on-state output current (I_{C0}), where (I_{C0}) is at 1% of the model equation's final collector current ($I_{2(on)}$). Hence the parameter $\alpha_{2(on)}$ is provided by Equation 5.57.

$$\alpha_{2(on)} = \frac{1}{1.25t_r} \ln\left(\frac{1}{0.99}\right) \quad (5.57)$$

The collector-emitter voltage (V_{CE}) transient during Phase 2, was modelled via an exponential decay as described by Equation 5.58.

$$V_{CE}(t) = V_{DC} - V_{2(ON)}(1 - e^{-\lambda_{2(on)}(t-t_{1(on)})}) \quad (5.58)$$

$V_{2(ON)}$ can be approximated by considering the average collector current rate of change (dI_C/dt) during Phase 2, across the stray inductance L_P. The average rate of change (dI_C/dt) during Phase 2 is obtained by considering 80% of the on-state output current (I_{C0}) over the rise time (t_r) as expressed by Equation 5.59. Hence:

$$V_{2(on)} = \frac{4I_{c0}}{5t_r} L_P \quad (5.59)$$

The parameter $\lambda_{2(on)}$ was obtained by assuming 90% decay of $V_{2(on)}$ during Phase 2 and is related to the rise time (t_r) since the collector current's (I_C) varies linearly with time, it reflects 80% of the time duration of Phase 2. This is provided by Equation 5.60.

$$\lambda_{2(on)} = \frac{1}{1.25t_r} \ln(10) \quad (5.60)$$

5.3.3 IGBT Non-Linear Model for Turn-On Transients during Phase 3

During this phase the collector current (I_C), is due to the reverse recovery current of the internal IGBT diode utilized as the free-wheeling diode. The dynamics of this phenomenon have been thoroughly discussed in Section 5.2.3. In relation to the reverse recovery section of the collector current (I_C) (i.e. Phase 3 and Phase 4) as depicted in Figure 5.12, one can notice that the entire reverse recovery can be divided into three section:

- The first section is the non-linear increase of the collector current until the peak reverse recovery current (I_{RMM}) is reached.
- The second section is the counter non-linear decrease of the collector current (I_C) once the peak reverse recovery current (I_{RRM}) is reached.
- The third section describes the non-linear "tailing" of the collector current (I_C) during Phase 4, mathematically asymptotic to the on-state output collector current (I_{C0}).

Hence the idea is to come up with a mathematical function which describes the entirety of the above three phases. The mathematical function should; pass through the origin, include a maximum point, include a "tailing section" characterized by a change in the direction of curvature hence a point of inflection transiting the function from concave down to concave up, and finally it needs to be asymptotic to the horizontal. The entire collector current (I_C) reverse recovery section can be generally best represented mathematically by Equation 5.61.

$$y = f(x) = xe^{-x^2} \tag{5.61}$$

1. *The function's 1st derivative*

$$\frac{dy}{dx} = \frac{d(xe^{-x^2})}{dx} = (x)'\left(e^{-(x^2)}\right) + x\left(e^{-(x^2)}\right)' = (1-2x^2)e^{-(x^2)} \tag{5.62}$$

2. *The function's 2nd derivative*

$$\frac{d^2(xe^{-x^2})}{dx^2} = (1-2x^2)'\left(e^{-(x^2)}\right) + (1-2x^2)\left(e^{-(x^2)}\right)' = 2xe^{-(x^2)}(2x^2-3) \tag{5.63}$$

The characteristics of function $f(x) = xe^{-x^2}$:

- The function passes through the origin (0,0).
- In relation to positive x-values the function has a relative maximum at ($\frac{\sqrt{2}}{2}$, 0.4288).
- In relation to positive x-values the function has a point of inflection at ($\frac{\sqrt{6}}{2}$, 0.2733).
- The function is asymptotic to $y = 0$;

X-Value	$\frac{dy}{dx}$ Polarity	$\frac{d^2y}{dx^2}$ Polarity	Y-Value	Y-Value Trend
$0 < x < \frac{\sqrt{2}}{2}$	Positive	Negative	Y-Value increases with a concave down.	
$\frac{\sqrt{2}}{2} < x < \frac{\sqrt{6}}{2}$	Negative	Negative	Y-Value decreases with a concave down.	
$\frac{\sqrt{6}}{2} < x$	Negative	Positive	Y-Value decreases with a concave up.	

Table 5-9 – Summary of Reverse Recovery Collector Current (I_C) general non-linear function modelling

Table 5-9 provides a summary of the salient characteristics of the above function for positive x-values. Figure 5.28 provides the corresponding plot highlighting the congruence with the collector current (I_C) reverse recovery section, as depicted in Figure 5.12. The above function was transformed to reflect the IGBT reverse recovery collector current (I_C) characteristics as depicted in Figure 5.12. The following are the transformations required:

1. Introduce time (t) as the x-axis parameter.
2. Introduce the collector current (I_C) as the y-axis parameter.

$$\therefore I_C(t) = te^{-t^2} \tag{5.64}$$

3. The function is shrunk horizontally such that $\frac{\sqrt{2}}{2}$ corresponds to $t_{a(rr)}$.

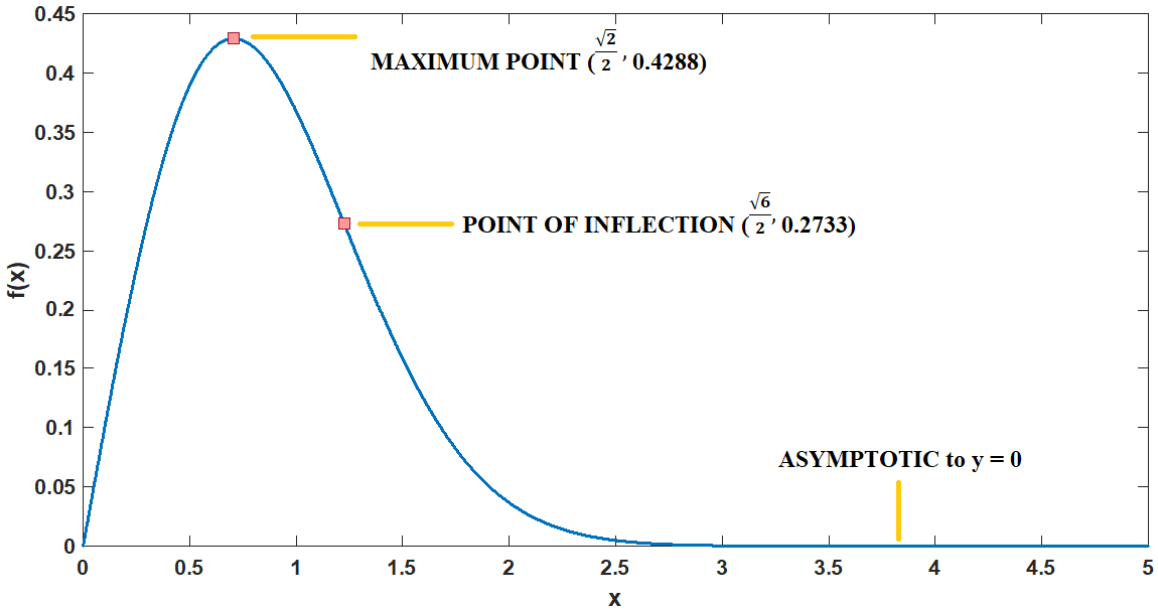


Figure 5.28 - Reverse Recovery Collector Current (I_C) general non-linear function plot.

The function is shrunk horizontally by considering:

$I_C(\alpha_{3(ON)}t)$ such that $\alpha_{3(ON)} > 1$ and $\alpha_{3(ON)}$ is the shrinking factor

$$\text{Hence } \alpha_{3(ON)} = {}^{\frac{\sqrt{2}}{2}}\Big/_{t_{a(rr)}} = {}^{\frac{1}{\sqrt{2}}}\Big/_{t_{a(rr)}} = \frac{1}{\sqrt{2}t_{a(rr)}} \tag{5.65}$$

$$\therefore I_C(\alpha_3 t) = \alpha_{3(ON)} te^{-\alpha_{3(ON)}(t^2)} = \frac{1}{\sqrt{2}t_{a(rr)}} te^{-\alpha_{3(ON)}(t)^2}$$

Hence after shrinking horizontally the function translates to:

$$I_C(t) = \frac{1}{\sqrt{2}t_{a(rr)}} te^{-\alpha_{3(ON)}(t)^2} \tag{5.66}$$

4. The function is stretched vertically by a stretching factor (I_3) such that $f(\frac{\sqrt{2}}{2})$ corresponds to I_{RRM}.

$$\therefore I_3 = \frac{I_{RRM}}{f(\frac{\sqrt{2}}{2})} = \frac{I_{RRM}}{\frac{1}{\sqrt{2}}e^{-\frac{1}{2}}} = \sqrt{2} I_{RRM} e^{\frac{1}{2}}$$

Hence after stretching vertically the function translates to:

$$I_C(t) = \frac{1}{\sqrt{2}t_{a(rr)}} I_3 e^{\frac{1}{2}} te^{-\alpha_{3(ON)}(t^2)} = \frac{I_{RRM}e^{\frac{1}{2}}}{t_{a(rr)}} te^{-\alpha_{3(ON)}(t^2)}$$

$$\text{With } I'_{3(REC)} = \frac{I_{RRM}e^{\frac{1}{2}}}{t_{a(rr)}} \tag{5.67}$$

$$\therefore I_C(t) = I'_{3(REC)} te^{-\alpha_{3(ON)}(t)^2} \tag{5.68}$$

5. The function is shifted vertically up by I_{C0}

$$\therefore I_C(t) = I_{C0} + I'_{3(REC)} te^{-\alpha_{3(ON)}(t)^2} \tag{5.69}$$

Introducing the turn-on Phase 3, time interval within Equation 5.70 yields to:

$$I_C(t) = I_{C0} + I'_{3(REC)}(t - t_{2(on)})e^{-\alpha_{3(ON)}(t-t_{2(on)})^2} \tag{5.70}$$

Hence Equation 5.70 models the collector current (I_C) during the reverse recovery stage of Phase 3. As depicted in Figure 5.12, the collector emitter voltage (V_{CE}) remains at a relatively constant voltage after experiencing the drop due to the stray inductance (L_p), which is based on the rate of change of the collector current (dI_C/dt) during Phase 2, which was modelled within Equation 5.71 as the 80% change in I_{C0} experienced during the rise time (t_r).

$$V_{CE}(t) = V_{DC} - L_p \frac{0.8 I_{C0}}{t_r} \tag{5.71}$$

5.3.4 IGBT Non-Linear Model for Turn-On Transients during Phase 4

After the peak reverse recovery current (I_{RRM}) is reached at $t_{3(on)}$, the reverse recovery current starts to decay. Equation 5.70 describes the collector current (I_C) experiencing reverse recovery during Phase 3. As explained earlier, this equation too is experiencing a decay once the maximum point is reached, as indicated in Figure 5.28. The only drawback of utilizing this equation, to model the decay stages of the diode's reverse recovery current, is the fact that the decay stages are somewhat independent from the rising stage as experienced during Phase 3. It is important to highlight that Equation 5.70 was transformed and adapted to the conditions of Phase 3 nominally the time duration ($t_{a(rr)}$). Hence for the reverse recovery decay stages experienced during Phase 4, a general model equation with congruences with the general model equation provided by Equation 5.61 was utilized and is provided by Equation 5.72.

$$y = f(x) = e^{-(x^2)} \tag{5.72}$$

The above model equation like Equation 5.61, possesses too, a relative maximum, include a "tail section" characterized by a change in the direction of curvature hence a point of inflection, transiting the function from concave down to concave up, and is asymptotic to the horizontal. Moreover, the above mathematical function has its maximum at x=0 with a corresponding y-value at unity. This is illustrated in Figure 5.29. These latter conditions contribute to a simpler adaptation of this general model equation to the IGBT's collector current (I_C) reverse recovery transient during this decaying phase.

$$\frac{dy}{dx} = \frac{d(e^{-(x^2)})}{dx} = (-2x)e^{-(x^2)} \tag{5.73}$$

$$\text{Moreover } \frac{d^2y}{dx^2} = \frac{d^2(e^{-(x^2)})}{dx^2} = \left(-2e^{-(x^2)}\right)(1-2x^2) \tag{5.74}$$

$$\text{Maximum Point @ (0,1), Point of Inflection @ } \left(\frac{\mathbf{1}}{\sqrt{\mathbf{2}}}, \frac{\mathbf{1}}{\boldsymbol{e^{\frac{1}{2}}}}\right)$$

The above function was transformed to reflect the IGBT reverse recovery collector current (I_C) characteristics as depicted in Figure 5.12. The following are the transformations required:

1. Replace the x-axis parameter with the parameter time (t)
2. Replace the y-axis parameter with the collector current (I_C)

$$\therefore I_C(t) = e^{-(t^2)} \tag{5.75}$$

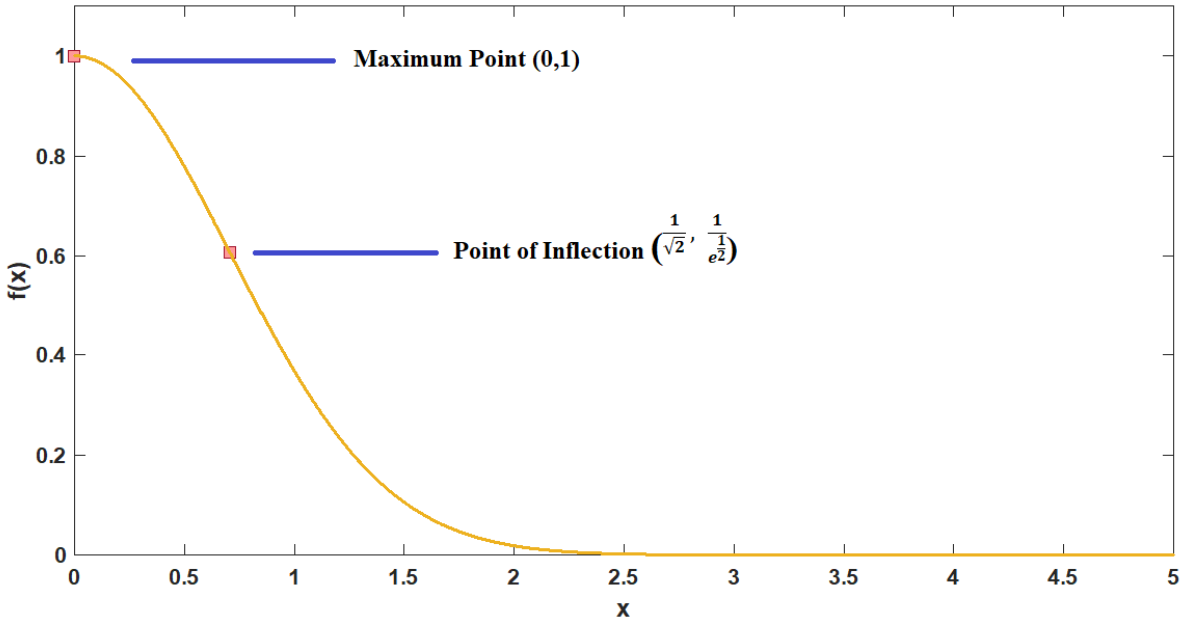


Figure 5.29 - Reverse Recovery Collector Current (I_C) decay general non-linear function plot.

3. The function is shrunk horizontally such that $t_{b(rr)}$ reflects the reverse recovery current decay to 10% of the peak reverse recovery current (I_{RRM}),

   The function is shrunk horizontally by:

   Determining x @ f(x) = 10% of (Maximum of f(x)) where {Maximum of f(x) = 1}

$$\therefore 0.1 = e^{-(x^2)}$$

$$-\ln(0.1) = x^2$$

$$\sqrt{\ln(10)} = x$$

   Therefore, the function is shrunk horizontally such that $\sqrt{\ln(10)}$ corresponds to $t_{b(rr)}$.

   The function is shrunk horizontally by considering:

$$I_C(\alpha_{4(ON)}t) \text{ such that } \alpha_{4(ON)} > 1 \text{ and } \alpha_{4(ON)} \text{ is the shrinking factor}$$

$$\text{Hence } \alpha_{4(ON)} = \sqrt{\ln(10)}/t_{b(rr)} = \ln(10)/t_{b(rr)}^2 \qquad (5.76)$$

$$\therefore I_C(\alpha_{4(ON)}t) = e^{-\alpha_{4(ON)}(t^2)}$$

4. The function is stretched vertically by a stretching factor (I_4) such that f(0) corresponds to I_{RRM}.

$$\therefore I_4 = \frac{I_{RRM}}{f(0)} = \frac{I_{RRM}}{1} = I_{RRM}$$

$$I_C(t) = I_4 e^{-\alpha_{4(ON)}(t^2)} = I_{RRM} e^{-\alpha_{4(ON)}(t^2)}$$

6. The function is shifted vertically up by I_{C0}

$$\therefore I_C(t) = I_{C0} + I_{RRM} e^{-\alpha_{4(ON)}(t^2)} \tag{5.77}$$

Introducing the turn-on Phase 4, time interval within Equation 5.77 yields to:

$$I_C(t) = I_{C0} + I_{RRM} e^{-\alpha_{4(ON)}(t-t_{3(on)})^2} \tag{5.78}$$

Hence, Equation 5.78 models the collector current (I_C) during the reverse recovery stage of Phase 4. During this phase the collector-emitter voltage (V_{CE}) decays to the collector-emitter on-state saturation voltage (V_{CE_SAT}). The decay during Phase 4 is conducted through two decay stages, an initial rapid decay, and a final slower decay. The combination of the two is modelled via the summation of two decaying functions, where each function is of the general type described by Equation 5.72, but with different horizontal shrinking factors and vertical stretching factors, hence obtaining distinct decays. The initial decay has the same shrinking factor as the collector current (I_C) decay, modelled by Equation 5.78, since both decays are conducted through the same time duration ($t_{b(rr)}$). Hence the shrinking factor for the initial rapid decay function is α_4. The vertical stretching factors are related to two distinct collector-emitter voltage (V_{CE}) parameters, the initial collector-emitter voltage (V_{CE}) of Phase 4, which is equal to the collector-emitter voltage (V_{CE}) during Phase 3 and the voltage parameter V_{TAIL}, which acts as the stretching coefficient of the final slow decaying function. These two voltage parameters are related to each other via parameter k_4, where this latter parameter varies between 0 and 1, and provides the ratio of the magnitude of the tail voltage (V_{TAIL}) vis-à-vis, the initial Phase 4 collector-emitter voltage (V_{4_INIT}) and is provided by Equation 5.80.

$$V_{4_{INIT}} = V_{CE\_PHASE3} = V_{ce0} - L_p \frac{0.8 I_{c0}}{t_r} \tag{5.79}$$

$$k_4 = \frac{V_{TAIL}}{V_{4\_INIT}} \tag{5.80}$$

$$V_{4_{FAST}} = (1 - k_4) V_{4_{INIT}} \tag{5.81}$$

The function is stretched vertically by a stretching factor ($V_{4_{FAST}}$). Hence the initial fast decay stage of the collector emitter voltage (V_{CE}) is modelled by,

$$V_{CE}(t) = V_{4_{FAST}} e^{-\alpha_{4(ON)}(t-t_{3on})^2} \tag{5.82}$$

The final slow decay shrinking coefficient (λ_4), for generic function $f(x) = e^{-(x^2)}$, is determined through the following.

The function is shrunk horizontally by:

Determining x @ f(x) = $\frac{V_{CE\_SAT}}{V_{TAIL}}$ x (Maximum of f(x)) where {Maximum of f(x) = 1}

$$\therefore \frac{V_{CE\_SAT}}{V_{TAIL}} x\ 1 = \ e^{-(x^2)}$$

$$-\ln\left(\frac{V_{CE\_SAT}}{V_{TAIL}}\right) = \ x^2$$

$$\sqrt{\ln\left(\frac{V_{TAIL}}{V_{CE\_SAT}}\right)} = x$$

Therefore, the function is shrunk horizontally such that:

$\sqrt{\ln\left(\frac{V_{TAIL}}{V_{CE\_SAT}}\right)}$ corresponds to $(t_{b(rr)} + t_{v(tail)})$

The function is shrunk horizontally by considering:

$I_C(\lambda_{4(ON)}t)$ such that $\lambda_{4(ON)} > 1$ and $\lambda_{4(ON)}$ is the shrinking factor

$$\lambda_{4(ON)} = \frac{\sqrt{\ln\left(\frac{V_{TAIL}}{V_{CE\_SAT}}\right)}}{(t_{b(rr)} + t_{vtail})} = \frac{\ln\left(\frac{V_{TAIL}}{V_{CE\_SAT}}\right)}{(t_{b(rr)} + t_{vtail})^2} \quad (5.83)$$

The function is stretched vertically by a stretching factor (V_{TAIL}). Hence the final slow decay stage of the collector emitter voltage (V_{CE}) is modelled by:

$$V_{CE}(t) = V_{TAIL} e^{-\lambda_{4(ON)}(t-t_{3on})^2} \quad (5.84)$$

Thus, the combined collector-emitter voltage (V_{CE}) including both the initial fast decay stage and final slow decay, is provided by Equation 5.85.

$$V_{CE}(t) = V_{4_{FAST}} e^{-\alpha_{4(ON)}(t-t_{3on})^2} + V_{TAIL} e^{-\lambda_{4(ON)}(t-t_{3on})^2} \quad (5.85)$$

5.3.5 IGBT Non-Linear Model for Turn-Off Transients during Phase 1 and Phase 2

During these phases, the collector current (I_C) remains at a constant value namely the output on-state output collector current (I_{C0}), as indicated by Equation 5.86.

$$I_C(t) = I_{C0} \tag{5.86}$$

The collector-emitter voltage (V_{CE}) transient during this phase, forms part of a single broader transient which entails Phase 2 too. Looking closely at Figure 5.20, this single collector-emitter voltage (V_{CE}) transient is characterized by an initial quasi-linear increase, lasting approximately half of Phase 1, eventually transiting to a steep exponential growth, lasting till the end of Phase 2. These transient characteristics indicate that the optimal model equation for the combined Phase 1 and Phase 2 collector-emitter voltage (V_{CE}), is a composite linear and exponential function. Moreover, the function needs to manifest a concave up nature with no maxima. The above characteristics reflect a generalized equation as provided by Equation 5.87.

$$y = f(x) = x + e^x \tag{5.87}$$

1. The function's first derivative

$$\frac{dy}{dx} = \frac{d(x+e^x)}{dx} = 1 + e^x \tag{5.88}$$

2. The function's second derivative

$$\frac{d^2y}{dx^2} = \frac{d^2(x+e^x)}{dx^2} = e^x \tag{5.89}$$

The above general composite function is illustrated in Figure 5.30

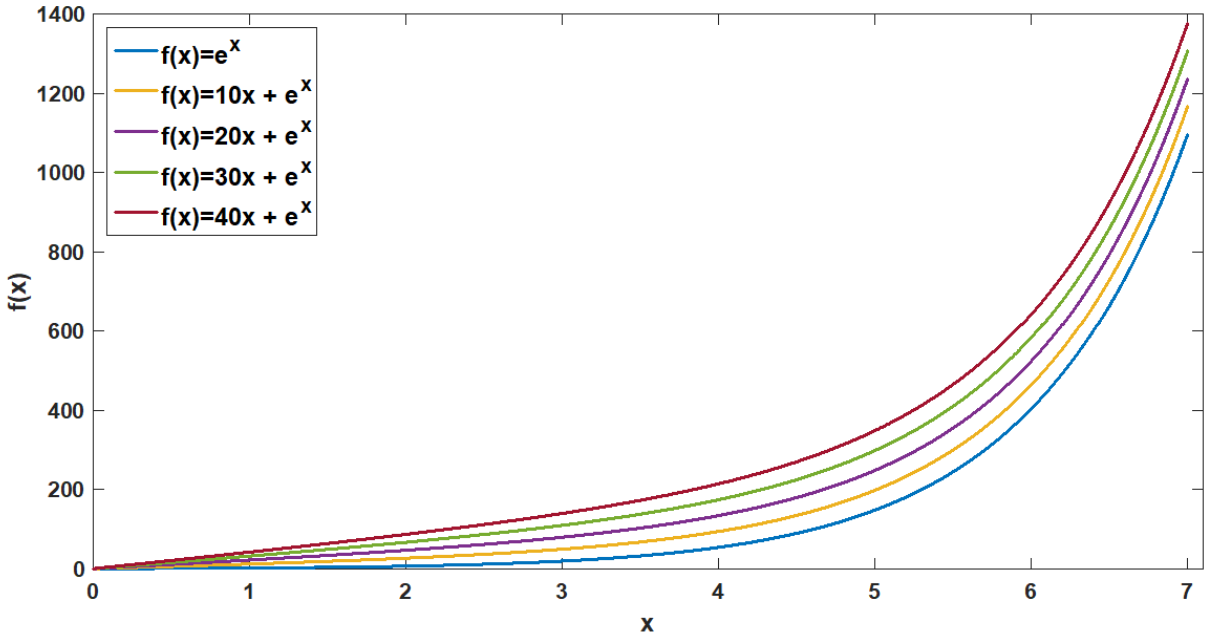


Figure 5.30 - Phase 1 & Phase 2 General V_{CE} Model Equation highlighting the enhanced control over the initial linear stage model via the introduction of the composite function,

Again, the above function was transformed to reflect the IGBT collector-emitter voltage (V_{CE}) characteristics as depicted in Figure 5.20. The following are the transformations required:

1. Replace the x-axis parameter with the parameter time (t)
2. Replace the y-axis parameter with the collector-emitter voltage (V_{CE})

$$\therefore V_{CE}(t) = t + e^t$$

3. In relation to Figure 5.20, the characteristic timing ($t_{Vd(OFF)}$) is the time required for the collector-emitter voltage (V_{CE}) to increase from the collector-emitter saturation voltage (V_{CE_SAT}) to 10% of the output off-state collector-emitter voltage (V_{DC}). Moreover, the off-delay time ($t_{d(off)}$) is the time duration between the start of Phase 1 and the instant the collector current (I_C) is equal to 90% of the on-state output collector current (I_{C0}). The ratio of these two parameters (k_{vd}) is provided by the approximation provided in Equation 5.90.

$$k_{vd} \approx \frac{t_{Vd(OFF)}}{t_{d(OFF)}} \tag{5.90}$$

The combined time duration of Phase 1 and Phase 2 ($t_{PH\_1\_2}$), is essentially the off delay-time ($t_{d(off)}$), less the initial duration for the collector-current (I_C) to decay by 10%. Due to the linear nature of the initial collector current (I_C) fall, during the fall-time (t_f), the initial 10% collector current (I_C) decay duration, can be approximated to be $1/8^{th}$ of the fall time (t_f). Hence the combined time duration of Phase 1 and Phase 2 ($t_{PH\_1\_2}$) can be approximated through Equation 5.91 where:

$$t_{PH\_1\_2} = (t_{d(OFF)} - \frac{1}{8}t_f) \tag{5.91}$$

At this point it is useful to determine the relevant transformation of the linear function within the above composite function by determining the relevant gradient for the corresponding IGBT collector-emitter voltage (V_{CE}) transient. This can be approximated as the linear rate of change of collector-emitter voltage during Phase 1, as provided by Equation 5.92.

$$\frac{dV'_{1(OFF)}}{dt} = \frac{0.1V_{CE0} - V_{CE\_SAT}}{t_{Vd(OFF)}} = \frac{0.1V_{CE0} - V_{CE\_SAT}}{k_{vd}(t_{d(OFF)} - \frac{1}{8}t_f)} \tag{5.92}$$

Hence the linear function is furthermore translated to take into consideration the starting time of Phase 1 ($t_{0(OFF)}$) and the corresponding collector-emitter voltage (V_{CE}) at this instant, yielding to Equation 5.93.

$$\therefore\ V_{CE_{LINEAR}}(t) = \frac{dV'_{1(OFF)}}{dt}\left(t - t_{0(OFF)}\right) + V_{CE\_SAT} \tag{5.93}$$

4. The exponential function within the above composite function is transformed to reflect the exponential growth of the IGBT's collector-emitter voltage (V_{CE}) during Phase 1 and Phase 2. Equation 5.87 is a composite function, which means that the final value at the end of Phase 2, which corresponds to the output off-state voltage (V_{DC}), is due to the summative contribution of both the linear function and the exponential function. Hence the final growth due to the exponential function required at the end of Phase 2 (V_{EXP}') is provided by Equation 5.94.

$$V'_{EXP} = V_{CE0} - \left\{\frac{dV'_{1(OFF)}}{dt}t_{PH_{1_2}} + V_{CE_{SAT}}\right\}$$

$$V'_{EXP} = V_{CE0} - \{\frac{dV'_{1(OFF)}}{dt}\left(t_{d(OFF)} - \frac{1}{8}t_f\right) + V_{CE\_SAT}\} \tag{5.94}$$

Hence the exponential function within the composite function is shrunk horizontally by:

Determining x @ f(x) = $\frac{V'_{EXP}}{V_{CE\_SAT}}$ (at x = 0, f(e^x)=1, which corresponds to V_{CE_SAT}, hence determining x such that f(e^x) produces a growth of $\frac{V'_{EXP}}{V_{CE\_SAT}}$, as this value of x corresponds to actual time duration of $t_{PH\_1\_2}$, through which we can obtain the required shrinking factor)

$$\therefore \frac{V'_{EXP}}{V_{CE\_SAT}} = e^x \Rightarrow \ln\left(\frac{V'_{EXP}}{V_{CE\_SAT}}\right) = x$$

Therefore, the exponential function within the composite function is shrunk horizontally such that: $\ln\left(\frac{V'_{EXP}}{V_{CE\_SAT}}\right)$ corresponds to $t_{PH\_1\_2}$ and by considering $V_{CE}\left(\lambda_{1(OFF)}t\right)$ such that $\lambda_{1(OFF)} > 1$ and $\lambda_{1(OFF)}$ is the shrinking factor.

$$\lambda_{1(OFF)} = \frac{\ln\left(\frac{V'_{EXP}}{V_{CE\_SAT}}\right)}{t_{PH\_1\_2}} = \frac{\ln\left(\frac{V'_{EXP}}{V_{CE\_SAT}}\right)}{\left(t_{d(OFF)} - \frac{1}{8}t_f\right)} \tag{5.95}$$

Hence the exponential function is furthermore translated to take into consideration the starting time of Phase 1 ($t_{0(OFF)}$) and the corresponding collector-emitter voltage (V_{CE}) at this instant, that is, the collector-emitter on-state saturation voltage (V_{CE_SAT}), yielding to Equation 5.96.

$$V_{CE_{EXP}}(t) = V_{CE\_SAT} e^{\lambda_{1(OFF)}(t-t_{0(OFF)})} \tag{5.96}$$

Finally, the two collector-emitter voltage (V_{CE}) functions are combined into the composite function yielding to Equation 5.97 which models the collector-emitter voltage (V_{CE}) during the turn-off Phase1 and Phase 2.

$$V_{CE}(t) = V_{CE\_SAT} + \frac{dV'_{1(OFF)}}{dt}\left(t - t_{0(OFF)}\right) + V_{CE\_SAT} e^{\lambda_{1(OFF)}(t-t_{0(OFF)})} \tag{5.97}$$

5.3.6 IGBT Non-Linear Model for Turn-Off Transients during Phase 3 and Phase 4

During Phase 3 and Phase 4, the collector current (I_C) experiences a decay, manifesting into two stages, a fast-decaying part due to the intrinsic MOSFET structure, and a slow decaying part due to the intrinsic BJT structure. The combination of these two decays, is modelled via the summation of two decaying functions, obtaining a composite function, where each function is of the general type described by Equation 5.59, but with different horizontal shrinking factors and vertical stretching factors, hence obtaining distinct decays. Hence, the modelling approach is like the approach undertaken to model the collector-emitter voltage (V_{CE}) decay during the turn-on Phase 4.

In relation to Figure 5.20, the parameter I_{TAIL} acts as the stretching coefficient of the final slow decaying function. The parameter k_{TAIL} is the ratio of the parameter I_{TAIL} to the output on-state collector current (I_{C0}) and is provided by Equation 5.98.

$$k_{TAIL} = \frac{I_{TAIL}}{I_{C0}} \tag{5.98}$$

The parameter (k_{TAIL}) is a factor which depends on the IGBT design (relative gains of MOSFET and BJT) and the technology type (if punch through or non-punch through). The stretching factor of the fast-decaying part of the collector current (I_C) is dictated by the intrinsic MOSFET structure and provided by Equation 5.99.

$$I_{MOS} = (1 - k_{TAIL}) I_{C0} \tag{5.99}$$

The initial fast decay shrinking coefficient ($\alpha_{3(OFF)}$), for generic function $f(x) = e^{-(x^2)}$, is determined through the following.

Determining x @ f(x) = $\frac{0.9I_{C0} - I_{TAIL}}{I_{CO} - I_{TAIL}}$ x (Maximum of f(x)) where {Maximum of f(x) = 1})

$$\therefore \frac{0.9I_{C0}-I_{TAIL}}{I_{CO}-I_{TAIL}} x\ 1 = \ e^{-(x^2)}$$

$$\frac{0.9I_{C0}-k_{TAIL}I_{c0}}{I_{CO}-k_{TAIL}I_{c0}} = \ e^{-(x^2)}$$

$$\frac{0.9-k_{TAIL}}{1-k_{TAIL}} = \ e^{-(x^2)}$$

$$-\ln\left(\frac{0.9-k_{TAIL}}{1-k_{TAIL}}\right) = x^2$$

$$\ln\left(\frac{1-k_{TAIL}}{0.9-k_{TAIL}}\right) = x$$

$$\sqrt{\ln\left(\frac{1-k_{TAIL}}{0.9-k_{TAIL}}\right)} = x$$

Therefore, the function is shrunk horizontally such that:

$\sqrt{\ln\left(\frac{1-k_{TAIL}}{0.9-k_{TAIL}}\right)}$ corresponds to $\left(\frac{1}{8}tf\right)$

The function is shrunk horizontally by considering:

$I_C(\alpha_{3(OFF)}t)$ such that $\alpha_{3(OFF)} > 1$ and $\alpha_{3(OFF)}$ is the shrinking factor

$$\alpha_{3(OFF)} = \frac{\sqrt{\ln\left(\frac{1-k_{TAIL}}{0.9-k_{TAIL}}\right)}}{\frac{1}{8}tf} = \frac{64}{{t_f}^2}\ln\left(\frac{1-k_{TAIL}}{0.9-k_{TAIL}}\right) \quad (5.100)$$

Hence the collector current (I_C) decay due to the intrinsic MOSFET structure, is provided by Equation 5.101.

$$I_{C_{MOS}}(t) = \ I_{MOS}e^{-\alpha_{3(OFF)}(t-t_{2(OFF)})^2} \quad (5.101)$$

The final slow decay shrinking coefficient ($\alpha_{4(OFF)}$), for generic function $f(x) = e^{-(x^2)}$, is determined through the following.

Determining x @ f(x) = $\frac{0.01I_{C0}}{I_{TAIL}}$ × (Maximum of f(x)) where {Maximum of f(x) = 1})

$$\therefore \frac{0.01I_{TAIL}}{I_{CO}} x\ 1 = \ e^{-(x^2)}$$

$$\frac{0.01I_{C0}}{k_{TAIL}I_{C0}} = \ e^{-(x^2)}$$

$$-\ln\left(\frac{0.01}{k_{TAIL}}\right) = \ x^2$$

$$\sqrt{\ln(100k_{TAIL})} = x$$

Therefore, the function is shrunk horizontally such that:

$\sqrt{\ln(100k_{TAIL})}$ corresponds approximately to $(tf + t_{itail})$

The function is shrunk horizontally by considering:

$I_C(\alpha_{4(OFF)}t)$ such that $\alpha_{4(OFF)} > 1$ and $\alpha_{4(OFF)}$ is the shrinking factor

$$\alpha_{4(OFF)} = \frac{\sqrt{\ln(100k_{TAIL})}}{(tf+t_{itail})} = \frac{\ln(100k_{TAIL})}{(tf+t_{itail})^2} \quad (5.102)$$

Hence the collector current (I_C) decay due to the intrinsic BJT structure, is provided by Equation 5.103.

$$I_{C_{BJT}}(t) = I_{TAIL}e^{-\alpha_{4(OFF)}(t-t_{2(OFF)})^2} \quad (5.103)$$

Thus, the composite function describing the collector current (I_C) during the turn-off Phase 3 and Phase 4 is provided by Equation 5.104.

$$I_C(t) = I_{MOS}e^{-\alpha_{3(OFF)}(t-t_{2(OFF)})^2} + I_{TAIL}e^{-\alpha_{4(OFF)}(t-t_{2(OFF)})^2} \quad (5.104)$$

The collector-emitter voltage (V_{CE}) during Phase 3 and Phase 4, is essentially an overshoot, induced by the parasitic inductance (L_P) due to the rate of change of the collector current (dI_C/dt) during these two phases.

$$V_{ce}(t) = V_{ce0} - L_p\frac{dI_c(t)}{dt} \quad (5.105)$$

$$\therefore\frac{dI_c(t)}{dt} = \frac{d(I_{MOS}e^{-\alpha_{3(OFF)}(t-t_{2(OFF)})^2} + I_{TAIL}e^{-\alpha_{4(OFF)}(t-t_{2(OFF)})^2})}{dt}$$

Now $\frac{d(I_{MOS}e^{-\alpha_{3(OFF)}(t-t_{2(OFF)})^2})}{dt} = -2\alpha_{3(OFF)}(t-t_{2(OFF)})(I_{MOS}e^{-\alpha_{3(OFF)}(t-t_{2(OFF)})^2})$

And $\frac{d(I_{TAIL}e^{-\alpha_{4(OFF)}(t-t_{2(OFF)})^2})}{dt} = -2\alpha_{4(OFF)}(t-t_{2(OFF)})(I_{TAIL}e^{-\alpha_{4(OFF)}(t-t_{2(OFF)})^2})$

$$\therefore\frac{dI_c(t)}{dt} = -2(t-t_{2(OFF)})\left\{\alpha_{3(OFF)}I_{MOS}e^{-\alpha_{3(OFF)}(t-t_{2(OFF)})^2} + \alpha_{4(OFF)}I_{TAIL}e^{-\alpha_{4(OFF)}(t-t_{2(OFF)})^2}\right\} \quad (5.106)$$

Hence the collector-emitter voltage (V_{CE}) during Phase 3 and Phase 4 is provided through Equation 5.107.

$$V_{ce}(t) = V_{ce0} + 2L_p\left(t - t_{2(OFF)}\right)\left\{\alpha_{3(OFF)} I_{MOS} e^{-\alpha_{3(OFF)}\left(t-t_{2(OFF)}\right)^2} + \alpha_{4(OFF)} I_{TAIL} e^{-\alpha_{4(OFF)}\left(t-t_{2(OFF)}\right)^2}\right\} \tag{5.107}$$

Tables 5-10 and 5-11 provide a summary of the salient turn-on and turn-off non-linear model equations for the collector-emitter voltage (V_{CE}) and collector current (I_C)

Transient Phase	**IGBT Turn-On Transient Non-Linear Model Equations**
Phase 1 I_C Transient	$I_{C(t_0 - t_1)} = 0\text{A}$
Phase 1 V_{CE} Transient	$V_{CE(t_0 - t_1)} = V_{DC}$
Phase 2 I_C Transient	$I_C(t) = I_{2(on)}(1 - e^{-\alpha_{2(on)}(t - t_{1(on)})})$ $I_{2(on)} \approx 100(I_{c0})$ $\alpha_{2(on)} = \frac{1}{1.25t_r}\ln\left(\frac{1}{0.99}\right)$
Phase 2 V_{CE} Transient	$V_{CE}(t) = V_{DC} - V_{2(ON)}(1 - e^{-\lambda_{2(on)}(t - t_{1(on)})})$ $V_{2(on)} = \frac{4I_{c0}}{5t_r}L_P$ $\lambda_{2(on)} = \frac{1}{1.25t_r}\ln(10)$
Phase 3 I_C Transient	$I_C(t) = I_{C0} + I'_{3(REC)}(t - t_{2(on)})e^{-\alpha_{3(ON)}(t - t_{2(on)})^2}$ $\alpha_{3(ON)} = \frac{1}{\sqrt{2}t_{a(rr)}}, I'_{3(REC)} = \frac{I_{RRM}e^{\frac{1}{2}}}{t_{a(rr)}}$
Phase 3 V_{CE} Transient	$\mathrm{V_{CE}(t)} = V_{DC} - L_p\frac{0.8I_{c0}}{t_r}$
Phase 4 I_C Transient	$I_C(t) = I_{C0} + I_{RRM}e^{-\alpha_{4(ON)}(t - t_{3(on)})^2}$, $\alpha_{4(ON)} = \ln(10)/t_{b(rr)}^2$,
Phase 4 V_{CE} Transient	$V_{CE}(t) = V_{4_{FAST}}e^{-\alpha_{4(ON)}(t - t_{3on})^2} + V_{TAIL}e^{-\lambda_{4(ON)}(t - t_{3on})^2}$, $\lambda_{4(ON)} = \frac{\ln\left(\frac{V_{TAIL}}{V_{CE\_SAT}}\right)}{(t_{b(rr)} + t_{vtail})^2}$, $V_{4_{INIT}} = V_{DC} - L_p\frac{0.8I_{c0}}{t_r}$, $k_4 = \frac{V_{TAIL}}{V_{4\_INIT}}$, $V_{4_{FAST}} = (1 - k_4)V_{4_{INIT}}$

Table 5-10 – Summary of the Non-Linear Turn-On V_{CE} and I_C Transient Model Equations.

Transient Phase	IGBT Turn-Off Transient Non-Linear Model Equations
Phase 1 & Phase 2 I_C Transient	$$I_C(t) = I_{C0}$$
Phase 1 & Phase 2 V_{CE} Transient	$$V_{CE}(t) = V_{CE\_SAT} + \frac{dV'_{1(OFF)}}{dt}\left(t - t_{0(OFF)}\right) + V_{CE\_SAT}e^{\lambda_{1(OFF)}(t-t_{0(OFF)})},$$ $$\lambda_{1(OFF)} = \frac{\ln\left(\frac{V'_{EXP}}{V_{CE\_SAT}}\right)}{\left(t_{d(OFF)} - \frac{1}{8}t_f\right)},$$ $$\frac{dV'_{1(OFF)}}{dt} = \frac{0.1V_{CE0} - V_{CE\_SAT}}{k_{vd}\left(t_{d(OFF)} - \frac{1}{8}t_f\right)},\ k_{vd} \approx \frac{t_{Vd(OFF)}}{t_{d(OFF)}},$$ $$V'_{EXP} = V_{CE0} - \left\{\frac{dV'_{1(OFF)}}{dt}\left(t_{d(OFF)} - \frac{1}{8}t_f\right) + V_{CE_{SAT}}\right\}$$
Phase 3 & Phase 4 I_C Transient	$$I_C(t) = I_{MOS}e^{-\alpha_{3(OFF)}(t-t_{2(OFF)})^2} + I_{TAIL}e^{-\alpha_{4(OFF)}(t-t_{2(OFF)})^2}$$ $$\alpha_{3(OFF)} = = \frac{64}{{t_f}^2}\ln\left(\frac{1-k_{TAIL}}{0.9-k_{TAIL}}\right),\ \alpha_{4(OFF)} = \frac{\ln(100k_{TAIL})}{(tf+t_{itail})^2}$$ $$I_{MOS} = (1-k_{TAIL})I_{C0}, k_{TAIL} = \frac{I_{TAIL}}{I_{C0}}$$
Phase 3 & Phase 4 V_{CE} Transient	$$V_{ce}(t) = V_{DC} + 2L_p\left(t - t_{2(OFF)}\right)\left\{\alpha_{3(OFF)}I_{MOS}e^{-\alpha_{3(OFF)}(t-t_{2(OFF)})^2}\right.$$ $$\left. + \alpha_{4(OFF)}I_{TAIL}e^{-\alpha_{4(OFF)}(t-t_{2(OFF)})^2}\right\}$$

Table 5-11 - Summary of the Non-Linear Turn-Off V_{CE} and I_C Transient Model Equations.

5.3.7 IGBT Non-Linear Model Parameters and Results

Figures 5.31 and 5.32, illustrate the above model equations implementation for the IRG4BC30KD IGBT, Sample 14, when new, for both the turn-on and turn-off transients.

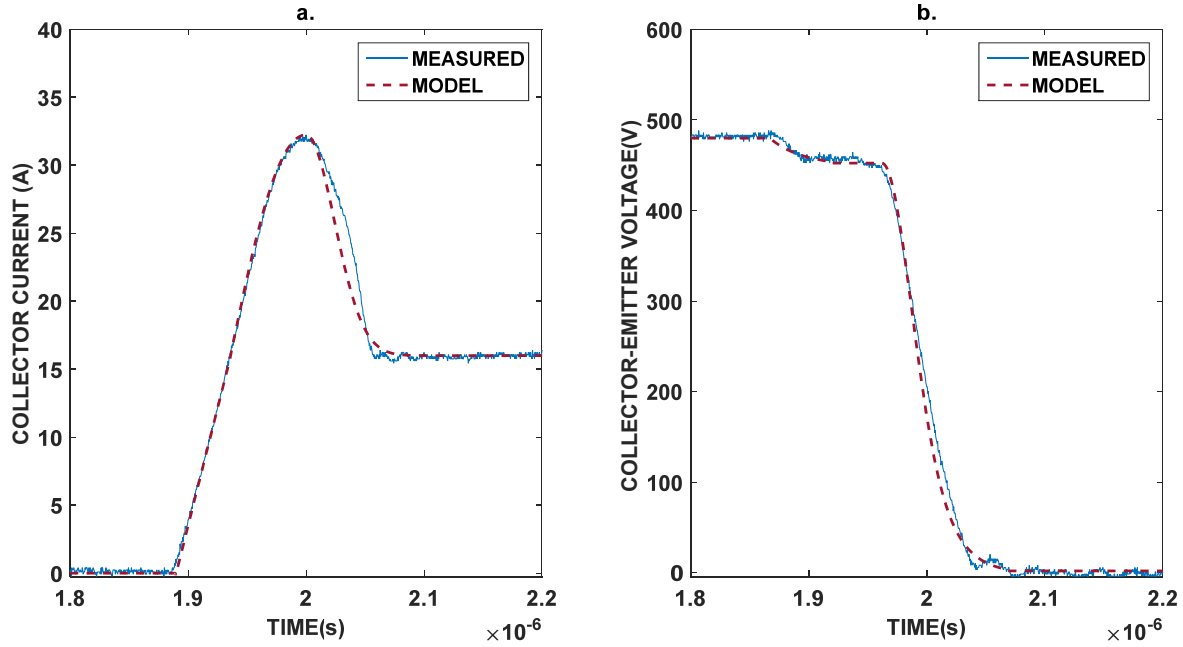


Figure 5.31 - IGBT Turn-On Non-Linear Model for IGBT Sample 14 (vNEW) (a) Collector Current (I_C) Transient (b) Collector-Emitter Voltage (V_{CE}) Transient

Table 5-12 provides the list of the different parameters utilized in the non-linear modelling of the turn-on and turn-off transients. Parameters were obtained through the Double-Pulse test conditions and through the acquired Double-Pulse transients. As indicated in Figures 5.31 and 5.32, the implemented equations provided a relatively adequate congruence between the transients' measurement and modelling. Minor incongruencies were observed during the turn-on collector current (I_C) reverse-recovery section, specifically during the second phase of the reverse recovery (i.e. turn-on Phase 4), during the turn-off collector-current (I_C) tailing section (i.e. turn-off Phase 4) and finally during the turn-off collector-emitter voltage (V_{CE}) overshoot (i.e. turn-off Phase 3). Evidently, the above implemented IGBT non-linear transients modelling provided a better representation of the measured transients than the presented linear piece-wise model.

TURN-ON MODEL PARAMETERS			**TURN-OFF MODEL PARAMETERS**		
Parameter	**Transient Phase**	**Value**	**Parameter**	**Transient Phase**	**Value**
$I_{C(OFF)}$	Phase 1 I_C Transient	0A	$t_{0(OFF)}$	Phase 1 & 2 V_{CE} Transient	1.798µs
V_{DC}	Phase 1 V_{CE} Transient	480V	$t_{Vd(OFF)}$	Phase 1 & 2 V_{CE} Transient	38ns
$t_{1(ON)}$	Phase 2 I_C Transient	1.855µs	$t_{d(OFF)}$	Phase 1 & 2 V_{CE} Transient	111ns
I_{C0}	Phase 2 I_C Transient	16A	t_f	Phase 1 & 2 V_{CE} Transient	78ns
$I_{2(ON)}$	Phase 2 I_C Transient	1600A	$\lambda_{1(OFF)}$	Phase 1 & 2 V_{CE} Transient	$49.85Ms^{-1}$
t_r	Phase 2 I_C Transient	39ns	k_{vd}	Phase 1 & 2 V_{CE} Transient	0.3423
$\alpha_{2(ON)}$	Phase 2 I_C Transient	$206.16ks^{-1}$	V_{CE0}	Phase 1 & 2 V_{CE} Transient	480V
L_P	Phase 2 V_{CE} Transient	100.2nH	V'_{EXP}	Phase 1 & 2 V_{CE} Transient	344V
$V_{2(ON)}$	Phase 2 V_{CE} Transient	32.9V	$\frac{dV'_{1(OFF)}}{dt}$	Phase 1 & 2 V_{CE} Transient	1321.12V/µs
$\lambda_{2(ON)}$	Phase 2 V_{CE} Transient	$47.23Ms^{-1}$	$t_{2(OFF)}$	Phase 3 & 4 I_C Transient	2.010µs
$t_{2(ON)}$	Phase 3 I_C Transient	1.936µs	t_{itail}	Phase 3 & 4 I_C Transient	57ns
$t_{a(rr)}$	Phase 3 I_C Transient	58ns	$\alpha_{3(OFF)}$	Phase 3 & 4 I_C Transient	$1.642x10^{15}s^{-1}$
I_{RRM}	Phase 3 I_C Transient	15.52A	$\alpha_{4(OFF)}$	Phase 3 & 4 I_C Transient	$1.881x10^{14}s^{-1}$
$I'_{3(REC)}$	Phase 3 I_C Transient	439.66A	$k_{(TAIL)}$	Phase 3 & 4 I_C Transient	0.3082
$t_{b(RR)}$	Phase 4 I_C Transient	60ns	I_{TAIL}	Phase 3 & 4 I_C Transient	4.5A
$\alpha_{4(ON)}$	Phase 4 I_C Transient	$6.396x10^{14}s^{-1}$	I_{MOS}	Phase 3 & 4 I_C Transient	11.1A
$t_{3(on)}$	Phase 4 I_C Transient	1.997µs	t_f	Phase 3 & 4 I_C Transient	78ns
V_{4INIT}	Phase 4 V_{CE} Transient	447.11V			
V_{CE_SAT}	Phase 4 V_{CE} Transient	2.21V			
k_4	Phase 4 V_{CE} Transient	0.2604			
V_{4FAST}	Phase 4 V_{CE} Transient	330.69V			
t_{vtail}	Phase 4 V_{CE} Transient	55ns			
$\lambda_{4(ON)}$	Phase 4 V_{CE} Transient	$3x10^{14}s^{-1}$			

Table 5-12 – IGBT Turn-On and Turn-Off Transient Model Parameters

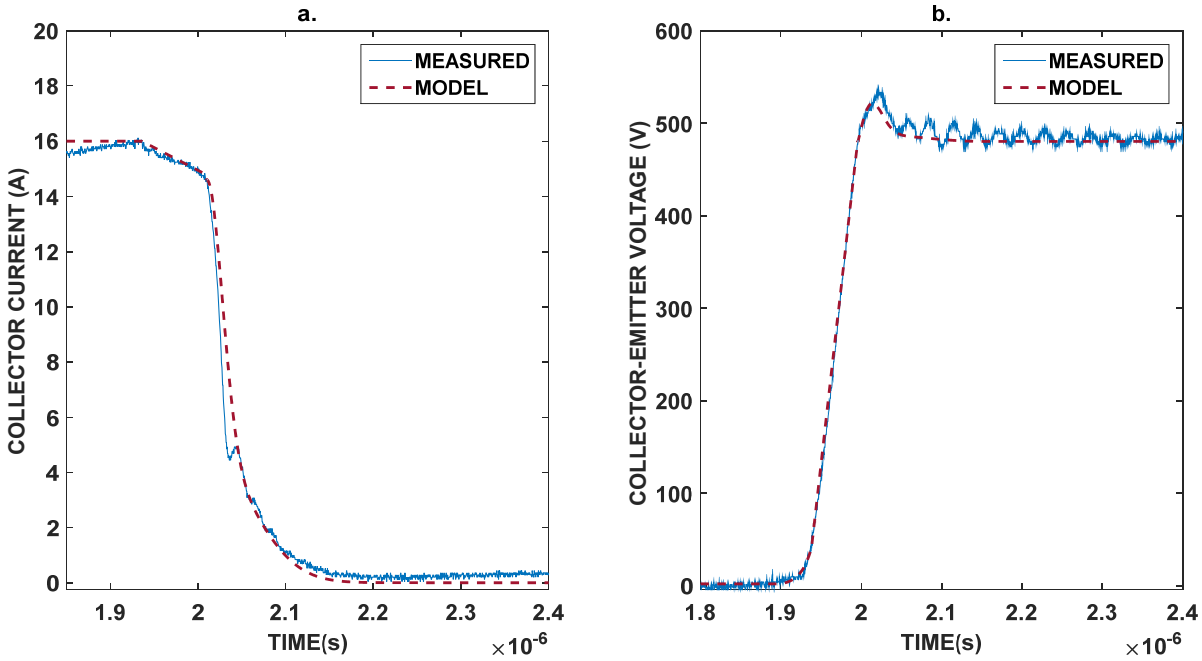


Figure 5.32 - IGBT Turn-Off Non-Linear Model for IGBT Sample 14 (vNEW) (a) Collector Current (IC) Transient (b) Collector-Emitter Voltage (VCE) Transient

5.4 IGBT Parasitic Capacitances

As discussed earlier, the complex structure of an IGBT comprises parasitic capacitances. As indicated these capacitances influence extensively the switching behaviour of the IGBT, predominantly the input non-linear parasitic capacitances, consisting of the gate-emitter capacitance (C_{GE}) and the Miller collector-gate capacitance (C_{CG}). The physical understanding and modelling of these capacitances become important to explain their impacts on the aged IGBTs' switching transients. In [228] and [229], the modelling of the gate-emitter capacitance (C_{GE}) and the collector-gate Miller capacitance (C_{CG}), focused on the operating point characteristics of these two capacitances. Baliga [5] considers the input capacitances as MOS capacitances, hence modelling predominantly the input capacitances, in relation to the voltage dependency. Rael et al. [226], bases the parasitic capacitances model on the voltage dependency as well, but including further within the proposed model the influence of the interelectrode MOS capacitances. The model takes into consideration negative gate biasing too but does not include the influence of the collector current (I_C). The collector-gate Miller capacitance (C_{CG}) is thoroughly influenced by the N^- drift region, especially the N^- region close to the gate, which is full of carriers, and hence cannot just be assumed to be predominantly a "depletion region" capacitance [224]. In another study Palmer et al. [230], analyses the dependency of the input capacitances to the rated current. This study showed that the input capacitances increase at high currents, but this study did not go into modelling this

phenomenon. Tan et al. [224], modelled this effect by including a factor within the input capacitances model equations, which considers this dependency.

5.4.1 MOS Capacitance Structure and the Flat-Band Condition

Figure 5.33 illustrates the basic structure of a metal oxide semiconductor (MOS) capacitor. It consists of a semiconductor substrate, a dielectric material commonly silicon-dioxide (SiO_2) and a gate metal electrode which commonly consists of heavily doped N^+ polysilicon. The metal acts as one plate of the capacitor, the semiconductor substrate (N-Type or P-Type) acts as the other plate.

The capacitance of a MOS structure depends upon the voltage applied on the gate electrode. An important parameter related to the MOS capacitor structure is the flat-band voltage (V_{FB}), which is defined as the voltage at which there is no charge on the MOS capacitor plates, yielding to no net electric field across the dielectric oxide. In relation to Figure 5.34, where the substrate is of the P-type, the flat-band condition occurs when the energy band (E_C-E_V) of the substrate is flat at the Silicon-Silicon dioxide (Si-SiO_2) interface, caused by a negative voltage at the gate, such that the band diagram is raised on the gate side. When the flat band condition is achieved, the substrate has zero electric field in the substrate surface. This yields to a zero electric field in the dielectric oxide too. Hence the applied voltage which produces the flat-band condition (V_{FB}), is essentially the difference between the Fermi levels of the N^+ polysilicon gate and the semiconductor of the substrate as provided by Equation 5.108 [224].

$$\boldsymbol{V_{FB} = \psi_{GATE} - \psi_{Si}} \tag{5.108}$$

Where ψ_{GATE} is the gate's N^+ polysilicon work function (V) and ψ_{GATE} is the semiconductor (Si) work function (V)

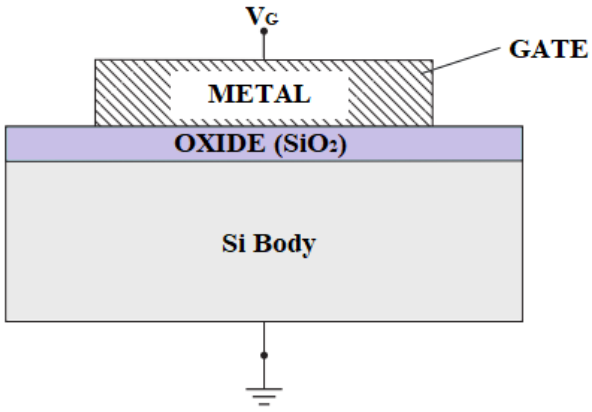


Figure 5.33 - Generic MOS Capacitor Structure [230].

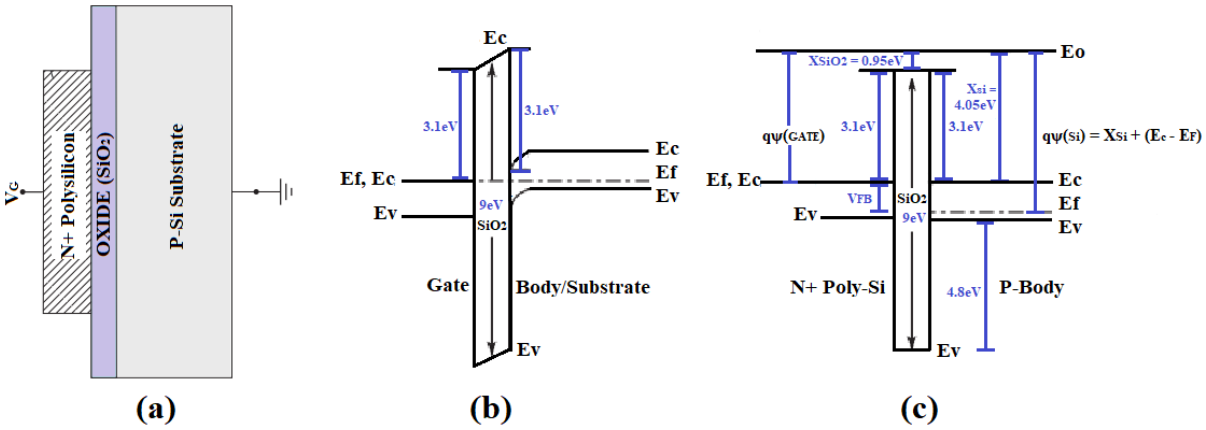


Figure 5.34 - (a) MOS capacitor structure (b) MOS capacitor energy band diagram with no applied gate voltage (c) MOS Capacitor energy band diagram at the flat-band condition when an applying a voltage equal to V_{FB} between the polysilicon gate and P-silicon body, where E_O is the energy level of vacuum [230].

5.4.2 MOS Structure during Surface Accumulation

If the voltage applied to the gate's polysilicon is negative enough (taking that the substrate is grounded and a P-type body), holes are attracted from the substrate bulk body, towards the surface, that is at the interface between the MOS capacitor dielectric oxide and the semiconductor (Si-SiO_2 interface). This forms an area close to this interface, where there is a large concentration of holes, known as the accumulation layer. Since the accumulated charge carriers are holes (for a P-type substrate but can be electrons for an N-type substrate), these holes are referred to as accumulation-layer holes, and the corresponding charge concentration as accumulation charge (Q_{ACC}) This phenomenon is known as surface accumulation and is illustrated in Figure 5.35. The accumulated holes can respond to an AC signal, offset by the negative DC voltage applied to the polysilicon gate. Consequently, the capacitance of the MOS structure is equal to the oxide layer capacitance under accumulation conditions and is provided by the following [224],[230]:

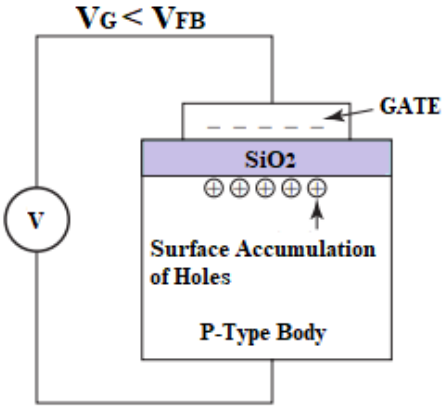


Figure 5.35 – MOS structure under surface accumulation [230].

$$V_G = V_{FB} + V_{SURF} + V_{OX} \tag{5.109}$$

where V_G is the gate voltage (V), V_{FB} is the flat-band voltage (V), V_{SURF} is the surface voltage (V), and V_{OX} is the oxide voltage (V).

At the flat band, the gate voltage (V_G) is equal to the flat band voltage (V_{FB}), while the surface voltage (V_{SURF}) is 0V since there is no surface accumulation, and the oxide voltage (V_{OX}) too, is 0V as there is no net electric field across the oxide. This satisfies Equation 5.109. When the MOS structure goes through surface accumulation, the gate voltage (V_G) is no longer equal to the flat-band voltage (V_{FB}), and hence according to Equation 5.109, the remaining voltage difference is due to the oxide voltage (V_{OX}) and the surface voltage (V_{SURF}). This latter parameter for a first order approximation is negligible in relation to the oxide voltage (V_{OX}), and hence during surface accumulation Equation 5.109, can be approximated to Equation 5.110 [230].

$$V_{OX} = V_G - V_{FB} \tag{5.110}$$

Hence the electric flux (ϕ_{OX}) within the MOS structure during surface accumulation is obtained through Gauss's Law, described by Equation 5.111.

$$\phi_{OX} = -\frac{Q_{SUB}}{\varepsilon_{OX}} \tag{5.111}$$

Where Q_{SUB} is the total charge in the substrate including the accumulated charge at the surface (C), ε_{OX} is the permittivity of the oxide (F/m). Hence the oxide voltage can be expressed as:

$$V_{OX} = \phi_{OX} t_{OX} = -\frac{Q_{ACC}}{C_{OX}} \tag{5.112}$$

Where t_{OX} is the oxide thickness (m), Q_{ACC} is the accumulated charge (C/m^2) and C_{OX} is the oxide capacitance (F/m^2). Essentially Equation 5.112, is a standard capacitor equation (Q = CV). Hence the oxide capacitance can be expressed as:

$$Q_{ACC} = -C_{OX}(V_G - V_{FB}) \tag{5.113}$$

Therefore, the MOS structure during surface accumulation behaves like a capacitor, but with an offset in the voltage by the flat band voltage (V_{FB}). It is important to note that in MOS capacitor theory, the voltage is taken at the gate, while the charge is the substrate charge, hence the negative sign in Equation 5.112, unlike in standard capacitors where charge and voltage are referenced to the same terminal [230].

5.4.3 MOS Structure during Surface Depletion

If the negative gate bias increases to a less negative value or to zero, less holes will move towards the oxide-semiconductor (Si-SiO_2) interface and hence surface accumulation will start to decay. Hence the MOS structure can be modelled as the oxide capacitance (C_{OX}) in series with a semiconductor layer (C_{Si}) capacitance. This yields to a slightly lower MOS capacitance value when compared to the MOS structure capacitance during surface accumulation [224]. If a gate voltage (V_G) greater than the flat-band voltage (V_{FB}) is applied, a depletion region at the oxide-semiconductor interface. is formed. This phenomenon is known as surface depletion and is illustrated in Figure 5.36. Hence Equation 5.109 translates to the following.

$$V_{OX} = -\frac{Q_{SUB}}{C_{OX}} = -\frac{Q_{DEP}}{C_{OX}} = \frac{qN_a w_{DEP}}{C_{OX}} \tag{5.114}$$

Where Q_{DEP} is the depletion charge concentration and is negative due to acceptor ions which accept the extra electrons hence getting negatively charged, q electronic charge 1.602×10^{-19}C, N_a is the bulk doping concentration (cm^{-3}) and w_{DEP} is the depletion region width (m) and is provided by Equation 5.115 [224], [230].

$$w_{DEP} = \sqrt{\frac{2\varepsilon_o \varepsilon_{Si} V_{SURF}}{qN_a}} \tag{5.115}$$

and hence

$$V_{SURF} = \frac{qN_a {w_{DEP}}^2}{2\varepsilon_o \varepsilon_{Si}} \tag{5.116}$$

where ε_{Si} is the relative permittivity of the semiconductor, ε_o is the absolute permittivity (8.85×10^{-12} F/m). Hence utilizing Equations 5.114 and 5.116 into Equation 5.109, yields to the quadratic equation described by Equation 5.117.

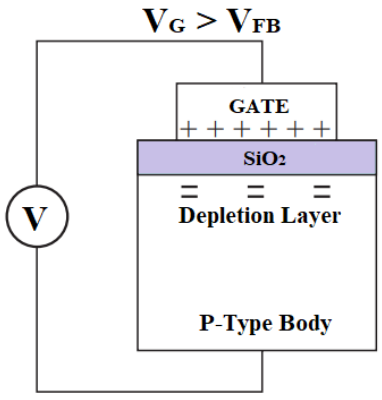


Figure 5.36 - MOS structure under surface depletion [230].

By rearranging this latter equation, the depletion region width (w_{DEP}) can be determined in terms of the gate voltage (V_G), hence leading to the determination of oxide voltage (V_{OX}) and surface voltage (V_{SURF}) during surface depletion, through Equations 5.114 and 5.116 respectively [224].

$$V_G = V_{FB} + \frac{qN_a w_{DEP}}{C_{OX}} + \frac{qN_a {w_{DEP}}^2}{2\varepsilon_{Si}} \tag{5.117}$$

During surface depletion, the MOS structure capacitance model can be still considered as an oxide layer capacitance (C_{OX}) in series with a semiconductor capacitance (C_{Si}) (the semiconductor capacitance is due to the formation of a depletion region, where the depleted layer acts as the dielectric and the semiconductor acts as the conducting terminals hence forming a capacitor structure). By considering the simple parallel plate capacitor structure ($C= \varepsilon A/d$), increasing the width of the depletion region yields to a smaller semiconductor capacitance (C_{Si}). This yields to the overall reduction of the MOS structure capacitance [224].

5.4.4 MOS Structure during Threshold Condition

If the gate bias voltage continues to increase, it will eventually lead to the formation of an inversion layer at the oxide-semiconductor (Si-SiO_2) interface. The initial stage of this phenomenon is known as weak inversion. The term inversion refers to the fact that the surface is inverted from P-type to N-type (for a P-body structure). During weak inversion the oxide-semiconductor (Si-SiO_2) interface does not remain in depletion but at the threshold of inversion. For a P-type body, the threshold condition arises when the surface electron concentration (n_s) is equal to the bulk body concentration (N_a). The surface voltage at the threshold condition (V_{SURF_TH}) is provided by Equation 5.118 [230]:

$$V_{SURF\_TH} = 2\frac{kT}{q} ln \frac{Na}{ni} \tag{5.118}$$

Where k is the Boltzmann constant 1.38064852 × 10^{-23} m^2 kg s^{-2} K^{-1}, T is the temperature in Kelvin, q is the electronic charge 1.602x10^{-19}C, N_a is body doping concentration (cm^{-3}) and n_i is the intrinsic carrier density of the semiconductor (carrier density of semiconductor which has not been doped. This parameter is temperature dependent).

Hence utilizing Equation 5.109, the gate voltage (V_G) at the threshold condition, that is the threshold voltage (V_{TH}), is provided by Equation 5.119. When the MOS structure is in weak inversion condition, the MOS capacitance behaves like the depletion condition and decreases as the bias voltage increases [230].

$$V_{TH} = V_{FB} + 2\frac{kT}{q}\ln\left(\frac{Na}{ni}\right) + 2\frac{\sqrt{kTN_a\varepsilon_{Si}\ln\left(\frac{Na}{ni}\right)}}{C_{OX}} \quad (5.119)$$

5.4.5 MOS Structure during Strong Inversion

If the positive gate bias is applied further, a strong inversion layer is formed. This is illustrated in Figure 5.37. On the other side when the strong inversion layer is formed, any further increase in the applied gate voltage across the dielectric oxide, does not reflect in an increase in the width of the depletion layer, hence reaching a maximum value (w_{DEP_MAX}). This is since the surface voltage (V_{SURF}) of the substrate will reach a saturation value and hence will not increase further. Equation 5.120 provides the corresponding maximum width of the depletion region under strong inversion [230].

$$w_{DEP\_MAX} = 2\sqrt{\frac{\varepsilon_{Si}kT\ln\left(\frac{Na}{ni}\right)}{N_a}} \quad (5.120)$$

Again, utilising Equation 5.109, the gate voltage under strong inversion is provided by Equation 5.121.

$$V_G = V_{FB} + 2\frac{kT}{q}\ln\left(\frac{Na}{ni}\right) - \left(\frac{Q_{DEP}}{C_{OX}} + \frac{Q_{INV}}{C_{OX}}\right) \quad (5.121)$$

$$V_G = V_{FB} + 2\frac{kT}{q}\ln\left(\frac{Na}{ni}\right) + 2\frac{\sqrt{kTN_a\varepsilon_{Si}\ln\left(\frac{Na}{ni}\right)}}{C_{OX}} - \left(\frac{Q_{INV}}{C_{OX}}\right) \quad (5.122)$$

Where Q_{INV} is the charge per unit area due to the inversion layer. Hence:

$$V_G = V_{TH} - \frac{Q_{INV}}{C_{OX}} \quad (5.123)$$

$$\therefore Q_{INV} = -C_{OX}(V_G - V_{TH}) \quad (5.124)$$

Equation 5.124 shows that the MOS structure during strong inversion essentially behaves as a capacitor except for the voltage offset of the threshold voltage (V_{TH}). Hence when the gate voltage (V_G) is at the threshold voltage the charge per unit area due to the inversion layer is zero [230].

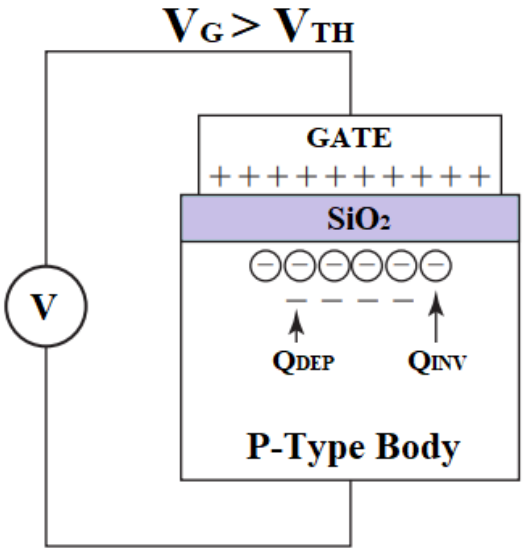


Figure 5.37 – MOS structure under strong inversion [230].

5.4.6 MOS Structure under high frequency AC

The inversion layer charge (Q_{INV}) takes significant time to develop as the P-type body is an inefficient supplier of electrons and produces only electrons through thermal generation, hence at a slow rate (10s to 100s). This means that the inversion layer cannot respond to high frequency AC signal and therefore the inversion layer charge during high frequency AC will essentially remain at its low frequency value [224]. The high frequency AC signal will cause the surface voltage (V_{SURF}) to oscillate, hence causing the depletion region width (w_{DEP}) to oscillate too around the maximum depletion region width (w_{DEP_MAX}). Hence in the high frequency scenario the MOS structure capacitance is modelled as the series combination of the oxide layer capacitance (C_{OX}) and the semiconductor layer capacitance (C_{Si}). When the thickness of the depletion layer reaches a maximum value, this yields to the MOS structure capacitance to saturate to a minimum value [230].

5.4.7 IGBT Input Capacitances in relation to the MOS Structure

Figure 5.38 shows the IGBT cell structure with the different parasitic capacitances. The gate-emitter capacitance (C_{GE}) is made up of three parasitic sub-capacitances: the capacitance due to the overlap between the gate and the P^+ semiconductor (C_{P+}), the capacitance due to the overlap between the gate and the N^+ semiconductor (C_{N+}), and the capacitance between the overlap of the gate and the emitter metallization (C_{GMe}) [224].

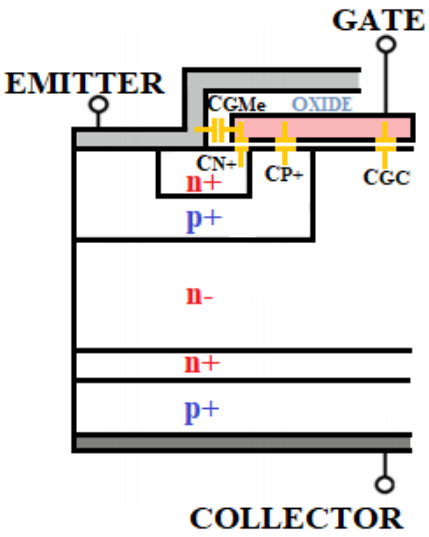


Figure 5.38 – IGBT cell structure input parasitic capacitances.

For the low frequency conditions, the gate-emitter capacitance's (C_{GE}) inversion layer is formed and hence this MOS capacitance can be considered as a single oxide layer capacitance. As discussed earlier, under high frequency condition, the inversion layer cannot be created immediately, and the MOS capacitance is modelled as an oxide layer capacitance in series with a depletion layer capacitance. Out of the three sub-capacitances forming up the combined gate-emitter parasitic capacitance (C_{GE}), the capacitance due to the overlap between the gate and the P^+ semiconductor (C_{P+}) is considered predominant, with the capacitance due to the overlap between the gate and the N^+ semiconductor (C_{N+}), and the capacitance between the overlap of the gate and the emitter metallization (C_{GMe}), are considered negligible. This is mainly due to the limited overlap area of the latter two capacitances when compared to the larger overlap area of the capacitance formed by the gate and the P^+ semiconductor (C_{P+}) [224]. Hence this latter capacitance is of the MOS structure type, with a P-body, but with the salient differences from the generic MOS structure, that the body is heavily doped, and the emitter metallization is shorting the P-body, with the N^+ region. Thus, with this configuration, the formation of the inversion layer is no longer slow, since the P-body will not be a weak supplier of electrons, yielding to the fast formation of the inversion layer. Hence, the capacitance due to the overlap between the gate and the P^+ semiconductor (C_{P+}), which is the predominant part of the gate-emitter capacitance (C_{GE}), can be considered as a single oxide layer capacitance under high frequency operation [224]. Hence, the gate-emitter capacitance (C_{GE}), can be calculated by the following Equation 5.125.

$$C_{GE} = \varepsilon_0 \varepsilon_{OX} \frac{A_1}{t_{OX}} \tag{5.125}$$

Where ε_{OX} is the relative permittivity of the dielectric oxide, ε_o is the absolute permittivity (8.85 x 10^{-12} F/m), A_1 is the overlap area of the gate with the P^+ region (m^2) and t_{OX} is the thickness of the gate oxide (m).

As illustrated in Figure 5.38, the collector-gate Miller capacitance (C_{CG}), is a MOS structure, but with an N-body, provided by the N^- drift region. The collector-gate Miller capacitance can be modelled as an oxide layer capacitance in series with a semiconductor layer capacitance. Based on the gate drive level, this latter capacitance changes from surface accumulation to depletion circumstances such that under hard depletion the gate-collector capacitance (C_{CG}) is provided by Equation 5.126 [224].

$$C_{CG} = \frac{C_{OX}C_{Si}}{C_{OX}+C_{Si}} \tag{5.126}$$

Where C_{OX} is the oxide layer capacitance, and C_{Si} is the semiconductor layer capacitance due to depletion and is provided by Equation 5.127,

$$C_{Si} = \varepsilon_o \varepsilon_{Si} \frac{A_2}{W_{DEP}} \tag{5.127}$$

Where A_2 is the overlap area of the gate and the N^- drift region (N substrate) (cm^2) and W_{DEP} is the width of the depletion region, provided by Equation 5.115 and is dependent on the surface voltage (V_{SURF}) (m). The larger the surface voltage (V_{SURF}), the larger the degree of depletion, the larger the depletion region width and hence the smaller the semiconductor layer capacitance (C_{Si}). This yields to an overall decrease of the collector-gate capacitance (C_{CG}) with increasing surface voltage (V_{SURF}) where this latter parameter is directly related to the collector-emitter voltage (V_{CE}). This leads to the non-linear relationship of the collector-gate Miller capacitance (C_{CG}) with the collector-emitter voltage (V_{CE}) as illustrated in Figure 5.5. According to Tan et al. [224], the above model, is considered limiting as the N^- drift region under the gate, is full of carriers during the switching period. As discussed earlier, during turn-off for an IGBT switching an inductive load, the collector current (I_C) remains at the on-state level until the collector-gate voltage (V_{GC}) reaches the DC link voltage. To sustain this collector current (I_C), the carrier density in the N^- drift layer remains at high levels, even when the depletion layer starts to form, exceeding the doping level of the N^- drift region. This highlights the limitation of the above model, with the depletion layer approximation as provided by Equation 5.126, becoming unsuitable due to the above phenomenon. The above collector-gate capacitance (C_{CG}) approximation provided by Equation 5.127 is not complete during switching and hence

Tan. et al. [224] modified it to include the collector current (I_C) dependence. The carrier density during depletion N_t is provided by Equation 5.128.

$$N_t \approx N_B + \frac{I_C}{qAv_{SAT}} \tag{5.128}$$

Where N_B is the N^- drift region doping level (cm^{-3}), I_C is the collector current (A), q is the electronic charge $1.602x10^{-19}C$, A is the effective N^- drift region conducting area (cm^2) and v_{sat} is the carrier saturation velocity (cm/s). Under depletion the Tan. et al. [224] approximation includes an empirical parameter (γ) which relates to the effective carrier density, to make the depletion dependent on the collector current (I_C).

$$C_{Si} = \varepsilon_o \varepsilon_{Si} \frac{\gamma A_2}{W_{DEP}} \tag{5.129}$$

Moreover, the width of the depletion region (w_{DEP}) was approximated through Equation 5.130.

$$w_{DEP} = \sqrt{\frac{2\varepsilon_O \varepsilon_{Si} V_{CE}}{qN_t}} \tag{5.130}$$

5.5 IGBT Modelling of the Turn-On and Turn-Off Transients' Evolution with Ageing

This section will discuss the observed changes in the measured turn-on and turn-off transients of the tested IGBTs, when subjected to the implemented accelerated ageing, yielding to the modelling of the IGBT's transients, including ageing effects. The discussion will be based on the obtained transients of the International Rectifier IRG4BC30KD and ST Microelectronics STGP19N60KD. All tested IGBTs for both International Rectifier IRG4BC30KD and ST Microelectronics STGP19N60KD manifested significant changes during the turn-off transients. This was discussed in Section 4.5.1 and illustrated in Figure 4.9 for the IRG4BC30KD IGBT, and in Section 4.6.1 and illustrated in Figure 4.32 for the STGP19N60KD IGBT. On the other side marginal changes were observed during the turn-on transients. This was discussed in Section 4.5.2 and illustrated in Figure 4.18 for the IRG4BC30KD IGBT, and in Section 4.6.2 and illustrated in Figure 4.33 for the STGP19N60KD IGBT. The following were the observed changes during the different phases.

5.5.1 IGBT Turn-Off Transient during Phase 1

During this phase, the collector-emitter voltage (V_{CE}) transient, experienced minimal changes after subjecting the IGBTs to the implemented accelerated ageing procedure. This is evidenced within Figure 5.39, highlighting that the rate of change of the,

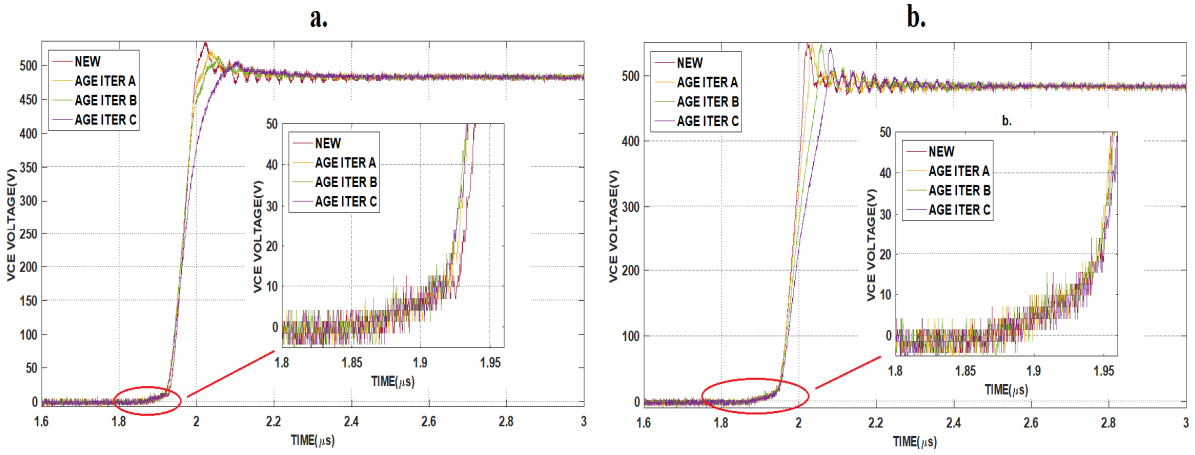


Figure 5.39 – IGBT Collector-Emitter Voltage (V_{CE}) Transient Turn-Off Phase 1 (a) IRG4BC30KD IGBT Sample 14 (b) STGP19N60KD IGBT Sample 1

collector-emitter voltage (dV_{CE}/dt), remained relatively unchanged. This is valid for the two IGBT types. In relation to the collector current (I_C) transient, this too remained relatively unchanged as evidenced in Figure 5.40. Table 5.13 tabulates the corresponding measured collector-emitter voltage rate of change (dV_{CE}/dt) and the measured collector current rate of change (dI_C/dt) for each age iteration, for IGBT IRG4BC30KD Sample 14.

AGE ITERATION	Measured Collector-Emitter Voltage Rate of Change $dV_{CE}/dt_{(PH1\_OFF)}$ (V/µs)	Measured Collector Current Rate of Change $dI_C/dt_{(PH1\_OFF)}$ (A/µs)
NEW	88.19	5.09
AGE ITERATION A	94.49	5.29
AGE ITERATION B	99.22	5.48
AGE ITERATION C	102.98	5.59

Table 5-13 – IRG4BC30KD IGBT Sample 14 Turn-Off Phase 1 Collector-Emitter Voltage (dV_{CE}/dt) and Collector Current (dI_C/dt) Evolution with Ageing

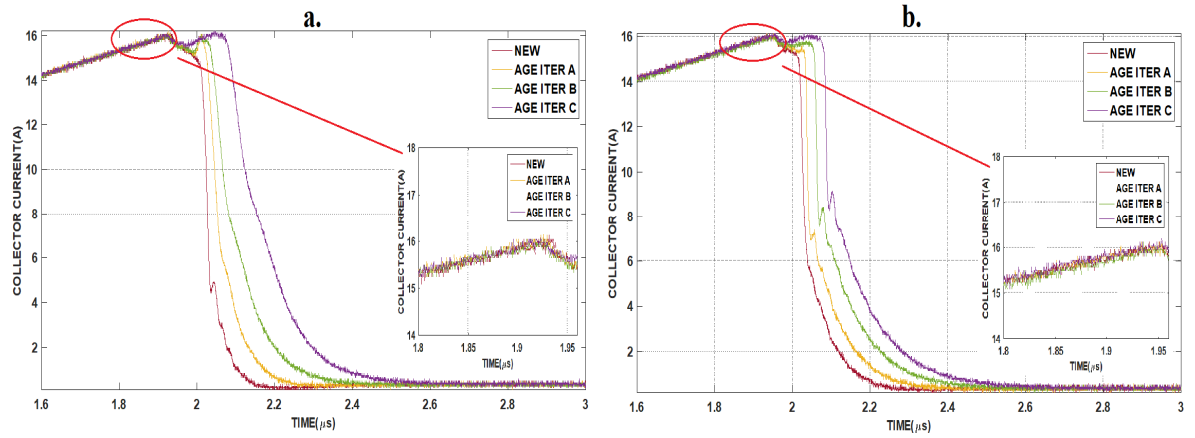


Figure 5.40 - IGBT Collector Current (I_C) Transient Turn-Off Phase 1 (a) IRG4BC30KD IGBT Sample 14 (b) STGP19N60KD IGBT Sample 1

5.5.2 IGBT Collector-Emitter Voltage (V_{CE}) Turn-Off Transient during Phase 2

This phase was characterized by substantial changes in the collector-emitter voltage (V_{CE}) transient, with a general decrease in the collector-emitter voltage rate of change (dV_{CE}/dt) with each age iteration. This is highlighted (orange section) in Figure 5.41 and tabulated in Table 5-14. Moreover, one can notice that for the new IGBT, the collector-emitter voltage rate of change ($dV_{CE}/dt_{(PH2\_OFF)}$) remained constant until reaching the off-state output voltage (V_{DC}). On the other side, for the consequent age iterations, the collector-emitter voltage rate of change ($dV_{CE}/dt_{(PH2\_OFF)}$), did not remain constant for the entire output voltage range. This can be observed in the latter stage of the collector-emitter voltage (V_{CE}) turn-off transient, highlighted in Figure 5.41 (blue section).

AGE ITERATION	Measured $dV_{CE}/dt_{(PH2\_OFF)}$ (V/µs)	Modelled $dV_{CE}/dt_{(PH2\_OFF)}$ (V/µs)
NEW	7885.71	7652.18
AGE ITERATION A	6519.40	7050.49
AGE ITERATION B	5000.48	5672.14
AGE ITERATION C	3219.05	4873.18

Table 5-14 – Measured and Modelled IGBT Sample 14 dV_{CE}/dt Phase 2 Evolution with Ageing

During this phase, for a new IGBT, the collector-emitter voltage (V_{CE}), is essentially linear, following the collector-emitter voltage rate of change ($dV_{CE}/dt_{(PH2(OFF))}$) modelled in the piecewise linear model approach via Equation 5.40. As evidenced in Table 5-15, for the IRG4BC30KD IGBT, with each age iteration both the forward transconductance (g_m) and the threshold voltage (V_{TH}) changed, decreasing, and increasing respectively Hence, for the linear piecewise model, to provide the best linear fit, reflecting the above parameters' changes, and the decreasing collector-emitter rate of change ($dV_{CE}/dt_{(PH2(OFF))}$), Equation 5.40 yields to an,

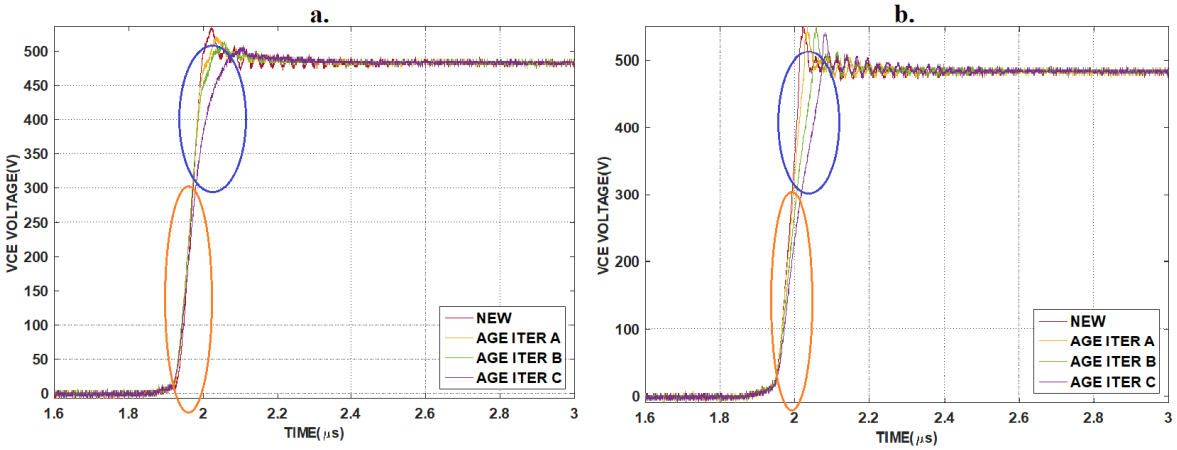


Figure 5.41 – Collector-Emitter Voltage (V_{CE}) turn-off transient Phase 2 (a) IRG4BC30KD IGBT Sample 14 (b) STGP19N60KD IGBT Sample 1

AGE ITERATION	NEW	AGE ITERR. A	AGE ITERR. B	AGE ITERR. C
V_{TH} (V)	5.38185	5.78505	5.93880	6.02545
g_m(S)	6.1050	5.7998	5.4945	5.1893
C_{CG2}(pF)	36.5	37.3	47	56.3
C_{CG1}(nF)	2.6	2.6	2.6	2.6

Table 5-15 - IRG4BC30KD IGBT Sample 14 Measured and Linear Piecewise Model Parameters Evolution with Ageing in relation to collector-voltage (V_{CE}) turn-off transient Phase 2.

increase in the equivalent high voltage collector-gate Miller capacitance (C_{CG2}), as indicated in Table 5-15. It is important to point out that since the collector-emitter voltage rate of change during the turn-off Phase 1 ($dV_{CE}/dt_{(PH1(OFF))}$), remained relatively unaltered, the equivalent low voltage collector-gate Miller capacitance (C_{CG1}) was retained the same value, for the different age iterations linear piecewise modelling. This is tabulated in Table 5-15. Figure 5.42 illustrates the corresponding Phase 1 and 2 collector-emitter voltage (V_{CE}) turn-off transient, linear piecewise model implementation for the different age iterations with the modelled collector-emitter voltage rate of change ($dV_{CE}/dt_{(PH2\_OFF)}$) variation with ageing as tabulated in Table 5-14.

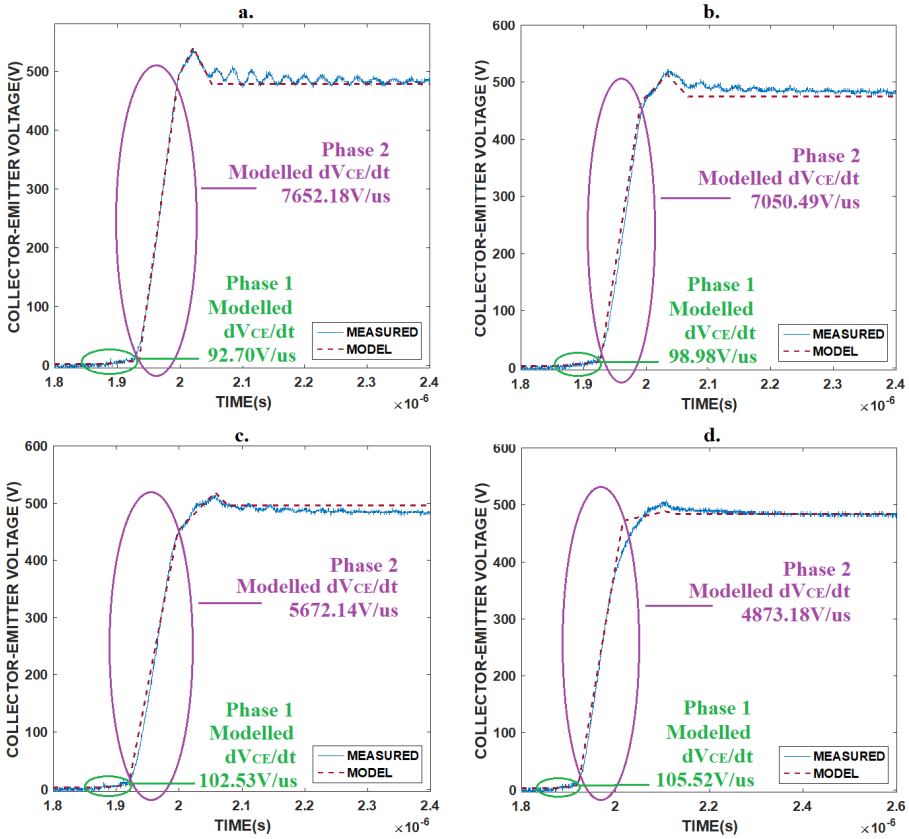


Figure 5.42 - Collector-Emitter Voltage (V_{CE}) turn-off transient, Phase 1, and Phase 2, IRG4BC30KD IGBT Sample 14, Linear Piecewise Model (a) New (b) Age Iteration A (c) Age Iteration B (d) Age Iteration C

As illustrated in Figures 5.41 and 5.42, as the accelerated ageing progressed, the collector-emitter voltage rate of change ($dV_{CE}/dt_{(PH2(OFF))}$) decreased. Moreover, this parameter did not remain constant during Phase 2, but manifested a further decrease, as the collector-emitter voltage (V_{CE}) approaches the off-state output voltage (V_{DC}) as can be noted within the blue section of Figure 5.41. Based on Equation 5.40, this latter observation indicates, that the sole increase of the equivalent high voltage collector-gate Miller capacitance (C_{CG2}) does not model sufficiently the observed ageing effects. Figure 5.5 already indicates the non-linear dependence of this capacitance with the corresponding collector-emitter voltage (V_{CE}). Hence, the above observation indicates that if the observed ageing changes are exclusively due to changes in the collector-gate capacitance (C_{CG}), then the relationship of this capacitance with the corresponding voltage is altered too, suggesting that the implemented accelerated ageing is degrading this parasitic capacitance. What is evident is the fact that the linear piecewise transient model, is not enough to effectively model the collector-emitter voltage (V_{CE}) turn-off transient during Phase 2. Predominantly the above observation is related to what is happening within the gate voltage (V_G) transient. The linear rise of the collector-emitter voltage (V_{CE}) during this phase is dependent on the fact that the gate current is predominantly passing through the Miller capacitance (C_{CG}). This happens during the Miller Plateau section, where the gate voltage (V_G) is relatively constant. This is visible for a new device within Figure 5.43(a). As soon as the Miller plateau elapses, the output collector-emitter voltage (V_{DC}) is reached, with the gate voltage (V_G) falling abruptly, hence turning-off the device.

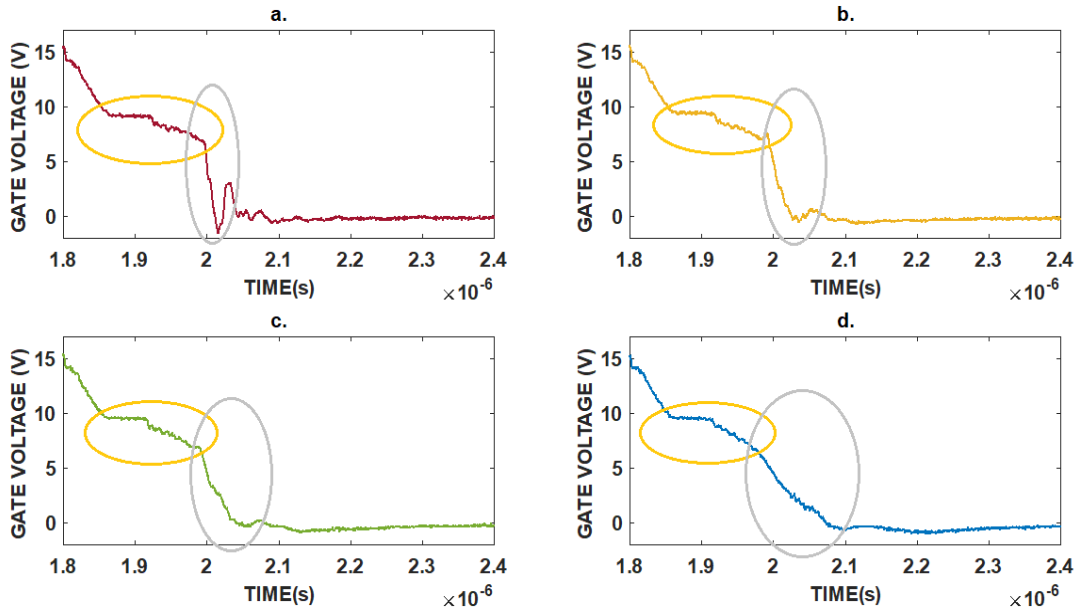


Figure 5.43 - Gate Voltage (V_G) turn-off transient, IRG4BC30KD IGBT Sample 14, Linear Piecewise Model (a) New (b) Age Iteration A (c) Age Iteration B (d) Age Iteration C

As the IGBT progresses through the implemented accelerated ageing procedure, one can notice that during turn-off, there is the contraction of the primary Miller plateau with the eventual extensive formation of a secondary Miller plateau. Largely, one can argue that there is the general elongation of the Miller plateau with the progression of the implemented accelerated ageing. This is illustrated in Figure 5.43, within the yellow and grey circles respectively. Figure 5.43(d), illustrates the gate voltage (V_G) of IRG4BC30KD IGBT Sample 14 for the Age Iteration C. It highlights the prelude of the formation of a secondary Miller plateau. This is more evident with the super positioning of this IGBT's gate voltage (V_G) transients for the different age iterations, as illustrated in Figure 5.44(a). Moreover, Figure 5.44(b) illustrates the superposed turn-off gate voltage (V_G) transients' evolution with ageing of IRG4BC30KD IGBT Sample 11. In this latter case, the device manifested harsher ageing effects, hence exhibiting further the formation of the secondary Miller plateau, contributing to the general elongation of this section during turn-off. The above phenomenon has been monitored in literature by Sundaramoorthy et al. [220] and utilized by Cottet et al. [221], to estimate the IGBT's junction temperature (T_J). In both cases, the IGBT's case temperature (T_C) was raised, while simultaneously monitoring the turn-off gate voltage (V_G) transient. An elongation in the turn-off Miller plateau was observed. The elongation extent was determined to be a function of the junction temperature (T_J) and hence it was utilized to estimate the value of this latter parameter during operation. This is depicted in Figure 5.45. In this case, the case temperature (T_C), was maintained at 25°C, with short pulse-duration. As depicted in Figure 5.44, one can still observe the turn-off Miller plateau elongation.

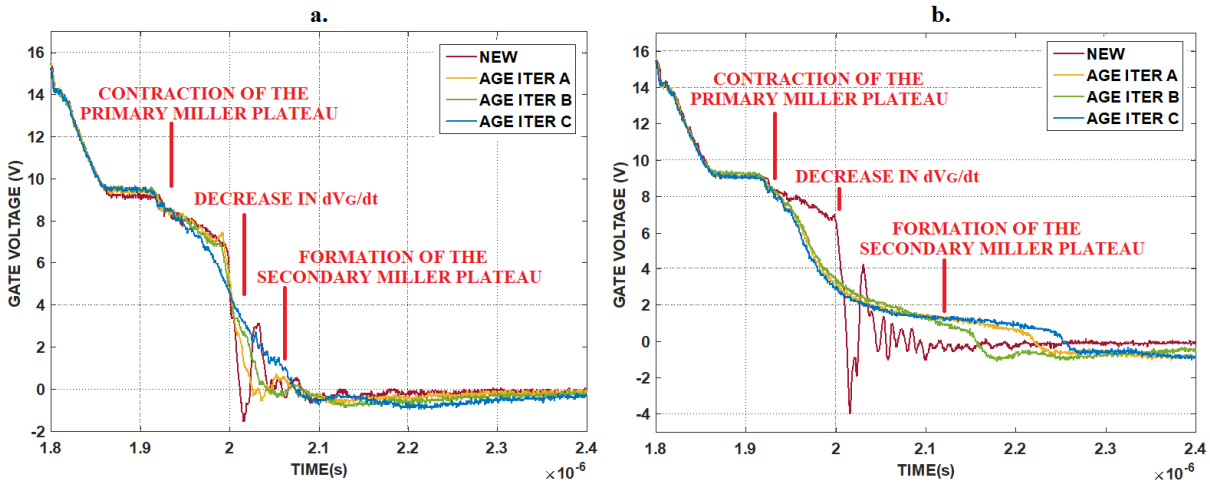


Figure 5.44 –Gate Voltage (V_G) turn-off transient evolution with ageing (a) IRG4BC30KD IGBT Sample 14 (b) IRG4BC30KD IGBT Sample 11

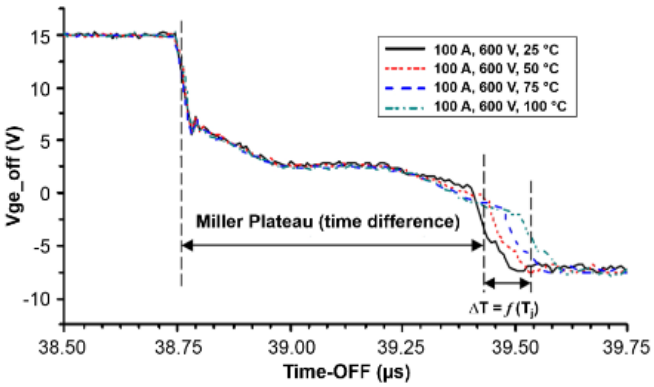


Figure 5.45 – Elongation of the IGBT's Miller Plateau during turn-off [221].

This is a direct consequence of the degraded die-attach, as evidenced in Chapter 3, contributing to the deterioration of the junction's thermal path (enhanced thermal impedance(θ_{JC})). The deteriorated thermal path increases the IGBT's junction temperature (T_J), contributing to the manifestation of the observed turn-off Miller plateau elongation after each age iteration, even though under the same thermal (T_C = 25°C) and electrical test conditions. This is the result of intrinsic IGBT degradation and ageing, rather than a consequence of external effects. Hence the final further slow-down of the collector-emitter voltage (V_{CE}) transient during Phase 2, is due to the general elongation of the Miller plateau and hence a general slow-down of the gate voltage (V_G) transient, which is due to an intrinsic increase of the junction temperature (T_J), catalyzed by the die-attach degradation and provoked by the implemented accelerated ageing.

To understand the physical reasons for the above, it is required to delve in the physical MOS structure of the collector-gate capacitance (C_{CG}). As described in Section 5.4.7 and illustrated in Figure 5.38, the MOS structure of the collector-gate capacitance (C_{CG}), is made up of the series combination of two parasitic capacitances. The first capacitance (C_{OX}) is composed of the gate metal electrode, the gate oxide, and the top of the semiconductor N^- layer. This structure is predominantly fixed and minimally varies with the dynamic electrical operation, The second capacitance is due to the extension of the depletion region of the collector junction and occurs when the IGBT is in the off state. The variation in the depletion region size, is essentially varying the width of this capacitance dielectric. As indicated in Equation 5.130, the width of the depletion region is dependent on the collector-emitter voltage (V_{CE}) [11], [224]. Hence the larger the collector-emitter voltage (V_{CE}), the larger the collector-gate voltage (V_{CG}), leading to an enhanced depletion layer width, and hence to a smaller value of the depletion semiconductor capacitance (C_{Si}). This yields to the domination of this latter capacitance on the series combination making up the collector-gate capacitance (C_{CG}), and hence to a lower value as the collector-emitter voltage (V_{CE}) increases, as indicated in Figure 5.5.

Equation 5.130, sheds light on the turn-off elongation of the Miller plateau, as accelerated ageing progresses, through the corresponding increase of the collector-gate capacitance (C_{CG}), caused by an increase of the junction temperature (T_J), triggered by a degradation of the die-attach. This is since, if the junction temperature (T_J) increases, it will trigger an enhanced presence of charge carriers in the N^- drift region of the IGBT, hence obtaining an increase in the carrier density (N_t). It is important to point out that an increase in the junction temperature (T_J) will trigger an increase in the N^- drift region doping level (N_B), as the other term due to the collector-current (I_C), is minimally influenced by the accelerated ageing procedure, as this was dictated by the experimental procedure of the Double Pulse test, which was kept constant during the different age iterations characterization. Hence for the same characterization conditions (collector current (I_C) and collector-emitter voltage (V_{CE})), the above phenomenon causes the semiconductor capacitance due to the depletion (C_{Si}) to increase, resulting in an overall increase of the collector-gate Miller capacitance (C_{CG}), thus contributing to the slow-down of the collector-emitter voltage rate of change during turn-off Phase 2, as illustrated in Figure 5.42.

Now from a non-linear model analysis point of view, the collector-emitter voltage (V_{CE}) turn-off transient during Phase 1 and Phase 2, due to the implemented accelerated ageing, can be divided mainly into three subphases, as illustrated in Figure 5.46:

- The first subphase is characterized by a low rate of change, due to the large non-linear Miller capacitance (C_{CG}), at low collector-emitter voltage (V_{CE}), (C_{CG1}). This phase was minimally affected by the implemented accelerated ageing.
- The second subphase is characterized by a large rate of change, due to the stabilization of the Miller capacitance (C_{CG}) to a lower value (C_{CG2}), occurring when the voltage across this capacitance increases during the Miller plateau. With ageing the rate of change during this section decreased, and was attributed to a general increase of the Miller capacitance at high voltage (C_{CG2})
- The third subphase is due to the elongation of the Miller plateau due to an increase in the junction temperature (T_J). This led to a further decrease in collector-emitter voltage rate of change (dV_{CE}/dt) from the rate of change (dV_{CE}/dt) during subphase 2.

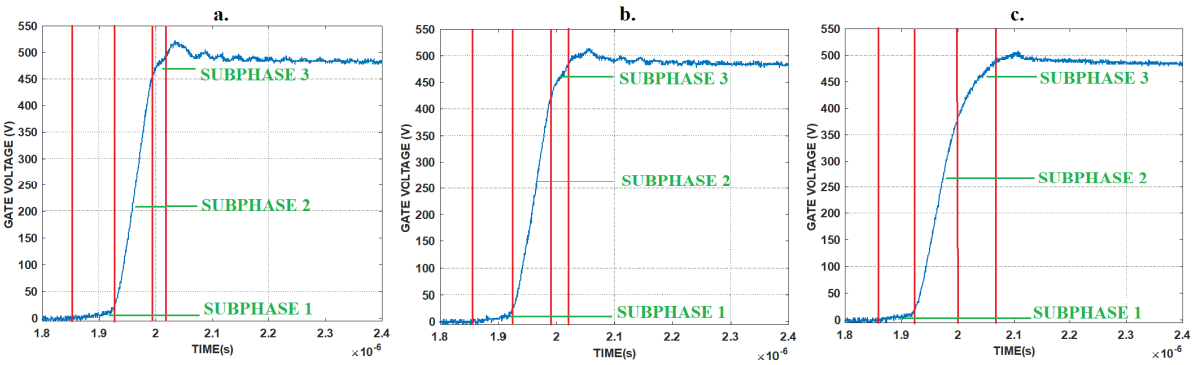


Figure 5.46 - IGBT IRG4BC30KD Sample 14 highlighting the different subphases (a) Age Iteration A (b) Age Iteration B (c) Age Iteration C.

The non-linear mathematical function proposed for a new IGBT for the collector-emitter voltage transient during Phase 1 and Phase 2, as described in section 5.3.5, is not suitable to describe the transient changes due to the implemented accelerated ageing, as illustrated in Figure 5.46. This is mainly due to the changes occurring during sub-phase 3. Hence a new mathematical function is proposed to cater for the ageing changes. This mathematical function which describes the entirety of the above three phases; should not include any maxima, must include a non-stationary point of inflection (at the mid-point of subphase 2), transiting the function from concave up (subphase 1) to concave down (subphase 3) and it should be asymptotic to x-axis (V_{CE} = 0V) and to the off-state output collector-emitter voltage (V_{CE} = V_{DC}). It was postulated that the generic model function which suits best the above characteristics is provided by Equation 5.131, which essentially is a sigmoid function.

$$y = f(x) = \frac{1}{(1+e^{-x})} \tag{5.131}$$

1. *The function's 1st derivative*

$$\frac{dy}{dx} = \frac{d(\frac{1}{1+e^{-x}})}{dx} = \frac{d((1+e^{-x})^{-1})}{dx} = -\frac{\frac{d(1+e^{-x})}{dx}}{(1+e^{-x})^2} = \frac{e^{-x}}{(1+e^{-x})^2} \tag{5.132}$$

2. *The function's 2nd derivative*

$$\frac{d^2y}{dx^2} = \frac{d^2\left(\frac{1}{1+e^{-x}}\right)}{dx^2} = \frac{d\left(\frac{e^{-x}}{(1+e^{-x})^2}\right)}{dx} = \frac{\frac{d}{dx}[e^x].(1+e^x)^2 - e^x.\frac{d}{dx}[(1+e^x)^2]}{((1+e^x)^2)^2} = \frac{e^{-2x}(1-e^x)}{(1+e^{-x})^3} \tag{5.133}$$

Figure 5.47 illustrates the plot of the above generic function and corresponding derivative, highlighting the characteristic requirements described earlier.

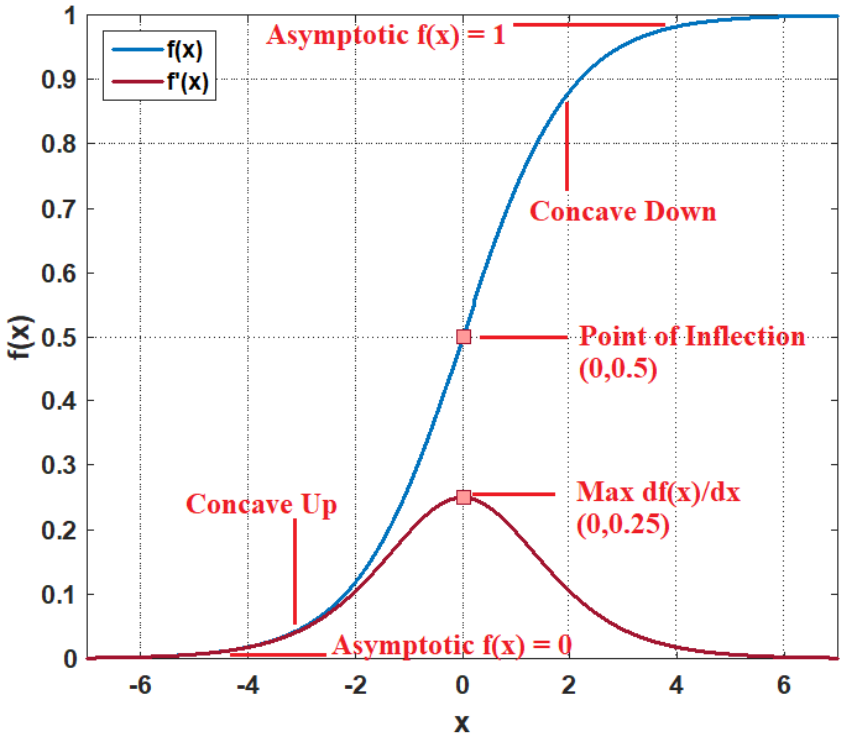


Figure 5.47 – IGBT Turn-Off Phase 1 & Phase 2 General V_{CE} Model Function and corresponding derivative for Aged IGBTs

Again, the above function was transformed to reflect the IGBT collector-emitter voltage (V_{CE}) characteristics as depicted in Figure 5.47. The following are the transformations required:

1. Introduce the time parameter (t) as the x-axis parameter
2. Introduce the collector-emitter voltage (V_{CE}) as the y-axis parameter.
3. Introduce the time parameter ($t_{\lambda_{2(OFF)}}$), corresponding to the x-position of the point of inflection, shifting the function horizontally such that the point of inflection is at the mid-point of sub-phase 2.
4. Stretch the function vertically such that it is upward asymptotic to the output off-state voltage (V_{DC}). For the above changes the function translates to the following:

$$V_{CE}(t) = \frac{V_{DC}}{\left(1 + e^{-(t - t_{\lambda_{2(OFF)}})}\right)}$$

5. Introduce the parameter ($\phi_{2(OFF)}$). This parameter controls the steepness of the above function, hence controlling the rate of change for the function to go from the on-state collector-emitter voltage (V_{CE_SAT}) to the off-state output voltage (V_{DC}). Hence the function translates to the following:

$$V_{CE}(t) = \frac{V_{DC}}{\left(1+e^{-\phi_{2(OFF)}(t-t_{\lambda_{2(OFF)}})}\right)} \tag{5.134}$$

Now the steepness or slope factor ($\phi_{2(OFF)}$) is given by considering the derivative of Equation 5.131 yielding to Equation 5.132 and hence Equation 5.135.

$$\frac{d(V_{CE}(t))}{dt} = \frac{V_{DC}\phi_{2(OFF)}e^{-\phi_{2(OFF)}(t-t_{\lambda_{2(OFF)}})}}{(1+e^{-\phi_{2(OFF)}(t-t_{\lambda_{2(OFF)}})})^2} \tag{5.135}$$

At the point of inflection, the time parameter $t = t_{\lambda_{2(OFF)}}$. Moreover, at this point the above function manifests the maximum collector-emitter voltage rate of change (dV_{CE}/dt), which can be approximated by the piecewise linear model equation of the collector-emitter voltage rate of change during the turn-off Phase 2 (dV_{CE}/dt_{PH2}), that is Equation 5.40. Therefore:

$$\frac{d(V_{CE}(t_{\lambda_{2(OFF)}}))}{dt} = \frac{V_{DC}\phi_{2(OFF)}}{4} \approx \frac{dV_{CE_{PH2}}}{dt} \approx \frac{V_{TH}+{}^{I_{C0}}/_{g_m}-V_{G-}}{R_g C_{cg2}} \tag{5.136}$$

$$Hence\ \phi_{2(OFF)} \approx \frac{4(V_{TH}+{}^{I_{C0}}/_{g_m}-V_{G-})}{V_{DC}R_g C_{cg2}} \approx \frac{4\{\frac{dV_{CE_{PH2}}}{dt}\}}{V_{DC}} \tag{5.137}$$

Based on the modelled collector-emitter rate of change ($dV_{CE}/dt_{(PH2\_OFF)}$) values, for IGBT IRG4BC30KD Sample 14, as listed in Table 5-14, the slope factor ($\phi_{2(OFF)}$), as computed through Equation 5.137, was determined to be $5.9x10^7 s^{-1}$ and $4.7x10^7 s^{-1}$, for Age Iteration A and Age Iteration B respectively. To obtain the best correlation with the measured transients

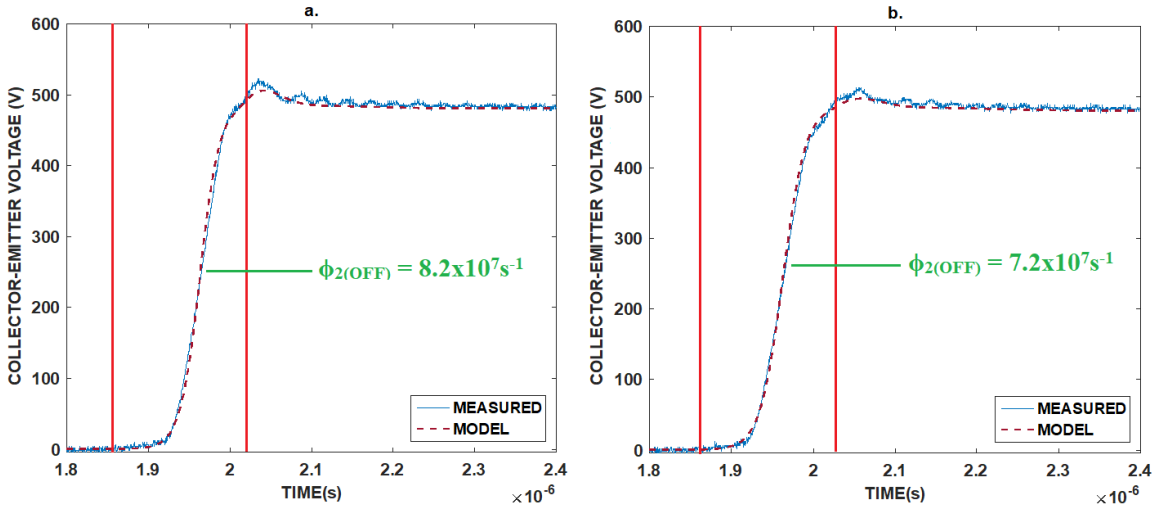


Figure 5.48 - Collector-Emitter Voltage (V_{CE}) turn-off transient, Phase 1, and Phase 2, IRG4BC30KD IGBT Sample 14, Non-Linear Model (a) Age Iteration A (b) Age Iteration B

the slope factors were optimized to $8.2x10^7s^{-1}$ and $7.2x10^7s^{-1}$, for Age Iteration A and Age Iteration B respectively. The above discrepancy was mainly due to the fact that the utilized modelled collector-emitter rate of change ($dV_{CE}/dt_{(PH2\_OFF)}$) values, as quoted in Table 5-14, are actually reflecting the best linear fit over the entire collector-emitter voltage (V_{CE}) range up to the off-state collector-emitter output voltage (V_{DC}), hence not translating to the maximum collector-emitter voltage rate of change (dV_{CE}/dt). When for Age Iteration A and Age Iteration B, the collector-emitter rate of change (dV_{CE}/dt) was measured close to half the off-state collector-emitter output voltage ($V_{DC}/2$), this led to a higher value of collector-emitter voltage rate of change (dV_{CE}/dt), yielding to the quoted optimized slope factor ($\phi_{2(OFF)}$) within Figure 5.48. For the consequent IRG4BC30KD Sample 14, Age Iteration C, harsher ageing effects were manifested, and the elongation of the Miller plateau will become more distinct. Hence the non-linear model provided by Equation 5.134, had to be modified to a weighted sigmoid function This is since the collector-emitter voltage (V_{CE}) transient, during the turn-off Phase 1 and Phase 2, tends to depart from the symmetricity occurring about half the off-state output voltage ($V_{DC}/2$), as was the case in the previous age iterations. One can observe that the transient tends to get slower in the second half. This is illustrated in Figure 5.46. Hence for this age iteration, the model function for turn-off Phase 1 and Phase 2, utilized two distinct values of slope factors, ($\phi_{2A(OFF)}$) $6.2x10^7s^{-1}$, for the transient modelling up to $V_{DC}/2$, and ($\phi_{2B(OFF)}$) $4.3x10^7s^{-1}$ for the transient modelling from $V_{DC}/2$ up to V_{DC}. These were computed utilizing two distinct values of the maximum collector-emitter rate of change (dV_{CE}/dt) for each section. This is illustrated in Figure 5.49.

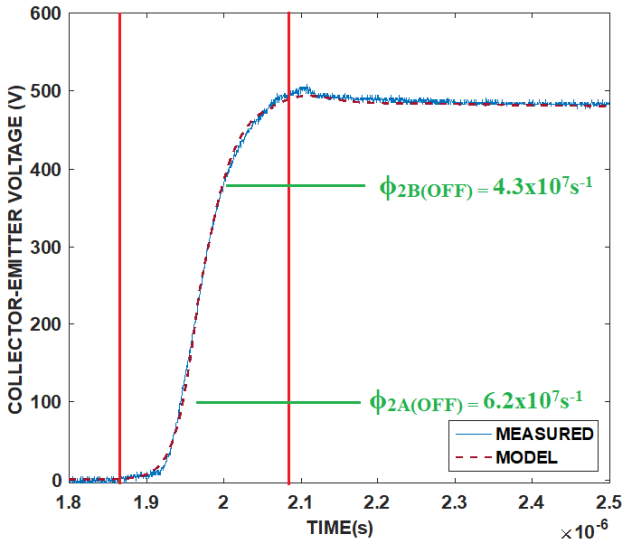


Figure 5.49 - Collector-Emitter Voltage (V_{CE}) turn-off transient, Phase 1, and Phase 2, IRG4BC30KD IGBT Sample 14, Non-Linear Model Age Iteration C.

Utilizing the approximation provided by Equation 5.137, hence highlighting the dependence of the slope factor ($\phi_{2(OFF)}$) on the Miller Capacitance (C_{CG}), this latter observation indicates that when the IGBT undergoes a certain ageing severity, there comes a point where the decrease in the Miller capacitance (to a stabilized value at high voltage (C_{CG2}), yielding to an enhanced collector-emitter voltage rate of change (dV_{CE}/dt)), at the beginning of the turn-off Phase 2, will be eventually compensated by the enhanced junction temperature (T_J) effects, manifesting in the elongation of the Miller plateau, hence yielding to a counter decrease in the collector-emitter voltage rate of change (dV_{CE}/dt), towards the end of the turn-off Phase 2 collector-emitter voltage (V_{CE}) transient.

Hence the above translates to the observation that when the IGBT undergoes a certain ageing severity, the Miller capacitance (C_{CG}) does not stabilize to the value at high voltage (C_{CG2}), as indicated in Figure 5.5, but rather tends to increase its value again. This occurs when this capacitance is exposed to a substantially high field (voltage) and enhanced junction temperature (T_J), leading to the final decrease in the collector-emitter voltage rate of change (dV_{CE}/dt) during Phase 2.

5.5.3 IGBT Collector Current (I_C) Turn-Off Transient during Phase 2

The collector current (I_C) experiences a drop, due to the free-wheeling diode's junction capacitance (C_{JD}), which discharges during this phase. As discussed in Section 5.2.7, for a new IGBT, this drop is modelled linearly via Equation 5.42. Even though, this function effectively models the collector current (I_C) drop, when the IGBT is new, it does not remain suitable, as the implemented ageing strategy progresses, due to the introduced non-linearities. This is illustrated in Figure 5.50. The model function provided by Equation 5.42, indicates that the collector current rate of change ($dI_C/dt_{(PH2\_OFF)}$), is proportional to the diode's junction capacitance (C_{JD}), and the collector-emitter voltage rate of change ($dV_{CE}/dt_{(PH2\_OFF)}$). Since the free-wheeling diode (internal free-wheeling diode of IGBT) is kept the same throughout the different measurements and is not subjected to any accelerated ageing, than the diode's junction capacitance is considered to remain relatively constant and minimally influences any changes caused by the implemented accelerated ageing in the collector current (I_C) during Phase 2. On the other side, the collector-emitter voltage rate of change ($dV_{CE}/dt_{(PH2\_OFF)}$), is generally decreasing with each age iteration, as illustrated in Figure 5.42. This yields to a general decrease in the modelled turn-off Phase 2, piecewise linear collector current rate of change ($dI_C/dt_{(PH2\_OFF)}$) as indicated in Figure 5.50. One can notice that the piecewise linear model,

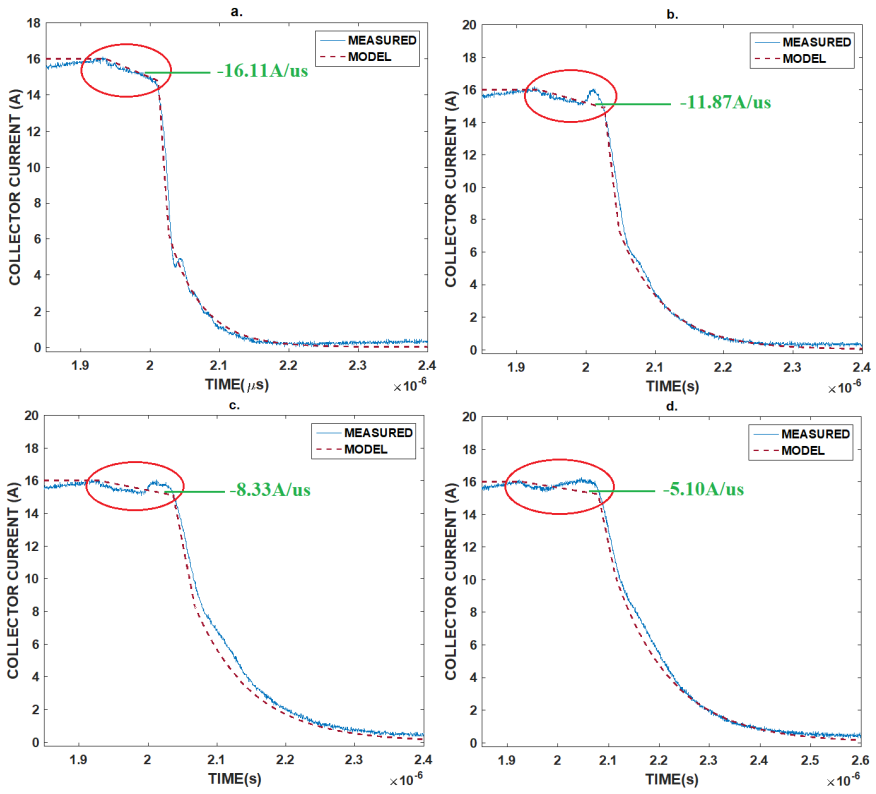


Figure 5.50 – Collector Current (I_C) turn-off transient Phase 2, IRG4BC30KD IGBT Sample 14, Linear Piecewise Model (a) New (b) Age Iteration A (c) Age Iteration B (d) Age Iteration C

is very limiting in representing the changes occurring due to the implemented ageing, in the collector current (I_C) transient during turn-off Phase 2. In the previous section it was already established, that the collector-emitter voltage (V_{CE}), after subjecting the IGBT to the implemented accelerated ageing, follows a non-linear relationship, modelled by the function

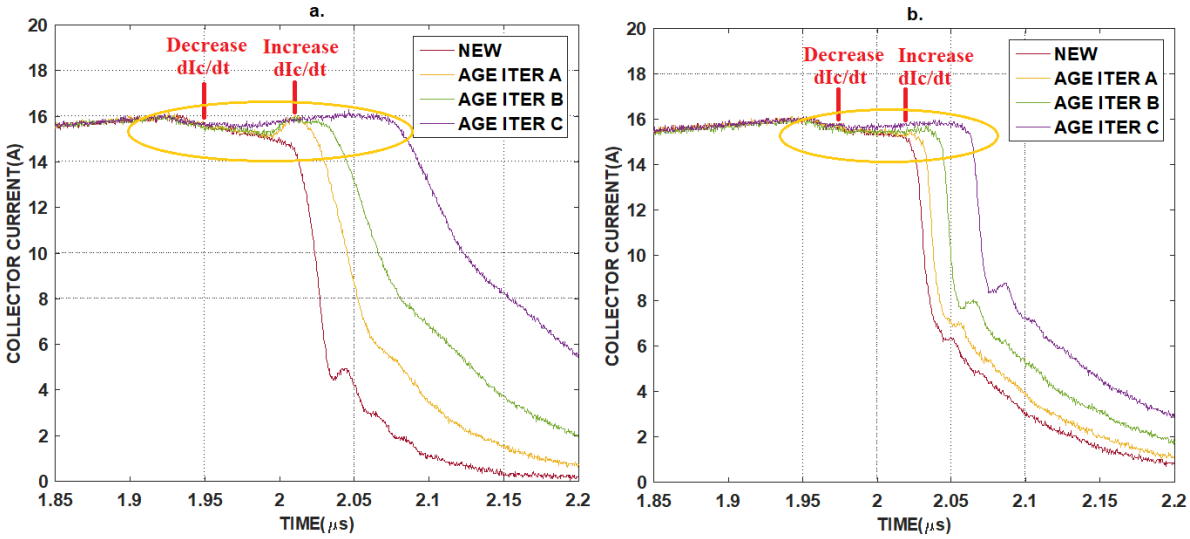


Figure 5.51 – Collector Current (I_C) turn-off transient Phase 2 (a) IRG4BC30KD IGBT Sample 14 (b) STGP19N60KD IGBT Sample 1

described by Equation 5.135. After ageing, the collector current (I_C) is manifesting a non-linear relationship too, characterized by an initial decrease and, followed by a consecutive increase experienced in approximately the second half of the turn-off Phase 2. As accelerated ageing progresses the initial decrease becomes shorter with a more noticeable consecutive increase. This effect is illustrated in Figure 5.51, for both the IRG4BC30KD IGBT Sample 14 and STGP19N60KD IGBT Sample 1.

Since the collector current (I_C) is dependent on the collector-emitter voltage rate of change ($dV_{CE}/dt_{(PH2\_OFF)}$), the non-linear changes experienced in the collector current (I_C) are a consequence of the non-linear changes occurring in the collector-emitter voltage rate of change ($dV_{CE}/dt_{(PH2\_OFF)}$). Figure 5.47 is providing a representation of the function provided by Equation 5.134 and the corresponding derivative. In this case the derivative is relevant, as the interest is in the collector-emitter voltage rate of change ($dV_{CE}/dt_{(PH2\_OFF)}$). The derivative of Equation 5.135 is characterized by an initial slow increase in the rate of change, followed by a rapid increase, until reaching the maximum rate of change occurring at the point of inflection. This is eventually followed by a rapid decrease in the rate of change, followed by a final slow decrease. In relation to the collector current (I_C), due to the initial increasing rate of change of the collector-emitter voltage ($dV_{CE}/dt_{(PH2\_OFF)}$), the freewheeling diode junction capacitance (C_{JD}) starts to discharge, hence a decreasing collector current (I_C) starts to manifest, but due to the eventual decrease in the rate of change of the collector-emitter voltage ($dV_{CE}/dt_{(PH2\_OFF)}$), the freewheeling diode junction capacitance (C_{JD}) starts to charge again manifesting as an increase in the collector current (I_C). Hence through the employment of the derivative of Equation 5.134, the model function for the collector current (I_C) transient during Phase 2, was obtained as described in Equation 5.138.

$$I_C(t) = I_{C0} + (-C_{JD})\frac{V_{DC}\phi_{2(OFF)}e^{-\phi_{2(OFF)}(t-t_{\lambda_{2(OFF)}})}}{(1+e^{-\phi_{2(OFF)}(t-t_{\lambda_{2(OFF)}})})^2} \tag{5.138}$$

Figure 5.52 depicts the overlayed collector current (I_C) model function over the measured transient for the IRG4BC30KD IGBT Sample 14. The same parameter values and approach, utilized through the model function of the collector-emitter voltage (V_{CE}) transient for the turn-off Phase 2, were utilized in the above model function.

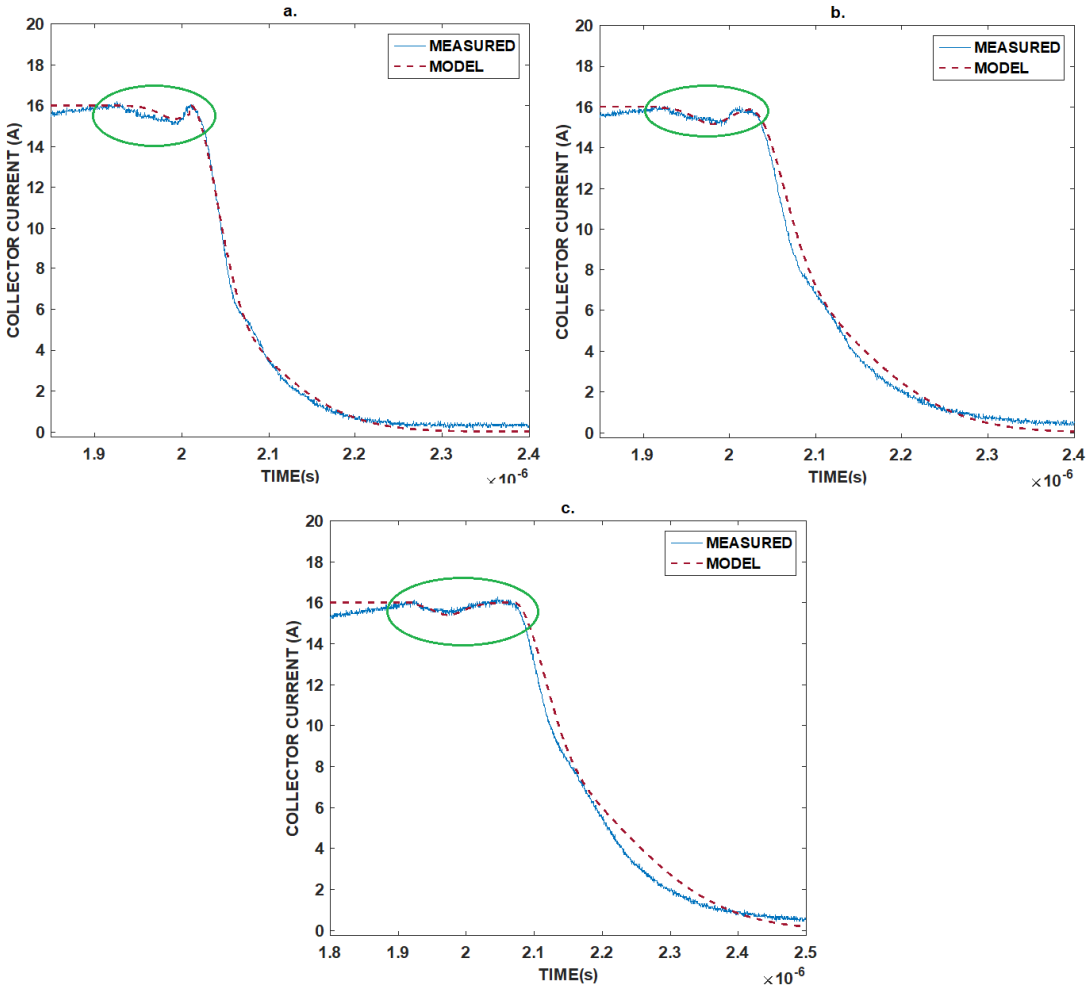


Figure 5.52 – Collector Current (I_C) turn-off transient, Phase 2, IRG4BC30KD IGBT Sample 14, Non-Linear Model (a) Age Iteration A (b) Age Iteration B (c) Age Iteration C.

The free-wheeling diode's junction capacitance (C_{JD}) was determined in Section 5.2.10 and quoted in Table 5-3. The only limitation is the parameter $t_{\lambda 2(OFF)}$, that is the location in time of the point of inflection, as for each age iteration the point of inflection of the collector-emitter voltage (V_{CE}) transient did not perfectly coincide with the collector current (I_C) transient. Thus, for this parameter, instead of utilizing the ones cited for the collector-emitter voltage (V_{CE}) transient modelling, these were measured from the collector current (I_C) transient at the point where the collector current (I_C) is at a minimum during turn-off Phase 2.

5.5.4 IGBT Collector Current (I_C) Turn-Off Transient during Phase 3 and Phase 4

Here the collector current (I_C) is typified by two transients. The first transient is characterized by a fast rate of change which is governed by the intrinsic IGBT MOSFET structure. According to Mohan [11], this phase is marginally affected by changes in the junction temperature (T_J). The second transient is the "tail current" governed by the IGBT BJT structure and is dependent

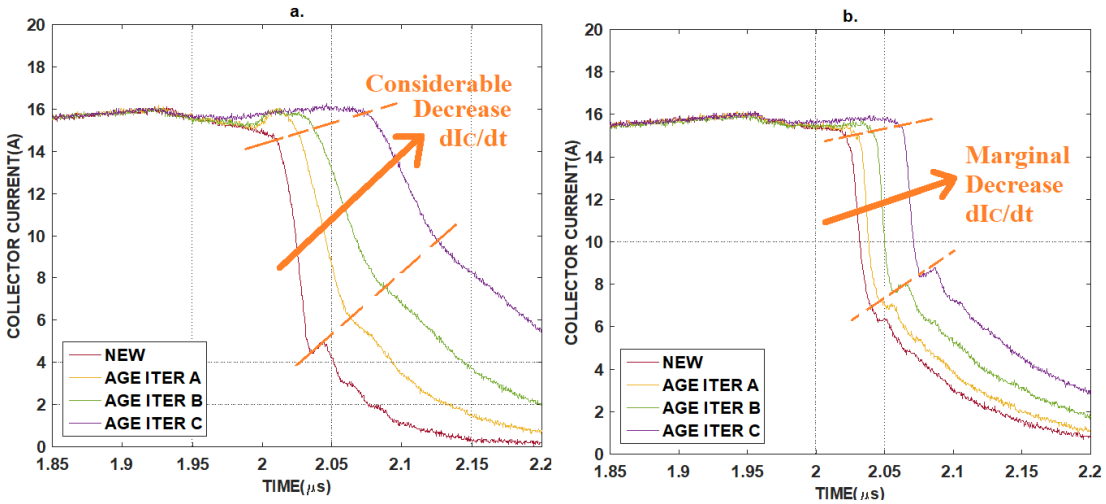


Figure 5.53 - Measured Phase 3 IGBT Intrinsic MOSFET controlled dI_C/dt Evolution with Ageing (a) IRG4BC30KD IGBT Sample 14 (b) STGP19N60KD IGBT Sample 1.

on the IGBT's junction temperature (T_J). In relation to the implemented accelerated ageing strategy, here, the collector current (I_C) manifested the following observations:

- During the fast collector current (I_C) decay, the International Rectifier IRG4BC30KD IGBT, experienced a progressive decrease in the collector current rate of change ($dI_C/dt_{PH3(OFF)}$) with each age iteration, as indicated in Figure 5.53(a) and in Table 5-16. On the other side, the ST Microelectronics STGP19N60KD IGBT, experienced a much less decrease in the collector current rate of change ($dI_C/dt_{PH3(OFF)}$), as indicated in Figure 5.53(b) and in Table 5-16. In fact, for the different age iterations, the STGP19N60KD IGBT, manifested collector current (I_C) transients which are almost parallel.

AGE ITERATION	IRG4BC30KD IGBT PHASE 3 INTRINSIC MOSFET dI_C/dt	STGP19N60KD IGBT PHASE 3 INTRINSIC MOSFET dI_C/dt
NEW	-472.58 A/μs	-940.12 A/μs
AGE ITERATION A	-262.40 A/μs	-880.23 A/μs
AGE ITERATION B	-200.00 A/μs	-848.77 A/μs
AGE ITERATION C	-143.32 A/μs	-834.27 A/μs

Table 5-16 - Measured Phase 3 IGBT Intrinsic MOSFET controlled dI_C/dt Evolution with Ageing (a) IRG4BC30KD IGBT Sample 14 (b) STGP19N60KD IGBT.

- For both IGBT models, the fast collector current (I_C) transient, remained relatively linear after accelerated ageing. Within the presented linear piecewise model, this transient was described by Equation 5.45. As evidenced in Table 5-15, the IRG4BC30KD IGBT, manifested changes in the forward transconductance (g_m) and

the threshold voltage (V_{TH}), with decreases, and increases respectively. Hence, for the linear piecewise model, to provide the best linear fit, reflecting the above parameters' changes, and the decreasing collector current rate of change ($dI_C/dt_{(PH3(OFF))}$), Equation 5.45 yields to an increase, in the input capacitance (C_{IES}). The stray inductance (L_{S1}) was decreased according to the indication in Figure 5.54. The reason for this will be explained later in Section 5.4.3, but it is necessary to ensure coherence with the measured transients during turn-on. At this point it is important to point out that the impact of the decreasing stray inductance (L_{S2}) value, as accelerated ageing progressed, still required the increase in the input capacitance (C_{IES}) to obtain the best linear fit. The gate resistance (R_G), low side gate drive voltage (V_{G-}) and the load test current ($I_L \equiv I_{C0}$) were kept constant as these were not varied during characterization. This is illustrated in Figure 5.54.

- As discussed in Chapter 4, the STGP19N60KD IGBT was subjected to the same accelerated ageing strategy. This IGBT too manifested changes in the forward transconductance (g_m) and the threshold voltage (V_{TH}), with decreases, and increases respectively as indicated in Table 5-17. On the other side this IGBT, did not manifest the same degree of change in these parameters, as the IRG4BC30KD IGBT. Having said that, employing the linear piecewise model Equation 5.45, with the above changes, yielded too to an increase in the input capacitance (C_{IES}). None the less, this IGBT, did not manifest the same degree of increase in this latter parameter, since the decrease in the rate of change of the collector current transient was less severe, when compared to the IRG4BC30KD IGBT.

• AGE • ITERATION	STGP19N60KD IGBT THRESHOLD VOLTAGE V_{TH} (V)	STGP19N60KD IGBT TRANSCONDUCTANCE g_m (S)
NEW	5.431	5.689
AGE ITERATION A	5.493	5.645
AGE ITERATION B	5.496	5.456
AGE ITERATION C	5.498	5.282

Table 5-17 – STGP19N60KD IGBT Sample 1 Threshold Voltage (V_{TH}) and Transconductance (g_m) evolution with ageing,

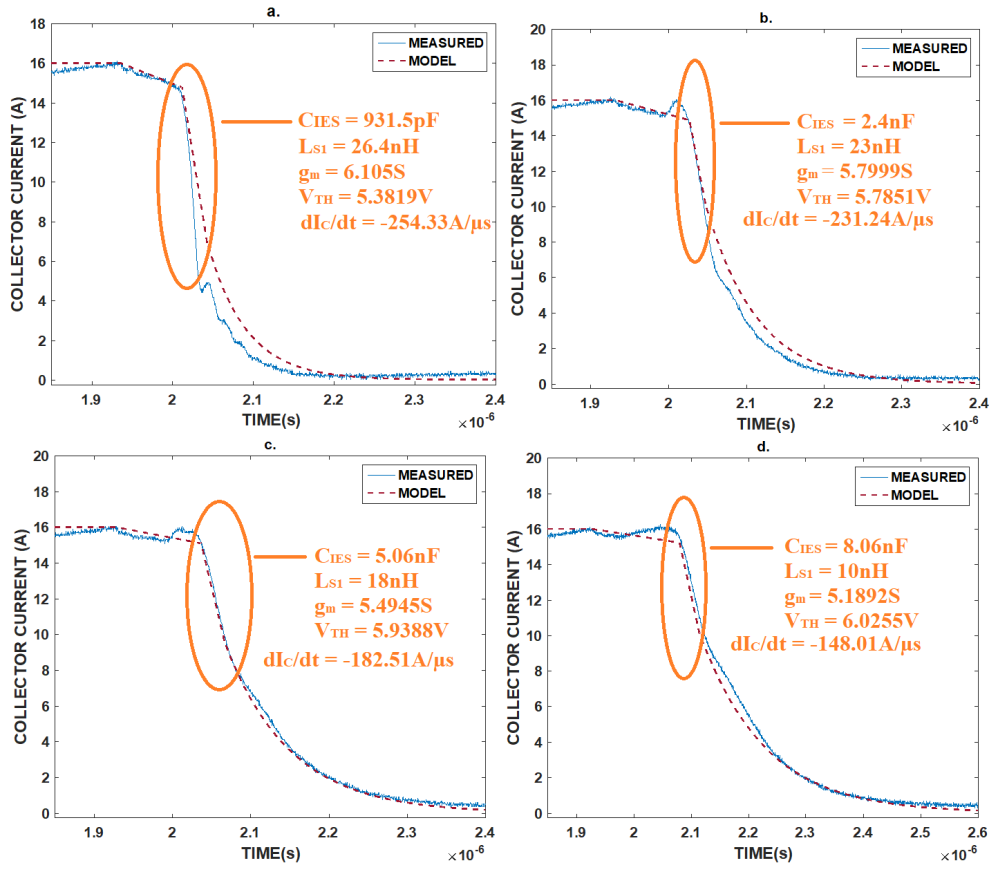


Figure 5.54 – IGBT Intrinsic MOSFET controlled Collector Current (I_C) turn-off transient Phase 3, IRG4BC30KD IGBT Sample 14, Linear Piecewise Model (a) New (b) Age Iteration A (c) Age Iteration B (d) Age Iteration C

- Theoretically, since the fast collector current (I_C) decay, which is controlled by the intrinsic MOSFET structure, is marginally affected by an increase in the junction temperature (T_J), then one can assume that the effect of the degraded die-attach and hence the consequential increase in the junction temperature (T_J) is minimally influencing the experienced changes due to the implemented accelerated ageing. Based on the previous observations, the hypothesis is that the input capacitance (C_{IES}) is being influenced by the implemented ageing strategy yielding to an increase in capacitance. The input capacitance (C_{IES}) is the combination of the gate-emitter capacitance (C_{GE}) and the Miller capacitance (C_{CG}). It has been already discussed how the Miller capacitance (C_{CG}) during turn-off is indicating an increase, influenced by enhanced junction temperature (T_J). This is contributing to the modelled global increase of the input capacitance (C_{IES}) and hence the effects of the junction temperature (T_J) cannot be completely ruled out. On the other side, the calculated increase in the Miller capacitance (C_{CG}) is of minimal contribution to

the modelled global increase of the input capacitance (C_{IES}), which indicates that if this hypothesis is to be considered, then this increase is mainly due to an enhanced gate-emitter capacitance (C_{GE}). In section 5.4.7, it was already established that the gate-emitter capacitance (C_{GE}) is a MOS structure capacitance and is predominantly due to the MOS structure overlap between the gate's polysilicon, the silicon-oxide, and the P^+ semiconductor (C_{P+}) and is provided by Equation 5.125. Hence, the capacitance (C) depends on the dielectric oxide's permittivity (ε_{OX}), the oxide's thickness (t_{OX}), and the overlap area (A). The likelihood of the implemented accelerated ageing affected the latter parameter is remote and is ignored in this analysis. Hence, possible explanations to the above observation are either that the dielectric material is progressively shrinking yielding to a decrease in the oxide's thickness (t_{OX}), or that the dielectric material is becoming more polarizable with the implemented accelerated ageing, leading to an increase in the dielectric's permittivity (ε_{OX}). Both scenarios contribute to a capacitance increase and both scenarios are related to the dielectric performance.

When an electric field is applied to a capacitor, since the insulative dielectric lacks free charges, the atomic negative charges orient themselves towards the positive conductive end, while the positive charges orient themselves towards the negative conductive end. Through this process, the dielectric is polarized, opposing the applied field, and hence drawing charge onto the capacitors conductive ends, with the result of storing energy in the capacitor. The easier the insulative material is to be polarized, the greater the amount of charge that can be stored, hence the bigger the capacitance. The capacitor's ability to store charge is essentially the degree of polarization (P) and is related to the absolute permittivity (ε_o), relative permittivity (ε_r), and electric field strength (E), through Equation 5.139 [225].

$$P = \varepsilon_o(\varepsilon_r - 1)E \tag{5.139}$$

Dielectric polarization is generally contributed by four charge displacement phenomena: electronic displacement (P_E), ionic displacement (P_I), permanent dipoles (P_D) and space charge displacement (P_S). Hence the total dielectric polarization (P_T) is provided by Equation 5.140 [225]:

$$P_T = P_E + P_I + P_D + P_S \tag{5.140}$$

- The electronic displacement polarization (P_E) manifests in all atoms when subjected to an electric field (E), where the nucleus and the corresponding cloud of electrons depart from each other.
- The ionic displacement polarization (P_I) manifests when the symmetrically aligned ions in a crystal lattice, which under no electric field has zero polarization, gets polarized when an electric field is applied, where the cations (positively charged ions, atoms that have an excess of protons than electrons) and anions (negatively charged ions, atoms that have an excess of electrons than protons) are attracted to opposite directions. This contributes to ionic displacement rather than charge displacement (electronic displacement), which contributes to the dielectric's enhanced relative permittivity (ε_r).
- Dipole Permanent Polarization (P_D) manifests in certain dielectric materials such as polymers, where these materials contain permanent molecular dipoles which occur when electrons in the same atom have different electronic charge value. Under the influence of an electric field, the dipoles rotate themselves in the direction of the field, causing an average dipole moment, which aids in the relative permittivity (ε_r) value of the dielectric.
- Space Charge (Interfacial) Polarization (P_S) happens from extraneous charges at the interface that can instill and contaminate the dielectric. Moreover, this phenomenon is abetted by possible irregular geometry in the dielectric crystalline structure and its evolution with extraneous influence. These latter phenomena have been already thoroughly discussed during Chapter 2. These implanted charges in the dielectric are partly mobile and hence can commute under an applied field, causing polarization, contributing to an increase in the relative permittivity (ε_r), and consequently an increase in capacitance (C) [225].

The first three dielectric polarization contributors are intrinsic to the material and are mainly governed by the dielectric material's characteristics. On the other side interfacial polarization happens due to extraneous circumstances.

Hence the modelled observed increase in the input capacitance (C_{IES}) and hence the gate-emitter capacitance (C_{GE}) is likely to be due to enhanced dielectric polarization of the interfacial type, contributing to an enhanced relative permittivity of the oxide layer (ε_r). This is triggered by the implemented accelerated ageing, which is causing dielectric contamination.

Unlike to other turn-off phases, there is a clear distinction between what happened during this phase, for the IRG4BC30KD IGBT transient and the STGP19N60KD IGBT transient, where the latter IGBT experienced less severe changes in the collector current rate of change ($dI_C/dt_{PH3(OFF)}$), modelled by an increase in the input capacitance (C_{IES}). When considering that the two IGBTs were subjected to relatively the same accelerated ageing methodology, the above observation can be attributed to a difference in the quality of the dielectric oxide of the two IGBTs, with the STGP19N60KD IGBT's oxide being of a better quality hence less prone to charge contamination and with less crystalline geometry defects, leading to a lesser increase of the input capacitance (C_{IES}). This is substantiated further by the lesser change in the threshold voltage (V_{TH}) experienced by the STGP19N60KD IGBT when compared to the IRG4BC30KD IGBT.

In relation to the "tail" collector current (I_C) transient, which is predominantly influenced by the intrinsic IGBT's BJT structure, resulted in a more prominent transient with an enhanced initial magnitude of "tail current" (I_{TAIL}) and corresponding duration, for both IGBT models as illustrated in Figure 5.55. It has been already discussed that this transient is heavily influenced by the junction temperature (T_J), and hence the observed changes due to the implemented ageing procedure concurs with the observations monitored in the die attach. Since the die attach is experiencing enhanced voiding, then this means that the IGBT has less ability to dissipate heat. Even though during measurements the case temperature (T_C), was maintained at 25°C and the utilisation of short pulse durations, the enhanced "tail" current is indicating that the die-attach degradation is keeping the junction temperature (T_J) at a higher temperature.

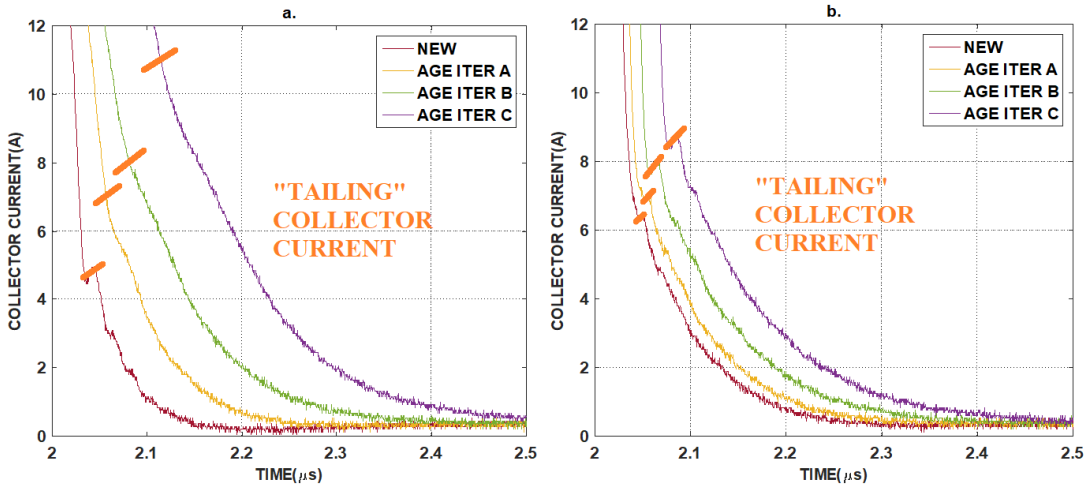


Figure 5.55 - Measured Phase 4 IGBT Intrinsic BJT "Tailing" Current Evolution with Ageing (a) IRG4BC30KD IGBT Sample 14 (b) STGP19N60KD IGBT Sample 1.

In the implementation of the non-linear IGBT transients' model, the turn-off Phase 3 and Phase 4, were combined into a single model function provided by Equation 5.104. The same equation was utilized to model the non-linear collector current (I_C) transient during Phase 3 and Phase 4, while varying the different function parameters to reflect the measured changes due to the implemented accelerated ageing strategy. Table 5-18 provides the evolution of the different parameters with ageing. This shows that the IGBT's intrinsic BJT controlled collector current (I_C) transient, becomes more predominant than the IGBT intrinsic MOSFET controlled collector current (I_C) transient, as illustrated in Figure 5.56.

PARAMETER	NEW	AGE ITERR. A	AGE ITERR. B	AGE ITERR. C
$t_{2(OFF)}$	2.010µs	2.011µs	2.026µs	2.070µs
t_{itail}	57ns	110ns	133ns	191ns
t_f	78ns	137ns	189ns	239ns
$\alpha_{3(OFF)}$	$1.642x10^{15}s^{-1}$	$5.673x10^{14}s^{-1}$	$3.856x10^{14}s^{-1}$	$2.688\ x10^{14}s^{-1}$
$\alpha_{4(OFF)}$	$1.881x10^{14}s^{-1}$	$5.798x10^{13}s^{-1}$	$3.741x10^{13}s^{-1}$	$2.149x10^{13}s^{-1}$
$k_{(TAIL)}$	0.3082	0.3438	0.4835	0.5313
I_{TAIL}	4.5A	5.5A	7.6A	8.5A
I_{MOS}	11.1A	10.5A	8.2A	7.5A

Table 5-18 - IGBT Sample 14 Turn-Off Phase 3 and Phase 4 collector current non-linear transient model parameters evolution with ageing.

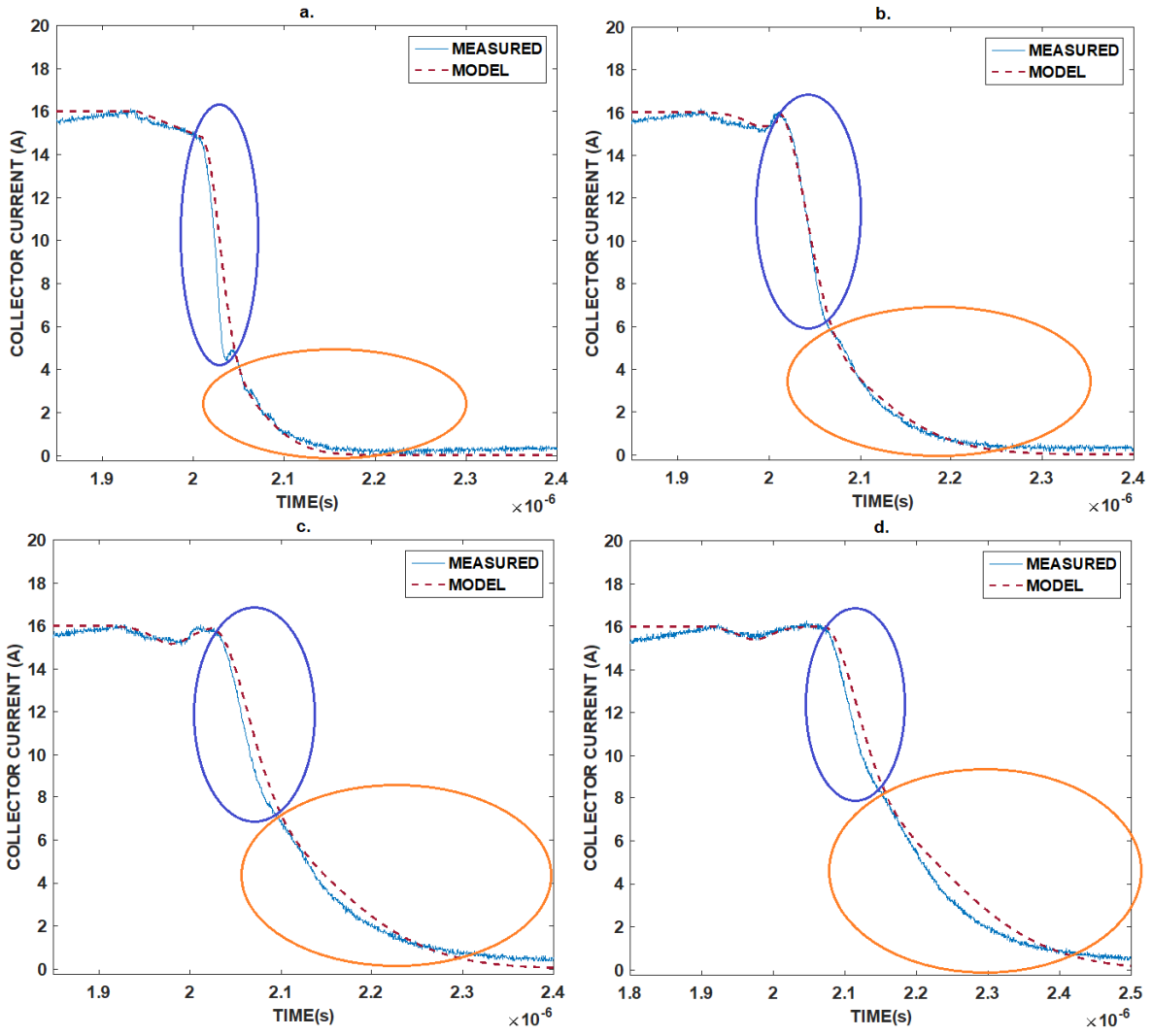


Figure 5.56 - IGBT Collector Current (IC) turn-off transient Phase 3 and Phase 4, IRG4BC30KD IGBT Sample 14, Non-Linear Model (a) New (b) Age Iteration A (c) Age Iteration B (d) Age Iteration C

5.5.5 IGBT Collector-Emitter Voltage (V_{CE}) Turn-Off Transient Phase 3 & 4

The collector-emitter voltage (V_{CE}) during the turn-off Phase 3 and Phase 4, manifested an overshoot due to the fast decay of the collector current (I_C), controlled by the IGBT's intrinsic MOSFET structure, through the stray inductance (L_{P1}). The following changes were observed as the IGBT progressed through the implemented accelerated ageing:

- The IRG4BC30KD IGBT, manifested a decrease in the overshoot peak voltage, as ageing progressed. This is due to a decrease in the collector current rate of change during turn-off Phase 3 ($dI_C/dt_{PH3(OFF)}$), as depicted in Figure 5.53. Even though the STGP19N60KD IGBT too, manifested a decrease in the peak overshoot voltage, the extent was less, when compared to the IRG4BC30KD IGBT. This is since the

STGP19N60KD IGBT manifested a lesser decrease in the collector current rate of change (dI_C/dt), when compared to the changes experienced by the IRG4BC30KD IGBT. This is evidenced in Figure 5.53.

- The IRG4BC30KD IGBT, manifested less ringing in the collector-emitter voltage (V_{CE}) transient, ending up in a nearly damped transient as ageing progressed. This again is directly related to a decrease in the collector current rate of change during turn-off Phase 3, ($dI_C/dt_{PH3(OFF)}$). The same observation was noted in STGP19N60KD IGBT collector-emitter voltage (V_{CE}) transient, even though the decrease in ringing was of a lesser extent when compared to the IRG4BC30KD IGBT. For the tested STGP19N60KD IGBTs, critical damping was never achieved after three age iterations as observed in the IRG4BC30KD IGBT. This is illustrated in Figure 5.57.

Figure 5.58 depicts the collector-emitter voltage (V_{CE}) transient, turn-off Phase 3 and Phase 4, linear piecewise model implementation, based on the model function described by Equation 5.47, which is dependent on the collector-current rate of change during turn-off Phase 3, ($dI_C/dt_{PH3(OFF)}$). Evidently, the linear piecewise model is very limited to model effectively the collector-emitter transient changes, especially in the final ageing stages.

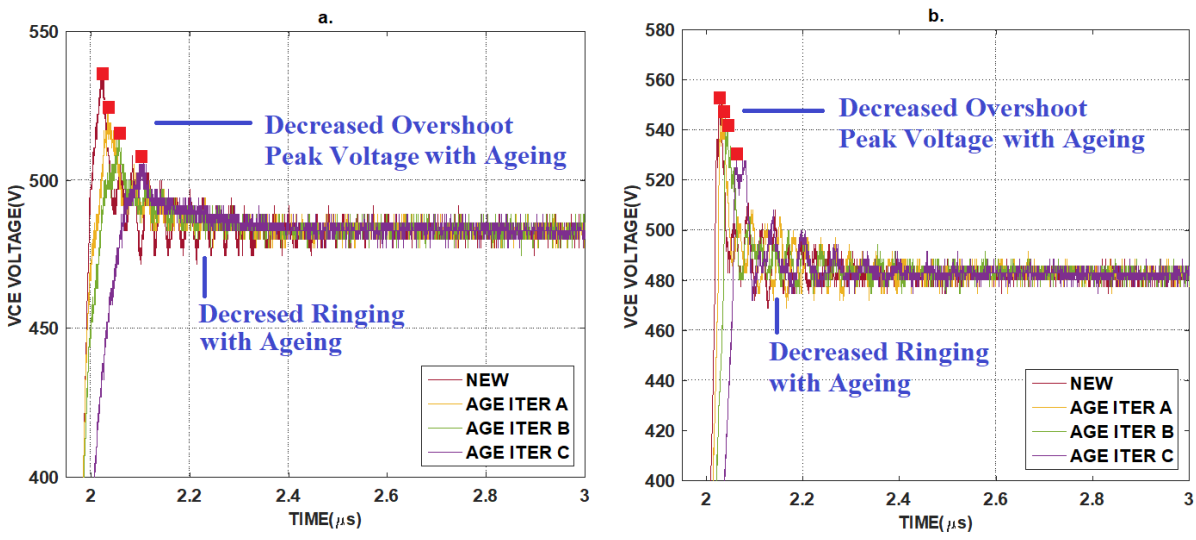


Figure 5.57 - Measured Phase 3 and Phase 4 IGBT Collector-Emitter Evolution with Ageing (a) IRG4BC30KD IGBT Sample 14 (b) STGP19N60KD IGBT Sample 1.

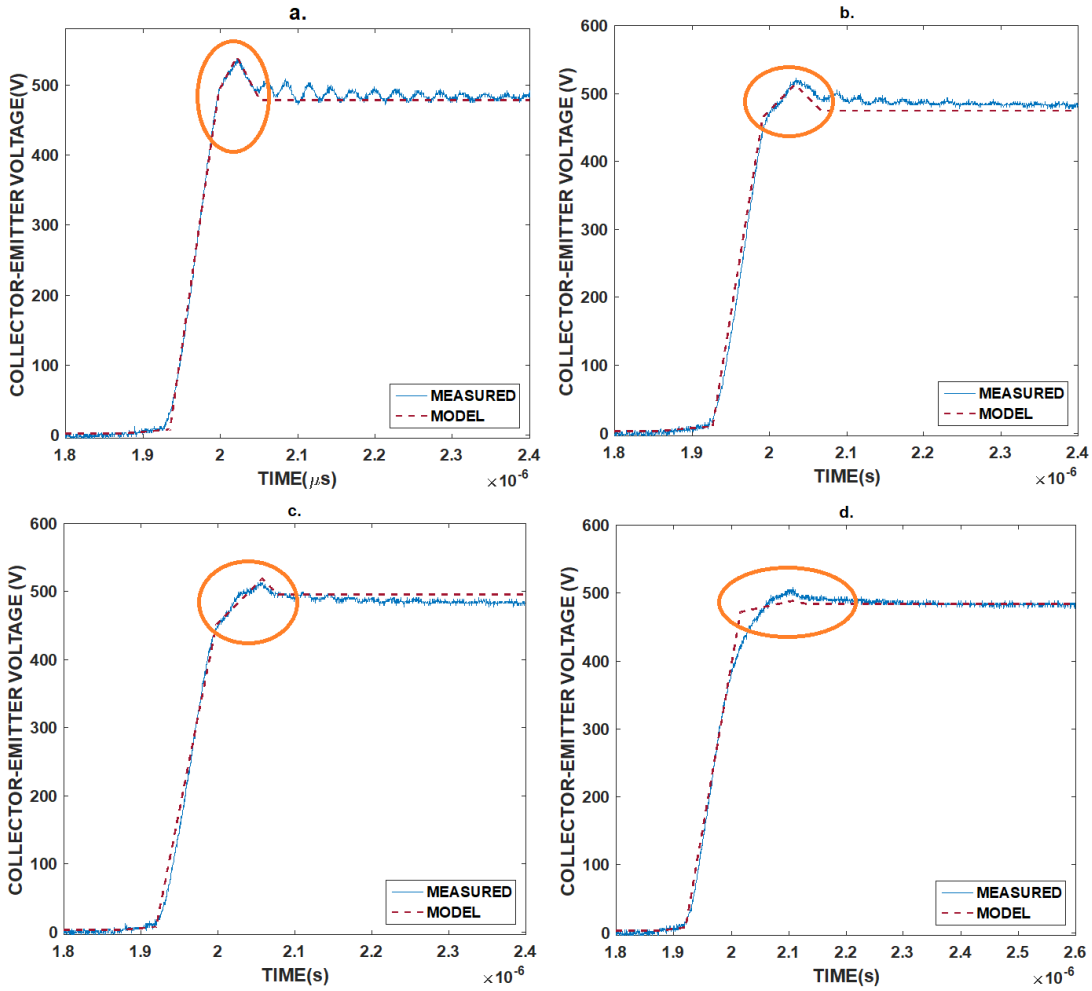


Figure 5.58 - IGBT Collector-Emitter Voltage (V_{CE}) turn-off transient Phase 3 & 4, IRG4BC30KD IGBT Sample 14, Linear Piecewise Model (a) New (b) Age Iteration A (c) Age Iteration B (d) Age Iteration C

Figure 5.59 depicts the collector-emitter voltage (V_{CE}) transient, turn-off Phase 3 and Phase 4, non-linear model implementation, based on the model function described by Equation 5.107. This same function was utilized to model these phases' consecutive age iterations. Since this function is dependent on the parameters tabulated in Table 5-18, since it is predominantly dependent on the collector current (I_C) during the turn-off Phase 3 and Phase 4, then the corresponding parameters changes due to the implemented accelerated ageing listed in Table 5-18, apply for the function changes here. The model values of the stray inductance (L_{P1}), and the output off-state collector-emitter voltage ($V_{DC} \equiv V_{CE0}$), were maintained constant throughout the different model age iterations. Furthermore, the ringing was not modelled in the presented model equation.

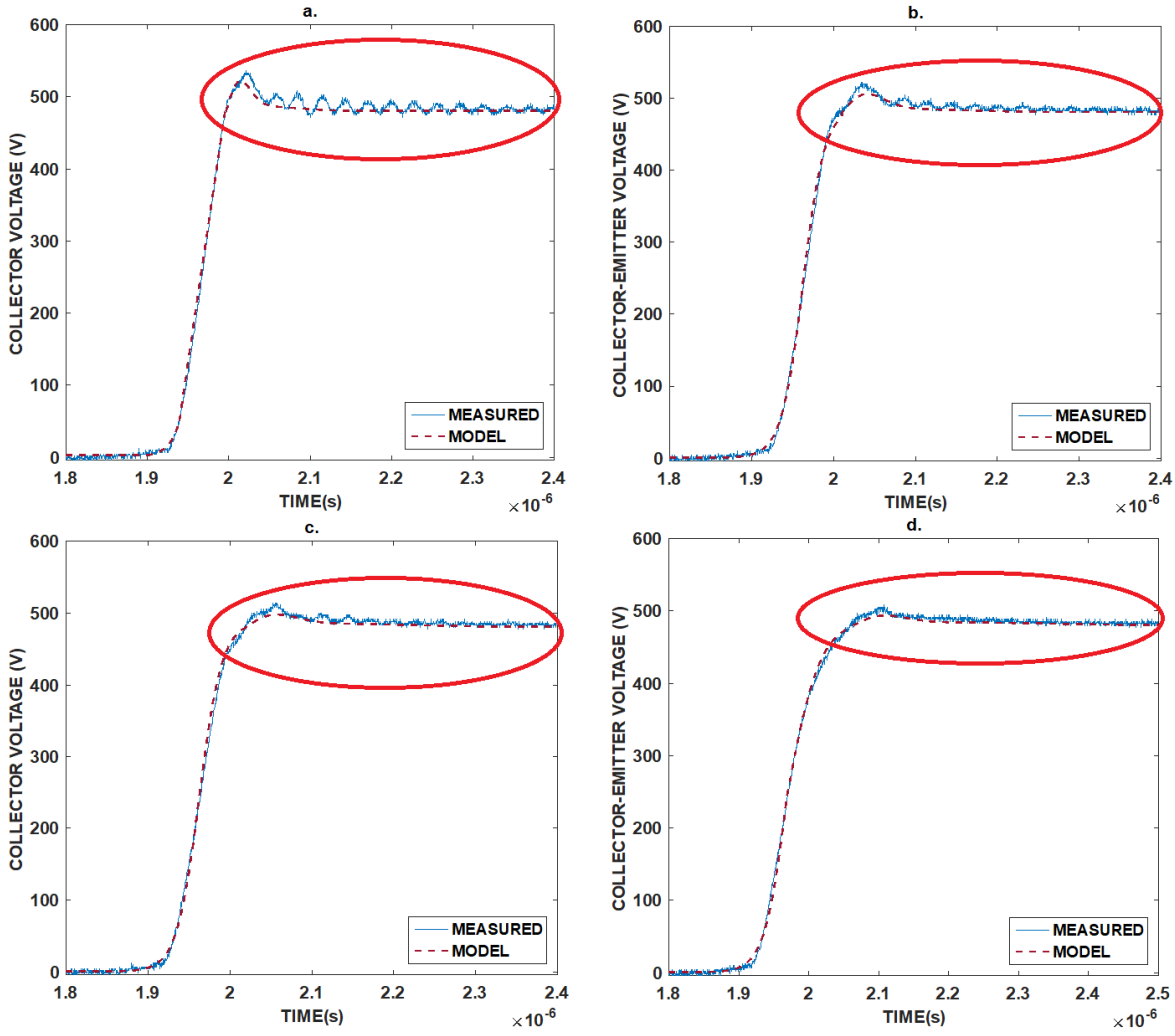


Figure 5.59 - IGBT Collector-Emitter Voltage (V_{CE}) turn-off transient Phase 3 and Phase 4, IRG4BC30KD IGBT Sample 14, Non-Linear Model (a) New (b) Age Iteration A (c) Age Iteration B (d) Age Iteration C

5.5.6 IGBT Turn-Off Energy Loss

Since both the IGBT turn-off transients, have experienced a considerable slow-down with the implemented accelerated ageing, it is expected that the switching power loss and hence the energy loss during the IGBT turn-off, experiences an increase. Figure 5.60 illustrates the resulting measured and modelled turn-off switching power pulse, for each age iteration, for the IRG4BC30KD IGBT Sample 14. Table 5-19 provides the corresponding calculated values of the measured and modelled energy loss for the IRG4BC30KD IGBT Sample 14. These were obtained by integrating the area under the power pulse for both the measured and modelled plots. This shows the congruence of the measured transient and modelled turn-off power loss transients and the corresponding computed turn-off energy loss, highlighting the expected increase in the turn-off switching power dissipation and hence energy loss.

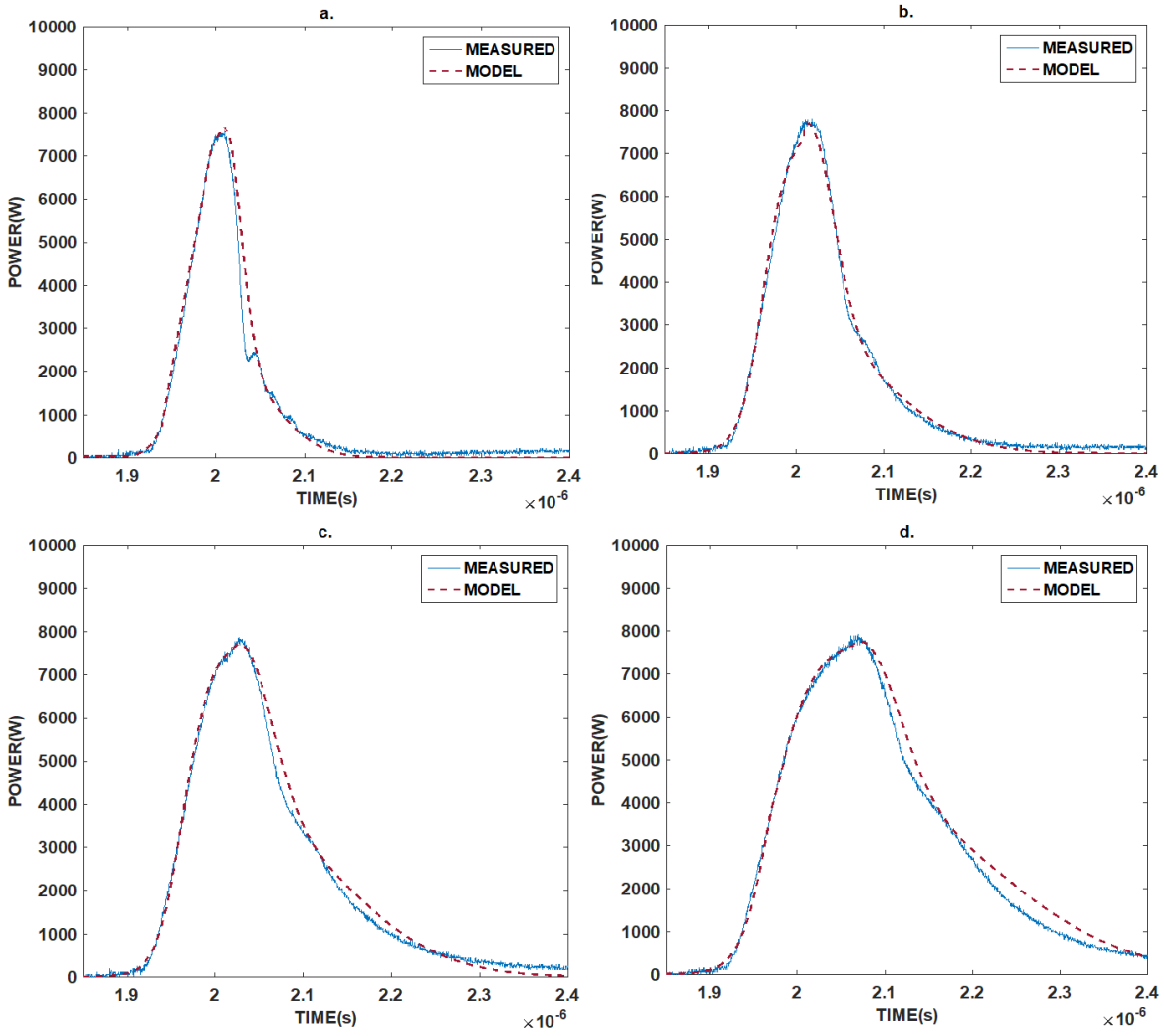


Figure 5.60 - IGBT Turn-Off Switching Power Loss, Measured and Non-Linear Model (a) New (b) Age Iteration A (c) Age Iteration B (d) Age Iteration C

PARAMETER	NEW	AGE ITERR. A	AGE ITERR. B	AGE ITERR. C
Measured Turn-Off Switching Energy Loss (mJ)	0.5581	0.8253	1.1148	1.5919
Modelled Turn-Off Switching Energy Loss (mJ)	0.5893	0.8401	1.1680	1.6320

Table 5-19 - IGBT IRG4BC30KD Sample 14 Turn-Off Switching Energy Loss, Measured and Non-Linear Model (a) New (b) Age Iteration A (c) Age Iteration B (d) Age Iteration

5.5.7 IGBT Turn-On Transients Evolution with Accelerated Ageing

In relation to the turn-on transient, tested IGBTs manifested marginal changes, when subjected to the accelerated ageing procedure described in Chapter 3. This is discussed in Section 4.5.2 and illustrated in Figure 4.18 for the IRG4BC30KD IGBT, and in Section 4.6.2 and illustrated in Figure 4.33 for the STGP19N60KD IGBT. The minimal changes observed in the turn-on is attributed to the following reasons.

1. The IGBT's collector current (I_C) turn-on transient, is predominantly influenced by the reverse recovery effect. As described earlier, the internal IGBT diode, utilized as the free-wheeling diode (S_1 reference Figure 4.1) was not subjected to accelerated ageing. Hence the turn-on phases governed by the reverse-recovery effect will remain unchanged, subject that the collector-current rate-of change during the turn-on Phase 2, ($dI_C/dt_{PH2(ON)}$), remains unchanged as indicated in Equations 5.12 and 5.13. As indicated earlier and in Table 5-20, this parameter remained relatively unchanged after subjecting the IGBT to the implemented accelerated ageing.

2. The second reason yields from the relatively unchanged collector-current rate of change during turn-on Phase 2, ($dI_C/dt_{PH2(ON)}$). This latter observation is attributed to the fact, that the turn-on collector current (I_C) transient, is predominantly controlled by the intrinsic MOSFET structure. This is unlike the turn-off collector current (I_C) transient, which is governed by both the IGBT's intrinsic MOSFET and BJT structures. As stated in [11], the MOSFET structure is marginally influenced by the junction temperature (T_J). This implies that the observed degradation of the die-attach is scantily influencing the turn-on collector current (I_C) transient.

3. In relation to the linear piecewise modelling, the collector-current rate of change during turn-on Phase 2, ($dI_C/dt_{PH2(ON)}$) is described by Equation 5.5. As the implemented accelerated ageing progressed, this phase remained relatively unchanged and linear. It has been already mentioned that the IRG4BC30KD IGBTs manifested changes in the forward transconductance (g_m) and the threshold voltage (V_{TH}), with decreases, and increases respectively. In Section 5.5.4, it was argued that for the above changes, the input capacitance (C_{IES}) had to increase, to model the observed decrease in the turn-off collector current rate of change during Phase 3, ($dI_C/dt_{PH3(OFF)}$), even when considering modelled changes in the stray inductance (L_{S1}), as indicated in Figure 5.54. Hence since Equation 5.5, is dependent on the input capacitance (C_{IES}), the modelled changes in this parameter, will impact the modelled collector-current rate of change during turn-on Phase 2, ($dI_C/dt_{PH2(ON)}$). For this latter parameter to remain relatively unchanged, as observed during measurement, the stray inductance (L_{S1}), was modelled to decrease with each age iteration to compensate for the input capacitance (C_{IES}) increase. The same decrease in the stray inductance (L_{S1}), was already included in the model function of the turn-off collector current rate of change during Phase 3, ($dI_C/dt_{PH3(OFF)}$), as

explained in Section 5.5.4 and indicated in Figure 5.54. Figure 5.61 depicts the turn-on linear piecewise model evolution with the implemented accelerated ageing of the collector current (I_C) during Phase 2. Table 5-20 provides the measured and modelled collector-current rate of change during turn-on Phase 2, ($dI_C/dt_{PH2(ON)}$). As explained earlier, the stray inductance (L_{S1}), was modelled as the summation of the gate drive circuit output inductance (L_{DRV}), the intrinsic IGBT's gate inductance (L_G), and the intrinsic IGBT's emitter inductance (L_E). The gate drive circuit output inductance (L_{DRV}) can be assumed to be unchanged. On the other side it is understandable that the IGBT's parasitic inductances suffered changes due to the implemented accelerated ageing procedure. Specifically, the intrinsic emitter inductance (L_E), which is common to the output collector circuit, as well as the gate drive circuit.

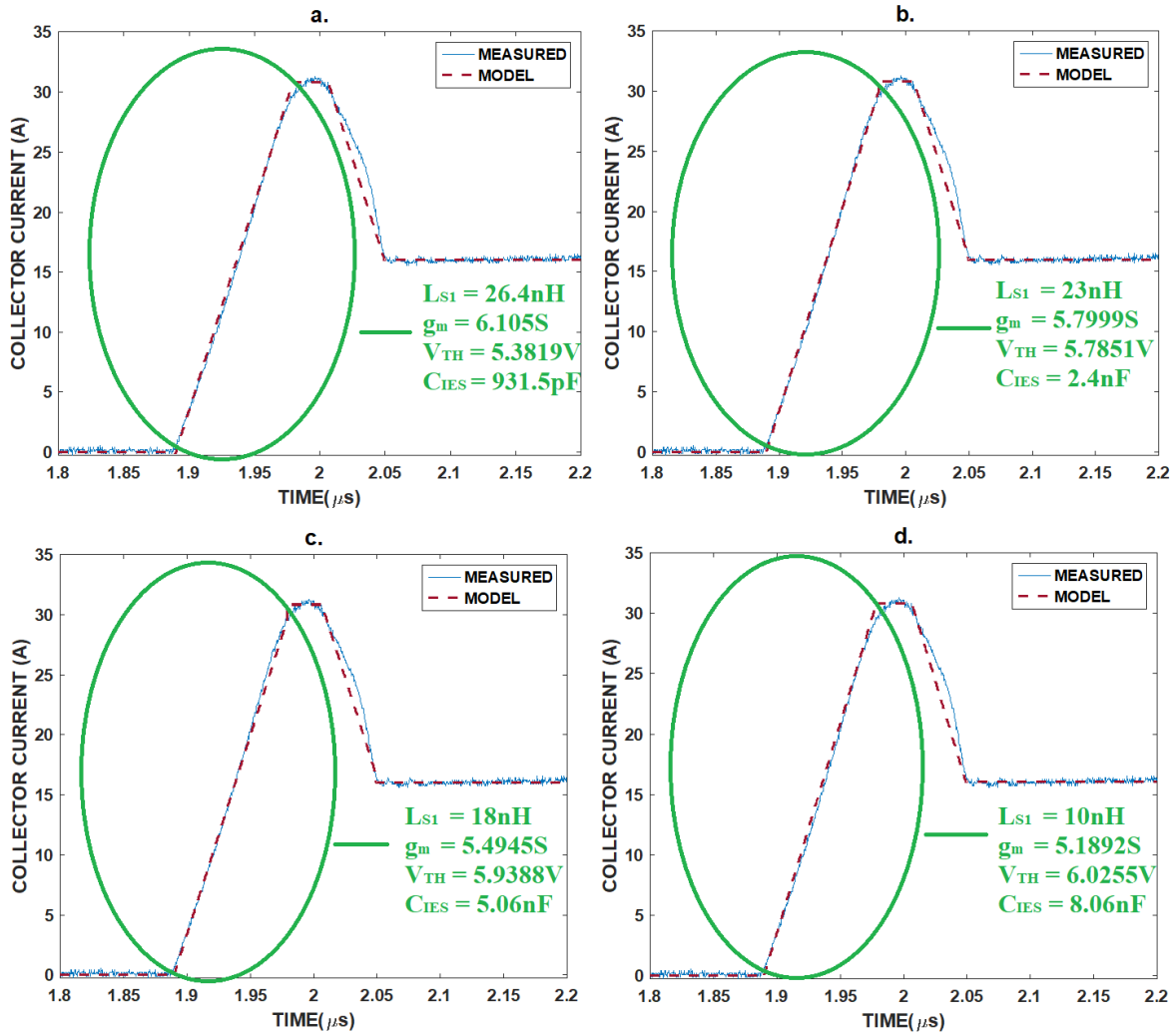


Figure 5.61 - IGBT Collector Current (I_C) turn-on transient Phase 2, IRG4BC30KD IGBT Sample 14, Linear Piecewise Model (a) New (b) Age Iteration A (c) Age Iteration B (d) Age Iteration C

AGE ITERATION	TURN-ON PHASE 2 dI_C/dt MEASURED (A/µs)	TURN-ON PHASE 2 dI_C/dt MODELLED (A/µs)
NEW	318.42	344.04
AGE ITERATION A	337.67	337.65
AGE ITERATION B	336.00	319.08
AGE ITERATION C	336.00	347.28

Table 5-20 - IGBT Collector Current Rate of Change (dI_C/dt) turn-on transient Phase 2, IRG4BC30KD IGBT Sample 14, Measured vs Linear Piecewise Model

4. This inductance establishes feedback from the collector circuit to the gate circuit and hence the voltage developed across this inductance subtracts from the applied gate voltage during turn-on transient and sums it during the turn-off, hence slowing down the switching of the IGBT. This is like the Miller effect, with the basic difference that this effect is proportional to the current rate of change (dI/dt), rather than the voltage rate of change (dV/dt), where the larger the inductance, the larger the voltage across the inductance, the slower the IGBT's transient. Since during the turn-off collector current rate of change during Phase 3, ($dI_C/dt_{PH3(OFF)}$), the input capacitance (C_{IES}) was modelled to increase, as age progressed, reflecting the experienced decrease in the collector-current rate of change ($dI_C/dt_{PH3(OFF)}$), here this input capacitance (C_{IES}) increase was compensated by the stray inductance (L_{S1}) decrease, hence cancelling the slow down caused by the larger input capacitance (C_{IES}) and hence retaining a relatively unchanged turn-on collector current (I_C). From a modelling point of view this compensation ensures that the collector-current rate of change during turn-on Phase 2, ($dI_C/dt_{PH2(ON)}$), remains relatively unchanged, but the translation to the physical explanation of the above has not been fully understood, apart from the justifications provided earlier.

5. In relation to the turn-on collector-emitter voltage (V_{CE}) transient, Phase 2 and Phase 3 are governed by the corresponding decay in collector-emitter voltage (V_{CE}) due to the collector current rate of change during Phase 2 ($dI_C/dt_{PH2(ON)}$), through the primary stray inductance (L_P) as described by the linear piecewise model Equation 5.47. The primary stray inductance (L_P) was retained as constant in relation to the different accelerated ageing iterations. This was motivated by the fact that this inductance is primarily influenced by the Double Pulse Test circuit and board parasitic inductances, which were

not influenced by the implemented accelerated procedure, and hence any intrinsic IGBT parasitic inductance change, was considered negligible, in relation to the global value of the primary stray inductance (L_P). Moreover, the rate of change of the collector current during Phase 2, remained relatively unchanged. This leads to an unchanged turn-on collector-emitter voltage transient during Phase 2 ($dV_{CE}/dt_{PH2(ON)}$), and Phase 3 ($dV_{CE}/dt_{PH3(ON)}$). This is illustrated in Figure 5.62.

6. The turn-on collector-emitter voltage (V_{CE}) transient during Phase 4, is characterized by a fast linear fall. As discussed earlier, this fall depends on the voltage rate of change across the collector-gate Miller capacitance (dV_{CCG}/dt), since during this phase, the gate-emitter voltage (V_{GE}) is at the Miller plateau. The current flowing through this capacitor is contributed by the gate current (I_G), and by the reverse–recovery current of the free-wheeling diode, through the gate-emitter capacitor (C_{GE}), as described in Section 5.2.4.

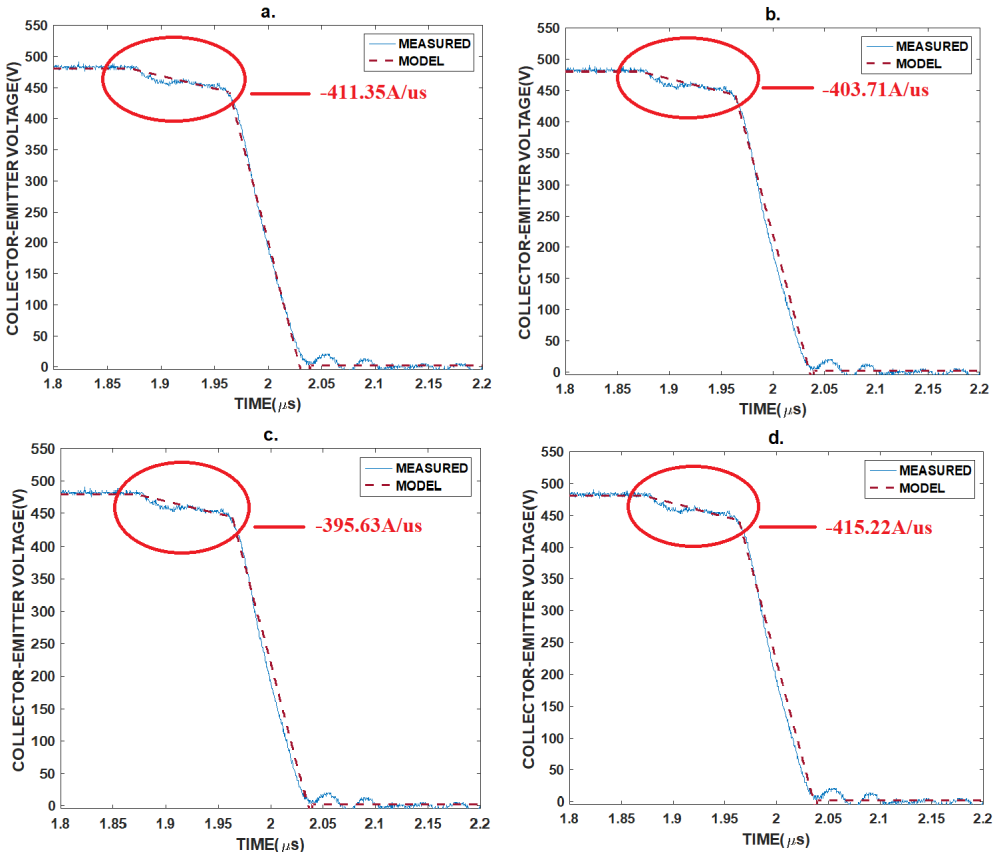


Figure 5.62 - IGBT Collector-Emitter Voltage (V_{CE}) turn-on transient Phase 2 & 3, IRG4BC30KD IGBT Sample 14, Linear Piecewise Model (a) New (b) Age Iteration A (c) Age Iteration B (d) Age Iteration C

The above collector-emitter voltage was described within the IGBT linear piecewise model by Equation 5.35. This equation is dependent on changing parameters due to the implemented accelerated ageing, namely, increase in the threshold voltage (V_{TH}), decrease in the transconductance (g_m), and an increase in the gate-emitter capacitance (C_{GE}). This latter parameter is a predominant part of the input capacitance (C_{IES}), where its value had to change to cater for the decrease in the turn-off collector current rate of change during Phase 3, ($dI_C/dt_{PH3(OFF)}$). When inputted into the model equation, the above changes tended to level out, hence not producing significant change in the collector-emitter voltage rate of change during turn-on Phase 4 ($dV_{CE}/dt_{PH4(ON)}$), It is important to point out that the remaining model parameters such as the high-side gate drive voltage (V_{G+}), and the gate resistance (R_G) were retained constant, since these are dictated by the Double Pulse test procedure and hence not altered by accelerated ageing. The collector current rate of change during Phase 2 ($dI_C/dt_{PH2(ON)}$), was obtained from the piecewise linear model described earlier, obtaining marginal changes due to ageing, as described in Table 5-20. Having said that the salient parameter which is predominantly dictating the collector-emitter voltage rate of change during turn-on Phase 4 ($dV_{CE}/dt_{PH4(ON)}$), is the Miller capacitance (C_{CG}). It has been already established in Section 6.4.2, that the overall modelled equivalent high-voltage collector-gate capacitance (C_{CG2}) is increasing, to cater for the decrease in the collector-emitter voltage rate of change during turn-off Phase 2 (dV_{CE}/dt), eventually explaining that this was related to the overall elongation of the Miller plateau during turn-off, which was triggered by an increase in the junction temperature (T_J), caused by the experienced degradation in the die-attach. On the other side for the turn-on collector-emitter voltage (V_{CE}) transient during Phase 4, to remain relatively unchanged with accelerated ageing, as observed from measurements, it implies that the collector-gate capacitance (C_{CG}) value, must be modelled as constant. It has been already explained that the collector-gate Miller capacitance (C_{CG}) MOS structure consists of the series combination of the oxide capacitance (C_{OX}) and the semiconductor depletion capacitance (C_{Si}). During turn-on, this latter capacitance will not be present since there is no formation of the depletion region and hence the collector-gate Miller capacitance (C_{CG}) will be only due to the oxide capacitance (C_{OX}) and hence independent of changes in the collector-emitter voltage (V_{CE}) which affect the width of the depletion region. Moreover, this latter capacitance and hence the turn-on collector-gate Miller capacitance (C_{CG}), is marginally affected by changes in the junction temperature (T_J), due to the omission of

the semiconductor depletion capacitance (C_{Si}) which during turn-off was experiencing an increase in the N^- drift region charge carrier density (N_B) due to enhanced junction temperature (T_J). The oxide capacitance (C_{OX}) is influenced by changes in the oxide's dielectric. It is important to point out that the oxide capacitance (C_{OX}) here is different from the oxide capacitance contributing to gate-emitter capacitance (C_{GE}), which was modelled as increasing during the turn-off transient. As indicated in Figure 5.38, the oxide capacitance contributing to the gate-emitter capacitance (C_{GE}), consists predominantly of the overlaying structure of the gate's polysilicon, the dielectric oxide, and the heavily doped P^+ region shorted with the N^+ region via the emitter metallization. These latter characteristics contributed to a faster formation of the inversion layer. In the case of the oxide capacitance (C_{OX}), contributing to the collector-gate Miller capacitance (C_{CG}), it consists of the gate's polysilicon, the dielectric oxide, and the lightly doped N^- drift region, which moreover during turn-on it is initially carrying no collector current and hence the N^- drift region surface, close to the silicon-silicon dioxide interface (Si-SiO_2) has a low-density of charge carriers. Hence the dependence of the collector-gate Miller capacitance on the collector-current (I_C) proposed by Tan. et al. [224], becomes immaterial during turn-on. The above yields to the oxide capacitance (C_{OX}) which is contributing to the collector-gate Miller capacitance (C_{CG}) to be less affected by dielectric's polarization, when compared to the oxide capacitance contributing to the gate-emitter capacitance (C_{GE}) and hence the input capacitance (C_{IES}). The above analysis leads to a more reliable and constant turn-on collector-gate Miller capacitance in relation to the implemented accelerated ageing, leading to a relatively unchanged turn-on Miller plateau and gate voltage (V_G) transient. This contributed to a practically unchanged turn-on collector-emitter voltage rate of change during Phase 4 ($dV_{CE}/dt_{PH4(ON)}$) as provided in Table 5-21 and depicted in Figure 5.64, where the collector-gate (C_{CG}) Miller capacitance, was modelled as relatively constant.

In relation to the IGBT turn-on transient non-linear modelling, it is important to point out that the same functions, parameters, and corresponding parameter values were retained, as described in Section 5.3 and Table 5-12 respectively, as computed for a new IGBT. Figures 5.65 and 5.66 illustrate the implemented turn-on non-linear model for the collector current (I_C) transient and collector-emitter voltage (V_{CE}) transient respectively.

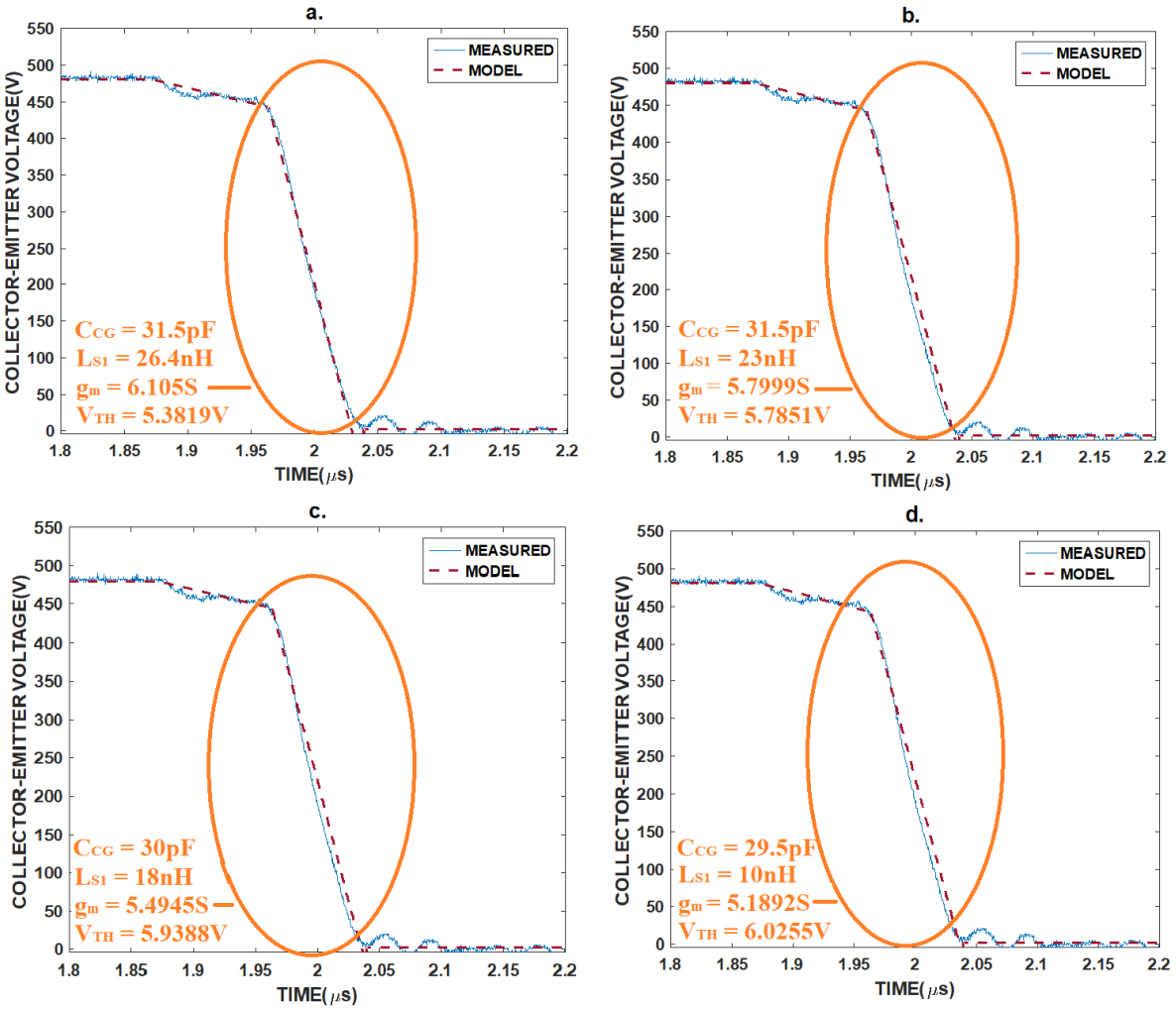


Figure 5.63 - IGBT Collector-Emitter Voltage (V_{CE}) turn-on transient Phase 4, IRG4BC30KD IGBT Sample 14, Linear Piecewise Model (a) New (b) Age Iteration A (c) Age Iteration B (d) Age Iteration C

Essentially the implemented non-linear model transients were left unchanged, while still obtaining satisfactory congruence to the measured transient, confirming what has been stated earlier that the turn-on transients were marginally affected by the implemented accelerated ageing.

AGE ITERATION	TURN-ON PHASE 4 dV_{CE}/dt MEASURED (V/µs)	TURN-ON PHASE 4 dV_{CE}/dt MODELLED (V/µs)
NEW	-7041.49	-6690.90
AGE ITERATION A	-6907.30	-6173.50
AGE ITERATION B	-6759.80	-6173.90
AGE ITERATION C	-6629.41	-6118.90

Table 5-21 - IGBT Collector-Emitter Voltage Rate of Change (dV_{CE}/dt) turn-on transient Phase 4, IRG4BC30KD IGBT Sample 14, Measured vs Linear Piecewise Model

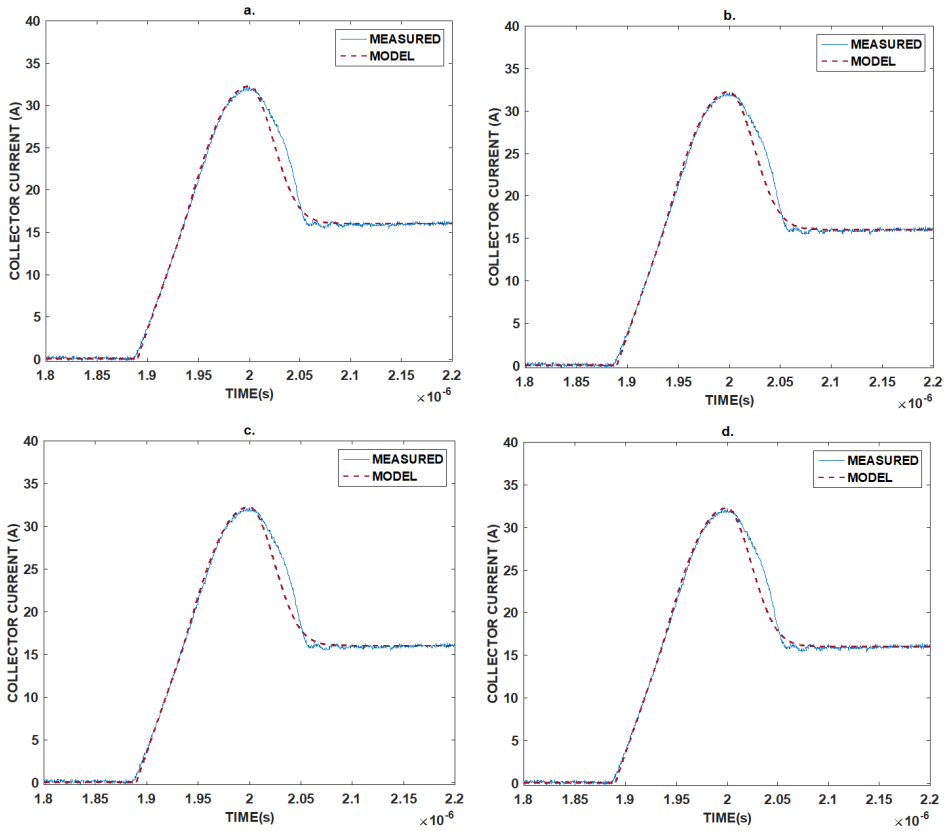


Figure 5.64 - IGBT Collector Current (I_C) turn-on transient, IRG4BC30KD IGBT Sample 14, Non-Linear Model (a) New (b) Age Iteration A (c) Age Iteration B (d) Age Iteration C

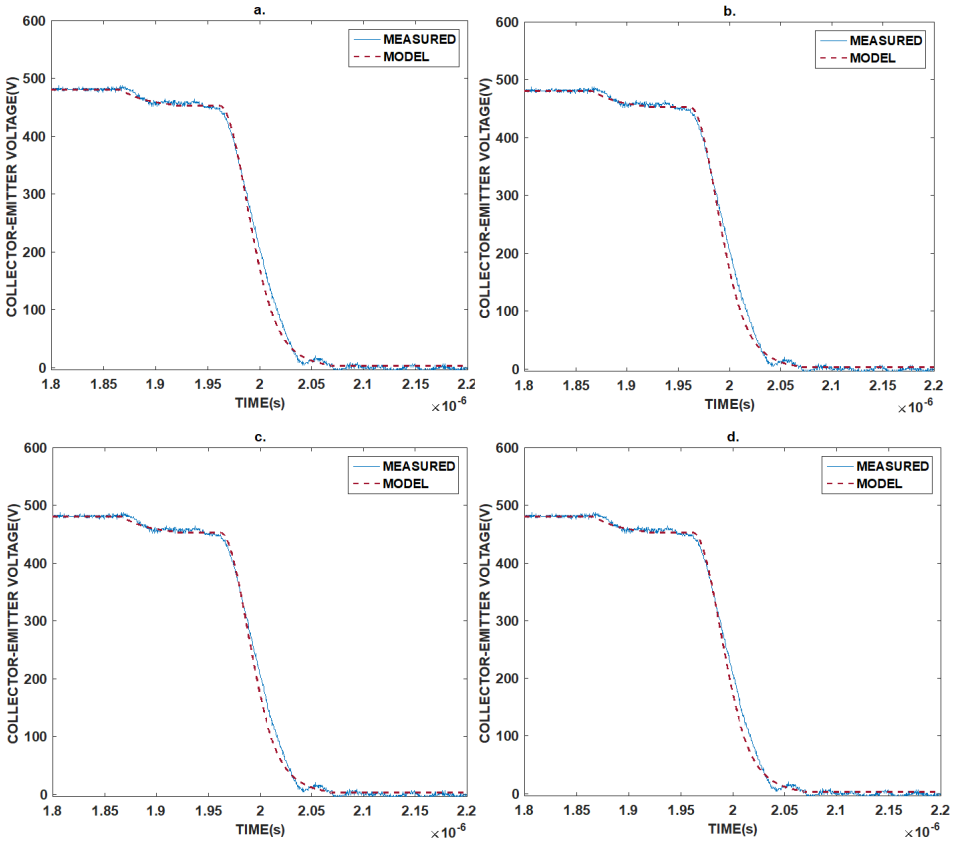


Figure 5.65 - IGBT Collector-Emitter Voltage (VCE) turn-on transient, IRG4BC30KD IGBT Sample 14, Non-Linear Model (a) New (b) Age Iteration A (c) Age Iteration B (d) Age Iteration C

5.6 Conclusions

This chapter presented the analysis and corresponding modelling of the IGBT's switching transients. Essentially the presented analysis took two approaches, to present mathematically the IGBT's switching collector-current (I_C) and collector-emitter voltage (V_{CE}) transients and the corresponding evolution with the implemented accelerated ageing. The first approach was conducted through an IGBT switching equivalent circuit, describing the different turn-on and turn-off switching phases via piece-wise linear modelling based on circuit analysis and the model put forward by Jin et al. [215]. The second approach was based on the Rajapakse et al. [213], time-domain switching transient analysis model, obtaining non-linear mathematical functions which were modelled on the transient's characteristic variation with time, for the different turn-on and turn-off phases. Moreover, this chapter presented the proposed equations' modifications or completely new model equations, accompanied with a detailed discussion, to reflect the changes introduced by the implemented accelerated ageing, which is considered a useful contribution to knowledge. The first approach was useful to understand the influence of the IGBT's parasitic elements on the switching transients vis-à-vis the implemented accelerated ageing, especially during the different turn-on and turn-off phases which were governed by a linear relationship with time. The second approach was useful to obtain a more representative model of the IGBT's switching transients, including the different non-linearities that manifest when the IGBT is new or introduced when the IGBT was subjected to the implemented accelerated ageing. From the above analysis, it was noticed that the implemented degradation was predominantly influencing the turn-off transients, hence slowing the IGBT's turn-off. On the other side it was minimally influencing the turn-on transients. A main contributor to these changes was the observed degradation in the die-attach, which led to an increase in the junction temperature (T_J). This heavily influenced the collector-current (I_C) turn-off transient, with an enhanced "tail current", but indirectly the increase of the junction temperature (T_J), influenced as well, the operation of the IGBT's parasitic devices predominantly the collector-gate Miller capacitance (C_{CG}) during turn-off, manifesting in the elongation of the Miller plateau during this phase. Moreover, it was hypothesized that the implemented accelerated ageing impacted the input capacitance (C_{IES}), more specifically the gate-emitter capacitance (C_{GE}), through contamination of the IGBT's gate dielectric oxide. Hence this chapter provided a clearer picture of the root causes of the monitored IGBT transient changes in relation to the inflicted degradation, hence providing a better understanding in interpreting the measured changes in the conducted EM emissions.

Chapter 6 IGBT's Ageing and EM Conducted Emissions

6.1 Introduction

Electromagnetic compatibility (EMC) is defined as "the ability of an equipment or system (installation) to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment" [231]. Hence EMC has two main requirements [232]:

1. Ensure that the equipment's or system's emissions of EM disturbances are limited to a satisfactory degree. This entails the determination of the amount of radio energy that can be picked up by third parties (radiated emissions). Moreover, it entails the determination of the energy conducted on power and communication cable interfaces (conducted emissions).
2. Ensure that the equipment or system has a sufficient level of immunity to maintain adequate performance in the presence of EM disturbances to which it is subjected. This includes immunity against both radiated and conducted interference.

To ensure equipment's EMC, a series of tests are conducted to determine that the design of the equipment conforms to national, international, and industry governed standards and legislation. Several international organizations promote these standards and their harmonization. These include the International Electrotechnical Commission (IEC), the "Comité International Special des Pertubations Radioelectriques" (CISPR), the Advisory Committee on Electromagnetic Compatibility (ACEC), and the International Organization for Standardization (ISO). The main continental organizations, include the European Committee for Electrotechnical Normalization (CENELEC) and the United States (US) Federal Communications Commission (FCC). From an industry point of view these include, the Society of Automotive Engineers (SAE), and the Radio Technical Commission for Aeronautics (RTCA), amongst others. In relation to European legislation (within the European Union), EMC is regulated by the EU directive EN-2014/30/EU (previous version 2004/108/EU) [233]. This legislation entails the harmonization of the laws of all EU member states relating to EMC, of a vast range of electrical and electronic equipment and systems. Hence companies which manufacture and install such equipment and systems, need to ensure compliance to the above

directive, to manifest the CE mark. This is achieved by running EMC tests, which can be mainly divided into two categories, EM emissions tests and EM immunity tests.

6.1.1 EM Emissions Testing

In relation to radiated emissions testing, this is normally carried out within an anechoic chamber, an open area test site (OATS), or for relatively small equipment in a gigahertz transverse electromagnetic (GTEM) cell [235]. A receiving antenna or the GTEM cell itself, is utilized in conjunction with a radio receiver to pick up the emitted radiated interference from the equipment under test (EUT), which is rotated, hence evaluating the radiated emissions for a 360° pattern [233-234]. For a typical electronics product, this is conducted over a frequency range between 30MHz to 1GHz, even though there are standards which request for higher frequency testing, for example EU test requirements can go up to 6GHz, while for the FCC, the upper frequency range of measurement is related to the highest clock frequency utilized by the EUT. From an FCC point of view, the same reasoning applies for the lower frequency range, where measurements are required down to the lowest clock signal employed by the EUT [234]. The measured radiated levels need to be under a predefined limit which is dictated by the standard.

Conducted emissions testing, measures the EM energy conducted out through the cable interfaces attached. Cable interfaces refer predominantly to power ports (DC or AC depending on the nature of the EUT's attached power distribution network), but it also includes network or telecommunication cables. This ensures that the local power supply remains relatively 'clean', hence minimizing the interference to the other devices which are connected to the same power distribution network or communication lines. The test procedure will be described in more detail in Section 6.2.

6.1.2 EM Immunity Testing

EM immunity testing can be mainly divided into three categories; electrostatic discharge (ESD), radiated immunity testing, and conducted immunity testing. ESD is related to the abrupt flow of electricity caused by electrically charged objects due to low electrical impedance or a dielectric breakdown. Electrostatic buildup is caused by triboelectric effect or by electrostatic induction. ESD can cause disruptive events such as the corruption of memories or the resetting of equipment as well as destructive events such as the failure of electronic components than can suffer permanent damage when subjected to high voltages. ESD testing is conducted via

the use of an ESD simulator. This device charges to a specified high voltage (specified by the test procedure) an output circuit referred as the human body model (HBM) equivalent circuit. It consists of a capacitor which charges to the specified high voltage and discharges in a series resistor. One of the most common HBM output circuit is the JEDEC 22-A114-B, consisting of a 100pF capacitor and a 1.5kΩ discharge resistor [237], [240]. Other discharge networks are utilized for other standards. The EN 61000-4-2 is one of the most common European ESD immunity compliance standard, utilized for commercial electronics [236].

Radiated immunity testing is conducted to ensure that the EUT operates adequately when subjected to strong radiated EM fields. The EUT is placed in an anechoic chamber or a GTEM cell, again depending on the EUT's size, where RF noise is broadcasted, while concurrently monitoring the EUT's operation. The test entails a frequency sweep at a certain fixed level of electric field strength (V/m) and modulation mode (as specified by the specific standard), which is measured by a field sensor during the test. Typical values of field strength include 3 V/m for domestic equipment and 10V/m for industrial equipment [238]. Higher field strengths are employed for specific industries' products such as medical, automotive, aerospace and defense. The broadcasted RF noise can be demodulated by the EUT, possibly causing performance issues. Another test which can be classified as radiated immunity test, is the Magnetic Field Test (MFT). This test aims to simulate the effects of a magnetic field on the operation of the EUT. Magnetic fields can be generated from small sources such as motors or products' transformers, while larger magnetic fields can be generated from overhead or underground low-voltage or high-voltage cables, electric traction, electrical switchyards, substations, and distribution transformers. The European standard governing the above test is the EN 61000-4-8. The test dictates a continuous magnetic field of 100A/m and pulsed magnetic field of 1000A/m. Such powerful magnetic field levels are utilized to cater for the latter described large magnetic field sources. The test is conducted by surrounding the EUT, with a magnetic field at the power frequency (50Hz/60Hz), using an induction coil which is sourced through a constant AC current source. The EUT is subjected to the magnetic field with the coil oriented along the three axes [239]. Other variants of the magnetic field test exist, these include the Impulse Magnetic Field Test (IMFT) EN 61000-4-9 and the Damped Sine Magnetic Field Test (DSMFT) EN 61000-4-10.

Conducted immunity testing entails a variety of tests catering for different conducted hazards that might occur during operation. One of the most important conducted immunity tests is the Fast Transient Burst (FTB) test [240]. FTB testing aims to simulate the EM disturbance created by a "showering arc" at the contacts of an electromechanical relay, solid state device, or mechanical switch, as it opens. The inductance of the supply cables plus any inductance of the load, produces a voltage burst as the current is interrupted, until it breaks the air gap at the contacts producing an arc. The European standard governing the above test is provided in the basic standard EN 6100-4-4. The test is conducted using an FTB simulator which issues a unidirectional impulse on the test conductor, repeated at a 5kHz rate, with bursts lasting 15ms each, with a rate of three bursts per second. The impulse itself is characterized by an exponential rise, reaching 90% of the peak impulse test voltage within 5ns, and then decaying to 50% within 50ns. The rapidity and high voltage of the impulse makes this test extensively disruptive. The transients' bursts are injected into the AC or DC power cables via coupling-decoupling networks (CDNs). On the other side for signals, network or telecommunication cables, bursts are coupled using a capacitive clamp [240]. Another important conducted immunity test is the surge test. The surge test simulates the impacts of lightning on power supply cables that are defined as "long cables" (longer than 10m). This test is governed by the basic European standard EN 61000-4-5, which establishes the surge waveform issued by the surge simulator. This waveform is characterized by a unidirectional impulse of two types: a 1.2μs 100% rise / 50μs 50% decay into an open-circuit and 8μs 100% rise / 20μs 50% decay into a short circuit. This test is less disruptive when compared to the FTB test as the impulse is slower. On the other side it is more destructive as it contains more energy [240]. Other more application specific conducted immunity tests are utilized to emulate specific interference scenarios. These include power quality tests such as the: Voltage Dips test - EN 61000-4-11, Ring Wave test - EN 61000-4-12, Harmonics test - EN 61000-4-13, Voltage Fluctuation test - EN 61000-4-14, Ripple on DC test (RDC) - EN 61000-4-17, Damped Oscillatory Wave test - EN 61000-4-18.

Another salient conducted immunity test procedure is the Conducted Disturbance by Induced RF - EN 61000-4-6. Similar standards exist for other industries which are: MIL-STD-461 (Defense), RTCA/DO-160 (Aerospace), and the ISO 11452-4 (Automotive). This test is utilized to ensure that RF signals, when coupled onto the EUT's interface cables (both power and signals), do not cause any alteration or degradation in the EUT's performance. The test specifies the use of the Bulk Current Injection (BCI) technique, which utilizes a current

injection probe, to inject RF disturbances on the lines under test. The injected RF is monitored via a monitoring probe to ensure the injected RF level. For the EN 61000-4-6, the injected RF is specified for the bandwidth of 150kHz-80MHz, (it can go up to 230MHz). Another method specified by the same standard is the Direct Injection (DI) technique which employs the utilization of CDNs and an EM capacitive clamp, hence utilizing a test methodology like the FTB test [241].

A similar conducted immunity test but executed at a lower test frequency is the one defined by the EN 61000-4-16 standard. The test is conducted to assess the immunity of the EUT to common mode disturbances over the interface cables, at 0Hz and over the frequency range of 15Hz to 150kHz. The proliferation of motor control via variable-speed motor drives (VSD), which operate at switching frequencies under 150kHz, is contributing to the electromagnetic environment below this frequency to become much noisier, compared to past scenarios where direct-on-line methods were employed. The test utilizes a test generator which generates the specified disturbances. It injects the test stimuli into the EUT through CDNs for each type of cable tested. CDNs are invasive equipment, but alternatives such as the current injection clamps mentioned earlier are not specified within the EN 61000-4-16 standard, while at DC, such equipment will not work anyway. On the other side the employment of CDNs for high-speed data lines or high impedance lines is not recommended, as these are more suited for low-frequency, low-impedance lines, tending to self-disturb these kinds of lines. Thus, for the above scenarios the implementation of the above test will be difficult, requiring the utilization of special designed CDNs. Since this test does not employ RF frequencies, it does not require any special arrangement such as shielded rooms or anechoic chambers, but only the use of a good ground plane to appropriately earth/ground the EUT and the corresponding test equipment [242]. Again, it is ensured that when the EUT is exposed to such disturbances, its operation remains unaltered in all the intended modes. Figure 6.1 provides a summary of the basic EN immunity standards.

It is important to point out that the above is a generic, brief description of the different basic EMC standards and corresponding pool of test methodologies employed, highlighting the salient objectives and features of each test. Moreover, the above list is not exhaustive, as there are multiple other industry specific standards and tests which have not been discussed.

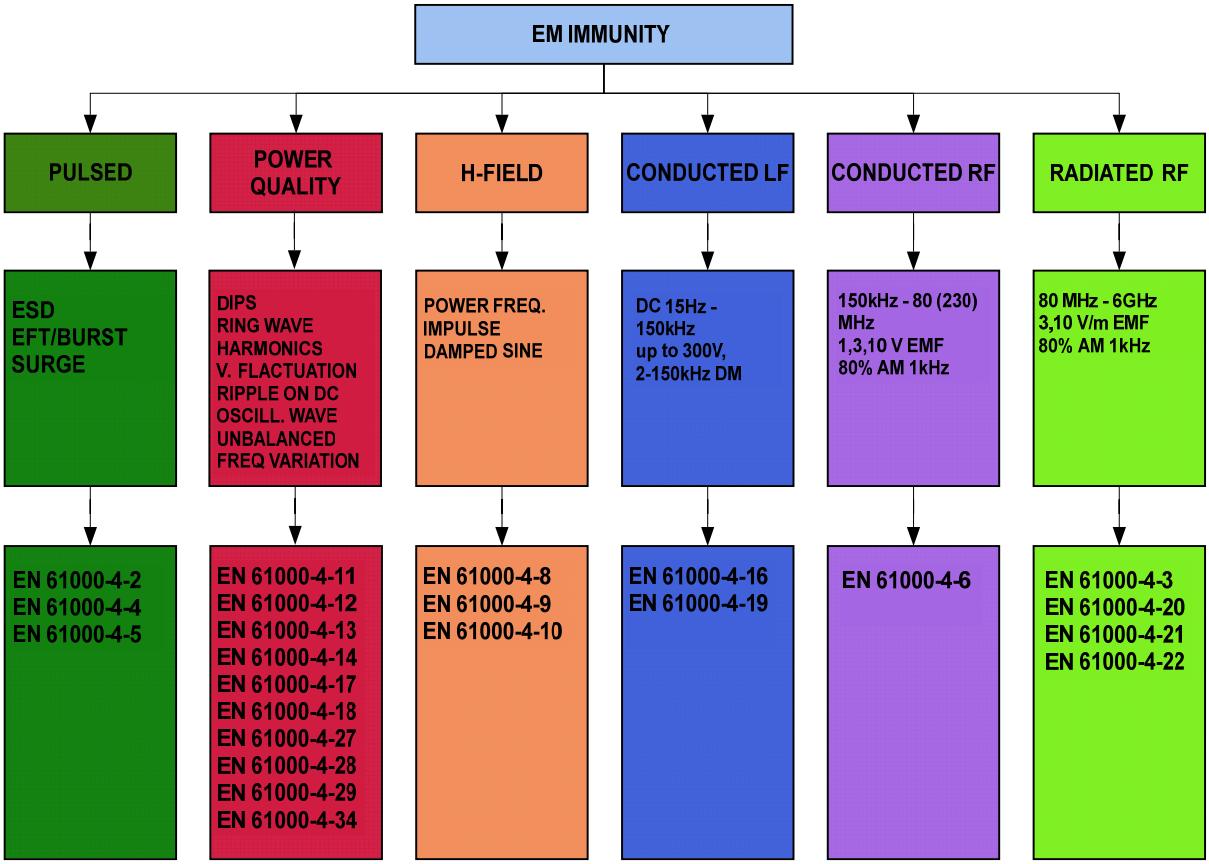


Figure 6.1 – EMC immunity tests and corresponding standards

6.2 EM Conducted Emissions

In EMC, conducted emissions testing is mainly concerned with the RF energy conducted by the EUT via its power lines, though interference on any other ancillary cables is also of interest. Conducted emissions can cause interference in two ways; first by entering another device which is connected to the same power network, secondly, they can become radiated emissions using the power network wiring and cabling, which act as an antenna. There are various EMC standards which govern conducted emissions testing. These include generic standards such as the IEC/EN 61000-6-4:2018 (EMC Generic standards – Emission standard for industrial environments) and the CISPR16-1-2:2014 (Specification for radio disturbance and immunity measurement apparatus and methods – Part 1-2 Conducted Disturbances), and more industry specific standards such as the military standard MIL-STD-461G-2015. These define the maximum permissible conducted signal levels (defined as disturbance voltages), over the different frequency ranges. Generally conducted emissions measurements are usually performed over the frequency range of 150kHz to 30MHz [248].

6.2.1 Line Impedance Stabilization Network (LISN)

During testing, measurement of the conducted disturbance out of the EUT, is determined via a special equipment referred as a Line Impedance Stabilization Network (LISN). This equipment is also referred as Artificial Mains Network (AMN). The LISN has three main functions during emissions testing [243]:

1. It provides a stable impedance (usually 50Ω) at the measurement frequencies, on the power network end of the EUT power lines.
2. It blocks RF signals available on the power network from entering the measurement equipment.
3. It provides a port for attaching measurement instruments (such as EMI receiver, spectrum analyzer or oscilloscope) to determine the conducted disturbance levels produced by the EUT.

Figure 6.2 illustrates a high-level generic connection of the LISN within an EM conducted emissions test setup. The EUT power cord is plugged into the output power connector of the LISN. The input power connector of the LISN is plugged to the power network. The measurement instrument (i.e. EMI receiver) is connected to the LISN's measurement port in order to be able to measure the levels of conducted emissions. Different types of LISNs maybe required for different device types or for different standards. LISNs can differ in terms of the maximum output current rating, maximum AC/DC sustained voltage, frequency range and the impedance they present to the EUT. Moreover, some LISNs can support AC three phase power applications or DC input power. Furthermore, LISNs may also have special features such as built-in high-pass filters, transient limiters, remote control capabilities, artificial hand capabilities etc.

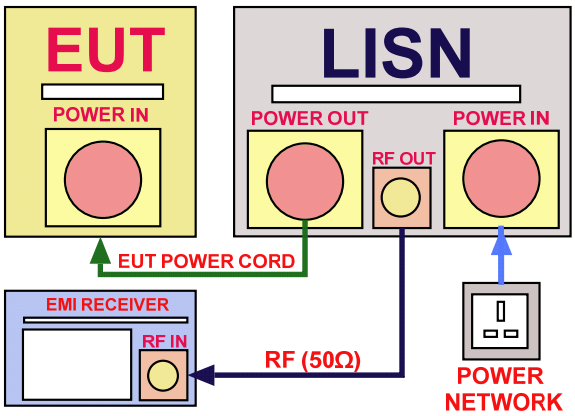


Figure 6.2 - Generic connection of the LISN within an EM conducted emissions test setup

Figure 6.3 shows the internal conceptual schematic of a 50Ω/50μH+5Ω LISN (impedance curve is governed by these parameters). It illustrates the use of 50μH series inductors, for both the forward and backward power lines. The construction of these inductors usually determines the maximum current rating of the LISN. The 0.25μF capacitors help to filter out the incoming RF interference, couple the EUT's RF conducted emissions, while decoupling the input power line. The RF measurement port impedance (50Ω) is part of the total LISN impedance and hence a 50Ω load termination is to be utilized when no measurement instrument is attached to the LISN. Moreover, the 1kΩ resistors are utilized to discharge the 0.25μF capacitors if no external terminations are fitted on the LISN's RF outputs [248]. As the name implies, one of the main scopes of a LISN, is to provide a stable line impedance. Considering an AC mains power network, the stable line impedance is required during conducted emissions testing, since the impedance of an AC power outlet is largely dependent on the wiring behind that outlet and hence it varies from location to location. In this regard, Nicholson et al. [244], measured unfiltered AC mains absolute impedance values, across the United States, over the frequency range of 0.02-30MHz, evidencing a measured absolute impedance range from 1Ω to 450Ω. This is illustrated in Figure 6.4. This poses a problem, to ensure that conducted emission testing is repeatable between locations (different test laboratories). Hence through the utilization of the LISN, the EUT always sees the same impedance at the end of its power line input, thus obtaining a stable and normalized impedance, over the frequency range as requested by the specific conducted emissions standard (normally 150kHz to 30MHz). Figure 6.5 provides a sample impedance curve for a 50Ω/50μH+5Ω LISN.

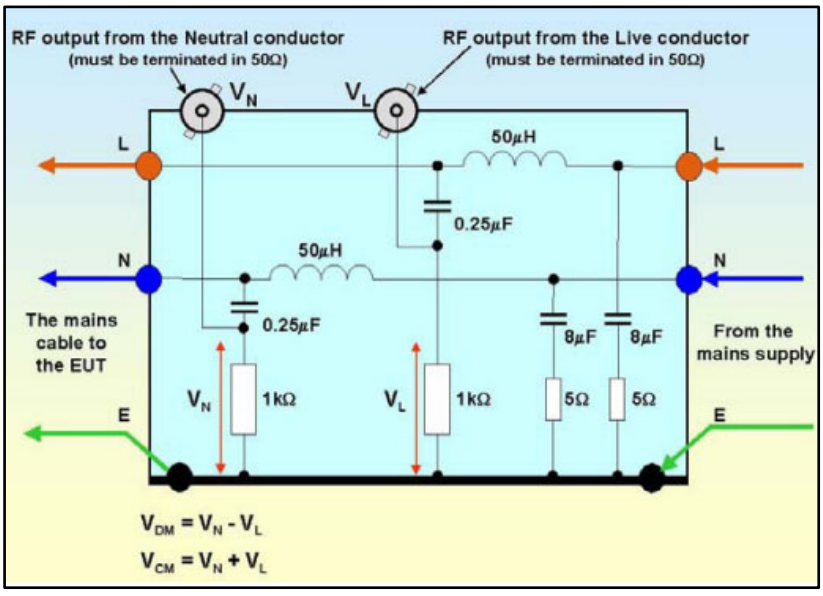


Figure 6.3 - Internal schematic of a 50Ω/50μH+5Ω LISN [248].

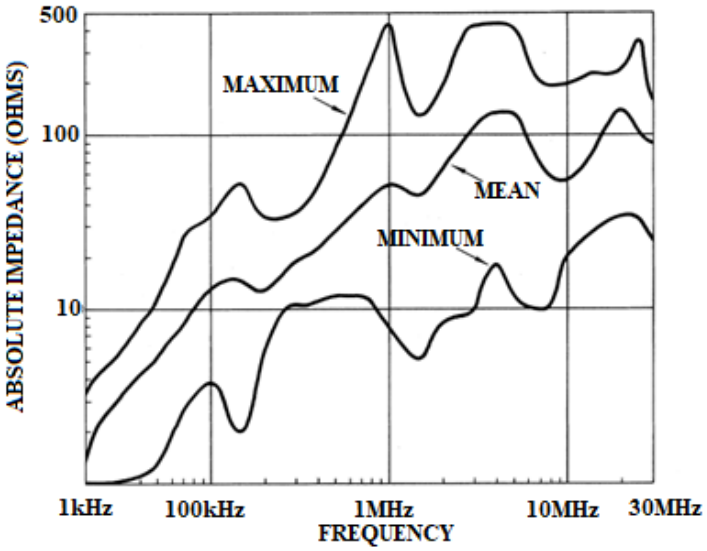


Figure 6.4 - Power line impedance variation 0.02-30MHz [244].

The impedance is very constant (close to 50Ω) over the frequency range of 150kHz to 30MHz. The drop experienced below 150kHz is due to the series inductor. Fully compliant LISNs must remain within a ±20% tolerance of the impedance curve, no matter the termination on the power network side [248]. The series inductor and shunt capacitor together form an LC low-pass filter, permitting the low frequency mains power (50/60Hz) to pass, while attenuating higher frequency signals. The value of the LISN inductance should be considered, when considering the wire harness inductance (i.e. 50µH for large wire power harness, whereas 5µH for small harness systems). However, the LISN type selection criteria must be based on the required measurement frequency range [245], as indicated in Figure 6.5.

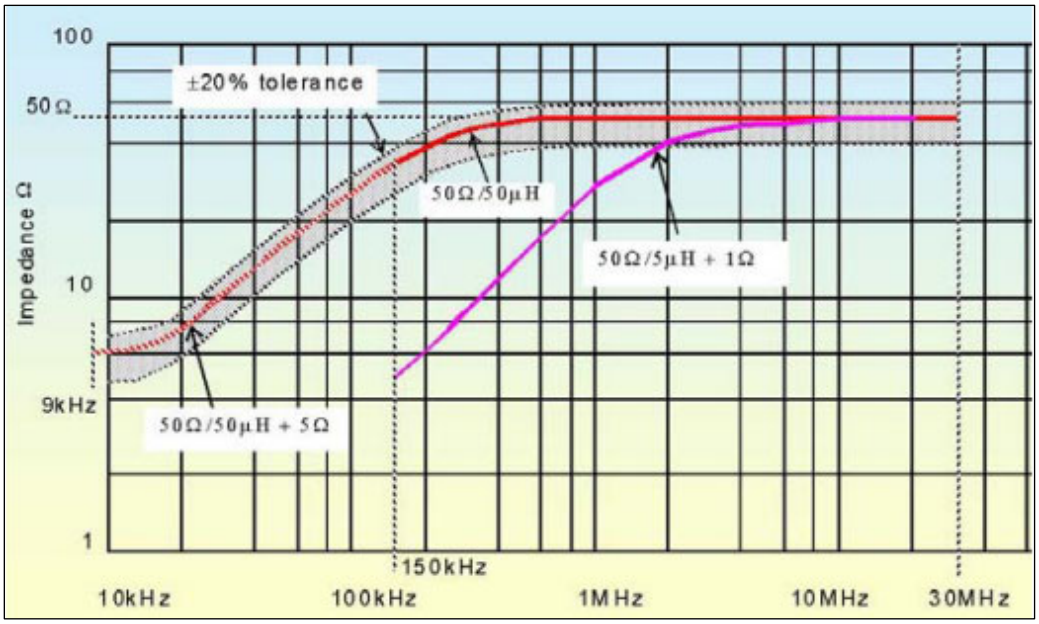


Figure 6.5 – LISN Impedance Curve [248].

6.2.2 General Conducted Emissions Test Setup

Conducted emissions standards which are based on the CISPR procedure specify limits on the conducted emissions over the frequency range of 150kHz to 30MHz. Conducted emissions European standards which are CISPR based include the EN55011, 55014-1, 55022, based on the CISPR-11, CISPR14-1, and CISPR-22 respectively. The methodology is largely similar between the above standards. The EN55015 which is based on the CISPR-15, on the other hand specifies a frequency range starting from a frequency of 9kHz [228]. Figure 6.6 illustrates the equivalent circuit of a single phase conducted emissions test setup. It highlights the use of the ground reference plane (GRP), consisting primarily of a horizontal conductive plane, which can be employed in conjunction with vertical conductive planes. Moreover, it illustrates how the measurement port is essentially measuring the combined contribution of differential mode (DM) noise and common mode (CM) noise on each of the two lines (Life or Forward line and Neutral or Return line) with respect to the GRP.

The LISN "earth" terminal (ET) connection, which is commonly an entire conductive plate, must be thoroughly bonded with the GRP. This is achieved by bolting the ET to the GRP or through the utilization of copper tape, or both. This ensures a low inductance path between the LISN's ET and the GRP. The EUT's "earth" connection, if available, too must be thoroughly bonded with the GRP. Standards such as the CISPR-22 specifies that any utilized GRP should be surfaced with at least 0.3cm of insulating material, to ensure safety during the test procedure [238]. Apart from the EUT's RF noise, there can be other causes which influence the conducted RF measurement. These include the stray capacitance between the EUT and the GRP, the RF impedance of the input cable and the RF impedance of the LISN, where the latter has been already discussed in the previous section. The stray capacitance between the EUT and the GRP provides a coupling path for the EUT's conducted RF disturbance to bypass the measurement systems. Hence full compliance standards such as EN55022 specifies a minimum fixed distance (40cm) between the EUT and the horizontal GRP [248]. This separation is utilized to minimize the stray capacitance between the EUT and the GRP and hence decreasing the effectiveness of the resultant coupling path. For relatively small EUTs, conducted emissions test procedure, specifies the use of a non-conducting (wooden) table (commonly 80cm high), where the EUT is placed on. This is illustrated in Figure 6.7. Again, standards specify that the EUT is placed at a fixed minimum distance (40cm) away from any vertical GRP [245].

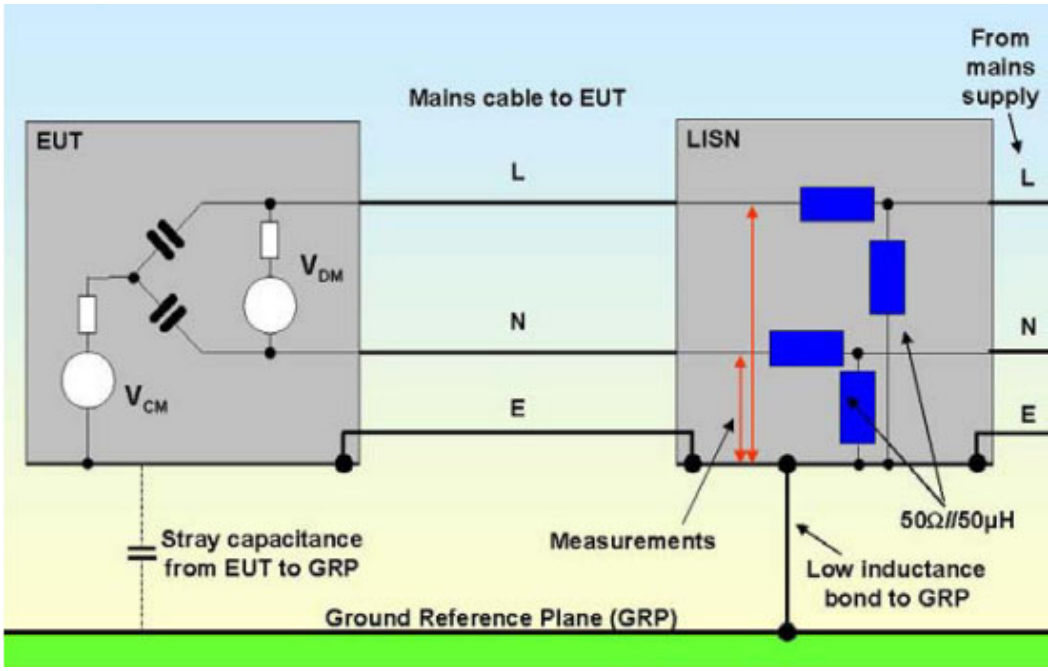


Figure 6.6 – EM conducted emissions single phase test setup equivalent circuit [238].

Another important aspect of the conducted emissions test setup is the input power network cable's impedance, which becomes significant in the conducted emissions frequency range of 20-30MHz. Hence full compliance standards, quoted earlier, advice against the laying out of these cables on the GRP to minimize the introduction of any stray capacitance. Moreover, these standards advice against the winding of the input cable extra length as this introduces stray inductance. It is often considered a good practice to utilize an unwounded (1m) input cable during the test procedure irrespective of the intended cable length of the EUT. Whatever the cable length and layout is, it must be fixed for the duration of the test and possibly photographed or drawn and reported with the test results [245].

CISPR procedures recommend that the ambient background noise level in the frequency band of interest, is measured multiple times during the conducted emissions test. This is conducted to ensure that no new ambient sources are introduced during the test procedure and hence mistakenly considered as part of the measurement [238], [245]. When conducting tests with AC mains as the input power network, an isolation transformer is to be utilized. This helps in the reduction of the electrical noise at the LISN input since any noise due the ground current path is omitted. Moreover, the use of an isolation transformer prevents from tripping the electrical system's residual current device (RCD), due to leakage current through the LISN circuitry [245].

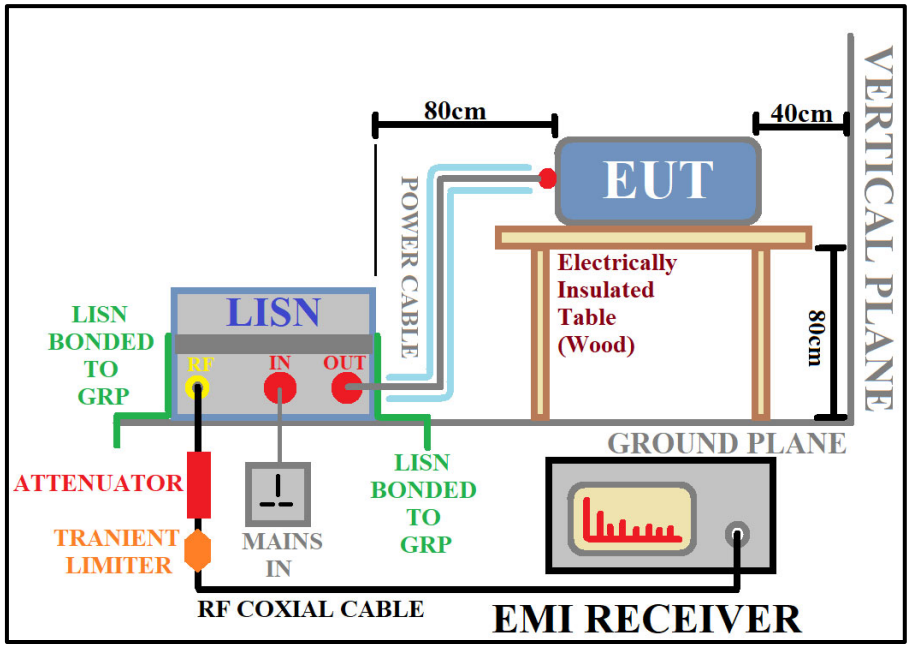


Figure 6.7 – Representation of the typical EM conducted emissions test setup as provided in [250].

6.3 IGBT's Ageing and its impacts on Conducted Emissions

In the past chapters it was established that the static and dynamic (switching) parameters of the tested IGBTs were manifesting changes due the implemented accelerated ageing. It was concluded that from a switching point of view, that tested IGBTs were experiencing a slow-down, predominantly in the turn-off transient, with the turn-on transient remaining relatively unchanged. It was argued that these changes were catalyzed by enhanced voiding in the die-attach which increased the thermal impedance of the junction, resulting in an enhanced junction temperature (T_J), and hence an enhanced presence of the "tail current". This latter effect, in conjunction with modelled changes in the parasitic elements of the IGBT, contributed to the general IGBT's slow-down.

Hence the aim of the study in this chapter, was to determine experimentally, measurable differences in the EM conducted emissions, of an EUT which utilizes a new IGBT and the same EUT but utilizing the same IGBT, when aged with the proposed accelerated ageing procedure. This was conducted by developing an experimental setup and following an experimental procedure to simultaneously measure the RF conducted emissions on both current paths (forward and reverse) of the EUT, as well as obtaining the IGBT's gate voltage (V_G), collector voltage (V_C) and collector current (I_C) to obtain the time-domain transients and frequency-domain spectra.

6.3.1 Implemented EM Conducted Emissions Test Setup

Figure 6.8 illustrates the high-level block diagram of the developed EM conducted emissions test setup. The setup is based on the setup developed to characterize the IGBT's switching parameters and transients, as described in Chapter 4. Commercial instrumentation includes the utilization of the MDO4104B-3 mixed domain oscilloscope, again utilized to capture a full cycle of the issued Double-Pulse for each of the gate voltage (V_G), the collector voltage (V_C) and the collector current (I_C), while computing on-board, for each of the above signals the Fast Fourier Transform (FFT) to obtain the corresponding frequency spectra. The same low voltage, high voltage, and current probes, as described in Chapter 4, were utilized for this purpose. The EUT during this test procedure, was the Double Pulse test circuit. Again, the double pulse was issued via a Tektronix AFG3015C programmable signal generator controlled via the already described custom-built software developed within National Instruments LabVIEW. The double-pulse was set with a first pulse duration of 2.2μs while the following pulse was set with a duration of 2μs. The double pulse was repeated every 0.1ms with a duty cycle of 6%. A low duty-cycle in conjunction with the monitoring of the IGBT's case temperature (T_C = 25°C), were implemented to ensure that the IGBT did not self-heat during EM characterization, hence making sure as much as possible, that any measured EM changes can be solely attributed to the inflicted IGBT degradation and not to any external source. In more practical applications larger duty cycles are utilized. For the power electronic circuit application employed here, a larger duty cycle would introduce heating effects (due to higher on-state power dissipation) which would possibly translate to greater EM conducting disturbances. The Keithley SMU2461 was utilized to issue the required auxiliary DC voltage, to power the double-pulse tester's gate drive circuit. This instrument was utilized due to its up-to-date calibration during the testing phase, and output voltage precision, with a quoted; resolution of 250μV, an accuracy at 25°C (±5°C) within a year of calibration of 2mV±0.015% of the set output voltage, and a noise (RMS < 10Hz) of 20μV [251]. This contributed to enhanced repeatability between the different conducted emissions experiments. It is important to point out that according to the CISPR conducted emissions procedure, all EUT's external power cables should be passed to the EUT via a LISN [245]. In the implemented conducted emissions test setup, the gate drive circuit auxiliary DC power supply, was not passed through a LISN. This was since only one LISN was available, and hence it was dedicated to the main power supply input, which is the DC Link voltage. On the other side the auxiliary DC voltage was not issued via a power network which has a variable output impedance (such as an AC mains network), but rather it

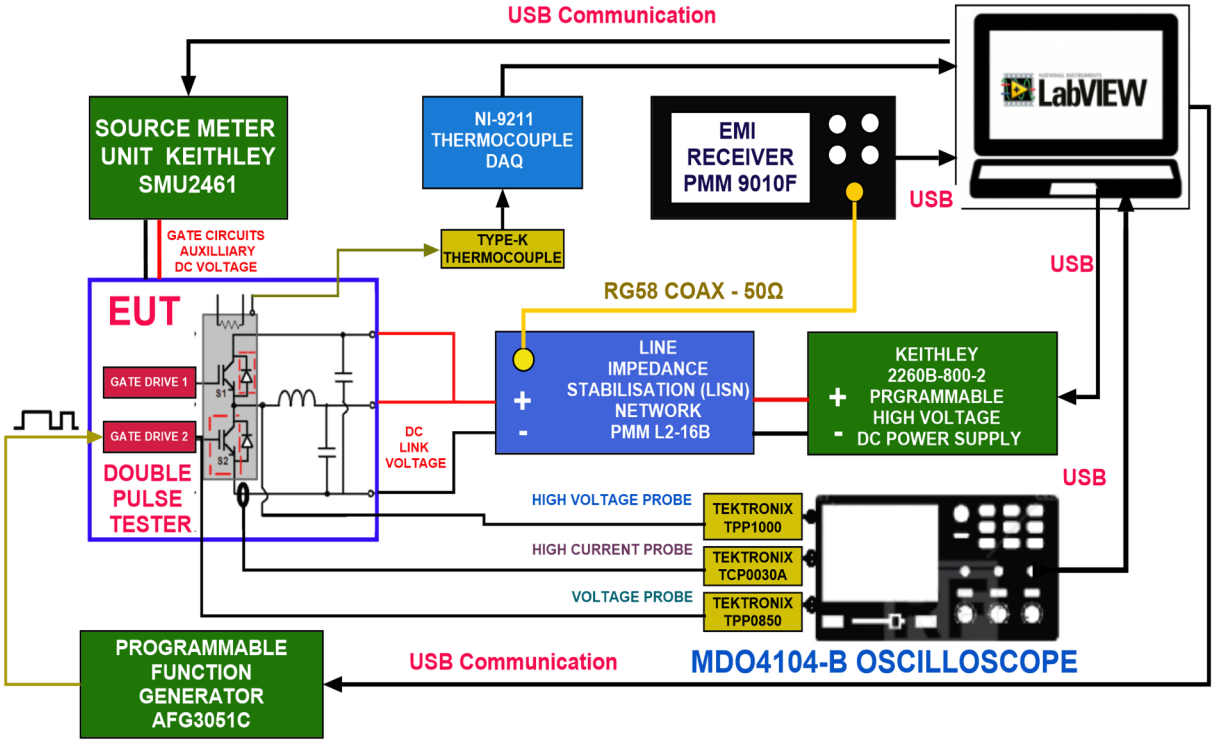


Figure 6.8 – High level EM conducted emissions, experimental setup.

was issued via the SMU2461 power supply, under the same output conditions, hence assuming a relatively constant output impedance during the different experiments. The Keithley 2260B-800-2 high voltage power supply, was again utilized to provide the DC link voltage to the EUT [252]. In this case the output of this power supply was not supplied directly to the Double-Pulse test circuit, but rather it was supplied to the input of the LISN. The utilized LISN was the NARDA PMM L2-16B. It is a CISPR compliant 50Ω//50μH+5Ω equivalent circuit LISN, with the following specifications: a BNC 50Ω RF output with frequency range of 9kHz-30MHz, continuous output rated current of 16A, maximum permissible output DC voltage of 250V DC, an allowable input power network supply frequency from DC-60Hz, an "Artificial Hand" capability for EUT's testing which involves manual handling and LISN remote control operation. Furthermore, it includes two front end switches, one to select the line for which the RF conducted emissions test is to be performed (L_1 forward line, L_2 return line), and the second switch to define the RF output frequency range according to CISPR16-1-1, with either conducted emissions tests in the range of 9kHz-30MHz or 100kHz-30MHz [254]. Figure 6.9 provides the CISPR equivalent circuit of the PMM L2-16B LISN. It is important to point out that this LISN had an up-to-date calibration during the testing phase. The LISN RF output was connected to a NARDA PMM-EMI Receiver 9010F. This EMI Receiver is a fully compliant CISPR 16-1-1 and MIL-STD-461 intended for measuring conducted disturbances from 10Hz up to 30MHz [250]. This EMI receiver is described as a real-time, gapless, direct conversion

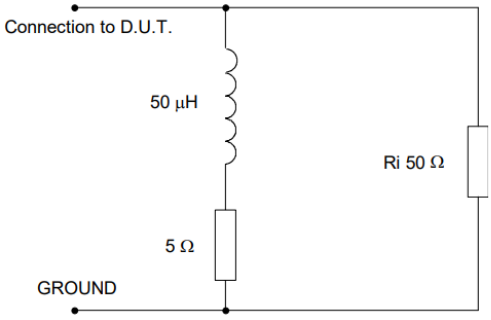


Figure 6.9 – NARDA PMM L2-16B LISN CISPR Equivalent Circuit [254].

EMI measuring receiver, based on a FFT calculation. This latter calculation is applied to a set of samples acquired in time domain, that outputs in a single shot the frequency contents of the input signal, within a frequency band. The EMI receiver is considered as real-time since the FFT is computed as fast as the incoming data. There are five salient parameters in relation to EMI receivers. These are the hold time, the frequency step, the test time, the gapless feature, and the detector. The hold time is defined as the minimum time the EMI receiver must wait at each frequency step. This time varies according to the standards, the nature of the disturbances, the minimum time required for the resolution bandwidth (RBW) filter to settle and the detector type. The frequency step is the amount by which the EMI receiver increases the tuning frequency. The test time is the total time required to fully scan the band of interest. For conventional receivers the test time corresponds approximately to, the required number of frequency steps within the band of interest, multiplied by the hold time, multiplied by the number of detectors and for conducted emissions multiplied by the LISN lines [255]. CISPR 16-1-1, specifies three EMI receiver's detectors which are referred to as the peak detector, average detector, and the quasi-peak detector. The choice of the detector depends on the type of signal to be measured based on the signal's amplitude, frequency, modulation, and discontinuities such as pulses. The peak detector considers the envelope of the signal by considering the peak value of each harmonic emitted in the signal during the hold-time. It is fast to execute and hence test results are obtained faster when compared to the other detectors but cannot be used for full compliance testing. It is commonly utilized as an initial test during pre-compliance, before proceeding to longer tests which employ full-compliance detectors, such as the quasi-peak or average detectors. The average detector as the name implies measures the average value of each harmonic emitted in the signal during the hold-time. The advantage of this detector is mainly for non-continuous signals such as pulsed signals since it will compute a lower average value when compared to the peak detector. The quasi-peak is a weighted detector (compromise between the peak and the average detectors) defined by two, time

parameters known as the charge time-constant and discharge time-constant (i.e. for CISPR16-1-1 Band B 100kHz to 30MHz, charge time-constant is 1ms and discharge time-constant is 160ms) [255]. This devalues the computation of a peak detector response especially for non-continuous signals. The CISPR16-1-1 defines other detectors such as the root mean square (RMS) detector where in this case the RMS is computed for each harmonic emitted in the signal during the hold-time. The RMS-average detector is a relatively new type of detector, defined in the CISPR16-1-1, making use of an RMS detector for pulse repetition frequencies above a cut-off frequency and the average detector for pulse repetition frequencies below the cut-off frequency [255]. The EMI receiver's gapless feature means that there are no time-gaps between consecutive time windows. The FFT capability of the NARDA PMM-EMI-9010F receiver, permits the processing of several frequencies at once, in a single time block corresponding to the hold-time. The wider the frequency band for each block the shorter the test time, but this width cannot be arbitrary wide as it impacts the reliability of the measurement. This technique significantly decreases the test time while ensuring direct conversion capability for the CISPR16-1-1 A band (9kHz-100kHz) and B Band (100kHz-30MHz) which are the common bands for conducted emissions testing. This procedure is depicted in Figure 6.10, where for a full A-Band and B-Band (9kHz-30MHz) scan with a quasi-peak detector and an RBW of 200Hz for the A-Band and 9kHz for the B-band and a hold time of 1s, the test time translates from 30 to 45 minutes with a legacy EMI receiver to 25 seconds with the NARDA PMM-EMI Receiver 9010F [250]. Moreover, this device includes various other capabilities, the salient ones being, RF input attenuators and pre-amplifier, RF input pre-selector utilized to filter any out-of-band energy, RF input pulse-limiter which is useful to protect the input stage of the receiver from any overvoltage transients. The pulse limiter has an integrated 10dB attenuator and a 30MHz low-pass filter. Finally, this receiver provides an RF output generator covering the CISPR16-1-1 A and B bandS. This has been extensively utilized during the testing procedure as will be described in Section 6.3.2. The EMI Receiver was configured, and data was captured through the accompanying PMM Emissions Suite software [250].

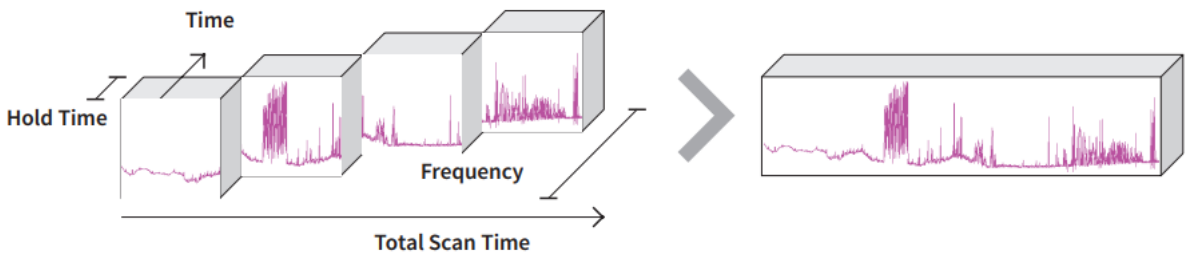


Figure 6.10 - NARDA PMM-EMI-9010Freceiver, FFT based, gapless direct conversion measurement method [250].

During the conducted emissions test procedure, the IGBT's case temperature (T_C) was monitored via a Type-K thermocouple and the NI DAQ, NI-9211. Vertical and horizontal planes were constructed out of aluminum sheets to act as the GRP. The two sheets were thoroughly bolted (16 Copper M6 bolts at intervals of 8cm) to each other to ensure an effective electrical connection between the two planes. The LISN was thoroughly bonded to the GRP by bolting (3 Copper M6 bolts on each side of the LISN) the LISN's bottom ground conductive plate to it. Moreover, the LISN's front earth connection was also wired and bonded to the GRP. All required power cables and wires were routed and fixed to the test table to keep the test setup unchanged between the multiple conducted emissions tests, executed for the different IGBT samples and age iterations. The rest of the area of the horizontal ground plane was covered with 5mm thick Perspex, to ensure electrical isolation and safety during the experimental procedure. The area occupied by the EUT was marked to ensure the same exact placement between the different conducted emissions tests. The EUT was placed 40cm away from the LISN (center to center), 50cm away from the vertical plane, 9.5cm above the horizontal plane, and 35cm away from the bottom of the wooden instrumentation table lying above the horizontal GRP plane. Figure 6.11 shows the developed setup.

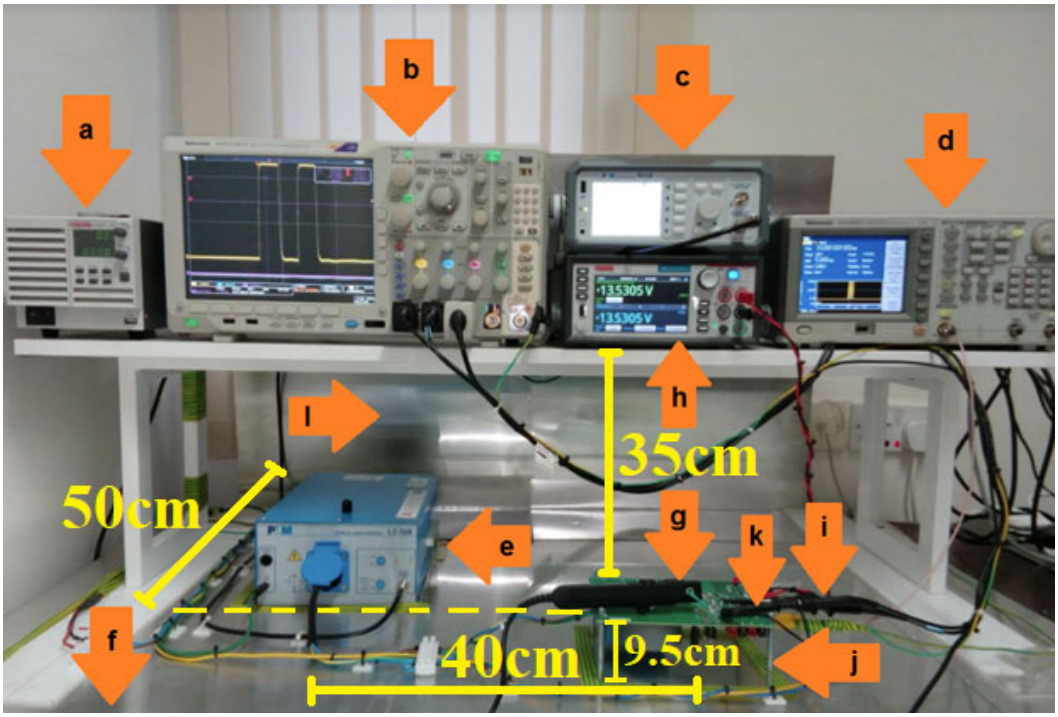


Figure 6.11 – Conducted Emissions experimental setup **(a)** High Voltage Power Supply (Keithley 2260B-800-2) **(b)** Mixed Domain Oscilloscope (Tektronix MDO4104B-3) **(c)** EMI Receiver (PMM 9010F) **(d)** Function Generator (Tektronix AFG3051C) **(e)** Line Impedance Stabilization Network LISN (PMM L2-16B) **(f)** Horizontal Ground Plane **(g)** High Current Probe **(h)** Low Voltage Power Supply (Keithley 2461 SMU) **(i)** High Voltage Probe **(j)** Double-Pulse Testing Circuit (EUT) (k) Low Voltage Probe **(l)** Vertical Ground Plane.

6.3.2 EM Conducted Emission Implemented Test Procedure

The following is the implemented methodology to characterize the impacts of the IGBT's ageing on the EM conducted emissions. The EUT's DC link voltage was set to 200V DC. This was conducted to ensure that this supply voltage is within the maximum permissible DC LISN's voltage (250V DC), hence allowing some safety margin. The utilized 200V DC link voltage in conjunction with an initial pulse duration of 2.2μs and load inductor of 66μH, translated to a test IGBT current of 6.67A. The front end of the PMM-9010F EMI receiver was protected via the activation of its internal pulse limiter which when utilized automatically introduces a 10dB attenuation. The PMM Emissions Suite software automatically accounts for the introduced attenuation. Moreover, a Panoma 4108-20 20dB 2W 50Ω attenuator was connected externally to the EMI receiver, to ensure that the front end is rigorously protected, and the rated EMI receiver input power of -10dBm/MHz is not exceeded [250]. This attenuator was characterized over the CISPR16-1-1 A and B bands spectrum (9kHz-30MHz). This was conducted by utilizing the embedded RF generator of the EMI receiver and the EMI receiver itself, relying on the fact that this instrument was covered by an updated instrument calibration certificate, where calibration factors were inserted within the PMM Emissions Suite software. This too applied for the PMM-16B LISN where the LISN's factor, as supplied via its calibration document was too inserted within the PMM Emissions Suite software. The procedure of characterizing the attenuator was executed by first obtaining the characterization of the utilized RG58 coaxial cable (supplied with the PMM-16B LISN), intended to connect the RF output of the LISN to the EMI receiver. This was conducted by looping the embedded RF generator output to the EMI receiver's RF input. The EMI receiver was configured with an RMS detector, a hold time of 0.1ms and RBW of 1kHz. Twelve power level readings corresponding to twelve frequencies, spread uniformly across the CISPR16-1-1 A and B band spectrum were obtained. The same procedure was conducted with the Panoma 4108-20 20dB attenuator in the loop. The PMM-9010F EMI receiver's embedded RF generator has a quoted output power level accuracy of ±0.5dBm while the EMI receiver itself has a quoted measurement accuracy of ±0.5dBm [250], hence contributing to a worst-case combined generation and measurement accuracy error of ±1dBm over the entire CISPR16-1-1 A and B bands. Table 7-1 tabulates the characterization results for the above procedure. The maximum measured difference between the theoretically issued power level by the RF generator, of -21.99dBm (85dBμV) and the actual measured level with the RG58 coaxial cable loop-back only, was of -0.44dBm, with a mean difference of -0.213dBm. This difference accounts for the

insertion loss of the cable as well as the combined inaccuracy of the embedded RF generator and EMI receiver. None the less, the measured maximum difference is well within the combined worst-case inaccuracy of the instrument. Moreover, Table 7-1 shows that the measured attenuation of the Panoma 4108-20 20dB external attenuator, was fairly constant over the bandwidth of interest, with a mean attenuation of 19.86dB and standard deviation (δ) of 0.012dB. During testing the PMM Emissions Suite software was configured in analyzer mode, obtaining a full-scan of the emissions over the full CISPR 16-1-1 A and B band spectrum. The PMM-9010F was configured to utilize an RMS detector with a hold time of 1ms and an RBW of 1kHz, translating to a test duration, to scan the entire bandwidth of interest, to approximately 10 seconds. These settings were considered optimal, when considering the nature of the signal (double-pulse signal manifesting discontinuous and pulsed conditions), the measurement resolution and the test duration. This latter parameter was fundamental vis-à-vis the amount of IGBT samples to survive the entirety of the pre-established accelerated ageing procedure (three age iterations), since the longer the scanning time, the more the device will be exposed to longer power dissipation, which accentuates self-heating effects, and enhances the probability of the IGBT to fail during conducted emissions testing, especially when considering that after age iterations, the device is already in a degraded state.

Characterization conducted with the PMM-9010F RF generator output power -21.99dBm (85dBμV)			
Frequency (MHz)	**Measured Power without 20dB Attenuator Cable Only (dBm)**	**Measured Input Power Cable with 20dB Attenuator (dBm)**	**Measured Panoma 4108-20 -20dB Attenuation (dB)**
0.09	-22.01	-41.86	-19.85
0.1	-22.02	-41.88	-19.86
3	-22.06	-41.92	-19.86
6	-22.13	-41.98	-19.85
9	-22.18	-42.05	-19.87
12	-22.19	-42.04	-19.85
15	-22.24	-42.10	-19.86
18	-22.28	-42.15	-19.87
21	-22.29	-42.12	-19.83
24	-22.37	-42.24	-19.87
27	-22.24	-42.11	-19.87
30	-22.43	-42.29	-19.86
Mean	**-22.20**	**-42.06**	**-19.86**
Standard Dev. (δ)	**0.132**	**0.135**	**0.012**

Table 6-1 – RG58 Cable and Panoma 4108-20 20dB attenuator characterization.

The following is the procedure followed to establish the impacts of the implemented IGBT's accelerated ageing on the EM conducted emissions:

1. The IGBT's static parameters namely the threshold voltage (V_{TH}) and transconductance (g_m) were measured when the device was new. These parameters were measured, first as ageing indicators, but also since they are important transient modelling parameters.
2. The EMI receiver was configured with an RMS detector, hold time of 1ms and RBW of 1kHz, and pulse limiter activated. The embedded EMI receiver's generator was looped to the EMI receiver's RF input via a 15cm RG58 cable (as now the LISN's cable was fixed with the setup as illustrated in Figure 6.11) and with the Panoma 20dB attenuator in the loop. Again, twelve power readings corresponding to twelve frequencies spread uniformly over the bandwidth of interest were measured via the EMI receiver. The test will proceed if the twelve frequencies' power readings are within ±1dBm of the measured readings within column three of Table 7-1.
3. The LISN's RF output was connected to the EMI receiver's RF input. At this point the setup is photographed, to have graphic evidence of exactly how the EUT was placed and how each cable was laid out. This was conducted to ensure setup consistency between the different experiments, hence ensuring experimental repeatability.
4. The EMI receiver was configured with an RMS detector, hold time of 1ms and RBW of 1kHz and pulse limiter activated. At this point an EM emissions CISPR 16-1-1 A and B bands scan was performed, but with the following instruments switched-off (low-voltage auxiliary power supply (Keithley SMU2461), the high-voltage power supply (Keithley 2260B-800-2), oscilloscope (MDO4104-B), and the function generator (AFG3051C)). This was performed to measure the conducted emissions noise floor for both the forward line (L_1) and the backward line (L_2). The test will proceed if all the measured frequencies for both lines are below -80dBm. Figure 6.12 illustrates a typical measurement of this background noise.
5. At this point the above instruments were switched-on, with the AFG3051C function generator issuing the double-pulse waveform, the low-voltage auxiliary power supply (SMU2461) supplying the gate drive supply voltage of 13.531V DC (to obtain a corresponding gate drive circuit, supply voltage of 15V DC), and the oscilloscope, ready to capture the relevant voltage and current transients. The high voltage DC

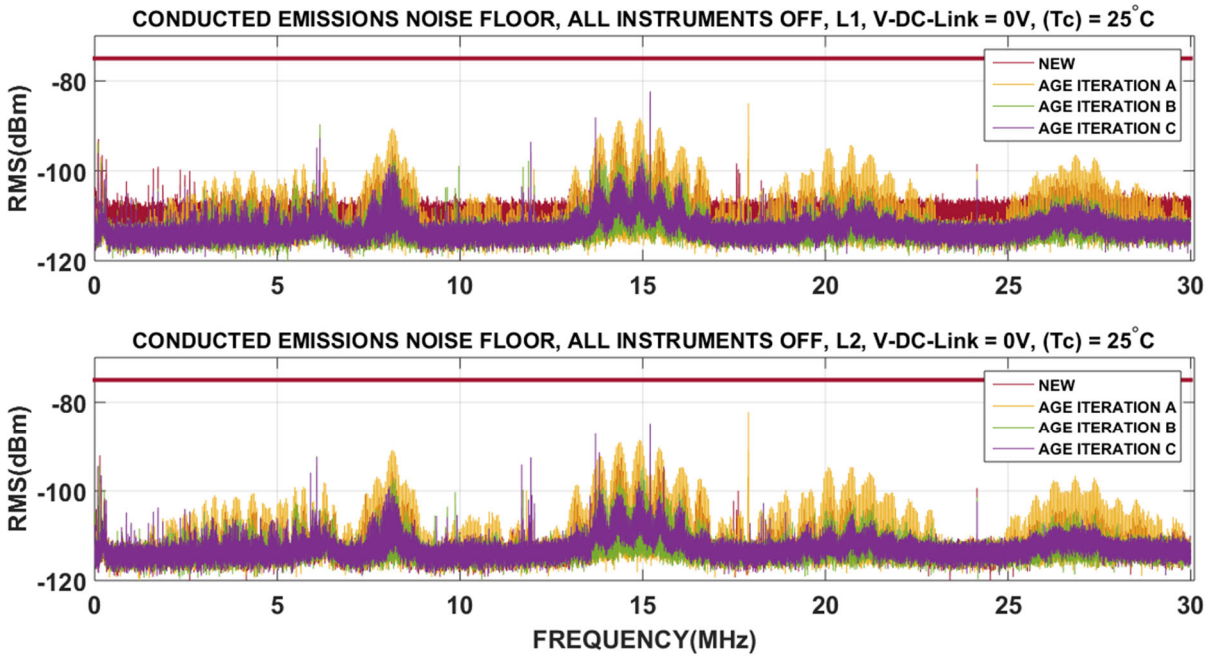


Figure 6.12 – IGBT Sample 3, conducted emissions noise floor, all instruments off.

power supply (Keithley 2260B-800-2) was switched on, but the output voltage at this point set to 0V DC. Again, the conducted emissions noise floor through the forward line (L_1) and backward line (L_2) were measured over the CISPR 16-1-1 A and B bands bandwidth, hence obtaining the background noise with the instruments on. The test would proceed if the measured frequencies for both lines are below -75dBm for frequencies smaller than 20MHz. Figure 6.13 illustrates a typical measurement of this background noise.

6. At this point the output of the high voltage DC power supply was enabled, where the DC link voltage would increase with a slew rate of 65V/s. As soon as the 200V DC is reached the PMM Emission Suite software performs a scan for the EM conducted emissions through the forward line (L_1). The output of the DC power supply is turned-off with a slew rate of 75V/s, eventually storing the captured spectral data for post-processing. This latter procedure was repeated to capture the EM conducted emissions through the return line (L_2)
7. During both measurements the collector-emitter voltage (V_{CE}) transient, and the collector current (I_C) transient, and the corresponding FFTs for each signal, were obtained through the mixed domain oscilloscope (MDO4104B-3). For both measurements, the FFT noise floor for the conditions described earlier (all instruments off and all instruments on but with the high voltage power supply output set to 0V DC),

were obtained. This evidenced an overall maximum noise floor level, of -35dBV for the collector voltage (V_C) and -60dBA for the collector current (I_C) FFTs.

8. The IGBT is aged according to the implemented accelerated ageing strategy, as described in Chapter 3, where each IGBT is subjected to three age iterations (Age Iteration A, B and C).
9. The measurement procedure as described through points 1 to 8 was repeated after each ageing iteration.

6.4 IGBT's Ageing and EM Conducted Emissions Characterization Results

The IGBT's conducted emissions characterization, vis-à-vis, the implemented accelerated ageing, involved the characterization of fifteen IRG4BC30KDPBF IGBTs, with ten IGBTs surviving the three full age iterations This section will mainly present two sets of frequency spectrum results. The first set of results presents the FFTs' of the IGBT's collector voltage (V_C) and the collector current (I_C). The second set of results presents the spectra of the conducted emissions for both the EUT's forward line (L_1) and return line (L_2).

6.4.1 IGBTs' Collector Voltage (V_C) Frequency Domain Evolution with Ageing

The FFT of the IGBTs' collector voltage (V_C) and the collector current (I_C) were computed via the embedded MDO4104B-3 mixed domain oscilloscope FFT function, capturing full double-pulse cycles for both measurements. The oscilloscope was configured with a time-domain sampling rate of 2.5GS/s. This meant that the maximum frequency that can be obtained via the FFT function was of 1.25GHz (since the $FFT_{BANDWIDTH}$ is equal to half of the time-domain sampling rate). This configuration was considered a good compromise between covering the relevant bandwidth of interests (<30MHz reflecting the Conducted Emissions CISPR16-1-1 A and B bands, at approximately the same FFT's bin resolution bandwidth, as the one set for the EMI receiver), while attaining the required time-domain resolution, to ensure the integrity of the captured time-domain collector voltage (V_C) and collector current (I_C) characteristics. Utilizing a Hanning window and capturing one million samples, this translated to an FFT bin resolution bandwidth of 1.25kHz. Figure 6.14(i-iv) provides the obtained collector voltage (V_C) FFT spectrum (till the bandwidth of interest <30MHz) of IGBT Sample 1, when the IGBT was new and after each age iteration. The obtained spectra were post-processed in MathWorks MATLAB, to obtain the predominant spectral peaks, moreover, obtaining a polynomial best fit curve (utilizing a least-squares technique) through the detected frequency peaks. This is again illustrated in Figure 6.14(i-iv), superposed on the obtained FFT spectra.

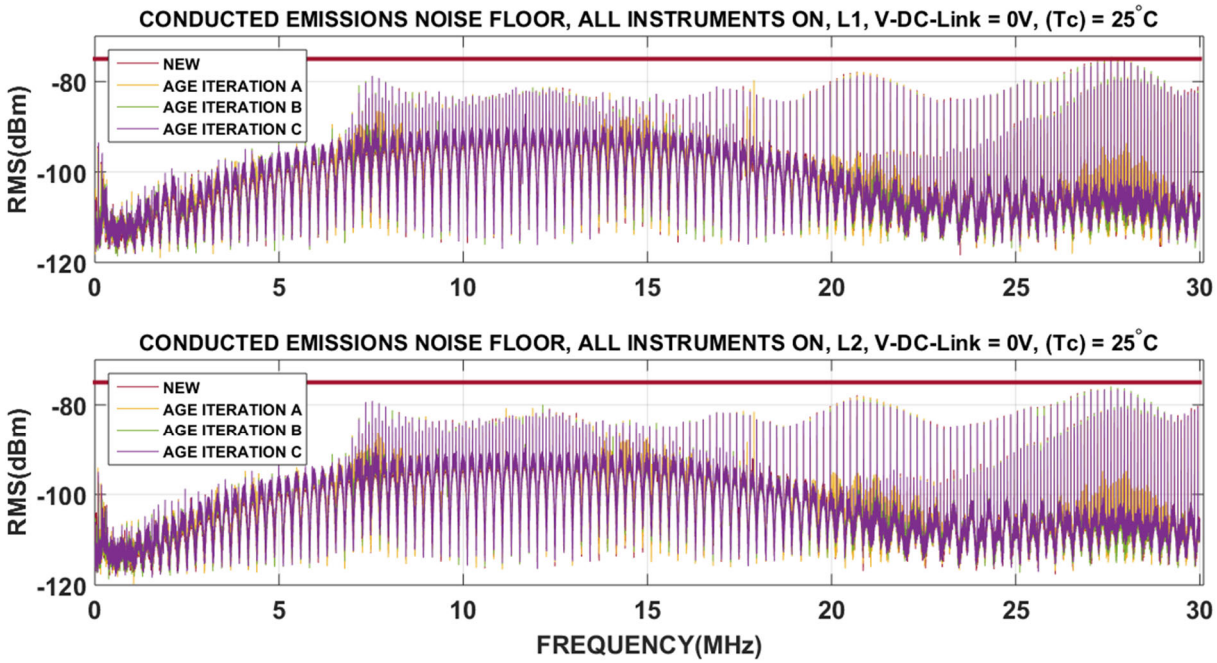


Figure 6.13 - IGBT Sample 3, conducted emissions noise floor, all instruments on, DC Link Voltage at 0V.

Figure 6.15(i-iii) provides the comparison between the collector voltage (V_C) FFT spectra of IGBT Sample 1, when new and after each age iteration. One can notice an evident decrease in the magnitude of the frequency peaks after each age iteration. Moreover, Figure 6.15(iv), illustrates the superposition of the detected frequency peaks fitted curves, when new and after each age iteration for IGBT Sample 1, evidencing that the monitored decrease in the magnitude of the collector voltage (V_C) spectral peaks, is progressive. This is further substantiated by Figure 6.18(i-iv) and Figure 6.19(i-iv), which illustrates the evolution of the detected frequency peaks fitted curves, of eight out of the ten IGBT samples characterized during this test phase, evidencing that this decrease is predominant in the frequency range of 8MHz to 25MHz.

Figures 6.20, 6.21, 6.22 and 6.23 illustrate the comparison of further post processing, conducted on the obtained IGBT's collector voltage (V_C) FFT spectrum, namely when the IGBT was new and after the final age iteration (Age Iteration C). These latter figures depict the corresponding FFT spectra, with a frequency bin resolution of 1MHz, computed from the corresponding detailed frequency spectra, illustrated in Figures 6.16 and 6.17. A bin resolution of 1MHz was utilized, to obtain a simplified analysis of the spectral changes happening across the bandwidth of interest. Figures 6.20 and 6.21 illustrate, the computed average magnitude, while Figures 6.22 and 6.23 illustrate the measured maximum magnitude, of the collector voltage (V_C) for every 1MHz frequency bin, for eight of the ten IGBT samples characterized. Both plots provide an easier understanding, of the spectral changes occurring due to the

implemented accelerated ageing, which through the detailed spectral plots provided in Figures 6.16 and 6.17, it would have been more difficult to analyze and visualize. This is especially true for the average magnitude, as it provides an easier and clearer understanding of the spectral changes (decrease or increase) happening within each frequency bin.

The data as depicted in Figure 6.20 and Figure 6.21, of all the ten IGBTs characterized during this test phase, were combined, and summarized in a box and whiskers plot, depicted in Figure 6.24, hence obtaining the statistics of the average spectral magnitude, for every 1MHz frequency bin. Similarly, the data as depicted in Figure 6.22 and Figure 6.23 were combined in Figure 6.25 obtaining the statistics of the maximum spectral magnitude, for every 1MHz frequency bin. For Figure 6.24, the center of each box represents the median of the IGBT samples' average spectral magnitude of the collector voltage (V_C) for every 1MHz frequency bin. The ends of each box represent the 25^{th} percentile and 75^{th} percentile, while the whiskers represent the minimum and maximum of the combined average magnitude of the IGBTs' collector voltage (V_C), for each 1MHz frequency bin.

Figure 6.24 demonstrates that the implemented accelerated ageing produced a general decrease, throughout the different IGBT samples, in the average collector voltage (V_C) spectral magnitude, across the frequency range of 8 to 30MHz, with the most predominant decrease, manifesting across the 13MHz to 20MHz bandwidth. The largest mean, average collector voltage (V_C) spectral magnitude decrease occurred in the frequency bin of 14MHz-15MHz, with a corresponding mean percentage decrease to the mean average value when the IGBTs were new of 14.52%. No frequency bin experienced any increase in the average collector voltage (V_C) magnitude. In addition, Figure 6.25 demonstrates that there was a general decrease, throughout the different IGBT samples, in the measured maximum collector voltage (V_C) spectral magnitude, across the frequency range of 8 to 30 MHz, with the most predominant decrease experienced across the 12MHz to 21MHz bandwidth. The largest mean, maximum collector voltage (V_C) spectral magnitude decrease, occurred in the frequency bin of 12MHz-13MHz, with a corresponding mean percentage decrease to the mean maximum value when the IGBTs were new of 18.63%.

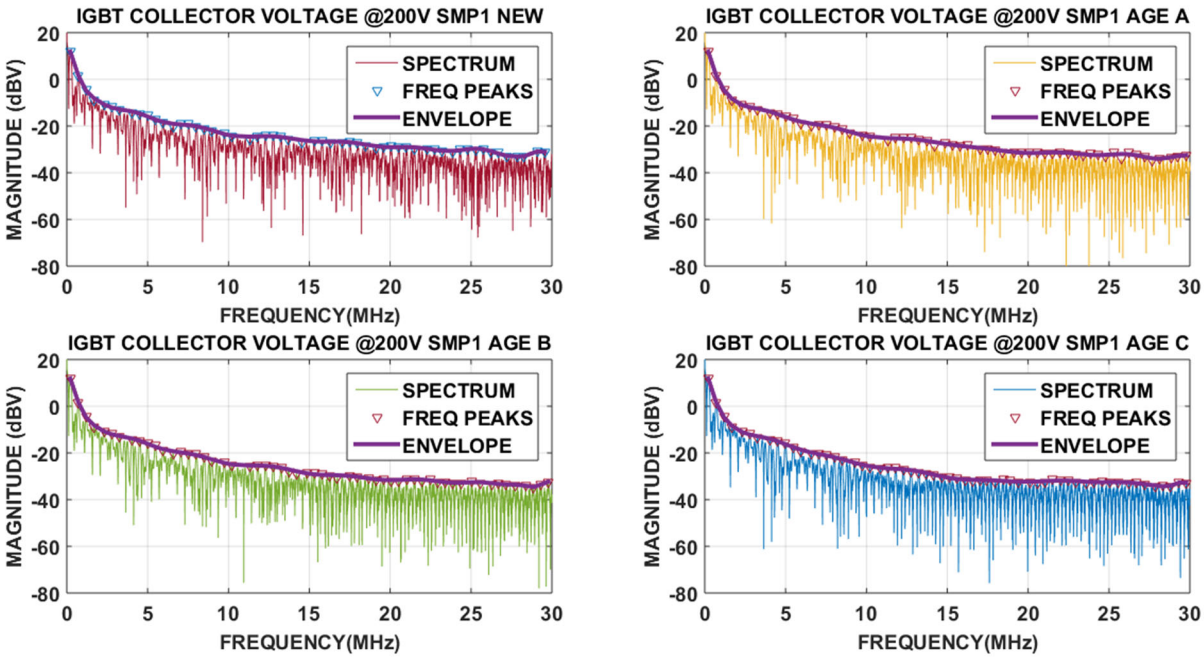


Figure 6.14 - IGBT Sample 1 Collector Voltage (V_C) FFT, Frequency Peaks, and corresponding Peaks Envelopes (i) New (ii) Age Iteration A (iii) Age Iteration B (iv) Age Iteration C.

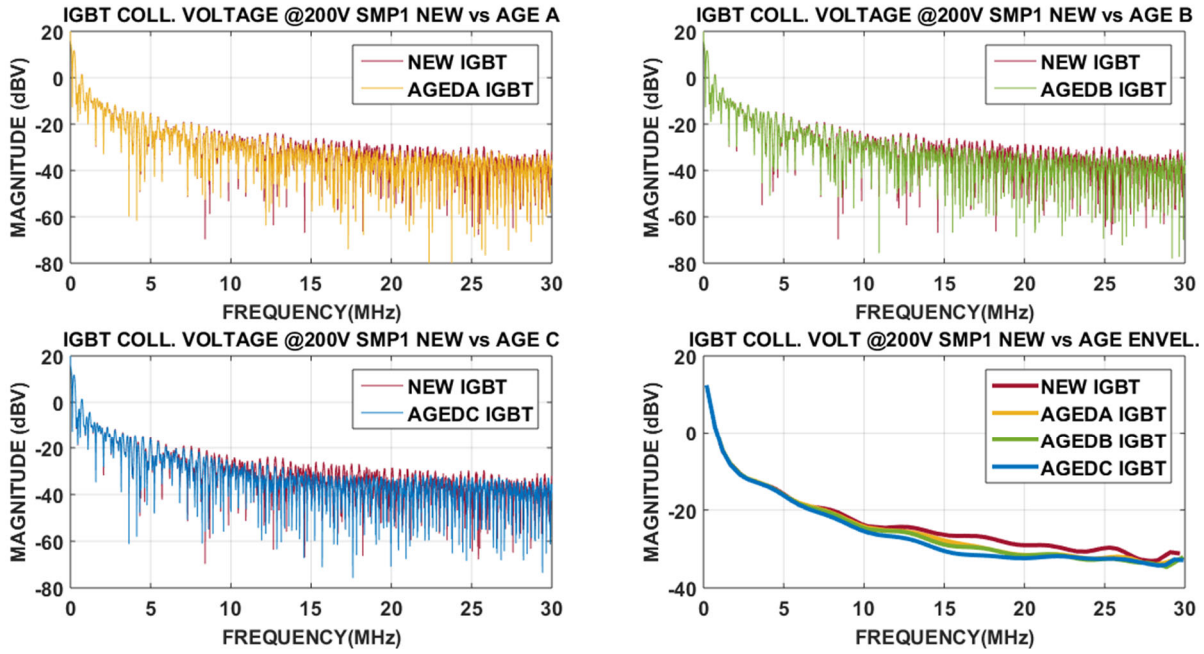


Figure 6.15 - IGBT Sample 1 Collector Voltage (V_C) FFT (i) New vs Age Iteration A (ii) New vs Age Iteration B (iii) New vs Age Iteration C (iv) Comparison of All Iterations Frequency Peaks Envelopes.

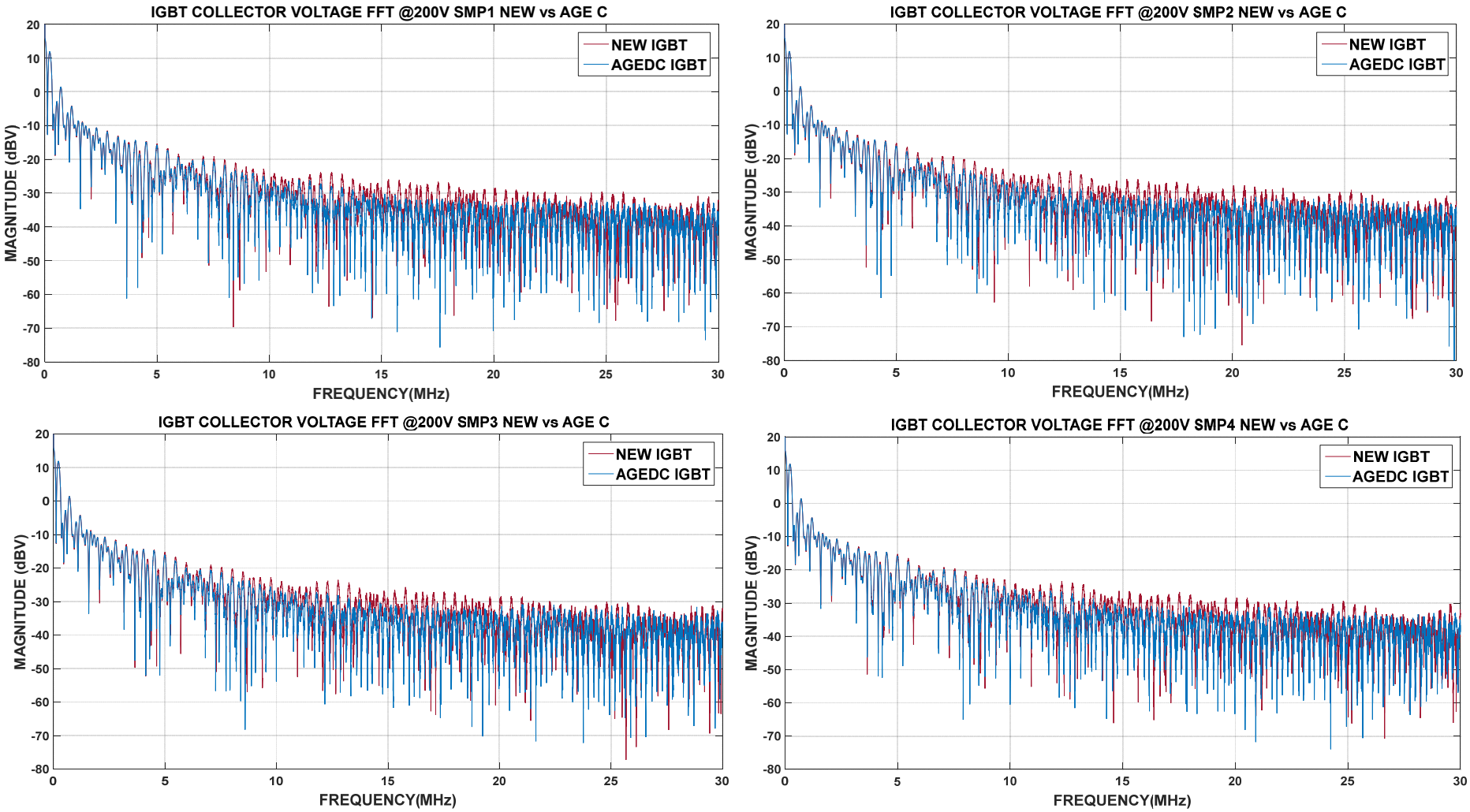


Figure 6.16 - IGBT Samples 1 to 4, Collector Voltage (V_C) FFT, New vs Age Iteration C.

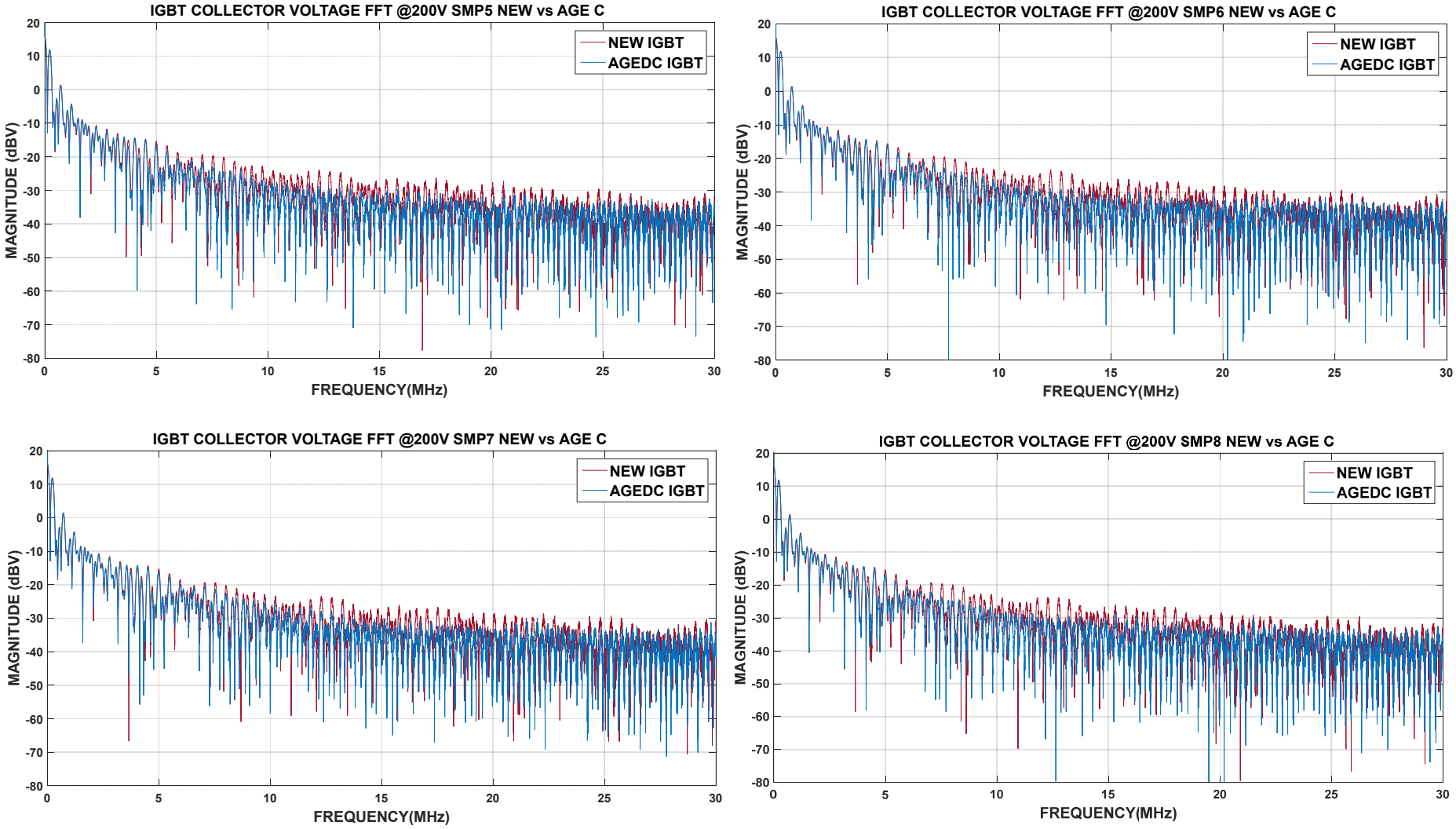


Figure 6.17 - IGBT Samples 5 to 8, Collector Voltage (V_C) FFT, New vs Age Iteration C.

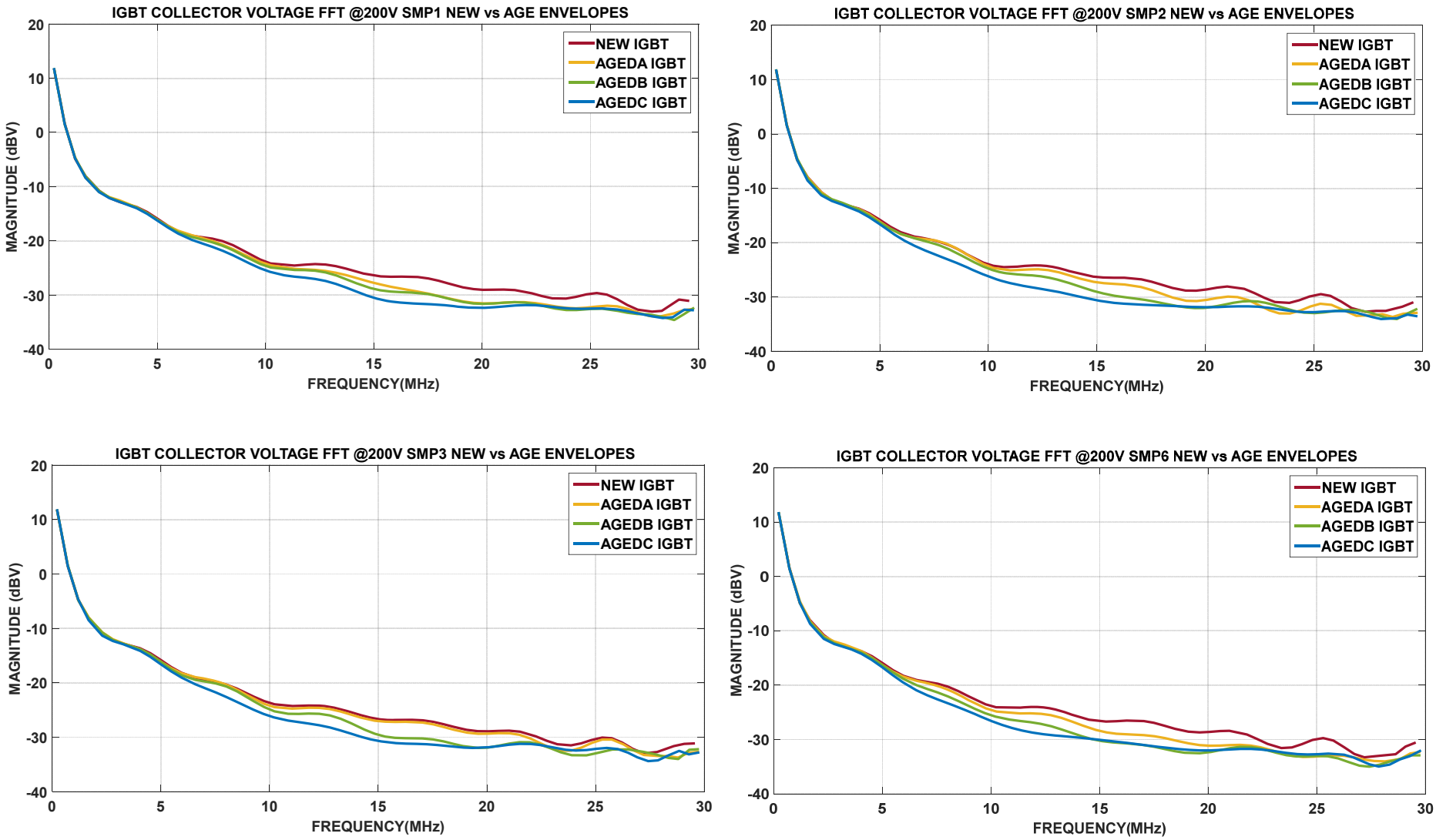


Figure 6.18 - IGBT Samples 1 to 4, Collector Voltage (V_C) FFT, Frequency Peaks Envelopes.

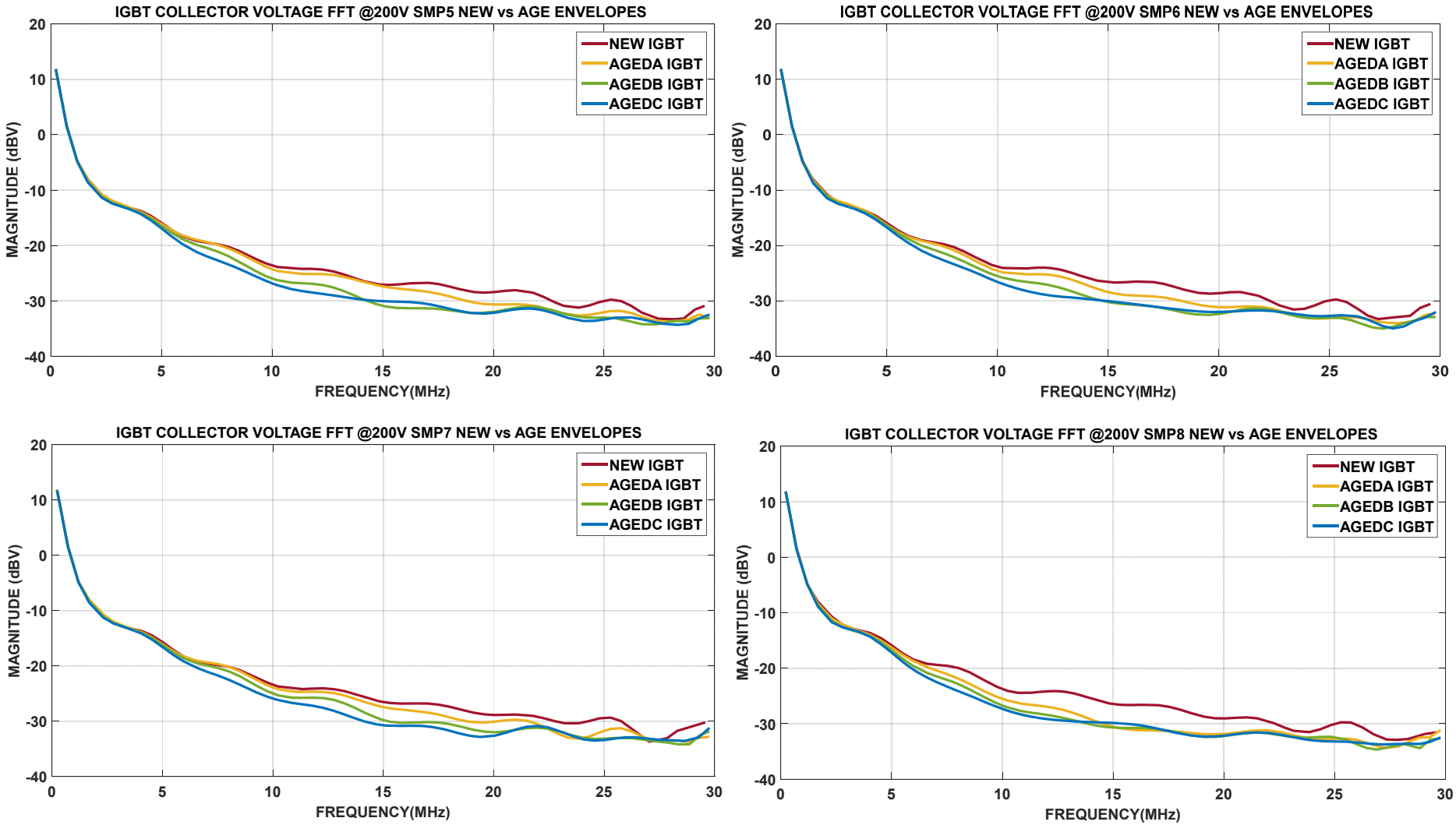


Figure 6.19 - IGBT Samples 5 to 8, Collector Voltage (V_C) FFT, Frequency Peaks Envelopes.

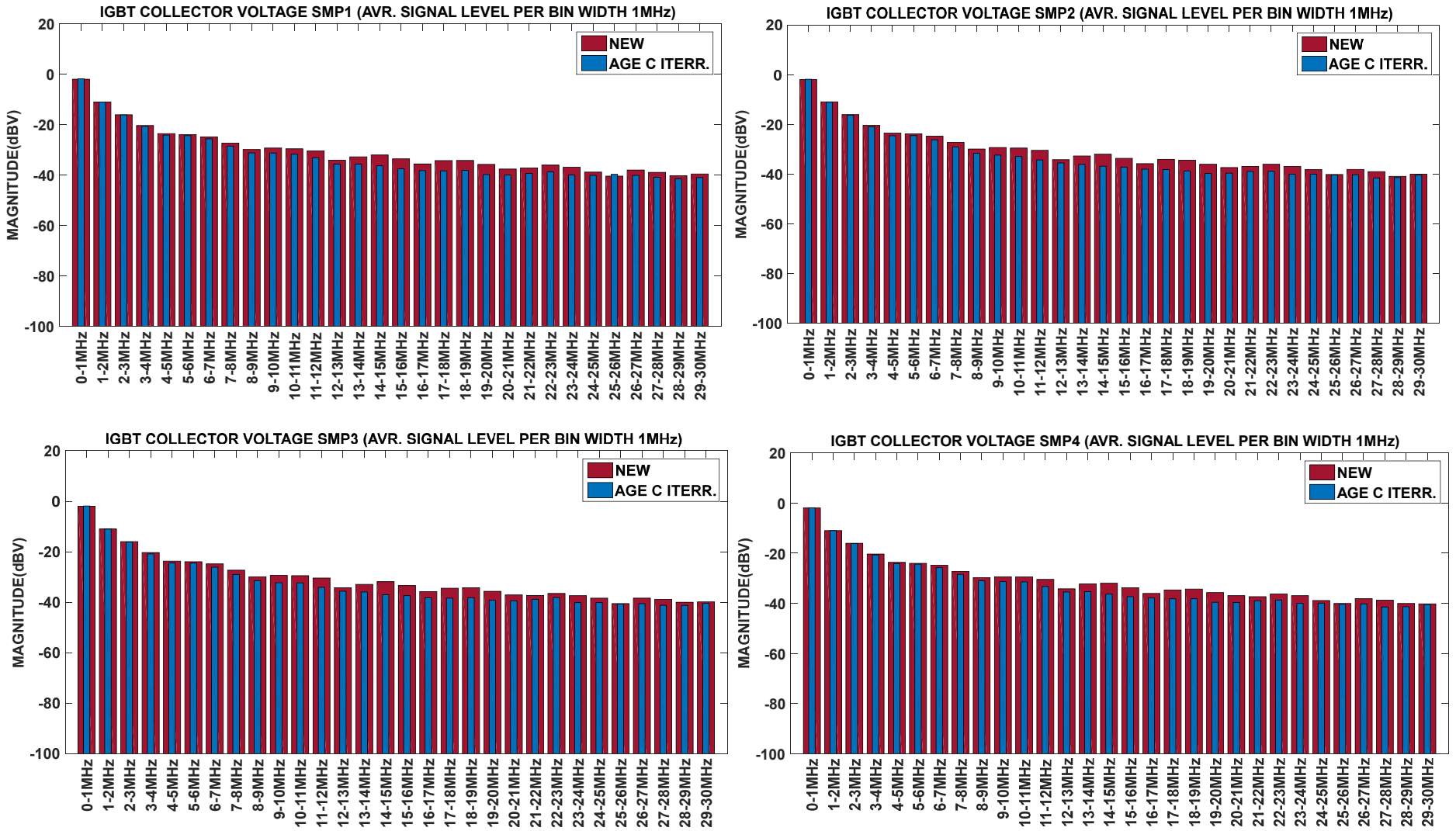


Figure 6.20 - IGBT Samples 1-4, Collector Voltage (V_C) FFT, Average Magnitude Level for every 1MHz bandwidth bin.

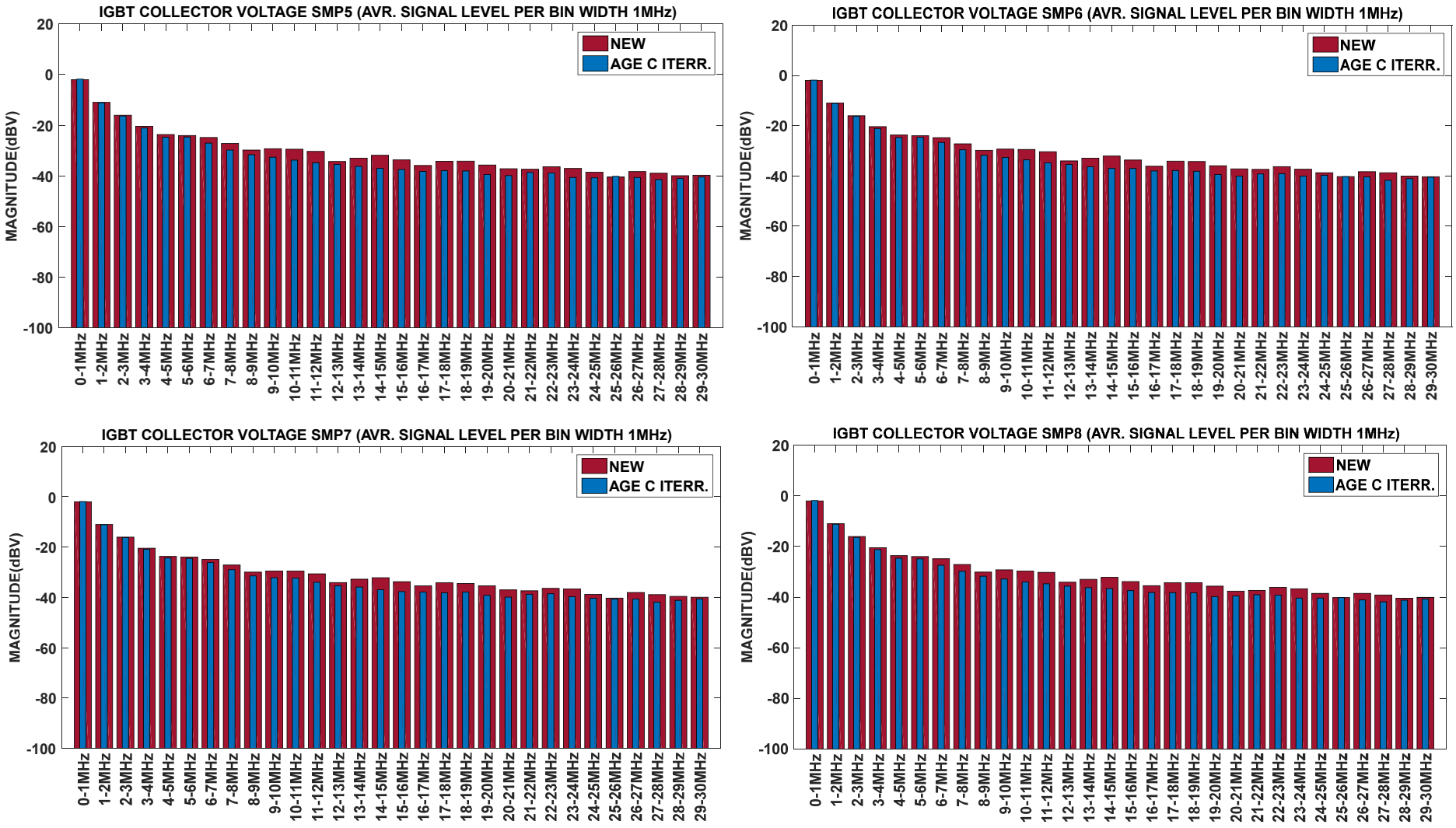


Figure 6.21 - IGBT Samples 5-8, Collector Voltage (V_C) FFT, Average Magnitude Level for every 1MHz bandwidth bin.

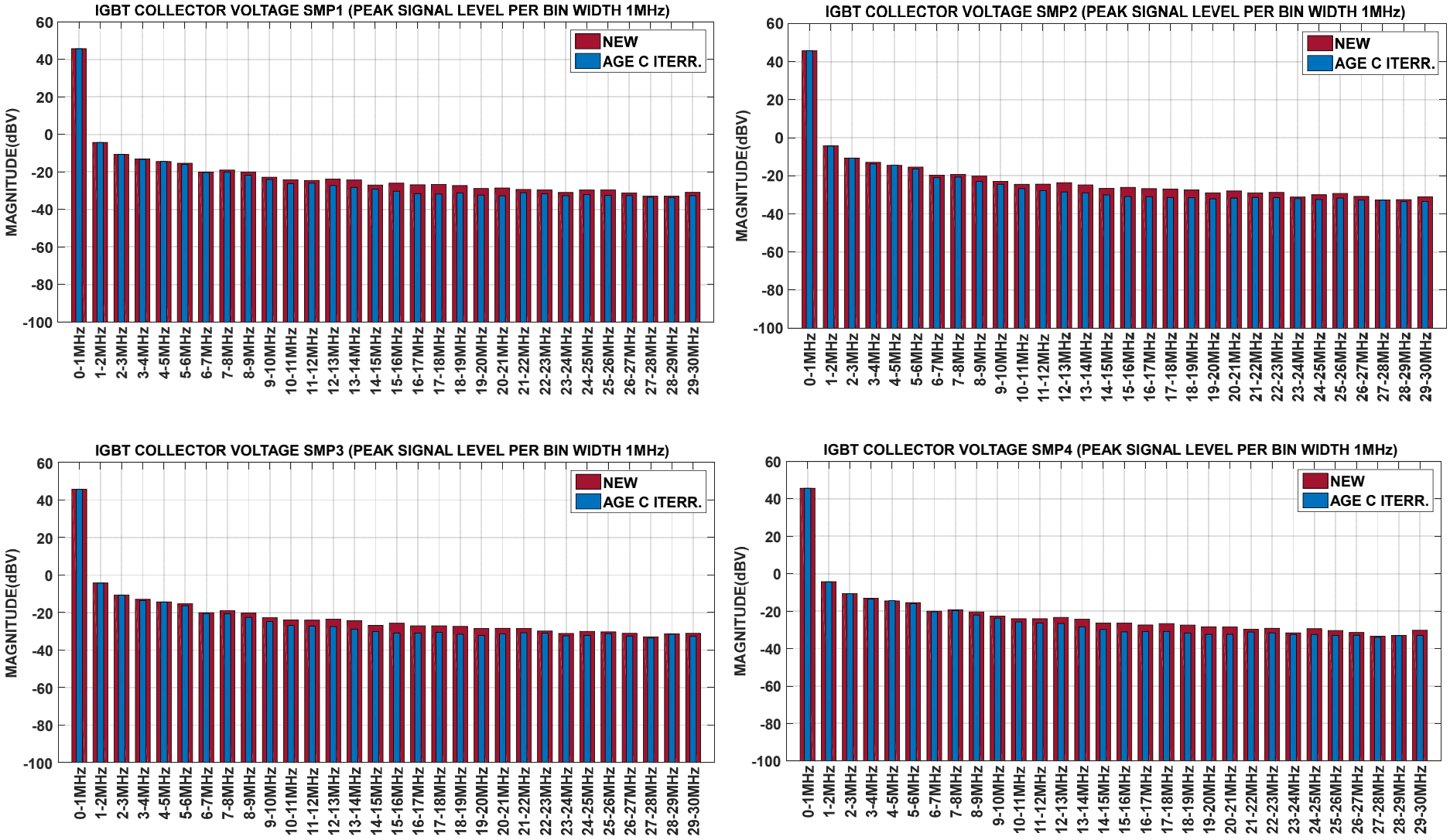


Figure 6.22 - IGBT Samples 1-4, Collector Voltage (V_C) FFT, Maximum Magnitude Level for every 1MHz bandwidth bin.

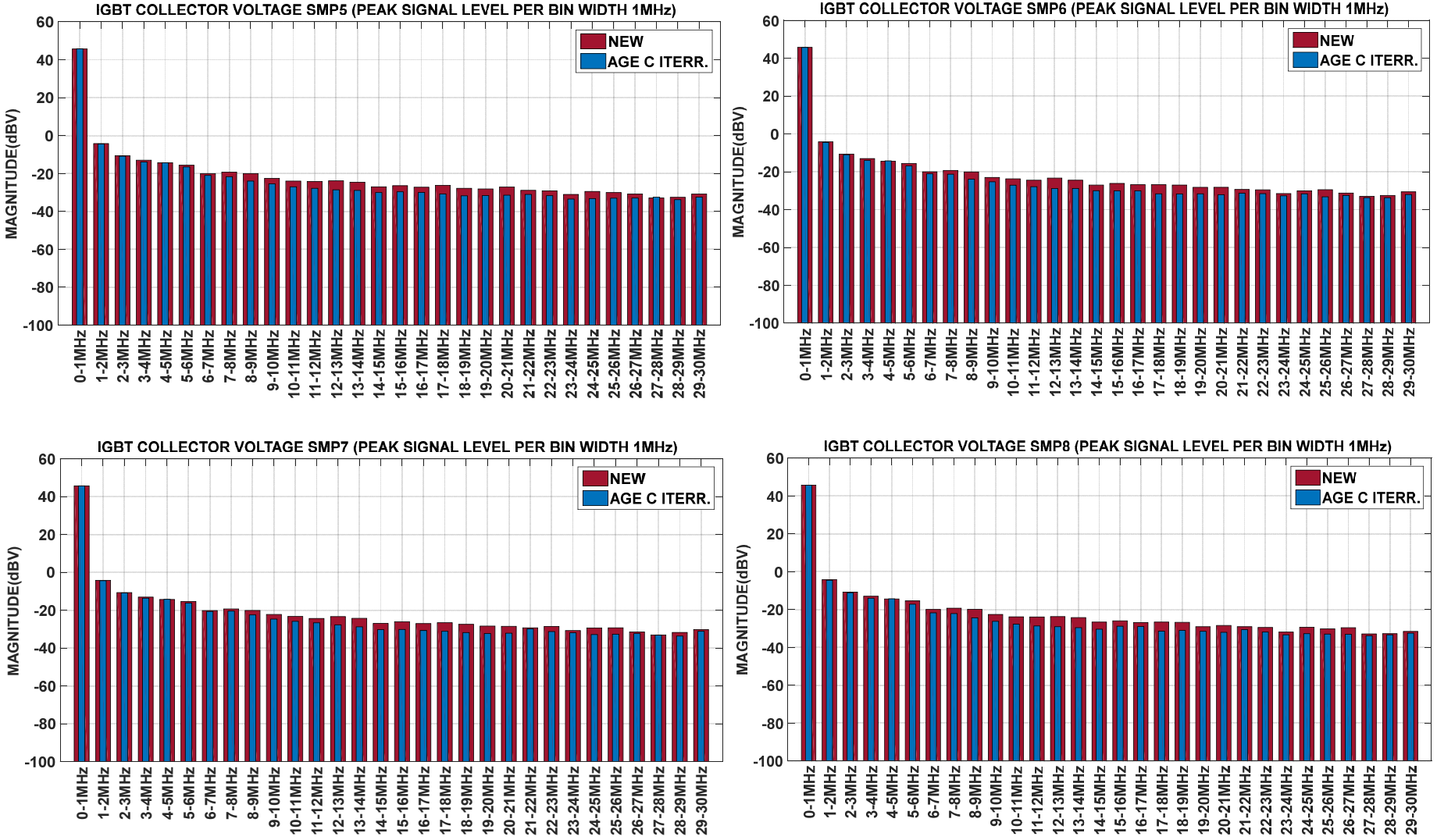


Figure 6.23 - IGBT Samples 5-8, Collector Voltage (V_C) FFT, Maximum Magnitude Level for every 1MHz bandwidth bin.

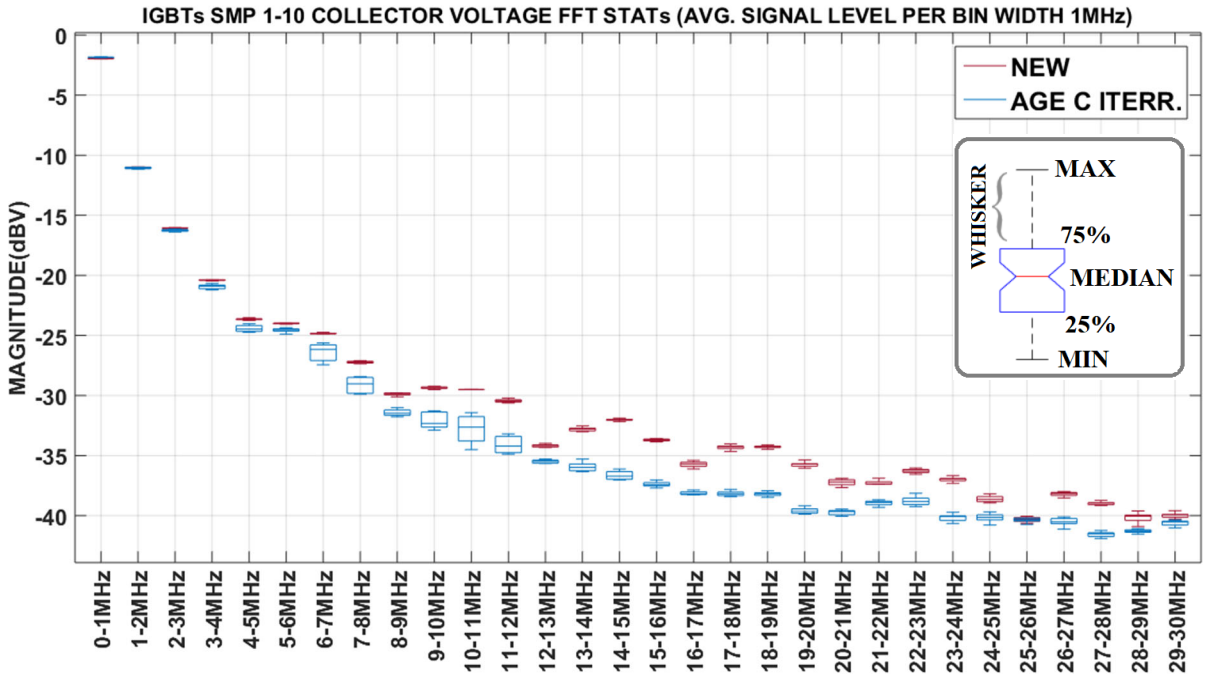


Figure 6.24 - Combined Statistics of IGBTs Samples 1-10, Collector Voltage (V_C) FFT, Average Magnitude Level for every 1MHz bandwidth bin.

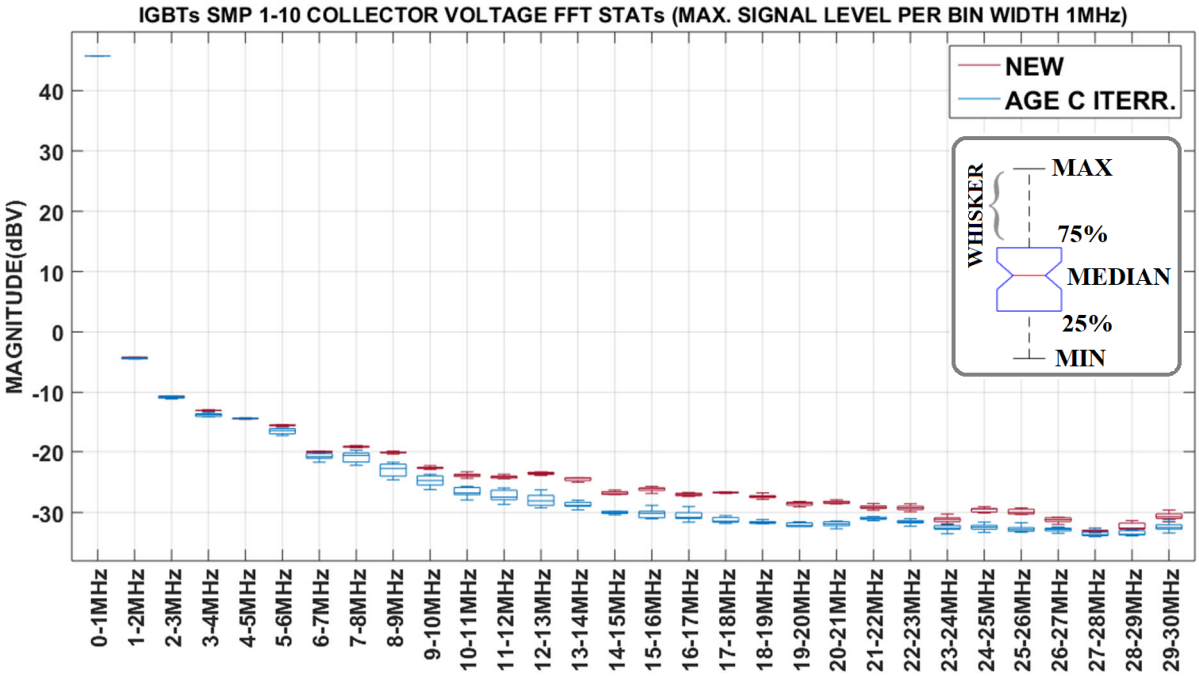


Figure 6.25 - Combined Statistics of IGBTs Samples 1-10, Collector Voltage (V_C) FFT, Maximum Magnitude Level for every 1MHz bandwidth bin.

6.4.2 Collector Current (I_C) Fast Fourier Transform (FFT) Evolution with Ageing

Figure 6.26 provides the obtained collector current (I_C) FFT spectrum of IGBT Sample 5, when the IGBT was new and after each age iteration, again obtaining the predominant spectral peaks and the corresponding polynomial best fit curves. Figure 6.27(i-iii) provides the comparison of the collector current (I_C) FFT spectra, when new and after each age iteration, evidencing too for this transient, a generic decrease in the magnitude of the frequency peaks. Figure 6.27(iv), provides the superposition of the detected frequency peaks fitted curves for IGBT Sample 5, again evidencing that the monitored decrease in the spectral peaks magnitude, is progressive. Figure 6.30 and Figure 6.31 illustrate the evolution of the detected frequency peaks fitted curves, of eight of the ten IGBT samples characterized, which demonstrate that this decrease is progressive, predominantly manifesting in the frequency range of 3MHz to 23MHz. On the other side, one can notice that there was a general magnitude increase of the spectral minima in the frequency range of 3MHz to 12MHz. This is evidenced in Figure 6.28 and Figure 6.29.

This shows that even though for the collector-current (I_C), there was a general, spectral peaks' magnitude decrease, other frequencies experienced an increase in magnitude. This is further substantiated by Figure 6.32 and Figure 6.33, which illustrate the respective post-processing of the average spectral magnitude, and Figure 6.34 and Figure 6.35, which illustrate the maximum spectral magnitude of the collector current (I_C), for every 1MHz frequency bin, as post-processed from the corresponding detailed frequency spectra, illustrated in Figure 6.28 and Figure 6.29.

The corresponding statistics of the maximum spectral magnitude data, as illustrated in Figure 6.34 and Figure 6.35, were summarized by the combined box and whisker plot provided by Figure 6.37. One can notice that there was a decrease in the maximum spectral magnitude of the collector current (I_C), across the 2MHz to 20MHz bandwidth. The largest mean, maximum collector current (I_C) spectral magnitude decrease, occurred in the frequency bin of 4MHz-5MHz, with a corresponding mean percentage decrease in relation to the mean maximum magnitude value when the IGBTs were new of 7.71%.

For frequencies greater than 20MHz, one can still notice a decrease in the maximum spectral content, of the collector current (I_C), even though the measured spectral magnitude within this bandwidth lies in the vicinity of the noise floor level. Figure 6.36 provides the summarized statistics of the average spectral magnitude, of the collector current (I_C), for every 1MHz frequency bin. This latter plot shows that after ageing, there was a general decrease in the

collector current (I_C) average spectral magnitude across the 2MHz to 20MHz bandwidth, with the largest mean, average collector current (I_C), spectral magnitude decrease, occurring in the frequency bin of 1MHz-2MHz, with a corresponding mean percentage decrease of 7.62%. On the other side four frequency bins (3-4MHz, 7-8MHz, 8-9MHz and 12-13MHz), manifested a mean percentage increase in the average magnitude, of 3.66%, 0.43%, 1.28% and 0.03%, respectively.

The above observations are substantiating the observations explained in Chapter 4 and Chapter 5, where after the IGBTs were subjected to the implemented accelerated ageing, a slow-down in the collector-voltage (V_C) and collector-current (I_C) turn-off transients were measured to the contrary of the turn-on transients where minimal changes were observed. The arguments put forward in Chapter 5 proposed that the measured slow-down of the turn-off was primarily caused by an enhanced junction temperature (T_J) even if the case temperature (T_C) was maintained at room temperature (25°C). This was due to the degradation of the die-attach, which contributed to an increase in the junction-to-case thermal impedance (θ_{JC}). This primarily affected the enhanced presence of the "tail current" accentuating the slow-down of the collector current (I_C) turn-off transient. Indirectly this increase in the junction temperature (T_J) contributed to changes in the IGBT's parasitic devices which in-turn contributed to the further slow-down of the IGBTs' turn-off transients. Hence, this slow-down impacted the spectral magnitude of the higher frequencies, contributing to the observed IGBTs' general decrease in the magnitude of the higher frequencies' spectral peaks, after being subjected to the implemented accelerated ageing. This was valid for both the collector voltage (V_C) and the collector current (I_C) transients, as both transients were experiencing a slow-down during turn-off. In contrast, only the collector current (I_C) manifested an increase in the average spectral magnitude (i.e. the four frequency bands listed earlier), with the collector voltage (V_C), manifesting no increase. This can be explained as the slowdown in the collector current (I_C) transient was more severe when compared with collector-voltage (V_C) transient. Moreover, this corroborates what has been noticed in Chapter 4 and Chapter 5, where it was showed that the turn-off switching energy increased due to the implemented accelerated ageing, predominantly due to the collector current (I_C) enhanced presence of the "tail-current", hence reflecting the increase, in the collector current (I_C) average spectral magnitude, in the four aforementioned frequency bands.

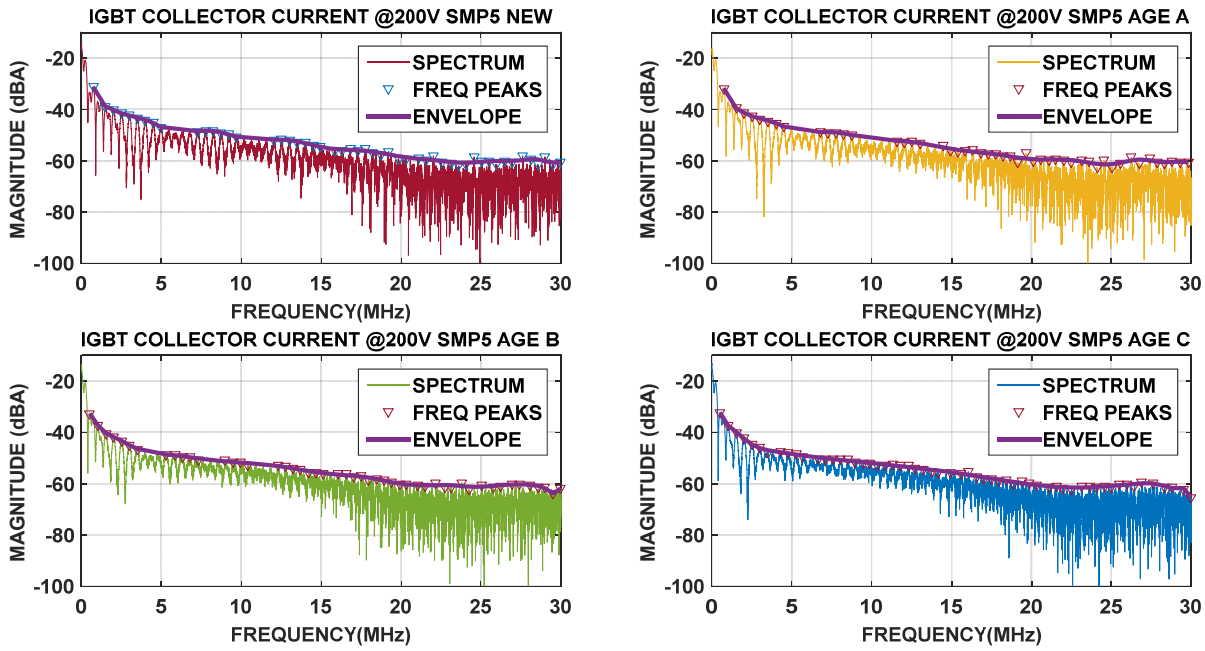


Figure 6.26 - IGBT Sample 5 Collector Current (I_C) FFT, Frequency Peaks, and corresponding Peaks Envelopes (i) New (ii) Age Iteration A (iii) Age Iteration B (iv) Age Iteration C.

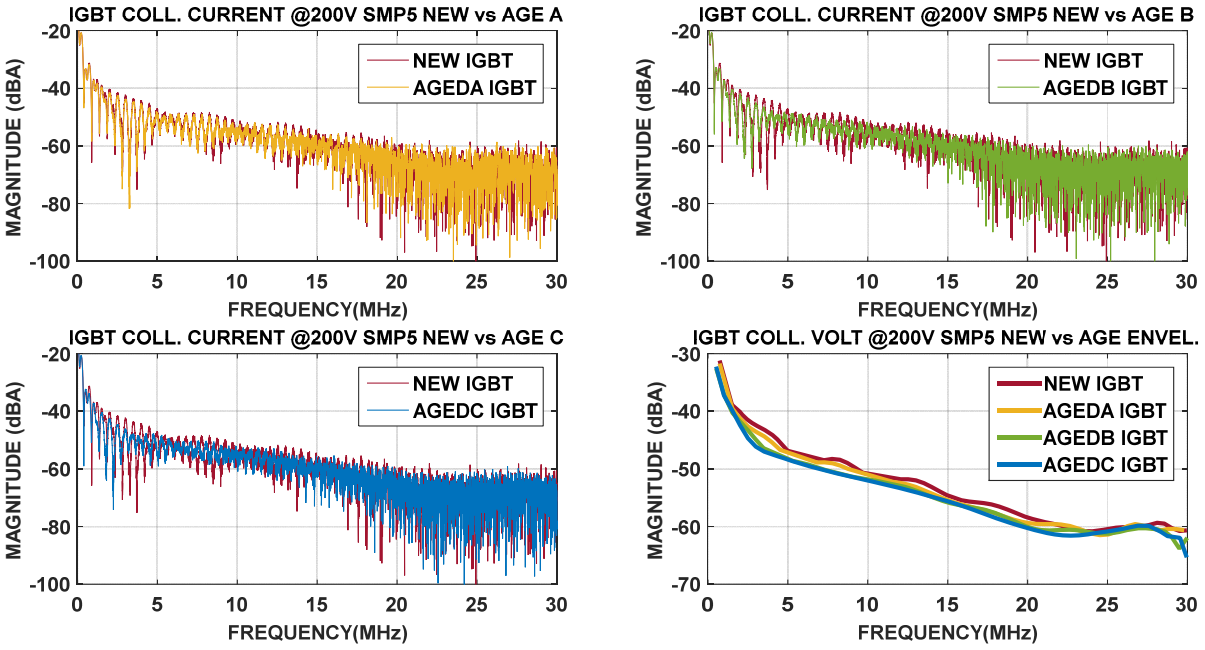


Figure 6.27 - IGBT Sample 5 Collector Voltage (V_C) FFT (i) New vs Age Iteration A (ii) New vs Age Iteration B (iii) New vs Age Iteration C (iv) Comparison of All Iterations Frequency Peaks Envelopes.

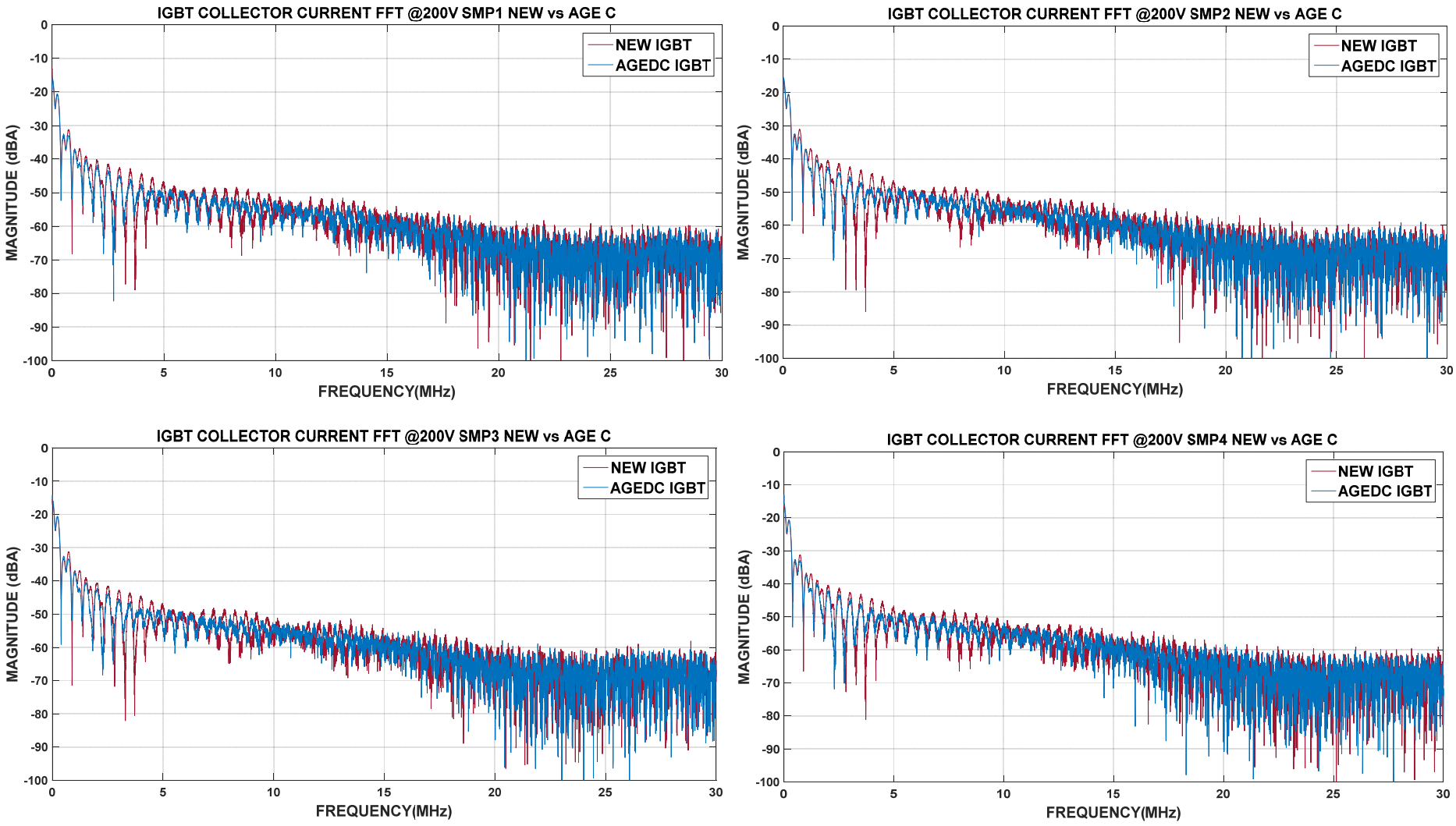


Figure 6.28 - IGBT Samples 1 to 4, Collector Current (I_C) FFT, New vs Age Iteration C.

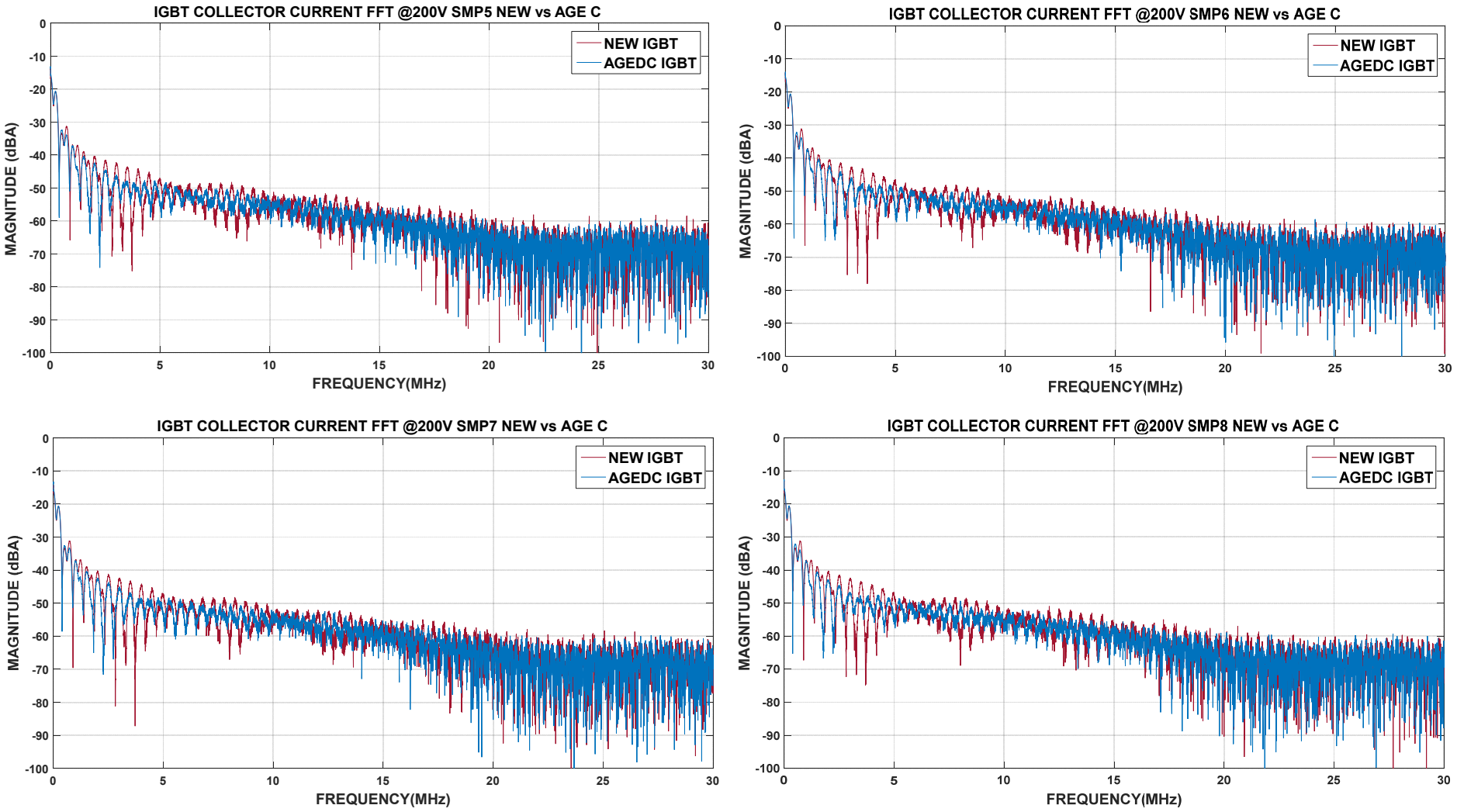


Figure 6.29 - IGBT Samples 5 to 8, Collector Current (I_C) FFT, New vs Age Iteration C.

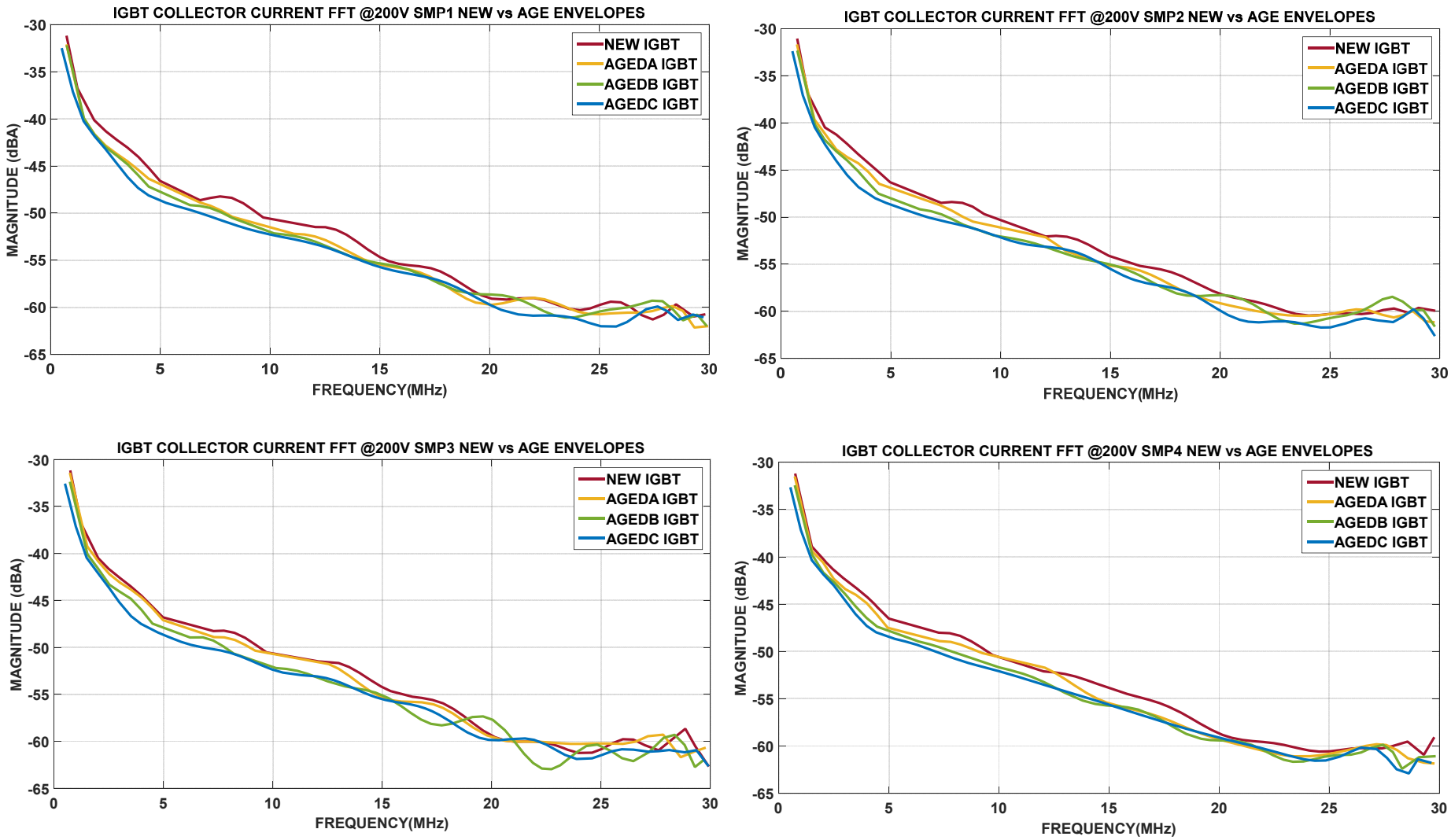


Figure 6.30 - IGBT Samples 1 to 4, Collector Current (I_C) FFT, Frequency Peaks Envelopes.

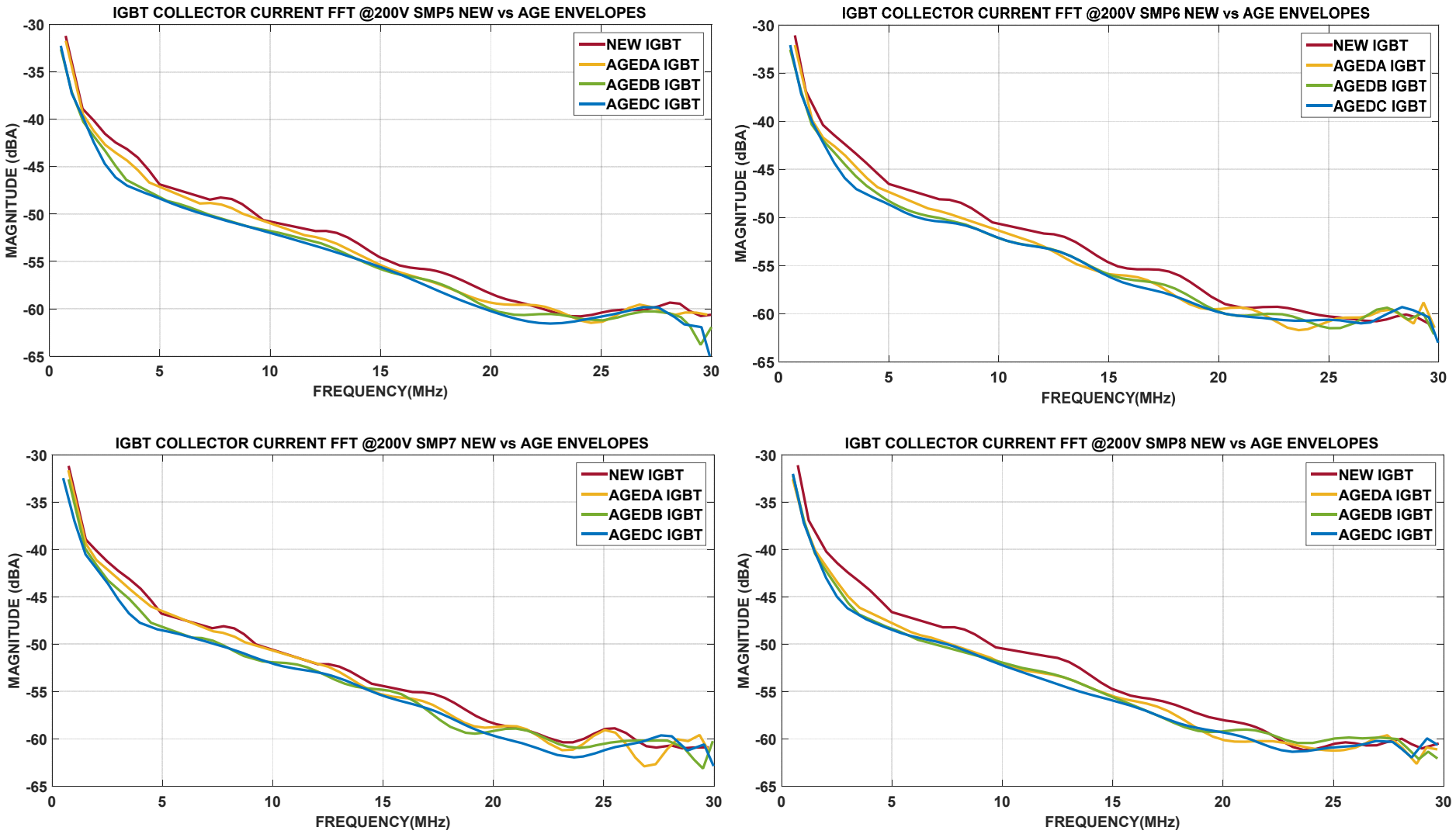


Figure 6.31 - IGBT Samples 5 to 8, Collector Current (I_C) FFT, Frequency Peaks Envelopes.

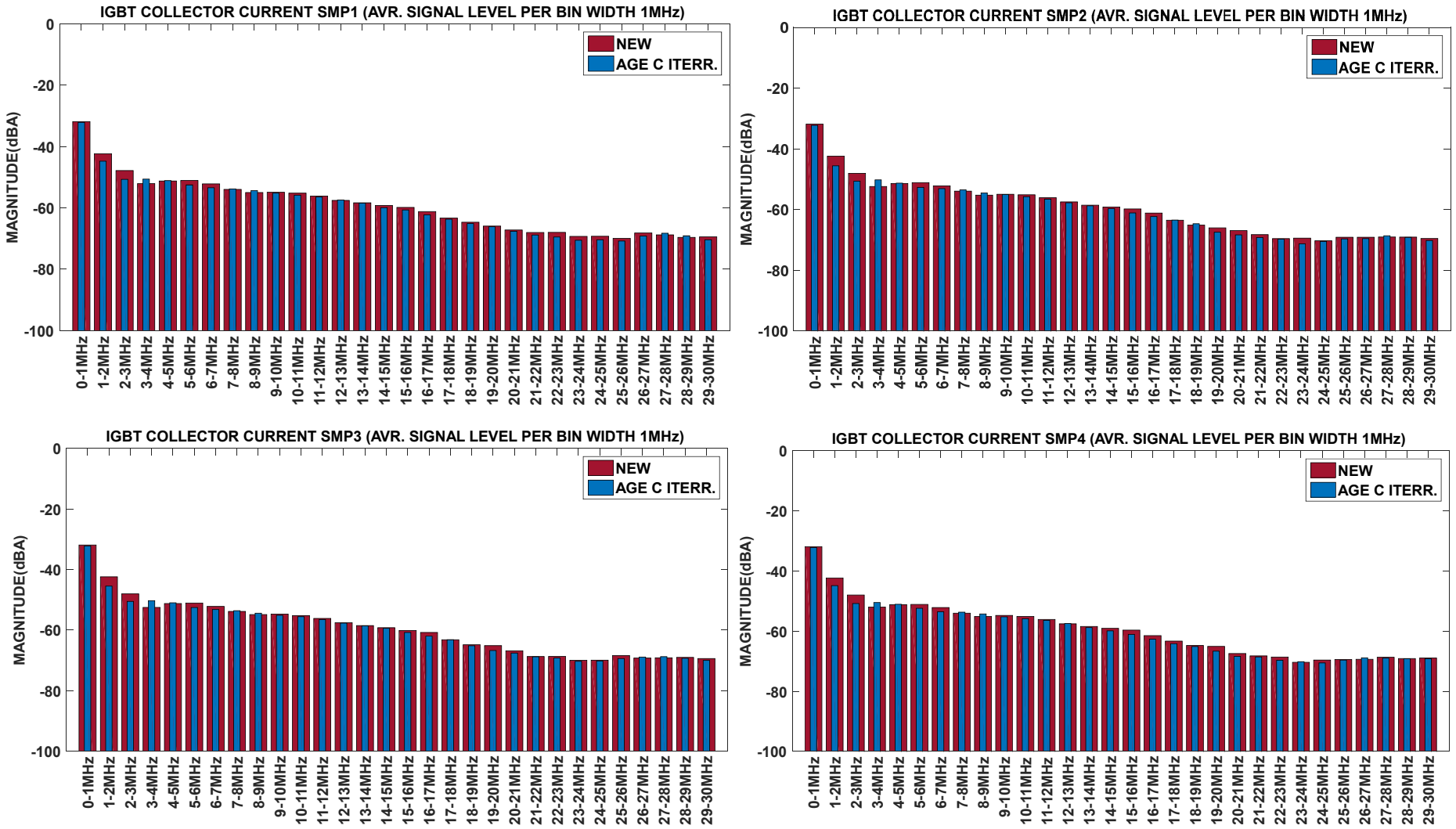


Figure 6.32 - IGBT Samples 1-4, Collector Current (I_C) FFT, Average Magnitude Level for every 1MHz bandwidth bin.

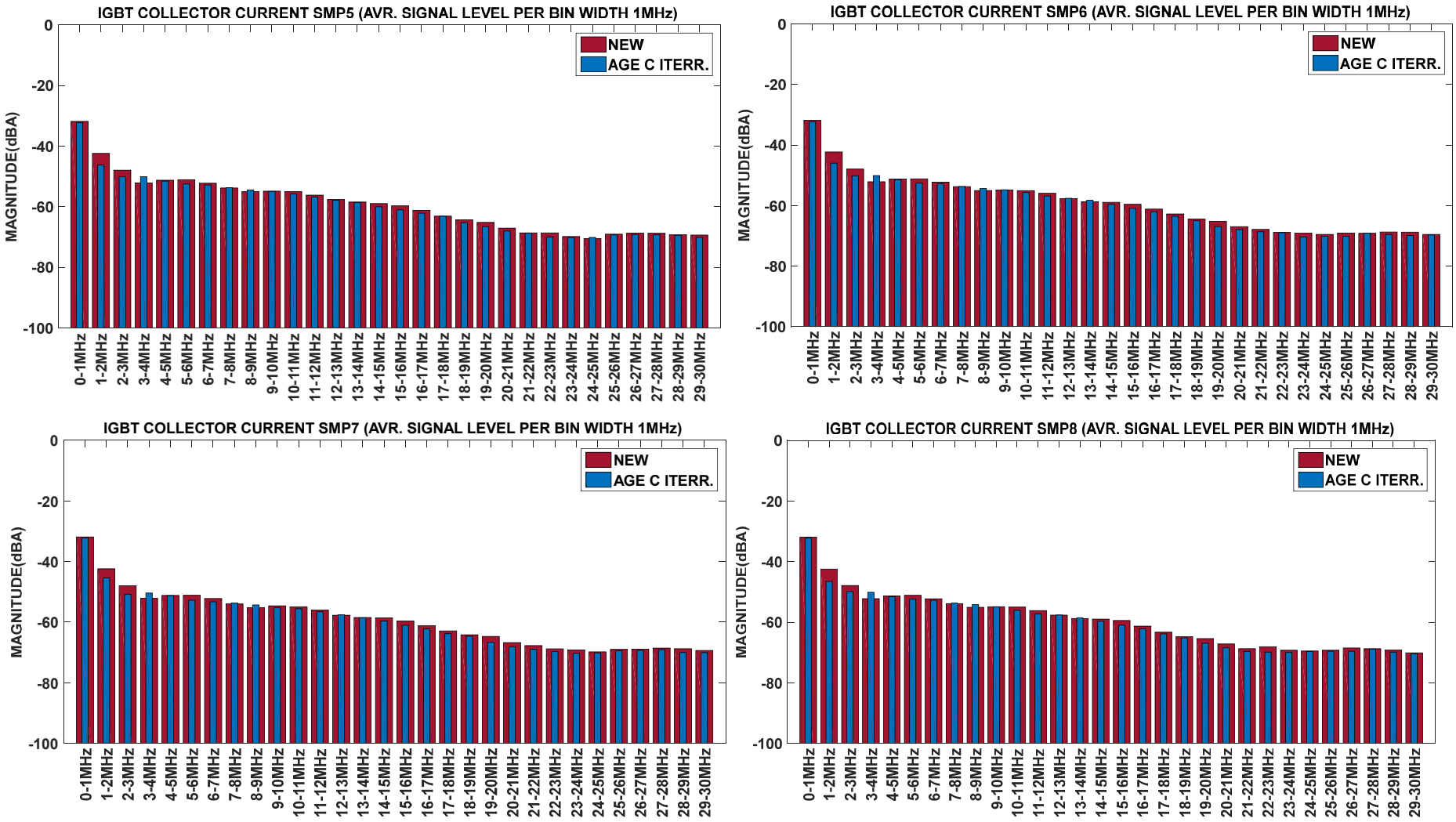


Figure 6.33 - IGBT Samples 5-8, Collector Current (I_C) FFT, Average Magnitude Level for every 1MHz bandwidth bin.

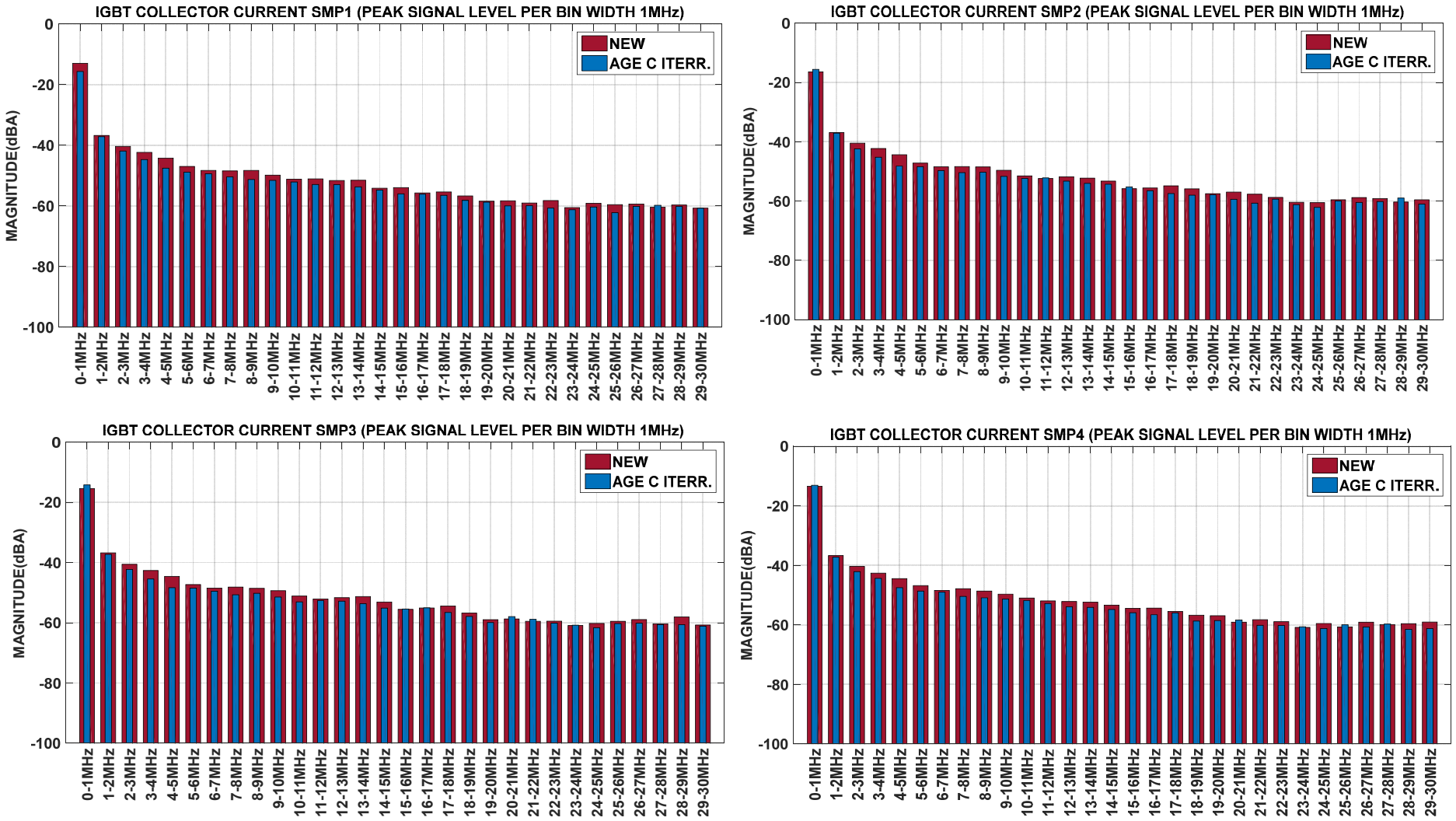


Figure 6.34 - IGBT Samples 1-4, Collector Current (I_C) FFT, Maximum Magnitude Level for every 1MHz bandwidth bin.

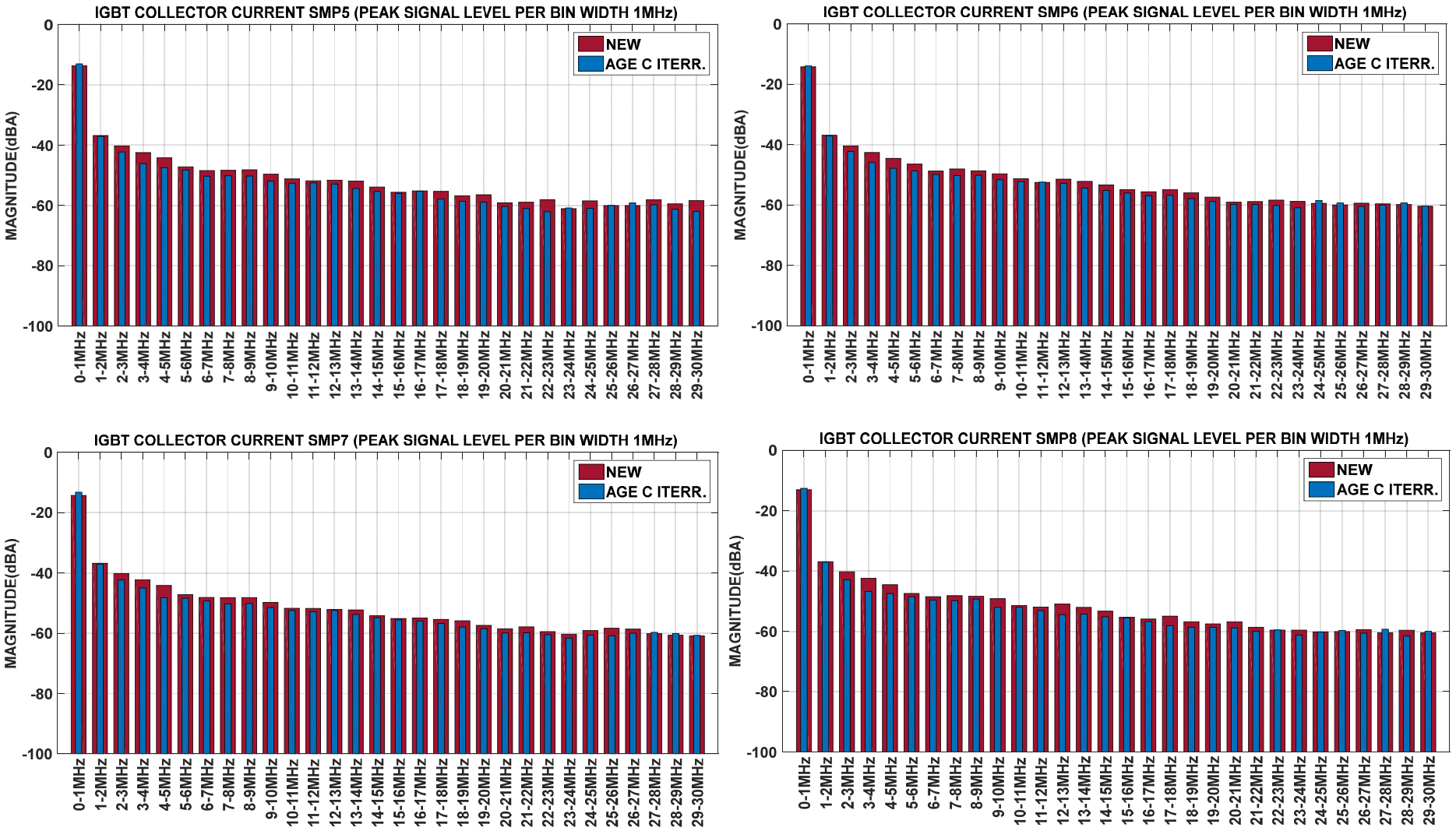


Figure 6.35 - IGBT Samples 5-8, Collector Current (I_C) FFT, Maximum Magnitude Level for every 1MHz bandwidth bin.

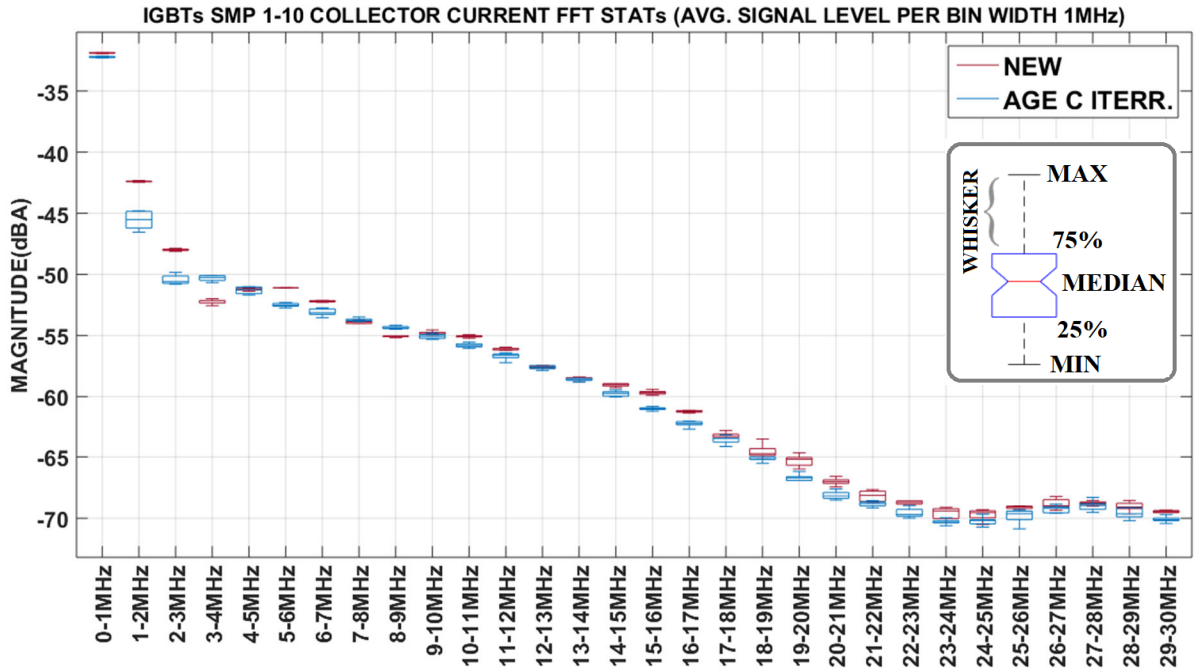


Figure 6.36 - Combined Statistics of IGBTs Samples 1-10, Collector Current (I_C) FFT, Average Magnitude Level for every 1MHz bandwidth bin.

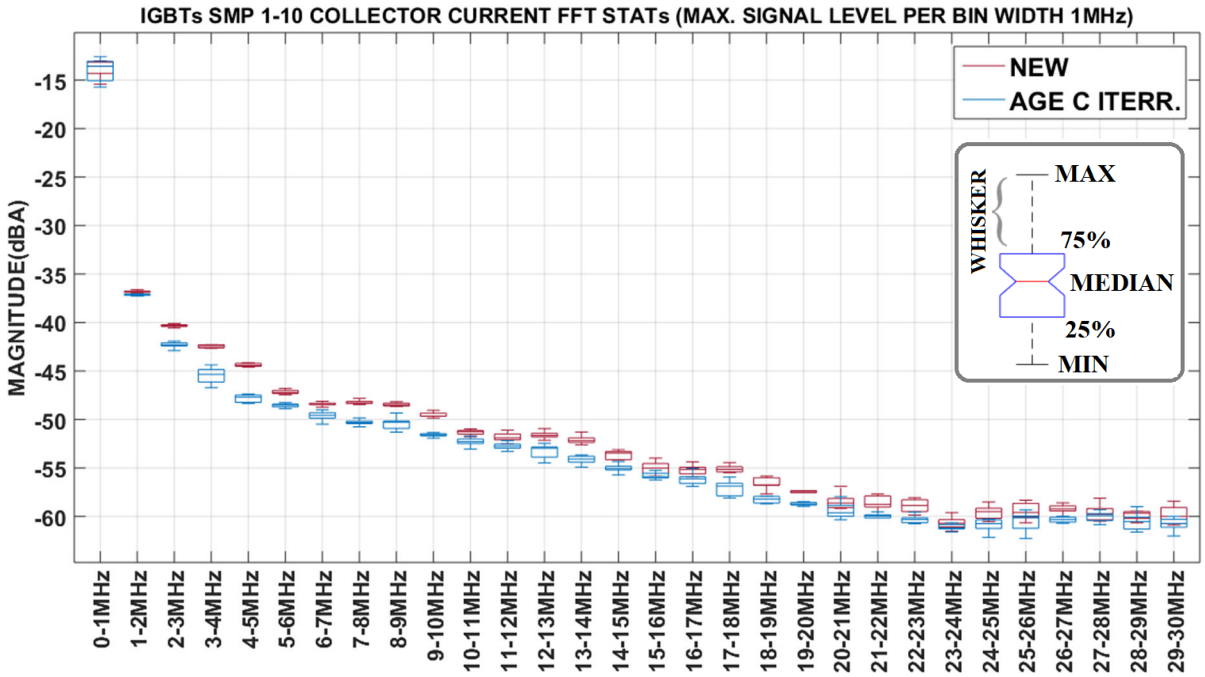


Figure 6.37 - Combined Statistics of IGBTs Samples 1-10, Collector Current (I_C) FFT, Maximum Magnitude Level for every 1MHz bandwidth bin.

6.4.1 EM Conducted Emissions Evolution with Ageing Results

A similar spectral analysis, conducted to assess the collector voltage (V_C) and collector current (I_C) frequency domain evolution with ageing, was performed for the EM conducted emissions spectra, for both the forward line (L_1) and the return line (L_2), obtained during the IGBTs' characterization with ageing. Figure 6.38(i-iv) provides the obtained conducted emissions spectra (for the CISPR16-1-1 A and B bands 9kHz-30MHz) for the forward line (L_1) of IGBT Sample 2, when the IGBT was new and after each age iteration, again obtaining the predominant spectral peaks and the corresponding polynomial best fit curves. Similarly, Figure 6.50(i-iv) provides the same plots but for the return line (L_2), for IGBT Sample 3. Correspondingly, Figure 6.39(i-iii) and Figure 6.51(i-iii) provides the comparison of the conducted emissions, obtained after each age iteration with the conducted emission obtained when the IGBT was new, for IGBT Sample 2 on the forward line (L_1) and IGBT Sample 3 on the return line (L_2), respectively. Both plots indicate that there was a general decrease in the power level of the conducted emissions' spectral peaks. Figure 6.39(iv) and Figure 6.51(iv) provide the superposition of the detected spectral peaks fitted curves, for the conducted emissions of IGBT Sample 2 on the forward line (L_1) and IGBT Sample 3 on the return line (L_2) respectively, indicating that in both cases, the monitored decrease is progressive with each age iteration.

This is furthermore substantiated by Figure 6.42 and Figure 6.43 which present the superposition of the detected spectral peaks fitted curves, of the conducted emissions on the forward line (L_1), while Figure 6.54 and Figure 6.55 provide the same plots but with the conducted emissions on the return line (L_2). These plots, which represent eight of the ten IGBTs characterized during this test phase, demonstrate that the monitored decrease in the conducted emissions' peaks, is progressive, manifesting essentially over the entire bandwidth of interest on both the forward line (L_1) and return line (L_2). By inspecting Figure 6.40 and Figure 6.41 for the conducted emissions on the forward line (L_1) and Figure 6.52 and Figure 6.53 for the conducted emissions on the return line (L_2), one can notice, that by the end of the implemented accelerated ageing procedure, there was an evident decrease in the 3MHz to 15MHz frequency range for the forward line (L_1), and in the 2MHz to 20MHz frequency range for the return line (L_2). On the other side, one can observe too, that there was a general increase of the spectral minima in these frequency ranges, indicating that apart from the monitored decreases in the spectral peaks, the implemented accelerated ageing was also contributing, to increases in the conducted emissions power level of certain frequencies.

The above observation was analyzed further, by utilizing the approach employed for the FFT analysis, of comparing the changes in the conducted emissions spectra before and after the implemented accelerated ageing procedure, by computing the average magnitude and maximum magnitude, for each 1MHz frequency bin. The average magnitude plots, of the conducted emissions on the forward line (L_1), of eight out of the ten IGBTs, are provided in Figure 6.44 and Figure 6.45. On the other side, Figure 6.56 and Figure 6.57 provide the same analysis but for the conducted emissions on the return line (L_2). The maximum magnitude 1MHz frequency bin plots, are provided in Figure 6.46 and Figure 6.47, for the conducted emissions on the forward line (L_1) and in Figure 6.58 and Figure 6.59 for the conducted emissions on the return line (L_2). Again, the data for the above plots was combined in box and whiskers plots, with the average magnitude analysis provided in Figure 6.48 and Figure 6.60 for the forward line (L_1) and return line (L_2) respectively, while the maximum magnitude analysis is provided in Figure 6.49 and Figure 6.61 for the conducted emissions on the forward line (L_1) and return line (L_2) respectively.

When comparing the data across the different IGBT samples, one can infer that the conducted emissions measurements obtained through the return line (L_2) were more repeatable when compared to the data obtained through the forward line (L_1). This was substantiated by inspecting the various IGBT samples' conducted emissions plots, as provided in Figure 6.40 and Figure 6.41, for the conducted emissions on the forward line (L_1), and Figure 6.52 and Figure 6.53 for the conducted emissions on the return line (L_2). One can notice that these latter plots exhibit more consistency and repeatability when compared to the forward line (L_1) plots. This is furthermore confirmed by the obtained box and whiskers plots. The forward line (L_1) data (especially the data set of the aged IGBTs), as provided in Figure 6.48 and Figure 6.49, is by enlarge demonstrating less concentration about the median of each frequency bin, manifesting larger interquartile ranges (box range). Moreover, this data is by enlarge displaying positive skewness for the different frequency bins (with the upper half-box longer of the median), translating to an asymmetric data distribution with the median being different (greater) than the mean. This is especially true for frequencies smaller than 20MHz (for frequencies larger than 20MHz the measured conducted emissions are close to the noise floor, hence measured changes will become more unreliable to attribute exclusively to the implemented accelerated ageing). In contrast the return line (L_2) data, is manifesting more concentration about the median, displaying smaller interquartile ranges, while exhibiting a relatively symmetric lower and upper half-boxes indicating that this data is manifesting a more

symmetric data distribution. Again, this is especially true for conducted emissions frequencies smaller than 20MHz. Having ensured the same level of experimental rigor, it is not clear if this repeatability inconsistency for the forward line (L_1) conducted emission measurements, is due to some experimental measurement error, or it is just reflecting the actual measurement. Even so, the maximum magnitude analysis, conducted for both the forward line (L_1) and return line (L_2), as provided in Figure 6.49 and Figure 6.61 respectively, clearly confirms that there was a general decrease in the conducted emissions spectral peaks due to the implemented accelerated ageing procedure. This decrease is predominantly manifested in the frequency range of 1MHz to 21MHz for the conducted emissions measurements on the forward line (L_1) and in the frequency range of 1 to 20MHz for the conducted emissions measurements on the return line (L_2), with the largest mean decrease manifesting for the forward line (L_1), in the frequency bin of 12MHz-13MHz, with a percentage decrease of 6.45%, and in the return line (L_2), in the frequency bin of 18MHz-19MHz, with a percentage decrease of 5.47%.

This result reflects the monitored changes in the collector voltage (V_C) and collector current (I_C) transients, which both manifested a slow-down in the turn-off transients as evidenced in Chapter 4 and Chapter 5. Moreover, the above result reflects the results obtained from the FFT analysis in Section 6.4.1 and Section 6.4.2, where it was shown that the collector voltage (V_C) and the collector current (I_C) frequency domain spectra, experienced a decrease in the spectral peaks, predominantly for the collector voltage (V_C) in the frequency range of 12MHz to 21MHz, and for the collector current (I_C) in the frequency range of 2MHz to 20MHz. These latter bandwidths (especially the collector current (I_C) bandwidth) match with the conducted emissions bandwidths where the predominant spectral peaks decrease was manifested, for both the forward line (L_1) and return line (L_2).

Since from an EMC/EMI point of view, the measurement of the power level of the conducted emissions spectral peaks is paramount, especially when considering that standards specify limits which must not be surpassed for the EUT to be considered compliant, the above result shows that the implemented accelerated ageing, which predominantly is producing a degradation of the IGBT's die-attach, is influencing a general decrease of the EM conducted emissions spectral peaks, on both the forward (L_1) and return (L_2) lines of measurement, predominantly within the 1MHz to 21MHz bandwidth.

In relation to the conducted emissions, average magnitude analysis, provided in Figure 6.60 (focusing on the data obtained through the return line (L_2), as it was deemed more reliable), one can notice a general decrease after ageing, of the average spectral power, for each 1MHz frequency bin, except for four frequency bins (3-4MHz, 7-8MHz, 8-9MHz and 12-13MHz). These latter bins manifested an increase after the full completion of the accelerated ageing procedure, with a respective mean percentage increase of 2.46%, 0.16%, 2.46% and 1.06%. Even though from Figure 6.48, one can infer the same conclusions, from the conducted emissions measurements obtained through the forward line (L_1) (i.e. an average spectral power increase in the above listed bins), the results provided are less categorical, when compared to the results obtained from the return line (L_2) provided in Figure 6.60.

Another interesting result, is that the frequency bins which manifested an average spectral power increase, correspond to the same four collector current (I_C) frequency bins, which manifested an average spectral magnitude increase, as presented in Figure 6.36. This shows that the measured changes in the EM conducted emissions (at least in the frequency range where the predominant changes are manifesting (1MHz-20MHz)), can be principally attributed to the degradation experienced by the IGBTs, during the implemented accelerated ageing procedure. Thus, the measured increase in the EM conducted emissions average power level, in the aforementioned four frequency bands, in conjunction with the measured general decrease of the EM conducted emission spectral peaks, are clearly reflecting the IGBTs' transients' turn-off slow down and consequently the increased turn-off switching power dissipation, due to the experienced IGBTs' degradation, as there is a direct correspondence between the changes happening in the frequency domain of the IGBTs' signals, and the measured EM conducted emissions.

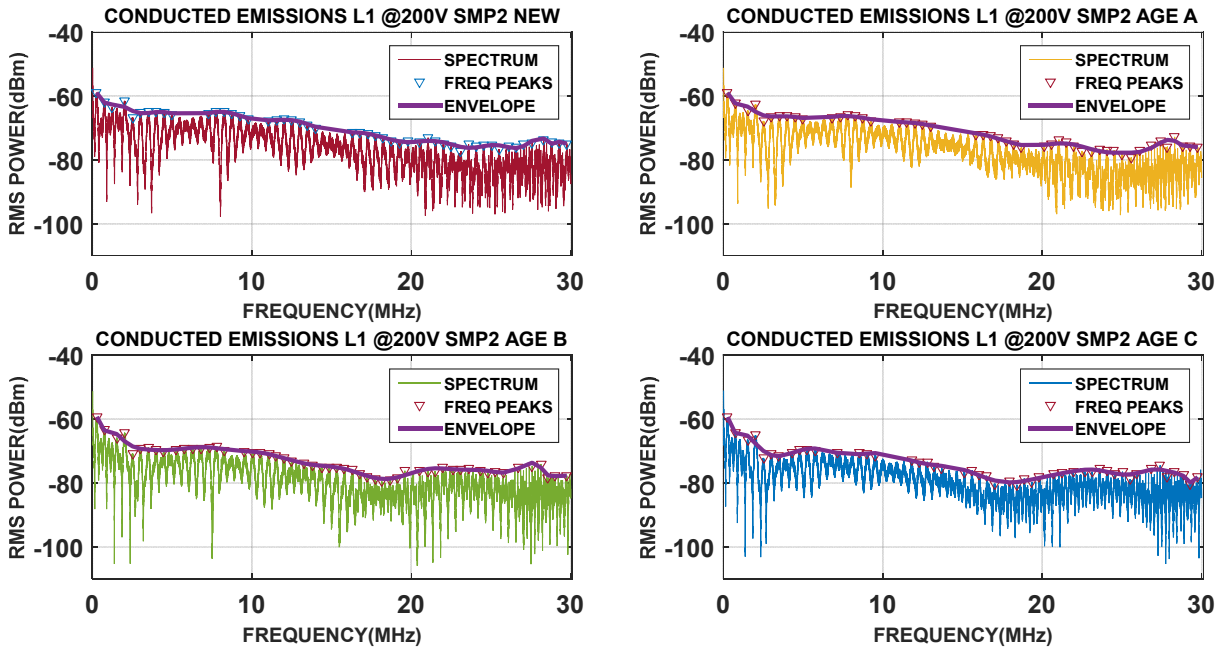


Figure 6.38 – IGBT Sample 2 CISPR16-1-1 A&B Bands, L_1 (Forward Line), Conducted Emissions Spectra, Frequency Peaks, and corresponding Peaks Envelopes (i) New (ii) Age Iteration A (iii) Age Iteration B (iv) Age Iteration C.

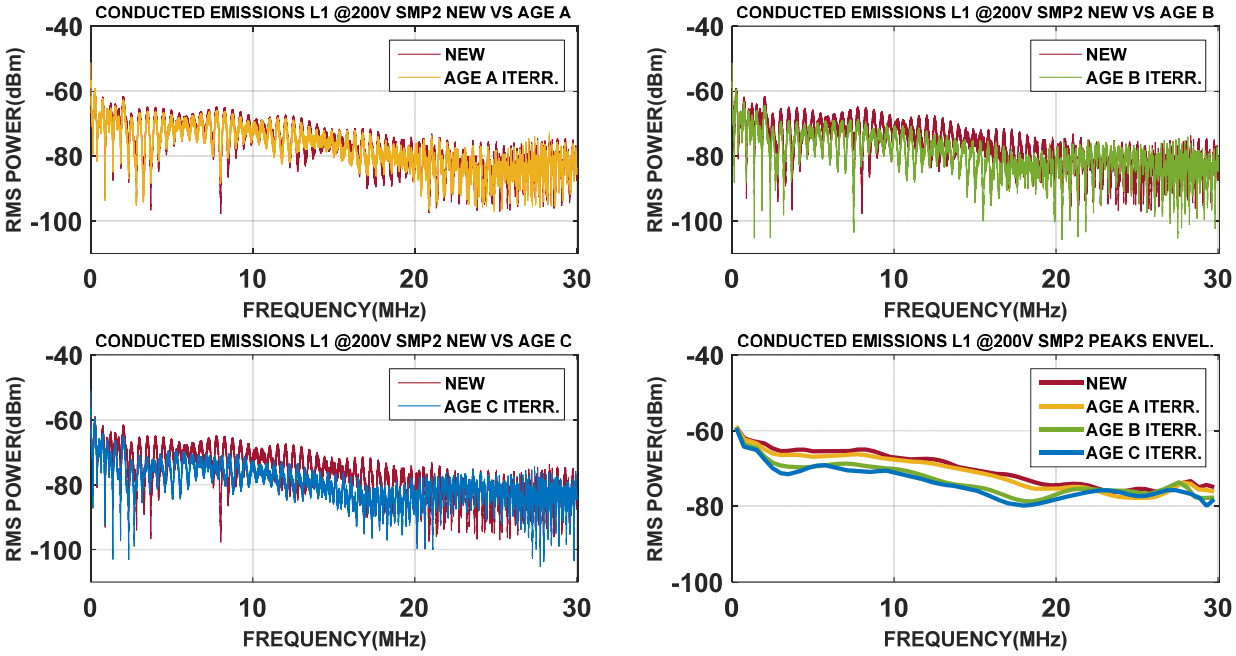


Figure 6.39 - IGBT Sample 2 CISPR16-1-1 A&B Bands, L_1 (Forward Line), Conducted Emissions Spectra (i) New vs Age Iteration A (ii) New vs Age Iteration B (iii) New vs Age Iteration C (iv) Comparison of All Iterations Frequency Peaks Envelopes.

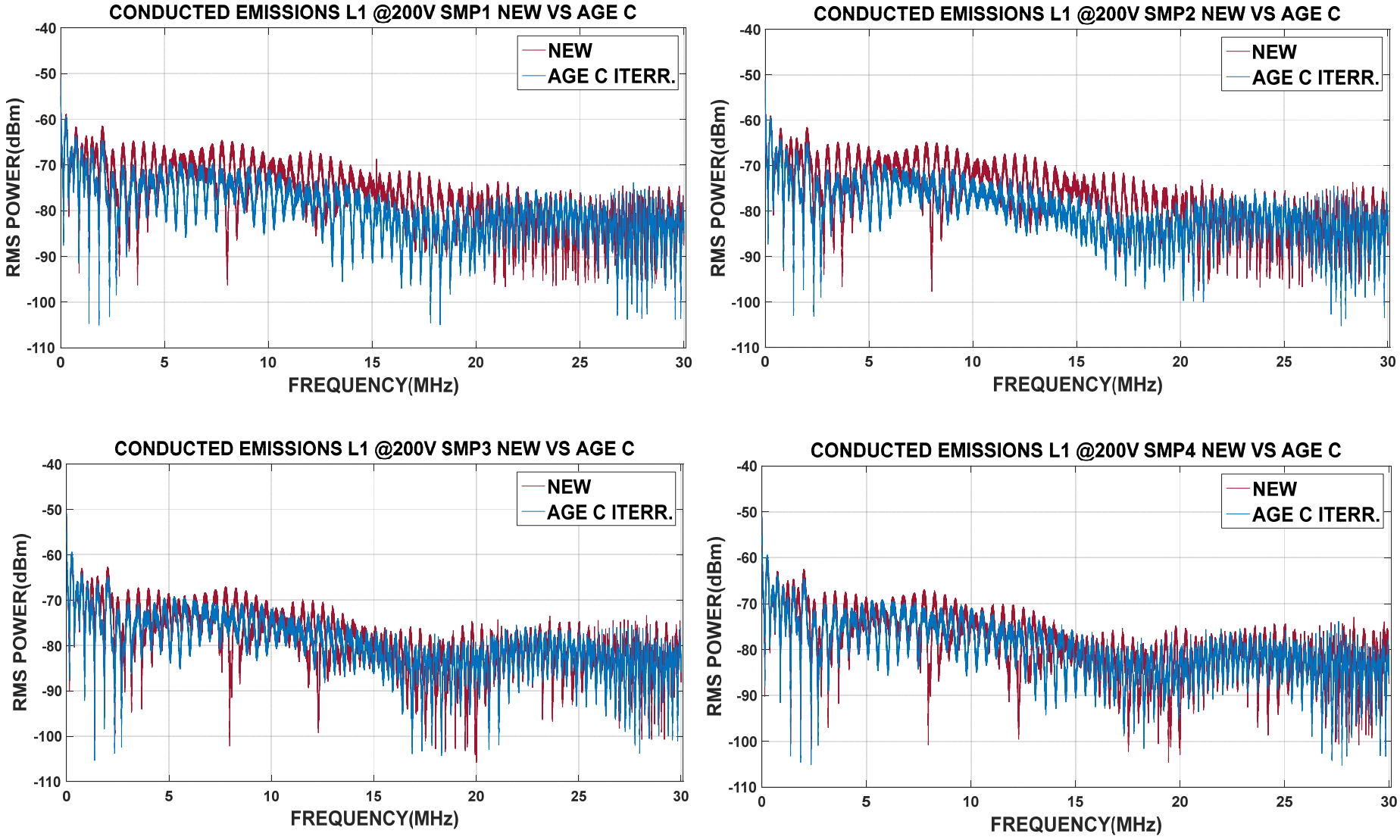


Figure 6.40 - IGBT Samples 1 to 4, CISPR16-1-1 A&B Bands Conducted, L_1 (Forward Line) Conducted Emissions Spectra, New vs Age Iteration C.

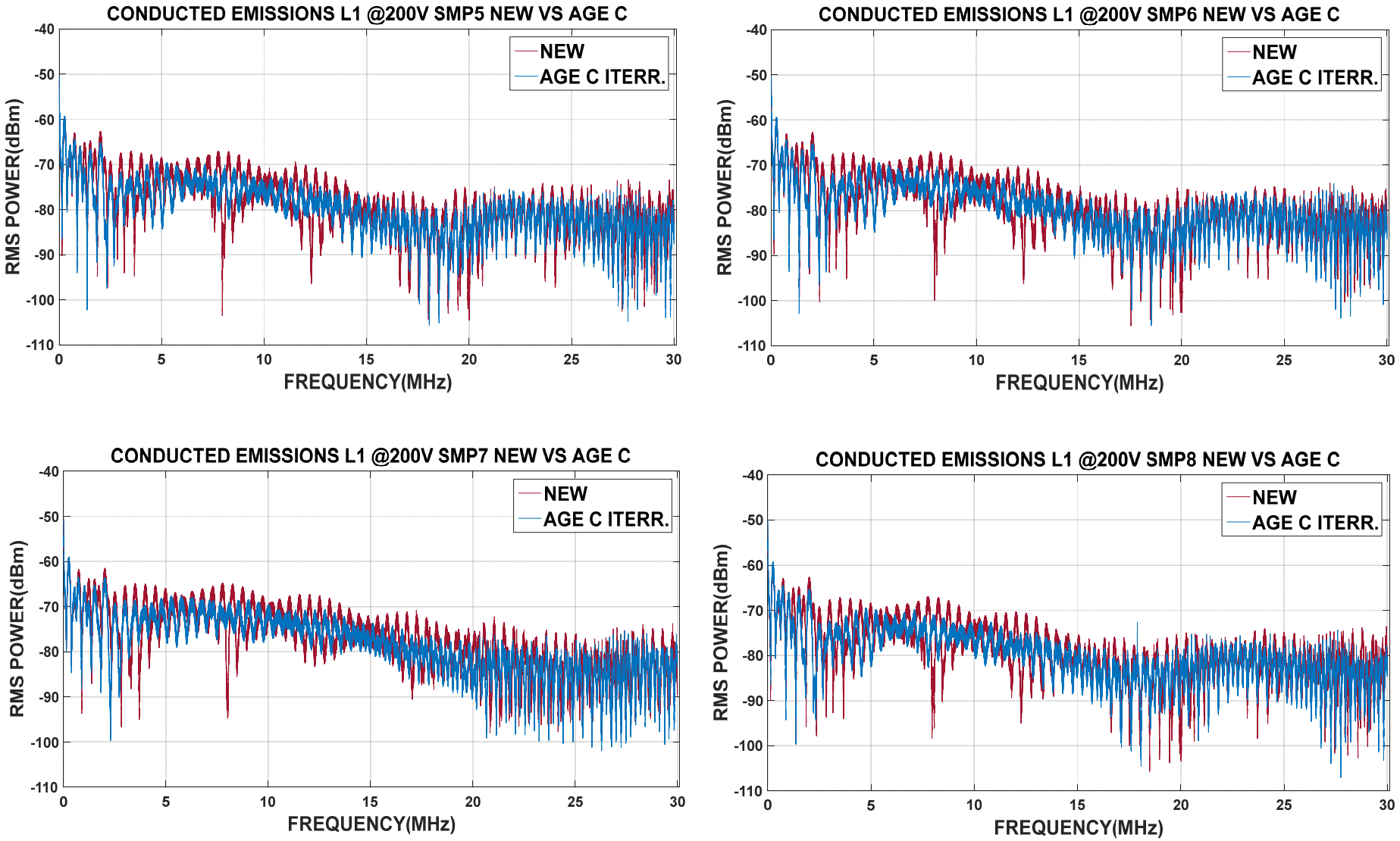


Figure 6.41 - - IGBT Samples 5 to 8, CISPR16-1-1 A&B Bands Conducted, L_1 (Forward Line) Conducted Emissions Spectra, New vs Age Iteration C.

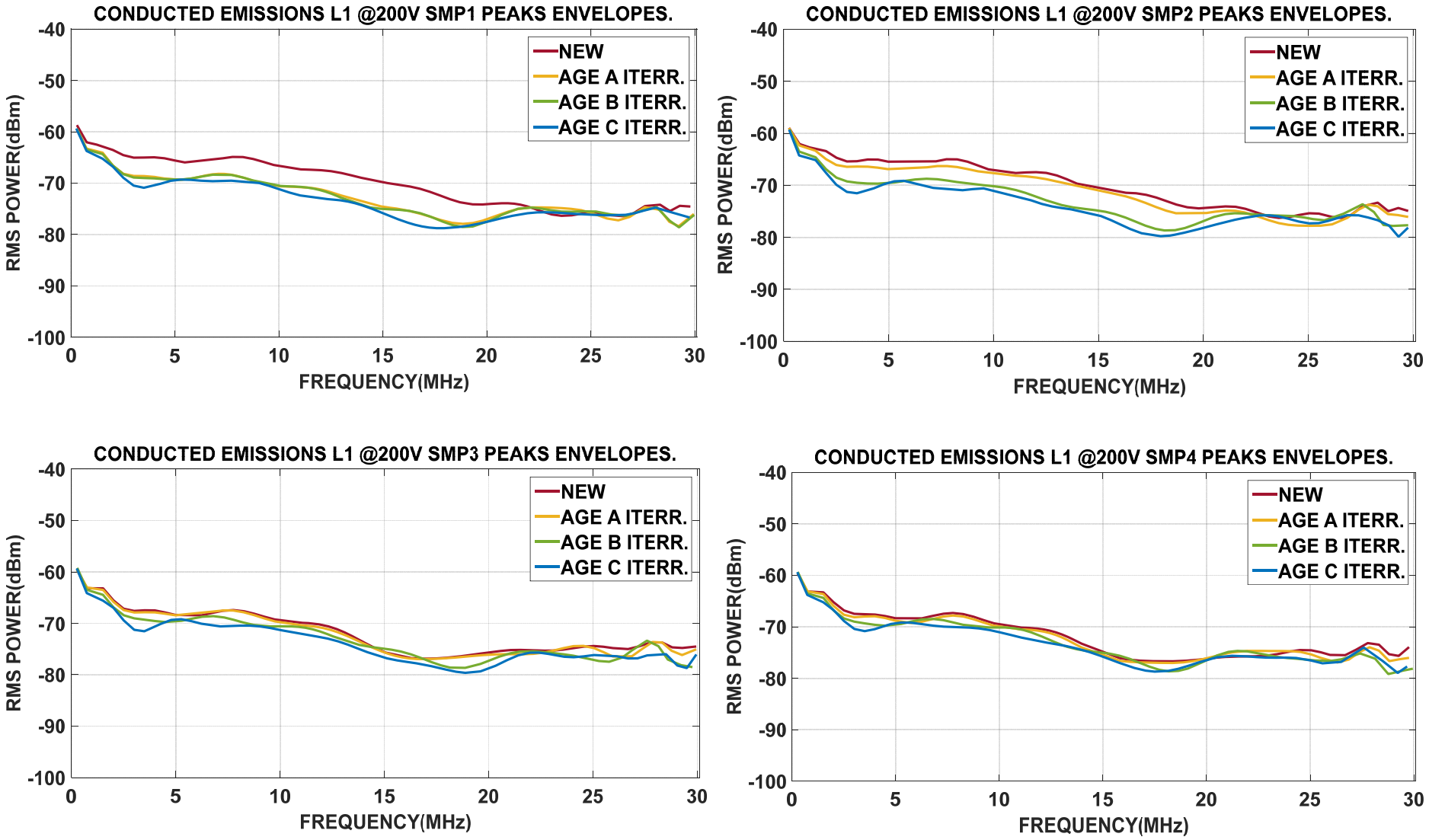


Figure 6.42 - IGBT Samples 1 to 4, CISPR16-1-1 A&B Bands, L_1 (Forward Line) Conducted Emissions Frequency Peaks Envelopes, All Age Iterations.

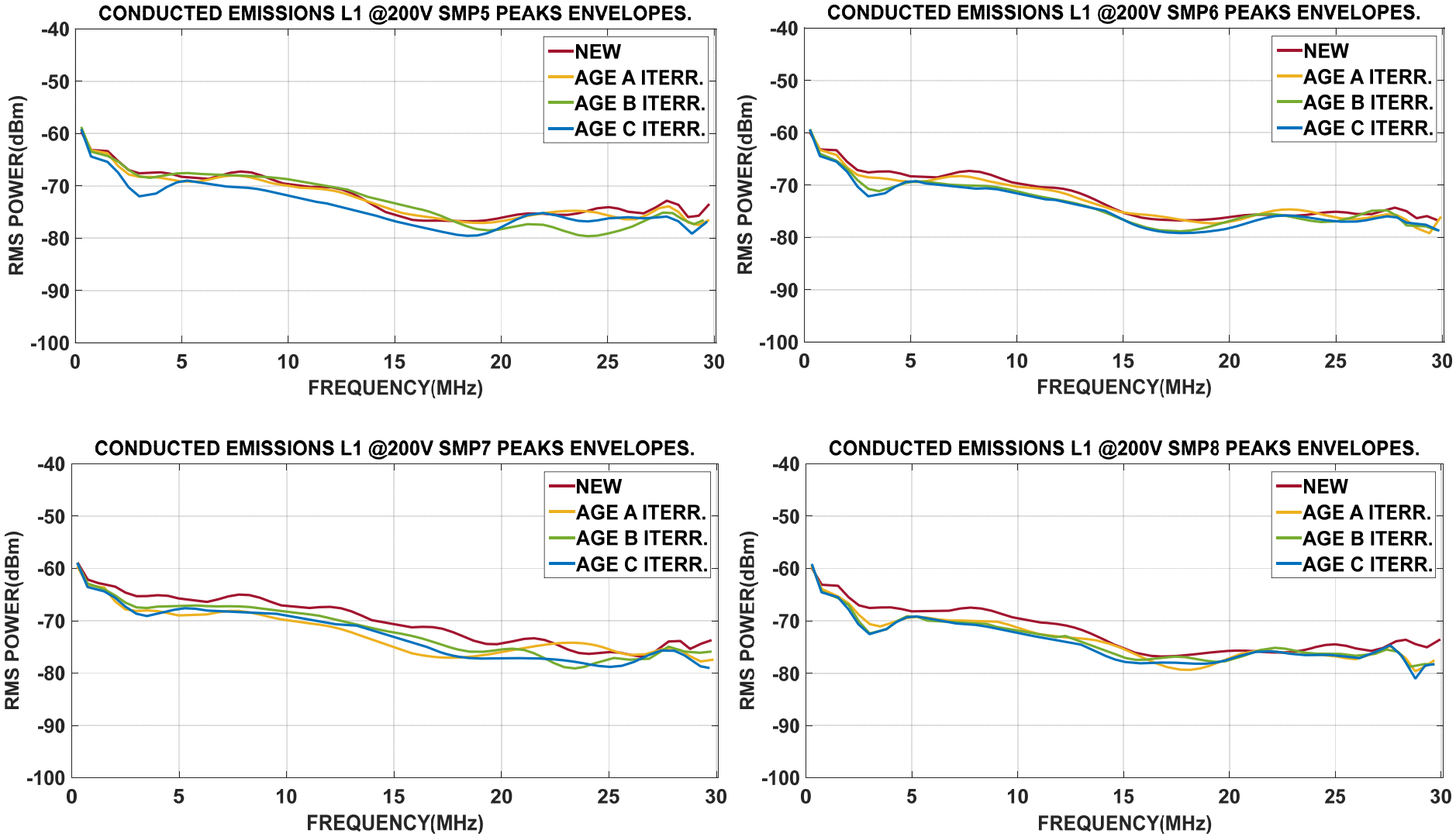


Figure 6.43 - IGBT Samples 5 to 8, CISPR16-1-1 A&B Bands, L_1 (Forward Line) Conducted Emissions Frequency Peaks Envelopes, All Age Iterations.

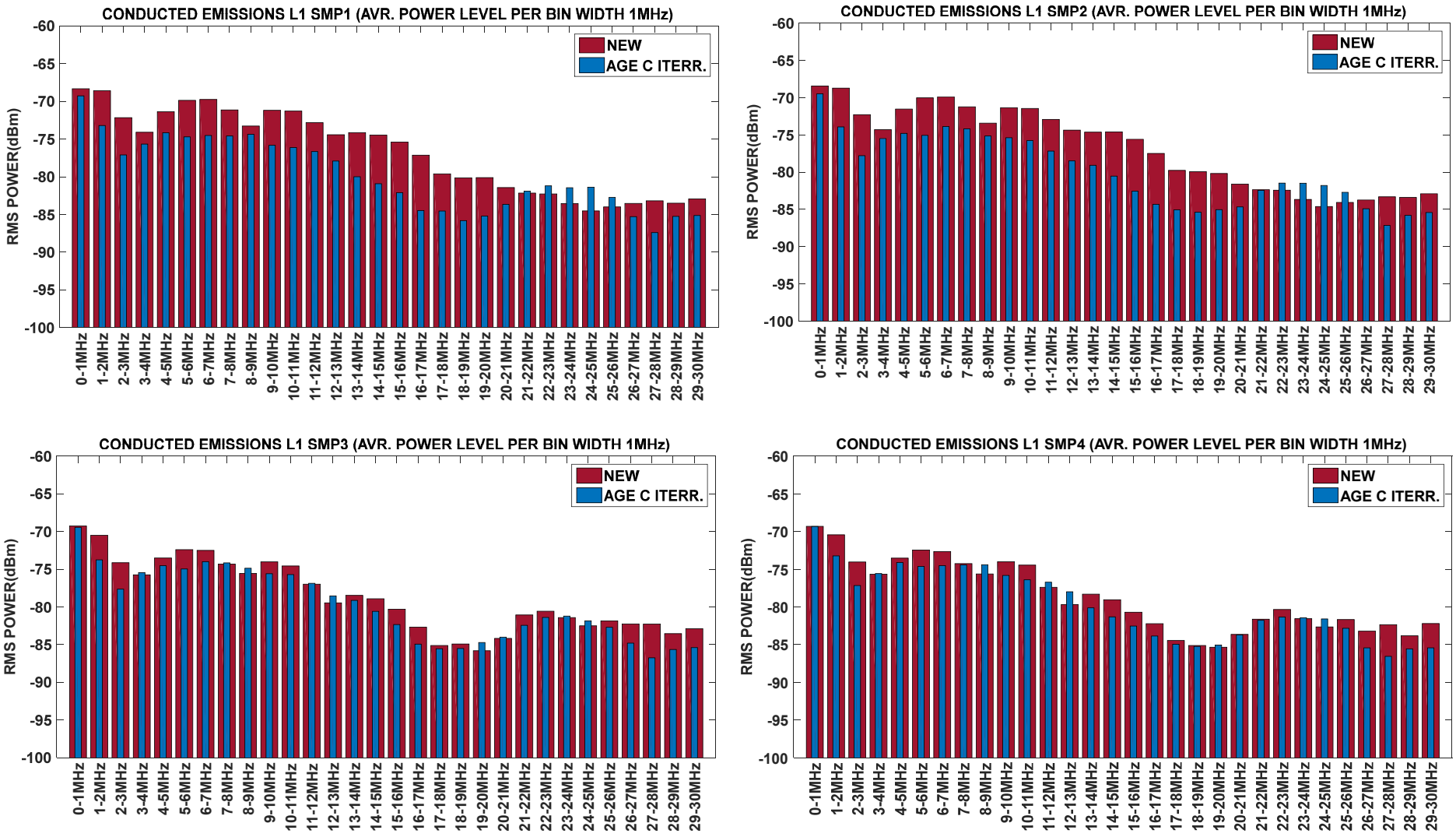


Figure 6.44 - IGBT Samples 1 to 4, CISPR16-1-1 A&B Bands, L_1 (Forward Line) Conducted Emissions, Average Power Level per 1MHz bandwidth bin.

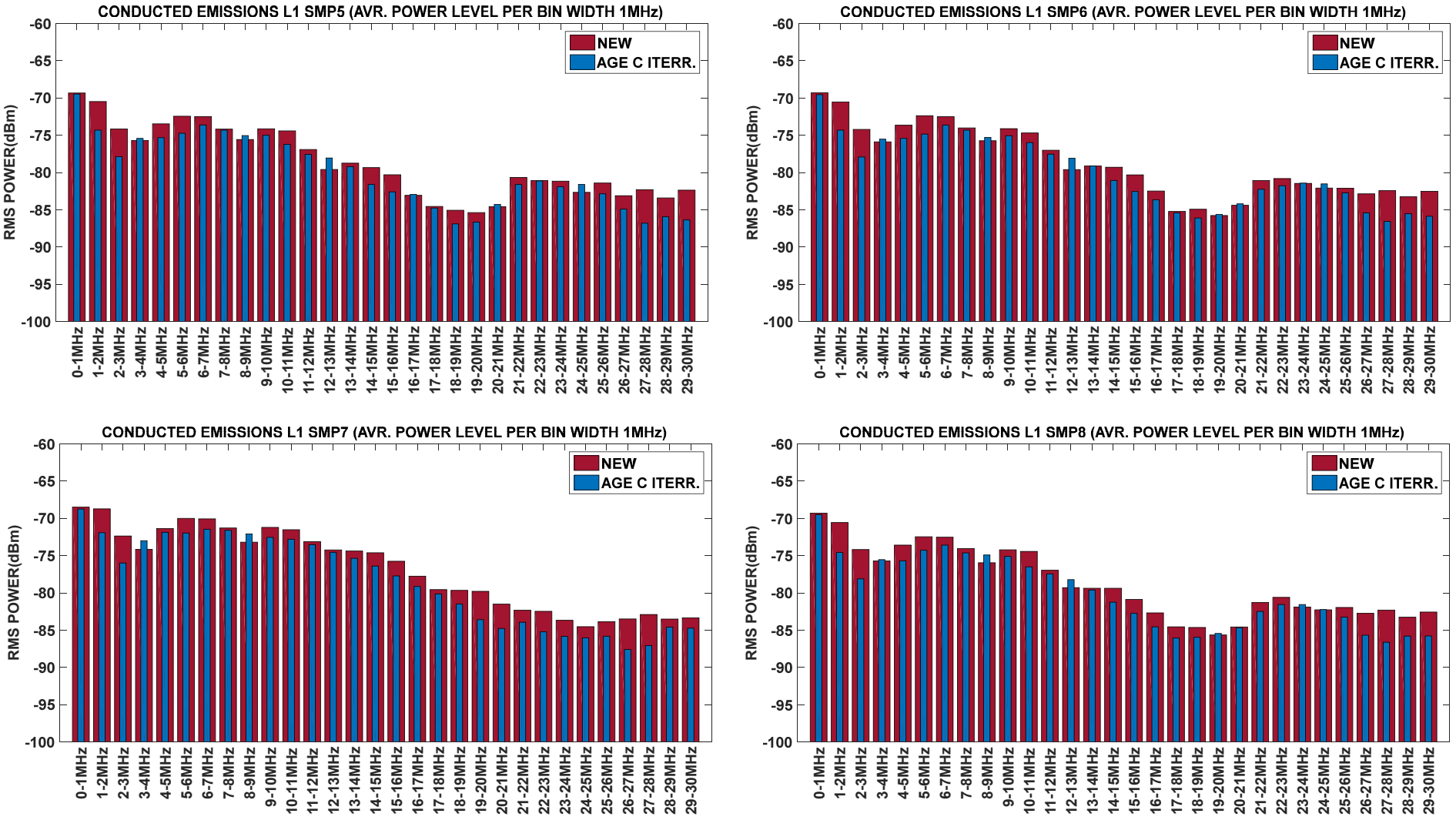


Figure 6.45 - IGBT Samples 5 to 8, CISPR16-1-1 A&B Bands, L_1 (Forward Line) Conducted Emissions, Average Power Level per 1MHz bandwidth bin.

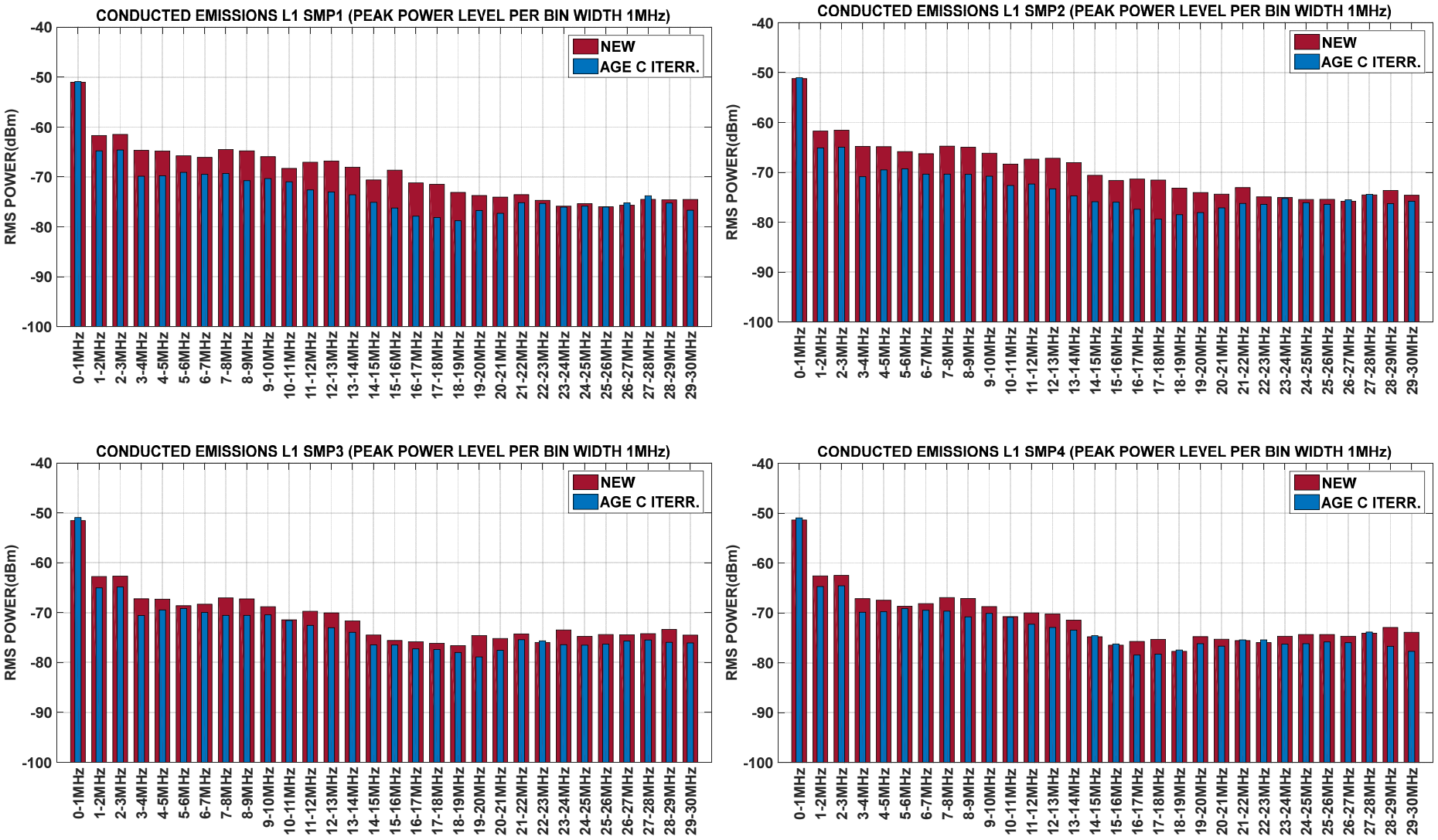


Figure 6.46 - IGBT Samples 1 to 4, CISPR16-1-1 A&B Bands, L_1 (Forward Line) Conducted Emissions, Peak Power Level per 1MHz bandwidth bin.

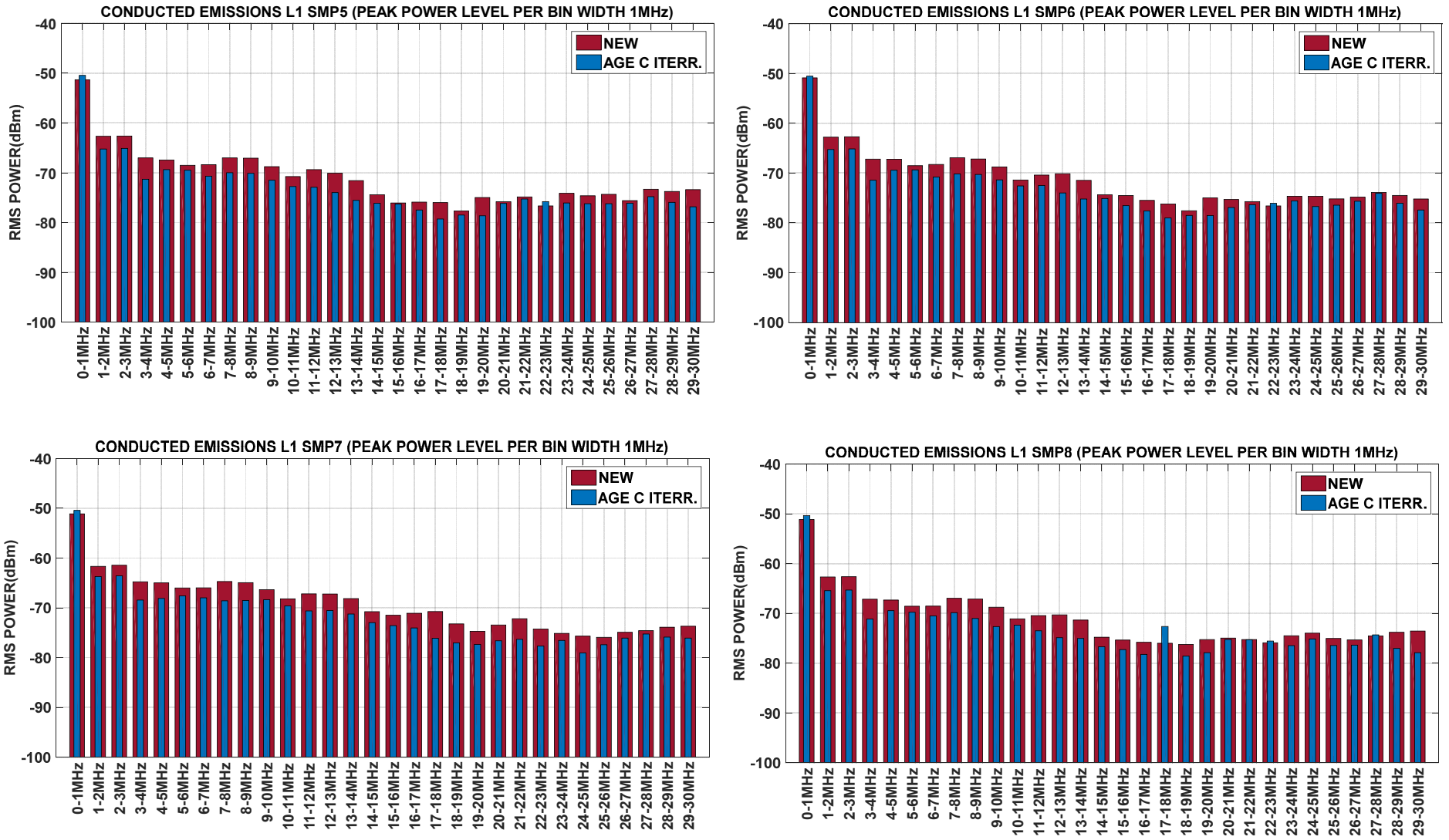


Figure 6.47 - IGBT Samples 5 to 8, CISPR16-1-1 A&B Bands, L_1 (Forward Line) Conducted Emissions, Peak Power Level per 1MHz bandwidth bin.

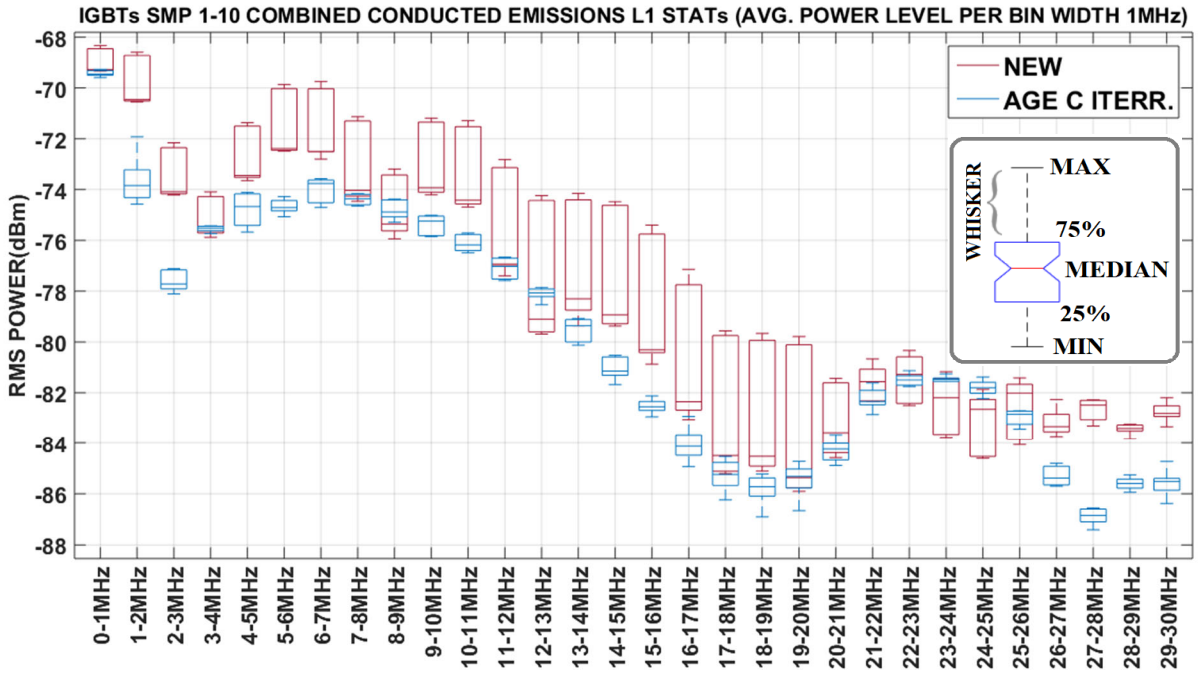


Figure 6.48 - Combined Statistics of IGBTs Samples 1-10, CISPR16-1-1 A&B Bands Conducted Emissions, L1 (Forward Line), Average Power Level for every 1MHz bandwidth bin, as detected by the EMI Receiver's RMS detector.

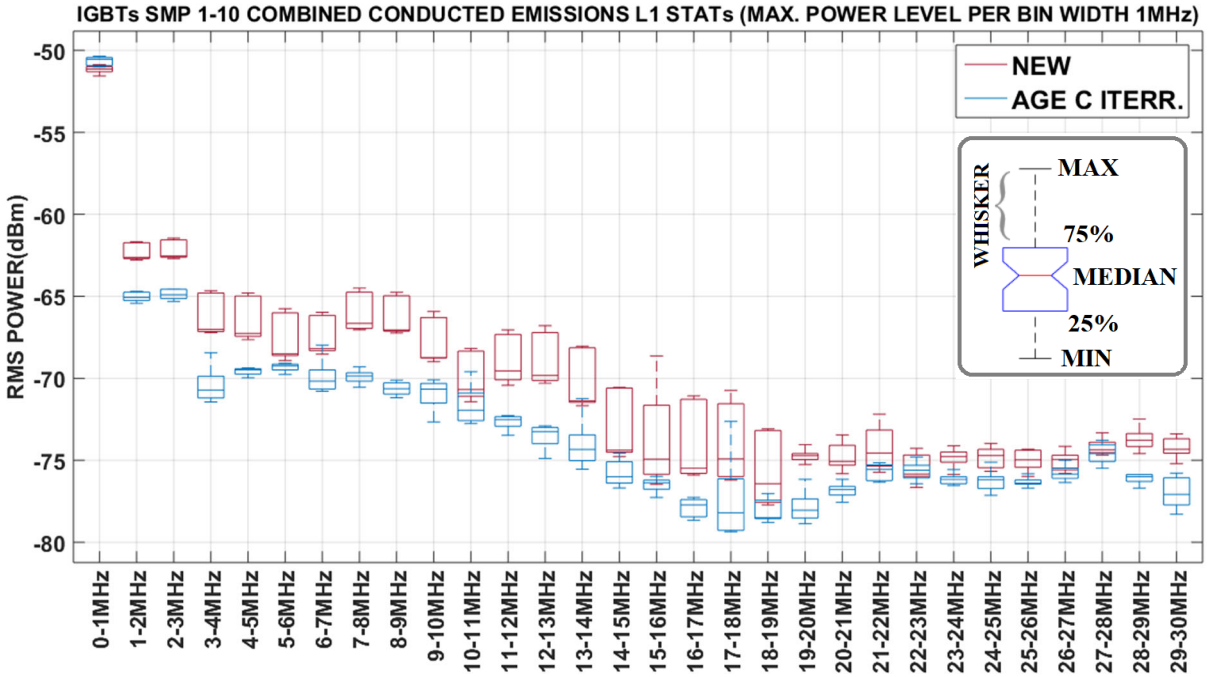


Figure 6.49 - Combined Statistics of IGBTs Samples 1-10, CISPR16-1-1 A&B Bands Conducted Emissions, L1 (Forward Line), Peak Power Level for every 1MHz bandwidth bin, as detected by the EMI Receiver's RMS detector.

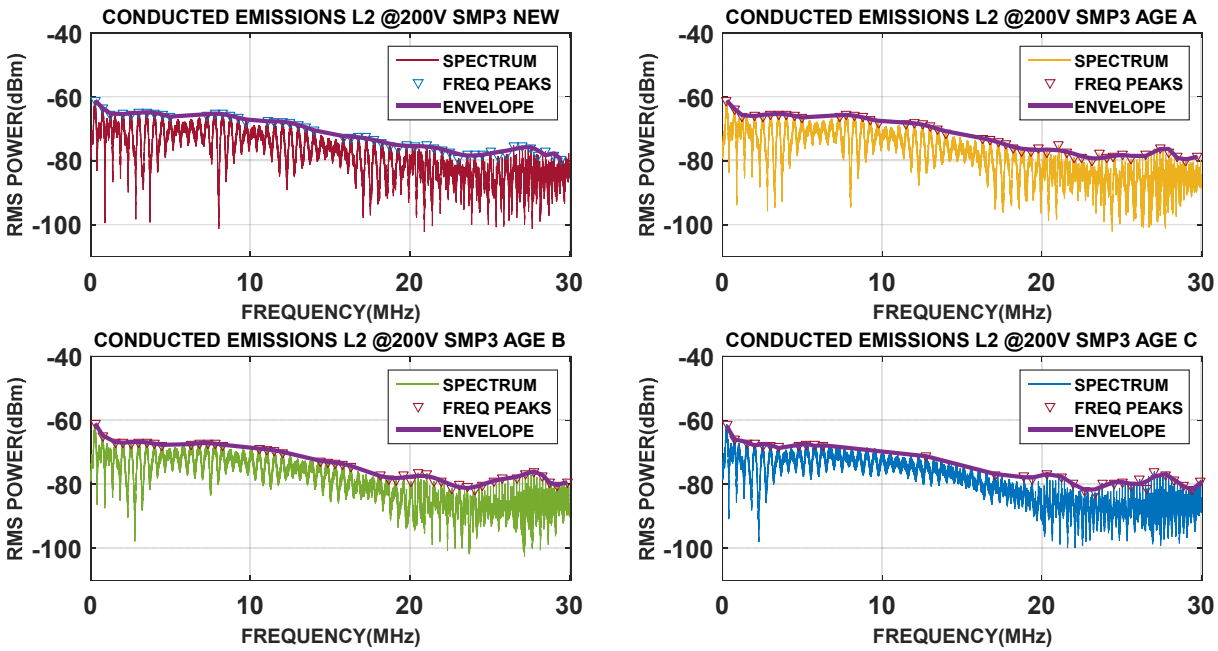


Figure 6.50 - IGBT Sample 3 CISPR16-1-1 A&B Bands, L_2 (Return Line), Conducted Emissions Spectra, Frequency Peaks, and corresponding Peaks Envelopes (i) New (ii) Age Iteration A (iii) Age Iteration B (iv) Age Iteration C.

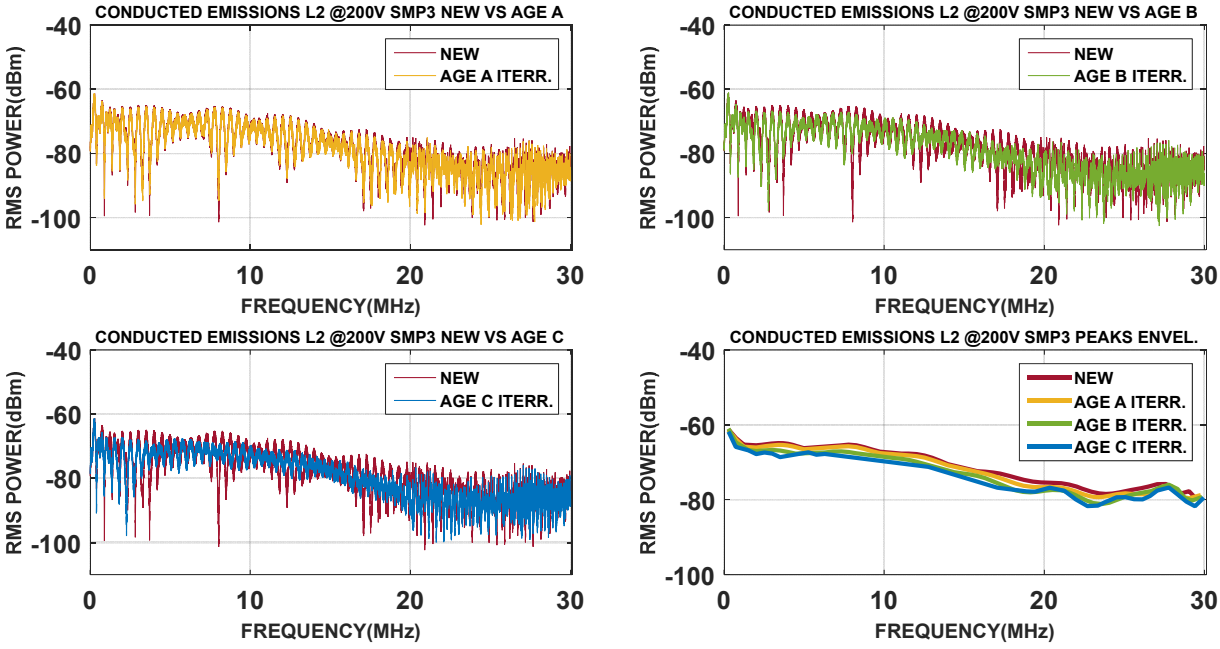


Figure 6.51 - IGBT Sample 2 CISPR16-1-1 A&B Bands, L_2 (Return Line) Conducted Emissions Spectra (i) New vs Age Iteration A (ii) New vs Age Iteration B (iii) New vs Age Iteration C (iv) Comparison of All Iterations, Frequency Peaks Envelopes.

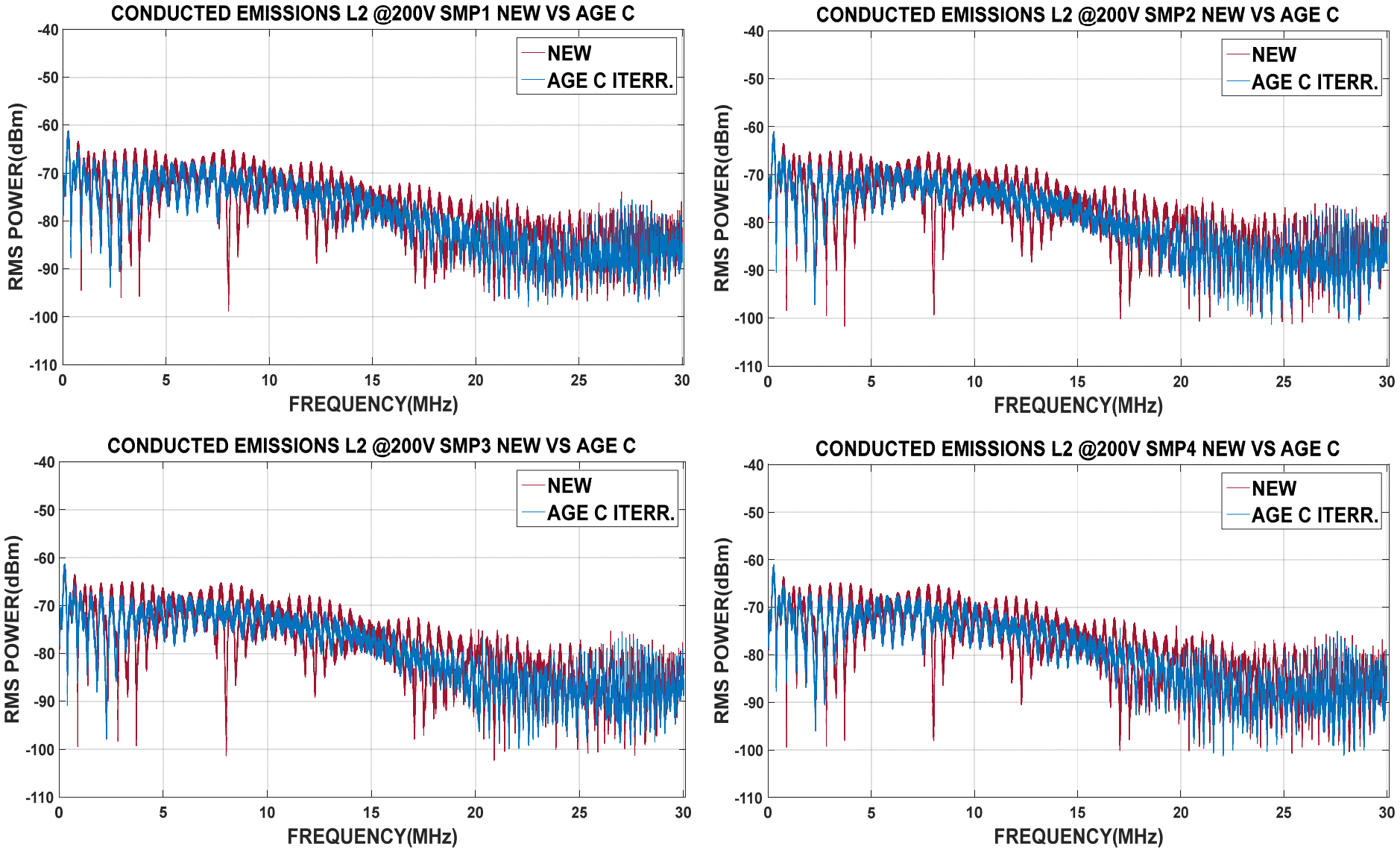


Figure 6.52 - IGBT Samples 1 to 4, CISPR16-1-1 A&B Bands, L_2 (Return Line), Conducted Emissions Spectra, New vs Age Iteration C.

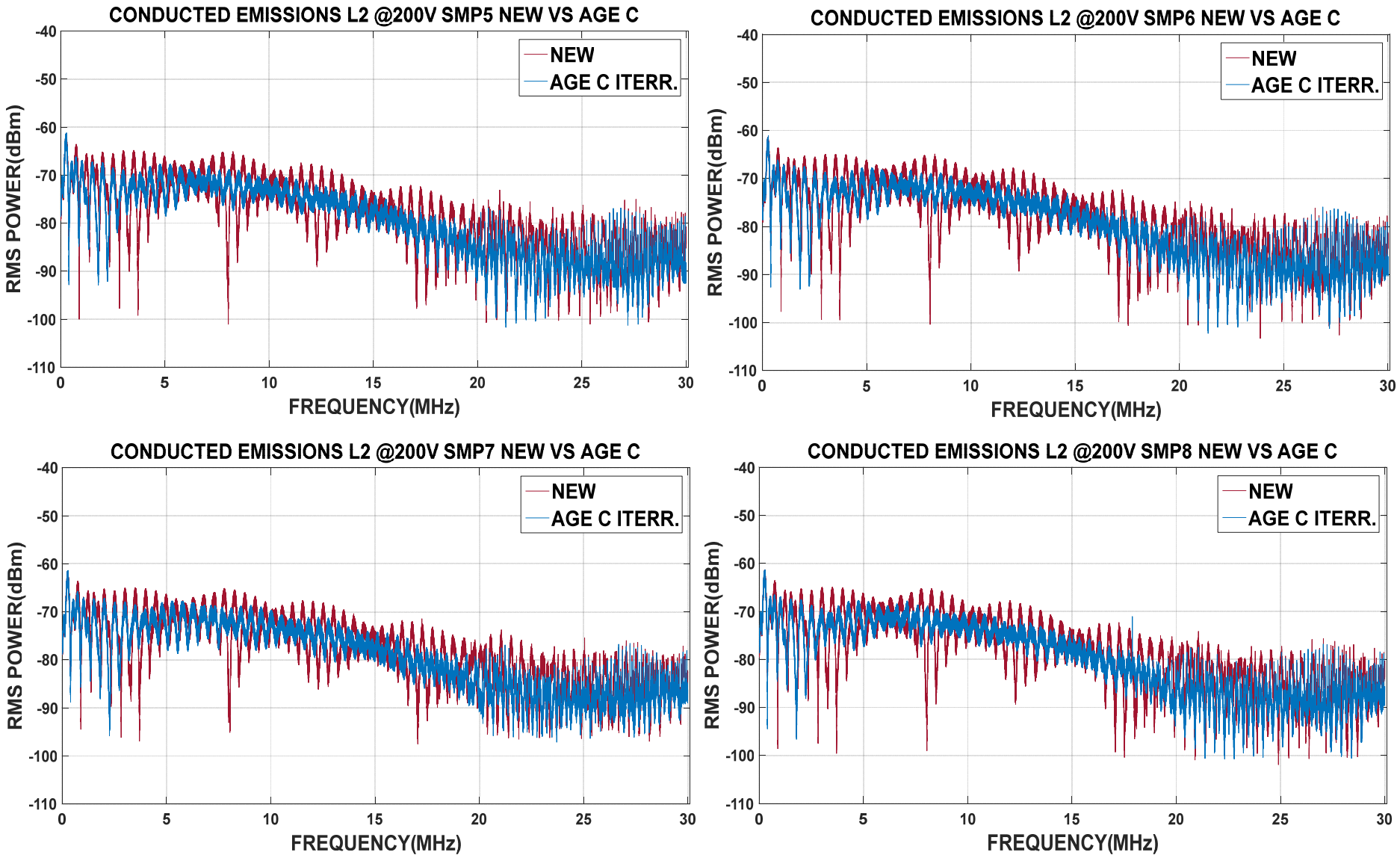


Figure 6.53 - IGBT Samples 5 to 8, CISPR16-1-1 A&B Bands, L_2 (Return Line), Conducted Emissions Spectra, New vs Age Iteration C.

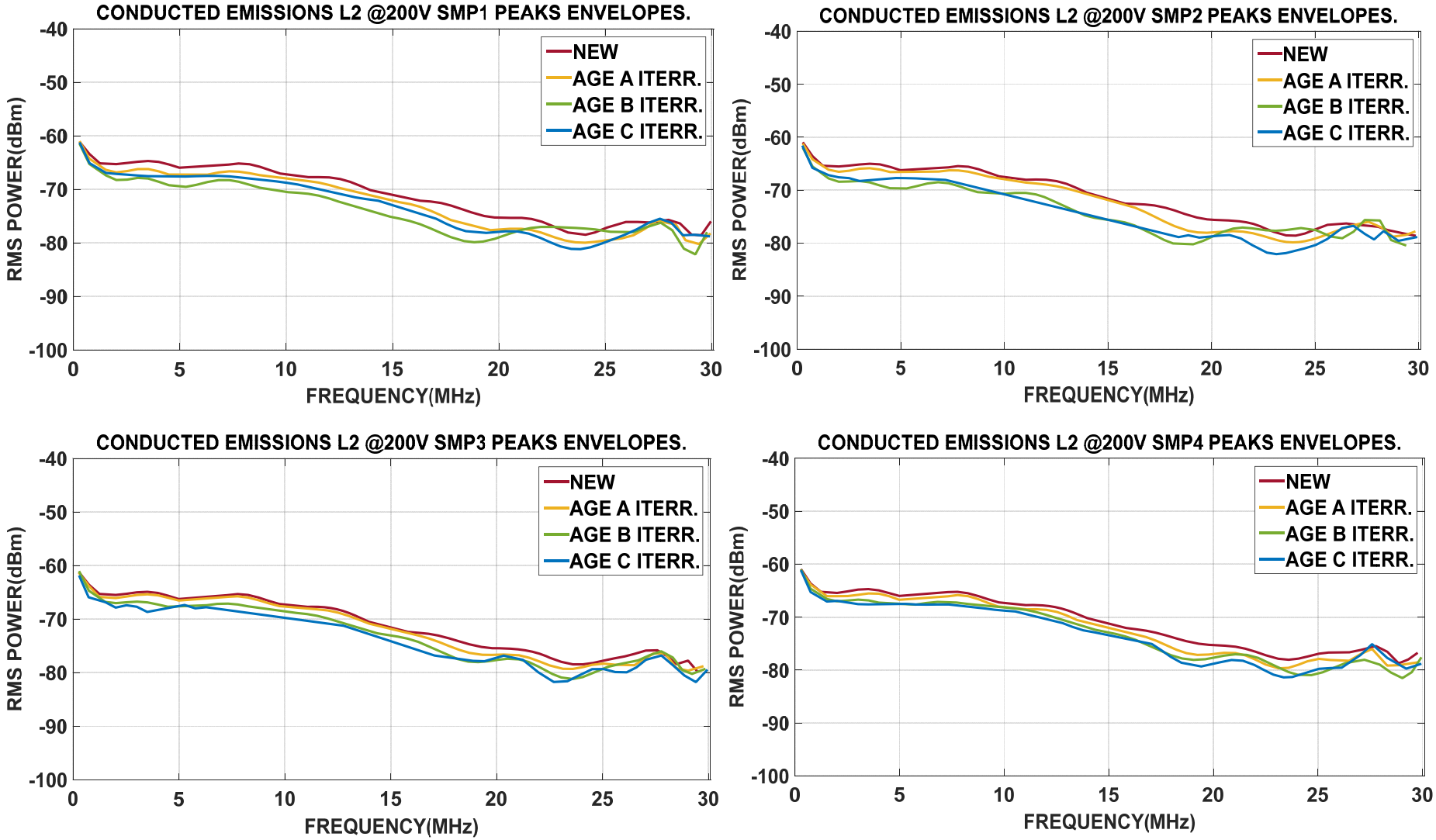


Figure 6.54 - IGBT Samples 1 to 4, CISPR16-1-1 A&B Bands, L_2 (Return Line), Conducted Emissions, Frequency Peaks Envelopes, All Age Iterations.

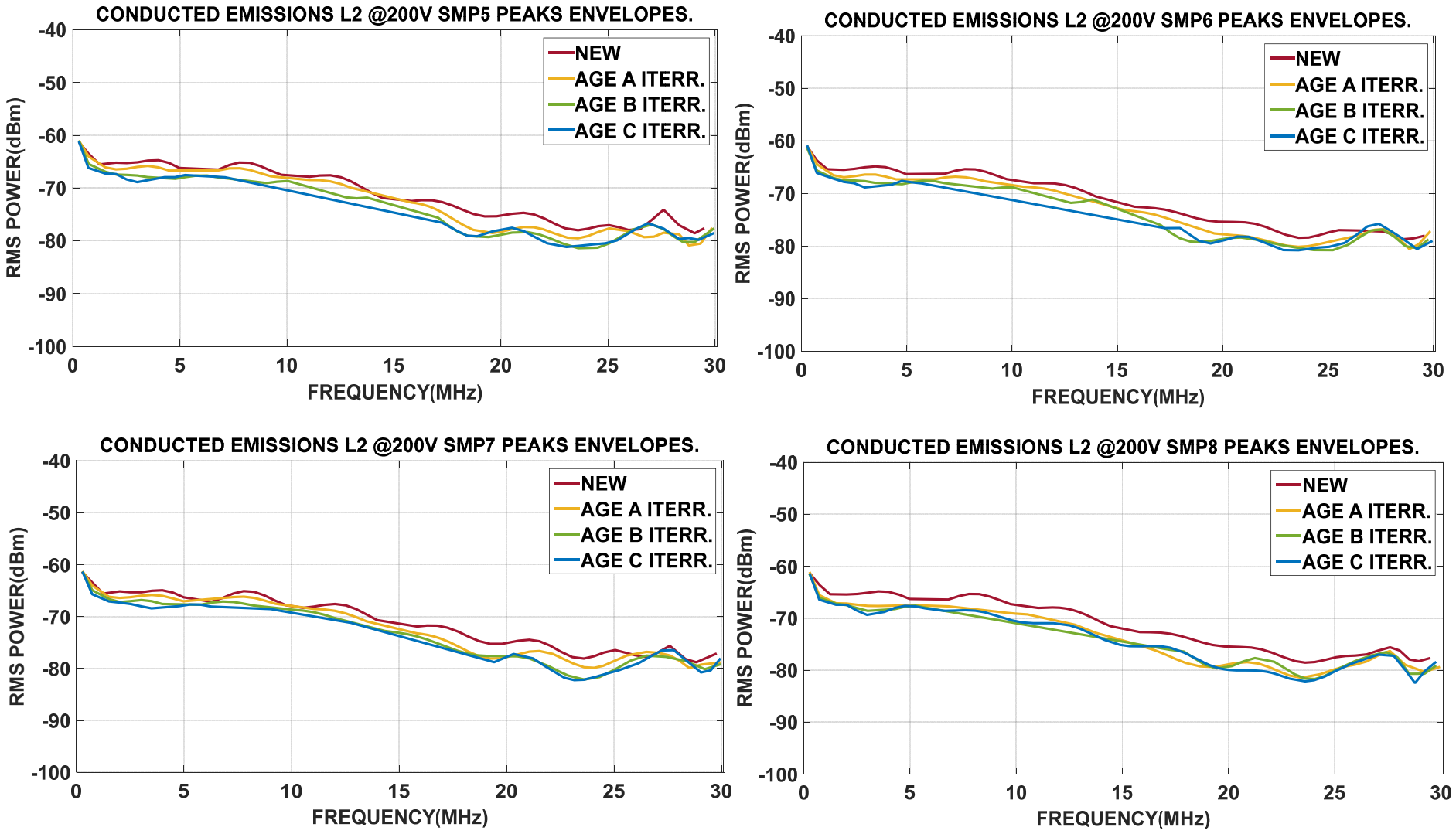


Figure 6.55 - IGBT Samples 5 to 8, CISPR16-1-1 A&B Bands, L_2 (Return Line), Conducted Emissions, Frequency Peaks Envelopes, All Age Iterations.

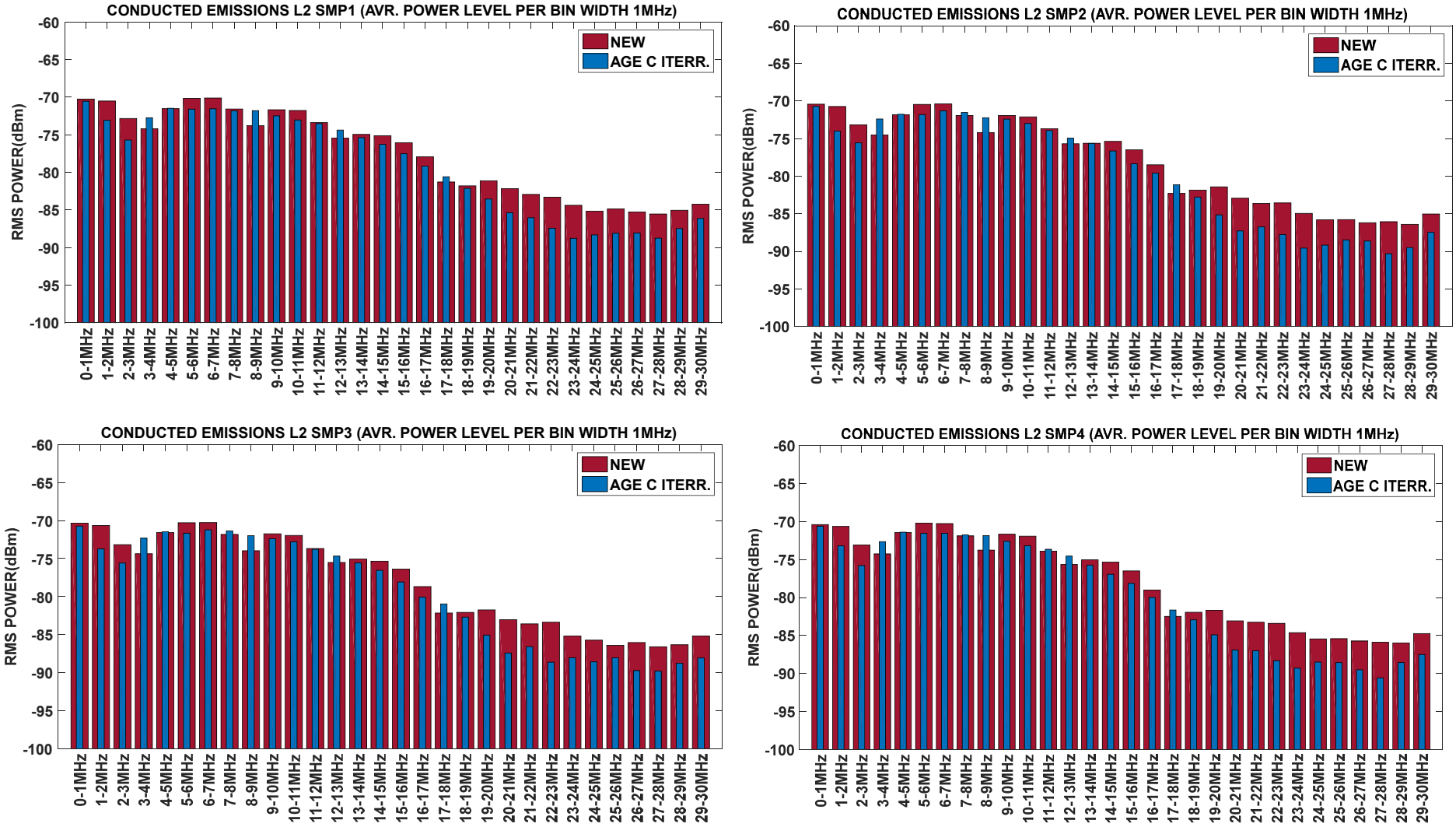


Figure 6.56 - IGBT Samples 1 to 4, CISPR16-1-1 A&B Bands, L_2 (Return Line) Conducted Emissions, Average Power Level per 1MHz bandwidth bin.

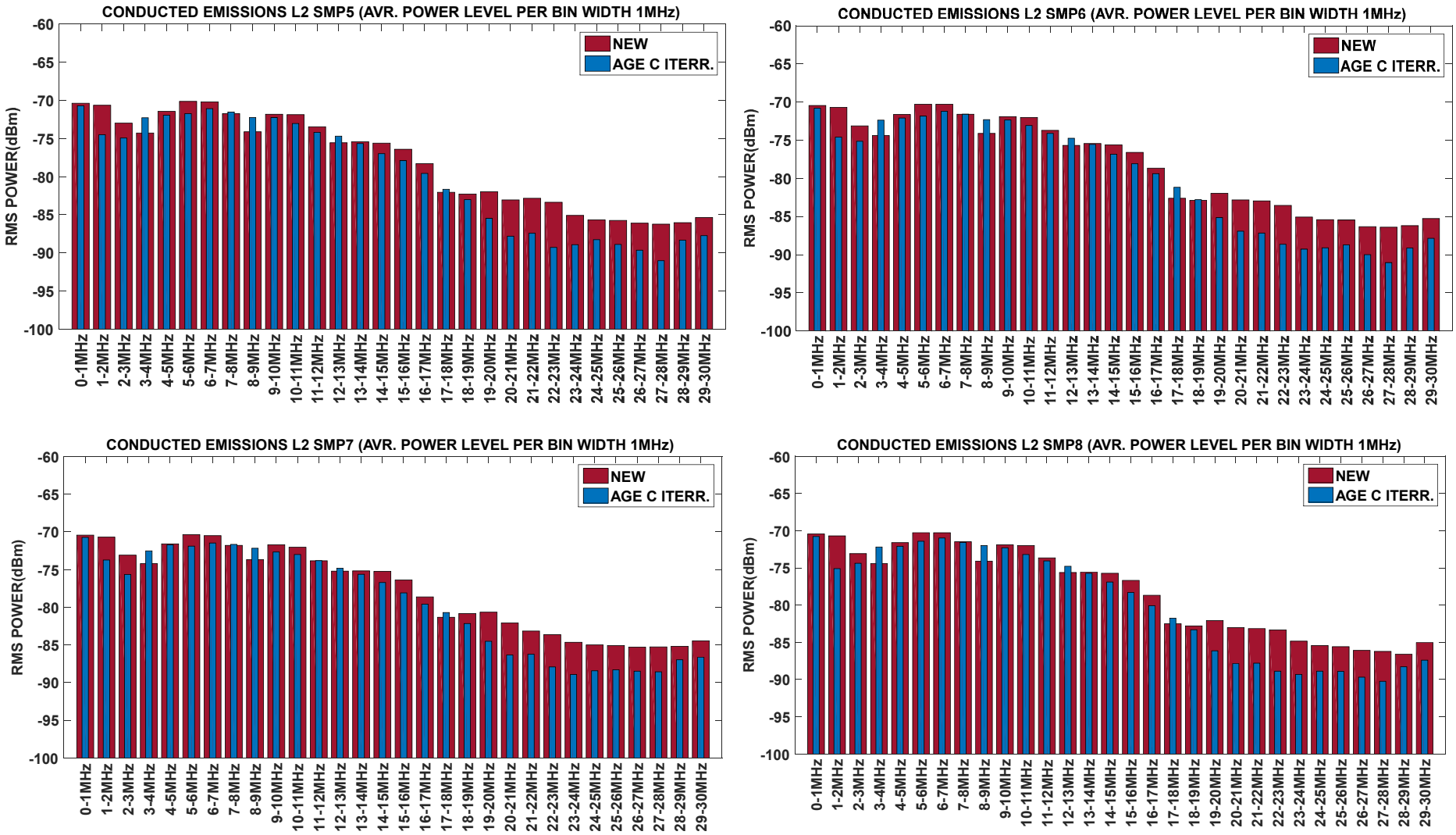


Figure 6.57 - IGBT Samples 5 to 8, CISPR16-1-1 A&B Bands, L_2 (Return Line) Conducted Emissions, Average Power Level per 1MHz bandwidth bin.

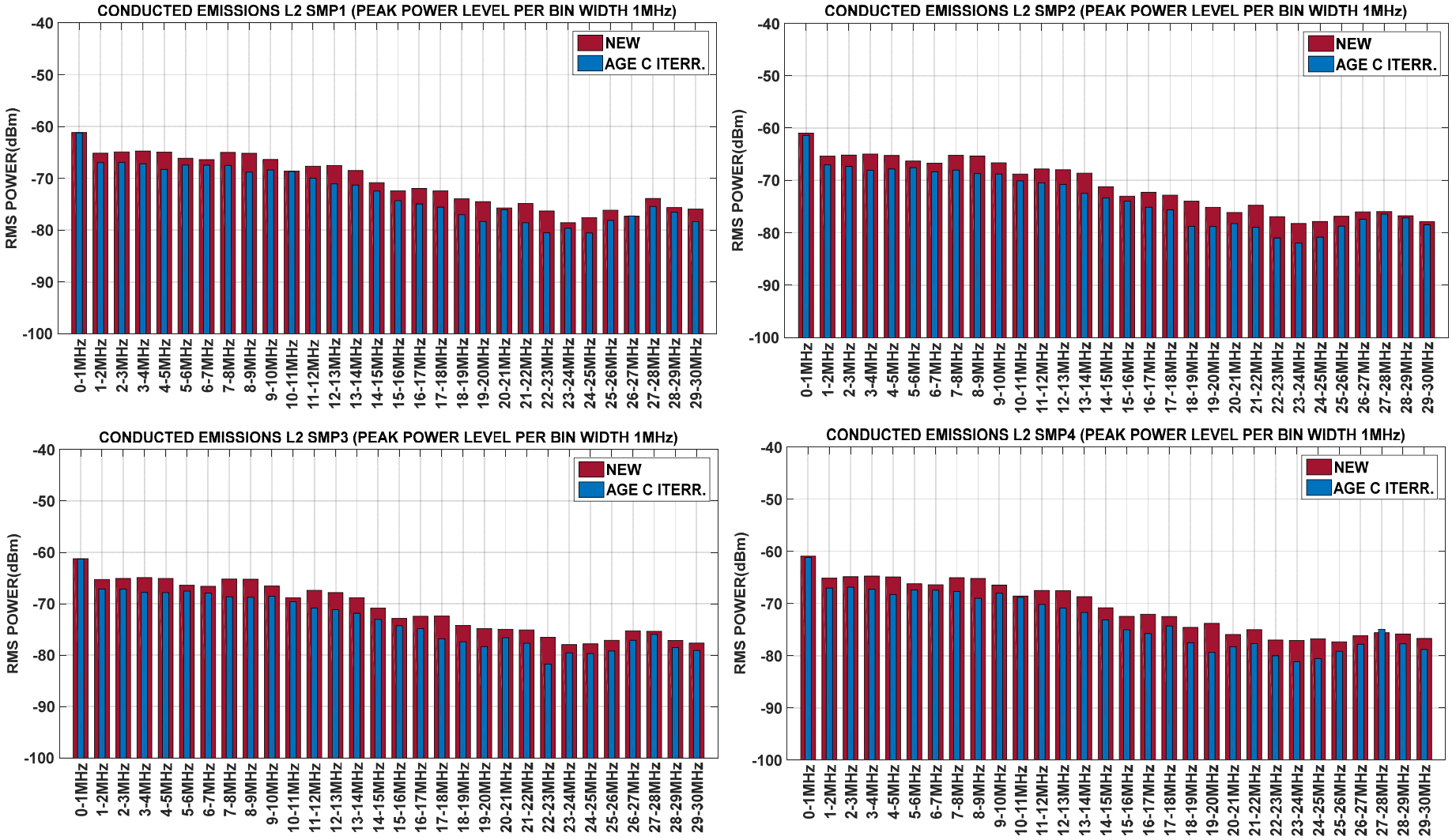


Figure 6.58 - IGBT Samples 1 to 4, CISPR16-1-1 A&B Bands, L2 (Return Line) Conducted Emissions, Maximum Power Level per 1MHz bandwidth bin.

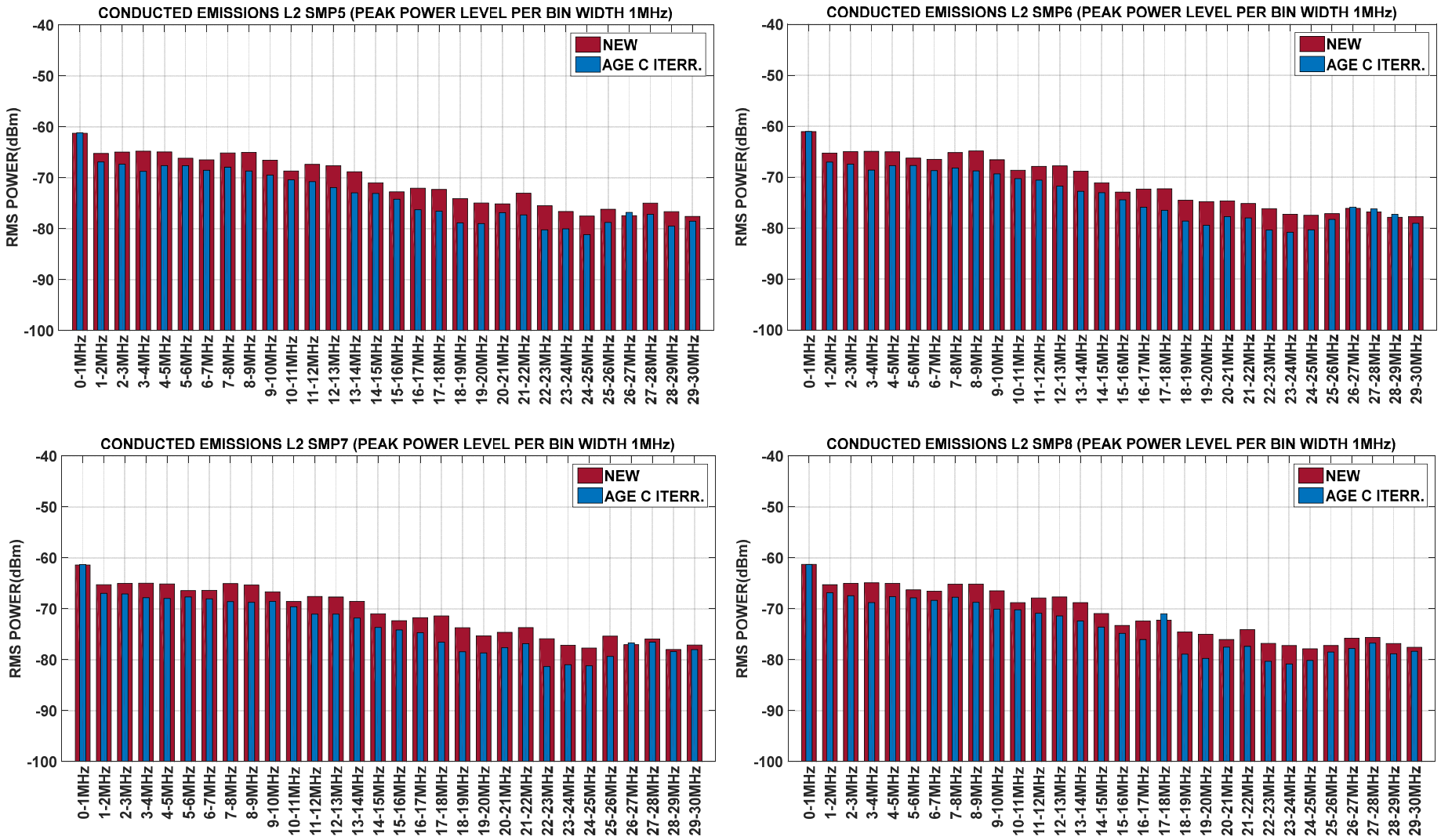


Figure 6.59 - IGBT Samples 5 to 8, CISPR16-1-1 A&B Bands, L_2 (Return Line) Conducted Emissions, Maximum Power Level per 1MHz bandwidth bin.

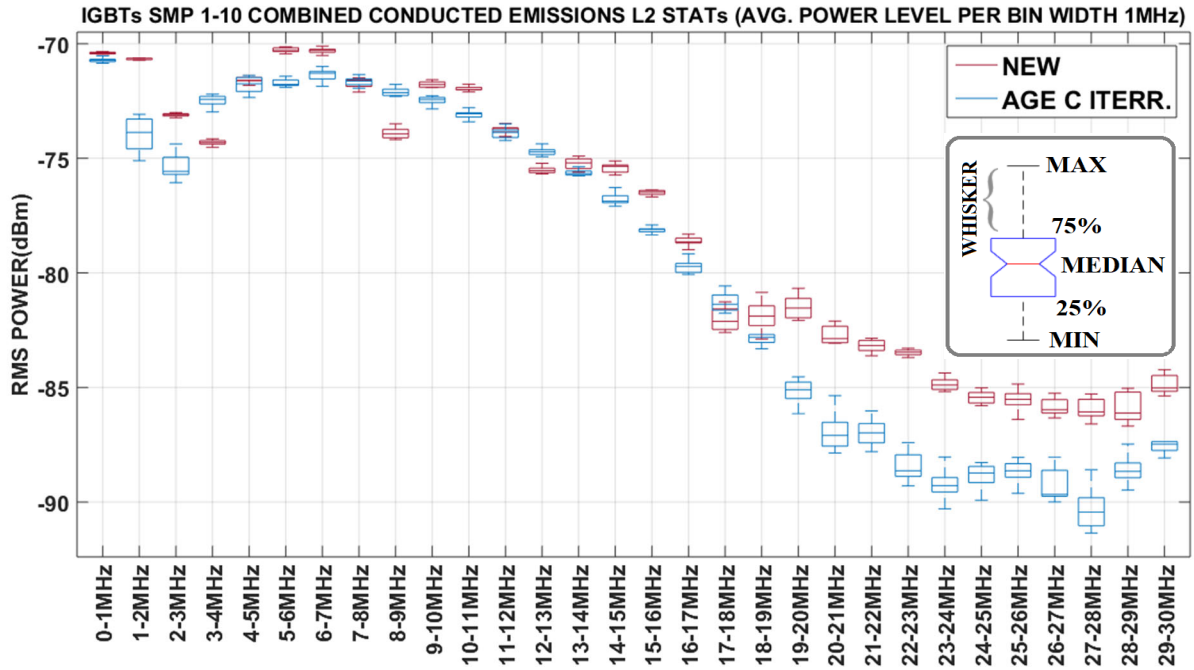


Figure 6.60 - Combined Statistics of IGBTs Samples 1-10, Conducted Emissions CISPR16-1-1 A&B Bands, L_2 (Return Line), Average Power Level for every 1MHz bandwidth bin, as detected by the EMI Receiver's RMS detector.

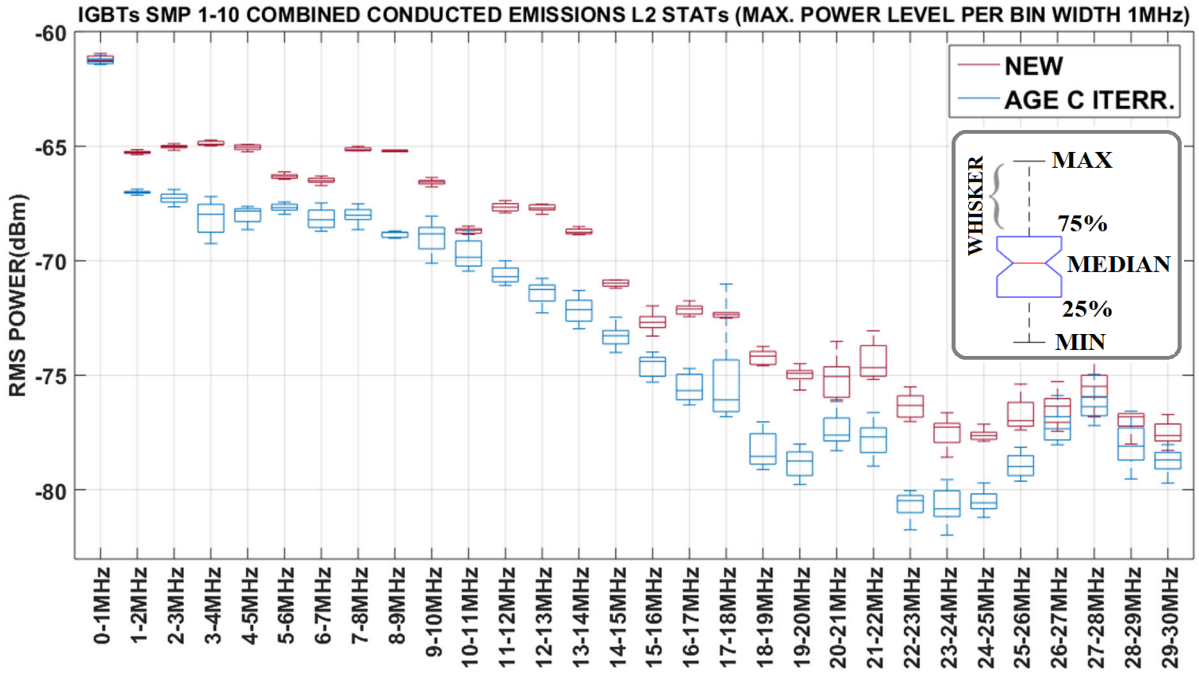


Figure 6.61 - Combined Statistics of IGBTs Samples 1-10, Conducted Emissions CISPR16-1-1 A&B Bands, L_2 (Return Line), Peak Power Level for every 1MHz bandwidth bin, as detected by the EMI Receiver's RMS detector.

6.5 Conclusions

As explained in Chapter 2, there are few studies which addressed the relationship between the conducted EMI and the degradation of an IGBT [166-168], with the referenced literature providing contrasting results. For instance, in [167], even though claiming that with the implemented accelerated ageing, the characterized IGBTs experienced a slow-down in both the turn-on and turn-off transients, it was still reported that there was an increase in the measured disturbance level, across the EM conducted emissions bandwidth (<100MHz). Moreover, it was reported that this increase became more definite as the ageing procedure duration increased. In [168], it was shown that the EM conducted emissions disturbance increased with the increase of bond-wire lift-off, for frequencies smaller than 600kHz. For higher frequencies, this study could not conclude if the measured enhanced disturbance was exclusively due to this degradation mechanism. This shows that the available studies in this regard, are very limiting and to a certain extent inconclusive. Hence, this chapter presented an experimental study, with the aim to determine, if any measurable changes in the conducted disturbances exit, between an EUT employing a new and healthy IGBT and the same EUT employing the same IGBT, after being subjected to accelerated ageing and hence in a degraded state. The presented study aimed to establish the influence of a degraded IGBT on the EM conducted emissions. The degradation procedure was qualified to be a DC PCAS of the constant case-temperature peak-to-peak fluctuation ($T_{C\_PK\text{-}PK}$) type, which predominantly produces degradation in the IGBT's metallization layers. As evidenced this accelerated ageing procedure, produced severe voiding in the die-attach layer of the characterized IGBT, which led to an enhanced junction temperature (T_J), even though the IGBT's case temperature (T_C) was maintained at room temperature. This latter effect led to a major slowdown of the collector current (I_C) and collector voltage (V_C) turn-off transients, with the turn-on transients remaining relatively unaltered. The turn-off slow down manifested predominantly in the collector current (I_C) transient, exhibiting an enhanced "tail current" due to the increase of the junction temperature (T_J). Moreover, this increase indirectly affected the operation of the parasitic devices of the IGBT, which impacted further other subphases of the IGBT's turn-off transient, contributing to the measured global slow-down of the IGBT's turn-off. This yielded to an increase in the IGBTs' turn-off switching power dissipation. Hence, this chapter presented the details of the experimental setup and procedure to measure the EM Conducted emissions, by taking into consideration the available standards and measurement practices. The measurement procedure involved the acquisition of both the individual signals' frequency domain spectra,

and the EM conducted emissions for the CISPR16-1-1 A and B bands. The comparative analysis of the individual signals' frequency domain and the EM conducted emissions, was considered important, as it provided a correlation between the spectral changes happening exclusively to the IGBT and the conducted emissions, which provide a more holistic EUT spectral analysis. In relation to the IGBT's signals, a prevalent decrease was measured in the magnitude of the spectral peaks of the collector voltage (V_C) signal, and the collector current (I_C) signal. Moreover, this decrease became more distinct, as the severity of the degradation progressed. Additionally, the collector current (I_C) signal experienced a measurable increase in the average harmonic magnitude within specific frequency bands lying in the lower half of the bandwidth of interest. Both results relate with the IGBT's turn-off transient slow-down and enhanced turn-off switching power dissipation. Correlative results were observed from the acquired EM conducted emissions of the EUT, for both the forward (L_1) and return (L_2) lines, these include:

1. A decrease in the conducted emissions disturbance peaks, with the decrease becoming more distinct as the IGBT's degradation progressed.
2. The bandwidth where the prevalent EM conducted emissions spectral peaks manifested, coincides in its entirety with the bandwidth where the prevalent decrease in magnitude of the collector current (I_C) spectral peaks occurred. Moreover, it overlaps with the bandwidth where the collector voltage (V_C), manifested the major decrease in the spectral peaks' magnitude.
3. The measured EUT's EM conducted emissions, especially those measured on the return line (L_2), experienced a measurable increase in the average harmonic power within the same frequency bands where the collector current (I_C) experienced an increase in the average spectral magnitude.

The above results yield to the conclusion that an IGBT, manifesting a degradation in the metallization layers (in this case the die-attach), hence with a hindered thermal path between the junction and case, will contribute to a decrease in the EM conducted emissions of an EUT employing such IGBT, when compared to the EM conducted emissions of an EUT employing a new or healthy IGBT. This is to a certain extent exclusively due to a slow-down of the IGBT's turn-off transient. Moreover, the changes happening within EM conducted emissions, constitute a considerable correlation to the changes occurring within the collector current (I_C) frequency domain, and hence both signals provide major diagnostic insight on the health state of the IGBT's solder layers (die-attach) which are involved in the heat dissipation of the IGBT.

Chapter 7 Conclusion and Future Work

7.1 Conclusions

Insulated Gate Bipolar Transistors (IGBTs) are power devices which combine the low-on-state capabilities of a bipolar transistor (at increased breakdown voltage levels), with the facilitated input voltage control of a MOSFET. These advantageous capabilities, in conjunction with the enhanced switching characteristics, promoted the employment of IGBTs, in various standard power electronic circuits and systems, in applications such as energy, transport and space. Some of these applications can present adverse operational environments, which means that it is important to determine the IGBT's sources of failure and the corresponding failure mechanisms. The conducted literature review and the presented FMEA, evidenced that there are multiple sources which can yield to the IGBT's degradation and eventual failure. The conducted FMEA outlined multiple locations where failure can manifest, but it showed three locations where degradation and eventual failure can be predominant. These are the gate dielectric oxide, the bonding wires and the metallization layers which are responsible of conducting and dissipating the generated heat. These failures commonly manifest when the IGBT is subjected to:

- Large junction temperature (T_J) swings, which due to the different IGBT's sub-components thermal expansion coefficients, degradations such as cracks, ruptures and lift-off evince within the IGBT's bonding-wires,
- Elevated junction temperature (T_J), which mainly effect the integrity of the metallization layers such as the die-attach, causing degradation such as cracks, voids, and melting, as well as, abetting the implant of charge carriers within the dielectric's oxide layer.

IGBT manufacturers, electronics engineers, and application engineers, utilize accelerated ageing systems, principally Power Cycling Ageing Systems (PCAS), where through power and thermal overstress, controlled degradation is induced within the IGBT. This helps to establish an understanding between the degradation mechanism and the corresponding mean time to failure (MTTF). Moreover, the conducted literature review showed how during ageing, the changes manifested, by the various IGBT's mechanical, electrical, and electronic parameters, yielded to the establishment of diagnostics, which were utilized within prognostic techniques,

to determine the health state of the IGBT. The conducted literature review evidenced limited research, where a particular failure mechanism was thoroughly studied vis-à-vis the changes experienced by the IGBT parameters, establishing the physical-electronics' changes happening within the IGBT, through empirical analysis and modelling, and eventually correlating the impacts of the IGBT's failure mechanism with the IGBT's operation. A significant gap in knowledge was evidenced in literature, in relation to the changes occurring in the conducted and radiated EMI of an EUT, in relation to the manifestation of specific IGBT's degradation, and hence the ascertainment if these changes can be effectively employed to diagnose the health state of the IGBT. Hence this research tried to address this gap, by studying the relationship between the degradation in the IGBT's metallization layers (particularly the die-attach layer), the static and dynamic operation of the IGBT, and the consequential influence this degradation has, on the EM conducted disturbances. This was achieved, by executing the following research phases, hence obtaining the following contributions to knowledge:

1. Design and development of a DC PCAS, consisting of custom-built hardware, the integration of commercially available instrumentation, and the development of the accelerated ageing control and data acquisition software. The implemented power cycling strategy was of the constant case-temperature peak-to-peak fluctuation ($T_{C\_PK\text{-}PK}$) type, where the IGBT's case temperature (T_C) and consequentially the junction temperature (T_J) was elevated well beyond the maximum junction temperature (T_{J_MAX}) and maintained oscillating around a pre-established elevated case temperature (T_C) until the IGBT manifested latch-up and hence thermal runaway. This strategy predominantly produced degradation in the IGBT's metallization layers (specifically the die-attach), manifesting enhanced voiding and melting as evidenced in the conducted X-Ray analysis, while contributing to the contamination of the gate oxide.
2. Design and development of an IGBT static parameters characterization system. The aim of this system was to measure the changes occurring within the degraded IGBTs' static parameters, namely the threshold voltage (V_{THRES}) which manifested an increase, the gate-emitter leakage current (I_{GE_LEAK}) which manifested an increase, the on-state voltage (V_{CE_ON}) which manifested a decrease, the output characteristics, the forward transconductance (g_{fe}) which manifested a decrease, the transfer characteristics, the internal diode's forward voltage which manifested a decrease and the internal diode's forward characteristics. The concurrent

presentation of the above IGBT's static parameters evolution, with the progression of the die-attach degradation, substantiated with X-Ray analysis and hence die-attach voiding progression, is considered a significant contribution to knowledge. Moreover, the gained knowledge of the changes experienced by the IGBT's static parameters, were utilized to model the IGBT switching transients' changes due to the implemented degradation.

3. Design and development of the IGBT's switching transients' characterization system (STCS), based on the Double-Pulse technique. This again involved the utilization of custom software and hardware along with the integration of commercial instrumentation, to measure the IGBT's turn-on and turn-off transients and the corresponding parameters namely, the Turn-Off Delay Time (t_{D_OFF}) which manifested a marginal decrease, the Fall-Time (t_F) which manifested a significant increase, the turn-off switching energy loss (E_{OFF}) which manifested a significant increase, the turn-off collector-emitter voltage rate of change (dV_{CE}/dt_{OFF}) which manifested a significant decrease, the turn-on delay time (t_{D_ON}) which manifested a marginal increase, the rise time (t_R) which manifested a marginal increase, the turn-on switching energy loss (E_{ON}) which manifested a marginal increase, the turn-on collector current rate of change (dI_C/dt_{OFF}) which manifested a marginal decrease, the internal diode reverse recovery time (t_{RR}) which manifested an increase, the internal diode peak reverse recovery current (I_{PRR}) which manifested an increase, and the internal diode energy loss during reverse recovery (E_{DRR}) which manifested an increase. The main result obtained during this research phase was, that the implemented IGBT degradation produced a general commutation slow-down, manifesting predominantly and to a certain extent exclusively within the IGBT's turn-off transient. These results were verified for IGBTs produced by different manufacturers. The concurrent presentation of the IGBT's switching parameters evolution with the implemented degradation, and the observed significant slow-down of the turn-off transients, is considered another important contribution to knowledge.
4. Modeling of the IGBT's switching transients (collector current (I_C) and collector-emitter voltage (V_{CE}) transients), including the changes influenced by the implemented degradation strategy. During this research phase, two modelling approaches were undertaken. The first method was based on the transient modelling, presented by Jin et al. [215], for new IGBTs. This approach was based

on the analysis of the equivalent IGBT switching circuit, thus describing the different turn-on and turn-off switching phases, via piece-wise linear modelling Moreover, this research presented the modified linear piece-wise modelling, to reflect the changes influenced by the implemented accelerated ageing. The second approach was based on the transient analysis, as provided by Rajapakse et al. [213] for new IGBTs, hence providing piecewise non-linear mathematical functions, which were modelled on the transients' characteristic variation with time, for the different turn-on and turn-off phases. Again, the non-linear model equations were modified, and new model equations were proposed, to include the influence of the implemented degradation. The first approach was useful to understand the influence of the IGBT's parasitic elements, on the switching transients, especially during the different turn-on and turn-off phases, which were governed by a linear relationship with time, both when new and after being subjected to degradation. The second approach was useful to obtain a more representative model of the IGBT's switching transients, including the different non-linearities that manifest both when the IGBT was new and after the IGBT was subjected to the implemented accelerated ageing. The observed significant turn-off slow-down, was determined to be due to the degradation in the die-attach, which led to an increase in the junction temperature (T_J), even though the case temperature (T_C) was maintained at room temperature (25°C). This heavily influenced the collector-current (I_C) turn-off transient, manifesting with an intensified presence of the "tail current". Indirectly, the manifested increase of the junction temperature (T_J), influenced as well, the operation of the IGBT's parasitic devices, predominantly the modelled increase of the collector-gate Miller capacitance (C_{CG}) during turn-off, manifesting in the elongation of the Miller plateau during turn-off. Moreover, it was postulated that the implemented accelerated ageing, influenced an increase in the input capacitance (C_{IES}), more specifically the gate-emitter capacitance (C_{GE}), through the contamination of the IGBT's gate dielectric oxide. This last postulate in conjunction with the compelling proposed changes, happening within the collector-gate Miller capacitance (C_{CG}), contributed in establishing a preliminary understanding, why the IGBT is manifesting significant slow-down during turn-off, but exhibiting insignificant changes during turn-off. Even though the measured changes in the threshold voltage (V_{TH}) are indicative of implanted charge carriers within the gate's dielectric oxide, the exact influence of the implemented accelerated ageing

procedure on the dynamic operation of the gate-emitter capacitance (C_{GE}), and consequentially, the complete understanding, of why the IGBT is manifesting a relatively unchanged turn-on, entails a more profound experimental investigation and modelling. These observations transcended from the proposed modified piecewise linear and non-linear IGBT switching transients' models, hence contributing towards a better understanding of the root causes, of the measured changes in the IGBT's transients and hence the corresponding influence on the EM conducted disturbances.

5. The final stage of this research presented the developed EM conducted emissions setup and procedure, which was centered around the IGBT's switching transients' characterization system, with the Double Pulse half-bridge circuit, serving as the EUT (hence employing an IGBT as the central commutation device within a standard power electronics circuit). This last research phase aimed at closing a circle, hence providing a holistic correlation between the electronic changes happening within the IGBT (both at the lower operational levels (physical electronics and static parameters) as well as the higher operational levels (switching parameters, switching transients, and switching power dissipation), the controlled inflicted degradation to the IGBT, and the EM conducted disturbances. The concurrent acquisition of the IGBT's signals (collector voltage (V_C) and collector current (I_C)) frequency domain spectra, and the EM conducted emissions for the CISPR16-1-1 A and B bands, for both the forward and return power lines, facilitated the establishment of this correlation. Hence it was shown, that an IGBT, manifesting a predominant degradation in the die-attach, leading to worsened heat dissipation capabilities, with the contribution of the gate oxide contamination, yield to a decrease in the EM conducted emissions of an EUT employing such IGBT, when compared to the EM conducted emissions of an EUT employing a new IGBT. This is to a certain extent, exclusively due to a slow-down of the IGBT's turn-off transients, primarily the collector current (I_C) transient.

7.2 Future Work

Different adaptations, experiments, and analyses of the conducted research have been left for the future. X-Ray imagery presented in Chapter 3, already established that the die-attach of the internal diode of the IGBT, experienced voiding and melting too, but not to the same extent as the IGBT's die-attach. This contributed to the measured changes in the internal diode's static and dynamic parameters. Hence, an evident continuation, of the research work conducted so far, will be, to isolate and measure the influence of the inflicted IGBT's internal diode degradation, on the EM conducted emissions. Moreover, it will be interesting to pursue this analysis, by assessing the combined utilization of the degraded IGBT and degraded internal diode, within a power electronic circuit and assess the corresponding influence on the EM conducted disturbance.

It will be interesting to extend the presented research approach, to IGBT modules and hence verify if the observed changes in the electrical and switching parameters of an IGBT transistor, and hence the corresponding measured EM conducted disturbances, are still valid for this scenario. Evidently the accelerated ageing and characterization setups will have to reflect the increased power handling and thermal capabilities of IGBT modules. Another interesting approach will be, to utilize an accelerated ageing strategy, which predominantly degrades the IGBT's bonding wires. This can be achieved by utilizing an accelerated ageing thermal profile, characterized by a relatively lower mean junction temperature (T_{J_AV}), but with large junction temperature (T_J) swings. The developed DC PCAS was designed, versatile enough, such that the proposed power cycling strategy, can be implemented with only minor changes within the accelerated ageing control and data acquisition software. The rest of the presented characterization hardware and software setups can be retained, if the IGBTs to be characterized have the same or similar electrical capabilities to the IGBTs utilized throughout this research. Moreover, the availability of a scanning electron microscope (SEM), will aid in evidencing the type and severity of the inflicted bonding-wire degradation.

Another appealing research path will be to investigate the impacts of the implemented accelerated ageing on the EM radiated emissions, especially from the near-field point of view. Since the presented work has already established, that there is an evident correlation between the inflicted degradation, the collector current (I_C) switching transient (predominantly the turn-off transient), and the EM conducted emissions, it is expected to obtain a similar correlation to the near magnetic field emissions. Limited work has been encountered in literature, which

investigates the research problem from a near-field point of view [179-180]. It might be useful to mention, that preliminary experiments have been conducted in this regard, by the author of this research, with the results agreeing with the expected outcomes. This was conducted by utilizing a near magnetic field probe, attached to the spectrum analyzer embedded within the MDO4104-B mixed domain oscilloscope, where the acquisition was triggered with the falling edge (turn-off) of the collector current (I_C), producing a distinctive disturbance in relation to the inflicted degradation. Even though the results obtained are promising, they are preliminary and hence these have not been presented in this work. The final idea is to obtain a non-invasive sensor, which can be also integrated within the IGBT package (for large packages) with the aim to detect the health state of the IGBT. The biggest challenge vis-à-vis, the radiated emissions, even from a near-field point of view, is to reliably isolate and discriminate from the emissions produced by neighboring electronic components, or other IGBTs, especially in the context of IGBT modules, where in a single package and hence a restricted space, there are multiple IGBT structures with their individual influence on the near-field disturbance. In this regard, the conduct disturbance approach is more reliable, with the evident drawback of being more invasive.

Finally, it will be interesting to pose the same research questions presented in this work, to the more recent silicon-carbide (SiC) IGBT technology, which provide an increased breakdown voltage and junction temperature (T_J) capabilities, when compared to silicon (Si) IGBT technology. This opens an entire research area, in relation to (SiC) IGBT's failure locations, mechanisms, detection and the corresponding prognostics, as well as understanding the best strategies of how to reliably degrade this IGBT technology for specific failure mechanisms.

Acronyms

ACEC	Advisory Committee on Electromagnetic Compatibility
AEC	Automotive Electronics Council
ARIMA	Auto Regressive Integrated Moving Average
AMN	Artificial Mains Network
BCI	Bulk Current Injection
BJT	Bipolar Junction Transistor
CDN	Coupling Decoupling Network
CE	Critical Energy
CHE	Channel Hot Electron
CISPR	Comité International Special des Pertubations Radioelectriques
CENELEC	European Committee for Electrotechnical Normalization
CM	Common Mode
DAHC	Drain Avalanche Hot Carrier
DC	Direct Current
DCB	Direct Copper Bonding
DI	Direct Injection
DM	Differential Mode
DMOS	Double Diffused Metal Oxide Semiconductor
DSMFT	Damped Sine Magnetic Field Test
DUT	Device Under Test
DUV	Deep Ultraviolet
EM	Electromigration
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ES	Energy Shock
ESD	Electrostatic Discharge
ESL	Equivalent Series Inductance
ESPRIT	Estimation of Signal Parameters via Rotational Invariance Technique
EST	Emitter Switched Thyristor
ET	Earth Terminal
ETP	Electromagnetic Transient Program
EUT	Equipment Under Test
FACTS	Flexible AC Transmission System
FCC	Federal Communications Commission
FCTF	Final Cycles To Failure
FFT	Fast Fourier Transform
FMEA	Failure Mode Effect and Analysis
FS-IGBT	Field Stop - Insulated Gate Bipolar Transistor
FTB	Fast Transient Burst

FTTF	Final Time To Failure
GCT	Gate Controlled Thyristor
GO	Gate Oxide
GRP	Ground Reference Plane
GTEM	Gigahertz Transverse Electromagnetic
GTO	Gate Turn-Off Thyristor
GUI	Graphical User Interface
HAST	High Accelerated Stress Test
HBM	Human Body Model
HC	Hot Carrier
HCI	Hot Carrier Injection
HCSD	High Current Short Duration
HGBS	High Gate Bias Stress
HS	Hot Storage
HTGB	High Temperature Gate Bias
HTOL	High Temperature Operating Life
HTSL	High Temperature Storage Life
HTRB	High Temperature Reverse Bias
HVDC	High Voltage Direct Current
IC	Integrated Circuit
IEC	International Electrotechnical Commission
IEGT	Injection Enhanced Gate Transistor
IGBT	Insulated Gate Bipolar Transistor
IGCT	Insulated Gate Commuted Thyristor
IMS	Insulated Metal Substrate
JEDEC	Joint Electronic Device Engineering Council
JFET	Junction Gate Field Effect Transistor
JTD	Junction Temperature Detection
LCLD	Low Current Long Duration
LDMOSFET	Laterally Diffused Metal Oxide Field Effect Transistor
LISN	Line Impedance Stabilization Network
LTSL	Low Temperature Storage Life
MCT	MOS-Controlled Thyristor
MOSFET	Metal Oxide Field Effect Transistor
MESFET	Metal Semiconductor Field Effect Transistor
NBTI	Negative Bias Temperature Instability
NPT	Non-Punch Through
OATS	Open Area Test Site
OTTF	Overall Time To Failure
PC	Power Cycling
PCAS	Power Cycling Ageing System
PSD	Power Semiconductor Device

PT	Punch Through
RBW	Resolution Bandwidth
RCA	Rain-flow Counting Algorithm
RCD	Residual Current Device
RDC	Ripple on Direct Current
RMS	Root Mean Square
RNN	Recurrent Neural Network
RTCA	Radio Technical Commission for Aeronautics
RUL	Remaining Useful Life
SAE	Society of Automotive Engineers
SC	Silicon Carbide
SCF	Short Circuit Failure
SCR	Silicon Controlled Rectifier
SCS	Short Circuit Stress
SEB	Single Event Burnouts
SEM	Scanning Electron Microscope
SES	Single Exponential Smoothing
SGHE	Secondary Generated Hot Electron
SJDTMOS	Super Junction Deep Trench MOS
SIT	Static Induction Transistor
SJ	Super Junction
SMU	Source Meter Unit
SO	Small Outline
SOA	Safe Operating Area
SOI	Silicon-On Insulator
SPCS	Switching Parameters Characterization System
SSO	Steady State Operation
STCS	Switching Transients Characterization System
TC	Thermal Cycling
TDDB	Time Dependent Dielectric Breakdown
TDR	Time Domain Reflectometry
TEOS	Tetraethoxysilane
TF	Thermal Fatigue
THBS	Temperature Humidity Bias Stress
TMCY	Temperature Cycling
TS	Thermal Shock
TSEP	Temperature Sensitive Electrical Parameters
UIS	Unclamped Inductive Switching
UHAST	Unbiased Humidity Accelerated Stress Test
UMOS	U-Shaped Metal Oxide Semiconductor
USB	Universal Serial Bus
VDMOS	Vertical Diffused MOS

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