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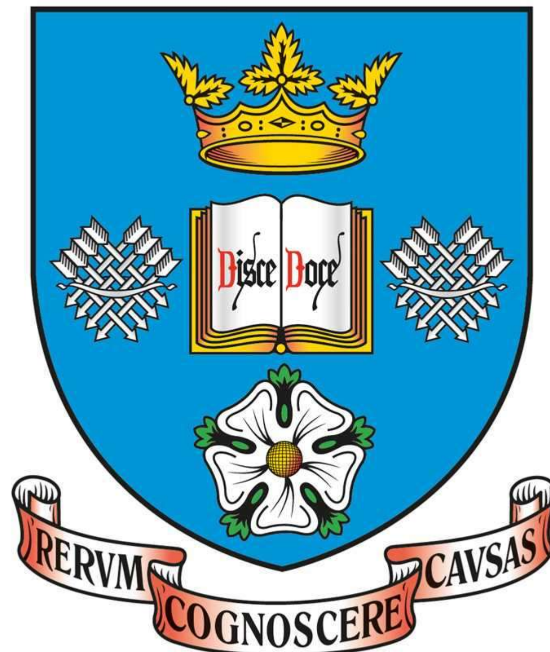

Development of a Current Limiting Solid-State Circuit Breaker Based on Wide-Band Gap Power Semiconductor Devices for 400V DC Microgrid Protection

By

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Abstract

Popularity of DC distribution systems is increasing for many residential and industrial applications such as data centres, commercial and residential buildings, telecommunication systems, and transport power networks etc. Compared to AC systems, they have demonstrated higher power efficiency, less complexity, and more readiness of integrating with various local power sources and DC electronic loads. However, one of the major technical issues hindering this trend is the lack of effective DC fault protection devices/circuits. Although conventional electromechanical circuit breakers work well in AC systems, they are not suitable for DC systems due to their long response time (ranging from tens of milliseconds to hundreds of milliseconds). Such a long response time is far beyond the withstand time (typically tens of microseconds) of most power electronic devices in short-circuit operating conditions. In contrast, Solid-State Circuit Breakers (SSCBs) are able to offer ultrafast switching speed thanks to the modern power semiconductor devices which can turn off in microseconds or even in tens of nanoseconds. Furthermore, the ever-increasing fault current level in DC systems poses a significant mechanical and thermal stress on the whole DC system. Therefore, the desire for the protection devices with the feature of fast switching speed along with the current-limiting capability has prompted intensive research in this area over the last decade in both academia and industry. However, the relatively high conduction losses and limited short-circuit capability are two of the major drawbacks of SSCBs. With the growing maturity and increasingly commercial availability of Wide-Bandgap (WBG) semiconductor devices, a SSCB based-on WBG devices is a promising solution to alleviate the issues since WBG semiconductors have demonstrated superior material properties over the conventional silicon material such as lower specific on-resistance, higher junction temperatures and higher breakdown voltage.

This research aims to design and develop a WBG-based solid-state circuit breaker for a 400V DC microgrid application. To accomplish this task, this work starts with a comprehensive review of DC microgrid technology followed by an extensive review of the state-of-the-art DC circuit breakers. Then, to develop a circuit topology for the proposed SSCB, a practical current limiter is analysed, simulated, and evaluated. Based on this topology, the proposed SSCB is configured with a high-voltage normally-on Silicon Carbide Junction Field Effect Transistors (SiC-JFETs) cascading a low-voltage normally-off power MOSFET. This solution offers several advantages. For example, it does not require any additional sensing and tripping circuitry for

short-circuit protection and therefore has a fast response speed. Meanwhile, the use of power SiC JFETs tends to reduce the conduction losses and enhance the short-circuit robustness of SSCBs. In addition, it offers the feature of current limiting which could ease the thermal and mechanical stresses on the whole DC system. The operating process of the proposed SSCB is analysed and the analytical results are compared with the simulated results; In the end, a prototype SSCB has been built and evaluated for short-circuit protection in a 400V DC system. In addition, to effectively suppress the overvoltage at the turn-off of SSCBs, a novel hybrid snubber circuit has been proposed by taking into account the advantages offered by both conventional Resistor-Capacitor-Diode (RCD) snubbers and Metal-Oxide Varistors (MOVs). Finally, other functions of the proposed SSCBs including overload protection, over temperature protection and protection coordination have been investigated and some operating issues such as false tripping and SSCB reset have been addressed.

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Chapter 1 Introduction

1.1 History of Competition between DC and AC technology

Dating back to the late 19th century, there was a bitter debate dubbed as 'war of currents' over the merits of DC and AC technology. Thomas Edison advocated DC technology while his rivals Nikola Tesla and George Westinghouse endorsed AC technology. To demonstrate the danger of AC power to the public, a controversial electric chair supplied by AC power was publicly used to execute a prisoner [1]. Despite all efforts to disgrace AC technology, DC eventually lost the 'war of currents'. As a result, Westinghouse Electric Company won some big projects such as power supply to the World's Fair in Chicago and construction of AC generators for a hydro-electric power plant at Niagara Falls. Since then, AC has been prevailing in the electric power industry.

One of the main reasons for AC to win the battle was that AC voltages could be stepped up to facilitate the power transmission over long distances and then stepped down to adapt to the end users by simply utilizing transformers. By contrast, there were no techniques for scaling up or down DC voltages. Consequently, DC systems were limited to a relatively low voltage level which resulted in significant power loss in long distance transmission due to the high-level current.

Since the first bipolar junction transistor (BJT) was invented at Bell Telephone Laboratories in 1948, modern power electronics have played a vital role in advancing the development of DC power systems. Today, DC voltages can be stepped up or down as easily as AC voltages using converters configured with power semiconductor devices. Compared to AC powers, DC powers have demonstrated many advantages to be presented in the next section. Nowadays, DC powers are gaining popularity for many residential and industrial applications.

1.2 Review of DC Microgrids

The concept of microgrid was first proposed in [2], which is a low-voltage (below 1kV) distribution system containing a number of local micro-sources. The aim of establishing microgrids is to meet local demands by directly connecting local distributed power sources to the end users and therefore avoiding costly extension of centralized power utility grids. Since the introduction of this concept, microgrids have been widely installed worldwide as a key solution for integrating local distributed sources in remote rural areas[3].

In recent years, DC power systems are progressively replacing conventional AC power systems in the distribution level of electrical networks[4][5][6][7]. DC microgrid becomes a preferred configuration integrating the renewable power sources such as Photovoltaic panels, wind power, storage batteries and stationary fuel cells with local loads. A large number of applications have been reported for residential and commercial buildings and industrial fields, for instance, telecom and data centres [8][9][10], residential and commercial buildings [11][12][13], electric vehicle fast charging stations[14] and ship networks[15].

1.2.1 DC microgrid configuration

DC microgrids are generally categorized into three types of configuration:1) single-bus 2) ring-bus 3) zonal configurations[16]. The decision to choose the configuration depends on a number of factors such as the control flexibility, reliability, voltage level, and costs etc. since each type of configuration has its advantages and limits.

- Single-bus configuration

This configuration is the most adopted in practical industrial applications. As shown in Figure 1.1, all power sources and various loads are connected to a single DC bus through either a converter or an inverter[17]. The main advantage of this configuration is its simplicity and low-cost. However, this topology has low reliability during fault conditions because a single fault on the bus can blackout all the end users.

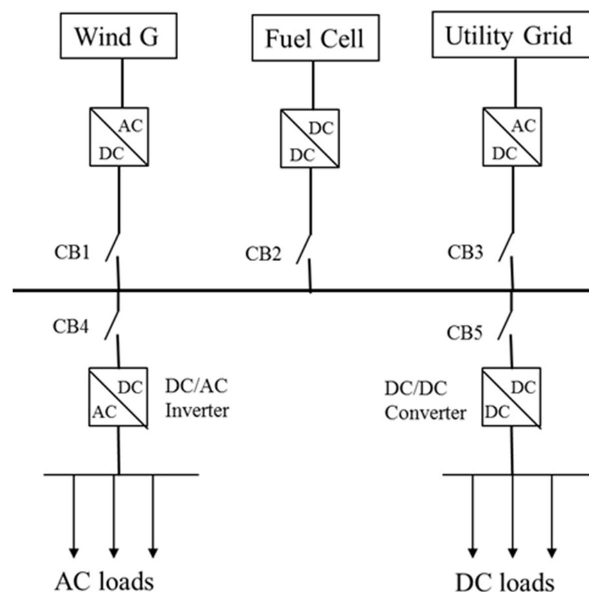


Figure 1.1 Single bus structure (adapted from [17])

- Ring-bus configuration

As shown in Figure 1.2, the ring-bus configuration is formed of a number of buses linked to a ring by Intelligent Electronic Devices (IEDs)[16]. When a fault occurs in any bus, the corresponding IEDs act to disconnect the faulty bus from the system and then supply the power to the customers using an alternative path. Compared to the single-bus configuration, the main advantage of this configuration is the higher reliability. However, both single-bus and ring-bus systems heavily rely on one main AC utility grid supply. If any fault leads to losing the AC power supply, the DC microgrid does not have sufficient power to maintain the normal load operation.

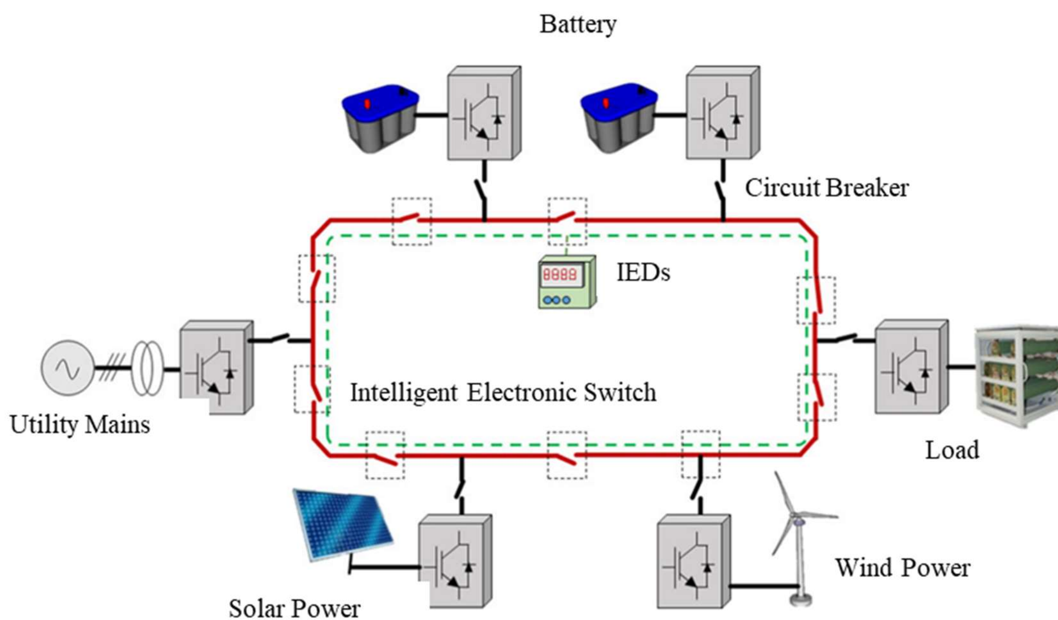


Figure 1.2 Ring bus Structure of DC microgrids ([16])

- Zonal configuration

As shown in Figure 1.3, the zonal architecture contains multiple zones powered by two main AC utility grid supplies and each zone connects to either of the two buses through the switches [18]. Loads in each zone can be flexibly powered by either bus. For example, in case of a fault occurring in the connected Bus 11, the corresponding switch S1 turns off and isolate the rest of system from the faulty bus. Then, the switch S2 connecting to the Bus 21 turns on and the load in this zone can continue to be served. Compared to the previous two configurations, this topology has the highest reliability and best flexibility. However, it is more complex and costs higher than the previous two configurations due to the requirement of a large number of switches.

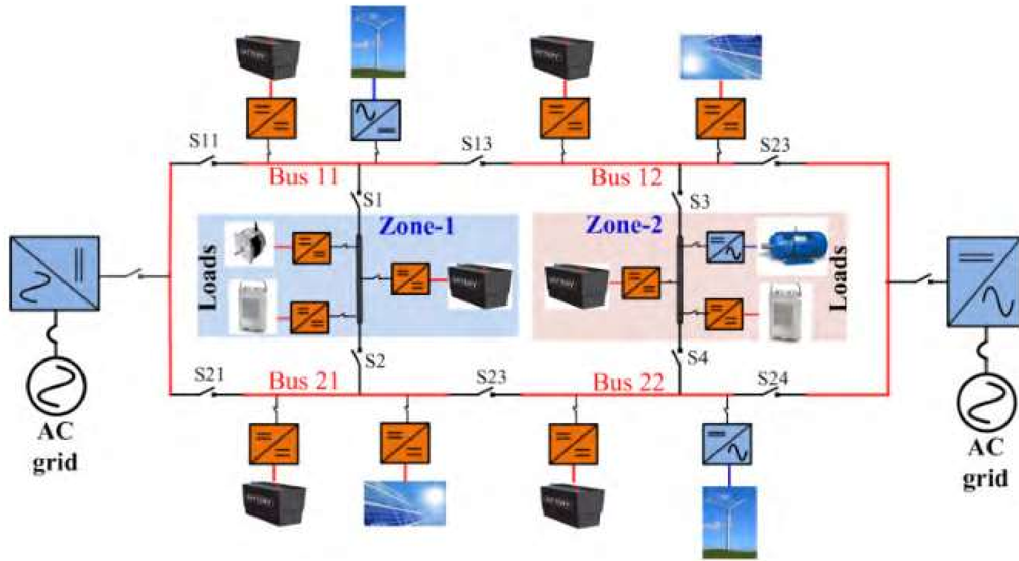


Figure 1.3 Zonal Structure of DC microgrids ([18])

1.2.2 Voltage polarity

Similar to single phase and three phases in AC systems, there are two types of DC wiring configurations: unipolar wiring and bipolar wiring as shown in Figure 1.4 [19]. In contrast to the two poles in a unipolar configuration: positive pole and negative pole, a bipolar DC system has a third pole: neutral pole. Therefore, the bipolar topology offers a higher reliability and more choices of voltage level than the unipolar wiring. However, it needs to address the voltage imbalance issue caused by the unequal loads.

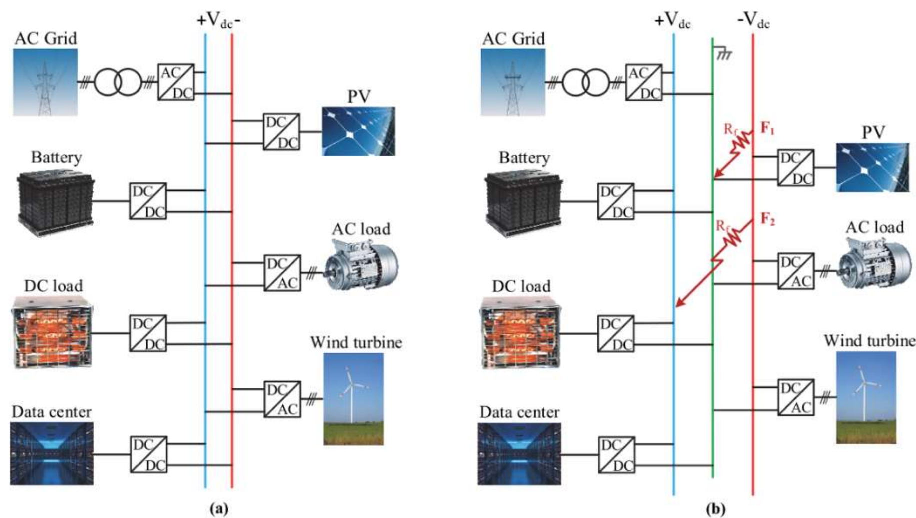


Figure 1.4 DC voltage polarity (a) Unipolar (b) Bipolar ([19])

1.2.3 Grounding

Design of grounding for DC microgrids needs to consider a number of factors such as grid reliability, stray current, safety of equipment and personnel and ground fault detection[20]. According to IEC 60364-1 standard: low-voltage electrical installations [21], low-voltage DC grounding systems can be classified into three types of topologies: TT, TN and IT. The letters T, I and N denote direct connection of the earth, isolation from the earth and connection to the neutral line respectively.

Figure 1.5(a) shows the TT grounding system where the neutral point of the converter and the exposed conductive parts of the equipment are separately connected to the Protective Earth (PE). The advantage of TT grounding system is that the fault will not shift to other parts of the grid whereas there exists an potential high voltage stress[22].

In the TN configuration, the middle point of converter is grounded while exposed conductive parts of equipment is connected to the neutral line. Depending on the way of connection to the neutral line, TN topology can be further sub-divided into the following three types:

TN-S:

N and PE conductors are separated throughout the system as shown in Figure 1.5 (b).

TN-C:

N and PE are merged into a single conductor throughout the system, as shown in Figure 1.5(c).

TN-C-S:

A hybrid of TN-C and TN-S as shown in Figure 1.5 (d).

Each sub-TN configuration has its own pros and cons. Overall, the advantages of the TN grounding topology include minimal touch potential, easy detection of the ground fault and less overvoltage stress on equipment insulation. However, TN grounding system would produce high current transients under a low-resistance ground fault[20].

In the IT configuration as shown in Figure 1.5(e), the middle point of the converter is isolated from the earth and the exposed conductive parts of the appliance are connected to the earth through PE. This grounding system has low current transients and can continue to operate for a certain amount of time under a single pole-to-ground fault. However, the high overvoltage

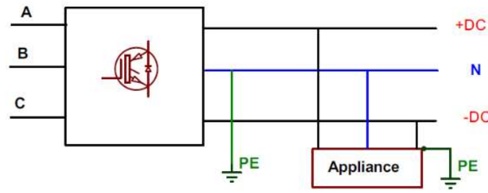
caused by one pole grounded fault may pose a threat to personnel and equipment safety. Moreover, it is difficult to detect ground fault due to the small grounded fault current[23].

Furthermore, grounding methods in DC source sides are broadly divided into ungrounded, solidly grounded and grounded with a resistor [24]. The main advantages of the ungrounded system are the simplicity and the continuous service during a single grounded fault. However, there are concerns about personal safety and the difficulty of detecting ground fault. By contrast, the solidly grounded system has the advantages of personal safety, low level of insulation requirement and easy fault detection[25]. Nevertheless, it is rarely adopted in modern DC systems due to the corrosion and disturbance on telecommunication induced by high fault current. To take advantages of both the above grounding topologies, a resistor is often added between the neutral point of the system and the earth. However, the high value of resistance would slow the protection speed[26].

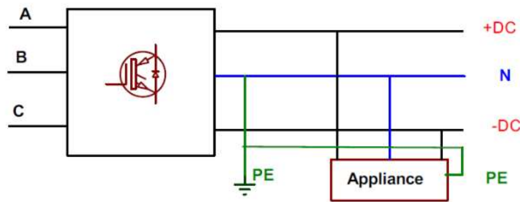
In the end, Table 1.1 summarises advantages and disadvantages of grounding topologies.

Table 1.1 Comparison of three grounding topologies

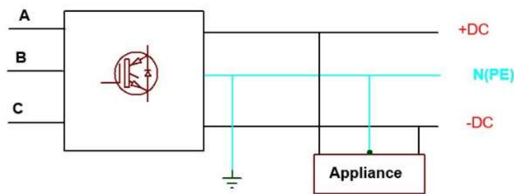
Grounding method	**Advantages**	**Disadvantages**
TT	• Simple installation • Easy detection of ground faults	• Current circulation • Potential high voltage stress
TN	• Minimal touch potential • Easy detection of ground faults • Less overvoltage stress	• High current transients under low-resistance ground faults
IT	• Low current transients • Continuous service under a single phase-to-ground fault	• Difficult detection of ground faults • High overvoltage under a ground fault



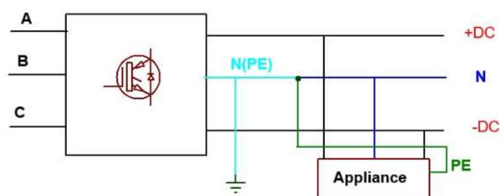
(a) TT



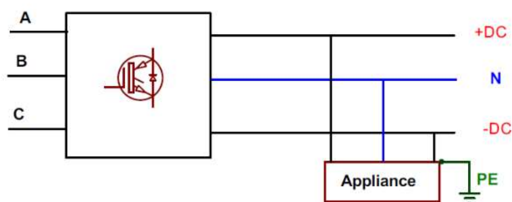
(b) TN-S



(c) TN-C



(d) TN-C-S



(e) IT

Figure 1.5 DC grounding configurations (adapted from [22])

1.2.4 Voltage level standards applied for DC microgrids

Apart from the protection issue, the lack of international standards and guidelines for regulating DC voltage level is another hurdle to deter the development of DC microgrids [16]. Several regional and international organizations have been working in this area. For example, ETSI, an European standard organization for the telecommunication industry set out the standard ETSI EN 300 132-3-1 for telecommunications and data equipment with DC voltage level between 260V and 400V[27]. International Electrotechnical Commission (IEC) organized a dedicated Strategic Group (SG) to study the standards for low voltage DC systems of up to 1500V[18]. In addition, International Telecommunication Union (ITU) has recommended a series of standards for up to 400 V DC systems applied for information and technology (IT) equipment in telecommunication centres, data centres and customer premises. Currently, the most commonly used voltage levels in DC microgrids are in range between 270V and 1500V. Although the debate on the optimal voltage level for DC microgrids is still open, 400V level appears to be the preferred one for data/telecom centre, EV charging, residential building and commercial building applications while 12V, 24V and 48V DC voltages are commonly selected for lower voltage ratings applications such as LED lights, motors and PV [18].

1.3 Benefits of DC Power over AC Power

In comparison to AC microgrids, DC microgrids have established some key advantages as follows [28][29][30]:

A. Easier integration of ever-increasing distributed generation sources

There have been increasing demands to accommodate renewable and other distributed sources. Many distributed power sources such as photovoltaic, fuel cells and batteries are inherently DC powers which can be either directly or through converters connected to DC power systems. Furthermore, AC distributed sources including wind and small capacity gas generators can also be conveniently integrated in a DC system through AC/DC converters without a complicated synchronization process as required by AC systems. Therefore, compared to AC power, DC power has significant benefits for applications where various local distributed sources need to be incorporated.

B. More efficiency for incorporation of fast-growing DC electronic loads

There are widespread and fast-growing DC loads in commercial buildings and households, such as LED lighting, Information and Technology (IT), and adjustable-speed DC motors. The supply

of DC power to DC loads can offer high efficiency and low-cost through eliminating conversion steps between sources and loads.

C. Higher reliability for critical loads

Critical loads such as banks and data centres require to operate 24/7 without disruption regardless of any unexpected power outages. To achieve this, either online uninterruptible power supplies (UPS) or backup power generators are commonly installed to supply powers to these critical loads during the unexpected power cut. As shown in Figure 1.6, compared with AC UPS, DC UPS offer more reliability and higher efficiency due to eliminating the additional DC/AC conversion step[31].

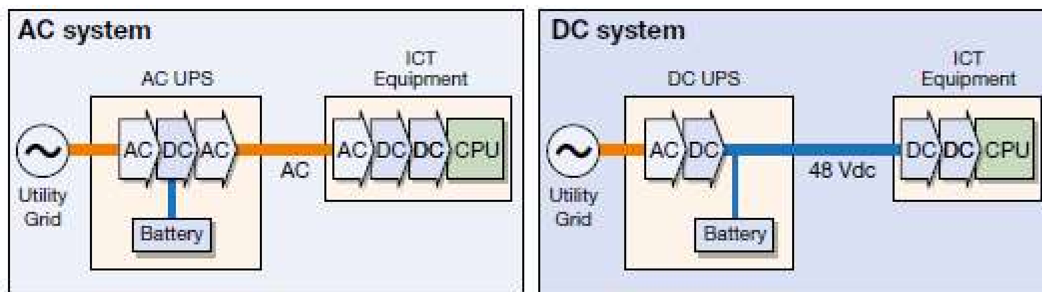


Figure 1.6 Comparison of UPS installed in AC and DC system [31]

D. Higher power quality

In AC grids, DC loads are powered through rectifiers. Consequently, non-sinusoidal currents would be injected or fed into the AC grid and therefore deteriorate power quality. By contrast, the elimination of rectifiers between DC sources and DC loads would improve power quality alongside with good design practices.

E. More safety

Although the arguments of which form of power is safer are still open, DC powers are generally considered to be less dangerous to the public than AC powers since human bodies tend to be more susceptible to time-changing AC stresses than constant DC ones. This can be implied by the safety voltage levels listed in Table 1.2, where DC safety voltages more than double that of AC counterparts under the same conditions.

Table 1.2 Safety Voltages

	Direct contact	**Indirect contact**
Alternating current (rms)	25V	50V
Direct current	60V	120V

F. Transmit more active powers

In contrast to no reactive components in DC power transmission, AC power transmission suffers from reactive power flow leading to less transmissible effective power. This can be evidenced by the following simple calculations.

For an AC system (three phases), the total transmissible real power can be calculated as:

$$P_{AC} = \sqrt{3}.V_{AC}.I_{AC}.\cos\varphi \quad (1.1)$$

where $\cos\varphi$ is power factor of AC loads and V_{AC} is line to line voltage.

For a DC system (three poles), the total transmissible real power can be calculated as:

$$P_{DC} = 2.V_{DC}.I_{DC} \quad (1.2)$$

where V_{DC} is the voltage between either the positive or negative pole and neutral conductor.

For the comparison between AC and DC systems, the following assumptions are made:

$V_{AC} = V_{DC}$, $I_{AC} = I_{DC}$ and $\cos\varphi = 0.9$

Hence, the relationship of DC and AC maximum active powers can be figured out in the following:

$$\frac{P_{DC}}{P_{AC}} = \frac{2.V_{DC}.I_{DC}}{\sqrt{3}.V_{AC}.I_{AC}.\cos\varphi} = 1.28 \quad (1.3)$$

The result demonstrates that DC systems can transport 1.28 times effective power than that in AC systems under the above assumption.

G. More cost-savings

Due to the skin effect that alternative current tends to flow at the outer portions of the conductors, the conductors in AC cables have to either increase their size or adopt twisted bundles of thinner conductors to accommodate an equal amount of currents as DC cables at the expense of higher cost. Moreover, under the same voltage level, the insulation level of DC systems is designed against maximum constant DC voltage whereas AC insulation level must be designed against the higher sinusoidal peak voltage at the higher cost.

1.4 Challenges of DC Power Protection

Despite the aforementioned advantages over AC systems, DC systems have not yet been widely deployed. Apart from some economic reasons such as high cost of power converters and control equipment, DC short-circuit protection remains a significant technical barrier [32][33]. There are two significant challenges presented as follow.

Challenge 1: High magnitude and high derivative (di/dt) of DC fault currents [34]

Generally, there are two types of faults in DC power systems:1) line to ground 2) line to line (short-circuit) faults. Short-circuit faults are most severe while line to ground faults are most frequent in DC distribution systems [35]. DC faults could occur in various locations for example source side, the DC bus or load side caused by either internal or external faults such as cable faults, components failure and switching devices overshoot. Due to lack of high inductance components in DC systems, short-circuit current would rise to high magnitude within a very short period. In addition, DC systems are highly capacitive since large DC-link capacitor banks are deployed to smooth output voltage ripples. Once a short-circuit fault occurs, these large capacitors would discharge and produce high transient currents that might lead to failure of vulnerable components[36]. Therefore, when designing the protection system or selecting appropriate protection devices, it is essential to comprehensively understand DC fault characteristics and estimate the fault current level for a given location.

As previously described in the section 1.2, in a DC microgrid, multiple AC or DC sources are either directly connected to DC buses or through power converters. The total short-circuit current is superimposed by the fault currents from all active sources with their contributions determined by the effective impedances between the corresponding source and the fault location[37]. For example, when a fault occurs at a DC bus, the contribution of a battery source directly connecting to the DC bus can be presented as [32]:

$$i_{bat(t)} = \frac{V_{bat}}{R_{bat}+R_{cable}}\left(1 - e^{-\frac{R_{bat}+R_{cable}}{L_{bat}+L_{cable}}t}\right) \quad (1.4)$$

where V_{bat} is the battery charged voltage, R_{bat} and L_{bat} are battery internal resistance and inductance respectively, while $R_{cable}$and L_{cable} are connection cable resistance and inductance respectively. Instead, when a power source is connected to the bus through a Voltage Source Converter (VSC) [38], the contribution from quick discharge of its output capacitor plays a dominant role, which can be calculated as [35]

$$i_t = \frac{V_0}{\omega L} e^{-\delta t} \sin \omega t - \frac{I_0 \omega_0}{\omega} e^{-\delta} \ \sin(\omega t - \beta) \quad (1.5)$$

Where R and L are the resistance and inductance of the connection cable between the converter and the fault location respectively, and

$\delta = R/2L$, $\omega = \sqrt{1/LC - (R/2L)^2}$, $\omega_0 = \sqrt{\delta^2 + \omega^2}$ and $\beta = \tan^{-1}(\omega/\delta)$

However, when the capacitor voltage reaches zero, the fault current commutates to the freewheeling diodes of VSC which have limited overcurrent capability. Therefore, the fault current must be quickly detected and cleared before the diodes reach their thermal limits[32].

Finally, total fault current can be obtained by superimposing the contributions from all sources [16].

$$i_{fault}(t) = i_{bat(t)} + \sum_{j=1}^{N} i_j(t) \quad (1.6)$$

where N is the number of sources connected to the DC bus through the power converters.
Take an example of calculating DC fault current. As shown in Figure 1.7, a simplified equivalent circuit of a DC grid includes a circuit breaker CB, a DC source V_{DC} and a cable represented by a resistor R and an inductor L. When a short-circuit fault occurs in the load side, fault current i_{sc} and rising rate $\frac{di_{sc}}{dt}$ can be simply calculated from the equations below:

$$i_{sc} = \frac{V_{DC}}{R}\left(1 - e^{-\frac{t}{L/R}}\right) \quad (1.7)$$

$$\frac{\mathrm{d}i_{sc}}{\mathrm{d}t} = \frac{V_{DC}}{L} e^{-\frac{t}{L/R}} \quad (1.8)$$

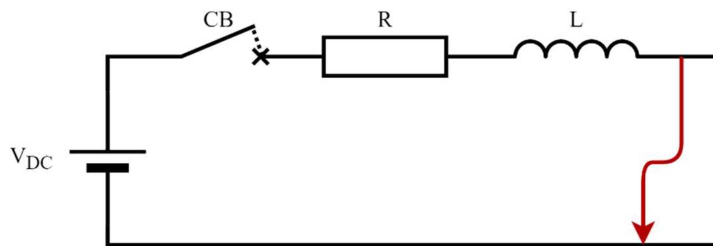


Figure 1.7 Simplified equivalent circuit of a DC grid

Now the cable inductance and resistance can be calculated below:
As shown in Figure 1.8, given the radius (r) and length (l) of the cable and separation distance (d) with the paralleling cable, the cable inductance and resistance can be calculated respectively[38].

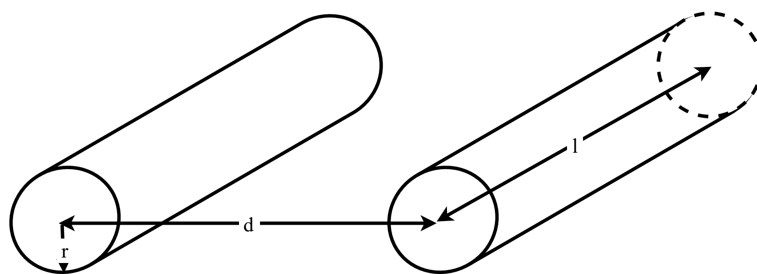


Figure 1.8 Cross-section of the cable

1) Self-inductance in μH:

$$L_{self} = 0.2l(\ln\frac{2l}{r} - \frac{3}{4}) \tag{1.9}$$

2) Mutual inductance in μH:

$$M = \frac{\mu l}{2\pi}\left[\ln\left(\frac{l}{d} + \sqrt{1 + (\frac{l}{d})^2}\right) - \sqrt{1 + \left(\frac{d}{l}\right)^2} + \frac{d}{l}\right] \tag{1.10}$$

where μ is the permeability of the medium between the cables, $\mu_0 = 0.4\pi\ \mu H/mm$ in vacuum or air.

3) Total inductance in μH:

$$L_{total} = 2(L_{self} - M) \tag{1.11}$$

4) Cable resistance in mΩ:

$$R = \rho\frac{2l}{A} \tag{1.12}$$

where ρ is the resistivity of the material and A is the cross-sectional area of the conductor. Table 1.3 provides American Wire Gauge (AWG) sizes and its corresponding electrical parameters.

Table 1.3 AWG wire sizes

Wire size (AWG)	**Wire area (mm^2)**	**Wire radius (mm)**	**Resistance/per meter (mΩ/m)**	**Maximum current (A) at up to 60ºC**	**Short-time current (kA) up to 1s**
0	53.5	4.1	0.3	125	16
2	33.6	3.3	0.5	95	10.2
4	21.2	2.6	0.8	70	6.4
6	13.3	2.0	1.3	55	4.0
8	8.4	1.6	2.1	40	2.5
10	5.3	1.3	3.3	30	1.6
12	3.3	1.0	5.2	20	1.0

Assuming a cable size of AWG 2 and 10cm spacing between two parallel cables, given the cable length, the total inductances and resistance can be calculated using Equation (1.11) and (1.12). The result is shown in Figure 1.9. Given a short-circuit fault at the location of 20 meters away from the DC power source, the total short-circuit resistance and inductance are obtained as 20 mΩ and 35 μH respectively. When V_{DC} =400 V, peak fault current and maximum rising rate can

be calculated from Equation (1.7) and Equation (1.8) as 20 kA and 11A/μs respectively. Such high magnitude and fast-rising fault current would result in a significant amount of thermal and electro-mechanical stresses on the system. Therefore, it is desirable that DC protection devices have features of both fast-switching speed and current-limiting ability.

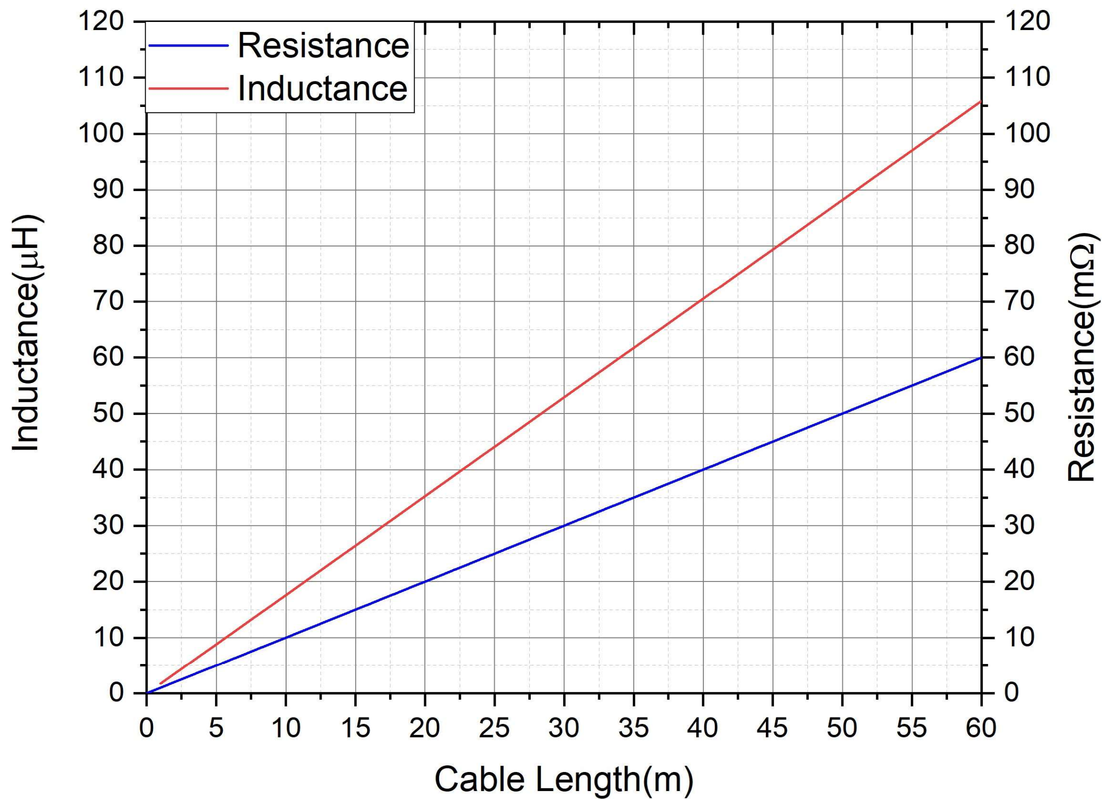


Figure 1.9 Cable inductance and resistance against cable length

Challenge 2: DC currents without zero-crossing points

Unlike AC currents, DC currents do not periodically go to zero. For this reason, traditional AC electromechanical circuit breakers cannot be directly used for protecting DC system since they require current passing the zero-point for extinguishing arc when switching off. To address this issue, an auxiliary circuit is commonly added to force DC currents to pass zeros. Despite all the efforts, traditional electromechanical circuit breakers are not suitable for DC protection due to its inherent slow switching speed.

1.5 Fault Protection Devices for DC Power Systems

DC protection devices can be broadly classified into three groups: fuses, current limiters, and circuit breakers, which are briefed as follow.

1) Fuses

Fuses as the simplest and oldest fault protection devices, were first used as early as in the 19th century [39]. Figure 1.10 illustrates a cross-section of one typical fuse[40]. As can be seen, it contains a metal fuse link element connected to the two electrical terminals, housed by a ceramic body filled with heat-absorbing granular quartz. Under a fault condition where the current reaches a certain value, the fuse link starts to melt and then open the circuit. However, fuses are one-off devices and must be replaced once it is blown up. In addition, it is rarely used for high reliability applications due to its unpredictable fusing time affected by circuit time constant [41].

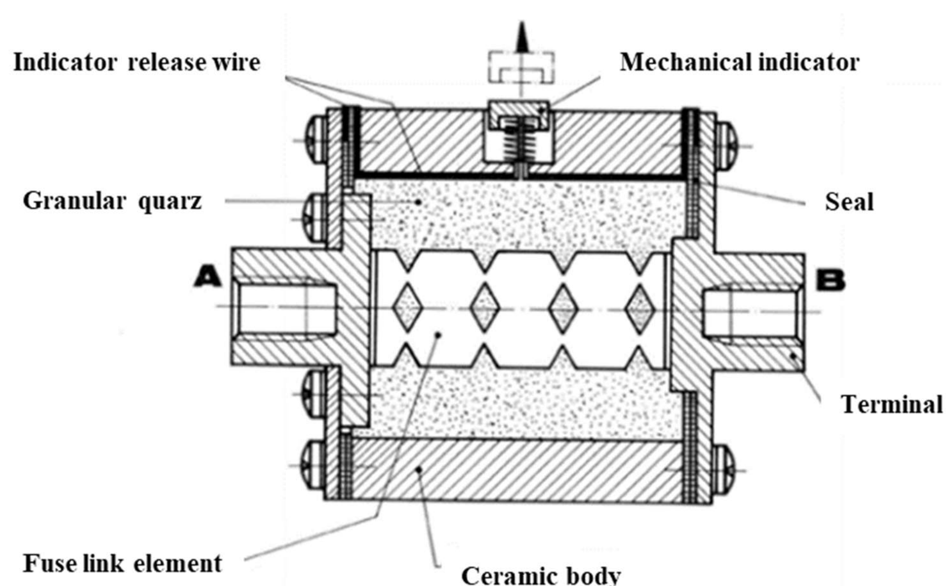


Figure 1.10 Cross-section of a fuse [40]

2) Current limiters

Most current limiters operate to limit fault currents by introducing a high resistance in the fault path when a fault occurs. For example, a superconductor was first proposed as current limiting mechanism in 1995[42] due to its excellent electrical properties such as negligible resistance below a critical temperature and a relatively high resistance above the critical temperature. Similarly, a current limiter using Positive Temperature Coefficient (PTC) thermistors was introduced in 1996 [43]. PTCs are thermally activated resistors whose resistance increases with the elevated temperature caused by the surge fault current. In addition, depletion-mode power

semiconductor devices can also be used as a basic two-terminals current limiter by tying theirs gate and source terminals together. Under a normal operating condition, the semiconductor device operates in the linear region and its on-state voltage drop is negligible. When a fault occurs, the rising fault current drives the device to operate in the saturation region where the current is limited by its channel pinch-off and self-heating. In 1996, [44] proposed a current limiter for voltage between 400V to 1kV based on a depletion mode silicon MOSFET. In 2002, a depletion mode silicon JFET-based 400V current limiter was reported in [45]. In 2016, a bidirectional current limiter using 1.2kV SiC JFETs was fabricated and studied in [46].

The adoption of current limiters can significantly reduce both thermal and electrical stresses on the entire system. However, current limiters are commonly used along with circuit breakers since the fault current must be interrupted before the current limiter reaches its thermal limit. For example, as shown in Figure 1.11, a superconductor fault current limiter(SFCL) integrated into a 250kV/2kA hybrid circuit breaker was proposed in [47] where SFCL is used for automatic fault current limiting before the fault is interrupted by the main DC breaker. During normal operation, the Ultrafast Disconnector Switch (UDS), Line Commutation Switch (LCS), and Residual Current Breaker (RCB) are closed and conduct load current while the Main Circuit breaker (MCB) is opened. When a fault occurs, the SFCL limits the fault current. In the meantime, the MCB is closed, and the LCS starts turning off. The current is commutated to the MCB. Once the current is completely shifted to the MCB, the UDS opens and isolates the LCS from exposing high voltage. Then, the MCB opens, redirecting the current to the surge arresters where the fault current is damped to zero. Finally, the RCB opens and isolates the high voltage.

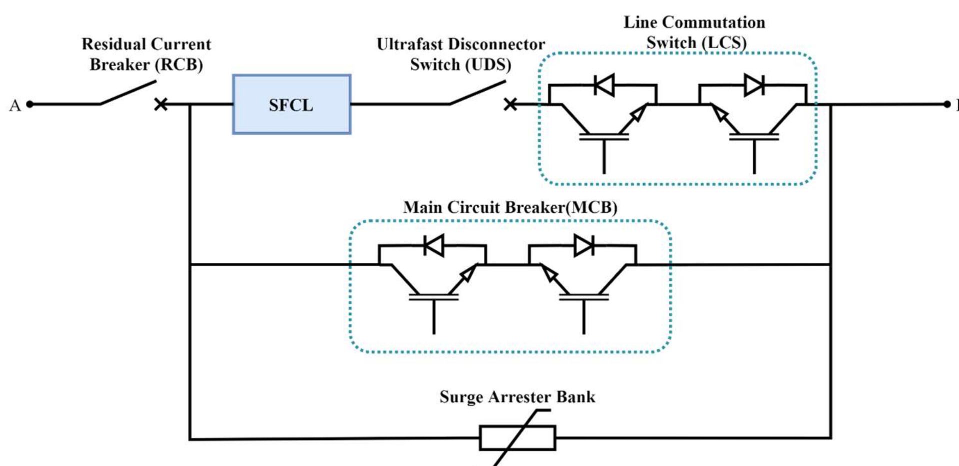


Figure 1.11 Hybrid circuit breaker with a superconductor current limiter (adapted from [47])

3) Circuit breakers

Circuit breakers have been the main protection devices for both AC and DC power systems due to their reliability and operability. According to their operation mechanism, circuit breakers are broadly categorized into three types: Electro-Mechanic Circuit Breakers (EMCBs), Solid State Circuit Breakers (SSCBs) and Hybrid Circuit Breakers (HCBs).

Over the past several decades, some efforts were made to transform AC EMCBs for DC applications. For instance, either passive or active resonance circuits are added to take the fault current to cross zero point. One of main advantages of EMCBs is relatively low conduction losses owing to its metal contacts. However, EMCBs suffer slow response time in the range of tens of milliseconds and also need regular maintenance as a result of arc erosion. By contrast, semiconductor based SSCBs have demonstrated an ultrafast response speed (less than hundreds of microseconds) However, its relatively high conduction losses and limited short-circuit capability remain the main issues to be addressed. The HCB solution combining a fast-mechanical switch with a SSCB, attempts to take benefits of both EMCBs and SSCBs. However, its switching speed is restricted by the mechanical parts and therefore it is difficult for a HCB to switch less than 100 microseconds.

With the growing maturity and increasingly commercial availability of Wide-Bandgap (WBG) semiconductor devices, SSCBs based-on WBG devices are considered to be a promising solution for DC protection since WBG semiconductors have demonstrated superior material properties over conventional silicon material such as lower specific conduction losses, higher junction temperatures and higher short-circuit capability.

1.6 Objective of this Research

The main objective of this research is to develop a WBG-based solid-state circuit breaker applied for 400V DC microgrids. To accomplish this task, this research focuses on the following aspects:

- Gain a comprehensive understanding of DC microgrid and state-of-the art SSCBs through an extensive literature review.
- Research and develop a circuit topology for ultrafast short-circuit protection through analysis, simulation, and experiment.
- Select commercial WBG power devices and develop SPICE models for SSCB applications.
- Design a snubber circuit for suppressing overvoltage at the turn-off of SSCBs.
- Build a prototype SSCB and evaluate it in a 400V DC system.
- Investigate other protection functions of SSCBs such as overload and over temperature protection.

- Address some issues during the SSCB operation such as false tripping caused by inrush currents and SSCB reset.

1.7 Main contributions of this research

The main contributions presented in this thesis include three aspects:

1) Developing a unique circuit topology to achieve an ultrafast response speed and current-limiting function

This unique circuit developed from a current limiter, is configured with a high-voltage normally-on SiC-JFET and low-voltage normally-off Si MOSFET. The proposed circuit for short-circuit protection offers several advantages. First, it does not require complicated and time-consuming sensing and tripping circuitry and therefore offers an significant fast response speed. In contrast, most SSCBs reported in the literature rely on dedicated fault current sensing circuit and complex communication system to response for short-circuit faults. Secondly, with this configuration, the fault current is limited below the tripping current level which is adjustable to meet the requirement of different applications. Thirdly, the normally-on SiC JFET offers both low specific on-resistance and exceptional robustness under short-circuit conditions. Finally, the number of components used for this circuit is kept minimum and therefore the solution is cost-effective and has high reliability.

2) Proposing a novel snubber circuit for suppressing overvoltage at the turn-off of the SSCB

A hybrid snubber circuit by combining an RCD with a MOV has been proposed. It explores the advantages of both effective overvoltage suppression of conventional RCD snubbers and high energy absorption capability of MOVs. Meanwhile, it eliminates the high-power resistor of RCD snubbers and mitigates the transient fluctuation of MOVs. In addition, analytical expressions describing each stage of the operating process provide guidance for the snubber design applied for SSCBs. In the end, the impact factors involved in the snubber on the response time of SSCBs have been identified and an equation has been given to optimise the snubber design to meet different application requirements. This work encompassed in Chapter 5 has been published in IET Power Electronics.

3) Providing an in-depth analysis and mathematical expressions for the Transient Block Unit (TBU)

The operating processes of the basic TBU, the basic TBU with two added resistors, the basic TBU with an added enhancement mode MOSFET, and three typical practical TBUs have been analysed in details and their corresponding output characteristic expressions have been derived,

which have laid a solid foundation on the development of the circuit topology for SSCB applications.

1.8 Outline of the Thesis

Chapter 2: This chapter provides an extensive review of DC circuit breaker technologies, especially solid-state circuit breakers and hybrid circuit breakers. In the first instance, the functionality and main parameters of a circuit breaker are discussed. In the following, the protection process and the key time periods during the process are illustrated. Then, the typical configuration of three topologies: EMCBs, SSCBs and HCBs are presented, and their advantages and limitations are discussed. Finally, both SSCBs and HCBs based on various semiconductor devices in the literature are thoroughly reviewed.

Chapters 3: This chapter gives insight into the operating principles of a current limiter called Transient Blocking Units (TBUs) from Bourns Inc and therefore paves the way for the development of a circuit topology for the proposed SSCB. First, an analysis of the static performances of the basic TBU is presented, with the output analytical expressions derived in multiple stages. In the following, the analytical results are validated by the simulation results. Finally, practical TBUs sourced from Bourns Inc are analysed and evaluated by both the simulation and experiment.

Chapter 4: In this chapter, to start with, the principal functions and technical specifications for the proposed SSCB are defined. In the following, the selection of commercial power semiconductor devices is conducted through the comparison of datasheet, simulation, and experiment. Then, the selected power device is characterized, and its original SPICE model is developed for SSCB applications. Finally, the thermal design of selected devices is conducted and devices in parallel are investigated.

Chapter 5: This chapter proposes a novel snubber circuit for 400V DC SSCBs. It takes the advantages of effective overvoltage suppression of RCD snubbers and high energy absorption capability of MOVs. The operating process of the proposed snubber circuit is analysed and then a snubber circuit for 400V DC SSCBs is designed and built. Finally, the effectiveness of the proposed snubber circuit is validated by both simulation and experimental results.

Chapter 6: In this chapter, an ultrafast SSCB for short-circuit protection is developed using a high-voltage normally-on SiC-JFET and low-voltage normally-off Si MOSFET based on the circuit topology of TBUs presented in Chapter 3. Initially, the requirement on DC short-circuit

protection design are discussed. In the following, the operating principle of the proposed SSCB is analysed and validated by the simulation. Then, a prototype SSCB is built and evaluated in a 400V DC system Finally, the protection coordination, inrush current issue and SSCB reset are investigated and addressed.

Chapter 7: This chapter presents the design, simulation and experiment for overload and over-temperature protection of SSCBs. It starts with the design, simulation and experiment of overload protection, especially time-current tripping curve design. Then, the over temperature protection is investigated, including the review of the methods for measuring device junction temperature, the choice of temperature-sensitive electrical parameters for the device and the practical circuit for real-time junction temperature monitoring. Finally, the realization of overload and over temperature protection are discussed.

Chapter 8: This chapter summarise this thesis and provides suggestion for future work.

1.9 List of Publication

- Z. Wang and E. M. S. Narayanan, "Design of a snubber circuit for low voltage DC solid-state circuit breakers," IET Power Electronics 2021
- Z. Wang and E. M. S. Narayanan, "Development of Current Limiting Ultra-Fast Solid-State Circuit Breakers," 47th Annual Conference of the IEEE Industrial Electronics Society (IES), IEEE IECON 2021

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Chapter 2 Review of DC Circuit Breaker Technologies

2.1 Basic Requirements and Main Parameters of a DC Circuit Breaker

International Electrotechnical Commission (IEC) defines a circuit breaker as "*A device, capable of making, carrying and breaking currents under normal circuit conditions and also making, carrying for a specified duration and breaking currents under specified abnormal circuit conditions such as those of short circuit.*"[1].The definition suggests two main functions as a circuit breaker: One is to conduct load current under normal conditions and another is to interrupt current under fault conditions.

2.1.1 Requirements on a DC Circuit Breaker

The requirements on a DC circuit breaker should be as below [2]:

a) **Fully controllable**

The state of the circuit breaker can be controlled by either mechanical or electronic/electrical means.

b) **Fast switching speed**

Circuit breakers should interrupt the fault current as fast as possible to protect components from a long exposure to the fault current.

c) **Low power loss**

Conduction loss under normal operating conditions should be minimized to reduce the requirement on cooling auxiliaries.

d) **Minimal arcing**

-During the process of interrupting the fault current, the electrical arc between the contacts should be minimized or prevented to ensure safety and longer life span.

2.1.2 Technical parameters

The technical specifications of a DC circuit breaker can be characterized by the following main parameters[3][4]:

- **Rated Voltage**

The maximum voltage at which the circuit breaker can operate safely.

- **Rated Current**

The maximum current that a circuit breaker can continuously carry under normal operating conditions.

- **Rated short-circuit breaking current**

The highest current value that the circuit breaker can break without being damaged.

- **Energy let-through capability I^2t**

Integral of the square of the current over a given time interval reflecting the maximum thermal energy a circuit breaker can contain without being damaged.

- **Maximum on-state voltage**

Maximum voltage drops across the circuit breaker under the rated current at the maximum allowed temperature.

- **Break time**

The time interval from the beginning of the opening operation of a circuit-breaker and the end of the arc extinction.

- **Response time**

The time interval from the moment at which the fault occurs to the point where the fault current is completed isolated.

2.2 Overcurrent Protection Process of a DC Circuit Breaker

The key functionality of a circuit breaker is to interrupt the fault current and isolate the fault. Figure 2.1 shows a typical process of overcurrent protection of a circuit breaker. During the normal operation, the circuit breaker stays on-state and conducts the load current i_L. When a fault occurs at t_0, the fault current rapidly rises until reaches the overcurrent threshold i_{th}.at t_1. A tripping signal is sent out to trigger the circuit breaker. After a short signal transmission time, at t_2, the circuit breaker receives the trip command and starts turning off. At t_3, the breaker is opened. The voltage across the circuit breaker starts building up until it reaches a certain value activating the voltage clamping circuit and the voltage is clamped to a safe level for the circuit breaker. In the following, the fault current is commutated to the overvoltage clamping circuit such as a snubber circuit or a MOV where the energy is dissipated, and the fault current is damped to zero at t_4.

Based on this process, several important time periods are defined in Table 2.1. As can be seen from the table, the complete response time T_{res} is a summation of the fault detection time T_{det}, communication time T_{com}, device turn-off time T_{off}, and energy dissipation time T_{dis} which is expressed as below:

$$T_{res} = T_{det} + T_{off} + T_{com} + T_{dis} \quad (2.1)$$

For a mechanical circuit breaker, T_{res} is mainly determined by T_{off} in the range of several tens of milliseconds. In contrast, for a solid-state circuit breaker, T_{res} largely depends on the fault detection time and the energy dissipation time T_{dis} since a power semiconductor device can turn off in microseconds or even less, negligible compared to the detection time and energy dissipation time.

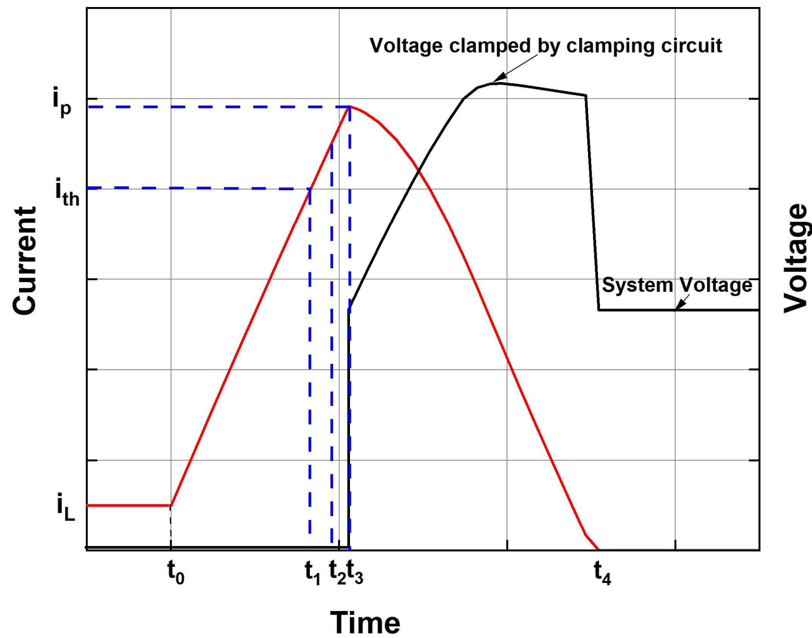


Figure 2.1 Typical overcurrent protection process of a circuit breaker

Table 2.1 Key time periods during the overcurrent protection process of a circuit breaker

Time period	**Definition**	**Value**
Detection time T_{det}	the time to detect a fault.	t_1- t_0
Communication time T_{com}	the time to communicate and transmit trip command to the breaker	t_2- t_1
Turn-off time T_{off}	Device turn-off time	t_3- t_2
Energy dissipation time T_{dis}	the time from the device turn-off until fault clearance	t_4- t_3
Response time T_{res}	the time from fault occurrence until fault clearance	t_4- t_0

2.3 DC Circuit Breaker Technologies

In the previous chapter (chapter 1), the three types of DC circuit breaker including EMCBs, SSCBs and HCBs have been presented. The following section will describe them further in detail.

2.3.1 Electro-Mechanical Circuit Breakers (EMCBs)

Traditional electro-mechanical breakers have been well developed and widely implemented for AC systems. However, due to the absence of zero crossings in DC currents, EMCBs must be retrofitted to be able to extinguish arc by either arc-manipulating technology or artificially creating zero-crossing points.

Structure of a typical EMCB

Figure 2.2 shows a typical EMCB where the main metal contacts carry the load current during normal operation while the arcing contacts break the fault current during fault interruption. Its main parts and corresponding functions are listed in Table 2.2[5].

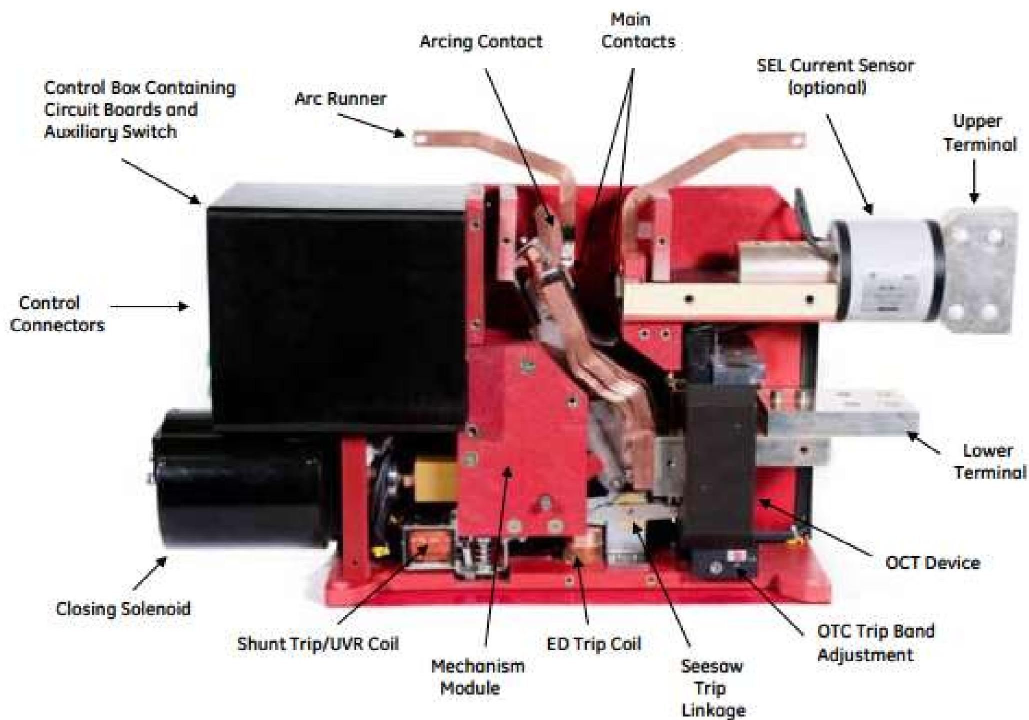


Figure 2.2 DC circuit breaker anatomy [5]

Table 2.2 Parts and functions of the EMCB

Part	Function
Main Contacts	Carry current under normal operation conditions
Arcing Contacts	Break arcing current under fault conditions
Current Sensor	Sense fault current
Mechanism	Drive the main contacts to open and close
Trip System	Initiate the opening operation of the circuit breaker
Auxiliary Switch	Physically linked to the main contacts and indicate the position of the circuit breaker for remote status and trip indication

Arc-manipulating technology

Most EMCBs have two tripping mechanisms. One mechanism for short-circuit interruption is based on electro-magnetic action driven by a solenoid and another one is for overload protection based on bimetallic action involved in two different metals with different thermal expansion [6]. The interruption system of a DC EMCB is most distinct from a AC EMCB because special technique is required to quench the no zero-point crossing DC current[7]. When a fault occurs, the current sensor detects the fault current, and the trip system sends the trip signal to the mechanism. Driven by the mechanism, the main contacts are separated, and then arc is produced. Guided by the arc runner, the arc is directed to the arcing contacts. With the aid of external force such as permanent magnets or electromagnetic coils, the arc is stretched, cooled, and finally extinguished. In practice, dielectric medium such as oil, Sulphur hexafluoride (SF6) gas and vacuum is used to surround the arcing contacts to help extinguish arc.

Artificial zero-crossings technology

Two circuits are commonly used to assist EMCBs to create artificial zero-crossings. They are called passive resonance circuits and active current injection circuits respectively[8]. For this reason, DC EMCBs can be further sub-categorized into passive DC EMCBs and active DC EMCBs.

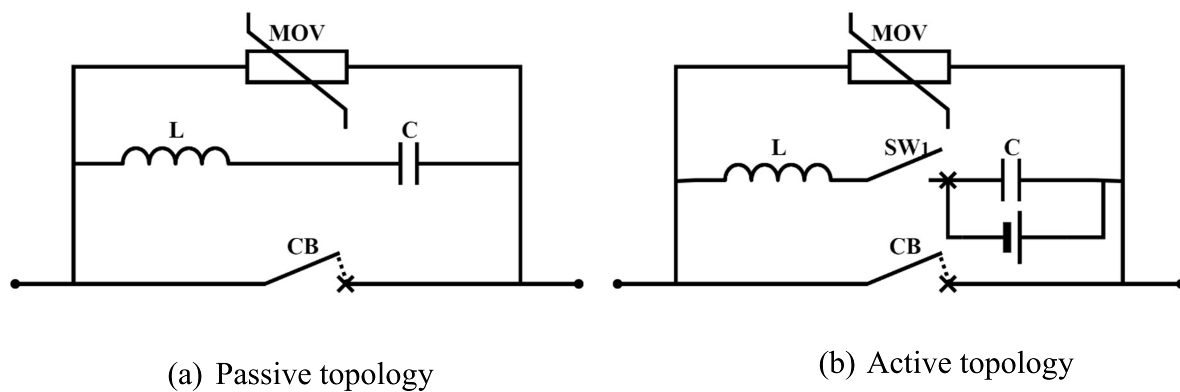
1) Passive DC EMCBs

Passive EMCBs have been widely used in HVDC transmission systems (above 100kV). Figure 2.3 (a)shows a schematic diagram of a passive DC EMCB where a LC resonant circuit is added in parallel with the mechanical circuit breaker and a MOV is used for clamping overvoltage and energy dissipation. Its operation principle exploits negative derivative dV/dI characteristic of the

arc. Once the fault occurs, the mechanical circuit breaker is open, generating the arc. The fault current is routed from the mechanical circuit breaker to the LC branch where oscillation is produced to create current zeros. When the arc is extinguished, the capacitor continues to be charged until the MOV is activated to limit the overvoltage. The main drawback of this topology is its instability under a certain condition, which would lead to the failure of fault interruption[8].

2) Active DC EMCBs

To address the instability issue, a pre-charged capacitor bank and a triggering switch is added as shown in Figure 2.3(b). Once the mechanical circuit breaker starts opening, the triggering switch is closed, and the pre-charged capacitor discharges its current into the mechanical circuit breaker. Due to the high frequency and high magnitude of the discharge current, current zeros can be instantly created.



(a) Passive topology

(b) Active topology

Figure 2.3 Two topologies of DC EMCBs

Advantages and Limitations

Thanks to the mature technology of AC EMCBs, conventional EMCBs could be used for DC systems by adding auxiliary circuits to create zero crossings. In addition, the on-resistance of EMCBs determined by the metal contacts is as low as several tens of micro-ohms. Therefore, during normal operation, EMCBs introduce minimal conduction power losses. However, due to inherent mechanical nature, EMCBs have relatively long switching time ranging from several milliseconds to hundreds of milliseconds. This response time is too long for most semiconductor devices in the converter-based DC power systems to survive[9]. In addition, EMCBs suffer short life spans because of degradation due to arching between the contacts. Last but not the least, EMCBs produce a high level of acoustic noise and Electro-Magnetic Interference (EMI) during the switching operations.

2.3.2 Solid-State Circuit Breakers (SSCBs)

Although conventional EMCBs have proved to be reliable protection devices for AC system, its slow operation speed restricts its use in DC microgrids. With the development of advanced power semiconductor technologies, solid-state circuit breakers have been frequently reported in the literature.

Typical configuration

A block diagram of SSCBs with power semiconductor devices as the main switching mechanism is shown in Figure 2.4. In practice, a cooling method is in place to prevent thermal runaway of semiconductor devices. A MOV or a snubber circuit in parallel with the main switch is used to dissipate the stored energy in the system inductance. The protection and control unit detects the fault via sensor and generate a signal to open or close the main switch. If required, it can communicate with upstream/downstream control equipment to achieve the whole system protection coordination. Due to the safety concerns, a mechanical disconnector in series with the semiconductor switch is mandatory in industries to have galvanic isolation when SSCBs are in off-state. Furthermore, multiples semiconductor devices could be connected in series or in parallel to scale up the level of power rating.

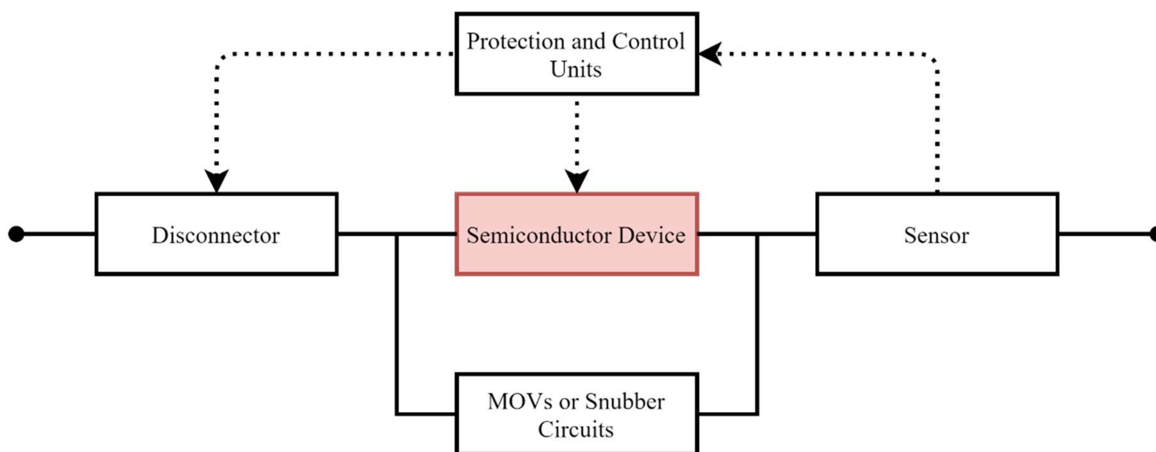


Figure 2.4 Typical configuration of SSCBs

Advantages and Limitations

SSCBs have demonstrates significant advantages over EMCBs including but not limited to:

1) Ultrafast operation speed: three orders faster than EMCBs

2) Arc-free operation minimising the concerns of fire hazards

3) Virtually infinite number of switching operations

4) No acoustic noise during the switching operations

However, there are some limitations described as follow:

1) Relatively high conduction losses

2) Limited short-circuit capability of semiconductor devices

3) Additional mechanical switch is required, leading to more complexity

2.3.3 Hybrid Circuit Breakers (HCBs)

As stated, EMCBs and SSCBs have their pros and cons. Hybrid Circuit Breakers have been proposed in the attempt to combine low on-resistance mechanical switches with fast-switching semiconductor devices.

Typical configuration

As shown in Figure 2.5, the conventional configuration of an HCB includes three paralleling branches: a mechanical switch, a semiconductor switch and a snubber or a MOV. During normal operation conditions, the mechanical switch carries load current. Once a fault is detected, the mechanical switch starts opening its contacts and simultaneously sends signal to turn on the semiconductor switch. When the voltage between the arcing contacts of mechanical switch exceeds the voltage drop of the semiconductor switch, the fault current is transferred from the mechanical branch to the semiconductor branch. In the following, the semiconductor switch turns off and then the fault current is commutated to the snubber where the energy is dissipated. In the end, the fault current is cut off.

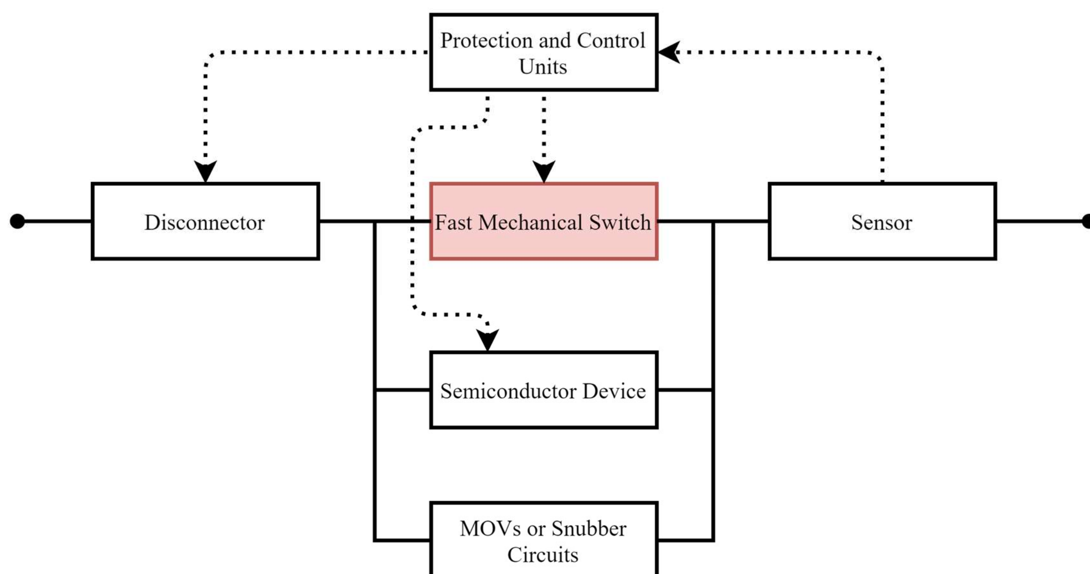


Figure 2.5 Typical configuration of HCBs

Figure 2.6 illustrates another configuration of an HCB proposed by ABB in 2011[10]. Compared with the conventional topology, a low voltage commutation switch is introduced in the branch of the mechanical switch. During the normal operation, the load current flows through both the mechanical switch and commutation switch. When a fault occurs, the commutation switch initially turns off and simultaneously the semiconductor switch turns on. As a result, the fault current is diverted to the semiconductor switch. Subsequently, the mechanical switch starts opening without arcing. In the end, the semiconductor switch turns off and the fault current fades away in the MOV branch.

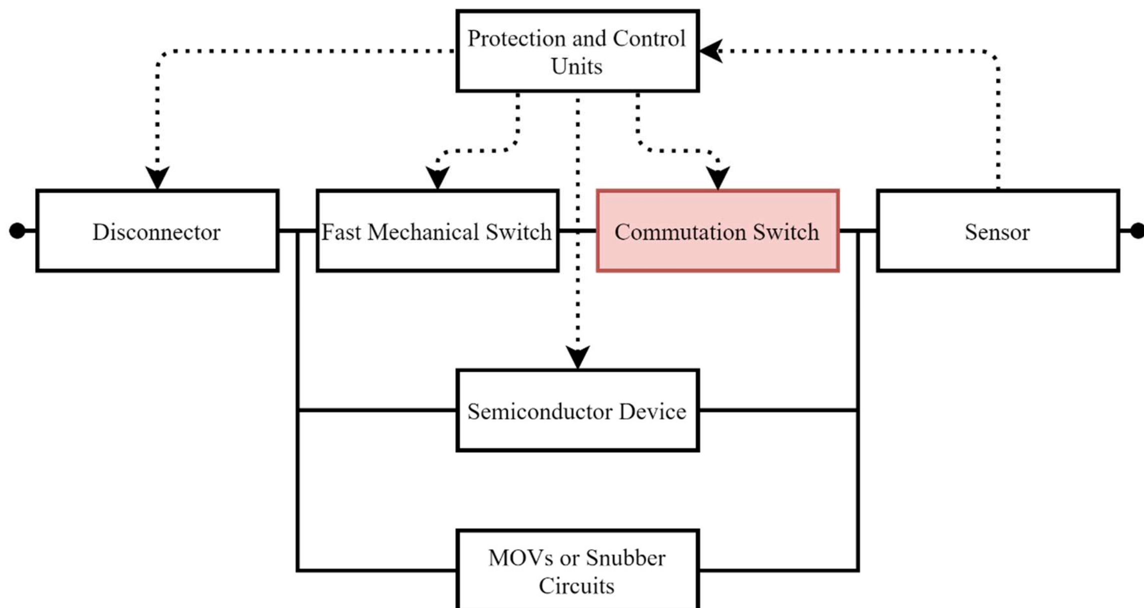


Figure 2.6 ABB Hybrid Circuit breaker (adapted from [10])

Advantages and Limitations

Compared with SSCBs, conduction losses of HCBs have been significantly reduced. However, its switching speed is still restrained by its mechanical parts. As far as it is concerned, the fastest mechanical switch reported in the literature is close to 1ms [11], which is still relatively slow for DC protection applications. In addition, the hybrid solution adds the complexity to the whole design.

To sum up, Table 2.3 compares the advantages and disadvantages of the three types of DC circuit breakers. As can be seen, SSCBs stand out for its ultrafast switching speed and almost unlimited switching operation numbers but have the main drawback of high conduction losses. In contrast, EMCBs offers extremely low conduction losses but suffer slow switching speed. A

HCB is a compromise solution suitable for those applications requiring low power losses but tolerating slow switching speed.

Table 2.3 Comparison of EMCBs, SSCBs and HCBs

Type	Advantages	Disadvantages
EMCBs	• Mature technology • Extremely low conduction losses	• Long response time (10-100ms) • Limited life span due to arc
SSCBs	• Ultrafast response time (hundreds of microseconds) • Arc-free • Almost unlimited number of switching operation	• Relatively high conduction losses • Needs additional mechanical switch for physical isolation
HCBs	• Low conduction loss • Fast response time (a few milliseconds) • Minimal arc	• Complex structure • Switching speed is limited by the mechanical parts

2.4 Review of SSCBs/HCBs Based on Various Semiconductor Devices

In the literature, various semiconductor devices have been proposed for SSCB applications. This review starts with Silicon-based semiconductor devices including Gate Turn-off Thyristor (GTO), Integrated Gate-Commutated Thyristor (IGCT), Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) and Silicon Insulated-Gate Bipolar Transistor (IGBT), followed by wide bandgap semiconductors devices such as Silicon Carbide Junction Field Effect Transistors (SiC-JFETs), SiC MOSFET and Gallium Nitrite High-Electron-Mobility Transistors (GaN-HEMTs).

2.4.1 SSCBs/HCBs based on Silicon power semiconductor devices

Silicon semiconductor devices have developed towards a very high maturity level and provide a wide range of commercial choices with different levels of voltage and current ratings.

- **Thyristors and thyristor-based devices**

Thyristor family including Silicon-Controlled Rectifiers (SCRs), Gate Turn-Off thyristors (GTOs), Emitter Turn-Off thyristors (ETOs) and Integrated Gate Commutated Thyristors (IGCTs), are the most powerful semiconductor devices since one single device can block voltage up to 12kV and conduct current up to 8kA. Additionally, they have demonstrated very low conduction losses. Therefore, they have been widely used for high power applications such as HVDC. However, thyristors cannot be switched off unless their currents fall below a certain level.

To do so, an additional resonance circuit is required to reduce the current for turn off. To address this issue, fully controlled thyristor-based switches have been developed such as GTOs, ETOs and IGCTs.

In 1976, the first thyristor-based DC SSCB was designed with 600V rated voltage and 800A rated current.[12]. As shown in Figure 2.7, the circuit topology consists of three branches in parallel: the main power thyristor T_1, the resonance circuit branch including an inductor, an auxiliary thyristor T_2 and the capacitor C_K which is pre-charged from an auxiliary rectifier composed of a transformer T_L, diode D_L and current-limiting resistor R_L, and a snubber branch formed of a resistor, a capacitor, and a diode. The experimental results show the SSCB is capable to interrupt current up to 1850A with the response time 1020μs.

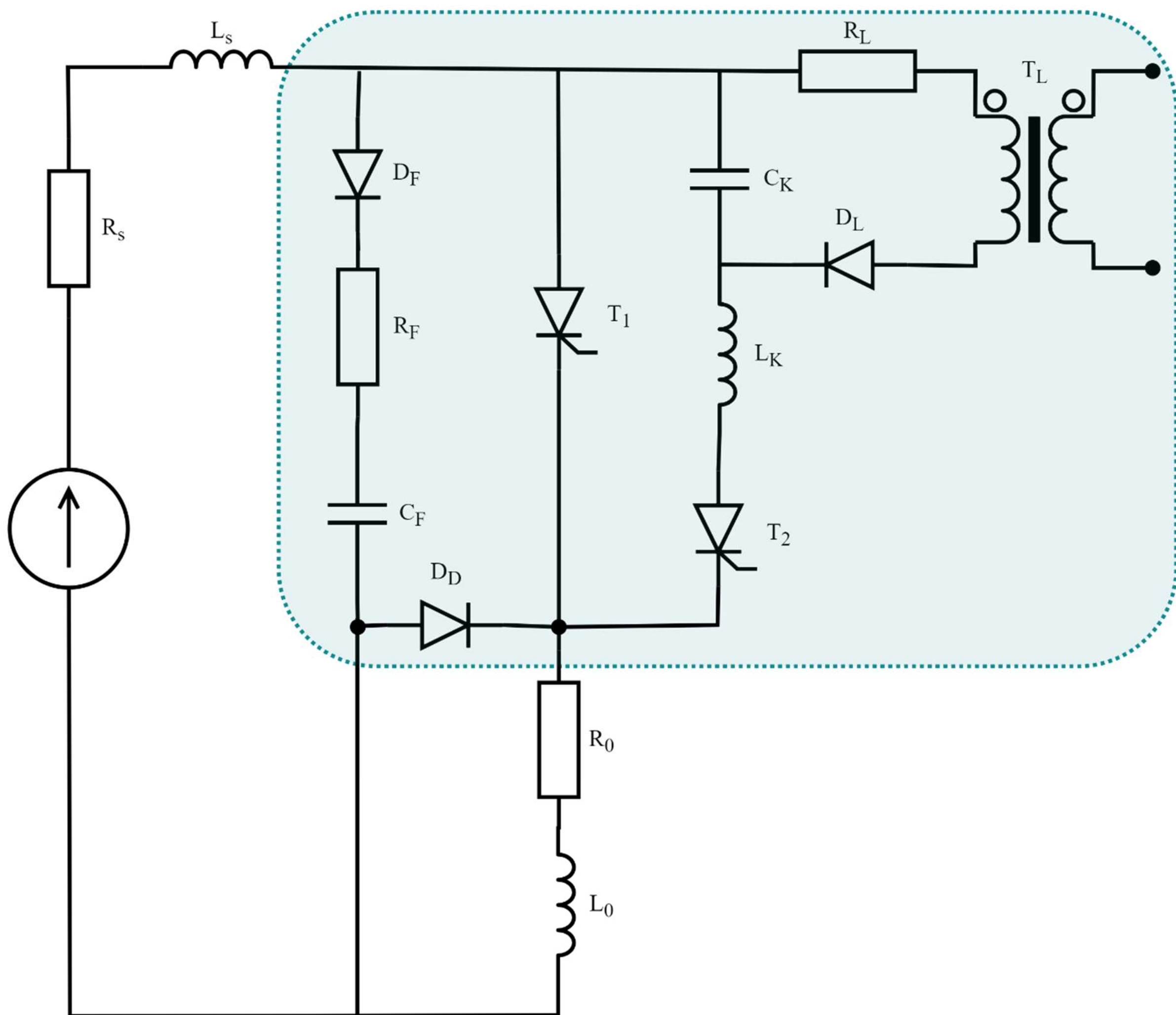


Figure 2.7 Thyristor based SSCB (adapted from [12])

In 2012, a circuit topology called Z-source was proposed for 6kV DC system[13] .As shown in Figure 2.8, this topology exploits the high transient fault current causing the resonance

of Z-source LC network and thereby generating zero-crossing current. After the SCR turns off, the energy is exhausted in the LCR resonance circuit and the current eventually fades away. Although the Z-source SSCBs have the advantages of a simple control and an isolation from the fault to the source, it only works under the high dynamic fault currents to activate the Z-source network.

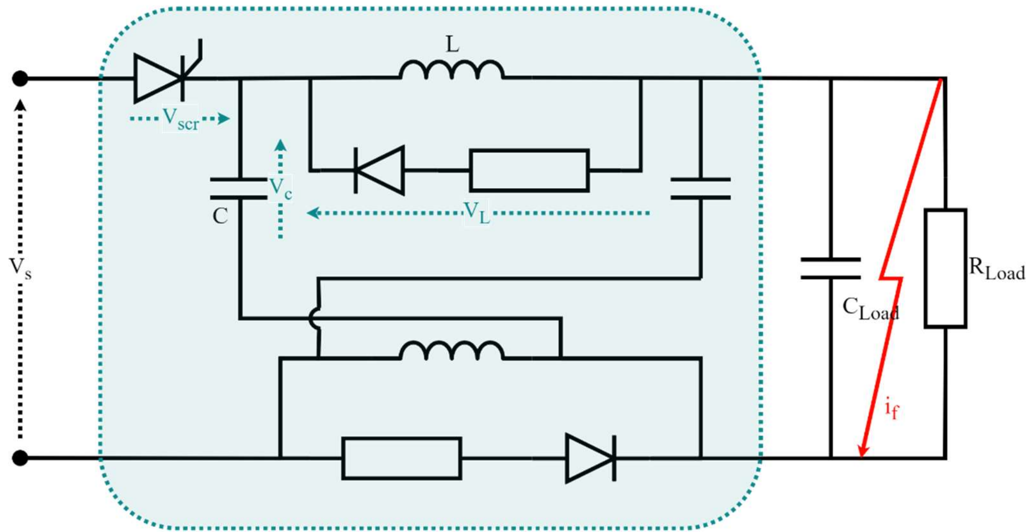


Figure 2.8 Z-source circuit breaker [11]

Since **GTOs** were reported in 1962, many SSCBs or HCBs using GTOs have been proposed in the literature. In 1994, a Japanese team built a HCB by combining GTOs with a high-speed vacuum switch for 400V AC power distribution system[14]. It demonstrates that it is capable of interrupting fault current of up to 10kA within 1ms. In the same year, Westinghouse Electric Corporation proposed a SSCB using six GTOs in series for 13.8kV AC MV systems [15]. Almost a decade later, in 2003, a current-limiting HCB (12kV/20kA AC) combining GTOs with Positive Temperature Coefficient (PTC) thermistors was proposed in [16]. In 2016, a SSCB configured by a hybrid of a GTO with an IGBT, was presented in [17], achieving both low conduction losses and high switching speed. The experimental results show it can interrupt 388A peak current at 2.1kV voltage. However, the main disadvantage of GTOs is its poor dynamic avalanche capability (dv/dt and di/dt) leading to the failure especially during inductive turn-off [16].

IGCTs were introduced by ABB in 1997, which is an improved GTO integrated with a gate-drive circuit[17]. They are further classified into three types: reverse-conducting, reverse-blocking and asymmetric. Among the three of them, the asymmetric IGCT has the lowest conduction losses[3]. In 2006, ABB designed a 1.5kV/4kA HCB using IGCTs[18]. The

prototype demonstrates the opening time less than 300μs is achievable. Using the same topology, a 1kV/10kA HCB based on IGCTs was developed by an Italian group in 2011[19]. A few years later, ABB developed a bidirectional SSCB based on two anti-parallel 2.5kV reverse-blocking IGCTs. It demonstrates it can interrupt the current up to 7 kA at 1kV [20]. Although showing great power capability, both GTOs and IGCTs need a complicated current controlled gate driver which are bulky and power consuming.

An **ETO** was first reported in 1998[21], which is the cascode of a GTO with a power MOSFET switch. Due to the MOS type voltage-controlled gate driving, the requirement on gate driving circuitry is greatly reduced. In 2002, an ETO-based SSCB was proposed for a MV DC system [22]. The experiment demonstrates that the prototype (1.5kA/2.5kV) can achieve a very fast switching speed (within 5μs).

- **Metal-oxide semiconductor field-effect transistors (MOSFETs)**

Over the past five decades, Silicon MOSFETs have been well-developed and become the most mature semiconductor devices in the industry. The MOSFET offers a voltage-controlled gate and easy paralleling. However, for the medium voltage (>1kV), a single silicon MOSFETs with a normal structure has a relatively high on-resistance (more than 200 mΩ-cm^2 at the voltage rating of 1200V), and therefore not suitable for MV SSCBs application. In contrast, Superjunction or CoolMOS MOSFETs demonstrate a low specific on-resistance in a range of 10-20 mΩ/cm^2 under 600 V rated voltage[9]. As shown in Figure 2.9, a 380V/45A bidirectional SSCB consisting of 20 units of 600V CoolMOS was proposed in [23]. The experimental results show it can interrupt the current up to 1240A. [24] reported a 270V/200A SSCB using 22 units of 650V MOSFETs, which demonstrates a 300A interruption current with switching time of 4μs.

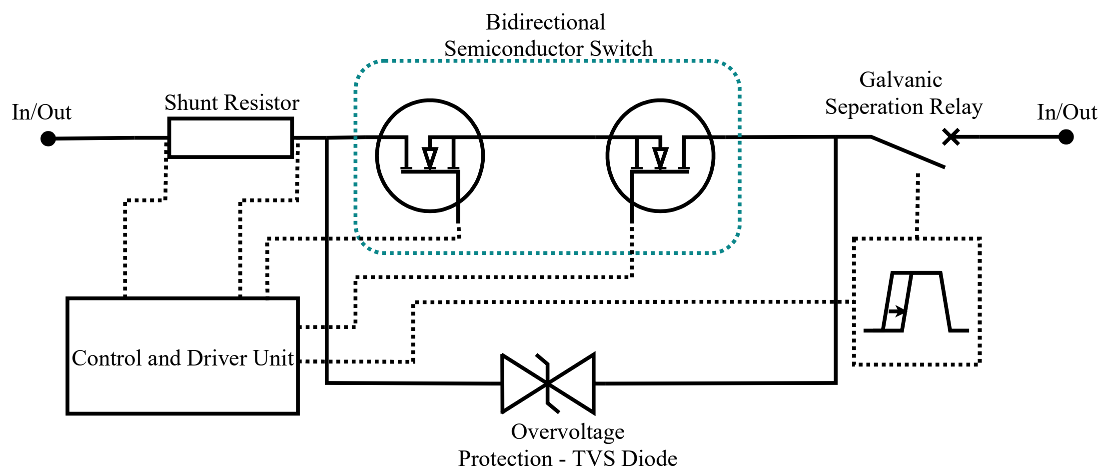


Figure 2.9 MOSFET-based SSCB schematic circuit (adapted from [23])

- **Insulated gate bipolar transistors (IGBTs)**

Since the invention in the late 1970s[25], IGBTs have been the most adopted semiconductor devices for SSCBs applications owing to its wide range of commercial availability (voltage ranging from 300V to 6500V and currents up to 3600A), MOS-type simple voltage controlled gate, and high power capability.

In 2006, [26] proposed a 400V/120A bidirectional SSCB based on back to back IGBTs as shown in Figure 2.10. The experimental results show that the prototype is capable of interrupting current 120 A for 0.8 s. In 2011, ABB developed a 320kV/2kA hybrid circuit breaker using IGBTs and fast mechanical switches, which demonstrates 9kA breaking current capability. A couple years later, in [27], a SSCB using a pair of IGBTs in parallel demonstrated 10kA breaking current capability at 1kV system voltage. In 2015, [28] presented a current limiting HVDC hybrid breaker (250kV/ 2kA) by adding a superconductor to the traditional HCB. In the following year, Siemens developed an IGBT-based SSCB for bus protection, showing the ability of breaking 2kA current at 1kV DC [27]. In the same year, a Chinese team reported a 10kV SSCB based on press-pack IGBTs with interrupting current up to 7.4kA [29].

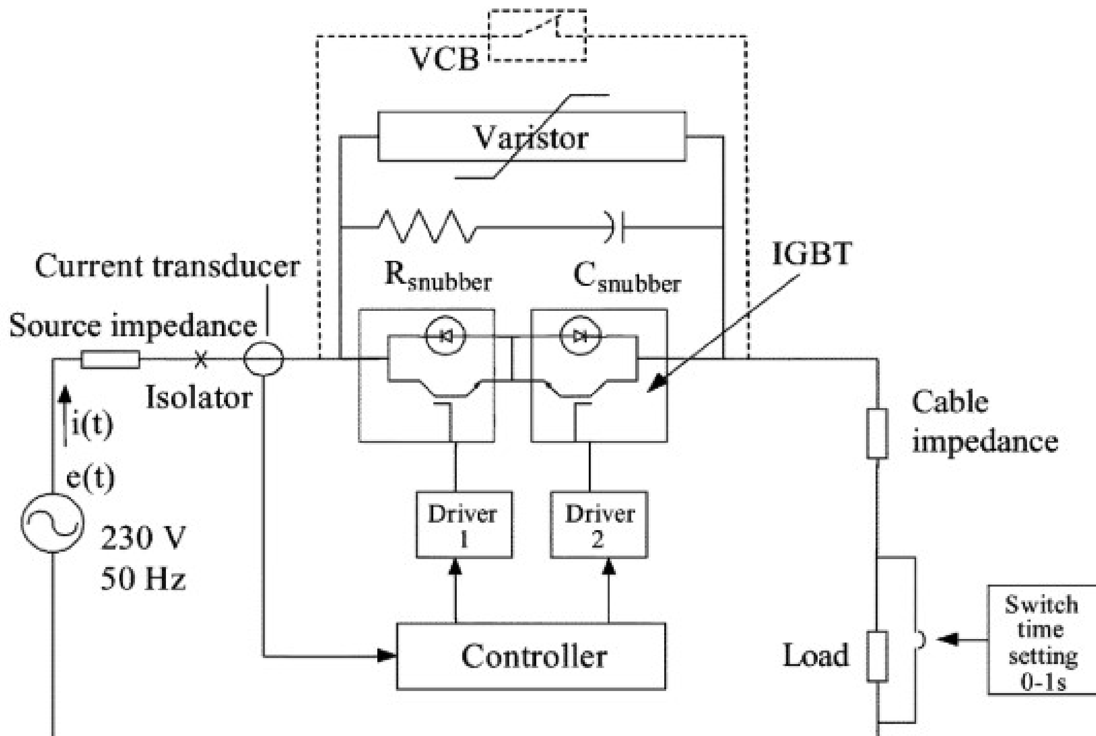


Figure 2.10 IGBT based SSCB configuration [26]

2.4.2 SSCBs/HCBs Based on Wide bandgap semiconductor devices

The main limitations of SSCBs using silicon power semiconductor devices are relatively high conduction losses and low maximum junction temperature. WBG devices could mitigate these limitations by offering superior material properties such as low conduction losses, high junction temperature and high voltage capability. Considering the theoretical performance and availability of material, up to now, Silicon Carbide (SiC) and Gallium-Nitride (GaN) are two most promising materials.

Figure 2.11 graphically compares the main properties of Si, SiC, and GaN materials [30]. As it can be seen, compared to Si, SiC and GaN materials can operate at much higher temperature, making them perfect for SSCB applications where the sudden energy-burst during short-circuit condition would drive the junction temperature beyond the device limit. Furthermore, SiC and GaN have twice or triple value of critical breakdown field (Ec) of Silicon respectively. That means for a vertical structure, with the same drift width and doping concentration, SiC and GaN devices have higher voltage blocking capability. In other words, provided the same blocking voltage, SiC and GaN device could have thinner drift region and higher doping concentration, translating to lower on-resistance. For example, given 1000V blocking voltage, the specific resistance of Si, SiC, and GaN unipolar vertical devices are theoretically estimated as 200, 0.6, and 0.1 mΩ-cm^2 respectively[31]. Although vertical unipolar GaN power semiconductor devices have the lowest theoretical on-state specific resistance, they are not available in the market and only lateral GaN HEMTs with high on-resistance are commercially available.

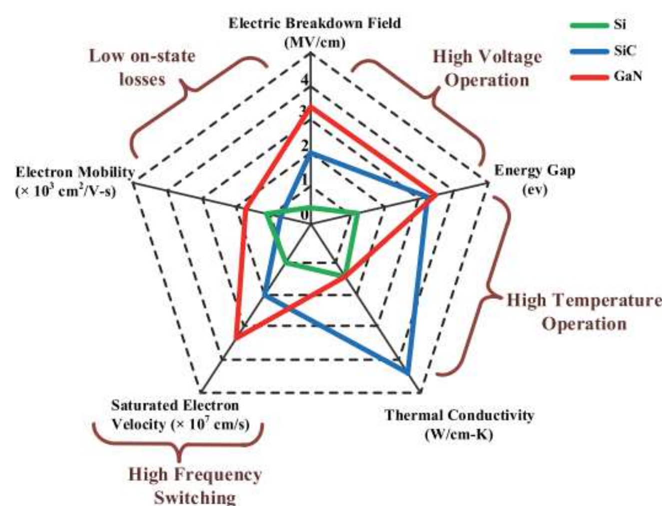


Figure 2.11 Comparison of Si, SiC, and GaN material properties [30]

Due to the significant benefits offered by SiC materials, SiC JFET devices have been rigorously researched for SSCBs applications. In 2008, Siemens proposed a low voltage SSCB using a 1.2kV SiC JFETs cascode with a low voltage MOSFET[32]. In 2011, the work in [33] reported a bidirectional SSCB based on 1.2kV SiC JFET with the capability of switching off 60A at 600V. In 2015, a SSCB using a 1.2k V vertical-channel implanted-gate SiC JFETs was proposed. It has demonstrated the excellent ruggedness of SiC JFET devices passing over 2.4 million pulsed hard switching test [34].In the same year, a self-powered ultrafast SSCB using 1.2kV normally-on SiC JFETs was reported in [35][36].

Figure 2.12 illustrates the concept of self-powered SSCBs topology. It uses a normally-on SiC JFET as the main switch and a DC/DC flyback converter as a protection driver for detecting fault and then driving the SiC JFET off. During the normal operating conditions, the load current flows through the SiC JFET and the protection driver is in stand-by mode since the on-state voltage of the SiC JFET is too small to activate the protection driver. Once a short-circuit fault occurs, the surging fault current will push up the drain voltage of SiC JFET and therefore activating the protection driver to produce negative biased gate voltage to turn off the SiC JFET. During the interruption process, the protection driver draws power from the voltage drops of the SiC JFET. Hence, this topology does not require an external power supply. The experimental results demonstrate it can interrupt current of up to 150A at 400V DC. Although this topology is simple and self-powered, some limitations should be considered for practical application. Firstly, the SSCB cannot be manually switched off due to lack of power supply, which is essential for the routine maintenance of a circuit breaker. Secondly, this topology is only suitable for high fault current protection since it requires the current high enough to enable the protection driver. Last but not the least, the SSCB is subject to false triggering caused by inrush currents at the initial connection of loads such as the start-up of motors.

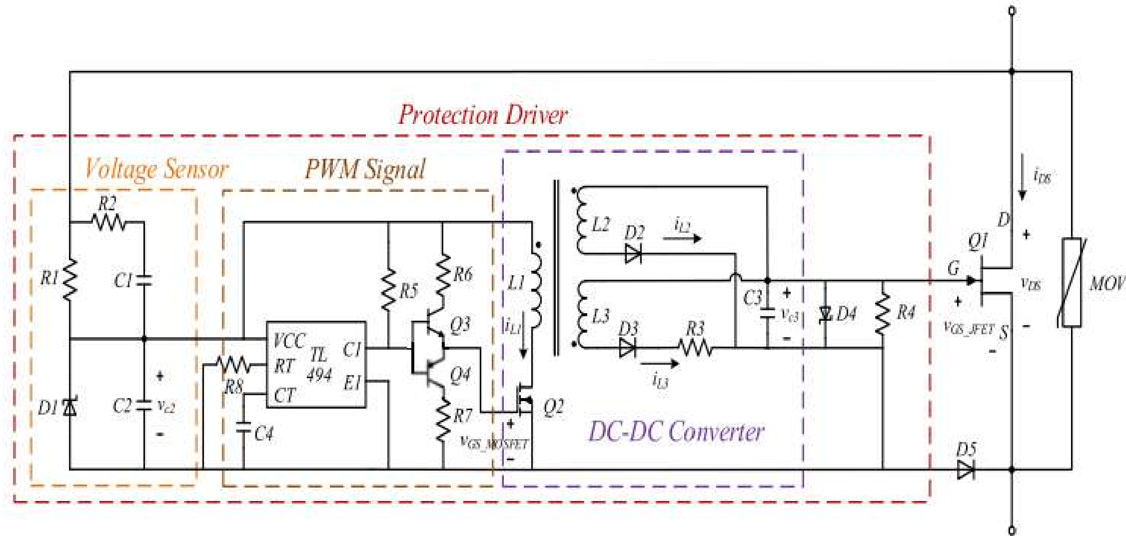


Figure 2.12 schematic circuit of self-powered SSCB topology ([36])

In 2016, the paper in [37] applied the self-powered topology to a 650V GaN HEMT device, achieving a bidirectional SSCB as shown in Figure 2.13. The experiment on the prototype shows the capability of interrupting current up to 45A at a DC bus voltage of 300V.

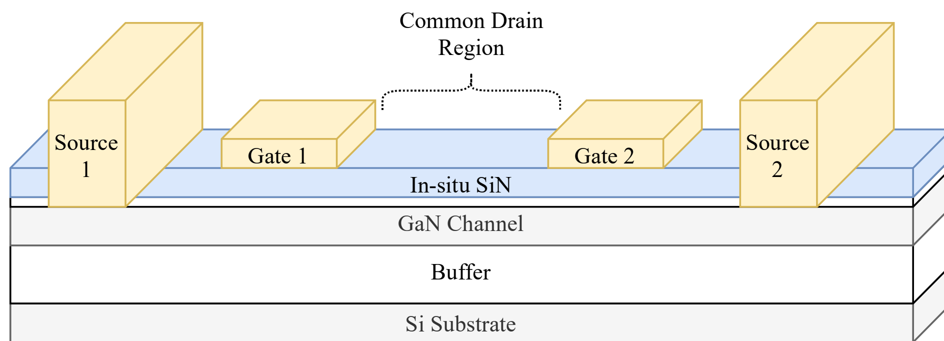


Figure 2.13 cross-section of monolithic dual-gate bidirectional GaN switch (adapted from [37])

Due to the increasing commercial availability from several semiconductor manufacturers, SiC MOSFETs have been frequently reported for SSCBs applications. For example, a SiC MOSFET-based 850V, 100A SSCB was proposed in 2016 [38]. In the same year, a SSCB based on 1.2kV SiC MOSFET was reported for 270V DC systems, experimentally demonstrating the capability of switching off current of 250 A within 10 µs, and 450 A within 70 µs[39]. In 2018, SiC MOSFET-based 380V/20A SSCB was proposed for data centre applications[40]. In 2020,

as shown in Figure 2.14, a 4kV/100A SSCB was configured with a five-layers structure and each layer was mounted with ten 1.2kV/115A SiC MOSFETs in parallel. This design achieves the efficiency as high as 99.97% [41].

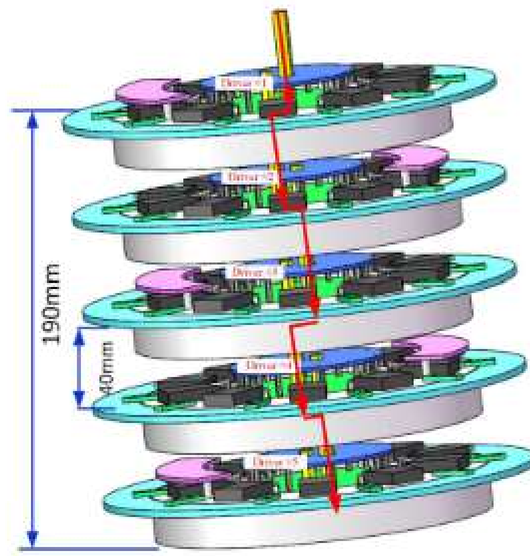


Figure 2.14 a SSCB based on SiC MOSFETs [41]

To summarize, in the literature, SSCBs/HCBs has been proposed with a wide range of voltage from a few hundred volts to hundreds of kV and current from tens of amps up to a few kA. Table 2.4 consolidates most DC SSCBs/HCBs arranged by the device type. As it can be seen, SSCBs/HCBs based on thyristor family and IGBTs are mainly used for high voltage and high current applications such as MVDC or HVDC due to their high-power ratings. For applications with low operating voltage, the use of WBG based SSCBs are the most popular choice. This is down to the excellent performance and the availability in the market for this voltage range.

Table 2.4 Summary of SSCBs/HCBs in the literature

Group	Topology	Devices	Bus voltage	Block Voltage	Rated current	Interrupting current	Response time*	Proposed Year
Thyristors based	SSCB	SCR [12]	600VDC		800A	1.8kA	1020μ	1976
	SSCB	ETO [22]	2.5kV	4.5kV	1.5kA	4kA	5μs	2002
	HCB	IGCT/FS [18]	1.5kV DC		4kA	-	1.3ms	2006(ABB)
	HCB	IGCT/FS [19]	1kV DC	6.5kV	3.8kA	10kA	350ms	2011
	SSCB	SCR/LC [13]	6kV DC		1kA	-	113μs	2012
	SSCB	IGCT [22]	1kV DC	2.5kV	1kA	6.8kA	10μs	2015(ABB)
	SSCB	GTO/IGBT [17]	2.1kV DC		200A	388A	10μs	2016
MOSFETs based	SSCB	CoolMOS [23]	380V	600V	45A	1240A	10μs	2019
	SSCB	MOSFET [24]	270	650V	200A	300A	4μs	2014
IGBTs based	HCB	IGBT/FS [10]	320kV DC		2.6kA	9kA	2ms	2011(ABB)
	SSCB	IGBT [27]	1kV DC		1.8kA	10kA	160μs	2013
	HCB	IGBT/FS/SC [28]	250kV DC		2kA	10kA	0.1s	2015
	SSCB	IGBT [29]	1kV DC		1kA	2kA	20μs	2016(Siemens)
	SSCB	IGBT [30]	10kV DC		3kA	5.1KA	-	2016
WBG based	SSCB	SiC JFET [33]	600V DC	1200V	60A		10μs	2011
	SSCB	SiC JFET [35]	400V DC	1200V	38A	180A	1μs	2015
	SSCB	GaN HEMT [37]	300V DC	650V	10A	40A	1μs	2016
	SSCB	SiC MOSFET [38]	850V DC	1200V	100A	234A	100μs	2016
	SSCB	SiC MOSFET [39]	270V DC	1200V	350A	450A	70 μs	2016
	SSCB	SiC MOSFET [40]	380V DC	1200V	20A			2018
	SSCB	SiC MOSFET [41]	4kV	12kV	100A			2020

*The response time presented highly depend on the inductance of the test setup which in most cases it is not given. In addition, the response time in most cases does not include the energy dissipation time by the MOV or the snubber circuit.

Based on the data in Table 2.4, a rough comparison between SSCBs and HCBs is made in Table 2.5.

Table 2.5 Comparison of SSCBs and HCBs

Parameter	**SSCBs**			**HCBs**	
	Thyristor	**IGBTs**	**WBG**	**Thyristor**	**IGBTs**
Turn-off time	≤1020 μs	≤160μs	≤100μs	≥1ms	≥1ms
Rated voltage	0.6-6kV	10kV	<1kV	1-12kV	<320kV
Interrupting current	0.2-1.5kA	<5kA	<250A	10-20kA	<10kA
Power losses	0.14%-0.3%	<1%	<1%	<0.001%	<0.001%
Comment	• Switching speed of SSCBs is much faster than HCBs. • HCBs show much lower conduction losses than SSCBs. • The current handling capabilities of WBG devices are relatively low.				

2.5 Review of Fault Sensing Technique

As mentioned in Section 2.1, the main function of a circuit breaker is to interrupt fault current during overcurrent event. The fault current is usually sensed by current sensors. The requirements on DC fault current sensors are fast response, low losses, and easy integration with control circuitry, which is not a trivial task. This section will review methods of current sensing in the literature.

Generally, four types of sensing techniques are reported for SSCB applications in the literature.

Shunt resistor Sensing [42][43]

A shunt resistor is introduced into the current path and the voltage drop across the resistor is measured, which is proportional to the current according to the Ohm's law. This method is simple, low cost and has good accuracy but inevitably introduces additional conduction loss and does not provide electrical isolation between the main power and protection circuit.

Hall effect sensing [44][45]

The Hall-effect is used for current measurement. When a current (I) flows through a thin layer of conductive material which is simultaneously penetrated by a magnetic flux density (B), a voltage across the material (V) is generated and determined by,

$$V = \frac{I.B}{n.q.d} \tag{2.2}$$

where q is the charge of the carrier, n is the carrier density and d is thickness of the sheet. Given the parameters B, n, q and d, the current can be obtained by measuring the voltage. This method provides electrical isolation between power circuits and protection circuits. However, it requires degaussing process if an overcurrent incident occurs. Moreover, it can cause measurement error by thermal drift.

On-state voltage sensing [46] [47]

During on-state of a semiconductor device, the on-state voltage drop across the power device is approximately proportional to the current flowing through the device in the linear region. The main advantage of this method is no requiring extra sensing element and therefore has fast response speed. However, it has poor accuracy and does not provide electrical isolation.

Giant Magneto Resistance (GMR) sensing [48]

Since the electrical resistance of some special material changes with the applied magnetic field induced by the current, the current can be derived by measuring the change of the resistance. As reported in [49], the current flow in the U-turn of a PCB trace, generating a magnetic field. A circuit bridge constructed by four GMR sensor elements is tuned so that the voltage across the bridge is proportional to the current. This method offers excellent accuracy, fast response speed and low power losses. However, it is susceptible to external magnetic fields and has limited bandwidth.

2.6 Conclusions

DC circuit breakers are broadly categorized into three types: EMCBs, SSCBs and HCBs. Due to the absence of natural zero-crossings in DC currents, conventional AC EMCBs must be retrofitted for DC applications either by arc-manipulating technology or by resonance circuits to create zero points. Though EMCBs have extremely low conduction losses, they suffer slow switching speed due to its inherent mechanical nature. In contrast, SSCBs offer ultrafast switching speed but its relatively high conduction losses are one of the major drawbacks. The topology of HCBs is a compromised solution by integrating a fast mechanical switch with the semiconductor devices. However, its switching speed is restricted by its mechanical parts. SSCBs/HCBs based on either IGBTs, or thyristor family have been widely used for

HVDC/MVDC systems due to device high power ratings. Whereas, for low voltage DC applications, SSCBs based on WBG devices are the preferred solutions thanks to the superior properties of WBG materials: high breakdown voltage, high temperature and low specific on-resistance. In addition, the normally-on feature of either SiC JFETs or GaN HEMT are more desirable for circuit breaker applications since they do not require active biased gate voltage to maintain its on-state and have natural ability to scale up current rating by paralleling multiple devices. However, SSCBs still face significant technical challenges such as high conduction losses and limited short-circuit capability. With the increasing maturity of technology and commercial availability of WBG devices especially SiC or GaN devices, WBG-based SSCBs are predicted to be widely used in low-voltage DC microgrids. This research focuses on the development of a SSCB based on WBG devices for 400V DC microgrid applications.

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Chapter 3 Analysis of Transient Blocking Units

3.1 Introduction

The Transient Blocking Units (TBUs) were originally invented and patented by Richard Allen Harris in 1998, which are used for a current limiting protection in the applications with signal interface[1].

As shown in Figure 3.1(a), the basic TBU is constructed by one p-channel depletion mode Field Effect Transistor (FET) device in series with one n-channel depletion mode FET. Their source terminals are linked together while their gate terminals are connected to the opposite drain terminals. With this configuration, the voltage across the n-channel FET is identical to the gate voltage of p-channel FET and vice versa. Under the normal operating condition, the load current flows through the TBU. The voltage drop across the TBU is negligible due to the low on-resistance of the two FET devices. When the load is inadvertently shorted, the current surges through the TBU causing the increases of the voltages across both FETs. The rise of voltage across the n-channel FET tends to turn off the p-channel FET and vice versa. When the current reaches a certain value depending on the characteristics of the FETs, both devices start limiting the current until the current is down to zero. Figure 3.1(b) shows a typical output characteristic of the TBU. It includes three distinct regions: 1) Current rising 2) current limiting 3) current cut-off. The response time of TBUs is extremely short with typical value of around 1μs [2], which is determined by a number of factors including tripping current level, system inductance and the parasitic capacitances of both FET devices.

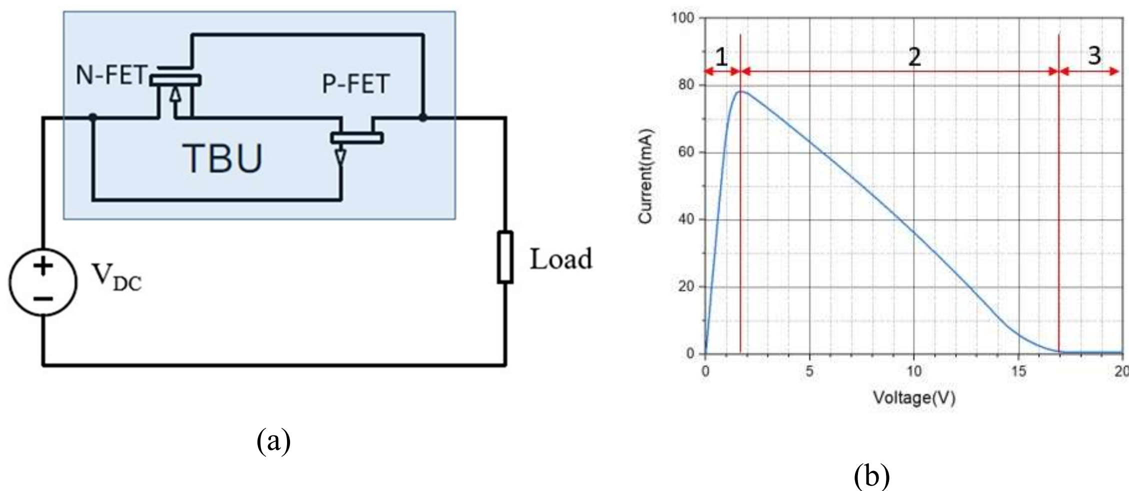


Figure 3.1(a) Basic TBU circuit (b) Typical I-V of the TBU

One of the most important features of the TBU is no requirement for costly and complex sensing circuitry, digital signal processing and data communication functions which accounts for most of response time during short-circuit fault interruption. Therefore, the TBU's switching operation is extremely fast. However, the TBUs are limited to very low tripping currents up to 1A [2]. To develop a SSCB applied for high power ratings based on the concept of the TBUs, it is essential to carry out a thorough and in-depth analysis of the TBUs.

This chapter is organized as follows: In the first instance, an analysis of the static performances of the basic TBU is presented, with the analytical expressions derived for output characteristics of the TBUs in multiple stages. Then, the analytical results are validated by simulation. Finally, the TBUs sourced from Bourns Inc are analysed and evaluated by both simulation and experiment.

3.2 Current-voltage Characteristics and Equations for FET devices

To model the behaviour of a semiconductor device in a circuit simulator, mathematical equations are required to calculate the drain current I_{DS} for a set of applied voltage, V_{DS} and V_{GS}. This set of mathematical equations is usually referred to as the device model. For the FET devices such as MOSFETs or JFETs, several models have been proposed in terms of their accuracy and complexity. They are generally categorised into three levels: Level 1, Level 2 and Level 3 models. Level 1 is the simplest model proposed by Shichman and Hodges in 1968 [3]. This model is suitable for the work requiring quick estimation rather than high accuracy. Level 2 model is a physically based model which offers higher level of accuracy than Level 1 model but add to the unnecessary complexity. Level 3 is an empirical model with less complexity than Level 2 while sacrificing accuracy. For the simplicity, Level 1 model is adopted in the following analysis, which is adequate for this work.

As shown in Figure 3.2, typical output characteristics simulated from a Level 1 n-channel MOSFET model have three distinct regions: cut-off region, linear region and saturation region. Its operating characteristics are presented below [4].

Cut-off region: When $V_{GS} \leq V_{TH}$ and $V_{DS} > 0$

$$I_{DS} = 0$$

Linear region: When $V_{GS} > V_{TH}$ and $0 < V_{DS} < V_{GS} - V_{TH}$

$$I_{DS} = \beta_M[(V_{GS} - V_{TH})V_{DS} - \frac{{V_{DS}}^2}{2}] \quad (3.1)$$

Saturation region: When $V_{GS} > V_{TH}$ and $V_{DS} \geq V_{GS} - V_{TH} \geq 0$

$$I_{DS} = \frac{\beta_M}{2}(V_{GS} - V_{TH})^2 \tag{3.2}$$

Where V_{TH} is gate threshold voltage and β_M is the gain factor defined by

$$\beta_M = \mu_0 C_{ox} \frac{W}{L_{eff}} = KP(\frac{W}{L_{eff}}) \tag{3.3}$$

Where μ_0 is channel mobility; C_{ox} is the gate oxide capacitance; W is channel width; L_{eff} is effective channel length and KP is transconductance parameter.

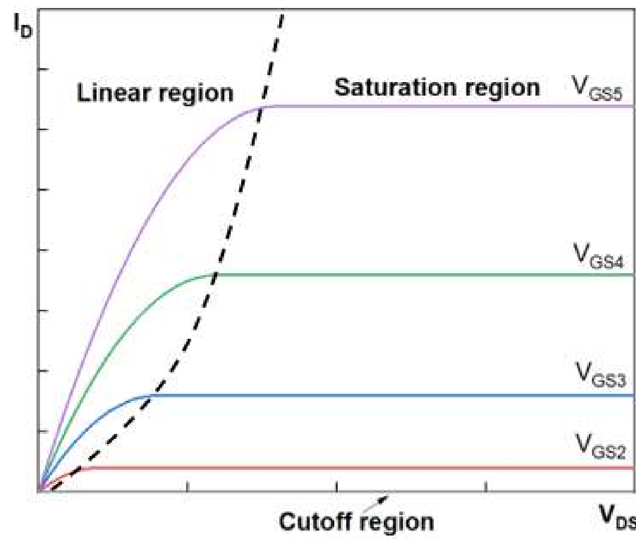


Figure 3.2 I-V characteristics of a typical MOSFET

Similarly, the output characteristics of Level 1 p-channel JFET model in three regions are:

Cut off region: When $V_{GS} \geq V_{PO}$, $V_{DS} < 0$

$$I_{DS} = 0$$

Linear region: When $V_{GS} < V_{PO}$ and $0 > V_{DS} > V_{GS} - V_{PO}$

$$I_{DS} = -\beta_J[2(V_{GS} - V_{PO})V_{DS} - {V_{DS}}^2] \tag{3.4}$$

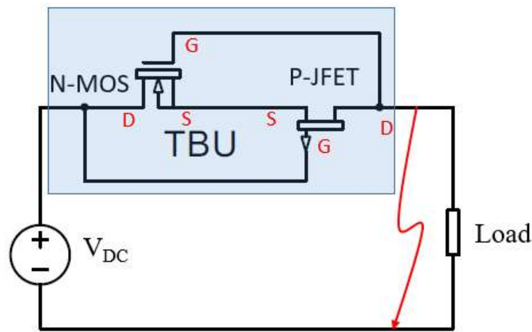
Saturation region: When $V_{GS} < V_{PO}$ and $V_{DS} \leq V_{GS} - V_{PO} \leq 0$

$$I_{DS} = -\beta_J(V_{GS} - V_{PO})^2 \tag{3.5}$$

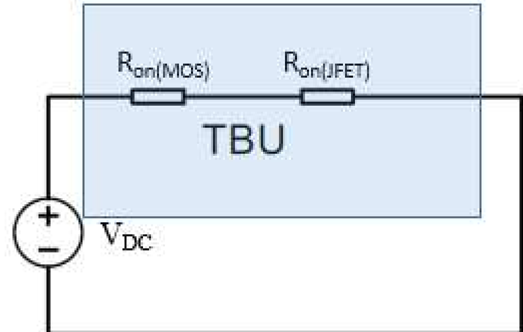
Where V_{PO} is gate pinch-off voltage and β_J is the gain factor.

It is worth noticing that the expressions of Level 1 n-channel JFET model become identical to the n-channel MOSFET model if the gain factor β_J of JFET is taken half of β_M of MOSFET.

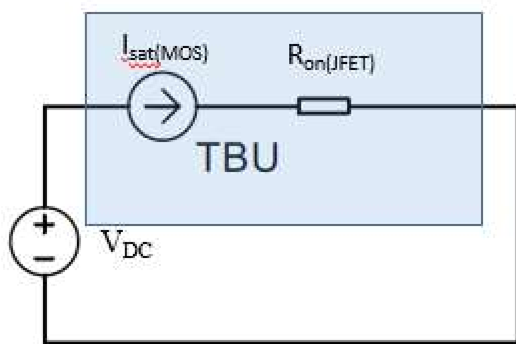
3.3 Analysis of Static Operating Principle of the Basic TBU



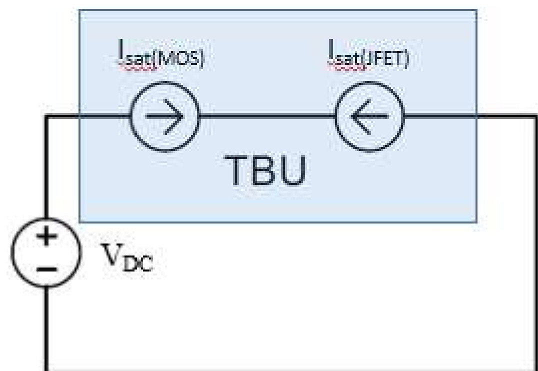
(a) TBU under a short-circuit event



(b) Equivalent circuit in Stage 1



(c) Equivalent circuit in Stage 2



(d) Equivalent circuit in Stage 3

Figure 3.3 Equivalent circuits of basic TBU in three stages

As shown in Figure 3.3(a), the basic TBU consists of a depletion mode n-channel MOSFET in series with a depletion mode p-channel JFET. When a short-circuit event occurs, the operating process of the TBU can be divided into three stages depending on the operating modes of both the MOSFET and the JFET.

Stage 1: Both n-channel MOSFET and p-channel JFET operate in the linear region.

The equivalent circuit for this stage is shown in Figure 3.3(b), where $R_{on\ (MOS)}$ and $R_{on\ (JFET)}$ are on-resistance of the MOSFET and the JFET respectively.

For the n-channel MOSFET in the linear region, the equation (3.1) is referred below:

$$I_{DS(MOS)} = \frac{\beta_M}{2}\left[2(V_{GS(MOS)} - V_{TH})V_{DS(MOS)} - V_{DS(MOS)}{}^2\right] \quad (3.6)$$

Since the voltage across the MOSFET during this stage is relatively low, a linear relationship between the current and the voltage can be assumed. Thus, Equation (3.6) can be simplified as:

$$\mathrm{I_{DS(MOS)}} = \beta_M\left[\left(\mathrm{V_{GS(MOS)}} - \mathrm{V_{TH}}\right)\mathrm{V_{DS(MOS)}}\right] \quad (3.7)$$

Similarly, for the p-channel JFET in the linear region, Equation (3.4) is referred as:

$$\mathrm{I_{DS(JFET)}} = -\beta_J\left[2\left(\mathrm{V_{GS(JFET)}} - \mathrm{V_{po}}\right)\mathrm{V_{DS(JFET)}} - \mathrm{V_{DS(JFET)}}^2\right] \quad (3.8)$$

Also, it can be simplified as by assuming linear I-V relationship and $V_{GS(JFET)} = 0$:

$$\mathrm{I_{DS(JFET)}} = 2\beta_J \mathrm{V_{po}} \mathrm{V_{DS(JFET)}} \quad (3.9)$$

Rearranged as:

$$V_{DS(JFET)} = \frac{I_{DS(JFET)}}{2\beta_J . V_{po}} \quad (3.10)$$

According to the circuit in Figure 3.3 (a), the following relationships can be found:

$$V_{GS(MOS)} = V_{DS(JFET)} \quad (3.11)$$

$$V = V_{DS(MOS)} - V_{DS(JFET)} \quad (3.12)$$

$$I = -\mathrm{I_{DS(JFET)}} = \mathrm{I_{DS(MOS)}} \quad (3.13)$$

According to Equations (3.7), (3.10), (3.11) and (3.13), $\mathrm{V_{DS(MOS)}}$ can be derived as:

$$\mathrm{V_{DS(MOS)}} = -\frac{\mathrm{I}}{\beta_M . \mathrm{V_{TH}} + \frac{\beta_M}{2\beta_J . V_{po}} I} \quad (3.14)$$

In the end, combining Equations (3.10), (3.12), (3.13) with (3.14), the output characteristics of the basic TBU in Stage 1 can be obtained as:

$$V = \frac{I}{2\beta_J . V_{po}} - \frac{I}{\beta_M . \mathrm{V_{TH}} + \frac{\beta_M}{2\beta_J . V_{po}} I} \quad (3.15)$$

Stage 2: The MOSFET enters the saturation region while the JFET remains in the linear region (assuming $V_{po} > -\mathrm{V_{TH}}$).

When the voltage across the TBU continues to increase, at some point, either the MOSFET or the JFET will first enter the saturation region.

When the following condition is met, a n-channel MOSFET operates in the saturation region [5]:

$$V_{DS(MOS)} \geq V_{GS(MOS)} - V_{TH} \quad (3.16)$$

Substituting Equations (3.11) and (3.12) into (3.16), the saturation condition of the MOSFET becomes:

$$V = V_{DS(MOS)} - V_{DS(JFET)} \geq -V_{TH} \tag{3.17}$$

Similarly, the saturation condition of p-channel JFET can be derived as:

$$V = V_{DS(MOS)} - V_{DS(JFET)} \geq V_{PO} \tag{3.18}$$

Thus, assuming $V_{po} > -V_{TH}$, the MOSFET will first move into the saturation region.

Figure 3.3(c) shows the equivalent circuit in this stage.

For the n-MOSFET in the saturation region, Equation (3.2) is referred as:

$$I_{DS(MOS)} = \frac{\beta_M}{2}(V_{GS(MOS)} - V_{TH})^2 \tag{3.19}$$

Substituting Equation (3.11) and (3.13) into (3.19), $V_{DS(JFET)}$ is obtained as:

$$V_{DS(JFET)} = \frac{\sqrt{2I}}{\sqrt{\beta_M}} + V_{TH} \tag{3.20}$$

For the p-JFET in the linear region, Equation (3.4) is rearranged as:

$$V_{GS(JFET)} = V_{PO} + \frac{V_{DS(JFET)}}{2} - \frac{I_{DS(JFET)}}{2\beta_J.V_{DS(JFET)}} \tag{3.21}$$

Substituting Equations (3.13) and (3.20) into (3.21), $V_{GS(JFET)}$ is derived as:

$$V_{GS(JFET)} = V_{PO} + \frac{V_{TH}}{2} + \frac{\sqrt{I}}{\sqrt{2\beta_M}} + \frac{\sqrt{\beta_M}}{2\beta_J.(\sqrt{2I}+V_{TH}\sqrt{\beta_M})}.I \tag{3.22}$$

According to the circuit in Figure 3.3(a), the following relationship is found:

$$V_{GS(JFET)} = V_{DS(MOS)} \tag{3.23}$$

In the end, according to the Equations (3.12), (3.19), (3.21) and (3.22), the output expression in Stage 2 is obtained as:

$$V = V_{PO} - \frac{V_{TH}}{2} - \frac{\sqrt{I}}{\sqrt{2\beta_M}} + \frac{\sqrt{\beta_M}}{2\beta_J.(\sqrt{2I}+V_{TH}\sqrt{\beta_M})}.I \tag{3.24}$$

Stage 3: Both the MOSFET and the JFET operate in the saturation region.

When the voltage across the TBU continues rising beyond Vpo, the JFET is also driven into the saturation region as shown in Figure 3.3(d).

For the MOSFET in the saturation region, Equation (3.20) is recalled as:

$$V_{DS(JFET)} = \frac{\sqrt{2I}}{\sqrt{\beta_M}} + V_{TH}$$

For the JFET in the saturation region, Equation (3.5) is referred as:

$$I_{DS(JFET)} = -\beta_J (V_{GS(JFET)} - V_{PO})^2 \qquad (3.25)$$

According to Equations (3.13), (3.23) and (3.25), $V_{DS(MOS)}$ is obtained as:

$$V_{DS(MOS)} = V_{PO} - \frac{\sqrt{I}}{\sqrt{\beta_J}} \qquad (3.26)$$

In the end, with Equations (3.12), (3.20) and (3.25), the output expression in Stage 3 is derived as:

$$V = V_{PO} - V_{TH} - \sqrt{I}(\frac{\sqrt{2}}{\sqrt{\beta_M}} + \frac{1}{\sqrt{\beta_J}}) \qquad (3.27)$$

In summary, the output characteristics of the basic TBU in each stage are given below:

Stage 1

$$V = \frac{I}{2\beta_J . V_{po}} - \frac{I}{\beta_M . V_{TH} + \frac{\beta_M}{2\beta_J . V_{po}} I} \qquad 0 \le V \le -V_{TH}$$

Stage 2

$$V = V_{PO} - \frac{V_{TH}}{2} - \frac{\sqrt{I}}{\sqrt{2\beta_M}} + \frac{\sqrt{\beta_M}}{2\beta_J . (\sqrt{2I} + V_{TH}\sqrt{\beta_M})} . I \qquad -V_{TH} \le V < V_{PO}$$

Stage 3

$$V = V_{PO} - V_{TH} - \sqrt{I}(\frac{\sqrt{2}}{\sqrt{\beta_M}} + \frac{1}{\sqrt{\beta_J}}) \qquad V \ge V_{PO}$$

3.4 Simulation Validation of the Basic TBU

Pspice simulator is used for simulating the operating process of the basic TBU. All parameters used for simulation are identical to the theoretic calculations as list in Table 3.1.

Table 3.1 Parameters for both simulation and calculations

Components	**Parameter**	**Value**	**Remark**
n-channel MOSFET	Threshold voltage V_{TH}	-1.2 V	
	Gain factor β_M (KP=2e-4, W=0.114, L=2e-5)	1.14	MOSFET SPICE model does not include the gain factor but can be calculated by KP using Equation (3.3)
p-channel JFET	Pinch-off voltage V_{PO}	7 V	
	Gain factor β_J	0.0065	

Theoretical calculations

Substituting the parameters in Table 3.1 into the output equations derived in previous section, the calculated expressions in three stages of the basic TBU are obtained below:

$$V = 11I - \frac{I}{-1.37+ \quad .5I} \qquad 0 \le V \le 1.2$$

$$V = 7.6 - \frac{5.9\sqrt{I}+564I}{8.9-9.8\sqrt{I}} \qquad 1.2 \le V < 7$$

$$V = 8.2 - 13.7\sqrt{I} \qquad V \ge 7$$

Figure 3.4 compares the calculated results with the simulated results. As it can be seen, an excellent match between the analytical results and simulated results has been achieved in Stage 2 and Stage 3 whereas the discrepancy is noticeable in Stage 1, which is due to the linear assumption of theoretical analysis since it does not hold true during the transition period from the linear region to the saturation region.

Overall, the simulated results validate the correctness of the theoretical analysis.

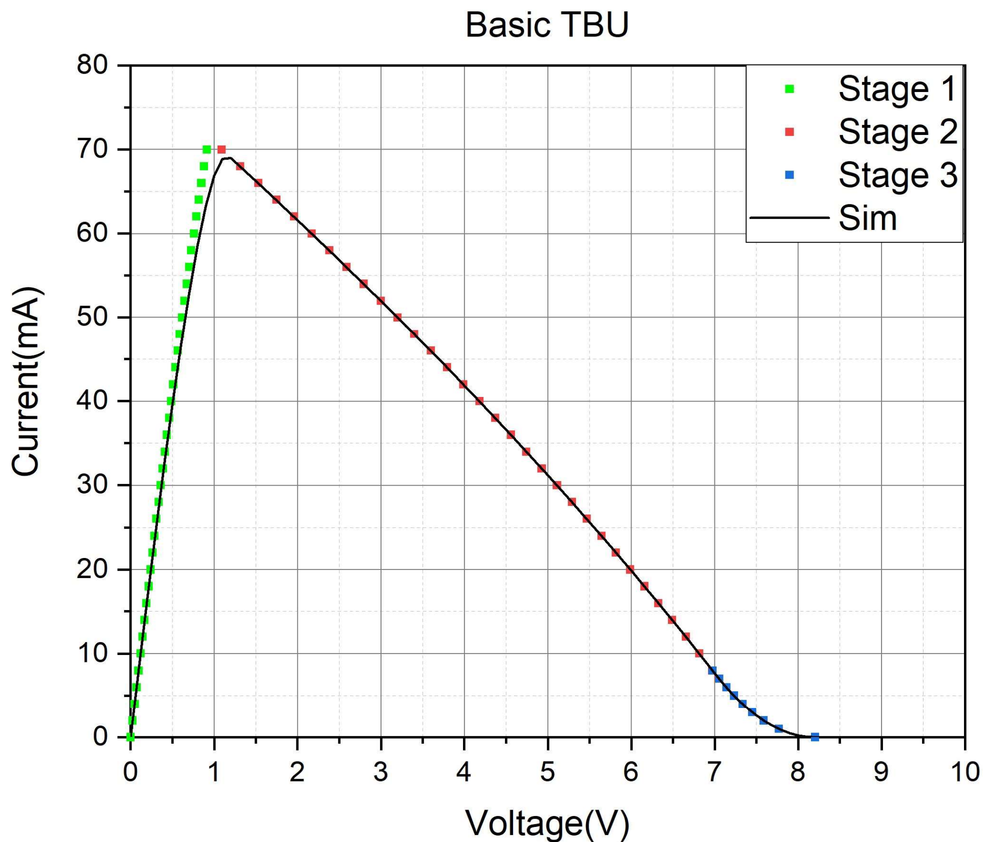


Figure 3.4 Comparison of simulated and calculated I-V curve of the basic TBU

3.5 Analysis of the Basic TBU with Two Added Resistors

For practical applications, there are two issues associated with the basic TBU. One is the avalanche of JFET gate caused by the high voltage at off-state of the TBU and the other is the long reset time after the TBU turns off since no discharge path is available for the JFET gate. To address the two issues, two high values of resistor R1, R3 are added to the basic TBU circuit as shown in Figure 3.5. R1 is used for limiting gate leakage current of JFET within its safe limits while R3 acts as a bleed resistor to discharge JFET gate for resetting the TBU.

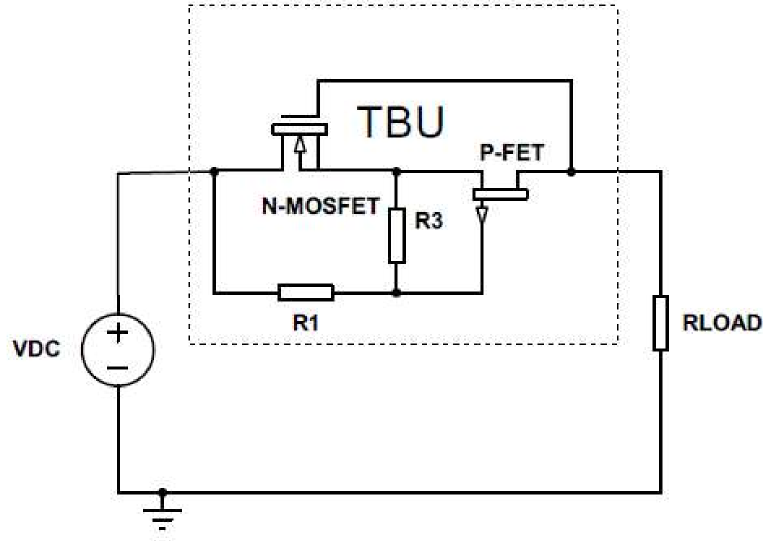


Figure 3.5 Schematic of the basic TBU with two resistors

Similar to the basic TBU, the operating process of this solution also goes through three stages, detailed as follows.

Stage 1: Both n-MOSFET and p- JFET work in the linear regions

This stage is the same as that of the basic TBU because the current flowing through R1 and R3 is negligible due to their much higher resistance than the on-resistance of both MOSFET and JFET. Hence, Equation (3.15) is recalled herein,

$$V = \frac{I}{2\beta_J . V_{po}} - \frac{I}{\beta_M . V_{TH} + \frac{\beta_M}{2\beta_J . V_{po}} I}$$

Stage 2: The MOSFET enters the saturation region while the JFET remains in the linear region (assuming$\left|(1+r)V_{po}\right| > |V_{TH}|$).

For the MOSFET, it will move in the saturation region when the following condition is met:

$$V = V_{DS(MOS)} - V_{DS(JFET)} \geq -V_{TH}$$

According to the circuit in Figure 3.5, the following relationship is found,

$$V_{GS(JFET)} + \frac{R1}{R3} V_{GS(JFET)} = V_{DS(MOS)} \tag{3.28}$$

Defining the ration $r = \frac{R1}{R3}$ and substituting Equation (3.28) into the following express, the voltage across the TBU is obtained,

$$V = V_{DS(MOS)} - V_{DS(JFET)} = (1+r)V_{GS(JFET)} - V_{DS(JFET)} \tag{3.29}$$

Hence, for the JFET, it will operate in the saturation region when the condition below is met:

$$V = V_{DS(MOS)} - V_{DS(JFET)} \geq (1+r)V_{PO}$$

With the assumption of $|(1+r)V_{po}| > |V_{TH}|$, the MOSFET will first move in the saturation region the moment the voltage across TBU reaches the absolute value of threshold voltage of the MOSFET $|V_{TH}|$.

For the MOSFET in the saturation region, recall Equation (3.19)

$$V_{DS(JFET)} = \frac{\sqrt{2I}}{\sqrt{\beta_M}} + V_{TH}$$

For the JFET in the linear region, recall Equation (3.22)

$$V_{GS(JFET)} = V_{PO} + \frac{V_{TH}}{2} + \frac{\sqrt{I}}{\sqrt{2\beta_M}} + \frac{\sqrt{\beta_M}}{2\beta_J.(\sqrt{2I} + V_{TH}\sqrt{\beta_M})} I$$

According to Equations (3.20), (3.22) and (3.29), the output characteristics in Stage 2 is derived as,

$$V = (1+r)V_{PO} - (1-r)\frac{V_{TH}}{2} + \frac{(2(r-1)\beta_J + (1+r)\beta_M)I + \sqrt{2}(r-1)\beta_J\sqrt{\beta_M}V_{TH}\sqrt{I}}{2\beta_J.(\beta_M.V_{TH} + \sqrt{2\beta_M I})} \tag{3.30}$$

Stage 3: Both the MOSFET and the JFET operate in the saturation regions.

For the MOSFET in the saturation region, recall Equation (3.20)

$$V_{DS(JFET)} = \frac{\sqrt{2I}}{\sqrt{\beta_M}} + V_{TH}$$

For the JFET in the saturation region, recall Equation (3.25)

$$I_{DS(JFET)} = \beta_J(V_{GS(JFET)} - V_{PO})^2$$

Rearrange the above equation,

$$V_{GS(JFET)} = V_{PO} - \frac{\sqrt{I}}{\sqrt{\beta_J}} \tag{3.31}$$

Substituting Equations (3.20) and (3.31) into (3.29), the output expression is obtained as,

$$V = (1+r)V_{PO} - V_{TH} - \sqrt{I}\left(\frac{\sqrt{2}}{\sqrt{\beta_M}} + \frac{1+r}{\sqrt{\beta_J}}\right) \qquad (3.32)$$

In summary, the output characteristics of the basic TBU with two added resistors are list as follows,

$$V = \frac{I}{2\beta_J.V_{po}} - \frac{I}{\beta_M.V_{TH} + \frac{\beta_M}{2\beta_J.V_{po}}I} \qquad 0 \le V \le -V_{TH}$$

$$V = (1+r)V_{PO} - (1-r)\frac{V_{TH}}{2} + \frac{(2(r-1)\beta_J + (1+r)\beta_M)I + \sqrt{2}(r-1)\beta_J\sqrt{\beta_M}V_{TH}\sqrt{I}}{2\beta_J.(\beta_M.V_{TH} + \sqrt{2\beta_M I})}$$

$$-V_{TH} \le V < (1+r)V_{PO}$$

$$V = (1+r)V_{PO} - V_{TH} - \sqrt{I}\left(\frac{\sqrt{2}}{\sqrt{\beta_M}} + \frac{1+r}{\sqrt{\beta_J}}\right) \qquad V \ge (1+r)V_{PO}$$

3.6 Simulation Validation of the Basic TBU with two Added Resistors

The value of each parameter for both calculations and simulation are taken from Table 3.1 while the resistance of R1 and R3 use the same value of 2.2MΩ.

Substituting these parameters into the output equations, the calculated results are obtained below.

$$V = 11I - \frac{I}{-1.37 + 12.5I} \qquad 0 \le V \le 1.2$$

$$V = 14 - \frac{175.4I}{1.37 - \ .5\sqrt{I}} \qquad 1.2 \le V < 14$$

$$V = 15.2 - 26.1\sqrt{I} \qquad V \ge 14$$

As shown in Figure 3.6, the simulated results demonstrate a good fit with the calculated results in both Stage 2 and Stage 3 whereas the discrepancy in Stage 1 is due to the linear assumption of theoretical analysis, which does not hold true during the period from the end of linear region to the beginning of saturation region.

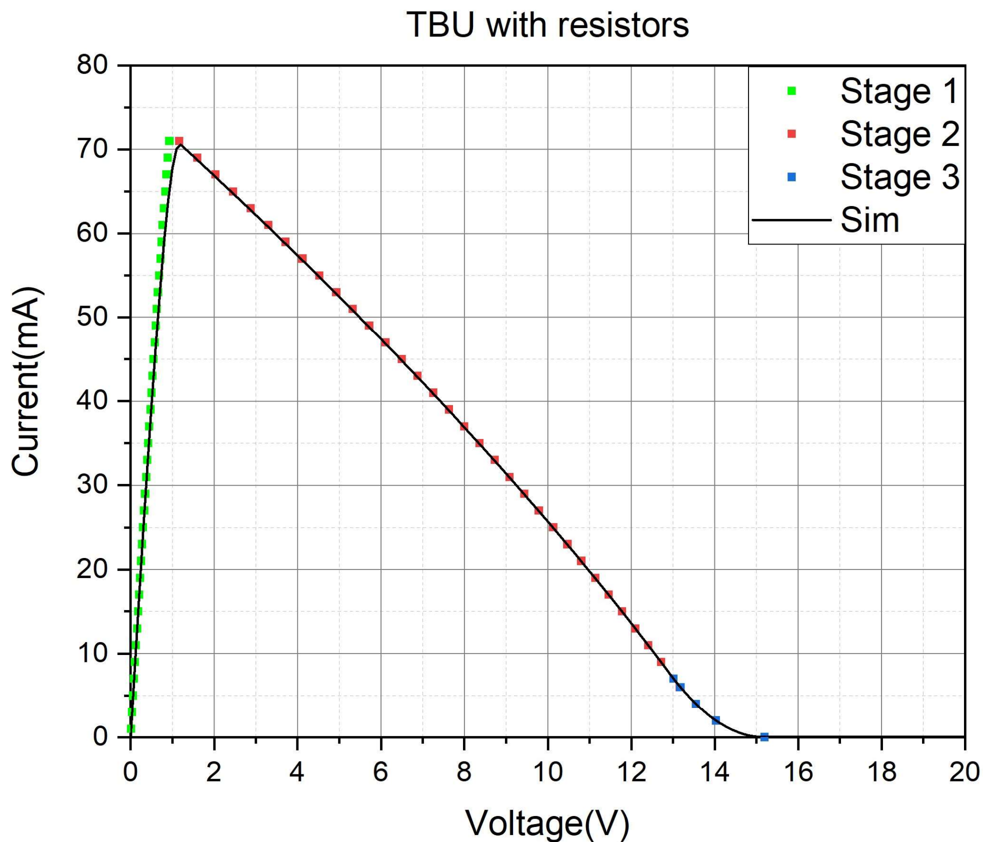


Figure 3.6 Comparison of simulated and calculated I-V curves of the basic TBU with two resistors

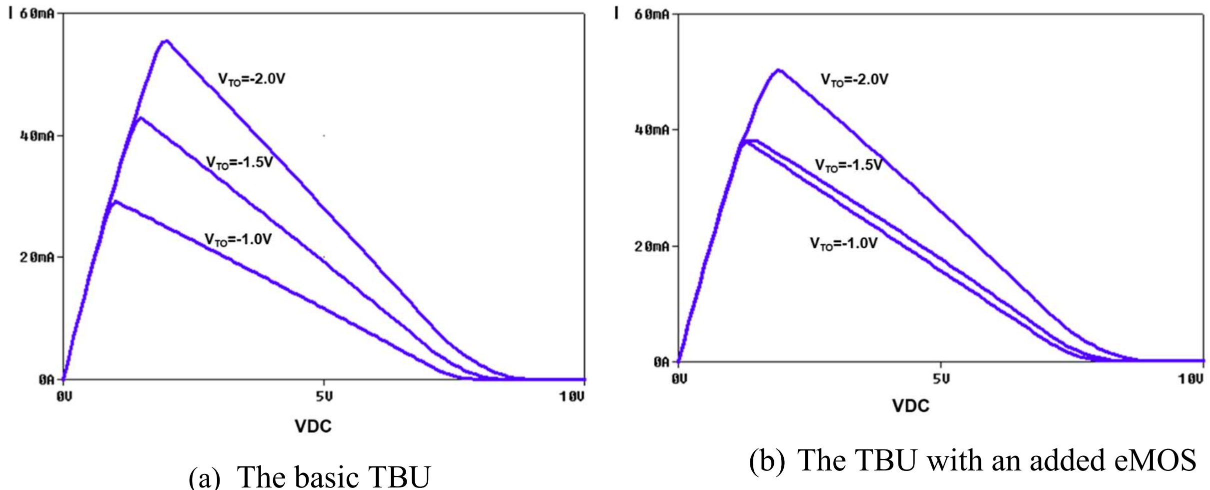
3.7 Analysis of the Basic TBU with an Added Enhancement Mode MOSFET

Figure 3.7(a) demonstrates how the basic TBU output characteristics are affected by the threshold voltages of the depletion mode n-channel MOSFET. The results reveal that tripping current level of the basic TBU are highly sensitive to the variation of the threshold voltage of the MOSFET. Compared to the enhancement MOSFET, the threshold voltages of depletion mode MOSFETs has much higher variants due to a buried-channel conduction present in the depletion mode devices[5]. This would cause extreme difficulty for manufacturers to control product consistency.

To address this issue, an enhancement mode MOSFET with a stable threshold voltage is added to the circuit as shown in Figure 3.8. When the voltage drops across the p-channel JFET (pJFET) approaches the threshold voltage of enhancement mode MOSFET (eMOS), the eMOS

turns on and therefore pulls down the gate voltage of the depletion mode MOSFET (dMOS). Since that, the TBU starts to limit the current towards the cut-off region.

As shown in Figure 3.7(b), the TBU with the eMOS demonstrates a much-improved performance in terms of the tolerance of tripping current level against the variation of the threshold voltage of the dMOS. It is worth noticing that the TBU loses control at the negative threshold voltage below -2.0V because the TBU becomes a basic TBU when the very negative threshold voltage simply turns the eMOS hard on.



(a) The basic TBU

(b) The TBU with an added eMOS

Figure 3.7 Output current of the TBU with varied threshold voltage

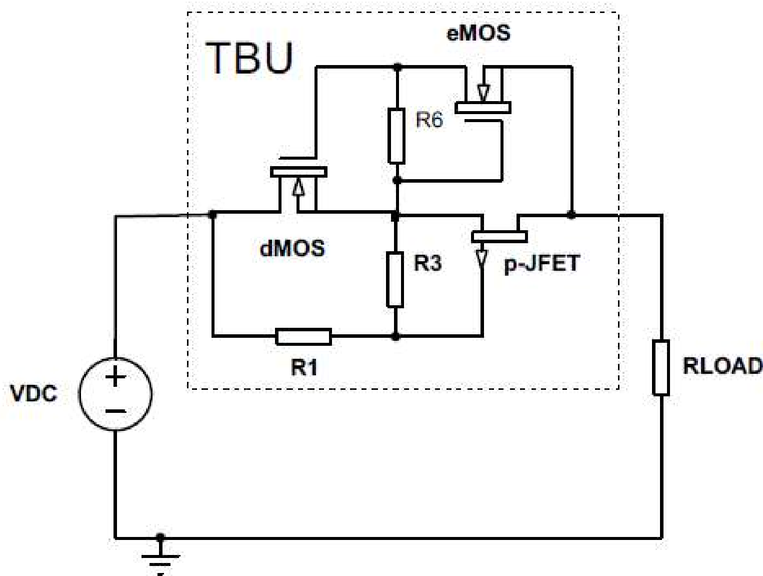


Figure 3.8 TBU with added enhancement mode MOSFET

The operating process of the TBU with the added eMOS is divided into 4 stages, detailed as below:

Stage 1: Both the dMOS and the pJFET operate in the linear region before the eMOS turns on

For the dMOS in the linear region, recall Equation (3.6)

$$I_{DS(dMOS)} = \frac{\beta_{dM}}{2}\left[2\left(V_{GS(dMOS)} - V_{dTH}\right)V_{DS(dMOS)} - V_{DS(dMOS)}{}^{2}\right]$$

Before the eMOS turns on, according to the circuit in Figure 3.8, it can be found:

$$V_{GS(dMOS)} = 0$$

Hence,

$$I_{DS(dMOS)} = -\beta_{dM}.V_{dTH}.V_{DS(dMOS)} - V_{DS(dMOS)}{}^{2} \tag{3.33}$$

Assuming the linear I-V relationship during this period, Equation (3.32) can be simplified as:

$$I_{DS(dMOS)} = -\beta_{dM}.V_{dTH}.V_{DS(dMOS)}$$

Rearrange the equation as:

$$V_{DS(dMOS)} = -\frac{I_{DS(dMOS)}}{\beta_{dM}V_{dTH}} \tag{3.34}$$

For the pJFET in the linear region, recall Equation (3.10) as,

$$V_{DS(JFET)} = \frac{I_{DS(JFET)}}{2\beta_J.V_{po}}$$

According to the circuit condition, the relationships (3.12) and (3.13) still hold on:

Voltage cross the TBU $V = V_{DS(MOS)} - V_{DS(JFET)}$

Current flowing through the TBU $I = -I_{DS(JFET)} = I_{DS(MOS)}$

In the end, based on Equation (3.10), (3.12), (3.13) and (3.34), the output express of the TBU in Stage 1 can be obtained as

$$V = V_{DS(dMOS)} - V_{DS(JFET)} = \frac{I}{2\beta_J V_{po}} - \frac{I}{\beta_{dM}V_{dTH}} \tag{3.35}$$

Stage 2: The dMOS enters the saturation region while pJFET remains in the linear region after eMOS turns on

When the voltage across the pJFET exceeds the threshold voltage V_{eTH} of eMOS, the eMOS turns on and its drain voltage is being pulled down driving the dMOS into the saturation region. For the dMOS in the saturation region, Equation (3.2) is referred as:

$$I_{DS(dMOS)} = \frac{\beta_{dM}}{2}(V_{GS(dMOS)} - V_{dTH})^2$$

Rearrange the equation as:

$$V_{GS(dMOS)} = \frac{\sqrt{2I_{DS(dMOS)}}}{\sqrt{\beta_{dM}}} + V_{dTH} \tag{3.36}$$

According to the circuit in Figure 3.8, the drain current of the eMOS can be calculated as:

$$I_{DS(eMOS)} = \frac{-V_{GS(dMOS)}}{R_6} \tag{3.37}$$

Substituting Equation (3.36) into (3.37), the drain current of eMOS is obtained as:

$$I_{DS(eMOS)} = -\frac{\sqrt{2I_{DS(dMOS)}}}{R_6\sqrt{\beta_{dM}}} - \frac{V_{dTH}}{R_6} \tag{3.38}$$

The eMOS will operate in the saturation region when the following condition is met:

$$V_{DS(eMOS)} \geq V_{GS(eMOS)} - V_{eTH}$$

According to the circuit in Figure 3.8

$$V_{DS(eMOS)} = V_{GS(eMOS)} + V_{GS(dMOS)}$$

Hence, the eMOS operates in the saturation region when the following condition is met:

$$-V_{GS(dMOS)} < V_{eTH} \tag{3.39}$$

When the eMOS is in the saturation region, Equation (3.2) is referred as:

$$I_{DS(eMOS)} = \frac{\beta_{eM}}{2}(V_{GS(eMOS)} - V_{eTH})^2$$

And can be rearranged as:

$$V_{GS(eMOS)} = \frac{\sqrt{2I_{DS(eMOS)}}}{\sqrt{\beta_{eM}}} + V_{eTH} \tag{3.40}$$

Substituting the equations (3.38) into (3.40), the gate voltage of the eMOS is obtained as:

$$V_{GS(eMOS)} = \mathrm{V}_{\mathrm{eTH}} + \sqrt{\frac{-2\beta_{dM}\mathrm{V}_{dTH}\sqrt{\beta_{eM}} - 2\sqrt{2\beta_{eM}\beta_{dM}}\sqrt{I}}{R_6\beta_{eM}\beta_{dM}}} \tag{3.41}$$

For the pJFET in the linear region, Equation (3.8) can be rewritten as:

$$V_{GS(JFET)} = V_{PO} + \frac{V_{DS(JFET)}}{2} - \frac{I_{DS(JFET)}}{2\beta_J . V_{DS(JFET)}}$$

According to the circuit in Figure 3.8, the following relationships are found,

$$-\mathrm{V}_{\mathrm{DS(JFET)}} = V_{GS(eMOS)}; I = -\mathrm{I}_{\mathrm{DS(JFET)}} = \mathrm{I}_{\mathrm{DS(MOS)}}$$

Recall Equation (3.29) as:

$$V = V_{DS(MOS)} - V_{DS(JFET)} = (1 + r)V_{GS(JFET)} - V_{DS(JFET)}$$

Finally, based on Equation (3.8), (3.29) and (3.41), the output characteristics of the TBU in Stage 2 is derived as:

$$\mathrm{V} = (1+\mathrm{r})\mathrm{V}_{\mathrm{po}} + (1-\mathrm{r})\frac{\mathrm{V}_{\mathrm{eTH}} + \sqrt{\frac{-2\beta_{dM}\mathrm{V}_{dTH}\sqrt{\beta_{eM}} - 2\sqrt{2\beta_{eM}\beta_{dM}}\sqrt{I}}{R_6\beta_{eM}\beta_{dM}}}}{2} - \frac{(1+\mathrm{r})\mathrm{I}}{2\beta_J(\mathrm{V}_{\mathrm{eTH}} + \sqrt{\frac{-2\beta_{dM}\mathrm{V}_{dTH}\sqrt{\beta_{eM}} - 2\sqrt{2\beta_{eM}\beta_{dM}}\sqrt{I}}{R_6\beta_{eM}\beta_{dM}}})} \quad (3.42)$$

Stage 3: The dMOS stays on the saturation region while both the eMOS and the pJFET operate in the linear regions.

For the dMOS in the saturation region, call back Equation (3.36):

$$V_{GS(dMOS)} = \frac{\sqrt{2I_{DS(dMOS)}}}{\sqrt{\beta_{dM}}} + V_{dTH}$$

For eMOS in the linear region, Equation (3.6) is referred as,

$$\mathrm{I}_{\mathrm{DS(eMOS)}} = \frac{\beta_{\mathrm{eM}}}{2}[2(\mathrm{V}_{\mathrm{GS(eMOS)}} - \mathrm{V}_{\mathrm{eTH}})\mathrm{V}_{\mathrm{DS(eMOS)}} - \mathrm{V}_{\mathrm{DS(eMOS)}}{}^2] \quad (3.43)$$

Equation (3.43) can be simplified by assuming linear I-V relationship of the eMOS:

$$\mathrm{I}_{\mathrm{DS(eMOS)}} = \beta_{\mathrm{eM}}(\mathrm{V}_{\mathrm{GS(eMOS)}} - \mathrm{V}_{\mathrm{eTH}})\mathrm{V}_{\mathrm{DS(eMOS)}} \quad (3.44)$$

According to the circuit in Figure 3.8,

$$V_{DS(eMOS)} = V_{GS(eMOS)} + V_{GS(dMOS)}; I = -\mathrm{I}_{\mathrm{DS(JFET)}} = \mathrm{I}_{\mathrm{DS(MOS)}}$$

Substituting Equations (3.36), (3.38) and (3.44) into the above expressions, $V_{GS(eMOS)}$ is derived as:

$$V_{GS(eMOS)} = \frac{V_{eTH} - V_{dTH} - \frac{\sqrt{2I}}{\sqrt{\beta_{dM}}} + \sqrt{\frac{2I}{\beta_{dM}} + (V_{eTH} + V_{dTH})^2 + \frac{4V_{dTH}}{R_6\beta_{eM}} + \frac{2\beta_{eM}R_6\sqrt{2\beta_{dM}}(V_{eTH} + V_{dTH}) + 4\sqrt{2\beta_{dM}}}{R_6\beta_{eM}\beta_{dM}}\sqrt{I}}}{2}$$

Due to the high resistance of R6, the above equation can be simplified as:

$$V_{GS(eMOS)} = \frac{V_{eTH} - V_{dTH} - \frac{\sqrt{2I}}{\sqrt{\beta_{dM}}} + \sqrt{\frac{2I}{\beta_{dM}} + (V_{eTH} + V_{dTH})^2}}{2} \tag{3.45}$$

Hence, the drain voltage of PJFET is obtained as:

$$\mathrm{V_{DS(JFET)}} = -V_{GS(eMOS)} = -\frac{V_{eTH} - V_{dTH} - \frac{\sqrt{2I}}{\sqrt{\beta_{dM}}} + \sqrt{\frac{2I}{\beta_{dM}} + (V_{eTH} + V_{dTH})^2}}{2} \tag{3.46}$$

For the JFET in the linear region, recall Equation (3.21):

$$V_{GS(JFET)} = V_{PO} + \frac{V_{DS(JFET)}}{2} - \frac{I_{DS(JFET)}}{2\beta_J . V_{DS(JFET)}}$$

Finally, the output expression of the TBU in Stage 3 is figured out as:

$$V = V_{DS(DMOS)} - V_{DS(JFET)} = (1 + r)V_{GS(JFET)} - V_{DS(JFET)}$$

$$= (1 + r)V_{PO} + (1 - r)\frac{V_{eTH} - V_{dTH}}{4} + (1 - r)\frac{\sqrt{\frac{2I}{\beta_{dM}} + (V_{eTH} + V_{dTH})^2}}{4} -$$

$$\frac{\left(4(1+r)\beta_{dM} - 2(1-r)\beta_J\right)I + (1-r)\beta_J\sqrt{2\beta_{dM}}(V_{eTH} - V_{dTH})\sqrt{I} + (1-r)\beta_J\sqrt{2I^2 + I\beta_{dM}(V_{eTH} + V_{dTH})^2}}{8\beta_J((V_{eTH} - V_{dTH}) - \sqrt{2\beta_{dM}I} + \sqrt{2\beta_{dM}I + 2(V_{eTH} + V_{dTH})^2})} \tag{3.47}$$

Stage 4: both the dMOS and the pJFET operate in the saturation region while the eMOS stays on the linear region

For the dMOS in the saturation region, recall Equation (3.36):

$$V_{GS(dMOS)} = \frac{\sqrt{2I_{DS(dMOS)}}}{\sqrt{\beta_{dM}}} + V_{dTH}$$

For the JFET in the saturation region, Equation (3.31) is referred as,

$$V_{GS(JFET)} = V_{PO} - \frac{\sqrt{I}}{\sqrt{\beta_J}}$$

For the eMOS in the linear region, recall Equation (3.45)

$$V_{GS(eMOS)} = \frac{V_{eTH} - V_{dTH} - \frac{\sqrt{2I}}{\sqrt{\beta_{dM}}} + \sqrt{\frac{2I}{\beta_{dM}} + \quad (V_{eTH+}V_{dTH})^2}}{2}$$

In the end, the I-V relationship of TBU is derived as,

$$V = V_{DS(MOS)} - V_{DS(JFET)} = (1 + r)V_{GS(JFET)} - V_{DS(JFET)}$$

$$= (1 + r)V_{PO} + \frac{V_{eTH} - V_{dTH}}{2} - \sqrt{I}\left(\frac{1}{\sqrt{2\beta_{dM}}} + \frac{1+r}{\sqrt{\beta_J}}\right) + \frac{1}{2}\sqrt{\frac{2I}{\beta_{dM}} + (V_{eTH+}V_{dTH})^2} \qquad (3.48)$$

To sum up, the output characteristics of the TBU with the added enhancement MOSFET are list as follows:

Stage 1:

$$V = \frac{I}{2\beta_J V_{po}} - \frac{I}{\beta_{dM} V_{dTH}}$$

Stage 2:

$$V = (1 + r)V_{po} + (1 - r)\frac{V_{eTH} + \sqrt{\frac{-2\beta_{dM}\mathrm{V}_{dTH}\sqrt{\beta_{eM}} - 2\sqrt{2\beta_{eM}\beta_{dM}}\sqrt{I}}{R_6\beta_{eM}\beta_{dM}}}}{2} - \frac{(1+r)I}{2\beta_J(V_{eTH} + \sqrt{\frac{-2\beta_{dM}\mathrm{V}_{dT}\ \sqrt{\beta_{eM}} - 2\sqrt{2\beta_{eM}\beta_{dM}}\sqrt{I}}{R_6\beta_{eM}\beta_{dM}}})}$$

Stage 3:

$$V$$

$$= (1 + r)V_{PO} + (1 - r)\frac{V_{eTH} - V_{dTH}}{4} + (1 - r)\frac{\sqrt{\frac{2I}{\beta_{dM}} + \quad (V_{eTH+}V_{dTH})^2}}{4}$$

$$- \frac{\left(4(1 + r)\beta_{dM} - 2(1 - r)\beta_J\right)I + (1 - r)\beta_J\sqrt{2\beta_{dM}}(V_{eTH} - V_{dTH})\sqrt{I} + (1 - r)\beta_J\sqrt{2I^2 + I\beta_{dM}(V_{eTH} + V_{dTH})^2}}{8\beta_J(V_{eTH} - V_{dTH}) - \sqrt{2\beta_{dM}I} + \sqrt{2\beta_{dM}I + 2(V_{eTH} + V_{dTH})^2})}$$

Stage 4:

$$V = (1 + r)V_{PO} + \frac{V_{eTH} - V_{dTH}}{2} - \sqrt{I}\left(\frac{1}{\sqrt{2\beta_{dM}}} + \frac{1 + r}{\sqrt{\beta_J}}\right) + \frac{1}{2}\sqrt{\frac{2I}{\beta_{dM}} + (V_{eTH+}V_{dTH})^2}$$

The above expressions are too complicated for practical use. Hence, they are simplified as three stages with some good approximations:

Stage 1:

$$V = \frac{I}{2\beta_J V_{po}} - \frac{I}{\beta_{dM} V_{dTH}} \qquad 0 \leq \mathrm{V} \leq V_{eTH} \frac{\beta_{dM} V_{dT} \quad 2\beta_J V_{po}}{\beta_{dM} V_{dTH}}$$

Stage 2:

$$V = (1+r)V_{PO} + (1-r)\frac{V_{eTH} - V_{dTH}}{4} - \frac{(1+r)I}{2.1\beta_J V_{eTH}}$$

$$V_{eTH} \frac{\beta_{dM} V_{dTH} - 2\beta_J V_{po}}{\beta_{dM} V_{dTH}} < V \leq (1+r)V_{po} - rV_{eTH}$$

Stage 3:

$$V = (1+r)V_{PO} + \frac{V_{eTH} - V_{dTH}}{2} - \sqrt{I}\left(\frac{1}{\sqrt{2\beta_{dM}}} + \frac{1+r}{\sqrt{\beta_J}}\right) \qquad V > (1+r)V_{po} - rV_{eTH}$$

3.8 Simulation Validation of the TBU with an Added Enhancement MOSFET

The values of each component parameters for both the simulations and calculations are list in Table 3.2.

Table 3.2 Value of component parameters

Components	**Parameter**	**Value**
Depletion mode MOSFET (dMOS)	Threshold voltage V_{dTH}	-1.2 V
	*Gain factor β_{dM}	1.14
p-channel JFET (pJFET)	Pinch-off voltage V_{PO}	7 V
	Gain factor β_J	0.0065
Enhancement mode MOSFET (eMOS)	Threshold voltage V_{eTH}	0.9 V
	*Gain factor β_{eM}	0.082
R1	Resistance	2.2MΩ
R3	Resistance	2.2MΩ
Note	*SPICE MOSFET models do not include the gain factors which can be calculated through KP using the equation (3.3)	

Substituting the parameter values given in Table 3.2 into the output expression of the TBU in each stage, the calculated results are,

$$V = 12I \qquad 0 \leq V \leq 0.96$$

$V = 14 \; - 162.8I \qquad\qquad 0.96 \le V < 13.1$

$V = 15.1 - 25.5\sqrt{I} \qquad\qquad V \ge 13.1$

Figure 3.9 compares the simulation result against the calculated results. It demonstrates an excellent match in both Stage 2 and Stage 3 while a small discrepancy is shown in Stage 1.

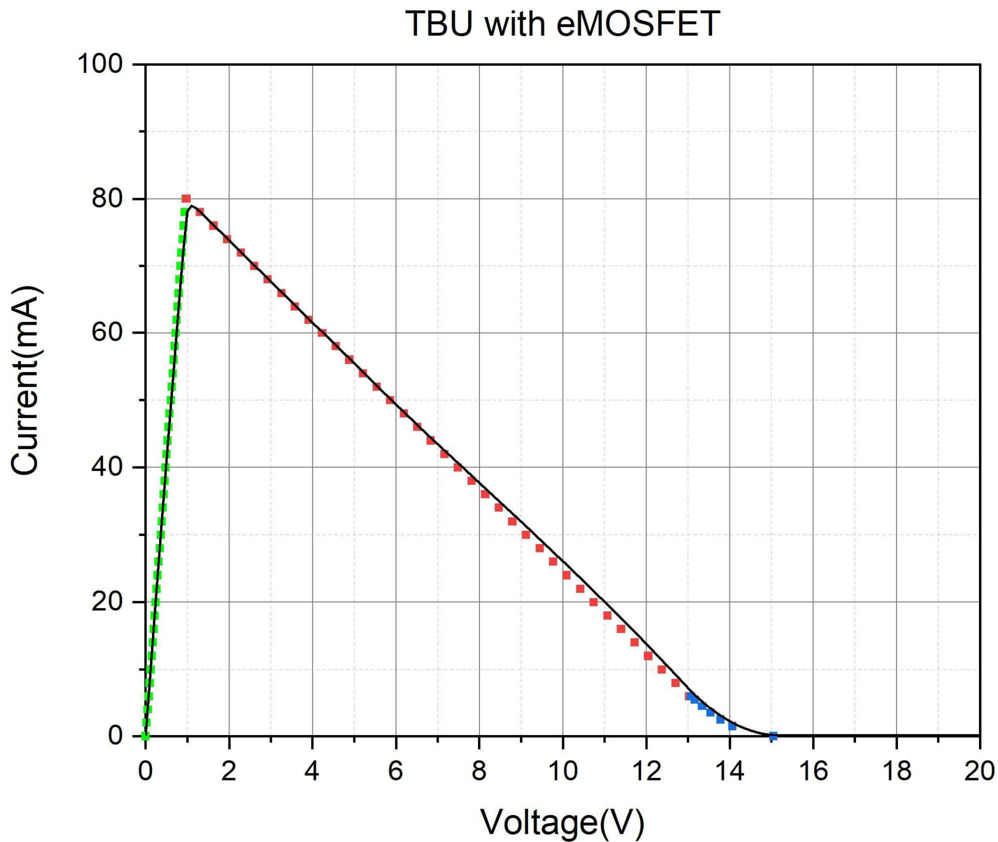


Figure 3.9 Comparison of simulated and calculated I-V curve of the TBU with eMOS

3.9 Analysis of the TBU with Added Diodes (practical TBUs)

The practical TBU is a bidirectional device using two back-to-back depletion mode n-MOSFETs in series with a p-JFET in the middle as shown in Figure 3.10. A number of diodes in either direction are added in the gate path of the p-JFET to protect the JFET gate from high voltage at the turn-off of the TBU.

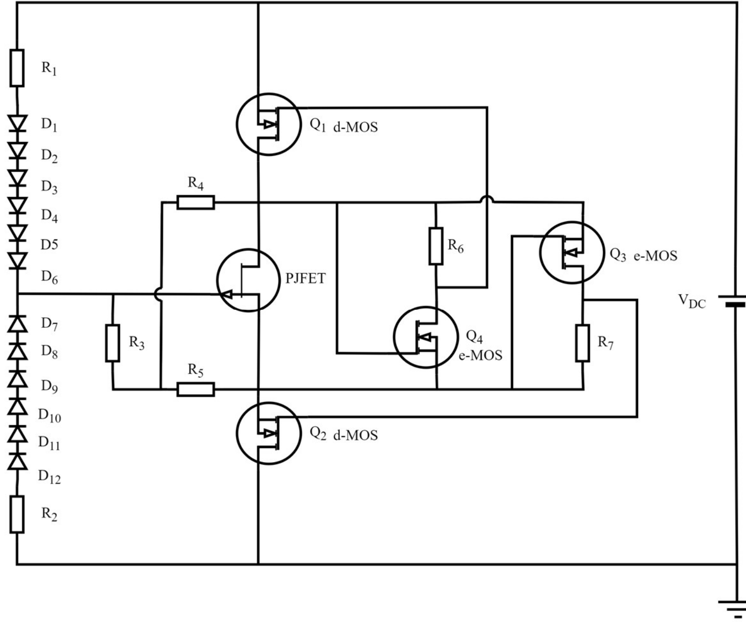


Figure 3.10 Practical bidirectional TBUs

Without compromising the accuracy, a unidirectional TBU is now analysed. Taking the same approach as with the previous analysis, the operating process of the practical TBU is divided into several stages as follows.

Two scenarios are considered for this analysis.

Scenario 1: Diodes stay off-state before the eMOS turns on

Stage 1: Both the dMOS and the pJFET operate in the linear region before eMOS turns on.

Equation (3.35) is straightforward taken for this stage as the process is the same of Stage 1 of the TBU with added eMOS.

$$V = \frac{I}{2\beta_J V_{po}} - \frac{I}{\beta_{dM} V_{dTH}}$$

Stage 2: The dMOS enters the saturation region while the pJFET remains in the linear region after the eMOS turns on

Due to the reverse biases state of the diodes, the gate-source voltage $V_{GS(JFET)}$ of the PJFET remains zero while its source-drain voltage $V_{SD(JFET)}$ is clamped by the threshold voltage V_{eTH} of the eMOS. Consequently, the current of the TBU stands on at a certain level, estimated by

$$I \cong 2.1\beta_J V_{po} V_{eTH} \tag{3.49}$$

Stage 3: Both the dMOS and the eMOS stay in the saturation region while the pJFET remains in the linear region after diodes start conducting.

Since this stage is similar to Stage 2 of the TBU with eMOS, Equation (3.42) is referred and an item is added associated with the diodes as,

$$V = (1+r)V_{po} + n \times V_{POLYD} + (1-r)\frac{V_{eTH} + \sqrt{\frac{-2\beta_{dM}V_{dTH}\sqrt{\beta_{eM}} - 2\sqrt{2\beta_{eM}\beta_{dM}}\sqrt{I}}{R_6\beta_{eM}\beta_{dM}}}}{2} - \frac{(1+r)I}{2\beta_J\left(V_{eTH} + \sqrt{\frac{-2\beta_{dM}V_{dTH}\sqrt{\beta_{eM}} - 2\sqrt{2\beta_{eM}\beta_{dM}}\sqrt{I}}{R_6\beta_{eM}\beta_{dM}}}\right)} \quad (3.50)$$

Where n is the number of diodes in one direction and V_{POLYD} is the knee voltage of a single diode.

Stage 4: The dMOS stays in the saturation region and pJFET remains in the linear region while eMOS enters the linear region.

Since it is the same of Stage 3 of the TBU with eMOS, Equation (3.47) is referred as the output expression of the TBU in this stage:

$$V = (1+r)V_{PO} + n \times V_{POLYD} + (1-r)\frac{V_{eTH} - V_{dTH}}{4} + (1-r)\frac{\sqrt{\frac{2I}{\beta_{dM}} + (V_{eTH} + V_{dTH})^2}}{4} - \frac{(4(1+r)\beta_{dM} - 2(1-r)\beta_J)I + (1-r)\beta_J\sqrt{2\beta_{dM}}(V_{eTH} - V_{dTH})\sqrt{I} + (1-r)\beta_J\sqrt{2I^2 + I\beta_{dM}(V_{eTH} + V_{dTH})^2}}{8\beta_J(V_{eTH} - V_{dTH}) - \sqrt{2\beta_{dM}I} + \sqrt{2\beta_{dM}I + 2(V_{eTH} + V_{dTH})^2})} \quad (3.51)$$

Stage 5: The dMOS stays in the saturation region and eMOS in the linear region while pJFET moves in the saturation region

The I-V relationship of the TBU in this stage can be developed from Equation (3.48) by adding an item associated with the diodes as follow.

$$V = (1+r)V_{PO} + \frac{V_{eTH} - V_{dTH}}{2} + n \times V_{POLYD} - \sqrt{I}\left(\frac{1}{\sqrt{2\beta_{dM}}} + \frac{1+r}{\sqrt{\beta_J}}\right) + \frac{1}{2}\sqrt{\frac{2I}{\beta_{dM}} + (V_{eTH} + V_{dTH})^2} \quad (3.52)$$

Scenario 2: The diodes are conduction before eMOS turns on

Stage 1: Both the dMOS and the pJFET operate in the linear region before eMOS turns on.

This process is identical to Stage 1 in Scenarios 1 except the voltage boundaries. Thus, I-V relationship of the TBU in this stage is taken from Equation (3.35):

$$V = \frac{I}{2\beta_J V_{po}} - \frac{I}{\beta_{dM}V_{dTH}}$$

Stage 2: Both the dMOS and the pJFET operate in the linear region after the eMOS turns on.

For the dMOS in the linear region, recall Equation (3.34):

$$V_{DS(dMOS)} = -\frac{I_{DS(dMOS)}}{\beta_{dM} V_{dTH}}$$

For the JFET in the linear region, recall Equation (3.8):

$$I_{DS(JFET)} = -\beta_J \left[2\left(V_{GS(JFET)} - V_{po}\right) V_{DS(JFET)} - V_{DS(JFET)}{}^2\right]$$

And can be simplified by the linear assumption of I-V relationship during this period:

$$I_{DS(JFET)} = -2\beta_J \left(V_{GS(JFET)} - V_{po}\right) V_{DS(JFET)})$$

In accordance with the circuit in Figure 3.10, the following relationship is found:

$$V_{GS(JFET)} + \frac{R1}{R3} V_{GS(JFET)} + n \times V_{POLYD} = V_{DS(dMOS)} \tag{3.53}$$

Based on the above equations, the I-V relationship of the TBU in this stage can be figured out:

$$V = V_{DS(dMOS)} - V_{DS(JFET)} = \frac{(1+r)I}{2(1+r)\beta_J V_{po} + n \times V_{POLYD} + \frac{1}{\beta_{dM} V_{dTH}}} - \frac{I}{\beta_{dM} V_{dTH}} \tag{3.54}$$

Stage 3, Stage 4 and Stage 5 are exactly same to the corresponding stages in Scenario 1 except the boundaries.

Finally, the output characteristics of the practical TBUs are summarized as:

Stage 1(same for two scenarios)

$$V = \frac{I}{2\beta_J V_{po}} - \frac{I}{\beta_{dM} V_{dTH}}$$

Stage 2

Scenarios 1

$$I \cong 2.1 \beta_J V_{po} V_{eTH}$$

Scenarios 2

$$V = \frac{(1+r)I}{2(1+r)\beta_J V_{po} + n \times V_{POLYD} + \frac{1}{\beta_{dM} V_{dTH}}} - \frac{I}{\beta_{dM} V_{dTH}}$$

Stage 3 (same for two scenarios)

$$V = (1+r)V_{po} + n \times V_{POLYD} + (1-r)\frac{V_{eTH} + \sqrt{\frac{-2\beta_{dM}V_{dTH}\sqrt{\beta_{eM}} - 2\sqrt{2\beta_{eM}\beta_{dM}}\sqrt{I}}{R_6\beta_{eM}\beta_{dM}}}}{2} - \frac{(1+r)I}{2\beta_J(V_{eTH} + \sqrt{\frac{-2\beta_{dM}V_{dTH}\sqrt{\beta_{eM}} - 2\sqrt{2\beta_{eM}\beta_{dM}}\sqrt{I}}{R_6\beta_{eM}\beta_{dM}}})}$$

Stage 4 (same for two scenarios)

$$V = (1+r)V_{PO} + n \times V_{POLYD} + (1-r)\frac{V_{eTH} - V_{dTH}}{4} + (1-r)\frac{\sqrt{\frac{2I}{\beta_{dM}} + (V_{eTH} + V_{dTH})^2}}{4} - \frac{\left(4(1+r)\beta_{dM} - 2(1-r)\beta_J\right)I + (1-r)\beta_J\sqrt{2\beta_{dM}}(V_{eTH} - V_{dTH})\sqrt{I} + (1-r)\beta_J\sqrt{2I^2 + I\beta_{dM}(V_{eTH} + V_{dTH})^2}}{8\beta_J(V_{eTH} - V_{dTH}) - \sqrt{2\beta_{dM}I} + \sqrt{2\beta_{dM}I + 2(V_{eTH} + V_{dTH})^2})}$$

Stage 5 (same for two scenarios)

$$V = (1+r)V_{PO} + \frac{V_{eTH} - V_{dTH}}{2} + n \times V_{POLYD} - \sqrt{I}\left(\frac{1}{\sqrt{2\beta_{dM}}} + \frac{1+r}{\sqrt{\beta_J}}\right) + \frac{1}{2}\sqrt{\frac{2I}{\beta_{dM}} + (V_{eTH} + V_{dTH})^2}$$

The above complex expressions can be approximated below:

Scenarios 1: The diodes are off-state before eMOS turns on

Stage 1

$$V = \frac{I}{2\beta_J V_{po}} - \frac{I}{\beta_{dM}V_{dTH}} \qquad 0 \le V \le V_{eTH}\frac{\beta_{dM}V_{dTH} - 2\beta_J V_{po}}{\beta_{dM}V_{dTH}}$$

Stage 2

$$I \cong 2.1\beta_J V_{po} V_{eTH} \qquad V_{eTH}\frac{\beta_{dM}V_{dTH} - 2\beta_J V_{po}}{\beta_{dM}V_{dTH}} < V \le n \times V_{polyd} + V_{eTH}$$

Stage 3

$$V = (1+r)V_{PO} + (1-r)\frac{V_{eTH} - V_{dTH}}{4} + n \times V_{polyd} - \frac{(1+r)I}{2.1\beta_J V_{eTH}}$$

$$V_{eTH} + n \times V_{polyd} < V \le (1+r)V_{po} - rV_{eTH} + n \times V_{polyd}$$

Stage 4

$$V = (1+r)V_{PO} + \frac{V_{eTH} - V_{dTH}}{2} + n \times V_{polyd} - \sqrt{I}\left(\frac{1}{\sqrt{2\beta_{dM}}} + \frac{1+r}{\sqrt{\beta_J}}\right)$$

$$V > (1+r)V_{po} - rV_{eTH} + n \times V_{polyd}$$

Scenarios 2: The diodes are conducting before eMOS turns on

Stage 1

$$V = \frac{I}{2\beta_J V_{po}} - \frac{I}{\beta_{dM} V_{dTH}} \qquad 0 \le V \le V_{eTH} \frac{\beta_{dM} V_{dTH-} 2\beta_J V_{po}}{\beta_{dM} V_{dTH}}$$

Stage 2

$$V = (1+r)V_{PO} + (1-r)\frac{V_{eTH} - V_{dTH}}{4} + n \times V_{polyd} - \frac{(1+r)I}{2.1\beta_J V_{eTH}}$$

$$V_{eTH} \frac{\beta_{dM} V_{dTH-} 2\beta_J V_{po}}{\beta_{dM} V_{dTH}} < V \le (1+r)V_{po} - rV_{eTH} + n \times V_{polyd}$$

Stage 3

$$V = (1+r)V_{PO} + \frac{V_{eTH} - V_{dTH}}{2} + n \times V_{polyd} - \sqrt{I}\left(\frac{1}{\sqrt{2\beta_{dM}}} + \frac{1+r}{\sqrt{\beta_J}}\right)$$

$$V > (1+r)V_{po} - rV_{eTH} + n \times V_{polyd}$$

3.10 Simulation and Experimental validation of the practical TBUs

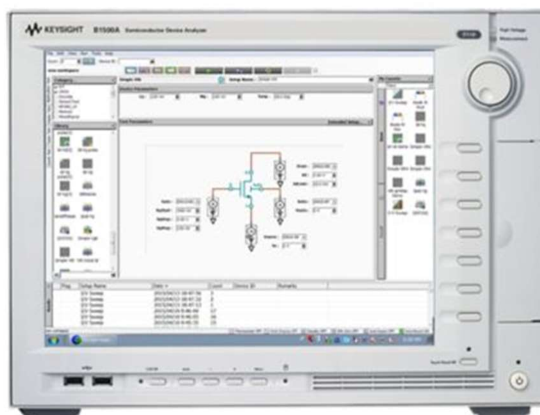
As shown in Figure 3.11, the TBU products are formed of the matrix of 5 voltage levels (250V, 400V, 500V, 650V and 800V) with 5 trip current levels (50mA, 100mA, 200mA, 300mA and 500mA) [2]. Three representative TBUs are chosen to be investigated. The first one is TBU-CA 250 050 with the lowest voltage 250V, the second one TBU-CA 650 100 with the middle voltage 650V and the third one TBU-CA 850 500 with the highest voltage 850V. All samples and components were provided by Bourns.

Starting with TBU-CA 250 050**,** each component of the TBU has been measured and its SPICE model has been built by curve-fitting technique. Finally, both simulation and experimental results have been compared with calculated results.

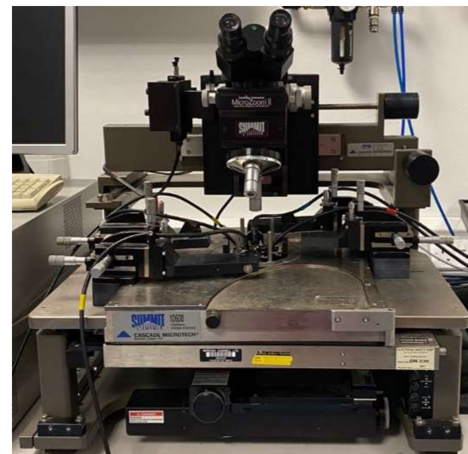
Figure 3.11 Photo of TBUs [2]

1) Component measurement and curve-fitted to SPICE model

The static characteristics of each component are measured by the B1500A Semiconductor Device Analyser and the Probe Station as shown in Figure 3.12(a) and (b) respectively.



(a)



(b)

Figure 3.12 (a) Device analyser B1500A (b) Probe Station

- **Diodes**

Figure 3.13 shows the measurement results against the simulated results. As can be seen, the diode SPICE model built by curve-fitting technique matches the measured component. The barrier potential of the diode is estimated at 0.62V@1µA.

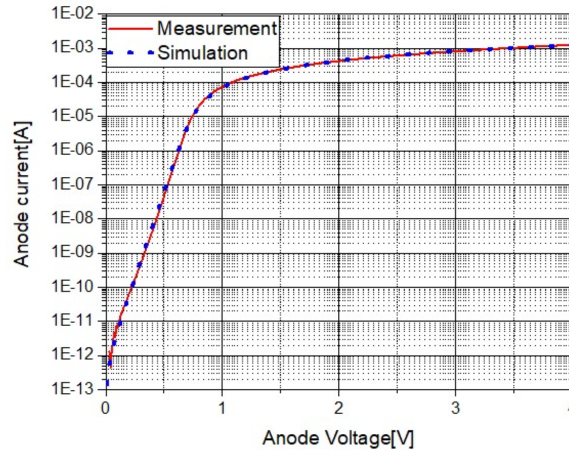
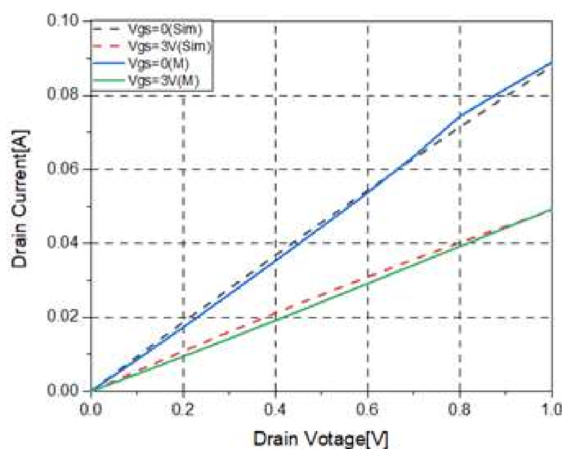


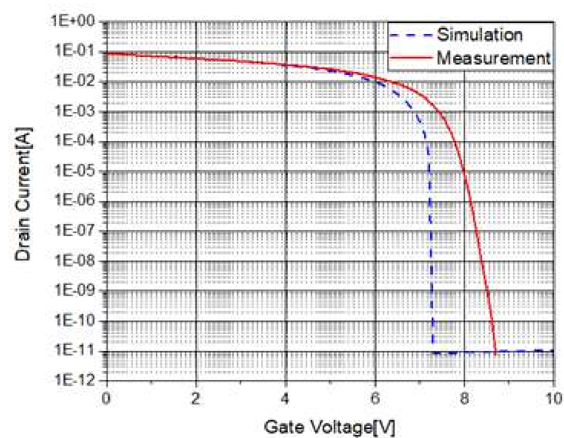
Figure 3.13 Forward characteristic of the diode

- **p-channel JFET**

The measured results of static characteristics of the p-JFET are shown in Figure 3.14. As can be observed, the simulated results of the output characteristics are well matched with the measured results as shown in Figure 3.14(a). Meanwhile, Figure 3.16(b) demonstrates the measured results against simulated results of the transfer characteristics. The noticeable discrepancy between them is due to the SPICE model without considering parasitic impedance of the real component. The pinch-off voltage V_{PO} of the p-JFET is obtained as 7.3V@100μA and the gain factor β_J is extracted as 0.0065.



(a)



(b)

Figure 3.14 (a) Output characteristics (b) Transfer characteristics of the pJFET

- **Enhancement mode MOSFET**

Figure 3.15 compares the measured results with simulated results of both output characteristics (Figure 3.15(a)) and transfer characteristics (Figure 3.15(b)) of the eMOS. The distinct disagreement between the measured and simulated result is due to the ideal SPICE model as opposed to the real component with parasitic elements. The threshold voltage V_{eTH} is obtained as 0.82V@100µA and the gain factor β_{eM} is extracted as 0.08.

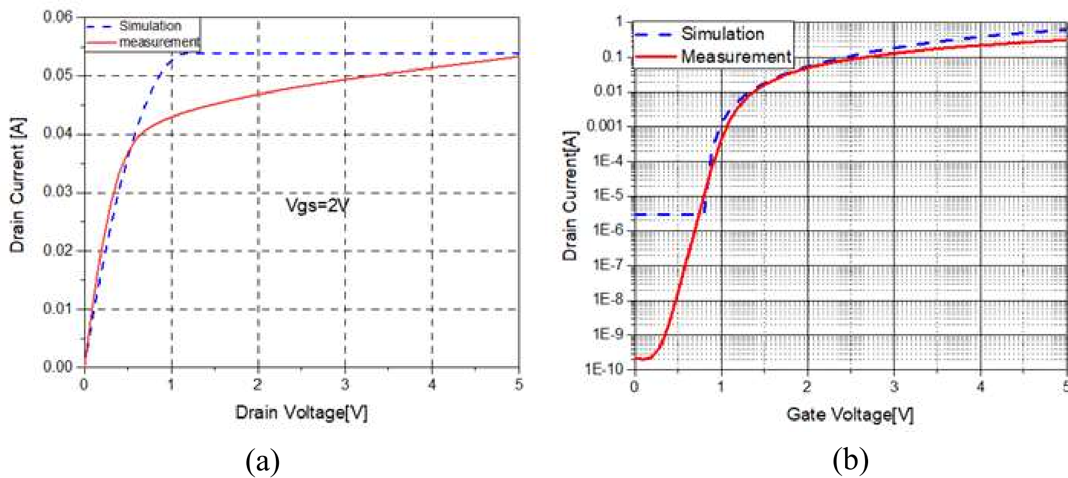


Figure 3.15(a) Output characteristics (b) Transfer characteristics of the eMOS

- **Depletion mode MOSFET**

The main parameters of the dMOS such as threshold voltage, on-resistance and gain factor are directly obtained from the specification provided by Bourns. The typical values of threshold voltage V_{dTH} -0.85V, on-resistance R_{on}=0.8Ω@Id=80mA and the gain factor β_{dM}=3.23 are chosen to build the SPICE model of dMOS. Figure 3.16 shows the simulated results of both output characteristics (Vg=0) and transfer characteristic of the dMOS.

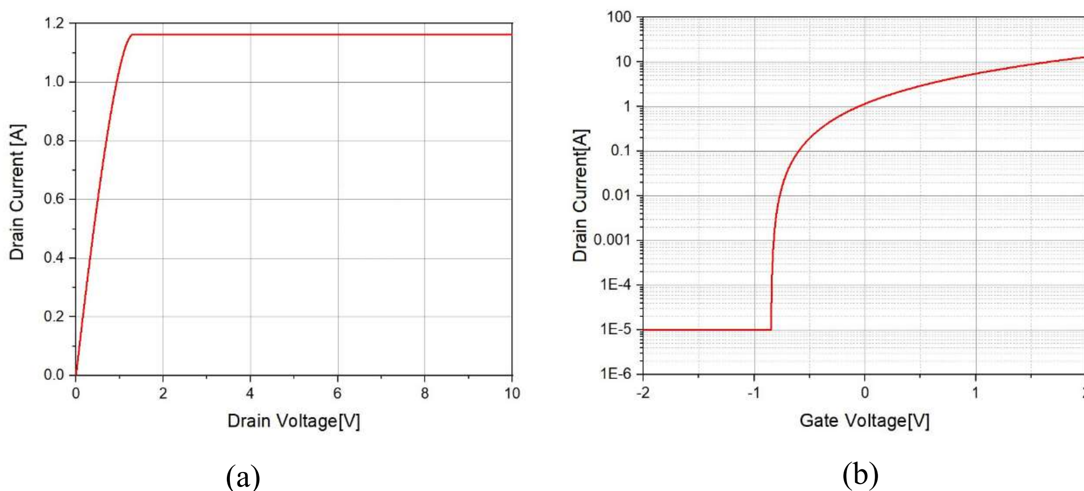


Figure 3.16 (a) Output characteristics (b) Transfer characteristics of the dMOS

- **Resistors R1-R7**

The resistance of each resistor has been measured and recorded in Table 3.3.

TBU-CA 250 50

The parameters of each component for TBU-CA 250 50 are consolidated in Table 3.3.

Table 3.3 Parameters of each component for TBU-CA 250 50

Components	Parameter	Value
Depletion mode MOSFET (dMOS)	Threshold voltage V_{dTH}	-0.85 V
	Gain factor β_{dM}	3.23
	On-resistance	0.8Ω
p-channel JFET (pJFET)	Pinch-off voltage V_{PO}	7.3 V
	Gain factor β_{J}	0.0065
Enhancement mode MOSFET (eMOS)	Threshold voltage V_{eTH}	0.82 V
	Gain factor β_{eM}	0.08
Diodes	Knee voltage V_{POLYD}	0.62V
Resistors	R1	2.2MΩ
	R3	3.6MΩ
	R4	50kΩ
	R6	10kΩ

2) Theoretical calculations

Substituting the parameters given in Table 3.3 into the equations for Scenario 1, the output characteristics for TBU-CA 250 50 in each stage are calculated as follows.

Stage 1: $\mathrm{V} = 11.3\mathrm{I}$ $\quad 0 \leq V < 0.85$

Stage 2: $\mathrm{I} = 0.082$ $\quad 0.85 \leq V < 4.6$

Stage 3: $\mathrm{V} = 15.6 - 143.9\mathrm{I}$ $\quad 4.6 \leq V < 15$

Stage 4: $\mathrm{V} = 16.3 - 20.4\sqrt{\mathrm{I}}$ $\quad 15 \leq V$

3) Comparison

The calculated results were compared with simulated and measured results as shown in Figure 3.17. As it is illustrated in the graph, a realistic matching has been demonstrated.

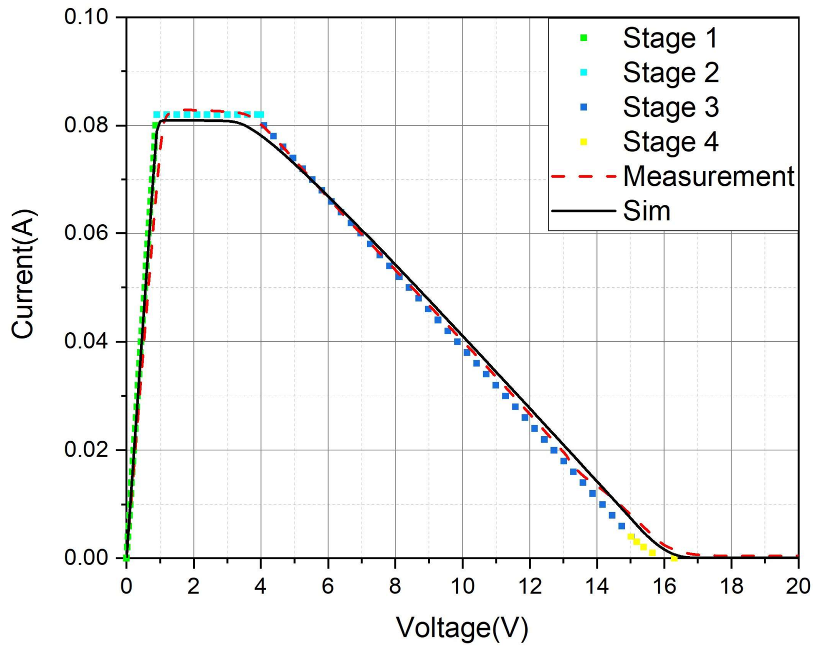


Figure 3.17 Comparison of calculation, simulation and measurement for TBU-CA 250 50

TBU-CA 650-100

Taking the same approach, TBU-CA 650 100 has been investigated. Table 3.4 list the parameters of each component for TBU-CA 650 100.

Table 3.4 Parameters of each component for TBU-CA 650 100

Components	**Parameter**	**Value**
Depletion mode MOSFET (dMOS)	Threshold voltage V_{dTH}	-0.85 V
	Gain factor β_{dM}	3.23
	On-resistance	3.2Ω
p-channel JFET (pJFET)	Pinch-off voltage V_{PO}	7.3 V
	Gain factor β_J	0.013
Enhancement mode MOSFET (eMOS)	Threshold voltage V_{eTH}	0.82 V
	Gain factor β_{eM}	0.08
Diodes	Knee voltage V_{POLYD}	0.62V
Resistors	R1/R2	2.2MΩ
	R3	3.6MΩ
	R4/R5	50kΩ
	R6/R7	10kΩ

1) Theoretical Calculations

Substituting the parameters given in Table 3.3 into the equations for Scenario 1, the output I-V expressions of TBU-CA 650 100 in each stage are obtained as:

Stage 1: $V = 11.6I$ $\quad 0 \leq V < 1.8$

Stage 2: $I_{trip} = 0.16A$ $\quad 1.8 \leq V < 5.5$

Stage 3: $V = 15.6 - 72I$ $\quad 5.5 \leq V < 15$

Stage 4: $V = 16.3 - 14.5\sqrt{I}$ $\quad 15 \leq V$

2) Comparison

The comparison of calculated, simulated and measured results for TBU-CA 650 100 is shown in Figure 3.18. As can be seen, a close match among them has been achieved.

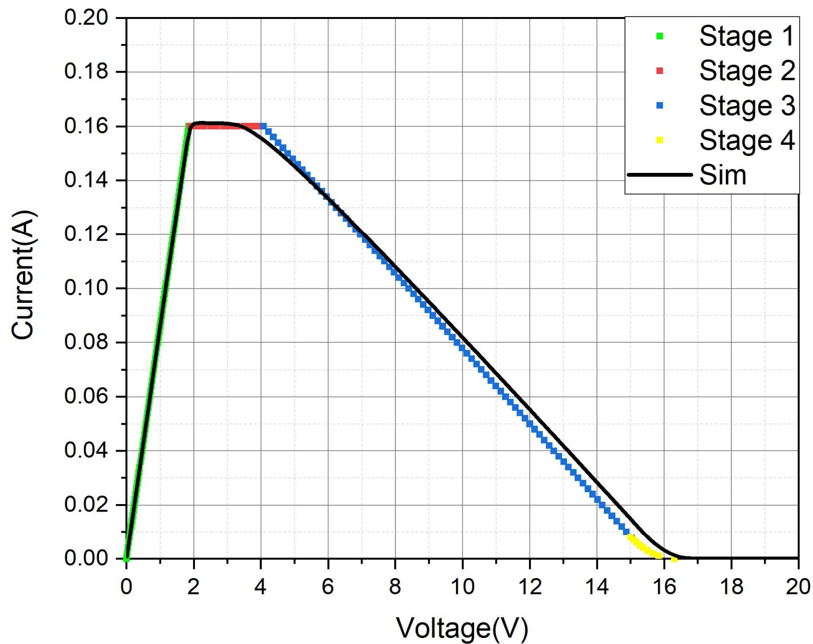


Figure 3.18 Comparison of calculation, simulation and measurement for TBU-CA 650 100

TBU-CA 850 500

This type of TBU has the highest voltage and current level. Table 3.5 list the parameters of each component for TBU-CA 850 500.

1)Calculation

With the parameters shown in Table 3.5, the I-V expressions for TBU-CA 850 500 in each stage are calculated as below:

Stage 1: $V = 9.2I$ $\quad 0 \leq V < 6$

Stage 2: $V = 15.6 - 14.4I$ $\quad 6 \leq V < 15$

Stage 3: $V = 16.3 - 6.7\sqrt{I}$ $15 \leq V$

Table 3.5 Summary of parameters of each component for TBU-CA 850 500

Components	Parameter	Value
Depletion mode MOSFET (dMOS)	Threshold voltage V_{dTH}	-0.85 V
	Gain factor β_{dM}	3.23
	On-resistance	4Ω
p-channel JFET (pJFET)	Pinch-off voltage V_{PO}	7.3 V
	Gain factor β_{J}	0.065
Enhancement mode MOSFET (eMOS)	Threshold voltage V_{eTH}	0.82 V
	Gain factor β_{eM}	0.08
Diodes	Knee voltage V_{POLYD}	0.62V
Resistors	R1/R2	2.2MΩ
	R3	3.6MΩ
	R4/R5	50kΩ
	R6/R7	10kΩ

2)Comparison

Figure 3.19 compares the measurement, calculation and simulation results for TBU-CA 850 500. The graph confirms the similarity among theoretically derived data, simulated results and measured results.

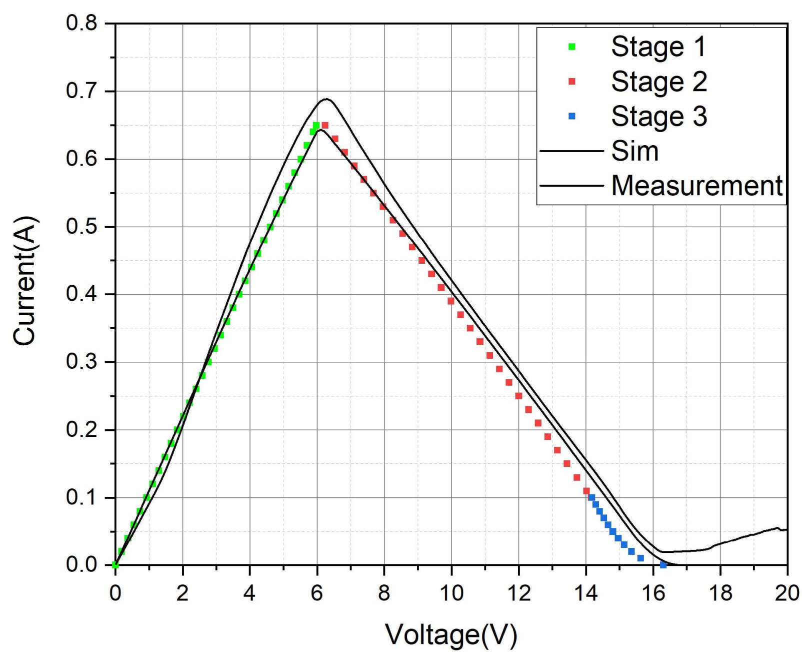


Figure 3.19 Comparison of calculation, simulation and measurement for TBU-CA 850 500

In the end, three typical types of practical TBUs have been investigated though theoretical analysis, simulation, and experiment. The results demonstrate a close matching among them, which confirms the correctness and accuracy of the theoretical analysis.

3.11 Conclusions

Without sensing and tripping circuity, the TBU features with ultrafast response speed and current limiting function. The operating processes of the basic TBU, the basic TBU with two added resistors, the basic TBU with an added enhancement Mode MOSFET, and the practical TBU have been analysed in details and their corresponding analytical expressions of output characteristic have been provided as a circuit design guideline for SSCB applications. Both circuit simulation and measurement have been conducted to verify the analysis results. Therefore, this chapter has laid a fundamental foundation for the development of the unique circuit used for the proposed SSCB in the later chapter.

3.12 References

[1] "United States Patent: 5742463." Online:http://patft.uspto.gov/

[2] "CO TBU-CA Series - TBU ® High-Speed Protectors," product leaflet, 2011 Online: https://www.bourns.com/products/circuit-protection/tbu-high-speed-protectors-hsps

[3] H. Shichman and D. A. Hodges, "Modeling and Simulation of Insulated-Gate Field-Effect Transistor Switching Circuits," *IEEE J. Solid-State Circuits*, vol. 3, no. 3, pp. 285–289, 1968, doi: 10.1109/JSSC.1968.1049902.

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Chapter 4 Power semiconductor devices for the proposed SSCB

4.1 Introduction

As discussed in Chapter 2, SSCBs can offer fast switching speed due to the superior properties of its power semiconductor devices. However, it suffers high conduction losses and limited short-circuit capability. Therefore, to design a SSCB, the choice of the semiconductor devices plays a key role for the success of SSCB performance.

In this chapter, first, the principal functions and technical specification for the proposed SSCB are defined. Then, the selection of commercial power semiconductor devices is conducted through the comparison of datasheet, simulation, and experimental results. Subsequently, the selected power device is characterized, and its original commercial SPICE model is modified for be closer to the performance of real component. Finally, thermal design is conducted and devices in parallel are investigated.

4.2 Device Requirement for the Proposed SSCB

4.2.1 A typical low voltage 400V DC distribution system

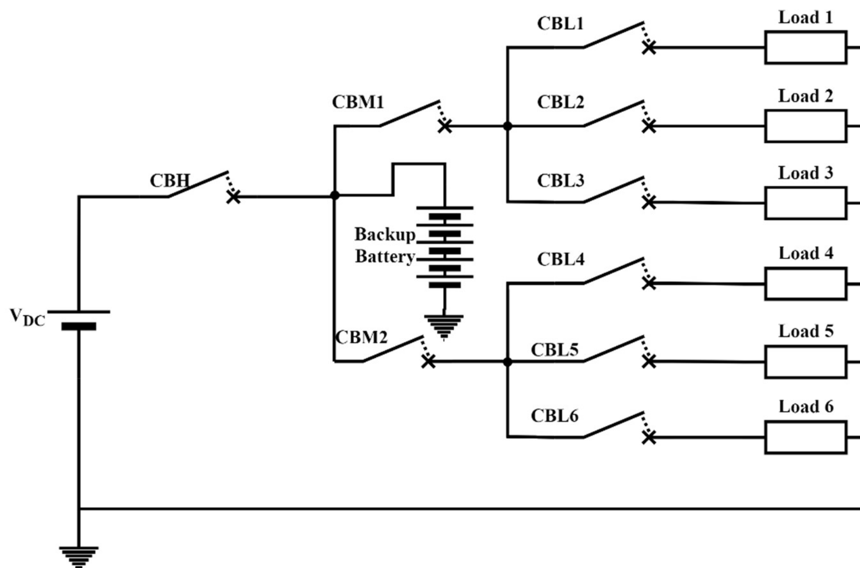


Figure 4.1 A typical 400V DC distribution system (adapt from [1])

A simple three-tiers DC distribution system is shown in Figure 4.1 [1]. A number of loads are supplied power by a common DC power source via three-tiers circuit breakers: Low level (CBL), Middle level (CBM) and High level (CBH). CBLs are used for protection of each load branch. CBMs act as the backup protection of CBLs. Once a CBL fails to protection the load, the CBM will stand up to provide the protection. Similarly, the CBH is the backup of CBMs. Meanwhile, the three-level of circuit breakers are required to coordinate for fault discrimination. Therefore, the protection setting of each level of circuit breaker should consider both maximum load current and prospective short-circuit current level at the point of the installation. This research focuses on the design of low and middle level circuit breakers.

4.2.2 Functionalities of the proposed SSCB

Figure 4.2 Functionalities of the proposed SSCB

Figure 4.2 shows the six principal functions of the proposed SSCB which are described as follows:

Short-circuit protection

This is the key function of a circuit breaker. Once a short-circuit fault has been detected, the SSCB should interrupt the fault current as fast as possible.

Overload protection

This function is used to protect both the SSCB itself and vulnerable components in the system from the thermal damage caused by overload current.

Over temperature protection

By monitoring the junction temperatures of the semiconductor devices in the SSCB, this function serves as a device condition monitoring and the backup of overload protection.

Normal switching on/off

The SSCB should be able to be switched on and off either locally or remotely.

Protection coordination

The SSCB should coordinate with other protective devices in the system to provide fault discrimination protection.

Immunity to inrush current

The SSCB should be able to avoid false trip, especially caused by the inrush current at the start-up of load connections.

4.2.3 International Standards for DC Circuit Breakers

Since the international standards for DC SSCBs have not yet been established standard, this design is to follow part of the international standard IEC EN 60898-3 for DC mechanical circuit-breakers[2]. Table 4.1 extracts the recommended values of main rated qualities from this standard.

Table 4.1 Recommended values from IEC EN 60898-3

Parameter	**Recommended value**
Rated operational voltage	200-400V
Rated direct current I_n	6-125A
Rated short-circuit capacity	1000-10000A
Range of instantaneous tripping	Type B: about 4 I_n up to and including 7I_n Type C: about 7 I_n up to and including 15 I_n

4.2.4 Technical specifications for the proposed SSCB

This research aims to develop an ultrafast either low-level or middle-level SSCB applied for a 400V DC system as shown in Figure 4.1. Following the recommended values from IEC EN 60898-3 as shown in Table 4.1, the technical specifications for the proposed SSCB are defined in Table 4.2.

As can be seen from the table, the rated current for the low level SSCB is as low as 10A. For one reason, this proposed SSCB intends to be placed in downstream branches with light loads such as below 40kW. For another reason, due to the limitation of the power equipment in the laboratory, a lab-scaled SSCB is reasonably built and tested. In addition, the response time is set below 55 μs. As discussed in Chapter 2, the response time for a SSCB mainly depends on the fault detection time, communication time and the energy dissipation time. Assuming the worst scenario with the highest system inductance L=100 μH, when a fault occurs, the time to reach the tripping current level can be estimated as 25 μs using the following equations:

$$\Delta t = L\frac{I_{trip}}{V_R} \tag{4.1}$$

After the device turns off, the fault current is commuted to the MOV or snubber circuit where the energy is dissipated. The energy dissipation time can be estimated of same of the fault detection time (25us). Therefore, the total response time is around 50 μs. Considering 10% margin, the response time 55 μs is an appropriate choice. Assuming the nominal DC system voltage is 400V, with the consideration of 10% tolerance, the rated voltage (maximum operating voltage) is set 440V. Finally, the system inductance mainly from cable inductance is set between 10 μH and 100 μH. According to Equation (1.9), (1.10) and (1.11), the value of cable inductance depends on cable area, cable length and the space between two parallel cables. As can been seen from Figure 1.9, with a paralleling cable with the size of AWG2 and 10cm spacing, its length would be in the range of 5m to 60m against the inductance value between 10 μH and 100 μH.

Table 4.2 Technical specifications for the proposed SSCB

Parameter	**Value**	
	Low-level SSCB	**Middle-level SSCB**
Rated voltage V_R	440V DC	440V DC
Rated current I_R	10A	20A
Response time T_{res}	<55µs	<110 µs
Trip current I_{trip}	>100A	>200A
Prospective fault current I_p	>1kA	>2kA
System inductance L	10-100µH	10-100µH
Maximum allowed Surge voltage Vs	<1000V	<1000V
Efficiency η	>99.7%	>99.7%
Device junction temperature	25°C - +175°C	

4.2.5 Calculation of maximum allowed on-Resistance for the proposed SSCB

Given the number of power devices in series N_s and number of power devices in parallel N_p, the efficiency η can be calculated as,

$$\eta = P_{out}/P_{in} = (P_{in} - P_{loss})/P_{in} \tag{4.1}$$

The input power P_{in} and conduction power loss P_{loss} can be figured out respectively as,

$$P_{in} = V_R I_R \tag{4.2}$$

$$P_{loss} = {I_R}^2 R_{on(total)(\mathrm{T})} \tag{4.3}$$

Assuming all the power devices are identical, the total resistance $R_{on(total)(T)}$ becomes,

$$R_{on(total)(\mathrm{T})} = N_s R_{DS(on)(T)}/N_p \tag{4.4}$$

According to Equation 4.1, 4.2, 4.3 and 4.4, the efficiency η is obtained as,

$$\eta = \left[V_R I_R - {I_R}^2 N_s \frac{R_{DS(on)(T)}}{N_p}\right] / (V_R I_R) \tag{4.5}$$

Rearranging Equation 4.5, the maximum allowed on-resistance is given by,

$$R_{DS(on)(T)} = \frac{N_p}{N_s} \frac{V_R}{I_R} (1 - \eta) \tag{4.6}$$

If a single power device is chosen, $N_p = N_s = 1$.
The maximum allowed on-resistance for the the low-level SSCB is obtained as,

$$R_{DS(on)(T)} \leq 132\text{m}\Omega \tag{4.7}$$

The maximum on-resistance for middle-level SSCB is,

$$R_{DS(on)(T)} \leq 66\text{m}\Omega \tag{4.8}$$

Alternatively, two devices in parallel are chosen for the middle-level SSCB, the maximum on-resistance of each single device becomes:

$$R_{DS(on)(T)} \leq 132\text{m}\Omega \tag{4.9}$$

4.3 Selection of Power Semiconductor Devices for the Proposed SSCB

There is a wide range of choices for power semiconductor device which meets the voltage/current requirement for low voltage SSCB applications. In the literature, Si MOSFET based SSCBs were reported in [3][4] and Si IGBTs for SSCBs in [5][6][7]. However, as concluded in Chapter 2, WBG devices are promising candidates for low-voltage SSCB applications due to their superior material properties over silicon. For this reason, SSCBs based on WBG devices, especially SiC devices, have been constantly reported in the literature [8][9][10].

4.3.1 Comparisons of wide bandgap materials over Silicon

WBG materials are defined as the material with a bandgap of 2.2eV or higher [11]. Among them, SiC and GaN are the most developed WBG semiconductors in the industry. Table 4.3 compares their intrinsic material properties and the Figures of Merit (FOM) with Silicon[12]. As it can be seen, both SiC and GaN have almost triple wider energy bandgap and one order higher critical electric breakdown field than Si. These features enable WBG-based devices to operate at higher temperature and higher voltage level. BFOM (Baliga's Figure of Merit), is inverse of conduction loss with specific die area. This FOM suggests that GaN vertical devices have the lowest theoretical specific on-resistance. However, the thermal conductivity of GaN is relatively lower than SiC, which implies less efficient heat transfer and a poor thermal performance.

Table 4.3 Comparison of SiC and GaN material properties over Si[12]

Properties	**Symbol**	**Silicon**	**GaN**	**4H-SiC**
Bandgap	Eg (eV)	1.12	3.39	3.26
Electric Breakdown Field	Ec (MV/cm)	0.23	3.3	2.2
Electron Mobility	μ_n (cm^2/V-sec)	1400	1500	950
Thermal conductivity	λ (W/cm-K)	1.5	1.3	3.8
Relative permittivity	ε_r	11.8	9.0	9.7
BFOM	$\varepsilon r \mu_n Ec^3$	1	2414	488

4.3.2 Commercial SiC power devices

The first SiC power Schottky diode in the voltage range of 300-600V was introduced in the market in 2001 by Infineon [13]. This event allowed further development of SiC based power devices for application with high efficiency and high-power requirements. Since then, SiC unipolar devices, such as JFETs and MOSFETs, have been developing towards maturity. For example, 1.2kV normally-on SiC JFET was commercialized in 2008 while 1.2kV SiC MOSFET was released on the market in 2011[14].

SiC JFETs

Normally-on SiC JFETs have been considered as the best fit for SSCB applications for a number of reasons. First, it has exhibited a very low specific on-resistance. For example, 1.2kV SiC JFETs have a typical specific on-resistance of 2-4 mΩ-cm^2, or 10 times lower than silicon MOSFETs[15]. Secondly, SiC JFETs demonstrates the exceptional robustness in short-circuit

mode. 1.2 kV SiC JFETs reported in [16] can withstand as long as 660 μs in the short-circuit test condition, corresponding to an energy of 60J/cm^2. Lastly, normally-on nature of SiC JFETs requires no active gate biased voltage to maintain SSCBs on. However, up to now, UnitedSiC is the only supplier to offer normally-on SiC JFETs in the market. Table 4.4 lists the commercial SiC JFET devices with the voltage ratings between1200V and 1700V.

Table 4.4 Commercial SiC JFET devices

Manufacturers	**Type**	**Voltage Ratings**	**Current Ratings**	**$R_{DS(on)}$@25°C**
UnitedSiC[17]	Normally-on	1200V	34-63A	35-66mΩ
	Normally-off	1200-1700V	8-120A	9-410 mΩ

SiC MOSFETs

SiC MOSFETs is another important type of SiC power devices for SSCB applications. Due to the potential high temperature operation and wide range of commercial availability from a number of leading semiconductor suppliers, they have been regularly reported for SSCB applications [18][19]. Table 4.5 lists the commercial SiC MOSFET devices with the voltage ratings between1200V and 1700V.

Table 4.5 Commercial SiC MOSFETs

Manufacturers	**Voltage Ratings**	**Current Ratings**	**$R_{DS(on)}$ @25 °C**
Infineon[20]	1200V	5-36A	60-350mΩ
STMicroelectronics[21]	1200V	12-100A	22-520 mΩ
	1700V	6-25A	65-1100 mΩ
Cree[22]	1200V	7-115A	16-350 mΩ
	1700V	5-72A	45-1000 mΩ
ROHM Semiconductor[23]	1700V	3.7-6A	750-1150 mΩ
	1200V	14-95A	22-280 mΩ

4.3.3 Commercial GaN devices

As mentioned before, theoretically, vertical GaN power devices have the lowest specific on-resistance. However, commercial vertical GaN devices are not yet available. At present, commercial GaN devices are all lateral heterojunction field-effect transistors (HFETs), also known as high electron mobility transistors (HEMTs). These devices are typically rated at 600–

650 V. Besides the low voltage rating level, two potential technical barriers also impede the lateral GaN devices for SSCB applications. One is the lack of avalanche capability. When exposed to high transient overvoltage, GaN HFETs would experience destructive and non-recoverable dielectric breakdown [24]. The other one is the much lower short-circuit capability compared to Si and SiC power devices [25]. Therefore, current commercial lateral GaN devices are generally less suitable for SSCB application. Table 4.6 lists the commercial GaN HEMT devices with the voltage ratings between 600V and 900V.

Table 4.6 Commercial GaN HEMTs

Manufacturers	**Voltage Ratings**	**Current Ratings**	**$R_{DS(on)}$@25 °C**
GaN Systems[26]	650 V	4-150A	10-450 mΩ
Panasonic[27]	600V	10-31A	56-270 mΩ
TI[28]	600V	6-12A	30-150 mΩ
Infineon[29]	600V	10-31A	70-190 mΩ
Transphorm[30]	650V	4-47A	35-480 mΩ
	900V	15-34A	50-170 mΩ

4.3.4 Comparison of four commercial power semiconductor devices

To meet the technical specifications defined in Table 4.2 for the proposed SSCB, four types of commercial power semiconductor device are selected for evaluation. Table 4.7 lists the four devices and the corresponding rated parameters extracted from their datasheet. As can be noted, except for Si MOSFET (650V), all other three devices are rated at 1200V since commercial power Si MOSFETs are all rated under 900V. Their rated current at 25°C is in the range of 60-80A. Additionally, they are all housed in TO247 package.

Table 4.7 Four candidates for the proposed SSCB

Device Type	**Manufacturer**	**Part No.**	**Rated Voltage**	**$R_{DS(on)max}$ @25°C**	**Rated Current @25 °C**	**Die Size**
Si MOSFET	IXYS	IXTH80N65X2[31]	650V	38mΩ	80A	0.80cm^2
Si IGBT	Infineon	IGW40T120[32]	1200V	$V_{CE(sat)}$=1.7V@40A	75A	0.41cm^2
SiC MOSFET	Cree	C3M0032120D[33]	1200V	43mΩ	63A	0.18cm^2
SiC JFET	USCi	UJ3N120035K3S[34]	1200V	45mΩ	63A	0.09cm^2

Comparison of device conduction losses

As mentioned in Chapter 2, the high conduction losses are one of the major drawbacks of SSCBs. Therefore, it is essential to select a power device with low conduction losses. Figure 4.3 compares the voltage drops against current at room temperature of the four devices. To fairly compare with other devices, two 650V MOSFET devices in series are assumed to meet the 1200V voltage rating. As it can be observed, at the low current level below 20A, the IGBT device has the highest voltage drops due to its inherent initial $V_{CE(SAT)}$ (about 0.7~1V). However, the IGBT outperforms other devices at the high current above 65A. Generally, the SiC JFET and SiC MOSFET share the lowest voltage drops at the current below 65A, almost half value of the Si MOSFET. Furthermore, taking account into the die size of each device, the specific on-resistances or equivalent value for the IGBT are calculated at current 20A as shown in Table 4.8.

It is concluded that the SiC JFET device has the lowest specific on-resistance at 3 mΩ.cm^2, less half of SiC MOSFET and one order lower than the counterparts' Si MOSFET and Si IGBT.

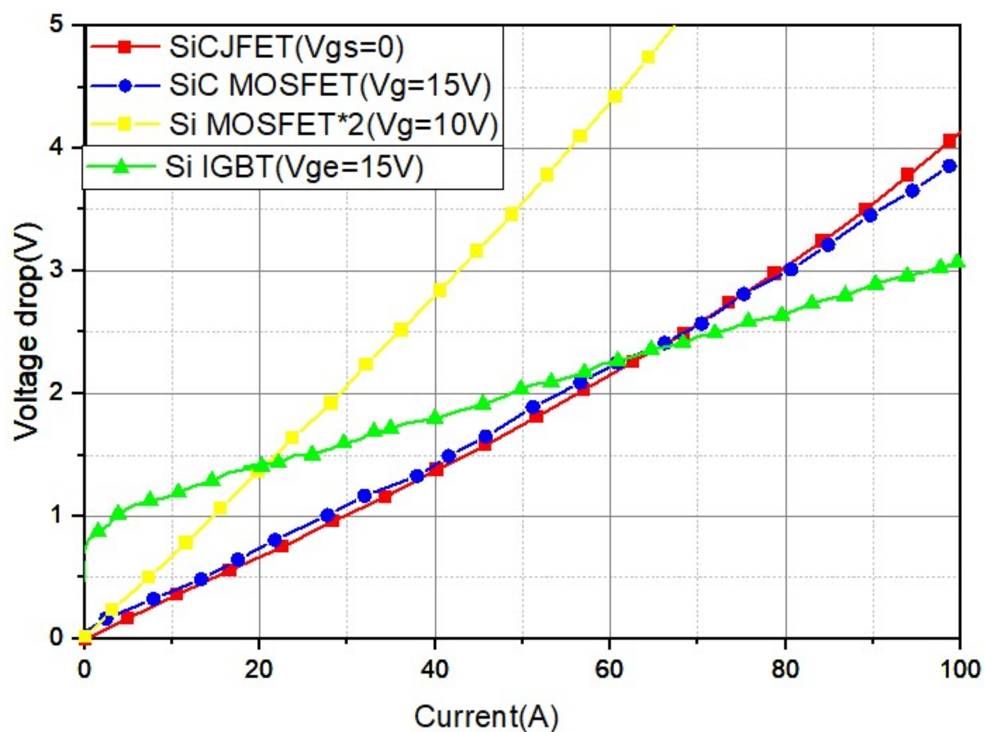


Figure 4.3 Comparison of voltage drops of four candidate devices

Table 4.8 Comparison of specific on-resistance

Type	Manufacturer	Part No.	Rated Voltage	Rated Current @25 °C	$R_{DS(on)}$ @25°C@20A	Die Size	Rds spec
Si MOSFET	IXYS	IXTH80N65X2	650V	80A	30*2mΩ	0.80cm^2	48 mΩ.cm^2
Si IGBT	Infineon	IGW40T120	1200V	75A	69 mΩ (equivalent)	0.41cm^2	28 mΩ.cm^2
SiC MOSFET	Cree	C3M0032120D	1200V	63A	37 mΩ	0.18cm^2	7 mΩ.cm^2
SiC JFET	USCi	UJ3N120035K3S	1200V	63A	34 mΩ	0.09cm^2	3 mΩ.cm^2

Comparison of device short-circuit capability

The short-circuit capability of a power semiconductor device is defined as the duration the device can survive under a short-circuit condition. This can be reflected by its critical energy which is the maximum thermal energy the device can dissipate before it fails. Power devices for SSCB applications are required to withstand the short-circuit current for a sufficiently long period before the SSCB can eventually isolate the fault[35]. Therefore, the short-circuit ruggedness of a power device for SSCB applications is a critical feature in order to assure the SSCB can safely interrupt the fault current without damaging.

A number of works in the literature have evaluated short-circuit capability of various types of power device. For example, [16] reported 1.2 kV SiC JFET can dissipate the energy as high as 60 J/cm^2 in the active area which conducts current when the device turns on. The work [36] demonstrates 1.2kV IGBT and 600V COOLMOS are able to dissipate the energy of 11.25J/cm^2 and 6.9J/cm^2 respectively. Also, 1.2kV SiC MOSFET was reported to have the critical energy around 13.5J/cm^2 [37]. However, the current trend to advance power semiconductor devices is to continue to improve the power density by reducing the chip size of the device, which is contradict to the short-circuit capability of the power devices.

For the fair comparisons, the chip size of each device is taken into account. The short-circuit capability of the four candidates has been evaluated by both simulation and experiment. Figure 4.4 shows the schematic circuit of the test bench for short-circuit capability test. It consists of a high power IGBT as a short-circuit switch in series with the Device Under Test (DUT). A large DC capacitor is added to maintain the DC output voltage level during the short-

circuit period. During the test, the DUT is kept in on-state by a constant biased gate voltage while the power IGBT controls the short-circuit duration. To determine short-circuit withstand time of the DUT, the test is repeated by gradually increasing the short-circuit time until the destructive failure of the DUT. Once the DUT fails, the short-circuit current is limited by the power IGBT. A photo of the test bench is shown in Figure 4.5.

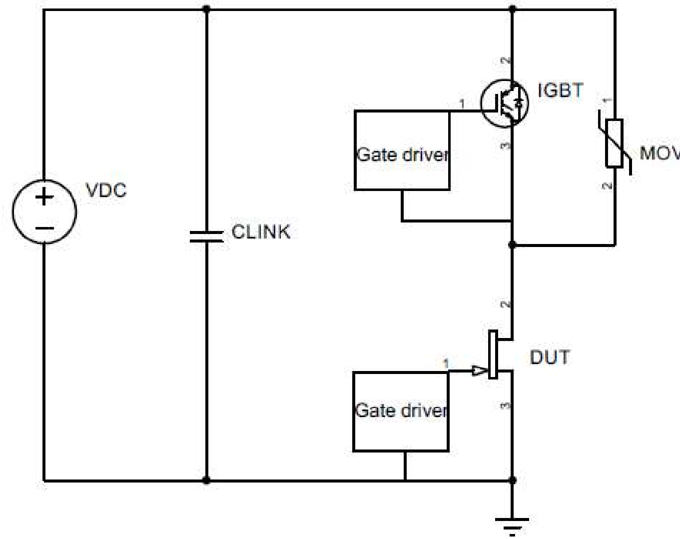


Figure 4.4 The schematic circuit for short-circuit capability test

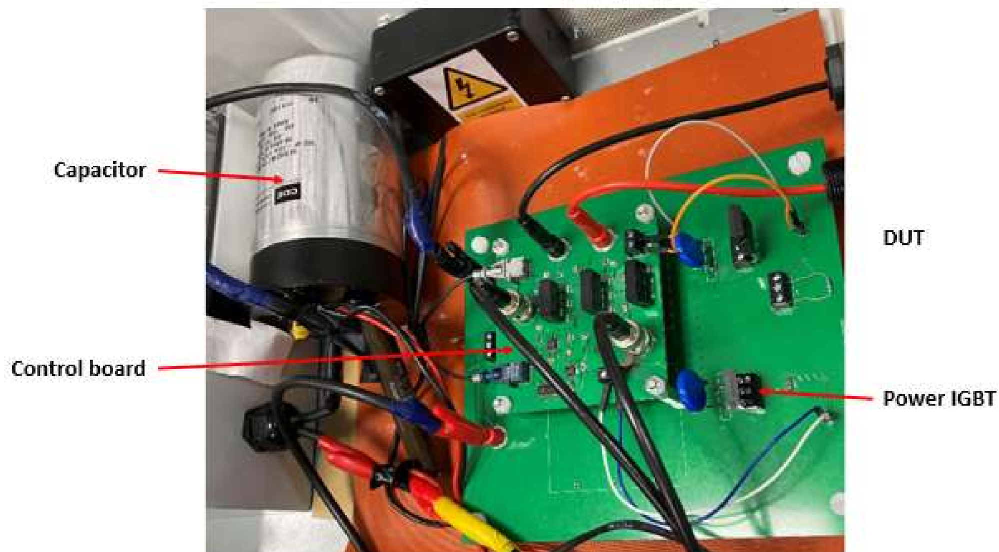
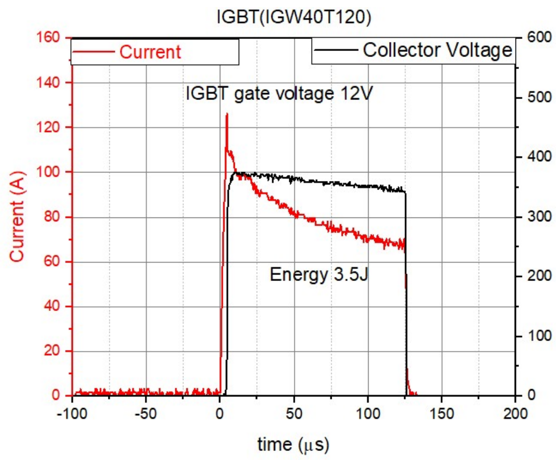


Figure 4.5 Photo of the test bench

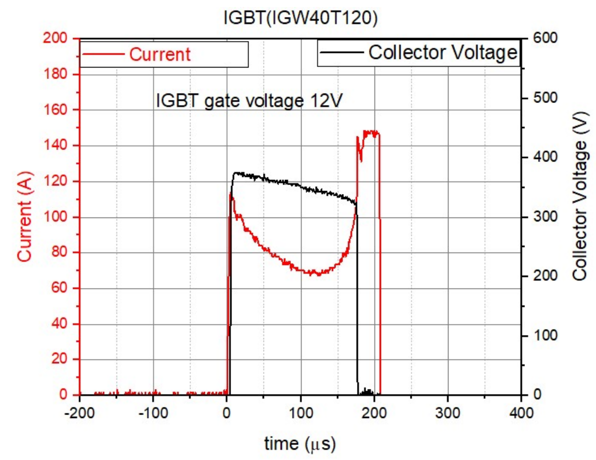
Both the simulated and experimental results of short-circuit capability for the Si IGBT are shown in Figure 4.6. As can be seen, the tested Si IGBT can withstand as long as 125μs under 100A current, corresponding to the critical energy of around 3.5J as shown in Figure 4.6(a). Figure 4.6(b) demonstrates the destructive test for the device. Meanwhile, the rising junction temperature of the Si IGBT is simulated under the short-circuit condition as shown in Figure 4.6(c). According to this results, Figure 4.6 (d) establishes how the junction temperature is associated with the dissipated energy. At the marked point of the critical energy 3.5J, the junction temperature of the Si IGBT during the test is predicted to reach 278°C. As reported in [37][38], under short-circuit conditions, the burst energy of the high current causes an extremely fast temperature rise in the die. However, the device will not fail immediately even if the rated junction temperature for instance 175°C is exceeded in a short-time span. In the end, the device will fail at a much higher temperature for example above 600°C than the rated junction temperature due to the device package elements such as the wire bonding or aluminium contact melted.

Similarly, Figure 4.7, 4.8 and 4.9 shows the results for the devices SiC MOSFET, Si MOSFET and SiC JFET respectively. Table 4.9 compares their critical energy and the corresponding energy density. It exhibits that all four devices have the same order of energy density, suggesting that the short-circuit capability might be restrained by the package rather than the device itself. Therefore, the high temperature potential of WBG devices has not been fully exploited due to the device package limitation.

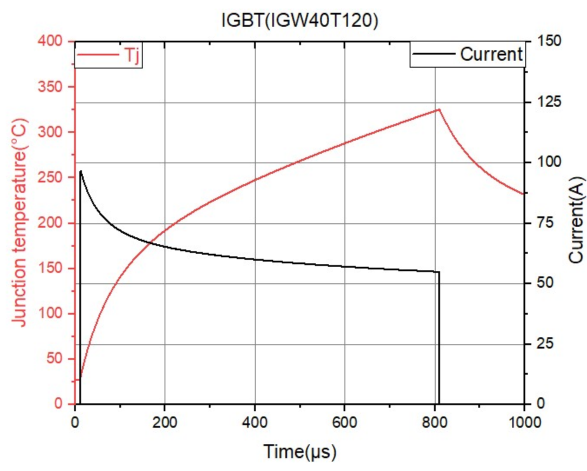
Furthermore, Figure 4.10 displays the saturation characteristic of the four devices under the different temperatures and gate biased voltages. As can be observed, with all the four devices, the saturation current at low gate voltage increases with the elevated temperature but decreases with the temperature at high gate voltage. However, for the Si MOSFET and SiC MOSFET, the drain currents slowly saturate at very high drain voltage under a high gate bias. In contrast, both the SiC JFET and Si IGBT can saturate at a much lower drain voltage under a high gate bias. This device feature is very important for short-circuit protection applications as it suggests the device can limit the current and survive at a longer short-circuit time under the same supply voltage. To conclude, both the SiC JFET and Si IGBT are more suitable for SSCB applications than the counterparts SiC MOSFET and Si MOSFET in terms of their saturation characteristics.



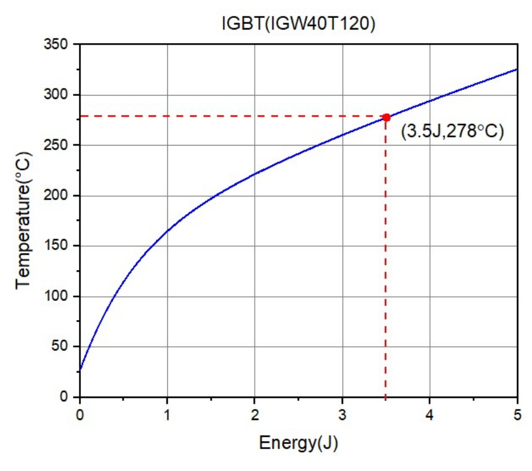
(a) Critical energy



(b) Destructive test

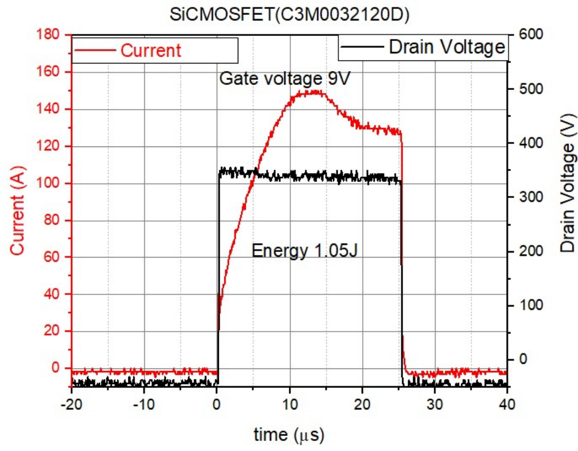


(c) Junction temperature rise

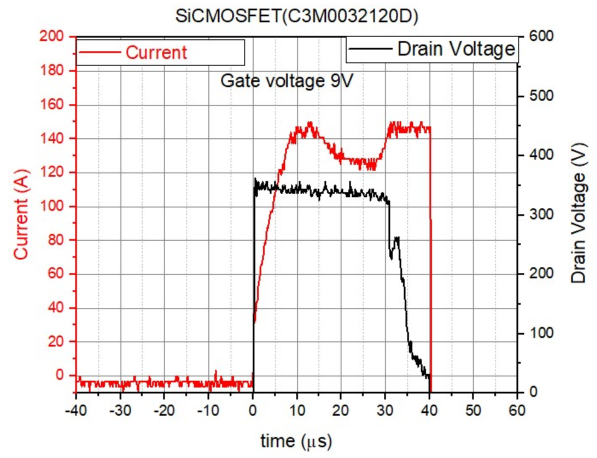


(d) Junction temperature vs. absorbed energy

Figure 4.6 Si IGBT Short-circuit capability



(a) Critical energy



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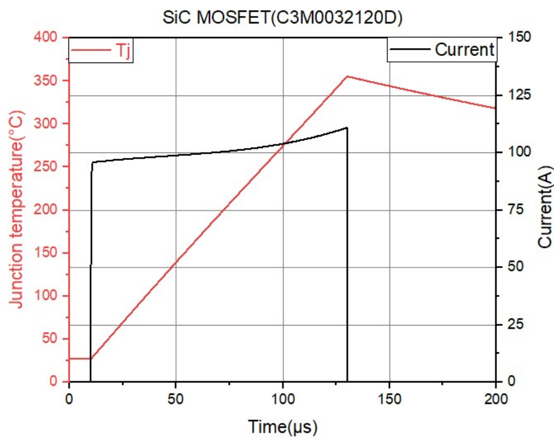
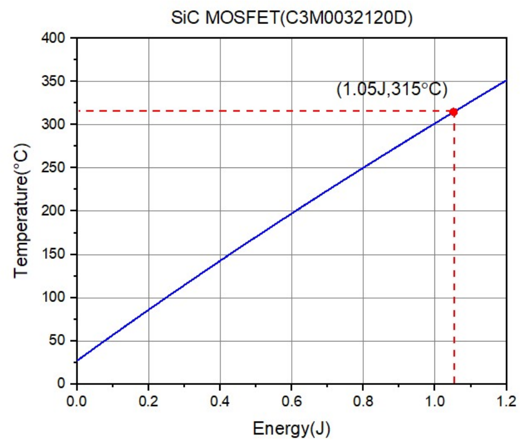
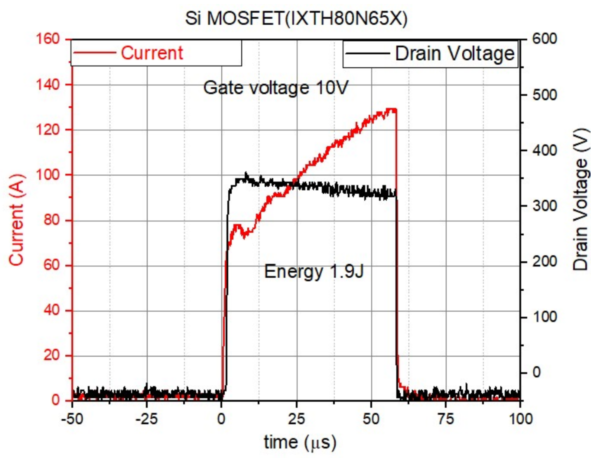


(c) Junction temperature rise

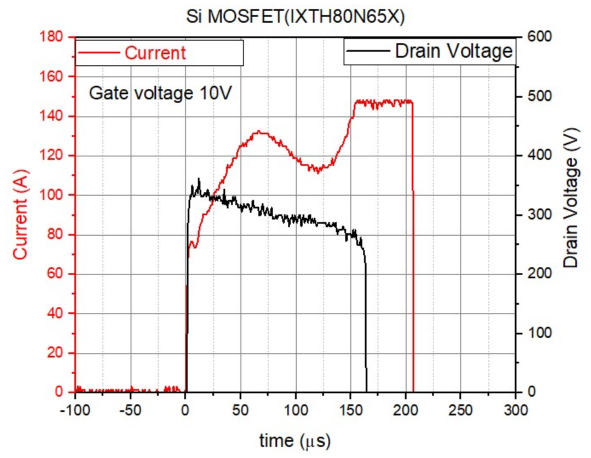


(d) Junction temperature vs. absorbed energy

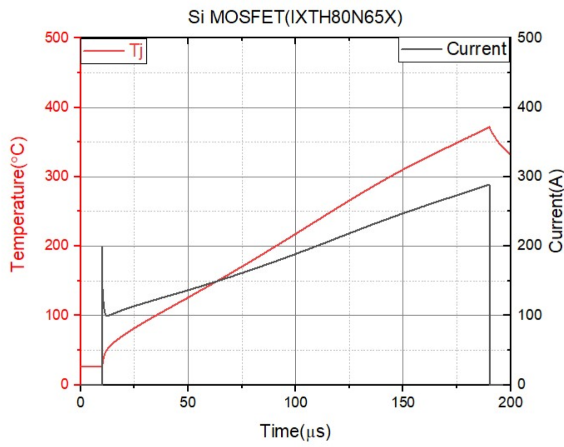
Figure 4.7 SiC MOSFET short-circuit capability



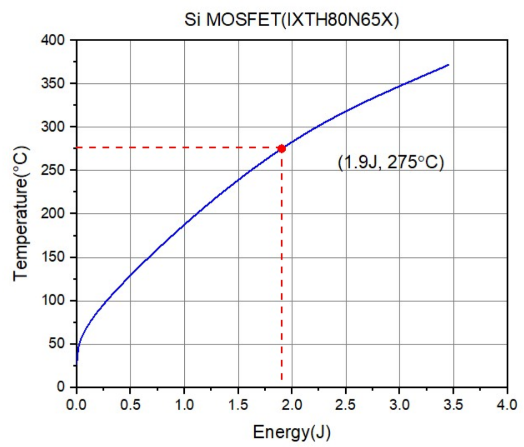
(a) Critical energy



(b) Destructive test

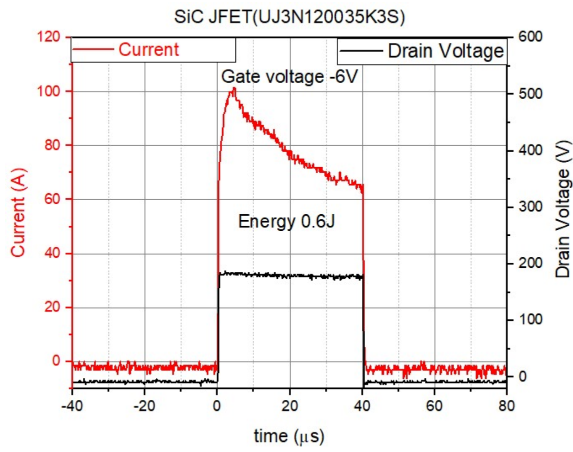


(c) Junction temperature rise

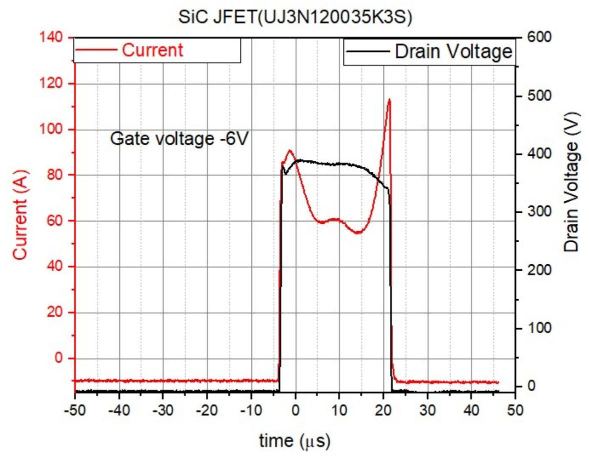


(d) Junction temperature vs. absorbed energy

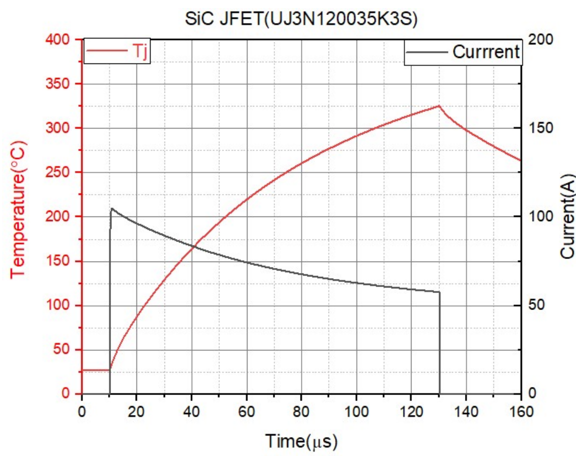
Figure 4.8 Si MOSFET short-circuit capability



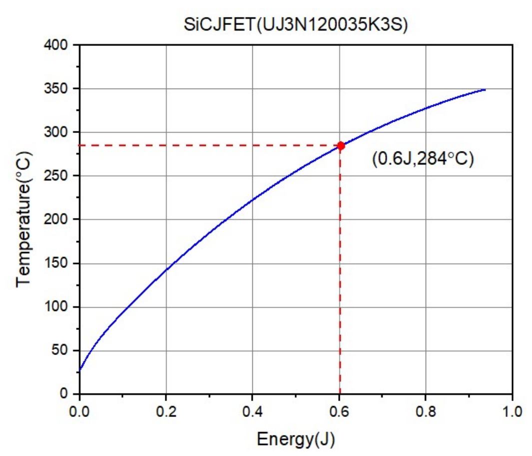
(a) Critical energy



(b) Destructive test



(c) Junction temperature rise



(d) Junction temperature vs. absorbed energy

Figure 4.9 SiC JFET short-circuit capability

Table 4.9 Comparison of short-circuit capability of four devices

Devices	**Manufac turer**	**Part No.**	**Rated Voltage**	**Rated Current @25 °C**	**Crit. energy Ec**	**Die Size**	**Crit energy density**
Si MOSFET	IXYS	IXTH80N 65X2	650V	80A	1.9J	0.80 cm^2	2.4 J/cm^2
Si IGBT	Infineon	IGW40T1 20	1200V	75A	3.5J	0.41cm^2	8.5 J/cm^2
SiC MOSFET	Cree	C3M0032 120D	1200V	63A	1.05J	0.18cm^2	5.8 J/cm^2
SiC JFET	USCi	UJ3N1200 35K3S	1200V	63A	0.6J	0.09 cm^2	6.7 J/cm^2

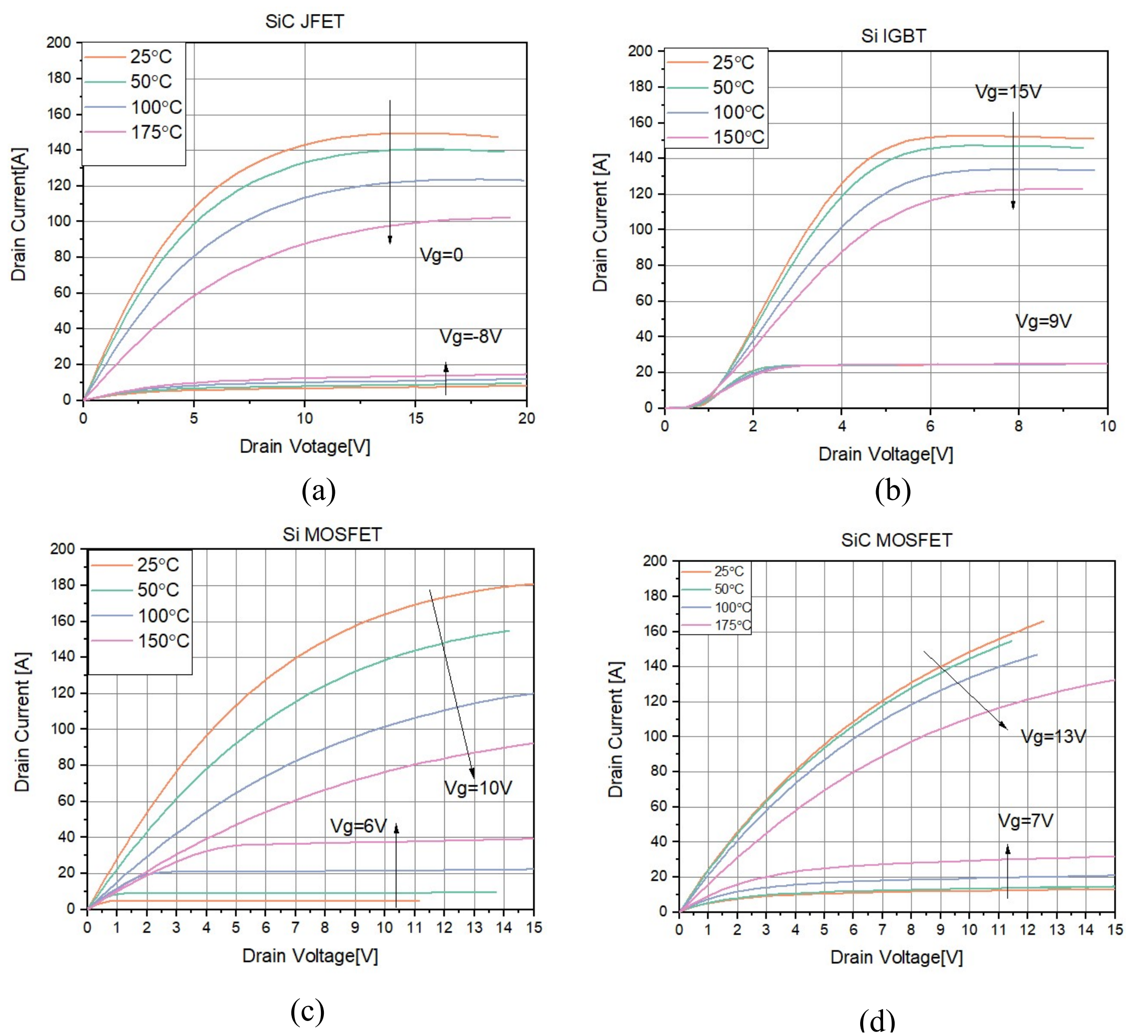


Figure 4.10 Saturation characteristics under various temperatures and gate voltages
(a) SiC JFET(b) Si IGBT (c) Si MOSFET (d) SiC MOSFET

To sum up, among the four evaluated devices, the SiC JFET device (UJ3N120035K3S) exhibits the lowest specific on-resistance under below 20A drain current while the Si IGBT (IGW40T120) shows the lowest voltage drops above 65A collect current. With the same package TO247, all four devices have demonstrated the same order of critical energy density, implying the device short-circuit capability limited by the package. However, the SiC JFET and Si IGBT saturate at a much lower drain voltage than the counterpart Si MOSFET and SiC MOSFET. In conclusion, the SiC JFET (UJ3N120035K3S) is chosen for the proposed SSCB due to its negative temperature coefficient, the specific on-resistance and saturation characteristics

4.4 Characterisation and Development of SPICE model of 1.2kV SiC JFET

Computer-aided circuit simulation is a great tool for optimising electronic circuit designs. However, to credit the simulation results, the accuracy of SPICE model should be as close as possible to the real component performance. The SPICE model of 1.2kV SiC JFET UJ3N120035K3S has been provided by the manufacturer USiC[39]. This model is trustworthy for the device operating in linear region but not suitable for device operation in the saturation region. In addition, this model does not reflect the temperature dynamics such as self-heating effect since the junction temperature is constant throughout the transient simulation.

4.4.1 Static characterization and model development of 1.2kV SiC JFET

Figure 4.11 compares the I-V curves of simulated results of the original SPICE model and the measured results with Tektronix 371B curve tracer at the room temperature. It appears there is a significant discrepancy between them. Hence, this model has to be modified to be closer to the measurement results. Figure 4.12 demonstrates simulated results of the modified model against the measured results at the room temperature. As it can be seen, a reasonable match has been achieved, especially the I-V curve at Vg=0, the most important curve for this application. The modified SPICE models are provided in Appendix B.

4.4.2 Dynamic characteristics and model development of 1.2kV SiC JFET

To accurately model the switching performance of semiconductor devices, the values of input and output capacitance should be as close as that of the real components. Figure 4.13 compares the C-V characteristic of simulated results of original SPICE model with that extracted from the datasheet[34]. It is obvious that both curves of input capacitance Ciss and output capacitance Coss have noticeable disagreement between them. As shown in Figure 4.14. both

curves of input and output capacitance of the modified model, is close matching to that from the datasheet. The simulation circuits for variable input and output capacitance of normally-on SiC JFET are provided in Appendix A.

4.4.3 Addition of junction temperature terminal Tj for SPICE model

To include the dynamic temperature feature, the model is modified by adding a fourth terminal Tj representing the junction temperature as shown in Figure 4.15(a). The voltage at the Tj reflects the dynamic junction temperature of the device. The simulated I-V output characteristics of the modified models under various junction temperatures setting Tj are shown in Figure 4.15(b).

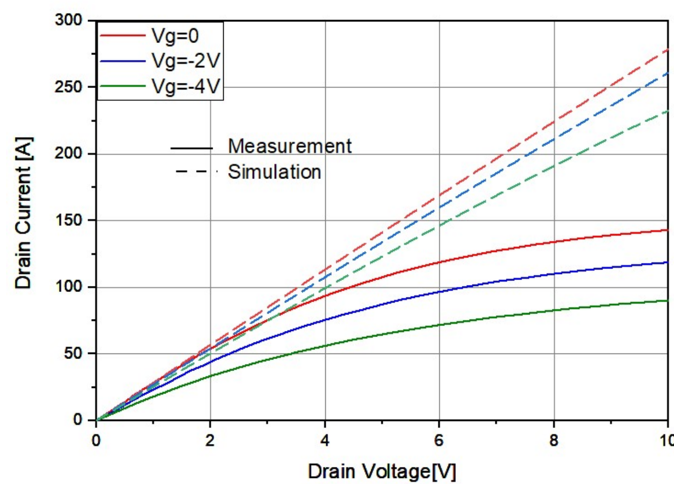


Figure 4.11 Measurement against Simulated output characteristics of original SPICE model at the room temperature

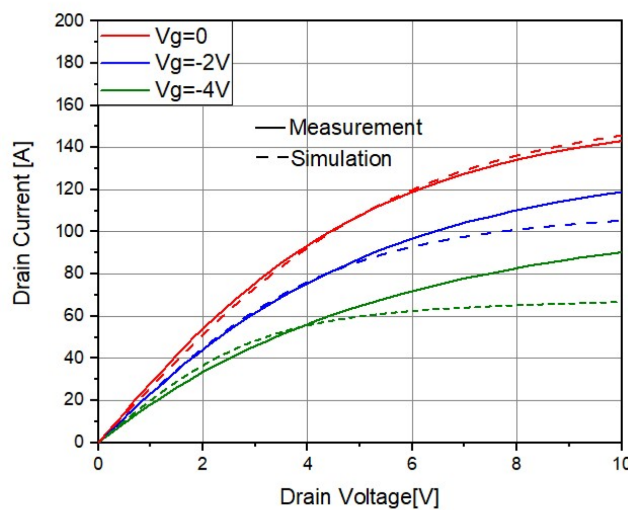


Figure 4.12 Measurement against Simulated output characteristics of modified SPICE model at the room temperature

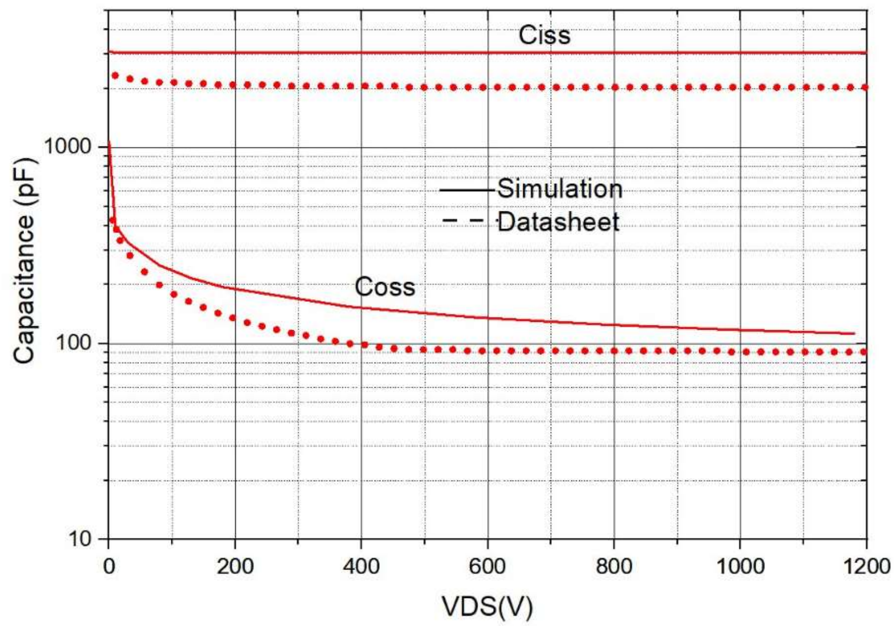


Figure 4.13 C-V curves extracted from datasheet against simulated results of original SPICE model

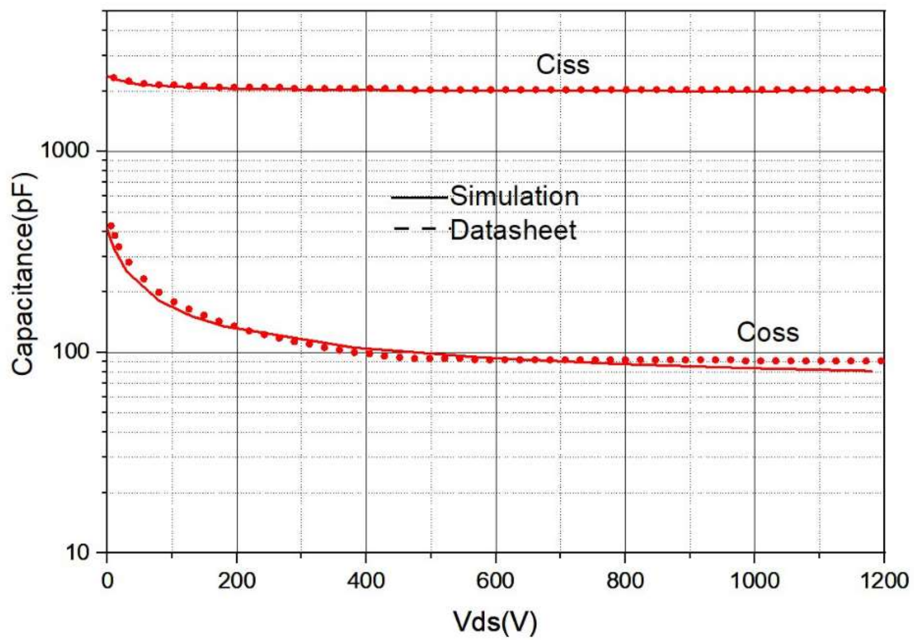


Figure 4.14 C-V curves extracted from datasheet against simulated results of the modified SPICE model

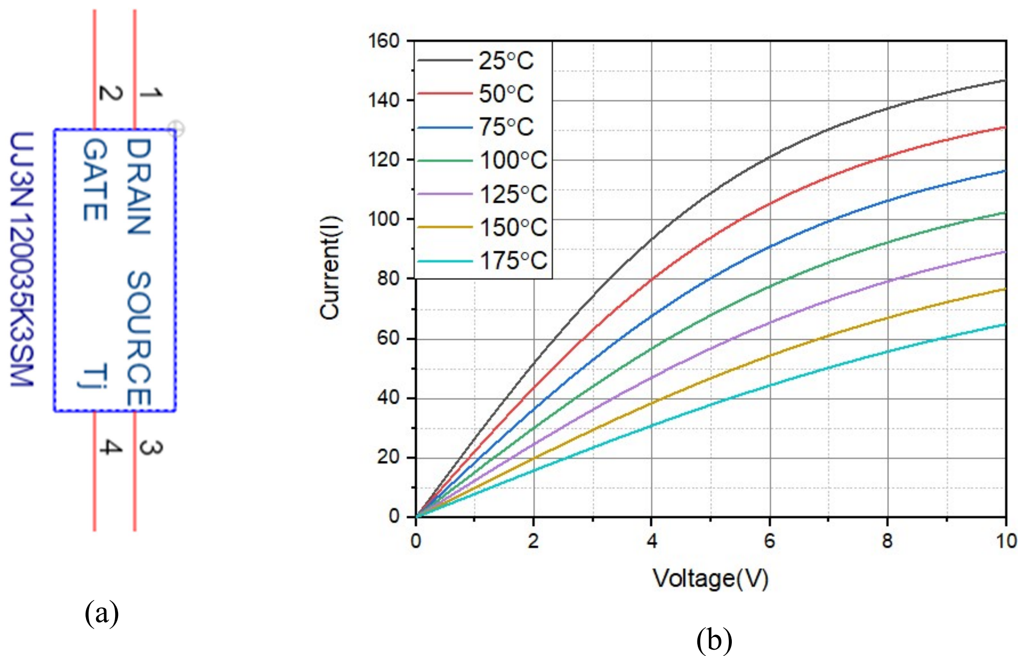


Figure 4.15(a) Symbol of the modified SPICE model (b) Simulated output characteristics of the modified SPICE model under various junction temperatures

4.5 Thermal Design

4.5.1 Introduction

Either the high conduction losses during normal operations or thermal energy burst during short-circuit operation would drive the power semiconductor devices beyond their thermal limits and result in the device failure. Therefore, it is vital to address the thermal concerns during both steady state and dynamic state of the SSCB operations. Since the thermal limit of a power semiconductor device is mainly determined by its maximum allowed junction temperature, the thermal design in this section focuses on the rising junction temperature though thermal analysis, simulations and experiment.

4.5.2 Thermal parameters

The heat transfer in a power module can be divided into three modes: conduction, convection, and radiation. For the convenience, an analogy between the electrical and thermal parameters is list in Table 4.10[40]. According to this analogy, a thermal network can be established and solved by the same means of electrical theories such as Ohm’s law.

Table 4.10 Analogy between electrical and thermal parameters[40]

Thermal Domain	Electrical Domain
Temperature Difference ΔT	Voltage V
Rate of heat flow Q	Current I
Thermal resistance R_{th}	Resistance R
Thermal capacitance C_{th}	Capacitance C
$\Delta T = P * R_{th}$	$V = I * R$
$P = C_{th} \frac{d\Delta T}{dt}$	$I = C \frac{dv}{dt}$

a) Thermal resistance

Thermal resistance is used to measure how difficult heat can flow through material or medium. Similar to the electrical resistance, it can be expressed as,

$$R_{th} = \frac{d}{\lambda * A} \tag{4.10}$$

Where d is material thickness, λ is heat conductivity and A is heat flow area.

b) Thermal capacitance

Thermal capacitance reflects the heat storage capacity of a component, defined by the change of heat with respect to the temperature. For a block of uniform material, it can be calculated as,

$$C_{th} = m * C_p \tag{4.11}$$

where m is the mass of the component and C_p is specific material heat capacity

4.5.3 Thermal modelling

A thermal design usually involves both numerical calculations and thermal modelling. In contrast with the time-consuming numerical calculations, the electro-thermal modelling provides a simple and effective way to evaluate the dynamic thermal behaviour of semiconductor devices. Either Foster or Cauer thermal networks are commonly used for semiconductor device thermal modelling.

a) Foster thermal model[40]

Figure 4.16(a) shows the Foster thermal network configured with a number of resistor(R)-capacitor(C) pairs in series. The current flowing through the network represents the power dissipation in the semiconductor device while the voltage reflects the junction temperature. The value of R and C can be obtained by curve fitted to the thermal impedance Z_{th} curve typically provided in the semiconductor device datasheet, using the following exponential equation,

$$Z_{th}(t) = \sum_{i=1}^{n} R_i(1 - e^{-\frac{t}{R_i C_i}}) \quad (4.12)$$

It is convenient to extract the values of both resistances and capacitances of the Foster network using curve-fitting method without knowing the physical structure of the semiconductor device. However, since this model do not reflect the physical properties, the values of R and C cannot be calculated from physical properties of each layer of a semiconductor device.

b) Cauer thermal network[40]

Cauer thermal model is shown in Figure 4.16(b). Similar to the Foster model, it is also built up by a chain of resistor-capacitor pairs. The difference between them is that the capacitors in the Cauer model are grounded. Furthermore, each pair of RC value in a Cauer model is associated with one layer of the physical device. Therefore, they can be directly calculated according to Equation 4.10 and 4.11 respectively. However, the geometrical size and material properties of the device are required to know for the calculations, which is not accessible in most cases.

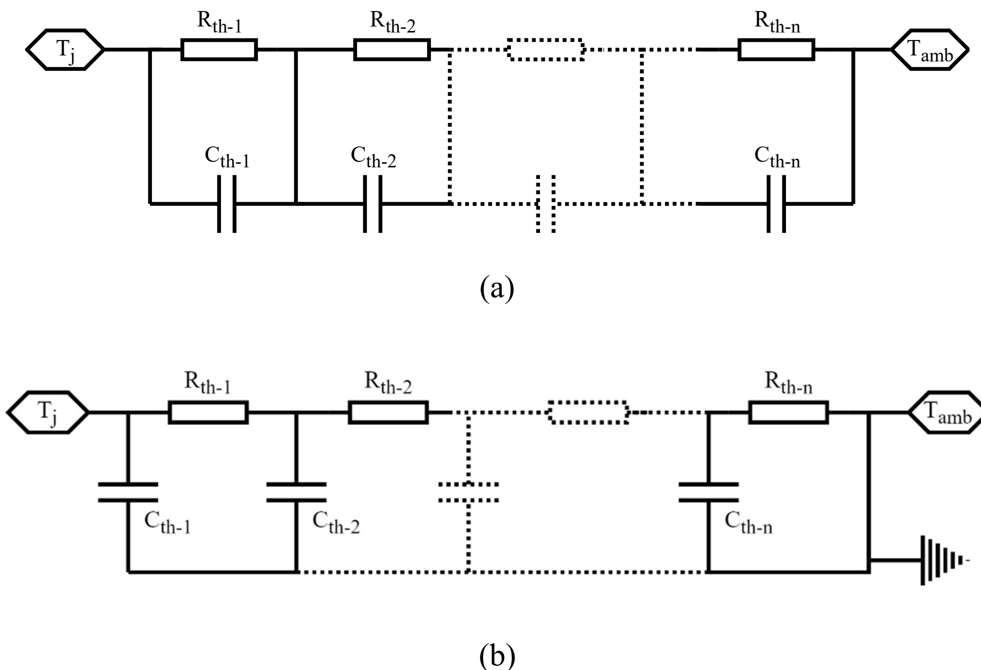


Figure 4.16 (a) Foster model (b) Cauer model

4.5.4 Junction temperature analysis during normal operating condition of a SSCB

During the normal operation condition, a SSCB stays on most time. Therefore, the power losses of the SSCB mainly come from its on-state conduction losses of semiconductor devices.
The conduction losses of a semiconductor devices can be calculated by the following equation,

$$P_{cond(T)} = I_d^2 R_{on(T)} \tag{4.13}$$

where $R_{on(T)}$ is temperature-dependent on-resistance of the semiconductor device and I_d is rated load current.
Figure 4.17 shows a schematic and basic structure of a typical semiconductor device and its equivalent thermal resistance network. As can be seen, it includes four parts: heatsink, thermal compound, device case and die. Assuming the ambient temperature Ta, the device junction temperature can be calculated by the following equation.

$$T_j = T_a + P_{cond(T)} * R_{th(j-a)} \tag{4.14}$$

where $R_{th(j-a)}$ is junction to ambient thermal resistance which is the summation of junction to case thermal resistance $R_{th(j-c)}$, case to thermal compound $R_{th(s-tc)}$, thermal compound to heat sink $R_{th(tc-s)}$ and heat sink to ambient environment $R_{th(s-a)}$.

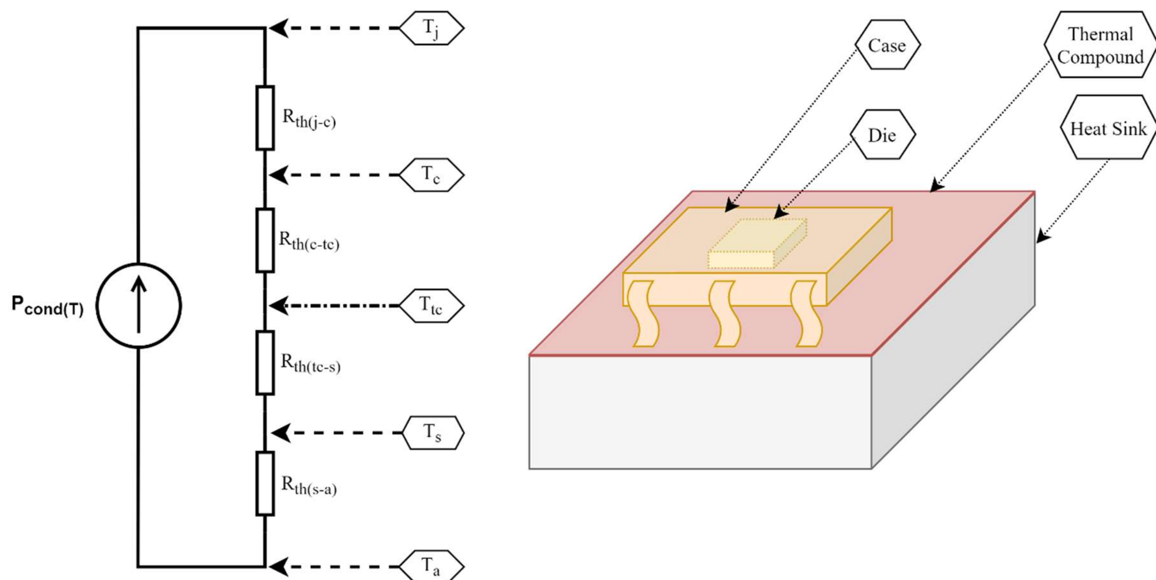


Figure 4.17 Thermal equivalent circuit and schematic diagram of a typical device

According to the datasheet of SiC JFET UJ3N120035K3S[34], maximum on-resistance at 25°C is $R_{on(25°C)} = 45m\Omega$ and normalized on-resistance vs temperature curve is also given. Therefore, $R_{on(T)}$ can be obtained by curve-fitted to a quadratic equation in the temperature range between 25˚C to 175˚C as shown in Figure 4.18.

$$R_{on(T)} = R_{on(25)} \times (0.906 + 2.27 \times 10^{-3}T + 2.79 \times 10^{-5}T^2) \quad (4.15)$$

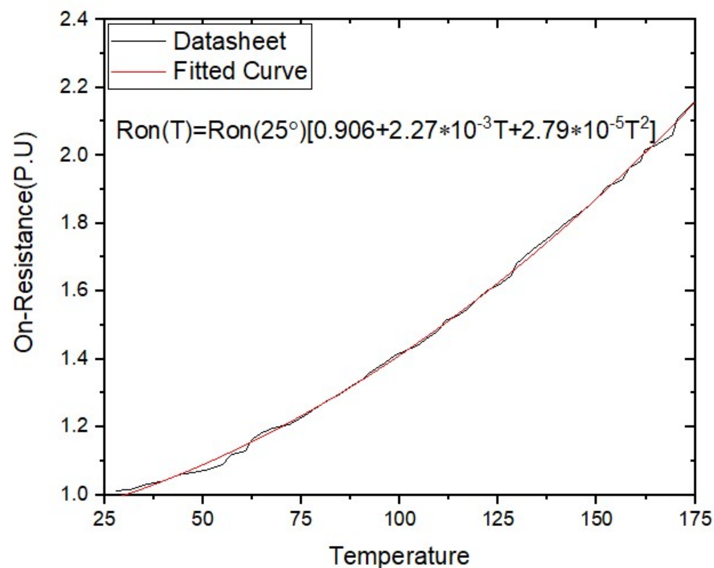


Figure 4.18 Curve fitted on-resistance against temperature

For the low level SSCB, rated load current Id=10A, inserting Equation 4.15 into Equation 4.13, the power conduction losses are obtained as,

$$P_{cond(T)} = 4.5 \times (0.906 + 2.27 \times 10^{-3}T + 2.79 \times 10^{-5}T^2) \quad (4.16)$$

Hence, at the maximum junction temperature $T_{j(max)}$=175°C, the conduction losses can be calculated as,

$$P_{cond(175)} = 9.7\text{W}.$$

Assuming the ambient temperature T_a=25°C, rearranging Equation 4.14, the maximum allowed junction to ambient thermal resistance $R_{th(j-a)}$ can be obtained as,

$$R_{th(j-a)} = 15.5°\text{C}/W$$

Also, junction to case thermal resistance $R_{th(j-c)}$is provided on the datasheet,

$$R_{th(j-c)} = 0.35°\text{C}/W$$

Assuming the interface material between device case and heatsink is silicon grease with 0.002 inches thick and 0.36 in^2 contact area, the thermal resistance of the interface material is estimated as [41],

$$R_{th(c-s)} = 1.13°C/W$$

Hence, the thermal resistance of selected heat sink should be less than,

$$R_{th(s-a)} = 15.5 - 0.35 - 1.13 = 14.0°C/W$$

For the middle level SSCB with a single device, Id=20A, by the same approach, the maximum allowed thermal resistance of selected heatsink can be calculated as,

$$R_{th(s-a)} = 2.4°C/W$$

Alternatively, two identical devices in parallel are mounted in a common heatsink. In this case, the maximum allowed thermal resistance of the heatsink is,

$$R_{th(s-a)} = 6.3°C/W$$

Since the value of thermal resistance of a heat sink given by manufacturers is an approximation, which neither takes into account non-uniform distribution of heat over the heatsink nor reflects the non-linearity of radiation and convection with respect to temperature rise, a heatsink with typical thermal resistance 1.4°C/W is conservatively selected as shown in Figure 4.19.

Assuming the ambient temperature Ta=25°C, with the selected heatsink, the maximum junction temperature at Id=10A and 20A can be calculated respectively as follows.

With Id=10A, Tj(max)=38.3°C

With Id=20A

Single device: $Tj_{(max)}$=97.4°C, two devices in parallel: $Tj_{(max)}$=72°C

Thus, the junction temperatures under normal operating condition are all well below the maximum allowed operating temperature 175°C.

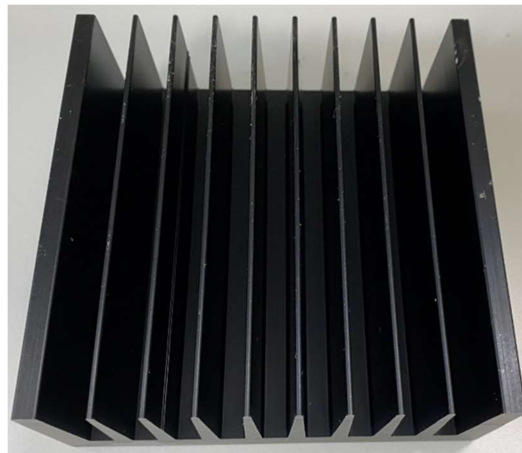
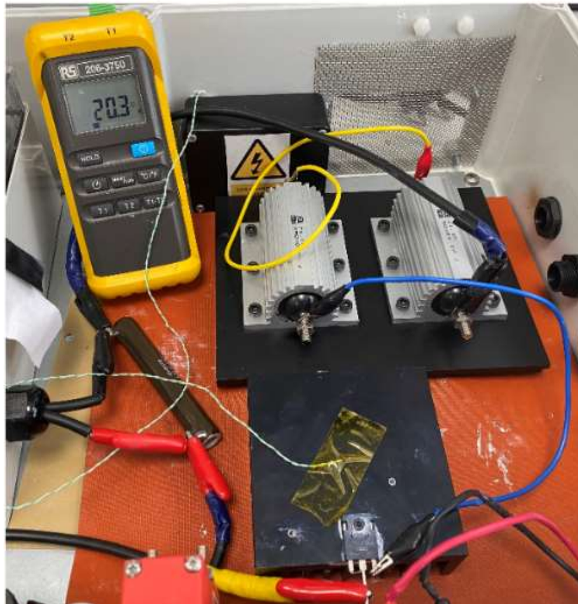


Figure 4.19 Heatsink with 1.4°C/W

Experiment validation

Figure 4.20 shows the pictures of temperature measurement setup with a single device (Figure 4.20(a)) and two devices in parallel (Figure 4.20(b)) mounted on the selected heatsink. The temperature of the heatsink is recorded every 30 minutes until reaching the steady value when injecting a 10 A constant current 10A into the single device and 20A into the two devices in parallel.

Figure 4.21 shows the measured temperatures over the time. As one can observe, after two hours, the temperatures stabilize at around 38.6°C with the single device and around 75.3°C with two devices in parallels respectively. As a result, the measured temperature of single device is slightly higher than the analytical value 38.3°C while the temperature of two devices in parallel is about three degrees higher than the analytical value 72°C. The difference between them is due to several factors such as negligence of thermal coupling between heatsinks of power resistors and the device, the discrepancies of the heatsink thermal resistance and device on-resistance between the calculation value and actual value. All in all, the experimental results have verified the correctness of the theoretical analysis.



(a) Single device

(b) Two devices in parallel

Figure 4.20 Hardware of temperature measurement

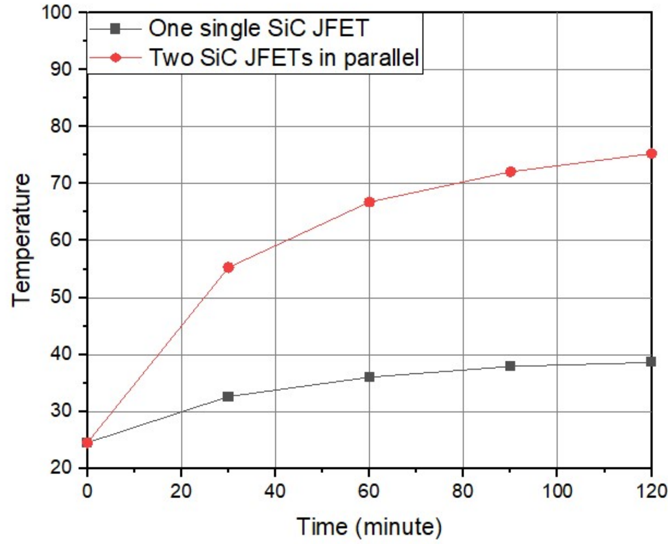


Figure 4.21 Measured temperature under rated current

4.5.5 Junction temperature analysis during short-circuit operation

Due to lack of data for the device physical size and internal structure, the Foster model will be used for modelling instead of Cauer model. As shown in Figure 4.22, the transient impedance curve obtained from the datasheet of SiC JFET UJ3N120035K3S[34] is curve fitted to the exponential equation given by Equation 4.12. Thus, the values of four pairs of RC parameters are obtained as list in Table 4.11. As demonstrated in Section 4.3.4, the SiC JFET UJ3N120035K3S can survive more than 10μs under 100A short-circuit and its junction temperature can reach as high as 284°C during the transient period.

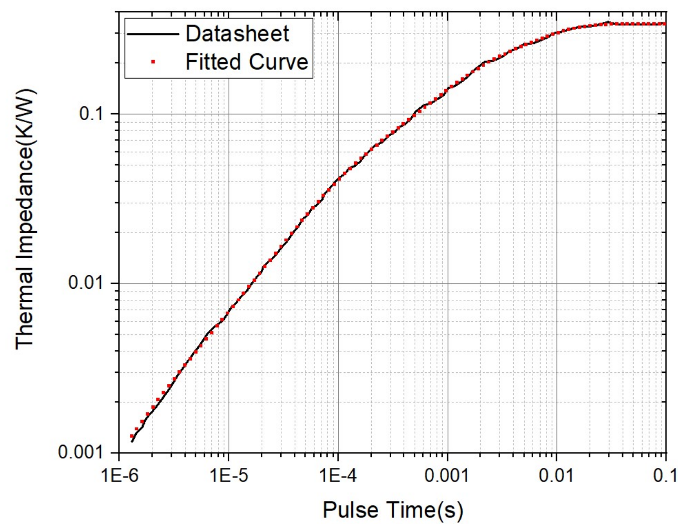


Figure 4.22 Curve fitted Foster network impedance

Table 4.11 Foster equivalent thermal circuit parameters

i	Ri(mK/W)	Ci(mJ/K)
1	1.4	2.0
2	36.7	2.4
3	119.6	8.4
4	183.7	35.8

4.6 SiC JFETs in Parallel

At present, the current rating of a single power SiC JFET in the market is still relatively low. Multiple SiC JFETs can be connected in parallel to increase the current capability. However, when several devices operate in parallel, there exists unbalanced currents between the devices due to their parameters mismatch. This issue might cause the thermal runaway resulting in the device failure. For the paralleling devices applied for SSCB applications, during the normal steady operation, the unbalanced currents are primarily caused by the mismatch of on-resistance among the devices. Whereas, during the short-circuit operation, the dynamic current sharing is essentially determined by the device variant threshold voltages [43]. This section will investigate the performance of SiC JFETS in parallel during both static and dynamic operations.

4.6.1 Analysis of static operation of normally-on SiC JFETs in parallel

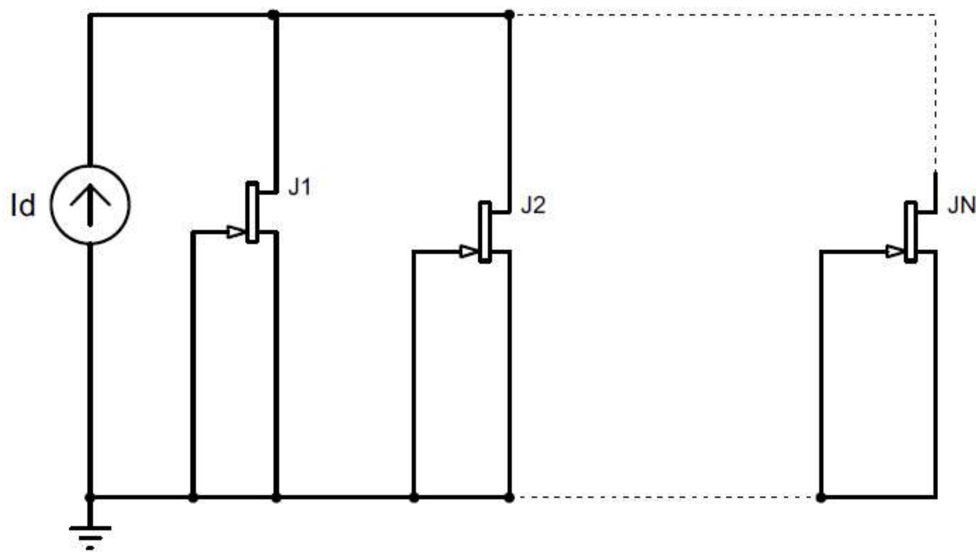


Figure 4.23 SiC JFETs in parallel

Figure 4.23 shows a N number of normally-on SiC JFETs in parallel. The total current Id flows through the devices and each individual device shares a proportion of the total current. The current shared by each device is inversely proportional to its on-resistance $R_{ds(on)(T)}$. The device with the lowest $R_{ds(on)(T)}$ shares the highest current and heat up most, and vice versa. Since the on-resistance of SiC JFETs has a positive temperature coefficient, over the time the current is going to be redistributed among the devices until a stable thermal equilibrium is eventually reached. Concerned on the performance of the devices in parallel, the priority is to assure each device operates below the maximum allowed junction temperature specified by the manufacturers rather than a good current sharing.

Considering the worst-case scenario of current unbalancing: The device J1 has the minimum on-resistance $R_{1(T)}$ and all others devices have the identical maximum on-resistance $R_{N(T)}$ [44].

Hence, the current flowing through each device is obtained,

Device J1
$$I_{d1(T)} = \frac{R_{N(T)}}{(N-1).R_{1(T)} + R_{N(T)}}.I_d \quad (4.17)$$

Other N-1 devices JN
$$I_{dN(T)} = \frac{R_{1(T)}}{(N-1).R_{1(T)} + R_{N(T)}}.I_d \quad (4.18)$$

In addition, all devices are assumed mounting on a common heatsink and having no thermal coupling between each other. Hence, the junction-to-ambient resistances $R_{th(j\text{-}a)}$ of all devices are identical. Furthermore, on-resistance is supposed to have a linear increase with the temperature between 25°C and 175°C. As a result, the on-resistance of each device at the temperature T can be figured out as,

Device J1
$$R_{1(T)} = R_{1(25)}[1 + K(T_a - 25 + I_{d1(T)}^2 R_{1(T)} R_{th(j-a)})] \quad (4.19)$$

Other N-1 device JN
$$R_{N(T)} = R_{N(25)}[1 + K(T_a - 25 + I_{dN(T)}^2 R_{N(T)} R_{th(j-a)})] \quad (4.20)$$

Where K is the per unit change of on- resistance per °C.

Solving Equation 4.19 for $R_{1(T)}$ and Equation 4.20 for $R_{N(T)}$,

Device J1
$$R_{1(T)} = \frac{R_{1(25)}(1 + K(T_a - 25))}{1 - K.R_{th(j-a)}R_{1(25)}I_{d1(T)}^2} \quad (4.21)$$

Other devices JN
$$R_{N(T)} = \frac{R_{N(25)}(1 + K(T_a - 25)}{1 - K.R_{th(j-a)}R_{N(25)}I_{dN(T)}^2} \quad (4.22)$$

According to Equation 4.17, 4.18, 4.21 and 4.22, the following express is obtained,

$$I_{d1(T)}.\frac{R_{1(25)}}{1 - K.R_{th(j-a)}R_{1(25)}I_{d1(T)}^2} = I_{dN(T)}.\frac{R_{N(25)}}{1 - K.R_{th(j-a)}R_{N(25)}I_{dN(T)}^2} \quad (4.23)$$

Rewriting Equation 4.23 as,

$$\frac{K.N.R_{1(25)}R_{N(25)}R_{th(j-a)}}{(N-1)^2}I_{d1}^3 - \frac{K.(N+1).R_{1(25)}R_{N(25)}R_{th(j-a)}I_d}{(N-1)^2}I_{d1}^2 - [\frac{R_{N(25)}}{N-1} + \left(R_{1(25)} - \frac{K.R_{1(25)}R_{N(25)}R_{th(j-a)}I_d^2}{(N-1)^2}\right)\Big].I_{d1} + \frac{R_{N(25)}I_d}{N-1} = 0 \quad (4.24)$$

Solving Equation 4.24 for I_{d1}, the junction temperature Tj at the final stable thermal equilibrium can be figured out accordingly.

Take an example of two SiC JFETs (UJ3N120035K3S) in parallel: One device with the maximum on-resistance 45mΩ at 25°C and the other one with the minimum on-resistance. The minimum value is not given on the datasheet but can be simply estimated as,

$$R_{ds(on)(min)} = R_{ds(on)(max)} - 2\left(R_{ds(on)(max)} - R_{ds(on)(typ)}\right) = 45 - 2(45 - 35) = 25m\Omega$$

Based on the curve of normalized on-resistance vs. temperature on the datasheet, the value K is obtained as,

$$K = 0.008$$

Assuming, $R_{th(j-a)} = 10\ k/W$, $I_d = 20A$, substituting these parameters into Equation 4.24, it becomes,

$$180I_{d1}^3 - 5400I_{d1}^2 - 34000I_{d1} + 900000 = 0$$

Solving this cubicle equation, the current flowing the device J1 is obtained as,

$$I_{d1}=12.3A$$

Assuming the ambient temperature Ta=25°C, the on-resistance of $R_{1(T)}$ can be calculated with Equation 4.21 as,

$$R_{1(T)} = 35.8\text{m}\Omega$$

Finally, the device J1 junction temperature T_{1j} is calculated by Equation 4.15 as,

$$T_{1j} = 79°C$$

Simulation validation

The value of all the parameters for simulation is list in Table 4.12, which is identical with the calculated value.

Table 4.12 Parameters for simulation

Parameter	**Value**
On-resistance at 25°C	J1:25mΩ J2:45mΩ
Total current Id	20A
Junction to ambient thermal resistance Rth(j-a)	10 k/W
Per unit change of on- resistance per °C K	0.008
Ambient temperature Ta	25°C

Figure 4.24 shows the simulated current sharing between the two paralleling SiC JFETs while Figure 4.25 illustrates the junction temperature against the rated current. As it can be seen, the device J1(red line) with lower on-resistance shares more current than J2 and its corresponding junction temperature is higher than J2. Meanwhile, as marked on the graph, when Id=20A, the Id1=12.3A and Tj1=79°C, exactly matches the analytical results. Furthermore, Figure 4.26 demonstrates how the junction temperature Tj1 is affected by the junction to ambient thermal resistance Rth(j-a). As marked on the graph, when Rth(j-a) reaches 19°C/W, the junction temperature Tj1 reaches its limit 175°C under Id=20A. This suggests the thermal resistance of selected heatsink must be less than 22.5 °C/W for sharing total load current 20A.

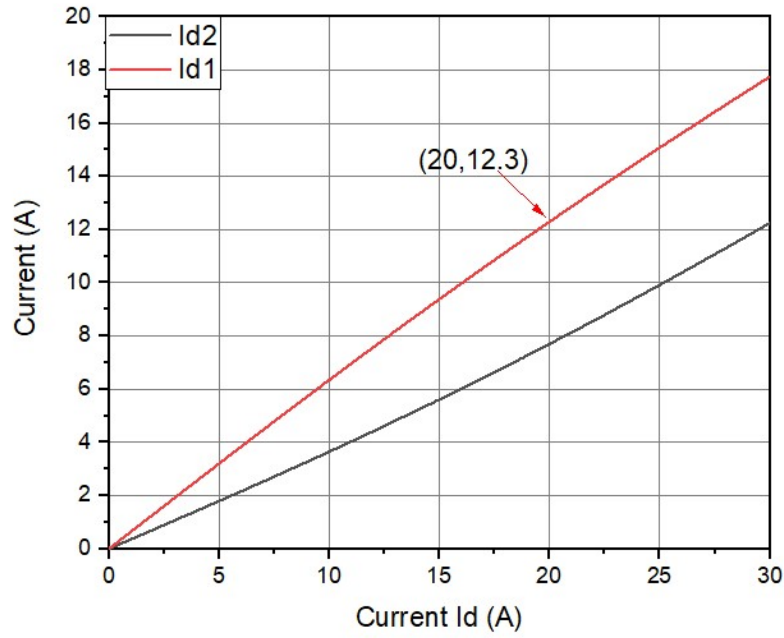


Figure 4.24 Current sharing between two SiC JFETs in parallel

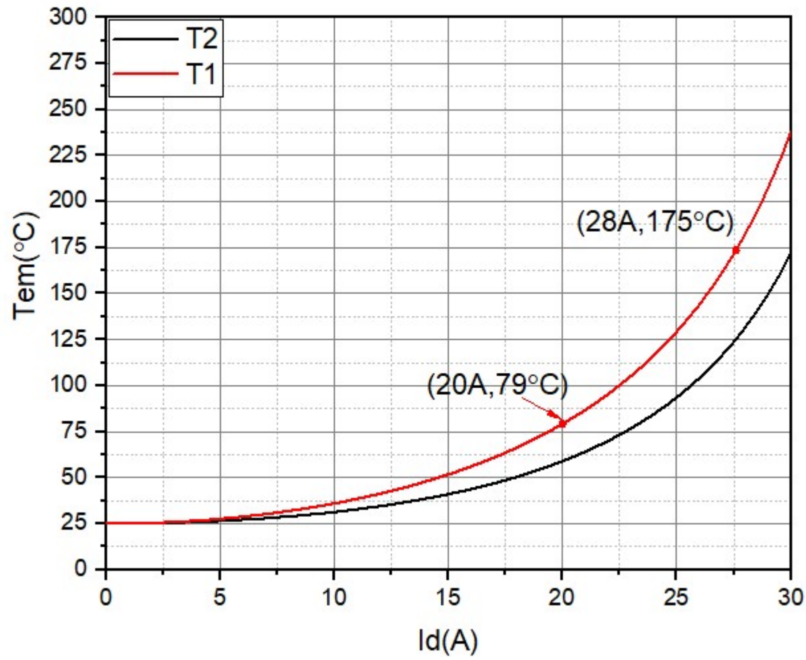


Figure 4.25 Junction temperature vs. current

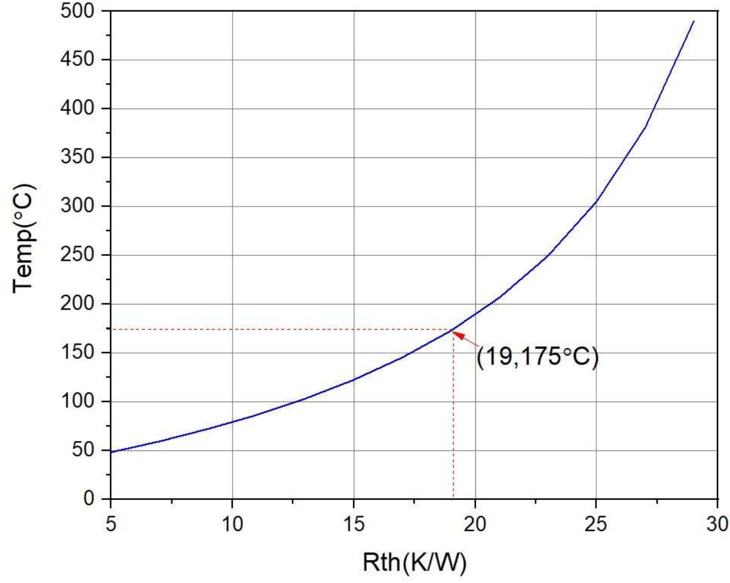


Figure 4.26 Impact of thermal resistance on the junction temperature

4.6.2 Dynamic current unbalancing

When a group of SiC JFETs in parallel operate in the saturation region, their variant gate threshold voltages have a significant impact on the dynamic current sharing and short-circuit capability as a whole. Initially, the device with lowest threshold voltage takes a highest current and heats up most. Over the time, due to self-heating effect, the current flowing through the device with lowest threshold voltage decreases fastest. In addition, as indicated from the device datasheet, the threshold voltage of an individual SiC JFET is almost invariable with the temperature.

Similarly, consider the worst-case scenario of current unbalancing: Device J1 with minimum threshold voltage V_{T1} and other N-1 devices are identical with the maximum threshold voltage V_{T2} as shown in Figure 4.27. Hence,

$$I_d = I_{d1} + (N-1)I_{d2} \tag{4.25}$$

When a JFET operates in the saturation region, its saturation current can be estimated as,

$$I_{DS} = \beta_J (V_{GS} - V_T)^2 \tag{4.26}$$

Where β_J is gain factor of JFET

With V_{GS}=0, it becomes

$$I_{d1} = \beta_{J1}.V_{T1}^2\,,\ I_{d2} = \beta_{J2}.V_{T2}^2$$

Hence, the total current Id is,

$$I_d = \beta_{J1}.V_{T1}^2 + (N-1)\beta_{J2}.V_{T2}^2 \tag{4.27}$$

The balance current for each device is defined by

$$I_b = I_d/N \tag{4.28}$$

Hence, ration of initial unbalanced current is,

$$\frac{\Delta I_d}{I_b} = \frac{|I_{d1} - I_{d2}|}{I_d/N} = \frac{N\left|\beta_{J1}.V_{T1}^2 - \beta_{J2}.V_{T2}^2\right|}{\beta_{J1}.V_{T1}^2 + (N-1)\beta_{J2}.V_{T2}^2} \tag{4.29}$$

Assuming JFET gain factors β_J are equal, then the initial unbalanced ration becomes,

$$\frac{\Delta I_d}{I_b} = \frac{N|V_{T1}^2 - V_{T2}^2|}{V_{T1}^2 + (N-1)V_{T2}^2} \tag{4.30}$$

Take an example of two SiC JFETs in parallel: One with the minimum gate threshold voltage -14V and the other with the maximum threshold voltage -6V

According to Equation 4.30, the ration of initial unbalance current is:

$$\frac{\Delta I_d}{I_b} = \frac{2|(-14)^2 - (-6)^2|}{(-14)^2 + (-6)^2} = 138\%$$

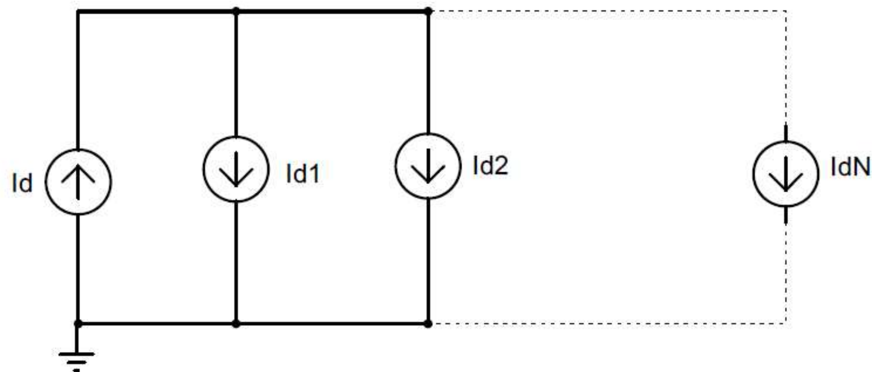


Figure 4.27 Paralleling SiC JFETs operates in saturation region

Simulation validation

The threshold voltages of the two simulated SiC JFETs are identical to the previous example. Figure 4.28 demonstrates the dynamic current sharing of the two devices. As one can observe, the initial current difference between the two devices is as high as 360A and the gap is gradually

close due to self-heating effect. Figure 4.29 shows the rising junction temperatures of the two devices during the short-circuit period. The device with lower threshold voltage has the higher junction temperature and will first reach the temperature limit. This suggests the short-circuit capability of the group paralleling devices is restricted by the device with the lowest threshold voltage.

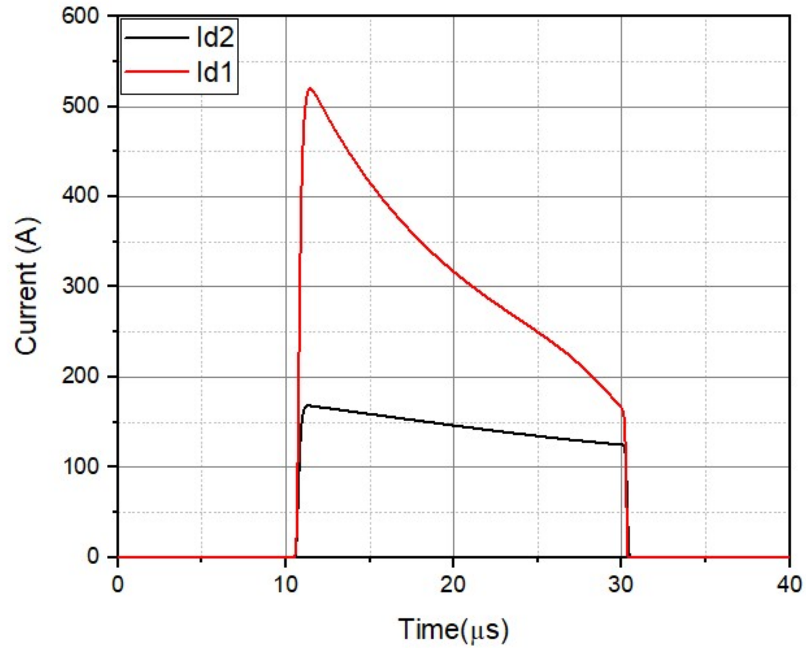


Figure 4.28 Dynamic current sharing of two SiC JFETs in parallel

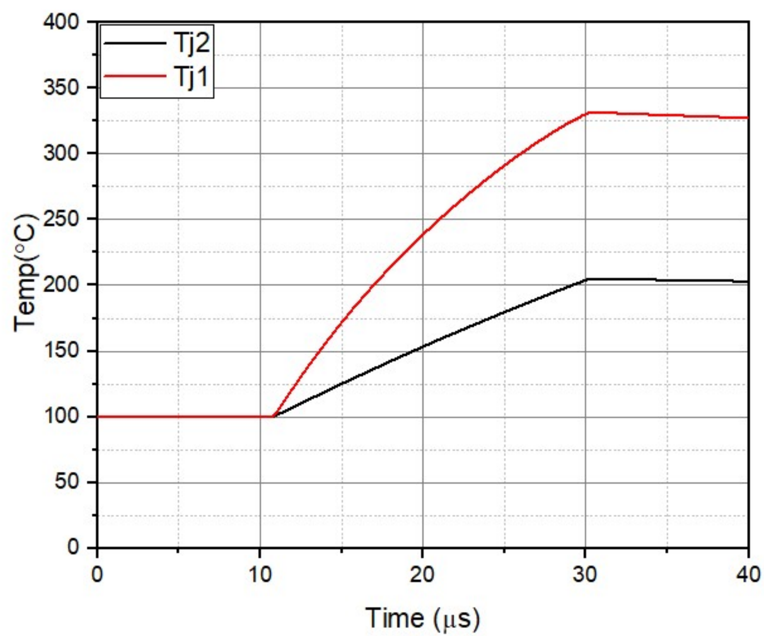


Figure 4.29 Junction temperatures of two paralleling SiC JFETs

4.7 Conclusions

Power semiconductor devices are critical components in SSCBs and must be low in conduction losses, fast in switching speed, and high in short-circuit capability. In this chapter, four types of commercial power semiconductor devices have been evaluated by simulation and experiment. They are compared in terms of device specific on-resistance and short-circuit capability. It concludes SiC JFET is the most suitable choice for low power rating SSCB applications. In the following, the commercial SPICE model of SiC JFET has been modified for being more accurate and being able to model device dynamic thermal performance in a short-circuit mode. Furthermore, device thermal design methodology has been given for both steady state and dynamic state. Finally, SiC JFET devices in parallel have been investigated in both static and dynamic operation. General equations are provided to predict device junction temperature and current sharing in the final stable thermal equilibrium. It concludes the device with lowest on-resistance shares highest static current, leading to the highest junction temperature, whereas the device with the lowest threshold voltage shares the highest dynamic current and would first lead to thermal runaway.

4.8 References

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Chapter 5 Transient Overvoltage Suppression Design

5.1 Introduction

As mentioned in Chapter 1, SSCBs are capable of interrupting fault currents typically three orders faster than its electromechanical counterparts. However, such ultrafast switching operations would produce a high overvoltage causing potential damages to SSCBs and other circuit elements in the system owing to the rapid fall of fault current and system inductance. Furthermore, large magnetic energy stored in the system inductance must be dissipated by other elements since the amount of the energy is usually far higher than that most semiconductor devices can tolerate. Consequently, some effective methods must be in place to suppress the overvoltage and absorb the energy stored in the system inductance. Several approaches were reported and discussed for SSCB applications[1][2][3][4][5]. Two topologies have been commonly adopted alone or combined to achieve this object: resistor-capacitor-diode (RCD) snubbers [6][7]and metal-oxide varistors (MOVs)[8][9].

This chapter begins by reviewing the operating process of both conventional RCD snubber circuits and MOVs including their advantages and disadvantages. Then, a novel snubber circuit by combining an RCD with a MOV is proposed and analysed. In the meantime, the impact factors on the response time of SSCBs are investigated. Then, the proposed snubber for 400V DC SSCBs is designed and is built. Finally, the design is evaluated by both simulation and experiment.

5.2 Review of Overvoltage Suppression Circuits for SSCB Applications

This section explores different voltage clamping solutions presented in the literature, briefly discusses their operating principles, and presents a qualitative comparison among them. Traditional snubber circuit design for converters is not suitable for SSCBs applications because converter snubbers design focuses on minimizing switching loss and fast suppressing voltage which are not the main concerns for SSCBs as the normal operation does not involve switching action. For SSCBs applications, the design of snubber circuit focuses on acceptable overvoltage, energy absorbing capability and peak allowed fault current[3]. Snubber circuits in the form of Capacitor(C), Resistor-Capacitor(RC) or Resistor-Capacitor-Diode(RCD) have been discussed in [2][10]. C type is the simplest using a capacitor across the power

semiconductor. However, the capacitor may oscillate with system inductance during the turn-off. Furthermore, a high discharge capacitive current could flow through the SSCB when it turns on, which may cause the unwanted trip of the SSCB. To address this issue, a current-limiting resistor is added in series to the capacitor forming a RC snubber. However, the high voltage drops across the resistor during interrupting high fault current may damage semiconductor components of SSCBs. To solve this issue, a diode is added in parallel to the resistor forming a conventional RCD snubber which not only eliminates the high voltage drops across the resistor but also avoids the oscillations during the turn-off.

Performance analysis of two fundamental types of circuit configurations of RCD snubber for low voltage DC Microgrid application is presented in [3].

Type 1: Charge-discharge type

As shown in Figure 5.1, charge-discharge type RCD snubber acts as C snubber in the process of interrupting fault current while it behaves as RC snubber when SSCB turns on. However, it results in a higher peak current than SSCB without a snubber circuit. In addition, there exists an oscillation between L_{DC} and C_s in the final stage until the fault energy is exhausted.
Its operating process is simply divided into four stages as described below:
Stage 1: When a short-circuit event occurs, the fault current ramps up until reaching the trip current level of the SSCB.
Stage 2: when the SSCB starts turning off and the diode D_S turns on until the fault current completely commutates from SSCB to the branch of snubber capacitor C_S and the diode D_S.
Stage 3 When C_S begins being charged until the energy stored in system inductance L_{DC} is completely transferred to C_S and hence the voltage across C_S reaches its peak.
Stage 4 When C_S begins discharging through the snubber resistor R_S until its stored energy is fully exhausted and fault current is dampened to zero.

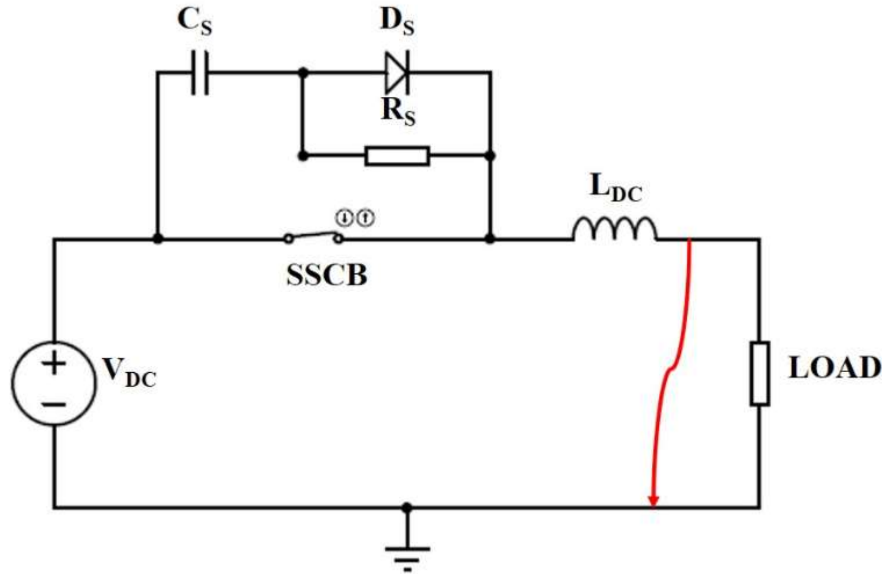


Figure 5.1 Charge-discharge type RCD snubber

Type 2: Discharge-suppressing type

As shown in Figure 5.2, the main difference of the discharge-suppressing type from charge–discharge type is that the resistor Rs is either connected to the ground or tied to Negative pole if the DC system is two poles configuration without Earth or Neutral. Consequently, the snubber capacitor Cs is pre-charged to V_{DC} in normal state. Therefore, in the process of interrupting fault current, the snubber will not turn on until the voltage across SSCB reaches V_{DC}. At this point, the fault current has already start declining. This means SSCB with discharge-suppressing type has the same peak current of the SSCB without snubber circuit. In addition, there is an inherent freewheeling path composed of the snubber diode Ds, snubber resistor Rs and line inductance L_{DC}. As a result, there is no oscillation in the final stage and the overvoltage protection performance of SSCB with this type of RCD snubber is enhanced.

Its operating process can also be divided into four stages as described below:

Stage 1 When a short-circuit fault occurs, the fault current ramps up until it reaches the trip current level of SSCB. At this stage, the snubber is inactive and no currents flow through C_S, D_S and Rs.

Stage 2 When SSCB starts turning off until the voltage across SSCB reaches V_{DC}. Then the snubber diode D_S turns on, the fault current starts commutating from SSCB to the branch of snubber capacitor C_S and diode D_S.

Stage 3 The snubber capacitor C_S is being charged. In the meantime, the freewheeling path

enables part of the energy stored in the inductance to be dissipated through Rs instead of being totally transferred to Cs.

Stage 4 Stored energy in L_{DC} and C_S is dissipated through Rs until the fault current is damped to zero.

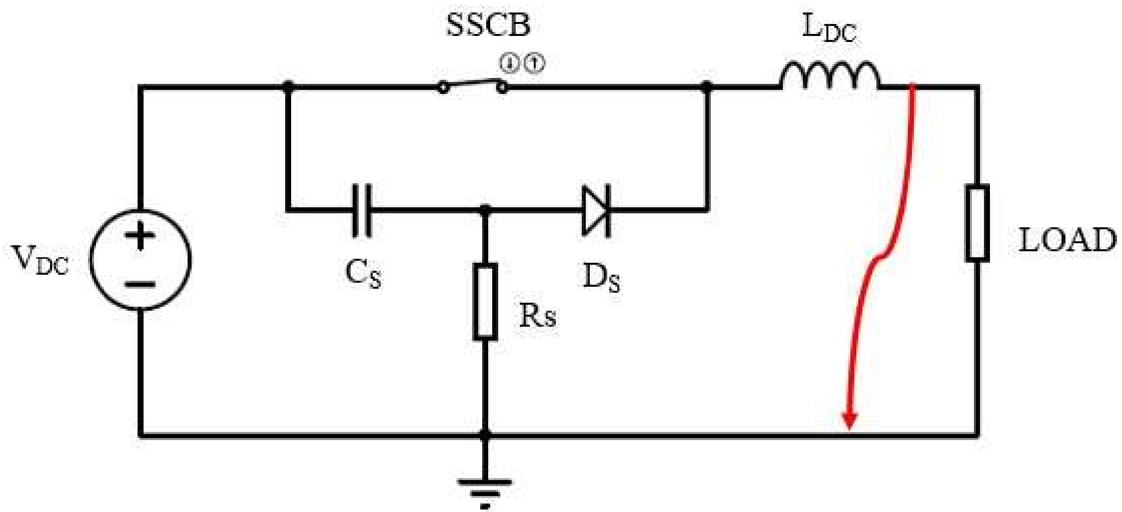


Figure 5.2 Discharge-supressing type RCD

In summary, both of the two types of RCD snubber have the advantage of effectiveness in slowing down the rising rate of the overvoltage(dv/dt) and the ability to clamp the voltage across the SSCBs while discharge-suppressing type RCD snubber has better performance in both overvoltage protection and fault current suppression than the charge-discharge type RCD snubber. However, both require a very high peak power resistor to exhaust the stored energy in a very short period. For example, a DC system with L_{DC}=100μH, trip current 100A and energy dissipating time 100μs, would require a resistor with peak power as high as 5kW resulting in the whole snubber bulky and expensive.

The other common type of voltage clamping component is the metal-oxide varistor (MOV). It is widely used as protecting devices against overvoltage caused by either lightning surges or switching operations. As shown in Figure 5.3, the internal structure of the MOV consists of conductive zinc oxide grains (ZnO) surrounded by thin insulating oxide barriers. The formed inter-grain boundaries between the ZnO grains and the oxide barriers exhibit a barrier potential similar to a semiconductor junction, which features highly nonlinear conductivity [11].

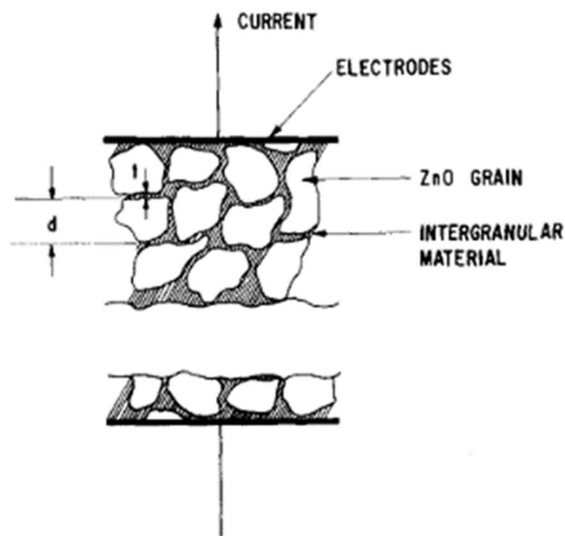


Figure 5.3 Physical Structure of the MOV [11]

A typical characteristic of a MOV is illustrated in Figure 5.4[12]. It has three distinct regions: Linear region (A): Normal operation region, leakage current ≤ 1 mA; Protection region (B): Highly non-linear region where the MOV is conducting to clamp overvoltage under a certain level; High current region (C): In this region, the maximum permissible peak voltage U_{pI} across the MOV is defined by the maximum discharge current I_n. For the appropriate selection of a MOV, several key parameters need to be considered as follows:

- **Continuous operating voltage:** the maximum permissible continuous voltage under normal operation conditions.
- **Reference voltage:** the voltage across the MOV at given reference current (typical value 1 mA). After this point, the MOV is assumed conducting.
- **Residual voltage:** the maximum clamping voltage at given discharge current. It is also called protection level.
- **Energy rating:** the maximum allowed let-through energy without thermal runaway.

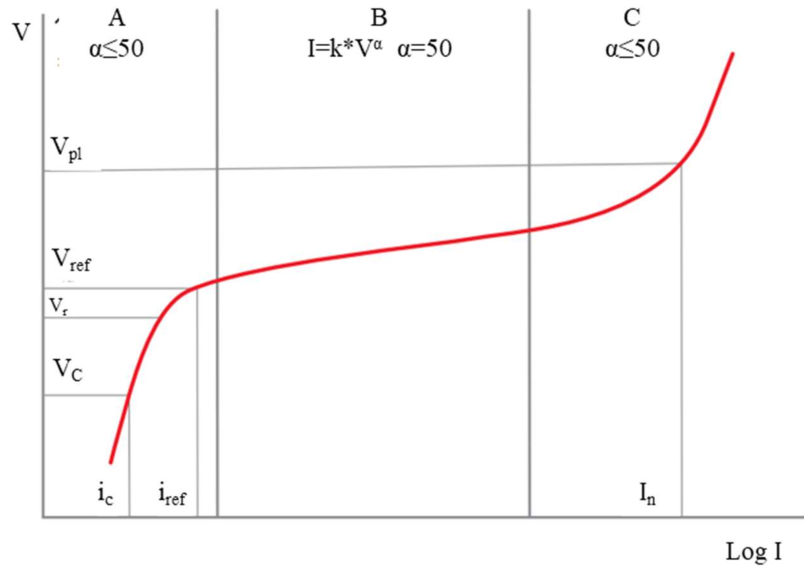


Figure 5.4 Typical V-I characteristic of MOVs ([12])

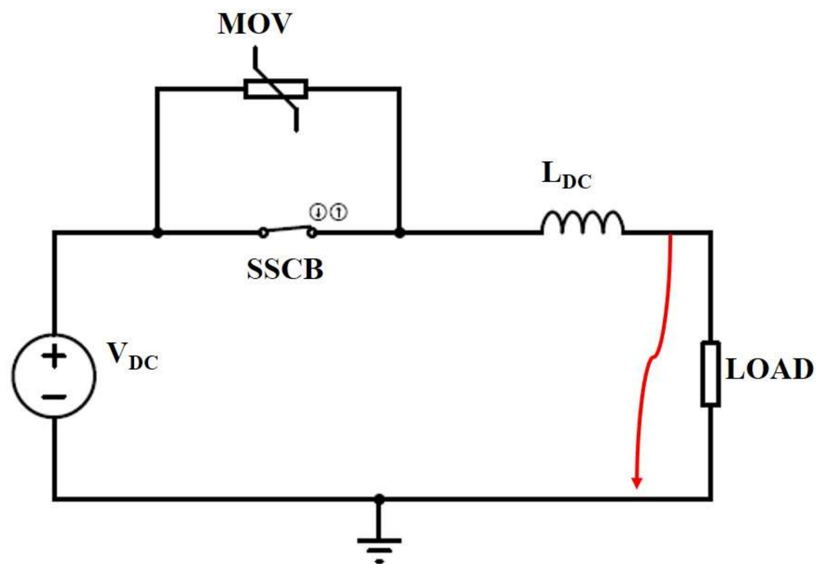


Figure 5.5 MOV as a snubber

Figure 5.5 shows a MOV as a snubber for SSCB applications. Its operating process is divided into two simple stages:

Stage 1: When a short-circuit event occurs, the fault current rapidly ramps up to the trip current level before SSCB starts turning off. Once the voltage across SSCB exceeds the activate voltage of MOV, fault current starts to commutate from SSCB to MOV.

Stage 2: When SSCB turns off and the fault current fully commutates to MOV where the voltage across SSCB is clamped to the protection level of MOV and the energy stored in system inductance L_{DC} is dissipated until fault current is dampened to zero.

The main advantages of the MOV is its simplicity and high energy handling capability with the typical value in the range of hundreds of joules per cubic centimetre[11] . However, it suffers from deterioration over time when frequently exposed to surges and overvoltage transients [13]. In addition, Compared to the RCD snubber, it has no dv/dt control and shows larger transient oscillation on the voltage across the circuit breaker at the turn-off [14].

To take advantages of both RCD snubbers and MOVs, a novel snubber circuit is proposed herein by combining a MOV with an RCD snubber as shown in Figure 5.6. This approach exploits both effective overvoltage suppression of RCD snubbers and high energy absorption capability of MOVs while it eliminates the high-power resistor of RCDs and mitigates the transient fluctuation of MOVs.

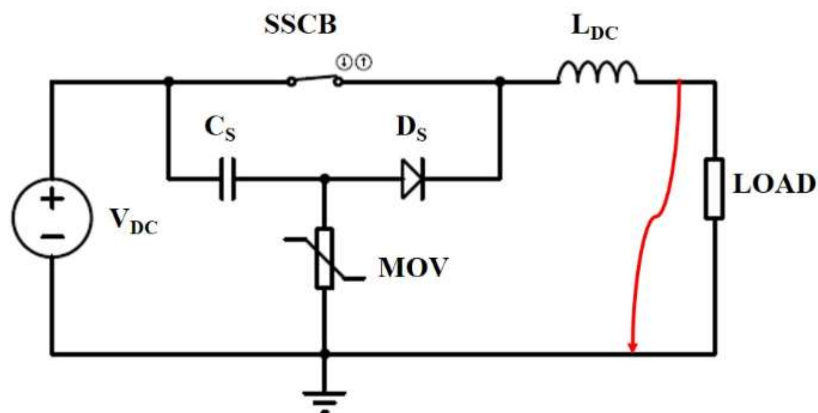
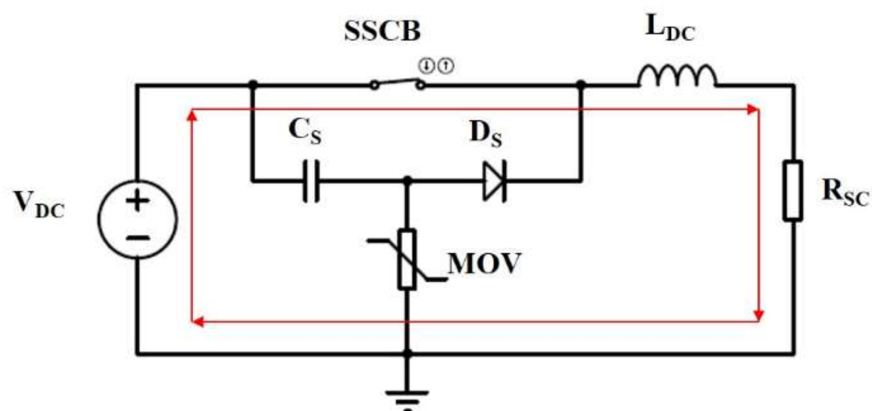
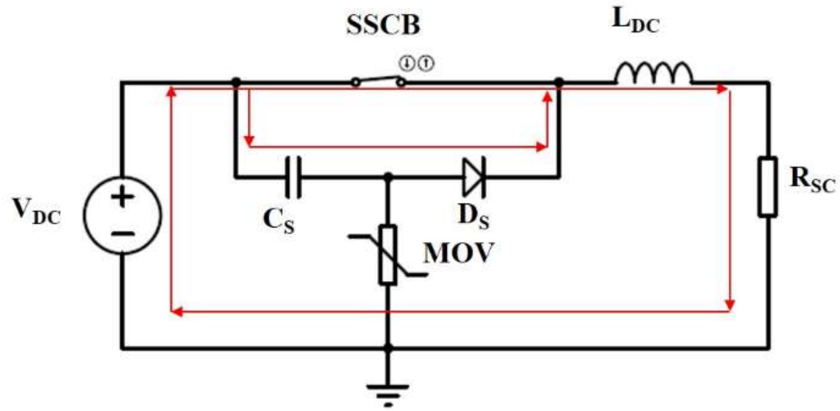


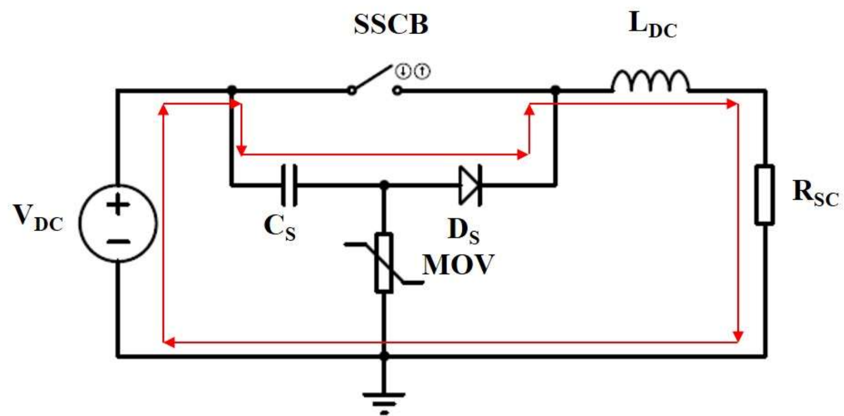
Figure 5.6 Proposed snubber circuit



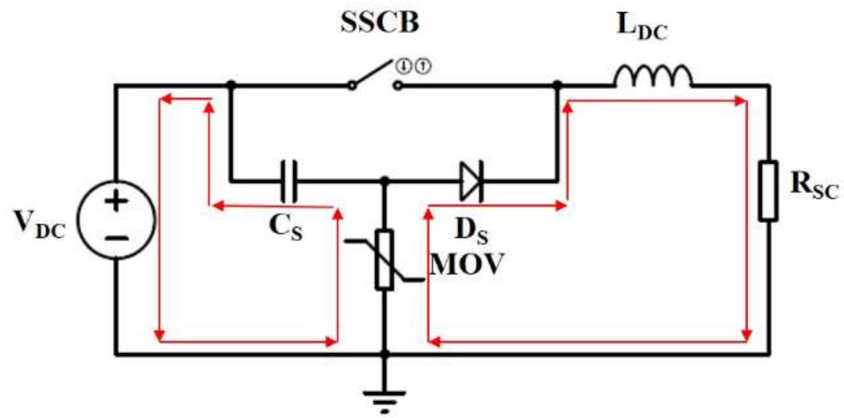
(a) Stage 1



(b) Stage 2



(c) Stage 3



(d) Stage 4

Figure 5.7 Operating process of the proposed snubber

5.3 Analysis of the Operating process of the Proposed Snubber Circuit

Under normal operating conditions, the SSCB remains on, and the snubber capacitor is pre-charged to the supply voltage. When a short-circuit fault occurs, the snubber is activated to suppress the overvoltage. The whole operating process can be divided into 4 stages as shown in Figure 5.7. As can be seen, the equivalent circuit consists of a SSCB, a DC supply voltage source V_{DC}, an equivalent system inductor L_{DC}, an equivalent short-circuits resistor R_{SC} and the proposed snubber circuit configured with C_S, D_S and MOV.

To achieve the main purpose of analysing the operating principle while reducing the complexity, several assumptions are made below:

(1) Ideal SSCB: turn off instantly: T_{off}=0 and on-resistance is neglected.

(2) Ideal Diode: reverse recover characteristic is neglected.

(3) MOV: Leaking current is neglected.

Stage 1 Fault current ramps up (Figure 5.7 (a))

When a short-circuit fault occurs, the fault current ramps up until it reaches the trip current level of SSCB. At this stage, the snubber is inactive and no currents flow through C_S, D_S and MOV.

By applying Kirchhoff Voltage Law (KVL) to the main power circuit loop, the following expression is obtained:

$$V_{DC} = i_f R_{SC} + L_{DC}\frac{di_f}{dt} \tag{5.1}$$

By integrating the equation (5.1) and rewriting it, fault current i_f at this stage can be derived as

$$i_f = I_r \mathrm{e}^{-\frac{R_{SC}}{L_{DC}}t} + \frac{V_{DC}}{R_{SC}}\left(1 - \mathrm{e}^{-\frac{R_{SC}}{L_{DC}}t}\right) \tag{5.2}$$

Hence, time period T_1 when fault current rise from I_r to I_{trip} at this stage can be calculated as:

$$T_1 = \frac{L_{DC}}{R_{SC}}\ln\frac{I_r - \frac{V_{DC}}{R_{SC}}}{I_{trip} - \frac{V_{DC}}{R_{SC}}} \tag{5.3}$$

Where I_{trip} and I_r represent trip current and rated current of SSCB respectively.

Due to the assumption of an ideal SSCB, the on-state voltage across SSCB is zero.

$$V_{SSCB} = 0 \tag{5.4}$$

Stage 2 Fault current commutates from SSCB to the capacitor C_S and D_S (Figure 5.7 (b))

When SSCB starts turning off and then the snubber diode D_S turns on, the fault current is commutating from SSCB to the branch of snubber capacitor C_S and diode D_S. Again, due to the assumption of an ideal SSCB, fault current and voltage across SSCB V_{SSCB} at this stage are considered constant. Thus,

$$i_f = I_{trip} \tag{5.5}$$

$$V_{SSCB} = V_{DC} \tag{5.6}$$

$$T_2 = 0 \tag{5.7}$$

Stage 3 C_S is charged until MOV is activated (Figure 5.7 (c))

The snubber capacitor C_S is being charged until the voltage across MOV reaches its active level (reference voltage V_{ref}). Fault current i_f and V_{SSCB} at this stage can be derived as

$$i_f = I_{trip}\mathrm{e}^{-\alpha_1(t-T_1-T_2)}\cos\left(\sqrt{\omega_1{}^2-\alpha_1{}^2}(t-T_1-T_2)\right) \tag{5.8}$$

$$V_{SSCB} = V_{DC} + \frac{I_{trip}\mathrm{e}^{-\alpha_1(t-T_1-T_2)}}{C_S\sqrt{\omega_1{}^2-\alpha_1{}^2}}\sin\left(\sqrt{\omega_1{}^2-\alpha_1{}^2}\,(t-T_1-T_2)\right) \tag{5.9}$$

where $\alpha_1 = \frac{R_{SC}}{2L_{DC}}, \omega_1 = \frac{1}{\sqrt{L_{DC}C_S}}$

Hence, time T_3 at this stage can be obtained as

$$T_3 = \frac{\sin^{-1}\frac{V_{ref}C_S\omega_1}{I_{trip}}}{\omega_1} \tag{5.10}$$

Stage 4 Fault current commutates from the branch of C_S and D_S to MOV (Figure 5.7 (d))

MOV has been activated and fault current is redirected from C_S and D_S to MOV where stored energy in L_{DC} and C_S is dissipated.

For simplicity, the V-I characteristic of MOV in its active region is assumed to be linear. Thus, V-I relationship of MOV can be simply expressed as:

$$V_{MOV} = V_A + R_B I_{MOV} \tag{5.11}$$

Where V_A and R_B are constant.

Thus, the initial current of MOV I_o can be estimated as

$$I_O = \mathrm{e}^{-\alpha_1 T_3}\sqrt{I_{trip}{}^2-(V_A C_s\omega_1)^2} = \mathrm{e}^{-\frac{R_{SC}}{2L_{DC}}T_3}\sqrt{I_{trip}{}^2-\frac{C_s V_A{}^2}{L_{DC}}} \tag{5.12}$$

Hence, fault current i_f and V_{SSCB} can be obtained respectively as:

$$i_f = I_O \mathrm{e}^{-\frac{R_{SC}+R_B}{L_{DC}}(t-T_1-T_2-T_3)} - \frac{V_A}{R_{SC}+R_B}(1-\mathrm{e}^{-\frac{R_{SC}+R_B}{L_{DC}}(t-T_1-T_2-T_3)}) \tag{5.13}$$

$$V_{SSCB} = V_{DC} + V_A + R_B I_O \mathrm{e}^{-\frac{R_{SC}+R_B}{L_{DC}}(t-T_1-T_2-T_3)} - \frac{V_A R_B}{R_{SC}+R_B}(1-\mathrm{e}^{-\frac{R_{SC}+R_B}{L_{DC}}(t-T_1-T_2-T_3)}) \tag{5.14}$$

Time period T_4 is estimated as

$$T_4 = \frac{L_{DC}}{R_{SC}+R_B}\ln(1+\frac{I_O(R_{SC}+R_B)}{V_A}) \tag{5.15}$$

In the end, the analytical expressions of fault current, voltage across SSCB and time period in each stage are summarised below:

Stage 1

$$\begin{cases} i_f = I_r \mathrm{e}^{-\frac{R_{SC}}{L_{DC}}t} + \frac{V_{DC}}{R_{SC}}\left(1-\mathrm{e}^{-\frac{R_{SC}}{L_{DC}}t}\right) \\ V_{SSCB} = 0 \\ T_1 = \frac{L_{DC}}{R_{SC}}\ln\frac{I_r - \frac{V_{DC}}{R_{SC}}}{I_{trip} - \frac{V_{DC}}{R_{SC}}} \end{cases}$$

Stage 2 $\quad i_f = I_{trip}; \quad V_{SSCB} = V_{DC}; \quad T_2 = 0$

Stage 3

$$\begin{cases} i_f = I_{trip}\mathrm{e}^{-\alpha_1(t-T_1-T_2)}\cos\left(\sqrt{{\omega_1}^2-{\alpha_1}^2}(t-T_1-T_2)\right) \\ V_{SSCB} = V_{DC} + \frac{I_{trip}\mathrm{e}^{-\alpha_1(t-T_1-T_2)}}{C_s\sqrt{{\omega_1}^2-{\alpha_1}^2}}\sin\left(\sqrt{{\omega_1}^2-{\alpha_1}^2}(t-T_1-T_2)\right) \\ T_3 = \frac{\sin^{-1}\frac{V_{ref}C_s\omega_1}{I_{trip}}}{\omega_1} \end{cases}$$

Stage 4

$$\begin{cases} i_f = I_O \mathrm{e}^{-\frac{R_{SC}+R_B}{L_{DC}}(t-T_1-T_2-T_3)} - \frac{V_A}{R_{SC}+R_B}(1-\mathrm{e}^{-\frac{R_{SC}+R_B}{L_{DC}}(t-T_1-T_2-T_3)}) \\ V_{SSCB} = V_{DC} + V_A + R_B I_O \mathrm{e}^{-\frac{R_{SC}+R_B}{L_{DC}}(t-T_1-T_2-T_3)} - \frac{V_A R_B}{R_{SC}+R_B}(1-\mathrm{e}^{-\frac{R_{SC}+R_B}{L_{DC}}(t-T_1-T_2-T_3)}) \\ T_4 = \frac{L_{DC}}{R_{SC}+R_B}\ln(1+\frac{I_O(R_{SC}+R_B)}{V_A}) \end{cases}$$

5.4 Snubber Design for Low Voltage DC SSCB Applications

Table 5.1 lists the main technical specification of the target low voltage DC SSCB for a 400V DC system.

Table 5.1 Technical specification of SSCB

Parameter	**Value**
Rated voltage (110%) V_{DC}	440V dc
Rated current I_r	10A
Response time T_{res}	<55μs
Interruption current I_{trip}	100A
Prospective fault current	>1kA
System inductance L_{DC}	1-100μH
Blocking voltage $V_{B(SSCB)}$	1000V

Selection of snubber components

(1)Selection of capacitor C_S

First condition: The energy stored in C_S must be greater than the energy stored in system inductance L_{DC}. Thus:

$$\frac{1}{2}C_S\left(V_{B(SSCB)} - V_{DC}\right)^2 \geq \frac{1}{2}L_{DC}{I_{trip}}^2 \quad (5.16)$$

$$C_S \geq \frac{L_{DC}{I_{trip}}^2}{\left(V_{B(SSCB)}-V_{DC}\right)^2} = 3\mu F \quad (5.17)$$

Second condition: Rated voltage of C_S must be higher than the maximum surge voltage across SSCB, thus

$$V_{r(Cs)} \geq V_{B(SSCB)} = 1000V \quad (5.18)$$

Hence, 3μF, 1.2kV film capacitor B32774X1305K000 from Vishay[15] is selected.

(2)Selection of diode D_S

A soft and fast recovery power diode is expected. Moreover, pulse current of D_S must be higher than the maximum trip current I_{trip}.

$$I_{r(Ds)} \geq I_{trip} = 100A \quad (5.19)$$

Hence, 120A pulse current, 650V diode IDP40E65D2 from Infineon [16] is selected.

(3)Selection of MOV

First condition: the energy absorption capability of MOV must be higher than the energy stored in the system inductance (L_{DC}=100μH). Thus,

$$E_{MOV} > \frac{1}{2} L_{DC} I_{trip}^{2} = 0.5J \tag{5.20}$$

Second condition: the clamping voltage of MOV must be lower than a certain level to assure the voltage across SSCB below allowed maximum value (1000V). Thus,

$$V_{res(MOV)} \leq V_{B(SSCB)} - V_{DC} = 560V \tag{5.21}$$

Hence, MOV B72220S0171K101 from TDK [17] is selected.

Figure 5.8 illustrates the selected MOV voltage-current characteristic against its linear fitted curve in the active current region (10-100A). Hence:

$$V_{MOV} = 390 + 0.56I \tag{5.22}$$

Thus, the value V_A and R_B is obtained below respectively:

$$V_A = 390V,\ R_B = 0.56\Omega$$

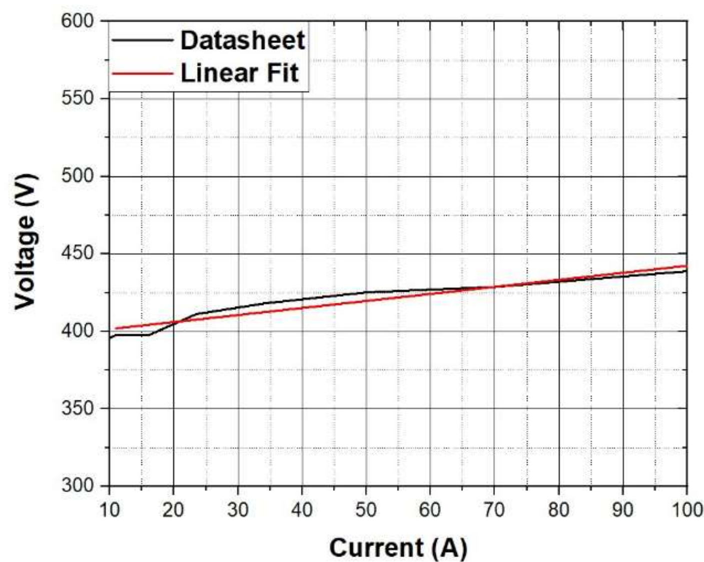


Figure 5.8 V-I characteristic of selected MOV and its linear fitted curve

A. Theoretic calculations of each stage for the proposed snubber

Substituting parameters of selected components into the corresponding equations derived in Section5.3 and assuming worst scenario L_{DC}=100μH and short-circuit resistance R_{SC}=0.4Ω,

fault current i_f, voltage across SSCB $V_{B(SSCB)}$ and time period T in each stage can be calculated as follows.

Stage 1

$$i_f = 1100 - 1090\mathrm{e}^{-0.004t};\ \ V_{B(SSCB)} = 0;\ T_1 = 21.5\mu s$$

Stage 2

$$i_f = 100A; \quad V_{B(SSCB)} = 440V; \quad T_2 = 0$$

Stage 3

$$i_f = 100\mathrm{e}^{-0.002(t-21.5)} \cos\frac{(t-21.5)}{17.3}$$

$$V_{SSCB} = 440 + 577e^{-0.002(t-21.5)} \sin\frac{(t-21.5)}{17.3}$$

$$T_3 = 13.2\mu s$$

Stage 4

$$i_f = 476\mathrm{e}^{-0.0096(t-34.7)} - 406$$

$$V_{SSCB} == 602 + 267\mathrm{e}^{-0.0096(t-3\ \ .7)}$$

$$T_4 = 18\mu s$$

In summary,

Total response time of SSCB is: $T_{res} = 21.5 + 13.2 + 18 = 52.7\mu s$

Maximum overvoltage across SSCB is:

$$V_{SSCB(max)} = V_{DC} + V_A + \frac{V_A R_B}{R_{SC} + R_B} = 869V$$

5.5 Simulation Validation

Pspice is used for simulating the snubber operating process. All parameters used for simulation are identical to the aforementioned theoretical calculations and an ideal semiconductor switch model is selected as SSCB.

Figure 5.9 shows the simulation waveforms including fault current (red line), capacitor current (green line), MOV current (blue line) and voltage across SSCB (black line). As it can be seen, SSCB turns off right after fault current reaches 100A. In the following, fault current is redirected to the snubber capacitor C_S then to MOV where it eventually damps to zero. Meanwhile, the voltage across SSCB starts to rise after turn-off of SSCB until it reaches the peak value around 870V when MOV is activated. In the end, the voltage converges to the steady supply voltage V_{DC} (440V) when fault current is totally cleared off at around 53μs. The simulation results confirm the proposed snubber can suppress the surge voltage below 1000V while keeping the total response time within 55μs.

Furthermore, the analytical results for fault currents in each stage obtained from Table 5.2 are compared with those from simulation. As demonstrated in Figure 5.10, the analytical results match simulation very well. In addition, analytical results of the voltage across SSCB are also compared with simulation results in Figure 5.11. As can be seen, the simulation results show reasonable matching with calculated results except for some discrepancies of transient period between stages due to the assumption involved between ideal SSCB and linear I-V relationship of MOV in the calculations. The simulation results verify the correctness of the theoretic analysis.

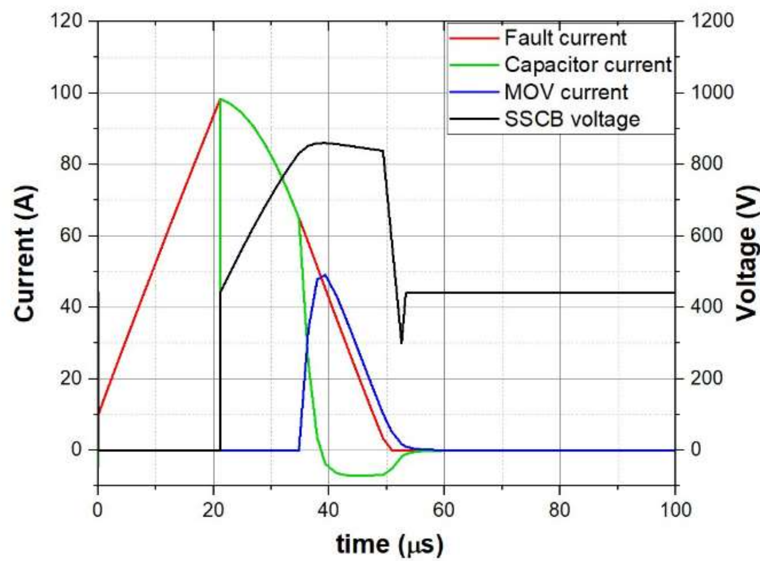


Figure 5.9 Simulation waveforms

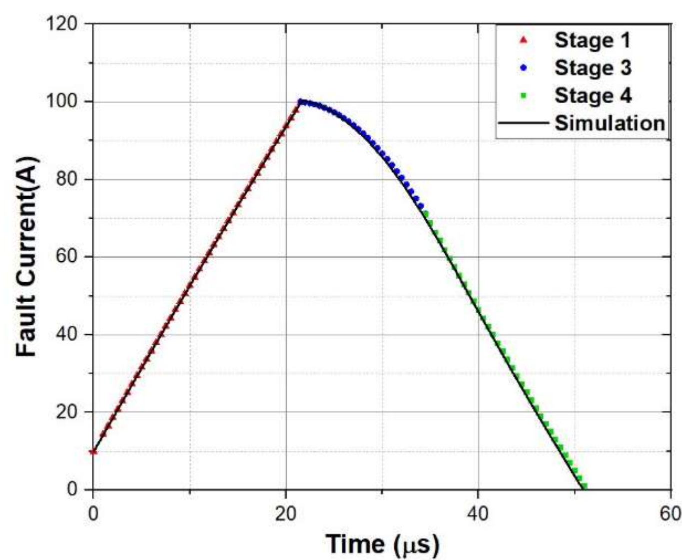


Figure 5.10 Comparison of simulated and calculated fault current in each stage

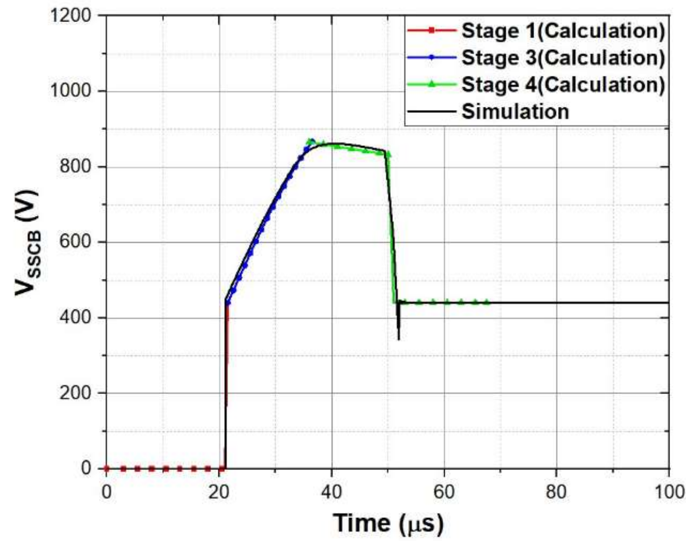


Figure 5.11 Comparison of simulated and calculated voltage across SSCB in each stage

5.6 Experiment Validation

The experiment of the proposed snubber circuit is conducted in a DC system. Table 5.2 lists the parameters of selected components of experimental set-up. A test bench is built as sketched in Figure 5.12 where a power switch IGBT IRG4PSH71UD [18] acting as a SSCB, is controlled by a gate driver setting the pulse duration of short-circuit current. Figure 5.13 shows the hardware of the experimental setup.

Table 5.2 Parameters of each component of test bench

Parameter	**Value**
Supply voltage V_{DC}	100-250V
Trip current Itrip	10-30A
Snubber Capacitance C_S	3 μF B32774X1305K000[16]
Snubber Diode D_S	IDP40E65D2[17]
MOV	B72220S0111K101[18]
Power switch (IGBT) SSCB	IRG4PSH71UD [19]
System inductance L_{DC}	100-200μH

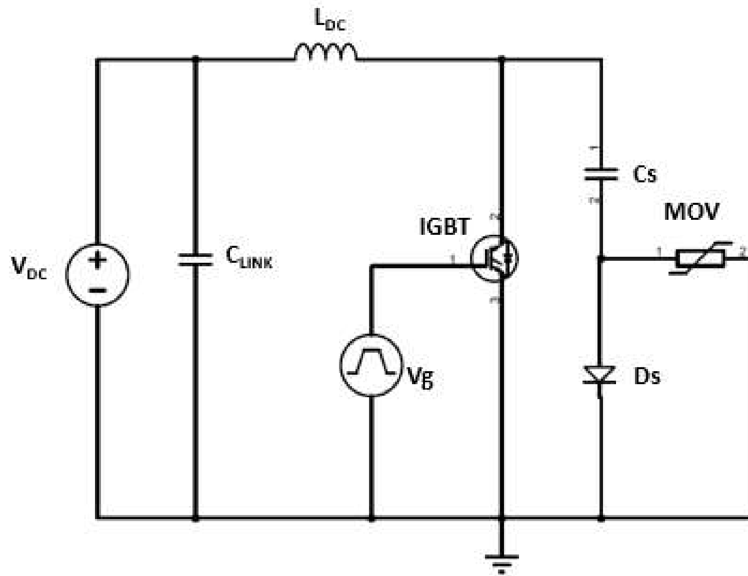


Figure 5.12 Schematic of the snubber test bench

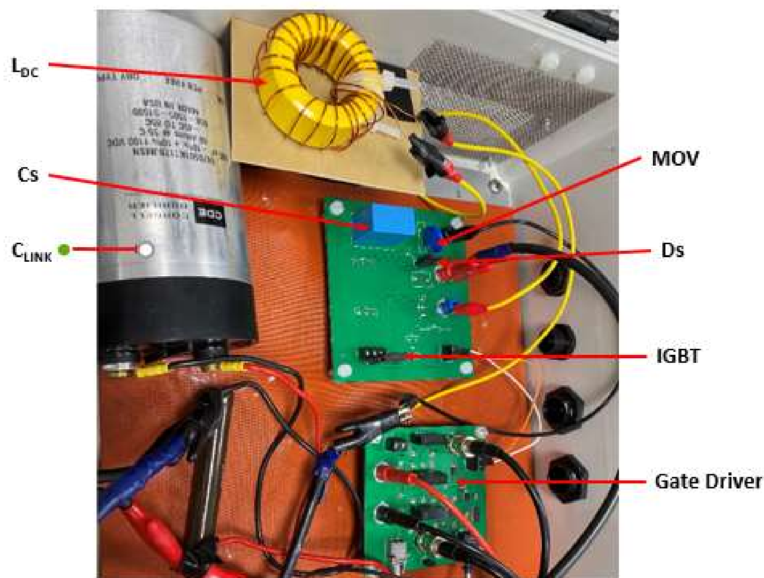
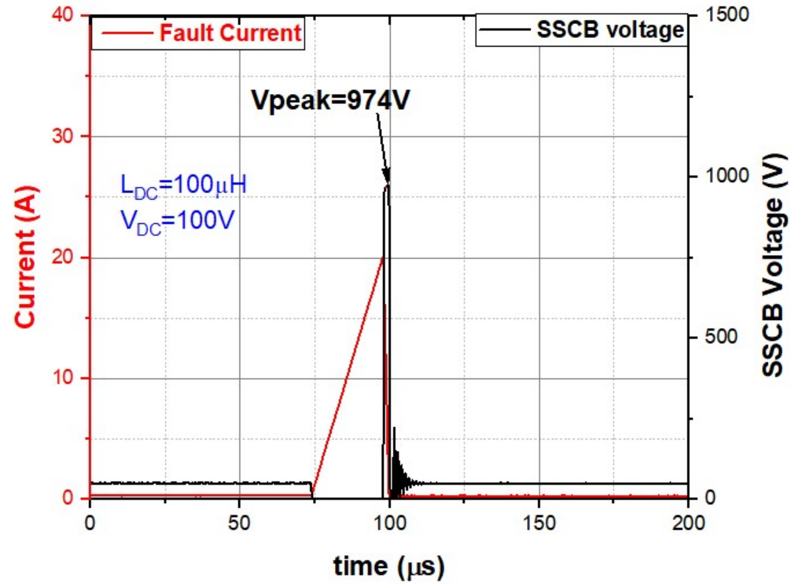


Figure 5.13 Hardware of the experimental setup

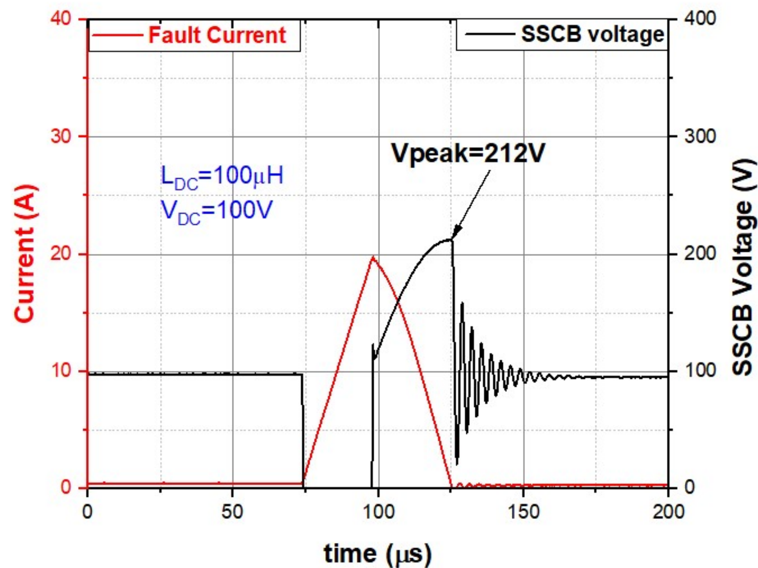
Figure 5.14 shows the experimental results of SSCB without a snubber in Figure 5.14 (a) and with the proposed snubber in Figure 5.14 (b) under the same test condition: L_{DC}=100μH, V_{DC}=100V. As can be seen, the peak voltage across SSCB is as high as 974V without a snubber compared to only 212V with the proposed snubber.

Figure 5.15 presents the waveforms under the test conditions: L_{DC}=180μH combined with different supply voltages of 150V, 200V and 250V respectively. The results demonstrate the overvoltage across SSCB can be effectively suppressed less than twice of the supply voltage

with the proposed snubber. Meanwhile, it is worth noticing that in Figure 5.15 (a) and (b) voltage ringing appears at the end of the process, which would lead to longer recovery time of SSCB. The reason is that MOV under lower overvoltage has not been fully activated, resulting in less dampening effect on the oscillation. In contrast, Figure 5.15 (c) shows no ringing due to higher overvoltage across MOV.

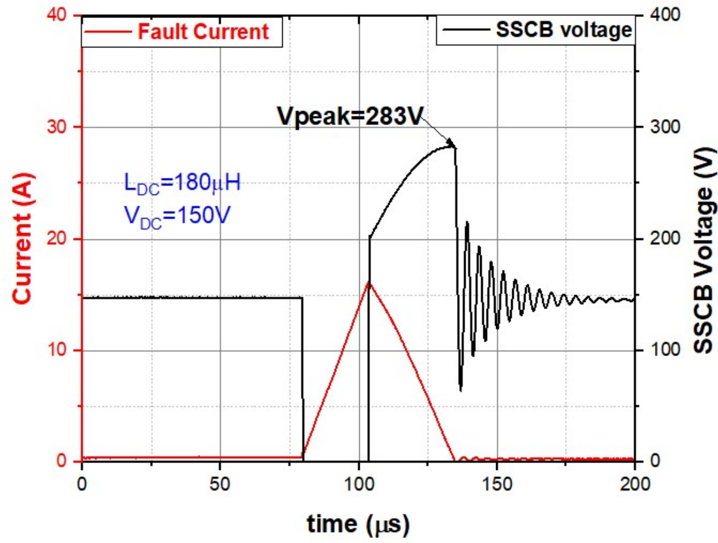


(a) Switching operation without a snubber
((L$_{DC}$=100 μH, V$_{DC}$=100V)

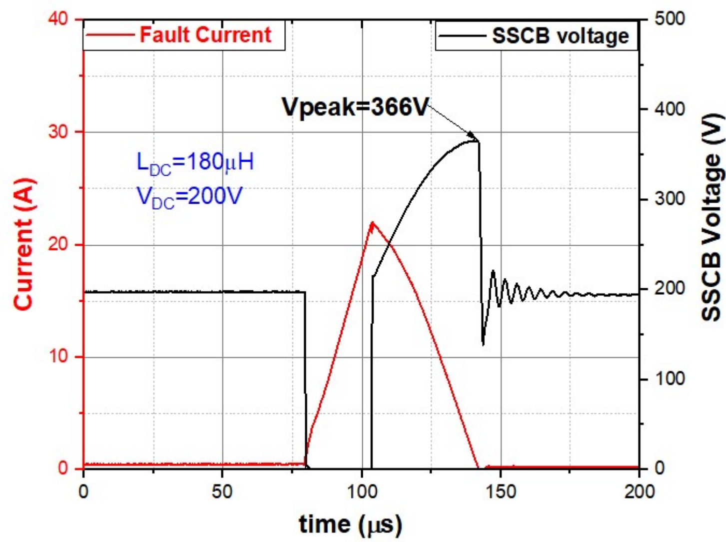


(b) Switching operation with the proposed Snubber
(L$_{DC}$=100 μH, V$_{DC}$=100V)

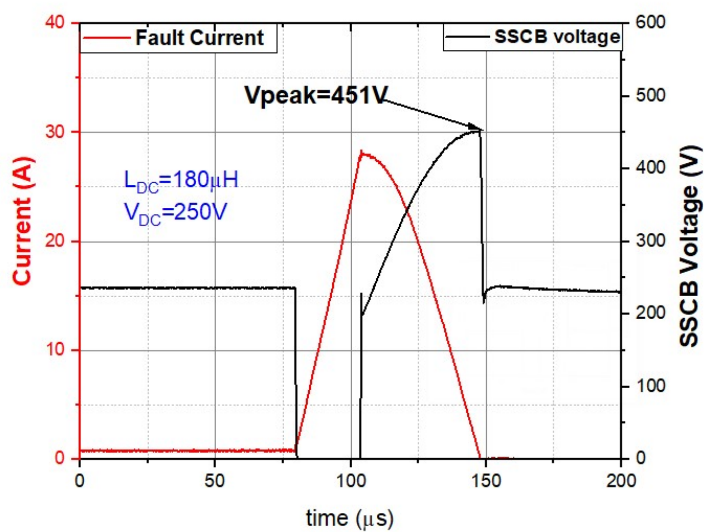
Figure 5.14 Switching operation without and with the proposed snubber



(a) V_{DC}=150V



(b) V_{DC}=200V



(c) V_{DC}=250V

Figure 5.15 Experimental Results with the proposed snubber under the condition of LDC=180 μH

Figure 5.16 compares the waveforms of fault current and voltage across SSCB of experiment against simulation under the same condition: L_{DC}=100µH and V_{DC}=135V. As can be seen, it demonstrates a reasonable match between them although there are obvious discrepancies mainly attributed to the parasitic impedance of the wires and PCB traces, which are not accounted for the simulation.

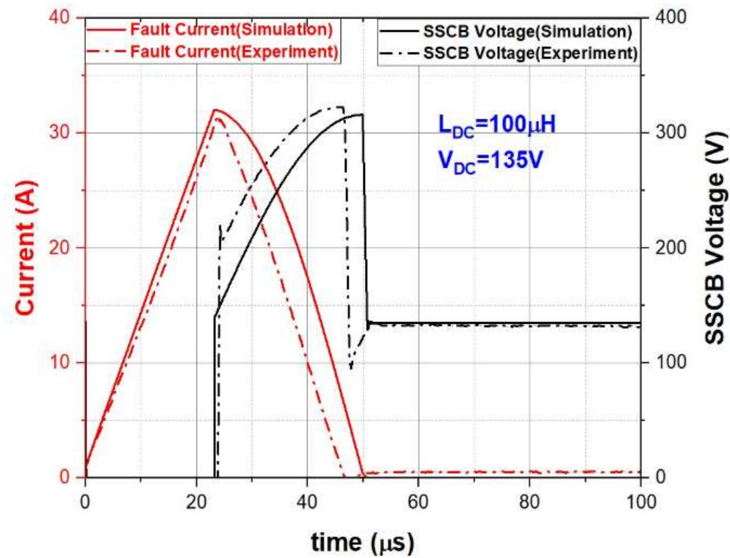


Figure 5.16 Comparison of experiment and simulation results

5.7 Discussions

A. Discussions of impact factors on the response time of SSCBs

It is well known that adoption of snubbers can prolong the response time of SSCBs. For this reason, it is vital to investigate how the response time is influenced. Figure 5.17 shows the simulation results of how the response time of SSCBs varies with MOV clamping voltage, snubber capacitance, system inductance and trip current respectively. As indicated, the increase of MOV clamping voltage can reduce the response time whereas the response time would increase in line with the rising snubber capacitance, system inductance and trip current level. Therefore, a designer can manipulate these factors to meet their own design objective. For simplicity, the response time of SSCBs can be approximated by the equation below:

$$T_{res} = L_{DC} I_{trip} \frac{V_{DC}+V_A}{V_{DC} V_A} + \frac{\sqrt{C_S L_{DC}}}{2} \tag{5.23}$$

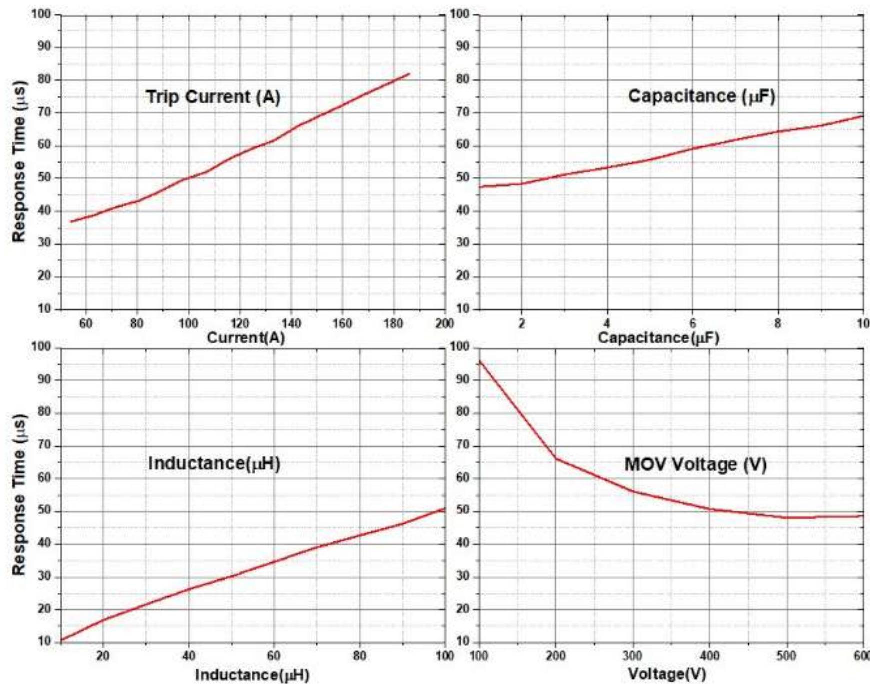


Figure 5.17 Response time as a function of trip current, snubber capacitance, system inductance and MOV clamping voltage

B. Discussions of impact of the assumptions on the snubber performance

Despite a limited impact on the snubber performance due to the assumptions for simplifying the theoretic analysis, it will be discussed here for completeness. First, the assumption of instant turn-off of SSCB tends to reduce the total response time. However, the turn-off time of semiconductor devices is generally on the order of several hundreds of nanoseconds, almost two orders lower than the total response time of SSCBs (tens of microseconds). Consequently, the influence is insignificant. Secondly, the negligence of on-state voltage of SSCBs would increase the rising speed rate of fault current thereby reducing the time period T1 in the first stage as defined by equations (5.1) and (5.3). However, compared to the power supply voltage V_{DC}, the voltage drop of SSCBs is negligible and hence its influence is very limited. The next assumption of no reverse current for diode D_S would have an impact on the snubber performance in the final stage where the diode is changing from a forward mode to a reverse mode. Since the diode with a slow and hard recovery characteristic would cause transient oscillations or high voltage spikes during this stage, a soft and fast recovery diode with the recovery time below 100 ns is expected. Undoubtedly, the selected diode should be verified in the actual circuit to ensure the snubber performance is as expected. The final assumption of no leaking current of MOV has no influence of the snubber performance rather than MOV itself

as a larger leaking current of MOVs tends to lead to the faster deterioration of MOV in the long run. In this scheme, the leaking current of MOV as a function of applied voltage is negligible as no voltage is exposed to MOV under normal operating conditions. To conclude, if designed properly, these assumptions have little impact on the total performance of snubbers.

C. Comparison with conventional RCD snubbers and MOVs

For comparison, a conventional RCD circuit is simulated, as constructed by simply replacing the MOV of the proposed snubber with a 20Ω snubber resistor R_S and keeping all other parameters of the system identical to the proposed snubber. As shown in Figure 5.18, the fault current waveforms of both solutions are almost identical. In addition, the peak voltage across SSCB with the proposed snubber has the same level with that of the conventional RCD snubber. Figure 5.19 compares the current and power through the resistor Rs of the RCD snubber with that through the MOV of the proposed snubber. As observed, both Rs and MOV experience very high peak power, 10kW and 20kW respectively. Also, it is noticed that as long as 300μs is needed to dampen the RCD snubber current to zero using the resistor Rs whereas the proposed snubber with MOV can do so by only around 55μs. Furthermore, Table 5.3 conceptually compares performances of the three topologies in terms of key parameters. It shows that the proposed snubber integrates short response time of MOV with low overvoltage and small transient fluctuation of RCD. To conclude, the results demonstrate that the proposed snubber not only can suppress the overvoltage as effectively as the conventional RCD snubber but also shorten the recovery time of SSCBs while it replaces the high-power bulky and expensive resistor with a low cost and high energy absorption capability of MOV.

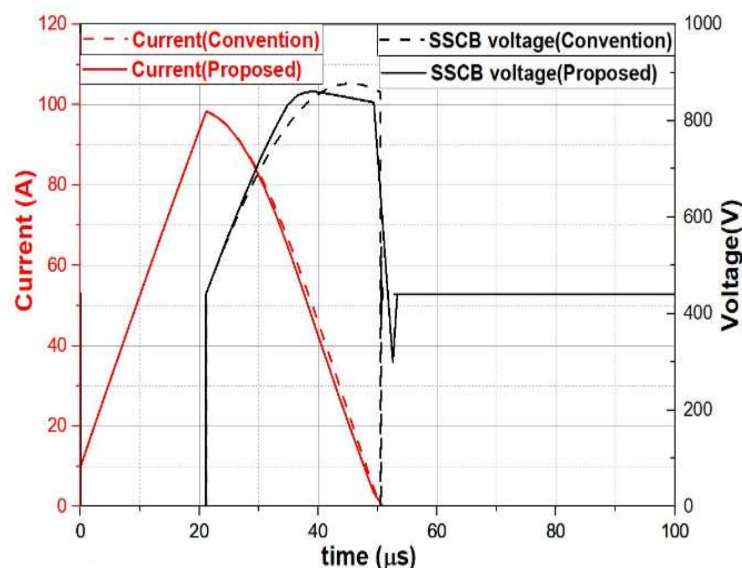


Figure 5.18 Comparison of fault current and SSCB voltage

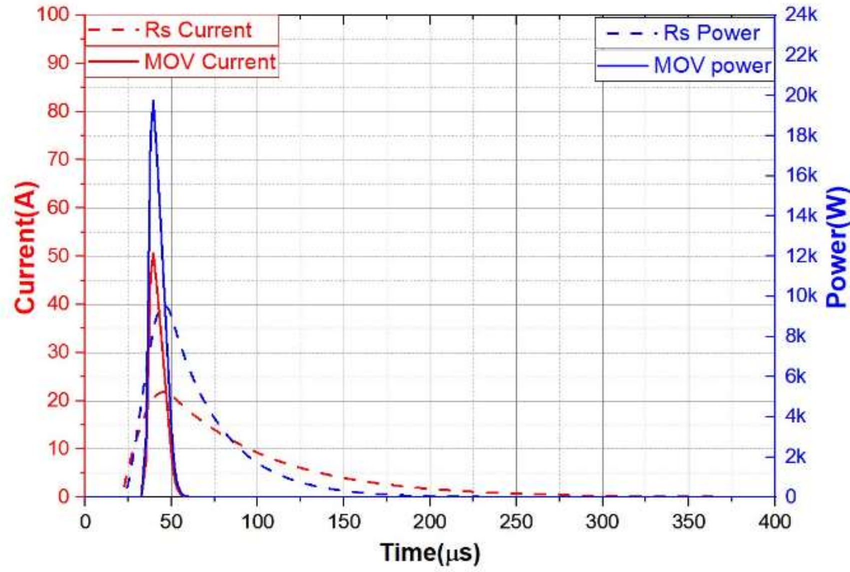


Figure 5.19 Comparison of current and power through Rs and MOV

Table 5.3 Comparison of the three snubber methods

Parameter	Conventional RCD	MOV	Proposed Snubber
Peak voltage	<900V	<1000V	<900V
Peak current	100A	100A	100A
Response time	<55 μs	<50 μs	<55 μs
Transient fluctuation	<1% peak voltage	<10% peak voltage	<1% peak voltage
Cost*	£45	£0.7	£5
*Note: component cost calculations are based on current UK market price.			

5.8 Conclusions

In this chapter, a novel snubber circuit has been proposed for 400V DC solid-state circuit breakers. It takes the advantages of effective overvoltage suppression of RCD snubbers and high energy absorption capability of MOVs while eliminates the requirement of high-power resistor of RCD snubbers and mitigates the transient fluctuation of MOVs. Its operation principle has been analysed and analytical expressions are given, providing guidance for the snubber design for SSCBs application. Both simulation and experiment results have validated the correctness of the snubber design. In addition, the impact factors on the response time of SSCBs have been investigated for optimal snubber design to meet different application requirements. Finally, a prototype snubber has been built and experimentally evaluated.

5.9 References

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Chapter 6 Development of a SSCB for Short-circuit Protection

6.1 Introduction

Short-circuit faults are the most severe in power converters-based DC systems. This could occur in various locations for example DC source sides, DC bus or load sides, caused by different mechanisms such as cable insulation breakdown [1], components failure [2] or switching devices overshoot [3]. The fault current could rise to a significantly high level within an extremely short-time span [4], which imposes tremendous thermal and electrical stresses to the DC system and its components. Therefore, it is vital to protect DC systems from the damages caused by short-circuit faults with fast protection speed devices such as SSCBs.

This chapter will demonstrate the design and development of a SSCB. The proposed SSCB is configured with a high-voltage normally-on SiC-JFET and low-voltage normally-off Si MOSFET based on the circuit topology of the TBU presented in Chapter 3. Compared to the conventional SSCBs, the proposed SSCB for short-circuit protection offers several advantages. First, it does not require complicated and time-consuming sensing and tripping circuitry and therefore has fast response speed. As reviewed in Chapter 2, most SSCBs reported in the literature rely on dedicated fault current sensing circuit and complicated communication system to response for short-circuit faults. For example, the SSCB reported in [5] uses a current sensor, a microcontroller and a high-speed D/A converter. Secondly, the normally-on SiC JFET offers both low specific on-resistance and exceptional robustness under short-circuit conditions. It is reported in [6] that a commercial 1.2kV SiC JFET can withstand a 10A current with duration of 660μs under a 400V DC voltage, corresponding to a critical energy of 2.4J. Last but not the least, the tripping current level of the proposed SSCB is adjustable for various applications.

6.2 Short-circuit Protection Requirements

According to the characteristics of DC fault currents, some of the key design requirements are provided in the following for DC short-circuit protection devices[7][8][9].

1) Speed

Short-circuit faults must be removed as fast as possible to prevent from any irreversible damages on the DC system. On the one hand, compared to other elements in a DC system, power semiconductor devices have the lowest short-circuit withstand capability, making them

the most vulnerable parts in a DC system. On the other hand, DC short-circuit fault currents feature with high magnitude and high derivative as discussed in Chapter 1. Therefore, the response speed is critical to restrain both the magnitude and duration of fault currents below the short-circuit withstand capability of semiconductor devices.

2) Selectivity

The protective devices in a DC system should coordinate each other to provide protection selectivity. This requires the only protective device closest to the fault location should act to isolate the fault without interrupting other parts of the system.

3) Reliability

The protective device should only act for the fault event but remain on for transients or noises such as inrush current caused by the start-up of load connections.

4) Simplicity

It is desirable to keep the component counts as low as possible with simplistic design approach.

5) Flexibility

The protection system should be as versatile as possible to accommodate various requirements based on the application.

6) Fail-safe

The protection device should be fail-save in the event of losing the external supply power.

6.3 Tripping mechanism in the literature

The tripping mechanism for SSCBs varies with circuit topology used. In the literature, most SSCBs adopt to communication-based topology [10][11][12]. The current sensing signal is fed to a digital control unit such as a microcontroller or DSP through signal amplifier and filter stage and A/D converter circuits, where the measured current is compared with the trigger level and open the circuit breaker when the value is exceeded. Meanwhile, other circuit topologies have been also reported in the literature. For example, a circuit topology called Z-source was proposed in [13]. This topology utilizes a LC network to automatically switch off SCR during a fault. It features fast turn-off and simple control. However, it only works under the high dynamic fault currents to be used for activating the Z-source network.

Reference [14] proposed a self-trigger turn-off circuit topology for SSCB application. The SSCB detects short circuit faults by sensing the drain voltage rise of the SiC JFET power device and switches off by an isolated DC/DC converter which draws power from the fault condition. Hence, the main advantage of this topology is not requiring an external power supply. However, there exist some limitations. For example, it cannot be manually switched off due to

lack of power supply, which is essential for the routine maintenance of a circuit breaker. In addition, this topology requires high fault current and high voltage drop across the power devices to activate its gate driver, which is contradict to the fundamental requirement of SSCBs : the least on-state conduction loss.

Some researchers proposed desaturation sensing and tripping circuits for IGBT-based SSCBs [15][16]. Desaturation detection utilizes the IGBT itself as the current measurement component. When a short-circuit event occurs, the IGBT is driven out of the saturated region and into the linear region of operation. This results in a rapid increase in the collector-emitter voltage which can be used to indicate the short-circuit fault and then activate the gate driving circuity to switch off the IGBT. This can be accomplished by commercially available gate driver chips with desaturation feature. However, care needs to be taken in implementing desaturation detection to prevent false tripping. For instance, it can occur when the IGBT transits from off-state to on-state when it is not fully in the saturated state.

6.4 Basic Configuration of the circuit topology for SSCB application

The basic circuit topology of the proposed SSCB comes from the basic TBU presented in Chapter 3. As shown in Figure 6.1, the basic circuit of the proposed SSCB is constructed by a high-voltage normally-on n-channel SiC JFET and a low-voltage normally off p-channel MOSFET with their sources tied together and their gates linked to the opposite drains. To turn on the normally-off p-MOSFET during normal operating conditions, an external gate biased voltage source Vs is required.

Table 6.1 analogies the proposed SSCB with the basic TBU. As can be seen, a high-voltage depletion-mode n-channel SiC JFET replaces the high-voltage depletion-mode n-channel MOSFET while a low-voltage enhancement mode p-channel MOSFET substitutes the low-voltage depletion mode p-channel JFET. In addition, an external voltage is required to achieve normally-on operation of the SSCB. Compared to the TBU, the proposed SSCB has much higher power rating, lower conduction losses, and higher short-circuit capability. In addition, the external voltage offers the possibility to tune the tripping current. However, the required external voltage might cause the inconvenience for some practical applications. In practice, it could be generated from a standard DC power supply through a DC/DC converter which can output multiple voltages [17]. For example, a standard 24V DC power supply can be used as the input of a DC/DC converter for producing various voltages.

Table 6.1 Analogue between basic TBU and the proposed SSCB

Basic TBU	**Proposed SSCB**
Depletion mode n-channel high-voltage Si MOSFET	Depletion mode n-channel high-voltage SiC JFET
Depletion mode p-Channel low-voltage Si JFET	Enchantement mode p-channel low-voltage Si MOSFET
No external voltage source	Need external voltage source Vs

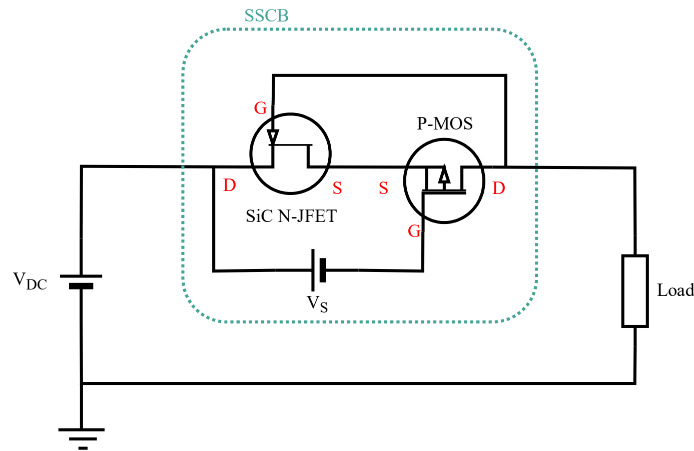
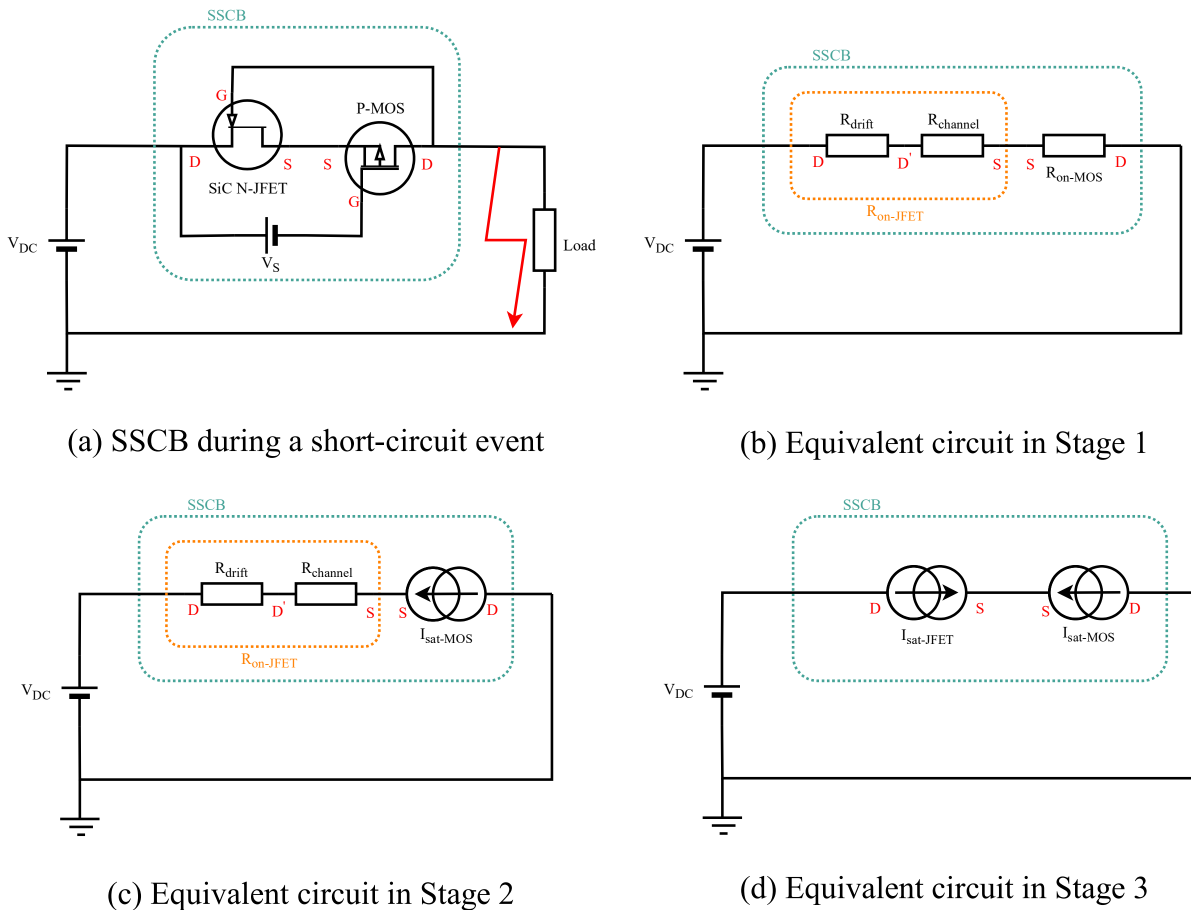


Figure 6.1 Basic circuit topology for SSCB application



(a) SSCB during a short-circuit event

(b) Equivalent circuit in Stage 1

(c) Equivalent circuit in Stage 2

(d) Equivalent circuit in Stage 3

Figure 6.2 Equivalent circuits of the proposed SSCB in each stage

6.5 Analysis of the Operating Principle of the Proposed Circuit

During the normal operating condition, the load current flows through the SSCB. As shown in Figure 6.2, when a short-circuit fault occurs in the load side, initially, the voltages across both SiC JFET and MOSFET linearly increases with the rising current. Then, at some point, either MOSFET or SiC JFET will be driven to operate in the saturation region. Thus, it starts limiting the current. In the end, both SiC JFET and MOSFET operates in the saturation region until the current decreases to zero. The turn-off process of the circuit can be divided into three stages as analysed in detail in the following.

Stage 1: Both the n-channel SiC JFET and the p-channel MOSFET operate in the linear region

Initially, the voltages across both the SiC JFET and MOSFET increases with the fault current (Ohmic). As shown in Figure 6.2(b), the equivalent circuit in this stage includes both on-resistances of SiC JFET ($R_{on\ (JFET)}$) and Si MOSFET ($R_{on\ (MOS)}$). The $R_{on\ (JFET)}$ of high voltage SiC JFET can be further subdivided into channel resistance $R_{channel}$ and drift region resistance R_{drift}.

For the low voltage p-channel MOSFET in the linear region, the expression of current-voltage relationship is presented as follows[18]:

$$-I_{DS(MOS)} = \frac{\beta_M}{2}\left[2\left(V_{GS(MOS)} - V_{th(MOS)}\right)V_{DS(MOS)} + V_{DS(MOS)}{}^2\right] \tag{6.4}$$

Where $V_{th(MOS)}$ is gate threshold voltage of p-MOSFET and β_M is the gain factor of p-MOSFET.

Since the voltage across the MOSFET is extremely low in this stage, a linear relationship between the current and the voltage is assumed. Thus, Equation (6.4) is simplified as:

$$I_{DS(MOS)} = -\beta_M\left[\left(V_{GS(MOS)} - V_{th(MOS)}\right)V_{DS(MOS)}\right] \tag{6.5}$$

According to the circuit as shown in Figure 6.2(a):

$$V_{GS(MOS)} = V_{DS(JFET)} - Vs \tag{6.6}$$

Substituting Equation (6.6) into (6.5) and rewriting, Equation 6.7 is obtained as:

$$I_{DS(MOS)} = \beta_M\left(Vs + V_{th(MOS)} - V_{DS(JFET)}\right)V_{DS(MOS)} \tag{6.7}$$

Re-arranged as:

$$V_{DS(MOS)} = \frac{I_{DS(MOS)}}{\beta_M\left(Vs + V_{th(MOS)} - V_{DS(JFET)}\right)} \tag{6.8}$$

Since a high-voltage SiC JFET has a thick drift region to support the blocking voltage, it is essential to include the drift region resistance R_{drift} into the equivalent circuit [19]. Therefore, for the n-channel high voltage SiC JFET in the linear region, the following relationship can be found as:

$$V_{DS(JFET)} = V'_{DS(JFET)} + I.R_{drift} \tag{6.9}$$

where $V'_{DS(JFET)}$ is the voltage across the channel.

Similarly, I-V relationship across the channel of the SiC JFET can be expressed as[10]:

$$I_{DS(JFET)} = \beta_J\left[2\left(V_{GS(JFET)} - V_{po}\right)V'_{DS(JFET)} - {V'_{DS(JFET)}}^2\right] \tag{6.10}$$

Where V_{po} is pinch-off voltage of the JFET and $\beta_J$is the gain factor of the JFET.

Since in this stage $V_{GS(JFET)}$ is almost zero, Equation (6.10) can be simplified as:

$$I_{DS(JFET)} = -2\beta_J V_{po}.V'_{DS(JFET)} - \beta_J {V'_{DS(JFET)}}^2 \tag{6.11}$$

Solving the quadratic equation (6.11), $V'_{DS(JFET)}$ is obtained as:

$$V'_{DS(JFET)} = -V_{po} - \sqrt{{V_{po}}^2 - \frac{I_{DS(JFET)}}{\beta_J}} \tag{6.12}$$

According to the circuit in Figure 6.2(a), the following relationships can be found.
The voltage across the SSCB:

$$V = V_{DS(JFET)} - V_{DS(MOS)} \tag{6.13}$$

The current flowing through the SSCB:

$$I = I_{DS(JFET)} = -I_{DS(MOS)} \tag{6.14}$$

In the end, using the Equations (6.8), (6.9), (6.12), (6.13) and (6.14), the output I-V characteristics of the SSCB can be derived as:

$$V = -V_{po} - \sqrt{{V_{po}}^2 - \frac{I}{\beta_J}} + \frac{I}{\beta_M\left(Vs + V_{th(MOS)} + V_{po} + \sqrt{{V_{po}}^2 - \frac{I}{\beta_J}} - I.R_{drift}\right)} + I.R_{drift} \tag{6.15}$$

Stage 2: The p channel MOSFET enters saturation region while the n channel JFET remains in the linear region (assuming $|V_{po}| > |Vs + V_{th(MOS)}|$).

As shown in Figure 6.2(c), when the voltage across the SSCB continues to increase, at some point, either the MOSFET or the JFET will first move into saturation region.

According to the saturation condition [20], the p-MOS will operate in the saturation region when the following condition is met:

$$-V_{DS(MOS)} \geq -(V_{GS(MOS)} - V_{th(MOS)}) \qquad (6.16)$$

Combing Equations (6.6), (6.13) and (6.16), the saturation condition of p-MOSFET can be obtained as:

$$V \geq Vs + V_{th(MOS)} \qquad (6.17)$$

Similarly, the n-JFET will enter the saturation region when the following condition is met:

$$V \geq -V_{PO} + I.R_{drift} \qquad (6.18)$$

Thus, assuming $-V_{PO} > Vs + V_{th(MOS)}$, the p-MOSFET will first move into the saturation region at the moment of the voltage across the SSCB $V = Vs + V_{th(MOS)}$.

For the p-MOS operating in the saturation region, the I-V relationship is expressed as[10]:

$$I_{DS(MOS)} = -\frac{\beta_M}{2}(V_{GS(MOS)} - V_{th(MOS)})^2 \qquad (6.19)$$

Substituting Equation (6.6) and (6.14) into (6.19) and rearranging it, the $V_{DS(JFET)}$ can be derived as:

$$V_{DS(JFET)} = -\frac{\sqrt{2I}}{\sqrt{\beta_M}} + V_{th(MOS)} + Vs \qquad (6.20)$$

Since the n-JFET remains in the linear region, Equation (6.10) is re-arranged as:

$$V_{GS(JFET)} = V_{PO} + \frac{V'_{DS(JFET)}}{2} + \frac{I_{DS(JFET)}}{2\beta_J.V'_{DS(JFET)}} \qquad (6.21)$$

According to Equation (6.9), (6.14), (6.20) and Equation (6.21), $V_{GS(JFET)}$ can be derived as:

$$V_{GS(JFET)} = V_{PO} + \frac{V_{th(MOS)}+Vs}{2} - \frac{\sqrt{I}}{\sqrt{2\beta_M}} + \frac{\sqrt{\beta_M}}{2\beta_J.(-\sqrt{2I}+(V_{th(MOS)}+Vs-I.R_{drift})\sqrt{\beta_M})}.I - \frac{I.R_{drift}}{2} \qquad (6.22)$$

According to the circuit as shown in Figure 6.2(a), the following relationship can be found:

$$V_{GS(JFET)} = V_{DS(MOS)} \qquad (6.23)$$

In the end, with the Equations (6.13), (6.22) and (6.23), the I -V relationship of the SSCB in Stage 2 can be derived as:

$$V = \frac{V_{th(MOS)}+V_S}{2} - V_{PO} - \frac{\sqrt{I}}{\sqrt{2\beta_M}} - \frac{\sqrt{\beta_M}}{2\beta_J.(-\sqrt{2I}+(V_{th(MOS)}+Vs-I.R_{drift})\sqrt{\beta_M})}.I + \frac{I.R_{drift}}{2} \quad (6.24)$$

Stage 3: Both the p-MOSFET and the n-JFET enters into saturation regions

As shown in Figure 6.2(d), when the voltage across the SSCB continues to rise, the n-JFET is also driven into the saturation region.

For the p-MOSFET in the saturation region, Equation (6.20) is recalled as,

$$V_{DS(JFET)} = -\frac{\sqrt{2I}}{\sqrt{\beta_M}} + V_{th(MOS)} + Vs$$

For the n-JFET in the saturation region, the I-V relationship can be expressed as [10]:

$$I_{DS(JFET)} = \beta_J(V_{GS(JFET)} - V_{PO})^2 \quad (6.25)$$

With Equations (6.14), (6.23) and (6.25), $V_{DS(MOS)}$ can be obtained as

$$V_{DS(MOS)} = V_{PO} + \frac{\sqrt{I}}{\sqrt{\beta_J}} \quad (6.26)$$

In the end, according to Equations (6.13), (6.20) and (6.26), the I-V relationship of the SSCB in Stage 3 can be derived as:

$$V = V_{th(MOS)} + Vs - V_{PO} - \sqrt{I}(\frac{\sqrt{2}}{\sqrt{\beta_M}} + \frac{1}{\sqrt{\beta_J}}) \quad (6.27)$$

To sum up, the output characteristics of the SSCB during the operating process is listed as follows:

Stage 1

$$V = -V_{po} - \sqrt{{V_{po}}^2 - \frac{I}{\beta_J}} + \frac{I}{\beta_M\left(Vs + V_{th(MOS)} + V_{po} + \sqrt{{V_{po}}^2 - \frac{I}{\beta_J}} - I.R_{drift}\right)} + I.R_{drift}$$

Stage 2

$$V = \frac{V_{th(MOS)}+V_S}{2} - V_{PO} - \frac{\sqrt{I}}{\sqrt{2\beta_M}} - \frac{\sqrt{\beta_M}}{2\beta_J.(-\sqrt{2I}+(V_{th(MOS)}+Vs-I.R_{drift})\sqrt{\beta_M}))}.I + \frac{I.R_{drift}}{2}$$

Stage 3

$$V = V_{th(MOS)} + Vs - V_{PO} - \sqrt{I}(\frac{\sqrt{2}}{\sqrt{\beta_M}} + \frac{1}{\sqrt{\beta_J}})$$

6.6 Simulation Validation of the Proposed SSCB

1.2kV SiC JFET (UJ3N120035K3S)[21] from United SiC and 40V low-voltage P-MOSFET IXTH140P10T [22] from Infineon are selected for the proposed SSCB. Figure 6.3 shows the simulated both output characteristics and transfer characteristics of the SiC JFET while Figure 6.4 for the P- MOSFET. Based on these figures, some key parameters of both devices are extracted in Table 6.1.

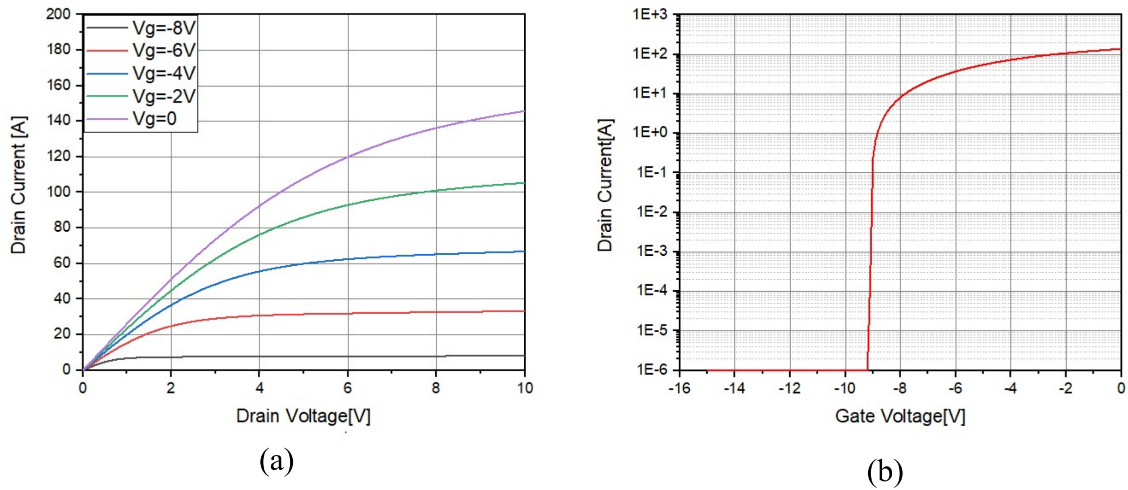


Figure 6.3 SiC JFET (a) Output characteristic (b) Transfer characteristic

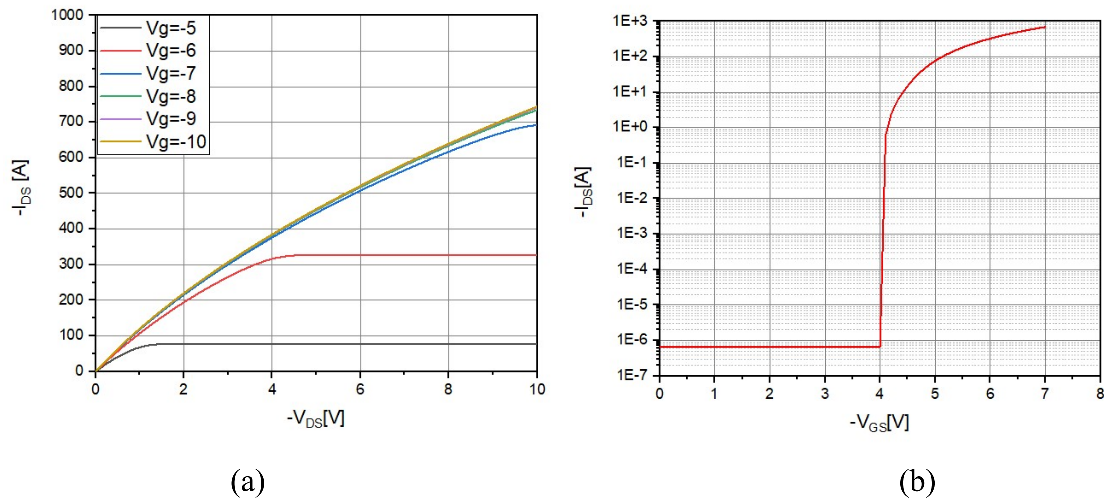


Figure 6.4 P-MOSFET (a) Output characteristic (b) Transfer characteristic

Table 6.2 Extracted device parameters

Components	**Parameter**	**Value**
P-MOSFET IXTH140P10T	Threshold voltage $V_{th(MOS)}$	-4 V
	Gain factor β_M	120
SiC JFET UJ3N120035K3S	Pinch-off voltage V_{PO}	-9.2 V
	Gain factor β_J	2.85
	Drift resistance R_{drift}	25mΩ
External voltage source	Vs	10V

Substituting the parameters in Table 6.1 into the output equations derived in previous section, the analytical expressions in three stages are obtained in the following.

Stage 1

$$V = 9.2 - \sqrt{84.6 - 0.35I} + 0.025I + \frac{0.008I}{\sqrt{84.6 - 0.35\ } - 0.025I - \ .2} \qquad 0 \leq V < 6$$

Stage 2

$$V = 12.2 - 0.065\sqrt{I} - \frac{1.9I}{65.7 - 0.22I - 1.41\sqrt{I}} + 0.0125I \qquad 6 \leq V < 10.4$$

Stage 3

$$V = 15.2 - 0.7\sqrt{I} \qquad 10.4 \leq V \leq 15.2$$

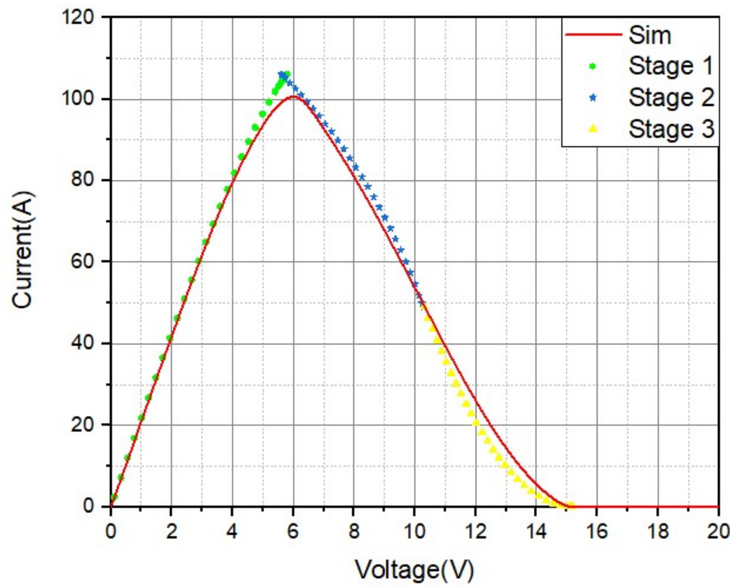


Figure 6.5 Comparison of simulated and calculated results

Meanwhile, the circuit constructed by the components in Table 6.2 are simulated by Pspice. Figure 6.5 compares the calculated results with the simulated results. It has demonstrated a reasonable matching despite the noticeable deviations. The discrepancies are mainly attributed to the inclusive parasitic impedance of commercial SPICE models as opposed to the model with some assumptions for the theoretical analysis. Furthermore, Figure 6.6 illustrates the junction temperature impacts on the tripping current. It displays the tripping current linearly deceases with the elevated temperature**.** Meanwhile, Figure 6.7 demonstrates the tripping current almost linearly increases with the external voltage. This feature implies that the tripping current is adjustable.

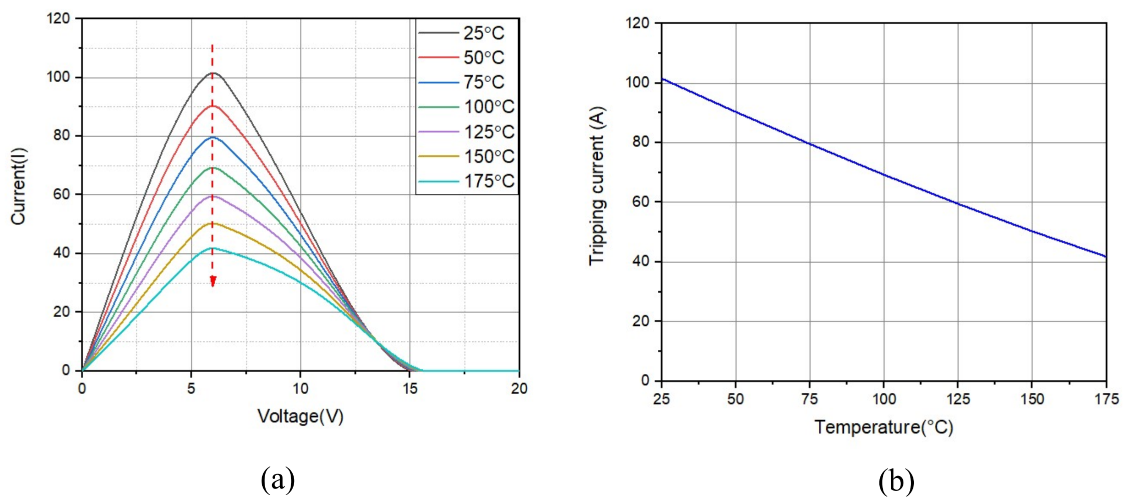


Figure 6.6 (a) I-V curves under different junction temperatures (b) Tripping current vs Junction temperature

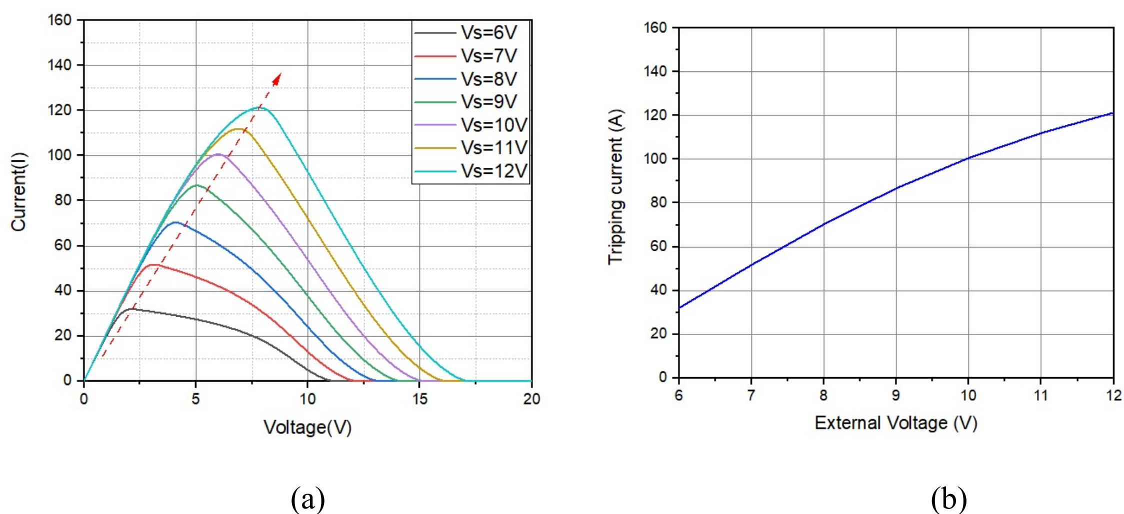


Figure 6.7 (a) I-V curves under external voltages (b) Tripping Current vs External Voltage

6.7 Analysis of voltage stress of the proposed SSCB

The low-voltage power p-MOSFET offers high-current capability and low conduction losses. However, in the off-state of the SSCB, the potential high voltage across the Si MOSFET might lead to the undesirable avalanche of the device. Therefore, it is essential to investigate the voltage distributions in either a static or a dynamic off-state of the SSCB before a preventive measure is taken.

6.7.1 Analysis of voltage distributions in a static off-state

In the static off-state of the SSCB, the DC voltage distributions mainly depends on the leakage current of off-state devices. The leakage current can be modelled by a large resistor (in MΩ range) in the equivalent circuit as shown in Figure 6.8(a). Figure 6.8(b) shows the re-arranged simplified equivalent circuit. According to the circuit, it can be concluded,

- The drain-gate terminals of both the JFET and the MOSFET withstand full supply DC voltage, which would damage the gate of MOSFET. To address this issue, a voltage clamping element like Zenner diode or TVS could be added across the drain-gate terminals of MOSFET to clamp the voltage.
- Voltage sharing between the MOSFET and the JFET can be calculated by the following equations:

$$V_{ds(JFET)} = \frac{R_{gs(MOS)}}{R_{gs(MOS)}+R_{ds(MOS)}//R_{gs(JFET)}} V_{DC} \tag{6.28}$$

$$V_{ds(MOS)} = \frac{R_{ds(MOS)}//R_{gs(JFET)}}{R_{gs(MOS)}+R_{ds(MOS)}//R_{gs(JFET)}} V_{DC} \tag{6.29}$$

$$\frac{V_{ds(MOS)}}{V_{ds(JFET)}} = \frac{R_{ds(MOS)}//R_{gs(JFET)}}{R_{gs(MOS)}} \tag{6.30}$$

Therefore, the high-voltage SiC JFET shares most supply voltage only if $R_{gs(MOS)}$ is far greater than $R_{ds(MOS)}//R_{gs(JFET)}$. In other words, the leakage current $I_{gs(MOS)}$ is far lower than the sum of $I_{ds(MOS)}$ and $I_{gs(JFET)}$.

According to the datasheet of SiC JFET UJ3N120035K3S[13] and P-MOSFET IXTH140P10T[14],

$I_{gs(JFET)} = 12\mu A$; $I_{gs(MOS)} = 100nA$; $I_{ds(MOS)} = 10\mu A$

Evidently, the condition $I_{gs(MOS)} \ll I_{ds(MOS)} + I_{gs(JFET)}$ has been well met. Thus, no measures need to be taken concerning this issue.

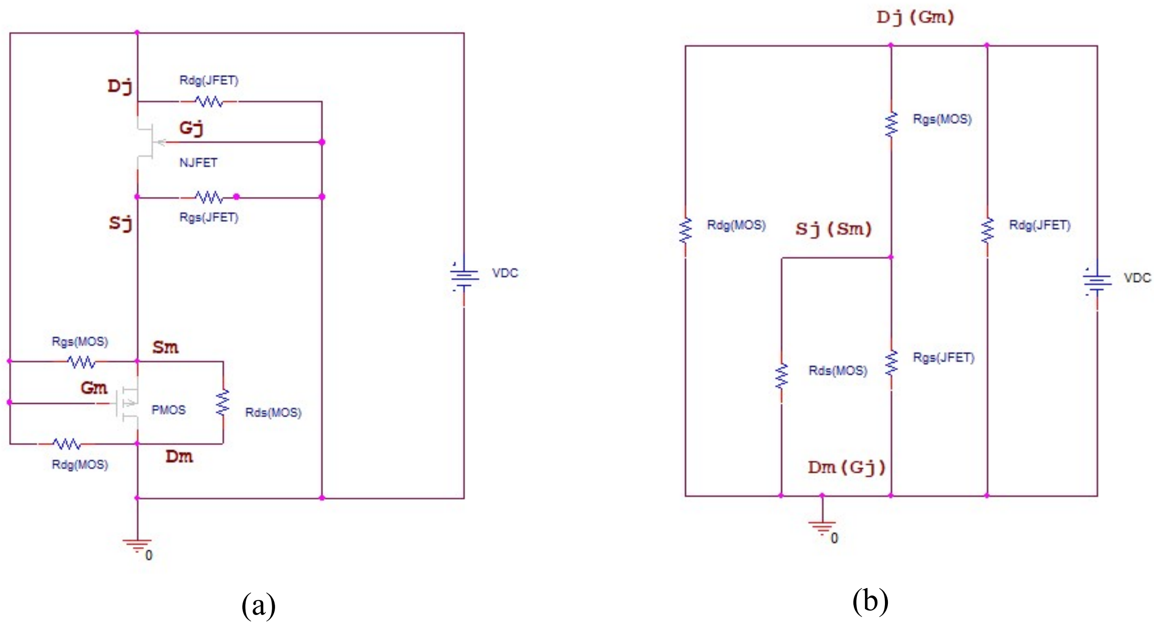


Figure 6.8 (a) Equivalent circuit of static off-state of the SSCB (b) Simplified equivalent circuit

6.7.2 Analysis of voltage distributions during turn-off transition of the SSCB

During the turn-off transient process of the SSCB, voltage distributions between the devices are essentially determined by the junction capacitances of the two devices. Figure 6.9(a) and (b) shows the equivalent circuit and simplified circuit respectively. As one can observe,

- The drain-gate terminals of both the JFET and the MOSFET withstand full DC voltage. This could lead to the damage of the low voltage MOSFET. To overcome this issue, the same measure with the static situation could be taken by adding a voltage clamping element like a Zenner diode or a TVS across drain-gate terminals of the MOSFE.
- Voltage sharing between the JFET and MOSFET can be obtained by the following equations:

$$V_{ds(JFET)} = \frac{C_{ds(MOS)}+C_{gs(JFET)}}{C_{gs(MOS)}+C_{ds(MOS)}+C_{gs(JFET)}} V_{DC} \tag{6.31}$$

$$V_{ds(MOS)} = \frac{C_{gs(MOS)}}{C_{gs(MOS)}+C_{ds(MOS)}+C_{gs(JFET)}} V_{DC} \tag{6.32}$$

$$\frac{V_{ds(MOS)}}{V_{ds(JFET)}} = \frac{C_{gs(MOS)}}{C_{ds(MOS)}+C_{gs(JFET)}} \qquad (6.33)$$

Similarly, to ensure the high-voltage SiC JFET withstand most voltages, the capacitance $C_{gs(MOS)}$ must be far smaller than the sum of $C_{ds(MOS)}$ and $C_{gs(JFET)}$.

According to the datasheet of SiC JFET UJ3N120035K3S[21] and P-MOSFET IXTH140P10T[22],

$$C_{gs(JFET)} = 2145pF$$

$$C_{gs(MOS)} = 321000pF$$

$$C_{ds(MOS)} = 1590pF$$

Apparently, the condition has not been met. To satisfy the condition, an external capacitor could be added to be in parallel with the MOSFET. Or a simple voltage clamping element is used.

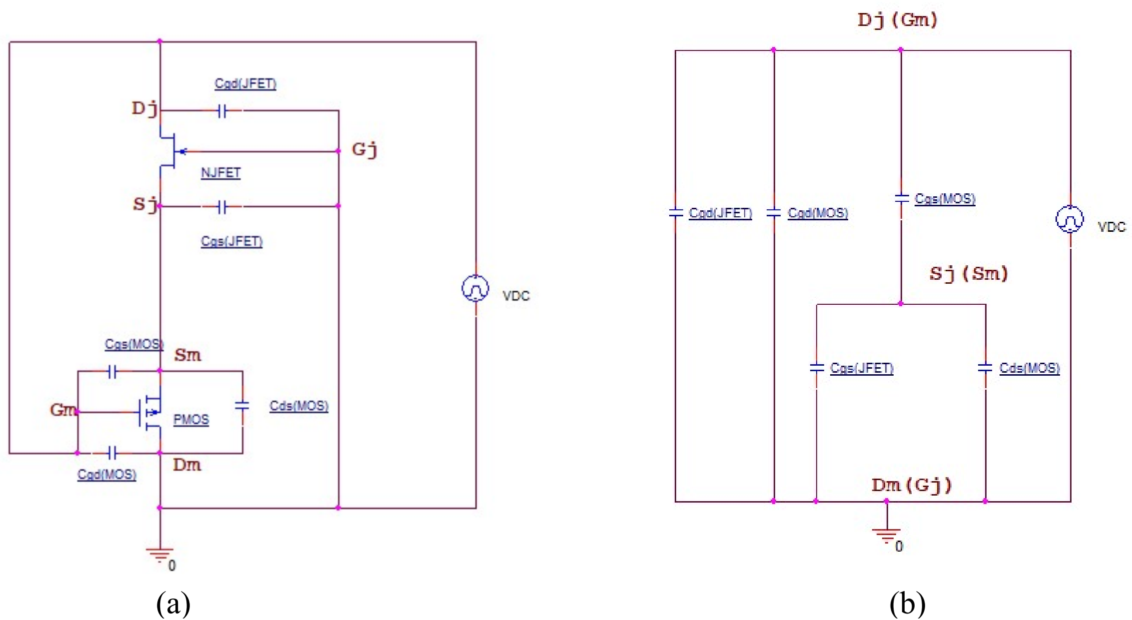
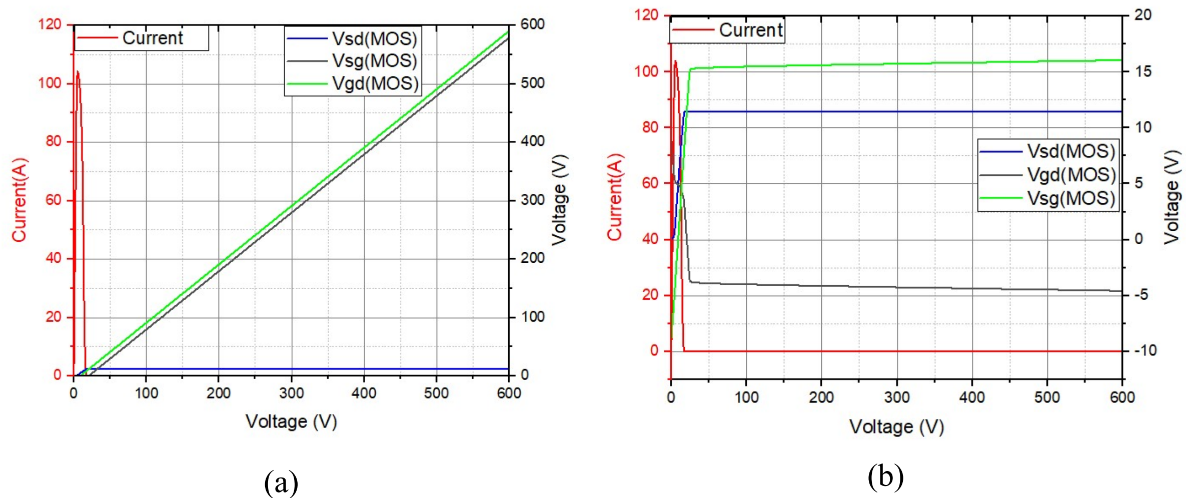


Figure 6.9 (a) Equivalent circuit of transient off-state of SSCB (b) Simplified circuit

6.7.3 Simulation validation

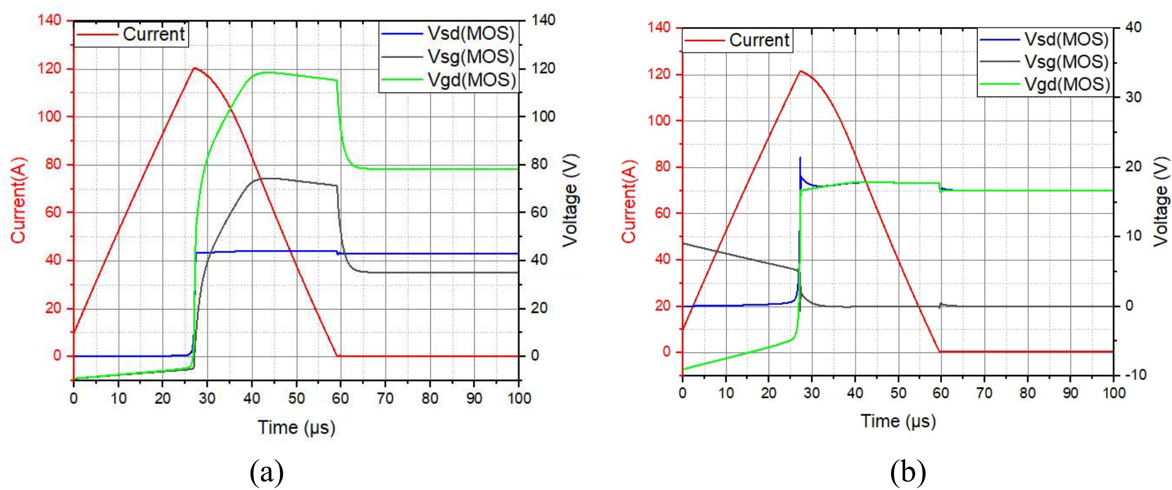
A back to back commercial Zener diodes N5352BRLG [23] is used for clamping the voltage. Figure 6.10(a) shows the simulated results of static voltages across the MOSFET terminals without the Zener diodes. As can be seen, the voltages across both the source-gate and drain-gate of the MOSFET reach the full supply voltage. In contrast, when a back-to-back Zener diode is added between gate and drain of the MOSFET, the voltages across the three terminals

of the MOSFET are effectively suppressed below 20V as shown in Figure 6.10(b). Meanwhile, Figure 6.11(a) and Figure 6.11(b) demonstrate the transient voltages across the MOSFET without and with the Zener diodes respectively. Similarly, without the Zener diode, the voltages across the gate-source and gate-drain exceed the maximum permitted value whereas with the Zener diode, both voltages are also limited within 20V. Therefore, the simulated results validate the correctness of the analysis and prove the effectiveness of the method of adding Zener diodes.



(a) (b)

Figure 6.10 (a) Static voltages across MOSFET terminals without the Zener diodes (b) Static voltages across MOSFET terminals with the Zener diodes



(a) (b)

Figure 6.11(a) Transient voltages across MOSFET terminals without the Zener diodes (b) Transient voltages across MOSFET terminals with the Zener diodes

6.8 Experiment Validation

6.8.1 Experimental setup

To conduct a short-circuit test, a dedicated test bench has been built as sketched in Figure 6.12. A high power IGBT acting as a short-circuit switch is in series with the proposed SSCB. The short-circuit duration is controlled by the pulse width of the IGBT gate voltage. The biased gate voltage for the P-MOSFET is provided by an external isolated voltage source. The inductor L_{DC} is changeable to emulate the system inductance between 10µH and 100µH. A 400V DC power supply source with a large output capacitor provides the high short-circuit current. The external voltages Vs are generated by the laboratory DC power supply unit through an isolated DC/DC converter. Figure 6.13 shows the hardware of this experimental setup.

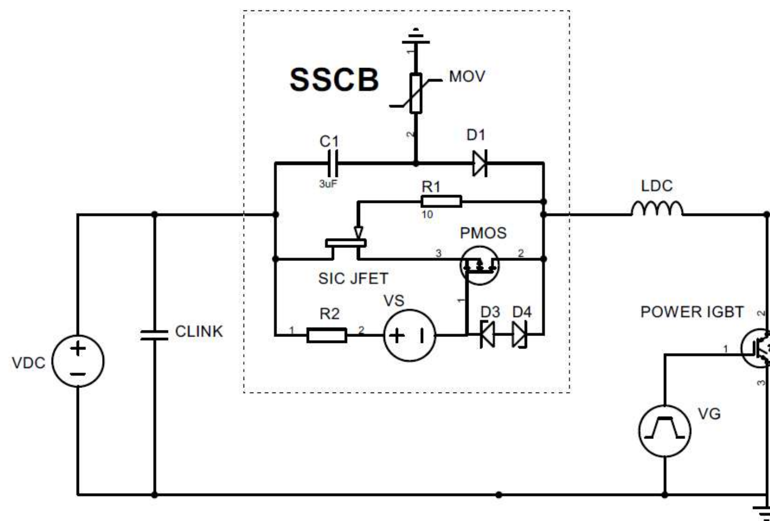


Figure 6.12 Schematic of the short-circuit test circuit

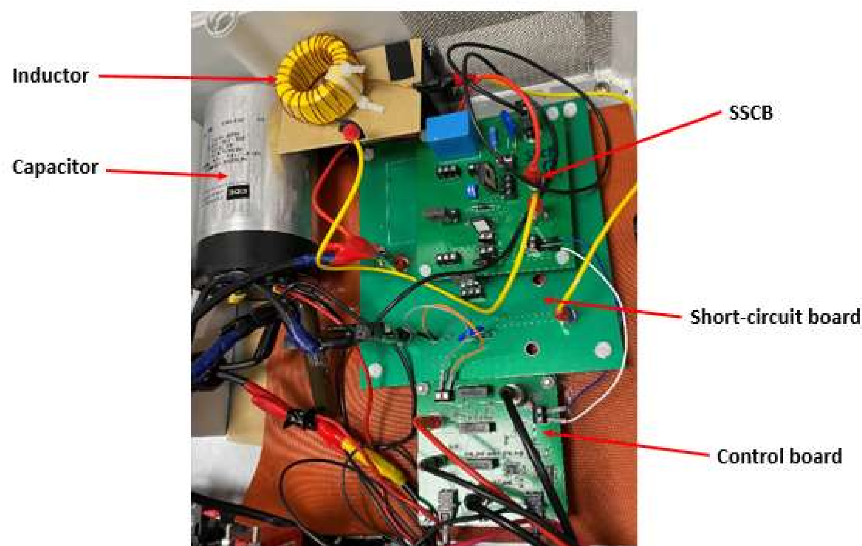


Figure 6.13 Hardware of short-circuit test

6.8.2 Main components of the test bench

As shown in Figure 6.13, the test bench consists of the following main components.

1) DC Power Supply

As shown in Figure 6.14, a 32 kW / 1000 VDC / 40A power supply equipment from TopCan Quadre [24] is used for suppling DC power. It is capable of sourcing up to 40A continuous current and 150A pulse current. Furthermore, it is integrated with the built-in fault protections such as overvoltage protection and overcurrent protection.

Figure 6.14 1000V DC power supply

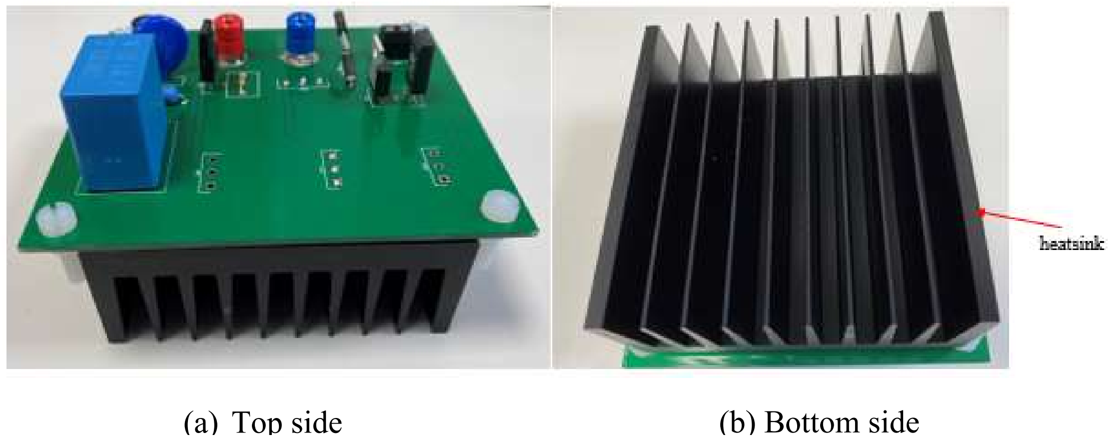
2) Enclosed safety box

When performing a short-circuit test, either high voltage or high current is dangerous to personal safety. Plus, some failed components might result in explosion and fire hazard. For the health and safety consideration, the test is carried out inside an enclosed box as shown in Figure 6.15. The box is equipped with an interlock switch. Whenever the box is opened, the DC supply voltage is disabled. Furthermore, a red emergency stop button is installed in the front of the box for emergently disconnecting the power supply.

Figure 6.15 enclosed test box

3) Hardware of the proposed SSCB

Figure 6.16 shows the hardware of the proposed SSCB with the heatsink while Figure 6.17 indicates the main components of the proposed SSCB without the heatsink.



(a) Top side (b) Bottom side

Figure 6.16 Pictures of the proposed SSCB

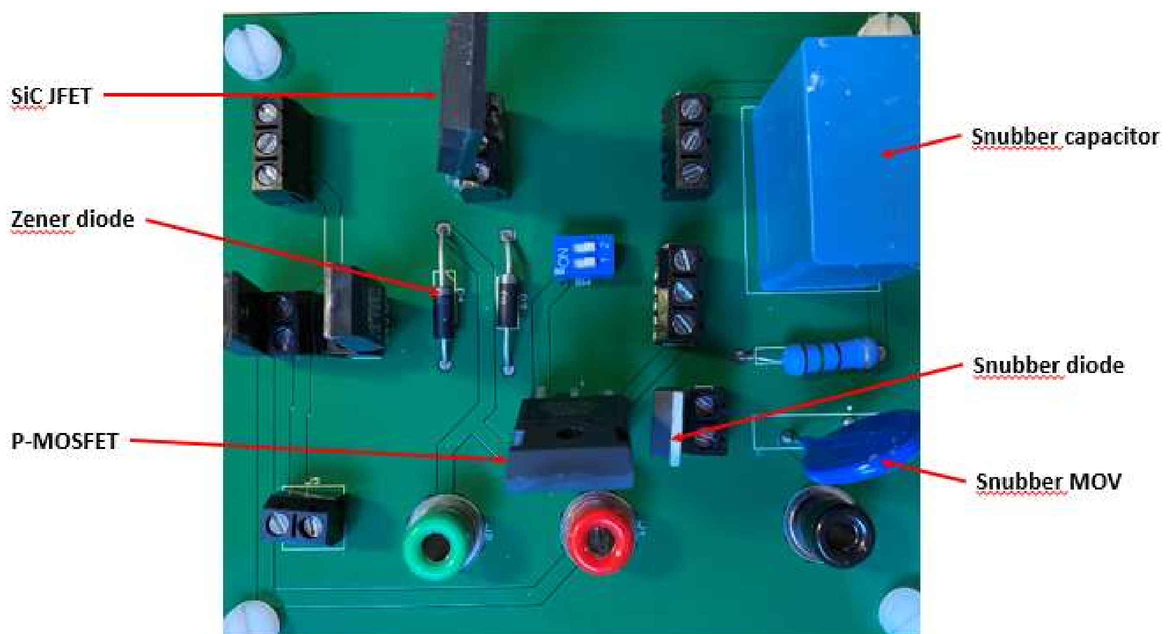


Figure 6.17 Main components on the SSCB board

4) Short-circuit board

Figure 6.18 shows the photo of the short-circuit board. It includes a large capacitor, a power IGBT device and an inductor.

Figure 6.18 Short-circuit board

5) Single-pulse gate-driving control board

The gate-driving control board is used for generating a single-pulse gate voltage to switch the power switch IGBT. Figure 6.19 shows the flow chart of the operating process. It starts with the pulse generator which outputs electrical pulse signals. The signals are passed to the optical transmitter where they are converted into optical signals. In the following, through the optical fibre cable, the optical signals are transmitted to the optical receiver where the optical signals are reversed back original electrical signals. Then, the electrical signals are filtered by the buffer chip before they input into the gate driving chip. Finally, the gate driving circuit outputs voltage pulses to drive the power IGBT. Figure 6.20 shows the photo of the control circuit board. It consists of four parts as presented in the following.

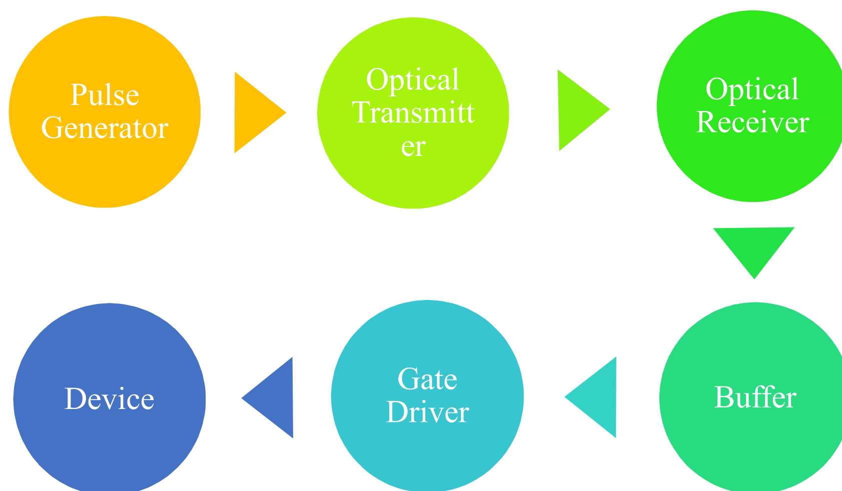


Figure 6.19 Flow chart of gate driving circuit

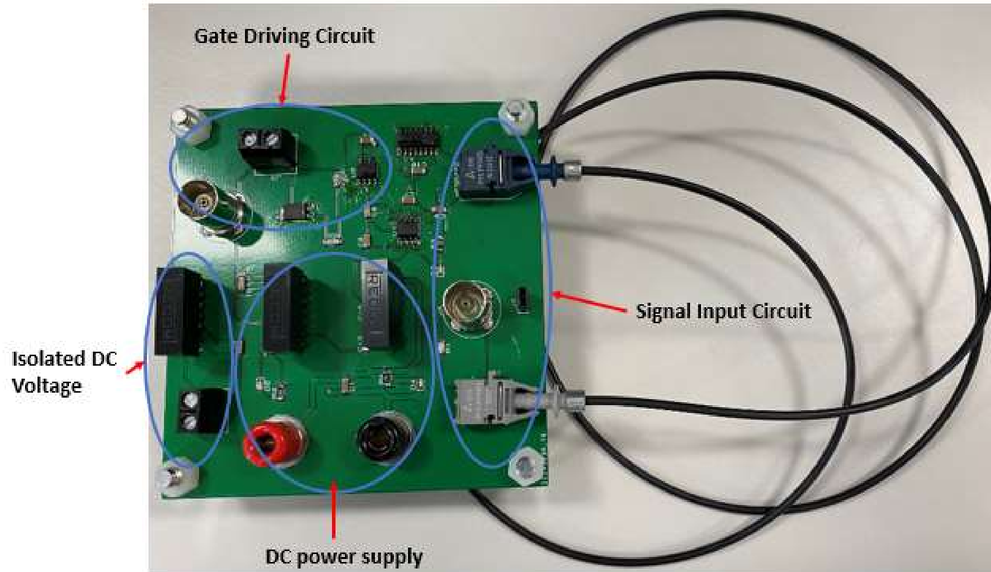


Figure 6.20 Gate driving circuit board

Part 1: DC power supply

The power is supplied through the isolated 24V/15V DC/DC converters and a 5V DC regulator. Filtering capacitors are used for both input and output sides of the DC/DC converters.

Part 2: Signal processing

The optical signals offer the advantages of voltage isolation and EMI immunity. This part includes an optical transmitter, an optical receiver and an optical cable.

Part 3: Gate driving circuit

The gate driver chip IXDN69SIA from IXYS [25] can provide up to 35V output voltage and source up to 9A peak current.

Part 4: Isolated DC power output

A single isolated DC/DC converter is used for providing the external voltage to the SSCB.

6) Measurement Instruments

As shown in Figure 6.21, a voltage differential probe is used to measure high DC voltages while currents are measured by the Rogowski coil probe which offers the flexibility to adapt to the circuit [26]. Measured waveforms are displayed on a four-channel 1 GHz digital oscilloscope.

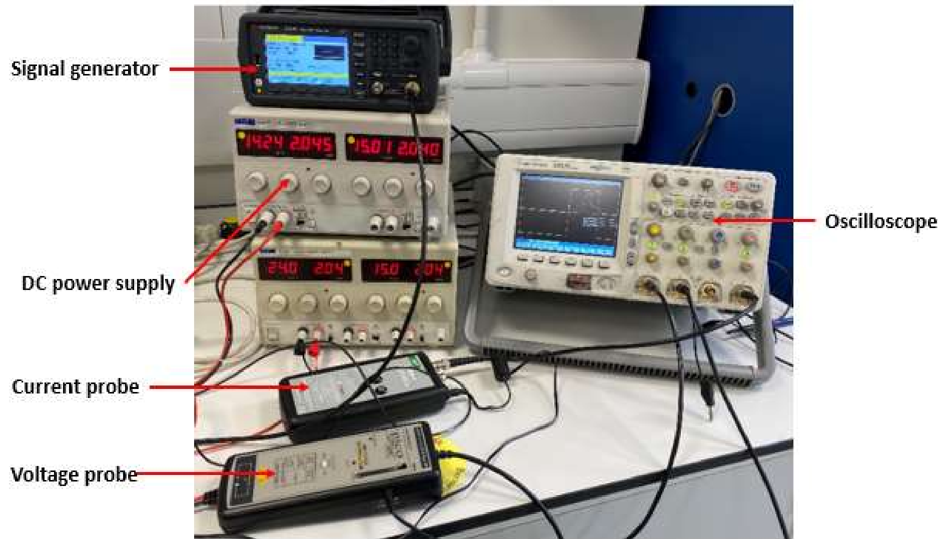


Figure 6.21 Measurement instruments

6.8.3 Experiment Results

Figure 6.22 shows the short-circuit experimental results under the test condition: L_{DC}=10μH, V_{DC}=100V and external voltage Vs=5.4V. As it can be seen, the SSCB trips at 83A with a response time around 20μs. By changing the inductance and supply voltage to: L_{DC}=30μH, V_{DC}=250V while maintaining the external voltage Vs=5.4V, the SSCB trips at 82A with a response time around 25μs as shown in Figure 6.23. Increasing the external voltage from 5.4V to 7.2V while maintaining other parameters, the SSCB trips at 123A with a response time around 28 μs as shown in Figure 6.24. According to the results under the three test conditions, one can conclude that the tripping current level depends on the external gate biased voltage while the response time is affected by both the line inductance and DC supply voltage. The higher the line inductance and the DC supply voltage is, the longer the response time is.

Figure 6.25 demonstrates the experimental results under the design conditions: supply voltage V_{DC}=400V, inductance L_{DC}=100μH and the external supply voltage Vs=6.2V. As can be observed, the SSCB trips at 104A with a response time around 53 μs and maximum over voltage 710V. All the parameters meet the design criteria as listed in Table 4.2. Therefore, the experiment results validate the correctness of the design of the proposed SSCB.

Furthermore, the voltage distributions are measured after the SSCB switches off. Figure 6.26(a) and (b) displays the voltages across the SiC JFET and the P-MOSFET respectively. Evidently, the SiC JFET shares most of the high voltages in either static or dynamic off-state of the SSCB. Meanwhile, the gate voltages of both SiC JFET and P-MOSFET devices are

restricted below the 20V. Therefore, the result verifies the effectiveness of the added back-to-back diodes.

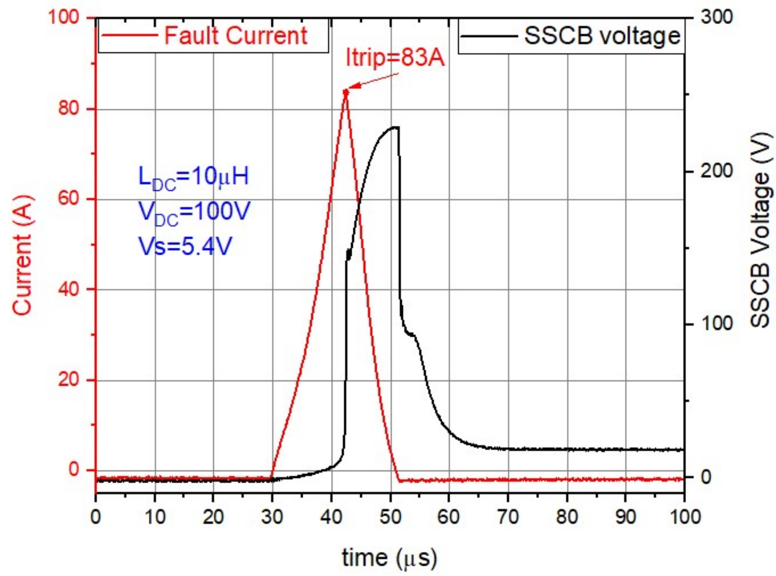


Figure 6.22: Short-circuit test under the condition:
L_{DC}=10µH, V_{DC}=100V and external voltage Vs=5.4V

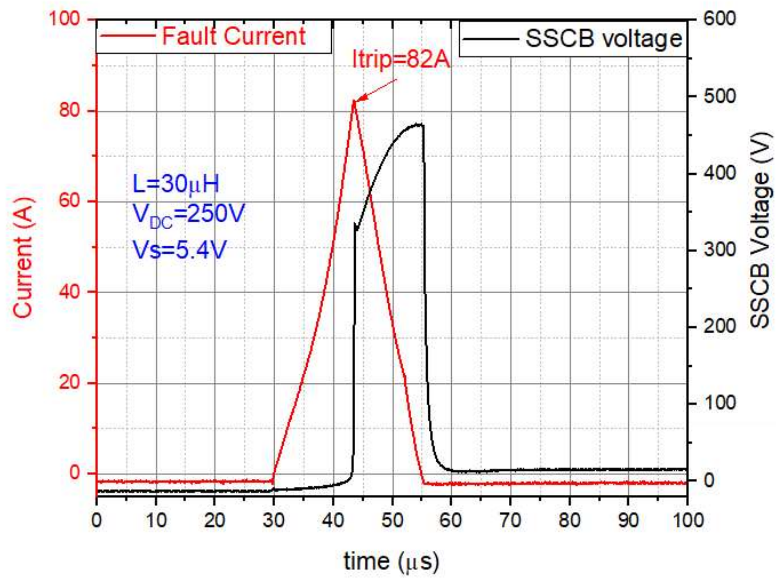


Figure 6.23 Short-circuit test under the condition:
LDC=30µH, VDC=250V and external voltage Vs=5.4V

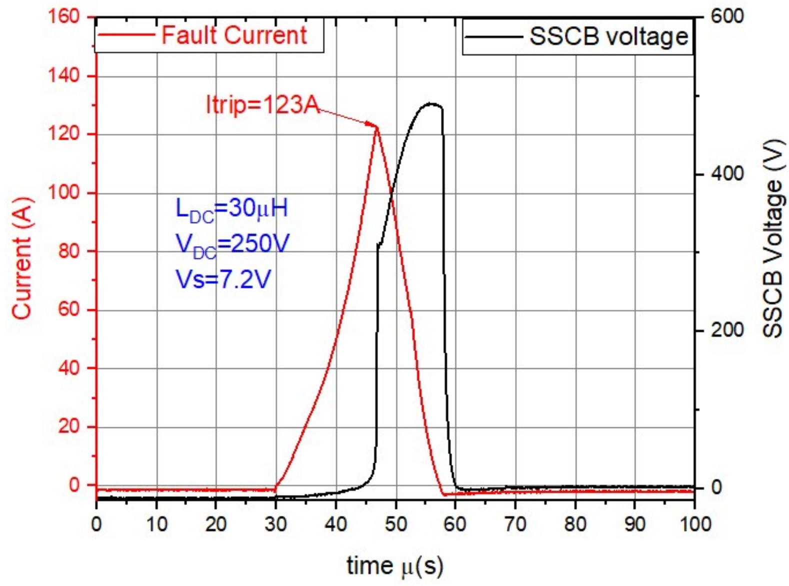


Figure 6.24 Short-circuit test under the condition: LDC=30μH, VDC=250V and external voltage Vs=7.2V

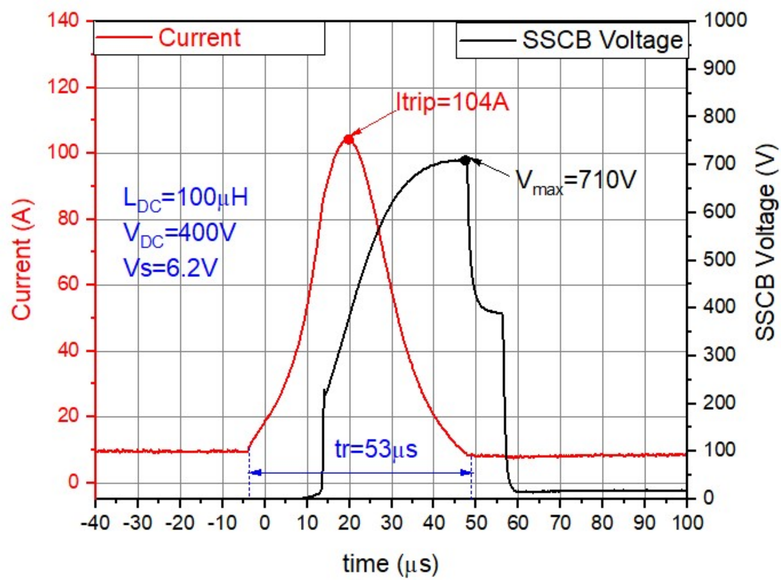
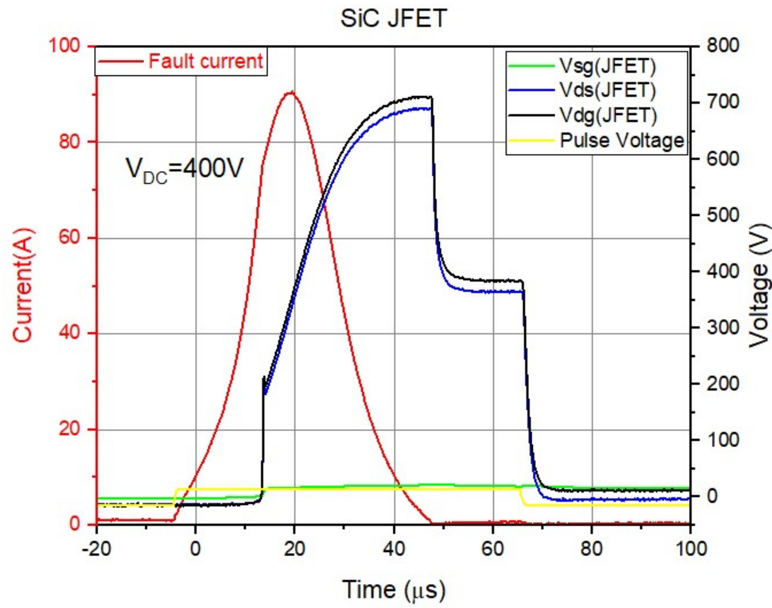
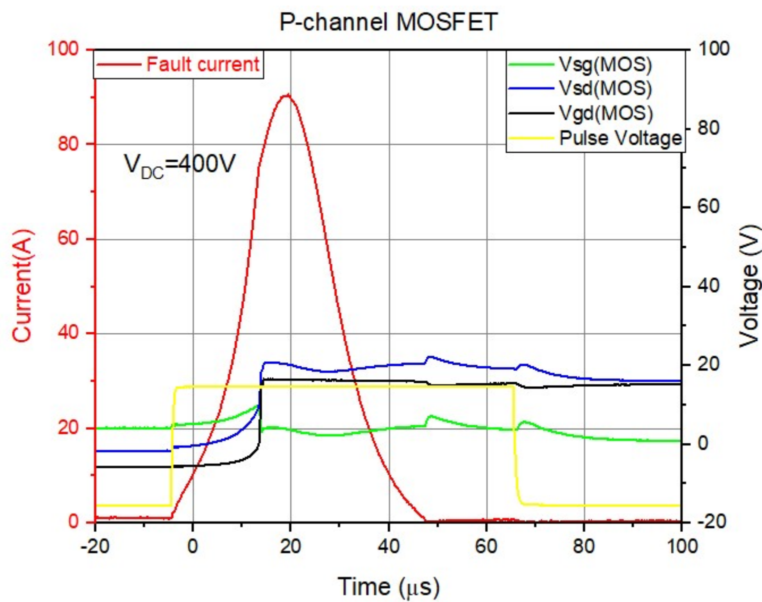


Figure 6.25 Short-circuit test under the condition: LDC=100μH, VDC=400V and external voltage Vs=6.2V



(a) Voltages across SiC JFET



(b) Voltages across p-channel MOSFET

Figure 6.26 Voltage distribution after turn-off of the SSCB

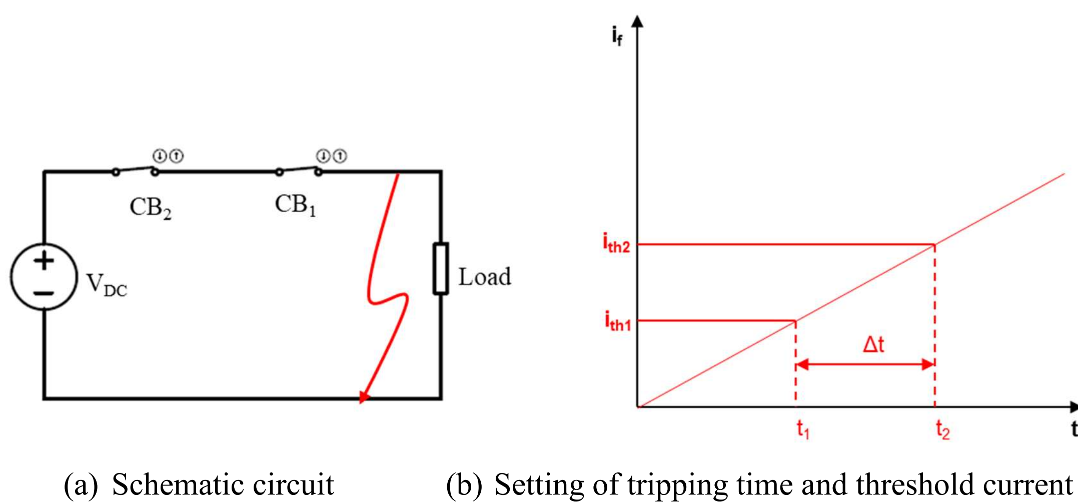
6.9 Protection Coordination

6.9.1 Introduction

For a complete system protection, the protective devices in the system should coordinate with each other to provide protection selectivity (fault discrimination). In other words, only the protective device closest to the fault location should act to isolate the region where the fault happened so that other healthy regions can continue to operate [27]. Realization of fault

discrimination in a DC system proves to be very challenging issue since almost same high magnitude and high derivatives of fault currents simultaneously flow through both upstream and downstream SSCBs. Consequently, the response speed of downstream SSCB is required to act faster than the upstream SSCBs[7][28]. At present, communication-based coordination methods are commonly adopted to fulfil the protection selectivity. However, such methods heavily relying on the advanced and fast communication techniques which are complicated and costly[29].

As shown in Figure 6.27, the overcurrent protection coordination between upstream CB_2 and downstream CB_1 are usually achieved by setting different threshold current levels and tripping time[7]. For example, the threshold current i_{th1} of the downstream CB_1 is set lower than i_{th2} of the upstream CB_2 and therefore the tripping time t_1 of CB_1 is shorter than time t_2 of CB_2. When a short-circuit fault occurs in the downstream, the fault current rises to first reach the threshold of CB_1 and then CB_1 is triggered to isolate the fault before the fault current reach the i_{th2} of CB_2. As a result, the upstream CBs remains on. However, if the turn-off delay time of CB_1 is longer than the tripping time difference of the two circuit breakers $\Delta t = t2 - t1$, the upstream CB_2 is also be triggered, causing the false trip. It can frequently occur in a DC system due to the high derivative of DC fault currents. As shown in Figure 6.28(a), the high derivative current (blue line) results in the shorter tripping time difference Δt than the low derivative current (red line) When the time difference is shorter than the delay time of CB_1, the CB_2 is also triggered and thereby losing the protection selectivity. Practically, to avoid the false trip of CB_2, an interlock signal is sent to the CB_2 to temporarily freeze the CB_2 once the CB_1 is activated [30].



(a) Schematic circuit (b) Setting of tripping time and threshold current

Figure 6.27 Overcurrent protection coordination between SSCBs

The proposed SSCB can overcome this issue due to its current-limiting function. The fault current in downstream is always limited to the tripping current level of downstream CB_1. As shown in Figure 6.28(b), even if the tripping time difference between the downstream and upstream SSCBs is shorter than the delay time of CB_1 (blue line), the upstream CB_2 would not be falsely triggered since the fault current will not reaches its tripping current level.

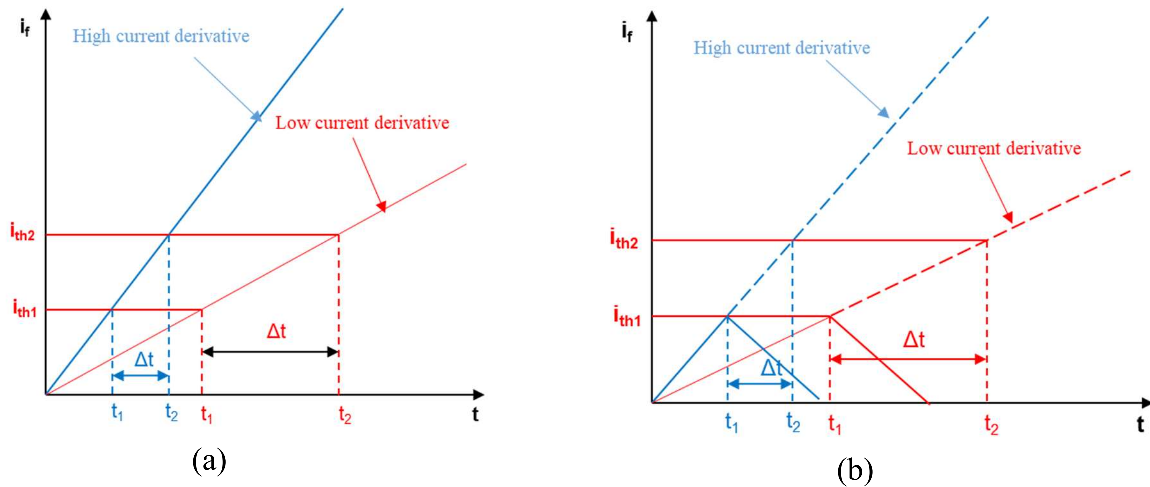


Figure 6.28 Protection coordination (a) Conventional SSCBs (b) The proposed SSCBs

6.9.2 Simulation validation

As mentioned in Chapter 4, the upstream SSCB can be designed by paralleling two SiC JFEFs. This method could not only increase the tripping current level but also improve the power capability of the upstream SSCB. Alternatively, the tripping current of upstream SSCB can be raised by simply increasing the external gate biased voltage. Referred to Table 4.2, the technical specifications of both upstream and downstream SSCBs are given in Table 6.3. Figure 6.29 shows the simulated output characteristics of upstream SSCB with two SiC JFETs in parallel in both static and transient conditions.

Table 6.3 technical requirement specification of both upstream and downstream SSCB

Parameter	**Upstream SSCB**	**Downstream SSCB**
Supply voltage (110%)	440V DC	440V DC
Rated current	20A	10A
Response time	<110μs	<55 μs
Tripping current	200A	100A
Prospective fault current	>1kA	>1kA
System inductance	10-100μH	10-100 μH
Breakdown voltage	>1000V	>1000V
Efficiency	>99.7%	>99.7%

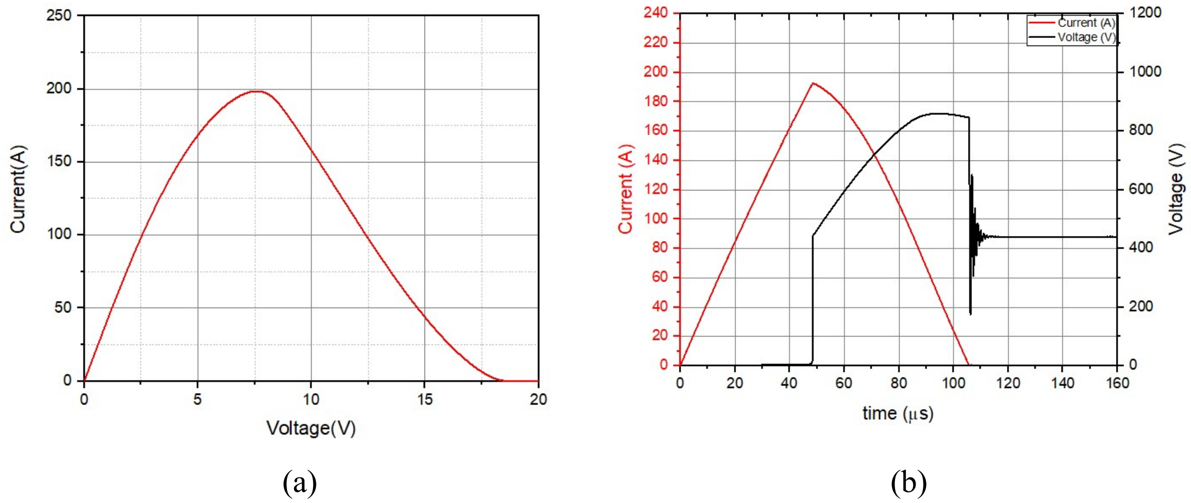


Figure 6.29 Output characteristic of upstream SSCB (a) Static output (b) Transient output

Figure 6.30 shows a simple scenario where the two load branches are supplied power through the downstream SSCB1 and SSCB2 respectively and the upstream SSCB acts as a backup protection for both SSCB1 and SSCB2. If a short-circuit fault occurs in the load branch 1, with proper protection coordination among the three SSCBs, only SSCB1 should act to isolate the fault while SSCB2 and SSCB remain on. As a result, Load 2 continues to be supplied power without the disruption. Figure 6.31 shows the simulated results. When the fault at Load 1 occurs at 10μs, the fault current surges to the tripping current level of SSCB1. Then, SSCB1 starts turning off and completely cut off the fault current at around 65μs. During this process, the Load 2 continue to operate without disruption and the upstream SSCB stays on although it experiences the same fault current of SSCB1. As a result, the protection coordination between the three SSCBs are achieved.

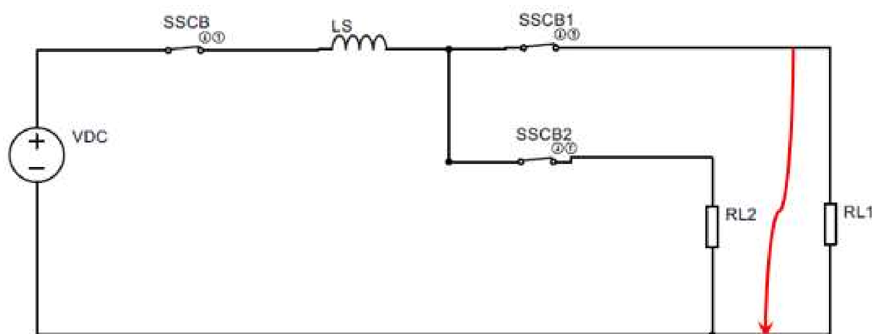


Figure 6.30 Overcurrent protection coordination between SSCBs

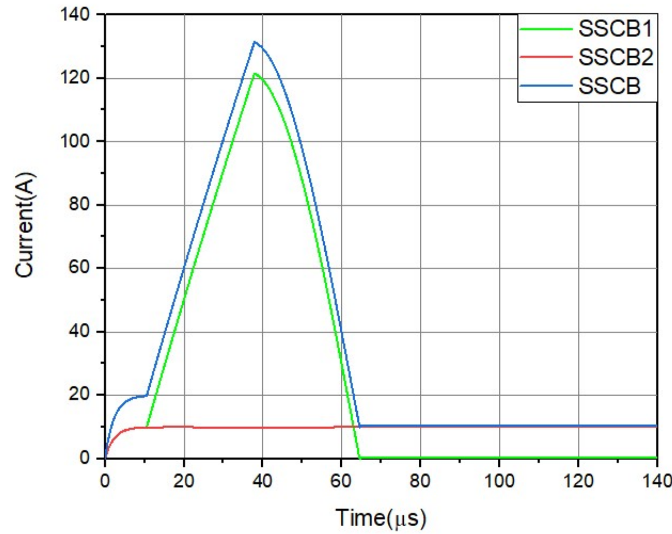


Figure 6.31 Simulated overcurrent protection coordination between SSCBs

6.9.3 Experimental validation

The upstream SSCB for the experiment is built of the same of the downstream SSCB instead of two SiC JFETs in parallel for the simulation. However, the tripping current of upstream SSCB are set higher than the downstream SSCB by providing a higher external gate biased voltage. As shown in Figure 6.32, the tripping currents of downstream and upstream SSCB are set at 83A and 128A respectively. Figure 6.33 shows the hardware of this experimental setup where the two SSCBs are in series under the test condition: V_{DC}=100V and L_{DC}=10μH. The experimental results are shown in Figure 6.34. It can be observed that during the short-circuit period, only the downstream SSCB trips at 82A while the upstream SSCB remains on as evidenced of the voltages across the two SSCBs. Hence, the protection coordination between the two SSCBs is achieved.

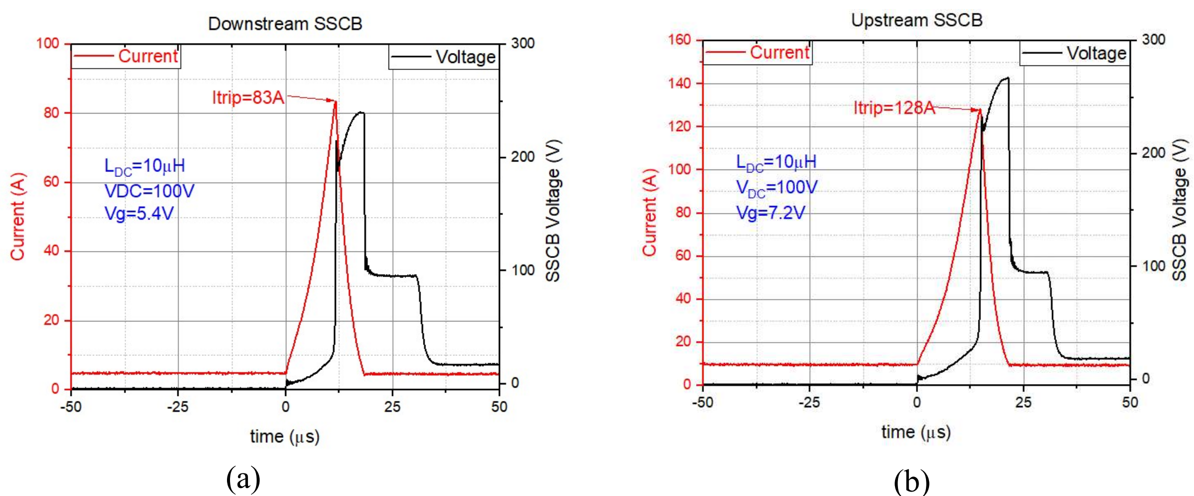


Figure 6.32 Tripping currents of SSCBs (a) Downstream SSCB (b) Upstream SSCB

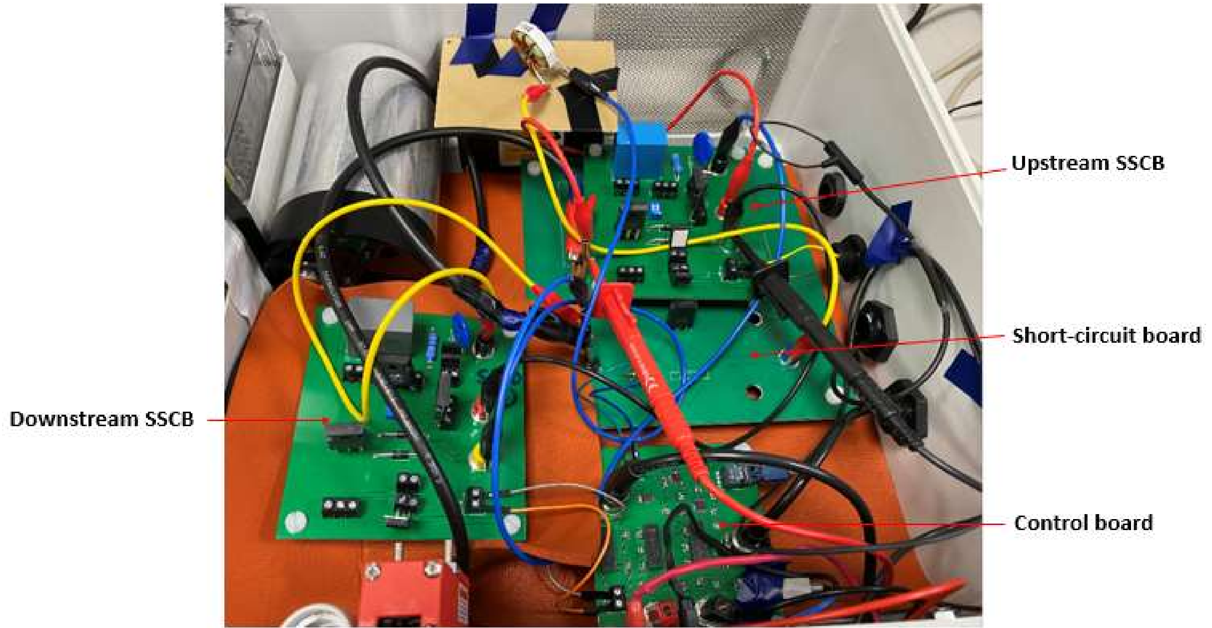


Figure 6.33 Hardware of overcurrent protection coordination experimental setup

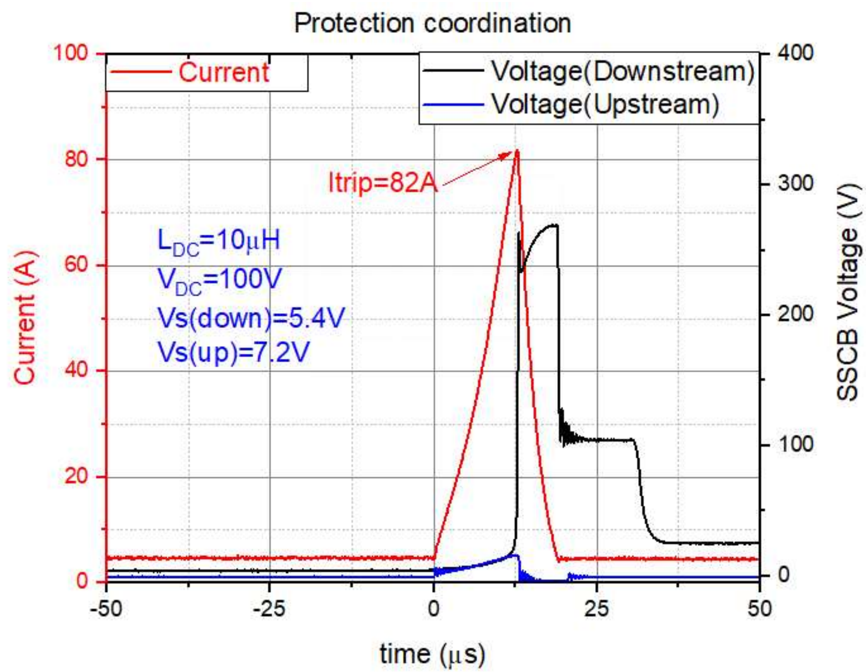


Figure 6.34 Protection coordination between two SSCBs

6.10 Inrush Current Issue

As discussed before, DC systems are highly capacitive. Figure 6.35 shows a simplified schematic DC system. A large DC power output capacitor bank C_{LINK} is deployed to maintain output DC voltage level. Additionally, a capacitor Cx as an electromagnetic interference (EMI) filter is regularly placed in front of DC loads. When the load starts connecting to the DC network, an high inrush current (several times of nominal load current) at the instant of connection, would flow through the load and the system [31]. The inrush current can result in false tripping of the SSCB.

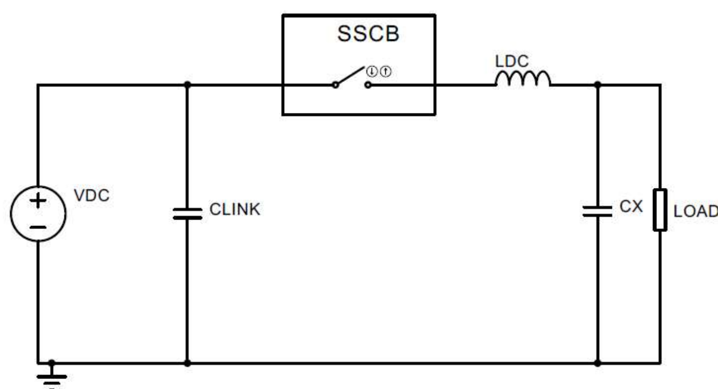


Figure 6.35 Schematic of a DC system

To overcome this issue, two-level tripping current solution is proposed to avoid the false tripping at the start-up of load connection. As shown in Figure 6.36(a), the SSCB with tripping current of 50A trips when experiencing the inrush current whereas the SSCB with 120A tripping current is immune to the inrush current. Therefore, at the start-up of load connections, the tripping current of SSCB can be raised to a higher level by temporarily increasing the external voltage and then returned back to the normal level when the load is connected. Figure 6.36(b) demonstrates the simulated results of the two-level tripping current solution. It is evident that the SSCB maintains on-state when a large transient inrush is produced during the process of load start-up.

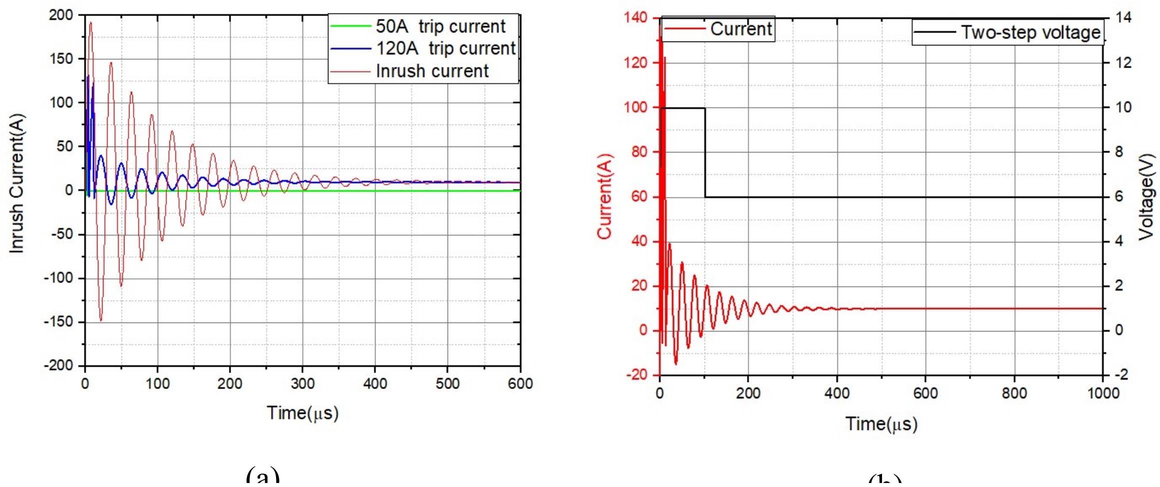


Figure 6.36 Two-step solution (a) SSCBs with different tripping current (b) Load start-up

6.11 SSCB Reset and Fail-Safe

After the turn-off, the SSCB will not automatically reset to the on-state until the applied voltage across the SSCB falls below the threshold voltage of the p-MOSFET. However, the reset of the SSCB can be realized by switching off the mechanical switch which is mandatary requirement in the industry as mentioned in Chapter 2. As shown in Figure 6.37, the mechanical switch can be associated with the SSCB. Once the SSCB is off, the mechanical switch is also switched off either manually or remotely.

In addition, the proposed SSCB is fail-save since the normally-off p-MOSFET automatically turns off and therefore the SSCB is off in the event of losing the external power. Therefore, it causes no harm to other equipment in the system.

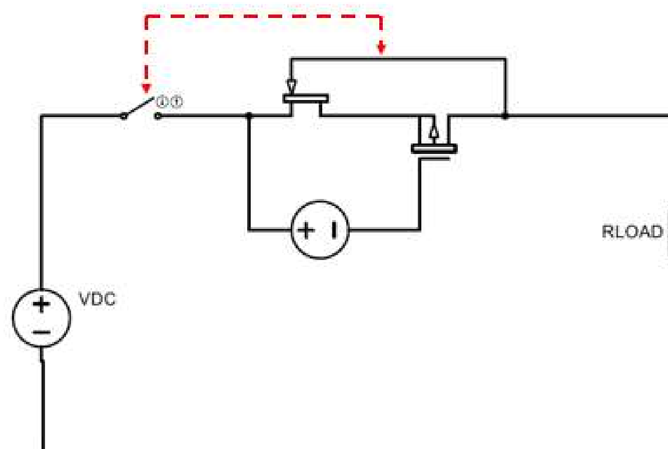


Figure 6.37 SSCB reset and fail-safe

6.12 Conclusions

This chapter has presented the development of an ultrafast SSCB for short-circuit protection applied for 400V DC systems. The analytical expressions of its operating principle have been provided and verified by the simulation. A prototype SSCB has been built and evaluated in a DC power system. The experiment results show the proposed SSCB is capable of interrupting 100A current within 55 μs while the overvoltage is suppressed below 1000V. Furthermore, protection coordination between upstream and downstream SSCBs have been demonstrated. Finally, both the inrush current issue and the SSCB reset issue have been addressed.

6.13 References

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Chapter 7 Overload and Over Temperature Protection

7.1 Introduction

Similar to the conventional EMCBs, apart from short-circuit protection, SSCBs are also required to provide overload protection. Hence, the tripping time-current characteristics of a circuit breaker should include two regions serving for short-circuit protection and overload protection respectively. The time-current tripping curve for overload protection is governed by the current square time (I^2t) of the power semiconductor devices which reflects the thermal capability of the power semiconductor device. Meanwhile, the overload protection also serves for SSCBs' self-thermal protection since semiconductor devices are the most vulnerable elements in a DC system[1]. Furthermore, it is well known that one of the most significant factors to impact the performance and reliability of a semiconductor device is its junction temperature. Therefore, a real-time monitoring device junction temperature during the normal operation can provide an extra reliability assurance for SSCBs and can act as a backup of overload protection.

This chapter starts with the design of an overload protection time-current tripping curve followed by the design of over temperature protection. Online measurement methods of device junction temperature are reviewed, and the choice of temperature-sensitive electrical parameters is discussed. Finally, a practical circuit for real-time junction temperature measurement is introduced and experimentally verified.

7.2 Overcurrent Protection

7.2.1 Comparison of time-current tripping curves of SSCBs and EMCBs

Figure 7.1 demonstrates the typical time-current tripping curves of SSCBs and EMCBs. The curve is divided into three regions described in the following.

Short-circuit protection region

This region serves short-circuit protection. It requires the circuit breaker to interrupt the current instantly when the fault current exceeds the pre-set level, around 5-10 times of the rated current. As it can be seen, SSCBs are able to interrupt the short-circuit current within the range of hundreds of microseconds as opposed to tens of milliseconds of EMCBs. Since most semiconductor devices can turn off within several microseconds, the response time of a SSCB is mainly constrained by the speed of current sensing and communication.

Overload protection region

This region is designed for the overload protection. The overload current is commonly set between 1- 5 times rated current. As it can be seen, for a same overload current, SSCBs have at least two orders lower endurance time than the counterpart EMCBs due to the limited thermal capability of semiconductor devices in SSCBs. Therefore, the region mainly serves for self-thermal protection of SSCBs. The inverse time-current curve of SSCBs is governed by the device thermal capability, represented by the value of I^2t [2]. The higher the current is, the shorter the time will be. The maximum current is determined by the Safe Operating Area (SOA) of the semiconductor device specified by the manufacturer [3].

Rated current region

The region defines the maximum allowed continuous current of circuit breakers. For a SSCB, when a steady thermal equilibrium is reached, heat generated from the SSCB equals heat dissipated to the ambient environment by the SSCB. Under this thermal equilibrium condition, the junction temperature of power devices must be kept below the temperature limit specified by the manufacturers. Therefore, the rated current largely depends on the cooling system of SSCBs.

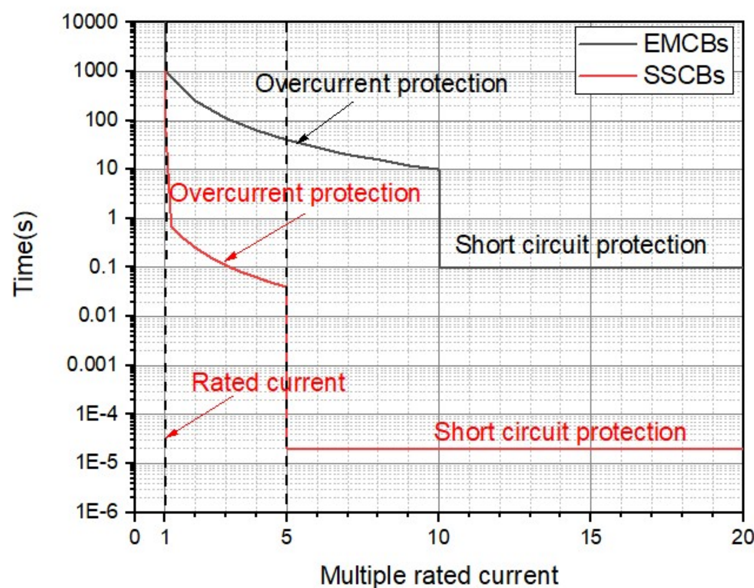


Figure 7.1 Typical trip curves of SSCBs and EMCBs

7.2.2 Design of I^2t for the proposed SSCB

The I^2t concept is used for dealing with overheating problems as a result of electrical current flowing through conductors in electric circuits. During the normal operation condition, the

SSCB is essentially a temperature-dependent resistor which is heated up by the current. For every current, there is a corresponding sustaining time before the junction temperature of the semiconductor device reaches its limit. During a transient event of less than one second, the thermal system can be deemed as an adiabatic environment where the heat in the system does not exchange with outside the system[2]. Since the duration of overload current for SSCB applications is usually less than one second, the device can be considered an adiabatic system where the heat generated by the device is dissipated by itself.

Hence, In an adiabatic system, the temperature rise ΔT for a conductor can be expressed as[2]:

$$I^2.R.t = C_w.m.\Delta T \tag{7.1}$$

where R is the resistance, C_w is the specific heat of the conductor material, [J/°C·kg] and m is the mass of the conductor [kg].

The mass of a square shape conductor can be expressed as:

$$m = \rho.L.S \tag{7.2}$$

Where ρ is the mass density of the conductor material [Kg/mm^3], L is the thickness of the conductor [mm], S is the area of the conductor [mm^2].

With Equations 7.1 and 7.2, the I^2t for a conductor is obtained as:

$$I^2t = \frac{C_w.\rho.L.S.\Delta T}{R} \tag{7.3}$$

As presented in Chapter 4, the temperature-dependent on-resistance $R_{on(T)}$ of 1.2kV SiC JFET UJ3N120035K3S can be fitted to a quadratic equation below:

$$R_{on(T)} = R_{on(25)}.[0.906 + 2.27 \times 10^{-3}T + 2.79 \times 10^{-5}T^2]$$

As shown in Figure 7.2, the die size of 35mΩ UJ3N120035K3S is provided by the supplier[4].

$S=9.42mm^2$ and L=150μm

Thus, substituting the physical parameters of 4H SiC material, C_w=690 J/°C·kg, ρ =3.211e-6 kg/mm^3[3], die size parameters and $R_{on(25°C)}$=35 mΩ into Equation 7.3, the value of $I^2\Delta t$ is derived as

$$I^2\Delta t = \frac{\Delta T}{10.11+2.52\times10^{-2}T+3.11\times10^{-4}T^2} \tag{7.4}$$

Integrating both sides, the value of I^2t can be obtained as,

$$I^2t = 18.3(\tan^{-1}\frac{5.1\times10^{-4}T_{max}+2.07\times10^{-2}}{8.95\times10^{-2}} - \tan^{-1}\frac{5.1\times10^{-4}T_{min}+2.07\times10^{-2}}{8.95\times10^{-2}}) \quad (7.5)$$

As discussed in Chapter 4, during a transient event, the junction temperature of the SiC JFET device can exceed 250°C. During the normal operation, the junction temperature of the proposed SSCB is designed to be less than 100°C. Therefore, given the maximum permitted junction temperature 250°C and minimum junction temperature 100°C during the transient period, the value of I^2t is calculated as 6.43 according to Equation 7.5.

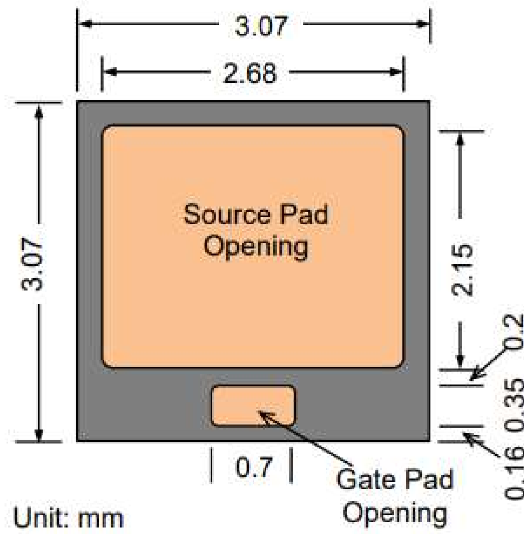


Figure 7.2 Die Size of UJ3N120035K3S [4]

Maximum allowed overload current

A semiconductor device should always operate within its safe operating area (SOA). Figure 7.3 shows the SOA curves of SiC JFET (UJ3N120035K3S) extracted from the datasheet[5]. It is defined by four distinct limit lines described respectively in the following[6].

1) Line 1: Voltage limit line

The line is defined by the device breakdown voltage. For this device, the breakdown voltage is 1200V at 25°C.

2) Line 2: Power limit line

This line represents the maximum power handling capability of the device, defined by

$$I_{DS} = \frac{\Delta T_{max}}{Z_{thjC} \cdot V_{DS}} \quad (7.6)$$

where Z_{thjC} is transient thermal impedance and ΔT_{max} is the maximum allowable temperature rise.

Since the transient thermal impedance varies with the pulsed width of time period, several lines with different pulse width are provided. The DC line is applied for this research.

3) Line 3: Current limit line

This line defines the maximum pulsed current, which is limited by the device maximum junction temperature. Theoretically, SiC semiconductors are capable of operating beyond 600°C [7]. Nevertheless, in reality, it is limited by either contact metal temperature limit or packaging materials. As observed, the maximum allowed pulsed drain current for this device is 200A@25°C. However, when the DC power limit line is used, the maximum permitted current decreases 65A, the intersection point of DC Line 2 and Line 4.

4) Line 4: On-resistance limit line

This line is defined by the maximum on-resistance at the maximum junction temperature Tj=175°C as follows.

$$I_{DS} = \frac{V_{DS}}{R_{DS(on)(175℃)}} \tag{7.7}$$

As indicated, the value of $R_{DS(on)(175℃)}$ for this device is around 0.1Ω.

Thus, the maximum overload current to satisfy SOA for this application is 65A.

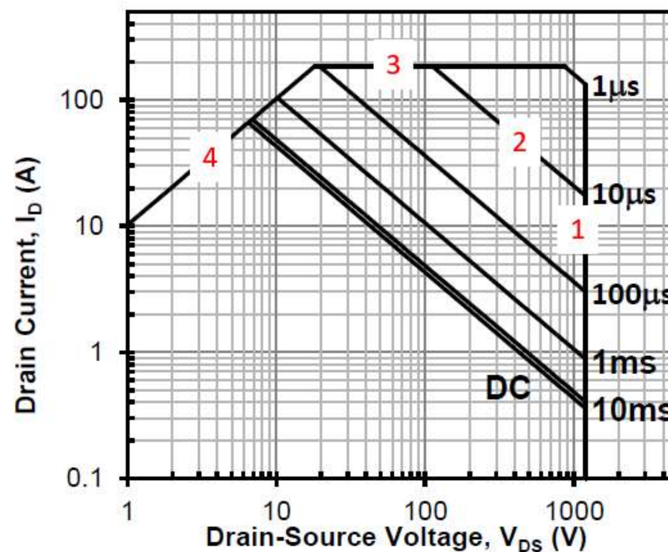


Figure 7.3 SOA curve of UJ3N120035K3S [5]

Simulation validation

Figure 7.4 shows the simulated junction temperature rise over the time for a constant 65A current injection. In line with the theoretical calculations, the temperature range is chosen between 100°C and 250°C. Then, the value of I^2t is obtained as 13.29A^2s which doubles the calculated result 6.43 A^2s. This is due to the assumption of the adiabatic condition for the theoretical calculations neglecting heat dissipating through the package. Based on the value of 13.29, the overload curve for the proposed SSCB is designed as shown in Figure 7.5.

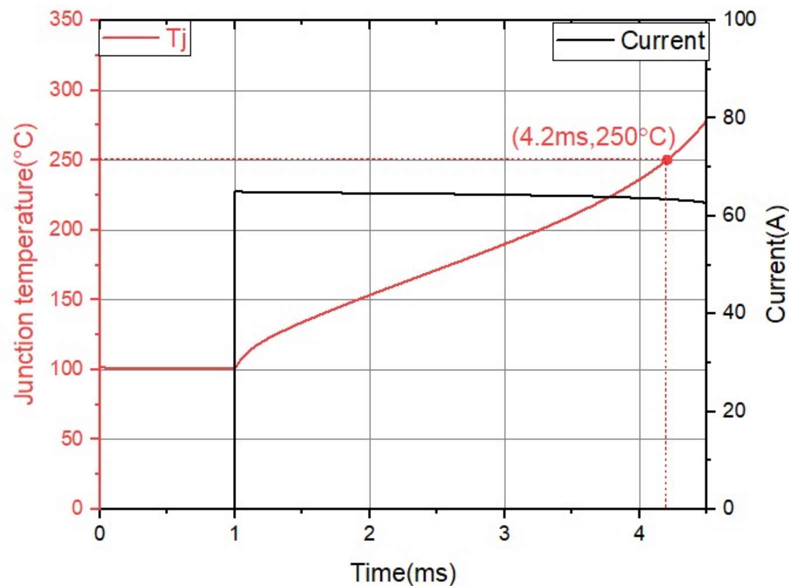


Figure 7.4 Simulated junction temperature for a 65A pulsed current injection

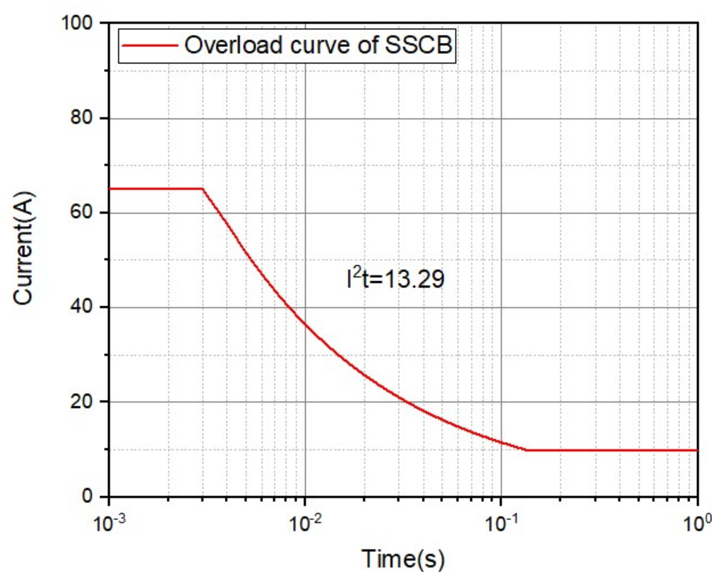


Figure 7.5 Overload curve for the proposed SSCB

7.2.3 Experimental validation

Figure 7.6 shows the circuit diagram of the experimental setup. A power IGBT is used for controlling the duration of the overload current while a power resistor is included to limit the magnitude of the current. A photo of the experimental setup is shown in Figure 7.7.

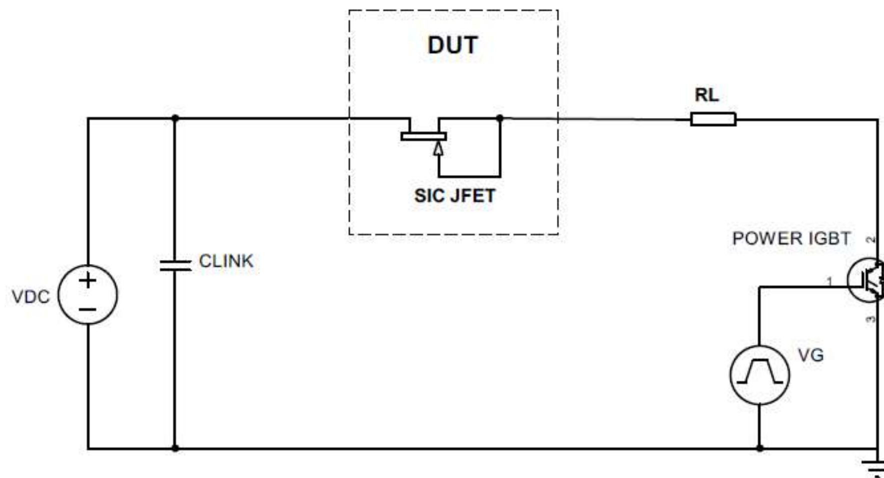


Figure 7.6 Schematic of the overload experimental setup

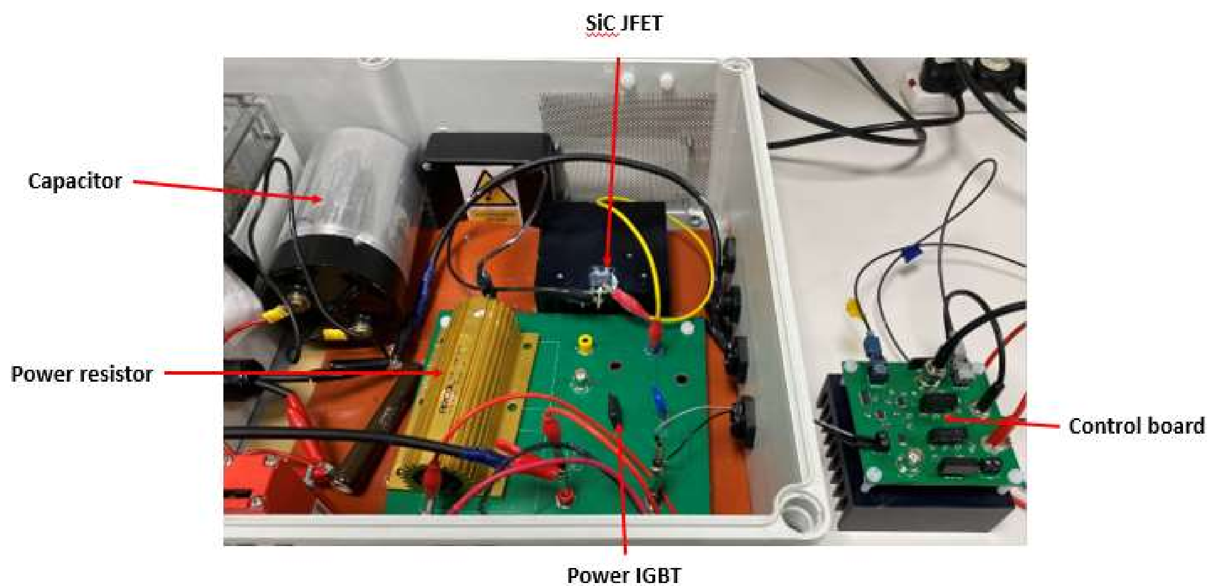


Figure 7.7 Photo of the overload test bench

Due to the limitation of the maximum output current(40A) of the DC power supply[8] in the laboratory, the current is set around 30A. Figure 7.8 shows the current waveform and the corresponding value of I^2t 13.65 A^2s, close to the value 13.29 A^2s of the simulated result. Therefore, the experimental results validate the correctness of the designed overload current tripping curve.

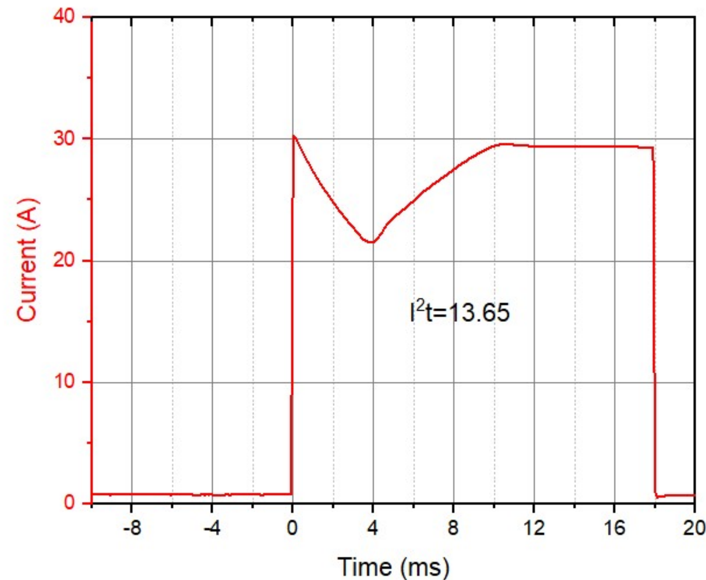


Figure 7.8 Overload current

7.2.4 Current sensing

A common process to realize the overload protection is first to sense the load current and then compare it with the pre-setting data according to the overload tripping curve. Once the load current exceeds the rated level, the timer starts timing until the accumulating time reaches the corresponding setting value. Then, a trigger signal is sent out to turn off the SSCB. The process could be completed by a current sensing element together with a digital processing unit such as DSP or Microcontroller[9].The accuracy and the speed of sensing current technique is fundamental to determine the performance of overload protection. Generally, five types of sensing techniques are commonly employed for detecting current to be briefed as follows[10][11].

Shunt resistor Sensing

A shunt resistor is introduced into the current path and the voltage drop across the resistor is measured, which is proportional to the current according to the Ohm's law.

Current Transformer/Rogowski coil

This method measures the current by exploiting Faraday's law of induction since a changing current would induce the voltage into a close-loop coil. A current transformer, usually made of Rogowski coils is placed around a current carrying conductor.

Hall effect sensors

The Hall-effect is used for this measurement. When a current (I) flows through a thin layer of conductive material which is simultaneously penetrated by a magnetic flux density (B), a voltage across the material is generated and determined by,

$$V = \frac{I.B}{n.q.d} \quad (7.8)$$

where q is the charge of the carrier, n is the carrier density and d is thickness of the sheet. Given the parameters B, n, q and d, the current is obtained by measuring the voltage.

On-state voltage sensing

During on-state of a semiconductor device, the on-state voltage drop across the power device is approximately proportional to the current flowing through the device in the linear region.

Giant magneto resistance sensor

Since the electrical resistance of some special material changes with the applied magnetic field induced by the current, the current can be derived by measuring the change of the resistance. Table 7.1 compares the above five methods.

Table 7.1 Comparison of five current sensing techniques

Method	Advantages	Disadvantages
Shunt resistor	1, Simple and low cost 2, Good accuracy 3, Easy integration with electronic devices	1, Poor transient response due to the parasitic inductance 2, No electrical isolation between the main power and the protection circuit 3, High power losses
Current transformer/ Rogowski coil	1, Provide isolation between the power circuit and the protection circuit. 2, Convenient to step down a high primary current to a low secondary current.	1, Not suitable for sensing DC currents. 2, A large core is required to avoid saturation for high current measurement.
Hall effect	1, Provide isolation between the power circuit and the protection circuit. 2, Capable of measuring DC currents	1, Require degaussing cycle after an overcurrent incident. 2, Error due to thermal drift
On-state voltage	1, No extra sensing element is required 2, Fast response speed 3, No extra cost	1, A coarse measurement 2, No electrical isolation between the main power and the protection circuit
Giant magneto resistance	1, Excellent accuracy and fast measurement 2, Capable of sensing small current 3, Conveniently integrated into an IC 4, Low power consumption	1, Susceptible to external magnetic fields. 2, Bandwidth is limited by the skin effect.

7.3 Over Temperature Protection

7.3.1 Methods of junction temperature measurements

The junction temperature is a key indicator for the reliability and health of semiconductor devices. Therefore, condition monitoring device junction temperature along with control methods is essential for the safe and reliable operation of SSCBs. However, the real-time measurement of the junction temperature of a power device proves to be a significant challenge. The measurement or estimation of junction temperature methods can be broadly categorized into three groups: 1) optical methods 2) physically contacting methods 3) electrical methods [12], which are introduced separately in the following.

Optical methods

This method senses the temperature by using the temperature-depend optical properties of the device material such as infrared radiation, reflected radiation, or stimulated emitted radiation. For instance, one common optical method is the measurement of the infrared radiation emission from a heated device using infrared thermal image camera[13]. The main advantage of this method can provide a temperature map of the whole device. However, this method is only suitable for either bare dies or devices which have an open window in their packages. Therefore, this method is impractical for real-time field operation.

Physically contacting methods

This method measures the temperature using thermal probes or thermo-sensitive materials which have direct contacts to the device chip[14]. Same requirement with the optical methods, the device chip under measurement must be physically accessible. Therefore, a significant packaging modification may be required to allow the thermal probes to access to the chip. Furthermore, there exist safety concerns when measuring the temperature of the device in high voltage operating conditions.

Electrical methods

This method is an indirect measurement of the junction temperature using Temperature Sensitive Electrical Parameters (TSEPs) of semiconductor devices[14]. Although this method estimates an average temperature of the semiconductor device and cannot detect hot spots of the device chip, TSEPs method provides a practical way to realize real-time junction temperature measurement on semiconductor chips most enclosed in sealed packages[15].

In the end, Table 7.2 summaries the three methods. Since both optical and physically contacting methods require either visually or physically access to the device chip, they are more suitable for laboratory research than industrial applications. By contrast, TSEPs method can be

practically adopted for real-time temperature measurement. For this research, the TSEPs method is used for monitoring the device temperature for the proposed SSCB.

Table 7.2 Comparisons of three methods of temperature measurement

Method	Example	Advantages	Disadvantages
Optical	Infrared thermal image camera	Map temperature of the whole device chip	Need device surface exposed
Physically contacting	Thermal couples or probes	Direct temperature measurement	• Need mechanical access to the chip • Safety concerns for the device under high operating voltage
Electrical (TSEPs)	• On-state resistance • Gate threshold voltage • di/dt during turn-on • dv/dt during turn-off • Body diode forward voltage	Suitable for sealed package devices	• Indirect measurement • Not be able to detect hot spots of the device chip

7.3.2 Selection of the TSEP for the proposed SSCB

A number of electrical parameters were reported for real time junction temperature measurement of semiconductor devices, such as di/dt [16], dv/dt [17], gate threshold voltage[18], on-state voltage drop[19][20], on resistance [21], internal gate resistance[22], gate drive turn-on current transient[23], and body diode junction forward voltage[24]. For this research, the main task is to monitor the device junction temperature during the normal operation. Since SSCBs stay on most time, transient or switching-related TSEPs such as di/dt, dv/dt and threshold voltage are not appropriate but those static parameters such as on-state voltage or on-resistance for this application. As on-state voltage is a current-dependent parameter and requires decoupling the load dependency from thermal effects, on-resistance is chosen as a TSEP for the junction temperature measurement of SiC JFETs power devices for this research.

7.3.3 On-resistance temperate dependency of a typical vertical power SiC JFET

A SiC JFET device is essentially a gate-voltage controlled resistor when it operates in the linear region. The on-resistance of a SiC JFET device is contributed by a number of resistances including the source contact resistance, channel resistance, drift region resistance, and drain

contact resistance. However, the on-resistance of a high-voltage JFET is mainly determined by its channel resistance and drift region resistance. Figure 7.9 shows a cross-section of a typical high-voltage vertical channel SiC JFET structure [25]. The basic device dimensions are denoted as the channel length L, the channel width 2a, the drift region width W_{DRIFT}, device thickness Z, and the drain length L_{DRIFT}. Hence, the on-resistance of high-voltage SiC JFET can be approximated from Equation 7.9 below, the summation of channel resistance and drift region resistance[26].

$$R_{on} = R_{CH} + R_{DRIFT} = \frac{L}{2q\mu_{CH}N_{CH}Z(a-W_{S})} + \frac{L_{DRIFT}}{q\mu_{DRIFT}N_{DRIFT}Z.W_{DRIFT}} \tag{7.9}$$

Where μ_{CH} and μ_{DRIFT} are carrier mobility in channel and drift region respectively.
It is well known that the carrier mobility of semiconductor materials is temperature-dependent parameter. For SiC JFET devices, the carrier mobility dependency on temperature can be estimated by an empirical equation below although the mobility in channel and drift region can be very different, depending on the structure and fabrication process of each device[26].

$$\mu_{T} = \frac{947}{1+\left(\frac{N_D}{1.94.10^{17}}\right)^{0.61}}\left(\frac{T}{300}\right)^{-2.15} \tag{7.10}$$

Based on Equation 7.9 and Equation 7.10, the temperature dependant on-resistance $R_{on(T)}$ of a vertical SiC JFET device has established the relationship with the temperature as follow.

$$R_{on(T)} = R_{on(300K)}\left(\frac{T}{300}\right)^{2.15} \tag{7.11}$$

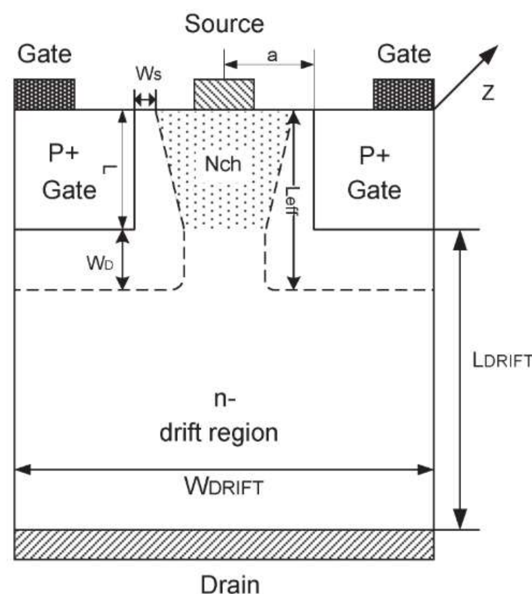


Figure 7.9 Cross-section of a vertical SiC JFET

7.3.4 Realization of real-time temperature measurements

The realization of TSEPs method needs two steps[15]. Step one is called Calibration step. The aim of this step is to establish the relationship between the TSEP and the junction temperature. Step two is called Measurement step. This step is to measure the TSEP and then compare it with the value acquired in Step one before the junction temperature is able to be extrapolated. The implementation of the two-step measurement on the junction temperature of a SiC JFET device using on-resistance as a TSEP is described as follows.

Step one: Calibration

Figure 7.10(a) shows a simple calibration circuit to establish the relationship between the on-resistance and the junction temperature of a SiC JFET device. A current source injects a low current into the on-state SiC JFET device and the voltage across the device is measured under the variant temperatures. The temperature is controlled by an external heating element such as an oven or a hot plate. During the measurement, the magnitude and pulse duration of injected current should be kept as low as possible to eliminate the self-heating influence. Alternatively, a curve tracer together with a temperature-controlled oven can be used for this step.

Step two: Measurement

For the real-time measurement, a dedicated circuit with a minimal influence on the performance of the device under measurement is required. Figure 7.10(b) shows a practical measurement circuit [27]. A n-channel MOSFET in series with resistor R1 is paralleled to the SiC JFET device. Meanwhile, a constant low DC voltage source V1 such as 9V supply the gate biased voltage to the MOSFET. During the on-state of the SiC JFET, the MOSFET turns on. Thus, the on-state voltage of the SiC JFET can be obtained by the measurement of voltage across the resistor R1. Simultaneously, the current flowing through the SiC JFET is measured by either a shunt resistor or a current sensor. As a result, the on-resistance of SiC JFET can be figured out and then the junction temperature can be extrapolated by comparing the measured on-resistance with the data acquired in Step one. When the SiC JFET device starts turning off and the drain voltage of SiC JFET exceeds the external DC voltage V1, the MOSFET is switched off and withstands the high voltage. Consequently, it prevents the measurement circuitry connecting to R1 from exposed to the high dangerous voltage.

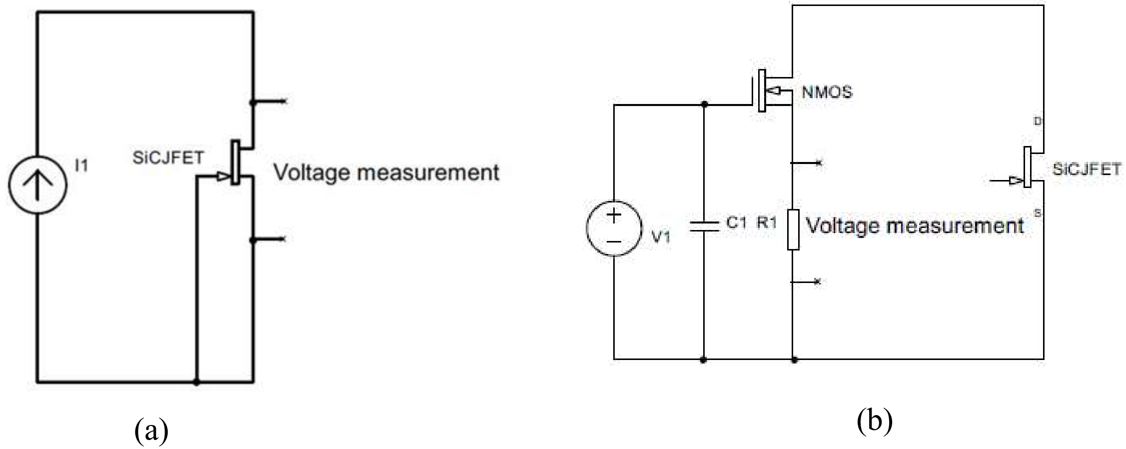


Figure 7.10(a) Circuit for Step one (b) Circuit for Step two

7.3.5 Simulation validation

Step one: Calibration

Figure 7.11 (a) shows the simulation circuit, exactly same of the designed circuit for Calibration. A low constant current such as 100mA feeds the SiC JFET model while the on-state voltage of the SiC JFET is probed under the variant junction temperature setting ranging from 25°C to 175°C. The on-resistance against the junction temperature is illustrated in Figure 7.11(b).

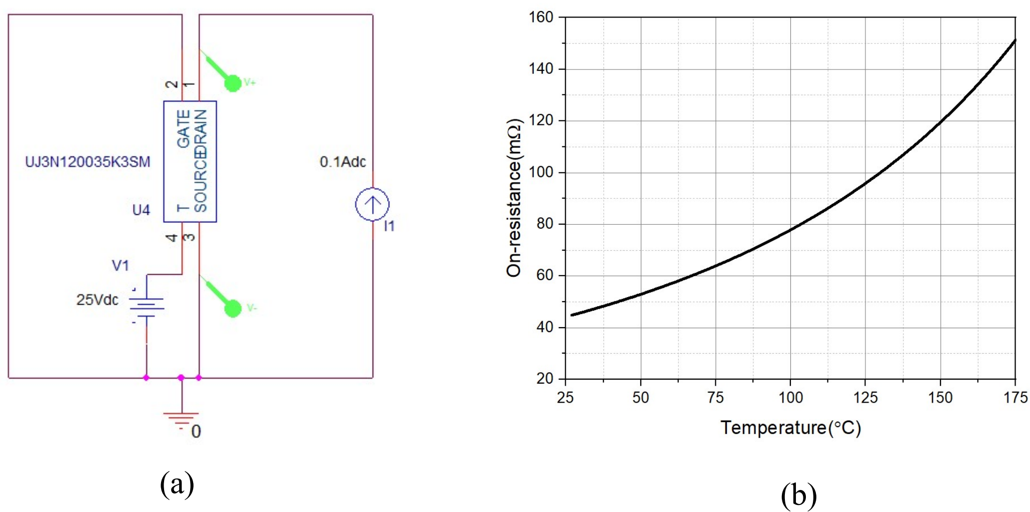
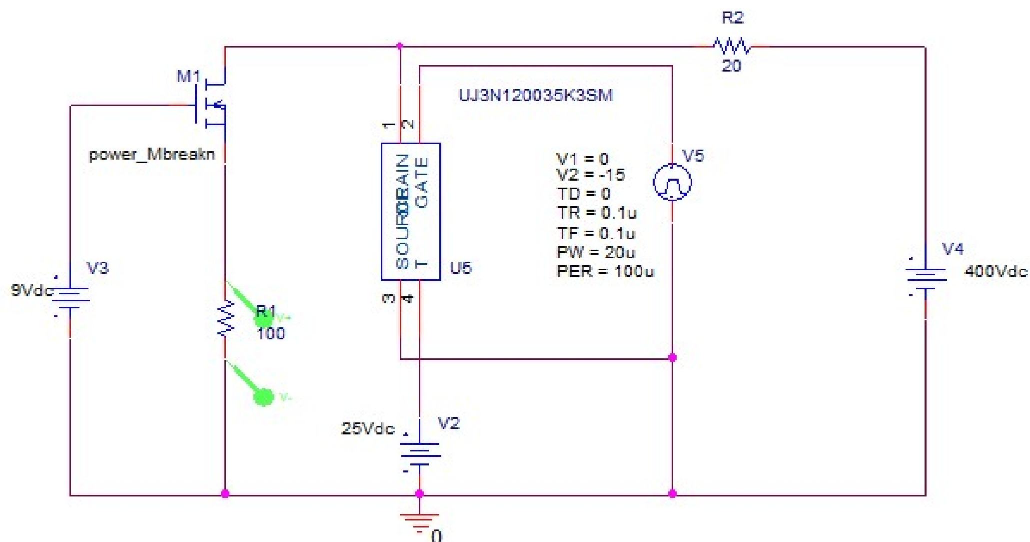


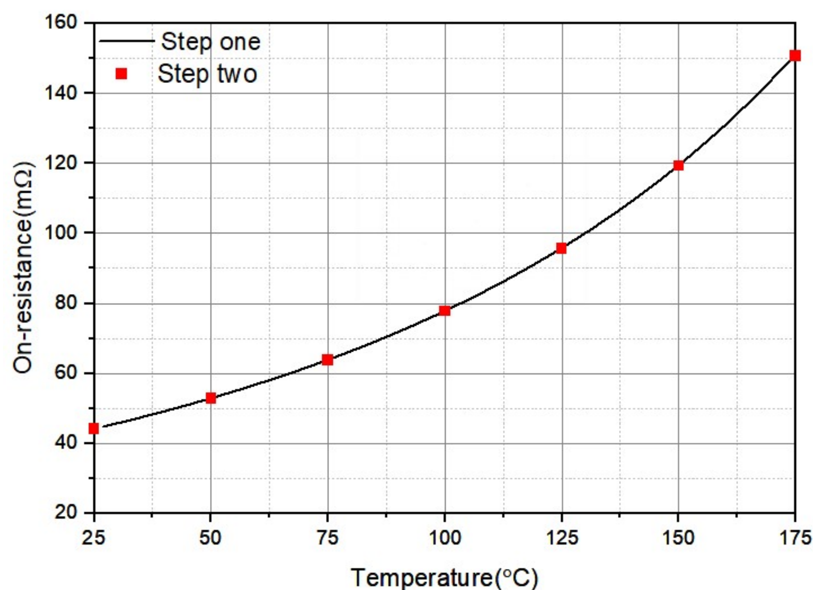
Figure 7.11 Step one (a) Simulated circuit (b) On-resistance.vs.junction temperature

Step two: Measurement

As shown in Figure 7.12(a), the simulation circuit is same of the designed circuit for Step two. When the SiC JFET turns on, both the voltage across R1 and the current through the SiC JFET are probed under variant junction temperature setting. The measured result is compared with that in Step one as shown in Figure 7.12 (b). It demonstrates an excellent match between them. To conclude, the simulated results validate the designed circuits for both steps.



(a)



(b)

Figure 7.12 Step 2 (a) Simulation circuit (b) Comparison of the results between two steps

7.3.6 Experiment validation

Step one Calibration

As shown in Figure 7.13, a curve tracer and an oven are used for Calibration. Figure 7.14(a) shows the output characteristics of the SiC JFET under the variant temperatures ranging from 25°C to 175°C while the on-resistance dependency on the temperature is plotted in Figure 7.14(b).

Figure 7.13 Curve tracer (left) and Oven (right)

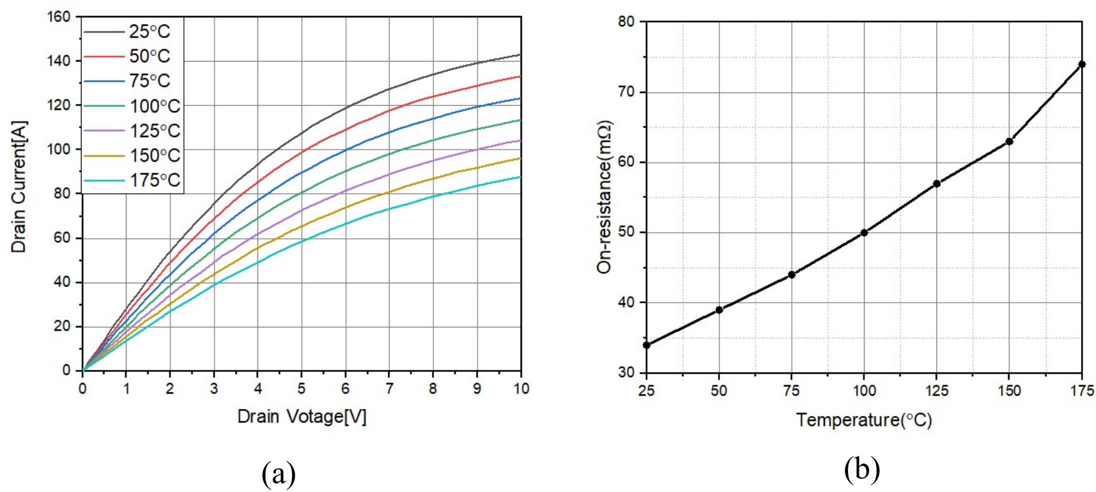


Figure 7.14(a) Output characteristics (b) On-resistance vs.temperature

Step 2 Measurement

A photo of the experimental setup is shown in Figure 15. A hot plate is used for heating the device and a thermometer for temperature measurement. The voltage across the resistor R1 is measured when a 10A current pulse is injected into the device. The pulsed time is limited to minimize the self-heating.

The waveforms of the measured voltage drop and injected pulsed current under room temperature is shown in Figure 16(a) The middle point of the voltage drop during the pulsed period is picked as the measured result. Figure 16(b) compares the measured on-resistance between Step one and Step two. As can be seen, the significant discrepancy is displayed, which is dauntedly due to the circuit parasitic resistance, the accuracy of voltage probe for small voltage measurement and device self-heating. However, they maintain the similar increasing trend with elevated temperature.

To conclude, the experimental results verify the feasibility of TSEP method for the online junction temperature measurement.

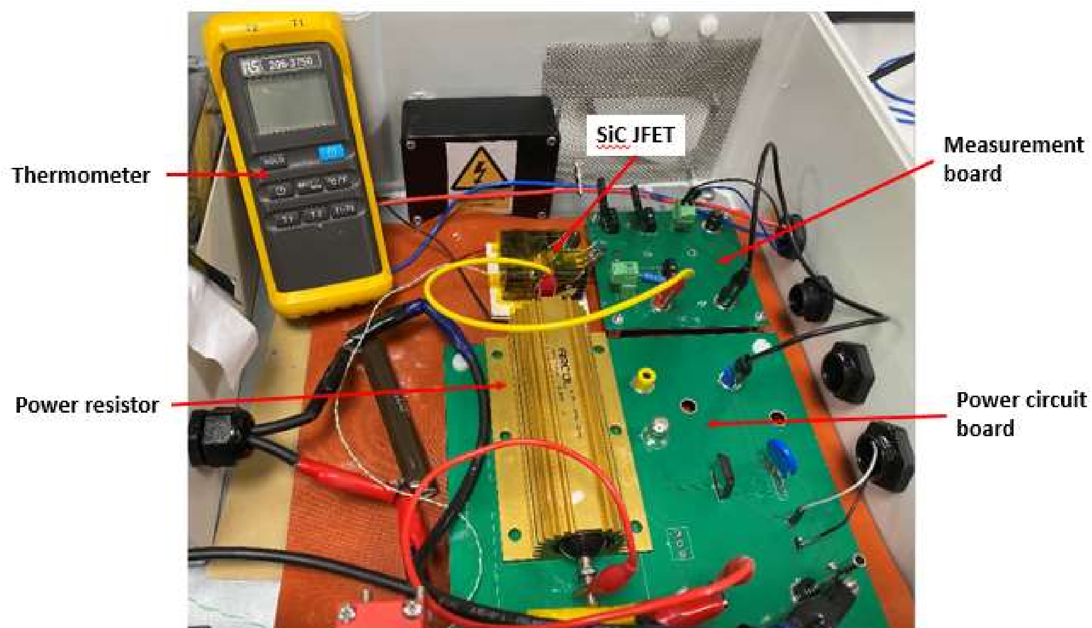
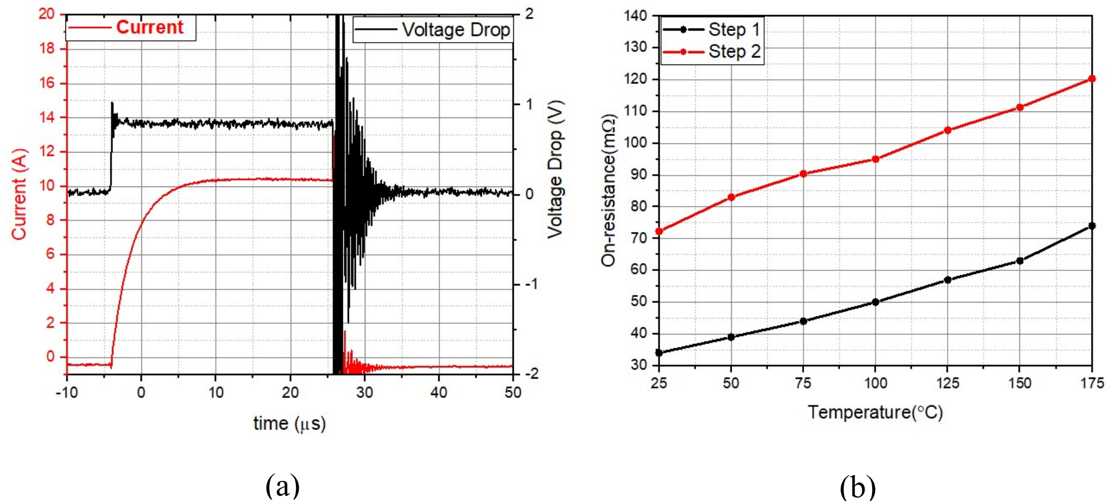


Figure 7.15 Experimental setup



(a) (b)

Figure 7.16 (a) Waveforms of measured voltage and current (b) Comparison of measured on-resistance between Step 1 and Step 2

7.4 Conclusions

This chapter has presented the design of the time-current tripping curve for overload protection. Both simulation and experimental results have demonstrated the value of I^2t of the SiC JFET (UJ3N120035K3S) around 13 A^2s, an indicator of the device thermal capability. Temperature-dependant on-resistance has been chosen for real-time measurement of device junction temperature. A practical circuit for the measurement has been provided and verified by both simulation and experiment.

7.5 References

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Chapter 8 Conclusions and Future Work

8.1 Conclusions

The high magnitude and rapid increasing of fault current in DC microgrids poses a significant mechanical and thermal stress on both component and system level of DC grids. Therefore, the desire for DC protection devices with the feature of fast switching speed along with the current-limiting capability has motivated this research on solid-state circuit breakers for 400V DC microgrids. In this research, a SiC JFET-based solid-state circuit breaker has been designed and built. The experimental results have demonstrated the proposed SSCB is capable of interrupting current beyond 100A within 55μs while the overvoltage across the SSCB is suppressed below 800V. In addition, other functionalities of the proposed SSCB such as protection coordination, immunity to inrush current, fail-safe, overload protection and over temperature protection, have also been designed and discussed. In addition, the research has made the following achievement.

- **Designing a unique circuit topology to achieve an ultrafast response speed and current-limiting capability**

This unique circuit is configured with a high-voltage normally-on SiC-JFET and low-voltage normally-off Si MOSFET. Compared to the conventional communication-based circuit topologies for SSCB application, this circuit for short-circuit protection offers several advantages. Firstly, it eliminates complicated and time-consuming sensing and tripping circuitry and therefore offers a significant fast response time. Secondly, with this configuration, the fault current can be limited below a certain current level which is adjustable to meet the requirement of different applications. Thirdly, the normally-on SiC JFET device offers both low specific on-resistance and exceptional robustness under short-circuit conditions. Finally, the component count is kept minimum which makes this solution cost effective and simple to implement in practical applications.

- **Designing a novel snubber for suppressing overvoltage at the turn-off of the SSCB**

A novel snubber has been designed for 400V DC solid-state circuit breakers. It takes the advantages of effective overvoltage suppression of RCD snubbers and high energy absorption capability of MOVs while eliminating the requirement of high-power resistor of RCD snubbers and mitigating the transient fluctuation of MOVs. Meanwhile, the analytical expressions of each stage for the operating process of the snubber are given, providing guidance for the snubber design for SSCBs application. Furthermore, the impact factors on the response time of SSCBs have been discussed and an equation is provided for optimal snubber design to meet different application requirements.

- **Providing analytical expressions of output characteristics of the TBU as a design guideline of the circuit topology for SSCB applications**

The operating processes of the basic TBU, the basic TBU with two added resistors, the basic TBU with an added enhancement mode MOSFET, and the practical TBU have been analysed in details and their corresponding output expressions have been provided respectively, which could be used as a design methodology for the development of the unique circuit topology for SSCB application.

- **Modifying the commercial SPICE model suitable for SSCB applications**

The commercial SPICE model is suitable for the typical applications of the device such as switched mode power supplies and motor drives. Thus, it has limited accuracy when operating in the saturation region (short-circuit mode). In addition, this model can only set the junction temperature to a fixed value and does not account for the effect of dynamic temperature. To overcome these limitations, the model texts have been modified so that it can be fitted for SSCB application and reflects the device dynamic thermal performance.

8.2 Future Work

This work could establish the foundation for the SSCBs based on wide-band gap power devices applied for low-voltage DC microgrids. However, it is understandable that further improvements could be made to increase the completeness of this work. The following several areas are summarised for further development which takes the lead from this research.

- **Implementation of overload and over temperature protection**

Although the design of both overload and overtemperature protection have been presented in Chapter 7, they have not been implemented. It could be realized by either a DSP or a microcontroller which is able to simultaneously sample the current and the voltage. Once the measured value exceeds the pre-set stored value, a trigger signal is sent out to switch off the SSCB. For completeness of this work, both hardware and software need to be developed for realizing this function.

- **Experimental evaluation of impact factors on the tripping current level**

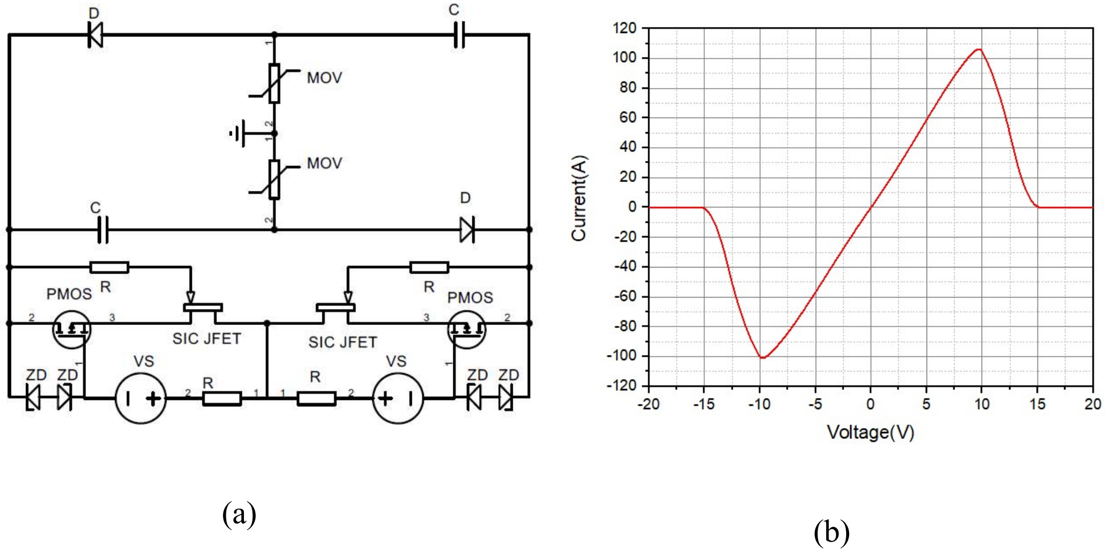
Tripping current is a critical parameter for the proposed SSCB, which directly impacts on the reliability of short-circuit protection. According to the analytic and simulated results presented in Chapter 6, it depends upon a number of factors including external voltage, junction temperature, on-resistance and threshold voltage of both high-voltage SiC JFET and low-voltage MOSFET. Experimental evaluation of the impacts on the tripling current by these factors could be undertaken. This result could provide design guidelines to control the tripping current level of the proposed SSCB.

- **Scale-up of current rating of SSCB by paralleling SiC JFET devices**

The current rating of the proposed SSCB for this research is only 10 A, whilst the loads for some applications such as data centre and shipboard will draw much higher current. Therefore, it is essential to improve the current rating of SSCBs. In theory, it can be achieved by paralleling multiple number of devices. In Chapter 4, SiC JFET devices in parallel have been investigated in both static and dynamic operation. General equations are provided to predict device junction temperature and current sharing among the devices in the final stable thermal equilibrium. However, implementation of paralleling devices is not a trivial thing since dynamic imbalanced current sharing could lead to one device thermal runaway due to being heated up more than the others. Therefore, a means of active current balance must be considered and implemented.

- **Realization of bidirectional function**

There are growing applications requiring bidirectional current flow in DC power systems such as rechargeable battery and matrix converters. For those applications, SSCBs must be able to interrupt fault currents and block voltages in both directions. As shown in Figure 8.1(a), back-to-back connection of two unidirectional SSCB could achieve the bidirectional fault protection. Figure 8.1 (b) show the preliminary simulated I-V curve of the bidirectional SSCB. However, a prototype bidirectional SSCB needs to be built and experimentally validated



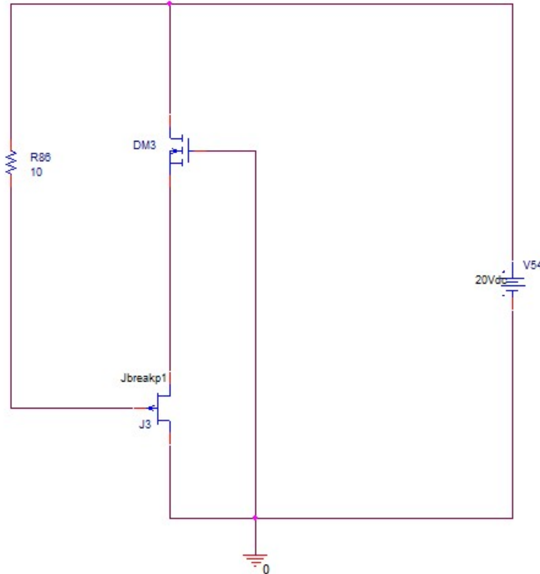
(a)

(b)

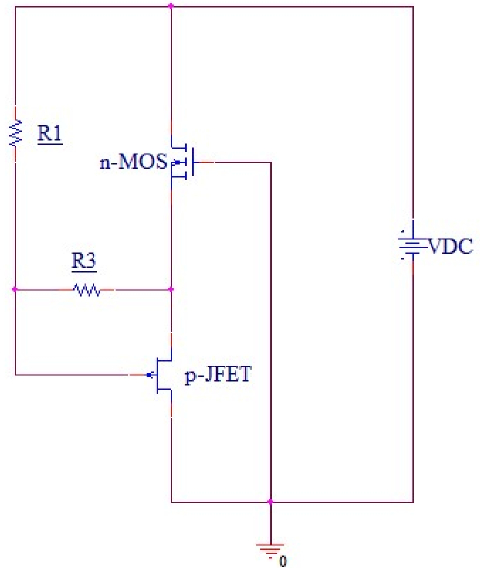
Figure 8.1 the proposed bidirectional SSCB (a) Schematic circuit (b) I-V curve

Appendix A: Simulation Circuits in the Thesis

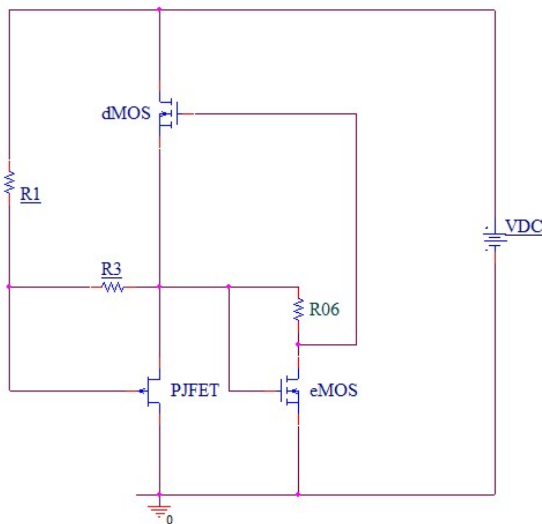
Chapter 3



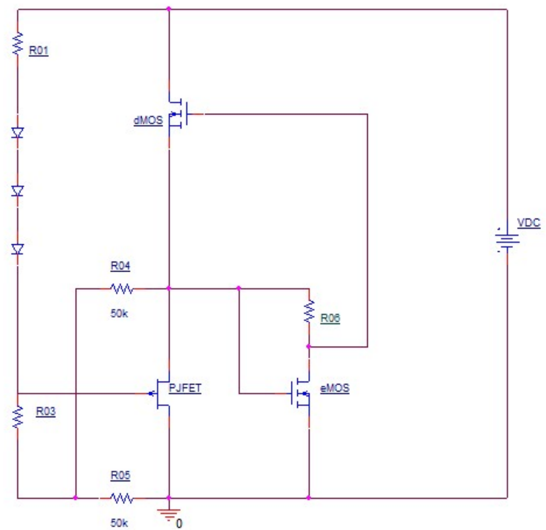
Basic TBU



TBU with two added resistors

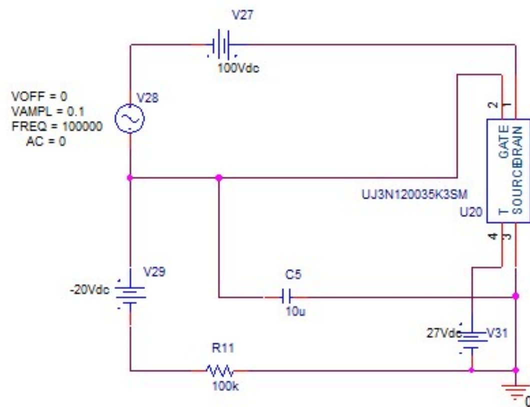


TBU with an added eMOS

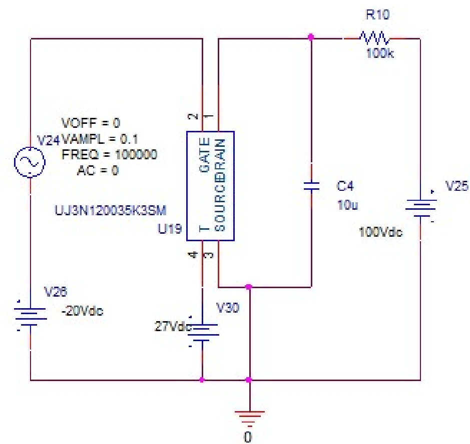


Unidirectional TBU

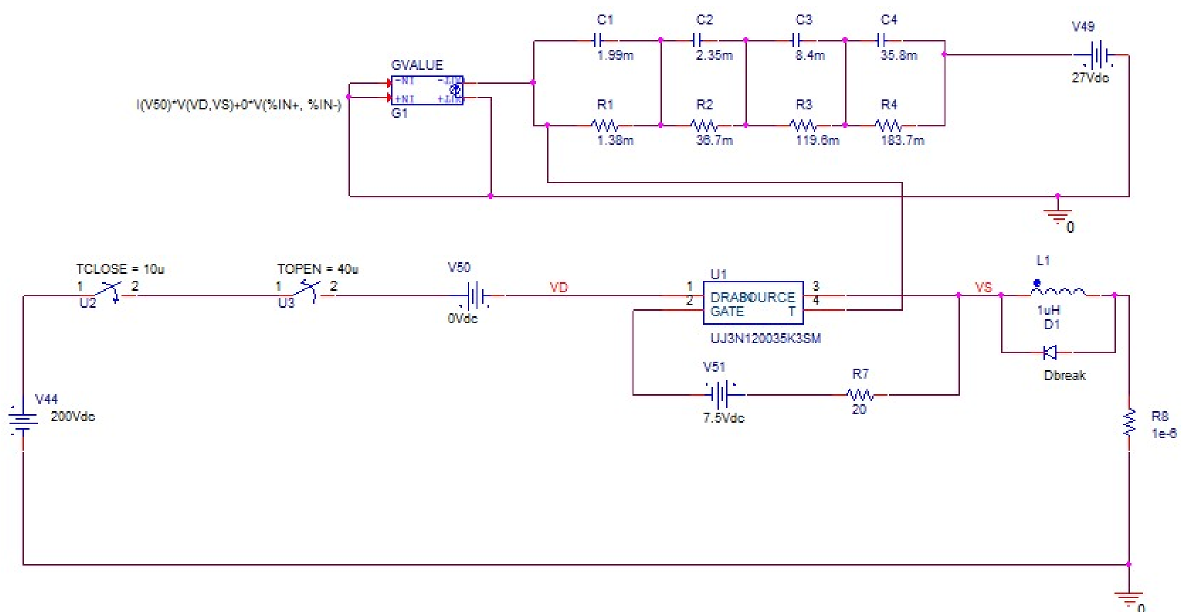
Chapter 4



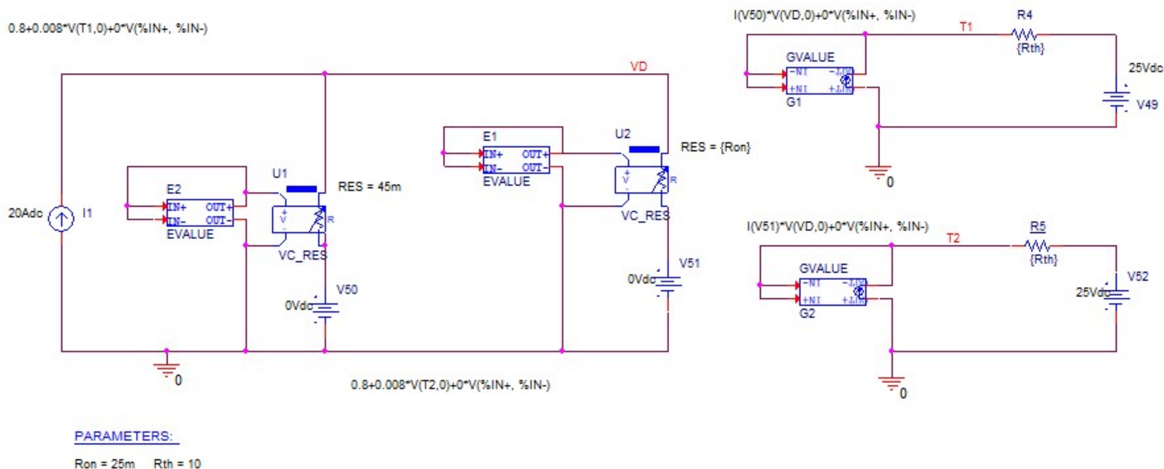
Measurement of output capacitance C_{oss}



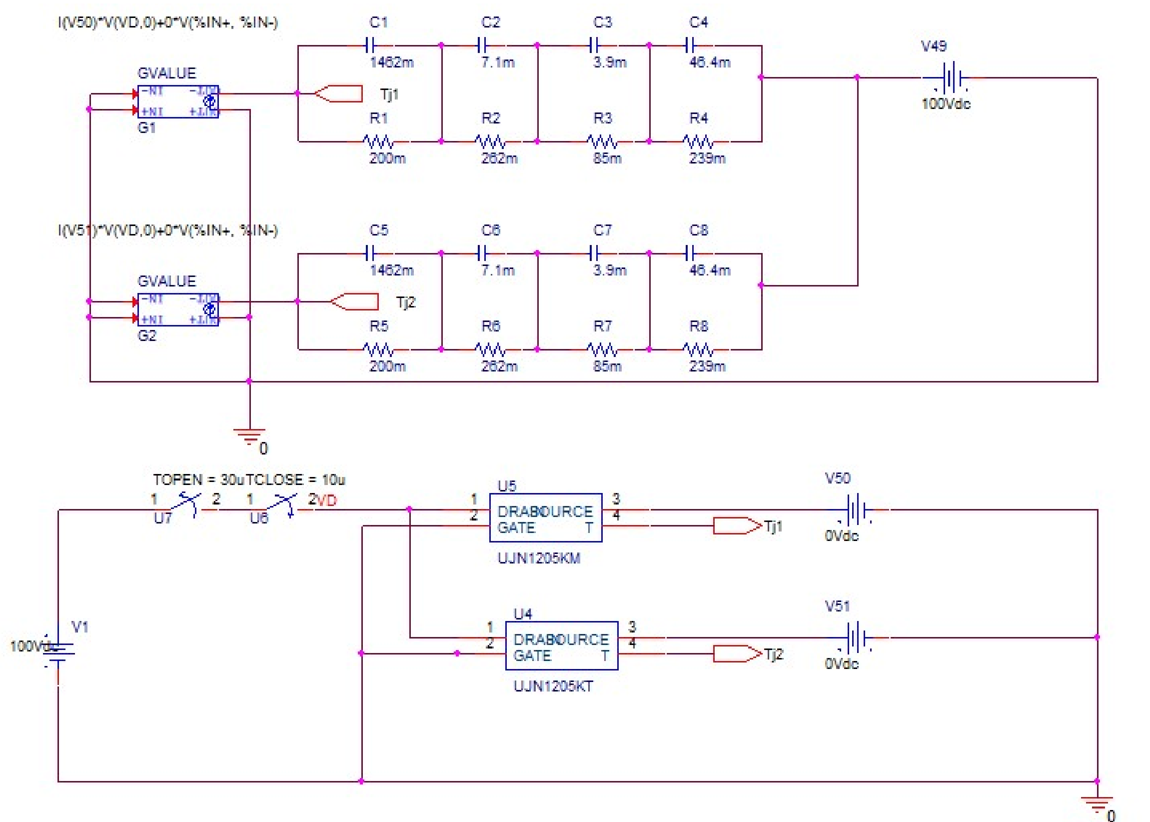
Measurement of input capacitance C_{iss}



Short-circuit capability of SiC JFETs

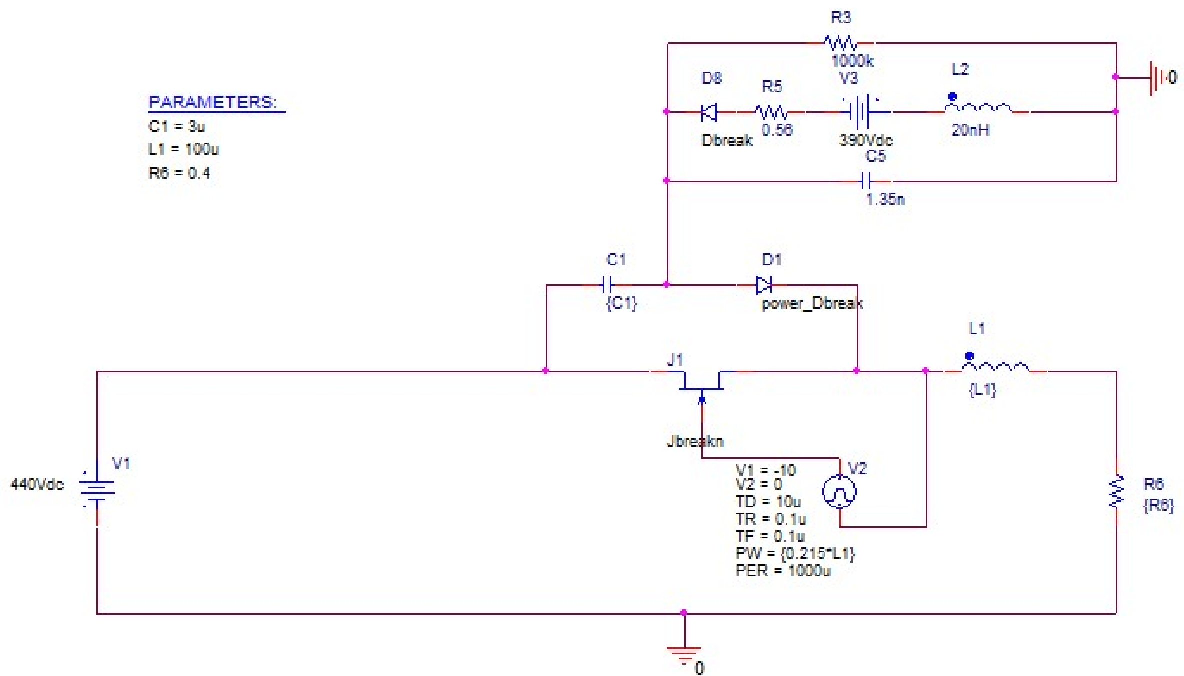


Static analysis of SiC JFETs in parallel



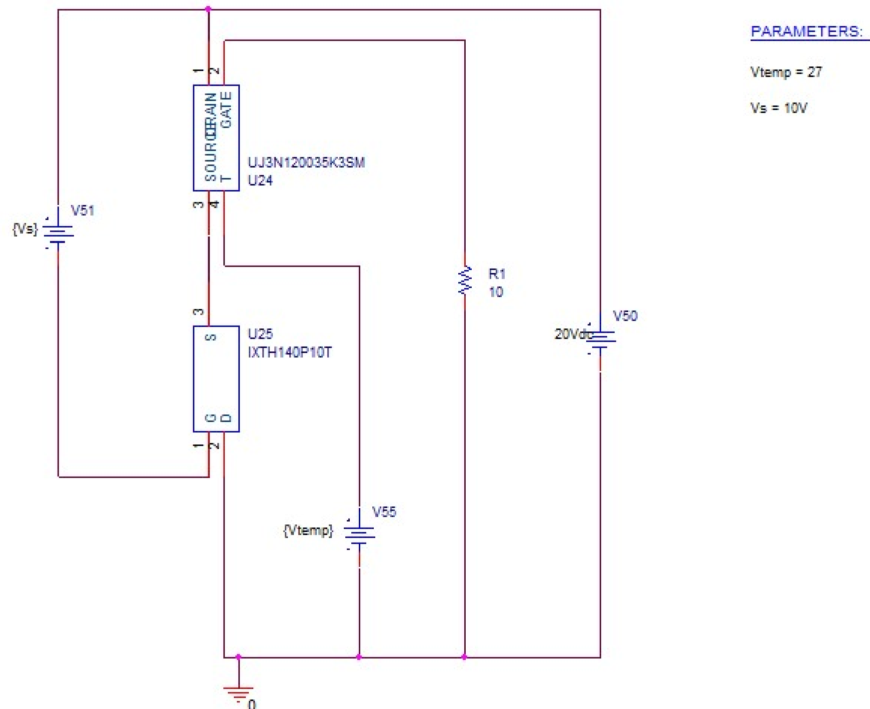
Transient analysis of SiC JFETs in parallel

Chapter 5

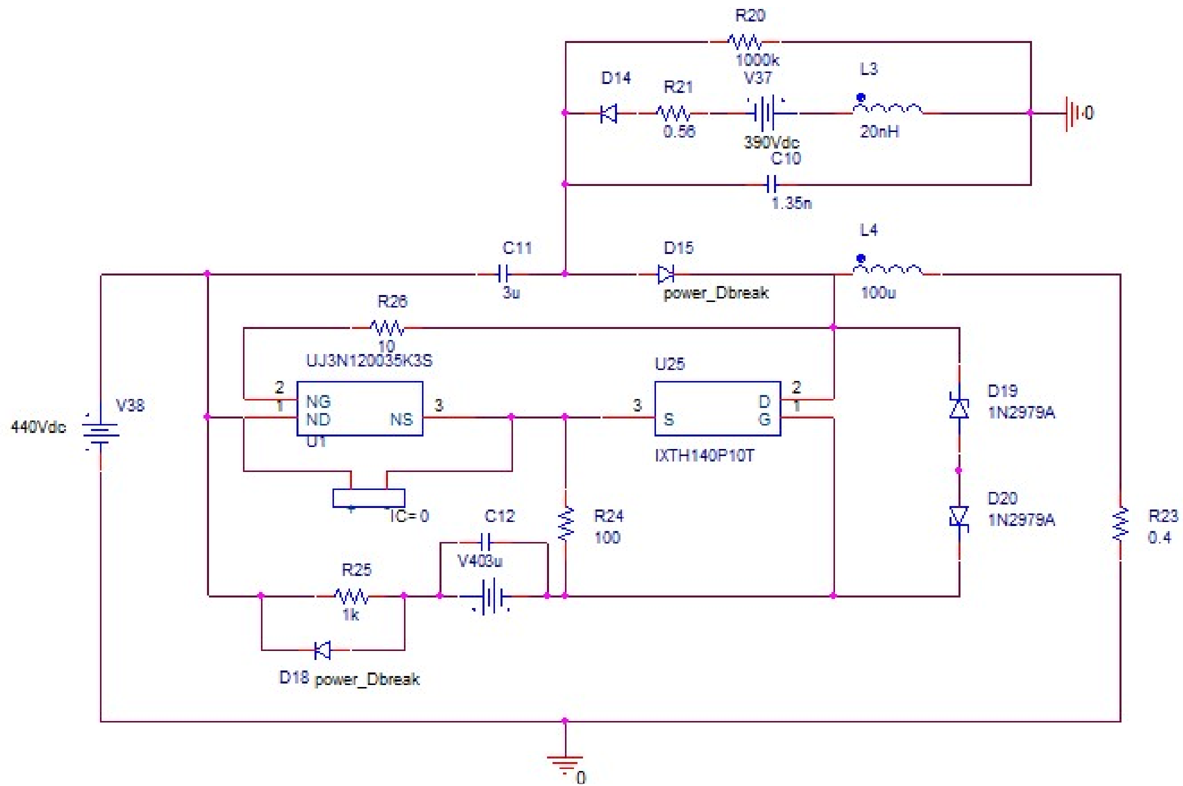


RCD snubber

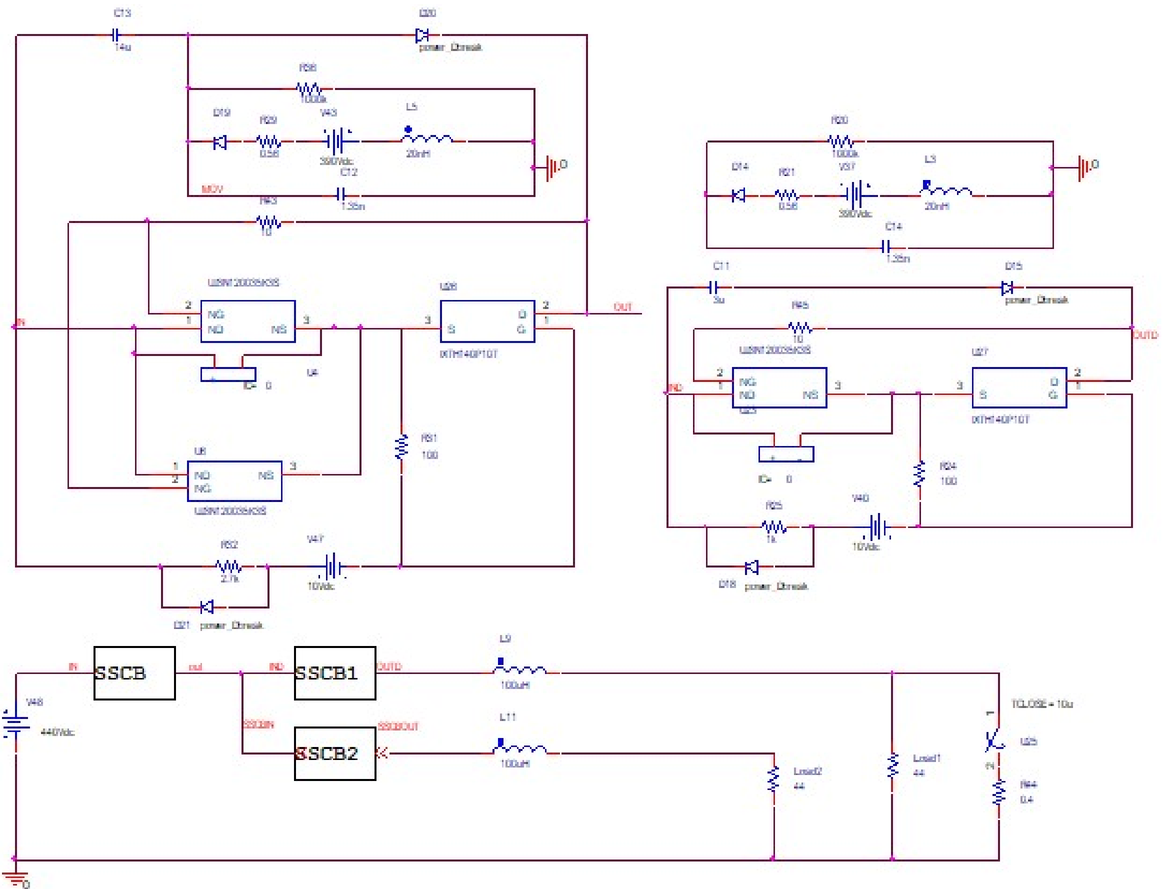
Chapter 6



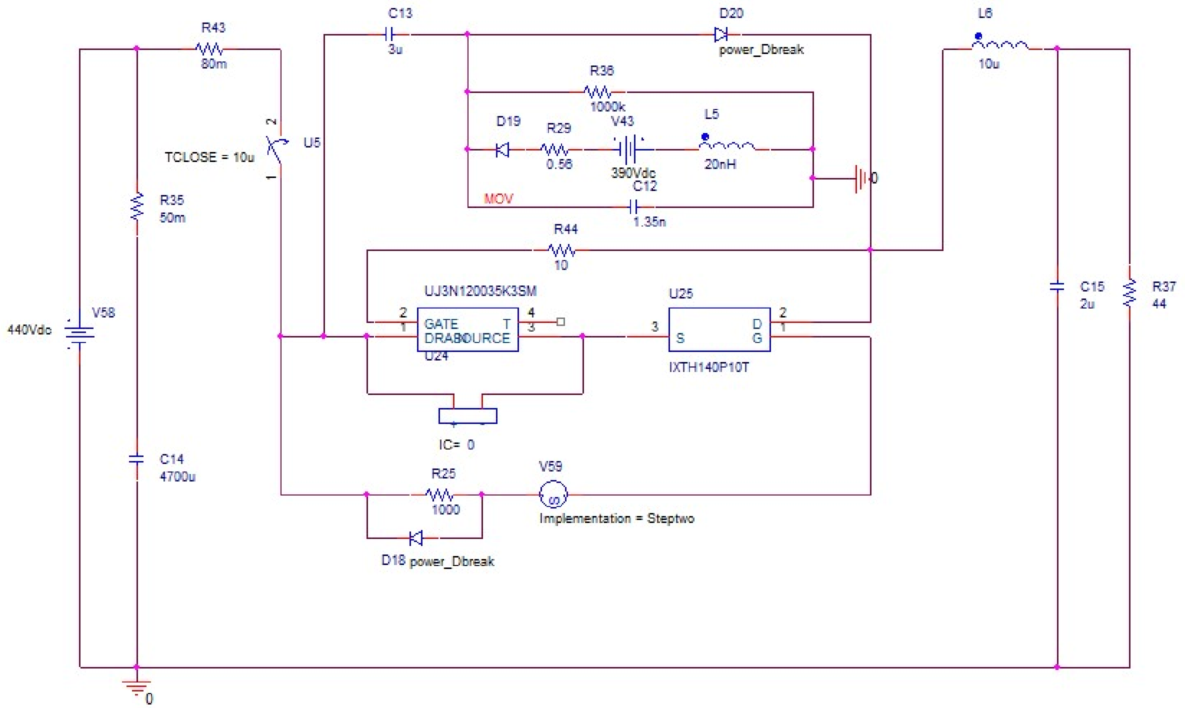
Static performance of the proposed SSCB



Transient performance of the proposed SSCB

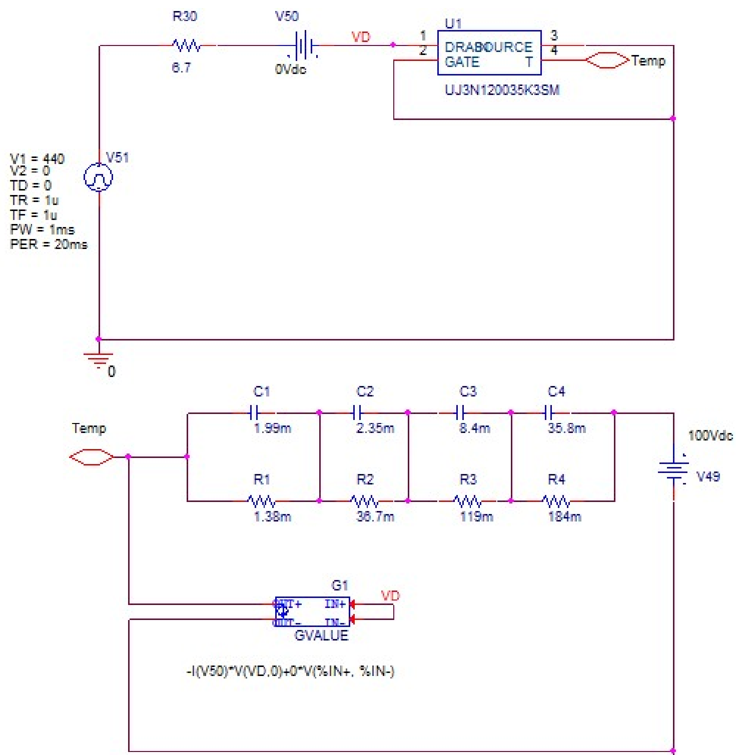


Protection coordination among three SSCBs



Inrush current issue

Chapter 7



Overload current

Appendix B: Silicon Carbide Junction Field Effect Transistor SPICE Models

Original Model	Modified model
.SUBCKT UJN1205k Drain Gate Source PARAMS: + beta=5.28 beta_tce=-30 vth=-7.892 vth_tc=4.0e-4 + npow=1.4480 npow_tc=-5.000e-04 lambda0=0.05 lambda1=-1.100e-01 + alpha=1.800 alpha_tc=-3.000e-03 + cdsa0=7e-12 cds0=8.82e-12 is0g=1.5000e-14 + cgda0=40e-12 cgd0=900e-12 cgd_FC=0.94 cgd_M=0.70 cgd_VJ=2.7 + cgsa0=150e-12 cgs0=1125e-12 cgs_FC=0.94 cgs_M=0.53 cgs_VJ=2.7 *Parasitics LD Drain D 5n R_RD D Dint 0.001 LS Source S 3n R_RS S Sint 0.001 LG Gate G 3n R_RG G Gint 0.5 R_RGAC1 Gint Gjd 1.5 R_RGAC2 Gjd Gjs 2.75 X_IDS Gjd Dint Sint IDJFET PARAMS: beta={beta} lambda0={lambda0} lambda1={lambda1} X_IGS Gint Gjd Sint IGATETOSOURCE *Current DBDD Gjd Dint DDBRKDWN DBDS Gjd Sint DSBRKDWN	.SUBCKT UJ3N120035K3SM Drain Gate Source T PARAMS: + beta=5.7 beta_tce=-30 vth=-9.2 vth_tc=4.0e-4 + npow=1.4480 npow_tc=-5.000e-04 lambda0=0.01 lambda1=-1.100e-01 + alpha=1.800 alpha_tc=-3.000e-03 + cdsa0=7e-12 cds0=8.82e-12 is0g=1.5000e-14 + cgda0=50e-12 cgd0=750e-12 cgd_FC=0.94 cgd_M=0.70 cgd_VJ=2.7 + cgsa0=150e-12 cgs0=2700e-12 cgs_FC=0.94 cgs_M=0.53 cgs_VJ=2.7 *Parasitics LD Drain D 5n R_RD D Dint 0.001 LS Source S 3n R_RS S Sint 0.001 LG Gate G 3n R_RG G Gint 0.5 R_RGAC1 Gint Gjd 1.5 R_RGAC2 Gjd Gjs 2.75 X_IDS Gjd Dint Sint T IDJFETM PARAMS: beta={beta} lambda0={lambda0} lambda1={lambda1} X_IGS Gint Gjd Sint T IGATETOSOURCEM *Current DBDD Gjd Dint DDBRKDWN DBDS Gjd Sint DSBRKDWN

DDGI Gjd Dint DGI	DDGI Gjd Dint DGI
DDGSI Gjd Sint DGSI	DDGSI Gjd Sint DGSI
*Capacitance	*Capacitance
DGD Gjd Dint Diodecgd	DGD Gjd Dint Diodecgd
CGDa Gjd Dint {0.5*cgda0}	CGDa Gjd Dint {0.5*cgda0}
DGD2 Gjs Dint Diodecgd	DGD2 Gjs Dint Diodecgd
CGDb Gjs Dint {0.5*cgda0}	CGDb Gjs Dint {0.5*cgda0}
DGS Gjs Sint Diodecgs	DGS Gjs Sint Diodecgs
CGSa Gjs Sint {0.5*cgsa0}	CGSa Gjs Sint {0.5*cgsa0}
DGS2 Gjd Sint Diodecgs	DGS2 Gjd Sint Diodecgs
CGSb Gjd Sint {0.5*cgsa0}	CGSb Gjd Sint {0.5*cgsa0}
CDSint Dint Sint {cdsa0}	CDSint Dint Sint {cdsa0}
CGSint Gint Sint 1e-13	CGSint Gint Sint 1e-13
CDS D S 1e-13	CDS D S 1e-13
CGD G D 1e-13	CGD G D 1e-13
CGS G S 1e-13	CGS G S 1e-13
.Model DGI D IS=5.6e-20 N=5.8 XTI=7 ISR=0 NR=2.9 VJ=12.7 CJO=0 Rs=.9	.Model DGI D IS=5.6e-20 N=5.8 XTI=7 ISR=0 NR=2.9 VJ=12.7 CJO=0 Rs=.9
.Model DGSI D EG=3.26 IS=1.500e-14 N=3.71 XTI=15 ISR=0 CJO=0 Rs=.1	.Model DGSI D EG=3.26 IS=1.500e-14 N=3.71 XTI=15 ISR=0 CJO=0 Rs=.1
.MODEL DDBRKDWN D IS=1e-40 ISR=0 N=1000 IBV=1.133 NBV=4.004e2 BV=1600 TBV1=1e-6 Rs=0.2	.MODEL DDBRKDWN D IS=1e-40 ISR=0 N=1000 IBV=1.133 NBV=4.004e2 BV=1600 TBV1=1e-6 Rs=0.2
.MODEL DSBRKDWN D EG=3.26 IS=1e-40 XTI=1 N=1000 ISR=0 IBV=1.823e-6 NBV=87.54 BV=45 Rs=0.2	.MODEL DSBRKDWN D EG=3.26 IS=1e-40 XTI=1 N=1000 ISR=0 IBV=1.823e-6 NBV=87.54 BV=45 Rs=0.2
.MODEL Diodecgd D IS=1e-40 XTI=1 N=1000 ISR=0 CJO={cgd0} EG=3.26 FC={cgd_FC} M={cgd_M} VJ={cgd_VJ} IKF=0 RS=0.2	.MODEL Diodecgd D IS=1e-40 XTI=1 N=1000 ISR=0 CJO={cgd0} EG=3.26 FC={cgd_FC} M={cgd_M} VJ={cgd_VJ} IKF=0 RS=0.2
.MODEL Diodecgs D IS=1e-40 XTI=1 N=1000 ISR=0 CJO={cgs0} EG=3.26	.MODEL Diodecgs D IS=1e-40 XTI=1 N=1000 ISR=0 CJO={cgs0} EG=3.26

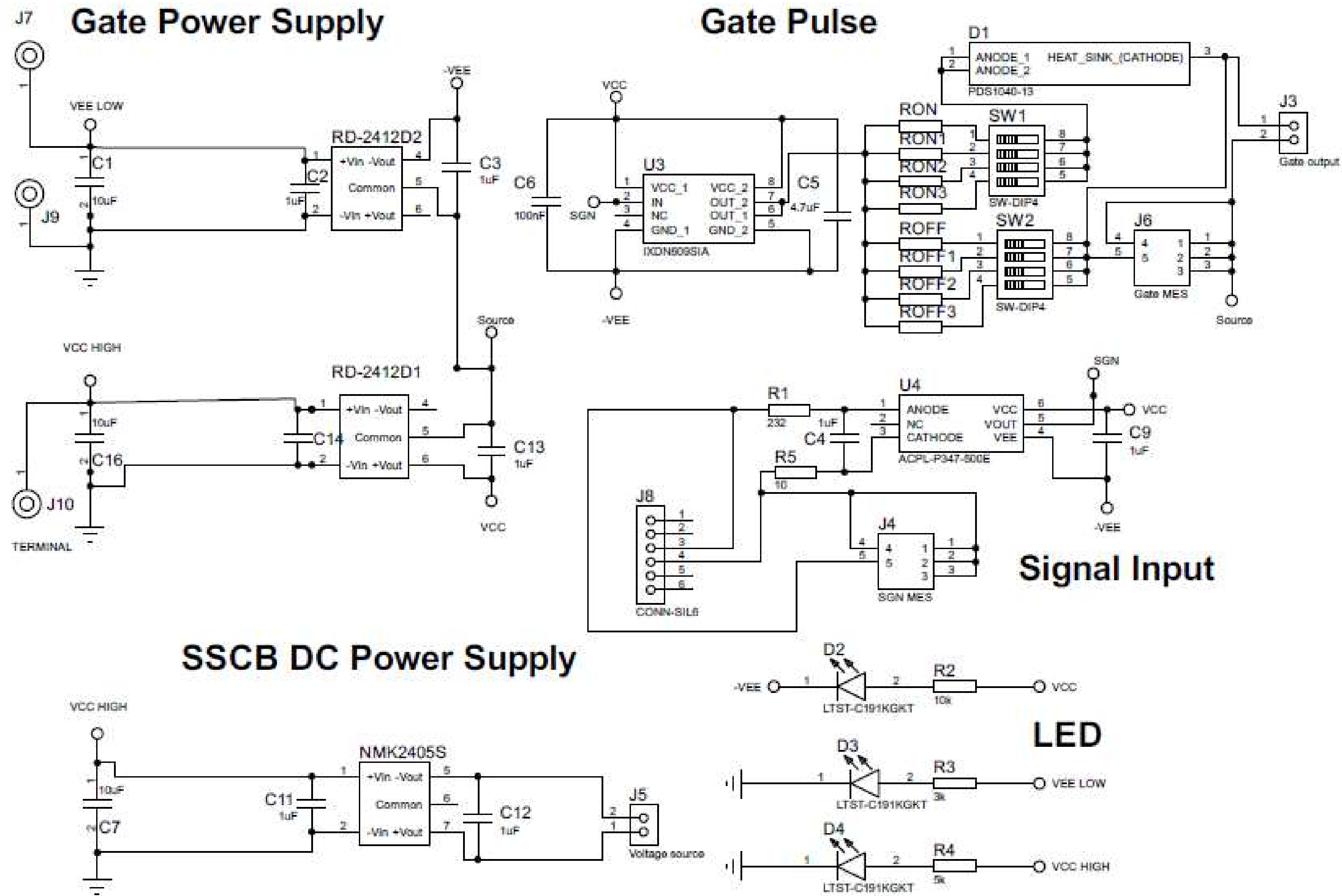
FC={cgs_FC} M={cgs_M} VJ={cgs_VJ} RS=0.2 .ENDS ujn1205k .SUBCKT IGATETOSOURCE 1 2 3 PARAMS: is0g=1.5000e-14 .param is0_tc=0.0000e+00 .param ngs=3.7100 ngs_tc=0.0020 .param xti=1.5e+01 .param egap=3.2600 .param egapt1=1.0000e+05 .param egapt2=3.3000e-02 .func ratio_t() {(TEMP+273.15)/(300)} .func vt() {1.38e-23*(TEMP+273.15)/1.602e-19} .func egap_t() {egap-(egapt2*((TEMP+273.15)*(TEMP+273.15)))/((TEMP+273.15)+egapt1)} .func is_t() {is0g*PWR(ratio_t(),(xti/ngs)) *EXP((ratio_t()-1)*(egap_t()/(ngs*vt())))} *.func IGS(vgs) {if(vgs<0, 0,is_t()*(EXP(vgs/(ngs*vt())) - 1))} .func IGS(vgs) {is_t()*(1)} G_GS 1 3 VALUE = {IGS(V(2,3))} . ENDS IGATETOSOURCE * JFET drain current .SUBCKT IDJFET Gate Drain Source PARAMS: beta=5.28 beta_tce=-30 vth=-7.892 vth_tc=4.0e-4	FC={cgs_FC} M={cgs_M} VJ={cgs_VJ} RS=0.2 .ENDS UJ3N120035K3SM .SUBCKT IGATETOSOURCEM 1 2 3 4 PARAMS: is0g=1.5000e-14 .param is0_tc=0.0000e+00 .param ngs=3.7100 ngs_tc=0.0020 .param xti=1.5e+01 .param egap=3.2600 .param egapt1=1.0000e+05 .param egapt2=3.3000e-02 .func ratio_t(Tj) {(Tj+273.15)/(300)} .func vt_t(Tj) {1.38e-23*(Tj+273.15)/1.602e-19} .func egap_t(Tj) {egap-(egapt2*((Tj+273.15)*(Tj+273.15)))/((Tj+273.15)+egapt1)} .func is_t(Tj) {is0g*PWR(ratio_t(Tj),(xti/ngs)) *EXP((ratio_t(Tj)-)*(egap_t(Tj)/(ngs*vt_t(Tj))))} *.func IGS(vgs,Tj) {if(vgs<0, 0,is_t(Tj)*(EXP(vgs/(ngs*vt_t(Tj))) - 1))} .func IGS(vgs,Tj) {is_t(Tj)*(1)} G_GS 1 3 VALUE = {IGS(V(2,3),V(4,3))} R_dummy 4 3 1G .ENDS IGATETOSOURCEM * JFET drain current .SUBCKT IDJFETM Gate Drain Source T PARAMS: beta=5.7 beta_tce=-30 vth=-9.2 vth_tc=4.0e-4

+ npow=1.4480 npow_tc=-5.0000e-04 lambda0=0.05 lambda1=-1.1000e-01	+ npow=1.4480 npow_tc=-5.0000e-04 lambda0=0.01 lambda1=-1.1000e-01
+ alpha=1.8000 alpha_tc=-3.0000e-03	+ alpha=1.8000 alpha_tc=-3.0000e-03
* Calculate Temperature Dependent Parameters	* Calculate Temperature Dependent Parameters
.func delta_t() {TEMP - 27}	.func delta_t(Tx) {Tx - 27}
.func beta_t() {beta*PWR(1.0001, beta_tce*delta_t())}	.func beta_t(Tx) {beta*PWR(1.0001, beta_tce*delta_t(Tx))}
.func vth_t() {vth * (1 + vth_tc * delta_t())}	.func vth_t(Tx) {vth * (1 + vth_tc * delta_t(Tx))}
.func npow_t() {npow * (1 + npow_tc * delta_t())}	.func npow_t(Tx) {npow * (1 + npow_tc * delta_t(Tx))}
.func alpha_t() {alpha * (1 + alpha_tc * delta_t())}	.func alpha_t(Tx) {alpha * (1 + alpha_tc * delta_t(Tx))}
* Calculate the terms of the ID equation	* Calculate the terms of the ID equation
.func vod(vgs) {if((vgs-vth_t()>0), (vgs-vth_t()),(vgs-vth_t()-1e-15))}	.func vod(vgs,Tx) {if((vgs-vth_t(Tx)>0),(vgs-vth_t(Tx)),(vgs-vth_t(Tx)-1e-15))}
.func npow_term(vgs) {PWR(vod(vgs),npow_t())} **(1+lambda1*vod(vgs))}	.func npow_term(vgs,Tx) {PWR(vod(vgs,Tx),npow_t(Tx))} **(1+lambda1*vod(vgs,Tx))}
.func lambda_factor(vds,vgs,vds_term) {if((vds_term>0), 1+lambda0*abs(vds)*(1+lambda1*vod(vgs)*0), 1+lambda0*abs(vds))}	.func lambda_factor(vds,vgs,vds_term,Tx) {if((vds_term>0), 1+lambda0*abs(vds)*(1+lambda1*vod(vgs,Tx)*0), 1+lambda0*abs(vds))}
.func tanh_term(vds,vgs) {tanh(alpha_t()*vds/vod(vgs))}	.func tanh_term(vds,vgs,Tx) {tanh(alpha_t(Tx)*vds/vod(vgs,Tx))}
.func IDSEQ(vds,vgs,vds_term) {if(vgs>vth_t(), (beta_t()*npow_term(vgs)*tanh_term (vds,vgs)*(lambda_factor(vds, vgs,vds_term))), 0)}	.func IDSEQ(vds,vgs,vds_term,Tx) {if(vgs>vth_t(Tx), (beta_t(Tx)*npow_term(vgs,Tx)*tanh_term (vds,vgs,Tx)*(lambda_factor(vds, vgs,vds_term,Tx))), 0)}

.func IDS(vds,vgs,vgd) {IF((vds>0), (IDSEQ(vds,vgs,vds)+ vds/5e6), - 0.8*(IDSEQ(-vds,vgd,vds)+ vds/5e6))} G_DS Drain Source VALUE = {IDS(V(Drain,Source),V(Gate,Source), V(Gate,Drain))} .ENDS IDJFET	.func IDS(vds,vgs,vgd,Tx) {IF((vds>0), (IDSEQ(vds,vgs,vds,Tx)+ vds/5e6), -0.8*(IDSEQ(-vds,vgd,vds,Tx)+ vds/5e6))} G_DS Drain Source VALUE = {IDS(V(Drain,Source),V(Gate,Source), V(Gate,Drain),V(T,Source))} R_dummy T Source 1G .ENDS IDJFETM

Appendix C: Schematic circuits and PCB layouts

Control board

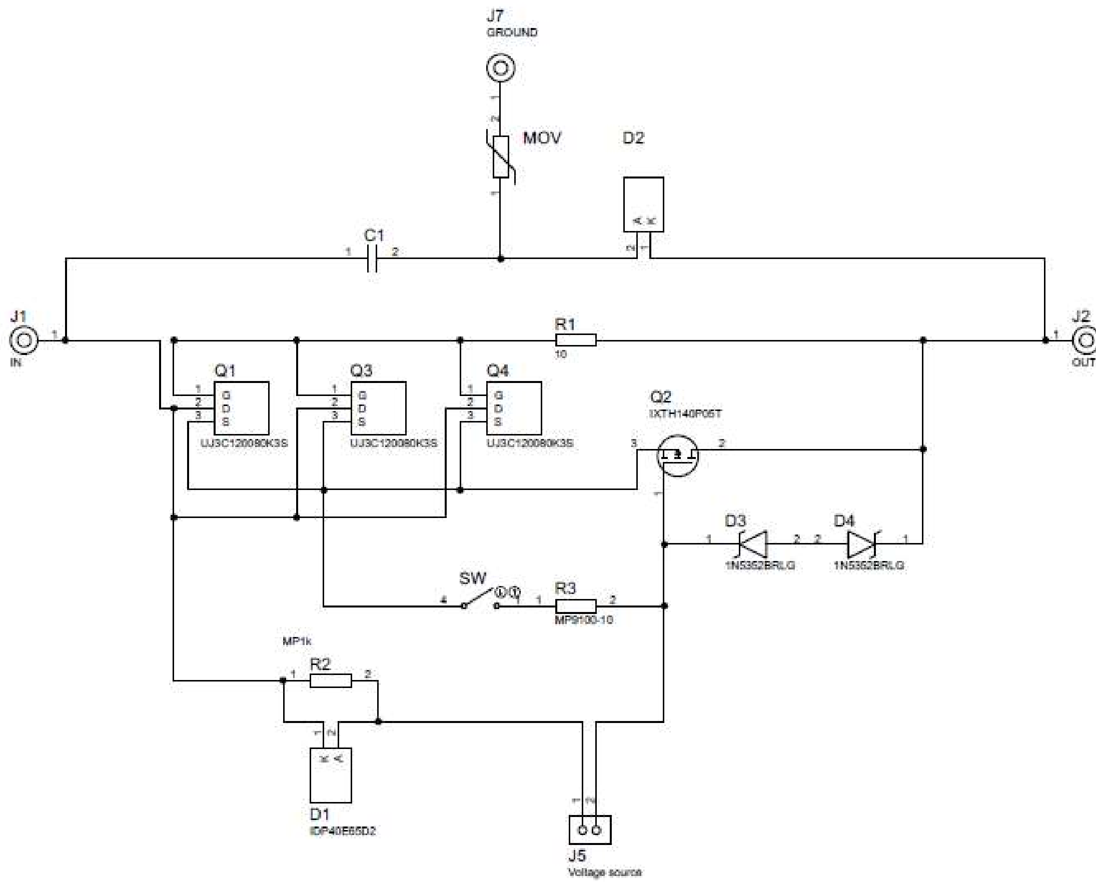


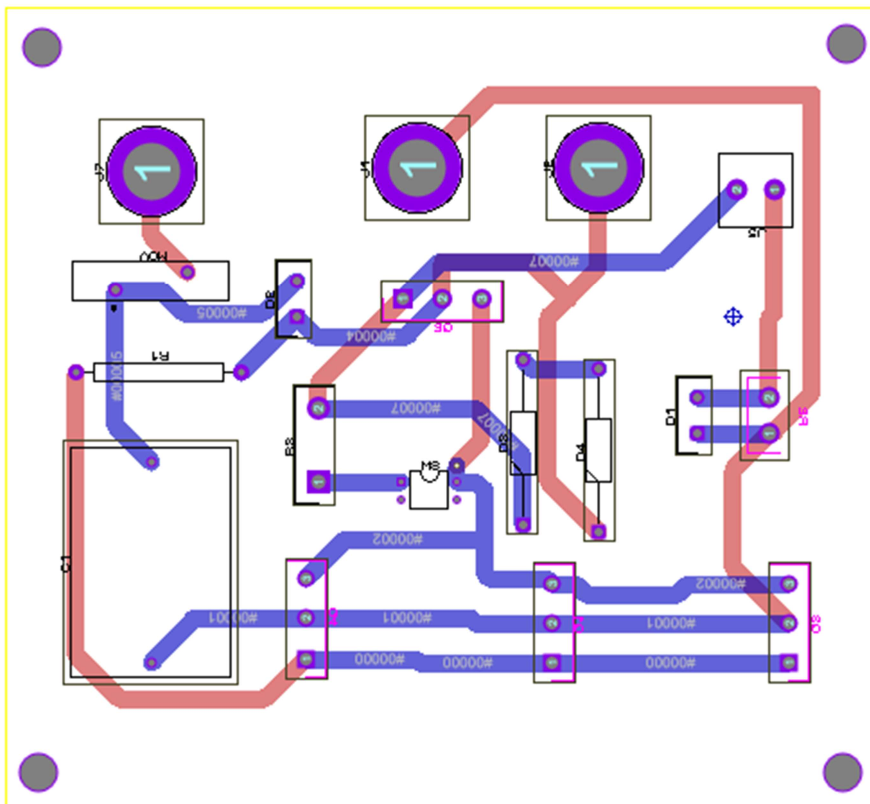
PCB layout

Bill of material

Item	Category	Quantity	References	Value	Part No
1	Capacitors	3	C1,C7,C16	10uF	
2	Capacitors	7	C2-C3,C9,C11-C14	1uF	
3	Capacitors	1	C4	1uF	
4	Capacitors	1	C5	4.7uF	
5	Capacitors	1	C6	100nF	
6	Resistors	1	R1	232	
7	Resistors	1	R2	10k	
8	Resistors	1	R3	3k	
9	Resistors	1	R4	5k	
10	Resistors	1	R5	10	
11	Gate Driver	1	U3		IXDN609SIA
12	Optocoupler	1	U4		ACPL-P347-500E
13	Diodes	1	D1		PDS1040-13
14	LED	3	D2-D4		LTST-C191KGKT
15	Jack terminal	1	J3		
16	BNC connector	1	J4		
17	Jack terminal	1	J5		
18	BNC connector	1	J6		
19	Jack terminal	3	J7,J9-J10		
20	Jack terminal	1	J8		
21	DC/DC converter	1	NMK2405S		NMK2405S
22	DC/DC converter	1	RD-2412D1		RD-2412D
23	DC/DC converter	1	RD-2412D2		RD-2412D
24	Gate resistor	8	ROFF,RON	10	
25	Mini Switch	2	SW1-SW2		SW-DIP4

SSCB board





Short-circuit board