# 

High Frequency Gate Driver Design for Gallium Nitride Power Devices

## By

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# A**bstract**

Increasing attention has been drawn to Gallium Nitride (GaN) based power devices, since its superior properties in comparison with Silicon counterparts. Gallium Nitride based power devices are very promising in a wide range application, such as battery chargers, point-of-load dc/dc converters, EV OBC and motor drives. GaN based devices exhibit a much lower specific ON resistance ( in comparison with Silicon counterparts. This enables a much smaller die size to a certain current capability, and thereby smaller input as well as output capacitances. The higher saturation velocity and lower capacitances allows fast switching transients. As a result, GaN based devices are capable of operating at a switching frequency around 10 times greater compared to current Silicon based MOSFETs. Therefore, Gallium Nitride device is expected as a candidate for next-generation power device in a near future. While, to make use of all advantages that GaN brings, there are numbers of issues need to overcome. For instance, soft switching technique, packing, gate driver, thermal management as well as converter topology.

This thesis is devoted towards the circuit design and associated application by using Gallium Nitride based power semiconductor devices. It will focus on the characterisation of selected GaN devices and related circuit design as well as the experimental verification. An overview of current power devices and its market is studied first, including overview of current power device market and future projection, comprehensive comparison among different trended power devices as well as key challenges faced by GaN-based devices.

This thesis also compares the difference between e-mode GaNFET and cascode GaNFET. Particularly, the insight characteristics of cascode GaNFET, which comprises unique features of cascode structure, switching transient analysis, switching loss mechanism, effect of parasitic elements. Furthermore, the importance of gate driving loop design of cascode GaN-based application has been addressed. Both SPICE-based simulation and experimental work are conducted for evaluation and verification purpose.

A synchronous buck converter is selected to further evaluate the influence of gate drive circuitry from efficiency perspective. A simulation model is implemented in synchronous buck converter to assess the impact of gate driving loop of cascode GaN device in both hard-switching (CCM) and soft-switching (CRM). Moreover, a prototype hardware with proposed gate driving loop design is presented. By applying the soft-switching and proposed gate driving loop design, the cascode GaN-based synchronous buck converter is demonstrated with 99.15% peak efficiency.

Lastly, this work analyses the specific requirement of d-mode device, such as isolated negative power supply and short-circuit protection. Two d-mode devices have been selected for evaluation purpose, namely, 650V SiC JFET and 1.2kV PSJ GaN HFET. Moreover, the PSJ GaN HFET is expected to be constructed in cascode configuration further to realise a novel high-voltage normally-off GaNFET. Therefore, it is necessary to deeply understand the technical challenge raised by d-mode devices. Accordingly, a protection scheme for normally-on device is proposed, which consists of desaturation scheme and negative power supply protection. The proposed scheme is initially implemented in Cadence Orcad for investigation purpose. A hardware prototype is also made to experimentally analyse the superiority of proposed protection scheme in comparison to state-of-the-art counterparts.

In conclusion, this work is concentrated on the evaluation of cascode GaNFETs. Parasitic effect, gate drive circuity and CRM soft-switching technique are addressed to fully making use of the potential of cascode GaN devices. Moreover, an ultra-fast-response protection scheme for d-mode WBG devices is introduced.

# Publication

1. Q. Tan and S. Madathil, "A Simple Approach to Improve the Switching Performance of Cascode GaNFETs," 2020 8th International Conference on Power Electronics Systems and Applications (PESA), 2020, pp. 1-5, doi: 10.1109/PESA50370.2020.9343953.
2. Q. Y. Tan and E. M. S. Narayanan, “Evaluation of gate drive circuit effect in cascode GaN-based applications,” *Bull. Polish Acad. Sci. Tech. Sci.*, vol. 69, no. 2, pp. 1–7, 2021, doi: 10.24425/bpasts.2021.136742.
3. Tan, Q., et al., “An ultra-fast protection scheme for normally-on wide bandgap devices,” *IET Power Electron.* (2021), 1– 9. <https://doi.org/10.1049/pel2.12179>.

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# List of Symbols

|  |  |
| --- | --- |
|  | Gate driver parasitic capacitance |
|  | Speed-up capacitor |
|  | Input capacitance |
|  | Input-output capacitance |
|  | Output capacitance |
|  | Reverse capacitance |
|  | Turn-on switching loss |
|  | Turn-off switching loss |
|  | Drain current |
|  | Gate parasitic inductance |
|  | Drain parasitic inductance |
|  | Source parasitic inductance |
|  | Gate driver parasitic inductance |
|  | Gate charge |
|  | Gate-drain charge |
|  | Gate-source charge |
|  | Reverse recovery charge |
|  | Specific on-resistance |
|  | On-resistance |
|  | Gate driver high-side on-resistance |
|  | Gate driver low-side on-resistance |
|  | Output resistance of gate driver |
|  | Gate resistor |
|  | Gate external series resistor |
|  | Internal gate resistance of the device |
|  | Turn-on gate resistor |
|  | Turn-off gate resistor |
|  | Rising propagation delay |
|  | Falling propagation delay |
|  | Rise time |
|  | Fall time |
|  | Propagation delay skew |
|  | Bus voltage |
|  | Drain-source voltage |
|  | Gate-source voltage |
|  | Allowed maximum gate voltage |
|  | Lower threshold of input |
|  | Higher threshold of input |
|  | Input voltage |
|  | Output voltage |
|  | Gate threshold voltage |

# List of Abbreviations

|  |  |
| --- | --- |
| 2DEG | Two-dimensional electron gas |
| AC | Alternating current |
| BOM | Bill of materials |
| BPS | Bi-directional power switch |
| BS | Bottom switch |
| CAGR | Compound annual growth rate |
| CCM | Continuous conduction mode |
| CMOS | Complementary metal-oxide-semiconductor |
| CMTI | Common-mode transient immunity |
| CRM | Critical conduction mode |
| CSI | Common source inductance |
| CV | Capacitance voltage |
| d-mode | Depletion mode |
| DBC | Direct bond copper |
| DC | Direct current |
| DUT | Device under test |
| DPT | Double pulse test |
| DT | Dead time |
| e-mode | Enhancement mode |
| EMI | Electromagnetic interference |
| EPC | Efficient Power Conversion Corporation |
| EV  FOM | Electric vehicle  Figure of merit |
| FP | Field plate |
| GaAs | Gallium Arsenide |
| GaN | Gallium Nitride |
| GaNFET | Gallium Nitride field-effect-transistor |
| GND | Ground pin |
| HEMT | High electron mobility transistor |
| HFET | Hetero-structure field-effect-transistor |
| HV | High voltage |
| IoT | Internet of things |
| IC | Integrated circuit |
| IV | Current voltage |
| JFET | Junction gate field-effect-transistor |
| LOP | Light output |
| LV | Low voltage |
| MOSFET | Metal-oxide-semiconductor field-effect-transistor |
| OBC | On-board charger |
| PCB | Printed circuit board |
| PFC | Power factor correction |
| PSJ  PSU | Polarization super junction  Power supply unit |
| PWM | Pulse width modulation |
| R&D | Research and development |
| RF | Radio frequency |
| RMS | Root mean square |
| SMPS | Switch mode power supply |
| SiC | Silicon Carbide |
| Si | Silicon |
| SJ | Super junction |
| SPICE | Simulation program with integrated circuit emphasis |
| TI | Texas Instruments |
| TS | Top switch |
| TTL | Transistor–transistor logic |
| UPS | Uninterruptible power source |
| UVLO | Under voltage lock out |
| VSI | Voltage source inverter |
| WBG | Wide band gap |
| ZCS | Zero current switching |
| ZVS | Zero voltage switching |

# Ch**apter 1: Introduction**

This chapter presents background and motivation, objectives and overview of this thesis. It will start from the background of current power semiconductor market to the expectation of GaN based power devices as well as GaN devices’ merits. Moreover, the comparison between three dominant semiconductor materials will be addressed in this chapter.

## 1.1: **Overview of Power Semiconductor Devices**

The first semiconductor device, namely, Silicon transistor was first introduced in 1950s. By far, the Silicon based device is still dominating current power electronics market. Among various power semiconductor devices, the power Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is the most common power device around the world, ascribed to its low gate drive power, robustness, easy biasing, wide bandwidth as well as fast switching speed. With time goes, power semiconductor device become an indispensable part of our daily life. The main power semiconductor devices and related applications with respect to operating power and switching frequency as depicted in Fig.1.1.1 [1].

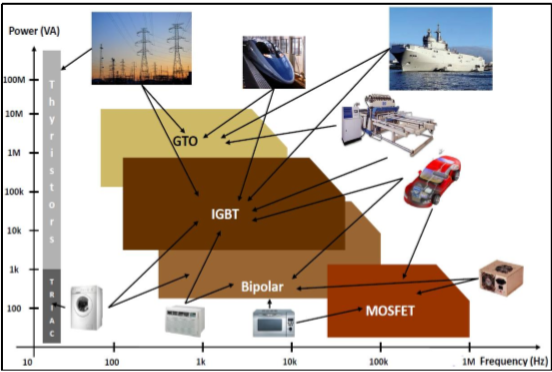


Figure 1.1.1: Power semiconductor devices and applications [1]

The power semiconductor market is projected to continue growing at a CAGR of 4% in upcoming 5 years [2]. While, due to limited number of vendors and global shortage of Silicon, the demand in power semiconductor device exceeds the factory capability. In the meantime, there are numbers of trending applications/technologies, such as electric automotive and 5G technology.

By far, the Silicon based device is still the majority in power semiconductor market. Unfortunately, the Silicon has almost ran out of its potential due to the Si technology is relatively mature and being restricted by its physical properties and theoretical limits. In the meantime, Silicon based devices seems not the ideal candidate for medium/high voltage (>400V) power devices as compared to the growth they provided toward low voltage power devices. This is due to low power efficiency at high voltage, lower quality, lesser reliability as well as instability of Silicon in coping with high voltages of electricity. Especially, Silicon based devices cannot realise high efficiency in some applications, such as PFC, power amplification, and power rectification when the voltage goes high. Therefore, to pursue higher power density and higher efficiency, the development and exploration in wide-bandgap (WBG) material-based power devices become indispensable. To date, there are two emerging WBG material platforms, Gallium Nitride (GaN) and Silicon Carbide (SiC). GaN based transistors and SiC based transistor are expected to be favourable candidates for high frequency and high efficiency power conversion applications ascribed to their advanced features. Both GaN and SiC based devices have demonstrated their superiority in terms of power efficiency, reliability and flexibility in comparison with pure Silicon based devices [3].

As a representative, the GaN-based Radio-Frequency (RF) market is predicted to continue soaring at an average rate of 20% and exceed US$ 2 billion by 2025 as depicted in Fig.1.1.2 [4]. GaN has been greatly adopted by the industries due to its higher power density, higher frequency and smaller footprint. GaN becomes a serious competitor to LDMOS and GaAs in RF application field recently, due to continuous development and reliability at lower cost. With 5G coming, the significantly increasing demands of power semiconductor devices is inevitable. Because of implementation of 5G networks, there is a strong surge will occur in forthcoming few years, and GaN RF market will be 3-4 times larger by 2024 in comparison to that of 2017 [5]. GaN-based device is very attractive and being assumed as a promising candidate in this huge market in the near future.

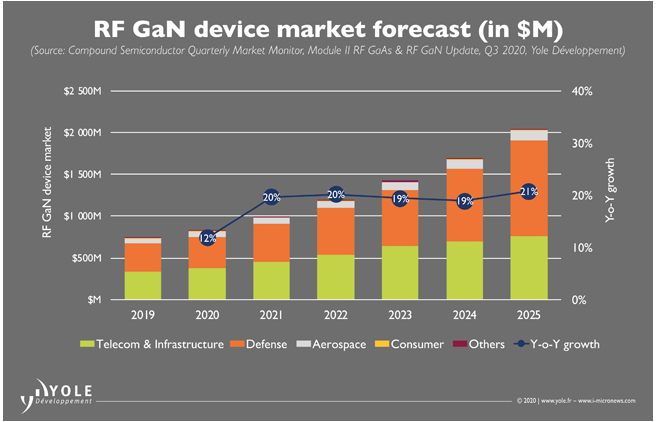


Figure 1.1.2: Market forecast for RF GaN device [4]

## 1.2: Overview of GaN Devices

The global Gallium Nitride (GaN) device market size reached US $1.44billion in 2019 and is anticipated to continue expand at a CAGR 19.8% from 2020 to 2027 [6]. The growth of GaN market can be attributed to the soaring demand for power electronics because of their attractive nature, such as notably low power consumption while relatively high efficiency. GaN-based devices introduce dynamic electrical properties, like high critical electric field, high saturation velocity as well as high thermal conduction. Ascribed to such superior properties, GaN has been presumed as an ideal choice for use in vast power devices. Meanwhile, the use of GaN-based power semiconductor device can achieve the reduction in both switching and conduction losses, and therefore an improved efficiency in power electronic systems become feasible. At present, the key players who are operating in the GaN semiconductor device market comprise GaN Systems, Inc., Efficient Power Conversion Corporation, Inc. (EPC), NXP Semiconductor N.V., Toshiba Corporation, Fujitsu Ltd., Cree, Inc., Texas Instruments, Inc. (Ti), Transphorm Inc., Navitas Semiconductor Inc., and Qorvo, Inc. Table 1.1 shows some of current available GaN devices with a voltage range from 30-900V, and a current range from 15-90A.

**Table 1.1: Several available GaN devices in the market (all data based on 25 °C unless specified)**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Manufacturer | Part No | Vds/V | Id/A | Qg/nC | Rds\_on/mΩ | FOM/mΩ•nC |
| GaN System | GS61008P | 100 | 90 | 8 | 7 | 56 |
| GS66516T | 650 | 60 | 14.2 | 25 | 355 |
| GS-065-080-1-D | 650 | 80 | 16 | 18 | 288 |
| Transphorm | TP65H035WS | 650 | 46.5 | 24 | 35 | 840 |
| [TP90H050WS](https://www.transphormusa.com/en/product/tp90h050ws-2/) | 900 | 50 | 15 | 50 | 750 |
| Efficient Power Conversion | EPC2023 | 30 | 90 | 19 | 1.15 | 21.85 |
| EPC2022 | 100 | 90 | 13 | 2.4 | 31.2 |
| EPC2034C | 200 | 48 | 11.1 | 6 | 66.6 |
| Panasonic | PGA26E06BA | 600 | 31 | 32 | 56 | 1792 |
| Infineon | [IGO60R070D1](https://www.infineon.com/cms/en/product/power/gan-hemt-gallium-nitride-transistor/igo60r070d1/) | 600 | 31 | 5.8 | 70 | 406 |

Among the worldwide GaN market, the North America (NA) play a dominant role in 2019 with more than 33% market share. The main growth in NA area is due to the rising investments in defense and aerospace sector in R&D. meanwhile, the government in NA is accelerating the adoption of energy-efficient power devices and offering corresponding contracts to a variety of companies/manufacturers operating in this continent. On the other hand, Asia Pacific (AP) has been expected to the most emerging region as rapid technical advancements that gives rise to expanded demand with regards to efficient, high performance RF components. Countries in this region, such as China and Japan have a number of large-scale manufacturers in term of consumer electronics, like smart phones, LED/OLED display device, mobile charger as well as gaming consoles. All of these directly affect the regional market and lead to significant growth in Asia Pacific. Like North America, countries such as China, India, and North Korea are increasing their budget in defense/aerospace field, which result in rising demand for robust communication devices. As 5G coming, a substantial increase with respect to the adoption of wireless electronic device and tele-communication infrastructure are expected to further drive the growth of regional market.

### 1.2.1: **Comparison of Si, SiC and GaN Devices**

The first GaN-based device was designed as RF amplifier in 2004 [7]. Although, the GaN-based power devices are still in the early stage, the figure of merit (FOM) has been improved significantly by unremitting development and exploration in recent years. Nowadays, the GaN devices have far better performance in comparison with the state-of-the-art Si MOSFETs. For example, GaN become a strong rival to existing technologies [8].

The advantage of GaN-based power devices derives from the intrinsic material properties of GaN in comparison to other primary semiconductor material, like Silicon (Si) and Silicon Carbide (SiC). The detailed key parameters of different material comparison among Si, 4H-SiC and GaN as shown in Table 1.2 and Fig. 1.2.1. All of these three materials are considered as the success candidate in power electronics field [7][9].

**Table 1.2: Intrinsic Material key parameters comparison between Si, 4H-SiC and GaN** [10]– [12]

|  |  |  |  |
| --- | --- | --- | --- |
| Properties | Si | 4H-SiC | GaN |
| Bandgap () | 1.12 | 3.26 | 3.39 |
| Breakdown Filed () | 0.3 | 2.2 | 3.3 |
| Saturated Drift Velocity () | 1.0 | 2.0 | 2.5 |
| Electron Mobility () | 1500 | 650 | 2000 |
| Thermal Conductivity ( | 3.8 | 1.5 | 1.3 |
| Baliga’s FOM ( | 1 | 488 | 2414 |

|  |
| --- |
| Figure 1.2.1: Material properties comparison between Si, 4H-SiC and GaN [13] |

Different from Si, both SiC-based and GaN-based devices are known as Wide Bandgap (WBG) devices, due to both materials exhibit significant higher band gap energy in comparison to Si-based devices. In general speaking, semiconductor materials’ band gap stands for the strength of the chemical bonds between atoms within the lattice. The higher the band gap, the more energy required for one electron jump from one site to another. In another words, higher band gap materials are more stable in term of lattice structure. This means that the power semiconductor devices those using high band gap material normally have lower leakage current and higher operation temperature, which will be beneficial to many power electronics system design.

Regarding to another key parameter, namely, critical electric field (), which is also in relationship with chemical bonds of the material. The stronger bonds, the higher critical electric field. The typical equation 1.1 shows the relationship between critical electric field, drift region width (, and breakdown voltage (. In accordance with this equation, the breakdown voltage is proportional to the drift region width as well as the critical electric field. This equation also demonstrates that with a given breakdown voltage, the WBG-based devices such as SiC and GaN devices are able to achieve 10 times smaller drift region width in comparison to Si-based devices.

(1.1)

Another equation 1.2 further proves the superiority of the WBG materials. This equation introduces the relationship between critical electric field and concentration carrier in the drift region for a given amount of electrons. In this equation, q stands for the charge of an electron, is the number of electrons, and and stand for vacuum permittivity and material relative permittivity respectively.

(1.2)

As shown in the equation 1.2, it is obvious that WBG-based power devices have strong potential to enable a significant better performance at high frequency operation compared to Si-based device. Since if the critical electric field is 100 times higher, the drift region wide is 100 times smaller, hence the total electron number become 10000 times higher.

As well-known, the one of the most important objectives for a power semiconductor device is on-state resistance (, and the on-state resistance can be expressed as equation 1.3, where is the mobility of electrons.

(1.3)

Deriving from above three equations, the relationship between breakdown voltage, critical electric field and electron mobility can be expressed as shown in equation 1.4. according to equation 1.4, it is easy to find out a higher critical electric field and electron mobility is able to attain relatively smaller on-state resistance for a given breakdown voltage.

(1.4)

The three candidates’ theoretical on-resistance can be calculated from equation 1.4. Three solid lines in Fig.1.2.2 depict the theoretical limit for Si, SiC and GaN. As aforementioned, Si technology has been well-developed and relatively mature through last few decades, thus the current Si MOSFET is very close to its ideal limit. As reported in [14], the advanced Si super junction (SJ) MOSFET exceed the Si’s theoretical limit. It is possible to push Si-based devices even further. Unlike Si-based devices, GaN-based devices are still in early stage and far below the GaN material limit. According to Fig.1.2.2, GaN deivces feature much higher theoretical limit than Si and SiC. For instance, GaN-based device is possible to attain 10 times smaller specific on-resistance in comparison to that of SiC at 600V-class as drawn in Fig. 1.2.2. Navitas Semiconductor as one of the pioneer in GaN field has demonstrated their GaNFET can switch up to 40MHz, which is way beyond than any state-of the-art Si technology [15]. Therefore, GaN power devices have very strong potential to develop and investigate. Moreover, the 650V GaN device shows significant advantage in term of gate charge (Qg) as illustrated in Fig. 1.2.3, which means GaN device is able to achieve lower switching loss as well as faster switching speed for given voltage/current rating.

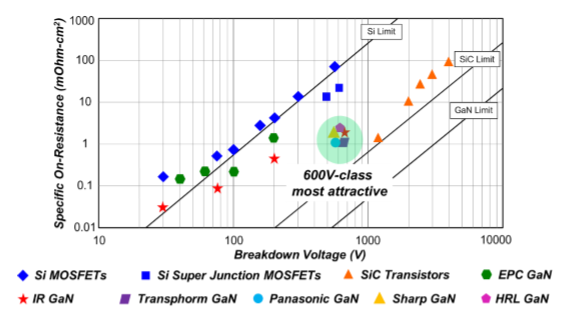


Figure 1.2.2: Theoretical specific on-resistance limits of Si, SiC and GaN vs breakdown voltage [16]

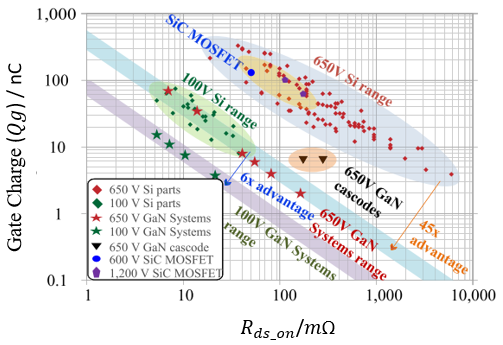


Figure 1.2.3: Gate charge vs on-resistance of Si, SiC and GaN devices [17]

With respect to SiC semiconductor devices, they are more expensive compared to GaN. Meanwhile, the supply chain restriction is another key issue to extensive use. For instance, SiC-based devices are unable to satisfy the increasing demand of electronic vehicle (EV) manufacture [18]. The SiC-based Schotty diode was the first commercialised SiC device, which is released by Infineon in 2001. The SiC diode does not have reverse recovery charge owing to it is a majority carrier device [19]. Furthermore, SiC diode exhibits a higher forward voltage drop (Vf) in comparison to that of Si because of larger bandgap energy and hereby higher conduction loss. Whereas, the forward voltage drop has a positive temperature coefficient and therefore making SiC diode suitable for paralleling connection [20]. On the other hand, the first commercial SiC JFET and SiC MOSFET were unveiled by SemiSouth and Cree in 2008 and 2011 respectively [21][22]. SiC power devices are mainly designed for high voltage and high temperature applications, because SiC material not only has high bandgap but also exhibit much higher thermal conductivity, which perfectly meets the high temperature operation requirements. SiC technology exhibits inescapable restrictions with respect to its maximum exploitation because shortage of appropriate package for SiC-based devices [23].

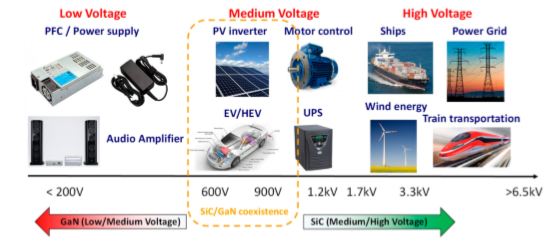


Figure 1.2.4: Possible application for GaN and SiC device as a function of voltage [24]

With respect to GaN-based devices, they can be seen as complementary to that of Si and SiC, since they are principally suitable for low/mid-range voltage requirement. In particular, GaN-based devices exhibit great potential in terms of achieving the reduction in weight and volume of the power devices. Possible applications using GaN and SiC device are shown in Fig. 1.2.4 [24]. According to [18], it mentions two reasons for customer will move from SiC toward GaN. Which can be concluded as following: limited materials and rising expense. When volumes increase, prices decrease, GaN devices are projected to offer competitive price in comparison to Si devices over time. Due to most of current commercially available GaN devices are using Silicon wafer/substrate, resulting in the further reduction in the price of GaN devices. The first GaN-based fast charger for mobile was unveiled in 2019 by OPPO, which enables 65w ultra-fast charging rate in comparison to contemporary counterparts ranging from 20w to 40w. Meanwhile, Navitas semiconductor recently announced that more than 50 GaN-based fast charging products and platforms are available in the market, realising wall chargers ranging from 24w up to 300w [25]. As said in [18], GaN deivce realises three times lower switching loss than SiC counterparts at 650V voltage level. The first generation GaN devices made by GaN Systems outperform recent fifth generation SiC devices. Additionally, e-mode GaN devices exhibit zero reverse-recovery charge and ultralow output charge (). Therefore, GaN will gain advantage in hard switching half-bridge design, since reverse-recovery charge will contribute to losses in such topology. GaN devices have lowest output charge in comparison to Si and SiC, which is beneficial to achieve soft switching operation. GaN has drawn increasingly international attention from both cost-effective manner and potential ability prospective. Overall GaN semiconductor device market is anticipated to grow to US$22.5 billion as shown in Fig.1.2.5 [26].

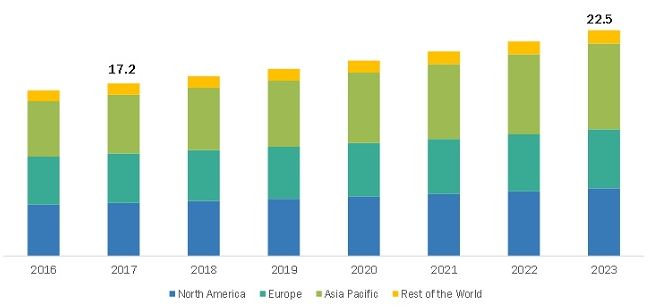


Figure 1.2.5: Projection of GaN semiconductor device market, by region (USD billion) [26]

### 1.2.2 Challenges of GaN Devices

As discussed above, there is no doubt that GaN-based devices have better parameters in comparison to current dominant Si-based devices. To fully make use of advantages that GaN brings, it is very important to comprehend and understand the technical challenges raised by GaN [27]. From this point of view, the key challenges can be addressed as following three aspects: switching characteristics, influence of package as well as dedicated gate driver owing to compared to Si and SiC, GaN is more ideally suited for high frequency, high efficiency power electronics.

Regarding to the switching behaviour, GaN devices exhibit relatively fast switching feature, and thereby the parasitic ringing/oscillation will be even more severe under hard switching operation in comparison with Si counterparts. Fig 1.2.6 shows GaN device turn-on transient under hard switching condition. Such ringing/oscillation results in significant losses and Electromagnetic Interference (EMI) noise, which is undesirable for circuit design.

|  |
| --- |
| (a) |
| (b)  Figure 1.2.6: TPH3205WSB turn-on transient under hard switching of (a) versus ; (b) versus |

This work mainly focuses on cascode GaN device, and the cascode GaN device has unique switching behaviour as there are two discrete switches integrated into one single package. The major benefits of the use of cascode structure fall into following categories: Firstly, the use of LV Si MOSFET ensures the gate structure become more robust, also lifts up the gate threshold voltage of the cascode GaN device compared to that of e-mode GaNFET. Secondly, the cascode GaN device realises an enlarged the gate driving voltage safety margin. Furthermore, the cascode structure enables an integrated body diode with ultralow forward voltage drop. All of abovementioned benefits are helpful to improve noise immunity and ease the complexity of gate drive design. The interaction between LV Si MOSFET and HV GaN HEMT might cause unwanted features. For instance, the HV d-mode GaN HEMT unable to turn on at zero voltage internally during soft switching turn-on process, Si MOSFET reach its avalanche breakdown during switching off transient. As a worst case, the cascode GaN device might suffer divergent ringing/oscillation when the device current switching off at high current condition [28]. These unwanted features should be taken into account during study and design to enhance the switching performance and prevent failure.

According to [29]–[31], the effect of device packing has been addressed for all three aforementioned materials Si, SiC and GaN. Especially, GaN-based power devices are targeted at high frequency, the parasitic elements within the package could resist the switching transition and even cause significant oscillation/ringing, which may result in device failure [32][33]. Among all the parasitic elements within the device package, the common source inductance (CSI) has significant influence in terms of switching loss. The detailed analysis will be addressed in Chapter 2. The cascode GaN devices are different from the pure enhancement-mode GaN, which consist of two discrete dies within one package. It is very necessary to study and investigate the internal parasitic inductance and the interaction between two devices within cascode GaN package to minimise switching loss, reduce parasitic oscillation and ringing, and achieve better switching performance eventually.

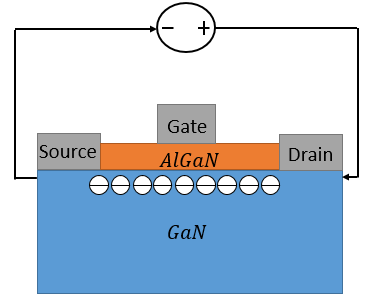
Due to the superiority of GaN, the GaN-based power devices exhibit significant smaller gate charge and output capacitance in comparison to Si-based counterparts. Hence, even GaN technology is still premature, it is very easy to find out that and of current commercial GaN device can be much higher (3-5 times) than that of Si devices [28].

The effect of and can be described as following: can couple any parasitic capacitance from switching node toward ground. This might affect the input PWM signal and lead to false switching events; while can combine with the common source inductance (CSI), and induce an opposite voltage drop across this inductance, which will reduce the effective gate driving voltage for both turn-on and turn-off events.

All the issues mentioned above should be carefully studied and taken into consideration for all circuit design, to prevent undesired events occur and not let these issues becoming the limiting factor.

## 1.3: Normally-off Enhancement Mode GaN and Normally-on Depletion Mode GaN

The fundamental structure of GaN device as shown in Fig.1.6, consisting of the two-dimensional electron gas (2DEG) along with the boundary of the AlGaN-GaN layers. The 2DEG is formed owing to the higher bandgap of AlGaN allows free electrons to diffuse from AlGaN toward the lower bandgap GaN near the interface. The electrons in 2DEG exhibit extremely high mobility and high conductivity, and hereby produce relatively small on-resistance [9]. The conventional GaN high-electron-mobility transistor (HEMT) is based on this concept. Generally, GaN devices can be classified into enhancement –mode (e-mode) and depletion-mode (d-mode) in term of gate structure prospective.



7Figure 1.3.1: Fundamental GaN device structure and its piezoelectric property

The conventional GaN HEMT is a depletion-mode device, which shows a naturally ON characteristic. The d-mode GaN device is more nature based on its crystal hexagonal structure, which is referred as wurtzite. Fig. 1.3.1 illustrates the basic structure of depletion mode GaN deivce. The depletion mode GaN device is a naturally ON if there is no gate-to-source voltage applied. A negative gate-to-source voltage is required to turn off the device, which is inconvenient and undesired for most circuit design.

|  |  |
| --- | --- |
|  | |
| (a) | (b) |

8Figure 1.3.2: Depletion-mode GaN device structure (a) ON state; (b) OFF state

Significant efforts have been made by researchers in order to achieve preferred normally-off operation. The e-mode (also referred as normally-off) GaN device can be made by utilising some sophisticated techniques, such as recessed gate [34], implanted gate [35] and p-GaN gate [36]. The basic structure of enhancement-mode GaN device as shown in Fig. 1.3.2. Different from the depletion-mode GaN device, the enhancement-mode GaN device is naturally OFF if there is no external gate-to-source voltage applied. A positive Vgs is required to switch on the e-mode GaN device. The e-mode GaN devices using above mentioned techniques have a common problem, which is the safety margin for gate driving voltage is relatively narrow (around 2V) [37]–[39]. A dedicated gate driver is vitally important for such e-mode GaN devices.

|  |  |
| --- | --- |
|  | |
| (a) | (b) |

9Figure 1.3.3: Enhancement-mode GaN device structure (a) ON state; (b) OFF state

|  |
| --- |
|  |
| (a) |
|  |
| (b) |

10Figue 1.3.4: I-V characteristics of (a) depletion-mode GaN device; (b) enhancement-mode GaN device

In order to further investigate into depletion-mode and enhancement-mode GaN device, Fig. 1.3.4 is drawn. According to Fig. 1.3.4, both d-mode and e-mode GaN devices are capable of bidirectional current flowing due to physical structure of GaN device. Major difference between d-mode and e-mode GaN device is the gate-to-source voltage applied on each curve. In the scenario drawn in Fig. 1.3.2 (a), the threshold voltage of this d-mode GaN device is -22V. Therefore, to turn this device off, a negative voltage below -22V is required. Regarding to the E-mode GaN device in Fig. 1.3.2 (b), the threshold voltage of this E-mode GaN device is 1.7V. Thus, the device will remain in OFF state if 0V applied to Vgs. A more detailed property of GaN device can be observed from I-V characteristics. Taking e-mode GaN used in Fig. 1.7 as an example: when Vgs is 0V, the device remains in off state before avalanche in first quadrant, while in third quadrant, the device starts conducting as long as Vds become -1.7V or lower. It is because GaN device symmetric lateral structure gives rise to same threshold voltage in both forward and reverse conduction. The reverse conduction mechanism for depletion-mode GaN device is similar to e-mode GaN device, which can be found in Fig. 1.3.4. With regards to cascode GaN device, it has a different mechanism of 3rd quadrant operation from e-mode GaN device. Table 1.3 shows the key parameters comparison of 3rd quadrant operation of e-mode GaN device and cascode GaN device. The detailed 3rd quadrant operation of cascode GaNFET and associated equation will be addressed in Chapter 2.1.

3**Table 1.3**: **Key parameter in 3rd quadrant comparison of e-mode GaN device and cascode GaN device @ 650V level**

|  |  |  |
| --- | --- | --- |
| Parameter | e-mode GaN  (GS66508B) | Cascode GaN  (TP65H050WS) |
| Maximum transient protection/V | 750 | 800 |
| Gate driving voltage safety margin /V | 1 | 10 |
| Gate threshold voltage/V | 1.7 | 4 |
| Reverse conduction operation ( | 6-9 | 1.3-1.8 |
| Gate charge (Qg)/nC | 6.1 | 16 |
| Reverse transfer capacitance (Crss)/pF | 1.5 | 19 |
| Reverse recovery charge (Qrr)/nC | 0 | 125 |
| Reverse recovery time ()/ns | 0 | 30 |
| On-resistance ()/mꭥ | 50 | 50 |

It is worth to point out the turn-off process of e-mode GaNFET and cascode GaNFET are different. Fig. 1.3.5 shows both e-mode GaNFET and cascode GaNFET equivalent circuit for comparison purpose. Regarding to an e-mode GaNFET, the inductor current flows and charges the reverse capacitor (CGD), which is also referred as miller capacitor, during turn-off. Therefore, this charging current directly affects the external gate driver. As shown in Fig. 1.3.5(a), this current has same direction with respect to the driving current to switch off the device. Therefore, the current charging miller capacitance flows into the gate drive circuitry, which further reduce the gate discharging current. As a result, the miller capacitor current weakens the driving capability of the external gate driver and results in a miller plateau with relatively high turn-off loss (Eoff), so-called miller effect [40].

With respect to a cascode GaNFET, the inductor current is charging the miller capacitors of the d-mode HV GaN device which is provided by the power loop. It is worth pointing out that such inductor current is much larger in comparison with external gate driving current and it can be assumed as a constant current source, which directly flowing out of the device as illustrated in Fig. 1.3.5(b). Thus, the charging current will not affect the external driver when using cascode GaNFETs. The miller capacitor is simply charged by a current source and thereby the gate driver is able to switch off the device very quickly, which is totally depending on the driving capability of the gate driver. Consequently, the turn-off loss of cascode GaNFET can be ultralow and not sensitive to the turn-off current [28].

|  |  |
| --- | --- |
|  |  |
| (a) | (b) |

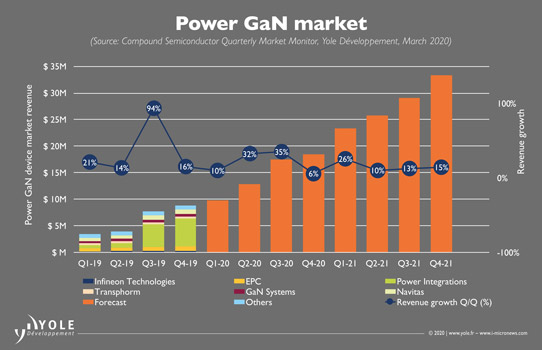
11Figure 1.3.5: Turn-off equivalent circuit of (a) e-mode GaNFET; (b) cascode GaNFET

It has to be mentioned that the reverse conduction of GaN power device is different from traditional Si devices. For a Si MOSFET, it consists of a built-in body diode from source to drain. Hence, once a positive voltage (Vsd) is applied across this body diode, the device is able to conduct even without gate-to-source voltage applied, and the device behaves like a normal diode. While, with respect to GaN HEMT, the body diode does not exist. The lateral structure of GaN HEMT (symmetric from both drain and source terminal) guarantee the reverse conduction capability in a different mechanism in comparison with Si MOSFET. The GaN HEMT can be turned on by applying a positive voltage greater than threshold voltage (Vth) on either gate-to-source or gate-to-drain. Consequently, in third quadrant, the device will be able to turn on if Vgd higher than the threshold voltage. Conduction loss of GaN device could be a serious concern for certain circuit design, it is because GaN device does not have body diode and the current increases significantly while the voltage drop across source-to-drain terminal only increases a little during reverse conducting. This results in a dramatically higher conduction loss than Si MOSFET, in which reverse conduction with off state gate-source voltage, such as synchronous rectifier during dead time. According to [41][42], such issue can be resolved.

## 1.4: Emerging GaN-based Applications

GaN devices are now very promising in many fields due to its better figure of merits (FOM) in comparison with Si MOSFET. Besides traditional radio frequency (RF) market, GaN-based devices stand out in many other fields, such as power supplies, adapters, battery chargers as well as EV. Among these applications, the mobile charger is the most representative applications with respect to GaN device [25][43][44]. Meanwhile, the GaN devices are emerging in applications, such as motor drive [45][46], power factor correction [47][48], and point-of-load (POL) converter [49]. Moreover, GaN-based devices realize different applications, which are previously not feasible by using Si MOSFETs. For instance, high frequency wireless power transfer [50] and LiDAR [51].

GaN power device market is currently dominated by radio frequency (RF) power devices, including radio, TV broadcast, radar, and satellite communication etc. The uses of GaN power device are motor control, power supplies, wireless charging and hybrid/EV battery. Fig. 1.4.1 shows the current GaN power device market as well as further expectation [52]. Among the increasing GaN power device market, GaN-based charger/adapter is one of the most promising products in terms of both volume and revenue. There are lots of Tech-companies unveiled GaN-based charger/adapter recently, such as RAVPower, AUKEY, Anker, OPPO, Xiaomi. GaN-based adpter/charger has reached $9 billion by 2018, and it is projected to keep growing in the future, due to increasing demand with regards to smartphones, tablets, Bluetooth earphones and enormous other emerging consumer electronics. As reported in [53], GaN-based adapter is able to achieve 25 power density, which is significantly higher than 6-9 of current Si-based adapter. Therefore, GaN-based devices have been assumed as a game-charger device in charger/adapter filed in terms of power density, efficiency as well as size.



12Figure 1.4.2: GaN power device market [51]

According to the anticipation from industry experts, GaN will substitute Si numerous of power electronics system, owing to its low power consumption and high efficiency, which makes GaN become a decent material with regards to manufacturing power semiconductor devices. Additionally, GaN-based devices offer higher thermal conduction, larger critical electric field as well as higher breakdown voltage in comparison with that of Si-based devices. Making GaN devices are functional at higher power density and higher switching frequency, and eventually result in higher efficiency as compared to Si-based devices. Achievement and development were made in GaN devices over past few years, enabling GaNFETs become commercially available and already to be used in some power electronics systems, such as Mobile charger, tele-communication station. As a result, the Gallium Nitride technology is projected to witness soaring demand in automotive, defense&aerospace, healthcare, information & communication technology, and both consumer and industrial electronics [6].

## 1.5: Proposed Dissertation Outline

In this thesis

Chapter 1: Literature review, study background, GaN device current market and situation, and motivation

Chapter 2: Comparison between e-mode GaNFETs and cascode GaN devices, including the key parameters comparison of two different GaN devices as well as the gate driver design consideration. Then both switching transients and characterisation of cascode GaN devices is studied, consisting of switching loss mechanism, analytical loss model and parasitic elements’ effect.

Chapter 3: General gate driver considerations for GaN power devices are introduced in this chapter. Three PCBs with different gate driving loop design are made to evaluate the influence of key parasitic elements for cascode GaN devices. Furthermore, the method to optimise the cascode GaN devices’ switching performance in term of key switching waveforms (Vgs, Vds, Id) is also proposed in this chapter.

Chapter 4: Evaluating the effect of gate drive circuit design in cascode GaN-based converter. A synchronous buck converter scheme is selected to access the influence of gate drive circuit design. A series of SPICE-based simulation are conducted in Cadence Orcad, which is use to investigate the influence of different gate drive circuit design based on the result of Chapter 3. In addition, a hardware prototype with optimised gate driving loop is made for demonstration purpose.

Chapter 5: A desaturation plus negative power supply protection scheme for normally-on WBG devices is proposed in this chapter. The entire protection scheme falls into two parts, namely, desaturation scheme, which is used to protect the circuit/system from overcurrent/short circuit event. Another one is so-called negative power supply protection scheme ascribed to the use of negative supply for normally-on device is indispensable. Therefore, it is necessary to have a proper protection for such negative power supply in case of contingencies.

Chapter 6: Conclusion and future possible research opportunities

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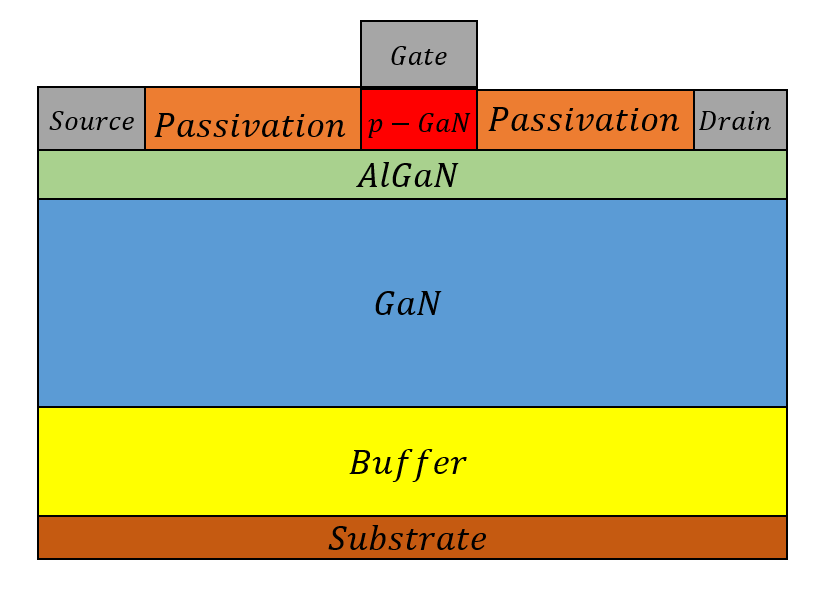
# Chapter 2: Cascode GaNFET

In comparison with e-mode GaN device, the main advantage that cascode GaN device bring can be described as following. As explained previously, the gate of cascode GaN device is also the gate of Si MOSFET, which means the requirement of cascode GaN gate driver is similar to that of Si MOSFET. This makes cascode GaN device become more welcoming for both industries and customers. On another hand, the LV Si MOSFET offers protection for GaN HEMT due to of Si MOSFET is anti-parallel to of GaN HEMT, which prevents GaN HEMT gate failure. Furthermore, thanks to the implementation of Si MOSFET, cascode GaN device no longer require negative gate bias during turn-off. In the meantime, the cascode GaN device can withstand much high gate voltage in both positive and negative magnitude. Therefore, the cascode GaN devices can significantly ease of complexity and requirement of gate driver, making GaN devices obtain normally-off operation with attractive features such as robust gate structure, high threshold voltage as well as stable dielectric etc.

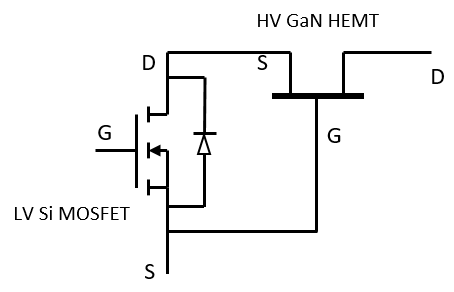
## 2.1: Introduction of e-mode GaNFET and Cascode GaNFET

As aforementioned, conventional GaN HEMT is a naturally depletion-mode device, making it unsuitable for most of power electronic applications. Since the normally-on characteristic of GaN HEMT poses a lot of safety concern when employ such d-mode GaN HEMT into most of power conversion applications. Meanwhile, the normally-on devices require more complicated gate driver design and dedicated protection scheme. Since the d-mode devices need negative voltage to turn off rather than simply shut down the power supply. Consequently, the depletion-mode GaN device is undesirable for most of circuit design and is not attractive like other enhancement-mode competitors, such as Si and SiC-based devices.

In order to overcome the shortcomings of GaN HEMT, it is necessary to make enhancement-mode GaN devices. By far, there are two trending techniques are used to achieve this purpose. One is adding a p-GaN layer underneath of the gate terminal to achieve normally-off operation [1]–[3], the schematic cross-sectional view of p-GaN gate HEMT is illustrated in Fig. 2.1.1 Another one is so-called cascode structure, which integrates two discrete devices into one single package [4][5]. The cascode configuration consisting of LV Si MOSFET and HV GaN HEMT as shown in Fig. 2.1.2.



13Figure 2.1.1: The cross-sectional view of normally-off GaN device using p-GaN cap layer

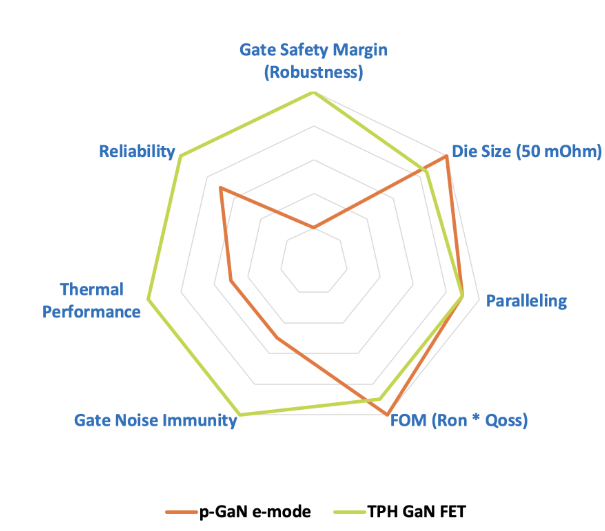


14Figure 2.1.2: The cascode GaN device configuration

Currently, there are lots of different p-GaN gate devices are available in the market, such as GS series from GaN System Inc. and EPC series from Efficient Power Conversion Corporation Inc. On the other hand, Transphorm Inc is a representative company of cascode GaN device. The key parameters between Si MOSFET, cascode GaN device and p-GaN gate e-mode GaN as shown in Table 2.1. Meanwhile, Fig. 2.1.3 depicts the detailed comparison of Transphorm’s cascode GaNFET and GaN System’s e-mode GaNFET.

4**Table 2.1**: **Key parameter comparison between current advanced Si MOSFET, cascode GaN device and e-mode GaN device @ 650V level** [6]–[8]

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter | Si MOSFET (NVB110N65S3F) | Cascode GaN (TP65H050WS) | e-mode GaN  (GS66508B) |
| Maximum transient protection/V | 700 | 800 | 750 |
| Gate driving voltage safety margin /V | 20 | 10 | 1 |
| Gate threshold voltage/V | 4 | 4 | 1.7 |
| Reverse conduction operation ( | 1.3 | 1.3-1.8 | 6-9 |
| Negative gate voltage required | No | No | Yes |
| Paralleling | / | Up to two devices | More than two devices possible |
| Gate charge (Qg)/nC | 58 | 16 | 6.1 |
| Reverse recovery charge (Qrr)/nC | 343 | 125 | 0 |
| On-resistance ()/mꭥ | 93 | 50 | 50 |



15Figure 2.1.3: Comparison between today’s e-mode GaN device and Transphorm cascode device @ 650V/50mΩ [9]

According to Table 2.1, both e-mode GaN and cascode GaN devices outperform the state-of-art Si MOSFET in term of gate charge (), reverse recovery charge () as well as on-resistance (). The gate charge () determines how fast and how frequently the transistor can be turned on and off. Lower gate charge allows faster switching speed, which is a desired characteristic in power semiconductor. The reverse recovery charge () affects the performance of overall system from switching loss prospective. Cascode GaN device exhibits much lower reverse recovery charge and e-mode GaN device can completely eliminate gate charge and thereby improve the switching performance of the system. The on resistance () of GaN device is significantly lower than Si MOSFET for given voltage and current capability, this feature result in a reduction in conduction loss, which is very attractive in electronic applications. Fig. 2.1.3 draws the detailed comparison between today’s e-mode GaN device and cascode GaN device. The casocde GaN shows superior properties in terms of robustness, thermal performance, reliability and gate noise immunity, but also exhibits similar die size and on-resistance. Meanwhile, it is very important to point out the cascode GaN exhibits a different mechanism during reverse conduction from purely e-mode GaN device. Regarding to the reverse conduction of cascode GaN device, the body diode of the LV Si MOSFET conducts the reverse current and the GaN HEMT gate-to-source voltage is clamped by the diode forward voltage. The GaN HEMT is turned-on and the on-resistance of GaN HEMT is added toward the total voltage drop of reverse conduction. This can be expressed as following equation 2.1, leading to cascode GaN device has lower voltage drop in comparison with e-mode GaN device for given voltage/current capability [10].

(2.1)

As discussed in Chapter 1, GaN-based devices have superior potential in comparison to current Si-based device for a given breakdown in low-medium range power applications. However, the relatively low gate threshold voltage () and the narrow gate voltage safety operation margin of current e-mode GaN device limit the use of GaN devices. Fast switching property of GaN-based devices aggravates such issues and poses significant difficulties when design the gate driver of GaN-based devices. The cascode GaN devices are developed to counter such issues that e-mode GaN devices bring. In accordance with Table 2.1, the current commercial cascode GaN devices (650V/50mΩ) enable 1.5-2.3 times higher gate threshold voltage and 10 times wider gate driving voltage safety margin at cost of increased reverse recovery charge () and gate charge () in comparison with e-mode GaN devices. Moreover, such two-chip normally-off device in cascode configuration offer simple design-ability and does not require dedicated gate driver, and hereby ease of major difficulties when using e-mode GaN device [11].

Common mode current is an inevitable issue for all kinds of fast switching power transistor. Not only GaN-based devices, but also Si and SiC-based MOSFETs. The following approaches are normally used to avoid such common mode current issue.

1. Implementation of high CMTI gate driver
2. Separation of the device gate source and power source with kelvin connections, and hence the voltage ringing/oscillation caused by parasitic inductance at source located on the gate can be minimised
3. Optimise the gate driving loop layout and apply negative gate biase for turn-off, this can effectively prevent false turn on due to high dv/dt
4. Different from Si and SiC-based MOSFETS, GaN-based devices have significantly lower reverse recovery charge, the EMI and noise management become much easier.

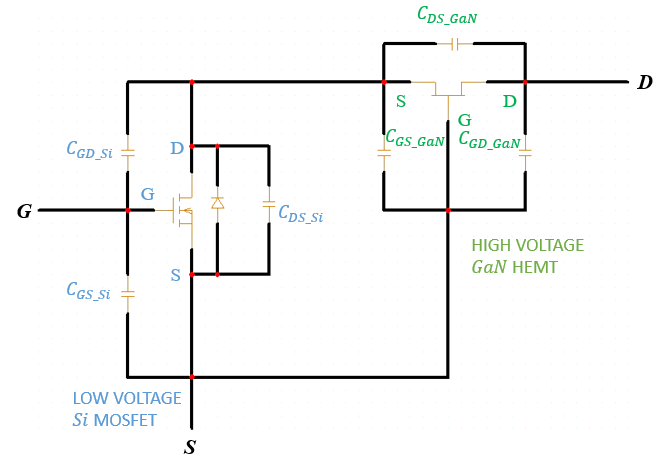
## 2.2: Cascode GaN Device Characterisation

By far, the cascode GaN devices can be found at 600V, 650V and 900V level in the market. The reason for cascode GaN device has not been developed in lower voltage rating is also one of major side effect of such device. As aforementioned, GaN device is able to achieve lower on-resistance, smaller die small for given voltage/current rating in comparison to Si device. For any cascode GaN device, Si MOSFET contributes additional on-resistance in comparison with other single-die e-mode GaN device. Consequently, the higher the cascode GaN device rating, the lower the Si MOSFET on-resistance contribution towards cascode device. The Silicon material and its related devices have been widely and deeply studied in past few decades. Hence, Si is quite mature, and the reduction of its on-resistance become very difficult. Compared to Si, GaN is relatively new and more likely to achieve lower on-resistance in the future because of its superior physical properties. Therefore, it can be seen that the LV Si MOSFET will take a larger percentage of overall on-resistance for cascode GaN device. As a result, the cascode structure is unsuitable for low voltage rating device, and 600V or above is the target range of cascode GaN device.

### 2.2.1: Insight of Cascode GaN Device

As aforementioned, two-chip GaN devices with cascode configuration realise much higher gate threshold voltage Vth (≥2.5V) and wider gate voltage operation margin (≥20V) in comparison with other current commercial e-mode GaN device in the market. Such casocode GaN device enable a simplified gate driver while better gate robustness compared to that of e-mode GaN devices.

Avalanche capability and its rating are both key parameters when accessing a power semiconductor. GaN-based devices generally do not exhibit avalanche capability because of natural structure. Instead, GaN-based devices offer higher voltage transient specification than traditional Si avalanche rating, to avoid the devices enter avalanche region [12]. In comparison with e-mode GaN devices, the cascode normally-off GaN solution offer the higher transient drain-source voltage rating in 650V rated level, which provide best reliability. Moreover, the use of LV SI MOSFET combined with GaN HEMT gives rise to additional advantage of cascode GaN devices. For instance, the cascode GaN device, which exhibits higher gate threshold voltage, does not require negative gate bias for turning off. This can mitigate the complexity when designing PCB for GaN devices in terms of board layout and the implementation of kelvin source connection. Moreover, it is reported that the e-mode GaN devices require 5V or more gate voltage in order to fully enhance the conducting channel and attain fastest switching speed. According to the regulation of current e-mode GaN device [8], [12]–[14], the maximum allowed gate voltage is around 6-7V. Extremely fast driving speed combined with relatively narrow gate voltage margin poses significant challenge for the e-mode GaN gate driver design. Built-in high dv/dt and di/dt of GaN devices result in large gate voltage swing/oscillation. As a result, all kinds of e-mode GaN device require a negative gate voltage to ensure the safety operation. Such gate driving power loss and design complexity can be avoided by using cascode GaN device. Last but not the least, cascode GaN devices allow TO-220 and TO-247 packages. This makes a few kilowatt design with single pair of device become feasible, without paralleling devices [11]. Consequently, the use of cascode GaN devices not only increase reliability but also reduce overall cost with similar high efficiency (>99%) in both totem-pole and half-bridge design.



16Figure 2.2.1: Detailed configuration for two-chip cascode GaN device with all junction capacitors

The detailed cascode configuration is illustrated in Fig. 2.2.1. It is obvious that the LV Si MOSFET controls the overall device’s ON and OFF. As reported in [15], the interaction between two internal devices might cause instability due to large parasitic inductance within the package. In order to reduce the package parasitic inductance, an approach called chip-on-chip technique has been introduced to cope with package inductance issue [16]. Since the cascode device is formed by two discrete devices, and therefore the junction capacitors of both LV Si MOSFET and HV GaN HEMT are critical for the purpose of high efficiency. The influence of those capacitors become more significant when operating at soft-switching condition. As well known, with respect to turn-off transition of cascode GaN device, the voltage distribution is mainly determined by the charge of junction capacitors. As documented in [18], if Si MOSFET enters avalanche region, it might lead to extra loss as well as concern of reliability. As said, such issues would become more severe if the devices are operating under soft-switching condition. For instance, the zero-voltage switching (ZVS) turn-on transient voltage distribution is opposite of turn-off transient. Which indicates if Si MOSFET reach avalanche condition during turning-off, then GaN HEMT unable to attain ZVS.

For Si MOSFET avalanche issue can be explained as follows. when Si reaches avalanche region, it might result in extra loss as well as reliability concern. Si MOSFET goes into avalanche when the charge stored in greater than the charge stored in and , where equals to the sum of and . It is also necessary to emphasise that the Si MOSFET might reaches avalanche if the breakdown voltage of LV Si MOSFET is lower than the threshold voltage of HV GaN HEMT. A cascode GaN-based boost converter is selected to analyse the voltage distribution as shown in Fig. 2.2.2 (a), and two possible turn-off transitions of cascode GaN devices are depicted in Fig. 2.2.2 (b) and (c) respectively. stands for the gate voltage that applied on gate-source terminal of the cascode GaN device in Fig. 2.2.2 (a), and and are the drain-source voltage of the LV Si MOSFET and HV GaN HEMT respectively. According to Fig. 2.2.2 (b) and (c), the main difference of these two cases is whether the LV Si MOSFET is driven to avalanche region. Accordingly, a well-matched cascode GaN device is defined by whether the charge stored in is lower than the charge stored in and .

The detailed turn-off transition of a well-matched cascode GaN device can be described as following:

1. At T0, the turn-off signal is applied to the gate-source terminal of the cascode GaN device.
2. At T1, the LV Si MOSFET channel is turned off
3. During T1-T2, and are charged in parallel via the HV GaN HEMT’s channel until the rises to its threshold voltage ()
4. During T2-T3, the HV GaN HEMT is turned off, and the is charged in series with and .
5. At T3, rises to V1 that is lower than its avalanche value (), and rises to .

However, with respect to a mis-matched cascode GaN device, the is driven to avalanche region at T3 in Fig.2.2.2 (b), however, only rises to that is slightly lower than steady state value. During T3-T4, the LV Si MOSFET remains in avalanche region, and is charged independently via the avalanche route as depicted in Fig. 2.2.2 (b). The rises from to its steady state value (). It is worth pointing out that the charging path via does not affect the voltage distribution between the LV Si MOSFET and HV GaN HEMT. By adding an additional capacitor, which is paralleling between the drain and source terminal of the Si MOSFET, can effectively resolve such capacitance mismatch issue [17].

|  |
| --- |
| Diagram  Description automatically generated |
| (a) |
| Chart, line chart  Description automatically generated |
| (b) |
| Chart, line chart  Description automatically generated |
| (c) |

17Figure 2.2.2: (a) boost converter example used in this work; (b) mis-matched cascode GaN device during turn-off; (c) well-matched cascode GaN device during turn-off

Regarding to ZVS of cascode GaN device, there are two possible ZVS turn-on transitions as shown in Fig. 2.2.3. The negative inductor current () indicated in Fig. 2.2.2 (a) is used to discharge the junction capacitors of cascode GaN device to achieve ZVS operation. Compared to a well-matched cascode GaN device, the mis-matched cascode GaN device has one additional stage as drawn in Fig. 2.2.3.

The detailed ZVS turn-on operation of a well-matched cascode GaN device can be described as following:

1. At T0, the negative inductor current () starts discharging the junction capacitors, the is discharged in series with and .
2. During To-T1, drops from initial value ( as drawn in Fig. 2.2.2 (c)) to . decreases from the value of to zero because of charge balance. The total amount of charge stored in and and is fully recycled to the input source at this stage.
3. At T1, is attained and the HV GaN HEMT is turned on. The remaining charge stored in and is ceaselessly discharged by inductor current ().

With respect to a mis-matched cascode GaN device, can only drops to as shown in Fig. 2.2.3 (b) when drops to because the charge stored in the HV GaN HEMT is much greater than the charge stored in the LV Si MOSFET. After T1, the HV GaN HEMT’s channel begins to conduct and the remaining charge of is dissipated via the channel, which indicates extra turn-on loss that is proportional to the switching frequency. During T1-T2, the voltages across and decrease in a constant speed and the majority of the inductor current () is flowing through at this stage. It is necessary to highlight that a very little decrease in gives rise to a significant increase of the HV GaN HEMT displacement current and thereby results in a relatively fast voltage drop. Therefore, remains almost constant during T1-T2 in order to maintain a consistent voltage slope. According to Fig. 2.2.3 (b), the ZVS turn-on can be achieved with a mis-matched cascode GaN device, while part of energy stored in is dissipated internally owing to a mis-matched charge. As a result, the mis-matched junction capacitances of LV Si MOSFET and HV GaN HEMT in cascode GaN device result in the occurrence of LV Si MOSFET avalanche and a failure of ZVS turn-on even a ZVS technique is applied.

|  |
| --- |
| Chart, line chart  Description automatically generated |
| (a) |
| Chart, line chart  Description automatically generated |
| (b) |

19Figure 2.2.3: Two possible zero-voltage switching transitions of (a) well-matched cascode GaN device; (b) mis-matched cascode GaN device

The cascode GaN device’s switching transient is different from e-mode GaN device, due to two discrete devices are integrated within single cascode device package. Regarding to cascode GaN device turn-on transient, the of Si MOSFET is firstly charged when gate bias applied, until the threshold voltage of cascode device is reached. Once the threshold voltage reached, the MOSFET channel become conductive and the displacement current starts flowing through Si MOSFET and . The GaN HEMT gate-to-source capacitor is in parallel with Si MOSFET drain-to-source capacitor , and hence the is charged with a phase delay because of internal parasitic inductance between Si MOSFET and GaN HEMT. When the voltage across exceeds the threshold voltage of GaN HEMT, the GaN HEMT channel is conductive and thereby the drain-source voltage falling. After drops to zero, continues rising until it reaches zero. At the same time, the exponentially increases until it equals to gate voltage, . With respect to turn-off transient, the gate of Si MOSFET is discharged via the gate drive circuit when it output is a LOW voltage, generally 0V. The is therefore discharged and the decreases until Si MOSFET reaches saturation region. Then the load current starts charging and , hence the drain-source voltage, , rising. It is necessary to address that the of the Si MOSFET starts to charge when the of the Si MOSFET is discharged to its Miller plateau. The is parallel to as described, therefore, it is discharged until the value where the GaN HEMT enters the saturation region. Once GaN HEMT reached saturation region, the drain-source voltage of GaN HEMT rises to the steady-state voltage level. Meanwhile, the load current is now transferred from cascode GaN device to another power device. The output capacitance of the GaN HEMT must charge before Si MOSFET output capacitance otherwise the MOSFET goes into avalanche. A buck converter is used to analyse the turn-on and turn-off event and switching loss of cascode GaN device as shown in Fig. 2.2.4. It is necessary to point out that the inductor current is assumed as current source during switching transient in following analysis.

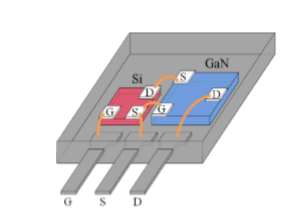
|  |  |
| --- | --- |
| **Cascode GaN Device Turning-on Transition** | |
| Stage I: Si MOSFET delay period | Diagram, schematic  Description automatically generated |
| Stage II: Si MOSFET falling, GaN HEMT rising | Diagram, schematic  Description automatically generated |
| Stage III: GaN HEMT channel current rising | Diagram, schematic  Description automatically generated |
| Stage IV: Bottom switch reverse recovery | Reverse recovery period starts when the current flow through rises to load current. This is due to the bottom device unable to block the reverse voltage until a certain amount of charge being removed from its junction. During this period, keeps decreasing, and the voltage difference between and is accordingly becomes larger. Thus, the current flowing through Ld rises rapidly. The internal parasitic inductance, , combined with this large di/dt slows down the increasing of , and eventually saturates the channel of GaN HEMT. Once bottom device completes its reverse recovery, stage IV finished. While, if the bottom device does not have any reverse recovery charge, , the stage IV should be omitted. |
| Stage V: GaN HEMT falling | Diagram, schematic  Description automatically generated |
| Stage VI: Remaining gate charging, until reaches zero | Diagram, schematic  Description automatically generated |
| (a) | |

|  |  |
| --- | --- |
| **Cascode GaN Device Turning-off Transition** | |
| Stage I: Si MOSFET delay period | Diagram, schematic  Description automatically generated |
| Stage II: Si MOSFET rising, GaN HEMT falling | Diagram, schematic  Description automatically generated |
| Stage III: GaN HEMT channel current falling | Diagram, schematic  Description automatically generated |
| Stage IV: GaN HEMT rising | Diagram, schematic  Description automatically generated |
| (b) | |

20Figure 2.2.4: The equivalent circuit of cascode GaN device (a) turn-on transient; (b) turn-off transient

### 2.2.2: Analysis of Switching Loss Mechanism for Cascode GaN Device

The switching loss analysis for cascode GaN devices is much different from e-mode GaN devices, ascribed to there are two discrete power devices are integrated within cascode device package. Both turn-on and turn-off transients of cascode GaN device have been detailed described in Chapter 2.2.1. The analytical loss model for cascode GaN device can be built based on its special switching transients. The package 3-D view of current cascode GaN device as depicted in Fig. 2.2.5 [18].



21Figure 2.2.5: TO-220/TO-247 Package for Commercial cascode GaN device

A proper analytical model should consist of all relevant parameters within practical cascode GaN device, such as parasitic capacitance and inductance, as well as non-linear transconductance. The PCB layout can also easily create nH level parasitic inductance outside of the device package, which is in a similar level in comparison to that of internal cascode device. Thus, both device internal parasitic inductance and the inductance caused by PCB trace have remarkable influence on cascode devices’ switching transition. Besides these parasitic inductances, both Si MOSFET and GaN HEMT have three intrinsic capacitors, which are gate-to-source capacitor (), gate-to-drain capacitor () and drain-to-source capacitor (). Among these three capacitors, remains almost constant regardless of the voltage applied. While both and are in a relationship with reverse biased p-n junction, which means the capacitance of these two capacitors are dependent upon the applied voltage. The relationship between such non-linear capacitance and the applied voltage can be described as equation 2.2, where is the capacitance at 0V, and is normally extracted from the datasheet of the device by using curve fitting.

(2.2)

Except parasitic inductor and intrinsic capacitor, another important parameter as aforementioned, namely, transconductance (). This parameter is determined by the change of output current () of the device over the input voltage () across the device. According to its physical definition, transconductance is related to gate-to-source voltage with a nearly linear function as drawn in equation 2.3, where k is generally derived from the datasheet of the device.

(2.3)

The approximate loss-analysis model of cascode GaN device can be built by using the equivalent circuit as illustrated in Fig. 2.2.4. As described in Chapter 2.2.1, the turn-on event of cascode GaN device has been divided into six stages, while the turn-off event has four stages. Therefore, the loss model of cascode GaN device can be built accordingly.

|  |  |
| --- | --- |
| **Cascode GaN device turning-on transition** | |
| Stage/Key equation | Equivalent circuit and current direction |
| Stage I:    During turn-on stage I, only gate driving loss should be considered, due to both Si MOSFET and GaN HEMT still in off-state. Once reaches , this stage ends. |  |
| Stage II:  -  During Stage II, the cascode Gan Device drain-to-source voltage is clamped at Vdc, the is still flowing through FWD,. The energy stored in , and being consumed and Si MOSFET conducting. This stage ends when equals to . | Diagram, schematic  Description automatically generated |
| Stage III:  -  The stage III finishes when the reaches inductor current . |  |
| This stage has same equivalent circuit and corresponding equation as stage III.  Once drain current through top switching reaches inductor current , the reverse recovery starts. If bottom switch has no reverse recovery charge, such as WBG-based device (GaN or SiC devices), and this stage can be omitted and directly go to stage V. |  |
| Stage V:  Stage V ends when drops to zero. | Diagram, schematic  Description automatically generated |
| Stage VI ends when reaches zero. In the meantime, the keep increasing till it attains . When the cascode GaN device fully turn on, the conduction loss can be calculated by using the steady-state current and related on-resistance of the cascode device. | Diagram, schematic  Description automatically generated |
| (a) | |

|  |  |
| --- | --- |
| **Cascode GaN Device Turning-off Transition** | |
| Stage/Key equation | Equivalent circuit and current direction |
| Stage I:  Stage I ends once the Si MOSFET reaches saturation region, the switching loss during this stage is relatively small and hence can be omitted. | Diagram, schematic  Description automatically generated |
| Stage II:  This stage finishes when reaches the value where the GaN HEMT attains saturation region. During this stage, decreases, while only rises a bit because of the increase of on-resistance. The switching loss occurs during this stage can be neglected. | Diagram, schematic  Description automatically generated |
| Stage III:  This stage finishes once the channel of GaN HEMT being shut down. | Diagram, schematic  Description automatically generated |
| Stage IV:  Stage IV end when bottom device) affording zero voltage (, and current now is flowing through the freewheeling diode. |  |
| (b) | |

22Figure 2.2.6: The detailed analysis with respect to (a) turn-on event; (b) turn-off event

Besides abovementioned switching loss, which consists of turn-on and turn-off losses. Another two important losses should also have taken into account, so-called conduction loss and gate driving loss.

The conduction loss is the loss when the device is conducting (ON-state). Unlike switching loss, the conduction loss is not dependent upon operation frequency. The equation used to calculate the conduction loss as shown following equation 2.4, where is the device on-state resistance, and is the current when device is conducting.

(2.4)

Regarding to gate driving loss, it is caused by the energy required to charge/discharge () the gate of the device. Therefore, it takes place in both turn-on and turn-off process. Similar to switching loss, the gate driving loss is also frequency dependent. The equation 2.5 shows the way to calculate gate driving loss. Where Qg is the total gate charge, Vg is the applied gate voltage, and is the switching frequency.

(2.5)

In general, the power losses for any power semiconductor devices can be classified as switching loss, conduction loss and gate driving loss as aforementioned.

A Double Pulse Test (DPT) is built to verify the analytical loss model. In order to ensure the accuracy of DPT. It is important to integrate all parasitic elements within the DPT circuit. As described above, the parasitic inductances within device package affect the switching loss of the device. Besides the package parasitic inductance, the parasitic inductance in PCB layout also plays an important factor with respect to switching performance. Therefore, the minimization of inductance for PCB design is highly desired. The gate driving loop and power loop as depicted in Fig. 2.2.7. The important inductance within PCB layout is extracted via Ansoft Q3D FEA simulation and both package inductance and gate driving loop and power loop inductance within PCB are summarized in Table. 2.2. As well-known, there are many parameters such as position, dimension as well as current direction of a conductor play a significant role in inductance within PCB layout. Therefore, the PCB layout is directly exported to Ansoft Q3D FET to ensure both dimensions and positions of all conductors in gate driving loop and power loop are exact as the practical board. Except from this, a source and a sink are required to be defined by users to create a loop. After defining the source and the sink, the operation frequency is set to 150MHz to simulate voltage ringing caused by parasitic inductance. In this work, the gate driving loop and power loop are drawn in Ansoft Q3D FET as indicated in Fig. 2.2.7. Apart from Ansoft Q3D FET, an experimental verification is conducted in this work in order to ensure the accuracy of the simulation result of important inductances. The parasitic inductances within gate driving loop and power loop are measured by using Agilent E4980A precision LCR meter with 16048A/D/E (from Keysight Technologies, Inc) cables in four-terminal pair. Parasitic inductance in cables and LCR meter were measured before the extraction of targeted inductance by short-connecting two measurement probes. With regards to the LCR meter set-up, taking the practical measurement of gate driving loop as an example, the tips of two measurement probes are attached to the ‘Vout’ pin and the ‘GND’ pin of the gate driver IC (Si8271) respectively. The parasitic inductances within coaxial current shunt are measured via Agilent E4980A precision LCR meter. Fig. 2.2.8 shows the view of used Agilent E4980A LCR meter. A coaxial current shunt (Part No: SSDN-10) from T&M Research Products Inc. is used to measure the drain current, key parameters of this current shunt as shown in Table 2.3. Fig. 2.2.9 illustrates the front view of the current shunt and related model.

5**Table 2.2: Parasitic inductance of package and PCB**

|  |  |
| --- | --- |
| **Package** | |
| / nH | 2.2 |
| / nH | 1.88 |
| / nH | 0.86 |
| / nH | 0.02 |
| / nH | 0.33 |
| **Double-Pulse-Test** | |
| / nH | 5.43 |
| / nH | 5.2 |

|  |
| --- |
|  |
| (a) |
|  |
| (b) |

23Figure 2.2.7: Parasitic inductance of (a) gate-driving loop; (b) power loop

Graphical user interface

Description automatically generated

24 Figure 2.2.8: View of Agilent E4980A LCR meter

6**Table 2.3: Key parameter of the coaxial current shunt used in this work**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Part No** | **Measured Resistance** | **Bandwidth** |  |  |
| SSDN-10 | 0.0986 m**ꭥ** | 2000 MHz | 1.92w | 1.92J |

|  |  |
| --- | --- |
|  |  |
| (a) | (b) |

25Figure 2.2.9: SSDN-10 coaxial current shunt (a) front view; (b) model

The SSDN-10 current shunt is form by a resistor with very small inductance, which are distributed at the top and bottom core of the current shunt respectively as depicted in Fig. 2.2.9 (b). The bandwidth of SSDN-10 is determined by the parasitic inductance shared by top and bottom loop, which is as small as few pH. The selection of the coaxial current shunt is also important for characterising of any device via DPT. Because the larger the resistance, the larger the size, and thus more inductances will be counted into power loop of the DPT circuit. On the other hand, the small the resistance of current shunt, the smaller bandwidth and smaller magnitude of target signal, which results in less accuracy of the measurement.

After the correction of all parts within DPT circuit, the experimental measurement is conducted in order to verify the model. Fig. 2.2.10 shows the DPT test circuit used in this work, which in addition to the DUT, has a free-wheeling SiC diode (Part No: FFSH3065B-F085). The original model of TPH3205WSB (DUT) is developed by Transphorm Inc [20]. A ferrite leaded 100uH inductor with partial single layer winding is used in this work. In order to improve the accuracy of the model, author further amend the model in accordance with practical measurement.

|  |
| --- |
| 26Figure 2.2.10: Double pulse test circuit |

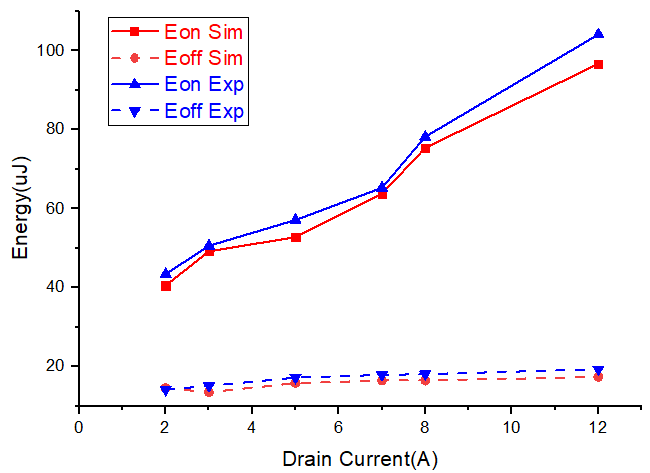
|  |  |
| --- | --- |
| (a) | (b) |
| (c) | (d) |
| (e) | (f) |

27Figure 2.2.11: Zoom-in switching transition of analytical loss model and experimental measurement for cascode GaN device (TPH3205WSB) (a) 400V/2A turn-on; (b) 400V/2A turn-off; (c) 400V/3A turn-on; (d) 400V/3A turn-off; (e) 400V/5A turn-on; (f) 400V/5A turn-off

Fig. 2.2.11 depicts the turn-on and turn-off waveform comparison between the experimental measurement result and the analytical model by using DPT circuit. Therefore, the switching loss can be calculated in accordance with switching waveforms. The switching loss is classified into two parts, namely, turn-on and turn-off loss. The turn-on energy () is the energies dissipated during switch-on transition. Similarly, the turn-off energy () is defined by the energies dissipated during switch-off transition. To be more specific, the turn-on loss is the integral of the instantaneous power starts from T0 to T1, T0 is the time when Id starts rising, and T1 is the time when Id enters steady-state level (within 10% error range) as shown in Fig. 2.2.12. Similarly, the turn-off loss can be calculated in same approach. It is necessary to point out the turn-on and turn-on energy calculated above including two parts, one is the transition loss, which forms majority of switching loss; another one is so-called oscillation loss, this is mainly caused by the parasitic oscillation and cannot be omitted during switching loss calculation. According to the comparison as shown in Fig. 2.2.11, the modified simulation model of cascode GaN device (TPH3205WSB) shows a 3.9% and 5.8% difference from practical turn-on and turn-off switching loss respectively, which performs a better accuracy in comparison with that of manufacturer [19].

|  |
| --- |
| 28Figure 2.2.12: The approach used to calculate Eon |

In order to find out the accuracy of the analytical model built in Cadence Orcad. The simulation result of switching loss based on analytical model is compared with that of experimental result as shown in Fig. 2.2.13.



29Figure 2.2.13: TPH3205WSB switching loss comparison between simulation model and experimental measurement

### 2.2.3: Cascode GaN Package Effect

The GaN devices is able to achieve much faster switching speed (3-5 times) over current Si MOSFET, because of the merit of GaN material. On the other hand, power devices cannot achieve their maximum switching speed due to the trade-off between switching speed and switching loss/performance always exist for any power devices. It is because oscillation/ringing during switching transitions is mainly caused by the combination of dc/dt, di/dt and parasitic elements. As a result, the parasitic elements caused by bulky device package become a critical limit factor of the switching performance of the device.

The parasitic elements play an even more significant role in the cascode GaN device in comparison with other fully integrated single die power semiconductor device. Among all parasitic elements within cascode GaN device, the Common Source Inductance (CSI) plays a significantly important role with respect to overall device switching performance. This is because the common source inductance is shared by both gate driving loop and power loop.

With regard to the conventional single die Si MOSFET, the effect of package has been widely studied [19]–[24]. Different from conventional single die power device, cascode GaN device has several source-sided parasitic inductances due to the structure uniqueness. Fig. 2.2.14 shows the source-sided parasitic inductance within the cascode GaN structure.

|  |
| --- |
| (a) |
| (b) |
| (c) |

30Figure 2.2.14: The common source inductance within cascode GaN device package from (a) Si MOSFET’s perspective; (b) GaN HEMT’s perspective; (c) overview of entire cascode structure

As shown in Fig. 2.2.14 (a), from Si MOSFET’s prospective, the blue loop represents the driving loop and red line stands for the power loop. Therefore, the Lint3 and Ls are the CSI of Si MOSFET, which are shared by both driving and power loop. In the same manner, the green line in Fig. 2.2.14 (b) is the driving loop with reference to GaN HEMT, and red line still represents the power loop. Consequently, the Lint1 and Lint3 become the CSI of the GaN HEMT. In accordance with the cascode GaN device’s structure as depicted in Fig. 2.2.13 (c), it is obvious that the Lint3 is the most important parasitic inductance within the cascode GaN device. Since the lint3 is common CSI for both Si MOSFET and GaN HEMT. Regarding to another two internal parasitic inductances, Lint1 should be considered as second important inductance due to it is part of CSI of HV GaN HEMT, which contributes the majority of overall switching loss. Hence, Ls is the third important parasitic inductance.

The internal circuit of cascode GaN device (TPH3205WSB), including resistance, inductance and capacitance, as shown in Fig. 2.2.15. The values for parasitic inductances are based on the SPICE file provided by manufacturer. In order to investigate the impact of each of parasitic inductance within the cascode package, namely, ,, , Lint1, Lint2, Lint3. A buck converter operating at 400V/15A with 50% duty cycle continuous current mode (CCM) condition is built by using TPH3205WSB in Cadence Orcad in order to verify the influence of above-mentioned six major internal parasitic inductance. As well-known, the switching loss dominates overall power loss during hard switching. Among the switching loss, the turn-on loss is accounted for a large proportion. Fig. 2.2.16 illustrates the influence of each parasitic inductance in terms of switching loss. The TO-247 package is set as the baseline (blue line), and other bars located on the right-hand side are used for comparison purpose, which accordingly eliminates one of afore-mentioned parasitic inductance to investigate the influence of that specific inductance. From the Fig.2.2.16, the influence of each parasitic inductance can be easily observed.

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| 31Figure 2.2.15: Internal circuit within TPH3205WSB package |

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| --- |
| 32Figure 2.2.16: Simulation of impact of internal parasitic inductance within cascode package @400V/15A |

Except the cascode GaN device internal parasitic, there are two more critical parasitic inductances need to be taken in account during PCB design, so-called external gate inductance in gate driving loop and external source inductance in power communication loop. Fig. 2.2.17 and Fig. 2.2.18 shows both external gate and source inductance impact to the switching waveforms of the GaN device.

|  |
| --- |
|  |
| (a) |
|  |
| (b) |
|  |
| (c) |
|  |
| (d) |

33Figure 2.2.17: Simulation of impact of external gate parasitic to cascode GaNFET switching waveforms of (a) during turn-on; (b) during turn-off; (c) during turn-on; (d) during turn-off

|  |
| --- |
|  |
| (a) |
|  |
| (b) |

34Figure 2.2.18: Simulation of impact of external source parasitic to cascode GaNFET switching waveforms of (a) Vds & Id during turn-on; (n) Vds & Id during turn-off

As drawn in above two figures, external gate inductance directly affects the gate-source voltage waveform. The larger the external gate inductance, the larger voltage oscillation in gate-source voltage. Whereas external source inductance only exhibits a very little influence on gate-source voltage waveforms according to simulation result. When external source inductance become large enough, a significant drain-source voltage and drain current overshoots can be observed for turn-off and turn-on event respectively as shown in Fig. 2.2.18. Therefore, a PCB with minimum external inductance is highly desirable to achieve a high-efficiency operation for power conversion systems.

## 2.3: Challenge in Cascode GaNFET

There is no doubt that GaN-based devices enables better characteriscs in terms of electric field strength, operating temperature, current density, switching speed and on-resistance over that of state-of-the-art Si MOSFET. It is vitally important to think of potential challenges and technical considerations raised by GaN [26]. Due to without deeply comprehension, the GaN-based applications might suffer a worse circuit performance. The major challenges consist of dynamic switching behaviour, effect of package as well as dedicated high-frequency gate driver etc.

### 2.3.1: Switching Behaviour of Cascode GaNFET

The superiority of material properties of GaN making GaN devices are extremely fast and therefore significant oscillation caused by parasitic elements become a significant limit factor of switching performance. Such high-frequency oscillation can further introduce an increased power loss and severe EMI noise. Fig. 2.3.1 illustrates switching waveforms of a cascode GaN device during hard-switching turn-on transition. Therefore, soft-switching technique is highly desired when GaN devices are used in the circuit in terms of loss and noise perspective.

Typically, the cascode GaN devices have special switching characteristics because of two discrete devices are integrated in one single package. As described in Chapter 2.2, the interaction between LV Si MOSFET and HV d-mode GaN HEMT could induces unwanted phenomena. For instance, the LV Si MOSFET enters avalanche region during turn-off; HV d-mode GaN HEMT unable to maintain ZVS turn-on internally when soft-switching technique is applied. As reported in [27], the cascode GaN device might subject to divergent voltage oscillation during high-current turn-off in worst case. Consequently, such undesired phenomena should be taken into consideration if GaN devices are used in the design.

|  |
| --- |
| 35Figure 2.3.1: Cascode GaNFET experimental switching waveforms during hard-switching turn-on |

### 2.3.2: Internal and External Parasitics Effect

Significant research on the influence of device package has been studied for Si MOSFET, SiC MOSFET and LV e-mode GaNFET [22][28][29]. These devices are all based on a single-die structure, and thereby the findings and conclusions are similar to that of Si MOSFET. Hence, the common source inductance (CSI) still plays a dominant role in terms of switching loss perspective due to the CSI is shared by both gate driving loop and power loop. Packaging has accordingly been assumed as a very important factor to GaN-based devices owing to its extremely fast switching speed. Whereas the CSI of the cascode GaNFET is not as straightforward as single-die device ascribed to its unique structure, which consists of two discrete devices within one package and hereby exhibits more package related parasitic elements. Both the identification of the importance of each parasitic inductance in cascode structure and the effect of cascode GaN device package have been studied in Chapter 2.2. As a result, the Lint3, Lint1 and Ls have been considered as most critical parasitic inductance within cascode GaN device as indicated in Fig. 2.2.12. Therefore, further research and development in cascode GaN package, afore-mentioned three inductances should be taken into account with priority. An novel package, so-called stack-die was introduced to minimised key parasitic inductance within cascode GaN package [30]. Moreover, once the advanced package achieved, which means the elimination of these three critical parasitic induces, a prominent reduction in switching loss of the cascode GaN device can be expected.

Apart from the parasitic elements within the cascode package, the external parasitic inductance caused by external circuitry in PCB layout is also accounted for the switching performance of cascode GaN-based design. The significance of PCB layout along with high-frequency operation will be discussed in Chapter 3.

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# Chapter 3: Gate Driver Design for GaN Devices

As well known, gate driver is one of the most important part of any power conversion applications/systems. It is because the Pulse Width Modulation (PWM) signal (0-5V from each I/O pin) from digital logic system unable to fully turn-on the power devices used in power systems since the desired driving voltage exceed the standard CMOS or TTL logic voltage. Therefore, an appropriate interface between digital logic control circuit and the corresponding power device is indispensable. The gate driver works as a power amplifier in the circuit, which accepts a low-power input from a controller circuitry and generates a high-current drive input for the gate/base of a high-power transistor. Gate drivers are perfectly suited for lots of applications, for instance, industrial motor drivers, Uninterruptible Power Source (UPS), Switch Mode Power Supply (SMPS) as well as most of home appliances. As the rapidly increasing demand of power semiconductor devices in various renewable energy systems, such as Electronic Vehicles (EV) and virtual systems, the adoption of gate driver ICs has been significantly accelerated among numerous manufacturers and producers.

Due to high dv/dt and di/dt feature, the gate drivers for GaN devices are facing many different technical challenges compared to Si devices’ counterparts. The detailed gate driver specifications and requirements for GaN devices will be addressed in this chapter. Unlike e-mode GaNFET, a significant high-frequency ringing is observed in waveform during cascode GaN device turn-on transition, which deteriorates the switching performance from loss perspective. Three PCBs with similar power loop while different gate driving loop are made to identify the source to result in such high frequency ringing and accordingly a gate drive circuitry design rule and further possible development for cascode GaNFET are proposed in this chapter.

## 3.1: Gate Drive Circuit Design Considerations for WBG-based Power Device

The modern world is currently experiencing great investigation and development in the electrification. With continuous improvement and advancement of power electronics, the associated demand is keep rising and tend to higher voltage, smaller footprints, lower energy consumption and higher efficiency. This is more urgent with respect to wide band gap (WBG) semiconductor devices ascribed to their superior properties and characterisation in comparison to conventional Si-based devices, in particular higher breakdown voltage, faster switching speed, higher operating temperature and lower system loss [1]. Even WBG-based power devices realise better characterisation, while the adoption of WBG-based power devices has been limited, due to less maturity, lower device reliability, lower availability as well as higher cost. To date, the commercial GaN power devices are still falling behind that of SiC in terms of market share as reported in [2], whereas they have demonstrate excellent potential and performance and relatively fast growth. In order to fully enabling the advantages those GaN bring, a dedicated gate driver or gate drive design is essential.

Wide band gap (WBG) devices enable higher frequencies and higher power density for power electronics over that of Si due to their superior characteristics and properties. Novel WBG-based power devices can play a significant role in energy efficient power systems. Among all potential candidates, GaN and SiC present better trade-off in term of theoretical characteristics, material availability as well as corresponding technological process. However, the inherent material properties of WBG-based devices pose a significant challenge to gate drive circuit design. It is mainly because of high dv/dt and di/dt feature of WBG material.

High dv/dt results in the occurrence of high-frequency circulating current within gate drive circuit [3]–[5]. This might further lead to an interference of gate drive control signal as such high-frequency current can find a path via inter-winding coupling capacitance of the isolation stage of the power supplies for gate driver. Moreover, high dv/dt causes a significant stress on isolation stage, which leads to a reduction in the lifetime of insulation. Therefore, a gate driver with ultra-low coupling capacitance is highly desirable for WBG-based power device. Meanwhile, the high-frequency operation result in an increased cost of control circuit owing to faster control is required [6]. Recently, significant investigation and research have been done by industrial and academics in order to produce low coupling capacitance gate driver. Another vital issue of controlling WBG device is associated with their physical structure. Both GaN and SiC devices require a more complicated control and additional care over that of Si for synchronous rectification due to poor body diode (SiC MOSFET) or no body diode (GaN HEMT).

On the other hand, the gate threshold voltage () and maximum gate voltage () of SiC-based and GaN-based power devices are remarkable different from Si-based power devices. For example, GaN-based devices require the gate driver can operate at high frequencies. Simultaneously, a sufficient driving capability with accurate voltages is indispensable in order to attain quick switching for both turn-on and turn-off transition with appropriate protection. Regarding to the gate driver for SiC-based devices, a relatively high supply voltage with narrow range as well as strong driving strength is required for low losses and hereby efficient-driving system. Such facets make the gate drive circuit for WBG-based power devices become more significant. As a result, WBG-based device unable to deliver the expected excellent performance at high frequencies and power levels in the absence of proper gate drivers. By far, there are a number of power semiconductor companies/manufacturers have developed gate driver ICs for WBG-based devices. On the GaN front, GaN Systems, Texas Instruments (TI), Efficient Power Conversion Corporation (EPC), Infineon Technologies, Transphorm as well as Silicon Labs are standing in a leading position among others. With respect to SiC arena, suppliers like Texas Instruments (TI), Power integrations, ROHM Semiconductors, Infineon Technologies, Microchip Technology and others have introduced numerous high-quality and high-performance gate driver ICs [7].

7**Table 3.1: Key specifications comparison between three commercial GaN devices**

|  |  |  |  |
| --- | --- | --- | --- |
|  | **GS66508B** | **TPH3205WSB** | **PGA26E07BA** |
| Gate Charge (Qg/nC) | 6.1 | 28 | 5 |
| Gain-Source Voltage/Current Driving Safety Margin (V/A) | -10 to +7 | -18 to +18 | -10 to +4 /5m to 1.5 |
| Turn On Delay Time + Rise Time (ns) | 7.8 | 43.6 | 9.3 |
| Turn Off Delay Time + Fall Time (ns) | 13.2 | 48.6 | 7.9 |
| Drain-Source Blocking Voltage (V) | 650 | 650 | 600 |
| Drain-Source Current @ 25°C (A) | 30 | 35 | 26 |
| Gate Threshold Voltage (V) | 1.7 | 2.1 | 1.2 |
| Drain-Source On-state Resistance@ 25°C (Ω) | 50m | 49m | 56m |

As shown in Table 3.1, every GaN power device has unique switching features, which poses different requirement for gate drive circuit. Furthermore, a faster switching and lower gate threshold voltage result in a significant limitation of adoption of GaN-based device. Fig. 3.1.1 illustrates both turn-on and turn-off comparison between e-mode GaNFET (GS66508B) and state-of-the-art Si MOSFET (IPB65R065C7) using DPT circuit. The detailed key parameters appliedd in the test are shown in Table 3.2. As drawn in Fig. 3.1.1, the turn-off di/dt for Si MOSFET (IPB65R065C7) is around 0.52A/ns, whereas the di/dt for GaNFET (GS66508B) is 3A/ns, which is around 6 times higher than that of Si MOSFET. The switching energy comparison of e-mode GaNFET and advanced Si MOSFET under 400/15A operation at room temperature as indicated in Table 3.3, which follows the calculation method shown in Fig. 2.2.12. Hence, even very small common source inductance (CSI) will give rise to high voltage ringing in turn-on and turn-off transition. Therefore, the PCB layout become even more critical when GaN power devices are used in the design.

8**Table 3.2: Key parameters applied in the switching comparison of e****-mode GaNFET and Si MOSFET**

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Value** | |
| **IPB65R065C7** | **GS66508B** |
| Rated drain-source voltage | 650V | |
| External turn-on resistor | 10Ω | |
| External turn-off resistor | 2Ω | |
| Temperature | 25℃ | |
| Gate charge | 6.1nC | 64nC |
| Input capacitance | 242pF | 3020pF |
| On-resistance | 50m Ω | 65m Ω |

|  |  |
| --- | --- |
|  |  |
| (a) | (b) |
|  |  |
| (c) | (d) |

36Figure 3.1.1: di/dt test results for e-mode GaNFET and Si MOSFET (a) GaNFET (GS66508B) 400V/20A turn-off; (b) Si MOSFET (IPB65R065C7) 400V/20A turn-off; (c) zoom-in view of GaNFET turn-off; (d) zoom-in view of Si MOSFET turn-off

9**Table 3.3: Switching energy comparison between e-mode GaNFET and Si MOSFET @ 400V/15A operation**

|  |  |  |
| --- | --- | --- |
| **Value/unit** | **GS66508B** | **IPB65R065C7** |
| Turn-on energy/uJ | 72.5 | 155.2 |
| Turn-off energy/uJ | 6.2 | 15.9 |

## 3.2: Gate Driver for Cascode GaN Device

Regarding to cascode GaN device, the Si MOSFET within the cascode structure provide the gate protection for GaN HEMT to prevent GaN device gate breakdown. The cascode GaN device TPH3205WSB from Transphorm Inc. used as an example to explain the reason. The GaN HEMT within TPH3205WSB, it has a gate threshold voltage at -22V, and it can withstand maximum -35V gate voltage. Therefore, the 30V Si MOSFET in TPH3205WSB ensure GaN HEMT can effectively turn-off. Meanwhile, it offers sufficient voltage margin between the gate threshold voltage and fully off voltage. This can also prevent the false turn on GaN HEMT. Moreover, the 30V breakdown voltage of Si MOSFET can clamped the drain-source voltage of Si MOSFET in extreme case at 30V because of its avalanche capability. As a result, the gate-source voltage of GaN HEMT unable to lower than -35V caused by voltage oscillation, and therefore GaN HEMT will not suffer gate breakdown. More importantly, the gate of Si MOSFET is also the gate of cascode device. Thus, the gate driver requirement of cascode GaN device is very similar to that of traditional Si MOSFET. Thanks to the implementation of Si MOSFET, the cascode GaN device is able to ease sophisticated gate driver design in comparison to that of e-mode GaNFET. Consequently, cascode GaN devices realize a simple gate drive design and gate protection for HV GaN HEMT due to the use of LV Si MOSFET. Although the cascode GaN device realizes a simple gate driver, but there are few special considerations need to be taken into account when using cascode GaN device in the design, which will be addressed in this thesis. Fig. 3.2.1 shows a typical gate drive circuit for GaN power devices. It is worth addressing that a gate driver for GaN devices with separated gate turn-on and turn-off path is preferred due to the requirement of separate control and such gate driver normally does not require an additional diode in turn-off path of gate drive circuitry to limit the current flowing during turn-off. The effect of turn-on resistor (), turn-off resistor (), and speed-up capacitor () to turn-on and turn-off transition of cascode GaN device (TPH3205WSB) have been evaluated in Cadence Orcad as depicted in Fig. 3.2.2. According to Fig. 3.2.2, the turn-on resistor () has direct influence on turn-on dv/dt, whereas turn-off dv/dt is highly depending upon the resistance of turn-off (). Turn-on dv/dt is calculated from 90% to 10% of drain-source voltage waveform while turn-off dv/dt is measured from 10% to 90%. Turn-on and turn-off resistors are aimed to prevent excessive gate-source voltage during turn-on and turn-off respectively. The speed-up capacitor () is used to accelerate the turn-on process and the capacitance value of this capacitor need to be sufficient to make gate voltage negative during turn-off. It is worth pointing out that the charge of has to be greater than the gate charge ) of the power device, and does not affect the turn-off dv/dt if it meets the [8]. FB in the Fig. 3.1.2 stands for ferrite bead, which is used to damp high frequency voltage ringing in the gate-source voltage waveform. The pull-down resistor is implemented to ensure gate-source voltage remain LOW state when drain-source voltage is applied to the drain during the absence of drive power supply.

|  |
| --- |
| 37Figure 3.2.1: A typical gate drive circuit for GaN devices |
|  |

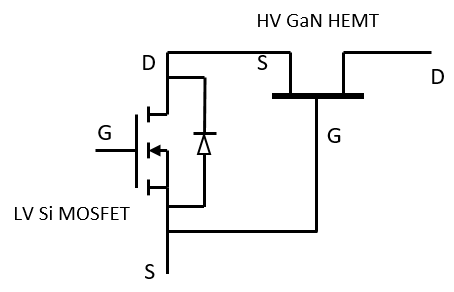
|  |  |
| --- | --- |
|  |  |
|  | (b) |
|  |  |
| (c) | (d) |
|  |  |
| (e) | (f) |

38Figure 3.2.2: Using Cadence Orcad to evaluate cascode GaNFET TPH3205WSB of (a) Rg\_on effect for turn-on event; (b) Rg\_on effect for turn-off event; (c) Rg\_off effect for turn-on event; (d) Rg\_off effect for turn-off event; (e) Cs effect for turn-on event; (f) Cs effect for turn-off event

Cascode GaN devices exhibit much higher input capacitance in comparison to that of e-mode GaNFETs, which results in a slower switching transition and lower maximum operation frequency. The main reason for such high input capacitance is that the cascode GaNFETs are required a sufficient protection to ensure the actual gate-source voltage of FET is relatively unchanged by a voltage oscillation caused by parasitic inductance within gate driving loop of the DUT. This issue and corresponding solation will be addressed in the Chapter 3.3.

## 3.3: Proposed Cascode GaN Device Gate Driver

There are two types of GaN power devices are available in the commercial market, pure eGaNFETs and two-chip cascode GaNFETs. The pure eGaNFETs are enhancement-mode devices, which exhibit two major challenges during design. Namely, a relatively low gate threshold voltage and very narrow gate-source voltage safety margin. This makes eGaNFETs gate drive design become more complex and challenging and thereby results in a reduction in turn-on dv/dt and di/dt [9]. In contrast, cascode GaNFFET exhibit higher gate threshold voltage and much wider gate-source voltage operation margin in comparison to that of eGaNFETs due to the use of a LV Si MOSFET in the cascode structure [10]–[12]. The cascode GaN device configuration as shown in Fig. 3.3.1.



39Figure 3.3.1: Cascode GaNFET configuration

However, a large input capacitance is required to act as a protection for the gate-source voltage oscillation [13]. This is because the existence of an inevitable voltage oscillation caused by a parasitic inductance in gate return path. The switching transients and maximum operation frequency of cascode GaNFET are accordingly limited by this large input capacitance. Such high input capacitance also introduces a higher driving loss and possible higher switching loss if gate-source voltage oscillation exceeds certain margin imposed by the cascode GaNFET itself. Therefore, a unique consideration needs to be taken in account when cascode GaN devices are used in the design. Moreover, one of the biggest drawbacks of cascode GaNFETs is slower switching transient in comparison with pure eGaNFETs. While the switching transient of cascode GaNFETs can be improved by reducing the input capacitance. Hence, the trade-off between gate-source voltage oscillation protection and switching speed is vitally important for cascode GaNFETs. Table 3.4 shows the key specification comparison between e-mode GaNFET (GS66508B) and cascode GaNFET (TPH3205WSB) in terms of switching speed prospective for a given voltage/current rating [14][15].

10**Table 3.4: Comparison between GS66508B and TPH3205WSB from switching speed prospective (@ 25°C)** [14][15]

|  |  |  |
| --- | --- | --- |
| **Parameter** | **GS66508B** | **TPH3205WSB** |
| Gate Charge (Qg/nC) | 6.1 | 28 |
| Input Capacitance (Ciss/pF) | 242 | 2200 |
| Gain-Source Voltage Driving Range (V) | -10 to +7 | -18 to +18 |
| Turn On Delay Time + Rise Time (ns) | 7.8 | 43.6 |
| Turn Off Delay Time + Fall Time (ns) | 13.2 | 48.6 |
| Drain-Source Blocking Voltage (V) | 650 | 650 |
| Transient Drain-Source Voltage (V) | 750 | 800 |
| Drain-Source Current (A) | 30 | 35 |
| Gate Threshold Voltage (V) | 1.7 | 2.1 |
| Drain-Source On-state Resistance (Ω) | 50m | 49m |

Three version PCBs are made to investigate the source of afore-mentioned gate-source voltage oscillation and evaluate the importance of key parasitic elements within gate driving loop. Cascode GaN device (TPH3205WSB) from Transphorm is used, and double pulse test (DPT) circuit is selected for the experimental test as drawn in Fig. 2.2.10. A SiC freewheeling diode (FFSH3065B-F085) is used to provide freewheeling path and eliminating reverse recovery phenomenon caused by high-side device. The reason for cascode GaNFETs have such high input capacitance (2200pF in this case) is that to ensure the actual gate-source signal of FET die is relatively unchanged by gate-source voltage ringing. All parasitic elements within gate driving loop as illustrated in Fig. 3.3.2. A significant gate-source voltage oscillation is found during turn-on transition of casocde GaN device. However, such phenomenon does not occur during e-mode GaNFET (GS66516T) hard-switching turn-on as illustrated in Fig. 3.3.3. Such high-frequency gate-source voltage ringing could affect drain-source voltage and therefore result in an increase in switching loss, which is undesired. It is obviously that the cascode GaN device exhibits a more significant drain-source voltage ringing in comparison to that of e-mode GaN device. Since there is a certain amount of unavoidable parasitic inductance located in the connection pins of the cascode GaN device with TO-247 package. Among all parasitic inductance and capacitance, source-side parasitic inductance in gate return path () and gate turn-on inductance () are assumed having direct influence on gate-source voltage oscillation. This is due to integrated gate driver IC (Si8271) is applied in order to minimise the parasitic capacitance (,) and inductance (,) introduced by gate drive circuitry.

|  |
| --- |
|  |
| (a) |
|  |
| (b) |

40Figure 3.3.2: Gate loop analysis of (a) turn-on; (b) turn-off

|  |
| --- |
|  |

41Figure 3.3.3: Switching waveform comparison of cascode GaNFET and e-mode GaNFET

In order to find out the source to cause such high-frequency gate-source voltage ringing, three version PCBs have similar power loop while different gate driving loop design are made. Key parasitic inductances comparison among three version PCBs as illustrated in Table 3.5, which are extracted via Ansys Q3D. Based on the practical parasitic inductance extraction of three version PCBs, a series of simulations using Cadence Orcad were conducted as drawn in Fig. 3.3.4 to firstly identify the source to cause high-frequency gate-source voltage ringing. The original board (labelled as ‘before amendment’ in Fig. 3.3.4), a significant gate-source voltage ringing can be obversed. In more specific terms, during turn-on, a maximum -20V voltage spike as illustrated in Fig. 3.3.4 (a); during turn-off, a 5V voltage spike is found, which could potentially result in false turn-on. In accordance with the simulation results, the optimisation of gate driving loop as shown in Table 3.5 can significantly improve the gate-source voltage waveform. Apart from simulation evaluation, practical tests were also conducted for experimental demonstration purpose. The original board is made to evaluate the switching performance of cascode GaNFET without careful gate drive circuitry design. In order to further investigate the influence of gate driving loop to the switching performance of cascode GaNFET, additional two PCBs are made. Compared to the original board, the 1st amended board has an increased gate turn-on inductance whereas reduced source-side parasitic inductance. With respect to the 2nd amended board, both gate turn-on inductance and source-side parasitic inductance are optimised during layout design. The experimental measured gate-source voltage and drain-source voltage of three PCBs as depicted in Fig. 3.3.5. A differential probe (P5202A) from Tektronix was used to extract the gate-source voltage of each version of PCB and a high voltage measurement probe from RS Pro with 1:100 ratio was used to record drain-source voltages. Apart from conventional measurement for the power devices, the measurement for voltage oscillation caused by source-side parasitic inductance in gate return path is also important for verification purpose. The way to measure this voltage oscillation/source ringing as shown in Fig. 3.3.5 (a), namely, one measurement probe is connected to the ‘GND’ pin of the gate driver IC and another is connected to the source pin of the DUT. The source ringing/oscillation measurement of three PCBs are depicted in following pictures of Fig. 3.3.6. All experimental measurement results as concluded in Table 3.6.

11**Table 3.5: Comparison of key parasitic inductance in gate driving loop in three PCBs**

|  |  |  |  |
| --- | --- | --- | --- |
| **Objective/unit** | **Original board (PCB V1)** | **1st amended board (PCB V2)** | **2nd amended board (PCB V3)** |
| Gate turn-on inductance /nH | 5.6012 | 9.4462 | 4.4326 |
| Source side parasitic inductance /nH | 10.376 | 4.2235 | 1.092 |

|  |
| --- |
| Chart  Description automatically generated |
| (a) |
| Chart, line chart  Description automatically generated |
| (b) |

42Figure 3.3.4：Simulation result of three version PCBs (a) turn-on; (b) turn-off @ 400V/5A

|  |  |
| --- | --- |
|  |  |
| (a) | (b) |
|  |  |
| (c) | (d) |
|  |  |
| (e) | (f) |

43Figure 3.3.5: Switching waveform comparison of three version PCBs @ 400V/5A of (a) PCB V1 turn-on; (b) PCB V1 turn-off; (c) PCB V2 turn-on; (d) PCB V2 turn-off; (e) PCB V3 turn-on; (f) PCB V3 turn-off

|  |  |
| --- | --- |
|  |  |
| (a) | (b) |
|  |  |
| (c) | (d) |

44Figure 3.3.6: (a) source ringing measurement; experimental measurement of source ringing measurement @ =100V of (b) original board (PCB V1); (c) 1st amended board (PCB V2); (d) 2nd amended board (PCB V3)

In accordance with Fig. 3.3.5 (a), a significant gate-source voltage oscillation is found in original board, and accordingly drain-source voltage waveform is affected by this gate-source voltage oscillation. Thus, gate driving loop as shown in Fig. 3.3.2 is assumed as the starting point of following analysis and evaluation. As illustrated in Fig. 3.3.2, the gate turn-on inductance in gate turn-on path and source-side parasitic inductance in gate return path are highlighted as the source to cause such significant gate-source voltage oscillation during turn-on period. In order to conduct further investigation, additional two boards with different gate driving loop whereas similar power loop design are made. Two key parasitic inductances comparison among these three PCBs as documented in Table 3.5. As illustrated in Fig 3.3.6 (b), the shape of source ringing is like to gate-source voltage oscillation, which indicates such high frequency gate-source voltage oscillation is highly depending upon the amount of source-side parasitic inductance. The 1st amended board with higher gate turn-on inductance whereas smaller source-side parasitic inductance is made for comparison purpose. As shown in Fig. 3.3.6 (c), the 1st amended board achieve an 8.4V reduction in source ringing as well as a 150ns shorter oscillation duration. The drain-source voltage waveform become much more stable in comparison to that of original board. This further proves that the gate-source voltage oscillation in cascode GaNFET is more relevant to source-side parasitic inductance rather than gate turn-on inductance. With further optimisation of both gate turn-on path and gate return path, both gate turn-on inductance and source-side parasitic inductance have been reduced in 2nd amended board as documented in Table 3.5. As a result, the 2nd amended board attain a 15.4V reduction in source ringing and a 320ns shorter source ringing duration, which significantly lower the gate driving loss. Moreover, the oscillation in drain-source voltage has been greatly reduced and settle down to its steady-state level in 25ns, which saves about 8uJ Eon at 400V/5A in comparison to that of original.

It is worth to point out the amendment rules applied during this evaluation:

1. Eliminating the vias/traces/power plane underneath the gate driver/isolation as depicted in Fig.3.3.7 (a), and therefore lower input-output capacitance of gate driver, also reduce the interference between gate loop and power loop.
2. The gate return path has been shorten as shown in Fig. 3.3.7 (b). This can effectively reduce the magnitude of source-side voltage ringing. Moreover, in 2nd amended board, the gate return path has been optimised by applying power plane for GND connection.
3. Additional Ferrite bead (60ohm@100MHz) is added to further damp high frequency Vgs ringing.

|  |
| --- |
|  |
| (a) |
|  |
| (b) |

45Figure 3.3.7: Gate return path comparison of original board (PCB V1) and 1st amended board (PCB V2) (indicated as yellow line)

12**Table 3.6: Experimental measurement of three version PCBs**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Parameter/unit** | **Original board (PCB V1)** | | **1st amended board (PCB V2)** | | **2nd amended board**  **(PCB V3)** | |
|  | Turn-on | Turn-off | Turn-on | Turn-off | Turn-on | Turn-off |
| /V | 28.4 | 10.3 | 13 | 10 | 10.3 | 10 |
| /V | 26.3 | 7.8 | 12.2 | 8.1 | 9.6 | 8.1 |
| /V | 438 | 403 | 413 | 406 | 409 | 400 |
| /V | 400 | 400 | 397 | 400 | 402 | 399 |
| Source ringing @=100V /V | 18.3 | | 9.9 | | 2.8 | |
| Source ringing  duration@=100V /ns | 510 | | 360 | | 190 | |
| Switching loss/uJ | 63.64 | | 55.7 | | 52.13 | |

Chart

Description automatically generated with low confidence

46Figure 3.3.8: Simplified gate drive resonant loop

As a result, the source-side parasitic inductance shows a more significant influence on gate-source voltage waveform in comparison with gate turn-on inductance. As shown in Fig. 3.3.8, both and become larger in the case of cascode GaNFET and lead to an additional source to cause gate-source voltage oscillation. Therefore, the gate return path design should be taken into consideration in priority for cascode GaNFET-based design compared to gate turn-on path. A well-designed gate drive circuitry can significantly improve the switching performance of cascode GaNFETs, and hereby no longer require that high input capacitance to prevent the gate-source voltage oscillation caused by source-side parasitic inductance. The finished 2nd amended board PCB layout and its practical view as illustrated in Fig. 3.3.9. In 2nd amended board, the gate driving loop has well-considered in terms of both gate turn-on path and gate return path. Therefore, the 2nd amended board shows a stable switching waveform in terms of gate-source voltage, drain-source voltage as well as drain current as illustrated in Fig. 3.1.8. The device switching speed of this board can be further enhanced by taking off the optional ferrite bead. As measured in Fig. 3.1.10, even without ferrite bead, the drain-source voltage waveform is unaffected by gate-source voltage oscillation and the Ton can be reduced by 5.5ns in comparison to that of with ferrite bead. Meanwhile, the source ringing measurement at 100Vds is also shown in Fig. 3.1.10, the amplitude of source ringing increased from 1.9V to 3.7V by taking off ferrite bead, whereas this still in an acceptable range due to stable drain-source voltage when device operating at 400V level.

|  |  |
| --- | --- |
|  |  |
| (a) | (b) |

47Figure 3.3.9: The 2nd amended board (PCB V3) (a) PCB layout; (b) practical view

|  |  |
| --- | --- |
|  |  |
| (a) | (b) |

48Figure 3.3.10: Experiment measurement of 2nd amended board (PCB V3) without ferrite bead of (a) and @ 400; (b) source ringing and @ 100

In order to investigate the possible future development for cascode GaN devices. A series of simulations based on the practical PCB parasitic inductance measurement of 2nd amended board are conducted for verification purpose. The simulation model is modified by author, which is based on the experimental measurement as shown in Fig. 2.2.11. Apart from the model in Chapter 2, another two simulation models are created for evaluation. The main difference among these three simulation models of cascode GaNFEET is that the LV Si MOSFET input capacitance value due to Si MOSFET contributes the majority of the input capacitance to the entire cascode GaNFET. According to the simulation result as shown in Table 3.7, it is possible to boost cascode GaNFET switching speed by replacing a LV Si MOSFET with smaller input capacitance without costing of switching loss.

13**Table 3.7: Simulation verification via Cadence Orcad @ 400V/5A**

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| --- | --- | --- | --- |
| **Parameter** | **Original Spice Model** | **Spice Model I** | **Spice Model II** |
| /pF | 2141.48 | 1641.48 | 1141.48 |
| Ton/ns | 35.34 | 34.2 | 30.899 |
| Toff/ns | 101 | 94.9 | 86.88 |
| Switching losses/uJ | 38.2 | 37.63 | 37.17 |

As shown in Table 3.7, with a 500pF reduced input capacitance, the Ton and Toff can be reduced by 1.14ns and 6.1ns respectively. It is necessary to address that the reduction in LV Si MOSFET is achieved by varying different kinds of MOSFET that are commercially available in the market. If the input capacitance of LV Si MOSFET further reduces by 1000pF, the Ton downs to 30.899ns and Toff drops to 86.88ns, which attains a 4.441ns and a 14.12ns for Ton and Toff respectively. Thanks to the maturity of Si technology and large Si MOSFET market. By far, there are countless Si MOSFET manufacturers can offer low input capacitance (about 1000pF) Si MOSFET in targeted voltage range (35-40V), such as Infineon Technologies, Nexperia [16][17]. Consequently, following proposed gate drive circuitry consideration, the cascode GaNFET is expected to achieve faster switching speed and maximum operation switching by replacing a LV Si MOSFET in cascode package with lower input capacitance (). However, a vitally important trade-off between input capacitance and conduction loss/junction temperatures needs to be taken into further consideration. A cascode GaN device with a lower input capacitance LV Si MOSFET will likely has higher conduction loss and junction temperatures owing to smaller chip size.

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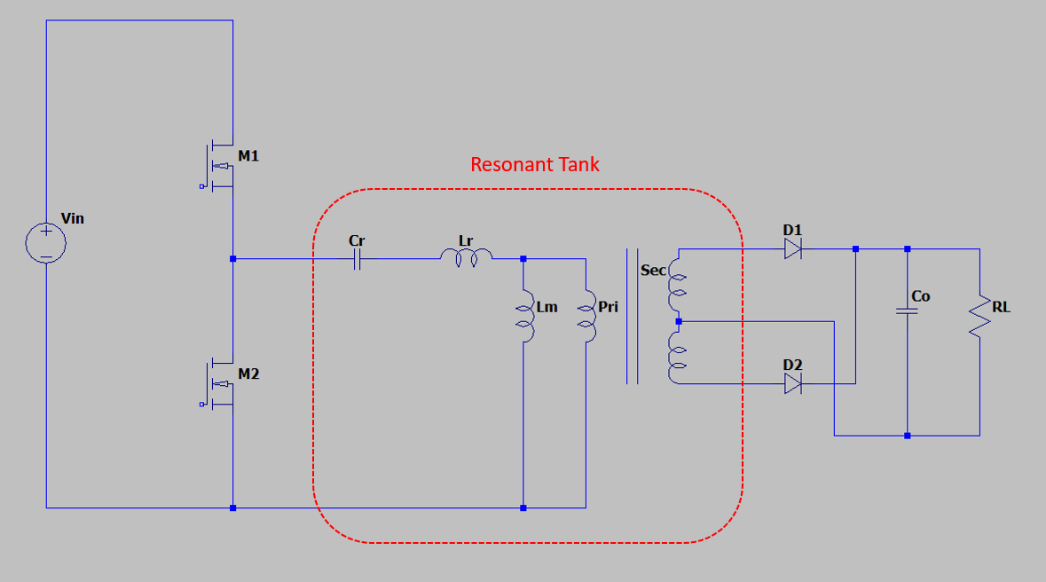
# Chapter 4: Evaluation of Cascode GaN-based Converter

Solid-state electronics application is the cornerstone of power electronics, which is used to control and converter one form of electrical power to another form. Power electronic converters act as the interface among all kind of different electrical forms, taking one electrical energy from its source and converting it into an appropriate form required by a motor. Therefore, the specification of a converter is determined by given power source and driving motor/load. Power semiconductors play a significant important role in any kinds of converter, which also determines the efficiency, cost as well as size of power electronic or electrical system. It is worth pointing out the power converters are widely used in myriad power conversion applications, which can be used from fraction of volt towards thousands of volts level. The advancement of soft-switching technique will be studied. Furthermore, this chapter will continue study the impact of gate drive circuitry to the cascode GaN-based converter under hard-switching (CCM) and soft-switching (CRM) operation.

## 4.1: Emerging GaN-based Topologies

With the emerging of GaN devices, there are many topologies become prevalent owing to the advancement of fast switching feature. Among all kinds of those topologies, LLC resonant converter and totem-pole bridgeless power factor correction (PFC) rectifier are the most discussed topologies that use GaN devices.

To commence with, with the increasingly demands and trends toward higher power, smaller size and higher efficiency, a high-frequency LLC resonant converter becomes a highly appealing solution as an isolated DC-DC topology. For instance, from a low power laptop adaptor (about 100W) to a higher power datacentre power supply unit (1kW-3kW). Moreover, the GaN-based LLC resonant converters is emerging in the on-board charger (OBC) for EVs that is normally rated at few kilowatt [1]. A typical half-bridge LLC resonant converter is shown in Fig. 4.1.1. The use of GaN devices can improve the switching frequency of such LLC resonant converter. Hence, it is obvious that the passive components’ size can be significantly reduced, such as resonant inductors ( and ), resonant capacitor () as well as the transformer, which can eventually achieve an improvement in power density. It is necessary to address that the LLC resonant converter topology exhibits several benefits owing to its full resonant behaviour and enabling soft-switching turn-on over the entire range, which minimises losses from both power devices and magnetic components’ perspective.



49Figure 4.1.1: Typical half-bridge LLC resonant converter

The primary side current () and voltage waveform as drawn in Fig. 4.1.2, which comprises a superposition of the secondary side current divided by the transformer turns ratio and the magnetising current (). It must be mentioned the magnetising current does not transfer to the output, however, is required to discharge the parasitic output capacitance of the power devices as well as a combination of the transformer intra-winding and associated capacitance to achieve ZVS turn-on at no cost of loss. To achieve ZVS turn-on, the parasitic output capacitance of the power devices should be completely discharged via the magnetising current during every dead time period. On the other hand, the magnetising current will cause extra circulating loss on the primary side during dead time. Therefore, the most important task for enhancing the efficiency of a high frequency LLC converter is minimising the magnetising current.

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| Diagram, schematic  Description automatically generated | Diagram  Description automatically generated |

50Figure 4.1.2: Primary side current and voltage waveform for half-bridge LLC resonant converter

With respect to the minimum dead time requirement for a half-bridge LLC converter to achieve ZVS turn-on can be described as equation 4.1, where is the magnetising inductance of the primary side of the transformer, is the switching frequency, and is the amount of output capacitance required to transition the drain to source voltage passively [1]. In accordance with the equation 4.1, the lower of the effective , the less magnetising current is required for a given drain to source transition time, which shows higher allowance of magnetising inductance for the transformer and enables shorter dead time. In the meantime, the lower value of the effective reduces the circulating loss on primary side of the transformer. Moreover, for a given magnetising inductance and dead time, the lower of the effective , the higher switching frequency and hence the greater the power density can be obtained when combined with ZVS operation.

(4.1)

Apart from the effective , the gate-drain charge of the power device () is also important, which describes the charge required for the gate to drain switching. indicate the turn-off capability and losses are highly depended upon the of the device and the switching turn-off time (, which determines the maximum switching frequency as well as efficiency. Si-based power devices and SiC MOSFETs are facing a significant challenge which is related to body diode reverse recovery charge. There is a potential reliability concern of the system caused by the incomplete body diode reverse recovery of the MOSFETs for any LLC resonant converters [2]. It is worth point out that the existing reverse recovery charge of the body diode will cause high dv/dt and a large shoot-through current will flow through the bridged power devices, which might give rise to a MOSFET breakdown. Compared to Si and SiC MOSFETs, the features of GaN devices, such as lowest effective , gate charge (), gate-drain charge () and nearly zero reverse recovery charge () and therefore making GaN-based LLC resonant converter become a superior power supply design [3][4].

The totem-pole bridgeless PFC rectifier become a prevalent solution for applications such as telecommunication PSUs and front-end converters in server and with the emerging of GaN power devices. Fig. 4.1.3 shows the schematic of totem-pole bridgeless PFC rectifier. The fundamental reason for this is the dramatic performance enhancement of GaN power devices over their Si equivalents, particularly is superior FOM as well as significantly lower body diode reverse recovery charge. The crucial drawbacks of Si MOSFET-based totem-pole PFC limit the use of this simple topology. In more specific terms, the tremendous turn-on switching loss and parasitic oscillation caused by the reverse recovery effect of the anti-parallel diode. The use of CRM technique to achieve soft-switching operation in Si-based totem-pole PFC rectifier can alleviate afore-mentioned issues by ZVS turn-on of the control switch and ZCS turn-off the body diode. However, the increased current ripple results in higher turn-off switching loss and conduction loss. Therefore, the Si-based totem-pole PFC rectifier using CRM technique is limited to the low frequencies and low power level applications. Significant efforts have been made to demonstrate the benefits of GaN-based totem-pole PFC rectifier using hard-switching technique [5]-[7]. Thanks to the lower reverse recovery charge of the GaN HEMT compared to that of the Si MOSFET, the totem-pole bridge converter realises the hard-switching operation. As proven in [8]-[10], the cascode GaN-based totem-pole PFC rectifiers enable above 1MHz switching frequency with CRM soft-switching operation.

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51Figure 4.1.3: The schematic of totem-pole bridgeless PFC rectifier

## 4.2: Analysis of Cascode GaNFET-based Converter

GaN device as one of most representative WBG-based power devices has drawn an increasing attention in low-medium voltage range application. Recently, the GaN-based mobile/laptop chargers have emerged, which realises three times faster charging speed in half size and weight [11]. In the meantime, GaN-based devices present excellent potential and capability in hybrid-electric and electric vehicles from entry level to premium models, which enables faster charging, farther driving as well as lowering barriers to high adoption [12].

The cascode structure is used to a depletion-mode GaN HEMT to achieve normally-off operation. Due to the use of LV Si MOSFET, the interaction within the cascode device package between LV Si MOSFET and HV GaN HEMT might cause some undesired features. The parasitic inductance and junction capacitor ratio between two discrete devices within the package require a careful design to prevent failure and enhance switching performance of the cascode device. Consequently, there are three major concerns during the design of cascode GaNFET, which are so-called Si MOSFET avalanche, GaN HEMT gate failure and divergent oscillations during turn-off transition at high current condition. The related solutions to aforementioned issues of cascode GaNFET design have been proposed in [13]–[15]. Therefore, the current cascode GaN devices available in the market are proved without significant drawbacks in term of reliability and switching performance.

### 4.2.1: Hard Switching Vs. Soft Switching

There is no doubt that with the adoption and development of GaN material and related techniques, GaN-based power devices realise a much better switching performance under hard switching in terms of switching speed, operation temperature, switching frequency compared to that of Si-based counterparts [16]–[19]. Both [16] and [17] are provided by the manufacturers, while the system operation frequency is below 100kHz. On the other hand, soft switching mode has been assumed as a proper approach to fully enable the advantages that GaN brings from noise and loss prospective.

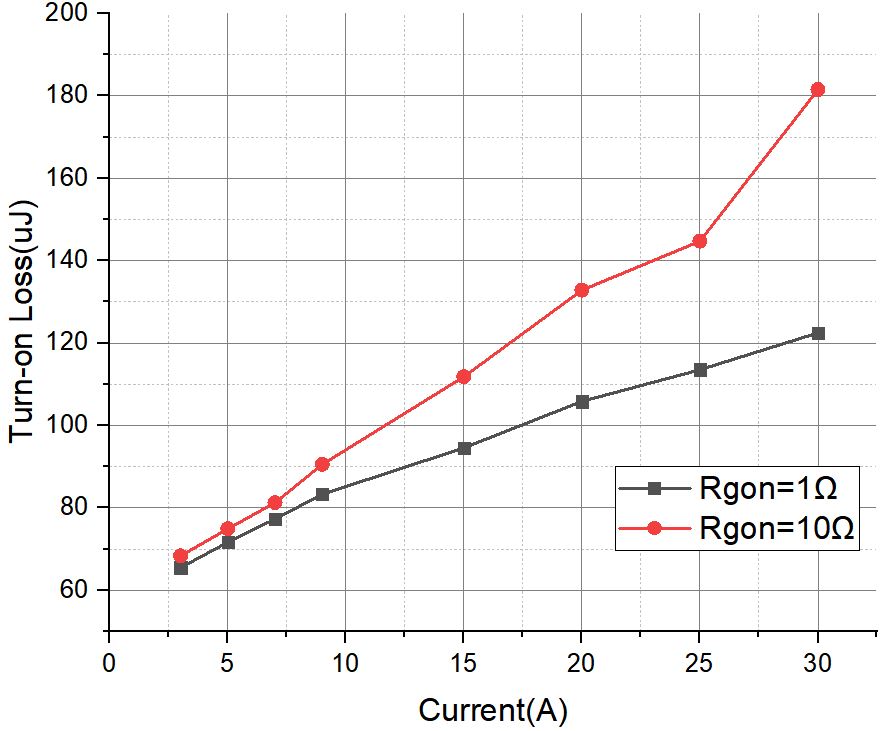
Hard switching and soft switching are two main operation modes for any power devices. A GaN-based half bridge double pulse test prototype is built in LTspice for the study of these two operation modes as shown in Fig. 4.2.1. GS66516T from GaN Systems is selected in order to assure minimal parasitic inductance owing to GS66516T is manufactured in surface mount package. Fig. 4.2.2 shows the hard switching turn-on waveforms of GS66516T under different conditions of (a) significant parasitic elements; (b) less parasitic elements. According to Fig. 4.2.2 (a), both drain-source voltage and current waveforms contain significant high frequency ringing (100-200MHz). Moreover, the high drain-source voltage and high drain current overlaps with each other for a relatively long time (> 15ns) and thereby result in a significant loss during this period. In the meantime, a large high frequency voltage ringing is observed in gate-source voltage waveform, which is mainly due to the coupling effect through gate-drain capacitor. An increased value of gate resistance is normally applied to avert abovementioned issues due to the larger the gate resistance, the slower the switching speed as shown in Fig. 4.2.2 (b).

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| 52Figure 4.2.1: GS66516T switching loss double pulse test bench |

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| (a) |
|  |
| (b) |

53Figure 4.2.2: GS66516T hard-switching turn-on transition with (a) severe parasitic elements; (b) less parasitic oscillation by increased gate resistance

After amendment, which is done by enlarging gate resistance, the slew rate of drain-source voltage is reduced. Meanwhile, one overshoot can be observed in drain current waveform owing to the unavoidable junction capacitor charge of the freewheeling switch. Moreover, the gate-source voltage gradually rises toward its steady-state value with a more obvious miller plateau period due to the switching speed is slowed down, whereas there is no voltage ringing can be observed in gate-source voltage waveform. However, the transition time of GS66516T rises from 20ns to 32ns and Fig. 4.2.3 shows the turn-on switching loss comparison with different gate turn-on resistance, which shows an about 40% increased loss at 400V/20A operation when 10 Ω gate turn-on resistor is used in comparison to that of 1 Ω. As a result, the turn-on switching loss and switching speed are controlled by gate turn-on resistance. In the meantime, the turn-on switching loss is much larger than turn-off switching loss as demonstrated in Fig. 2.2.10. In hard switching condition, the turn-on switching loss occupy a large portion of the total loss, hence it becomes the most significant target during the system optimisation for most of GaN-based designs and applications.



54Figure 4.2.3: GS66516T turn-on loss vs. turn-on gate resistance (Rgon) under hard switching

As discussed above, the hard switching turn-on is obviously unable to achieve both lower power loss and less noise/ringing simultaneously. Relatively large turn-on switching loss in hard switching condition become a major limitation to improve the switching performance in terms of efficiency prospective. In contrast, the soft switching turn-on can significantly reduce both turn-on switching loss as well as noise at the cost of slightly increased conduction loss [20][21]. Although there are other soft switching techniques, such as converters with isolating transformers, ZVS enabled by active switching of auxiliary devices etc. As reported in [13], the critical conduction mode (CRM) is the most effective and simple method to attain zero voltage switching (ZVS) turn-on and broadly implemented in low-medium power applications. A synchronous 400V/200V GaN-based (GS66516T) buck converter is built in Cadence Orcad for further investigation as illustrated in Fig. 4.2.4. The SPICE model used in the simulation is provided by GaN Systems, which shows a very little error (<4%) compared to the experimental measurement [22]. Moreover, the CRM is able to attain both zero voltage switching (ZVS) turn-on for the active control switch (TS in Fig. 4.2.4) and zero current switching (ZCS) turn-off for bottom freewheeling switch (BS in Fig. 4.2.4) as shown in Fig. 4.2.5. Nevertheless, it is necessary to mention that the main drawback of the CRM operation is the inductor peak current become twice or more than the output load current, which might give rise to an increase in turn-off switching loss () as well as a minor penalty of increased conduction loss and inductor loss [23]. However, as demonstrated in Fig. 2.2.10, the turn-off switching loss of GaN devices is relatively low and not sensitive to the load current. In a more specific term, the turn-off switching loss for 650V cascode GaN devices is lower than 16uJ, and e-mode GaNFETs exhibit even smaller turn-off loss. Furthermore, the root-mean-square (RMS) value of the inductor current, which can be considered as a triangular waveform current, is about 15% higher in comparison to that of a pure DC current for a given DC value in accordance with mathematical calculation. As a result, the conduction loss under CRM operation can be increased by 33% at most. Thus, the CRM operation can be considered as the most simple and effective approach to improve system efficiency due to the saved turn-on switching loss is much larger than the amount of increased conduction loss plus turn-off switching loss. The main targeted device in this chapter is cascode GaN device. As discussed in Chapter 1.3, for a cascode GaN device, the miller capacitor is charged by a current source and gate driver is able to switch-off the cascode GaN device as fast as possible. Therefore, the corresponding turn-off switching loss is relatively low and making the cascode GaN device not sensitive to the turn-off current. This helps to the adoption of the CRM technique applied to cascode GaN-based applications. The ripple requirement is strict when CRM technique is applied, the output capacitor and load inductor should be carefully designed. The passive components are selected based on manufacturer components list, since the evaluation kit made by manufacturer is the main comparison object [16]. The superiority and advancement of soft switching over hard switching as depicted in Fig. 4.2.6 (a), and Fig 4.2.6 (b), shows the control switch (TS) turn-on switching loss () comparison under two different operation modes. The loss breakdown at 400V/10A is illustrated in Fig .4.2.6 (c).

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| 55Figure 4.2.4: Synchronous buck converter scheme |

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| 56Figure 4.2.5: Operation principle of critical current mode (CRM) |

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| (a) |
|  |
| (b) |
|  |
| (c) |

57Figure 4.2.6: Comparison between hard-switching (CCM) and soft-switching (CRM) @ f\_sw=200kHz (a) buck converter efficiency; (b) turn-on switching loss; (c) loss breakdown at 400V/10A

### 4.2.2: High dv/dt and di/dt issues

One of the merits of GaN-based power devices in comparison to Si MOSFET is that lower turn-off switching loss () owing to GaN enables higher switching speed capability. The external gate drive circuit is vital to attain a very fast switching speed when GaN device is implemented owing to zero voltage switching (ZVS) turn-on is preferred for all kinds of GaN devices in order to reduce large turn-on loss. As a result, the external gate drive circuit design should pay more attention on turn-off transition.

Gate resistor (), as most important part in any gate drive circuit, also play a significant role in the GaN devices in terms of turn-off transition. The gate turn-off resistor () restricts the gate discharging current and hereby decelerate the drain-source voltage as well as drain current transitions as depicted in Fig. 4.2.5. Consequently, the turn-off energy can be reduced when a lower gate turn-off resistance is used as shown in Fig. 4.2.6. It is worth pointing out that the external gate resistor is less effective in cascode GaNFETs owing to the HV GaN HEMT in cascode structure is actually controlled by LV Si MOSFET. The internal gate resistance is normally very small and mainly designed for limiting the gate current and damping internal ringing caused by parasitic inductance.

A small gate resistor is preferred in order to lower the turn-off loss of the GaN device. In general, gate voltage oscillation in certain range is allowed by most of GaN devices. However, a special consideration needs to be taken to prevent the gate voltage ringing rise above the gate threshold of the device. Hence, the gate driving loop inductance should be well designed and keep it as low as possible. There are two common reasons for resulting in gate voltage ringing, one is miller feedback capacitance due to high dv/dt, another is so-called source bounce caused by source inductance. If a large gate voltage ringing is created by high dv/dt, then an external gate resistor of larger resistance located in gate turn-on path is recommended; whereas if the gate ringing is mainly caused by source inductance, then the best approach to mitigate such ringing is to optimise the PCB layout and thereby reduce the source inductance.

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| 58Figure 4.2.5: GS66516T turn-off transition with different gate turn-off resistor |

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| 59Figure 4.2.6: GS66516T turn-off loss comparison with different gate turn-off resistor |

Apart from the considerations related to gate/power loop, the high dv/dt and di/dt issue is also critical when GaN devices are used in the design. The use of CRM to attain soft switching will further aggravate such high dv/dt and di/dt concern due to very high turn-off current as illustrated in Fig. 4.2.5. According to Fig. 3.2.1, the GaN-based power devices exhibit about 5-6 times higher dv/dt and di/dt in comparison to that of Si MOSFET. Consequently, such high dv/dt and di/dt pose novel challenge to the GaN devices’ circuit design.

As discussed in Chapter 2.2, the common source inductance (CSI) in device package plays an important role in terms of eventual switching performance. In the meantime, the CSI is normally formed by two parts, which consists of package parasitic inductance located in source terminal as shown in Fig.2.2.12 as well as the parasitic inductance in PCB traces. During GaN device turning off, the CSI induces a negative voltage due to falling di/dt. Such negative voltage will induce an opposing voltage across the gate drive voltage and thereby increase the Miller turn-on sensitivity. In order to identify the hazard that high di/dt bring, the buck converter as drawn in Fig 4.2.7 is used, additional CSI is applied to the circuit in order to identify the large CSI impact on the GaN device’s switching waveforms. As shown in Fig 4.2.8, a 3.8V voltage spike is observed in top switch Vgs waveform, which might spurs a false turn-on of the top switch as soon as the internal gate signal attains its threshold voltage and eventually results in shoot-through. As a result, di/dt might induce an opposing voltage drop on the CSI which prevents either turn-on or turn-off from the gate drive circuit. Therefore, it is vital important to enhance the di/dt immunity by minimising CSI during GaN-based circuit design. If applicable, separating the gate driving loop and power loop via so-called Kelvin connections can be significantly mitigate the issue that high di/dt brings.

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| 60Figure 4.2.7: di/dt impact on gate driving loop |

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| 61Figure 4.2.8: spikes induced by high di/dt   |  | | --- | |  |   62Figure: 4.2.9: waveform with less di/dt |

With respect to dv/dt issue, it usually occurs to the high-side device in a converter with half-bridge configuration during high positive/negative switch node dv/dt. It is well-known that the switch node dv/dt generates a common-mode current, and parasitic capacitance of the high-side gate driver forms a high frequency noise path for this common-mode current. Fig. 4.2.10 illustrates the loop of common-mode current, which is generated by a high voltage slew rate across input-output capacitor () during positive dv/dt. Such common-mode current could introduce a ground bounce on the input side of PWM signal, and hereby may lead to variations/changes in the logic state. On the other hand, the common-mode current flows in clockwise direction and might deteriorate the PWM signal during negative dv/dt as shown in Fig. 4.2.11 [20]. Especially, the use of GaN devices leading to a very high slew rate (might exceed ) at switch node. There is a significant amount of literature on mitigating crosstalk in fast switching power devices, ranging from using different gate resistance (), miller clamps as well as active gate driving [24]-[26]. The dv/dt issue is common to all GaN-based designs/applications that have a high-side floating device and required to be addressed in order to avert becoming a limiting factor in terms of circuit performance.

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| 63Figure 4.2.10: Common-mode current across parasitic capacitance of isolation caused by high dv/dt [20] |

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| 64Figure 4.2.11: A fault signal induced by high dv/dt [20] |

The approaches to mitigate abovementioned high dv/dt issues as following:

1. Minimising the parasitic capacitance and make the high-side gate driver power supply as simple as possible. Therefore, a high voltage bootstrap diode can be applied. Meanwhile, the decoupling capacitor for the high-side driver power supply (Vcc in Fig. 4.2.9) should place in proximity to the bootstrap diode as well as dv/dt noise source ground to ensure the noise current loop as small as possible.
2. In order to enhance dv/dt immunity, a RC low pass filter and can be used at the PWM input terminal of the driver IC. A negative bias circuit for the input PWM signal is also helpful to improve dv/dt immunity due to the increased withstand margin.
3. A well-designed PCB layout can also improve dv/dt immunity. This is because an additional parasitic capacitance will be caused by the overlap of switch node panel and ground panel, which result in a reduction in dv/dt immunity of high-side driver. Therefore, it is vitally important to eliminate PCB layout overlap between switch node and ground.

## 4.3: Cascode GaNFET-based Synchronous Buck Converter

### 4.3.1: Impact of Gate Driver Design to Cascode GaNFET-based Converter

Significant effort has been made for the investigation and development of cascode GaN devices [27]–[31], whereas most of presented researches are focusing on power loop and common source inductance optimisation [32]–[34]. As discussed in Chapter 3, the gate driving loop also has critical influence on cascode GaN devices’s switching performance. Three version PCBs with different gate driving loop as documented in Table 3.3 are made for comparison purpose. All these three PCB exhibit same power loop design and therefore parasitic inductance in power loop. Among three version PCBs, PCB V1, the original board exhibits relatively large gate turn-on inductance (5.6nH) and highest source-side parasitic inductance (10.376nH). Whereas PCB V3, the gate driving loop of 2nd amended board has been optimised and thereby PCB V3 has minimal gate turn-on inductance (4.43nH) and source-side parasitic inductance (1.09nH). Meanwhile, source-side parasitic inductance shows a more significant influence on the high frequency gate-source voltage ringing in comparison to that of gate turn-on inductance as demonstrated in Chapter 3.2.3. Fig. 4.3.1 shows the significance of cascode GaNFET gate driving loop by comparing switching waveforms of PCB V1 and PCB V3. An inappropriate gate driving loop with large source-side parasitic inductance is able to cause a significant high frequency gate-source voltage oscillation, and further result in a variation in drain-source voltage waveform. The drain-source voltage oscillation combined with non-zero drain current can give rise to an increase in switching loss, and the switching loss comparison between PCB V1 and PCB V3 in different current level as illustrated in Fig. 4.3.2. With poor gate drive circuit design (PCB V1), the oscillation in drain-source voltage is more significant and the turn-on switching loss become about 20% higher than that of PCB V3 in all tested current range. Such switching loss should be avoided in order to achieve high frequency and high efficiency operation for cascode GaN-based applications due to the switching loss is normally increasing along with the increase of switching frequency.

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| (a) 400V/3Aturn-on transient of the PCB with 5.6nH gate turn-on and 10.376nH gate return loop inductance | (b) 400V/3A turn-off transient of the PCB with 5.6nH gate turn-on and10.376nH gate return loop inductance |
|  |  |
| (c) 400V/3A turn-on transient of the PCB with 4.43nH gate turn-on and 1.09nH gate return loop inductance | (d) 400V/3A turn-off transient of the PCB with 4.43nH gate turn-on and 1.09nH gate return loop inductance |
|  |  |
| (e) 400V/6Aturn-on transient of the PCB with 5.6nH gate turn-on and 10.376nH gate return loop inductance | (f) 400V/6Aturn-off transient of the PCB with 5.6nH gate turn-on and 10.376nH gate return loop inductance |
|  |  |
| (g) 400V/6A turn-on transient of the PCB with 4.43nH gate turn-on and 1.09nH gate return loop inductance | (h) 400V/6A turn-off transient of the PCB with 4.43nH gate turn-on and 1.09nH gate return loop inductance |

65Figure 4.3.1: and waveform comparison between PCB V1 and PCB V3 (a) V1 turn-on transition @ 400V/3A; (b) V1 turn-off transition @ 400V/3A; (c) V3 turn-on transition @ 400V/3A; (d) V3 turn-off transition @ 400V/3A; (e) V1 turn-on transition @ 400V/6A; (f) V1 turn-off transition@ 400V/6A; (g) V3 turn-on transition@ 400V/6A; (h) V3 turn-off transition @ 400V/6A

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| 66Figure 4.3.2: PCB V1 and PCB V3 switching loss comparison |

### 4.3.2: Simulation and Experimental Verification

In order to evaluate the impact of gate drive circuit to the cascade GaNFET-based applications, both simulation and experimental verification are conducted. The synchronous buck converter with two active switches has been chosen for evaluation purpose as drawn in Fig. 4.3.3. Table 4.1 shows all key parameters used in this work. As indicated in Table 4.1, separated turn-on and turn-off resistors are implemented in order to reduce the possibility of false turn-on caused by high dv/dt and speed-up the turn-off process. Both gate driving loop and power loop inductances are extracted via Ansys Q3D in accordance with the practical PCB layouts. It is necessary to address that the SPICE model used here is the one modified by author as documented in Chapter 2.2. For a synchronous buck converter design, it shows a less than 5% error range in terms of both turn-on and turn-off switching losses.

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| 67Figure 4.3.3: Selected synchronous buck converter scheme |

14**Table 4.1: List of parameters used for evaluation**

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| --- | --- | --- | --- |
| Component/parameter name | | Value | Unit |
| Load inductor | | 500 | uH |
| Turn-on resistor | | 10 | Ω |
| Turn-off resistor | | 2 | Ω |
| Gate driving loop | Gate turn-on inductance | 5.6(V1)/4.43(V3) | nH |
| Source-side inductance | 10.376(V1)/1.092(V3) | nH |
| Power loop inductance | | 5.2 | nH |
| Bus voltage | | 400 | V |
| Output voltage | | 200 | V |
| Switching frequency | | 100 | kHz |

Cadence Orcad, which is a SPICE-based simulation software, has been used to compare the synchronous buck converter performance with different gate drive circuitry design namely, PCB V1 and PCB V3. Accordingly, a synchronous buck converter is constructed in Cadence Orcad, including two identical cascade GaN devices (TPH3205WSB), which are defined as top switch (TS) and bottom switch (BS) respectively as illustrated in Fig. 4.3.3. It is necessary to mention that all parameters filled into simulation are the same as practical PCB V1 and PCB V3 for accurate comparison purpose. As one source to cause additional losses, the corresponding losses caused by inductor parasitic resistance and capacitance equivalent parasitic resistance are estimated in accordance with the datasheet stated value. A ferrite core 500uH inductor with single layer flat winding is used in this work and the associated resistance is 40mΩ; on the other hand, the capacitor-related equivalent resistance is 2 mΩ. Both inductance parasitic resistance and capacitance equivalent resistance are taken into consideration in simulation environment.

There is no doubt that the implementation of CRM in synchronous buck converter as illustrated in Fig. 4.2.4. Switch Ts is the main switch in this case. It is important to note that the main switch can accomplish minial voltage turn-on if the turn-on instant is precisely tuned to half the resonant period after inductor current () crosses zero by any zero-current detection technique [35]. In this work, a synchronous buck converter is used and the key CRM waveforms as drawn in Fig. 4.2.5. Another important factor that need to be taken into account is so-called resonant time (), which is described as half of the resonant period constructed by the inductance of load inductor (L) and the capacitance of device junction capacitors, the equation is accordingly as follows:

(4.1)

During the resoannt period, the charge stored in the junction capacitors of the main switch (Ts) is recyled toward the source, the same amount of charge is stored in the junction capacitors of the free-wheeling switch (Bs). In addition to the reaosnt time, a strictly controlled delay time (), about of the resonant time (), is also the key to permit ZVS operation when zero crossing detection technique is used [36].

Both hard-switching (CCM) and soft-switching (CRM) operation are conducted in order to find out the superiority of soft-switching technique from efficiency perspective as mentioned in Chapter 4.2.1 and to determine the possible maximum efficiency of the converter with proposed gate drive circuitry. A hardware prototype with optimised gate driving loop design and similar power loop parasitic inductance to the PCB V3 is made for experimental demonstration as shown in Fig. 4.3.4. A 500uH load inductor, which has same value as simulation setting, is used in the practical hardware. An integrated gate driver (Si8230) from Silicon Lab is implemented in the hardware buck converter prototype, which provides 2.5kV input-output isolation, very high 45kV/us CMTI and fast 30ns propagation delay time [37]. By implementation of this integrated gate driver IC, the dead time can be easily set by connection a series resistor from the DT pin of the gate driver to its ground. Therefore, regarding to the soft-switching operation (CRM), a 5.9kΩ resistor is used to present a 59ns dead time, which is based on the experimental measurement of turn-off time of the cascode GaNFET. In this work, a 59ns deadtime set by gate driver IC puls 35ns inhrent delay time of the gate drive circuitry, namely, a total of 94ns deadtime is set for both simulation and experimental demonstration based on the equation 4.1. It is necessary to address that the value of load inductor value is also selected in accordance with the equation 4.1 and the inductance used in the manufactuer reference design [16]. Fig. 4.3.5 shows the principle of dead time operation of the gate driver IC.

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| (a) |
|  |
| (b) |

68Figure 4.3.4: View of (a) synchronous buck converter prototype; (b) experimental test environment

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| 69Figure 4.3.5: Typical dead time operation |

The simulation result of V1 and V3 based converter and prototype experimental result in hard-switching (CCM) and soft-switching (CRM) operation as depicted in Fig. 4.3.6. The major difference between V1 and V3 is that the gate drive circuitry design. In more specific terms, the PCB V3 exhibits much smaller source-side parasitic inductance in gate return path compared to that of PCB V1 as indicated in Table 4.1. By reducing the source-side parasitic inductance, the drain-source voltage oscillation become less significant owing to this parasitic inductance can cause a severe voltage oscillation in drain-source voltage waveform as demonstrated in Chapter 2. Moreover, PCB V3’s gate turn-on path has also been minimised to further damp the gate-source voltage oscillation. Therefore, an improvement of buck converter from efficiency aspect is expected by optimising gate driving loop. As indicated in Fig. 4.3.6, regarding to the hard-switching (CCM) operation, the buck converter with PCB V3’s parameters can achieve an average of 0.27% efficiency improvement, whereas for the soft-switching (CRM) operation, an average of 0.138% efficiency improvement is reached.

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|  |
| (a) |
|  |
| (b) |

70Figure 4.3.6: Efficiency comparison between PCB V1 & V3 simulation result and experimental measurement in (a) hard-switching (CCM); (b) soft-switching (CRM)

With respect to the hardware prototype, it was fabricated with proposed gate drive circuitry design, which only exhibits 1nH source-side parasitic inductance in gate return path. As illustrated in Fig. 4.3.6, the hardware prototype can achieve a maximum efficiency of 98.79% at 4.4A when hard-switching operation is applied and a 99.15% efficiency at 5A under soft-switching operation, which realises a 0.06% higher efficiency over advanced manufacturer-made counterparts [38].

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# Chapter 5: Protection Scheme for Normally-on WBG Device

Polarization super junction (PSJ) GaNFET is the main targeted device in this chapter. As aforementioned, the GaN HEMT is a naturally normally-on device. With regards to PSJ GaNFET, it makes use of super junction effect in AlGaN/GaN interface where the polarization effect function as super junction in Si MOSFET, which improves both breakdown voltage and conductivity of the PSJ GaNFET. Moreover, the normally-off operation of PSJ GaNFET can be obtained by the implementation of cascode structure [1]–[3]. Before moving forward, it is necessary to analyse PSJ GaNFET circuit performance in various conditions and environments. Therefore, a protection scheme is accordingly proposed in this chapter.

## 5.1: Normally-on PSJ GaN Device

With regards to PSJ, which consists of double hetero-junction GaN/AlGaN/GaN, high density positive and negative polarization charges induce two-dimensional electron gas (2DEG) and two-dimensional hole gas (2DHG) at hetero-interfaces as drawn in Fig. 5.1.1 [4]. The concept of PSJ is based on charge compensation among polarisation charges in the GaN hetero structure, which provides an alternative solution to obtain a flatten electric field and gets rid of field plates (FP) in conventional GaN HEMT. In a more specific term, a flat electric field distribution is achieved due to inherent positive and negative charge quantities balance each other, and eventually result in an enhanced breakdown voltage for a given drift region length as shown in Fig, 5.1.1(b) [4]–[6]. Consequently, the combination of PSJ and relatively high electric field result in PSJ GaN HFET become a very promising candidate for next-generation power semiconductor devices in the near future.

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| --- | --- |
|  |  |
| (a) | (b) |

71Figure 5.1.1: Device cross-section, simplified electric field distribution during OFF state and circuit model of (a) conventional GaN HEMT (with/without FP); (b) PSJ GaN HFET [4]

In contrast to e-mode GaN devices, d-mode GaN devices have lower on-resistance because the two-dimensional electron gas (2DEG) is induced at GaN/AlGaN interface. What is more, for a d-mode GaN device, the 2DEG does not have to be disrupted and re-created to turn on the device [7]. Hence, it is worthwhile to investigate and explore d-mode GaN devices to fully appreciate all of GaN’s benefits. However, the complexity of gate driver design result in a significant difficulty to the adoption of the d-mode GaN devices. There are innumerable studies have been conducted on the gate drive circuitry with protection scheme for normally-on device [8]–[11], where the response time that is required to clear the fault condition is insufficient to cope with the extremely fast WBG devices. This work proposes a gate drive circuitry design for normally-on GaN devices with effective protection in terms of the failure of negative gate voltage supply and the overcurrent/short-circuit event. Moreover, GaN devices realise the bidirectional current flow capability. Both the desaturation and negative power supply protection circuits are applied to a 1.2kV polarisation super-junction (PSJ) GaN FET [4][12][13]. Since 1.2kV PSJ GaN FETs have a limited current rating of 8A, a 650V/85A SiC JFET (UJ3N065025K3S) with an 85A maximum drain current rating is selected to validate the desaturation protection scheme for the higher current operation.

The 1.2kV PSJ GaN HFET (TO-247 package) designed by University of Sheffield and produced by Powdec is the main targeted device to investigate in this chapter. The current-voltage (IV) and capacitance-voltage (CV) characteristics of the 1.2kV GaN HFET is measured via Agilent B1505A device analyser as illustrated in Fig. 5.1.2. Accordingly, both IV and CV characteristics of 1.2kV GaN HFET are shown in Fig. 5.1.3.

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| 72Figure 5.1.2: Agilent B1505A device analyser mainframe with enclousre for device placement |

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|  |
| (a) |
|  |
| (b) |

73Figure 5.1.3: 1.2kV PSJ GaN HFET (a) IV characteristic; (b) CV characteristic

The bidirectional power switch (BPS) is very attractive in power converter applications, such as charger, battery [14][15]. Different from traditional Silicon IGBT-based bidirectional switching module, GaN devices are capable of bidirectional current flowing in nature, which allows the elimination of external antiparallel diodes [16]. In the meantime, GaN devices are able to offer better conduction efficiency owing to lower specific on-resistance ( and the absence of offset voltage in IGBT. Both traditional IGBT-based and GaN-based bi-directional switching module as shown in Fig. 5.1.4.

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| --- | --- |
|  |  |
| (a) | (b) |

74Figure 5.1.4: The schematic of bidirectional switching module using (a) IGBT-based; (b) GaNFET-based

## 5.2: Operation of Targeted Circuit

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| Bi-directional power switches (BPS) are very promising in power converters, such as voltage source inverters (VSI) [17][18], power storage units [19], direct and indirect matrix converters [20]–[22]. In order to fully making use of the superiority of PSJ GaN HFET in the applications that require bi-directional switching capability. It is necessary to work out a proper gate drive circuit with protection scheme for d-mode PSJ GaN HFET. Among these applications, one bridge of three-phase buck-boost current source inverter as illustrated in Fig. 5.2.1 has been selected for the investigation purpose. Fig. 5.2.2 shows the implementation of the protection circuit for PSJ GaN HFET-based converter in Cadence Orcad. The bidirectional switching module is formed by two-source connected PSJ GaN HFETs, upper bidirectional switching module is constructed with proposed protection scheme to evaluate the performance of both desaturation and negative power supply protection circuits. The normal operation of the one-phase bridge-leg as show in Fig. 5.2.3, including voltage of switching node (), output current () as well as gate signal with multi-step commutation strategy [20].    75Figure 5.2.1: The schematic of three-phase buck-boost current source inverter (CSI) systems [23] |

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| 76Figure 5.2.2: The implementation of the protection circuit for GaN-based bidirectional module |

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| --- | --- |
|  |  |
| (a) | (b) |
|  |  |
| (c) | (d) |
|  |  |
| (e) | (f) |

77Figure 5.2.3: The normal operation of one-phase half-bridge using 2-S connected bidirectional switching module @400V/10A (a) and versus time; (b) Zoom-in view of switching transition; (c) pattern of commutation strategy

## 5.3: Proposed Protection Scheme for d-mode WBG Device

It is important to understand the circuit performance of PSJ GaN HFET. Therefore, a proper protection scheme is highly desired to prevent, and clear fault events might occur during d-mode PSJ GaN HFET normal operation. The proposed protection scheme consists of two parts: one is used to protect the device from short-circuit and overcurrent event, namely desaturation scheme; another one is aimed to protect the negative voltage failure, so-called negative power supply protection scheme. This negative power supply is used to provide negative voltage for both desaturation circuit and the gate drive circuit. PSJ GaN HFET is the main target device, and a SiC JFET (UJ3N065025K3S) is selected to evaluate the proposed protection scheme for higher current operation.

### 5.3.1: Desaturation Circuit

The desaturation circuit is designed to against overcurrent and short-circuit event. The desaturation circuit should monitor the current level of the power devices and offer a protection mechanism when the power device being pulled out of its saturation region, which leads to an increase in drain-source voltage. Especially, WBG-based devices are different from Si-based devices due to the transition from ohmic to active region cannot be clearly defined. Moreover, the use of WBG-based power device requires better noise immunity of the desaturation to avert false triggering of the desaturation protection circuit. However, maintaining an ultra-fast response time is still essential of the desaturation circuit.

With respect to the proposed desaturation circuit, which can monitor drain-source voltage drop of the DUT, and only trigger the desaturation operation in DUT conduction period as shown in Fig. 5.3.1. During normal operation, the comparator () sends logic ‘0’ signal toward the opto-coupler. The opto-coupler therefore sends inverted logic ‘1’ as the ENABLE signal to the gate driver of the device. As a result, the device will follow the gate driving signal to turn on or off. Thanks to the combination of CMOS module and desaturation MOSFET (), the comparison between and via the comparator () only take place when the DUT is ON. Since, when the device is in OFF state, the MOSFET () is turned on and thereby the is pulled down to and always below . The high voltage diode with low voltage drop and fast recovery feature is aimed to monitor the drain current of the DUT. and perform as a RC low pass filter to stabilize the from noise. is set by the voltage divider constructed by two resistors, namely and . This reference voltage determines the limit of drain current (, and used to compare to . Thus, the comparator (in the desaturation circuit will produce the fault signal to opto-coupler and eventually pull-down the gate-to-source signal of the DUT. The most important object in this desaturation circuit is the response time between and . For instance, when has been pulled down to by gate driving signal, while the MOSFET ( is still turned-off, the is now equal to . This result in a fault triggering of the desaturation circuit. This time is defined by rises to the steady-state level at a time constant. Where R is formed by and , and C is formed by and the output capacitance of . Furthermore, by employing different resistor value in CMOS configuration can further amend the turn-on and turn-off time of the MOSFET (. The desired synchronisation of and can be achieved by the MOSFET ( with ultra-fast turn-on transition. The value of during conduction period can be expressed as equation 5.1.

(5.1)

|  |
| --- |
| Diagram, schematic  Description automatically generated |
| (a) |
|  |
| (b) |

78Figure 5.3.1: The proposed desaturation circuit for d-mode PSJ GaN HFET (a) circuit diagram; (b) implementation block diagram

The detailed operation of the desaturation circuit can be described as following. When overcurrent events take place, the will rise above . Then a fault signal (logic 1) will be triggered by comparator (), since the IN+ of comparator is now greater than IN-. This fault signal received by the opto-coupler, and it sends logic ‘0’ signal toward the gate driver of the device to turn off the device via an AND gate IC. It is necessary to emphasise that every BDS module protection circuit including both desaturation circuit and negative power supply protection circuit only require one AND gate IC due to BDS module is two-source connected. When the desaturation operation triggered, the MOSFET ( will be triggered ON as well. Once this MOSFET is turned-on, the gate driving signal of the device will be pulled down towards to turn the device off.

### 5.3.2: Negative Power Supply Protection Scheme

Regarding to negative power supply protection, this protection circuit is designed to protect the desaturation circuit as well as the negative gate voltage for gate driver. In case negative voltage supply used for desaturation circuit and gate driver failure. Therefore, the gate driver unable to turn-off the d-mode bidirectional switching module anymore since it cannot generate desired negative bias for switching-off the device. The detailed circuit of this negative power supply protection as illustrated in Fig. 5.3.2, and the operation of the proposed negative power supply protection scheme can be described as following. During normal operation, the MOSFET ( stays in OFF state. It is because the capacitor () is charged to via discharging diode (), and hereby the gate-to-source voltage is about zero during normal operation. Another comparator ( with collector output is employed to monitor the state of the negative power supply (). As shown in Fig. 5.3.2(a), the is connected to the positive input (IN+) of the comparator (. An adjustable potential divider formed by two resistors is used to set the reference voltage and connected to the negative input of the comparator (, and this reference voltage ( is below 0V. Since IN+ is lower than IN- in normal operation, the comparator sends logic ‘0’toward opto-coupler. Hence, the opto-coupler outputs logic ‘1’ to the AND gate. As shown in Fig. 5.3.2(b), each AND gate IC can in charge two devices or one bidirectional switching module. If both devices in bidirectional switching module working properly, in accordance with the truth table of AND logic, the AND gate IC will send logic ‘1’ as ENABLE signal toward gate driver of dc-link switch and thereby connect converter to the high voltage power supply. Compared to [10], the proposed protection circuit realises lower number of components at cost of increased power supply due to additional protection power supply (). Thanks to the two-source-connected method, each bidirectional switching module which consists of two discrete devices in this work only require the same number of power supply as single device.

|  |
| --- |
| Diagram, schematic  Description automatically generated |
| (a) |
|  |
| (b) |

79Figure 5.3.2: The proposed negative power supply protection scheme for d-mode device (a) circuit diagram; (b) implementation block diagram

When the negative power supply ( ) fail, the gate voltage of the negative power supply protection MOSFET ( rises towards zero. This leads to the gate-to-source voltage of the MOSFET ( become positive and therefore the MOSFET ( turns on. The Vgs of the DUT will be pulled down to negative value (), which is the voltage across the capacitor (. In the meantime, due to fail, the IN+ of comparator (become higher than IN- (. Consequently, the opto-coupler receives a logic 1 signal from comparator and it sends an inverted output (logic 0) signal to AND gate IC. Eventually, the dc-link control switch will be turned off and isolate the converter from high voltage power supply.

### 5.3.3: Simulation Set-up and Experimental Verification

Both simulation and experimental verification are conducted to access the performance of the proposed protection circuit for d-mode PSJ GaNFET. The simulation circuit as illustrated in 5.2.2 is constructed in Cadence Orcad, which comprises two bidirectional switching modules. **The overall simulation can be divided into following parts, namely, desaturation circuit and negative power supply protection circuit implementation. It is worth to point out that the SiC JFET (**UJ3N065025K3S) from United Silicon Carbide, Inc. has been selected to validate proposed desaturation scheme for higher current evaluation due to limited current rating of the PSJ GaN HFET**. Fig. 5.3.3(b) shows the schematic of the experimental verification circuit, which consists of a high-voltage DC source, an inductive load and two optional freewheeling SiC diodes (GB10MPS17-247). The optional freewheeling diodes are implemented for higher current testing when SiC JFETs are used. The fault signal is triggered by** C2000 Piccolo LaunchPad evaluation board with **Ti F28027F microcontroller as shown in Fig. 5.3.3(a). The experimental evaluation PCB is presented in Fig. 5.3.3(c). Fig. 5.3.4 depicts the IV-curves and selected forward operation points of the PSJ GaN HFET and SiC JFET used in this work, respectively. The gate-source voltage for both PSJ GaN HFET and SiC JFET is varied from**  to 0V, and [2V, 13A] and [1.4V, 60A] have been respectively selected as forward operation points based on their IV characteristics for PSJ GaN HFET and SiC JFET.

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| (a) |
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| (b) | |
|  | |
| (c) | |

80Figure 5.3.3: (a) fault signal triggered by Ti C2000 Piccolo Launchpad; (b) experimental set-up; (c) top view of the practical PCB

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| --- | --- |
|  |  |
| (a) | (b) |

81Figure 5.3.4: vs. characteristics and selected forward operation points of (a) PSJ GaN HFET; (b) SiC JFET [24]

**The key components and parameters used in proposed desaturation and negative power supply protection scheme as shown in Table 5.1 and Table 5.2 respectively.**

15**Table 5.1: Key components used in the proposed protection scheme**

|  |  |
| --- | --- |
| **Component** | **Model** |
| voltage regulator | ISA2415 |
| voltage regulator | ITQ2405SA |
|  | ES1A |
|  | BY203-20S |
|  | [EEEFT1V561AP](https://uk.farnell.com/panasonic/eeeft1v561ap/cap-560-f-35v-radial-smd/dp/1868420?iscrfnonsku=true&st=7296289) |
|  | LM311 |
| Opto-coupler | ACPL-H61L |
|  | IRF5305/IRLR2905 |
|  | IPD220N06L3 |
| dc-link switch | IXBF20N360 |
| dc-link switch gate driver | IX3120 |
| DUT/desaturation gate driver | Si8271 |

16**Table 5.2: Key parameters in the proposed protection scheme**

|  |  |
| --- | --- |
| **Parameter/unit** | **Value** |
| /Ω | 100 |
| /Ω | 220 |
| /F | 1500p |
| / Ω | 1 |
| / Ω | 500 |
| / Ω | 100 |
| /F | 560u |
| /Ω | 600/300 |
| /Ω | 500 |
| /Ω | 100 |
| /V | +5 |
| /V | ±15 |

In order to evaluate the performance of proposed desaturation circuit in Cadence Orcad, a fault signal is generated by lower switching module Sa in the one-phase half bridge converter in Cadence, whereas the upper switching module Sb is operating at 50kHz. With respect to experimental validation, this fault signal is triggered by upper device as shown in Fig. 5.3.3(a). The maximum current limit is set by two reference resistors ( and ) as previously mentioned. In this work, the PSJ GaN HFET based converter is operating at 600V/5A, and is set at 13A; the SiC JFFET-based converter is operating at 400V/25A, and 60A has been set as , corresponding with 2V and 1.4V drain-to-source voltage respectively according to their IV-curve as depicted in Fig. 5.3.4. In accordance with the equation (5.1), the as “IN-” of comparator is set to 4.167V of PSJ GaN HFET and 3.846V of SiC JFET. Table 5.3 s critical values in desaturation scheme, including overcurrent limit (), reference voltage of the comparator (), change in sensing voltage when faults occur (). The CMOS configuration within desaturation scheme ensures that the comparison of the comparator between and only take place when DUT is ON-state, since when DUT is off, the value of is pulled down towards . It is because when DUT under normal operation, always below . The fault signal results in an increase of due to the voltage drop across the device is increased in line with its IV characteristics. Therefore, a logic LOW signal is yielded by desaturation circuit to turn-off the DUT. The triggering of fault signal eventually leads to the desaturation circuit stops gating signal due to is forcedly applied to gate-source terminal of the DUT.

17**Table 5.3: Critical values of desaturation circuit**

|  |  |  |
| --- | --- | --- |
| **Objective/unit** | **PSJ GaN HFET** | **SiC JFET** |
| / Ω | 200 | 300 |
| / Ω | 1000 | 1000 |
| / A | 13 | 60 |
| /V | 4.167 | 3.846 |
| /V | 2.48 | 2.02 |
| Response time ()/ns | 321 | 290 |
| Detect time (/ns | 20 | 40.6 |

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| --- | --- |
|  | Chart, line chart  Description automatically generated |
|  |  |
|  |  |
| (a) | (b) |

82Figure 5.3.5: Comparison of simulation and experimental result of proposed desaturation scheme of (a) PSJ GaN HFET drain current, zoom-in view of drain current and corresponding Vdesat; (b) SiC JFET drain current, zoom-in view of drain current and corresponding Vdesat

The response time ( of this desaturation circuit is determined by the time from the instant of the drain current exceeds the specified limitation of the drain current () to the fault event is cleared by the desaturation circuit. As shown in Fig. 5.3.5(b) and (e), the overcurrent event lasts for 341ns of PSJ GaN HFET and 330.6ns of SiC JFET. A maximum 38A drain current is observed within desaturation period for PSJ GaN HFET. With regards to SiC JFET, a maximum 92.1A drain current is reached within this period. Meanwhile, Fig. 5.3.5(c) shows the proposed desaturation circuit only requires tens of nanoseconds ( upon the setting and devices’ characteristics to detect the fault event, which saves more than 2.9us in comparison to the desaturation scheme proposed in [10]. It is worth pointing out that the response time of the proposed desaturation circuit is much lower than the 5us which is the common minimum requirement of short circuit capability for WBG device [25]. As a result, the proposed desaturation circuit is able to detect and clear faults within 341ns, which shows significant advancement in comparison with that of [10]. The proposed desaturation scheme demonstrates not only a fast response time to clear overcurrent event, but also a ultra-fast detection time, which is also the major improvement compared to [10]. Moreover, there is no significant ringing observed in Vdesat waveform during normal conduction period, which states the proposed desaturation circuit exhibit a strong noise immunity. The proposed desaturation scheme presents a shorter time to clear desaturation condition in comparison to that of the state-of-the-art integrated gate driver with built-in desaturation protection as indicated in Fig. 5.3.6 [26]. What is more, by using advanced gate driver IC, it has a 400ns response to clear the overcurrent event, while the proposed desaturation scheme is able to wipe out the overcurrent event within 342ns, which shows a significant improvement from desaturation response time perspective. Lastly, the proposed desaturation scheme can be further modified and implemented in normally-off devices. The main difference of the desaturation scheme between normally-on and normally-off device is the gate driving voltage range, since a normally-on device always require a sufficient negative bias to switch-off, which makes gate drive circuitry design as well as protection scheme become more complex and sophisticated; while a normally-off device only need ‘zero’ to keep device off and a positive bias to turn-on.

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83Figure 5.3.6: Si828x series integrated gate driver desaturation detector parameters [26]

In order to evaluate the performance of proposed negative supply protection circuit scheme in Fig. 5.3.2, the failure of negative power supply for gate drive is caused by turning off the supporting gate drive power supply during PSJ GaN HEFT operating at 50kHz frequency. Fig. 5.3.7 illustrates the response of negative power supply protection circuit. React time and time frame are the two critical objectives in the proposed negative power supply protection scheme. The react time is defined by how quick the DUT is switched-off by the negative power supply protection scheme. The time frame describes the allowed time for the converter is isolated from its main source after the proposed negative power supply protection circuit pull-down the gate signal of the device.

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|  |
| (a) |
|  |
| (b) |

84Figure 5.3.7: The proposed negative power supply protection result (a) time frame; (b) zoom-in view of and

As shown in Fig. 5.3.7(a), once negative voltage supply failure, the of DUT will be accordingly pulled down toward within 0.12us. It is because the reservoir capacitor () is previously charged to via diode () during normal operation. An EN signal is simultaneously generated by negative power supply protection circuit and sends to gate driver IC of the dc-link switch. This EN signal commands dc-link switch to be turned off and isolates the converter from its high voltage source. The proposed negative supply protection scheme keeps the converter in off state for 60.5ms as illustrated in Fig. 5.3.7(b), which is sufficient to isolate the converter from high voltage power supply via the dc-link control switch. A longer isolation time can be achieved by increasing the capacitance of due to the of the DUT follows the discharge curve as depicted in Fig. 5.3.7(a).

In conclusion, an ultra-fast protection scheme is proposed, which consists of two parts, namely, desaturation circuit and negative gate voltage protection. The key to the d-mode device gate drive design is the negative supply and overcurrent protection, due to the safety concern for d-mode devices when a failure happens in power conversion applications. This work evaluates specific requirement of d-mode devices, such as the isolated negative power supply and short-circuit protection. Normally-on d-mode GaN devices have lower on-resistance and minimal dead time in comparison with enhancement-mode (e-mode) GaN devices, which can further reduce the switching loss and conduction loss. Cadence Orcad is used to evaluate the proposed protection scheme under simulation environment. Moreover, an experimental prototype is made for experimental verification purpose. With respect to the performance of proposed protection scheme, the overcurrent event can be removed in a very short time, 341ns of PSJ GaN HFET at 600V/5A operation and 330.6ns for SiC JFET at 400V/25A operation. On the other hand, the negative gate voltage protection circuit is able to offer 60.5ms time frame, which can be easily adjust by either capacitance of or operation frequency. The time frame provided by negative gate voltage protection circuit is aimed to offer sufficient time to command isolation of one-phase half bridge converter from high DC supply voltage.

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# Chapter 6: Conclusion and Future Work

## 6.1: Conclusion

The WBG-based devices have demonstrated their superiority and advancement in comparison to Si-based counterparts. Therefore, this work is mainly forced on the development and investigation on GaN-based devices and related applications. Both key findings and contributions of this work are summarised in this chapter.

### 6.1.1: Switching Characteristics of Cascode GaNFET

The differences between e-mode GaNFET and cascode GaNFET are addressed in this work. The switching characteristics of the cascode GaNFET is studied, including the analysis of switching transients, parasitic effect as well as the challenges faced by cascode GaN devices. Spice-based simulation models are modified by author based on experimental measurement to evaluate the switching performance of cascode GaNFET. Proper simulation combined with experimental validation, which helps to analyse the switching behaviour of the cascode GaNFET and consolidate the understanding of the impact of parasitic elements. Practical PCBs are made to experimentally access the switching performance with different gate driving loop design and identify the potential challenges of cascode GaNFET.

### 6.1.2: Cascode GaN Gate Drive Design Consideration

This work evaluates the influence of gate drive circuitry to cascode GaN device’s switching waveforms. This is done by comparing three PCBs using double-pulse-test (DPT) with different gate driving loop design. Among important parasitic elements, source-side inductance shows a significant impact to gate-source voltage waveform. A simulation model based on experimental measurement of the cascode GaNFET used in this work is modified by author. The simulation model is implemented in a synchronous buck converter topology with different gate driving loop design and hereby to assess the impact of gate driving loop of cascode GaN device in both continuous conduction mode (CCM) and critical conduction mode (CRM). Apart from simulation, a synchronous buck converter prototype with proposed gate driving loop design is presented for experimental evaluation, which shows a 99.15% efficiency at 5A under soft-switching operation (CRM) with a 59ns dead time.

### 6.1.3: Protection Scheme for WBG d-mode Device

The key for the d-mode device gate drive design is the negative supply and overcurrent protection since the safety concern for all kinds of d-mode device in power conversion applications. This work evaluates the specific requirement of d-mode device, such as isolated negative power supply and short-circuit protection. Since GaN HEMT is a naturally normally-on device, utilizing d-mode GaN device can make use of all advantages that GaN material brings. With proper management, the d-mode GaN device is able to overcome the major drawbacks of e-mode GaN device. Natural d-mode GaN device realises an even smaller on-resistance and a minimal dead time, which can further achieve smaller switching loss and conduction loss. Both simulation and experimental verification are conducted in this work to evaluate the performance of the proposed protection scheme. The proposed desaturation scheme can wipe out the overcurrent event within 341ns. On the other hand, the proposed negative power supply scheme can offer 60.5ms time frame, which provides sufficient action time for users.

## 6.2: Future Work and Research Opportunities

The emerging GaN-based power devices have drawn international attention and show a very promising future in power electronics field. Therefore, further research and opportunities can be described as following:

1. Further improvement in cascode GaNFET can be achieved by replacing a LV Si MOSFET with lower input capacitance. Parasitic inductance in gate return loop is considered as the most significant source to cause gate-source voltage oscillation for cascode GaNFET. Once the gate return loop is carefully designed, the cascode GaNFET no longer requires that high input capacitance to prevent false triggering caused by massive high-frequency gate-source voltage oscillation. In addition, the relatively slower switching speed of cascode GaNFET is considered as the most crucial disadvantage in comparison to that of e-mode GaNFET. With lower input capacitance, the switching speed as well as maximum allowed switching frequency can be improved. Therefore, a cascode GaNFET prototype with lower input capacitance can be made further to verify this assumption. Moreover, the further research should involve LV Si MOSFET section as mentioned in Chapter 3, which is related to input capacitance and conduction loss/junction temperatures.

2. The impact of gate driving loop to cascode GaN-based converter was evaluated at 100 kHz, which is relatively conservative considering the potential of cascode GaNFET used in this work. 100 kHz is a reasonable starting point for this research in accordance with industrial-made counterparts. Further assessment and investigation can be made by varying switching frequency, and it could be systematically evaluated from converter loss, passive elements size, EMI filter, thermal management perspectives.

3. The performance of the proposed protection scheme for d-mode WBG devices was evaluated at 400V and 600V level in this work. It is possible to build a buck converter based on current PCB to check the efficiency of the PSJ GaN HFET-based converter with the proposed protection circuit to identify the major trade-off between protection circuit and efficiency of the converter in system level. In addition, the proposed protection could be implemented with another kind of PSJ GaN HFET, which is rated at 3kV, to evaluate its performance under higher voltage condition.

4. A novel cascode PSJ GaN HFET can be fabricated further to explore the potential of high voltage PSJ GaN HFET with normally-off operation. Both the impact of gate driving loop and parasitic effect of cascode PSJ GaN HFET can be evaluated via similar approaches proposed in this work. The cascode PSJ GaN HFET is expected to achieve higher breakdown voltage and therefore making GaN-based power devices become more competitive in various power electronic applications.

# Appendix:

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| (b) |
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| (c) |

85Figure A.1: Depletion mode device capacitance-voltage measurement setup using Agilent B1505A of (a) Coss; (b) Crss; (c) Ciss [1]

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| (a) |
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| (b) |

86Figure A.2: (a) practical view of 1.2kV PSJ GaNFET mounted on DBC structure; (b) practical view of 1.2kV PSJ GaNFET in TO-247 package

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87Figure A.3: The schematic of normally-on WBG device protection scheme

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| (a) |
|  |
| (b) |

88Figure A.4: Normally-on WBG device protection PCB layout (a) top layer + inner layer1; (b) bottom layer + inner layer 2

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89Figure A.5: DPT signal generated by Matlab Simulink (adds-on package: Embedded Coder Support Package for Texas Instruments C2000 Processors)

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90Figure A.6: Fault signal generated by Matlab Simulink (adds-on package: Embedded Coder Support Package for Texas Instruments C2000 Processors)

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